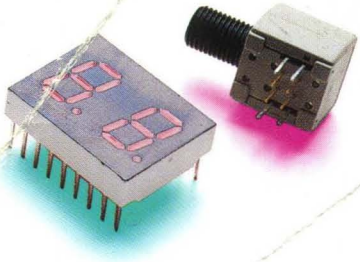
HEWLETT PACKARD

Optoelectronics Designer's Catalog



HEWLETT® PACKARD

Hewlett-Packard Company
321 East Evelyn Avenue, MS 330B21
Mountain View, California 94039

415/694-2280
or 800/235-0312
Voice Mail 415/694-2400 Ext. 2280
Fax 415/694-2589

HEWLETT PACKARD

Hewlett-Packard: A Leader in Components

A Brief Sketch

Headquartered in San Jose, California the Hewlett-Packard Components Group is a leading supplier of components for the wireless and fiber-optic communications, computer equipment, industrial and automotive markets. Included in the Components Group's extensive line of more than 9,000 components are RF and microwave semiconductors, fiber-optic transmitters and receivers, LEDs, motion control devices, optocouplers, solid-state relays, bar-code scanners, and millimeter-wave subassemblies.

Founded more than thirty years ago, the Components Group has evolved into a global manufacturer of microwave, RF, high-speed digital and electro-optical semiconductors, components and integrated subsystems. Today the group has 7,600 employees and projected revenues for 1993 of $650 million.

The Components Group markets products through a sales force of 300 technically-educated sales professionals located in 20 countries. An additional 30 distributors sell products worldwide.

The Components Group maintains five marketing centers worldwide in San Jose, California; Boeblingen, Germany; Tokyo, Japan; Frimley, U.K.; and Singapore. Each is fully staffed with product application and support engineers and each is responsible for regional decision making. In 1991 the Components Group opened a Design Center in Tokyo, specifically chartered to develop products for the Japanese market.

Local decision-making is central of HP's transnational business strategy which focuses on customer satisfaction. In addition to providing the right product with superior quality and reliability, the Components Group strives to ensure worldwide product availability, accurate on-time delivery and up-to-date technical information for its customers.

Quality and Reliability

Quality and reliability are very important concepts to Hewlett-Packard in maintaining the commitment to product performance.

At Hewlett-Packard, quality is integral to product development, manufacturing, and final introduction. "Parts per million" (PPM), as a measure of quality, is used in HP's definition of product assurance. And HP's commitment to quality means that there is a continuous process of improvement and tightening of quality standards. Manufacturing quality circles and quality testing programs are important ingredients in HP products.

Reliability testing is also required for the introduction of new HP components. Lifespan calculations in "mean-time-between-failure" (MTBF) terms are published and available as reliability data sheets. HP's stringent reliability testing assures long component lifetimes and consistent product performance.

The body of this book is printed on recycled paper.

HEWLETT PACKARD

About This Catalog

To help you choose and design with Hewlett-Packard optoelectronic components, this catalog includes detailed specifications for HP component products. The catalog is divided into nine sections:

1. Motion Sensing and Encoder Products
2. LED Light Bars and Bar Graph Arrays
3. LED Lamps
4. LED Displays
5. Fiber Optics
6. Optocouplers
7. Bar Code Components
8. Applications
9. Appendix

How to Find the Right Information

- The table of Contents (p. iii) helps you to locate the product sections as well as the selection guides for each of the product sections.
- The Alphanumeric Index (p. iv) lists every component represented in this catalog.
- Selection guides at the beginning of each of the seven product sections, contain basic product specifications which allows you to quickly select products most suitable for your application.

Following the product sections is a complete listing of application bulletins and notes which are frequently useful as design aids. The final section is an appendix containing HP sales, service, and authorized distributor locations.

How to Order

To order any component in this catalog or additional applications information, call the HP office nearest you and ask for a Components representative. A complete listing of the U.S. sales offices is on page 9-10; offices located outside of the U.S. are listed on page 9-11.

A worldwide listing of HP authorized distributors is on page 9-3. These distributors can offer off-the-shelf delivery for most HP components.

HEWLETT PACKARD

Contents

HEWLETT PACKARD

Alphanumeric Index

Bold = New Product

Note: Standard Options Available (see page xix).

Bold = New Product

Note: Standard Options Available (see page xix).

Bold = New Product

Note: Standard Options Available (see page xix).

Bold = New Product

Note: Standard Options Available (see page xix).

Bold = New Product

Note: Standard Options Available (see page xix).

Bold = New Product

Note: Standard Options Available (see page xix).

Bold = New Product

Note: Standard Options Available (see page xix).

Bold = New Product

Note: Standard Options Available (see page xix).

Bold = New Product

Note: Standard Options Available (see page xix).

Bold = New Product

Note: Standard Options Available (see page xix).

Bold = New Product

Note: Standard Options Available (see page xix).

Bold = New Product

Note: Standard Options Available (see page xix).

Bold = New Product

Note: Standard Options Available (see page xix).

Bold = New Product

Note: Standard Options Available (see page xix).

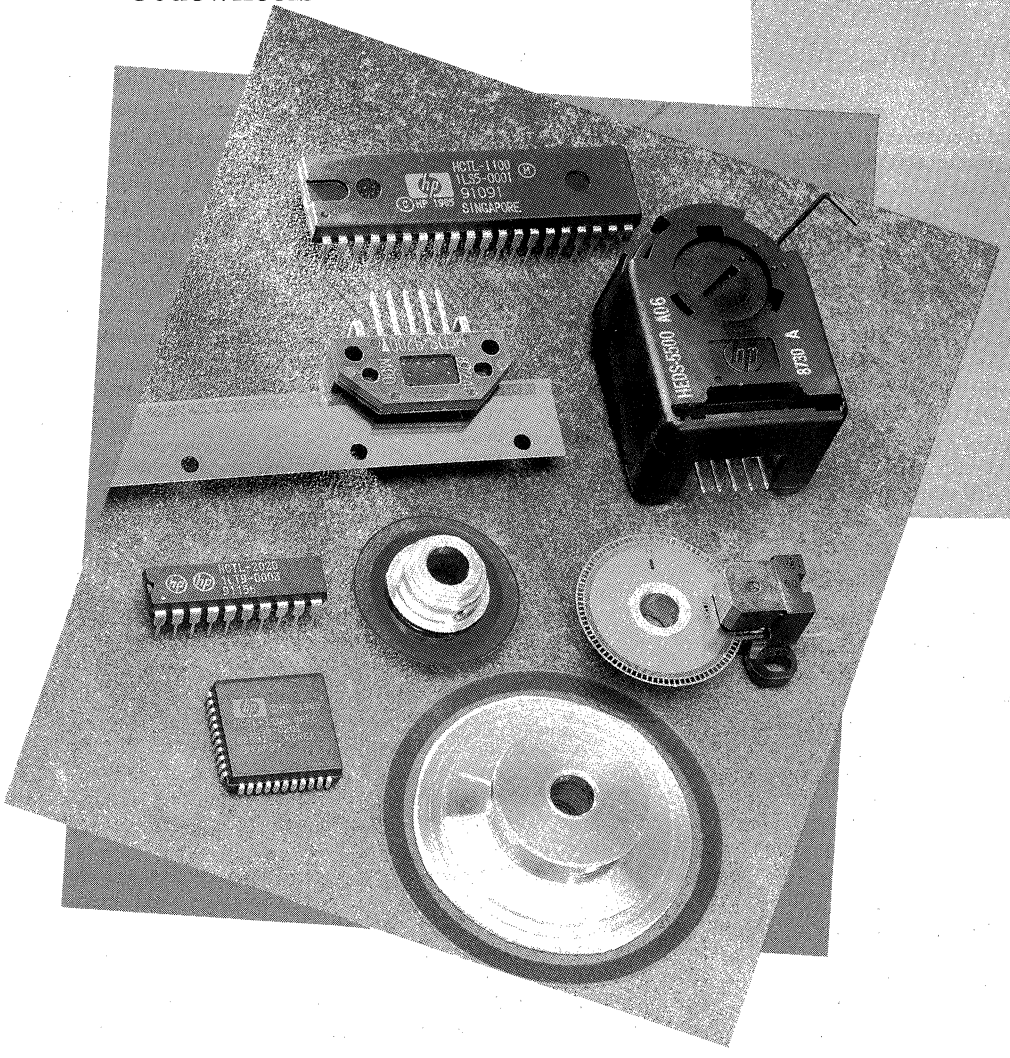
Bold = New Product

Note: Standard Options Available (see page xix).

HEWLETT PACKARD

Motion Sensing and Control

- Optical Encoder Modules
- Optical Encoders
- Rotary Pulse Generators
- Motion Control ICs
- Codewheels



HEWLETT PACKARD

Motion Sensing and Control

Motion Sensing and Control

Hewlett-Packard's growing family of motion sensing and control products developed as an extension of our emitter/detector systems capabilities. Motion sensing products include optical shaft encoders and optical encoder modules for closed-loop servo applications, and rotary pulse generators for manual input applications. HP's optical products provide digital link converting mechanical shaft rotation into digital signals. HP's motion control ICs complement the optical products and greatly simplify the design of digital motion control systems.

Our HEDS-9000, HEDS-9100, HEDS-9200, and HEDS-9700 series optical encoder modules provide sophisticated motion detection at a low price, making them ideal for high volume applications such as a printers, plotters, and industrial automation equipment. The HEDS-9000 and HEDS-9100 are now available in three channel versions, the HEDS-9040 and 9140, which provide a third channel index pulse in addition to the standard two channel outputs. The HEDS-9200 series linear encoder module uses the same emitter/detector technology as the HEDS-9000 to sense linear position. We have also increased the resolution performance of the HEDS-9000/9100/9200 to nearly twice the previous limit. The HEDS-9700 comes in a super small, wavesolderable package with a variety of mounting options.

The HEDS-5500 and HEDS-5600 series are complete, quick assembly, low cost optical shaft encoders. No adhesives or last minute adjustments are necessary for assembly. In addition, the HEDS-5540 and HEDS-5640 provide a third channel index pulse for home position sensing. The HEDS-5500 and 5600 series encoders offer a complete solution in industrial, medical, and office automation equipment.

For applications in noisy environments, line driver options are available on both the HEDS-9001/9100/9200 series module encoders, as well as the HEDS-5500/5600 encoder kits.

Hewlett-Packard's HRPG series of low cost miniature rotary pulse generators (RPGs) use reflective optics technology for superior reliability and consistent rotational feel for more than 1 million revolutions. The HRPG is ideal for front panel applications such as test and measurement equipment, medical equipment, CAD/CAM systems, and audio/video equipment. The HRPG is available in a variety of configurations including smooth or detented turning, multiple terminations and mounting options, and a wide selection of shaft configurations.

To complement the motion sensing products, HP offers two motion control IC family of products. The HCTL-1100 CMOS general purpose motion control IC performs all of the time-intensive tasks of digital motion control. The HCTL-1100 controls position or velocity while using an incremental encoder for feedback information. The HCTL-1100 is also available in a surface mount package. The HCTL-2000, HCTL-2016, and HCTL-2020 Quadrature Decoder/Counter ICs provide a one chip, easy to implement solution to interfacing the quadrature output of an encoder or RPG to a microprocessor. These CMOS ICs include a quadrature decoder, a 12 or 16 bit up/down

counter, and an 8 bit bus interface. In addition, the HCTL-2020 has cascade output signals as well as quadrature decoder output signals. The HCTL-2016 and HCTL-2020 are also available in surface mount packages.

New Products

Encoder Line Driver Options, HEDL-90XX/91XX/92XX

Now most of HP's Encoder Kits and Encoder Modules have Line Driver options available! The base parts are the HEDS-55XX and HEDS-9000/9100/9200.

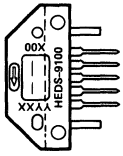
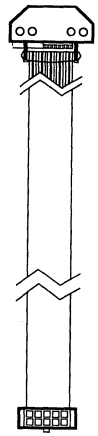
Extended Resolution Encoder Modules, HEDS-9000/9100

New, higher resolution encoder modules available up to 1024 CPR on a 11mm Rop, or up to 1024 CPR on a 23mm Rop.

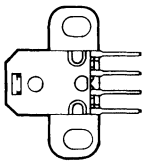
High Resolution Codewheels,HEDM/HEDG-5120/6120.

These new codewheels are designed to work with the High Resolution Encoder Modules and are available in film and glass to meet your specific environmental needs.

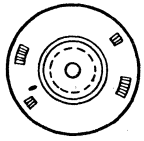
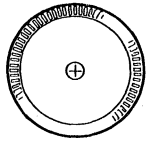
Optical Encoder Modules

Package Outline Drawing	Part No.	Channels	Resolution	Page No.
 HEDS-90XX HEDS-91XX HEDS-92XX	HEDS-9000 OPT□ 00	A, B	□ A 500 CPR B 1000 CPR	1-22
	New HEDS-9000 Extended Resolution OPT□ 00		□ T 2000 CPR U 2048 CPR	1-13
	New HEDL-9000 OPT□ 00		□ ALL	1-73
	HEDS-9040 OPT□ 00	A, B, I	□ B 1000 CPR	1-32
	New HEDL-9040 OPT□ 00		J 1024 CPR	1-73
	HEDS-9100 OPT□ 00	A, B	□ K 96 CPR B 1000 CPR C 100 CPR J 1024 CPR	1-22
 HEDL-90XX HEDL-91XX HEDL-92XX	New HEDL-9100 OPT□ 00		D 192 CPR E 200 CPR F 256 CPR G 360 CPR H 400 CPR A 500 CPR I 512 CPR	1-73
	HEDS-9140 OPT□ 00	A, B, I	□ C 100 CPR E 200 CPR	1-32
	New HEDL-9140 OPT□ 00		F 256 CPR G 360 CPR H 400 CPR A 500 CPR I 512 CPR	1-73
	HEDS-9200 OPT□ 00	A, B	□□□ □□□ L00 120 LPI 300 300 CPI M00 127 LPI 360 360 CPI	1-28
	New HEDL-9200 OPT□ 00		P00 150 LPI Q00 180 LPI R00 200 LPI	1-73

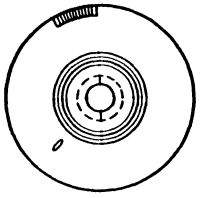
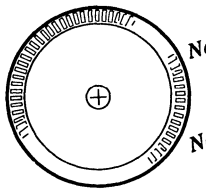
Small Optical Encoder Modules – HEDS-9700 Series

Package Outline Drawing	Part No.	Lead Bend	Channels	Resolution	Mounting Options	Page No.
	HEDS-9700 OPT [1][2][2]	Straight	A, B	[1] K 96 CPR C 100 CPR	[2][2] 50 – Standard 51 – Rounded Outline	1-41
	HEDS-9701 OPT [1][2][2]	Bent	A, B	D 192 CPR E 200 CPR F 256 CPR G 360 CPR H 400 CPR	52 – Backplane 53 – Standard w/Posts 54 – Tabless 55 – Backplane w/Posts	
	HEDS-9720 OPT [3][2][2]	Straight	A, B	[3] L 120 LPI M 127 LPI		
	HEDS-9721 OPT [3][2][2]	Bent	A, B	P 150 LPI		

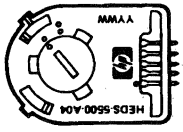
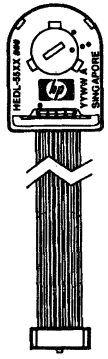
Codewheels – 11.00 mm (0.433 in) Optical Radius

Package Outline Drawing	Part No.	Matching Encoder Module	Channels	Resolution	Shaft Size	Page No.
	HEDS-5120 OPT [1][2][2]	HEDS-9100 HEDS-9700	A, B	[1] K 96 CPR C 100 CPR D 192 CPR E 200 CPR F 256 CPR G 360 CPR H 400 CPR A 500 CPR I 512 CPR	[2][2] 01 2 mm 02 3 mm 03 1/8 in. 04 5/32 in. 05 3/16 in. 06 1/4 in. 11 4 mm 14 5 mm 12 6 mm 13 8 mm	1-51
	HEDS-5140 OPT [3][2][2]	HEDS-9140	A, B, I	[3] C 100 CPR E 200 CPR F 256 CPR G 360 CPR H 400 CPR A 500 CPR I 512 CPR		
	*New* HEDM-5120 OPT [4][2][2] *New* HEDG-5120 OPT [4][2][2]	HEDS-9100 Extended Resolution	A, B	[4] B 1000 CPR J 1024 CPR		

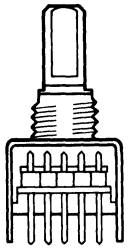
Codewheels – 23.36 mm (0.920 in) Optical Radius

Package Outline Drawing	Part No.	Matching Encoder Module	Channels	Resolution	Shaft Size	Page No.
	HEDS-6100 OPT [1][2][2]	HEDS-9000	A, B	[1] D 192 CPR E 200 CPR H 400 CPR A 500 CPR I 512 CPR B 1000 CPR J 1024 CPR	[2][2] 03 1/8 in. 06 1/4 in. 07 5/16 mm 08 3/8 mm 09 1/2 in. 10 54/8 in. 11 4 mm 12 6 mm 13 8 mm	1-51
	HEDS-6140 OPT [3][2][2]	HEDS-9040	A, B, I	[3] B 1000 CPR J 1024 CPR		
 New	HEDM-6120 OPT [4][2][2]	HEDS-9000 Extended Resolution	A, B	[4] T 2000 CPR U 2048 CPR		
New	HEDG-6120 OPT [4][2][2]					

Quick Assembly Encoder – HEDS-5500 Series

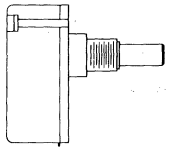
Package Outline Drawing	Part No.	Channels	Mounting Type	Through Hole	Resolution	Shaft Size	Page No.
 HEDS-55XX HEDS-56XX HEDM-550X HEDM-560X  HEDL-55XX HEDL-56XX	HEDS-5500 HEDL-5500 OPT [1][2][2]	A, B	Standard	None	[1] K 96 CPR C 100 CPR	[2][2] 01 2 mm 02 3 mm	1-61 1-73
	HEDS-5505 HEDL-5505 OPT [1][2][2]	A, B	Standard	8.9 mm (0.35 in.)	D 192 CPR E 200 CPR	03 1/8 in. 04 5/32 in.	1-61 1-73
	HEDS-5600 HEDL-5600 OPT [1][2][2]	A, B	External Mounting Ears	None	F 256 CPR G 360 CPR	05 3/16 in. 06 1/4 in.	1-61 1-73
	HEDS-5605 HEDL-5605 OPT [1][2][2]	A, B	External Mounting Ears	8.9 mm (0.35 in.)	H 400 CPR A 500 CPR I 512 CPR	11 4 mm 14 5 mm 12 6 mm 13 8 mm	1-61 1-73
	HEDS-5540 HEDL-5540 OPT [3][2][2]	A, B, I	Standard	None	[3] L 100 CPR E 200 CPR		1-61 1-73
	HEDS-5545 HEDL-5545 OPT [3][2][2]	A, B, I	Standard	8.9 mm (0.35 in.)	F 256 CPR G 360 CPR		1-61 1-73
	HEDS-5640 HEDL-5640 OPT [3][2][2]	A, B, I	External Mounting Ears	None	H 400 CPR A 500 CPR		1-61 1-73
	HEDS-5645 HEDL-5645 OPT [3][2][2]	A, B, I	External Mounting Ears	8.9 mm (0.35 in.)	I 512 CPR		1-61 1-73
	HEDM-5500 OPT [4][2][2]	A, B	Standard	None	B 1000 CPR		1-61
	HEDM-5505 OPT [4][2][2]	A, B	Standard	8.9 mm (0.35 in.)	J 1024 CPR		
	HEDM-5600 OPT [4][2][2]	A, B	External Mounting Ears	None			
	HEDM-5605 OPT [4][2][2]	A, B	External Mounting Ears	8.9 mm (0.35 in.)			

Rotary Pulse Generator – HRPG Series

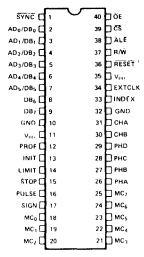
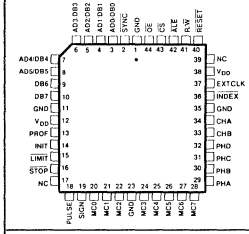
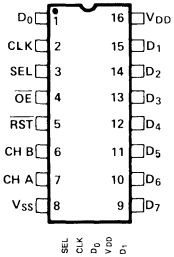
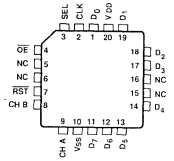
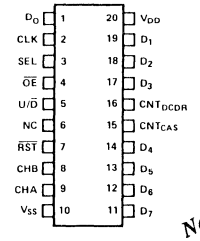
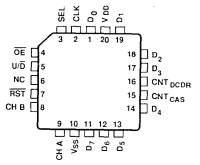
Package Outline Drawing	Part No.	Shaft Feel/ Resolution*	Mechanical Configuration	Termination	Page No.
	HRPG- A[1][1][1] OPT [2][2][3]	[1][1][1] S16 – Smooth 16 CPR D16 – Detented 16 CPR S 32 – Smooth 32 CPR D32 – Detented 32 CPR S64 – Smooth 64 CPR SCA – Smooth 120 CPR	[2][2] 11 – 0.3" x 0.25" 13 – 0.3" x 0.25" D-cut 14 – 0.5" x 0.25" 16 – 0.5" x 0.25" D-cut 17 – 0.8" x 0.25" 19 – 0.8" x 0.25" D-cut 51 – 7.6 mm x 6 mm 53 – 7.6 mm x 6 mm D-cut 54 – 12.7 mm x 6 mm 56 – 12.7 mm x 6 mm D-cut 57 – 20.3 mm x 6 mm 59 – 20.3 mm x 6 mm D-cut	[3] F – Pins Front with Bracket R – Pins Rear with Bracket C – Cable Connector with Strain Relief	1-76

*When ordering detented versions, a D-cut shaft is recommended.

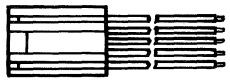
Rotary Pulse Generator – HEDS-5700

Package Outline Drawing	Part No.	Termination	Resolution	Drag Option	Shaft Configuration	Page No.
			[1]	[2]	[3]	1-84
	HEDS-5700	Pins	K 96 CPR	0 – free spinning	0 – 0.25" dia	
	OPT [1][2][3]		C 100 CPR	1 – static drag	1 – 6 mm dia	
	HEDS-5701	6" Color Coded Leads	D 192 CPR		2 – 0.25" dia D-cut	
	OPT [1][2][3]		E 200 CPR			
			F 256 CPR			
			G 360 CPR			
			H 400 CPR			
			A 500 CPR			
			I 512 CPR			

Motion Control ICS – HCTL-XXXX Series

Package Outline Drawing	Part No.	Package	Description	Page No.
	HCTL-1100	PDIP	CMOS General Purpose Motion Control IC	1-104
	HCTL-1100 OPT PLC	PLCC	CMOS General Purpose Motion Control IC	
	HCTL-2000	PDIP	CMOS Quadrature Decoder/Counter IC, 12-bit Counter	1-86
	HCTL-2016	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	
	*New* HCTL-2016 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	1-102
	HCTL-2020	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-86
	*New* HCTL-2020 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-102

Accessories for Encoders and Encoder Modules

Package Outline Drawing	Part No.	Description	Page No.
	HEDS-8902	4-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5500 and HEDS-5600 2 channel encoders. Also fits HEDS-9000, HEDS-9100, and HEDS-9200 2 channel encoder modules.	1-61 1-22 1-28
	HEDS-8903	5-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5540 and HEDS-5640 three channel encoders. Also fits HEDS-9040 and HEDS-9140 three channel encoder modules.	1-61 1-32
	HEDS-8905	Alignment Tool for HEDS-9140	1-32
	HEDS-8906	Alignment Tool for HEDS-9040	1-32
	HEDS-8901	Gap Setting shown for film codewheels	1-51
	HEDS-8932	Gap Setting shown for glass codewheels	1-51
	HEDS-8910 OPT 0 □□	Alignment Tool for HEDS-5540/5545 and HEDS-5640/5645. Order in appropriate shaft size.	1-61

HEWLETT PACKARD

New

Two Channel High Resolution Optical Incremental Encoder Modules

Technical Data

HEDS-9000/9100/9200 Extended Resolution Series

Features

- **High Resolution: Up to 2048 Cycles per Revolution**
- **Up to 8192 Counts per Revolution with 4X Decoding**
- **Two Channel Quadrature Output**
- **Low Cost**
- **Easy to Mount**
- **No Signal Adjustment Required**
- **Small Size**
- **-40°C to 100°C Operating Temperature**
- **TTL Compatible**
- **Single 5 V Supply**

Description

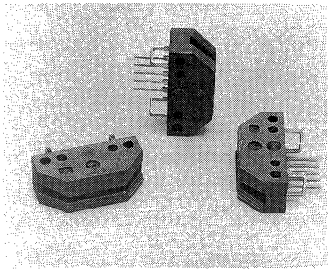
The HEDS-9000 Options T and U and the HEDS-9100 Options B and J are high resolution two channel rotary incremental encoder modules. These options are an extension of our popular HEDS-9000 and HEDS-9100 series. When used with a codewheel, these modules detect relative rotary position. The HEDS-9200 Option 300 and 360 are high resolution linear encoder modules. When used with a codestrip, these modules detect relative linear position.

These modules consist of a lensed Light Emitting Diode (LED) source and detector IC enclosed in a small C shaped plastic package. Due to a highly collimated light source and unique photodetector array, these modules provide a highly reliable quadrature output.

The HEDS-9000 and HEDS-9100 are designed for use with codewheels which have an optical radius of 23.36 mm and 11 mm respectively. The HEDS-9200 is designed for use with a linear codestrip.

These components produce a two channel quadrature output which can be accessed through five 0.025 inch square pins located on 0.1 inch centers.

The resolution of the HEDS-9000 Options T and U are 2000 and 2048 counts per revolution respectively. The HEDS-9100 Options B and J are 1000 and



1024 counts per revolution respectively. The HEDS-9200 Option 300 and 360 linear encoder modules have resolutions of 300 and 360 lines per inch.

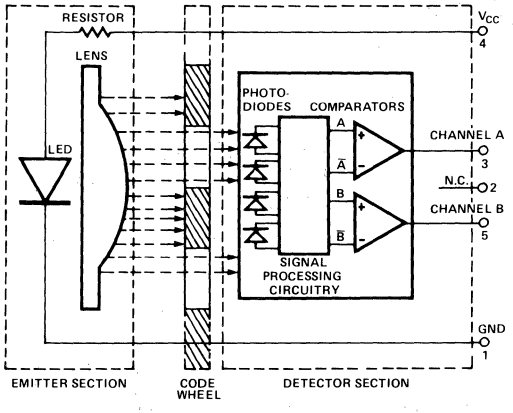
Consult local Hewlett-Packard sales representatives for other resolutions.

Theory of Operation

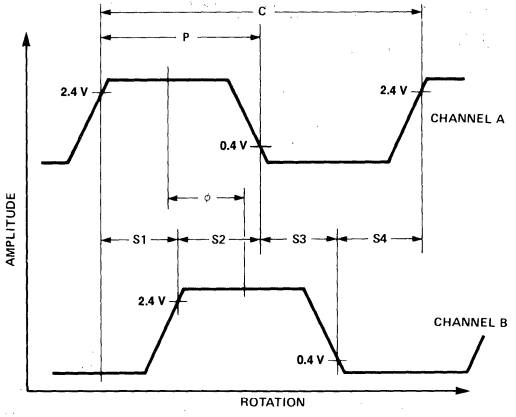
The diagram shown on the following page is a block diagram of the encoder module. As seen in this block diagram, the module contains a single LED as its light source. The light is collimated into a parallel beam by means of a single polycarbonate lens located directly over the

ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

Block Diagram



Output Waveforms



LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel/codestrip passes between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the codewheel/codestrip. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\bar{A}$, B, and $\bar{B}$. Comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

Definitions

Count (N): The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

1 cycle (C): 360 electrical degrees (°e), 1 bar and window pair.

1 Shaft Rotation: 360 mechanical degrees, N cycles.

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

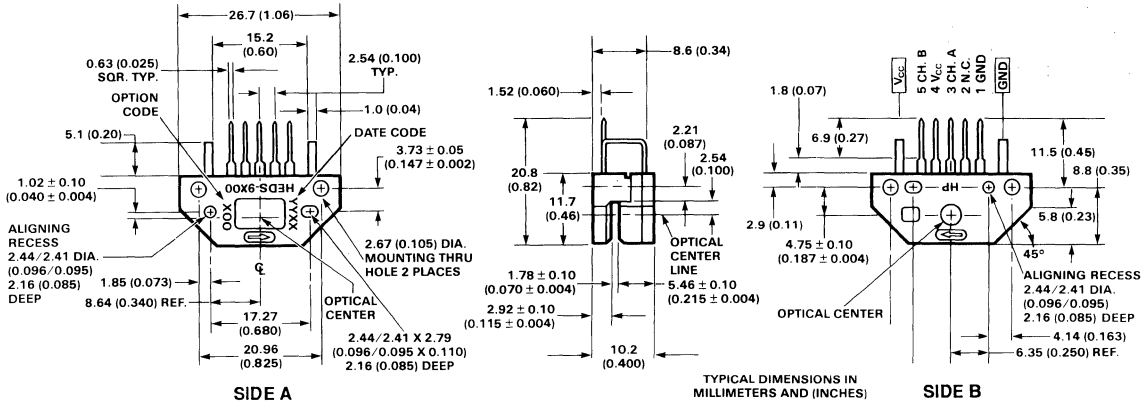
Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error ($\Delta\phi$): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates in the direction of the arrow on top of the module, channel A will lead channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (R_{op}): The distance from the codewheel's center of rotation to the optical center (O.C.) of the encoder module.

Package Dimensions



Absolute Maximum Ratings

Storage Temperature, T_S ..... -40°C to 100°C
Operating Temperature, T_A ..... -40°C to 100°C
Supply Voltage, V_{CC} ..... -0.5 V to 7 V
Output Voltage, V_O ..... -0.5 V to V_{CC}
Output Current per Channel, I_{out} ..... -1.0 mA to 5 mA

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T_A	-40		100	°C	
Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts	Ripple < 100 mV_{p-p}
Load Capacitance	C_L			100	pF	3.3 kΩ pull-up resistor
Count Frequency	f			100	kHz	Velocity (rpm) x N/60
Shaft Axial Play				±0.125 ±0.005	mm in.	

Note: The module performance is guaranteed to 100 kHz but can operate at higher frequencies. For frequencies above 100 kHz it is recommended that the load capacitance not exceed 25 pF and the pull up resistance not exceed 3.3 kΩ. For typical module performance above 100 kHz please see derating curves.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, typical at 25°C.

Parameter	Symbol	Min.	Typical	Max.	Units	Notes
Supply Current	I_{CC}	30	57	85	mA	
High Level Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -200 µA max.
Low Level Output Voltage	V_{OL}			0.4	Volts	I_{OL} = 3.86 mA
Rise Time	t_r		180		ns	C_L = 25 pF R_L = 3.3 kΩ pull-up
Fall Time	t_f		40		ns	

Encoding Characteristics

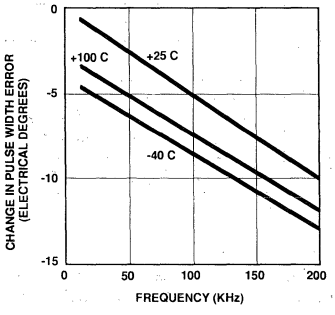
Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances. These Characteristics do not include codewheel/codestrip contribution. The Typical Values are averages over the full rotation of the codewheel. For operation above 100 kHz, see frequency derating curves.

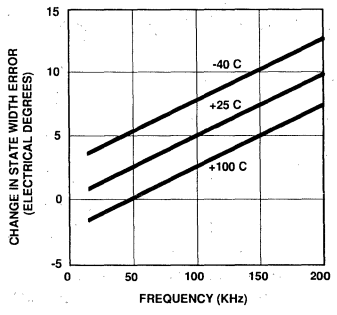
Description	Symbol	Typical	Maximum	Units
Pulse Width Error	ΔP	5	45	°e
Logic State Width Error	ΔS	3	45	°e
Phase Error	Δϕ	2	15	°e

Note: Module mounted on tolerance circle of ±0.13 mm (±0.005 in.) radius referenced from module Side A aligning recess centers. 3.3 kΩ pull-up resistors used on all encoder module outputs.

Frequency Derating Curves

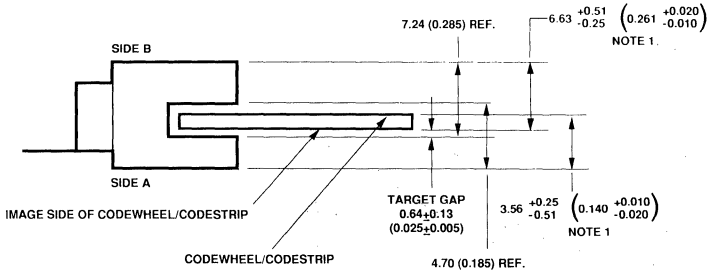
Typical performance over extended operating range. These curves were derived using a 25 pF load with a 3.3 k pull-up resistor. Greater load capacitances will cause more error than shown in these graphs.





Gap Setting for Rotary and Linear Modules

Gap is the distance between the image side of the codewheel and the detector surface of the module. This gap dimension must always be met and codewheel warp and shaft end play must stay within this range. This dimension is shown in Figure 1.



NOTES:
1. THESE DIMENSIONS INCLUDE CODEWHEEL/CODESTRIP WARP AND SHAFT END PLAY.
2. DIMENSIONS IN MILLIMETERS AND (INCHES).

Figure 1. Module Gap Setting.

Mounting Considerations for Rotary Modules

Figure 2 shows a mounting tolerance *requirement* for proper operation of the high resolution rotary encoder modules. The Aligning Recess Centers must be located within a tolerance circle of 0.13 mm (0.005 in.) radius from the nominal locations. This tolerance must be maintained whether the module is mounted with side A as the mounting plane using aligning pins (see Figure 3), or mounted with Side B as the mounting plane using an alignment tool.

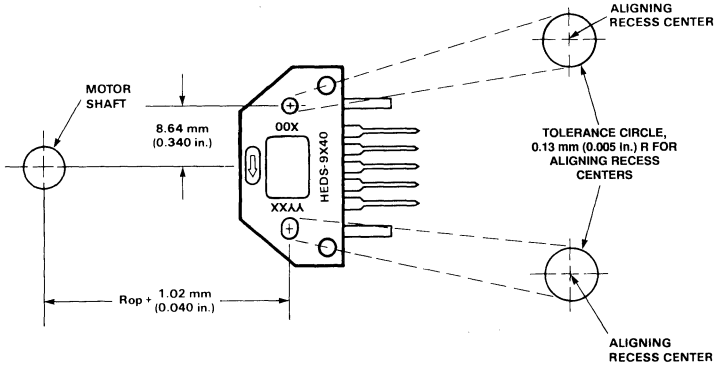


Figure 2. Rotary Module Mounting Tolerance.

Mounting with Aligning Pins

The high resolution rotary encoder modules can be mounted using aligning pins on the motor base. (HP does not provide aligning pins.) For this configuration, Side A *must* be used as the mounting plane. The Aligning Recess Centers must be located within the 0.13 mm (0.005 in.) R Tolerance Circle as explained above. Figure 3 shows the necessary dimensions.

Mounting with HP Alignment Tools

HP offers alignment tools for mounting HP encoder modules in conjunction with HP codewheels, using side B as the mounting plane. Please refer to the HP codewheel data sheet for more information.

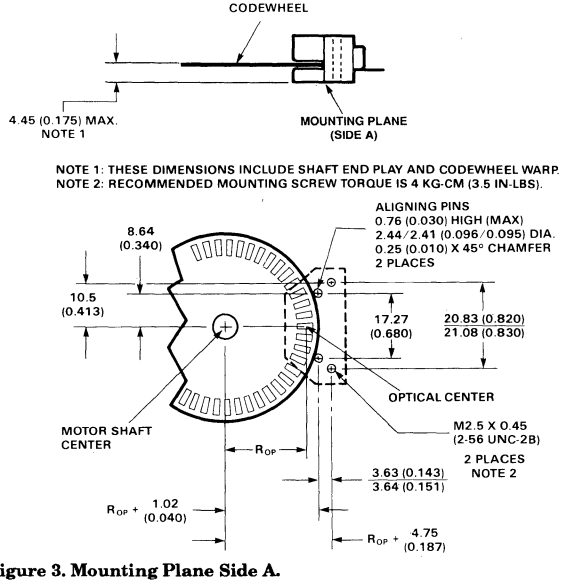
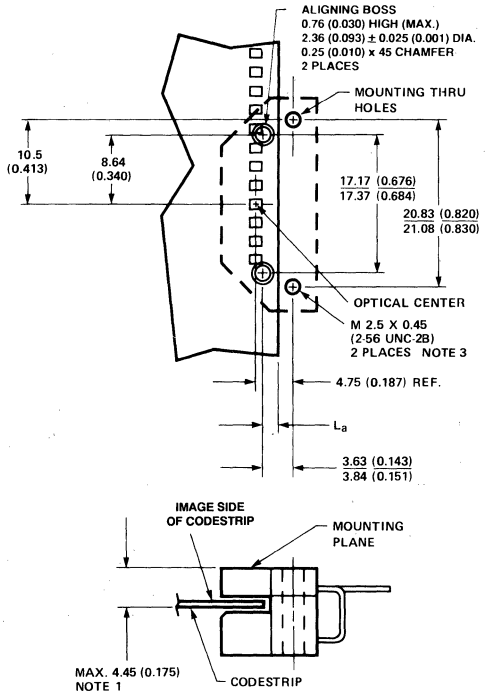
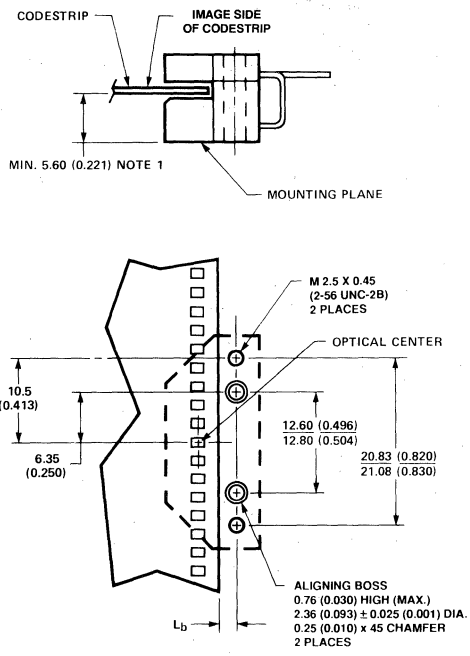


Figure 3. Mounting Plane Side A.

Mounting Considerations for Linear Modules



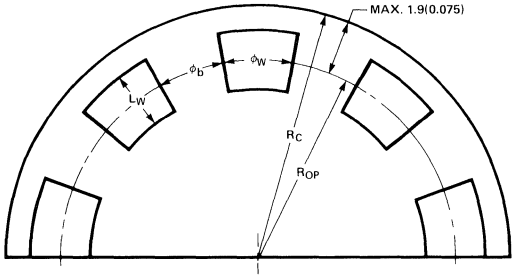


Mounting Plane Side A

Mounting Plane Side B

NOTES:
1. THESE DIMENSIONS INCLUDE CODESTRIP WARP.
2. REFERENCE DEFINITIONS OF L_a AND L_b ON THE FOLLOWING PAGE.
3. MAXIMUM RECOMMENDED MOUNTING SCREW TORQUE IS 4 kg-cm (3.5 in-lbs).

Recommended Codewheel Characteristics

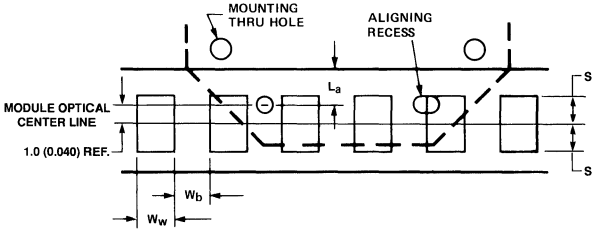


Parameter	Symbol	Minimum	Maximum	Units	Notes
Window/Bar Ratio	ϕ_w/ϕ_b	0.7	1.4		
Window Length	L_w	1.8 (0.07)		mm (inch)	
Absolute Maximum Codewheel Radius	R_c		$R_{op} + \frac{1.9}{(0.075)}$	mm (inch)	Includes eccentricity errors

Recommended Codestrip Characteristics and Alignment

Codestrip design must take into consideration mounting as referenced to either side A *or* side B (see Figure 4).

Mounting as Referenced to Side A



Mounting as Referenced to Side B

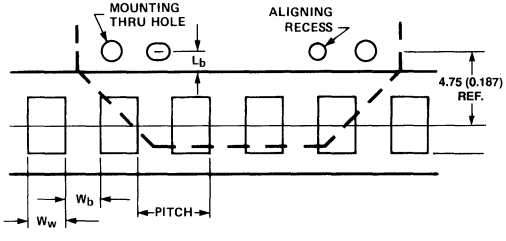


Figure 4. Codestrip Design.

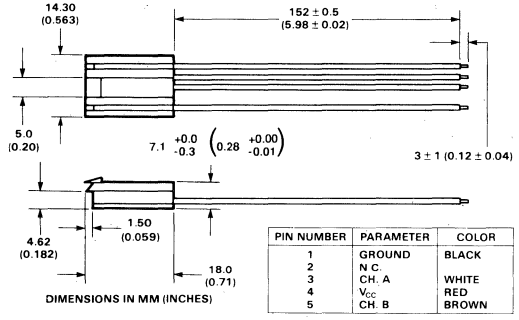
STATIC CHARGE WARNING: LARGE STATIC CHARGE ON CODESTRIP MAY HARM MODULE. PREVENT ACCUMULATION OF CHARGE.

Parameter	Symbol	Mounting Ref. Side A	Mounting Ref. Side B	Units
Window/Bar Ratio	W_w/W_b	0.7 min., 1.4 max.	0.7 min., 1.4 max.	
Window Distance	L	$L_a \leq 0.51$ (0.020)	$L_b \geq 3.23$ (0.127)	mm (inch)
Window Edge to Module Opt Center Line	S	0.90 (0.035) min.	0.90 (0.035) min.	mm (inch)
Parallelism Module to Codestrip	α	1.3 max.	1.3 max.	deg.

Note: All parameters and equations must be satisfied over the full length of codestrip travel including maximum codestrip runout.

Connectors

Manufacturer	Part Number	Mounting Surface
AMP	103686-4 640442-5	Both Side B
DuPont	65039-032 with 4825X-000 term.	Both
HP	HEDS-8902 with 4-wire leads	Side B (see Fig. 7)
Molex	2695 series with 2759 series term.	Side B



PIN NUMBER	PARAMETER	COLOR
1	GROUND	BLACK
2	N.C.	
3	CH. A	WHITE
4	V_{CC}	RED
5	CH. B	BROWN

Figure 7. HEDS-8902 Connector.

Ordering Information

Two Channel Encoder Modules with a 23.36 mm Optical Radius

HEDS-9000 Option ☐ 0 0 *

Resolution (Cycles/Rev)
T - 2000 CPR
U - 2048 CPR

Two Channel Encoder Modules with an 11.00 mm Optical Radius

HEDS-9100 Option ☐ 0 0 *

Resolution (Cycles/Rev)
B - 1000 CPR
J - 1024 CPR

Two Channel Linear Encoder Module

HEDS-9200 Option ☐☐☐

Resolution (Cycles/Rev)
300 - 300 LPI
360 - 360 LPI

*Codewheel Information

For information on matching codewheels and accessories for use with HP rotary encoder modules, please refer to the HP Codewheel Data sheet HEDS-5120/6100, HEDG-5120/6120, HEDM-5120/6120

HEWLETT PACKARD

Two Channel Optical Incremental Encoder Module

Technical Data

HEDS-9000
HEDS-9100

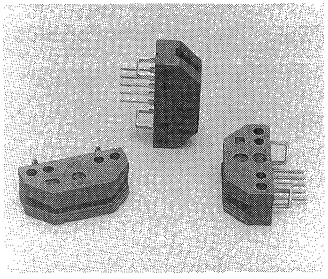
Features

- **High Performance**
- **High Resolution**
- **Low Cost**
- **Easy to Mount**
- **No Signal Adjustment Required**
- **Insensitive to Radial and Axial Play**
- **Small Size**
- **-40°C to 100°C Operating Temperature**
- **Two Channel Quadrature Output**
- **TTL Compatible**
- **Single 5 V Supply**

Description

The HEDS-9000 and HEDS-9100 series are high performance, low cost, optical incremental encoder modules. When used with a codewheel, these modules detect rotary position. The modules consist of a lensed LED source and a detector IC enclosed in a small C-shaped plastic package. Due to a highly collimated light source and a unique photo-detector array, the modules are extremely tolerant to mounting misalignment.

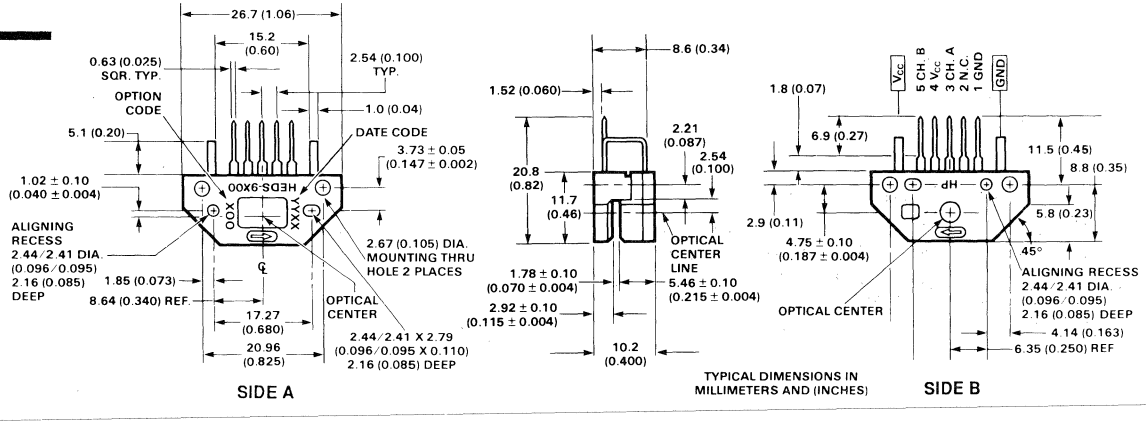
The two channel digital outputs and the single 5 V supply input



are accessed through five 0.025 inch square pins located on 0.1 inch centers.

Standard resolutions for the HEDS-9000 are 500 CPR and 1000 CPR for use with a HEDS-

Package Dimensions



ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

6100 codewheel or equivalent. For the HEDS-9100, standard resolutions between 96 CPR and 512 CPR are available for use with a HEDS-5120 codewheel or equivalent.

Applications

The HEDS-9000 and 9100 provide sophisticated motion detection at a low cost, making them ideal for high volume applications. Typical applications include printers, plotters, tape drives, and factory automation equipment.

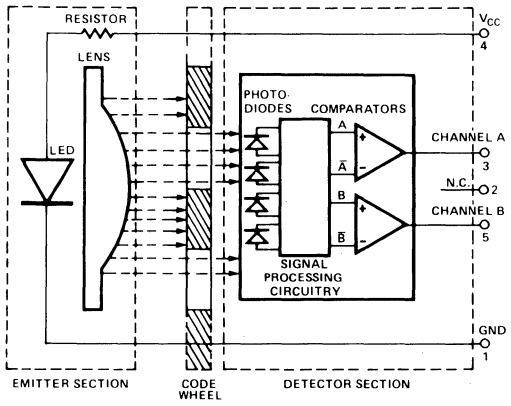
Theory of Operation

The HEDS-9000 and 9100 are C-shaped emitter/detector modules. Coupled with a codewheel, they translate the rotary motion of a shaft into a two-channel digital output.

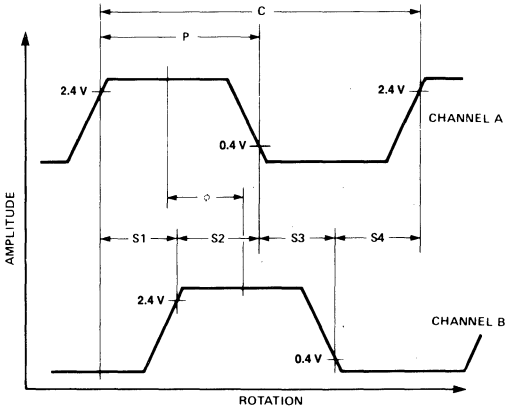
As seen in the block diagram, each module contains a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single polycarbonate lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel rotates between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and design of the codewheel. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\bar{A}$, B, and $\bar{B}$. Two comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

Block Diagram



Output Waveforms



Definitions

Count (N) = The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

1 Shaft Rotation = 360 mechanical degrees
= N cycles
1 cycle (c) = 360 electrical degrees (°e)
= 1 bar and window pair

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Absolute Maximum Ratings

Storage Temperature, T_S ..... -40°C to 100°C
Operating Temperature, T_A ..... -40°C to 100°C
Supply Voltage, V_{CC} ..... -0.5 V to 7 V
Output Voltage, V_O ..... -0.5 V to V_{CC}
Output Current per Channel, I_O ..... -1.0 mA to 5 mA

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error (Δϕ): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates in the direction of the arrow on top of the module, channel A will lead channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (R_{OP}): The distance from the codewheel's center of rotation to the optical center (O.C.) of the encoder module.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T	–40		100	°C	
Supply Voltage	V_{CC}	4.5		5.5	Volts	Ripple < 100 mV_{p-p}
Load Capacitance	C_L			100	pF	3.2 kΩ pull-up resistor
Count Frequency	f			100	kHz	$\frac{\text{Velocity (rpm) x N}}{60}$

Note: The module performance is guaranteed to 100 kHz but can operate at higher frequencies.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances. These characteristics do not include codewheel contributions.

Parameter	Sym.	Typ.	Case 1 Max.	Case 2 Max.	Units	Notes
Pulse Width Error	ΔP	7	30	40	°e	
Logic State Width Error	ΔS	5	30	40	°e	
Phase Error	Δϕ	2	10	15	°e	

Case 1: Modules mounted on tolerances of ±0.13 mm (0.005").
Case 2: HEDS-9000 mounted on tolerances of ±0.50 mm (0.020").
HEDS-9100 mounted on tolerances of ±0.38 mm (0.015").

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, typical at 25°C.

Parameter	Symbol	Min.	Typical	Max.	Units	Notes
Supply Current	I_{CC}		17	40	mA	
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40 µA max.
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA
Rise Time	t_r		200		ns	C_L = 25 pF
Fall Time	t_f		50		ns	R_L = 11 kΩ pull-up

Recommended Codewheel Characteristics

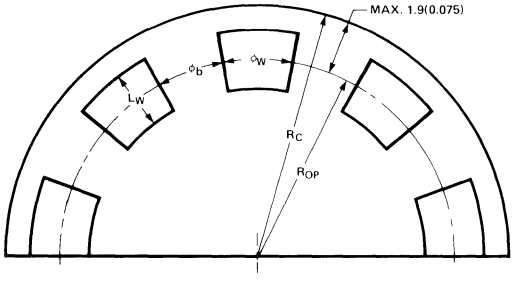


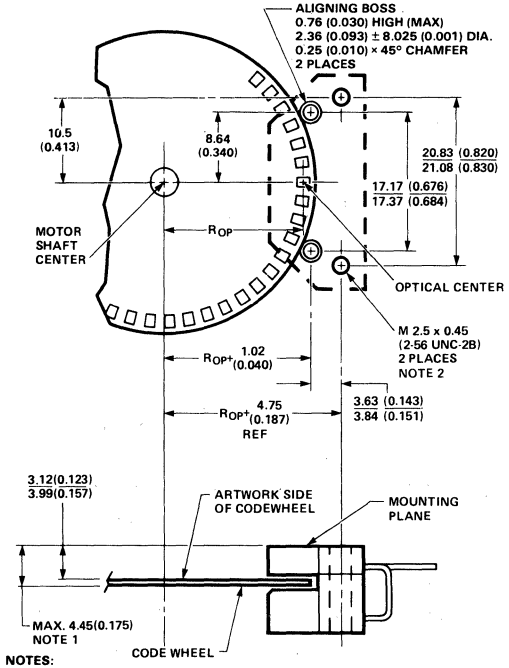
Figure 1. Codewheel Design.

Codewheel Options

HEDS Series	CPR (N)	Option	Optical Radius mm (in.)
5120	96	K	11.00 (0.433)
5120	100	C	11.00 (0.433)
5120	192	D	11.00 (0.433)
5120	200	E	11.00 (0.433)
5120	256	F	11.00 (0.433)
5120	360	G	11.00 (0.433)
5120	400	H	11.00 (0.433)
5120	500	A	11.00 (0.433)
5120	512	I	11.00 (0.433)
6100	500	A	23.36 (0.920)
6100	1000	B	23.36 (0.920)

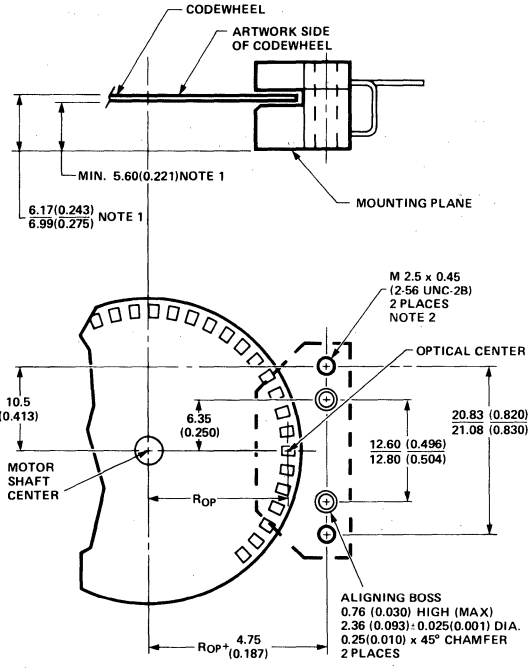
Parameter	Symbol	Minimum	Maximum	Units	Notes
Window/Bar Ratio	ϕ_w/ϕ_b	0.7	1.4		
Window Length	L_w	1.8 (0.07)	2.3 (0.09)	mm (inch)	
Absolute Maximum Codewheel Radius	R_C		R_{OP} + 1.9 (0.075)	mm (inch)	Includes eccentricity errors

Mounting Considerations



NOTES:
1. THESE DIMENSIONS INCLUDE SHAFT END PLAY, AND CODEWHEEL WARP.
2. MAXIMUM RECOMMENDED MOUNTING SCREW TORQUE IS 4 kg-cm (3.5 in-lbs).

Figure 2. Mounting Plane Side A.



NOTES:
1. THESE DIMENSIONS INCLUDE SHAFT END PLAY, AND CODEWHEEL WARP.
2. MAXIMUM RECOMMENDED MOUNTING SCREW TORQUE IS 4 kg-cm (3.5 in-lbs).

Figure 3. Mounting Plane Side B.

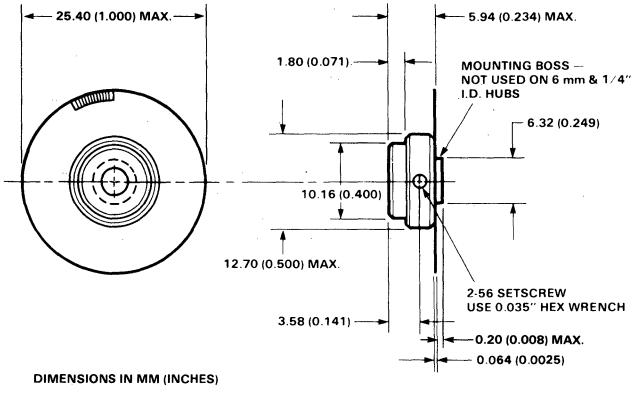


Figure 4. HEDS-5120 Codewheel.

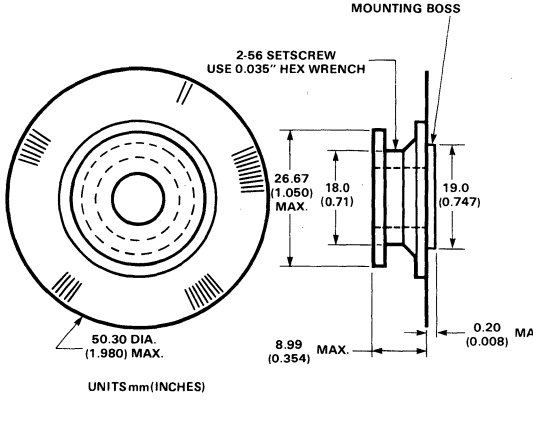


Figure 5. HEDS-6100 Codewheel.

Connectors

Manufacturer	Part Number	Mounting Surface
AMP	103686-4 640442-5	Both Side B
DuPont	65039-032 with 4825X-000 term.	Both
HP	HEDS-8902 with 4-wire leads	Side B (see Fig. 6)
Molex	2695 series with 2759 series term.	Side B

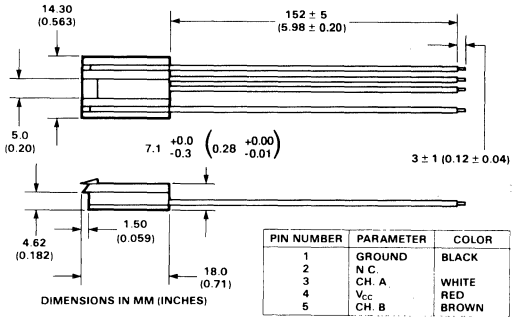


Figure 6. HEDS-8902 Connector.

Ordering Information

HEDS-9000 Option ☐ 0 0 **HEDS-6100 Option** ☐ ☐ ☐

Resolution (Cycles/Rev)
A - 500 CPR
B - 1000 CPR
T = 2000 CPR*
U = 2048 CPR*

Shaft Diameter	
05 - 3/16 in.	10 - 5/8 in.
06 - 1/4 in.	11 - 4 mm
07 - 5/16 in.	12 - 6 mm
08 - 3/8 in.	13 - 8 mm
09 - 1/2 in.	

HEDS-9100 Option ☐ 0 0 **HEDS-5120 Option** ☐ ☐ ☐

Resolution (Cycles/Rev)	
K - 96 CPR	G - 360 CPR
C - 100 CPR	H - 400 CPR
D - 192 CPR	A - 500 CPR
E - 200 CPR	I - 512 CPR
F - 256 CPR	B - 1000 CPR*
	J - 1024 CPR*

Shaft Diameter	
01 - 2 mm	11 - 4 mm
02 - 3 mm	14 - 5 mm
03 - 1/8 in.	12 - 6 mm
04 - 5/32 in.	13 - 8 mm
05 - 3/16 in.	
06 - 1/4 in.	

*Please refer to separate Extended Resolution D/S for detailed information.

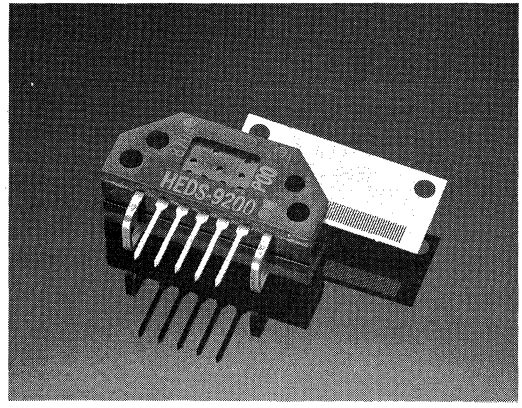
HEWLETT PACKARD

LINEAR OPTICAL INCREMENTAL ENCODER MODULE

HEDS-9200 SERIES

Features

- **HIGH PERFORMANCE**
- **HIGH RESOLUTION**
- **LOW COST**
- **EASY TO MOUNT**
- **NO SIGNAL ADJUSTMENT REQUIRED**
- **INSENSITIVE TO MECHANICAL DISTURBANCES**
- **SMALL SIZE**
- **-40° C TO 100° C OPERATING TEMPERATURE**
- **TWO CHANNEL QUADRATURE OUTPUT**
- **TTL COMPATIBLE**
- **SINGLE 5 V SUPPLY**



Note: Codestrip not included with HEDS-9200.

Description

The HEDS-9200 series is a high performance, low cost, optical incremental encoder module. When operated in conjunction with a codestrip, this module detects linear position. The module consists of a lensed LED source and a detector IC enclosed in a small C-shaped plastic package. Due to a highly collimated light source and a unique photo-detector array, the module is extremely tolerant to mounting misalignment.

The two channel digital outputs and the single 5 V supply input are accessed through four 0.025 inch square pins located on 0.1 inch centers.

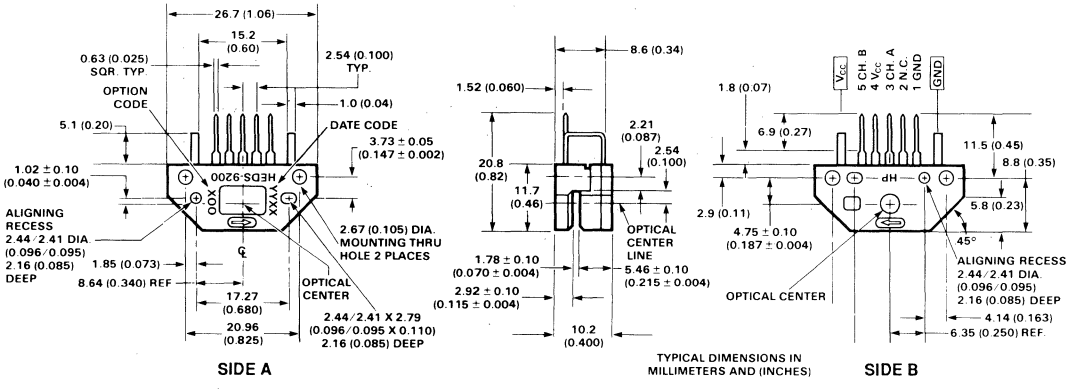
Five standard resolutions between 4.72 counts per mm (120 counts per inch) and 7.87 counts per mm (200 counts per inch) are available. Consult local Hewlett-Packard sales representatives for other resolutions ranging from 1.5 to 7.87 counts per mm (40 to 200 counts per inch).

Applications

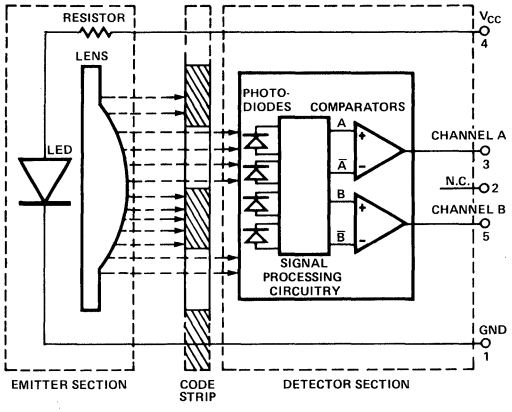
The HEDS-9200 provides sophisticated motion detection at a low cost, making it ideal for high volume applications. Typical applications include printers, plotters, tape drives, and factory automation equipment.

ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

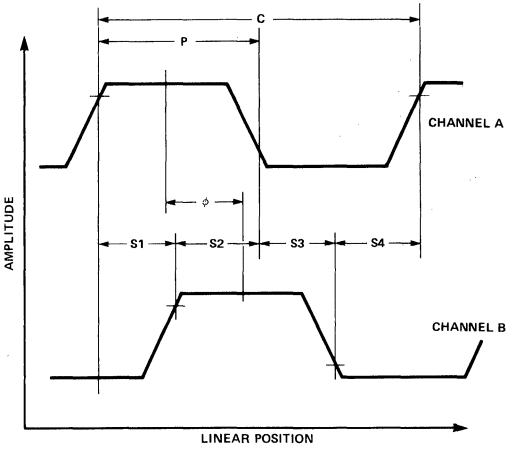
Package Dimensions



Block Diagram



Output Waveforms



Theory of Operation

The HEDS-9200 is a C-shaped emitter/detector module. Coupled with a codestrip it translates linear motion into a two-channel digital output.

As seen in the block diagram, the module contains a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single poly-carbonate lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codestrip moves between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codestrip. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the count density of the codestrip. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\overline{A}$, B and $\overline{B}$. Two comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

Definitions

Count density (D): The number of bar and window pairs per unit length of the codestrip.

Pitch: 1/D, The unit length per count.

Electrical degree (° e): Pitch/360, The dimension of one bar and window pair divided by 360.

1 cycle (C): 360 electrical degrees, 1 bar and window pair.

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180° e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180° e.

State Width(S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90° e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90° e.

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90° e for quadrature output.

Phase Error ($\Delta\phi$): The deviation of the phase from its ideal value of 90° e.

Direction of Movement: When the codestrip moves, relative to the module, in the direction of the arrow on top of the module, channel A will lead channel B. If the codestrip moves in the opposite direction, channel B will lead channel A.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Storage Temperature	T_S	-40		100	°C	
Operating Temperature	T_A	-40		100	°C	
Supply Voltage	V_{CC}	-0.5		7	Volts	
Output Voltage	V_O	-0.6		V_{CC}	Volts	
Output Current per Channel	I_O	-1.0		5	mA	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T	-40		100	°C	
Supply Voltage	V_{CC}	4.5		5.5	Volts	Ripple < 100 m Vp-p
Load Capacitance	C_L			100	pF	3.2 KΩ pull-up resistor
Count Frequency	f			100	kHz	Velocity X D

Note:
The module performance is guaranteed to 100 kHz but can operate at higher frequencies.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances. These characteristics do not include codestrip defects.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Pulse Width Error	ΔP		7	35	elec. deg.	
Logic State Width Error	ΔS		5	35	elec. deg.	
Phase Error	Δφ		2	13	elec. deg.	

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, typical at 25° C

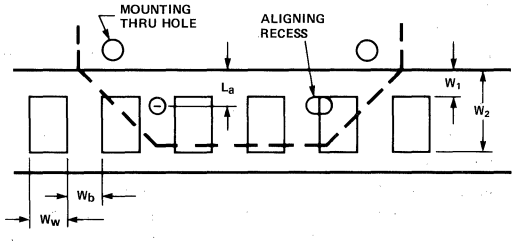
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		17	40	mA	
High Level Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -40 μA Max.
Low Level Output Voltage	V_{OL}			0.4	Volts	I_{OL} = 3.2 mA
Rise Time	t_r		200		ns	C_L = 25 pF
Fall Time	t_f		50		ns	R_L = 11 KΩ pull-up

Note:
1. For improved performance in noisy environments or high speed applications, a 3.3 kΩ pull-up resistor is recommended.

Recommended Codestrip Characteristics

Codestrip design must take into consideration mounting as referenced to either side A *or* side B (See figure 1).

MOUNTING AS REFERENCED TO SIDE A



MOUNTING AS REFERENCED TO SIDE B

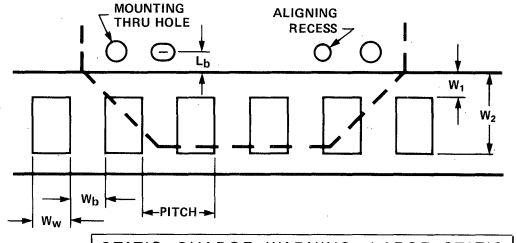


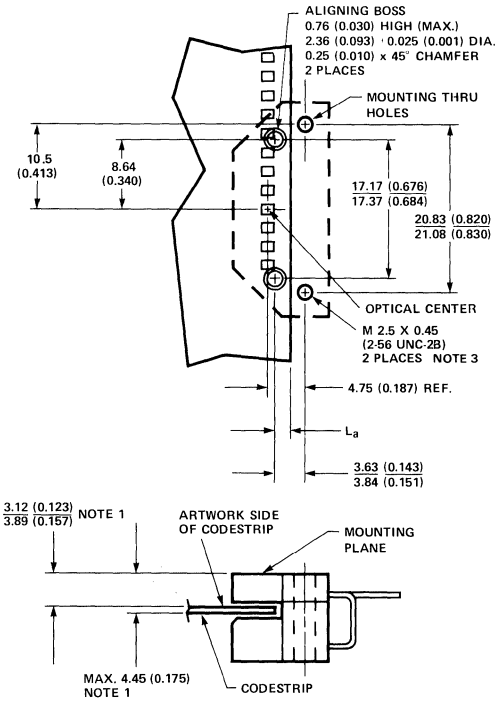
Figure 1. Codestrip Design

STATIC CHARGE WARNING: LARGE STATIC CHARGE ON CODESTRIP MAY HARM MODULE. PREVENT ACCUMULATION OF CHARGE.

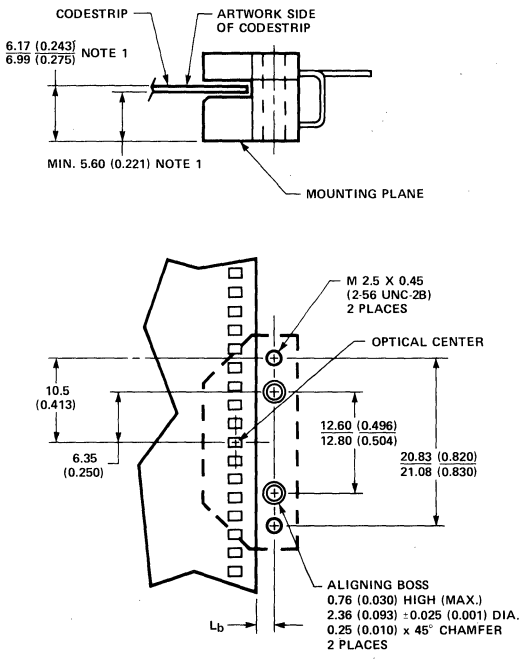
Parameter	Symbol	Mounting Ref. Side A	Mounting Ref. Side B	Units
Window/Bar Ratio	W_W/W_b	0.7 Min. 1.4 Max.	0.7 Min. 1.4 Max.	
Mounting Distance	L	$L_a \leq 0.51$ (0.020)	$L_b \geq 3.23$ (0.127)	mm (inch)
Codestrip edge to inside window edge	W_1	$W_1 \leq 0.53$ (0.021) + L_a	$W_1 \leq 4.27$ (0.168) - L_b	mm (inch)
Codestrip edge to outside window edge	W_2	$W_2 \geq 1.50$ (0.059) + L_a	$W_2 \geq 5.23$ (0.206) - L_b	mm (inch)

Note:
All parameters and equations must be satisfied over the full length of codestrip travel including maximum codestrip runout.

Mounting Considerations



MOUNTING PLANE SIDE A



MOUNTING PLANE SIDE B

Notes:

1. These dimensions include codestrip warp.
2. Reference definitions of L_a and L_b on page 3.
3. Maximum recommended mounting screw torque is 4 kg-cm (3.5 in-lbs).

Connectors

Manufacturer	Part Number	Mounting Surface
AMP	103686-4	Both
	640442-5	Side B
DuPont	65039-032 with 4825X-000 term.	Both
HP	HEDS-8902 with 4-wire leads	Side B
Molex	2695 series with 2759 series term.	Side B

Ordering Information

HEDS-9200 Option

RESOLUTION Counts per mm (inch)	PITCH mm (inch) per count
L00 - 4.72 (120)	0.212 (0.0083)
M00 - 5.00 (127)	0.200 (0.0079)
P00 - 5.91 (150)	0.169 (0.0067)
Q00 - 7.09 (180)	10.141 (0.0056)
R00 - 7.87 (200)	0.127 (0.0050)
300 - 11.81 (300)*	0.085 (0.0033)*
360 - 14.17 (360)*	0.071 (0.0028)*

Consult local Hewlett-Packard sales representatives for other resolutions.

*Please refer to separate Extended Resolution D/S for detailed information.

HEWLETT PACKARD

Three Channel Optical Incremental Encoder Modules

Technical Data

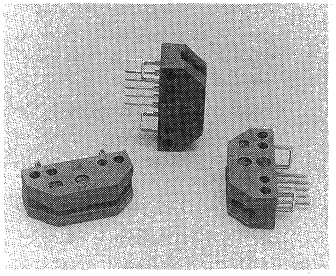
HEDS-9040
HEDS-9140

Features

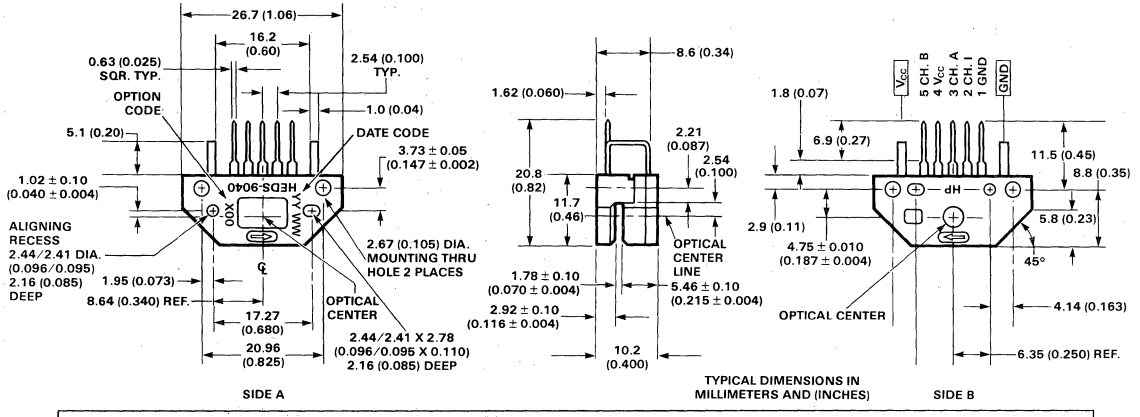
- **Two Channel Quadrature Output with Index Pulse**
- **Resolution Up to 1024 Counts Per Revolution**
- **Low Cost**
- **Easy to Mount**
- **No Signal Adjustment Required**
- **Small Size**
- **-40°C to100°C Operating Temperature**
- **TTL Compatible**
- **Single 5 V Supply**

Description

The HEDS-9040 and HEDS-9140 series are three channel optical incremental encoder modules. When used with a codewheel, these low cost modules detect rotary position. Each module consists of a lensed LED source and a detector IC enclosed in a small plastic package. Due to a highly collimated light source and a unique photodetector array, these modules provide the same high performance found in the HEDS-9000/9100 two channel encoder family.



Package Dimensions



ESD WARNING; NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

The HEDS-9040 and 9140 have two channel quadrature outputs plus a third channel index output. This index output is a 90 electrical degree high true index pulse which is generated once for each full rotation of the codewheel.

The HEDS-9040 is designed for use with a HEDS-6140 codewheel which has an optical radius of 23.36 mm (0.920 inch). The HEDS-9140 is designed for use with a HEDS-5140 codewheel which has an optical radius of 11.00 mm (0.433 inch).

The quadrature signals and the index pulse are accessed through five 0.025 inch square pins located on 0.1 inch centers.

Standard resolutions between 256 and 1024 counts per revolution are available. Consult local Hewlett-Packard sales representatives for other resolutions.

Applications

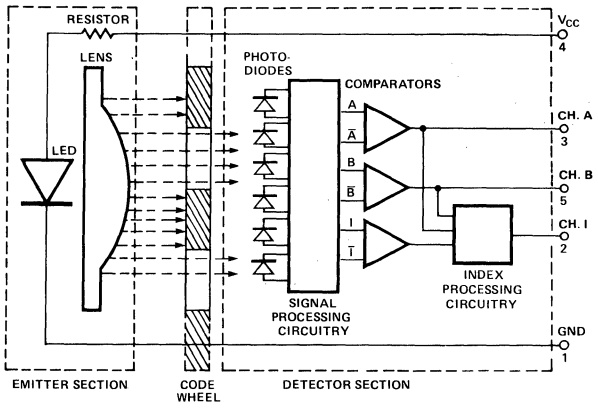
The HEDS-9040 and 9140 provide sophisticated motion control detection at a low cost, making then ideal for high volume applications. Typical applications include printers, plotters, tape drives, and industrial and factory automation equipment.

Theory of Operation

The HEDS-9040 and 9140 are emitter/detector modules. Coupled with a codewheel, these modules translate the rotary motion of a shaft into a three-channel digital output.

As seen in the block diagram, the modules contain a single

Block Diagram

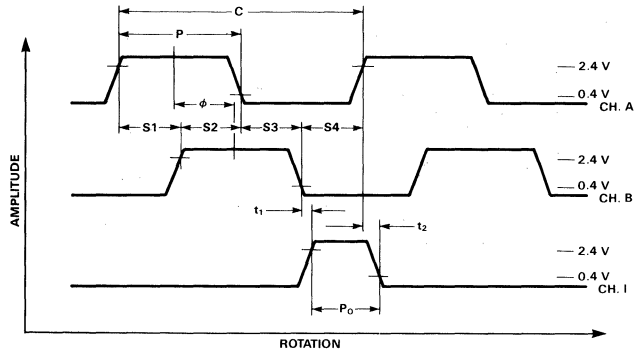


Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single polycarbonate lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel rotates between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and design of the codewheel. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\overline{A}$, B, $\overline{B}$, I and $\overline{I}$. Comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

The output of the comparator for I and $\overline{I}$ is sent to the index processing circuitry along with the outputs of channels A and B. The final output of channel I is an index pulse P_0 which is generated once for each full rotation of the codewheel. This output P_0 is a one state width (nominally 90 electrical degrees), high true index pulse which is coincident with the low states of channels A and B.

Output Waveforms



Definitions

Count (N): The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

One Cycle (C): 360 electrical degrees (°e), 1 bar and window pair.

One Shaft Rotation: 360 mechanical degrees, N cycles.

Position Error ($\Delta\Theta$): The normalized angular difference between the actual shaft position and the position indicated by the encoder cycle count.

Cycle Error (ΔC): An indication of cycle uniformity. The difference between an observed shaft angle which gives rise to one electrical cycle, and the nominal angular increment of 1/N of a revolution.

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error ($\Delta\phi$): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates in the direction of the arrow on top of the module, channel A will lead channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (R_{OP}): The distance from the codewheel's center of rotation to the optical center (O.C.) of the encoder module.

Index Pulse Width (P_O): The number of electrical degrees that an index is high during one full shaft rotation. This value is nominally 90°e or 1/4 cycle.

Absolute Maximum Ratings

Storage Temperature, T_S	-40°C to 100°C
Operating Temperature, T_A	-40°C to 100°C
Supply Voltage, V_{CC}	-0.5 V to 7 V
Output Voltage, V_O	-0.5 V to V_{CC}
Output Current per Channel, I_{OUT}	-1.0 mA to 5 mA
Shaft Axial Play	±0.25 mm (±0.010 in.)
Shaft Eccentricity Plus Radial Play	0.1 mm (0.004 in.) TIR
Velocity	30,000 RPM[1]
Acceleration	250,000 rad/sec^2[1]

Note:

1. Absolute maximums for HEDS-5140/6140 codewheels only.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T_A	-40		100	°C	
Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts	Ripple < 100 mV_{p-p}
Load Capacitance	C_L			100	pF	2.7 kΩ pull-up
Count Frequency	f			100	kHz	Velocity (rpm) x N/60
Shaft Perpendicularity Plus Axial Play				±0.25 (±0.010)	mm (in.)	6.9 mm (0.27 in.) from mounting surface
Shaft Eccentricity Plus Radial Play				0.04 (0.0015)	mm (in.) TIR	6.9 mm (0.27 in.) from mounting surface

Note: The module performance is guaranteed to 100 kHz but can operate at higher frequencies.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances unless otherwise specified. Values are for the worst error over the full rotation of HEDS-5140 and HEDS-6140 codewheels.

Parameter		Symbol	Min.	Typ.*	Max.	Units
Cycle Error		ΔC		3	5.5	°e
Pulse Width Error		ΔP		7	30	°e
Logic State Width Error		ΔS		5	30	°e
Phase Error		Δϕ		2	15	°e
Position Error		ΔΘ		10	40	min. of arc
Index Pulse Width		P_O	60	90	120	°e
CH. I rise after CH. B or CH. A fall	-25°C to +100°C	t_1	10	100	250	ns
	-40°C to +100°C	t_1	-300	100	250	ns
CH. I fall after CH. A or CH. B rise	-25°C to +100°C	t_2	70	150	300	ns
	-40°C to +100°C	t_2	70	150	1000	ns

Note: Module mounted on tolerance circle of ±0.13 mm (±0.005 in.) radius referenced from module Side A aligning recess centers. 2.7 kΩ pull-up resistors used on all encoder module outputs.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Notes
Supply Current	I_{CC}	30	57	85	mA	
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -200 μA max.
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.86 mA
Rise Time	t_r		180		ns	C_L = 25 pF R_L = 2.7 kΩ pull-up
Fall Time	t_f		40		ns	

* Typical values specified at V_{CC} = 5.0 V and 25°C.

Mechanical Characteristics

Part No.	Parameter	Dimension	Tolerance	Units
HEDS-6140 23.36 mm optical radius codewheel	Codewheel Available to Fit These Standard Shaft Diameters	4 6 8	+0.000 -0.015	mm
		3/16 1/4 5/16 3/8 1/2 5/8	+0.000 -0.0007	in
	Moment of Inertia	7.7 (110 x 10^{-6})		g-cm^2 (oz-in-s^2)
HEDS-5140 11.00 mm optical radius codewheel	Codewheel Available to Fit These Standard Shaft Diameters	2 3 4 5 6 8	+0.000 -0.015	mm
		5/32 1/8 3/16 1/4	+0.000 -0.0007	in
	Moment of Inertia	0.6 (8.0 x 10^{-6})		g-cm^2 (oz-in-s^2)

Note: The tolerance requirements are on the mating shaft, not on the codewheel.

Electrical Interface

To insure reliable encoding performance, the HEDS-9040 and 9140 three channel encoder modules require 2.7 kΩ (±10%) pull-up resistors on output pins 2, 3, and 5 (Channels I, A and B) as shown in Figure 1. These pull-up resistors should be located as close to the encoder module as possible (within 4 feet). Each of the three encoder module outputs can drive a single TTL load in this configuration.

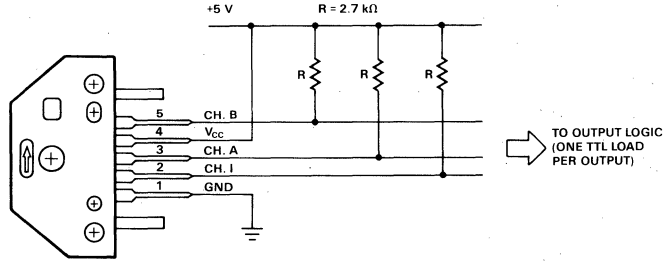


Figure 1. Pull-up Resistors on HEDS-9X40 Encoder Module Outputs.

Mounting Considerations

Figure 2 shows a mounting tolerance *requirement* for proper operation of the HEDS-9040 and HEDS-9140. The Aligning Recess Centers must be located within a tolerance circle of 0.005 in. radius from the nominal locations. This tolerance must be maintained whether the module is mounted with side A as the mounting plane using aligning pins (see Figure 5), or mounted with Side B as the mounting plane using an alignment tool (see Figures 3 and 4).

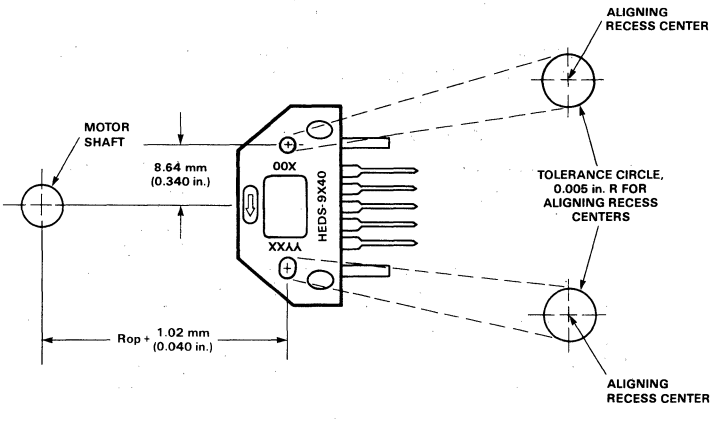


Figure 2. HEDS-9X40 Mounting Tolerance.

Mounting with an Alignment Tool

The HEDS-8905 and HEDS-8906 alignment tools are recommended for mounting the modules with Side B as the mounting plane. The HEDS-8905 is used to mount the HEDS-9140, and the HEDS-8906 is used to mount the HEDS-9040. These tools fix the module position using the codewheel hub as a reference. They will not work if Side A is used as the mounting plane.

The following assembly procedure uses the HEDS-8905/8906 alignment tool to mount a HEDS-9140/9040 module and a HEDS-5140/6140 codewheel:

Instructions:

1. Place codewheel on shaft.

2. Set codewheel height: (a) place alignment tool on motor base (pins facing up) flush up against the motor shaft as shown in Figure 3. (b) Push codewheel down against alignment tool. The codewheel is now at the proper height. (c) Tighten codewheel setscrew and remove alignment tool.

Some motors have a boss around the shaft that extends above the mounting plane. In this case, the alignment tool cannot be used as a gage block to set the codewheel height as described in 2(a), (b), and (c).
If boss is above mounting plane: Slide module onto motor base, adjusting height of codewheel so that it sits approximately in the middle of module slot. Lightly tighten setscrew. The codewheel height will be more precisely set in step 5.

3. Insert mounting screws through module and thread into the motor base. Do not tighten screws.

4. Slide alignment tool over codewheel hub and onto module as shown in Figure 4. The pins of the alignment tool should fit snugly inside the alignment recesses of the module.

If boss is above mounting plane: The pins of the tool may not mate properly because the codewheel is too high on the shaft. Loosen codewheel setscrew and lower codewheel slightly. Retighten setscrew lightly and attempt this step again.

5. While holding alignment tool in place, tighten screws down to secure module.

If boss is above mounting plane: Push codewheel up flush against alignment tool to set codewheel height. Tighten codewheel setscrew.

6. Remove alignment tool.

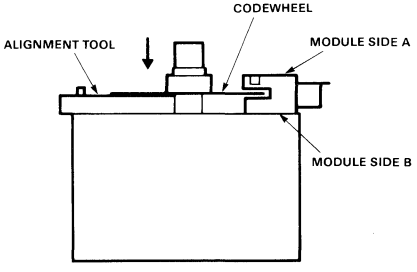


Figure 3. Alignment Tool is Used to Set Height of Codewheel.

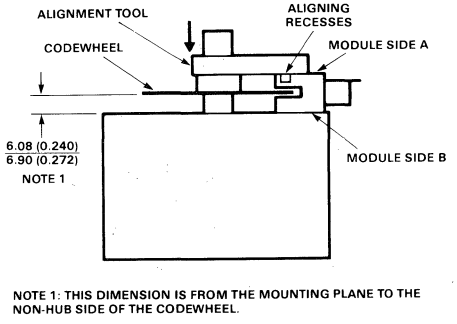


Figure 4. Alignment Tool is Placed over Shaft and onto Codewheel Hub. Alignment Tool Pins Mate with Aligning Recesses on Module.

Mounting with Aligning Pins

The HEDS-9040 and HEDS-9140 can also be mounted using aligning pins on the motor base. (Hewlett-Packard does not provide aligning pins.) For this configuration, Side A *must* be used as the mounting plane. The aligning recess centers must be located within the 0.005 in. Radius Tolerance Circle as explained in "Mounting Considerations." Figure 5 shows the necessary dimensions.

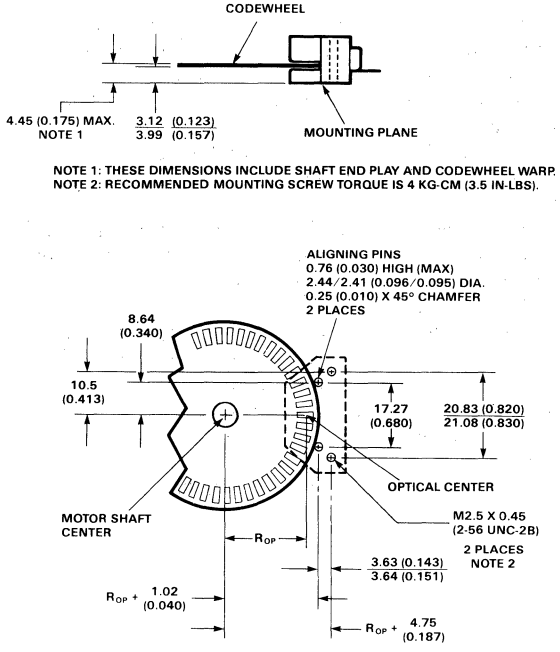


Figure 5. Mounting Plane Side A.

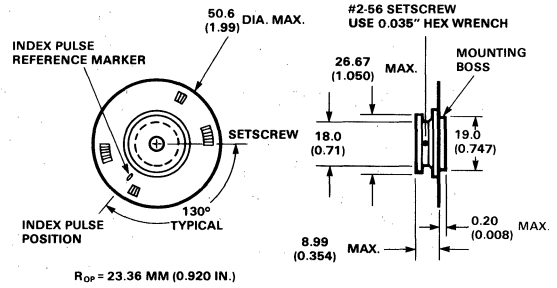


Figure 6. HEDS-6140 Codewheel Used with HEDS-9040.

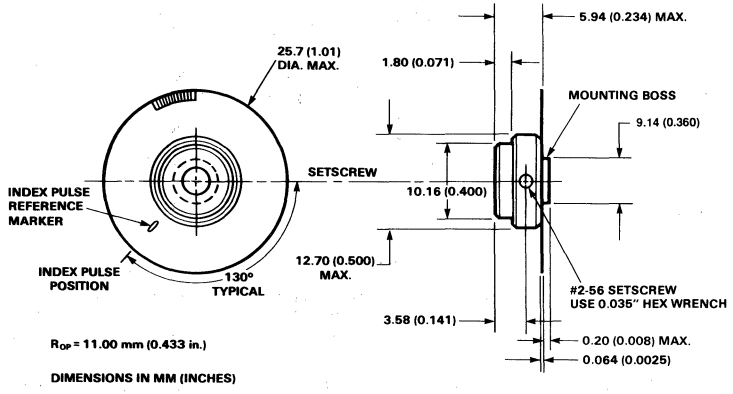
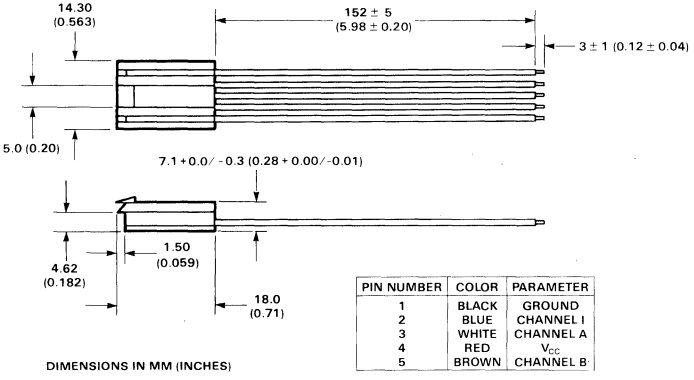


Figure 7. HEDS-5140 Codewheel Used with HEDS-9140.

Connectors

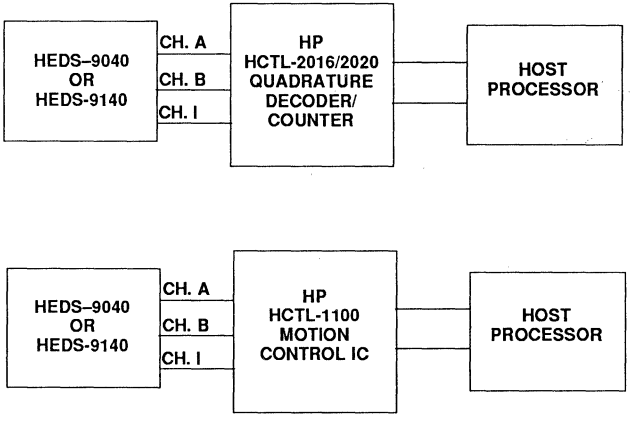
Manufacturer	Part Number	Mounting Surface
AMP	103686-4	Both
	640442-5	Side B
DuPont	65039-032 with 4825X-000 term.	Both
HP	HEDS-8903 with 5-wire leads	Side B (see Figure 8)
Molex	2695 series with 2759 series term.	Side B



PIN NUMBER	COLOR	PARAMETER
1	BLACK	GROUND
2	BLUE	CHANNEL I
3	WHITE	CHANNEL A
4	RED	V_{CC}
5	BROWN	CHANNEL B

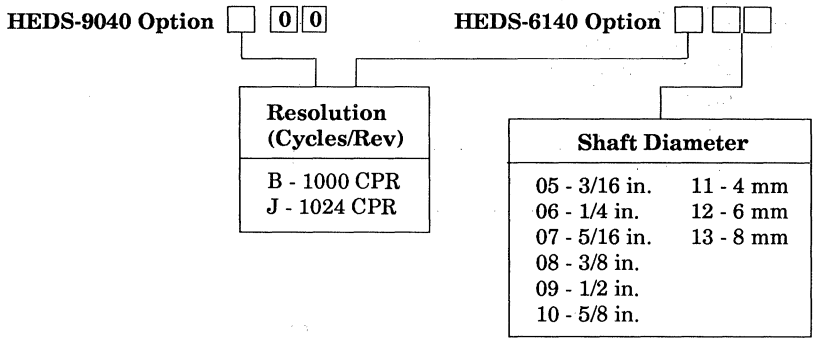
Figure 8. HEDS-8903 Connector.

Typical Interfaces

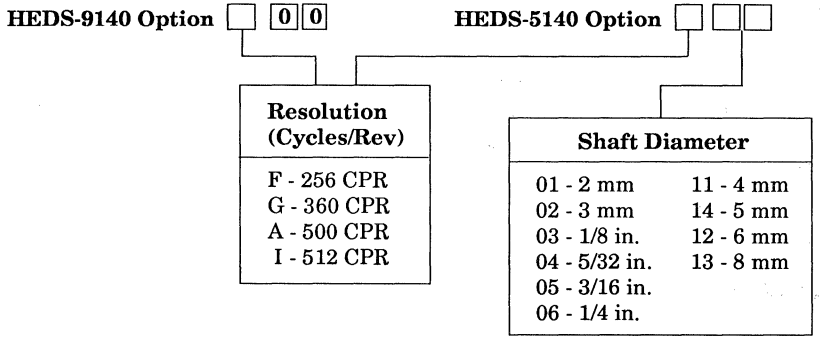


Ordering Information

Three Channel Encoder Modules and Codewheels, 23.36 mm Optical Radius



Three Channel Encoder Modules and Codewheels, 11.00 mm Optical Radius



Accessories

HEDS-8905
Alignment Tool for mounting the HEDS-9140.

HEDS-8906
Alignment Tool for Mounting the HEDS-9040.

Small Optical Encoder Module

Technical Data

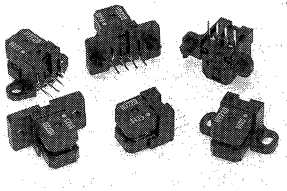
HEDS-9700 Series

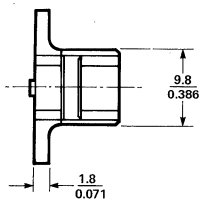
Features

- **Small Size**
- **Low Cost**
- **Multiple Mounting Options**
- **Wide Resolution Range**
- **Linear and Rotary Options Available**
- **No Signal Adjustment Required**
- **Insensitive to Radial and Axial Play**
- **-40°C to +85°C Operating Temperature**
- **Two Channel Quadrature Output**
- **TTL Compatible**
- **Single 5V Supply**
- **Wave Solderable**

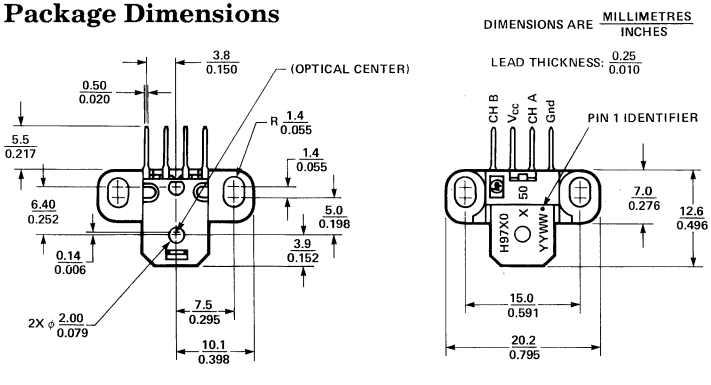
Description

The HEDS-9700 series is a high performance, low cost, optical incremental encoder module. When operated in conjunction with either a codewheel or codestrip, this module detects rotary or linear position. The





Package Dimensions



Mounting Option #50 - Standard

Contact Factory for Detailed Package Dimensions

ESD WARNING; NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

module consists of a lensed LED source and a detector IC enclosed in a small C-shaped plastic package. Due to a highly collimated light source and a unique photodetector array, the module is extremely tolerant to mounting misalignment.

The two channel digital outputs and 5V supply input are accessed through four solder-plated leads located on 2.54 mm (0.1 inch) centers.

The standard HEDS-9700 is designed for use with an 11 mm optical radius codewheel, or linear codestrip. Other options are available. Please contact factory for more information.

Applications

The HEDS-9700 provides sophisticated motion detection at a low cost, making closed-loop control very cost-competitive! Typical applications include printers, plotters, copiers, and office automation equipment.

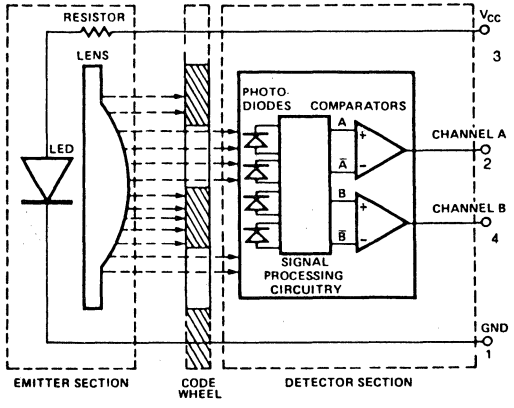
Theory of Operation

The HEDS-9700 is a C-shaped emitter/detector module. Coupled with a codewheel, it translates rotary motion into a two-channel digital output. Coupled with a codestrip, it translates linear motion into a digital output.

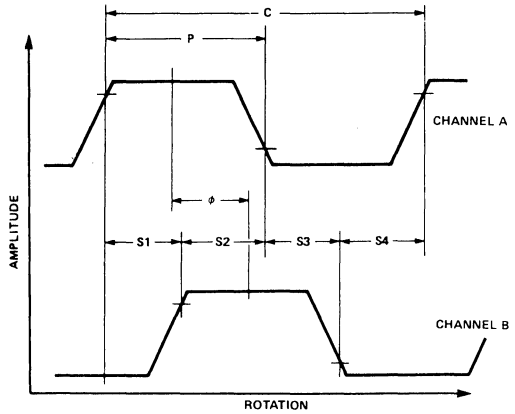
As seen in the block diagram, the module contains a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel/codestrip moves between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel/codestrip. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and count density of the codewheel/codestrip. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are fed through the signal processing circuitry. Two comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with channel B (90 degrees out of phase).

Block Diagram



Output Waveforms



Definitions

Count (N) = The number of bar and window pairs or counts per revolution (CPR) of the codewheel, or the number of lines per inch of the codestrip (LPI).

1 Shaft Rotation = 360 mechanical degrees
= N cycles

1 cycle (c) = 360 electrical degrees (°e)
= 1 bar and window pair

Pulse Width (P): The number of electrical degrees that an output is high during one cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error (Δϕ): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates counterclockwise, as viewed looking down on the module (so the marking is visible), channel A will lead channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (Rop): The distance from the codewheel's center of rotation to the optical center (O.C.) of the encoder module.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	85	°C	See Note
Operating Temperature	T_A	-40	85	°C	See Note
Supply Voltage	V_{CC}	-0.5	7	V	
Output Voltage	V_O	-0.5	V_{CC}	V	
Output Current per Channel	I_O	-1.0	5	mA	
Soldering Temperature			260	°C	t ≤ 5 sec.

Note: Higher operating ranges available, contact factory for more information.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	–40	85	°C	
Supply Voltage	V_{CC}	4.5	5.5	V	Ripple < 100 mV_{p-p}
Load Capacitance	C_L		100	pF	3.2 kΩ pull-up
Count Frequency			20	kHz	(Velocity (rpm) x N)/60

Note: The module performance is guaranteed to 20 kHz but can operate at higher frequencies. Contact factory for more information.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances. These characteristics do not include codewheel/codestrip contributions.

Parameter	Symbol	Typ.	Case 1 Max.	Case 2 Max.	Units	Notes
Pulse Width Error	ΔP	7	30	40	°e	
Logic State Width Error	ΔS	5	30	40	°e	
Phase Error	Δϕ	2	10	15	°e	

Case 1: Module mounted on tolerances of ±0.13 mm (0.005"). Case 2: Module mounted on tolerances of ±0.25 mm (0.010")

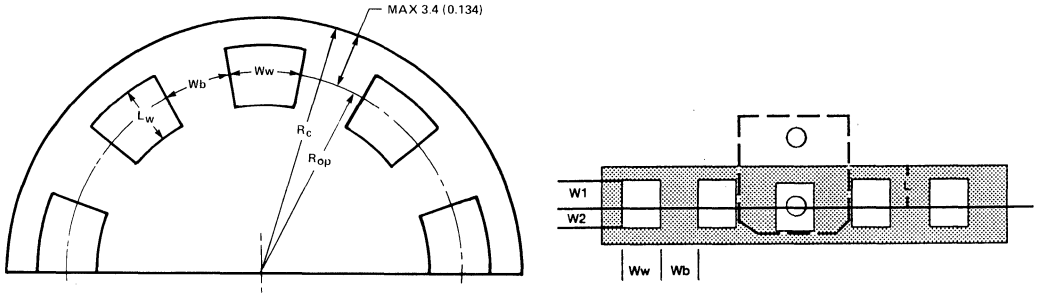
Note: See Figures in Mounting Considerations for details on Case 1 and Case 2 mounting tolerances.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, Typical at 25°C.

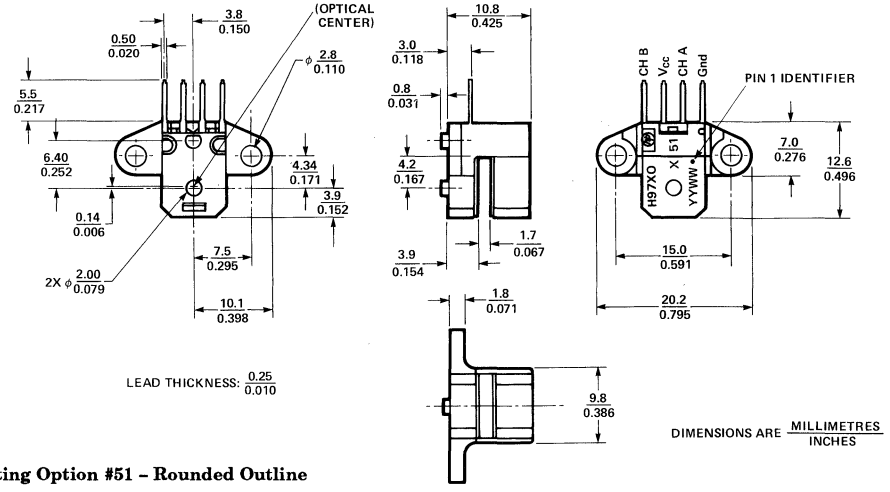
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		17	40	mA	
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40 μA
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA
Rise Time	t_r		200		ns	C_L = 25 pF, R_L = 11 kΩ
Fall Time	t_f		50		ns	C_L = 25 pF, R_L = 11 kΩ

Recommended Codewheel and Codestrip Characteristics



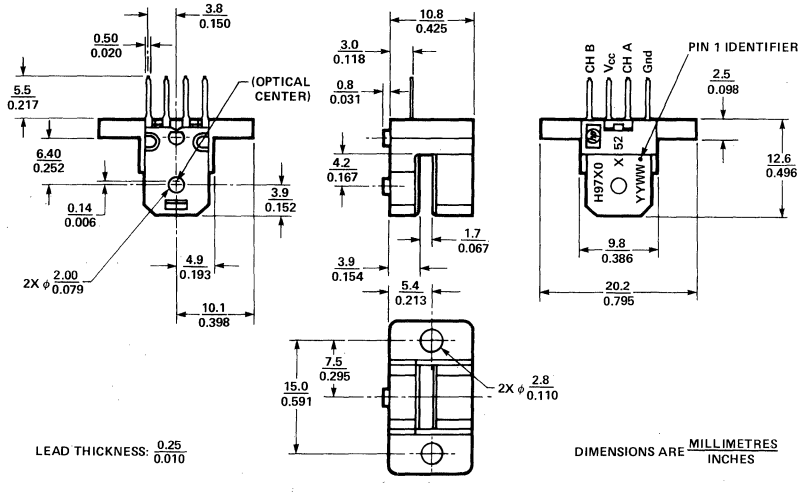
Parameter	Symbol	Min.	Max.	Units	Notes
Window/Bar Ratio	Ww/Wb	0.7	1.4		
Window Length (Rotary)	Lw	1.80 (0.071)	2.30 (0.091)	mm (inch)	
Absolute Maximum Codewheel Radius (Rotary)	Rc		Rop + 3.40 (Rop + 0.134)	mm (inch)	Includes eccentricity errors
Center of Post to Inside Edge of Window	W1	1.04 (0.041)		mm (inch)	
Center of Post to Outside Edge of Window	W2	0.76 (0.030)		mm (inch)	
Center of Post to Inside Edge of Codestrip	L		3.60 (0.142)	mm (inch)	

Optional Packages Available

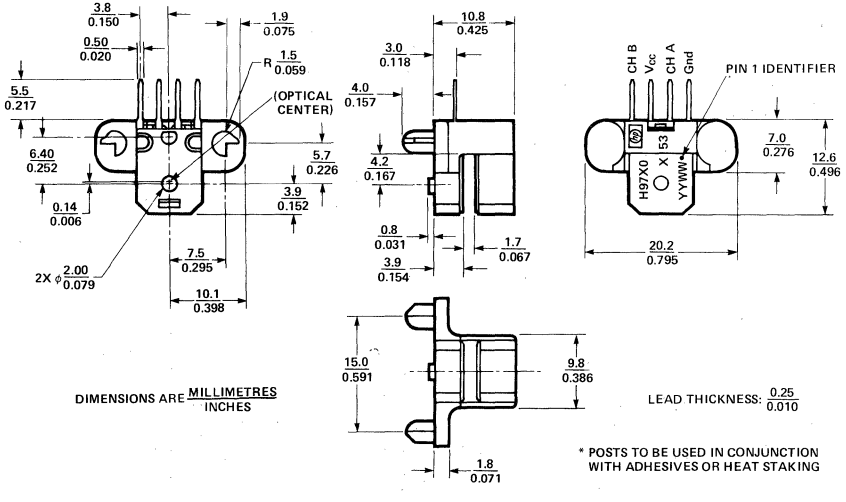


Mounting Option #51 – Rounded Outline

Optional Packages Available (cont'd.)

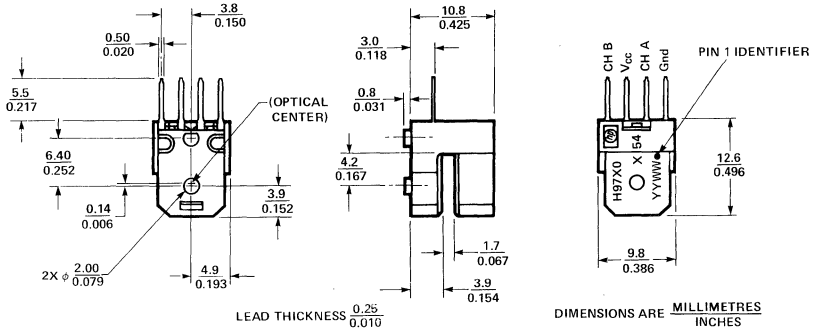


Mounting Option #52 – Backplane

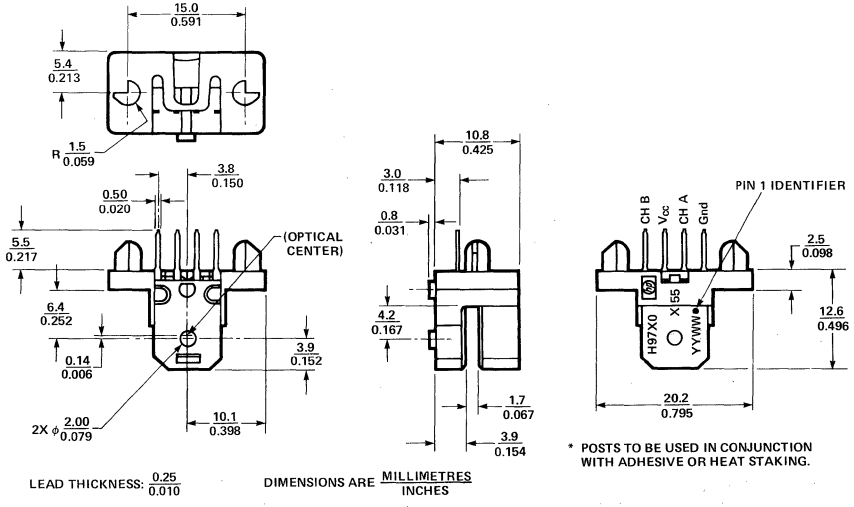


Mounting Option #53 – Standard with Posts

Optional Packages Available (cont'd.)

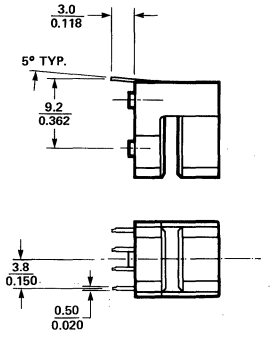


Mounting Option #54 – Tabless



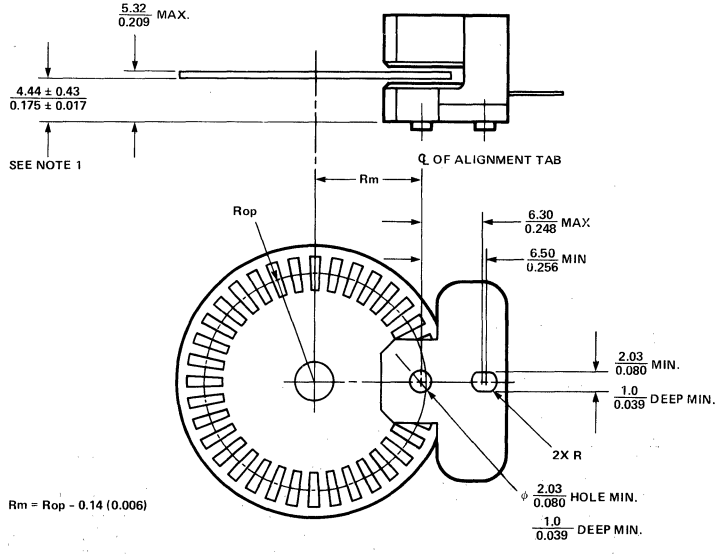
Mounting Option #55 – Backplane with Posts

Bent Lead Option



DIMENSIONS ARE MILLIMETERS / INCHES

Mounting Considerations



Note: These dimensions include shaft end play and codewheel warp.

All dimensions for mounting the module and codewheel/codestrip should be measured with respect to the two mounting posts, shown above.

Mounting Tolerances

Case 1 and Case 2 specify the mounting tolerances required on Rm in order to achieve the respective encoding characteristics shown on page 4. The mounting tolerances are as follows:

Case 1: Rm ± 0.13 mm (.005 inches)
Case 2: Rm ± 0.25 mm (.010 inches)

Recommended Screw Size: M2.5 x 0.45 or 2-56

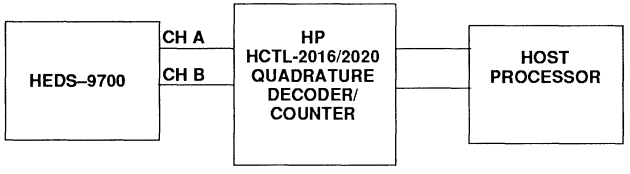
Wave Solder Conditions

Flux – RMA Water Soluble (per MIL-F-14256D)

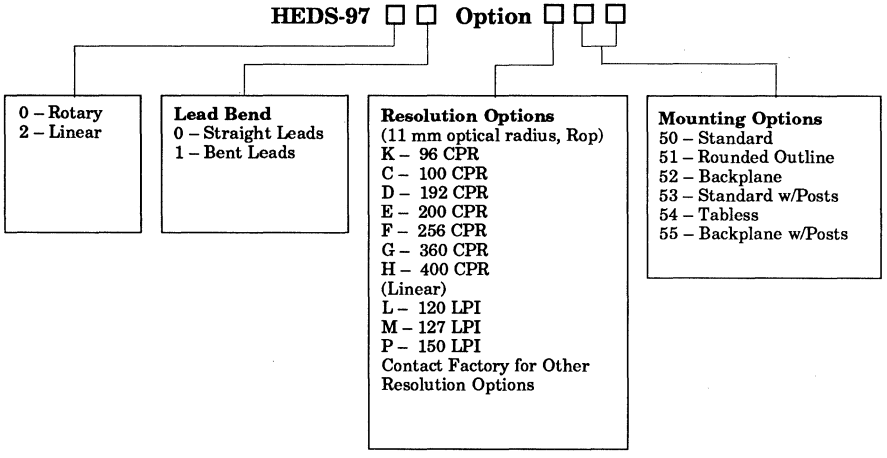
Process Parameters

1. Flux
2. Pre-heat 60 seconds total
   PCB top side @ 230°C
   PCB bottom side @ 260°C
3. Wave solder 255°C, 1.2 meters/min line speed
4. Hot Water Wash
   1st: 30°C 45 seconds
   2nd: 70°C 90 seconds
5. Rinse
   1st: 23°C 45 seconds
   2nd: 23°C 45 seconds
6. Dry
   1st: 80°C 105 seconds
   2nd: 95°C 105 seconds

Typical Interface



Ordering Information



Note: Please contact factory for codewheel and codestrip information.

Two and Three Channel Codewheels for Use with HP Optical Encoder Modules

Technical Data

HEDS-51X0/61X0 Series
New **HEDG-5120/6120**
New **HEDM-5120/6120**

Features:

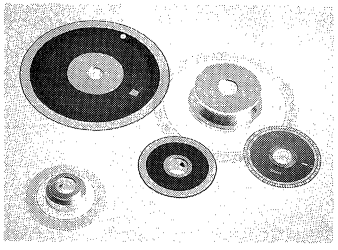
- **Codewheels Available in Glass, Film, and Metal**
- **Available in Two Standard Diameters**
- **Cost Effective**
- **Resolutions From 96 CPR to 2048 CPR**
- **For Use With HEDS-9000/ 9100 Series Two and Three Channel Encoders**

Description

Hewlett-Packard offers a wide variety of codewheels for use with Hewlett Packard HEDS-9000, HEDS-9100, HEDS-9040, and HEDS-9140 series Encoder Modules. Designed for many environments, applications, and budgets, HP codewheels are available in Glass, Film, and Metal. These codewheels are available in resolutions from 96 Counts Per Revolution (CPR) to 1024 CPR on a 28 mm diameter, and 500 to 2048 CPR on a 56 mm diameter.

Each of the three codewheel materials offers a certain advantage. Metal codewheels are the most versatile, with a temperature rating up to 100°C, resolution to 512 CPR (28 mm diameter), as well as 2 and 3 channel outputs. Film codewheels offer higher resolution (up to 1024 CPR on a 28 mm diameter) with an operating temperature of 70°C. Glass codewheels combine the best of film and metal, offering a temperature rating of 100°C and resolutions to 1024 CPR on a 28 mm diameter.

In addition, each material offers a specific reliability rating. It is important to consider the specific application operating environment, long term operating conditions, and temperature ranges when choosing a codewheel material.



Also See:

- HEDS-9000/HEDS-9100 Encoder Module Data Sheet
- HEDS-9000/9100/9200 Extended Resolution Encoder Module Data Sheet
- HEDS-9040/9140 Three Channel Encoder Module Data Sheet
- HEDS-9700 Small Encoder Module Data Sheet.

Absolute Maximum Ratings

It is important to consider the environment in which the codewheels will be used when selecting a codewheel material. In brief, metal codewheels are rugged, but do not offer higher resolution capabilities. Film codewheels allow higher resolution, but cannot endure the same temperatures and high humidity as metal. Glass codewheels offer both high temperature and higher resolution, but are also more expensive. Consider the following rating table when choosing a codewheel material.

Parameter	Symbol	HEDS-XXXX Metal Codewheels	HEDM-XXXX Film Codewheels	HEDG-XXXX Glass Codewheels
Storage Temperature	T_S	-40°C to +100°C	-40°C to +70°C	-40°C to +100°C
Operating Temperature	T_A	-40°C to +100°C	-40°C to +70°C	-40°C to +100°C
Humidity			non condensing	
Velocity		30,000 RPM	30,000 RPM	12,000 RPM
Shaft Axial Play		±0.25 mm (±0.010 in)	±0.175 mm (±0.007 in)	±0.175 mm (±0.007 in)
Shaft Eccentricity Plus Radial Play		±0.1 mm (±0.004 in) TIR	±0.04 mm (±0.0015 in) TIR	±0.04 mm (±0.0015 in) TIR
Acceleration		250,000 Rad/Sec^2	250,000 Rad/Sec^2	100,000 Rad/Sec^2

Recommended Operating Conditions

Parameter	HEDS-XXXX Metal Codewheels	HEDM-XXXX Film Codewheels	HEDG-XXXX Glass Codewheels
Maximum Count Frequency	100 kHz	200 kHz	200 kHz
Shaft Plus Axial Play	±0.25 mm (±0.010 in)	±0.175 mm (±0.007 in)	±0.175 mm (±0.007 in)
Shaft Eccentricity Plus Radial Play	±0.1 mm (±0.004 in) TIR	±0.04 mm (±0.0015 in) TIR	±0.04 mm (±0.0015 in) TIR

Note: HP Encoder Modules are guaranteed to 100 kHz, but can operate at higher frequencies. See Encoder Module Data Sheet for specifications and output load recommendations.

Encoding Characteristics

Encoding characteristics over recommended operating range and recommended mounting tolerances unless otherwise specified. Values are for worst error over a full rotation. Please refer to Encoder Module Data Sheet for definitions of Encoding characteristics.

Part Number	Description	Symbol	Min.	Typ.	Max.	Units
HEDS-512X	Cycle Error Position Error	ΔC Δθ		3 10	5.5 40	°e min. of arc
HEDS-61XX	Cycle Error Position Error	ΔC Δθ		3 7	5.5 20	°e min. of arc
HEDM-512X	Cycle Error Position Error	ΔC Δθ		3 4	7.5 40	°e min. of arc
HEDM-612X	Cycle Error Position Error	ΔC Δθ		3 2	7.5 20	°e min. of arc
HEDG-512X	Cycle Error Position Error	ΔC Δθ		3 4	7.5 30	°e min. of arc
HEDG-612X	Cycle Error Position Error	ΔC Δθ		3 2	7.5 15	°e min. of arc

Reliability

In addition to the absolute maximum specifications of codewheels, the environment characteristics of the application are also important. For example, consistent, large temperature swings over the life of the product will affect the codewheel performance characteristics depending on the material. The following reliability table shows results of lifetests under varying conditions of temperature and humidity.

Glass Codewheel Tests

Test	Duration	Number of Parts	Number of Failures
Storage at 100°C	1000 hours	44	0
Rotating at 100°C	500 hours	10	0
Temperature Cycle: -40°C to +100°C	500 cycles	98	0
Temperature/Humidity: 85°C/85 % R.H.	500 hours	43	0

Film Codewheel Tests

Test	Duration	Number of Parts	Number of Failures
Storage at 70°C	1000 hours	118	0
Rotating at 70°C	500 hours	10	0
Temperature Cycle: -40°C to +70°C	500 cycles	66	0
Temperature Cycle: +20°C to +40°C	1000 cycles	64	0
Temperature Cycle: +20°C to +55°C	1000 cycles	46	0
Temperature Cycle: +20°C to +70°C	500 cycles	50	0

Mounting Rotary Encoders with Codewheels

There are two orientations for mounting the HP encoder module and HP codewheel. Figure 1a shows mounting the module with side A as the mounting plane. Figure 1b shows mounting the module with side B as the mounting plane. When assembling the encoder and codewheel, it is important to maintain the tolerances of Side A of the module, and the image side of the codewheel.

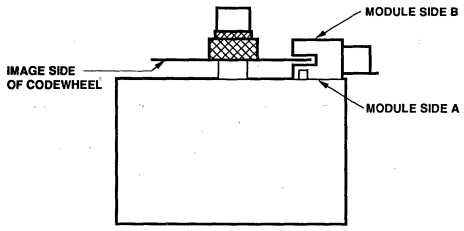


Figure 1a.

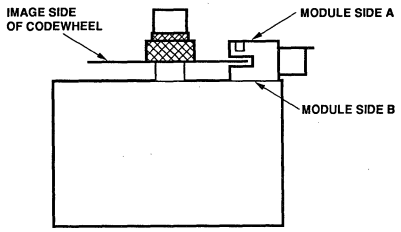


Figure 1b.

*Please note that the image side of the codewheel must always be facing the module Side A.

Mounting with Module Side A as the Mounting Plane

Mounting a high resolution or three channel encoder with Module Side A as the mounting plane requires alignment pins in the motor base. These alignment pins provide the necessary centering of the module with respect to the center of the motor shaft. In addition to centering, the codewheel gap is also important. Please refer to the respective encoder data sheet for necessary mounting information.

Mounting with Module Side B as the Mounting Plane, using HP Assembly Tools

When mounting the encoder module with an HP codewheel using the Module Side B as the mounting plane, HP offers assembly tools for centering and gap setting.

The HEDS-8905 and HEDS-8906 are alignment/centering tools available for the high resolution and three channel encoder modules. The HEDS-8901 and HEDS-8932 are gap setting shims used to set the codewheel gap in the encoder module. Please refer to the selection guide in this data sheet to choose the correct assembly tools. Also note that these tools are only useful when using Side B of the encoder module as the mounting plane.

Assembly Instructions Using HP Assembly Tools

Instructions

1. Place codewheel on shaft.
2. Set codewheel height:
   (a) Place HEDS-8901 or HEDS-8932 gap setting shim on motor base flush up against the motor shaft as shown in Figure 2. The shim has two different size steps, choose the one that most closely matches the width of the codewheel boss. The shim should not contact the codewheel boss.
   (b) Push codewheel down against gap setting shim. The codewheel is now at the proper height.
   (c) Tighten codewheel setscrew.
3. Insert mounting screws through module and thread into the motor base. Do not tighten screws.
4. Slide the HEDS-8905 or HEDS-8906 centering tool over codewheel hub and onto module as shown in Figure 3. The pins of the alignment tool should fit snugly inside the alignment recesses of the module.
5. While holding alignment tool in place, tighten screws down to secure module.
6. Remove alignment tools.

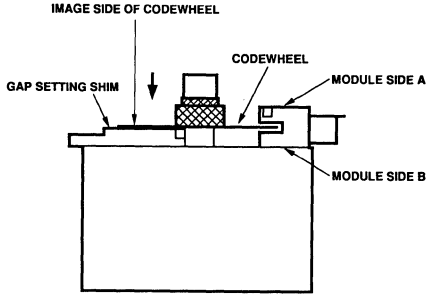


Figure 2. Alignment Tool is Used to Set Height of Codewheel.

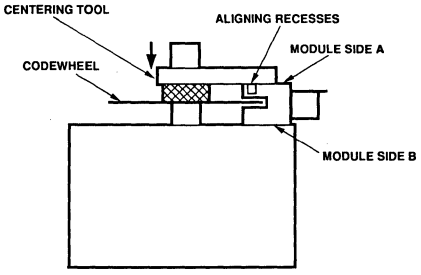


Figure 3. Alignment Tool is Placed over Shaft and onto Codewheel Hub. Alignment Tool Pins Mate with Aligning Recesses on Module.

Selection Guide

Use the following selection guide to choose the necessary codewheel and assembly tools for the appropriate HP encoder module.

Codewheel Part Number	Material	Optical Radius	For Use with HP Encoder Module	Centering Tool	Gap-Setting Shim
HEDS-5120#XXX	Metal	Rop = 11 mm	HEDS-9100#XXX (96 to 512 CPR)	HEDS-8905[1]	HEDS-8901[1]
HEDS-5140#XXX	Metal	Rop = 11 mm	HEDS-9140#XXX (96 to 512 CPR)	HEDS-8905[2]	HEDS-8905[2]
HEDM-5120#XXX	Film	Rop = 11 mm	HEDS-9100#XXX (1000 to 1024 CPR)	HEDS-8905	HEDS-8901
HEDG-5120#XXX	Glass	Rop = 11 mm	HEDS-9100#XXX (1000 to 1024 CPR)	HEDS-8905	HEDS-8932
HEDS-6100#XXX	Metal	Rop = 23 mm	HEDS-9000#XXX (500 to 1000 CPR)	HEDS-8906[1]	HEDS-8901[1]
HEDS-6140#XXX	Metal	Rop = 23 mm	HEDS-9040#XXX (1000,1024 CPR)	HEDS-8906[2]	HEDS-8906[2]
HEDM-6120#XXX	Film	Rop = 23 mm	HEDS-9000#XXX (2000,2048 CPR)	HEDS-8906	HEDS-8901
HEDG-6120#XXX	Glass	Rop = 23 mm	HEDS-9000#XXX (2000,2048 CPR)	HEDS-8906	HEDS-8932

Notes:

1. For the lower resolution, two channel encoders, the centering tool and gap-setting shim are not necessary, but sometimes helpful in an assembly process.
2. For the three channel modules (HEDS-9040/9140), the centering tool is also used for gap setting. Refer to the HEDS-9040/9140 data sheet for more information.

Mechanical Drawings

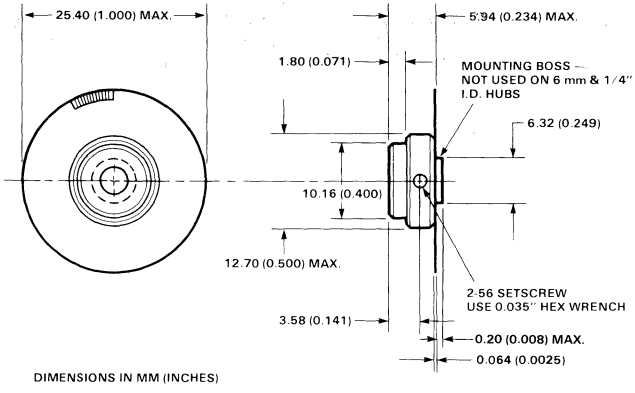


Figure 4. HEDS-5120 Codewheel.

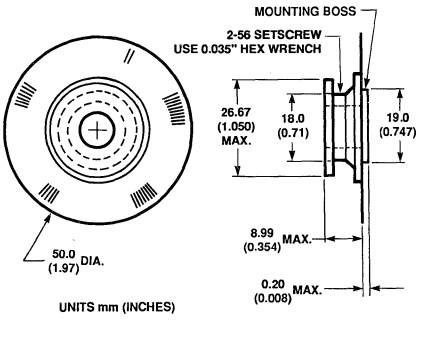


Figure 5. HEDS-6100 Codewheel.

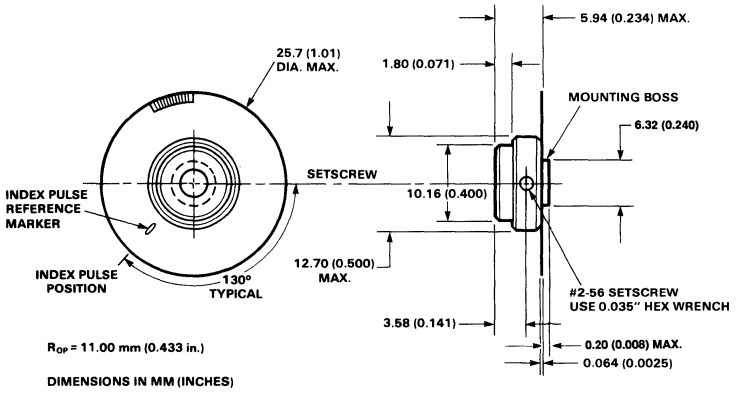


Figure 6. HEDS-5140 Codewheel Used with HEDS-9140.

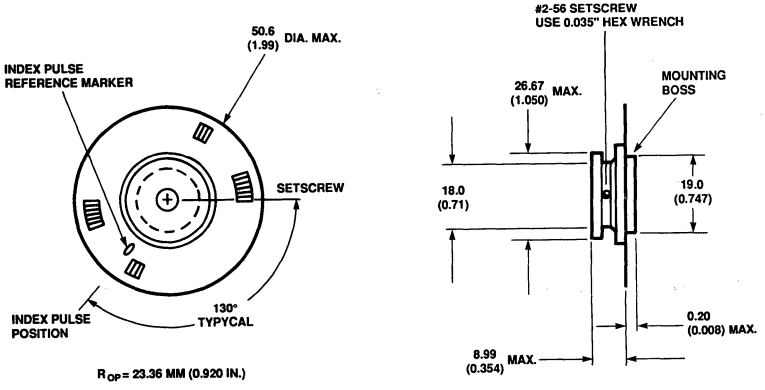


Figure 7. HEDS-6140 Codewheel Used with HEDS-9040.

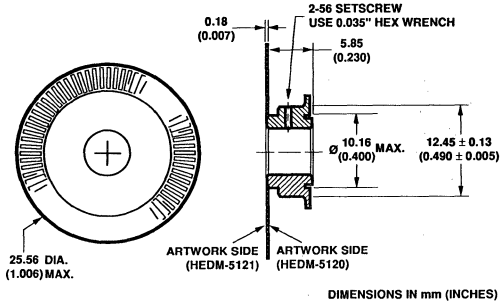


Figure 8. HEDM-5120 Codewheel/HEDM-5121 Codewheel.

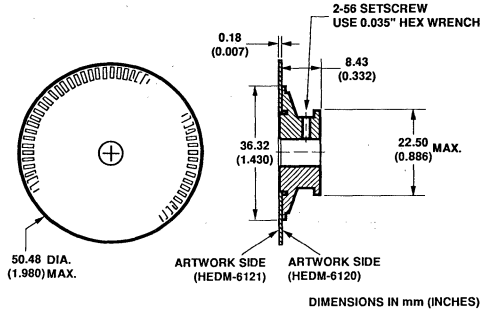


Figure 9.HEDM-6120 Codewheel/HEDM-6121 Codewheel.

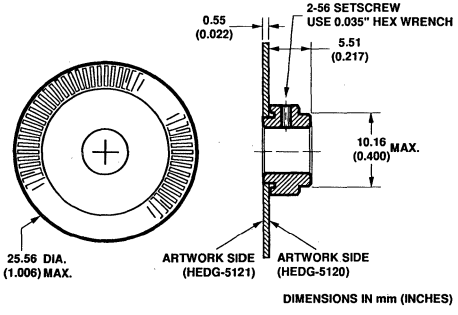


Figure 10. HEDG-5120 Codewheel/HEDG-5121 Codewheel.

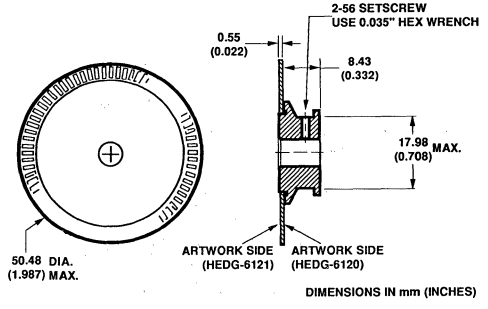


Figure 11. HEDG-6120 Codewheel/HEDG-6121 Codewheel.

Ordering Information

Metal Codewheels

HEDS- 5120 Option ☐☐ Rop = 11 mm, 2 channels

Resolution (Cycles/Rev)		Shaft Diameter	
K - 96 CPR	G - 360 CPR	01 - 2 mm.	11 - 4 mm
C - 100 CHR	H - 400 CPR	02 - 3 mm	14 - 5 mm
D - 192 CPR	A - 500 CPR	03 - 1/8 in.	12 - 6 mm
E - 200 CPR	I - 512 CPR	04 - 5/32 in.	13 - 8 mm
F - 256 CPR		05 - 3/16 in.	
		06 - 1/4 in.	

HEDS- 5140 Option ☐☐ Rop = 11 mm, 3 channels

Resolution (Cycles/Rev)		Shaft Diameter	
C - 100 CPR	H - 400 CPR	01 - 2 mm.	11 - 4 mm
E - 200 CPR	A - 500 CPR	02 - 3 mm	14 - 5 mm
F - 256 CPR	I - 512 CPR	03 - 1/8 in.	12 - 6 mm
G - 360 CPR		04 - 5/32 in.	13 - 8 mm
		05 - 3/16 in.	
		06 - 1/4 in.	

HEDS- 6100 Option ☐☐ Rop = 23 mm, 2 channels

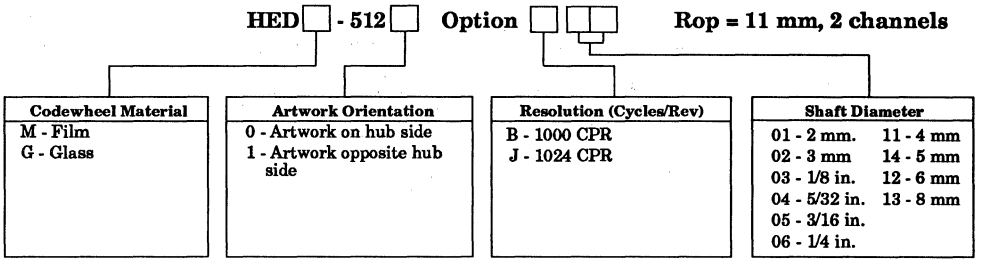
Resolution (Cycles/Rev)	Shaft Diameter	
A - 500 CPR	05 - 3/16 in.	10 - 5/8 in.
B - 1000 CPR	06 - 1/4 in.	11 - 4 mm
	07 - 5/16 in.	12 - 6 mm
	08 - 3/8 in.	13 - 8 mm
	09 - 1/2 in.	

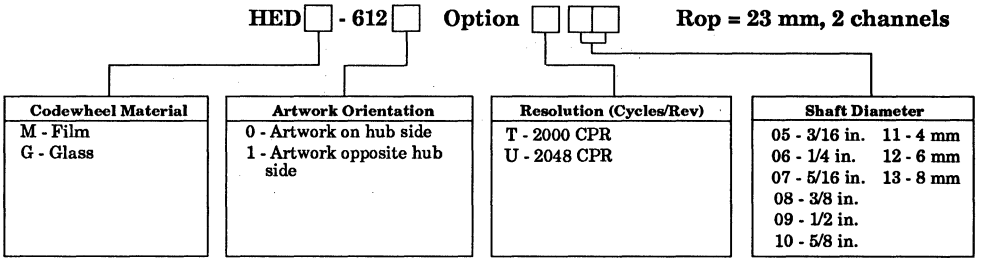
HEDS- 6140 Option ☐☐ Rop = 23 mm, 3 channels

Resolution (Cycles/Rev)	Shaft Diameter	
B - 1000 CPR	05 - 3/16 in.	11 - 4 mm
J - 1024 CPR	06 - 1/4 in.	12 - 6 mm
	07 - 5/16 in.	13 - 8 mm
	08 - 3/8 in.	
	09 - 1/2 in.	
	10 - 5/8 in.	

Ordering Information (continued)

Glass and Film Codewheels





Assembly Tools

HEDS-8905 centering tool for HEDS-9100/9140
HEDS-8906 centering tool for HEDS-9000/9040
HEDS-8901 gap-setting tool for metal and film codewheels
HEDS-8932 gap-setting tool for glass codewheels

Quick Assembly Two and Three Channel Optical Encoders

Technical Data

HEDS-5500/5540
HEDS-5600/5640
New **HEDM-5500/5600**

Features

- **Two Channel Quadrature Output with Optional Index Pulse**
- **Quick and Easy Assembly**
- **No Signal Adjustment Required**
- **External Mounting Ears Available**
- **Low Cost**
- **Resolutions Up to 1024 Counts Per Revolution**
- **Small Size**
- **-40°C to 100°C Operating Temperature**
- **TTL Compatible**
- **Single 5 V Supply**

Description

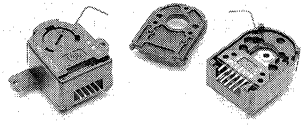
The HEDS-5500/5540, HEDS-5600/5640, and HEDM-5500/5600 are high performance, low cost, two and three channel optical incremental encoders. These encoders emphasize high reliability, high resolution, and easy assembly.

Each encoder contains a lensed LED source, an integrated circuit with detectors and output circuitry, and a codewheel which rotates between the emitter and detector IC. The outputs of the HEDS-5500/5600 and HEDM-5500/ 5600 are two square waves in quadrature. The HEDS-5540 and 5640 also have a third channel index output in addition to the two channel quadrature. This index output is a 90 electrical degree, high true index pulse which is generated once for each full rotation of the codewheel.

The HEDS series utilizes metal codewheels, while the HEDM series utilizes a film codewheel allowing for resolutions to 1024 CPR. The HEDM series is not available with a third channel index.

These encoders may be quickly and easily mounted to a motor. For larger diameter motors, the HEDM-5600, and HEDS-5600/ 5640 feature external mounting ears.

The quadrature signals and the index pulse are accessed through five 0.025 inch square pins located on 0.1 inch centers.



Standard resolutions between 96 and 1024 counts per revolution are presently available. Consult local Hewlett-Packard sales representatives for other resolutions.

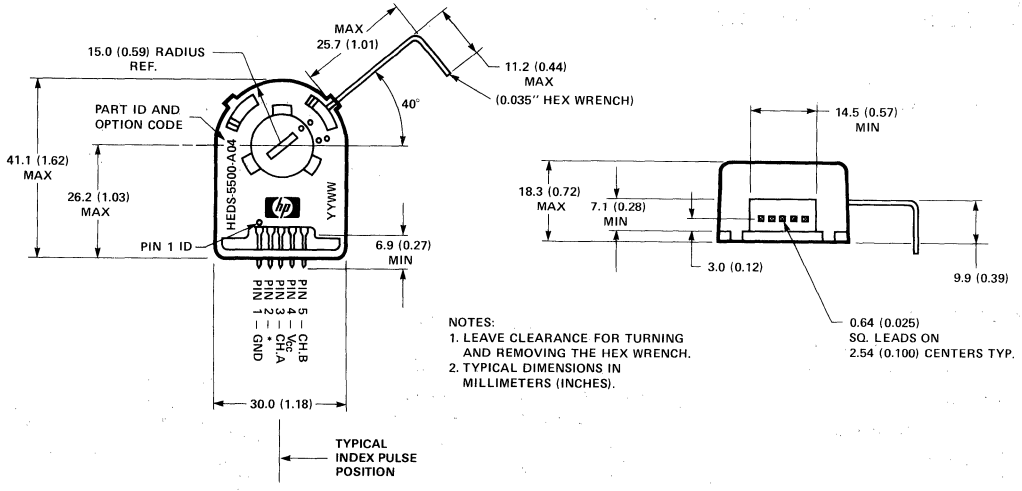
Applications

The HEDS-5500, 5540, 5600, 5640, and the HEDM-5500, 5600 provide motion detection at a low cost, making them ideal for high volume applications. Typical applications include printers, plotters, tape drives, positioning tables, and automatic handlers.

ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

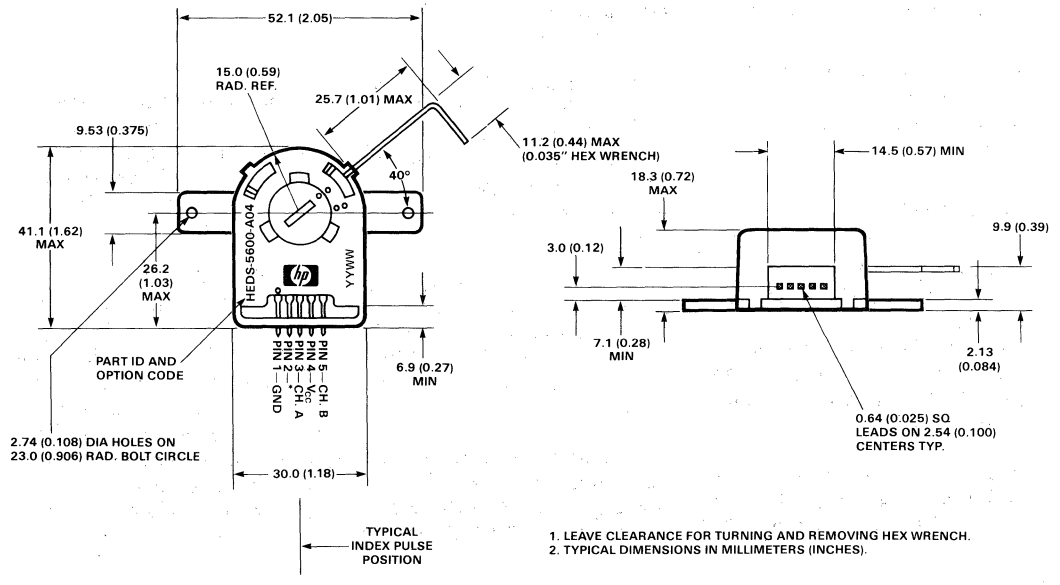
Package Dimensions

HEDS-5500/5540



***Note:** For the HEDS-5500, Pin #2 is a No Connect. For the HEDS-5540, Pin #2 is CH. I, the index output.*

HEDS-5600/5640



***Note:** For the HEDS-5600, Pin #2 is a No Connect. For the HEDS-5640, Pin #2 is CH. I, the index output.*

Theory of Operation

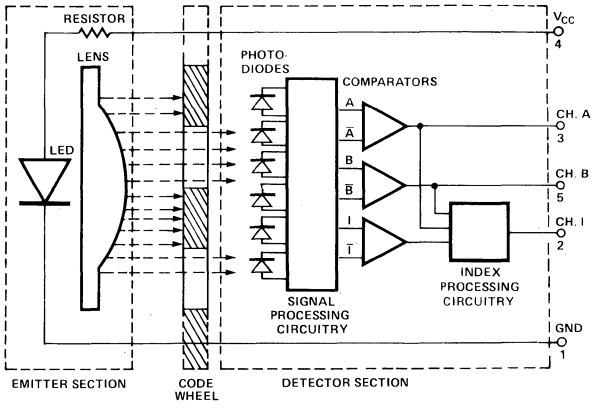
The HEDS-5500, 5540, 5600, 5640, and HEDM-5500, 5600 translate the rotary motion of a shaft into either a two- or a three-channel digital output.

As seen in the block diagram, these encoders contain a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single polycarbonate lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel rotates between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and design of the codewheel. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\overline{A}$, B and $\overline{B}$ (also I and $\overline{I}$ in the HEDS-5540 and 5640). Comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

In the HEDS-5540 and 5640, the output of the comparator for I and $\overline{I}$ is sent to the index processing circuitry along with

Block Diagram



NOTE: CIRCUITRY FOR CH. I IS ONLY IN HEDS-5540 AND 5640 THREE CHANNEL ENCODERS.

the outputs of channels A and B. The final output of channel I is an index pulse P_O which is generated once for each full rotation of the codewheel. This output P_O is a one state width (nominally 90 electrical degrees), high true index pulse which is coincident with the low states of channels A and B.

Definitions

Count (N): The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

One Cycle (C): 360 electrical degrees (°e), 1 bar and window pair.

One Shaft Rotation: 360 mechanical degrees, N cycles.

Position Error ($\Delta\Theta$): The normalized angular difference between the actual shaft position and the position indicated by the encoder cycle count.

Cycle Error (ΔC): An indication of cycle uniformity. The difference between an observed shaft angle which gives rise to one electrical cycle, and the nominal angular increment of 1/N of a revolution.

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Absolute Maximum Ratings

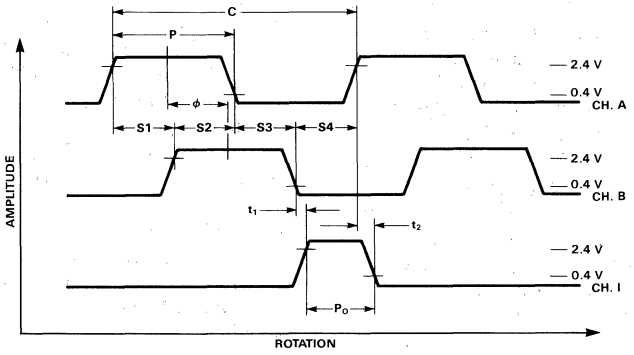
Parameter	HEDS-55XX/56XX	HEDM-550X/560X
Storage Temperature, T_S	-40°C to 100°C	-40°C to +70°C
Operating Temperature, T_A	-40°C to 100°C	-40°C to +70°C
Supply Voltage, V_{CC}	-0.5 V to 7 V	-0.5 V to 7 V
Output Voltage, V_O	-0.5 V to V_{CC}	-0.5 V to V_{CC}
Output Current per Channel, I_{OUT}	-1.0 mA to 5 mA	-1.0 mA to 5 mA
Vibration	20 g, 5 to 1000 Hz	20 g, 5 to 1000 Hz
Shaft Axial Play	±0.25 mm (±0.010 in.)	±0.175 mm (±0.007 in.)
Shaft Eccentricity Plus Radial Play	0.1 mm (0.004 in.) TIR	0.04 mm (0.0015 in.) TIR
Velocity	30,000 RPM	30,000 RPM
Acceleration	250,000 rad/sec^2	250,000 rad/sec^2

Phase Error (Δϕ): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates in the counterclockwise direction (as viewed from the encoder end of the motor), channel A will lead channel B. If the codewheel rotates in the clockwise direction, channel B will lead channel A.

Index Pulse Width (P_O): The number of electrical degrees that an index output is high during one full shaft rotation. This value is nominally 90°e or 1/4 cycle.

Output Waveforms



Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature HEDS Series	T_A	-40		100	°C	
Temperature HEDM Series	T_A	-40		70	°C	non-condensing atmosphere
Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts	Ripple < 100 mV_{p-p}
Load Capacitance	C_L			100	pF	2.7 kΩ pull-up
Count Frequency	f			100	kHz	Velocity (rpm) x N/60
Shaft Perpendicularity Plus Axial Play (HEDS Series)				±0.25 (±0.010)	mm (in.)	6.9 mm (0.27 in.) from mounting surface
Shaft Eccentricity Plus Radial Play (HEDS Series)				0.04 (0.0015)	mm (in.) TIR	6.9 mm (0.27 in.) from mounting surface
Shaft Perpendicularity Plus Axial Play (HEDM Series)				±0.175 (±0.007)	mm (in.)	6.9 mm (0.27 in.) from mounting surface
Shaft Eccentricity Plus Radial Play(HEDM Series)				0.04 (0.0015)	mm (in.) TIR	6.9 mm (0.27 in.) from mounting surface

Note: The module performance is guaranteed to 100 kHz but can operate at higher frequencies. 2.7 kΩ pull-up resistors required for HEDS-5540 and 5640.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances unless otherwise specified. Values are for the worst error over the full rotation.

Part No.	Description		Sym.	Min.	Typ.*	Max.	Units
HEDS-5500 HEDS-5600 (Two Channel)	Pulse Width Error		ΔP		7	45	°e
	Logic State Width Error		ΔS		5	45	°e
	Phase Error		Δϕ		2	20	°e
	Position Error		Δϴ		10	40	min. of arc
	Cycle Error		ΔC		3	5.5	°e
HEDM-5500 HEDM-5600	Pulse Width Error		ΔP		10	45	°e
	Logic State Width Error		ΔS		10	45	°e
	Phase Error		Δϕ		2	15	°e
	Position Error		Δϴ		10	40	min. of arc
	Cycle Error		ΔC		3	7.5	°e
HEDS-5540 HEDS-5640 (Three Channel)	Pulse Width Error		ΔP		5	35	°e
	Logic State Width Error		ΔS		5	35	°e
	Phase Error		Δϕ		2	15	°e
	Position Error		Δϴ		10	40	min. of arc
	Cycle Error		ΔC		3	5.5	°e
	Index Pulse Width		P_O	55	90	125	°e
	CH. I rise after	-25°C to +100°C	t_1	10	100	250	ns
	CH. A or CH. B fall	-40°C to +100°C	t_1	-300	100	250	ns
	CH. I fall after	-25°C to +100°C	t_2	70	150	300	ns
	CH. B or CH. A rise	-40°C to +100°C	t_2	70	150	1000	ns

Note: See Mechanical Characteristics for mounting tolerances.
*Typical values specified at V_{cc} = 5.0 V and 25°C.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range.

Part No.	Parameter	Sym.	Min.	Typ.*	Max.	Units	Notes
HEDS-5500 HEDS-5600	Supply Current High Level Output Voltage Low Level Output Voltage	I_{CC} V_{OH} V_{OL}	 2.4 	17 	40 0.4	mA V V	 I_{OH} = -40 µA max. I_{OL} = 3.2 mA
	Rise Time Fall Time	t_r t_f	 	200 50	 	ns ns	C_L = 25 pF R_L = 11 kΩ pull-up
HEDS-5540 HEDS-5640 HEDM-5500 HEDM-5600	Supply Current High Level Output Voltage Low Level Output Voltage	I_{CC} V_{OH} V_{OL}	30 2.4 	57 	85 0.4	mA V V	 I_{OH} = -200 µA max. I_{OL} = 3.86 mA
	Rise Time Fall Time	t_r t_f	 	180 40	 	ns ns	C_L = 25 pF R_L = 2.7 kΩ pull-up
HEDM-5500 HEDM -5600	Supply Current High Level Output Voltage Low Level Output Voltage	I_{CC} V_{OH} V_{OL}	30 2.4 	57 	85 0.4	mA V V	 I_{OH} = -40 µA max. I_{OL} = 3.86 mA
	Rise Time Fall Time	t_r t_f	 	180 40	 	ns ns	C_L = 25 pF R_L = 3.2 kΩ pull-up

*Typical values specified at V_{CC} = 5.0 V and 25°C.

Mechanical Characteristics

Parameter	Symbol	Dimension	Tolerance [1]	Units
Codewheel Fits These Standard Shaft Diameters		2 3 4 5 6 8	+0.000 -0.015	mm
		5/32 1/8 3/16 1/4	+0.0000 -0.0007	in
Moment of Inertia	J	0.6 (8.0 x 10^{-6})		g-cm^2 (oz-in-s^2)
Required Shaft Length[2]		14.0 (0.55)	±0.5 (±0.02)	mm (in.)
Bolt Circle[3]	2 screw mounting	19.05 (0.750)	±0.13 (±0.005)	mm (in.)
	3 screw mounting	20.90 (0.823)	±0.13 (±0.005)	mm (in.)
	external mounting ears	46.0 (1.811)	±0.13 (±0.005)	mm (in.)
Mounting Screw Size[4]	2 screw mounting	M 2.5 or (2-56)		mm (in.)
	3 screw mounting	M 1.6 or (0-80)		mm (in.)
	external mounting ears	M 2.5 or (2-56)		mm (in.)
Encoder Base Plate Thickness		0.33 (0.130)		mm (in.)
Hub Set Screw		(2-56)		(in.)

Notes:
1. These are tolerances required of the user.
2. The HEDS-55X5 and 56X5, HEDM-5505, 5605 provide an 8.9 mm (0.35 inch) diameter hole through the housing for longer motor shafts. See Ordering Information.
3. The HEDS-5540 and 5640 must be aligned using the aligning pins as specified in Figure 3, or using the alignment tool as shown in "Encoder Mounting and Assembly". See also "Mounting Considerations."
4. The recommended mounting screw torque for 2 screw and external ear mounting is 1.0 kg-cm (0.88 in-lbs). The recommended mounting screw torque for 3 screw mounting is 0.50 kg-cm (0.43 in-lbs).

Electrical Interface

To insure reliable encoding performance, the HEDS-5540 and 5640 three channel encoders require 2.7 kΩ (±10%) pull-up resistors on output pins 2, 3, and 5 (Channels I, A, and B) as shown in Figure 1. These pull-up resistors should be located as close to the encoder as possible (within 4 feet). Each of the three encoder outputs can drive a single TTL load in this configuration.

The HEDS-5500, 5600, and HEDM-5500, 5600 two channel encoders do not normally require pull-up resistors. However, 3.2 kΩ pull-up resistors on output pins 3 and 5 (Channels A and B) are recommended to improve rise times, especially when operating above 100 kHz frequencies.

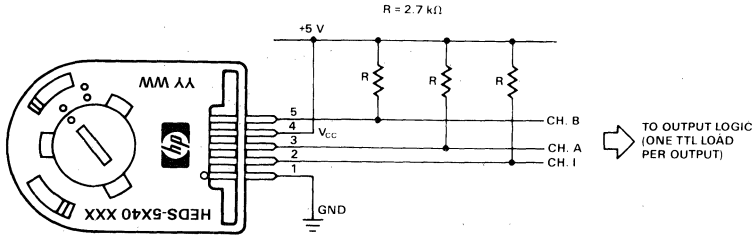


Figure 1. Pull-up Resistors on HEDS-5X40 Encoder Outputs.

Mounting Considerations

The HEDS-5540 and 5640 three channel encoders and the HEDM Series high resolution encoders must be aligned using the aligning pins as specified in Figure 3, or using the HEDS-8910 Alignment Tool as shown in Encoder Mounting and Assembly.

The use of aligning pins or alignment tool is recommended but not required to mount the HEDS-5500 and 5600. If these two channel encoders are attached to a motor with the screw sizes and mounting tolerances specified in the mechanical characteristics section without any additional mounting bosses, the encoder output errors will be within the maximums specified in the encoding characteristics section.

The HEDS-5500 and 5540 can be mounted to a motor using either the two screw or three screw mounting option as shown in Figure 2. The optional aligning pins shown in Figure 3 can be used with either mounting option.

The HEDS-5600, 5640, and HEDM-5600 have external mounting ears which may be used for mounting to larger motor base plates. Figure 4 shows the necessary mounting holes with optional aligning pins and motor boss.

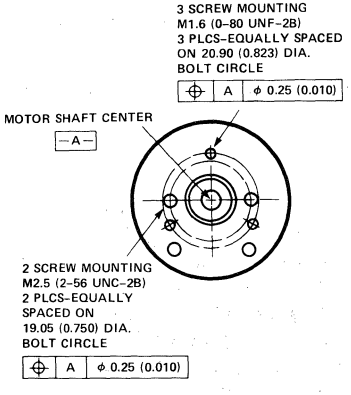


Figure 2. Mounting Holes.

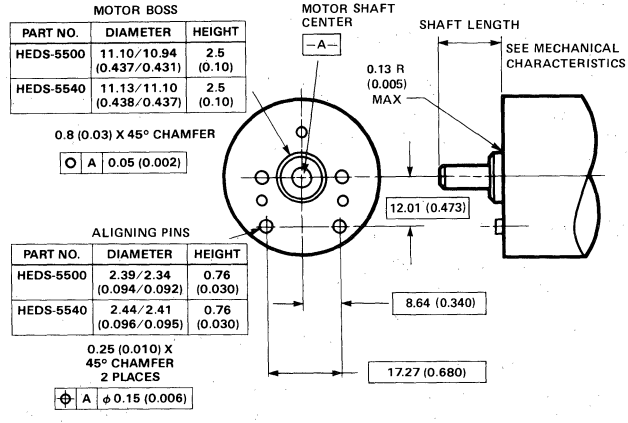


Figure 3. Optional Mounting Aids.

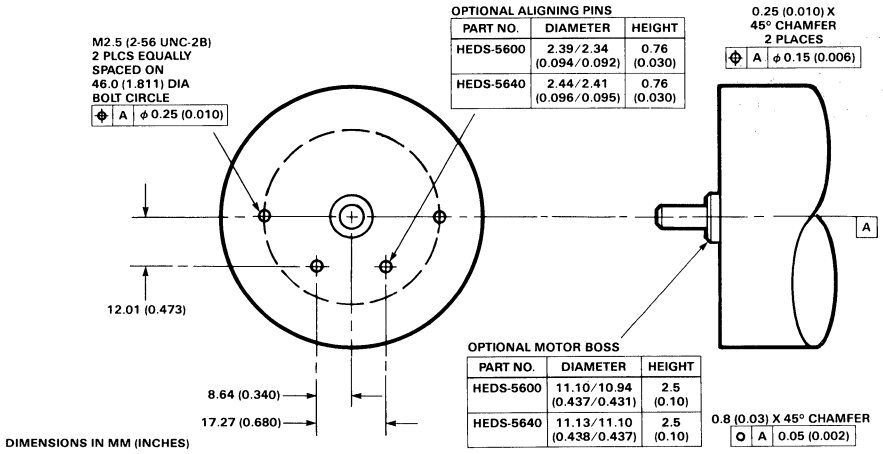
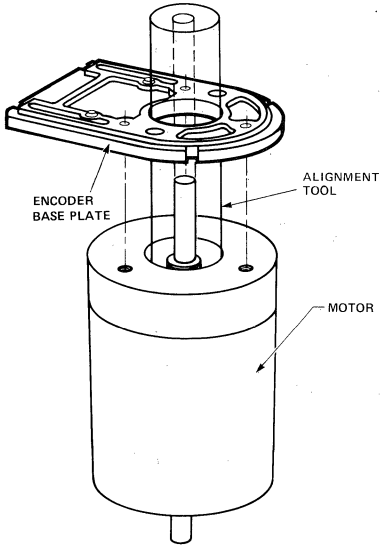


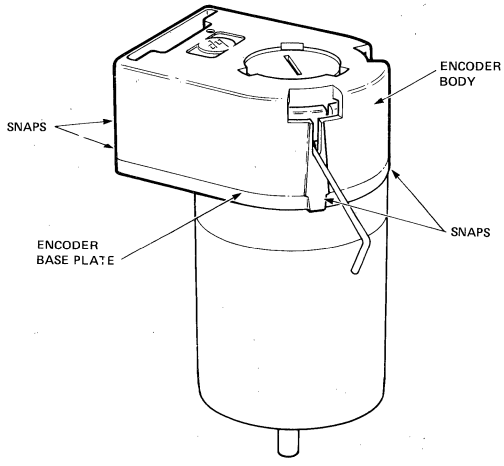
Figure 4. Mounting with External Ears.

Encoder Mounting and Assembly

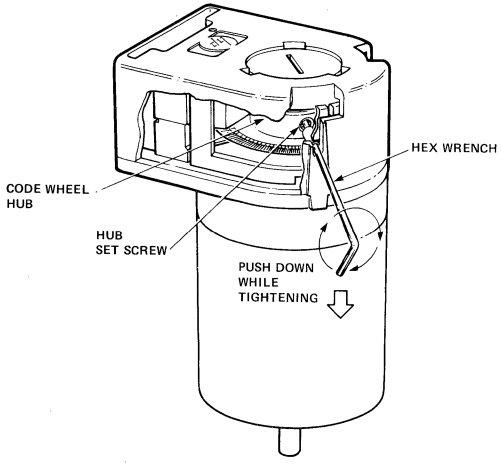


1. For HEDS-5500 and 5600: Mount encoder base plate onto motor. Tighten screws. Go on to step 2.

1a. For HEDS-5540, 5640 and HEDM-5500, 5600: Slip alignment tool onto motor shaft. With alignment tool in place, mount encoder baseplate onto motor as shown above. Tighten screws. Remove alignment tool.



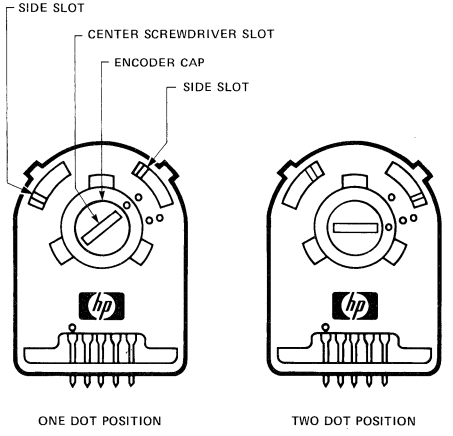
2. Snap encoder body onto base plate locking all 4 snaps.



3a. Push the hex wrench into the body of the encoder to ensure that it is properly seated into the code wheel hub set screws. Then apply a downward force on the end of the hex wrench. This sets the code wheel gap by levering the code wheel hub to its upper position.

3b. While continuing to apply a downward force, rotate the hex wrench in the clockwise direction until the hub set screw is tight against the motor shaft. The hub set screw attaches the code wheel to the motor's shaft.

3c. Remove the hex wrench by pulling it straight out of the encoder body.

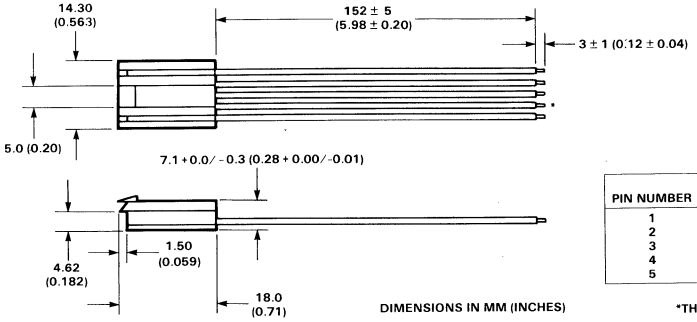


4. Use the center screwdriver slot, or either of the two side slots, to rotate the encoder cap dot clockwise from the one dot position to the two dot position. Do not rotate the encoder cap counterclockwise beyond the one dot position.

The encoder is ready for use!

Connectors

Manufacturer	Part Number
AMP	103686-4 640442-5
Dupont/Berg	65039-032 with 4825X-000 term.
HP (designed to mechanically lock into the HEDS-55XX, HEDM-5XXX Series)	HEDS-8902 (2 ch.) with 4-wire leads
	HEDS-8903 (3 ch.) with 5-wire leads
Molex	2695 series with 2759 series term.

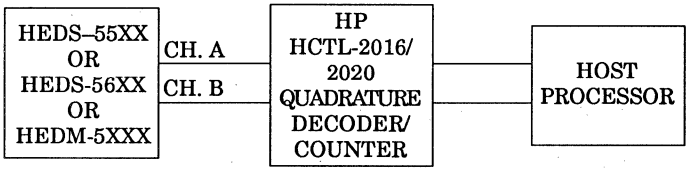


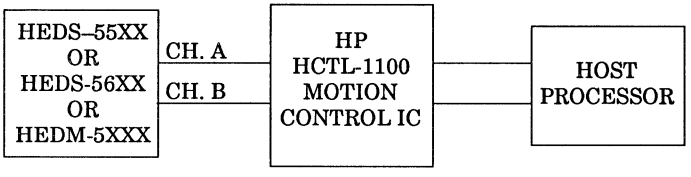
PIN NUMBER	PARAMETER	HEDS-8902 COLORS	HEDS-8903 COLORS
1	GROUND	BLACK	BLACK
2	CH. I	N/A*	BLUE
3	CH. A	WHITE	WHITE
4	V_{CC}	RED	RED
5	CH. B	BROWN	BROWN

*THIS WIRE IS NOT ON HEDS-8902.

Figure 5. HEDS-8902 and 8903 Connectors.

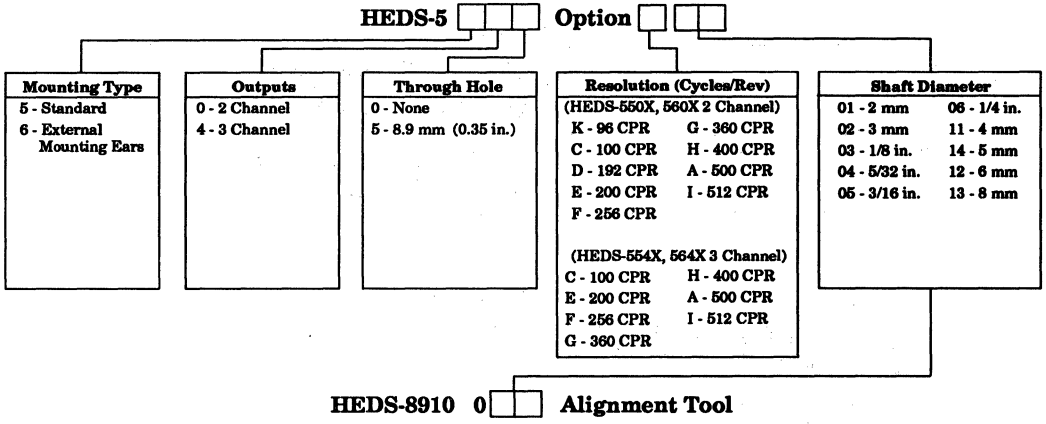
Typical Interfaces





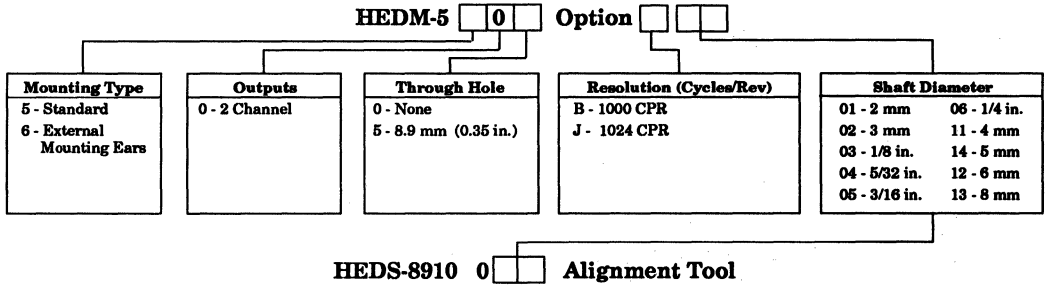
Ordering Information

Encoders with Metal Codewheels



(Included with each order of HEDS-554X/564X three channel encoders)

Encoders with Film Codewheels



(Included with each order of HEDM-550X/560X three channel encoders)

HEWLETT PACKARD

New

Encoder Line Driver Options

Technical Data

HEDL-9000/9100/9200
HEDL-9040/9140
HEDL-550X/554X
HEDL-560X/564X

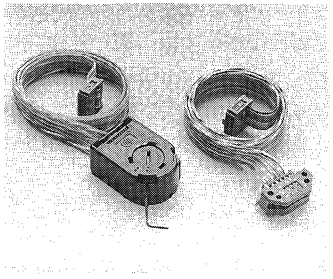
Features

- **Available on Both Encoder Modules (HEDS-9000 Series) and Encoder Kit Housings (HEDS-5500 Series)**
- **Complementary Outputs**
- **High Flex Twisted Pair Cable with Connector**
- **Industry Standard 26LS31 Line Driver IC**
- **Single 5 V Supply**
- **Onboard Bypass Capacitor**

Description

Line Driver options are available on the HEDS-55XX/56XX series and the HEDS-9000/9100/9200/9040/9140 series encoders. The line driver option offers enhanced performance when the encoder is used in noisy environments, or when it is required to drive long distances.

This option utilizes an industry standard line driver IC (26LS31) which provides complementary outputs for each encoder channel. Thus, the output of the line driver encoder is A, $\overline{A}$, B, $\overline{B}$ and I/$\overline{I}$ for three channel versions. In addition, this option comes standard with a 10 conductor flat ribbon cable with complementary outputs in twisted pairs – providing increased noise immunity. Suggested line receivers are 26LS32 and 26LS33.



For additional information, please refer to:
HEDS-5500/5540/5600/5640 data sheet,
HEDS-90X0/91X0/92X0 data sheets,
HEDS-9000 series extended resolution data sheet, and
26LS31 data sheet.

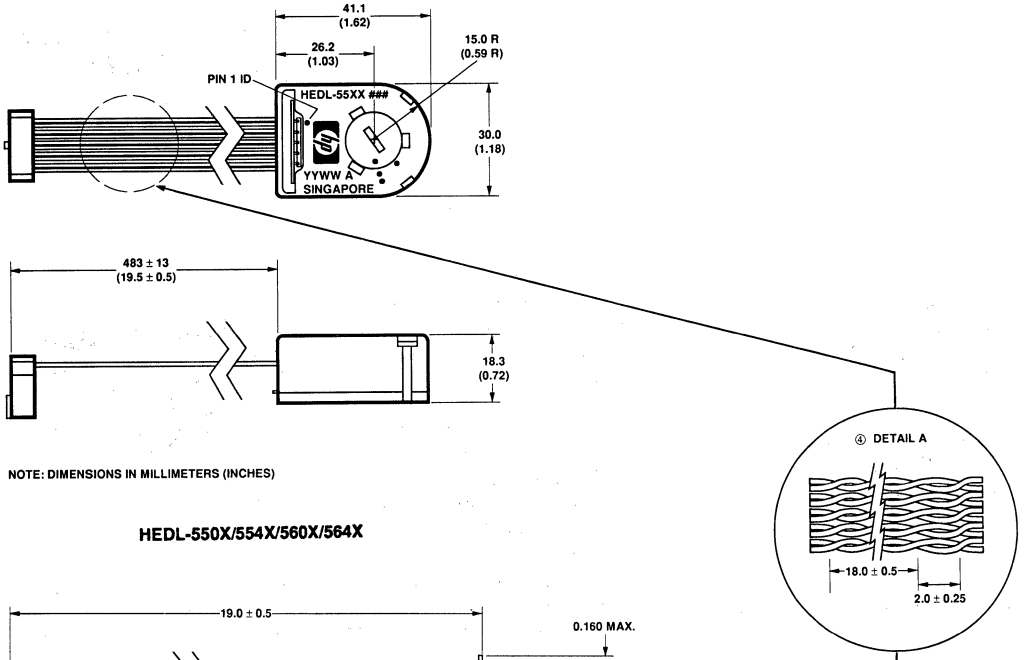
Device Characteristics

Option	Characteristic	Notes
Termination	10 conductor twisted pair cable with 10 position IDC Berg connector	See pinout
Electrical Outputs	Complementary outputs: A, $\overline{A}$, B, $\overline{B}$, I, $\overline{I}$	I and $\overline{I}$ available only on three channel encoders
Line Driver Components	26LS31 line driver IC, decoupling capacitor on PC board.	
Operating Temperature Range	0° C to 70° C	100° C available. Contact factory
Storage Temperature	-40° C to 70° C	

ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

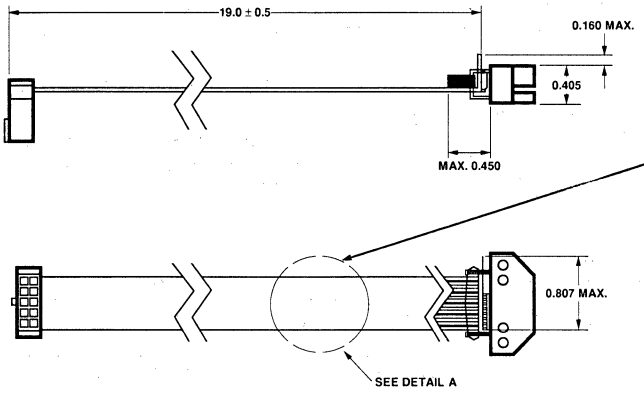
Line Driver Package Dimensions

For Detailed Dimensions on encoder packages, please refer to the respective data sheets.



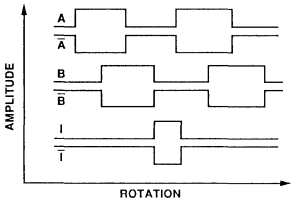
NOTE: DIMENSIONS IN MILLIMETERS (INCHES)

HEDL-550X/554X/560X/564X

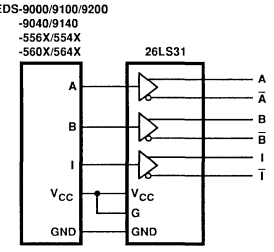


HEDL-9000/9100/9200/9040/9140

Waveforms



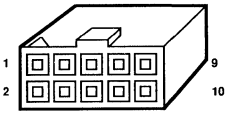
Block Diagram



Pinouts

10-PIN CONNECTOR

NO.	COLOR	PARAMETER
1	BROWN	NC
2	RED	V_{CC} (+ 5 V)
3	ORANGE	GND
4	YELLOW	NC
5	GREEN	Ā
6	BLUE	A
7	VIOLET	B̄
8	GREY	B
9	WHITE	Ī (INDEX)
10	BLACK	I (INDEX)



10 POSITION IDC CONNECTOR
CENTER POLARIZED.

Note: I/Ī only available on the HEDL/554X/564X/904X/914X three channel encoders.

Line Driver Base Parts Available:

Line Driver Base Part	Description	Refer to the following encoder data sheet for additional information and option codes (XXX = resolution and/or shaft size).
HEDL-5500#XXX	HEDS-5500#XXX with Line Driver/Cable/Connector	HEDS-5500/5540 HEDS-5600/5640
HEDL-5505#XXX	HEDS-5505#XXX with Line Driver/Cable/Connector	
HEDL-5540#XXX	HEDS-5540#XXX with Line Driver/Cable/Connector	
HEDL-5545#XXX	HEDS-5545#XXX with Line Driver/Cable/Connector	
HEDL-5600#XXX	HEDS-5600#XXX with Line Driver/Cable/Connector	
HEDL-5605#XXX	HEDS-5605#XXX with Line Driver/Cable/Connector	
HEDL-5640#XXX	HEDS-5640#XXX with Line Driver/Cable/Connector	
HEDL-5645#XXX	HEDS-5645#XXX with Line Driver/Cable/Connector	
HEDL-9000#XXX	HEDS-9000#XXX with Line Driver/Cable/Connector	HEDS-9000/9100/9200 HEDS-9040/9140 HEDS-9000/9100/9200 Extended Resolution
HEDL-9040#XXX	HEDS-9040#XXX with Line Driver/Cable/Connector	
HEDL-9100#XXX	HEDS-9100#XXX with Line Driver/Cable/Connector	
HEDL-9140#XXX	HEDS-9140#XXX with Line Driver/Cable/Connector	
HEDL-9200#XXX	HEDS-9200#XXX with Line Driver/Cable/Connector	

Ordering Information:

To identify the line driver option when ordering an encoder, simply use the "HEDL" base (instead of "HEDS").

HEWLETT PACKARD

Miniature Panel Mount Optical Encoder

Technical Data

HRPG Series

Features

- **Miniature Size**
- **Smooth Turning and Detented Options**
- **Multiple Mounting Bracket Options**
- **Uses Optical Reflective Technology**
- **Quadrature Digital Output**
- **Small Footprint for Versatile Mounting**
- **TTL Compatible**

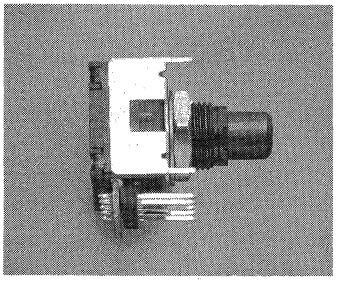
Description

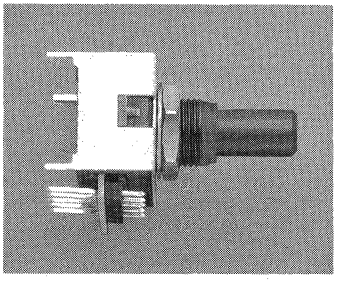
The HRPG series is a family of miniature panel mount optical encoders, also known as Rotary Pulse Generators (RPG) and digital potentiometers. The HRPG is designed to be mounted on a front panel and used as a rotary, data-entry device. The HRPG is very flexible for numerous applications due to the many configuration options available. These options include detents or smooth, multiple terminations, versatile mounting capabilities, and different shaft configurations.

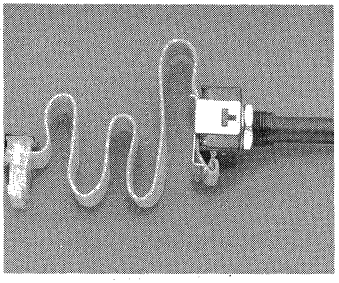
The HRPG uses optical reflective technology providing accuracy and reliability to the encoder. An LED emits a beam of light onto the specular codewheel surface. When the light strikes the surface, it projects the image of the codewheel back on the photo-detector, causing the output to change. The entire detector circuit is on one IC, thus the part is less sensitive to temperature and other environmental variations.

Applications

Typical applications for the Rotary Pulse Generator include front panel instruments, audio/visual boards, and other devices requiring digital output from a turning knob.







Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	+85	°C	
Operating Temperature	T_A	0	+70	°C	
Vibration			20	g	20 Hz to 2 kHz
Supply Voltage	V_{CC}	-0.5	7	V	
Output Voltage	V_O	-0.5	V_{CC}	V	
Output Current Per Channel	I_O	-1	5	mA	
Shaft Load – Axial			4.0	N	10^6 Revolutions
Shaft Load – Radial			0.1	Nm	10^6 Revolutions
Revolution Life		10^6		Rev	At Maximum Loads

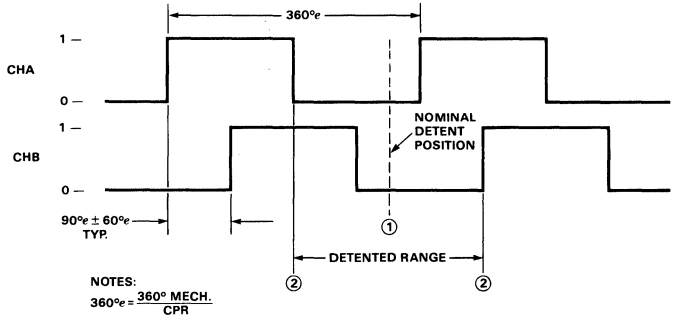
Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	0	+70	°C	Non Condensing Atmosphere
Supply Voltage	V_{CC}	4.5	5.5	V	Ripple < 100 mV_{P-P}
Rotation Speed – Detented			200	RPM	
– Smooth			300	RPM	

Electrical Characteristics
Over Recommended Operating Range

Parameter	Symbol	Min.	Max.	Units	Notes
Supply Current	I_{CC}		40	mA	
High Level Output Voltage	V_{OH}	2.4		V	I_{OH} = - 40 µA Max.
Low Level Output Voltage	V_{OL}		0.4	V	I_{OL} = 3.2 mA

Output Waveforms



NOTES:

$360°e = \frac{360° \text{ MECH.}}{CPR}$

CHANNEL A LEADS CHANNEL B FOR CLOCKWISE ROTATION
CHANNEL B LEADS CHANNEL A FOR COUNTERCLOCKWISE ROTATION

1. FOR HRPG-ADXX #XXX THE NOMINAL DETENT POSITION IS CENTERED AROUND LOW-LOW STATE (CHA = 0, CHB = 0).
2. DETENT POSITION WILL LIE WITHIN THESE BOUNDARIES, NEVER IN HIGH-HIGH STATE (CHA = 1, CHB = 1).

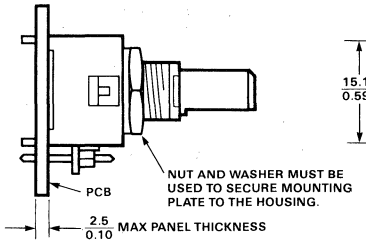
Mechanical Configurations

Termination Options

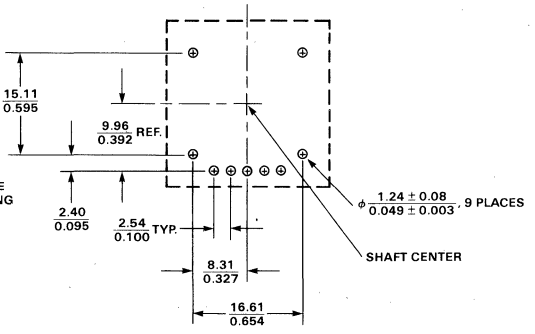
Option R – Pins Rear with Bracket

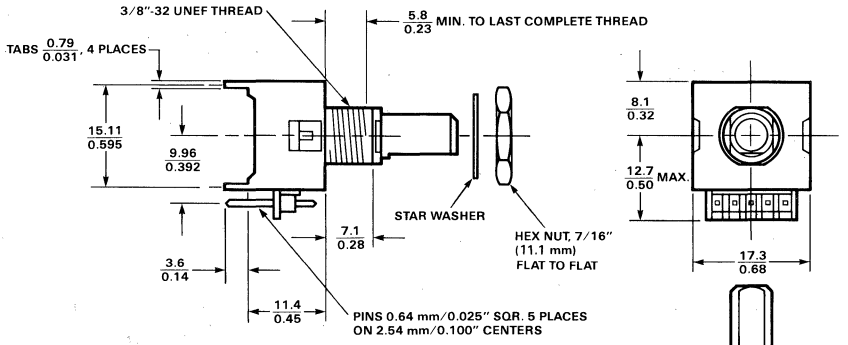
HRPG-AXXX#XXR

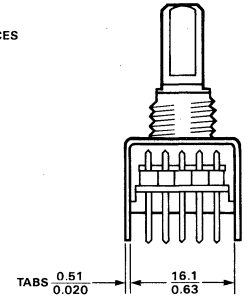
SUGGESTED CONFIGURATION



PCB MOUNTING DIMENSIONS







1. GROUND (DOT ON BOTTOM)
2. CHANNEL B
3. V_{CC} (+5 VOLTS)
4. CHANNEL A
5. SHIELD (HOUSING GROUND)

NOTES:

DIMENSIONS ARE: mm / INCHES

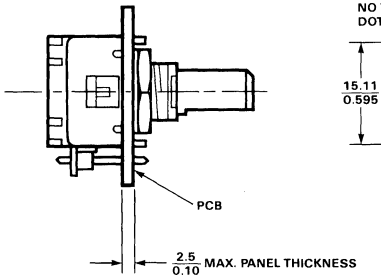
TOLERANCES ARE: X ± 0.25 mm / .XX ± 0.01"

.XX ± 0.13 mm / .XXX ± 0.005"

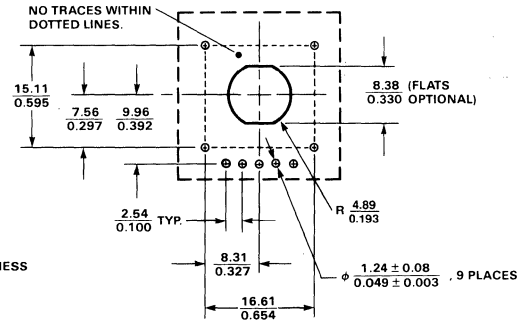
SHIELD IS FOR HOUSING ESD PATH ONLY

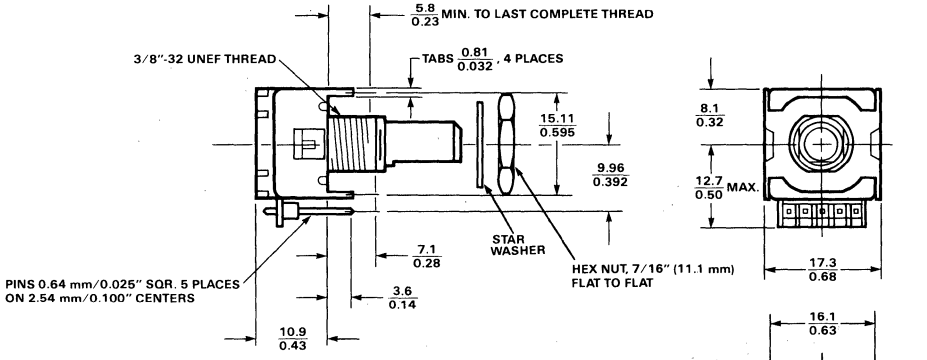
Option F – Pins Front with Bracket
HRPG-AXXX#XXF

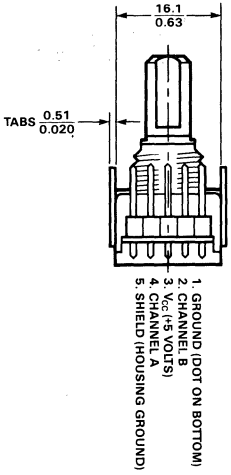
SUGGESTED CONFIGURATION



PCB MOUNTING DIMENSIONS



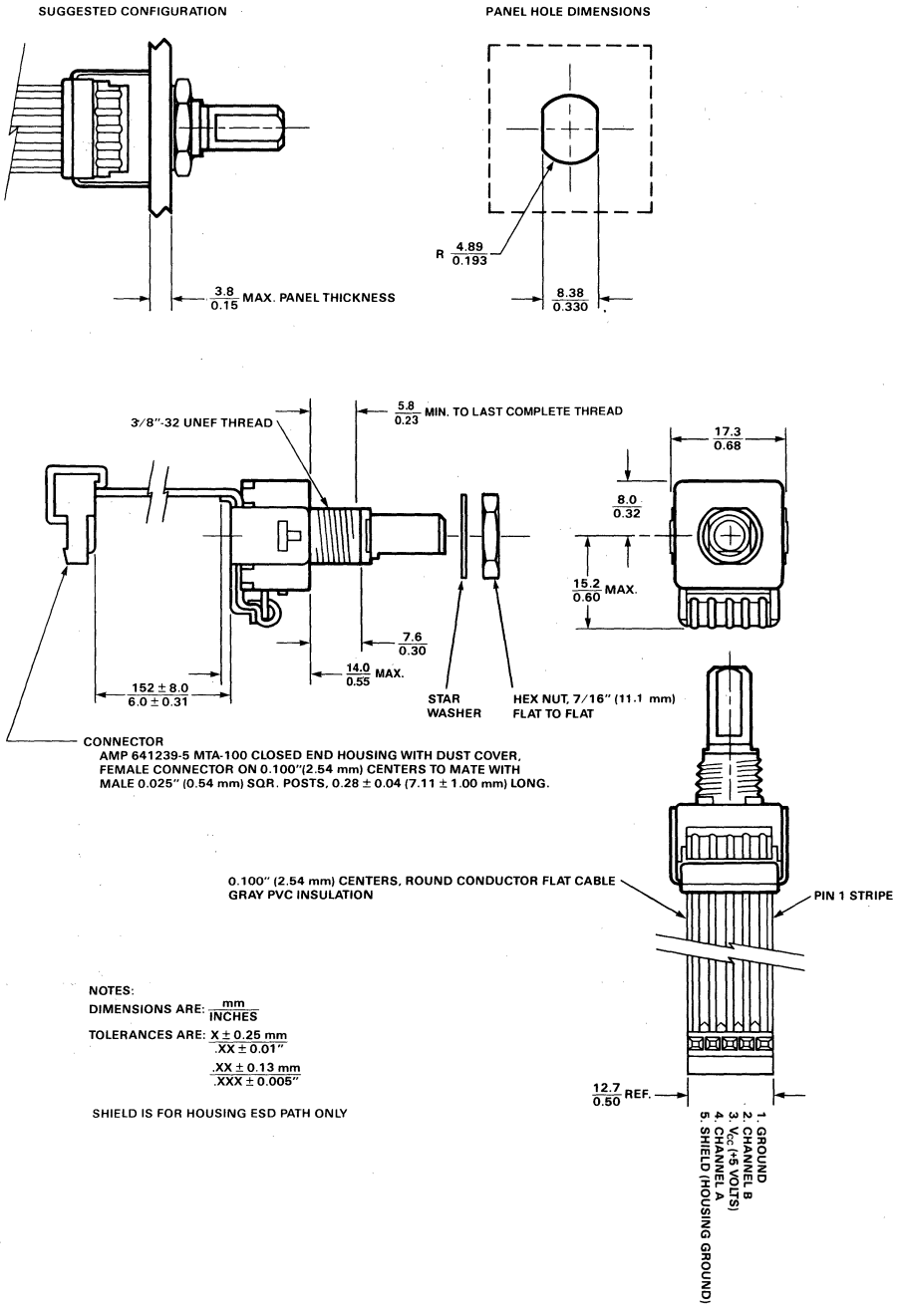




NOTES:
DIMENSIONS ARE: mm / INCHES
TOLERANCES ARE: X ± 0.25 mm / .XX ± 0.01"
.XX ± 0.13 mm / .XXX ± 0.005"

SHIELD IS FOR HOUSING ESD PATH ONLY

Option C – Cable Connector with Strain Relief
HRPG-AXXX#XXC

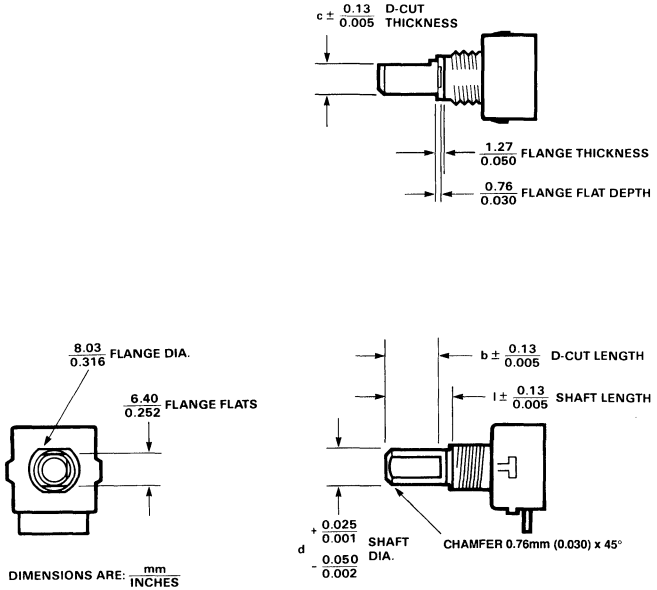


NOTES:
DIMENSIONS ARE: mm / INCHES
TOLERANCES ARE: X ± 0.25 mm / .XX ± 0.01"
.XX ± 0.13 mm / .XXX ± 0.005"

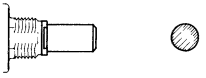
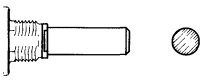
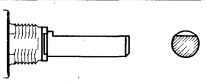
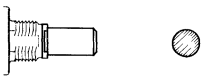
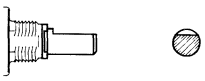
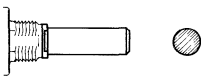
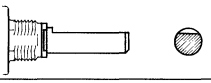
SHIELD IS FOR HOUSING ESD PATH ONLY

Shaft Configurations

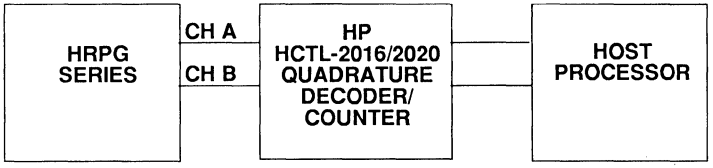
Shaft Dimensions (D-cut shown also)



Shaft Options Available

Option #	Shaft Length (l)	Shaft Diameter (d)	D-Cut Thickness (c)	D-Cut Length (b)	Sketch (not to scale)
11	0.30"	0.251"	–	–	
13	0.30"	0.250"	0.225"	0.230"	
14	0.50"	0.251"	–	–	
16	0.50"	0.250"	0.225"	0.400"	
17	0.80"	0.251"	–	–	
19	0.80"	0.250"	0.225"	0.700"	
51	7.6 mm	6.02 mm	–	–	
53	7.6 mm	6.00 mm	5.33 mm	5.84 mm	
54	12.7 mm	6.02 mm	–	–	
56	12.7 mm	6.00 mm	5.33 mm	10.16 mm	
57	20.32 mm	6.02 mm	–	–	
59	20.32 mm	6.00 mm	5.33 mm	17.78 mm	

Typical Interface



Ordering Information

HRPG - A □□□ # □□□

Shaft Feel / Resolution

S16 – Smooth 16CPR
D16 – Detented 16CPR*
S32 – Smooth 32CPR
D32 – Detented 32CPR*
S64 – Smooth 64CPR
SCA – Smooth 120CPR

Mechanical Configuration

11 – 0.3" long, 0.25" dia.
13 – 0.3" long, 0.25" dia. D-cut
14 – 0.5" long, 0.25" dia.
16 – 0.5" long, 0.25" dia. D-cut
17 – 0.8" long, 0.25" dia.
19 – 0.8" long, 0.25" dia. D-cut
51 – 7.6 mm long, 6 mm dia.
53 – 7.6 mm long, 6 mm dia. D-cut
54 – 12.7 mm long, 6 mm dia.
56 – 12.7 mm long, 6 mm dia. D-cut
57 – 20.3 mm long, 6 mm dia.
59 – 20.3 mm long, 6 mm dia. D-cut

Termination

F – Pins Front with Bracket
R – Pins Rear with Bracket
C – Cable Connector with Strain Relief

*Note: When ordering detented versions, a D-cut shaft is recommended.

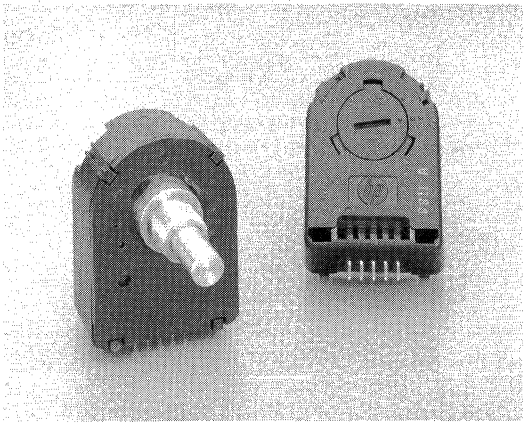
HEWLETT PACKARD

PANEL MOUNT OPTICAL ENCODER

HEDS-5700 SERIES

Features

- **AVAILABLE WITH OR WITHOUT STATIC DRAG FOR MANUAL OR MECHANIZED OPERATION**
- **HIGH RESOLUTION - UP TO 512 CPR**
- **LONG ROTATIONAL LIFE, >1 MILLION REVS**
- **-20 TO 85 °C OPERATING TEMPERATURE RANGE**
- **TTL QUADRATURE OUTPUT**
- **SINGLE 5V SUPPLY**
- **AVAILABLE WITH COLOR CODED LEADS**



Description

The HEDS-5700 series is a family of low cost, high performance, optical incremental encoders with mounted shafts and bushings. The HEDS-5700 is available with tactile feedback for hand operated panel mount applications, or with a free spinning shaft for applications requiring a pre-assembled encoder for position sensing.

The encoder contains a collimated LED light source and special detector circuit which allows for high resolution, excellent encoding performance, long rotational life, and increased reliability. The unit outputs two digital waveforms which are 90 degrees out of phase to provide position and direction information.

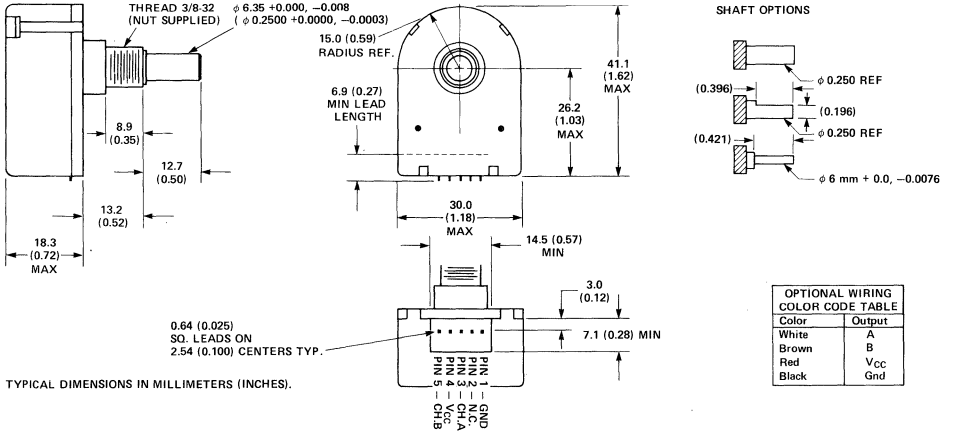
The HEDS-5700 is quickly and easily mounted to a front panel using the threaded bushing, or it can be directly coupled to a motor shaft (or gear train) for position sensing applications.

Applications

The HEDS-5700 with the static drag option is best suited for applications requiring digital information from a manually operated knob. Typical front panel applications include instruments, CAD/CAM systems, and audio/video control boards.

The HEDS-5700 without static drag (free spinning) is best suited for low speed, mechanized operations. Typical applications are copiers, X-Y tables, and assembly line equipment.

Package Dimensions



TYPICAL DIMENSIONS IN MILLIMETERS (INCHES).

OPTIONAL WIRING COLOR CODE TABLE	
Color	Output
White	A
Brown	B
Red	V_{CC}
Black	Gnd

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	+85	°C	
Operating Temperature	T_a	-20	+85	°C	
Vibration			20	g	20Hz - 2kHz
Supply Voltage	V_{CC}	-0.5	7	V	
Output Voltage	V_O	-0.5	V_{CC}	V	
Output Current Per Channel	I_O	-1	5	mA	
Shaft Load - Axial			1	lb	
- Radial			1	lb	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	-20	+85	°C	Non Condensing Atmosphere
Suppy Voltage	V_{CC}	4.5	5.5	V	Ripple <100mV_{p-p}
Rotation Speed - Drag			300	RPM	
- Free Spinning			2000	RPM	

Electrical Characteristics Over Recommended Operating Range, Typical at 25°C

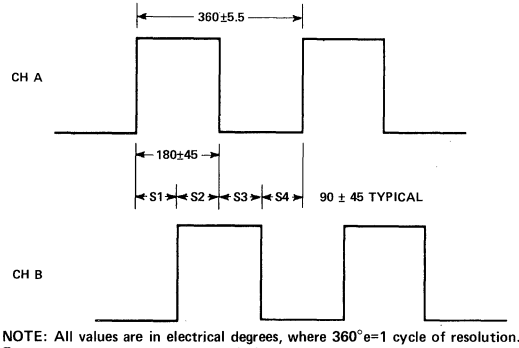
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		17	40	mA	
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40μA Max.
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2mA

Note: If more source current is required, use a 3.2K pullup resistor on each output.

Mechanical Characteristics

Parameter	Min.	Typ.	Max.	Units	Notes
Starting Torque - Static Drag		0.47		oz in	
- Free Spinning			0.14	oz in	
Dynamic Drag - Static Drag		1.1		oz in	100 RPM
- Free Spinning		0.70		oz in	2000 RPM
Rotational Life - Static Drag	1 x 10^6			Revolutions	1 lb Load
- Free Spinning	12 x 10^6			Revolutions	4 oz Radial Load
Mounting Torque of Nut			13	lb in	

Output Waveforms



NOTE: All values are in electrical degrees, where 360°e=1 cycle of resolution.
Errors are worst case over one revolution.
CH B leads CH A for counterclockwise rotation.
CH A leads CH B for clockwise rotation.

Ordering Information

HEDS-570□-□□□

Mechanical Configuration
0 - Pins
1 - 6" Color Coded Leads

Shaft Configuration
0 - 1/4" dia.with no flat
1 - 6mm dia.with no flat
2 - 1/4" dia.with flat

Resolutions
(Cycles Per Revolution)
K=96 CPR G=360 CPR
C=100 CPR H=400 CPR
D=192 CPR A=500 CPR
E=200 CPR I=512 CPR
F=256 CPR

Drag Option
0 - Free Spinning
1 - Static Drag

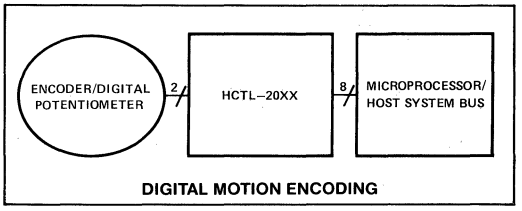
HEWLETT PACKARD

QUADRATURE DECODER/ COUNTER INTERFACE ICs

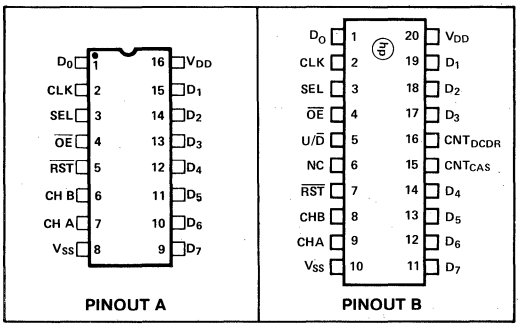
HCTL-2000
HCTL-2016
HCTL-2020

Features

- **INTERFACES ENCODER TO MICROPROCESSOR**
- **14 MHz CLOCK OPERATION**
- **FULL 4X DECODE**
- **HIGH NOISE IMMUNITY:**
  SCHMITT TRIGGER INPUTS
  DIGITAL NOISE FILTER
- **12 OR 16-BIT BINARY UP/DOWN COUNTER**
- **LATCHED OUTPUTS**
- **8-BIT TRISTATE INTERFACE**
- **8, 12, OR 16-BIT OPERATING MODES**
- **QUADRATURE DECODER OUTPUT SIGNALS, UP/DOWN AND COUNT**
- **CASCADE OUTPUT SIGNALS, UP/DOWN AND COUNT**
- **SUBSTANTIALLY REDUCED SYSTEM SOFTWARE**



DIGITAL MOTION ENCODING



PINOUT A **PINOUT B**

Description

The HCTL-2000, 2016, 2020 are CMOS ICs that perform the quadrature decoder, counter, and bus interface function. The HCTL-20XX family is designed to improve system performance in digital closed loop motion control systems and digital data input systems. It does this by shifting time intensive quadrature decoder functions to a cost effective hardware solution. The entire HCTL-20XX family consists of a 4x quadrature decoder, a binary up/down state counter, and an 8-bit bus interface. The use of Schmitt-triggered CMOS inputs and input noise filters allows reliable operation in noisy environments. The HCTL-2000 contains a 12-bit counter. The HCTL-2016 and 2020 contain a 16-bit counter. The HCTL-2020 also contains quadrature decoder output signals and cascade signals for use with many standard counter ICs. The HCTL-20XX family provides LSTTL compatible tri-state output buffers. Operation is specified for a temperature range from -40 to +85°C at clock frequencies up to 14 MHz.

Applications

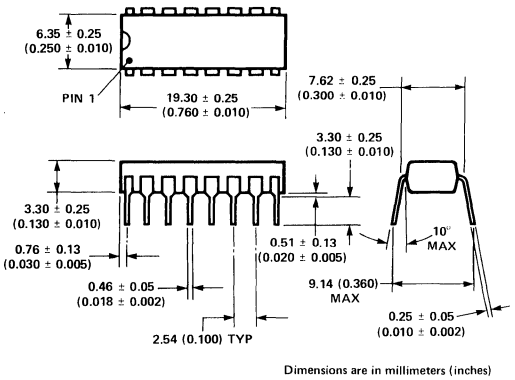
- **INTERFACE QUADRATURE INCREMENTAL ENCODERS TO MICROPROCESSORS**
- **INTERFACE DIGITAL POTENTIOMETERS TO DIGITAL DATA INPUT BUSES**

ESD WARNING: Standard CMOS handling precautions should be observed with the HCTL-20XX family ICs.

Devices

Part Number	Description	Package Drawing
HCTL-2000	12-bit counter. 14 MHz clock operation.	A
HCTL-2016	All features of the HCTL-2000. 16-bit counter.	A
HCTL-2020	All features of the HCTL-2016. Quadrature decoder output signals. Cascade output signals.	B

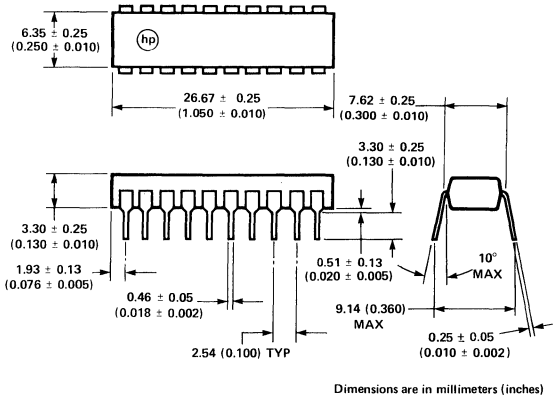
Package Dimensions



Dimensions are in millimeters (inches)

PACKAGE A LEAD FINISH: SOLDER DIPPED

PACKAGE A



Dimensions are in millimeters (inches)

PACKAGE B LEAD FINISH: SOLDER DIPPED

PACKAGE B

Operating Characteristics

Table 1. Absolute Maximum Ratings (All voltages below are referenced to V_{SS})

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	-0.3 to +5.5	V
Input Voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Storage Temperature	T_S	-40 to +125	°C
Operating Temperature	T_A[1]	-40 to +85	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	+4.5 to +5.5	V
Ambient Temperature	T_A[1]	-40 to +85	°C

Table 3. DC Characteristics V_{DD} = 5 V ± 5%; T_A = -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}[2]	Low-Level Input Voltage				1.5	V
V_{IH}[2]	High-Level Input Voltage		3.5			V
V_{T+}	Schmitt-Trigger Positive-Going Threshold			3.5	4.0	V
V_{T-}	Schmitt-Trigger Negative-Going Threshold		1.0	1.5		V
V_H	Schmitt-Trigger Hysteresis		1.0	2.0		V
I_{IN}	Input Current	V_{IN} = V_{SS} or V_{DD}	-10	1	+10	μA
V_{OH}[2]	High-Level Output Voltage	I_{OH} -1.6 mA	2.4	4.5		V
V_{OL}[2]	Low-Level Output Voltage	I_{OL} = +4.8 mA		0.2	0.4	V
I_{OZ}	High-Z Output Leakage Current	V_O = V_{SS} or V_{DD}	-10	1	+10	μA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{SS} or V_{DD}, V_O = HiZ		1	5	μA
C_{IN}	Input Capacitance	Any Input[3]		5		pF
C_{OUT}	Output Capacitance	Any Output[3]		6		pF

Notes:

1. Free Air
2. In general, for any V_{DD} between the allowable limits (+4.5 V to +5.5 V), V_{IL} = 0.3 V_{DD} and V_{IH} = 0.7 V_{DD}; typical values are V_{OH} = V_{DD} - 0.5 V @ I_{OH} = -40 μA and V_{OL} = V_{SS} + 0.2 V @ I_{OL} = 1.6 mA.
3. Including package capacitance.

Functional Pin Description

Table 4. Functional Pin Descriptions

Symbol	Pin 2000/2016	Pin 2020	Description
V_{DD}	16	20	Power Supply
V_{SS}	8	10	Ground
CLK	2	2	CLK is a Schmitt-trigger input for the external clock signal.
CHA CHB	7 6	9 8	CHA and CHB are Schmitt-trigger inputs which accept the outputs from a quadrature encoded source, such as incremental optical shaft encoder. Two channels, A and B, nominally 90 degrees out of phase, are required.
$\overline{RST}$	5	7	This active low Schmitt-trigger input clears the internal position counter and the position latch. It also resets the inhibit logic. $\overline{RST}$ is asynchronous with respect to any other input signals.
$\overline{OE}$	4	4	This CMOS active low input enables the tri-state output buffers. The $\overline{OE}$ and SEL inputs are sampled by the internal inhibit logic on the falling edge of the clock to control the loading of the internal position data latch.
SEL	3	3	This CMOS input directly controls which data byte from the position latch is enabled into the 8-bit tri-state output buffer. As in $\overline{OE}$ above, SEL also controls the internal inhibit logic. **SEL** / **BYTE SELECTED** 0 / High 1 / Low
CNT_{DCDR}		16	A pulse is presented on this LSTTL-compatible output when the quadrature decoder has detected a state transition.
$U/\overline{D}$		5	This LSTTL-compatible output allows the user to determine whether the IC is counting up or down and is intended to be used with the CNT_{DCDR} and CNT_{CAS} outputs. The proper signal U (high level) or $\overline{D}$ (low level) will be present before the rising edge of the CNT_{DCDR} and CNT_{CAS} outputs.
CNT_{CAS}		15	A pulse is presented on this LSTTL-compatible output when the HCTL-2020 internal counter overflows or underflows. The rising edge on this waveform may be used to trigger an external counter.
D0	1	1	These LSTTL-compatible tri-state outputs form an 8-bit output port through which the contents of the 12/16-bit position latch may be read in 2 sequential bytes. The high byte, containing bits 8-15, is read first (on the HCTL-2000, the most significant 4 bits of this byte are set to 0 internally). The lower byte, bits 0-7, is read second.
D1	15	19	
D2	14	18	
D3	13	17	
D4	12	14	
D5	11	13	
D6	10	12	
D7	9	11	
NC		6	Not connected — this pin should be left floating.

Switching Characteristics

Table 5. Switching Characteristics Min/Max specifications at V_{DD} = 5.0 ± 5%, T_A = −40 to + 85°C

	Symbol	Description	Min.	Max.	Units
1	t_{CLK}	Clock period	70		ns
2	t_{CHH}	Pulse width, clock high	28		ns
3	t_{CD}[1]	Delay time, rising edge of clock to valid, updated count information on D0-7		65	ns
4	t_{ODE}	Delay time, $\overline{OE}$ fall to valid data		65	ns
5	t_{ODZ}	Delay time, $\overline{OE}$ rise to Hi-Z state on D0-7		40	ns
6	t_{SDV}	Delay time, SEL valid to stable, selected data byte (delay to High Byte = delay to Low Byte)		65	ns
7	t_{CLH}	Pulse width, clock low	28		ns
8	t_{SS}[2]	Setup time, SEL before clock fall	20		ns
9	t_{OS}[2]	Setup time, $\overline{OE}$ before clock fall	20		ns
10	t_{SH}[2]	Hold time, SEL after clock fall	0		ns
11	t_{OH}[2]	Hold time, $\overline{OE}$ after clock fall	0		ns
12	t_{RST}	Pulse width, $\overline{RST}$ low	28		ns
13	t_{DCD}	Hold time, last position count stable on D0-7 after clock rise	10		ns
14	t_{DSD}	Hold time, last data byte stable after next SEL state change	5		ns
15	t_{DOD}	Hold time, data byte stable after $\overline{OE}$ rise	5		ns
16	t_{UDD}	Delay time, U/$\overline{D}$ valid after clock rise		45	ns
17	t_{CHD}	Delay time, CNT_{DCDR} or CNT_{CAS} high after clock rise		45	ns
18	t_{CLD}	Delay time, CNT_{DCDR} or CNT_{CAS} low after clock fall		45	ns
19	t_{UDH}	Hold time, U/$\overline{D}$ stable after clock rise	10		ns
20	t_{UDCS}	Setup time, U/$\overline{D}$ valid before CNT_{DCDR} or CNT_{CAS} rise	t_{CLK}−45		ns
21	t_{UDCH}	Hold time, U/$\overline{D}$ stable after CNT_{DCDR} or CNT_{CAS} rise	t_{CLK}−45		ns

Notes:

1. t_{CD} specification and waveform assume latch not inhibited.
2. t_{SS}, t_{OS}, t_{SH}, t_{OH} only pertain to proper operation of the inhibit logic. In other cases, such as 8 bit read operations, these setup and hold times do not need to be observed.

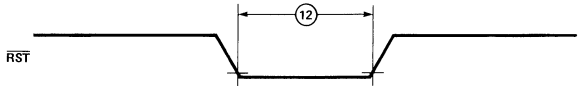


Figure 1. Reset Waveform

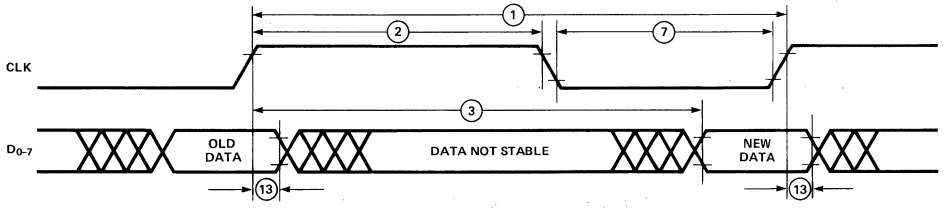


Figure 2. Waveform for Positive Clock Related Delays

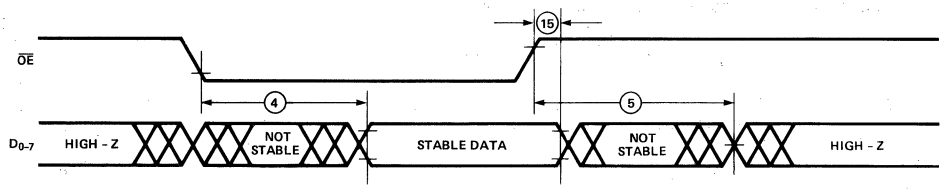


Figure 3. Tri-State Output Timing

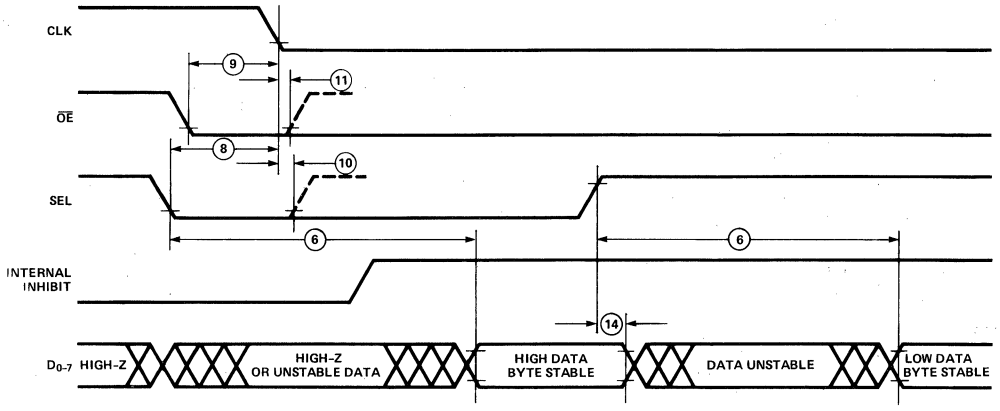


Figure 4. Bus Control Timing

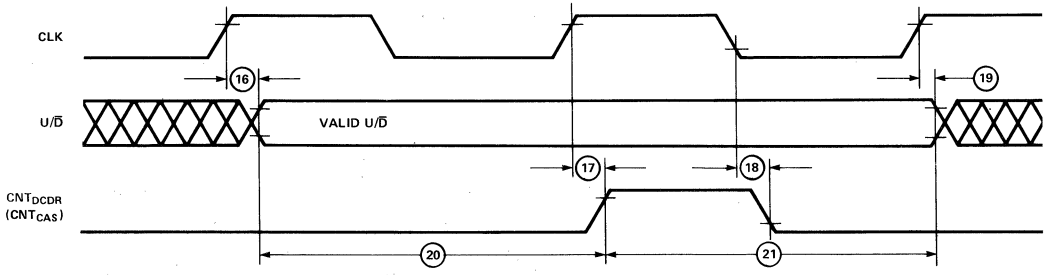


Figure 5. Decoder, Cascade Output Timing (HCTL-2020 only)

Operation

A block diagram of the HCTL-20XX family is shown in Figure 6. The operation of each major function is described in the following sections.

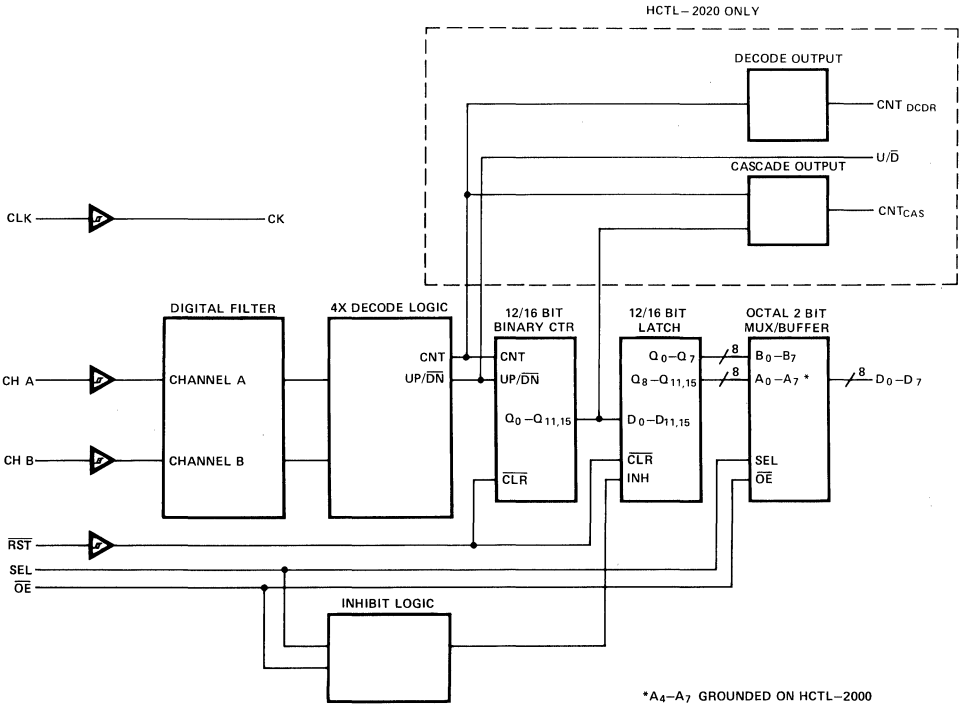


Figure 6. Simplified Logic Diagram

DIGITAL NOISE FILTER

The digital noise filter section is responsible for rejecting noise on the incoming quadrature signals. The input section uses two techniques to implement improved noise rejection. Schmitt-trigger inputs and a three-clock-cycle delay filter combine to reject low level noise and large, short duration noise spikes that typically occur in motor system applications. Both common mode and differential mode noise are rejected. The user benefits from these techniques by improved integrity of the data in the counter. False counts triggered by noise are avoided.

Figure 7 shows the simplified schematic of the input section. The signals are first passed through a Schmitt trigger buffer to address the problem of input signals with slow rise times and low level noise (approximately < 1 V). The cleaned up signals are then passed to a four-bit delay filter. The signals on each channel are sampled on rising clock edges. A time history of the signals is stored in the four-bit shift register. Any change on the input is tested for a stable level being present for three consecutive rising clock edges. Therefore, the filtered output waveforms can change only after an input level has the same value for three consecutive rising clock edges. Refer to Figure 8 which shows the timing diagram. The result of this circuitry is that short noise spikes between rising clock edges are ignored and pulses shorter than two clock periods are rejected.

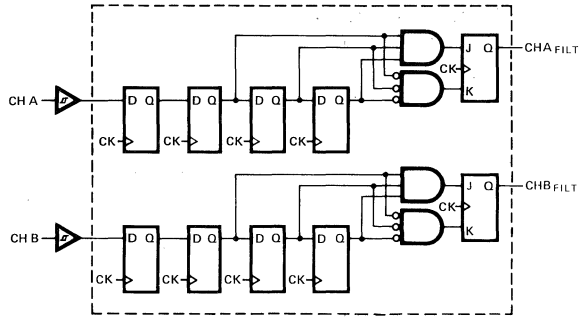


Figure 7. Simplified Digital Noise Filter Logic

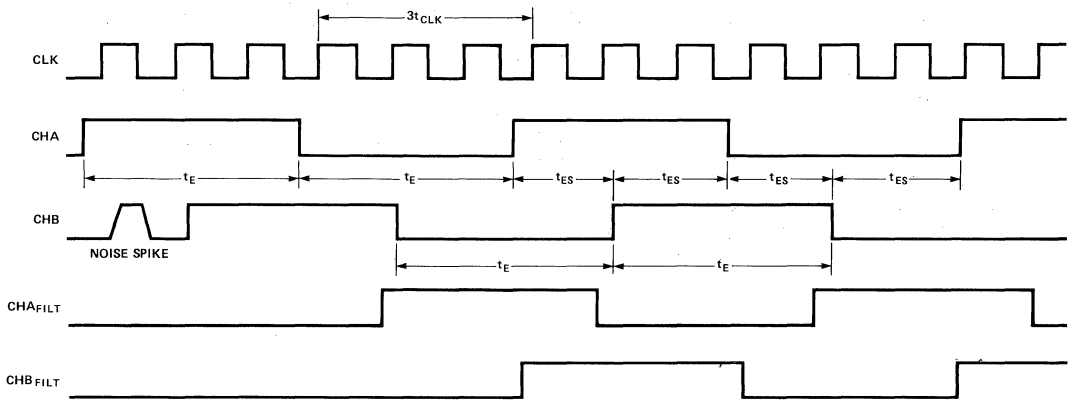


Figure 8. Signal Propagation Through Digital Noise Filter

QUADRATURE DECODER

The quadrature decoder decodes the incoming filtered signals into count information. This circuitry multiplies the resolution of the input signals by a factor of four (4X decoding). When using an encoder for motion sensing, the user benefits from the increased resolution by being able to provide better system control.

The quadrature decoder samples the outputs of the CHA and CHB filters. Based on the past binary state of the two signals and the present state, it outputs a count signal and a direction signal to the internal position counter. In the case of the HCTL-2020, the signals also go to external pins 5 and 16 respectively.

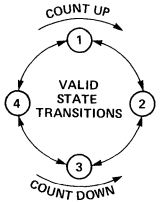
Figure 9 shows the quadrature states and the valid state transitions. Channel A leading channel B results in counting up. Channel B leading channel A results in counting down. Illegal state transitions, caused by faulty encoders or noise severe enough to pass through the filter, will produce an erroneous count.

DESIGN CONSIDERATIONS

The designer should be aware that the operation of the digital filter places a timing constraint on the relationship between incoming quadrature signals and the external clock. Figure 8 shows the timing waveform with an incremental encoder input. Since an input has to be stable for three rising clock edges, the encoder pulse width (t_E - low or high), has to be greater than three clock periods ($3t_{CLK}$). This guarantees that the asynchronous input will be stable during three consecutive rising clock edges. A realistic design also has to take into account finite rise times of the waveforms, asymmetry of the waveforms, and noise. In the presence of large amounts of noise, t_E should be much

greater than $3t_{CLK}$ to allow for the interruption of the consecutive level sampling by the three-bit delay filter. It should be noted that a change on the inputs that is qualified by the filter will internally propagate in a maximum of seven clock periods.

The quadrature decoder circuitry imposes a second timing constraint between the external clock and the input signals. There must be at least one clock period between consecutive quadrature states. As shown in Figure 9, a quadrature state is defined by consecutive edges on both channels. Therefore, t_{ES} (encoder state period) > t_{CLK}. The designer must account for deviations from the nominal 90 degree phasing of input signals to guarantee that t_{ES} > t_{CLK}.



CHA	CHB	STATE
1	0	1
1	1	2
0	1	3
0	0	4

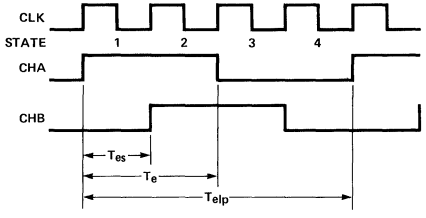


Figure 9. 4x Quadrature Decoding

POSITION COUNTER

This section consists of a 12-bit (HCTL-2000) or 16-bit (HCTL-2016/2020) binary up/down counter which counts on rising clock edges as explained in the Quadrature Decoder Section. All 12 or 16 bits of data are passed to the position data latch. The system can use this count data in several ways:

A. System total range is ≤ 12 or 16 bits, so the count represents "absolute" position.

B. The system is cyclic with ≤ 12 or 16 bits of count per cycle. $\overline{RST}$ is used to reset the counter every cycle and the system uses the data to interpolate within the cycle.

C. System count is > 8, 12 or 16 bits, so the count data is used as a relative or incremental position input for a system software computation of absolute position. In this case counter rollover occurs. In order to prevent loss of position information, the processor must read the outputs of the IC before the count increments one-half of the maximum count capability (i.e. 127, 2047, or 32,767 quadrature counts). Two's-complement arithmetic is normally used to compute position from these periodic position updates. Three modes can be used:

1. The IC can be put in 8-bit mode by tying the SEL line high, thus simplifying IC interface. The outputs must then be read at least once every 127 quadrature counts.
2. The HCTL-2000 can be used in 12-bit mode and sampled at least once every 2047 quadrature counts.
3. The HCTL-2016 or 2020 can be used in 16-bit mode and sampled at least once every 32,767 quadrature counts.

D. The system count is > 16 bits so the HCTL-2020 can be cascaded with other standard counter IC's to give absolute position.

POSITION DATA LATCH

The position data latch is a 12/16-bit latch which captures the position counter output data on each rising clock edge, except when its inputs are disabled by the inhibit logic section during two-byte read operations. The output data is passed to the bus interface section. When active, a signal from the inhibit logic section prevents new data from being captured by the latch, keeping the data stable while successive reads are made through the bus section. The latch is automatically reenabled at the end of these reads. The latch is cleared to 0 asynchronously by the $\overline{RST}$ signal.

INHIBIT LOGIC

The Inhibit Logic Section samples the $\overline{OE}$ and SEL signals on the falling edge of the clock and, in response to certain conditions (see Figure 10 below), inhibits the position data latch. The $\overline{RST}$ signal asynchronously clears the inhibit logic, enabling the latch. A simplified logic diagram of the inhibit circuitry is illustrated in Figure 11.

STEP	SEL	$\overline{OE}$	CLK	INHIBIT SIGNAL	ACTION
1	L	L	⌊	1	SET INHIBIT; READ HIGH BYTE
2	H	L	⌊	1	READ LOW BYTE; STARTS RESET
3	X	H	⌊	0	COMPLETES INHIBIT LOGIC RESET

Figure 10. Two Byte Read Sequence

BUS INTERFACE

The bus interface section consists of a 16 to 8 line multiplexer and an 8-bit, three-state output buffer. The multiplexer allows independent access to the low and high bytes of the position data latch. The SEL and $\overline{OE}$ signals determine which byte is output and whether or not the output bus is in the high-Z state. In the case of the HCTL-2000 the data latch is only 12 bits wide and the upper four bits of the high byte are internally set to zero.

QUADRATURE DECODER OUTPUT (HCTL-2020 ONLY)

The quadrature decoder output section consists of count and up/down outputs derived from the 4X decode logic of the HCTL-2020. When the decoder has detected a count, a pulse, one-half clock cycle long, will be output on the CNT_{DCDR} pin. This output will occur during the clock cycle in which the internal counter is updated. The $U/\overline{D}$ pin will be set to the proper voltage level one clock cycle before the rising edge of the CNT_{DCDR} pulse, and held one clock cycle after the rising edge of the CNT_{DCDR} pulse. These outputs are not affected by the inhibit logic. See Figures 5 and 12 for detailed timing.

CASCADE OUTPUT (HCTL-2020 ONLY)

The cascade output also consists of count and up/down outputs. When the HCTL-2020 internal counter overflows or underflows, a pulse, one-half clock cycle long, will be output on the CNT_{CAS} pin. This output will occur during the clock cycle in which the internal counter is updated. The $U/\overline{D}$ pin will be set to the proper voltage level one clock cycle before the rising edge of the CNT_{CAS} pulse, and held one clock cycle after the rising edge of the CNT_{CAS} pulse. These outputs are not affected by the inhibit logic. See Figures 5 and 12 for detailed timing.

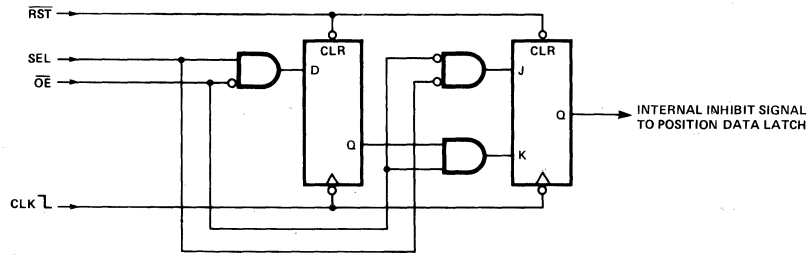
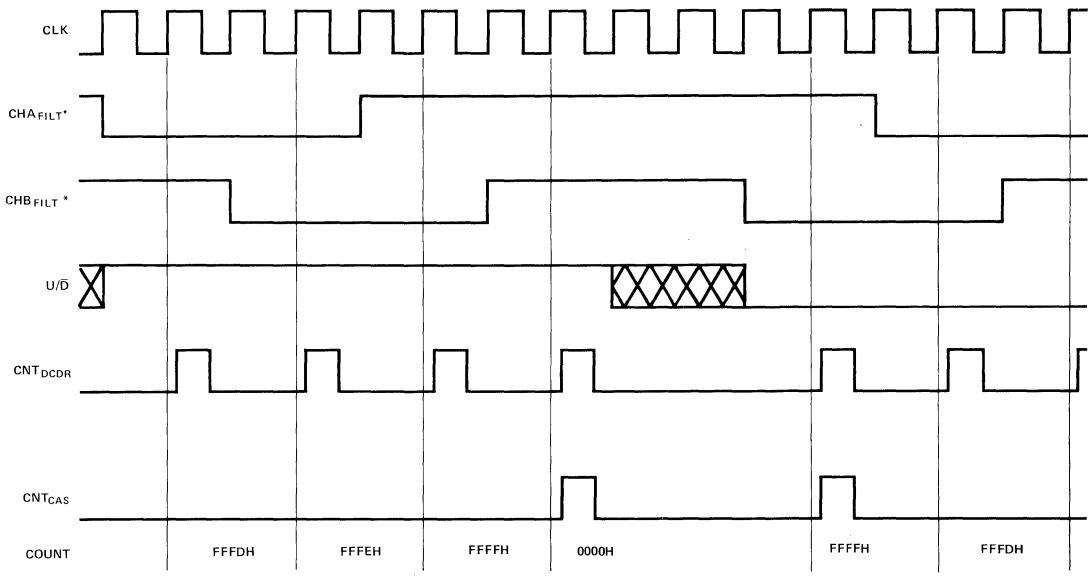


Figure 11. Simplified Inhibit Logic



*CHA_{FILT} and CHB_{FILT} are the outputs of the digital noise filter (see figures 7 and 8).

Figure 12. Decode and Cascade Output Diagram

CASCADE CONSIDERATIONS (HCTL-2020 ONLY)

The HCTL-2020's cascading system allows for position reads of more than two bytes. These reads can be accomplished by latching all of the bytes and then reading the bytes sequentially over the 8-bit bus. Care must be taken to latch all of the bytes such that they represent the count as it actually is, despite propagation delays through the counters.

A good understanding of the mechanics of count propagation is important in designing a proper interface. Consider the sequence of events for a read cycle that starts as the HCTL-2020's internal counter rolls over. On the rising clock edge, count data is updated in the internal counter, rolling it over. A count-cascade pulse (CNT_{CAS}) will be generated with some delay after the rising clock edge (t_{CHD}). There will be additional propagation delays through the external counters and registers. Meanwhile, with $\overline{OE}$ and SEL low to start the read, this new count on the HCTL-2020 will be latched in on the falling clock edge of this cycle. If the external registers are latched too soon, before the CNT_{CAS} pulse has toggled the external counters and registers, a major count error will occur.

Valid data can be ensured by latching the external counter data on the first rising clock edge following the falling edge on which the internal count on the HCTL-2020 is latched (provided that all the delays are less than one clock cycle). This will ensure that a cascade pulse that occurs during the clock cycle when the read begins has adequate time to propagate. This also guarantees that a cascade pulse occurring on the clock cycle after the read is initiated will not be erroneously latched.

For example, suppose the HCTL-2020 count is at FFFFH and an external counter is at F0H, with the count going up. A count occurring in the HCTL-2020 will cause the counter to roll over and a cascade pulse will be generated. A read starting on this clock cycle will show 0000H from the HCTL-2020. The external counter should read F1H, but if the host latches the count before the cascade signal propagates through, the external counter will still read F0H.

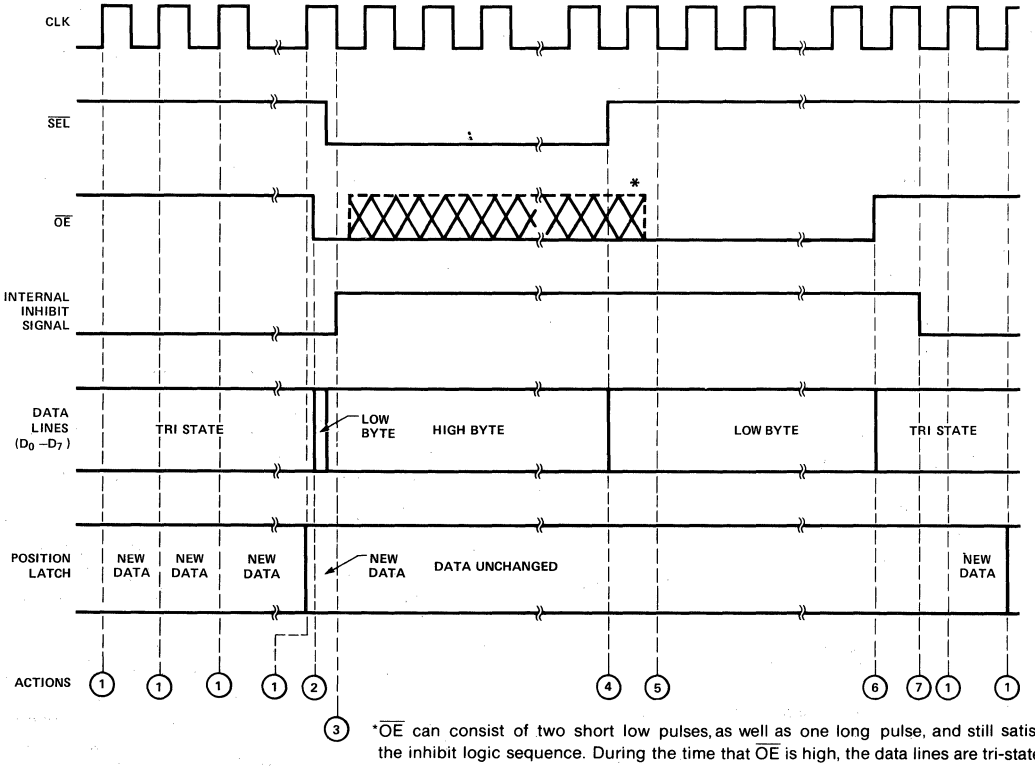
General Interfacing

The 12-bit (HCTL-2000) or 16-bit (HCTL-2016/2020) latch and inhibit logic allows access to 12 or 16 bits of count with an 8-bit bus. When only 8-bits of count are required, a simple 8-bit (1-byte) mode is available by holding SEL high continuously. This disables the inhibit logic. $\overline{OE}$ provides control of the tri-state bus, and read timing is shown in Figures 2 and 3.

For proper operation of the inhibit logic during a two-byte read, $\overline{OE}$ and SEL must be synchronous with CLK due to the falling edge sampling of $\overline{OE}$ and SEL.

The internal inhibit logic on the HCTL-20XX family inhibits the transfer of data from the counter to the position data latch during the time that the latch outputs are being read. The inhibit logic allows the microprocessor to first read the high order 4 or 8 bits from the latch and then read the low order 8 bits from the latch. Meanwhile, the counter can continue to keep track of the quadrature states from the CHA and CHB input signals.

Figure 11 shows the simplified inhibit logic circuit. The operation of the circuitry is illustrated in the read timing shown in Figure 13.



*$\overline{OE}$ can consist of two short low pulses, as well as one long pulse, and still satisfy the inhibit logic sequence. During the time that $\overline{OE}$ is high, the data lines are tri-stated.

Figure 13. Typical Interface Timing

ACTIONS

1. On the rising edge of the clock, counter data is transferred to the position data latch, provided the inhibit signal is low.

2. When $\overline{OE}$ goes low, the outputs of the multiplexer are enabled onto the data lines. If SEL is low, then the high order data bytes are enabled onto the data lines. If SEL is high, then the low order data bytes are enabled onto the data lines.

3. When the IC detects a low on $\overline{OE}$ and SEL during a falling clock edge, the internal inhibit signal is activated. This blocks new data from being transferred from the counter to the position data latch.

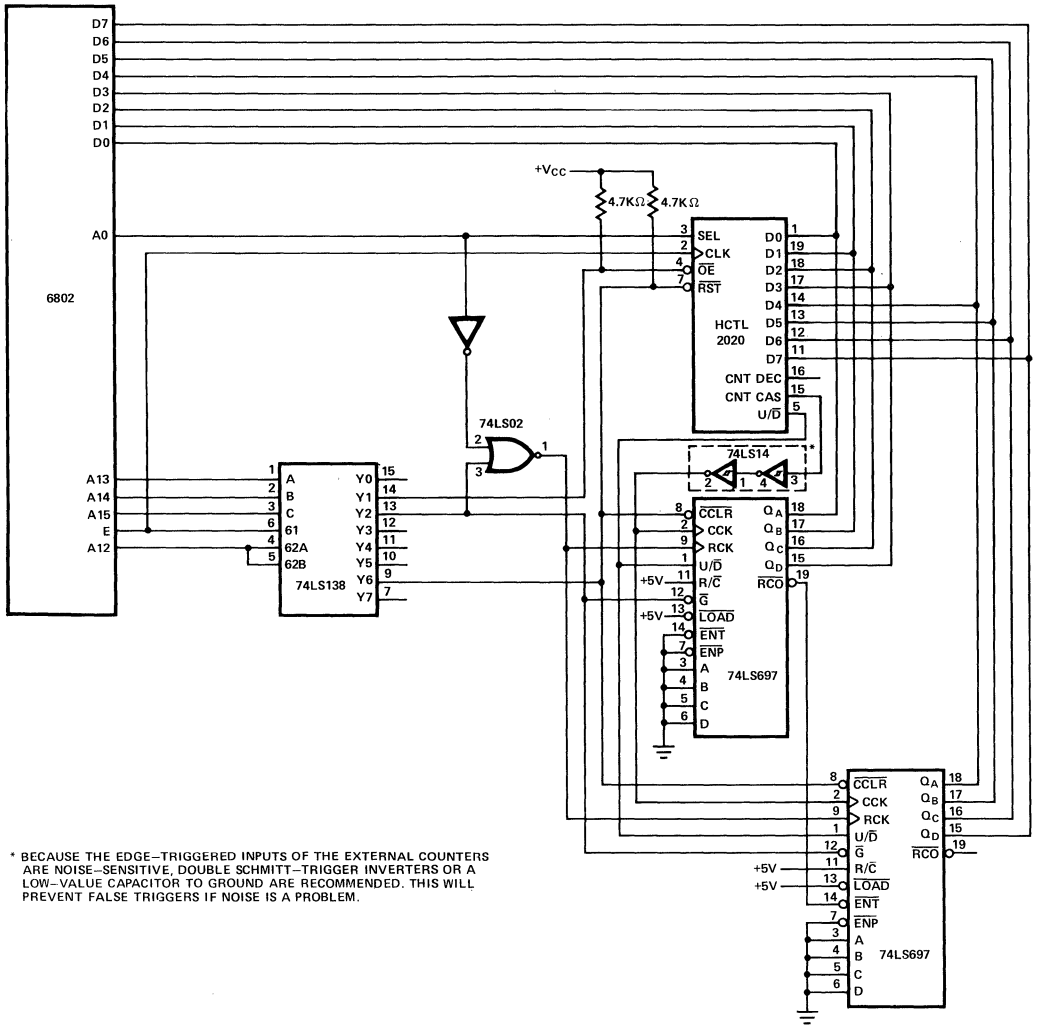
4. When SEL goes high, the data outputs change from the high byte to the low byte.

5. The first of two reset conditions for the inhibit logic is met when the IC detects a logic high on SEL and a logic low on $\overline{OE}$ during a falling clock edge.

6. When $\overline{OE}$ goes high, the data lines change to a high impedance state.

7. The IC detects a logic high on $\overline{OE}$ during a falling clock edge. This satisfies the second reset condition for the inhibit logic.

Interfacing the HCTL-2020 to a Motorola 6802/8 and Cascading the Counter for 24 Bits



* BECAUSE THE EDGE–TRIGGERED INPUTS OF THE EXTERNAL COUNTERS ARE NOISE–SENSITIVE, DOUBLE SCHMITT–TRIGGER INVERTERS OR A LOW–VALUE CAPACITOR TO GROUND ARE RECOMMENDED. THIS WILL PREVENT FALSE TRIGGERS IF NOISE IS A PROBLEM.

Figure 14. A Circuit to Interface to the 6802/8

In this circuit an interface to a Motorola 6802/8 and a cascading scheme for a 24-bit counter are shown. This circuit provides a minimum part count by: 1) using two 74LS697 Up/Down counters with output registers and tri-state outputs and 2) using a Motorola 6802/8 LDX instruction which stores 16 bits of data into the index registers in two consecutive clock cycles.

The HCTL-2020 $\overline{OE}$ and the 74LS697 $\overline{G}$ lines are decoded from Address lines A15-A13. This results in counter data being enabled onto the bus whenever an external memory access is made to locations 4XXX or 2XXX. Address line A12 and processor clock E enable the 74LS138. The processor clock E is also used to clock the HCTL-2020. Address A0 is connected directly to the SEL pin on the HCTL-2020. This line selects the low or high byte of data from the HCTL-2020.

Cascading is accomplished by connecting the CNT_{CAS} output on the HCTL-2020 with the counter clock (CCK) input on both 74LS697's. The U/$\overline{D}$ pin on the HCTL-2020 and the U/$\overline{D}$ pin on both 74LS697's are also directly connected for easy expansion. The $\overline{RCO}$ of the first 4-bit 74LS697 is connected to the $\overline{ENT}$ pin of the second 74LS697. This enables the second counter only when there is a $\overline{RCO}$ signal on the first counter.

This configuration allows the 6802 to read both data bytes with a single double-byte fetch instruction (LDX 2XX0). This instruction is a five cycle instruction which reads external memory location 2XX0 and stores the high order byte into the high byte of the index register. Memory location 2XX1 is next read and stored in the low order byte of the index register. The high byte of counter data is clocked into the 74LS697 registers when SEL is high and $\overline{OE}$ goes low. This upper byte can be read at any time by pulling the 74LS697 $\overline{G}$ low when reading address 4XXX. Figure 15 shows memory addresses and gives an example of reading the HCTL-2020. Figure 16 shows the interface timing for the circuit.

Address	Function
CXXX	Reset Counters
4XXX	Enable High Byte on Data Lines
2XX0	Enable Low Byte on Data Lines
2XX1	Enable Mid Byte on Data Lines

Read Example	
LDX 2000 STX 0100 LDAA 4000 STAA 0102	Loads mid byte and then low byte into memory locations 0100 and 0101 Loads the high byte into memory location 0102

Figure 15. Memory Addresses and Read Example

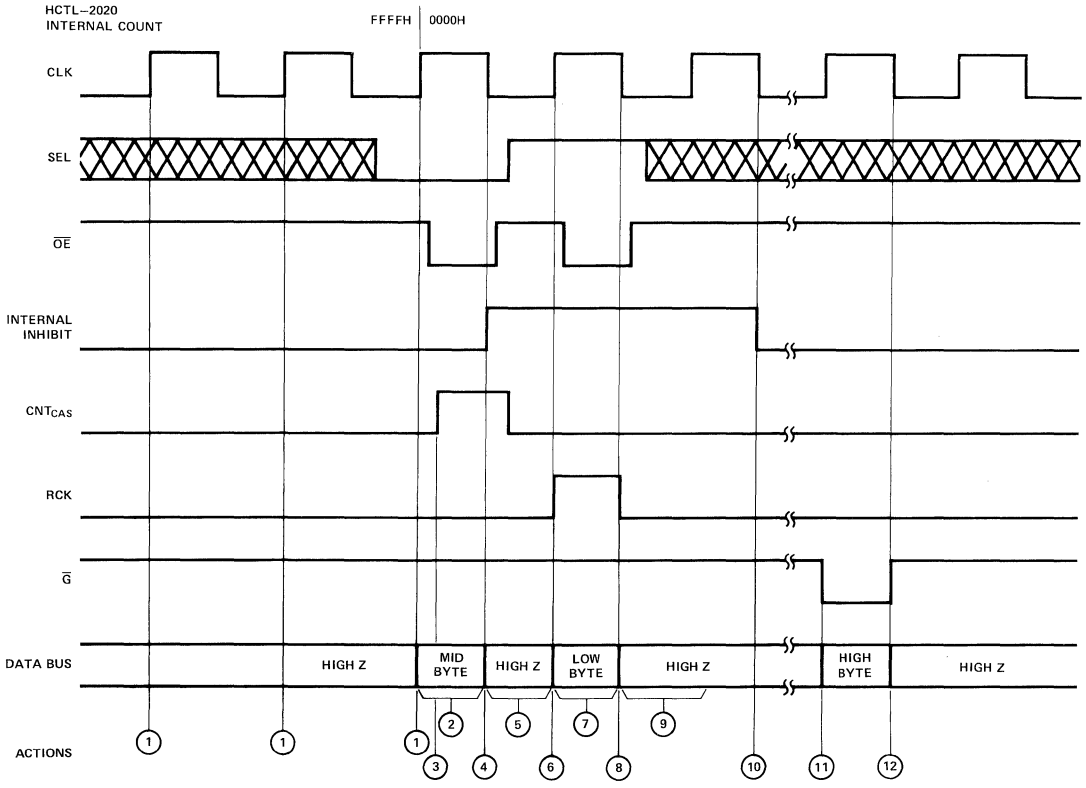


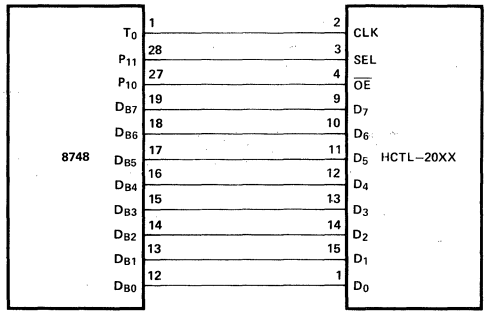
Figure 16. Interface Timing for the 6802/8

ACTIONS

1. The microprocessor clock output is E. If the internal HCTL-2020 inhibit is not active, new data is transferred from the internal counter to the position data latch.
2. An even address output from the 6802 causes SEL to go low. When E goes high, the address decoder output for the HCTL-2020 $\overline{OE}$ signal goes low. This causes the HCTL-2020 to output the middle byte of the system counter (high byte of the HCTL-2020 counter).
3. In this case, the HCTL-2020 counter has overflowed and there is an output on the CNT_{CAS} line. This pulse is counted by the 74LS697 but not loaded into the output register of the 74LS697 at this time.
4. The 6802 reads the data bus on the falling edge of E, storing the high order 2020 data byte (middle system byte) into the high byte of the index register. The chip detects that $\overline{OE}$ and SEL are low on the falling edge of E and activates the internal inhibit signal. The position data latch is inhibited and data cannot be transferred from the internal counter to the latch.
5. When E goes low, the address decoder output is disabled and $\overline{OE}$ goes high. The 6802 increments the address, causing SEL to go high. The position data latch is still inhibited.
6. When SEL is high and $\overline{OE}$ is low the 74LS697 register clock (RCK) goes high. The rising edge of RCK loads the 74LS697 count into the 74LS697 register. Delaying the RCK signal until the second $\overline{OE}$ allows for delays on the CNT_{CAS} signal.
7. The address decoder is enabled after E goes high. The $\overline{OE}$ line goes low and the low data byte is enabled onto the bus.
8. The 6802 reads the data bus on the falling edge of E, storing the low order data byte into the low byte of the index register. The HCTL-2020 detects that $\overline{OE}$ is low and SEL is high on the falling edge of E, thus meeting the first inhibit reset condition.
9. When E goes low, the address decoder is disabled, causing $\overline{OE}$ to go high and the data lines to go to the high impedance state. The 6802 continues its instruction execution, and the state of SEL is indeterminate.
10. The HCTL-2020 detects $\overline{OE}$ is high on the next falling edge of E. This satisfies the second inhibit reset condition and the inhibit signal is reset.
11. When E goes high, a new address causes the $\overline{G}$ line on the 74LS697 to go low and enables the high byte onto the data bus.
12. When E goes low, the high byte is read into the 6802. The data bus returns to tri-state.

Interfacing the HCTL-20XX to an Intel 8748

The circuit shown in Figure 17 shows the connections between an HCTL-20XX and an 8748. Data lines D0-D7 are connected to the 8748 bus port. Bits 0 and 1 of port 1 are used to control the SEL and $\overline{OE}$ inputs of the HCTL-20XX respectively. T0 is used to provide a clock signal to the HCTL-20XX. The frequency of T0 is the crystal frequency divided by 3. T0 must be enabled by executing the ENT0 CLK instruction after each system reset, but prior to the first encoder position change. An 8748 program which interfaces to the circuit in Figure 17 is given in Figure 18. The resulting interface timing is shown in Figure 19.



* NOTE: PIN NUMBERS ARE DIFFERENT FOR THE HCTL-2020

Figure 17. An HCTL-20XX-to-Intel 8748 Interface

LOC	Object Code	Source Statements	Comments
000	99 00	ANL P1, 00H	Enable output and higher order bits
002	08	INS A, BUS	Load higher order bits into ACC
003	A8	MOVE R0 A	Move data to register 0
004	89 03	ORL P1, 01H	Change data from high order to low order bits
006	08	INS A, BUS	Load order bits into AC
008	A9	MOV R1, A	Move data to register 1
009	89 03	ORL P1, 03H	Disable outputs
00B	93	RETR	Return

Figure 18. A Typical Program for Reading HCTL-20XX with an 8748

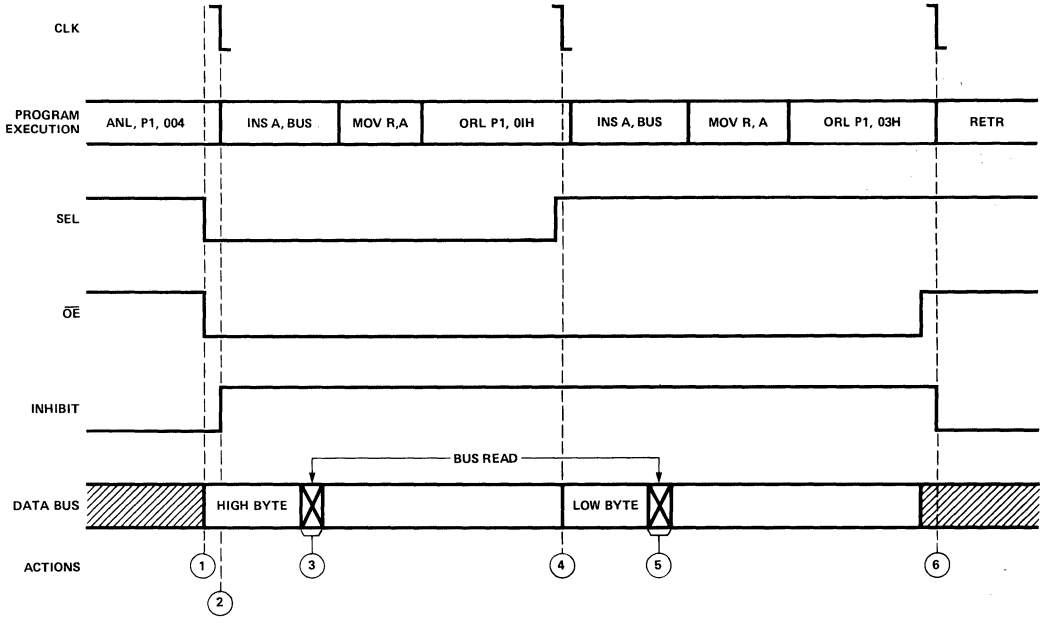


Figure 19. 8748 READ Cycle from Figure 18.

ACTIONS

1. ANL P1, 00H has just been executed. The output of bits 0 and 1 of Port 1 cause SEL and $\overline{OE}$ to be logic low. The data lines output the higher order byte.
2. The HCTL-20XX detects that $\overline{OE}$ and SEL are low on the next falling edge of the CLK and asserts the internal inhibit signal. Data can be read without regard for the phase of the CLK.
3. INS A, BUS has just been executed. Data is read into the 8748.
4. ORL PORT 1, 01H has just been executed. The program sets SEL high and leaves $\overline{OE}$ low by writing the correct values to port 1. The HCTL-20XX detects $\overline{OE}$ is low and SEL is high on the next falling edge of the CLK, and thus the first inhibit reset condition is met.
5. INS A, BUS has just been executed. Lower order data bits are read into the 8748.
6. ORL P1, 03H has just been executed. The HCTL-20XX detects $\overline{OE}$ high on the next falling edge of CLK. The program sets $\overline{OE}$ and SEL high by writing the correct values to port 1. This causes the data lines to be tri-stated. This satisfies the second inhibit and reset condition. On the next rising CLK edge new data is transferred from the counter to the position data latch.

HEWLETT PACKARD

New

Surface Mount Quadrature Decoder/Counter Interface IC

Technical Data

HCTL-2016 #PLC
HCTL-2020 #PLC

Features

- **20 Pin PLCC Surface Mount Package**
- **All Features of the HCTL-2016 and HCTL-2020 PDIP**

Description

The HCTL-2016 #PLC and HCTL-2020 #PLC are quadrature decoder/counter interface ICs in a 20 pin PLCC (plastic leaded chip carrier) surface mount package. These CMOS ICs interface incremental encoders to microprocessors by performing the quadrature decoder, counter, and bus transfer functions.

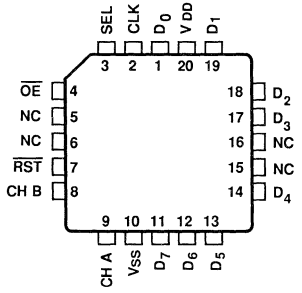
The HCTL-2016 #PLC and HCTL-2020 #PLC have all of the same features, functions, and operating characteristics as the HCTL-2016 and HCTL-2020 PDIP (plastic dual-in-line package).

For further information on the operation and function of the HCTL-2016 #PLC and 2020 #PLC, please refer to the HCTL-2000/HCTL-2016/HCTL-2020 data sheet.

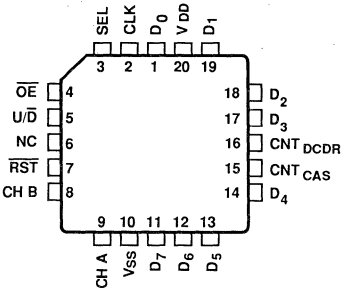
Applications

Typical applications include interfacing incremental encoders to microprocessors and interfacing digital potentiometers to digital data input buses.

Pinouts



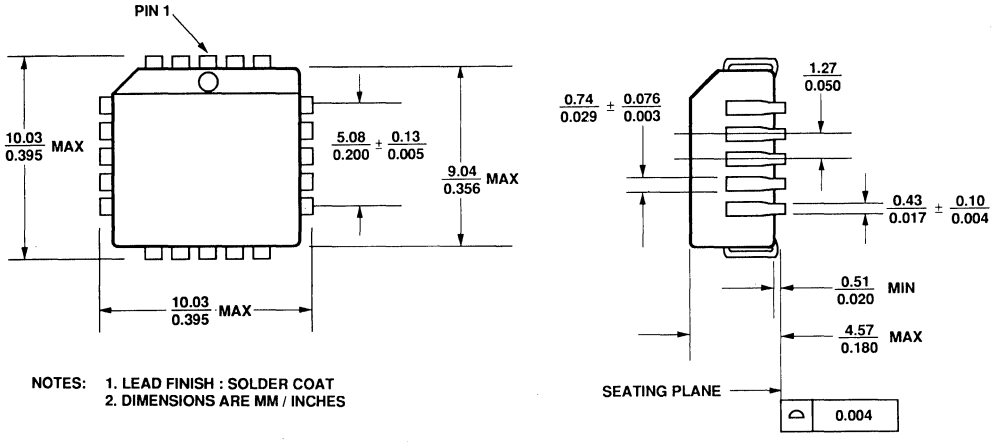
HCTL-2016 #PLC



HCTL-2020 #PLC

ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

Package Dimensions



NOTES: 1. LEAD FINISH : SOLDER COAT
2. DIMENSIONS ARE MM / INCHES

20 PIN PLASTIC LEADED CHIP CARRIER PACKAGE

Devices

Part No.	Description
HCTL-2016 #PLC	16-bit counter; 14 MHz clock operation; 20 pin PLCC surface mount package.
HCTL-2020 #PLC	All features of HCTL-2016 #PLC plus quadrature decoder output signals and cascade output signals.

HEWLETT PACKARD

General Purpose Motion Control IC

Technical Data

HCTL-1100 Series

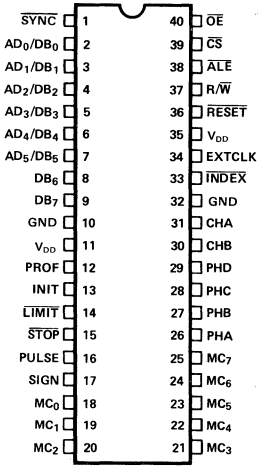
Features

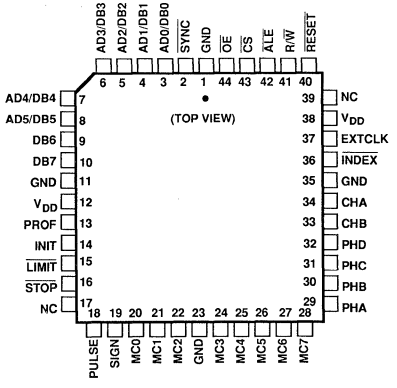
- **Low Power CMOS**
- **PDIP and PLCC Versions Available**
- **Enhanced Version of the HCTL-1000**
- **DC, DC Brushless, and Step Motor Control**
- **Position and Velocity Control**
- **Programmable Digital Filter and Commutator**
- **8-Bit Parallel, and PWM Motor Command Ports**
- **TTL Compatible**
- **SYNC Pin for Coordinating Multiple HCTL-1100 ICs**
- **100 kHz to 2 MHz Operation**
- **Encoder Input Port**

Description

The HCTL-1100 series is a high performance, general purpose motion control IC, fabricated in HP CMOS technology. It frees the host processor for other tasks by performing all the time-intensive functions of digital motion control. The programmability of all control parameters provides maximum flexibility and quick design of control systems with a minimum number of components. In addition to the HCTL-1100, the complete control system consists of a host processor to specify commands, an amplifier, and a motor with an incremental encoder (such as the HP HEDS-5XXX, -6XXX, -9XXX series). No analog compensation or velocity feedback is necessary.

Pinouts





ESD WARNING; NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

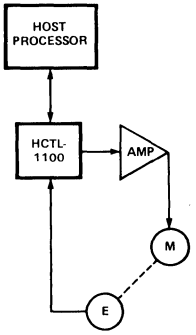
Table of Contents

Applications

Typical applications for the HCTL-1100 include printers, medical instruments, material handling machines, and industrial automation.

HCTL-1100 vs. HCTL-1000

The HCTL-1100 is designed to replace the HCTL-1000. Some differences exist, and some enhancements have been added.

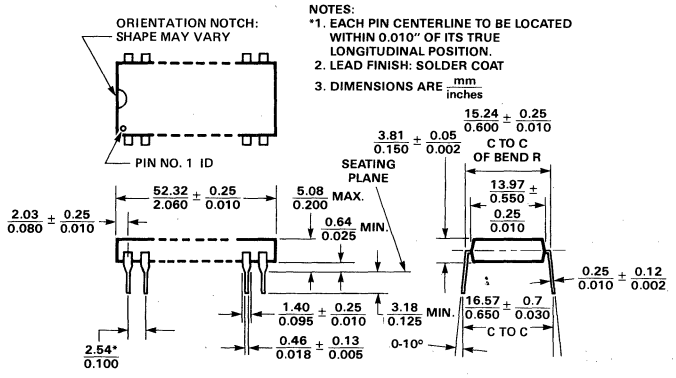


System Block Diagram

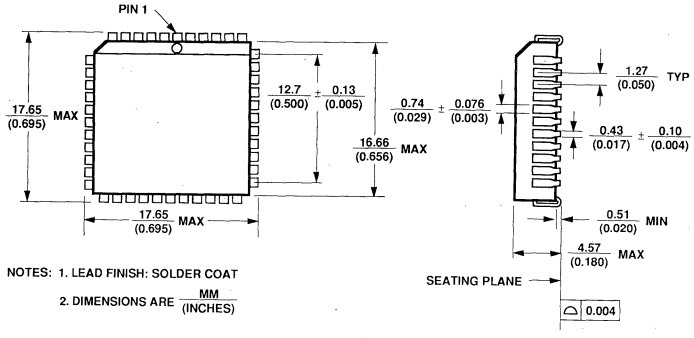
Comparison of HCTL-1100 and HCTL-1000

Description	HCTL-1100	HCTL-1000
Max. Supply Current	30 mA	180 mA
Max. Power Dissipation	165 mW	950 mW
Max. Tri-State Output Leakage Current	150 nA	10 µA
Operating Frequency	100 kHz-2 MHz	1 MHz-2 MHz
Operating Temperature Range	-20°C to +85°C	0°C to 70°C
Storage Temperature Range	-55°C to +125°C	-40°C to +125°C
Synchronize 2 or More ICs	Yes	–
Preset Actual Position Registers	Yes	–
Read Flag Register	Yes	–
Limit and Stop Pins	Must be pulled up to V_{DD} if not used.	Can be left floating if not used.
Hard Reset	Required	Recommended
PLCC Package Available	Yes	–

Package Dimensions



40-PIN PLASTIC DUAL INLINE PACKAGE



44 PIN PLASTIC LEADED CHIP CARRIER PACKAGE

Theory of Operation

The HCTL-1100 is a general purpose motor controller which provides position and velocity control for DC, DC brushless and stepper motors. The internal block diagram of the HCTL-1100 is shown in Figure 1. The HCTL-1100 receives its input commands from a host processor and position feedback from an incremental encoder with quadrature output. An 8-bit bi-directional multiplexed address/data bus interfaces the HCTL-1100 to the host processor. The encoder feedback is decoded into quadrature counts and a 24-bit counter keeps track of position. The HCTL-1100 executes any one of four control algorithms selected by the user. The four control modes are:

- Position Control
- Proportional Velocity Control
- Trapezoidal Profile Control for point to point moves
- Integral Velocity Control with continuous velocity profiling using linear acceleration

The resident Position Profile Generator calculates the necessary profiles for Trapezoidal Profile Control and Integral Velocity Control. The HCTL-1100 compares the desired position (or velocity) to the actual position (or velocity) to compute compensated motor commands using a programmable digital filter D(z). The motor command is externally available at the Motor Command port as an 8-bit byte and at the PWM port as a Pulse Width Modulated (PWM) signal.

The HCTL-1100 has the capability of providing electronic commutation for DC brushless and stepper motors. Using the encoder position information, the motor phases are enabled in the correct sequence. The commutator is fully programmable to encompass most motor/encoder combinations. In addition, phase overlap and phase advance can be programmed to improve torque ripple and high speed performance. The HCTL-1100 contains a number of flags including two externally available flags, Profile and Initialization, which allow the user to see or check the status of the controller. It also has two emergency inputs, $\overline{\text{Limit}}$ and $\overline{\text{Stop}}$, which allow operation of the HCTL-1100 to be interrupted under emergency conditions.

The HCTL-1100 controller is a digitally sampled data system. While information from the host processor is accepted asynchronously with respect to the control functions, the motor command is computed on a discrete sample time basis. The sample timer is programmable.

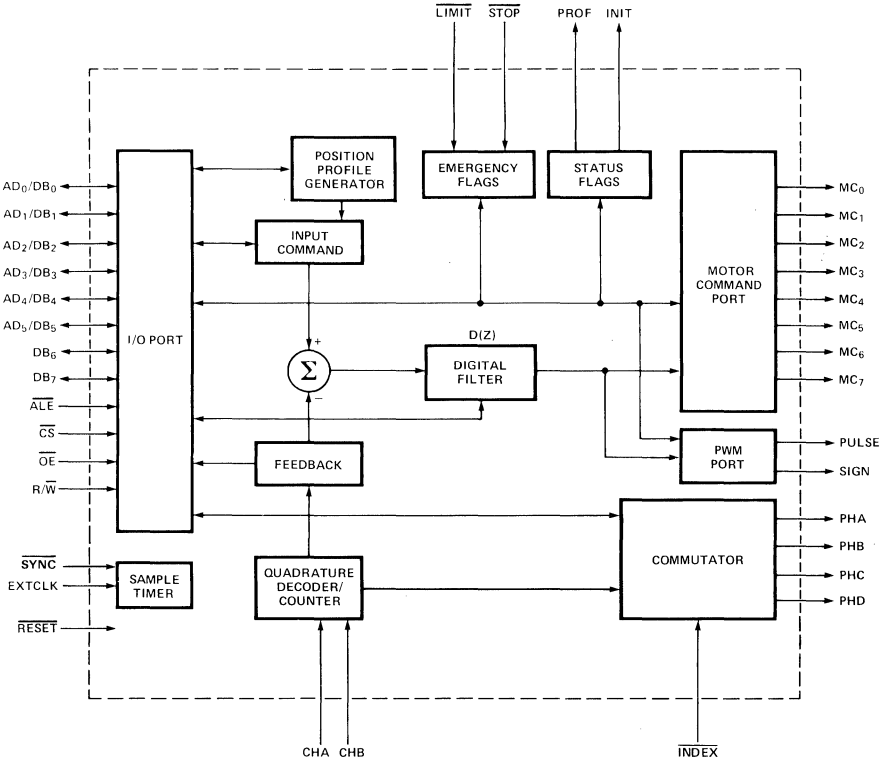


Figure 1. Internal Block Diagram.

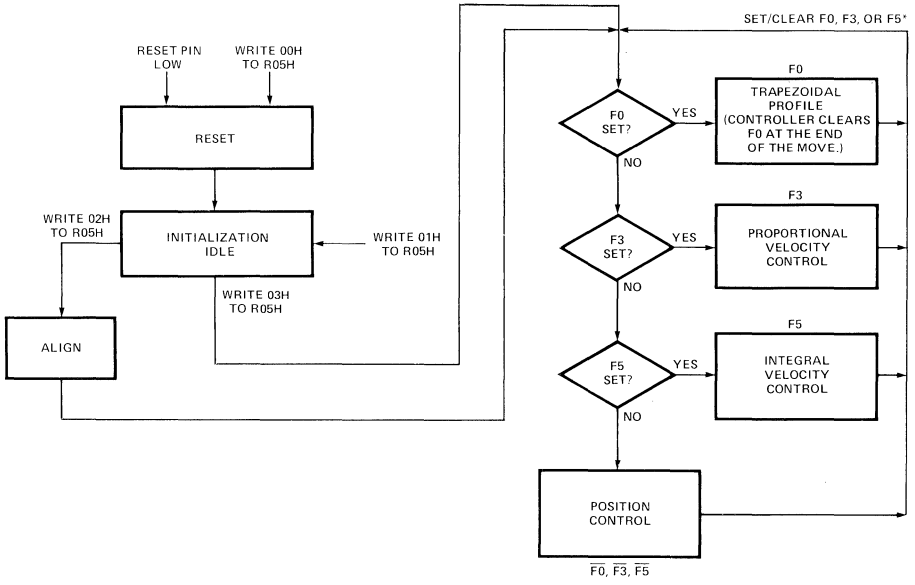


Figure 2. Operating Mode Flowchart

Electrical Specifications

Absolute Maximum Ratings

Operating Temperature, T_A ..... -20°C to 85°C
Storage Temperature, T_S ..... -55°C to 125°C
Supply Voltage, V_{DD} ..... -0.3 V to 7 V
Input Voltage, V_{IN} ..... -0.3 V to V_{DD} +0.3 V
Maximum Operating Clock Frequency, f_{CLK} ..... 2 MHz

DC Electrical Characteristics

V_{DD} = 5 V ± 5%; T_A = -20°C to +85°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Voltage	V_{DD}	4.75	5.00	5.25	V	
Supply Current	I_{DD}		15	30	mA	
Input Leakage Current	I_{IN}		10	100	nA	V_{IN} = 0.00 and 5.25 V
Input Pull-Up Current SYNC PIN	I_{PU}		-40	-100	µA	V_{IN} = 0.00 V
Tristate Output Leakage Current	I_{OZ}		10	150	nA	V_{OUT} = -0.3 to 5.25 V
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{DD}	V	
Output Low Voltage	V_{OL}	-0.3		0.4	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4		V_{DD}	V	I_{OH} = -200 µA
Power Dissipation	P_D		75	165	mW	
Input Capacitance	C_{IN}			20	pF	
Output Capacitance	C_{OUT}		100		pF	

AC Electrical Characteristics

V_{DD} = 5 V ± 5%; T_A = -20°C to +85°C; Units = nsec

ID #	Signal	Symbol	Clock Frequency				Formula*	
			2 MHz		1 MHz			
			Min.	Max.	Min.	Max.	Min.	Max.
1	Clock Period (clk)	t_{CPER}	500		1000			
2	Pulse Width, Clock High	t_{CPWH}	230		300			
3	Pulse Width, Clock Low	t_{CPWL}	200		200		200	
4	Clock Rise and Fall Time	t_{CR}		50		50		50
5	Input Pulse Width $\overline{\text{Reset}}$	t_{IRST}	2500		5000		5 clk	
6	Input Pulse Width $\overline{\text{Stop}}$, $\overline{\text{Limit}}$	t_{IP}	600		1100		1 clk + 100 ns	
7	Input Pulse Width $\overline{\text{Index}}$, Index	t_{IX}	1600		3100		3 clk + 100 ns	
8	Input Pulse Width CHA, CHB	t_{IAB}	1600		3100		3 clk + 100 ns	
9	Delay CHA to CHB Transition	t_{AB}	600		1100		1 clk + 100 ns	
10	Input Rise/Fall Time CHA, CHB, Index	t_{IABR}		450		900		900 (clk < 1 MHz)
11	Input Rise/Fall Time $\overline{\text{Reset}}$, $\overline{\text{ALE}}$, $\overline{\text{CS}}$, $\overline{\text{OE}}$, $\overline{\text{Stop}}$, $\overline{\text{Limit}}$	t_{IR}		50		50		50
12	Input Pulse Width $\overline{\text{ALE}}$, $\overline{\text{CS}}$	t_{IPW}	80		80		80	
13	Delay Time, $\overline{\text{ALE}}$ Fall to $\overline{\text{CS}}$ Fall	t_{AC}	50		50		50	
14	Delay Time, $\overline{\text{ALE}}$ Rise to $\overline{\text{CS}}$ Rise	t_{CA}	50		50		50	
15	Address Setup Time Before $\overline{\text{ALE}}$ Rise	t_{ASR1}	20		20		20	
16	Address Setup Time Before $\overline{\text{CS}}$ Fall	t_{ASR}	20		20		20	
17	Write Data Setup Time Before $\overline{\text{CS}}$ Rise	t_{DSR}	20		20		20	
18	Address/Data Hold Time	t_H	20		20		20	
19	Setup Time, R/$\overline{\text{W}}$ Before $\overline{\text{CS}}$ Rise	t_{WCS}	20		20		20	
20	Hold Time, R/$\overline{\text{W}}$ After $\overline{\text{CS}}$ Rise	t_{WH}	20		20		20	
21	Delay Time, Write Cycle, $\overline{\text{CS}}$ Rise to $\overline{\text{ALE}}$ Fall	t_{CSAL}	1700		3400		3.4 clk	
22	Delay Time, Read/Write, $\overline{\text{CS}}$ Rise to $\overline{\text{CS}}$ Fall	t_{CSCS}	1500		3000		3 clk	
23	Write Cycle, $\overline{\text{ALE}}$ Fall to $\overline{\text{ALE}}$ Fall For Next Write	t_{WC}	1830		3530		3.7 clk	

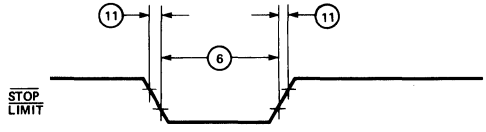
AC Electrical Characteristics (continued).

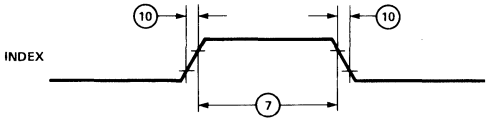
ID #	Signal	Symbol	Clock Frequency				Formula*	
			2 MHz		1 MHz			
			Min.	Max.	Min.	Max.	Min.	Max.
24	Delay Time, $\overline{CS}$ Rise to $\overline{OE}$ Fall	t_{CSOE}	1700		3200		3 clk + 200 ns	
25	Delay Time, $\overline{OE}$ Fall to Data Bus Valid	t_{OEDB}	100		100		100	
26	Delay Time, $\overline{CS}$ Rise to Data Bus Valid	t_{CSDB}	1800		3300		3 clk + 300 ns	
27	Input Pulse Width $\overline{OE}$	t_{IPWOE}	100		100		100	
28	Hold Time, Data Held After $\overline{OE}$ Rise	t_{DOEH}	20		20		20	
29	Delay Time, Read Cycle, $\overline{CS}$ Rise to $\overline{ALE}$ Fall	t_{CSALR}	1820		3320		3 clk + 320 ns	
30	Read Cycle, $\overline{ALE}$ Fall to $\overline{ALE}$ Fall For Next Read	t_{RC}	1950		3450		3 clk + 450 ns	
31	Output Pulse Width, PROF, INIT, Pulse, Sign, PHA-PHD, MC Port	t_{OF}	500		1000		1 clk	
32	Output Rise/Fall Time, PROF, INIT, Pulse, Sign, PHA-PHD, MC Port	t_{OR}	20	150	20	150	20	150
33	Delay Time, Clock Rise to Output Rise	t_{EP}	20	300	20	300	20	300
34	Delay Time, $\overline{CS}$ Rising to MC Port Valid	t_{CSMC}		1600		3200		3.2 clk
35	Hold Time, $\overline{ALE}$ High After $\overline{CS}$ Rise	t_{ALH}	100		100		100	
36	Pulse Width, $\overline{ALE}$ High	t_{ALPWH}	100		100		100	
37	Pulse Width, $\overline{SYNC}$ Low	t_{SYNC}	9000		18000		18 clk	

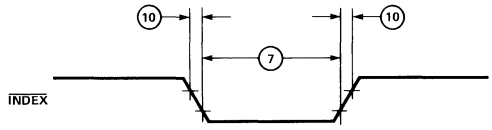
*General formula for determining AC characteristics for other clock frequencies (clk), between 100 kHz and 2 MHz.

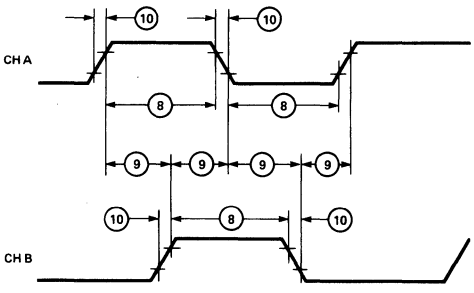
HCTL-1100 I/O Timing Diagrams

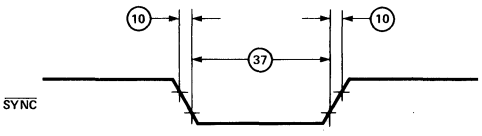
Input logic level values are the TTL Logic levels V_{IL} = 0.8 V and V_{IH} = 2.0 V. Output logic levels are V_{OL} = 0.4 V and V_{OH} = 2.4 V.

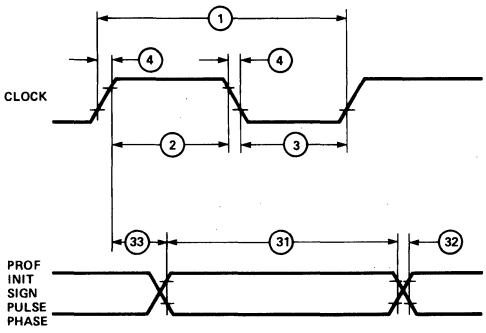


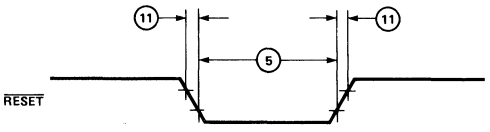










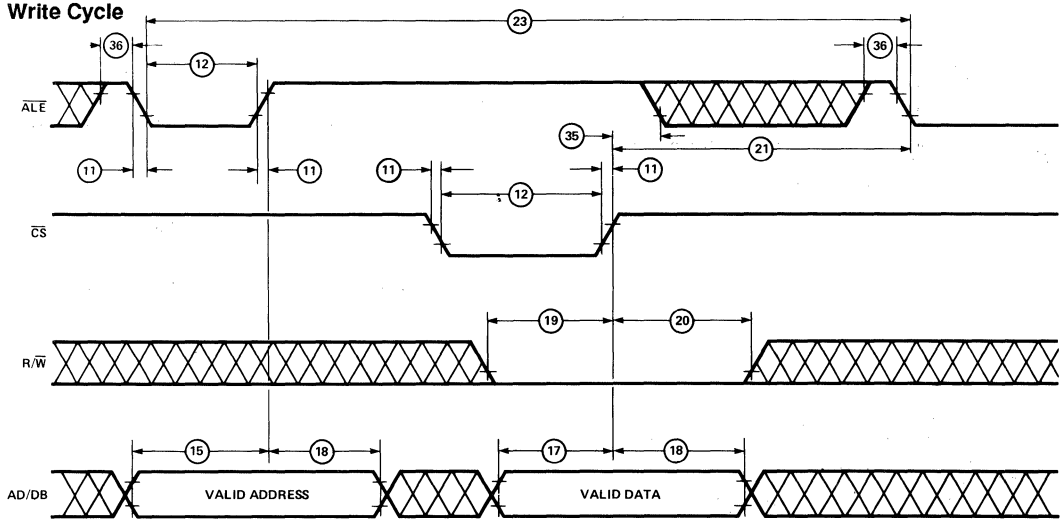


HCTL-1100 I/O Timing Diagrams

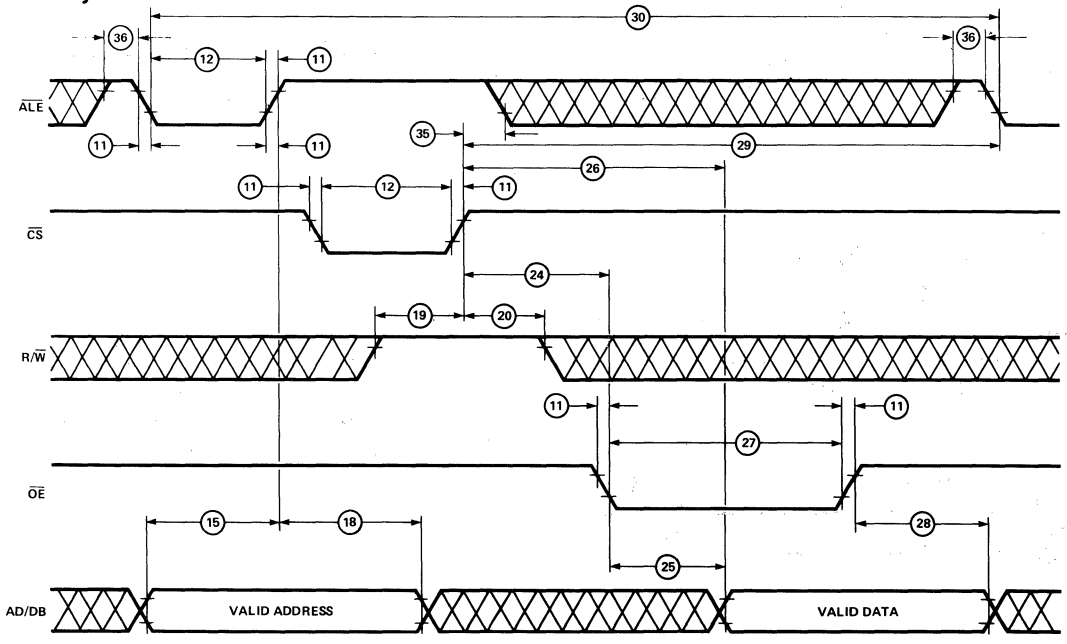
There are three different timing configurations which can be used to give the user flexibility to interface the HCTL-1100 to most microprocessors. See the I/O interface section for more details.

$\overline{ALE}/\overline{CS}$ NON OVERLAPPED

Write Cycle



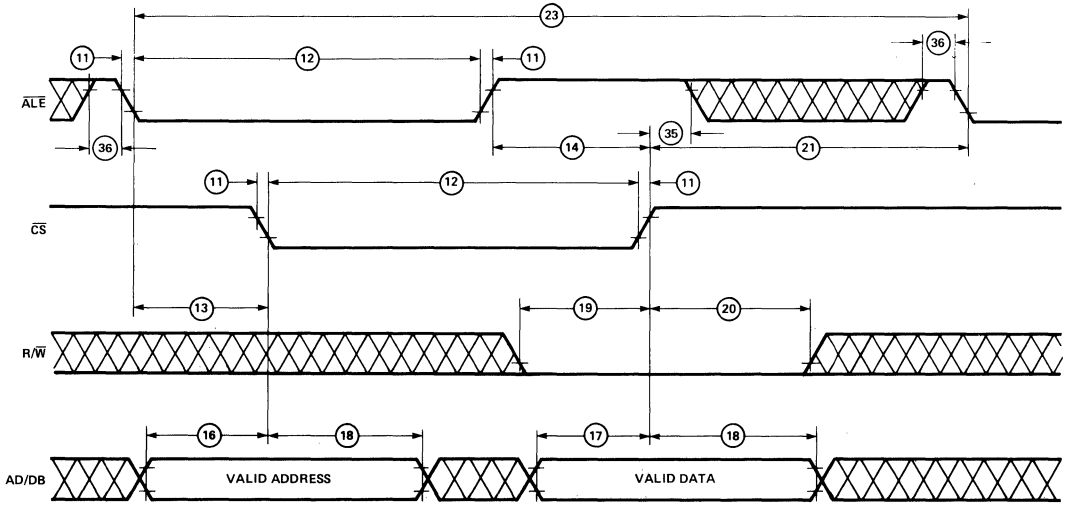
Read Cycle



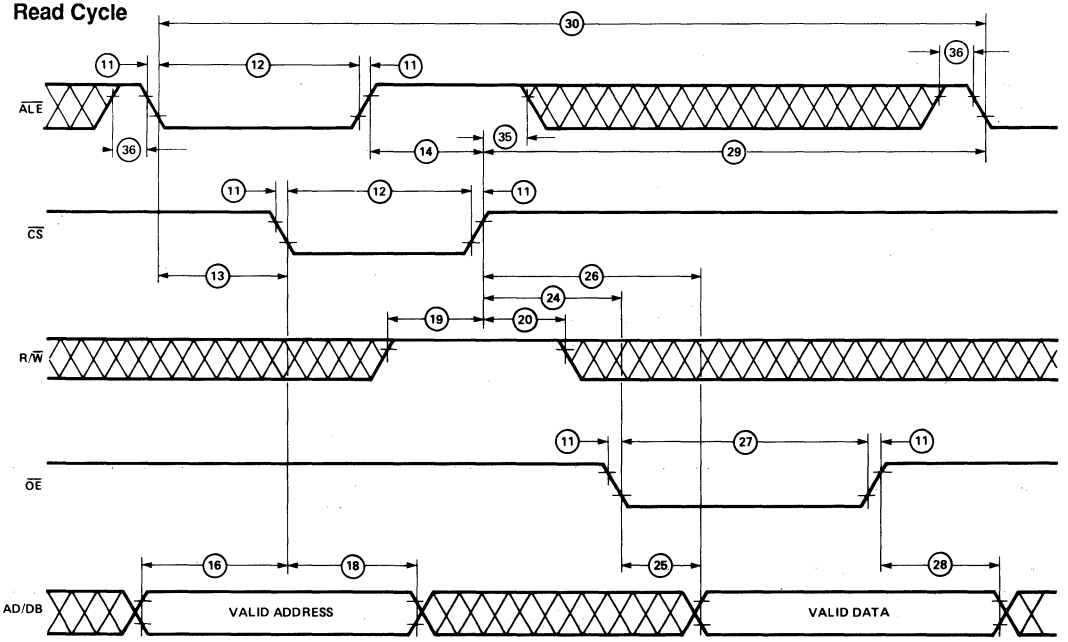
HCTL-1100 I/O Timing Diagrams

$\overline{ALE}/\overline{CS}$ OVERLAPPED

Write Cycle



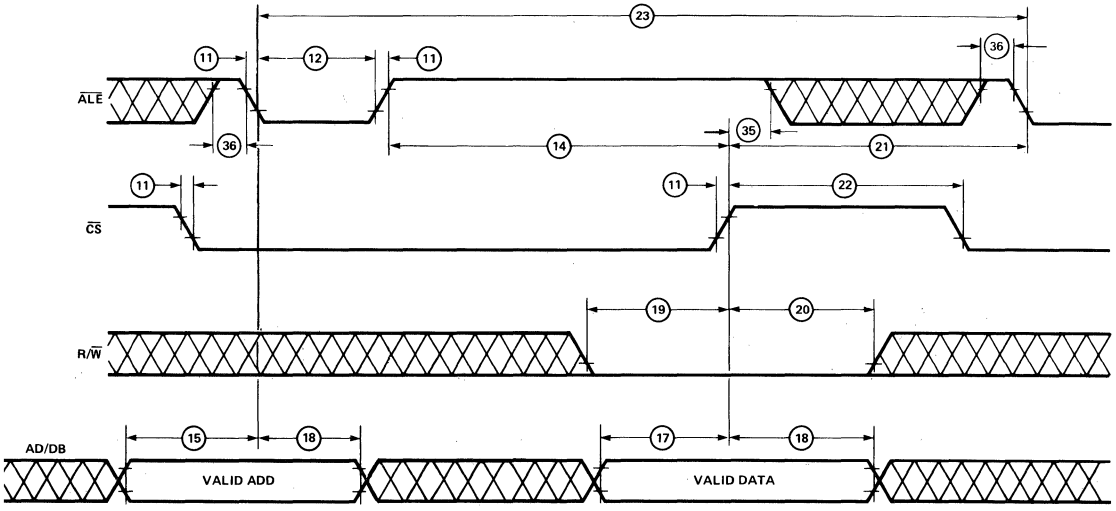
Read Cycle



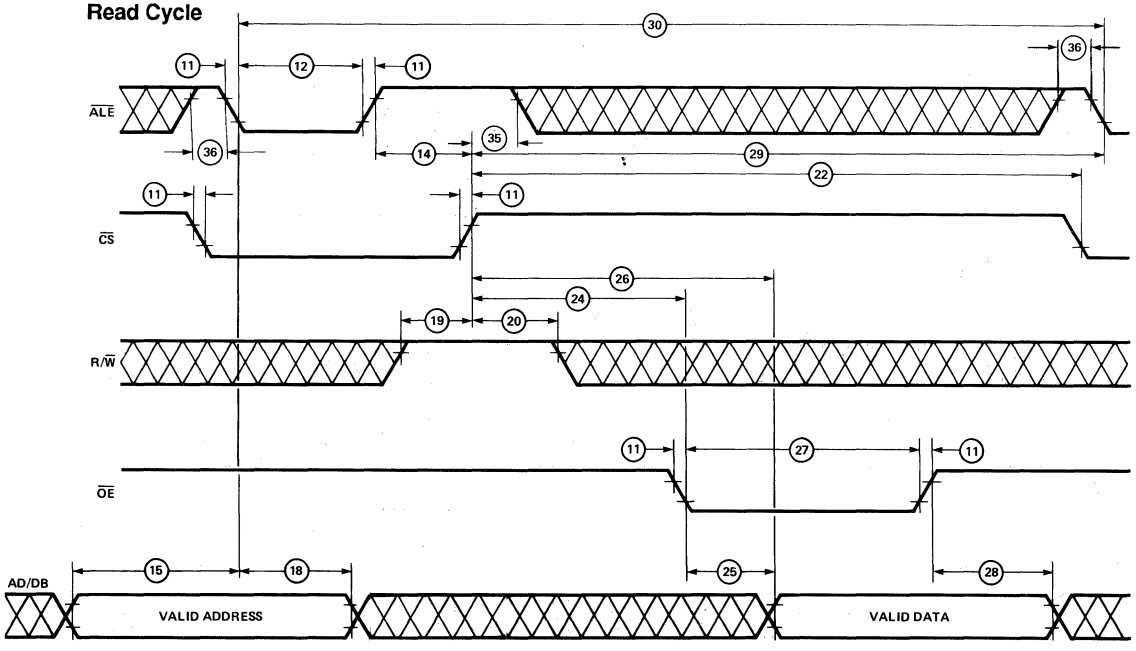
HCTL-1100 I/O Timing Diagrams

$\overline{ALE}$ WITHIN $\overline{CS}$

Write Cycle



Read Cycle



Pin Descriptions and Functions

Input/Output Pins

Symbol	Pin Number PDIP	Pin Number PLCC	Description
AD0/DB0-AD5/DB5	2-7	3-8	Address/Data Bus – Lower 6 bits of 8-bit I/O port which are multiplexed between address and data.
DB6, DB7	8, 9	9, 10	Data bus – Upper 2 bits of 8-bit I/O port used for data only.

Input Signals

Symbol	Pin Number PDIP	Pin Number PLCC	Description
CHA/CHB	31, 30	34, 33	Channel A, B – Input pins for position feedback from an incremental shaft encoder. Two channels, A and B, 90 degrees out of phase are required.
$\overline{\text{Index}}$	33	36	Index Pulse – Input from the reference or index pulse of an incremental encoder. Used only in conjunction with the Commutator. Either a low or high true signal can be used with the Index pin. See Timing Diagrams and Encoder Interface section for more detail.
R/$\overline{\text{W}}$	37	41	Read/Write – Determines direction of data exchange for the I/O port.
$\overline{\text{ALE}}$	38	42	Address Latch Enable – Enables lower 6 bits of external data bus into internal address latch.
$\overline{\text{CS}}$	39	43	Chip Select – Performs I/O operation dependent on status of R/$\overline{\text{W}}$ line. For a Write, the external bus data is written into the internal addressed location. For Read, data is read from an internal location into an internal output latch.
$\overline{\text{OE}}$	40	44	Output Enable – Enables the data in the internal output latch onto the external data bus to complete a Read operation.
$\overline{\text{Limit}}$	14	15	Limit Switch – An internal flag which when externally set, triggers an unconditional branch to the Initialization/Idle mode before the next control sample is executed. Motor Command is set to zero. Status of the Limit flag is monitored in the Status register.
$\overline{\text{Stop}}$	15	16	Stop Flag – An internal flag that is externally set. When flag is set during Integral Velocity Control mode, the Motor Command is decelerated to a stop.
$\overline{\text{Reset}}$	36	40	Reset – A hard reset of internal circuitry and a branch to Reset mode.
ExtClk	34	37	External Clock
V_{DD}	11, 35	12, 38	Voltage Supply – Both V_{DD} pins must be connected to a 5.0 volt supply.
GND	10, 32	1, 11, 23, 35	Circuit Ground
$\overline{\text{SYNC}}$	1	2	Used to synchronize multiple HCTL-1100 sample timers.
NC	–	17, 39	Not connected. These pins should be left floating.

Output Pins

Symbol	Pin Number		Description
	PDIP	PLCC	
MC0-MC7	18-25	20-22, 24-28	Motor Command Port – 8-bit output port which contains the digital motor command adjusted for easy bipolar DAC interfacing. MC7 is the most significant bit (MSB).
Pulse	16	18	Pulse – Pulse width modulated signal whose duty cycle is proportional to the Motor Command magnitude. The frequency of the signal is External Clock/100 and pulse width is resolved into 100 external clocks.
Sign	17	19	Sign – Gives the sign/direction of the pulse signal.
PHA-PHD	26-29	29-32	Phase A, B, C, D – Phase Enable outputs of the Commutator.
Prof	12	13	Profile Flag – Status flag which indicates that the controller is executing a profiled position move in the Trapezoidal Profile Control mode.
Init	13	14	Initialization/Idle Flag – Status flag which indicates that the controller is in the Initialization/Idle mode.

Pin Functionality

$\overline{\text{SYNC}}$ Pin

The $\overline{\text{SYNC}}$ pin is used to synchronize two or more ICs. It is only valid in the INIT/IDLE mode (see Operating the HCTL-1100). When this pin is pulled low, the internal sample timer is cleared and held to zero. When the level on the pin is returned to high, the internal sample timer instantly starts counting down from the programmed value.

Connecting all $\overline{\text{SYNC}}$ pins together in the system and pulsing the $\overline{\text{SYNC}}$ signal from the host processor will synchronize all controllers.

$\overline{\text{Limit}}$ Pin

This emergency-flag input is used to disable the control modes of the HCTL-1100. A low level on this input pin causes the internal Limit flag to be set. If this pin is NOT used, it must be pulled up to V_{DD}. If it is not connected, the pin could float low, and possibly trigger a false emergency condition.

The Limit flag, when set in any control mode, causes the HCTL-1100 to go into the Initialization/Idle mode, clearing the Motor Command and causing an immediate motor shutdown. When the Limit flag is set, none of the three control mode flags (F0, F3, or F5) are cleared as the HCTL-1100 enters the Initialization/Idle mode. The user should be aware that these flags are still set before commanding the HCTL-1100 to re-enter one of the four control modes from Initialization/Idle mode.

In general, the user should clear all control mode flags after the $\overline{\text{limit}}$ pin has been pulled low, then proceed.

$\overline{\text{Stop}}$ Pin

The Stop flag affects the HCTL-1100 only in the Integral Velocity Mode.

When a low level is present on this emergency-flag input, the internal stop flag is set. If this pin is NOT used, it must be pulled up to V_{DD}. If it is not connected, the pin could float low, and possibly trigger a false emergency condition.

When the STOP flag is set, the system will come to a decelerated stop and stay in this mode with a command velocity of zero until the Stop flag is cleared and a new command velocity is specified.

Notes on Limit and Stop Flags

Stop and Limit flags are set by a low level input at their respective pins. The flags can only be cleared when the input to the corresponding pin goes high, signifying that the emergency condition has been corrected, AND a write to the Status register (R07H) is executed. That is, after the emergency pin has been set and cleared, the flag also must be cleared by writing to R07H. Any word that is written to R07H after the emergency pin is set and cleared will clear the emergency flag. The lower four bits of that word will also reconfigure the Status register.

Encoder Input Pins (CHA, CHB, $\overline{\text{INDEX}}$)
The HCTL-1100 accepts TTL compatible outputs from 2 and 3 channel incremental encoders such as the HEDS-5XXX, 6XXX, and 9XXX series encoders. Channels A and B are internally decoded into quadrature counts which increment or decrement the 24-bit position counter. For example, a 500-count encoder is decoded into 2000 quadrature counts per revolution. The position counter will be incremented when Channel B leads Channel A. The Index channel is used only for the Commutator and its function is to serve as a reference point for the internal Ring Counter.

The HCTL-1100 employs an internal 3-bit state delay filter to remove any noise spikes from the encoder inputs to the HCTL-1100. This 3-bit state delay filter requires the encoder inputs to remain stable for three consecutive clock rising edges for an encoder pulse to be considered valid by the HCTL-1100's actual position counter (i.e., an encoder pulse must remain at a logic level high or low for three consecutive clock rising edges for the HCTL-1100's actual position counter to be incremented or decremented.) The designer should therefore generally avoid creating the encoder pulses of less than 3 clock cycles.

The index signal of an encoder is used in conjunction with the Commutator. It resets the internal ring counter which keeps track of the rotor position so that no cumulative errors are generated.

The $\overline{\text{Index}}$ pin of the HCTL-1100 also has a 3-bit filter on its input. The $\overline{\text{Index}}$ pin is *active low and level transition sensitive*. It detects a valid high-to-low transition and qualifies the low input level through the 3-bit filter. At this point, the Index signal is internally detected by the commutator logic. This type of configuraiton allows an Index or $\overline{\text{Index}}$ signal to be used to generate the reference mark for commutator operation as long as the AC specifications for the Index signal are met.

Motor Command Port (MC0-MC7)
The 8-bit Motor Command port consists of register R08H whose data goes directly to external pins MC0-MC7. MC7 is the most significant bit. R08H can be read and written to, however, it should be written to only during the Initialization/Idle mode. During any of the four Control modes, the controller writes the motor command into R08H.

This topic is further discussed in the "Register Section" under "Motor Command Register R08H".

Pulse Width Modulation (PWM) Output Port (Pulse, Sign)
The PWM port consists of the Pulse and Sign pins. The PWM port outputs the motor command as a pulse width modulated signal with the correct polarity. This topic is further discussed in the "Register Section" under "PWM Motor Command Register R09H".

Trapezoid Profile Pin (Prof)
The Trapezoid Profile Pin is internally connected to software flag bit 4 in the Status Register. This flag is also represented by bit 0 in the Flag Register (R00H). See the "Register Section" for more information. Both the Pin and the Flag indicate the status of a trapezoid profile move. When the HCTL-1100 begins a trapezoid move, this flag is set by the controller (a high level appears on the pin), indicating the move is in progress. When the HCTL-1100 finishes the move, this flag is cleared by the controller.

Note that the instant the flag is cleared may not be the same instant the motor stops. The flag indicates the completion of the command profile, not the actual profile. If the motor is stalled during the move, or cannot physically keep up with the move, the flag will be cleared before the move is finished.

INIT/IDLE Pin (INIT)
This pin indicates that the HCTL-1100 is in the INIT/IDLE mode, waiting to begin control. This pin is internally connected to the software flag bit 5 in the Status Register R07H. This flag is also represented by bit 1 in the Flag Register (R00H) (See the "Register Section" for more information).

Commutator Pins (PHA-PHD)
These pins are connected only when using the commutator of the HCTL-1100 to drive a brushless motor or step motor. The four pins can be programmed to energize each winding on a multiphase motor.

Operation of the HCTL-1100

Registers

The HCTL-1100 operation is controlled by a bank of 64 8-bit registers, 35 of which are user accessible. These registers contain command and configuration information necessary to properly run the controller chip. The 35 user-accessible registers are listed in Tables 1 and 2. The register number is also the address. A functional block diagram of the HCTL-1100 which shows the role of the user-accessible registers is also included in Figure 3. The other 29 registers are used by the internal CPU as scratch registers and should not be accessed by the user.

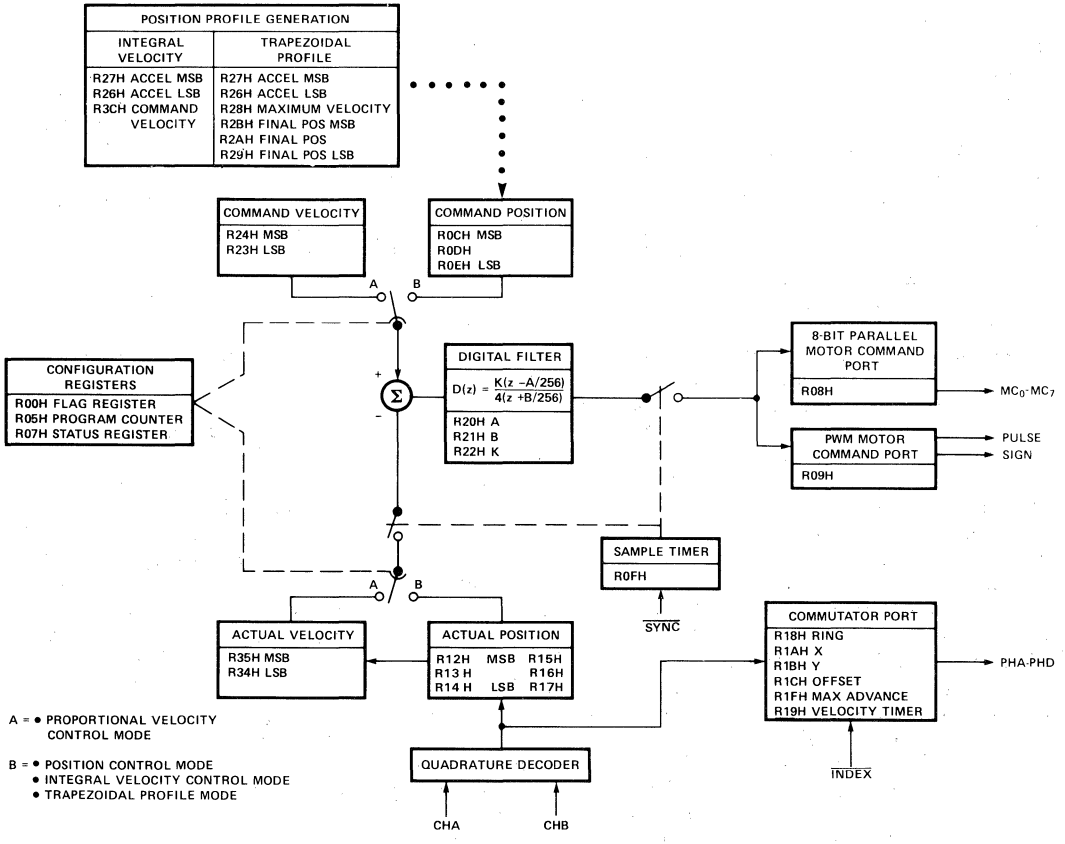


Figure 3. Register Block Diagram

Table 1. Register Reference By Mode

Register		Function	Data Type[1]	User Access
Hex	Dec.			
General Control				
R00H	R00D	Flag Register		r/w
R05H	R05D	Program Counter	scalar	r/w
R07H	R07D	Status Register	-	r/w[2]
R0FH	R15D	Sample Timer	scalar	r/w
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R15H	R21D	Preset Actual Position MSB	2's Complement	w[8]
R16H	R22D	Preset Actual Position	2's Complement	w[8]
R17H	R23D	Preset Actual Position LSB	2's Complement	w[8]
Output Registers				
R07H	R07D	Sign Reversal Inhibit	-	r/w[2]
R08H	R08D	8 bit Motor Command	2's Complement+80H	r/w
R09H	R09D	PWM Motor Command	2's Complement	r/w
Filter Registers				
R20H	R32D	Filter Zero, A	scalar	r/w
R21H	R33D	Filter Pole, B	scalar	r/w
R22H	R34D	Gain, K	scalar	r/w
Commutator Registers				
R07H	R07D	Status Register	-	r/w[2]
R18H	R24D	Commutator Ring	scalar[6,7]	r/w
R19H	R25D	Velocity Timer	scalar	w
R1AH	R26D	X	scalar[6,7]	r/w
R1BH	R27D	Y Phase Overlap	scalar[6,7]	r/w
R1CH	R28D	Offset	2's Complement[7]	r/w
R1FH	R31D	Max. Phase Advance	scalar[6,7]	r/w
Position Control Mode				
R00H	R00D	Flag Register	-	r/w
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R0CH	R12D	Command Position MSB	2's Complement	r/w[3]
R0DH	R13D	Command Position	2's Complement	r/w[3]
R0EH	R14D	Command Position LSB	2's Complement	r/w[3]

Table 1 (continued).

Register		Function	Data Type	User Access
Hex	Dec.			
Trapezoid Profile Control Mode				
R00H	R00D	Flag Register	-	r/w
R07H	R07D	Status Register	-	r/w[2]
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R29H	R41D	Final Position LSB	2's Complement	r/w
R2AH	R42D	Final Position	2's Complement	r/w
R2BH	R43D	Final Position MSB	2's Complement	r/w
R26H	R38D	Acceleration LSB	scalar	r/w
R27H	R39D	Acceleration MSB	scalar[6]	r/w
R28H	R40D	Maximum Velocity	scalar[6]	r/w
Integral Velocity Mode				
R00H	R00D	Flag Register	-	r/w
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R26H	R38D	Acceleration LSB	scalar	r/w
R27H	R39D	Acceleration MSB	scalar[6]	r/w
R3CH	R60D	Command Velocity	2's Complement	r/w
Proportional Velocity Mode				
R00H	R00D	Flag Register	-	r/w
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R23H	R35D	Command Velocity LSB	2's Complement	r/w
R24H	R36D	Command Velocity MSB	2's Complement	r/w
R34H	R52D	Actual Velocity LSB	2's Complement	r
R35H	R53D	Actual Velocity MSB	2's Complement	r

Notes:
1. Consult appropriate section for data format and use.
2. Upper 4 bits are read only.
3. Writing to R0EH (LSB) latches all 24 bits.
4. Reading R14H (LSB) latches data in R12H and R13H.
5. Writing to R13H clears Actual Position Counter to zero.
6. The scalar data is limited to positive numbers (00H to 7FH).
7. The commutator registers (R18H, R1CH, R1FH) have further limits which are discussed in the Commutator section of this data sheet.
8. Writing to R17H (R23D) latches all 24 bits (only in INIT/IDLE mode).

Table 2. Register Reference Table by Register Number

Register					
Hex	Dec.	Function	Mode Used	Data Type	User Access
R00H	R00D	Flag Register	All	–	r/w
R05H	R05D	Program Counter	All	scalar	w
R07H	R07D	Status Register	All	–	r/w[2]
R08H	R08D	8 bit Motor Command Port	All	2's complement + 80H	r/w
R09H	R09D	PWM Motor Command Port	All	2's complement	r/w
R0CH	R12D	Command Position (MSB)	All except Proportional Velocity	2's complement	r/w[3]
R0DH	R13D	Command Position	All except Proportional Velocity	2's complement	r/w[3]
R0EH	R14D	Command Position (LSB)	All except Proportional Velocity	2's complement	r/w[3]
R0FH	R15D	Sample Timer	All	scalar	r/w
R12H	R18D	Read Actual Position (MSB)	All	2's complement	r[4]
R13H	R19D	Read Actual Position	All	2's complement	r[4]/w[5]
R14H	R20D	Read Actual Position (LSB)	All	2's complement	r[4]
R15H	R21D	Preset Actual Position (MSB)	INIT/IDLE	2's complement	w[8]
R16H	R22D	Preset Actual Position	INIT/IDLE	2's complement	w[8]
R17H	R23D	Preset Actual Position (LSB)	INIT/IDLE	2's complement	w[8]
R18H	R24D	Commutator Ring	All	scalar[6,7]	r/w
R19H	R25D	Commutator Velocity Timer	All	scalar	w
R1AH	R26D	X	All	scalar[6]	r/w
R1BH	R27D	Y Phase Overlap	All	scalar[6]	r/w
R1CH	R28D	Offset	All	2's complement[7]	r/w
R1FH	R31D	Maximum Phase Advance	All	scalar[6,7]	r/w
R20H	R32D	Filter Zero, A	All except Proportional Velocity	scalar	r/w
R21H	R33D	Filter Pole, B	All except Proportional Velocity	scalar	r/w
R22H	R34D	Gain, K	All	scalar	r/w
R23H	R35D	Command Velocity (LSB)	Proportional Velocity	2's complement	r/w
R24H	R36D	Command Velocity (MSB)	Proportional Velocity	2's complement	r/w
R26H	R38D	Acceleration (LSB)	Integral Velocity and Trapezoidal Profile	scalar	r/w
R27H	R39D	Acceleration (MSB)	Integral Velocity and Trapezoidal Profile	scalar[6]	r/w
R28H	R40D	Maximum Velocity	Trapezoidal Profile	scalar[6]	r/w
R29H	R41D	Final Position (LSB)	Trapezoidal Profile	2's complement	r/w
R2AH	R42D	Final Position	Trapezoidal Profile	2's complement	r/w
R2BH	R43D	Final Position (MSB)	Trapezoidal Profile	2's complement	r/w
R34H	R52D	Actual Velocity (LSB)	Proportional Velocity	2's complement	r
R35H	R53D	Actual Velocity (MSB)	Proportional Velocity	2's complement	r
R3CH	R60D	Command Velocity	Integral Velocity	2's complement	r/w

Notes:
1. Consult appropriate section for data format and use.
2. Upper 4 bits are read only.
3. Writing to R0EH (LSB) latches all 24 bits.
4. Reading R14H (LSB) latches data in R12H and R13H.
5. Writing to R13H clears Actual Position Counter to zero.
6. The scalar data is limited to positive numbers (00H to 7FH).
7. The commutator registers (R18H, R1CH, R1FH) have further limits which are discussed in the Commutator section of this data sheet.
8. Writing to R17H (R23D) latches all 24 bits (only in INIT/IDLE mode).

Register Descriptions – General Control, Output, Filter, and Commutator

Flag Register (R00H)

The Flag register contains flags F0 through F5. This register is a read/write register. Each flag is set and cleared by writing an 8-bit data word to R00H. When writing to R00H, the upper four bits are ignored by the HCTL-1100, bits 0,1,2 specify the flag address, and bit 3 specifies whether to set (bit=1) or clear (bit=0) the addressed flag.

Flag Descriptions

F0–Trapezoidal Profile Flag – set by the user to execute Trapezoidal Profile Control. The flag is reset by the controller when the move is completed. The status of F0 can be monitored at the Profile pin and in Status register R07H bit 4.

F1–Initialization/Idle Flag – set/cleared by the HCTL-1100 to indicate execution of the Initialization/Idle mode. The status of F1 can be monitored at the Initialization/Idle pin and in bit 5 of the Status register (R07H). The user should not attempt to set or clear F1.

F2–Unipolar Flag – set/cleared by the user to specify Bipolar (clear) or Unipolar (set) mode for the Motor Command port.

F3–Proportional Velocity Control Flag – set by the user to specify Proportional Velocity control.

F4–Hold Commutator flag – set/cleared by the user or automatically by the Align mode. When set, this flag inhibits the internal commutator counters to allow open loop stepping of a motor by using the commutator. (See "Offset register" description in the "Commutator section.")

F5–Integral Velocity Control – set by the user to specify Integral Velocity Control. Also set and cleared by the HCTL-1100 during execution of the Trapezoidal Profile mode. This is transparent to the user except when the Limit flag is set (see "Emergency Flags" section).

Writing to the Flag Register

When writing to the flag register, only the lower four bits are used. Bit 3 indicates whether to set or clear a certain flag, and bits 0,1,and 2 indicate the desired flag. The following table shows the bit map of the Flag register:

Bit Number	Function
7-4	Don't Care
3	1 = set 0 = clear
2	AD2
1	AD1
0	AD0

The following table outlines the possible writes to the Flag Register:

Flag	SET	CLEAR
F0	08H	00H
F1	-	-
F2	0AH	02H
F3	0BH	03H
F4	0CH	04H
F5	0DH	05H

Reading the Flag Register

Reading register R00H returns the status of the flags in bits 0 to 5. For example, if bit 0 is set (logic 1), then flag F0 is set. If bit 4 is set, then flag F4 is set. If bits 0 and 5 are set, then both flags F0 and F5 are set.

The following table outlines the Flag Register Read:

Bit Number	Flag (1 = set) (0 = clear)
8-6	Don't Care
5	F5
4	F4
3	F3
2	F2
1	F1
0	F0

Notes:

1. A soft reset (writing 00H to R05H) will not reset the flags in the flag register. A hard reset ($\overline{\text{RESET}}$ pin low) is required to reset all the flags. The flags can also be reset by writing the proper word to the Flag register as explained above.
2. While in Trapezoid Profile Mode, Flag F0 will be set, and Flag F5 may be set. F5 is used for internal purposes. Both flags will be cleared at the end of the profile.

Program Counter Register (R05H)

The Program Counter, which is a write-only register, executes the preprogrammed functions of the controller. The program counter is used along with the control flags F0, F3, and F5 in the Flag register (R00H) to change control modes. The user can write any of the following four commands to the Program Counter.

Value written to R05H	Action
00H	Software Reset
01H	Enter Init/Idle Mode
02H	Enter Align Mode (only from INIT/IDLE Mode)
03H	Enter Control Mode (only from INIT/IDLE Mode)

These Commands are discussed in more detail in the "Operating Modes" section.

Status Register (R07H)
The Status register indicates the status of the HCTL-1100. Each bit decodes into one signal. All 8 bits are user readable and are decoded as shown below. Only the lower 4 bits can be written to by the user to configure the HCTL-1100. To set or clear any of the lower 4 bits, the user writes an 8-bit word to R07H. The upper 4 bits are ignored. Each of the lower 4 bits directly sets/clears the corresponding bit of the Status register as shown below. For example, writing XXXX0101 to R07H sets the PWM Sign Reversal Inhibit, sets the Commutator Phase Configuration to "3 Phase", and sets the Commutator Count Configuration to "full".

Motor Command Register (R08H)
The 8-bit Motor Command Port consists of register R08H. The register is connected to external pins MC0-MC7. MC7 is the most significant bit. R08H can be read and written to; however, it should be written to only in the Initialization/Idle mode. During any of the four control modes, the HCTL-1100 writes values to register R08H.

The Motor Command Port operates in two modes, bipolar and unipolar, when under control of internal software. Bipolar mode allows the full range of values in R08H (-128D to +127D). The data written to the Motor Command Port by the control algorithms is the internally computed 2's-complement motor command with an 80H offset added. This allows direct interfacing to a DAC. Connecting the Motor Command Port to a DAC, Bipolar mode allows the full voltage swing (positive and negative).

Unipolar mode functions such that with the same DAC circuit, the motor command output is restricted to positive values (80H to FFH) when in a control mode. Unipolar mode is used with multi-phase motors when the commutator controls the direction of movement. (If needed, the Sign pin could be used to indicate direction). In Unipolar mode, the user can still write a negative value to R08H in INIT/IDLE mode.

Unipolar mode or Bipolar mode is programmed by setting or clearing flag F2 in the Flag Register R00H.

Internally, the HCTL-1100 operates on data of 24, 16 and 8-bit lengths to produce the 8-bit motor command, available externally. Many times the computed motor command will be greater than 8 bits. At this point, the motor command is saturated by the controller. The saturated value output by the controller is not the full scale value 00H (00D), or FFH

Table 3. Status Register

Status Bit	Function
0	PWM Sign Reversal Inhibit 0 = off 1 = on
1	Commutator Phase Configuration 0 = 3 phase 1 = 4 phase
2	Commutator Count Configuration 0 = quadrature 1 = full
3	Should always be set to 0
4	Trapezoidal Profile Flag F0 1 = in Profile Control
5	Initialization/Idle Flag F1 1 = in Initialization/Idle Mode
6	Stop Flag 0 = set (Stop triggered) 1 = cleared (no Stop)
7	Limit Flag 0 = set (Limit triggered) 1 = cleared (no Limit)

(255D). The saturated value is adjusted to 0FH (15D) (negative saturation) and F0H (240D) (positive saturation). Saturation levels for the Motor Command port are in Figure 4.

PWM Motor Command Register (R09H)

The PWM port outputs the motor command as a pulse width modulated signal with the correct sign of polarity. The PWM port consists of the Pulse and Sign pins and R09H.

The PWM signal at the Pulse pin has a frequency of External Clock/100 and the duty cycle is resolved into the 100 clocks. (For example, a 2 MHz clock gives a 20 KHz PWM frequency).

The Sign pin gives the polarity of the command. Low output on Sign pin is positive polarity.

The 2's-complement contents of R09H determine the duty cycle and polarity of the PWM command. For example, D8H (–40D) gives a 40% duty cycle signal at the Pulse pin and forces the Sign pin high. Data outside the 64H (+100D) to 9CH (–100D) linear range gives 100% duty cycle. R09H can be read and written to. However, the user should only write to R09H when the controller is in the Initialization/Idle mode. Figure 5 shows the PWM output versus the internal motor command.

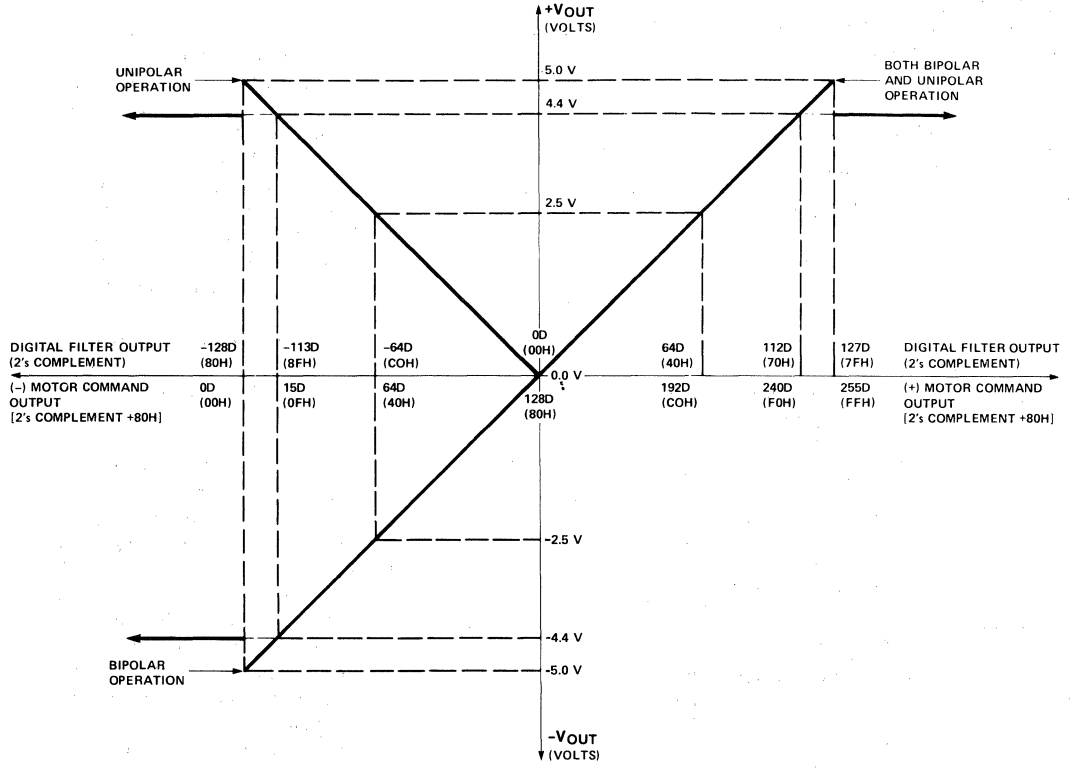


Figure 4. Motor Command Port Output

When any Control mode is being executed, the unadjusted internal 2's-complement motor command is written to R09H. Because of the hardware limit on the linear range (64H to 9CH, ±100D), the PWM port saturates sooner than the 8-bit Motor Command port (00H to FFH, +127D to –128D). When the internal motor command saturates above 8 bits, the PWM port is saturated to the full ±100% duty cycle level. Figure 5 shows the actual values inside the PWM port. Note that the Unipolar flag, F2, does *not* affect the PWM port.

For commutation of brushless motors with the PWM port, only use the Pulse pin from the PWM port as the commutator already contains sign information. (See Figure 9.)

The PWM port has an option that can be used with H-bridge type amplifiers. The option is Sign Reversal Inhibit, which inhibits the Pulse output for one PWM period after a sign polarity reversal. This allows one pair of transistors to turn off before others are turned on and thereby avoids a short across the power supply. Bit 0 in the Status register (R07H) controls the Sign Reversal Inhibit option. Figure 6 shows the output of the PWM port when Bit 0 is set.

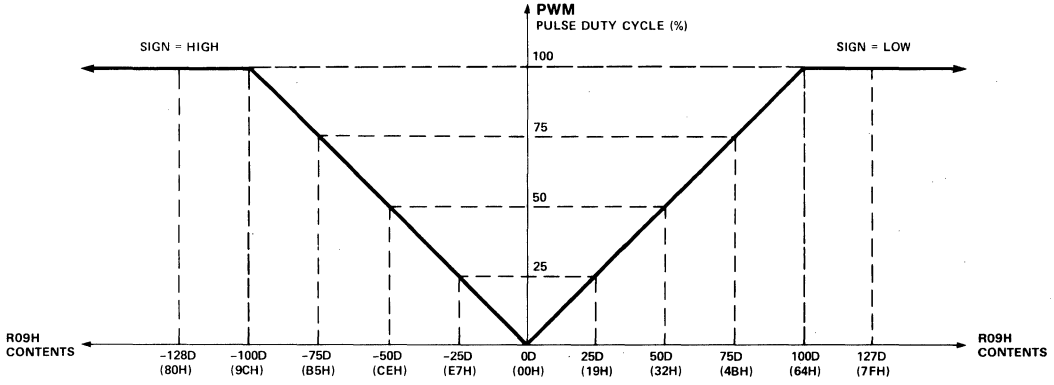


Figure 5. PWM Port Output

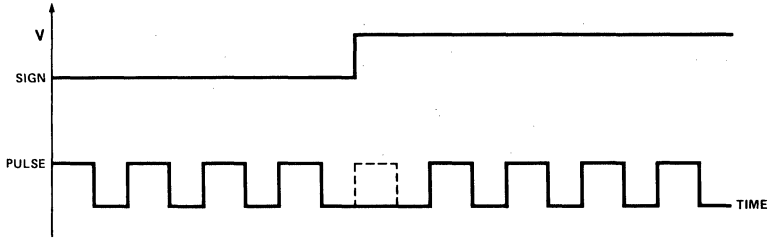


Figure 6. Sign Reversal Inhibit

Actual Position Registers
Read, Clear: R12H,R13H,R14H
Preset : R15H,R16H,R17H

The Actual Position Register is accessed by two sets of registers in the HCTL-1100. When reading the Actual Position from the HCTL-1100, the host processor will read Registers R12H(MSB), R13H, and R14H(LSB). When presetting the Actual Position Register, the processor will write to Registers R15H(MSB), R16H, and R17H(LSB).

When reading the Actual Position registers, the order should be R14H, R13H, R12H. These registers are latched, such that, when reading Register R14H, all three bytes will be latched so that count data does not change while reading three separate bytes.

When presetting the Actual Position Register, write to R15H and R16H first. When R17H is written to, all three bytes are simultaneously loaded into the Actual Position Register.

Note that presetting the Actual Position Registers is only allowed while the HCTL-1100 is in INIT/IDLE mode.

The Actual Position Registers can be simultaneously cleared at any time by writing any value to R13H.

Digital Filter Registers

Zero (A)	R20H
Pole (B)	R21H
Gain (K)	R22H

All control modes use some part of the programmable digital filter D(z) to compensate for closed loop system stability. The compensation D(z) has the form:

$$D(z) = \frac{K\left(z - \frac{A}{256}\right)}{4\left(z + \frac{B}{256}\right)} \qquad [1]$$

where:
z = the digital domain operator
K = digital filter gain (R22H)
A = digital filter zero (R20H)
B = digital filter pole (R21H)

The compensation is a first-order lead filter which in combination with the Sample Timer T (R0FH) affects the dynamic step response and stability of the control system. The Sample Timer, T, determines the rate at which the control algorithm gets executed. All parameters, A, B, K, and T, are 8-bit scalars that can be changed by the user any time.

As shown in equations [2] and [3], the digital filter uses previously sampled data to calculate D(z). This old internally sampled data is cleared when the Initialization/ Idle mode is executed.

In Position Control, Integral Velocity Control, and Trapezoidal Profile Control the digital filter is implemented in the time domain as shown below:

$$MC_n = (K/4)(X_n) - [(A/256)(K/4)(X_{n-1}) + (B/256)(MC_{n-1})] \qquad [2]$$

where:
n = current sample time
n-1 = previous sample time
MC_n = Motor Command Output at n
MC_{n-1} = Motor Command Output at n-1
X_n = (Command Position – Actual Position) at n
X_{n-1} = (Command Position – Actual Position) at n-1

In Proportional Velocity control the digital compensation filter is implemented in the time domain as:

$$MC_n = (K/4)(Y_n) \qquad [3]$$

where:

Y_n = (Command Velocity – Actual Velocity) at n

For more information on system sampling times, bandwidth, and stability, please consult Hewlett-Packard Application Note 1032, *Design of the HCTL-1000's Digital Filter Parameters by the Combination Method.*

Sample Timer Register (R0FH)

The contents of this register set the sampling period of the HCTL-1100. The sampling period is:

$$t = 16(T+1)(1/\text{frequency of the external clock}) \quad [4]$$

where:
T = contents of register R0FH

The Sample Timer has a limit on the minimum allowable sample time depending on the control mode being executed. The limits are given in Table 4 below.

The minimum value limits are to make sure the internal programs have enough time to complete proper execution.

The maximum value of T (R0FH) is FFH (255D). With a 2 MHz clock, the sample time can vary from 64 µsec to 2048 µsec. With a 1 MHz clock, the sample time can vary from 128 µsec to 4096 µsec.

Digital closed-loop systems with slow sampling times have lower stability and a lower bandwidth than similar systems with faster sampling times. To keep the system stability and bandwidth as high as possible the HCTL-1100 should typically be programmed with the fastest sampling time possible. This rule of thumb must be balanced by the needs of the velocity range to be controlled. Velocities are specified to the HCTL-1100 in terms of quadrature encoder counts per sample time. The faster the sampling time, the higher the slowest possible speed.

Hardware Description

The Sample Timer consists of a buffer and a decrement counter. Each time the counter reaches 00H, the Sampler Timer Value T (value written to R0FH) is loaded from the buffer into the counter, which immediately begins to decrement from T.

Writing to the Sample Timer Register

Data written to R0FH will be latched into the internal buffer and used by the counter after it completes the present sample time cycle by decrementing to 00H. The next sample time will use the newly written data.

Reading the Sample Timer Register

Reading R0FH gives the values directly from the decrementing counter. Therefore, the data read from R0FH will have a value anywhere between T and 00H, depending where in the sample time cycle the counter is.

Example –
1. On reset, the value of the timer is pre-set to 40H.
2. Reading R0FH shows
   3EH . . . 2BH . . . 08H . . .
   3CH . . .

Synchronizing Multiple Axes

Synchronizing multiple axes with HCTL-1100s can be achieved by using the $\overline{\text{SYNC}}$ pin as explained in the Pin Discussion section. Some users may not only want to synchronize several HCTL-1100s but also follow custom profiles for each axis. To do this, the user may need to write a new command position or command velocity during each sample time for the duration of the profile. In this case, data written to the HCTL-1100 has to be coordinated with the Sample Timer. This is so that only one command position or velocity is received during any one sample period, and that it is written at the proper time within a sample period.

At the beginning of each sample period, the HCTL-1100 is performing calculations and executions. New command positions and velocities should not be written to the HCTL-1100 during this time. If they are, the calculations may be thrown off and cause unpredictable control.

The user can read the Sample Timer Register to avoid writing too early during a sample period. Since the Sample Timer Register continuously counts down from its programmed value, the user can check if enough time has passed in the sample period to insure the completion of the internal calculations. The length of time needed by the HCTL-1100 to do

Table 4.

Control Mode	R0FH Contents Minimum Limit
Position Control	07H(07D)
Proportional Velocity Control	07H(07D)
Trapezoidal Profile Control	0FH(15D)
Integral Velocity Control	0FH(15D)

its calculations is given by the Minimum Limits of R0FH (Sample Timer Register) as shown in Table 4. For Position Control Mode, the user should wait for the Sample Timer to count down 07H from its programmed value before writing the next command position or velocity. If the programmed sample timer value is 39H, wait until the Sample Timer Register reads 32H. Writing between 32H and 00H will make the command information available for the next sample period.

Commutator

Status Register	(R07H)
Commutator Ring	(R18H)
X Register	(R1AH)
Y Phase Overlap	(R1BH)
Offset	(R1CH)
Max. Phase Advance	(R1FH)
Velocity Timer	(R19H)

The commutator is a digital state machine that is configured by the user to properly select the phase sequence for electronic commutation of multiphase motors. The Commutator is designed to work with 2, 3, and 4-phase motors of various winding configurations and with various encoder counts. Along with providing the correct phase enable sequence, the Commutator provides programmable phase overlap, phase advance, and phase offset.

Phase overlap is used for better torque ripple control. It can also be used to generate unique state sequences which can be further decoded externally to drive more complex amplifiers and motors.

Phase advance allows the user to compensate for the frequency characteristics of the motor/amplifier combination. By advancing the phase enable command (in position), the delay in reaction of the motor/amplifier combination can be offset and higher performance can be achieved.

Phase offset is used to adjust the alignment of the commutator output with the motor torque curves. By correctly aligning the HCTL-1100's commutator output with the motor's torque curves, maximum motor output torque can be achieved.

The inputs to the Commutator are the three encoder signals, Channel A, Channel B, and Index, and the configuration data stored in registers.

The Commutator uses both channels and the index pulse of an incremental encoder. The index pulse of the encoder must be physically aligned to a known torque curve location because it is used as the reference point of the rotor position with respect to the Commutator phase enables.

The index pulse should be permanently aligned during motor encoder assembly to the last motor phase. This is done by energizing the last phase of the motor during assembly and permanently attaching the encoder codewheel to the motor shaft such that the index pulse is active as shown in Figures 7 and 8. Fine tuning of alignment for commutation purposes is done electronically by the Offset register (R1CH) once the complete control system is set up.

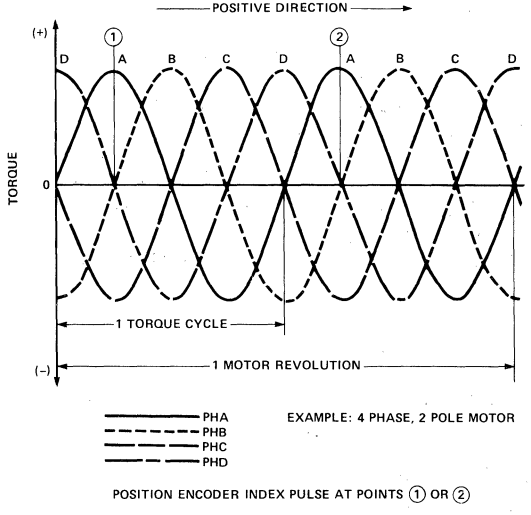


Figure 7. Index Pulse Alignment to Motor Torque Curves.

Each time an index pulse occurs, the internal commutator ring counter is reset to 0. The ring counter keeps track of the current position of the rotor based on the encoder feedback. When the ring counter is reset to 0, the Commutator is reset to its origin (last phase going low, Phase A going high) as shown in Figure 10.

The output of the Commutator is available as PHA, PHB, PHC, and PHD. The HCTL-1100's commutator acts as the electrical equivalent of the mechanical brushes in a motor. Therefore, the outputs of the commutator provide only proper phase sequencing for bidirectional operation. The magnitude information is provided to the motor via the Motor Command and PWM ports. The outputs of the commutator must be combined with the outputs of one of the motor ports to provide proper DC brushless and stepper motor control. Figure 9 shows an example of circuitry which uses the outputs of the commutator with the Pulse output of the PWM port to control a DC brushless or stepper motor. A similar procedure could be used to combine the commutator outputs PHA-PHD with a linear amplifier interface output (Figure 16) to create a linear amplifier system.

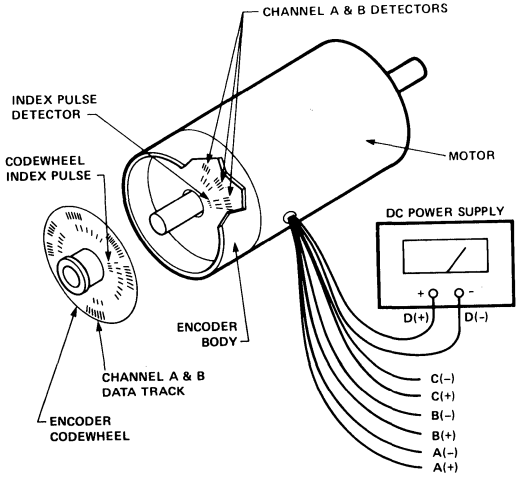


Figure 8. Codewheel Index Pulse Alignment.

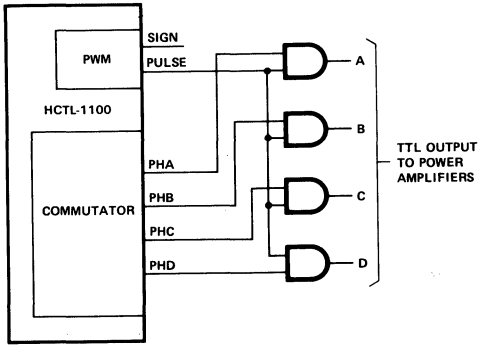


Figure 9. PWM Interface to Brushless DC Motors.

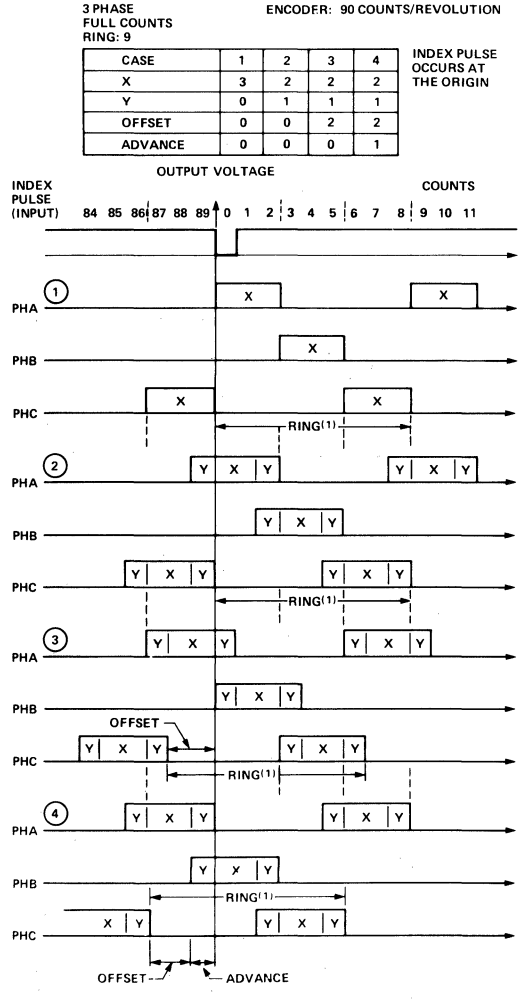


Figure 10. Commutator Configuration.

The Commutator is programmed by the data in the following registers. Figure 10 shows an example of the relationship between all the parameters.

Status Register (R07H)

Bit #1- 0 = 3-phase configuration, PHA, PHB, and PHC are active outputs.
1 = 4-phase configuration, PHA – PHD are active outputs.

Bit #2- 0 = Rotor position measured in quadrature counts (4x decoding).
1 = Rotor position measured in full counts (1 count = 1 codewheel bar and space.)

Bit #2 only affects the commutator's counting method. This includes the Ring register (R18H), the X and Y registers (R1AH & R1BH), the Offset register (R1CH), the Velocity Timer register (R19H), and the Maximum Advance register (R1FH).

Quadrature counts (4x decoding) are always used by the HCTL-1100 as a basis for position, velocity, and acceleration control.

Ring Register (R18H)

The Ring register is defined as 1 electrical cycle of the commutator which corresponds to 1 torque cycle of the motor. The Ring register is scalar and determines the length of the commutation cycle measured in full or quadrature counts as set by bit #2 in the Status register (R07H). The value of the ring must be limited to the range of 0 to 7FH.

X Register (R1AH)

This register contains scalar data which sets the interval during which only one phase is active.

Y Register (R1BH)

This register contains scalar data which set the interval during which two sequential phases are both active. Y is phase overlap. X and Y must be specified such that:

$$X + Y = \text{Ring}/(\#\text{ of phases}) \quad [5]$$

These three parameters define the basic electrical commutation cycle.

Offset Register (R1CH)

The Offset register contains two's-complement data which determines the relative start of the commutation cycle with respect to the index pulse. Since the index pulse must be physically referenced to the rotor, offset performs fine alignment between the electrical and mechanical torque cycles.

The Hold Commutator flag (F4) in the Status register (R07H) is used to decouple the internal commutator counters from the encoder input. Flag (F4) can be used in conjunction with the Offset register to allow the user to advance the commutator phases open loop. This technique may be used to create a custom commutator alignment procedure. For example, in Figure 10, case 1, for a three-phase motor where the ring = 9, X = 3, and Y = 0, the phases can be made to advance open loop by setting the Hold Commutator flag (F4) in the Flag register (R07H). When the values 0, 1, or 2 are written to the Offset register, phase A will be enabled. When the values 3, 4 or 5 are written to the Offset register, phase B will be enabled. And, when the values 6, 7, or 8 are written to the Offset register, phase C will be enabled. No values larger than the value programmed into the Ring register should be programmed into the Offset register.

Phase Advance Registers (R19H, R1FH)

The Velocity Timer register and Maximum Advance register linearly increment the phase advance according to the measured speed for rotation up to a set maximum.

The Velocity Timer register (R19H) contains scalar data which determines the amount of phase advance at a given velocity. The phase advance is interpreted in the units set for the Ring counter by bit #2 in R07H. The velocity is measured in revolutions per second.

$$\text{Advance} = N_f v \Delta t \quad [6]$$

$$\text{where: } \Delta t = \frac{16\,(\text{R19H} + 1)}{\text{f external clk}} \quad [7]$$

N_f = full encoder counts/revolution.
v = velocity (revolutions/second)

The Maximum Advance register (R1FH) contains scalar data which sets the upper limit for phase advance regardless of rotor speed.

Figure 11 shows the relationship between the Phase Advance registers. Note: If the phase advance feature is not used, set both R19H and R1FH to 0.

Commutator Constraints and Use

When choosing a three-channel encoder to use with a DC brushless or stepper motor, the user should keep in mind that the number of quadrature encoder counts (4x the number of slots in the encoder's codewheel) must be an integer multiple (1x, 2x, 3x, 4x, 5x, etc.) of the number of pole pairs in the DC brushless motor or steps in a stepper motor. To take full advantage of the commutator's overlap feature, the number of quadrature counts should be at least 3 times the number of pole pairs in the DC brushless motor or steps in the stepper motor. For example, a 1.8°, (200 step/revolution) stepper motor should employ at least a 150 slot codewheel = 600 quadrature counts/revolution = 3 x 200 steps/revolution).

There are several numerical constraints the user should be aware of to use the Commutator.

The parameters of Ring, X, Y, and Max Advance must be positive numbers (00H to 7FH). Additionally, the following equation must be satisfied:

(-128D) 80H ≤ 3/2 Ring + Offset ± Max Advance ≤ 7FH (127D) [8]

In order to utilize the greatest flexibility of the Commutator, it must be realized that the Commutator works on a circular ring counter principle, whose range is defined by the Ring register (R18H). This means that for a ring of 96 counts and a needed offset of 10 counts, numerically the Offset register can be programmed as 0AH (10D) or AAH (-86D), the latter satisfying Equation 8.

If bit #2 in the Status register is set to allow the commutator to count in full counts, a higher resolution codewheel may be chosen for precise motor control without violating the commutator constraints equation (Equation 8).

Example: Suppose you want to commutate a 3-phase 15 deg/step Variable Reluctance Motor attached to a 192 count encoder.

1. Select 3-phase and quadrature mode for commutator by writing 0 to R07H.
2. With a 3-phase 15 degree/step Variable Reluctance motor the torque cycle repeats every 45 degrees or 8 times/revolution.
3. Ring register
$$= \frac{(4)(192)\ \text{counts/revolution}}{8/\text{revolution}}$$
= 96 quadrature counts
= 1 commutation cycle
4. By measuring the motor torque curve in both directions, it is determined that an offset of 3 mechanical degrees, and a phase overlap of 2 mechanical degrees is needed.
$$\text{Offset} = 3° \frac{(4)(192)}{360°}$$
≅ 6 quadrature counts

To create the 3 mechanical degree offset, the Offset

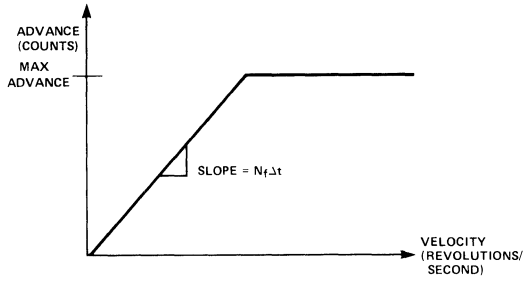


Figure 11. Phase Advance vs. Motor Velocity.

register (R1CH) could be programmed with either A6H (-90D) or 06H (+06D). However, because 06H (+06D) would violate the commutator constraints Equation 8, A6H (-90D) is used.

$$Y = \text{overlap} = \frac{(2°)\,(4)\,(192)}{360°} \cong 4$$

$$X + Y = 96/3$$

Therefore, X = 28
Y = 4

For the purposes of this example, the Velocity Timer and Maximum Advance are set to 0.

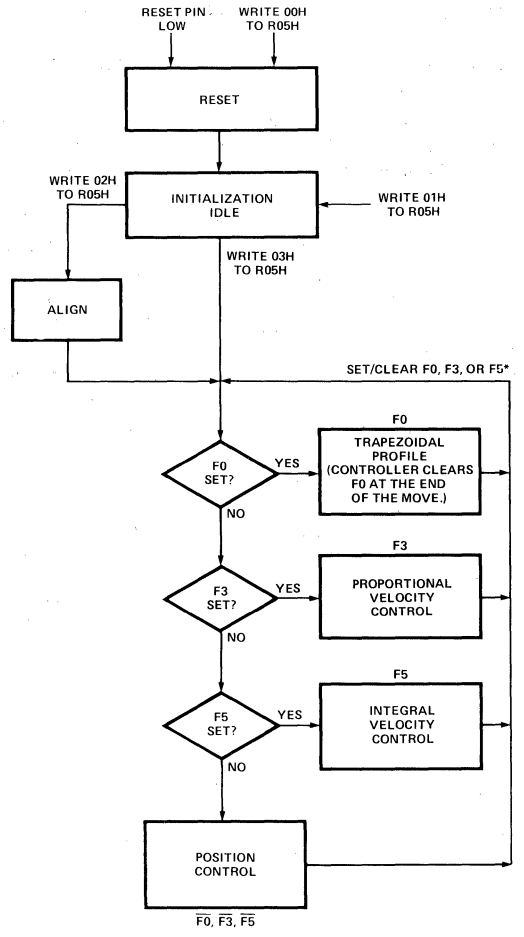
Operation Flowchart

The HCTL-1100 executes any one of three setup routines or four control modes selected by the user. The three setup routines include:
- Reset
- Initialization/Idle
- Align.

The four control modes available to the user include:
- Position Control
- Proportional Velocity Control
- Trapezoidal Profile Control
- Integral Velocity Control

The HCTL-1100 switches from one mode to another as a result of one of the following three mechanisms:
1. The user writes to the Program Counter.
2. The user sets/clears flags F0, F3, or F5 by writing to the Flag register (R00H).
3. The controller switches automatically when certain initial conditions are provided by the user.

This section describes the function of each setup routine and control mode and the initial conditions which must be provided by the user to switch from one mode to another. Figure 12 shows a flowchart of the setup routines and control modes, and shows the commands required to switch from one mode to another.



*Only one flag should be set at a time.

Figure 12. Operation Flowchart.

Setup Modes

Hard Reset

Executed by:
-Pulling the RESET pin low (required at power up)

When a hard reset is executed (RESET pin goes low), the following conditions occur:
- All output signal pins are held low except Sign, Data bus, and Motor Command.
- All flags (F0 to F5) are cleared.
- The Pulse pin of the PWM port is set low while the Reset pin is held low. After the Reset pin is released (goes high) the Pulse pin goes high for one cycle of the external clock driving the HCTL-1100. The Pulse pin then returns to a low output.
- The Motor Command port (R08H) is preset to 80H (128D).
- The Commutator logic is cleared.
- The I/O control logic is cleared.
- A soft reset is automatically executed.

Soft Reset

Executed by:
- Writing 00H to R05H, or
- Automatically called after a hard reset

When a soft reset is executed, the following conditions occur:
- The digital filter parameters are preset to
  A (R20H) = E5H (229D)
  B (R21H) = K (R22H) = 40H (64D)
- The Sample Timer (R0FH) is preset to 40H (64D).
- The Status register (R07H) is cleared.
- The Actual Position Counters (R12H, R13H, R14H) are cleared to 0.

From Reset mode, the HCTL-1100 goes automatically to Initialization/Idle mode.

Initialization/Idle

Executed by:
- Writing 01H to R05H, or
- Automatically executed after a hard reset, soft reset, or
- Limit pin goes low.

The Initialization/Idle mode is entered either automatically from Reset, by writing 01H to the Program Counter (R05H) under any conditions, or pulling the Limit pin low.

In the Initialization/Idle mode, the following occur:
- The Initialization/Idle flag (F1) is set.
- The PWM port R09H is set to 00H (zero command).
- The Motor Command port (R08H) is set to 80H (128D) (zero command).
- Previously sampled data stored in the digital filter is cleared.

It is at this point that the user should pre-program all the necessary registers needed to execute the desired control mode. The HCTL-1100 stays in this mode (idling) until a new mode command is given.

Align

Executed by:
- Writing 02H to R05H

The Align mode is executed only when using the commutator feature of the HCTL-1100. This mode automatically aligns multiphase motors to the HCTL-1100's internal Commutator.

The Align mode can be entered only from the Initialization/Idle mode by writing 02H to the Program Counter register (R05H).

Before attempting to enter the Align mode, the user should clear all control mode flags and set both the Command Position registers (R0CH, R0DH, and R0EH) and the Actual Position registers (R12H, R13H, and R14H) to zero. After the Align mode has been executed, the HCTL-1100 will automatically enter the Position Control mode and go to position zero. By following this procedure, the largest movement in the Align mode will be one torque cycle of the motor.

The Align mode assumes: the encoder index pulse has been physically aligned to the last motor phase during encoder/motor assembly, the Commutator parameters have been correctly preprogrammed (see the section called Commutator for details), and a hard reset has been executed while the motor is stationary.

The Align mode first disables the Commutator and with open loop control enables the first phase (PHA) and then the last phase (PHC or PHD) to orient the motor on the last phase torque detent. Each phase is energized for 2048 system sampling periods (t). For proper operation, the motor must come to a complete stop during the last phase enable. At this point the Commutator is enabled and commutation is closed loop.

The HCTL-1100 then automatically switches from the Align mode to Position Control mode.

Control Modes

Control flags F0, F3, and F5 in the Flag register (R00H) determine which control mode is executed. Only one control flag can be set at a time. After one of

these control flags is set, the control modes are entered either automatically from Align or from the Initialization/Idle mode by writing 03H to the Program Counter (R05H).

Position Control Mode

Flags: F0 Cleared
F3 Cleared
F5 Cleared

Registers Used:

Register		Function
R00H	R00D	Flag Register
R12H	R18D	Read Actual Position MSB
R13H	R19D	Read Actual Position
R14H	R20D	Read Actual Position LSB
R0CH	R12D	Command Position MSB
R0DH	R13D	Command Position
R0EH	R14D	Command Position LSB

Position Control performs point-to-point position moves with no velocity profiling. The user specifies a 24-bit position command, which the controller compares to the 24-bit actual position. The position error is calculated, the full digital lead compensation is applied and the motor command is output.

The controller will remain position-locked at a destination until a new position command is given.

The actual and command position data is 24-bit two's-complement data stored in six 8-bit registers. Position is measured in encoder quadrature counts.

The command position resides in R0CH (MSB), R0DH, R0EH (LSB). Writing to R0EH latches all 24 bits at once for the control algorithm. Therefore, the command position is written in the sequence R0CH, R0DH and R0EH. The command registers can be read in any desired order.

The actual position resides in R12H (MSB), R13H, and R14H (LSB). Reading R14H latches the upper two bytes into an internal buffer. Therefore, Actual Position registers are read in the order of R14H, R13H, and R12H for correct instantaneous position data.

The largest position move possible in Position Control mode is 7FFFFFH (8,388,607D) quadrature encoder counts.

Proportional Velocity Mode

Flags: F0 Cleared
F3 Set
F5 Cleared

Registers Used:

Register		Function
R00H	R00D	Flag Register
R23H	R35D	Command Velocity LSB
R24H	R36D	Command Velocity MSB
R34H	R52D	Actual Velocity LSB
R35H	R53D	Actual Velocity MSB

Proportional Velocity Control performs control of motor speed using only the gain factor, K, for compensation. The dynamic pole and zero lead compensation are not used. (See the "Digital Filter" section of this data sheet.)

```
Example Code to Program Position Moves

    { Begin }
        Hard Reset { HCTL-1100 goes into INIT/IDLE Mode }

        Initialize Filter, Timer, Command Position Registers

        Write 03H to Register R05H
            { HCTL-1100 is now in Position Mode }

        Write Desired Command Position to Command Position Registers
            { Controller Moves to new position }

        Continue writing in new Command Positions
    { end }
```

The command and actual velocity are 16-bit two's-complement words.

The command velocity resides in registers R24H (MSB) and R23H (LSB). These registers are unlatched which means that the command velocity will change to a new velocity as soon as the value in either R23H or R24H is changed. The registers can be read or written to in any order.

R24H	R23H
IIII IIII	IIII FFFF

COMMAND VELOCITY FORMAT

The units of velocity are quadrature counts/sample time. To convert from rpm to quadrature counts/sample time, use the formula shown below:

$$Vq = (Vr)(N)(t)(0.01667/rpm\text{-}sec) \quad [9]$$

Where:
Vq = velocity in quadrature counts/sample time
Vr = velocity in rpm
N = 4 times the number of slots in the codewheel (i.e., quadrature counts).
t = The HCTL-1100 sample time in seconds. (See the section on the HCTL-1100's Sample Timer register).

Because the Command Velocity registers (R24H and R23H) are internally interpreted by the HCTL-1100 as 12 bits of integer and 4 bits of fraction, the host processor must multiply the desired command velocity (in quadrature counts/sample time) by 16 before programming it into the HCTL-1100's Command Velocity registers.

The actual velocity is computed only in this algorithm and stored in scratch registers R35H (MSB) and R34H (LSB). There is no fractional component in the actual velocity registers and they can be read in any order.

The controller tracks the command velocity continuously until new mode command is given. The system behavior after a new velocity command is governed only by the system dynamics until a steady state velocity is reached.

Integral Velocity Mode

Flags: F0 Cleared
F3 Cleared
F5 Set to begin move

Registers Used:

Register		Function
R00H	R00D	Flag Register
R26H	R38D	Acceleration LSB
R27H	R39D	Acceleration MSB
R3CH	R60D	Command Velocity

Integral Velocity Control performs continuous velocity profiling which is specified by a command velocity and command acceleration. Figure 13 shows the capability of this control algorithm.

The user can change velocity and acceleration any time to continuously profile velocity in time. Once the specified velocity is reached, the HCTL-1100 will maintain that velocity until a new command is specified. Changes between actual velocities occur at the presently specified linear acceleration.

The command velocity is an 8-bit two's-complement word

```
Example Code for Programming Proportional Velocity Mode

    { Begin }
        Hard Reset { HCTL-1100 goes into INIT/IDLE Mode }

        Initialize Filter, Timer, Command Position Registers

        Write 03H to Register R05H
            { HCTL-1100 is now in Position Mode }

        Write Desired Command Velocity (if needed)

        Set Flag F3 {Proportional Velocity Move Begins}

        { System ramps to Command Velocity }

        Continue writing new Command Velocities
    {end}
```

stored in R3CH. The units of velocity are quadrature counts/sample time.

The conversion from rpm to quadrature counts/sample time is shown in equation 9. The Command Velocity register (R3CH) contains only integer data and has no fractional component.

While the overall range of the velocity command is 8 bits, two's-complement, the difference between any two sequential commands cannot be greater than 7 bits in magnitude (i.e., 127 decimal). For example, when the HCTL-1100 is executing a command velocity of 40H (+64D), the next velocity command must fall in the range of 7FH (+127D), the maximum command range, C1H (-63D), the largest allowed difference.

The command acceleration is a 16-bit scalar word stored in R27H and R26H. The upper byte (R27H) is the integer part and the lower byte (R26H) is the fractional part provided for resolution. The integer part has

R27H	R26H
0IIIIIII	FFFFFFFF/256

Command Acceleration Format

a range of 00H to 7FH. The contents of R26H are internally divided by 256 to produce the fractional resolution.

The units of acceleration are quadrature counts/sample time squared.

To convert from rpm/sec to quadrature counts/[sample time]^2, use the formula shown below:

$$Aq = (Ar)(N)(t^2)(0.01667/rpm\text{-}sec) \quad [10]$$

Where:

Aq = Acceleration in quadrature counts/[sample time]^2

Ar = Acceleration in rpm/sec

N = 4 times the number of slots in the codewheel (i.e., quadrature counts)

t = The HCTL-1100 sample time in seconds. (See the section on the HCTL-1100's Sample Timer register).

Because the Command Acceleration registers (R27H and R26H) are internally interpreted by the HCTL-1100 as 8 bits of integer and 8 bits of fraction, the host processor must multiply the desired command acceleration (in quadrature counts/[sample time]^2) by 256 before programming it into the HCTL-1100's Command Acceleration registers.

Internally, the controller performs velocity profiling through position control.

Each sample time, the internal profile generator uses the information which the user has programmed into the Command Velocity register (R3CH) and the Command Acceleration registers (R27H and R26H) to determine the value which will be automatically loaded into the Command Position registers (R0CH, R0DH, and R0EH). After the new command position has been generated, the difference between the value in the Actual Position registers (R12-R13H, and R14H) and the new value in the Command Position registers is calculated as the new position error. This new position error is used by the full digital compensation filter to compute a new motor command output by this sample time. The register block in Figure 3 further shows how the internal profile generator works in Integral Velocity mode. In control theory terms, integral compensation has been added and therefore, this system has zero steady-state error.

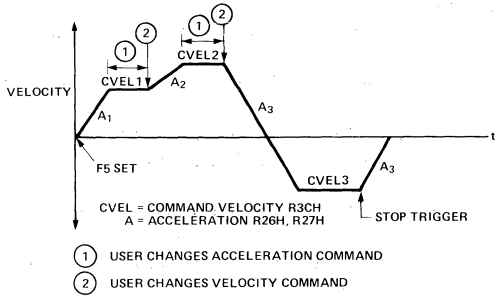


Figure 13. Integral Velocity Modes.

Although Integral Velocity Control mode has the advantage over Proportional Velocity mode of zero steady state velocity error, its disadvantage is that the closed loop stability is more difficult to achieve. In Integral Velocity Control mode the system is actually a position control system and therefore the complete dynamic compensation D(z) is used.

If the external Stop flag F6 is set during this mode signalling an emergency situation, the controller automatically decelerates to zero velocity at the presently specified acceleration factor and stays in this condition until the flag is cleared. The user then can specify new velocity profiling data.

Trapezoid Profile Mode

Flags: F0 Set to begin move
F3 Cleared
F5 Cleared

Registers Used:

Register		Function
R00H	R00D	Flag Register
R07H	R07D	Status Register
R12H	R18D	Read Actual Position MSB
R13H	R19D	Read Actual Position
R14H	R20D	Read Actual Position LSB
R29H	R41D	Final Position LSB
R2AH	R42D	Final Position
R2BH	R43D	Final Position MSB
R26H	R38D	Acceleration LSB
R27H	R39D	Acceleration MSB
R28H	R40D	Maximum Velocity

Trapezoid Profile Control performs point-to-point position moves and profiles the velocity trajectory to a trapezoid or triangle. The user specifies only the desired final position, acceleration and maximum velocity. The controller computes the necessary profile to conform to the command data. If maximum velocity is reached before the distance halfway point, the profile will be trapezoidal, otherwise the profile will be triangular. Figure 14 shows the possible trajectories with Trapezoidal Profile Control.

The command data for Trapezoidal Profile Control mode consists of a final position, a command acceleration, and a

```
Example Code for Programming Integral Velocity Mode

     (Begin)
          Hard Reset {HCTL-1100 goes into INIT/IDLE Mode}

          Initialize Filter, Timer, Command Position Registers

          Write 03H to Register R05H
               {HCTL-1100 is now in Position Mode}

          Write Desired Acceleration (if needed)

          Write Desired Maximum Velocity (if needed)

          Set Flag F5 {Integral Velocity Move Begins}

          {System ramps to Maximum Velocity}

          Continue writing new Accelerations and Velocities
     { end }
```

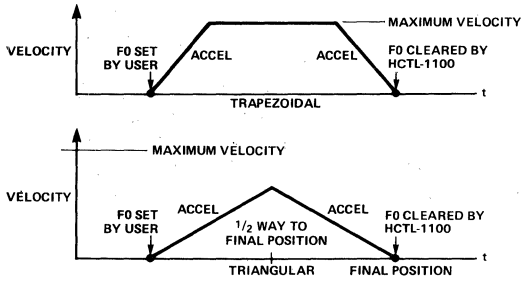


Figure 14. Trapezoidal Profile Mode.

maximum velocity. The 24-bit, two's-complement final position is written to registers R2BH, (MSB), R2AH, and R29H (LSB). The 16-bit command acceleration resides in registers R27H (MSB) and R26H (LSB). The command acceleration has the same integer and fraction format as discussed in the Integral Velocity Control mode section. The 7-bit maximum velocity is a scalar value with the range of 00H to 7FH (0D to 127D). The maximum velocity has the units of quadrature counts per sample time, and resides in register R28H. The command data registers may be read or written to in any order.

The internal profile generator produces a position profile using the present Command Position (R0CH-R0EH) as the starting point and the Final Position (R2BH-R29H) as the end point.

Once the desired data is entered, the user sets flag F0 in the Flag register (R00H) to commence motion (if the HCTL-1100 is already in Position Control mode).

When the profile generator sends the last position command to the Command Position registers to complete the trapezoidal move, the controller clears flag F0. The HCTL-1100 then automatically goes to Position Control mode with the final position of the trapezoidal move as the command position.

When the HCTL-1100 clears flag F0 it does NOT indicate that the motor and encoder are at the final position NOR that the motor and encoder have stopped. The flag indicates that the command profile has finished. The motor and encoder's true position can only be determined by reading the Actual Position registers. The only way to determine if the motor and encoder have stopped is to read the Actual Position registers at successive intervals.

The status of the Profile flag can be monitored both in the Status register (R07) and at the external Profile pin at any time. While the Profile flag is high NO new command data should be sent to the controller.

Each sample time, the internal profile generator uses the information which the user has programmed into the Maximum Velocity register (R28H), the Command Acceleration registers (R27H and R26H), and the Final Position registers (R2BH, R2AH, and R29H) to determine the value which will be automatically loaded into the Command Position registers (R0EH, R0DH, and R0CH). After the new command position has been generated, the difference between the value in the Actual Position registers (R12H, R13H, and R14H) and the new value in the Command Position registers is calculated as the new position error. This new position error is used by the full digital compensation filter to compute a new motor command output for the sample time. (The register block diagram in Figure 3 further shows how the internal profile generator works in Trapezoidal Profile mode.)

Example Code for Programming Trapezoid Moves

```
{ Begin }
     Hard Reset { HCTL-1100 goes into INIT/IDLE Mode }

     Inititalize Filter, Timer, Command Position Registers

     Write 03H to Register R05H
        { HCTL-1100 is now in Position Mode }

     { Profile #1}

     Write Desired Acceleration

     Write Desired Maximum Velocity

     Write Final Position

     Set Flag F0 {Trapezoid Move Begins, PROF pin goes high}

     Poll PROF pin until it goes low (Move is complete)

     { Profile #2}

     Write Desired Acceleration

     Write Desired Maximum Velocity

     Write Final Position

     Set Flag F0 {Trapezoid Move Begins, PROF pin goes high}

     Poll PROF pin until it goes low (Move is complete)

     { Repeat }
     .
     .
     .
     .
{ end }
```

Applications of the HCTL-1100

Interfacing the HCTL-1100 to Host Processors

The HCTL-1100 looks to the host microprocessor like a bank of 8-bit registers to which the host processor can read and write (i.e., the host processor treats the HCTL-1100 like RAM). The data in these registers controls the operation of the HCTL-1100. The host processor communicates to the HCTL-1100 over a bidirectional multiplexed 8-bit data bus. The four I/O control lines. $\overline{ALE}$, $\overline{CS}$, $\overline{OE}$, and R/$\overline{W}$ execute the data transfers (see Figure 15).

There are three different timing configurations which can be used to give the user greater flexibility to interface the

HCTL-1100 to most microprocessors (see Timing diagrams). They are differentiated from one another by the arrangement of the $\overline{ALE}$ signal with respect to the $\overline{CS}$ signal. The three timing configurations are listed below.

1. $\overline{ALE}$, $\overline{CS}$ non-overlapped
2. $\overline{ALE}$, $\overline{CS}$ overlapped
3. $\overline{ALE}$ within $\overline{CS}$

Any I/O operation starts by asserting the $\overline{ALE}$ signal which starts sampling the external bus into an internal address latch. Rising $\overline{ALE}$ or falling $\overline{CS}$ during $\overline{ALE}$ stops the sampling into the address latch.

$\overline{CS}$ low after rising $\overline{ALE}$ samples the external bus into the data latch. Rising $\overline{CS}$ stops the sampling into the data latch, and starts the internal synchronous process.

In the case of a write, the data in the data latch is written into the addressed location. In the case of a read, the addressed location is written into an internal output latch. $\overline{OE}$ low enables the internal output latch onto the external bus. The $\overline{OE}$ signal and the internal output latch allow the I/O port to be flexible and avoid bus conflicts during read operations.

It is important that the host microprocessor does not attempt to perform too many I/O operations in a single sample time of the HCTL-1100. Each I/O operation interrupts the execution of the HCTL-1100's internal code for 1 clock cycle. Although extra clock cycles have been allotted in each sample time for I/O operations, the number of extra cycles is reduced as the value programmed into the Sample Timer register (R0FH) is reduced.

Table 5 shows the maximum number of I/O operations allowed under the given conditions.

The number of external clock cycles available for I/O operations in any of the four control modes can be increased by increasing the value in the Sample Timer register (R0FH).

For every unit increase in the Sample Timer register (R0FH) above the minimums shown in Table 5 the user may perform 16 additional I/O operations per sample time.

Interfacing the HCTL-1100 to Amplifiers and Motors

The Motor Command port is the ideal interface to an 8-bit DAC, configured for bipolar output. The data written to the 8-bit Motor Command port by the control algorithms is the internally computed 2's-complement motor command with an 80H offset added. This allows direct interfacing to a DAC. Figure 16 shows a typical DAC interface to the HCTL-1100. An inexpensive DAC, such as MC1408 or equivalent, has its digital inputs directly connected to the Motor Command port. The DAC produces an output current which is converted to a voltage by an operational amplifier. R_O and R_G control the analog offset and gain. The circuit is easily adjusted for +5 V to –5 V operation by first writing 80H to R08H and adjusting R_O for 0 V output. Then FFH is written to R08H and R_G is adjusted until the output is 5 V. Note that 00H in R08H corresponds to –5 V out.

Figure 17 shows an example of how to interface the HCTL-1100 to an H-bridge amplifier. An H-bridge amplifier allows bipolar motor operation with a unipolar power supply. The Sign Reversal Inhibit feature prevents all transistors from being on at the same time when the direction of motion is reversed.

Table 5. Maximum Number of I/O Allowed

Sample Timer Register Value	Operating Mode	Maximum Number of I/O Operations Allowed per Sample
07H (07D)	Position Control or Prop. Vel. Control	5
OFH (15D)	Position Control or Prop. Vel. Control	133
	Trapezoidal Prof. or Integral Vel. Control	6

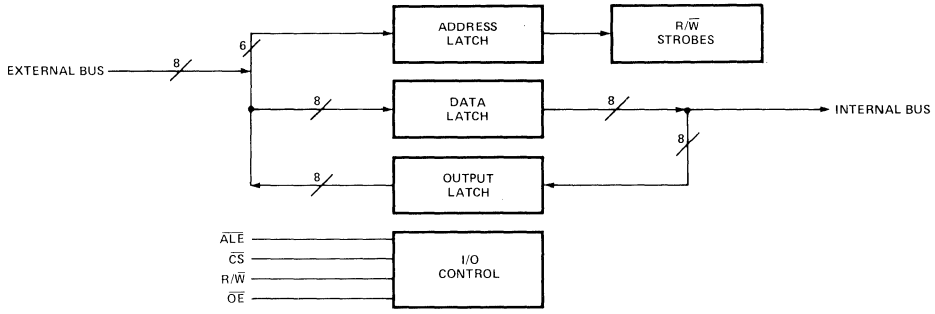


Figure 15. I/O Port Block Diagram.

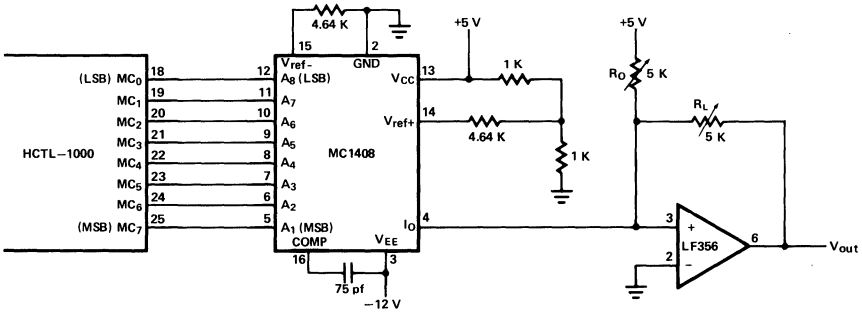


Figure 16. Linear Amplifier Interface.

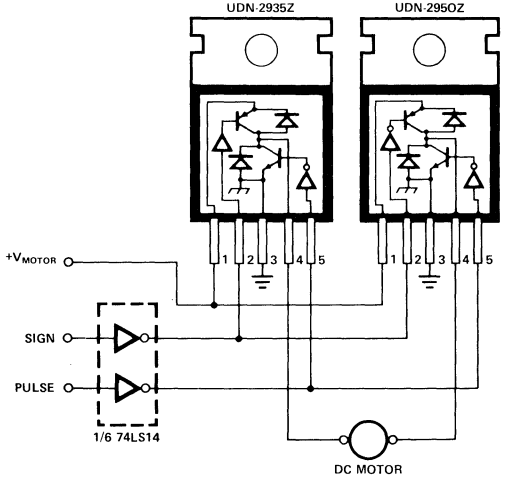


Figure 17. H-Bridge Amplifier Interface.

Additional Information From Hewlett-Packard

Additional information regarding the HCTL-1100 is available from the Hewlett-Packard Motion Control Factory. Please contact your local HP sales representative for more information.

1. Application Note 1032: "Design of the HCTL-1000's Digital Filter Parameters by the Combination Method"
2. Intel 8051 interface to the HCTL-1100
3. Zilog Z80 interface to the HCTL-1100
4. Motorola 6803-1 interface to the HCTL-1100
5. HCTL-1100 Sample Timer and Digital Filter (Seminar Slides)
6. DC Brush Motor Interfaces (Seminar Slides)
7. DC Brushless Motor Interfaces (Seminar Slides)
8. Step Motor Interfaces– including half-step mode (Seminar Slides)
9. List of Board Level Vendors using the HCTL-1000/ HCTL-1100. Many companies provide board level products using the HCTL-1000 and HCTL-1100 compatible with numerous busses.
10. HCTL-1000/HCTL-1100 Troubleshooting Guide. An answer guide to the most often asked questions about the operation of the HCTL-1000 and HCTL-1100.

Ordering Information

HCTL-1100: 40 Pin DIP Package
HCTL-1100#PLC: 44 Pin PLCC Package

HEWLETT PACKARD

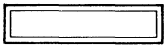
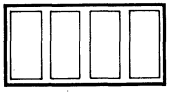
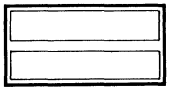
Light Bars and Bar Graph Arrays

Light Bars and Arrays

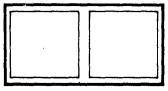
LED Light Bars are Hewlett-Packard's innovative solution to fixed message annunciation. The large, uniformly illuminated light emitting surface may be used for backlighting legends or simple indicators. Four distinct colors are offered: AlGaAs red, high efficiency red, yellow, and high performance green with two bicolor combinations. The AlGaAs Red Light Bars provide exceptional brightness at very low drive currents for those applications where portability and battery backup are important considerations. Each of the eight X-Y stackable package styles offers one, two, or four light emitting surfaces. Along with this family of stackable light bars, HP also provides a single chip light bar for high brightness indication of small areas. Panel Mounts are also available for all devices.

In addition to light bars, HP offers effective analog message annunciation with the 10-element LED Bar Graph Arrays. These bar graph arrays eliminate the matching and alignment problems commonly associated with arrays of discrete LED indicators. Each device offers easy to handle packages that are compatible with standard DIP sockets. The 10-element Bar Graph Array is available in standard red, AlGaAs red, high efficiency red, yellow, and high performance green. The multicolor 10-element arrays have high efficiency red, yellow, and green LEDs in one package. The package is X-Y stackable, with a unique interlock allowing easy end-to-end alignment.

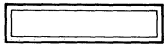
LED Light Bars

Device		Description			Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLMP-2300	High Efficiency Red	4 Pin In-Line; 0.100" Centers; 0.400"L x 0.195"W x 0.245"H	Diffused	23 mcd	2.0 V	2-8
	HLMP-2400	Yellow		Diffused	20 mcd	2.1 V	
	HLMP-2500	Green		Green Diffused	25 mcd	2.2 V	
	HLMP-2350	High Efficiency Red	8 Pin In-Line; 0.100" Centers; 0.800"L x 0.195"W x 0.245"H	Diffused	45 mcd	2.0 V	
	HLMP-2450	Yellow		Diffused	38 mcd	2.1 V	
	HLMP-2550	Green		Green Diffused	50 mcd	2.2 V	
	HLMP-2600	High Efficiency Red	8 Pin DIP; 0.100" Centers; 0.400"L x 0.400"W x 0.245"H Dual Arrangement	Diffused	22 mcd	2.0 V	
	HLMP-2700	Yellow		Diffused	18 mcd	2.1 V	
	HLMP-2800	Green		Green Diffused	25 mcd	2.2 V	
	HLMP-2620	High Efficiency Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Quad Arrangement	Diffused	25 mcd	2.0 V	
	HLMP-2720	Yellow		Diffused	18 mcd	2.1 V	
	HLMP-2820	Green		Green Diffused	25 mcd	2.2 V	
	HLMP-2635	High Efficiency Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Dual Bar Arrangement	Diffused	45 mcd	2.0 V	
	HLMP-2735	Yellow		Diffused	35 mcd	2.1 V	
	HLMP-2835	Green		Green Diffused	50 mcd	2.2 V	

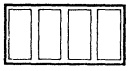
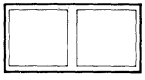
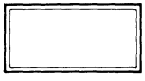
LED Light Bars (Continued)

Device		Description			Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLMP-2655	High Efficiency Red	8 Pin DIP; 0.100" Centers; 0.400"L x 0.400"W x 0.245"H Square Arrangement	Diffused	43 mcd	2.0 V	2-8
	HLMP-2755	Yellow		Diffused	35 mcd	2.1 V	
	HLMP-2855	Green		Green Diffused	50 mcd	2.2 V	
	HLMP-2670	High Efficiency Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Dual Square Arrangement	Diffused	45 mcd	2.0 V	
	HLMP-2770	Yellow		Diffused	35 mcd	2.1 V	
	HLMP-2870	Green		Green Diffused	50 mcd	2.2 V	
	HLMP-2685	High Efficiency Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Single Bar Arrangement	Diffused	80 mcd	2.0 V	
	HLMP-2785	Yellow		Diffused	70 mcd	2.1 V	
	HLMP-2885	Green		Green Diffused	100 mcd	2.2 V	

DH AlGaAs Low Current LED Light Bars

Device		Description			Typical Luminous Intensity @ 3 mA	Typical Forward Voltage @ 3mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLCP-A100	AlGaAs Red	4 Pin In-Line; 0.100" Centers; 0.400"L x 0.195"W x 0.245"H	Diffused	7.5 mcd	1.6 V	2-8
	HLCP-B100	AlGaAs Red	8 Pin In-Line; 0.100" Centers; 0.800"L x 0.195"W x 0.245"H	Diffused	15.0 mcd		

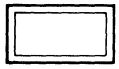
DH AlGaAs Low Current LED Light Bars (Continued)

Device		Description			Typical Luminous Intensity	Typical Forward Voltage	Page
Package Outline Drawing	Part No.	Color	Package	Lens	@ 3 mA	@ 3 mA	No.
	HLCP-D100	AlGaAs Red	8 Pin DIP; 0.100" Centers; 0.400"L x 0.400"W x 0.245"H Dual Arrangement	Diffused	7.5 mcd	1.6 V	2-8
	HLCP-E100	AlGaAs Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Quad Arrangement	Diffused	7.5 mcd		
	HLCP-F100	AlGaAs Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Dual Bar Arrangement	Diffused	15.0 mcd		
	HLCP-C100	AlGaAs Red	8 pin DIP; 0.100" Centers; 0.400"L x 0.400"W x 0.245"H Square Arrangement	Diffused	15.0 mcd		
	HLCP-G100	AlGaAs Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Dual Square Arrangement	Diffused	15.0 mcd		
	HLCP-H100	AlGaAs Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Single Bar Arrangement	Diffused	30.0 mcd		

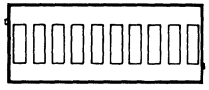
LED Bicolor Light Bars

Device		Description			Typical Luminous Intensity	Typical Forward Voltage	Page
Package Outline Drawing	Part No.	Color	Package	Lens	@ 20 mA	@ 20 mA	No.
	HLMP-2950	High Efficiency Red/ Yellow	8 Pin DIP; 0.100" Centers; 0.400"L x 0.400"W x 0.245"H Square Arrangement	Diffused	HER: 20 mcd Yellow: 12 mcd	HER: 2.0 V Yellow: 2.1 V	2-8
	HLMP-2965	High Efficiency Red/ Green		Diffused	HER: 20 mcd Green: 20 mcd	HER: 2.0 V Green: 2.2 V	

Single Chip LED Light Bar

Device		Description			Tylcal Luminous Intensity @ 20 mA	2θ 1/2	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-T200	High Efficiency Red (626 nm)	One Chip LED Light Bar	Tinted Diffused	4.8 mcd	100°	2.2 V	2-19
	HLMP-T300	Yellow (585 nm)			6.0 mcd		2.2 V	
	HLMP-T400	Orange (608 nm)			4.8 mcd		2.2 V	
	HLMP-T500	Green (569 nm)			6.0 mcd		2.3 V	

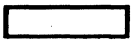
LED Bar Graph Arrays

Device		Description			Typical Luminous Intensity	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HDSP-4820	Standard Red	20 Pin DIP; 0.100" Centers;1.0"L x 0.400"W x 0.200"	Diffused	1250 µcd @ 20 mA DC	1.6 V @ 20 mA DC	2-23
	HDSP-4830	High Efficiency Red		Diffused	3500 µcd @ 10 mA DC	2.1 V @ 20 mA DC	
	HDSP-4840	Yellow		Diffused	1900 µcd @ 10 mA DC	2.2 V @ 20 mA DC	
	HDSP-4850	High Performance Green		Green Diffused	1900 µcd @ 10 mA DC	2.1 V @ 10 mA DC	
	HDSP-4832	Multicolor		Diffused	1900 µcd @ 10 mA DC		
	HDSP-4836	Multicolor		Diffused	1900 µcd @ 10 mA DC		
	HLCP-J100	AlGaAs Red		Diffused	1000 µcd @ 1 mA	1.6 V @ 1 mA	

LED Bar Graph 101-Element Array

Device		Description			Typical Luminous Intensity @	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HDSP-8820	Standard Red	22 Pin DIP; 0.100" Centers; 4.16" L x 0.390" W x 0.236" H	Red, Non-Diffused	20 µcd @ 100 mA Pk; 1 of 110 D.F.	1.7 V @ 100 mA Pk; 1 of 110 DF.	2-30
	HDSP-8825	High Efficiency Red		Clear	175 µcd @ 100 mA Pk; 1 of 110 D.F.	2.3 V @ 100 mA Pk; 1 of 110 DF.	
	HDSP-8835	High Efficiency Green		Clear	175 µcd @ 100 mA Pk; 1 of 110 D.F.	2.3 V @ 100 mA Pk; 1 of 110 DF.	

Panel Mounts for LED Light Bars

Device			Page No.
Package Outline Drawing	Part No.	Corresponding Light Bar Module Part Number	
	HLMP-2598	HLMP-2350, -2450, -2550, HLCP-B100	2-38
	HLMP-2599	HLMP-2300, -2400, -2500, HLCP-A100	
	HLMP-2898	HLMP-2600, -2700, -2800 -2655, -2755, -2855 -2950, -2965, HLCP-C100, -D100	
	HLMP-2899	HLMP-2620, -2720, -2820, -2635, -2735, -2835 -2670, -2770, -2870 -2685, -2785, -2885 HLCP-E100, -F100, -G100, -H100	

LED Light Bars Standard Options

Option Number	Description	Page Number
S02	Devices Selected to Two (2) Iv Categories	2-41
S22	Devices Selected to Two (2) Iv Categories and Two (2) Color Bin Categories	

HEWLETT PACKARD

LED Light Bars

Technical Data

HLCP-A100, -B100, -C100, -D100, -E100, -F100, -G100, -H100
HLMP-2300, -2350, -2400, -2450, -2500, -2550, -2600, -2620, -2635, -2655, -2670, -2685, -2700, -2720, -2735, -2755, -2770, -2785, -2800, -2820, -2835, -2855, -2870, -2885, -2950, -2965

Features

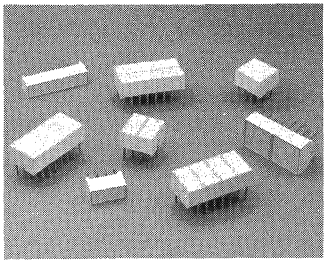
- **Large Bright, Uniform Light Emitting Areas**
- **Choice of Colors**
- **Categorized for Light Output**
- **Yellow and Green Categorized for Dominant Wavelength**
- **Excellent ON-OFF Contrast**
- **X-Y Stackable**
- **Flush Mountable**
- **Can be Used with Panel and Legend Mounts**
- **Light Emitting Surface Suitable for Legend Attachment per Application Note 1012**
- **HLCP-X100 Series Designed for Low Current Operation**
- **Bicolor Devices Available**

Applications

- **Business Machine Message Annunciators**
- **Telecommunications Indicators**
- **Front Panel Process Status Indicators**
- **PC Board Identifiers**
- **Bar Graphs**

Description

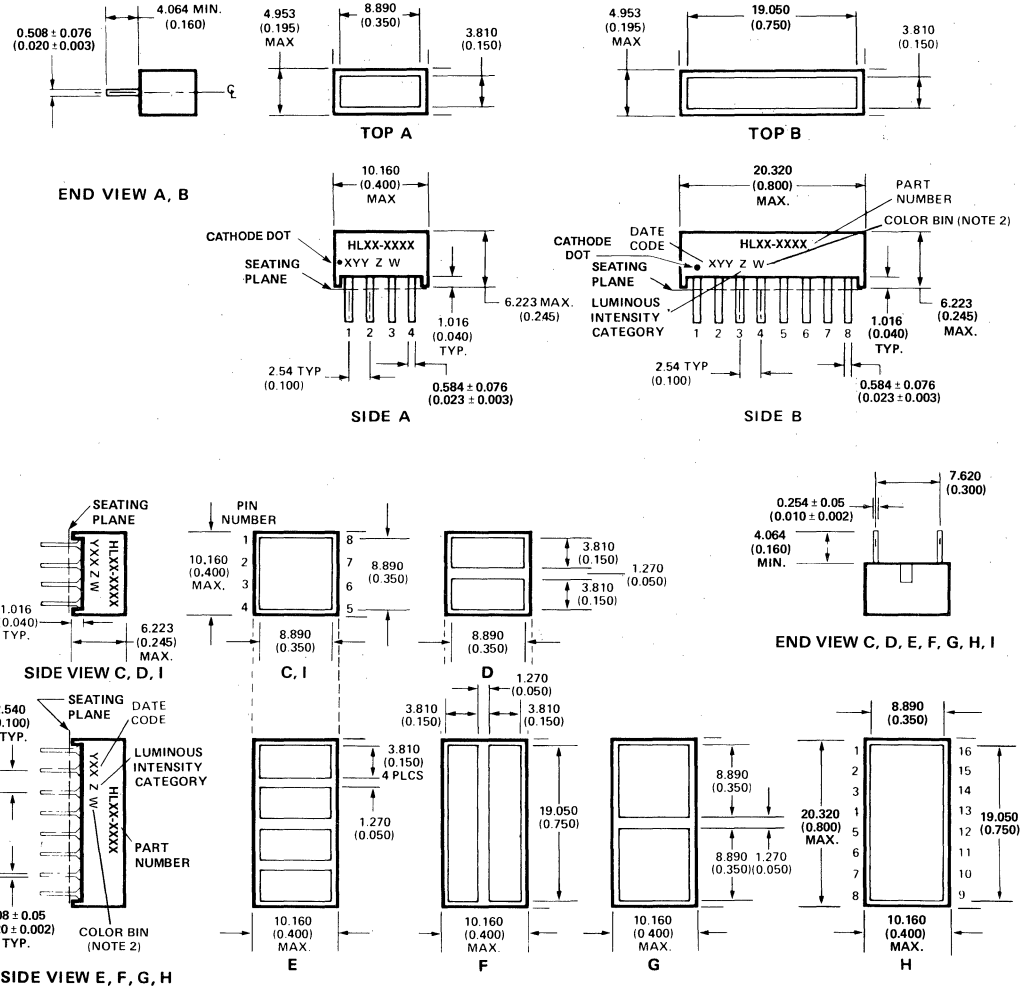
The HLCP-X100 and HLMP-2XXX series light bars are rectangular light sources designed for a variety of applications where a large bright source of light is required. These light bars are configured in single-in-line and dual-in-line packages that contain either single or segmented light emitting areas. The AlGaAs Red HLCP-X100 series LEDs use double heterojunction AlGaAs on a GaAs substrate. The HER HLMP-2300/2600 and Yellow HLMP-2400/2700 series LEDs have their p-n junctions diffused into a GaAsP epitaxial layer on a GaP substrate. The Green HLMP-2500/2800 series LEDs use a liquid phase GaP epitaxial layer on a GaP substrate. The bicolor HLMP-2900 series use a combination of HER/Yellow or HER/Green LEDs.



Selection Guide

Light Bar Part Number				Size of Light Emitting Areas	Number of Light Emitting Areas	Package Outline		Corresponding Panel and Legend Mount Part No. HLMP-
HLCP-	HLMP-							
AlGaAs	HER	Yellow	Green					
A100	2300	2400	2500	8.89 mm x 3.81 mm (.350 in. x .150 in.)	1	A		2599
B100	2350	2450	2550	19.05 mm x 3.81 mm (.750 in. x .150 in.)	1	B		2598
D100	2600	2700	2800	8.89 mm x 3.81 mm (.350 in. x .150 in.)	2	D		2898
E100	2620	2720	2820	8.89 mm x 3.81 mm (.350 in. x .150 in.)	4	E		2899
F100	2635	2735	2835	3.81 mm x 19.05 mm (.150 in. x .750 in.)	2	F		2899
C100	2655	2755	2855	8.89 mm x 8.89 mm (.350 in. x .350 in.)	1	C		2898
G100	2670	2770	2870	8.89 mm x 8.89 mm (.350 in. x .350 in.)	2	G		2899
H100	2685	2785	2885	8.89 mm x 19.05 mm (.350 in. x .750 in.)	1	H		2899
	2950	2950		8.89 mm x 8.89 mm (.350 in. x .350 in.)	Bicolor	I		2898
	2965		2965	8.89 mm x 8.89 mm (.350 in. x .350 in.)	Bicolor	I		2898

Package Dimensions

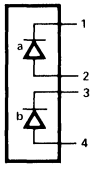


NOTES:

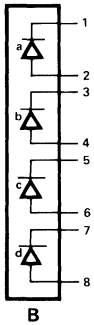
1. DIMENSIONS IN MILLIMETRES (INCHES). TOLERANCES ±0.25 mm (±0.010 IN.) UNLESS OTHERWISE INDICATED.

2. FOR YELLOW AND GREEN DEVICES ONLY.

Internal Circuit Diagrams

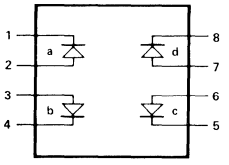


A

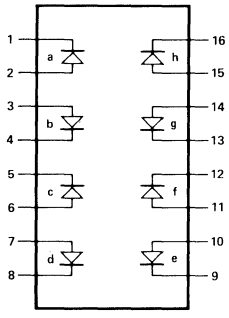


B

PIN	PIN FUNCTION A -2300/-2400 -2500/A100	PIN FUNCTION B -2350/-2450 -2550/B100
1	CATHODE a	CATHODE a
2	ANODE a	ANODE a
3	CATHODE b	CATHODE b
4	ANODE b	ANODE b
5		CATHODE c
6		ANODE c
7		CATHODE d
8		ANODE d

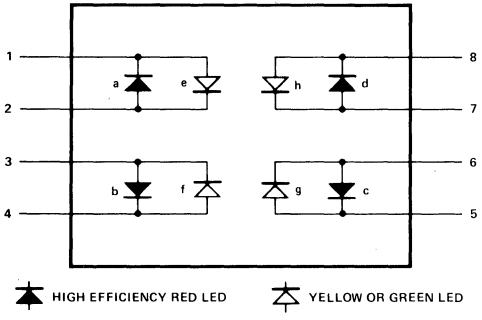


C,D



E,F,G,H

PIN	PIN FUNCTION C, D	PIN FUNCTION E, F, G, H
1	CATHODE a	CATHODE a
2	ANODE a	ANODE a
3	ANODE b	ANODE b
4	CATHODE b	CATHODE b
5	CATHODE c	CATHODE c
6	ANODE c	ANODE c
7	ANODE d	ANODE d
8	CATHODE d	CATHODE d
9		CATHODE e
10		ANODE e
11		ANODE f
12		CATHODE f
13		CATHODE g
14		ANODE g
15		ANODE h
16		CATHODE h



I

PIN	PIN FUNCTION HER	PIN FUNCTION YELLOW/ GREEN
1	CATHODE a	ANODE e
2	ANODE a	CATHODE e
3	ANODE b	CATHODE f
4	CATHODE b	ANODE f
5	CATHODE c	ANODE g
6	ANODE c	CATHODE g
7	ANODE d	CATHODE h
8	CATHODE d	ANODE h

Absolute Maximum Ratings

Parameter	AlGaAs Red HLCP-X100 Series	HER HLMP-2300/ 2600/29XX Series	Yellow HLMP-2400/ 2700/2950 Series	Green HLMP-2500/ 2800/2965 Series
Average Power Dissipated per LED chip	37 mW[1]	135 mW[2]	85 mW[3]	135 mW[2]
Peak Forward Current per LED chip	45 mA[4]	90 mA[5]	60 mA[5]	90 mA[5]
Average Forward Current per LED chip	15 mA	25 mA	20 mA	25 mA
DC Forward Current per LED chip	15 mA[1]	30 mA[2]	25 mA[3]	30 mA[2]
Reverse Voltage per LED chip	5 V	6 V[6]		
Operating Temperature Range	–20°C to +100°C[7]	–40°C to +85°C		–20°C to +85°C
Storage Temperature Range	–40°C to +85°C			
Lead Soldering Temperature 1.6 mm (1/16 inch) Below Seating Plane3	260°C for 3 seconds[8]			

Notes:
1. Derate above 87°C at 1.7 mW/°C per LED chip. For DC operation, derate above 91°C at 0.8 mA/°C.
2. Derate above 25°C at 1.8 mW/°C per LED chip. For DC operation, derate above 50°C at 0.5 mA/°C.
3. Derate above 50°C at 1.8 mW/°C per LED chip. For DC operation, derate above 60°C at 0.5 mA/°C.
4. See Figure 1 to establish pulsed operation. Maximum pulse width is 1.5 mS.
5. See Figure 6 to establish pulsed operation. Maximum pulse width is 2 mS.
6. Does not apply to bicolor parts.
7. For operation below –20°C, contact your local HP sales representative.
8. Maximum tolerable component side temperature is 134°C during solder process.

Electrical/Optical Characteristics at T_A = 25°C
AlGaAs Red HLCP-X100 Series

Parameter	HLCP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity per Lighting Emitting Area[1]	A100/D100/E100	I_V	3	7.5		mcd	I_F = 3 mA
	B100/C100/F100/G100		6	15		mcd	
	H100		12	30		mcd	
Peak Wavelength		λ_{PEAK}		645		nm	
Dominant Wavelength[2]		λ_d		637		nm	
Forward Voltage per LED		V_F		1.8	2.2	V	I_F = 20 mA
Reverse Breakdown Voltage per LED		V_R	5	15		V	I_R = 100 µA
Thermal Resistance LED Junction-to-Pin		$R\theta_{J\text{-}PIN}$		250		°C/W/ LED	

High Efficiency Red HLMP-2300/2600/2900 Series

Parameter	HLMP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity per Lighting Emitting Area[1]	2300/2600/2620	I_V	6	23		mcd	I_F = 20 mA
	2350/2635/2655/2670/2950[3]		13	45		mcd	
	2965[4]		19	45		mcd	
	2685		22	80		mcd	
Peak Wavelength		λ_{PEAK}		635		nm	
Dominant Wavelength[2]		λ_d		626		nm	
Forward Voltage per LED		V_F		2.0	2.6	V	I_F = 20 mA
Reverse Breakdown Voltage per LED[5]		V_R	6	15		V	I_R = 100 µA
Thermal Resistance LED Junction-to-Pin		$R\theta_{J\text{-}PIN}$		150		°C/W/ LED	

Yellow HLMP-2400/2700/2950 Series

Parameter	HLMP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity per Lighting Emitting Area[1]	2400/2700/2720	I_V	6	20		mcd	I_F = 20 mA
	2450/2735/2755/2770/2950[3]		13	38		mcd	
	2785		26	70		mcd	
Peak Wavelength		λ_{PEAK}		583		nm	
Dominant Wavelength[2]		λ_d		585		nm	
Forward Voltage per LED		V_F		2.1	2.6	V	I_F = 20 mA
Reverse Breakdown Voltage per LED[5]		V_R	6	15		V	I_R = 100 µA
Thermal Resistance LED Junction-to-Pin		$R\theta_{J\text{-}PIN}$		150		°C/W/ LED	

High Performance Green HLMP-2500/2800/2965 Series

Parameter	HLMP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity per Lighting Emitting Area[1]	2500/2800/2820	I_V	5	25		mcd	I_F = 20 mA
	2550/2835/2855/2870		11	50		mcd	
	2965[4]		25	50		mcd	
	2885		22	100		mcd	
Peak Wavelength		λ_{PEAK}		565		nm	
Dominant Wavelength[2]		λ_d		572		nm	
Forward Voltage per LED		V_F		2.2	2.6	V	I_F = 20 mA
Reverse Breakdown Voltage per LED[5]		V_R	6	15		V	I_R = 100 μA
Thermal Resistance LED Junction-to-Pin		$R\theta_{J\text{-}PIN}$		150		°C/W/ LED	

Notes:

1. These devices are categorized for luminous intensity. The intensity category is designated by a letter code on the side of the package.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is the single wavelength which defines the color of the device. Yellow and Green devices are categorized for dominant wavelength with the color bin designated by a number code on the side of the package.
3. This is an HER/Yellow bicolor light bar. HER electrical/optical characteristics are shown in the HER table. Yellow electrical/ optical characteristics are shown in the Yellow table.
4. This is an HER/Green bicolor light bar. HER electrical/optical characteristics are shown in the HER table. Green electrical/ optical characteristics are shown in the Green table.
5. Does not apply to HLMP-2950 or HLMP-2965.

AlGaAs Red

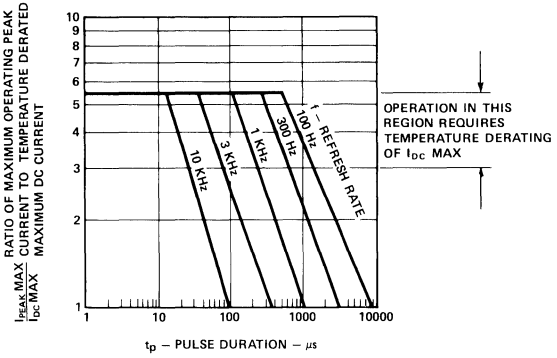


Figure 1. Maximum Allowable Peak Current vs. Pulse Duration

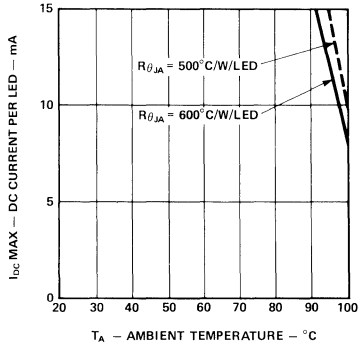


Figure 2. Maximum Allowed DC Current per LED vs. Ambient Temperature, T_JMAX = 110°C

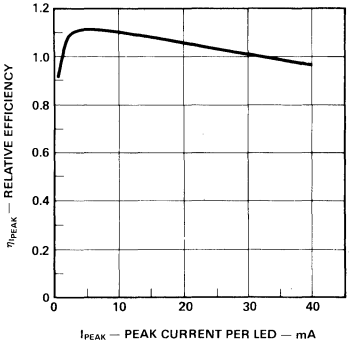


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current

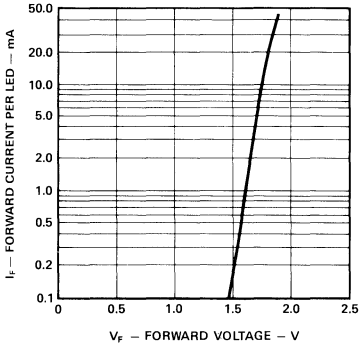


Figure 4. Forward Current vs. Forward Voltage

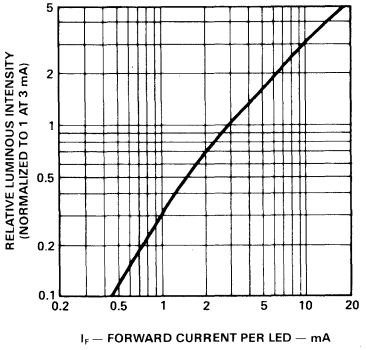


Figure 5. Relative Luminous Intensity vs. DC Forward Current

HER, Yellow, Green

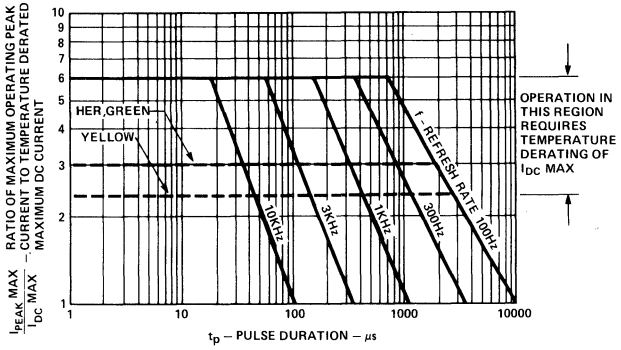


Figure 6. Maximum Allowed Peak Current vs. Pulse Duration

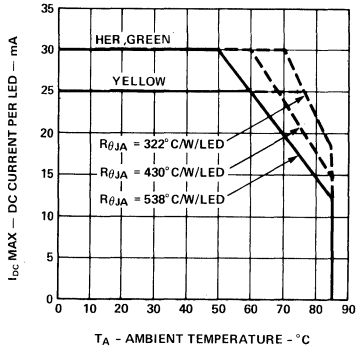


Figure 7. Maximum Allowable DC Current per LED vs. Ambient Temperature, T_J MAX = 100°C

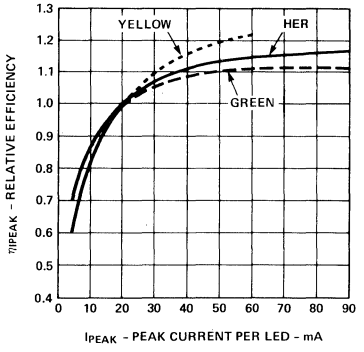


Figure 8. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak PED Current

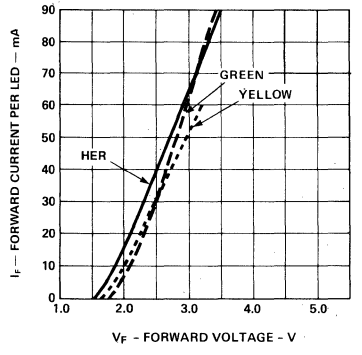


Figure 9. Forward Current vs. Forward Voltage Characteristics

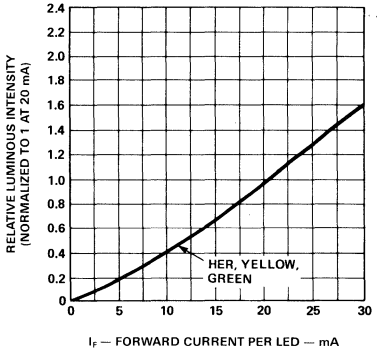


Figure 10. Relative Luminous Intensity vs. DC Forward Current

For a detailed explanation on the use of data sheet information and recommended soldering procedures, see Application Notes 1005, 1027, and 1031.

Electrical

These light bars are composed of two, four, or eight light emitting diodes, with the light from each LED optically scattered to form an evenly illuminated light emitting surface.

The anode and cathode of each LED is brought out by separate pins. This universal pinout arrangement allows the LEDs to be connected in three possible configurations: parallel, series, or series parallel. The typical forward voltage values can be scaled from Figures 4 and 9. These values should be used to calculate the current limiting resistor value and typical power consumption. Expected maximum V_F values for driver circuit design and maximum power dissipation, may be calculated using the following V_FMAX models:

AlGaAs Red HLCP-X100 series

$V_F MAX = 1.8\ V + I_{Peak}\ (20\Omega)$
For: $I_{Peak} \leq 20$ mA
$V_F MAX = 2.0\ V + I_{Peak}\ (10\Omega)$
For: 20 mA $\leq I_{Peak} \leq$ 45 mA

HER (HLMP-2300/2600/2900), Yellow (HLMP-2400/2700/2900) and Green (HLMP-2500/2800/2900) series

$V_F MAX = 1.6 + I_{Peak}\ (50\Omega)$
For: 5 mA $\leq I_{Peak} \leq$ 20 mA
$V_F MAX = 1.8 + I_{Peak}\ (40\Omega)$
For: $I_{Peak} \geq$ 20 mA

The maximum power dissipation can be calculated for any pulsed or DC drive condition. For DC operation, the maximum power dissipation is the product of the maximum forward voltage and the maximum forward current. For pulsed operation, the maximum power dissipation is the product of the maximum forward voltage at the peak forward current times the maximum average forward current. Maximum allowable power dissipation for any given ambient temperature and thermal resistance ($R\theta_{J\text{-}A}$) can be determined by using Figure 2 or 7. The solid line in Figure 2 or 7 ($R\theta_{J\text{-}A}$ of 600/538 C/W) represents a typical thermal resistance of a device socketed in a printed circuit board. The dashed lines represent achievable thermal resistances that can be obtained through improved thermal design. Once the maximum allowable power dissipation is determined, the maximum pulsed or DC forward current can be calculated.

Optical

Size of Light Emitting Area	Surface Area	
	Sq. Metres	Sq. Feet
8.89 mm x 8.89 mm	67.74×10^{-6}	729.16×10^{-6}
8.89 mm x 3.81 mm	33.87×10^{-6}	364.58×10^{-6}
8.89 mm x 19.05 mm	135.48×10^{-6}	1458.32×10^{-6}
3.81 mm x 19.05 mm	72.85×10^{-6}	781.25×10^{-6}

The radiation pattern for these light bar devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas:

$$L_v\ (cd/m^2) = \frac{I_v\ (cd)}{A\ (m^2)}$$

$$L_v\ (footlamberts) = \frac{\pi I_v\ (cd)}{A\ (ft^2)}$$

Refresh rates of 1 kHz or faster provide the most efficient operation resulting in the maximum possible time average luminous intensity.

The time average luminous intensity may be calculated using the relative efficiency characteristic of Figure 3 or 8, ηI_{PEAK}, and adjusted for operating ambient temperature. The time average luminous intensity at $T_A = 25°C$ is calculated as follows:

$$I_{v\ TIME\ AVG} = \left[\frac{I_{AVG}}{I_{TEST}}\right](\eta I_{PEAK})\ (I_v\ Data\ Sheet)$$

where:

I_{TEST} = 3 mA for AlGaAs Red (HLMP-X000 series)
20 mA for HER, Yellow and Green (HLMP-2XXX series)

Example:
For HLMP-2735 series

$\eta I_{PEAK} = 1.18$ at $I_{PEAK} = 48$ mA

$$I_{v\ TIME\ AVG} = \left[\frac{12\ mA}{20\ mA}\right](1.18)\ (35\ mcd)$$
$$= 25\ mcd$$

The time average luminous intensity may be adjusted for operating ambient temperature by the following exponential equation:

$$I_v(T_A) = I_v(25°C)e^{[K(T_A - 25°C)]}$$

Color	K
AlGaAs Red	–0.0095/°C
HER	–0.0131/°C
Yellow	–0.0112/°C
Green	–0.0104/°C

Example:

$I_v(80°C) = (25\ mcd)e^{[-0.0112(80-25)]}$
$= 14\ mcd.$

Mechanical

These light bar devices may be operated in ambient temperatures above +60°C without derating when installed in a PC board configuration that provides a thermal resistance pin to ambient value less than 280°C/W/LED. See Figure 2 or 7 to determine the maximum allowed thermal resistance for the PC board, $R\theta_{PC\text{-}A}$, which will permit nonderated operation in a given ambient temperature.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DES, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

For further information on soldering LEDs please refer to Application Note 1027.

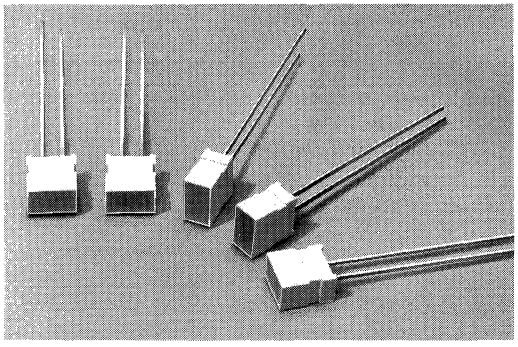
HEWLETT PACKARD

SINGLE CHIP LED LIGHT BAR

HIGH EFFICIENCY RED HLMP-T200 SERIES
YELLOW HLMP-T300 SERIES
ORANGE HLMP-T400 SERIES
HIGH PERFORMANCE GREEN HLMP-T500 SERIES

Features

- **FLAT RECTANGULAR LIGHT EMITTING SURFACE**
- **CHOICE OF 4 BRIGHT COLORS**
- **EXCELLENT ON/OFF CONTRAST**
- **IDEAL AS FLUSH MOUNTED PANEL INDICATORS**
- **LONG LIFE: SOLID STATE RELIABILITY**
- **SOLDER COATED LEADS**



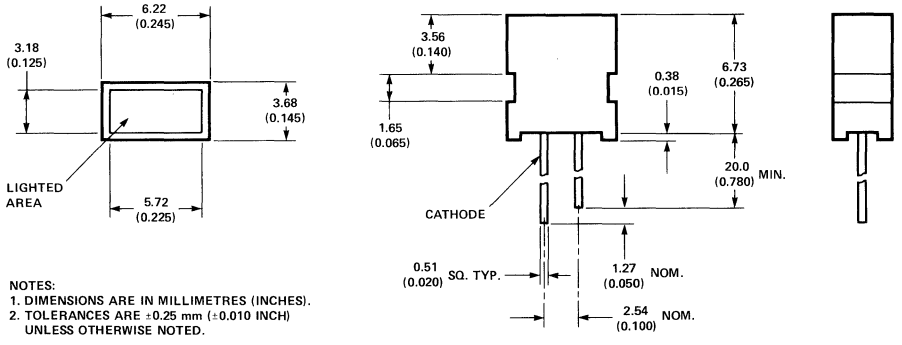
Description

The HLMP-T200/-T300/-T400/-T500 light bars are rectangular light sources designed for a variety of applications where this shape and a high sterance are desired. These light bars consist of a rectangular plastic case around an epoxy encapsulated LED lamp. The encapsulant is tinted to match the color of the emitted light. The flat top surface is exceptionally uniform in light emission and the plastic case eliminates light leakage from the sides of the device.

Applications

- **BAR GRAPHS**
- **FRONT PANEL STATUS INDICATORS**
- **TELECOMMUNICATIONS INDICATORS**
- **PUSH BUTTON ILLUMINATION**
- **PC BOARD IDENTIFIERS**
- **BUSINESS MACHINE MESSAGE ANNUNCIATORS**

Package Dimensions



NOTES:
1. DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. TOLERANCES ARE ±0.25 mm (±0.010 INCH) UNLESS OTHERWISE NOTED.

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	High Efficiency Red T200	3.0	4.8		mcd	I_F = 20 mA
		Orange T400	3.0	4.8			
		Yellow T300	3.0	4.8			
		Green T500	3.0	6.0			
$2\Theta 1/2$	Included Angle Between Half Luminous Intensity Points	All		100		Deg.	I_F = 20 mA See Note 1
λ_{PEAK}	Peak Wavelength	High Efficiency Red Orange Yellow Green		635 612 583 565		nm	Measurement at Peak
λ_d	Dominant Wavelength	High Efficiency Red Orange Yellow Green		626 608 585 569		nm	See Note 2
τ_S	Speed of Response	High Efficiency Red Orange Yellow Green		350 350 390 870		ns	
C	Capacitance	High Efficiency Red Orange Yellow Green		4 4 8 11		pF	V_F = 0; f = 1 MHz
$R\theta_{JC}$	Thermal Resistance	All		120		°C/W	Junction to Cathode Lead at Seating Plane
V_F	Forward Voltage	HER/Orange Yellow Green	1.5 1.5 1.6	2.2 2.2 2.3	2.6 2.6 2.6	V	I_F = 20 mA
V_R	Reverse Breakdown Volt.	All	5.0			V	I_R = 100 μA
η_V	Luminous Efficacy	High Efficiency Red Orange Yellow Green		145 262 500 595		$\frac{\text{lumens}}{\text{Watt}}$	See Note 3

Notes:
1. $\Theta 1/2$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Characteristics at $T_A = 25°C$

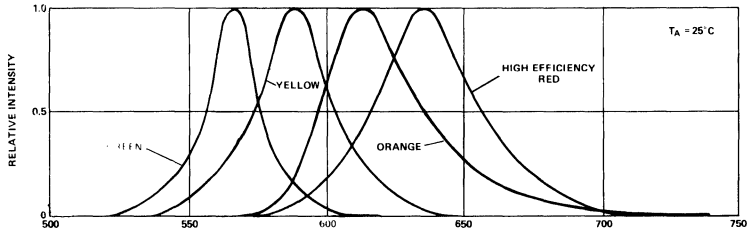


Figure 1. Relative Intensity vs. Wavelength.

High Efficiency Red, Orange, Yellow, and Green Light Bars

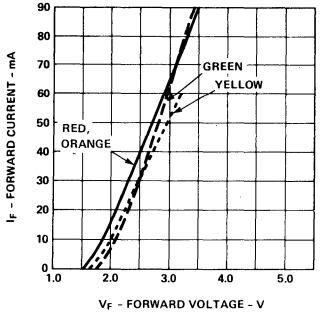


Figure 2. Forward Current vs. Forward Voltage Characteristics.

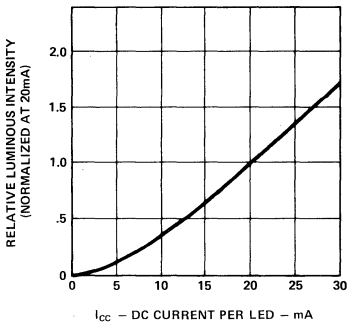


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

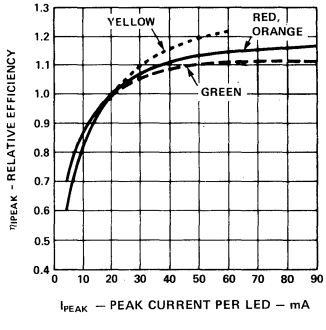


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. LED Peak Current.

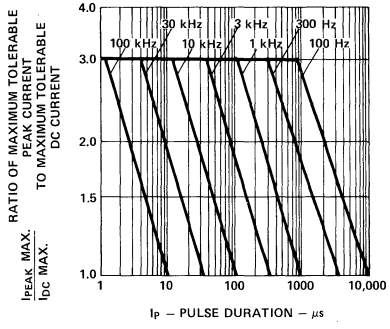


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

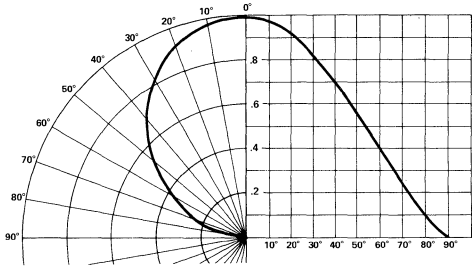


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	High Efficiency Red/ Orange	Yellow	Green	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Operating Temperature Range	-40 to +85	-40 to +85	-20 to +85	°C
Storage Temperature Range	-55 to +100	-55 to +100	-55 to +100	
Reverse Voltage (I_R = 100 μA)	5			V
Transient Forward Current[4] (10 μsec Pulse)	500			mA
Lead Soldering Temperature [1.6 mm (0.063 in.) below seating plane]	260° C for 3 seconds			

Notes:
1. See Figure 5 to establish pulsed operating conditions.
2. For Red, Orange, and Green derate linearly from 50° C at 0.5 mA/° C. For Yellow derate linearly from 50° C at 0.34 mA/° C.
3. For Red, Orange, and Green derate power linearly from 25° C at 1.6 mW/° C. For Yellow derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

Electrical

The typical forward voltage values, scaled from Figure 2, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design and maximum power dissipation may be calculated using the following V_F models:

$$V_F = 1.8V + I_{PEAK}(40\Omega)$$
For $I_{PEAK} \geq 20$ mA

$$V_F = 1.6V + I_{DC}(50\Omega)$$
For 5 mA $\leq I_{DC} \leq$ 20 mA

Optical

The radiation pattern for these light bar devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas:

$$L_V\ (cd/m^2) = \frac{I_V\ (cd)}{A\ (m^2)}$$

$$L_V\ (footlamberts) = \frac{\pi I_V\ (cd)}{A\ (ft^2)}$$

Size of light emitting area (A)= 3.18 mm x 5.72 mm
$= 18.19 \times 10^{-6}\ m^2$
$= 195.8 \times 10^{-6}\ ft^2$

Mechanical

These light bar devices may be operated in ambient temperatures above +50° C without derating when installed in a PC board configuration that provides a thermal resistance (junction to ambient) value less than 625° C/W.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60° C (140° F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

10-Element Bar Graph Array

Technical Data

HLCP-J100
HDSP-4820
HDSP-4830
HDSP-4832
HDSP-4836
HDSP-4840
HDSP-4850

Features

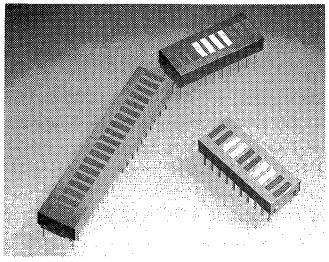
- **Custom Multicolor Array Capability**
- **Matched LEDs for Uniform Appearance**
- **End Stackable**
- **Package Interlock Ensures Correct Alignment**
- **Low Profile Package**
- **Rugged Construction**
- **Large, Easily Recognizable Segments**
- **High ON-OFF Contrast, Segment to Segment**
- **Wide Viewing Angle**
- **Categorized for Luminous Intensity**
- **HDSP-4832/4836/4840/4850 Categorized for Dominant Wavelength**
- **HLCP-J100 Operates at Low Current**
  Typical Intensity of 1.0 mcd at 1 mA Drive Current

Applications

- **Industrial Controls**
- **Instrumentation**
- **Office Equipment**
- **Computer Peripherals**
- **Consumer Products**

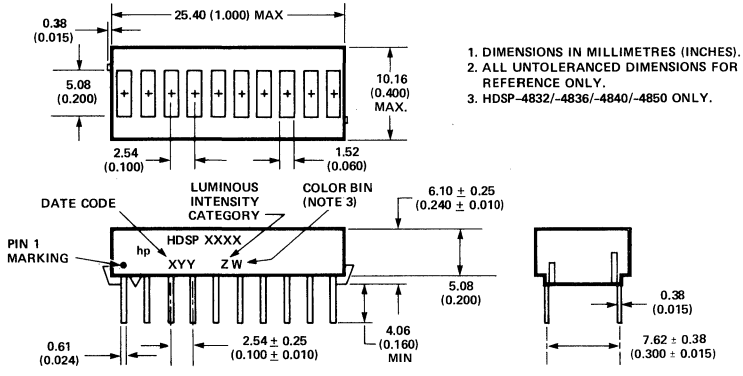
Description

These 10-element LED arrays are designed to display information in easily recognizable bar graph form. The packages are end stackable and therefore capable of displaying long strings of information. Use of these bar graph arrays eliminates the alignment, intensity, and color matching problems associated with discrete LEDs. The HDSP-4820/4830/4840/4850 and HLCP-J100 each contain LEDs of one color. The HDSP-4832/4836 are multicolor arrays with High Efficiency Red, Yellow, and High Performance Green LEDs in a single package.



CUSTOM MULTICOLOR ARRAYS ARE AVAILABLE WITH MINIMUM DELIVERY REQUIREMENTS. CONTACT YOUR LOCAL DISTRIBUTOR OR HP SALES OFFICE FOR DETAILS.

Package Dimensions



1. DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS FOR REFERENCE ONLY.
3. HDSP-4832/-4836/-4840/-4850 ONLY.

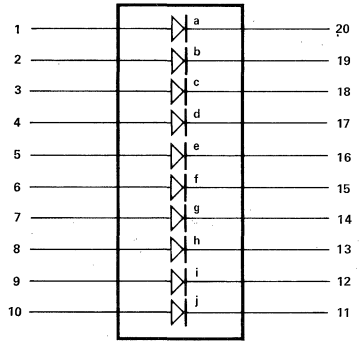
Absolute Maximum Ratings[7]

Parameter	Red HDSP-4820	AlGaAs Red HLCP-J100	HER HDSP-4830	Yellow HDSP-4840	Green HDSP-4850
Average Power Dissipation per LED (T_A = 25°C)	63 mW	37 mW	87 mW	50 mW	105 mW
Peak Forward Current per LED	150 mA[1]	45 mA[2]	90 mA[3]	60 mA[3]	90 mA[3]
DC Forward Current per LED	30 mA[4]	15 mA[4]	30 mA[5]	20 mA[5]	30 mA[5]
Operating Temperature Range	–40°C to +85°C	–20°C to +100°C	–40°C to +85°C		–20°C to +85°C
Storage Temperature Range	–40°C to +85°C	–55°C to +100°C	–40°C to +85°C		
Reverse Voltage per LED	3.0 V	5.0 V	3.0 V		
Lead Soldering Temperature (1.59 mm (1/16 inch) below seating plane)[6]	260°C for 3 seconds[8]				

Notes:

1. See Figure 1 to establish pulsed operating conditions. Maximum pulse width is 1.5 ms.
2. See Figure 2 to establish pulsed operating conditions. Maximum pulse width is 1.5 ms.
3. See Figure 8 to establish pulsed operating conditions. Maximum pulse width is 2 ms.
4. Derate maximum DC current for Red above T_A = 62°C at 0.79 mA/°C, and AlGaAs Red above T_A = 91°C at 0.8 mA°C. See Figure 3.
5. Derate maximum DC current for HER above T_A = 48°C at 0.58 mA/°C, Yellow above T_A = 70°C at 0.66 mA/°C, and Green above T_A = 37°C at 0.48 mA/°C. See Figure 9.
6. Clean only in water, isopropanol, ethanol, Freon TF or TE (or equivalent), or Genesolve DI-15 (or equivalent).
7. Absolute maximum ratings for HER, Yellow, and Green elements of the multicolor arrays are identical to the HDSP-4830/4840/4850 maximum ratings.
8. Maximum tolerable component side temperature is 134°C during solder process.

Internal Circuit Diagram



Pin	Function	Pin	Function
1	Anode a	11	Cathode j
2	Anode b	12	Cathode i
3	Anode c	13	Cathode h
4	Anode d	14	Cathode g
5	Anode e	15	Cathode f
6	Anode f	16	Cathode e
7	Anode g	17	Cathode d
8	Anode h	18	Cathode c
9	Anode i	19	Cathode b
10	Anode j	20	Cathode a

Multicolor Array Segment Colors

Segment	HDSP-4832 Segment Color	HDSP-4836 Segment Color
a	HER	HER
b	HER	HER
c	HER	Yellow
d	Yellow	Yellow
e	Yellow	Green
f	Yellow	Green
g	Yellow	Yellow
h	Green	Yellow
i	Green	HER
j	Green	HER

Electrical/Optical Characteristics at $T_A = 25°C$[4]

Red HDSP-4820

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity per LED (Unit Average)[1]	I_V	610	1250		µcd	I_F = 20 mA
Peak Wavelength	λ_{PEAK}		655		nm	
Dominant Wavelength[2]	λ_d		645		nm	
Forward Voltage per LED	V_F		1.6	2.0	V	I_F = 20 mA
Reverse Voltage per LED[5]	V_R	3	12		V	I_R = 100 µA
Temperature Coefficient V_F per LED	ΔV_F / °C		–2.0		mV/°C	
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		300		°C/W/LED	

AlGaAs Red HLCP-J100

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity per LED (Unit Average)[1]	I_V	600	1000		µcd	I_F = 1 mA
			5200			I_F = 20 mA Pk; 1 of 4 Duty Factor
Peak Wavelength	λ_{PEAK}		645		nm	
Dominant Wavelength[2]	λ_d		637		nm	
Forward Voltage per LED	V_F		1.6		V	I_F = 1 mA
			1.8	2.2		I_F = 20 mA
Reverse Voltage per LED[5]	V_R	5	15		V	I_R = 100 µA
Temperature Coefficient V_F per LED	ΔV_F / °C		–2.0		mV/°C	
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		300		°C/W/LED	

High Efficiency Red HDSP-4830

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity per LED (Unit Average)[1,4]	I_V	900	3500		µcd	I_F = 10 mA
Peak Wavelength	λ_{PEAK}		635		nm	
Dominant Wavelength[2]	λ_d		626		nm	
Forward Voltage per LED	V_F		2.1	2.5	V	I_F = 20 mA
Reverse Voltage per LED[5]	V_R	3	30		V	I_R = 100 µA
Temperature Coefficient V_F per LED	ΔV_F/°C		–2.0		mV/°C	
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		300		°C/W/LED	

Yellow HDSP-4840

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity per LED (Unit Average)[1,4]	I_V	600	1900		µcd	I_F = 10 mA
Peak Wavelength	λ_{PEAK}		583		nm	
Dominant Wavelength[2,3]	λ_d	581	585	592	nm	
Forward Voltage per LED	V_F		2.2	2.5	V	I_F = 20 mA
Reverse Voltage per LED[5]	V_R	3	40		V	I_R = 100 µA
Temperature Coefficient V_F per LED	ΔV_F/°C		–2.0		mV/°C	
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		300		°C/W/LED	

Green HDSP-4850

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity per LED (Unit Average)[1,4]	I_V	600	1900		µcd	I_F = 10 mA
Peak Wavelength	λ_{PEAK}		566		nm	
Dominant Wavelength[2,3]	λ_d		571	577	nm	
Forward Voltage per LED	V_F		2.1	2.5	V	I_F = 10 mA
Reverse Voltage per LED[5]	V_R	3	50		V	I_R = 100 µA
Temperature Coefficient V_F per LED	ΔV_F /°C		–2.0		mV/°C	
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		300		°C/W/LED	

Notes:

1. The bar graph arrays are categorized for luminous intensity. The category is designated by a letter located on the side of the package.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
3. The HDSP-4832/-4836/-4840/-4850 bar graph arrays are categorized by dominant wavelength with the category designated by a number adjacent to the intensity category letter. Only the yellow elements of the HDSP-4832/-4836 are categorized for color.
4. Electrical/optical characteristics of the High-Efficiency Red elements of the HDSP-4832/-4836 are identical to the HDSP-4830 characteristics. Characteristics of Yellow elements of the HDSP-4832/-4836 are identical to the HDSP-4840. Characteristics of Green elements of the HDSP-4832/-4836 are identical to the HDSP-4850.
5. Reverse voltage per LED should be limited to 3.0 V max. for the HDSP-4820/4830/4840/4850/4832/4836 and 5.0 V max. for the HLCP-J100.

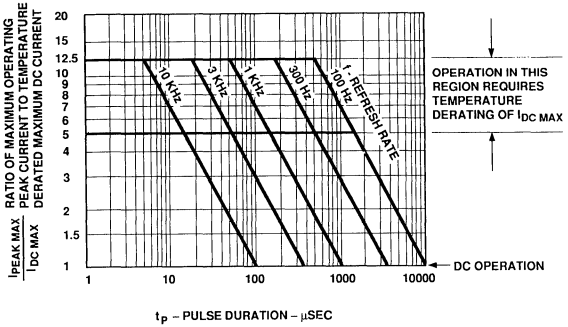


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration – Red.

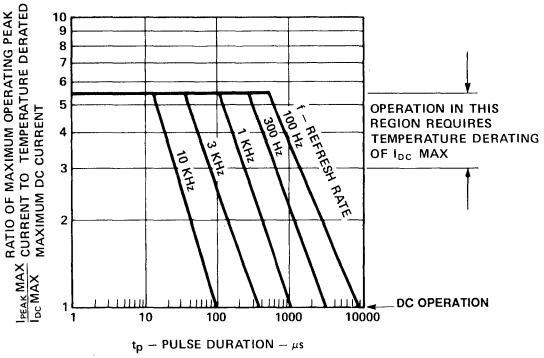


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration – AlGaAs Red.

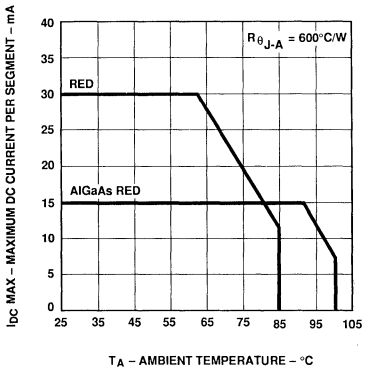


Figure 3. Maximum Allowable DC Current vs. Ambient Temperature. T_{JMAX} = 100°C for Red and T_{JMAX} = 110°C for AlGaAs Red.

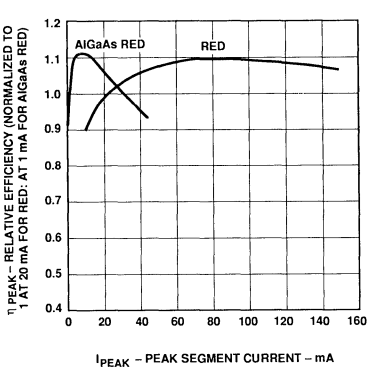


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

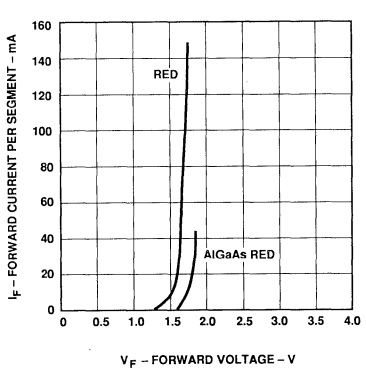


Figure 5. Forward Current vs. Forward Voltage.

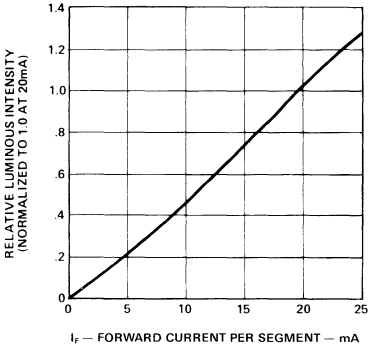


Figure 6. Relative Luminous Intensity vs. DC Forward Current – Red.

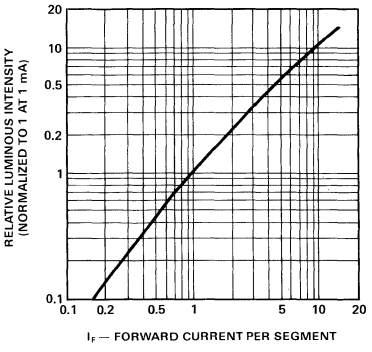


Figure 7. Relative Luminous Intensity vs. DC Forward Current – AlGaAs.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

HER, Yellow, Green

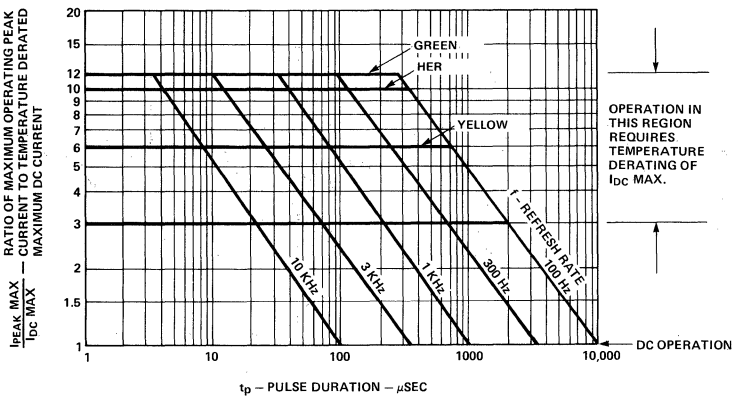


Figure 8. Maximum Tolerable Peak Current vs. Pulse Duration - HER/Yellow/Green.

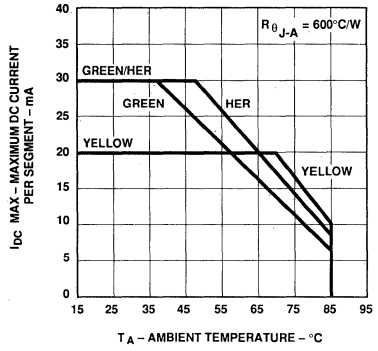


Figure 9. Maximum Allowable DC Current vs. Ambient Temperature. T_{JMAX} = 100°C.

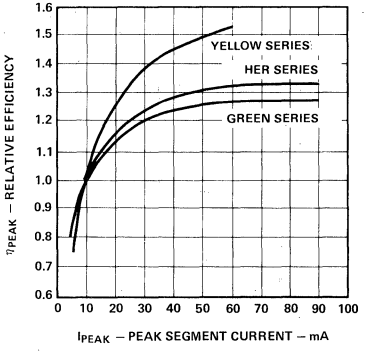


Figure 10. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

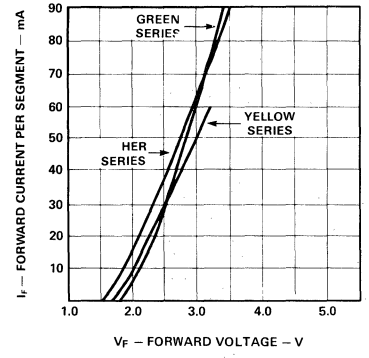


Figure 11. Forward Current vs. Forward Voltage.

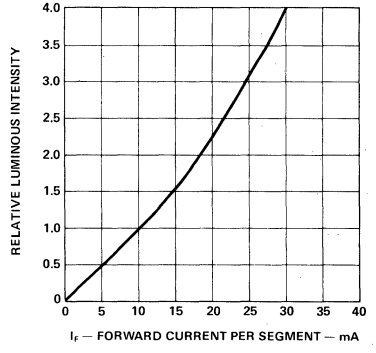


Figure 12. Relative Luminous Intensity vs. DC Forward Current.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

Electrical/Optical

These versatile bar graph arrays are composed of ten light emitting diodes. The light from each LED is optically stretched to form individual elements. The Red (HDSP-4820) bar graph array LEDs use a p-n junction diffused into a GaAsP epitaxial layer on a GaAs substrate. The AlGaAs Red (HLCP-J100) bar graph array LEDs use double heterojunction AlGaAs on a GaAs substrate. HER (HDSP-4830) and Yellow (HDSP-4840) bar graph array LEDs use a GaAsP epitaxial layer on a GaP substrate. Green (HDSP-4850) bar graph array LEDs use liquid phase GaP epitaxial layer on a GaP substrate. The multicolor bar graph arrays (HDSP-4832/4836) have HER, Yellow, and Green LEDs in one package.

These displays are designed for strobed operation. The typical forward voltage values can be scaled from Figures 5 and 11. These values should be used to calculate the current limiting resistor value and typical power consumption. Expected maximum V_F values for driver circuit design and maximum power dissipation may be calculated using the following V_FMAX models:

Standard Red HDSP-4820 series

$V_F MAX = 1.8\ V + I_{Peak}\ (10\ \Omega)$
For: $I_{Peak} \geq 5$ mA

AlGaAs Red HLCP-J100 series

$V_F MAX = 1.8\ V + I_{Peak}\ (20\ \Omega)$
For: $I_{Peak} \leq 20$ mA
$V_F MAX = 2.0\ V + I_{Peak}\ (10\ \Omega)$
For: $I_{Peak} \geq 20$ mA

HER (HDSP-4830) and Yellow (HDSP-4840) series

$V_F MAX = 1.6 + I_{Peak}\ (45\ \Omega)$
For: $5\ mA \leq I_{Peak} \leq 20$ mA
$V_F MAX = 1.75 + I_{Peak}\ (38\ \Omega)$
For: $I_{Peak} \geq 20$ mA

Green (HDSP-4850) series

$V_F MAX = 2.0 + I_{Peak}\ (50\ \Omega)$
For: $I_{Peak} > 5$ mA

Figures 4 and 10 allow the designer to calculate the luminous intensity at different peak and average currents. The following equation calculates intensity at different peak and average currents:

$I_V AVG = (I_F AVG / I_F AVG\ DATA\ SHEET)(\eta_{peak})(I_V DATA\ SHEET)$

Where:

$I_V AVG$ is the calculated time averaged luminous intensity resulting from $I_F AVG$.

$I_F AVG$ is the desired time averaged LED current.

$I_F AVG$ DATA SHEET is the data sheet test current for I_VDATA SHEET.

η_{peak} is the relative efficiency at the peak current, scaled from Figure 4 or 10.

I_V DATA SHEET is the data sheet luminous intensity, resulting from $I_F AVG$ DATA SHEET.

For example, what is the luminous intensity of an HDSP-4830 driven at 50 mA peak 1/5 duty factor?

$I_F AVG = (50\ mA)(0.2) = 10\ mA$
$I_F AVG$ DATA SHEET = 10 mA
$\eta_{Peak} = 1.3$
I_V DATA SHEET = 3500 µcd

Therefore

$I_V AVG = (10\ mA/10\ mA)(1.3)(3500\ \mu cd) = 4550\ \mu cd$

HEWLETT PACKARD

101 Element Bar Graph Array

Technical Data

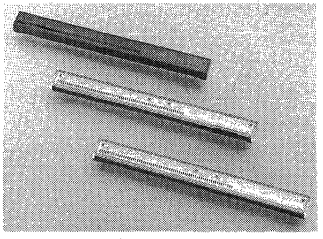
HDSP-8820
HDSP-8825
HDSP-8835

Features

- **High Resolution (1%)**
- **Excellent Element Appearance**
  Wide, Recognizable Elements
  Matched LEDs for Uniformity
  Excellent Element Alignment
- **Single-in-line Package Design**
  Sturdy Leads on Industry Standard 2.54 mm (0.100 in.) Centers
  Environmentally Rugged Package
  Common Cathode Configuration
- **Low Power Requirements 1.0 mA Average per Element at 1% Duty Cycle**
- **Support Electronics Easy Interface with Microprocessors**

Applications

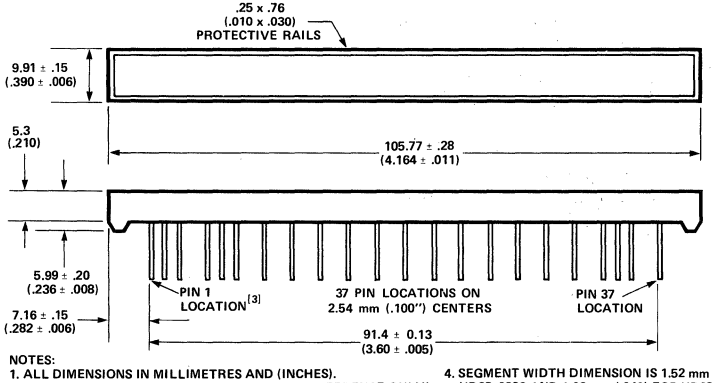
- **Industrial Process Control Systems**
- **Edgewise Panel Meters**
- **Instrumentation**
- **Position Indicators**
- **Fluid Level Indicators**



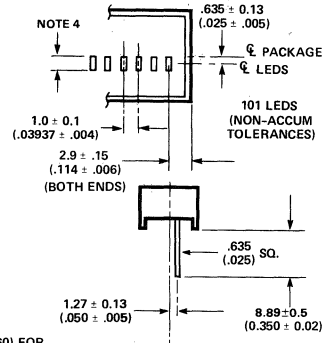
Description

The HDSP-88XX series is a family of 101-element LED linear arrays designed to display information in easily recognizable bar graph or position indicator form. The HDSP-8820, utilizing red GaAsP LED chips assembled on

Package Dimensions[1, 2]



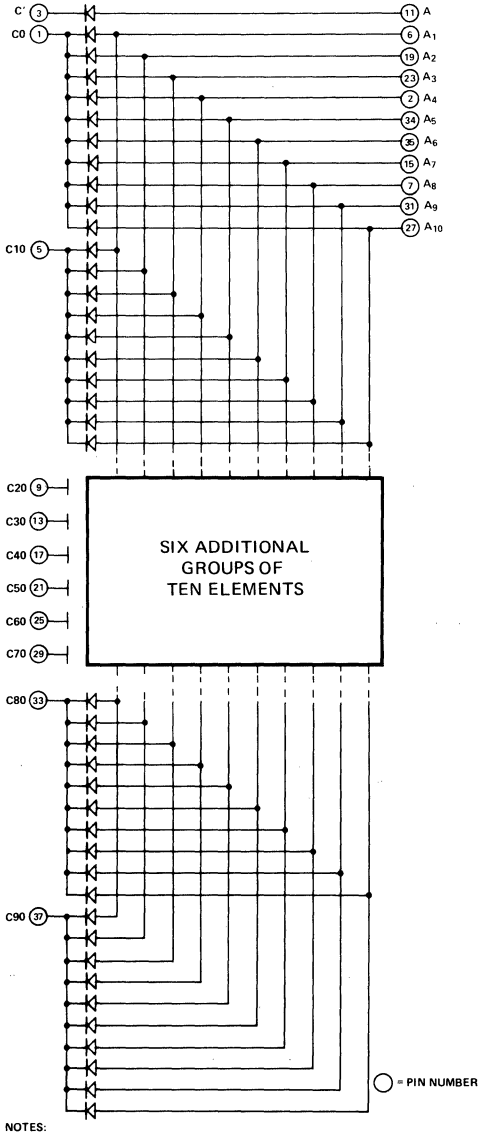
MAGNIFIED ELEMENT DESCRIPTION



NOTES:
1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. PIN 1 IDENTIFIED BY INK DOT ADJACENT TO LEAD AND HP PART NUMBER ON BACK OF PACKAGE.
4. SEGMENT WIDTH DIMENSION IS 1.52 mm (.060) FOR HDSP-8820 AND 1.02 mm (.040) FOR HDSP-8825 AND HDSP-8835. ALL OTHER DIMENSIONS INCLUDING CENTERLINE OF LEDs AND PACKAGE ARE IDENTICAL ON ALL 3 DEVICES.

a PC board and enclosed in a red polycarbonate cover with an epoxy backfill seal, has 1.52 mm (0.060 inch) wide segments. The HDSP-8825 and HDSP-8835 are high efficiency red and high performance green respectively, each with a 1.02 mm (0.040 inch) segment width. The HDSP-8825 and HDSP-8835 have a clear polycarbonate lens. Mechanical considerations and pin-out are identical among all 3 devices. The common cathode chips are addressed via 22 single-in-line pins extending from the back side of the package.

Internal Circuit Diagram[5,6]



NOTES:
5. ELEMENT LOCATION NUMBER = COMMON CATHODE NUMBER + ANODE NUMBER. FOR EXAMPLE, ELEMENT 83 IS OBTAINES BY ADDRESSING C80 AND A3.
6. A' AND C' ARE ANODE AND CATHODE OF ELEMENT ZERO.

Device Pin Description

PIN LOCATION	FUNCTION
1	C0
2	A4
3	C'(6)
4	No Pin
5	C10
6	A1
7	A8
8	No Pin
9	C20
10	No Pin
11	A'(6)
12	No Pin
13	C30
14	No Pin
15	A7
16	No Pin
17	C40
18	No Pin
19	A2
20	No Pin
21	C50
22	No Pin
23	A3
24	No Pin
25	C60
26	No Pin
27	A10
28	No Pin
29	C70
30	No Pin
31	A9
32	No Pin
33	C80
34	A5
35	A6
36	No Pin
37	C90

Absolute Maximum Ratings

Parameter	HDSP-8820	HDSP-8825	HDSP-8835
Average Power per Element (T_A = 25° C)	15 mW	20 mW	20 mW
Peak Forward Current per Element (T_A = 25° C)[7] (Pulse Width ≤ 300 μs)	200 mA	150 mA	150 mA
Average Forward Current per Element (T_A = 25° C)[8]	7 mA	5 mA	5 mA
Operating Temperature Range	−40° to +85° C	−40° to +85° C	−40° to +85° C
Storage Temperature Range	−40° to +85° C	−40° to +85° C	−40° to +85° C
Reverse Voltage per Element or DP	5.0 V	5.0 V	5.0 V
Lead Solder Temperature 1.59 mm [1.16 inch] below seating plane[9]	260° C for 3 sec.	260° C for 3 sec.	260° C for 3 sec.

Notes:

7. See Figures 1 and 2 to establish pulsed operating conditions.
8. Derate maximum average forward current above T_A = 70° C at 0.16 mA/°C/Element for the HDSP-8820 and 0.11 mA/°C/Element for the HDSP-8825 and HDSP-8835. See Figures 3 and 4.
9. Clean only in water, Isopropanol, Ethanol, Freon TF or TE (or equivalent) and Genesolv DI-15 or DE-15 (or equivalent). See mechanical section of this data sheet for information on wave soldering conditions.

Electrical/Optical Characteristics at T_A = 25°C

RED HDSP-8820

Parameter	Symbol	Units	Min.	Typ.	Max.	Test Conditions
Time averaged Luminous Intensity per Element (Unit average) [10]	I_v	μcd	8	20		100 mA Pk.: 1 of 110 Duty Factor
Peak Wavelength	λ_{PEAK}	nm		655		
Dominant Wavelength [11]	λ_d	nm		640		
Forward Voltage per Element	V_F	V		1.7	2.1	I_F = 100 mA
Reverse Voltage per Element	V_R	V	3.0			I_R = 100 μA
Temperature Coefficient V_F per Element	ΔV_F/° C	mV/° C		-2.0		
Thermal Resistance LED Junction-to-Pin	$R\Theta_{J-PIN}$	° C/W/ LED		700		

HIGH EFFICIENCY RED HDSP-8825

Parameter	Symbol	Units	Min.	Typ.	Max.	Test Conditions
Time averaged Luminous Intensity per Element (Unit average) [10]	I_v	μcd	60	175		100 mA Pk.: 1 of 110 Duty Factor
Peak Wavelength	λ_{PEAK}	nm		635		
Dominant Wavelength [11]	λ_d	nm		626		
Forward Voltage per Element	V_F	V		2.3	3.1	I_F = 100 mA
Reverse Voltage per Element	V_R	V	3.0			I_R = 100 μA
Temperature Coefficient V_F per Element	ΔV_F/° C	mV/° C		-2.0		
Thermal Resistance LED Junction-to-Pin	$R\Theta_{J-PIN}$	° C/W/ LED		1000		

Electrical/Optical Characteristics at T_A = 25°C (continued)

HIGH PERFORMANCE GREEN HDSP-8835

Parameter	Symbol	Units	Min.	Typ.	Max.	Test Conditions
Time Averaged Luminous Intensity per Element (Unit average)[10]	I_V	μcd	70	175		100 mA Pk.: 1 of 110 Duty Factor
Peak Wavelength	λ_{PEAK}	nm		568		
Dominant Wavelength[11]	λ_d	nm		574		
Forward Voltage per Element	V_F	V		2.3	3.1	I_F = 100 mA
Reverse Voltage per Element	V_R	V	3.0			I_F = 100 μA
Temperature Coefficient V_F per Element	ΔV_F/°C	mV/°C		-2.0		
Thermal Resistance LED Junction-to-Pin	$R\Theta_{J-PIN}$	°C/W/ LED		1000		

Notes:

10. Operation at peak currents of less than 100 mA may cause intensity mismatch. Consult factory for low current operation.
11. The dominant wavelength, λd, is derived from the CIE chromaticity diagram and is the single wavelength which defines the color of the device.

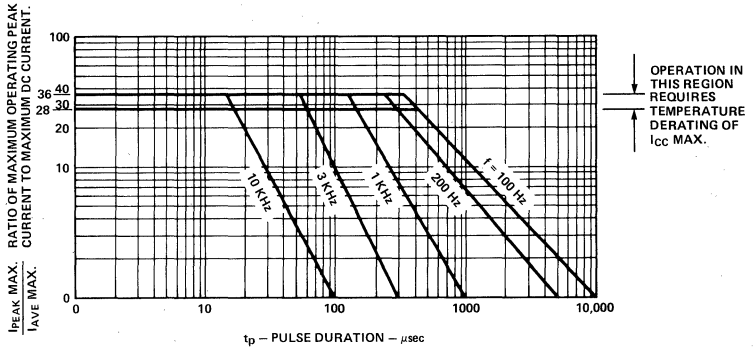


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration HDSP-8820.

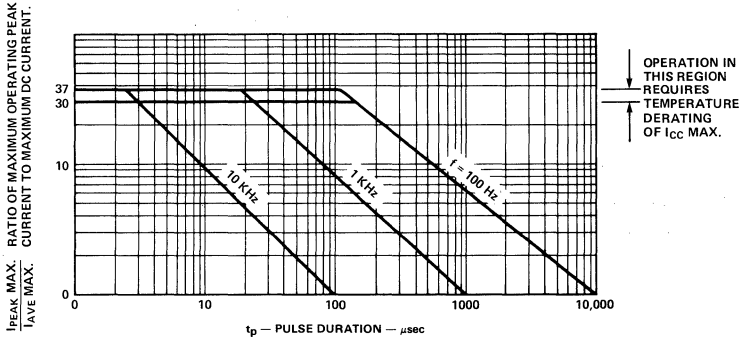


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration HDSP-8825 and HDSP-8835.

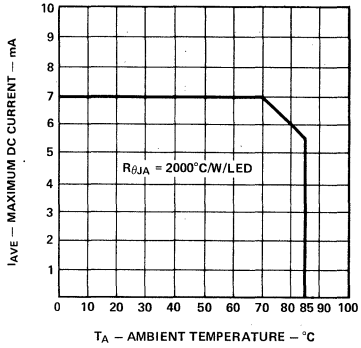


Figure 3. Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance, LED Junction-to-Ambient on a per LED Basis. T_{JMAX} = 115° C HDSP-8820.

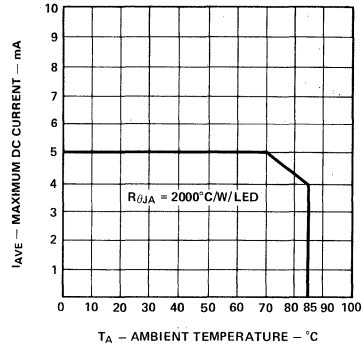


Figure 4. Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance, LED Junction-to-Ambient on a per LED Basis. T_{JMAX} = 115° C HDSP-8825/ HDSP-8835.

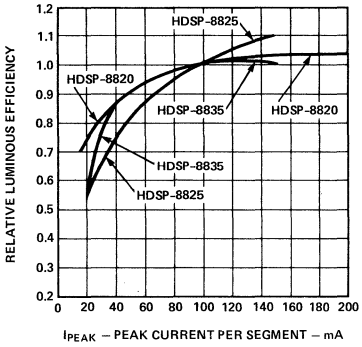


Figure 5. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current.

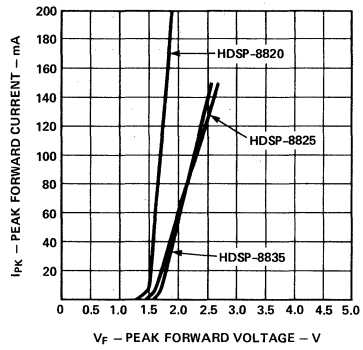


Figure 6. Forward Current vs. Forward Voltage.

For a Detailed Explanation on the Use of Data Sheet Information, See Application Note 1005.

Operational Considerations

Electrical

The HDSP-88XX is a 101 element bar graph array. The linear array is arranged as ten groups of ten LED elements plus one additional element. The ten elements of each group have common cathodes. Like elements in the ten groups have common anodes. The device is addressed via 22 single-in-line pins extending from the back side of the display.

This display is designed specifically for strobed (multiplexed) operation. Minimum peak forward current at which all elements will be illuminated is 15 mA. Display aesthetics are specified at 100 mA, 1/110 DF, peak forward current. The typical forward voltage values, scaled from Figure 6 should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum VF values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following VF model:

HDSP-8820
$V_{FMAX} = 2.02\ V + I_{PEAK}\ (0.8\Omega)$
For $I_{PEAK} > 40$ mA

HDSP-8825
$V_{FMAX} = 1.7\ V + I_{PEAK}\ (14\ \Omega)$
For $I_{PEAK} > 40$ mA

HDSP-8835
$V_{FMAX} = 1.7\ V + I_{PEAK}\ (14\ )$
For $I_{PEAK} > 40$ mA

The time averaged luminous intensity at $T_A = 25°$ C may be calculated using:
I_V Time Avg. =
$[I_{F\text{-}AVG}/I_{F\text{-}SPEC\text{-}AVG}] \cdot \eta I_{PEAK} \cdot I_{V\text{-}SPEC}$

where η, relative efficiency, may be determined from Figure 5.

The circuit in Figure 7 displays an analog input voltage in bar graph form with 101 bit resolution. The 74390 dual decade counter has been configured to count from 0 to 99. The 1Q outputs correspond to "ones" and the 20 outputs correspond to "tens". The "one" outputs from the counter drives the display element anodes through a 7442 1 of 10 BCD decoder. Sprague UDN 2585 drivers source the anodes with 80 mA peak/segment. The "ten" outputs from the counter drive the group cathodes through a 74145 BCD decoder. The circuit multiplexes segments 100 to 91 first, then segments 90 to 81, and so on with segments 10 to 1 last. During the time that the output from the T.l. TL507C A/D converter is low the corresponding display elements will be illuminated.

The TL507C is an economical A/D converter with 7 bit resolution. The single output is pulse-width-modulated to correspond to the analog input voltage magnitude. With V_{CC} = 5 V the analog input voltage range is 1.3 V to 3.9 V. The TL507C output is reset each time the 74390 resets. Duration of the high output pulse is shorter for larger analog input voltages. A high output from the TL507C disables the display by forcing the 7442 inputs to an invalid state. Hence, as the analog input voltage increases more elements of the bar graph display are illuminated. Display element zero is DC driven.

The circuit in Figure 8 uses the HDSP-88XX as a 100 bit position indicator. Two BCD input words define the position of the illuminated element. Display duty factor, 1/100, is controlled by the $\overline{\text{ENABLE}}$ signal.

Mechanical

Suitable conditions for wave soldering depend on the specific kind of equipment and procedure used. A cool down period after flow solder and before flux rinse is recommended.

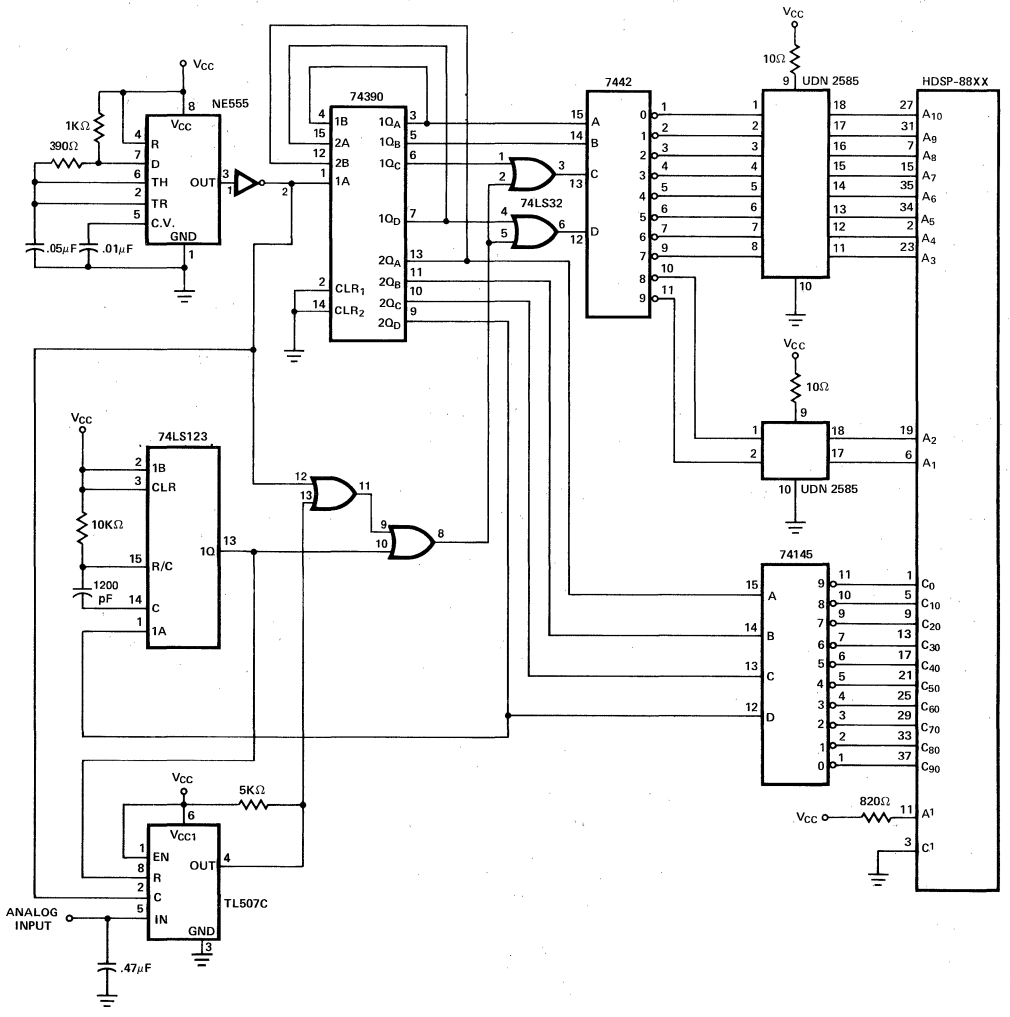


Figure 7. 101 Element Bar Graph.

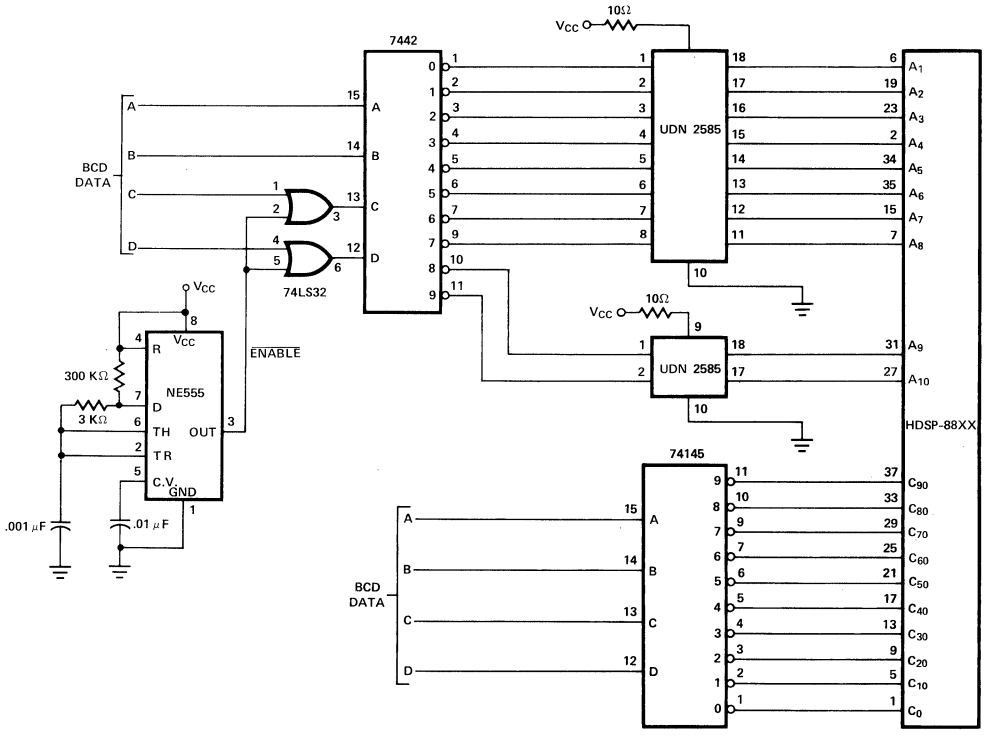


Figure 8. 100 Element Position Indicator.

HEWLETT PACKARD

Panel and Legend Mounts for LED Light Bars

Technical Data

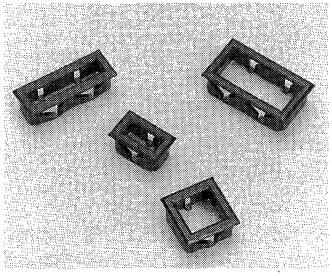
HLMP-2598
HLMP-2599
HLMP-2898
HLMP-2899

Features

- **Firmly Mounts Light Bars in Panels**
- **Holds Legends for Front Panel or PC Board Applications[1]**
- **One Piece, Snap-in Assembly**
- **Matte Black Bezel Design Enhances Panel Appearance**
- **Four Sizes Available**
- **May Be Installed in a Wide Range of Panel Thicknesses**
- **Panel Hole Easily Punched or Milled**

Description

This series of black plastic bezel mounts is designed to install Hewlett-Packard Light Bars in instrument panels ranging in thickness from 1.52 mm (0.060 inch) to 3.18 mm (0.125 inch). A space has been provided for holding a 0.13 mm (0.005 inch) film legend over the light emitting surface of the light bar module.

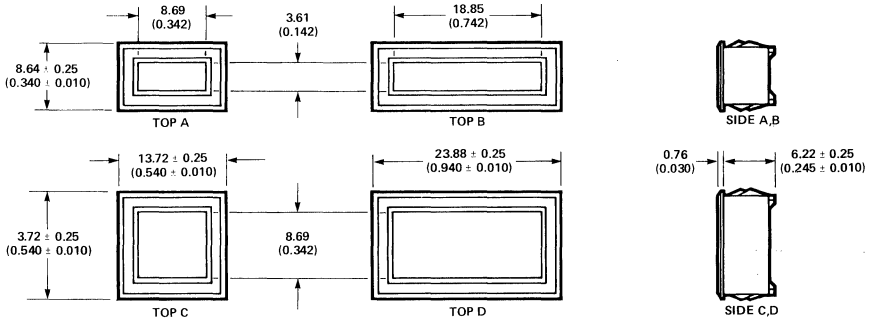


Selection Guide

Panel and Legend Mount Part No. HLMP-	Corresponding Light Bar Module Part No.		Panel Hole Installation Dimensions[2]	Package Outline	
	HLCP-	HLMP-			
2598	B100	2350, 2450, 2550	7.62 mm (0.300 inch) x 22.86 mm (0.900 inch)		B
2599	A100	2300, 2400, 2500	7.62 mm (0.300 inch) x 12.70 mm (0.500 inch)		A
2898	D100 C100	2600, 2700, 2800 2655, 2755, 2855 2950, 2965, 2980	12.70 mm (0.500 inch) x 12.70 mm (0.500 inch)		C
2899	E100 F100 G100 H100	2620, 2720, 2820 2635, 2735, 2835 2670, 2770, 2870 2685, 2785, 2885	12.70 mm (0.500 inch) x 22.86 mm (0.900 inch)		D

Notes:
1. Application Note 1012 addresses legend fabrication options.
2. Allowed hole tolerance: +0.00 mm, -0.13 mm (+0.000 inch, -0.005 inch). Permitted radius: 1.60 mm (0.063 inch).

Package Dimensions



NOTES: 1. DIMENSIONS IN MILLIMETRES (INCHES)
2. UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.

Mounting Instructions

1. Mill[3] or punch a hole in the panel. Deburr, but do not chamfer, the edges of the hole.
2. Place the front of the mount against a solid, flat surface. A film legend with outside dimensions equal to the outside dimensions of the light bar may be placed in the mount or on the light bar light emitting surface. Press the light bar into the mount until the tabs snap over the back of the light bar[4]. When inserting the HLMP-2898, align the notched sides of the light bar with the mount sides which do not have the tabs). (See Figure 1.)
3. Applying even pressure to the top of the mount, press the entire assembly into the hole from the front of the panel[5]. (See Figure 2.)

Note: For thinner panels, the mount may be pressed into the panel first, then the light bar may be pressed into the mount from the back side of the panel.

Suggested Punch Sources

Hole punches may be ordered from one of the following sources:

Danly Machine Corporation
Punchrite Division
15400 Brookpark Road
Cleveland, OH 44135
(216) 267-1444

Ring Division
The Producto Machine Company
Jamestown, NY 14701
(800) 828-2216

Porter Precision Products Company
12522 Lakeland Road
Santa Fe Springs, CA 90670
(213) 946-1531

Di-Acro Division
Houdaille Industries
800 Jefferson Street
Lake City, MN 55041
(612) 345-4571

Notes:
3. A 3.18 mm (0.125 inch) diameter mill may be used.
4. Repetitve insertion of the light bar into mount may cause damage to the mount.
5. Repetitive insertion of the mount into the panel will degrade the retention force of the mount.

Installation Sketches

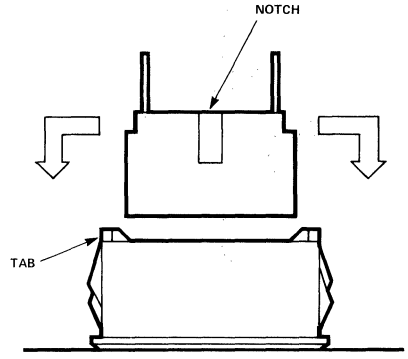


Figure 1. Installation of a Light Bar into a Panel Mount.

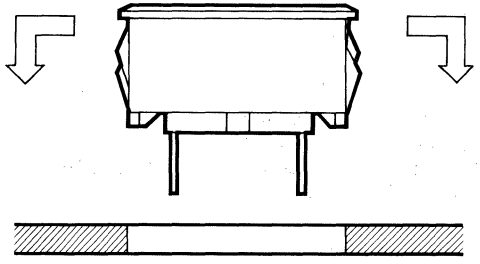


Figure 2. Installation of the Light Bar/Panel Mount Assembly into a Front Panel.

LED Light Bars Standard Options

Technical Data

Option S02, S22

Description

Due to applications that require tightly matched devices, Hewlett-Packard has developed several standard options to service these requirements.

Option S02 consists of devices which are selected to two Iv categories. All color bins of the base parts (yellow and green devices) fulfill the color requirements of these products.

Option S22 consists of devices which are selected to two Iv categories and two color bin categories.

Ordering Information

To order Light Bars with these standard options, order the base part number and add the option code (S02, S22). For any base part number that does not appear in the following tables, please consult your local Hewlett-Packard representative or your local franchise distributor.

OPTION S02 – Partial base part number list:

HDSP-4820
HDSP-4830
HDSP-4840
HDSP-4850
HLCP-A100
HLCP-B100
HLCP-C100
HLCP-D100
HLCP-E100
HLCP-F100
HLCP-G100
HLCP-H100
HLMP-2300
HLMP-2316
HLMP-2350
HLMP-2400
HLMP-2450
HLMP-2500
HLMP-2550
HLMP-2600
HLMP-2620
HLMP-2635
HLMP-2655
HLMP-2670
HLMP-2685
HLMP-2700
HLMP-2720
HLMP-2735
HLMP-2755
HLMP-2770
HLMP-2785
HLMP-2800
HLMP-2820
HLMP-2835
HLMP-2855
HLMP-2870
HLMP-2885
HLMP-2950

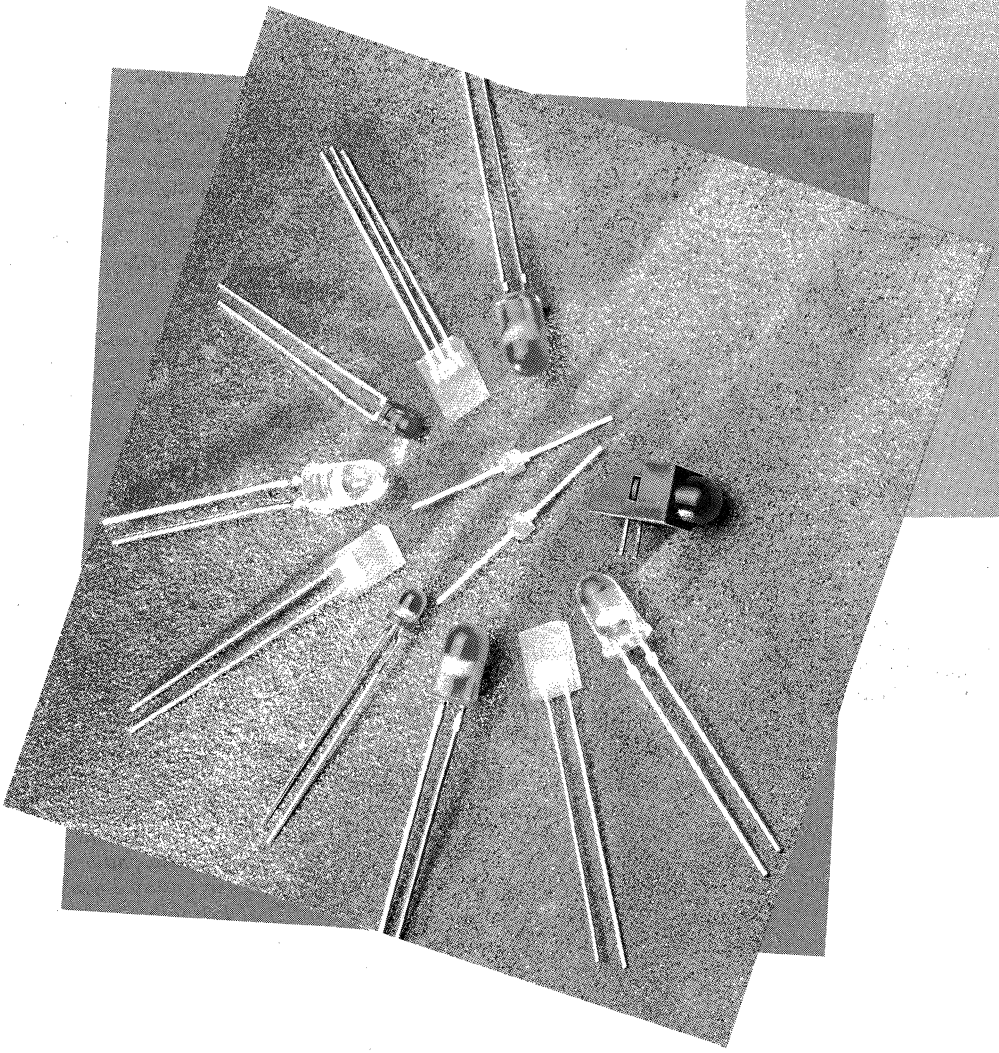
OPTION S22 - Partial base part number list:

HLMP-2400
HMLP-2500
HLMP-2855
HLMP-2965
HLMP-2450
HLMP-2735
HLMP-2755
HLMP-2785
HLMP-2885
HLMP-2550
HDSP-4840
HDSP-4850

HEWLETT PACKARD

Solid State Lamps

- AlInGaP Lamps
- AlGaAs Lamps
- General Purpose Lamps
- Special Purpose Lamps
- Standard Options
- JAN Qualified Hermetic Lamps



HEWLETT PACKARD

Solid State Lamps

From General to Special Purpose Solid State Lamps, Hewlett-Packard continues to grow its LED lamp product offering. This year, HP has expanded its material technology from AS AlGaAs to TS AlGaAs and then to AlInGaP.

In coupling with its superior packaging technology, HP is ready to address the growth sector of high brightness applications such as Moving Message Panels and Automotive Exterior Lightings. In addition, these LEDs are capable of being driven by higher current than traditional LEDs and this results in increased light output. Finally, designers will have a high reliability alternative to applications which traditionally required the brightness supplied by incandescent bulbs.

NEW Product Offerings!

Solid State Lamps

High Power AlInGaP Amber and Reddish Orange Lamps
HLMA-BL00/CL00/CH00/DH00/DG00/DL00/KL00/QL00/QH00
HSMA-T125, HSML-T125
These lamps utilize a newly developed aluminum indium gallium phosphide LED material and are available in various water clear packages. This material has a very high luminous efficiency, capable of producing high light output over a wide range of drive currents. The lamp package incorporates an advanced optical design that produces an extremely high peak intensity within a very narrow viewing angle.

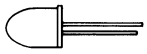
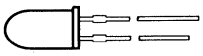
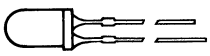
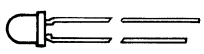
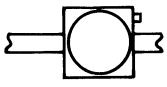
Blue T-1¾, 5 mm Lamps
HLMP-DB00/HLMP-DB15
These untinted diffused and nondiffused T-1¾ LED blue lamps utilize single crystal silicon carbide technology. The color is an 80% saturated blue with a dominant wavelength of 481 nanometers.

Low Profile Surface Mount Indicator Lamps
HSMX-C650/C670, HSMF-C655
These single and bicolor LEDs are designed in an industry standard package for ease of handling and use. Five different LED colors are available in two compact, low profile, single color packages.

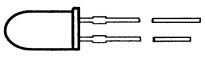
Surface Mount Lamps
HSMS-TX00/HSMS-TX00/HSMD-TX00/HSMY-TX00/HSMG-TX00
These solid state surface mount indicators are designed with a flat top and sides to be easily handled by automatic placement equipment. Two new colors were added to the existing product family. They are now available in yellow and High Performance Green as well as DH AlGaAs Red, HER, and orange.

High Power T-1¾, 5 mm TS AlGaAs Red Lamps
HLMP-C100, HLMP-C110
These lamps utilize the highly optimized LED material, transparent substrate aluminum gallium arsenide, and are available in untinted non-diffused T-1¾, 5 mm packages.

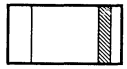
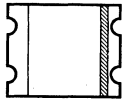
AlinGaP Lamps

Device		Description			Typical Luminous Intensity @ 20 mA	2θ 1/2	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	New HLMA-BL00	Amber (592 nm)	T-4	Untinted Nondiffused	15.0 cd	3°	1.9 V	3-30
	New HLMA-CH00 New HLMA-CL00	Amber (592 nm) and Reddish Orange (615/ 622 nm)	T-1¾	Untinted Nondiffused	3000 mcd	7°		3-24
	New HLMA-DG00 New HLMA-DH00 New HLMA-DL00				600 800 1000 mcd	30°		
	New HLMA-KH00 New HLMA-KL00		T-1		200 mcd	45°		
	New HLMA-QH00 New HLMA-QL00		Subminiature		500 mcd	28°		

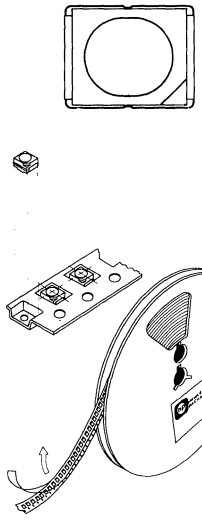
Blue Lamps

Device		Description			Typical Luminous Intensity @ 20 mA	2θ 1/2	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	New HLMP-DB00	Blue	T-1¾	Diffused	3.0 mcd	38	3 V	3-33
	New HLMP-DB15			Untinted Nondiffused	12 mcd	15		

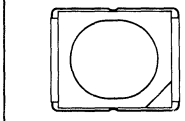
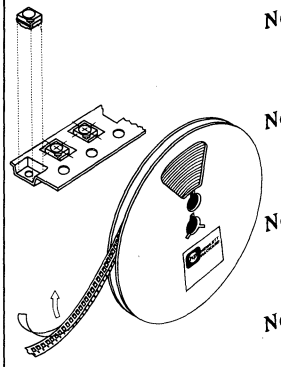
Surface Mount Lamps

Device		Description			Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
 -C650	New HSMH-C650	DH AlGaAs Red (639 nm)	Very low profile, Small footprint	Flat Diffused	16.0	1.8	3-37
	New HSMH-C670		Very low profile, Very small footprint				
 -C670	New HSMS-C650	HER (626 nm)	Very low profile, Small footprint		5.0	1.9	
	New HSMS-C670		Very low profile, Very small footprint				
 -C655	New HSMD-C650	Orange (604 nm)	Very low profile, Small footprint		4.0	2.1	
	New HSMD-C670		Very low profile, Very small footprint				
	New HSMY-C650	Yellow (584 nm)	Very low profile, Small footprint		5.0	2.1	
	New HSMY-C670		Very low profile, Very small footprint				
	New HSMG-C650	Green (571 nm)	Very low profile, Small footprint		9.0	2.2	
	New HSMG-C670		Very low profile, Very small footprint				
	New HSMF-C655	Bi-color HER Green	Very low profile		5.0 9.0	1.9 2.2	

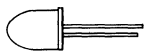
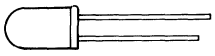
Surface Mount Lamps (contd.)

Device		Description			Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	New HSMH-T400	DH AS AlGaAs Red (637 nm)	Low Profile 12 mm Tape 7" Reel, 2000 Devices	Oval, Flat Non-diffused	17.0 mcd @ 10 mA	10 mA @ 1.8 V	3-81
	New HSMH-T500		Low Profile 12 mm Tape 13" Reel, 8000 Devices				
	New HSMH-T600		Low Profile 8 mm Tape 7" Reel, 2000 Devices				
	New HSMH-T700		Low Profile 8 mm Tape 13" Reel, 8000 Devices				
	New HSMS-T400	HER (626 nm)	Low Profile 12 mm Tape 7" Reel, 2000 Devices		6.0 mcd @ 10 mA	10 mA @ 1.9 V	
	New HSMS-T500		Low Profile 12 mm Tape 13" Reel, 8000 Devices				
	New HSMS-T600		Low Profile 8 mm Tape 7" Reel, 2000 Devices				
	New HSMS-T700		Low Profile 8 mm Tape 13" Reel, 8000 Devices				

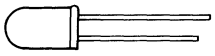
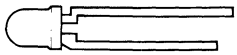
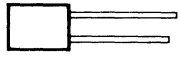
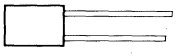
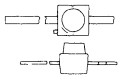
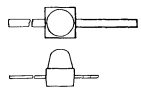
Surface Mount Lamps (contd.)

Device		Description			Typical Luminous Intensity @ 10 mA	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
 	New HSMD-T400	Orange (602 nm)	Low Profile 12 mm Tape 7" Reel, 2000 Devices	Oval, Flat Non-diffused	5.0 mcd	10 mA @ 1.9 V	3-81
	New HSMD-T500		Low Profile 12 mm Tape 13" Reel, 8000 Devices				
	New HSMD-T600		Low Profile 8 mm Tape 7" Reel, 2000 Devices				
	New HSMD-T700		Low Profile 8 mm Tape 13" Reel, 8000 Devices				
	New HSMY-T400	Yellow (585 nm)	Low Profile 12 mm Tape 7" Reel, 2000 Devices		5.0 mcd	10 mA @ 2.0 V	
	New HSMY-T500		Low Profile 12 mm Tape 13" Reel, 8000 Devices				
	New HSMY-T600		Low Profile 8 mm Tape 7" Reel, 2000 Devices				
	New HSMY-T700		Low Profile 8 mm Tape 13" Reel, 8000 Devices				
	New HSMG-T400	High Perfor-mance Green (572 nm)	Low Profile 12 mm Tape 7" Reel, 2000 Devices		10.0 mcd	10 mA @ 2.0 V	
	New HSMG-T500		Low Profile 12 mm Tape 13" Reel, 8000 Devices				
	New HSMG-T600		Low Profile 8 mm Tape 7" Reel, 2000 Devices				
	New HSMG-T700		Low Profile 8 mm Tape 13" Reel, 8000 Devices				

High Power TS AlGaAs Lamps

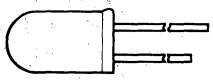
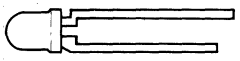
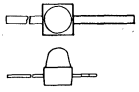
Device		Description			Typical Luminous Intensity @ 20 mA	2θ 1/2	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-8150	Red (637 nm)	T-4	Untinted Nondiffused	15.0 cd	4°	1.85 V	3-89
	HLMP-8103	Red (644 nm)	T-1¾		3.0 cd	7°		3-44
	HLMP-8102				2.0 cd			
	HLMP-8100				1.0 cd	19°		
	New HLMP-C100				0.75	30°		
	New HLMP-C110				0.40	40°		

High Intensity DH AlGaAs Lamps

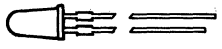
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-D101 ✪	AlGaAs Red (637 nm)	T-1¾	Tinted Diffused	70.0 mcd @ 20 mA	65°	1.8 V @ 20 mA	3-49
	HLMP-D105			Untinted Nondiffused	240.0 mcd @ 20 mA	24°		
	HLMP-K101	AlGaAs Red (637 nm)	T-1	Tinted Diffused	45.0 mcd @ 20 mA	60°		
	HLMP-K105 ✪			Untinted Nondiffused	65.0 mcd @ 20 mA	45°		
	HLMP-R100		Rectangular	Tinted Diffused	7.5 mcd @ 20 mA	100°		3-133
	HLMP-S100		2 mm x 5 mm Rectangular		7.5 mcd @ 20 mA	110°		3-137
	HLMP-P105		Flat Top Subminiature	Untinted Nondiffused	10.0 mcd @ 10 mA	125°	1.7 V @ 10 mA	3-141
	HLMP-Q101		Subminiature	Tinted Diffused	45.0 mcd @ 20 mA	70°	1.8 V @ 20 mA	
	HLMP-Q105			Untinted Nondiffused	55.0 mcd @ 10 mA	28°	1.7 V @ 10 mA	

✪This product is a regularly stocked item for Hewlett-Packard and is recommended for new designs.

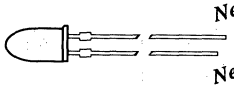
Low Current DH AlGaAs Lamps

Device		Description			Typical Luminous Intensity @ 1 mA	2θ 1/2	Typical Forward Voltage @ 1 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-D150	AlGaAs Red (637 nm)	T-1 3/4	Tinted Diffused	3.0 mcd	65°	1.6 V	3-54
	HLMP-D155			Untinted Nondiffused	10.0 mcd	24°		
	HLMP-K150 ✪		T-1	Tinted Diffused	2.0 mcd	60°		
	HLMP-K155 ✪			Untinted Nondiffused	3.0 mcd	45°		
	HLMP-Q150		Subminiature	Tinted Diffused	1.8 mcd	70°		3-141
	HLMP-Q155			Untinted Nondiffused	4.0 mcd	28°		

Very High Intensity AlGaAs Lamps

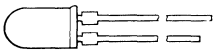
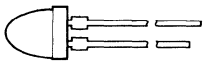
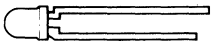
Device		Description			Typical Luminous Intensity @ 20 mA	2θ 1/2	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-4100	AlGaAs Red (637 nm)	T-1 3/4	Untinted Nondiffused	750.0 mcd	8°	1.8 V	3-59
	HLMP-4101				1000.0 mcd			

Super Ultrabright Lamps

Device		Description			Typical Luminous Intensity @ 20 mA	2θ 1/2	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	New HLMP-8115 New HLMP-8109	DH AS AlGaAs (637 nm)	T-1¾	Untinted Non-diffused	1200 mcd 500 mcd	15° 25°	1.8 V	3-63
	New HLMP-8205 New HLMP-8209	HER (626 nm)			350 mcd 260 mcd	15° 25°	1.9 V	
	New HLMP-8305 New HLMP-8309	Yellow (585 nm)			350 mcd 260 mcd	15° 25°	2.1 V	
	New HLMP-8405 New HLMP-8409	Orange (602 nm)			350 mcd 260 mcd	15° 25°	1.9 V	
	New HLMP-8505 New HLMP-8509	High Perf. Green (569 nm)			350 mcd 260 mcd	15° 25°	2.2 V	
	New HLMP-8605	Emerald Green (560 nm)			75 mcd	15°	2.2 V	

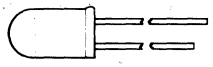
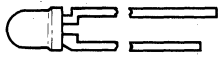
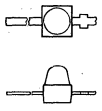
✪This product is a regularly stocked item for Hewlett-Packard and is recommended for new designs.

Ultrabright Lamps

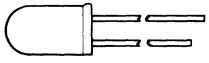
Device		Description			Typical Luminous Intensity		Typical Forward Voltage	Page
Package Outline Drawing	Part No.	Color	Package	Lens	@ 20 mA	2θ 1/2	@ 20 mA	No.
	HLMP-3750 ✪	High Efficiency Red (626 nm)	T-1¾	Untinted Non-diffused	125 mcd	24°	1.9 V	3-71
	HLMP-3850	Yellow (585 nm)			140 mcd		2.1 V	
	HLMP-3950 ✪	Green (569 nm)			120 mcd		2.2 V	
New	HLMP-D640	Emerald Green (558 nm)			21 mcd		2.2 V	
	HLMP-3390	High Efficiency Red (626 nm)	T-1¾ Low Profile	Untinted Non-diffused	55 mcd	32°	1.9 V	
	HLMP-3490	Yellow (585 nm)					2.1 V	
	HLMP-3590	Green (569 nm)					2.2 V	
	HLMP-1340 ✪	High Efficiency Red (626 nm)	T-1	Untinted Non-diffused	45 mcd	45°	1.9 V	
	HLMP-1440	Yellow (585 nm)					2.1 V	
	HLMP-1540 ✪	Green (569 nm)					2.2 V	
New	HLMP-K640	Emerald Green (558 nm)			21 mcd		2.2 V	

✪This product is a regularly stocked item for Hewlett-Packard and is recommended for new designs.

Low Current Lamps

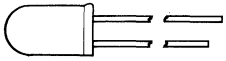
Device		Description			Typical Luminous Intensity @ 2 mA	2θ 1/2	Typical Forward Voltage @ 2 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-4700 ✪	High Efficiency Red (626 nm)	T-1¾	Tinted Diffused	2.0 mcd	50°	1.8 V	3-76
	HLMP-4719	Yellow (585 nm)			1.8 mcd		1.9 V	
	HLMP-4740	Green (569 nm)			1.8 mcd		1.8 V	
	HLMP-1700 ✪	High Efficiency Red (626 nm)	T-1	Tinted Diffused	1.8 mcd	50°	1.8 V	
	HLMP-1719 ✪	Yellow (585 nm)			1.6 mcd		1.9 V	
	HLMP-1790 ✪	Green (569 nm)			1.6 mcd		1.8 V	
	HLMP-7000	High Efficiency Red (626 nm)	Subminiature	Tinted Diffused	0.8 mcd	90°	1.8 V	3-141
	HLMP-7019	Yellow (585 nm)			0.6 mcd		1.9 V	
	HLMP-7040	Green (569 nm)			0.6 mcd		1.8 V	

High Intensity T-1¾ Lamps

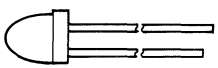
Device		Description			Typical Luminous Intensity @ 10 mA	2θ 1/2	Typical Forward Voltage @ 10 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-3315	High Efficiency Red (626 nm)	T-1¾	Tinted Non-diffused	40 mcd	35°	1.9 V	3-93
	HLMP-3316				60 mcd			
	HLMP-3415	Yellow (585 nm)			40 mcd		2.0 V	
	HLMP-3416				50 mcd			
	HLMP-3517	Green (569 nm)			50 mcd	24°	2.1 V	
	HLMP-3519				70 mcd			

✪This product is a regularly stocked item for Hewlett-Packard and is recommended for new designs.

Diffused (Wide Angle) T-1 3/4 Lamps

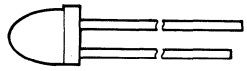
Device		Description			Typical Luminous Intensity @ 10 mA	2θ 1/2	Typical Forward Voltage @ 10 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-3300 ✪	High Efficiency Red (626 nm)	T-1 3/4	Tinted Diffused	3.5 mcd	60°	1.9 V	3-99
	HLMP-3301 ✪				7.0 mcd			
	HLMP-3762 ✪				12.0 mcd			
	HLMP-D400	Orange (602 nm)			3.5 mcd		1.9 V	
	HLMP-D401				7.0 mcd			
	HLMP-3400	Yellow (585 nm)			4.0 mcd		2.0 V	
	HLMP-3401 ✪				8.0 mcd			
	HLMP-3862				12.0 mcd			
	HLMP-3502 ✪	Green (569 nm)			2.4 mcd		2.1 V	
	HLMP-3507 ✪				5.2 mcd			
	HLMP-3962				11.0 mcd			
New	HLMP-D600	Emerald Green (558 nm)			3.0 mcd		2.1 V	

High Intensity T-1 3/4 Low Profile Lamps

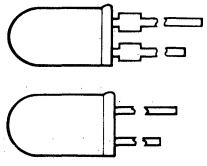
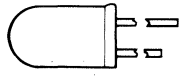
Device		Description			Typical Luminous Intensity @ 10 mA	2θ 1/2	Typical Forward Voltage @ 10 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-3365	High Efficiency Red (626 nm)	T-1 3/4 Low Profile	Tinted Non-Diffused	10 mcd	45°	1.9 V	3-106
	HLMP-3366				18 mcd			
	HLMP-3465	Yellow (585 nm)			12 mcd		2.0 V	
	HLMP-3466				18 mcd			
	HLMP-3567	Green (569 nm)			7 mcd	40°	2.1 V	
	HLMP-3568				15 mcd			

✪This product is a regularly stocked item for Hewlett-Packard and is recommended for new designs.

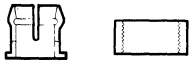
Diffused (Wide Angle) T-1 3/4 Low Profile Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-3200	Red (640 nm)	T-1 3/4 Low Profile	Tinted Diffused	2.0 mcd @ 20 mA	60°	1.6 V @ 20 mA	3-106
	HLMP-3201				4.0 mcd @ 20 mA			
	HLMP-3350	High Efficiency Red (626 nm)			3.5 mcd @ 10 mA	50°	1.9 V @ 10 mA	
	HLMP-3351				7.0 mcd @ 10 mA			
	HLMP-3450	Yellow (585 nm)			4.0 mcd @ 10 mA		2.0 V @ 10 mA	
	HLMP-3451				10.0 mcd @ 10 mA			
	HLMP-3553	Green (569 nm)			3.2 mcd @ 10 mA		2.1 V @ 10 mA	
	HLMP-3554				10.0 mcd @ 10 mA			

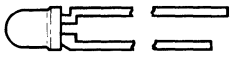
Standard Red T-1 3/4 Lamps

Device		Description			Typical Luminous Intensity @ 20 mA	2θ 1/2	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-3000	Red (648 nm)	T-1 3/4	Tinted Diffused	2.0 mcd	60°	1.6 V	3-114
	HLMP-3001				4.0 mcd			
	HLMP-3002				2.0 mcd			
	HLMP-3003				4.0 mcd			
	HLMP-3050			Tinted Non-Diffused	2.5 mcd	24°		

T-1 3/4 Mounting Hardware

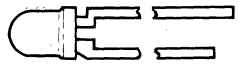
Device		Description	Page No.
Package Outline Drawing	Part No.		
	HLMP-0104	Mounting Clip and Ring for T-1 3/4 Lamps	3-169

T-1 High Intensity Lamps

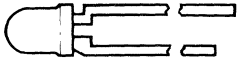
Device		Description			Typical Luminous Intensity @ 10 mA	2θ 1/2	Typical Forward Voltage @ 10 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-1320	High Efficiency Red (626 nm)	T-1	Untinted Nondiffused	12 mcd	45°	1.9 V	3-117
	HLMP-1321			Tinted Nondiffused				
	HLMP-1420	Yellow (585 nm)		Untinted Nondiffused	12 mcd		2.0 V	
	HLMP-1421			Tinted Nondiffused				
	HLMP-1520	Green (569 nm)		Untinted Nondiffused	12 mcd		2.1 V	
	HLMP-1521 ✪			Tinted Nondiffused				

✪This product is a regularly stocked item for Hewlett-Packard and is recommended for new designs.

T-1 Diffused (Wide Angle) Lamps

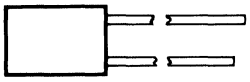
Device		Description			Typical Luminous Intensity @ 10 mA	2θ 1/2	Typical Forward Voltage @ 10 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-1300	High Efficiency Red (626 nm)	T-1	Tinted Diffused	5.0 mcd	60°	1.9 V	3-123
	HLMP-1301 ✪				5.5 mcd			
	HLMP-1302 ✪				7.0 mcd			
	HLMP-1385				10.0 mcd			
	HLMP-K400	Orange (602 nm)			4.0 mcd		1.9 V	
	HLMP-K401				5.0 mcd			
	HLMP-K402				6.5 mcd			
	HLMP-1400	Yellow (585 nm)			5.0 mcd		2.0 V	
	HLMP-1401				6.0 mcd			
	HLMP-1402				7.0 mcd			
	HLMP-1485				10.0 mcd			
	HLMP-1503 ✪	Green (569 nm)			5.0 mcd		2.1 V	
	HLMP-1523				7.0 mcd			
	HLMP-1585 ✪				8.5 mcd			
New	HLMP-K600	Emerald Green (558 nm)			1.0 mcd		2.1 V	

T-1 Standard Red Lamps

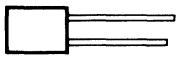
Device		Description			Typical Luminous Intensity @ 20 mA	2θ 1/2	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-1000	Red (648 nm)	T-1	Tinted Diffused	1.0 mcd	60°	1.6 V	3-129
	HLMP-1002				2.5 mcd			
	HLMP-1080			Untinted Diffused	1.5 mcd			
	HLMP-1071			Untinted Non-Diffused	2.0 mcd	45°	1.6 V	
	HLMP-1200		T-1 Low Profile	Untinted Non-Diffused	1.0 mcd	55°	1.6 V	
	HLMP-1201				2.5 mcd			

✪This product is a regularly stocked item for Hewlett-Packard and is recommended for new designs.

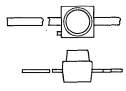
Rectangular Lamps

Device		Description			Typical Luminous Intensity @ 20 mA	2θ 1/2	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-R100	DH AlGaAs Red (637 nm)	Rectangular	Tinted Diffused	7.5 mcd	100°	1.8 V	3-133
	HLMP-0300	High Efficiency Red (626 nm)			2.5 mcd		1.9 V	
	HLMP-0301				5.0 mcd			
	HLMP-0400	Yellow (585 nm)			2.5 mcd		2.1 V	
	HLMP-0401				5.0 mcd			
	HLMP-0503	Green (569 nm)			2.5 mcd		2.2 V	
	HLMP-0504				5.0 mcd			

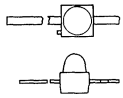
2 mm x 5 mm Rectangular Lamps

Device		Description			Typical Luminous Intensity @ 20 mA	2θ 1/2	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-S100	DH AlGaAs Red (637 nm)	2 mm x 5 mm Rectangular	Tinted Diffused	7.5 mcd	110°	1.8 V	3-137
	HLMP-S200	High Efficiency Red (626 nm)			3.5 mcd		1.9 V	
	HLMP-S201				4.8 mcd			
	HLMP-S400	Orange (602 nm)			3.5 mcd		1.9 V	
	HLMP-S401				4.8 mcd			
	HLMP-S300	Yellow (585 nm)			2.1 mcd		2.1 V	
	HLMP-S301				3.5 mcd			
	HLMP-S500	Green (569 nm)			4.0 mcd		2.2 V	
	HLMP-S501				5.8 mcd			
New	HLMP-S600	Emerald Green (558 nm)			3.0 mcd		2.2 V	

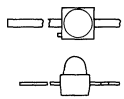
Subminiature Flat Top Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-P005	Standard Red (640 nm)	Flat Top Subminiature	Untinted Non-Diffused	2.5 mcd @ 10 mA	125°	1.6 V @ 10 mA	3-141
	HLMP-P105	DH AlGaAs Red (637 nm)			45.0 mcd @ 20 mA		1.8 V @ 20 mA	
	HLMP-P205	High Efficiency Red (626 nm)			5.0 mcd @ 10 mA		1.8 V @ 10 mA	
	HLMP-P405	Orange (602 nm)			4.0 mcd @ 10 mA		1.9 V @ 10 mA	
	HLMP-P305	Yellow (585 nm)			4.0 mcd @ 10 mA		2.0 V @ 10 mA	
	HLMP-P505	Green (569 nm)			5.0 mcd @ 10 mA		2.0 V @ 10 mA	
New	HLMP-P605	Emerald Green (558 nm)			1.5 mcd @ 10 mA		2.0 V @ 10 mA	

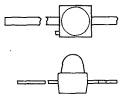
Subminiature Diffused Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-6000	Standard Red (640 nm)	Subminiature	Tinted Diffused	1.2 mcd @ 10 mA	90°	1.6 V @ 10 mA	3-141
	HLMP-6001				3.2 mcd @ 10 mA		1.6 V @ 10 mA	
	HLMP-Q101	DH AlGaAs Red (637 nm)			45.0 mcd @ 20 mA		1.8 V @ 20 mA	
	HLMP-6300	High Efficiency Red (626 nm)			3.0 mcd @ 10 mA		1.8 V @ 10 mA	
	HLMP-Q400	Orange (602 nm)			3.0 mcd @ 10 mA		1.9 V @ 10 mA	
	HLMP-6400	Yellow (585 nm)			3.0 mcd @ 10 mA		2.0 V @ 10 mA	
	HLMP-6500	Green (569 nm)			3.0 mcd @ 10 mA		2.0 V @ 10 mA	
New	HLMP-Q600	Emerald Green (558 nm)			1.5 mcd @ 10 mA		2.0 V @ 10 mA	

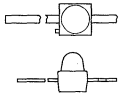
Subminiature Nondiffused Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-Q105	DH AlGaAs Red (637 nm)	Subminiature	Untinted Non-diffused	55.0 mcd @ 20 mA	28°	1.8 V @ 20 mA	3-141
	HLMP-6305	High Efficiency Red (626 nm)			12.0 mcd @ 10 mA		1.8 V @ 10 mA	
	HLMP-6405	Yellow (585 nm)			12.0 mcd @ 10 mA		2.0 V @ 10 mA	
	HLMP-6505	Green (569 nm)			12.0 mcd @ 10 mA		2.0 V @ 10 mA	

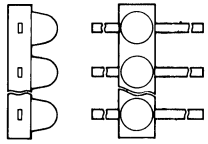
Subminiature Low Current Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-Q150	DH AlGaAs Red (637 nm)	Subminiature	Tinted Diffused	1.8 mcd @ 1.0 mA	90°	1.6 V @ 1.0 mA	3-141
	HLMP-Q155			Untinted Nondiffused	4.0 mcd @ 1.0 mA	28°		
	HLMP-7000	High Efficiency Red (626 nm)		Tinted Diffused	0.8 mcd @ 2.0 mA	90°	1.8 V @ 10.0 mA	
	HLMP-7019	Yellow (585 nm)			0.6 mcd @ 2.0 mA		2.0 V @ 10.0 mA	
	HLMP-7040	Green (569 nm)			0.6 mcd @ 2.0 mA		2.0 V @ 10.0 mA	

Subminiature Resistor Lamps

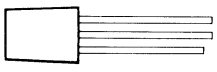
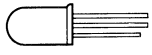
Device		Description			Typical Luminous Intensity @ 5.0 V	2θ 1/2	Typical Forward Voltage @ 5.0 V	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-6600	High Efficiency Red (626 nm)	Subminiature Resistor	Tinted Diffused	5 mcd	90°	9.6 mA	3-141
	HLMP-6620				2 mcd		3.5 mA	
	HLMP-6700	Yellow (585 nm)			5 mcd		9.6 mA	
	HLMP-6720				2 mcd		3.5 mA	
	HLMP-6800	Green (569 nm)			5 mcd		9.6 mA	
	HLMP-6820				2 mcd		3.5 mA	

Subminiature Lamp Arrays

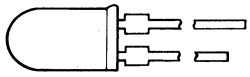
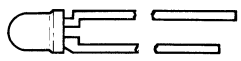
Device		Description				Typical Luminous Intensity @ 10 mA	2θ 1/2	Typical Forward Voltage @ 10 mA	Page No.
Package Outline Drawing	Part No.	Color	Package		Lens				
	HLMP-6203 HLMP-6204 HLMP-6205 HLMP-6206 HLMP-6208	Red (640 nm)	Array †	3 4 5 6 8	Tinted Diffused	1.2 mcd	90°	1.6 V	3-141
	HLMP-6653 HLMP-6654 HLMP-6655 HLMP-6656 HLMP-6658	High Efficiency Red (626 nm)		3 4 5 6 8		3.0 mcd		1.8 V	
	HLMP-6753 HLMP-6754 HLMP-6755 HLMP-6756 HLMP-6758	Yellow (585 nm)		3 4 5 6 8				2.0 V	
	HLMP-6853 HLMP-6854 HLMP-6855 HLMP-6856 HLMP-6858	Green (569 nm)		3 4 5 6 8				2.0 V	

†Array length

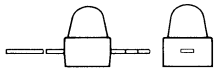
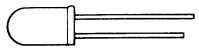
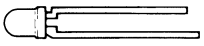
Bicolor Solid State Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-0800	High Efficiency Red (626 nm)	2 mm x 5 mm Rectangular	Untinted Diffused	3.5 mcd @ 20 mA	100°	1.9 V @ 10 mA	3-155
		Green (569 nm)			4.0 mcd @ 20 mA		2.1 mA @ 10 mA	
	HLMP-4000	High Efficiency Red (626 nm)	T-1 3/4	Untinted Diffused	5.0 mcd @ 10 mA	65°	1.9 V @ 10 mA	
		Green (569 nm)			2.0 mcd @ 10 mA		2.1 mA @ 10 mA	

T-1 3/4 and T-1 Integrated Resistor Lamps

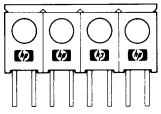
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-3105	Red (648 nm)	T-1 3/4	Tinted Diffused	3.0 mcd @ 5 V	60°	13 mA @ 5 V	3-159
	HLMP-3112				3.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-3600	High Efficiency Red (626 nm)			8.0 mcd @ 5 V		10 mA @ 5 V	
	HLMP-3601				8.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-3650	Yellow (585 nm)			8.0 mcd @ 5 V		10 mA @ 5 V	
	HLMP-3651				8.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-3680	Green (569 nm)			8.0 mcd @ 5 V		12 mA @ 5 V	
	HLMP-3681				8.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-1100	Red (648 nm)	T-1	Tinted Diffused	2.5 mcd @ 5 V	60°	13 mA @ 5 V	3-159
	HLMP-1120			Untinted Diffused				
	HLMP-1600	High Efficiency Red (626 nm)		Tinted Diffused	8.0 mcd @ 5 V		10 mA @ 5 V	
	HLMP-1601				8.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-1620	Yellow (585 nm)			8.0 mcd @ 5 V		10 mA @ 5 V	
	HLMP-1621				8.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-1640	Green (569 nm)			8.0 mcd @ 5 V		12 mA @ 5 V	
	HLMP-1641				8.0 mcd @ 12 V		13 mA @ 12 V	

Emitter Components

Device		Description	Features	Page No.
Package Outline Drawing	Part No.			
	HEMT-6000	700 nm High Intensity Subminiature Emitter	• Visible (Near IR) emission facilitates alignment. • Compatible with most silicon phototransistors and photodiodes.	*
	HEMT-3301	940 nm T-1 3/4 High Radiant Emitter	• Efficiency at Low Currents • Radiated spectrum matches response of silicon photodetectors • Non-saturated, high radiant flux output	*
	HEMT-1001	940 nm T-1 High Radiant Emitter		

* Contact your local HP sales representative for information regarding this product (See section 9).

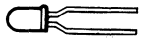
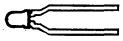
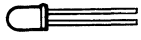
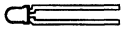
Right Angle and Panel Mount Options

Device		Description	Page No.
Package Outline Drawing	Option No.		
	102	T-1 Rt. Angle, 2 Element Array	3-175
	103	T-1 Rt. Angle, 3 Element Array	
	104	T-1 Rt. Angle, 4 Element Array	
	105	T-1 Rt. Angle, 5 Element Array	
	106	T-1 Rt. Angle, 6 Element Array	
	107	T-1 Rt. Angle, 7 Element Array	
	108	T-1 Rt. Angle, 8 Element Array	

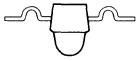
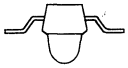
Panel Mount Option

Device		Description	Page No.
Package Outline Drawing	Option No.		
	007	High Profile T-13/4 w/HLMP-0104 Clip & Ring	3-169
	010	T-1$^3/_4$ Rt. Angle, Leads Sheared Even	3-171
	100	T-1$^3/_4$ Rt. Angle, Leads Unsheared Uneven	
	101	T-1 Rt. Angle, Leads Sheared Even	3-173
	010	T-1 Rt. Angle, Leads Unsheared Uneven	
	010	Subminiature Rt. Angle	3-177

Tape and Reel Options

Device		Description	Page No.
Package Outline Drawing	Option No.		
	001	T-1$^3/_4$, 5 mm (0.197 in) Formed Leads, 1300 Lamps per Reel	3-164
		T-1, 5 mm (0.197 in) Formed Leads, 1800 Lamps per Reel	
	002	T-1$^3/_4$, 5 mm (0.197 in) Formed Leads, 1300 Lamps per Reel	
		T-1, 5 mm (0.197 in) Formed Leads, 1800 Lamps per Reel	

Lead Bend Options, Subminiature Lamps

Device		Description	Page No.
Package Outline Drawing	Option No.		
	011	Tape and Reel, 1500 Lamps per Reel	3-179
	012	Gull Wing, Bulk Packaging	
	013	Gull Wing Array, Shipping Tube	
	021	Yoke Lead, Tape and Reel, 1500 Lamps per Reel	
	022	Yoke Lead, Bulk Packaging	
	031	Z-Bend, Tape and Reel, 1500 Lamps per Reel	
	032	Z-Bend, Bulk Packaging	
	1L1	2.54 mm (0.100 in) Rt. Angle Bend, Long Leads	
	1S1	2.54 mm (0.100 in) Rt. Angle Bend, Short Leads	
	2L1	5.08 mm (0.200 in) Rt. Angle Bend, Long Leads	
	2S1	5.08 mm (0.200 in) Rt Angle Bend, Short Leads	

Luminous Intensity and Color Binning Options

Device		Description	Page No.
Package Outline Drawing	Option No.		
	S02	This option provides the selection of lamps from two adjacent luminous intensity categories	3-188
	S20	Devices selected to two color bin categories	
	S22	Devices selected to two IV categories and two Color bin categoreis	

HEWLETT PACKARD

New

High Power AlInGaP Amber and Reddish-Orange Lamps

Technical Data

HLMA-CH00/-CL00
HLMA-DG00/-DH00/-DL00
HLMA-KH00/-KL00
HLMA-QH00/-QL00

Features

- **Outstanding LED Material Efficiency**
- **High Light Output Over a Wide Range of Currents**
- **Low Electrical Power Dissipation**
- **CMOS/MOS Compatible**
- **Colors: 592 nm Amber, 615 nm and 622 nm Reddish-Orange**
- **Variety of Packages Available**

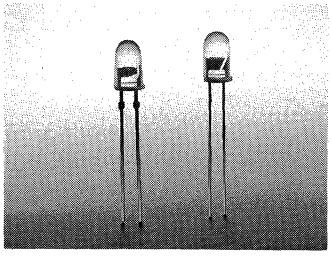
Applications

- **Outdoor Message Boards**
- **Safety Lighting Equipment**
- **Signaling Applications**
- **Emitter for Emitter/ Detector Applications**
- **Changeable Message Signs**
- **Portable Equipment**
- **Medical Equipment**
- **Automotive Lighting**
- **Alternative to Incandescent Lamps**

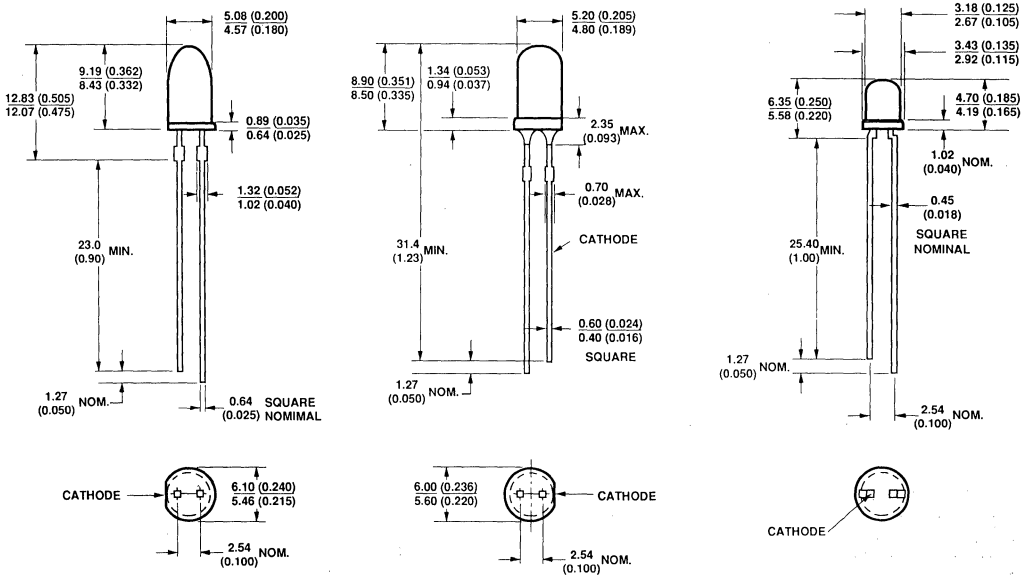
Description

These untinted, non-diffused, solid state lamps utilize the newly developed aluminum indium gallium phosphide (AlInGaP) LED technology. This material has a very high luminous efficiency, capable of producing high light output over a wide range of drive currents.

The 592 nm amber and 615 nm reddish-orange colors are available in both wide (30°) and narrow (7°) viewing angle T-1¾ (5 mm) lamps, as well as T-1 (3 mm) and subminiature packages. In addition, a 622 nm reddish-orange color, 30°, T-1¾ lamp is also available.



Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES).
2. THE LEADS ARE MILD STEEL, SOLDER DIPPED.
3. AN EPOXY MENISCUS MAY EXTEND ABOUT 1 MM (0.040") DOWN THE LEADS, UNLESS OTHERWISE NOTED.

HLMA-CH00/-CL00

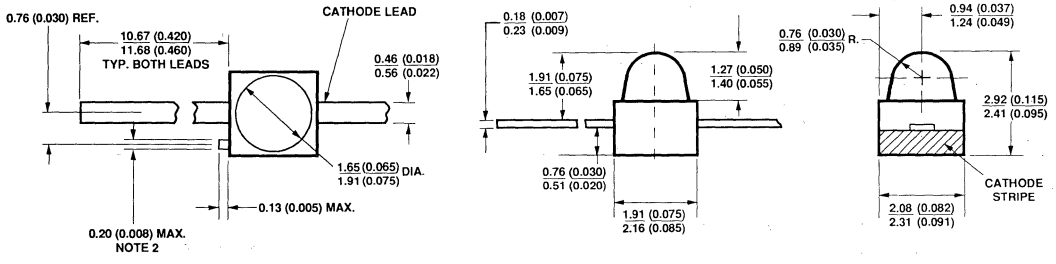
A

HLMA-DG00/-DH00/-DL00

B

HLMA-KH00/-KL00

C



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. PROTRUDING SUPPORT TAB IS CONNECTED TO CATHODE LEAD.
3. FOR RIGHT ANGLE MOUNTING TO A PC BOARD, MOUNT CATHODE DOWN. DO NOT MOUNT ANODE DOWN.

HLMA-QH00/-QL00

D

Device Selection Guide

Package Description	Viewing Angle $2\theta_{1/2}$	Amber λ_d = 592 nm	Reddish-Orange λ_d = 615 nm	Reddish-Orange λ_d = 622 nm	Package Outline
T-1¾ (5 mm), Untinted, Non-diffused	7°	HLMA-CL00	HLMA-CH00	–	A
T-1¾ (5 mm), Untinted, Non-diffused	30°	HLMA-DL00	HLMA-DH00	HLMA-DG00	B
T-1 (3 mm), Untinted, Non-diffused	45°	HLMA-KL00	HLMA-KH00	–	C
Subminiature, Untinted, Non-diffused	28°	HLMA-QL00	HLMA-QH00	–	D

Absolute Maximum Ratings at T_A = 25°C

Parameters	HLMA-CX00	HLMA-DX00	HLMA-KX00	HLMA-QX00	Units
DC Forward Current[1]	50	50	50	30	mA
Peak Forward Current[2]	200	200	200	200	mA
Average Forward Current (at I_{PEAK} = 200 mA, f ≥ 1 KHz)[2]	45	45	45	45	mA
Transient Forward Current[3] (10 μs Pulse)	500	500	500	500	mA
Reverse Voltage (I_R = 100 μA)	5	5	5	5	V
LED Junction Temperature	110	110	110	110	°C
Operating Temperature Range	-40 to +100	-40 to +100	-40 to +100	-40 to +100	°C
Storage Temperature Range	-55 to +100	-55 to +100	-55 to +100	-55 to +100	°C
Soldering Temperature [1.59 mm (0.06 in.) below seating plane]	260°C for 5 seconds	260°C for 5 seconds	260°C for 5 seconds	260°C for 3 seconds	

Notes:
1. Derate linearly as shown in Figure 4.
2. Refer to Figure 5 to establish pulsed operating condition.
3. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bonds.

Electrical Characteristics at $T_A = 25°C$

Part Number HLMA-	Forward Voltage V_F (volts) @ I_F = 20 mA Typ.	Forward Voltage V_F (volts) @ I_F = 20 mA Max.	Reverse Breakdown Voltage V_R (volts) @ I_R = 100 μA Min.	Reverse Breakdown Voltage V_R (volts) @ I_R = 100 μA Typ.	Capacitance C (pF) V_F = 0, f = 1 MHz Typ.	Thermal Resistance $R\theta_{J\text{-}PIN}$ (°C/W) Junction to Cathode Lead	Speed of Response τ_s (ns) Time Constant $e^{-t/\tau s}$ Typ.
CX00	1.9	2.4	5	25	60	210	13
DX00	1.9	2.4	5	25	60	260	13
KX00	1.9	2.4	5	25	60	290	13
QX00	1.9	2.4	5	25	60	170	13

Optical Characteristics at $T_A = 25°C$

Part Number HLMA-	Luminous Intensity I_V (mcd) @ I_F = 20 mA Min.	Luminous Intensity I_V (mcd) @ I_F = 20 mA Typ.	Peak Wavelength λ_p (nm) Typ.	Dominant Wavelength λ_d[1] (nm) Typ.	Viewing Angle $2\theta_{1/2}$[2] (Degrees) Typ.	Luminous Efficacy η_v[3] (lm/w) Typ.
CH00[4]	1000	3000	621	615	7	263
CL00[4]	1000	3000	594	592	7	480
DG00[5]	300	600	630	622	30	197
DH00[5]	300	800	621	615	30	263
DL00[5]	300	1000	594	592	30	480
KH00[5]	35	200	621	615	45	263
KL00[5]	35	200	594	592	45	480
QH00[5]	135	500	621	615	28	263
QL00[5]	135	500	594	592	28	480

Notes:

1. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and represents the perceived color of the device.
2. $\theta_{1/2}$ is the off-axis angle where the luminous intensity is 1/2 the intensity.
3. The radiant intensity, I_e in watts per steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity and η_v is the luminous efficacy in lumens/watt.
4. The luminous intensity, I_V, is measured at the peak of the spatial radiation pattern which may not be aligned with the mechanical axis of the lamp package.
5. The luminous intensity, I_v, is measured on the mechanical axis of the lamp package. The actual peak of the spatial radiation pattern may not be aligned with this axis.

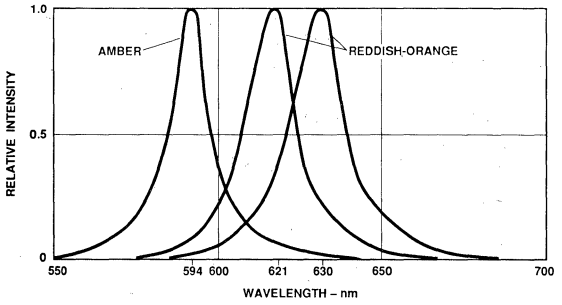


Figure 1. Relative Intensity vs. Wavelength.

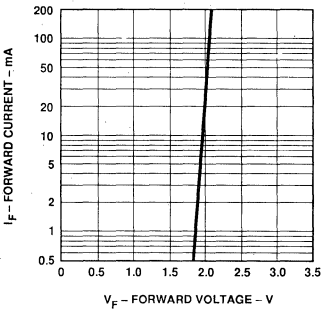


Figure 2. Forward Current vs. Forward Voltage.

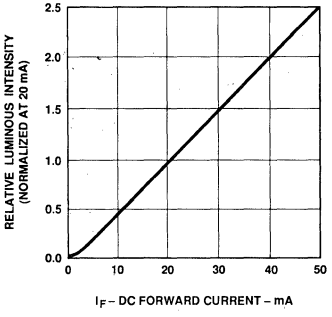


Figure 3. Relative Luminous Intensity vs. Forward Current.

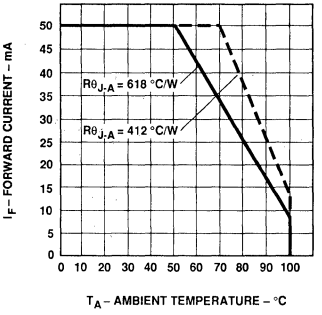


Figure 4. Maximum Forward Current vs. Ambient Temperature. Derating Based on T_J Max = 110°C.

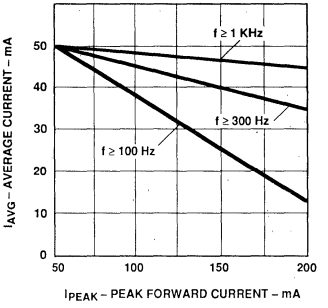


Figure 5. Maximum Average Current vs. Peak Forward Current.

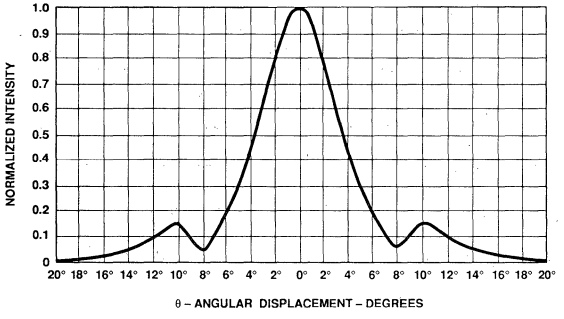


Figure 6. Normalized Luminous Intensity vs. Angular Displacement, HLMA-CH00/-CL00.

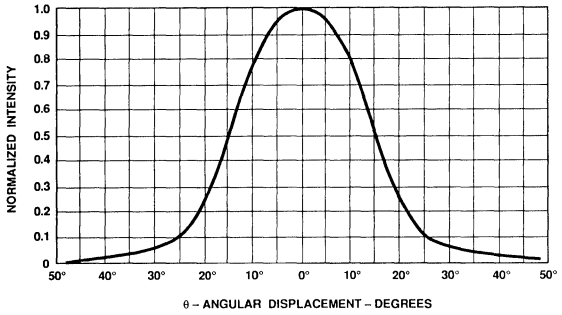


Figure 7. Normalized Luminous Intensity vs. Angular Displacement, HLMA-DG00/-DH00/-DL00.

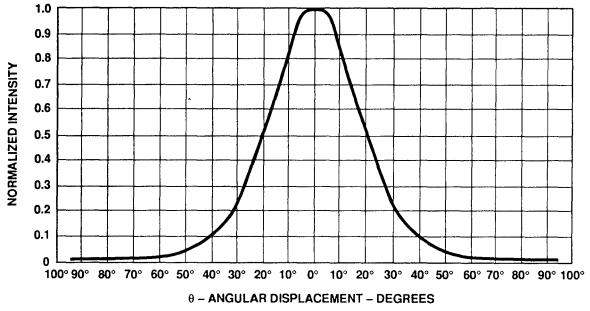


Figure 8. Normalized Luminous Intensity vs. Angular Displacement, HLMA-KH00/-KL00.

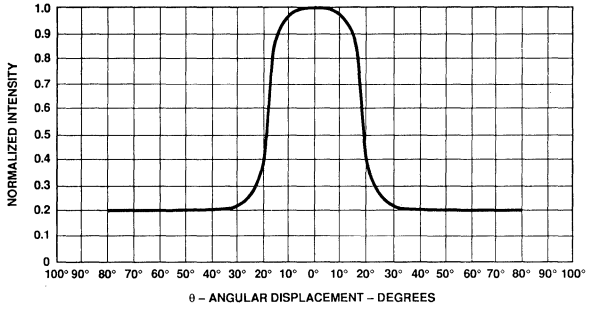


Figure 9. Normalized Luminous Intensity vs. Angular Displacement, HLMA-QH00/-QL00.

HEWLETT PACKARD

New

High Power T-4 (13.3 mm) AlInGaP Amber Lamp

Technical Data

HLMA-BL00

Features

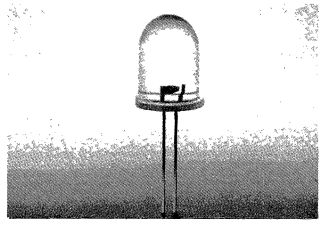
- **15.0 Candelas at 20 mA**
- **Outstanding LED Material Efficiency**
- **High Light Output Over a Wide Range of Currents**
- **3° Viewing Angle**
- **Low Electrical Power Dissipation**
- **CMOS/MOS Compatible**
- **Color: 592 nm Amber**

Applications

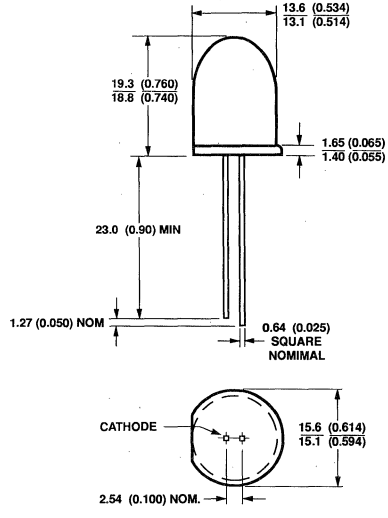
- **Power Signaling**
- **Emitter for Emitter/ Detector Applications**
- **Bright Ambient Lighting Conditions**
- **Replacement for Laser Diodes and Low Power Lasers**
- **Alternative to Incandescent Lamps**

Description

This untinted, nondiffused, solid state lamp utilizes the newly developed aluminum indium gallium phosphide (AlInGaP) LED technology. This material has a very high luminous efficiency, capable of producing high light output over a wide range of drive currents. The color is 592 nm amber. The lamp package incorporates an advanced optical design that produces an extremely high peak intensity within a very narrow viewing angle of 3 degrees.



Package Dimensions



Notes:

1. All dimensions are in millimetres (inches).
2. The leads are mild steel, solder dipped.
3. An epoxy meniscus may extend about 1 mm (0.040") down the leads.

Axial Luminous Intensity, Total Flux, Color, and Viewing Angle @ 25°C

Luminous Intensity I_v (cd) @ 20 mA[1] Min.	Luminous Intensity I_v (cd) @ 20 mA[1] Typ.	Radiant Intensity I_e (mW/sr) @ 20 mA Typ.	ϕ_v Total Flux (mlm) @ 20 mA[2] Typ.	Color Dominant, Wavelength λ_d nm[3] Typ.	Viewing Angle 2 $\theta_{1/2}$ Degrees[4] Typ.
6.5	15.0	31.2	300	Amber 592	3

Notes:
1. The luminous intensity, I_v, is measured at the peak of the spatial radiation pattern which may not be aligned with the geometric axis of the lamp package.
2. ϕ_v is the total luminous flux output as measured with an integrating sphere.
3. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and represents the color of the device.
4. $\theta_{1/2}$ is the off-axis angle where the luminous intensity is 1/2 the peak intensity.

Absolute Maximum Ratings

Parameters		Units
DC Forward Current[1]	50	mA
Peak Forward Current[2]	200	mA
Average Forward Current (at I_{PEAK} = 200 mA, f ≥ 1 KHz)[2]	45	mA
Transient Forward Current[3] (10 μs Pulse)	500	mA
Reverse Voltage (I_R = 100 μA)	5	V
LED Junction Temperature	110	°C
Operating Temperature Range	-40 to +100	°C
Storage Temperature Range	-55 to +100	°C
Soldering Temperature [1.59 mm (0.06 in.) below seating plane]	260°C for 3 seconds	

Notes:
1. Derate linearly as shown in Figure 4.
2. Refer to Figure 5 to establish pulsed operating conditions.
3. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bonds.

Electrical/Optical Characteristics at T_A = 25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Forward Voltage	V_F		1.9	2.4	V	I_F = 20 mA
Reverse Voltage	V_R	5	25		V	I_R = 100 μA
Peak Wavelength	λ_{PEAK}		595		nm	
Spectral Line Halfwidth	$\Delta\lambda_{1/2}$		15		nm	
Speed of Response	τ_s		13		ns	Exponential Time Constant, e^{-t/τ_s}
Capacitance	C		60		pF	V_F = 0, f = 1 MHz
Thermal Resistance	$R\theta_{J\text{-}PIN}$		210		°C/W	Junction-to-Cathode Lead
Luminous Efficacy[1]	η_v		480		lm/W	

Note:
1. The radiant intensity I_e, in watts per steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is luminous efficacy in lumens/watt.

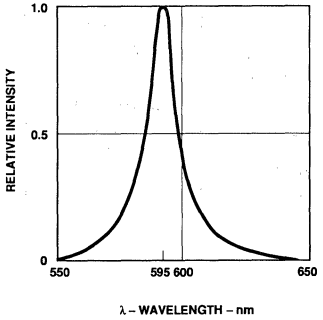


Figure 1. Relative Intensity vs. Wavelength.

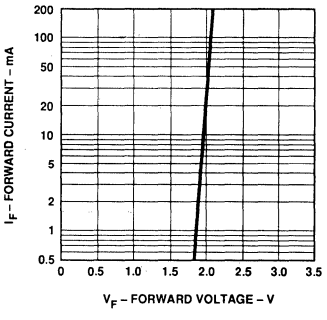


Figure 2. Forward Current vs. Forward Voltage.

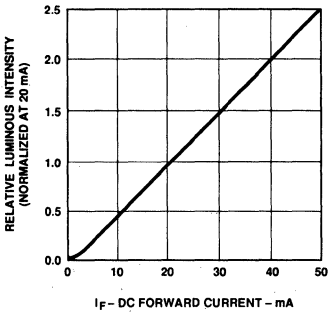


Figure 3. Relative Luminous Intensity vs. Forward Current.

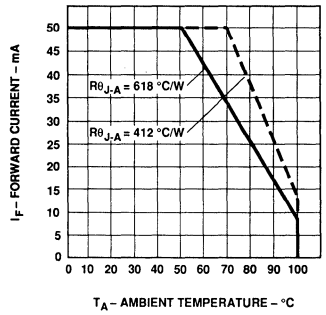


Figure 4. Maximum Forward Current vs. Ambient Temperature. Derating Based on T_J Max = 110°C.

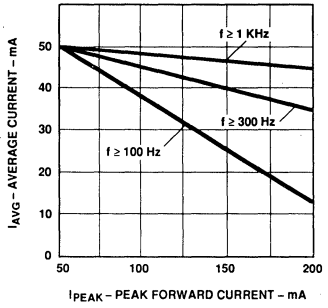


Figure 5. Normalized Luminous Intensity vs. Angular Displacement.

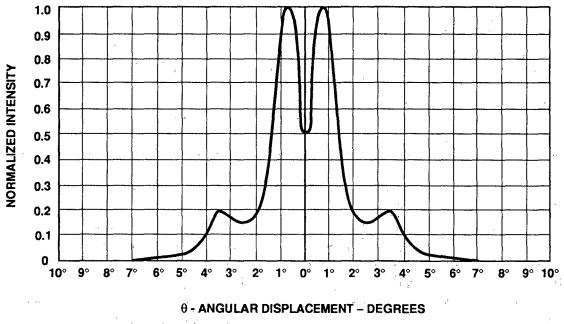


Figure 6. Normalized Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

New

Blue T-1¾ LED Lamps

Technical Data

HLMP-DB00
HLMP-DB15

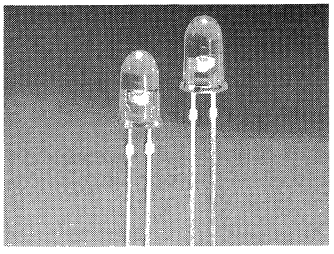
SOLID STATE LAMPS

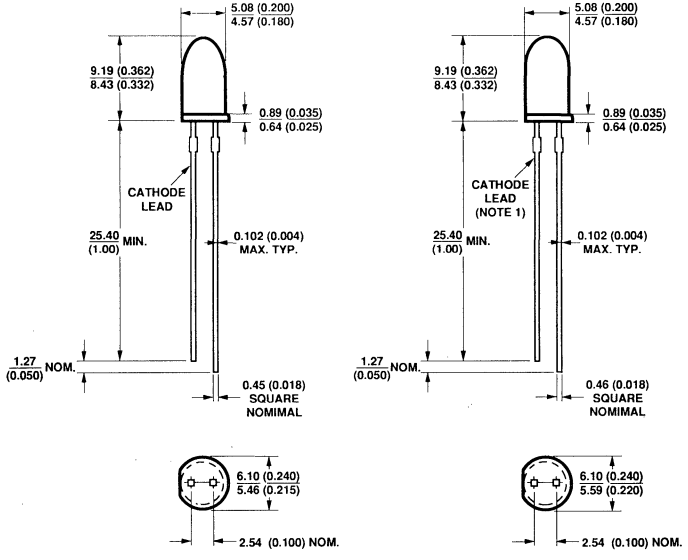
Features

- **Silicon Carbide Technology**
- **481 nm Blue Color**
- **Viewing Angles: Narrow and Wide**
- **CMOS/MOS Compatible**

Applications

- **Moving Message Signs**
- **Automotive Interior Lighting**
- **Front Panel Status Indicator**
- **Medical Instrumentation**





NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. THE LEADS ARE MILD STEEL, SOLDER DIPPED.
3. AN EPOXY MENISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.

HLMP-DB15 HLMP-DB00

Description

These untinted diffused and nondiffused T-1¾ LED blue lamps utilize single crystal silicon carbide technology. The color is an 80% saturated blue with a dominant wavelength of 481 nanometers. The HLMP-DB00 is a 38 degree cone angle diffused lamp for use in moving message panel signs or as a front panel indicator. The HLMP-DB15 is a nondiffused lamp with a 15 degree cone angle that may be used for backlighting legends or as a blue wavelength emitter.

Absolute Maximum Ratings at T_A = 25°C

DC Forward Current[1] ..... 50 mA
Peak Forward Current[2] ..... 100 mA
Average Forward Current (@ I_{PEAK} = 100 mA, f = 1 KHz)[2] ..... 40 mA
LED Junction Temperature ..... 110°C
Transient Forward Current (10 μs Pulse)[3] ..... 500 mA
Reverse Voltage (I_R = 100 μA) ..... 5 V
Operating Temperature Range ..... -55 to 85°C
Storage Temperature Range ..... -55 to 100°C
Lead Soldering Temperature (1.59 mm [0.063 in.] from body) ..... 260°C for 5 seconds

Notes:
1. Derate linearly as shown in Figure 5.
2. Refer to Figure 6 to establish pulsed operating conditions.
3. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bonds. Operating the device at peak currents above the absolute Maximum Peak Forward Current is not recommended.

Optical Characteristics at T_A = 25°C

Part Number HLMP-	Luminous Intensity I_v (Mcd) @ I_F 20 mA[1] Min.	Typ.	Radiant Intensity I_e (μW/sr) @ 20 mA Typ.	Total Flux ϕ_v (mlm) @ 20 mA[2] Typ.	Color, Dominant Wavelength λ_d[3] (nm) Typ.	Peak Wavelength λ_{PEAK} (nm) Typ.	Viewing Angle 2 $\theta_{1/2}$ Degrees[4] Typ.
DB00	1.6	3.0	23.1	2.0	481	468	38
DB15	6.0	12.0	93.3	2.0	481	468	15

Notes:
1. The luminous intensity, I_v, is measured at the peak of the spatial radiation pattern which may not be aligned with the geometric axis of the lamp package.
2. ϕ_v is the total luminous flux output as measured with an integrating sphere.
3. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and represents the color of the device.
4. $\theta_{1/2}$ is the off-axis angle where the luminous intensity is 1/2 the peak intensity.

Electrical Characteristics at T_A = 25°C

Forward Voltage V_F (Volts) @ I_F 20 mA Typ.	Max.	Reverse Breakdown V_R (Volts) @ I_R = 100 μA Min.	Typ.	Speed of Response τ_s (ns) Time Constant e^{-t/τ_s} Typ.	Capacitance C (pF) V_F = 0, f = 1 MHz Typ.	Thermal Resistance $R\theta_{J\text{-}PIN}$ (°C/W) Junction to Cathode Lead
3.0	3.6	5.0	45.0	500	29	260

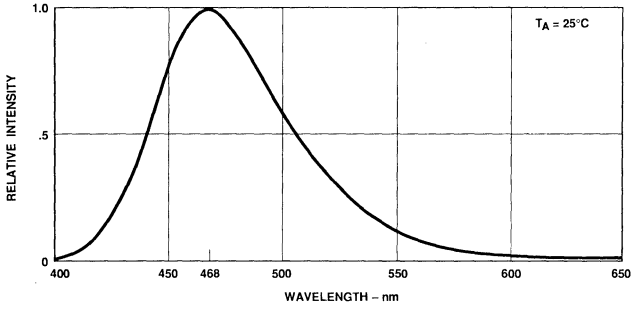


Figure 1. Relative Intensity vs. Wavelength.

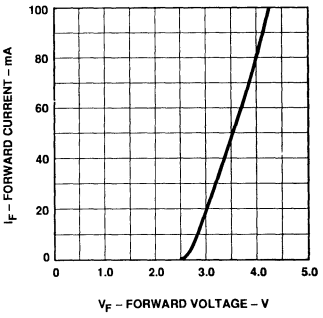


Figure 2. Forward Current vs. Forward Voltage.

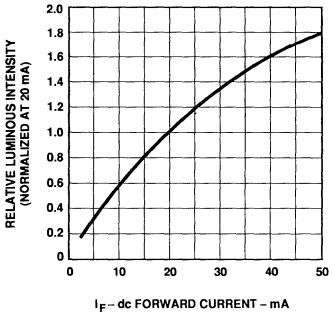


Figure 3. Relative Luminous Intensity vs. dc Forward Current.

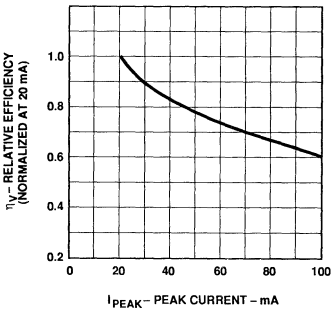


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

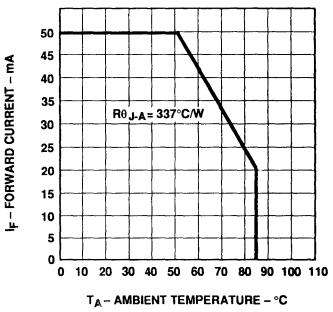


Figure 5. Maximum dc Current vs. Ambient Temperature. Derating Based on T_J Max. = 110°C.

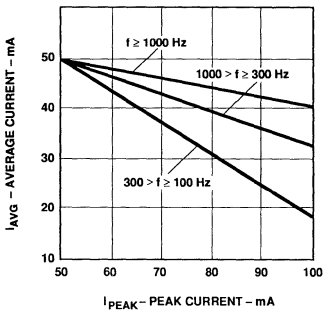


Figure 6. Time Average Current vs. Peak Forward Current as a Function of Pulsed Refresh Rate, f (Hz).

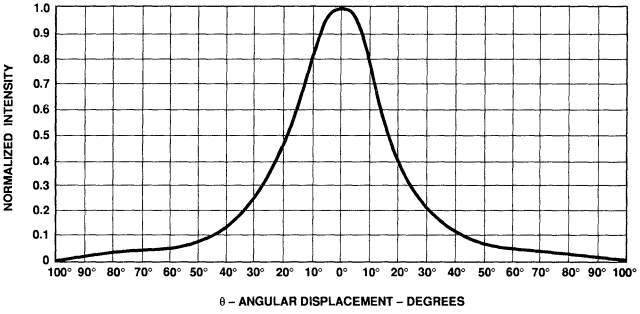


Figure 7. Normalized Luminous Intensity vs. Angular Displacement, HLMP-DB00.

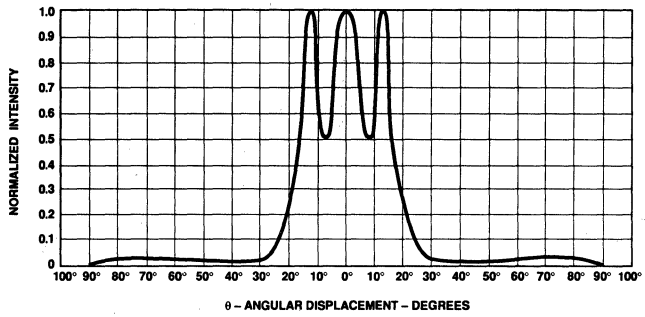


Figure 8. Normalized Luminous Intensity vs. Angular Displacement HLMP-DB15.

HEWLETT PACKARD

New

Surface Mount Chip LEDs

Technical Data

HSMX-C650 Series
HSMX-C670 Series
HSMF-C655

Features

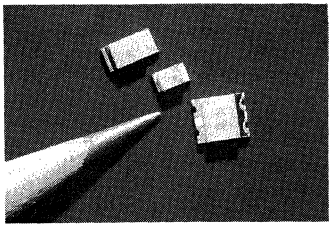
- **Small Size**
- **Industry Standard Footprint**
- **Low Profile**
- **Tinted, Diffused Optics**
- **Compatible with IR Solder Process**
- **Five Colors and Bicolor Available**
- **Available in 8 mm Tape on 7" (178 mm) Diameter Reels**

Applications

- **Push-Button Backlighting**
- **LCD Backlighting**
- **Symbol Backlighting**
- **Front Panel Indicator**

Description

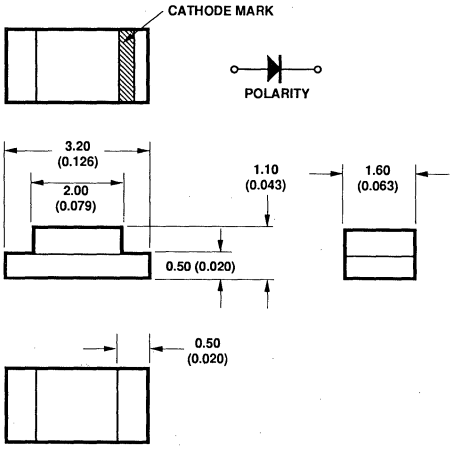
These single and bicolor LEDs are designed in an industry standard package for ease of handling and use. Five different LED colors are available in two compact, low profile, single color packages. The 3.2 x 1.6 mm is an excellent all around package, and the small 2.0 x 1.25 mm package is designed for applications where space is limited. The single color LEDs have tinted diffused optics. The bicolor package is untinted, diffused.



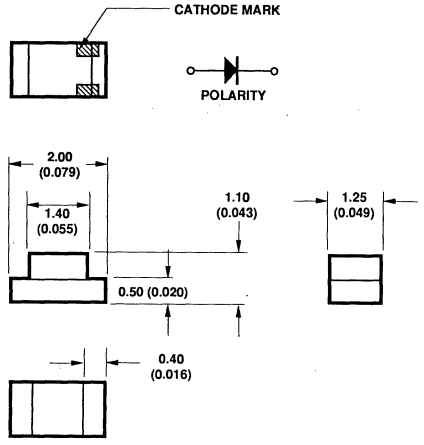
The small size, low 1.1 mm profile and wide viewing angle make these LEDs excellent for backlighting applications and front panel illumination. They are compatible with IR reflow soldering processes.

Device Selection Guide

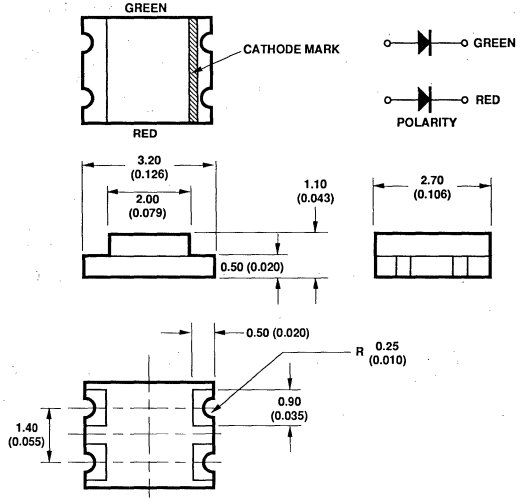
Footprint (mm)	DH AlGaAs Red	High Efficiency Red	Orange	Yellow	Green	Bicolor (Red-Green)
3.20 x 1.60	HSMH-C650	HSMS-C650	HSMD-C650	HSMY-C650	HSMG-C650	
2.00 x 1.25	HSMH-C670	HSMS-C670	HSMD-C670	HSMY-C670	HSMG-C670	
3.20 x 2.70						HSMF-C655



HSMX-C650 Series



HSMX-C670 Series



HSMF-C655

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS (INCHES).
2. TOLERANCE, UNLESS OTHERWISE SPECIFIED, ± 0.1 mm (± 0.004 INCH).

Absolute Maximum Ratings at T_A = 25°C

Parameter	HSMX-C650 HSMF-C655	HSMX-C670	Units
DC Forward Current[1]	25	20	mA
Power Dissipation	65	50	mW
Reverse Voltage (I_R = 100 μA)	5	5	V
LED Junction Temperature	95	95	°C
Operating Temperature Range	-25 to +80	-25 to +80	°C
Storage Temperature Range	-30 to +85	-30 to +85	°C
Soldering Temperature	See IR soldering profile, Figure 6		

Notes:
1. Derate linearly as shown in Figure 4 for temperatures above 25°C.

Optical Characteristics at T_A = 25°C

Part Number	Color	Luminous Intensity I_V (mcd) @ I_F 20 mA[1] Min.	Typ.	Peak Wavelength λ_{peak} (nm) Typ.	Color, Dominant Wavelength λ_d[2] (nm) Typ.	Viewing Angle 2 $\theta_{1/2}$ Degrees[3] Typ.
HSMH-C650 HSMH-C670	DH AlGaAs Red	6.3	16.0	650	639	155
HSMS-C650 HSMS-C670	High Efficiency Red	1.6	5.0	639	626	155
HSMD-C650 HSMD-C670	Orange	1.6	4.0	606	604	155
HSMY-C650 HSMY-C670	Yellow	1.6	5.0	584	586	155
HSMG-C650 HSMG-C670	Green	4.0	9.0	566	571	155
HSMF-C655	High Efficiency Red	1.6	5.0	639	626	155
	Green	4.0	9.0	566	571	155

Notes:
1. The luminous intensity, I_V, is measured at the peak of the spatial radiation pattern which may not be aligned with the mechanical axis of the lamp package.
2. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and represents the perceived color of the device.
3. $\theta_{1/2}$ is the off-axis angle where the luminous intensity is 1/2 the peak intensity.
4. Chip LEDs are supplied in 8 mm embossed tape on 178 mm (7 in.) diameter reels, with 3000 devices per reel. Minimum order quantity and order incremenets are in quantity of reels only.

Electrical Characteristics at $T_A = 25°C$

Part Number	Color	Forward Voltage V_F (Volts) @ $I_F = 20$ mA Typ.	Max.	Reverse Breakdown V_R (Volts) @ $I_R = 100\,\mu A$ Min.	Capacitance C (pF) $V_F = 0$, f = 1 MHz Typ.	Thermal Resistance $R\theta_{J\text{-}PIN}$ (°C/W)
HSMH-C650 HSMH-C670	DH AlGaAs Red	1.8	2.2	5	46	460 300
HSMS-C650 HSMS-C670	High Efficiency Red	1.9	2.6	5	4.0	400 250
HSMD-C650 HSMD-C670	Orange	2.1	2.6	5	4.0	400 250
HSMY-C650 HSMY-C670	Yellow	2.1	2.6	5	3.0	400 250
HSMG-C650 HSMG-C670	Green	2.2	3.0	5	8.0	400 250
HSMF-C655	High Efficiency Red	1.9	2.6	5	3.7	325
	Green	2.2	3.0	5	6.3	325

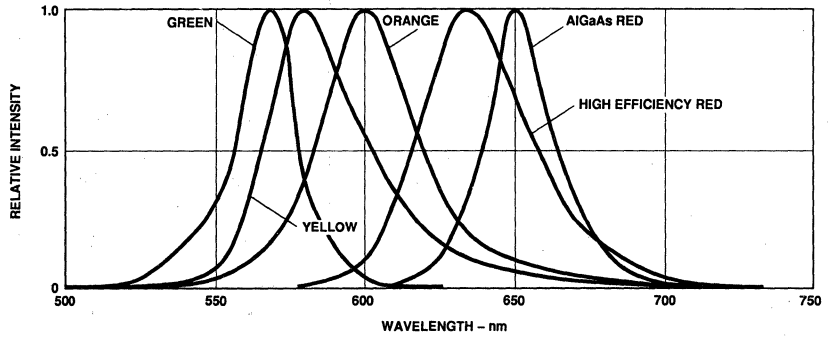


Figure 1. Relative Intensity vs. Wavelength.

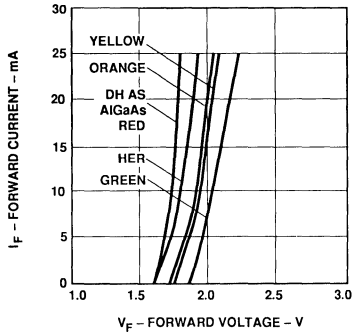


Figure 2. Forward Current vs. Forward Voltage.

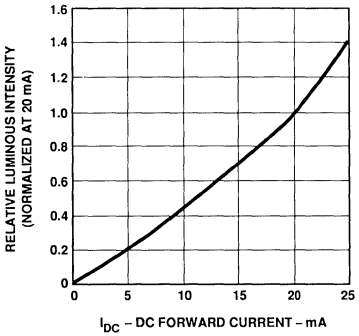


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

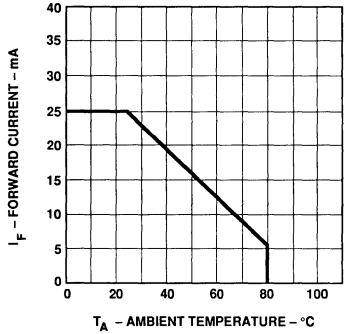


Figure 4. Maximum DC Current vs. Ambient Temperature.

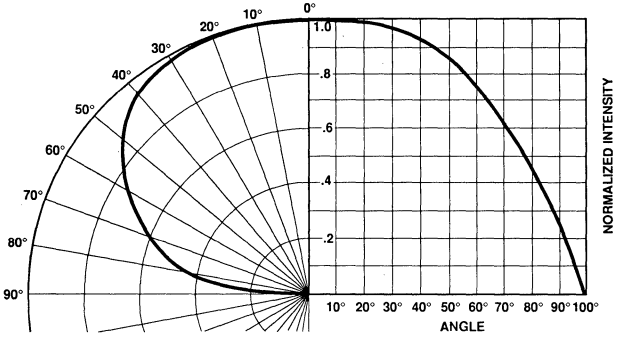


Figure 5. Intensity vs. Angle.

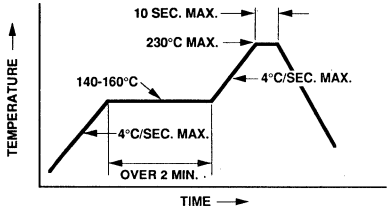


Figure 6. Recommended IR Reflow Soldering Profile.

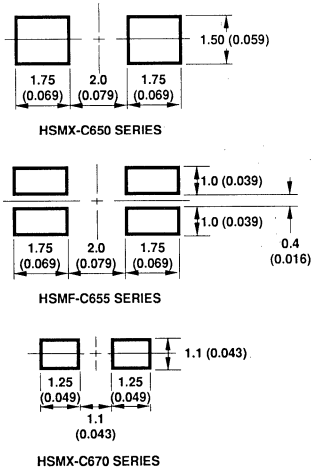


Figure 7. Recommended Solder Patterns.

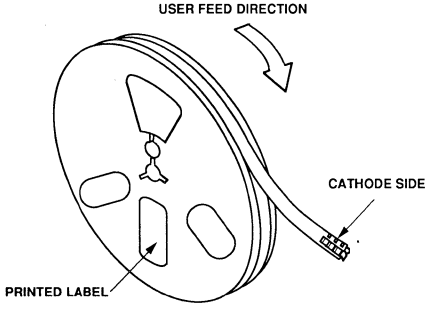


Figure 8. Reeling Orientation.

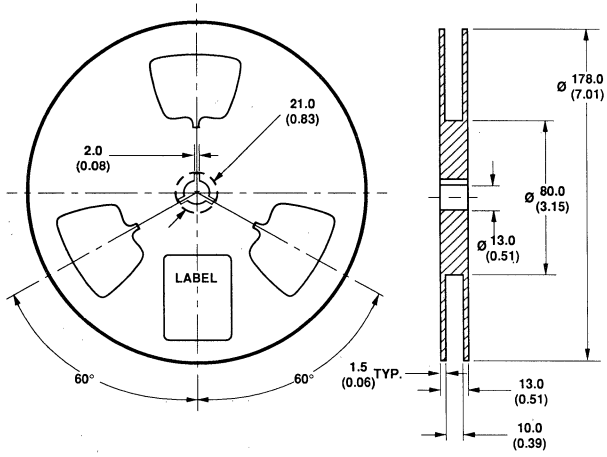


Figure 9. Reel Dimensions.

NOTE:
ALL DIMENSIONS IN
MILLIMETERS (INCHES).

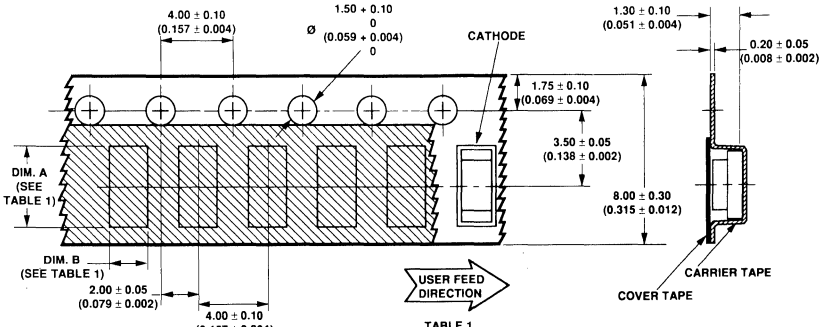


TABLE 1
DIMENSIONS IN MILLIMETERS (INCHES)

PART NUMBER	DIM. A ± 0.10 (0.004)	DIM. B ± 0.10 (0.004)
HSMX-C650 SERIES	3.75 (0.148)	2.10 (0.083)
HSMX-C670 SERIES	2.40 (0.094)	1.60 (0.064)
HSMF-C655	3.70 (0.146)	3.15 (0.124)

Figure 10. Tape Dimensions.

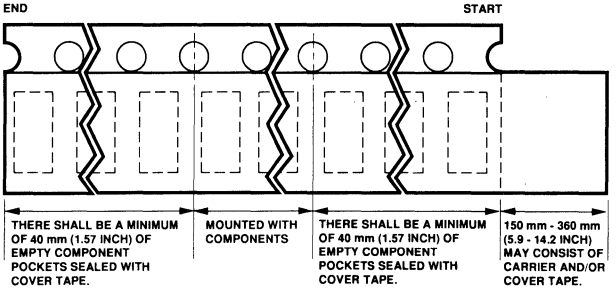


Figure 11. Tape Leader and Trailer Dimensions.

Convective IR Reflow Soldering

For information on IR reflow soldering, refer to Application Note 1060, *Surface Mounting SMI LED Indicator Components.*

HEWLETT PACKARD

High Power T-1¾ (5 mm) TS AlGaAs Red Lamps

Technical Data

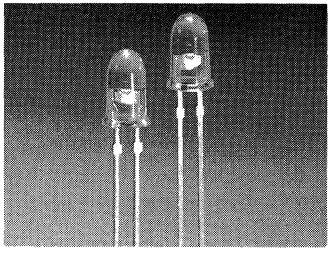
HLMP-810X Series
New **HLMP-C100**
New **HLMP-C110**

Features

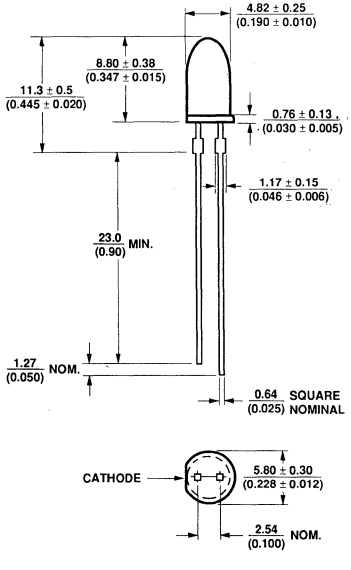
- **Exceptional Brightness**
- **Outstanding LED Material Efficiency**
- **High Light Output Over a Wide Range of Drive Currents**
- **Viewing Angle: Narrow or Wide**
- **Low Forward Voltage**
- **Low Power Dissipation**
- **CMOS/MOS Compatible**
- **Red Color**

Description

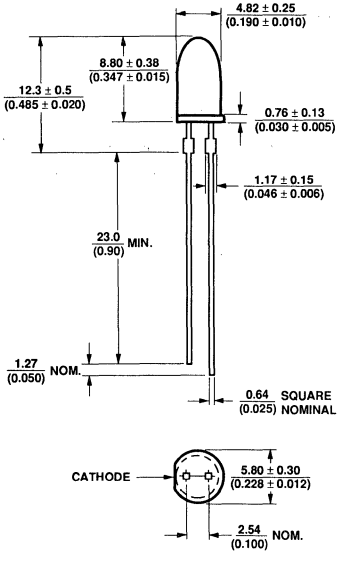
These untinted, nondiffused solid state lamps utilize a highly optimized LED material, transparent substrate aluminum gallium arsenide, TS AlGaAs. This material has outstanding light output efficiency over a wide range of currents, and has superior high current capability compared to most other LED materials. The LED color is red at a dominant wavelength of 644 nm.



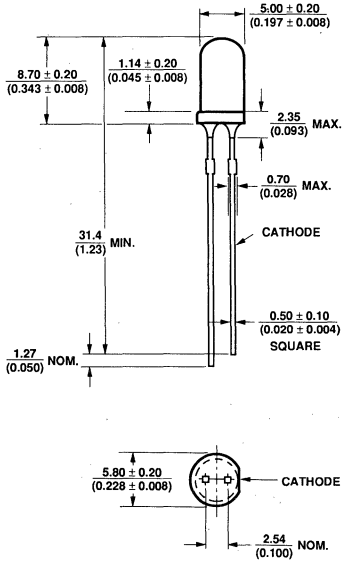
Package Dimensions



HLMP-8100



HLMP-8102/-8103



HLMP-C100/-C110

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS/INCHES.
2. THE LEADS ARE MILD STEEL, SOLDER DIPPED.
3. AN EPOXY MENISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS, UNLESS OTHERWISE NOTED.

Axial Luminous Intensity and Viewing Angle at $T_A = 25°C$

Part Number HLMP-	Minimum Intensity (cd) @ 20 mA	Typical Intensity (cd) @ 20 mA	Maximum Intensity (cd) @ 20 mA	Typical Radiant Intensity (mW/sr) @ 20 mA	$2\theta_{1/2}$[1] Degrees
8103	2.0	3.0	5.8	35.3	7
8102	1.4	2.0	4.0	23.5	7
8100	0.29	1.0	–	11.8	19
C100	0.29	0.75	–	8.8	30
C110	0.20	0.40	–	4.7	40

Note:
1. $\theta_{1/2}$ is the off axis angle from optical centerline where the luminous intensity is 1/2 the on-axis value.

Absolute Maximum Ratings at $T_A = 25°C$

Peak Forward Current[2] ..... 300 mA
Average Forward Current (@ I_{PEAK} = 300 mA) [1,2] ..... 30 mA
DC Forward Current[3] ..... 50 mA
Power Dissipation ..... 100 mW
Reverse Voltage (I_R=100 μA) ..... 5 V
Transient Forward Current (10 μs Pulse)[4] ..... 500 mA
Operating Temperature Range ..... -55 to +100°C
Storage Temperature Range ..... -55 to +100°C
LED Junction Temperature ..... 110°C
Lead Soldering Temperature
[1.6 mm (0.063 in.) from body] ..... 260°C for 5 seconds

Notes:
1. Maximum I_{AVG} at f = 1 kHz, DF = 10%.
2. Refer to Figure 6 to establish pulsed operating conditions.
3. Derate linearly as shown in Figure 5.
4. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bonds. It is not recommended that the device be operated at peak currents above the Absolute Maximum Peak Forward Current.

Electrical/Optical Characteristics at T_A = 25°C

Description	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Forward Voltage	V_F		1.85	2.4	V	I_F = 20 mA
Reverse Voltage	V_R	5.0	20.0		V	I_R = 100 μA
Peak Wavelength	λ_{PEAK}		654		nm	
Dominant Wavelength[1]	λ_d		644		nm	
Spectral Line Halfwidth	$\Delta\lambda 1/2$		18		nm	
Speed of Response	τ_S		45		ns	Exponential Time Constant, e^{-t/τ_s}
Capacitance	C		20		pF	V_F = 0, f = 1 MHz
Thermal Resistance HLMP-810X	$R\theta_{J\text{-}PIN}$		210		°C/W	Junction-to-Anode Lead
HLMP-C1X0			237			
Luminous Efficacy[2]	η_v		85		lm/W	

Notes:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the color of the device.
2. The radiant intensity, I_e, in watts per steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is luminous efficacy in lumens/watt.
3. The approximate total luminous flux output within a cone angle of 2θ about the optical axis may be obtained from the following formula:
   $\phi_V 2(\theta) = [\phi_V(\theta)/I_V(0)]I_V$;
   Where: $\phi_V(\theta)/I_V(0)$ is obtained from Figure 7.

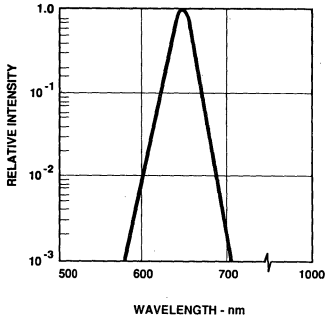


Figure 1. Relative Intensity vs. Wavelength.

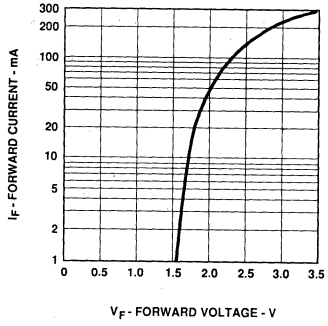


Figure 2. Forward Current vs. Forward Voltage.

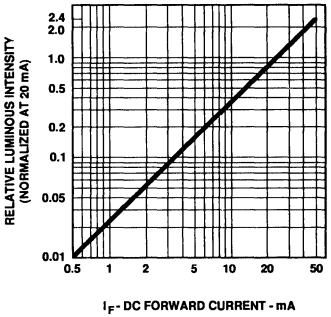


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

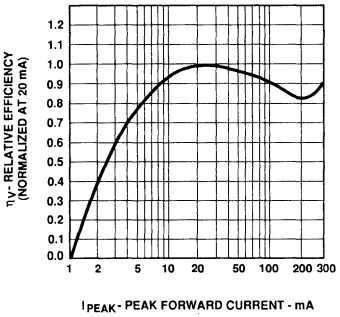


Figure 4. Relative Efficiency vs. Peak Forward Current.

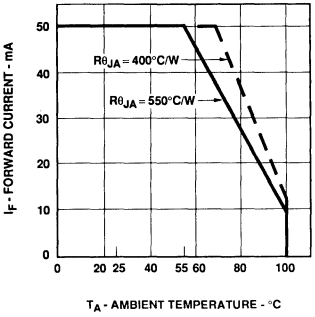


Figure 5. Maximum Forward DC Current vs. Ambient Temperature. Derating Based on T_JMAX = 110°C.

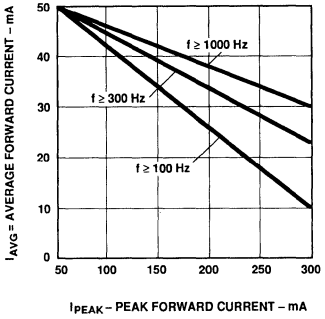


Figure 6. Maximum Average Current vs. Peak Forward Current.

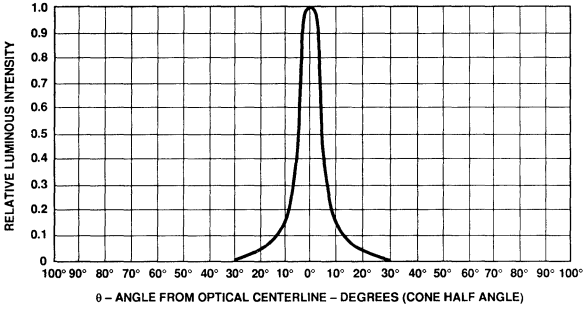


Figure 7. Relative Luminous Intensity vs. Angular Displacement. HLMP-8103 and HLMP-8102.

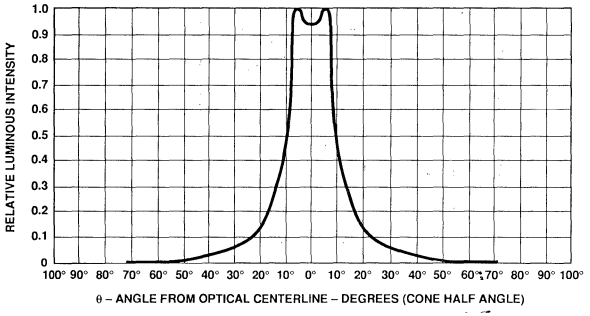


Figure 8. Relative Luminous Intensity vs. Angular Displacement. HLMP-8100.

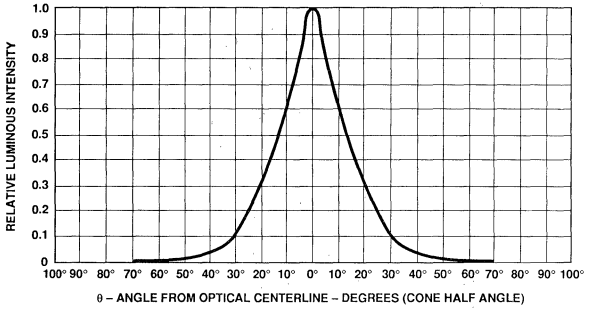


Figure 9. Relative Luminous Intensity vs. Angular Displacement. HLMP-C100.

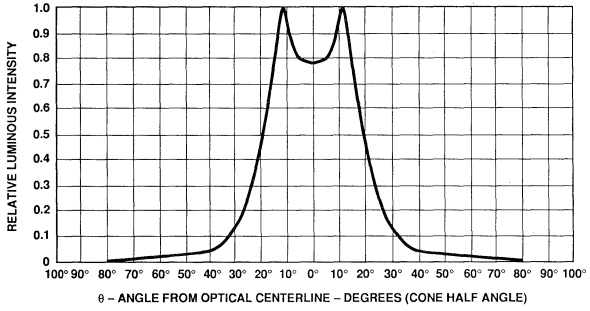


Figure 10. Relative Luminous Intensity vs. Angular Displacement. HLMP-C110.

HEWLETT PACKARD

Double Heterojunction AlGaAs High Intensity Red LED Lamps

Technical Data

HLMP-D101/D105
HLMP-K101/K105
HLMP-Q101

SOLID STATE LAMPS

Features

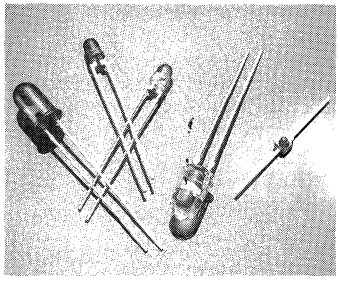
- Exceptional Brightness
- Wide Viewing Angle
- Outstanding Material Efficiency
- Low Forward Voltage
- CMOS/MOS Compatible
- TTL Compatible
- Deep Red Color

Applications

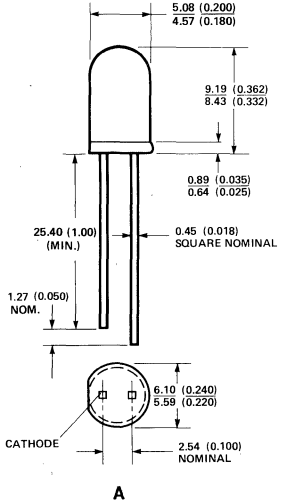
- Bright Ambient Lighting Conditions
- Moving Message Panels
- Portable Equipment
- General Use

Description

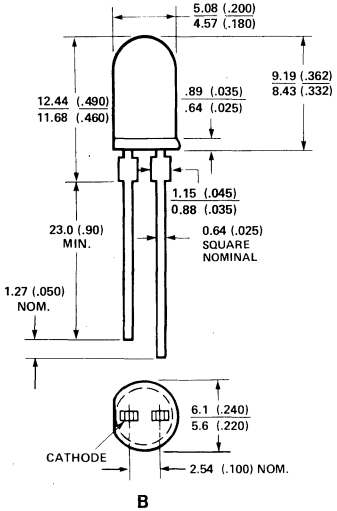
These solid state LED lamps utilize newly developed double heterojunction (DH) AlGaAs/GaAs material technology. This LED material has outstanding light output efficiency over a wide range of drive currents. The color is deep red at the dominant wavelength of 637 nanometres. These lamps may be DC or pulse driven to achieve desired light output.



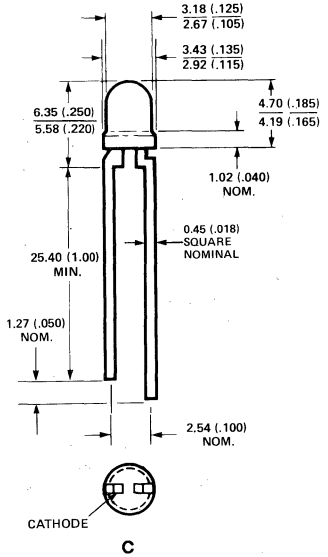
Package Dimensions



A



B

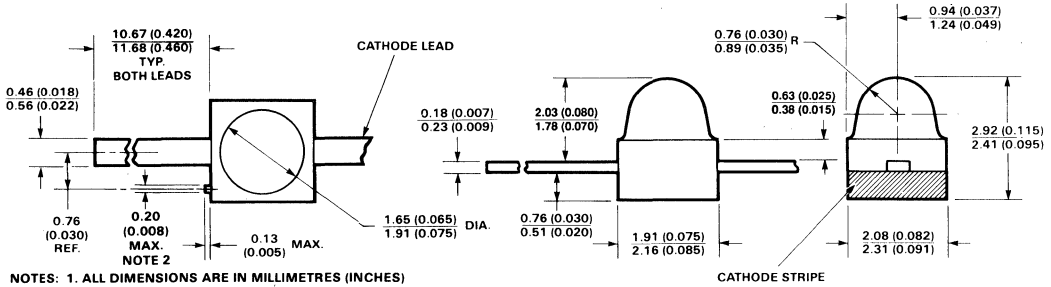


C

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MINISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.

(Continued on next page.)

Package Dimensions



NOTES: 1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)
2. PROTRUDING SUPPORT TAB IS CONNECTED TO CATHODE LEAD.

Axial Luminous Intensity and Viewing Angle @ 25°C

Part Number HLMP-	Package Description	I_v (mcd) @ 20 mA		$2\theta_{1/2}$[1] Degrees	Package Outline
		Min.	Typ.		
D101	T-1¾ Red Tinted Diffused	35	70	65	A
D105	T-1¾ Red Untinted, Non-diffused	100	240	24	B
K101	T-1 Red Tinted Diffused	22	45	60	C
K105	T-1 Red Untinted Non-diffused	35	65	45	C
Q101	Subminiature Red Tinted Diffused	20	45	70	D

Note:
1. $\theta_{1/2}$ is the off axis angle from lamp centerline where the luminous intensity is ½ the on-axis value.

Absolute Maximum Ratings at $T_A = 25°C$

Peak Forward Current[1,2] ..... 300 mA
Average Forward Current[2] ..... 20 mA
DC Current[3] ..... 30 mA
Power Dissipation ..... 87 mW
Reverse Voltage (I_R = 100 μA) ..... 5 V
Transient Forward Current (10 μs Pulse)[4] ..... 500 mA
LED Junction Temperature ..... 110°C
Operating Temperature Range ..... -20 to +100°C
Storage Temperature Range ..... -55 to +100°C
Lead Soldering Temperature [1.6 mm (0.063 in.) from body] ..... 260°C for 5 seconds

Notes:
1. Maximum I_{PEAK} at f = 1 kHz, DF = 6.7%.
2. Refer to Figure 6 to establish pulsed operating conditions.
3. Derate linearly as shown in Figure 5.
4. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bonds. It is not recommended that the device be operated at peak currents beyond the Absolute Maximum Peak Forward Current.

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	Min.	Typ.	Max.	Unit	Test Condition
V_F	Forward Voltage		1.8	2.2	V	$I_F = 20$ mA
V_R	Reverse Breakdown Voltage	5.0	15.0		V	$I_R = 100\ \mu A$
λ_p	Peak Wavelength		645		nm	Measurement at Peak
λ_d	Dominant Wavelength		637		nm	Note 1
$\Delta\lambda 1/2$	Spectral Line Halfwidth		20		nm	
τ_S	Speed of Response		30		ns	Exponential Time Constant, e^{-t/T_S}
C	Capacitance		30		pF	$V_F = 0$, f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance		260[3] 210[4] 290[5] 170[6]		°C/W	Junction to Cathode Lead
η_V	Luminous Efficacy		80		Im/W	Note 2

Notes:

1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the color of the device.
2. The radiant intensity, I_e, in watts per steradian, may be found from the equation $I_e = I_v/\eta_V$, where I_V is the luminous intensity in candelas and η_V is luminous efficacy in lumens/watt.
3. HLMP-D101.
4. HLMP-D105.
5. HLMP-K101/-K105.
6. HLMP-Q101.

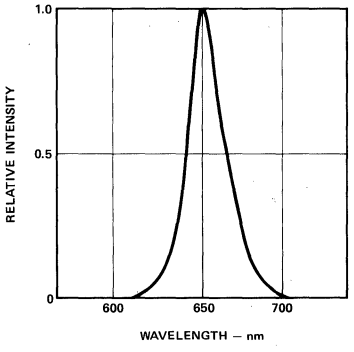


Figure 1. Relative Intensity vs. Wavelength.

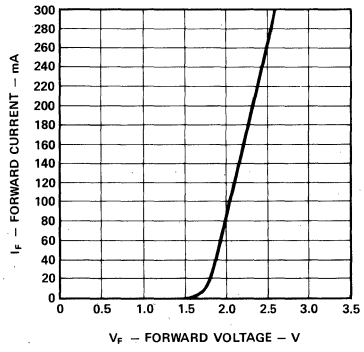


Figure 2. Forward Current vs. Forward Voltage.

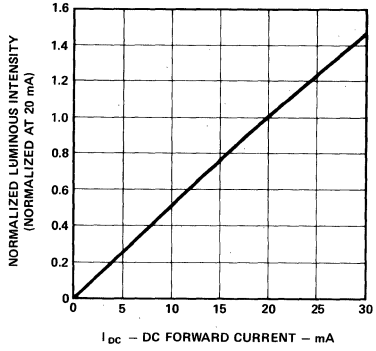


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

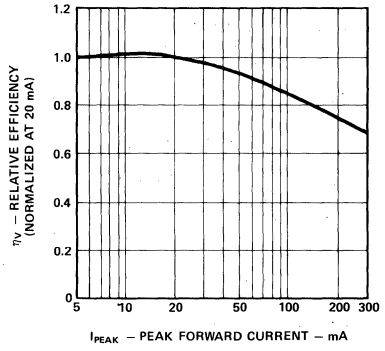


Figure 4. Relative Efficiency vs. Peak Forward Current.

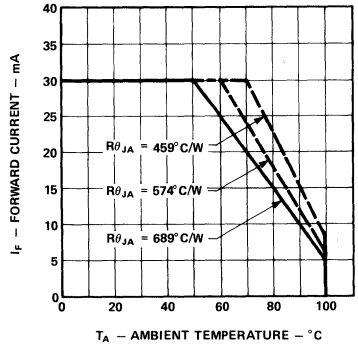


Figure 5. Maximum Forward DC Current vs. Ambient Temperature. Derating Based on T_J MAX = 110°C.

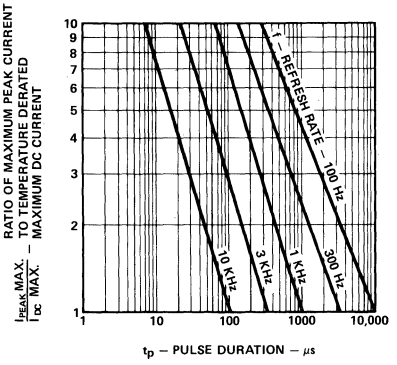


Figure 6. Maximum Tolerable Peak Current vs. Peak Duration (I_{PEAK} MAX Determined from Temperature Derated I_{DC} MAX).

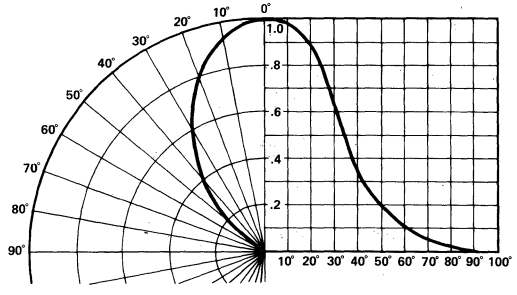


Figure 7. Relative Luminous Intensity vs. Angular Displacement. HLMP-D101.

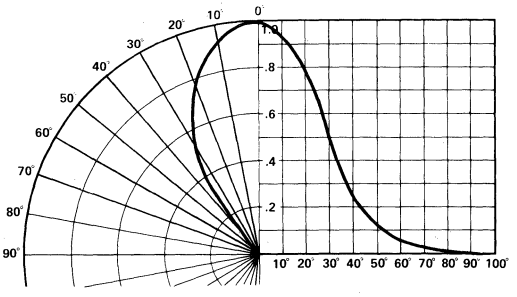


Figure 8. Relative Luminous Intensity vs. Angular Displacement. HLMP-K101

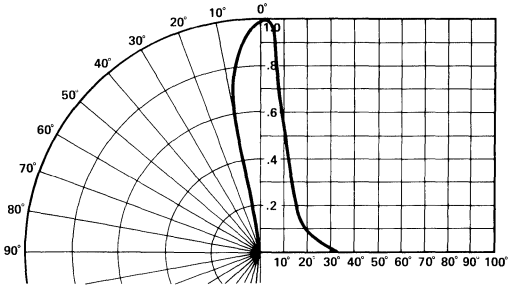


Figure 9. Relative Luminous Intensity vs. Angular Displacement. HLMP-D105.

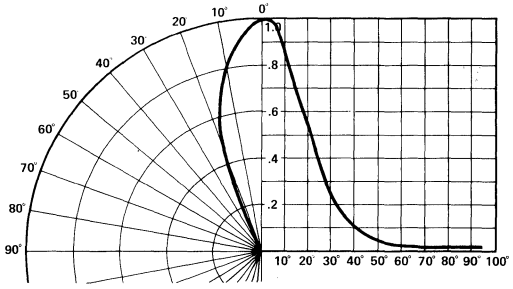


Figure 10. Relative Luminous Intensity vs. Angular Displacement. HLMP-K105.

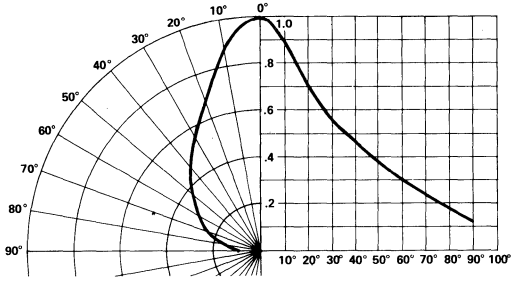


Figure 11. Relative Luminous Intensity vs. Angular Displacement for Subminiature Lamp.

HEWLETT PACKARD

Double Heterojunction AlGaAs Low Current Red LED Lamps

Technical Data

HLMP-D150/D155
HLMP-K150/K155
HLMP-Q150

Features

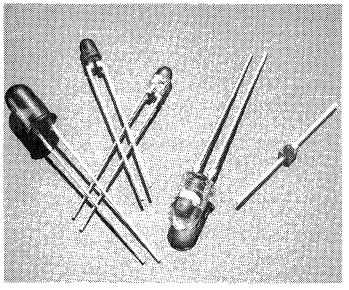
- **Minimum Luminous Intensity Specified at 1 mA**
- **High Light Output at Low Currents**
- **Wide Viewing Angle**
- **Outstanding Material Efficiency**
- **Low Power/Low Forward Voltage**
- **CMOS/MOS Compatible**
- **TTL Compatible**
- **Deep Red Color**

Applications

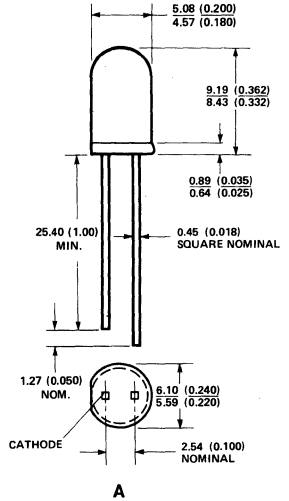
- **Low Power Circuits**
- **Battery Powered Equipment**
- **Telecommunication Indicators**

Description

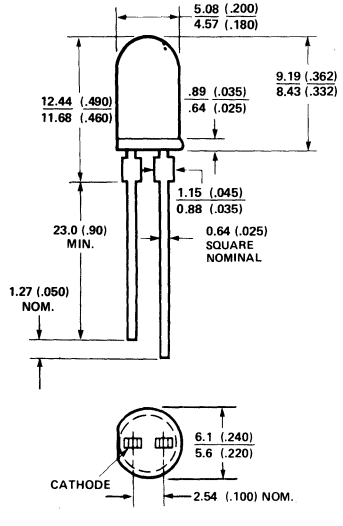
These solid state LED lamps utilize newly developed double heterojunction (DH) AlGaAs/GaAs material technology. This LED material has outstanding light output efficiency at very low drive currents. The color is deep red at the dominant wavelength of 637 nanometres. These lamps are ideally suited for use in applications where high light output is required with minimum power output.



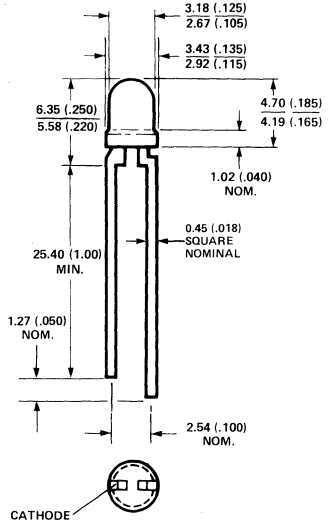
Package Dimensions



A



B

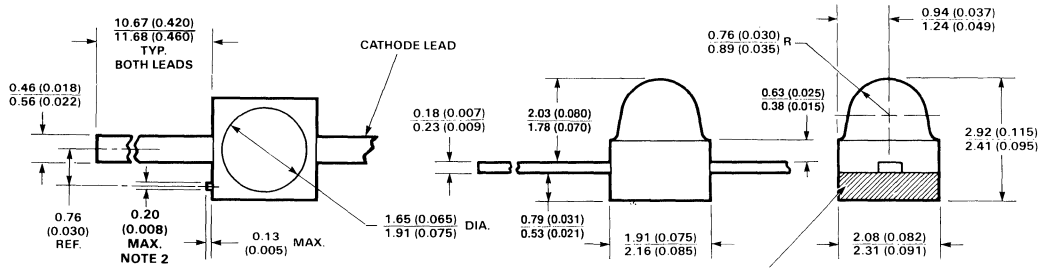


C

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MINISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.

(Continued on next page.)

Package Dimensions



NOTES: 1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)
2. PROTRUDING SUPPORT TAB IS CONNECTED TO CATHODE LEAD.

Axial Luminous Intensity and Viewing Angle @ 25°C

Part Number HLMP-	Package Description	I_v (mcd) @ 1 mA DC		$2\theta 1/2$[1] Degrees	Package Outline
		Min.	Typ.		
D150	T-1¾ Red Tinted Diffused	1.2	3	65	A
D155	T-1¾ Red Untinted, Non-diffused	5	10	24	B
K150	T-1 Red Tinted Diffused	1.2	2	60	C
K155	T-1 Red Untinted Non-diffused	2	3	45	C
Q150	Subminiature Red Tinted Diffused	1	1.8	70	D

Note:
1. $\theta 1/2$ is the off axis angle from lamp centerline where the luminous intensity is ½ the on-axis value.

Absolute Maximum Ratings at T_A = 25°C

Peak Forward Current[1] ..... 300 mA
Average Forward Current ..... 20 mA
DC Current[2] ..... 30 mA
Power Dissipation ..... 87 mW
Reverse Voltage (I_R = 100 μA) ..... 5 V
Transient Forward Current (10 μs Pulse)[3] ..... 500 mA
LED Junction Temperature ..... 110°C
Operating Temperature Range ..... -20 to +100°C
Storage Temperature Range ..... -55 to +100°C
Lead Soldering Temperature [1.6 mm (0.063 in.) from body] ..... 260°C for 5 seconds

Notes:
1. Maximum I_{PEAK} at f = 1 kHz, DF = 6.7%.
2. Derate linearly as shown in Figure 4.
3. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bonds. It is not recommended that the device be operated at peak currents beyond the Absolute Maximum Peak Forward Current.

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	Min.	Typ.	Max.	Unit	Test Condition
V_F	Forward Voltage		1.6	1.8	V	$I_F = 1$ mA
V_R	Reverse Breakdown Voltage	5.0	15.0		V	$I_R = 100\ \mu A$
λ_p	Peak Wavelength		645		nm	Measurement at Peak
λ_d	Dominant Wavelength		637		nm	Note 1
$\Delta\lambda 1/2$	Spectral Line Halfwidth		20		nm	
τ_S	Speed of Response		30		ns	Exponential Time Constant, e^{-t/T_S}
C	Capacitance		30		pF	$V_F = 0, f = 1$ MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance		260[3] 210[4] 290[5] 170[6]		°C/W	Junction to Cathode Lead
η_V	Luminous Efficacy		80		Im/W	Note 2

Notes:

1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the color of the device.
2. The radiant intensity, I_e, in watts per steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is luminous efficacy in lumens/watt.
3. HLMP-D150.
4. HLMP-D105.
5. HLMP-K150/-K105.
6. HLMP-Q150.

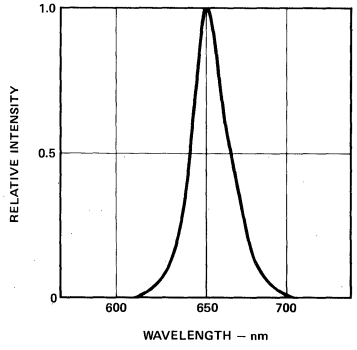


Figure 1. Relative Intensity vs. Wavelength.

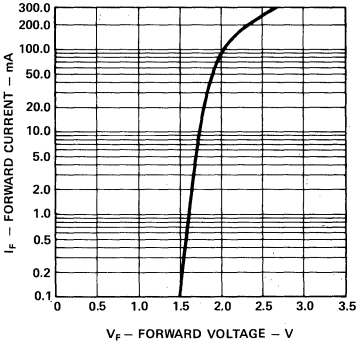


Figure 2. Forward Current vs. Forward Voltage.

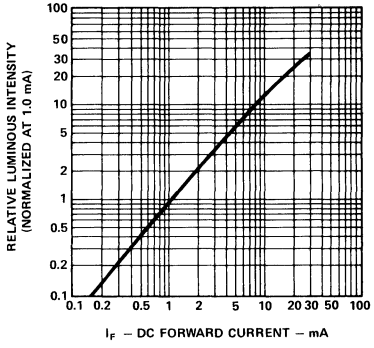


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

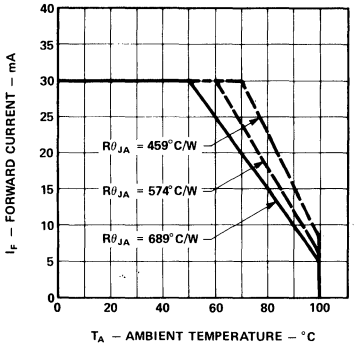


Figure 4. Maximum Forward DC Current vs. Ambient Temperature. Derating Based on T_J Max. = 110°C.

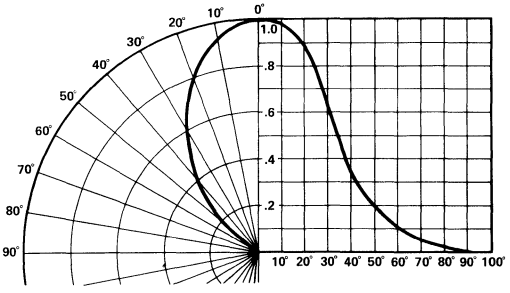


Figure 5. Relative Luminous Intensity vs. Angular Displacement. HLMP-D150.

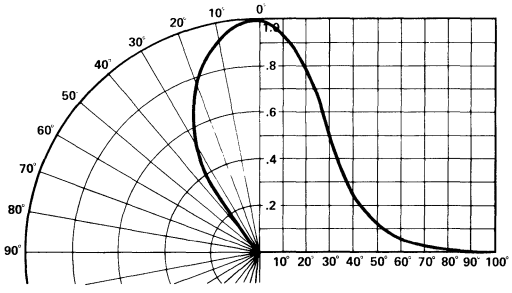


Figure 6. Relative Luminous Intensity vs. Angular Displacement. HLMP-K150.

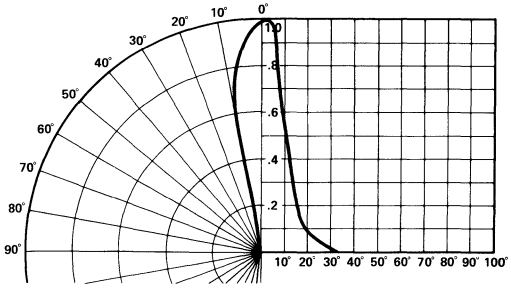


Figure 7. Relative Luminous Intensity vs. Angular Displacement. HLMP-D155.

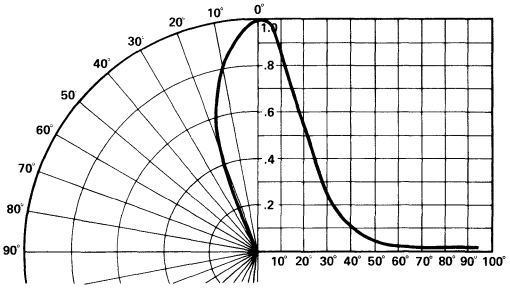


Figure 8. Relative Luminous Intensity vs. Angular Displacement. HLMP-K155.

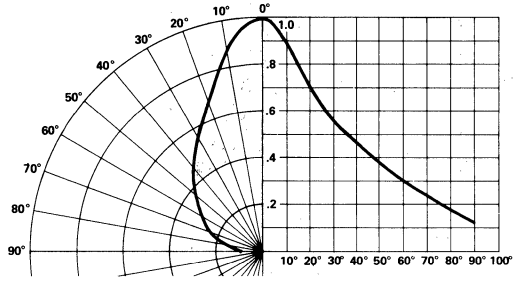


Figure 9. Relative Luminous Intensity vs. Angular Displacement for Subminiature Lamp.

Double Heterojunction AlGaAs Very High Intensity Red LED Lamps T-1¾ (5 mm)

Technical Data

HLMP-4100/4101

Features

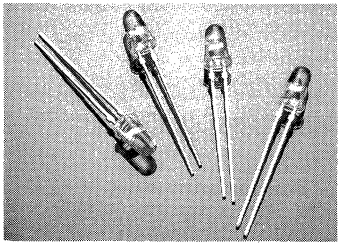
- 1000 mcd at 20 mA
- Very High Intensity at Low Drive Currents
- Narrow Viewing Angle
- Outstanding Material Efficiency
- Low Forward Voltage
- CMOS/MOS Compatible
- TTL Compatible
- Deep Red Color

Applications

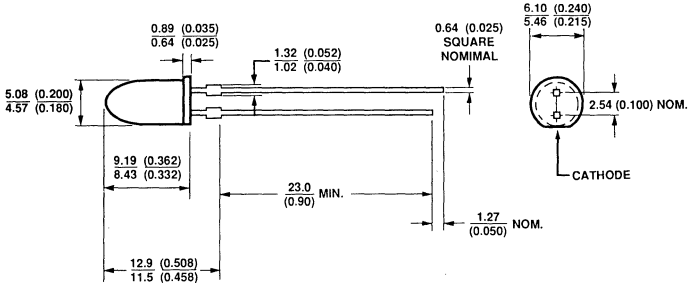
- Bright Ambient Lighting Conditions
- Emitter/Detector and Signaling Applications
- General Use

Description

These solid-state LED lamps utilize newly developed double heterojunction (DH) AlGaAs/GaAs material technology. This LED material has outstanding light output efficiency over a wide range of drive currents. The lamp package has a tapered lens, designed to concentrate the luminous flux into a narrow radiation pattern to achieve a very high intensity. The LED color is deep red at the dominant wavelength of 637 nanometres. These lamps may be DC or pulse driven to achieve desired light output.



Package Dimensions



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.

Luminous Intensity @ 25°C

P/N HLMP-	Package Description	I_V (mcd) @ 20 mA DC Min.	Typ.	2θ1/2 [1] Degrees
4100	T-1¾ Red Untinted, Non-diffused	500	750	8
4101		700	1000	

Note:
1. θ1/2 is the angle from optical centerline where the luminous intensity is 1/2 the optical centerline value.

Absolute Maximum Ratings at T_A = 25°C

Parameter	Maximum Rating	Units
Peak Forward Current[1,2]	300	mA
Average Forward Current[2]	20	mA
DC Current[3]	30	mA
Power Dissipation	87	mW
Reverse Voltage (I_R = 100 μA)	5	V
Transient Forward Current (10 μs Pulse)[4]	500	mA
LED Junction Temperature	110	°C
Operating Temperature Range	-20 to +100	°C
Storage Temperature Range	-55 to +100	°C
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 5 seconds	

Notes:
1. Maximum I_{PEAK} at f = 1 kHz, DF = 6.7%.
2. Refer to Figure 6 to establish pulsed operating conditions.
3. Derate linearly as shown in Figure 5.
4. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bonds. It is not recommended that the device be operated at peak currents beyond the Absolute Maximum Peak Forward Current.

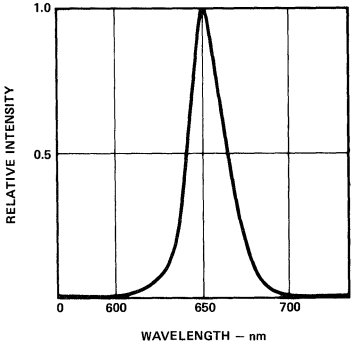


Figure 1. Relative Intensity vs. Wavelength.

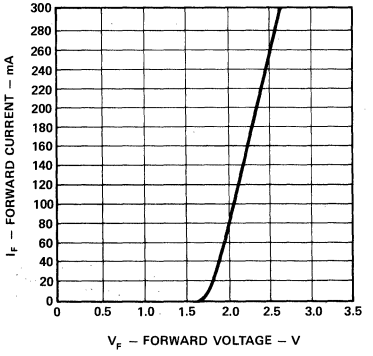


Figure 2. Forward Current vs. Forward Voltage.

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	Min.	Typ.	Max.	Unit	Test Condition
V_F	Forward Voltage		1.8	2.2	V	20 mA
V_R	Reverse Breakdown Voltage	5.0	15.0		V	$I_R = 100\ \mu A$
λ_p	Peak Wavelength		645		nm	Measurement at Peak
λ_d	Dominant Wavelength		637		nm	Note 1
$\Delta\lambda 1/2$	Spectral Line Halfwidth		20		nm	
τ_S	Speed of Response		30		ns	Exponential Time Constant, $e^{-t/s}$
C	Capacitance		30		pF	$V_F = 0, f = 1$ MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance		210		°C/W	Junction to Cathode Lead
η_V	Luminous Efficacy		80		Im/W	Note 2

Notes:

1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the color of the device.
2. The radiant intensity, I_e, in watts per steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is luminous efficacy in lumens/watt.
3. The approximate total luminous flux output within a cone angle of 2θ about the optical axis, $\phi_V(2\theta)$, may be obtained from the following formula:

   $\phi_V(2\theta) = [\phi_V(\theta)/I_V(0)]I_V$;

   Where: $\phi_V(\theta)/I_V(0)$ is obtained from Figure 7.

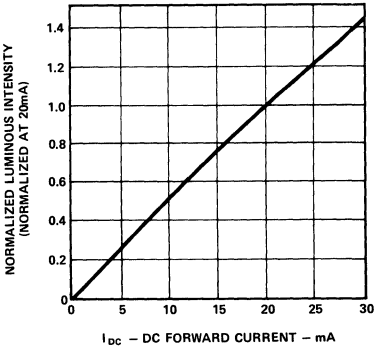


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

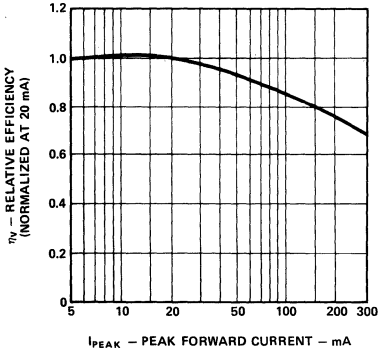


Figure 4. Relative Efficiency vs. Peak Forward Current.

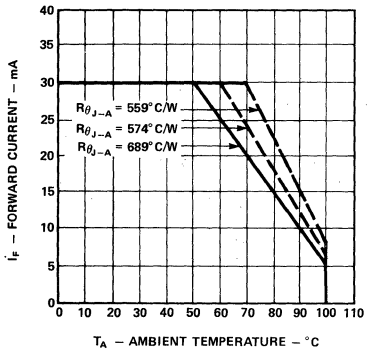


Figure 5. Maximum Forward DC Current vs. Ambient Temperature. Derating Based on T_J MAX = 110°C.

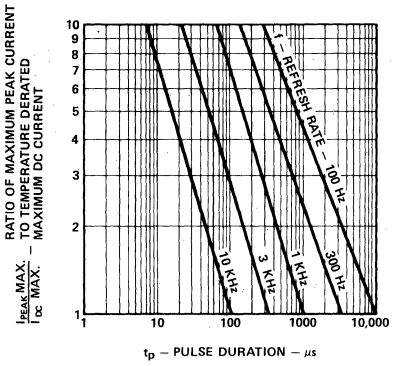


Figure 6. Maximum Tolerable Peak Current vs. Peak Duration (I_{PEAK} MAX Determined from Temperature Derated I_{DC} MAX).

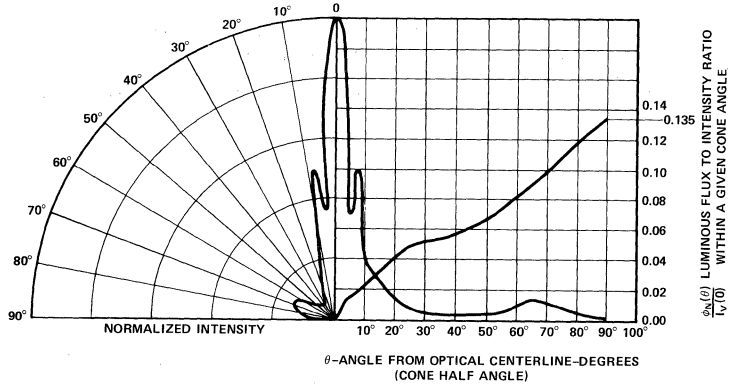


Figure 7. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

New

T-1¾ Super Ultra-Bright LED Lamps

Technical Data

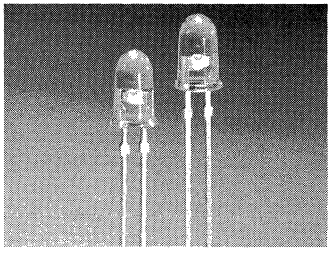
HLMP-8115 HLMP-8109
HLMP-8205 HLMP-8209
HLMP-8305 HLMP-8309
HLMP-8405 HLMP-8409
HLMP-8505 HLMP-8509
HLMP-8605

Features

- **Very High Intensity**
- **Narrow and Medium Viewing Angles**
- **Untinted, Nondiffused Lens**
- **Choice of Five Colors**
- **Sturdy Leads with Seating Plane Tabs**

Description

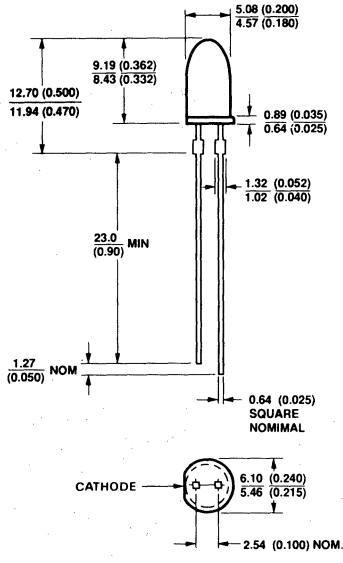
These untinted, nondiffused solid state lamps are designed with special internal optics to give a very high luminous intensity within a well defined viewing angle. The LED materials used within these devices is specifically grown to assure the high light output performance these lamps provide.



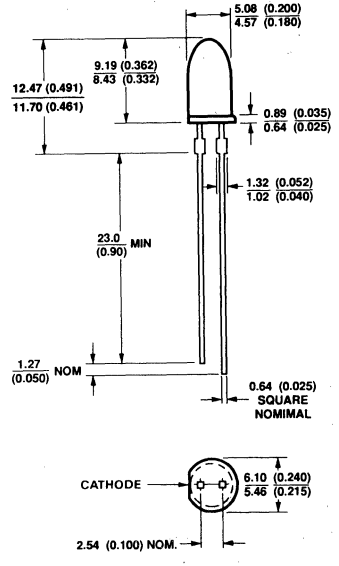
Device Selection Guide

LED Color	Part Number	Typical Luminous Intensity (mcd @ 20 mA dc)	$2\theta_{1/2}$ Viewing Angle
DH AS AlGaAs	HLMP-8115 HLMP-8109	1200 500	15° 25°
High Efficiency Red	HLMP-8205 HLMP-8209	350 260	15° 25°
Yellow	HLMP-8305 HLMP-8309	350 260	15° 25°
Orange	HLMP-8405 HLMP-8409	350 260	15° 25°
High Performance Green	HLMP-8505 HLMP-8509	350 260	15° 25°
Emerald Green	HLMP-8605	75	15°

Package Dimensions



HLMP-8115/-8X05



HLMP-8X09

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. THE LEADS ARE MILD STEEL, SOLDER DIPPED.
3. AN EPOXY MENISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	DH AS AlGaAs Red	High Efficiency Red and Orange	Yellow	High Performance Green/Emerald Green	Units
DC Forward Current[1]	30	30	20	30	mA
Peak Forward Current[2]	300	90	60	90	mA
Average Forward Current[2]	20	25	20	25	mA
Transient Forward Current[3] (10 μs Pulse)	500	500	500	500	mA
Reverse Voltage (I_R = 100 μA)	5	5	5	5	V
LED Junction Temperature	110	110	110	110	°C
Operating Temperature Range	-20 to +100	-55 to +100		-20 to +100	°C
Storage Temperature Range	-55 to +100				°C
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 5 seconds				

Notes:
1. See Figure 5 for maximum current derating vs. ambient temperature.
2. See Figure 6 for maximum peak current vs. pulse duration and allowable duty factor.
3. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bond. Do not operate these lamps at peak currents above the Absolute Maximum Peak Forward Current.

Electrical/Optical Characteristics $T_A = 25°C$

DH AS AlGaAs HLMP-8115/8109

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity HLMP-8115 HLMP-8109	I_v	 500 200	 1200 500		mcd	$I_F = 20$ mA
Forward Voltage	V_F		1.8	2.2	V	$I_F = 20$ mA
Reverse Breakdown Voltage	V_R	5.0	15.0		V	$I_R = 100\ \mu A$
Included Angle Between Half Intensity Points HLMP-8115 HLMP-8109	$2\theta_{1/2}$		 15 25		Deg.	
Total Luminous Flux	ϕ_d		120		mlm	$I_F = 20$ mA
Peak Wavelength	λ_{PEAK}		645		nm	Measured at Peak
Dominant Wavelength[1]	λ_d		637		nm	
Spectral Line Half Width	$\Delta\lambda_{1/2}$		20		nm	
Speed of Response	τ_s		30		ns	Time Constant, e^{-t/τ_s}
Capacitance	C		30		pF	$V_F = 0$, f = 1 MHz
Thermal Resistance	$R\theta_{J\text{-}LEAD}$		210		°C/W	LED Junction-to-Cathode Lead
Luminous Efficacy[2]	η_v		80		lm/W	

High Efficiency Red HLMP-8205/8209

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity HLMP-8205 HLMP-8209	I_v	 200 100	 350 260		mcd	$I_F = 20$ mA
Forward Voltage	V_F		1.9	2.6	V	$I_F = 20$ mA
Reverse Breakdown Voltage	V_R	5.0	30.0		V	$I_R = 100\ \mu A$
Included Angle Between Half Intensity Points HLMP-8205 HLMP-8209	$2\theta_{1/2}$		 15 25		Deg.	
Total Luminous Flux	ϕ_v		45		mlm	$I_F = 20$ mA
Peak Wavelength	λ_{PEAK}		635		nm	Measured at Peak
Dominant Wavelength[1]	λ_d		626		nm	
Spectral Line Half Width	$\Delta\lambda_{1/2}$		40		nm	
Speed of Response	τ_s		90		ns	
Capacitance	C		11		pF	$V_F = 0$, f = 1 MHz
Thermal Resistance	$R\theta_{J\text{-}LEAD}$		210		°C/W	LED Junction-to-Cathode Lead
Luminous Efficacy[2]	η_v		145		lm/W	

Yellow HLMP-8305/8309

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity HLMP-8305 HLMP-8309	I_v	 200 100	 350 260		mcd	I_F = 20 mA
Forward Voltage	V_F		2.1	2.6	V	I_F = 20 mA
Reverse Breakdown Voltage	V_R	5.0	30.0		V	I_R = 100 μA
Included Angle Between Half Intensity Points HLMP-8305 HLMP-8309	$2\theta_{1/2}$		 15 25		Deg.	
Total Luminous Flux	ϕ_v		45		mlm	I_F = 20 mA
Peak Wavelength	λ_{PEAK}		583		nm	Measured at Peak
Dominant Wavelength[1]	λ_d		585		nm	
Spectral Line Half Width	$\Delta\lambda_{1/2}$		36		nm	
Speed of Response	τ_s		90		ns	
Capacitance	C		15		pF	V_F = 0, f = 1 MHz
Thermal Resistance	$R\theta_{J\text{-}LEAD}$		210		°C/W	LED Junction-to-Cathode Lead
Luminous Efficacy[2]	η_v		500		lm/W	

Orange HLMP-8405/8409

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity HLMP-8405 HLMP-8409	I_v	 200 100	 350 260		mcd	I_F = 20 mA
Forward Voltage	V_F		1.9	2.6	V	I_F = 20 mA
Reverse Breakdown Voltage	V_R	5.0	30.0		V	I_R = 100 μA
Included Angle Between Half Intensity Points HLMP-8405 HLMP-8409	$2\theta_{1/2}$		 15 25		Deg.	
Total Luminous Flux	ϕ_v		45		mlm	I_F = 20 mA
Peak Wavelength	λ_{PEAK}		600		nm	Measured at Peak
Dominant Wavelength[1]	λ_d		602		nm	
Spectral Line Half Width	$\Delta\lambda_{1/2}$		40		nm	
Speed of Response	τ_s		280		ns	
Capacitance	C		4		pF	V_F = 0, f = 1 MHz
Thermal Resistance	$R\theta_{J\text{-}LEAD}$		210		°C/W	LED Junction-to-Cathode Lead
Luminous Efficacy[2]	η_v		380		lm/W	

High Performance Green HLMP-8505/8509

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity HLMP-8505 HLMP-8509	I_v	 200 100	 350 260		mcd	I_F = 20 mA
Forward Voltage	V_F		2.2	3.0	V	I_F = 20 mA
Reverse Breakdown Voltage	V_R	5.0	30		V	I_R = 100 µA
Included Angle Between						
Half Intensity Points HLMP-8505 HLMP-8509	$2\theta_{1/2}$		 15 25		Deg.	
Total Luminous Flux	ϕ_v		115		mlm	I_F = 20 mA
Peak Wavelength	λ_{PEAK}		568		nm	Measured at Peak
Dominant Wavelength[1]	λ_d		570		nm	
Spectral Line Half Width	$\Delta\lambda_{1/2}$		28		nm	
Speed of Response	τ_s		260		ns	
Capacitance	C		18		pF	V_F = 0, f = 1 MHz
Thermal Resistance	$R\theta_{J\text{-}LEAD}$		210		°C/W	LED Junction-to-Cathode Lead
Luminous Efficacy[2]	η_v		595		lm/W	

Notes:
1. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and represents the color of the device.
2. The readiant intensity, I_e, in watts per steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

Emerald Green HLMP-8605[1]

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity HLMP-8605	I_v	67	75		mcd	I_F = 20 mA
Forward Voltage	V_F		2.2	3.0	V	I_F = 20 mA
Reverse Breakdown Voltage	V_R	5.0	30		V	I_R = 100 µA
Included Angle Between Half Intensity Points HLMP-8605	$2\theta_{1/2}$		15		Deg.	
Peak Wavelength	λ_{PEAK}		558		nm	Measured at Peak
Dominant Wavelength[2]	λ_d		560		nm	
Spectral Line Half Width	$\Delta\lambda_{1/2}$		24		nm	
Speed of Response	τ_s		3100		ns	
Capacitance	C		35		pF	V_F = 0, f = 1 MHz
Thermal Resistance	$R\theta_{J\text{-}LEAD}$		210		°C/W	LED Junction-to-Cathode Lead
Luminous Efficacy[3]	η_v		656		lm/W	

Notes:
1. Pleae refer to Application Note 1061 for information comparing standard green and emerald green light output degradation.
2. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and represents the color of the device.
3. The readiant intensity, I_e, in watts per steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

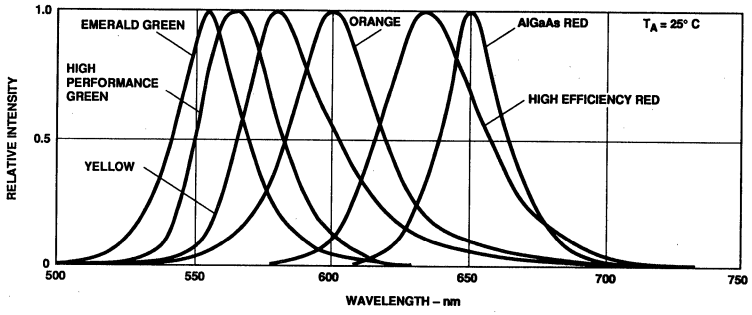


Figure 1. Relative Intensity vs. Wavelength.

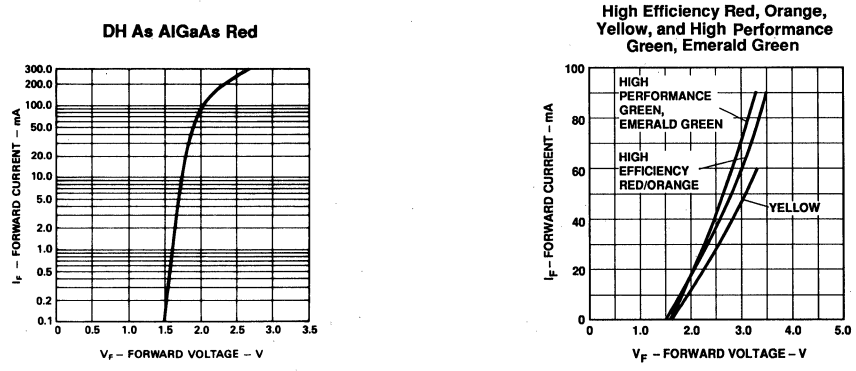


Figure 2. Forward Current vs. Forward Voltage (Non-Resistor Lamp).

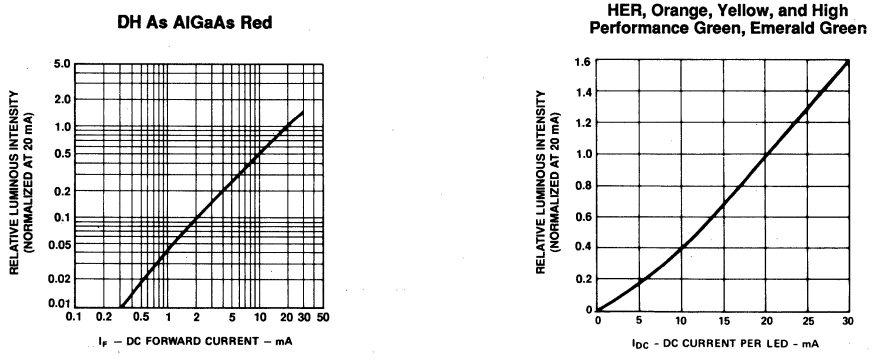


Figure 3. Relative Luminous Intensity vs. Forward Current.

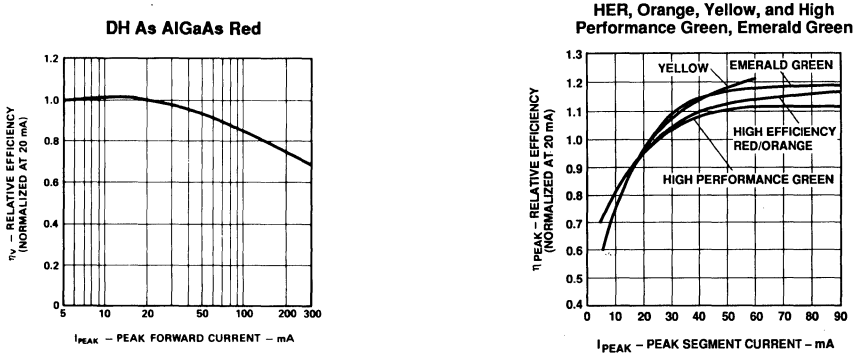


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

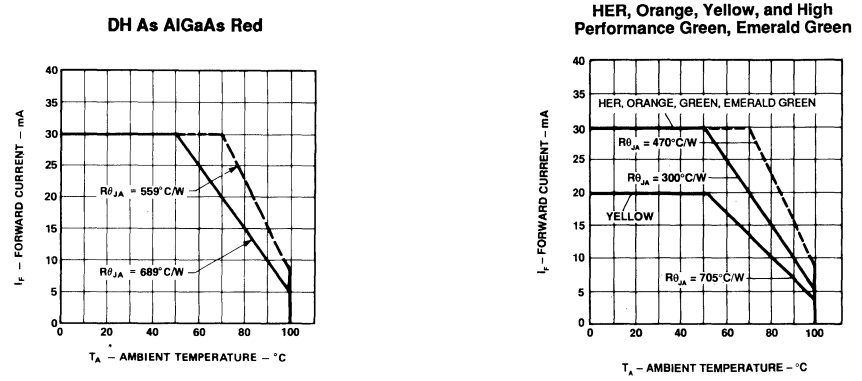


Figure 5. Maximum Forward dc Current vs. Ambient Temperature. Derating Based on T_J MAX = 110 °C.

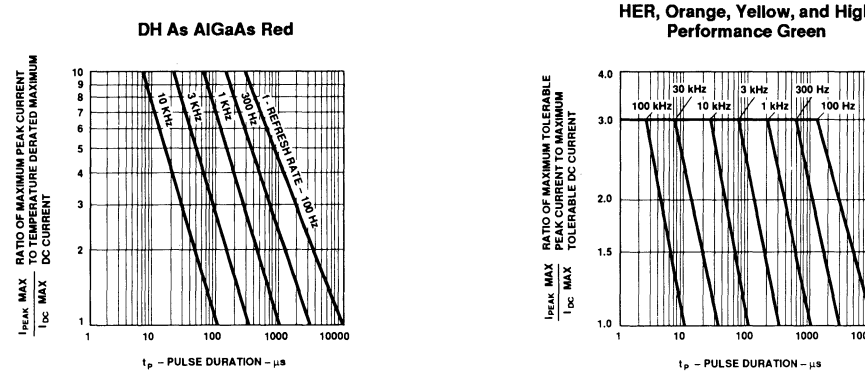


Figure 6. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

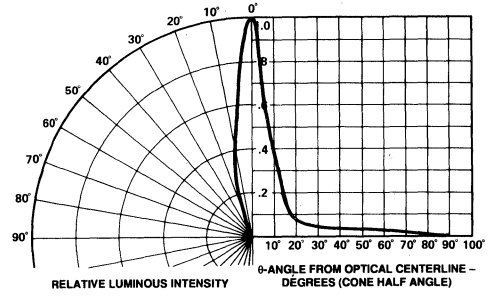


Figure 7. Relative Luminous Intensity vs. Angular Displacement. HLMP-8115/-8X05.

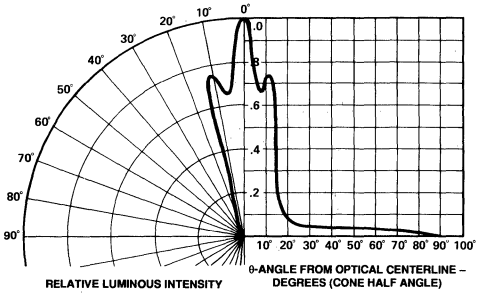


Figure 8. Relative Luminous Intensity vs. Angular Displacement. HLMP-8X09.

Ultra-Bright LED Lamps

Technical Data

HLMP-3750, -3850, -3950
HLMP-3390, -3490, -3590
HLMP-1340, -1440, -1540
New **HLMP-D640**
New **HLMP-K640**

Features

- **Improved Brightness**
- **Improved Color Performance**
- **Available in Popular T-1 and T-1¾ Packages**
- **New Sturdy Leads**
- **IC Compatible/Low Current Capability**
- **Reliable and Rugged**
- **Choice of 3 Bright Colors**
  High Efficiency Red
  High Brightness Yellow
  High Performance Green

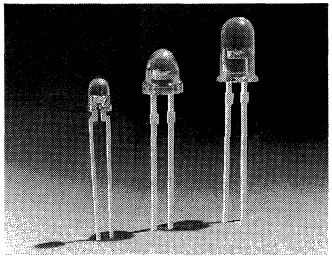
Applications

- **Lighted Switches**
- **Backlighting Front Panels**
- **Light Pipe Sources**
- **Keyboard Indicators**

Description

These clear, non-diffused lamps out-perform conventional LED lamps. By utilizing new higher intensity material, we achieve superior product performance.

The HLMP-3750/-3390/-1340 Series Lamps are Gallium Arsenide Phosphide on Gallium Phosphide red light emitting diodes. The



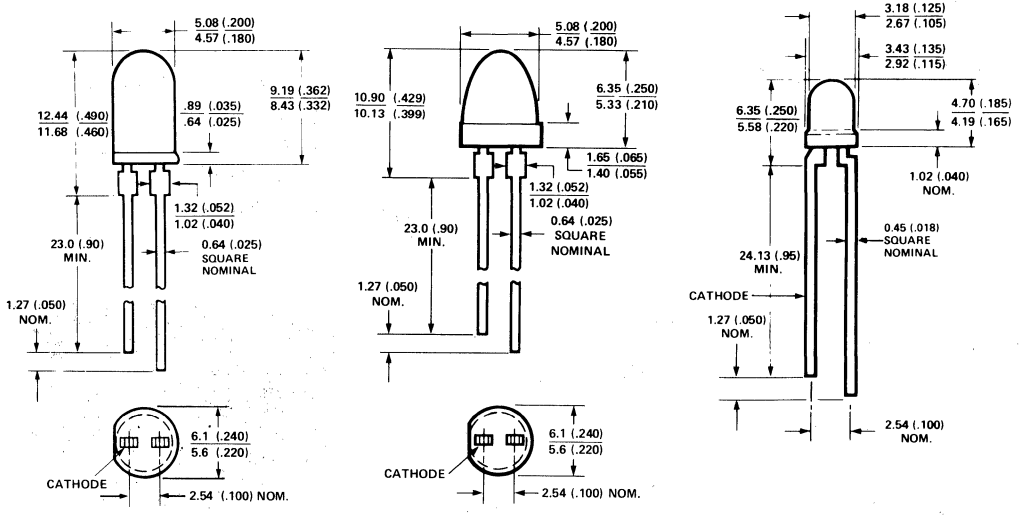
HLMP-3850/-3490/-1440 Series are Gallium Arsenide Phosphide on Gallium Phosphide yellow light emitting diodes. The HLMP-3950/-3590/-1540 Series Lamps are Gallium Phosphide green light emitting diodes.

Axial Luminous Intensity and Viewing Angle @ 25°C

Part Number HLMP-	Package Description	Color	I_v (mcd) @ 20 mA DC		$2\theta_{1/2}$[1]	Package Outline
			Min.	Typ.		
3750	T-1¾	HER	80	125	24°	A
3850		Yellow	80	140	24°	A
3950		Green	80	120	24°	A
D640[2]		Emerald Green	6.7	21	24°	A
3390	T-1¾ Low Profile	HER	35	55	32°	B
3490		Yellow	35	55	32°	B
3590		Green	35	55	32°	B
1340	T-1	HER	24	45	45°	C
1440		Yellow	24	45	45°	C
1540		Green	24	45	45°	C
K640[2]		Emerald Green	4.2	21	45°	C

Note:
1. $\theta_{1/2}$ is the typical off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. Please refer to Application Note 1061 for information comparing standard green and emerald green light output degradation.

Package Dimensions



PACKAGE OUTLINE "A"
HLMP-3750, -3850, -3950

PACKAGE OUTLINE "B"
HLMP-3390, -3490, -3590

PACKAGE OUTLINE "C"
HLMP-1340, -1440, -1540

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1 mm (0.40") DOWN THE LEADS.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	Red	Yellow	Green/Emerald Green	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Transient Forward Current[3] (10 μs Pulse)	500	500	500	mA
Reverse Voltage (I_R = 100 μA)	5	5	5	V
LED Junction Temperature	110	110	110	°C
Operating Temperature Range	-55 to +100	-55 to +100	-20 to +100	°C
Storage Temperature Range			-55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 5 seconds			

Notes:
1. See Figure 2 to establish pulsed operating conditions.
2. For Red and Green series derate linearly from 50°C at 0.5 mA/°C. For Yellow series derate linearly from 50°C at 0.2 mA/°C.
3. The transient peak current is the maximum non-recurring peak current the devices can withstand without damaging the LED die and wire bonds. It is not recommended that the device be operated at peak currents beyond the Absolute Maximum Peak Forward Current.

Electrical/Optical Characteristics at T_A = 25°C

Symbol	Description	T-1¾	T-1¾ Low Dome	T-1	Min.	Typ.	Max.	Units	Test Conditions
λ_{PEAK}	Peak Wavelength	3750 3850 3950 D640	3390 3490 3590	1340 1440 1540 K640		635 583 565 558		nm	Measurement at Peak
λ_d	Dominant Wavelength	3750 3850 3950 D640	3390 3490 3590	1340 1440 1540 K640		626 585 569 560		nm	Note 1
$\Delta\lambda 1/2$	Spectral Line Halfwidth	3750 3850 3950 D640	3390 3490 3590	1340 1440 1540 K640		40 36 28 24		nm	
τ_S	Speed of Response	3750 3850 3950 D640	3390 3490 3590	1340 1440 1540 K640		90 90 500 3100		ns	
C	Capacitance	3750 3850 3950 D640	3390 3490 3590	1340 1440 1540 K640		11 15 18 35		pF	V_F = 0, f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance	3750 3850 3950 D640	3390 3490 3590	 1340 1440 1540 K640		210 210 210 510 290 290 290 290		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	3750 3850 3950 D640	3390 3490 3590	1340 1440 1540 K640	1.5 1.5 1.5	1.9 2.1 2.2 2.2	2.6 2.6 3.0 3.0	V	I_F = 20 mA (Figure 3)
V_R	Reverse Breakdown Voltage	3750 3850 3950 D640	3390 3490 3590	1340 1440 1540 K640	5.0			V	I_F = 100 µA
η_V	Luminous Efficacy	3750 3850 3950 D640	3390 3490 3590	1340 1440 1540 K640		145 500 595 655		$\frac{\text{lumens}}{\text{watt}}$	Note 2

Notes:

1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. The radiant intensity, I_e, in watts per steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Red, Yellow, and Green

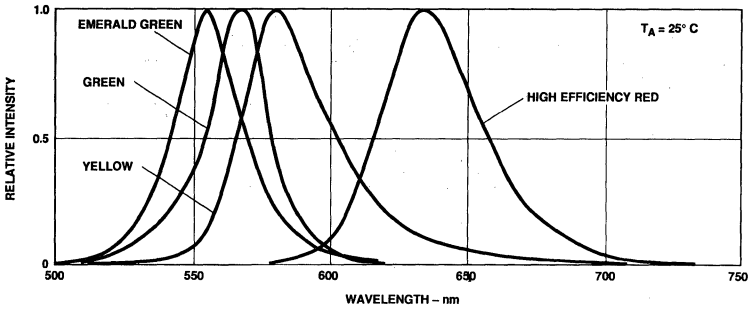


Figure 1. Relative Intensity vs. Wavelength.

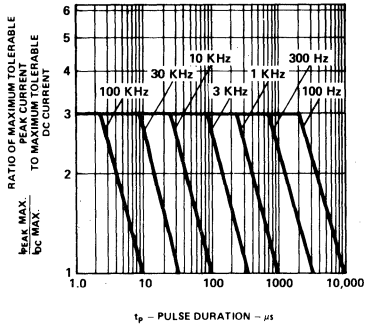


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

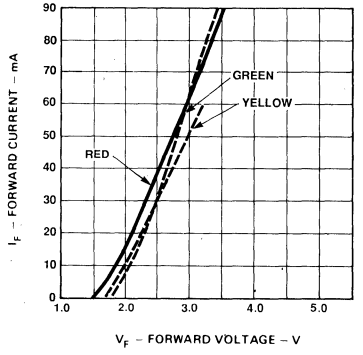


Figure 3. Forward Current vs. Forward Voltage.

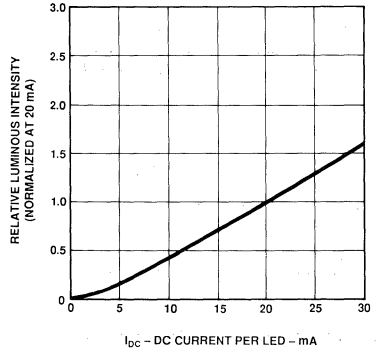


Figure 4. Relative Luminous Intensity vs. Forward Current.

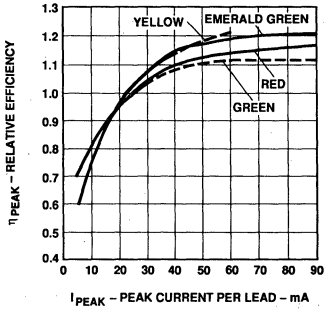


Figure 5. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

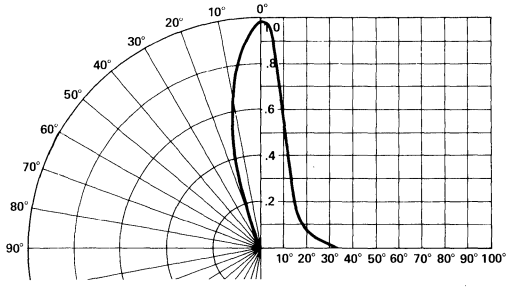


Figure 6. Relative Luminous Intensity vs. Angular Displacement. T-1 3/4 Lamp.

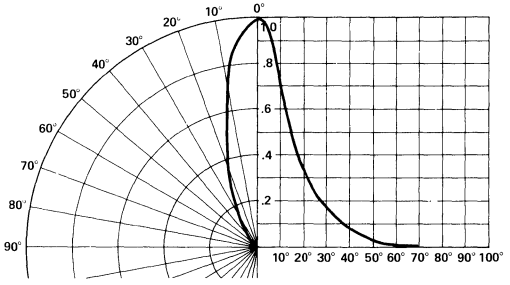


Figure 7. Relative Luminous Intensity vs. Angular Displacement. T-1 3/4 Low Profile Lamp.

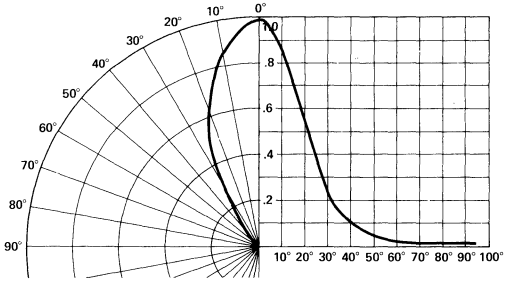


Figure 8. Relative Luminous Intensity vs. Angular Displacement. T-1 Lamp.

HEWLETT PACKARD

Low Current LED Lamps

Technical Data

HLMP-4700, -4719, -4740
HLMP-1700, -1719, -1790
HLMP-7000, -7019, -7040

Features

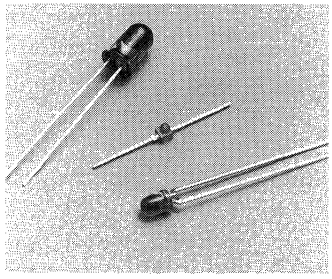
- **Low Power**
- **High Efficiency**
- **CMOS-MOS Compatible**
- **TTL Compatible**
- **Wide Viewing Angle**
- **Choice of Package Styles**
- **Choice of Colors**

Applications

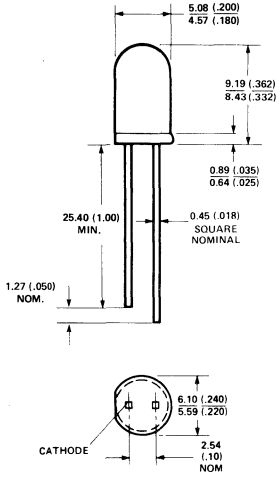
- **Low Power DC Circuits**
- **Telecommunications Indicators**
- **Portable Equipment**
- **Keyboard Indicators**

Description

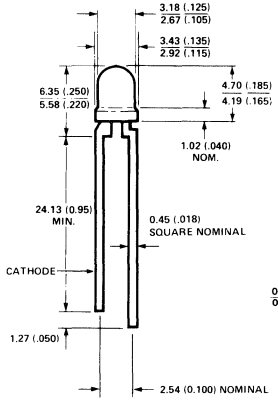
These tinted diffused LED lamps were designed and optimized specifically for low DC current operation. Luminous intensity and forward voltage are tested at 2 mA to assure consistent brightness at TTL output current levels.



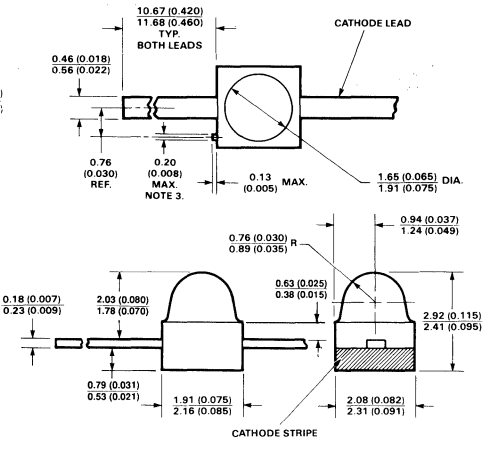
Package Dimensions



HLMP-4700, -4719, -4740



HLMP-1700, -1719, -1790



HLMP-7000, -7019, -7040

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MINISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.
3. PROTRUDING SUPPORT TAB IS CONNECTED TO CATHODE LEAD.

Low Current Lamp Selection Guide

Size	Color		
	Red HLMP-	Yellow HLMP-	Green HLMP-
T-1 3/4	4700	4719	4740
T-1	1700	1719	1790
Subminiature	7000	7019	7040

Axial Luminous Intensity and Viewing Angle @ 25°C

Part Number HLMP-	Package Description	Color	I_V (mcd) @ 2 mA DC		$2\theta_{1/2}$[1]	Package Outline
			Min.	Typ.		
4700	T-1 3/4	Red	1.2	2.0	50°	A
4719	Tinted Diffused	Yellow	1.2	1.8		
4740		Green	1.2	1.8		
1700	T-1	Red	1.0	1.8	50°	B
1719	Tinted Diffused	Yellow	1.0	1.6		
1790		Green	1.0	1.6		
7000	Subminiature	Red	0.4	0.8	90°	C
7019	Tinted Diffused	Yellow	0.4	0.6		
7040		Green	0.4	0.6		

Note:
1. $\theta_{1/2}$ is the typical off-axis angle at which the luminous intensity is half the axial luminous intensity.

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	T-1¾	T-1	Sub-miniature	Min.	Typ.	Max.	Units	Test Conditions
V_F	Forward Voltage	4700 4719 4740	1700 1719 1790	7000 7019 7040		1.8 1.9 1.8	2.0 2.5 2.2	V	2 mA
V_R	Reverse Breakdown Voltage	4700 4719 4740	1700 1719 1790	7000 7019 7040	5.0 5.0 5.0			V	$I_R = 50\ \mu A$
λ_d	Dominant Wavelength	4700 4719 4740	1700 1719 1790	7000 7019 7040		626 585 569		nm	Note 1
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	4700 4719 4740	1700 1719 1790	7000 7019 7040		40 36 28		nm	
τ_S	Speed of Response	4700 4719 4740	1700 1719 1790	7000 7019 7040		90 90 500		ns	
C	Capacitance	4700 4719 4740	1700 1719 1790	7000 7019 7040		11 15 18		pF	$V_F = 0$, f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance	4700 4719 4740	1700 1719 1790	7000 7019 7040		260[3] 290[4] 170[5]		°C/W	Junction to Cathode Lead
λ_{PEAK}	Peak Wavelength	4700 4719 4740	1700 1719 1790	7000 7019 7040		635 583 565		nm	Measurement at peak
η_V	Luminous Efficacy	4700 4719 4740	1700 1719 1790	7000 7019 7040		145 500 595		$\frac{\text{lumens}}{\text{watt}}$	Note 2

Notes:

1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. The radiant intensity, I_e, in watts per steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is luminous efficacy in lumens/watt.
3. T-1¾.
4. T-1.
5. Subminiature.

Absolute Maximum Ratings

Parameter	Maximum Rating		Units
Power Dissipation (Derate linearly from 92°C at 1.0 mA/°C)	Red Yellow Green	24 36 24	mW
DC and Peak Forward Current	7		mA
Transient Forward Current (10 μs Pulse)[1]	500		mA
Reverse Voltage (I_R = 50 μA)	5.0		V
Operating Temperature Range	Red/Yellow Green	-55°C to 100°C -20°C to 100°C	
Storage Temperature Range	-55°C to +100°C		
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 5 seconds (T-1, T-1 3/4) 260°C for 5 seconds (Subminiature)		

Note:

1. The transient peak current is the maximum non-recurring peak current the devices can withstand without damaging the LED die and wire bonds. It is not recommended that the device be operated at peak currents beyond the Absolute Maximum Peak Forward Current.

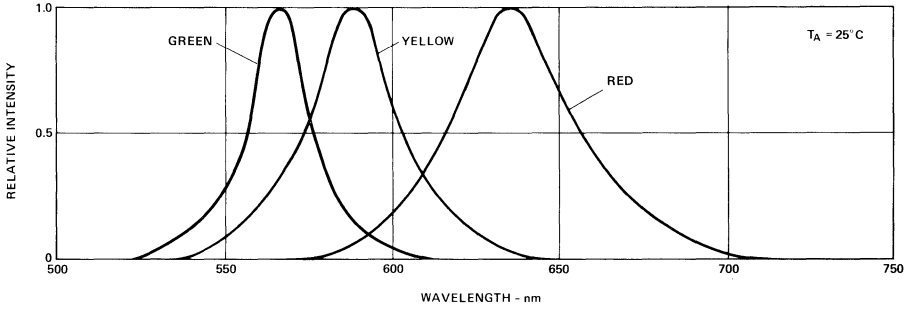


Figure 1. Relative Intensity vs. Wavelength.

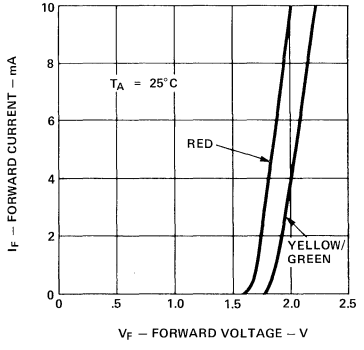


Figure 2. Forward Current vs. Forward Voltage.

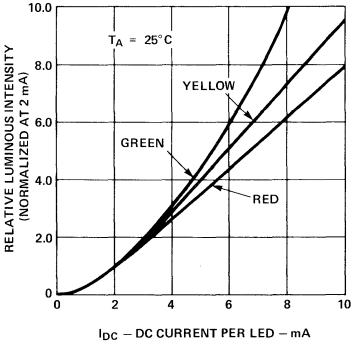


Figure 3. Relative Luminous Intensity vs. Forward Current.

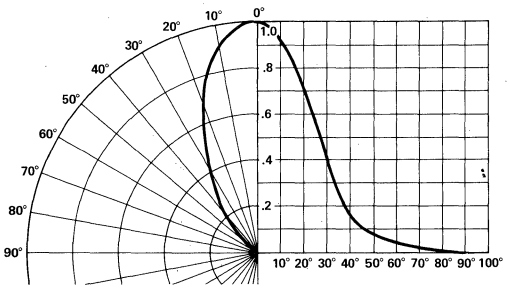


Figure 4. Relative Luminous Intensity vs. Angular Displacement for T-1¾ Lamp.

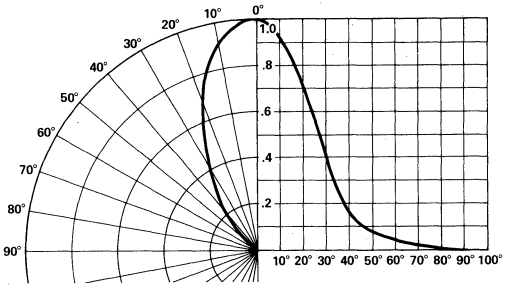


Figure 5. Relative Luminous Intensity vs. Angular Displacement for T-1 Lamp.

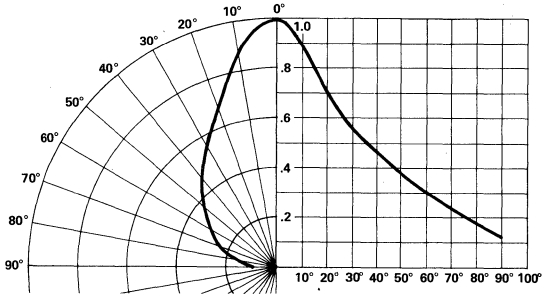


Figure 6. Relative Luminous Intensity vs. Angular Displacement for Subminiature Lamp.

HEWLETT PACKARD

new

Surface Mount Indicator Lamps

Technical Data

HSMH-TX00
HSMS-TX00
HSMD-TX00
HSMY-TX00
HSMG-TX00

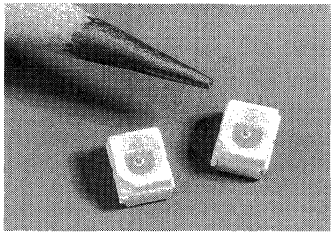
Features

- **Compatible with Automatic Placement Equipment**
- **Compatible with Infrared and Vapor Phase Reflow Solder Processes**
- **Packaged in 12 mm or 8 mm tape on 7" or 13" Diameter Reels**
- **EIA Standard Package**
- **Low Package Profile**
- **Non-diffused Package Excellent for Backlighting and Coupling to Light Pipes**

Description

These solid state surface mount indicators are designed with a flat top and sides to be easily handled by automatic placement equipment. A glue pad is provided for adhesive mounting processes. They are compatible with convective IR and vapor phase reflow soldering and conductive epoxy attachment processes.

The package size and configuration conform to the EIA-535 BAAC standard specification for case size 3528 tantalum capacitors. The folded leads



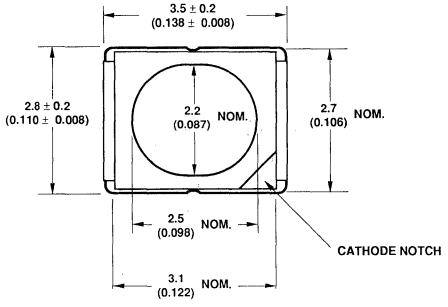
permit dense placement and provide an external solder joint for ease of inspection.

These devices are non-diffused, providing high intensity for applications such as backlighting, light pipe illumination, and front panel indication.

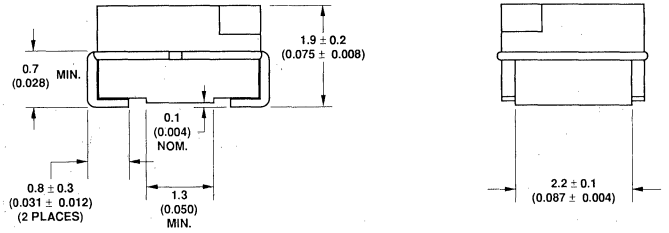
Device Selection Guide

DH AS AlGaAs Red	High Efficiency Red	Orange	Yellow	High Performance Green	Description
HSMH-T400	HSMS-T400	HSMD-T400	HSMY-T400	HSMG-T400	12 mm Tape, 7" Reel, 2000 Devices
HSMH-T500	HSMS-T500	HSMD-T500	HSMY-T500	HSMG-T500	12 mm Tape, 13" Reel, 8000 Devices
HSMH-T600	HSMS-T600	HSMD-T600	HSMY-T600	HSMG-T600	8 mm Tape, 7" Reel, 2000 Devices
HSMH-T700	HSMS-T700	HSMD-T700	HSMY-T700	HSMG-T700	8 mm Tape, 13" Reel, 8000 Devices

Package Dimensions

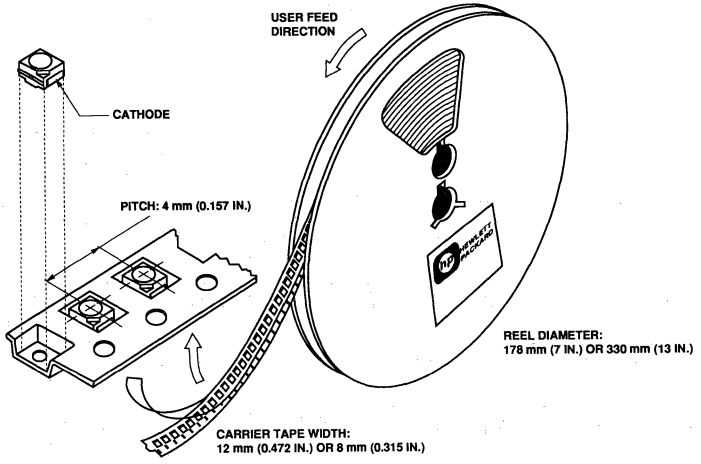


NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES).
2. THE LEADS ARE COPPER ALLOY, 85% Sn/15% Pb PLATING.



Tape and Reel Specifications

Hewlett Packard surface mount LEDs are packaged tape and reel in accordance with EIA-481A, *Taping of Surface Mount Components for Automatic Placement*. This packaging system is compatible with tape-fed automatic pick and place systems. Each reel is sealed in a vapor barrier bag for added protection. Bulk packaging in vapor barrier bags is available upon special request.



Absolute Maximum Ratings at T_A = 25°C

Parameter	DH AS AlGaAs Red	High Efficiency Red	Orange	Yellow	High Performance Green	Units
DC Forward Current[1]	30	30	30	20	30	mA
Peak Forward Current[2]	300	90	90	60	90	mA
Average Forward Current[2]	20	25	25	20	25	mA
LED Junction Temperature	95					°C
Transient Forward Current[3] (10 μs Pulse)	500					mA
Reverse Voltage (I_R = 100 μA)	5					V
Operating Temperature Range	-40 to +85					°C
Storage Temperature Range	-40 to +85					°C
Reflow Soldering Temperatures Convective IR Vapor Phase	235°C Peak, above 185°C for 90 seconds. 215°C for 3 minutes.					

Notes:

1. Derate dc current lineally from 50°C: For AlGaAs red, high efficiency red, and green devices at 0.67 mA/°C. For yellow devices at 0.44 mA/°C.
2. Refer to Figure 5 showing Maximum Tolerable Peak Current vs. Pulse duration to establish pulsed operating conditions.
3. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bond. The device should not be operated at peak currents above the Absolute Maximum Peak Forward Current.

Electrical/Optical Characteristics at T_A = 25°C

DH AS AlGaAs Red HSMH-TX00

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity	I_v	9.0	17.0		mcd	I_F = 10 mA
Forward Voltage	V_F		1.8	2.2	V	I_F = 10 mA
Reverse Breakdown Voltage	V_R	5.0	15.0		V	I_R = 100 μA
Included Angle Between Half Intensity Points[1]	$2\theta_{1/2}$		120		deg.	
Peak Wavelength	λ_{PEAK}		645		nm	
Dominant Wavelength[2]	λ_d		637		nm	
Spectral Line Half Width	$\Delta\lambda_{1/2}$		20		nm	
Speed of Response	τ_s		30		ns	Time Constant, e^{-t/τ_s}
Capacitance	C		30		pF	V_F = 0, f = 1 MHz
Thermal Resistance	$R\theta_{J-C}$		180		°C/W	Junction-to-Cathode
Luminous Efficacy[3]	η_v		80		lm/W	

High Efficiency Red HSMS-TX00

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity	I_v	2.0	6.0		mcd	I_F = 10 mA
Forward Voltage	V_F		1.9	2.5	V	I_F = 10 mA
Reverse Breakdown Voltage	V_R	5.0	30.0		V	I_R = 100 µA
Included Angle Between Half Intensity Points[1]	$2\theta_{1/2}$		120		deg.	
Peak Wavelength	λ_{PEAK}		635		nm	
Dominant Wavelength[2]	λ_d		626		nm	
Spectral Line Half Width	$\Delta\lambda_{1/2}$		40		nm	
Speed of Response	τ_s		90		ns	Time Constant, e^{-t/τ_s}
Capacitance	C		11		pF	V_F = 0, f = 1 MHz
Thermal Resistance	$R\theta_{J-C}$		160		°C/W	Junction-to-Cathode
Luminous Efficacy[3]	η_v		145		lm/W	

Orange HSMD-TX00

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity	I_v	1.5	5.0		mcd	I_F = 10 mA
Forward Voltage	V_F		1.9	2.5	V	I_F = 10 mA
Reverse Breakdown Voltage	V_R	5.0	30.0		V	I_R = 100 µA
Included Angle Between Half Intensity Points[1]	$2\theta_{1/2}$		120		deg.	
Peak Wavelength	λ_{PEAK}		600		nm	
Dominant Wavelength[2]	λ_d		602		nm	
Spectral Line Half Width	$\Delta\lambda_{1/2}$		40		nm	
Speed of Response	τ_s		260		ns	Time Constant, e^{-t/τ_s}
Capacitance	C		4		pF	V_F = 0, f = 1 MHz
Thermal Resistance	$R\theta_{J-C}$		160		°C/W	Junction-to-Cathode
Luminous Efficacy[3]	η_v		380		lm/W	

Notes:
1. $\theta_{1/2}$ is the off-axis angle where the luminous intensity is half the on-axis value.
2. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and represents the color of the device.
3. The radiant intensity, I_e, in watts per steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is luminous efficacy in lumens/watt.

Yellow HSMY-TX00

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity	I_v	2.0	5.0		mcd	I_F = 10 mA
Forward Voltage	V_F		2.0	2.5	V	I_F = 10 mA
Reverse Breakdown Voltage	V_R	5.0	50.0		V	I_R = 100 µA
Included Angle Between Half Intensity Points[1]	$2\theta_{1/2}$		120		deg.	
Peak Wavelength	λ_{PEAK}		583		nm	
Dominant Wavelength[2]	λ_d		585		nm	
Spectral Line Half Width	$\Delta\lambda_{1/2}$		36		nm	
Speed of Response	τ_s		90		ns	Time Constant, e^{-t/τ_s}
Capacitance	C		15		pF	V_F = 0, f = 1 MHz
Thermal Resistance	$R\theta_{J-C}$		160		°C/W	Junction-to-Cathode
Luminous Efficacy[3]	η_v		500		lm/W	

High Performance Green HSMG-TX00

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity	I_v	5.0	10.0		mcd	I_F = 10 mA
Forward Voltage	V_F		2.0	2.5	V	I_F = 10 mA
Reverse Breakdown Voltage	V_R	5.0	50.0		V	I_R = 100 µA
Included Angle Between Half Intensity Points[1]	$2\theta_{1/2}$		120		deg.	
Peak Wavelength	λ_{PEAK}		570		nm	
Dominant Wavelength[2]	λ_d		572		nm	
Spectral Line Half Width	$\Delta\lambda_{1/2}$		28		nm	
Speed of Response	τ_s		500		ns	Time Constant, e^{-t/τ_s}
Capacitance	C		18		pF	V_F = 0, f = 1 MHz
Thermal Resistance	$R\theta_{J-C}$		160		°C/W	Junction-to-Cathode
Luminous Efficacy[3]	η_v		595		lm/W	

Notes:
1. $\theta_{1/2}$ is the off-axis angle where the luminous intensity is half the on-axis value.
2. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and represents the color of the device.
3. The radiant intensity, I_e, in watts per steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is luminous efficacy in lumens/watt.

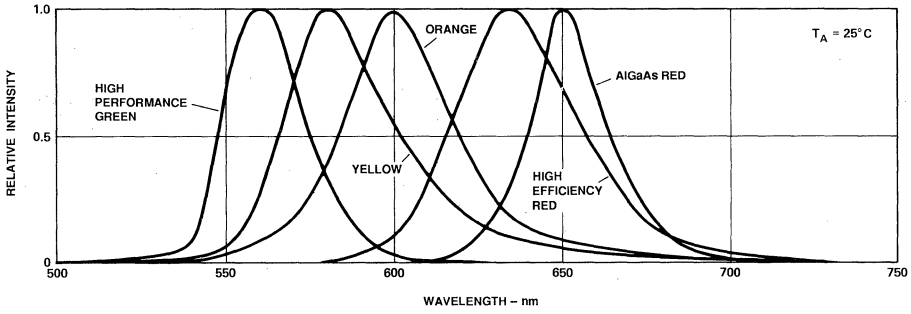


Figure 1. Relative Intensity vs. Wavelength.

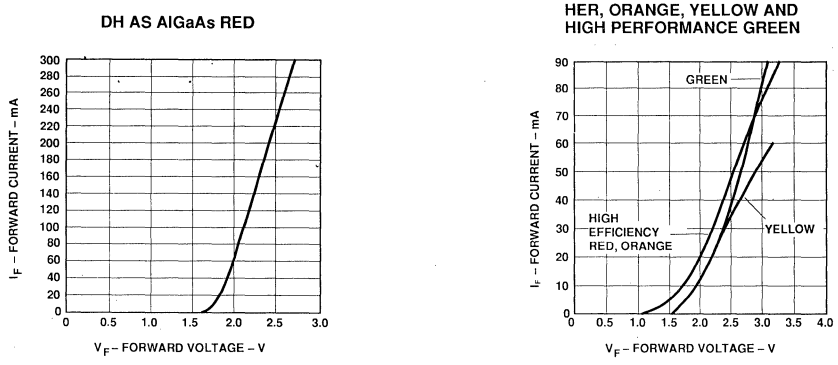


Figure 2. Forward Current vs. Forward Voltage.

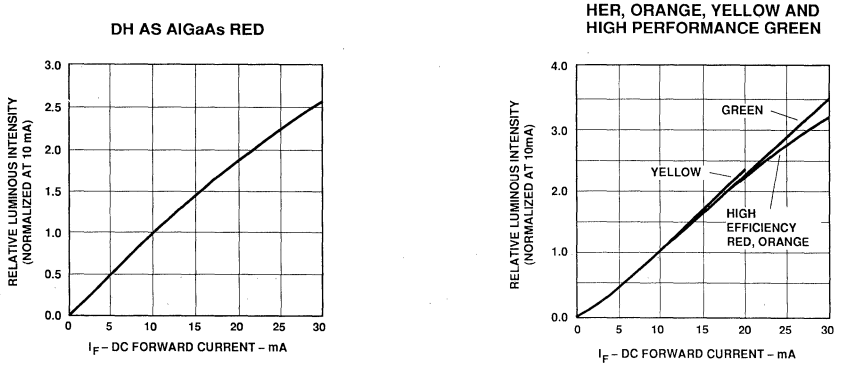


Figure 3. Relative Luminous Intensity vs. Forward Current.

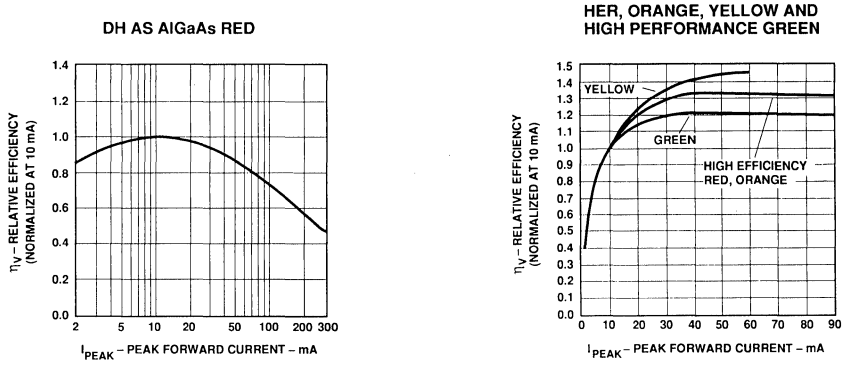


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

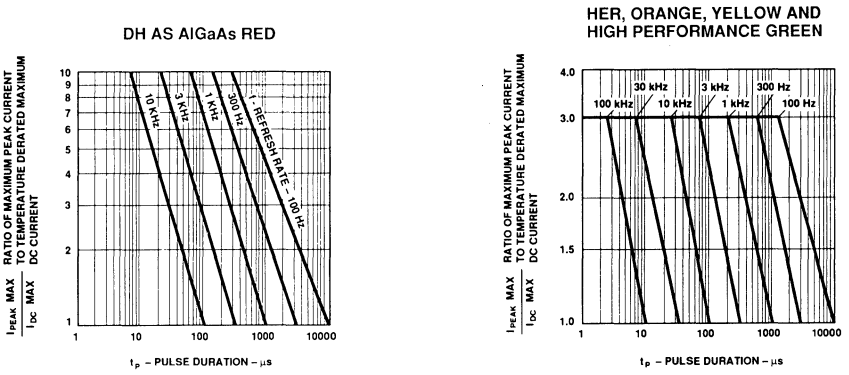


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration (I_{DC} MAX per MAX Ratings).

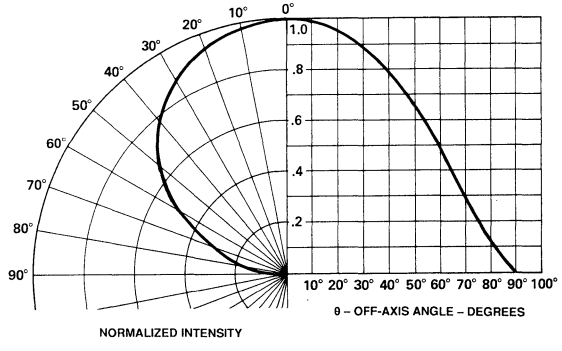
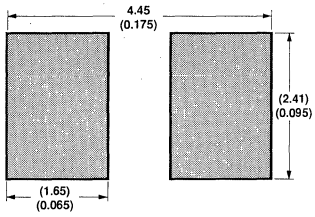


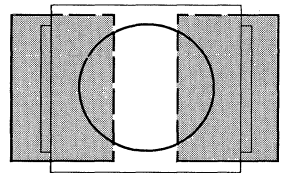
Figure 6. Relative Intensity vs. Angular Displacement.

Recommended Printed Circuit Board Attachment Pad Geometries

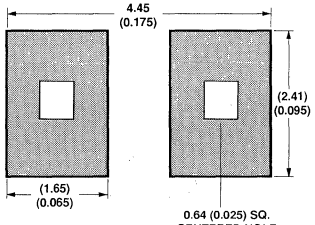
INFRARED/VAPOR PHASE
REFLOW SOLDERING



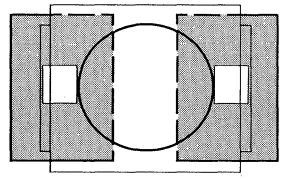
COMPONENT LOCATION
ON PAD



CONDUCTIVE ATTACHMENT



COMPONENT LOCATION
ON PAD



NOTE: ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).

Convective IR Reflow Soldering

For information on IR reflow soldering, refer to Application Note 1060, *Surface Mounting SMT Led Indicator Components.*

High Power T - 4 (13.3 mm) TS AlGaAs Red Lamp

Technical Data

HLMP-8150 15 Candela

Features

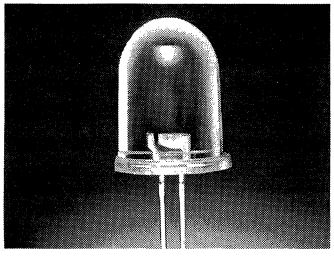
- **15 Candelas at 20 mA**
- **Outstanding LED Material Efficiency**
- **High Light Output Over a Wide Range of Drive Currents**
- **4° Viewing Angle**
- **Low Forward Voltage**
- **Low Power Dissipation**
- **CMOS/MOS Compatible**
- **Red Color**

Applications

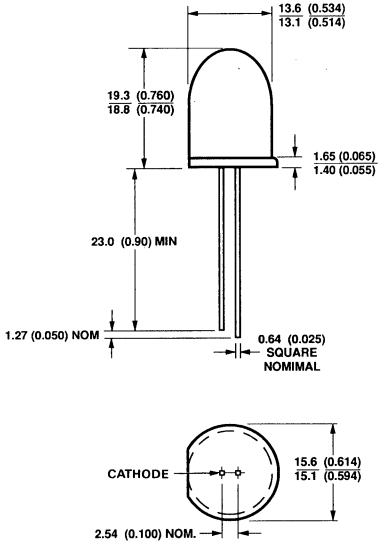
- **Emitter for Emitter/ Detector Applications**
- **Power Signaling**
- **Bright Ambient Lighting Conditions**
- **Bar Code Readers**
- **Replacement for a Low Power Laser**

Description

This untinted, nondiffused solid state lamp utilizes a highly optimized LED material, transparent substrate aluminum gallium arsenide, TS AlGaAs. This material has outstanding light output efficiency over a wide range of currents, and has superior high current capability to most other LED materials. The lamp design utilizes advanced optical methods to enable extremely high peak intensity and a very narrow viewing angle. The LED color is red at a dominant wavelength of 637 nm.



Package Dimensions



Notes:
1. All dimensions are in millimetres (inches).
2. The leads are mild steel, solder dipped.
3. An epoxy meniscus may extend about 1 mm (0.040 ") down the leads.

Axial Luminous Intensity and Viewing Angle at T_A = 25°C

Minimum Intensity (cd) @ 20 mA	Typical Intensity (cd) @ 20 mA	Maximum Intensity (cd) @ 20 mA	Typical Radiant Intensity (mW/sr) @ 20 mA	$2\theta_{1/2}$ [1] (degrees)
8.0	15.0	36.0	176	4.0

Note. 1. $\theta_{1/2}$ is the off axis angle from optical centerline where the luminous intensity is 1/2 the on-axis value.

Absolute Maximum Ratings at T_A = 25 °C

Peak Forward Current[2] ..... 200 mA
Average Forward Current (@ I_{PEAK} = 200 mA)[1,2] ..... 35 mA
DC Forward Current[3] ..... 50 mA
Power Dissipation ..... 100 mW
Reverse Voltage (I_R=100 μA) ..... 5 V
Transient Forward Current (10 μs Pulse)[4] ..... 500 mA
Operating Temperature Range ..... -55 to +100°C
Storage Temperature Range ..... -55 to +100°C
LED Junction Temperature ..... 110°C
Lead Soldering Temperature
[1.6 mm (0.063 in.) from body] ..... 260°C for 5 seconds

Notes:
1. Maximum I_{AVG} at f = 1 kHz, DF = 17.5%.
2. Refer to Figure 6 to establish pulsed operating conditions.
3. Derate linearly as shown in Figure 5.
4. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bonds. It is not recommended that the device be operated at peak currents above the Absolute Maximum Peak Forward Current.

Electrical/Optical Characteristics at T_A = 25 °C

Description	Symbol	Min.	Typ.	Max.	Units	Test Condition
Forward Voltage	V_F		1.85	2.4	V	I_F = 20 mA
Reverse Voltage	V_R	5.0	20.0		V	I_R = 100 μA
Peak Wavelength	λ_{PEAK}		650		nm	
Dominant Wavelength [1]	λ_d		637		nm	
Spectral Line Halfwidth	$\Delta\lambda 1/2$		22		nm	
Speed of Response	τ_S		45		ns	Exponential Time Constant, $e^{-t/\tau s}$
Capacitance	C		20		pF	V_F = 0, f = 1 MHz
Thermal Resistance	$R\theta_{J\text{-}PIN}$		210		°C/W	Junction-to-Anode Lead
Luminous Efficacy [2]	η_v		85		lm/W	

Notes:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the color of the device.
2. The radiant intensity, I_e, in watts per steradian, may be found from the equation $I_e=I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is luminous efficacy in lumens/watt.
3. The approximate total luminous flux output within a cone angle of 2θ about the optical axis may be obtained from the following formula:
$\phi_V 2(\theta) = [\phi_V(\theta)/I_V(0)]I_V$;
Where: $\phi_V(\theta)/I_V(0)$ is obtained from Figure 7.

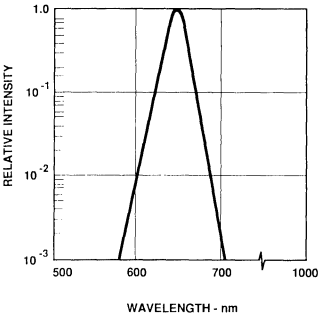


Figure 1. Relative Intensity vs. Wavelength.

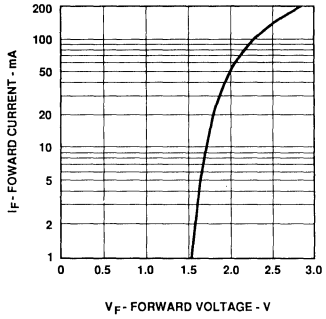


Figure 2. Forward Current vs. Forward Voltage.

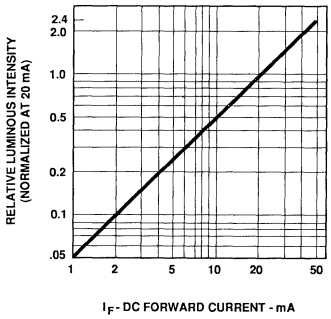


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

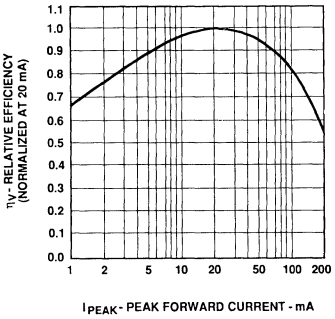


Figure 4. Relative Efficiency vs. Peak Forward Current.

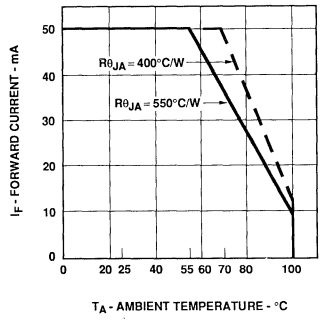


Figure 5. Maximum Forward DC Current vs. Ambient Temperature.
Derating Based on T_JMAX = 110°C.

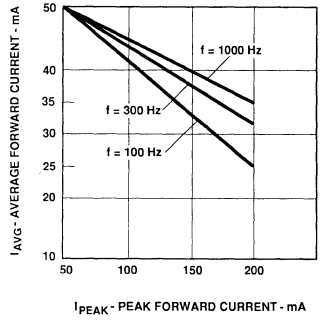


Figure 6. Maximum Average Current vs. Peak Forward Current.

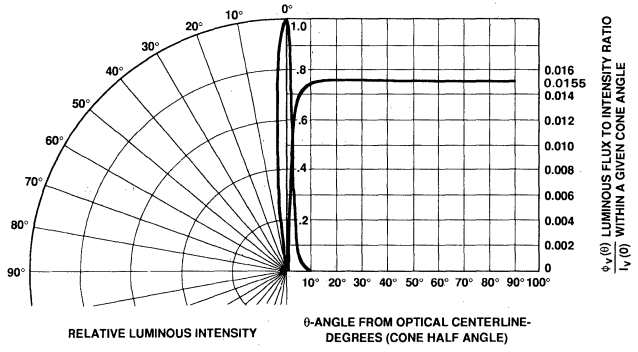


Figure 7. Relative Luminous Intensity vs. Angular Displacement, HLMP-8150.

HEWLETT PACKARD

T-1¾ (5 mm) High Intensity Solid State Lamps

Technical Data

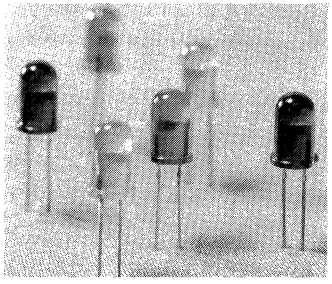
HLMP-331X Series
HLMP-341X Series
HLMP-351X Series

Features

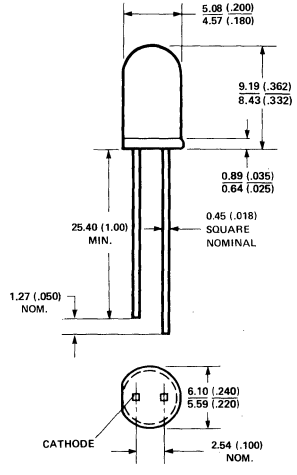
- **High Intensity**
- **Choice of 3 Bright Colors**
  High Efficiency Red
  Yellow
  High Performance Green
- **Popular T-1¾ Diameter Package**
- **Selected Minimum Intensities**
- **Narrow Viewing Angle**
- **General Purpose Leads**
- **Reliable and Rugged**
- **Available on Tape and Reel**

Description

This family of T-1¾ lamps is specially designed for applications requiring higher on-axis intensity than is achievable with a standard lamp. The light generated is focused to a narrow beam to achieve this effect.



Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Selection Guide

Part Number HLMP-	Description	Minimum Intensity (mcd) at 10 mA	Color (Material)
3315	Illuminator/ Point Source	12	High Efficiency Red (GaAsP on GaP)
3316	Illuminator/ High Brightness	20	
3415	Illuminator/ Point Source	10	Yellow (GaAsP on GaP)
3416	Illuminator/ High Brightness	20	
3517	Illuminator/ Point Source	6.7	Green (GaP)
3519	Illuminator/ High Brightness	10.6	

Electrical Characteristics at $T_A = 25°C$

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	3315 3316	12.0 20.0	40.0 60.0		mcd	I_F = 10 mA (Figure 3)
		3415 3416	10.0 20.0	40.0 50.0		mcd	I_F = 10 mA (Figure 8)
		3517 3519	6.7 10.6	50.0 70.0		mcd	I_F = 10 mA (Figure 13)
$2\theta_{1/2}$	Including Angle Between Half Luminous Intensity Points	3315 3316		35 35		Deg.	I_F = 10 mA See Note 1 (Figure 6)
		3415 3416		35 35		Deg.	I_F = 10 mA See Note 1 (Figure 11)
		3517 3519		24 24		Deg.	I_F = 10 mA See Note 1 (Figure 16)
λ_{PEAK}	Peak Wavelength	331X 341X 351X		635 583 565		nm	Measurement at Peak (Figure 1)
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	331X 341X 351X		40 36 28		nm	
λ_d	Dominant Wavelength	331X 341X 351X		626 585 569		nm	See Note 2 (Figure 1)
τ_s	Speed of Response	331X 341X 351X		90 90 500		ns	
C	Capacitance	331X 341X 351X		11 15 18		pF	V_F = 0; f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance	331X 341X 351X		260		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	331X 341X 351X		1.9 2.0 2.1	2.4 2.4 2.7	V	I_F = 10 mA (Figure 2) I_F = 10 mA (Figure 7) I_F = 10 mA (Figure 12)
V_R	Reverse Breakdown Volt.	All	5.0			V	I_R = 100 μA
η_V	Luminous Efficacy	331X 341X 351X		145 500 595		lumens Watt	See Note 3

Notes:

1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at T_A = 25°C

Parameter	331X Series	341X Series	351X Series	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage (I_R = 100 μA)	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	500	500	mA
LED Junction Temperature	110	110	110	°C
Operating Temperature Range	-55 to +100	-55 to +100	-20 to +100	°C
Storage Temperature Range			-55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 5 seconds			

Notes:
1. See Figure 5 (Red), 10 (Yellow), or 15 (Green) to establish pulsed operating conditions.
2. For Red and Green series derate linearly from 50°C at 0.5 mA/°C. For Yellow series derate linearly from 50°C at 0.2 mA/°C.
3. For Red and Green series derate power linearly from 25°C at 1.8 mW/°C. For Yellow series derate power linearly from 50°C at 1.6 mW/°C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

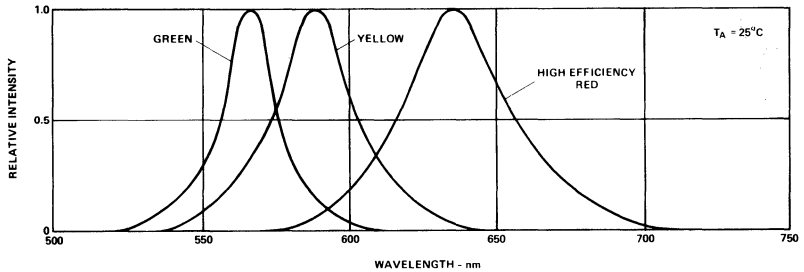


Figure 1. Relative Intensity vs. Wavelength.

High Efficiency Red HLMP-331X Series

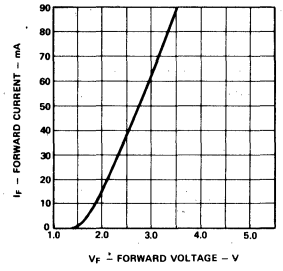


Figure 2. Forward Current vs. Forward Voltage Characteristics.

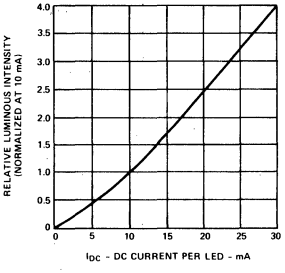


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

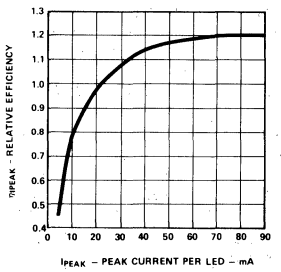


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

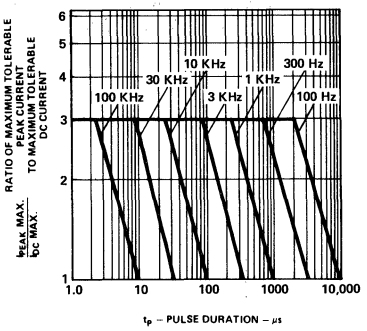


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration (I_{DC} MAX as per MAX Ratings).

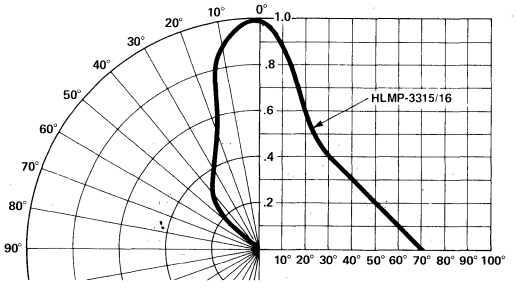


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

Yellow HLMP-341X Series

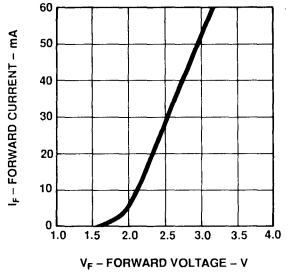


Figure 7. Forward Current vs. Forward Voltage Characteristics.

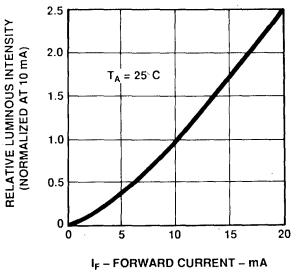


Figure 8. Relative Luminous Intensity vs. DC Forward Current.

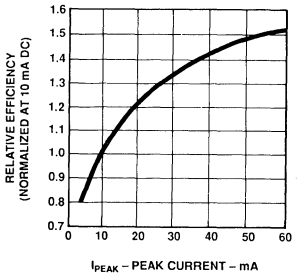


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

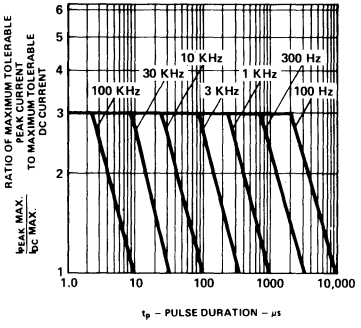


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration (I_{DC} MAX as per MAX Ratings).

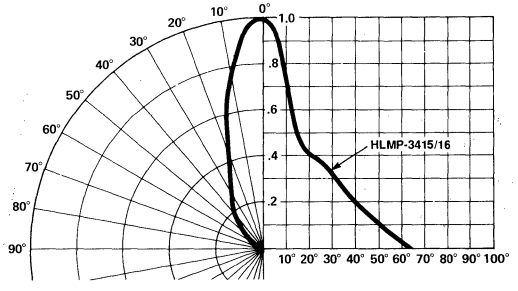


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

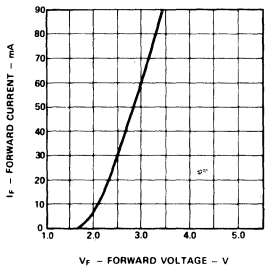


Figure 12. Forward Current vs. Forward Voltage Characteristics.

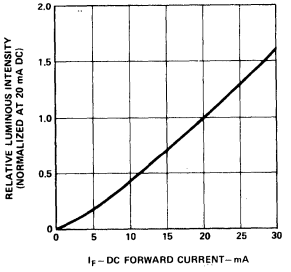


Figure 13. Relative Luminous Intensity vs. DC Forward Current.

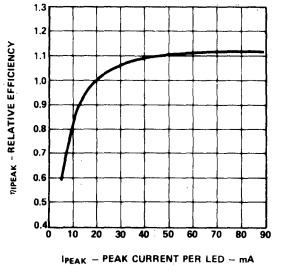


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

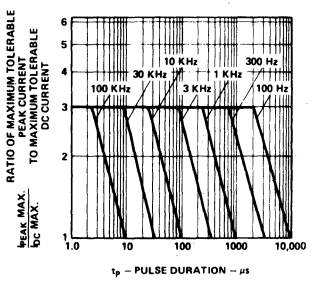


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration (I_{DC} MAX as per MAX Ratings).

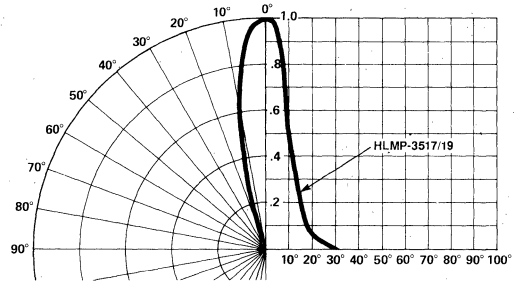


Figure 16. Relative Luminous Intensity vs. Angular Displacement. T-1¾ Lamp.

HEWLETT PACKARD

T-1¾ (5 mm) Diffused Solid State Lamps

Technical Data

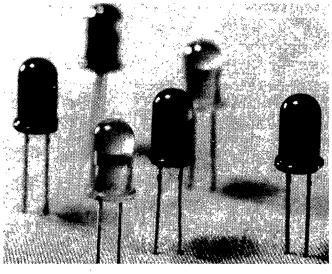
HLMP-3300 Series
HLMP-3400 Series
HLMP-3500 Series
HLMP-3762
HLMP-3862
HLMP-3962
HLMP-D400 Series
new **HLMP-D600**

Features

- **High Intensity**
- **Choice of 4 Bright Colors**
  High Efficiency Red
  Orange
  Yellow
  High Performance Green
- **Popular T-1¾ Diameter Package**
- **Selected Minimum Intensities**
- **Wide Viewing Angle**
- **General Purpose Leads**
- **Reliable and Rugged**
- **Available on Tape and Reel**

Description

This family of T-1¾ lamps is widely used in general purpose indicator applications. Diffusants, tints, and optical design are balanced to yield superior light output and wide viewing angles. Several intensity choices are available in each color for increased design flexibility.

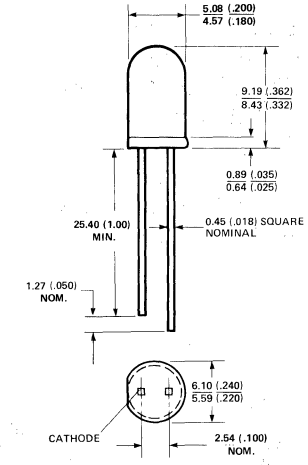


Selection Guide

Part Number HLMP-	Application	Minimum Intensity (mcd) at 10 mA	Color (Material)
3300	General Purpose	2.1	High Efficiency Red (GaAsP on GaP)
3301	High Ambient	4.0	
3762	Premium Lamp	8.0	
D400	General Purpose	2.1	Orange (GaAsP on GaP)
D401	High Ambient	4.0	
3400	General Purpose	2.2	Yellow (GaAsP on GaP)
3401	High Ambient	4.0	
3862	Premium Lamp	8.0	
3502	General Purpose	1.6	Green (GaP) 565 nm
3507	High Ambient	4.2	
3962	Premium Lamp	8.0	
D600[1]	General Purpose	1.0	Emerald Green (GaP) 558 nm

Note:
1. Please refer to Application Note 1061 for information comparing standard green and emerald green light output degradation.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Optical/Electrical Characteristics at T_A = 25°C

Symbol	Parameter	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	High Efficiency Red				mcd	I_F = 10 mA
		3300	2.1	3.5			
		3301	4.0	7.0			
		3762	8.0	12.0			
		Orange					
		D400	2.1	3.5			
		D401	4.0	7.0			
		Yellow					
		3400	2.2	4.0			
		3401	4.0	8.0			
		3862	8.0	12.0			
		Green					
		3502	1.6	2.4			
		3507	4.2	5.2			
		3962	8.0	11.0			
		Emerald Green					
		D600	1.0	3.0			
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	High Efficiency Red		60		Deg.	I_F = 10 mA See Note 1
		Orange		60			
		Yellow		60			
		Green		60			
		Emerald Green		60			
λ_{PEAK}	Peak Wavelength	High Efficiency Red		635		nm	Measurement at Peak
		Orange		600			
		Yellow		583			
		Green		565			
		Emerald Green		558			

Optical/Electrical Characteristics at T_A = 25°C (cont.)

Symbol	Parameter	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	HER/Orange Yellow Green Emerald Green		40 36 28 24		nm	
λ_d	Dominant Wavelength	High Efficiency Red Orange Yellow Green Emerald Green		626 602 585 569 560		nm	See Note 2
τ_s	Speed of Response	High Efficiency Red Orange Yellow Green Emerald Green		90 280 90 500 560		ns	
C	Capacitance	High Efficiency Red Orange Yellow Green Emerald Green		11 4 15 18 3100		pF	V_F = 0; f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance	All		260		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	HER/Orange Yellow Green Emerald Green		1.9 2.0 2.1 2.1	2.4 2.4 2.7 2.7	V	I_F = 10 mA
V_R	Reverse Breakdown Voltage	All	5.0			V	I_R = 100 μA
η_V	Luminous Efficacy	High Efficiency Red Orange Yellow Green Emerald Green	– – 	145 380 500 595 656		$\frac{\text{lumens}}{\text{Watt}}$	See Note 3

Notes:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in Watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/Watt.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	HER/Orange	Yellow	Green/ Emerald Green	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage (I_R = 100 μA)	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	500	500	mA
LED Junction Temperature	110	110	110	°C
Operating Temperature Range	-55 to +100	-55 to +100	-20 to +100	°C
Storage Temperature Range			-55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 5 seconds			

Notes:

1. See Figure 5 (Red/Orange), 10 (Yellow), or 15 (Green) to establish pulsed operating conditions.
2. For Red, Orange and Green series derate linearly from 50°C at 0.5 mA/°C. For Yellow series derate linearly from 50°C at 0.2 mA/°C.
3. 1.8 mW/°C. For Yellow series derate power linearly from 50°C at 1.6 mW/°C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

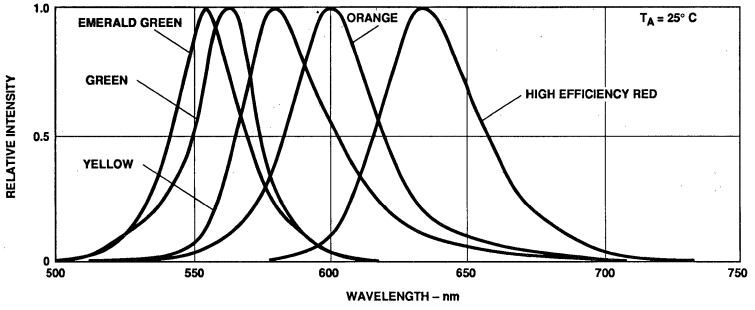


Figure 1. Relative Intensity vs. Wavelength.

T-1¾ High Efficiency Red, Orange Diffused Lamps

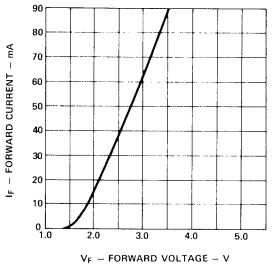


Figure 2. Forward Current vs. Forward Voltage Characteristics.

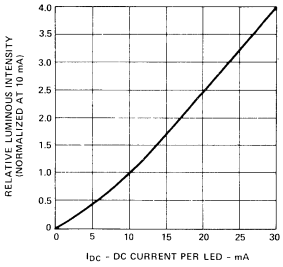


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

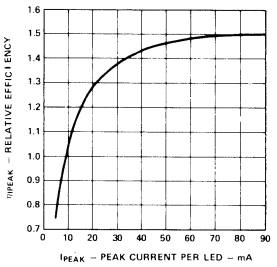


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

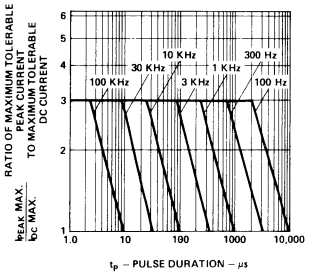


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

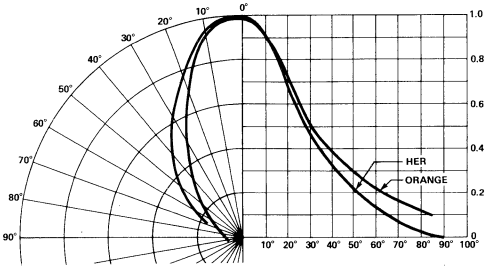


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

T-1¾ Yellow Diffused Lamps

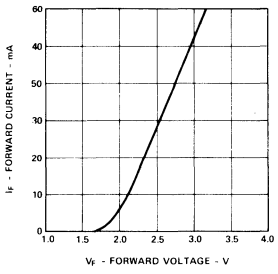


Figure 7. Forward Current vs. Forward Voltage Characteristics.

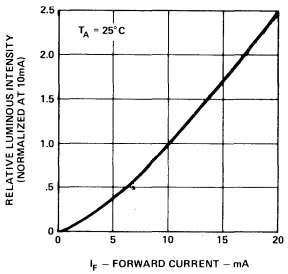


Figure 8. Relative Luminous Intensity vs. Forward Current.

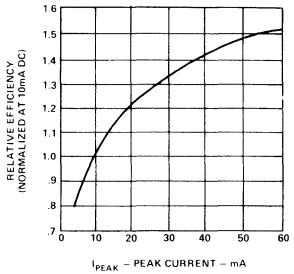


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

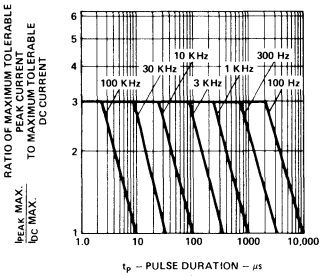


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

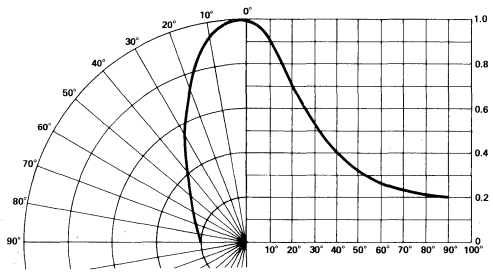


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

T-1¾ Green/Emerald Green Diffused Lamps

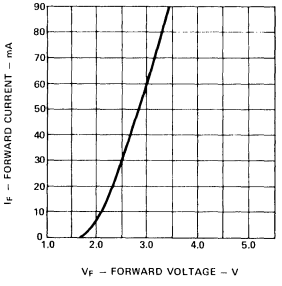


Figure 12. Forward Current vs. Forward Voltage Characteristics.

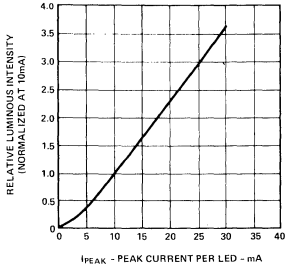


Figure 13. Relative Luminous Intensity vs. DC Forward Current.

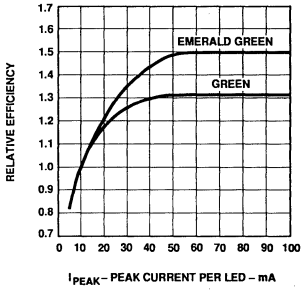


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

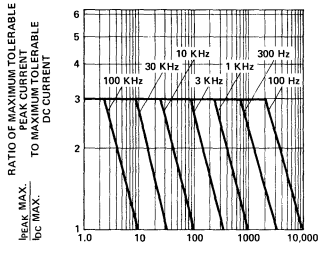


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

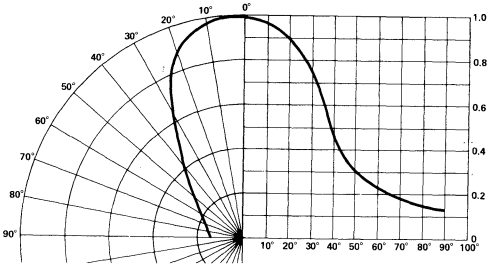


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

T-1¾ (5 mm) Low Profile Solid State Lamps

Technical Data

HLMP-320X Series
HLMP-335X Series
HLMP-336X Series
HLMP-345X Series
HLMP-346X Series
HLMP-355X Series
HLMP-356X Series

Features

- **High Intensity**
- **Low Profile: 5.8 mm (0.23 in.) Nominal**
- **T-1¾ Diameter Package**
- **Diffused and Non-diffused Types**
- **General Purpose Leads**
- **IC Compatible/Low Current Requirements**
- **Reliable and Rugged**

Description

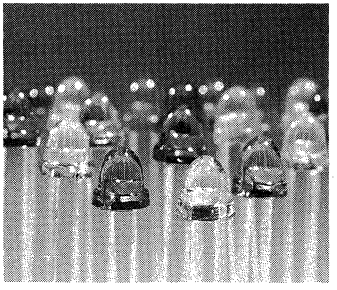
The HLMP-320X Series are Gallium Arsenide Phosphide Red Light Emitting Diodes with a red diffused lens.

The HLMP-335X/-336X Series are Gallium Arsenide Phosphide on Gallium Phosphide High Efficiency Red Light Emitting Diodes.

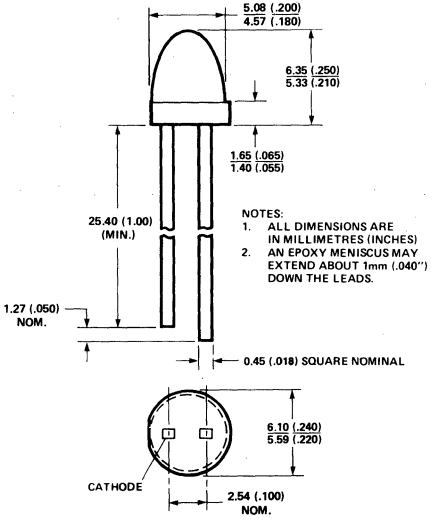
The HLMP-345X/-346X Series are Gallium Arsenide Phosphide on Gallium Phosphide Yellow Light Emitting Diodes.

The HLMP-355X/-356X Series are Gallium Phosphide Green Light Emitting Diodes.

The Low Profile T-1¾ package provides space savings and is excellent for backlighting applications.



Package Dimensions



Selection Guide

Part Number HLMP-	Application	Minimum Intensity @ 10 mA (mcd)	Lens
3200	Indicator – General Purpose	1.0[1]	Tinted Diffused Wide Angle
3201	Indicator – High Brightness	2.0[1]	Red
3350	Indicator – General Purpose	2.0	Tinted Diffused Wide Angle
3351	Indicator – High Brightness	5.0	HER
3365	General Purpose Point Source	7.0	Tinted Non-diffused Narrow Angle
3366	Indicator – High Brightness	12.0	HER
3450	Indicator – General Purpose	2.5	Tinted Diffused Wide Angle
3451	Indicator – High Brightness	6.0	Yellow
3465	General Purpose Point Source	6.0	Tinted Non-diffused Narrow Angle
3466	Indicator – High Brightness	12.0	Yellow
3553	Indicator – General Purpose	1.6	Tinted Diffused Wide Angle
3554	Indicator – High Brightness	6.7	Green
3567	General Purpose Point Source	4.2	Tinted Non-diffused Narrow Angle
3568	Indicator – High Brightness	10.6	Green

Notes:
1. I_F = 20 mA.

Red HLMP-320X/-335X Series Electrical Specifications at T_A = 25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3200 3201	1.0 2.0	2.0 4.0		mcd	I_F = 20 mA
$2\theta_{1/2}$	Including Angle Between Half Luminous Intensity Points			60		deg.	Note 1
λ_{PEAK}	Peak Wavelength			655		nm	Measurement at Peak
λ_d	Dominant Wavelength			648		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth			24		nm	
τ_s	Speed of Response			10		ns	
C	Capacitance			100		pF	V_F = 0; f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance			260		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.4	1.6	2.0	V	I_F = 20 mA
V_R	Reverse Breakdown Voltage		5.0			V	I_R = 100 µA
η_V	Luminous Efficacy			65		lm/W	See Note 3

Notes:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant Intensity, I_e, in watts/steradian may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

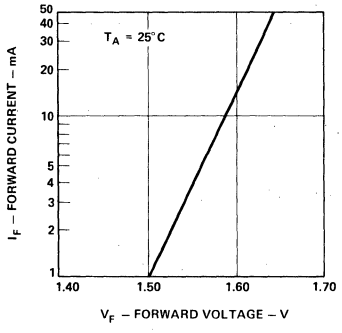


Figure 2. Forward Current vs. Forward Voltage.

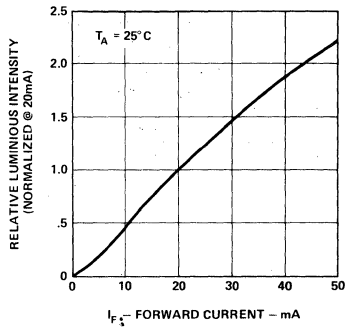


Figure 3. Relative Luminous Intensity vs. Forward Current.

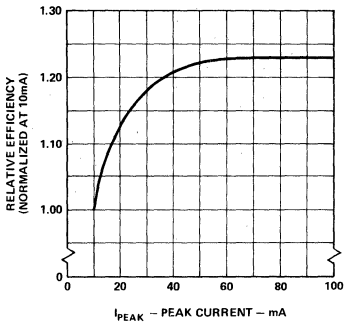


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

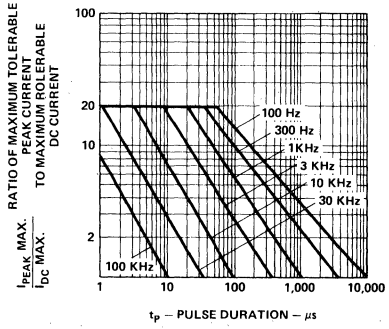


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

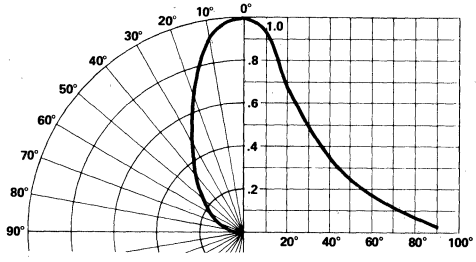


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

High Efficiency Red HLMP-335X/-336X Series Electrical Specifications at T_A = 25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3350 3351 3365 3366	2.0 5.0 7.0 12.0	3.5 7.0 10.0 18.0		mcd	I_F = 10 mA (Figure 8)
$2\theta_{1/2}$	Including Angle Between Half Luminous Intensity Points	3350 3351 3365 3366		50 50 45 45		Deg.	Note 1 (Figure 11)
λ_{PEAK}	Peak Wavelength			635		nm	Measurement at Peak (Figure 1)
λ_d	Dominant Wavelength			626		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth			40		nm	
τ_s	Speed of Response			90		ns	
C	Capacitance			11		pF	V_F = 0; f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance			260		°C/W	Junction to Cathode Lead
V_F	Forward Voltage			1.9	2.4	V	I_F = 10 mA (Figure 7)
V_R	Reverse Breakdown Voltage		5.0			V	I_R = 100 μA
η_V	Luminous Efficacy			145		lm/W	Note 3

Notes:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant Intensity, I_e, in watts/steradian may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

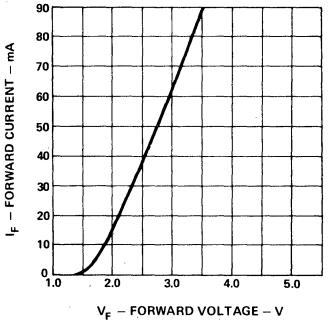


Figure 7. Forward Current vs. Forward Voltage.

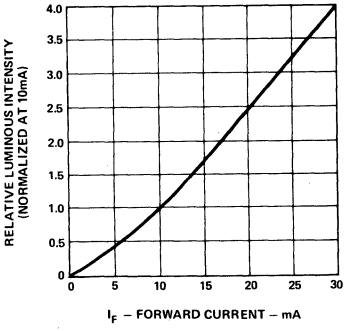


Figure 8. Relative Luminous Intensity vs. Forward Current.

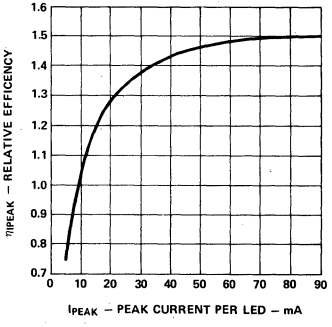


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

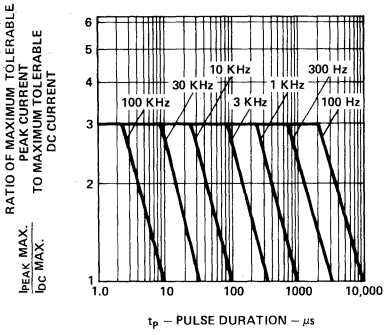


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

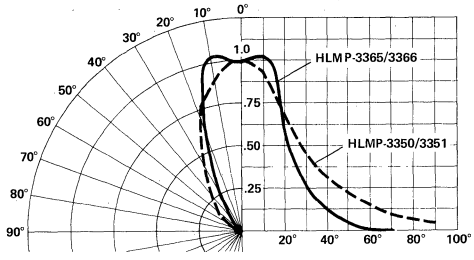


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Yellow HLMP-345X/-346X Series Electrical Specifications at T_A = 25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3450 3451 3465 3466	2.5 6.0 6.0 12.0	4.0 10.0 12.0 18.0		mcd	I_F = 10 mA (Figure 13)
$2\theta_{1/2}$	Including Angle Between Half Luminous Intensity Points	3450 3451 3465 3466		50 50 45 45		Deg.	Note 1 (Figure 16)
λ_{PEAK}	Peak Wavelength			583		nm	Measurement at Peak (Figure 1)
λ_d	Dominant Wavelength			585		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth			36		nm	
τ_s	Speed of Response			90		ns	
C	Capacitance			15		pF	V_F = 0; f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance			260		°C/W	Junction to Cathode Lead
V_F	Forward Voltage			2.0	2.4	V	I_F = 10 mA (Figure 12)
V_R	Reverse Breakdown Voltage		5.0			V	I_R = 100 μA
η_V	Luminous Efficacy			500		lm/W	Note 3

Notes:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant Intensity, I_e, in watts/steradian may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

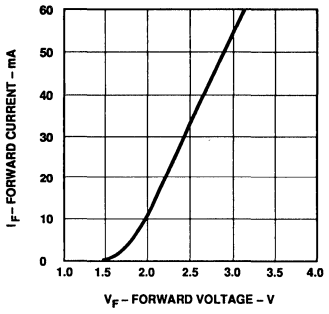


Figure 12. Forward Current vs. Forward Voltage.

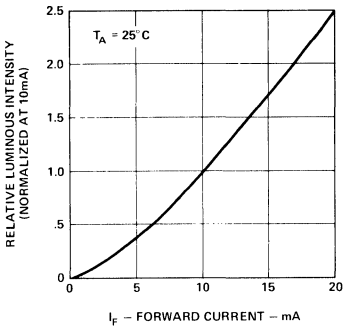


Figure 13. Relative Luminous Intensity vs. Forward Current.

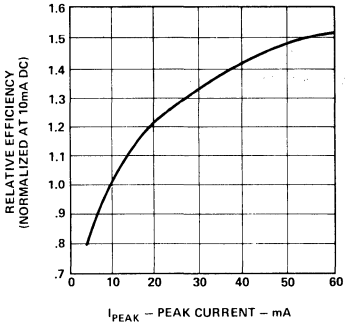


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

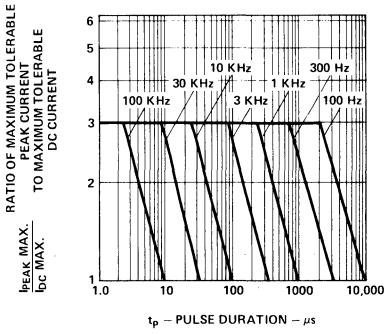


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

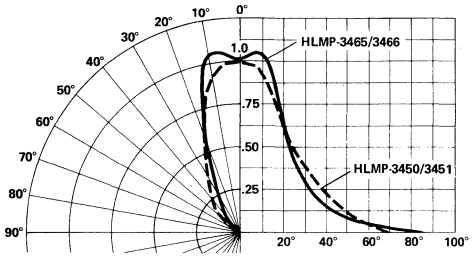


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

Green HLMP-355X/-356X Series
Electrical Specifications at T_A = 25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3553 3554 3567 3568	1.6 6.7 4.2 10.6	3.2 10.0 7.0 15.0		mcd	I_F = 10 mA (Figure 18)
$2\theta_{1/2}$	Including Angle Between Half Luminous Intensity Points	3553 3554 3567 3568		50 50 40 40		Deg.	Note 1 (Figure 21)
λ_{PEAK}	Peak Wavelength			565		nm	Measurement at Peak (Figure 1)
λ_d	Dominant Wavelength			569		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth			28		nm	
τ_s	Speed of Response			500		ns	
C	Capacitance			18		pF	V_F = 0; f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance			260		°C/W	Junction to Cathode Lead
V_F	Forward Voltage			2.1	2.7	V	I_F = 10 mA (Figure 17)
V_R	Reverse Breakdown Voltage		5.0			V	I_R = 100 μA
η_V	Luminous Efficacy			595		lm/W	Note 3

Notes:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant Intensity, I_e, in watts/steradian may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

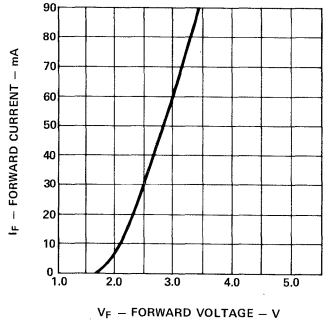


Figure 17. Forward Current vs. Forward Voltage.

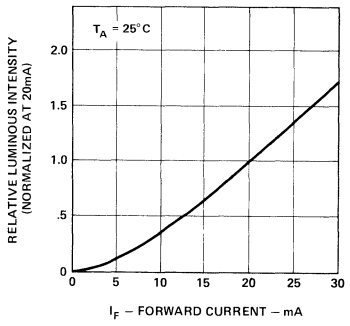


Figure 18. Relative Luminous Intensity vs. Forward Current.

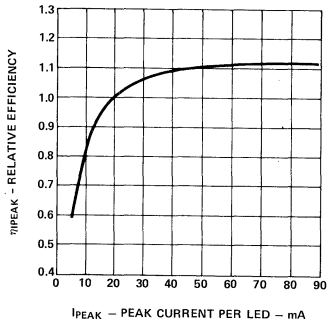


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

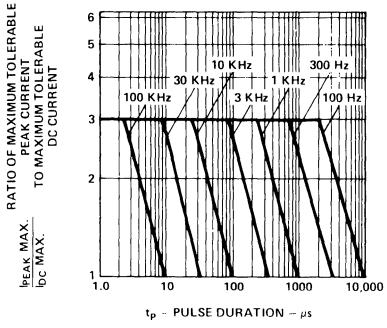


Figure 20. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

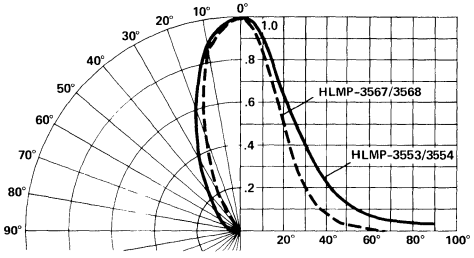


Figure 21. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

T-1¾ (5 mm) Red Solid State Lamps

Technical Data

HLMP-3000
HLMP-3001
HLMP-3002
HLMP-3003
HLMP-3050

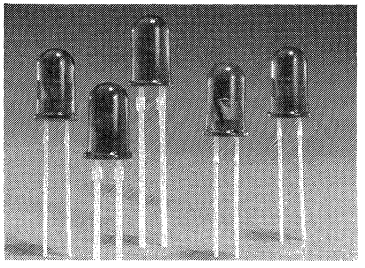
Features

- **Low Cost, Broad Applications**
- **Long Life, Solid State Reliability**
- **Low Power Requirements: 20 mA @ 1.6 V**
- **High Light Output:**
  2.0 mcd Typical for HLMP-3000
  4.0 mcd Typical for HLMP-3001
- **Wide and Narrow Viewing Angle Types**
- **Red Diffused and Non-diffused Versions**

Description

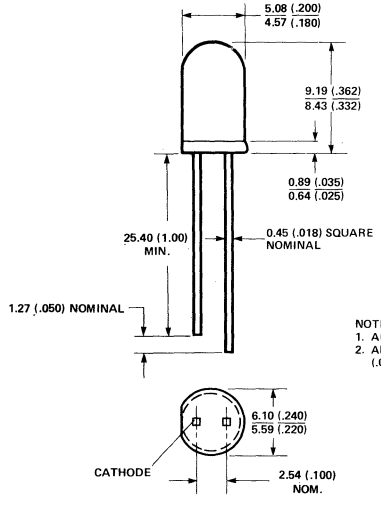
The HLMP-3000 series lamps are Gallium Arsenide Phosphide light emitting diodes intended for High Volume/Low Cost applications such as indicators for appliances, smoke detectors, automobile instrument panels, and many other commercial uses.

The HLMP-3000/-3001/-3002/-3003 have red diffused lenses whereas the HLMP-3050 has a red non-diffused lens. These lamps can be panel mounted using mounting clip



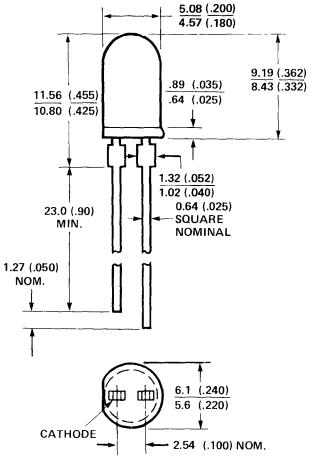
HLMP-0103. The HLMP-3000/-3001 lamps have 0.025" leads and the HLMP-3002/-3003/-3050 have 0.018" leads.

Package Dimensions



HLMP-3002/-3003/-3050

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.



HLMP-3000/-3001

Absolute Maximum Ratings at T_A = 25°C

Parameter	3000 Series	Units
Power Dissipation	100	mW
DC Forward Current (Derate linearly from 50°C at 0.2 mA/°C)	50	mA
Average Forward Current	50	mA
Peak Operating Forward Current	1000	mA
Reverse Voltage (I_R = 100 μA)	5	V
Transient Forward Current[1] (10 μsec Pulse)	2000	mA
LED Junction Temperature	110	°C
Operating and Storage Temperature Range	-55°C to +100°C	
Lead Solder Temperature (1.6 mm [0.063 inch] below package base)	260°C for 5 seconds	

Note:

1. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

Electrical Characteristics at T_A = 25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	3000/3002 3001/3003 3050	1.0 2.0 1.0	2.0 4.0 2.5		mcd mcd mcd	I_F = 20 mA I_F = 20 mA I_F = 20 mA
$2\theta_{1/2}$	Including Angle Between Half Luminous Intensity Points	3000/3002 3001/3003 3050		60 60 24		Deg.	I_F = 20 mA
λ_P	Peak Wavelength	3000/3002 3001/3003 3050		655 655 655		nm	Measurement at Peak
λ_d	Dominant Wavelength	3000/3002 3001/3003 3050		648		nm	
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	3000/3002 3001/3003 3050		24		nm	
τ_s	Speed of Response	3000/3002 3001/3003 3050		10		ns	
C	Capacitance	3000/3002 3001/3003 3050		100		pF	V_F = 0, f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance	3000/3001 3002/3003 3050		210 260 260		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	3000/3002 3001/3003 3050	1.4	1.6	2.0	V	I_F = 20 mA (Fig. 2)
V_R	Reverse Breakdown Voltage	3000/3002 3001/3003 3050	5.0			V	I_R = 100 μA

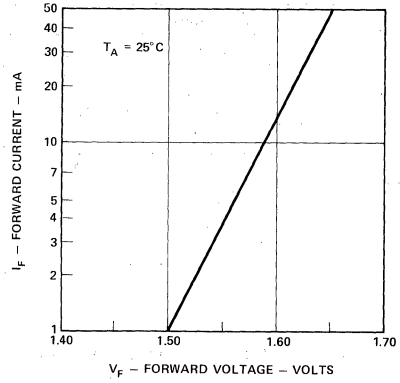


Figure 1. Forward Current vs. Forward Voltage.

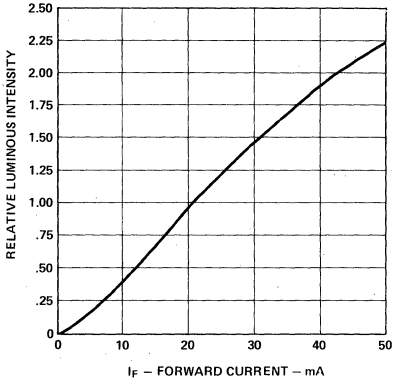


Figure 2. Relative Luminous Intensity vs. Forward Current.

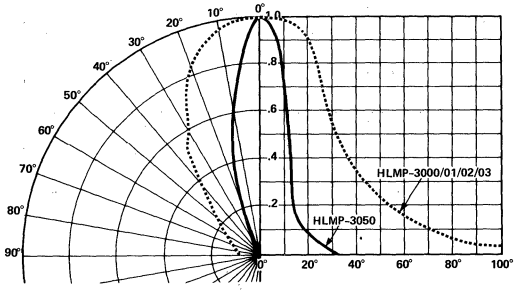


Figure 3. Relative Luminous Intensity vs. Angular Displacement.

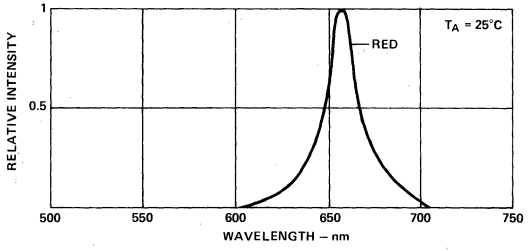


Figure 4. Relative Luminous Intensity vs. Wavelength.

HEWLETT PACKARD

T-1 (3 mm) High Intensity Solid State Lamps

Technical Data

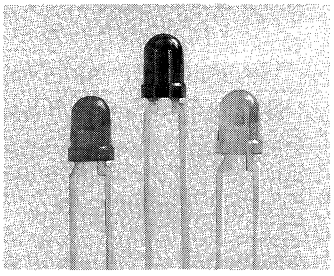
HLMP-132X Series
HLMP-142X Series
HLMP-152X Series

Features

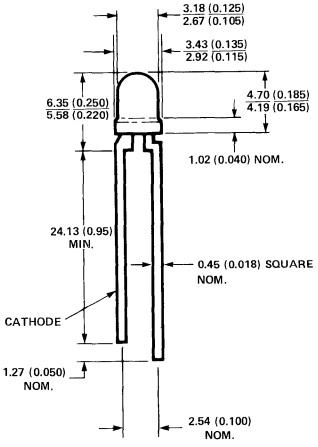
- **High Intensity**
- **Choice of 3 Bright Colors**
  High Efficiency Red
  Yellow
  High Performance Green
- **Popular T-1 Diameter Package**
- **Selected Minimum Intensities**
- **Narrow Viewing Angle**
- **General Purpose Leads**
- **Reliable and Rugged**
- **Available on Tape and Reel**

Description

This family of T-1 lamps is specially designed for applications requiring higher on-axis intensity than is achievable with a standard lamp. The light generated is focused to a narrow beam to achieve this effect.



Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (0.040") DOWN THE LEADS.

Selection Guide

Part Number HLMP-	Description	Minimum Intensity (mcd) at 10 mA	Color (Material)
1320	Untinted Non-diffused	8.6	High Efficiency Red (GaAsP on GaP)
1321	Tinted Non-diffused	8.6	
1420	Untinted Non-diffused	9.2	Yellow (GaAsP on GaP)
1421	Tinted Non-diffused	6.0	
1520	Untinted Non-diffused	4.2	Green (GaP)
1521	Tinted Non-diffused	4.2	

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	Red	Yellow	Green	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage (I_R = 100 μA)	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	500	500	mA
LED Junction Temperature	110	110	110	°C
Operating Temperature Range	-55 to +100	-55 to +100	-20 to +100	°C
Storage Temperature Range			-55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 5 seconds			

Notes:

1. See Figure 5 (Red), 10 (Yellow), or 15 (Green) to establish pulsed operating conditions.
2. For Red and Green series derate linearly from 50°C at 0.5 mA/°C. For Yellow series derate linearly from 50°C at 0.2 mA/°C.
3. For Red and Green series derate power linearly from 25°C at 1.8 mW/°C. For Yellow series derate power linearly from 50°C at 1.6 mW/°C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

Electrical Characteristics at $T_A = 25°C$

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	1320 1321	8.6 8.6	12.0 12.0		mcd	I_F = 10 mA (Figure 3)
		1420 1421	9.2 6.0	12.0 12.0		mcd	I_F = 10 mA (Figure 8)
		1520 1521	4.2 4.2	12.0 12.0		mcd	I_F = 10 mA (Figure 3)
$2\theta_{1/2}$	Including Angle Between Half Luminous Intensity Points	All		45		Deg.	I_F = 10 mA See Note 1 (Figures 6, 11, 16, 21)
λ_{PEAK}	Peak Wavelength	132X 142X 152X		635 583 565		nm	Measurement at Peak (Figure 1)
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	132X 142X 152X		40 36 28		nm	
λ_d	Dominant Wavelength	132X 142X 152X		626 585 569		nm	See Note 2 (Figure 1)
τ_s	Speed of Response	132X 142X 152X		90 90 500		ns	
C	Capacitance	132X 142X 152X		11 15 18		pF	V_F = 0; f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance	All		290		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	132X 142X 152X		1.9 2.0 2.1	2.4 2.4 2.7	V	I_F = 10 mA
V_R	Reverse Breakdown Voltage	All	5.0			V	I_R = 100 μA
η_V	Luminous Efficacy	132X 142X 152X		145 500 595		$\frac{\text{lumens}}{\text{Watt}}$	See Note 3

Notes:

1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

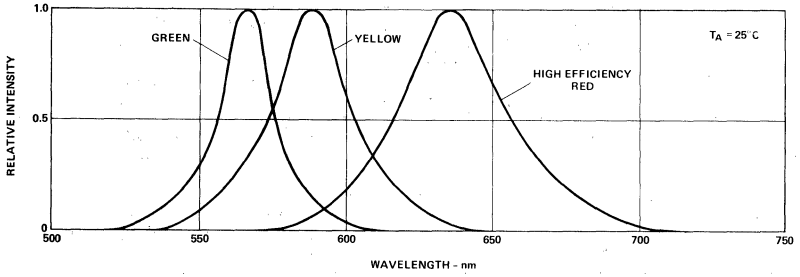


Figure 1. Relative Intensity vs. Wavelength.

T-1 High Efficiency Red Non-Diffused

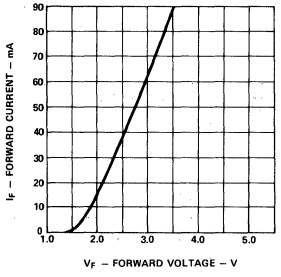


Figure 2. Forward Current vs. Forward Voltage Characteristics.

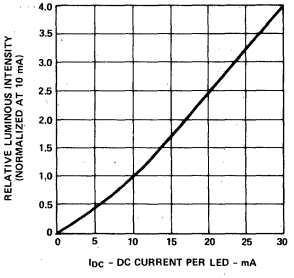


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

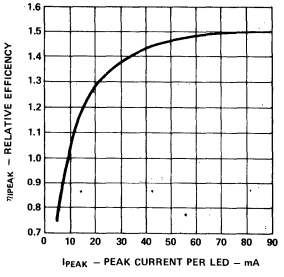


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

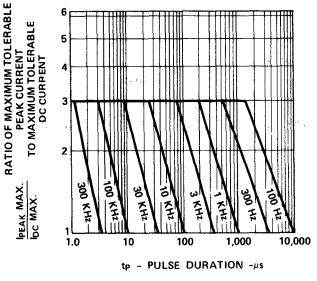


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

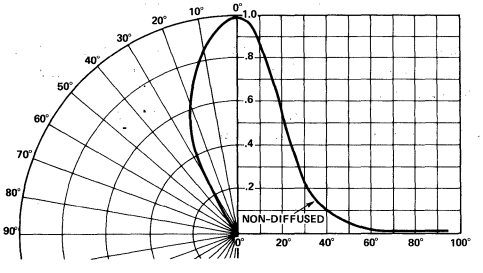


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

T-1 Yellow Non-Diffused

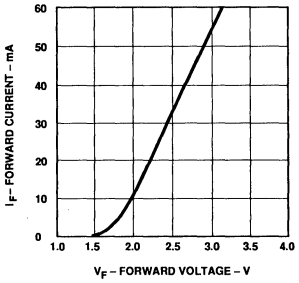


Figure 7. Forward Current vs. Forward Voltage Characteristics.

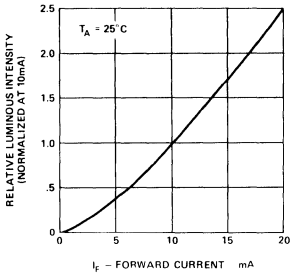


Figure 8. Relative Luminous Intensity vs. Forward Current.

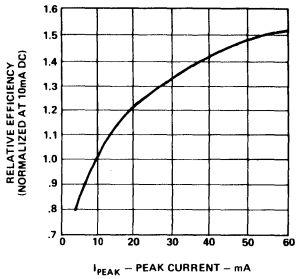


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

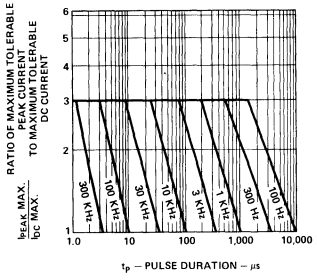


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC}MAX as per MAX Ratings)

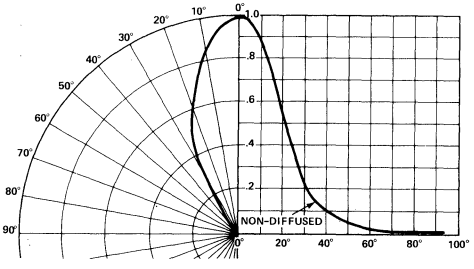


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

T-1 Green Non-Diffused

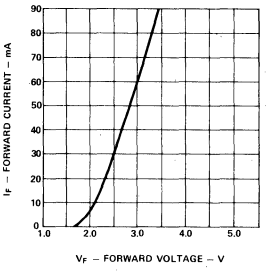


Figure 12. Forward Current vs. Forward Voltage Characteristics.

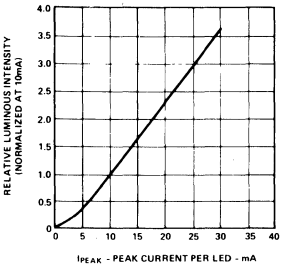


Figure 13. Relative Luminous Intensity vs. Forward Current.

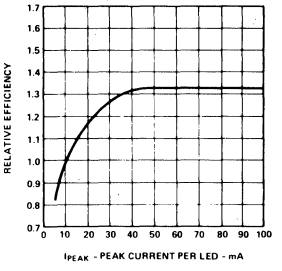


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

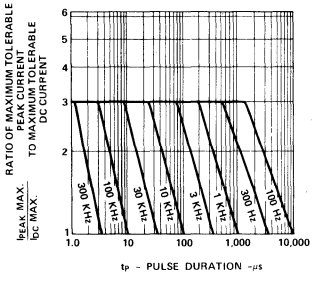


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC}MAX as per MAX Ratings)

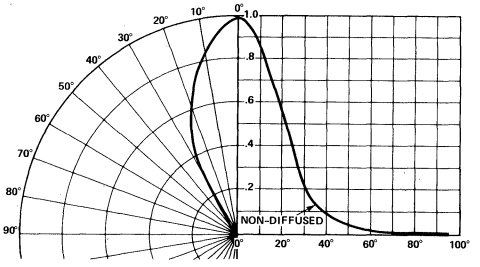


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

T-1 (3 mm) Diffused Solid State Lamps

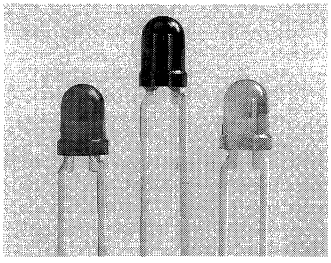
Technical Data

HLMP-130X Series
HLMP-1385
HLMP-K40X Series
HLMP-140X Series
HLMP-1485
HLMP-1503
HLMP-1523
HLMP-1585
New **HLMP-K600**

SOLID STATE LAMPS

Features

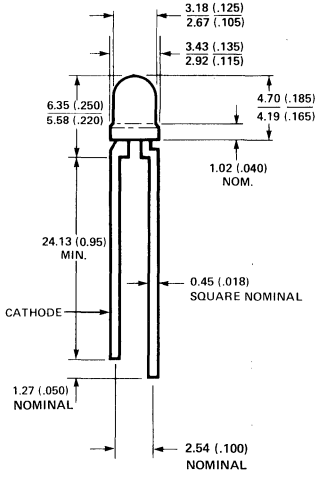
- **High Intensity**
- **Choice of 4 Bright Colors**
  High Efficiency Red
  Orange
  Yellow
  High Performance Green
- **Popular T-1 Diameter Package**
- **Selected Minimum Intensities**
- **Wide Viewing Angle**
- **General Purpose Leads**
- **Reliable and Rugged**
- **Available on Tape and Reel**



Description

This family of T-1 lamps is widely used in general purpose indicator applications. Diffusants, tints, and optical design are balanced to yield superior light output and wide viewing angles. Several intensity choices are available in each color for increased design flexibility.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Part Number HLMP-	Application	Minimum Intensity (mcd) at 10 mA	Color (Material)
1300	General Purpose	1.0	High Efficiency Red (GaAsP on GaP)
1301	General Purpose	2.0	
1302	High Ambient	3.0	
1385	Premium Lamp	6.0	
K400	General Purpose	1.0	Orange (GaAsP on GaP)
K401	High Ambient	2.0	
K402	Premium Lamp	3.0	
1400	General Purpose	1.0	Yellow (GaAsP on GaP)
1401	General Purpose	2.0	
1402	High Ambient	3.0	
1485	Premium Lamp	6.0	
1503	General Purpose	1.0	Green (GaP)
1523	High Ambient	2.6	
1585	Premium Lamp	4.0	
K600[1]	General Purpose	1.0	Emerald Green (GaP)

Note:
1. Please refer to Application Note 1061 for information comparing standard green and emerald green light output degradation.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	HER/Orange	Yellow	Green	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Reverse Voltage (I_R = 100 µA)	5	5	5	V
Transient Forward Current[4] (10 µsec Pulse)	500	500	500	mA
LED Junction Temperature	110	110	110	°C
Operating Temperature Range	-55 to +100	-55 to +100	-20 to +100	°C
Storage Temperature Range			-55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 5 seconds			

Notes:

1. See Figure 5 (HER/Orange), 10 (Yellow), or 15 (Green/Emerald Green) to establish pulsed operating conditions.
2. For Red, Orange, and Green series derate linearly from 50°C at 0.5 mA/°C. For Yellow series derate linearly from 50°C at 0.2 mA/°C.
3. For Red, Orange, and Green series derate power linearly from 25°C at 1.8 mW/°C. For Yellow series derate power linearly from 50°C at 1.6 mW/°C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

Electrical Characteristics at $T_A = 25°C$

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	High Efficiency Red				mcd	I_F = 10 mA
		1300	1.0	5.0			
		1301	2.0	5.5			
		1302	3.0	7.0			
		1385	6.0	10.0			
		Orange					
		K400	1.0	4.0			
		K401	2.0	5.0			
		K402	3.0	6.5			
		Yellow					
		1400	1.0	5.0			
		1401	2.0	6.0			
		1402	3.0	7.0			
		1485	6.0	10.0			
		Green					
		1503	1.0	5.0			
		1523	2.6	7.0			
		1585	4.0	8.5			
		Emerald Green					
		K600	1.0	4.5			

Electrical Characteristics at T_A = 25°C (cont.)

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	All		60		Deg.	I_F = 10 mA See Note 1
λ_{PEAK}	Peak Wavelength	High Efficiency Red Orange Yellow Green Emerald Green		635 600 583 565 558		nm	Measurement at Peak
λ_d	Dominant Wavelength	High Efficiency Red Orange Yellow Green Emerald Green		626 602 585 569 560		nm	See Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	High Efficiency Red Yellow Green Emerald Green		40 36 28 24		nm	
τ_s	Speed of Response	High Efficiency Red Orange Yellow Green Emerald Green		90 280 90 500 3100		ns	
C	Capacitance	High Efficiency Red Orange Yellow Green Emerald Green		11 4 15 18 35		pF	V_F = 0; f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance	All		290		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	HER/Orange Yellow Green Emerald Green	1.5 1.5 1.5	1.9 2.0 2.1 2.1	2.4 2.4 2.7 2.7	V	I_F = 10 mA
V_R	Reverse Breakdown Voltage	All	5.0			V	I_R = 100 μA
η_V	Luminous Efficacy	High Efficiency Red Orange Yellow Green Emerald Green		145 380 500 595 655		lumens / Watt	See Note 3

Notes:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

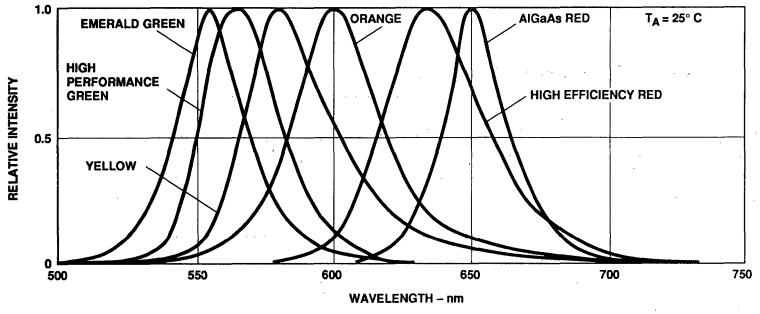


Figure 1. Relative Intensity vs. Wavelength.

T-1 High Efficiency Red, Orange Diffused Lamps

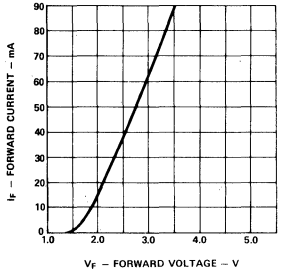


Figure 2. Forward Current vs. Forward Voltage Characteristics.

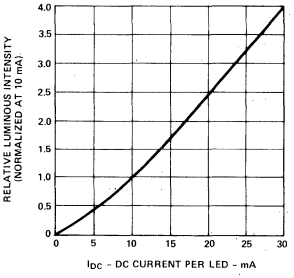


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

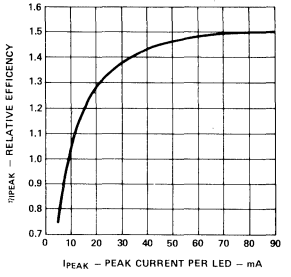


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

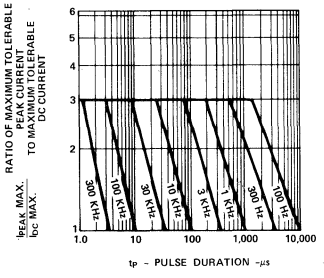


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

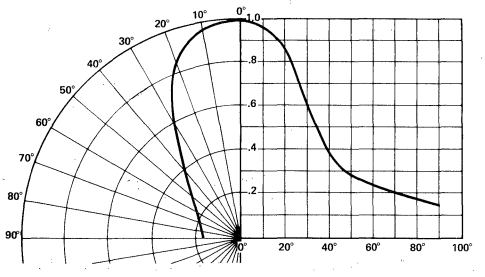


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

T-1 Yellow Diffused Lamps

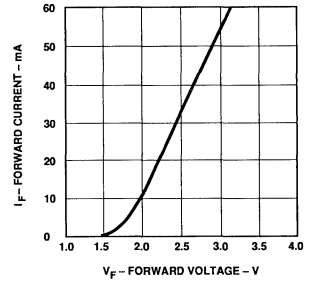


Figure 7. Forward Current vs. Forward Voltage Characteristics.

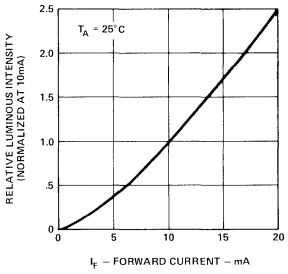


Figure 8. Relative Luminous Intensity vs. Forward Current.

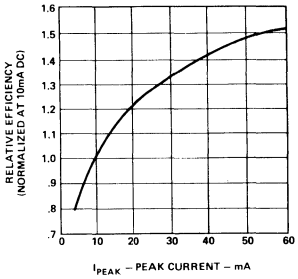


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

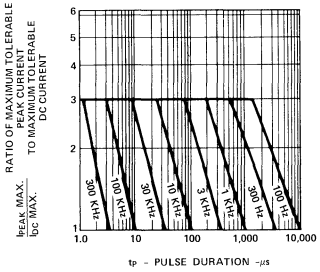


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

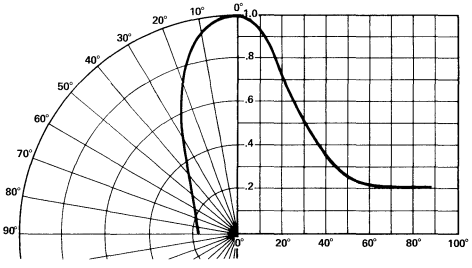


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

T-1 Green/Emerald Green Diffused Lamps

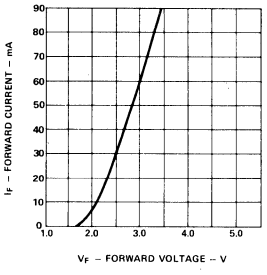


Figure 12. Forward Current vs. Forward Voltage Characteristics.

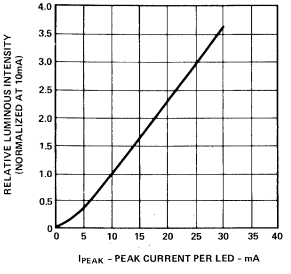


Figure 13. Relative Luminous Intensity vs. Forward Current.

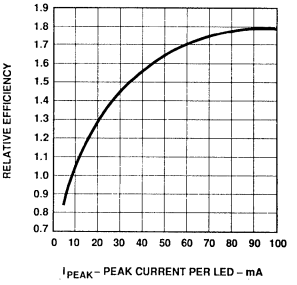


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

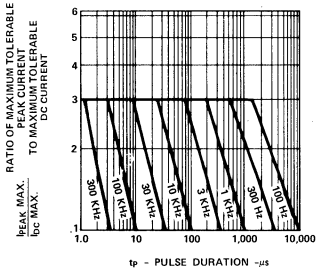


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

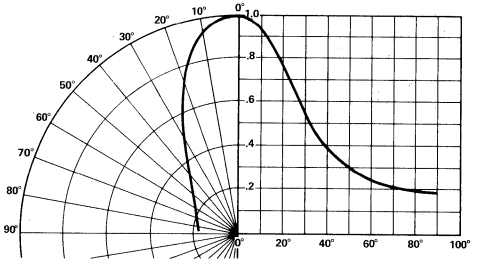


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

Red Solid State T-1 (3 mm) Lamps

Technical Data

HLMP-100X Series
HLMP-1071
HLMP-1080
HLMP-120X Series

Features

- **Wide Viewing Angle**
- **Small Size T-1 Diameter 3.18 mm (0.125")**
- **IC Compatible**
- **Reliable and Rugged**

Description

The HLMP-1000 is a series of Gallium Arsenide Phosphide Light Emitting Diodes designed for applications where space is at a premium, such as in high density arrays.

The HLMP-1000 series is available in three lens configurations.

HLMP-1000 – Red Diffused lens provides excellent on-off contrast ratio, high axial luminous intensity, and wide viewing angle.

HLMP-1080 – Same as HLMP-1000, but untinted diffused to mask red color in the "off" condition.

HLMP-1071/-1201 – Untinted non-diffused plastic lens provides a point source. Useful when illuminating external lens, annunciators, or photo-detectors.

Package Dimensions

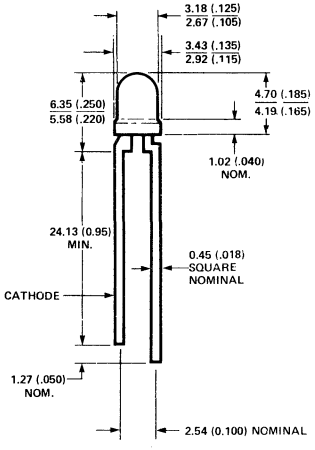


Figure A

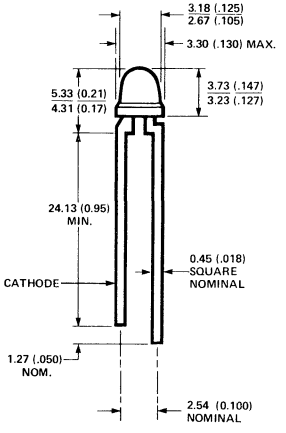


Figure B

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Selection Guide

Part Number HLMP-	Package & Lens Type	I_v (mcd) @ 20 mA		Typical Viewing Angle $2\theta_{1/2}$
		Min.	Typ.	
1000	A-Tinted Diffused	0.5	1.0	60°
1002	A-Tinted Diffused	1.5	2.5	60°
1080	A-Untinted Diffused	0.5	1.5	60°
1071	A-Untinted Non-Diffused	1.0	2.0	45°
1200	B-Untinted Non-Diffused	0.5	1.0	55°
1201	B-Untinted Non-Diffused	1.5	2.5	55°

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	1000 Series	Units
Power Dissipation	100	mW
DC Forward Current[1]	50	mA
Average Forward Current	50	mA
Peak Operating Forward Current	1000	mA
Reverse Voltage (I_R = 100 μA)	5	V
Transient Forward Current[1] (10 μs Pulse)	2000	mA
LED Junction Temperature	110	°C
Operating and Storage Temperature Range	-55 to +100°C	
Lead Soldering Temperature (1.6 mm [0.063 in.] below package base)	260°C for 5 seconds	

Note:
1. Derate linearly from 50°C at 0.2 mA/°C.

Electrical Characteristics at $T_A = 25°C$

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions
λ_{PEAK}	Peak Wavelength		655		nm	Measurement at Peak
λ_d	Dominant Wavelength		648		nm	
$\Delta\lambda 1/2$	Spectral Line Halfwidth		24		nm	
τ_S	Speed of Response		10		ns	
C	Capacitance		100		pF	$V_F = 0$, f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance		290		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	1.4	1.6	2.0	V	$I_F = 20$ mA
V_R	Reverse Breakdown Voltage	5			V	$I_R = 100\ \mu A$

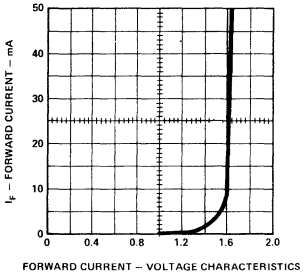


Figure 1. Forward Current vs. Voltage Characteristic.

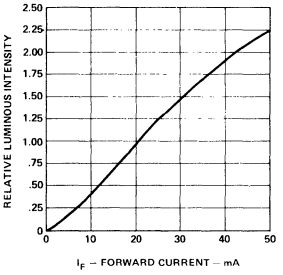


Figure 2. Luminous Intensity vs. Forward Current (IF).

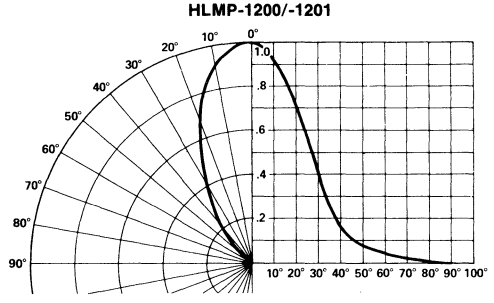


Figure 3. Typical Relative Luminous Intensity vs. Angular Displacement.

HLMP-1000/-1002/-1080

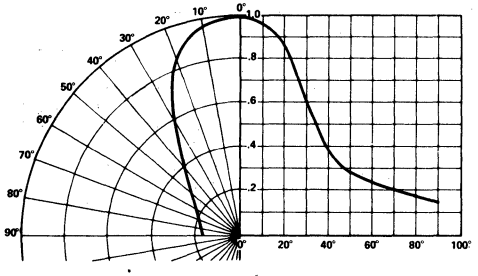


Figure 4. Relative Luminous Intensity vs. Angular Displacement.

HLMP-1071

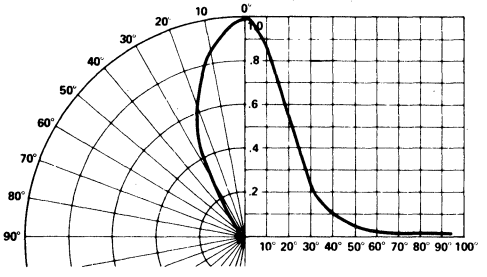


Figure 5. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

Rectangular Solid State Lamps

Technical Data

HLMP-R100
HLMP-0300/0301
HLMP-0400/0401
HLMP-0503/0504

Features

- **Rectangular Light Emitting Surface**
- **Flat High Sterance Emitting Surface**
- **Stackable on 2.54 mm (0.100 inch) Centers**
- **Ideal as Flush Mounted Panel Indicators**
- **Ideal for Backlighting Legends**
- **Long Life: Solid State Reliability**
- **Choice of 4 Bright Colors**
  - DH AS AlGaAs Red
  - High Efficiency Red
  - Yellow
  - High Performance Green
- **IC Compatible/Low Current Requirements**

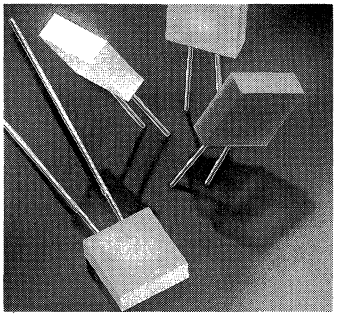
Description

The HLMP–R100, -030X, -040X, -050X are solid state lamps encapsulated in a radial lead rectangular epoxy package. They utilize a tinted, diffused epoxy to provide high on-off contrast and a flat high intensity emitting surface. Borderless package design allows creation of uninterrupted light emitting areas.

The HLMP-R100 uses a double heterojunction (DH) absorbing substrate (AS) aluminum gallium arsenide (AlGaAs) red LED chip in a light red epoxy package. This combination produces outstanding light output over a wide range of drive currents.

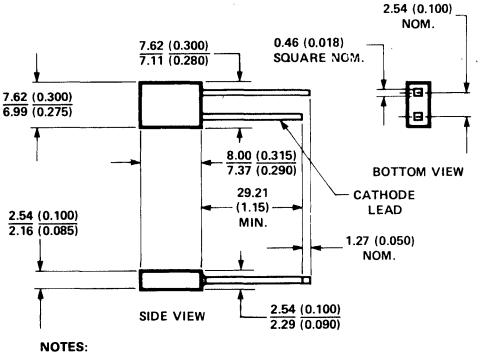
The HLMP-0300 and -0301 have a high efficiency red GaAsP on GaP LED chip in a light red epoxy package.

The HLMP-0400 and -0401 provide a yellow GaAsP on GaP LED chip in a yellow epoxy package.



The HLMP-0503 and -0504 provide a green GaP LED chip in a green epoxy package.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.
3. THERE IS A MAXIMUM 1° TAPER FROM BASE TO TOP OF LAMP.

Axial Luminous Intensity

Color	Part Number	I_v (mcd) @ 20 mA DC	
		Min.	Typ.
AlGaAs Red	HLMP-R100	3.4	7.5
High Efficiency Red	HLMP-0300	1.0	2.5
	HLMP-0301	2.5	5.0
Yellow	HLMP-0400	1.5	2.5
	HLMP-0401	3.0	5.0
High Performance Green	HLMP-0503	1.5	2.5
	HLMP-0504	3.0	5.0

Absolute Maximum Ratings at T_A = 25°C

Parameter	HLMP-R100	HLMP-0300/-0301	HLMP-0400/0401	HLMP-0503/-0504	Units
Peak Forward Current	300	90	60	90	mA
Average Forward Current[1]	20	25	20	25	mA
DC Current[2]	30	30	20	30	mA
Power Dissipation	87	135	85	135	mW
Reverse Voltage (I_R = 100 μA)	5	5	5	5	V
Transient Forward Current[3] (10 μs Pulse)	500	500	500	500	mA
Operating Temperature Range	-20 to +100	-55 to +100	-55 to +100	-20 to +100	°C
Storage Temperature Range	-55 to +100			-55 to +100	
Lead Soldering Temperature (1.6 mm [0.063 in.] from body)	260°C for 5 seconds				

Notes:
1. See Figure 5 to establish pulsed operating conditions.
2. For AlGaAs Red, Red, and Green Series derate linearly from 50°C at 0.5 mA/°C. For Yellow Series derate linearly from 50°C at 0.2 mA/°C.
3. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak current beyond the peak forward current listed in the Absolute Maximum Ratings.

Electrical/Optical Characteristics at $T_A = 25°C$

Sym.	Description	HLMP-R100			HLMP -0300/-0301			HLMP -0400/-0401			HLMP -0503/-0504			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		100			100			100			100		Deg.	Note 1. Fig. 6
λ_p	Peak Wavelength		645			635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		637			626			585			569		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth		20			40			36			28		nm	
τ_s	Speed of Response		30			90			90			500		ns	
C	Capacitance		30			16			18			18		pF	$V_F = 0$; f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance		260			260			260			260		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.8	2.2		1.9	2.6		2.1	2.6		2.2	3.0	V	$I_F = 20$ mA Figure 2.
V_R	Reverse Breakdown Voltage	5.0			5.0			5.0			5.0			V	$I_R = 100\ \mu A$
η_v	Luminous Efficacy		80			145			500			595		lm/W	Note 3

Notes:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

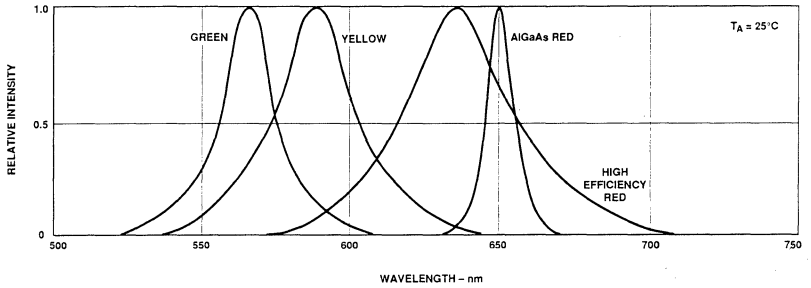


Figure 1. Relative Intensity vs. Wavelength.

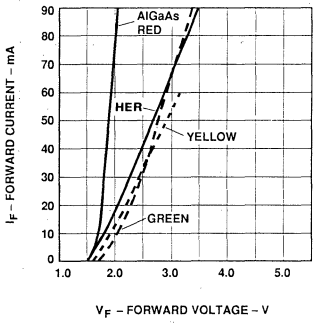


Figure 2. Forward Current vs. Forward Voltage. V_p (300 mA) for AlGaAs Red = 2.6 Volts Typical.

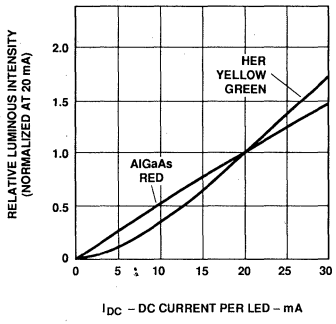


Figure 3. Relative Luminous Intensity vs. Forward Current.

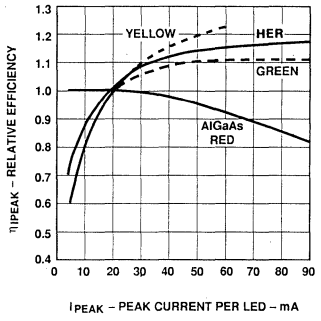
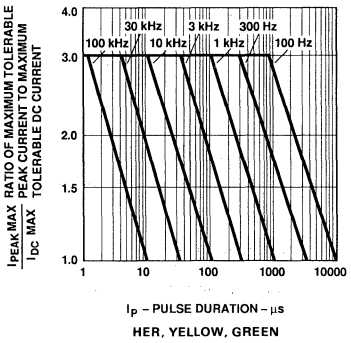


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current. η_v (300 mA) for AlGaAs Red = 0.7.



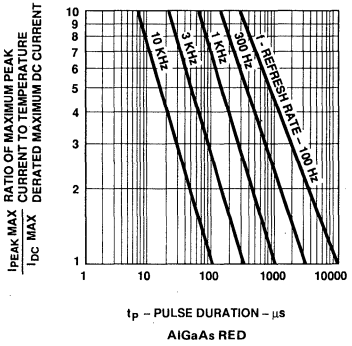


Figure 5. Maximum Tolerable Peak Current vs. Peak Duration (I_{PEAK} MAX Determined from Temperature Derated I_{DC} MAX).

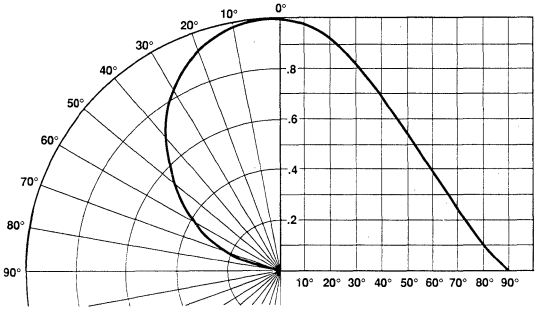


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

2 mm x 5 mm Rectangular Lamps

Technical Data

HLMP-S100
HLMP-S20X Series
HLMP-S30X Series
HLMP-S40X Series
HLMP-S50X Series
new **HLMP-S600**

Features

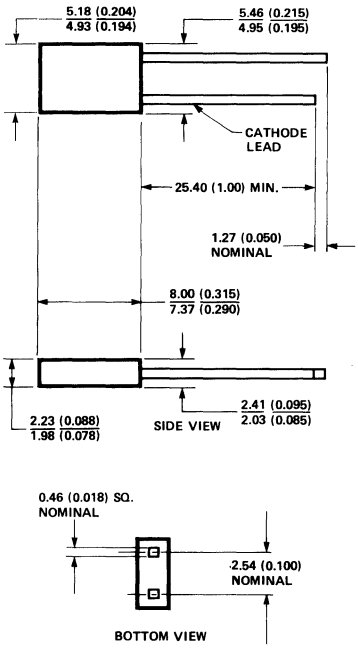
- **Rectangular Light Emitting Surface**
- **Excellent for Flush Mounting on Panels**
- **Choice of Five Bright Colors**
- **Long Life: Solid State Reliability**
- **Excellent Uniformity of Light Output**

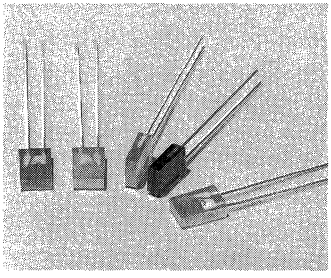
Description

The HLMP-S100, -S200, -S300, -S400, -S500, S600 are epoxy encapsulated lamps in rectangular packages which are easily stacked in arrays or used for discrete front panel indicators. Contrast and light uniformity are enhanced by a special epoxy diffusion and tinting process.

The HLMP-S100 uses double heterojunction (DH) absorbing substrate (AS) aluminum gallium arsenide (AlGaAs) LEDs to produce outstanding light output over a wide range of drive currents.

Package Dimensions





NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES)
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.
3. THERE IS A MAXIMUM 1° TAPER FROM BASE TO THE TOP OF LAMP.

Electrical/Optical Characteristics at $T_A = 25°C$

Sym.	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_v	Luminous Intensity	AlGaAs Red				mcd	$I_F = 20$ mA
		S100	3.6	7.5			
		High Efficiency Red					
		S200	2.1	3.5			
		S201	3.4	4.8			
		Orange					
		S400	2.1	3.5			
		S401	3.4	4.8			
		Yellow					
		S300	1.4	2.1			
		S301	2.2	3.5			
		Green					
		S500	2.6	4.0			
		S501	4.1	5.8			
		Emerald Green					
		S600[4]	1.0	3.0			
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	All		110		Deg.	$I_F = 20$ mA See Note 1
λ_{PEAK}	Peak Wavelength	AlGaAs Red		645		nm	Measurement at Peak
		High Efficiency Red		635			
		Orange		600			
		Yellow		583			
		Green		565			
		Emerald Green		558			
λ_d	Dominant Wavelength	AlGaAs Red		637		nm	See Note 2 Time const, e^{-t/τ_s}
		High Efficiency Red		626			
		Orange		602			
		Yellow		585			
		Green		569			
		Emerald Green		560			
τ_s	Speed of Response	AlGaAs Red		30		ns	
		High Efficiency Red		90			
		Orange		280			
		Yellow		90			
		Green		500			
		Emerald Green		3100			
C	Capacitance	AlGaAs Red		30		pF	$V_F = 0$; f = 1 MHz
		High Efficiency Red		11			
		Orange		4			
		Yellow		15			
		Green		18			
		Emerald Green		35			
$R\theta_{J\text{-}PIN}$	Thermal Resistance	All		260		°C/W	Junction to Cathode Lead at Seating Plane
V_F	Forward Voltage	AlGaAs Red	1.6	1.8	2.2	V	$I_F = 20$ mA
		HER/Orange	1.5	1.9	2.6		
		Yellow	1.5	2.1	2.6		
		Green/Emerald Green	1.5	2.2	3.0		
V_R	Reverse Breakdown Voltage	All	5.0			V	$I_R = 100$ µA

Electrical/Optical Characteristics at T_A = 25°C contd.

Sym.	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
η_V	Luminous Efficacy	AlGaAs Red		80		lumens/ watt	See Note 3
		High Efficiency Red		145			
		Orange		380			
		Yellow		500			
		Green		595			
		Emerald Green		656			

Notes:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.
4. Please refer to Application Note 1061 for information comparing standard green and emerald green light output degradation.

Absolute Maximum Ratings at T_A = 25°C

Parameter	AlGaAs Red	High Efficiency Red/Orange	Yellow	Green/ Emerald Green	Units
Peak Forward Current	300	90	60	90	mA
Average Forward Current[1]	20	25	20	25	mA
DC Current[2]	30	30	20	30	mA
Transient Forward Current[3] (10 µsec Pulse)	500				mA
LED Junction Temperature	110	110	110	110	°C
Operating Temperature Range	-20 to +100	-55 to +100	-55 to +100	-20 to +100	°C
Storage Temperature Range	-55 to +100			-55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) below seating plane]	260°C for 5 seconds				

Notes:
1. See Figure 5 to establish pulsed operating conditions.
2. For AlGaAs Red, Red, Orange, and Green series derate linearly from 50°C at 0.5 mA/°C. For Yellow series derate linearly from 50°C at 0.34 mA/°C.
3. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wire bond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

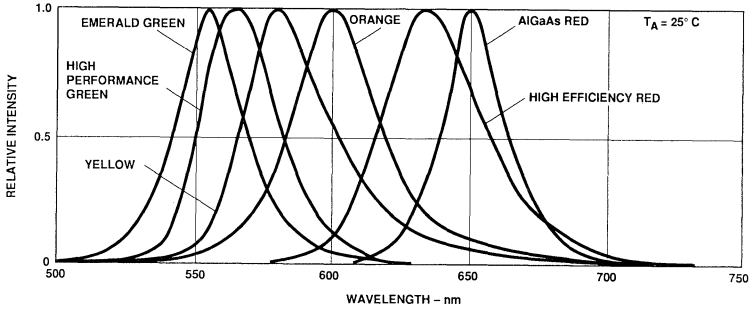


Figure 1. Relative Intensity vs. Wavelength.

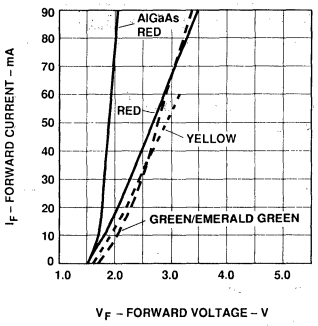


Figure 2. Forward Current vs. Forward Voltage Characteristics. V_F (300 mA) for AlGaAs Red = 2.6 Volts Typical.

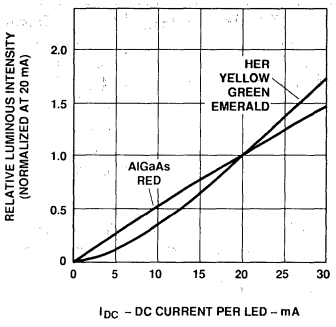


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

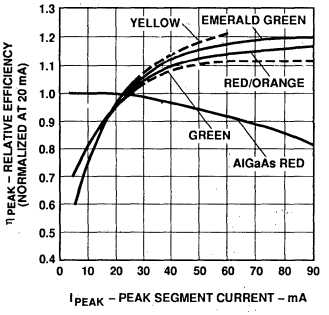
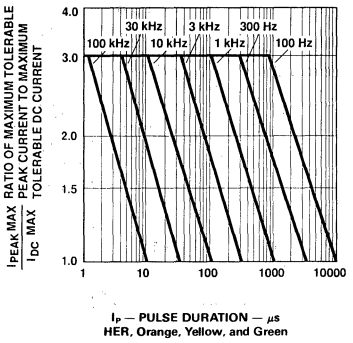


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. LED Peak Current. ηv (300 mA) for AlGaAs Red = 0.7.



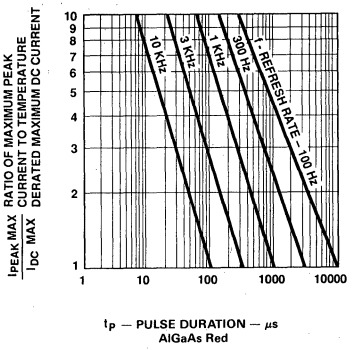


Figure 5. Maximum Tolerable Peak Current vs. Peak Duration. (I_{PEAK} MAX Determined from Temperature Derated I_{DC} MAX)

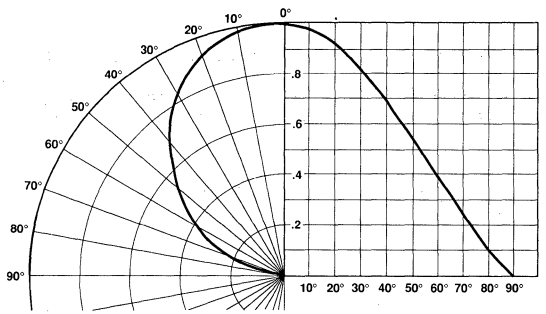


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

Subminiature Solid State Lamps

Technical Data

HLMP-PXXX Series
HLMP-Q1XX Series
HLMP-6XXX Series
HLMP-70XX Series

Features

- **Subminiature Flat Top Package**
  Ideal for Backlighting and Light Piping Applications
- **Subminiature Dome Package**
  Diffused Dome for Wide Viewing Angle
  Nondiffused Dome for High Brightness
- **Arrays**
- **TTL and LSTTL Compatible 5 Volt Resistor Lamps**
- **Available in Six Colors**
- **Ideal for Space Limited Applications**
- **Axial Leads**
- **Available with Lead Configurations for Surface Mount and Through Hole PC Board Mounting**

Description

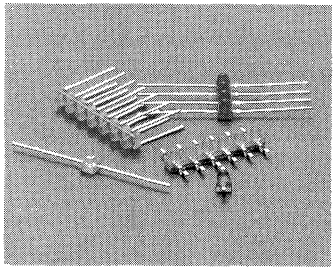
Flat Top Package
The HLMP-PXXX Series flat top lamps use an untinted, non-diffused, truncated lens to provide a wide radiation pattern that is necessary for use in backlighting applications. The flat top lamps are also ideal for use as emitters in light pipe applications.

Dome Packages
The HLMP-6XXX Series dome lamps for use as indicators use a tinted, diffused lens to provide a wide viewing angle with a high on-off contrast ratio. High brightness lamps use an untinted, nondiffused lens to provide a high luminous intensity within a narrow radiation pattern.

Arrays
The HLMP-66XX Series subminiature lamp arrays are available in lengths of 3 to 8 elements per array. The luminous intensity is matched within an array to assure a 2.1 to 1.0 ratio.

Resistor Lamps
The HLMP-6XXX Series 5 volt subminiature lamps with built in current limiting resistors are for use in applications where space is at a premium.

Lead Configurations
All of these devices are made by encapsulating LED chips on axial lead frames to form molded epoxy subminiature lamp packages. A variety of package configuration options is available. These include special surface mount lead configurations, gull wing, yoke lead or Z-bend. Right angle lead bends at 2.54 mm (0.100 inch) and 5.08 mm (0.200 inch) center spacing are available for through hole mounting. For more information refer to Subminiature Solid State Lamps Standard Options data sheet.

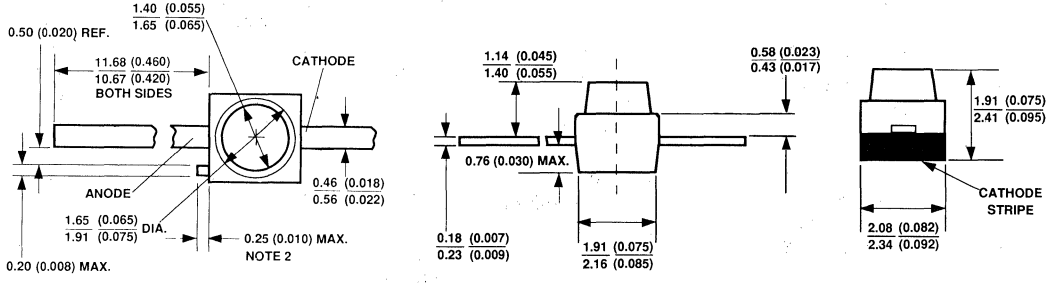


Device Selection Guide
Part Number: HLMP-XXXX

Standard Red	DH AS AlGaAs Red	High Efficiency Red	Orange	Yellow	High Perf. Green	Emerald Green	Device Description[1]		Device Outline Drawing
P005	P105	P205	P405	P305	P505	P605	Nondiffused, Flat Top		A
P002	P102	P202	P402	P302	P502		Diffused, Flat Top		B
6000/6001	Q101	6300	Q400	6400	6500	Q600	Diffused		
	Q105	6305		6405	6505		Nondiffused, High Brightness		
	Q150	7000		7019	7040		Diffused, Low Current		B
	Q155						Nondiffused, Low Current		
		6600		6700	6800		Diffused, Resistor, 5 V, 10 mA		
		6620		6720	6820		Diffused, Resistor, 5 V, 4 mA		
6203		6653		6753	6853		3 Element	Matched Array, Diffused	
6204		6654		6754	6854		4 Element		
6205		6655		6755	6855		5 Element		C
6206		6656		6756	6856		6 Element		
6208		6658		6758	6858		8 Element		

Package Dimensions

(A) Flat Top Lamps

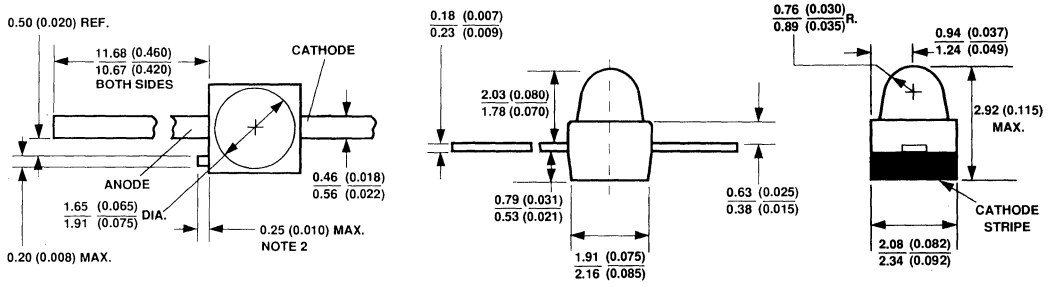


NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES).
2. PROTRUDING SUPPORT TAB IS CONNECTED TO CATHODE LEAD.

*Refer to Figure 1 for design concerns.

Package Dimensions (cont.)

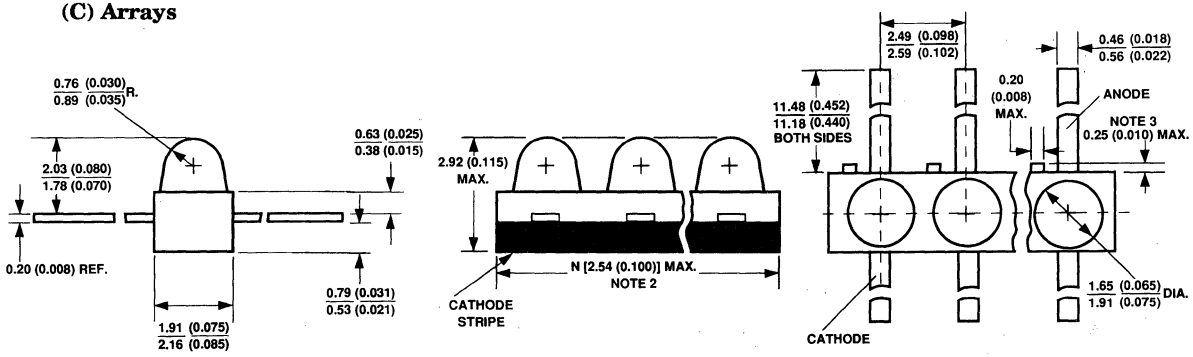
(B) Diffused and Nondiffused



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES).
2. PROTRUDING SUPPORT TAB IS CONNECTED TO CATHODE LEAD.

*Refer to Figure 1 for design concerns.

(C) Arrays



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES).
2. PROTRUDING SUPPORT TAB IS CONNECTED TO CATHODE LEAD.

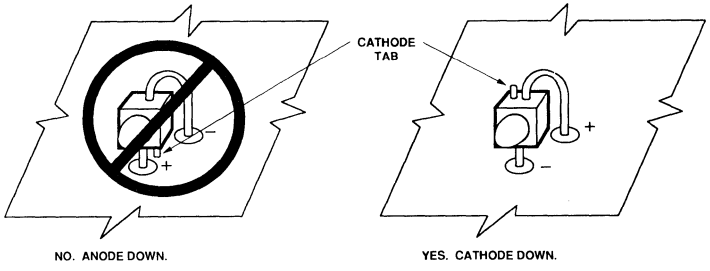


Figure 1. Proper Right Angle Mounting to a PC Board to Prevent Protruding Cathode Tab from Shorting to Anode Connection.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	Standard Red	DH AS AlGaAs Red	High Eff. Red	Orange	Yellow	High Perf. Green	Emerald Green	Units
DC Forward Current[1]	50	30	30	30	20	30	30	mA
Peak Forward Current[2]	1000	300	90	90	60	90	90	mA
DC Forward Voltage (Resistor Lamps Only)			6		6	6	6	V
Reverse Voltage (I_R = 100 µA)	5	5	5	5	5	5	5	V
Transient Forward Current[3] (10 µs Pulse)	2000	500	500	500	500	500	500	mA
Operating Temperature Range: Non-Resistor Lamps	-55 to +100	-55 to +100	-55 to +100			-40 to +100	-20 to +100	°C
Resistor Lamps			-40 to +85			-20 to +85		°C
Storage Temperature Range	-55 to +100							°C
Wave Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 5 Seconds							
Surface Mount Reflow Soldering: Convective IR	235°C for 90 Seconds							
Vapor Phase	215°C for 3 Minutes							

Notes:
1. See Figure 5 for current derating vs. ambient temperature. Derating is not applicable to resistor lamps.
2. Refer to Figure 6 showing Max. Tolerable Peak Current vs. Pulse Duration to establish pulsed operating conditions.
3. The transient peak current is the maximum non-recurring peak current the device can withstand without failure. Do not operate these lamps at this high current.

Electrical/Optical Characteristics, T_A = 25°C

Standard Red

Device HLMP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
P005	Luminous Intensity[1]	I_v	1.0	2.5		mcd	I_F = 10 mA
6000			0.5	1.2			
6001			1.3	3.2			
6203 to 6208			0.5	1.2			
All	Forward Voltage	V_F	1.4	1.6	2.0	V	I_F = 10 mA
	Reverse Breakdown Voltage	V_R	5.0	12.0		V	I_R = 100 µA
P005	Included Angle Between Half Intensity Points[2]	$2\theta_{1/2}$		125		Deg.	
All Others				90			
All	Peak Wavelength	λ_{PEAK}		655		nm	
	Dominant Wavelength[3]	λ_d		640		nm	
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		24		nm	
	Speed of Response	τ_s		15		ns	
	Capacitance	C		100		pF	V_F = 0; f = 1 MHz
	Thermal Resistance	$R\theta_{J\text{-}PIN}$		170		°C/W	Junction-to-Cathode Lead
	Luminous Efficacy[4]	η_v		65		lm/W	

DH AS AlGaAs Red

Device HLMP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
P102	Luminous Intensity	I_v	4.0	20.0		mcd	I_F = 20 mA
P105			8.6	30.0			
Q101			22.0	45.0			
Q105			22.0	55.0			
Q150			1.0	1.8			I_F = 1 mA
Q155			2.0	4.0			
Q101	Forward Voltage	V_F		1.8	2.2	V	I_F = 20 mA
P105/Q105				1.8	2.2		
Q150/Q155				1.6	1.8		I_F = 1 mA
All	Reverse Breakdown Voltage	V_R	5.0	15.0		V	I_R = 100 µA
P105	Included Angle Between Half Intensity Points[2]	$2\theta_{1/2}$		125		Deg.	
Q101/Q150				90			
Q105/Q155				28			
All	Peak Wavelength	λ_{PEAK}		645		nm	Measured at Peak
	Dominant Wavelength[3]	λ_d		637		nm	
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		20		nm	
	Speed of Response	τ_s		30		ns	Exponential Time Constant; e^{-t/τ_s}
	Capacitance	C		30		pF	V_F = 0; f = 1 MHz
	Thermal Resistance	$R\theta_{J\text{-}PIN}$		170		°C/W	Junction-to Cathode Lead
	Luminous Efficacy[4]	η_v		80		lm/W	

High Efficiency Red

Device HLMP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
P202	Luminous Intensity[1]	I_v	1.0	5.0		mcd	I_F = 10 mA
P205			1.0	5.0			
6300			1.0	3.0			
6305			3.4	12.0			
7000			0.4	0.8			I_F = 2 mA
6600			1.3	5.0			V_F = 5.0 Volts
6620			0.8	2.0			
6653 to 6658			1.0	3.0			I_F = 10 mA
All	Forward Voltage (Nonresistor Lamps)	V_F	1.5	1.8	3.0	V	I_F = 10 mA
6600	Forward Current (Resistor Lamps)	I_F		9.6	13.0	mA	V_F = 5.0 V
6620				3.5	5.0		
All	Reverse Breakdown Voltage	V_R	5.0	30.0		V	I_R = 100 μA
P205	Included Angle Between Half Intensity Points[2]	$2\theta_{1/2}$		125		Deg.	
6305				28			
All Diffused				90			
All	Peak Wavelength	λ_{PEAK}		635		nm	Measured at Peak
	Dominant Wavelength[3]	λ_d		626		nm	
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		40		nm	
	Speed of Response	τ_s		90		ns	
	Capacitance	C		11		pF	V_F = 0; f = 1 MHz
	Thermal Resistance	$R\theta_{J\text{-}PIN}$		170		°C/W	Junction-to-Cathode Lead
	Luminous Efficacy[4]	η_v		145		lm/W	

Orange

Device HLMP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
P402	Luminous Intensity	I_v	1.0	4.0		mcd	I_F = 10 mA
P405			1.0	4.0			
Q400			1.0	3.0			
P405 Q400	Forward Voltage	V_F	1.5	1.9	3.0	V	I_F = 10 mA
	Reverse Breakdown Voltage	V_R	5.0	30.0		V	I_R = 100 μA
P405	Included Angle Between Half Intensity Points[2]	$2\theta_{1/2}$		125		Deg.	
Q400				90			
P405/ Q400	Peak Wavelength	λ_{PEAK}		600		nm	
	Dominant Wavelength[3]	λ_d		602		nm	Measured at Peak
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		40		nm	
	Speed of Response	τ_s		260		ns	
	Capacitance	C		4		pF	V_F = 0; f = 1 MHz
	Thermal Resistance	$R\theta_{J\text{-}PIN}$		170		°C/W	Junction-to-Cathode Lead
	Luminous Efficacy[4]	η_v		380		lm/W	

Yellow

Device HLMP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
P302	Luminous Intensity[1]	I_v	1.0	3.0		mcd	I_F = 10 mA
P305			1.0	4.0			
6400			1.0	3.0			
6405			3.6	12			
7019			0.4	0.6			I_F = 2 mA
6700			1.4	5.0			V_F = 5.0 Volts
6720			0.9	2.0			
6753 to 6758			1.0	3.0			I_F = 10 mA
All	Forward Voltage (Nonresistor Lamps)	V_F		2.0	2.4	V	I_F = 10 mA
6700	Forward Current (Resistor Lamps)	I_F		9.6	13.0	mA	V_F = 5.0 V
6720				3.5	5.0		
All	Reverse Breakdown Voltage	V_R	5.0	50.0		V	
P305	Included Angle Between Half Intensity Points[2]	$2\theta_{1/2}$		125		Deg.	
6405				28			
All Diffused				90			
All	Peak Wavelength	λ_{PEAK}		583		nm	Measured at Peak
	Dominant Wavelength[3]	λ_d		585		nm	
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		36		nm	
	Speed of Response	τ_s		90		ns	
	Capacitance	C		15		pF	V_F = 0; f = 1 MHz
	Thermal Resistance	$R\theta_{J\text{-}PIN}$		170		°C/W	Junction-to-Cathode Lead
	Luminous Efficacy[4]	η_v		500		lm/W	

High Performance Green

Device HLMP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
P502	Luminous Intensity[1]	I_v	1.0	6.0		mcd	I_F = 10 mA
P505			1.0	5.0			
6500			1.0	3.0			
6505			4.2	12.0			
7040			0.4	0.6			I_F = 2 mA
6800			1.6	5.0			V_F = 5.0 Volts
6820			0.8	2.0			
6853 to 6858			1.0	3.0			I_F = 10 mA
All	Forward Voltage (Nonresistor Lamps)	V_F		2.1	2.7	V	I_F = 10 mA
6800	Forward Current (Resistor Lamps)	I_F		9.6	13.0	mA	V_F = 5.0 V
6820				3.5	5.0		
All	Reverse Breakdown Voltage	V_R	5.0	50.0		V	I_R = 100 μA
P505	Included Angle Between Half Intensity Points[2]	$2\theta_{1/2}$		125		Deg.	
6505				28			
All Diffused				90			
All	Peak Wavelength	λ_{PEAK}		565		nm	
	Dominant Wavelength[3]	λ_d		569		nm	
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		28		nm	
	Speed of Response	τ_s		500		ns	
	Capacitance	C		18		pF	V_F = 0; f = 1 MHz
	Thermal Resistance	$R\theta_{J\text{-}PIN}$		170		°C/W	Junction-to-Cathode Lead
	Luminous Efficacy[4]	η_v		595		lm/W	

Notes:
1. The luminous intensity for arrays is tested to assure a 2.1 to 1.0 matching between elements. The average luminous intensity for an array determines its light output category bin. Arrays are binned for luminous intensity to allow I_v matching between arrays.
2. $\theta_{1/2}$ is the off-axis angle where the luminous intensity is half the on-axis value.
3. Dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and represents the single wavelength that defines the color of the device.
4. Radiant intensity, I_e, in watts/steradian, may be calculated from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

New

Emerald Green[1]

Device HLMP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
P605	Luminous Intensity	I_v	1.0	1.5		mcd	I_F = 10 mA
Q600			1.0	1.5			
	Forward Voltage	V_F		2.0	3.0	V	I_F = 10 mA
	Reverse Breakdown Voltage	V_R	5.0			V	I_R = 100 µA
P605	Included Angle Between Half Intensity Points[2]	$2\theta_{1/2}$		125		Deg.	
Q600				90			
P605/ Q600	Peak Wavelength	λ_{PEAK}		558		nm	
	Dominant Wavelength[3]	λ_d		560		nm	Measured at Peak
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		24		nm	
	Speed of Response	τ_s		3100		ns	
	Capacitance	C		35		pF	V_F = 0; f = 1 MHz
	Thermal Resistance	$R\theta_{J\text{-}PIN}$		170		°C/W	Junction-to-Cathode Lead
	Luminous Efficacy[4]	η_v		656		lm/W	

Note:
1. Please refer to Application Note 1061 for information comparing stnadard green and emerald green light ouptut degradation.

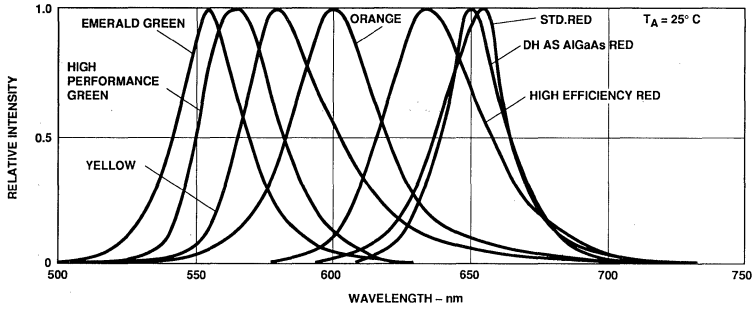


Figure 1. Relative Intensity vs. Wavelength.

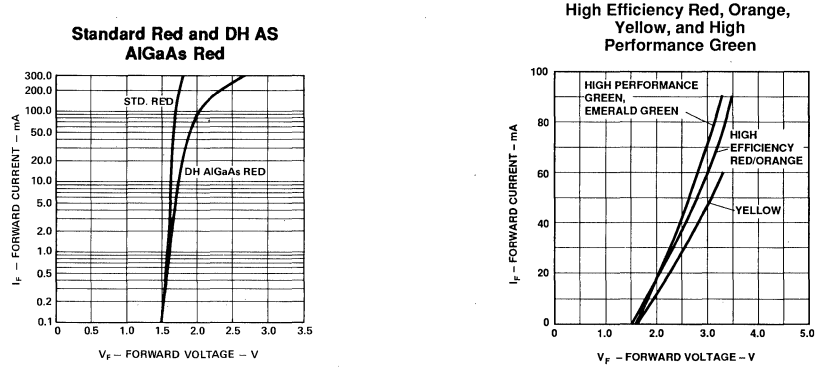


Figure 2. Forward Current vs. Forward Voltage. (Non-Resistor Lamp)

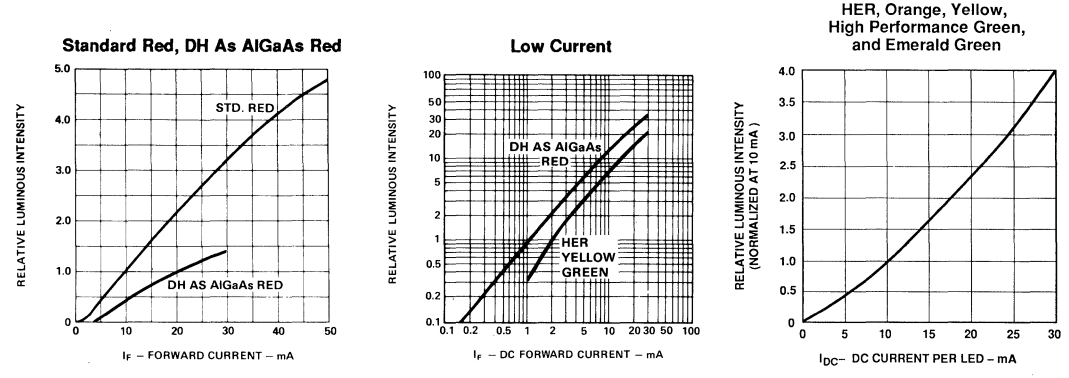


Figure 3. Relative Luminous Intensity vs. Forward Current. (Non-Resistor Lamp)

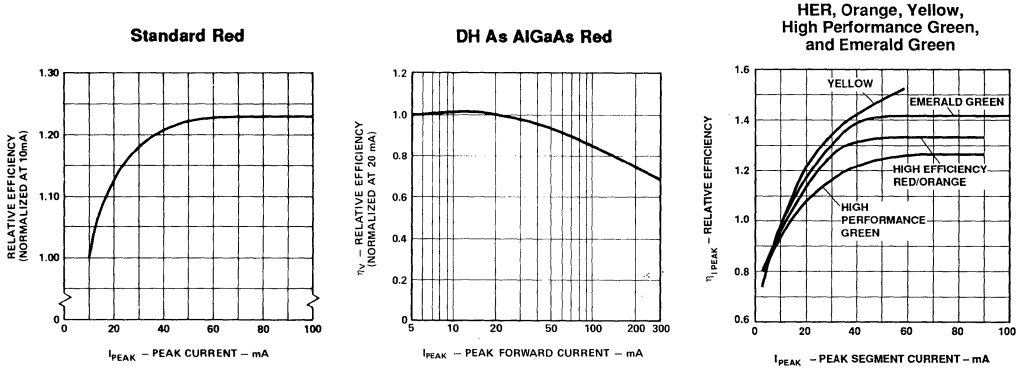
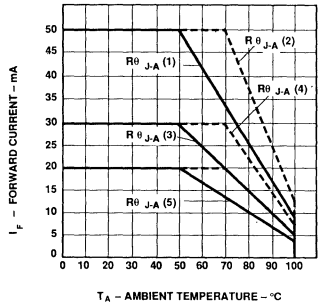


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current (Non-Resistor Lamps).



$R\theta_{J-A}(X)$	STD RED	AlGaAs RED	HI-EFF RED	ORANGE	YELLOW	GREEN	UNITS
1	600						°C/W LED JUNCTION TO AMBIENT
2	400						
3		689	444	444	470	444	
4		559	296	296		296	
5					705		

Figure 5. Maximum Forward dc Current vs. Ambient Temperature. Derating Based on T_J MAX = 110°C (Non-Resistor Lamps).

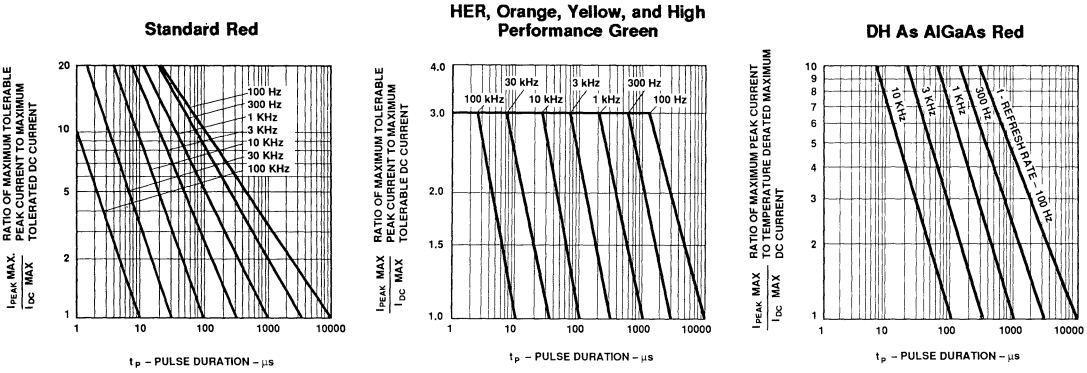


Figure 6. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings) (Non-Resistor Lamps).

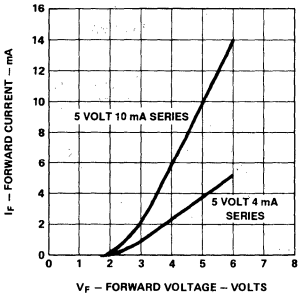


Figure 7. Resistor Lamp Forward Current vs. Forward Voltage.

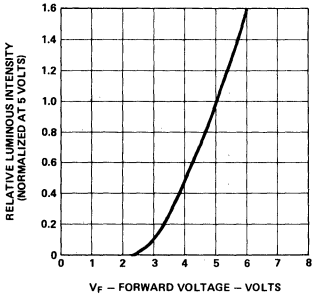


Figure 8. Resistor Lamp Luminous Intensity vs. Forward Voltage.

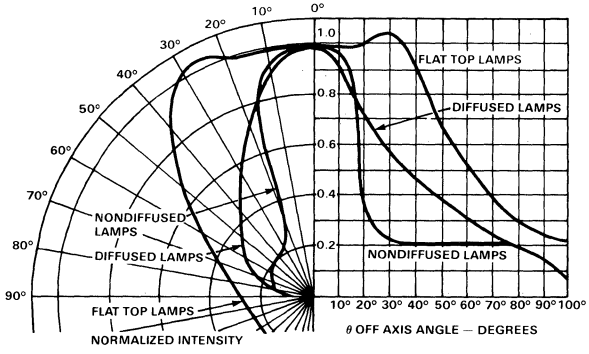


Figure 9. Relative Intensity vs. Angular Displacement.

HEWLETT PACKARD

High Efficiency Red/ High Performance Green Bicolor Solid State Lamps

Technical Data

HLMP-4000
HLMP-0800

SOLID STATE LAMPS

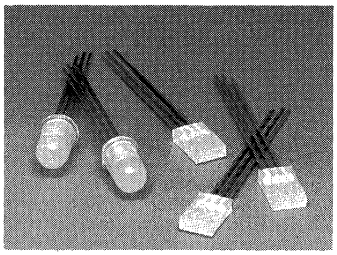
Features:

- **Two Color (Red, Green) Operation**
- **(Other Two LED Color Combinations Available)**
- **Three Leads with One Common Cathode**
- **Diffused, Wide Visibility Lens**

Description

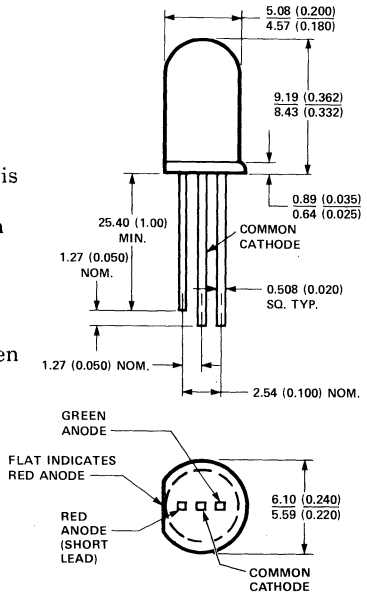
The T-1 3/4 HLMP-4000 and 2 mm by 5 mm rectangular HLMP-0800 are three leaded bicolor light sources designed for a variety of applications where dual state illumination is required in the same package. There are two LED chips, high efficiency red (HER), and high performance green (Green), mounted on a central common cathode lead for maximum on-axis viewability. Colors between HER and Green can be generated by independently pulse width modulating the LED chips.

Note: Other possible LED combinations available are AlGaAs, orange, yellow.

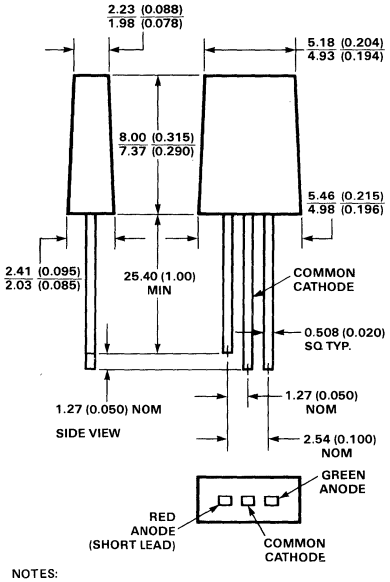


Package Dimensions

HLMP-4000



HLMP-0800



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	High Efficiency Red/Green	Units
Peak Forward Current	90	mA
Average Forward Current[1,2] (Total)	25	mA
DC Current[2,4] (Total)	30	mA
Power Dissipation[3,5] (Total)	135	mW
Operating Temperature Range	-20 to +85	°C
Storage Temperature Range	-55 to +100	
Reverse Voltage (I_R = 100 μA)	5	V
Transient Forward Current[6] (10 μsec Pulse)	500	mA
Lead Soldering Temperature [1.6 mm (0.063 in.) below seating plane]	260°C for 5 seconds	

Notes:
1. See Figure 5 to establish pulsed operating conditions.
2. The combined simultaneous current must not exceed the maximum.
3. The combined simultaneous power must not exceed the maximum.
4. For HER and Green derate linearly from 50°C at 0.5 mA/°C.
5. For HER and Green derate linearly from 25°C at 1.8 mW/°C.
6. The transient peak current is the maximum non-recurring current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

Electrical/Optical Characteristics at $T_A = 25°C$

Sym.	Parameter	Red			Green			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Luminous Intensity HLMP-4000	2.1	5		4.2	8		mcd	$I_F = 10$ mA
	HLMP-0800	2.1	3.5		2.6	4.0			$I_F = 20$ mA
λ_{PEAK}	Peak Wavelength		635			565		nm	
λ_d	Dominant Wavelength[1]		626			569			
τ_s	Speed of Response		90			500		ns	
C	Capacitance		11			18		pF	$V_F = 0$, f = 1 MHz
V_F	Forward Voltage		1.9	2.4		2.1	2.7	V	$I_F = 10$ mA
V_R	Reverse Breakdown Voltage	5			5			V	$I_R = 100\ \mu A$
$R\theta_{J\text{-}PIN}$	Thermal Resistance		260		260			°C/W	Junction to Cathode Lead
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points[2] HLMP-4000		65			65		Deg.	$I_F = 10$ mA
	HLMP-0800		100			100			$I_F = 20$ mA
η_V	Luminous Efficacy[3]		145			595		Lumen/ Watt	

Notes:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
3. Radiant intensity, I_e, in watts steradian, may be found from the equation $I_e = I_v/\eta_v$ where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

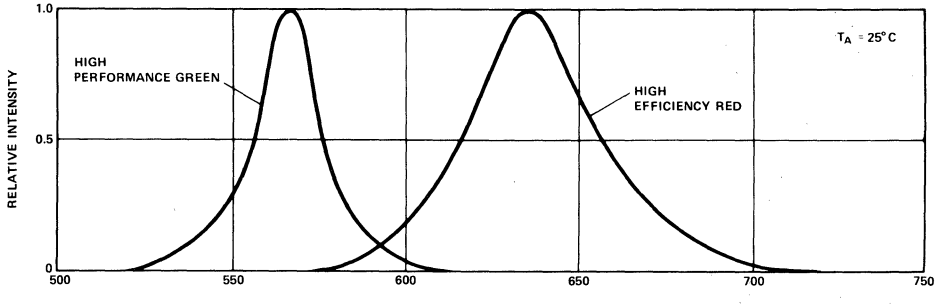


Figure 1. Relative Intensity vs. Wavelength.

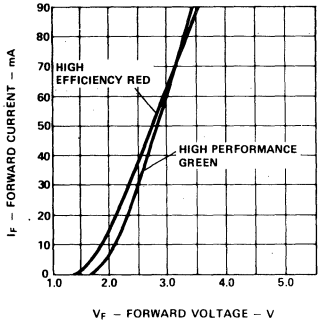


Figure 2. Forward Current vs. Forward Voltage Characteristics.

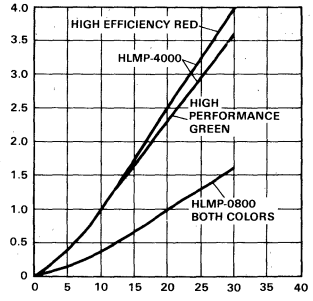


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

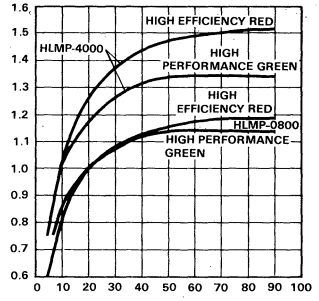


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

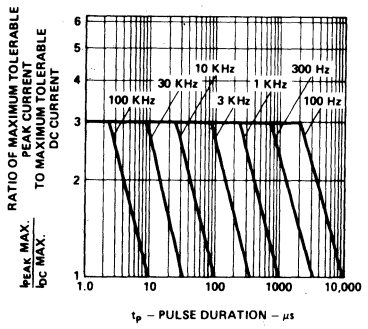


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings

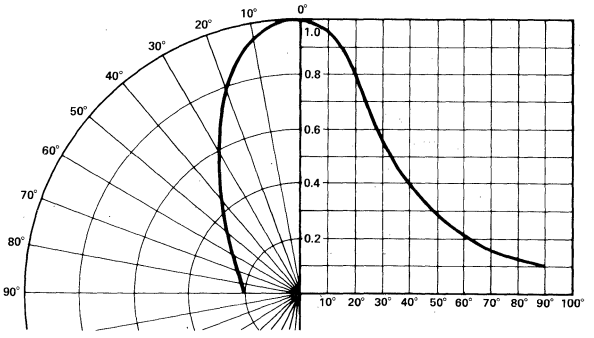


Figure 6. Relative Luminous Intensity vs. Angular Displacement for the HLMP-4000.

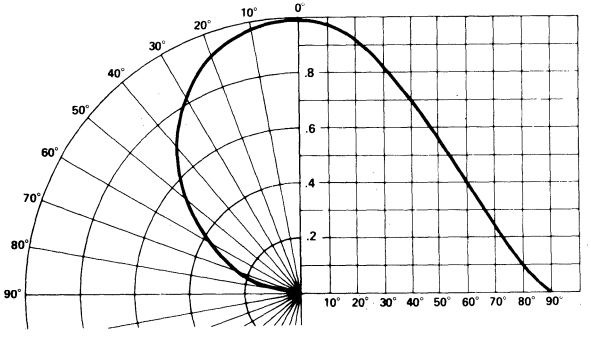


Figure 7. Relative Luminous Intensity vs. Angular Displacement for the HLMP-0800.

HEWLETT PACKARD

Integrated Resistor Lamps 5 Volt and 12 Volt in T-1 and T-1¾ Packages

Technical Data

HLMP-1100, HLMP-1120
HLMP-1600, HLMP-1601
HLMP-1620, HLMP-1621
HLMP-1640, HLMP-1641
HLMP-3105, HLMP-3112
HLMP-3600, HLMP-3601
HLMP-3650, HLMP-3651
HLMP-3680, HLMP-3681

SOLID STATE LAMPS

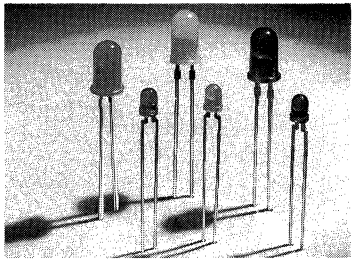
Features

- **Integral Current Limiting Resistor**
- **TTL Compatible**
  Requires no External Current Limiter with 5 Volt/12 Volt Supply
- **Cost Effective**
  Saves Space and Resistor Cost
- **Wide Viewing Angle**
- **Available in All Colors**
  Red, High Efficiency Red, Yellow, and High Performance Green in T-1 and T-1¾ Packages

Description

The 5 volt and 12 volt series lamps contain an integral current limiting resistor in series with the LED. This allows the lamp to be driven from a 5 volt/12 volt source without an external current limiter. The red LEDs are made from GaAsP on a GaAs substrate. The High Efficiency Red and Yellow devices use GaAsP on a GaP substrate.

The green devices use GaP on a GaP substrate. The diffused lamps provide a wide off-axis viewing angle.



The T-1¾ lamps are provided with sturdy leads suitable for wire wrap applications. The T-1¾ lamps may be front panel mounted by using the HLMP-0103 clip and ring.

Package Dimensions

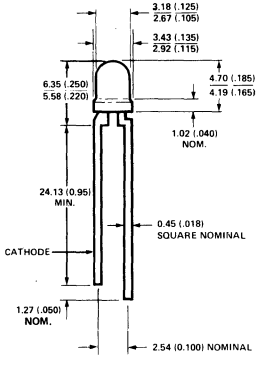


Figure A. T-1 Package.

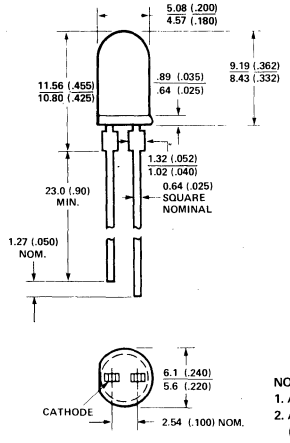


Figure B. T-1¾ Package.

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Selection Guide

Color	Part Number HLMP-	Package	Operating Voltage	I_v mcd		$2\theta_{1/2}$[1]	Package Outline
				Min.	Typ.		
Red	1100	T-1 Tinted Diffused	5	0.8	2.5	60°	A
	1120	T-1 Untinted Diffused	5	0.8	2.5	60°	A
	3105	T-1¾ Tinted Diffused	5	1.0	3.0	60°	B
	3112		12	1.0	3.0	60°	B
High Efficiency Red	1600	T-1 Tinted Diffused	5	2.0	8.0	60°	A
	1601		12				
	3600	T-1¾ Tinted Diffused	5			60°	B
	3601		12				
Yellow	1620	T-1 Tinted Diffused	5	2.0	8.0	60°	A
	1621		12				
	3650	T-1¾ Tinted Diffused	5			60°	B
	3661		12				
High Performance Green	1640	T-1 Tinted Diffused	5	2.0	8.0	60°	A
	1641		12				
	3680	T-1¾ Tinted Diffused	5			60°	B
	3681		12				

Note:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is ½ the axial luminous intensity.

Absolute Maximum Ratings at T_A = 25°C

	Red/HER/ Yellow 5 Volt Lamps	Red/HER/ Yellow 12 Volt Lamps	Green 5 Volt Lamps	Green 12 Volt Lamps
DC Forward Voltage (T_A = 25°C)	7.5 Volts[2]	15 Volts[3]	7.5 Volts[2]	15 Volts[3]
Reverse Voltage (I_R = 100 µA)	5 Volts	5 Volts	5 Volts	5 Volts
Operating Temperature Range	-40°C to 85°C	-40°C to 85°C	-20°C to 85°C	-20°C to 85°C
Storage Temperature Range	-55°C to 100°C	-55°C to 100°C	-55°C to 100°C	-55°C to 100°C
Lead Soldering Temperature	260°C for 5 seconds			

Notes:
2. Derate from T_A = 50°C at 0.071 V/°C, see Figure 3.
3. Derate from T_A = 50°C at 0.086 V/°C, see Figure 4.

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	Red			High Efficiency Red			Yellow			Green			Unit	Test Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
λ_P	Peak Wavelength		655			635			583			565		nm	
λ_d	Dominant Wavelength		648			626			585			569		nm	Note 4
$\Delta\lambda 1/2$	Spectral Line Halfwidth		24			40			36			28		nm	
$R\theta_{J\text{-}PIN}$	Thermal Resistance		290			290			290			290		°C/W	Junction to Cathode Lead (Note 6)
$R\theta_{J\text{-}PIN}$	Thermal Resistance		210			210			210			210		°C/W	Junction to Cathode Lead (Note 7)
I_F	Forward Current 12 V Devices		13	20		13	20		13	20		13	20	mA	$V_F = 12$ V
I_F	Forward Current 5 V Devices		13	20		10	15		10	15		12	15	mA	$V_F = 5$ V
η_V	Luminous Efficacy		65			145			500			595		lumen /Watt	Note 2
V_R	Reverse Breakdown Voltage	5.0			5.0			5.0			5.0			V	$I_R = 100\ \mu A$

Notes:

4. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
5. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/Watt.
6. For Figure A package type.
7. For Figure B package type.

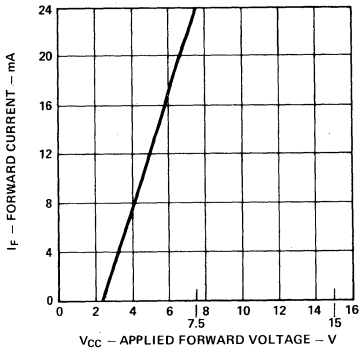


Figure 1. Forward Current vs. Applied Forward Voltage. 5 Volt Devices.

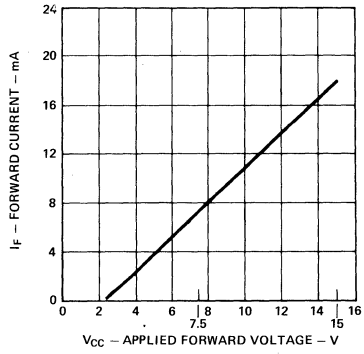


Figure 2. Forward Current vs. Applied Forward Voltage. 12 Volt Devices.

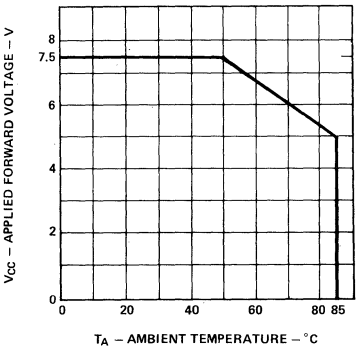


Figure 3. Maximum Allowed Applied Forward Voltage vs. Ambient Temperature $R\theta_{JA}$ = 175°C/W. 5 Volt Devices.

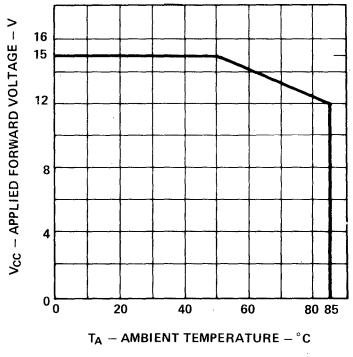


Figure 4. Maximum Allowed Applied Forward Voltage vs. Ambient Temperature $R\theta_{JA}$ = 175°C/W. 12 Volt Devices.

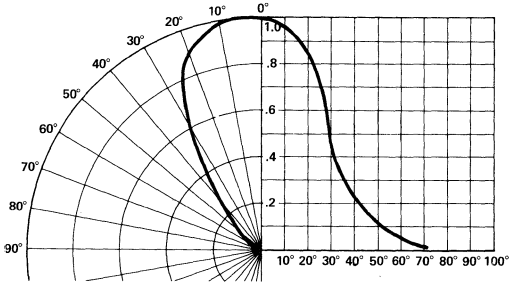


Figure 4. Relative Luminous Intensity vs. Angular Displacement for T-1 Package.

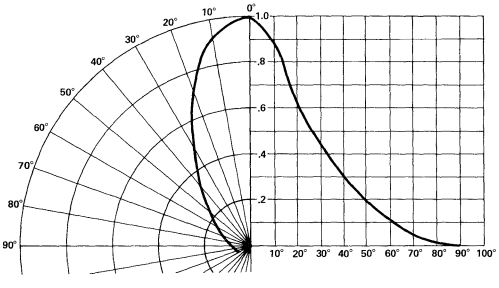


Figure 5. Relative Luminous Intensity vs. Angular Displacement for T-1¾ Package.

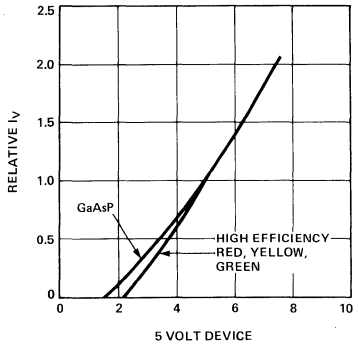


Figure 6. Relative Luminous Intensity vs. Applied Forward Voltage. 5 Volt Devices.

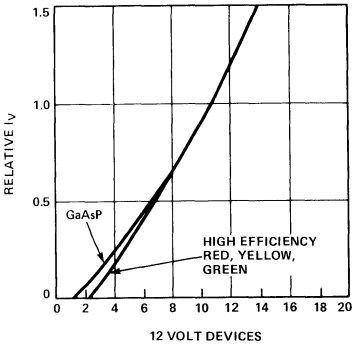


Figure 7. Relative Luminous Intensity vs. Applied Forward Voltage. 12 Volt Devices.

HEWLETT PACKARD

Tape and Reel Solid State Lamps

Technical Data

Option 001
Option 002

Features

- **Compatible with Radial Lead Automatic Insertion Equipment**
- **Meets Dimensional Specifications of IEC Publication 286 and ANSI/EIA Standard RS-468 for Tape and Reel**
- **Reel Packaging Simplifies Handling and Testing**
- **T-1 and T-1¾ LED Lamps Available Packaged on Tape and Reel**
- **5 mm (0.197 inch) Formed Lead and 2.54 mm (0.100 inch) Straight Lead Spacing Available**

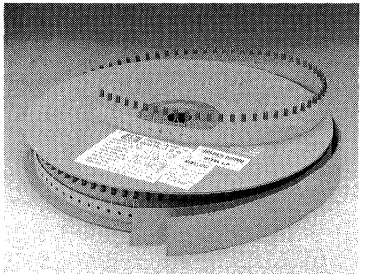
Description

T-1 and T-1¾ LED lamps are available on tape and reel as specified by the IEC Publication 286 and ANSI/EIA Standard RS-468. The Option 001 lamp devices have formed leads with 5 mm (0.197 inch) spacing for automatic insertion into PC boards by radial lead insertion equipment. The Option 002 lamp devices have straight leads with 2.54 mm (0.100 inch) spacing, packaged on tape and reel for ease of handling. T-1 lamps are packaged 1800/reel. T-1¾ lamps are packaged 1300/reel.

Ordering Information

To order LED lamps packaged on tape and reel, include the appropriate option code along with the device catalog part number. Example: to order the HLMP-3300 on tape and reel with formed leads (5 mm lead spacing) order as follows: HLMP-3300 Option 001. Minimum order quantities vary by part number. Orders must be placed in reel increments. Please contact your local Hewlett-Packard sales office or franchised Hewlett-Packard distributor for a complete list of lamps available on tape and reel.

LED lamps with 0.46 mm (0.018 inch) square leads with 5 mm



(0.197 inch) lead spacing are recommended for use with automatic insertion equipment. It is suggested that insertion machine compatibility be confirmed.

Device Selection Guide

Option	Description
001	Tape and reel, 5 mm (0.197 inch) formed leads.
002	Tape and reel, 2.54 mm (0.100 inch) straight leads.

Package	Quantity/Reel	Order Increments
T-1	1800	1800
T-1¾	1300	1300

Absolute Maximum Ratings and Electrical/ Optical Characteristics

The absolute maximum ratings, mechanical dimension tolerances and electrical/optical characteristics for lamps packaged on tape and reel are identical to the basic catalog device. Refer to the basic data sheet for the specified values.

Notes:

1. Minimum leader length at either end of tape is 3 blank part spaces.
2. Silver saver paper is used as the interlayer for silver plated lead devices.
3. The maximum number of consecutive missing lamps is 3.
4. In accordance with EIA and IEC specs, the anode lead leaves the reel first.
5. Drawings apply to devices with 0.46 mm (0.018 inch) square leads only. Contact Hewlett-Packard Sales Office for dimensions of 0.635 mm (0.025 inch) square lead devices.

Tape and Reel LED Configurations

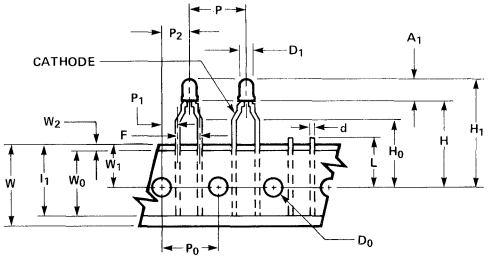


Figure 1. T-1 High Profile Lamps, Option 001.

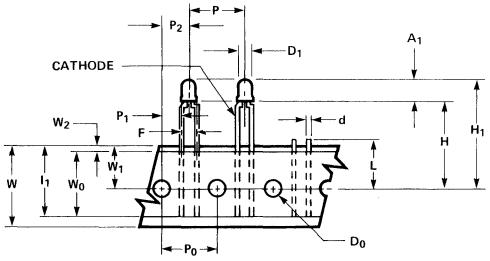


Figure 2. T-1 High Profile Lamps, Option 002.

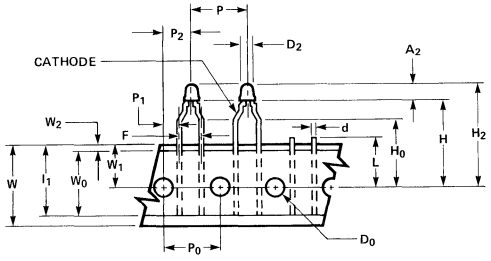


Figure 3. T-1 Low Profile Lamps, Option 001.

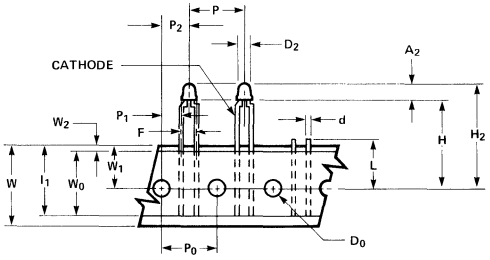


Figure 4. T-1 Low Profile Lamps, Option 002.

Tape and Reel LED Configurations (cont.)

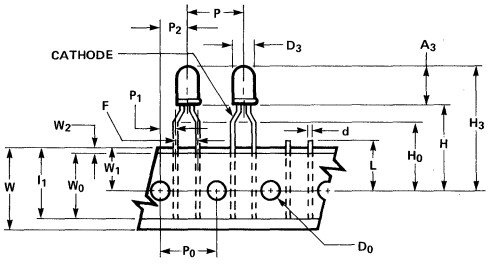


Figure 5. T-1¾ High Profile Lamps, Option 001.

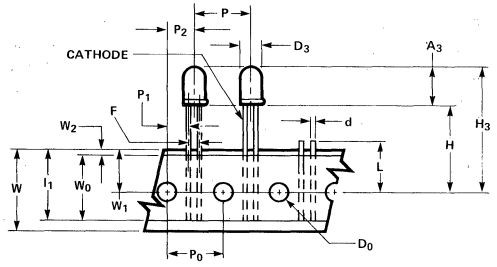


Figure 6. T-1¾ High Profile Lamps, Option 002.

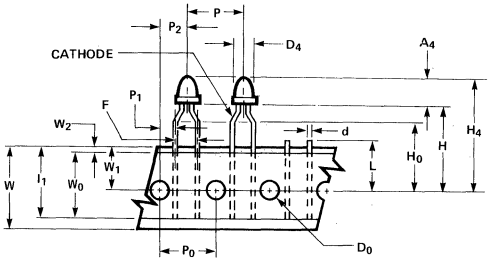


Figure 7. T-1¾ Low Profile Lamps, Option 001.

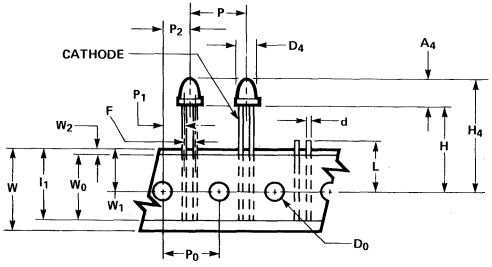
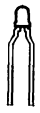
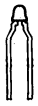
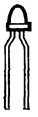


Figure 8. T-1¾ Low Profile Lamps, Option 002.

Dimensional Specifications for Tape and Reel

Item	Option 001	002	Symbol	Specification	Notes
T1 High Profile Body Height			A1	4.70 (0.185) / 4.19 (0.165)	
Body Diameter			D1	3.18 (0.125) / 2.67 (0.105)	
Component Height			H1	25.7 (1.012) Max.	
T1 Low Profile Body Height			A2	3.73 (0.147) / 3.23 (0.127)	
Body Diameter			D2	3.05 (0.120) / 2.79 (0.110)	
Component Height			H2	24.7 (0.974) Max.	
T1¾ High Profile Body Height			A3	9.19 (0.362) / 8.43 (0.332)	
Body Diameter			D3	5.08 (0.200) / 4.32 (0.170)	
Component Height			H3	30.2 (1.189) Max.	
T1¾ Low Profile Body Height			A4	6.35 (0.250) / 5.33 (0.210)	
Body Diameter			D4	5.08 (0.200) / 4.32 (0.170)	
Component Height			H4	27.4 (1.079) Max.	
Lead Wire Thickness			d	0.45 (0.018)	Square Leads
Pitch of Component			P	13.7 (0.539) / 11.7 (0.461)	
Feed Hole Pitch			P_0	12.9 (0.508) / 12.5 (0.492)	Cumulative error: 1.0 mm/20 pitches
Feed Hole Center to Lead Center			P1	4.55 (0.179) / 3.15 (0.124)	Measure at crimp bottom 5.78/3.68 (0.227/0.1448) for straight leads
Hole Center to Component Center			P2	7.35 (0.289) / 5.35 (0.211)	
Lead to Lead Distance			F	5.40 (0.213) / 4.90 (0.193)	2.54 (0.100) nominal for straight leads
Component Alignment, Front-rear			Δh	0 ± 1.0 (0.039)	Figure 9
Tape Width			W	18.5 (0.728) / 17.5 (0.689)	
Hold Down Tape Width			W_0	15.3 (0.602) / 14.7 (0.579)	
Hole Position			W1	9.75 (0.384) / 8.50 (0.335)	

Dimensional Specifications for Tape and Reel (cont.)

Item Option 001 002	Symbol	Specification	Notes
Hold Down Tape Position	W2	2.54 (0.100) Max.	
Height of Component from Hole Center	H	21.0 (0.827) 20.0 (0.787)	
Lead Clinch Height	H_O	16.5 (0.650) 15.5 (0.610)	
Feed Hole Diameter	D_O	4.20 (0.165) 3.80 (0.150)	
Total Tape Thickness	t	0.90 (0.035) 0.50 (0.020)	Paper thickness: 0.55 (0.022) 0.45 (0.018) Figure 9
Length of Snipped Lead	L	11.0 (0.433) Max.	
Lead Length Under Hold Down Tape	I1	14.5 (0.571) Min.	

Note:
1. Dimensions in millimetres (inches) maximum/minimum.

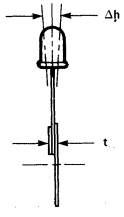


Figure 9. Front to Rear Alignment and Tape Thickness, Typical All Device Types.

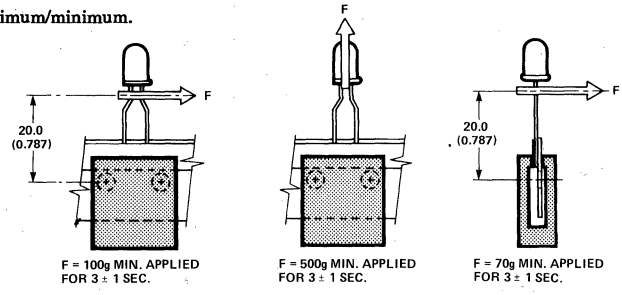


Figure 10. Device Retention Tests and Specifications.

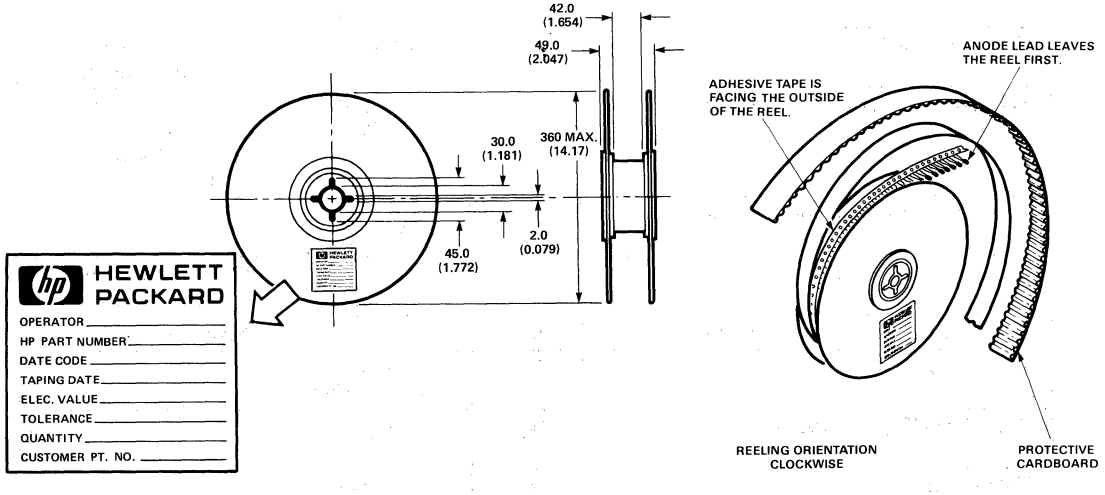


Figure 11. Reel Configuration and Labeling.

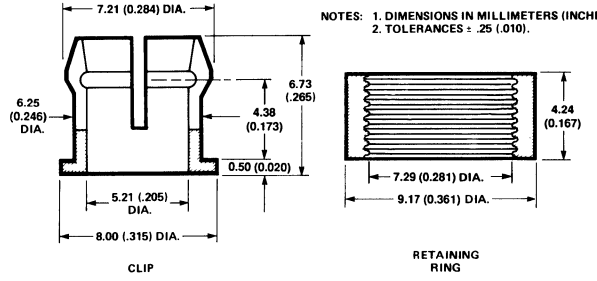
Clip and Retaining Ring for Panel Mounted T-1¾ LEDs

Technical Data

Option 007 (HLMP-0104)

Description

The Option 007 (HLMP-0104) is a black plastic mounting clip and retaining ring. It is designed to panel mount Hewlett-Packard Solid State high profile T-1¾ size lamps. This clip and ring combination is intended for installation in instrument panels from 1.52 mm (0.060") to 3.18 mm (0.125") thick. For panels greater than 3.18 mm (0.125") counterboring is required to the 3.18 mm (0.125") thickness.

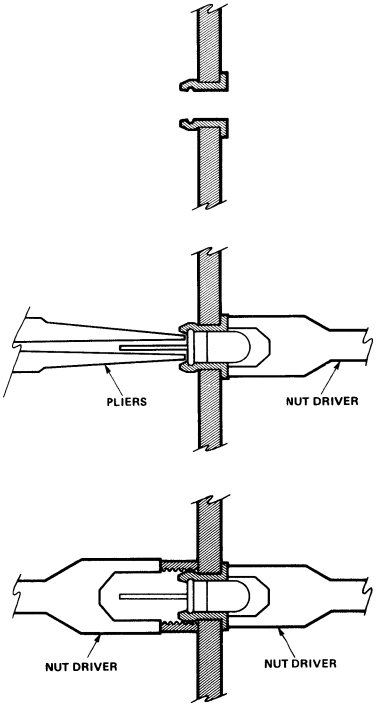


Mounting Instructions

1. Drill a 6.35/6.53 (0.250/0.257 in.) dia. hole in the panel. Deburr but do not chamfer the edges of the hole.

2. Press the panel clip into the hole from the front of the panel.

3. Press the LED into the clip from the back. Use blunt long nose pliers to push on the LED. Do not use force on the LED leads. A tool such as a nut driver may be used to press on the clip.



Note: Clip and retaining ring are also available for T-1 package, from a non-HP source. Please contact Interconsal Association, 2584 Wyandotte Way, Mountain View, CA for additional information. Telephone: (408) 745-0161.

4. Slip a plastic retaining ring onto the back of the clip and press tight using tools such as two nut drivers.

Ordering Information

T-1¾ High Dome LED Lamps can be purchased to include clip and ring by adding Option Code 007 to the device catalog part number.

Example: To order the HLMP-3300 including clip and ring, order as follows: HLMP-3300 Option 007.

T-1¾ (5 mm) LED Right Angle Indicators

Technical Data

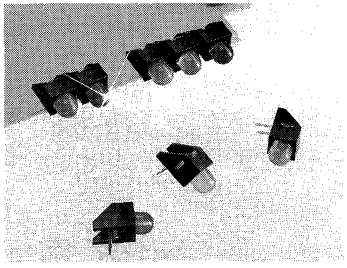
Option 010
Option 100

Features

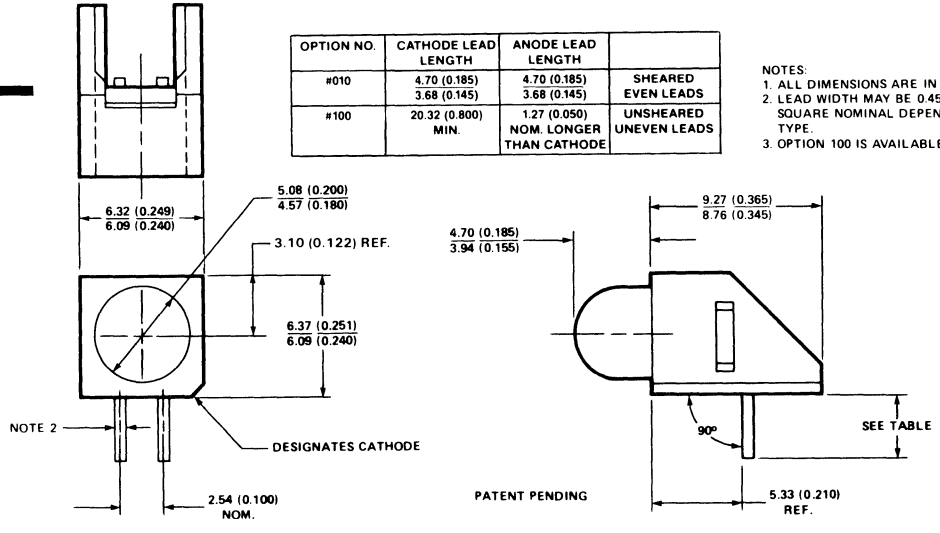
- **Ideal for Card Edge Status Indication**
- **Package Design Allows Flush Seating on a PC Board**
- **May be Side Stacked on 6.35 mm (0.25") Centers**
- **LEDs Available in Four Colors, With or Without Integrated Current Limiting Resistor in T-1¾ Tinted Diffused Packages**
- **Housing Meets UL9V-0 Flammability Rating**
- **Additional Catalog Lamps Available as Options**

Description

The T-1¾ Option 010 and 100 series of Right Angle Indicators are industry standard status indicators that incorporate a T-1¾ LED lamp in a black plastic right angle mount housing. The indicators are available in



Package Dimensions



OPTION NO.	CATHODE LEAD LENGTH	ANODE LEAD LENGTH	
#010	4.70 (0.185) 3.68 (0.145)	4.70 (0.185) 3.68 (0.145)	SHEARED EVEN LEADS
#100	20.32 (0.800) MIN.	1.27 (0.050) NOM. LONGER THAN CATHODE	UNSHEARED UNEVEN LEADS

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. LEAD WIDTH MAY BE 0.45 (0.018) OR 0.64 (0.025) SQUARE NOMINAL DEPENDING UPON PRODUCT TYPE.
3. OPTION 100 IS AVAILABLE FOR LONGER LEADS.

standard Red, High Efficiency Red, Yellow, or High Performance Green with or without an integrated current limiting resistor. These products are designed to be used as back panel diagnostic indicators and card edge logic status indicators.

Ordering Information

To order T-1¾ high dome lamps with right angle mount housing, select the base part number and add the option code 010 or 100. For example: HLMP-3750 option 010.

All Hewlett-Packard T-1¾ high-dome lamps are available in right angle housing. Contact your local Hewlett-Packard Sales Office or authorized components distributor for additional ordering information.

The Plastic right angle housing may be purchased separately as part number HLMP-5029.

Absolute Maximum Ratings and Electrical/ Optical Characteristics

The absolute maximum ratings and device characteristics are identical to those of the T-1¾ LED lamps. For information about these characteristics, see the data sheets of the equivalent T-1¾ LED lamp.

T-1 (3 mm) Right Angle LED Indicators

Technical Data

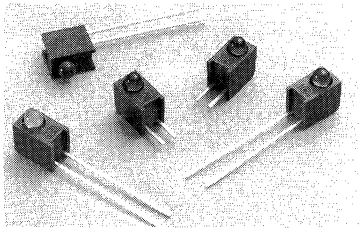
Option 010
Option 101

Features

- **Ideal for Card Edge Status Indication**
- **Package Design Allows Flush Seating on a PC Board**
- **May be Side Stacked on 4.57 mm (0.18") Centers**
- **Up to 8 Units May be Coupled for a Horizontal Array Configuration with a Common Coupling Bar (See T-1 Right Angle Array Data Sheet)**
- **LEDs Available in All LED Colors, With or Without Integrated Current Limiting Resistor in T-1 Packages**
- **Easy Flux Removal Design**
- **Housing Material Meets UL 94V-0 Rating**
- **Additional Catalog Lamps Available as Options**

Description

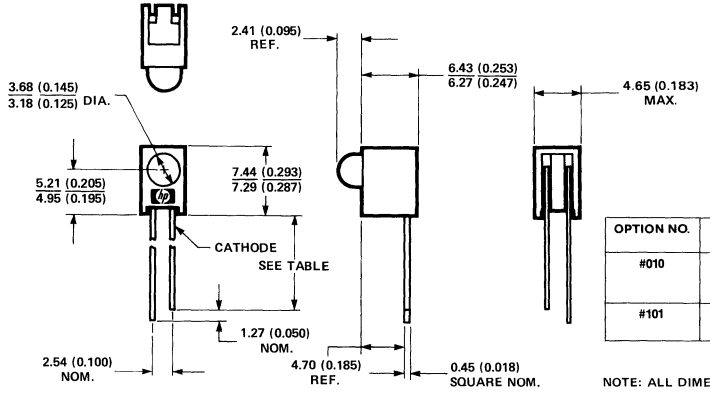
Hewlett-Packard T-1 Right Angle Indicators are industry standard status indicators that incorporate a T-1 LED lamp in a black plastic right angle mount housing. The indicators are available in Standard Red, High Efficiency Red, Orange, Yellow, and High Performance Green, with or without an integrated current limiting resistor. These products are designed to be used as back panel diagnostic indicators and card edge logic status indicators.



Ordering Information

To order other T-1 High Dome Lamps in Right Angle Housings in addition to the parts indicated above, select the base

Package Dimensions



OPTION NO.	CATHODE LEAD LENGTH	ANODE LEAD LENGTH	
#010	18.03 (0.710) MIN.	1.27 (0.050) NOM. LONGER THAN CATHODE	UNSHEARED UNEVEN LEADS
#101	3.43 (0.135) MIN.	3.43 (0.135) MIN.	SHEARED EVEN LEADS

NOTE: ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).

part number and add the option code 010 or 101, depending on the lead length desired. For example, by ordering HLMP-1302 Option 010, you would receive the long lead option. By ordering HLMP-1302 Option 101, you would receive the short lead option.

Arrays made by connecting two to eight single Right Angle Indicators with a Common Coupling Bar are available. Ordering information for arrays may be found on the T-1 Right Angle Array data sheet.

Absolute Maximum Ratings and Other Electrical/Optical Characteristics

The absolute maximum ratings and typical device characteristics are identical to those of the T-1 LED lamps. For information about these characteristics, see the data sheets of the equivalent T-1 LED lamp.

T-1 (3 mm) Right Angle Arrays

Technical Data

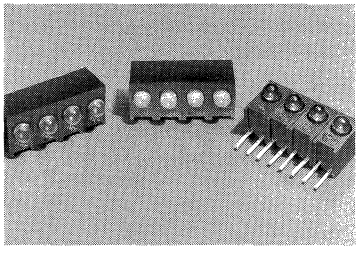
Option 102, 103, 104, 105, 106, 107, 108

Features

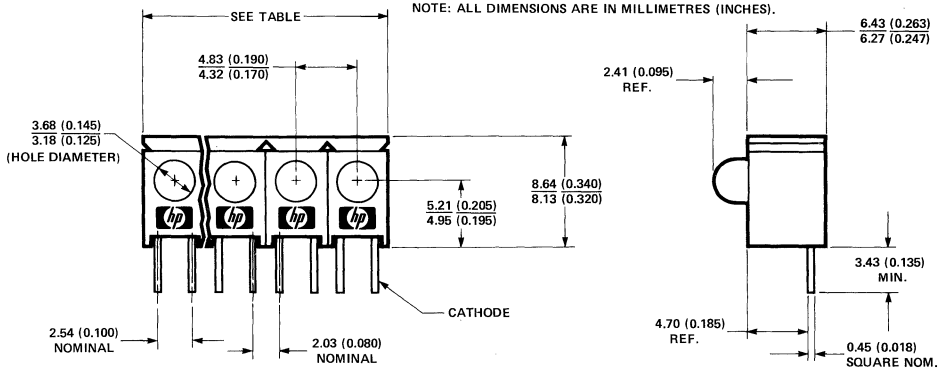
- **Ideal for PC Board Status Indication**
- **Standard 4 Element Configuration**
- **Easy Handling**
- **Easy Flux Removal**
- **Housing Meets UL 94V-O Flammability Rating**
- **Other Catalog Lamps Available**

Description

These T-1 right angle arrays incorporate standard T-1 lamps for a good balance of viewing angle and intensity. Single units are held together by a plastic tie bar. The leads of each member of the array are spaced on 2.54 mm (0.100 in.) centers. Lead spacing between adjacent lamps in the array is on 2.03 mm (0.080 in.) centers. These



Package Dimensions



OPTION NO.	ARRAY LENGTH	OPTION NO.	ARRAY LENGTH	OPTION NO.	ARRAY LENGTH
#102	9.65 (0.380) 8.79 (0.346)	#105	23.14 (0.911) 22.73 (0.895)	#108	36.70 (1.445) 36.45 (1.435)
#103	14.22 (0.560) 13.36 (0.526)	#106	27.71 (1.091) 27.31 (1.075)		
#104	18.57 (0.731) 18.16 (0.715)	#107	32.28 (1.271) 31.88 (1.255)		

products are designed to be used as back panel diagnostic indicators and logic status indicators on PC boards.

Ordering Information

Use the option code 102 through 108 in addition to the base part number to order these arrays. Example: HLMP-1300 option 102. Arrays from 2 to 8 elements in length and special lamp color combinations within an array are available. Please contact your nearest Hewlett-Packard Components representative for ordering information on these special items.

Absolute Maximum Ratings and Other Electrical/Optical Characteristics

The absolute maximum ratings and typical device characteristics are identical to those of the T-1 LED lamps. For information about these characteristics, see the data sheets of the equivalent T-1 LED lamp.

HEWLETT PACKARD

Subminiature LED Right Angle Indicators

Technical Data

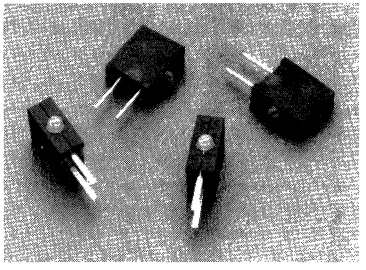
Option 010

Features

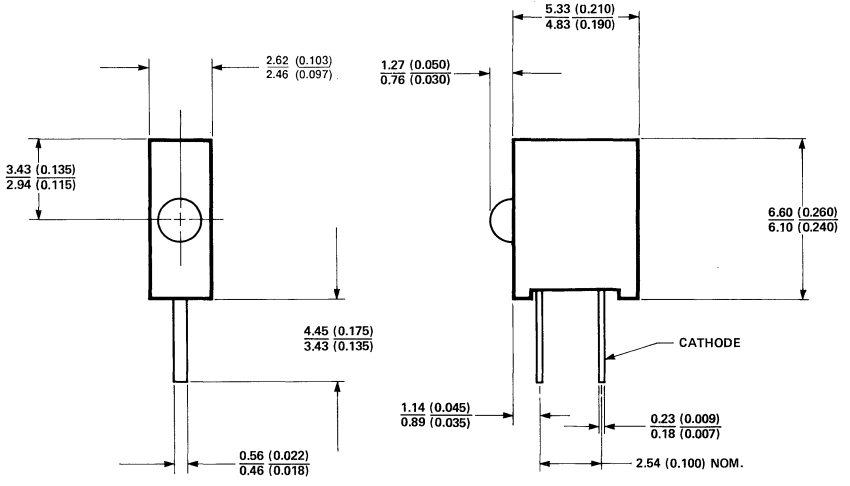
- **Ideal for PC Board Status Indication**
- **Side Stackable on 2.54 mm (0.100 in.) Centers**
- **Available in Four Colors**
- **Housing Meets UL 94V-O Flammability Rating**
- **Additional Catalog Lamps Available as Options**

Description

The Hewlett-Packard series of Subminiature Right Angle Indicators are industry standard status indicators that incorporate tinted diffused LED lamps in black plastic housings. The 2.54 mm (0.100 in.) wide packages may be side stacked for maximum board space savings. The silver plated leads are in line on 2.54 mm



Package Dimensions



NOTE: ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).

(0.100 in.) centers, a standard spacing that makes the PC board layout straight-forward. These products are designed to be used as back panel diagnostic indicators and logic status indicators on PC boards.

Ordering Information

To order Subminiature Right Angle indicators, order the base part number and add the option code 010. Example: HLMP-6300 option 010. For price and delivery on Resistor Subminiature Right Angle Indicators and other subminiature LEDs not indicated above, please contact your nearest HP Components representative.

Absolute Maximum Ratings and Other Electrical/Optical Characteristics

The absolute maximum ratings and typical device characteristics are identical to those of the Subminiature lamps. For information about these characteristics, see the data sheets of the equivalent Subminiature lamp.

Subminiature Solid State Lamps Standard Lead Bend Options

Technical Data

Option 011, 012, 013, 021, 022, 031, 032, 1L1, 1S1, 2L1, 2S1

Features

- **Surface Mount Lead Configurations**
- **Right Angle Lead Bend for Through Hole Mounting**
- **Tape and Reel in Accordance with ANSI/EIA RS-481 Specifications**

Description

Subminiature lamps (HLMP-PXXX, HLMP-Q1XX, HLMP-6XXX, HLMP-70XX) are available with the above standard options. Subminiature Lamps with Options 01X, 02X and 03X are suitable for surface mount applications and their leads are formed with gull wing, yoke bend and Z bend respectively. They are available in Tape and Reel (compatible to ANSI/EIA RS-481), bulk or arrays in a shipping tube. Option 1X1 and 2X1 are right angle lead bends suitable for through hole applications.

Ordering Information

To order Subminiature Lamps packaged with these standard options, include the appropriate option code along with the device catalog part number. Example: to order the HLMP-P005 with Option 011 gull wing leads in 12 mm embossed tape on 178 mm (7 inch) diameter reels, with 1500 lamps per reel; order as follows: HLMP-P005 Option 011. Order must be placed in reel increments. For any additional information, please contact your local Hewlett-Packard sales office or franchised distributor for assistance.

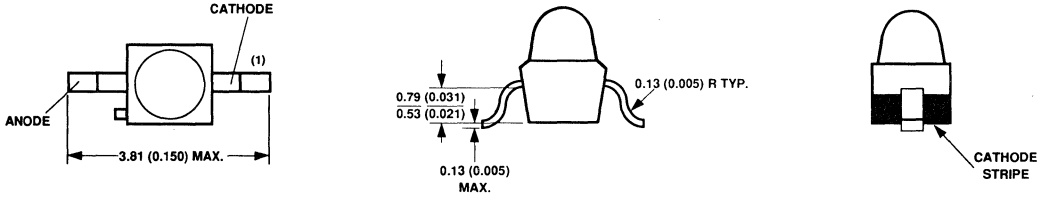
Selection Guide

Option Code	Package Configuration Description			Package Outline Drawing
011	Gull Wing Lead, Tape and Reel[2]		Surface Mount Lead Configurations	A, I, M
012	Gull Wing Lead, Bulk Packaging[3]			
013	Gull Wing Lead, Arrays, Shipping Tube			B, J
021	Yoke Lead, Tape and Reel[2]			C, K, M
022	Yoke Lead, Bulk Packaging[3]			
031	Z-Bend, Tape and Reel[2]			D, L, M
032	Z-Bend, Bulk Packaging[3]			
1L1	2.54 mm (0.100 inch) Center Lead Spacing	Long Leads; 10.4 mm (0.410 in.)	Right Angle Lead Bends for Through Hole Mounting	E
1S1		Short Leads; 3.7 mm (0.145 in.)		F
2L1	5.08 mm (0.200 inch) Center Lead Spacing	Long Leads; 9.2 mm (0.364 in.)		G
2S1		Short Leads; 3.7 mm (0.145 in.)		H

Notes:
1. Diffused lamps have tinted lenses. Nondiffused lamps have untinted lenses.
2. Lamps are supplied in 12 mm embossed tape on 178 mm (7 inch) diameter reels, with 1500 lamps per reel. Minimum order quantity and order increment are in quantity of reels only.
3. Vapor barrier bags are used for bulk packaging.

Package Dimensions, Lead Bend Options

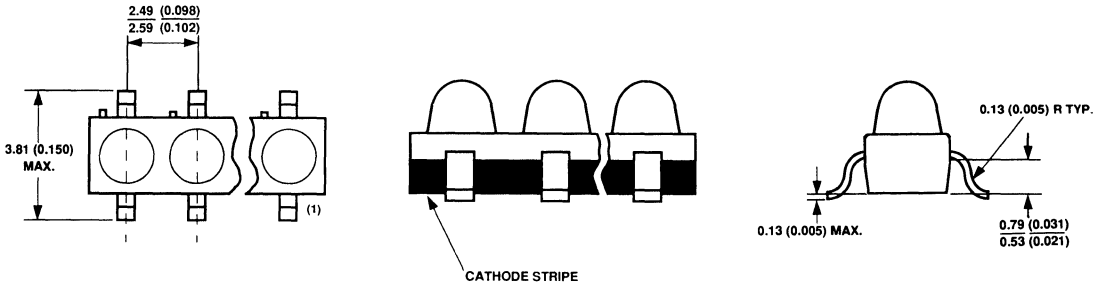
(A) Individual Lamp, Gull Wing Lead, Option 011 and 012



ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)

(1) DUE TO SHEARING PROCESS, LEAD WIDTH AT END MAY VARY 0.483 mm/0.663 mm.

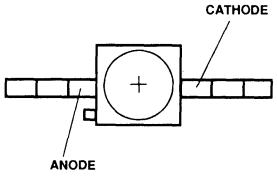
(B) Subminiature Array, Gull Wing Lead, Option 013



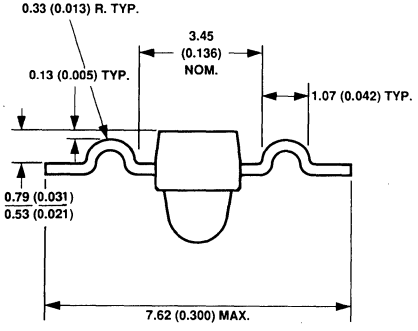
ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)

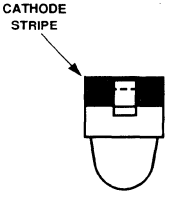
(1) DUE TO SHEARING PROCESS, LEAD WIDTH AT END MAY VARY 0.483 mm/0.663 mm.

(C) Individual Lamp, "Yoke" Lead, Options 021 and 022

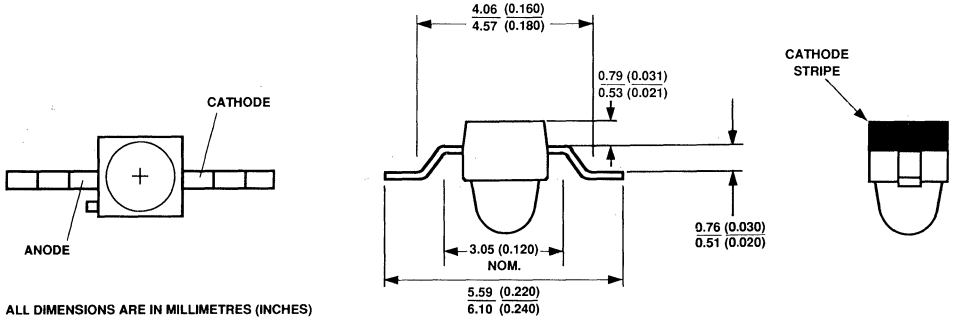


ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)



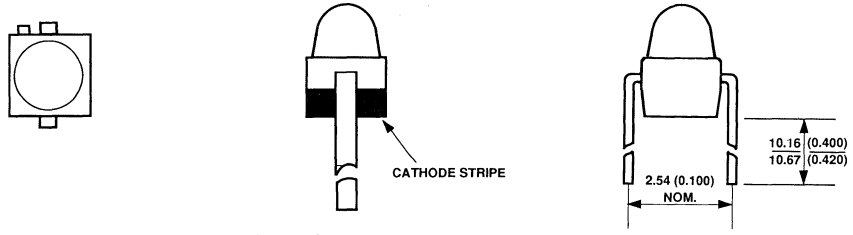


(D) Individual Lamp, Z-Bend Lead, Options 031 and 032



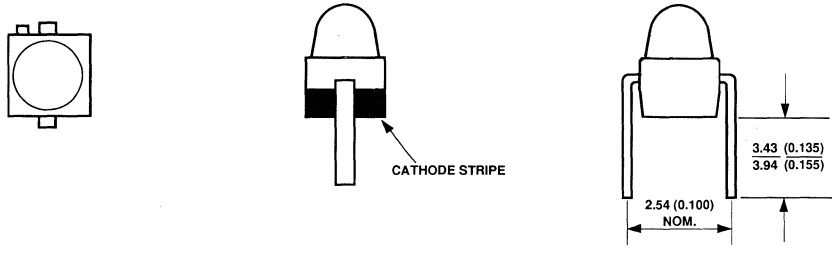
ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)

(E) Individual Lamp or Array, Rt. Angle Bend Option 1L1



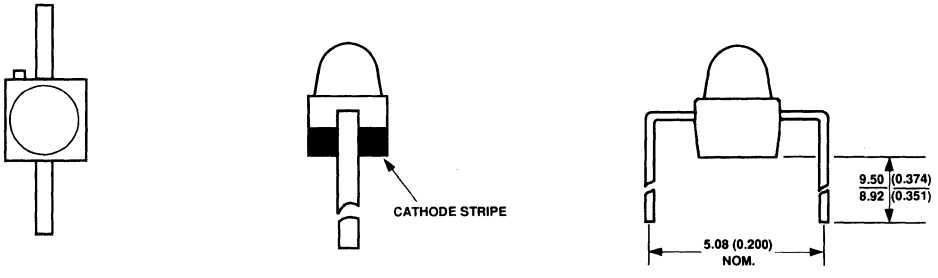
ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)

(F) Individual Lamp or Array, Rt. Angle Bend Option 1S1



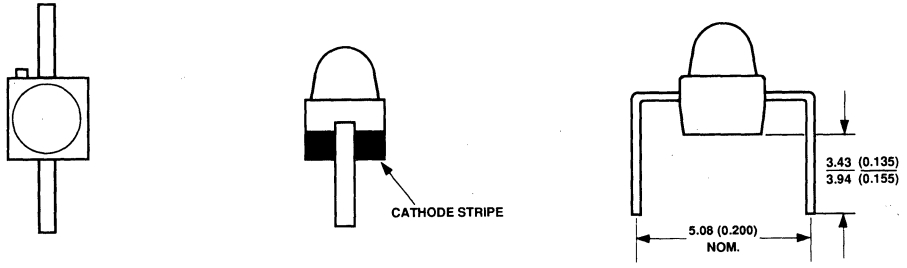
ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)

(G) Individual Lamp or Array, Rt. Angle Bend Option 2L1



ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)

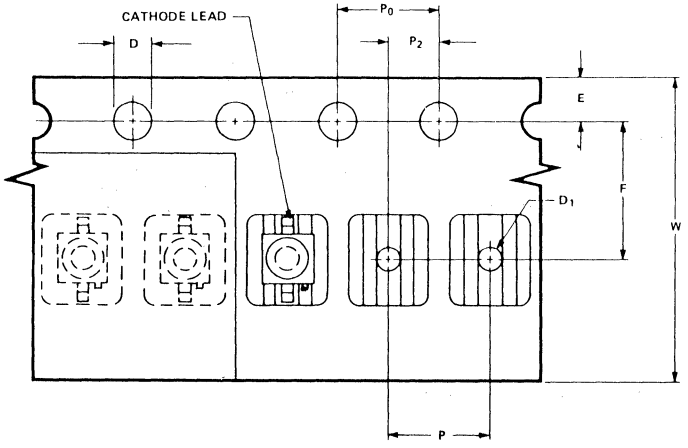
(H) Individual Lamp or Array, Rt. Angle Bend Option 2S1

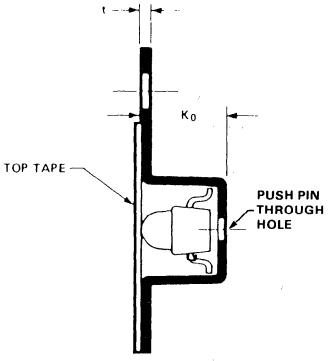


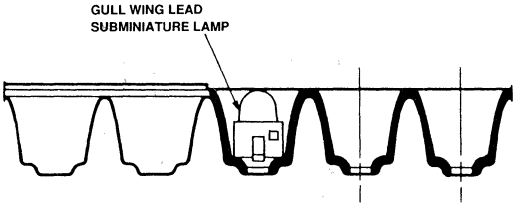
ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)

Package Dimensions: Surface Mount Tape and Reel Options

(I) 12 mm Tape and Reel, Gull Wing Lead, Option 011

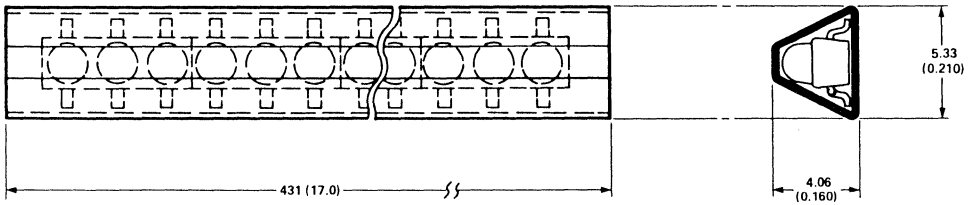


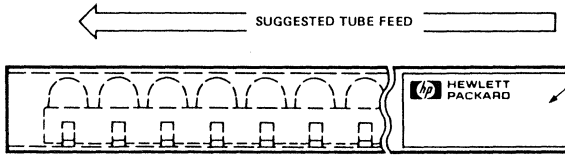




NOTES:
1. EMPTY COMPONENT POCKETS SEALED WITH TOP COVER TAPE.
2. 7 INCH REEL-1500 PIECES PER REEL.
3. MINIMUM LEADER LENGTH AT EITHER END OF THE TAPE IS 500 mm.
4. THE MAXIMUM NUMBER OF CONSECUTIVE MISSING LAMPS IS TWO.
5. IN ACCORDANCE WITH ANSI/EIA RS-481 SPECIFICATIONS, THE CATHODE IS ORIENTED TOWARDS THE TAPE SPROCKET HOLE.

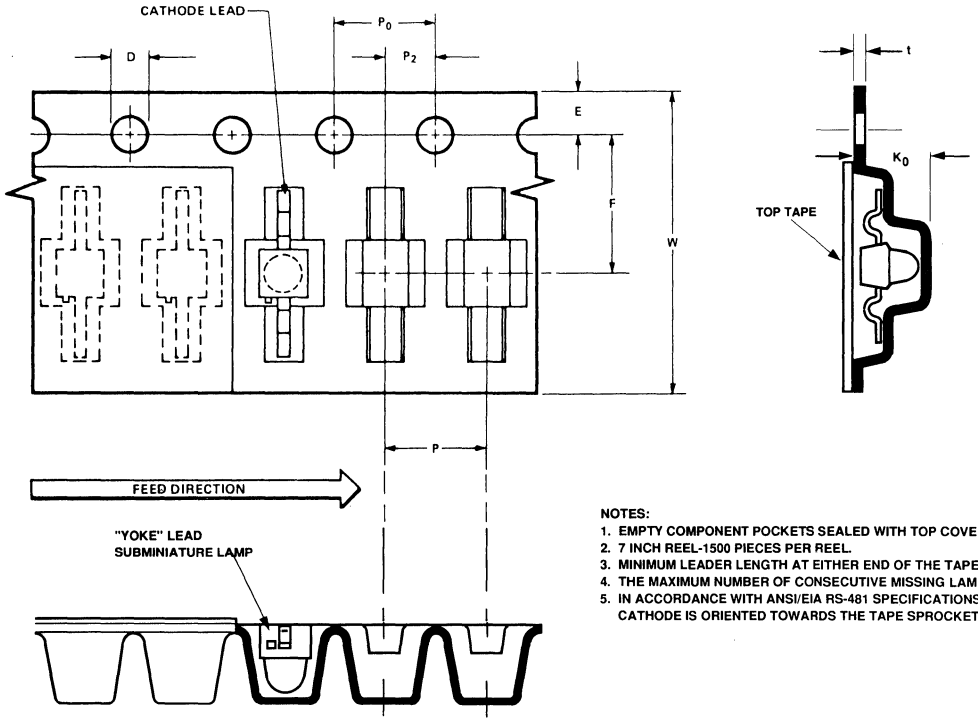
(J) Array Shipping Tube, Gull Wing Lead, Option 013





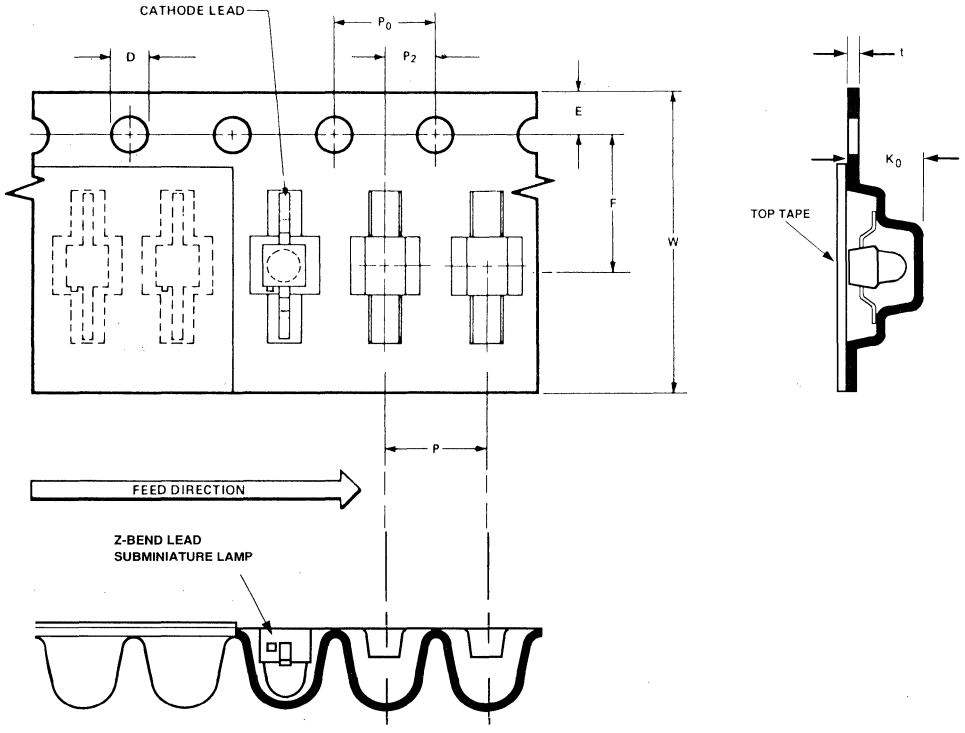
HLMP-	NO. OF LAMP ELEMENTS PER ARRAY	QUANTITY OF ARRAYS PER TUBE
6XX3	3	53
6XX4	4	40
6XX5	5	32
6XX6	6	26
6XX8	8	20

(K) 12 mm Tape and Reel, "Yoke" Lead, Option 021

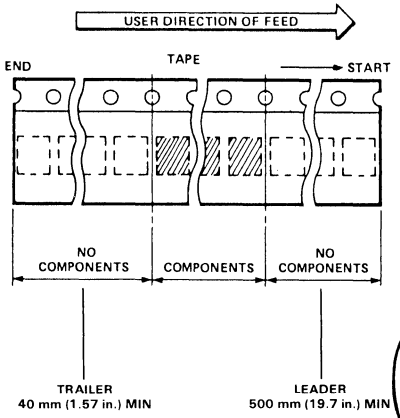


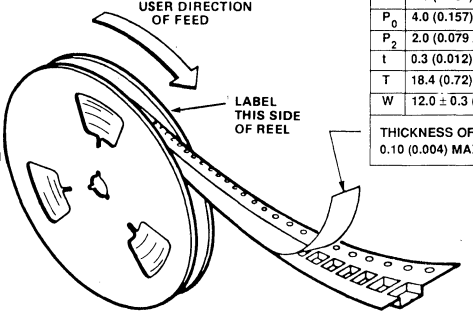
NOTES:
1. EMPTY COMPONENT POCKETS SEALED WITH TOP COVER TAPE.
2. 7 INCH REEL-1500 PIECES PER REEL.
3. MINIMUM LEADER LENGTH AT EITHER END OF THE TAPE IS 500 mm.
4. THE MAXIMUM NUMBER OF CONSECUTIVE MISSING LAMPS IS TWO.
5. IN ACCORDANCE WITH ANSI/EIA RS-481 SPECIFICATIONS, THE CATHODE IS ORIENTED TOWARDS THE TAPE SPROCKET HOLE.

(L) 12 mm Tape and Reel, Z-Bend Lead, Option



(M) 12 mm Tape and Reel

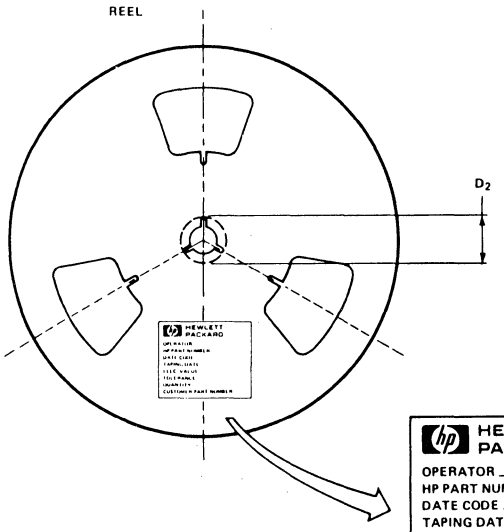


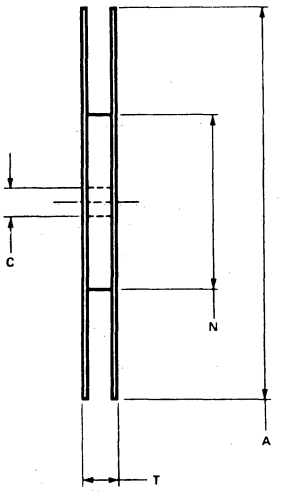


DIMENSIONS PER ANSI/EIA STANDARD RS-481.
ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).

A	178.0 ± 2.0 (7.0 ±0.08) DIA.
C	13.0 (0.512) DIA. TYP.
D	1.55 (0.061 ± 0.002) DIA.
D_1	1.0 (0.039) DIA. MIN.
D_2	20.2 (0.795) DIA. MIN.
E	1.75 ± 0.1 (0.069)
F	5.50 (0.127 ± 0.002)
K_0	3.05 ± 0.1 (0.120) TYP.
N	50.0 (1.970) MIN.
P	4.0 (0.157) TYP.
P_0	4.0 (0.157) TYP.
P_2	2.0 (0.079 ± 0.002) TYP.
t	0.3 (0.012) TYP.
T	18.4 (0.72) MAX.
W	12.0 ± 0.3 (0.472 ± 0.012)

THICKNESS OF TOP COVER TAPE 0.10 (0.004) MAX.





HEWLETT PACKARD
OPERATOR _____
HP PART NUMBER _____
DATE CODE _____
TAPING DATE _____
ELEC. VALUE _____
TOLERANCE _____
QUANTITY _____
CUSTOMER PART NUMBER _____

Convective IR Reflow Soldering

For information on IR reflow soldering, refer to Application Note 1060, *Surface Mounting SMT LED Components.*

HEWLETT PACKARD

LED Indicators Standard Intensity and Color Binning Options

Technical Data

Option S02, S20, S22

Description

Due to applications that require tightly matched devices, Hewlett-Packard has developed several standard options to service these requirements.

Option S02 consists of devices which are selected to two Iv categories. All color bins of the base parts (yellow and green devices) fulfill the color requirements of these products.

Option S20 consists of devices which are selected to two color bins. All Iv bins of the base parts fulfill the Iv requirements of these products.

Option S22 consists of devices which are selected to two Iv categories and two color bin categories.

Ordering Information

To order LED indicators with these standard options, order the base part number and add the option code (S02, S20, S22). For any base part number that does not appear in the following lists, please consult your local Hewlett-Packard representative or your local franchise distributor.

OPTION S02 – Partial base part number list:

HLMP-D101
HLMP-D105
HLMP-D150
HLMP-D155
HLMP-D401
HLMP-K100
HLMP-K101
HLMP-K105
HLMP-K150
HLMP-K155
HLMP-K402
HLMP-L250
HLMP-R100
HLMP-S200
HLMP-S300
HLMP-S400
HLMP-S500
HLMP-T200
HLMP-T300
HLMP-T500
HLMP-0300
HLMP-0400
HLMP-0503
HLMP-0800
HLMP-1002
HLMP-1100
HLMP-1120
HLMP-1301
HLMP-1302
HLMP-1320
HLMP-1321
HLMP-1340
HLMP-1385
HLMP-1402
HLMP-1421
HLMP-1440
HLMP-1485
HLMP-1521
HLMP-1523
HLMP-1540
HLMP-1550
HLMP-1585
HLMP-1600
HLMP-1601
HLMP-1620
HLMP-1640
HLMP-1700
HLMP-1719
HLMP-1790
HLMP-3001
HLMP-3002
HLMP-3301
HLMP-3316
HLMP-3351
HLMP-3401
HLMP-3416
HLMP-3451
HLMP-3502
HLMP-3507
HLMP-3517
HLMP-3519
HLMP-3554
HLMP-3600
HLMP-3650
HLMP-3680
HLMP-3744
HLMP-3750
HLMP-3810
HLMP-3850
HLMP-3860
HLMP-3910
HLMP-3950
HLMP-3960

HLMP-4000
HLMP-4600
HLMP-4700
HLMP-4719
HLMP-4740
HLMP-5030
HLMP-5040
HLMP-5050
HLMP-5060
HLMP-5070
HLMP-5080
HLMP-6001
HLMP-6300
HLMP-6305
HLMP-6400
HLMP-6500
HLMP-6505
HLMP-7000
HLMP-7019
HLMP-7040
HLMP-8109
HLMP-8110
HLMP-8115
HLMP-8205
HLMP-8209
HLMP-8305
HLMP-8309
HLMP-8320
HLMP-8405
HLMP-8409
HLMP-8505
HLMP-8509
HLMP-8510
HLMP-8520

OPTION S20 - Partial base part number list:

HLMP-1620
HLMP-1640
HLMP-3400
HLMP-3651

OPTION S22 - Partial base part number list:

HLMP-S301
HMLP-S500
HLMP-T300
HLMP-T500
HLMP-0401
HLMP-0504
HLMP-1402
HLMP-1440
HLMP-1523
HLMP-1620
HLMP-1719
HLMP-3401
HLMP-3450
HLMP-3850
HLMP-3862
HLMP-4719

HEWLETT PACKARD

Hermetic Lamps

Hermetic Lamps

Hewlett-Packard offers a complete line of hermetically sealed solid state lamps, hi-rel screened to military specifications, and listed on MIL-S-19500 Qualified Parts List (QPL).

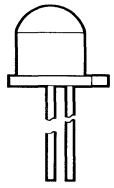
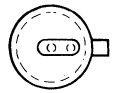
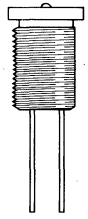
- JAN and JANTX hermetic and panel mount hermetic lamps, screened to the requirements of MIL-S-19500 slash sheet specifications and listed on the MIL-S-19500 Qualified Parts List.
- Ultrabright hermetic and ultrabright panel mount hermetic lamps screened to the JAN and JANTX requirements of MIL-S-19500.

These military grade hermetic and panel mount hermetic lamps are produced and hi-rel screened at Hewlett-Packard's DESC qualified facilities, approved to the requirements of MIL-S-19500 and MIL-STD-750.

The applicable MIL-S-19500 screening tables are detailed on each hermetic lamp data sheet.

Commercial grade versions of these hermetic lamps are available without hi-rel screening, identified by 1NXXXX or HLMP- part numbers.

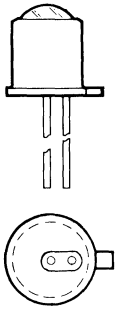
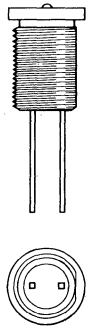
Hermetically Sealed JAN Qualified LED Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
 	1N5765 JAN1N5765[1] JANTX1N5765[1]	Red (640 nm)	Hermetic/T0-46	Red Diffused	1.0 mcd @ 20 mA	70°	1.6 V @ 20 mA	3-194
	1N6092 JAN1N6092[1] JANTX1N6092[1]	High Efficiency Red (626 nm)			8.0 mcd @ 20 mA		2.0 V @ 20 mA	
	1N6093 JAN1N6093[1] JANTX1N6093[1]	Yellow (585 nm)		Yellow Diffused	8.0 mcd @ 20 mA		2.0 V @ 20 mA	
	1N6094 JAN1N6094[1] JANTX1N6094[1]	Green (570 nm)		Green Diffused	8.0 mcd @ 25 mA		2.1 V @ 25 mA	
 	HLMP-0930 HLMP-0931	Red (640 nm)	Panel Mount Version	Red Diffused	1.0 mcd @ 20 mA	70°	1.6 V @ 20 mA	
	JANM19500/ 51901[1] JTXM19500/ 51902[1]	High Efficiency Red (626 nm)			8.0 mcd @ 20 mA		2.0 V @ 20 mA	
	JANM19500/ 52001[1] JTXM19500/ 52002[1]	Yellow (585 nm)		Yellow Diffused	8.0 mcd @ 20 mA		2.0 V @ 20 mA	
	JANM19500/ 52101[1] JTXM19500/ 52102[1]	Green (570 nm)		Green Diffused	8.0 mcd @ 25 mA		2.1 V @ 25 mA	

Note:

1. Military qualified and listed on the MIL-S-19500 Qualified Parts List (QPL).

Hermetically Sealed JAN Qualified Ultra-Bright LED Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	1N6609 JAN1N6609[1] JANTX1N6609[1]	High Efficiency Red (626 nm)	Hermetic T0-18[3]	Clear Glass	50.0 mcd @ 20 mA	18	2.0 V @ 20 mA	3-206
	1N6610 JAN1N6610[1] JANTX6610[1]	Yellow (585 nm)			50.0 mcd @ 20 mA		2.0 V @ 20 mA	
	1N6611 JAN1N6611[1] JANTX6611[1]	Green (570 nm)			50.0 mcd @ 25 mA		2.1 V @ 25 mA	
	JANM19500/ 51903[1] JANTXM19500/ 51904[1]	High Efficiency Red (626 nm)	Panel Mount Version	Clear Glass	50.0 mcd @ 20 mA	18	2.0 V @ 20 mA	
	JANM19500/ 52003[1] JANTXM19500/ 52004[1]	Yellow (585 nm)			50.0 mcd @ 20 mA		2.0 V @ 20 mA	
	JANM19500/ 52103[1] JANTXM19500/ 52104[1]	Green (570 nm)			50.0 mcd @ 25 mA		2.1 V @ 25 mA	

Notes:

1. Military qualified and listed on theMIL-S-19500 Qualified Parts List (QPL).

HEWLETT PACKARD

JAN Qualified Hermetic Solid State Lamps*

Technical Data

1N5765
JAN1N5765
JANTX1N5765
1N6092
JAN1N6092
JANTX1N6092
1N6093
JAN1N6093
JANTX1N6093
1N6094
JAN1N6094
JANTX1N6094

Features

- **Military Qualified**
- **Listed on MIL-S-19500 QPL**
- **Choice of Four Colors**
  Red
  High Efficiency Red
  Yellow
  Green
- **Designed for High-Reliability Applications**
- **Hermetically Sealed**
- **Wide Viewing Angle**
- **Low Power Operation**
- **IC Compatible**
- **Long Life**
- **Panel Mount Configuration**

Description

The 1N5765, 1N6092, 1N6093 and 1N6094 solid state LEDs are hermetically sealed in a TO-46 package with a tinted, diffused plastic lens over a glass window. These devices are designed for high reliability applications and provide excellent on-off contrast, high axial luminous intensity, and a wide viewing angle. The panel mount versions consist of an LED unit permanently mounted in an anodized aluminum sleeve.

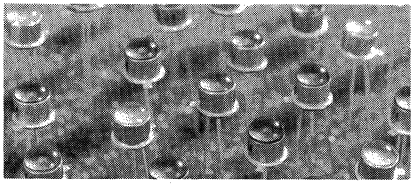
The 1N5765 utilizes a GaAsP LED chip with a red diffused lens over a glass window.

The 1N6092 has a high efficiency red GaAsP on GaP LED chip with a red diffused lens over a glass window. This device is comparable to the 1N5765 but its efficiency extends to higher currents and it provides greater luminous intensity.

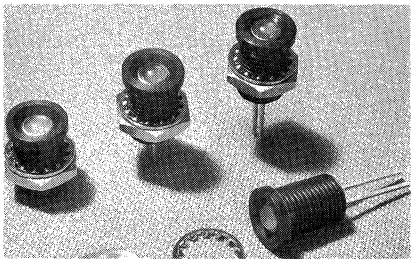
The 1N6093 provides a yellow GaAsP on GaP LED chip with a yellow, diffused lens over a glass window.

The 1N6094 utilizes a green GaP LED chip with a green, diffused lens over a glass window.

The plastic lens over glass window system is extremely durable and has exceptional temperature cycling capabilities.



HERMETIC TO-46 LAMP



PANEL MOUNT LAMP ASSEMBLY

*Panel mount versions of all of the above are available per the selection matrix on the next page.

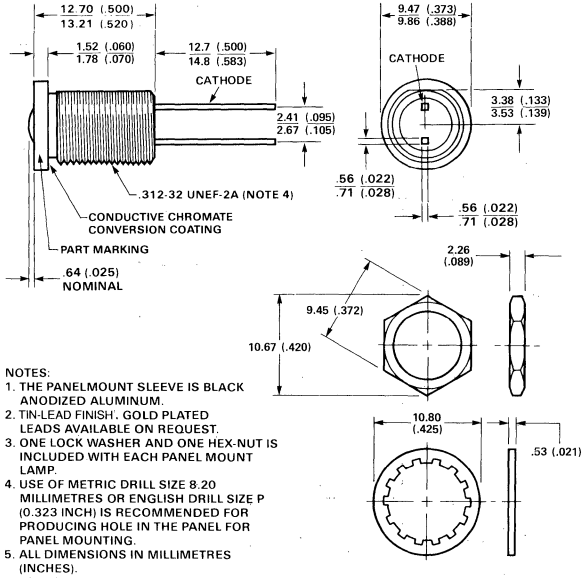
Selection Guide

COLOR – PART NUMBER – LAMP AND PANEL MOUNT MATRIX				
Description	**Standard Product**	**With JAN Qualification[1]**	**JAN Plus TX Testing[2]**	**Controlling MIL-S-19500 Document[4]**
TABLE A. Hermetic TO-46 Part Number System				
Standard Red	1N5765	JAN1N5765	JANTX1N5765	/467
High Efficiency Red	1N6092	JAN1N6092	JANTX1N6092	/519
Yellow	1N6093	JAN1N6093	JANTX1N6093	/520
Green	1N6094	JAN1N6094	JANTX1N6094	/521
TABLE B. Panel Mountable Part Number System[3]				
Standard Red	HLMP-0904	HLMP-0930	HLMP-0931	None
High Efficiency Red	HLMP-0354	HLMP-0380 (JANM19500/51901)	HLMP-0381 (JTXM19500/51902)	/519
Yellow	HLMP-0454	HLMP-0480 (JANM19500/52001)	HLMP-0481 (JTXM19500/52002)	/520
Green	HLMP-0554	HLMP-0580 (JANM19500/52101)	HLMP-0581 (JTXM19500/52102)	/521

Notes:
1. Parts are marked with the JAN part number.
2. Parts are marked with the JANTX part number.
3. Panel mountable packaging incorporates the Table A TO-46 part into a panel mount enclosure.
4. JAN and JANTX parts only.

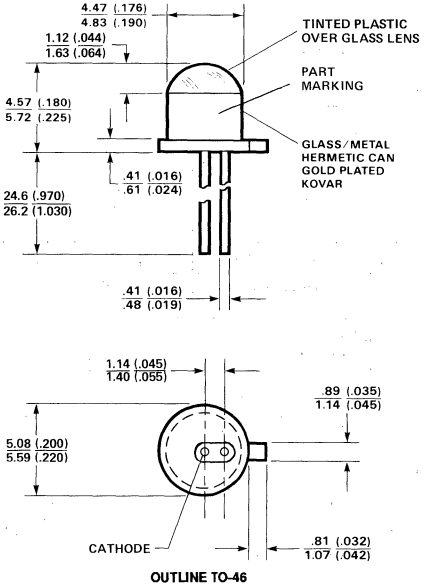
Package Dimensions

HLMP-0904, 0354, 0454, 0554



NOTES:
1. THE PANELMOUNT SLEEVE IS BLACK ANODIZED ALUMINUM.
2. TIN-LEAD FINISH. GOLD PLATED LEADS AVAILABLE ON REQUEST.
3. ONE LOCK WASHER AND ONE HEX-NUT IS INCLUDED WITH EACH PANEL MOUNT LAMP.
4. USE OF METRIC DRILL SIZE 8.20 MILLIMETRES OR ENGLISH DRILL SIZE P (0.323 INCH) IS RECOMMENDED FOR PRODUCING HOLE IN THE PANEL FOR PANEL MOUNTING.
5. ALL DIMENSIONS IN MILLIMETRES (INCHES).
6. PACKAGE WEIGHT INCLUDING LAMP AND PANEL MOUNT IS 1.2 - 1.8 GRAMS. NUT AND WASHER IS AN EXTRA 0.6 - 1.0 GRAM.

1N5765, 1N6092, 1N6093, 1N6094



OUTLINE TO-46

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. GOLD-PLATED KOVAR LEADS.
3. PACKAGE WEIGHT OF LAMP ALONE IS .25 - .40 GRAMS.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	Red 1N5765 HLMP-0904	High Eff. Red 1N6092 HLMP-0354	Yellow 1N6093 HLMP-0454	Green 1N6094 HLMP-0554	Units
Power Dissipation (derate linearly from 50°C at 1.6 mW/°C)	100	120	120	120	mW
DC Forward Current	50[1]	35[2]	35[2]	35[2]	mA
Peak Forward Current	1000 See Fig. 5	60 See Fig. 10	60 See Fig. 15	60 See Fig. 20	mA
Operating and Storage Temperature Range	-65°C to +100°C				
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 7 seconds				

Notes:
1. Derate from 50°C at 0.2 mA/°C.
2. Derate from 50°C at 0.5 mA/°C.

Electrical/Optical Characteristics at $T_A = 25°C$

		1N5765/ HLMP-0904			1N6092/ HLMP-0354			1N6093/ HLMP-0454			1N6094/ HLMP-0554				
Sym.	Description	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units	Test Conditions
I_{V1}	Axial Luminous Intensity	0.5	1.0		3.0	8.0		3.0	8.0		3.0	8.0		mcd	I_F = 20 mA Figs. 3, 8, 13, 18 $\theta = 0°$
I_{V2}	Luminous Intensity at $\theta = 30°$	1.5			1.5			1.5			1.5			mcd	I_F = 20 mA $\theta = 30°$
$2\theta_{1,2}$	Included Angle Between Half Luminous Intensity Points[1]		60			70			70			70		deg	Figures 6, 11, 16, 21
λ_{PEAK}	Peak Wavelength	630	655	700	590	635	695	550	583	660	525	565	600	nm	Measurement at Peak
λ_d	Dominant Wavelength[2]		640			626			585			570		nm	
τ_S	Speed of Response		10			200			200			200		ns	
C	Capacitance		200	300		35	100		35	100		35	100	pF	$V_F = 0$; f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance*[3]		425			425			425			425		°C/W	
$R\theta_{J\text{-}PIN}$	Thermal Resistance**[3]		550			550			550			550		°C/W	
V_F	Forward Voltage		1.6	2.0		2.0	3.0		2.0	3.0		2.1	3.0	V	I_F = 20 mA Figures 2, 7, 12, 17
I_R	Reverse Current			1.0			1.0			1.0			1.0	μA	V_R = 3 V
BV_R	Reverse Breakdown Voltage	4.0	5.0		5.0			5.0			5.0			V	I_R = 100 μA
η_v	Luminous Efficacy[4]		56			140			455			600		lm/W	

Notes:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Junction to Cathode Lead with 3.18 mm (0.125 inch) of leads exposed between base of flange and heat sink.
4. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e=I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

*Panel mount.
**T0-46.

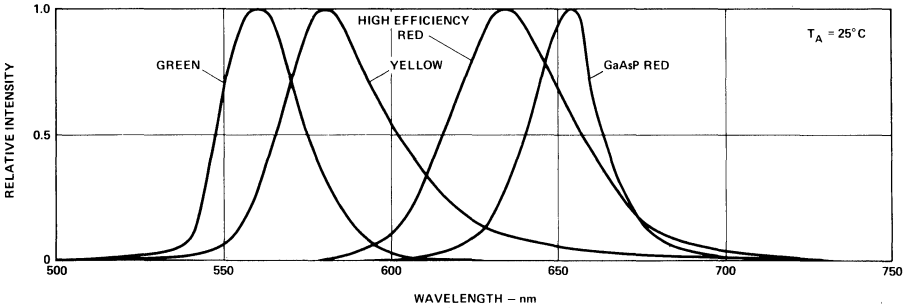


Figure 1. Relative Intensity vs. Wavelength.

Family of Red 1N5765/HLMP-0904

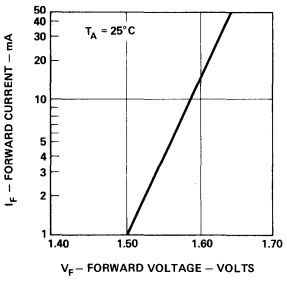


Figure 2. Forward Current vs. Forward Voltage.

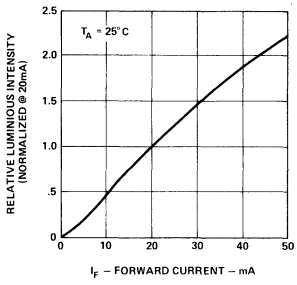


Figure 3. Relative Luminous Intensity vs. Forward Current.

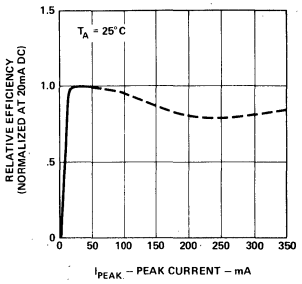


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

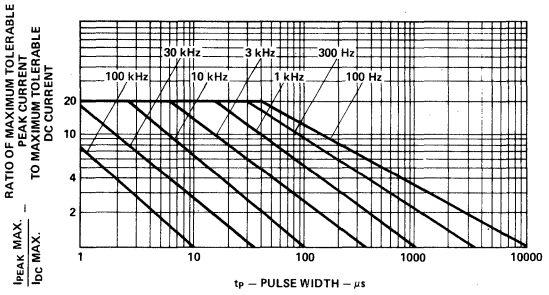


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

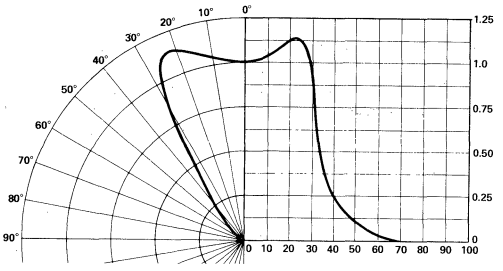


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

Family of High Efficiency Red 1N6092/HLMP-0354

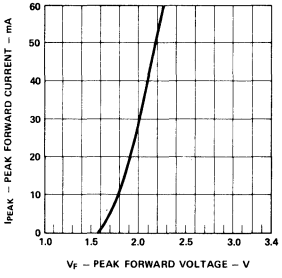


Figure 7. Forward Current vs. Forward Voltage.

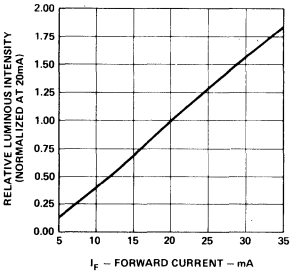


Figure 8. Relative Luminous Intensity vs. Forward Current.

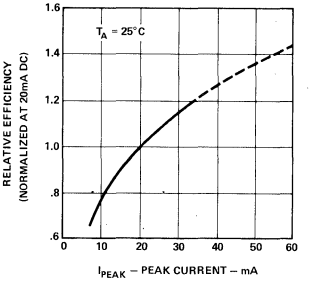


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

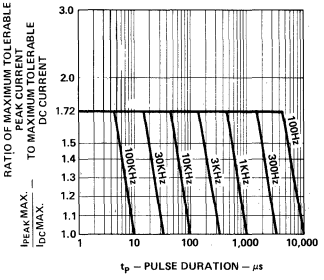


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

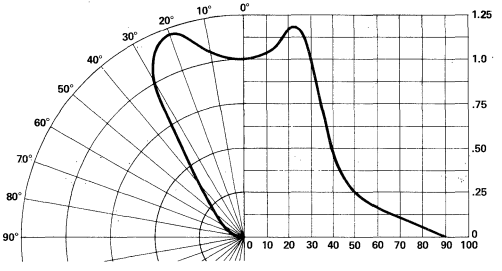


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Family of Yellow 1N6093/HLMP-0454

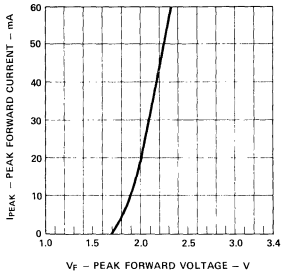


Figure 12. Forward Current vs. Forward Voltage.

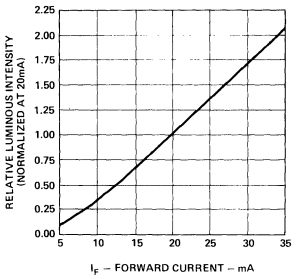


Figure 13. Relative Luminous Intensity vs. Forward Current.

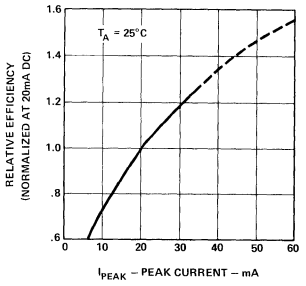


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

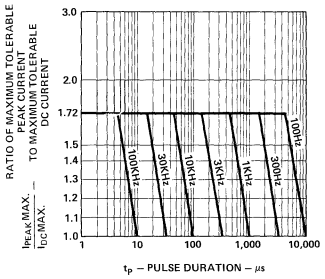


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

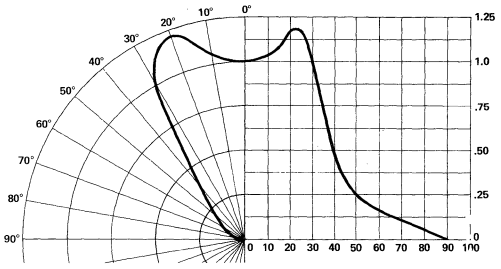


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

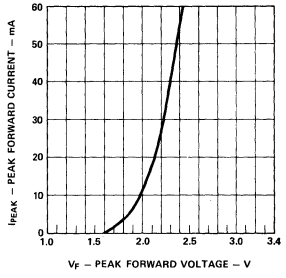


Figure 17. Forward Current vs. Forward Voltage.

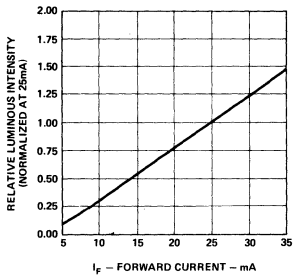


Figure 18. Relative Luminous Intensity vs. Forward Current.

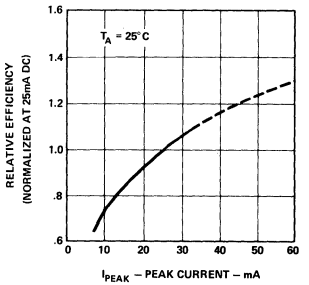


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

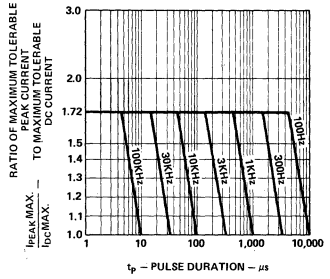


Figure 20. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

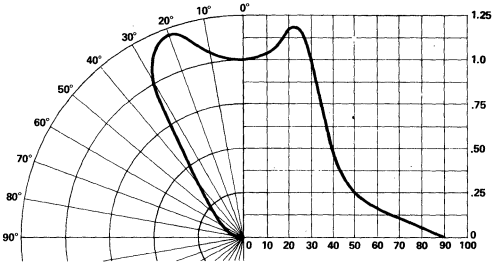


Figure 21. Relative Luminous Intensity vs. Angular Displacement.

JAN PART: Samples of each lot are subjected to Group A and B tests listed below. Every six months, samples from a single lot of each part type are subjected to Group C testing. All tests are to the conditions and limits specified by the appropriate MIL-S-19500 slash sheet specifications.

JANTX PART: These devices undergo 100% screening tests as listed below to the conditions and limits specified by the MIL-S-19500 slash sheet specification. The JANTX lot has also been subjected to Group A, B, and C sample tests as for the JAN PART above.

The following test tables apply to 1N6092, 1N6093 and 1N6094 devices. Refer to MIL-S-19500/467 slash sheet specifications for 1N5765 devices.

Table I. 100% Screening

Examination or Test	MIL-STD-750	
	Method	Conditions
1. High Temperature Life	1032	T_A = +100°C, Time = 24 hours
2. Temperature Cycling	1051	Condition A, T (high) = +100°C
3. Constant Acceleration	2006	20,000 g's. Y1 Axis
4. Fine Leak	1071	Condition H
5. Gross Leak	1071	Condition K, Test Temperature = +100°C
6. Electrical Test		I_V, V_F, and I_R, T_A = 25°C
7. Burn-In[1]	1015	I_F = 35 mA, T_A = 25°C, Time = 96 hours
8. Final Electrical Test		Same as Step 6
9. Deltas Determinations		ΔI_{V1} = -20%, V_F = ±50 mV
10. External Visual[1]	2071	

Note:
1. MIL-STD-883 Method applies.

Table II. Group A Inspection for TO-46 Lamps

Examination or Test	MIL-STD-750		LTPD	Symbol	Limits		Unit
	Method	Details			Min.	Max.	
Subgroup 1			5				
Visual and mechanical inspection	2071						
Subgroup 2			5				
Luminous intensity		I_F = 20 mA dc;[1] θ = 0°		I_{V1}	0.5[2] 3.0[3]		mcd mcd
Luminous intensity		I_F = 20 mA dc;[1] θ = 30°		I_{V2}	0.3[2] 1.5[3]		mcd mcd
Reverse current	4016	DC method; V_R = 3 V dc		I_R		1.0	μA dc
Forward current	4011	DC method; I_F = 20 mA[1]		V_F		3.0	V dc
Subgroup 3			10				
High temperature:		T_A = 100°C					
Reverse current	4016	DC method; V_R = 3 V dc		I_R		1.0	μA dc
Forward voltage	4011	DC method; I_F = 20 mA[1]		V_F		3.0	V dc
Low Temperature:		T_A = -55°C					
Reverse current	4016	DC method; V_R = 3 V dc		I_R		1.0	μA dc
Forward voltage	4011	DC method; I_F = 20 mA[1]		V_F		3.0	V dc
Subgroup 4			5				
Capacitance	4001	V_R = 0; f = 1 MHz		C		100	pF

Notes:
1. I_F = 25 mA for 1N6094.
2. For 1N5765.
3. For 1N6092, 1N6093, and 1N6094.

Table III. Group B Inspection

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Limits Min.	Limits Max.	Unit
Subgroup 1			15				
Solderability	2026						
Resistance to solvents	1022						
Subgroup 2			10				
Thermal shock (temperature cycle)	1051	Test condition A T (high) = 100°C; 25 cycles					
Hermetic seal	1071	Test condition H					
Fine leak							
Gross Leak		Test condition C or K, indicator fluid/device maintained at 100°C ±5°C					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°		I_{V1}	0.5[1] 3.0[2]		mcd mcd
Subgroup 3			5				
Steady-state-operation life	1027	I_F = 35 mA dc, 340 hours T_A = 25°C					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°		I_{V1}	0.45[1] 2.7[2]		mcd mcd
Subgroup 4							
Decap internal design verification	2075	Test 1 device/0 failure					
Subgroup 5							
(Not applicable)							
Subgroup 6			7				
High temperature life (nonoperating)	1032	T_A = 100°C, 340 hours					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°		I_{V1}	0.45[1] 2.7[2]		mcd mcd

Notes:
1. For 1N5765.
2. For 1N6092, 1N6093, and 1N6094.
3. 25 mA for 1N6094.

Table IV. Group C Inspection

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Limits Min.	Limits Max.	Unit
Subgroup 1			15				
Physical dimensions	2066						
Subgroup 2			10				
Thermal shock (glass strain)	1056	Test condition A					
Terminal strength	2036	Test condition E					
Hermetic seal	1071						
Fine leak		Test condition H					
Gross leak		Test condition C or K, indicator fluid/device maintained at 100°C ± 5°C					
Moisture resistance	1021	Omit initial conditioning					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°	I_{V1}		0.5[1] 3.0[2]		mcd mcd
Subgroup 3			10				
Shock	2016	Nonoperating, 1500 g's, 0.5 ms, 5 blows in X1, Y1, Z1 orientation					
Vibration, variable frequency	2056	Nonoperating					
Constant acceleration	2006	20,000 g's X1, Y1, Z1 orientation					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°	I_{V1}		0.5[1] 3.0[2]		mcd mcd
Subgroup 4			15				
Salt atmosphere (corrosion)	1041						
Subgroup 5 (Not applicable)							
Subgroup 6							
Steady-state-operation life	1027	I_F = 35 mA dc, 1000 hours, T_A = 25°C					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°	I_{V1}		0.45[1] 2.7[2]		mcd mcd

Table V. Group C Inspection (continued)

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Limits Min.	Limits Max.	Unit
Subgroup 7			10				
Peak forward pulse current (transient)		t_p = 1 µs, pps = 300, total test time = 5 s, I_{ptr} = 1.0 A(pk)					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°		I_{V1}	0.45[1] 2.7[2]		mcd mcd
Subgroup 8			10				
Peak forward pulse current (operating)		t_p = 0.5 ms, $P_{FM} \leq$ 120 mW, T_A = 25°C, I_P = 60 mA, 500 hours					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°		I_{V1}	0.45[1] 2.7[2]		mcd mcd

Notes:
1. For 1N5765.
2. For 1N6092, 1N6093, and 1N6094.
3. I_F = 25 mA for 1N6094.

Table VI. Group A Inspection for Panel Mount Lamps

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Limits Min.	Limits Max.	Unit
Subgroup 1			5				
External visual examination	2071						
Subgroup 2			5				
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°		I_{V1}	0.5[1] 3.0[2]		mcd mcd
Forward voltage		DC method: I_F = 20 mA[3]		V_F		3.0	V dc
Reverse current		DC method: V_R = 3 V dc		I_R		1.0	µA dc
Subgroup 3			5				
Resistance to solvents	1022	Omit solution 2.1d					
Subgroup 4			5				
Physical dimensions	2066						

Notes:
1. For 1N5765.
2. For 1N6092, 1N6093, and 1N6094.
3. I_F = 25 mA for 1N6094.

HEWLETT PACKARD

JAN Qualified Ultra-Bright Hermetic Solid State Lamps*

Technical Data

1N6609
JAN1N6609
JANTX1N6609
1N6610
JAN1N6610
JANTX1N6610
1N6611
JAN1N6611
JANTX1N6611

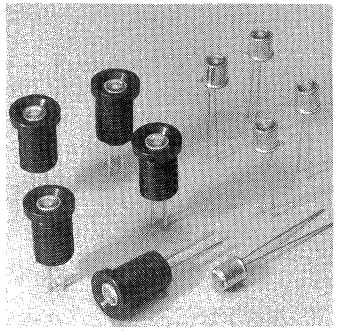
Features

- **Military Qualified**
- **Listed on MIL-S-19500 QPL**
- **Sunlight Viewable with Proper Contrast Enhancement Filter**
- **Hermetically Sealed**
- **Choice of Three Colors**
  High Efficiency Red
  Yellow
  High Performance Green
- **Low Power Operation**
- **IC Compatible**
- **Long Life/Reliable/Rugged**
- **Panel Mount Configuration**

Description

The 1N6609, 1N6610, and 1N6611 are hermetically sealed solid state lamps in a TO-18 package with a clear glass lens. These hermetic lamps provide improved brightness over conventional hermetic LED lamps, excellent on-off contrast, and high axial luminous intensity. These LED indicators are designed for use in applications requiring readability in bright sunlight. With a proper contrast enhancement filter, these LED indicators are readable in sunlight ambients, see Application Note 1015 *Contrast Enhancement Techniques for LED Displays.* The panel mount versions consist of an LED unit permanently mounted in an anodized aluminum sleeve.

The 1N6609 utilizes a high efficiency red GaAsP on GaP LED chip. The 1N6610 uses a yellow GaAsP on GaP LED chip. The 1N6611 uses a green GaP LED chip.



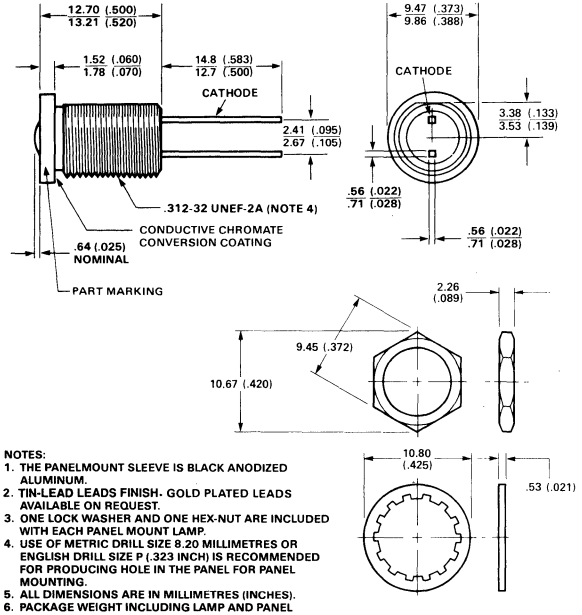
*Panel Mount versions of all of the above are available per the selection matrix on the next page.

Selection Guide

COLOR – PART NUMBER – LAMP AND PANEL MOUNT MATRIX				
Description	**Standard Product**	**With JAN Qualification[1]**	**JAN Plus TX Testing[2]**	**Controlling MIL-S-19500 Document[4]**
TABLE A. Hermetic TO-18 Part Number System				
High Efficiency Red	1N6609	JAN1N6609	JANTX1N6609	/519
Yellow	1N6610	JAN1N6610	JANTX1N6610	/520
Green	1N6611	JAN1N6611	JANTX1N6611	/521
TABLE B. Panel Mountable Part Number System[3]				
High Efficiency Red	HLMP-0364	HLMP-0365 (JANM19500/51903)	HLMP-0366 (JANTXM19500/51904)	/519
Yellow	HLMP-0464	HLMP-0465 (JANM19500/52003)	HLMP-0466 (JANTXM19500/52004)	/520
Green	HLMP-0564	HLMP-0565 (JANM19500/52103)	HLMP-0566 (JANTXM19500/52104)	/521

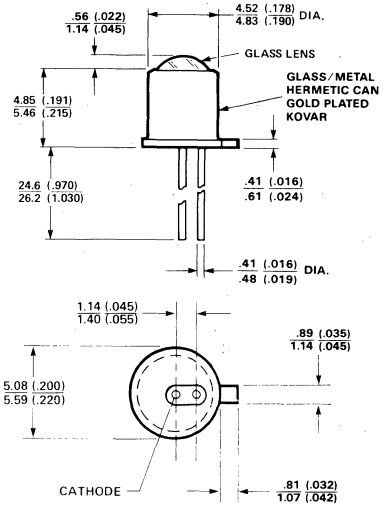
Notes:
1. Parts are marked with JAN part number.
2. Parts are marked with JANTX/JTX part number.
3. Panel mountable packaging incorporates the Table A TO-18 part into a panel mount enclosure.
4. JAN and JANTX parts only.

HLMP-0364, 0464, 0564



NOTES:
1. THE PANELMOUNT SLEEVE IS BLACK ANODIZED ALUMINUM.
2. TIN-LEAD LEADS FINISH. GOLD PLATED LEADS AVAILABLE ON REQUEST.
3. ONE LOCK WASHER AND ONE HEX-NUT ARE INCLUDED WITH EACH PANEL MOUNT LAMP.
4. USE OF METRIC DRILL SIZE 8.20 MILLIMETRES OR ENGLISH DRILL SIZE P (.323 INCH) IS RECOMMENDED FOR PRODUCING HOLE IN THE PANEL FOR PANEL MOUNTING.
5. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
6. PACKAGE WEIGHT INCLUDING LAMP AND PANEL MOUNT IS 1.2 - 1.8 GRAMS. NUT AND WASHER IS AN EXTRA .6 - 1.0 GRAM.

1N6609, 1N6610, 1N6611



OUTLINE TO-18

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. GOLD-PLATED KOVAR LEADS.
3. PACKAGE WEIGHT OF LAMP ALONE IS .25 - .40 GRAMS.

Absolute Maximum Ratings at T_A = 25°C

Parameter	High Efficiency Red 1N6609 HLMP-0364	Yellow 1N6610 HLMP-0464	Green 1N6611 HLMP-0564	Units
Power Dissipation (derate linearly from 50°C at 1.6 mW/°C)	120	120	120	mW
DC Forward Current	35[1]	35[1]	35[1]	mA
Peak Forward Current	60 See Fig. 5	60 See Fig. 10	60 See Fig. 15	mA
Operating and Storage Temperature	-65°C to +100°C			
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 7 seconds.			

Note:
1. Derate from 50°C at 0.5 mA/°C.

Electrical/Optical Characteristics at T_A = 25°C

Symbol	Description	1N6609 HLMP-0364			1N6610 HLMP-0464			1N6611 HLMP-0564			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{V1}	Axial Luminous Intensity	20	50		20	50		20	50		mcd	I_F = 20 mA Figs. 3, 8, 13 θ = 0°
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points[1]		18			18			18		deg.	Figures 6, 11, 16
λ_{PEAK}	Peak Wavelength	590	635	695	550	583	660	525	565	600	nm	Measurement at Peak
λ_d	Dominant Wavelength[2]		626			585			570		nm	
τ_S	Speed of Response		200			200			200		ns	
C	Capacitance		35	100		35	100		35	100	pF	V_F = 0; f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance*[3]		425			425			425		°C/W	
$R\theta_{J\text{-}PIN}$	Thermal Resistance**[3]		550			550			550		°C/W	
V_F	Forward Voltage		2.0	3.0		2.0	3.0		2.1	3.0	V	I_F = 20 mA Figures 2, 7, 12,
I_R	Reverse Current			1.0			1.0			1.0	μA	V_R = 3 V
BV_R	Reverse Break-down Voltage	5.0			5.0			5.0			V	I_R = 100 μA
η_v	Luminous Efficacy[4]		140			455			600		lm/W	

Notes:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Junction to Cathode Lead with 3.18 mm (0.125 inch) of leads exposed between base of flange and heat sink.
4. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

*Panel mount.
**T0-18.

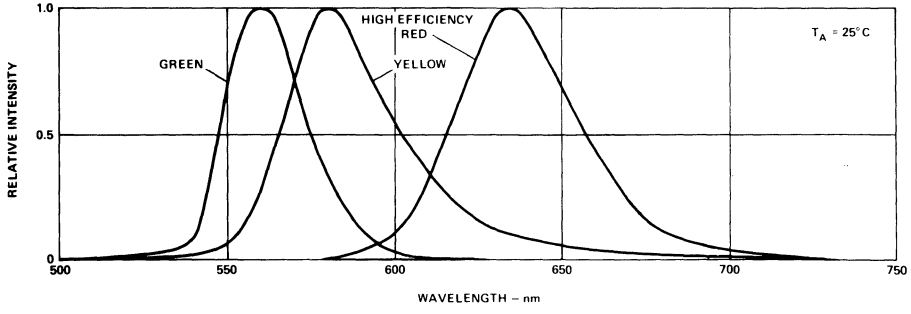


Figure 1. Relative Intensity vs. Wavelength.

Family of High Efficiency Red 1N6609/HLMP-0364

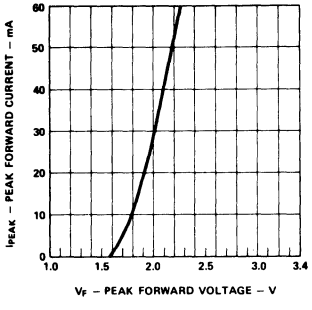


Figure 2. Forward Current vs. Forward Current.

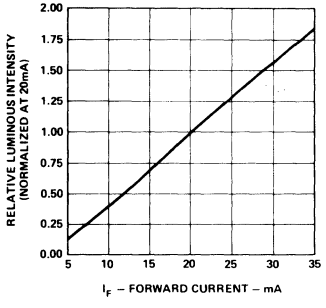


Figure 3. Relative Luminous Intensity vs. Forward Current.

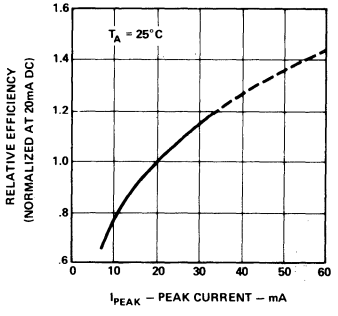


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

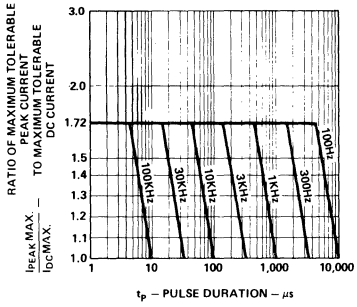


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

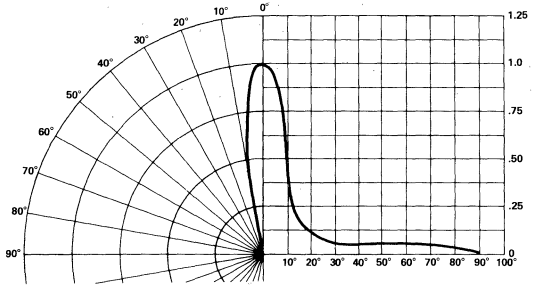


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

Family of Yellow 1N6610/HLMP-0464

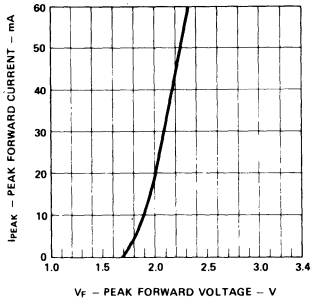


Figure 7. Forward Current vs. Forward Voltage.

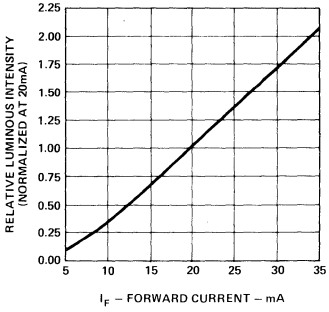


Figure 8. Relative Luminous Intensity vs. Forward Current.

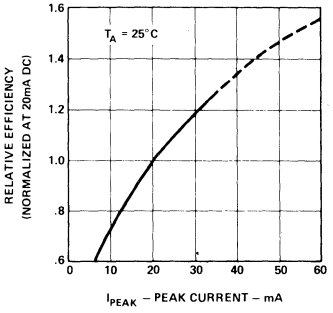


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

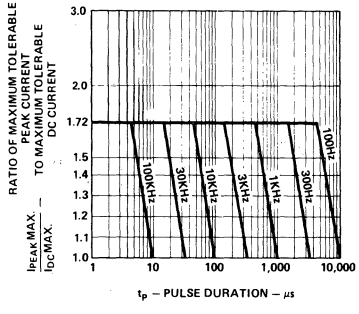


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

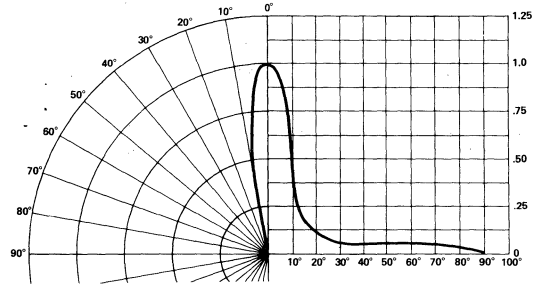


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Family of Green 1N6611/HLMP-0564

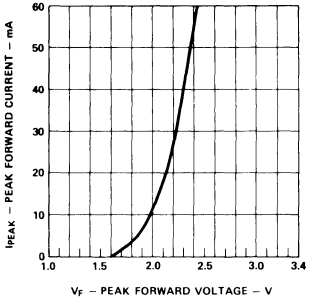


Figure 12. Forward Current vs. Forward Voltage.

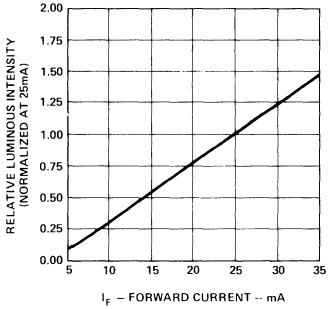


Figure 13. Relative Luminous Intensity vs. Forward Current.

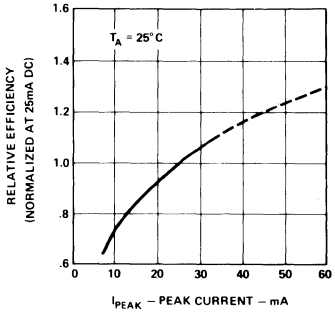


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

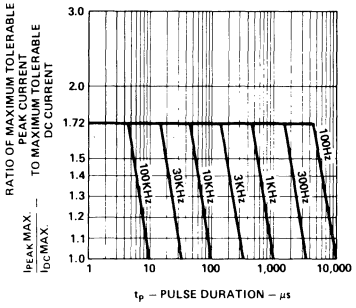


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

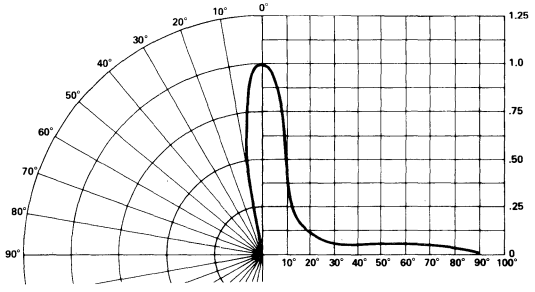


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

JAN PART: Samples of each lot are subjected to Group A and B tests listed below. Every six months, samples from a single lot of each part type are subjected to Group C testing. All tests are to the conditions and limits specified by the appropriate MIL-S-19500 slash sheet specification.

JANTX PART: These devices undergo 100% screening tests as listed below to the conditions and limits specified by the MIL-S-19500 slash sheet specification. The JANTX lot has also been subjected to Group A, B, and C sample tests as for the JAN PART above.

Table I. 100% Screening

Examination or Test	MIL-STD-750	
	Method	Conditions
1. High Temperature Life	1032	T_A = +100°C, Time = 24 hours
2. Temperature Cycling	1051	Condition A, T (high) = +100°C
3. Constant Acceleration	2006	20,000 g's. Y1 Axis
4. Fine Leak	1071	Condition H
5. Gross Leak	1071	Condition K, Test Temperature = +100°C
6. Electrical Test		I_V, V_F, and I_R, T_A = 25°C
7. Burn-In[1]	1015	I_F = 35 mA, T_A = 25°C, Time = 96 hours
8. Final Electrical Test		Same as Step 6
9. Deltas Determinations		ΔI_{V1} = -20%, V_F = ±50 mV
10. External Visual[1]	2071	

Note:
1. MIL-STD-883 Method applies.

Table II. Group A Inspection for TO-18 Lamps

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Sym.	Limits Min.	Limits Max.	Unit
Subgroup 1 Visual and mechanical inspection	2071		5				
Subgroup 2 Luminous intensity		I_F = 20 mA dc;[1] θ = 0°	5	I_{V1}	20.0		mcd
Reverse current	4016	DC method; V_R = 3 V dc		I_R		1.0	µA dc
Forward current	4011	DC method; I_F = 20 mA		V_F		3.0	V dc
Subgroup 3 High temperature:		T_A = 100°C	10				
Reverse current	4016	DC method; V_R = 3 V dc		I_R		1.0	µA dc
Forward voltage	4011	DC method; I_F = 20 mA[1]		V_F		3.0	V dc
Low Temperature:		T_A = -55°C					
Reverse current	4016	DC method; V_R = 3 V dc		I_R		1.0	µA dc
Forward voltage	4011	DC method; I_F = 20 mA[1]		V_F		3.0	V dc
Subgroup 4 Capacitance	4001	V_R = 0; f = 1 MHz	5	C		100	pF
Subgroups 5, 6, and 7 Not applicable							

Note:
1. I_F = 25 mA for 1N6611.

Table III. Group B Inspection

Examination or Test	MIL-STD-750		LTPD	Symbol	Limits		Unit
	Method	Details			Min.	Max.	
Subgroup 1			15				
Solderability	2026						
Resistance to solvents	1022						
Subgroup 2			10				
Thermal shock (temperature cycle)	1051	Test condition A, T (high) = 100°C; 25 cycles					
Hermetic seal	1071	Test condition H					
Fine leak							
Gross Leak		Test condition C or K, leak indicator fluid/ device maintained at 100°C ±5°C					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	20.0		mcd
Subgroup 3			5				
Steady-state-operation life	1027	I_F = 35 mA dc, 340 hours, T_A = 25°C					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	18.0		mcd
Subgroup 4							
Decap internal design verification	2075	Test 1 device/0 failure					
Subgroup 5							
(Not applicable)							
Subgroup 6			7				
High temperature life (nonoperating)	1032	T_A = 100°C, 340 hours					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	18.0		mcd

Note:
1. I_F = 25 mA for 1N6611.

Table IV. Group C Inspection

Examination or Test	MIL-STD-750		LTPD	Symbol	Limits		Unit
	Method	Details			Min.	Max.	
Subgroup 1			15				
Physical dimensions	2066						
Subgroup 2			10				
Thermal shock (glass strain)	1056	Test condition A					
Terminal strength	2036	Test condition E					
Hermetic seal	1071						
Fine leak		Test condition H					
Gross leak		Test condition C or K, indicator fluid/device maintained at 100°C ±5°C					
Moisture resistance	1021	Omit initial conditioning					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	20.0		mcd
Subgroup 3			10				
Shock	2016	Nonoperating, 1500 g's, 0.5 ms, 5 blows in X1, Y1, Z1 orientation.					
Vibration, variable frequency	2056	Nonoperating					
Constant acceleration	2006	20,000 g's; X1, Y1, Z1 orientation					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	20.0		mcd
Subgroup 4			15				
Salt atmosphere (corrosion)	1041						
Subgroup 5 (Not applicable)							
Subgroup 6							
Steady-state-operation life	1027	I_F = 35 mA dc, 1000 hours, T_A = 25°C					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	18.0		mcd

Table IV. Group C Inspection (cont.)

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Limits Min.	Limits Max.	Unit
Subgroup 7			10				
Peak forward pulse current (transient)		t_p = 1 µs, pps = 300, total test time = 5 s, I_{ptr} = 1.0 A(pk)					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	18.0		mcd
Subgroup 8			10				
Peak forward pulse current (operating)		t_p = 0.5 ms, $P_{FM} \leq$ 120 mW, T_A = 25°C, I_F = 60 mA, 500 hours					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	18.0		mcd

Note:
1. I_F = 25 mA for 1N6611.

Table V. Group A Inspection for Panel Mount Assemblies

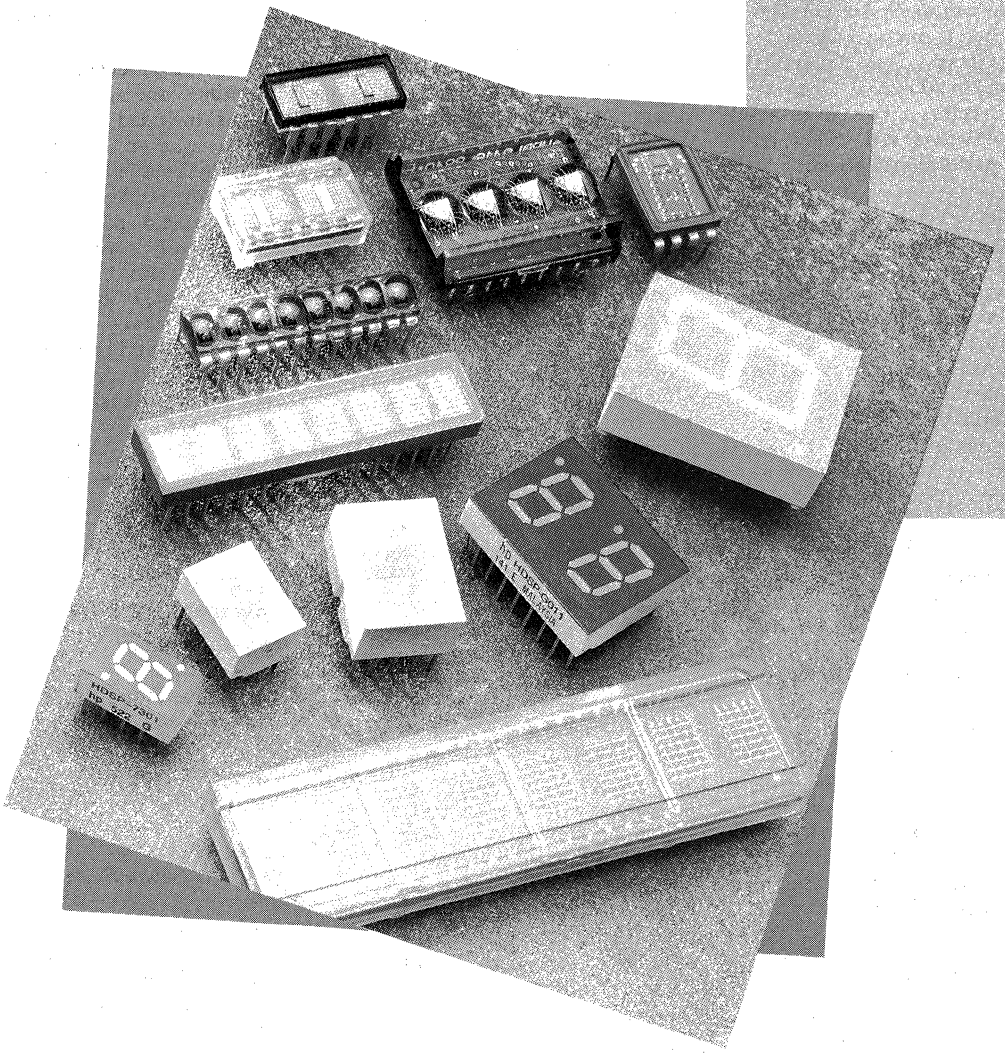
Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Limits Min.	Limits Max.	Unit
Subgroup 1			5				
External visual examination	2071						
Subgroup 2			5				
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	20.0		mcd
Forward voltage		DC method: I_F = 20 mA[1]		V_F		3.0	V dc
Reverse current		DC method: V_R = 3 V dc		I_R		1.0	µA dc
Subgroup 3			5				
Resistance to solvents	1022	Omit solution 2.1d					
Subgroup 4			5				
Physical dimensions	2066						

Note:
1. I_F = 25 mA for HLMP-0564.

HEWLETT PACKARD

Solid State Displays

- Seven Segment Numeric Displays
- Alphanumeric Displays
- Hexadecimal Displays
- Hermetic Displays



Solid State Displays

Hewlett-Packard's line of Solid State Displays answers all the needs of the designer. From small alphanumeric displays to low cost numeric displays the selection is complete. They range in sizes from 3 mm (0.15 inches) to 20 mm (0.8 inches) and in colors of red, AlGaAs red, high efficiency red, yellow, and high performance green.

Hewlett-Packard's 5 X 7 dot matrix alphanumeric displays are available in several different packages; 4, 8, and 16 characters, and 3.8 mm (0.15 inches), 5 mm (0.2 inches), and 6.9 mm (0.27 inches) font sizes. All the dot matrix displays are available in four colors: high efficiency red, orange, yellow, and green. Many of the newer and most popular products are also now available in AlGaAs Red. Standard Red is also available in many of the products. This wide diversity of packages, font heights, and colors mean solutions for your diverse applications.

Many new additions are now available to HP's alphanumeric display line. In the intelligent display family look for the HDSP-250X large font (0.27 inches) eight digit, HDSP-253X medium font (0.2 inches) eight digit displays. For high performance, the HCMS-29XX small and medium font (0.15 inches and 0.20 inches) four, eight, and sixteen digit displays. For your hi-reliability applications the HDSP-665X medium font (0.20 inches) four character hermetic displays are also available. These new products double the intelligent alphanumeric displays available. They give each customer a wider choice of new products to design into medical equipment, avionics, telecommunications, computer products, industrial or office equipment applications.

Also part of HP's alphanumeric display line is the large (0.68 inches and 1.04 inches) 5 X 7 dot matrix alphanumeric display family. This family offers standard red, high efficiency red, AlGaAs red, and high performance green colors. Viewing distance is excellent. You can read the 1.04 inch character font at up to 18 meters (12 meters for the 0.68 inch display). Applications for these large 5 X 7 displays include industrial machinery and process controllers, weighing scales, computer tape drives, and transportation.

Hewlett-Packard also features a broad line of numeric seven segment displays. Included are low cost, standard red displays to high light ambient displays producing 7.5 mcd/segment. HP's 0.3 inches, 0.4 inches, 0.43 inches, 0.56 inches, and 0.8 inches, characters can provide a solution to every display need. HP's product offering includes 0.4 inches and 0.56 inches dual digit displays and a line of small package, bright 0.3 inches displays - the 0.3 inches Microbright. HP's broad line of numeric seven segment displays is ideal for electronic instrumentation, industrial, weighing scales, point-of-sale terminals, game machines, and appliance applications. Included in HP's line of numeric seven segment displays is the Double Heterojunction AlGaAs red low current sunlight viewable display family. This family is available in the 0.3 inches Mini 0.4 inches, 0.43 inches, 0.56 inches, and 0.8 inches package sizes. These AlGaAs numeric displays are very bright at low drive currents - typical intensity of 650 mcd/segment at 1 mA/segment drive. These displays are ideal for battery operated and other low power applications.

NEW Products!

Seven Segment Displays

Black Surface Seven Segment Displays

These devices use industry standard size package and pinout. They are available with a black surface finish. All devices are available as either common anode or cathode.

Orange Color Seven Segment Displays

These devices are designed with industry standard size packages and pinouts and utilize Hewlett-Packard's GaP to achieve a bright orange color. They have

been added to two (2) Seven Segment Display family of products (10 mm Seven Segment Displays; 78 mm Ultra-Mini Seven Segment Displays). New orange products (14.2 mm, 20 mm) to be introduced shortly. Contact your local Field Engineer for more up-to-date information.

Ultra Mini 8 mm (0.31") Seven Segment Displays
The 8 mm (0.31 inch) LED seven segment displays are HP's most space-efficient character size. They are designed for viewing distances up to 3 metres (10 feet). The numeric devices feature a right hand decimal point. All devices are available as either common anode or common cathode.

Alphanumeric Displays:

CMOS 5x7 Small Alphanumeric Displays
Three 5X7 dot matrix alphanumeric displays come in four, eight and sixteen character packages. The four character (HCMS-270X series) is a dual in-line 12 pin plastic package. The on-board CMOS ICs form a 28 bit shift register. The eight character (HCMS-271X Series) is a dual in-line plastic package with 26 pin positions. The on-board CMOS ICs form a 56 bit shift register. The sixteen character (HCMS-272X series) are assembled by enclosing two HCMS-271X devices in a common lens assembly forming two rows of eight characters. The plastic package had two dual in-line rows of 26 pin positions for a total of 52 pin positions. The two on-board CMOS IC 56 bit shift registers for each row are electrically separate from each other. The on-board CMOS ICs form serial input shift registers with constant current output LED row drivers. Decoded column data is clocked into the shift registers for each refresh cycle. Full character display is accomplished with external column strobing at a refresh rate of 100 Hz or faster.

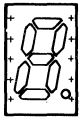
All of these display devices may be end stacked in the X-direction to form a strong of characters if desired length.

High Performance CMOS 5x7 Alphanumeric Displays
The HCMS-29XX series are high performance, easy to use dot matrix displays driven by on-board CMOS ICs. Each display can be directly interfaced with a microprocessor, thus eliminating the need for cumbersome interface components. The serial IC interface allows higher character count information displays with a minimum of data lines. A variety of colors, font heights, and character counts gives designers a wide range of product choices for their specific applications and the easy to read 57 pixel format allows the display of uppercase, lower case, Katakana, and custom -user defined characters. These displays are stackable in the X- and y- directions, making them ideal for high character count displays.

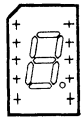
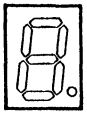
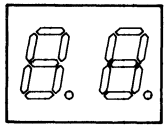
8 Character 5 mm and 7 mm Smart Alphanumeric Displays, 0.27 inches
A new size (7 mm, 0.27 inches) has been added to our existing 8 Character 5 mm Smart Alphanumeric Display family. These devices are 8-digit, 5X7 dot matrix alphanumeric displays and are all packaged in a standard 15.24 mm (0l6 inch) 28 pin dual-inline package. The products are designed for standard microprocessor interface techniques. The display and special features are accessed through a bidirectional 8-bit data bus.

8 Character 5 mm Smart Alphanumeric Displays
The HDSP-253X series is ideal for applications where displaying eight or more characters of dot matrix information in an aesthetically pleasing manner is required. They are eight digit, 5X7 dot matrix, alphanumeric displays. Seven brightness levels provide versatility versatility in adjusting the display intensity and power consumption. They are designed for standard microprocessor interface techniques. The display and special features are accessed through a bidirectional eight-bit data bus.

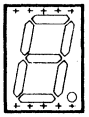
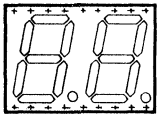
8 mm (0.31 inch) Ultra Mini Seven Segment Displays

Device	P/N	Description	Color	Typical I_v	Page No.
 8.0 mm (0.31 in.) Dual-in-Line 0.43" H x 0.28" W x 0.20" D	New HDSP-U001	Common Anode Right Hand Decimal, Gray Surface	Red	1100 µcd @ 20 mA	4-45
	New HDSP-U003	Common Cathode Right Hand Decimal, Gray Surface			
	New HDSP-U011	Common Anode Right Hand Decimal, Black Surface			
	New HDSP-U013	Common Cathode Right Hand Decimal, Black Surface			
	New HDSP-U101	Common Anode Right Hand Decimal, Gray Surface	AlGaAs Red	600 µcd @ 1 mA	
	New HDSP-U103	Common Cathode Right Hand Decimal, Gray Surface			
	New HDSP-U111	Common Anode Right Hand Decimal, Black Surface			
	New HDSP-U113	Common Cathode Right Hand Decimal, Black Surface			
	New HDSP-U201	Common Anode Right Hand Decimal, Gray Surface	High Efficiency Red	980 µcd @ 5 mA	
	New HDSP-U203	Common Cathode Right Hand Decimal, Gray Surface			
	New HDSP-U211	Common Anode Right Hand Decimal, Black Surface			
	New HDSP-U213	Common Cathode Right Hand Decimal, Black Surface			
	New HDSP-U301	Common Anode Right Hand Decimal, Gray Surface	Yellow	480 µcd @ 1 mA	
	New HDSP-U303	Common Cathode Right Hand Decimal, Gray Surface			
	New HDSP-U311	Common Anode Right Hand Decimal, Black Surface			
	New HDSP-U313	Common Cathode Right Hand Decimal, Black Surface			
	New HDSP-U501	Common Anode Right Hand Decimal, Gray Surface	Green	3000 µcd @ 10 mA	
	New HDSP-U503	Common Cathode Right Hand Decimal, Gray Surface			
	New HDSP-U511	Common Anode Right Hand Decimal, Black Surface			
	New HDSP-U513	Common Cathode Right Hand Decimal, Black Surface			
	New HDSP-U401	Common Anode Right Hand Decimal, Gray Surface	Orange	980 µcd @ 5 mA	
	New HDSP-U403	Common Cathode Right Hand Decimal, Gray Surface			
	New HDSP-U411	Common Anode Right Hand Decimal, Black Surface			
	New HDSP-U413	Common Cathode Right Hand Decimal, Black Surface			

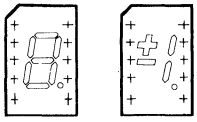
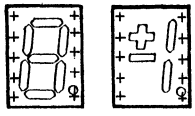
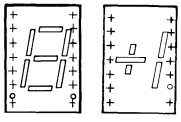
Black Surface Seven Segment Displays

Device	P/N	Description	Color	Typical I_v	Page No.
 7.62 mm (0.30 in.) Mini Dual-in-Line 0.5" H x 0.3" W x 0.24" D	New HDSP-A011 New HDSP-A013	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal	Red	1100 µcd @ 20 mA	4-20
	New HDSP-A211 New HDSP-A213	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal	High Efficiency Red	980 µcd @ 5 mA	
	New HDSP-A111 New HDSP-A113	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal	AlGaAs Red	600 µcd @ 1 mA	
	New HDSP-A511 New HDSP-A513	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal	Green	3000 µcd @ 10 mA	
 10.16 mm (0.40 in.) Dual-in-Line (Single Digit) 0.51" H x 0.39" W x 0.25" D	New HDSP-F011 New HDSP-F013	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal	Red	1200 µcd @ 20 mA	
	New HDSP-F211 New HDSP-F213	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal	High Efficiency Red	1200 µcd @ 5 mA	
	New HDSP-F111 New HDSP-F113	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal	AlGaAs Red	650 µcd @ 1 mA	
	New HDSP-F161 New HDSP-F163	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal	AlGaAs Red	15.0 mcd @ 20 mA	
	New HDSP-F511 New HDSP-F513	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal	Green	3500 µcd @ 10 mA	
 10.16 mm (0.40 in.) Dual-in-Line (Dual Digit) 0.51" H x 0.39" W x 0.25" D	New HDSP-G011 New HDSP-G013	Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	Red	1200 µcd @ 20 mA	
	New HDSP-G211 New HDSP-G213	Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	High Efficiency Red	1200 µcd @ 5 mA	
	New HDSP-G111 New HDSP-G113	Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	AlGaAs Red	650 µcd @ 1 mA	
	New HDSP-G161 New HDSP-G163	Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	AlGaAs Red	15.0 mcd @ 20 mA	
	New HDSP-G511 New HDSP-G513	Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	Green	3500 µcd @ 10 mA	

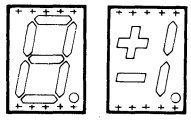
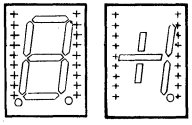
Black Surface Seven Segment Displays (cont.)

Device		P/N	Description	Color	Typical I_v	Page No.
 14.2 mm (0.56 in.) Dual-in-Line (Single Digit) 0.67" H x 0.49" W x 0.31" D	New	HDSP-H011	Common Anode Right Hand Decimal	Red	1300 µcd @ 20 mA	4-20
	New	HDSP-H013	Common Cathode Right Hand Decimal			
	New	HDSP-H211	Common Anode Right Hand Decimal	HER	2800 µcd @ 10 mA	
	New	HDSP-H213	Common Cathode Right Hand Decimal			
	New	HDSP-H111	Common Anode Right Hand Decimal	AlGaAs Red	700 µcd @ 1 mA	
	New	HDSP-H113	Common Cathode Right Hand Decimal			
	New	HDSP-H161	Common Anode Right Hand Decimal	AlGaAs Red	16.0 mcd @ 20 mA	
	New	HDSP-H163	Common Cathode Right Hand Decimal			
	New	HDSP-H511	Common Anode Right Hand Decimal	Green	2500 µcd @ 10 mA	
	New	HDSP-H513	Common Cathode Right Hand Decimal			
 14.2 mm (0.56 in.) Dual-in-Line (Dual Digit) 0.67" H x 1.0" W x 0.31" D	New	HDSP-K011	Two Digit Common Anode Right Hand Decimal	Red	1300 µcd @ 20 mA	
	New	HDSP-K013	Two Digit Common Cathode Right Hand Decimal			
	New	HDSP-K211	Two Digit Common Anode Right Hand Decimal	HER	2800 µcd @ 10 mA	
	New	HDSP-K213	Two Digit Common Cathode Right Hand Decimal			
	New	HDSP-K111	Two Digit Common Anode Right Hand Decimal	AlGaAs Red	700 µcd @ 10 mA	
	New	HDSP-K113	Two Digit Common Cathode Right Hand Decimal			
	New	HDSP-K511	Two Digit Common Anode Right Hand Decimal	Green	2500 µcd @ 10 mA	
	New	HDSP-K513	Two Digit Common Cathode Right Hand Decimal			

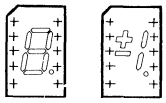
Low Current Seven Segment Displays

Device	P/N	Description	Color	Typical I_v	Page No.
 7.62 mm (0.30 in.) Mini Dual-in-Line 0.5" H x 0.3" W x 0.24" D	HDSP-A101 HDSP-A103 HDSP-A107 HDSP-A108	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	AlGaAs Red	600 µcd @ 1 mA	4-30
	HDSP-7511 HDSP-7513 HDSP-7517 HDSP-7518	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	High Efficiency Red	270 µcd @ 2 mA	
	HDSP-A801 HDSP-A803 HDSP-A807 HDSP-A808	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	Yellow	420 µcd @ 4 mA	
	HDSP-A901 HDSP-A903 HDSP-A907 HDSP-A908	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	Green	475 µcd @ 4 mA	
 10.16 mm (0.40 in.) Dual-in-Line (Single Digit) 0.51" H x 0.39" W x 0.25" D	HDSP-F101 HDSP-F103 HDSP-F107 HDSP-F108 HDSP-G101 HDSP-G103	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	AlGaAs Red	650 µcd @ 1 mA	
 10.92 mm (0.43 in.) Dual-in-Line 0.75" H x 0.5" W x 0.25" D	HDSP-E100 HDSP-E101 HDSP-E103 HDSP-E108	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow	AlGaAs Red	650 µcd @ 1 mA	
	HDSP-3350 HDSP-3351 HDSP-3353 HDSP-3356	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	High Efficiency Red	300 µcd @ 2 mA	

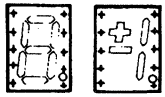
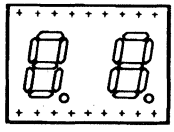
Low Current Seven Segment Displays (cont.)

Device	P/N	Description	Color	Typical I_v	Page No.
 14.2 mm (0.56 in.) Dual-in-Line (Single Digit) 0.67" H x 0.49" W x 0.31" D	HDSP-H101 HDSP-H103 HDSP-H107 HDSP-H108 HDSP-K121 HDSP-K123	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	AlGaAs Red	700 µcd @ 1 mA	4-30
	HDSP-5551 HDSP-5553 HDSP-5557 HDSP-5558 HDSP-K701 HDSP-K703	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	High Efficiency Red	370 µcd @ 2 mA	
 20 mm (0.8 in.) Dual-in-Line 1.09" H x 0.78" W x 0.33" D	HDSP-N100 HDSP-N101 HDSP-N103 HDSP-N105 HDSP-N106	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Cathode Left Hand Decimal Universal ±1. Overflow	AlGaAs Red	590 µcd @ 1 mA	

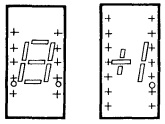
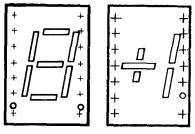
Seven Segment Displays

Device	P/N	Description	Color	Typical I_v	Page No.
	HDSP-7301 HDSP-7302 HDSP-7303 HDSP-7304 HDSP-7307 HDSP-7308	Common Anode Right Hand Decimal Common Anode Right Hand Decimal, Colon Common Cathode Right Hand Decimal Common Cathode Right Hand Decimal, Colon Common Anode ±1. Overflow Common Cathode ±1. Overflow	Red	1100 µcd @ 20 mA	4-53
	HDSP-A151 HDSP-A153 HDSP-A157 HDSP-A158	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	AlGaAs Red	14 mcd @ 20 mA	
	HDSP-7501 HDSP-7502 HDSP-7503 HDSP-7504 HDSP-7507 HDSP-7508	Common Anode Right Hand Decimal Common Anode Right Hand Decimal, Colon Common Cathode Right Hand Decimal Common Cathode Right Hand Decimal, Colon Common Anode ±1. Overflow Common Cathode ±1. Overflow	High Efficiency Red	980 µcd @ 5 mA	
	HDSP-7401 HDSP-7402 HDSP-7403 HDSP-7404 HDSP-7407 HDSP-7408	Common Anode Right Hand Decimal Common Anode Right Hand Decimal, Colon Common Cathode Right Hand Decimal Common Cathode Right Hand Decimal, Colon Common Anode ±1. Overflow Common Cathode ±1. Overflow	Yellow	480 µcd @ 5 mA	
7.62 mm (0.3 in.) Microbright Dual-in-Line 0.5" H x 0.3" W x 0.24" D	HDSP-7801 HDSP-7802 HDSP-7803 HDSP-7804 HDSP-7807 HDSP-7808	Common Anode Right Hand Decimal Common Anode Right Hand Decimal, Colon Common Cathode Right Hand Decimal Common Cathode Right Hand Decimal, Colon Common Anode ±1. Overflow Common Cathode ±1. Overflow	Green	3000 µcd @ 10 mA	

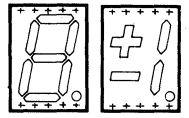
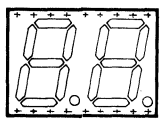
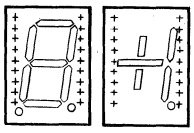
Seven Segment Displays (cont.)

Device	P/N	Description	Color	Typical I_v	Page No.
	HDSP-F001 HDSP-F003 HDSP-F007 HDSP-F008 HDSP-G001 HDSP-G003	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	Red	1200 µcd @ 20 mA	4-70
	HDSP-F151 HDSP-F153 HDSP-F157 HDSP-F158 HDSP-G151 HDSP-G153	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	AlGaAs Red	15.0 mcd @ 20 mA	
	HDSP-F201 HDSP-F203 HDSP-F207 HDSP-F208 HDSP-G201 HDSP-G203	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	High Efficiency Red	1200 µcd @ 5 mA	
10.16 mm (0.4 in.) Dual-In-Line (Single Digit) 0.51" H x 0.39" W x 0.25" D	HDSP-F401 HDSP-F403 HDSP-F407 HDSP-F408 HDSP-G401 HDSP-G403	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	Orange	1200 µcd @ 5 mA	
	HDSP-F301 HDSP-F303 HDSP-F307 HDSP-F308 HDSP-G301 HDSP-G303	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two DigitCommon Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	Yellow	800 µcd @ 5 mA	
10.16 mm (0.4 in.) Dual-In-Line (Two Digit) 0.67" H x 0.90" W x 0.25" D	HDSP-F501 HDSP-F503 HDSP-F507 HDSP-F508 HDSP-G501 HDSP-G503	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two DigitCommon Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	Green	3500 µcd @ 10 mA	

Seven Segment Displays (cont.)

Device	P/N	Description	Color	Typical I_v	Page No.
	5082-7730 5082-7731 5082-7740 5082-7736	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	Red	770 µcd @ 20 mA	4-61
	5082-7610 5082-7611 5082-7613 5082-7616	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	High Efficiency Red	800 µcd @ 5 mA	
	5082-7620 5082-7621 5082-7623 5082-7626	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	Yellow	620 µcd @ 5 mA	
7.62 mm (0.3 in.) Dual-in-Line 0.75" H x 0.4" W x 0.18" D	HDSP-3600 HDSP-3601 HDSP-3603 HDSP-3606	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	Green	2700 µcd @ 10 mA	
	5082-7750 5082-7751 5082-7760 5082-7756	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	Red	1100 µcd @ 20 mA	
	HDSP-E150 HDSP-E151 HDSP-E153 HDSP-E156	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	AlGaAs Red	15.0 mcd @ 20 mA	
	5082-7650 5082-7651 5082-7653 5082-7656	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	High Efficiency Red	1115 µcd @ 5 mA	
	5082-7660 5082-7661 5082-7663 5082-7666	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	Yellow	835 µcd @ 5 mA	
10.92 mm (0.43 in.) Dual-in-Line 0.75" H x 0.5" W x 0.25" D	HDSP-4600 HDSP-4601 HDSP-4603 HDSP-4606	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	Green	4000 µcd @ 10 mA	

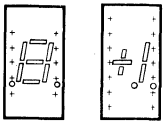
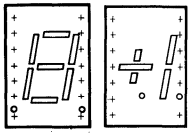
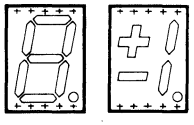
Seven Segment Displays (cont.)

Device	P/N	Description	Color	Typical I_v	Page No.
 14.2 mm (0.56 in.) Dual-in-Line (Single Digit) 0.67" H x 0.49" W x 0.31" D	HDSP-5301 HDSP-5303 HDSP-5307 HDSP-5308 HDSP-5321 HDSP-5323	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	Red	1300 µcd @ 20 mA	4-80
	HDSP-H151 HDSP-H153 HDSP-H157 HDSP-H158 HDSP-K121 HDSP-K123	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	AlGaAs Red	16.0 mcd @ 20 mA	
	HDSP-5501 HDSP-5503 HDSP-5507 HDSP-5508 HDSP-5521 HDSP-5523	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	High Efficiency Red	2800 µcd @ 10 mA	
 14.2 mm (0.56 in.) Dual-in-Line (Two Digit) 0.67" H x 1.0" W x 0.31" D	HDSP-5701 HDSP-5703 HDSP-5707 HDSP-5708 HDSP-5721 HDSP-5723	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	Yellow	1800 µcd @ 10 mA	
	HDSP-5601 HDSP-5603 HDSP-5607 HDSP-5608 HDSP-5621 HDSP-5623	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	Green	2500 µcd @ 10 mA	
 20 mm (0.8 in.) Dual-in-Line 1.09" H x 0.78" W x 0.33" D	HDSP-3400 HDSP-3401 HDSP-3403 HDSP-3405 HDSP-3406	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Cathode Left Hand Decimal Universal ±1. Overflow Right Hand Decimal	Red	1200 µcd @ 20 mA	4-89
	HDSP-N150 HDSP-N151 HDSP-N153 HDSP-N155 HDSP-N156	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Cathode Left Hand Decimal Universal ±1. Overflow Right Hand Decimal	AlGaAs Red	14.0 mcd @ 20 mA	
	HDSP-3900 HDSP-3901 HDSP-3903 HDSP-3905 HDSP-3906	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Cathode Left Hand Decimal Universal ±1. Overflow Right Hand Decimal	High Efficiency Red	7000 µcd @ 100 mA peak 1/5 Duty Factor	
	HDSP-4200 HDSP-4201 HDSP-4203 HDSP-4205 HDSP-4206	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Cathode Left Hand Decimal Universal ±1. Overflow Right Hand Decimal	Yellow	7000 µcd @ 100 mA peak 1/5 Duty Factor	

Seven Segment Displays (cont.)

Device	P/N	Description	Color	Typical I_v	Page No.
(See previous page)	HDSP-8600 HDSP-8601 HDSP-8603 HDSP-8605 HDSP-8606	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Cathode Left Hand Decimal Universal ±1. Overflow Right Hand Decimal	Green	1500 µcd @ 10 mA	4-89

High Ambient Light, Seven Segment Displays

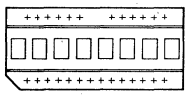
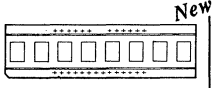
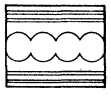
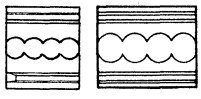
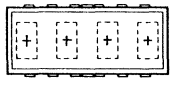
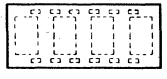
Device	P/N	Description	Typical I_v @ 100 mA Peak 1/5 Duty Factor	Page No.
 7.62 mm (0.3 in.) Dual-in-Line 0.75" H x 0.4" W x 0.18" D	HDSP-3530 HDSP-3531 HDSP-3533 HDSP-3536	High Efficiency Red, Common Anode, LHDP High Efficiency Red, Common Anode, RHDP High Efficiency Red, Common Cathode, RHDP High Efficiency Red, Universal Polarity Overflow Indicator, RHDP	7100 µcd/seg	*
	HDSP-4030 HDSP-4031 HDSP-4033 HDSP-4036	Yellow, Common Anode, LHDP Yellow, Common Anode, RHDP Yellow, Common Cathode, RHDP Yellow, Universal Polarity Overflow Indicator, RHDP	4500 µcd/seg	
 10.92 mm (0.43 in.) Dual-in-Line 0.75" H x 0.5" W x 0.25" D	HDSP-3730 HDSP-3731 HDSP-3733 HDSP-3736	High Efficiency Red, Common Anode, LHDP High Efficiency Red, Common Anode, RHDP High Efficiency Red, Common Cathode, RHDP High Efficiency Red, Universal Polarity Overflow Indicator, RHDP	10900 µcd/seg	
	HDSP-4130 HDSP-4131 HDSP-4133 HDSP-4136	Yellow, Common Anode, LHDP Yellow, Common Anode, RHDP Yellow, Common Cathode, RHDP Yellow, Universal Polarity Overflow Indicator, RHDP	5000 µcd/seg	
 14.2 mm (0.56 in.) Dual-in-Line 0.67" H x 0.49" W x 0.31" D	HDSP-5531 HDSP-5533 HDSP-5537 HDSP-5538	High Efficiency Red, Common Anode, RHDP High Efficiency Red, Common Cathode, RHDP High Efficiency Red ±1. Common Anode High Efficiency Red ±1. Common Cathode	6000 µcd/seg	
	HDSP-5731 HDSP-5733 HDSP-5737 HDSP-5738	Yellow, Common Anode, RHDP Yellow, Common Cathode, RHDP Yellow, ±1. Common Anode Yellow, ±1. Common Cathode	5500 µcd/seg	

Solid State Display Intensity and Color Selections

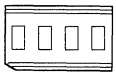
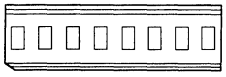
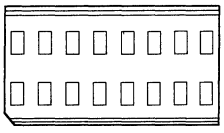
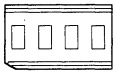
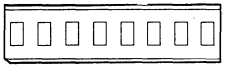
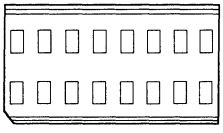
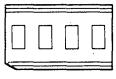
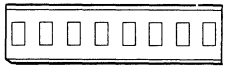
Option	Description	Page No.
Option S01 Option S02 Option S20	Intensity and Color Selected Displays	*

*Contact your local Hewlett-Packard sales representative for information regarding this product. (See section 9.)

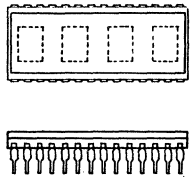
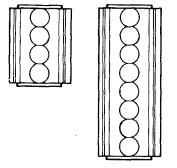
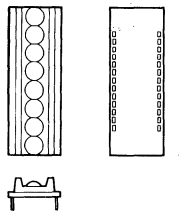
Alphanumeric LED Displays

Device	P/N	Description	Color	Application	Page No.
	HDSP-2110 HDSP-2111 HDSP-2112 HDSP-2113 HDSP-2107 HDSP-2121 HDSP-2122 HDSP-2123	5.0 mm (0.2 in.) 5 x 7 Eight Character Intelligent Display Operating Temperature Range: 45°C to +85°C HDSP-211X ASCII HDSP-212X Katakana	Orange Yellow High Efficiency Red Green AlGaAs Red Yellow High Efficiency Red Green	• Medical • Telecommunications • Analytical Equipment • Computer Products • Office Equipment • Industrial Equipment	4-135
	New HDSP-2500 New HDSP-2501 New HDSP-2502 New HDSP-2503	15.24 mm (0.6 in.) 28 pin DIP, ASCII 5 x 7 Eight Character Intelligent Display Operating Temperature Range: 45°C to +85°C	Orange Yellow High Efficiency Red Green	• Computer Peripherals • Industrial Instrumentation • Medical Equipment • Portable Data Entry Devices • Cellular Phones • Telecommunications • Test Equipment	
	New HDSP-2530 New HDSP-2531 New HDSP-2532 New HDSP-2533 New HDSP-2534	5.0 mm (0.2 in.) Eight Character Intelligent Display Operating Temperature Range: -40°C to +85°C	Orange Yellow High Efficiency Red Green AlGaAs Red	• Avionics • Computer Peripherals • Industrial Instrumentation • Medical Equipment • Portable Data Entry Devices • Telecommunications • Test Equipment	4-151
	HDLA-2416 HDLG-2416 HDLO-2416 HDLR-2416 New HDLS-2416 New HDLU-2416 HDLY-2416	5.0 mm (0.2 in.) 5 x 7 Four Character Intelligent Display Operating Temperature Range: -40°C to +85°C	Orange Green High Efficiency Red Red AlGaAs Red (SV) AlGaAs Red (LP) Yellow	• Portable Data Entry Devices • Industrial Instrumentation • Computer Peripherals • Telecommunications	4-123
	HPDL-1414 HPDL-2416	2.85 mm (0.112 in.) 4.1 mm (0.16 in.) 16-Segment Four Character Monolithic Intelligent Display Operating Temperature Range: -40°C to +85°C	Red Red	• Portable Data Entry Devices • Medical Equipment • Industrial Instrumentation • Computer Peripherals • Telecommunications	4-166
	HCMS-2000 HCMS-2001 HCMS-2002 HCMS-2003 HCMS-2004	3.8 mm (0.15 in.) 5 x 7 Four Character Display 12 pin Ceramic DIP 7.6 mm (0.30 in.) Operating Temperature Range: -40°C to +85°C	Red Yellow High Efficiency Red Green Orange	• Computer Terminals • Business Machines • Portable, Hand-held or Mobile Data Entry, Read-out, or Communications	4-178
	HCMS-2300 HCMS-2301 HCMS-2302 HCMS-2303 HCMS-2304	5.0 mm (0.20 in.) 5 x 7 Four Character Display 12 pin Ceramic DIP 6.35 mm (0.250 in.) Operating Temperature Range: -40°C to +85°C	Red Yellow High Efficiency Red Green Orange	• Avionics • Ground Support, Cockpit, Shipboard Systems • Medical Equipment • Industrial and Process Control • Computer Peripherals and Terminals	

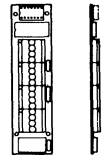
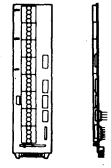
Alphanumeric LED Displays (Continued)

Device		P/N	Description	Color	Application	Page No.
	New	HCMS-2700	1 Row of 4 Characters	Standard Red	• Telecommunications	4-97
	New	HCMS-2701	3.8 mm (0.15 in.) 5 x 7 Dot	Yellow	• Instrumentation	
	New	HCMS-2702	Matrix, Full ASCII	HER	• Medical Instrumentation	
	New	HCMS-2703	Character Set	Green	• Business Machines	
	New	HCMS-2704		Orange		
	New	HCMS-2710	1 Row of 8 Characters	Standard Red		
	New	HCMS-2711		Yellow		
	New	HCMS-2712		HER		
	New	HCMS-2713		Green		
	New	HCMS-2714		Orange		
	New	HCMS-2720	2 Rows of 8 Characters	Standard Red		
	New	HCMS-2721		Yellow		
	New	HCMS-2722		HER		
	New	HCMS-2723		Green		
	New	HCMS-2724		Orange		
	New	HCMS-2901	1 Row of 4 Characters	Yellow	• Telecommunications	4-107
	New	HCMS-2902	3.8 mm (0.15 in.) 5 x 7 Dot	HER	• Portable Data Entry Devices	
	New	HCMS-2903	Matrix Fully Integrated	Green	• Computer Peripherals	
	New	HCMS-2904	Serial-in Display	Orange	• Medical Equipment	
	New	HCMS-2905		AlGaAs	• Test Equipment	
	New	HCMS-2911	1 Row of 4 Characters	Yellow	• Business Machines	
	New	HCMS-2912	3.8 mm (0.15 in.)	HER	• Avionics	
	New	HCMS-2913		Green	• Industrial Controls	
	New	HCMS-2914		Orange		
	New	HCMS-2915		AlGaAs		
	New	HCMS-2921	2 Rows of 8 Characters	Yellow		
	New	HCMS-2922	3.8 mm (0.15 in.)	HER		
	New	HCMS-2923		Green		
	New	HCMS-2924		Orange		
	New	HCMS-2925		AlGaAs		
	New	HCMS-2961	1 Row of 4 Characters	Yellow		
	New	HCMS-2962	5.0 mm (0.20 in.)	HER		
	New	HCMS-2963		Green		
	New	HCMS-2964		Orange		
	New	HCMS-2965		AlGaAs		
	New	HCMS-2971	1 Row of 8 Characters	Yellow		
	New	HCMS-2972	5.0 mm (0.20 in.)	HER		
	New	HCMS-2973		Green		
	New	HCMS-2974		Orange		
	New	HCMS-2975		AlGaAs		

Alphanumeric LED Displays (Continued)

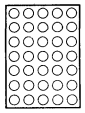
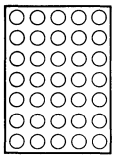
Device	P/N	Description	Color	Application	Page No.
	HDSP-2490 HDSP-2491 HDSP-2492 HDSP-2493	6.9 mm (0.27 in.) 5 x 7 Four Character Alphanumeric 28 Pin Ceramic 15.24 mm (0.6 in.) DIP with untinted glass lens Operating Temperature Range: -20°C to +85°C	Red Yellow High Efficiency Red High Performance Green	• High Brightness Ambient Systems • Industrial and Process Control • Computer Peripherals • Ground Support Systems For further information see Application Note 1016.	*
	HDSP-6504	3.8 mm (0.15 in.) Sixteen Segment Four Character Alphanumeric 22 Pin 15.2 mm (0.6 in.) DIP	Red	• Computer Terminals • Hand Held Instruments • In-Plant Control Equipment • Diagnostic Equipment	
	HDSP-6508	3.8 mm (0.15 in.) Sixteen Segment Eight Character Alphanumeric 26 Pin 15.2 mm (0.6 in.) DIP			
	HDSP-6300	3.56 mm (0.14 in.) Sixteen Segment Eight Character Alphanumeric 26 Pin 15.2 mm (0.6 in.) DIP		• Computer Peripherals and Terminals • Computer Base Emergency Mobile Units • Automotive Instrument Panels • Desk Top Calculators • Hand-Held Instruments For further information ask for Application Note 931.	

Alphanumeric Display Systems

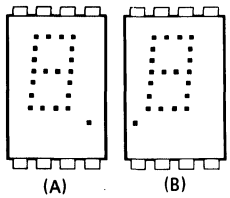
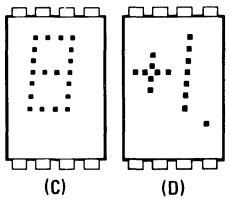
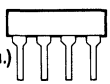
Device	P/N	Description	Color	Application	Page No.
	HDSP-6621	Single Line 16 Character Display Board Utilizing the HPDL-1414	114.30 mm (4.50 in.) L x 30.48 mm (1.20 in.) H x 8.12 mm (0.32 in.) D	• Computer Peripherals • Telecommunications • Industrial Equipment • Instruments	*
	HDSP-6624	Single Line 32 Character Display Board Utilizing the HPDL-2416	223.52 mm (8.80 in.) L x 58.42 mm (2.30 in.) H x 15.92 mm (0.62 in.) D		

*Contact your local Hewlett-Packard sales representative for information regarding this product. (See section 9.)

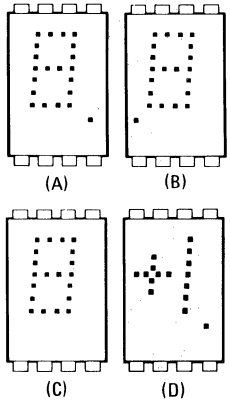
Large Alphanumeric 5 X 7 Displays

Device	P/N	Description	Color	Package	Typical I_v	Page No.
	HDSP-4701 HDSP-4703 HDSP-L101 HDSP-L103 HDSP-L201 HDSP-5401 HDSP-5403	Common Row Anode Common Row Cathode Common Row Anode Common Row Cathode Common Row Anode Common Row Anode Common Row Cathode	Red Red AlGaAs Red AlGaAs Red High Efficiency Red Green Green	17.3 mm (0.68 in.) Dual-in-Line 0.70 in. H x 0.50 in. W x 0.26 in. D	770 µcd/dot 100 mA peak 1/5 Duty Factor 1650 µcd/dot 10 mA peak 1/5 Duty Factor 2800 µcd/dot 50 mA peak 1/5 Duty Factor 4000 µcd/dot 50 mA peak 1/5 Duty Factor	4-186
	HDSP-4401 HDSP-4403 HDSP-M101 HDSP-M103 HDSP-4501 HDSP-4503 HDSP-5101 HDSP-5103	Common Row Anode Common Row Cathode Common Row Anode Common Row Cathode Common Row Anode Common Row Cathode Common Row Anode Common Row Cathode	Red Red AlGaAs Red AlGaAs Red High Efficiency Red High Efficiency Red Green Green	26.5 mm (1.04 in.) Dual-in-Line 1.10 in. H x 0.79 in. W x 0.25 in. D	800 µcd/dot 100 mA peak 1/5 Duty Factor 1850 µcd/dot 10 mA peak 1/5 Duty Factor 3500 µcd/dot 50 mA peak 1/5 Duty Factor 4500 µcd/dot 50 mA peak 1/5 Duty Factor	

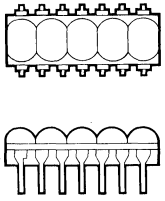
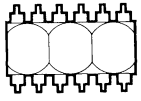
Hexadecimal and Dot Matrix Displays

Device	P/N	Description	Package	Application	Page No.
 (A) (B)	5082-7300 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	8 Pin Epoxy 15.2 mm (0.6 in.) DIP	General Purpose Market • Test Equipment • Business Machines • Computer Peripherals • Avionics	4-193
	5082-7302 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	5082-7340 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	5082-7304 (D)	Over Range ±1			
 (C) (D)	5082-7356 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	8 Pin Glass Ceramic 15.2 mm (0.6 in.) DIP	• Medical Equipment • Industrial and Process Control Equipment • Computers • Where Ceramic Package ICs are required • High Reliability Applications	4-197
	5082-7357 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	5082-7359 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
 7.4 mm (0.29 in.) 4 x 7 Single Digit	5082-7358 (D)	Over Range ±1			

Hexadecimal and Dot Matrix Displays (Cont.)

Device	P/N	Description	Package	Application	Page No.
	HDSP-0760 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	High Efficiency Red Low Power	• Military Equipment • Ground Support Equipment • Avionics • High Reliability Applications	4-202
	HDSP-0761 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	HDSP-0762 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	HDSP-0763 (D)	Over Range ±1			
	HDSP-0770 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	High Efficiency Red High Brightness	• High Brightness Ambient Systems • Cockpit, Shipboard Equipment • High Reliability Applications	
	HDSP-0771 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	HDSP-0772 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	HDSP-0773 (D)	Over Range ±1			
7.4 mm (0.29 in.) 4 x 7 Single Digit Package: 8 Pin Glass Ceramic 15.2 mm (0.6 in.) DIP	HDSP-0860 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	Yellow	• Business Machines • Fire Control Systems • Military Equipment • High Reliability Applications	
	HDSP-0861 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	HDSP-0862 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	HDSP-0863 (D)	Over Range ±1			
	HDSP-0960 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	High Performance Green	• Business Machines • Fire Control Systems • Military Equipment • High Reliability Applications	
	HDSP-0961 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	HDSP-0962 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	HDSP-0963 (D)	Over Range ±1			

Monolithic Numeric Displays

Device	P/N	Description	Package	Application	Publ. No.
	5082-7404	2.79 mm (0.11 in.) Red, 4 Digits, Centered D.P.	12 Pin Epoxy, 7.62 mm (0.3 in.) DIP	Small Display Market • Portable/Battery Power Instruments • Portable Calculators • Digital Counters • Digital Thermometers • Digital Micrometers • Stopwatches • Cameras • Copiers • Digital Telephone Peripherals • Data Entry Terminals • Taxi Meters For further information ask for Application Note 937.	*
	5082-7405	2.79 mm (0.11 in.) Red, 5 Digits, Centered D.P.	14 Pin Epoxy, 7.62 mm (0.3 in.) DIP		
	5082-7414	2.79 mm (0.11 in.) Red, 4 Digits, RHDP	12 Pin Epoxy, 7.62 mm (0.3 in.) DIP		
	5082-7415	2.79 mm (0.11 in.) Red, 5 Digits, RHDP	14 Pin Epoxy, 7.62 mm (0.3 in.) DIP		
	5082-7432	2.79 mm (0.11 in.) Red, 2 Digits, Right, RHDP	12 Pin Epoxy, 7.62 mm (0.3 in.) DIP		
	5082-7433	2.79 mm (0.11 in.) Red, 3 Digits, RHDP			

*Contact your local Hewlett-Packard sales representative for information regarding this product. (See section 9.)

HEWLETT PACKARD

New

Black Surface Seven Segment Displays

Technical Data

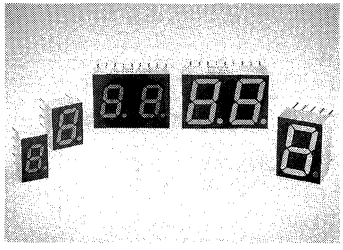
HDSP-AX11/-AX13 Series
HDSP-FX11/-FX13 Series
HDSP-GX11/-GX13 Series
HDSP-HX11/-HX13 Series
HDSP-KX11/-KX13 Series

Features

- **Black Surface and Color Tinted Epoxy**
- **Industry Standard Size**
- **Industry Standard Pinout**
- **Choice of Character Size**
  7.6 mm (0.30 in.), 10 mm (0.40 in.), 14.2 mm (0.56 in.)
- **Choice of Colors**
  Red, AlGaAs Red, High Efficiency Red (HER), Green
- **Excellent Appearance**
  Evenly Lighted Segments
  ±50° Viewing Angle
- **Design Flexibility**
  Common Anode or Common Cathode
  Single and Two Digit
- **Categorized for Luminous Intensity**
  Categorized for Color: Green
  Use of Like Categories Yields a Uniform Display
- **Excellent for Long Digit String Multiplexing**

Description

These devices use industry standard size package and pinout. Available with black surface finish. All devices are available as either common anode or common cathode.

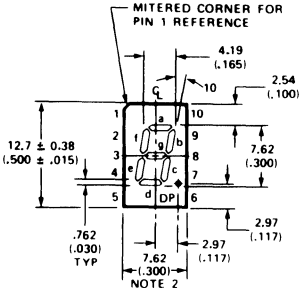


Typical applications include appliances, channel indicators of TV, CATV converters, game machines, and point of sale terminals.

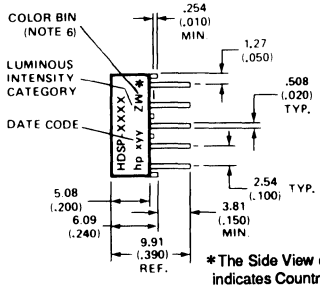
Devices

Red HDSP-	AlGaAs Red HDSP-	HER HDSP-	Green HDSP-	Description	Package Drawing
A011	A111	A211	A511	7.6 mm Common Anode Right Hand Decimal	A
A013	A113	A213	A513	7.6 mm Common Cathode Right Hand Decimal	B
F011	F111	F211	F511	10 mm Common Anode Right Hand Decimal	C
F013	F113	F213	F513	10 mm Common Cathode Right Hand Decimal	D
G011	G111	G211	G511	10 mm Two Digit Common Anode Right Hand Decimal	E
G013	G113	G213	G513	10 mm Two Digit Common Cathode Right Hand Decimal	F
H011	H111	H211	H511	14.2 mm Common Anode Right Hand Decimal	G
H013	H113	H213	H513	14.2 mm Common Cathode Right Hand Decimal	H
K011	K111	K211	K511	14.2 mm Two Digit Common Anode Right Hand Decimal	I
K013	K113	K213	K513	14.2 mm Two Digit Common Cathode Right Hand Decimal	J

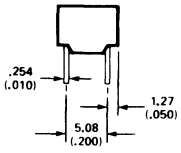
Package Dimensions (7.6 mm Series)



A, B



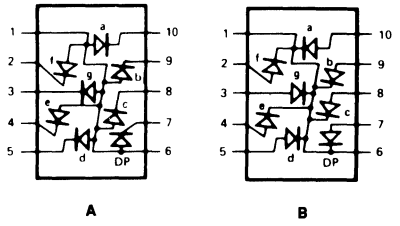
*The Side View of package indicates Country of Origin.



A, B

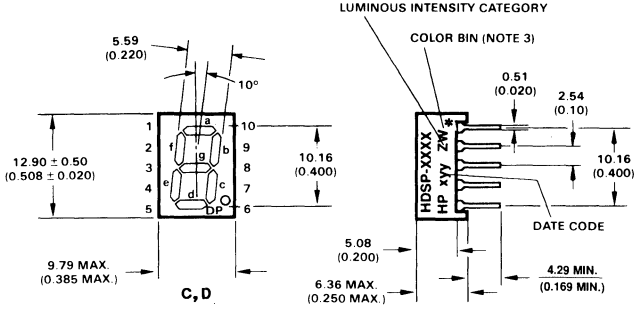
PIN	FUNCTION	
	A	B
1	ANODE[4]	CATHODE[5]
2	CATHODE f	ANODE f
3	CATHODE g	ANODE g
4	CATHODE e	ANODE e
5	CATHODE d	ANODE d
6	ANODE[4]	CATHODE[5]
7	CATHODE DP	ANODE DP
8	CATHODE c	ANODE c
9	CATHODE b	ANODE b
10	CATHODE a	ANODE a

Internal Circuit Diagram



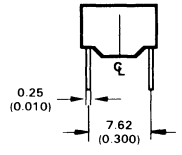
NOTES:
1. ALL DIMENSIONS IN MILLIMETERS (INCHES).
2. MAXIMUM.
3. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
4. REDUNDANT ANODES.
5. REDUNDANT CATHODES.
6. FOR HDSP-A511/-A513 ONLY.

Package Dimensions (10 mm Series: Single)



C, D

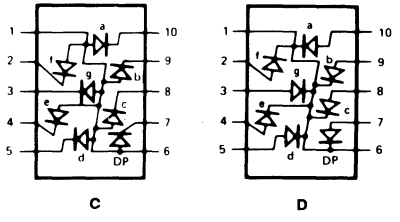
*The Side View of package indicates Country of Origin.



C, D

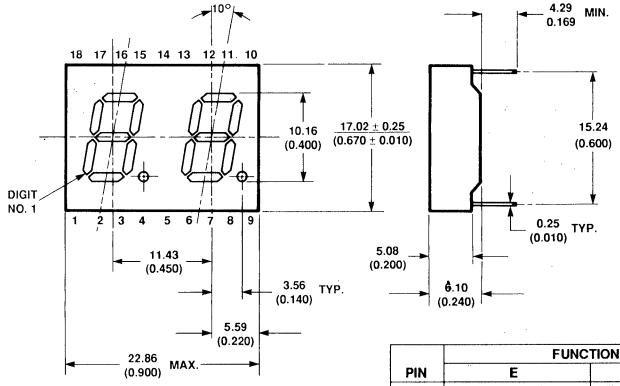
PIN	FUNCTION	
	C	D
1	ANODE[4]	CATHODE[5]
2	CATHODE f	ANODE f
3	CATHODE g	ANODE g
4	CATHODE e	ANODE e
5	CATHODE d	ANODE d
6	ANODE[4]	CATHODE[5]
7	CATHODE DP	ANODE DP
8	CATHODE c	ANODE c
9	CATHODE b	ANODE b
10	CATHODE a	ANODE a

Internal Circuit Diagram

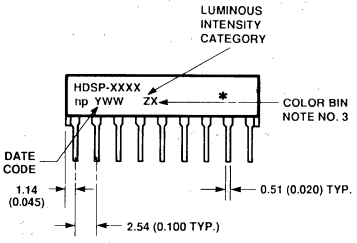


NOTES:
1. ALL DIMENSIONS IN MILLIMETERS (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. FOR HDSP-F511/-F513 ONLY.
4. REDUNDANT ANODES.
5. REDUNDANT CATHODES.

Package Dimensions (10 mm Series: Two Digit)



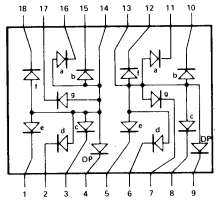
E, F



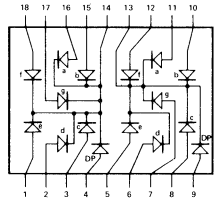
E, F

* The Side View of package indicates Country of Origin.

Internal Circuit Diagram



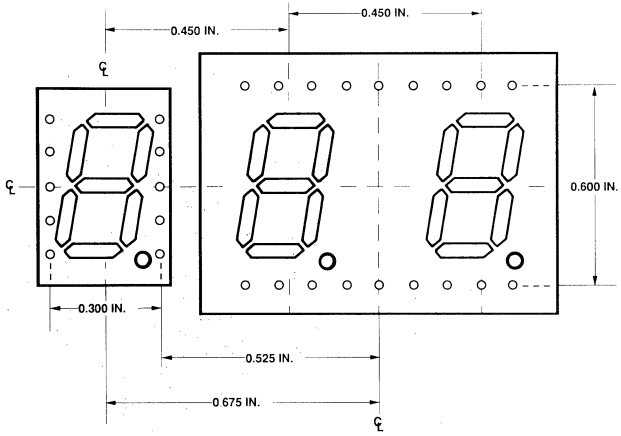
E



F

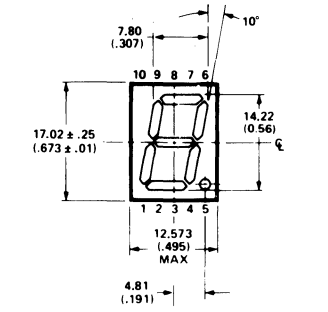
PIN	FUNCTION	
	E	F
1	E CATHODE NO 1	E ANODE NO. 1
2	D CATHODE NO. 1	D ANODE NO. 1
3	C CATHODE NO. 1	C ANODE NO. 1
4	DP CATHODE NO. 1	DP ANODE NO. 1
5	E CATHODE NO. 2	E ANODE NO. 2
6	D CATHODE NO. 2	D ANODE NO. 2
7	G CATHODE NO. 2	G ANODE NO. 2
8	C CATHODE NO. 2	C ANODE NO. 2
9	CP CATHODE NO. 2	DP ANODE NO. 2
10	B CATHODE NO. 2	B ANODE NO. 2
11	A CATHODE NO. 2	A ANODE NO. 2
12	F CATHODE NO. 2	F ANODE NO. 2
13	DIGIT NO. 2 ANODE	DIGIT NO. 2 CATHODE
14	DIGIT NO. 1 ANODE	DIGIT NO. 1 CATHODE
15	B CATHODE NO. 1	B ANODE NO. 1
16	A CATHODE NO. 2	A ANODE NO. 1
17	G CATHODE NO. 1	G ANODE NO. 1
18	F CATHODE NO. 1	F ANODE NO. 1

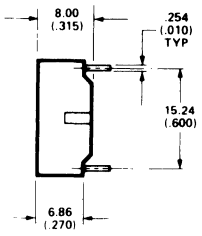
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. FOR HDSP-G511/-G513 ONLY.

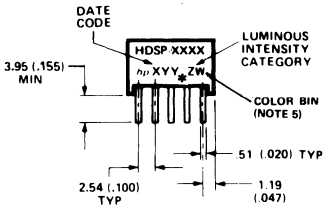


HOLE PATTERN FOR PCB LAYOUT TO ACHIEVE UNIFORM 0.450 DIGIT TO DIGIT PITCH. FOR HDSP-FXXX TO HDSP-GXXX.

Package Dimensions (14.2 mm Series: Single)







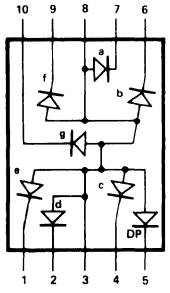
G, H

*The End View of package indicates Country of Origin.

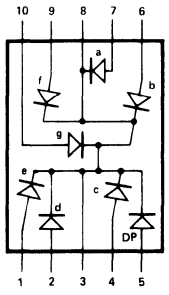
PIN	FUNCTION	
	G	H
1	CATHODE e	ANODE e
2	CATHODE d	ANODE d
3	ANODE[3]	CATHODE[4]
4	CATHODE c	ANODE c
5	CATHODE DP	ANODE DP
6	CATHODE b	ANODE b
7	CATHODE a	ANODE a
8	ANODE[3]	CATHODE[4]
9	CATHODE f	ANODE f
10	CATHODE g	ANODE g

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. REDUNDANT ANODES.
4. REDUNDANT CATHODES.
5. FOR HDSP-H511/-H513 ONLY.

Internal Circuit Diagram

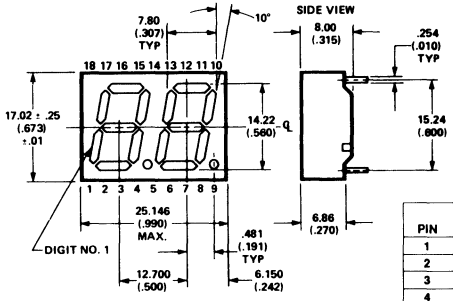


G

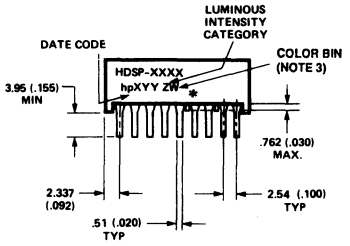


H

Package Dimensions (14.2 mm Series: Two Digit)



I, J



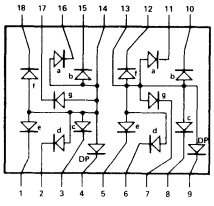
I, J

*The Side View of package indicates Country of Origin.

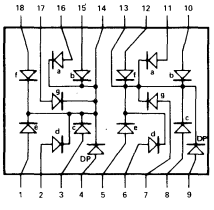
PIN	FUNCTION	
	I	J
1	E CATHODE NO 1	E ANODE NO. 1
2	D CATHODE NO. 1	D ANODE NO. 1
3	C CATHODE NO. 1	C ANODE NO. 1
4	DP CATHODE NO. 1	DP ANODE NO. 1
5	E CATHODE NO. 1	E ANODE NO. 2
6	D CATHODE NO. 2	D ANODE NO. 2
7	G CATHODE NO. 2	G ANODE NO. 2
8	C CATHODE NO. 2	C ANODE NO. 2
9	DP CATHODE NO. 2	DP ANODE NO. 2
10	B CATHODE NO. 2	B ANODE NO. 2
11	A CATHODE NO. 2	A ANODE NO. 2
12	F CATHODE NO. 2	F ANODE NO. 2
13	DIGIT NO. 2 ANODE	DIGIT NO. 2 CATHODE
14	DIGIT NO. 1 ANODE	DIGIT NO. 2 CATHODE
15	B CATHODE NO. 2	B ANODE NO. 1
16	A CATHODE NO. 1	A ANODE NO. 1
17	G CATHODE NO. 1	G ANODE NO. 1
18	F CATHODE NO. 1	F ANODE NO. 1

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. FOR HDSP-K511/-K513 ONLY.

Internal Circuit Diagram



I



J

Absolute Maximum Ratings

Description	Red HDSP-X01X Series	AlGaAs Red HDSP-X11X Series	HER HDSP-X21X Series	Green HDSP-X51X Series	Units
Average Power per Segment or DP	82	37	105	105	mW
Peak Forward Current per Segment or DP	150[1]	45[3]	90[4]	90[6]	mA
DC Forward Current per Segment or DP	25[2]	15[8]	30[5]	30[7]	mA
Operating Temperature Range	-40 to +100	-20 to +100	-40 to +100		°C
Storage Temperature Range	-55 to +100				°C
Reverse Voltage per Segment or DP	3.0				V
Lead Solder Temperature for 3 Seconds (1.60 mm [0.063 in.] below seating plane)	260				°C

Notes:
1. See Figure 1 to establish pulsed conditions.
2. Derate above 80°C at 0.63 mA/°C (see Figure 2).
3. See Figure 11 to establish pulsed conditions.
4. See Figure 10 to establish pulsed conditions.
5. Derate above 53°C at 0.45 mA/°C (see Figure 12).
6. See Figure 11 to establish pulsed conditions.
7. Derate above 39°C at 0.37 mA/°C (see Figure 12).
8. Derate above 91°C at 0.53 mA/°C (see Figure 6).

Electrical/Optical Characteristics at T_A = 25°C

Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A01X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	600	1100		µcd	I_F = 20 mA
				500			I_F = 10 mA
F01X, G01X			650	1200			I_F = 20 mA
H01X, K01X			600	1300			I_F = 20 mA
				1400			I_F = 100 mA Peak: 1/5 Duty Factor
All Devices	Forward Voltage/Segment or DP	V_F		1.6	2.0	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		655		nm	
	Dominant Wavelength[3]	λ_d		640		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	12		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
A01X	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W/ Seg.	
F01X, G01X				320			
H01X, K01X				345			

AlGaAs Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A11X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	315	600		µcd	I_F = 1 mA
				3600			I_F = 5 mA
F11X, G11X			330	650			I_F = 1 mA
				3900			I_F = 5 mA
H11X, K11X			400	700			I_F = 1 mA
				4200			I_F = 5 mA
All Devices	Forward Voltage/Segment or DP	V_F		1.6	2.0	V	I_F = 1 mA
				1.7			I_F = 5 mA
				1.8	22		I_F = 20 mA Peak
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
A11X	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		255		°C/W/ Seg.	
F11X, G11X				320			
H11X, K12X				400			

High Efficiency Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A21X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	360	980		µcd	I_F = 5 mA
				5390			I_F = 20 mA
F21X, G21X			420	1200			I_F = 5 mA
H21X, K21X			900	2800			I_F = 10 mA
				3700			I_F = 60 mA Peak: 1/6 Duty Factor
All Devices	Forward Voltage/Segment or DP	V_F		2.0	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
A21X	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W/ Seg.	
F21X, G21X				320			
H21X, K21X				345			

High Performance Green

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A51X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	860	3000		µcd	I_F = 10 mA
				6800			I_F = 20 mA
F51X, G51X			1030	3500			I_F = 10 mA
H51X, K51X			900	2500			I_F = 10 mA
				3100			I_F = 60 mA Peak: 1/6 Duty Factor
All Devices	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 10 mA
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,5]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
A51X	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W/ Seg.	
F51X, G51X				320			
H51X, G51X				345			

Notes:

1. Case temperature of device immediately prior to the intensity measurement is 25°C.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. Green (HDSP-A51X/F51X/G51X/H512X/K51X) series displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

Red

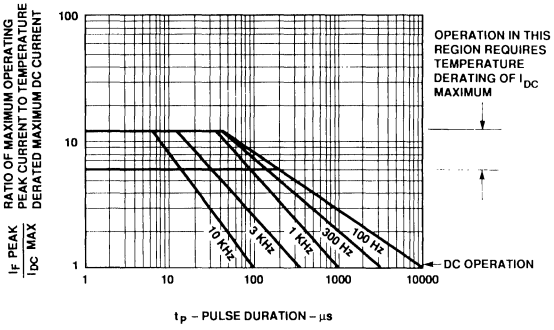


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration – Red.

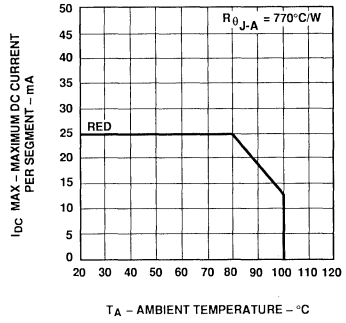


Figure 2. Maximum Allowable DC Current vs. Ambient Temperature.

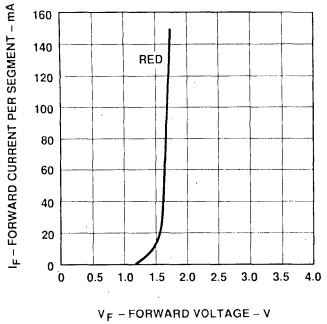


Figure 3. Forward Current vs. Forward Voltage.

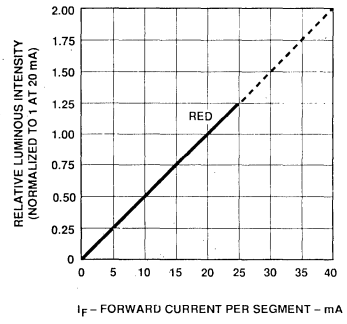


Figure 4. Relative Luminous Intensity vs. DC Forward Current.

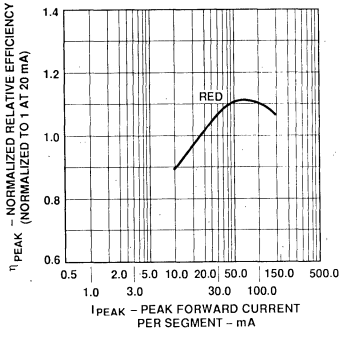


Figure 5. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

AlGaAs Red

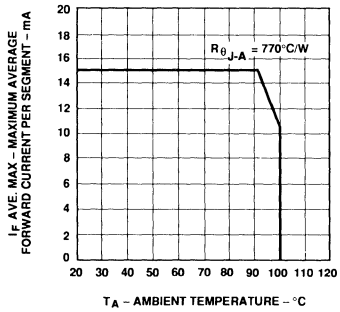


Figure 6. Maximum Allowable Average or DC Current vs. Ambient Temperature.

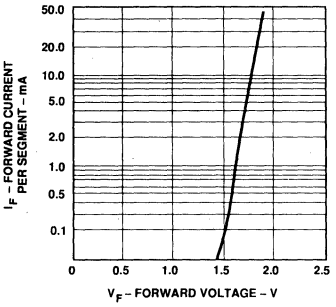


Figure 7. Forward Current vs. Forward Voltage.

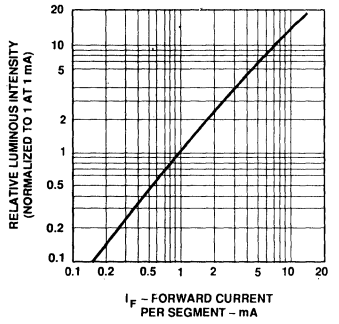


Figure 8. Relative Luminous Intensity vs. DC Forward Current.

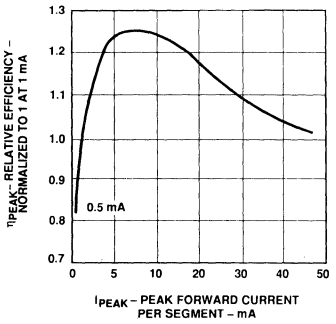


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Green

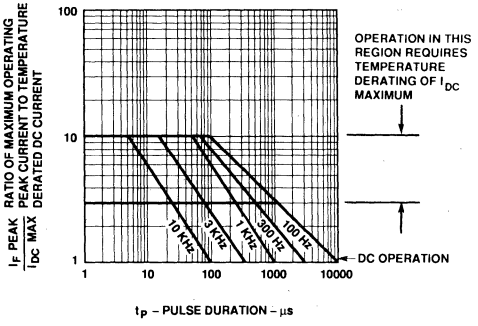


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration – HER.

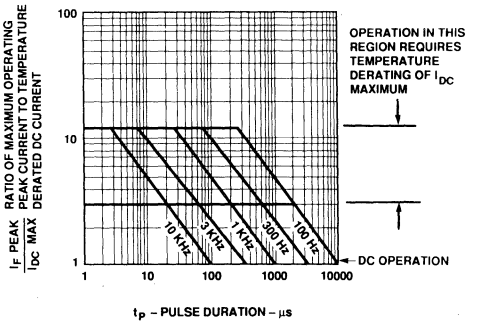


Figure 11. Maximum Tolerable Peak Current vs. Pulse Duration – Green.

HER, Green, contd.

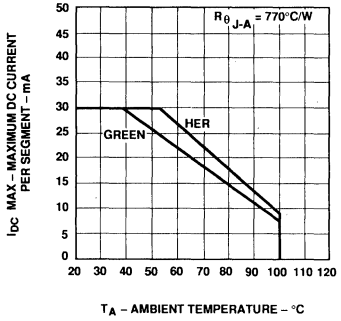


Figure 12. Maximum Allowable DC Current vs. Ambient Temperature.

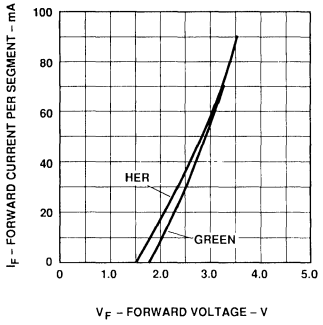


Figure 13. Forward Current vs. Forward Voltage Characteristics.

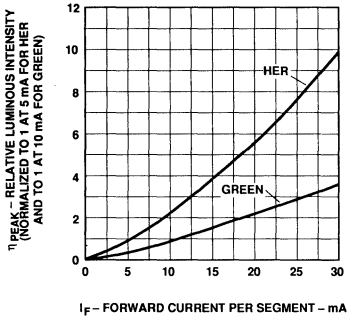


Figure 14. Relative Luminous Intensity vs. DC Forward Current.

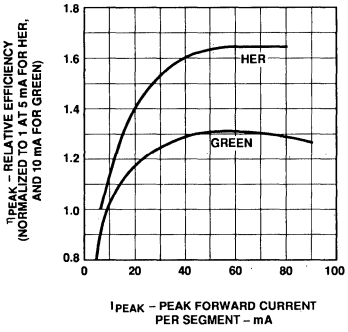


Figure 15. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Contrast Enhancement

For information on contrast enhancement, please see Application Note 1015.

Soldering/Cleaning

For information on soldering LEDs please refer to Application Note 1029.

Electrical/Optical

For more information on electrical/optical characteristics, please see Application Note 1005.

HEWLETT PACKARD

Low Current Seven Segment Displays

Technical Data

HDSP-335X Series
HDSP-555X Series
HDSP-751X Series
HDSP-A10X Series
HDSP-A80X Series
HDSP-A90X Series
HDSP-E10X Series
HDSP-F10X Series
HDSP-G10X Series
HDSP-H10X Series
HDSP-K12X, K70X Series
HDSP-N10X Series

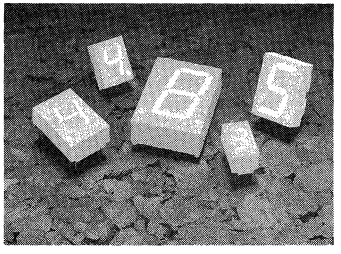
Features

- **Low Power Consumption**
- **Industry Standard Size**
- **Industry Standard Pinout**
- **Choice of Character Size**
  7.6 mm (0.30 in), 10 mm (0.40 in), 10.9 mm (0.43 in), 14.2 mm (0.56 in), 20 mm (0.8 in)
- **Choice of Colors**
  AlGaAs Red, High Efficiency Red (HER), Yellow, Green
- **Excellent Appearance**
  Evenly Lighted Segments
  ±50° Viewing Angle
- **Design Flexibility**
  Common Anode or Common Cathode
  Single and Dual Digit
  Left and Right Hand Decimal Points
  ±1. Overflow Character
- **Categorized for Luminous Intensity**
  Yellow and Green Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **Excellent for Long Digit String Multiplexing**

Description

These low current seven segment displays are designed for applications requiring low power consumption. They are tested and selected for their excellent low current characteristics to ensure that the segments are matched at low currents. Drive currents as low as 1 mA per segment are available.

Pin for pin equivalent displays are also available in a standard current or high light ambient design. The standard current displays are available in all colors and are ideal for most applications. The high light ambient displays are ideal for sunlight ambients or long string lengths. For additional information see the 7.6 mm Micro Bright Seven Segment Displays, 10 mm Seven Segment Displays, 7.6 mm/10.9 mm Seven Segment Displays, 14.2 mm Seven Segment Displays, 20 mm Seven Segment Displays, or High Light Ambient Seven Segment Displays data sheets.

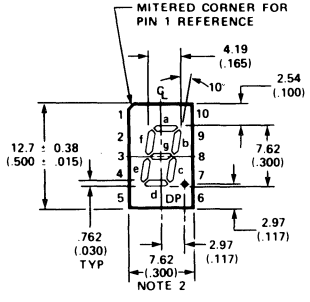


Devices

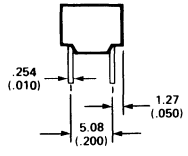
AlGaAs HDSP-	HER HDSP-	Yellow HDSP-	Green HDSP-	Description	Package Drawing
A101	7511	A801	A901	7.6 mm Common Anode Right Hand Decimal	A
A103	7513	A803	A903	7.6 mm Common Cathode Right Hand Decimal	B
A107	7517	A807	A907	7.6 mm Common Anode ±1. Overflow	C
A108	7518	A808	A908	7.6 mm Common Cathode ±1. Overflow	D
F101				10 mm Common Anode Right Hand Decimal	E
F103				10 mm Common Cathode Right Hand Decimal	F
F107				10 mm Common Anode ±1. Overflow	G
F108				10 mm Common Cathode ±1. Overflow	H
G101				10 mm Two Digit Common Anode Right Hand Decimal	X
G103				10 mm Two Digit Common Cathode Right Hand Decimal	Y
E100	3350			10.9 mm Common Anode Left Hand Decimal	I
E101	3351			10.9 mm Common Anode Right Hand Decimal	J
E103	3353			10.9 mm Common Cathode Right Hand Decimal	K
E106	3356			10.9 mm Universal ±1. Overflow[1]	L
H101	5551			14.2 mm Common Anode Right Hand Decimal	M
H103	5553			14.2 mm Common Cathode Right Hand Decimal	N
H107	5557			14.2 mm Common Anode ±1. Overflow	O
H108	5558			14.2 mm Common Cathode ±1. Overflow	P
K121	K701			14.2 mm Two Digit Common Anode Right Hand Decimal	R
K123	K703			14.2 mm Two Digit Common Cathode Right Hand Decimal	S
N100				20 mm Common Anode Left Hand Decimal	Q
N101				20 mm Common Anode Right Hand Decimal	T
N103				20 mm Common Cathode Right Hand Decimal	U
N105				20 mm Common Cathode Left Hand Decimal	V
N106				20 mm Universal ±1. Overflow[1]	W

Note:
1. Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagrams L or W.

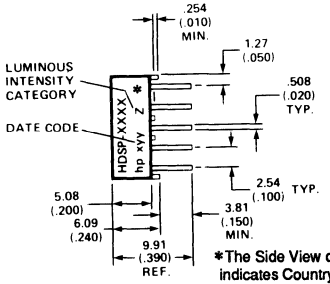
Package Dimensions

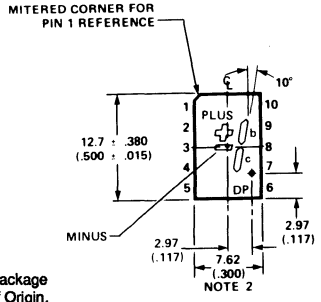


A, B



A, B, C, D



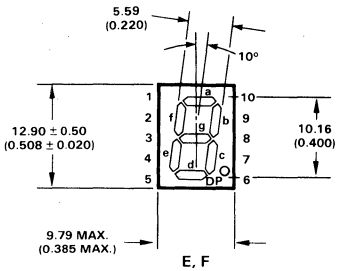


C, D

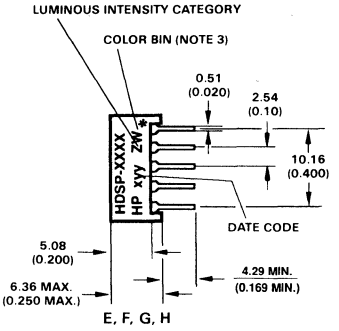
PIN	FUNCTION A	B	C	D
1	ANODE[4]	CATHODE[5]	ANODE[4]	CATHODE[5]
2	CATHODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	ANODE e	NC	NC
5	CATHODE d	ANODE d	NC	NC
6	ANODE[4]	CATHODE[5]	ANODE[4]	CATHODE[5]
7	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	ANODE a	NC	NC

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. MAXIMUM.
3. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
4. REDUNDANT ANODES.
5. REDUNDANT CATHODES.

Package Dimensions (continued)

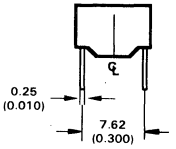


E, F

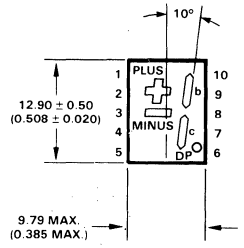


E, F, G, H

* The Side View of package indicates Country of Origin.



E, F, G, H



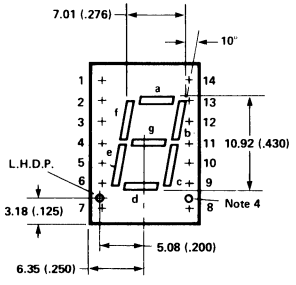
G, H

PIN	FUNCTION			
	E	F	G	H
1	ANODE[4]	CATHODE[5]	ANODE[4]	CATHODE[5]
2	CATHODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	ANODE e	NC	NC
5	CATHODE d	ANODE d	NC	NC
6	ANODE[4]	CATHODE[5]	ANODE[4]	CATHODE[5]
7	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	ANODE a	NC	NC

NOTES:

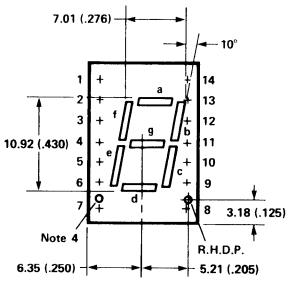
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. FOR YELLOW AND GREEN SERIES PRODUCT ONLY.
4. REDUNDANT ANODES.
5. REDUNDANT CATHODES.

Package Dimensions (continued)



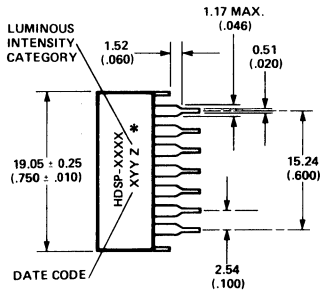
I

FRONT VIEW



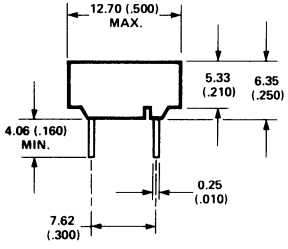
J, K

FRONT VIEW



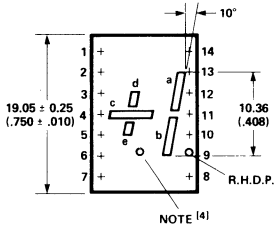
SIDE VIEW

*The Side View of package indicates Country of Origin.



END VIEW

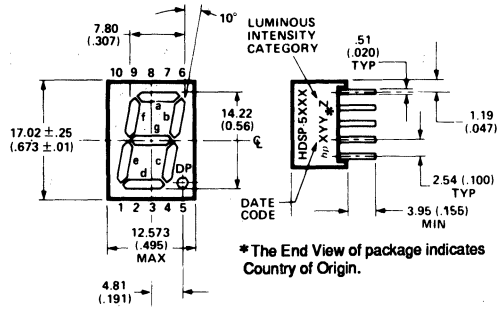
PIN	FUNCTION			
	I	J	K	L
1	CATHODE·a	CATHODE·a	ANODE·a	CATHODE·d
2	CATHODE·f	CATHODE·f	ANODE·f	ANODE·d
3	ANODE[3]	ANODE[3]	CATHODE[6]	NO PIN
4	NO PIN	NO PIN	NO PIN	CATHODE·c
5	NO PIN	NO PIN	NO PIN	CATHODE·e
6	CATHODE·dp	NO CONN.[5]	NO CONN.[5]	ANODE·e
7	CATHODE·e	CATHODE·e	ANODE·e	ANODE·c
8	CATHODE·d	CATHODE·d	ANODE·d	ANODE·dp
9	NO CONN.[5]	CATHODE·dp	ANODE·dp	CATHODE·dp
10	CATHODE·c	CATHODE·c	ANODE·c	CATHODE·b
11	CATHODE·g	CATHODE·g	ANODE·g	CATHODE·a
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE·b	CATHODE·b	ANODE·b	ANODE·a
14	ANODE[3]	ANODE[3]	CATHODE[6]	ANODE·b

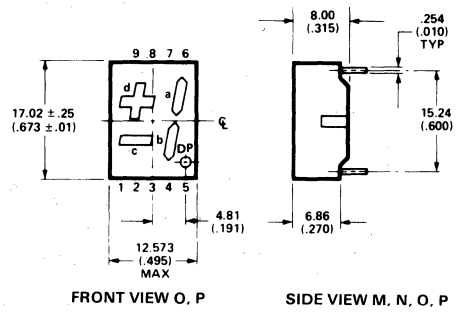


L

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. REDUNDANT ANODES.
4. UNUSED dp POSITION.
5. SEE INTERNAL CIRCUIT DIAGRAM.
6. REDUNDANT CATHODES.
7. SEE PART NUMBER TABLE FOR L.H.D.P. AND R.H.D.P. DESIGNATION.

Package Dimensions (continued)





PIN	FUNCTION			
	M	N	O	P
1	CATHODE e	ANODE e	CATHODE c	ANODE c
2	CATHODE d	ANODE d	ANODE c, d	CATHODE c, d
3	ANODE[4]	CATHODE[5]	CATHODE b	ANODE b
4	CATHODE c	ANODE c	ANODE a, b, DP	CATHODE a, b, DP
5	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
6	CATHODE b	ANODE b	CATHODE a	ANODE a
7	CATHODE a	ANODE a	ANODE a, b, DP	CATHODE a, b, DP
8	ANODE[4]	CATHODE[5]	ANODE c, d	CATHODE c, d
9	CATHODE f	ANODE f	CATHODE d	ANODE d
10	CATHODE g	ANODE g	NO PIN	NO PIN

NOTES:

1. ALL DIMENSIONS IN MILLIMETRES (INCHES).

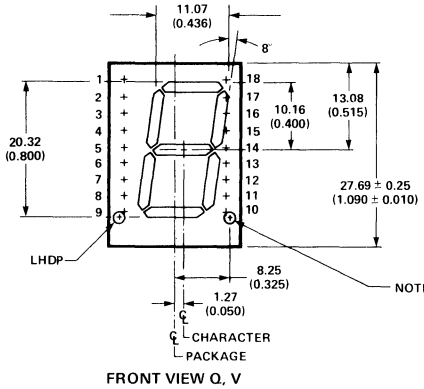
2. MAXIMUM.

3. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.

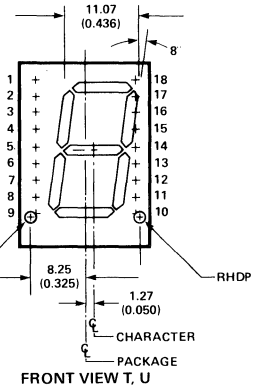
4. REDUNDANT ANODES.

5. REDUNDANT CATHODES.

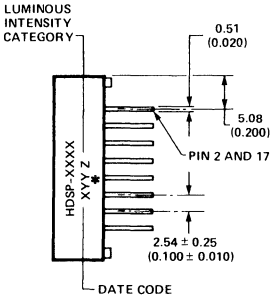
Package Dimensions (continued)



FRONT VIEW Q, V

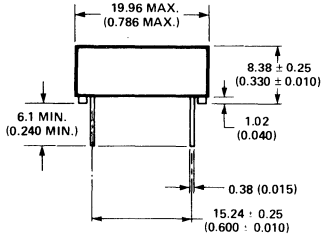


FRONT VIEW T, U



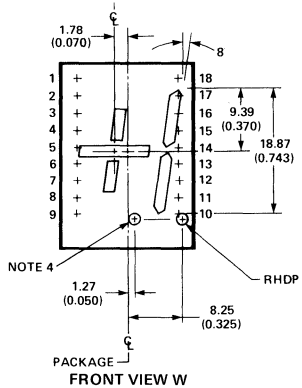
SIDE VIEW Q, T, U, V, W

***The Side View of package indicates Country of Origin.**



END VIEW Q, T, U, V, W

Pin	Function				
	Q	T	U	V	W
1	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
2	CATHODE a	CATHODE a	ANODE a	ANODE a	CATHODE a
3	CATHODE f	CATHODE f	ANODE f	ANODE f	ANODE d
4	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE d
5	CATHODE e	CATHODE e	ANODE e	ANODE e	CATHODE c
6	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE e
7	CATHODE dp	NO. CONNEC.	NO. CONNEC.	ANODE dp	ANODE e
8	NO PIN	NO PIN	NO PIN	NO PIN	CATHODE dp
9	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
10	NO PIN	CATHODE dp	ANODE dp	NO PIN	ANODE dp
11	CATHODE d	CATHODE d	ANODE d	ANODE d	CATHODE dp
12	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE b
13	CATHODE c	CATHODE c	ANODE c	ANODE c	ANODE b
14	CATHODE g	CATHODE g	ANODE g	ANODE g	ANODE c
15	CATHODE b	CATHODE b	ANODE b	ANODE b	ANODE a
16	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
17	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE a
18	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN

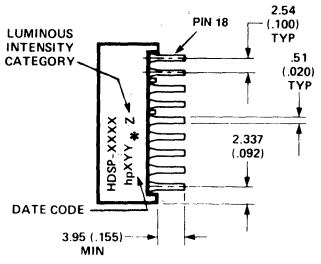


FRONT VIEW W

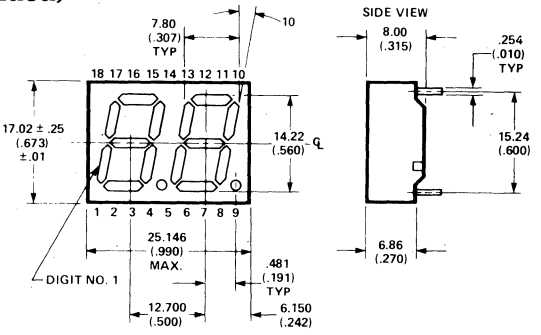
NOTES:

1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. REDUNDANT ANODES.
4. UNUSED dp POSITION.
5. SEE INTERNAL CIRCUIT DIAGRAM.
6. REDUNDANT CATHODES.
7. SEE PART NUMBER TABLE FOR L.H.D.P. AND R.H.D.P. DESIGNATION.

Package Dimensions (continued)

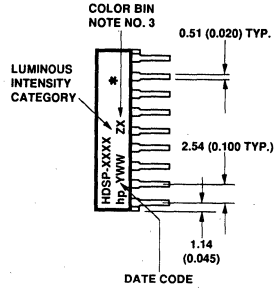


TOP END VIEW R, S

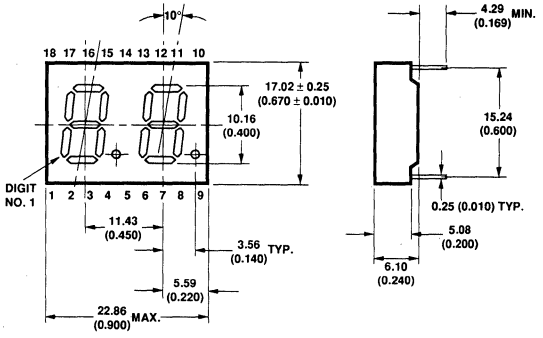


FRONT VIEW R, S

*The Side View of package indicates Country of Origin.



TOP END VIEW X, Y



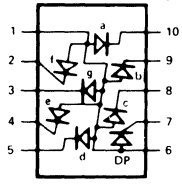
FRONT VIEW X, Y

*The Side View of package indicates Country of Origin.

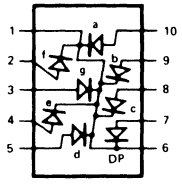
Pin	Function	
	R,X	S,Y
1	E CATHODE NO. 1	E ANODE NO. 1
2	D CATHODE NO. 1	D ANODE NO. 1
3	C CATHODE NO. 1	C ANODE NO. 1
4	DP CATHODE NO. 1	DP ANODE NO. 1
5	E CATHODE NO. 2	E ANODE NO. 2
6	D CATHODE NO. 2	D ANODE NO. 2
7	G CATHODE NO. 2	G ANODE NO. 2
8	C CATHODE NO. 2	C ANODE NO. 2
9	DP CATHODE NO. 2	DP ANODE NO. 2
10	B CATHODE NO. 2	B ANODE NO. 2
11	A CATHODE NO. 2	A ANODE NO .2
12	F CATHODE NO. 2	F ANODE NO. 2
13	DIGIT NO. 2 ANODE	DIGIT NO. 2 CATHODE
14	DIGIT NO. 1 ANODE	DIGIT NO. 1 CATHODE
15	B CATHODE NO. 1	B ANODE NO. 1
16	A CATHODE NO. 1	A ANODE NO. 1
17	G CATHODE NO. 1	G ANODE NO. 1
18	F CATHODE NO. 1	F ANODE NO. 1

NOTES:
1. DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIIMENSIONS ARE FOR REFERENCE ONLY.
3. WHERE APPLICABLE.

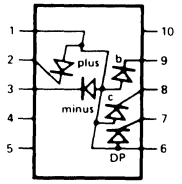
Internal Circuit Diagram



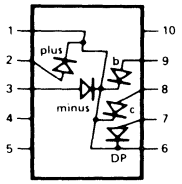
A, E



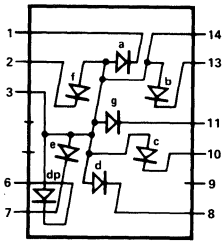
B, F



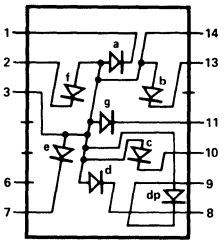
C, G



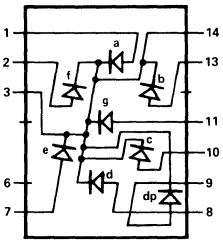
D, H



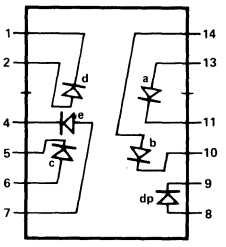
I



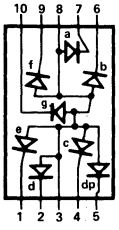
J



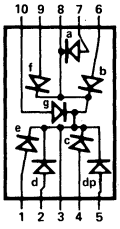
K



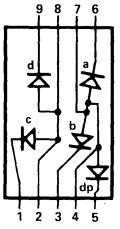
L



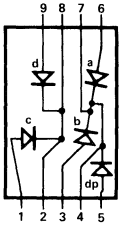
M



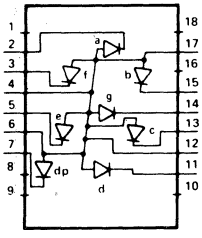
N



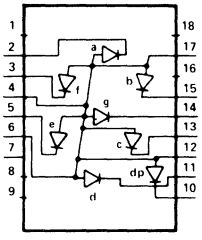
O



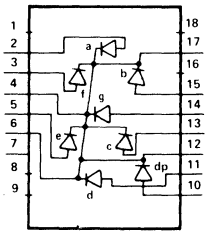
P



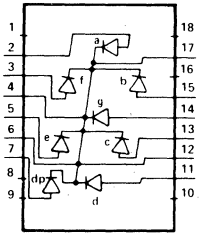
Q



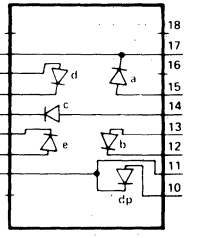
T



U

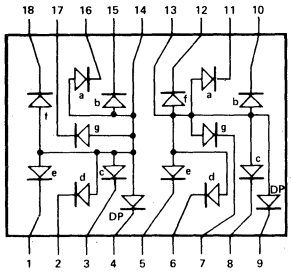


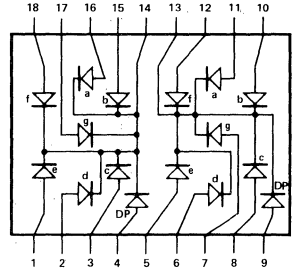
V

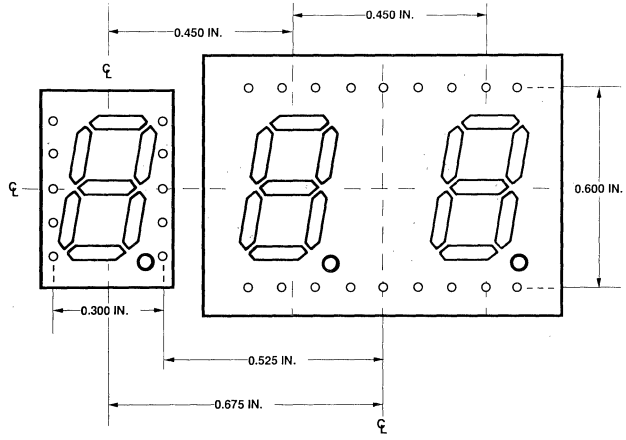


W

Internal Circuit Diagram (continued)







HOLE PATTERN FOR PCB LAYOUT TO ACHIEVE UNIFORM 0.450 In. DIGIT TO DIGIT PITCH. FOR HDSP-FXXX TO HDSP-GXXX.

Absolute Maximum Ratings

Description	AlGaAs Red HDSP-A10X/E10X/ H10X/K12X/N10X/ F10X, G10X Series	HER HDSP-751X/ 335X/555X/ K70X Series	Yellow HDSP-A80X Series	Green HDSP-A90X Series	Units
Average Power per Segment or DP	37	52		64	mW
Peak Forward Current per Segment or DP	45				mA
DC Forward Current per Segment or DP	15[1]	15[2]			mA
Operating Temperature Range	-20 to +100	-40 to +100			°C
Storage Temperature Range	-55 to +100				°C
Reverse Voltage per Segment or DP	3.0				V
Lead Solder Temperature for 3 Seconds (1.60 mm [0.063 in.] below seating plane)	260				°C

Notes:
1. Derate above 91°C at 0.53 mA/°C.
2. Derate HER/Yellow above 80°C at 0.38 mA/°C and Green above 71°C at 0.31 mA/°C.

Electrical/Optical Characteristics at T_A = 25°C

AlGaAs Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A10X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	315	600		µcd	I_F = 1 mA
				3600			I_F = 5 mA
F10X, G10X			330	650			I_F = 1 mA
				3900			I_F = 5 mA
E10X			390	650			I_F = 1 mA
				3900			I_F = 5 mA
H10X, K12X			400	700			I_F = 1 mA
				4200			I_F = 5 mA
N10X			270	590			I_F = 1 mA
				3500			I_F = 5 mA
All Devices	Forward Voltage/Segment or DP	V_F		1.6		V	I_F = 1 mA
				1.7			I_F = 5 mA
				1.8	2.2		I_F = 20 mA Pk
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2 mV		mV/°C	
A10X	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		255		°C/W/Seg	
F10X, G10X				320			
E10X				340			
H10X, K12X				400			
N10X				430			

High Efficiency Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
751X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	160	270		µcd	I_F = 2 mA
				1050			I_F = 5 mA
335X, 555X, K70X			200	300			I_F = 2 mA
				1200			I_F = 5 mA
			270	370			I_F = 2 mA
				1480			I_F = 5 mA
All Devices	Forward Voltage/Segment or DP	V_F		1.6		V	I_F = 2 mA
				1.7			I_F = 5 mA
				2.1	2.5		I_F = 20 mA Pk
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
751X	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W	
335X				280			
555X, K70X				345			

Yellow

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A80X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	250	420		µcd	I_F = 4 mA
				1300			I_F = 10 mA
	Forward Voltage/Segment or DP	V_F		1.7		V	I_F = 4 mA
				1.8			I_F = 5 mA
				2.1	2.5		I_F = 20 mA Pk
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,5]	λ_d	581.5	585	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W	

Green

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A90X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	250	475		µcd	I_F = 4 mA
				1500			I_F = 10 mA
	Forward Voltage/Segment or DP	V_F		1.9		V	I_F = 4 mA
				2.0			I_F = 10 mA
				2.1	2.5		I_F = 20 mA Pk
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,5]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W	

Notes:
1. Device case temperature is 25°C prior to the intensity measurement.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is the single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. The yellow (HDSP-A800) and Green (HDSP-A900) displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

AlGaAs Red

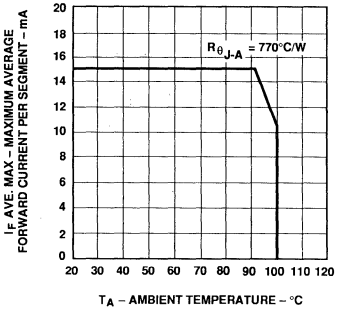


Figure 1. Maximum Allowable Average or DC Current vs. Ambient Temperature.

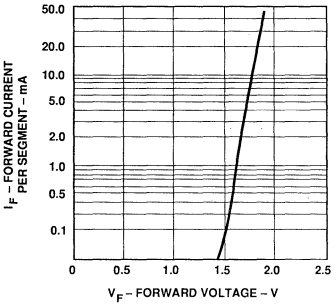


Figure 2. Forward Current vs. Forward Voltage.

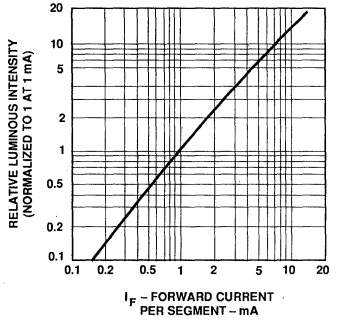


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

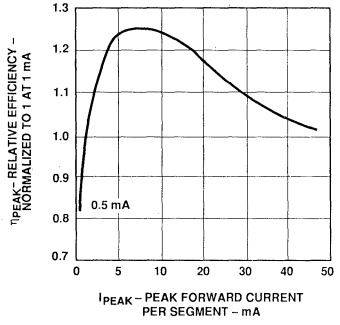


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Yellow, Green

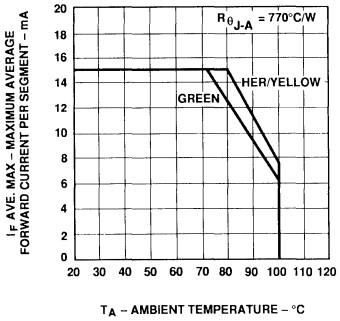


Figure 5. Maximum Allowable Average or DC Current vs. Ambient Temperature.

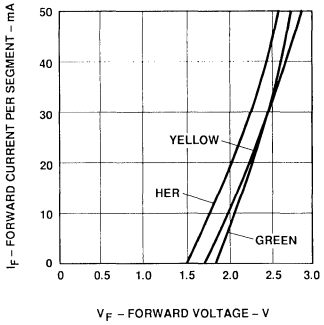


Figure 6. Forward Current vs. Forward Voltage.

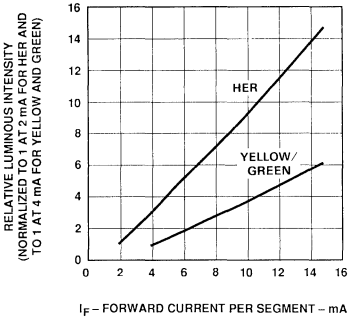


Figure 7. Relative Luminous Intensity vs. DC Forward Current.

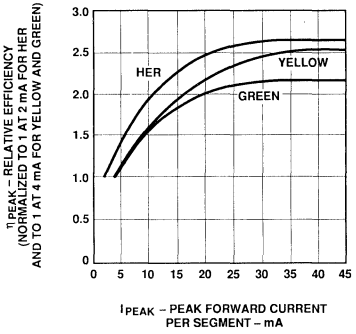


Figure 8. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Electrical/Optical

For more information on electrical/optical characteristics, please see Application Note 1005.

Contrast Enhancement

For information on contrast enhancement please see Application Note 1015.

Soldering/Cleaning

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chorinated hydrocarbon family (methylene chloride, trichloro-ethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

For information on soldering LEDs please refer to Application Note 1027.

HEWLETT PACKARD

New

8 mm (0.31 inch) Ultra Mini Seven Segment Displays

Technical Data

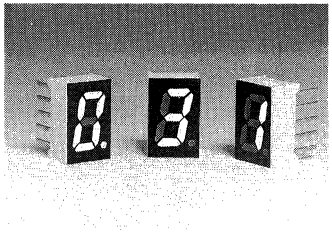
HDSP-U0XX Series
HDSP-U1XX Series
HDSP-U2XX Series
HDSP-U3XX Series
HDSP-U4XX Series
HDSP-U5XX Series

Features

- **Compact Package**
- **8 mm (0.31 inch) Character Height**
- **Choice of Colors**
  Wide Range of Colors
- **Excellent Appearance**
  Evenly Lighted Segments
  Mitered Corners on Segments
  Gray/Black Surface Gives Optimum Contrast
  ±50° Viewing Angle
- **Design Flexibility**
  Common Anode or Common Cathode
  Right Hand Decimal Point
- **Categorized for Luminous Intensity**
  Yellow and Green also Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **High Light Output**
- **High Peak Current**
- **Excellent for Long Digit String Multiplexing**
- **Intensity and Color Selection Option**

Description

The 8 mm (0.31 inch) LED seven segment displays are HP's most space-efficient character size. They are designed for viewing distances up to 3 metres (10 feet). The numeric devices feature a right hand decimal point. All devices are available as either common anode or common cathode.

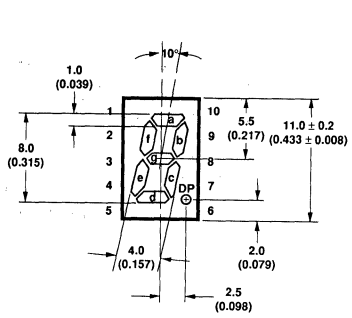


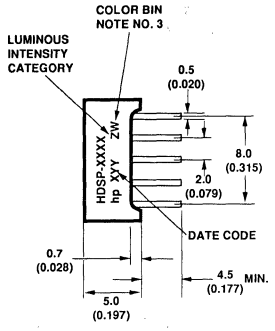
Typical applications include appliances, temperature controllers, and digital panel meters.

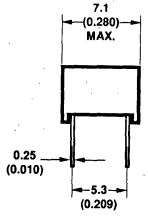
Devices

Red HDSP-	AlGaAs Red HDSP-	HER HDSP-	Orange HDSP-	Yellow HDSP-	Green HDSP-	Description	Circuit Diagram
U001	U101	U201	U401	U301	U501	Common Anode, Right Hand Decimal, Gray Surface	A
U003	U103	U203	U403	U303	U503	Common Cathode, Right Hand Decimal, Gray Surface	B
U011	U111	U211	U411	U311	U511	Common Anode, Right Hand Decimal, Black Surface	A
U013	U113	U213	U413	U313	U513	Common Cathode, Right Hand Decimal, Black Surface	B

Package Dimensions

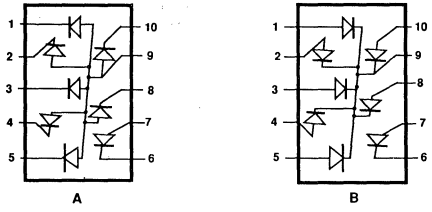






NOTES:
1. ALL DIMENSIONS IN MILLIMETERS (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. FOR YELLOW AND GREEN SERIES PRODUCT ONLY.

Internal Circuit Diagram



PIN	FUNCTION	
	A	B
1	CATHODE a	ANODE a
2	CATHODE f	ANODE f
3	CATHODE g	ANODE g
4	CATHODE e	ANODE e
5	CATHODE d	ANODE d
6	CATHODE DP	CATHODE DP
7	ANODE DP	ANODE DP
8	CATHODE c	ANODE c
9	ANODE	CATHODE
10	CATHODE b	ANODE b

HDSP-UXXX circuit

Absolute Maximum Ratings

Description	Red HDSP-U0XX Series	AlGaAs Red HDSP-U1XX Series	HER/Orange HDSP-U2XX/-4XX Series	Yellow HDSP-U3XX Series	Green HDSP-U5XX Series	Units
Average Power per Segment or DP	82	37	105	80	105	mW
Peak Forward Current per Segment or DP	150[1]	45[3]	90[5]	60[7]	90[9]	mA
DC Forward Current per Segment or DP	25[2]	15[4]	30[6]	20[8]	30[10]	mA
Operating Temperature Range	-25 to +90	-20 to +90	-25 to +90			°C
Storage Temperature Range	-30 ~ +90					°C
Reverse Voltage per Segment or DP	3.0					V
Lead Solder Temperature for 3 Seconds (1.60 mm [0.063 in.] below seating plane)	260					°C

Notes:

1. See Figure 1 to establish pulsed conditions.
2. Derate above 80°C at 0.63 mA/°C (see figure 3).
3. See Figure 2 to establish pulsed conditions.
4. No derating over specified temperature range.
5. See Figure 7 to establish pulsed conditions.
6. Derate above 53°C at 0.45 mA/°C (see figure 10).
7. See Figure 8 to establish pulsed conditions.
8. Derate above 81°C at 0.52 mA/°C (see figure 10).
9. See Figure 9 to establish pulsed conditions.
10. Derate above 39°C at 0.37 mA/°C (see figure 10).

Electrical/Optical Characteristics at T_A = 25°C

Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-U0XX	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	600	1100		µcd	I_F = 20 mA
				500			I_F = 10 mA
	Forward Voltage/Segment or DP	V_F		1.6	2.0	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		655		nm	
	Dominant Wavelength[3]	λ_d		640		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	12		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		200		°C/W/ Seg	

AlGaAs Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-U1XX	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	315	600		µcd	I_F = 1 mA
				3600			I_F = 5 mA
	Forward Voltage/Segment or DP	V_F		1.6		V	I_F = 1 mA
				1.7			I_F = 5 mA
				1.8	2.2		I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		255		°C/W/ Seg	

High Efficiency Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-U2XX	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	360	980		µcd	I_F = 5 mA
				5390			I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.0	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		200		°C/W/ Seg	

Orange

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-U4XX	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	360	980		µcd	I_F = 5 mA
				5390			I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.0	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		600		nm	
	Dominant Wavelength[3]	λ_d		603		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		200		°C/W/ Seg	

Yellow

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-U3XX	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	225	480		µcd	I_F = 5 mA
				2740			I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.2	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,5]	λ_d	581.5	586	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50.0		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		200		°C/W/ Seg	

High Performance Green

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-U5XX	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	860	3000		µcd	I_F = 10 mA
				6800			I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 10 mA
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,5]	λ_d		571		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50.0		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		200		°C/W/ Seg	

Notes:

1. Case temperature of device immediately prior to the intensity measurement is 25°C.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. The Yellow (HDSP-U3XX) series and Green (HDSP-U5XX) series displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

Red, AlGaAs Red

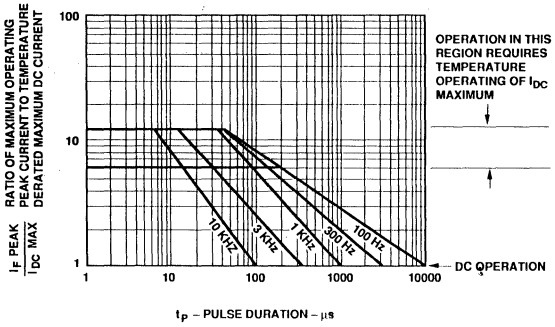


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration – Red.

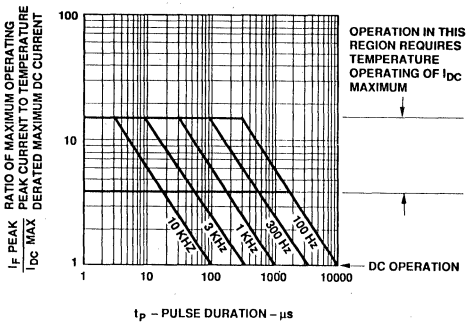


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration – AlGaAs Red.

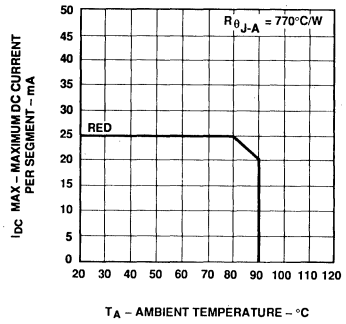


Figure 3. Maximum Allowable DC Current vs. Ambient Temperature.

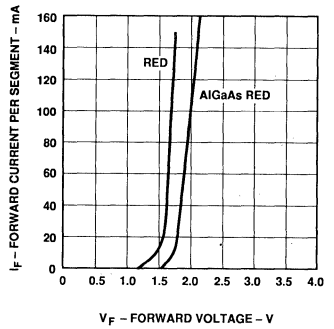


Figure 4. Forward Current vs. Forward Voltage.

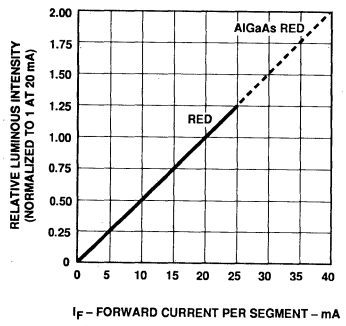


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

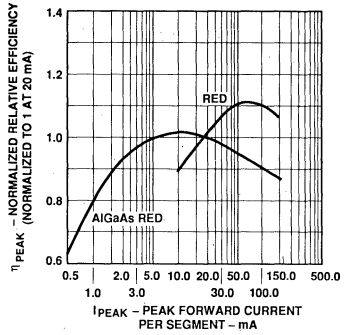


Figure 6. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Orange, Yellow, Green

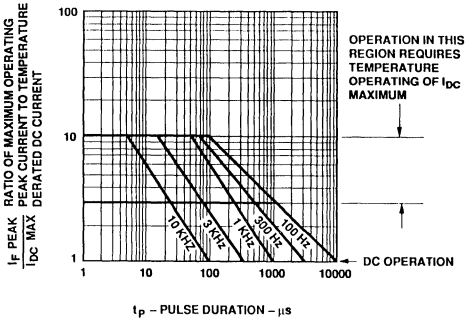


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration – Her, Orange.

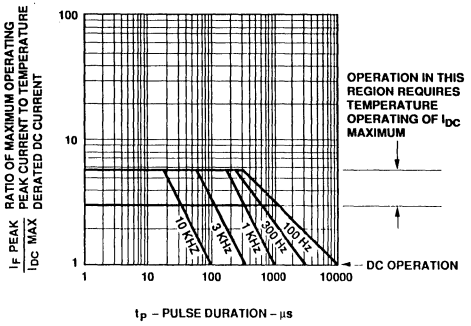


Figure 8. Maximum Tolerable Peak Current vs. Pulse Duration – Yellow.

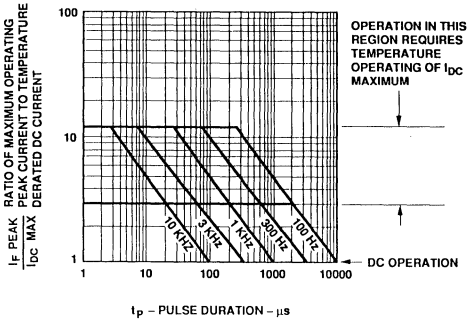


Figure 9. Maximum Tolerable Peak Current vs. Pulse Duration – Green.

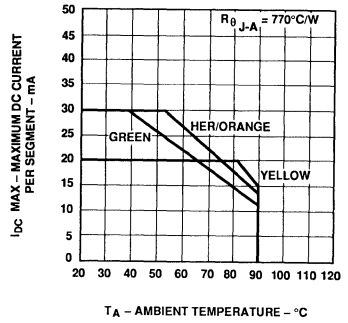


Figure 10. Maximum Allowable DC Current vs. Ambient Temperature.

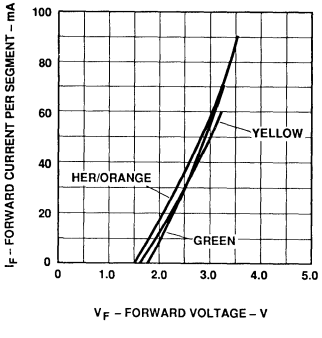


Figure 11. Forward Current vs. Forward Voltage Characteristics.

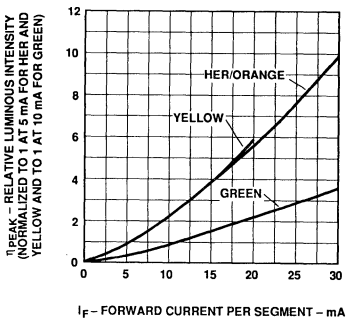


Figure 12. Relative Luminous Intensity vs. DC Forward Current.

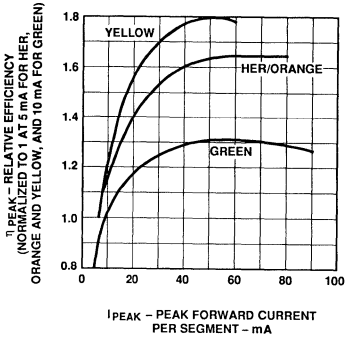


Figure 13. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Electrical/Optical

For more information on electrical/optical characteristics, please see Application Note 1005.

Contrast Enhancement

For information on contrast enhancement please see Application Note 1015.

Soldering/Cleaning

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chorinated hydrocarbon family (methylene chloride, trichloro-ethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating materials used to form the package of plastic LED parts.

For more information on soldering LEDs please refer to Application Note 1027.

HEWLETT PACKARD

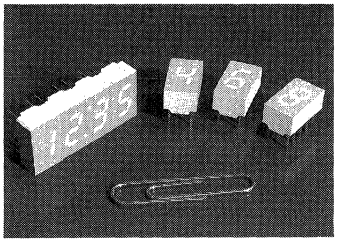
7.6 mm (0.3 inch) Micro Bright Seven Segment Displays

Technical Data

HDSP-730X Series
HDSP-731X Series
HDSP-740X Series
HDSP-750X Series
HDSP-780X Series
HDSP-A15X Series

Features

- **Available with Colon for Clock Display**
- **Compact Package**
  0.300 x 0.500 inches
  Leads on 2.54 mm (0.1 inch) Centers
- **Choice of Colors**
  Red, AlGaAs Red, High Efficiency Red, Yellow, Green
- **Excellent Appearance**
  Evenly Lighted Segments
  Mitered Corners on Segments
  Surface Color Gives Optimum Contrast
  ±50° Viewing Angle
- **Design Flexibility**
  Common Anode or Common Cathode
  Right Hand Decimal Point
  ±1. Overflow Character
- **Categorized for Luminous Intensity**
  Yellow and Green
  Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **High Light Output**
- **High Peak Current**
- **Excellent for Long Digit String Multiplexing**
- **Intensity and Color Selection Available**
  See Intensity and Color Selected Displays Data Sheet
- **Sunlight Viewable AlGaAs**



Description

The 7.6 mm (0.3 inch) LED seven segment displays are designed for viewing distances up to 3 metres (10 feet). These devices use an industry standard size package and

Devices

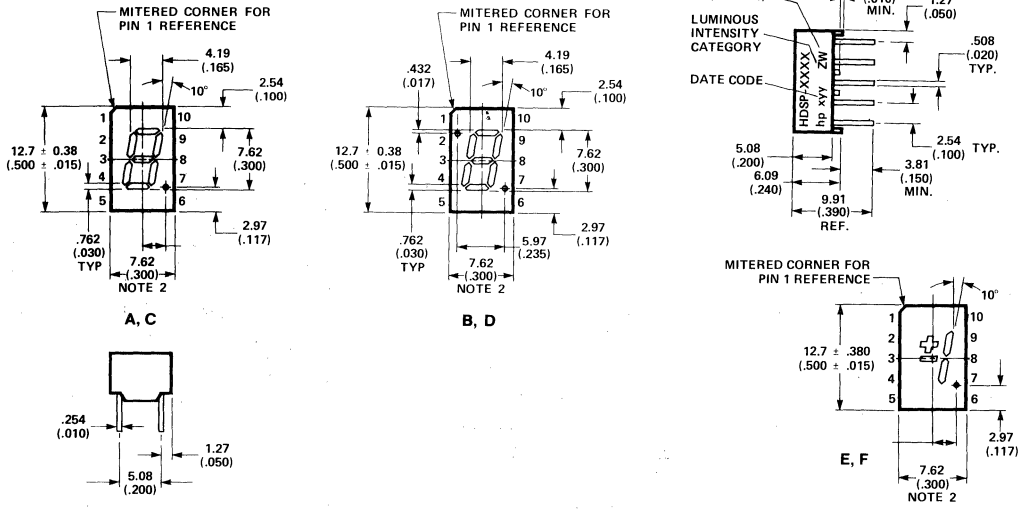
Red HDSP-	AlGaAs[1] HDSP-	HER[1] HDSP-	Yellow[1] HDSP-	Green[1] HDSP-	Description	Package Drawing
7301	A151	7501	7401	7801	Common Anode Right Hand Decimal	A
7302		7502	7402	7802	Common Anode Right Hand Decimal, Colon	B
7303	A153	7503	7403	7803	Common Cathode Right Hand Decimal	C
7304		7504	7404	7804	Common Cathode Right Hand Decimal, Colon	D
7307	A157	7507	7407	7807	Common Anode ±1. Overflow	E
7308	A158	7508	7408	7808	Common Cathode ±1. Overflow	F

Note:
1. These displays are recommended for high ambient light operation. Please refer to the HDSP-A10X AlGaAs, HDSP-335X HER, HDSP-A80X Yellow, and HDSP-A90X Green data sheet for low current operation.

pinout. Both the numeric and ±1. overflow devices feature a right hand decimal point. All devices are available as either common anode or common cathode.

These displays are ideal for most applications. Pin for pin equivalent displays are also available in a low current design. The low current displays are ideal for portable applications. For additional information see the Low Current Seven Segment Displays.

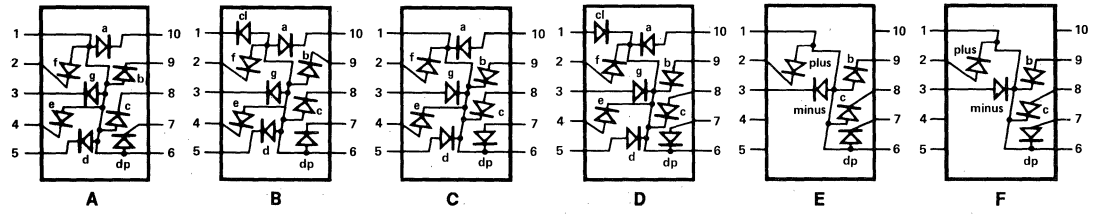
Package Dimensions



NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. MAXIMUM.
3. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
4. REDUNDANT ANODES.
5. REDUNDANT CATHODES.
6. FOR HDSP-7400/-7800 SERIES PRODUCT ONLY.

	FUNCTION					
PIN	A	B	C	D	E	F
1	ANODE[4]	CATHODE COLON	CATHODE[5]	ANODE COLON	ANODE[4]	CATHODE[5]
2	CATHODE f	CATHODE f	ANODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	CATHODE g	ANODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	CATHODE e	ANODE e	ANODE e	NC	NC
5	CATHODE d	CATHODE d	ANODE d	ANODE d	NC	NC
6	ANODE[4]	ANODE	CATHODE[5]	CATHODE	ANODE[4]	CATHODE[5]
7	CATHODE DP	CATHODE DP	ANODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	CATHODE c	ANODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	CATHODE b	ANODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	CATHODE a	ANODE a	ANODE a	NC	NC

Internal Circuit Diagram



Absolute Maximum Ratings

Description	Red HDSP-7300 Series	AlGaAs Red HDSP-A150 Series	HER HDSP-7500 Series	Yellow HDSP-7400 Series	Green HDSP-7800 Series	Units
Average Power per Segment or DP	82	96	105	80	105	mW
Peak Forward Current per Segment or DP	150[1]	160[3]	90[5]	60[7]	90[9]	mA
DC Forward Current per Segment or DP	25[2]	40[4]	30[6]	20[8]	30[10]	mA
Operating Temperature Range	-40 to +100	-20 to +100[11]	-40 to +100			°C
Storage Temperature Range	-55 to +100					°C
Reverse Voltage per Segment or DP	3.0					V
Lead Solder Temperature for 3 Seconds (1.60 mm [0.063 in.] below seating plane)	260					°C

Notes:

1. See Figure 1 to establish pulsed conditions.
2. Derate above 80°C at 0.63 mA/°C.
3. See Figure 2 to establish pulsed conditions.
4. Derate above 46°C at 0.54 mA/°C.
5. See Figure 7 to establish pulsed conditions.
6. Derate above 53°C at 0.45 mA/°C.
7. See Figure 8 to establish pulsed conditions.
8. Derate above 81°C at 0.52 mA/°C.
9. See Figure 9 to establish pulsed conditions.
10. Derate above 39°C at 0.37 mA/°C.
11. For operation below -20°C, contact your local HP components sales office or an authorized distributor.

Electrical/Optical Characteristics at T_A = 25°C

Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
730X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	600	1100		µcd	I_F = 20 mA
				500			I_F = 10 mA
All	Forward Voltage/Segment or DP	V_F		1.6	2.0	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		655		nm	
	Dominant Wavelength[3]	λ_d		640		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	12		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W/Seg	

AlGaAs Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A15X	Luminous Intensity/Segment[1,2,5] (Digit Average)	I_V	6.9	14.0		mcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.8		V	I_F = 20 mA
				2.0	3.0	V	I_F = 100 mA
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15.0		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		255		°C/W/Seg	

High Efficiency Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
750X	Luminous Intensity/Segment[1,2,6] (Digit Average)	I_V	360	980		µcd	I_F = 5 mA
				5390			I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.0	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W/Seg	

Yellow

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
740X	Luminous Intensity/Segment[1,2,7] (Digit Average)	I_V	225	480		µcd	I_F = 5 mA
				2740			I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.2	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,9]	λ_d	581.5	586	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50.0		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W/Seg	

High Performance Green

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
780X	Luminous Intensity/Segment[1,2,8] (Digit Average)	I_V	860	3000		µcd	I_F = 10 mA
				6800			I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 10 mA
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,9]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50.0		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W/Seg	

Notes:
1. Case temperature of device immediately prior to the intensity measurement is 25°C.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. For low current operation the AlGaAs HDSP-A101 series displays are recommended.
6. For low current operation the HER HDSP-7511 series displays are recommended.
7. For low current operation the Yellow HDSP-A801 series displays are recommended.
8. For low current operation the Green HDSP-A901 series displays are recommended.
9. The yellow (HDSP-7400) and Green (HDSP-7800) displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

Red, AlGaAs Red

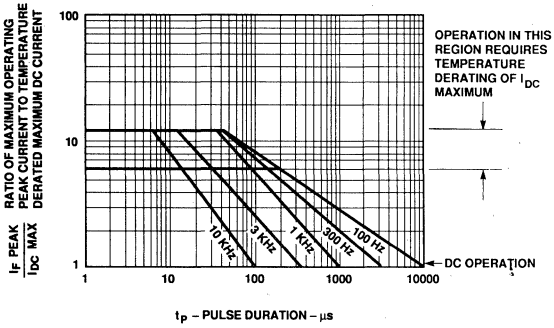


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration – Red.

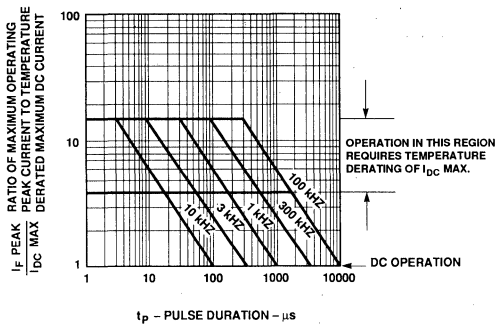


Figure 2. Maximum Allowed Peak Current vs. Pulse Duration – AlGaAs Red.

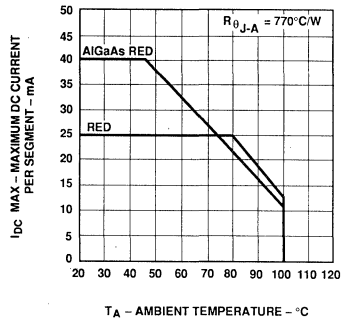


Figure 3. Maximum Allowable DC Current per Segment as a Function of Ambient Temperature.

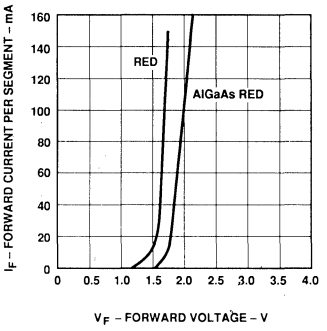


Figure 4. Forward Current vs. Forward Voltage.

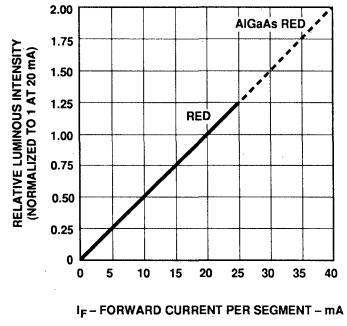


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

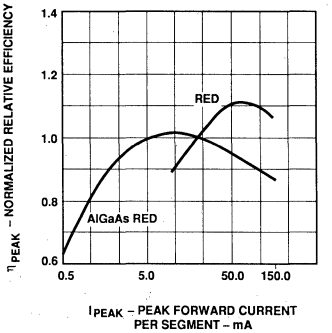


Figure 6. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Yellow, Green

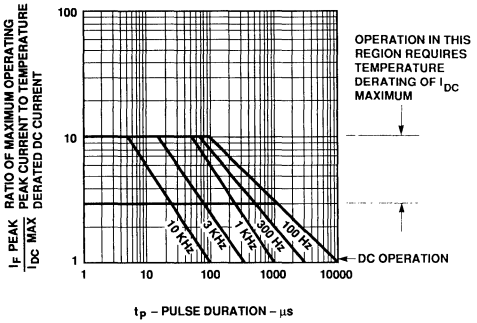


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration – HER.

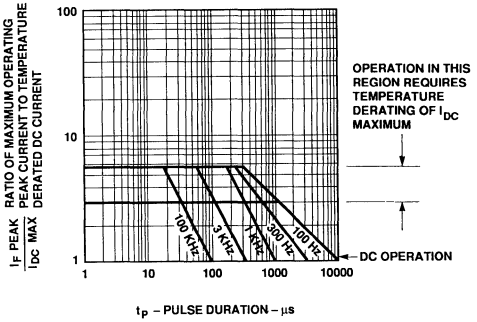


Figure 8. Maximum Tolerable Peak Current vs. Pulse Duration – Yellow.

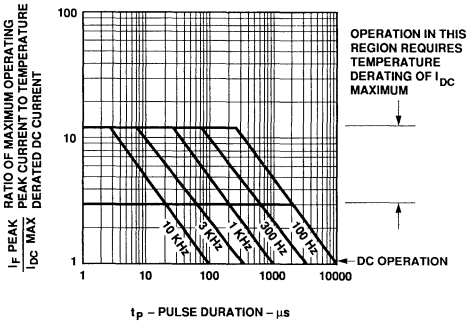


Figure 9. Allowable Peak Current vs. Pulse Duration – Green.

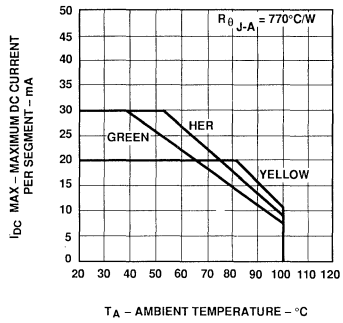


Figure 10. Maximum Allowable DC Current per Segment as a Function of Ambient Temperature.

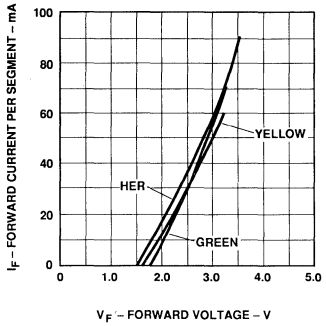


Figure 11. Forward Current vs. Forward Voltage Characteristics.

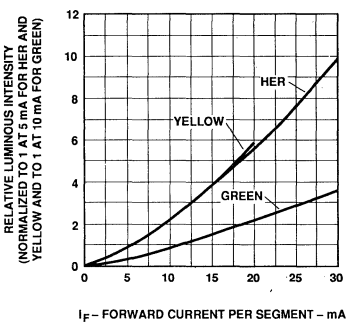


Figure 12. Relative Luminous Intensity vs. DC Forward Current.

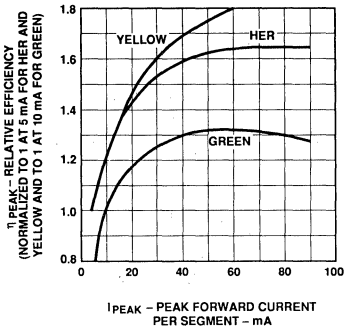


Figure 13. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Electrical/Optical

For more information on electrical/optical characteristics, please see Application Note 1005.

Contrast Enhancement

For information on contrast enhancement please see Application Note 1015.

Soldering/Cleaning

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloro-ethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

For further information on soldering LEDs please refer to Application Note 1027.

HEWLETT PACKARD

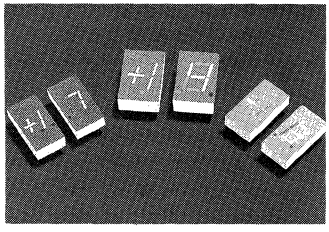
7.6 mm (0.3 inch)/10.9 mm (0.43 inch) Seven Segment Displays

Technical Data

5082-761X Series
5082-762X Series
5082-765X Series
5082-766X Series
5082-773X Series
5082-7740
5082-775X Series
5082-7760
HDSP-360X Series
HDSP-460X Series
HDSP-E15X Series

Features

- **Industry Standard Size**
- **Industry Standard Pinout**
  7.62 mm (0.300 inch) DIP Leads on 2.54 mm (0.100 inch) Centers
- **Choice of Colors**
  Red, AlGaAs Red, High Efficiency Red, Yellow, Green
- **Excellent Appearance**
  Evenly Lighted Segments
  Surface Color Gives Optimum Contrast
  ±50° Viewing Angle
- **Design Flexibility**
  Common Anode or Common Cathode
  Single Digits
  Left or Right Hand Decimal Point
  ±1. Overflow Character
- **Categorized for Luminous Intensity**
  Yellow and Green Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **High Light Output**
- **High Peak Current**
- **Excellent for Long Digit String Multiplexing**
- **Intensity and Color Selection Available**
  See Intensity and Color Selected Displays Data Sheet
- **Sunlight Viewable AlGaAs**



Description

The 7.6 mm (0.3 inch) and 10.9 mm (0.43 inch) LED seven segment displays are designed for viewing distances up to 3 metres (10 feet) and 5 metres (16 feet). These devices use an industry standard size package and pinouts. All devices are available as either common anode or common cathode.

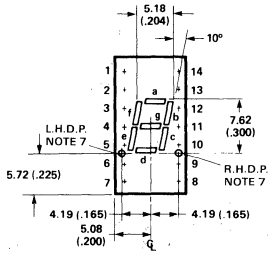
Devices

Red 5082-	AlGaAs[1] Red HDSP-	HER[1] 5082-	Yellow 5082-	Green HDSP-	Description	Package Drawing
7730		7610	7620	3600	7.6 mm Common Anode Left Hand Decimal	A
7731		7611	7621	3601	7.6 mm Common Anode Right Hand Decimal	B
7740		7613	7623	3603	7.6 mm Common Cathode Right Hand Decimal	C
7736		7616	7626	3606	7.6 mm Universal ±1. Overflow Right Hand Decimal[2]	D
7750	E150	7650	7660	4600	10.9 mm Common Anode Left Hand Decimal	E
7751	E151	7651	7661	4601	10.9 mm Common Anode Right Hand Decimal	F
7760	E153	7653	7663	4603	10.9 mm Common Cathode Right Hand Decimal	G
7756	E156	7656	7666	4606	10.9 mm Universal ±1. Overflow Right Hand Decimal[2]	H

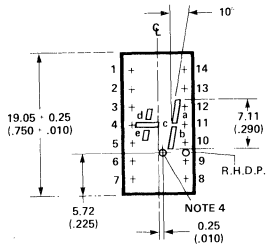
Notes:
1. These displays are recommended for high ambient light operation. Please refer to the HDSP-E10X AlGaAs and HDSP-335X HER data sheet for low current operation.
2. Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram H.

These displays are ideal for most applications. Pin for pin equivalent displays are also available in a low current or high light ambient design. The low current displays are ideal for portable applications. The high light ambient displays are ideal for high light ambients or long string lengths. For additional information see the Low Current Seven Segment Displays, or High Light Ambient Seven Segment Displays data sheets.

Package Dimensions

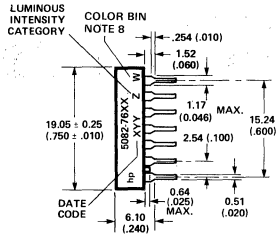


A,B,C

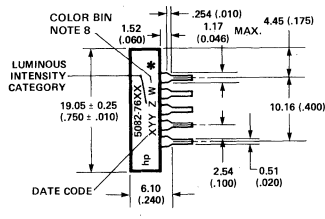


D

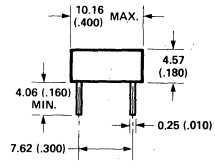
	FUNCTION			
PIN	A	B	C	D
1	CATHODE-a	CATHODE-a	NO PIN	ANODE-d
2	CATHODE-f	CATHODE-f	CATHODE[6]	NO PIN
3	ANODE[3]	ANODE[3]	ANODE-f	CATHODE-d
4	NO PIN	NO PIN	ANODE-g	CATHODE-c
5	NO PIN	NO PIN	ANODE-e	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	ANODE-d	ANODE-e
7	CATHODE-e	CATHODE-e	NO PIN	ANODE-c
8	CATHODE-d	CATHODE-d	NO PIN	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	CATHODE[6]	NO PIN
10	CATHODE-c	CATHODE-c	ANODE-dp	CATHODE-dp
11	CATHODE-g	CATHODE-g	ANODE-c	CATHODE-b
12	NO PIN	NO PIN	ANODE-b	CATHODE-a
13	CATHODE-b	CATHODE-b	ANODE-a	ANODE-a
14	ANODE[3]	ANODE[3]	NO PIN	ANODE-b



A,B,C SIDE



C SIDE

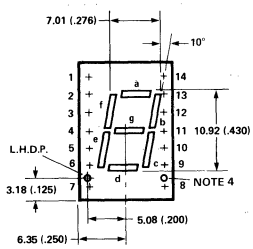


A,B,C,D END

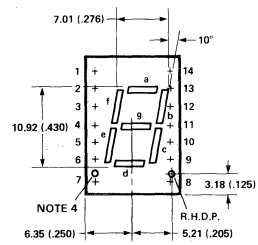
*The Side View of package indicates Country of Origin.

NOTES;

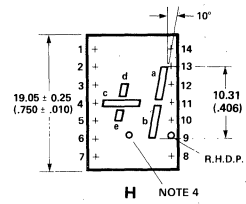
1. **DIMENSIONS IN MILLIMETRES AND (INCHES).**
2. **ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.**
3. **REDUNDANT ANODES.**
4. **UNUSED DP POSITION.**
5. **SEE INTERNAL CIRCUIT DIAGRAM.**
6. **REDUNDANT CATHODE.**
7. **SEE PART NUMBER TABLE FOR L.H.D.P. AND R.H.D.P. DESIGNATION.**
8. **FOR YELLOW AND GREEN DEVICES ONLY.**



E

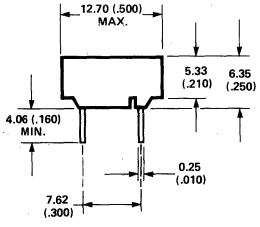


F,G FRONT VIEW

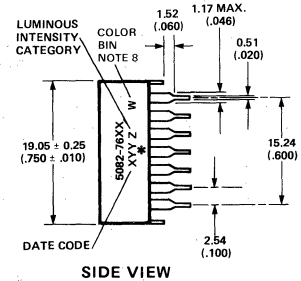


H NOTE 4

	FUNCTION			
PIN	E	F	G	H
1	CATHODE-a	CATHODE-a	ANODE-a	CATHODE-d
2	CATHODE-f	CATHODE-f	ANODE-f	ANODE-d
3	ANODE[3]	ANODE[3]	CATHODE[6]	NO PIN
4	NO PIN	NO PIN	NO PIN	CATHODE-c
5	NO PIN	NO PIN	NO PIN	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	NO CONN.[5]	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-e	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-d	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	ANODE-dp	CATHODE-dp
10	CATHODE-c	CATHODE-c	ANODE-c	CATHODE-b
11	CATHODE-g	CATHODE-g	ANODE-g	CATHODE-a
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE-b	CATHODE-b	ANODE-b	ANODE-a
14	ANODE[3]	ANODE[3]	CATHODE[6]	ANODE-b



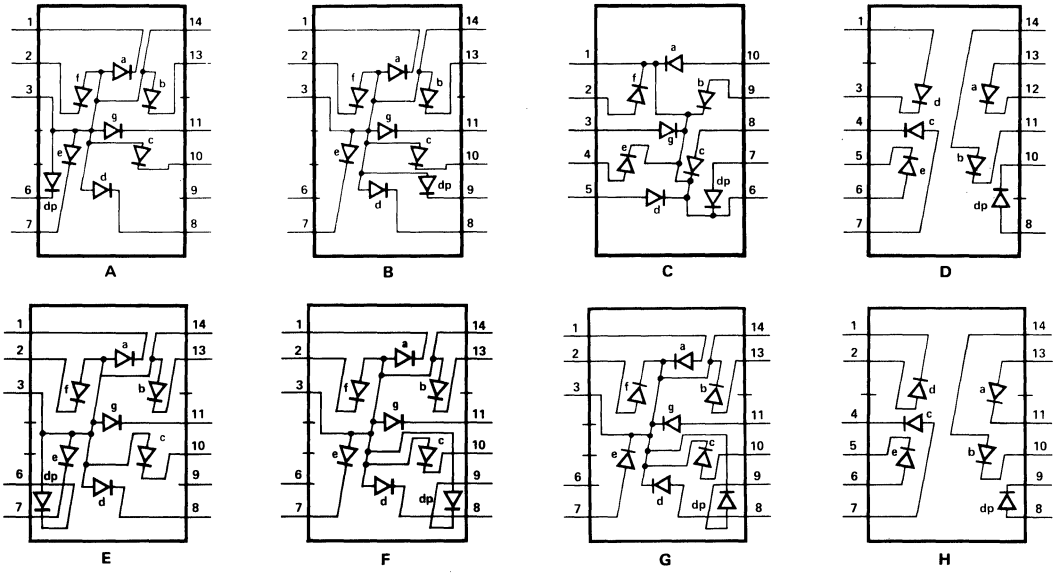
END VIEW



SIDE VIEW

*The Side View of package indicates Country of Origin.

Internal Circuit Diagram



Absolute Maximum Ratings

Description	Red 5082-7700 Series	AlGaAs Red HDSP-E150 Series	HER 5082-7610/ 7650 Series	Yellow 5082-7620/ 7660 Series	Green HDSP-3600/ 4600 Series	Units
Average Power per Segment or DP	82	96	105	80	105	mW
Peak Forward Current per Segment or DP	150[1]	160[3]	90[5]	60[7]	90[9]	mA
DC Forward Current per Segment or DP	25[2]	40[4]	30[6]	20[8]	30[10]	mA
Operating Temperature Range	-40 to +100	-20 to +100[11]	-40 to +100			°C
Storage Temperature Range	-55 to +100					°C
Reverse Voltage per Segment or DP	3.0					V
Lead Solder Temperature for 3 Seconds (1.59 mm [0.063 in.] below seating plane	260					°C

Notes:

1. See Figure 1 to establish pulsed conditions.
2. Derate above 80°C at 0.63 mA/°C.
3. See Figure 2 to establish pulsed conditions.
4. Derate above 46°C at 0.54 mA/°C.
5. See Figure 7 to establish pulsed conditions.
6. Derate above 53°C at 0.45 mA/°C.
7. See Figure 8 to establish pulsed conditions.
8. Derate above 81°C at 0.52 mA/°C.
9. See Figure 9 to establish pulsed conditions.
10. Derate above 39°C at 0.37 mA/°C.
11. For operation below -20°C, contact your local HP components sales office or an authorized distributor.

Electrical/Optical Characteristics at T_A = 25°C

Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
5082-773X 5082-774X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	360	770		µcd	I_F = 20 mA
5082-775X 5082-776X			360	1100		µcd	I_F = 20 mA
All	Forward Voltage/Segment or DP	V_F		1.6	2.0	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		655		nm	
	Dominant Wavelength[3]	λ_d		640		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	12		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		280		°C/W/Seg	

AlGaAs Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-E15X	Luminous Intensity/Segment[1,2,5] (Digit Average)	I_V	8.5	15.0		mcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.8		V	I_F = 20 mA
				2.0	3.0	V	I_F = 100 mA
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		340		°C/W/Seg	

High Efficiency Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
5082-761X	Luminous Intensity/Segment[1,2,6] (Digit Average)	I_V	340	800		µcd	I_F = 5 mA
5082-765X			340	1115		µcd	I_F = 5 mA
All	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		280		°C/W	

Yellow

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
5082-762X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	205	620		µcd	I_F = 5 mA
5082-766X			290	835		µcd	I_F = 5 mA
All	Forward Voltage/Segment or DP	V_F		2.2	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,7]	λ_d	581.5	586	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	40		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		280		°C/W/Seg	

High Performance Green

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-360X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	860	2700		µcd	I_F = 10 mA
HDSP-460X			1030	4000		µcd	I_F = 10 mA
All	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 10 mA
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,7]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		280		°C/W/Seg	

Notes:
1. Device case temperature is 25°C prior to the intensity measurement.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. For low current operation, the AlGaAs HDSP-E10X series displays are recommended. They are tested at 1 mA dc/segment and are pin for pin compatible with the HDSP-E15X series.
6. For low current operation, the HER HDSP-335X series displays are recommended. They are tested at 2 mA dc/segment and are pin for pin compatible with the 5082-7650 series.
7. The Yellow (5082-7620/7660) and Green (HDSP-3600/4600) displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

Red, AlGaAs Red

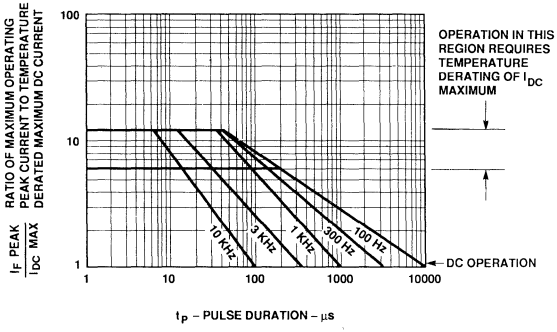


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration – Red.

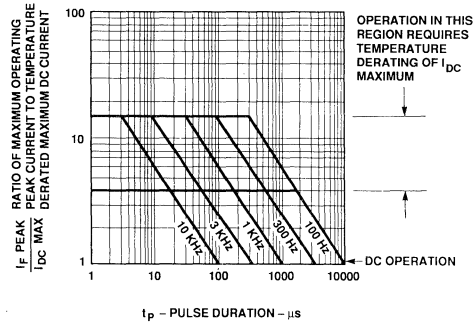


Figure 2. Maximum Allowed Peak Current vs. Pulse Duration – AlGaAs Red.

Red, AlGaAs Red (Continued)

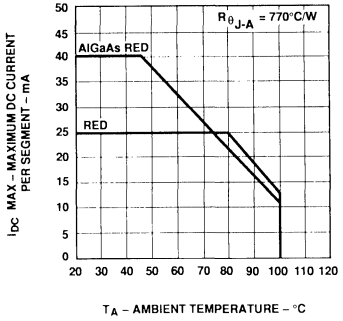


Figure 3. Maximum Allowable DC Current vs. Ambient Temperature.

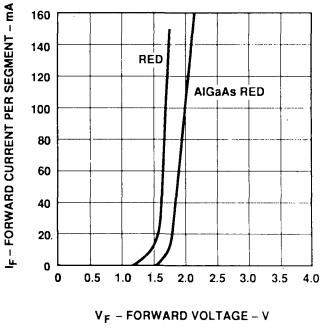


Figure 4. Forward Current vs. Forward Voltage.

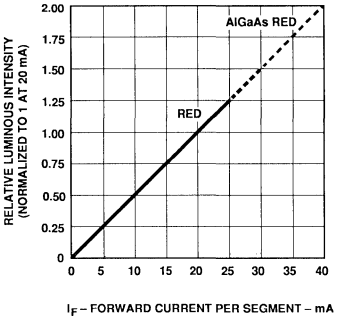


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

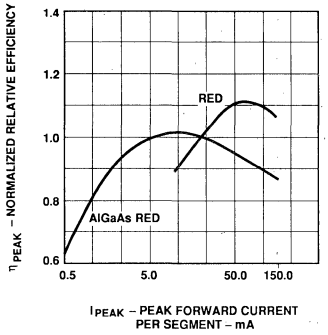


Figure 6. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Yellow, Green

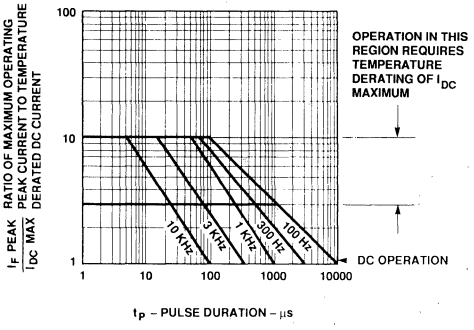


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration – HER Series.

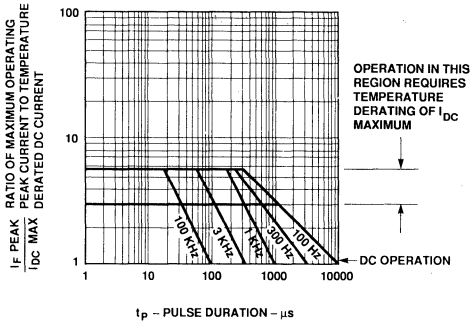


Figure 8. Maximum Tolerable Peak Current vs. Pulse Duration – Yellow Series.

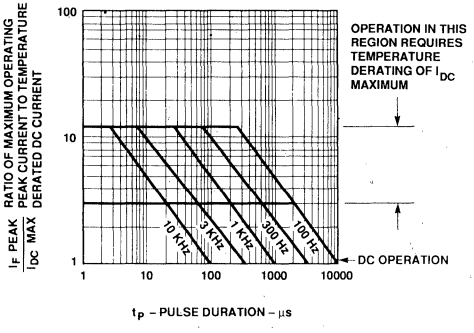


Figure 9. Allowable Peak Current vs. Pulse Duration – Green Series.

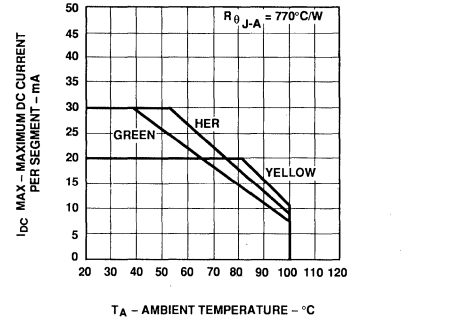


Figure 10. Maximum Allowable DC Current vs. Ambient Temperature.

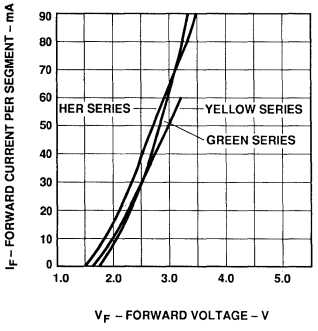


Figure 11. Forward Current vs. Forward Voltage.

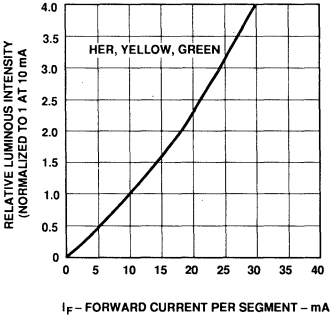


Figure 12. Relative Luminous Intensity vs. DC Forward Current.

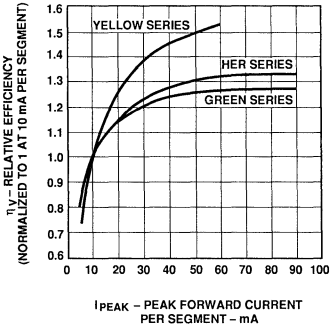


Figure 13. Relative Luminous Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Contrast Enhancement

For information on contrast enhancement please see Application Note 1015.

Soldering/Cleaning

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloro-ethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

For further information on soldering LEDs please refer to Application Note 1027.

HEWLETT PACKARD

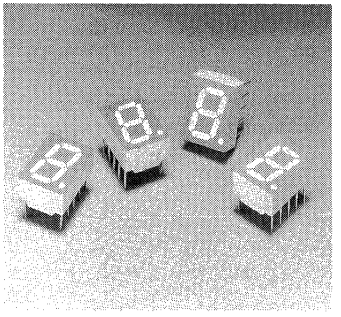
10 mm (0.40 inch) Seven Segment Displays

Technical Data

HDSP-F00X Series
HDSP-F15X Series
HDSP-F20X Series
HDSP-F30X Series
HDSP-F40X Series
HDSP-F50X Series
HDSP-G00X Series
HDSP-G15X Series
HDSP-G20X Series
HDSP-G30X Series
HDSP-G40X Series
HDSP-G50X Series

Features

- **Industry Standard Size**
- **Industry Standard Pinout**
  7.6 mm (0.3 inch) DIP Single
  15.24 mm (0.6 inch) DIP Dual
  Leads on 2.54 mm
  (0.1 inch) Centers
- **Choice of Colors**
  Red, AlGaAs Red, High Efficiency Red, Orange, Yellow, Green
- **Excellent Appearance**
  Evenly Lighted Segments
  Mitered Corners on Segments
  Gray Package Gives Optimum Contrast
  ±50° Viewing Angle
- **Design Flexibility**
  Common Anode or
  Common Cathode
  Single and Dual Digits
  Right Hand Decimal Point
  ±1. Overflow Character
- **Categorized for Luminous Intensity**
  Yellow and Green
  Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **High Light Output**
- **High Peak Current**
- **Excellent for Long Digit String Multiplexing**



- **Intensity and Color Selection Option**
- **Sunlight Viewable AlGaAs**

Devices

Red HDSP-	AlGaAs Red[1] HDSP-	HER HDSP-	Orange HDSP-	Yellow HDSP-	Green HDSP-	Description	Package Drawing
F001	F151	F201	F401	F301	F501	Common Anode Right Hand Decimal	A
F003	F153	F203	F403	F303	F503	Common Cathode Right Hand Decimal	B
F007	F157	F207	F407	F307	F507	Common Anode ±1. Overflow	C
F008	F158	F208	F408	F308	F508	Common Cathode ±1. Overflow	D
G001	G151	G201	G401	G301	G501	Two Digit Common Anode Right Hand Decimal	E
G003	G153	G203	G403	G303	G503	Two Digit Common Cathode Right Hand Decimal	F

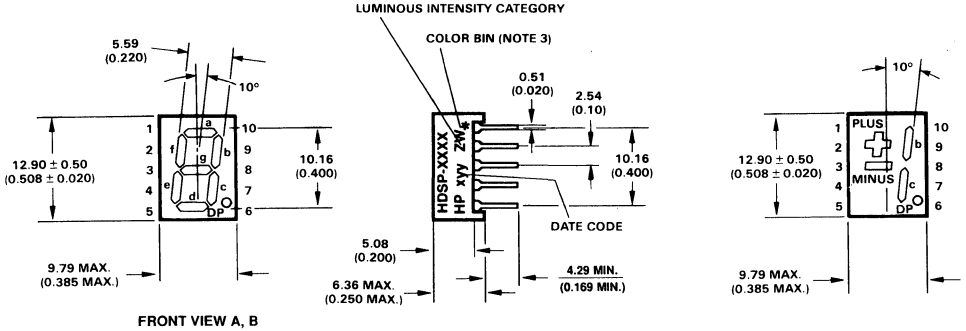
Note:
1. These displays are recommended for high ambient light operation. Please refer to the HDSP-F10X data sheet for low current operation.

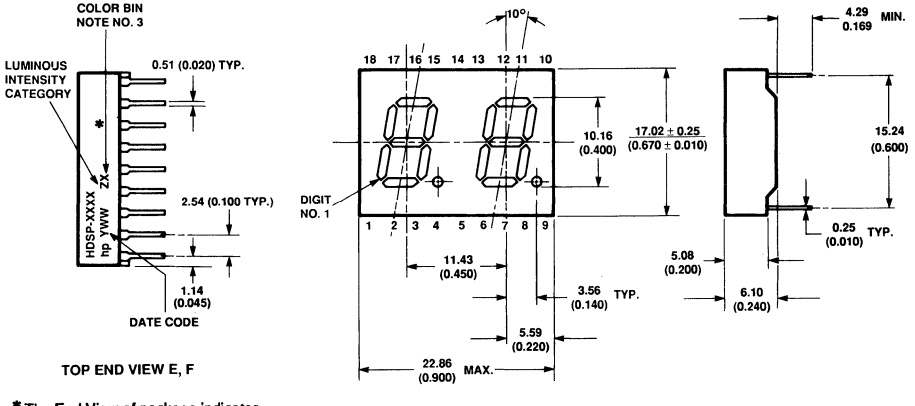
Description

The 10 mm (0.40 inch) LED seven segment displays are HP's most space-efficient character size. They are designed for viewing distances up to 4.5 metres (15 feet). These devices use an industry standard size package and pinout. The dual numeric, single numeric, and ±1. overflow devices feature a right hand decimal point. All devices are available as either common anode or common cathode.

Typical applications include instruments, point of sale terminals, and appliances.

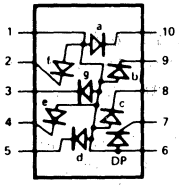
Package Dimensions



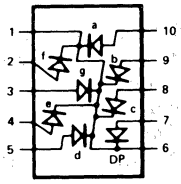


NOTES:
1. DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIIMENSIONS ARE FOR REFERENCE ONLY.
3. WHERE APPLICABLE.

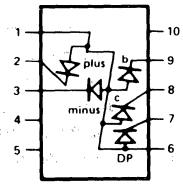
Internal Circuit Diagram



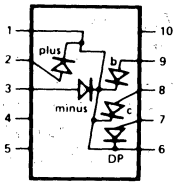
A



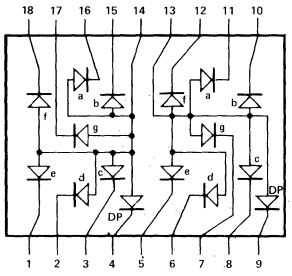
B



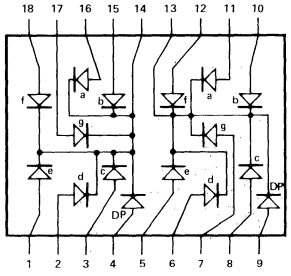
C



D



E

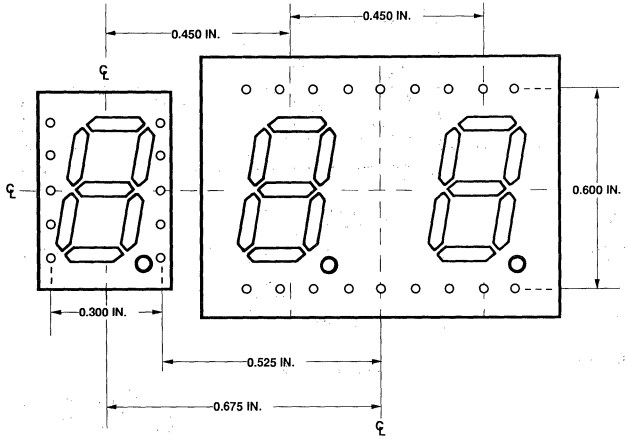


F

PIN	FUNCTION			
	A	B	C	D
1	ANODE[1]	CATHODE[2]	ANODE[1]	CATHODE[2]
2	CATHODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	ANODE e	NC	NC
5	CATHODE d	ANODE d	NC	NC
6	ANODE[1]	CATHODE[2]	ANODE[1]	CATHODE[2]
7	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	ANODE a	NC	NC

NOTES:
1. REDUNDANT ANODES
2. REDUNDANT CATHODES

PIN	FUNCTION	
	E	F
1	E CATHODE NO. 1	E ANODE NO. 1
2	D CATHODE NO. 1	D ANODE NO. 1
3	C CATHODE NO. 1	C ANODE NO. 1
4	DP CATHODE NO. 1	DP ANODE NO. 1
5	E CATHODE NO. 2	E ANODE NO. 2
6	D CATHODE NO. 2	D ANODE NO. 2
7	G CATHODE NO. 2	G ANODE NO. 2
8	C CATHODE NO. 2	C ANODE NO. 2
9	CP CATHODE NO. 2	DP ANODE NO. 2
10	B CATHODE NO. 2	B ANODE NO. 2
11	A CATHODE NO. 2	A ANODE NO. 2
12	F CATHODE NO. 2	F ANODE NO. 2
13	DIGIT NO. 2 ANODE	DIGIT NO. 2 CATHODE
14	DIGIT NO. 1 ANODE	DIGIT NO. 1 CATHODE
15	B CATHODE NO. 1	B ANODE NO. 1
16	A CATHODE NO. 1	A ANODE NO. 1
17	G CATHODE NO. 1	G ANODE NO. 1
18	F CATHODE NO. 1	F ANODE NO. 1



HOLE PATTERN FOR PCB LAYOUT TO ACHIEVE UNIFORM 0.450 In. DIGIT TO DIGIT PITCH. FOR HDSP-FXXX TO HDSP-GXXX.

Absolute Maximum Ratings

Description	Red HDSP-F00X/G00X Series	AlGaAs Red HDSP-F15X/G15X Series	HER/Orange HDSP-F20X/G20X/G40X Series	Yellow HDSP-F30X/G30X Series	Green HDSP-F50X/G50X Series	Units
Average Power per Segment or DP	82	96	105	80	105	mW
Peak Forward Current per Segment or DP	150[1]	160[3]	90[7]	60[7]	90[9]	mA
DC Forward Current per Segment or DP	25[2]	40[4]	30[6]	20[8]	30[10]	mA
Operating Temperature Range	-40 to +100	-20 to +100[11]	-40 to +100			°C
Storage Temperature Range	-55 to +100					°C
Reverse Voltage per Segment or DP	3.0					V
Lead Solder Temperature for 3 Seconds (1.59 mm [0.63 in.] below seating plane)	260					°C

Notes:
1. See Figure 1 to establish pulsed conditions.
2. Derate above 80°C at 0.63 mA/°C.
3. See Figure 2 to establish pulsed conditions.
4. Derate above 46°C at 0.54 mA/°C.
5. See Figure 7 to establish pulsed conditions.
6. Derate above 53°C at 0.45 mA/°C.
7. See Figure 8 to establish pulsed conditions.
8. Derate above 81°C at 0.52 mA/°C.
9. See Figure 9 to establish pulsed conditions.
10. Derate above 39°C at 0.37 mA/°C.
11. For operation below -20°C, contact your local HP components sales office or an authorized distributor.

Electrical/Optical Characteristics at T_A = 25°C

Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-F00X/G00X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	650	1200		µcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.6	2.0	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		655		nm	
	Dominant Wavelength[3]	λ_d		640		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	12		V	I_F = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		320		°C/W/Seg	

AlGaAs Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-F15X/ G15X	Luminous Intensity/Segment[1,2,5] (Digit Average)	I_V	7.5	15.0		mcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.8	2.2	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		320		°C/W/Seg	

High Efficiency Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-F20X/ G20X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	420	1200		µcd	I_F = 5 mA
	Forward Voltage/Segment or DP	V_F		2.0	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		320		°C/W/Seg	

Orange

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-F40X/ G40X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	420	1200		µcd	I_F = 5 mA
	Forward Voltage/Segment or DP	V_F		2.0	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		600		nm	
	Dominant Wavelength[3]	λ_d		603		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		320		°C/W/Seg	

Yellow

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-F30X/ G30X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	290	800		µcd	I_F = 5 mA
	Forward Voltage/Segment or DP	V_F		2.2	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,6]	λ_d	581.5	586	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	40		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		320		°C/W/Seg	

High Performance Green

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-F50X/ G50X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	1030	3500		µcd	I_F = 10 mA
	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 10 mA
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,6]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		320		°C/W/Seg	

Notes:
1. Case temperature of device immediately prior to the intensity measurement is 25°C.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. For low current operation, the AlGaAs HDSP-F10X, G10X series displays are recommended. They are tested at 1 mA dc/segment and are pin for pin compatible with the HDSP-F15X/G15X series.
6. The Yellow (HDSP-F30X/G30X) series and Green (HDSP-F50X/G50X) series displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

RED, AlGaAs Red

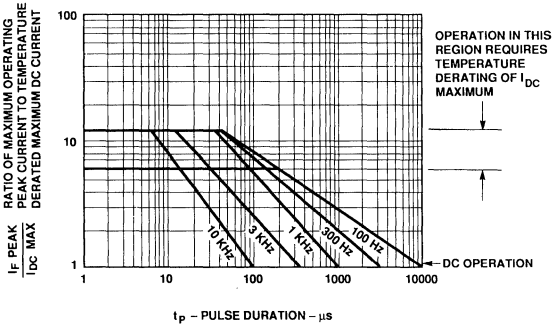


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration – Red.

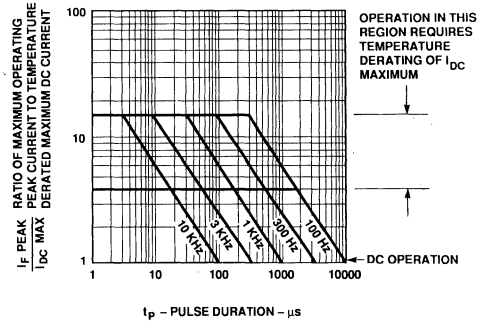


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration – AlGaAs Red.

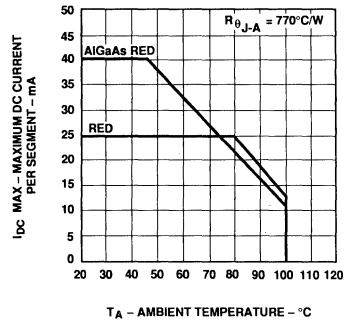


Figure 3. Maximum Allowable DC Current vs. Ambient Temperature.

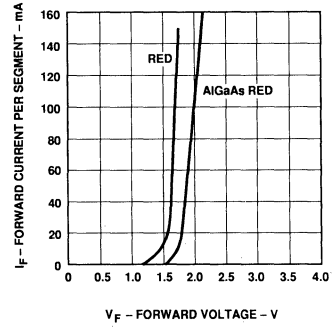


Figure 4. Forward Current vs. Forward Voltage.

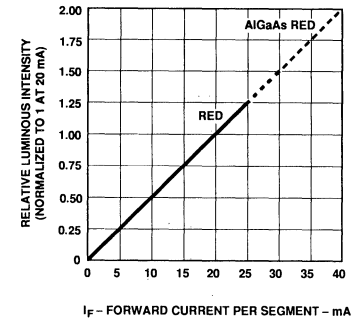


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

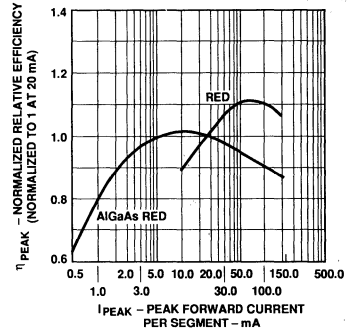


Figure 6. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Orange, Yellow, Green

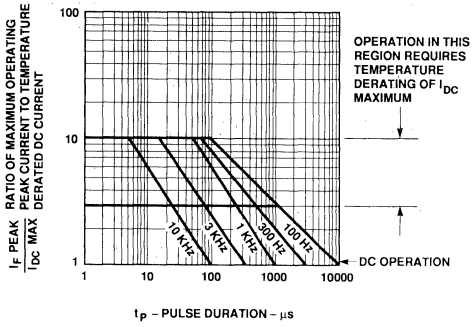


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration – HER, Orange.

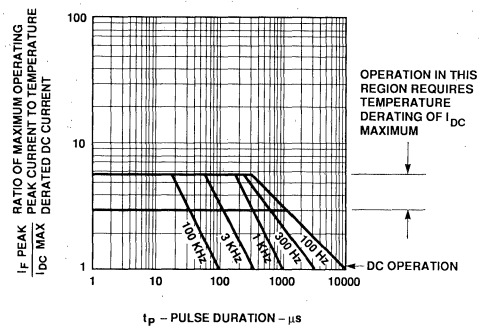


Figure 8. Maximum Tolerable Peak Current vs. Pulse Duration – Yellow.

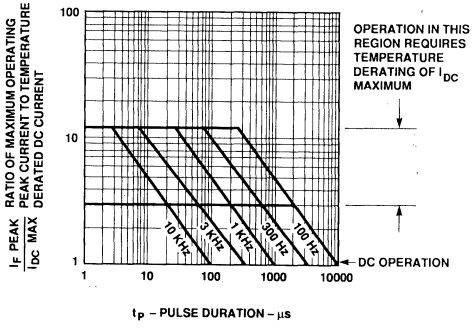


Figure 9. Maximum Tolerable Peak Current vs. Pulse Duration – Green.

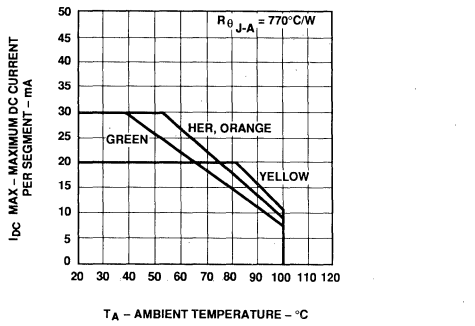


Figure 10. Maximum Allowable DC Current vs. Ambient Temperature.

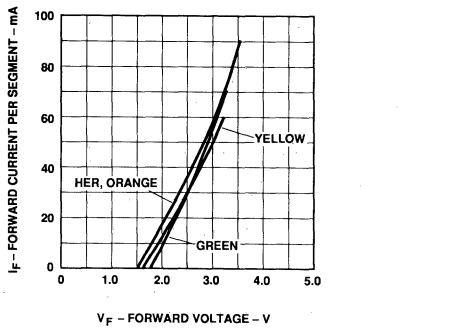


Figure 11. Forward Current vs. Forward Voltage Characteristics.

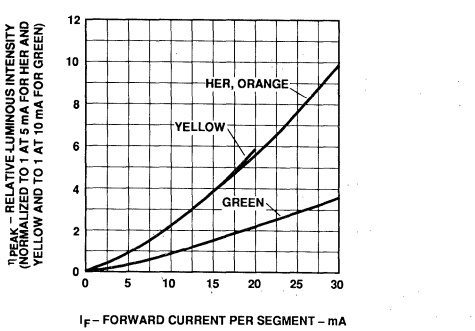


Figure 12. Relative Luminous Intensity vs. DC Forward Current.

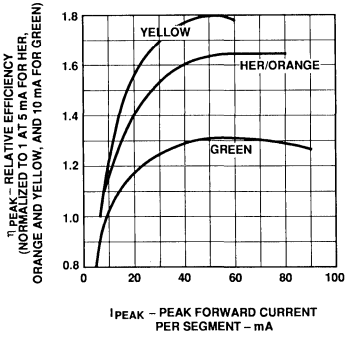


Figure 13. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Contrast Enhancement

For information on contrast enhancement please see Application Note 1015.

Soldering/Cleaning

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

For information on soldering LEDs please refer to Application Note 1027.

HEWLETT PACKARD

14.2 mm (0.56 inch) Seven Segment Displays

Technical Data

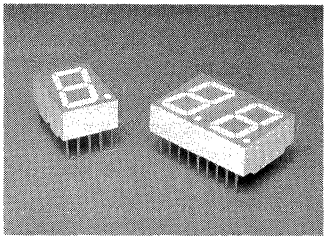
HDSP-530X Series
HDSP-532X Series
HDSP-550X Series
HDSP-552X Series
HDSP-560X Series
HDSP-562X Series
HDSP-570X Series
HDSP-572X Series
HDSP-H15X Series

Features

- **Industry Standard Size**
- **Industry Standard Pinout**
  15.24 mm (0.6 in.) DIP Leads on 2.54 mm (0.1 in.) Centers
- **Choice of Colors**
  Red, AlGaAs Red, High Efficiency Red, Yellow, Green
- **Excellent Appearance**
  Evenly Lighted Segments
  Mitered Corners on Segments
  Gray Package Gives Optimum Contrast
  ±50° Viewing Angle
- **Design Flexibility**
  Common Anode or Common Cathode
  Single and Dual Digits
  Right Hand Decimal Point
  ±1. Overflow Character
- **Categorized for Luminous Intensity**
  Yellow and Green Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **High Light Output**
- **High Peak Current**
- **Excellent for Long Digit String Multiplexing**
- **Intensity and Color Selection Option**
  See Intensity and Color Selected Displays Data Sheet
- **Sunlight Viewable AlGaAs**

Description

The 14.2 mm (0.56 inch) LED seven segment displays are designed for viewing distances up to 7 metres (23 feet). These devices use and industry standard size package and pinout. Both the numeric and ±1 overflow devices feature a right hand decimal point. All devices are available as either common anode or common cathode.



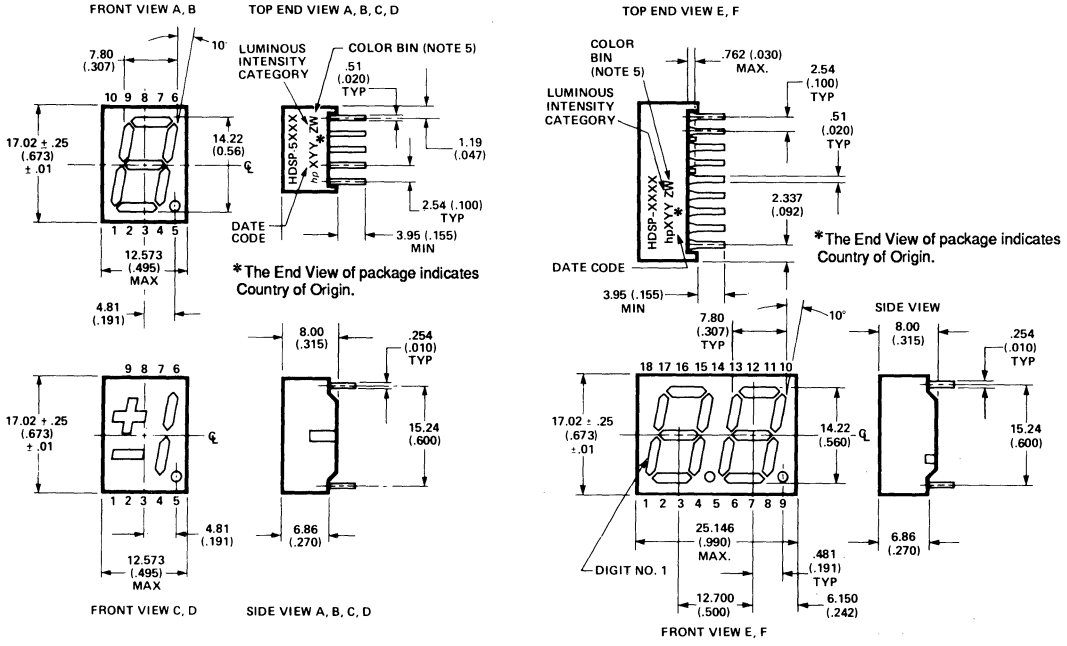
Devices

Red HDSP-	AlGaAs Red HDSP-[1]	HER HDSP-[1]	Yellow HDSP-	Green HDSP-	Description	Package Drawing
5301	H151	5501	5701	5601	Common Anode Right Hand Decimal	A
5303	H153	5503	5703	5603	Common Cathode Right Hand Decimal	B
5307	H157	5507	5707	5607	Common Anode ±1. Overflow	C
5308	H158	5508	5708	5608	Common Cathode ±1. Overflow	D
5321		5521	5721	5621	Two Digit Common Anode Right Hand Decimal	E
5323		5523	5723	5623	Two Digit Common Cathode Right Hand Decimal	F

Note:
1. These displays are recommended for high ambient light operation. Please refer to the HDSP-H10X/K12X AlGaAs and HDSP-555X HER data sheet for low current operation.

These displays are ideal for most applications. Pin for pin equivalent displays are also available in a low current design. The low current displays are ideal for portable applications. For additional information see the Low Current Seven Segment Displays data sheet.

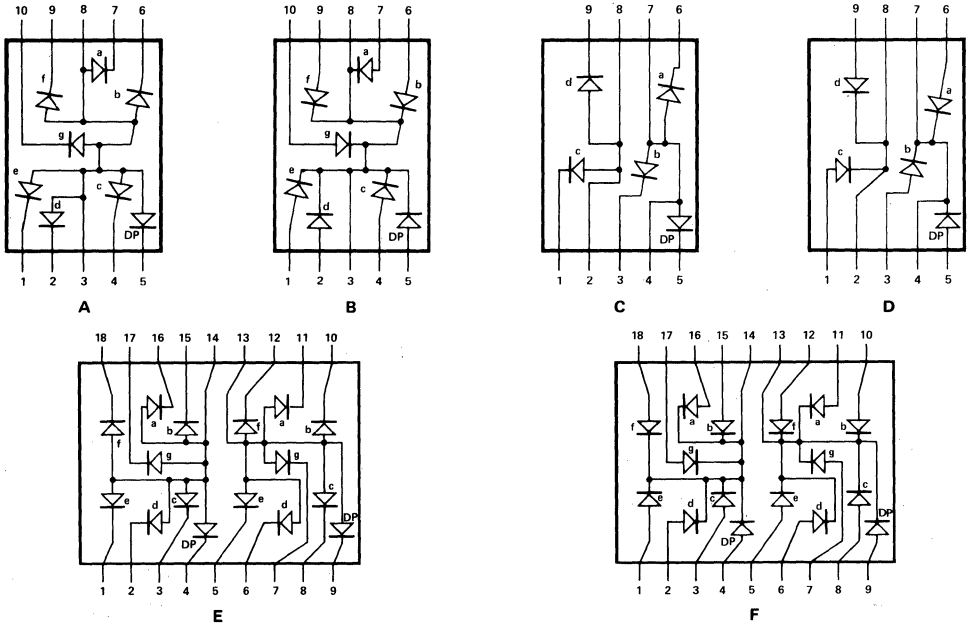
Package Dimensions



PIN	FUNCTION					
	A	B	C	D	E	F
1	CATHODE e	ANODE e	CATHODE c	ANODE c	E CATHODE NO. 1	E ANODE NO. 1
2	CATHODE d	ANODE d	ANODE c, d	CATHODE c, d	D CATHODE NO. 1	D ANODE NO. 1
3	ANODE[3]	CATHODE[4]	CATHODE b	ANODE b	C CATHODE NO. 1	C ANODE NO. 1
4	CATHODE c	ANODE c	ANODE a, b, DP	CATHODE a, b, DP	DP CATHODE NO. 1	DP ANODE NO. 1
5	CATHODE DP	ANODE DP	CATHOPDE DP	ANODE DE	E CATHODE NO. 1	E ANODE NO. 2
6	CATHODE b	ANODE b	CATHODE a	ANODE a	D CATHODE NO. 2	D ANODE NO. 2
7	CATHODE a	ANODE a	ANODE a, b, DP	CATHODE a, b, DP	G CATHODE NO. 2	G ANODE NO. 2
8	ANODE[3]	CATHODE[4]	ANODE c, d	CATHODE c, d	C CATHODE NO. 2	C ANODE NO. 2
9	CATHODE f	ANODE f	CATHODE d	ANODE d	DP CATHODE NO. 2	DP ANODE NO. 2
10	CATHODE g	ANODE g	NO PIN	NO PIN	B CATHODE NO. 2	B ANODE NO. 2
11					A CATHODE NO. 2	A ANODE NO. 2
12					F CATHODE NO. 2	F ANODE NO. 2
13					DIGIT NO. 2 ANODE	DIGIT NO. 2 CATHODE
14					DIGIT NO. 1 ANODE	DIGIT NO. 1 CATHODE
15					B CATHODE NO. 1	B ANODE NO. 1
16					A CATHODE NO. 1	A ANODE NO. 1
17					G CATHODE NO. 1	G ANODE NO. 1
18					F CATHODE NO. 1	F ANODE NO. 1

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. REDUNDANT ANODES.
4. REDUNDANT CATHODES.
5. FOR HDSP-5600/-5700 SERIES PRODUCT ONLY.

Internal Circuit Diagram



Absolute Maximum Ratings

Description	Red HDSP-5300 Series	AlGaAs Red HDSP-H150 Series	HER HDSP-5500 Series	Yellow HDSP-5700 Series	Green HDSP-5600 Series	Units
Average Power per Segment or DP	82	96	105	80	105	mW
Peak Forward Current per Segment or DP	150[1]	160[3]	90[5]	60[7]	90[9]	mA
DC Forward Current per Segment or DP	25[2]	40[4]	30[6]	20[8]	30[10]	mA
Operating Temperature Range	-40 to +100	-20 to +100[11]	-40 to +100			°C
Storage Temperature Range	-55 to +100					°C
Reverse Voltage per Segment or DP	3.0					V
Lead Solder Temperature for 3 Seconds (1.60 mm [0.063 in.] below seating plane)	260					°C

Notes:

1. See Figure 1 to establish pulsed conditions.
2. Derate above 80°C at 0.63 mA/°C.
3. See Figure 2 to establish pulsed conditions.
4. Derate above 46°C at 0.54 mA/°C.
5. See Figure 7 to establish pulsed conditions.
6. Derate above 53°C at 0.45 mA/°C.
7. See Figure 8 to establish pulsed conditions.
8. Derate above 81°C at 0.52 mA/°C.
9. See Figure 9 to establish pulsed conditions.
10. Derate above 39°C at 0.37 mA/°C.
11. For operation below -20°C, contact your local HP components sales office or an authorized distributor.

Electrical/Optical Characteristics at T_A = 25°C

Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
53XX	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	600	1300		µcd	I_F = 20 mA
				1400			I_F = 100 mA Peak: 1 of 5 df
	Forward Voltage/Segment or DP	V_F		1.6	2.0	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		655		nm	
	Dominant Wavelength[3]	λ_d		640		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	12		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		345		°C/W/ Seg	

AlGaAs Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
H15X	Luminous Intensity/Segment[1,2,5] (Digit Average)	I_V	9.1	16.0		mcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.8		V	I_F = 20 mA
				2.0	3.0		I_F = 100 mA
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		400		°C/W/ Seg	

High Efficiency Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
55XX	Luminous Intensity/Segment[1,2,6] (Digit Average)	I_V	900	2800		µcd	I_F = 10 mA
				3700			I_F = 60 mA Peak: 1 of 6 df
	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		345		°C/W/	

Yellow

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
57XX	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	600	1800		µcd	I_F = 10 mA
				2750			I_F = 60 mA Peak: 1 of 6 df
	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,7]	λ_d	581.5	586	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	40		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		345		°C/W/ Seg	

High Performance Green

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
56XX	Luminous Intensity/Segment[1,2] (Digit Average)`	I_V	900	2500		µcd	I_F = 10 mA
				3100			I_F = 60 mA Peak: 1 of 6 df
	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 10 mA
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,7]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		345		°C/W/ Seg	

Notes:
1. Device case temperature is 25°C prior to the intensity measurement.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. For low current operation, the AlGaAs HDSP-H10X series displays are recommended. They are tested at 1 mA dc/segment and are pin for pin compatible with the HDSP-H15X series.
6. For low current operation, the HER HDSP-555X series displays are recommended. They are tested at 2 mA dc/segment and are pin for pin compatible with the HDSP-550X series.
7. The Yellow (HDSP-5700) and Green (HDSP-5600) displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

Red, AlGaAs Red

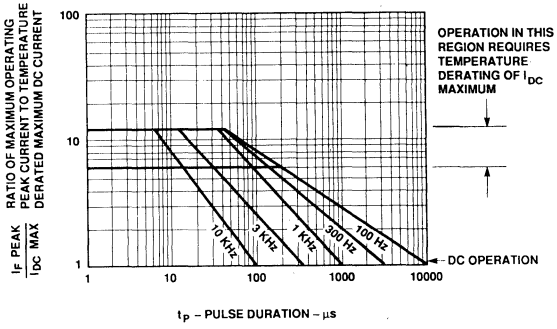


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration - Red.

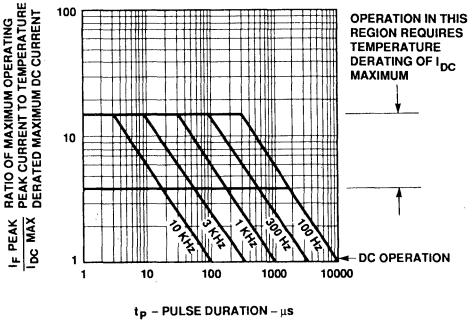


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration - AlGaAs Red.

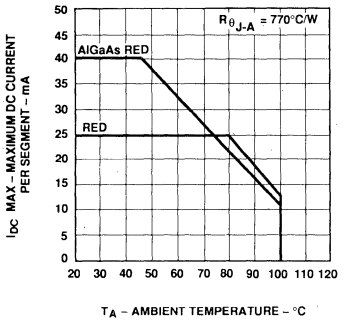


Figure 3. Maximum Allowable DC Current vs. Ambient Temperature.

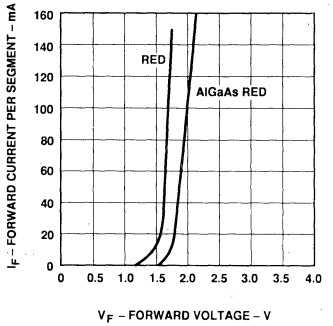


Figure 4. Forward Current vs. Forward Voltage.

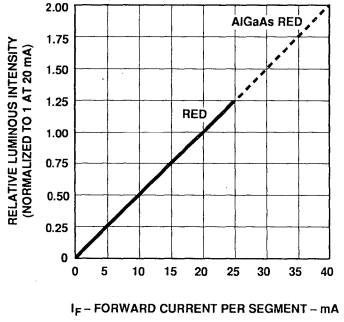


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

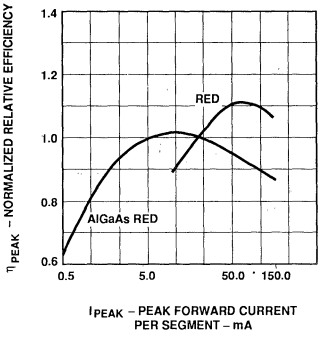


Figure 6. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Yellow, Green

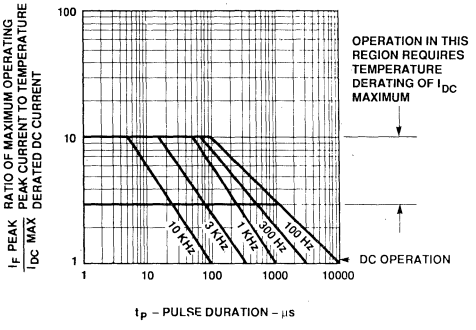


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration – HER.

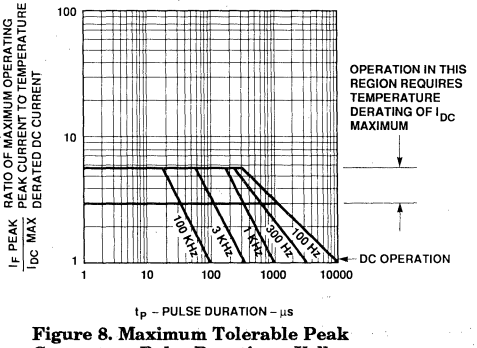


Figure 8. Maximum Tolerable Peak Current vs. Pulse Duration – Yellow.

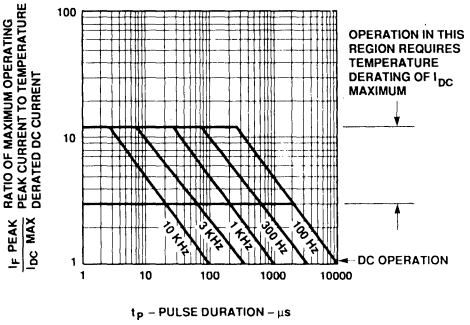


Figure 9. Maximum Tolerable Peak Current vs. Pulse Duration – Green.

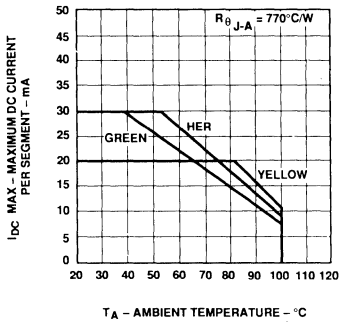


Figure 10. Maximum Allowable DC Current vs. Ambient Temperature.

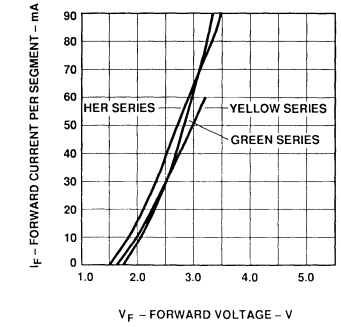


Figure 11. Forward Current vs. Forward Voltage.

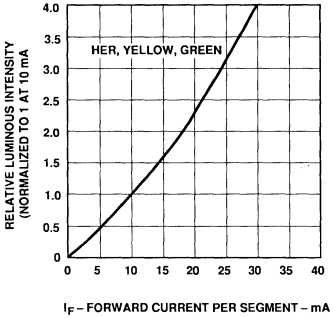


Figure 12. Relative Luminous Intensity vs. DC Forward Current.

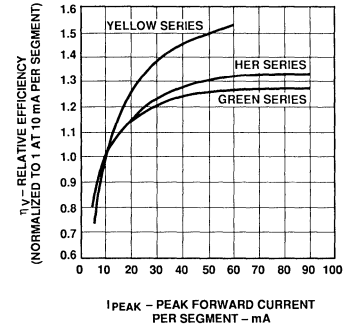


Figure 13. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Electrical/Optical

For more information on electrical/optical characteristics, please see Application Note 1005.

Contrast Enhancement

For information on contrast enhancement please see Application Note 1015.

Soldering/Cleaning

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloro–ethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

For information on soldering LEDs please refer to Application Note 1027.

HEWLETT PACKARD

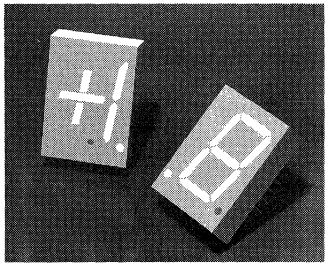
20 mm (0.8 inch) Seven Segment Displays

Technical Data

HDSP-340X Series
HDSP-390X Series
HDSP-420X Series
HDSP-860X Series
HDSP-N15X Series

Features

- **Industry Standard Size**
- **Industry Standard Pinout**
  15.24 mm (0.6 in.) DIP Leads on 2.54 mm (0.1 in.) Centers
- **Choice of Colors**
  Red, AlGaAs Red, High Efficiency Red, Yellow, Green
- **Excellent Appearance**
  Evenly Lighted Segments
  Mitered Corners on Segments
  Gray Package Gives Optimum Contrast
  ±50° Viewing Angle
- **Design Flexibility**
  Common Anode or Common Cathode
  Left and Right Hand Decimal Points
  ±1. Overflow Character
- **Categorized for Luminous Intensity**
  Yellow and Green
  Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **High Light Output**
- **High Peak Current**
- **Excellent for Long Digit String Multiplexing Intensity and Color Selection Option**
  See Intensity and Color Selected Displays Data Sheet
- **Sunlight Viewable AlGaAs**



Description

The 20 mm (0.8 inch) LED seven segment displays are designed for viewing distances up to 10 metres (33 feet). These devices use an industry standard size package and pinout. All devices are available as either common anode or common cathode.

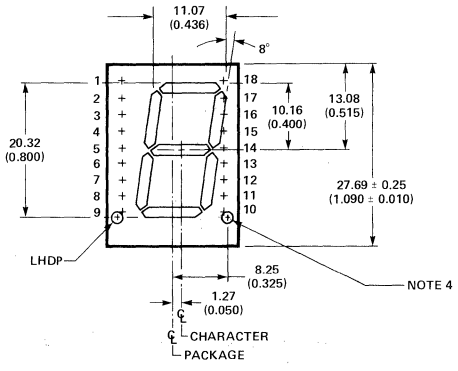
These displays are ideal for most applications. Pin for pin equivalent displays are also available in a low current design. The low current displays are ideal for portable applications. For additional information see the Low Current Seven Segment Displays data sheet.

Devices

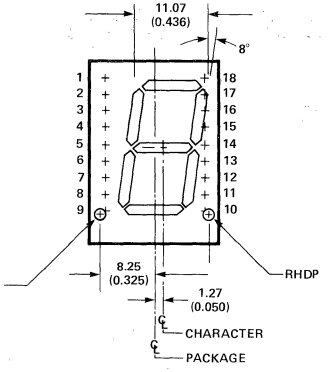
Red HDSP-	AlGaAs[1] HDSP-	HER HDSP-	Yellow HDSP-	Green HDSP-	Description	Package Drawing
3400	N150	3900	4200	8600	Common Anode Left Hand Decimal	A
3401	N151	3901	4201	8601	Common Anode Right Hand Decimal	B
3403	N153	3903	4203	8603	Common Cathode Right Hand Decimal	C
3405	N155	3905	4205	8605	Common Cathode Left Hand Decimal	D
3406	N156	3906	4206	8606	Universal ±1. Overflow[2]	E

Notes:
1. These displays are recommended for high ambient light operation. Please refer to the HDSP-N10X AlGaAs data sheet for low current operation.
2. Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram E.

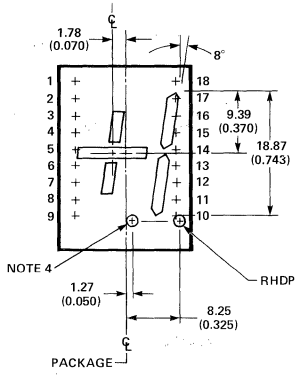
Package Dimensions



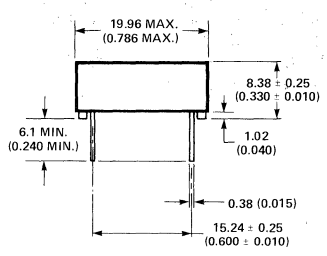
FRONT VIEW A, D



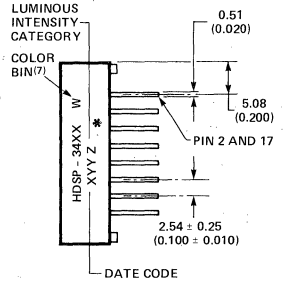
FRONT VIEW B, C



FRONT VIEW E



END VIEW



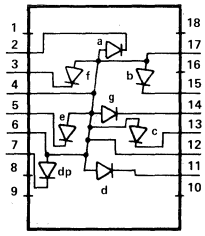
SIDE VIEW

*The Side View of package indicates Country of Origin.

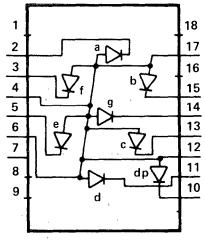
Pin	Function A	B	C	D	E
1	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
2	CATHODE a	CATHODE a	ANODE a	ANODE a	CATHODE a
3	CATHODE f	CATHODE f	ANODE f	ANODE f	ANODE d
4	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE d
5	CATHODE e	CATHODE e	ANODE e	ANODE e	CATHODE c
6	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE e
7	CATHODE dp	NO. CONNEC.	NO. CONNEC.	ANODE dp	ANODE e
8	NO PIN	NO PIN	NO PIN	NO PIN	CATHODE dp
9	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
10	NO PIN	CATHODE dp	ANODE dp	NO PIN	ANODE dp
11	CATHODE d	CATHODE d	ANODE d	ANODE d	CATHODE dp
12	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE b
13	CATHODE c	CATHODE c	ANODE c	ANODE c	ANODE b
14	CATHODE g	CATHODE g	ANODE g	ANODE g	ANODE c
15	CATHODE b	CATHODE b	ANODE b	ANODE b	ANODE a
16	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
17	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE a
18	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN

NOTES:
1. DIMENSIONS IN MILLIMETERS AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. REDUNDANT ANODES.
4. UNUSED dp POSITION.
5. SEE INTERNAL CIRCUIT DIAGRAM.
6. REDUNDANT CATHODES.
7. FOR HDSP-4200/-8600 SERIES PRODUCT ONLY.

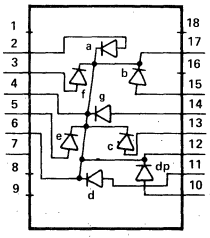
Internal Circuit Diagram



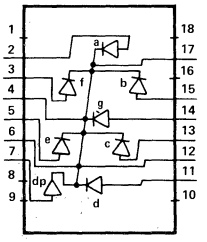
A



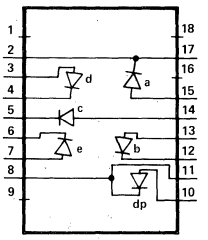
B



C



D



E

Absolute Maximum Ratings

Description	Red HDSP-3400 Series	AlGaAs Red HDSP-N150 Series	HER HDSP-3900 Series	Yellow HDSP-4200 Series	Green HDSP-8600 Series	Units
Average Power per Segment or DP	115	96	105	105	105	mW
Peak Forward Current per Segment or DP	200[1]	160[3]	135[5]	135[5]	90[7]	mA
DC Forward Current per Segment or DP	50[2]	40[4]	40[6]	40[6]	30[8]	mA
Operating Temperature Range	-40 to +100	-20 to +100	-40 to +100		-40 to +100	°C
Storage Temperature Range	-55 to +100					°C
Reverse Voltage per Segment or DP	3.0					V
Lead Solder Temperature for 3 Seconds (1.60 mm [0.063 in.] below seating plane)	260					°C

Notes:
1. See Figure 1 to establish pulsed conditions.
2. Derate above 45°C at 0.83 mA/°C.
3. See Figure 2 to establish pulsed conditions.
4. Derate above 55°C at 0.8 mA/°C.
5. See Figure 7 to establish pulsed conditions.
6. Derate above 50°C at 0.73 mA/°C.
7. See Figure 8 to establish pulsed conditions.
8. Derate above 50°C at 0.54 mA/°C.

Electrical/Optical Characteristics at T_A = 25°C

Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-340X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	500	1200		µcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.6	2.0	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		655		nm	
	Dominant Wavelength[3]	λ_d		640		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	20		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		375		°C/W	

AlGaAs Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-N15X	Luminous Intensity/Segment[1,2,5] (Digit Average)	I_V	6.0	14.0		mcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.8		V	I_F = 20 mA
				2.0	3.0	V	I_F = 100 mA
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		430		°C/W/ Seg	

High Efficiency Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-390X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	3350	7000		µcd	I_F = 100 mA Peak: 1 of 5 df
				4800		µcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.6	3.5	V	I_F = 100 mA
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	25		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		375		°C/W/ Seg	

Yellow

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-420X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	2200	7000		µcd	I_F = 100 mA Peak: 1 of 5 df
				3400		µcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.6	3.5	V	I_F = 100 mA
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,6]	λ_d	581.5	586	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	25.0		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		375		°C/W/ Seg	

Green

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-860X	Luminous Intensity/Segment[1,2] (Digit Average)`	I_V	680	1500		µcd	I_F = 10 mA
				1960		µcd	I_F = 50 mA Peak: 1 of 5 df
	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 10 mA
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,6]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50.0		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		375		°C/W/ Seg	

Notes:
1. Case temperature of the device immediately prior to the intensity measurement is 25°C.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. For low current operation, the AlGaAs Red HDSP-N100 series displays are recommended. They are tested at 1 mA dc/segment and are pin for pin compatible with the HDSP-N150 series.
6. The Yellow (HDSP-4200) and Green (HDSP-8600) displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

Red, AlGaAs Red

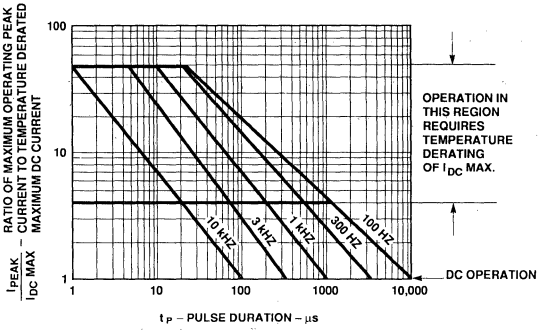


Figure 1. Maximum Allowable Peak Current vs. Pulse Duration – Red.

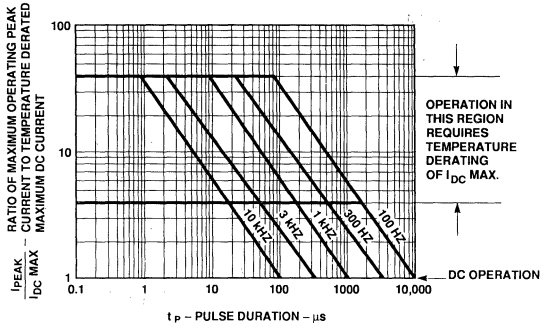


Figure 2. Maximum Allowed Peak Current vs. Pulse Duration – AlGaAs Red.

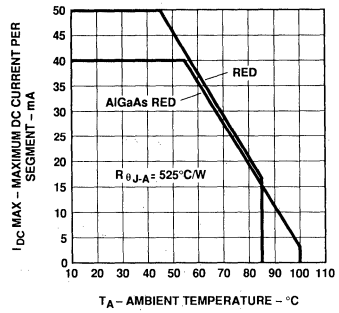


Figure 3. Maximum Allowable DC Current vs. Ambient Temperature.

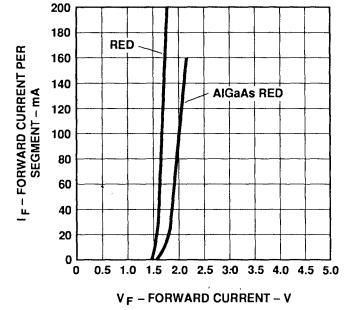


Figure 4. Forward Current vs. Forward Voltage.

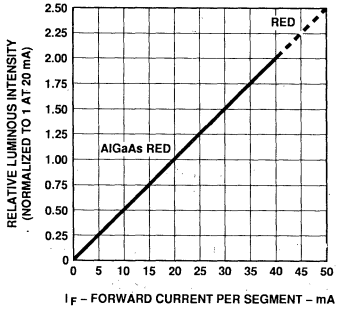


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

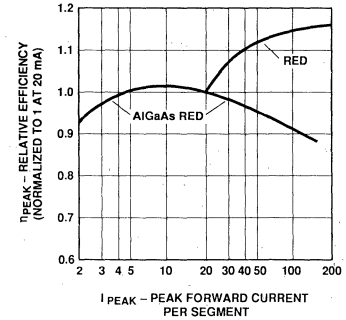


Figure 6. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Yellow, Green

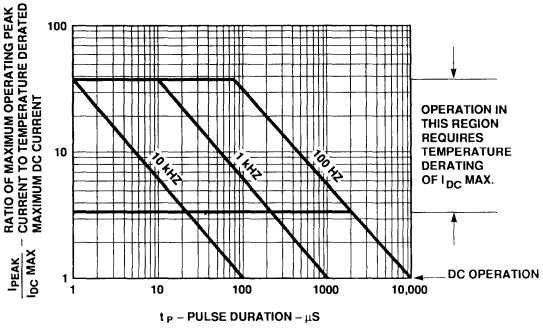


Figure 7. Maximum Allowed Peak Current vs. Pulse Duration – HER, Yellow.

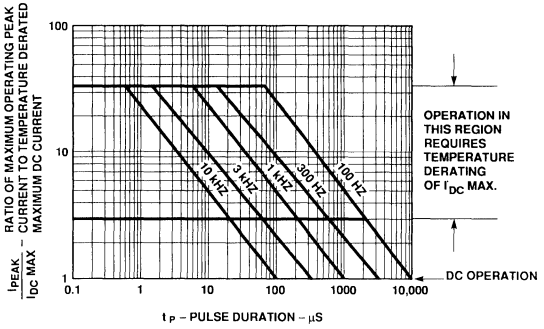


Figure 8. Maximum Allowed Peak Current vs. Pulse Duration – Green.

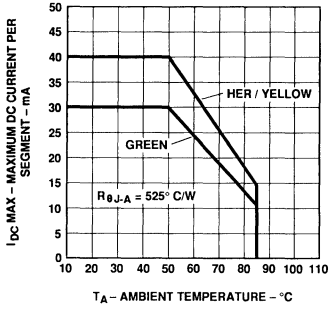


Figure 9. Maximum Allowable DC Current vs. Ambient Temperature.

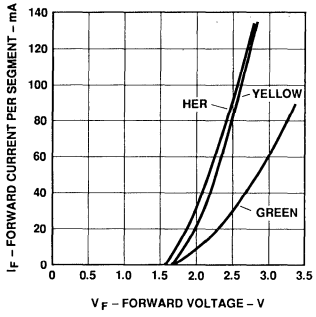


Figure 10. Forward Current vs. Forward Voltage.

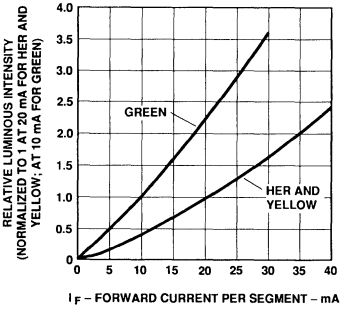


Figure 11. Relative Luminous Intensity vs. DC Forward Current.

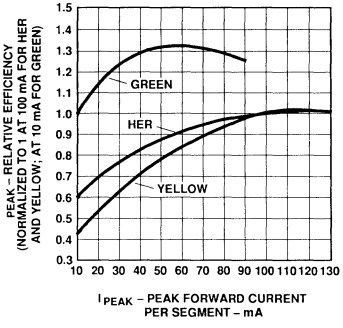


Figure 12. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Contrast Enhancement

For information on contrast enhancement please see Application Note 1015.

Soldering/Cleaning

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

For further information on soldering LEDs please refer to Application Note 1027.

HEWLETT PACKARD

New

CMOS 5x7 Small Alphanumeric Displays

Technical Data

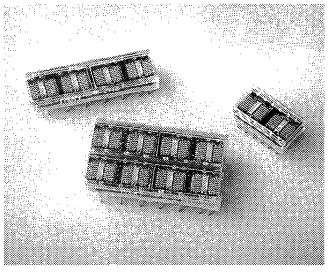
HCMS-270X Series
HCMS-271X Series
HCMS-272X Series

Features

- **On-Board Low Power CMOS ICs**
  Integrated Shift Registers with Constant Current LED Drivers
- **Wide Operating Temperature Range**
  -40°C to +85°C
- **Three Package Styles**
  1 Row of 4 Characters
  1 Row of 8 Characters
  2 Rows of 8 Characters
- **Five LED Colors**
  Standard Red
  High Efficiency Red
  Orange
  Yellow
  High Performance Green
- **5x7 LED Matrix**
  Displays Full ASCII Character Set
- **Character Height**
  3.8 mm (0.15 inch)
- **Long Viewing Distance**
  2.6 Metres (8.6 Feet)
- **Wide Viewing Angle**
  X Axis = ±30°
  Y Axis = ±55°
- **Categorized for Luminous Intensity**
- **Categorized for Color**
  HCMS-2701/-2703
  HCMS-2711/-2713
  HCMS-2721/-2723

Typical Applications

- **Telecommunications Equipment**
- **Instrumentation**
- **Medical Instruments**
- **Business Machines**



Device Selection Guide

Part Number	Display Package Style	LED Color
HCMS-2700 -2701 -2702 -2703 -2704	1 Row of 4 Characters	Standard Red Yellow HER Green Orange
HCMS-2710 -2711 -2712 -2713 -2714	1 Row of 8 Characters	Standard Red Yellow HER Green Orange
HCMS-2720 -2721 -2722 -2723 -2724	2 Rows of 8 Characters	Standard Red Yellow HER Green Orange

Description

The HCMS-270X series are four character 5x7 dot matrix alphanumeric displays in a dual in-line 12 pin plastic package. The on-board CMOS ICs form a 28 bit shift register.

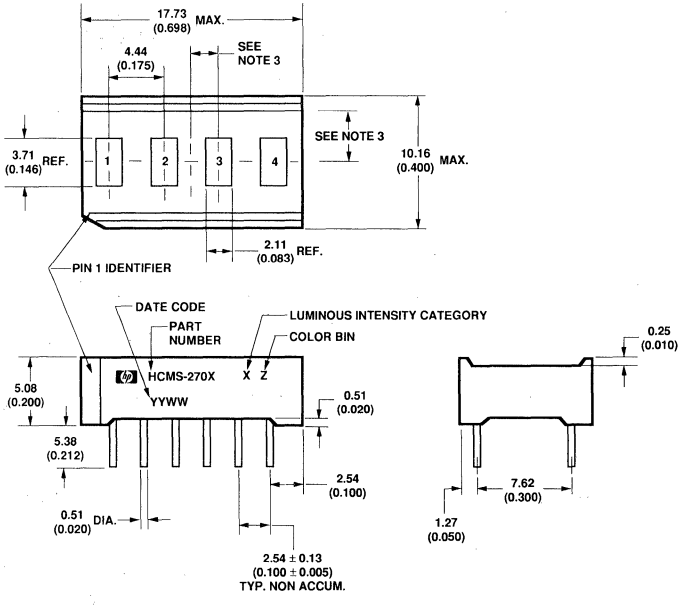
The HCMS-271X series are eight character 5x7 dot matrix alphanumeric displays in a dual in-line plastic package with 26 pin positions. The on-board CMOS ICs form a 56 bit shift register.

The HCMS-272X series are sixteen character 5x7 dot matrix alphanumeric displays. Each device is assembled by enclosing two HCMS-271X devices in a common lens assembly forming two rows of eight characters. The plastic package has two dual in-line rows of 26 pin positions for a total of 52 pin positions. The two on-board CMOS IC 56 bit shift registers for each row are electrically separate from each other.

The on-board CMOS ICs form serial input shift registers with constant current output LED row drivers. Decoded column data is clocked into the shift registers for each refresh cycle. Full character display is accomplished with external column strobing at a refresh rate of 100 Hz or faster.

All of these display devices may be end stacked in the X-direction to form a string of characters of desired length.

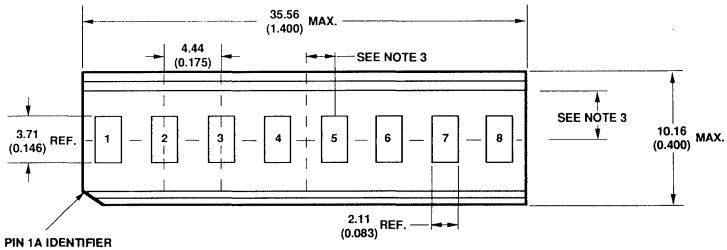
Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{DD}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

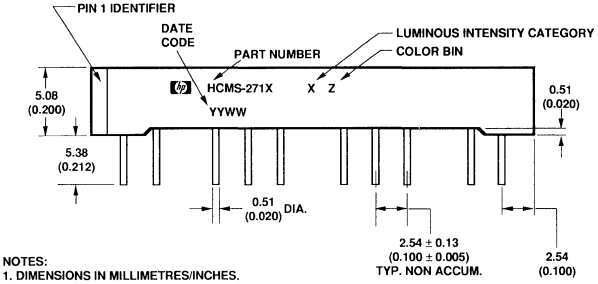
*DO NOT CONNECT OR USE.

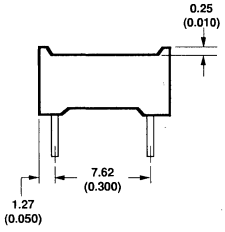
NOTES:
1. DIMENSIONS IN MILLIMETRES/INCHES.
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS 0.38MM (0.015").
3. CHARACTERS ARE CENTERED WITH RESPECT TO LEAD WITHIN 0.13MM (0.005").
4. LEAD MATERIAL: SOLDER PLATED COPPER ALLOY.



PIN	FUNCTION	PIN	FUNCTION
1	NO PIN	14	DATA OUT
2	COLUMN 2	15	$V_{B(5-8)}$
3	NO PIN	16	NO PIN
4	COLUMN 4	17	CLOCK
5	NO PIN	18	GROUND
6	INT. CONNECT*	19	NO PIN
7	NO PIN	20	NO PIN
8	COLUMN 1	21	INT. CONNECT*
9	NO PIN	22	$V_{B(1-4)}$
10	COLUMN 3	23	V_{DD}
11	NO PIN	24	NO PIN
12	COLUMN 5	25	GROUND
13	INT. CONNECT*	26	DATA IN

*DO NOT CONNECT OR USE.



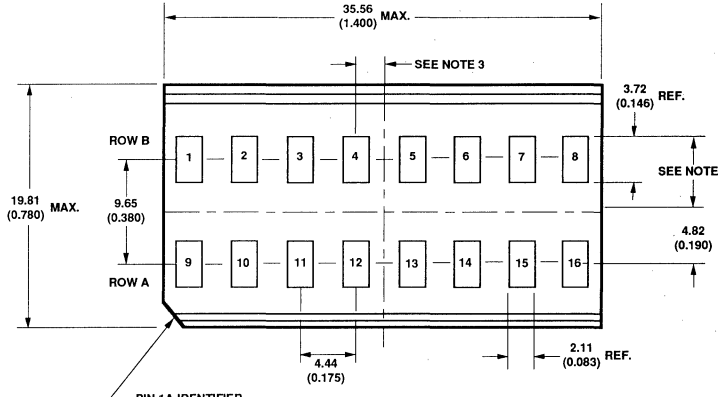


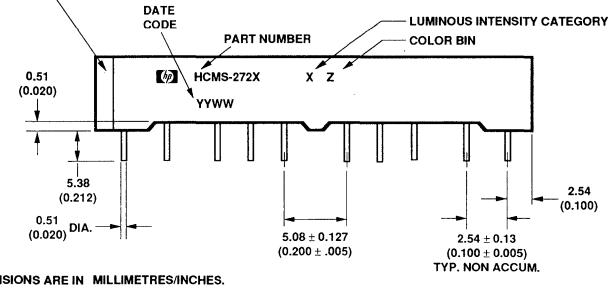
NOTES:
1. DIMENSIONS IN MILLIMETRES/INCHES.
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS 0.38MM (0.015").
3. CHARACTERS ARE CENTERED WITH RESPECT TO LEAD WITHIN 0.13MM (0.005").
4. LEAD MATERIAL: SOLDER PLATED COPPER ALLOY.

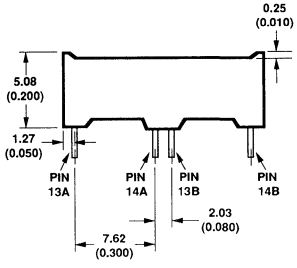
HCMS-271X

PIN	ROW A FUNCTION	PIN	ROW B FUNCTION
1A	NO PIN	1B	NO PIN
2A	COLUMN 2	2B	COLUMN 2
3A	NO PIN	3B	NO PIN
4A	COLUMN 4	4B	COLUMN 4
5A	NO PIN	5B	NO PIN
6A	INT. CONNECT*	6B	INT. CONNECT*
7A	NO PIN	7B	NO PIN
8A	COLUMN 1	8B	COLUMN 1
9A	NO PIN	9B	NO PIN
10A	COLUMN 3	10B	COLUMN 3
11A	NO PIN	11B	NO PIN
12A	COLUMN 5	12B	COLUMN 5
13A	INT. CONNECT*	13B	INT. CONNECT*
14A	DATA OUT	14B	DATA OUT
15A	$V_{B(13-16)}$	15B	$V_{B(5-8)}$
16A	NO PIN	16B	NO PIN
17A	CLOCK	17B	CLOCK
18A	GROUND	18B	GROUND
19A	NO PIN	19B	NO PIN
20A	NO PIN	20B	NO PIN
21A	INT. CONNECT*	21B	INT. CONNECT*
22A	$V_{B(9-12)}$	22B	$V_{B(1-4)}$
23A	V_{DD}	23B	V_{DD}
24A	NO PIN	24B	NO PIN
25A	GROUND	25B	GROUND
26A	DATA IN	26B	DATA IN

*DO NOT CONNECT OR USE INTERNAL CONNECTION PINS.







NOTES:
1. DIMENSIONS ARE IN MILLIMETRES/INCHES.
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE IS ± 0.38MM (0.015").
3. CHARACTERS ARE POSITIONED WITH RESPECT TO LEADS WITHIN ±0.13MM (0.005").
4. LEAD MATERIAL IS SOLDER PLATED COPPER ALLOY.

HCMS-272X

Absolute Maximum Ratings

Supply Voltage V_{DD} to Ground . . . . . -0.3 V to 7.0 V
Data Input, Clock, Data Output, V_B . . . . . -0.3 V to V_{DD}
Column Input Voltage, V_{COL} . . . . . -0.3 V to V_{DD}
Free Air Operating Temperature, T_A . . . . . -40°C to +85°C
Storage Temperature, T_S . . . . . -55°C to +100°C
Maximum Allowable Package Power Dissipation, P_D at 55°C[1,2]
HCMS-270X . . . . . 0.837 W
HCMS-271X . . . . . 1.674 W
HCMS-272X (per 8 character row) . . . . . 1.674 W
(total per package . . . . . 3.348 W)
Maximum Solder Temperature
1.59 mm (0.063") Below Seating Plane, t<5sec . . . . . 260°C
ESD Protection @ 1.5 kΩ, 100 pF . . . . . V_Z = 4 kV (each pin)

Notes:
1. Maximum allowable power dissipation is derived from V_{DD} = 5.25 V and V_B = 2.4 V, V_{COL} = 3.5 V, 20 LEDs illuminated per character, 20% on-time duty factor.
2. See Figure 1 for power derating. Thermal resistance from device V_{DD} pin(s) to ambient through the PC board mounting assembly is assumed to be $R\theta_{PC\text{-}A} \leq 35°C/W$ per device for the HSMS-270X, ≤17.5°C/W per device for the HCMS-271X, and ≤17.5°C/W per row for the HCMS-272X.

Recommended Operating Conditions, T_A = -40°C to +85°C

Description	Symbol	Minimum	Nominal	Maximum	Unit
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Data Out Current, Low State	I_{OL}			1.6	mA
Data Out Current, High State	I_{OH}			-0.5	mA
Column Input Voltage	V_{COL}	2.75	3.0	3.5	V
Setup Time	t_{SETUP}	10			ns
Hold Time	t_{HOLD}	25			ns
Clock Pulse Width High	$t_{WH(CLOCK)}$	50			ns
Clock Pulse Width Low	$t_{WL(CLOCK)}$	50			ns
Clock High to Low Transition	t_{THL}			200	ns
Clock Frequency	f_{CLOCK}			5	MHz

Electrical Characteristics, -40°C to +85°C

Parameter	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit
Supply Current, Dynamic [2]		V_{DD} = 5.25 V				
HCMS-270X	I_{DDD}	f_{CLOCK} = 5 MHz		6.2	7.8	
HCMS-271X		V_B = 0.4 V		12.4	15.6	mA
HCMS-272X (per row)				15.6	15.6	
Supply Current, Static [3]						
HCMS-270X		V_{DD} = 5.25 V		1.8	2.6	
HCMS-271X	I_{DDSoff}	V_B = 0.4 V		3.6	5.2	
HCMS-272X (per row)				3.6	5.2	mA
HCMS-270X		V_{DD} = 5.25 V		2.2	3.3	
HCMS-271X	I_{DDSon}	V_B = 2.4 V		4.4	6.6	
HCMS-272X (per row)				4.4	6.6	
Column Input Current		V_{DD} = 5.25				
HCMS-270X		V_{COL} = 3.5 V		335	410	
HCMS-271X	I_{COL}	V_B = 2.4 V		670	820	mA
HCMS-272X (per row)				670	820	
Input Logic High:						
Data,V_B, Clock	V_{IH}	V_{DD} = 4.75 V	2.0			V
Input Logic Low:						
Data,V_B, Clock	V_{IL}	V_{DD} = 5.25 V			0.8	V
Input Current:		V_{DD} = 5.25 V				
Data		0<V_I<5.25 V	-10		+1	
Clock						
HCMS-270X			-10			μA
HCMS-271X	I_I	V_{DD} = 5.25 V	-20		+1	
HCMS-272X (per row)		0<V_I<5.25 V	-20			
V_B						
HCMS-270X			-40			
HCMS-271X		V_{DD} = 5.25 V	-80		0	
HCMS-272X (per row)		0<V_B<5.25 V	-80			
		V_{DD} = 4.75 V				
	V_{OH}	I_{OH} = -0.5 mA	2.4	4.2		
Data Out Voltage		I_{COL} = 0 mA				V
		V_{DD} = 5.25 V				
	V_{OL}	I_{OH} = 1.6 mA		0.2	0.4	
		I_{COL} = 0 mA				

Electrical Characteristics, -40°C to +85°C (Continued)

Parameter	Symbol	Test Conditions	Minimum	Typical[1]	Maximum	Unit
Power Dissipation [4] Per Package		V_{DD} = 5.0 V V_{COL} = 3.5 V 17.5% DF				
HCMS-270X	P_D	V_B = 2.4 V		451		mW
HCMS-271X		15 LEDs ON		902		
HCMS-272X (per row)		Per Character		902		
Thermal Resistance [5] IC Junction-to-Pin(V_{DD})						
HCMS-270X	$R\theta_{J\text{-}PIN}$			50		°C/W
HCMS-271X				25		
HCMS-272X (per row)				25		

Notes:

1. All typical values at V_{DD} = 5.0 volts, T_A = 25°C.
2. I_{DD} Dynamic is the IC current while clocking column data through the on-board shift register at a clock frequency of 5 MHz.
3. I_{DD} Static is the IC current after column data is loaded and not being clocked through the on-board shift register.
4. Four, eight, or sixteen characters are illuminated with a typical ASCII character composed of 15 dots per character.
5. The IC junction temperature T_J(IC), is:

$T_J(IC) = (P_D)(R\theta_{J\text{-}PIN} + R\theta_{PC\text{-}A}) + T_A$

Where: P_D is the total power into the display for HCMS-270X and HCMS-271X, and the total power into one row of an HCMS-272X display.

$P_D = P(I_{DDSon}) + P(I_{COL})$

$P(I_{DDSon}) = I_{DDSon} * V_{DD}$

$P(I_{COL}) = 5 * I_{COL} * V_{COL} * n/35 * DF$

n = Quantity of LED dots illuminated per character.

DF = LED on-time duty factor.

The IC junction temperature rise above the temperature of the V_{DD} pin(s), ΔT_J(IC), is:

$\Delta T_J(IC) = (P_D)(R\theta_{J\text{-}PIN})$

The IC junction temperatuire, T_J(IC), should not exceed +125°C.

Optical Characteristics at T_A = 25°C

Standard Red HCMS-2700/-2710/-2720

Description	Test Conditions	Symbol	Min.	Typ.	Unit
Peak Luminous Intensity per LED (Digit average)[1,5]	V_{DD} = 5.0 V, V_{COL} = 3.5 V V_B = 2.4 V, T_j = 25°C [3]	I_v	105	200	µcd
Dominant Wavelength[4]		λ_d		640	nm
Peak Wavelength		λ_{PEAK}		655	nm

Yellow HCMS-2701/-2711/-2721

Description	Test Conditions	Symbol	Min.	Typ.	Unit
Peak Luminous Intensity per LED (Digit average)[1,5]	V_{DD} = 5.0 V, V_{COL} = 3.5 V, V_B = 2.4 V, T_j = 25°C [3]	I_v	400	750	µcd
Dominant Wavelength[2,4]		λ_d		585	nm
Peak Wavelength		λ_{PEAK}		583	nm

High Efficiency Red HCMS-2702/-2712/-2722

Description	Test Conditions	Symbol	Min.	Typ.	Unit
Peak Luminous Intensity per LED (Digit average)[1,5]	V_{DD} = 5.0 V, V_{COL} = 3.5 V, V_B = 2.4 V, T_j = 25°C [3]	I_v	400	1430	µcd
Dominant Wavelength[4]		λ_d		626	nm
Peak Wavelength		λ_{PEAK}		635	nm

High Performance Green HCMS-2703/-2713/-2723

Description	Test Conditions	Symbol	Min.	Typ.	Unit
Peak Luminous Intensity per LED (Digit average)[1,5]	V_{DD} = 5.0 V, V_{COL} = 3.5 V, V_B = 2.4 V, T_j = 25°C [3]	I_v	400	1550	µcd
Dominant Wavelength[2,4]		λ_d		574	nm
Peak Wavelength		λ_{PEAK}		568	nm

Orange HCMS-2704/-2714/-2724

Description	Test Conditions	Symbol	Min.	Typ.	Unit
Peak Luminous Intensity per LED (Digit average)[1,5]	V_{DD} = 5.0 V, V_{COL} = 3.5 V, V_B = 2.4 V, T_j = 25°C [3]	I_v	400	1400	µcd
Dominant Wavelength[4]		λ_d		602	nm
Peak Wavelength		λ_{PEAK}		600	nm

Notes:

1. These displays are categorized for luminous intensity with the intensity category designated by a letter code located on the side of the display package.
2. Yellow and high performance green devices are categorized for color with the color category designated by a number code on the side of the display package.
3. T_j refers to the initial device temperature immediately prior to the light measurement.
4. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the LED color.
5. The luminous sterance of the individual LED pixels may be calculated using the following equations:

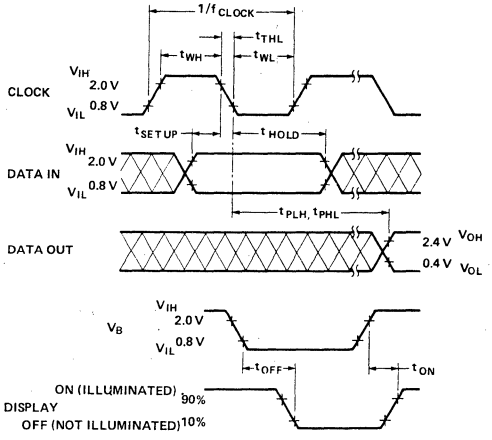
$L_v(cd/m^2) = I_v(Candela)*DF/A(Meter^2)$

$L_v(Footlamberts) = \pi I_v(Candela)*DF/A(Foot^2)$

Where: A = LED pixel area = $3.32x10^{-8}$ m^2 or $3.57x10^{-7}$ ft^2

DF = LED on-time duty factor.

Switching Characteristics, T_A = -40°C to +85°C



Parameter	Condition	Typ.	Max.	Units
f_{CLOCK} CLOCK Rate			5	MHz
t_{PLH}, t_{PHL} Propagation Delay CLOCK to DATA OUT	C_L = 15 pF R_L = 2.4 kΩ		105	ns
t_{OFF} V_B (0.4 V) to Display OFF		4	5	µs
t_{ON} V_B (2.4 V) to Display ON		1	2	

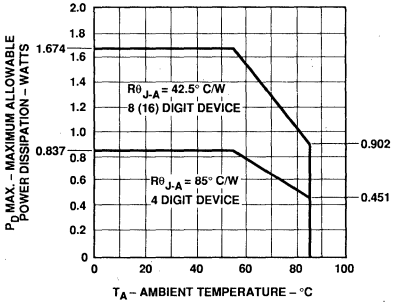


Figure 1. Maximum Allowable Power Dissipation vs. Ambient Temperature as a Function of Thermal Resistance IC Junction-to-Ambient, $R\theta_{J-A}$. Operation at 85°C Assumes a Thermal Resistance for the Printed Circuit Board of $R\theta_{PC-A}$ = 35°C/W per Device for the HCMS-270X, 17.5°C/W Per Device for the HCMS-271X , and 17.5°C/W per Row for the HCMS-272X. T_J(IC)MAX =125 °C.

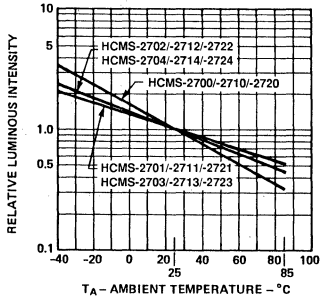


Figure 2. Relative Luminous Intensity vs. Display Pin Temperature.

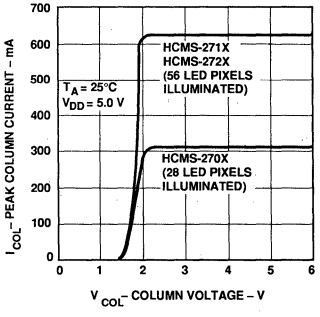


Figure 3. Peak Column Current vs. Column Voltage.

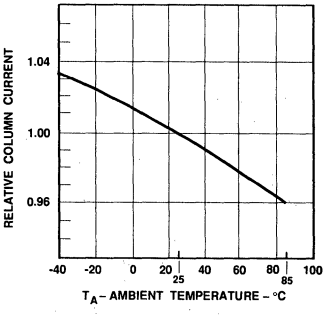


Figure 4. Relative Column Current, I_{COL}, vs. Ambient Temperature.

Electrical Description

Each display device contains four or eight 5x7 LED dot matrix characters and two or four CMOS integrated circuits, as shown in Figure 5. The CMOS integrated circuits form an on-board 28 bit or 56 bit serial-in-parallel-out shift register that will accept standard TTL logic levels. The Data Input pin is connected to bit position 1 and the Data Output pin is connected to bit position 28 (56). The shift register outputs control constant current sinking LED row drivers. The nominal current sink per LED driver is 11 mA. A logic 1 stored in the shift register enables the corresponding LED row driver and a logic 0 stored in the shift register disables the corresponding LED row driver.

The electrical configuration of these CMOS IC alphanumeric displays allows for an effective interface to a display controller circuit that supplies decoded character information. The row data for a given column (one 7 bit byte per character) is loaded (bit serial) into the on-board 28 (56) bit shift register with high to low transitions of the Clock input. To load decoded character information into the display, column data for character 4 (8) is loaded first and the column data for character 1 is loaded last in the following manner. The 7 data bits for column 1, character 4 (8), are loaded into the on-board shift register. Next, the 7 data bits for column 1, character 3 (7), are loaded into the shift register, shifting the character 4 (8) data bits over one character position. This process is repeated for the other 2 (6) characters until all 28 (56) bits of column data (four or eight 7 bit bytes of character column data) are loaded into the on-board shift register. Then the column 1 input, V_{COL}, pin 1, is energized to illuminate column 1 in all 4 (8) characters. This process is repeated for columns 2, 3, 4, and 5. All of the V_{COL} inputs should be at logic low to insure the display is off when loading data. The display will be blanked when the blanking input V_B is at logic low

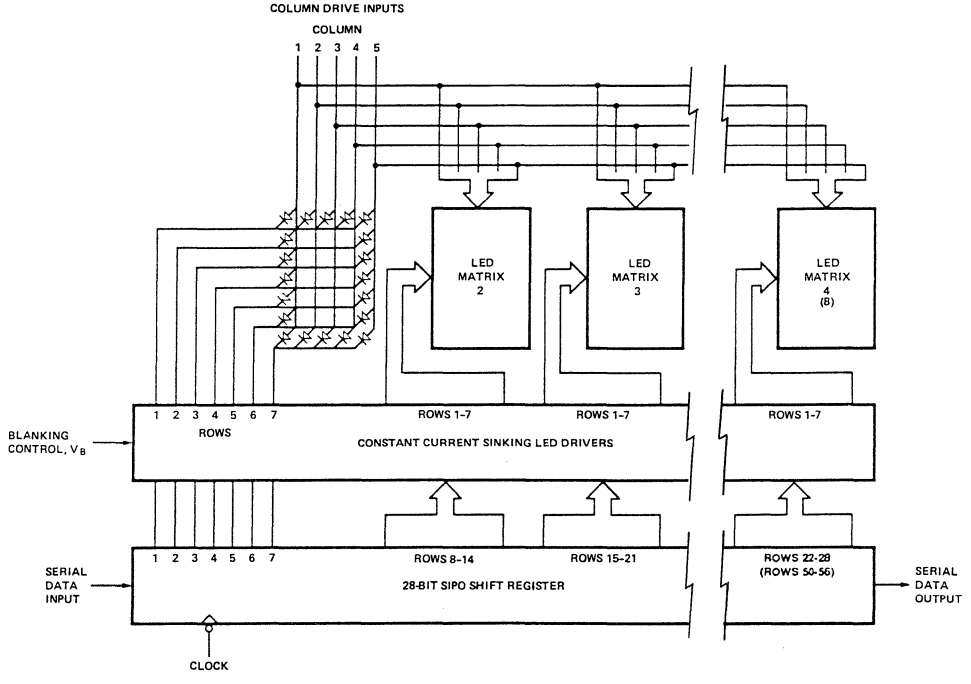


Figure 5. Block Diagram of an HCMS-27XX Series LED Alphanumeric Display.

regardless of the outputs of the shift registers or whether one of the V_{COL} inputs is energized.

Refer to Application Note 1016 *Using the HDSP-2000 Alphanumeric Display Family* for drive circuit information.

ESD Susceptibility

The HCMS-27XX series displays have an ESD susceptibility ratings of CLASS 3 per DOD-STD-1686 and CLASS B per MIL-STD-883C. It is recommended that normal CMOS handling precautions be observed with these devices.

Soldering and Post Solder Cleaning

These displays may be wave soldered using either an RMA rosin based flux and terpene solvent semi-aqueous cleaning or with an OA flux and aqueous cleaning. For optimum soldering, the solder wave temperature should be 245°C and the dwell time should be 1 1/2 to 2 seconds for any lead passing through the wave. For terpene semi-aqueous cleaning, the terpene solvent should be used in concentrate form. The water rinse should be 49°C (120°F). For aqueous cleaning, a water temperature of 60°C (140°F) with an immersion time not exceeding 15 minutes is recommended. For solvent cleaning, Genesolv DES is recommended. For more detailed information, refer to Application Note 1027*Soldering LED Components* and AN 1027 Supplement *Post Solder Cleaning LEDs with BIOACT EC-7R Terpene Based Defuxer.*

Contrast Enhancement

When used with the proper contrast enhancement filters, the HCMS-27XX series displays are readable in bright ambients. For information on contrast enhancement, refer to Application Note 1015 *Contrast Enhancement Techniques for LED Displays* and Application Note 1029 *Luminous Contrast and Sunlight Readability of the HDSP-238X Series Alphanumeric Displays for Military Applications.*

HEWLETT PACKARD

New

High Performance CMOS 5X7 Alphanumeric Displays

Technical Data

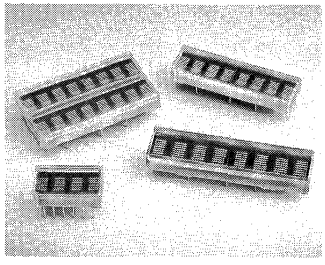
HCMS-29XX Series

Features

- **Easy to Use**
- **Interfaces Directly with Microprocessor**
- **0.15" Character Height in 4, 8, and 16 (2x8) Character Packages**
- **0.20" Character Height in 4 and 8 Character Packages**
- **Rugged X- and Y-Stackable Package**
- **Serial Input**
- **Convenient Brightness Controls**
- **Wave Solderable**
- **Offered in Five Colors**
- **Low Power CMOS Technology**
- **TTL Compatible**

Description

The HCMS-29XX series are high performance, easy to use dot matrix displays driven by on-board CMOS ICs. Each display can be directly interfaced with a microprocessor, thus eliminating the need for cumbersome interface components. The serial IC interface allows higher character count information displays with a minimum of data lines. A variety of colors, font heights, and character counts gives designers a wide range of product choices for their specific applications and the easy to read 5 x 7 pixel format allows the display of uppercase, lower case, Katakana, and custom user-defined characters. These displays are stackable in the x- and y-directions, making them ideal for high character count displays.



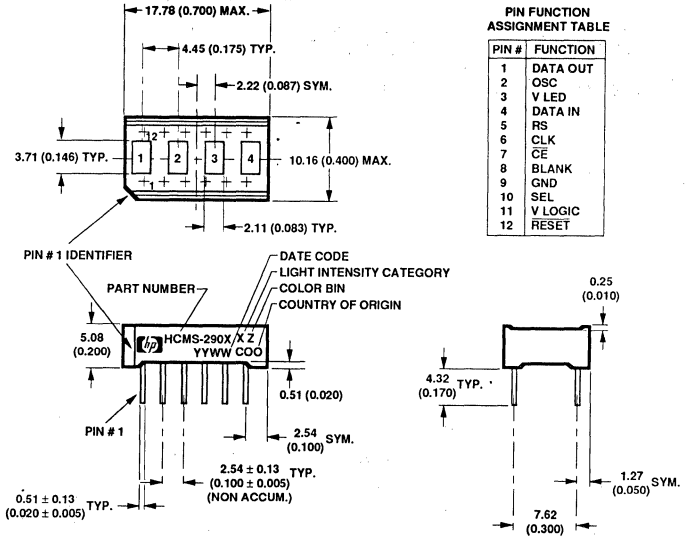
Applications

- **Telecommunications Equipment**
- **Portable Data Entry Devices**
- **Computer Peripherals**
- **Medical Equipment**
- **Test Equipment**
- **Business Machines**
- **Avionics**
- **Industrial Controls**

Device Selection Guide

Description	AlGaAs HCMS-	HER HCMS-	Orange HCMS-	Yellow HCMS-	Green HCMS-	Package Drawing
1 x 4 0.15" Character	2905	2902	2904	2901	2903	A
1 x 8 0.15" Character	2915	2912	2914	2911	2913	B
2 x 8 0.15" Character	2925	2922	2924	2921	2923	C
1 x 4 0.20" Character	2965	2962	2964	2961	2963	D
1 x 8 0.20" Character	2975	2972	2974	2971	2973	E

ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED TO AVOID STATIC DISCHARGE.

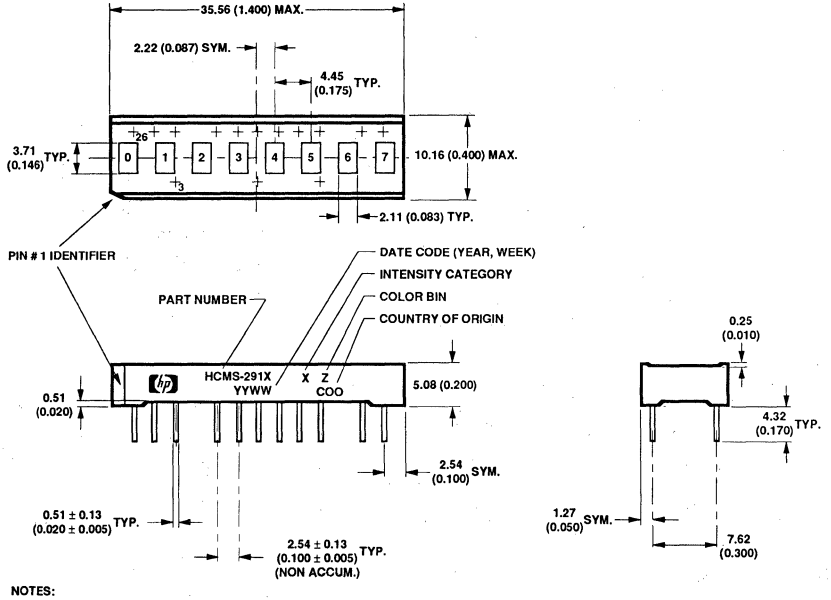


PIN FUNCTION ASSIGNMENT TABLE

PIN #	FUNCTION
1	DATA OUT
2	OSC
3	V LED
4	DATA IN
5	RS
6	CLK
7	$\overline{CE}$
8	BLANK
9	GND
10	SEL
11	V LOGIC
12	$\overline{RESET}$

NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE ON DIMENSIONS IS ± 0.38 mm (0.015 INCH).
3. LEAD MATERIAL: SOLDER PLATED COPPER ALLOY.

HCMS-290X

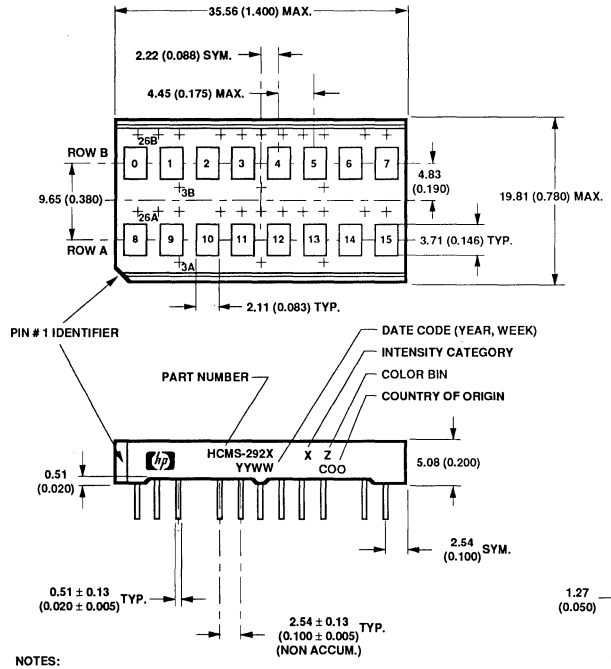


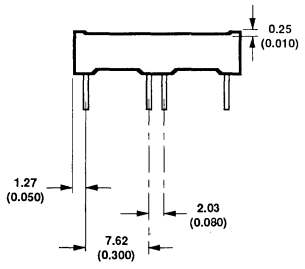
PIN FUNCTION ASSIGNMENT TABLE

PIN #	FUNCTION
1	NO PIN
2	NO PIN
3	V LED
4	NO PIN
5	NO PIN
6	NO PIN
7	GND LED
8	NO PIN
9	NO PIN
10	V LED
11	NO PIN
12	NO PIN
13	NO PIN
14	DATA IN
15	RS
16	NO PIN
17	CLOCK
18	$\overline{CE}$
19	BLANK
20	GND LOGIC
21	SEL
22	V LOGIC
23	NO PIN
24	$\overline{RESET}$
25	OSC
26	DATA OUT

NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE ON DIMENSIONS IS ± 0.38 mm (0.015 INCH).
3. LEAD MATERIAL: SOLDER PLATED COPPER ALLOY.

HCMS-291X



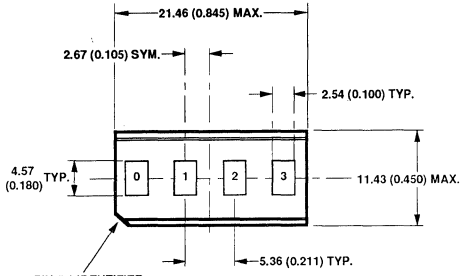


PIN FUNCTION ASSIGNMENT TABLE

PIN #	FUNCTION	PIN #	FUNCTION
1A	NO PIN	1B	NO PIN
2A	NO PIN	2B	NO PIN
3A	V LED	3B	V LED
4A	NO PIN	4B	NO PIN
5A	NO PIN	5B	NO PIN
6A	NO PIN	6B	NO PIN
7A	GND LED	7B	GND LED
8A	NO PIN	8B	NO PIN
9A	NO PIN	9B	NO PIN
10A	V LED	10B	V LED
11A	NO PIN	11B	NO PIN
12A	NO PIN	12B	NO PIN
13A	NO PIN	13B	NO PIN
14A	DATA IN	14B	DATA IN
15A	RS	15B	RS
16A	NO PIN	16B	NO PIN
17A	CLOCK	17B	CLOCK
18A	$\overline{CE}$	18B	$\overline{CE}$
19A	BLANK	19B	BLANK
20A	GND LOGIC	20B	GND LOGIC
21A	SEL	21B	SEL
22A	V LOGIC	22B	V LOGIC
23A	NO PIN	23B	NO PIN
24A	$\overline{RESET}$	24B	$\overline{RESET}$
25A	OSC	25B	OSC
26A	DATA OUT	26B	DATA OUT

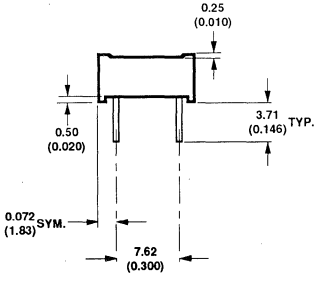
NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE ON DIMENSIONS IS ± 0.38 mm (0.015 INCH).
3. LEAD MATERIAL: SOLDER PLATED COPPER ALLOY.

HCMS-292X



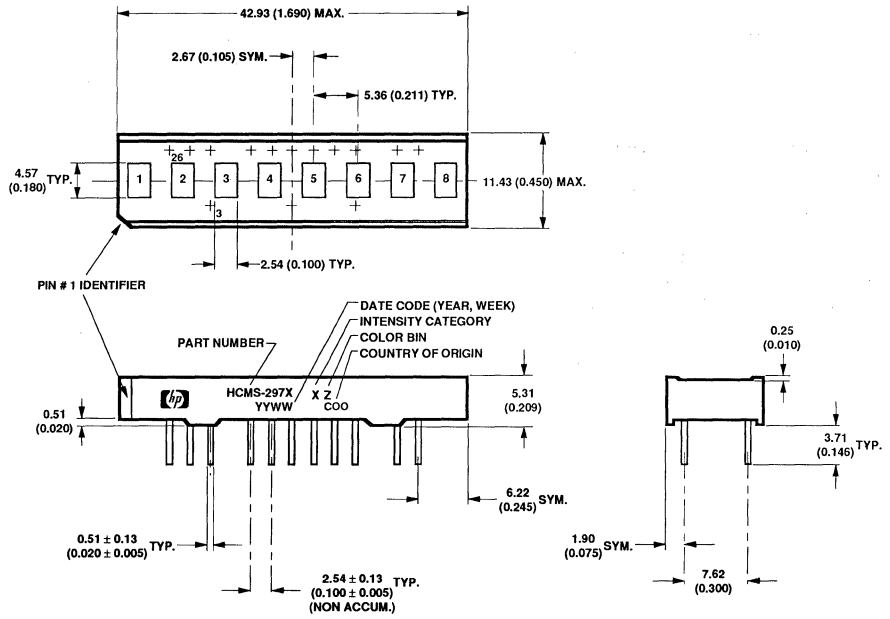
PIN FUNCTION ASSIGNMENT TABLE

PIN #	FUNCTION
1	DATA OUT
2	OSC
3	V LED
4	DATA IN
5	RS
6	CLK
7	$\overline{CE}$
8	BLANK
9	GND
10	SEL
11	V LOGIC
12	$\overline{RESET}$



NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON DIMENSIONS IS ± 0.38 mm (0.015 INCH).
3. LEAD MATERIAL: SOLDER PLATED COPPER ALLOY.

HCMS-296X



PIN FUNCTION ASSIGNMENT TABLE

PIN #	FUNCTION
1	NO PIN
2	NO PIN
3	V LED
4	NO PIN
5	NO PIN
6	NO PIN
7	GND LED
8	NO PIN
9	NO PIN
10	V LED
11	NO PIN
12	NO PIN
13	NO PIN
14	DATA IN
15	RS
16	NO PIN
17	CLOCK
18	$\overline{CE}$
19	BLANK
20	GND LOGIC
21	SEL
22	V LOGIC
23	NO PIN
24	$\overline{RESET}$
25	OSC
26	DATA OUT

NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE ON DIMENSIONS IS ± 0.38 mm (0.015 INCH).
3. LEAD MATERIAL: SOLDER PLATED COPPER ALLOY.

HCMS-297X

Absolute Maximum Ratings

Logic Supply Voltage, V_{LOGIC} to GND_{LOGIC}[1] ..... -0.3 V to 7.0 V
LED Supply Voltage, V_{LED} to GND_{LED} ..... -0.3 V to 5.5 V
Input Voltage, Any Pin to GND ..... -0.3 V to V_{LOGIC} +0.3 V
Free Air Operating Temperature Range T_A[2] ..... -40°C to +85°
Relative Humidity (non-condensing) 85%
Storage Temperature, T_S ..... -55°C to 100°C
Maximum Solder Temperature
1.59 mm (0.063 in.) Below Seating Plane, t< 5 sec ..... 260°C
ESD Protection @ 1.5 kΩ, 100 pF (each pin) ..... 2 KV
TOTAL Package Power Dissipation at T_A = 25°C[2]
4 character ..... 1.2 W
8 character ..... 2.4 W
16 character ..... 4.8 W

Notes:
1. Transient only.
2. For operation in high ambient temperatures, see Appendix A, Thermal Considerations.

Recommended Operating Conditions Over Temperature Range

(-40°C to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
Logic Supply Voltage	V_{LOGIC}	3.0	5.0	5.5	V
LED Supply Voltage	V_{LED}	4.0	5.0	5.5	V
GND_{LED} to GND_{LOGIC}	–	-0.3	0	+0.3	V

Electrical Characteristics Over Operating Temperature Range (-40°C to +85°C)

Parameter	Symbol	T_A = 25°C, V_{LOGIC} = 5.0 V Typ.	Max.	-40°C < T_A < 85°C, 3.0 V < V_{LOGIC} < 5.5 V Min.	Max.	Units	Test Conditions
Input Leakage Current	I_I					µA	V_{IN} = 0 V to V_{LOGIC}
HCMS-290X/296X (4 char)			+7.5	-2.5	+50		
HCMS-291X/297X (8 char)			+15	-5.0	+100		
HCMS-292X (16 char)			+15	-5.0	+100		
I_{LOGIC} OPERATING	I_{LOGIC}(OPT)					mA	V_{IN} = V_{LOGIC}
HCMS-290X/296X (4 char)		0.4	2.5		5		
HCMS-291X/297X (8 char)		0.8	5		10		
HCMS-292X (16 char)		0.8	5		10		
I_{LOGIC} SLEEP[1]	I_{LOGIC}(SLP)					µA	V_{IN} = V_{LOGIC}
HCMS-290X/296X (4 char)		5	15		25		
HCMS-291X/297X (8 char)		10	30		50		
HCMS-292X (16 char)		10	30		50		
I_{LED} BLANK	I_{LED}(BL)					mA	BL = 0 V
HMCS-290X/296X (4 char)		0.4	1.8		2.5		
HCMS-291X/297X (8 char)		0.8	3.5		5		
HCMS-292X (16 char)		0.8	3.5		5		
I_{LED} SLEEP[1]	I_{LED}(SLP)					µA	
HCMS-290X/296X (4 char)		1	3		50		
HCMS 291X/297X (8 char)		2	6		100		
HCMS-292X (16 char)		2	6		100		
Peak Pixel Current[2]	I_{PIXEL}						V_{LED} = 5.5 V
HCMS-29X5 (AlGaAs)		15.4	17.1		18.7	mA	All pixels ON,
HCMS-29XX (Other Colors)		14.0	15.9		17.1	mA	Average value per pixel
HIGH level input voltage	V_{ih}			2.0		V	4.5 V < V_{LOGIC} < 5.5 V
				0.8 V_{LOGIC}		V	3.0 V < V_{LOGIC} < 4.5 V
LOW level input voltage	V_{il}				1.1	V	4.5 V < V_{LOGIC} < 5.5 V
					0.2 V_{LOGIC}	V	3.0 V < V_{LOGIC} < 4.5 V
HIGH level output voltage	V_{oh}			2.4		V	V_{LOGIC} = 4.5 V, I_{oh} = -40 µA
				0.8 V_{LOGIC}		V	3.0 V < V_{LOGIC} < 4.5 V
LOW level output voltage	V_{ol}				0.4	V	V_{LOGIC} = 5.5 V, I_{ol} = 1.6 mA[3]
					0.2 V_{LOGIC}	V	3.0 V < V_{LOGIC} < 4.5 V
Thermal Resistance	$R\theta_{J-P}$	70				°C/W	IC junction to pin

Notes:
1. In SLEEP mode, the internal oscillator and reference current for LED drivers are off.
2. Average peak pixel current is measured at the maximum drive current set by Control Register 0. Individual pixels may exceed this value.
3. For the Oscillator Output, I_{ol} = 40 µA.

Optical Characteristics at 25°C[1]

V_{LED} = 5.0 V, 50% Peak Current, 100% Pulse Width

Display Color	Part Number	Luminous Intensity per LED[2] Character Average (μcd) Min.	Typ.	Peak Wavelength λ_{Peak} (nm) Typ.	Dominant Wavelength λ_d[3] (nm) Typ.
AlGaAs Red	HCMS-29X5	95	230	645	637
High Efficiency Red	HCMS-29X2	29	64	635	626
Orange	HCMS-29X4	29	64	600	602
Yellow	HCMS-29X1	29	64	583	585
Green	HCMS-29X3	57	114	568	574

Notes:
1. Refers to the initial case temperature of the device immediately prior to measurement.
2. Measured with all LEDs illuminated.
3. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the perceived LED color.

Electrical Description

Pin Function	Description
$\overline{\text{RESET}}$ ($\overline{\text{RST}}$)	Sets Control Register bits to logic low. The Dot Register contents are unaffected by the Reset pin. (logic low = reset; logic high = normal operation).
DATA IN (D_{IN})	Serial Data input for Dot or Control Register data. Data is entered on the rising edge of the Clock input.
DATA OUT (D_{OUT})	Serial Data output for Dot or Control Register data. This pin is used for cascading multiple displays.
CLOCK (CLK)	Clock input for writing Dot or Control Register data. When $\overline{\text{Chip Enable}}$ is logic low, data is entered on the rising Clock edge.
REGISTER SELECT (RS)	Selects Dot Register (RS = logic low) or Control Register (RS = logic high) as the destination for serial data entry. The logic level of RS is latched on the falling edge of the $\overline{\text{Chip Enable}}$ input.
$\overline{\text{CHIP ENABLE}}$ ($\overline{\text{CE}}$)	This input must be a logic low to write data to the display. When $\overline{\text{CE}}$ returns to logic high and CLK is logic low, data is latched to either the LED output drivers or a Control Register.
OSCILLATOR SELECT (SEL)	Selects either an internal or external display oscillator source. (logic low = External Display Oscillator; logic high = Internal Display Oscillator).
OSCILLATOR (OSC)	Output for the Internal Display Oscillator (SEL = logic high) or input for an External Display Oscillator (SEL = logic low).
BLANK (BL)	Blanks the display when logic high. May be modulated for brightness control.
GND_{LED}	Ground for LED drivers.
GND_{LOGIC}	Ground for logic.
V_{LED}	Positive supply for LED drivers.
V_{LOGIC}	Positive supply for logic.

AC Timing Characteristics Over Temperature Range (-40°C to +85°C)

Timing Diagram Ref. Number	Description	Symbol	4.5 V < V_{LOGIC} <5.5 V		V_{LOGIC} = 3 V		Units
			Min.	Max.	Min.	Max.	
1	Register Select Setup Time to $\overline{\text{Chip Enable}}$	t_{rss}	10		10		ns
2	Register Select Hold Time to $\overline{\text{Chip Enable}}$	t_{rsh}	10		10		ns
3	Rising Clock Edge to Falling $\overline{\text{Chip Enable}}$ Edge	t_{clkce}	20		20		ns
4	$\overline{\text{Chip Enable}}$ Setup Time to Rising Clock Edge	t_{ces}	35		55		ns
5	$\overline{\text{Chip Enable}}$ Hold Time to Rising Clock Edge	t_{ceh}	20		20		ns
6	Data Setup Time to Rising Clock Edge	t_{ds}	10		10		ns
7	Data Hold Time after Rising Clock Edge	t_{dh}	10		10		ns
8	Rising Clock Edge to D_{OUT}[1]	t_{dout}	10	40	10	65	ns
9	Propagation Delay D_{IN} to D_{OUT} Simultaneous Mode for one IC[1,2]	t_{doutp}		18		30	ns
10	CE Falling Edge to D_{OUT} Valid	t_{cedo}		25		45	ns
11	Clock High Time	t_{clkh}	80		100		ns
12	Clock Low Time	t_{clkl}	80		100		ns
	Reset Low Time	t_{rstl}	50		50		ns
	Clock Frequency	F_{cyc}		5		4	MHz
	Internal Display Oscillator Frequency	F_{inosc}	80	210	80	210	KHz
	Internal Refresh Frequency	F_{rf}	150	410	150	400	Hz
	External Display Oscillator Frequency	F_{exosc}					
	Prescaler = 1		51.2	1000	51.2	1000	KHz
	Prescaler = 8		410	8000	410	8000	KHz

Notes:
1. Timing specifications increase 0.3 ns per pf of capacitive loading above 15 pf.
2. This parameter is valid for simultaneous Mode data entry of the Control Register.

Display Overview

The HCMS-29XX series is a family of LED displays driven by on-board CMOS ICs. The LEDs are configured as 5 x 7 font characters and are driven in groups of 4 characters per IC. Each IC consists of a 160-bit shift register (the Dot Register), two 7-bit Control Words, and refresh circuitry. The Dot Register contents are mapped on a one-to-one basis to the display. Thus, an individual Dot Register bit uniquely controls a single LED.

8-character displays have two ICs that are cascaded. The Data Out line of the first IC is internally connected to the Data In line of the second IC forming a 320-bit Dot Register. The display's other control and power lines are connected directly to both ICs. In 16-character displays, each row functions as an independent 8-character display with its own 320-bit Dot Register.

Reset

Reset initializes the Control Registers (sets all Control Register bits to logic low) and places the display in the sleep mode. The $\overline{\text{Reset}}$ pin should be connected to the system power-on reset circuit. The Dot Registers are not cleared upon power-on or by $\overline{\text{Reset}}$. After power-on, the Dot Register contents are random; however, $\overline{\text{Reset}}$ will put the display in sleep mode, thereby blanking the LEDs. The Control Register and the Control Words are cleared to all zeros by $\overline{\text{Reset}}$.

To operate the display after being $\overline{\text{Reset}}$, load the Dot Register with logic lows. Then load Control Word 0 with the desired brightness level and set the sleep mode bit to logic high.

Dot Register

The Dot Register holds the pattern to be displayed by the LEDs. Data is loaded into the Dot Register according to the procedure shown in Table 1 and the Write Cycle Timing Diagram.

First RS is brought low, then $\overline{\text{CE}}$ is brought low. Next, each successive rising CLK edge will shift in the data at the D_{IN} pin. Loading a logic high will turn the corresponding LED on; a logic low turns the LED off. When all 160 bits have been loaded (or 320 bits in an 8-digit display), $\overline{\text{CE}}$ is brought to logic high.

When CLK is next brought to logic low, new data is latched into the display dot drivers. Loading data into the Dot Register takes place while the previous data is displayed and eliminates the need to blank the display while loading data.

Pixel Map

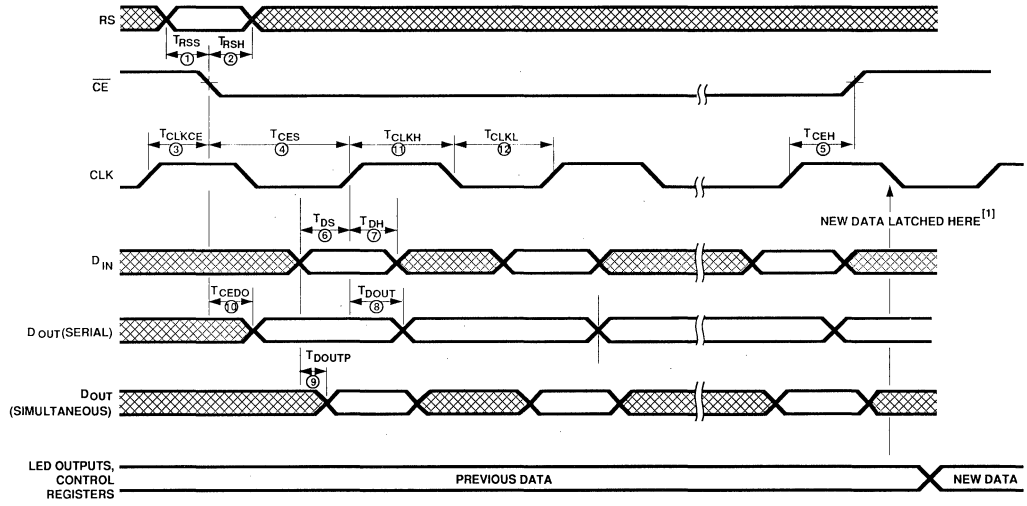
In a 4-character display, the 160-bits are arranged as 20

Table 1. Register Truth Table

Function	CLK	$\overline{\text{CE}}$	RS
Select Dot Register	Not Rising	↓	L
Load Dot Register D_{IN} = HIGH LED = "ON" D_{IN} = LOW LED = "OFF"	↑	L	X
Copy Data from Dot Register to Dot Latch	L	H	X
Select Control Register	Not Rising	↓	H
Load Control Register[1]	↑	L	X
Latch Data to Control Word 1[2]	L	H	X

Notes:

1. BIT D_0 of Control Word 1 must have been previously set to Low for serial mode or High for simultaneous mode.
2. Selection of Control Word 1 or Control Word 0 is set by D_7 of the Control Shift Register. The unselected control word retains its previous value.



NOTE:
1. DATA IS COPIED TO THE CONTROL REGISTER OR THE DOT LATCH AND LED OUTPUTS WHEN $\overline{CE}$ IS HIGH AND CLK IS LOW.

HCMS-29XX Write Cycle Diagram

columns by 8 rows. This array can be conceptualized as four 5 x 8 dot matrix character locations, but only 7 of the 8 rows have LEDs (see Figures 1 & 2). The bottom row (row 0) is not used. Thus, latch location 0 is never displayed. Column 0 controls the left-most column. Data from Dot Latch locations 0-7 determine whether or not pixels in Column 0 are turned-on or turned-off. Therefore, the lower left pixel is turned-on when a logic high is stored in Dot Latch location 1. Characters are loaded-in serially, with the left-most character being loaded first and the right-most character being loaded last. By loading one character at a time and latching the data before loading the next character, the figures will appear to scroll from right to left.

Control Register

The Control Register allows software modification of the IC's operation and consists of two independent 7-bit control words. Bit D_7 in the shift register selects one of the two 7-bit control words. Control Word 0 performs pulse width modulation brightness control, peak pixel current brightness control, and sleep mode. Control Word 1 sets serial/simultaneous data out mode, and external oscillator prescaler. Each function is independent of the others.

Control Register Data Loading

Data is loaded into the Control Register according to the procedure shown in Table 1 and the Write Cycle Timing Diagram. First, RS is brought to logic high and then $\overline{CE}$ is brought to logic low. Next, each successive rising CLK edge will shift in the data on the D_{IN} pin. Finally, when 8 bits have been loaded, the $\overline{CE}$ line is brought to logic high. When CLK goes to logic low, new data is copied into the selected control word. Loading data into the Control Register takes place while the previous control word configures the display.

Control Word 0

Loading the Control Register with D_7 = Logic low selects Control Word 0 (see Table 2). Bits D_0-D_3 adjust the display brightness by pulse width modulating the LED on time. While Bits D_4-D_5 adjust the display brightness by changing the peak pixel current. Bit D_6 selects normal operation or sleep mode.

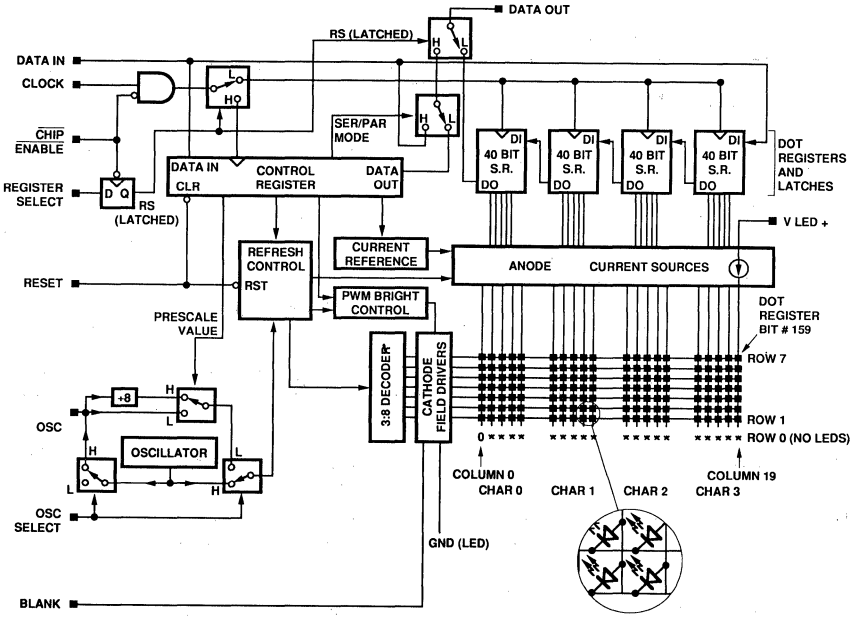


Figure 1.

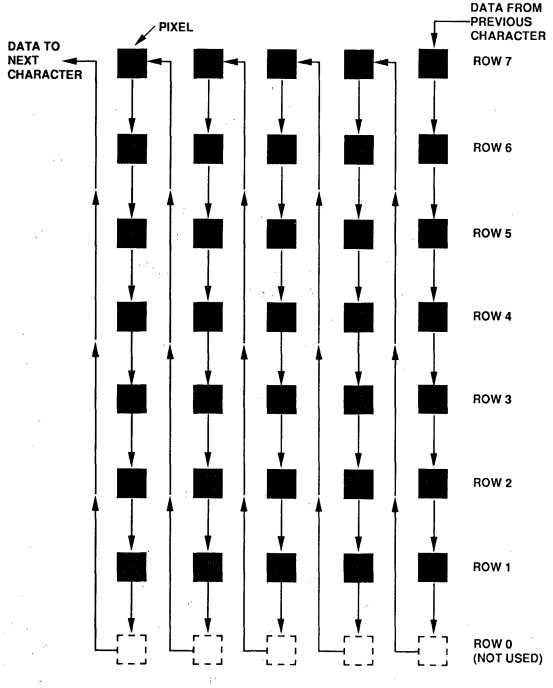


Figure 2.

Sleep mode (Control Word 0, bit D_6 = Low) turns off the Internal Display Oscillator and the LED pixel drivers. This mode is used when the IC needs to be powered up, but does not need to be active. Current draw in sleep mode is nearly zero. Data in the Dot Register and Control Words are retained during sleep mode.

Control Word 1

Loading the Control Register with D_7 = logic high selects Control Word 1. This Control Word performs two functions: serial/simultaneous data out mode and external oscillator prescale select (see Table 2).

Serial/Simultaneous Data Output D_0

Bit D_0 of control word 1 is used to switch the mode of D_{OUT} between serial and simultaneous data entry during Control Register writes. The default mode (logic low) is the serial D_{OUT} mode. In serial mode, D_{OUT} is connected to the last bit (D_7) of the Control Shift Register.

Storing a logic high to bit D_0 changes D_{OUT} to simultaneous mode which affects the Control Register only. In simultaneous mode, D_{OUT} is logically connected to D_{IN}. This arrangement allows multiple ICs to have their Control Registers written to simultaneously. For example, for N ICs in the serial mode, N * 8 clock pulses are needed to load the same data in all Control Registers. In the simultaneous mode, N ICs only need 8 clock pulses to load the same data in all Control Registers. The propagation delay from the first IC to the last is N * t_{DOUTP}.

External Oscillator Prescaler Bit D_1

Bit D_1 of Control Word 1 is used to scale the frequency of an external Display Oscillator. When this bit is logic low, the external Display Oscillator directly sets the internal display clock rate. When this bit is a logic high, the external oscillator is divided by 8. This scaled frequency then sets the internal display clock rate. It takes 512 cycles of the display clock (or 8 x 512 = 4096 cycles of an external clock with the divide by 8 prescaler) to completely refresh the display once. Using the prescaler bit allows the designer to use a higher external oscillator frequency without extra circuitry.

This bit has no affect on the internal Display Oscillator Frequency.

Bits D_2-D_6

These bits must always be programmed to logic low.

Cascaded ICs

Figure 3 shows how two ICs are connected within an HCMS-29XX display. The first IC controls the four left-most characters and the second IC controls the four right-most characters. The Dot Registers are connected in series to form a 320-bit dot shift register. The location of pixel 0 has not changed. However, Dot Shift Register bit 0 of IC2 becomes bit 160 of the 320-bit dot shift register.

The Control Registers of the two ICs are independent of each other. This means that to adjust the display brightness the same control word must be entered into both ICs, unless the Control Registers are set to simultaneous mode.

Longer character string systems can be built by cascading multiple displays together. This is accomplished by creating a five line bus. This bus consists of $\overline{CE}$, RS, BL, $\overline{Reset}$, and CLK. The display pins are connected to the corresponding bus line. Thus, all $\overline{CE}$ pins are connected to the $\overline{CE}$ bus line. Similarly, bus lines for RS, BL, $\overline{Reset}$, and CLK are created. Then D_{IN} is connected to the right-most display. D_{OUT} from this display is connected to the next display. The left-most display receives its D_{IN} from the D_{OUT} of the display to its right. D_{OUT} from the left-most display is not used.

Each display may be set to use its internal oscillator, or the displays may be synchronized by setting up one display as the master and the others as slaves. The slaves are set to receive their oscillator input from the master's oscillator output.

Table 2. Control Shift Register

CONTROL WORD 0

L	D_6	D_5	D_4	D_3	D_2	D_1	D_0

↑ Bit D_7 Set Low to Select Control Word 0

DWM Brightness Control

				On-Time Oscillator Cycles	Duty Factor (%)	Relative Brightness (%)
L	L	L	L	0	0	0
L	L	L	H	1	0.2	1.7
L	L	H	L	2	0.4	3.3
L	L	H	H	3	0.6	5.0
L	H	L	L	4	0.8	6.7
L	H	L	H	5	1.0	8.3
L	H	H	L	7	1.4	11.7
L	H	H	H	9	1.8	15
H	L	L	L	11	2.1	18
H	L	L	H	14	2.7	23
H	L	H	L	18	3.5	30
H	L	H	H	22	4.3	37
H	H	L	L	28	5.5	47
H	H	L	H	36	7.0	60
H	H	H	L	48	9.4	80
H	H	H	H	60	11.7	100

Peak Current Brightness Control	Typical Peak Pixel Current (mA)	Relative Full Scale Current (Relative Brightness, %)
H L	4.0	31
L H	6.4	50
L L	9.3	73 (Default at Power Up)
H H	12.8	100

$\overline{\text{SLEEP MODE}}$ L – DISABLES INTERNAL OSCILLATOR-DISPLAY BLANK
H – NORMAL OPERATION

CONTROL WORD 1

H	L	L	L	L	L	D_1	D_0

↑ Bit D_7 Set High to Select Control Word 1

Reserved for Future Use (Bits D_2-D_6 must be set Low)

Serial/Simultaneous Data Out
L – D_{out} holds contents of Bit D_7
H – D_{out} is functionally tied to D_{in}

External Display Oscillator Prescaler
L – Oscillator Freq ÷ 1
H – Oscillator Freq ÷ 8

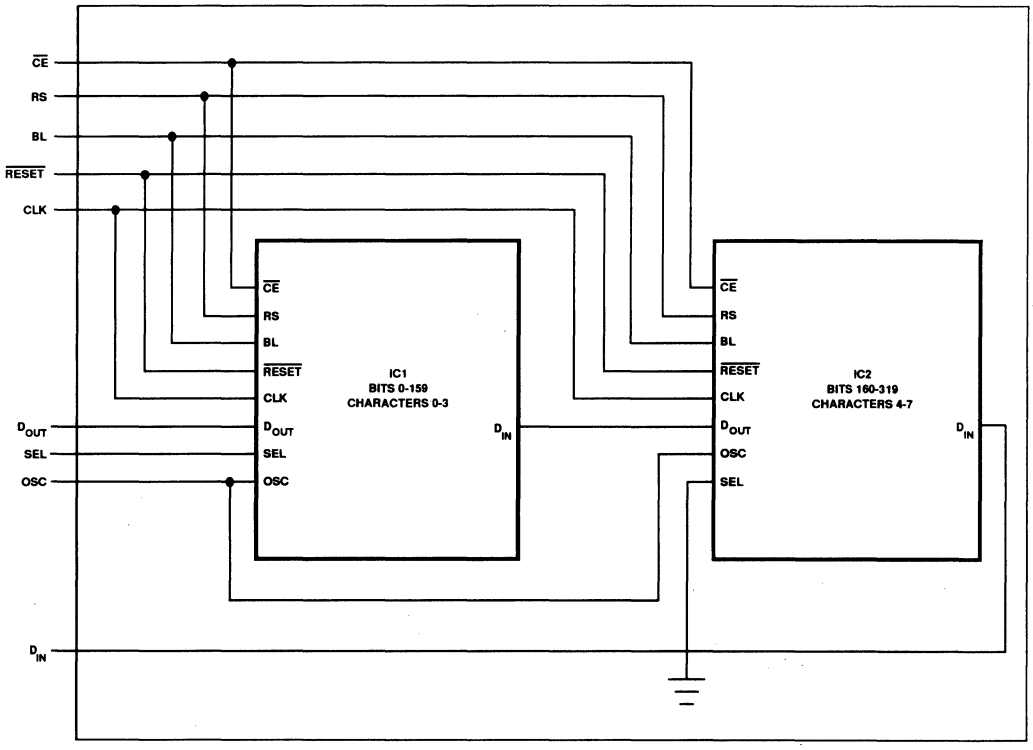


Figure 3. Cascaded ICs.

Appendix A. Thermal Considerations

The display IC has a maximum junction temperature of 150°C. The IC junction temperature can be calculated with Equation 1 below.

A typical value for $R\theta_{JA}$ is 100°C/W. This value is typical for a display mounted in a socket and covered with a plastic filter. The socket is soldered to a .062 in. thick PCB with .020 inch wide, one ounce copper traces.

P_D can be calculated as Equation 2 below.

Figure 4 shows how to derate the power of one IC versus ambient temperature. Operation at high ambient temperatures may require the power per IC to be reduced. The power consumption can be reduced by changing either the N, I_{PIXEL}, Osc cyc or V_{LED}. Changing V_{LOGIC} has very little impact on the power consumption.

Equation 1:

$T_JMAX = T_A + P_D * R\theta_{JA}$

Where:

T_JMAX = maximum IC junction temperature
T_A = ambient temperature surrounding the display
$R\eta_{JA}$ = thermal resistance from the IC junction to ambient
P_D = power dissipated by the IC

Equation 2:

$P_D = (N * I_{PIXEL} * \text{Duty Factor} * V_{LED}) + I_{LOGIC} * V_{LOGIC}$

Where:

P_D = total power dissipation
N = number of pixels on (maximum 4 char * 5 * 7 = 140)
I_{PIXEL} = peak pixel current.
Duty Factor = 1/8 * Osccyc/64
Osc cyc = number of ON oscillator cycles per row
I_{LOGIC} = IC logic current
V_{LOGIC} = logic supply voltage

Equation 3:

$I_{PEAK} = M * 20 * I_{PIXEL}$

Where:

I_{PEAK} = maximum instantaneous peak current for the display
M = number of ICs in the system
20 = maximum number of LEDs on per IC
I_{PIXEL} = peak current for one LED

Equation 4:

$I_{LED}(AVG) = N * I_{PIXEL} * 1/8 * (\text{oscillator cycles})/64$

(see Variable Definitions above)

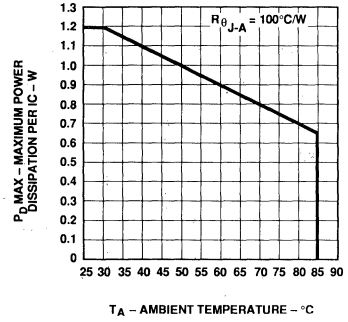


Figure 4.

Appendix B. Electrical Considerations

Current Calculations

The peak and average display current requirements have a significant impact on power supply selection. The maximum peak current is calculated with Equation 3 below.

The average current required by the display can be calculated with Equation 4 below.

The power supply has to be able to supply I_{PEAK} transients and supply $I_{LED}(AVG)$ continuously. The range on V_{LED} allows noise on this supply without significantly changing the display brightness.

V_{LOGIC} and V_{LED} Considerations

The display uses two independent electrical systems. One system is used to power the display's logic and the other to power the display's LEDs. These two systems keep the logic supply clean.

Separate electrical systems allow the voltage applied to V_{LED} and V_{LOGIC} to be varied independently. Thus, V_{LED} can vary from 0 to 5.5 V without

effecting either the Dot or the Control Registers. V_{LED} can be varied between 4.0 to 5.5 V without any noticeable variation in light output. However, operating V_{LED} below 4.0 V may cause objectionable mismatch between the pixels and is not recommended. Dimming the display by pulse width modulating V_{LED} is also not recommended.

V_{LOGIC} can vary from 3.0 to 5.5 V without effecting either the displayed message or the display intensity. However, operation below 4.5 V will change the timing and logic levels and operation below 3 V may cause the Dot and Control Registers to be altered.

The logic ground is internally connected to the LED ground by a substrate diode. This diode becomes forward biased and conducts when the logic ground is 0.4 V greater then the LED ground. The LED ground and the logic ground should be connected to a common ground which can withstand the current introduced by the switching LED drivers. When separate ground connections are used, the LED ground can vary from -0.3 V to +0.3 V with respect to the logic ground. Voltages below -0.3 V can cause all the dots to be ON. Voltage above +0.3 V can cause dimming and dot mismatch. The LED ground for the LED drivers can be routed separately from the logic ground until an appropriate ground plane is available. On long interconnections between the display and the host system, voltage drops on the analog ground can be kept from affecting the display logic levels by isolating the two grounds.

Electrostatic Discharge
The inputs to the ICs are protected against static discharge and input current latchup. However, for best results, standard CMOS handling precautions should be used. Before use, the HCMS-29XX should be stored in antistatic tubes or in conductive material. During assembly, a grounded conductive work area should be used and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static buildup. Input current latchup is caused when the CMOS inputs are subjected to either a voltage below ground (V_{IN} < ground) or to a voltage higher then V_{LOGIC} (V_{IN} > V_{LOGIC}) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected to either ground or V_{LOGIC}. Voltages should not be applied to the inputs until V_{LOGIC} has been applied to the display.

Appendix C. Oscillator

The oscillator provides the internal refresh circuitry with a signal that is used to synchronize the columns and rows. This ensures that the right data is in the dot drivers for that row. This signal can be supplied from either an external source or an internal source.

A display refresh rate of 100 Hz or faster ensures flicker-free operation. Thus for an external oscillator the frequency should be greater than or equal to 512 x 100 Hz = 51.2 kHz. Operation above 1 MHz without the prescaler or 8 MHz with the prescaler may cause noticeable pixel to pixel mismatch.

Appendix D. Refresh Circuitry

This display driver consists of 20 one-of-eight column decoders and 20 constant current sources, 1 one-of-eight row decoder and eight row sinks, a pulse width modulation control block, a peak current control block, and the circuit to refresh the LEDs. The refresh counters and oscillator are used to synchronize the columns and rows.

The 160 bits are organized as 20 columns by 8 rows. The IC illuminates the display by sequentially turning ON each of the 8 row-drivers. To refresh the display once takes 512 oscillator cycles. Because there are eight row-drivers, each row-driver is selected for 64 (512/8) oscillator cycles. Four cycles are used to briefly blank the display before the following row is switched on. Thus, each row is ON for 60 oscillator cycles out of a possible 64. This corresponds to the maximum LED on time.

Appendix E. Display Brightness

Two ways have been shown to control the brightness of this LED display: setting the peak current and setting the duty factor. Both values are set in Control Word 0. To compute the resulting display brightness when both PWM and peak current control are used, simply multiply the two relative brightness factors. For example, if Control Register 0 holds the word 1001101, the peak current is 73% of full scale (BIT D_5 = L, BIT D_4 = L) and the PWM is set to 60% duty factor (BIT D_3 = H, BIT D_2 = H, BIT D_1 = L, BIT D_0 = H). The resulting brightness is 44% (.73 x .60 = .44) of full scale.

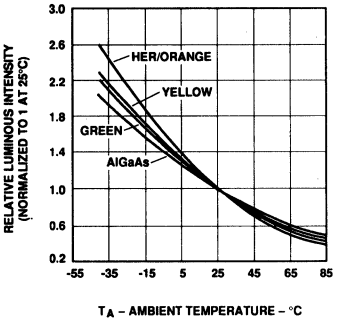


Figure 5.

The temperature of the display will also affect the LED brightness as shown in Figure 5.

Appendix F. Reference Material

Application Note 1027: *Soldering LED Components*
Application Note 1015: *Contrast Enhancement Techniques for LED Displays*

HEWLETT PACKARD

Four Character 5.0mm (0.2 in.) Smart 5 x 7 Alphanumeric Displays

Technical Data

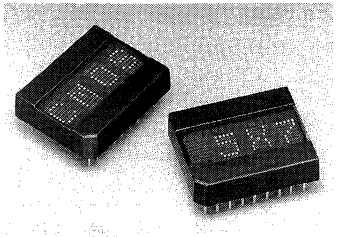
HDLX-2416 Series

Features

- **Enhanced Drop-in Replacement to HPDL-2416**
- **Smart Alphanumeric Display**
  Built-in RAM, ASCII Decoder, and LED Drive Circuitry
- **CMOS IC for Low Power Consumption**
- **Software Controlled Dimming Levels and Blank**
- **128 ASCII Character Set**
- **End-Stackable**
- **Categorized for Luminous Intensity; YELLOW and GREEN Categorized for Color**
- **Low Power and Sunlight Viewable AlGaAs Versions**
- **Wide Operating Temperature Range**
  -40°C to +85°C
- **Excellent ESD Protection**
- **Wave Solderable**
- **Wide Viewing Angle (50° typ)**

Description

These are 5.0 mm (0.2 inch) four character 5 x 7 dot matrix displays driven by an on-board CMOS IC. These displays are pin for pin compatible with the HPDL-2416. The IC stores and decodes 7 bit ASCII data and displays it using a 5 x 7 font. Multiplexing circuitry, and drivers are also part of the IC. The IC has fast setup and hold times which makes it easy to interface to a microprocessor.



Absolute Maximum Ratings

Supply Voltage, V_{DD} to Ground[1] ..... -0.5 V to 7.0 V
Input Voltage, Any Pin to Ground ..... -0.5 V to V_{DD} + 0.5 V
Free Air Operating Temperature Range, T_A ..... -40°C to +85°C
Storage Temperature, T_S ..... -40°C to 100°C
CMOS IC Junction Temperature, T_J (IC) ..... +150°C
Relative Humidity (non-condensing) at 65°C 85%
Maximum Solder Temperature, 1.59 mm (0.063 in.) below Seating Plane, t < 5 sec. ..... 260°C
ESD Protection, R = 1.5 kΩ, C = 100 pF ..... V_Z = 2 kV (each pin)

Note:
1. Maximum Voltage is with no LEDs illuminated.

Devices:

Standard Red	AlGaAs Red	High Efficiency Red	Orange	Yellow	Green
HDLR-2416	New HDLS-2416	HDLO-2416	HDLA-2416	HDLY-2416	HDLG-2416
	New HDLU-2416				

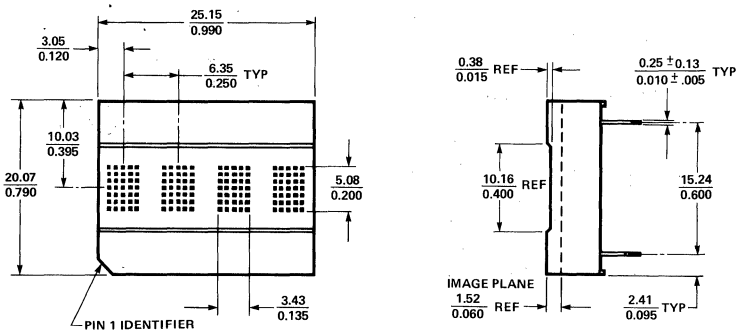
ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED WITH THE HDLX-2416

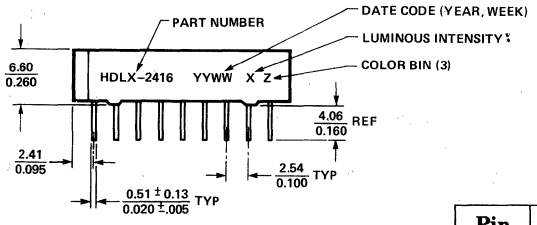
The address and data inputs can be directly connected to the microprocessor address and data buses.

The HDLX-2416 has several enhancements over the HPDL-2416. These features include an expanded character set, internal 8 level dimming control, external dimming capability, and individual digit blanking. Finally, the extended functions can be disabled which allows the HDLX-2416 to operate exactly like an HPDL-2416 by disabling all of the enhancements except the expanded character set.

The difference between the sunlight viewable HDLS-2416 and the low power HDLU-2416 occurs at power-on or at the default brightness level. Following power up, the HDLS-2416 operates at the 100% brightness level, while the HDLU-2416 operates at the 27% brightness level. Power on sets the internal brightness control (bits 3-5) in the control register to binary code (000). For the HDLS-2416 binary code (000) corresponds to a 100% brightness level, and for the HDLU-2416 binary code (000) corresponds to a 27% brightness level. The other seven brightness levels are identical for both parts.

Package Dimensions





Pin No.	Function	Pin No.	Function
1	$\overline{CE}_1$ Chip Enable	10	GND
2	$\overline{CE}_2$ Chip Enable	11	D_0 Data Input
3	$\overline{CLR}$ Clear	12	D_1 Data Input
4	$\overline{CUE}$ Cursor Enable	13	D_2 Data Input
5	$\overline{CU}$ Cursor Select	14	D_3 Data Input
6	$\overline{WR}$ Write	15	D_6 Data Input
7	A_1 Address Input	16	D_5 Data Input
8	A_0 Address Input	17	D_4 Data Input
9	V_{DD}	18	$\overline{BL}$ Display Blank

Notes:
1. Unless otherwise specified the tolerance on all dimensions is ±0.254 mm (±0.010")
2. All dimensions are in mm/inches.
3. For yellow and green displays only.

Character Set

ASCII CODE																			
			D0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
			D1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			D2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			D3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
D6	D5	D4	Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	0																
0	0	1	1																
0	1	0	2																
0	1	1	3																
1	0	0	4																
1	0	1	5																
1	1	0	6																
1	1	1	7																

Notes: 1. High = 1 level.
2. Low = 0 level.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

Electrical Characteristics Over Operating Temperature Range

$4.5 < V_{DD} < 5.5$ V (unless otherwise specified)

All Devices

Parameter	Symbol	Min.	25°C[1] Typ.	25°C[1] Max.	Max.	Units	Test Conditions
I_{DD} Blank	I_{DD}(blnk)		1.0		4.0	mA	All Digits Blanked
Input Current	I_I	-40			10	µA	V_{IN} = 0 V to V_{DD} V_{DD} = 5.0 V
Input Voltage High	V_{IH}	2.0			V_{DD}	V	
Input Voltage Low	V_{IL}	GND			0.8	V	

HDLO/HDLA/HDLY/HDLG-2416

Parameter	Symbol	Min.	25°C[1] Typ.	25°C[1] Max.	Max.	Units	Test Conditions
I_{DD} 4 digits 20 dots/character[2, 3]	I_{DD}(#)		110	130	160	mA	"#" ON in all four locations
I_{DD} Cursor all dots ON @ 50%	I_{DD} (CU)		92	110	135	mA	Cursor ON in all four locations

HDLS/HDLU-2416

Part Number	Parameter	Symbol	25°C[1] Typ.	25°C[1] Max.	Max.	Units	Test Conditions
HDLS-2416	I_{DD} 4 digits 20 dots/character[2,3]	I_{DD}(#)	125	146	180	mA	Four "#" ON in all four locations
HDLU-2416			34	42	52		
HDLS-2416	I_{DD} Cursor all dots ON @ 50%	I_{DD}(CU)	105	124	154	mA	Four cursors ON in all four locations
HDLU-2416			29	36	45		

HDLR-2416

Parameter	Symbol	Min.	25°C[1] Typ.	25°C[1] Max.	Max.	Units	Test Conditions
I_{DD} 4 digits 20 dots/character[2,3]	I_{DD} (#)		125	146	180	mA	"#" ON in all four locations
I_{DD} Cursor all dots ON @ 50%	I_{DD}(CU)		105	124	154	mA	Cursor ON in all four locations

Notes:

1. V_{DD} = 5.0 V
2. Average I_{DD} measured at full brightness. Peak I_{DD} = 28/15 x Average I_{DD}(#).
3. I_{DD}(#) max. = 130 mA for HDLO/HDLA/HDLY/HDLG-2416, 146 mA for HDLR/HDLS-2416, and 42 mA for HDLU-2416 at default brightness, 150°C IC junction temperature and V_{DD} = 5.5 V.

Optical Characteristics at 25°C[1]

V_{DD} = 5.0 V at Full Brightness

HDLR-2416

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	0.5	1.1	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		655	nm	
Dominant Wavelength[2]	λ_d		640	nm	

HDLS/HDLU-2416

Part Number	Parameter	Symbol	Min.	Typ.	Units	Test Conditions
HDLS-2416	Average Luminous Intensity per digit, Character Average	I_V	4.0	12.7	mcd	"*" illuminated in all four digits, 19 dots ON per digit.
HDLU-2416			1.2	3.1	mcd	
All	Peak Wavelength	λ_{PEAK}		645	nm	
	Dominant Wavelength[2]	λ_d		637	nm	

HDLO-2416

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	1.2	3.5	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		635	nm	
Dominant Wavelength[2]	λ_d		626	nm	

HDLA-2416

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	1.2	3.5	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		600	nm	
Dominant Wavelength[2]	λ_d		602	nm	

HDLY-2416

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	1.2	3.7	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		583	nm	
Dominant Wavelength[2]	λ_d		585	nm	

HDLG-2416

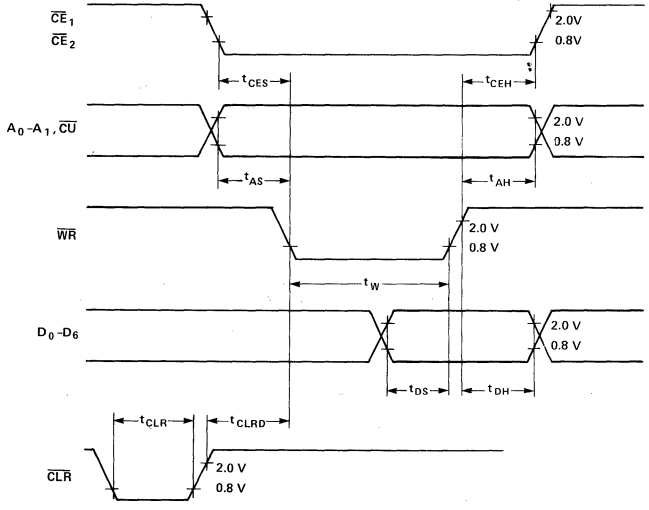
Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	1.2	5.6	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		568	nm	
Dominant Wavelength[2]	λ_d		574	nm	

Notes:
1. Refers to the initial case temperature of the device immediately prior to the light measurement.
2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.

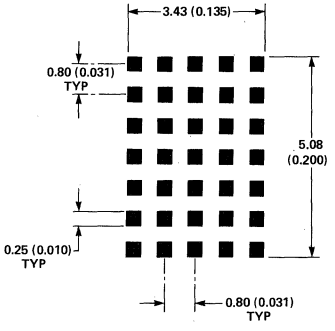
AC Timing Characteristics Over Operating Temperature Range at V_{DD} = 4.5 V

Parameter	Symbol	Min	Units
Address Setup	t_{AS}	10	ns
Address Hold	t_{AH}	40	ns
Data Setup	t_{DS}	50	ns
Data Hold	t_{DH}	40	ns
Chip Enable Setup	t_{CES}	0	ns
Chip Enable Hold	t_{CEH}	0	ns
Write Time	t_W	75	ns
Clear	t_{CLR}	10	µs
Clear Disable	t_{CLRD}	1	µs

Timing Diagram



Enlarged Character Font



NOTES:
1. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ± 0.254 mm (0.010 IN.)
2. DIMENSIONS ARE IN MILLIMETRES (INCHES).

Electrical Description

Pin Function	Description
Chip Enable ($\overline{CE}_1$ and $\overline{CE}_2$, pins 1 and 2)	$\overline{CE}_1$ and $\overline{CE}_2$ must be a logic 0 to write to the display.
Clear ($\overline{CLR}$, pin 3)	When $\overline{CLR}$ is a logic 0 the ASCII RAM is reset to 20hex (space) and the Control Register/ Attribute RAM is reset to 00hex.
Cursor Enable (CUE pin 4)	CUE determines whether the IC displays the ASCII or the Cursor memory. (1 = Cursor, 0 = ASCII).
Cursor Select ($\overline{CU}$, pin 5)	$\overline{CU}$ determines whether data is stored in the ASCII RAM or the Attribute RAM/Control Register. (1 = ASCII, 0 = Attribute RAM/Control Register).
Write ($\overline{WR}$, pin 6)	$\overline{WR}$ must be a logic 0 to store data in the display.
Address Inputs (A_1 and A_0, pins 8 and 7)	A_0-A_1 selects a specific location in the display memory. Address 00 accesses the far right display location. Address 11 accesses the far left location.
Data Inputs (D_0-D_6, pins 11-17)	D_0-D_6 are used to specify the input data for the display.
V_{DD} (pin 9)	V_{DD} is the positive power supply input.
GND (pin 10)	GND is the display ground.
Blanking Input ($\overline{BL}$, pin 18)	$\overline{BL}$ is used to flash the display, blank the display or to dim the display.

Display Internal Block Diagram

Figure 1 shows the HDLX-2416 display internal block diagram. The CMOS IC consists of a 4 x 7 Character RAM, a 2 x 4 Attribute RAM, a 5 bit Control Register, a 128 character ASCII decoder and the refresh circuitry necessary to synchronize the decoding and driving of four 5 x 7 dot matrix displays.

Four 7 bit ASCII words are stored in the Character RAM. The IC reads the ASCII data and decodes it via the 128 character ASCII decoder. The ASCII decoder includes the 64 character set of the HPDL-2416, 32 lower case ASCII symbols, and 32 foreign language symbols.

A 5 bit word is stored in the Control Register. Three fields within the Control Register provide an 8 level brightness control, master blank, and extended functions disable.

For each display digit location, two bits are stored in the Attribute RAM. One bit is used to enable a cursor character at each digit location. A second bit is used to individually disable the blanking features at each digit location.

The display is blanked and dimmed through an internal blanking input on the row drivers. Logic within the IC allows the user to dim the display either through the $\overline{BL}$ input or through the brightness control in the control register. Similarly the display can be blanked through the $\overline{BL}$ input, the Master Blank in the Control Register, or the Digit Blank Disable in the Attribute RAM.

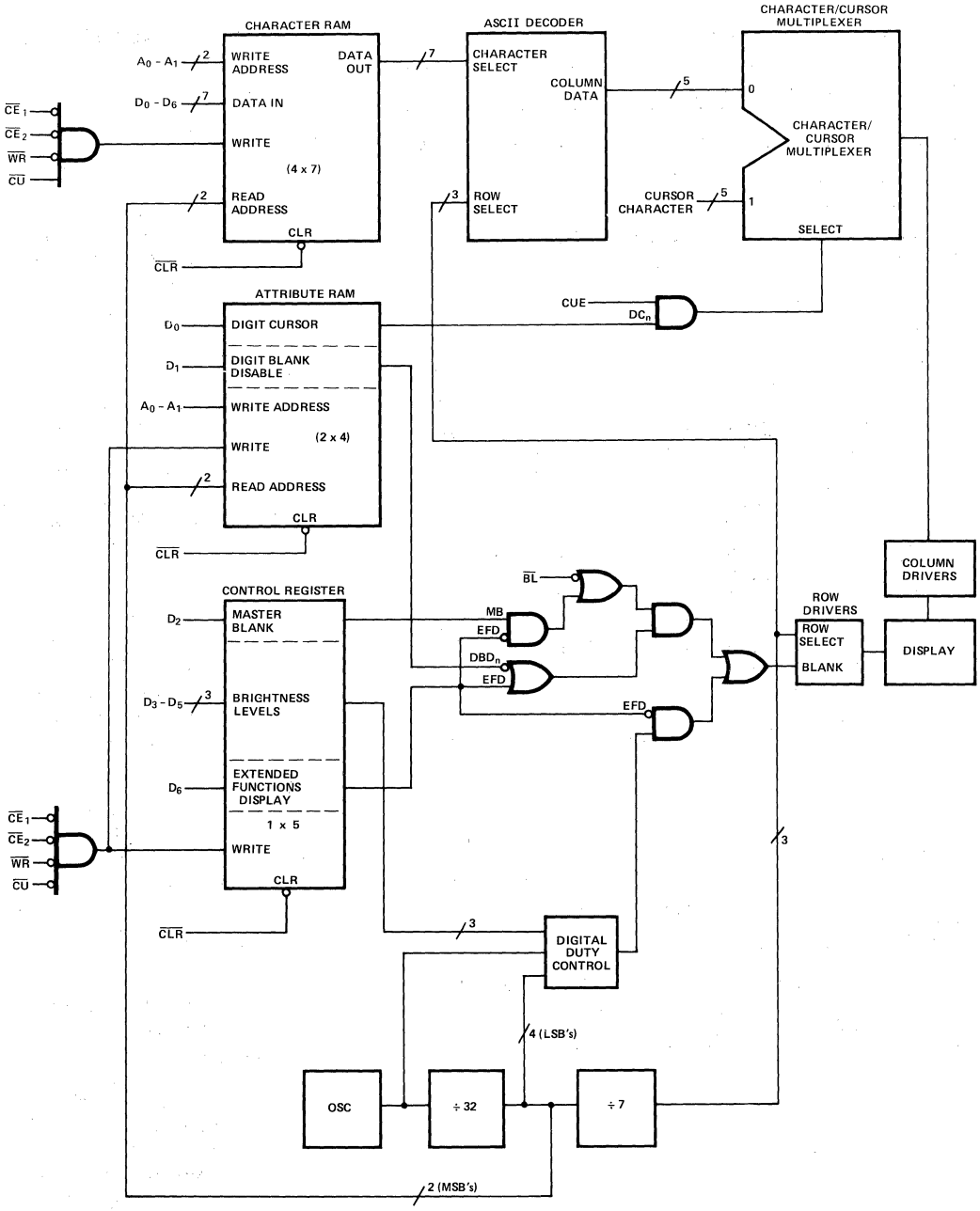


Figure 1. Internal Block Diagram

Display Clear

Data stored in the Character RAM, Control Register, and Attribute RAM will be cleared if the clear ($\overline{CLR}$) is held low for a minimum of 10 µs. Note that the display will be cleared regardless of the state of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$). After the display is cleared, the ASCII code for a space (20hex) is loaded into all character RAM locations and 00hex is loaded into all Attribute RAM/Control Register memory locations.

Data Entry

Figure 2 shows a truth table for the HDLX-2416 display. Setting the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) to logic 0 and the cursor select ($\overline{CU}$) to logic 1 will enable ASCII data loading. When cursor select ($\overline{CU}$) is set to logic 0, data will be loaded into the Control Register and Attribute RAM. Address inputs A_0-A_1 are used to select the digit location in the display. Data inputs D_0-D_6 are used to load information into the display. Data will be latched into the display on the rising edge of the $\overline{WR}$ signal. D_0-D_6, A_0-A_1, $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CU}$ must be held stable during the write cycle to ensure that correct data is stored into the display. Data can be loaded into the display in any order. Note that when A_0 and A_1 are logic 0, data is stored in the right most display location.

Cursor

When cursor enable (CUE) is a logic 1, a cursor will be displayed in all digit locations where a logic 1 has been stored in the Digit Cursor memory in the Attribute RAM. The cursor consists of all 35 dots ON at half brightness. A flashing cursor can be displayed by pulsing CUE. When CUE is a logic 0, the ASCII data stored in the Character RAM will be displayed regardless of the Digit Cursor bits.

Blanking

Blanking of the display is controlled through the $\overline{BL}$ input, the Control Register and Attribute RAM. The user can achieve a variety of functions by using these controls in different combinations, such as full hardware display blank, software blank, blanking of individ-

CUE	$\overline{BL}$	$\overline{CLR}$	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WR}$	$\overline{CU}$	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Function
0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Display ASCII
1	1	1															Display Stored Cursor
X	X	0															Reset RAMs
X	0	1															Blank Display but do not reset RAMS and Control Register
X	X	1	0	0	0	0	0	0	Extended Functions Disable	Intensity Control			Master Blank		Digit Blank Disable 0	Digit Cursor 0	Write to Attribute RAM and Control Register
						0	0	1	0 = Enable D_1-D_6	000 = 100%* 001 = 60% 010 = 40% 011 = 27% 100 = 17% 101 = 10% 110 = 7% 111 = 3%			0 = Display ON		Digit Blank Disable 1	Digit Cursor 1	DBD_n = 0, Allows Digit n to be blanked
						0	1	0	1 = Disable D_1-D_6				1 = Display Blanked		Digit Blank Disable 2	Digit Cursor 2	DBD_n = 1 Prevents Digit n from being blanked. DC_n = 0 Removes cursor from Digit n
						0	1	1	D_0 Always Enabled						Digiit Blank Disable 3	Digit Cursor 3	DC_n = 1 Stores cursor at Digit n
X	X	1	0	0	0	1	0	0	Digit 0 ASCII Data (Right Most Character)								Write to Character RAM
						1	0	1	Digit 1 ASCII Data								
						1	1	0	Digit 2 ASCII Data								
						1	1	1	Digit 3 ASCII Data (Left Most Character)								
X	X	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	No Change
			X	1	X												
			X	X	1												

0 = Logic 0; 1 = Logic 1; X = Do Not Care; * 000 = 27% for HDLU-2416

Figure 2. Display Truth Table

ual characters, and synchronized flashing of individual characters or entire display (by strobing the blank input). All of these blanking modes affect only the output drivers, maintaining the contents and write capability of the internal RAMs and Control Register, so that normal loading of RAMs and Control Register can take place even with the display blanked.

Figure 3 shows how the Extended Function Disable (bit D_6 of the Control Register), Master Blank (bit D_2 of the Control Register), Digit Blank Disable (bit D_1 of the Attribute RAM), and $\overline{BL}$ input can be used to blank the display.

When the Extended Function Disable is a logic 1, the display can be blanked only with the $\overline{BL}$ input. When the Extended Function Disable is a logic 0, the display can be blanked through the $\overline{BL}$ input, the Master Blank, and the Digit Blank Disable. The entire display will be blanked if either the $\overline{BL}$ input is logic 0 or the Master Blank is logic 1, providing all Digit Blank Disable bits are logic 0. Those digits with Digit Blank Disable bits a logic 1 will ignore both blank signals and remain ON. The Digit Blank Disable bits allow individual characters to be blanked or flashed in synchronization with the $\overline{BL}$ input.

EFD	MB	DBD_n	$\overline{BL}$	
0	0	0	0	Display Blanked by $\overline{BL}$
0	0	X	1	Display ON
0	X	1	0	Display Blanked by $\overline{BL}$. Individual characters "ON" based on "1" being stored in DBD_n
0	1	0	X	Display Blanked by MB
0	1	1	1	Display Blanked by MB. Individual characters "ON" based on "1" being stored in DBD_n
1	X	X	0	Display Blanked by $\overline{BL}$
1	X	X	1	Display ON

Figure 3. Display Blanking Truth Table

Dimming

Dimming of the display is controlled through either the $\overline{BL}$ input or the Control Register. A pulse width modulated signal can be applied to the $\overline{BL}$ input to dim the display. A three bit word in the Control Register generates an internal pulse width modulated signal to dim the display. The internal dimming feature is enabled only if the Extended Function Disable is a logic 0.

Bits 3-5 in the Control Register provide internal brightness control. These bits are interpreted as a three bit binary code, with code (000) corresponding to the maximum brightness and code (111) to the minimum brightness. In addition to varying the display brightness, bits 3-5 also vary the average value of I_{DD}. I_{DD} can be specified at any brightness level as shown in Table 1:

Table 1. Current Requirements at Different Brightness Levels

Symbol	D_5	D_4	D_3	Brightness	25°C Typ.	25°C Max.	Max. over Temp.	Units
I_{DD}(#)	0	0	0	100%	110	130	160	mA
	0	0	1	60%	66	79	98	mA
	0	1	0	40%	45	53	66	mA
	0	1	1	27%	30	37	46	mA
	1	0	0	17%	20	24	31	mA
	1	0	1	10%	12	15	20	mA
	1	1	0	7%	9	11	15	mA
	1	1	1	3%	4	6	9	mA

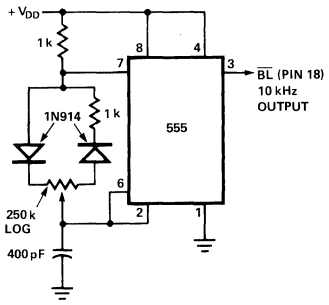


Figure 4. Intensity Modulation Control Using an Astable Multivibrator (reprinted with permission from *Electronics* magazine, Sept. 19, 1974, VNU Business pub. Inc.)

Figure 4 shows a circuit designed to dim the display from 98% to 2% by pulse width modulating the $\overline{BL}$ input. A logarithmic or a linear potentiometer may be used to adjust the display intensity. However, a logarithmic potentiometer matches the response of the human eye and therefore provides better resolution at low intensities. The circuit frequency should be designed to operate at 10 kHz or higher. Lower frequencies may cause the display to flicker.

Extended Function Disable

Extended Function Disable (bit D_6 of the Control Register) disables the extended blanking and dimming functions in the HDLX-2416. If the Extended Function Disable is a logic 1, the internal brightness control, Master Blank, and Digit Blank Disable bits are ignored. However the $\overline{BL}$ input and Cursor control are still active. This allows downward compatibility to the HPDL-2416.

Mechanical and Electrical Considerations

The HDLX-2416 is an 18 pin DIP package that can be stacked horizontally and vertically to create arrays of any size. The HDLX-2416 is designed to operate continuously from -40°C to + 85°C for all possible input conditions.

The HDLX-2416 is assembled by die attaching and wire bonding 140 LEDs and a CMOS IC to a high temperature printed circuit board. A polycarbonate lens is placed over the PC board creating an air gap environment for the LED wire bonds. Backfill epoxy environmentally seals the display package. This package construction makes the display highly tolerant to temperature cycling and allows wave soldering.

The inputs to the CMOS IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HDLX-2416 should be stored in antistatic tubes or conductive material. During assembly a grounded conductive work area should be used, and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static charge build-up.

Input current latchup is caused when the CMOS inputs are subjected either to a voltage below ground (V_{in} < ground) or to a voltage higher than V_{DD} (V_{in} > V_{DD}) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{DD}. Voltages should not be applied to the inputs until V_{DD} has been applied to the display. Transient input voltages should be eliminated.

Soldering and Post Solder Cleaning Instructions for the HDLX-2416

The HDLX-2416 may be hand soldered or wave soldered with SN63 solder. When hand soldering it is recommended that an electronically temperature controlled and securely grounded soldering iron be used. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux can be used. The solder wave temperature should be set at 245°C ±5°C (473°F ±9°F), and dwell in the wave should be set between 1 1/2 to 3 seconds for optimum soldering. The preheat temperature should not exceed 110°C (230°F) as measured on the solder side of the PC board.

Post solder cleaning may be performed with a solvent or aqueous process. For solvent cleaning, Allied Chemical's Genesolv DES, or DuPont's Freon TE may be used. These solvents are azeotropes of trichlorotrifluroethane FC-113 with low concentrations of ethanol (5%). The maximum exposure time in the solvent vapors at boiling temperature should not exceed 2 minutes. Parts should not be handled until dry and cool. Solvents containing high concentrations of alcohols such as methanol, ketones such as acetone or chlorinated solvent should not

be used as they will chemically attack the polycarbonate lens. Solvents containing trichloroethane FC-111 or FC-112 and trichloroethylene (TCE) are also not recommended.

An aqueous cleaning process may be used. A saponifier, such as Kester bio-kleen Formula 5799 or its equivalent, may be added to the wash cycle of an aqueous process to remove rosin flux residues. Organic acid flux residues must be thoroughly removed by an aqueous cleaning process to prevent corrosion of the leads and solder connections. The optimum water temperature is 60°C (140°F). The maximum cumulative exposure of the HDLX-2416 to wash and rinse cycles should not exceed 15 minutes. For additional information on soldering and post solder cleaning, see Application Note 1027.

Contrast Enhancement

The objective of contrast enhancement is to provide good readability in the end user's ambient lighting conditions. The concept is to employ both luminance and chrominance contrast techniques. These enhance readability by having the OFF-dots blend into the display background and the ON-dots vividly stand out against the same background. Contrast enhancement may be achieved by using one of the following filters listed below. For additional information on contrast enhancement, see Application Note 1015.

HDLR-2416/ HDLU-2416/ HDLS-2416:	Panelgraphic RUBY RED 60 SGL Homalite H100-1605 RED 3M Louvered Filter R6610 RED or N0210 GRAY
HDLO-2416:	Panelgraphic SCARLET RED 65 or GRAY 10 SGL Homalite H100-1670 RED or -1266 GRAY 3M Louvered Filter R6310 RED or N0210 GRAY
HDLA-2416:	Panelgraphic AMBER 23, AMBER 26 or GRAY 10 SGL Homalite H100-1709 AMBER or -1266 GRAY 3M Louvered Filter A6010 or N0210 GRAY
HDLY-2416:	Panelgraphic YELLOW 27 or GRAY 10 SGL Homalite H100-1720 AMBER or -1266 GRAY 3M Louvered Filter A5910 AMBER or N0210 GRAY
HDLG-2416:	Panelgraphic GREEN 48 SGL Homalite H100-1440 GREEN 3M Louvered Filter G5610 GREEN or N0210 GRAY

HEWLETT PACKARD

8 Character 5 mm and 7 mm Smart Alphanumeric Displays

Technical Data

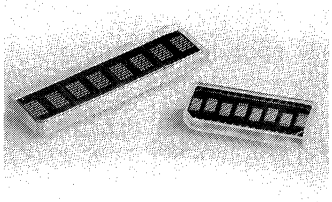
HDSP-211X Series
HDSP-212X Series
New **HDSP-250X Series**

Features

- **X Stackable (HDSP-211X/ -212X)**
- **XY Stackable (HDSP-250X)**
- **128 Character ASCII Decoder or 128 Character Katakana Decoder**
- **Programmable Functions**
- **16 User Definable Characters**
- **Multi-Level Dimming and Blanking**
- **TTL Compatible CMOS IC**
- **Wave Solderable**

Description

The HDSP-211X/-212X/-250X series of products is ideal for applications where displaying eight or more characters of dot matrix information in an aesthetically pleasing manner is required. These devices are 8-digit, 5 x 7 dot matrix, alphanumeric displays and are all packaged in a standard 15.24 mm (0.6 inch) 28 pin DIP. The on-board CMOS IC has the ability to decode 128 ASCII characters (HDSP-211X/-250X) or 128 Katakana characters (HDSP-212X), which are permanently stored in ROM. In addition, 16 programmable symbols may be stored in on-board ROM, allowing considerable flexibility for displaying additional symbols and icons. Seven brightness levels provide versatility in adjusting the display intensity and power consumption. The HDSP-211X/-212X/-250X products are designed for standard microprocessor interface techniques. The display and special features are accessed through a bidirectional 8-bit data bus.



Applications

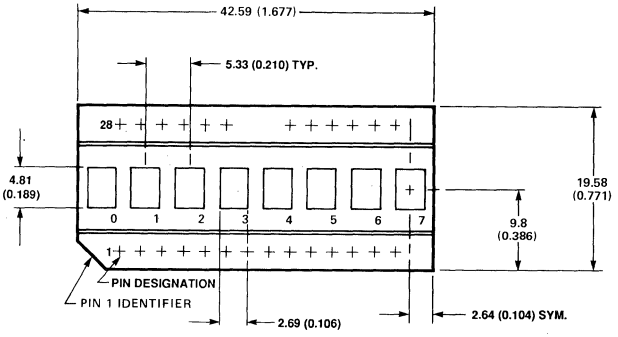
- **Computer Peripherals**
- **Industrial Instrumentation**
- **Medical Equipment**
- **Portable Data Entry Devices**
- **Cellular Phones**
- **Telecommunications Equipment**
- **Test Equipment**

Device Selection Guide

Font Height	Character Set	High Efficiency Red	Orange	Yellow	Green
0.2 inches	ASCII	HDSP-2112	HDSP-2110	HDSP-2111	HDSP-2113
0.2 inches	Katakana*	HDSP-2122	–	HDSP-2121	HDSP-2123
0.27 inches	ASCII	HDSP-2502	HDSP-2500	HDSP-2501	HDSP-2503

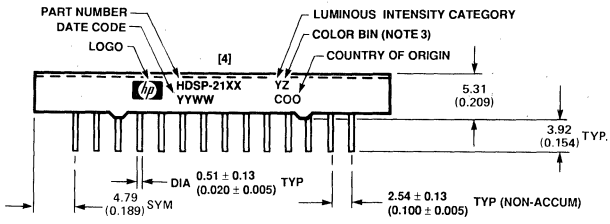
*Katakana is a simplified version of the Japanese alphabet.

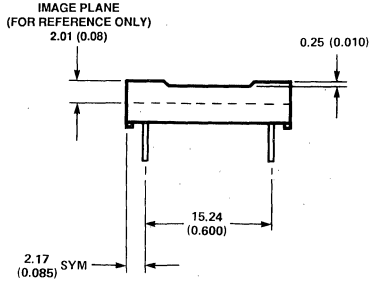
Package Dimensions



Pin Function Assignment Table

Pin No.	Function	Pin No.	Function
1	$\overline{RST}$	15	GND(SUPPLY)
2	$\overline{FL}$	16	GND (LOGIC)
3	A_0	17	$\overline{CE}$
4	A_1	18	$\overline{RD}$
5	A_2	19	D_0
6	A_3	20	D_1
7	DO NOT CONNECT	21	NO PIN
8	DO NOT CONNECT	22	NO PIN
9	DO NOT CONNECT	23	D_2
10	A_4	24	D_3
11	CLS	25	D_4
12	CLK	26	D_5
13	$\overline{WR}$	27	D_6
14	V_{DD}	28	D_7





NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE ON ALL DIMENSIONS IS ± 0.25 mm (0.010 INCH).
3. FOR YELLOW AND GREEN DEVICES ONLY.
4. MARKING IS ON SIDE OPPOSITE PIN 1.

HDSP-21XX

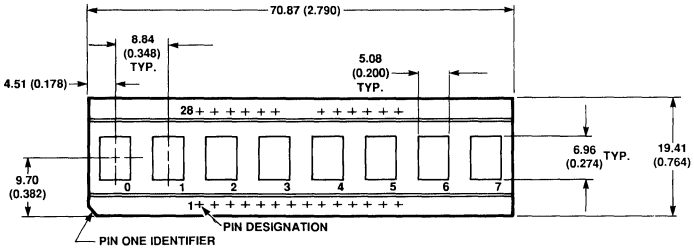
Absolute Maximum Ratings

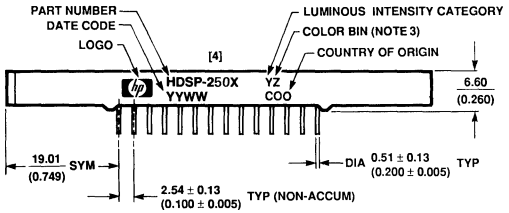
Supply Voltage, V_{DD} to Ground[1] ..... -0.3 to 7.0 V
Operating Voltage, V_{DD} to Ground[2] ..... 5.5 V
Input Voltage, Any Pin to Ground ..... -0.3 to V_{DD} +0.3 V
Free Air Operating Temperature Range, T_A[3] ..... -45°C to +85°C
Storage Temperature Range, T_S ..... -55°C to +100°C
Relative Humidity (non-condensing) 85%
Maximum Solder Temperature
(Below Seating Plane), t < 5 sec ..... 260°C
ESD Protection @ 1.5 kΩ, 100 pF ..... V_Z = 4 kV (each pin)

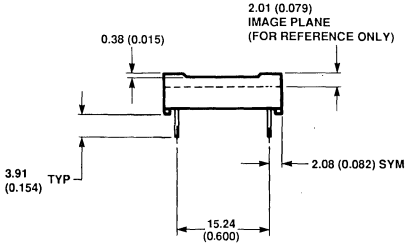
Notes:
1. Maximum Voltage is with no LEDs illuminated.
2. 20 dots ON in all locations at full brightness.
3. Maximum supply voltage is 5.25 V for operation above 70°C.

ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED TO AVOID STATIC DISCHARGE.

Package Dimensions







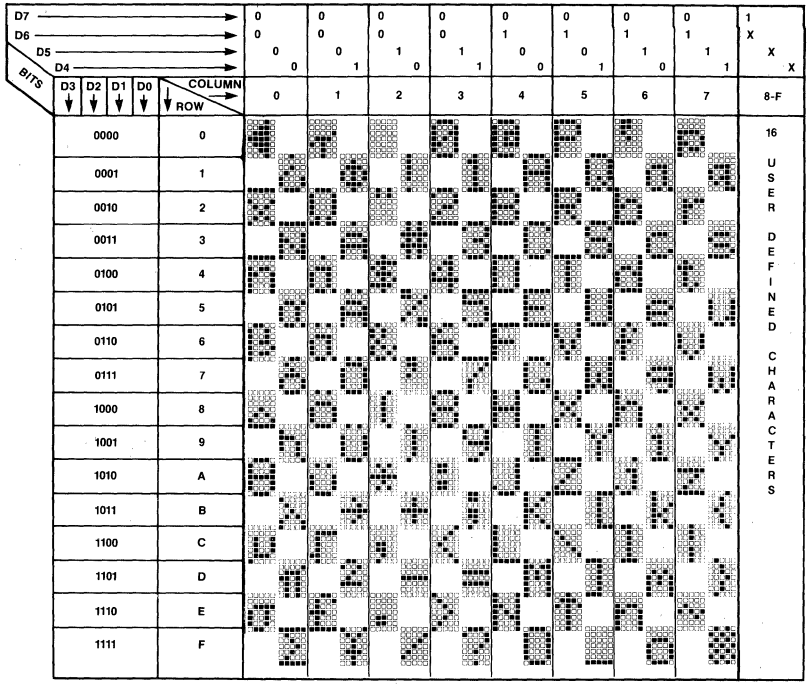
Pin Function Assignment Table

Pin No.	Function	Pin No.	Function
1	$\overline{RST}$	15	GND(SUPPLY)
2	$\overline{FL}$	16	GND (LOGIC)
3	A_0	17	$\overline{CE}$
4	A_1	18	$\overline{RD}$
5	A_2	19	D_0
6	A_3	20	D_1
7	DO NOT CONNECT	21	NO PIN
8	DO NOT CONNECT	22	NO PIN
9	DO NOT CONNECT	23	D_2
10	A_4	24	D_3
11	CLS	25	D_4
12	CLK	26	D_5
13	$\overline{WR}$	27	D_6
14	V_{DD}	28	D_7

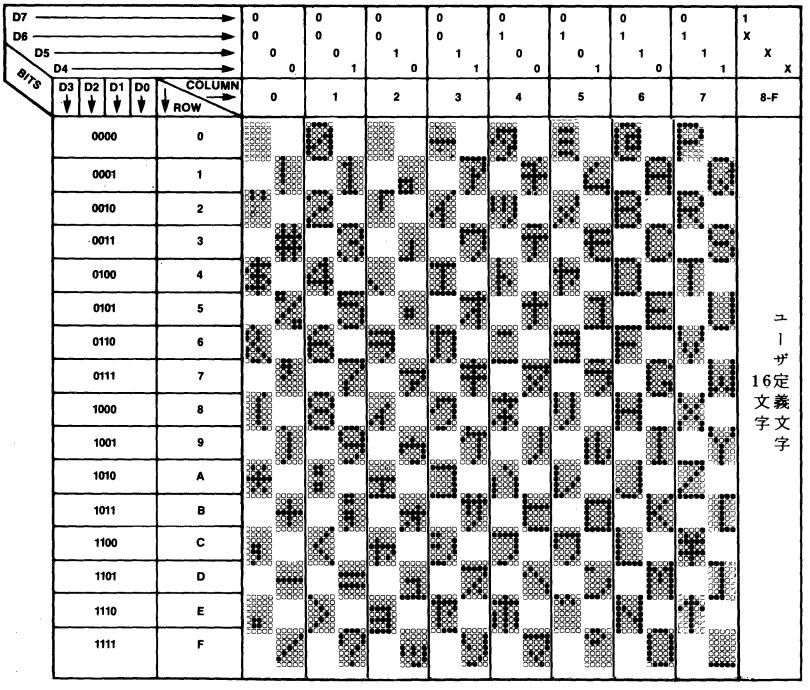
NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE ON ALL DIMENSIONS IS ± 0.25 mm (0.010 INCH).
3. FOR YELLOW AND GREEN DEVICES ONLY.
4. MARKING IS ON SIDE OPPOSITE PIN 1.

HDSP-250X

ASCII Character Set HDSP-211X, HDSP-250X Series



Katakana Character Set HDSP-212X Series



Recommended Operating Conditions

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

Electrical Characteristics Over Operating Temperature Range (-45°C to +85°C)

4.5 V < V_{DD} < 5.5 V, unless otherwise specified

Parameter	Symbol	T_A = 25°C, V_{DD} = 5.0 V		-45°C < T_A < + 85°C, 4.5 V < V_{DD} < 5.5 V		Units	Test Conditions
		Typ.	Max.	Min.	Max.		
Input Leakage (Input without pullup)	I_{IH} I_{IL}				1.0 -1.0	µA	V_{IN} = 0 to V_{DD}, pins CLK, D_0-D_7, A_0-A_4
Input Current (Input with pullup)	I_{IPL}	-11	-18		-30	µA	V_{IN} = 0 to V_{DD}, pins $\overline{CLS}$, $\overline{RST}$, $\overline{WR}$, $\overline{RD}$, $\overline{CE}$, $\overline{FL}$
I_{DD} Blank	I_{DD} (BLK)	0.5	3.0		4.0	mA	V_{IN} = V_{DD}
I_{DD} 8 digits 12 dots/character[1,2]	I_{DD}(V)	200	255		330	mA	"V" on in all 8 locations
I_{DD} 8 digits 20 dots/character[1,2,3,4]	I_{DD}(#)	300	370		430	mA	"#" on in all locations
Input Voltage High	V_{IH}			2.0	V_{DD} +0.3	V	
Input Voltage Low	V_{IL}			GND -0.3 V	0.8	V	
Output Voltage High	V_{OH}			2.4		V	V_{DD} = 4.5 V, I_{OH} = -40 µA
Output Voltage Low D_0-D_7	V_{OL}				0.4	V	V_{DD} = 4.5 V, I_{OL} = 1.6 mA
Output Voltage Low CLK	V_{OL}				0.4	V	V_{DD} = 4.5 V, I_{OL} = 40 µA
High Level Output Current	I_{OH}				-60	mA	V_{DD} = 5.0 V
Low Level Output Current	I_{OL}				50	mA	V_{DD} = 5.0 V
Thermal Resistance IC Junction-to-Case	$R\theta_{J-C}$	15				°C/W	

Notes:
1. Average I_{DD} measured at full brightness. See Table 2 in Control Word Section for I_{DD} at lower brightness levels. Peak I_{DD} = 28/15 x I_{DD} (#).
2. Maximum I_{DD} occurs at -55°C.
3. Maximum I_{DD}(#) = 355 mA at V_{DD} = 5.25 V and IC T_J = 150°C.
4. Maximum I_{DD}(#) = 375 mA at V_{DD} = 5.5 V and IC T_J = 150°C.

Optical Characteristics at 25°C[1]

V_{DD} = 5.0 V at Full Brightness

Description	Part Number	Luminous Intensity Character Average (#) Iv (mcd) Min.	Typ.	Peak Wavelength λ_{Peak} (nm)	Dominant Wavelength λ_d (nm)
HER	HDSP-2112 -2122 -2502	2.5	7.5	635	626
Orange	HDSP-2110 -2500	2.5	7.5	600	602
Yellow	HDSP-2111 -2121 -2501	2.5	7.5	583	585
High Performance Green	HDSP-2113 -2123 -2503	2.5	7.5	568	574

Note: 1. Refers to the initial case temperature of the device immediately prior to measurement.

AC Timing Characteristics Over Temperature Range (-45°C to +85°C)

4.5 V < V_{DD} < 5.5 V, unless otherwise specified

Reference Number	Symbol	Description	Min.[1]	Units
1	t_{ACC}	Display Access Time Write Read	 210 230	 ns
2	t_{ACS}	Address Setup Time to Chip Enable	10	ns
3	t_{CE}	Chip Enable Active Time[2, 3] Write Read	 140 160	 ns
4	t_{ACH}	Address Hold Time to Chip Enable	20	ns
5	t_{CER}	Chip Enable Recovery Time	60	ns
6	t_{CES}	Chip Enable Active Prior to Rising Edge of[2, 3] Write Read	 140 160	 ns
7	t_{CEH}	Chip Enable Hold Time to Rising Edge of Read/Write Signal[2, 3]	0	ns
8	t_W	Write Active Time	100	ns
9	t_{WSU}	Data Write Setup Time	50	ns
10	t_{WH}	Data Write Hold Time	20	ns
11	t_R	Chip Enable Active Prior to Valid Data	160	ns
12	t_{RD}	Read Active Prior to Valid Data	75	ns
13	t_{DF}	Read Data Float Delay	10	ns
	t_{RC}	Reset Active Time[4]	300	ns

Notes:

1. Worst case values occur at an IC junction temperature of 150°C.
2. For designers who do not need to read from the display, the Read line can be tied to V_{DD} and the Write and Chip Enable lines can be tied together.
3. Changing the logic levels of the Address lines when $\overline{CE}$ = "0" may cause erroneous data to be entered into the Character RAM, regardless of the logic levels of the $\overline{WR}$ and $\overline{RD}$ lines.
4. The display must not be accessed until after 3 clock pulses (110 µs min. using the internal refresh clock) after the rising edge of the reset line.

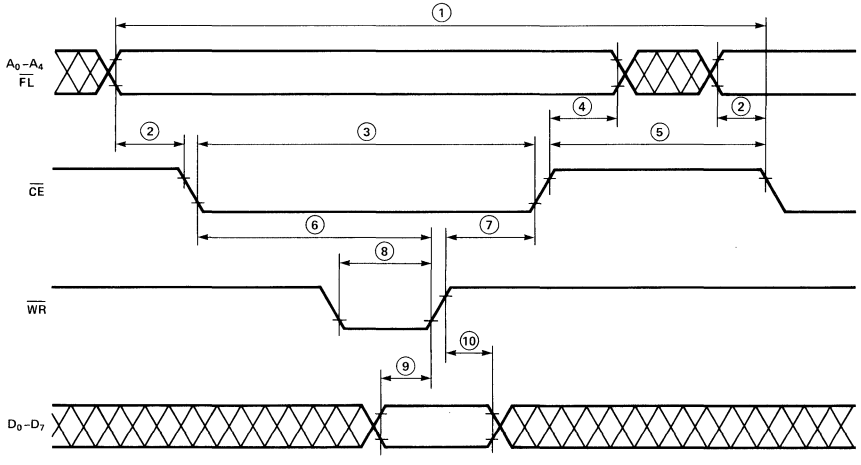
AC Timing Characteristics Over Temperature Range (-45°C to +85°C)

4.5 V < V_{DD} < 5.5 V, unless otherwise specified

Symbol	Description	25°C Typ.	Min.[1]	Units
F_{OSC}	Oscillator Frequency	57	28	kHz
F_{RF}[2]	Display Refresh Rate	256	128	Hz
F_{FL}[3]	Character Flash Rate	2	1	Hz
t_{ST}[4]	Self Test Cycle Time	4.6	9.2	sec

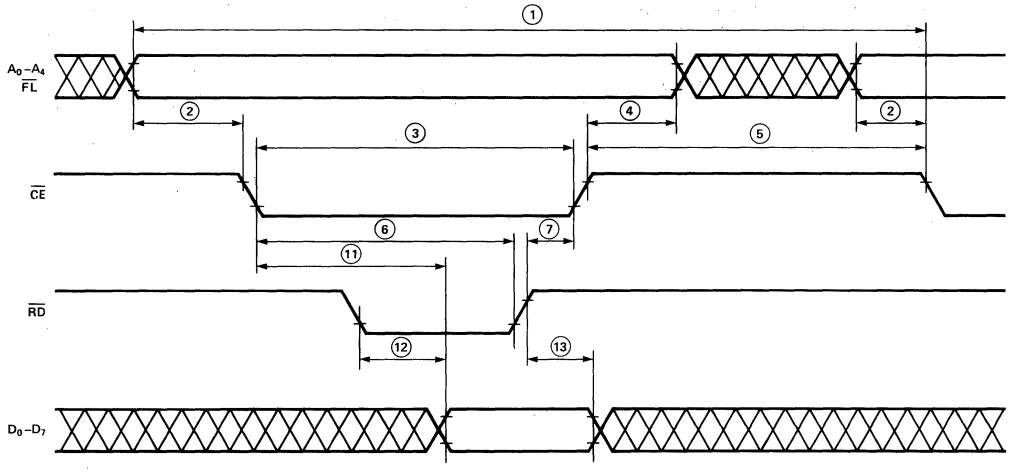
Notes:
1. Worst case values occur at an IC junction temperature of 150°C.
2. $F_{RF} = F_{OSC}/224$
3. $F_{FL} = F_{OSC}/28,672$
4. $t_{ST} = 262,144/F_{OSC}$

Write Cycle Timing Diagram



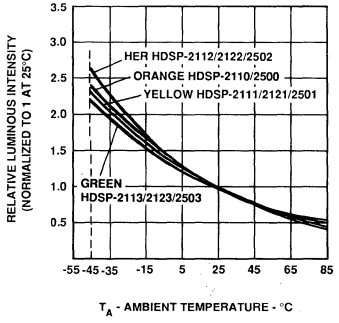
INPUT PULSE LEVELS – 0.6 V TO 2.4 V

Read Cycle Timing Diagram



INPUT PULSE LEVELS: 0.6 V TO 2.4 V
OUTPUT REFERENCE LEVELS: 0.6 V TO 2.2 V
OUTPUT LOADING = 1 TTL LOAD AND 100pFd

Relative Luminous Intensity vs. Temperature



Electrical Description

Pin Function	Description
RESET ($\overline{RST}$, pin 1)	Initializes the display.
FLASH ($\overline{FL}$, pin 2)	$\overline{FL}$ low indicates an access to the Flash RAM and is unaffected by the state of address lines A_3-A_4.
ADDRESS INPUTS (A_0-A_4, pins 3-6, 10)	Each location in memory has a distinct address. Address inputs (A_0-A_2) select a specific location in the Character RAM, the Flash RAM or a particular row in the UDC (User-Defined Character) RAM. A_3-A_4 are used to select which section of memory is accessed. Table 1 shows the logic levels needed to access each section of memory.

Table 1. Logic Levels to Access Memory

Section of Memory	$\overline{FL}$	A_4	A_3	A_2 A_1 A_0
Flash RAM	0	X	X	Char. Address
UDC Address Register	1	0	0	Don't Care
UDC RAM	1	0	1	Row Address
Control Word Register	1	1	0	Don't Care
Character RAM	1	1	1	Character Address

CLOCK SELECT (CLS, pin 11)	Used to select either an internal or external clock source.
CLOCK INPUT/OUTPUT (CLK, pin 12)	Outputs the master clock (CLS = 1) or inputs a clock (CLS = 0) for slave displays.
WRITE ($\overline{WR}$, pin 13)	Data is written into the display when the $\overline{WR}$ input is low and the $\overline{CE}$ input is low.
CHIP ENABLE ($\overline{CE}$, pin 17)	Must be at a logic low to read or write data to the display and must go high between each read and write cycle.
READ ($\overline{RD}$, pin 18)	Data is read from the display when the $\overline{RD}$ input is low and the $\overline{CE}$ input is low.
DATA Bus (D_0-D_7, pins 19, 20, 23-28)	Used to read from or write to the display.
GND (SUPPLY) (pin 15)	Analog ground for the LED drivers.
GND (LOGIC) (pin 16)	Digital ground for internal logic.
V_{DD} (POWER) (pin 14)	Positive power supply input.

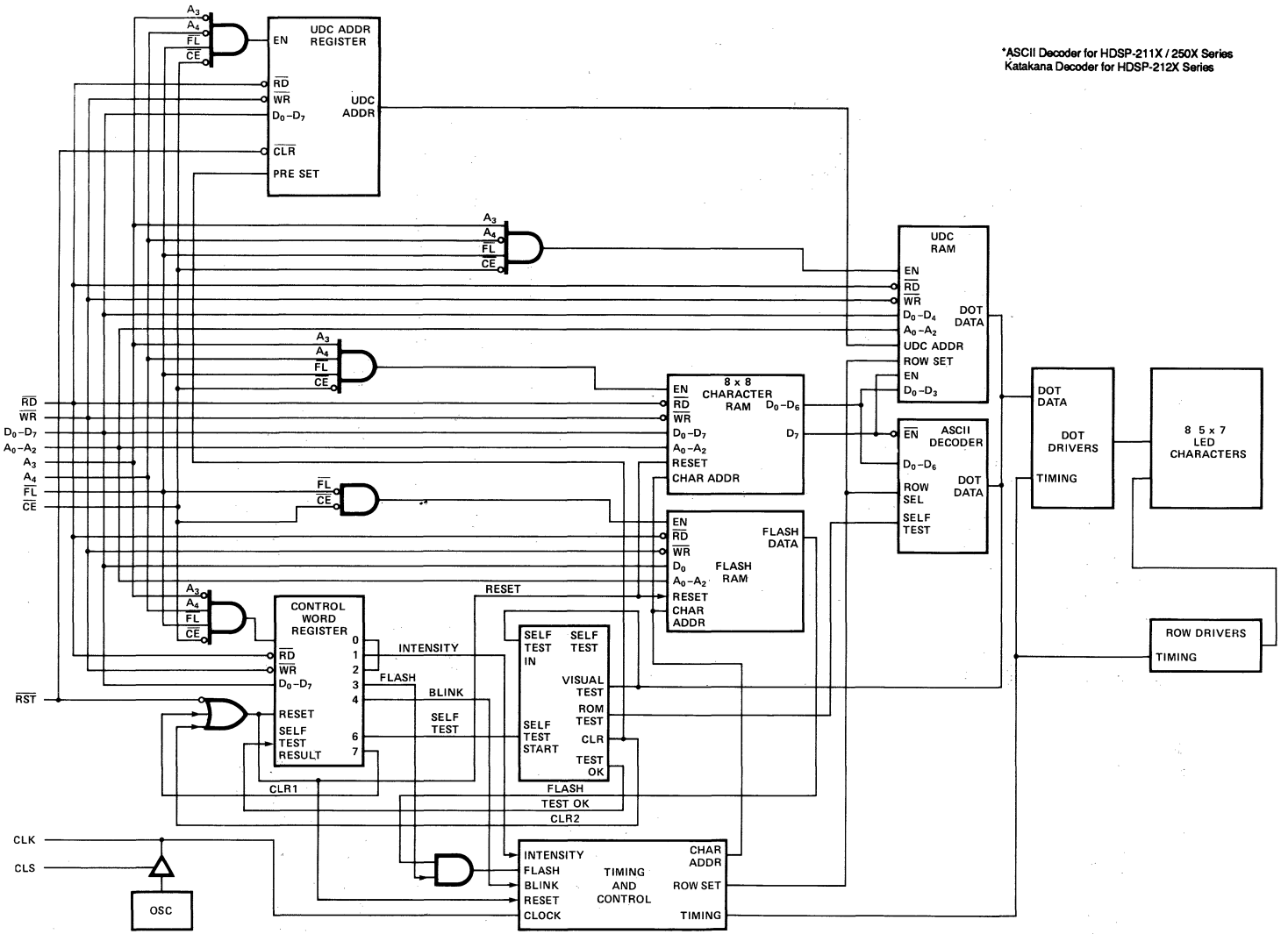


Figure 1. HDSP-211X/-212X/-250X Internal Block Diagram.

Display Internal Block Diagram

Figure 1 shows the internal block diagram of the HDSP-211X/-212X/-250X displays. The CMOS IC consists of an 8 byte Character RAM, an 8 bit Flash RAM, a 128 character ASCII (Katakana) decoder, a 16 character UDC RAM, a UDC Address Register, a Control Word Register, and refresh circuitry necessary to synchronize the decoding and driving of eight 5 x 7 dot matrix characters. The major user-accessible portions of the display are listed below:

Character RAM	This RAM stores either ASCII (Katakana) character data or a UDC RAM address.
Flash RAM	This is a 1 x 8 RAM which stores Flash data.
User-Defined Character RAM (UDC RAM)	This RAM stores the dot pattern for custom characters.
User-defined Character Address Register (UDC Address Register)	This register is used to provide the address to the UDC RAM when the user is writing or reading a custom character.
Control Word Register	This register allows the user to adjust the display brightness, flash individual characters, blink, self test, or clear the display.

Character Ram

Figure 2 shows the logic levels needed to access the HDSP-211X/-212X/-250X Character RAM. During a normal access, the $\overline{CE}$ = "0" and either $\overline{RD}$ = "0" or $\overline{WR}$ = "0". However, erroneous data may be written into the Character RAM if the address lines are unstable when $\overline{CE}$ = "0" regardless of the logic levels of the $\overline{RD}$ or $\overline{WR}$ lines. Address lines A_0-A_2 are used to select the location in the Character RAM. Two types of data can be stored in each Character RAM location: an ASCII (Katakana) code or a UDC RAM address. Data bit D_7 is used to differentiate between the ASCII (Katakana) character and a UDC RAM address. D_7 = 0 enables the ASCII (Katakana) decoder and D_7 = 1 enables the UDC RAM. D_0-D_6 are used to input ASCII (Katakana) data and D_0-D_3 are used to input a UDC address.

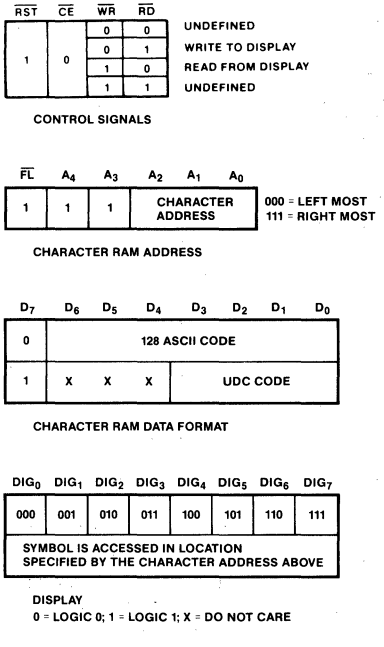


Figure 2. Logic Levels to Access the Character RAM.

UDC RAM and UDC Address Register

Figure 3 shows the logic levels needed to access the UDC RAM and the UDC Address Register. The UDC Address Register is eight bits wide. The lower four bits (D_0-D_3) are used to select one of the 16 UDC locations. The upper four bits (D_4-D_7) are not used. Once the UDC address has been stored in the UDC Address Register, the UDC RAM can be accessed.

To completely specify a 5 x 7 character, eight write cycles are required. One cycle is used to store the UDC RAM address in the UDC Address Register and seven cycles are used to store dot data in the UDC RAM. Data is entered by rows and one cycle is needed to access each row. Figure 4 shows the organization of a UDC character assuming the symbol to be stored is an "F". A_0-A_2 are used to select the row to be accessed and D_0-D_4 are used to transmit the row dot data. The upper three bits (D_5-D_7) are ignored. D_0 (least significant bit) corresponds to the right most column of the 5 x 7 matrix and D_4 (most significant bit) corresponds to the left most column of the 5 x 7 matrix.

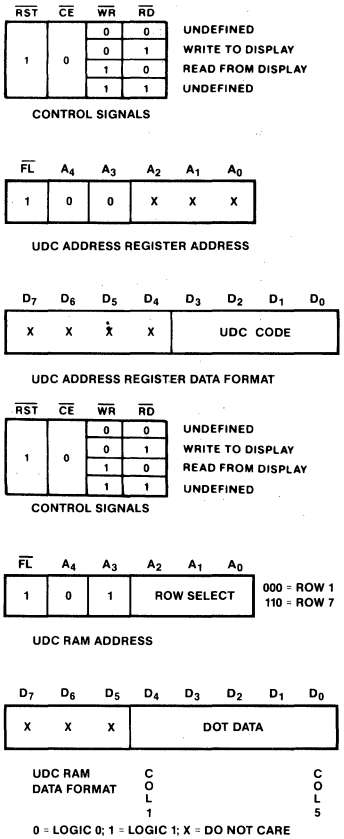


Figure 3. Logic Levels to Access a UDC Character.

COL 1	COL 2	COL 3	COL 4	COL 5		UDC CHARACTER	HEX CODE
D_4	D_3	D_2	D_1	D_0			
1	1	1	1	1	ROW 1	* * * * *	1F
1	0	0	0	0	ROW 2	*	10
1	0	0	0	0	ROW 3	*	10
1	1	1	1	0	ROW 4	* * * *	1D
1	0	0	0	0	ROW 5	*	10
1	0	0	0	0	ROW 6	*	10
1	0	0	0	0	ROW 7	*	10

IGNORED

0 = LOGIC 0; 1 = LOGIC 1; * = ILLUMINATED LED.

Figure 4. Data to Load "F" into the UDC RAM.

Flash RAM

Figure 5 shows the logic levels needed to access the Flash RAM. The Flash RAM has one bit associated with each location of the Character RAM. The Flash input is used to select the Flash RAM while address lines A_3-A_4 are ignored. Address lines A_0-A_2 are used to select the location in the Flash RAM to store the attribute. D_0 is used to store or remove the flash attribute. D_0 = "1" stores the attribute and D_0 = "0" removes the attribute.

When the attribute is enabled through bit 3 of the Control Word and a "1" is stored in the Flash RAM, the corresponding character will flash at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock the flash rate can be calculated by dividing the clock frequency by 28,672.

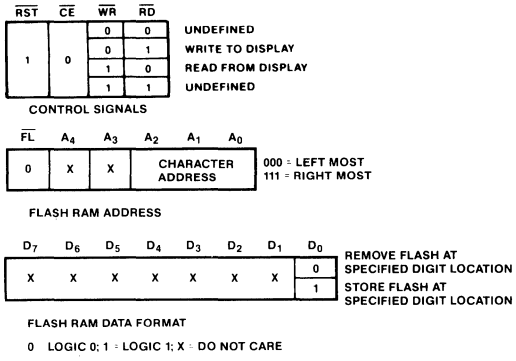


Figure 5. Logic Levels to Access the Flash RAM.

Control Word Register

Figure 6 shows how to access the Control Word Register. This 8-bit register performs five functions: Brightness control, Flash RAM control, Blinking, Self Test, and Clear. Each function is independent of the others; however, all bits are updated during each Control Word write cycle.

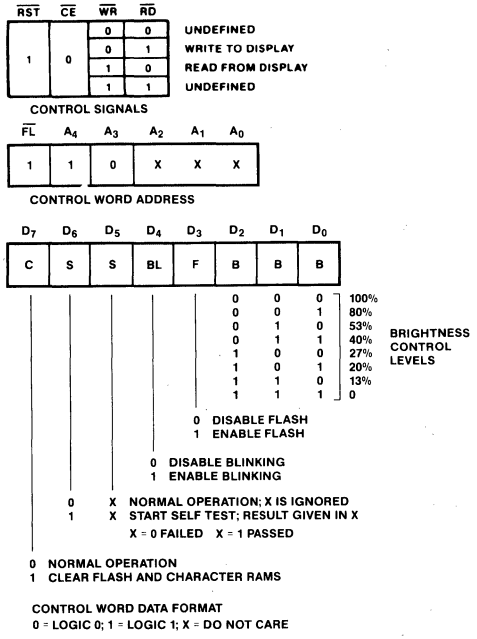


Figure 6. Logic Levels to Access the Control Word Register

Brightness (Bits 0-2)

Bits 0-2 of the Control Word adjust the brightness of the display. Bits 0-2 are interpreted as a three bit binary code with code (000) corresponding to maximum brightness and code (111) corresponding to a blanked display. In addition to varying the display brightness, bits 0-2 also vary the average value of I_{DD}. I_{DD} can be calculated at any brightness level by multiplying the percent brightness level by the value of I_{DD} at the 100% brightness level. These values of I_{DD} are shown in Table 2.

Table 2. Current Requirements at Different Brightness Levels V_{DD} = 5.0 V

Symbol	D_2	D_1	D_0	% Brightness	Current at 25°C Typ.	Units
I_{DD} (V)	0	0	0	100	200	mA
	0	0	1	80	160	mA
	0	1	0	53	106	mA
	0	1	1	40	80	mA
	1	0	0	27	54	mA
	1	0	1	20	40	mA
	1	1	0	13	26	mA

Flash Function (Bit 3)

Bit 3 determines whether the flashing character attribute is on or off. When bit 3 is a "1", the output of the Flash RAM is checked. If the content of a location in the Flash RAM is a "1", the associated digit will flash at approximately 2 Hz. For an external clock, the blink rate can be calculated by driving the clock frequency by 28,672. If the flash enable bit of the Control Word is a "0", the content of the Flash RAM is ignored. To use this function with multiple display systems, see the Display Reset section.

Blink Function (Bit 4)

Bit 4 of the Control Word is used to synchronize blinking of all eight digits of the display. When this bit is a "1" all eight digits of the display will blink at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock, the blink rate can be calculated by dividing the clock frequency by 28,672. This function will override the Flash function when it is active. To use this function with multiple display systems, see the Display Reset section.

Self Test Function (Bits 5, 6)
Bit 6 of the Control Word Register is used to initiate the self test function. Results of the internal self test are stored in bit 5 of the Control Word. Bit 5 is a read only bit where bit 5 = "1" indicates a passed self test and bit 5 = "0" indicates a failed self test.

Setting bit 6 to a logic 1 will start the self test function. The built-in self test function of the IC consists of two internal routines which exercise major portions of the IC and illuminate all of the LEDs. The first routine cycles the ASCII (Katakana) decoder ROM through all states and performs a checksum on the output. If the checksum agrees with the correct value, bit 5 is set to "1". The second routine provides a visual test of the LEDs using the drive circuitry. This is accomplished by writing checkered and inverse checkered patterns to the display. Each pattern is displayed for approximately 2 seconds.

During the self test function the display must not be accessed. The time needed to execute the self test function is calculated by multiplying the clock period by 262,144. For example, assume a clock frequency of 58 KHz, then the time to execute the self test function frequency is equal to (262,144/58,000) = 4.5 second duration.

At the end of the self test function, the Character RAM is loaded with blanks, the Control Word Register is set to zeros except for bit 5, the Flash RAM is cleared, and the UDC Address Register is set to all ones.

Clear Function (Bit 7)
Bit 7 of the Control Word will clear the Character RAM and the Flash RAM. Setting bit 7 to a "1" will start the clear function. Three clock cycles (110 µs minimum using the internal refresh clock) are required to complete the clear function. The display must not be accessed while the display is being cleared. When the clear function has been completed, bit 7 will be reset to a "0". The ASCII (Katakana) character code for a space (20H) will be loaded into the Character RAM to blank the display and the Flash RAM will be loaded with "0"s. The UDC RAM, UDC Address Register, and the remainder of the Control Word are unaffected.

Display Reset

Figure 7 shows the logic levels needed to Reset the display. The display should be Reset on Power-up. The external Reset clears the Character RAM, Flash RAM, Control Word and resets the internal counters. After the rising edge of the Reset signal, three clock cycles (110 µs minimum using the internal refresh clock) are required to complete the reset sequence. The display must not be accessed while the display is being reset. The ASCII (Katakana) Character code for a space (20H) will be loaded into the Character RAM to blank the display. The Flash RAM and Control Word Register are loaded with all "0"s. The UDC RAM and UDC Address Register are unaffected. All displays which operate with the same clock source must be simultaneously reset to synchronize the Flashing and Blinking functions.

$\overline{RST}$	$\overline{CE}$	$\overline{WR}$	$\overline{RD}$	$\overline{FL}$	A_4-A_0	D_7-D_0
0	1	X	X	X	X	X

0 = LOGIC 0; 1 = LOGIC 1; X = DO NOT CARE

NOTE:
IF RST, CE AND WR ARE LOW, UNKNOWN DATA MAY BE WRITTEN INTO THE DISPLAY.

Figure 7. Logic Levels to Reset the Display.

Mechanical and Electrical Considerations

The HDSP-211X/-212X/-250X are 28 pin dual-in-line packages with 26 external pins. The devices can be stacked horizontally and vertically to create arrays of any size. The HDSP-211X/212X/250X are designed to operate continuously from -45°C to +85°C with a maximum of 20 dots on per character at 5.25 V. Illuminating all thirty-five dots at full brightness is not recommended.

The HDSP-211X/-212X/250X are assembled by die attaching and wire bonding 280 LED chips and a CMOS IC to a thermally conductive printed circuit board. A polycarbonate lens is placed over the PC board creating an air gap over the LED wire bonds. A protective cap creates an air gap over the CMOS IC. Backfill epoxy environmentally seals the display package. This package construction makes the display highly tolerant to temperature cycling and allows wave soldering.

The inputs to the IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HDSP-211X/-212X/250X should be stored in antistatic tubes or

in conductive material. During assembly, a grounded conductive work area should be used, and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static buildup. Input current latchup is caused when the CMOS inputs are subjected to either a voltage below ground (V_{IN} < ground) or to a voltage higher than V_{DD} (V_{IN} > V_{DD}) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{DD}. Voltages should not be applied to the inputs until V_{DD} has been applied to the display.

Thermal Considerations

The HDSP-211X/-212X/250X have been designed to provide a low thermal resistance path for the CMOS IC to the 26 package pins. Heat is typically conducted through the traces of the printed circuit board to free air. For most applications no additional heatsinking is required.

Measurements were made on a 32 character display string to determine the thermal resistance of the display assembly. Several display boards were constructed using .062. in. thick printed circuit material, and one ounce copper .020 in. traces. Some of the device pins were connected to a heatsink formed by etching a copper area on the printed circuit board surrounding the display. A maximally metalized printed circuit board was also evaluated. The junction temperature was measured for displays soldered directly to these PC boards, displays installed in sockets, and finally displays installed in sockets with a filter over the display to restrict airflow. The results of these thermal resistance measurements, $R\theta_{J-A}$ are shown in Table 3 and include the effects of $R\theta_{J-C}$.

Ground Connections

Two ground pins are provided to keep the internal IC logic ground clean. The designer can, when necessary, route the analog ground for the LED drivers separately from the logic ground until an appropriate ground plane is available. On long interconnections between the display and the host system, the designer can keep voltage drops on the analog ground from affecting the display logic levels by isolating the two grounds.

The logic ground should be connected to the same ground potential as the logic interface circuitry. The analog ground and the logic ground should be connected at a common ground which can withstand the current introduced by the switching LED drivers. When separate ground connections are used, the analog ground can vary from -0.3 V to +0.3 V with respect to the logic ground. Voltage below -0.3 V can cause all dots to be on. Voltage above +0.3 V can cause dimming and dot mismatch.

Soldering and Post Solder Cleaning Instructions for the HDSP-211X/-212X/-250X

The HDSP-211X/-212X/-250X may be hand soldered or wave soldered with SN63 solder. When hand soldering, it is recommended that an electronically temperature controlled and securely grounded soldering iron be used. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux can be used. The solder wave temperature should be set at 245°C ± 5°C (473°F ± 9°F), and the dwell in the wave should be set between 1-1/2 to 3 seconds for optimum soldering. The preheat temperature should not exceed 105°C (221°F) as measured on the solder side of the PC board.

Post solder cleaning may be performed with a solvent or aqueous process. For solvent cleaning, Allied Chemical's Genesolv DES, Baron Blakeslee's Blaco-Tron TES or DuPont's Freon TE may be

Table 3. Thermal Resistance, θ_{JA}, Using Various Amounts of Heatsinking Material

Heatsinking Metal per Device sq. in.	W/Sockets W/O Filter (Avg.)	W/O Sockets W/O Filter (Avg.)	W/Sockets W/Filter (Avg.)	Units
0	31	30	35	°C/W
1	31	28	33	°C/W
3	30	26	33	°C/W
Max. Metal	29	25	32	°C/W
4 Board Avg	30	27	33	°C/W

used. These solvents are azeotropes of trichlorotrifluoroethane FC-113 with low concentrations of ethanol (5%). The maximum exposure time in the solvent vapors at boiling temperature should not exceed 2 minutes. Solvents containing high concentrations of alcohols such as methanol, ketones such as acetone, or chlorinated solvents should not be used as they will chemically attack the polycarbonate lens. Solvents containing trichloroethylene (TCE), FC-111, FC-112, or trichloroethylane (TCA) are also not recommended.

An aqueous cleaning process may be used. A saponifier, such as Kesterbio-kleen Formula 5799 or its equivalent, may be added to the wash cycle of an aqueous process to remove rosin flux residues. Organic acid flux residues must be thoroughly removed by an aqueous cleaning process to prevent corrosion of the leads and solder connections. The optimum water temperature is 60°C (140°F). The maximum cumulative exposure of the HDSP-211X/-212X/-250X to wash and rinse cycles should not exceed 15 minutes. For additional information on soldering and post solder cleaning, see Application Note 1027, *Soldering LED Components.*

Contrast Enhancement

The objective of contrast enhancement is to provide good readability in a variety of ambient lighting conditions. For information on contrast enhancement see Application Note 1015, *Contrast Enhancement Techniques for LED Displays.*

HEWLETT PACKARD

New

8 Character 5mm Smart Alphanumeric Displays

HDSP-253X Series

Features

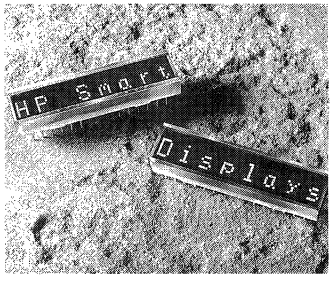
- **XY Stackable**
- **128 Character ASCII Decoder**
- **Programmable Functions**
- **16 User Definable Characters**
- **Multi-Level Dimming and Blanking**
- **TTL Compatible CMOS IC**
- **Wave Solderable**

Applications

- **Avionics**
- **Computer Peripherals**
- **Industrial Instrumentation**
- **Medical Equipment**
- **Portable Data Entry Devices**
- **Telecommunications**
- **Test Equipment**

Description

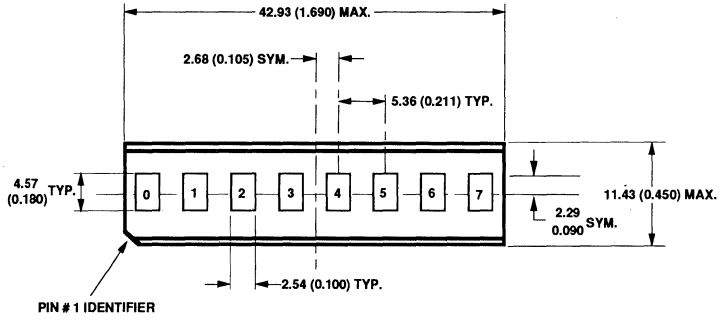
The HDSP-253X is ideal for applications where displaying eight or more characters of dot matrix information in an aesthetically pleasing manner is required. These devices are eight-digit, 5 x 7 dot matrix, alphanumeric displays. The 5.0 mm (0.2 inch) high characters are packaged in a 0.300 mm (7.62 inch) 30 pin DIP. The on-board CMOS IC has the ability to decode 128 ASCII characters, which are permanently stored in ROM. In addition, 16 programmable symbols may be stored in on-board RAM. Seven brightness levels provide versatility in adjusting the display intensity and power consumption. The HDSP-253X is designed for standard microprocessor interface techniques. The display and special features are accessed through a bidirectional eight-bit data bus.



Device Selection Guide

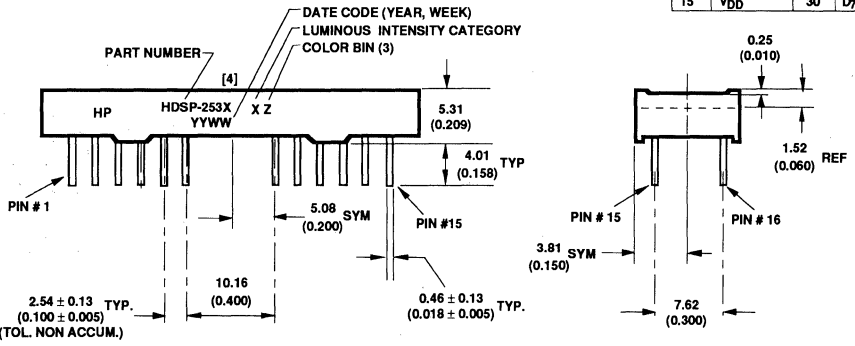
AlGaAs Red	HER	Orange	Yellow	Green
HDSP-2534	HDSP-2532	HDSP-2530	HDSP-2531	HDSP-2533

Package Dimensions



PIN FUNCTION ASSIGNMENT TABLE

PIN #	FUNCTION	PIN #	FUNCTION
1	$\overline{RST}$	16	GND (SUPPLY)
2	$\overline{FL}$	17	THERMAL TEST
3	A_0	18	GND (LOGIC)
4	A_1	19	$\overline{RD}$
5	A_2	20	D_0
6	A_3	21	D_1
7	NO PIN	22	NO PIN
8	NO PIN	23	NO PIN
9	NO PIN	24	NO PIN
10	A_4	25	D_2
11	CLS	26	D_3
12	CLK	27	D_4
13	$\overline{WR}$	28	D_5
14	$\overline{CE}$	29	D_6
15	V_{DD}	30	D_7



NOTES:
1. DIMENSIONS ARE IN MM (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE ON DIMENSIONS IS ± 0.25 MM (0.010 IN.).
3. FOR YELLOW AND GREEN DISPLAYS ONLY.
4. MARKING IS ON SIDE OPPOSITE PIN 1.

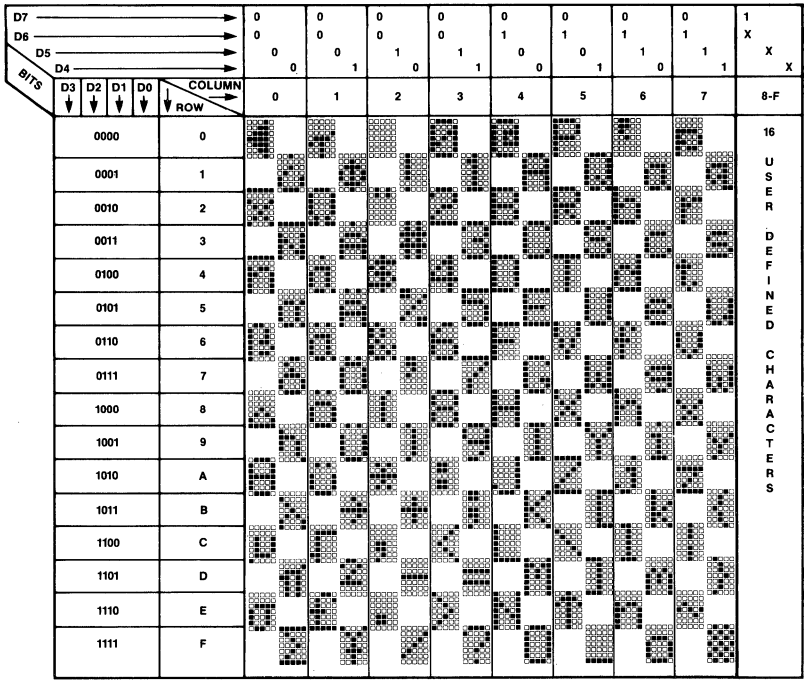
Absolute Maximum Ratings

Supply Voltage, V_{DD} to Ground[1] ..... -0.3 V to 7.0 V
Operating Voltage, V_{DD} to Ground[2] ..... 5.5 V
Input Voltage, Any pin to Ground ..... -0.3 V to V_{DD} +0.3 V
Free Air Operating Temperature Range, T_A[3] ..... -40°C to + 85°C
Relative Humidity (non-condensing) 85%
Storage Temperature Range, T_S ..... -55°C to 100°C
Maximum Solder Temperature
1.59 mm (0.063 in.) Below Seating Plane, t< 5 sec. ..... 260°C
ESD Protection @ 1.5 kΩ, 100 pF ..... 4 k V (each pin)

Notes:
1. Maximum Voltage is with no LEDs illuminated.
2. 20 dots ON in all locations at full brightness.
3. See Thermal Considerations section for information about operation in high temperature ambients.

ESD WARNING: NORMAL CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED TO AVOID STATIC DISCHARGE.

ASCII Character Set



Optical Characteristics at 25°C[1]

V_{DD} = 5.0 V at Full Brightness

LED Color	Part Number	Luminous Intensity Character Average (#) I_V (mcd) Min.	Luminous Intensity Character Average (#) I_V (mcd) Typ.	Peak Wavelength λ_{PEAK} (nm) Typ.	Dominant Wavelength[2] λ_d (nm) Typ.
AlGaAs Red	HDSP-2534	5.1	25	645	637
High Eff. Red	HDSP-2532	2.5	7.5	635	626
Orange	HDSP-2530	2.5	7.5	600	602
Yellow	HDSP-2531	2.5	7.5	583	585
Green	HDSP-2533	2.5	7.5	568	574

Notes:

1. Refers to the initial case temperature of the device immediately prior to measurement.
2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.

Recommended Operating Conditions

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

Electrical Characteristics Over Operating Temperature Range

4.5 < V_{DD} < 5.5 (unless otherwise specified)

Parameter	Symbol	Min.	25°C Typ.[1]	25°C Max.[1]	Max.	Units	Test Conditions
Input Leakage (Input without pull-up)	I_I	-1.0			1.0	µA	V_{IN} = 0 to V_{DD}, pins CLK, D_0-D_7, A_0-A_4
Input Current (Input with pull-up)	I_{IP}	-30	-11	-18	0	µA	V_{IN} = 0 to V_{DD}, pins $\overline{CLS}$, $\overline{RST}$, $\overline{WR}$, $\overline{RD}$, $\overline{CE}$, $\overline{FL}$
I_{DD} Blank	$I_{DD}(BL)$		0.5	3.0	4.0	mA	V_{IN} = V_{DD}
I_{DD} 8 digits 12 dots/char[2,3,4] (AlGaAs)	$I_{DD}(V)$		230	295	390	mA	"V" on in all 8 locations
I_{DD} 8 digits 20 dots/char[2,3,4] (AlGaAs)	$I_{DD}(\#)$		330	410	480	mA	"#" on in all 8 locations
I_{DD} 8 digits 12 dots/char[2,3,4] (all colors except AlGaAs)	$I_{DD}(V)$		200	255	330	mA	"V" on in all 8 locations
I_{DD} 8 digits 20 dots/char[2,3,4] (all colors except AlGaAs)	$I_{DD}(\#)$		300	370	430	mA	"#" on in all 8 locations
Input Voltage High	V_{IH}	2.0			V_{DD} +0.3 V	V	
Input Voltage Low	V_{IL}	GND -0.3 V				V	
Output Voltage High	V_{OH}	2.4				V	V_{DD} = 4.5 V, I_{OH} = -40 µA
Output Voltage Low D_0-D_7	V_{OL}				0.4	V	V_{DD} = 4.5 V, I_{OL} = 1.6 mA
Output Voltage Low CLK	V_{OL}				0.4	V	V_{DD} = 4.5 V, I_{OL} = 40 µA
Thermal Resistance IC Junction-to-PIN	$R\theta_{J\text{-}PIN}$		16			°C/W	Measured at pin 17

Notes:

1. V_{DD} = 5.0 V.
2. See Thermal Considerations Section for information about operation in high temperature ambients.
3. Average I_{DD} measured at full brightness. See Table 2 in Control Word Section for I_{DD} at lower brightness levels. Peak I_{DD} = 28/15 x $I_{DD}(\#)$.
4. Maximum I_{DD} occurs at -55°C.

AC Timing Characteristics Over Temperature Range

V_{DD} = 4.5 to 5.5 V unless otherwise specified.

Reference Number	Symbol	Description	Min.[1]	Units
1	t_{ACC}	Display Access Time Write Read	 210 230	 ns
2	t_{ACS}	Address Setup Time to Chip Enable	10	ns
3	t_{CE}	Chip Enable Active Time[2, 3] Write Read	 140 160	 ns
4	t_{ACH}	Address Hold Time to Chip Enable	20	ns
5	t_{CER}	Chip Enable Recovery Time	60	ns
6	t_{CES}	Chip Enable Active Prior to Rising Edge of[2, 3] Write Read	 140 160	 ns
7	t_{CEH}	Chip Enable Hold Time to Rising Edge of Read/Write Signal[2, 3]	0	ns
8	t_W	Write Active Time	100	ns
9	t_{WD}	Data Valid Prior to Rising Edge of Write Signal	50	ns
10	t_{DH}	Data Write Hold Time	20	ns
11	t_R	Chip Enable Active Prior to Valid Data	160	ns
12	t_{RD}	Read Active Prior to Valid Data	75	ns
13	t_{DF}	Read Data Float Delay	10	ns
	t_{RC}	Reset Active Time[4]	300	ns

Notes:

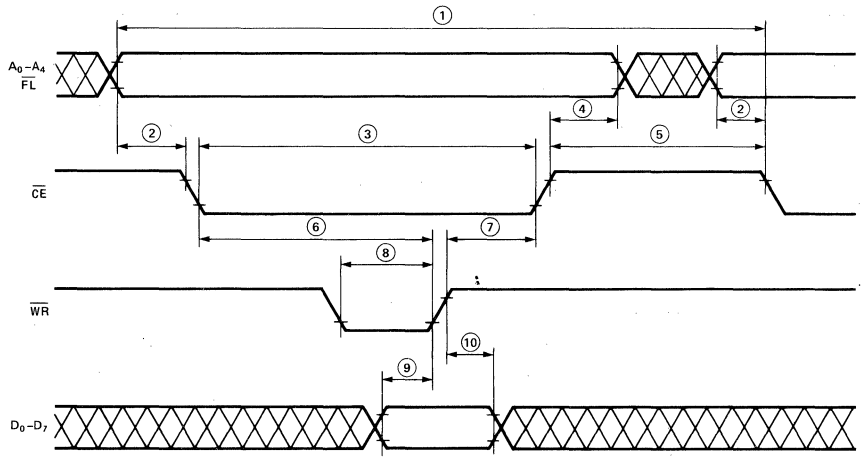
1. Worst case values occur at an IC junction temperature of 125°C.
2. For designers who do not need to read from the display, the Read line can be tied to V_{DD} and the Write and Chip Enable lines can be tied together.
3. Changing the logic levels of the Address lines when $\overline{CE}$ = "0" may cause erroneous data to be entered into the Character RAM, regardless of the logic levels of the $\overline{WR}$ and $\overline{RD}$ lines.
4. The display must not be accessed until after 3 clock pulses (110 µs min. using the internal refresh clock) after the rising edge of the reset line.

Symbol	Description	25°C Typical	Minimum[1]	Units
F_{OSC}	Oscillator Frequency	57	28	kHz
F_{RF}[5]	Display Refresh Rate	256	128	Hz
F_{FL}[6]	Character Flash Rate	2	1	Hz
t_{ST}[7]	Self Test Cycle Time	4.6	9.2	sec

Notes:

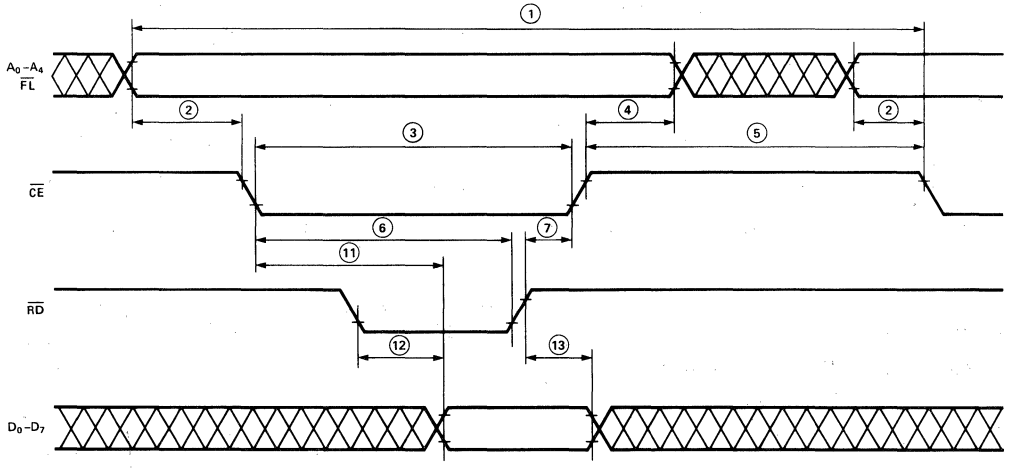
5. $F_{RF} = F_{OSC}/224$.
6. $F_{FL} = F_{OSC}/28{,}672$.
7. $t_{ST} = 262{,}144/F_{OSC}$.

Write Cycle Timing Diagram



INPUT PULSE LEVELS – 0.6 V TO 2.4 V

Read Cycle Timing Diagram



INPUT PULSE LEVELS: 0.6 V TO 2.4 V
OUTPUT REFERENCE LEVELS: 0.6 V TO 2.2 V
OUTPUT LOADING = 1 TTL LOAD AND 100pF

Electrical Description

Pin Function	Description
RESET ($\overline{RST}$, pin 1)	Reset initializes the display.
FLASH ($\overline{FL}$, pin 2)	$\overline{FL}$ low indicates an access to the Flash RAM and is unaffected by the state of address lines A_3-A_4.
ADDRESS INPUTS (A_0-A_4, pins 3-6, 10)	Each location in memory has a distinct address. Address inputs (A_0-A_2) select a specific location in the Character RAM, the Flash RAM or a particular row in the UDC (User-Defined Character) RAM. A_3-A_4 are used to select which section of memory is accessed. Table 1 shows the logic levels needed to access each section of memory.

Table 1. Logic Levels to Access Memory

$\overline{FL}$	A_4	A_3	Section of Memory	A_2 A_1 A_0
0	X	X	Flash RAM	Character Address
1	0	0	UDC Address Register	Don't Care
1	0	1	UDC RAM	Row Address
1	1	0	Control Word Register	Don't Care
1	1	1	Character RAM	Character Address

CLOCK SELECT (CLS, pin 11)	This input is used to select either an internal or external clock source.
CLOCK INPUT/OUTPUT (CLK, pin 12)	Outputs the master clock (CLS = 1) or inputs a clock (CLS = 0) for slave displays.
WRITE ($\overline{WR}$, pin 13)	Data is written into the display when the $\overline{WR}$ input is low and the $\overline{CE}$ input is low.
CHIP ENABLE ($\overline{CE}$, pin 14)	This input must be at a logic low to read or write data to the display and must go high between each read and write cycle.
READ ($\overline{RD}$, pin 19)	Data is read from the display when the $\overline{RD}$ input is low and the $\overline{CE}$ input is low.
DATA Bus (D_0-D_7, pins 20, 21, 25-30)	The Data bus is used to read from or write to the display.
GND (SUPPLY) (pin 16)	This is the analog ground for the LED drivers.
GND (LOGIC) (pin 18)	This is the digital ground for internal logic.
V_{DD} (POWER) (pin 15)	This is the positive power supply input.
Thermal Test (pin 17)	This pin is used to measure the IC junction temperature. Do not connect.

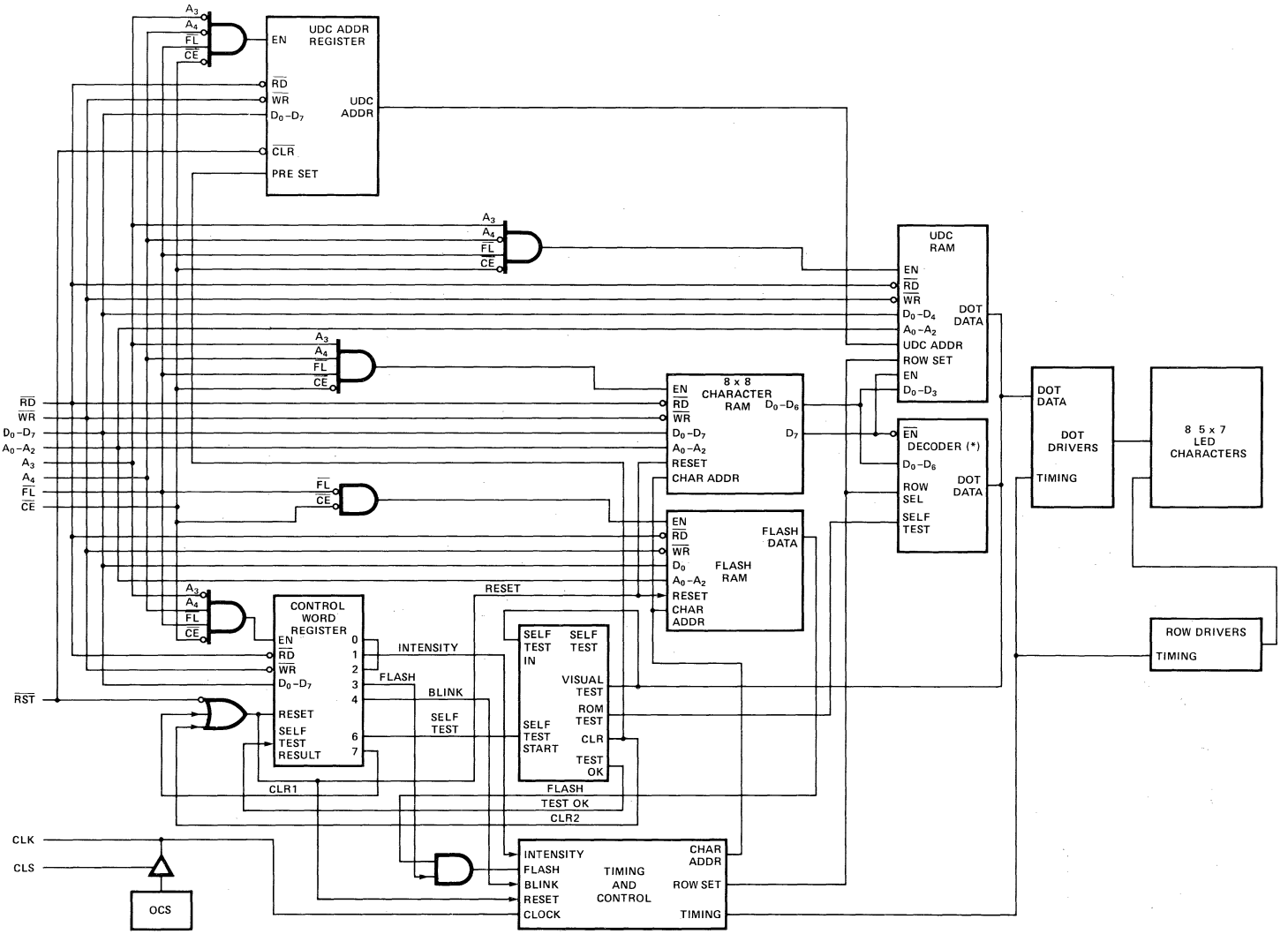


Figure 1. HDSP-253X Internal Block Diagram.

Display Internal Block Diagram

Figure 1 shows the internal block diagram of the HDSP-253X display. The CMOS IC consists of an 8 byte Character RAM, an 8 bit Flash RAM, a 128 character ASCII decoder, a 16 character UDC RAM, a UDC Address Register, a Control Word Register and the refresh circuitry necessary to synchronize the decoding and driving of eight 5 x 7 dot matrix characters. The major user accessible portions of the display are listed below:

Character RAM	This RAM stores either ASCII character data or a UDC RAM address.
Flash RAM	This is a 1 x 8 RAM which stores Flash data.
User-Defined Character RAM (UDC RAM)	This RAM stores the dot pattern for custom characters.
User-defined Character Address Register (UDC Address Register)	This register is used to provide the address to the UDC RAM when the user is writing or reading a custom character.
Control Word Register	This register allows the user to adjust the display brightness, flash individual characters, blink, self test or clear the display.

Character Ram

Figure 2 shows the logic levels needed to access the HDSP-253X Character RAM. During a normal access the $\overline{CE}$ = "0" and either $\overline{RD}$ = "0" or $\overline{WR}$ = "0". However, erroneous data may be written into the Character RAM if the Address lines are unstable when $\overline{CE}$ = "0" regardless of the logic levels of the $\overline{RD}$ or $\overline{WR}$ lines. Address lines A_0-A_2 are used to select the location in the Character RAM. Two types of data can be stored in each Character RAM location: an ASCII code or a UDC RAM address. Data bit D_7 is used to differentiate between the ASCII character and a UDC RAM address. D_7 = 0 enables the ASCII decoder and D_7 = 1 enables the UDC RAM. D_0-D_6 are used to input ASCII data and D_0-D_3 are used to input a UDC address.

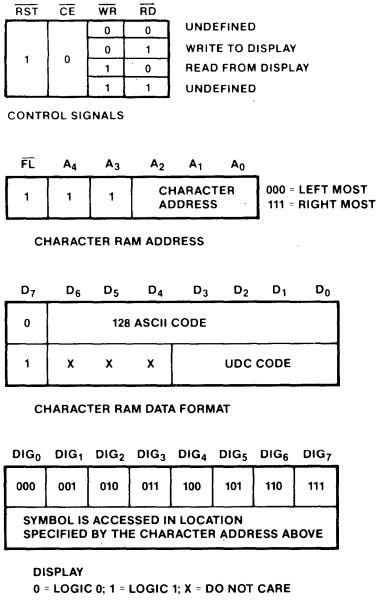


Figure 2. Logic Levels to Access the Character RAM.

UDC RAM and UDC Address Register

Figure 3 shows the logic levels needed to access the UDC RAM and the UDC Address Register. The UDC Address Register is eight bits wide. The lower four bits (D_0-D_3) are used to select one of the 16 UDC locations. The upper four bits (D_4-D_7) are not used. Once the UDC address has been stored in the UDC Address Register, the UDC RAM can be accessed.

To completely specify a 5 x 7 character requires eight write cycles. One cycle is used to store the UDC RAM address in the UDC Address Register. Seven cycles are used to store dot data in the UDC RAM. Data is entered by rows. One cycle is needed to access each row. Figure 4 shows the organization of a UDC character assuming the symbol to be stored is an "F". A_0-A_2 are used to select the row to be accessed and D_0-D_4 are used to transmit the row dot data. The upper three bits (D_5-D_7) are ignored. D_0 (least significant bit) corresponds to the right most column of the 5 x 7 matrix and D_4 (most significant bit) corresponds to the left most column of the 5 x 7 matrix.

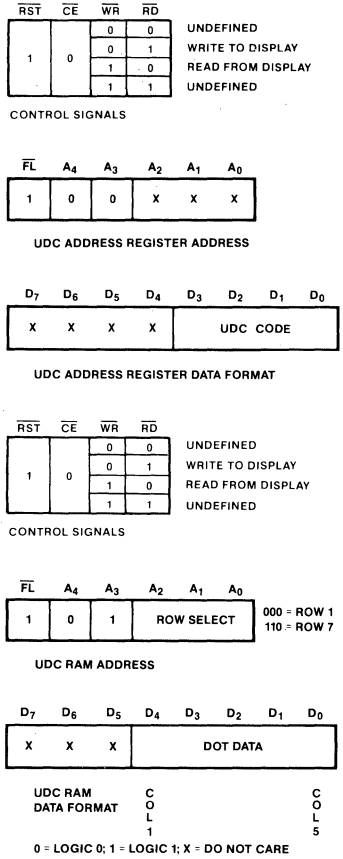


Figure 3. Logic Levels to Access a UDC Character.

Flash RAM

Figure 5 shows the logic levels needed to access the Flash RAM. The Flash RAM has one bit associated with each location of the Character RAM. The Flash input is used to select the Flash RAM. Address lines A_3-A_4 are ignored. Address lines A_0-A_2 are used to select the location in the Flash RAM to store the attribute. D_0 is used to store or remove the flash attribute. D_0 = "1" stores the attribute and D_0 = "0" removes the attribute.

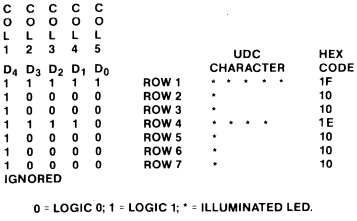


Figure 4. Data to Load "F" into the UDC RAM.

When the attribute is enabled through bit 3 of the Control Word and a "1" is stored in the Flash RAM, the corresponding character will flash at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock the flash rate can be calculated by dividing the clock frequency by 28,672.

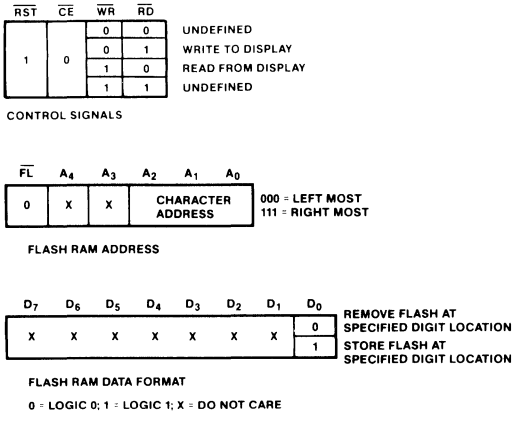


Figure 5. Logic Levels to Access the Flash RAM.

Control Word Register

Figure 6 shows how to access the Control Word Register. This is an eight bit register which performs five functions. They are Brightness control, Flash RAM control, Blinking, Self Test and Clear. Each function is independent of the others. However, all bits are updated during each Control Word write cycle.

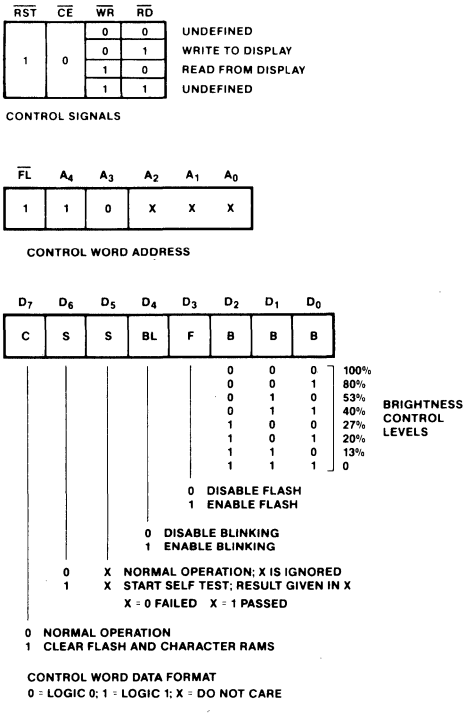


Figure 6. Logic Levels to Access the Control Word Register

Brightness (Bits 0-2)

Bits 0-2 of the Control Word adjust the brightness of the display. Bits 0-2 are interpreted as a three bit binary code with code (000) corresponding to maximum brightness and code (111) corresponding to a blanked display. In addition to varying the display brightness, bits 0-2 also vary the average value of I_{DD}. I_{DD} can be calculated at any brightness level by multiplying the percent brightness level by the value of I_{DD} at the 100% brightness level. These values of I_{DD} are shown in Table 2.

Table 2. Current Requirements at Different Brightness Levels for All Colors Except AlGaAs

Symbol	D_2	D_1	D_0	% Brightness	V_{DD} = 5.0 V 25°C Typ.	Units
I_{DD} (V)	0	0	0	100	200	mA
	0	0	1	80	160	mA
	0	1	0	53	106	mA
	0	1	1	40	80	mA
	1	0	0	27	54	mA
	1	0	1	20	40	mA
	1	1	0	13	26	mA

Flash Function (Bit 3)

Bit 3 determines whether the flashing character attribute is on or off. When bit 3 is a "1", the output of the Flash RAM is checked. If the content of a location in the Flash RAM is a "1", the associated digit will flash at approximately 2 Hz. For an external clock, the blink rate can be calculated by dividing the clock frequency by 28,672. If the flash enable bit of the Control Word is a "0", the content of the Flash RAM is ignored. To use this function with multiple display systems see the Reset section.

Blink Function (Bit 4)

Bit 4 of the Control Word is used to synchronize blinking of all eight digits of the display. When this bit is a "1" all eight digits of the display will blink at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock, the blink rate can be calculated by dividing the clock frequency by 28,672. This function will override the Flash function when it is active. To use this function with multiple display systems see the Reset section.

Self Test Function (Bits 5, 6)
Bit 6 of the Control Word Register is used to initiate the self test function. Results of the internal self test are stored in bit 5 of the Control Word. Bit 5 is a read only bit where bit 5 = "1" indicates a passed self test and bit 5 = "0" indicates a failed self test.

Setting bit 6 to a logic 1 will start the self test function. The built-in self test function of the IC consists of two internal routines which exercises major portions of the IC and illuminates all of the LEDs. The first routine cycles the ASCII decoder ROM through all states and performs a checksum on the output. If the checksum agrees with the correct value, bit 5 is set to "1". The second routine provides a visual test of the LEDs using the drive circuitry. This is accomplished by writing checkered and inverse checkered patterns to the display. Each pattern is displayed for approximately 2 seconds.

During the self test function the display must not be accessed. The time needed to execute the self test function is calculated by multiplying the clock period by 262,144. For example, assume a clock frequency of 58 KHz, then the time to execute the self test function frequency is equal to (262,144/58,000) = 4.5 second duration.

At the end of the self test function, the Character RAM is loaded with blanks, the Control Word Register is set to zeros except for bit 5, and the Flash RAM is cleared and the UDC Address Register is set to all ones.

Clear Function (Bit 7)
Bit 7 of the Control Word will clear the Character RAM and the Flash RAM. Setting bit 7 to a "1" will start the clear function. Three clock cycles (110 µs min. using the internal refresh clock) are required to complete the clear function. The display must not be accessed while the display is being cleared. When the clear function has been completed, bit 7 will be reset to a "0". The ASCII character code for a space (20H) will be loaded into the Character RAM to blank the display and the Flash RAM will be loaded with "0"s. The UDC RAM, UDC Address Register and the remainder of the Control Word are unaffected.

Display Reset

Figure 7 shows the logic levels needed to Reset the display. The display should be Reset on Power-up. The external Reset clears the Character RAM, Flash RAM, Control Word and resets the internal counters. After the rising edge of the Reset signal, three clock cycles (110 µs min. using the internal refresh clock) are required to complete the reset sequence. The display must not be accessed while the display is being reset. The ASCII Character code for a space (20H) will be loaded into the Character RAM to blank the display. The Flash RAM and Control Word Register are loaded with all "0"s. The UDC RAM and UDC Address Register are unaffected. All displays which operate with the same clock source must be simultaneously reset to synchronize the Flashing and Blinking functions.

$\overline{RST}$	$\overline{CE}$	$\overline{WR}$	$\overline{RD}$	$\overline{FL}$	A_4-A_0	D_7-D_0
0	1	X	X	X	X	X

0 = LOGIC 0; 1 = LOGIC 1; X = DO NOT CARE
NOTE:
IF RST, CE AND WR ARE LOW, UNKNOWN DATA MAY BE WRITTEN INTO THE DISPLAY.

Figure 7. Logic Levels to Reset the Display.

Mechanical Considerations

The HDSP-253X is assembled by die attaching and wire bonding 280 LED chips and a CMOS IC to a thermally conductive printed circuit board. A polycarbonate lens placed over the pcb creates an air gap over the LED wire bonds. A backfill epoxy seals the display package.

Figure 8 shows the proper method to insert the display by hand. To prevent damage to the LED wire bonds, apply pressure uniformly with fingers located at both ends of the part. Using a tool, shown in Figure 9, such as a screwdriver or pliers to push the display into the printed circuit board or socket may damage the LED wire bonds. The force exerted by a screwdriver is sufficient to push the lens into the LED wire bonds. The bent wire bonds cause shorts or opens that result in catastrophic failure of the LEDs.

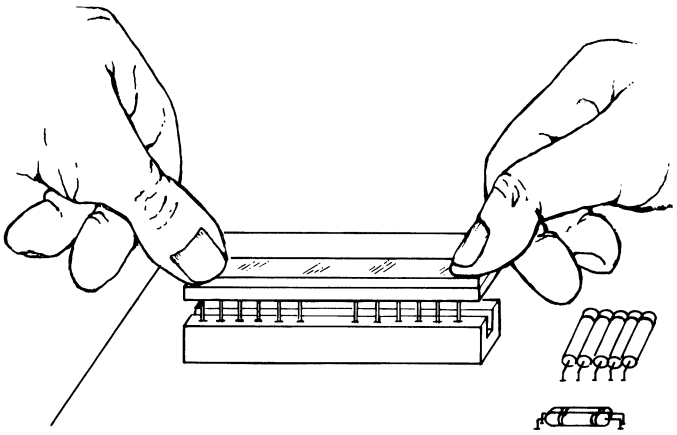


Figure 8. Proper Method to Manually Insert a Display.

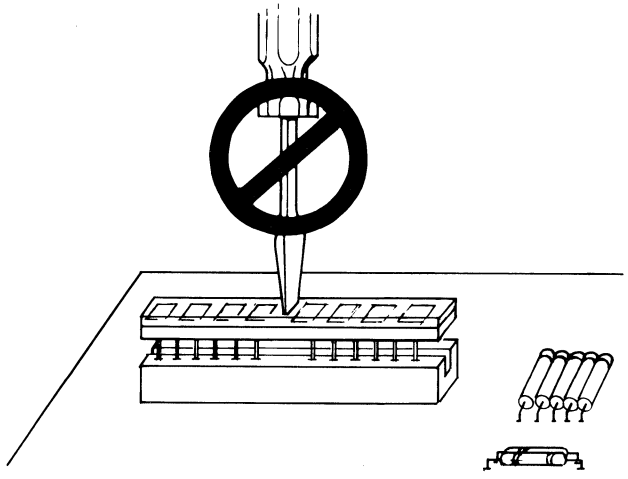


Figure 9. Improper Method to Manually Insert a Display.

Thermal Considerations

The HDSP-253X can operate from -40°C to +85°C. The display's low thermal resistance allows heat to flow from the CMOS IC to the 24 package pins. Typically, this heat is conducted through the printed circuit board traces to free air. For most applications, no additional heatsinking is needed. Illuminating all 280 LEDs simultaneously at full brightness is not recommended for continuous operation. However, all 280 LEDs can be illuminated simultaneously at full brightness for 10 seconds at 25°C as a lamp test.

The IC has a maximum allowable junction temperature of 150°C. The IC junction temperature can be calculated with the following equation:

$T_J MAX = T_A + (P_D \times R\theta_{J\text{-}A})$

$T_J MAX$ is the maximum allowable IC junction temperature.
T_A is the ambient temperature surrounding the display.
P_D is the power dissipated by the IC.
$R\theta_{J\text{-}A}$ is the thermal resistance from the IC through the display package and printed circuit board to the ambient.

A typical value for $R\theta_{J\text{-}A}$ is 39°C/W. This value is typical for a display mounted in a socket and covered with a plastic filter. The socket is soldered to a 0.062 in. thick printed circuit board with 0.020 in. wide one-ounce copper traces.

P_D can be calculated as follows:

$P_D = V_{DD} \times I_{DD}$

V_{DD} is the supply voltage and I_{DD} is the supply current. V_{DD} can vary from 4.5 V to 5.5 V. I_{DD} changes with V_{DD}, temperature, brightness level, and number of on-pixels.

For AlGaAs

$I_{DD}(\#) = (83.8 \times V_{DD} - 0.35 \times T_J) \times B \times N/8$

$I_{DD}(V) = (63 \times V_{DD} - 0.79 \times T_J) \times B \times N/8$

For the other colors

$I_{DD}(\#) = (75.4 \times V_{DD} - 0.28 \times T_J) \times B \times N/8$

$I_{DD}(V) = (54 \times V_{DD} - 0.6 \times T_J) \times B \times N/8$

I_{DD} (#) is the supply current using "#" as the displayed character.
I_{DD}(V) is the supply current using "V" as the displayed character.
T_J is the IC junction temperature.
B is the percent brightness level.
N is the number of characters illuminated.

Operation in high temperature ambients may require power derating or heatsinking. Figure 10 shows how to derate the power for an HDSP-253X. You can reduce the power by tighter supply voltage regulation or lowering the brightness level.

Table 3 shows the calculated maximum allowable ambient temperature for several different sets of operating conditions.

The worst case alphanumeric characters (#,@,B) have 20 pixels. Displaying eight 20-pixel characters will not occur in normal operation. Thus, using eight 20-pixel characters to calculate power dissipation will over estimate the power and the IC junction temperature. The average number of pixels per character, supply voltage, brightness level, and number of characters are needed to calculate the power dissipated by the IC. The ambient temperature, power dissipated by the IC, and the thermal resistance are then used to calculate IC junction temperature. The typical alphanumeric character is 15 pixels. For conditions not listed in Table 3, you can calculate the power dissipated by the IC and use Figure 10 to determine the maximum ambient temperature.

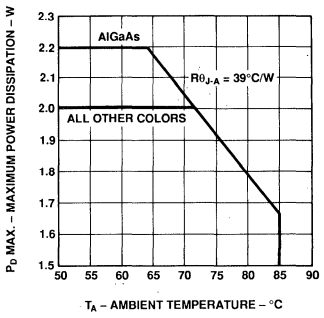


Figure 10. Maximum Allowable Power Dissipation vs. Ambient Temperature. T_JMAX = 150 °C.

Table 3. Maximum Allowable Ambient Temperature for Various Operating Conditions

AlGaAs Red

Character	Number of Characters	Brightness Level	V_{DD} V	I_{DD} mA	P_D W	$R\theta_{J-A}$ °C/W	T_AMAX °C
# (20 dots)	8	100%	5.5	408	2.2	39	64
# (20 dots)	8	100%	5.25	387	2.0	39	72
# (20 dots)	8	100%	5.0	366	1.8	39	80
# (20 dots)	7	100%	5.5	357	2.0	39	72
# (20 dots)	6	100%	5.5	306	1.7	39	84
# (20 dots)	8	80%	5.5	327	1.8	39	80
# (20 dots)	8	80%	5.25	310	1.6	39	85
# (20 dots)	8	53%	5.5	216	1.2	39	85
V (12 dots)	8	100%	5.5	228	1.3	39	85

Table 3. Maximum Allowable Ambient Temperature for Various Operating Conditions (cont'd.)

All Colors Except AlGaAs Red

Character	Number of Characters	Brightness Level	V_{DD} V	I_{DD} mA	P_D W	$R\theta_{J-A}$ °C/W	T_AMAX °C
# (20 dots)	8	100%	5.5	373	2.0	39	72
# (20 dots)	8	100%	5.25	354	1.9	39	77
# (20 dots)	8	100%	5.0	335	1.67	39	85
# (20 dots)	7	100%	5.5	326	1.8	39	80
# (20 dots)	6	100%	5.5	280	1.5	39	85
# (20 dots)	8	80%	5.5	298	1.6	39	85
V (12 dots)	8	100%	5.5	207	1.1	39	85

The actual IC temperature is easy to measure. Pin 17 is thermally and electrically connected to the IC substrate. The thermal resistance from pin 17 to the IC is 16°C/W. The procedure to measure the IC junction temperature is as follows:

1. Measure V_{DD} and I_{DD} for the display. Measure V_{DD} between pins 15 and 16. Measure the current entering pin 15.
2. Measure the temperature of pin 17 after 45 minutes. Use an electrically isolated thermal couple probe.
3. $T_J(IC) = T_{pin} + V_{DD} \times I_{DD} \times 16°C/W$.

Ground Connections

Two ground pins are provided to keep the internal IC logic ground clean. The designer can, when necessary, route the analog ground for the LED drivers separately from the logic ground until an appropriate ground plane is available. On long interconnections between the display and the host system, the designer can keep voltage drops on the analog ground from affecting the display logic levels by isolating the two grounds.

The logic ground should be connected to the same ground potential as the logic interface circuitry. The analog ground and the logic ground should be connected at a common ground which can withstand the current introduced by the switching LED drivers. When separate ground connections are used, the analog ground can vary from -0.3 V to +0.3 V with respect to the logic ground. Voltage below -0.3 V can cause all dots to be on. Voltage above +0.3 V can cause dimming and dot mismatch.

Solder and Post Solder Cleaning

Note: Freon vapors can cause the black paint to peel off the display. See Application Note 1027 for information of soldering and post solder cleaning.

Contrast Enhancement (Filtering)

See Application Note 1015 for information on contrast enhancement.

HEWLETT PACKARD

Four Character Smart Alphanumeric Displays

Technical Data

HPDL-1414
HPDL-2416

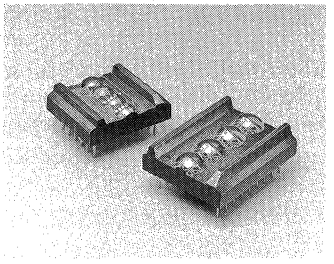
Features

- **Smart Alphanumeric Display**
  Built-in RAM, ASCII Decoder and LED Drive Circuitry
- **Wide Operating Temperature Range**
  -40°C to +85°C
- **Fast Access Time**
  160 ns
- **Excellent ESD Protection**
  Built-in Input Protection Diodes
- **CMOS IC for Low Power Consumption**
- **Full TTL Compatibility Over Operating Temperature Range**
  V_{IL} = 0.8 V
  V_{IH} = 2.0 V
- **Wave Solderable**
- **Rugged Package Construction**
- **End-Stackable**
- **Wide Viewing Angle**

Description

The HPDL-1414 and 2416 are smart, four character, sixteen-segment, red GaAsP displays. The HPDL-1414 has a character height of 2.85 mm (0.112"). The HPDL-2416 has a character height of 4.10 mm (0.160"). The on-board CMOS IC contains memory, ASCII decoder, multiplexing circuitry and drivers. The monolithic LED characters are magnified by an immersion lens which increases both character size and luminous intensity. The encapsulated dual-in-line package provides a rugged, environmentally sealed unit.

The HPDL-1414 and 2416 incorporate many improvements over competitive products. They have a wide operating temperature range, very fast IC access time, and improved ESD protection. The displays are also fully TTL compatible, wave solderable, and highly reliable. These displays are ideally suited for industrial and commercial applications where a good-looking, easy-to-use alphanumeric display is required.



Typical Applications

- **Portable Data Entry Devices**
- **Medical Equipment**
- **Process Control Equipment**
- **Test Equipment**
- **Industrial Instrumentation**
- **Computer Peripherals**
- **Telecommunication Instrumentation**

ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED WITH THE HPDL-1414 AND HPDL-2416.

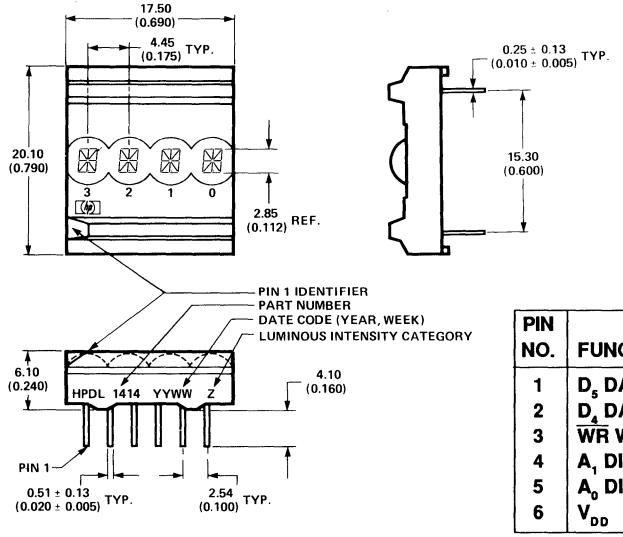
Absolute Maximum Ratings

Supply Voltage, V_{DD} to Ground ..... -0.5 V to 7.0 V
Input Voltage, Any Pin to Ground ..... -0.5 V to V_{DD} + 0.5 V
Free Air Operating Temperature Range, T_A [1] ..... -40°C to +85°C
Relative Humidity (non-condensing) at 65°C 90%
Storage Temperature, T_S ..... -40°C to +85°C
Maximum Solder Temperature, 1.59 mm (0.063 in.)
below Seating Plane, t < 5 sec.[2] ..... 260°C
ESD Protection @ 1.5 kΩ, 100 pF ..... V_Z = 2 kV (each Pin)

Note:
1. Free air operating temperature range (HPDL-2416 only):
   T_A > 75°C No Cursors On
   T_A ≤ 75°C 1 Cursor On
   T_A ≤ 68°C 2 Cursors On
   T_A ≤ 60°C 3 Cursors On
   T_A ≤ 55°C 4 Cursors On
2. Warning: Alcohol based cleaning solvents or fluxes will attack the package of this product.

Package Dimensions

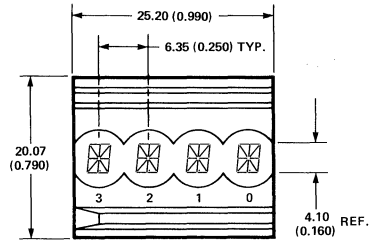
HPDL-1414

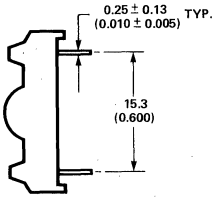


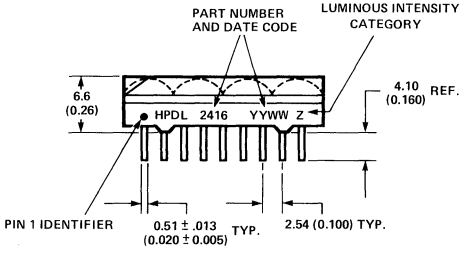
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	D_5 DATA INPUT	7	GND
2	D_4 DATA INPUT	8	D_0 DATA INPUT
3	$\overline{WR}$ WRITE	9	D_1 DATA INPUT
4	A_1 DIGIT SELECT	10	D_2 DATA INPUT
5	A_0 DIGIT SELECT	11	D_3 DATA INPUT
6	V_{DD}	12	D_6 DATA INPUT

NOTES:
1. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS 0.254 mm (0.010 in.).
2. DIMENSIONS IN mm (inches).

HPDL-2416







PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	$\overline{CE}_1$ CHIP ENABLE	10	GND
2	$\overline{CE}_2$ CHIP ENABLE	11	D_0 DATA INPUT
3	$\overline{CLR}$ CLEAR	12	D_1 DATA INPUT
4	CUE CURSOR ENABLE	13	D_2 DATA INPUT
5	$\overline{CU}$ CURSOR SELECT	14	D_3 DATA INPUT
6	$\overline{WR}$ WRITE	15	D_6 DATA INPUT
7	ADDRESS INPUT A_1	16	D_5 DATA INPUT
8	ADDRESS INPUT A_0	17	D_4 DATA INPUT
9	V_{DD}	18	$\overline{BL}$ DISPLAY BLANK

NOTES:
1. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS 0.254 mm (0.010 in.).
2. DIMENSIONS IN mm (inches).

Recommended Operating Conditions

Parameter	Sym.	Min.	Nom.	Max.	Units
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

DC Electrical Characteristics Over Operating Temperature Range

Parameter	Sym.	Min.	25°C Typ.	25°C Max.	Max.[1]	Units	Test Conditions
Input Current HPDL-1414	I_{IL}		17	30	50	µA	V_{DD} = 5.0 V, $\overline{BL}$ = 0.8 V
HPDL-2416			17	30	40	µA	
I_{DD} Blank HPDL-1414	I_{DD} ($\overline{BL}$)		1.2	2.3	4.0	mA	V_{DD} = 5.0 V, $\overline{BL}$ = 0.8 V
HPDL-2416			1.5	3.5	8.0	mA	
I_{DD} 4 Digits ON (10 Segments/digit)[2,3] HPDL-1414	I_{DD}		70	90	130	mA	V_{DD} = 5.0 V
HPDL-2416			85	115	170	mA	
I_{DD} 4 Digits ON Cursor[4] HPDL-2416	I_{DD}(CU)		125	165	232	mA	V_{DD} = 5.0 V
Input Voltage High	V_{IH}	2.0			V_{DD}	V	
Input Voltage Low	V_{IL}	GND			0.8	V	
Power Dissipation[5] HPDL-1414	P_D		350	450	715	mW	V_{DD} = 5.0 V
HPDL-2416			425	575	910	mW	

Notes:
1. V_{DD} = 5.5 V.
2. "%" illuminated in all four characters.
3. Measured at five seconds.
4. Cursor character is sixteen segments and DP ON.
5. Power Dissipation = $(V_{DD})(I_{DD})$ for 10 segments ON.

Optical Characteristics at 25°C[6]

Parameter	Sym.	Min.	Typ.	Units	Test Conditions
Peak Luminous Intensity per Digit, 8 segments ON (character average) HPDL-1414	I_v Peak	0.4	1.0	mcd	V_{DD} = 5.0 V, "*" illuminated in all 4 digits
HPDL-2416		0.5	1.25	mcd	
Peak Wavelength	λ_{Peak}		655	nm	
Dominant Wavelength	λ_d		640	nm	
Off Axis Viewing Angle HPDL-1414			±40	degrees	
HPDL-2416			±50	degrees	

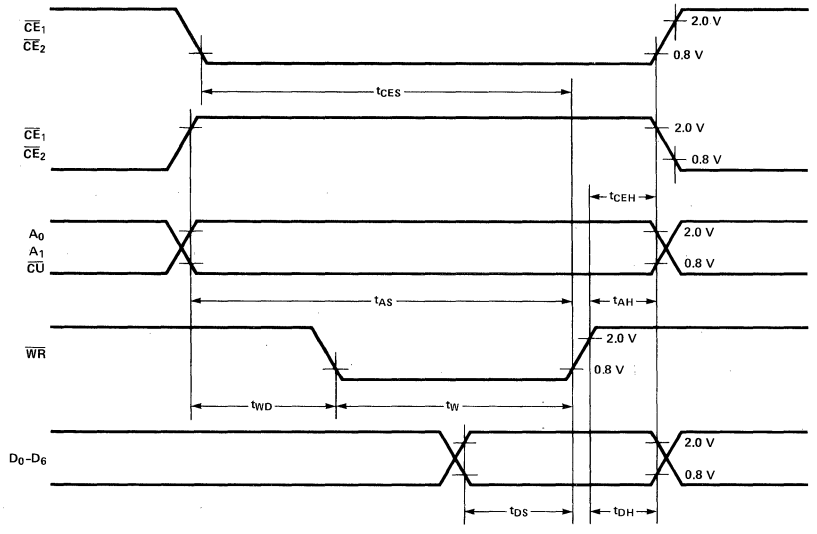
Note:
6. Refers to the initial case temperature of the device immediately prior to the light measurement.

AC Timing Characteristics Over Operating Temperature Range at V_{CC} = 4.5 V

Parameter	Symbol	-20°C t_{MIN}	25°C t_{MIN}	70°C t_{MIN}	Units
Address Setup Time	t_{AS}	90	115	150	ns
Write Delay Time	t_{WD}	10	15	20	ns
Write Time	t_{W}	80	100	130	ns
Data Setup Time	t_{DS}	40	60	80	ns
Data Hold Time	t_{DH}	40	45	50	ns
Address Hold Time	t_{AH}	40	45	50	ns
Chip Enable Hold Time[1]	t_{CEH}	40	45	50	ns
Chip Enable Setup Time[1]	t_{CES}	90	115	150	ns
Clear Time[1]	t_{CLR}	2.4	3.5	4.0	ms
Access Time		130	160	200	ns
Refresh Rate		420-790	310-630	270-550	Hz

Note:
1. HPDL-2416 only.

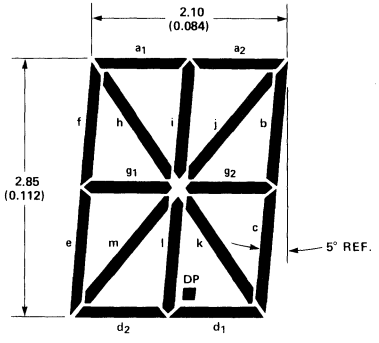
Timing Diagram



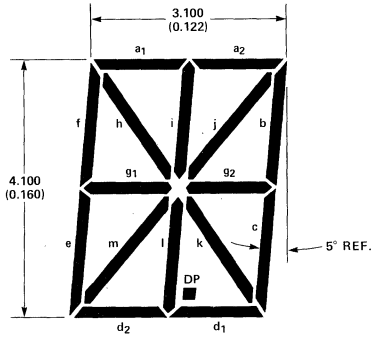
Character Set

BITS	D_3 D_2 D_1 D_0	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
D_6 D_5 D_4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 1 0	2	(space)	!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
0 1 1	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
1 0 0	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1 0 1	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_

Magnified Character Font Description

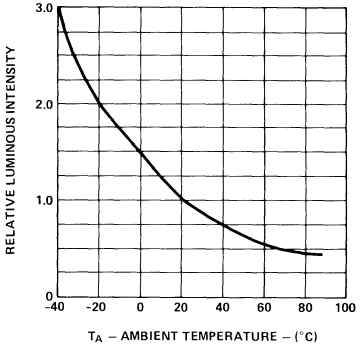


HPDL-1414



HPDL-2416

Relative Luminous Intensity vs. Temperature



Electrical Description

Display Internal Block Diagram HPDL-1414

Figure 1 shows the internal block diagram of the HPDL-1414. It consists of two parts: the display LEDs and the CMOS IC. The CMOS IC consists of a four-word ASCII memory, a 64-word character generator, 17 segment drivers, four digit drivers, and the scanning circuitry necessary to multiplex the four monolithic LED characters. In normal operation, the divide-by-four counter sequentially accesses each of the four RAM locations and simultaneously enables the appropriate display digit driver. The output of the RAM is decoded by the character generator which, in turn, enables the appropriate display segment drivers. Seven-bit ASCII data is stored in RAM. Since the display uses a 64-character decoder, half of the possible 128 input combinations are invalid. For each display location where $D_5 = D_6$ in the ASCII RAM, the display character is blanked.

Data Entry HPDL-1414

Figure 2 shows a truth table for the HPDL-1414. Data is loaded into the display through the DATA inputs (D_6-D_0), ADDRESS inputs (A_1-A_0), and WRITE ($\overline{WR}$). After a character has been written to memory, the IC decodes the ASCII data, drives the display and refreshes it without any external hardware or software.

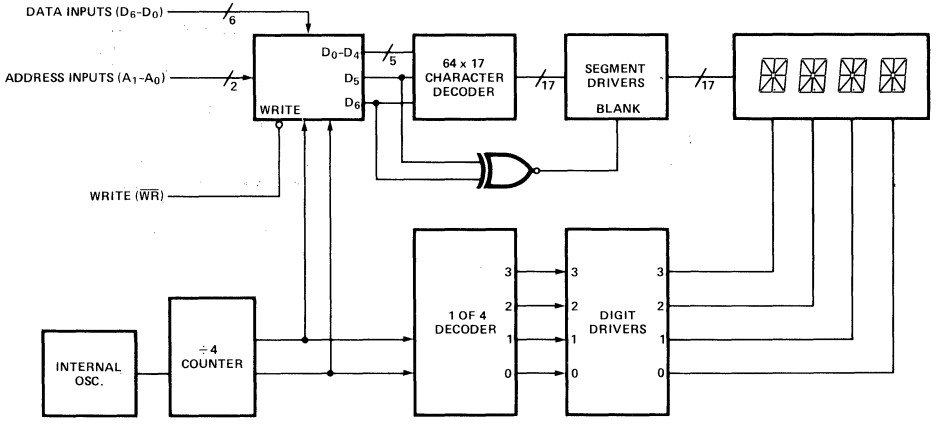


Figure 1. HPDL-1414 Internal Block Diagram.

$\overline{WR}$	A_1	A_0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	DIG_3	DIG_2	DIG_1	DIG_0
L	L	L	a	a	a	a	a	a	a	NC	NC	NC	A
L	L	H	b	b	b	b	b	b	b	NC	NC	B	NC
L	H	L	c	c	c	c	c	c	c	NC	C	NC	NC
L	H	H	d	d	d	d	d	d	d	D	NC	NC	NC
H	X	X	X	X	X	X	X	X	X	Previously Written Data			

L = LOGIC LOW INPUT
H = LOGIC HIGH INPUT
X = DON'T CARE
"a" = ASCII CODE CORRESPONDING TO SYMBOL "A"
NC = NO CHANGE

Figure 2. HPDL-1414 Write Truth Table.

Display Internal Block Diagram HPDL-2416

Figure 3 shows the internal block diagram for the HPDL-2416 display. The CMOS IC consists of a four-word ASCII memory, a four-word cursor memory, a 64-word character generator, 17 segment drivers, four digit drivers, and the scanning circuitry necessary to multiplex the four monolithic LED characters. In normal operation, the divide-by-four counter sequentially accesses each of the four RAM locations and simultaneously enables the appropriate display digit driver. The output of the RAM is decoded by the character generator which, in turn, enables the appropriate display segment drivers. For each display location, the cursor enable (CUE) selects whether the data from the ASCII RAM (CUE = 0) or the stored cursor (CUE = 1) is to be displayed. The cursor character is denoted by all sixteen segments and the DP ON. Seven-bit ASCII data is stored in RAM. Since the display utilizes a 64-character decoder, half of the possible 128 input combinations are invalid. For each display location where $D_5 = D_6$ in the ASCII RAM, the display character is blanked. The entire display is blanked when $\overline{BL} = 0$.

Data is loaded into the display through the data inputs (D_6-D_0), address inputs (A_1, A_0), chip enables ($\overline{CE_1}$, $\overline{CE_2}$), cursor select ($\overline{CU}$), and write ($\overline{WR}$). The cursor select ($\overline{CU}$) determines whether data is stored in the ASCII RAM ($\overline{CU} = 1$) or cursor memory ($CU = 0$). When $\overline{CE_1} = \overline{CE_2} = \overline{WR} = 0$ and $\overline{CU} = 1$, the information on the data inputs is stored in the ASCII RAM at the location specified by the address inputs (A_1, A_0). When $\overline{CE_1} = \overline{CE_2} = \overline{WR} = 0$ and $\overline{CU} = 0$, information on the data input, D_0, is stored in the cursor at the location specified by the address inputs (A_1, A_0). If $D_0 = 1$, a cursor character is stored in the cursor memory. If $D_0 = 0$, a previously stored cursor character will be removed from the cursor memory.

If the clear input ($\overline{CLR}$) equals zero for one internal display cycle (4 ms minimum), the data in the ASCII RAM will be rewritten with zeroes and the display will be blanked. Note that the blanking input ($\overline{BL}$) must be equal to logical one during this time.

Data Entry HPDL-2416

Figure 4 shows a truth table for the HPDL-2416 display. Setting the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) to their low state and the cursor select ($\overline{CU}$) to its high state will enable data loading. The desired data inputs (D_6-D_0) and address inputs (A_1, A_0) as well as the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) and cursor select ($\overline{CU}$) must be held stable during the write cycle to ensure that the correct data is stored into the display. Valid ASCII data codes are shown in Figure 1. The display accepts standard seven-bit ASCII data. Note that $D_6 \neq D_5$ for the codes shown in Figure 4. If $D_6 = D_5$ during the write cycle, then a blank will be stored in the display. Data can be loaded into the display in any order. Note that when $A_1 = A_0 = 0$, data is stored in the furthest right-hand display location.

Cursor Entry HPDL-2416

As shown in Figure 4, setting the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) to their low state and the cursor select (CU) to its low state will enable cursor loading. The cursor character is indicated by the display symbol having all 16 segments and the DP ON. The least significant data input (D_0), the address inputs (A_1, A_0), the chip enables ($\overline{CE_1}$, $\overline{CE_2}$), and the cursor select ($\overline{CU}$) must be held stable during the write cycle to ensure that the correct data is stored in the display. If D_0 is in a low state during the write cycle, then a cursor character will be removed at the indicated location. If D_0 is in a high state during the write

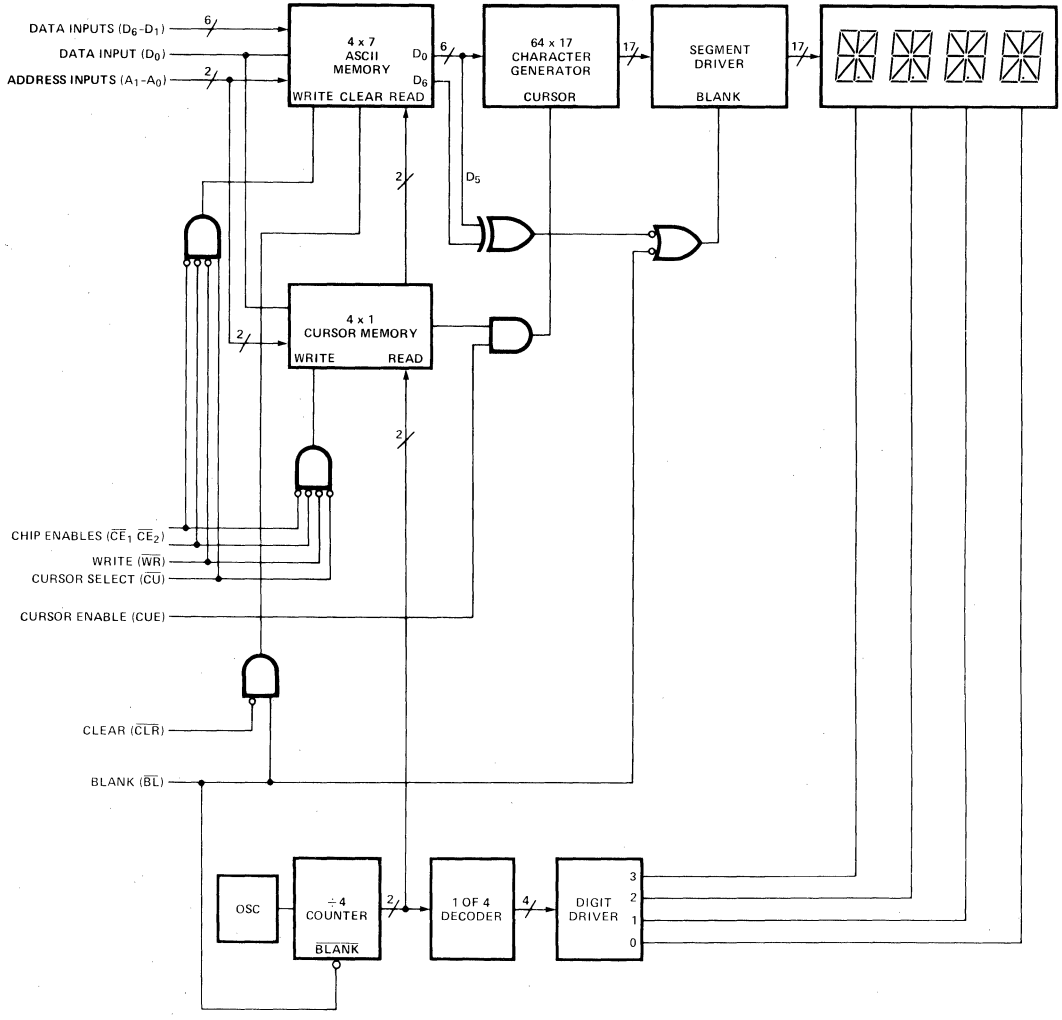


Figure 3. HPDL-2416 Internal Block Diagram.

cycle, then a cursor character will be stored at the indicated location. The presence or absence of a cursor character does not affect the ASCII data stored at that location. Again, when $A_1 = A_0 = 0$, the cursor character is stored in the furthest right-hand display location.

All stored cursor characters are displayed if the cursor enable (CUE) is high. Similarly, the stored ASCII data words are displayed, regardless of the cursor characters, if the cursor enable (CUE) is low. The cursor enable (CUE) has no effect on the storage or removal of the cursor characters within the display. A flashing cursor is displayed by pulsing the cursor enable (CUE). For applications not requiring a cursor, the cursor enable (CUE) can be connected to ground and the cursor select (CU) can be connected to V_{CC}. This inhibits the cursor function and allows only ASCII data to be loaded into the display.

Function	$\overline{BL}$	$\overline{CLR}$	CUE	$\overline{CU}$	$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WR}$	A_1	A_0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	DIG_3	DIG_2	DIG_1	DIG_0
Write Data Memory	L	X	X	H -OR- H	L	L	L	L	L	a	a	a	a	a	a	a	NC	NC	NC	A
								L	H	b	b	b	b	b	b	b	NC	NC	B	NC
								H	L	c	c	c	c	c	c	c	NC	C	NC	NC
								H	H	d	d	d	d	d	d	d	D	NC	NC	NC
Disable Data Memory Write	X	X	X	H	X	X	H	X	X	X	X	X	X	X	X	X	Previously Written Data			
	X	X	X	H	X	H	X													
	X	X	X	H	H	X	X													
Write Cursor	X	X	X	L	L	L	L	L	L	X	X	X	X	X	X	H	NC	NC	NC	▩
								L	H	X	X	X	X	X	X	H	NC	NC	▩	NC
								H	L	X	X	X	X	X	X	H	NC	▩	NC	NC
								H	H	X	X	X	X	X	X	H	▩	NC	NC	NC
Clear Cursor	X	X	X	L	L	L	L	L	L	X	X	X	X	X	X	L	NC	NC	NC	⬚
								L	H	X	X	X	X	X	X	L	NC	NC	⬚	NC
								H	L	X	X	X	X	X	X	L	NC	⬚	NC	NC
								H	H	X	X	X	X	X	X	L	⬚	NC	NC	NC
Disable Cursor Memory	X	X	X	L	X	X	H	X	X	X	X	X	X	X	X	X	Previously Written Cursor			
	X	X	X	L	X	H	X													
	X	X	X	L	H	X	X													

L = LOGIC LOW INPUT
H = LOGIC HIGH INPUT
X = DON'T CARE

"a" = ASCII CODE CORRESPONDING TO SYMBOL "A"
NC = NO CHANGE
▩ = CURSOR CHARACTER (ALL SEGMENTS ON)

Figure 4a. Cursor/Data Memory Write Truth Table.

Function	$\overline{BL}$	$\overline{CLR}$	CUE	$\overline{CU}$	$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WR}$	DIG_3	DIG_2	DIG_1	DIG_0	
CUE	H	H	L	X	X	X	X	A	B	C	D	Display previously written data
	H	H	H	X	X	X	X	▩	▩	▩	▩	Display previously written cursor
Clear	H	L	X	X	X	X	X*	⬚	⬚	⬚	⬚	Clear data memory, cursor memory unchanged
	*NOTE: CLR should be held low for 4 ms following the last WRITE cycle to ensure all data is cleared.											
Blanking	L	X	X	X	X	X	X	⬚	⬚	⬚	⬚	Blank display, data and cursor memories unchanged.

Figure 4b. Displayed Data Truth Table.

Display Clear HPDL-2416
As shown in Figure 4, the ASCII data stored in the display will be cleared if the clear ($\overline{CLR}$) is held low and the blanking input ($\overline{BL}$) is held high for 4 ms minimum. The cursor memory is not affected by the clear ($\overline{CLR}$) input. Cursor characters can be stored or removed even while the clear ($\overline{CLR}$) is low. Note that the display will be cleared regardless of the state of the chip enables (CE_1, $\overline{CE_2}$). However, to ensure that all four display characters are cleared, CLR should be held low for 4 ms following the last write cycle.

Display Blank HPDL-2416
As shown in Figure 4, the display will be blanked if the blanking input ($\overline{BL}$) is held low. Note that the display will be blanked regardless of the state of the chip enables (CE_1, $\overline{CE_2}$) or write (WR) inputs. The ASCII data stored in the display and the cursor memory are not affected by the blanking input. ASCII data and cursor data can be stored even while the blanking input ($\overline{BL}$) is low. Note that while the blanking input ($\overline{BL}$) is low, the clear ($\overline{CLR}$) function is inhibited. A flashing display can be obtained by applying a low frequency square wave to the blanking input ($\overline{BL}$). Because the blanking input ($\overline{BL}$) also resets the internal display multiplex counter, the frequency applied to the blanking input ($\overline{BL}$) should be much slower than the display multiplex rate. Finally, dimming of the display through the blanking input ($\overline{BL}$) is not recommended.

For further application information please consult Application Note 1026.

Optical Considerations/ Contrast Enhancement

The HPDL-1414 and HPDL-2416 displays use a precision aspheric immersion lens to provide excellent readability and low off-axis distortion. For the HPDL-1414, the aspheric lens produces a magnified character height of 2.85 mm (0.112 in.) and a viewing angle of ±40°. For the HPDL-2416, the aspheric lens produces a magnified character height of 4.1 mm (0.160 in.) and a viewing angle of ±50°. These features provide excellent readability at distances up to 1.5 metres (4 feet) for the HPDL-1414 and 2 metres (6 feet) for the HPDL-2416.

Each HPDL-1414/2416 display is tested for luminous intensity and marked with an intensity category on the side of the display package. To ensure intensity matching for multiple package applications, mixing intensity categories for a given panel is not recommended.

The HPDL-1414/2416 display is designed to provide maximum contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60, Panelgraphic Dark Red 63, SGL Homalite H100-1650, Rohm and Haas 2423, Chequers Engraving 118, and 3M R6510. For further information on contrast enhancement, see Hewlett-Packard Application Note 1015.

Mechanical and Electrical Considerations

The HPDL-1414/2416 are dual in-line packages that can be stacked horizontally and vertically to create arrays of any size. These displays are designed to operate continuously between -40°C to +85°C with a maximum of 10 segments on per digit.

During continuous operation of all four Cursors the operating temperature should be limited to -40°C to +55°C. At temperatures above +55°C, the maximum number of Cursors illuminated continuously should be reduced as follows: No Cursors illuminated at operating temperatures above 75°C. One Cursor can be illuminated continuously at operating temperatures below 75°C. Two Cursors can be illuminated continuously at operating temperatures below 68°C. Three Cursors can be illuminated continuously at operating temperatures below 60°C.

The HPDL-1414/2416 are assembled by die attaching and wire bonding the four GaAsP/GaAs monolithic LED chips and the CMOS IC to a high temperature printed circuit board. An immersion lens is formed by placing the PC board assembly into a nylon lens filled with epoxy. A plastic cap creates an air gap to protect the CMOS IC. Backfill epoxy environmentally seals the display package. This package construction provides the display with a high tolerance to temperature cycling.

The inputs to the CMOS IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HPDL-1414/2416 should be stored in

anti-static tubes or conductive material. During assembly a grounded conductive work area should be used, and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static charge build-up. Input current latchup is caused when the CMOS inputs are subjected either to a voltage below ground (V_{IN} < ground) or to a voltage higher than V_{DD} ($V_{IN} > V_{DD}$) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{DD}. Voltages should not be applied to the inputs until V_{DD} has been applied to the display. Transient input voltages should be eliminated.

Soldering and Post Solder Cleaning Instructions

The HPDL-1414/2416 may be hand soldered or wave soldered with SN63 solder. Hand soldering may be safely performed only with an electronically temperature-controlled and securely grounded soldering iron. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux can be used. The solder wave temperature should be 245°C ± 5°C (473°F ± 9°F), and the dwell in the wave should be set at 1-1/2 to 3 seconds for optimum soldering. Preheat temperature should not exceed 93°C (200°F) as measured on the solder side of the PC board.

Post solder cleaning may be performed with a solvent or aqueous process. For solvent cleaning, Allied Chemical Genesolv DES, Baron Blakeslee Blaco-Tron TES or DuPont Freon TE can only be used. These solvents are azeotropes of trichlorotrifluoroethane FC-113 with low concentrations of ethanol (5%). The maximum exposure time in the solvent vapors at boiling temperature should not exceed 2 minutes. Solvents containing high concentrations of alcohols, pure alcohols, isopropanol or acetone should not be used as they will chemically attack the nylon lens. Solvents containing trichloroethane FC-111 or FC-112 and trichloroethylene (TCE) are not recommended.

An aqueous cleaning process is highly recommended. A saponifier, such as Kester-Biokleen Formula 5799 or equivalent, may be added to the wash cycle of an aqueous process to remove rosin flux residues. Organic acid flux residues must be thoroughly removed by an aqueous cleaning process to prevent corrosion of the leads and solder connections. The optimum water temperature is 60°C (140°F). The maximum cumulative exposure of the HPDL-2416 to wash and rinse cycles should not exceed 15 minutes.

HEWLETT PACKARD

CMOS 5x7 Alphanumeric Displays

Technical Data

HCMS-200X Series
HCMS-230X Series

Features

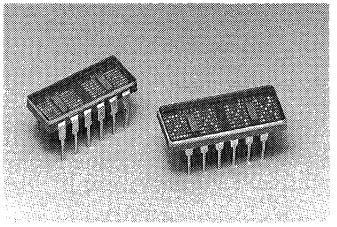
- **On-Board Low Power CMOS IC:** Integrated Shift Register with Constant Current LED Drivers
- **Wide Operating Temperature Range:** -40°C to +85°C
- **Compact Glass Ceramic 4 Character Package:** HCMS-200X Series End Stackable HCMS-230X Series X-Y Stackable
- **Five Colors:** Standard Red High Efficiency Red Orange Yellow High Performance Green
- **5 X 7 LED Matrix Displays Full ASCII Set**
- **Two Character Heights:** 3.8mm (0.15 inch) 5.0mm (0.20 inch)
- **Wide Viewing Angle:** X Axis = ± 50° Y Axis = ± 65°
- **Long Viewing Distance:** HCMS-200X Series to 2.6 Meters (8.6 Feet) HCMS-230X Series to 3.5 Meters (11.5 Feet)
- **Categorized for Luminous Intensity**
- **HCMS-2001/-2003, HCMS-2301/-2303:** Categorized for Color

Typical Applications

- **Commercial Avionics**
- **Instrumentation**
- **Medical Instruments**
- **Business Machines**

Description

The HCMS-200X and HCMS-230X series are 5x7 LED four character displays contained in 12 pin dual-in-line packages designed for displaying alphanumeric information. The character height for the HCMS-200X series displays is 3.8mm (0.15 inch), and for the HCMS-230X series displays the character height is 5.0mm (0.20 inch). These displays are available in all five LED colors: standard red, high efficiency red, orange, yellow and high performance green. The HCMS-200X series displays are end stackable and the HCMS-230X series displays are end/row stackable.



Display Selection Table

Part Number	Character Size	LED Color
HCMS-2000	3.8 mm (0.15 inch)	Standard Red
HCMS-2001	3.8 mm (0.15 inch)	Yellow
HCMS-2002	3.8 mm (0.15 inch)	High-Efficiency Red
HCMS-2003	3.8 mm (0.15 inch)	High-Performance Green
HCMS-2004	3.8 mm (0.15 inch)	Orange
HCMS-2300	5.0 mm (0.20 inch)	Standard Red
HCMS-2301	5.0 mm (0.20 inch)	Yellow
HCMS-2302	5.0 mm (0.20 inch)	High-Efficiency Red
HCMS-2303	5.0 mm (0.20 inch)	High-Performance Green
HCMS-2304	5.0 mm (0.20 inch)	Orange

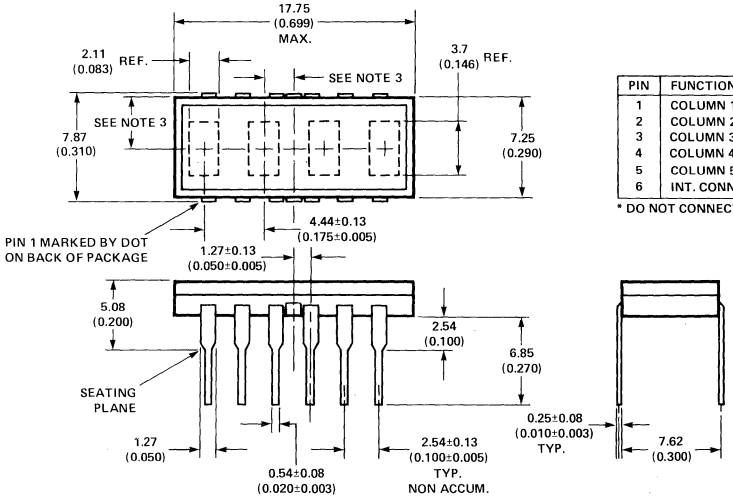
ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED.

These displays are designed with on-board CMOS integrated circuits for use in applications where conservation of power is important. The two CMOS ICs form an on-board serial-in-parallel-out 28-bit shift register with constant current output LED row drivers. Decoded column data is clocked into the on-board shift register for each refresh cycle. Full character display is achieved with external column strobing.

Compatibility with HDSP-200X/230X TTL IC Series Displays

The HCMS-200X, HCMS-230X CMOS IC displays are "drop-in" replacements for the equivalent HDSP-200X, HDSP-230X TTL IC displays. The 12 pin glass/ceramic package configuration, four digit character matrix and pin functions are identical.

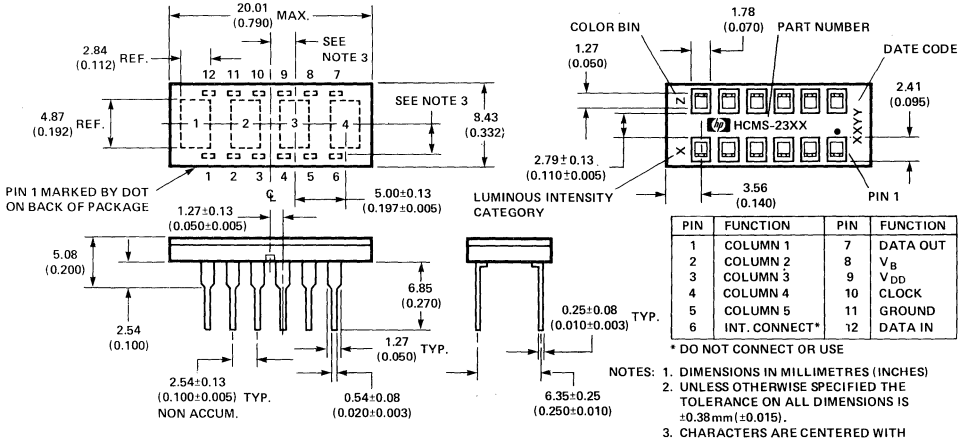
Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{DD}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

* DO NOT CONNECT OR USE

HCMS-200X Series



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{DD}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

* DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN MILLIMETRES (INCHES)
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±0.38mm(±0.015).
3. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±0.13mm(±0.005").
4. LEAD MATERIAL IS COPPER ALLOY, SOLDER DIPPED.

HCMS-230X Series

Absolute Maximum Ratings

Supply Voltage V_{DD} to Ground ..... -0.3 V to 7.0 V
Data Input, Data Output, V_B ..... -0.3 V to V_{DD}
Column Input Voltage, V_{COL} ..... -0.3 V to V_{DD}
Free Air Operating Temperature Range, T_A ..... -40°C to +85°C
Storage Temperature Range, T_S ..... -55°C to +100°C
Maximum Allowable Package Power Dissipation, P_D [1,2]
HCMS-2000/-2001/-2002/-2003/-2004 at T_A = 78°C ..... 0.79 Watts
HCMS-2300 at T_A = 85°C ..... 0.79 Watts
HCMS-2301/-2302/-2303/-2304 at T_A = 85°C ..... 0.92 Watts
Maximum Solder Temperature
1.59 mm (0.063") Below Seating Plane, t < 5 sec ..... 260°C
ESD Protection @ 1.5 kΩ, 100 pF ..... V_Z = 4 kV (each pin)

Notes:
1. Maximum allowable power dissipation is derived from V_{DD} = 5.25 V, V_B = 2.4 V, V_{COL} = 3.5 V, 20 LEDs on per character, 20% DF.
2. The power dissipation for these displays should be derated as follows:
   HCMS-200X series derate above 78°C at 18 mW/°C, $R\theta_{J-A}$ = 60°C/W.
   HCMS-230X series may be operated without derating up to T_A = 85°C, $R\theta_{J-A}$ = 45°C/W.

Deratings based on $R\theta_{PC-A}$ = 35°C/W per display for printed circuit board assembly.
See Figure 1 for power derating.

Recommended Operating Conditions Over Operating Temperature Range (-40°C to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}	4.75	5.00	5.25	V
Data Out Current, Low State	I_{OL}			1.6	mA
Data Out Current, High State	I_{OH}			-0.5	mA
Column Input Voltage	V_{COL}	2.75	3.0	3.5	V
Setup Time	t_{SETUP}	10			ns
Hold Time	t_{HOLD}	25			ns
Clock Pulse Width High	$t_{WH(CLOCK)}$	50			ns
Clock Pulse Width Low	$t_{WL(CLOCK)}$	50			ns
Clock High to Low Transition	t_{THL}			200	ns
Clock Frequency	f_{CLOCK}			5	MHz

Electrical Characteristics Over Operating Temperature Range (-40°C to +85°C)

Parameter	Symbol	Test Conditions	Min.	Typ.*	Max.	Units
Supply Current, Dynamic[1]	I_{DDD}	f_{CLOCK} = 5 MHz		6.2	7.8	mA
Supply Current, Static[2]	I_{DDSoff} I_{DDSon}	V_B = 0.4 V V_B = 2.4 V		1.8 2.2	2.6 3.3	mA
Column Input Current	I_{COL}	V_B = 0.4 V			10	µA
HCMS-2000/-2001/-2002/-2003/-2004		V_B = 2.4 V		310	384	
HCMS-2300		V_B = 2.4 V		310	384	mA
HCMS-2301/-2302/-2303/-2304		V_B = 2.4 V		360	451	mA
Input Logic High Data, V_B, Clock	V_{IH}	V_{DD} = 4.75 V	2.0			V
Input Logic Low Data, V_B, Clock	V_{IL}	V_{DD} = 5.25 V			0.8	V
Input Current	I_I	V_{DD} = 5.25 V				
Data, Clock		0 < V_I < 5.25 V	-10		+1	µA
V_B		0 < V_B < 5.25 V	-40		0	
Data Out Voltage	V_{OH}	V_{DD} = 4.75 V I_{OH} = -0.5 mA I_{COL} = 0 mA	2.4	4.2		V
	V_{OL}	V_{DD} = 5.25 V I_{OL} = 1.6 mA I_{COL} = 0 mA		0.2	0.4	V
Power Dissipation Per Package[3]	P_D	V_{DD} = 5.0 V V_{COL} = 3.5 V 17.5% DF V_B = 2.4 V 15 LEDs ON per Character				
HCMS-2000/-2001/-2002/-2003/-2004				414		mW
HCMS-2300				414		
HCMS-2301/-2302/-2303/-2304				481		
Thermal Resistance IC Junction-to-Pin[4]	$R\theta_{J\text{-}PIN}$					
HCMS-2000/-2001/-2002/-2003/-2004				25		°C/W
HCMS-2300/-2301/-2302/-2303/-2304				10		

*All typical values specified at V_{DD} = 5.0 V and T_A = 25°C.

Notes:
1. I_{DD} Dynamic is the IC current while clocking column data through the on-board shift register at a clock frequency of 5MHz, the display is not illuminated.
2. I_{DD} Static is the IC current after column data is loaded and not being clocked through the on-board shift register.
3. Four characters are illuminated with a typical ASCII character composed of 15 dots per character.
4. IC junction temperature $T_J(IC) = (P_D)(R\theta_{J\text{-}PIN} + R\theta_{PC\text{-}A}) + T_A$

Optical Characteristics at $T_A = 25°C$

Standard Red HCMS-2000/-2300

Description	Symbol	Test Condition	Min.	Typ.*	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2000 HCMS-2300	I_{vPEAK}	V_{DD} = 5.0 V, V_{COL} = 3.5 V, V_B = 2.4 V, T_j = 25°C[7]	105 130	200 300		µcd
Dominant Wavelength[8]	λ_d			639		nm
Peak Wavelength	λ_{PEAK}			655		nm

Yellow HCMS-2001/-2301

Description	Symbol	Test Condition	Min.	Typ.*	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2001 HCMS-2301	I_{vPEAK}	V_{DD} = 5.0 V, V_{COL} = 3.5 V, V_B = 2.4 V, T_j = 25°C[7]	400 650	750 1140		µcd
Dominant Wavelength[6,8]	λ_d			585		nm
Peak Wavelength	λ_{PEAK}			583		nm

High Efficiency Red HCMS-2002/-2302

Description	Symbol	Test Condition	Min.	Typ.*	Max.	Unit
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2002 HCMS-2302	I_{vPEAK}	V_{DD} = 5.0 V, V_{COL} = 3.5 V, V_B = 2.4 V, T_j = 25°C[7]	400 650	1430 1430		µcd
Dominant Wavelength[8]	λ_d			625		nm
Peak Wavelength	λ_{PEAK}			635		nm

High Performance Green HCMS-2003/-2303

Description	Symbol	Test Condition	Min.	Typ.*	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2003 HCMS-2303	I_{vPEAK}	V_{DD} = 5.0 V, V_{COL} = 3.5 V, V_B = 2.4 V, T_j = 25°C[7]	850 1280	1550 2410		µcd
Dominant Wavelength[6,8]	λ_d			574		nm
Peak Wavelength	λ_{PEAK}			568		nm

Orange HCMS-2004/-2304

Description	Symbol	Test Condition	Min.	Typ.*	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2004	I_{vPEAK}	V_{DD} = 5.0 V, V_{COL} = 3.5 V, V_B = 2.4 V, T_j = 25°C[7]	400	1430		µcd
HCMS-2304			650	1430		
Dominant Wavelength[8]	λ_d			602		nm
Peak Wavelength	λ_{PEAK}			600		nm

*All typical values specified at V_{DD} = 5.0 V and T_A = 25°C unless otherwise noted.

Notes:

5. These LED displays are categorized for luminous intensity, with the intensity category designated by a letter code on the back of the package.
6. The HCMS-2001/-2301 and HCMS-2003/-2303 are categorized for color with the color category designated by a number on the back of the package.
7. T_j refers to the initial case temperature of the display immediately prior to the light measurement.
8. Dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram, and represents the single wavelength which defines the color of the device.
9. The luminous sterance of the individual LED pixels may be calculated using the following equations:

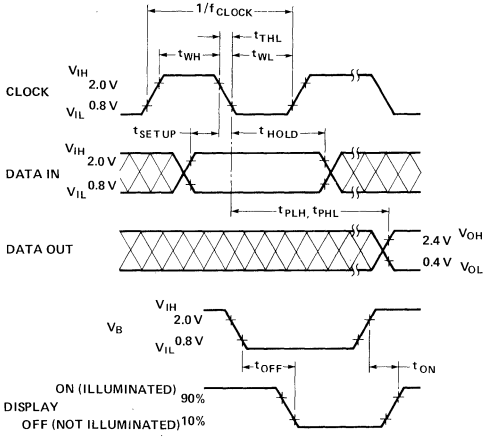
$$L_v(cd/m^2) = I_v(Candela)*DF/A(Metre)^2$$

$$L_v(Footlamberts) = \pi I_v(Candela)*DF/A(Foot)^2$$

Where: A = LED pixel area = 5.3 x $10^{-8}M^2$ or 5.8 x $10^{-7}ft^2$

DF = LED on-time duty factor

Switching Characteristics, T_A = -40°C to +85°C



Parameter	Condition	Typ.	Max.	Units
f_{CLOCK} CLOCK Rate			5	MHz
t_{PLH}, t_{PHL} Propagation Delay CLOCK to DATA OUT	C_L = 15 pF, R_L = 2.4 kΩ		105	ns
t_{OFF} V_B (0.4 V) to Display OFF		4	5	µs
t_{ON} V_B (2.4 V) to Display ON		1	2	

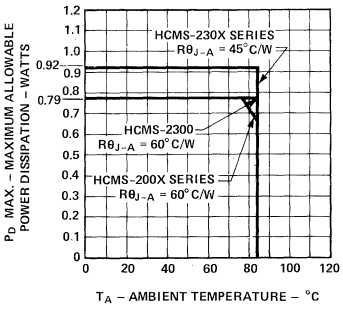


Figure 1. Maximum Allowable Power Dissipation vs Ambient Temperature as a Function of Thermal Resistance Junction-to-Ambient, $R\theta_{J-A}$. Derated Operation Assumes $R\theta_{PC-A}$ = 35°C/W Per Display for the Printed Circuit Board. T_J (IC) MAX = 125°C.

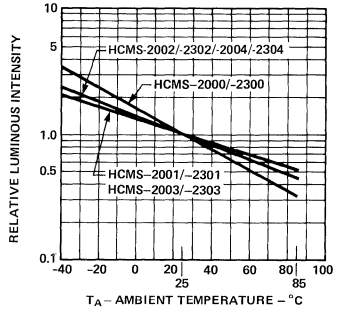


Figure 2. Relative Luminous Intensity vs Display Pin Temperature

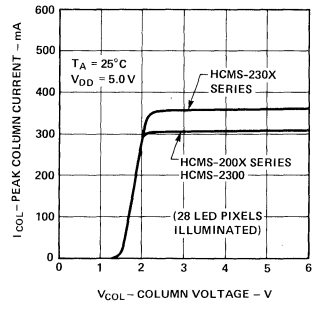


Figure 3. Peak Column Current vs Column Voltage

Electrical Description

Each display device contains four 5x7 LED dot matrix characters and two CMOS integrated circuits, as shown in Figure 4. The two CMOS integrated circuits form an on-board 28 bit serial-in-parallel-out shift register that will accept standard TTL logic levels. The Data Input, pin 12, is connected to bit position 1 and the Data Output, pin 7, is connected to bit position 28. The shift register outputs control constant current sinking LED row drivers. The nominal current sink per LED driver is 11mA for the HCMS-200X displays, 13 mA for the HCMS-230X. A logic 1 stored in the shift register enables the corresponding LED row driver and a logic 0 stored in the shift register disables the corresponding LED row driver.

The electrical configuration of these CMOS IC alphanumeric displays allows for an effective interface to a display controller circuit that supplies decoded character information. The row data for a given column (one 7 bit byte per character) is loaded (bit serial) into the on-board 28 bit shift register with high to low transitions of the Clock input. To load decoded character information into the display, column data for character 4 is loaded first and the column data for character 1 is loaded last in the following manner. The 7 data bits for column 1, character 4, are loaded into the on-board shift register. Next, the 7 data bits for column 1, character 3, are loaded into the shift register, shifting the character 4 data over one character position. This process is repeated for the other two characters until all 28 bits of column data (four 7 bit bytes of character column data) are loaded into the on-board shift register. Then the column 1 input, V_{COL} pin 1, is energized to illuminate column 1 in all four characters. This process is repeated for columns 2, 3, 4 and 5. All V_{COL} inputs should be at logic low to insure the display is off when loading data. The display will be blanked when the blanking input V_B, pin 8, is at logic low regardless of the outputs of the shift register or whether one of the V_{COL} inputs is energized.

Refer to Application Note 1016 for drive circuit information.

ESD Susceptibility

The HCMS-200X/-230X series displays have an ESD susceptibility ratings of CLASS 3 per DOD-STD-1686 and CLASS B per MIL-STD-883C. It is recommended that normal CMOS handling precautions be observed with these devices.

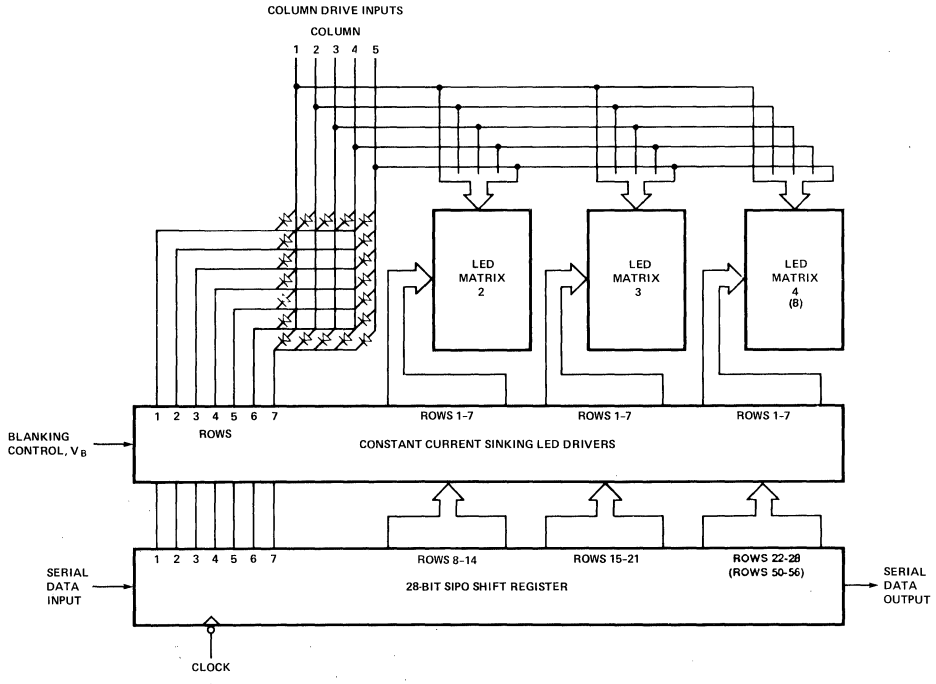


Figure 4. Block Diagram of an HCMS-2XXX Series LED Alphanumeric Display.

Soldering and Post Solder Cleaning

These displays may be soldered with a standard wave solder process using either an RMA flux and solvent cleaning or an OA flux and aqueous cleaning. For optimum soldering, the solder wave temperature should be 245°C and the dwell time for any display lead passing through the wave should be 1 1/2 to 2 seconds. The recommended solvent for post solder cleaning is Genesolv DES, manufactured by Allied Chemical. For aqueous cleaning, a water temperature of 60°C (140°F) with an immersion time not exceeding 15 minutes is recommended. For more detailed information, refer to Application Note 1027 *Soldering LED Components.*

Contrast Enhancement

When used with the proper contrast enhancement filters, the HCMS-200X/-230X series displays are readable in bright ambients. Refer to Application Note 1029 *Luminous Contrast and Sunlight Readability of the HDSP-238X Series Alphanumeric Displays for Military Applications* for contrast enhancement in bright ambients. Refer to Application Note 1015 *Contrast Enhancement Techniques for LED Displays* for information on contrast enhancement in moderate ambients.

Controller Circuits, Power Calculations and Display Dimming

Refer to Application Note 1016 *Using the HDSP-2000 Alphanumeric Display Family* for information on controller circuits to drive these displays, how to do power calculations and a technique for display dimming.

HEWLETT PACKARD

Large 5 X 7 Dot Matrix Alphanumeric Displays 17.3/26.5 mm Character Heights

Technical Data

HDSP-440X Series
HDSP-450X Series
HDSP-470X Series
HDSP-510X Series
HDSP-540X Series
HDSP-L10X Series
HDSP-L20X Series
HDSP-M10X Series

Features

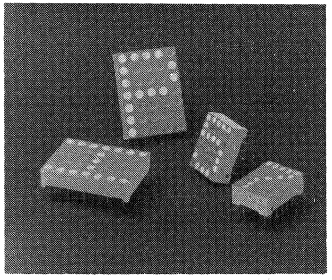
- **Multiple Colors Available**
- **Large Character Height**
- **5 X 7 Dot Matrix Font**
- **Viewable Up to 18 Meters (26.5 mm Display)**
- **X-Y Stackable**
- **Ideal for Graphics Panels**
- **Available in Common Row Anode and Common Row Cathode Configurations**
- **AlGaAs Displays Suitable for Low Power or Bright Ambients**
  Typical Intensity 1650 mcd at 2 mA Average Drive Current
- **Categorized for Intensity**
- **Mechanically Rugged**
- **Green Categorized for Color**

Description

The large 5 X 7 dot matrix alphanumeric display family consists of 26.5 mm (1.04 inch) and 17.3 mm (0.68 inch) character height packages. These devices have excellent viewability; the 26.5 mm character can be read at up to 18 meters (12 meters for the 0.68 inch part).

The 26.5 mm font has a 10.2 mm (0.4 inch) dual-in-line (DIP) configuration, while the 17.3 mm font has an industry standard 7.6 mm (0.3 inch) DIP configuration.

The HDSP-L203/4503 can be ordered with a smart driver IC. Information about the IC is available in the Smart Display Sets data sheet. For ordering information see the HP Smart Display Sets data sheet.



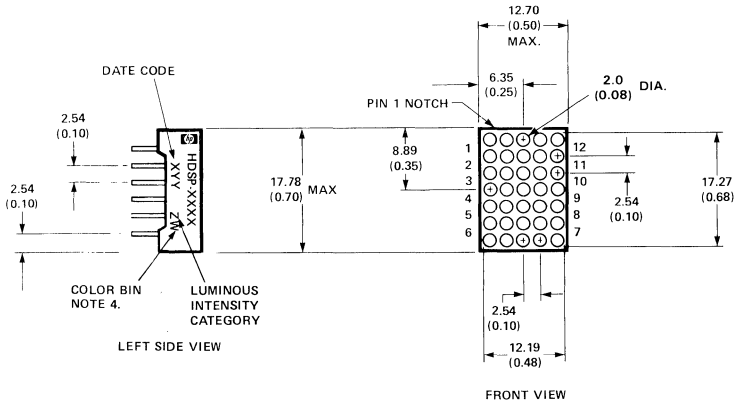
Applications include electronic instrumentation, computer peripherals, point of sale terminals, weighing scales, and industrial electronics.

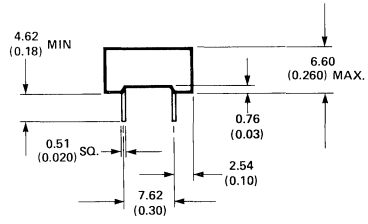
Devices

Standard Red	AlGaAs Red	High Efficiency Red	High Performance Green	Description
HDSP-4701	HDSP-L101	HDSP-L201	HDSP-5401	17.3 mm Common Row Anode
HDSP-4703	HDSP-L103	HDSP-L203	HDSP-5403	17.3 mm Common Row Cathode
HDSP-4401	HDSP-M101	HDSP-4501	HDSP-5101	26.5 mm Common Row Anode
HDSP-4403	HDSP-M103	HDSP-4503	HDSP-5103	26.5 mm Common Row Cathode

Package Dimensions

HDSP-470X/L10X/L20X/540X Series

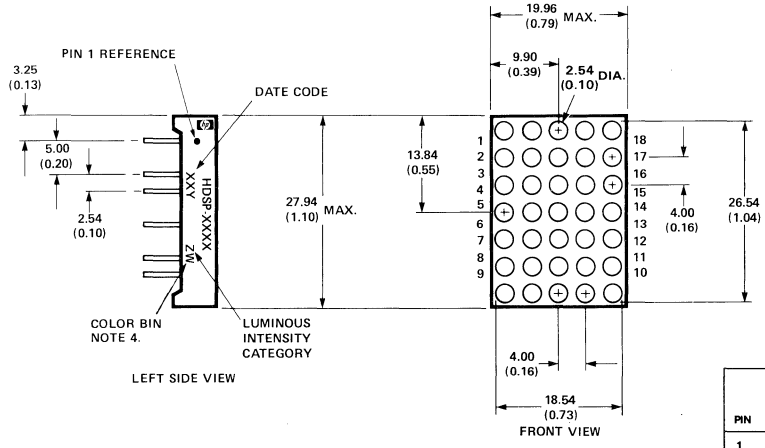


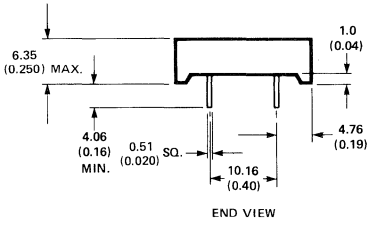


PIN	FUNCTION	
	HDSP-4701/-5401/ L101/L201	HDSP-4703/-5403/ L103/L203
1	COLUMN 1 CATHODE	ROW 1 CATHODE
2	ROW 3 ANODE	ROW 2 CATHODE
3	COLUMN 2 CATHODE	COLUMN 2 ANODE
4	ROW 5 ANODE	COLUMN 1 ANODE
5	ROW 6 ANODE	ROW 6 CATHODE
6	ROW 7 ANODE	ROW 7 CATHODE
7	COLUMN 4 CATHODE	COLUMN 3 ANODE
8	COLUMN 5 CATHODE	ROW 5 CATHODE
9	ROW 4 ANODE	COLUMN 4 ANODE
10	COLUMN 3 CATHODE	ROW 4 CATHODE
11	ROW 2 ANODE	ROW 3 CATHODE
12	ROW 1 ANODE	COLUMN 5 ANODE

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. A NOTCH ON SCRAMBLER SIDE DENOTES PIN 1.
4. FOR GREEN ONLY.

HDSP-440X/M10X/450X/510X Series



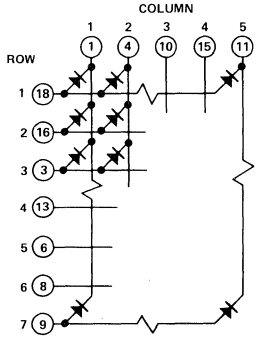


PIN	FUNCTION	
	HDSP-4401/-M101/ -4501/-5101	HDSP-4403/-M103/ -4503/-5103
1	COLUMN 1 CATHODE	ROW 1 CATHODE
2	NO PIN	NO PIN
3	ROW 3 ANODE	COLUMN 3 ANODE
4	COLUMN 2 CATHODE	ROW 3 CATHODE
5	NO PIN	NO PIN
6	ROW 5 ANODE	COLUMN 1 ANODE
7	NO PIN	NO PIN
8	ROW 6 ANODE	COLUMN 2 ANODE
9	ROW 7 ANODE	ROW 7 CATHODE
10	COLUMN 3 CATHODE	ROW 6 CATHODE
11	COLUMN 5 CATHODE	COLUMN 4 ANODE
12	NO PIN	NO PIN
13	ROW 4 ANODE	ROW 5 CATHODE
14	NO PIN	NO PIN
15	COLUMN 4 CATHODE	ROW 4 CATHODE
16	ROW 2 ANODE	ROW 2 CATHODE
17	NO PIN	NO PIN
18	ROW 1 ANODE	COLUMN 5 ANODE

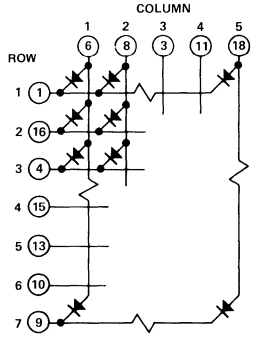
NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. A BLACK DOT ON SCRAMBLER SIDE INDICATES PIN #1.
4. FOR GREEN ONLY.

Internal Circuit Diagrams

HDSP-4401/M101/4501/5101
COMMON ANODE ROW

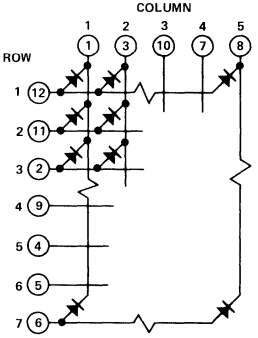


HDSP-4403/M103/4503/5103
COMMON CATHODE ROW

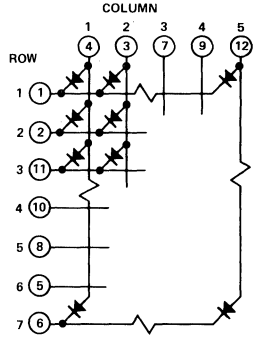


X = ROW OR COLUMN NUMBER, (X) = PIN NUMBER

HDSP-4701/L101/L201/5401
COMMON ANODE ROW



HDSP-4703/L103/L203/5403
COMMON CATHODE ROW



X = ROW OR COLUMN NUMBER, (X) = PIN NUMBER

Absolute Maximum Ratings at 25°C

Description	HDSP-470X/ 440X Series	HDSP-L10X/ M10X Series	HDSP-L20X/ 450X Series	HDSP-540X/ 510X Series
Average Power per Dot (T_A = 25°C)[1]	75 mW			
Peak Forward Current per Dot (T_A = 25°C)[1,2]	125 mA	125 mA	90 mA	90 mA
Average Forward Current per Dot (T_A = 25°C)[1,3]	32 mA	23 mA	15 mA	15 mA
Operating Temperature Range	-40°C to +85°C	-20°C to +85°C	-40°C to +85°C	-20°C to +85°C
Storage Temperature Range	-40°C to +85°C			
Lead Solder Temperature (1.59 mm [0.062 in.] below seating plane)	260°C for 3 s			

Notes:
1. Average power is based on 20 dots per character. Total package power dissipation should not exceed 1.5 W.
2. Do not exceed maximum average current per dot.
3. For the HDSP-440X/470X series displays, derate maximum average current above 35°C at 0.43 mA/°C. For the HDSP-L10X/M10X series displays, derate maximum average current above 35°C at 0.31 mA/°C. For the HDSP-L20X/450X series and HDSP-540X/510X series displays, derate maximum average current above 35°C at 0.2 mA/°C. This derating is based on a device mounted in a socket having a thermal resistance junction to ambient of 50°C/W per package.

Electrical/Optical Characteristics at T_A = 25°C

Standard Red HDSP-440X/470X Series

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Dot[4] (Digit Average)	I_V	100 mA pk: 1 of 5 Duty Factor (20 mA Avg.)				
HDSP-470X (17.3 mm)			360	770		µcd
HDSP-440X (26.5 mm)			400	800		
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[5]	λ_d			640		nm
Forward Voltage	V_F	I_F = 100 mA		1.8	2.2	V
Reverse Voltage[6]	V_R	I_R = 100 µA	3.0	12		V
Temperature Coefficient of V_F	ΔV_F/°C			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin per package						
HDSP-470X	$R\theta_{J\text{-}PIN}$			15		°C/W/
HDSP-440X				13		PACK

AlGaAs Red HDSP-L10X/M10X Series

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Dot[4] (Digit Average)	I_V	10 mA pk: 1 of 5 Duty Factor (2 mA Avg.)				
HDSP-L10X (17.3 mm)			730	1650		µcd
HDSP-M10X (26.5 mm)			760	1850		
Luminous Intensity/Dot[4] (Digit Average)	I_V	30 mA pk: 1 of 14 Duty Factor (2.1 mA Avg.)				
HDSP-L10X				1750		µcd
HDSP-M10X				1980		
Peak Wavelength	λ_{PEAK}			645		nm
Dominant Wavelength[5]	λ_d			637		nm
Forward Voltage	V_F	I_F = 10 mA		1.7	2.1	V
Reverse Voltage[6]	V_R	I_R = 100 µA	3.0	15.0		V
Temperature Coefficient of V_F	ΔV_F/°C			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin per package						
HDSP-L10X	$R\theta_{J\text{-}PIN}$			20		°C/W/
HDSP-M10X				18		PACK

High Efficiency Red HDSP-450X/L20X Series

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Dot[4] (Digit Average)	I_V	50 mA pk: 1 of 5 Duty Factor (10 mA Avg.)				
HDSP-L20X (17.3 mm)			1150	2800		µcd
HDSP-450X (26.5 mm)			1400	3500		
Luminous Intensity/Dot[4] (Digit Average)	I_V	30 mA pk: 1 of 14 Duty Factor (2.1 mA Avg.)				
HDSP-L20X				740		µcd
HDSP-450X				930		
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[5]	λ_d			626		nm
Forward Voltage	V_F	I_F = 50 mA		2.6	3.5	V
Reverse Voltage[6]	V_R	I_R = 100 µA	3.0	25.0		V
Temperature Coefficient of V_F	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin per package						
HDSP-L20X	$R\theta_{J\text{-}PIN}$			15		°C/W/
HDSP-450X				13		PACK

High Performance Green HDSP-540X/510X Series

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Dot[4] (Digit Average)	I_V	50 mA pk: 1 of 5 Duty Factor (10 mA Avg.)				
HDSP-540X (17.3 mm)			1290	4000		µcd
HDSP-510X (26.5 mm)			1540	4500		
Luminous Intensity/Dot[4] (Digit Average)	I_V	30 mA pk: 1 of 14 Duty Factor (2.1 mA Avg.)				
HDSP-540X				570		µcd
HDSP-510X				630		
Peak Wavelength	λ_{PEAK}			566		nm
Dominant Wavelength[5,7]	λ_d			571		nm
Forward Voltage	V_F	I_F = 50 mA		2.6	3.5	V
Reverse Voltage[6]	V_R	I_R = 100 µA	3.0	25.0		V
Temperature Coefficient of V_F	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin per package						
HDSP-540X	$R\theta_{J\text{-}PIN}$			15		°C/W/
HDSP-510X				13		PACK

Notes:

4. The displays are categorized for luminous intensity with the intensity category designated by a letter on the left hand side of the package. The luminous intensity minimum and categories are determined by computing the numerical average of the individual dot intensities.
5. The dominant wavelength is derived from the C.I.E. Chromaticity diagram and is that single wavelength which defines the color of the device.
6. Typical specification for reference only. Do not exceed absolute maximum ratings.
7. The displays are categorized for dominant wavelength with the category designated by a number adjacent to the intensity category letter.

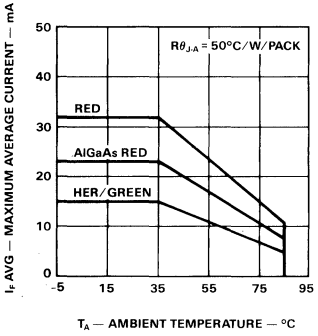


Figure 1. Maximum Allowable Average Current Per Dot as a Function of Ambient Temperature.

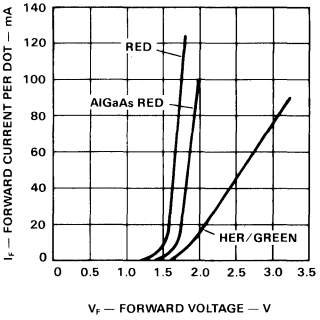


Figure 2. Forward Current vs. Forward Voltage.

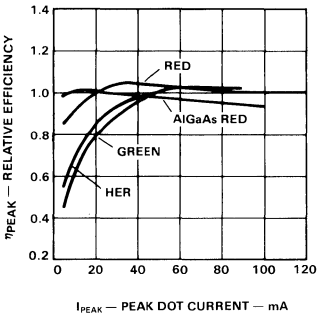


Figure 3. Relative Efficiency (Luminous Intensity per Unit Dot) vs. Peak Current per Dot.

Operational Considerations

Electrical Description

These display devices are composed of light emitting diodes, with the light from each LED optically stretched to form individual dots.

These display devices are well suited for strobed operation. The typical forward voltage values can be scaled from Figure 2. These values should be used to calculate the current limiting resistor value and the typical power dissipation. Expected maximum V_F values, for driver circuit design and maximum power dissipation, may be calculated using the following V_FMAX models:

Red (HDSP-440X/470X):
$V_F MAX = 1.55\ V + I_{Peak}(6.5\Omega)$
For $I_{Peak} \geq 5$ mA

AlGaAs Red (HDSP-L10X/M10X):
$V_F MAX = 1.8\ V + I_{Peak}(20\Omega)$
For $I_{Peak} \leq 20$ mA
$V_F MAX = 2.0\ V + I_{Peak}(10\Omega)$
For $I_{Peak} \geq 20$ mA

HER (HDSP-450X/L20X):
$V_F MAX = 1.75\ V + I_{Peak}(35\Omega)$
For $I_{Peak} \geq 5$ mA

Green (HDSP-540X/510X):
$V_F MAX = 1.75\ V + I_{Peak}(38\Omega)$
For $I_{Peak} \geq 5$ mA

Figure 3 allows the designer to calculate the luminous intensity at different peak and average currents. The following equation calculates intensity at different peak and average currents:

$I_V AVG = (I_F AVG/I_F AVG$ DATA SHEET$)(\eta_{peak})(I_V$ DATA SHEET)

Where:
$I_F AVG$ is the desired time averaged LED current.
$I_F AVG$ DATA SHEET is the time averaged data sheet test current for I_VDATA SHEET.
η_{peak} is the relative efficiency at the peak current, scaled from Figure 3.
I_V DATA SHEET is the time averaged data sheet luminous intensity, resulting from $I_F AVG$ DATA SHEET.
$I_V AVG$ is the calculated time averaged luminous intensity resulting from $I_F AVG$.

For example, what is the luminous intensity of an AlGaAs Red (HDSP-L10X) driven at 50 mA peak 1/5 duty factor?

$I_F AVG = 50$ mA * 0.2 = 10 mA
$I_F AVG$ DATA SHEET = 2 mA
$\eta_{peak} = 0.98$
I_V DATA SHEET = 1650 µcd

Therefore

$I_V AVG = (10$ mA/2 mA$)(0.98)$ (1650 µcd) = 8085 µcd

Circuit Design

Smart IC Circuit

HDSP-L203/4503 displays can be ordered with a smart IC driver. Information about the IC is available in the Smart Display data sheet. For ordering information see the HP Smart Displays Sets data sheet.

Thermal Considerations

The device thermal resistance may be used to calculate the junction temperature of the central LED. The equation below calculates the junction temperature of the central (hottest) LED.

$$T_J = T_A + (P_D)(R\theta_{J\text{-}A})(N)$$
$$P_D = (V_F MAX)(I_F AVG)$$
$$R\theta_{J\text{-}A} = R\theta_{J\text{-}PIN} + R\theta_{PIN\text{-}A}$$

T_J is the junction temperature of the central LED.
T_A is the ambient temperature.
P_D is the power dissipated by one LED.
N is the number of LEDs ON per character.
$V_F MAX$ is calculated using the appropriate V_F model.
$R\theta_{J\text{-}A}$ is the package thermal resistance from the central LED to the ambient.
$R\theta_{J\text{-}PIN}$ is the package thermal resistance from the central LED to pin.
$R\theta_{PIN\text{-}A}$ is the package thermal resistance from the pin to the ambient.

For example, what is the maximum ambient temperature an HDSP-L10X can operate with the following conditions:

$I_{PEAK} = 125$ mA
$I_F AVG = 10$ mA
$R\theta_{J\text{-}A} = 50°C/W$
N = 35
$T_J MAX = 110°C$

$V_F MAX = 2.0$ V + (0.125 A)(10)
= 3.25 V
$P_D = (3.25$ V$)(0.01$ A$)$
= 0.0325 W
$T_A = 110°C -$
(50°C/W)(0.0325 W)(35)
= 53°C

The maximum number of dots ON for the ASCII character set is 20. What is the maximum ambient temperature an HDSP-L10X can operate with the following conditions:

$I_{PEAK} = 125$ mA
$I_F AVG = 10$ mA
$R\theta_{J\text{-}A} = 50°C/W$
N = 20
$T_J MAX = 110°C$

$V_F MAX = 3.25$ V
$P_D = 0.0325$ W
$T_A = 110°C -$
(50°C/W)(0.0325 W)(20)
= 77°C

Therefore, the maximum ambient temperature can be increased by reducing the average number of dots ON from 35 to 20 dots ON per display.

Contrast Enhancement

For information on contrast enhancement please see Application Note 1015.

For Soldering/Cleaning information on soldering LEDs please refer to Application Note 1027.

HEWLETT PACKARD

HEXADECIMAL AND NUMERIC DISPLAYS

5082-7300
5082-7302
5082-7304
5082-7340

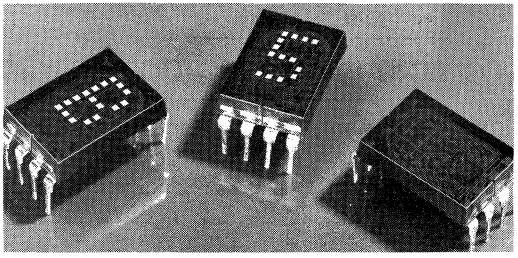
Features

- **NUMERIC**
  5082-7300/-7302
  0-9, Test State, Minus Sign, Blank States, Decimal Point
  7300 Right Hand D. P.
  7302 Left Hand D.P.
- **HEXADECIMAL**
  5082-7340
  0-9, A-F, Base 16 Operation, Blanking Control, Conserves Power, No Decimal Point
- **TTL COMPATIBLE**
- **INCLUDES DECODER/DRIVER WITH MEMORY**
  8421 Positive Logic Input
- **4 x 7 DOT MATRIX ARRAY**
  Shaped Character, Excellent Readability
- **STANDARD DUAL-IN-LINE PACKAGE INCLUDING CONTRAST FILTER**
  15.2 mm x 10.2 mm (0.6 inch x 0.4 inch)
- **CATEGORIZED FOR LUMINOUS INTENSITY**

Description

The HP 5082-7300 series solid state numeric and hexadecimal displays with on-board decoder/driver and memory provide 7.4 mm (0.29 inch) displays for reliable, low-cost methods of displaying digital information.

The 5082-7300 numeric display decodes positive 8421 BCD logic inputs into characters 0-9, a "—" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point.



The 5082-7302 is the same as the 5082-7300, except that the decimal point is located on the left-hand side of the digit.

The 5082-7340 hexadecimal display decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LEDs off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

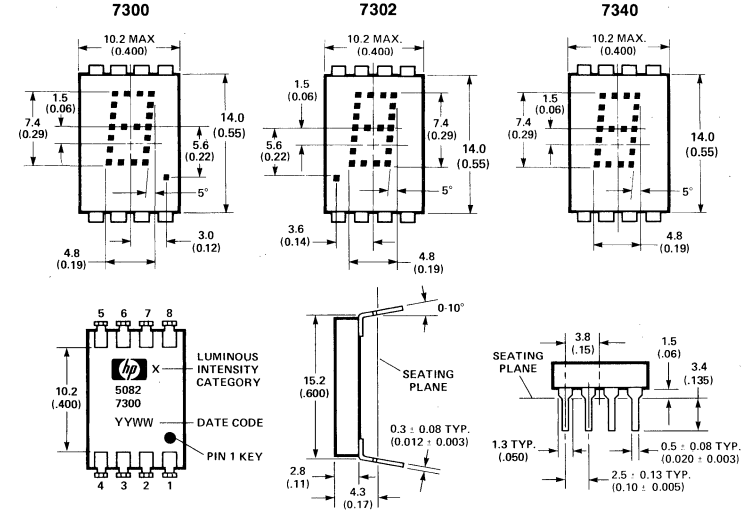
The 5082-7304 is a (±1) overrange display including a right-hand decimal point.

The ESD susceptibility of these IC devices is Class A of MIL-STD-883 or Class 2 of DOD-STD-1686 and DOD-HDBK-263.

Applications

Typical applications include point-of-sale terminals, instrumentation, and computer system.

Package Dimensions



Pin	Function	
	5082-7300 and 7302 Numeric	5082-7340 Hexadecimal
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal Point	Blanking Control
5	Latch Enable	Latch Enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

Notes:
1. Dimensions in millimeters and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±0.38 mm (± 0.015 inch).
3. Digit center line is ±0.25 mm (±0.01 inch) from package center line.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	-40	+100	°C
Operating temperature, case[1,2]	T_C	-20	+85	°C
Supply voltage[3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	+7.0	V
Voltage applied to blanking input[7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ⩽ 5 seconds			230	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, case	T_C	-20		+85	°C
Enable Pulse Width	t_W	120			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics (T_C = -20° C to +85° C, Unless Otherwise Specified)

Description	Symbol	Test Conditions	Min.	Typ.[4]	Max.	Unit
Supply Current	I_{CC}	V_{CC} = 5.5 V (characters		112	170	mA
Power dissipation	P_T	"5." or "B" displayed)		560	935	mW
Luminous intensity per LED (Digit average)[5,6]	I_v	V_{CC}=5.0V, T_C = 25° C	32	70		μcd
Logic low-level input voltage	V_{IL}				0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}	V_{CC}=4.5V			0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked[7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked[7]	V_{BH}		3.5			V
Blanking low-level input current[7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			20	μA
Blanking high-level input current[7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			2.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+250	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+250	μA
Peak wavelength	λ_{PEAK}	T_C = 25° C		655		nm
Dominant Wavelength[8]	λ_d	T_C = 25° C		640		nm
Weight				0.8		gm

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA} = 50° C/W; Θ_{JC} = 15° C/W; 2. Θ_{CA} of a mounted display should not exceed 35° C/W for operation up to T_C =+85° C. 3.Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC} = 5.0 Volts, T_A = 25° C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific case temperature, $I_V(T_C)$ may be calculated from this relationship: $I_V(T_C) = I_V$ (25° C) e [-0.0188/° C($T_{C-25°C}$)] 7. Applies only to 7340. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

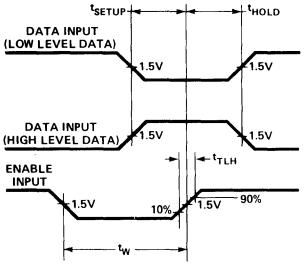


Figure 1. Timing Diagram of 5082-7300 Series Logic.

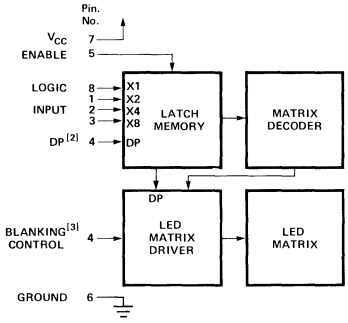


Figure 2. Block Diagram of 5082-7300 Series Logic.

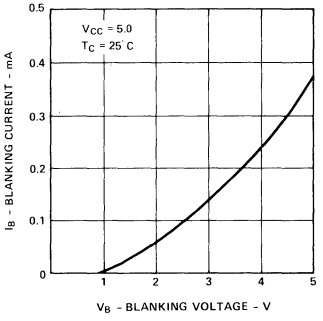


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7340.

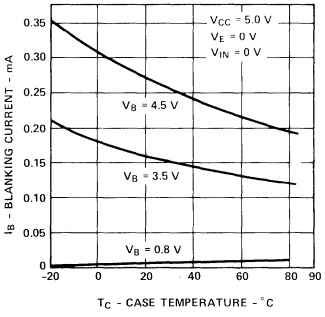


Figure 4. Typical Blanking Control Input Current vs. Temperature, 5082-7340.

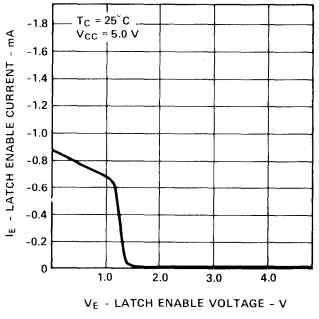


Figure 5. Typical Latch Enable Input Current vs. Voltage for the 5082-7300 Series Devices.

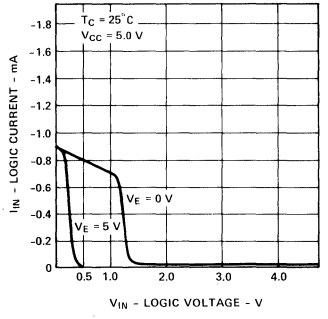


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage for the 5082-7300 Series Devices. Decimal Point Applies to 5082-7300 and -7302 Only.

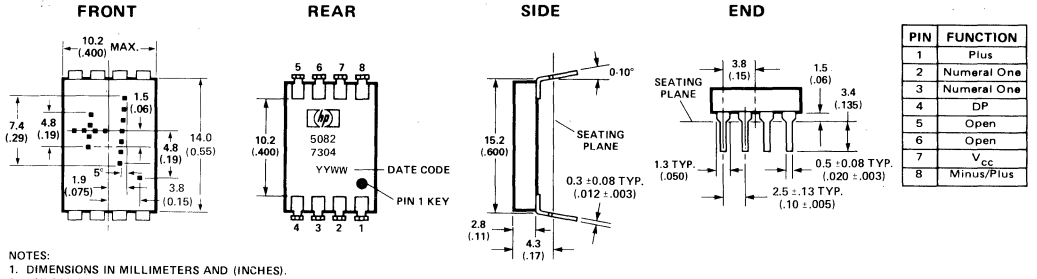
TRUTH TABLE					
BCD DATA[1]				5082-7300/7302	5082-7340
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L		A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	----	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE[1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING[3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7300 and 5082-7302 displays.
3. The blanking control input, B, pertains only to the 5082-7340 hexadecimal display. Blanking input has no effect upon display memory.

Solid State Over Range Display

For display applications requiring a ±, 1, or decimal point designation, the 5082-7304 over range display is available. This display module comes in the same package as the 5082-7300 series numeric display and is completely compatible with it.

Package Dimensions



PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{cc}
8	Minus/Plus

NOTES:
1. DIMENSIONS IN MILLIMETERS AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±0.38 MM (±0.015 INCHES).

5082-7304

TRUTH TABLE FOR 5082-7304

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 7 cutoff.
H: Line switching transistor in Figure 7 saturated.
X: 'Don't care'

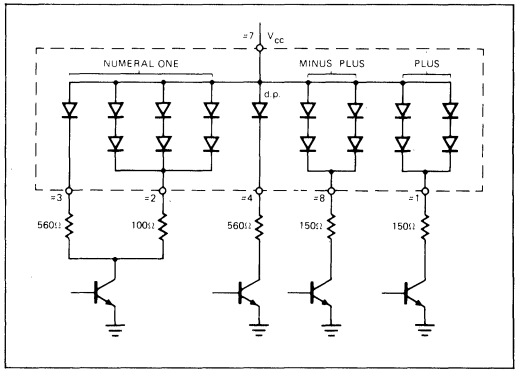


Figure 7. Typical Driving Circuit for 5082-7304

Recommended Operating Conditions

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 7 for recommended resistor values.

Absolute Maximum Ratings

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	–40	+100	°C
Operating temperature, case	T_C	–20	+85	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

Electrical/Optical Characteristics

5082-7358 (T_C = –20° C to +85° C; Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		250	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	32	70		µcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λd	T_C = 25°C		640		nm
Weight				0.8		gm

HEWLETT PACKARD

HEXADECIMAL AND NUMERIC DISPLAYS FOR INDUSTRIAL APPLICATIONS

5082-7356
5082-7357
5082-7358
5082-7359

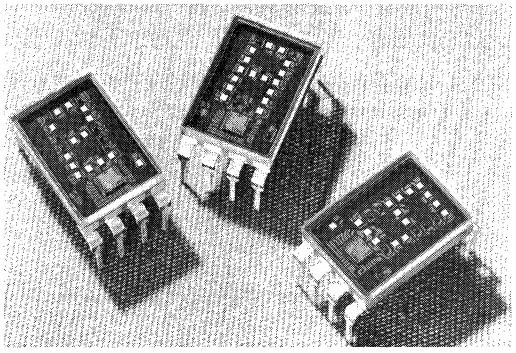
Features

- **CERAMIC/GLASS PACKAGE**
- **ADDED RELIABILITY**
- **NUMERIC 5082-7356/-7357**
  0-9, Test State, Minus Sign, Blank States, Decimal Point
  7356 Right Hand D.P., 7357 Left Hand D.P.
- **HEXADECIMAL 5082-7359**
  0-9, A-F, Base 16 Operation, Blanking Control, Conserves Power, No Decimal Point
- **TTL COMPATIBLE**
- **INCLUDES DECODER/DRIVER WITH MEMORY**
  8421 Positive Logic Input
- **4 x 7 DOT MATRIX ARRAY**
  Shaped Character, Excellent Readability
- **STANDARD DUAL-IN-LINE PACKAGE**
  15.2 mm x 10.2 mm (0.6 inch x 0.4 inch)
- **CATEGORIZED FOR LUMINOUS INTENSITY**

Description

The HP 5082-735X series solid state numeric and hexadecimal displays with on-board decoder/driver and memory provide 7.4 mm (0.29 inch) displays for use in adverse industrial environments.

The 5082-7356 numeric display decodes positive 8421 BCD logic inputs into characters 0-9 "—" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point.



The 5082-7357 is the same as the 5082-7356, except that the decimal point is located on the left-hand side of the digit.

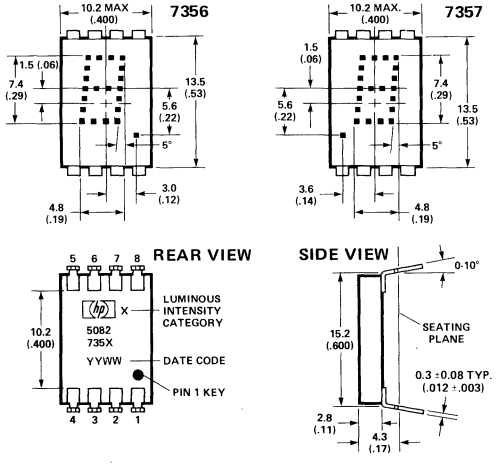
The 5082-7359 hexadecimal display decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

The 5082-7358 is a (±1) overrange display including a right-hand decimal point.

Applications

Typical applications include control systems, instrumentation, communication systems, and transportation equipment.

Package Dimensions



PIN	FUNCTION	
	5082-7356 AND 7357 NUMERIC	5082-7359 HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimeters and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ± 0.38mm (±0.015 in.)
3. Digit center line is ± 0.25mm (±0.01 in.) from package center line.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1,2]	T_A	−55	+100	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	+7.0	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ⩽ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient	T_A	-55		+85	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics (T_A = -55° C to +85° C, Unless Otherwise Specified)

Description	Symbol	Test Conditions	Min.	Typ.[4]	Max.	Unit
Supply Current	I_{CC}	V_{CC} = 5.5 V (characters		112	170	mA
Power dissipation	P_T	"5." or "B" displayed)		560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_A=25° C	40	85		μcd
Logic low-level input voltage	V_{IL}				0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}	V_{CC}=4.5V			0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			50	μA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			1.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+100	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+130	μA
Peak wavelength	λ_{PEAK}	T_A=25° C		655		nm
Dominant Wavelength [8]	λ_d	T_A=25° C		640		nm
Weight				1.0		gm

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50° C/W; Θ_{JC}=15° C/W; 2. Θ_{CA} of a mounted display should not exceed 35° C/W for operation up to T_A=+100° C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_A=25° C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship: $I_V(T_A)=I_{V(25°C)}(.985)^{[T_A-25°C]}$ 7. Applies only to 7359. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

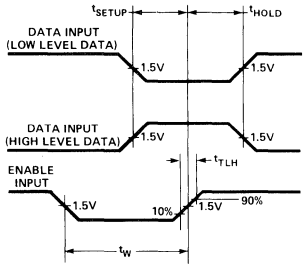


Figure 1. Timing Diagram of 5082-735X Series Logic.

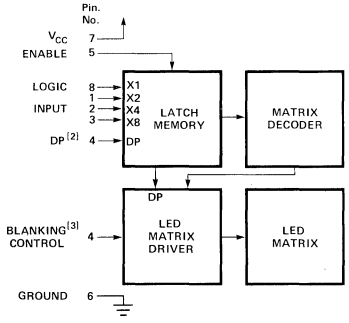


Figure 2. Block Diagram of 5082-735X Series Logic.

TRUTH TABLE					
BCD DATA[1]				5082-7356/7357	5082-7359
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L		A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	....	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE[1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING[3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7356 and 5082-7357 displays.
3. The blanking control input, B, pertains only to the 5082-7359 hexadecimal display. Blanking input has no effect upon display memory.

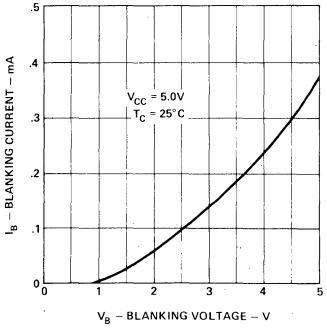


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7359.

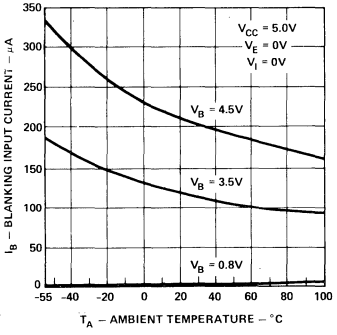


Figure 4. Typical Blanking Control Input Current vs. Ambient Temperature for 5082-7359.

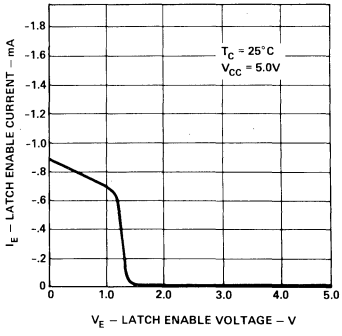


Figure 5. Typical Latch Enable Input Current vs. Voltage.

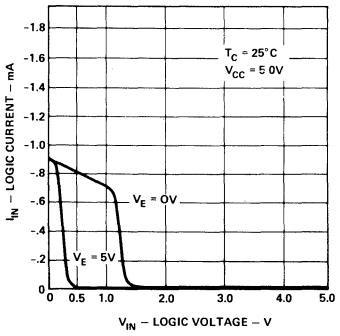


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage.

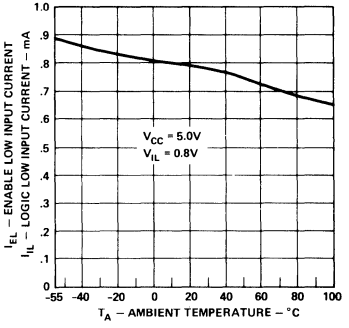


Figure 7. Typical Logic and Enable Low Input Current vs. Ambient Temperature.

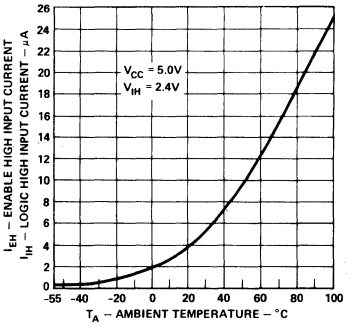


Figure 8. Typical Logic and Enable High Input Current vs. Ambient Temperature.

Operational Considerations

ELECTRICAL

The 5082-735X series devices use a modified 4 x 7 dot matrix of light emitting diodes (LED's) to display decimal/hexadecimal numeric information. The LED's are driven by constant current drivers. BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. To avoid the latching of erroneous information, the enable pulse rise time should not exceed 200 nanoseconds. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7MHz rate.

The blanking control input on the 5082-7395 display blanks (turns off) the displayed hexadecimal information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 3.5 volts. This may be easily achieved by using an open collector TTL gate and a pull-up resistor. For example, (1/6) 7416 hexinverter buffer/driver and a 120 ohm pull-up resistor will provide sufficient drive to blank eight displays. The size of the blanking pull-up resistor may be calculated from the following formula, where N is the number of digits:

$$R_{blank} = (V_{CC} - 3.5V)/[N\ (1.0mA)]$$

The decimal point input is active low true and this data is latched into the display memory in the same fashion as is the BCD data. The decimal point LED is driven by the on-board IC.

The ESD susceptibility of these IC devices is Class A of MIL-STD-883 or Class 2 of DOD-STD-1686 and DOD-HDBK-263.

MECHANICAL

These displays are designed for use in adverse industrial environments.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54mm (0.100 inch) and the lead row spacing is 15.24mm (0.600 inch). These displays may be end stacked with 2.54mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100°C, it is important to maintain a case-to-ambient thermal resistance of less than 35°C/watt as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

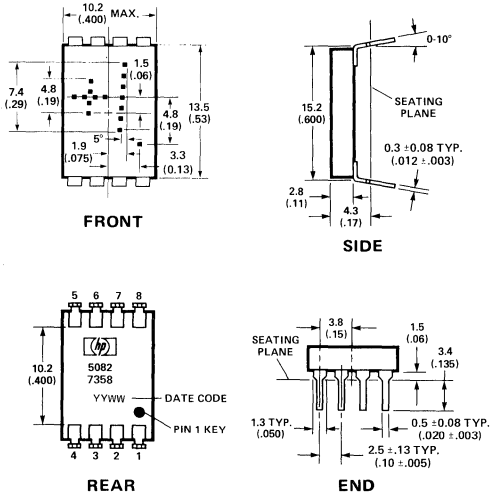
CONTRAST ENHANCEMENT

The 5082-735X displays have been designed to provide the maximum posible ON/OFF contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60 and Dark Red 63, SGL Homalite H100-1605, 3M Light Control Film and Polaroid HRCP Red Circular Polarizing Filter. For further information see Hewlett-Packard Application Note 964.

Solid State Over Range Display

For display applications requiring a ±, 1, or decimal point designation, the 5082-7358 over range display is available. This display module comes in the same package as the 5082-735X series numeric display and is completely compatible with it.

Package Dimensions



NOTES:
1. DIMENSIONS IN MILLIMETERS AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±0.38 MM (±0.015 INCHES).

PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{cc}
8	Minus/Plus

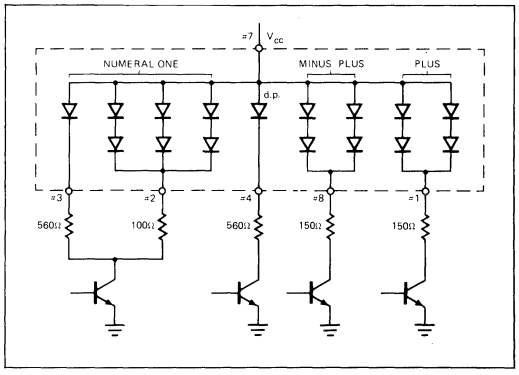


Figure 9. Typical Driving Circuit.

TRUTH TABLE

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 9 cutoff.
H: Line switching transistor in Figure 9 saturated.
X: 'Don't care'

Electrical/Optical Characteristics

5082-7358 (T_A = -55°C to +85°C, Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		280	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	40	85		μcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λ_d	T_C = 25°C		640		nm
Weight				1.0		gm

Recommended Operating Conditions

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 9 for recommended resistor values.

Absolute Maximum Ratings

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	-65	+125	°C
Operating temperature, ambient	T_A	-55	+100	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

HEWLETT PACKARD

HEXADECIMAL AND NUMERIC DISPLAYS FOR INDUSTRIAL APPLICATIONS

HIGH EFFICIENCY RED

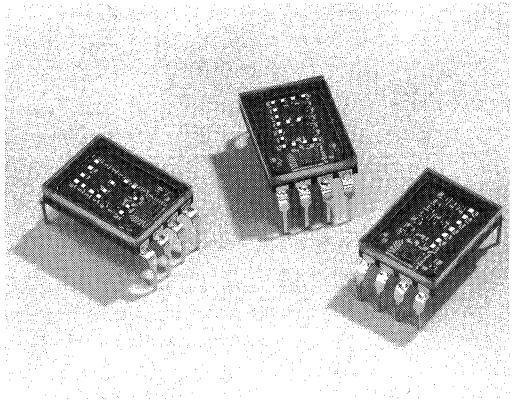
Low Power	HDSP-0760/0761/0762/0763
High Brightness	HDSP-0770/0771/0772/0773
YELLOW	HDSP-0860/0861/0862/0863
GREEN	HDSP-0960/0961/0962/0963

Features

- **THREE COLORS**
  High-Efficiency Red
  Yellow
  High Performance Green
- **THREE CHARACTER OPTIONS**
  Numeric
  Hexadecimal
  Over Range
- **TWO HIGH-EFFICIENCY RED OPTIONS**
  Low Power
  High Brightness
- **PERFORMANCE GUARANTEED OVER TEMPERATURE**
- **MEMORY LATCH/DECODER/DRIVER TTL Compatible**
- **4x7 DOT MATRIX CHARACTER**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
- **YELLOW AND GREEN CATEGORIZED FOR COLOR**

Typical Applications

- **INDUSTRIAL EQUIPMENT**
- **COMPUTER PERIPHERALS**
- **INSTRUMENTATION**
- **TELECOMMUNICATION EQUIPMENT**



Description

These solid state display devices are designed and tested for use in adverse industrial environments. The character height is 7.4mm (0.29 inch). The numeric and hexadecimal devices incorporate an on-board IC that contains the data memory, decoder and display driver functions.

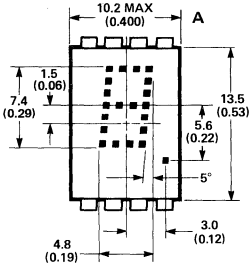
The numeric devices decode positive BCD logic into characters "0-9", a "—" sign, decimal point, and a test pattern. The hexadecimal devices decode positive BCD logic into 16 characters, "0-9, A-F". An input is provided on the hexadecimal devices to blank the display (all LED's off) without losing the contents of the memory.

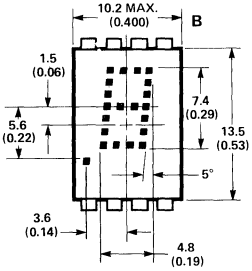
The over range device displays "±1" and right hand decimal point and is typically driven via external switching transistors.

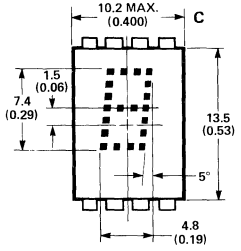
Devices

Part Number HDSP-	Color	Description	Front View
0760	High-Efficiency Red Low Power	Numeric, Right Hand DP	A
0761		Numeric, Left Hand DP	B
0762		Hexadecimal	C
0763		Over Range ±1	D
0770	High-Efficiency Red High Brightness	Numeric, Right Hand DP	A
0771		Numeric, Left Hand DP	B
0772		Hexadecimal	C
0763		Over Range ±1	D
0860	Yellow	Numeric, Right Hand DP	A
0861		Numeric, Left Hand DP	B
0862		Hexadecimal	C
0863		Over Range ±1	D
0960	Green	Numeric, Right Hand DP	A
0961		Numeric, Left Hand DP	B
0962		Hexadecimal	C
0963		Over Range ±1	D

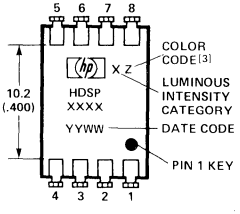
Package Dimensions

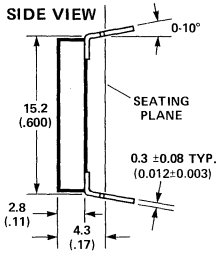


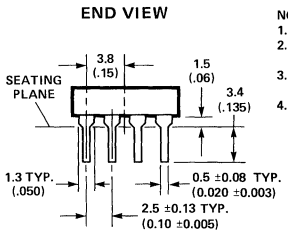




PIN	FUNCTION	
	NUMERIC	HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1







NOTES:
1. Dimensions in millimetres and (inches).
2. Digit center line is ±0.38 mm (±0.015 inch) from package center line.
3. Unless otherwise specified, the tolerance on all dimensions is ±0.38 mm (±0.015 inch).
4. HDSP-0860 and HDSP-0960 series.

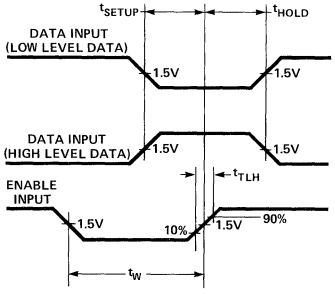


Figure 1. Timing Diagram

TRUTH TABLE					
BCD DATA[1]				NUMERIC	HEXA-DECIMAL
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	[	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	....	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE[1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING[3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels have no effect upon display memory, displayed character, or DP.
2. The decimal point input, DP, pertains only to the numeric displays.
3. The blanking control input, B, pertains only to the hexadecimal displays. Blanking input has no effect upon display memory.

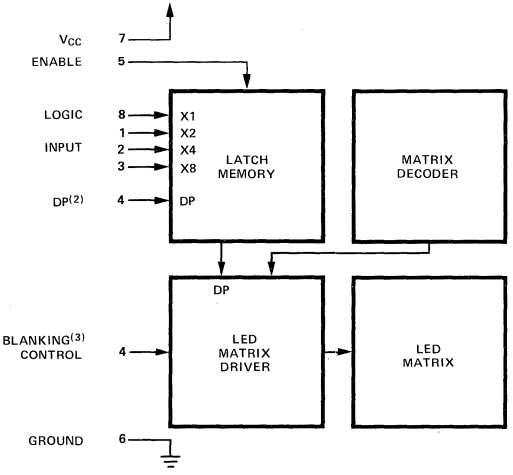


Figure 2. Logic Block Diagram

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+100	°C
Operating temperature, ambient [1]	T_A	−55	+85	°C
Supply voltage [2]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	V_{CC}	V
Voltage applied to blanking input [2]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ⩽ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage [2]	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1]	T_A	-55		+85	°C
Enable Pulse Width	t_W	.100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			1.0	msec

Optical Characteristics at T_A = 25°C, V_{CC} = 5.0V

Device	Description	Symbol	Min.	Typ.	Max.	Unit
HDSP-0760 Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	65	140		μcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength [5]	λ_d		626		nm
HDSP-0770 Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	260	620		μcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength [5]	λ_d		626		nm
HDSP-0860 Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	215	490		μcd
	Peak Wavelength	λ_{PEAK}		583		nm
	Dominant Wavelength [5,6]	λ_d		585		nm
HDSP-0960 Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	298	1100		μcd
	Peak Wavelength	λ_{PEAK}		568		nm
	Dominant Wavelength [5,6]	λ_d		574		nm

Notes:
1. The nominal thermal resistance of a display mounted in a socket that is soldered onto a printed circuit board is $R\theta_{JA}$ = 50° C/W/device. The device package thermal resistance is $R\theta_{J-PIN}$ = 15° C/W/device. The thermal resistance device pin-to-ambient through the PC board should not exceed 35° C/W/device for operation at T_A = +85° C.
2. Voltage values are with respect to device ground, pin 6.
3. These displays are categorized for luminous intensity with the intensity category designated by a letter code located on the back of the display package. Case temperature of the device immediately prior to the light measurement is equal to 25° C.

Electrical Characteristics; T_A = -55°C to +85°C

Description		Symbol	Test Conditions	Min.	Typ.[7]	Max.	Unit
Supply Current	HDSP-0760 Series	I_{CC}	V_{CC} = 5.5V (characters "5." or "B" displayed)		78	105	mA
	HDSP-0770 Series HDSP-0860 Series HDSP-0960 Series				120	175	
Power Dissipation	HDSP-0760 Series	P_T			390	573	mW
	HDSP-0770 Series HDSP-0860 Series HDSP-0960 Series				690	963	
Logic, Enable and Blanking Low-Level Input Voltage		V_{IL}	V_{CC} = 4.5V			0.8	V
Logic, Enable and Blanking High-Level Input Voltage		V_{IH}		2.0			V
Logic and Enable Low-Level Input Current		I_{IL}	V_{CC} = 5.5V			-1.6	mA
Blanking Low-Level Input Current		I_{BL}	V_{IL} = 0.4V			-10	μA
Logic, Enable and Blanking High-Level Input Current		I_{IH}	V_{CC} = 5.5V V_{IH} = 2.4V			+40	μA
Weight					1.0		gm
Leak Rate						$5x10^{-8}$	cc/sec

Notes:

4. The luminous intensity at a specific operating ambient temperature, I_V (T_A) may be approximated from the following expotential equation: I_V (T_A = I_V (25°C) $e^{K(T_A - 25°C)}$.

Device	K
HDSP-0760 Series HDSP-0770 Series	-0.0131/°C
HDSP-0860 Series	-0.0112/°C
HDSP-0960 Series	-0.0104/°C

5. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
6. The HDSP-0860 and HDSP-0960 series devices are categorized as to dominant wavelength with the category designated by a number on the back side of the display package.
7. All typical values at V_{CC} = 5.0V and T_A = 25°C.

Operational Considerations

ELECTRICAL

These devices use a modified 4 x 7 dot matrix of light emitting diode to display decimal/hexadecimal numeric information. The high efficiency red and yellow LED's are GaAsP epitaxial layer on a GaP transparent substrate. The green LED's are GaP epitaxial layer on a GaP transparent substrate. The LED's are driven by constant current drivers, BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7 MHz rate.

The decimal point input is active low true and this data is latched into the display memory in the same fashion as the BCD data. The decimal point LED is driven by the on-board IC.

The blanking control input on the hexadecimal displays blanks (turns off) the displayed information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 2.0 volts. When blanked, the display standby power is nominally 250 mW at T_A = 25°C.

MECHANICAL

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +85°C, it is important to maintain a cast-to-ambient thermal resistance of less than 35°C watt/device as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixutres formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

CONTRAST ENHANCEMENT

These display devices are designed to provide an optimum ON/OFF contrast when placed behind an appropriate contrast enhancement filter. The following filters are suggested:

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-0860 Series Yellow	Panelgraphic Yellow 27 Chequers Amber 107	Polaroid HNCP 37 3M Light Control Film Panelgraphic Gray 10 Chequers Grey 105	Polaroid Gray HNCP10 HOYA Yellowish-Orange HLF-608-3Y Marks Gray MCP-0301-8-10
HDSP-0760 Series HDSP-0770 Series High Efficiency Red	Panelgraphic Ruby Red 60 Chequers Red 112		Polaroid Gray HNCP10 HOYA Reddish-Orange HLF-608-5R Marks Gray MCP-0301-8-10 Marks Reddish-Orange MCP-0201-2-22
HDSP-0960 Series HP Green	Panelgraphic Green 48 Chequers Green 107		Polaroid Gray HNCP10 HOYA Yellow-Green HLF-608-1G Marks Yellow-Green MCP-0101-5-12

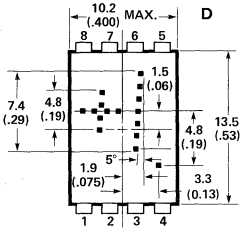
Over Range Display

The over range devices display "±1" and decimal point. The character height and package configuration are the same as the numeric and hexadecimal devices. Character selection is obtained via external switching transistors and current limiting resistors.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	-65	+100	°C
Operating Temperature Ambient	T_A	-55	+85	°C
Forward Current, Each LED	I_F		10	mA
Reverse Voltage, Each LED	V_R		5	V

Package Dimensions



FRONT VIEW

Pin	Function
1	Plus
2	Numeral One
3	Numeral One
4	DP.
5	Open
6	Open
7	V_{CC}
8	Minus/Plus

Note:
1. Dimensions in millimetres and (inches).

Character	Pin			
	1	2,3	4	8
+	1	X	X	1
—	0	X	X	1
1	X	1	X	X
Decimal Point	X	X	1	X
Blank	0	0	0	0

Notes:
0: Line switching transistor in Figure 7 cutoff.
1: Line switching transistor in Figure 7 saturated.
X: 'don't care'

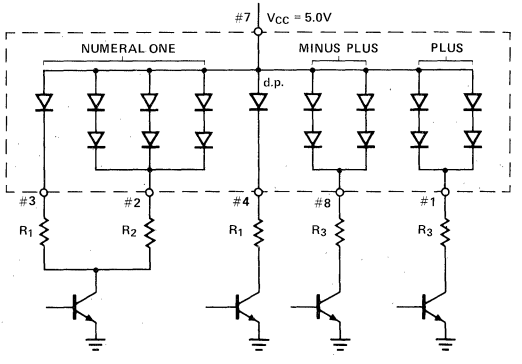


Figure 3. Typical Driving Circuit

Recommended Operating Conditions V_{CC} = 5.0V

Device		Forward Current Per LED, mA	Resistor Value		
			R_1	R_2	R_3
HDSP-0763	Low Power	2.8	1300	200	300
	High Brightness	8	360	47	68
HDSP-0863		8	360	36	56
HDSP-0963		8	360	30	43

Luminous Intensity Per LED

(Digit Average)[3,4] at T_A = 25°C

Device	Test Conditions	Min.	Typ.	Units
HDSP-0763	I_F = 2.8 mA	65	140	μcd
	I_F = 8 mA		620	μcd
HDSP-0863	I_F = 8 mA	215	490	μcd
HDSP-0963	I_F = 8 mA	298	1100	μcd

Electrical Characteristics; T_A = -55°C to +85°C

Device	Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
HDSP-0763	Power Dissipation (all LED's Illuminated)	P_T	I_F = 2.8 mA		72		mW
			I_F = 8 mA		224	282	
	Forward Voltage per LED	V_F	I_F = 2.8 mA		1.6		V
			I_F = 8 mA		1.75	2.2	
HDSP-0863	Power Dissipation (all LED's Illuminated)	P_T	I_F = 8 mA		237	282	mW
	Forward Voltage per LED	V_F			1.90	2.2	V
HDSP-0963	Power Dissipation (all LED's Illuminated)	P_T	I_F = 8 mA		243	282	mW
	Forward Voltage per LED	V_F			1.85	2.2	V

HEWLETT PACKARD

Hermetic Displays

Hermetic Displays

Military Grade Displays

Hewlett-Packard families of military grade numeric and alphanumeric LED displays are screened to the requirements of MIL-D-87157. MIL-D-87157 is the general specification for LED display devices and defines four screening levels for hermetic and nonhermetic devices, termed "Quality Levels".

Quality Level A: Hermetic displays with 100% screening and Group A, B, and C testing.
Quality Level B: Hermetic displays with Group A, B, and C testing, but without 100% screening.
Quality Level C: Nonhermetic displays with 100% screening and Group A, B, and C testing.
Quality Level D: Nonhermetic displays with Group A, B, and C testing, but without 100% screening.

The 4N5X series single digit dot matrix numeric and hexadecimal displays are listed on the MIL-D-87157 Qualified Parts List (QPL) under the number series M871570010XAAX.

Displays with TXV part numbers are 100% screened with Group A testing. Displays with TXVB part numbers are 100% screened to Quality Level A.

The applicable MIL-D-87157 screening tables are detailed on each display data sheet.

High Reliability Displays

In addition to Hewlett-Packard commercial solid state displays, Hewlett-Packard offers a complete line of hermetic packages for high reliability military and aerospace applications. These packages consist of numeric and hexadecimal displays, 5 x 7 dot matrix alphanumeric displays with extended temperature ranges, and fully intelligent monolithic 16 segment displays with extended temperature ranges and on board CMOS ICs. Similar to the commercial display product selection, the high reliability display products are offered in a variety of character sizes and colors: standard red, high efficiency red, yellow, and high performance green. Orange displays are sometimes available upon request.

Hewlett-Packard offers three different testing programs for the high reliability conscious display customer. These programs include DESC Qualification on the MIL-D-87157 for the hermetically sealed 4N51-4N54 hexadecimal and numeric displays; and two levels of in-house high reliability testing programs that conform or a modification to MIL-D-87157 Quality Level A Test Tables for all other high reliability display products. Please refer to the individual data sheets for a complete description of each display's testing program.

Integrated numeric and hexadecimal displays (with on-board ICs) solve the designer's decoding/driving problems. They are available in plastic packages for general purpose usage, ceramic/glass packages for industrial applications, and hermetic packages for high reliability applications. This family of displays has been designed for ease of use in a wide range of environments.

Hewlett-Packard's line of Solid State Displays answers all the needs of the designer. From

smart alphanumeric displays to low cost numeric displays in sizes from 3 mm (0.15 in.) to 20 mm (0.8 in.) and colors of red, AlGaAs red, high efficiency red, yellow, and high performance green, the selection is complete.

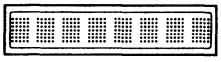
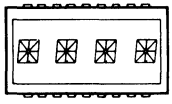
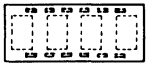
Hewlett-Packard's 5 x 7 dot matrix alphanumeric display line comes in three character sizes: 3.8 mm (0.15 in.), 5 mm (0.2 in.), and 6.9 mm (0.27 in.). In addition, there are now four colors available for each size: standard red, yellow, high efficiency red, and green. This wide selection of package sizes and colors makes these products ideal for a variety of applications in avionics, industrial control, and instrumentation.

The newest addition to HP's alphanumeric display line, the intelligent eight character, 5.0 mm (0.2 in.) alphanumeric display in the very flexible 5 x 7 dot matrix font. Product features include a low power on-board CMOS IC, ASCII decoder, the complete 128 ASCII character set, and the LED drivers. In addition, an on-board RAM offers the designer the ability to store up to 16 user-definable characters, such as foreign characters, special symbols and logos. These features make it ideal for avionics, medical, telecommunications, analytical equipment, computer products, office and industrial equipment applications.

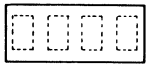
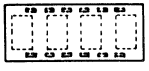
Also part of HP's alphanumeric display line is the large (0.68 in. and 1.04 in.) 5 x 7 dot matrix alphanumeric display family. This family is offered in standard red, high efficiency red, AlGaAs red, and high performance green. These displays have excellent viewability; the 1.04 inch character font can be read at up to 18 meters (12 meters for the 0.68 inch display). Applications for these large 5 x 7 displays include industrial machinery and process controllers, weighing scales, computer tape drive systems, and transportation.

Hewlett-Packard's line of numeric seven segment displays is one of the broadest. From low cost, standard red displays to high light ambient displays producing 7.5 mcd/segment, HP's 0.3 in., 0.43 in., 0.56 in., and 0.8 in. characters can provide a solution to every display need. HP's product offering includes 0.56 in. dual digit displays and a line of small package, bright 0.3 in. displays – the 0.3 in. Microbright. HP's broad line of numeric seven segment displays is ideal for electronic instrumentation, industrial, weighing scales, point-of-sale terminals, and appliance applications. Included in HP's line of numeric seven segment displays is the Double Heterojunction AlGaAs red low current sunlight viewable display family. This family is offered in the 0.3 in. Mini, 0.43 in., 0.56 in., and 0.8 in. package sizes. These AlGaAs numeric displays are very bright at low drive currents – typical intensity of 650 mcd/segment at 1 mA/segment drive. These displays are ideal for battery operated and other low power applications.

Hermetic Alphanumeric Displays

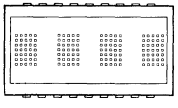
Device	P/N	Description	Color	Application	Page No.
	HDSP-2131 HDSP-2131 TXV HDSP-2131 TXVB	5.0 mm (0.20 in.) 5 x 7 Eight Character Smart Alphanumeric Display Operating Temperature Range: -55°C to +85°C TXV – Hi Rel Screened TXVB – Hi Rel Screened to Level A MIL-D-87157	Yellow	• Military Equipment • Military Avionics • Military Ground Support Systems • Military Telecommunications	4-232
	HDSP-2132 HDSP-2132 TXV HDSP-2132 TXVB		High Efficiency Red		
	HDSP-2133 HDSP-2133 TXV HDSP-2133 TXVB		High Performance Green		
	HDSP-2179 HDSP-2179 TXV HDSP-2179 TXVB		Orange		
	HMDL-2416 HMDL-2416 TXV HMDL-2416 TXVB	4.1 mm (0.16 in.) Four Character Monolithic Smart Alphanumeric Display Operating Temperature Range: -55°C to +100°C TXV – Hi Rel Screened TXVB – Hi Rel Screened to Level A MIL-D-87157	Red	• Military Equipment • High Reliability Applications • Military Telecommunications	4-251
	HCMS-2351 HCMS-2351 TXV HCMS-2351 TXVB	5.0 mm (0.20 in.) 5 x 7 Four Character Alphanumeric Sunlight Viewable Display CMOS IC Operating Temperature Range: -55°C to +100°C TXV – Hi Rel Screened TXVB – Hi Rel Screened to Level A Mil-D-87157	Yellow	• Military Avionics • Military Cockpit • Military Ground Support Systems	4-261
	HCMS-2352 HCMS-2352 TXV HCMS-2352 TXVB		High Efficiency Red		
	HCMS-2353 HCMS-2353 TXV HCMS-2353 TXVB		High Performance Green		
	HCMS-2354 HCMS-2354 TXV HCMS-2354 TXVB		Orange		

Hermetic Alphanumeric Displays (Continued)

Device	P/N	Description	Color	Application	Page No.
	HCMS-2010 HCMS-2010 TXV HCMS-2010 TXVB	3.7 mm (0.15 in.) 5 x 7 Four Character Alphanumeric CMOS IC	Red, Red Glass Contrast Filter	• Extended temperature applications requiring high reliability. • I/O Terminals • Avionics	4-261
	HCMS-2011 HCMS-2011 TXV HCMS-2011 TXVB	Operating Temperature Range: -55°C to +100°C TXV – Hi Rel Screened	Yellow		
	HCMS-2012 HCMS-2012 TXV HCMS-2012 TXVB	TXVB – Hi Rel Screened to Level A MIL-D-87157	High Efficiency Red		
	HCMS-2013 HCMS-2013 TXV HCMS-2013 TXVB		High Performance Green		
	HCMS-2310 HCMS-2310 TXV HCMS-2310 TXVB	5.0 mm (0.20 in.) 5 x 7 Four Character Alphanumeric CMOS IC	Standard Red	• Military Equipment • Avionics • High Rel Industrial Equipment	
	HCMS-2311 HCMS-2311 TXV HCMS-2311 TXVB	12 Pin Ceramic 6.35 mm (0.25 in.) DIP with untinted glass lens	Yellow		
	HCMS-2312 HCMS-2312 TXV HCMS-2312 TXVB	Operating Temperature Range: -55°C to +100°C TXV – Hi Rel Screened	High Efficiency Red		
	HCMS-2313 HCMS-2313 TXV HCMS-2313 TXVB	TXVB – Hi Rel Screened to Level A MIL-D-87157	High Performance Green		
	HCMS-2314 HCMS-2314 TXV HCMS-2314 TXVB		Orange		
	HDSP-2351 HDSP-2351 TXV HDSP-2351 TXVB	4.87 mm (0.19 in.) 5 x 7 Four Character Alphanumeric Sunlight Viewable Display Operating Temperature Range: -55°C to +100°C	Yellow	• Military Avionics • Military Cockpit • Military Ground Support Systems	*
	HDSP-2352 HDSP-2352 TXV HDSP-2352 TXVB		High Efficiency Red		
	HDSP-2353 HDSP-2353 TXV HDSP-2353 TXVB		High Performance Green		

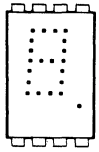
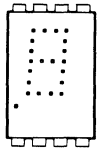
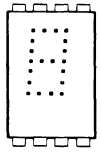
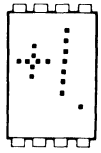
*Contact your local Sales Representative for information regarding this product. (See Section 9.)

Hermetic Alphanumeric Displays (Continued)

Device	P/N	Description	Color	Application	Page No.
	HDSP-2010 HDSP-2010 TXV HDSP-2010 TXVB	3.7 mm (0.15 in.) 5 x 7 Four Character Alphanumeric Operating Temperature Range: -40°C to +85°C TXV – Hi Rel Screened TXVB – Hi Rel Screened to Level A MIL-D-87157	Red, Red Glass Contrast Filter	• Extended temperature applications requiring high reliability • I/O Terminals • Avionics For further information see Application Note 1016.	*
	HDSP-2310 HDSP-2310 TXV HDSP-2310 TXVB	5.0 mm (0.20 in.) 5 x 7 Four Character Alphanumeric 12 Pin Ceramic 6.35 mm (0.25 in.) DIP with untinted glass lens Operating Temperature Range: -55°C to +85°C True Hermetic Seal TXV – Hi Rel Screened TXVB – Hi Rel Screened to Level A MIL-D-87157	Standard Red	• Military Equipment • Avionics • High Rel Industrial Equipment	*
	HDSP-2311 HDSP-2311 TXV HDSP-2311 TXVB		Yellow		
	HDSP-2312 HDSP-2312 TXV HDSP-2312 TXVB		High Efficiency Red		
	HDSP-2313 HDSP-2313 TXV HDSP-2313 TXVB		High Performance Green		
	HDSP-2450 HDSP-2450 TXV HDSP-2450 TXVB	6.9 mm (0.27 in.) 5 x 7 Four Character Alphanumeric 28 Pin Ceramic 15.24 mm (0.6 in.) DIP Operating Temperature Range: -55°C to +85°C True Hermetic Seal TXV – Hi Rel Screened TXVB – Hi Rel Screened to Level A MIL-D-87157	Red	• Military Equipment • High Reliability Applications • Avionics • Ground Support, Cockpit, Shipboard Systems	*
	HDSP-2451 HDSP-2451 TXV HDSP-2451 TXVB		Yellow		
	HDSP-2452 HDSP-2452 TXV HDSP-2452 TXVB		High Efficiency Red		
	HDSP-2453 HDSP-2453 TXV HDSP-2453 TXVB		High Performance Green		
	New HDSP-6650 New HDSP-6650 TXV New HDSP-6650 TSVB	5.0 mm (0.2 in.) 5 X 7 Four Character Dot Matrix Fully Intelligent Display Operating Temperature Range: -55°C to +85 °C	Orange	• Avionics • Military • High End • Industrial	4-217
	New HDSP-6651 New HDSP-6651 TXV New HDSP-6651 TXVB		Yellow		
	New HDSP-6652 New HDSP-6652 TXV New HDSP-6652 TXVB		High Efficiency Red		
	New HDSP-6653 New HDSP-6653 TXV New HDSP-6653 TXVB		Green		

* Contact your local HP Sales Representative for information regarding this product (See Section 9).

Hermetic Hexadecimal and Numeric Dot Matrix Displays

Device	P/N	Description	Package	Application	Page No.
 (A)  (B)  (C)  (D) 7.4 mm (0.29 in.) 4 x 7 Single Digit Package 8 Pin Glass Ceramic 15.2 mm (0.6 in.) DIP Truly Hermetic	4N51 4N51TXV JM87157/00101AAX[1] (4N51TXVB) (A)	Numeric RHDP Decoder/Driver/Memory TXV – Hi Rel Screened	8 Pin Hermetic Built-in 15.2 mm (0.6 in.) DIP with gold plated leads	• Military High Reliability Applications • Avionics/Space Flight Systems • Fire Control Systems • Ground Support, Shipboard Equipment	4-273
	4N52 4N52TXV JM87157/00102AAX[1] (4N52TXVB) (B)	Numeric LHDP Built-in Decoder/Driver/Memory TXV – Hi Rel Screened			
	4N54 4N54TXV JM87157/00104AAX[1] (4N54TXVB) (C)	Hexadecimal Built-in Decoder/Driver/Memory TXV – Hi Rel Screened			
	4N53 4N53TXV JM87157/00103AAX[1] (4N53TXVB) (D)	Character Plus/Minus Sign TXV – Hi Rel Screened			
	HDSP-0781 (A) HDSP-0781 TXV HDSP-0781 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157	High Efficiency Red Low Power	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	4-281
	HDSP-0782 (B) HDSP-0782 TXV HDSP-0782 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0783 (D) HDSP-0783 TXV HDSP-0783 TXVB	Overrange ±1 TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0784 (C) HDSP-0784 TXV HDSP-0784 TXVB	Hexadecimal, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			

[1]Military Approved and Qualified for High Reliability Applications.

Hermetic Hexadecimal and Numeric Dot Matrix Displays (Continued)

Device	P/N	Description	Package	Application	Page No.
7.4 mm (0.29 in.) 4 x 7 Single Digit Package 8 Pin Glass Ceramic 15.2 mm (0.6 in.) DIP Truly Hermetic	HDSP-0791 (A) HDSP-0791 TXV HDSP-0791 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157	High Efficiency Red High Brightness	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	4-281
	HDSP-0792 (B) HDSP-0792 TXV HDSP-0792 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0793 (D) HDSP-0793 TXV HDSP-0793 TXVB	Overrange ±1 TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0794 (C) HDSP-0794 TXV HDSP-0794 TXVB	Hexadecimal, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0881 (A) HDSP-0881 TXV HDSP-0881 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157	Yellow		
	HDSP-0882 (B) HDSP-0882 TXV HDSP-0882 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0883 (D) HDSP-0883 TXV HDSP-0883 TXVB	Overrange ±1 TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0884 (C) HDSP-0884 TXV HDSP-0884 TXVB	Hexadecimal, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			

Hermetic Hexadecimal and Numeric Dot Matrix Displays (cont.)

Device	P/N	Description	Package	Application	Page No.
7.4 mm (0.29 in.) 4 x 7 Single Digit Package 8 Pin Glass Ceramic 15.2 mm (0.6 in.) DIP Truly Hermetic	HDSP-0981 (A) HDSP-0981 TXV HDSP-0981 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157	High Performance Green	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	4-281
	HDSP-0982 (B) HDSP-0982 TXV HDSP-0982 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0983 (C) HDSP-0983 TXV HDSP-0983 TXVB	Overrange ±1 TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0984 (D) HDSP-0984 TXV HDSP-0984 TXVB	Hexadecimal, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			

HEWLETT PACKARD

New

Four Character 5 mm Hermetic 5x7 Alphanumeric Displays for Avionic Applications

Technical Data

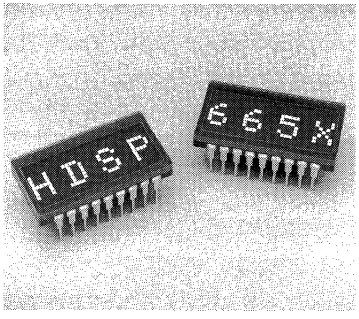
HDSP-665X/TXV/TXVB Series

Features

- **Readable in 8000 fc Daylight with Filter**
- **Wide 60° Viewing Angle**
- **Glass/Ceramic Hermetic Package**
- **Operating Temperature Range: -55°C to +85°C**
- **TXVB Version Conforms to MIL-D-87157, Quality Level A**
- **On-Board CMOS IC**
- **Data RAM, Decoder, LED Drive Circuitry**
- **128 ASCII Character Set**
- **Dimming and Blanking**

Description

These devices are hermetic, 5.0 mm (0.20 in.) high, four character, 5 x 7 dot matrix alphanumeric LED displays designed specifically for use in avionic systems, both commercial and military. These displays are also ideal for use in other non-avionic high reliability and military applications. When used with the proper contrast enhancement filter, these displays are readable in an 8000 fc daylight ambient. Each display has an on-board CMOS IC that decodes and stores 7 bit ASCII data and drives the LED matrix within each character. The IC may be interfaced to a microprocessor by connecting the inputs directly to the microprocessor address and data buses. Display blanking and eight levels of dimming are software controlled.



For military applications, TXV and TXVB screening per MIL-D-87157 is available. The HDSP-6651/6653/6650 displays are suitable for use in NVG lighting applications.

Device Selection Guide

Yellow	High Efficiency Red	High Performance Green	Orange
HDSP-6651	HDSP-6652	HDSP-6653	HDSP-6650
HDSP-6651TXV	HDSP-6652TXV	HDSP-6653TXV	HDSP-6650 TXV
HDSP-6651TXVB	HDSP-6652TXVB	HDSP-6653TXVB	HDSP-6650TXVB

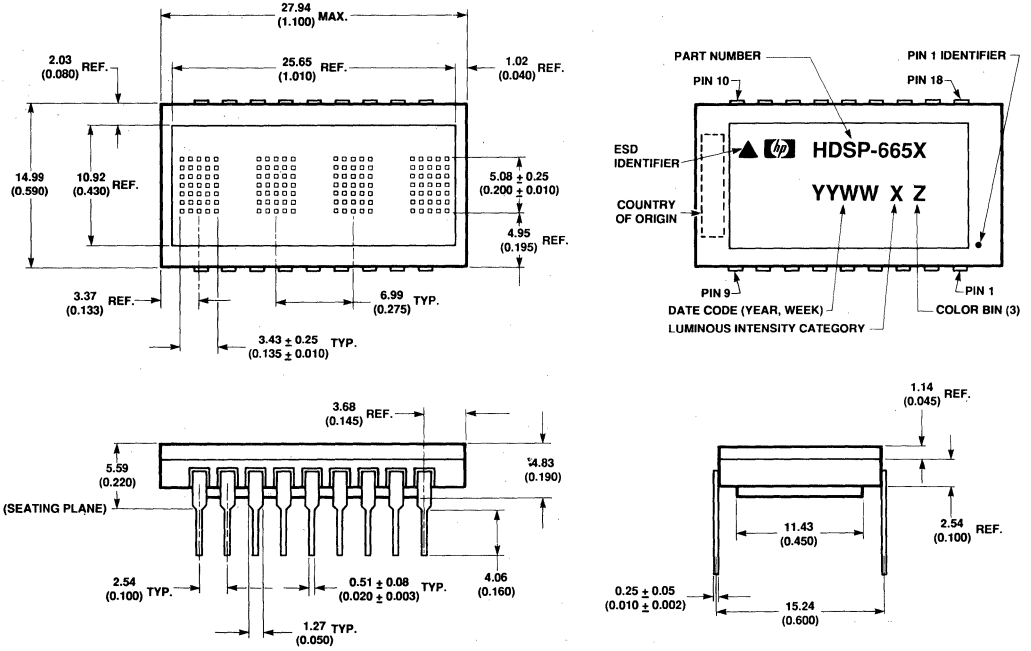
ESD WARNING: NORMAL CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED TO AVOID STATIC DISCHARGE.

Absolute Maximum Ratings

Supply Voltage, V_{DD} to Ground[1] ..... -0.5 V to 7.0 V
Input Voltage, Any Pin to Ground ..... -0.5 to V_{DD} +0.5 V
Free Air Operating Temperature Range, T_A ..... -55°C to +85°C
Storage Temperature Range, T_S ..... -55°C to +100°C
CMOS IC Junction Temperature, T_J(IC) ..... +150°C
ESD Protection, R = 1.5 kΩ, C = 100 pF ..... V_Z = 4 kV (each pin)
Maximum Solder Temperature
at Lead Seating Plane, t < 5 sec. ..... 260°C

Note:
1. Maximum voltage is with no LEDs illuminated.

Package Dimensions



HDSP-665X/TXV/TXVB

Notes:
1. All dimensions are in mm (inches).
2. Unless otherwise specified, tolerance on dimensions is ±0.38 mm (±0.015 in.).
3. For yellow and green devices only.
4. Leads are Alloy 42, solder dipped.

Pin No.	Function	Pin No.	Function
1	$\overline{CE}_1$ Chip Enable	10	GND
2	$\overline{CE}_2$ Chip Enable	11	D_0 Data Input
3	$\overline{CLR}$ Clear	12	D_1 Data Input
4	CUE Cursor Enable	13	D_2 Data Input
5	$\overline{CU}$ Cursor Select	14	D_3 Data Input
6	$\overline{WR}$ Write	15	D_6 Data Input
7	A_1 Address Input	16	D_5 Data Input
8	A_0 Address Input	17	D_4 Data Input
9	V_{DD}	18	$\overline{BL}$ Display Blank

Character Set

ASCII CODE																		
			D0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
			D1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			D2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			D3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
D6	D5	D4	Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	0																
0	0	1	1																
0	1	0	2																
0	1	1	3																
1	0	0	4																
1	0	1	5																
1	1	0	6																
1	1	1	7																

Notes:
1. High = 1 level.
2. Low = 0 level.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

Electrical Characteristics over Operating Temperature Range

4.5 < V_{DD} < 5.5 V (unless otherwise specified)

All Devices

Parameter	Symbol	Min.	25°C[1] Typ.	25°C[1] Max.	Max.	Units	Test Conditions
I_{DD} Blank	I_{DD} (blnk)		1.0		4.0	mA	All Digits Blanked
Input Current	I_I	-40			10	µA	V_{IN} = 0 V to V_{DD} V_{DD} = 5.0 V
Input Voltage High	V_{IH}	2.0			V_{DD}	V	
Input Voltage Low	V_{IL}	GND			0.8	V	
I_{DD} 4 digits 20 dots/character[2,3]	I_{DD} (#)		110	130	160	mA	"#" ON in all four locations
I_{DD} Cursor all dots ON @ 50%	I_{DD} (CU)		92	110	135	mA	Cursor ON in all four locations
Thermal Resistance IC Junction to Pin	$R\theta_{J\text{-}PIN}$		11			°C/W	IC Junction to GND Pin 10.

Notes:

1. V_{DD} = 5.0 V.
2. Average I_{DD} measured at full brightness. Peak I_{DD} = 28/15 x Average I_{DD}(#).
3. I_{DD}(#) max. = 130 mA at full brightness, 150°C IC junction temperature and V_{DD} = 5.5 V.

Optical Characteristics at 25°C[1]

V_{DD} = 5.0 V at Full Brightness

HDSP-6651 Yellow

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	3.9	5.0	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		583	nm	
Dominant Wavelength[2]	λ_d		585	nm	

HDSP-6652 High Efficiency Red

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	3.9	5.0	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		635	nm	
Dominant Wavelength[2]	λ_d		626	nm	

HDSP-6653 Green

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	5.55	7.40	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		568	nm	
Dominant Wavelength[2]	λ_d		572	nm	

HDSP-6650 Orange

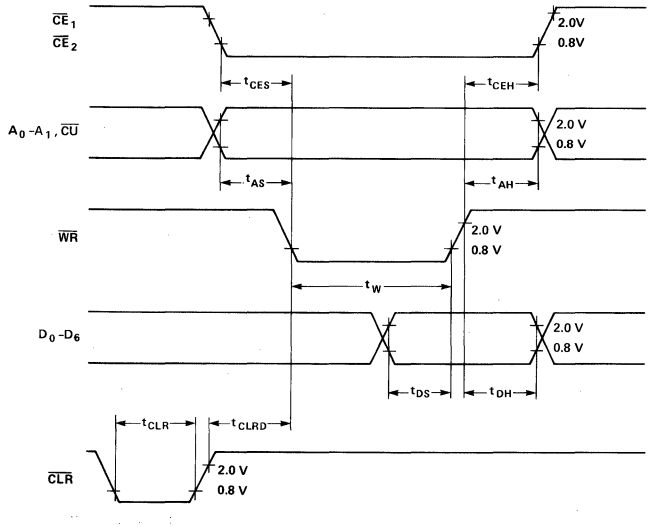
Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	3.9	5.0	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		600	nm	
Dominant Wavelength[2]	λ_d		602	nm	

Notes:
1. Refers to the initial case temperature of the device immediately prior to the light measurement.
2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.

AC Timing Characteristics over Operating Temperature Range at V_{DD} = 4.5 V

Parameter	Symbol	Min.	Units
Address Setup	t_{AS}	10	ns
Address Hold	t_{AH}	40	ns
Data Setup	t_{DS}	50	ns
Data Hold	t_{DH}	40	ns
Chip Enable Setup	t_{CES}	0	ns
Chip Enable Hold	t_{CEH}	0	ns
Write Time	t_{W}	75	ns
Clear	t_{CLR}	10	µs
Clear Disable	t_{CLRD}	1	µs

Timing Diagram



Electrical Description

Pin Function	Description
Chip Enable ($\overline{CE_1}$ and $\overline{CE_2}$, pins 1 and 2)	$\overline{CE_1}$ and $\overline{CE_2}$ must be a logic 0 to write to the display.
Clear ($\overline{CLR}$, pin 3)	When $\overline{CLR}$ is a logic 0 the ASCII RAM is reset to 20hex (space) and the Control Register/ Attribute RAM is reset to 00hex.
Cursor Enable (CUE pin 4)	CUE determines whether the IC displays the ASCII or the Cursor memory. (1 = Cursor, 0 = ASCII).
Cursor Select ($\overline{CU}$, pin 5)	$\overline{CU}$ determines whether data is stored in the ASCII RAM or the Attribute RAM/Control Register. (1 = ASCII, 0 = Attribute RAM/Control Register).
Write ($\overline{WR}$, pin 6)	$\overline{WR}$ must be a logic 0 to store data in the display.
Address Inputs (A_1 and A_0, pins 8 and 7)	A_0-A_1 selects a specific location in the display memory. Address 00 accesses the far right display location. Address 11 accesses the far left location.
Data Inputs (D_0-D_6, pins 11-17)	D_0-D_6 are used to specify the input data for the display.
V_{DD} (pin 9)	V_{DD} is the positive power supply input.
GND (pin 10)	GND is the display ground.
Blanking Input ($\overline{BL}$, pin 18)	$\overline{BL}$ is used to flash the display, blank the display or to dim the display.

Display Internal Block Diagram

Figure 1 shows the HDSP-665X display internal block diagram. The CMOS IC consists of a 4 x 7 Character RAM, a 2 x 4 Attribute RAM, a 5 bit Control Register, a 128 character ASCII decoder and the refresh circuitry necessary to synchronize the decoding and driving of four 5 x 7 dot matrix characters.

Four 7 bit ASCII words are stored in the Character RAM. The IC reads the ASCII data and decodes it via the 128 character ASCII decoder.

A 5 bit word is stored in the Control Register. Three fields within the Control Register provide an 8 level brightness control, master blank, and extended functions disable.

For each display digit location, two bits are stored in the Attribute RAM. One bit is used to enable a cursor character at each digit location. A second bit is used to individually disable the blanking features at each digit location.

The display is blanked and dimmed through an internal blanking input on the row drivers. Logic within the IC allows the user to dim the display either through the $\overline{BL}$ input or through the brightness control in the control register. Similarly, the display can be blanked through the $\overline{BL}$ input, the Master Blank in the Control Register, or the Digit Blank Disable in the Attribute RAM.

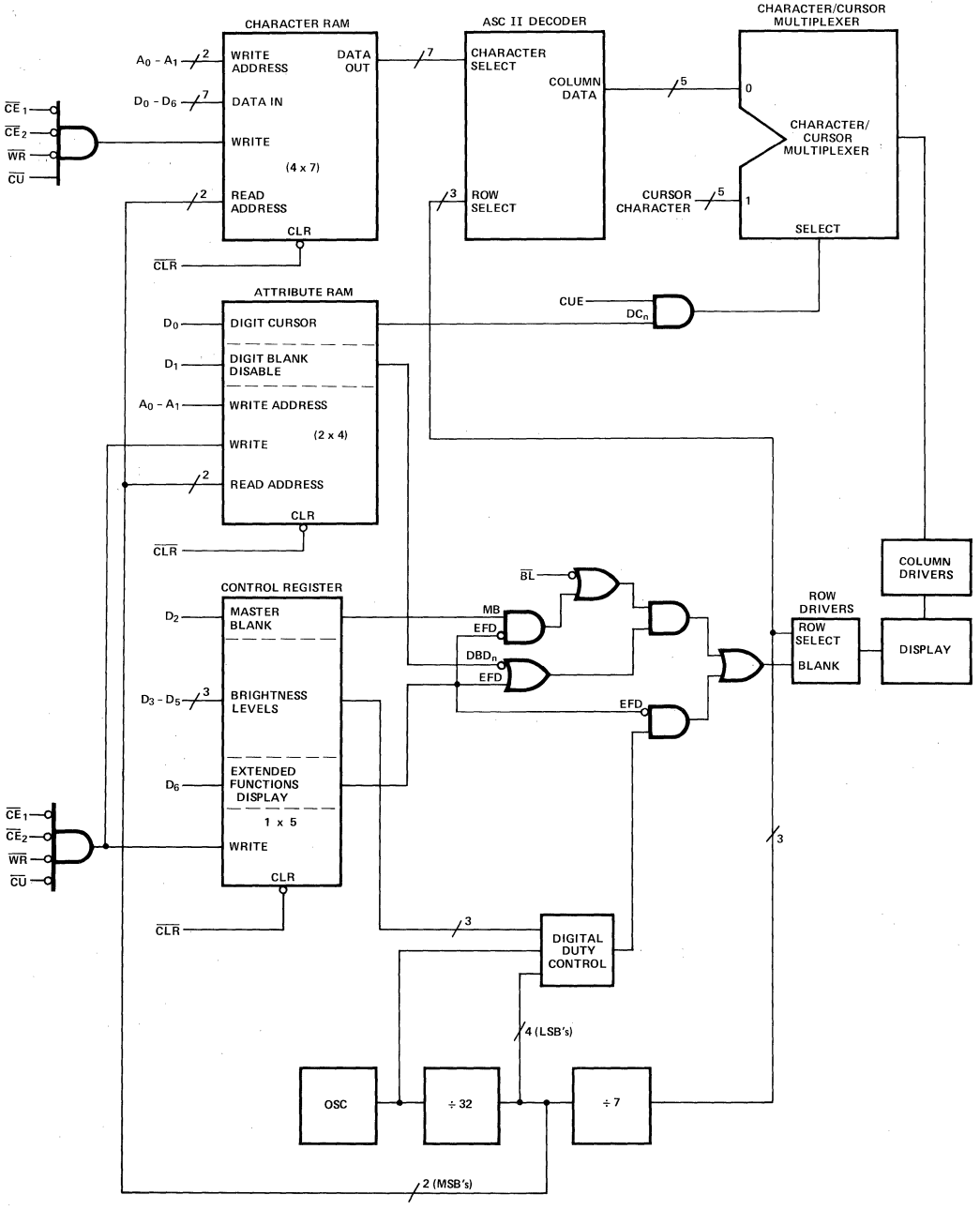


Figure 1. Internal Block Diagram

Display Clear

Data stored in the Character RAM, Control Register, and Attribute RAM will be cleared if the clear ($\overline{CLR}$) is held low for a minimum of 10 µs. Note that the display will be cleared regardless of the state of the chip enables ($\overline{CE_1}$, $\overline{CE_2}$). After the display is cleared, the ASCII code for a space (20hex) is loaded into all character RAM locations and 00hex is loaded into all Attribute RAM/Control Register memory locations.

Data Entry

Figure 2 shows the truth table for the HDSP-665X displays. Setting the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) to logic 0 and the cursor select ($\overline{CU}$) to logic 1 will enable ASCII data loading. When cursor select ($\overline{CU}$) is set to logic 0, data will be loaded into the Control Register and Attribute RAM. Address inputs A_0-A_1 are used to select the digit location in the display. Data inputs D_0-D_6 are used to load information into the display. Data will be latched into the display on the rising edge of the $\overline{WR}$ signal. D_0-D_6, A_0-A_1, $\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CU}$ must be held stable during the write cycle to ensure that correct data is stored into the display. Data can be loaded into the display in any order. Note that when A_0 and A_1 are logic 0, data is stored in the right most display location.

Cursor

When cursor enable (CUE) is a logic 1, a cursor will be displayed in all digit locations where a logic 1 has been stored in the Digit Cursor memory in the Attribute RAM. The cursor consists of all 35 dots ON at half brightness. A flashing cursor can be displayed by pulsing CUE. When CUE is a logic 0, the ASCII data stored in the Character RAM will be displayed regardless of the Digit Cursor bits.

Blanking

Blanking of the display is controlled through the $\overline{BL}$ input, the Control Register and Attribute RAM. The user can achieve a variety of functions by using these controls in different combinations, such as full hardware display blank, software blank, blanking of individ-

CUE	$\overline{BL}$	$\overline{CLR}$	$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WR}$	$\overline{CU}$	A_1	A_0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Function
0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	Display ASCII
1	1	1														Display Stored Cursor
X	X	0														Reset RAMs
X	0	1														Blank Display but do not reset RAMS and Control Register
X	X	1	0	0	0	0	0	0	Extended Functions Disable	Intensity Control			Master Blank	Digit Blank Disable 0	Digit Cursor 0	Write to Attribute RAM and Control Register
						0	0	1	0 = Enable D_1-D_5	000 = 100% 001 = 60% 010 = 40% 011 = 27% 100 = 17% 101 = 10% 110 = 7% 111 = 3%			0 = Display ON	Digit Blank Disable 1	Digit Cursor 1	DBD_n = 0, Allows Digit n to be blanked
						0	1	0	1 = Disable D_1-D_5				1 = Display Blanked	Digit Blank Disable 2	Digit Cursor 2	DBD_n = 1 Prevents Digit n from being blanked. DC_n = 0 Removes cursor from Digit n
						0	1	1	D_0 Always Enabled					Digit Blank Disable 3	Digit Cursor 3	DC_n = 1 Stores cursor at Digit n
X	X	1	0	0	0	1	0	0	Digit 0 ASCII Data (Right Most Character)							Write to Character RAM
						1	0	1	Digit 1 ASCII Data							
						1	1	0	Digit 2 ASCII Data							
						1	1	1	Digit 3 ASCII Data (Left Most Character)							
X	X	1	1	X	X	X	X	X	X	X	X	X	X	X	X	No Change
			X	1	X											
			X	X	1											

0 = Logic 0; 1 = Logic 1; X = Do Not Care.

Figure 2. Display Truth Table

ual characters, and synchronized flashing of individual characters or entire display (by strobing the blank input). All of these blanking modes affect only the output drivers, maintaining the contents and write capability of the internal RAMs and Control Register, so that normal loading of RAMs and Control Register can take place even with the display blanked.

Figure 3 shows how the Extended Function Disable (bit D_6 of the Control Register), Master Blank (bit D_2 of the Control Register), Digit Blank Disable (bit D_1 of the Attribute RAM), and $\overline{BL}$ input can be used to blank the display.

When the Extended Function Disable is a logic 1, the display can be blanked only with the $\overline{BL}$ input. When the Extended Function Disable is a logic 0, the display can be blanked through the $\overline{BL}$ input, the Master Blank, and the Digit Blank Disable. The entire display will be blanked if either the $\overline{BL}$ input is logic 0 or the Master Blank is logic 1, providing all Digit Blank Disable bits are logic 0. Those digits with Digit Blank Disable bits a logic 1 will ignore both blank signals

EFD	MB	DBD_n	$\overline{BL}$	
0	0	0	0	Display Blanked by $\overline{BL}$
0	0	X	1	Display ON
0	X	1	0	Display Blanked by $\overline{BL}$. Individual characters "ON" based on "1" being stored in DBD_n
0	1	0	X	Display Blanked by MB
0	1	1	1	Display Blanked by MB. Individual characters "ON" based on "1" being stored in DBD_n
1	X	X	0	Display Blanked by $\overline{BL}$
1	X	X	1	Display ON

Figure 3. Display Blanking Truth Table

and remain ON. The Digit Blank Disable bits allow individual characters to be blanked or flashed in synchronization with the $\overline{BL}$ input.

Dimming

Dimming of the display is controlled through either the $\overline{BL}$ input or the Control Register. A pulse width modulated signal can be applied to the $\overline{BL}$ input to dim the display. A three bit word in the Control Register generates an internal pulse width modulated signal to dim the display. The internal dimming feature is enabled only if the Extended Function Disable is a logic 0.

Bits 3-5 in the Control Register provide internal brightness control. These bits are interpreted as a three bit binary code, with code (000) corresponding to the maximum brightness and code (111) to the minimum brightness. In addition to varying the display brightness, bits 3-5 also vary the average value of I_{DD}. I_{DD} can be specified at any brightness level as shown in Table 1:

Table 1. Current Requirements at Different Brightness Levels

Symbol	D_5	D_4	D_3	Brightness	25°C Typ.	25°C Max.	Max. over Temp.	Units
I_{DD}(#)	0	0	0	100%	110	130	160	mA
	0	0	1	60%	66	79	98	mA
	0	1	0	40%	45	53	66	mA
	0	1	1	27%	30	37	46	mA
	1	0	0	17%	20	24	31	mA
	1	0	1	10%	12	15	20	mA
	1	1	0	7%	9	11	15	mA
	1	1	1	3%	4	6	9	mA

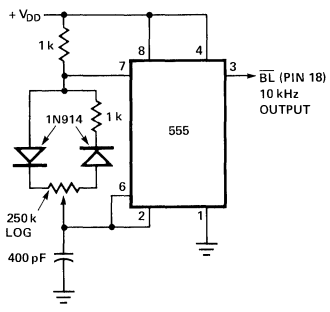


Figure 4. Intensity Modulation Control Using an Astable Multivibrator (reprinted with permission from *Electronics* magazine, Sept. 19, 1974, VNU Business pub. Inc.)

Figure 4 shows a circuit designed to dim the display from 98% to 2% by pulse width modulating the $\overline{BL}$ input. A logarithmic or a linear potentiometer may be used to adjust the display intensity. However, a logarithmic potentiometer matches the response of the human eye and therefore provides better resolution at low intensities. The circuit frequency should be designed to operate at 10 kHz or higher. Lower frequencies may cause the display to flicker.

Mechanical and Electrical Considerations

These HDSP-665X series displays are 18 pin DIP class ceramic packages designed to meet the rugged reliability requirements of modern day avionic systems. These displays may be stacked horizontally to form a character string of desired length. These displays are assembled by die attaching and wire bonding 140 LED dice and one CMOS IC to a ceramic substrate. A clear glass window is placed over the LEDs and sealed to form a hermetic air gap cavity. A similar window on the backside of the package forms a hermetic air gap cavity over the CMOS IC. Both windows permit post cap internal visual inspection of the LED dice and CMOS IC.

The inputs to the CMOS IC have protection against electrostatic discharge and input current latchup. However, for best results standard CMOS handling practice and precautions should be used. Prior to use, the HDSP-665X displays should be stored in antistatic or electrically conductive containers.

Input current latchup is caused when the CMOS inputs are subjected to either a voltage below ground (V_{in} < ground), a higher voltage than V_{DD} ($V_{in} > V_{DD}$), and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected to either ground or V_{DD}. Do not apply voltages to inputs until V_{DD} has been applied to the display. V_{DD} must be applied to the display prior to applying voltages to inputs in order to prevent latchup. Transient voltages should be eliminated from V_{DD} and data lines. A 0.1 µF capacitor placed between pin 9 (V_{DD}) and pin 10 (GND) at each display will help eliminate extraneous noise from affecting the ICs. The impedance of the ground return line from pin 10 of each display to the power supply should be as close to zero as possible at a frequency of 200 Hz.

ESD Susceptibility

These displays have an ESD susceptibility rating of CLASS 3 per MIL-HDBK-263A and CLASS 3 per MIL-STD-883C.

Contrast Enhancement Filter Vendors

Glass, passband, circular polarized, antireflection coated, daylight viewing contrast enhancement filters are available from:

HOYA Optics
3400 Edison Way
Fremont, CA 94538
(510) 490-1880

Marks Polarized Corp.
275-D Marcus Blvd.
Hauppauge, NY 11788
(516) 273-1190

Plastic contrast enhancement filters are available from:

Homalite
11 Brookside Drive
Wilmington, DE 19804
(302) 652-3686

Panelgraphic Corp.
10 Henderson Drive
West Caldwell, NJ 07006
(201) 227-1500

Soldering and Post Solder Cleaning

For information on soldering and post solder cleaning, see Application Note 1027 *Soldering LED Components*. These displays are fully compatible with semi-aqueous cleaning processes that use the terpene solvent BIOACT EC-7R.

Night Vision Lighting

With the use of NVG/DV filters, the HDSP-6651/6653/6650 displays may be designed into NVG lighting applications. For further information, refer to Application Note 1030 *LED Displays and Indicators and Night Vision Imaging System Lighting*.

High Reliability Testing

Two standard high reliability testing programs are available. The TXVB program is in conformance with MIL-D-87157 level A Test Tables. The TXVB product is tested to Tables I, II, IIIa, and IVa. The TXV program is an HP modification to the full conformance program and offers the 100% screening of Quality Level A, Table I, and Group A, Table II.

100% Screening

Table I. Quality Level A of MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	2072	Interpreted by HP Procedure 5956-7235-52
2. High Temperature Storage	1032	T_A = 100°C, Time = 24 hours
3. Temperature Cycling	1051	Condition A, T_{HIGH} = +100°C, 10 cycles, 15 min. dwell
4. Constant Acceleration	2006	5,000 Gs at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K
7. Interim Electrical/Optical Tests[2]	–	I_{CC}, I_V @ V_{CC} = 5.0 V, T_A = 25°C
8. Burn-In[1]	1015	Condition B at V_{CC} = 5.5 V, T_A = 85°C, t = 160 hours
9. Final Electrical Test[2]	–	I_{CC}, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$) I_{IL}, I_V @ V_{CC} = 5.0 V, T_A = 25°C
10. Delta Determinations	–	ΔI_{CC} = ±10%, ΔI_V = -20%, T_A = 25°C
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method Applies.
2. Limits and conditions are per the electrical optical characteristics.

Table II. Group A Electrical Tests – MIL-D-87157

Subgroup/Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_{CC}, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V and visual function @ V_{CC} = 5.0 V	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = 85°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = -55°C	7
Subgroup 4, 5, and 6 not applicable		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

Notes:
1. Limits and conditions are per the electrical/optical characteristics.

Table IIIa. Group B, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Design Verification[1]	2075[6]		1 Device/ 0 Failures
Subgroup 2[2,3] Solderability	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	Condition A, T_{HIGH} = +100°C, 15 min. dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Electrical/Optical Endpoints[5]	–	I_{CC}, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V @ V_{CC} = 5.0 V and visual function. T_A = 25°C	
Subgroup 4 Operating Life Test (340 hrs.)	1027	T_A = 85°C @ V_{CC} = 5.5 V	LTPD = 10
Electrical/Optical Endpoints[5]	–	Same as Subgroup 3	
Subgroup 5 Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = 100°C	LTPD = 10
Electrical/Optical Endpoints[5]	–	Same as Subgroup 3	

Notes:
1. Visual inspection is performed through the display window.
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend for one cycle.
5. Limits and conditions are per the electrical/optical characteristics.
6. Equivalent to MIL-STD-883, Method 2014.

Table IVa. Group C, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2] Lead Integrity[7,9]	2004	Condition B2	LTPD = 15
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Subgroup 3 Shock	2016	1500G. Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	5,000 Gs at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	–	I_{CC}, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V @ V_{CC} = 5.0 V and visual function. T_A = 25°C	
Subgroup 4[1,3] Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5 Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6 Operating Life Test[6]	1026	T_A = 85°C @ V_{CC} = 5.5 V	λ = 10
Electrical/Optical Endpoints[8]	–	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.
9. Initial conditioning is a 15° inward bend for one cycle.

HEWLETT PACKARD

Eight Character 5.0 mm (0.2 inch) Hermetic Smart 5 X 7 Alphanumeric Displays For Military Applications

Technical Data

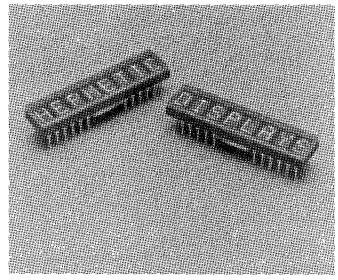
HDSP-2131/2131TXV/ 2131TXVB
HDSP-2132/2132TXV/ 2132TXVB
HDSP-2133/2133TXV/ 2133TXVB
HDSP-2179/2179TXV/ 2179TXVB

Features

- **Wide Operating Temperature Range -55°C to +85°C**
- **True Hermetic Package for Yellow, Orange and High Efficiency Red Displays[1]**
- **TXVB Version Conforms to MIL-D-87157 Quality Level A Test Tables**
- **Smart Alphanumeric Display**
  On-Board CMOS IC
  Built-In RAM
  ASCII Decoder
  LED Drive Circuitry
- **128 ASCII Character Set**
- **16 User Definable Characters**
- **Programmable Features**
  Individual Flashing Character
  Full Display Blinking
  Multi-Level Dimming and Blanking
  Self Test
  Clear Function
- **Read/Write Capability**
- **Full TTL Compatibility**
- **HDSP-2131/-2133/-2179 Useable in Night Vision Lighting Applications**
- **Categorized for Luminous Intensity**
- **HDSP-2131/2133 Categorized for Color**
- **Excellent ESD Protection**
- **Wave Solderable**
- **X-Y Stackable**

Description

The HDSP-2131 (yellow), HDSP-2179 (orange), HDSP-2132 (high efficiency red) and the HDSP-2133 (green) are eight-digit, 5 x 7 dot matrix, alphanumeric displays. The 5.0 mm (0.2 inch) high characters are packaged in a standard 7.64 mm (0.30 inch) 32 pin DIP. The on-board CMOS IC has the ability to decode 128 ASCII characters, which are permanently stored in ROM. In addition, 16 programmable symbols may be stored in an on-board RAM. Seven brightness levels provide versatility in adjusting the display intensity and power consumption. The HDSP-213X is designed for standard microprocessor interface techniques. The display and special features are accessed through a bidirectional eight-bit data bus. These features make the HDSP-213X ideally suited for applications where an hermetic, low power alphanumeric display is required.

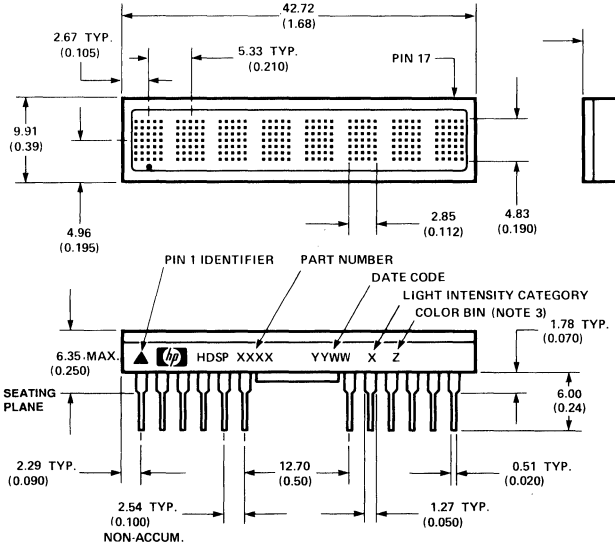


Devices

Yellow	High Efficiency Red	High Performance Green	Orange
HDSP-2131	HDSP-2132	HDSP-2133	HDSP-2179
HDSP-2131TXV	HDSP-2132TXV	HDSP-2133TXV	HDSP-2179TXV
HDSP-2131TXVB	HDSP-2132TXVB	HDSP-2133TXVB	HDSP-2179TXVB

Note: 1. The HDSP-2133 high peformance green displays conform to MIL-D-87157 hermeticity requirements.

Package Dimensions



HDSP-213X/2179/TXV/TXVB

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	CLS	17	GND (SUPPLY)
2	CLK	18	GND (LOGIC)
3	$\overline{WR}$	19	D4
4	$\overline{CE}$	20	D5
5	$\overline{RST}$	21	D6
6	$\overline{RD}$	22	D7
7	NO PIN	23	NO PIN
8	NO PIN	24	NO PIN
9	NO PIN	25	NO PIN
10	NO PIN	26	NO PIN
11	D0	27	$\overline{FL}$
12	D1	28	A0
13	D2	29	A1
14	D3	30	A2
15	NC	31	A3
16	V_{DD}	32	A4

Note:
1. All dimensions are in mm (inches).
2. Unless otherwise specified tolerance is ±0.30 mm (±0.015).
3. For green and yellow devices only.
4. Leads are copper alloy, solder dipped.

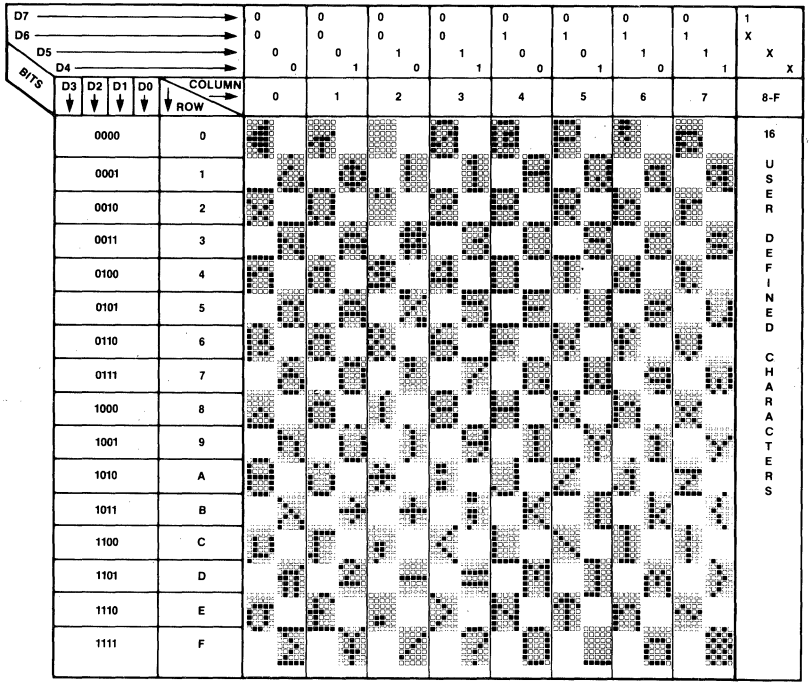
Absolute Maximum Ratings

Supply Voltage, V_{DD} to Ground[1] ..... -0.3 to 7.0 V
Operating Voltage, V_{DD} to Ground[2] ..... 5.5 V
Input Voltage, Any Pin to Ground ..... -0.3 to V_{DD} +0.3 V
Free Air Operating Temperature Range, T_A ..... -55°C to +85°C
Storage Temperature, T_S
HDSP-2131/-2132/-2179 ..... -65°C to +125°C
HDSP-2133 ..... -55°C to +100°C
CMOS IC Junction Temperature, T_J (IC) ..... +150°C
Maximum Solder Temperature
at Seating Plane, t < 5 sec ..... 260°C
ESD Protection @ 1.5 kΩ, 100 pF ..... V_Z = 4 kV (each pin)

Notes:
1. Maximum Voltage is with no LEDs illuminated.
2. 20 dots ON in all locations at full brightness.

ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED WITH THE HDSP-2131, HDSP-2132, HDSP-2133, AND HDSP-2179.

Character Set



Recommended Operating Conditions

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

Electrical Characteristics Over Operating Temperature Range

$4.5 < V_{DD} < 5.5$ V (unless otherwise specified)

Parameter	Symbol	Min.	25°C Typ.[1]	25°C Max.[1]	Max.[2]	Units	Test Conditions
Input Leakage (Input without pullup)	I_I	-10.0			+10.0	µA	V_{IN} = 0 to V_{DD}, pins CLK, D_0-D_7, A_0-A_4
Input Current (Input with pullup)	I_{IP}	-30.0	11	18	30	µA	V_{IN} = 0 to V_{DD}, pins RST, CLS, WR, RD, CE, FL
I_{DD} Blank	I_{DD} (BLK)		0.5	1.5	2.0	mA	$V_{IN} = V_{DD}$
I_{DD} 8 digits 12 dots/character[3]	I_{DD}(V)		200	255	330	mA	"V" on in all 8 locations
I_{DD} 8 digits 20 dots/character[3]	I_{DD}(#)		300	370	430	mA	"#" on in all 8 locations
Input Voltage High	V_{IH}	2.0			V_{DD} +0.3	V	V_{DD} = 5.5 V
Input Voltage Low	V_{IL}	GND -0.3 V			0.8	V	V_{DD} = 4.5 V
Output Voltage High	V_{OH}	2.4				V	V_{DD} = 4.5 V, I_{OH} = -40 µA
Output Voltage Low D_0-D_7	V_{OL}				0.4	V	V_{DD} = 4.5 V, I_{OL} = 1.6 mA
Output Voltage Low CLK					0.4	V	V_{DD} = 4.5 V, I_{OL} = 40 µA
Thermal Resistance IC Junction-to-PIN	$R\theta_{J\text{-}PIN}$		11			°C/W	

Notes:
1. V_{DD} = 5.0 V.
2. Maximum I_{DD} occurs at -55°C.
3. Average I_{DD} measured at full brightness. See Table 2 in Control Word Section for I_{DD} at lower brightness levels. Peak I_{DD} = 28/15 x Average I_{DD} (#).

Optical Characteristics at 25°C[4]

V_{DD} = 5.0 V at Full Brightness

High Efficiency Red HDSP-2132

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		635	nm
Dominant Wavelength	λ_d		626	nm

Orange HDSP-2179

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		600	nm
Dominant Wavelength	λ_d		602	nm

Yellow HDSP-2131

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		583	nm
Dominant Wavelength	λ_d		585	nm

High Performance Green HDSP-2133

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		568	nm
Dominant Wavelength	λ_d		574	nm

Note:
4. Refers to the initial case temperature of the device immediately prior to the light measurement.

AC Timing Characteristics Over Temperature Range

V_{DD} = 4.5 to 5.5 V unless otherwise specified.

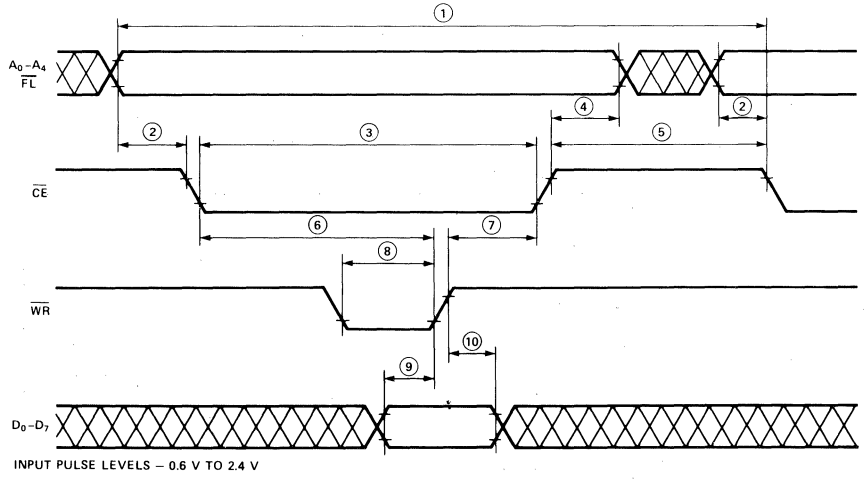
Reference Number	Symbol	Description	Min.[1]	Units
1	t_{ACC}	Display Access Time Write Read	 210 230	 ns
2	t_{ACS}	Address Setup Time to Chip Enable	10	ns
3	t_{CE}	Chip Enable Active Time[2, 3] Write Read	 140 160	 ns
4	t_{ACH}	Address Hold Time to Chip Enable	20	ns
5	t_{CER}	Chip Enable Recovery Time	60	ns
6	t_{CES}	Chip Enable Active Prior to Rising Edge of[1,2] Write Read	 140 160	 ns
7	t_{CEH}	Chip Enable Hold Time to Rising Edge of Read/Write Signal[2, 3]	0	ns
8	t_W	Write Active Time[2,3]	100	ns
9	t_{WD}	Data Valid Prior to Rising Edge of Write Signal	50	ns
10	t_{DH}	Data Write Hold Time	20	ns
11	t_R	Chip Enable Active Prior to Valid Data	160	ns
12	t_{RD}	Read Active Prior to Valid Data	75	ns
13	t_{DF}	Read Data Float Delay	10	ns
	t_{RC}	Reset Active Time[4]	300	ns

Notes:
1. Worst case values occur at an IC junction temperature of 150°C.
2. For designers who do not need to read from the display, the Read line can be tied to V_{DD} and the Write and Chip Enable lines can be tied together.
3. Changing the logic levels of the Address lines when $\overline{CE}$ = "0" may cause erroneous data to be entered into the Character RAM, regardless of the logic levels of the $\overline{WR}$ and $\overline{RD}$ lines.
4. The display must not be accessed until after 3 clock pulses (110 µs min. using the internal refresh clock) after the rising edge of the reset line.

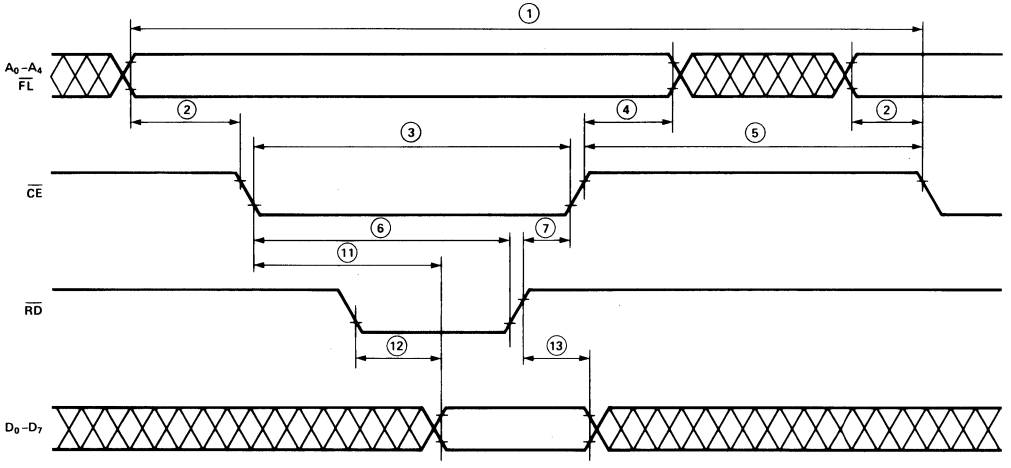
Symbol	Description	25°C Typical	Minimum[1]	Units
F_{OSC}	Oscillator Frequency	57	28	kHz
F_{RF}[5]	Display Refresh Rate	256	128	Hz
F_{FL}[6]	Character Flash Rate	2	1	Hz
t_{ST}[7]	Self Test Cycle Time	4.6	9.2	Sec

Notes:
5. $F_{RF} = F_{OSC}/224$
6. $F_{FL} = F_{OSC}/28{,}672$
7. $t_{ST} = 262{,}144/F_{OSC}$

Write Cycle Timing Diagram



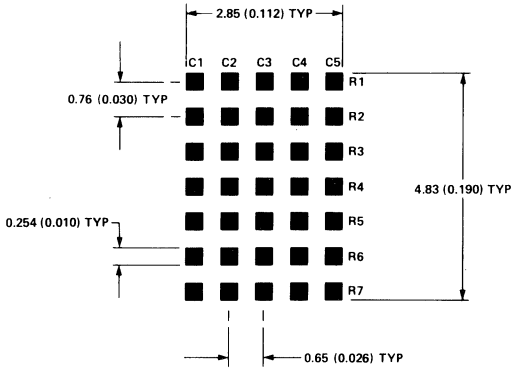
Read Cycle Timing Diagram



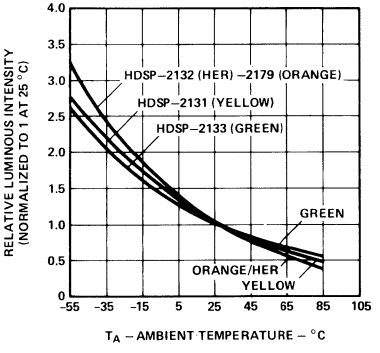
INPUT PULSE LEVELS: 0.6 V TO 2.4 V
OUTPUT REFERENCE LEVELS: 0.6 V TO 2.2 V
OUTPUT LOADING = 1 TTL LOAD AND 100pF

Character Font

(Not to Scale)



Relative Luminous Intensity vs. Temperature



Electrical Description

Pin Function

RESET ($\overline{RST}$, pin 5) — Reset initializes the display.

FLASH ($\overline{FL}$, pin 27) — $\overline{FL}$ low indicates an access to the Flash RAM and is unaffected by the state of address lines A_3-A_4.

ADDRESS INPUTS (A_0-A_4, pins 28-32) — Each location in memory has a distinct address. Address inputs (A_0-A_2) select a specific location in the Character RAM, the Flash RAM or a particular row in the UDC (User-Defined Character) RAM. A_3-A_4 are used to select which section of memory is accessed. Table 1 shows the logic levels needed to access each section of memory.

Table 1. Logic Levels to Access Memory

$\overline{FL}$	A_4	A_3	Section of Memory	A_2 A_1 A_0
0	X	X	Flash RAM	Character Address
1	0	0	UDC Address Register	Don't Care
1	0	1	UDC RAM	Row Address
1	1	0	Control Word Register	Don't Care
1	1	1	Character RAM	Character Address

CLOCK SELECT (CLS, pin 1) — This input is used to select either an internal or external clock source.

CLOCK INPUT/OUTPUT (CLK, pin 2) — Outputs the master clock (CLS = 1) or inputs a clock (CLS = 0) for slave displays.

WRITE ($\overline{WR}$, pin 3) — Data is written into the display when the $\overline{WR}$ input is low and the $\overline{CE}$ input is low.

CHIP ENABLE ($\overline{CE}$, pin 4) — This input must be at a logic low to read or write data to the display and must go high between each read and write cycle.

READ ($\overline{RD}$, pin 6) — Data is read from the display when the $\overline{RD}$ input is low and the $\overline{CE}$ input is low.

DATA Bus (D_0-D_7, pins 11-14, 19-22) — The Data bus is used to read from or write to the display.

$GND_{(SUPPLY)}$ (pin 17) — This is the analog ground for the LED drivers.

$GND_{(LOGIC)}$ (pin 18) — This is the digital ground for internal logic.

$V_{DD(POWER)}$ (pin 16) — This is the positive power supply input.

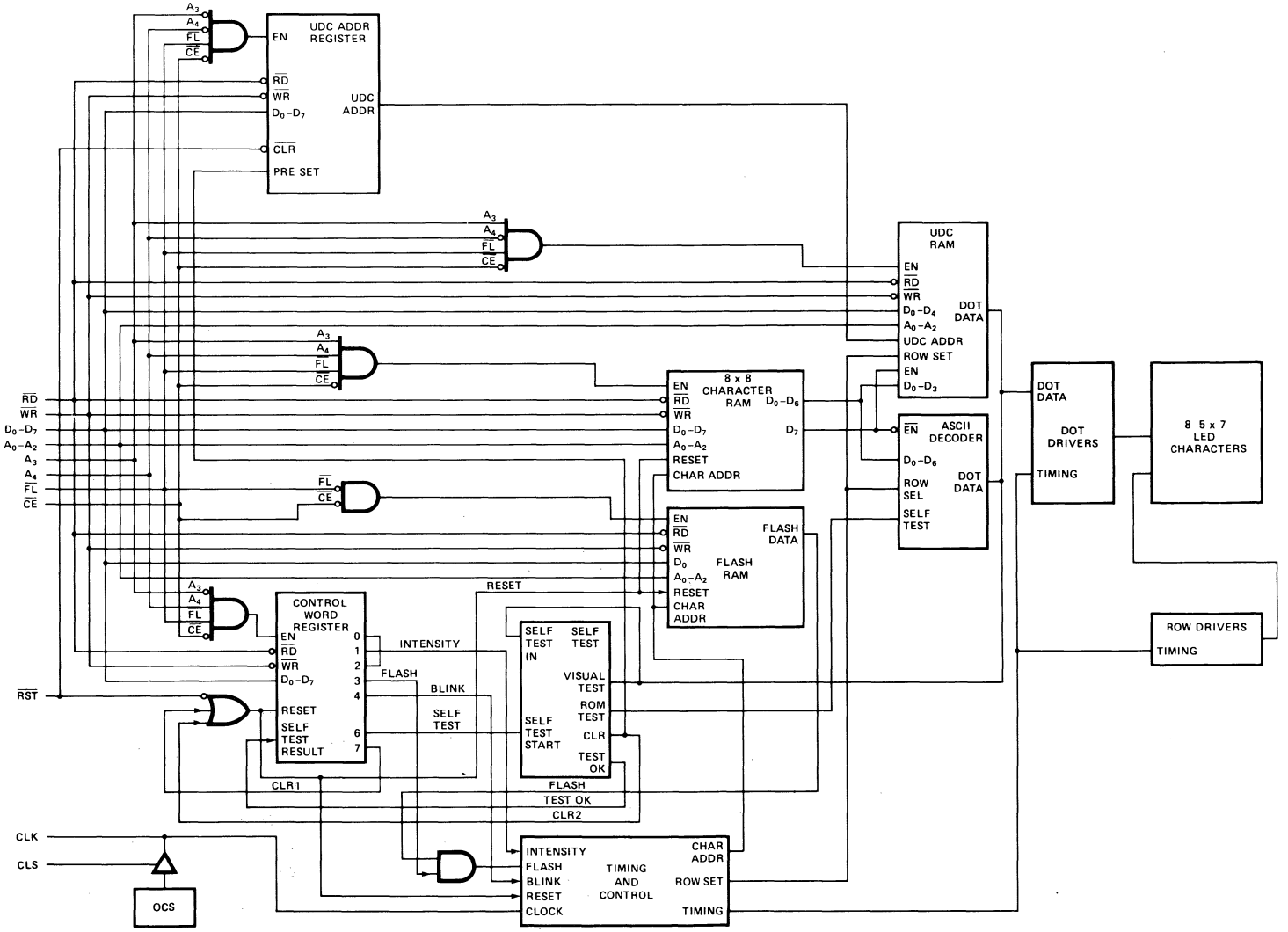


Figure 1. HDSP-213X Internal Block Diagram.

Display Internal Block Diagram

Figure 1 shows the internal block diagram of the HDSP-213X display. The CMOS IC consists of an 8 byte Character RAM, an 8 bit Flash RAM, a 128 character ASCII decoder, a 16 character UDC RAM, a UDC Address Register, a Control Word Register, and the refresh circuitry necessary to synchronize the decoding and driving of eight 5 x 7 dot matrix characters. The major user accessible portions of the display are listed below:

Character RAM	This RAM stores either ASCII character data or a UDC RAM address.
Flash RAM	This is a 1 x 8 RAM which stores Flash data.
User-Defined Character RAM (UDC RAM)	This RAM stores the dot pattern for custom characters.
User-defined Character Address Register (UDC Address Register)	This register is used to provide the address to the UDC RAM when the user is writing or reading a custom character.
Control Word Register	This register allows the user to adjust the display brightness, flash individual characters, blink, self test or clear the display.

Character Ram

Figure 2 shows the logic levels needed to access the HDSP-213X Character RAM. During a normal access the $\overline{CE}$ = "0" and either $\overline{RD}$ = "0" or $\overline{WR}$ = "0". However, erroneous data may be written into the Character RAM if the Address lines are unstable when $\overline{CE}$ = "0" regardless of the logic levels of the $\overline{RD}$ or $\overline{WR}$ lines. Address lines A_0-A_2 are used to select the location in the Character RAM. Two types of data can be stored in each Character RAM location: an ASCII code or a UDC RAM address. Data bit D_7 is used to differentiate between an ASCII character and a UDC RAM address. D_7 = 0 enables the ASCII decoder and D_7 = 1 enables the UDC RAM. D_0-D_6 are used to input ASCII data and D_0-D_3 are used to input a UDC address.

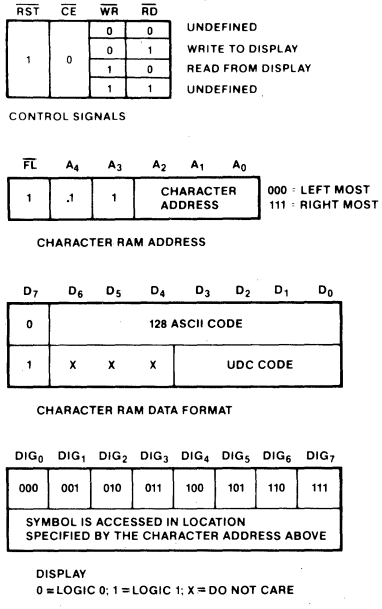


Figure 2. Logic Levels to Access the Character RAM.

UDC RAM and UDC Address Register

Figure 3 shows the logic levels needed to access the UDC RAM and the UDC Address Register. The UDC Address Register is eight bits wide. The lower four bits (D_0-D_3) are used to select one of the 16 UDC locations. The upper four bits (D_4-D_7) are not used. Once the UDC address has been stored in the UDC Address Register, the UDC RAM can be accessed.

To completely specify a 5 x 7 character requires eight write cycles. One cycle is used to store the UDC RAM address in the UDC Address Register. Seven cycles are used to store dot data in the UDC RAM. Data is entered by rows. One cycle is needed to access each row. Figure 4 shows the organization of a UDC character assuming the symbol to be stored is an "F". A_0-A_2 are used to select the row to be accessed and D_0-D_4 are used to transmit the row dot data. The upper three bits (D_5-D_7) are ignored. D_0 (least significant bit) corresponds to the right most column of the 5 x 7 matrix and D_4 (most significant bit) corresponds to the left most column of the 5 x 7 matrix.

Flash RAM

Figure 5 shows the logic levels needed to access the Flash RAM. The Flash RAM has one bit associated with each location of the Character RAM. The Flash input is used to select the Flash RAM. Address lines A_3-A_4 are ignored. Address lines A_0-A_2 are used to select the location in the Flash RAM to store the attribute. D_0 is used to store or remove the flash attribute. D_0 = "1" stores the attribute and D_0 = "0" removes the attribute.

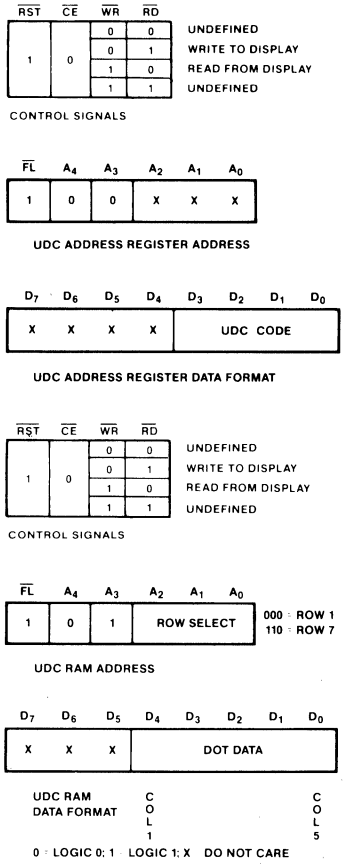


Figure 3. Logic Levels to Access a UDC Character.

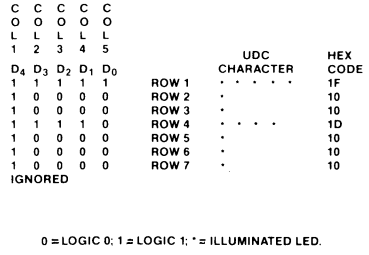


Figure 4. Data to Load "F" into the UDC RAM.

When the attribute is enabled through bit 3 of the Control Word and a "1" is stored in the Flash RAM, the corresponding character will flash at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock the flash rate can be calculated by dividing the clock frequency by 28,672.

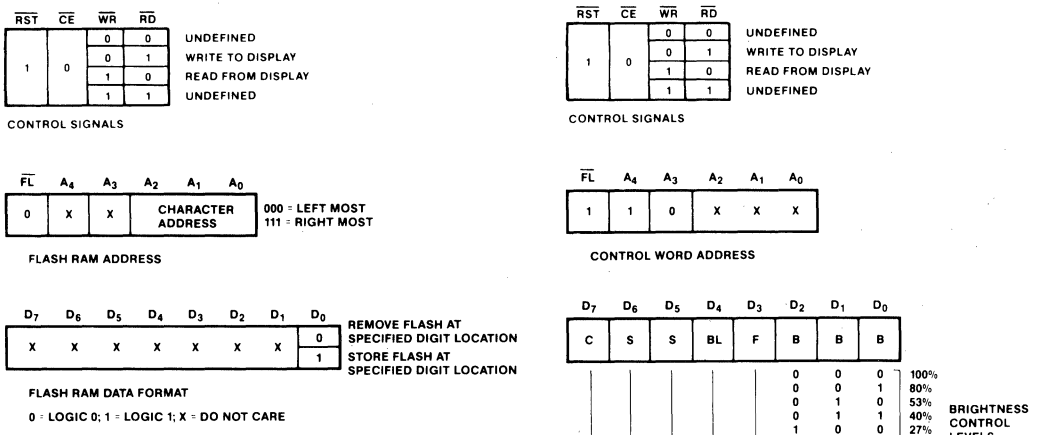


Figure 5. Logic Levels to Access the Flash RAM.

Figure 6. Logic Levels to Access the Control Word Register

Control Word Register

Figure 6 shows how to access the Control Word Register. This is an eight bit register which performs five functions. They are Brightness control, Flash RAM control, Blinking, Self Test and Clear. Each function is independent of the others. However, all bits are updated during each Control Word write cycle.

Brightness (Bits 0-2)

Bits 0-2 of the Control Word adjust the brightness of the display. Bits 0-2 are interpreted as a three bit binary code with code (000) corresponding to maximum brightness and code (111) corresponding to a blanked display. In addition to varying the display brightness, bits 0-2 also vary the average value of I_{DD}. I_{DD} can be calculated at any brightness level by multiplying the percent brightness level by the value of I_{DD} at the 100% brightness level. These values of I_{DD} are shown in Table 2.

Table 2. Current Requirements at Different Brightness Levels

Symbol	D_2	D_1	D_0	% Brightness	25°C Typical	Units
I_{DD} (V)	0	0	0	100	200	mA
	0	0	1	80	160	mA
	0	1	0	53	106	mA
	0	1	1	40	80	mA
	1	0	0	27	54	mA
	1	0	1	20	40	mA
	1	1	0	13	26	mA

Flash Function (Bit 3)

Bit 3 determines whether the flashing character attribute is on or off. When bit 3 is a "1", the output of the Flash RAM is checked. If the content of a location in the Flash RAM is a "1", the associated digit will flash at approximately 2 Hz. For an external clock, the blink rate can be calculated by driving the clock frequency by 28,672. If the flash enable bit of the Control Word is a "0", the content of the Flash RAM is ignored. To use this function with multiple display systems see the Reset section.

Blink Function (Bit 4)

Bit 4 of the Control Word is used to synchronize blinking of all eight digits of the display. When this bit is a "1" all eight digits of the display will blink at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock, the blink rate can be calculated by dividing the clock frequency by 28,672. This function will override the Flash function when it is active. To use this function with multiple display systems see the Reset section.

Self Test Function (Bits 5, 6)
Bit 6 of the Control Word Register is used to initiate the self test function. Results of the internal self test are stored in bit 5 of the Control Word. Bit 5 is a read only bit where bit 5 = "1" indicates a passed self test and bit 5 = "0" indicates a failed self test.

Setting bit 6 to a logic 1 will start the self test function. The built-in self test function of the IC consists of two internal routines which exercises major portions of the IC and illuminates all of the LEDs. The first routine cycles the ASCII decoder ROM through all states and performs a checksum on the output. If the checksum agrees with the correct value, bit 5 is set to "1". The second routine provides a visual test of the LEDs using the drive circuitry. This is accomplished by writing checkered and inverse checkered patterns to the display. Each pattern is displayed for approximately 2 seconds.

During the self test function the display must not be accessed. The time needed to execute the self test function is calculated by multiplying the clock period by 262,144. For example, assume a clock frequency of 58 KHz, then the time to execute the self test function frequency is equal to (262,144/58,000) = 4.5 second duration.

At the end of the self test function, the Character RAM is loaded with blanks, the Control Word Register is set to zeros except for bit 5, and the Flash RAM is cleared and the UDC Address Register is set to all ones.

Clear Function (Bit 7)
Bit 7 of the Control Word will clear the Character RAM and the Flash RAM. Setting bit 7 to a "1" will start the clear function. Three clock cycles (110 µs min. using the internal refresh clock) are required to complete the clear function. The display must not be accessed while the display is being cleared. When the clear function has been completed, bit 7 will be reset to a "0". The ASCII character code for a space (20H) will be loaded into the Character RAM to blank the display and the Flash RAM will be loaded with "0"s. The UDC RAM, UDC Address Register, and the remainder of the Control Word are unaffected.

Display Reset

Figure 7 shows the logic levels needed to Reset the display. The display should be Reset on Power-up. The external Reset clears the Character RAM, Flash RAM, Control Word and resets the internal counters. After the rising edge of the Reset signal, three clock cycles (110 µs min. using the internal refresh clock) are required to complete the reset sequence. The display must not be accessed while the display is being reset. The ASCII Character code for a space (20H) will be loaded into the Character RAM to blank the display. The Flash RAM and Control Word Register are loaded with all "0"s. The UDC RAM and UDC Address Register are unaffected. All displays which operate with the same clock source must be simultaneously reset to synchronize the Flashing and Blinking functions.

$\overline{RST}$	$\overline{CE}$	$\overline{WR}$	$\overline{RD}$	$\overline{FL}$	A_4-A_0	D_7-D_0
0	1	X	X	X	X	X

0 = LOGIC 0; 1 = LOGIC 1; X = DO NOT CARE

NOTE:
IF $\overline{RST}$, $\overline{CE}$ AND $\overline{WR}$ ARE LOW, UNKNOWN DATA MAY BE WRITTEN INTO THE DISPLAY.

Figure 7. Logic Levels to Reset the Display.

Mechanical and Electrical Considerations

The HDSP-213X is a 32 pin dual-in-line package with 24 external pins, which can be stacked horizontally and vertically to create arrays of any size. The HDSP-213X is designed to operate continuously from -55°C to +85°C with a maximum of 20 dots ON per character. Illuminating all thirty-five dots at full brightness is not recommended.

The HDSP-213X is assembled by die attaching and wire bonding 280 LED chips and a CMOS IC to a ceramic substrate. A glass window is placed over the ceramic substrate creating an air gap over the LED wire bonds. A second glass window creates an air gap over the CMOS IC. This package construction makes the display highly tolerant to temperature cycling and allows wave soldering and visual inspection of the IC.

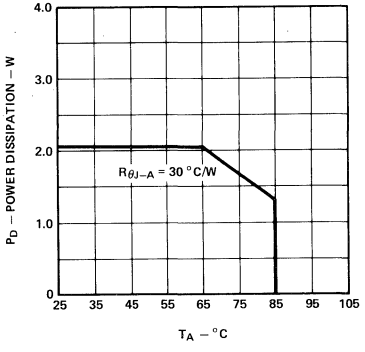


Figure 8. Maximum Power Dissipation vs. Ambient Temperature Derating Based on T_JMAX = 125°C.

The inputs to the CMOS IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HDSP-213X should be stored in antistatic packages or conductive material. During assembly, a grounded conductive work area should be used, and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static charge buildup. Input current latchup is caused when the CMOS inputs are subjected to either a voltage below ground (V_{IN} < ground) or to a voltage higher than V_{DD} ($V_{IN} > V_{DD}$) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{DD}. Voltages should not be applied to the inputs until V_{DD} has been applied to the display. Transient input voltages should be eliminated.

Thermal Considerations

The HDSP-213X has been designed to provide a low thermal resistance path from the CMOS IC to the 24 package pins. This heat is then typically conducted through the traces of the user's printed circuit board to free air. For most applications no additional heatsinking is required.

The maximum operating IC junction temperature is 150°C. The maximum IC junction temperature can be calculated using the following equation:

$$T_J(IC)\ MAX = T_A + (P_D MAX)\ (R\theta_{J\text{-}PIN} + R\theta_{PIN\text{-}A})$$

Where

$$P_D MAX = (V_{DD} MAX)\ (I_{DD} MAX)$$

I_{DD}MAX = 370 mA with 20 dots ON in eight character locations at 25°C ambient. This value is from the Electrical Characteristics table.

$$P_D MAX = (5.5\ V)(0.370\ A) = 2.04\ W$$

Ground Connections

Two ground pins are provided to keep the internal IC logic ground clean. The designer can, when necessary, route the analog ground for the LED drivers separately from the logic ground until an appropriate ground plane is available. On long interconnects between the display and the host system, the designer can keep voltage drops on the analog ground from affecting the display logic levels by isolating the two grounds.

The logic ground should be connected to the same ground potential as the logic interface circuitry. The analog ground and the logic ground should be connected at a common ground which can withstand the current introduced by the switching LED drivers. When separate ground connections are used, the analog ground can vary from -0.3 V to +0.3 V with respect to the logic ground. Voltage below -0.3 V can cause all dots to be on. Voltage above +0.3 V can cause dimming and dot mismatch.

ESD Susceptibility

These displays have ESD susceptibility ratings of CLASS 3 per DOD-STD-1686 and CLASS B per MIL-STD-883C.

Soldering and Post Solder Cleaning Instructions for the HDSP-213X

The HDSP-213X may be hand soldered or wave soldered with SN63 solder. When hand soldering it is recommended that an electronically temperature controlled and securely grounded soldering iron be used. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux can be used. The solder wave temperature should be set at 245°C ± 5°C (473°F ± 9°F), and dwell in the wave should be set between 1-1/2 to 3 seconds for optimum soldering. The preheat temperature should not exceed 105°C (221°F) as measured on the solder side of the PC board.

Post solder cleaning may be performed using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling temperature is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, Genesolv DES, and water.

An aqueous cleaning process may be used. A saponifier, such as Kester Bio-Kleen Formula 5799 or its equivalent, may be added to the wash cycle of an aqueous process to remove rosin flux residues. Organic acid flux residues must be thoroughly removed by an aqueous cleaning process to prevent corrosion of the leads and solder connections. The optimum water temper-

ature is 60°C (140°F). The maximum cumulative exposure of the HDSP-213X to wash and rinse cycles should not exceed 15 minutes. For additional information on soldering and post solder cleaning, see Application Note 1027.

High Reliability Testing

Two standard high reliability testing programs are available. The TXVB program is in conformance with MIL-D-87157 level A Test Tables. The TXVB product is tested to Tables I, II, IIIa and IVa. The TXV program is an HP modification to the full conformance program and offers the 100% screening of Quality Level A, Table I, and Group A, Table II.

Contrast Enhancement

When used with the proper contrast enhancement filters, the HCMS-213X series displays are readable daylight ambients. Refer to Application Note 1029 *Luminous Contrast and Sunlight Readability of the HDSP-238X Series Alphanumeric Displays for Military Applications* for information on contrast enhancement for daylight ambients. Refer to Application Note 1015 *Contrast Enhancement Techniques for LED Displays* for information on contrast enhancement in moderate ambients.

Night Vision Lighting

When used with the proper NVG/DV filters, the HDSP-2131, HDSP-2179 and HDSP-2133 may be used in night vision lighting applications. The HDSP-2131 (yellow), HDSP-2179 (orange) displays are used as master caution and warning indicators. The HDSP-2133 (high performance green) displays are used for general instrumentation. For a list of NVG/DV filters and a discussion on night vision lighting technology, refer to Application Note 1030 *LED Displays and Indicators and Night Vision Imaging System Lighting.* An external dimming circuit must be used to dim these displays to night vision lighting levels to meet NVIS radiance requirements. Refer to AN 1039 *Dimming HDSP-213X Displays to Meet Night Vision Lighting Levels.*

100% Screening
Table I. Quality Level A of MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	2072	Interpreted by HP Procedure 5956-7512-52
2. High Temperature Storage	1032	T_A = 125°C[3], Time = 24 hours
3. Temperature Cycling	1051	Condition B[4] , 10 cycles, 15 minute dwell
4. Constant Acceleration	2006	10,000 Gs at Y_1 & Y_2 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K[5]
7. Interim Electrical/ Optical Tests[2]	—	I_{DD}(BLK), I_{DD}(V), I_{DD}(#), I_{IH}, I_{IL}, I_{OH}, I_{OL}, I_V and Visual Function T_A = 25°C
8. Burn-In[1]	1015	Condition B at V_{DD} = 5.5 V, cycle through character set 1 per second, T_A = +85°C, Time = 160 hours
9. Final Electrical Test[2]	—	Same as step 7
10. Delta Determinations	—	I_{DD}(V) & I_{DD}(#) = ±10%, I_V = -20%
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics.
3. T_A = +100°C for HDSP-2133.
4. T_A = -55°C to +100°C for HDSP-2133.
5. Fluid temperature = +100°C for HDSP-2133.

Table II. Group A Electrical Tests – MIL-D-87157

Subgroup Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_{DD}(BLK), I_{DD}(V), I_{DD}(#), I_{IH}, I_{IL}, I_{OH}, I_{OL}, I_V, and function test	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1 except delete I_V and visual function. T_A = +85°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1 except delete I_V and visual function. T_A = -55°C	7
Subgroup 4, 5, and 6 not applicable		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

Notes:
1. Limits and conditions are per the electrical/optical characteristics.

Table IIIa. Group B Electrical Tests – MIL-D-87157

Subgroup Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices 0 Failures
Internal Visual and Design Verification[1]	2075[6]		1 Device 0 Failures
Subgroup 2[2,3] Solderability[7]	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock Temperature Cycle	1051	Condition B1, 15 minute dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K[8]	
Electrical/Optical Endpoints[5]	—	I_{DD}(BLK), I_{DD}(V), I_{DD}(#), I_{IH}, I_{IL}, I_{OH}, I_{OL}, I_V & function, T_A = 25°C	
Subgroup 4 Operating Life Test 340 hrs	1027	T_A = +85°C @ V_{DD} = 5.5 V	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	
Subgroup 5 Non-Operating Storage Life Test 340 hrs	1032	T_A = +125°C[9]	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	

Notes:
1. Visual inspection is performed through the display window.
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend for one cycle.
5. Limits and conditions as per the electrical/optical characteristics.
6. Equivalent to MIL-STD-883, Method 2014.
7. The steam aging is not performed on gold plated leads.
8. Fluid temperature = +100°C for HDSP-2133.
9. T_A = +100°C for HDSP-2133.

Table IVa. Group C, Class A and B of MIL-D-87157

Subgroup Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1[1] Physical Dimensions	2066		2 Devices 0 Failures
Subgroup 2[2] Lead Integrity[7,9]	2004	Condition B2	LTPD = 15
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K[10]	
Subgroup 3 Shock	2016	1500 G. Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1, Y_2 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_{DD}(BLK), I_{DD}(V), I_{DD}(#), I_{IH}, I_{IL}, I_{OH}, I_{OL}, I_V and Visual Function, T_A = 25°C	
Subgroup 4[1,3] Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5 Bond Strength[5]	2037	Condition A	LTPD = 20 C = 0
Subgroup 6 Operating Life Test[6]	1026	T_A = +85°C at V_{DD} = 5.5 V	λ = 10
Electrical/Optical Endpoints[6]	—	Same as Subgroup 3	

Notes:

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.
9. Initial conditioning is a 15° inward bend for three cycles.
10. Fluid temperature = +100°C for HDSP-2133.

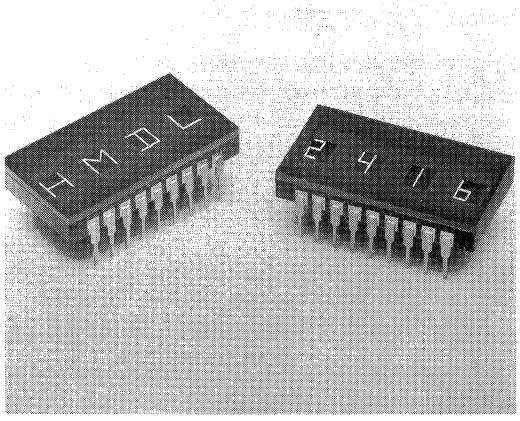
HEWLETT PACKARD

FOUR CHARACTER 3.8mm (0.15 inch) HERMETIC, SMART ALPHANUMERIC DISPLAY

HMDL-2416
HMDL-2416TXV
HMDL-2416TXVB

Features

- **WIDE OPERATING TEMPERATURE RANGE -55° C to +100° C**
- **TRUE HERMETIC PACKAGE**
- **TXVB VERSION CONFORMS TO MIL-D-87157 QUALITY LEVEL A TEST TABLES**
- **CMOS IC FOR LOW POWER CONSUMPTION**
- **SMART ALPHANUMERIC DISPLAY Built-in RAM, ASCII Decoder, and LED Drive Circuitry**
- **VERY FAST ACCESS TIME, 160 ns**
- **EXCELLENT ESD PROTECTION Built-in Protective Diodes**
- **FULL TTL COMPATIBILITY OVER OPERATING TEMPERATURE RANGE**
- **END-STACKABLE**
- **WIDE VIEWING ANGLE**
- **WAVE SOLDERABLE**



Description

The HMDL-2416 is a smart 3.8 mm (0.15") four character, sixteen segment red GaAsP display. It is contained in a hermetic 18 pin dual-in-line, glass sealed ceramic package. The on-board CMOS IC contains memory, ASCII decoder, multiplexing circuitry, and drivers. It has a wide operating temperature range, and is fully TTL compatible, wave solderable, and highly reliable. This display is ideally suited for military and high reliability industrial applications where a rugged, reliable, easy-to-use alphanumeric display is required.

Typical Applications

- **MILITARY EQUIPMENT**
- **AVIONICS**
- **HIGH RELIABILITY INDUSTRIAL EQUIPMENT**

Absolute Maximum Ratings

Supply Voltage, V_{CC} to Ground ..... -0.5 V to 7.0 V

Input Voltage,
Any Pin to Ground ..... -0.5 V to V_{CC} + .5 V

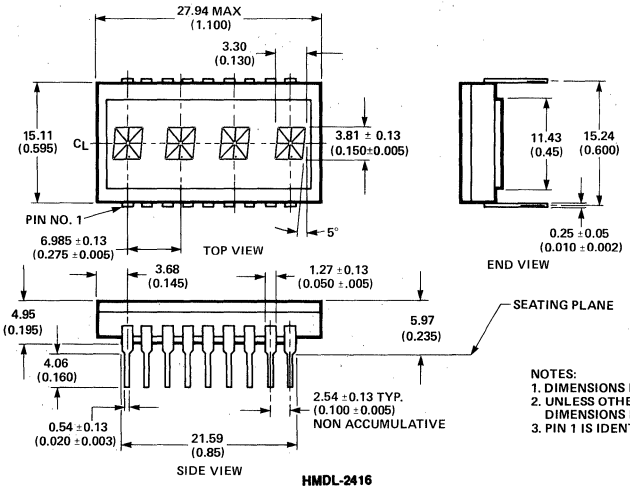
Free Air Operating
Temperature Range, T_A ..... -55° to +100° C

Storage Temperature, T_S ..... -65° to +125° C

Maximum Solder Temperature, 1.59 mm (0.063 in.)
below Seating Plane, t < 5 sec. ..... 260° C

ESD WARNING: The HMDL-2416 is implemented in a standard CMOS process with diode protection of all inputs. The ESD susceptibility of this IC device is Class A of MIL-STD-883 or Class 2 of DOD-STD-1686 and DOD-HDBK-263. Standard precautions for handling CMOS devices should be observed.

Package Dimensions



HMDL-2416

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	$\overline{CE}_1$ CHIP ENABLE	10	GND
2	$\overline{CE}_2$ CHIP ENABLE	11	D_0 DATA INPUT
3	$\overline{CLR}$ CLEAR	12	D_1 DATA INPUT
4	$\overline{CUE}$ CURSOR ENABLE	13	D_2 DATA INPUT
5	$\overline{CU}$ CURSOR SELECT	14	D_3 DATA INPUT
6	$\overline{WR}$ WRITE	15	D_6 DATA INPUT
7	A_1 DIGIT SELECT	16	D_5 DATA INPUT
8	A_0 DIGIT SELECT	17	D_4 DATA INPUT
9	V_{CC}	18	$\overline{BL}$ DISPLAY BLANK

NOTES:
1. DIMENSIONS IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±0.38 mm (0.015").
3. PIN 1 IS IDENTIFIED BY INK DOT ON BOTTOM OF PACKAGE.

Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage High	V_{IH}	2.0			V
Input Voltage Low	V_{IL}			0.8	V

DC Electrical Characteristics Over Operating Temperature Range

TYPICAL VALUES

Parameter	Symbol	Units	-55°C	25°C	+100°C	Test Condition
I_{CC} 4 digits on (10 seg/digit)[1,2]	I_{CC}	mA	120	85	70	V_{CC} = 5.0 V
I_{CC} Cursor[2,3,4]	$I_{CC}(\overline{CU})$	mA	170	125	105	V_{CC} = 5.0 V
I_{CC} Blank	$I_{CC}(\overline{BL})$	mA	1.8	1.5	1.3	V_{CC} = 5.0 V $\overline{BL}$ = 0.8 V
Input Current, Max.	I_{IL}	μA	22	17	12	V_{CC} = 5.0 V V_{IN} = 0.8 V
Thermal Resistance Junction to Case	$R\Theta_{J-C}$	°C/W/ Device		20		

GUARANTEED VALUES

Parameter	Symbol	Units	25°C V_{CC} = 5.0 V	Maximum Over Operating Temperature Range V_{CC} = 5.5 V
I_{CC} 4 digits on (10 seg/digit)[1,2]	I_{CC}	mA	115	167
I_{CC} Cursor[2,3,4]	$I_{CC}(\overline{CU})$	mA	165	225
I_{CC} Blank	$I_{CC}(\overline{BL})$	mA	3.5	8.0
Input Current, Max.	I_{IL}	μA	30	40
Power Dissipation[5]	P_D	mW	575	918
Leak Rate	LR	cc/sec		5×10^{-8}

Notes:
1. "%" illuminated in all four characters.
2. Measured at five seconds.
3. Cursor character is sixteen segments and DP on.
4. Cursor operates continuously over operating temperature range.
5. Power dissipation = $V_{CC} \cdot I_{CC}$ (10 seg.).

AC Timing Characteristics Over Temperature at V_{CC} = 4.5 V [1]

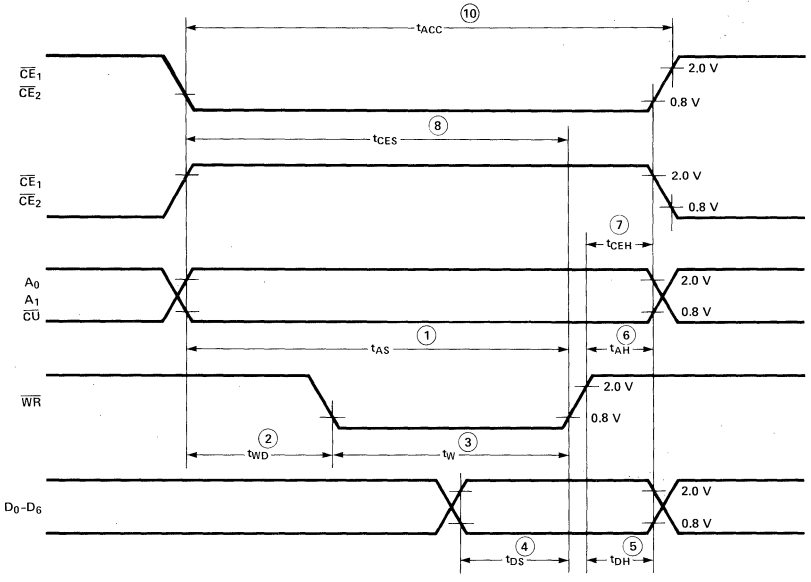
Symbol	Description	-20° C t_{MIN}	25° C t_{MIN}	70° C t_{MIN}	Units
1 t_{AS}	Address Setup Time	90	115	150	ns
2 t_{WD}	Write Delay Time	10	15	20	ns
3 t_W	Write Time	80	100	130	ns
4 t_{DS}	Data Setup Time	40	60	80	ns
5 t_{DH}	Data Hold Time	40	45	50	ns
6 t_{AH}	Address Hold Time	40	45	50	ns
7 t_{CEH}	Chip Enable Hold Time	40	45	50	ns
8 t_{CES}	Chip Enable Setup Time	90	115	150	ns
9 t_{CLR}	Clear Time	2.4	3.5	4.0	ms
10 t_{ACC}	Access Time	130	160	200	ns
	Refresh Rate	420-790	310-630	270-550	Hz

Note: 1. These parameters are guaranteed by design but are not tested.

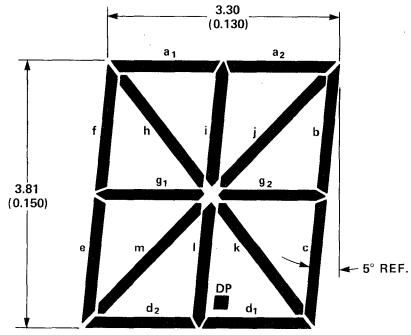
Optical Characteristics

Parameter	Symbol	Test Condition	Min.	Typ.	Units
Peak Luminous Intensity per digit, 8 segments on (character average)	I_V Peak	V_{CC} = 5.0 V "✳" illuminated in all 4 digits (25°C)	0.2	0.6	mcd
Peak Wavelength	λpeak			655	nm
Dominant Wavelength	λ_d			640	nm
Off Axis Viewing Angle				±65	degrees
Digit Size				3.81	mm

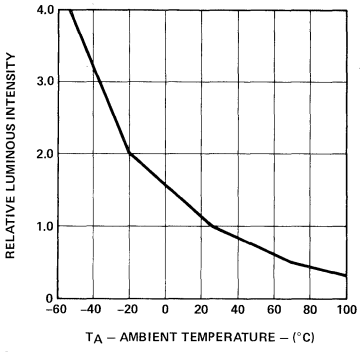
Timing Diagram



Character Font Description



Relative Luminous Intensity vs. Temperature



Electrical Description

Display Internal Block Diagram

Figure 1 shows the internal block diagram for the HMDL-2416 display. The CMOS IC consists of a four-word ASCII memory, a four-word cursor memory, a 64-word character generator, 17 segment drivers, four digit drivers, and the scanning circuitry necessary to multiplex the four monolithic LED characters. In normal operation, the divide-by-four counter sequentially accesses each of the four RAM locations and simultaneously enables the appropriate display digit driver. The output of the RAM is decoded by the character generator which, in turn, enables the appropriate display segment drivers. For each display location, the cursor enable (CUE) selects whether the data from the ASCII RAM (CUE = 0) or the stored cursor (CUE = 1) is to be displayed. The cursor character is denoted by all sixteen segments and the DP ON. Seven-bit ASCII data is stored in RAM. Since the display utilizes a 64-character decoder, half of the possible 128 input combinations are invalid. For each display location where $D_5 = D_6$ in the ASCII RAM, the display character is blanked. The entire display is blanked when $\overline{BL} = 0$.

Data is loaded into the display through the data inputs (D_6- D_0), digit selects (A_1, A_0), chip enables ($\overline{CE}_1$, $\overline{CE}_2$, cursor select ($\overline{CU}$), and write ($\overline{WR}$). The cursor select ($\overline{CU}$) determines whether data is stored in the ASCII RAM ($\overline{CU}$ = 1) or cursor memory ($\overline{CU}$ = 0). When $\overline{CE}_1 = \overline{CE}_2 = \overline{WR} = 0$ and $\overline{CU} = 1$, the information on the data inputs is stored in the ASCII RAM at the location specified by the digit selects (A_1, A_0). When $\overline{CE}_1 = \overline{CE}_2 = \overline{WR} = 0$ and $\overline{CU} = 0$, the information on the data input, D_0, is stored in the cursor at the location specified by the digit selects (A_1, A_0). If $D_0 = 1$, a cursor character is stored in the cursor memory. If $D_0 = 0$, a previously stored cursor character will be removed from the cursor memory.

If the clear input ($\overline{CLR}$) equals zero for one internal display cycle (4 ms minimum), the data in the ASCII RAM will be rewritten with zeroes and the display will be blanked. Note that the blanking input ($\overline{BL}$) must be equal to logical one during this time.

Data Entry

Figure 2 shows a truth table for the HMDL-2416 display. Setting the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) to their low state and the cursor select ($\overline{CU}$) to its high state will enable data loading. The desired data inputs (D_6-D_0) and address inputs (A_1, A_0) as well as the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and cursor select ($\overline{CU}$) must be held stable during the write cycle to ensure that the correct data is stored into the display. Valid ASCII data codes are shown in Figure 3. The display accepts standard seven-bit ASCII data. Note that $D_6 = \overline{D}_5$ for the codes shown in Figure 2. If $D_6 = D_5$ during the write cycle, then a blank will be stored in the display. Data can be loaded into the display in any order. Note that when $A_1 = A_0 = 0$, data is stored in the furthest right-hand display location.

Cursor Entry

As shown in Figure 2, setting the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) to their low state and the cursor select ($\overline{CU}$) to its low state will enable cursor loading. The cursor character is indicated by the display symbol having all 16 segments and the DP ON. The least significant data input (D_0), the digit selects (A_1, A_0), the chip enables ($\overline{CE}_1$, $\overline{CE}_2$), and the cursor select ($\overline{CU}$) must be held stable during the write cycle to ensure that the correct data is stored in the display. If D_0 is in a low state during the write cycle, then a cursor character will be removed at the indicated location. If D_0 is in a high state during the write cycle, then a cursor character will be stored at the indicated location. The presence or absence of a cursor character does not affect the ASCII data stored at that location. Again, when $A_1 = A_0 = 0$, the cursor character is stored in the furthest right-hand display location.

All stored cursor characters are displayed if the cursor enable (CUE) is high. Similarly, the stored ASCII data words are displayed, regardless of the cursor characters, if the cursor enable (CUE) is low. The cursor enable (CUE) has no effect on the storage or removal of the cursor characters within the display. A flashing cursor is displayed by pulsing the cursor enable (CUE). For applications not requiring a cursor, the cursor enable (CUE) can be connected to ground and the cursor select ($\overline{CU}$) can be connected to V_{CC}. This inhibits the cursor function and allows only ASCII data to be loaded into the display.

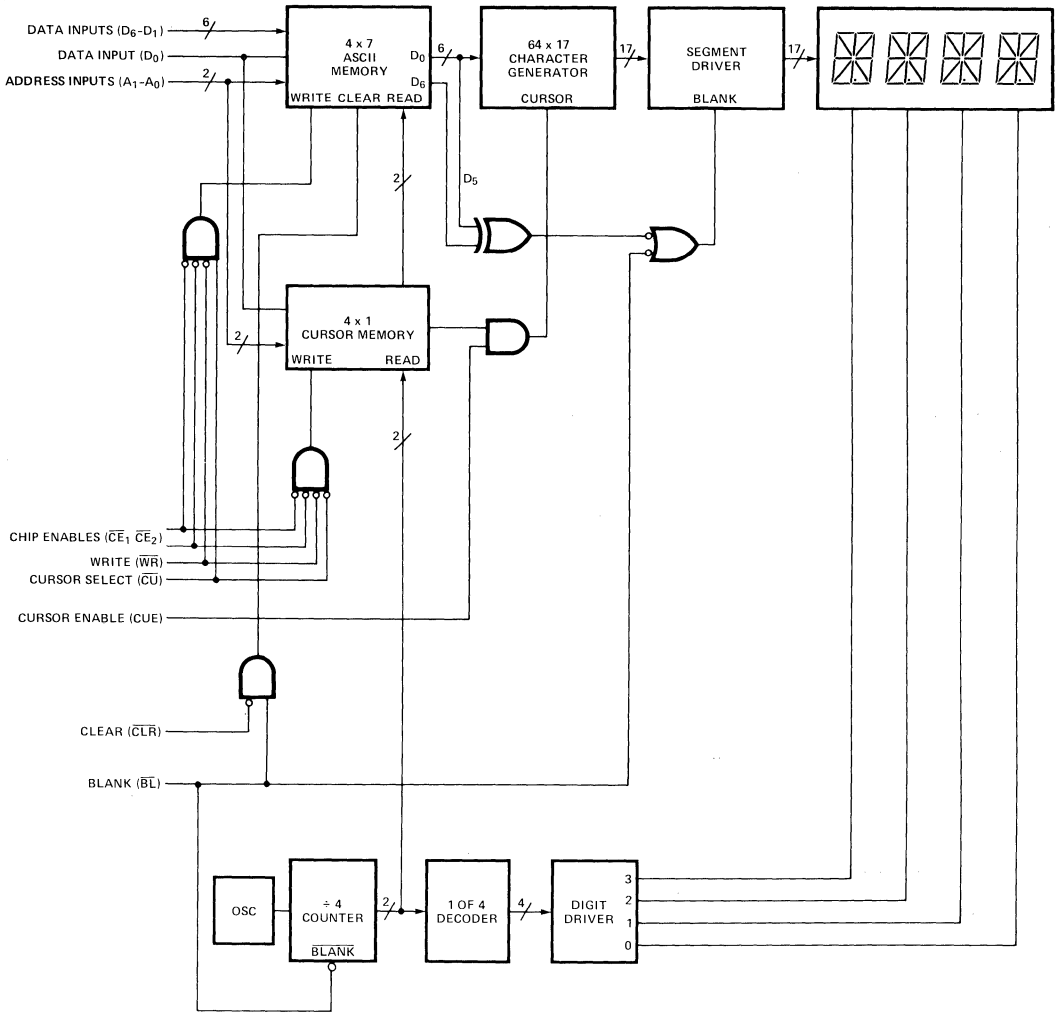


Figure 1. HMDL-2416 Internal Block Diagram

Display Clear

As shown in Figure 2, the ASCII data stored in the display will be cleared if the clear ($\overline{CLR}$) is held low and the blanking input ($\overline{BL}$) is held high for 4 ms minimum. The cursor memory is not affected by the clear ($\overline{CLR}$) input. Cursor characters can be stored or removed even while the clear ($\overline{CLR}$) is low. Note that the display will be cleared regardless of the state of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$). However, to ensure that all four display characters are cleared, $\overline{CLR}$ should be held low for 4 ms following the last write cycle.

Display Blank

As shown in Figure 2, the display will be blanked if the blanking input ($\overline{BL}$) is held low. Note that the display will be blanked regardless of the state of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) or write ($\overline{WR}$) inputs. The ASCII data stored in the display and the cursor memory are not affected by the blanking input. ASCII data and cursor data can be stored even while the blanking input ($\overline{BL}$) is low. Note that while the blanking input ($\overline{BL}$) is low, the clear ($\overline{CLR}$) function is inhibited. A flashing display can be obtained by applying a low frequency square wave to the blanking input ($\overline{BL}$). Because the blanking input ($\overline{BL}$) also resets the internal display multiplex counter, the frequency applied to the blanking input ($\overline{BL}$) should be much slower than the display multiplex rate. Finally, dimming of the display through the blanking input ($\overline{BL}$) is not recommended.

For further application information please consult Application Note 1026.

Function	$\overline{BL}$	$\overline{CLR}$	CUE	$\overline{CU}$	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WR}$	A_1	A_0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	DIG_3	DIG_2	DIG_1	DIG_0
Write Data Memory	L	X	X	H	L	L	L	L	L	a	a	a	a	a	a	a	NC	NC	NC	A
				—OR—				L	H	b	b	b	b	b	b	b	NC	NC	B	NC
	X	H	X	H	L	L	L	H	L	c	c	c	c	c	c	c	NC	C	NC	NC
								H	H	d	d	d	d	d	d	d	D	NC	NC	NC
Disable Data Memory Write	X	X	X	H	X	X	H	X	X	X	X	X	X	X	X	X	Previously Written Data			
	X	X	X	H	X	H	X													
	X	X	X	H	H	X	X													
Write Cursor	X	X	X	L	L	L	L	L	L	X	X	X	X	X	X	H	NC	NC	NC	▩
								L	H	X	X	X	X	X	X	H	NC	NC	▩	NC
								H	L	X	X	X	X	X	X	H	NC	▩	NC	NC
								H	H	X	X	X	X	X	X	H	▩	NC	NC	NC
Clear Cursor	X	X	X	L	L	L	L	L	L	X	X	X	X	X	X	L	NC	NC	NC	⬚
								L	H	X	X	X	X	X	X	L	NC	NC	⬚	NC
								H	L	X	X	X	X	X	X	L	NC	⬚	NC	NC
								H	H	X	X	X	X	X	X	L	⬚	NC	NC	NC
Disable Cursor Memory	X	X	X	L	X	X	H	X	X	X	X	X	X	X	X	X	Previously Written Cursor			
	X	X	X	L	X	H	X													
	X	X	X	L	H	X	X													

L = LOGIC LOW INPUT
H = LOGIC HIGH INPUT
X = DON'T CARE

"a" = ASCII CODE CORRESPONDING TO SYMBOL "A"
NC = NO CHANGE
▩ = CURSOR CHARACTER (ALL SEGMENTS ON)

Figure 2a. Cursor/Data Memory Write Truth Table

Function	$\overline{BL}$	$\overline{CLR}$	CUE	$\overline{CU}$	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WR}$	DIG_3	DIG_2	DIG_1	DIG_0	
CUE	H	H	L	X	X	X	X	A	B	C	D	Display previously written data
	H	H	H	X	X	X	X	▩	▩	▩	▩	Display previously written cursor
Clear	H	L	X	X	X	X	X*	⬚	⬚	⬚	⬚	Clear data memory, cursor memory unchanged
	*NOTE: CLR should be held low for 4 ms following the last WRITE cycle to ensure all data is cleared.											
Blanking	L	X	X	X	X	X	X	⬚	⬚	⬚	⬚	Blank display, data and cursor memories unchanged.

Figure 2b. Displayed Data Truth Table

BITS	D_3 D_2 D_1 D_0	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
D_6 D_5 D_4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 1 0	2	(space)	!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
0 1 1	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
1 0 0	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1 0 1	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_

Figure 3. HPDL-2416 ASCII Character Set

Mechanical and Electrical Considerations

The HMDL-2416 is an 18 pin dual-in-line package, that can be stacked horizontally and vertically to create arrays of any size. The HMDL-2416 is designed to operate continuously from -55° to +100°C for all possible input conditions including the illuminated cursor in all four character locations. The HMDL-2416 is assembled by die attaching and wire bonding the four GaAsP/GaAs monolithic LED chips and the CMOS IC to a 18 lead ceramic-glass dual-in-line package. It is designed either to plug into DIP sockets or to solder into PC boards.

The inputs of the CMOS IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HMDL-2416 should be stored in anti-static tubes or conductive material. During assembly, a grounded conductive work area should be used. The assembly personnel should use conductive wrist straps. Lab coats made of synthetic materials should be avoided since they are prone to static charge build-up. Input current latchup is caused when the CMOS inputs are subjected to a voltage either below ground (V_{IN} < ground) or to a higher voltage than V_{CC} (V_{IN} > V_{CC}) and a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{CC}, voltages should not be applied to the inputs until V_{CC} has been applied to the display, and transient input voltages should be eliminated.

Soldering and Post Solder Cleaning Instructions for the HMDL-2416

The HMDL-2416 may be hand soldered or wave soldered with SN63 solder. Hand soldering may be safely performed only with an electronically temperature-controlled and securely grounded soldering iron. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux or a water soluble organic acid (OA) flux can be used. The solder wave temperature should be 245°C ±5°C (473°F ±9°F), and the dwell in the wave should be set at 1 1/2 to 3 seconds for optimum soldering.

Post solder cleaning may be accomplished using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, Genesolv DES, and water.

For further information on soldering, refer to Application Note 1027, "Soldering LED Components".

Optical Considerations/ Contrast Enhancement

Each HMDL-2416 display is tested for luminous intensity and marked with an intensity category on the back of the display package. To ensure intensity matching for multiple package applications, all displays for a given panel should have the same category.

The HMDL-2416 display is designed to provide maximum contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Dark Red 63, SGL Homalite H100-1650, Rohm and Haas 2423, Chequers Engraving 118, and 3M R6510. For further information on contrast enhancement, see Hewlett-Packard Application Note 1015.

High Reliability Testing

Two standard high reliability testing programs are available. The TXVB program is in conformance with MIL-D-87157 level A Test Tables. The TXVB product is tested to Tables I, II, IIIa, and IVa. The TXV program is an HP modification to the full conformance program and offers the 100% screening of Quality Level A, Table I, and Group A, Table II.

Part Marking System

Standard Product	With Table I and II	With Tables I, II, IIIa, IVa
HMDL-2416	HMDL-2416TXV	HMDL-2416TXVB

100% Screening

Table I. Quality Level A of MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	2072	Interpreted by HP Procedure 5956-7235-52
2. High Temperature Storage	1032	T_A = 125°C, Time = 24 hours
3. Temperature Cycling	1051	Condition B, 10 cycles, 15 min. dwell
4. Constant Acceleration	2006	5,000 G's at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K
7. Interim Electrical/Optical Tests[2]	—	I_{CC}, I_V @ V_{CC} = 5.0 V T_A = 25°C
8. Burn-In[1]	1015	Condition B at V_{CC} = 5.5 V T_A = 100°C t = 160 hours
9. Final Electrical Test[2]	—	I_{CC}%, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$) I_{IL}, I_V @ V_{CC} = 5.0 V T_A = 25°C
10. Delta Determinations	—	$\Delta I_{CC} = \pm$ 10% ΔI_V = - 20% T_A = 25°C
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method Applies
2. Limits and conditions are per the electrical optical characteristics.

Table II. Group A Electrical Tests — MIL-D-87157

Subgroup/Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_{CC}%, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V and visual function @ V_{CC} = 5.0 V	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = +100°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = -55°C	7
Subgroup 4, 5, and 6 not applicable		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

Note:
1. Limits and conditions are per the electrical/optical characteristics.

Table IIIa. Group B, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Design Verification[1]	2075[6]		1 Device/ 0 Failures
Subgroup 2[2,3] Solderability	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	Condition B1, 15 minute dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Electrical/Optical Endpoints[5]	—	I_{CC}%, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V @ V_{CC} = 5.0 V and visual function. T_A = 25°C	
Subgroup 4 Operating Life Test (340 hrs.)	1027	T_A = 100°C @ V_{CC} = 5.5 V	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	
Subgroup 5 Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +125°C	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	

Notes:
1. Visual inspection is performed through the display window.
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend for one cycle.
5. Limits and conditions are per the electrical/optical characteristics.
6. Equivalent to MIL-STD-883, Method 2014.

Table IVa. Group C, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2]			
Lead Integrity[7, 9]	2004	Condition B2	LTPD = 15
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	5,000 G's at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_{CC}%, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V @ V_{CC} = 5.0 V and visual function. T_A = 25°C	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			
Operating Life Test[6]	1026	T_A = 100°C @ V_{CC} = 5.5 V	λ = 10
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.
9. Initial conditioning is a 15° inward bend for three cycles.

HEWLETT PACKARD

CMOS Hermetic Extended Temperature Range 5x7 Alphanumeric Displays

Technical Data

HCMS-201X/201XTXV/ 201XTXVB Series
HCMS-231X/231XTXV/ 231XTXVB

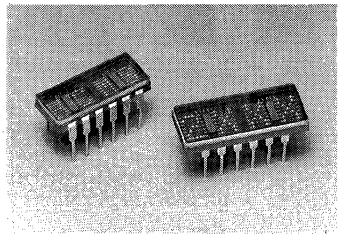
Sunlight Viewable Series HCMS-235X/ 235XTXV/235XTXVB Series

Features

- **On-Board Low Power CMOS IC**
  Integrated Shift Register with Constant Current LED Drivers
- **Wide Operating Temperature Range**
  -55°C to +100°C
- **HI-REL Screening per MIL-D-87157**
  Quality Level A
  TXV or TVXB
- **Hermetic Package**
- **Compact Glass Ceramic 4 Character Package**
  HCMS-201X Series End Stackable
  HCMS-231X/-235X Series X-Y Stackable
- **HCMS-235X Series are Sunlight Viewable**
- **Five Colors**
  Standard Red
  High Efficiency Red
  Orange
  Yellow
  High Performance Green
- **5x7 LED Matrix Displays Full ASCII Set**
- **Two Character Heights**
  3.8mm (0.15 inch)
  5.0mm (0.20 inch)
- **Wide Viewing Angle**
  X Axis = ±50°
  Y Axis = ±65°
- **Long Viewing Distance**
  HCMS-201X Series to 2.6 Meters (8.6 Feet)
  HCMS-231X/-235X Series to 3.5 Meters(11.5 Feet)
- **Categorized for Luminous Intensity**
- **HCMS-2011/2013**
  HCMS-2311/-2313/-2314
  HCMS-2351/-2353/-2354
  Useable in Night Vision Lighting Applications
- **HCMS-2011/-2013, HCMS-2311/-2313 and HCMS-2351/-2353:**
  Categorized for Color

Typical Applications

- **Military Avionics**
- **Communications Systems**
- **Radar Systems**
- **Fire Control Systems**



Description

The HCMS-201X, HCMS-231X and the sunlight viewable HCMS-235X series are 5x7 LED four character displays contained in 12 pin dual-in-line packages designed for displaying alphanumeric information. The character height for the HCMS-201X series displays is 3.8mm (0.15 inch), and for the HCMS-231X and HCMS-235X series displays the character height is 5.0mm (0.20 inch). The HCMS-201X series displays are available in four LED colors: standard red, high efficiency red, yellow and high performance green. The HCMS-231X series are available in all five

ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED.

LED colors. The HCMS-235X series displays are available in four LED colors: high efficiency red, orange, yellow and high performance green. The HCMS-201X series displays are end stackable. The HCMS-231X and HCMS-235X series displays are end/row stackable.

These displays are designed with on-board CMOS integrated circuits for use in applications where conservation of power is important. The two CMOS ICs form an on-board 28-bit serial-in-parallel-out shift register with constant current output LED row drivers. Decoded column data is clocked into the on-board shift register for each refresh cycle. Full character display is achieved with external column strobing.

Compatibility with HDSP-201X/-231X/-235X TTL IC Series Displays

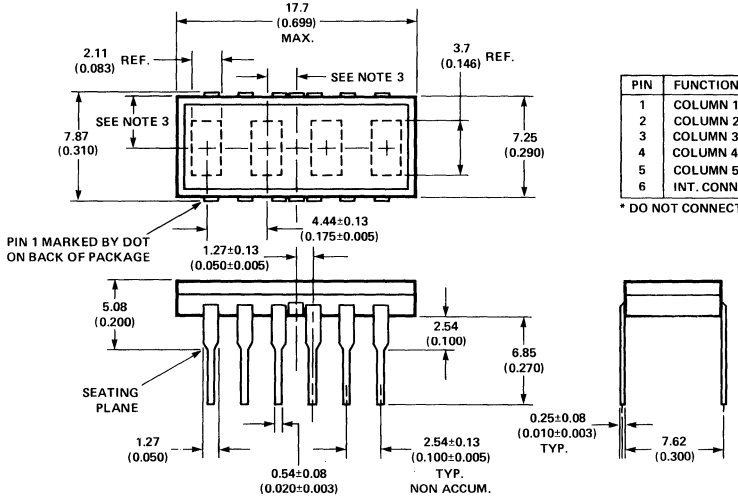
The HCMS-201X, HCMS-231X and HCMS-235X CMOS IC displays are "drop-in" replacements for the equivalent HDSP-201X, HDSP-231X and HDSP-235X TTL IC displays. The 12 pin glass/ceramic package configuration, four digit character matrix and pin functions are identical.

Display Selection Table

Part Number	Character Size	LED Color
HCMS-2010/2010TXV/2010TXVB	3.8 mm (0.15 inch)	Standard Red
HCMS-2011/2011TXV/2011TXVB	3.8 mm (0.15 inch)	Yellow
HCMS-2012/2012TXV/2012TXVB	3.8 mm (0.15 inch)	High-Efficiency Red
HCMS-2013/2013TXV/2013TXVB	3.8 mm (0.15 inch)	High-Performance Green
HCMS-2310/2310TXV/2310TXVB	5.0 mm (0.20 inch)	Standard Red
HCMS-2311/2311TXV/2311TXVB	5.0 mm (0.20 inch)	Yellow
HCMS-2312/2312TXV/2312TXVB	5.0 mm (0.20 inch)	High-Efficiency Red
HCMS-2313/2313TXV/2313TXVB	5.0 mm (0.20 inch)	High-Performance Green
HCMS-2314/2314TXV/2314TXVB	5.0 mm (0.20 inch)	Orange
Sunlight Viewable Displays		
HCMS-2351/2351TXV/2351TXVB	5.0 mm (0.20 inch)	Yellow
HCMS-2352/2352TXV/2352TXVB	5.0 mm (0.20 inch)	High-Efficiency Red
HCMS-2353/2353TXV/2353TXVB	5.0 mm (0.20 inch)	High-Performance Green
HCMS-2354/2354TXV/2354TXVB	5.0 mm (0.20 inch)	Orange

Note:
Basic part numbers (ie. HCMS-2351) are without hi-rel screening. Part numbers with TXV or TXVB suffix (ie. HCMS-2351TXV) are with hi-rel screening per MIL-D-87157, Quality Level A.

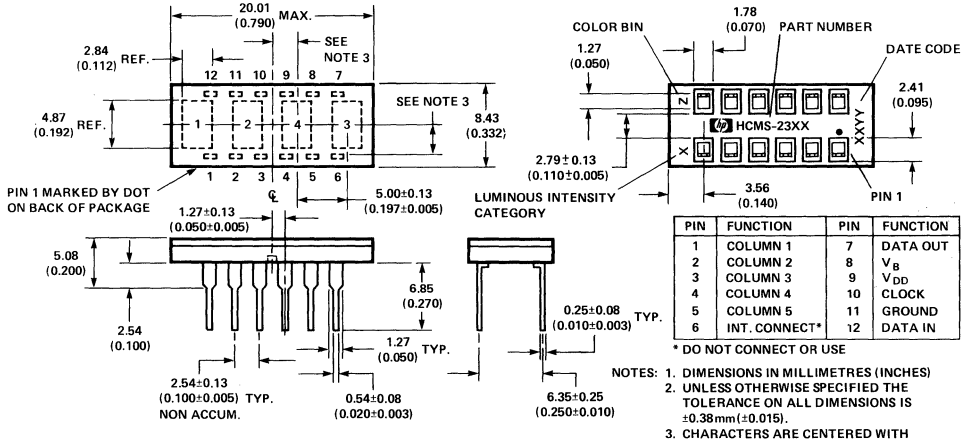
Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{DD}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

* DO NOT CONNECT OR USE

HCMS-201X Series



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{DD}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

* DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN MILLIMETRES (INCHES)
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±0.38mm (±0.015).
3. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±0.13mm (±0.005").
4. LEAD MATERIAL IS COPPER ALLOY, SOLDER DIPPED.

HCMS-231X/-235X Series

Absolute Maximum Ratings

Supply Voltage V_{DD} to Ground .....–0.3 V to 7.0 V
Data Input, Data Output, V_B .....–0.3 V to V_{DD}
Column Input Voltage, V_{COL} .....–0.3 V to V_{DD}
Free Air Operating Temperature Range, T_A .....–55°C to +100°C
Storage Temperature Range, T_S .....–65°C to +125°C
HCMS-2310/-2311/-2312/-2314
HCMS-2351/-2352/-2354
Storage Temperature Range, T_S .....–55°C to +100°C
HCMS-2010/-2011/-2012/-2013
HCMS-2313
HCMS-2353
Maximum Allowable Package Power Dissipation, P_D [1,2]
HCMS-2010/-2011/-2012/-2013 at T_A = 83°C .....0.79 Watts
HCMS-2310/-2311/-2312/-2313/-2314 at T_A = 88°C .....0.92 Watts
HCMS-2351/-2352/-2353/-2354 at T_A = 71°C .....1.31 Watts
Maximum Solder Temperature
1.59 mm (0.063") Below Seating Plane, t ≤ 5 sec .....260°C
ESD Protection @ 1.5kΩ, 100pf .....V_Z = 4 kV (each pin)

Notes:
1. Maximum allowable power dissipation is derived from V_{DD} = 5.25 V, V_B = 2.4 V, V_{COL} = 3.5 V, 20 LEDs ON per character, 20% DF.
2. The power dissipation for these displays should be derated as follows:
   HCMS-201X series derate above 83°C at 17 mW/°C, $R\theta_{J-A}$ = 60°C/W
   HCMS-231X series derate above 88°C at 22 mW/°C, $R\theta_{J-A}$ = 45°C/W
   HCMS-325X series derate above 71°C at 23 mW/°C, $R\theta_{J-A}$ = 45°C/W.

Deratings based on $R\theta_{PC-A}$ = 35°C/W per display for printed circuit board assembly.
See Figure 1 for power derating based on lower $R\theta_{J-A}$ values.

Recommended Operating Conditions Over Operating Temperature Range (-55°C to +100°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}	4.75	5.00	5.25	V
Data Out Current, Low State	I_{OL}			1.6	mA
Data Out Current, High State	I_{OH}			-0.5	mA
Column Input Voltage	V_{COL}	2.75	3.0	3.5	V
Setup Time	t_{SETUP}	10			ns
Hold Time	t_{HOLD}	25			ns
Clock Pulse Width High	$t_{WH(CLOCK)}$	50			ns
Clock Pulse Width Low	$t_{WL(CLOCK)}$	50			ns
Clock High to Low Transition	t_{THL}			200	ns
Clock Frequency	f_{CLOCK}			5	MHz

Electrical Characteristics
Over Operating Temperature Range (-55°C to +100°C)

Parameter	Symbol	Test Conditions	Min.	Typ.*	Max.	Units
Supply Current, Dynamic[1]	I_{DDD}	f_{CLOCK} = 5 MHz		6.2	7.8	mA
Supply Current, Static[2]	I_{DDSoff} I_{DDSon}	V_B = 0.4 V V_B = 2.4 V		1.8 2.2	2.6 3.3	mA
Column Input Current	I_{COL}	V_B = 0.4 V			10	µA
HCMS-2010/-2011/-2012/-2013		V_B = 2.4 V		310	384	mA
HCMS-2310/-2311/-2312/-2313/-2314		V_B = 2.4 V		360	451	mA
HCMS-2351/-2352/-2353/-2354		V_B = 2.4 V		500	650	mA
Input Logic High Data, V_B, Clock	V_{IH}	V_{DD} = 4.75 V	2.0			V
Input Logic Low Data, V_B, Clock	V_{IL}	V_{DD} = 5.25 V			0.8	V
Input Current Data, Clock V_B	I_I	V_{DD} = 5.25 V $0 \le V_I \le 5.25$ V $0 \le V_B \le 5.25$ V	 -10 -40		 +10 0	µA
Data Out Voltage	V_{OH}	V_{DD} = 4.75 V I_{OH} = -0.5 mA I_{COL} = 0 mA	2.4	4.2		V
	V_{OL}	V_{DD} = 5.25 V I_{OL} = 1.6 mA I_{COL} = 0 mA		0.2	0.4	V
Power Dissipation Per Package[3] HCMS-2010/-2011/-2012/-2013 HCMS-2310/-2311/-2312/-2313/-2314 HCMS-2351/-2352/-2353/-2354	P_D	V_{DD} = 5.0 V V_{COL} = 3.5 V 17.5% DF V_B = 2.4 V 15 LEDs ON per Character		 414 481 668		mW
Thermal Resistance IC Junction-to-Pin[4] HCMS-2010/-2011/-2012/-2013 HCMS-2310/-2311/-2312/-2313/-2314 HCMS-2351/-2352/-2353/-2354	$R\theta_{J\text{-}PIN}$			 25 10 10		°C/W
Leak Rate					$5x10^{-8}$	cc/sec

*All typical values specified at V_{DD} = 5.0V and T_A = 25°C.

Notes:
1. I_{DD} Dynamic is the IC current while clocking column data through the on-board shift register at a clock frequency of 5MHz, the display is not illuminated.
2. I_{DD} Static is the IC current after column data is loaded and not being clocked through the on-board shift register.
3. Four characters are illuminated with a typical ASCII character composed of 15 dots per character.
4. IC junction temperature $T_J(IC) = (P_D)(R\theta_{J\text{-}PIN} + R\theta_{PC\text{-}A}) + T_A$

Optical Characteristics at $T_A = 25°C$

Standard Red HCMS-2010/-2310

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2010	I_{vPEAK}	$V_{DD} = 5.0$ V, $V_{COL} = 3.5$ V, $V_B = 2.4$ V, $T_j = 25°C$[7]	105	200		µcd
HCMS-2310			220	370		
Dominant Wavelength[8]	λ_d			639		nm
Peak Wavelength	λ_{PEAK}			655		nm

Yellow HCMS-2011/-2311/-2351

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2011	I_{vPEAK}	$V_{DD} = 5.0$ V, $V_{COL} = 3.5$ V, $V_B = 2.4$ V, $T_j = 25°C$[7]	400	750		µcd
HCMS-2311			650	1140		
HCMS-2351			2400	3400		
Dominant Wavelength[6,8]	λ_d			585		nm
Peak Wavelength	λ_{PEAK}			583		nm

High Efficiency Red HCMS-2012/-2312/-2352

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2012	I_{vPEAK}	$V_{DD} = 5.0$ V, $V_{COL} = 3.5$ V, $V_B = 2.4$ V, $T_j = 25°C$[7]	400	1430		µcd
HCMS-2312			650	1430		
HCMS-2352			1920	2850		
Dominant Wavelength[8]	λ_d			625		nm
Peak Wavelength	λ_{PEAK}			635		nm

High Performance Green HCMS-2013/-2313/-2353

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2013	I_{vPEAK}	$V_{DD} = 5.0$ V, $V_{COL} = 3.5$ V, $V_B = 2.4$ V, $T_j = 25°C$[7]	850	1550		µcd
HCMS-2313			1280	2410		
HCMS-2353			2400	3000		
Dominant Wavelength[6,8]	λ_d			574		nm
Peak Wavelength	λ_{PEAK}			568		nm

Orange HCMS-2314/-2354

Description		Symbol	Test Condition	Min.	Typ.	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average)	HCMS-2314 HCMS-2354	I_{vPEAK}	V_{DD} = 5.0 V V_{COL} = 3.5 V V_B = 2.4 V T_j = 25°C[7]	650 1920	1430 2850		µcd
Dominant Wavelength[8]		λ_d			602		nm
Peak Wavelength		λ_{PEAK}			600		nm

All typical values specified at V_{DD} = 5.0 V and T_A = 25°C unless otherwise noted.

Notes:

5. These LED displays are categorized for luminous intensity, with the intensity category designated by a letter code on the back of the package.
6. The HCMS-2011/-2311/-2351 and HCMS-2013/-2313/-2353 are categorized for color with the color category designated by a number on the back of the package.
7. Ti refers to the initial case temperature of the display immediately prior to the light measurement.
8. Dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram, and represents the single wavelength which defines the color of the device.
9. The luminous sterance of the individual LED pixels may be calculated using the following equations:

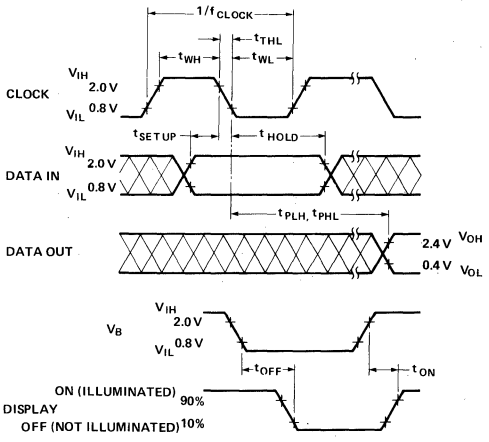
$L_v(cd/m^2) = I_v(Candela)*DF/A(Metre)^2$

$L_v(Footlamberts) = \pi I_v(Candela)*DF/A(Foot)^2$

Where: A = LED pixel area = 5.3 x $10^{-8}M^2$ or 5.8 x $10^{-7}ft^2$

DF = LED on-time duty factor

Switching Characteristics, T_A = –55°C to +100°C



Parameter	Condition	Typ.	Max.	Units
f_{clock} CLOCK Rate			5	MHz
t_{PLH}, t_{PHL} Propagation Delay CLOCK to DATA OUT	C_L = 15 pF R_L = 2.4 kΩ		105	ns
t_{OFF} V_B (0.4 V) to Display OFF		4	5	µs
t_{ON} V_B (2.4 V) to Display ON		1	2	

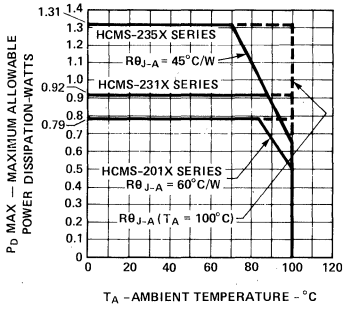


Figure 1. Maximum Allowable Power Dissipation vs Ambient Temperature as a Function of Thermal Resistance Junction-to-Ambient, $R\theta_{J-A}$. Derated Operation Assumes $R\theta_{PC-A}$ = 35°C/W per Display for Printed Circuit Board.
T_J (IC) MAX = 130°C.
$R\theta_{J-A}$ (T_A = 100°C)
= 22°C/W for HCMS-235X Series
= 32°C/W for HCMS-231X Series
= 38°C/W for HCMS-201X Series

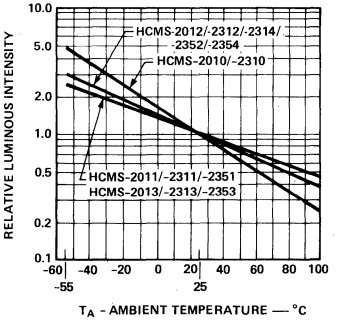


Figure 2. Relative Luminous Intensity vs Display Pin Temperature

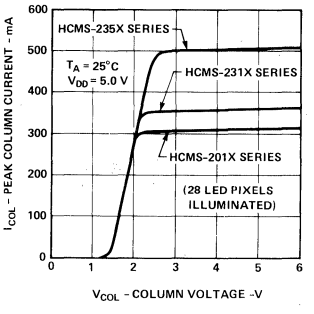


Figure 3. Peak Column Current vs Column Voltage

Electrical Description

Each display device contains four 5x7 LED dot matrix characters and two CMOS integrated circuits, as shown in Figure 4. The two CMOS integrated circuits form an on-board 28 bit serial-in-parallel-out shift register that will accept standard TTL logic levels. The Data Input, pin 12, is connected to bit position 1 and the Data Output, pin 7, is connected to bit position 28. The shift register outputs control constant current sinking LED row drivers. The nominal current sink per LED driver is 11mA for the HCMS-201X displays, 13mA for the HCMS-231X displays and 18mA for the HCMS-235X displays. A logic 1 stored in the shift register enables the corresponding LED row driver and a logic 0 stored in the shift register disables the corresponding LED row driver.

The electrical configuration of these CMOS IC alphanumeric displays allows for an effective interface to a display controller circuit that supplies decoded character information. The row data for a given column (one 7 bit byte per character) is loaded (bit serial) into the on-board 28 bit shift register with high to low transitions of the Clock input. To load decoded character information into the display, column data for character 4 is loaded first and the column data for character 1 is loaded last in the following manner. The 7 data bits for column 1, character 4, are loaded into the on-board shift register. Next, the 7 data bits for column 1, character 3, are loaded into the shift register, shifting the character 4 data over one character position. This process is repeated for the other two characters until all 28 bits of column data (four 7 bit bytes of character column data) are loaded into the on-board shift register. Then the column 1 input, V_{COL} pin 1, is energized to illuminate column 1 in all four characters. This process is repeated for columns 2, 3, 4 and 5. All V_{COL} inputs should be at logic low to insure the display is off when loading data. The display will be blanked when the blanking input V_B, pin 8, is at logic low regardless of the outputs of the shift register or whether one of the V_{COL} inputs is energized.

Refer to Application Note 1016 for drive circuit information.

ESD Susceptibility

The HCMS-201X/-231X/-235X series displays have an ESD susceptibility ratings of CLASS 3 per DOD-STD-1686 and CLASS B per MIL-STD-883C. It is recommended that normal CMOS handling precautions be observed with these devices.

Soldering and Post Solder Cleaning

These displays may be soldered with a standard wave solder process using either an RMA flux and solvent cleaning or an OA flux and aqueous cleaning.

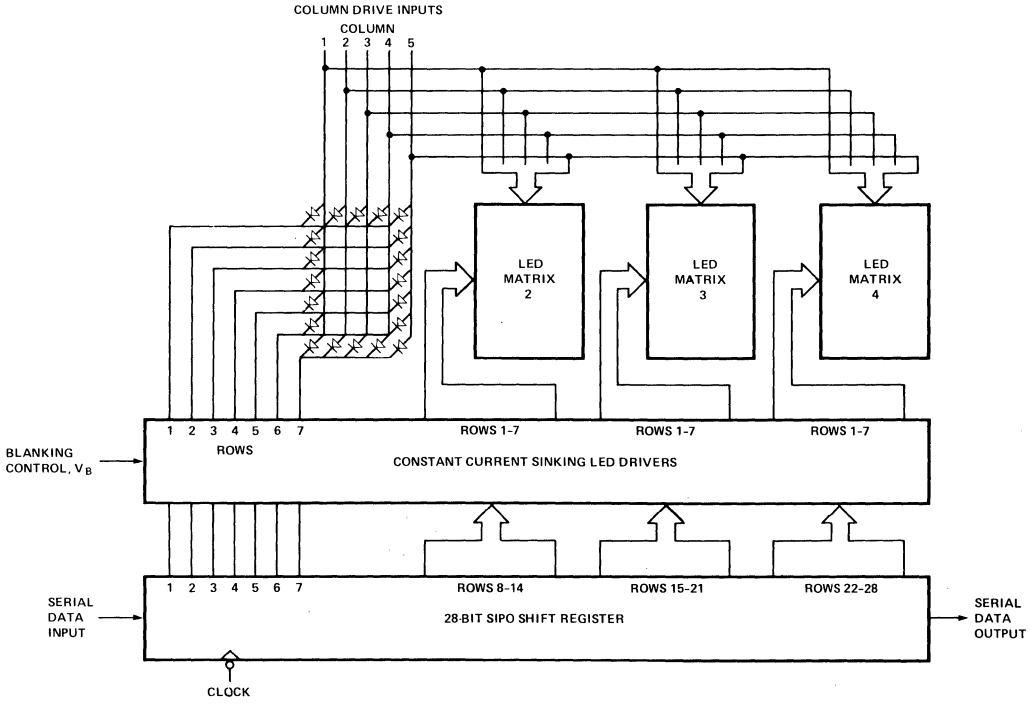


Figure 4. Block Diagram of an HCMS-2XXX Series LED Alphanumeric Display.

For optimum soldering, the solder wave temperature should be 245°C and the dwell time for any display lead passing through the wave should be 1 1/2 to 2 seconds. The recommended solvent for post solder cleaning is Genesolv DES, manufactured by Allied Chemical. For aqueous cleaning, a water temperature of 60°C (140°F) with an immersion time not exceeding 15 minutes is recommended. For more detailed information, refer to Application *Note 1027 Soldering LED Components.*

Contrast Enhancement

When used with the proper contrast enhancement filters, the HCMS-235X series displays are readable in sunlight and the HCMS-201X/231X series displays are readable in daylight ambients. Refer to Application Note 1029 *Luminous Contrast and Sunlight Readability of the HDSP-238X Series Alphanumeric Displays* for Military Applications for information on contrast enhancement for sunlight and daylight ambients. Refer to Application Note 1015 *Contrast Enhancement Techniques for LED Displays* for information on contrast enhancement in moderate ambients.

Night Vision Lighting

When used with the proper NVG/DV filters, the HCMS-2311/-2351 and HCMS-2133/-2353 displays may be used in night vision lighting applications. The HCMS-2311/-2351 (yellow) displays are used as master caution and warning indicators. The HCMS-2313/-2353 (high performance green) displays are used for general instrumentation. For a list of NVG/DV filters and a discussion on night vision lighting technology, refer to Application Note 1030 *LED Displays and Indicators and Night Vision Imaging System Lighting.*

Controller Circuits, Power Calculations and Display Dimming

Refer to Application Note 1016 *Using the HDSP-2000 Alphanumeric Display Family* for information on controller circuits to drive these displays, how to do power calculations and a technique for display dimming.

Table I. Quality Level A of MIL-D-87157 – 100% Screening

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	2072	Interpreted by HP Procedure 5956-7512-52
2. High Temperature Storage	1032	T_A = 125°C, Time = 24 hours[3]
3. Temperature Cycling	1051	Condition B, 10 cycles, 15 minute dwell
4. Constant Acceleration	2006	10,000 G's at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K[4]
7. Interim Electrical/ Optical Tests[1]	—	I_{DD} (at V_B = 0.4 V and 2.4 V), I_{COL} (at V_B = 0.4 V and 2.4 V) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} and I_{VPEAK}. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C
8. Burn-In[1]	1015	Condition B at V_{DD} = V_B = 5.25 V, V_{COL} = 3.5 V, T_A = +100°C LED ON-Time Duty Factor = 5%, 35 Dots On; t = 160 hours
9. Final Electrical Test[2]	—	Same as step 7
10. Delta Determinations	—	ΔI_{DD} = ±6 mA, ΔI_{IH} (clock) = ±10 µA, ΔI_{IH} (Data In) = ±10 µA ΔI_{OH} = ±10% of initial value, and ΔI_V = -20%, T_A = 25°C
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.
3. T_A = +100°C for HCMS-2013/-2313/-2353.
4. Fluid temperature = +100°C for HCMS-2013/-2313/-2353.

Table II. Group A Electrical Tests – MIL-D-87157

Subgroup Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_{DD} (at V_B = 0.4 V and 2.4 V), I_{COL} (at V_B = 0.4 V and 2.4 V) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and I_{VPEAK}. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test.	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1 except delete I_V and visual function, T_A = +100°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1 except delete I_V and visual function, T_A = -55°C	7
Subgroup 4, 5, and 6 not tested		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

Notes:
1. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

Table IIIa. Group B, Class A and B of MIL-D-87157

Subgroup Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Design Verification[1]	2075[7]		1 Device/ 0 Failures
Subgroup 2[2,3] Solderability	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	Condition B1, 15 minute dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K[8]	
Electrical/Optical Endpoints[5]	—	I_{DD} (at V_B = 0.4 V and 2.4 V), I_{COL} (at V_B = 0.4 V and 2.4 V), I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and I_{VPEAK}. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C	
Subgroup 4 Operating Life Test (340 hrs.)	1027	T_A = +100°C at V_{DD} = V_B = 5.25 V, V_{COL} = 3.5 V, LED ON-Time Duty Factor = 5%, 35 Dots On	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	
Subgroup 5 Non-Operating Storage Life Test (340 hrs.)	1032	T_A = +125°C[6]	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	

Notes:
1. Visual inspection is performed through the display window.
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend for one cycle.
5. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.
6. T_A = 100°C for HCMS-2013/-2313/-2353.
7. Equivalent to MIL-STD-883, Method 2014.
8. Fluid temperature = +100°C for HCMS-2013/-2313/-2353.

Table IVa. Group C, Class A and B of MIL-D-87157

Subgroup Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2] Lead Integrity[7,9]	2004	Condition B2	LTPD = 15
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K[10]	
Subgroup 3 Shock	2016	1500G. Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_{DD} (at V_B = 0.4 V and 2.4 V), I_{COL} (at V_B = 0.4 V and 2.4 V), I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL}, Visual Function and I_{VPEAK}. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C	
Subgroup 4[1,3] Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5 Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6 Operating Life Test[6]	1026	T_A = +100°C at V_{DD} = V_B = 5.25 V, V_{COL} = 3.5 V LED ON-Time Duty Factor = 5%, 35 Dots On	λ = 10
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical specifications.
9. Initial conditioning is a 15° inward bend for three cycles.
10. Fluid temperature = +100°C for HCMS-2013/-2313/-2353.

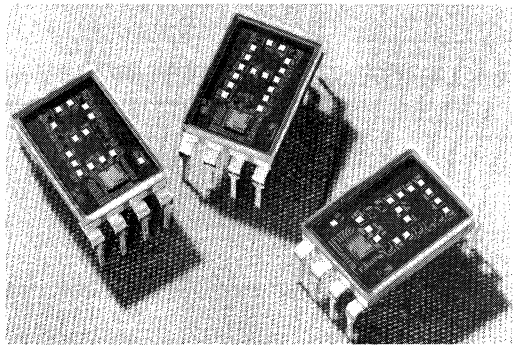
HEWLETT PACKARD

JAN QUALIFIED, HERMETIC, NUMERIC AND HEXADECIMAL DISPLAYS FOR MILITARY APPLICATIONS

4N51 / 4N51TXV / JM87157 / 00101AAX
4N52 / 4N52TXV / JM87157 / 00102AAX
4N53 / 4N53TXV / JM87157 / 00103AAX
4N54 / 4N54TXV / JM87157 / 00104AAX

Features

- **MILITARY QUALIFIED LISTED ON MIL-D-87157 QPL**
- **TRUE HERMETIC PACKAGE**
- **TXV VERSION AVAILABLE**
- **THREE CHARACTER OPTIONS Numeric, Hexadecimal, Over Range**
- **4 x 7 DOT MATRIX CHARACTER**
- **PERFORMANCE GUARANTEED OVER TEMPERATURE**
- **HIGH TEMPERATURE STABILIZED**
- **SOLDER DIPPED LEADS**
- **MEMORY LATCH/DECODER/DRIVER TTL Compatible**
- **CATEGORIZED FOR LUMINOUS INTENSITY**



Description

These standard red solid state displays have a 7.4 mm (0.29 inch) dot matrix character and an on-board IC with data memory latch/decoder and LED drivers in a glass/ceramic package. These devices utilize a solder glass frit seal and conform to the hermeticity requirements of MIL-D-87157, the general specification for LED displays. These 4N5X series displays are designed for use in military and aerospace applications.

These military qualified displays are designated as M87157/00101 AAX through -/00104AAX in the MIL-D-87157 Qualified Parts List (QPL). The letter designations at the end of the part numbers are defined as follows: "A" signifies MIL-D-87157 Quality Level A. "A" signifies solder dipped leads, "X" signifies the luminous intensity category.

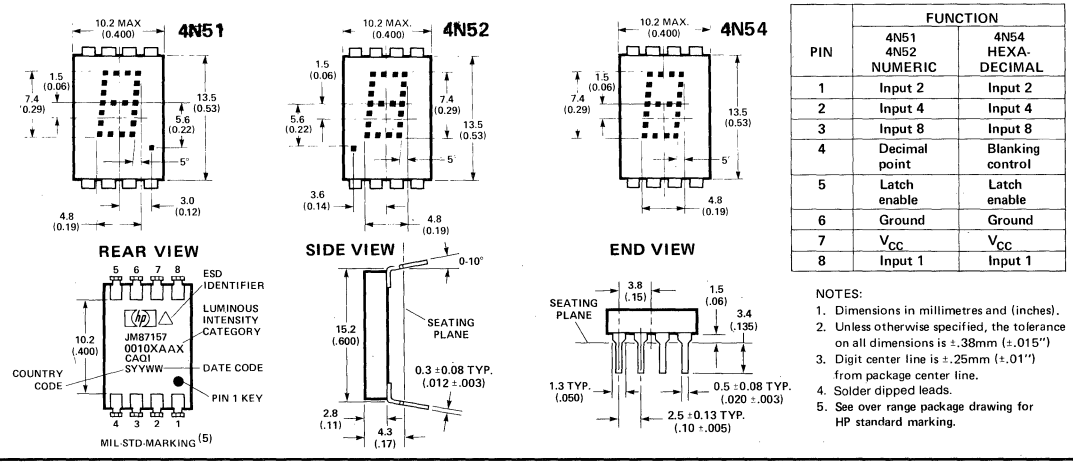
The 4N51 numeric display decodes positive 8421 BCD logic inputs into characters 0-9, a "—" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point.

The 4N52 is the same as the 4N51 except that the decimal point is located on the left-hand side of the digit.

The 4N54 hexadecimal display decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory.

The 4N53 is a "±1." overrange display, including a right-hand decimal point.

Package Dimensions*



PIN	FUNCTION	
	4N51 4N52 NUMERIC	4N54 HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38mm (±.015")
3. Digit center line is ±.25mm (±.01") from package center line.
4. Solder dipped leads.
5. See over range package drawing for HP standard marking.

*JEDEC Registered Data.

Absolute Maximum Ratings*

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1,2]	T_A	−55	+100	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	V_{CC}	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ⩽ 5 seconds			260	°C

Recommended Operating Conditions*

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1,2]	T_A	−55		+100	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics* (T_A = −55°C to +100°C, unless otherwise specified)

Description	Symbol	Test Conditions	Min.	Typ. [4]	Max.	Unit
Supply Current	I_{CC}	V_{CC} = 5.5 V (Characters		112	170	mA
Power dissipation	P_T	"5." or "B")		560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_A=25°C	40	85		μcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			50	μA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			1.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+100	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+130	μA
Peak wavelength	λ_{PEAK}	T_A=25°C		655		nm
Dominant Wavelength [8]	λ_d	T_A=25°C		640		nm
Weight**				1.0		gm
Leak Rate					$5x10^{-8}$	cc/sec

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50°C/W; Θ_{JC}=15°C/W. 2. Θ_{CA} of a mounted display should not exceed 35°C/W for operation up to T_A=+100°C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_A=25°C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship: $I_V(T_A)=I_{V(25°C)}(.985)^{[T_A-25°C]}$ 7. Applies only to 4N54. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

*JEDEC Registered Data. **Non Registered Data.

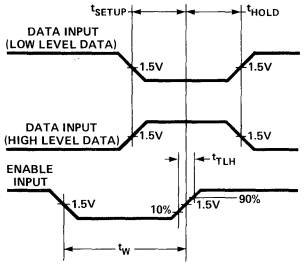


Figure 1. Timing Diagram of 4N51-4N54 Series Logic.

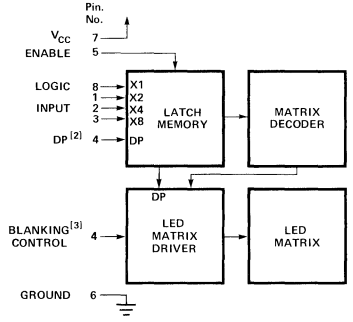


Figure 2. Block Diagram of 4N51-4N54 Series Logic.

TRUTH TABLE					
BCD DATA [1]				4N51 AND 4N52	4N54
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	-	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	....	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT. [2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE [1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING [3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

Notes:

1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 4N51 and 4N52 displays.
3. The blanking control input, B, pertains only to the 4N54 hexadecimal display. Blanking input has no effect upon display memory.

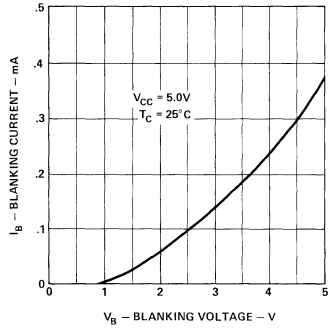


Figure 3. Typical Blanking Control Current vs. Voltage for 4N54.

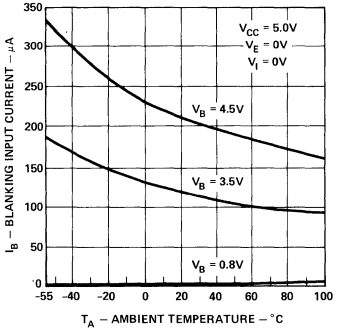


Figure 4. Typical Blanking Control Input Current vs. Ambient Temperature for 4N54.

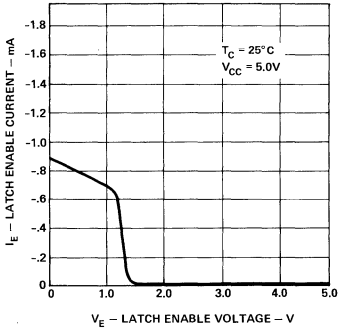


Figure 5. Typical Latch Enable Input Current vs. Voltage.

*JEDEC Registered Data.

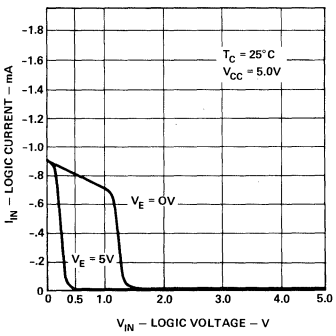


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage.

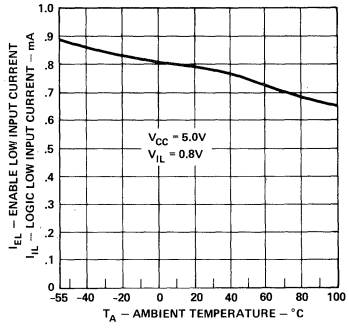


Figure 7. Typical Logic and Enable Low Input Current vs. Ambient Temperature.

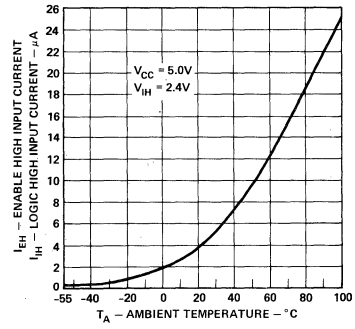


Figure 8. Typical Logic and Enable High Input Current vs. Ambient Temperature.

Operational Considerations

ELECTRICAL

The 4N51-4N54 series devices use a modified 4 x 7 dot matrix of light emitting diodes (LED's) to display decimal/hexadecimal numeric information. The LED's are driven by constant current drivers. BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. To avoid the latching of erroneous information, the enable pulse rise time should not exceed 200 nanoseconds. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7MHz rate.

The blanking control input on the 4N54 display blanks (turns off) the displayed hexadecimal information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 3.5 volts. This may be easily achieved by using an open collector TTL gate and a pull-up resistor. For example, (1/6) 7416 hexinverter buffer/driver and a 120 ohm pull-up resistor will provide sufficient drive to blank eight displays. The size of the blanking pull-up resistor may be calculated from the following formula, where N is the number of digits:

$$R_{blank} = (V_{CC} - 3.5V)/[N\ (1.0mA)]$$

The decimal point input is active low true and this data is latched into the display memory in the same fashion as the BCD data. The decimal point LED is driven by the on-board IC.

The ESD susceptibility of the IC devices is Class A of MIL-STD-883 or Class 2 of DOD-STD-1686 and DOD-HDBK-263.

MECHANICAL

4N51-4N54 series displays are hermetically tested for use in environments which require a high reliability device. These displays are designed and tested to meet a helium leak rate of 5 x 10^{-8} CC/SEC and a fluorocarbon gross leak bubble test.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54mm (0.100 inch) and the lead row spacing is 15.24mm (0.600 inch). These displays may be end stacked with 2.54mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100° C, it is important to maintain a case-to-ambient thermal resistance of less than 35° C/watt as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

PRECONDITIONING

4N51-4N54 series displays are 100% preconditioned by 24 hour storage at 125° C.

CONTRAST ENHANCEMENT

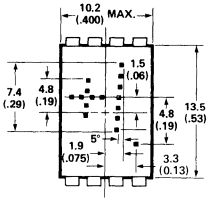
The 4N51-4N54 displays have been designed to provide the maximum posible ON/OFF contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60 and Dark Red 63, SGL Homalite H100-1605, 3M Light Control Film and Polaroid HRCP Red Circular Polarizing Filter. For further information see Hewlett-Packard Application Note 1015.

*JEDEC Registered Data.

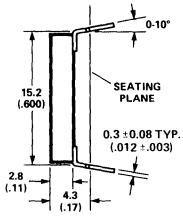
Solid State Over Range Display

For display applications requiring a ±, 1, or decimal point designation, the 4N53 over range display is available. This display module comes in the same package as the 4N51-4N54 series numeric display and is completely compatible with it.

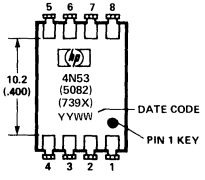
Package Dimensions*



FRONT

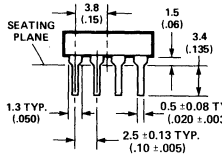


SIDE



REAR

HP STANDARD MARKING



END

NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±.38 MM (± .015 INCHES).

PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{cc}
8	Minus/Plus

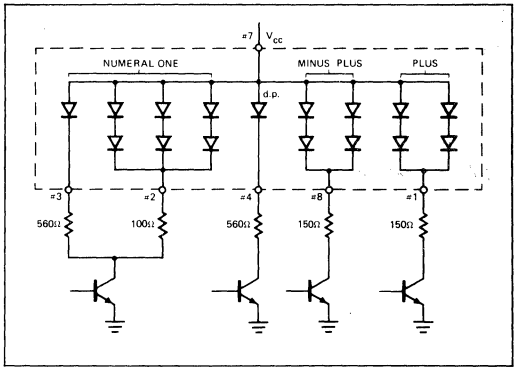


Figure 9. Typical Driving Circuit.

TRUTH TABLE

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 9 cutoff.
H: Line switching transistor in Figure 9 saturated.
X: 'Don't care'

Electrical/Optical Characteristics*

4N53 (T_A = -55°C to +100°C, Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		280	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	40	85		µcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λ_d	T_C = 25°C		640		nm
Weight * *				1.0		gm

Recommended Operating Conditions*

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 9 for recommended resistor values.

*JEDEC Registered Data. **Non Registered Data.

Absolute Maximum Ratings*

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	-65	+125	°C
Operating temperature, ambient	T_A	-55	+100	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

High Reliability Testing

Two standard reliability testing programs are available. The military program provides QPL parts that comply to MIL-D-87157 Quality Level A, per Tables I, II, IIIa, and IVa. A second program is an HP modification to the full conformance program and offers the 100% screening portion of Level A, Table I, and Group A, Table II. In addition, a MIL-D-87157 Level B equivalent testing program is available upon request.

PART MARKING SYSTEM

Standard Product	With Table I and II	With Tables I, II, IIIa and IVa
PREFERRED PART NUMBER SYSTEM		
4N51	4N51TXV	JM87157 / 00101AAX
4N52	4N52TXV	JM87157 / 00102AAX
4N54	4N54TXV	JM87157 / 00103AAX
4N53	4N53TXV	JM87157 / 00104AAX

100% Screening

TABLE I.
QUALITY LEVEL A OF MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	2072	Interpreted by HP Procedure 5956-7572-52
2. High Temperature Storage	1032	T_A = 125°C, Time = 24 hours
3. Temperature Cycling	1051	Condition B, 10 Cycles, 15 Min. Dwell
4. Constant Acceleration	2006	10,000 G's at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K
7. Interim Electrical/Optical Tests[2]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} T_A = 25°C
8. Burn-In[1, 3]	1015	Condition B at V_{CC} = 5V and cycle through logic at 1 character per second. T_A = 100°C, t = 160 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	ΔI_V = -20%, ΔI_{CC} = ± 10 mA, ΔI_{IH} = ±10μA and ΔI_{EH} = ±13 μA
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics.
3. Burn-in for the over range display shall use Condition B at a nominal I_F = 8 mA per LED, with all LEDs illuminated for t = 160 hours minimum.

TABLE II
GROUP A ELECTRICAL TESTS — MIL-D-87157

Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} and visual function, T_A = 25°C	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. T_A = +100°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. T_A = -55°C	7
Subgroup 4, 5, and 6 not applicable		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

1. Limits and conditions are per the electrical/optical characteristics.

TABLE IIIa
GROUP B, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Design Verification[1]	2075[7]		1 Device/ 0 Failures
Subgroup 2[2,3]			
Solderability	2026	T_A = 245° C for 5 seconds	LTPD = 15
Subgroup 3			
Thermal Shock (Temp. Cycle)	1051	Condition B1, 15 Min. Dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Electrical/Optical Endpoints[5]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual function. T_A = 25° C	
Subgroup 4			
Operating Life Test (340 hrs.)[6]	1027	T_A = +100° C at V_{CC} = 5.0V and cycling through logic at 1 character per second.	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3.	
Subgroup 5			
Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +125° C	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	

Notes:
1. Visual inspection performed through the display window.
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend, one cycle.
5. Limits and conditions are per the electrical/optical characteristics.
6. Burn-in for the over range display shall use Condition B at a nominal I_F = 8 mA per LED, with all LEDs illuminated for t = 160 hours minimum.
7. Equivalent to MIL-STD-883, Method 2014.

TABLE IVa
GROUP C, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7,9]			LTPD = 15
Lead Integrity	2004	Condition B2	
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual Function, $T_A = 25°C$	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			$\lambda = 10$
Operating Life Test[6]	1026	$T_A = +100°C$	
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C Life Test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.
9. Initial conditioning is a 15° inward bend, three cycles.

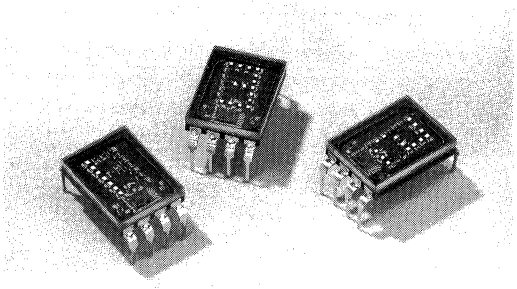
HEWLETT PACKARD

HERMETIC, NUMERIC AND HEXADECIMAL DISPLAYS FOR MILITARY APPLICATIONS

HIGH EFFICIENCY RED	
Low Power	HDSP-078X/078XTXV/078XTXVB
High Brightness	HDSP-079X/079XTXV/079XTXVB
YELLOW	HDSP-088X/088XTXV/088XTXVB
High Performance GREEN	HDSP-098X/098XTXV/098XTXVB

Features

- **CONFORM TO MIL-D-87157, QUALITY LEVEL A TEST TABLES**
- **TRUE HERMETIC PACKAGE FOR HIGH EFFICIENCY RED AND YELLOW[1]**
- **TXV AND TXVB VERSIONS AVAILABLE**
- **THREE CHARACTER OPTIONS**
  Numeric, Hexadecimal, Over Range
- **THREE COLORS**
  High Efficiency Red, Yellow,
  High Performance Green
- **4 x 7 DOT MATRIX CHARACTER**
- **HIGH EFFICIENCY RED, YELLOW, AND HIGH PERFORMANCE GREEN**
- **TWO HIGH EFFICIENCY RED OPTIONS**
  Low Power, High Brightness
- **PERFORMANCE GUARANTEED OVER TEMPERATURE**
- **HIGH TEMPERATURE STABILIZED**
- **GOLD PLATED LEADS**
- **MEMORY LATCH/DECODER/DRIVER**
  TTL Compatible
- **CATEGORIZED FOR LUMINOUS INTENSITY**



Description

These solid state displays have a 7.4 mm (0.29 inch) dot matrix character and an onboard IC with data memory latch/decoder and LED drivers in a glass/ceramic package.

The hermetic HDSP-078X,-079X/-088X displays utilize a solder glass frit seal. The HDSP-098X displays utilize an epoxy glass-to-ceramic seal. All packages conform to the hermeticity requirements of MIL-D-87157, the general specification for LED displays. These displays are designed for use in military and aerospace applications.

The numeric devices decode positive BCD logic into characters "0-9", a "—" sign, decimal point, and a test pattern. The hexadecimal devices decode positive BCD logic into 16 characters, "0-9, A-F". An input is provided on the hexadecimal devices to blank the display (all LEDs off) without losing the contents of the memory.

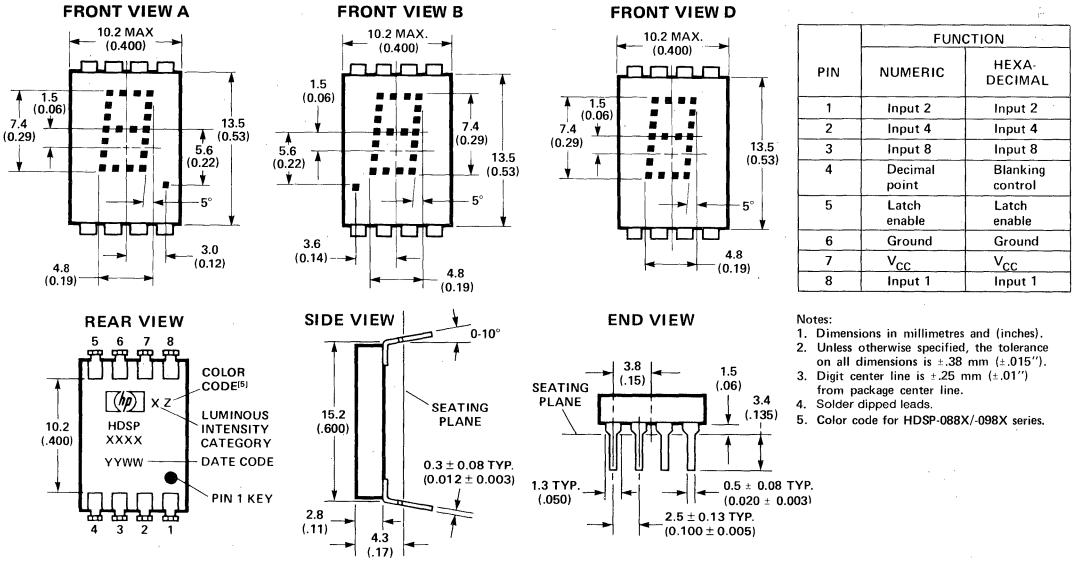
The over range device displays "±1" and right hand decimal point and is typically driven via external switching transistors.

Note:
1. The HDSP-098X high performance green displays are epoxy sealed and conform to MIL-D-87157 hermeticity requirements.

Devices

Part Number HDSP-	Color	Description	Front View
0781/0781TXV/0781TXVB	High-Efficiency Red Low Power	Numeric, Right Hand DP	A
0782/0782TXV/0782TXVB		Numeric, Left Hand DP	B
0783/0783TXV/0783TXVB		Over Range ±1	C
0784/0784TXV/0784TXVB		Hexadecimal	D
0791/0791TXV/0791TXVB	High-Efficiency Red High Brightness	Numeric, Right Hand DP	A
0792/0792TXV/0792TXVB		Numeric, Left Hand DP	B
0783/0783TXV/0783TXVB		Over Range ±1	C
0794/0794TXV/0794TXVB		Hexadecimal	D
0881/0881TXV/0881TXVB	Yellow	Numeric, Right Hand DP	A
0882/0882TXV/0882TXVB		Numeric, Left Hand DP	B
0883/0883TXV/0883TXVB		Over Range ±1	C
0884/0884TXV/0884TXVB		Hexadecimal	D
0981/0981TXV/0981TXVB	High Performance Green	Numeric, Right Hand DP	A
0982/0982TXV/0982TXVB		Numeric, Left Hand DP	B
0983/0983TXV/0983TXVB		Over Range ±1	C
0984/0984TXV/0984TXVB		Hexadecimal	D

Package Dimensions



PIN	FUNCTION	
	NUMERIC	HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

Notes:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38 mm (±.015").
3. Digit center line is ±.25 mm (±.01") from package center line.
4. Solder dipped leads.
5. Color code for HDSP-088X/-098X series.

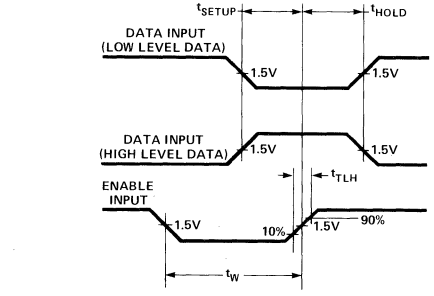


Figure 1. Timing Diagram

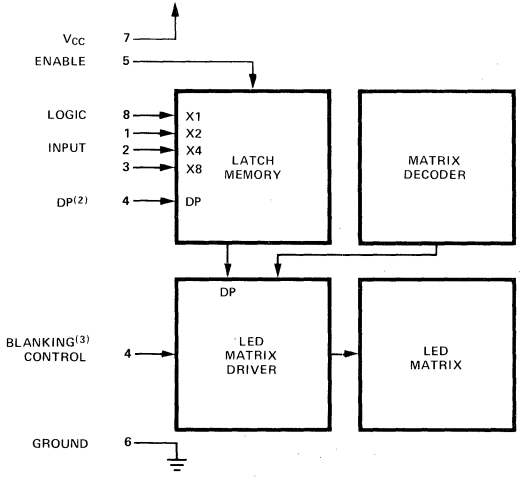


Figure 2. Logic Block Diagram

TRUTH TABLE					
BCD DATA[1]				NUMERIC	HEXA-DECIMAL
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L		A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	----	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE[1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING[3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels have no effect upon display memory, displayed character, or DP.
2. The decimal point input, DP, pertains only to the numeric displays.
3. The blanking control input, B, pertains only to the hexadecimal displays. Blanking input has no effect upon display memory.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient HDSP-078X/-079X/-088X	T_S	-65	+125	°C
HDSP-098X		-55	+100	
Operating temperature, ambient[1]	T_A	-55	+100	°C
Supply voltage[2]	V_{CC}	-0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	-0.5	V_{CC}	V
Voltage applied to blanking input[2]	V_R	-0.5	V_{CC}	V
Maximum solder temperature at 1.59 mm (0.062 inch) below seating plane: t ≤ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage [2]	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1]	T_A	-55		+100	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			1.0	msec

Optical Characteristics at T_A = 25°C, V_{CC} = 5.0V

Device	Description	Symbol	Min.	Typ.	Max.	Unit
HDSP-078X Series	Luminous Intensity per LED (Digit Average)[3,4]	I_V	65	140		μcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength[5]	λ_d		626		nm
HDSP-079X Series	Luminous Intensity per LED (Digit Average)[3,4]	I_V	260	620		μcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength[5]	λ_d		626		nm
HDSP-088X Series	Luminous Intensity per LED (Digit Average)[3,4]	I_V	215	490		μcd
	Peak Wavelength	λ_{PEAK}		583		nm
	Dominant Wavelength[5,6]	λ_d		585		nm
HDSP-098X Series	Luminous Intensity per LED (Digit Average)[3,4]	I_V	298	1100		μcd
	Peak Wavelength	λ_{PEAK}		568		nm
	Dominant Wavelength	λ_d		574		nm

Notes:
1. The nominal thermal resistance of a display mounted in a socket that is soldered onto a printed circuit board is $R\theta_{JA}$ = 50° C/W/device. The device package thermal resistance is $R\theta_{J-PIN}$ = 15° C/W/device. The thermal resistance device pin-to-ambient through the PC board should not exceed 35° C/W/device for operation at T_A = +100° C.
2. Voltage values are with respect to device ground, pin 6.
3. These displays are categorized for luminous intensity with the intensity category designated by a letter code located on the back of the display package. Case temperature of the device immediately prior to the light measurement is equal to 25° C.

Electrical Characteristics; (T_A = -55° C to +100° C)

Description		Symbol	Test Conditions	Min.	Typ.[7]	Max.	Unit
Supply Current	HDSP-078X Series	I_{CC}	V_{CC} = 5.5 V Characters "5." or "B" displayed		78	105	mA
	HDSP-079X/-088X/ -098X Series				120	175	
Power Dissipation	HDSP-078X Series	P_T	V_{CC} = 5.5 V Characters "5." or "B" displayed		390	573	mW
	HDSP-079X/-088X/ -098X Series				690	963	
Logic, Enable and Blanking Low-Level Input Voltage		V_{IL}	V_{CC} = 4.5 V			0.8	V
Logic, Enable High-Level Input Voltage		V_{IH}		2.0			V
Blanking High Voltage; Display Blanked		V_{BH}		2.3			V
Logic and Enable Low-Level Input Current		I_{IL}	V_{CC} = 5.5 V			-1.6	mA
Blanking Low-Level Input Current		I_{BL}	V_{IL} = 0.4 V			-10	μA
Logic, Enable and Blanking High-Level Input Current		I_{IH}	V_{CC} = 5.5 V V_{IH} = 2.4 V			+40	μA
Weight					1.0		gm
Leak Rate						5×10^{-8}	cc/sec.

Notes:

4. The luminous intensity at a specific operating ambient temperature, $I_V(T_A)$ may be approximated from the following expotential equation: $I_V(T_A = I_V(25° C)\, e^{[k(T_A - 25° C)]}$.

Device	K
HDSP-078X Series HDSP-079X Series	-0.0131/° C
HDSP-088X Series	-0.0112/° C
HDSP-098X Series	-0.0104/° C

5. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
6. The HDSP-088X and HDSP-098X series devices are categorized as to dominant wavelength with the category disignated by a number on the back side of the display package.
7. All typical values at V_{CC} = 5.0 V and T_A = 25° C.

Operational Considerations

ELECTRICAL

These devices use a modified 4 x 7 dot matrix of light emitting diodes to display decimal/hexadecimal numeric information. The high efficiency red and yellow displays use GaAsP/GaP LEDs and the high performance green displays use GaP/GaP LEDs. The LEDs are driven by constant current drivers, BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at 6.7 MHz rate.

The decimal point input is active low true and this data is latched into the display memory in the same fashion as the BCD data. The decimal point LED is driven by the on-board IC.

The blanking control input on the hexadecimal displays blanks (turns off) the displayed information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 2.0 volts. When blanked, the display standby power is nominally 250 mW at T_A = 25° C.

The ESD susceptibility of the IC devices is Class A of MIL-STD-883 or Class 2 of DOD-STD-1686 and DOD-HDBK-263.

MECHANICAL

These displays are hermetically sealed for use in environments that require a high reliability device. These displays are designed and tested to meet a helium leak rate of 5 x 10^{-8} cc/sec.

These displays may be mounted by soldering directly to a printed circuit board or insertion into a socket. The lead-to-lead pin spacing is 2.54 mm (0.100 inch) and the lead row spacing is 15.24 mm (0.600 inch). These displays may be end stacked with 2.54 mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100° C, it is important to maintain a base-to-ambient thermal resistance of less than 35° C watt/device as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

PRECONDITIONING

These displays are 100% preconditioned by 24 hour storage at 125°C, at 100°C for the HDSP-098X Series.

CONTRAST ENHANCEMENT

These display devices are designed to provide an optimum ON/OFF contrast when placed behind an appropriate contrast enhancement filter. The following filters are suggested:

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-088X Yellow	Panelgraphic Yellow 27 Chequers Amber 107	Polaroid HNCP 37 3M Light Control Film Panelgraphic Gray 10	Polaroid Gray HNCP10 HOYA Yellowish-Orange HLF-608-3Y Marks Gray MCP-0301-8-10
HDSP-078X/-079X HER	Panelgraphic Ruby Red 60 Chequers Red 112	Chequers Grey 105	Polaroid Gray HNCP10 HOYA Reddish-Orange HLF-608-5R Marks Gray MCP-0301-8-10 Marks Reddish-Orange MCP-0201-2-22
HDSP-098X HP Green	Panelgraphic Green 48 Chequers Green 107		Polaroid Gray HNCP10 HOYA Yellow-Green HLF-608-1G Marks Yellow-Green MCP-0101-5-12

Over Range Display

The over range devices display "±1" and decimal point. The character height and package configuration are the same as the numeric and hexadecimal devices. Character selection is obtained via external switching transistors and current limiting resistors.

Absolute Maximum Ratings

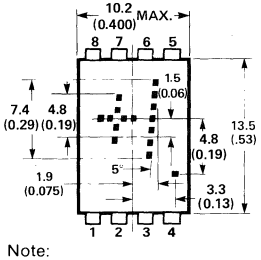
Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	-65	+125	°C
Operating Temperature Ambient	T_A	-55	+100	°C
Forward Current, Each LED	I_F		10	mA
Reverse Voltage, Each LED	V_R		5	V

Character	Pin			
	1	2,3	4	8
+	1	X	X	1
—	0	X	X	1
1	X	1	X	X
Decimal Point	X	X	1	X
Blank	0	0	0	0

Notes:
0: Line switching transistor in Figure 7 cutoff.
1: Line switching transistor in Figure 7 saturated.
X: 'don't care'

Package Dimensions

FRONT VIEW C



Pin	Function
1	Plus
2	Numeral One
3	Numeral One
4	DP.
5	Open
6	Open
7	V_{CC}
8	Minus/Plus

Note:
1. Dimensions in millimetres and (inches).

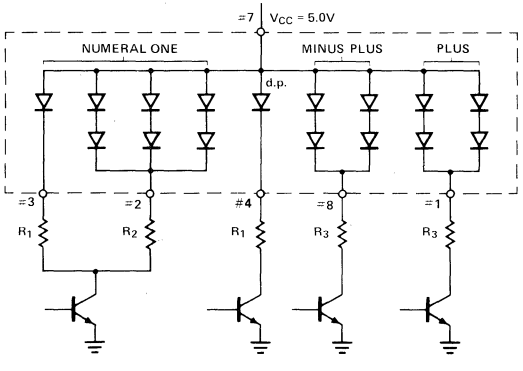


Figure 3. Typical Driving Circuit

Luminous Intensity Per LED

(Digit Average) at $T_A = 25°C$

Device	Test Conditions	Min.	Typ.	Units
HDSP-0783	$I_F = 2.8$ mA	65	140	μcd
	$I_F = 8$ mA		620	μcd
HDSP-0883	$I_F = 8$ mA	215	490	μcd
HDSP-0983	$I_F = 8$ mA	298	1100	μcd

Recommended Operating Conditions $V_{CC} = 5.0V$

Device		Forward Current Per LED, mA	Resistor Value		
			R_1	R_2	R_3
HDSP-0783	Low Power	2.8	1300	200	300
	High Brightness	8	360	47	68
HDSP-0883		8	360	36	56
HDSP-0983		8	360	30	43

Electrical Characteristics ($T_A = -55°C$ to $+100°C$)

Device	Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
HDSP-0783	Power Dissipation (all LEDs Illuminated)	P_T	$I_F = 2.8$ mA		72		mW
			$I_F = 8$ mA		224	282	
	Forward Voltage per LED	V_F	$I_F = 2.8$ mA		1.6		V
			$I_F = 8$ mA		1.75	2.2	
HDSP-0883	Power Dissipation (all LEDs Illuminated)	P_T	$I_F = 8$ mA		237	282	mW
	Forward Voltage per LED	V_F			1.90	2.2	V
HDSP-0983	Power Dissipation (all LEDs illuminated)	P_T	$I_F = 8$ mA		243	282	mW
	Forward Voltage per LED	V_F			1.85	2.2	V

High Reliability Testing

Two standard reliability testing programs are available. The TXVB program is in conformance with Quality Level A Test Tables of MIL-D-87157 for hermetically sealed displays with 100% screening tests. A TXVB product is tested to Tables I, II, IIIa, and IVa, A second program is an HP modification to the full conformance program and offers the 100% screening portion of Level A, Table I, and Group A, Table II.

PART MARKING SYSTEM

Standard Product	With Table I and II	With Tables I, II, IIIa and IVa
HDSP-078X	HDSP-078XTXV	HDSP-078XTXVB
HDSP-079X	HDSP-079XTXV	HDSP-079XTXVB
HDSP-088X	HDSP-088XTXV	HDSP-088XTXVB
HDSP-098X	HDSP-098XTXV	HDSP-098XTXVB

100% Screening **TABLE I. QUALITY LEVEL A OF MIL-D-87157**

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	2072	Interpreted by HP Procedure 5956-7572-52
2. High Temperature Storage	1032	$T_A = 125°C$, Time = 24 hours[4]
3. Temperature Cycling	1051	Condition B, 10 Cycles, 15 Min. Dwell
4. Constant Acceleration	2006	10,000 G at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K[5]
7. Interim Electrical/Optical Tests[2]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} $T_A = 25°C$
8. Burn-In[1, 3]	1015	Condition B at $V_{CC} = 5V$ and cycle through logic at 1 character per second. $T_A = 100°C$, t = 160 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	ΔI_V = -20%, $\Delta I_{CC} = \pm 10$ mA, $\Delta I_{IH} = \pm 10\mu A$ and $\Delta I_{EH} = \pm 13\ \mu A$
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics.
3. Burn-in for the over range display shall use Condition B at a nominal $I_F = 8$ mA per LED, with all LEDs illuminated for T = 160 hours minimum.
4. $T_A = +100°C$ for HDSP-098X Series.
5. Fluid temperature = +100°C for HDSP-098X Series.

TABLE II
GROUP A ELECTRICAL TESTS — MIL-D-87157

Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25° C[1]	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} and visual function, T_A = 25° C	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. T_A = +100° C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. T_A = -55° C	7
Subgroup 4, 5, and 6 not applicable		
Subgroup 7 Optical and Functional Tests at 25° C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

Notes:
1. Limits and conditions are per the electrical/optical characteristics.

TABLE IIIa
GROUP B, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Design Verification[1]	2075[7]		1 Device/ 0 Failures
Subgroup 2[2,3] Solderability	2026	T_A = 245° C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	Condition B1, 15 min. Dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K[9]	
Electrical/Optical Endpoints[5]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual function. T_A = 25° C	
Subgroup 4 Operating Life Test (340 hrs.)[6]	1027	T_A = +100° C at V_{CC} = 5.0V and cycling through logic at 1 character per second.	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3.	
Subgroup 5 Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +125°C[7,8]	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	

Notes:
1. Visual inspection performed through the display window.
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend, one cycle.
5. Limits and conditions are per the electrical/optical characteristics.
6. Burn-in for the over range display shall use Condition B at a nominal $I_F \pm 8$ mA with '+' illuminated for t = 160 hours.
7. Equivalent to MIL-STD-883, Method 2014.
8. T_A = +100°C for HDSP-098X Series.
9. Fluid temperature = +100°C for HDSP-098X Series.

TABLE IVa
GROUP C, CLASS A AND B OF MIL-D-87157

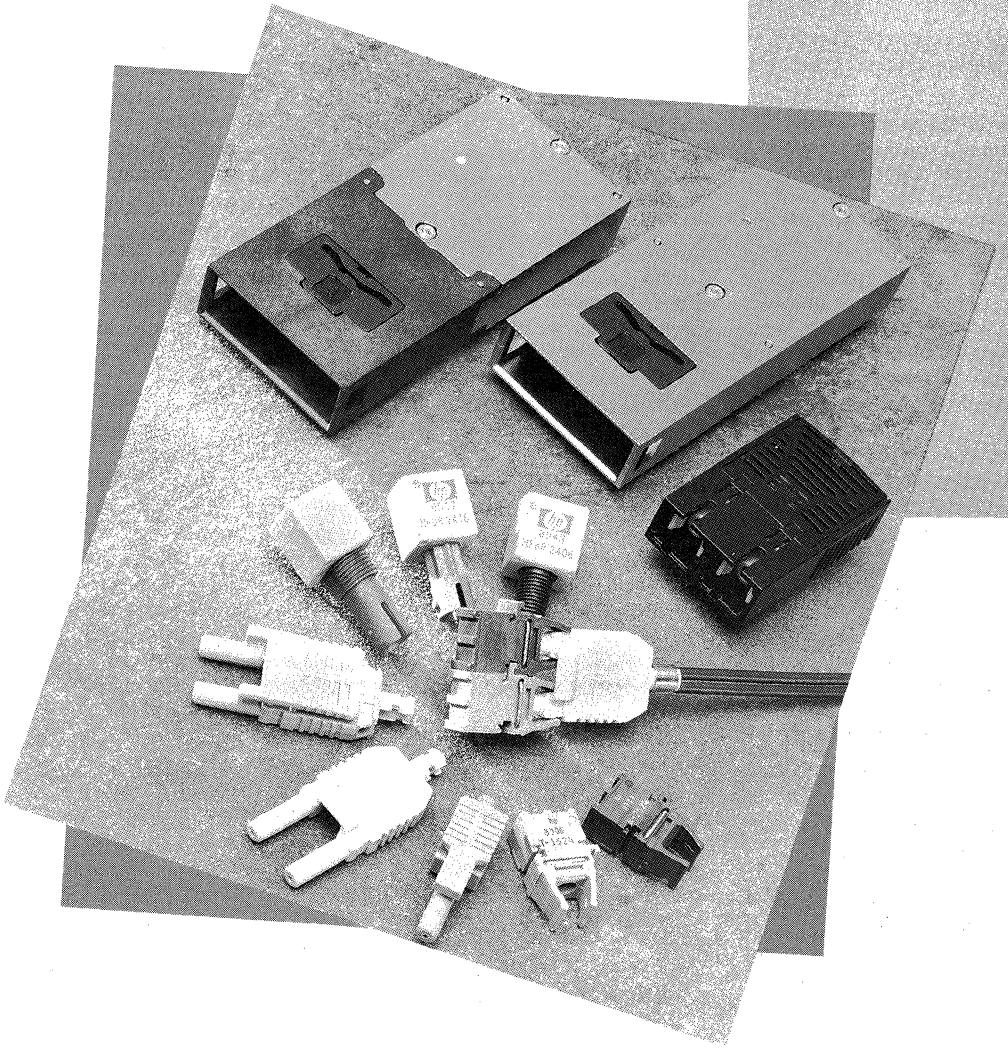
Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7,9]			LTPD = 15
Lead Integrity	2004	Condition B2	
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K[10]	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual Function, $T_A = 25°C$	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			$\lambda = 10$
Operating Life Test[6]	1026	$T_A = +100°C$	
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C Life Test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.
9. Initial conditioning is a 15° inward bend, 3 cycles.
10. Fluid temperature = +100°C for HDSP-098X Series.

HEWLETT PACKARD

Fiber Optics

- Fiber Optic Transmitter/Receiver Components
- Support ICs
- High Speed Digital Communications Products
- Cables, Connectors, and Accessories



Fiber Optics

Fiber-optic technology plays a key role in data communications today, providing a higher speed, greater distance and noise immune alternative to communication over copper wire.

HP has been in the forefront of fiber-optic communications from the beginning. We are committed to using our unique combination of high technology and high-volume manufacturing processes to meet your fiber-optic needs.

Because those needs may vary, we have developed three product families of high-quality transmitters and receivers. Each of the three families - Low Cost Miniature Link, FDDI Transceiver, and Versatile Link - was designed to provide you with the performance you need for your specific application.

NEW Product Offerings!

10Base - FL Transceiver Chip

This new support chip from HP, HFBR-4663, is a highly integrated circuit for IEEE 802.3 10Base - FL transceivers. When used with HP's Low Cost Miniature Link transmitter and receiver (HFBR-14X4, HFBR-24X6), this products ensure compliance to 10Base - FL standard with a minimum number of external components and board space.

Designed for internal or external Medium Attachment Units (MAUs), this chip offers a standard IEEE 802.3 AU interface that allows it to be directly connected to encoder/decoder chips or an AUI connector.

1300nm Fiber Optic Transmitter and Receiver

HP's new HFBR-0300 series 1300 nm transmitter and receiver are designed to provide the most cost-effective 1300 nm fiber optic links for a wide variety of data communication applications: from low speed distance extenders to FDDI and SONET OC-3 Signal Rates.

Pinouts identical to HP's Low Cost Miniature Link allow designers to easily upgrade their 820 nm links for greater distance. The optical performance of the transmitter and receiver are compatible with the specifications of the FDDI Low Cost PMD. Typical distance capabilities are 2 km at 125 MBd and 5 km at 32 MBd.

Low-Cost Miniature Link Components

HP's 820 nm HFBR-0400 Low Cost Miniature Link series is designed to provide cost-effective, high-performance fiber-optic communication links for local area networks, computers, central office switches, PBXs, and industrial control applications with link distances of up to four kilometers and data rates up to 150 MBd.

The transmitters and receivers are available in a variety of package styles and are compatible with three popular connector standards: ST®, SMA and FC. To provide you with manufacturing and design flexibility, the transmitters and receivers are auto-insertable and wave-solderable and they are specified for use with glass fiber sizes of 50/125 µm, 62.5/125 µm, 100/140 µm and 200 µm plastic clad silica.

FDDI Transceiver

HP's FDDI transceiver, is part of a growing family of 1300 nm technology fiber-optic products available from HP. The device complies with the ANSI Fiber Distributed Data Interface (FDDI) Physical Layer Medium Dependent (PMD) standard and

transmits and receives data at a rate of 100 Mbits/sec.

In addition, HP is part of a worldwide multisourcing agreement with AT&T and Siemens that defined an industry-standard 2 x 11 pinout and user-installable key. Hewlett-Packard now offers two package styles: metal or plastic Media Interface Connector Receptacles. The devices are wave-solderable and wash-compatible and a process plug is supplied with each part for this purpose.

Versatile Link Components

When it comes to the lowest-cost HP solution that's easy to design in, the choice is our 665 nm HFBR-0501 Versatile Link family. These fiber-optic links were designed for ease of use, versatility, and reliability. You get a complete family of cost-effective fiber-optic components that's ideal for solving problems associated with noisy EMI/RFI environments, voltage isolation, and data security.

Plus, the Versatile Link family provides you with guaranteed link performance over temperature at data rates up to 50 MBd and distances up to 82 meters.

The compact, low-profile transmitter and receiver packages are stackable and can be used for high-volume, low-cost assembly because they are auto-insertable and wave-solderable. A variety of connector options are available, including snapping, latching, simplex or duplex for use with 1mm plastic fiber.

Typical applications for the Versatile Link family include industrial control links, PC-to-peripheral links, local area networks, secure data transmission, and medical equipment.

SERCOS Components

Designed for European industrial environments, the Serial Realtime Communications System (SERCOS) is a standard digital interface for communication between controls and drives for numerically controlled machines. These products can also be used for industrial control data links and reduction of electromagnetic noise susceptibility.

HP's HFBR-0600 SERCOS-compatible 655 nm fiber-optic transmitters and receivers are fully compliant with the SERCOS optical specifications for transmitters and receivers and mate with SERCOS-specific SMA connectors.

The components are auto-insertable and wave-solderable, and are capable of data transmission at symbol rates from DC to over 2 MBd at typical distances of 55 meters.

High Speed Digital Communications Products

Each device type in this family was developed using one of the high performance, silicon bipolar processes available within Hewlett-Packard. The performance requirements of each device is matched to the most appropriate process. This offers a superior blend of reliability, performance, and manufacturability. Hewlett-Packard's silicon bipolar processes are capable of sub-micron dimensions, and an f_t as high as 25 GHz.

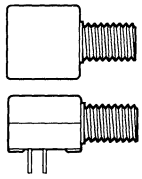
Products in this family operate at data rates as high as 2.8 Gbps, and cover many standard rates for telecom and datacom systems. Product complexity varies from basic building block ICs such as laser drivers, trans-impedance amplifier, variable gain control amplifiers, decision circuits, to that of complete gigabit rate, subsystem ICs and fiber channel interface cards.

NOTES:
1. Optical power budget calculations are typical at 25°C.
2. For Link performance with other fiber sizes, contact your local HP sales office.
3. All transmitters are LEDs except for FDDI transceiver, which includes a driver IC.
4. The Low Cost Miniature Link family is available in three package styles, compatible with SMA, ST, and FC connector styles.
5. All link distances are typical only; refer to product data sheets for minimum values.

				VERSATILE LINK					SERCOS		LOW COST MINIATURE[4]					FDDI TRANSCEIVER
				TRANSMITTERS[3]												
				λ = 665 nm HFBR-1521/1531	λ = 665 nm HFBR-1522/1532	λ = 665 nm HFBR-1524/1534	λ = 665 nm HFBR-1523/1533	λ = 665 nm HFBR-1526/1536	λ = 665 nm HFBR-1602	λ = 665 nm HFBR-1604	λ = 820 nm HFBR-14X2	λ = 820 nm HFBR-14X2	λ = 820 nm HFBR-14X4	λ = 820 nm HFBR-14X4	λ = 1300 nm HFBR-1312T	λ = 1300 nm HFBR-510X
				TYPICAL COUPLED OPTICAL POWER (dBm)												
				-11.1 @ 60 mA	-8.2 @ 60 mA	-10.3 @ 60 mA	-8.2 @ 60 mA	-12.2			-6.5 @ 60 mA	-12.0 @ 60 mA	-12.0 @ 60 mA	-16.5 @ 60 mA	-17 dBm @ 75 mA	-16.5
				FIBER SIZE (μm) (ATTENUATION)												
				1000 (0.21 dB/m)	1000 (0.21 dB/m)	1000 (0.21 dB/m)	1000 (0.21 dB/m)	1000 (0.21 dB/m)	1000 (0.21 dB/m)	1000 (0.21 dB/km)	200 PCS (5.3 dB/km)	100/140 (3.3 dB/km)	62.5/125 (2.8 dB/km)	50/125 (2.8 dB/km)	62.5/125 (2.8 dB/km)	62.5/125 (2.8 dB/km)
Versatile Link		HFBR-2521/2531	Logic IC	-21.6	5 MBd 50 m[5]											
		HFBR-2522/2532	Logic IC	-24		1 MBd 73 m[5]										
		HFBR-2524/2534	Logic IC	-20			1 MBd 43 m[5]									
		HFBR-2523/2533	Logic IC	-39				40 KBd 145 m[5]								
		HFBR-2526/2536	PIN/ Preamp	-28.7					50 MBd 65 m[5]							
SERCOS	RECEIVERS	HFBR-2602	Logic IC	SENSITIVITY (dBm)						2 MBd 55 m[5]						
		HFBR-2602	FUNCTION Logic IC													
Low Cost Miniature Link		HFBR-24X2	Logic IC	-25.4							5 MBd 3.5 Km[5]	5 MBd 4.1 Km[5]	5 MBd 4.7 Km[5]	5 MBd 3.2 Km[5]		
		HFBR-24X4	PIN/ Preamp	-36							5 MBd 5.6 Km[5]	5 MBd 7.3 Km[5]	5 MBd 8.6 Km[5]	5 MBd 7.0 Km[5]		
		HFBR-24X4	PIN/ Preamp	-33							30 MBd 600 m*[5]	30 MBd 3.0 Km*[5]	30 MBd 4.0 Km*[5]	30 MBd 4.0 Km*[5]		
		HFBR-24X6	PIN/ Preamp	-35.6							30 MBd 650 m*[5]	30 MBd 3.3 Km*[5]	30 MBd 4.5 Km*[5]	30 MBd 4.5 Km*[5]		
		HFBR-24X6	PIN/ Preamp	-32							100 MBd 130 m*[5]	100 MBd 750 m*[5]	100 MBd 1.0 Km*[5]	100 MBd 1.0 Km*[5]		
		HFBR-2316T	PIN/ Preamp												125 MBd 2.0 Km[5]	
FDDI Trans-ceiver		HFBR-510X	Logic IC	-37												125 MBd 2.0 Km[5]

*Distance is limited by a combination of fiber bandwidth, transmitter optical rise/fall time and LED spectral width.

Low Cost Miniature Link Family



Features: Dual-in-line package, operates at 820 nm, interfaces directly with ST*, SMA or FC connectors, specified for use with 50/125 μm, 62.5/1235 μm, 100/140 μm and 200 μm Plastic Coated Silica (PCS) fiber. Auto insertable, wave solderable, no mounting hardware required.

Product/Part Numbers	Description	Page No.
Evaluation Kits		5-12 thru 5-43
HFBR-0410 (ST*)	HFBR-1412 transmitter, HFBR-2412 receiver, 3 meter connectored 62.5/125 μm cable, literature.	
HFBR-0400 (SMA)	HFBR-1402 transmitter, HFBR-2402 receiver, 2 meter connectored 1,000 μm (plastic) cable, literature.	
Transmitters/Receivers		
HFBR-14X2 Standard Transmitter	Optimized for large size fiber such as 100/140 μm and 200 μm PCS	
HFBR-14X4 High Power Transmitter	Optimized for small size fiber such as 50/125 μm or 62.5/125 μm	
HFBR-24X2 5 MBd Receiver	TTL/CMOS compatible receiver with -25.4 dBm sensitivity	
HFBR-24X4 25 MHz Receiver	PIN-preamp receiver for signal rates up to 35 MBd	
HFBR-24X6 125 MHz Receiver	PIN-preamp receiver for signal rates up to 150 MBd	

Transmitter/Receiver Pairs	Optical Power Budget**	Data Rate
HFBR-14X2/24X2	20.5 dB (200 μm fiber)	5 MBd
	15 dB (100/140 μm fiber)	5 MBd
HFBR-14X4/24X2	15 dB (62.5/125 μm fiber)	5 MBd
	10.5 dB (50/125 μm fiber)	5 MBd
HFBR-14X2/24X4	18 dB (100/140 μm fiber)	5 MBd
	13.5 dB (100/140 μm fiber)	30 MBd
HFBR-14X4/24X4	18 dB (62.5/125 μm fiber)	5 MBd
	13.5 dB (62.5/125 μm fiber)	30 MBd
HFBR-14X2/24X6	21 dB (100/140 μm fiber)	30 MBd
	19 dB (100/140 μm fiber)	150 MBd
HFBR-14X4/24X6	21 dB (62.5/125 μm fiber)	30 MBd
	19 dB (62.5/125 μm fiber)	150 BMd

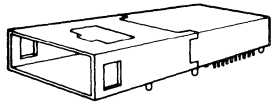
*ST (R) is a registered trademark of AT&T for Lightwave Cable Connectors.
**Link performance at 25°C.

Low Cost Miniature Link Family (cont.)

Product/Part Numbers	Description	Page No.
Mechanical Styles		5-12 thru 5-43
HFBR-XX0X	SMA housed product	
HFBR-XX3X	SMA port product, bent leads	
HFBR-XX5X	SMA port product, straight leads	
HFBR-XX0XC	HFBR-XX0X with SMA Conductive Port Option (RX only)	
HFBR-XX3XC	HFBR-XX3X with SMA Conductive Port Option (RX only)	
HFBR-XX5XC	HFBR-XX5X with SMA Conductive Port Option (RX only)	
HFBR-XX1X	ST* housed product	
HFBR-XX4X	ST* port product, bent leads	
HFBR-XX6X	ST* port product, straight leads	
HFBR-XX1XT	HFBR-XX1X with Threaded ST* Option	
HFBR-XX4XT	HFBR-XX4X with Threaded ST* Option	
HFBR-XX6XT	HFBR-XX6X with Threaded ST* Option	
HFBR-XX2X	FC housed product	

*ST (R) is a registered trademark of AT&T for Lightwave Cable Connectors.
**Link performance at 25°C.

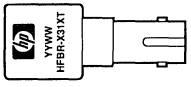
FDDI Transceiver



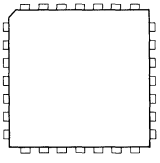
Features: Fully compliant with FDDI PMD standard. Industry standard, multi-sourced 2 rows of 11 pin package. User selectable keying. Dual-in-line package, interface directly with FDDI MIC connector. Specified for use with both 62.5/125 μm and 50/125 μm fiber. Single +5 V power supply and shifted ECL logic interface. Now offered in two package options; metal MIC receptacle (HFBR-5101) and plastic MIC receptacle (HFBR-5102).

Product/Part Numbers		Description		Page No.
Transceiver		**Distance**	**Data Rate**	5-67
FDDI link	HFBR-5101 (Metal MIC)	2 km	125 MBd	
	New HFBR-5102 (Plastic MIC)	2 km	125 MBd	

1300 nm Fiber Optic Transmitter and Receiver

Product/Part Numbers	Description	Page No.
 New HFBR-1312T – Transmitter New HFBR-2316T – Receiver	**Features:** Dual-in-line package, operates at 1300 nm wavelength, interfaces directly with ST* connectors, specified for use with 50/125 µm and 62.5/125 µm fiber. Typical distance capabilities are 2 km at 125 MBd and 5 km at 32 MBd.	5-59

10Base-FL Transceiver Chip

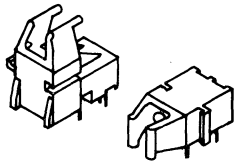
Product/Part Numbers	Description	Page No.
 New HFBR-4663 – Support IC	**Features:** Single chip solution for 10Base-FL internal or external MAUs, directly compatible with HFBR-14X4 and HFBR-24X6 fiber optic transmitters and receivers, incorporates an AU interface.	5-44

ST and SMA Connectored Cable*

	Description							
	Fiber Size			Connector Style		Cable Type		
Part Number	100/ 140/0.30	62.5/ 125/0.275	50/ 125/0.18	SMA	ST*	Single Channel	Dual Channel	Page No.
HFBR-AWSyyy	X			X		X		5-148
HFBR-AWDyyy	X			X			X	
HFBR-AXSyyy	X				X	X		
HFBR-AXDyyy	X				X		X	
HFBR-BWSyyy		X		X		X		
HFBR-BWDyyy		X		X			X	
HFBR-BXSyyy		X			X	X		
HFBR-BXDyyy		X			X		X	
HFBR-CXSyyy			X		X	X		

*ST (R) is a registered trademark of AT&T for Lightwave Cable Connectors.
**Note: All cable assemblies except for HFBR-CXSyyy are available in 1 metre increments from 1 metre to 10 metres and 5 metre increments from 25 m to 50 m. HFBR-CXSyyy is available in 1 and 10 metre lengths only. Eg. yyy = 050 designates 50 metres and yyy = 005 designates 5 m.

Versatile Link Family



Features: Dual-in-line package, horizontal and vertical PCB mounting, plastic snap-in connectors, specified for 1 mm dia. plastic fiber. TTL/CMOS compatible output, auto insertable, wave solderable.

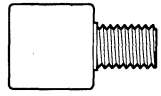
Product/Part Numbers			Description		Page No.
Evaluation Kit HFBR-0501			HFBR-1524 Transmitter. HFBR-2524 Receiver. 5 metre connectored cable, connectors, bulkhead feedthrough adapter, polishing kit, literature.		5-98
Transmitter/Receiver Pairs					
	Horizontal	**Vertical**	**Distance***	**Data Rate**	
50 MBd High Speed Link	HFBR-1526/2526	HFBR-1536/2536	65 m	50 mBd	
5 MBd High Performance Link	HFBR-1521/2521	HFBR-1531/2531	50 m	5 MBd	
1 MBd High Performance Link	HFBR-1522/2522	HFBR-1532/2532	73 m	1 MBd	
1 MBd Standard Performance Link	HFBR-1524/2524	HFBR-1534/2534	43 m	1 MBd	
40 KBd Extended Distance Link	HFBR-1523/2523	HFBR-1533/2533	145 m	40 KBd	
Low Current Link	HFBR-1523/2523	HFBR-1533/2523	45 m	40 KBd	
Photo Interrupter Link	HFBR-1523/2523	HFBR-1533/2523	N.A.	20 KHz	
	HFBR-1522/2522	HFBR-1532/2532	N.A.	500 KHz	
Plastic Fiber Cable Available in various lengths (yyy m)					
Attenuation	**Simplex**	**Duplex**			
Standard	HFBR-RUSyyy	HFBR-RUDyyy	Unconnectored cable		
Standard	HFBR-RNSyyy	HFBR-RNDyyy	Cable with simplex connectors		
Standard	HFBR-RLSyyy	HFBR-RLDyyy	Cable with latching simplex connectors		
Standard	N.A.	HFBR-RMDyyy	Duplex connectored cable		
Standard	N.A.	HFBR-RTDyyy	Latching duplex connectored cable		
Extra Low Loss	HFBR-EUSyyy	HFBR-EUDyyy	Unconnectored cable		
Extra Low Loss	HFBR-ENSyyy	HFBR-ENDyyy	Cable with simplex connectors		
EXtra Low Loss	HFBR-ELSyyy	HFBR-ELDyyy	Cable with latching simplex connectors		
Extra Low Loss	N.A.	HFBR-EMDyyy	Duplex connectored cable		
Extra Low Loss	N.A.	HFBR-ETDyyy	Latching duplex connectored cable		
Connectors					
	Simplex Standard	HFBR-4501	Gray connector/crimp ring		
		HFBR-4511	Blue connector/crimp ring		
	Simplex Latching	HFBR-4503	Gray connector/crimp ring		
		HFBR-4513	Blue connector/crimp ring		
	Duplex Standard	HFBR-4506	Parchment connector/crimp ring		
	Duplex Latching	HFBR-4516	Gray connector/crimp ring		

Versatile Link Family (cont.)

Product/Part Numbers		Description	Page No.
Polishing Kit			
	HFBR-4593	Plastic polishing fixture (used for all connectors), abrasive paper, lapping film.	5-98
Bulkhead Feedthrough In-Line Splice			
	HFBR-4505	Gray bulkhead feedthrough adapter, simplex	
	HFBR-4515	Blue bulkhead feedthrough adapter, simplex	

*Link performance at 25°C, improved attenuation cable.

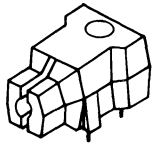
SERCOS Family



Features: Dual-in-line package, fully compliant to SERCOS optical specifications, optimized for 1000 μm plastic optical fiber, compatible with SMA connectors, auto-insertable and wave-solderable.

Product/Part Numbers		Description		Page No.
Transmitter/Receiver Pairs				5-142
		Distance (Typ.)	**Data Rate**	
Standard Link	HFBR-1602/2602	55 m	2 MBd	
Extended Distance Link	HFBR-1604/2602	66 m	2 MBd	
Evaluation Cable HFBR-RWS002		Two meter SMA 1000 μm plastic fiber optic cable.		5-143

Snap-In Family



Features: Operate with 1 mm dia. plastic fiber, plastic snap-in connector compatible (standard simplex only). TTL compatible output.

FOR NEW DESIGNS: Refer to the Versatile Link Family on page 5-8 to achieve the best price-performance value.

Product/Part Numbers		Description		Page No.
Transmitter/Receiver Pairs		**Distance***	**Data Rate***	5-82
5 MBd Link	HFBR-1510/-2501	40 metre	5 MBd	
1 MBd Link	HFBR-1502/-2502	65 metre	1 MBd	
Extended Distance Link	HFBR-1512/-2503	125 metre	40 kBd	
Low Current Link	HFBR-1512/-2503	40 metre	40 kHz	
Photo Interrupter Link	HFBR-1512/-2503	N/A	20 kHz	
	HFBR-1502/-2502	N/A	500 kHz	

*Link performance at 25°C, improved attenuation cable.

High Speed Digital Communications

Variable Gain Control Amplifiers (Typical Specifications at +25°C Case Temperature)

Part Number	$G_{P\,@}$ (dB)	Gain Control Range (dB)	3 dB Bandwidth (GHz)	P_{1dB} @ 0.5 GHz	Supply Voltage (V)	Device Current (mA)	Package	Page
HPVA-0180	21 @ 0.3 GHz	20 @ 0.3 GHz	2.5	-3	6	41	SO-8 SM plastic	5-224

Transimpedance Amplifiers (Typical Specifications at +25°C Case Temperature)

Part Number	Data Rate (Gb/s)	Bandwidth (GHz)	Gain (W)	Input Current Noise (pA/√Hz)	Supply Voltage (V)	Device Current (mA)	Package	Page
ITA-06300	1.5	1.5	2800	3.5	5	34	chip	5-240
ITA-12300	0.8	0.9	4200	2.8	5	43	chip	5-236
ITA-06318	1.5	1.3	2800	3.5	5	34	180 mil SM	5-242
ITA-12318	0.8	0.75	4200	2.8	5	43	180 mil SM	5-236

Decision Circuits (Typical Specifications at +25°C Ambient Temperature)

Part Number	Maximum Rate (Gb/s)	Amplitude Margin (mV)	Phase Margin (ps)	Data Input Amplitude (mVp-p)	t_r (ps)	t_f (ps)	Package	Page
HDMP-2003	2.0	115	370	—	120	90	HBIC-0.5" SM	5-181
HDMP-2004	2.8	90	190	—	120	90	HBIC-0.5" SM	
HDMP-2006	1.5	130	800	—	200	200	SOIC-8 SM hermetic	5-192
IDC-51418	1.5	—	620	20	200	190	180 mil SM	5-234

Data and Clock Recovery Circuit (Typical Specifications at +25°C Ambient Temperature)

Part Number	Data Rate (Mb/s)	Lock Time (ms)	Clock & Data Rise & Fall Time (ps)	Jitter Generation (per rms)	Clock Output Voltage (V)	Data Output Voltage (V)	Package	Page
HDMP-2501	600-650	2.3	200	7.5	0.7	0.7	F6 16 lead herrmetic	5-200

High Speed Digital Communications (cont.)

Laser Driver (Typical Specifications at +25°C Ambient Temperature)

Part Number	Data Rate (Gb/s)	Bandwidth (GHz)	Prebias Current (mA)	Modulation Current (mA)	Input VSWR	Supply Voltage (V)	Package	Page
IDA-07318	1.5	1.0	0-50	5-50	2:1	$^{-}$5 or $^{-}$5.2	180 mil SM	5-232

Gigabit Rate Transmit Receive Chip Set

Part Number	Description	Package	Page
HDMP-1000*	Transmitter Receiver Chip set, Parallel data (16, 17, 20, or 21 bits wide) is loaded into the Tx and delivered to the Rx over optical fiber or coax cable. Contains encoding, mux, clock extraction, demux, and decoding.	ceramic quad flat pack (CQFP)	5-151
HDMP-100K	Gigabit Rate Transmit Receive Chipset Evaluation Board. Evaluation board; literature.		5-180

*HDMP-1000 is the Tx/Rx pair. The transmitter chip can be ordered separately as the HDMP-1002; the receiver as the HDMP-1004.

Fiber Channel Optical Link Card

Part Number	Data Rate (Mbaud/s)	Wavelength λ (nm)	Description	Page
HOLC-0266	266	780	Transmitter/Receiver card which implements the emerging ANSI X3T9.3 Fiber Channel Standard (FC-O layer). Contains all functions necessary for sending 10-bit wide encoded data serially. SC connectors.	5-209
HOLC-K266	266	780	Evaluation kit. Two HOLC-0266 cards; 4m SC duplex 50/125 μm cable; electrical connectors; literature.	5-223

HEWLETT PACKARD

Low Cost, Miniature Fiber Optic Components with ST*, SMA and FC Ports

Technical Data

HFBR-0400 ST*, SMA and FC Series

Features

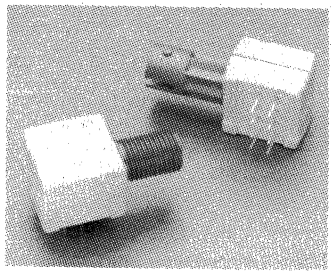
- **Low Cost Transmitters and Receivers**
- **Choice of ST, SMA or FC Ports**
- **820 Nanometre Wavelength Technology**
- **Signal Rates up to 155 Megabaud**
- **Link Distances up to 4 Kilometres**
- **Specified with 50/125 μm, 62.5/125 μm, 100/140μm, and 200 μm PCS Fiber Sizes**
- **Repeatable ST Connections within 0.2 dB Typical**
- **Unique Optical Port Design for Efficient Coupling**
- **Auto-Insertable and Wave Solderable**
- **No Board Mounting Hardware Required**
- **Wide Operating Temperature Range – –40°C to 85°C**
- **AlGaAs Emitters 100% Burn-In Ensures High Reliability**
- **Demonstrated Reliability @ 40°C Exceeds 4 Million Hours MTBF**
- **Conductive Port Option with the SMA and ST Threaded Port Styles**

Applications

- **Local Area Networks**
- **Computer to Peripheral Links**
- **Computer Monitor Links**
- **Digital Cross Connect Links**
- **Central Office Switch/PBX Links**
- **Video Links**
- **Modems and Multiplexers**
- **Suitable for Tempest Systems**
- **Industrial Control Links**

Description

The HFBR-0400 Series of components is designed to provide cost effective, high performance fiber optic communication links for information systems and industrial applications with link distances of up to 4 kilometres. With the HFBR-24X6, the 125 MHz analog receiver, data rates of up to 155 megabaud are attainable.



Transmitters and receivers are directly compatible with popular "industry-standard" connectors: ST, SMA and FC. They are completely specified with multiple fiber sizes; including 50/125 μm, 62.5/125 μm, 100/140 μm, and 200 μm.

Complete evaluation kits are available for ST and SMA product offerings; including transmitter, receiver, connectored cable, and technical literature. In addition, ST and SMA connectored cables are available.

*ST is a registered trademark of AT&T Lightguide Cable Connectors.

HFBR-0400 Series Selection Guide

HFBR-X4XXaa

1 = Transmitter
2 = Receiver

4 = 820 nm Transmitter and Receiver Products

0 = SMA, Housed
1 = ST, Housed
2 = FC, Housed
3 = SMA Port, 90 deg. Bent Leads
4 = ST Port, 90 deg. Bent Leads
5 = SMA Port, Straight Leads
6 = ST Port, Straight Leads

T = Threaded ST Port
C = SMA, Conductive Port (Rx only)
TC = Threaded ST, Conductive Port (Rx only)

2 = Tx, Standard Power
4 = Tx, High Power
2 = Rx, 5 MBd, TTL Output
4 = Rx, 25 MHz, Analog Output
6 = Rx, 125 MHz, Analog Output

HFBR-0400 Series Evaluation Kit Selection Guide

Data Rate Capability	SMA Ports	ST Ports
DC to 5 MBd	HFBR-0400	HFBR-0410
2 to 70 MBd		HFBR-0414

Literature Guide

Title	Description
HFBR-0400 Series Reliability Data	Transmitter & Receiver Reliability Data
Application Bulletin 73	Low-Cost Fiber Optic Transmitter & Receiver Interface Circuits
Application Bulletin 78	Low Cost Fiber Optic Links for Digital Applications up to 150 MBd
Application Note 1038	Low-Cost Components for IEEE 802.3 Fiber Optic Inter-Repeater Links
Technical Brief 105	ST Connector/Cable Guide
Technical Brief 101	Fiber Optic SMA Connector Technology
HFBR-0400 ST and SMA Series	Transmitter & Receiver Specifications

Contact your local HP components sales office to obtain these publications.

Package Information

All HFBR-0400 Series transmitters and receivers are housed in a low-cost, dual-in-line package that is made of high strength, heat resistant, chemically resistant, and UL V-O flame retardant plastic. The transmitters are easily identified by the light grey color connector port. The receivers are easily identified by the dark grey color connector port. (Black color for conductive port.) The package is designed for auto-insertion and wave soldering so it is ideal for high volume production applications.

Handling and Design Information

When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean. Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol on a cotton swab also works well.

CAUTION: The small junction sizes inherent to the design of these components increases the components' susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of these components to prevent damage and/or degradation which may be induced by ESD.

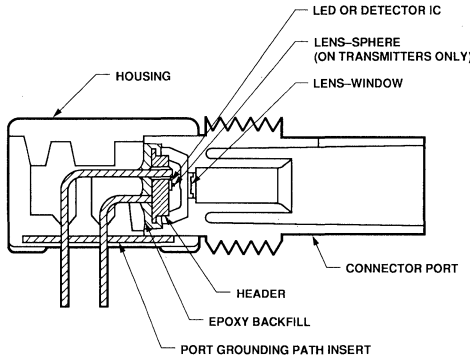


Figure 1. HFBR-0400 ST Series Cross-Sectional View

Link Design Considerations

The HFBR-14XX transmitter and the HFBR-24XX receiver can be used to design fiber optic data links that operate with 50/125 µm, 62.5/125 µm, 100/140 µm and 200 µm PCS fiber cables.

The HFBR-14X2 standard transmitter and the HFBR-24X2 receiver are suitable for systems requiring up to 5 MBd and 2 Km. For higher data rate or longer distance, the HFBR-14X4 high power transmitter and/or the HFBR-24X4 receiver should be considered.

5 MBd Logic Link Design

The HFBR-14X4/24X2 Logic Link is guaranteed to work with 62.5/125 µm fiber optic cable over the entire range of 0 to 1200 metres at a data rate of dc to 5 MBd, with arbitrary data format and typically less than 25% pulse width distortion, when the transmitter is driven with I_F = 30 mA, R_L = 115 Ohm as shown in Figure 2. If it is desired to economize on power or achieve lower pulse distortion, then a lower drive current (I_F) may be used. The following example will illustrate the technique for optimizing I_F.

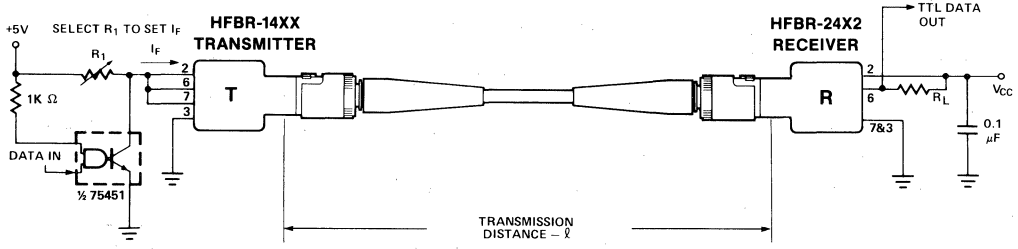
Example: Maximum distance required = 400 metres. From Figure 3 the drive current should be 15 mA. From the transmitter data V_F = 1.5 V (max.) as shown in Figure 9.

$$R_1 = \frac{V_{CC} - V_F}{I_F} = \frac{5\text{ V} - 1.5\text{ V}}{15\text{ mA}}$$

$$= 233 \text{ ohm}$$

The curves in Figures 3, 4, and 5 are constructed assuming no in-line splice or any additional system loss. Should the link consist of any in-line splices, these curves can still be used to calculate link limits provided they are shifted by the additional system loss in dB. For example, with 20 mA of transmitter drive current, 1.6 km link distance is achievable. With 2 dB of additional system loss, 1.2 km link distance is achievable.

5 MBd Link Performance



NOTE:
IT IS ESSENTIAL THAT A BYPASS CAPACITOR (0.01 µF TO 0.1 µF CERAMIC) BE CONNECTED FROM PIN 2 TO PIN 7 OF THE RECEIVER. TOTAL LEAD LENGTH BETWEEN BOTH ENDS OF THE CAPACITOR AND THE PINS SHOULD NOT EXCEED 20 mm.

Figure 2. Typical Circuit Configuration

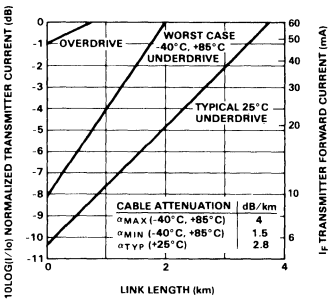


Figure 3. HFBR-1414/HFBR-2412 Link Design Limits with 62.5/125 µm Cable

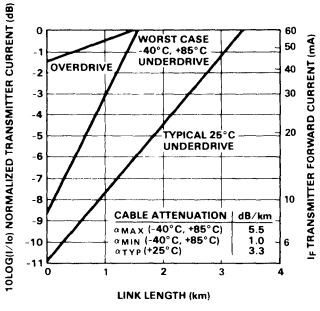


Figure 4. HFBR-14X2/HFBR-24X2 Link Design Limits with 100/140µm Cable

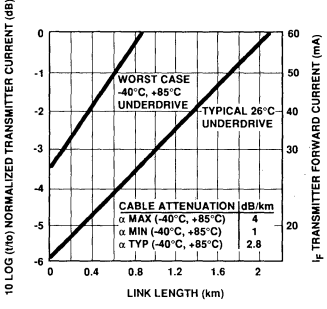


Figure 5. HFBR-14X4/HFBR-24X2 Link Design Limits with 50/125 µm Cable

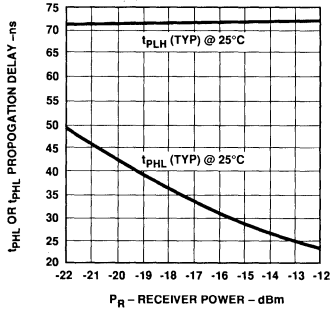


Figure 6. Propagation Delay through System with One Metre of Cable

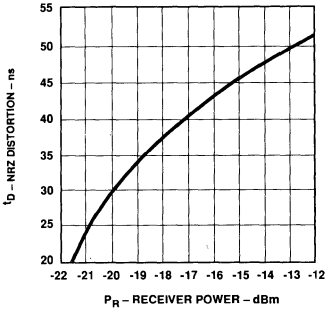


Figure 7. Typical Distortion of NRZ EYE-pattern with Pseudo Random Data at 5 Mb/s (see Note 2)

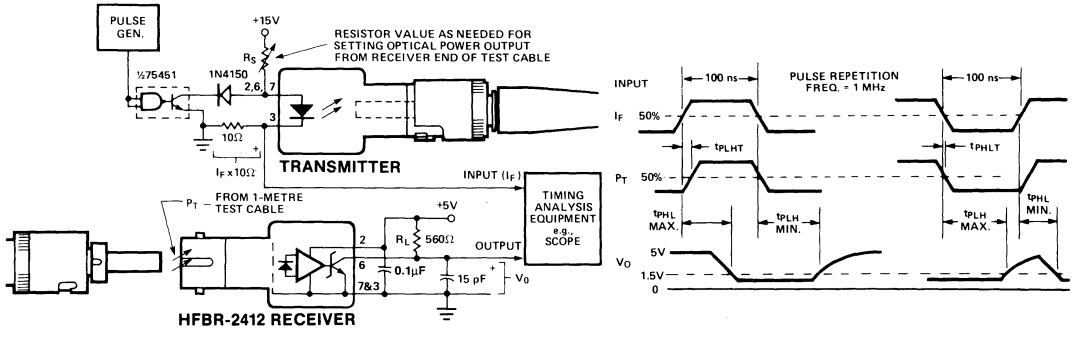


Figure 8. System Propagation Delay Test Circuit and Waveform Timing Definitions

Logic Link Design up to 35 MBd

For data rates up to 35 MBd, or longer distance, the HFBR-14X4 high power transmitter and/or the HFBR-24X4 receiver can be used. The table on the following page summarizes the typical performance of a 30 MBd link. For more details, please refer to HP Application Bulletin 73 (5954-8415). For design assistance for Ethernet applications, refer to HP Application Note 1038 (5954-2215). If circuit design assistance is needed, please contact your local Hewlett-Packard Components Field Sales Engineer.

Logic Link Design up to 155 MBd

For data rates of up to 155 MBd, the HFBR-14X4 transmitter and the HFBR-24X6 receiver can be used. The table on the following page summarizes the typical performance of a 100 MBd link. For more details, please refer to HP Application Bulletin 78. If circuit design assistance is needed, please contact your local Hewlett-Packard Components Field Sales Engineer.

Cable Selection

The HFBR-0400 Series can be used with fiber sizes such as 50/125 μm, 62.5/125 μm, 100/140 μm, 200 μm PCS, and 1000 μm Plastic. Before selecting a fiber type, several parameters need to be carefully evaluated.

The bandwidth and attenuation (dB/km) of the selected fiber, in conjunction with the amount of optical power coupled into it will determine the achievable link length. The parameters that will significantly affect the optical power coupled into the fiber are as follows:

a. Fiber Core Diameter. As the core diameter is increased, the optical power coupled increases, leveling off at about 250 μm diameter.

b. Numerical Aperture (NA). As the NA is increased, the optical power coupled increases, leveling off at an NA of about 0.34.

In addition to the optical parameters, the environmental performance of the selected fiber/cable must be evaluated. Finally, the ease of installing connectors on the selected fiber/cable must be considered.

ST connectored fiber optic cable is available from a variety of manufacturers and distributors, including those listed in HP Technical Brief 105; ST Connector/Cable Guide. For ST Evaluation Cables from Hewlett-Packard, please refer to page 00.

ST Connectors

ST connections are locking, vibration resistant, low loss and very repeatable. The HFBR-0400 ST Series Transmitters and Receivers are compatible with ST type connectors from a variety of manufacturers and distributors. For more information about ST Connectors, please refer to Technical Brief 105; ST Connector/Cable Guide.

SMA Connectors

The HFBR-0400 SMA Series Transmitters and Receivers are compatible with SMA type connectors. Depending upon the type of SMA connector that is chosen, price, performance, and reliability will vary. For more information about SMA connectors, please refer to Technical Brief 101; Fiber Optic SMA Connector Technology.

5 MBd Link Performance –40°C to +85°C unless otherwise specified

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions	Reference
Optical Power Budget w/50/125 µm Fiber	OPB_{50}	4.2	9.6		dB	HFBR-14X4/24X2 w/50/125 µm, NA = 0.2	
Optical Power Budget w/62.5/125 µm Fiber	$OPB_{62.5}$	8.0	15.0		dB	HFBR-14X4/24X2 w/62.5/125 µm, NA = 0.27	
Optical Power Budget w/100/140 µm Fiber	OPB_{100}	8.5	15.0		dB	HFBR-14X2/24X2 w/100/140 µm, NA = 0.30	
Optical Power Budget w/200 µm PCS Fiber	OPB_{200}	13	20.5		dB	HFBR-14X2/24X2 w/200 µm PCS, NA = 0.40	
Data Rate Synchronous		dc		5	MBaud		Note 2
Asynchronous		dc		2.5	MBaud		Note 2, Fig. 7
Propagation Delay LOW to HIGH	t_{PLH}		72		nsec	T_A = 25°C P_R = –21 dBm Peak	Fig. 6, 7, 8
Propagation Delay HIGH to LOW	t_{PHL}		46		nsec		
System Pulse Width Distortion	t_{PLH}-t_{PHL}		26		nsec	= 1.0 metre	
Bit Error Rate	BER			10^{-9}		Data Rate ≤ 5 MBaud P_R > –24 dBm Peak	

Notes:
1. Typical data at T = 25°C, V_{CC} = 5.0 V dc, P_R = 27.0 dBm.
2. Synchronous data rate limit is based on these assumptions: a) 50% duty factor modulation, e.g., Manchester I or BiPhase Manchester II; b) continuous data; c) PLL Phase Lock Loop demodulation; d) TTL threshold.

   Asynchronous data rate limit is based on these assumptions: a) NRZ data; b) arbitrary timing—no duty factor restriction; c) TTL threshold.

   The EYE pattern describes the timing range within which there is no uncertainty of the logic state, relative to a specific threshold, due to either noise or intersymbol prop. delay effects.

30 MBd Link Performance (see Application Bulletin 73 for details)

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions
Optical Power Budget w/50/125 µm Fiber	OPB_{50}		9.7		dB	HFBR-14X4/24X4 w/50/125 µm, NA = 0.2
Optical Power Budget w/62.5/125 µm Fiber	$OPB_{62.5}$		13.5		dB	HFBR-14X4/24X4 w/62.5/125 µm, NA = 0.27
Optical Power Budget w/100/140 µm Fiber	OPB_{100}		13.5		dB	HFBR-14X2/24X4 w/100/140 µm, NA = 0.30
Optical Power Budget w/200 µm PCS Fiber	OPB_{200}		19		dB	HFBR-14X4/24X4 w/200 µm PCS, NA = 0.40
Data Format NRZ		dc	30		MBaud	Reference AB 73 for circuit details, Note 2, 3
Propagation Delay LOW to HIGH	t_{PLH}		12		nsec	T_A = 25°C P_R = –13 dBm Peak
Propagation Delay HIGH to LOW	t_{PHL}		8		nsec	
System Pulse Width Distortion	t_{PLH}-t_{PHL}		4		nsec	= 1.0 metre
Bit Error Rate	BER			10^{-9}		Data Rate ≤ 30 MBaud P_R > –25.5 dBm Peak

Notes:
1. Typical data at T = 25°C, V_{CC} = 5.0 V dc.
2. This circuit utilizes the LT1016 comparator from Linear Technology Corporation. If operated at 5 MBd, an additional 4.5 dB of optical power budget can be obtained.
3. If HFBR-24X4 is replaced with the HFBR-24X6, an additional 5.5 dB of optical power budget can be obtained at 30 MHz NRZ.

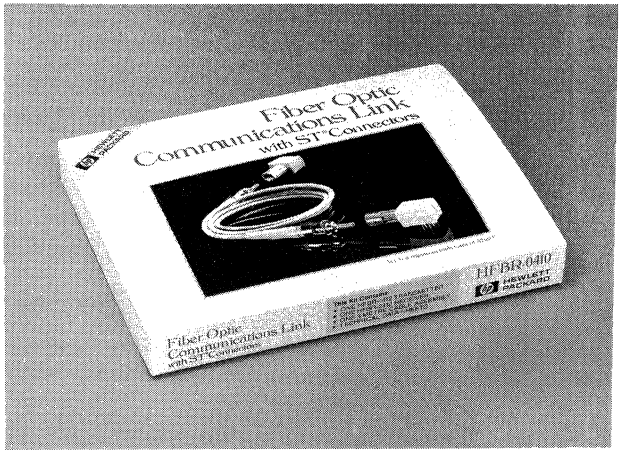
100 MBd Link Performance (see Application Bulletin 78 for details)

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions
Optical Power Budget w/50/125 µm Fiber	OPB_{50}		14.7		dB	HFBR-14X4/24X6 w/50/125 µm, NA = 0.2
Optical Power Budget w/62.5/125 µm Fiber	$OPB_{62.5}$		19		dB	HFBR-14X4/24X6 w/62.5/125 µm, NA = 0.27
Optical Power Budget w/100/140 µm Fiber	OPB_{100}		19		dB	HFBR-14X2/24X6 w/100/140 µm, NA = 0.30
Optical Power Budget w/200 µm PCS Fiber	OPB_{200}		24		dB	HFBR-14X2/24X6 w/200 µm PCS, NA = 0.40
Data Format 20% to 80% Duty Factor			100		MBaud	Reference AB 78 for circuit details, Note 2
Propagation Delay LOW to HIGH	t_{PLH}		5		nsec	T_A = 25°C P_R = –7 dBm Peak
Propagation Delay HIGH to LOW	t_{PHL}		4		nsec	
System Pulse Width Distortion	t_{PLH}-t_{PHL}		1		nsec	= 1.0 metre
Bit Error Rate	BER			10^{-9}		Data Rate ≤ 100 MBaud P_R > –31 dBm Peak

Notes:
1. Typical data at T_A = 25°C, V_{EE} = –5.2 V dc, V_{CC} = 0 (ECL).
2. The optical power budgets at 100 MBd were measured with an unrestricted receiver, without a Nyquist filter. A 10116 ECL line receiver was used in the receiver digitizing circuit. If unnecessary bandwidth is eliminated by low-pass filtering, an additional 2 dB of link budget is attainable at 30 MBd.

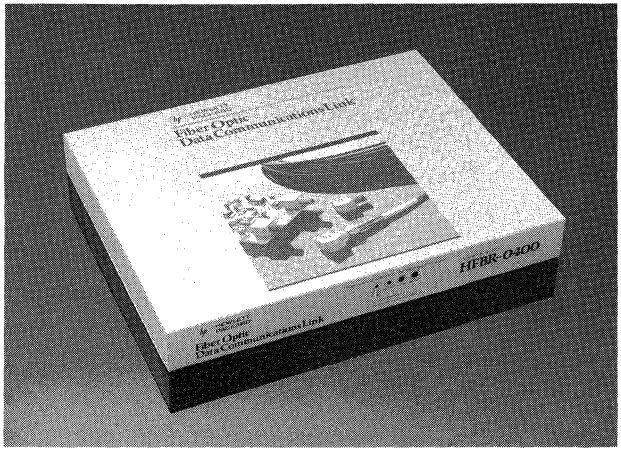
ST Evaluation Kit

There are two kits available that are compatible with the ST connector. The HFBR-0410 and the HFBR-0414 kits is a simple and inexpensive way to demonstrate the performance of Hewlett-Packard's HFBR-0400 ST Series transmitters and receivers.



The HFBR-0410 ST Evaluation Kit is useful for applications up to 5 MBd and contains the following items:

- One HFBR-1412 transmitter
- One HFBR-2412 five megabaud TTL receiver
- Three metres of ST connectored 62.5/125 µm fiber optic cable with low cost plastic ferrules
- HFBR-0400 Series data sheets
- HP Application Bulletin 73
- ST connector and cable data sheets



The HFBR-0414 ST Evaluation Kit is useful for applications up to 70 MBd and contains additional components to interface to the transmnitter and receiver as well as the PCB to reduce design time.

- One HFBR-1414T transmitter
- One HFBR-2416T receiver
- Three meters of ST connectored 62.5/125 µm fiber optic cable
- Printed circuit board
- ML 4622 CP Data Quantizer
- 74ACT11000N LED Driver
- LT1016CN8 Comparator
- 4.7 µH Inductor

SMA Evaluation Kit

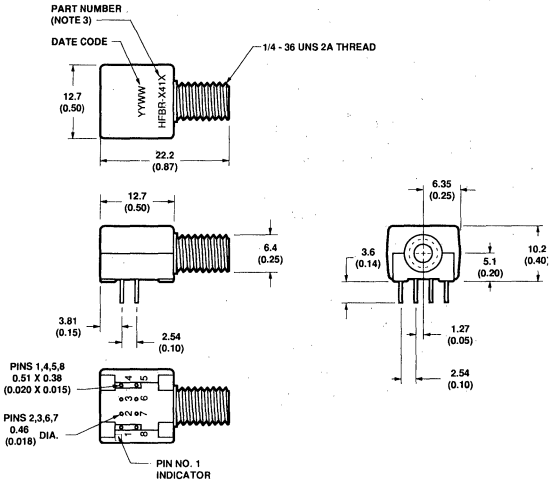
The HFBR-0400 kit is a simple and inexpensive way to demonstrate the performance of Hewlett-Packard's HFBR-0400 SMA Series transmitters and receivers.

The HFBR-0400 SMA Evaluation Kit contains the following items:

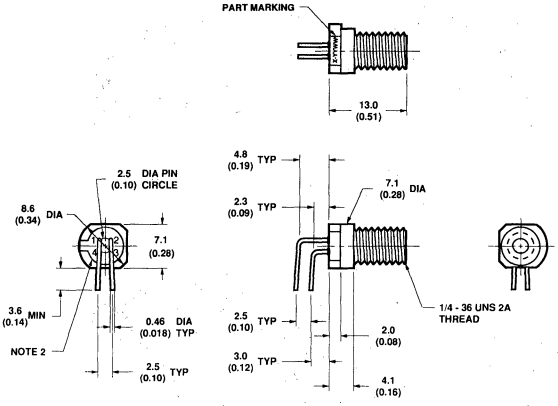
- One HFBR-1402 transmitter
- One HFBR-2402 five megabaud TTL receiver
- Two metres of SMA connectored 1000 µm plastic core fiber optic cable
- HFBR-0400 Series data sheets
- HP Applications Bulletin 73

Mechanical Dimensions HFBR-0400 SMA Series

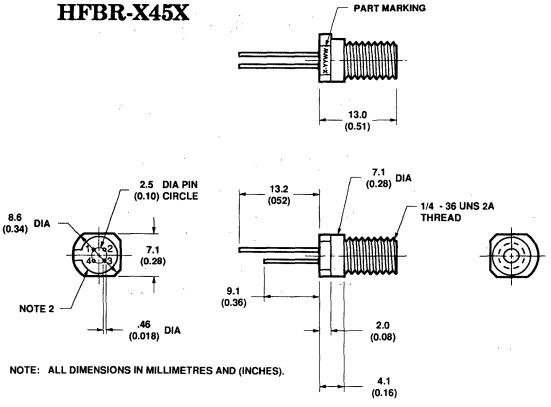
HFBR-X40X



HFBR-X43X



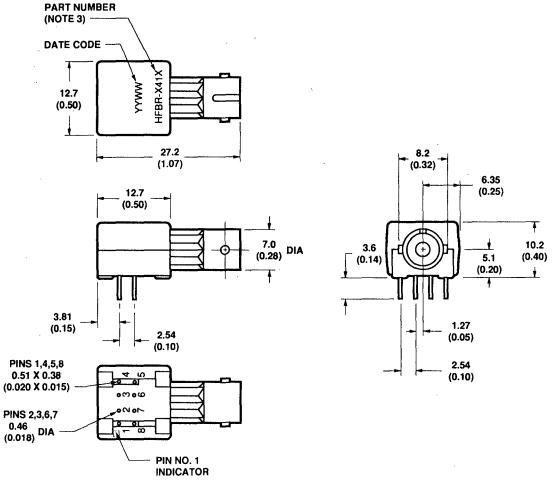
HFBR-X45X



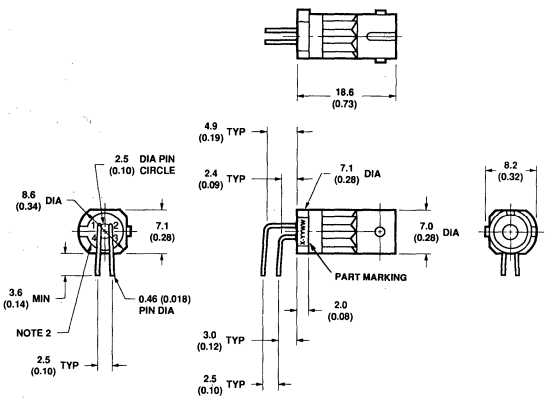
NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES).

Mechanical Dimensions HFBR-0400 ST Series

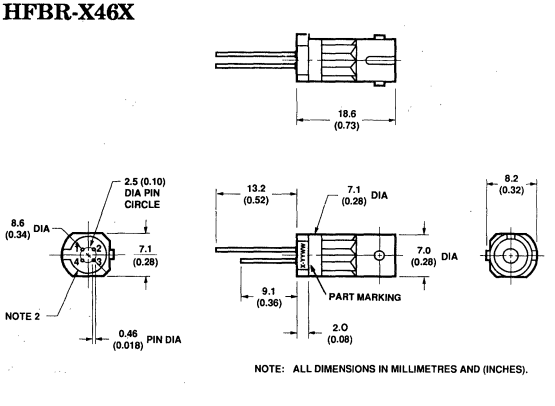
HFBR-X41X



HFBR-X44X



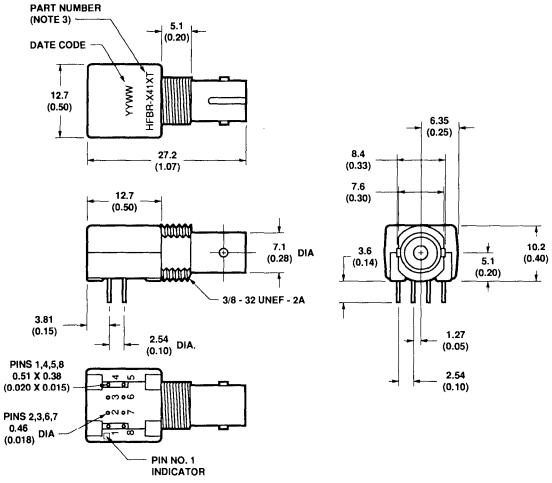
HFBR-X46X



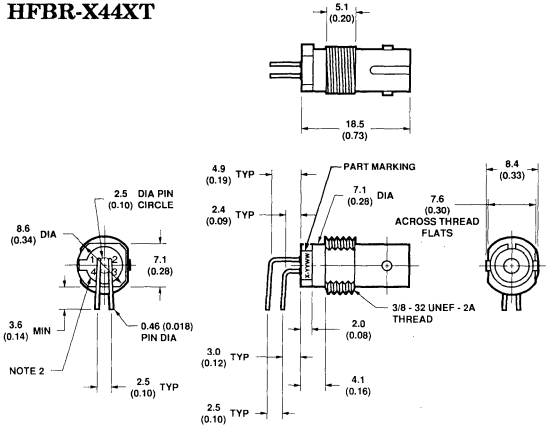
NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES).

Mechanical Dimensions
HFBR-0400T Threaded ST Series

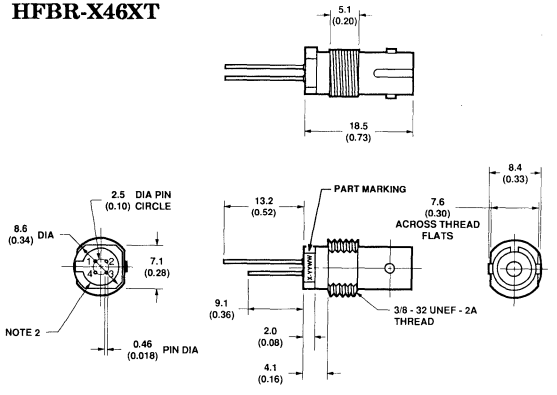
HFBR-X41XT



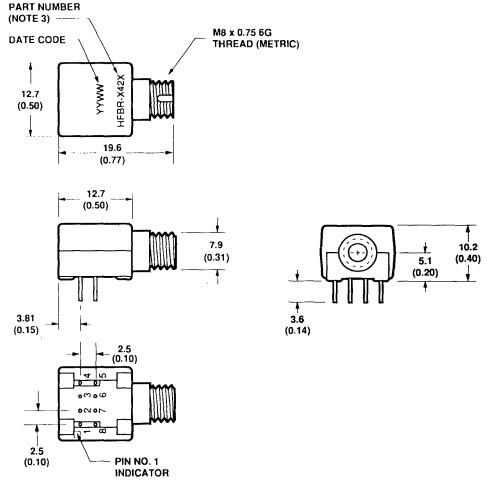
HFBR-X44XT



HFBR-X46XT

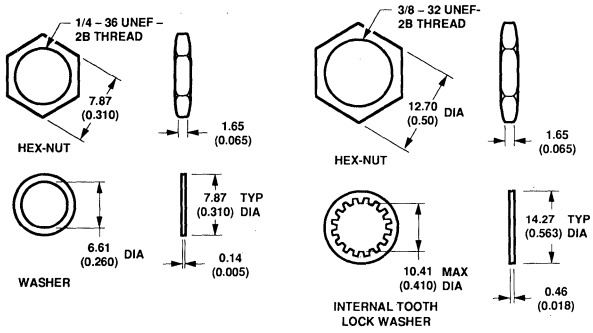


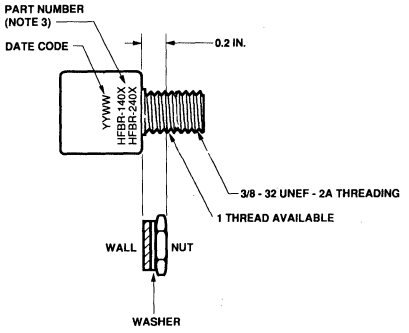
Mechanical Dimensions
HFBR-0400FC Series



Panel Mounting Hardware

HFBR-4401: for SMA Ports **HFBR-4411: for ST Ports**





(Each HFBR-4401 and HFBR-4411 kit consists of 100 nuts and 100 washers.)

Port Cap Hardware

HFBR-4402: SMA Port Caps
HFBR-4412: ST Port Caps
(Each HFBR-4402 and HFBR-4412 consists of 500 port caps)

Recommended Chemicals for Cleaning/Degreasing HFBR-0400 Products

Alcohols (methyl, isopropyl, isobutyl)
Aliphatics (hexane, heptane)
Other (soap solution, naphtha)

(Do not use partially halogenated hydrocarbons (such as 1,1.1 trichloroethane), ketones (such as MEK), acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride, or N-methylpyrolldone. Also, HP does not recommend the use of cleaners that use halogenated hydrocarbons because of their potential environmental harm.)

Notes:

1. All dimensions are in millimetres and (inches).
2. Unhoused products are distinguished by the combination of the first character in the part marking and the part marking color.
   YYWW represents the date code

Base Part Number	Part Marking	Part Marking Color
HFBR-14X2	2-YYWW	Red
HFBR-14X4	4-YYWW	Red
HFBR-24X2	2-YYWW	White
HFBR-24X4	4-YYWW	White
HFBR-24X6	6-YYWW	White

   This marking scheme does not distinguish between different connector styles.
3. The ports are shaded as shown below.

Transmitters **Receivers** **Conductive Port Receivers**

HEWLETT PACKARD

High Speed Low Cost Fiber Optic Transmitter

Technical Data

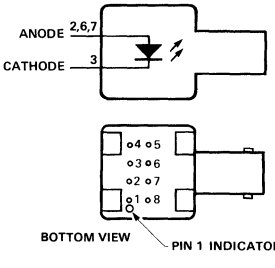
HFBR-14X2 and HFBR-14X4 Series

Description

The HFBR-14XX fiber optic transmitter contains an 820 nm GaAlAs emitter capable of efficiently launching optical power into four different optical fiber sizes: 50/125 µm, 62.5/125 µm, 100/140 µm, and 200 µm PCS. This allows the designer flexibility in choosing the fiber size. The HFBR-14XX is designed to operate with the Hewlett-Packard HFBR-24XX fiber optic receivers.

The HFBR-14XX transmitter's high coupling efficiency allows the emitter to be driven at low current levels resulting in low power consumption and increased reliability of the transmitter. The HFBR-14X4 high power transmitter is optimized for small size fiber and typically can launch –15.8 dBm optical power @ 60 mA into 50/125 µm fiber and –12 dBm into 62.5/125 µm fiber. The HFBR-14X2 standard transmitter typically can couple –11.5 dBm of optical power @ 60 mA into 100/140 µm fiber cable. It is ideal for large size fiber such as 100/140 µm. The high power level is useful for systems where star couplers, taps, or inline connectors create large fixed losses.

Housed Product



PIN	FUNCTION
1†	N.C.
2	ANODE
3*	CATHODE
4†	N.C.
5†	N.C.
6	ANODE
7*	ANODE
8†	N.C.

*PINS 2,6 AND 7 ARE ELECTRICALLY CONNECTED TO HEADER

†PINS 1, 4, 5, AND 8 ARE ELECTRICALLY CONNECTED

Unhoused Product

PIN	FUNCTION
1	ANODE
2	CATHODE
3	ANODE
4	ANODE

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–55	+85	°C	
Operating Temperature		T_A	–40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	
	Time			10	sec	
Forward Input Current	Peak	I_{FPK}		200	mA	Note 1
	DC	I_{FDC}		100	mA	
Reverse Input Voltage		V_{BR}		1.8	V	

Consistent coupling efficiency is assured by the double-lens optical system (Figure 1). Power coupled into any of the three fiber types varies less than 5 dB from part to part at a given drive current and temperature. The benefit of this is reduced dynamic range requirements on the receiver.

CAUTION: The small junction sizes inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Electrical / Optical Specifications –40°C to +85°C unless otherwise specified.

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Reference
Forward Voltage	V_F	1.48	1.70	2.09	V	I_F = 60 mA	Figure 9
			1.84			I_F = 100 mA	
Forward Voltage Temperature Coefficient	V_F/T		–0.22		mV/°C	I_F = 60 mA	Figure 9
			–0.18			I_F = 100 mA	
Reverse Input Voltage	V_{BR}	1.8	3.8		V	I_R = 100 µA	
Center Emission Wavelength	λ_P	792	820	865	nm		
Diode Capacitance	C_T		55		pF	V = 0, f = 1 MHz	
Optical Power Temperature Coefficient	P_T/T		–0.006		dB/°C	I = 60 mA	
			–0.010			I = 100 mA	
Thermal Resistance	θ_{JA}		260		°C/W		Notes 3, 8
Numerical Aperture (HFBR – 14X4)	NA_{14X4}		0.31				
Numerical Aperture (HFBR – 14X2)	NA_{14X2}		0.49				
Optical Port Diameter (HFBR – 14X4)	D_{14X4}		150		µm		Note 4
Optical Port Diameter (HFBR – 14X2)	D_{14X2}		290		µm		Note 4

Electrical / Optical Specifications –40°C to +85°C unless otherwise specified

HFBR-14X4 Peak Output Power Measured Out of 1m of Cable

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions		Reference
50/125 µm Fiber Cable NA = 0.20	$P_{T_{50}}$	–18.8	–15.8	–13.8	dBm	T_A = 25°C	I_F = 60 mA	Notes 5, 6, 9
		–19.8		–12.8				
		–17.3	–13.8	–11.4		T_A = 25°C	I_F = 100 mA	
		–18.9		–10.8				
62.5/125 µm Fiber Cable NA = 0.275	$P_{T_{62}}$	–15.0	–12.0	–10.0	dBm	T_A = 25°C	I_F = 60 mA	
		–16.0		–9.0				
		–13.5	–10.0	–7.6		T_A = 25°C	I_F = 100 mA	
		–15.1		–7.0				
100/140 µm Fiber Cable NA = 0.30	$P_{T_{100}}$	–9.5	–6.5	–4.5	dBm	T_A = 25°C	I_F = 60 mA	
		–10.5		–3.5				
		–8.0	–4.5	–2.1		T_A = 25°C	I_F = 100 mA	
		–9.6		–1.5				
200 µm PCS Fiber Cable NA = 0.40	$P_{T_{200}}$	–4.5	–3.0	+1.5	dBm	T_A = 25°C	I_F = 60 mA	
		–5.5		+2.5				
		–3.0	–1.0	+3.9		T_A = 25°C	I_F = 100 mA	
		–4.6		+4.5				

HFBR-14X2 Peak Output Power Measured Out of 1m of Cable

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions		Reference
50/125 µm Fiber Cable NA = 0.20	$P_{T_{50}}$	–21.8	–18.8	–16.8	dBm	T_A = 25°C	I_F = 60 mA	Notes 5, 6, 9
		–22.8		–15.8				
		–20.3	–16.8	–14.4		T_A = 25°C	I_F = 100 mA	
		–21.9		–13.8				
62.5/125 µm Fiber Cable NA = 0.275	$P_{T_{62}}$	–19.0	–16.0	–14.0	dBm	T_A = 25°C	I_F = 60 mA	
		–20.0		–13.0				
		–17.5	–14.0	–11.6		T_A = 25°C	I_F = 100 mA	
		–19.1		–11.0				
100/140 µm Fiber Cable NA = 0.30	$P_{T_{100}}$	–15.0	–12.0	–10.0	dBm	T_A = 25°C	I_F = 60 mA	
		–16.0		–9.0				
		–13.5	–10.0	–7.6		T_A = 25°C	I_F = 100 mA	
		–15.1		–7.0				
200 µm PCS Fiber Cable NA = 0.40	$P_{T_{200}}$	–10.0	–6.5	–4.0	dBm	T_A = 25°C	I_F = 60 mA	
		–11.0		–3.0				
		–8.5	–4.5	–1.6		T_A = 25°C	I_F = 100 mA	
		–10.1		–1.0				

WARNING: Observing the transmitter output power under magnification may cause injury to the eye. When viewed with the unaided eye, the infrared output is radiologically safe. However, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Reference
Rise Time, Fall Time (10% to 90%)	t_r, t_f		4.0	6.5	nsec	I_F = 60 mA No Pre-bias	Note 7, Figure 12
Rise Time, Fall Time (10% to 90%)	t_r, t_f		3.0		nsec	I_F = 10 to 100 mA	Note 7, Figure 11
Pulse Width Distortion	PWD		0.5		nsec		Figure 11

Notes:
1. For I_{FPK} > 100 mA, the time duration should not exceed 2 ns.
2. Typical data at T_A = 25°C.
3. Thermal resistance is measured with the transmitter coupled to a connector assembly and mounted on a printed circuit board.
4. D_T is measured at the plane of the fiber face and defines a diameter where the optical power density is within 10 dB of the maximum.
5. P_T is measured with a large area detector at the end of 1 metre of mode stripped cable, with an ST* precision ceramic ferrule (MIL-STD-83522/13) for HFBR-1412/1414, and with an SMA 905 precision ceramic ferrule for HFBR-1402/1404. This approximates a standard test connector.
6. When changing µW to dBm, the optical power is referenced to 1 mW (1000 µW). Optical Power P (dBm) = 10 log P (µW)/ 1000 µW.
7. Pre-bias is recommended if signal rate > 10 MBd, see recommended drive circuit in Figure 11.
8. Pins 2, 6 and 7 are welded to the anode header connection to minimize the thermal resistance from junction to ambient. To further reduce the thermal resistance, the anode trace should be made as large as is consistent with good RF circuit design.
9. Fiber NA is measured at the end of 2 metres of mode stripped fiber, using the far-field pattern. NA is defined as the sine of the half angle, determined at 5% of the peak intensity point. When using other manufacturer's fiber cable, results will vary due to differing NA values and specification methods.

Recommended Drive Circuits

The circuit used to supply current to the LED transmitter can significantly influence the optical switching characteristics of the LED. The optical rise/fall times and propagations delays can be improved by using certain circuit techniques.

The LED drive circuit shown in Figure 11 uses current-peaking to reduce the typical rise/fall times of the LED and a small pre-bias voltage to minimize propagation delay differences that cause pulse-width distortion. The circuit will typically produce rise/fall times of 3 ns, and a total jitter including pulse-width distortion of less than 2 ns. This circuit is recommended for applications requiring low edge jitter or high-speed data transmission at signal rates of up to 125 MBd. Component values for this circuit can be calculated for different LED drive currents using the equations shown below.

For additional details about LED drive circuits, the reader is encouraged to read Hewlett-Packard Application Bulletin 78 and Application Note 1038.

$$R_y(\Omega) = \frac{(V_{CC} - V_F) + 3.97\,(V_{CC} - V_F - 1.6\ V)}{I_{F_{ON}}(A)}$$

$$R_{x_1}(\Omega) = \frac{1}{2}\left(\frac{R_y}{3.97}\right)$$

$$R_{EQ_2}(\Omega) = R_{x_1} - 1$$

$$R_{x_2} = R_{x_3} = R_{x_4} = 3\,(R_{EQ_2})$$

$$C\,(pF) = \frac{2000\,(ps)}{R_{x_1}(\Omega)}$$

Example for $I_{F_{ON}}$ = 100 mA: V_F can be obtained from Figure 9 (= 1.84 V)

$$R_y = \frac{(5 - 1.84) + 3.97\,(5 - 1.84 - 1.6)}{0.100}$$

$$R_y = \frac{3.16 + 6.19}{0.100} = 93.5\ \Omega$$

$$R_{x_1} = \frac{1}{2}\left(\frac{R_y}{3.97}\right) = 11.8\ \Omega$$

$$R_{EQ_2} = 11.8 - 1 = 10.8\ \Omega$$

$$R_{x_2} = R_{x_3} = R_{x_4} = 3\,(10.8) = 32.4\ \Omega$$

$$C = \frac{2{,}000\ pS}{11.8\ \Omega} = 169\ pF$$

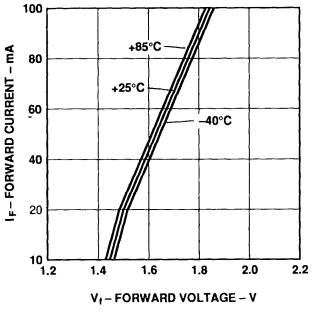


Figure 9. Forward Voltage and Current Characteristics.

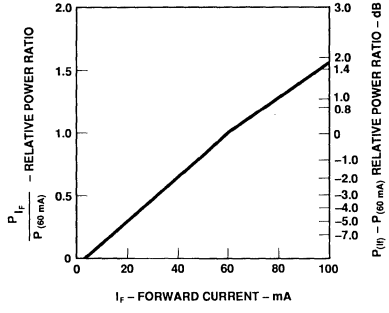


Figure 10. Normalized Transmitter Output vs. Forward Current.

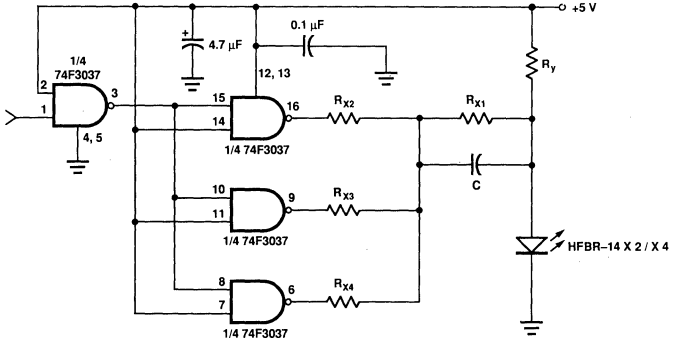


Figure 11. Recommended Drive Circuit.

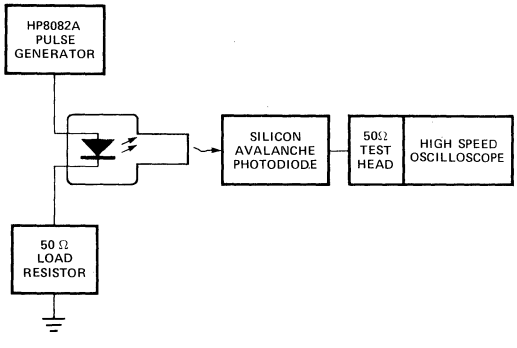


Figure 12. Test Circuit for Measuring t_r, t_f.

HEWLETT PACKARD

5 MBd Low Cost Fiber Optic Receiver

Technical Data

HFBR-24X2 Series

Description

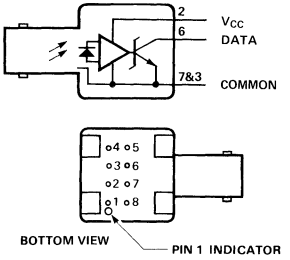
The HFBR-24X2 fiber optic receiver is designed to operate with the Hewlett-Packard HFBR-14XX fiber optic transmitter and 50/125 µm, 62.5/125 µm, and 100/140 µm fiber optic cable. Consistent coupling into the receiver is assured by the lensed optical system (Figure 1). Response does not vary with fiber size.

The HFBR-24X2 receiver incorporates an integrated photo IC containing a photodetector and dc amplifier driving an open-collector Schottky output transistor. The HFBR-24X2 is designed for direct interfacing to popular logic families. The absence of an internal pull-up resistor allows the open-collector output to be used with logic families such as CMOS requiring voltage excursions much higher than V_{CC}.

Both the open-collector "Data" output Pin 6 and V_{CC} Pin 2 are referenced to "Com" Pin 3, 7. The "Data" output allows busing, strobing and wired "OR" circuit configurations. The transmitter is designed to operate from a single +5 V supply. It is essential that a bypass capacitor (0.1 µF ceramic) be connected from Pin 2 (V_{CC}) to Pin 3 (circuit common) of the receiver.

CAUTION: The small junction sizes inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Housed Product



PIN	FUNCTION
1†	N.C.
2	V_{CC} (5 V)
3*	COMMON
4†	N.C.
5†	N.C.
6	DATA
7*	COMMON
8†	N.C.

*PINS 3 AND 7 ARE ELECTRICALLY CONNECTED TO HEADER

†PINS 1, 4, 5, AND 8 ARE ELECTRICALLY CONNECTED

Unhoused Product

BOTTOM VIEW

PIN	FUNCTION
1	V_{CC} (5 V)
2	COMMON
3	DATA
4	COMMON

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–55	+85	°C	
Operating Temperature		T_A	–40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	Note 1
	Time			10	sec	
Supply Voltage		V_{CC}	–0.5	7.0	V	
Output Current		I_O		25	mA	
Output Voltage		V_O	–0.5	18.0	V	
Output Collector Power Dissipation		$P_{O\,AV}$		40	mW	
Fan Out (TTL)		N		5		Note 2

Electrical / Optical Characteristics –40°C to + 85°C unless otherwise specified;

Fiber sizes with core diameter ≤ 100 µm and NA ≤ 0.35, 4.75 V ≤ V_{CC} ≤ 5.25 V

Parameter	Symbol	Min.	Typ.[9]	Max.	Units	Conditions	Reference
High Level Output Current	I_{OH}		5	250	µA	V_O = 18 V P_R < –40 dBm	
Low Level Output Voltage	V_{OL}		0.4	0.5	V	I_O = 8 mA P_R > –24 dBm	
High Level Supply Current	I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V P_R < –40 dBm	
Low Level Supply Current	I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V P_R > –24 dBm	
Equivalent N.A.	NA		0.50				
Optical Port Diameter	D_R		400		µm		Note 4

Dynamic Characteristics –40°C to +85°C unless otherwise specified; 4.75 V ≤ V_{CC} ≤ 5.25 V; BER ≤ 10^{-9}

Parameter	Symbol	Min.	Typ.[3]	Max.	Units	Conditions	Reference
Peak Input Power Level Logic HIGH	P_{RH}			–40 0.1	dBm μW	λ_P = 820 nm	Note 5
Peak Input Power Level Logic LOW	P_{RL}	–25.4		–9.2	dBm	T_A = +25°C,	Note 5
		2.9		120	μW	I_{OL} = 8 mA	
		–24.0		–10.0	dBm	I_{OL} = 8 mA	
		4.0		100	μW		
Propagation Delay LOW to HIGH	t_{PLHR}		65		nsec	T_A = 25°C, P_R = –21 dBm, Data Rate = 5 MBd	Note 6
Propagation Delay HIGH to LOW	t_{PHLR}		49		nsec		

Notes:

1. 2.0 mm from where leads enter case.
2. 8 mA load (5 x 1.6 mA), R_L = 560 Ω.
3. Typical data at T_A = 25° C, V_{CC} = 5.0 Vdc.
4. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
5. Measured at the end of 100/140 μm fiber optic cable with large area detector.
6. Propagation delay through the system is the result of several sequentially-occurring phenomena. Consequently it is a combination of data-rate-limiting effects and of transmission-time effects. Because of this, the data-rate limit of the system must be described in terms of time differentials between delays imposed on falling and rising edges.
   As the cable length is increased, the propagation delays increase at 5 ns per metre of length. Data rate, as limited by pulse width distortion, is not affected by increasing cable length if the optical power level at the receiver is maintained.

HEWLETT PACKARD

25 MHz Low Cost Fiber Optic Receiver

Technical Data

HFBR-24X4 Series

Description

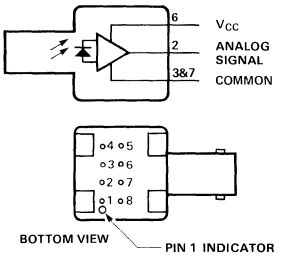
The HFBR-24X4 fiber optic receiver is designed to operate with the Hewlett-Packard HFBR-14XX fiber optic transmitters and 50/125 µm, 62.5/125 µm, and 100/140 µm fiber optic cable. Consistent coupling into the receiver is assured by the lensed optical system (Figure 1). Response does not vary with fiber size.

The receiver output is an analog signal that can be optimized for a variety of distance/data rate requirements. Low-cost external components can be used to convert the analog output to logic compatible signal levels for various data formats and data rates up to 35 MBaud. This distance/data rate tradeoff results in increased optical power budget at lower data rates which can be used for additional distance or splices.

The HFBR-24X4 receiver contains a PIN photodiode and low noise transimpedance pre-amplifier integrated circuit with an inverting output (see note 3). The HFBR-24X4 receives an optical signal and converts it to an analog voltage. The output is a buffered emitter-follower. Because the signal amplitude from the HFBR-24X4 receiver is much larger than from a simple PIN photodiode, it is less susceptible to EMI, especially at high signal rates. A receiver dynamic range of 15 dB over temperature is achievable (assuming 10^{-9} BER). For very noisy environments, the conductive port option is recommended.

The frequency response is typically dc to 25 MHz. Although the HFBR-24X4 is an analog receiver, it is easily made compatible with digital systems. Please refer to Application Bulletin 73 for simple and inexpensive circuits that operate up to 35 MBd.

Housed Product



PIN	FUNCTION
1†	N.C.
2	SIGNAL
3*	COMMON
4†	N.C.
5†	N.C.
6	V_{CC} (5 V)
7*	COMMON
8†	N.C.

*PINS 3 AND 7 ARE ELECTRICALLY CONNECTED TO HEADER

†PINS 1, 4, 5, AND 8 ARE ELECTRICALLY CONNECTED

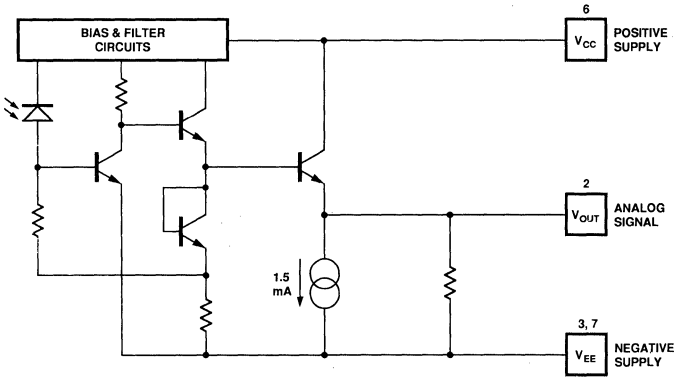
Unhoused Product

BOTTOM VIEW

PIN	FUNCTION
1	SIGNAL
2	COMMON
3	V_{CC} (5 V)
4	COMMON

CAUTION: *The small junction sizes inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Simplified Schematic Diagram



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–55	+85	°C	
Operating Temperature		T_A	–40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	Note 1
	Time			10	sec	
Signal Pin Voltage		V_{SIGNAL}	–0.5	1	V	
Supply Voltage		V_{CC}	–0.5	7.0	V	

Electrical / Optical Characteristics –40°C to +85°C; 4.75 V ≤ V_{CC} ≤ 5.25 V; R_{LOAD} = 511 Ω; Fiber sizes with core diameter ≤ 100 µm, and N.A. ≤ 0.35 unless otherwise specified.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Reference
Responsivity	R_P	5.1	7	10.9	mV/µW	T_A = 25°C @ 820 nm	Figure 14
		4.6		12.3	mV/µW		
RMS Output Noise Voltage	V_{NO}		0.30	0.36	mV	T_A = 25°C, P_R = 0 µW	Figure 15
				0.43	mV	P_R = 0 µW	
Equivalent Optical Noise Input Power (RMS)	P_N		–43.7	–40.3	dBm		
			0.042	0.094	µW		
Peak Input Power	P_R			–12.6	dBm	T_A = 25°C	Note 2
				55	µW		
				–14	dBm		
				40	µW		
Output Impedance	Z_O		20		Ω	Test Frequency = 20 MHz	
DC Output Voltage	V_{odc}		0.7		V	P_R = 0 µW	Note 3
Power Supply Current	I_{CC}		3.4	6.0	mA	R_{LOAD} = ∞	
Equivalent N.A.	NA		0.35				
Equivalent Diameter	D_R		250		µm		Note 4

Dynamic Characteristics –40°C to +85°C; 4.75 V ≤ V_{CC} ≤ 5.25 V; R_{LOAD} = 511 Ω, C_{LOAD} = 13 pF unless otherwise specified.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Reference
Rise/Fall Time, 10% to 90%	t_r, t_f		14	19.5	ns	T_A = 25°C P_R = 10 µW Peak	Note 6
				26	ns		
Pulse Width Distortion	$t_{phl} - t_{plh}$			2	ns	P_R = 40 µW Peak	
Overshoot			10		%	T_A = 25°C	Note 7
Bandwidth (Electrical)	BW_e		25		MHz	–3 dB Electrical	
Power Supply Rejection Ratio (Referred to Output)	PSRR		50		dB	at 1 MHz	Figure 16 Note 8
Bandwidth - Rise Time Product			0.35		Hz · s		

Notes:

1. 2.0 mm from where leads enter case.
2. If P_R > 40 µW, then pulse width distortion may increase. At P_{in} = 80 µW and T_A = 85°C, some units have exhibited as much as 100 ns pulse width distortion.
3. $V_{OUT} = V_{ODC} - (R_p \times P_R)$.
4. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
5. Typical specifications are for operation at T_A = 25°C and V_{CC} = 5.0 V.
6. Input optical signal is assumed to have 10% - 90% rise and fall times of less than 6 ns.
7. Percent overshoot is defined as: $\left(\frac{V_{PK} - V_{100\%}}{V_{100\%}}\right)$ x 100%.
8. Output referred P.S.R.R. is defined as 20 log $\left(\frac{V_{POWER\ SUPPLY\ RIPPLE}}{V_{OUT\ RIPPLE}}\right)$.

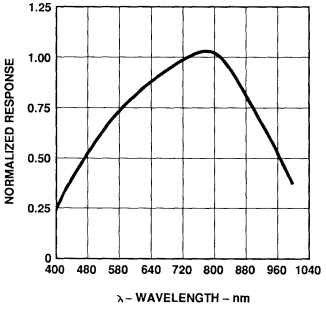


Figure 14. Receiver Spectral Response Normalized to 820 nm.

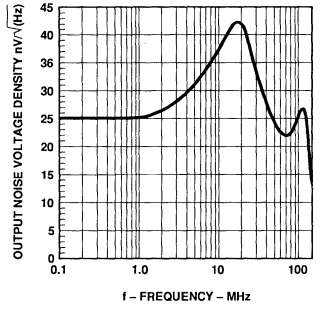


Figure 15. Receiver Noise Spectral Density.

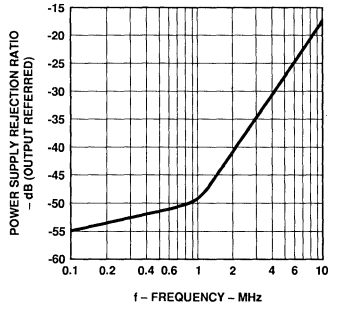


Figure 16. Receiver Power Supply Rejection vs. Frequency.

HEWLETT PACKARD

125 MHz Low Cost Fiber Optic Receiver

Technical Data

HFBR-24X6 Series

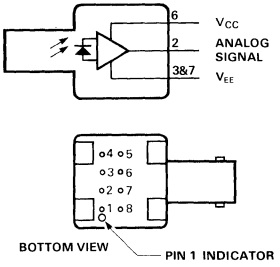
Description

The HFBR-24X6 fiber optic receiver is designed to operate with the Hewlett-Packard HFBR-14XX fiber optic transmitters and 50/125 µm, 62.5/125 µm, and 100/140 µm fiber optic cable. Consistent coupling into the receiver is assured by the lensed optical system (Figure 1). Response does not vary with fiber size for core diameters of 100 µm or less.

The receiver output is an analog signal which allows follow-on circuitry to be optimized for a variety of distance/data rate requirements. Low-cost external components can be used to convert the analog output to logic compatible signal levels for various data formats and data rates up to 155 MBd. This distance/data rate tradeoff results in increased optical power budget at lower data rates which can be used for additional distance or splices.

The HFBR-24X6 receiver contains a PIN photodiode and low noise transimpedance pre-amplifier integrated circuit. The HFBR-24X6 receives an optical signal and converts it to an analog voltage. The output is a buffered emitter-follower. Because the signal amplitude from the HFBR-24X6 receiver is much larger than from a simple PIN photodiode, it is less susceptible to EMI, especially at high signal rates. For very noisy environments, the conductive port option is recommended. A receiver dynamic range of 23 dB over temperature is achievable (assuming 10^{-9} BER). Because the maximum receiver input power is 6 dB larger and the noise is 2 dB lower over temperature than HP's HFBR-24X4 25 MHz receiver, the HFBR-24X6 is well suited for more demanding link designs that require wide receiver dynamic range.

Housed Product



PIN	FUNCTION
1†	N.C.
2	SIGNAL
3*	V_{EE}
4†	N.C.
5†	N.C.
6	V_{CC}
7*	V_{EE}
8†	N.C.

*PINS 3 AND 7 ARE ELECTRICALLY CONNECTED TO HEADER

†PINS 1, 4, 5 AND 8 ARE ELECTRICALLY CONNECTED.

Unhoused Product

BOTTOM VIEW

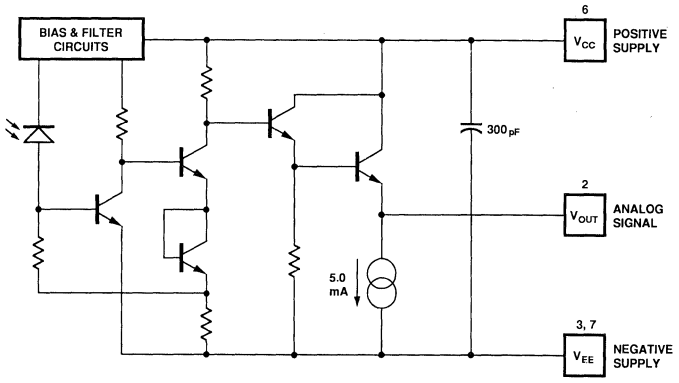
PIN	FUNCTION
1	SIGNAL
2*	V_{EE}
3	V_{CC}
4*	V_{EE}

CAUTION: *The small junction sizes inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

The frequency response is typically dc to 125 MHz. Although the HFBR-24X6 is an analog receiver, it is easily made compatible with digital systems. Please refer to Application Bulletin 78 for simple and inexpensive circuits that operate up to 155 MBd.

The recommended ac coupled receiver circuit is shown in Figure 17. It is essential that a 10 ohm resistor be connected between V_{EE} and the power supply, and a 0.1 µF ceramic bypass capacitor be connected between the power supply and ground.

Simplified Schematic Diagram



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–55	+85	°C	
Operating Temperature		T_A	–40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	Note 1
	Time			10	sec	
Signal Pin Voltage		V_{SIGNAL}	–0.5	V_{CC}	V	
Supply Voltage		V_{CC}-V_{EE}	–0.5	6.0	V	
Output Current		I_O		25	mA	

Electrical / Optical Characteristics -40°C to +85°C; -5.45 V ≤ Supply Voltage ≤ -4.75 V, R_{LOAD} = 511 Ω, Fiber sizes with core diameter ≤ 100 µm, and N.A. ≤ 0.35 unless otherwise specified.

Parameter	Symbol	Min.	Typ.[3]	Max.	Units	Conditions	Reference
Responsivity	R_P	5.3	7	9.6	mV/µW	T_A = 25° C @ 820 nm, 50 MHz	Note 3, 4 Figure 21
		4.5		11.5	mV/µW	@ 820 nm, 50 MHz	
RMS Output Noise Voltage	V_{NO}		0.40	0.59	mV	Bandwidth Filtered @ 75 MHz P_R = 0 µW	Note 5
				0.70	mV	Unfiltered Bandwidth P_R = 0 µW	Figure 18
Equivalent Optical Noise Input Power (RMS)	P_N		-43.0	-41.4	dBm	Bandwidth Filtered @ 75 MHz	
			0.050	0.065	µW		
Peak Input Power	P_R			-7.6	dBm	T_A = 25°C	Figure 19 Note 6
				175	µW		
				-8.2	dBm		
				150	µW		
Output Impedance	Z_O		30		Ω	Test Frequency = 50 MHz	
DC Output Voltage	V_{odc}	-4.2	-3.1	-2.4	V	P_R = 0 µW	
Power Supply Current	I_{EE}		9	15	mA	R_{LOAD} =	
Equivalent N.A.	NA		0.35				
Equivalent Diameter	D_R		324		µm		Note 7

Dynamic Characteristics –40°C to +85°C; –5.45 V ≤ Supply Voltage ≤ –4.75 V; R_{LOAD} = 511 Ω, C_{LOAD} = 5 pF unless otherwise specified.

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Reference
Rise/Fall Time 10% to 90%	t_r, t_f		3.3	6.3	ns	P_R = 100 µW	Figure 20
Pulse Width Distortion	PWD		0.4	2.5	ns	P_R = 150 µW Peak	Note 8, Figure 19
Overshoot			2		%	P_R = 5 µW Peak, $t_{r_{optical}}$ = 1.5 ns	Note 9
Bandwidth (Electrical)	BW_e		125		MHz	–3 dB Electrical	
Power Supply Rejection Ratio	PSRR		20		dB	@ 10 MHz	Note 10
Bandwidth - Rise Time Product			0.41		Hz · s		Note 11

Notes:

1. 2.0 mm from where leads enter case.
2. Typical specifications are for operation at T_A = 25°C and V_{EE} = –5.2 Vdc.
3. For 200 µm PCS fibers, typical responsivity will be 6 mV/µW. Other parameters will change as well.
4. Pin #2 should be ac coupled to a 511 ohm load. Load capacitance must be less than 5 pF.
5. Measured with a 3 pole Bessel filter with a 75 MHz, –3 dB bandwidth. Recommended receiver filters for various bandwidths are provided in Application Bulletin 78.
6. Overdrive is defined at PWD = 2.5 ns.
7. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
8. Measured with a 10 ns pulse width, 50% duty cycle, at the 50% amplitude point of the waveform.
9. Percent overshoot is defined as: $\left(\frac{V_{PK} - V_{100\%}}{V_{100\%}}\right)$ x 100%.
10. Output referred P.S.R.R. is defined as 20 log $\left(\frac{V_{POWER\ SUPPLY\ RIPPLE}}{V_{OUT\ RIPPLE}}\right)$.
11. The conversion factor for the rise time to bandwidth is 0.41 since the HFBR-24X6 has a second order bandwidth limiting characteristic.

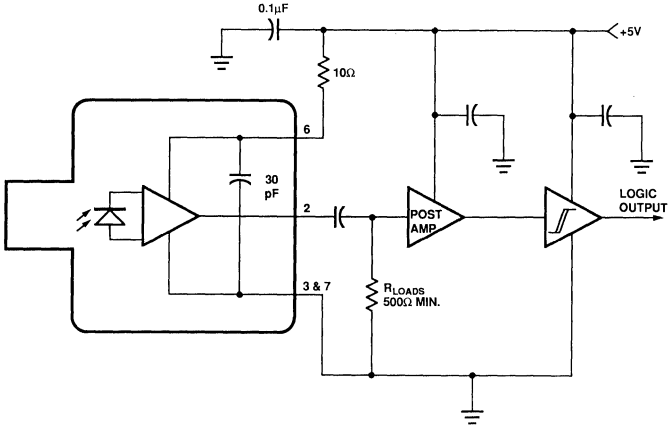


Figure 17. Recommended ac Coupled Receiver Circuit (See AB 78 and AN 1038 for More Information)

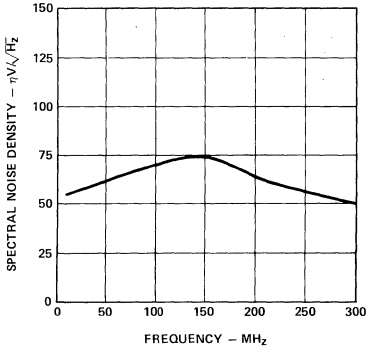


Figure 18. Typical Spectral Noise Density vs. Frequency

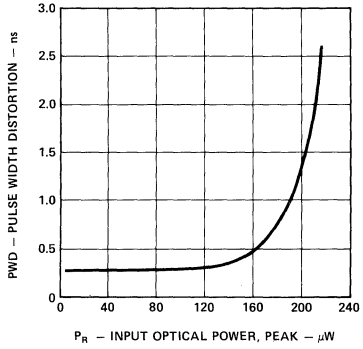


Figure 19. Typical Pulse Width Distortion vs. Peak Input Power

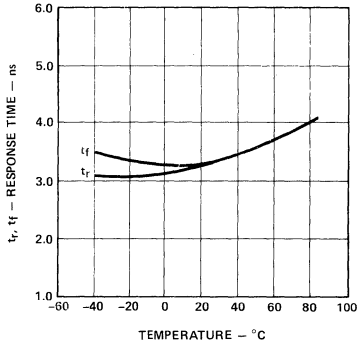


Figure 20. Typical Rise and Fall Times vs. Temperature

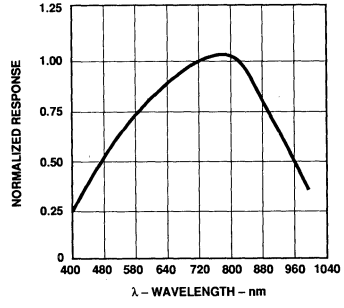


Figure 21. Receiver Spectral Response Normalized to 820 nm.

HEWLETT PACKARD

Conductive Port Option for Low Cost Miniature Link Components

Technical Data

OPTION C

Features

- **Significantly Decreases Effect of Electro-magnetic Interference (EMI) on Receiver Sensitivity**
- **Available with Both SMA and Threaded ST Styled Port Receivers**
- **Allows the Designer to Separate the Signal and Conductive Port Grounds**

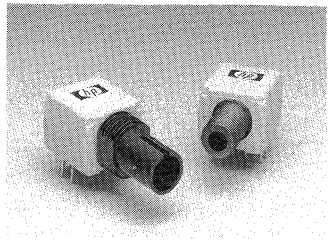
Description

The conductive port option for the Low Cost Miniature Link component family consists of a grounding path from the conductive port to four grounding pins as shown in the package outline drawing. Signal ground is separate from the four grounding pins to give the designer more flexibility. This option is available with all SMA and ST panel mount styled port receivers. Electrical/optical performance of the receivers is not affected by the conductive port. Refer to the HFBR-0400 data sheets for more information.

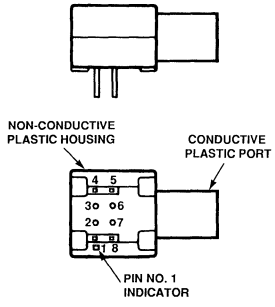
Applications

HP recommends that the designer use separate ground paths for the signal ground and the conductive port ground in order to minimize the effects of coupled noise on the receiver circuitry. If the designer notices that extreme noise is present on the system chassis, care should be taken to electrically isolate the conductive port from the chassis.

In the case of ESD, the conductive port option does not alleviate the need for system recovery procedures. A 15 kV ESD event entering through the port will not cause catastrophic failure for any HFBR-0400 receivers, but may cause soft errors. The conductive port option can reduce the amount of soft errors due to ESD events, but does not guarantee error-free performance.



Package Outline



Pin	Function
1	Port Ground Pin
2	Part Dependent
3	Part Dependent
4	Port Ground Pin
5	Port Ground Pin
6	Part Dependent
7	Part Dependent
8	Port Ground Pin

Reliability Information

Low Cost Miniature Link components with the Conductive Port Option are as reliable as standard HFBR-0400 components. The following tests were performed to verify the mechanical reliability of this option.

Ordering Information

To order the Conductive Port Option with a particular receiver component, place a "C" after the base part number. For example, to order an HFBR-2406 with this option, order an HFBR-2406C. As another example, to order an HFBR-2416T with this option, order an HFBR-2416TC.

This option is available with the following part numbers:

HFBR-2402	HFBR-2442T
HFBR-2404	HFBR-2444T
HFBR-2406	HFBR-2446T
HFBR-2412T	HFBR-2452
HFBR-2414T	HFBR-2454
HFBR-2416T	HFBR-2456
HFBR-2432	HFBR-2462T
HFBR-2434	HFBR-2464T
HFBR-2436	HFBR-2466T

Mechanical and Environmental Tests[1]

Test	MIL-STD-883/ Other Reference	Test Conditions	Units Tested	Total Failed
Temperature Cycling	1010 Condition B	-55°C to +125°C 15 min. dwell/5 min. transfer 100 cycles	70	0
Thermal Shock	1011 Condition B	-55°C to +125°C 5 min. dwell/10 sec. transfer 500 cycles	45	0
High Temp. Storage	1008 Condition B	T_A = 125°C 1000 hours	50	0
Mechanical Shock	2002 Condition B	1500 g/0.5 ms 5 impacts each axis	40	0
Port[2] Strength	T_A = 25°C	6 Kg-cm no port damage	20	0
Seal Dye Penetrant (Zyglo)	1014 Condition D	45 psi, 10 hours No leakage into microelectronic cavity	15	0
Solderability	2003	245°C	10	0
Resistance to Solvents	2015	3 one min. immersion brush after solvent	13	0
Chemical Resistance	-	5 minutes in Acetone, Methanol, Boiling Water	12	0
Temperature-Humidity	-	T_A = 85°C, RH = 85% Biased, 500 hours	30	0
Lead Integrity	2004 Condition B2	8 oz. wt. to each lead tested for three 90° arcs of the case	16	0
Electrostatic Discharge (ESD)	IEC-801-2	Direct contact discharge to port, 0-15 kV[3]	16	0

Notes:

1. Tests were performed on both SMA and ST products with the conductive port option.
2. The Port Stength test was designed to address the concerns with hand tightening the SMA connector to the fiber optic port. The limit is set to a level beyond most reasonable hand fastening loading.
3. HP has previously used an air discharge method to measure ESD; results using this method vary with air temperature and humidity. The direct contact discharge method is preferred due to better repeatability and conformance with IEC procedures. ESD immunity measured with the air discharge method is generally higher than with the direct contact discharge method.

HEWLETT PACKARD

Threaded ST Port Option for Low Cost Miniature Link Components

Technical Data

OPTION T

Features

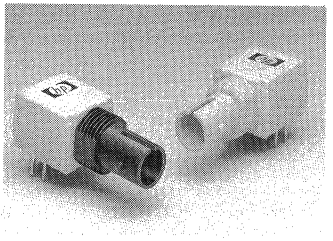
- **Threading Allows ST Styled Port Components to be Panel Mounted**
- **Compatible with all Current Makes of ST Multimode Connectors**
- **Mechanical Dimensions are Compliant with MIL-STD-83522/13**

Description

Low Cost Miniature Link components with the Threaded ST Port Option come with 0.2 inch (5.1mm) of 3/8-32 UNEF-2A threads on the port. This option is available with all HFBR-0400, ST styled port components. Components with this option retain the same superior electrical/optical and mechanical performance as that of the base HFBR-0400 components. Refer to the HFBR-0400 data sheets for more information on electrical/optical performance and the HFBR-0400 Reliability data sheet for more information on mechanical durability.

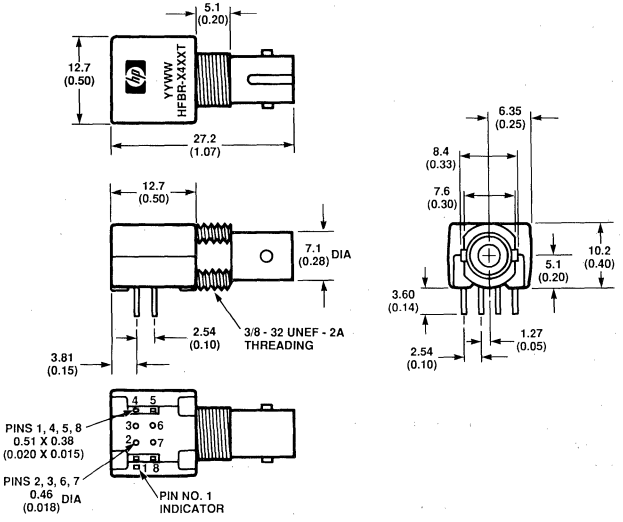
Panel Mounting

Low Cost Miniature Link components with the Threaded ST Port Option are suitable for panel mounting to chasis walls. The maximum wall thickness possible when using nuts and washers from the HFBR-4411 kit is 0.11 inch (2.8mm).



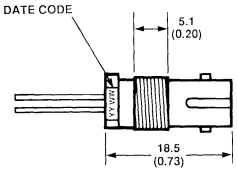
Package Outline

Housed Product

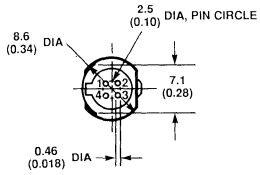


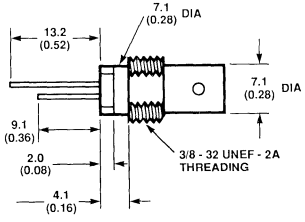
Package Outline

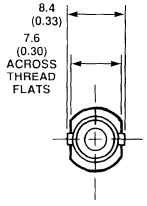
Port Product



NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES)







The HFBR-4411 kit consists of 100 nuts and 100 washers with dimensions as shown in Figure 1. These kits are available from HP or any authorized distribtor. Any standard size nut and washer will work, provided the total thickness of the wall, nut, and washer does not exceed 0.2 inch (5.1mm).

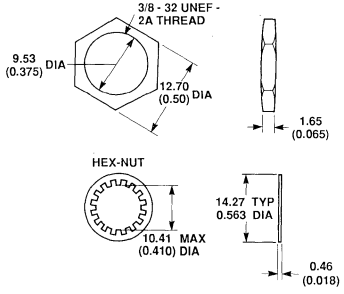
When preparing the chasis wall for panel mounting, use the mounting template in Figure 2. When tightening the nut, torque should not exceed 0.8 N-m (8.0 in-lb).

Ordering Information

To order the Threaded ST Port Option with a particular component, place a "T" after the base part number. For example, to order an HFBR-2416 with this option, order an HFBR-2416T.

This option is available with the following part numbers:

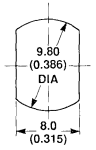
HFBR-1412	HFBR-2416
HFBR-1414	HFBR-2442
HFBR-1442	HFBR-2444
HFBR-1444	HFBR-2446
HFBR-1462	HFBR-2462
HFBR-1464	HFBR-2464
HFBR-2412	HFBR-2466
HFBR-2414	



NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES)

INTERNAL TOOTH LOCK WASHER

Figure 1. HFBR-4411 Mechanical Dimensions.



NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES)

Figure 2. Recommended Cut-out for Panel Mounting.

HEWLETT PACKARD

New

Single Chip 10BASE-FL Transceiver

Technical Data

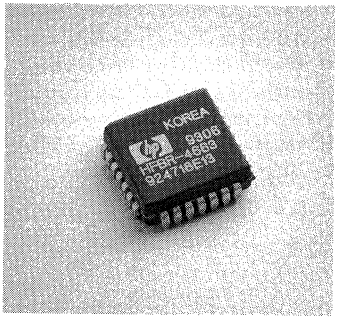
HFBR-4663

General Description

The HFBR-4663 Single Chip 10BASE-FL Transceiver is a highly integrated circuit for IEEE 802.3 10Base-FL transceivers. This product, when used with HP's fiber-optic transmitters and receivers (HFBR-14X4 and HFBR-2416), ensures compliance to the 10Base-FL Standard with a minimum number of external components and board space.

The HFBR-4663 offers a standard IEEE 802.3 AU interface that allows it to be directly connected to industry standard manchester encoder/ decoder chips or an AUI connector. The fiber-optic LED driver offers a current drive output that directly drives the HFBR-14X4 transmitter. The data quantizer section of the HFBR-4663 is directly compatible with the output of the HFBR-24X6 fiber-optic receiver and is capable of accepting input signals as low as 2 mVp-p with a 55 dB dynamic range.

The transmitter automatically inserts 1 MHz signal during idle time and removes this signal on reception. Low light is continuously monitored for both activity as well as power level. Five LED status indicators monitor error conditions as well as transmissions, receptions, and collisions.

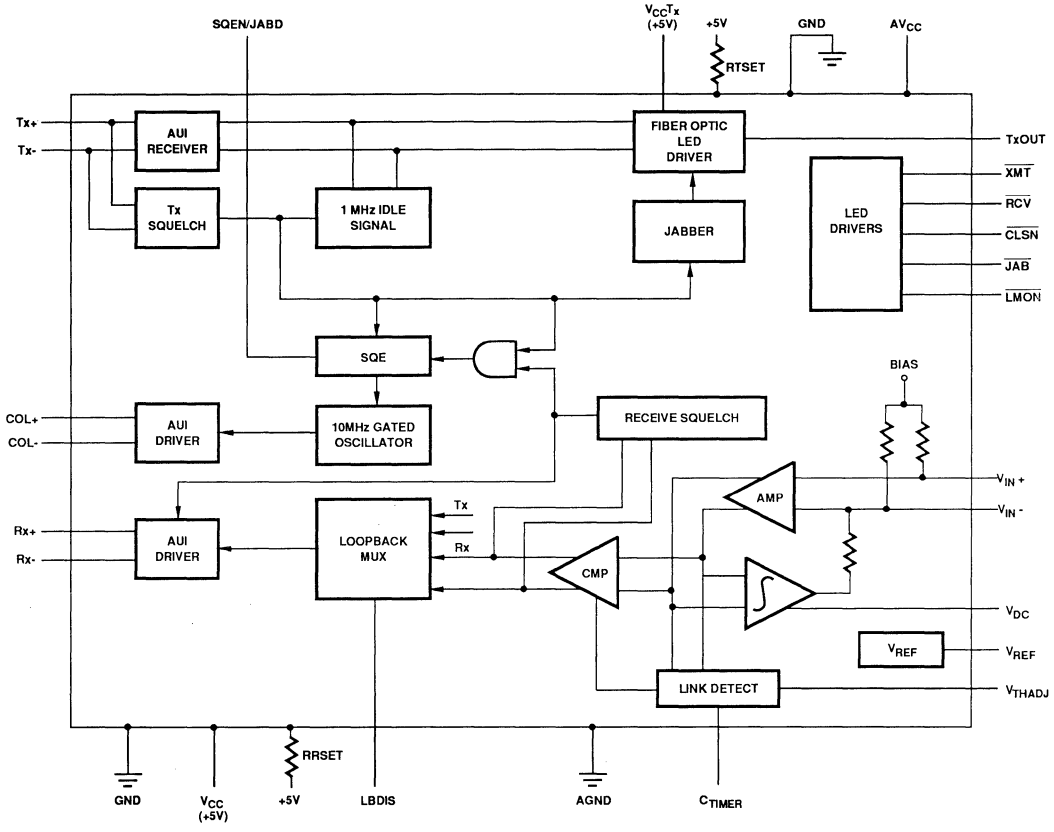


Features

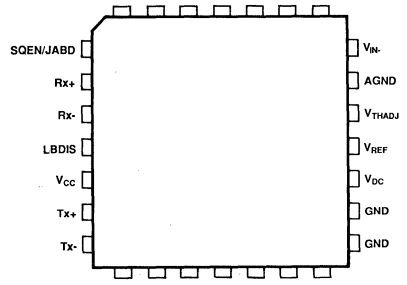
- **Single Chip Solution for 10BASE-FL Internal or External Medium Attachment Units (MAUs)**
- **Specifically Designed for Use with HFBR-14X4 and HFBR-24X6 Fiber-optic Transmitters and Receivers**
- **Incorporates an AU Interface**
- **Highly Stable Data Quantizer with 55 dB Input Dynamic Range**
- **Input Sensitivity as Low as 2 mV_{P-P}**
- **Current Driven Fiber Optic LED Driver for Accurate Launch Power**
- **Single +5 Volt Supply**
- **No Crystal or Clock Required**
- **Five Network Status LED Outputs**
- **Available in 28 Pin PCC Package**
- **Semi-Standard Option Available**

CAUTION: The small junction sizes inherent to the design of this component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Block Diagram



Pin Connectio



Pin Descripı

Pin	Name	Function
1	$\overline{\text{CLSN}}$	Indicates that a collision is taking place. Active low LED driver, open collector. Event is extended with internal timer for visibility.
2	COL+	Gated 10 MHz oscillation used to indicate a collision, SQE test, or jabber.
3	COL-	Balanced differential line driver outputs that meet AUI specifications.
4	C_{TIMER}	A capacitor from this pin to V_{CC} determines the Link Monitor response time.
5	SQEN/JABD	SQE Test Enable, jabber Disable. When tied low, SQE test is disabled, when tied high SQE test is enabled. When tied to 2.0 V both SQE test and jabber are disabled.
6	Rx+	Manchester encoded receive data output to the local device. Balanced
7	Rx-	differential line driver outputs that meet AUI specifications.
8	LBDIS	Loopback Disable. When this pin is tied to V_{CC}, the AUI transmit pair data is not looped back to the AUI receive pair, and collision is disabled. When this pin is tied to GND (normal operation) or left floating, the AUI transmit pair data is looped back to the AUI receiver pair, except during collision.
9	V_{CC}	+5 V power input.
10	Tx+	Balanced differential line receiver inputs that meet AUI specifications. These
11	Tx-	inputs may be transformer or capacitively coupled. The Tx input pins are internally DC biased for AC coupling.
12	RTSET	Sets the current driven output of the transmitter.
13	RRSET	A 1% 61.9 kΩ resistor tied from this pin to V_{CC} sets the biasing currents for internal nodes.
14	$\overline{\text{LMON}}$	Link Monitor "Low Light" LED status output. This pin is pulled low when the voltage on the V_{IN}+, V_{IN}- inputs exceed the minimum threshold set by the V_{THADJ} pin, and there are transitions on V_{IN}+, V_{IN}- indicating an idle signal or active data. If either the voltage on the V_{IN}+, V_{IN}- inputs fall below the minimum threshold or transitions cease on V_{IN}+, V_{IN}-, $\overline{\text{LMON}}$ will go high. Active low LED driver, open collector.

Pin Description (cont.)

Pin	Name	Function
15	$\overline{XMT}$	Indicates that transmission is taking place. Active low LED driver, open collector. Event is extended with internal timer for visibility.
16	$\overline{RCV}$	Indicates that the transceiver is receiving a frame from the optical input. Active low LED driver, open collector. Event is extended with internal timer for visibility.
17	$V_{CC}Tx$	+5 V supply for fiber optic LED driver.
18	TxOUT	Fiber optic LED driver output.
19	GND	Ground Reference.
20	GND	Ground Reference.
21	V_{DC}	An external capacitor on this pin integrates an error signal which nulls the offset of the input amplifier. If the DC feedback loop is not being used, this pin should be connected to V_{REF}.
22	V_{REF}	A 2.5 V reference with respect to GND.
23	V_{THADJ}	This input pin sets the link monitor threshold.
24	AGND	Analog Filtered Ground.
25	V_{IN}-	This input pin should be capacitively coupled to the input source or to filtered AV_{CC}. (The input resistance is approximately 1.3 kΩ.)
26	V_{IN}+	This input pin should be capacitively coupled to the input source or to filtered AV_{CC}. (The input resistance is approximately 1.3 kΩ.)
27	AV_{CC}	Analog Filtered +5 V.
28	$\overline{JAB}$	Jabber network status LED. When in the jabber state, this pin will be low and the transmitter will be disabled. In the jabber "OK" state this pin will be high. Active low LED, open collector.

Absolute Maximum Ratings[1]

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-65	+150	C
Operating Temperature	T_A	0	70	C
Lead Soldering Cycle Temperature			260	C
Lead Soldering Cycle Time			10	sec
Power Supply Voltage Range	V_{CC}	-0.3	6.0	V
Input Voltage Range	Digital Inputs (SQEN, LBDIS) Tx+, Tx-, V_{IN}+, V_{IN}-	-0.3 -0.3	6.0 6.0	V V
Input Current	RRSET, RTSET, JAB, CLSN, XMT, RCV, LMON		60	mA
Output Current	TxOUT		70	mA

Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
LED on Current		10		mA
RRSET		61.9 k ± 1%		Ω
RTSET		140 ± 1%		Ω

Electrical Characteristics

Unless otherwise specified, T_A = 0°C to 70°C, V_{CC} = V_{CC}Tx = 5 V ± 5% [2,3]

Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply Current I_{CC}: While Transmitting	V_{CC} = 5 V, RTSET = 140 Ω[4]			220	mA
LED Drivers: V_{CC}	I_{OL} = 10 mA[5]			0.8	V
Transmit Peak Output Current[6]	RTSET = 140 Ω	55	60	65	mA
Transmit Squelch Voltage Level (Tx+, Tx-)		-300	-250	-200	mV
Differential Output Voltage (Rx±, COL±)		±550		±1200	mV
Common Mode Output Voltage (Rx±, COL±)			4.0		V
Differential Output Voltage Imbalance (Rx±, COL±)				±40	mV
SQE/JABD	SQE Test Disable Both Disabled Both Enabled	 1.5 V_{CC} - 0.5		0.3 V_{CC} - 2	V V V
LBDIS Threshold	Disabled Enabled	V_{CC} - 0.1		 1	V V
Common Mode Voltage (Tx+, Tx-)			3.5		V
Common Mode Voltage (V_{IN}+, V_{IN}-)			1.65		V
Reference Voltage		2.35	2.45	2.55	V
V_{REF} Output Source Current				5	mA
Amplifier Gain			100		V/V
Input Signal Range		2		1600	mV_{P-P}
External Voltage at V_{THADJ} to Set V_{TH}		0.5		2.7	V
Input Offset	V_{DC} = V_{REF} (DC loop active)		3		mV
Input Referred Noise	50 MHz BW		25		µV
Input Resistance	V_{IN}+, V_{IN}-	0.8	1.3	2.0	kΩ
Input Bias Current of V_{THADJ}		-200	10	+200	µA
Input Threshold Voltage	V_{THADJ} = V_{REF}[7]	5	6	7	mV_{P-P}
Hysteresis			20		%

AC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
Transmit					
t_{TXNPW}	Transmit Turn-On Pulse Width		20		ns
t_{TXFPW}	Transmit Turn-Off Pulse Width from Data to Idle	400		2100	ns
t_{TXLP}	Transmit Loopback Start-up Delay			500	ns
t_{TXODY}	Transmit Turn-On Delay			150	ns
t_{TXIDF}	Transmit Idle Frequency	0.85		1.25	MHz
t_{TXDC}	Transmit Idle Duty Cycle	45		55	%
t_{TXSDY}	Transmit Steady State Propagation delay		15	50	ns
t_{TXJ}	Transmit Jitter into 31 Ω Load			±1.5	ns
Receive					
t_{RXSFT}	Receive Squelch Frequency Threshold	2.51		4.5	MHz
t_{RXODY}	Receive Turn-On Delay			285	ns
t_{RXFX}	Last Bit Received to Slow Decay Output	230	300		ns
t_{RXSDY}	Receive Steady State Propagation Delay		15	50	ns
t_{RXJ}	Receive Jitter			±1.5	ns
t_{AR}	Differential Output Rise Time 20% to 80% (Rx±, COL±)		4		ns
t_{AF}	Differential Output Fall Time 20% to 80% (Rx±, COL±)		4		ns
Collision					
t_{CPSQE}	Collision Present to SQE Assert	0		350	ns
t_{SQEXR}	Time for SQE to Deactivate After Collision	0		700	ns
t_{CLF}	Collision Frequency	8.5		11.5	MHz
t_{CLPDC}	Collision Pulse Duty Cycle	40	50	60	%
t_{SQEDY}	SQE Test Delay (Tx Inactive to SQE)	0.6		1.6	µs
t_{SQETD}	SQE Test Duration	0.5	1.0	1.5	µs
Jabber and LED Timing					
t_{JAD}	Jabber Activation Delay	20	70	150	ms
t_{JRT}	Jabber Reset Unjab Time	250	450	750	ms
t_{JSQE}	Delay from Outputs Disabled to Collision Oscillator On		100		ns
t_{LED}	$\overline{RCV}$, $\overline{CLSN}$, $\overline{XMT}$ On Time	8	16	32	ms
t_{LLPH}	Low Light Present to $\overline{LMON}$ High	3	5	10	µs
t_{LLCL}	Low Light Present to $\overline{LMON}$ Low	250		750	ms

Notes:
1. Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
2. Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
3. Low Duty Cycle pulse testing is performed at T_A.
4. This does not include the current from the AUI pull-down resistors, or LED status otuputs.
5. LED drivers can sink up to 20 mA, but V_{OL} will be higher.
6. Does not include pre-bias current for fiber optic LED which would typically be 3 mA.
7. Threshold for switching from Link Fail ot Link Pass (Low Light).

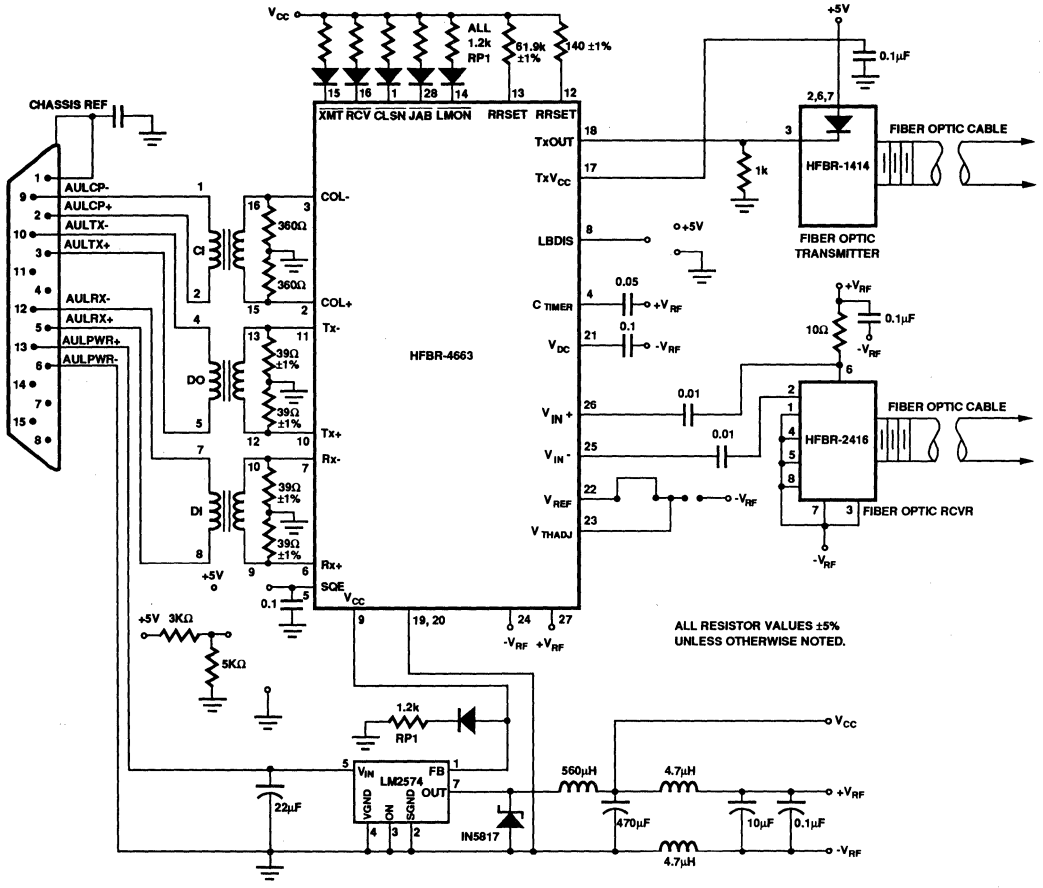


Figure 1. HFBR-4663 Schematic Diagram.

System Description

Figure 1 shows a schematic diagram of the HFBR-4663 in an internal or external 10BASE-FL MAU. On one side of the transceiver is the AU interface and the other is the fiber optic interface. The AU interface is AC coupled when used in an external transceiver or an internal transceiver. The AU interface for an external transceiver includes isolation transformers, some biasing resistors, and a voltage regulator for power.

The fiber optic side of the transceiver requires an external fiber optic transmitter and fiber optic receiver. The transmitter uses a current driven output that directly drives the fiber optic transmitter. The receive side of the transceiver accepts the data after passing through a fiber optic receiver, which consists of a module containing a pin diode and a transimpedance amplifier.

AU Interface

The AU interface consists of 3 pairs of signals, DO, CI and DI as shown in Figure 1. The DO pair contains transmit data from the DTE which is received by the transceiver and sent out onto the fiber optic cable. The DI pair contains valid data that has been either received from the fiber optic cable or looped back from the DO and output through the DI pair to the DTE. The CI pair indicates whether a collision has occurred. It is an output that oscillates at 10 MHz if a collision, jabber or SQE Test has taken place, otherwise it remains idle.

When the transceiver is external, these three pairs are AC coupled through isolation transformers, while an internal transceiver may be capacitively coupled. Tx+, Tx- is internally DC biased (shifted up in voltage) for the proper common mode input voltage.

The two 39 Ω 1% resistors (or one 78 Ω 1% resistor) tied to he Tx+ and Tx- pins will provide the proper termination. The CI and DI pair, which are output from the transceiver to the AUI cable, require 360 Ω pull down resistors when terminated with a 78 Ω load. However on a DTE card, CI and DI do not need 78 Ω terminating resistors. This also means that the pull down resistors on CI and DI can be 1 kΩ or greater depending upon the particular Manchester encoder/decoder chip used. Using higher value pull down resistors as in a DTE card will save power.

The AUI drivers are capable of driving the full 50 meters of cable length and have a rise and fall time of typically 4 ns. In the idle state, the outputs go to the same voltage to prevent DC standing current in the isolation transformers.

Transmission

The transmit function consists of detecting the presence of data from the AUI DO input (Tx+, Tx-) and driving that data onto the fiber optic LED transmitter. A positive signal on the Tx+ lead relative to the Tx- lead of the DO circuit will result in no current, hence the fiber optic LED is in a low light condition.

When Tx+ is more negative than Tx-, the HFBR-4663 will sink current into the chip and the fiber optic LED will emit light.

Before data will be transmitted onto the fiber optic cable from the AU interface, it must exceed the squelch requirements for the DO pair. The Tx squelch circuit serves the function of preventing any noise from being transmitted onto the fiber. This circuit rejects signals with pulse widths less than typically 20 ns (negative going), or with levels less than -250 mV. Once Tx squelch circuit has unsquelched, it looks for the start of idle signal to turn on the squelch circuit again. The transmitter turns on the squelch again when it receives an input signal at Tx+, Tx- that is more positive than -250 mV for more than approximately 180 ns.

At the start of a packet transmission, no more than 2 bits are received from the DO circuit and not transmitted onto the fiber optic cable. The difference between start-up delays (bit loss plus steady-state propagation delay) for any two packets that are separated by 9.6 µs or less will not exceed 200 ns.

Fiber Optic LED Driver

The output stage of the transmitter is a current mode switch which controls the output light by sinking current through the LED into the TxOUT pin. Once the current requirement for the LED is determined, the RTSET resistor is selected. The following equation is used to select the correct RTSET

resistor:

$$RTSET = \left(\frac{52\ mA}{IOUT}\right) 162\ \Omega$$

The transmitter enters the idle state when it detects start of idle on Tx+ and Tx- input pins. After detecting the start of idle, the transmitter switches to a 1 MHz output idle signal.

The output current is switched through the TxOUT pin during the on cycle and the V_{CC}Tx pin during the off cycle as shown in figure 2. Since the sum of the current in these two pins is constant, V_{CC}Tx should be connected as close as possible to the V_{CC} connection for the LED.

If not driving an optical LED directly, a differential output can be generated by tying resistors from V_{CC}Tx and TxOUT to V_{CC} as shown in Figure 3. The minimum voltage on these two pins should not be less than V_{CC} - 2 V.

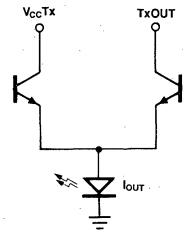


Figure 2. Fiber Optic LED Driver Structure.

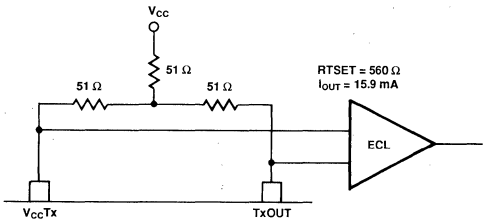


Figure 3. Converting Optical LED Driver Output to Differential ECL.

Reception

The input to the transceiver comes from a fiber optic receiver as shown in figure 1. At the start of packet reception no more than 2.7 bits are received from the fiber cable and not transmitted onto the DI circuit. The receive squelch will reject frequencies lower than 2.51 MHz.

While in the unsquelch state, the receive squelch circuit looks for the start of idle signal at the end of the packet. Start of idle occurs when the input signal remains idle for more than 160 ns. When start of idle is detected, the receive squelch circuit returns to the squelch state and the start of idle signal is output on the DI circuit (Rx+, Rx-).

Collision

Whenever the receiver and the transmitter are active at the same time the chip will activate the collision output, except when loopback is disabled (LBDIS = Vcc). The collision output is a differential square wave matching the AUI specifications and capable of driving a 78 Ω load. The frequency of the square wave is 10 MHz ± 15% with a 60/40 to 40/60 duty cycle. The collision oscillator also is activated during SQE Test and jabber.

Loopback

The loopback function emulates a 10BASE-T transceiver whereby the transmit data sent by the DTE is looped back over the AUI receive pair. Some LAN controllers use this loopback information to determine whether a MAU is connected by monitoring the carrier sense while transmitting. The software can use this loopback information to determine whether a MAU is connected to the DTE by checking the status of carrier sense after each packet transmission.

When data is received by the chip while transmitting, a collision condition exits. This will cause the collision oscillator to turn on and the data on the DI pair will follow V_{IN}+, V_{IN}-. After a collision is detected, the collision oscillator will remain on until either DO or V_{IN}+, V_{IN}- go idle.

Loopback can be disabled by strapping LBDIS to V_{CC}. In this mode the chip operates as a full duplex transmitter and receiver, and collision detection is disabled. A loopback through the transceiver can be accomplished by tying the fiber transmitter to the receiver.

SQE Test Function Signal Quality Error

The SQE test function allows the DTE to determine whether the collision detect circuitry is functional. After each transmission, during the inter packet gap time, the collision oscillator will be activated for typically 1 µs. The SQE test will not be activated if the chip is in the low light state, or the jabber on state.

For SQE to operate, the SQEN pin must be tied to V_{CC}. This allows the MAU to be interfaced to a DTE. The SQE test can be disabled by tying the SQEN pin to ground, for a repeater interface.

Jabber Function Requirements

The Jabber function prevents a babbling transmitter from bringing down the network. Within the transceiver is a Jabber timer that starts at the beginning of each transmission and resets at the end of each transmission. If the transmission lasts longer than 20 ms the jabber logic disables the transmitter, and turns on the collision signal COL+, COL-. When Tx+ and Tx- finally go idle, a second timer measures 0.5 seconds of idle time before the transmitter is enabled and collision is turned off. Even though the transmitter is disabled during jabber, the 1 MHz idle signal is still transmitted.

LED Drivers

The HFBR-4663 has five LED drivers. The LED driver pins are active low, and the LEDs are normally off (except for $\overline{\text{LMON}}$). The LEDs are tied to their respective pins through a 500 Ω resistor to 5 volts.

The $\overline{\text{XMT}}$, $\overline{\text{RCV}}$ and $\overline{\text{CLSN}}$ pins have pulse stretchers on them which enable the LEDs to be visible. When transmission or reception occurs, the LED $\overline{\text{XMT}}$, $\overline{\text{RCV}}$ or $\overline{\text{CLSN}}$ status pins will activate low for several milliseconds. If another transmit, receive or collision condition occurs before the timer expires, the LED timer will reset and restart the timing. Therefore rapid events will leave the LEDs continuously on. The $\overline{\text{JAB}}$ and $\overline{\text{LMON}}$ LEDs do not have pulse stretchers on them since their conditions occur long enough for the eye to see.

Low Light Condition

The $\overline{\text{LMON}}$ LED output is used to indicate a low light condition. $\overline{\text{LMON}}$ is activated low when both the receive power exceeds the Link Monitor threshold and there are transitions on V_{IN}+, V_{IN}- less than 3 µs apart. If either one of these conditions do not exist, $\overline{\text{LMON}}$ will go high.

Input Amplifier

The V_{IN}+, V_{IN}- input signal is fed into a limiting amplifier with a gain of about 100 and input resistance of 1.3 kΩ. Maximum sensitivity is achieved through the use of a DC restoration feedback loop and AC coupling the input. When AC coupled, the input DC bias voltage is set by an on-chip network at about 1.7 V. These coupling capacitors, in conjunction with the input impedance of the amplifier, establish a high pass filter with 3 dB corner frequency, f_L, at

$$f_L = \frac{1}{2\pi 1300C}$$

Since the amplifier has a differential input, two capacitors of equal value are required. If the signal driving the input is single ended, one of the coupling capacitors can be tied to AV_{CC} as shown in Figure 1.

The internal amplifier has a lowpass filter built-in to band limit the input signal which in turn will improve the signal noise ratio.

Although the input is AC coupled, the offset voltage *within* the amplifier will be present at the amplifier's output. This is represented by V_{OS} in Figure 4. In order to reduce this error a DC feedback loop is incorporated. This negative feedback loop nulls the offset voltage, forcing V_{OS} to be zero. Although the capacitor on V_{DC} is non-critical, the pole it creates can affect the stability of the feedback loop. To avoid stability problems, the value of this capacitor should be at least 10 times larger than the input coupling capacitors.

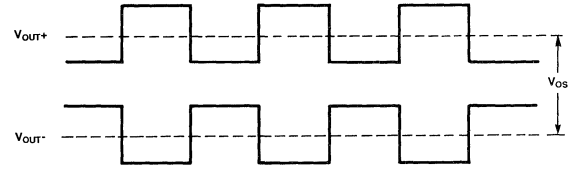


Figure 4.

The comparator is a high-speed differential zero crossing detector that slices and accurately digitizes the receive signal. The output of the comparator is fed in parallel into both the receive squelch circuit and the loopback MUX.

Link Detect Circuitry and Low Light

The link detect circuit monitors the input signal and determines when the input falls below a preset voltage level. When the input falls below a preset voltage, the HFBR-4663 goes into the Low Light state. In the Low Light state the transmitter is disabled, but continues sending the I MHz idle signal, the loopback is disabled, the receiver is disabled and the $\overline{\text{LMON}}$ LED pin goes to high shutting off the $\overline{\text{LMON}}$ LED. To return to the Link Pass state, the optical receiver power must be 20% higher than the shut-off state. This built-in hysteresis adds stability to the Link Monitor circuit. Once the receiver power threshold is exceeded, the HFBR-4663 waits 250 ms to 750 ms, then checks to see that Tx+, Tx- is idle and no data is being received before re-enabling the transmitter, receiver, loopback circuit, and lighting up the $\overline{\text{LMON}}$ LED.

The V_{THADJ} pin is used to adjust the sensitivity of the receiver. The HFBR-4663 is capable of exceeding the 10BASE-FL specifications for sensitivity. The sensitivity is dependent on the layout of the PC board. A good low noise layout will exceed the 10BASE-FL specifications, while a poor layout will fail to meet the sensitivity and BER spec.

The threshold generator shifts the reference voltage at V_{THADJ} through a circuit which has a temperature coefficient matching that of the limiting amplifier. The relationship between the V_{THADJ} and the V_{TH} (the peak to peak input threshold) is:

$$V_{THADJ} = 408\ V_{TH} \quad (2)$$

In a 10BASE-FL receiver, there must be less than 1 x 10^{-9} bit errors at a receive power level of -32.5 dBm average. One procedure to determine the sensitivity of a receiver is to start at the lowest optical power level and gradually increase the optical power until the BER is met. In this case the Link Detect circuit must not disable the receiver (i.e. V_{THADJ} should be tied to Ground). Once the sensitivity of the receiver is determined, V_{THADJ} can be set just above the power level that meets the BER specification. This way the receiver will shut-off before the BER is exceeded.

For 10-BASE-FL, V_{THADJ} can be tied directly to V_{REF}. However if greater sensitivity is required the circuit in Figure 5 can be used to adjust the V_{THADJ} voltage. Even if V_{REF} is tied to V_{THADJ}, it is a good idea to layout a board with these two resistors available. This will allow potential future adjustments without board revisions.

The response time of the Link Detect circuit is set by the C_{TIMER} pin. Starting from the link off state the link can be switched on if the input exceeds the set threshold for a time given by:

$$T = \frac{C_{TIMER} \times 0.7\ V}{700\ \mu A}$$

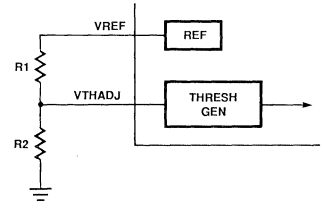


Figure 5.

To switch the link from on to off, the above time will be doubled. A value of 0.05 µF will meet the 10BASE-FL specifications.

Differences between 10BASE-FL and FOIRL

10BASE-FL is an improved version of the original FOIRL standard. The 10BASE-FL standard allows backward compatibility of a 10BASE-FL transceiver with a FOIRL transceiver. The main improvements incorporated into 10BASE-FL are that it can attach to a DTE by adding the SQE test, and the distance has been increased from 1 km to 2 km. The other differences are much more subtle.

1. SQE Test: The FOIRL standard did not include the option of attaching a fiber transceiver to a DTE. Adding the SQE test to 10BASE-FL enables a 10BASE-FL transceiver to attach to a DTE.

2. 0 to at Least 2 Km Distance: The FOIRL standard specifies a 1 km distance while 10BASE-FL specifies 2 km. The additional 1 km distance for 10BASE-FL comes from an increased flux budget for the cable of 3.5 dB. This 3.5 dB increase came from an increase of 2.5 dB sensitivity for the receiver and a 1 dB improvement for the transmitter. The following table illustrates the transmit and receive power requirements for the two standards. Note: FOIRL specifies optical power in peak and 10BASE-FL specifies it in average. Subtracting 3 dB from peak will give the average. In the table below the FOIRL specifications were converted from peak to average power.

3. MAU State Diagrams are Different: The state diagrams for 10BASE-FL are similar to 10BASE-T, while the state diagrams for FOIRL are slightly different. The differences are in the AUI loopback, and in the link integrity function.

AUI Loopback - In 10BASE-FL the DO to DI loopback is always disabled during a collision, and optical receive data is passed through to DI. For FOIRL there are some cases where loopback continues (i.e. DO looped to DI) during a collision, and others where loopback is disabled during a collision. 10BASE-FL is identical to 10BASE-T in this case. Please refer to the IEEE standards for greater detail.

Link Integrity - 10BASE-FL adds an additional state to the Link Integrity Test function that will not allow an exit from the Low Light State until both the transmitter and receiver are idle. In FOIRL, it is possible to exit from the Low Light State while still receiving data.

MAU Timing Differences - The timing differences between 10BASE-FL and FOIRL relate to propagation delays, start-up delays, and collision deassert delays. The following table provides the details of these parameters.

Timing Parameter Differences	FOIRL (BIT Times)	10BASEFL (BIT Times)
ORD input to input on DI		
Steady State Prop Delay	0.5	2
Start-Up Delay	3.5	5
Output on DO to OTD_output		
Steady State Prop Delay	0.5	2
Start-Up Delay	3.5	5
Collision Deassert to SQE Deassert minimum	**4.5**	**0**

OTD - Optical Transmit Data
ORD - Optical Receive Data
DI, DO, CI - AU Interface Signals

Transmit/Receive Average Power	Min.	Max.	Conditions
FOIRL			
Transmitter	-12 dBm	-21 dBm	
Receiver	-12 dBm	-30 dBm	BER < 10^{-10}
10BASE-FL			
Transmitter	-12 dBm	-20 dBm	
Receiver	-12 dBm	-32.5 dBm	BER < 10^{-9}

Timing Diagrams

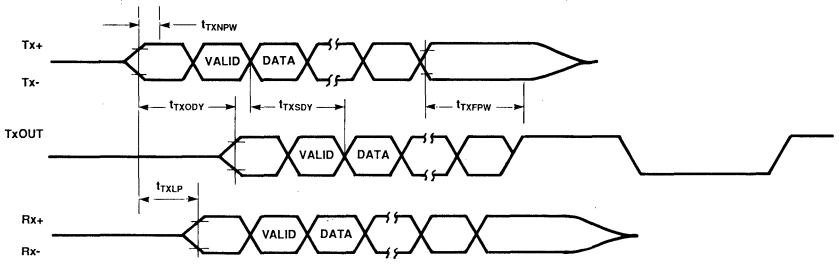


Figure 6. Transmit and Loopback Timing.

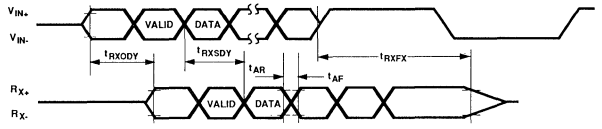


Figure 7. Receive Timing.

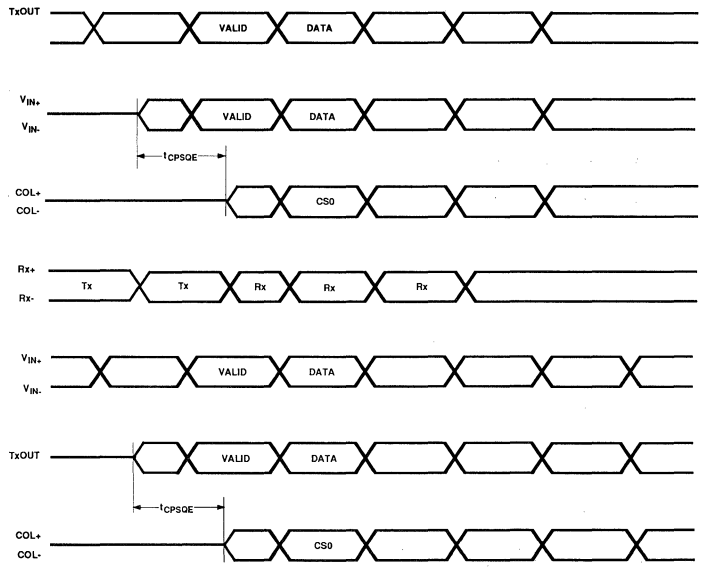


Figure 8. Collision Timing.

Timing Diagrams

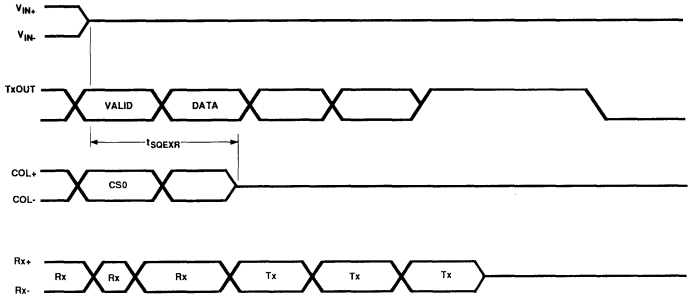


Figure 9. Collision Timing.

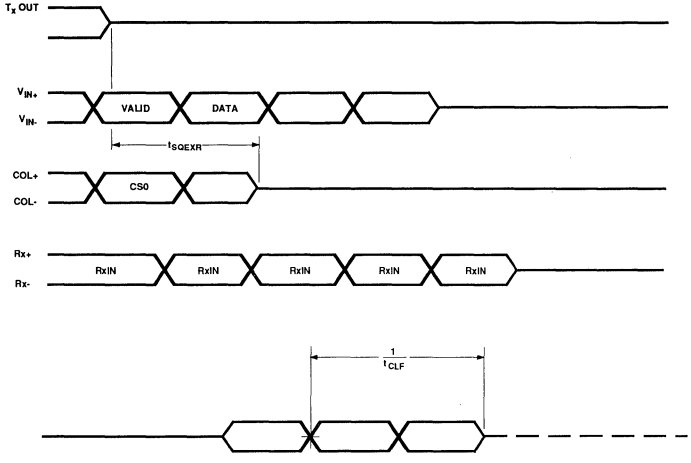


Figure 10. Collision Timing.

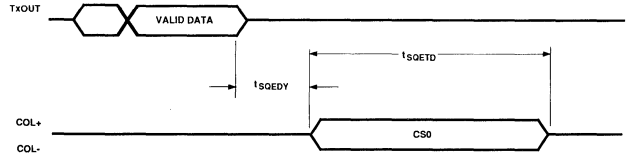


Figure 11. SQE Timing.

Timing Diagrams

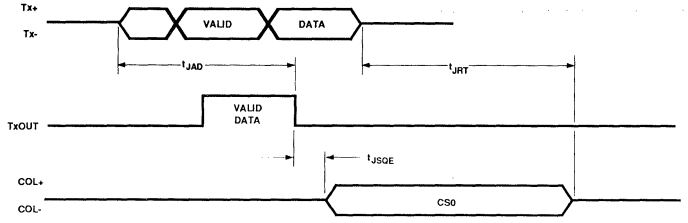


Figure 12. Jabber Timing.

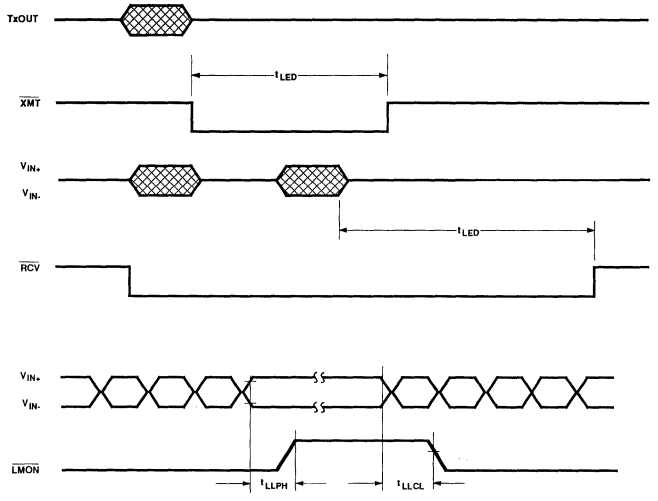


Figure 13. LED Timing.

HEWLETT PACKARD

New

1300 nm Fiber Optic Transmitter and Receiver

Technical Data

HFBR-0300 Series:
HFBR-1312T Transmitter
HFBR-2316T Receiver

Features

- **Low Cost Fiber Optic Link**
- **Signal Rates over 155 Megabaud**
- **1300 nm Wavelength**
- **Link Distances over 5 km**
- **Dual-in-line Package Panel-Mountable ST* Connector Receptacles**
- **Auto-Insertable and Wave-Solderable**
- **Specified with 62.5/125 µm and 50/125 µm Fiber**
- **Compatible with HFBR-0400 Series**

Applications

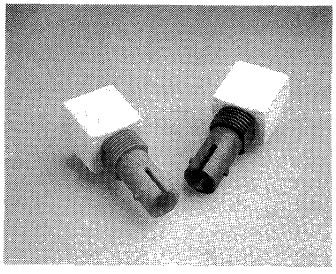
- **Low Cost FDDI Links**
- **Desktop Links for High Speed LANs**
- **Distance Extension Links**
- **Telecom Switch Systems**
- **TAXIchip® Compatible**

Description

The HFBR-0300 Series is designed to provide the most cost-effective 1300 nm fiber optic links for a wide variety of data communication applications from low-speed distance extenders up to SONET OC-3 signal rates. The optical performance of the transmitter and receiver are compatible with the specifications of the FDDI Low Cost PMD. Pinouts identical to Hewlett-Packard HFBR-0400 Series allow designers to easily upgrade their 820 nm links for farther distance. The transmitter and receiver are compatible with two popular optical fiber sizes: 50/125 µm and 62.5/125 µm diameter. This allows flexibility in choosing a fiber size. The 1300 nm wavelength is in the lower dispersion and attenuation region of fiber, and provides longer distance capabilities than 820 nm LED technology. Typical distance capabilities are 2 km at 125 MBd and 5 km at 32 MBd.

Transmitter

The HFBR-1312T fiber optic transmitter contains a 1300 nm InGaAsP light emitting diode capable of efficiently launching optical power into 50/125 µm and 62.5/125 µm diameter fiber. The HFBR-1312T is compatible



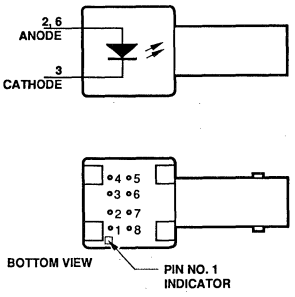
with the electro-optical specifications of the ANSI X3T9.5 Low-Cost PMD when used with the appropriate LED driver circuit. Converting the interface circuit from a HFBR-14XX 820 nm transmitter to the HFBR-1312T requires only the removal of a few passive components.

Receiver

The HFBR-2316T receiver contains an InGaAs PIN photodiode and a low-noise transimpedance preamplifier that operate in the 1300 nm wavelength region. The HFBR-2316T receives an optical signal and converts it to an analog voltage. The buffered output is an emitter-follower, with

*ST is a registered trademark of AT&T Lightguide Cable Connectors

HFBR-1312T Transmitter

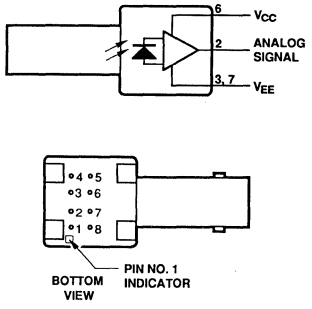


PIN	FUNCTION
1†	N.C.
2	ANODE
3	CATHODE
4†	N.C.
5†	N.C.
6	ANODE
7*	N.C.
8†	N.C.

* PIN 7 IS ELECTRICALLY ISOLATED FROM PINS 1, 4, 5, AND 8, BUT IS CONNECTED TO THE HEADER.

† PINS 1, 4, 5, AND 8 ARE ISOLATED FROM THE INTERNAL CIRCUITRY, BUT ARE ELECTRICALLY CONNECTED TO EACH OTHER.

HFBR-2316T Receiver

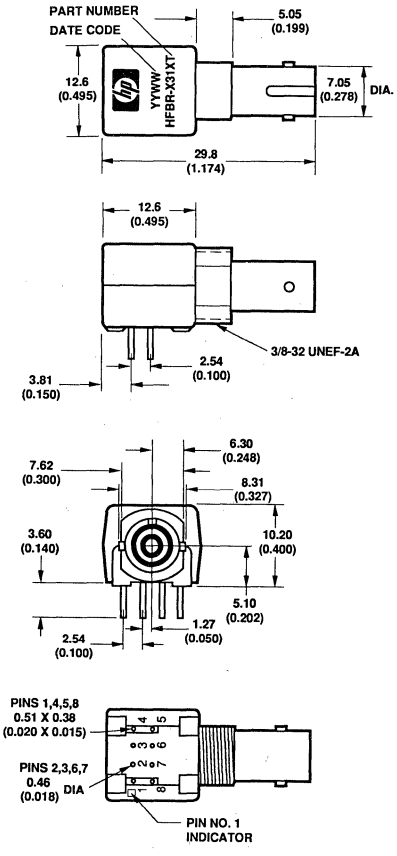


PIN	FUNCTION
1†	N.C.
2	SIGNAL
3*	VEE
4†	N.C.
5†	N.C.
6	VCC
7*	VEE
8†	N.C.

* PINS 3 AND 7 ARE ELECTRICALLY CONNECTED TO THE HEADER.

† PINS 1, 4, 5, AND 8 ARE ISOLATED FROM THE INTERNAL CIRCUITRY, BUT ARE ELECTRICALLY CONNECTED TO EACH OTHER.

HFBR-0300 Series Mechanical Dimensions



frequency response from DC to typically 125 MHz. Low-cost external components can be used to convert the analog output to logic compatible signal levels for a variety of data formats and data rates. The HFBR-2316T is compatible with the electro-optical specifications of the ANSI X3T9.5 Low-Cost PMD when used with the appropriate interface circuitry. The HFBR-2316T is pin compatible with HFBR-24X6 receivers and can be used to extend the distance of an existing application by substituting the HFBR-2316T for the HFBR-2416.

Package Information

HFBR-0300 Series transmitters and receivers are housed is a dual-in-line package made of high strength, heat resistant, chemically resistant, and UL V-0 flame retardant plastic. Transmitters are identified by the brown port color; receivers have black ports. The package is auto-insertable and wave solderable for high volume production applications.

Note: The "T" in the product numbers indicates a Threaded ST connector (panel mountable), for both transmitter and receiver.

Handling and Design Information

When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean. Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air is often sufficient to remove particles of dirt; methanol on a cotton swab also works well.

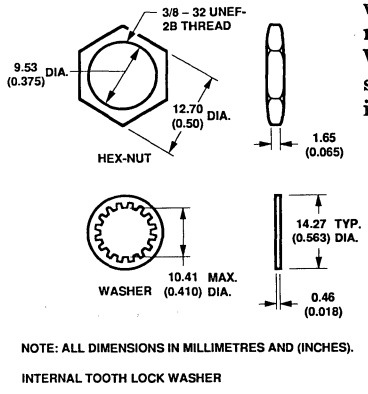


Figure 1. HFBR-4411 Mechanical Dimensions.

Panel Mounting Hardware

The HFBR-4411 kit consists of 100 nuts and 100 washers with dimensions as shown in Figure 1. These kits are available from HP or any authorized distributor. Any standard size nut and washer will work, provided the total thickness of the wall, nut, and washer does not exceed 0.2 inch (5.1mm).

When preparing the chassis wall for panel mounting, use the mounting template in Figure 2. When tightening the nut, torque should not exceed 0.8 N-m (8.0 in-lb).

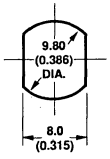


Figure 2. Recommended Cut-out for Panel Mounting.

Recommended Chemicals for Cleaning/ Degreasing HFBR-0300 Products

Alcohols (methyl, isopropyl, isobutyl)
Aliphatics (hexane, heptane)
Other (soap solution, naphtha)

Do not use partially halogenated hydrocarbons (such as 1.1.1 trichloroethane), ketones (such as MEK), acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride, or N-methylpyrolldone. Also, HP does not recommend the use of cleaners that use halogenated hydrocarbons because of their potential environmental harm.

FIBER OPTICS

HFBR-1312T Transmitter Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Reference
Storage Temperature	T_S	-55	85	°C	
Operating Temperature	T_A	-40	85	°C	
Lead Soldering Cycle Temperature			260	°C	Note 8
Lead Soldering Cycle Time			10	sec	
Forward Input Current DC	I_{FDC}		100	mA	
Reverse Input Voltage	V_R		1	V	

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

HFBR-1312T Transmitter Electrical/Optical Characteristics

0 to 70°C unless otherwise specified

Parameter	Symbol	Min.	Typ.[1]	Max.	Unit	Condition	Ref.
Forward Voltage	V_F	1.1	1.4	1.7	V	I_F = 75 mA	Fig. 1
			1.5			I_F = 100 mA	
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-1.5		mV/°C	I_F = 75 - 100 mA	
Reverse Input Voltage	V_R	1	4		V	I_R = 100 µA	
Center Emission Wavelength	λ_C	1270	1300	1370	nm		
Full Width Half Maximum	FWHM		130	185	nm		
Diode Capacitance	C_T		16		pF	V_F = 0 V, f = 1 MHz	
Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-0.03		dB/°C	I_F = 75 - 100 mA DC	
Thermal Resistance	Θ_{JA}		260		°C/W		Note 2

HFBR-1312T Transmitter Output Optical Power and Dynamic Characteristics

Parameter	Symbol	Min.	Typ.[1]	Max.	Unit	Condition		Ref.
						T_A	$I_{F,\ peak}$	
Average Power 62.5/125 µm NA = 0.275	P_{T62}	-19.0	-17.0	-15.5	dBm	25°C	75 mA	Notes 3, 4, 5 Fig. 2
		-20.5		-14.5		0-70°C	75 mA	
		-18.5	-16.5	-15.0		25°C	100 mA	
		-20.0		-14.0		0-70°C	100 mA	
Average Power 50/125 µm NA = 0.20	P_{T50}	-22.5	-20.0	-17.5	dBm	25°C	75 mA	Notes 3, 4, 5 Fig. 2
		-24.0		-16.5		0-70°C	75 mA	
		-22.0	-19.5	-17.0		25°C	100 mA	
		-23.5		-16.0		0-70°C	100 mA	
Optical Overshoot	OS		5	10	%	0-70°C	75 mA	Note 6 Fig. 3
Rise Time	t_r		1.8	4.0	ns	0-70°C	75 mA	Note 7 Fig. 3
Fall Time	t_f		2.2	4.0	ns	0-70°C	75 mA	Note 7 Fig. 3

Notes:

1. Typical data are at T_A = 25°C.
2. Thermal resistance is measured with the transmitter coupled to a connector assembly and mounted on a printed circuit board; $\Theta_{JC} < \Theta_{JA}$.
3. Optical power is measured with a large area detector at the end of 1 meter of mode stripped cable, with an ST* precision ceramic ferrule (MIL-STD-83522/13), which approximates a standard test connector. Average power measurements are made at 12.5 MHz with a 50% duty cycle drive current of 0 to $I_{F,peak}$; $I_{F,average} = I_{F,peak}/2$. Peak optical power is 3 dB higher than average optical power.
4. When changing from µW to dBm, the optical power is referenced to 1 mW (1000 µW).
   Optical power P(dBm) = 10*log[P(µW)/1000µW].
5. Fiber NA is measured at the end of 2 meters of mode stripped fiber using the far-field pattern. NA is defined as the sine of the half angle, determined at 5% of the peak intensity point. When using other manufacturer's fiber cable, results will vary due to differing NA values and test methods.
6. Overshoot is measured as a percentage of the peak amplitude of the optical waveform to the 100% amplitude level. The 100% amplitude level is determined at the end of a 40 ns pulse, 50% duty cycle. This will ensure that ringing and other noise sources have been eliminated.
7. Optical rise and fall times are measured from 10% to 90% with 62.5/125 µm fiber. LED response time with recommended test circuit (Figure 3) at 25 MHz, 50% duty cycle.
8. 2.0 mm from where leads enter case.

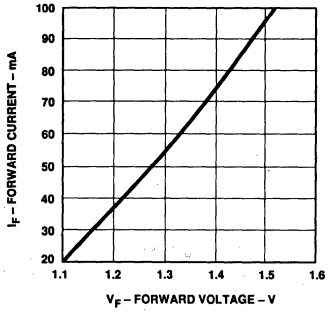


Figure 1. Typical Forward Voltage and Current Characteristics.

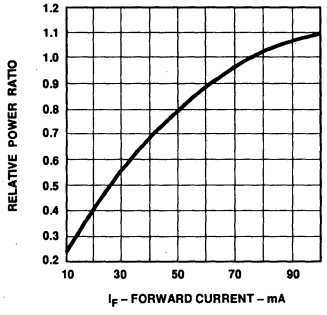


Figure 2. Normalized Transmitter Output Power vs. Forward Current.

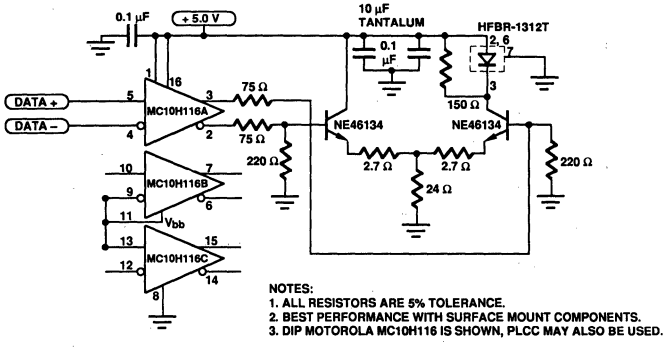


Figure 3. Recommended Transmitter Drive and Test Circuit.

HFBR-2316T Receiver Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Reference
Storage Temperature	T_S	-55	85	°C	
Operating Temperature	T_A	-40	+85	°C	
Lead Soldering Temperature			260	°C	Note 1
Cycle Time			10	s	
Signal Pin Voltage	V_O	-0.5	V_{CC}	V	
Supply Voltage	V_{CC} - V_{EE}	-0.5	6.0	V	Note 2
Ouptut Current	I_O		25	mA	

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

HFBR-2316T Receiver Electrical/Optical and Dynamic Characteristics

0 to 70°C; 4.75 V < V_{CC} - V_{EE} < 5.25 V; power supply m ust be filtered (see note 2).

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit	Condition	Ref.
Responsitivity	R_P	6.5	13	19	mV/μW	λ_p = 1300 nm, 50 MHz	Note 4 Fig. 1, 5
RMS Output Noise Voltage	V_{NO}		0.4	0.59	mV_{RMS}	100 MHz bandwidth, P_R = 0 μW	Note 5 Fig. 2
				1.0	mV_{RMS}	Unfiltered Bandwidth P_R = 0 μW	
Equivalent Optical Noise Input Power (RMS)	$P_{N,RMS}$		-45	-41.5	dBm	@ 100 MHz, P_R = 0 μW	Note 5
			0.032	0.071	μW		
Peak Input Optical Power	P_R			-11.0	dBm	50 MHz, 1 ns PWD	Note 6 Fig. 3
				80	μW		
Output Resistance	R_O		30		Ohm	f = 50 MHz	
DC Output Voltage	$V_{O,DC}$	0.8	1.8	2.6	V	V_{CC} = 5 V, V_{EE} = 0 V P_R = 0 μW	
Supply Current	I_{CC}		9	15	mA	R_{LOAD} = ∞	
Electrical Bandwidth	BW_E	75	125		MHz	-3 dB electrical	Note 7
Bandwidth * Rise Time Product			0.41		Hz *s		
Electrical Rise, Fall Times, 10-90%	t_r,t_f		3.3	5.3	ns	P_R = -15 dBm peak, @ 50 MHz	Note 8 Fig. 4
Pulse-Width Distortion	PWD		0.4	1.0	ns	P_R = -11 dBm, peak	Note 6,9 Fig. 3
Overshoot			2		%	P_R = -15 dBm, peak	Note 10

Notes:

1. 2.0 mm from where leads enter case.
2. The signal output is referred to V_{CC}, and does not reject noise from the V_{CC} power supply. Consequently, the V_{CC} power supply must be filtered. The recommended power supply is +5 V on V_{CC} for typical usage with +5 V ECL logic. A -5 V power supply on V_{EE} is used for test purposes to minimize power supply noise.
3. Typical specifications are for operation at T_A = 25°C and V_{CC} = +5 V_{DC}.
4. The test circuit layout should be in accordance with good high frequency circuit design techniques.
5. Measured with a 9-pole "brick wall" low-pass filter [Mini-Circuits™, BLP-100*] with -3 dB bandwidth of 100 MHz.
6. -11.0 dBm is the maximum peak input optical power for which pulse-width distortion is less than 1 ns.
7. Electrical bandwidth is the frequency where the responsivity is -3 dB (electrical) below the responsivity measured at 50 MHz.
8. The specified rise and fall times are referenced to a fast square wave optical source. Rise and fall times measured using an LED optical source with a 2.0 ns rise and fall time (such as the HFBR-1312T) will be approximately 0.6 ns longer than the specified rise and fall times. E.g.: measured $t_{r,f} \simeq [(\text{specified } t_{r,f})^2 + (\text{test source optical } t_{r,f})^2]^{1/2}$.
9. 10 ns pulse width, 50% duty cycle, at the 50% amplitude point of the waveform.
10. Percent overshoot is defined as: $((V_{PK} - V_{100\%})/V_{100\%}) \times 100\%$. The overshoot is typically 2% with an input optical rise time $\leq$ 1.5 ns.
11. The bandwidth*risetime product is typically 0.41 because the HFBR-2316T has a second-order bandwidth limiting characteristic.

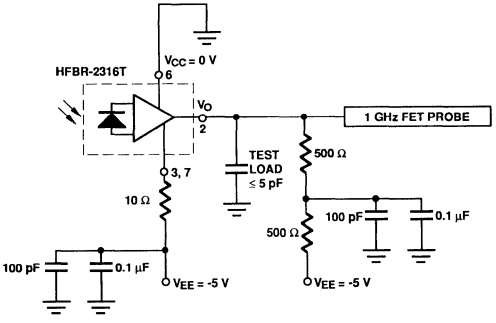


Figure 1. HFBR-2316T Receiver Test Circuit.

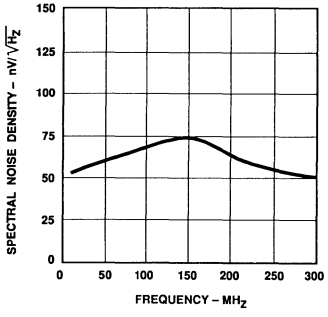


Figure 2. Typical Output Spectral Noise Density vs. Frequency.

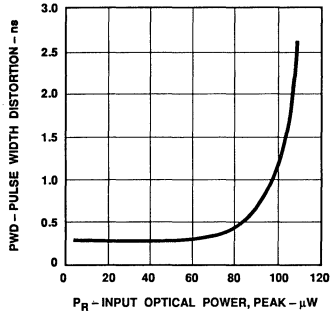


Figure 3. Typical Pulse Width Distortion vs. Peak Input Power.

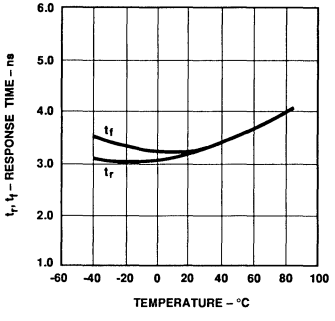


Figure 4. Typical Rise and Fall Times vs. Temperature.

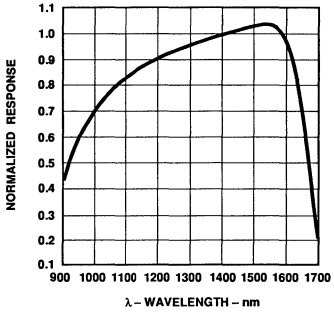
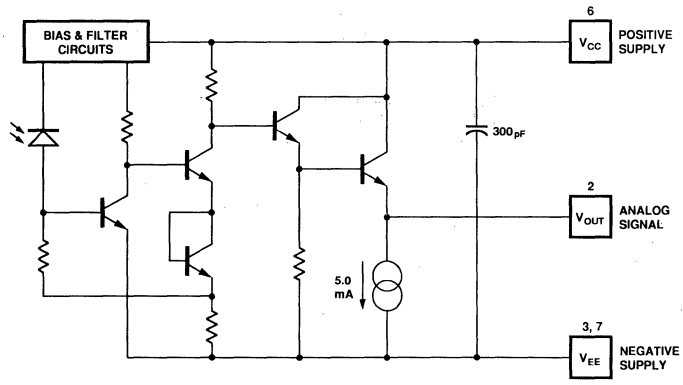


Figure 5. Normalized Receiver Spectral Response.

*Mini-Circuits Division of Scientific Components Corporation

HFBR-2316T Simplified Schematic Diagram



HEWLETT PACKARD

FDDI 1300 nm Transceiver

Technical Data

HFBR-5101
new **HFBR-5102**

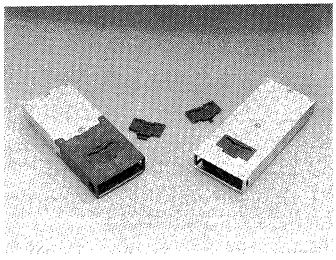
Features

- **Full Compliance with FDDI PMD Standard**
- **Multisourced Package Style with:**
  - 2 X 11 Pins
  - User Installable Key
- **Available with Either Metal or Plastic Media Interface Connector/ Receptacle**
- **Suitable for Use in Equipment Regulated for:**
  - VCCI Class 2, CISPR 22B, CENELEC 55022B and FCC Class B
  - Immunity to EMI/RFI
  - Immunity to ESD
- **Wavesolder and Aqueous Wash Compatible**
- **Single +5 V Power Supply**
- **Shifted ECL Logic Interface Directly Compatible with FDDI PHY Circuits**
- **Compatible with TAXIchip™* Encode/ Decode Circuits**

*TAXIchip™ is a trademark of Advanced Micro Devices, Inc.

Applications

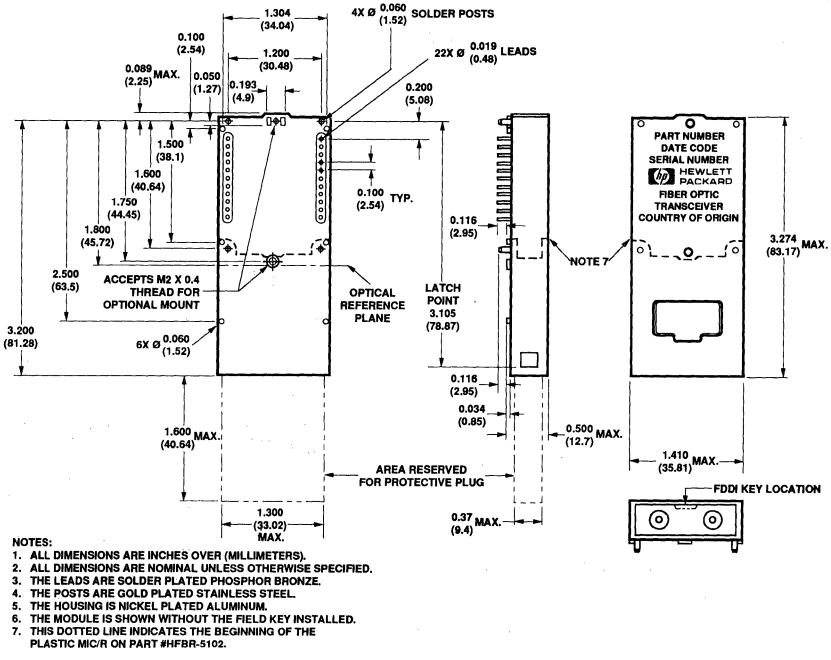
- **FDDI Single or Dual Attachment Stations**
- **Local ATM Interfaces at 125 MBd, 140 MBd, 155 MBd**
- **Fiber Channel Interfaces at 133 MBd**
- **Proprietary Interfaces**



Description

The FDDI transceiver described in this data sheet is a member of a growing family of 1300 nm technology fiber optic products available from Hewlett-Packard. FDDI is an acronym for the Fiber Distributed Data Interface local area network standard. This FDDI transceiver product supplies the performance necessary for the system designer who seeks to develop equipment with fully compliant FDDI interfaces per the FDDI Physical Layer Medium Dependent (PMD) standard. This standard has been approved as an International Standard, ISO/IEC 9314-3, and an American National Standard, ANSI X3.166-1990. The performance of this Hewlett-Packard transceiver is guaranteed over the operating temperature and power supply voltage ranges found in most commercial equipment. Sufficient margin exists over the FDDI PMD requirements to allow for substantial equipment mission-life and configuration flexibility.

Hewlett-Packard is a vertically integrated supplier. The 1300 nm LED and PIN devices along with the three custom bipolar integrated circuits (ICs) used in these products have been developed and manufactured by Hewlett-Packard. The transceiver assembly and testing is performed in facilities wholly-owned and operated by Hewlett-Packard.



NOTES:
1. ALL DIMENSIONS ARE INCHES OVER (MILLIMETERS).
2. ALL DIMENSIONS ARE NOMINAL UNLESS OTHERWISE SPECIFIED.
3. THE LEADS ARE SOLDER PLATED PHOSPHOR BRONZE.
4. THE POSTS ARE GOLD PLATED STAINLESS STEEL.
5. THE HOUSING IS NICKEL PLATED ALUMINUM.
6. THE MODULE IS SHOWN WITHOUT THE FIELD KEY INSTALLED.
7. THIS DOTTED LINE INDICATES THE BEGINNING OF THE PLASTIC MIC/R ON PART #HFBR-5102.

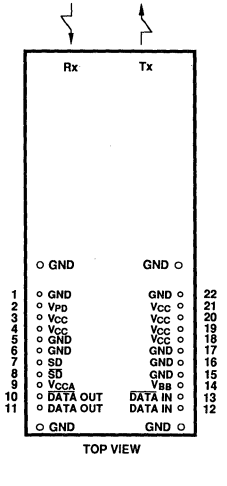
Figure 1. Outline Drawing. HFBR-5101 – Metal MIC/R, HFBR-5102 – Plastic MIC/R

Transmitter Section

The transmitter section of the FDDI transceiver uses a 1300 nm InGaAsP LED and a single custom silicon bipolar LED driver integrated circuit. The LED has an integral etched lens that provides efficient coupling to multimode fibers when combined with the Hewlett-Packard custom optical subassembly. The driver circuit provides temperature compensation for a predictable output optical power over the recommended operating temperature range. It also maintains a steady power supply current due to internal loads which conduct the LED drive current when logic "0"s are being transmitted to minimize creation of high frequency noise on power supply lines. The data input to the transmitter section is differential, 100K ECL compatible, referenced (shifted) to operate from a +5 volt supply.

Receiver Section

The receiver section of the FDDI transceiver uses a 1300 nm InGaAs PIN photodiode and two custom silicon bipolar integrated circuits. The PIN is a planar top-illuminated device which provides ease of assembly into the Hewlett-Packard custom optical subassembly. The preamplifier IC is mounted in the optical subassembly with the PIN detector to maximize the receiver sensitivity. This sensitivity is guaranteed over a wide time-window in the data output eye-pattern. The second IC, a quantizer, provides the final pulse shaping for the logic



GND IS BOTH SIGNAL AND CASE GROUND

Figure 2. Pin Assignments.

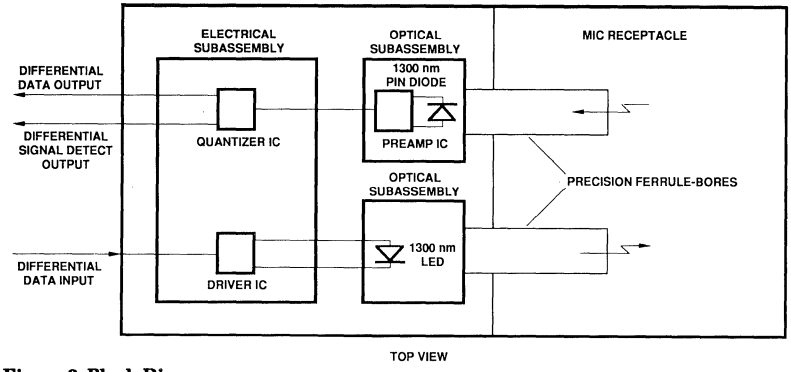


Figure 3. Block Diagram.

output and the Signal Detect function. Both the Data and Signal Detect logic outputs are differential, 100K ECL compatible, referenced (shifted) to a +5 volt power supply.

A strong attribute of the receiver section of this transceiver is the ability to provide excellent sensitivity over a wide output data eye-opening. A wide window time-width (eye-opening) that results in only a small sensitivity change from the center symbol time-position relaxes strict timing requirements on the FDDI PHY clock recovery circuitry. The receiver sensitivity is guaranteed over a wide 4.6 ns window time-width under minimum input jitter conditions. This wide window time-width ensures that under maximum FDDI PMD worst case Active Input Interface peak-to-peak jitter conditions of DCD (1.0 ns), DDJ (1.2 ns), and RJ (0.76 ns), the receiver will maintain a minimum 2.13 ns window time-width for a clock recovery circuit per the example in the FDDI PMD Annex E. Receiver tests using a wider window time-width opening along with corresponding smaller input jitter conditions are equivalent to testing with the larger worst case FDDI PMD input jitter conditions, and the minimum window time-width of 2.13 ns. Please read Note 17 for a detailed explanation.

When only small sensitivity changes occur over a wide window time-width, the clock recovery circuit can exhibit larger static alignment error (a time offset from true center symbol position) plus more data dependent and random clock jitter and still maintain the FDDI PMD error rate requirements. Figure 9 illustrates the typical tradeoff of available window time-width versus sensitivity penalty. Designers can tradeoff for less clock recovery performance with little loss of sensitivity in this Hewlett-Packard receiver.

Package

The overall package concept for the Hewlett-Packard FDDI transceiver consists of three basic elements; the optical subassemblies, the electrical subassembly, and the housing with integral FDDI Media Interface Connector Receptacle (MIC/R). The objective of the design is to provide consistent optoelectronic performance in commercial equipment environments over extended equipment mission- lifetimes. The two versions provide design flexibility for different chassis grounding schemes. Two versions of the transceiver are available:

- The HFBR-5102 is constructed with a non-conductive plastic MIC/R mated to an aluminum case for the electrial subassembly. See Figure 1 for the outline drawing. This part is intended for use in equipment designs where separation is desired between the system signal ground and the chassis ground. The plastic MIC/R provides this ground isolation. The low emissions signature of the HFBR-5102 makes it compatible with VCCI Class 2, CISPR 22B, CENELEC 55022B and FCC Class B EMI Regulations.

- The HFBR-5101 is an all aluminum package part including the MIC/R. See Figure 1 for the outline drawing. The HFBR-5101 has

a low electromagnetic emissions signature but can be used in conjunction with conductive gasketing to the equipment chassis to form an EMI shield. This shield can prevent emissions generated inside the equipment from leaking outside.

The package is mechanically attached to the designer's circuit board by wave-soldered posts that eliminate the need for secondary operations which screw or rivet the device to the board. Two holes are provided in the bottom of the package for those circuit board applications where additional, or alternate, mechanical attachment is desired.

The optical subassemblies contain the 1300 nm LED (transmitter section) and the 1300 nm PIN with preamplifier IC (receiver section). Both transmitter and receiver optical subassemblies are hermetically sealed. These optical subassemblies are actively aligned to optical elements in the ferrule-bores. This active alignment provides optimal optical coupling for both the transmitter and receiver functions.

The electrical subassembly contains the driver and quantizer integrated circuits along with various surface-mounted passive components. This electrical subassembly provides optimum electrical performance with good noise immunity.

The housing for the electrical subassembly is aluminum with nickel plating. Aluminum is used for its excellent thermal conductivity which maintains the junction temperatures of the active semiconductors at low levels for high reliability and long mission-life. The optical subassemblies with their precision connector ferrule-bores are attached to the electrical subassembly and aligned to the MIC/R. Electrical and optical subassembly signal grounds are connected to the aluminum housing for maximum shielding.

The optical ports in the MIC/R are covered with an easily removable, high temperature, protective plug to prevent contamination during wave solder assembly of circuit boards and for shipment to end-user sites.

This package is compatible with normal wave solder and aqueous wash assembly procedures used in the industry today.

The transceiver is delivered in a specially designed shipping container to protect the part from mechanical or ESD damage during shipment or storage.

Product Reliability Data

Various environmental and life tests are performed on these products on an ongoing basis. Contact your local Hewlett-Packard sales representative to obtain copies of the latest test summaries as they become available.

Ordering Information

The Hewlett-Packard FDDI Transceivers are available packaged with key inserts per Table 1. The all metal HFBR-5101 directly replaces the HFBR-5125 transceiver per Table 1, and the HFBR-5102 is identical to the HFBR-5101 except for the plastic MIC/R.

Table 1. Ordering Information

	Transceiver Metal MIC/R	Transceiver Plastic MIC/R
Transceiver with a set of 4 key inserts (A, B, M and S)	HFBR-5101 Option ALL (Replaces HFBR-5125 Option ALL)	HFBR-5102 Option ALL
Transceiver with no key inserts included	HFBR-5101 Option 0FN	HFBR-5102 Option 0FN
Transceiver with A key installed	HFBR-5101 Option 0FA	HFBR-5102 Option 0FA
Transceiver with B key installed	HFBR-5101 Option 0FB	HFBR-5102 Option 0FB
Transceiver with M key installed	HFBR-5101 Option 0FM	HFBR-5102 Option 0FM
Transceiver with S key installed	HFBR-5101 Option 0FS	HFBR-5102 Option 0FS
Bag of 50 bags of 4 key inserts (A, B, M, and S)	HFBR-ABMS	
Bag of 100 A key inserts	HFBR-000A	
Bag of 100 B key inserts	HFBR-000B	
Bag of 100 M key inserts	HFBR-000M	
Bag of 100 S key inserts	HFBR-000S	

Figure 4 shows the key inserts which are black plastic parts with an identifying key letter code molded into the top surface of each key.

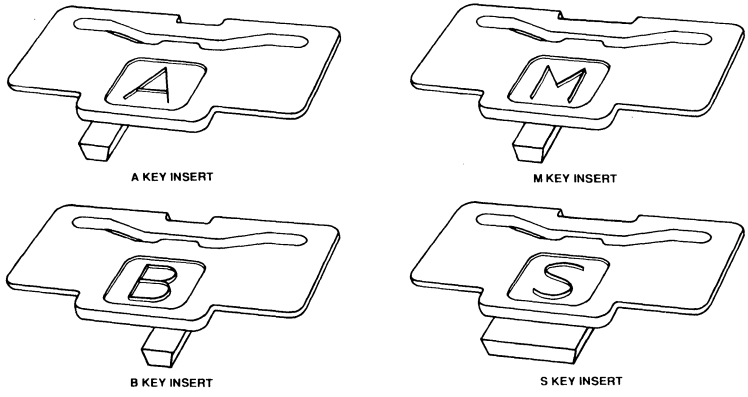


Figure 4. Key Inserts.

FDDI Transceiver

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	-40		100	°C	
Operating Temperature-Ambient	T_A	-10		80	°C	Note 1
Lead Soldering Temperature	T_{SOLD}			270	°C	
Lead Soldering Time	t_{SOLD}			4	sec.	
Supply Voltage	V_{CC}	-0.5		7.0	V	Note 2
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage	V_D			1.4	V	Note 3
Output Current	I_O			50	mA	Note 4

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by electrostatic discharge (ESD).

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Operating Temperature-Ambient	T_A	0		70	°C	Note 1
Supply Voltage	V_{CC}	4.75		5.25	V	Note 2
Supply Voltage – ECL Driver	V_{CCA}	4.75		5.25	V	Note 2
Supply Voltage – PIN	V_{PD}	4.75		5.25	V	Note 2
Data Input Voltage – Low	V_{IL} - V_{CC}	-1.810		-1.475	V	
Data Input Voltage – High	V_{IH} - V_{CC}	-1.165		-0.880	V	
Data and Signal Detect Output Load	R_L		50		Ω	Note 5
Signaling Rate	f_s	10		125	MBd	Note 6 Figures 5, 6

Transmitter Section

Transmitter Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		170	240	mA	Note 7
Power Dissipation	P_{DISS}		0.85	1.2	W	Note 7
Threshold Voltage	V_{BB} - V_{CC}	-1.420		-1.240	V	Note 8
Data Input Current – Low	I_{IL}	-350			µA	
Data Input Current – High	I_{IH}			350	µA	

Transmitter Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 62.5/125 µm, NA = 0.275 Fiber	P_O	-18.5	-16.2	-14	dBm avg	Note 9
Output Optical Power Temperature Coefficient	$\frac{\Delta P_O}{\Delta T}$		-0.015	-0.02	dB/°C	
Optical Extinction Ratio			0.01 -40	1.0 -20	% dB	Note 10
Center Wavelength	λ_C	1270	1320	1380	nm	Note 11 Figure 7
Spectral Width – FWHM	$\Delta\lambda$		140	170	nm	Note 12 Figure 7
Optical Rise Time	t_r	0.6	1.3	3.0	ns	Note 13 Figures 7, 8
Optical Fall Time	t_f	0.6	2.0	3.0	ns	Note 13 Figures 7, 8
Duty Cycle Distortion Contributed by the Transmitter	DCD		0.13	0.4	ns pk-to-pk	Note 14
Data Dependent Jitter Contributed by the Transmitter	DDJ		0.20	0.6	ns pk-to-pk	Note 15
Random Jitter Contributed by the Transmitter	RJ		0.01	0.69	ns pk-to-pk	Note 16

Receiver Section

Receiver Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power Minimum at Window Edge	$P_{IN\ Min}$ (W)		-35.4	-33	dBm avg	Note 17 Figure 9
Input Optical Power Minimum at Center	$P_{IN\ Min}$ (C)		-37	-34.5	dBm avg	Note 18 Figure 9
Input Optical Power Maximum	$P_{IN\ Max}$	-14	-12.9		dBm avg	Note 32
Operating Wavelength	λ	1270		1380	nm	
Signal Detect Asserted	P_A	P_D + 1.5 dB	-37.5	-33.5	dBm avg	Note 19, 29 Figure 10
Signal Detect Deasserted	P_D	-45	-39.8		dBm avg	Note 20, 30 Figure 10
Signal Detect Hysteresis	$P_A - P_D$	1.5	2.3		dB	Figure 10

Receiver Electrical Characteristics
(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		70	115	mA	Note 21
Supply Current	I_{CCA}		30	50	mA	Note 21
Supply Current – PIN Diode	I_{PD}		35	500	µA	Note 22
Power Dissipation	P_{DISS}		0.3	0.5	W	Note 23
Data Output Voltage – Low	V_{OL} - V_{CC}	-1.840		-1.620	V	Note 24
Data Output Voltage – High	V_{OH} - V_{CC}	-1.045		-0.880	V	Note 24
Data Output Rise Time	t_r	0.35	1.2	2.2	ns	Note 25
Data Output Fall Time	t_f	0.35	1.1	2.2	ns	Note 25
Duty Cycle Distortion	DCD		0.04	0.4	ns p-p	Note 26
Data Dependent Jitter	DDJ		0.7	1.0	ns p-p	Note 27
Random Jitter	RJ			2.14	ns p-p	Note 28
Signal Detect Output Voltage – Low	V_{OL} - V_{CC}	-1.840		-1.620	V	Note 24
Signal Detect Output Voltage – High	V_{OH} - V_{CC}	-1.045		-0.880	V	Note 24
Signal Detect Output Rise Time	t_r	0.35	0.9	2.2	ns	Note 24
Signal Detect Output Fall Time	t_f	0.35	0.7	2.2	ns	Note 25
Signal Detect Assert Time (off to on)	AS_Max	0	58	100	µs	Note 19, 29 Figure 10
Signal Detect Deassert Time (on to off)	ANS_Max	0	130	350	µs	Note 20, 30 Figure 10

Notes:

1. This maximum rating applies to still air environments around the transceiver.
2. When component testing these products all supply voltages should be applied simultaneously to avoid damage to the part.
3. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
4. When component testing these products do not short the receiver data or signal detect outputs directly to ground to avoid damage to the part.
5. The outputs are terminated with 50 Ω connected to V_{CC} - 2 V.
6. The specified signaling rate of 10 MBd to 125 MBd guarantees operation of the transmitter and receiver link to the full conditions listed in the FDDI Physical Layer Medium Dependent standard. Specifically, the link bit error ratio will be equal to or better than 2.5 x 10^{-10} for any valid FDDI pattern. The transmitter section of the link is capable of dc to 125 MBd. The receiver is internally ac-coupled which limits the lower signaling rate to 10 MBd. For purposes of definition, the symbol rate (Baud), also called signaling rate, f_s, is the reciprocal of the shortest symbol time. Data rate (bits/sec) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit).
7. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated, whether the noise is conducted or emitted, to neighboring receiver or logic circuitry.
8. This value is measured with an output load R_L = 10 kΩ.
9. These optical power values are measured with the following conditions:
   - At the Beginning Of Life (BOL).
   - Over the specified operating voltage and temperature ranges.
   - With HALT Line State, (12.5 MHz square-wave), input signal.
   - At the end of one meter of noted optical fiber with cladding modes removed.

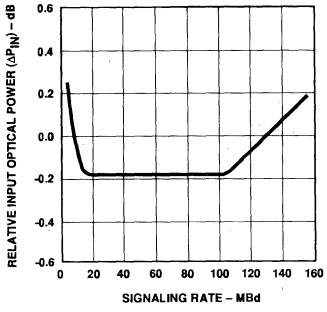
   The average power value can be converted to a peak power value by adding 3 dB. Higher output optical power transmitters are available on special request.
10. The Extinction Ratio is a measure of the modulation depth of the optical signal. The data "0" output optical power is compared to the data "1" peak output optical power and expressed as a percentage. With the transmitter driven by a HALT Line State (12.5 MHz square-wave) signal the optical signal is detected with a receiver that linearly converts optical power to voltage. The extinction ratio is the ratio of the voltage of the "0" level compared to the voltage at the "1" level expressed as a percentage.
11. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 7. The temperature coefficient of the center wavelength is typically +0.39 nm/°C.
12. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 7. The temperature coefficient of the spectral width is typically +0.25 nm/°C.
13. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 7. This parameter also complies with the optical pulse envelope shown in Figure 8. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by the FDDI HALT Line State (12.5 MHz square-wave) input signal.
14. Duty Cycle Distortion is measured at a 50% threshold using an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. The maximum value for this parameter is 0.2 ns better than required by the FDDI PMD standard.
15. Data Dependent Jitter is specified with the FDDI test pattern described in FDDI PMD Annex A.5.
16. Random Jitter is specified with an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal.
17. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following definitions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Ratio (BER) better than or equal to 2.5 x 10^{-10}. The BER will be better than or equal to 1 x 10^{-12} at input optical power levels greater than $P_{IN\ Min}$ plus approximately 0.8 dB with this Hewlett-Packard receiver. This is 1.2 dB better than required by the FDDI PMD. The measurement conditions are stated below.

    - At the Beginning of Life (BOL)
    - Over the specified operating temperature and voltage ranges
    - Input symbol pattern is the FDDI test pattern defined in FDDI PMD Annex A.5 with 4B/5B NRZI encoded data that contains a duty cycle base-line wander effect of 50 kHz. This sequence causes a near worst case condition for inter-symbol interference.
    - Input optical rise and fall times are approximately 1 ns and 2 ns respectively.
    - Receiver data window time-width is 2.13 ns or greater and centered at mid-symbol. This worst case window time-width is the minimum allowed eye-opening presented to the FDDI PHY PM_Data.indication input (PHY input) per the example in FDDI PMD Annex E. This minimum window time-width of 2.13 ns is based upon the worst case FDDI PMD Active Input Interface optical conditions for peak-to-peak DCD (1.0 ns), DDJ (1.2 ns) and RJ (0.76 ns) presented to the receiver.

To test a receiver with the worst case FDDI PMD Active Input jitter conditions require exacting control over DCD, DDJ and RJ jitter components that is difficult to implement with production test equipment. The receiver can be equivalently tested to the worst case FDDI PMD input jitter conditions and meet the minimum output data window time-width of 2.13 ns. This is accomplished by using a nearly ideal input optical signal (no DCD, insignificant DDJ and RJ) and measuring for a wider window time-width of 4.6 ns. This is possible due to the accumulative effect of jitter components through their superposition (DCD and DDJ are directly additive and RJ components are rms additive). Specifically, when a nearly ideal input optical test signal is used and the maximum receiver peak-to-peak jitter contributions of DCD (0.4 ns), DDJ (1.0 ns), and RJ (2.14 ns) exist, the minimum window time-width becomes 8.0 ns - 0.4 ns - 1.0 ns - 2.14 ns = 4.46 ns, or conservatively 4.6 ns. This wider window time-width of 4.6 ns guarantees the FDDI PMD Annex E minimum window time- width of 2.13 ns under worst case input jitter conditions to the Hewlett-Packard receiver.

- Transmitter operating with an IDLE Line State pattern, 125 MBd (62.5 MHz square-wave), input signal to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.

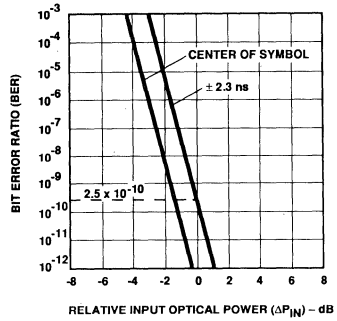
18. All conditions of Note 17 apply except that the measurement is made at the center of the symbol with no window time-width.
19. This value is measured during the transition from low to high levels of input optical power.
20. This value is measured during the transition from high to low levels of input optical power. The minimum value will be either -45 dBm average or when the input optical power yields a BER of 10^{-3} or better, whichever power is higher.
21. These values are measured with the outputs terminated into 50 Ω connected to V_{CC} - 2 V.
22. Measured at P_{IN} = -14 dBm average.
23. The power dissipation value is the power dissipated in the receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and supply currents, minus the sum of the products of the output voltages and currents.
24. These values are measured with respect to V_{CC} with the output terminated into 50 Ω connected to V_{CC} - 2 V. The minimum values are corrected for +5.25 V operation for 100 K ECL values that are usually specified at -4.8 V operation.
25. The output rise and fall times are measured between 20% and 80% levels with the output connected to V_{CC} - 2 V through 50 Ω.
26. Duty Cycle Distortion is measured at 50% threshold using an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. The input optical power level is -20 dBm average.
27. Data Dependent Jitter is specified with the FDDI test pattern described in PMD Annex A.5. The input optical power level is -20 dBm average.
28. Random Jitter is specified with an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. The input optical power level is at maximum "$P_{IN\ Min}$ (W)".
29. The Signal Detect output shall be asserted within 100 µs after a step increase of the Input Optical Power. The step will be from a low Input Optical Power, ≤ -45 dBm, into the range between greater than P_A, and -14 dBm. The BER of the receiver output will be 10^{-3} or better during the time, LS_Max (15 µs) after Signal Detect has been asserted. See Figure 10 for more information.
30. Signal detect output shall be deasserted within 350 µs after a step decrease in the Input Optical Power from a level which is the lower of; -31 dBm or P_D + 4 dB (P_D is the power level at which signal detect was deasserted), to a power level of -45 dBm or less. This step decrease will have occurred in less than 8 ns. The receiver output will have a BER of 10^{-3} or better for a period of 12 µs or until signal detect is deasserted. The input data stream is the Quiet Line State. Also, signal detect will be deasserted within a maximum of 350 µs after the BER of the receiver output degrades above 10^{-3} for an input optical data stream that decays with a negative ramp function instead of a step function. See Figure 10 for more information.
31. The transceiver under test was supplied with a 62.5 MHz square wave (125 MBd) optical signal from outside a semi-anechoic chamber to the receiver section located inside this chamber. An input optical power level of -20 dBm average was applied. Electrical output signals from the receiver section were connected directly to the electrical input of the transmitter section of the test transceiver. In turn, the transmitter section returned the optical data to a receiver outside the test chamber to be compared for data integrity. The noise floor of Figure 13 is dictated by the measuring equipment. From DC to one GHz, one set of test instrumentation monitored the emissions. Above 1 GHz, a different instrumentation system measured emissions up to 2 GHz. The difference in the bandwidths of the two systems causes the discontinuity in the noise floor at 1 GHz.
32. Tested at 125 Mb/s and with a data-pattern PRBS 2^7-1. The sampling clock is adjusted to minimum (0.0 ns) delay and incremented in 0.5 ns steps up to a total of 7.5 ns delay. At each clock delay increment, the BER is checked. The total number of delay positions (N) yielding a BER <1E-5 is recorded. The Receiver Saturation level is the highest input optical power at which N ≥ 9.



CONDITIONS:

1. P_{IN} NORMALIZED (ΔP_{IN} = 0 dB) TO $P_{IN\ Min}$ (C) AT 125 MBd AT CENTER OF SYMBOL.
2. $\Delta P_{IN} = P_{IN}$ @ MBd - P_{IN} @ 125 MBd
3. FDDI PMD APPENDIX A.5 125 MBd TEST PATTERN WITH 50 kHz BASELINE WANDER
4. BER = 2.5 X 10^{-10}
5. T_A = 25°C
6. V_{CC} = 5 Vdc
7. INPUT OPTICAL RISE/FALL TIMES = 1.0 ns/2.1 ns

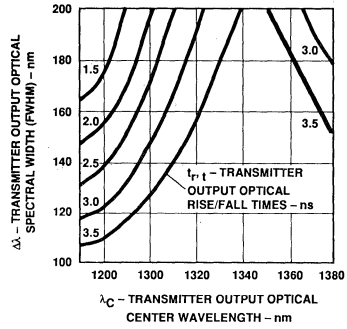
Figure 5. Relative Input Optical Power vs. Signaling Rate.



CONDITIONS:

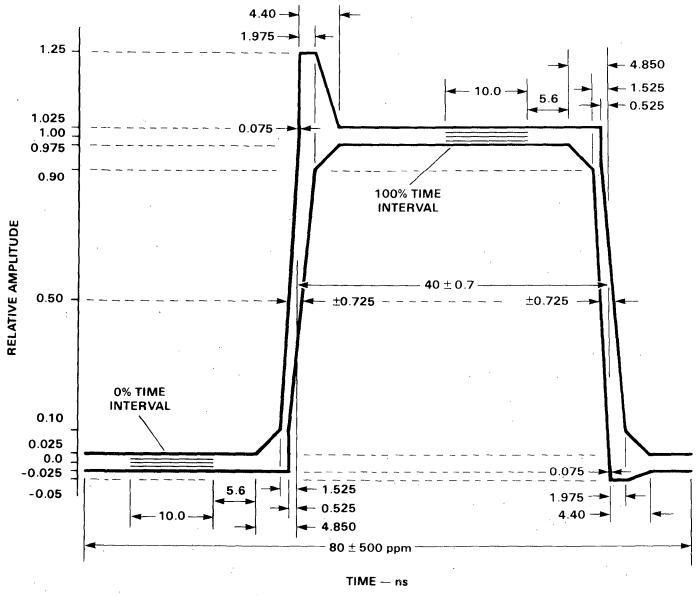
1. P_{IN} IS NORMALIZED (ΔP_{IN} = 0 dB) AT $P_{IN\ Min}$ (W) WITH BER = 2.5 x 10^{-10} AND WINDOW TIME-WIDTH OF ±2.3 ns EITHER SIDE OF SYMBOL CENTER.
2. $\Delta P_{IN} = P_{IN}$ @ BER - P_{IN} @ 2.5 x 10^{-10} BER
3. FDDI PMD APPENDIX A.5 125 MBd TEST PATTERN WITH 50 kHz BASELINE WANDER.
4. T_A = 25°C
5. V_{CC} = 5.0 Vdc
6. INPUT OPTICAL RISE/FALL TIMES = 1.0 ns/2.1 ns

Figure 6. Typical Bit Error Rate vs. Relative Input Optical Power.



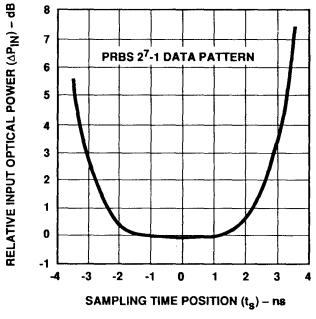
HEWLETT PACKARD FDDI TRANSMITTER TEST RESULTS OF λ_C, $\Delta\lambda$ AND $t_{r,f}$ ARE CORRELATED AND COMPLY WITH THE ALLOWED SPECTRAL WIDTH AS A FUNCTION OF CENTER WAVELENGTH FOR VARIOUS RISE AND FALL TIMES.

Figure 7. Transmitter Output Optical Spectral Width (FWHM) vs. Transmitter Output Optical Center Wavelength and Rise/Fall Times.



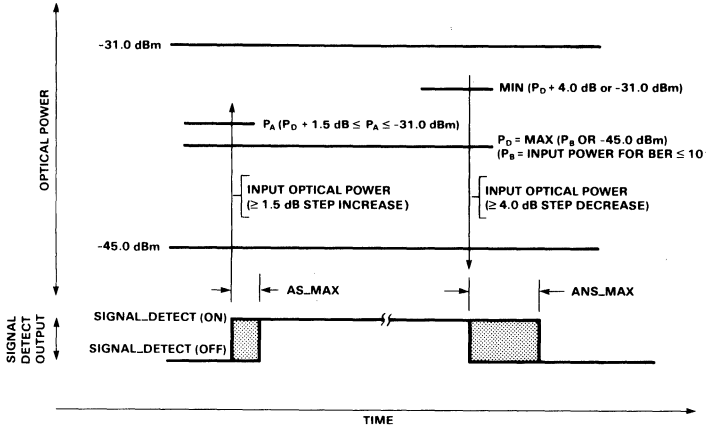
THE OUTPUT OPTICAL PULSE SHAPE SHALL FIT WITHIN THE BOUNDARIES OF THE PULSE ENVELOPE. FOR RISE AND FALL TIME MEASUREMENTS, THE MAXIMUM POSITIVE AND MINIMUM NEGATIVE WAVEFORM EXCURSIONS IN THE ZERO AND 100% TIME INTERVALS SHALL BE CENTERED AROUND THE 0.0 AND 1.00 LEVELS, RESPECTIVELY. A MINIMUM BANDWIDTH RANGE OF 100 kHz TO 750 MHz IS REQUIRED FOR THE MEASUREMENT EQUIPMENT USED TO EVALUATE THE PULSE ENVELOPE.

Figure 8. Output Optical Pulse Envelope.



CONDITIONS:
1. PIN IS NORMALIZED TO $P_{IN\ Min}$ (C) AT CENTER OF SYMBOL.
2. $\Delta P_{IN} = P_{IN} @ t_f - P_{IN} @ t_{CENTER}$.
3. PRBS 2^7-1 DATA PATTERN.
4. BER = 2.5 x 10^{-10}
5. T_A = 25° C.
6. VCC = 5 Vdc
7. INPUT OPTICAL RISE/FALL TIMES = 1.0 ns/2.1 ns.

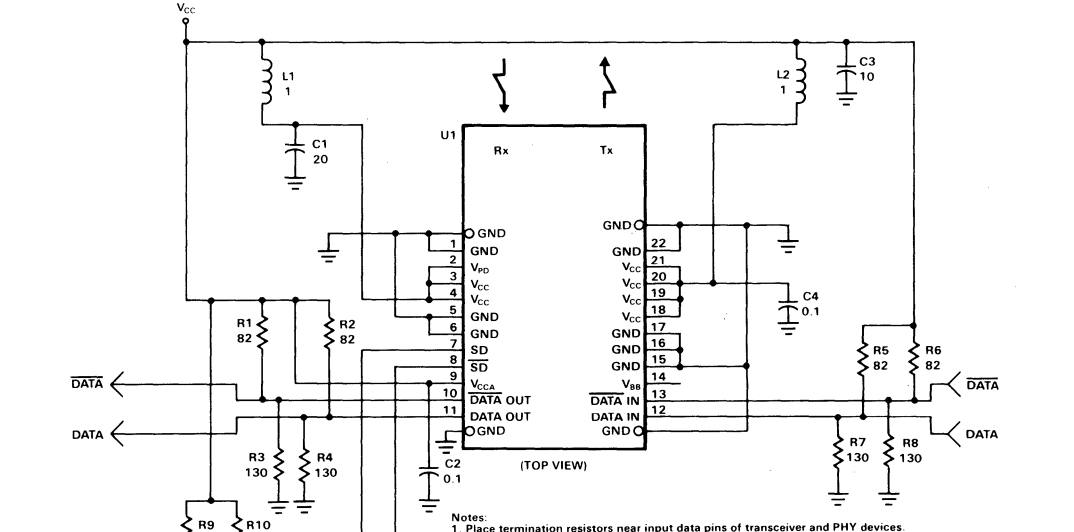
Figure 9. Relative Input Optical Power vs. Sampling Time Position.



AS_MAX—MAXIMUM ACQUISITION TIME (SIGNAL).
AS_MAX IS THE MAXIMUM SIGNAL_DETECT ASSERTION TIME FOR THE STATION. AS_MAX SHALL NOT EXCEED 100.0 µs. THE DEFAULT VALUE OF AS_MAX IS 100.0 µs.

ANS_MAX—MAXIMUM ACQUISITION TIME (NO SIGNAL).
ANS_MAX IS THE MAXIMUM SIGNAL_DETECT DEASSERTION TIME FOR A STATION. ANS_MAX SHALL NOT EXCEED 350 µs. THE DEFAULT VALUE OF ANS_MAX IS 350 µs.

Figure 10. Signal Detect Thresholds and Timing.



Notes:
1. Place termination resistors near input data pins of transceiver and PHY devices.
2. Make differential signal paths short and of the same length with equal terminations to V_{CC}-2 volts.
3. Signal traces should be 50 Ohm transmission lines: Microstrip (or stripline). Use ground plane (or multi-layer) printed circuit board for best high frequency performance.
4. Resistors in Ohms. Capacitors in microFarads. Inductors in microHenries.
5. Use high-frequency monolithic ceramic bypass capacitors and low series dc resistance inductors. Ferrite inductors can be used. Locate power supply filter components close to fiber-optic devices.
6. CAUTION: Do not directly connect fiber optic module ECL outputs - (Data, Data, Signal Detect, Signal Detect) to ground without proper current limiting impedence.
7. All power supply voltages for the fiber optic receiver or transmitter section should be applied simultaneously to prevent possible damage to the device.
8. Device ground pins should be directly and individually connected to ground.
9. Device solder posts should be directly and individually connected to ground for best EMI shielding.

Figure 11. Recommended Decoupling Circuit Diagram.

Application Assistance

The Applications Engineering group in the Hewlett-Packard Optical Communication Division is available to assist with the technical understanding and design trade-offs associated with this FDDI transceiver. You can contact them through your local Hewlett-Packard sales representative.

The following information is provided to answer some of the most common application questions that have been asked relative to the use of the HFBR-5101/5102 transceivers.

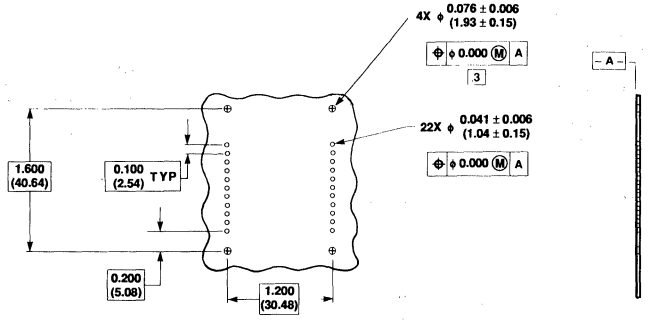
Board Layout - Decoupling Circuit and Ground Planes

It is important to take care in the layout of your circuit board to achieve optimum performance from the HFBR-5101/5102 transceiver. Figure 11 provides a good example of a schematic for a decoupling circuit that works well with this product. It is further recommended that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices. Layouts that overlay the multisourced 2X11 footprint with the alternative 1X13 transceiver footprint need to pay special attention to this recommendation for a contiguous ground plane under the transceiver to achieve good performance.

Board Layout - Hole Pattern

Figure 12 shows the recommended board hole pattern to be used for the HFBR-5101/5102 transceivers. This recommendation complies with the original Multisource FDDI Transceiver definition announced by AT&T, Hewlett-Packard, and Siemens in 1989. This hole size and location recommendation allows for easy insertion of the transceiver into the circuit board during assembly operations.

To interpret Figure 12 it is important to remember to allow for some positional tolerance beyond the perfect position noted and trade this off for tighter hole size tolerance. For example, if you desire a 0.006 inch tolerance on hole location then the consequent hole size should be held to 0.076 inch minimum instead of 0.070 minimum allowed for the case where the holes would be drilled in the perfect location.



NOTES:
1. DIMENSIONS ARE IN INCHES OVER (MILLIMETERS).
2. DIMENSIONS PER ANSI Y14.5M.
3. SEE APPLICATION ASSISTANCE: BOARD LAYOUT – HOLE PATTERN SECTION FOR MORE INFORMATION.

Figure 12. Board Layout – Hole Pattern.

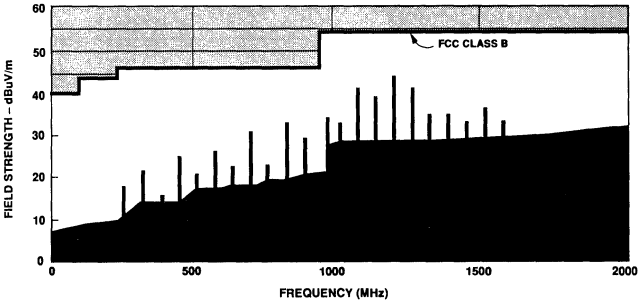


Figure 13. HFBR-5102, Typical Electric Field Strength at 3 m, 125 MBd.

Electromagnetic Emissions

Figure 13 shows typical radiated emissions from a sample of HFBR-5102 transceivers. The units meet FCC Class B far-field emission limits at three metres with the transceiver mounted on a printed circuit board in an open, unshielded environment within an approved semi-anechoic chamber. See note 31 for details on the test method.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled work areas.

The Hewlett-Packard HFBR-5101/5102 has been characterized per MIL-STD-883C Method 3015.4 to tolerate more than 2 kV between pins without damage. This is within the ESD Class 2 specification range of 2000 V to 3999 V.

The second case to consider is static discharges to the exterior of the equipment chassis after the FDDI interface card is installed. In many equipment designs the MIC/R of the FDDI transceiver is exposed outside the exterior of the chassis. With this exposure it is subject to the same ESD test criteria that apply to the entire product in which it is installed. Another specific exposure occurs whenever a Media Interface Connector/Plug is inserted into the transceiver MIC/R.

The Hewlett-Packard HFBR-5101/5102 transceiver has been characterized to withstand up to 25 kV air discharge from a human body source without catastrophic damage. A test procedure similar to IEC 801-2 was used for this characterization test.

When designing equipment the designer should consider the ESD discharge path to ground. In designs that allow contact between chassis and signal/logic ground this can be accomplished either with a conductive shield or gasket between the chassis and the conductive (aluminum) MIC/R of the HFBR-5101 transceiver, or by connecting the transceiver solder posts and/or ground pins to chassis ground on the circuit board.

In the design case where contact between chassis ground and signal/logic ground is not allowed, the HFBR-5102, which has a non-conductive MIC/R, may be used. To assist an ESD event to transfer to ground, a metal ground plane can be located near the aperture, inside the equipment chassis. This would provide a local, conductive arc-path to ground. Also, this metal can take the form of a guard ring at the peripheral edge of a printed circuit board that is connected to Earth ground. For best EMI/ESD performance, the ground posts should be soldered to the designer's PCB ground.

HEWLETT PACKARD

SNAP-IN FIBER OPTIC LINKS TRANSMITTERS, RECEIVERS, CABLE AND CONNECTORS

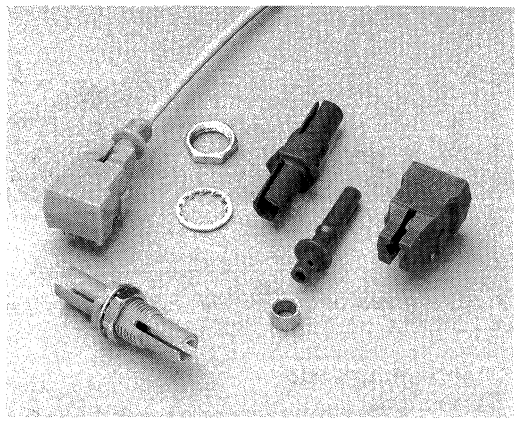
HFBR-0500 SERIES

Features

- **GUARANTEED LINK PERFORMANCE OVER TEMPERATURE**
  High Speed Links: dc to 5 MBd
  Extended Distance Links up to 111 m
  Low Current Links: 6 mA Peak Supply Current for an 10 m Link
  Photo Interrupters
- **LOW COST PLASTIC DUAL-IN-LINE PACKAGE**
- **EASY FIELD CONNECTORING**
- **EASY TO USE RECEIVERS:**
  Logic Compatible Output Level
  Single +5 V Receiver Power Supply
  High Noise Immunity
- **LOW LOSS PLASTIC CABLE:**
  Simplex and Zip Cord Style Duplex Cable
  Extra Low Loss Simplex and Duplex

Applications

- **HIGH VOLTAGE ISOLATION**
- **SECURE DATA COMMUNICATIONS**
- **REMOTE PHOTO INTERRUPTER**
- **LOW CURRENT LINKS**
- **INTER/INTRA-SYSTEM LINKS**
- **STATIC PROTECTION**
- **EMC REGULATED SYSTEMS (FCC, VDE)**



Description

The HFBR-0500 series is a complete family of fiber optic link components for configuring low-cost control, data transmission, and photo interrupter links. These components are designed to mate with plastic snap-in connectors and low-cost plastic cable.* Link design is simplified by the logic compatible receivers and the ease of connectoring the plastic fiber cable. The key parameters of links configured with the HFBR-0500 family are fully guaranteed.

*Cable is available in standard low loss and extra low loss varieties.

Link Selection Guide

GUARANTEED LINKS

Data	Data Rate	Guaranteed Link Length 0-70°C		Typical Link Lengths 25°C		Transmitter	Receiver
		Standard Cable	Extra Low Loss Cable	Standard Cable	Extra Low Loss Cable		
5 MBd Link	5 MBd	19	22	48 m	53 m	HFBR-1510	HFBR-2501
1 MBd Link	1 MBd	39	45	70 m	78 m	HFBR-1502	HRBR-2502
Low Current Link	40 kBd	13	15	41 m	45 m	HFBR-1512	HFBR-2503
Extended Distance Link	40 kBd	94	111	138	154 m	HFBR-1512	HFBR-2503
Photo Interrupter Link	20 kHz 500 kHz	N/A N/A	N/A N/A	N/A N/A	N/A N/A	HFBR-1512 HFBR-1502	HFBR-2503 HFBR-2502

Component Selection Guide

TRANSMITTERS

	Minimum Output Optical Power 0 to 70° C	Peak Emission Wavelength
HFBR-1510	−16.5 dBm	665 nm
HFBR-1502	−13.6 dBm	665 nm
HFBR-1512	−13.6 dBm	665 nm

RECEIVERS

	Sensitivity 0 to 70° C	Data Rate
HFBR-2501	−21.6 dBm	5 MBd
HFBR-2502	−24 dBm	1 MBd
HFBR-2503	−39 dBm	40 kBd

CABLES

Please refer to the Versatile Link Fiber Optics for cable specifications.

CONNECTORS

HFBR-4501 Gray Connector/Crimp Ring
HFBR-4511 Blue Connector/Crimp Ring
HFBR-4593 Polishing Kit
Bulkhead Feedthrough/In-Line Splice:
HFBR-4505 Gray
HFBR-4515 Blue

5 MBd Link

HFBR-1510 AND HFBR-2501

The dc to 5 MBd link is guaranteed over temperature to operate up to 19 m with a transmitter drive current of 60 mA. This link uses the 665 nnm HFBR-1510 Transmitter, the HFBR-2501 Receiver, and Extra Low Loss Plastic Cable. The receiver compatible with LSTTL/TTL/CMOS logic levels offers a choice of internal pull-up or open collector output.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units	Ref.
Ambient Temperature	T_A	0	70	°C	
Transmitter Peak Forward Current	$I_{F\,PK}$	10	750	mA	Note 1
Avg. Forward Current	$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	V_{CC}	4.75	5.25	V	Note 2
Fan-Out (TTL)	N		5		

SYSTEM PERFORMANCE Using Standard Cable under recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Data Rate		dc		5	MBd	BER ≤ 10^{-9}	
Transmission Distance Standard Cable	ℓ	19 27	 48		m m	I_{FPK} = 60 mA, 0–70° C I_{FPK} = 60 mA, 25° C	
Transmission Distance Extra Low Loss Cable		22 32	 53		m m	I_{FPK} = 60 mA, 0–70° C I_{FPK} = 60 mA, 25° C	
Propagation Delay	t_{PLH} t_{PHL}		80 50	140 140	ns ns	R_L = 560 Ω, C_L = 30 pF P_R = −21.6≤P_R≤−9.5dBm	Fig. 4, 5 Note 3
Pulse Width Distortion	t_D		30		ns	P_R = −15 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 4, 6 Note 4
EMI Immunity			8000		V/m	BER ≤ 10^{-9}	

Notes: 1. For I_{FPK} > 80 mA, the duty factor must be such as to keep I_{FAV} ≤ 80 mA. In addition, for I_{FPK} > 80 mA, the following rules for pulse width apply: I_{FPK} ≤ 160 mA: Pulse width ≤ 1 ms I_{FPK} > 160 mA: Pulse width ≤ 1 μs

2. It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from pin 3 to pin 4 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.
3. The propagation delay of 1 m of cable (5 ns) is included.
4. $T_D = t_{PLH} - t_{PHL}$.
5. Typical data is at 25° C, V_{CC} = 5 V.

Link Design Considerations

The HFBR-1510/2501 Transmitter/Receiver pair is guaranteed for operation at data rates up to 5 MBd over link distances from 0 to 19 metres with standard cable and from 0 to 22 metres with improved cable. The value of transmitter drive current, I_F, depends on the link distance as shown in Figures 2 and 3. Note that there is an upper as well as a lower limit on the value of I_F for any given distance. The dotted lines in Figures 2 and 3 represent pulsed operation. When operating in the pulsed mode, the conditions in Note 1 must be met. After selecting a value of the transmitter drive current I_F, the value of R_1 in Figure 1 can be calculated as follows:

$$R_1 = \frac{V_{CC} - V_F}{I_F}$$

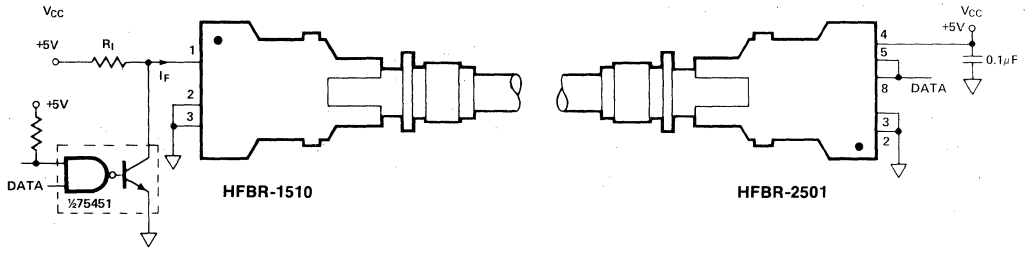


Figure 1. Typical Circuit Operation (5 MBd ≤ 12 m)

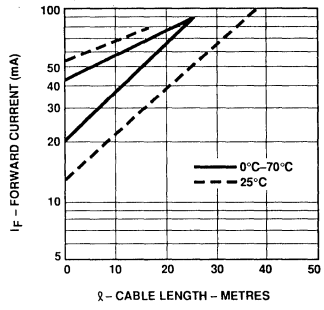


Figure 2. Guaranteed System Performance with HFBR-1510 and HFBR-2501, Standard Cable

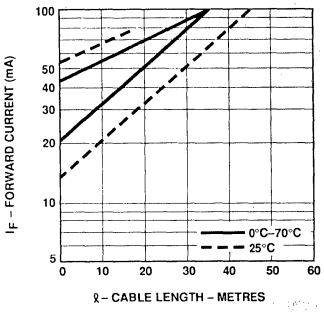
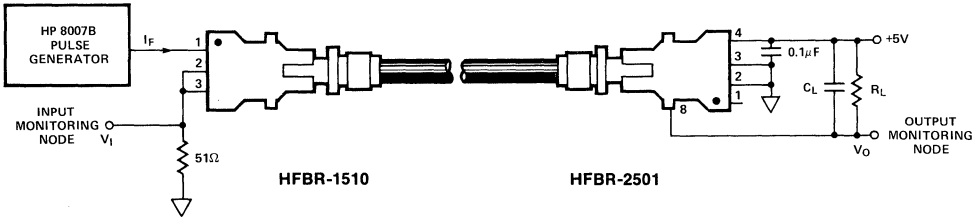


Figure 3. Guaranteed System Performance with HFBR-1510 and HFBR-2501, Extra Low Loss Cable



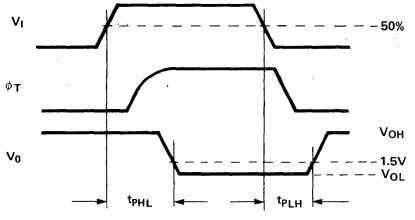


Figure 4. A.C. Test Circuit

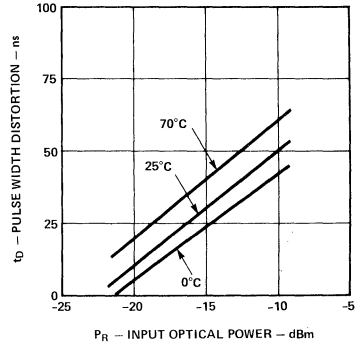


Figure 5. HFBR-1510/2501 Link Pulse Width Distortion vs. Optical Power

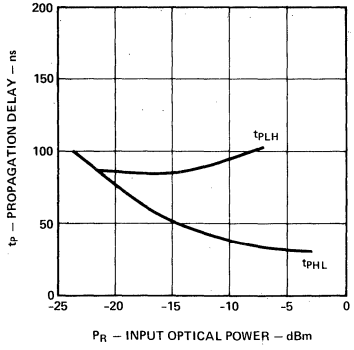


Figure 6. HFBR-1510/2501 Link Propagation Delay vs. Optical Power

1 MBd Link HFBR-1502 AND HFBR-2502

The dc to 1 MBd link is guaranteed over temperature to operate from 0 to 39 m with a transmitter drive current of 60 mA. This link uses the 665 nm HFBR-1502 Transmitter, the HFBR-2502 Receiver, and Improved Cable. The receiver is compatible with LSTTL/TTL/CMOS logic levels and offers a choice of an internal pull-up or open collector output.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units	Ref.
Ambient Temperature	T_A	0	70	°C	
Transmitter Peak Forward Current	$I_{F\,PK}$	10	750	mA	Note 1
Avg. Forward Current	$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	V_{CC}	4.75	5.25	V	Note 2
Fan-Out (TTL)	N		5		

SYSTEM PERFORMANCE Using Standard Cable under recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Data Rate		dc		1	MBd	BER ≤ 10^{-9}	
Transmission Distance Standard Cable	ℓ	39			m	I_{FPK} = 60 mA, 0–70° C	
		47	70		m	I_{FPK} = 60 mA, 25° C	
Transmission Distance Extra Low Loss Cable	ℓ	45			m	I_{FPK} = 60 mA, 0–70° C	
		56	78		m	I_{FPK} = 60 mA, 25° C	
Propagation Delay	t_{PLH}		180	250	ns	R_L = 560 Ω, C_L = 30 pF	Fig. 4, 5
	t_{PHL}		100	140	ns	P_R = −24 dBm	Note 3
Pulse Width Distortion	t_D		80		ns	P_R = −24 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 4, 6 Note 4
EMI Immunity			8000		V/m	BER ≤ 10^{-9}	

Notes: 1. For I_{FPK} > 80 mA, the duty factor must be such as to keep $I_{FAV} \leq 80$ mA. In addition, for I_{FPK} > 80 mA, the following rules for pulse width apply: $I_{FPK} \leq 160$ mA: Pulse width ≤ 1 ms I_{FPK} > 160 mA: Pulse width ≤ 1 μs

2. It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from pin 3 to pin 4 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.

3. The propagation delay of 1 m of cable (5 ns) is included. 4. $T_D = t_{PLH} - t_{PHL}$. 5. Typical data is at 25° C, V_{CC} = 5 V.

Link Design Considerations

The HFBR-1502/2502 Transmitter/Receiver pair is guaranteed for operation at data rates up to 1 MBd over link distances from 0 to 32 metres with standard cable and from 0 to 37 metres with improved cable. The value of transmitter drive current, I_F, depends on the link distance as shown in Figures 2 and 3. Note that there is a lower limit on the value of I_F for any given distance. The dotted lines in Figures 2 and 3 represent pulsed operation. When operating in the pulsed mode, the conditions in Note 1 must be met. After selecting a value of the transmitter drive current I_F, the value of R_1 in Figure 1 can be calculated as follows:

$$R_1 = \frac{V_{CC} - V_F - V_{OL}\ (75451)}{I_F}$$

For the HFBR-1502/2502 pair, the value of the capacitor, C_1 (Figure 1) must be chosen such that $R_1 C_1 \geq 75$ ns.

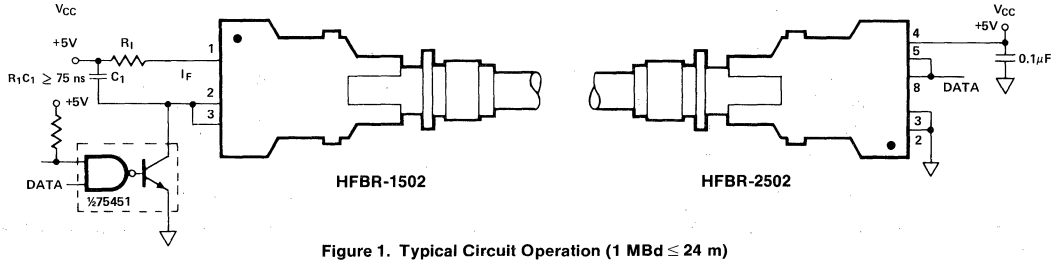


Figure 1. Typical Circuit Operation (1 MBd ≤ 24 m)

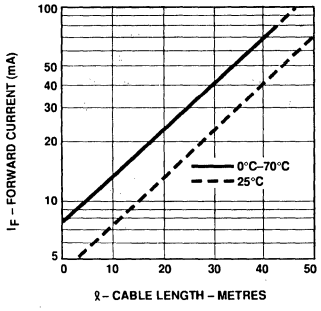


Figure 2. Guaranteed System Performance with HFBR-1502 and HFBR-2502, Standard Cable

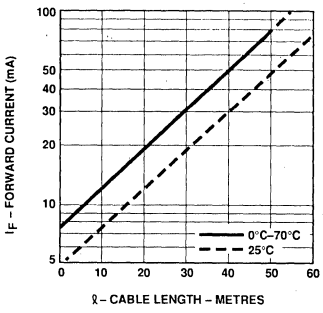


Figure 3. Guaranteed System Performance with HFBR-1502 and HFBR-2502, Extra Low Loss Cable

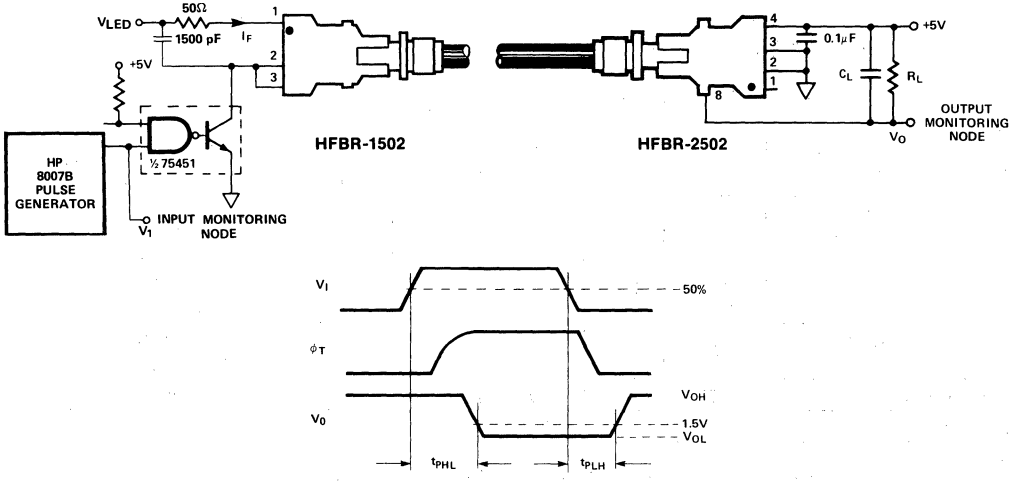


Figure 4. A.C. Test Circuit

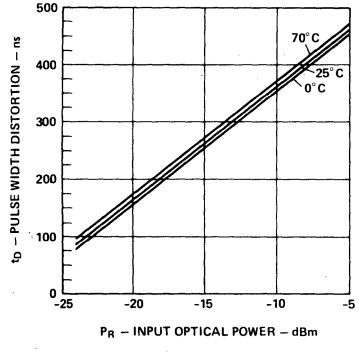


Figure 5. HFBR-1502/2502 Link Pulse Width Distortion vs. Optical Power

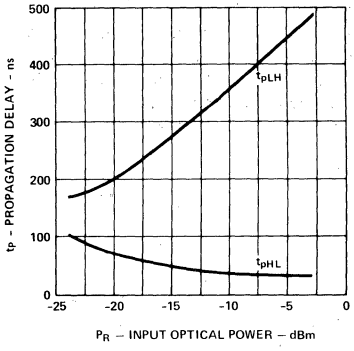


Figure 6. HFBR-1502/2502 Link Propagation Delay vs. Optical Power

Low Current/Extended Distance Link

HFBR-1512 AND HFBR-2503

The low current link requires only 6 mA peak supply current for the transmitter and receiver combined to achieve a 13 m link. Extended distances up to 94 m can be achieved at a maximum transmitter drive current of 60 mA peak. This link can be driven with TTL/LSTTL and most CMOS logic gates.

The black plastic housing of the HFBR-1512 Transmitter is designed to prevent the penetration of ambient light into the cable through the transmitter. This prevents the sensitive receiver from being triggered by ambient light pulses.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units	Ref.
Ambient Temperature	T_A	0	70	°C	
Transmitter Peak Forward Current	$I_{F\,PK}$	2	120	mA	Note 1
Avg. Forward Current	$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	V_{CC}	4.5	5.5	V	Note 2
Output Voltage	V_O		V_{CC}	V	
Fan-Out (TTL)	N		1		

SYSTEM PERFORMANCE Using Standard Cable under recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Data Rate		dc		40	kBd	$t_D \leq 7.0\ \mu s$	
Transmission Distance Standard Cable	ℓ	13	41		m	I_{FPK} = 2 mA, 0–70° C	
		94	138		m	I_{FPK} = 60 mA, 0–70° C	
Transmission Distance Extra Low Loss Cable	ℓ	15	45		m	I_{FPK} = 2 mA, 0–70° C	
		111	154		m	I_{FPK} = 60 mA, 0–70° C	
Propagation Delay	t_{PLH}		4		μs	R_L = 3.3K Ω, C_L = 30 pF	Fig. 4, 5
	t_{PHL}		2.5		μs	P_R = −25 dBm	Note 3
Pulse Width Distortion	t_D			7.0	μs	$-39 \leq P_R \leq -14$ dBm R_L = 3.3 KΩ, C_L = 30 pF	Fig. 4, 6 Note 4
Bit Error Rate	BER		10^{-9}			P_R = −30 dBm	
EMI Immunity			5000		V/m	P_R = 0 mW	

Notes:
1. For I_{FPK} > 80 mA, the duty factor must be such as to keep $I_{FAV} \leq 80$ mA. In addition, if I_{FAV} > 80 mA, then the pulse width must be equal to or less than 1 ms.
2. It is recommended that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from pin 3 to pin 4 of the receiver.
3. The propagation delay of 1 m of cable (5 ns) is included.
4. $t_D = t_{PLH} - t_{PHL}$.
5. Typical data is at 25° C, V_{CC} = 5 V.

Link Design Considerations

The HFBR-1512/2503 Transmitter/Receiver pair is guaranteed for operation at data rates up to 40 kBd for transmitter drives as low as 2 mA. The value of transmitter drive current, I_F, depends on the link distance as shown in Figures 2 and 3. Note that there is an upper as well as a lower limit on the value of I_F for any given distance. After selecting a value of the transmitter drive current I_F, the value of R_1 in Figure 1 can be calculated as follows:

$$R_1 = \frac{V_{CC} - V_F}{I_F}$$

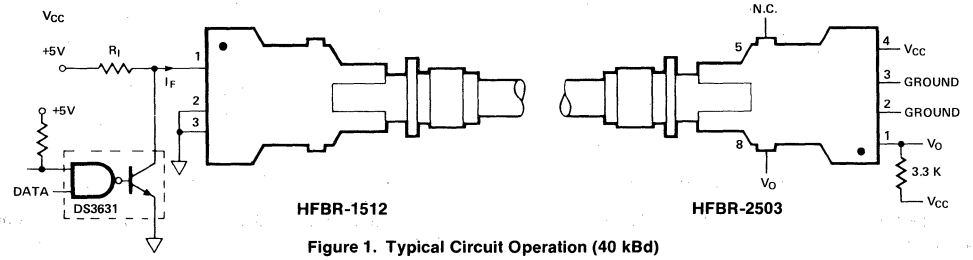


Figure 1. Typical Circuit Operation (40 kBd)

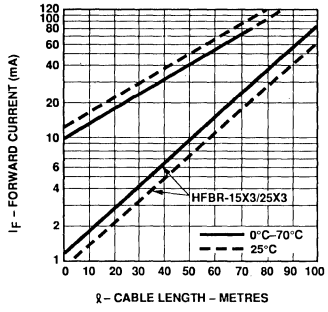


Figure 2. Guaranteed System Performance with HFBR-1512 and HFBR-2503, Standard Cable

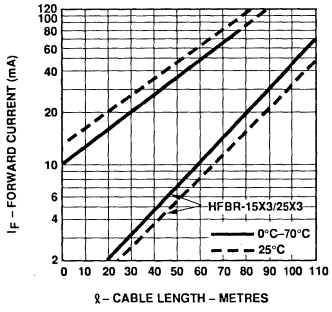
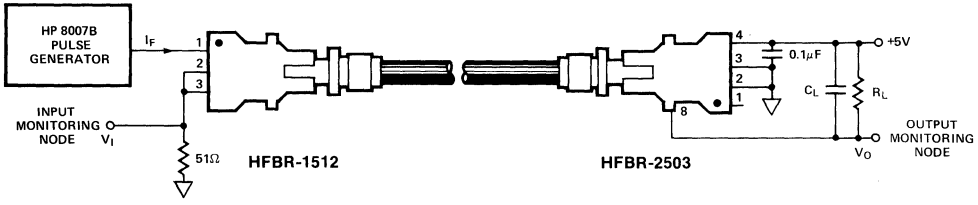


Figure 3. Guaranteed System Performance with HFBR-1512 and HFBR-2503, Extra Low Loss Cable



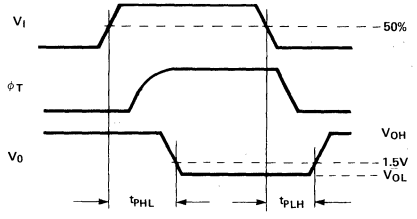


Figure 4. A.C. Test Circuit

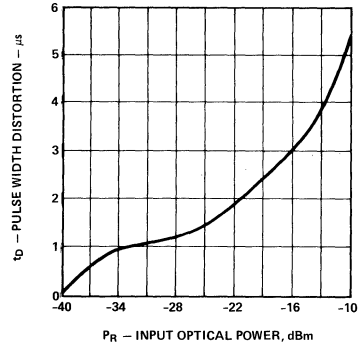


Figure 5. HFBR-1512/2503 Link Pulse Width Distortion vs. Optical Power

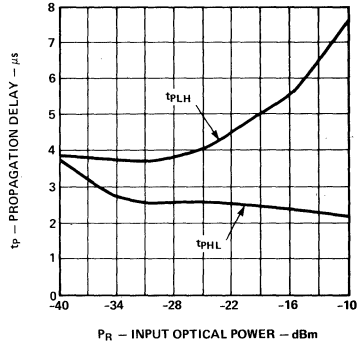


Figure 6. HFBR-1512/2503 Link Propagation Delay vs. Optical Power

Photo Interrupter Links

HFBR-1502/2502
HFBR-1512/2503

These links may be used in optical switches, shaft position sensors, and velocity sensors. They are particularly useful where high voltage, electrical noise, or explosive environments prohibit the use of electromechanical or optoelectronic sensors.

The HFBR-1512/2503 link (20 kHz) has an optical power budget of 24 dB, and the HFBR-1502/2502 link (500 kHz) budget is 10 dB. Total system losses (cable attenuation, air-gap loss, etc) must not exceed the link optical power budget.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min.	Max.	Units	Ref.
Ambient Temperature		T_A	0	70	°C	
Transmitter Peak Forward Current		$I_{F\,PK}$	10	750	mA	Note 1
Avg. Forward Current		$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	HFBR-2503	V_{CC}	4.50	5.50	V	Note 2
	HFBR-2502		4.75	5.25		
Output Voltage	HFBR-2503	V_O		V_{CC}	V	
	HFBR-2502			18		
Fanout (TTL)	HFBR-2503			1		
	HFBR-2502			5		

SYSTEM PERFORMANCE

See HFBR-1502/2502 link data sheet (page 4-10) and HFBR-1512/2503 link data sheet (page 4-12) for more design information. These specifications apply when using HFBR-3510/3610 series cable and, unless otherwise specified, under recommended operating conditions.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
HFBR-1512/HFBR-2503							
Max. Count Frequency		dc		20	kHz		
Optical Power Budget		25.4			dB	I_{FPK} = 60 mA, 0–70° C	
		27.8	34		dB	I_{FPK} = 60 mA, 25° C	Note 3, 4
HFBR-1502, HFBR-2502							
Max. Count Frequency		dc		500	kHz		
Optical Power Budget		10.4			dB	I_{FPK} = 60 mA, 0–70° C	
		12.8	15.6		dB	I_{FPK} = 60 mA, 25° C	Note 3

Notes:

1. For I_{FPK} > 80 mA, the duty factor must be such as to keep $I_{FAV} \leq 80$ mA. In addition, for I_{FPK} > 80 mA, the following rules for pulse width apply:
   $I_{FPK} \leq 160$ mA: Pulse width ≤ 1 ms
   $I_{FPK} > 160$ mA: Pulse width ≤ 1 μs
2. A bypass capacitor (0.01 μF to 0.1 μF ceramic) connected from pin 3 to pin 4 of the receiver is recommended for the HFBR-2503 and essential for the HFBR-2502. For the HFBR-2502, the total lead length between both ends of the capacitor and the pins should not exceed 20 mm.
3. Optical Power Budget = P_T Min. - $P_{R(L)}$ Min. Refer to HFBR-1502/1512 data sheet, HFBR-2502 data sheet, and HFBR-2503 data sheet, for additional design information.
4. In addition to a minimum power budget, care should be taken to avoid overdriving the HFBR-2503 receiver with too much optical power. For this reason power levels into the receiver should be kept less than -13.7 dBm to eliminate any overdrive with the recommended operating conditions.
5. Typical data is at 25° C, V_{CC} = 5 V.

Link Design Considerations

The HFBR-1512/2503 and HFBR-1502/2502 Transmitter/Receiver pairs are intended for applications where the photo interrupter must be physically separate from the optoelectronic emitter and detector. This separation would be useful where high voltage, electrical noise or explosive environments prohibit the use of electronic devices. To ensure reliable long term operation, links designed for this application should operate with an ample optical power margin $\alpha_M \geq 3$ dB, since the exposed fiber ends are subject to environmental contamination that will increase the optical attenuation of the slot with time. A graph of air gap separation versus attenuation for clean fiber ends with minimum radial error ≤ 0.005 inches (0.127 mm) and angular error ($\leq 3.0°$) is provided in Figure 2. The following equations can now be used to determine the transmitter output power, P_T, for both the overdrive and minimum drive cases. Overdrive is defined as a condition where excessive optical power is delivered to the receiver. The first equation enables the maximum P_T that will not result in receiver overdrive to be calculated for a predetermined link length and slot attenuation. The second equation defines the minimum P_T allowed for link operation.

$$P_T\,(MAX) - P_R\,(MAX) \leq \alpha_{O\ MIN}\ell + \alpha_{SLOT} \qquad \text{Eq. 1}$$

$$P_T\,(MIN) - P_{RL}\,(MIN) \geq \alpha_{O\ MAX}\ell + \alpha_{SLOT} + \alpha_M \qquad \text{Eq. 2}$$

Once P_T (MIN) has been determined in the second equation for a specific link length (ℓ), slot attenuation (α_{SLOT}) and margin (α_M), Figure 3 can then be used to find I_F.

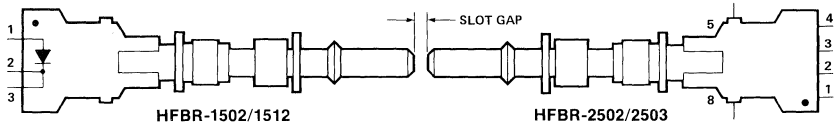


Figure 1. Typical Slot Interrupter Configuration. Refer to 1 MBd or Low Current Links for Schematic Diagrams

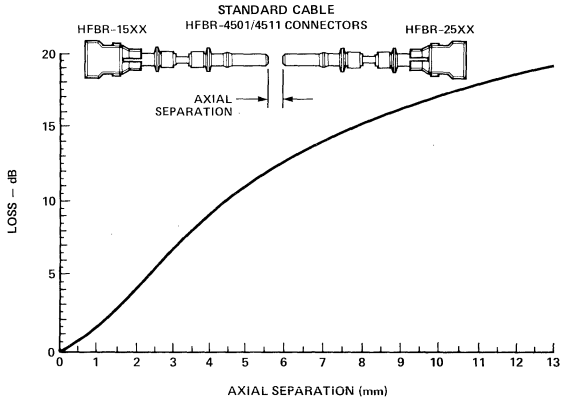


Figure 2. Typical Loss vs. Axial Separation

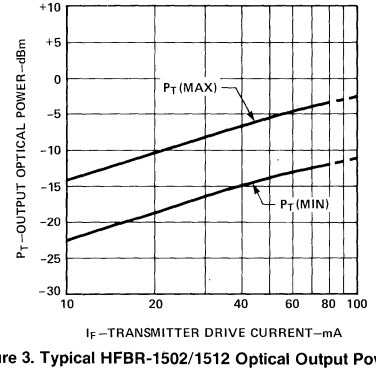


Figure 3. Typical HFBR-1502/1512 Optical Output Power vs. Transmitter I_F (0—70° C)

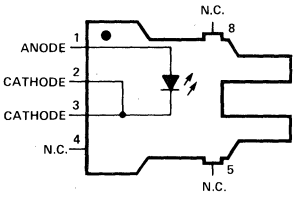
FIBER OPTICS

665 nm Transmitters

HFBR-1502/HFBR-1510 and HFBR-1512

The HFBR-1510/1502/1512 Transmitter modules incorporate a 665 nm LED emitting at a low attenuation wavelength for the HFBR-R/E plastic fiber optic cable. The transmitters can be easily interfaced to standard TTL logic. The optical power output of the HFBR-1510/1512/1502 is specified at the end of 0.5 m of cable. The HFBR-1512 output optical power is tested and guaranteed at low drive currents.

HFBR-1510/1512/1502 Transmitter



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec.	
Peak Forward Input Current		$I_{F\,PK}$		1000	mA	Note 2
Average Forward Input Current		$I_{F\,AV}$		80	mA	
Reverse Input Voltage		V_R		5	V	

Electrical/Optical Characteristics 0° C to +70° C Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Transmitter Output Optical Power	HFBR-1510	P_T	-16.5		-7.6	dBm	I_F = 60 mA, 0–70° C	
			-14.3		-8.0	dBm	I_F = 60 mA, 25° C	
	HFBR-1502 and HFBR-1512	P_T	-13.6		-4.5	dBm	I_F = 60 mA, 0–70° C	Fig. 2
			-11.2		-5.1	dBm	I_F = 60 mA, 25° C	Note 4
	HFBR-1512	P_T	-35.5			dBm	I_F = 2 mA, 0–70° C	Note 3
Output Optical Power Temperature Coefficient		$\frac{\Delta P_T}{\Delta T}$		-0.026		dB/° C		
Peak Emission Wavelength		λ_{PK}		665		nm		
Forward Voltage		V_F	1.45	1.67	2.02	V	I_F = 60 mA	
Forward Voltage Temperature Coefficient		$\frac{\Delta V_F}{\Delta T}$		-1.37		mV/° C		Fig. 1
Effective Diameter		D_T		1		mm		
Numerical Aperture		N.A.		0.5				
Reverse Input Breakdown Voltage		V_{BR}	5.0	12.4		V	I_F = -10 μA, T_A = 25° C	
Diode Capacitance		C_O		86		pF	V_F = 0, f = 1 MHz	
Rise and Fall Time		t_R, t_F		50		ns	10% to 90%	

Notes:
1. 1.6 mm below seating plane.
2. 1 μs pulse, 20 μs period.
3. Measured at the end of 0.5 m standard Fiber Optic Cable with large area detector.
4. Optical power, P (dBm) = 10 Log P (μW)/1000 μW.
5. Typical data is at 25° C.

WARNING. When viewed under some conditions, the optical port of the Transmitter may expose the eye beyond the Maximum Permissible Exposure recommended in ANSI Z-136-1, 1981. Under most viewing conditions there is no eye hazard.

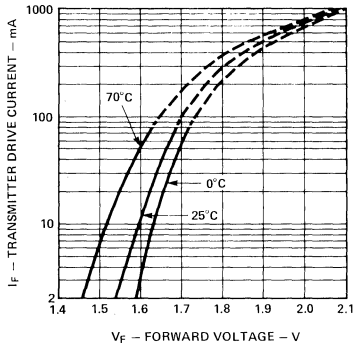


Figure 1. Typical Forward Voltage vs. Drive Current for HFBR-1510/1502/1512

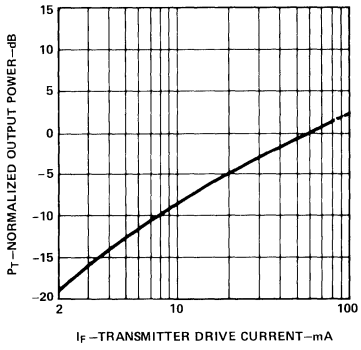


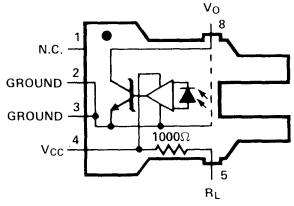
Figure 2. Normalized HFBR-1510/1502/1512 Typical Output Optical Power vs. Drive Current

Receivers

HFBR-2501 (5 MBd) and HFBR-2502 (1 MBd)

The HFBR-2501/2502 Receiver modules feature a shielded integrated photodetector and wide bandwidth DC amplifier for high EMI immunity. A Schottky clamped open-collector output transistor allows interfacing to common logic families and enables "wired-OR" circuit designs. The open collector output is specified up to 18V. An integrated 1000 ohm resistor internally connected to V_{CC} may be externally jumpered to provide a pull-up for ease-of-use with +5V logic. The combination of high optical power levels and fast transitions falling edge could result in distortion of the output signal (HFBR-2502 only), that could lead to multiple triggering of following circuitry.

HFBR-2501/2502 Receiver



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp			260	°C	Note 1
	Time			10	sec	
Supply Voltage		V_{CC}	-0.5	7	V	Note 6
Output Collector Current		I_O		25	mA	
Output Collector Power Dissipation		P_{OD}		40	mW	
Output Voltage		V_O	-0.5	18	V	
Pullup Voltage		V_{RL}	-0.5	V_{CC}	V	

Electrical/Optical Characteristics $0°C$ to $+70°C$, $4.75 \leq V_{CC} \leq 5.25$ Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Receiver Input Optical Power Level for Logic "0"	HFBR-2501	$P_{R(L)}$	-21.6		-9.5	dBm	0-70°C, V_{OL} = 0.5 V I_{OL} = 8 mA	Note 2, 3
			-21.6		-8.7	dBm	25°C, V_{OL} = 0.5 V I_{OL} = 8 mA	
	HFBR-2502	$P_{R(L)}$	-24			dBm	0-70°C, V_{OL} = 0.5 V I_{OL} = 8 mA	
			-24			dBm	25°C, V_{OL} = 0.5 V I_{OL} = 8 mA	
Input Optical Power Level for Logic "1"		$P_{R(H)}$			-43	dBm	V_{OH} = 5.25 V, $I_{OH} \leq 250\ \mu A$	Note 2
High Level Output Current		I_{OH}		5	250	μA	V_O = 18 V, P_R = 0	Note 4
Low Level Output Voltage		V_{OL}		0.4	0.5	V	I_{OL} = 8 mA, $P_R = P_{RL\ MIN}$	Note 4
High Level Supply Current		I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V, P_R = 0 μW	Note 4
Low Level Supply Current		I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V, P_R = -12.5 dBm	Note 4
Effective Diameter		D_R		1		mm		
Numerical Aperture		$N.A._R$		0.5				
Internal Pull-Up Resistor		R_L	680	1000	1700	Ohms		

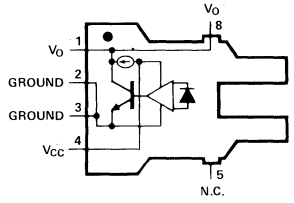
Notes:
1. 1.6 mm below seating plane.
2. Optical flux, P (dBm) = 10 Log P (μW)/1000 μW.
3. Measured at the end of standard Fiber Optic Cable with large area detector.
4. R_L is open.
5. Typical data is at 25°C, V_{CC} = 5 V.
6. It is essential that a bypass capacitor 0.01 μF to 0.1 μF be connected from pin 3 to pin 4 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.

High Sensitivity Receiver

HFBR-2503

The blue plastic HFBR-2503 Receiver module has a sensitivity of −39 dBm. It features an integrated photodetector and DC amplifier for high EMI immunity. The output is an open collector with a 150 μA internal current source pull-up and is compatible with TTL/LSTTL and most CMOS logic families. For minimum rise time add an external pull-up resistor of at least 3.3K ohms. V_{CC} must be greater than or equal to the supply voltage for the pull-up resistor.

HFBR-2503 Receiver



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	−40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp			260	°C	Note 1
	Time			10	sec	
Supply Voltage		V_{CC}	−0.5	7	V	Note 7
Output Collector Current (Average)		I_O	−1	5	mA	
Output Collector Power Dissipation		P_{OD}		25	mW	
Output Voltage		V_O	−0.5	V_{CC}	V	

Electrical/Optical Characteristics 0° C to +70° C, 4.5 ≤ V_{CC} ≤ 5.5 Unless Otherwise Specified

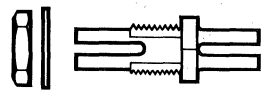
Parameter		Symbol	Min.	Typ. (5)	Max.	Units	Conditions	Ref.
Receiver Input Optical Power Level for Logic "0"	HFBR-2503	$P_{R(L)}$	−39		−13.7	dBm	0-70° C, $V_O = V_{OL}$ I_{OL} = 3.2 mA	Note 2, 3, 4
			−39		−13.3	dBm	25° C, $V_O = V_{OL}$ I_{OL} = 3.2 mA	
Input Optical Power Level for Logic "1"		$P_{R(H)}$			−53	dBm	V_{OH} = 5.5V, $I_{OH} \leq 40$ μA	Note 2
High Level Output Voltage		V_{OH}	2.4			V	I_{OH} = −40 μA, P_R = 0 μW	
Low Level Output Voltage		V_{OL}			0.4	V	I_{OL} = 3.2 mA, $P_R = P_{RL\ MIN}$	Note 6
High Level Supply Current		I_{CCH}		1.2	1.9	mA	V_{CC} = 5.5V, P_R = 0 μW	
Low Level Supply Current		I_{CCL}		2.9	3.7	mA	V_{CC} = 5.5V, $P_R \geq P_{RL}$ (MIN)	Note 6
Effective Diameter		D_R		1		mm		
Numerical Aperture		$N.A._R$		0.5				

Notes:
1. 1.6 mm below seating plane.
2. Optical flux, P (dBm) = 10 Log P (μW)/1000 μW.
3. Measured at the end of the standard Fiber Optic Cable with large area detector.
4. Because of the very high sensitivity of the HFBR-2503, the digital output may switch in response to ambient light levels when a cable is not occupying the receiver optical port. The designer should take care to filter out signals from this source if they pose a hazard to the system.
5. Typical data is at 25° C, V_{CC} = 5 V.
6. Including current in 3.3K pull-up resistor.
7. It is recommended that a bypass capacitor 0.01 μF to 0.1 μF ceramic be connected from pin 3 to pin 4 of the receiver.

Snap-in Fiber Optic Connector, Bulkhead Feedthrough/Splice and Polishing Tools

HFBR-4501 (GRAY)/4511 (BLUE) CONNECTOR

HFBR-4505 (GRAY)/4515 (BLUE) BULKHEAD FEEDTHROUGH



HFBR-4501/4511 CONNECTORS
HFBR-4505/4515 BULKHEAD FEEDTHROUGHS

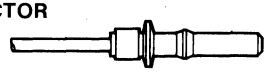
The HFBR-4501 and HFBR-4511 snap-in connectors terminate low cost plastic fiber cable and mate with the Hewlett-Packard HFBR-0500 family of fiber optic transmitters and receivers. They are quick and easy to install. The metal crimp ring provides strong and stable cable retention and the polishing technique ensures a smooth optical finish which results in consistently high optical coupling efficiency.

The HFBR-4505 and HFBR-4515 bulkhead feedthroughs mate two snap-in connectors and can be used either as an in-line splice or as a panel feedthrough for plastic fiber cable. The connector to connector loss is low and repeatable.

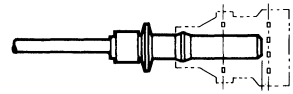
Applications

For further information on the connectors, please refer to the connectoring section of the Versatile Link section of the catalog.

- **CONNECTOR**

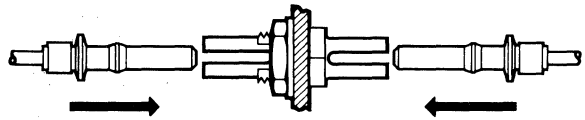


TERMINATION FOR HEWLETT-PACKARD PLASTIC FIBER OPTIC CABLE

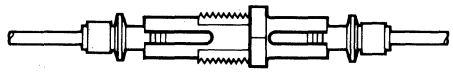


INTERFACE TO HEWLETT-PACKARD HFBR-15XX/25XX SNAP-IN FIBER OPTIC LINK COMPONENTS

- **BULKHEAD FEEDTHROUGH**



BULKHEAD FEEDTHROUGH OR PANEL MOUNTING OF HFBR-45XX CONNECTORS



IN-LINE SPLICE FOR PLASTIC FIBER OPTIC CABLE

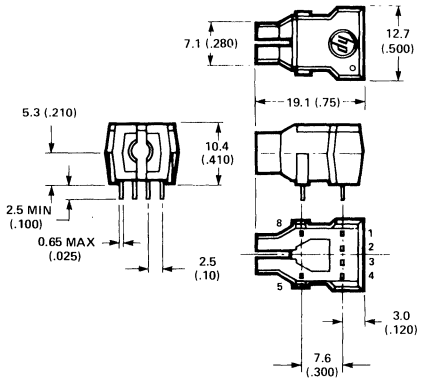
Cable Terminations

For a step-by-step guide to connectoring plastic cable, please refer to the connectoring section of the Versatile Link section of the catalog.

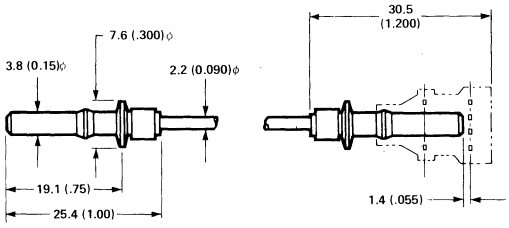
Mechanical Dimensions

All dimensions in mm (inches).
All dimensions ±0.25 mm unless otherwise specified.

HFBR-15XX (GRAY OR BLACK)/250X (BLUE) MODULE

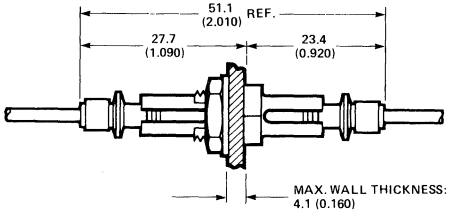


HFBR-4501 (GRAY)/4511 (BLUE) CONNECTOR

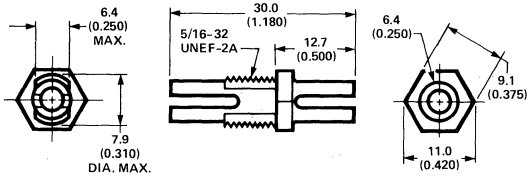


CONNECTORS DIFFER ONLY IN COLOR

BULKHEAD FEEDTHROUGH WITH TWO HFBR-4501/4511 CONNECTORS



HFBR-4505 (GRAY)/4515 (BLUE) BULKHEAD FEEDTHROUGH



BULKHEAD FEEDTHROUGHS DIFFER ONLY IN COLOR

FIBER OPTICS

HEWLETT PACKARD

Versatile Link
The Versatile Fiber Optic Connection

Technical Data

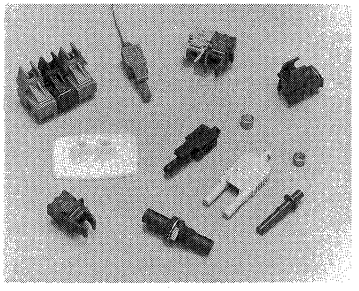
HFBR-0501 Series

Features

- **Low Cost Fiber Optic Components**
- **Guaranteed Link Performance over Temperature**
  Enhanced High Speed Links 2-50 MBd
  High Speed Links: dc to 5 MBd
  Extended Distance Links: up to 111 meters
  Low Current Link: 6 mA Peak Supply Current
  Low Cost Standard Link: dc to 1 MBd
  Photo-interrupter Link
- **Compact, Low Profile Packages**
  Horizontal and Vertical Mounting
  Interlocking Feature
  Flame Retardant
- **Easy to Use Receivers**
  TTL, CMOS Compatible Output Level
  High Noise Immunity
- **Easy Connectoring**
  Simplex, Duplex, and Latching Connectors
  Flame Retardant Material
- **Low Attenuation 1 mm Plastic Cable**
  Simplex and Zip Cord Style Duplex
  Extra Low Loss Simplex and Duplex
  UL VW-1 Flame Retardancy Conformance
- **No Optical Design Required**
- **Auto-Insertable and Wave Solderable**
- **Demonstrated Reliability at 40°C Exceeds 2 Million Hours MTBF**

Description

The Versatile Link series is a complete family of fiber optic link components for applications requiring a low cost solution. The HFBR-0501 series includes transmitters, receivers, connectors and cable specified for easy design. This series of components is ideal for solving problems with voltage isolation/insulation, EMI/RFI immunity or data security. The Link design is simplified by the logic compatible receivers and



complete specifications for each component. No optical design is necessary. The key optical and electrical parameters of links configured with the HFBR-0501 family are fully guaranteed from 0° to 70°C. A wide variety of package configurations and connectors provide the designer with numerous mechanical solutions to meet application requirements. The transmitter and receiver components have been designed for use in high volume/low cost assembly processes such as auto insertion and wave soldering.

Versatile Link Applications

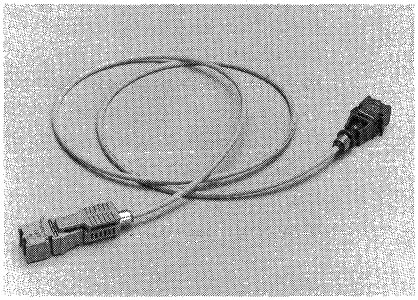
- Reduction of lightning/ voltage transient susceptibility
- Motor controller triggering
- Data communications and Local Area Networks
- Electromagnetic Compatibility (EMC) for regulated systems: FCC, VDE, CSA, etc.
- Tempest-secure data processing equipment
- Isolation in test and measurement instruments
- Error free signaling for industrial and manufacturing equipment
- Power supply control
- Communication and isolation in medical instruments
- Noise immune communication in audio and video equipment
- Remote photo interrupter for office and industrial equipment
- Robotics communication
- PC to peripheral links
- Intra-system links; board-to-board, rack-to-rack
- Digitized video
- Medical instruments

Link Selection Guide

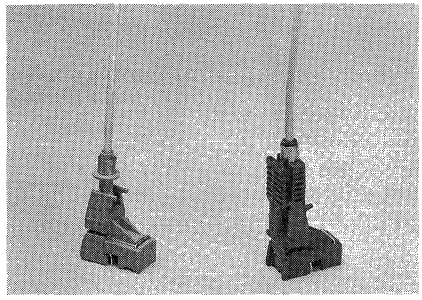
Versatile Link		Guaranteed Minimum Link Length (Meters)				Typical Link Length (Meters)	
		0°C-70°C		25°C		25°C	
		Standard Cable	Extra Low Loss Cable	Standard Cable	Extra Low Loss Cable	Standard Cable	Extra Low Loss Cable
50 MBd Link	50 MBd	15	17	–	–	59	65
High Performance	5 MBd	19	22	27	32	48	53
High Performance	1 MBd	39	45	47	56	70	78
Low Current Link	40 kBd	13	15	–	–	41	45
Extended Distance Link	40 kBd	94	111	103	121	138	154
Standard	1 MBd	8	10	17	20	43	48
Photo Interrupter	500 kHz	NA	NA	NA	NA	NA	NA
Evaluation Kit	1 MBd (Standard)	Contents: Horizontal transmitter, horizontal receiver packages; 5 meters of simplex cable with simplex and simplex latching connectors installed; individual connectors: simplex, duplex, simplex latching, bulkhead adapter, polisihng tool, abrasive paper, literature.					

Versatile Link Product Family

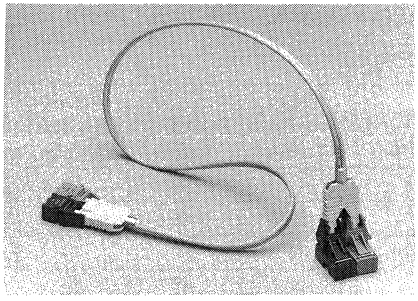
50 MBd, 5 MBd, 1 MBd and 40 kBd Fiber Optic Links



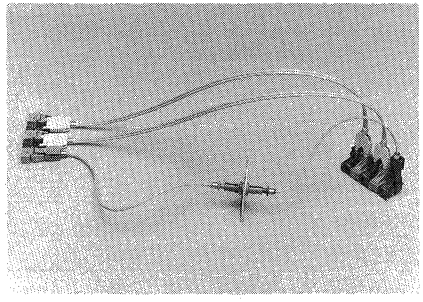
Simplex Link–Horizontal Packages



Simplex Link–Vertical Packages



Duplex Link–Combination of Horizontal & Vertical Packages



N-Plex Link–Combinations

Versatile Link Product Description

Mechanical: The compact Versatile Link package is made of a flame retardant material (UL V-0) in a standard, eight pin dual-in-line package (DIP) with 7.6 millimeter (0.3 inch) pin spacing. Vertical and horizontal mountable parts are available. These low profile Versatile Link packages are stackable and are enclosed to provide a dust resistant seal. Snap action simplex, simplex latching, duplex, and duplex latching connectors are offered with simplex or duplex cables.

Electrical: Transmitters incorporate a 660 nanometer light emitting diode (LED). Receivers include a monolithic dc coupled, digital IC receiver with open collector Schottky output transistor. An internal pullup resistor is available for use in the HFBR-25X1/2/4 receivers. Transmitter and receiver are compatible with standard TTL circuitry. A shield has been integrated into the receiver IC to provide additional, localized noise immunity.

Optical: Internal optics have been optimized for use with 1 mm diameter plastic optical fiber. Versatile Link specifications incorporate all component interface losses. Therefore, the need of optical calculations for common link applications is eliminated.

Optical power budget is graphically displayed to facilitate electrical design for customized links.

Designing with Versatile Link

When designing with Versatile Link the following topics should be considered:

Distance and Data Rate

Distances and data rates guaranteed with Versatile Link depend upon the Versatile Link transmitter/receiver pair chosen.

Typically a data rate requirement is first specified. This determines the choice of the 50 MBd, 5 MBd, 1 MBd, or 40 kBd Versatile Link components. Distances guaranteed with Versatile Link then depend upon choice of cable, specific drive condition and circuit configuration. Extended distance operation is possible with pulsed operation of the LED (see Figure 2a, 2b, 2c, 2d, 2e, and 2f dotted lines.)

Drive circuits are described in the Link Design sections. Cable is discussed in the Plastic Cable section. Pulsed operation of the LED at larger current will result in increased pulse width distortion of the receiver output signal.

Versatile Link can also be used as a photo interrupter at frequencies up to 500 KHz.

Package Orientation

As shown in the photograph Versatile Link is available in vertical and horizontal packages. Performance and pinouts for the two packages are identical. To provide additional attachment support for the Vertical Versatile Link housing, the designer has the option of using a self-tapping screw through a printed circuit board into a mounting hole at the bottom of the package. For most applications this is not necessary.

Package Housing Color

Versatile Link components and simplex connectors are color coded to eliminate confusion when making connections. The HFBR-15X1/2/4/6 transmitters are gray and the HFBR-25X1/2/3/4/6 receivers are blue. The HFBR-15X3 transmitter is black.

All of the above transmitter and receivers are also available in black versions for special applications. These black components combined with black fiber optic cable form a "black link" which has superior immunity to external light. The black link is appropriate where improved housing opacity is required due to very bright ambient light or bright flashes of light. Black link components are otherwise identical to blue and gray components.

Connector Style

As shown, Versatile Link can be used with snap-in connectors: simplex, simplex latching, duplex, and duplex latching.

The simplex connector is intended for applications requiring simple, stable connection capability with a moderate retention force. The simplex latching connector provides similar convenience with a larger retention force. Connector/cable retention force can be improved by using an RTV adhesive within the connector. A suggested adhesive is GE Company RTV-128 or Dow Corning 3154.

The duplex connector connects a cable containing two fibers to two similar Versatile Link components. A lockout feature ensures the connection can be made in only one orientation. The duplex connector is intended for Versatile Link components interlocked together as discussed in the next section.

Stacking

Versatile Link components can be stacked or interlocked together to minimize use of printed circuit board space and provide efficient, dual connections with the duplex connector. Up to eight identical package styles can be interlocked and inserted by hand into a printed circuit board without difficulty. However, auto-insertion of stacked units becomes limited when more than two packages are interlocked together.

Plastic Cable

Two 1 mm plastic cable versions are available: simplex (single channel) and marked duplex (dual channel). Each version of the low optical loss cable complies with the UL VW-1 flame retardancy specification. Two grades of plastic cable are available: standard attenuation and extra low-loss attenuation. Extra low-loss cable is recommended for applications requiring longer distance needs, as reflected in the Link Selection Guide. Flexible cable construction allows simple cable installation techniques. Cables are discussed in detail in the Plastic Cable section.

Accessories

A variety of accessories are available. The bulkhead feed-through adapter discussed in the Mechanical Dimensions section is designed to mate two simplex snap-in connectors to act as either a splice or panel feedthrough for a panel thickness <4.1 mm (0.16 inch).

Several accessories are offered to help with proper fiber/connector polishing. These are shown in the Mechanical Dimensions section.

Manufacturing with Versatile Link

Non-stacked Versatile Link parts require no special handling during assembly of units onto printed circuit boards. Versatile Link components are auto-insertable. When wave soldering is performed with Versatile Link components, an optical port plug is recommended to be used to prevent contamination of the port. Water soluble fluxes, not rosin based fluxes, are recommended for use with Versatile Link components.

Refer to the Connectoring Section for details of connectors and cable connectoring.

Versatile Link Performance

50 MBd Link Performance

The HFBR-15X6 transmitter is a 660 nm LED in a low cost plastic housing designed to efficiently couple power into 1 mm diameter plastic optical fiber. With the recommended drive circuit, the LED operates at speeds from 2-50 MBd. The HFBR-25X6 is a high bandwidth analog receiver with a PIN photo diode and internal transimpedance amplifier. The transmitter and receiver interface to plastic optical fiber, which is easily terminated with the HP Versatile Link family connectors. These components can be used for high speed data links without the problems common to copper wire solutions at a competitive cost.

HFBR-0506 Series 50 MBd Data Link

Data link operating conditions and performance are specified for the HFBR-15X6 transmitter and HFBR-26X6 receiver in the recommended applications circuits shown in Figures 1, 2, and 3. These circuits have been optimized for 50 MBd operation. The Applications Engineering Department in the Hewlett-Packard Optical Communication Division is available to assist in optimizing link performance for higher or lower speed operation.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Reference
Ambient Temperature	T_A	0	70	°C	
Supply Voltage	V_{CC}	+4.75	+5.25	V	
Data Input Voltage - Low	V_{IL}	V_{CC} - 1.89	V_{CC} - 1.62	V	
Data Input Voltage - High	V_{IH}	V_{CC} - 1.06	V_{CC} - 0.70	V	
Data Output Load	R_L	45	55	Ω	Note 1
Signaling Rate	f_S	2	50	MBd	
Duty Cycle	D.C.	40	60	%	Note 2

Link Performance: 2-50 MBd, BER ≤ 10^{-9}, under recommended operating conditions with recommended transmit and receive application circuits, with transmitter and receiver locked together.

Parameter	Symbol	Min.[3]	Typ.[4]	Max.	Unit	Condition	Reference
Optical Power Budget with 1 mm Plastic Optical Fiber	OPB		16.5		dB	25°C	
		8.1	14.0		dB	0-70°C	Note 5
Link Distance with Standard Cable	ℓ		59		m	25°C	
		15	42		m	0-70°C	Note 6, 7, 8
Link Distance with Extra Low Loss Cable	ℓ		65		m	25°C	
		17	46		m	0-70°C	Note 6, 7, 8

Notes:

1. If the output of U1C in Figure 2, page 106 is transmitted via coaxial cable, terminate with a 50 Ω resistor to V_{CC} - 2 V.
2. Run length limited code with maximum run length of 10 µs.
3. Minimum link performance is projected based on the worst case specifications of the HFBR-15X6 transmitter, HFBR-25X6 receiver, and cable attenuation, and the typical performance of other circuit components (e.g. logic gates, transistors, resistors, capacitors, quantizer).
4. Typical performance measured with typical values of all circuit components.
5. When the transmitter and receiver are separated by at least 4 cm, the minimum optical power budget is 10.1 dB. When the transmitter and receiver are locked together, coupled electrical noise (crosstalk) from the transmitter circuit reduces the receiver sensitivity by 2 dB, and the minimum optical power budget is also reduced by 2 dB to 8.1 dB as specified in the table above.
6. Standard cable is HFBR-RXXYYY plastic optical fiber, with a maximum attenuation of 0.240 dB/m at 650 nm and NA = 0.5. Extra low loss cable is HFBR-EXXYYY plastic optical fiber, with a maximum attenuation of 0.190 dB/m at 650 nm and NA = 0.5.
7. Minimum link distances when the transmitter and receiver are separated by at least 4 cm is 23 metres for standard cable and 25 metres for extra low loss cable (see Note 5).
8. Plastic optical fiber has a spectral attenuation minimum at 650 nm. Because the LED wavelength shifts with temperature, the minimum link distance over 0-70°C is less than the optical power budget (OPB) divided by the maximum attenuation of the fiber at 650 nm. From 25°C to 70°C, the LED wavelength increases as much as 10 nm, causing the fiber attenuation at 70°C to be as much as 0.5 dB/m greater than the attenuation at 25°C.

50 MBd Link Design Considerations

Transmitter Application Circuit: Performance of the HFBR-15X6 transmitter in the recommended application circuit (Figure 1); 2-50 MBd, 25°C, unless otherwise stated.

Parameter	Symbol	Typical	Unit	Condition	Reference
Average Optical Power	P_{avg}	-8.8 130	dBm μW	50% Duty Cycle	Note 1, Figure 4
Average Modulated Power	P_{mod}	-12.2 60	dBm μW		Note 2, Figure 4
Optical Rise Time (10% to 90%)	t_r	5.0	ns	1 MHz	
Optical Fall Time (90% to 10%)	t_f	6.0	ns	1 MHz	
Extinction Ratio		2.8:1			
Optical Overshoot		50	%		
Hold-on Current	I_O	30	mA		Note 3
Transmitter Application Circuit Current Consumption	I_{CC}	240	mA		Figure 1

Receiver Application Circuit: Performance[4] of the HFBR-25X6 receiver in the recommended application circuit (Figure 2); 2-50 MBd, 25°C, unless otherwise stated.

Parameter	Symbol	Typical	Unit	Condition	Reference
Data Output Voltage - Low	V_{OL}	V_{CC} - 1.7	V	R_L = 50 Ω	Note 5
Data Output Voltage - High	V_{OH}	V_{CC} - 0.9	V	R_L = 50 Ω	Note 5
Receiver Sensitivity to Average Modulated Optical Power	P_{min}	-28.7 1.4	dBm μW	50% eye opening	Note 2, 6
Receiver Overdrive Level of Average Modulated Optical Power	P_{max}	-8.4 145	dBm μW	50% eye opening	Note 2
Receiver Application Circuit Current Consumption	I_{CC}	85	mA	R_L = Inf.	Figure 2

Notes:

1. Average optical power is measured with an average power meter, at a 50% duty cycle.
2. To allow the LED to switch at high speeds, the recommended drive circuit never switches the LED fully off; the light output power is modulated between two non-zero power levels. The modulated (useful) power is the difference between the high and low level of light output power (transmitted) or input power (received), which can be measured with an average power meter as a function of duty cycle (see Figure 4). *Average modulated power* is defined as one half the slope of the average power versus duty cycle:

$$\text{Average Modulated Power} = \frac{[P_{avg} @ \text{ 80\% duty cycle} - P_{avg} @ \text{ 20\% duty cycle}]}{(2)[0.80 - 0.20]}$$

3. Hold-on Current is the low light level current through the HFBR-15X6 transmitter.
4. Performance in response to a signal from the HFBR-15X6 driven with the recommended circuit at 2-50 MBd over 1-17 metres of HFBR-R/EXXYYY plastic optical fiber.
5. Terminated through a 50 Ω resistor to V_{CC} - 2 V.
6. When the transmitter and receiver are separated by at least 4 cm, the receiver sensitivity is -30.7 dBm. However, when the transmitter and receiver are locked together, coupled electrical noise (crosstalk) from the transmitter circuit reduces the receiver sensitivity by 2 dB to -28.7 dBm.
7. If there is no input optical power to the receiver, electrical noise can result in false triggering of the receiver. In typical applications, data encoding and error detection prevent random triggering from being interpreted as valid data. Refer to Application Note 1045 for design guidelines.

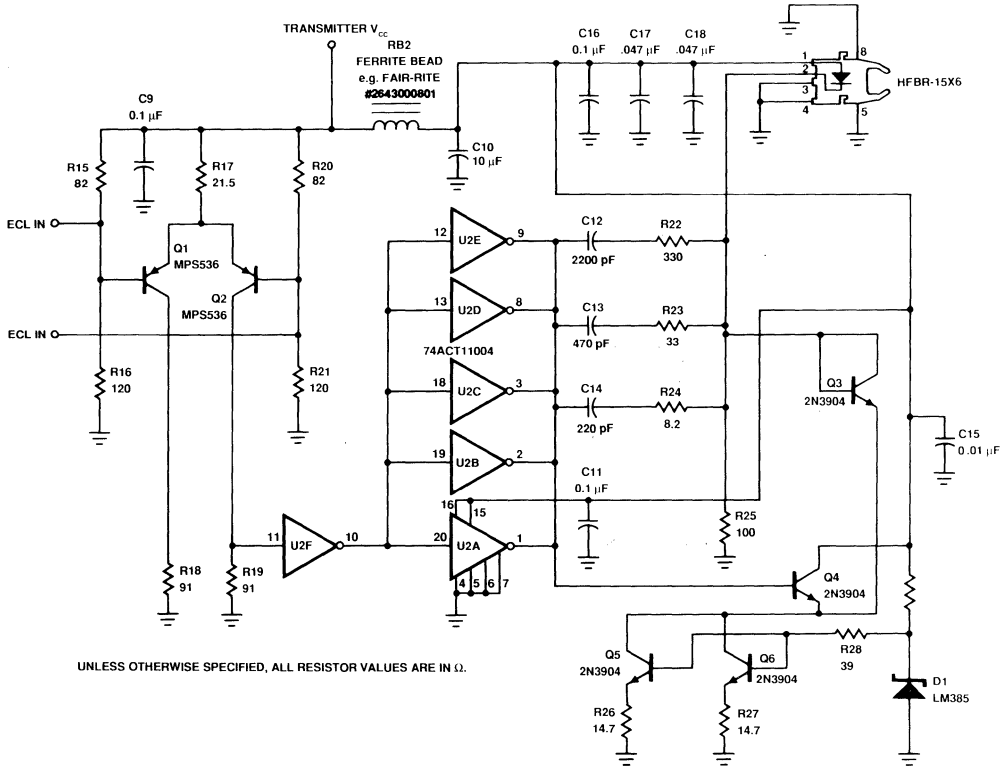


Figure 1. Transmitter Application Circuit with +5 V ECL Inputs.

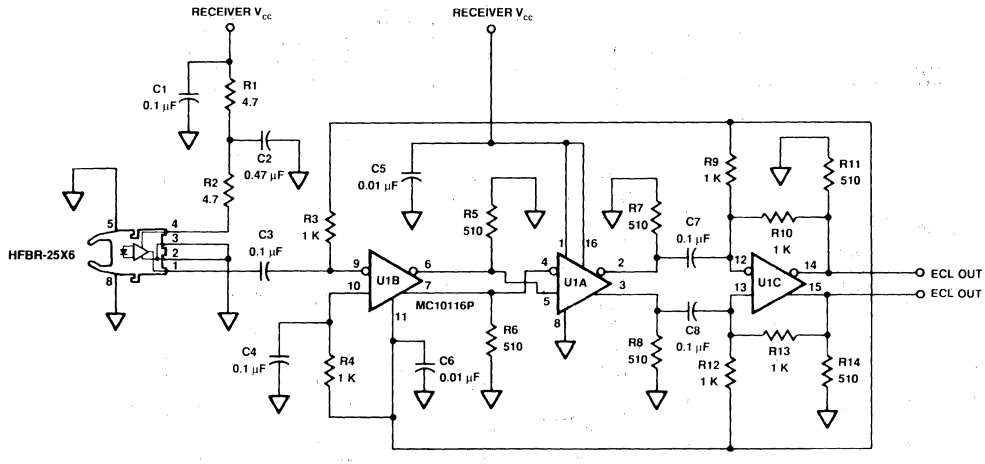


Figure 2. Receiver Application Circuit with +5 V ECL Outputs.

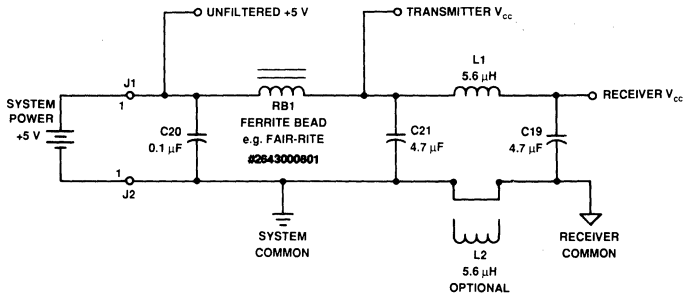


Figure 3. Power Distribution and Filter.

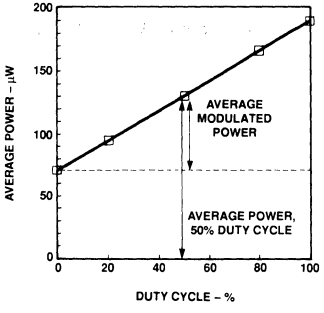


Figure 4. Average Modulated Power.

5 MBd, 1 MBd, and 40 kBd Link Performance

The 5 Megabaud (MBd) Versatile Link is guaranteed to perform from dc to 5 Mb/s (megabits per second, NRZ). Distances up to 22 meters are guaranteed when the transmitter is driven with a current of 60 milliamperes. This represents worst case performance throughout the temperature range of 0 to 70 degrees centigrade. With the required drive circuit of Figure lb and at 60 milliamp drive current, the High Performance 1 Megabaud Versatile Link has guaranteed performance over 0° to 70°C from dc to 1 Mb/s (NRZ) up to 45 meters.

The low current link requires only 6 mA peak supply current for the transmitter and receiver combined to achieve a 15 meter link. Extended distances up to 111 meters can be achieved at a maximum transmitter drive current of 60 mA peak. The 40 kBd Versatile Link is guaranteed to perform from dc to 40 kb/s (NRZ) over 0° - to 70°C up to the distances just described.

Receivers are compatible with LSTTL, TTL, CMOS logic levels and offer a choice of an internal pull-up resistor or an open collector output. Horizontal or vertical packages provide identical performance and are compatible with simplex, simplex latching, duplex, and duplex latching connectors. Refer to the Connector Section and the Cable Section for further information about these products. A list of specific part numbers is found below and in the Link Selection Guide.

5 MBd, 1 MBd, and 40 kBd Link Guide

Versatile Link		Unit	Horizontal Package	Vertical Package	Cable Link Length (0°C-70°C)	
					Standard Cable	Extra Low Loss Cable
High Performance	5 MBd	Tx	HFBR-1521	HFBR-1531	19 meters	22 meters
		Rx	HFBR-2521	HFBR-2531		
High Performance	1 MBd	Tx	HFBR-1522	HFBR-1532	39 meters	45 meters
		Rx	HFBR-2522	HFBR-2532		
Low Current/ Extended Distance	40 kBd	Tx	HFBR-1523	HFBR-1533	13 meters/ 94 meters	15 meters/ 111 meters
		Rx	HFBR-2523	HFBR-2533		
Standard	1 MBd	Tx	HFBR-1524	HFBR-1534	8 meters	10 meters
		Rx	HFBR-2524	HFBR-2534		

Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Units	Ref.
Ambient Temperature		T_A	0	70	°C	
Transmitter Peak Forward Current		$I_{F\,PK}$	10	750	mA	Note 1, 8
Average Forward Current		$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	HFBR-25X3	V_{CC}	4.50	5.50	V	Note 2
	HFBR-25X1/25X2/25X4		4.75	5.25		
Output Voltage	HFBR-25X3	V_O		V_{CC}	V	
	HFBR-25X1/25X2/25X4			18		
Fanout (TTL)	HFBR-25X3	N		1		
	HFBR-25X1/25X2/25X4			5		

System Performance Under recommended operating conditions unless otherwise specified.

Link	Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
High Performance 5 MBd	Data Rate		dc		5	MBd	BER ≤ 10^{-9}, PRBS: 2^7 - 1	
	Link Distance with Standard Cable	ℓ	19			m	I_{Fdc} = 60 mA	Fig. 2a Note 7
			27	48		m	I_{Fdc} = 60 mA, 25°C	
	Link Distance with Extra Low Loss Cable	ℓ	22			m	I_{Fdc} = 60 mA	Fig. 2b Note 7
			32	53		m	I_{Fdc} = 60 mA, 25°C	
	Propagation Delay	t_{PLH}		80	140	ns	R_L = 560 Ω, C_L = 30 pF ℓ = 0.5 metre -21.6 ≤ P_R ≤ -9.5 dBm	Fig. 3, 5 Notes 3, 6
		t_{PHL}		50	140	ns		
	Pulse Width Distortion	t_D		30		ns	P_R = -15 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 3, 4 Note 4
High Performance 1 MBd	Data Rate		dc		1	MBd	BER ≤ 10^{-9}, PRBS: 2^7 - 1	
	Link Distance with Standard Cable	ℓ	39			m	I_{Fdc} = 60 mA	Fig. 2a Notes 1, 7, 8
			47	70		m	I_{Fdc} = 60 mA, 25°C	
	Link Distance with Extra Low Loss Cable	ℓ	45			m	I_{Fdc} = 60 mA	Fig. 2b Notes 1, 7, 8
			56	78		m	I_{Fdc} = 60 mA, 25°C	
	Propagation Delay	t_{PLH}		180	250	ns	R_L = 560 Ω, C_L = 30 pF ℓ = 0.5 metre P_R = -24 dBm	Fig. 3, 5 Notes 3, 8
		t_{PHL}		100	140	ns		
	Pulse Width Distortion	t_D		80		ns	P_R = -24 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 3, 4 Notes 4, 8

System Performance Under recommended operating conditions unless otherwise specified, contd.

Link	Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Low Current/ Extended Distance 40 kBd	Data Rate		dc		40	kBd	BER ≤ 10^{-9}, PRBS: 2^7 - 1	
	Link Distance with Standard Cable	ℓ	13	41		m	I_{Fdc} = 2 mA	Fig. 2c Note 7
			94	138		m	I_{Fdc} = 60 mA	
	Link Distance with Extra Low Loss Cable	ℓ	15	45		m	I_{Fdc} = 2 mA	Fig. 2d Note 7
			111	154		m	I_{Fdc} = 60 mA	
	Propagation Delay	t_{PLH}		4		µs	R_L = 3.3 kΩ, C_L = 30 pF ℓ = 1 metre P_R = -25 dBm	Fig. 3, 7 Note 3
		t_{PHL}		2.5		µs		
	Pulse Width Distortion	t_D			7.0	µs	-39 ≤ P_R ≤ -14 dBm R_L = 3.3 kΩ, C_L = 30 pF	Fig. 3, 6 Note 4
Standard 1 MBd	Data Rate	ℓ	dc		1	MBd	BER ≤ 10^{-9}, PRBS: 2^7 - 1	
	Link Distance with Standard Cable	ℓ	8			m	I_{Fdc} = 60 mA	Fig. 2e Notes 1, 7, 8
			17	43		m	I_{Fdc} = 60 mA, 25°C	
	Link Distance with Extra Low Loss Cable		10			m	I_{Fdc} = 60 mA	Fig. 2f Notes 1, 7, 8
			19	48		m	I_{Fdc} = 60 mA, 25°C	
	Propagation Delay	t_{PLH}		180	250	ns	R_L = 560 Ω, C_L = 30 pF ℓ = 0.5 metre P_R = -20 dBm	Fig. 3, 5 Notes 3, 8
		t_{PHL}		100	140	ns		
	Pulse Width Distortion	t_D		80		ns	P_R = -20 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 3, 4 Notes 4, 8

Notes:

1. For I_{FPK} > 80 mA, the duty factor must be such as to keep I_{FDC} ≤ 80 mA. In addition, for I_{FPK} > 80 mA, the following rules for pulse width apply:
   I_{FPK} ≤ 160 mA: Pulse width ≤ 1 ms
   I_{FPK} ≥ 160 mA: Pulse width ≤ 1 µs, period ≥ 20 µS.
2. It is essential that a bypass capacitor, 0.1 µF ceramic, be connected from pin 2 to pin 3 of the HFBR-25X1/25X2/25X4 receivers and from pin 2 to pin 4 of the HFBR-25X3 receiver. Total lead length between both ends of the capacitor and the supply pins should not exceed 20 mm.
3. The propagation delay for one metre of cable is typically 5 ns.
4. $t_D = t_{PLH} - t_{PHL}$.
5. Typical data is at 25°C, V_{CC} = 5 V.
6. Typical propagation delay is measured at P_R = -15 dBm.
7. Estimated typical link life expectancy at 40°C exceeds 10 years at 60 mA.
8. Pulsed LED operation at I_{FPK} > 80 mA will cause increased link t_{PLH} propagation delay time. This extended t_{PLH} time contributes to increased pulse width distortion of the receiver output signal.
9. Pins 5 and 8 of both the transmitter and receiver are for mounting and retaining purposes only. Do not electrically connect pin 5 and/or pin 8.

5 MBd, 1 MBd, and 40 kBd Link Design Considerations

Simple interface circuits for use with the 5 MBd, 1 MBd and 40 kBd Versatile Links are shown in Figure 1. The value of the transmitter drive current depends upon the desired link distance. This is shown in Figures 2a through 2f. After selecting a value of transmitter drive current, I_F, the value of R1 can be determined with the aid of Figures 1a, 1b, and 1d. Note that the 5 MBd and 40 kBd Versatile Links can have an overdrive and underdrive limit for the chosen value of I_F while the 1 MBd Versatile Link has only an underdrive limit. Dotted lines in Figures 2a through 2f represent pulsed operation for extended link distance requirements. For the HFBR-1522/1532/1524/1534 interface circuit, the R1Cl time constant must be > 75 ns. Conditions described in Note 1 must be met for pulse operation. Refer to Note 8 for performance comments when pulse operation is used.

All specifications are guard-banded for worst case conditions between 0 to 70 degrees centigrade. All tolerances and variations (including end-of-line transmitter power, receiver sensitivity, coupling variances connector and cable variations) are taken into account.

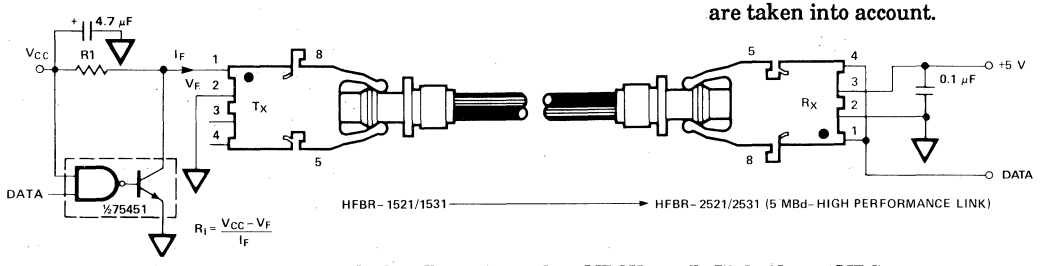


Figure 1a. Typical Interface Circuit for the HFBR-1521/1531, the 5 MBd Versatile Link (dc to 5 MBd).

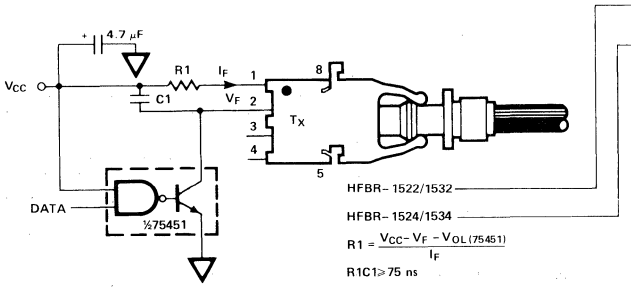


Figure 1b. Required Interface Circuit for the HFBR-1522/1532/1524/1534, the 1 MBd Versatile Link (dc to 1 MBd).

PIN	Tx	Rx
1	ANODE	V_o
2	CATHODE	GND
3	OPEN	V_{CC}
4	OPEN	R_L
5	PIN 8*	PIN 8*
8	PIN 5*	PIN 5*

*PINS 5 AND 8 CONNECTED INTERNALLY TO EACH OTHER ONLY.

Figure 1c. Electrical Pin Assignments for 5 MBd and 1 MBd Transmitters and Receivers.

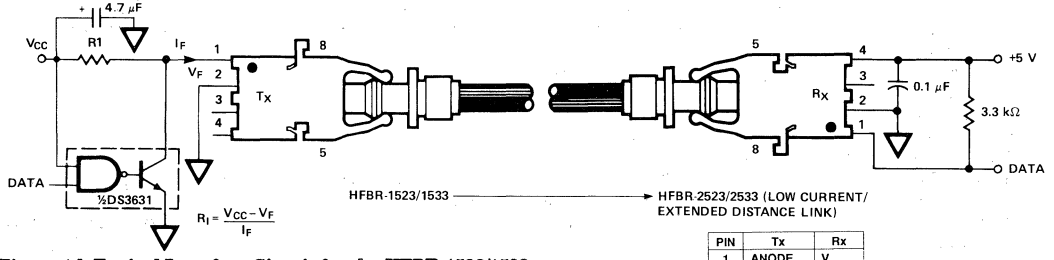


Figure 1d. Typical Interface Circuit for the HFBR-1523/1533, the 40 kBd Versatile Link (dc to 40 kBd).

PIN	Tx	Rx
1	ANODE	V_o
2	CATHODE	GND
3	OPEN	OPEN
4	OPEN	V_{CC}
5	PIN 8*	PIN 8*
8	PIN 5*	PIN 5*

*PINS 5 AND 8 CONNECTED INTERNALLY TO EACH OTHER ONLY.

Figure 1e. Electrical Pin Assignments for 40 kBd Transmitters and Receivers.

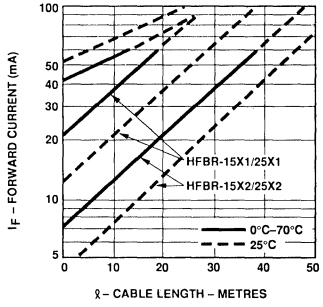


Figure 2a. Guaranteed System Performance for the HFBR-15X1/25X1 and HFBR-15X2/25X2 Links with Standard Cable.

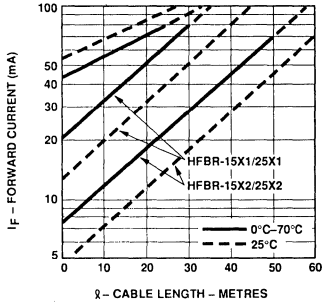


Figure 2b. Guaranteed System Performance for the HFBR-15X1/25X1 and HFBR-15X2/25X2 Links with Extra Low Loss Cable.

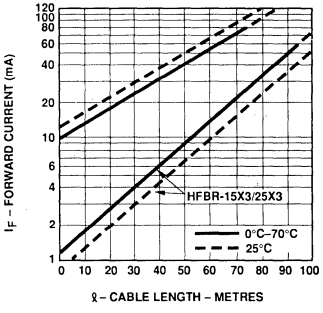


Figure 2c. Guaranteed System Performance for the HFBR-15X3/25X3 Link with Standard Cable.

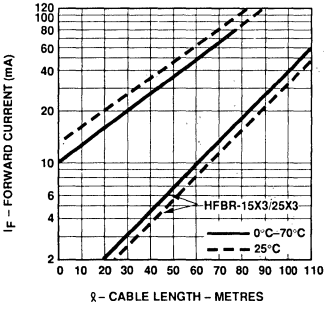


Figure 2d. Guaranteed System Performance for the HFBR-15X3/25X3 Link with Extra Low Loss Cable.

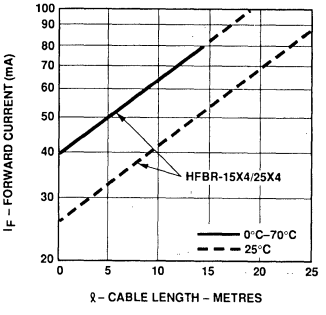


Figure 2e. Guaranteed System Performance for the HFBR-15X4/25X4 Link with Standard Cable.

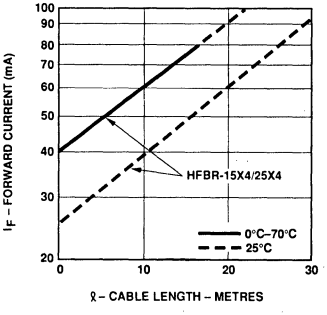


Figure 2f. Guaranteed System Performance for the HFBR-15X4/25X4 Link with Extra Low Loss Cable.

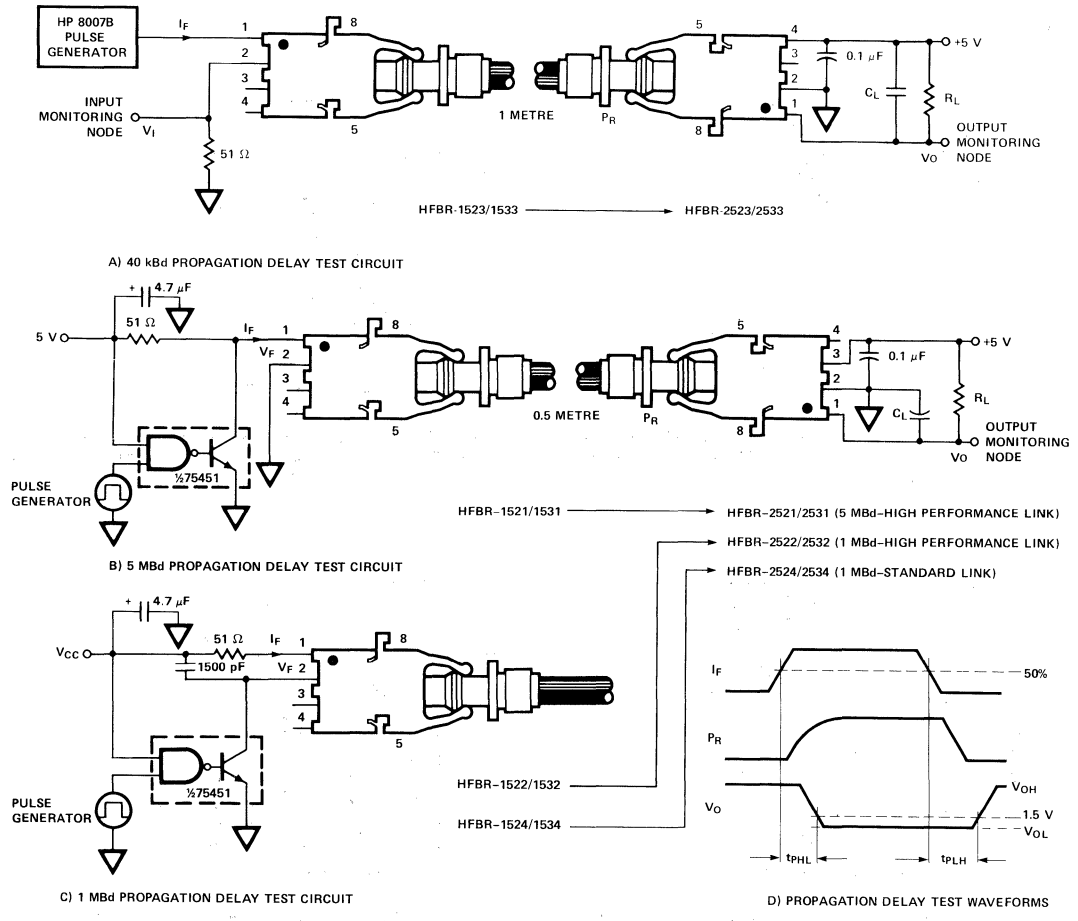


Figure 3. Propagation Delay Test Circuits and Waveforms: a) 40 kBd, b) 5 MBd, c) 1 MBd, d) Test Waveforms.

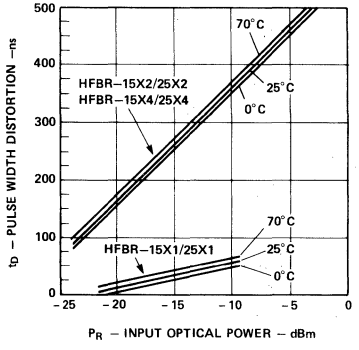


Figure 4. Typical HFBR-15X1/25X1, HFBR-15X2/25X2 and HFBR-15X4/25X4 Link Pulse Width Distortion vs. Optical Power.

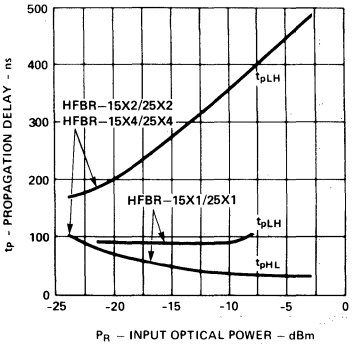


Figure 5. Typical HFBR-15X1/25X1, HFBR-15X2/25X2 and HFBR-15X4/25X4 Link Propagation Delay vs. Optical Power.

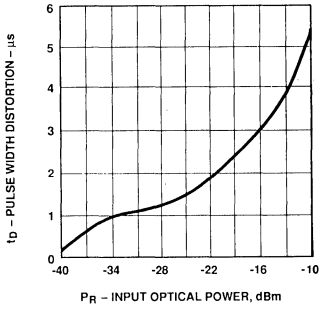


Figure 6. Typical HFBR-15X3/-25X3 Link Pulse Width Distortion vs. Optical Power.

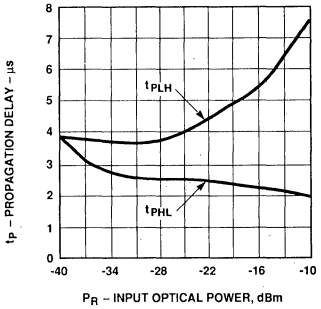


Figure 7. Typical HFBR-15X3/-25X3 Link Propagation Delay vs. Optical Power.

Photo-interrupter Link Performance 20 kHz (40 kBd) Link, 500 kHz (1 MBd) Link

Versatile Link may be used as a photo-interrupter in optical switches, shaft position sensors, velocity sensors, position sensors, and other similar applications. This link is particularly useful where high voltage, electrical noise, or explosive environments prohibit the use of electromechanical or optoelectronic sensors. The 20 kHz (40 kBd) transmitter/receiver pair has an optical power budget of 25 dB. The 500 kHz (1 MBd) transmitter/receiver pair has an optical power budget of 10 dB. Total system losses (cable attenuation, air gap loss, etc.) must not exceed the link optical power budget.

Recommended Operating Conditions

Recommended operating conditions are identical to those of the Low Current/Extended Distance and High Performance 1 MBd links. Refer to page 15.

System Performance

These specifications apply when using Standard and Extra-Low Loss cable and, unless otherwise specified, under recommended operating conditions. Refer to the appropriate link data on pages 5-17 and 5-18 for additional design information.

Parameter	Min.	Typ.[1]	Max.	Units	Conditions	Ref.
HFBR-15X3/25X3						
Max. Count Frequency	dc		20	kHz		
Optical Power Budget	25.4			dB	I_{Fdc} = 60 mA, 0-70°C	Note 2
	27.8	34		dB	I_{Fdc} = 60 mA, 25°C	
HFBR-15X2/25X2						
Max. Count Frequency	dc		500	kHz		
Optical Power Budget	10.4			dB	I_{Fdc} = 60 mA, 0-70°C	Note 2
	12.8	15.6		dB	I_{Fdc} = 60 mA, 25°C	

1. Typical data is at T_A = 25°C. V_{CC} = 5 V.
2. Optical Power Budget = P_T min. = P_R (L) min. Refer to the Link Design section for additional design information.

Photo-interrupter Link Design Considerations

The fiber optic Transmitter/ Receiver pair is intended for applications where the photo interrupter must be physically separated from the optoelectronic emitter and detector This separation would be useful where high voltage, electrical noise or explosive environments prohibit the use of electronic devices. To ensure reliable long term operation, link design for this application should operate with an ample optical power margin $\alpha_M \geq 3$ dB, since the exposed fiber ends are subject to environmental contamination that will increase the optical attenuation of the slot with time. A graph of air gap separation versus attenuation for clean fiber ends with minimum radial error ≤ 0.127 mm (0.005 inches) and angular error (≤3.0°) is provided In Figure 8.

The following equations can be used to determine the transmitter output power, P_T, for both the overdrive and underdrive cases. Overdrive is defined as a condition where excessive optical power is delivered to the receiver. The first equation calculates, for a predetermined link length and slot attenuation. The maximum P_T in order not to overdrive the receiver The second equation defines the minimum P_T allowed for link operation to prevent underdrive condition from occurring, where α_o is the fiber attenuation.

$$P_T (MAX) - P_R (MAX) \leq \alpha_{o\,MIN}\, \ell + \alpha_{SLOT} \quad \text{Eq. 1}$$

$$P_T (MIN) - P_{RL} (MIN) \geq \alpha_{o\,MAX}\, \ell + \alpha_{SLOT} + \alpha_M \quad \text{Eq. 2}$$

Once P_T (MIN) has been determined in the second equation for a specific link length (l), slot attenuation (α_{SLOT}) and margin (α_M). Figure 9 can then be used to find I_F.

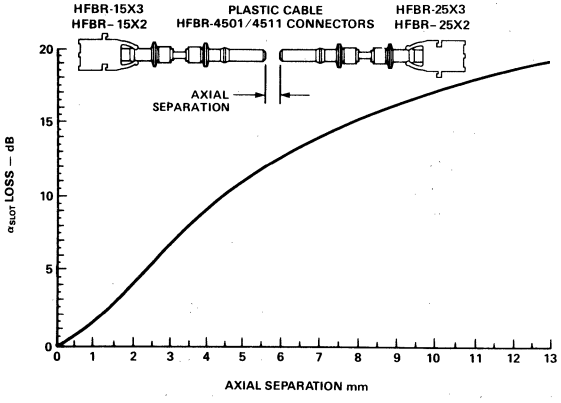


Figure 8. Typical Loss vs. Axial Separation.

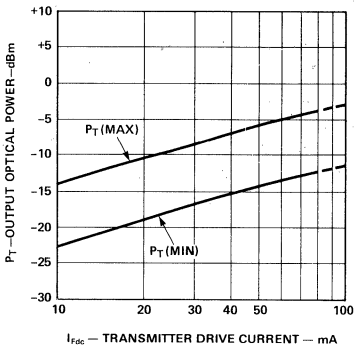


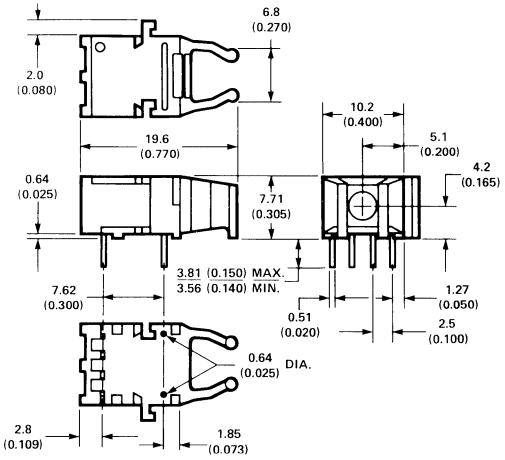
Figure 9. Typical HFBR-15X3/15X2 Optical Power vs. Transmitter I_F (0-70°C).

Versatile Link Mechanical Dimensions

All dimensions in mm (inches).
All dimensions ±0.25 mm unless otherwise specified.

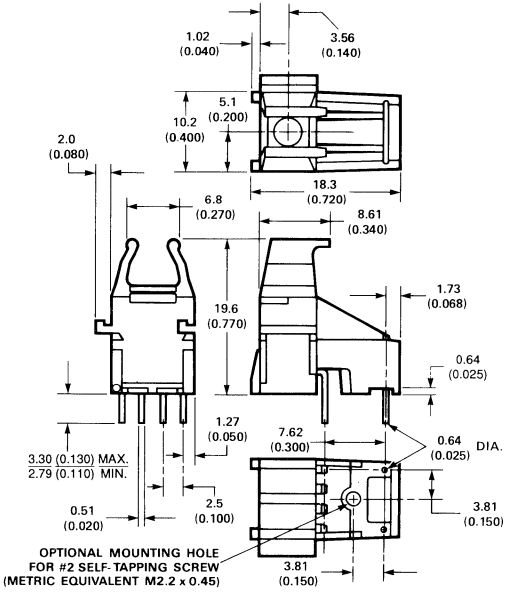
HORIZONTAL MODULES

HFBR-1521/1522/1524/1526 (GRAY), HFBR-1523 (BLACK)
HFBR-2521/2522/2523/2524/2526 (BLUE)

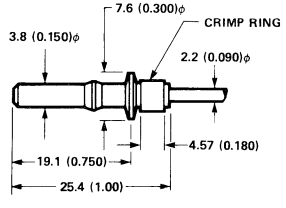


VERTICAL MODULES

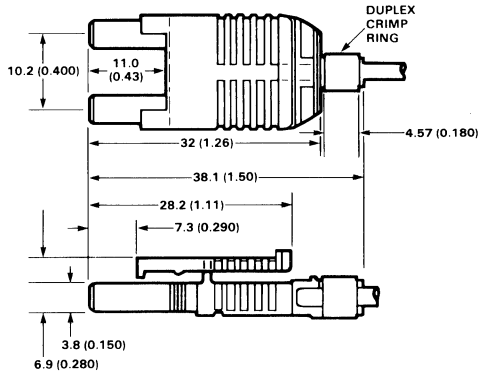
HFBR-1531/-1532/-1534/-1536 (GRAY), HFBR-1533 (BLACK)
HFBR-2531/-2532/-2533/-2534/-2536 (BLUE)



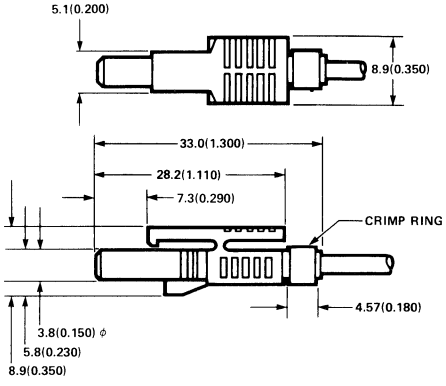
HFBR-4501 (GRAY)/-4511 (BLUE) SIMPLEX CONNECTOR



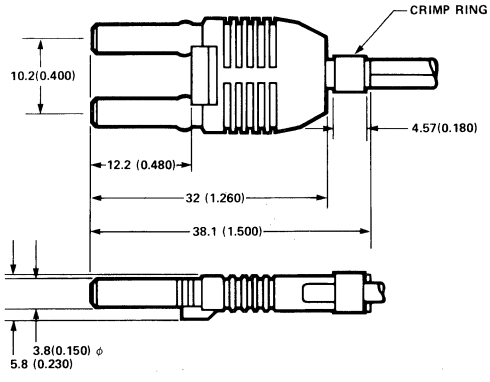
HFBR-4516 (GRAY) DUPLEX LATCHING CONNECTOR



HFBR-4503 (GRAY)/-4513 (BLUE) SIMPLEX LATCHING CONNECTOR

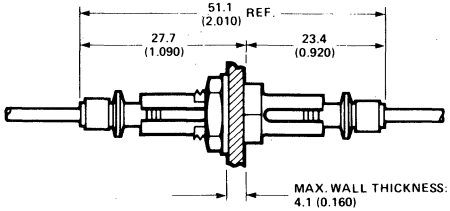


HFBR-4506 (PARCHMENT) DUPLEX CONNECTOR

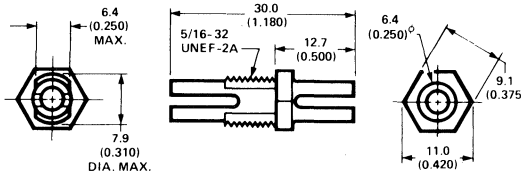


FIBER OPTICS

BULKHEAD FEEDTHROUGH WITH TWO HFBR-4501/-4511 CONNECTORS



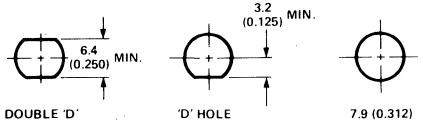
HFBR-4505 (GRAY)/-4515 (BLUE) ADAPTERS



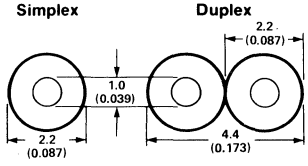
PANEL MOUNTING – BULKHEAD FEEDTHROUGH

THREE TYPES OF PANEL/BULKHEAD HOLES CAN BE USED.

DIMENSIONS IN mm (INCHES)
ALL DIMENSIONS ± 0.2 mm



FIBER OPTIC CABLE DIMENSIONS



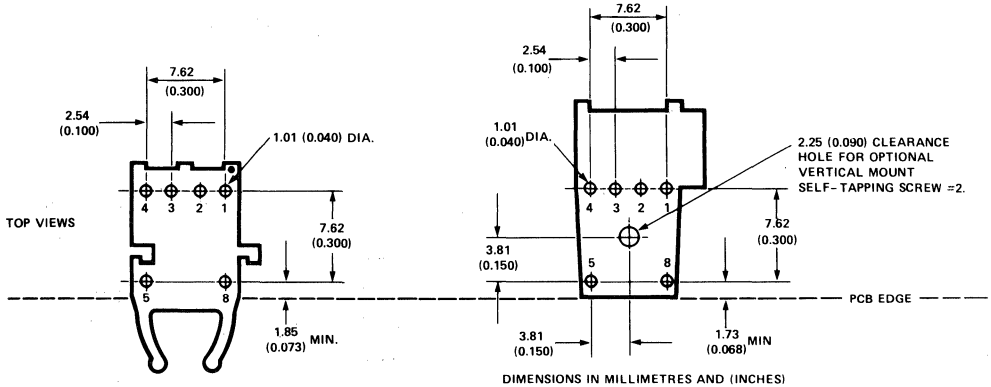
DIMENSIONS IN MILLIMETRES AND (INCHES)

Versatile Link Printed Circuit Board Layout Dimensions

TOP VIEWS

HORIZONTAL MODULE

VERTICAL MODULE



DIMENSIONS IN MILLIMETRES AND (INCHES)

ELECTRICAL PIN FUNCTIONS

PIN NO.	TRANSMITTERS HFBR-15XX	RECEIVERS EXCLUDING HFBR-25X3	RECEIVERS HFBR-25X3	TRANSMITTERS HFBR-15X6	RECEIVERS HFBR-25X6
1	ANODE	V_O	V_O	ANODE	SIGNAL GROUND
2	CATHODE	GROUND	GROUND	CATHODE	GROUND
3	OPEN	V_{CC}	OPEN	GROUND*	GROUND
4	OPEN	R_L	V_{CC}	GROUND*	V_{CC} (+5V)
5	PIN 8**	PIN 8**	PIN 8**	PIN 8**	PIN 8**
8	PIN 5**	PIN 5**	PIN 5**	PIN 5**	PIN 5**

*NO INTERNAL CONNECTION.
**PINS 5 AND 8 CONNECTED INTERNALLY TO EACH OTHER ONLY.

Interlocked (Stacked) Assemblies

Recommended stacking assembly of horizontal packages is easily accomplished by placing units upside down with pins facing upward. Initially engage the interlocking mechanism by sliding the L bracket body from above into the L slot body of the lower package. Lay the partially interlocked units on a flat surface and push down with a thin, rigid, rectangular edged object to bring all stacked units into uniform alignment. This technique prevents potential harm that could occur to fingers and hands of assemblers from the package pins. Refer to Figure 1 below that illustrates this assembly. Stacked horizontal packages can be disengaged should there be a need to do so. Repeated stacking and unstacking causes no damage to individual units.

Recommended stacking of vertical packages is to hold two vertical units, one in each hand, with the pins facing away from the assembler and the optical ports located in the bottom front of each unit. Engage completely, the L bracket unit from above into the lower L slot unit. Package to package alignment is easily insured by laying the full, flat, bottom side of the assembled units onto a flat surface pushing with a finger the two packages into complete, parallel alignment. The thin rectangular edged tool, used for horizontal package alignment, is not needed with the vertical packages. Stacked vertical packages can be disengaged should there be a need to do so. Repeated stacking and unstacking causes no damage to individual units.

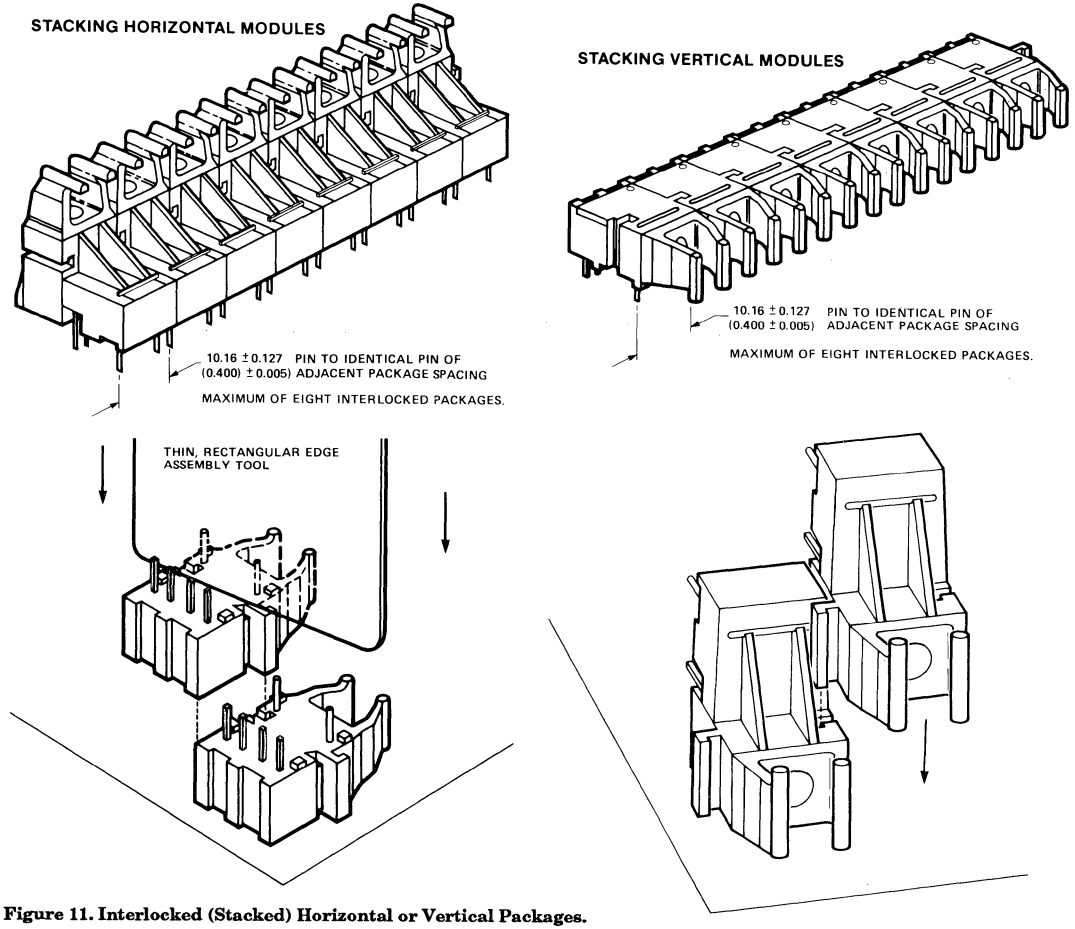


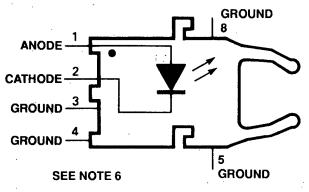
Figure 11. Interlocked (Stacked) Horizontal or Vertical Packages.

Versatile Link Transmitters and Receivers

50 MBd Link Transmitters

HFBR-1526/-1536 (50 MBd)

The HFBR-15X6 transmitters incorporate a 660 nanometre LED in a horizontal (HFBR-1526) or vertical (HFBR-1536) gray housing. The HFBR-15X6 transmitters are suitable for use with current peaking to decrease the response times, and can be used with HFBR-25X6 receivers in data links operating at signal rates from 2 to 50 megabaud over 1 mm diameter plastic optical fiber. Refer to Application Note 1045 for details of recommended interface circuits.



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Reference
Storage Temperature	T_S	-40	75	°C	
Operating Temperature	T_A	0	70	°C	
Lead Soldering Temperature			260	°C	Note 1
Cycle Time			3	s	
Forward Input Current Peak	I_{FPK}		500	mA	15 % duty cycle ≥ 1 KHz
Forward Input Current Average	I_{Favg}		80	mA	
Reverse Input Voltage	V_R		5	V	

CAUTION: The small junction sizes inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Electrical/Optical Characteristics 0 to 70°C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.[2]	Max.	Unit	Condition	Ref.
Peak Output Optical Power	P_T	-12.0	-9.6	-7.8	dBm	I_{Fdc} = 60 mA, 25°C	Note 3
		-13.6		-6.9	dBm	I_{Fdc} = 60 mA, 0-70°C	
Output Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-0.036		dB/°C	I_{Fdc} = 60 mA	
Peak Emission Wavelength	λ_{PK}	655	660	670	nm	25°C	
		645		680	nm	0-70°C	
Spectral Width	FWHM			30	nm	Full Width, Half Maximum	
Forward Voltage	V_F	1.45	1.67	2.02	V	I_{Fdc} = 60 mA	
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-1.37		mV/°C	I_{Fdc} = 60 mA	
Thermal Resistance, Junction to Case	θ_{jc}		140		°C/W		Note 4
Numerical Aperture	NA		0.5				
Reverse Input Breakdown Voltage	V_{BR}	5.0	11.0		V	I_{Fdc} = -10 μA, 25°C	
Diode Capacitance	C_O		100		pF	V_F = 0 f = 1 MHz	
Unpeaked Optical Rise Time, 10%-90%	t_r		45		ns	I_{Fdc} = 60 mA f = 100 kHz	Figure 1, Note 5
Unpeaked Optical Fall Time, 90%-10%	t_f		20		ns	I_{Fdc} = 60 mA f = 100 kHz	Figure 1, Note 5

Notes:
1. 1.6 mm below seating plane.
2. Typical data is at 25°C.
3. Optical power measured at the end of 0.5 metres of 1 mm diameter plastic optical fiber with large area detector.
4. Typical value measured from junction to PC board solder joint for horizontal mount package, HFBR-1526. θ_{jc} is approximately 30°C/W higher for vertical mount package, HFBR-1536.
5. Optical rise and fall times can be reduced with the appropriate driver circuit; refer to Application Note 1045.
6. Pins 5 and 8 are primarily for mounting and retaining purposes, but are electrically connected; pins 3 and 4 are electrically unconnected. It is recommended that pins 3, 4, 5, and 8 all be connected to ground to reduce coupling of electrical noise.
7. Refer to VERSATILE LINK HFBR-0501 Series Technical Data Sheet, for cable connector options.
8. The LED current peaking necessary for high frequency circuit design contributes to electromagnetic interference (EMI). Care must be taken in circuit board layout to minimize emissions for compliance with governmental EMI emissions regulations. Refer to Application Note 1045 for design guidelines.

WARNING: When viewed under some conditions, the optical port may expose the eye beyond the Maximum Permissible Exposure recommended in ANSI Z136.1, 1981. Under most viewing conditions there is no eye hazard.

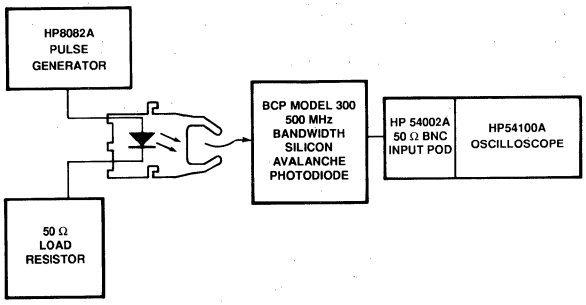


Figure 1. Test Circuit for Measuring Rise and Fall Times.

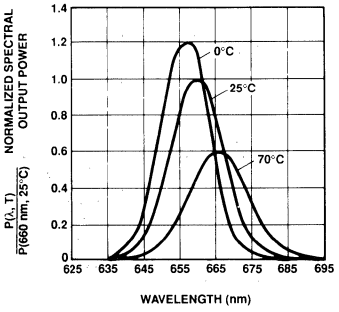


Figure 2. Typical Transmitter Spectra Normalized to the Peak at 25°C.

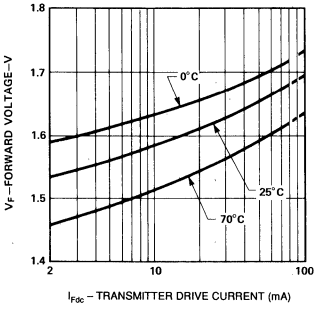


Figure 3. Typical Forward Voltage vs. Drive Current for HFBR-1526/ 1536 Transmitters.

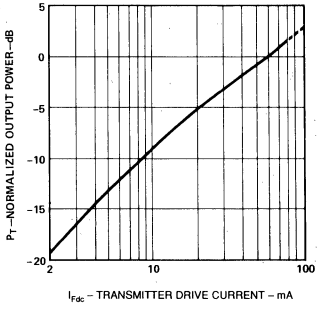
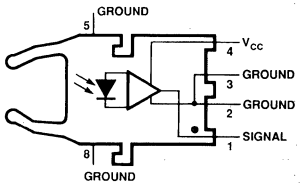


Figure 4. Normalized HFBR-1526/ 1536 Transmitter Typical Output Optical Power vs. Drive Current.

50 MBd Link Receivers

HFBR-2526/-2536 (50 MBd)

The HFBR-25X6 receivers contain a PIN photodiode and transimpedance pre-amplifier circuit in a horizontal (HFBR-2526) or vertical (HFBR-2536) blue housing, and are designed to interface to 1 mm diameter plastic optical fiber. The receivers convert a received optical signal to an analog output voltage. Follow-on circuitry can optimize link performance for a variety of distance and data rate requirements. Electrical bandwidth greater than 65 MHz allows design of high speed data links with plastic optical fiber. Refer to Application Note 1045 for details of recommended receiver circuits.



SEE NOTES 2, 4, 9

Absolute Maximum Ratings

Parameter	Symbol	Mininum	Maximum	Unit	Reference
Storage Temperature	T_S	-40	75	°C	
Operating Temperature	T_A	0	70	°C	
Lead Soldering Temp.			260	°C	Note 1
Cycle Time			3	s	
Signal Pin Voltage	V_O	-0.5	V_{CC}	V	
Supply Voltage	V_{CC}	-0.5	6.0	V	
Output Current	I_O		25	mA	

CAUTION: The small junction sizes inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Electrical/Optical Characteristics 0 to 70°C; Fiber core diameter ≤ 1.0 mm, fiber N.A. ≤ 0.5. 5.25 V < V_{CC} < 4.75 V; power supply must be filtered (see Figure 1, Note 2).

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit	Condition	Reference
AC Responsivity	R_P	1.7	3.9	6.5	mV/μW	660 nm	Note 4
RMS Output Noise	V_{NO}		0.46	0.69	mV_{RMS}		Note 5
Equivalent Optical Noise Input Power, RMS	$P_{N,RMS}$		-39 0.12	-36 0.25	dBm μW		Note 5
Peak Input Optical Power	P_R			-5.8 260	dBm μW	5 ns PWD	Note 6
Output Impedance	Z_O		30		Ω	50 MHz	Note 4
DC Output Voltage	V_O	0.8	1.8	2.6	V	P_R = 0 μW	
Supply Current	I_{CC}		9	15	mA		
Electrical Bandwidth	BW_E	65	125		MHz	-3 dB electrical	
Bandwidth * Rise Time			0.41		Hz *s		
Electrical Rise Time, 10-90%	t_r		3.3	6.3	ns	P_R = -10 dBm, peak	
Electrical Fall Time, 10-90%	t_f		3.3	6.3	ns	P_R = -10 dBm, peak	
Pulse Width Distortion	PWD		0.4	1.0	ns	P_R = -10 dBm, peak	Note 7
Overshoot			4		%	P_R = -10 dBm, peak	Note 8

Notes:

1. 1.6 mm below seating plane.
2. The signal output is an emitter follower, which does not reject noise in the power supply. Consequently, the power supply must be filtered as shown in Figure 1.
3. Typical data is at 25°C and V_{CC} = +5 Vdc.
4. Pin 1 should be ac coupled to a load ≥ 510 Ω, with load capacitance less than 5 pF.
5. Measured with a 3 pole Bessel filter with a 75 MHz, -3 dB bandwidth.
6. -5.8 dBm is the maximum input optical power for which pulse width distortion is guaranteed to be less than 5 ns. Pulse width distortion is typically less than 5 ns when the input optical power is less than -3.4 dBm.
7. 10 ns pulse width, 50% duty cycle, at the 50% amplitude point of the waveform.
8. Percent overshoot is defined at: $\frac{(V_{PK} - V_{100\%})}{V_{100\%}} \times 100\%$.
9. Pins 5 and 8 are primarily for mounting and retaining purposes, but are electrically connected. It is recommended that these both be connected to ground to reduce coupling of electrical noise.
10. Refer to VERSATILE LINK HFBR-0501 Series Technical Data Sheet for cable connector options.
11. If there is no input optical power to the receiver (no transmitted signal), electrical noise can result in false triggering of the receiver. In typical applications, data encoding and error detection prevent random triggering from being interpreted as valid data. Refer to Application Note 1045 for design guidelines.

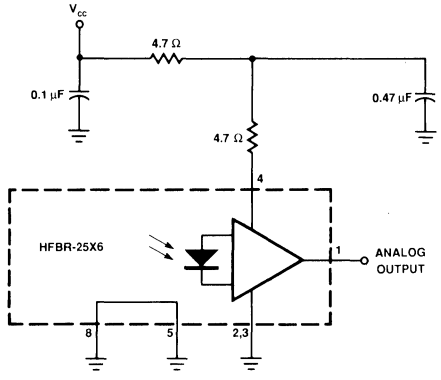


Figure 1. Recommended Power Supply Filter Circuit.

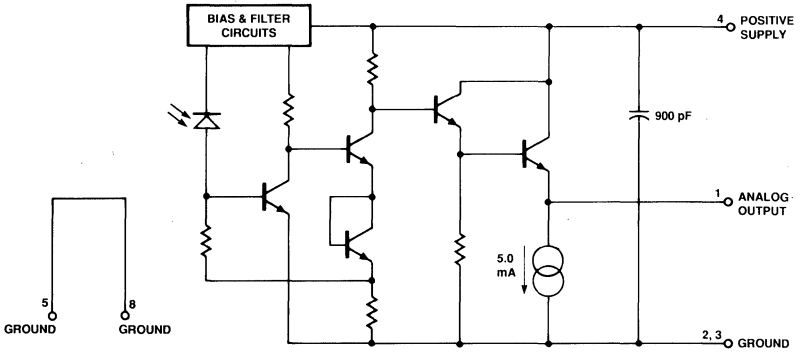


Figure 2. Simplified Receiver Schematic.

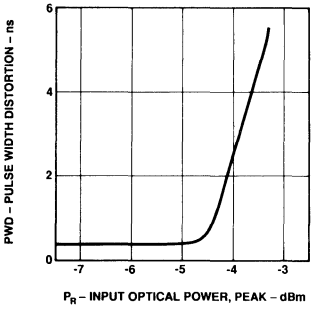


Figure 3. Typical Pulse Width Distortion vs. Peak Input Power.

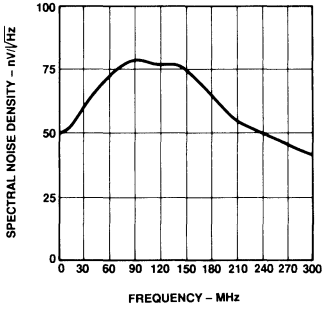


Figure 4. Typical Output Spectral Noise Density vs. Frequency.

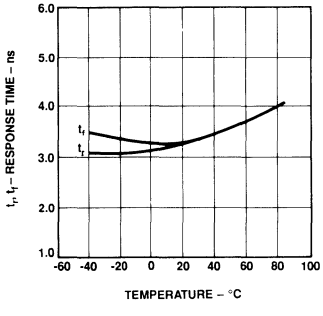


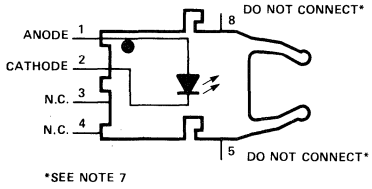
Figure 5. Typical Rise and Fall Times vs. Temperature.

5 MBd, 1 MBd, and 40 kBd Link Transmitters

HFBR-1521/1531 (5 MBd - High Performance)
HFBR-1522/1532 (1 MBd - High Performance)
HFBR-1523/1533 (40 kBd - Low Current/Extended Distance)
(HFBR-1524/1534 (1 MBd - Standard)

Versatile Link transmitters incorporate a 660 nanometre LED in a horizontal or vertical housing. The HFBR-15X3 transmitter housing is black. HFBR-15X1/2/4 standard housings are gray, but black versions are available. The transmitters can be easily interfaced to standard TTL or CMOS logic. The optical output power of the HFBR-152X/153X series is specified at the end of 0.5 m of cable. The mechanical and electrical pin spacing and connections are identical for both the horizontal and vertical packages.

HFBR-152X/153X Series Transmitters



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec.	
Peak Forward Input Current		$I_{F\,PK}$		1000	mA	Note 2
DC Forward Input Current		$I_{F\,DC}$		80	mA	
Reverse Input Voltage		V_R		5	V	

Electrical/Optical Characteristics 0°C to +70°C Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Transmitter Ouptut Optical Power	HFBR-15X1	P_T	-16.5		-7.6	dBm	I_{Fdc} = 60 mA, 0-70°C	Fig. 13 Notes 3, 4
			-14.3		-8.0	dBm	I_{Fdc} = 60 mA, 25°C	
	HFBR-15X2 and HFBR-15X3	P_T	-13.6		-4.5	dBm	I_{Fdc} = 60 mA, 0-70°C	
			-11.2		-5.1	dBm	I_{Fdc} = 60 mA, 25°C	
	HFBR-15X3	P_T	-35.5			dBm	I_{Fdc} = 2 mA, 0-70°C	
	HFBR-15X4	P_T	-17.8		-4.5	dBm	I_{Fdc} = 60 mA, 0-70°C	
			-15.5		-5.1	dBm	I_{Fdc} = 60 mA, 25°C	
Output Optical Power Temperature Coefficient		$\frac{\Delta P_T}{\Delta T}$		-0.85		%/°C		
Peak Emission Wavelength		λ_{PK}		660		nm		
Forward Voltage		V_F	1.45	1.67	2.02	V	I_{Fdc} = 60 mA	
Forward Voltage Temperature Coefficient		$\frac{\Delta V_F}{\Delta T}$		-1.37		mV/°C		Fig. 12
Effective Diameter		D_T		1		mm		
Numerical Aperture		N.A.		0.5				
Reverse Input Breakdown Voltage		V_{BR}	5.0	11.0		V	I_{FDC} = -10 μA, T_A = 25°C	
Diode Capacitance		C_O		86		pF	V_F = 0, f = 1 MHz	
Rise Time		t_r		80		ns	10% to 90%, I_F = 60 mA	Note 6
Fall Time		t_f		40		ns		

Notes:
1. 1.6 mm below seating plane.
2. 1 μs pulse, 20 μs period.
3. Measured at the end of 0.5 m Standard Fiber Optic Cable with large area detector.
4. Optical power. P (dBm) = 10 Log [P (μW)/1000 μW].
5. Typical data is at 25°C.
6. Rise and fall times are measured with a voltage pulse driving the transmitter and a series connected 50 ohm load. A wide bandwidth optical to electrical waveform analyzer (transducer), terminated to a 50 ohm input of a wide bandwidth oscilloscope, is used for this response time measurement.
7. Pins 5 and 8 of the transmitter are for mounting and retaining purposes only. Do not electrically connect pin 5 and/or pin 8.

WARNING: When viewed under some conditions, the optical port of the Transmitter may expose the eye beyond the Maximum Permissible Exposure recommended in ANSI Z-136-1, 1981. Under most viewing conditions there is no eye hazard.

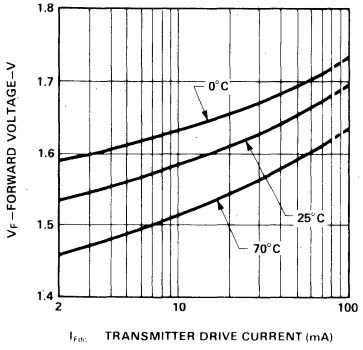


Figure 12. Typical Forward Voltage vs. Drive Current for HFBR-152X/153X Series Transmitters.

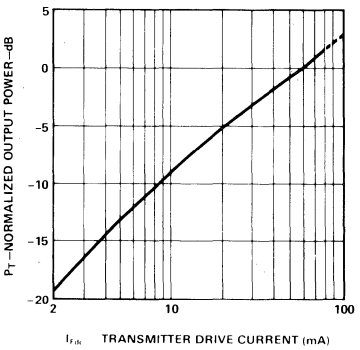


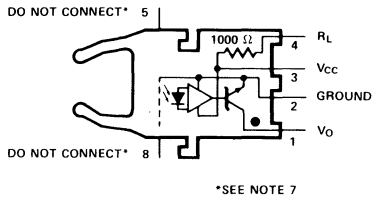
Figure 13. Normalized HFBR-152X/153X Series Transmitter Typical Output Optical Power vs. Drive Current.

5 MBd, 1 MBd, and 40 kBd Link Receivers

HFBR-2521/2531 (5 MBd - High Performance)
HFBR-2522/2532 (1 MBd - High Performance)
HFBR-2524/2534 (1 MBd - Standard)

The Versatile Link receivers feature a shielded, integrated photodetector and a wide bandwidth dc amplifier with high EMI immunity. A Schottky clamped open-collector output transistor allows interfacing to common logic families and enables "wired-OR" circuit designs. The open collector output is specified up to 18 V. An integrated 1000 ohm resistor internally connected to V_{CC} may be externally connected to provide a pull-up for ease of use with +5 V logic. Under pulsed LED current operation (I_F > 80 mA), the combination of a high optical power level and the optical falling edge of the LED transmitter will result in increased pulse width distortion of the receiver output signal. The standard receiver housings are blue; black versions are available.

HFBR-25X1/25X2/25X4 Receiver



Absolute Maximum Ratings

Parameter		Symbol	Mininum	Maximum	Unit	Reference
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec.	
Supply Voltage		V_{CC}	-0.5	7	V	Note 6
Output Collector Current		I_O		25	mA	
Output Collector Power Dissipation		P_{OD}		40	mW	
Output Voltage		V_O	-0.5	18	V	
Pullup Voltage		V_{RL}	-0.5	V_{CC}	V	

Electrical/Optical Characteristics

0°C to +70°C, 4.75 V ≤ V_{CC} ≤ 5.25 V Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Receiver Input Optical Power Level for Logic "0"	HFBR-2521 and HFBR-2531	$P_{R(L)}$	-21.6		-9.5	dBm	V_{OL} = 0.5 V I_{OL} = 8 mA	Notes 2, 3, 8
			-21.6		-8.7	dBm	25°C, V_{OL} = 0.5 V I_{OL} = 8 mA	
	HFBR-2522 and HFBR-2532	$P_{R(L)}$	-24			dBm	V_{OL} = 0.5 V I_{OL} = 8 mA	Notes 2, 3, 8, 9
			-24			dBm	25°C, V_{OL} = 0.5 V I_{OL} = 8 mA	
	HFBR-2524 and HFBR-2534	$P_{R(L)}$	-20			dBm	V_{OL} = 0.5 V I_{OL} = 8 mA	Notes 2, 3, 8, 9
			-20			dBm	25°C, V_{OL} = 0.5 V I_{OL} = 8 mA	
Input Optical Power Level for Logic "1"		$P_{R(H)}$			-43	dBm	V_{OH} = 5.25 V, I_{OH} ≤ 250 µA	Note 2
High Level Output Current		I_{OH}		5	250	µA	V_O = 18 V, P_R = 0	Note 4
Low Level Output Voltage		V_{OL}		0.4	0.5	V	I_{OL} = 8 mA, P_R = $P_{R(L)MIN}$	Note 4
High Level Supply Current		I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V, P_R = 0 µW	Note 4
Low Level Supply Current		I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V, P_R = 12.5 dBm	Note 4
Effective Diameter		D_R		1		mm		
Numerical Aperture		N.A.		0.5				
Internal Pull-Up Resistor		R_L	680	1000	1700	Ohms		

Notes:

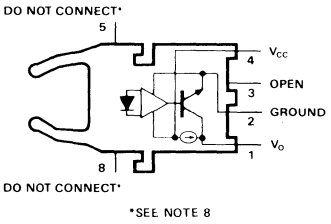
1. 1.6 mm below seating plan.
2. Optical flux, P (dBm) = 10 Log [P (µW)/1000 µW].
3. Measured at the end of Fiber Optic Cable with large area detector.
4. RL is open.
5. Typical data is at 25°C, V_{CC} = 5 V.
6. It is essential that a bypass capacitor 0.01 µF be connected from pin 2 to pin 3 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.
7. Pins 5 and 8 of both the transmitter and receiver are for mounting and retaining purposes only. Do not electrically connect pin 5 and/or pin 8.
8. Pulsed LED operation at I_F > 80 mA will cause increased link t_{PLH} propagation delay time. This extended t_{PLH} time contributes to increased pulse width distortion of the receiver output signal.
9. The HFBR-1522/1532/1524/1534 LED driver circuit of Figure 1b (Link Design Considerations) is required for operation of the HFBR-2522/2532/2524/2534.

High Sensitivity Receiver

HFBR-25X3

The blue plastic HFBR-25X3 Receiver module has a sensitivity of -39 dBm. It features an integrated photodetector and dc amplifier with high EMI immunity. The output is an open collector with a 150 μA internal current source pull-up and is compatible with TTL/ LSTTL and most CMOS logic families. For minimum rise time add an external pull-up resistor of at least 3.3 K ohms. V_{CC} must be greater than or equal to the supply voltage for the pull-up resistor.

HFBR-25X3 Receiver



Absolute Maximum Ratings

Parameter		Symbol	Mininum	Maximum	Unit	Reference
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec.	
Supply Voltage		V_{CC}	-0.5	7	V	Note 7
Output Collector Current (Average)		I_O	-1	5	mA	
Output Collector Power Dissipation		P_{OD}		25	mW	
Output Voltage		V_O	-0.5	V_{CC}	V	

Electrical/Optical Characteristics

0°C to +70°C, 4.5 V ≤ V_{CC} ≤ 5.5 V Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Receiver Input Optical Power Level for Logic "0"	HFBR-2523 and HFBR-2533	$P_{R(L)}$	-39		-13.7	dBm	$V_O = V_{OL}$, I_{OL} = 3.2 mA	Notes 2, 3, 4
			-39		-13.3	dBm	25°C, $V_O = V_{OL}$, I_{OL} = 3.2 mA	
Input Optical Power Level for Logic "1"		$P_{R(H)}$			-53	dBm	V_{OH} = 5.5 V, $I_{OH} \leq 40$ µA	Note 2
High Level Output Voltage		V_{OH}	2.4			V	I_{OH} = -40 µA, P_R = 0 µW	
Low Level Output Voltage		V_{OL}			0.4	V	I_{OL} = 3.2 mA, $P_R = P_{RL\ MIN}$	Note 6
High Level Supply Current		I_{CCH}		1.2	1.9	mA	V_{CC} = 5.5 V, P_R = 0 µW	
Low Level Supply Current		I_{CCL}		2.9	3.7	mA	V_{CC} = 5.5 V, $P_R \geq P_{RL}$(MIN)	Note 6
Effective Diameter		D_R		1		mm		
Numerical Aperture		N.A.		0.5				

Notes:

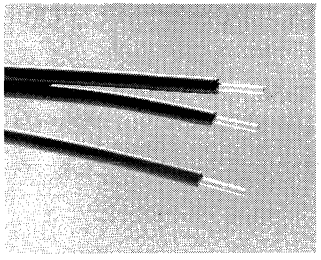
1. 1.6 mm below seating plan.
2. Optical flux, P (dBm) = 10 Log [P (µW)/1000 µW].
3. Measured at the end of Fiber Optic Cable with large area detector.
4. Because of the very high sensitivity of the HFBR-25X3, the digital output may switch in response to ambient light levels when a cable is not occupying the receiver optical port. The designer should take care to filter out signals from this source if they pose a hazard to the system.
5. Typical data is at 25°C, V_{CC} = 5 V.
6. Including current in 3.3 K pull-up resistor.
7. It is recommended that a bypass capacitor 0.01 µF to 0.1 µF ceramic be connected from pin 2 to pin 4 of the receiver.
8. Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect pin 5 and/or pin 8.

Plastic Cable

The HFBR-R/EXXYYY series of fiber optic cables are constructed of single step index fibers sheathed in a black polyethylene jacket. The duplex fiber consists of two Simplex fibers joined with a zipcord web. The individual channels of the duplex fiber are identified by a marking on one channel of the cable. Additionally, the polyethylene jackets of these cables complies with the UL VW-1 flame retardant specifications.

Along with the standard attenuation HFBR-RXXYYY series of plastic cable, an extra low attenuation version, HFBR-EXXYYY is available. The extra low attenuation cable is identical to the standard attenuation cable except that the attenuation is lower.

Both series of cables are available unconnectored or connectored options. Refer to the Ordering Guide for part number information.



Absolute Maximum Ratings

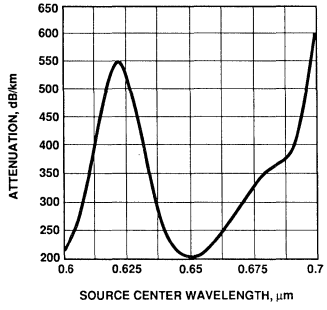
Parameter		Symbol	Minimum	Maximum	Unit	Reference
Storage Temperature		T_S	-55	+85	°C	
Installation Temperature		T_I	-20	+70	°C	Note 1
Short Term Tensile Force	Single Channel	F_T		50	N	Note 2
	Dual Channel	F_T		100	N	
Short Term Bend Radius		r	25		mm	Note 3, 4
Long Term Bend Radius		r	35		mm	
Long Term Tensile Load		F_T		1	N	
Flexing				1000	Cycles	Note 4

Mechanical/Optical Characteristics

Parameter		Symbol	Min.	Typ.[5]	Max.	Unit	Condition
Cable Attenuation	Standard Cable	α_O	0.15	0.22	0.27	dB/m	Source is HFBR-15XX (660 nm LED, 0.5 NA), = 50 metres. Note 7.
	Extra Low Loss		0.15	0.19	0.23		
Reference Attenuation	Standard Cable	α_R	0.12	0.19	0.24	dB/m	Source is 650 nm, 0.5 NA monochrometer, = 50 metres
	Extra Low Loss		0.12	0.16	0.19		
Numerical Aperture		N.A.	0.46	0.47	0.50		> 2 metres
Diameter, Core and Cladding		D_C	0.94	1.00	1.06	mm	
Diameter, Jacket		D_J	2.13	2.20	2.27	mm	Simplex Cable
Propagation Delay Constant		1/v		5.0		ns/m	Note 6
Mass per Unit Length/Channel		m/		5.3		g/m	Without connectors
Cable Leakage Current		I_L		12		nA	50 kV, = 0.3 metres
Refractive Index	Core	n		1.492			
	Cladding			1.417			

Notes:

1. Installation temperature is the range over which the cable can be bent and pulled without damage. Below -20°C the cable becomes brittle and should not be subjected to mechanical stress.
2. Less than 30 minutes.
3. Less than 1 hour, non-operating.
4. 90° bend on 25 mm radius mandrel. Bend radius is the radius of the mandrel around which the cable is bent.
5. Typical data are at 25°C.
6. Propagation delay constant is the reciprocal of the group velocity for propagation of optical power. Group velocity is v = c/n, where c is the velocity of light in free space (3 x 10^8 m/s) and n is the effective core index of refraction.
7. Note that α_o rises at the rate of about 0.0067 dB/m/°C where the thermal rise refers to LED temperature changes above 25°C. Please refer to Figure 3 which shows the typical plastic optical fiber attenuation versus wavelength at 25°C and Figure 2 of the 50 MBd transmitter section of the catalog which shows typical transmitter spectral normalized to the peak at 25°C.



Typical Plastic Optical Fiber Attenuation Versus Wavelength (25°C).

Versatile Link Fiber Optic Connectors

Connectors, Feedthrough/ Splice, Polishing Tools

Versatile Link transmitters and receivers are compatible with four connector styles: simplex, simplex latching, duplex, and duplex latching. All connectors provide a snap-action when mated to Versatile Link components. Simplex connectors are color coded to match with transmitter and receiver color coding. Duplex connectors are keyed so that proper orientation is ensured. When removing a connector from a module, pull at the connector body. Do not pull on the cable alone. The same, quick and simple connectoring technique is used with all connectors and cable. This technique is described on page N. Note that simplex and duplex crimp rings are different sizes.

Simplex Connector Styles

HFBR-4501/4511-Simplex

The simplex connector provides a quick and stable connection for applications that require a component to provide retention force of 8 newtons (1.8 lb). These connectors are available in colors of gray (HFBR-4501) or blue (HFBR-4511).

HFBR-4503/4513-Simplex Latching

The simplex latching connector is designed for rugged applications requiring greater retention force, 80 N (18 lbs), than that provided by a simplex connector. When inserting the simplex latching connector into a module, the connector latch mechanism should be aligned with the top surface of the horizontal module, or with the tall vertical side of the vertical module. Misalignment of an inserted latching connector into either module housing will not result in a positive latch. The connector is released by depressing the rear section of the connector lever, and then pulling the connector assembly away from the module housing.

If the cable/connector will be used at elevated operating temperatures or experience frequent and wide temperature cycling effects, the cable/ connector attachment can be strengthened by applying an RTV adhesive within the connector. A recommended adhesive is GE Company RTV-128 or Dow Corning 3154. In most applications use of an RTV is unnecessary. The simplex latching connector is available in gray (HFBR-4503) or blue (HFBR-4513).

Duplex Connector Styles

HFBR-4506-Duplex

Duplex connectors provide convenient duplex cable termination and are keyed to prevent incorrect connection. The duplex connector is compatible with dual combinations of identical Versatile Link components (e.g., two horizontal transmitters, two vertical receivers, a horizontal transmitter and a horizontal receiver, etc.). A duplex connector cannot connect to two different packages simultaneously. The duplex connector is an off-white color.

HFBR-4516-Duplex Latching

The duplex latching connector is designed for rugged applications requiring greater retention force than the standard duplex connector. When inserting the duplex latching connector into a module, the connector latch mechanism should be aligned with the top surface of the dual combinations of identical versatile link components. The combinations are described in the previous section on duplex connectors. The duplex latching connector is a gray color.

Feedthrough/Splice

HFBR-4505/4515-Adapter

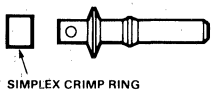
The HFBR-4505/4515 adapter mates two simplex connectors for panel/bulkhead feedthrough of plastic fiber cable. Maximum panel thickness is 4.1 mm (0.16 inch). This adapter can serve as a cable in-line splice using two simplex connectors. The colors of the adapters are gray (HFBR-4505) and blue (HFBR-4515). The adapter is not compatible with the duplex or simplex latching connectors.

Absolute Maximum Ratings

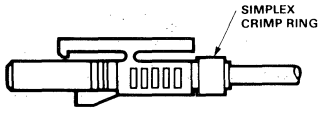
Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	+75	°C	
Operating Temperature	T_A	0	+70	°C	
Nut Torque HFBR-4505/4515	T_N		0.7	N-m	1
			100	OzF-in	

Note:
1. Recommended nut torque is 0.57 N-m (80 OzF-in).

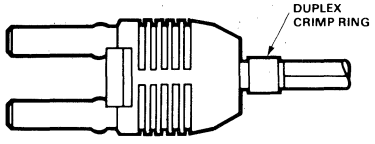
HFBR-4501 (Gray)/4511 (Blue) Simplex Connector



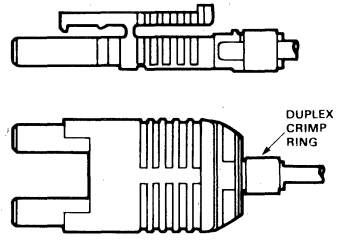
HFBR-4503 (Gray)/4513 (Blue) Simplex Latching Connector



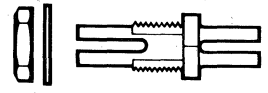
HFBR-4506 (Parchment) Duplex Connector



HFBR-4516 (Gray) Duplex Latching Connector



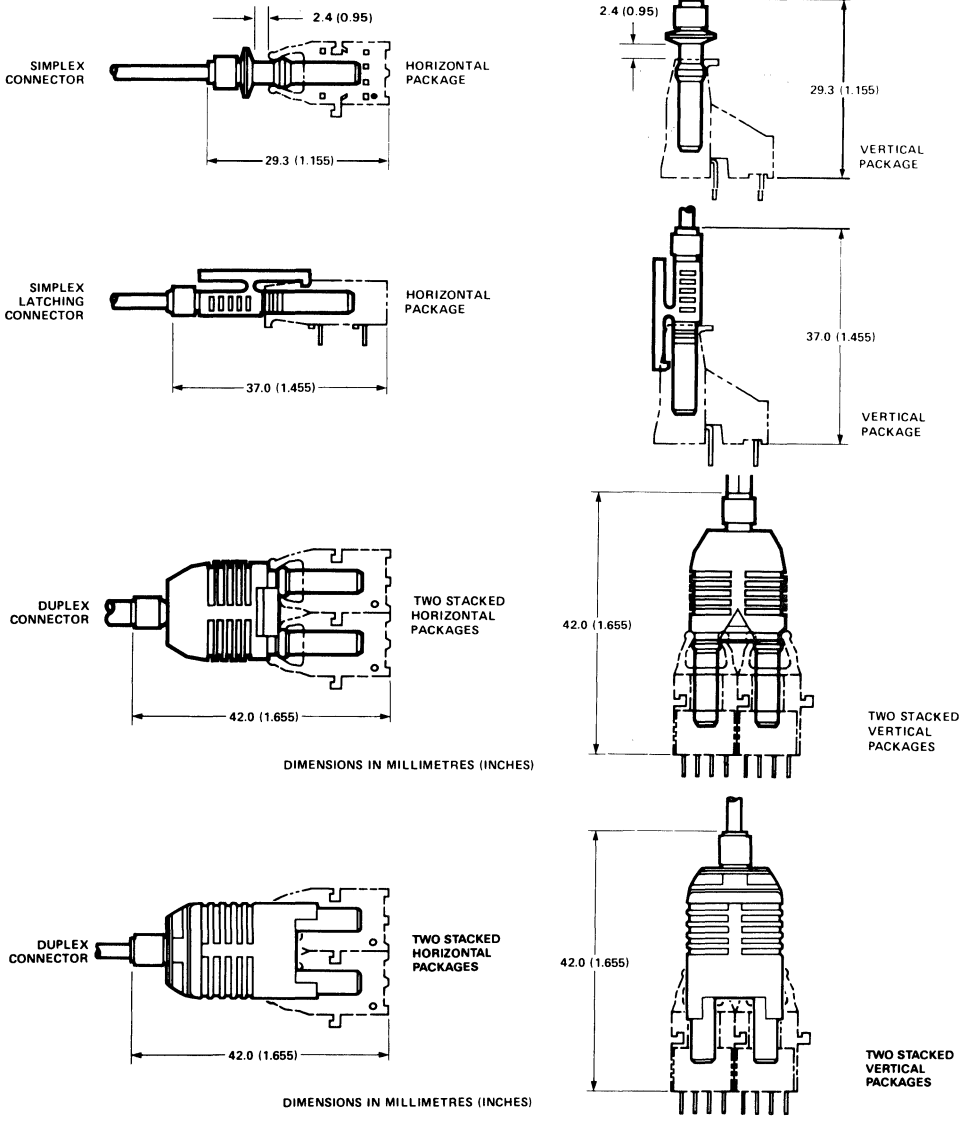
HFBR-4505 (Gray)/4515 (Blue) Adapter



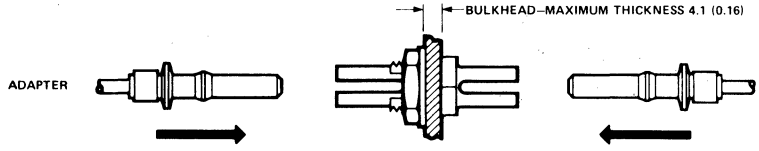
(USE WITH SIMPLEX CONNECTORS ONLY)

Connector Applications

ATTACHMENT TO HEWLETT-PACKARD HFBR-152X/153X/252X/253X VERSATILE LINK FIBER OPTIC COMPONENTS



BULKHEAD FEEDTHROUGH OR PANEL MOUNTING FOR HFBR-4501/4511 SIMPLEX CONNECTORS



Connector Mechanical/Optical Characteristics

25°C Unless Otherwise Specified

Parameter	Part Number		Sym.	Min.	Typ.	Max.	Units	Ref.
Retention Force Connector to HFBR-152X 153X/252X/253X Modules	Simplex	HFBR-4501/4511	F_{R-C}	7	8		N	Note 4
	Simplex Latching	HFBR-4503/4513		47	80			
	Duplex	HFBR-4506		7	12			
	Duplex Latching	HFBR-4516		50	80			
Tensile Force Connector to Cable	Simplex	HFBR-4501/4511	F_T	8.5	22		N	Notes 3, 4
	Simplex Latching	HFBR-4503/4513		8.5	22			
	Duplex	HFBR-4506		14	35			
	Duplex Latching	HFBR-4516		14	35			
Adapter Connector to Connector Loss	HFBR-4505/4515 with HFBR-4501/4511		α_{CC}	0.7	1.5	2.8	dB	Notes 1, 5
Retention Force Connector to Adapter	HFBR-4505/4515 with HFBR-4501/4511		F_{R-B}	7	8		N	Note 4
Insertion Force Connector to HFBR-152X/ 153X/252X/253X Modules	Simplex	HFBR-4501/4511	F_I		8	12	N	Notes 2, 4
	Simplex Latching	HFBR-4503/4513			16	35		
	Duplex	HFBR-4506			13	46		
	Duplex Latching	HFBR-4516			22	51		

Notes:

1. Factory polish or field polish per recommended procedure.
2. No perceivable reduction in insertion force was observed after 2000 insertions. Destructive insertion force was typically at 178 N (40 lbs).
3. For applications where frequent temperature cycling over temperature extremes is expected please contact Hewlett-Packard for alternate connectoring techniques.
4. All mechanical forces were measured after units were stored at 70°C for 168 hours and returned to 25°C for one hour.
5. Minimum and maximum limits of α_{CC} for 0°C to 70°C temperature range. Typical value of α_{CC} is at 25°C.

Step-by-Step Plastic Cable Connectoring Instructions

The following step-by-step guide describes how to terminate cable. It is ideal for both field and factory installation. If a high volume connectoring technique is required please contact your Hewlett-Packard sales engineer for the recommended procedure and equipment.

Connectoring the cable is accomplished with the Hewlett-Packard HFBR-4593 Polishing Kit consisting of a Polishing Fixture, 600 grit abrasive paper and 3 μm pink lapping film (3M Company, OC3-14). No adhesive material is needed to secure the cable in the connector, and the connector can be used immediately after polishing. Improved connector to cable attachment can be achieved with the use of an RTV (GE Company, RTV-128 or Dow Corning 3154-RTV) adhesive for frequent, extreme temperature cycling environments or for elevated temperature operation.

Connectors may be easily installed on the cable ends with readily available tools. Materials needed for the terminating procedure are:

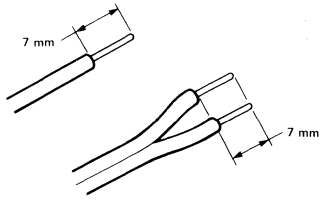
1. Hewlett-Packard Plastic Fiber Optic Cable
2. HFBR-4593 Polishing Kit
3. HFBR-4501/4503 Gray Simplex/Simplex Latching Connector and Silver Color Crimp Ring
4. HFBR-4511/4513 Blue Simplex/Simplex Latching Connector and Silver Color Crimp Ring
5. HFBR-4506 Parchment Duplex Connector and Duplex Crimp Ring
6. HFBR-4516 Gray Latching Duplex Connector and Duplex Crimp Ring
7. Industrial Razor Blade or Wire Cutters
8. 16 Gauge Latching Wire Strippers
9. Crimp Tool, HFBR-4597

Step 1

The zip cord structure of the duplex cable permits easy separation of the channels. The channels should be separated approximately 50 mm (2.0 in.) back from the ends to permit connectoring and polishing.

After cutting the cable to the desired length, strip off approximately 7 mm (0.3 in.) of the outer jacket with the 16 gauge wire strippers. Excess webbing on duplex cable may have to be trimmed to allow the simplex or simplex latching connector to slide over the cable.

When using the duplex connector and duplex cable, the separated duplex cable must be stripped to equal lengths on each cable. This allows easy and proper seating of the cable into the duplex connector.

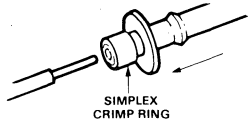


Step 2

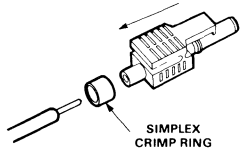
Place the crimp ring and connector over the end of the cable; the fiber should protrude about 3 mm (0.12 in.) through the end of the connector. Carefully position the ring so that it is entirely on the connector with the rim of the crimp ring flush with the connector, leaving a small space between the crimp ring and the flange. Then crimp the ring in place with the crimping tool. One crimp tool is used for all connector crimping requirements.

Note: Place the gray connector on the cable end to be connected to the transmitter and the blue connector on the cable end to be connected to the receiver to maintain the color coding (both connectors are the same mechanically). For duplex connector and duplex cable application, align the color coded side of the cable with the appropriate ferrule of the duplex connector in order to match connections to the respective optical ports. The simplex connector crimp ring cannot be used with the duplex connector. The duplex connector crimp ring cannot be used with the simplex or simplex latching connectors. The simplex crimp has a dull lustre; the duplex ring is shiny and has a thinner wall.

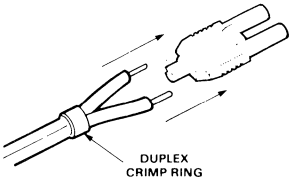
Simplex



Simplex Latching



Duplex/Duplex Latching

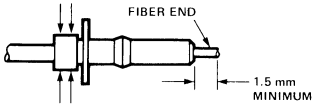


Step 3
Any excess fiber protruding from the connector end may be cut off; however, the trimmed fiber should extend at least 5 mm (0.06 in.) from the connector end.

Insert the connector fully into the polishing fixture with the trimmed fiber protruding from the bottom of the fixture. This plastic polishing fixture can be used to polish two simplex connectors or two simplex latching connectors simultaneously, or one duplex connector.

Note: The four dots on the bottom of the polishing fixture are wear indicators. Replace the polishing fixture when any dot is no longer visible. Typically, the polishing fixture can be used 10 times: 10 duplex connectors or 20 simplex connectors, two at a time.

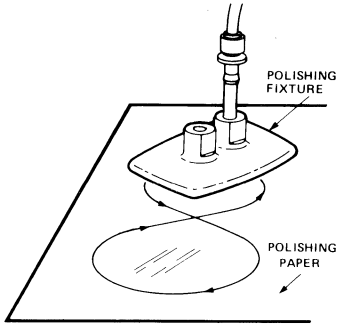
Place the 600 grit abrasive paper on a flat smooth surface. Pressing down on the connector, polish the fiber and the connector using a fixture eight pattern of strokes until the connector is flush with the bottom of the polishing fixture. Wipe the connector and fixture with a clean cloth or tissue.



Step 4
Place the flush connector and polishing fixture on the dull side of the 3 micron pink lapping film and continue to polish the fiber and connector for approximately 25 strokes. The fiber end should be flat, smooth and clean.

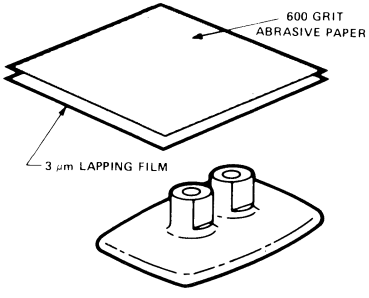
The cable is now ready for use.

Note: Use of the pink lapping film fine polishing step results in approximately 2 dB improvement in coupling performance of either a transmitter-receiver clink or a bulk-head/splice over 600 grit polish alone. This fine polish is comparable Hewlett-Packard factory polish. The fine polishing step may be omitted where an extra 23 dB of optical power is not essential, as with short link lengths. Proper polishing of the tip of the fiber/connector face results in a tip diameter between 2.8 mm (0.110 in.) minimum and 3.2 mm (0.125 in.) maximum.



For simultaneous multiple connector polishing techniques please contact Hewlett-Packard.

HFBR-4593 Polishing Kit



(USED WITH ALL CONNECTOR TYPES)

Ordering Guide

Transmitters (Tx)/Receivers (Rx)

Versatile Link	Unit	Horizontal Modules	Vertical Modules
50 MBd High Performance	Tx	HFBR-1526	HFBR-1536
5 MBd High Performance	Tx	HFBR-1521	HFBR-1531
1 MBd High Performance	Tx	HFBR-1522	HFBR-1532
40 kBd Low Current/Extended Distance	Tx	HFBR-1523	HFBR-1533
1 MBd Standard	Tx	HFBR-1524	HFBR-1534
50 MBd High Performance	Rx	HFBR-2526	HFBR-2536
5 MBd High Performance	Rx	HFBR-2521	HFBR-2531
1 MBd High Performance	Rx	HFBR-2522	HFBR-2532
40 kBd Low Current/Extended Distance	Rx	HFBR-2523	HFBR-2533
1 MBd Standard	Rx	HFBR-2524	HFBR-2534

Connectors

HFBR-4501	Gray Simplex Connector/Crimp Ring
HFBR-4511	Blue Simplex Connector/Crimp Ring
HFBR-4503	Gray Simplex Latching Connector with Crimp Ring
HFBR-4513	Blue Simplex Latching Connector with Crimp Ring
HFBR-4506	Parchment Duplex Connector with Crimp Ring
HFBR-4516	Gray Duplex Latching Connector with Crimp Ring
HFBR-4505	Gray Adapter
HFBR-4515	Blue Adapter

Evaluation Kit, HFBR-0501	**Contents**
HFBR-1524	Transmitter
HFBR-2524	Receiver
HFBR-4501	Gray Simplex Connector with Crimp Ring
HFBR-4506	Duplex Connector with Crimp Ring
—	5 metres of Connectored Simplex Cable with Blue Simplex and Gray Simplex Latching Connectors
HFBR-4513	Blue Simplex Latching Connector with Crimp Ring
HFBR-4505	Gray Adapter
—	Polishing Tool and 600 grit paper
HFBR-0501	Data Sheet and Brochure

Accessories

HFBR-4522	500 Port Plugs
HFBR-4525	1000 Simplex Crimp Rings
HFBR-4526	500 Duplex Crimp Rings
HFBR-4593	Polishing Kit (one polishing tool, two pieces 600 grit abrasive paper, and two pieces 3-μm lapping film).
HFBR-4597	Crimping Tool

A Note About Ordering Plastic Cable

Four steps are required to determine the proper part number for a desired cable.

Step 1
Select Standard or Extra Low Loss Attenuation Cable. As explained on page N, two levels of attenuation are available: Standard or Extra Low.

Step 2
Select the connector style. Connector styles are described on page N.

Step 3
Select Simplex or Duplex.

Step 4
Determine the cable length.

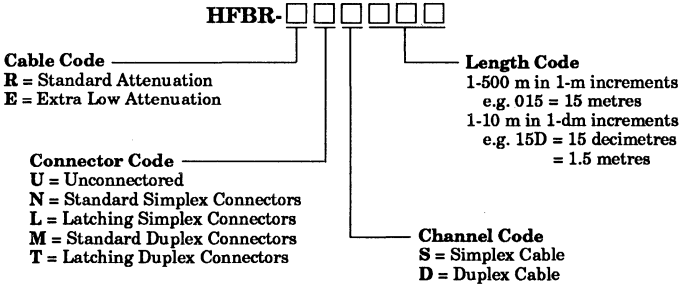
To determine the appropriate part number, select the letter corresponding to your selection and fill in the following:

For Example:
HFBR-RUD500 is a Standard Attenuation, Unconnectored, Duplex, 500 meter cable.
HFBR-ELS001 is an Extra Low Attenuation, Latching Simplex Connectored, Simplex, 1 meter cable.
HFBR-RMD010 is a Standard Attenuation, Standard Duplex Connectored, Duplex, 10 meter cable.
HFBR-RND100 is a Standard Attenuation Standard Simplex Connectored, Duplex, 100 meter cable.

Cable Length Tolerances:
The plastic cable length tolerances are: +10%/-0%.

Note: 0.1 metre Standard Attenuation Simplex lengths are available: 0.5 metre Standard Attenuation Simplex and Duplex lengths are also available. The lengths are ordered as HFBR-xxx1DM or HFBR-xxx5DM. Cables of 1 to 10 meter lengths in 1 decimeter increments are also available. The cable is ordered as HFBR-xxxyyD where "yy" is the length of the cable. For example, a 1.5 meter Standard Attenuation, Standard Simplex Connectored, Simplex cable would be ordered as HFBR-RNS15D.

Attention: Pre-connectored simplex cables have oppositely colored (GRAY vs. BLUE) connectors are the opposite ends of the same fiber; although oppositely colored, the connectors are mechanically identical. For duplex cables with simplex connectors, the same rule applies to each fiber; also, the side-by-side fibers at each end of the cable have oppositely colored connectors. For duplex cables with duplex connectors similar rules apply so the connectors at opposite ends are oppositely keyed relative to the marked fiber in a duplex cable.



HEWLETT PACKARD

SERCOS Fiber Optic Transmitters and Receiver

Technical Data

HFBR-0600 Series

Features

- **Fully Compliant to SERCOS Optical Specifications**
- **Optimized for 1 mm Plastic Optical Fiber**
- **Compatible with SMA Connectors**
- **Auto-Insertable and Wave Solderable**
- **Data Transmission at Symbol Rates from DC to over 2 MBd for Distances from 0 to over 20 Metres.**

Applications

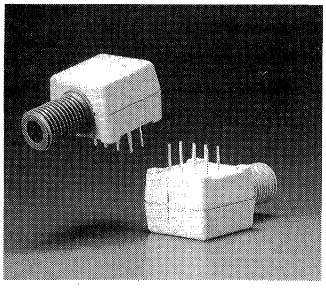
- **Industrial Control Data Links**
- **Reduction of Lightning and Voltage Transient Susceptibility**
- **Tempest-Secure Data Processing Equipment**
- **Isolation in Test and Measurement Instruments**
- **Robotics Communication**

SERCOS

SERCOS is a SErial Realtime COmmunication System, a standard digital interface for communication between controls and drives for numerically controlled machines. The SERCOS interface specification was written by a joint working group of the VDW (German Machine Tool Builders Association) and ZVEI (German Electrical and Electronic Manufacturer's Association) to allow data exchange between NC controls and drives via fiber optic rings, with isolation and noise immunity. The HFBR-0600 family of fiber optic transmitters and receivers comply to the SERCOS specifications for transmitter and receiver optical characteristics and connector style (SMA).

Description

The HFBR-0600 components are capable of operation at symbol rates from DC to over 2 MBd and distances from 0 to over 20 metres. The HFBR-1602 and HFBR-1604 transmitters contain a 655-nm AlGaAs emitter capable of efficiently launching optical power into 1000 µm plastic optical fiber. The optical output is specified at the end of 0.5 m of plastic optical fiber.

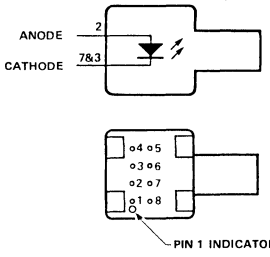


The HFBR-1604 is a selected version of the HFBR-1602, with power specified to meet the SERCOS high attenuation specifications.

The HFBR-2602 receiver incorporates an integrated photo IC containing a photodetector and dc amplifier driving an open-collector Schottky output transistor. The HFBR-2602 is designed for direct interfacing to popular logic families. The absence of an internal pull-up resistor allows the open-collector output to be used with logic families such as CMOS requiring voltage excursions higher than V_{CC}. The HFBR-2602 has a dynamic range of 15 dB.

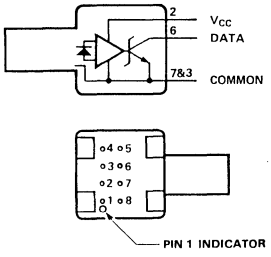
CAUTION: The small junction sizes inherent to the design of this component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

HFBR-160X Transmitters



Pin	Function
1*	N.C.
2	ANODE
3	CATHODE
4*	N.C.
5*	N.C.
6	N.C.
7**	CATHODE
8*	N.C

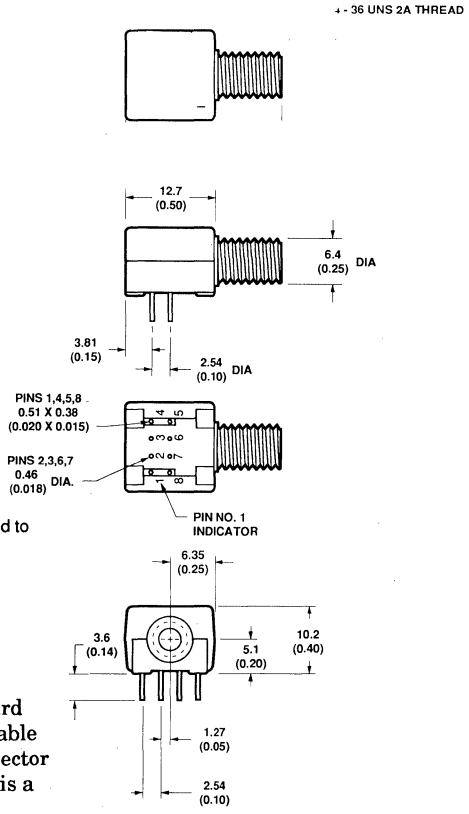
HFBR-2602 Receiver



Pin	Function
1*	N.C.
2	V_{CC} (5 V)
3	COMMON
4*	N.C.
5*	N.C.
6	DATA
7	COMMON
8*	N.C.

*Pins 1, 4, 5, and 8 are isolated from the internal circuitry, but electrically connected to one another.
**Transmitter Pin 7 may be left unconnected if necessary.

HFBR-0600 SMA Series Mechanical Dimensions



In the receiver, both the open-collector "Data" output Pin 6 and V_{CC} Pin 2 are referenced to "Common" Pin 3 and 7. It is essential that a bypass capacitor (0.1 µF ceramic) be connected from Pin 2 (V_{CC}) to Pin 3 (circuit common) of the receiver.

SMA is an industry standard fiber optic connector, available from many fiber optic connector suppliers. HFBR-RWS002 is a two meter SMA, 1000 µm plastic fiber optic cable for evaluation purposes. HFBR-4401 is a kit consisting of 100 nuts and 100 washers for panel mounting the HFBR-0600 components.

HFBR-1602/1604 Transmitters

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Reference
Storage Temperature		T_S	-55	85	°C	
Operating Temperature		T_A	-40	85	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	s	Note 1
Forward Input Current Peak		I_{FPK}		120	mA	
Forward Input Current Average		I_{Favg}		60	mA	
Reverse Input Voltage		V_{BR}		-5	V	

Electrical/Optical Characteristics 0 to 55°C, unless otherwise stated

Parameter	Symbol	Min.	Typ.[2]	Max.	Unit	Condition	Reference
Forward Voltage	V_F	1.5	1.9	2.2	V	I_F = 35 mA	
Forward Voltage Temp. Coefficient	$\Delta V_F/\Delta T$		-1.2		mV/°C	I_F = 35 mA	
Reverse Input Voltage	V_{BR}	-5.0	-18		V	I_R = 100 µA	
Peak Emission Wavelength	λ_P	640	655	675	nm		
Full Width Half Maximum	FWHM		20	30	nm	25°C	
Diode Capacitance	C_T		30		pF	V_F = 0 f = 1 MHz	
Optical Power Temp. Coefficient	$\Delta P_T/\Delta T$		-0.01		dBm/°C	I_F = 35 mA	
Thermal Resistance	θ_{JA}		330		°C/W		Notes 3, 4
Peak Optical Output Power of HFBR-1602	P_{T1602}	-10.5		-5.5	dBm	I_F = 35 mA	Notes 5, 6, 11
Peak Optical Output Power of HFBR-1604	P_{T1604}	-7.5 -10.5		-3.5 -5.5	dBm dBm	I_F = 60 mA I_F = 35 mA	Notes 5, 6, 11
Rise Time (10% to 90%)	t_r		57 50		ns ns	I_F = 60 mA I_F = 35 mA	
Fall Time (90% to 10%)	t_f		40 27		ns ns	I_F = 60 mA I_F = 35 mA	

HFBR-2602 Receiver

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Reference
Storage Temperature		T_S	-55	85	°C	
Operating Temperature		T_A	-40	85	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	s	Note 1
Supply Voltage		V_{CC}	-0.5	7.0	V	
Output Current		I_O		25	mA	
Output Voltage		V_O	-0.5	18.0	V	
Output Collector Power Dissipation		$P_{O\,AVG}$		40	mW	
Fan Out (TTL)		N		5		Note 8

Electrical/Optical Characteristics 0 to 55°C;
Fiber core diameter ≤ 1.0 mm, fiber N.A. ≤ 0.5, 4.75 V ≤ V_{CC} ≤ 5.25 V

Parameter	Symbol	Min.	Typ.[2]	Max.	Unit	Condition	Reference
High Level Output Current	I_{OH}		5	250	µA	V_{OH} = 18 V P_R < -31.2 dBm	
Low Level Output Voltage	V_{OL}		0.4	0.5	V	I_{OL} = 8 mA P_R > -20.0 dBm	
High Level Supply Current	I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V P_R < -31.2 dBm	
Low Level Supply Current	I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V P_R > -20.0 dBm	

Dynamic Characteristics 0 to 55°C unless otherwise specified; 4.75 V ≤ V_{CC} ≤ 5.25 V; BER ≤ 10^{-9}

Parameter	Symbol	Min.	Typ.[2]	Max.	Unit	Condition	Reference
Peak Input Power Level Logic HIGH	P_{RH}			-31.2	dBm	λ_P = 655 nm	Note 7
Peak Input Power Level Logic LOW	P_{RL}	-20.0		-5.0	dBm	I_{OL} = 8 mA	Note 7
Propagation Delay LOW to HIGH	t_{PLH}		60		ns	P_R = -20 dBm 2 MBd	Note 8, 9
Propagation Delay HIGH to LOW	t_{PHL}		110		ns	P_R = -20 dBm 2 MBd	Note 8, 9
Pulse Width Distortion, $t_{PLH} - t_{PHL}$	PWD		50 -50		ns ns	P_R = -5 dBm P_R = -20 dBm	Note 10 Figure 6

Notes:

1. 2.0 mm from where leads enter case.
2. Typical data at T_A = 25°C.
3. Thermal resistance is measured with the transmitter coupled to a connector assembly and fiber, and mounted on a printed circuit board.
4. Transmitter pins 3 and 7 are welded to the cathode header connection to minimize the thermal resistance from junction to ambient. To further reduce the thermal resistance, the cathode trace should be made as large as is consistent with good RF circuit design. Pin 7 may be left unconnected if necessary for board compatibility HFBR-14XX transmitters.
5. P_T is measured with a large area detector at the end of 0.5 metre of plastic optical fiber with 1 mm diameter and numerical aperture of 0.5.
6. When changing μW to dBm, the optical power is referenced to 1 mW (1000 μW). Optical Power P(dBm) = 10 log [P (μW)/1000 μW].
7. Measured at the end of 1mm plastic fiber optic cable with a large area detector.
8. 8 mA load (5 x 1.6 mA), R_L = 560 ohms.
9. Propagation delay through the system is the result of several sequentially occurring phenomena. Consequently it is a combination of data-rate-limiting effects and of transmission-time effects. Because of this, the data-rate limit of the system must be described in terms of time differentials between delays imposed on falling and rising edges. As the cable length is increased, the propagation delays increase. Data-rate, as limited by pulse width distortion, is not affected by increasing cable length if the optical power level at the receiver is maintained.
10. Pulse width distortion is the difference between the delay of the rising and falling edges.
11. Both HFBR-1602 and HFBR-1604 meet the SERCOS "low attenuation" specifications when operated at 35 mA; only HFBR-1604 meets the SERCOS "high attenuation" limits when operated at 60 mA.

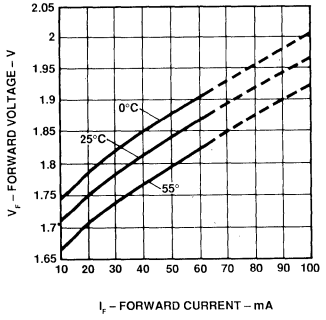


Figure 1. Forward Voltage and Current Characteristics.

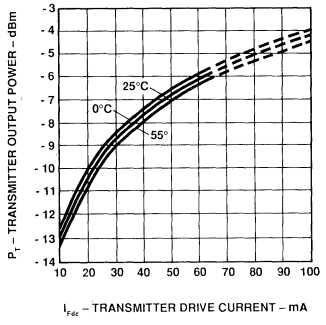


Figure 2. Typical Transmitter Output vs. Forward Current.

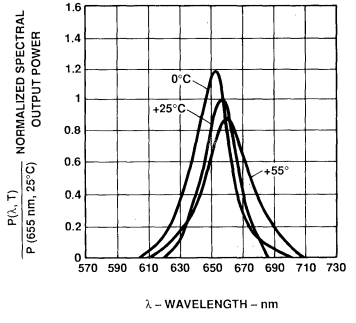


Figure 3. Transmitter Spectrum Normalized to the Peak at 25°C.

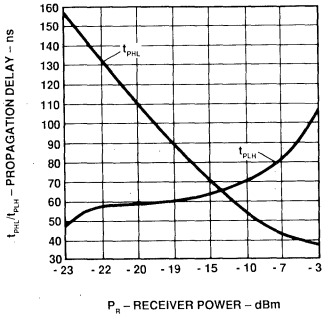


Figure 4. Typical Propagation Delay through System with 0.5 Metre of Cable.

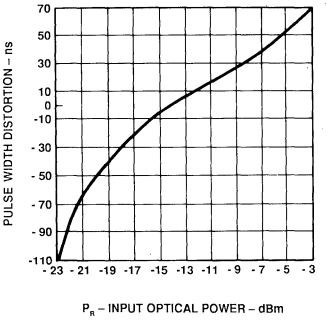


Figure 5. Typical HFBR-160X/2602 Link Pulsewidth Distortion vs. Optical Power.

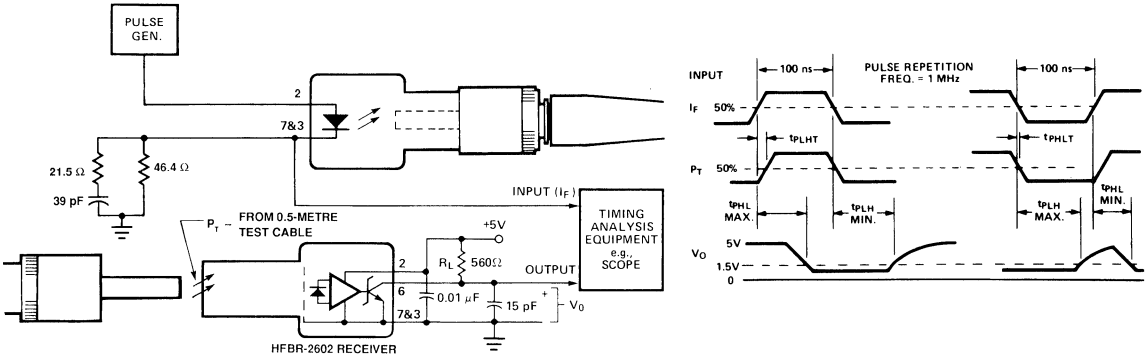


Figure 6. System Propagation Delay Test Circuit and Waveform Timing Definitions.

HEWLETT PACKARD

Glass Fiber-Optic Cable/ Connector Assemblies

Technical Data

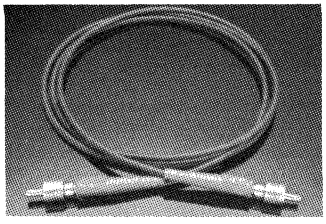
Features

- **Choice of ST or SMA Connectors**
- **Connectors Factory Installed and Tested**
- **Choice of 50/125 µm, 62.5/ 125 µm or 100/140 µm Fiber**
- **Tight Jacket Construction**
- **UL Recognized, Meets OFNR Listing (UL 1666)**
- **Parameters Optimized for Data Communication Applications**

Description

HP connectored cable assemblies are available in various industry standard sizes and styles. The designer may choose among 50/125 µm, 62.5/125 µm and 100/140 µm cable and ST and SMA connectors (50/125 µm is available with only ST connectors in one- and ten-metre lengths). These cable assemblies have been specified for use with HP's 820 nm and 1300 nm fiber-optic transmitters and receivers and are ideal for various data communication applications.

Each cable assembly has been factory assembled and 100% tested according to industry-standard procedures. Therefore, designers can be assured that they are receiving the highest possible quality cable assemblies for their prototyping, testing or production needs.



Ordering Information[1]

HFBR- □ □ □ □ □ □

Cable Code
A - 100/140 µm
B - 62.5/125 µm
C - 50/125 µm*

Connector Code
W - SMA connector
X - ST connector

Length Code
1-10 m, 1-m increments
e.g. 005 = 5 m
25-50 m, 5-m increments
e.g. 025 = 25 m

Channel Code
S - single channel
D - dual channel

*Available only in single channel one- and ten-metre lengths with ST connectors.

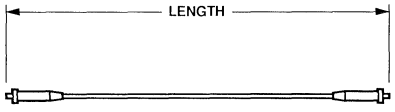
Order Examples

HFBR-AWS050, quantity 1: one 50 m simplex, 100/140 µm cable assembly with SMA connectors

HFBR-BXD005, quantity 2: two 5 m duplex, 62.5/125 µm cable assemblies with ST connectors

Cable Length Tolerances

Cable Length (metres)	Tolerance
1 - 10	+10/-0 %
25 - 50	+1/-0 metre



Cable Information

Temperature Ratings

Parameter	Min.	Max.	Unit
Storage Temperature	-40	+70	°C
Operating Temperature	-20	+70	°C

Mechanical Specifications (25°C)

Parameter	Single Channel	Dual Channel	Unit	Conditions	Note
Maximum Tensile Load				EIA-455-33	
Short Term	500	1000	N		2
Long Term	300	500	N		
Minimum Bend Radius					
Short Term	5.0	5.0	cm	500 N Tensile Load	
Long Term	3.0	3.0	cm	300 N Tensile Load	
Crush Resistance	750	750	N/cm	EIA-455-41	
Impact Resistance	1000	1000	cycles	EIA-455-25 @ 1.6 N-m	
Flex Resistance	7500	7500	cycles	EIA-455-104	
Maximum Vertical Rise	1000	1000	m		

OPTICAL SPECIFICATIONS (850 nm/1300 nm)

50/125 um 62.5/125 um 100/140 um Conditions

Maximum Attenuation (dB/km) 5.0/4.0 5.0/3.0 6.0/5.0 EIA-

Mechanical Dimensions

	50/125 µm	62.5/125 µm	100/140 µm
Core Diameter (µm)	50	62.5	100
Cladding Diameter (µm)	125	125	140
Buffer Diameter (µm)	900	900	900
Cable Outside Diameter (mm)			
Single Channel	2.9	2.9	2.9
Dual Channel	2.9x5.8	2.9x5.8	2.9x5.8

Optical Specifications (850 nm/1300 nm)

	50/125 µm	62.5/125 µm	100/140µm	Conditions
Maximum Attenuation (dB/km)	5.0/4.0	5.0/3.0	6.0/5.0	EIA-455-46
Typical Attenuation (dB/km)	4.0/2.0	4.5/2.0	5.5/3.5	
Minimum Modal Bandwidth (MHz-km)	400/400	160/200	100/100	EIA-455-30
Typical 3dB Optical Bandwidth- Length Product (MHz-km)[3]	41/250	40/180	38/95	
Numerical Aperture	0.20	0.275	0.29	EIA-455-47 method A,B,C

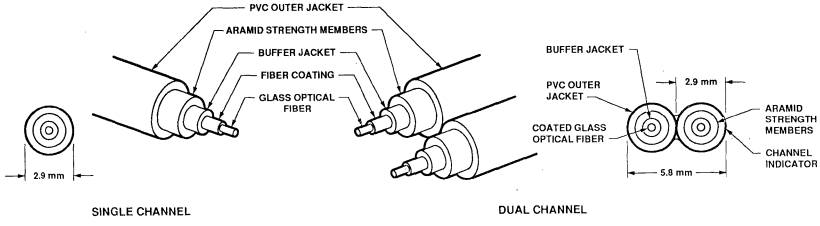


Figure 1. Cable Construction Diagram.

Notes:

1. HP is in the process of obsoleting the following part numbers and does not recommend their use for new designs: HFBR-AHDxxx and HFBR-AHSxxx cable assemblies, the HFBR-4000 connector, the HFBR-3099 mating adapter, and HFBR-0100/0101/0102 connectoring kits. Please contact your local HP components representative for more information.
2. Short term is ≤ 6 hours.
3. Calculations are based on worst case parameters of HP 820 nm and 1300 nm optical components.

HEWLETT PACKARD

Gigabit Rate Transmit Receive Chip Set

Technical Data

HDMP-1000 Tx/Rx Pair
HDMP-1002 Transmitter
HDMP-1004 Receiver

Features

- **Transparent, Extended Ribbon Cable Replacement**
- **High-Speed Serial Rate** 110-1400 MBaud
- **Standard 100K ECL Interface** 16, 17, 20, or 21 Bits Wide
- **Reliable Monolithic Silicon Bipolar Implementation**
- **On-chip Phase-Locked Loops**
  - Transmit Clock Generation
  - Receive Clock Extraction

Applications

- **Point to Point Data Links**
- **Implement SCI-FI Standard**
- **Implement Serial HIPPI Specification**
- **Backplane Extender**

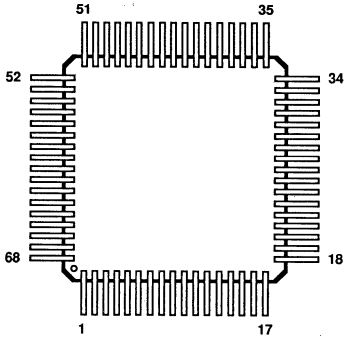
Description

The HDMP-1002 transmitter and the HDMP-1004 receiver are used to build a high speed data link for point to point communication. The HDMP-1000 consists of one HDMP-1002 and one HDMP-1004. The monolithic silicon bipolar transmitter chip and receiver chip are each provided in a standard, 68 pin, ceramic quad flat pack (CQFP).

From the user's viewpoint, these products can be thought of as providing a "virtual ribbon cable" interface for the transmission of data. Parallel data loaded into the Tx (transmitter) chip is delivered to the Rx (receiver) chip over a serial channel, which can be either a coaxial copper cable or optical link.

The chip set hides from the user all the complexity of encoding, multiplexing, clock extraction, demultiplexing and decoding. Unlike other links, the phase-locked-loop clock extraction circuit also transparently provides for frame synchronization - the user is not troubled with the periodic insertion of frame synchronization words. In addition, the dc balance of the line code is automatically maintained by the chip set. Thus, the user can transmit arbitrary data without restriction. The Rx chip also includes a state-machine controller (SMC) that provides a startup handshake protocol for the duplex link configuration.

Package Outline



PIN VIEW

The serial data rate of the T/R link is selectable in four ranges (see tables on page 3), and extends from 110Mbits/s up to 1.4Gbits/s. The parallel data interface is 16 or 20 bit single-ended ECL, pin selectable. A flag bit is available and can be used as an extra 17th or 21st bit under the user's control. The flag bit can also be used as an even or odd frame indicator for dual-frame transmission. If not used, the link performs expanded error detection. The serial link is synchronous, and both frame synchronization and bit synchronization are maintained. When data is not available to send, the link

maintains synchronization by transmitting fill frames. Two (training) fill frames are reserved for handshaking during link startup.

User control words are supported. If CAV* is asserted at the Tx chip, the least significant 14 or 18 bits of the data are sent and the Rx CAV* line will indicate the data as a control word.

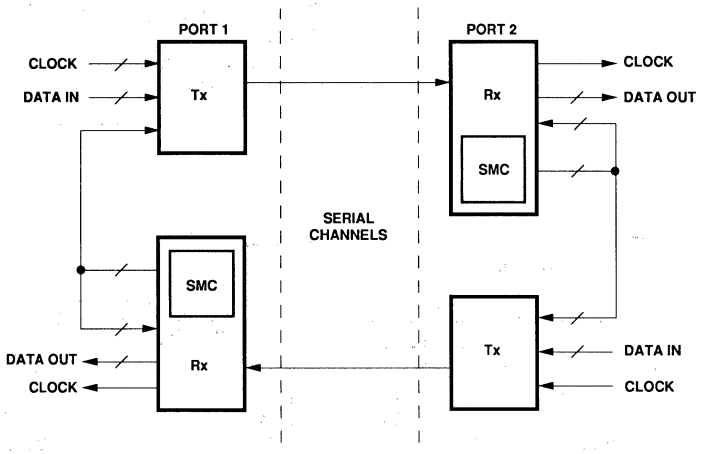


Figure 1. Point-to-Point Gigabit Data Link.

HDMP-1002 (Tx), HDMP-1004 (Rx)
Absolute Maximum Ratings

T_c = 25°C, except as specified. Operation in excess of any one of these conditions may result in permanent damage to this device.

Symbol	Parameter	Units	Minimum	Maximum
V_{EE}	Supply Voltage	V	-7	+0.5
$V_{IN,ECL}$	ECL Input Voltage	V	-3	+0.5
$V_{IN,BBL}$	H50 Input Voltage	V	-2	+1
$I_{O,ECL}$	ECL Output Source Current	mA		+50
T_{stg}	Storage Temperature	°C	-40	+130
T_J	Junction Temperature	°C	-40	+130
T_{max}	Maximum Assembly Temperature (for 10 seconds maximum)	°C		+260

HDMP-1002 (Tx), HDMP-1004 (Rx)
Guaranteed Operating Rates For 16 Bit Mode[1]

T_c = 0°C to +85°C, V_{EE} = -4.5 V to -5.5 V

		Parallel Word Rate (Mbit/sec)		Serial Data Rate (Mbit/sec)		Serial Baud Rate (MBaud)	
DIV1	DIV0	Min.	Max.	Min.	Max.	Min.	Max.
0	0	42.5	65	680	1040	850	1300
0	1	21.3	41	340	656	425	820
1	0	10.6	20.7	169.6	332	212	415
1	1	5.5	10.2	88	164	110	205

Note:
1. Extended operating rates to 1520 MBaud/sec (typ) are possible for T_c = 0°C to +55°C.

HDMP-1002 (Tx), HDMP-1004 (Rx)
Guaranteed Operating Rates For 20 Bit Mode[1]

T_c = 0°C to +85°C, V_{EE} = -4.5 V to -5.5 V

		Parallel Word Rate (Mbit/sec)		Serial Data Rate (Mbit/sec)		Serial Baud Rate (MBaud)	
DIV1	DIV0	Min.	Max.	Min.	Max.	Min.	Max.
0	0	35.4	58.3	708.3	1166.7	850	1400
0	1	17.7	34.2	354.2	683.3	425	820
1	0	8.8	17.3	176.6	345.8	212	415
1	1	4.6	8.5	91.7	170.8	110	205

Note:
1. Extended operating rates to 1640 MBaud/sec (typ) are possible for T_c = 0°C to +55°C.

HDMP-1002 (Tx), HDMP-1004 (Rx)
DC Electrical Specifications

T_c = 0°C to +85°C, V_{GND} = Ground, V_{EE} = -4.5 V to -5.5 V

Symbol	Parameter	Unit	Minimum	Typical	Maximum
$V_{IH,ECL}$	ECL Input High Voltage Level, Guaranteed high signal for all inputs	mV	-1150		
$V_{IL,ECL}$	ECL Input Low Voltage Level, Guaranteed low signal for all inputs	mV			-1600
$V_{OH,ECL}$	ECL Output High Voltage Level, Terminated with 300 Ω to -2.0 V	mV	-1050		
$V_{OL,ECL}$	ECL Output Low Voltage Level, Terminated with 300 Ω to -2.0 V	mV			-1500
$V_{IP,H50}$	H50 Input Peak-to-Peak Voltage	mV	200		
$V_{OH,BLL}$	BLL Output High Voltage Level, Terminated with 50 Ω to -1.3 V	V		-0.9	
$V_{OL,BLL}$	BLL Output Low Voltage Level, Terminated with 50 Ω to -1.3 V	V		-1.70	
$V_{OP,BLL}$	BLL Output Peak-to-Peak Voltage, Terminated with 50 Ω, ac coupled	V		+0.8	
$I_{EE,Tx}$	Transmitter V_{EE} Supply Current, with HCLKSEL off, V_{EE} = -5.0 V, T_c = 25°C	mA		+340	
$I_{EE,Rx}$	Receiver V_{EE} Supply Current, V_{EE} = -5.0 V, T_c = 25°C	mA		+427	

HDMP-1002 (Tx), HDMP-1004 (Rx)
AC Electrical Specifications, T_c = 25°C

Symbol	Parameter	Unit	Min.	Typ.	Max.
$t_{r,ECL}$	ECL Rise Time, (20-80%), Terminated with 300 Ω to -2.0 V	nsec		1	
$t_{f,ECL}$	ECL Fall Time, (80-20%), Terminated with 300 Ω to -2.0 V	nsec		2	
$t_{r,BLL}$	BLL Rise Time, (20-80%), Terminated with 50 Ω, ac coupled	psec		170	
$t_{f,BLL}$	BLL Fall Time, (80-20%), Terminated with 50 Ω, ac coupled	psec		200	
$VSWR_{i,H50}$	H50 Input VSWR			2:1	
$VSWR_{o,BLL}$	BLL Output VSWR			2:1	

HDMP-1002 (Tx)
Timing Characteristics

T_c = 0°C to +85°C, V_{EE} = -4.5 V to -5.5 V

Symbol	Parameter	Unit	Min.	Typ.	Max.
t_s	Setup Time, for Rising Edge of STRBIN Relative to D_0-D_{19}, ED, FF, DAV*, CAV*, and FLAG	nsec		2.0	
t_h	Hold Time, for Rising Edge of STRBIN Relative to D_0-D_{19}, ED, FF, DAV*, CAV*, and FLAG	nsec		2.0	
t_d	Delay Time, from Rising Edge of STRBIN to First Data Bit Out (D_0)	nsec		1.0	
ΔT_{strb}	STRBOUT - STRBIN Delay	nsec	1	3	5

HDMP-1004 (Rx)
Timing Characteristics

T_c = 0°C to +85°C

Symbol	Parameter	Unit	Min.	Typ.	Max.
t_{d1}	Synchronous Output Delay	nsec		2.0	
t_{d2}	State Machine Output Delay	nsec		4.0	

HDMP-1002 (Tx), HDMP-1004 (Rx)
Typical Lock-Up Time, T_c = 25°C

DIV1	DIV0	HDMP-1002, msec	HDMP-1004, msec	LINK[1], msec
0	0	2.0	2.2	2.5
0	1	3.0	3.2	3.5
1	0	4.5	4.7	5.0
1	1	8.0	11.0	12.0

Note:
1. Measured in Local Loop-Back mode with the state machine engaged and 0 cable length.

HDMP-1002 (Tx)
Thermal Characteristics, T_A = 25°C

Symbol	Parameter	Units	Typical
θ_{jc}	Thermal Resistance Die to Case	°C/Watt	12
P_D	Power Dissipation, V_{EE} = -5 V	Watt	1.75

HDMP-1004 (Rx)
Thermal Characteristics, T_A = 25°C

Symbol	Parameter	Units	Typical
θ_{jc}	Thermal Resistance Die to Case	°C/Watt	12
P_D	Power Dissipation, V_{EE} = -5 V	Watt	2.25

I/O Type Definitions

I/O Type	Definition
I-ECL	Input ECL. Similar to 100K ECL, but with pull-down. Thus, if the input is left unconnected, the buffer generates a default value of "0". The input can also be directly connected to ground to generate a "1".
O-ECL	Output ECL. Similar to 100K ECL but should be terminated with RTT ≥300 Ω, and do not exceed 10 cm connection distance.
IT-ECL	Input Test ECL. Can be turned off when not used.
OT-ECL	Output Test ECL. Can be turned off when not used.
O-BLL	50 Ω buffer line logic output driver. Will put out ECL levels if terminated with 50 Ω to -1.3 V, otherwise can be AC coupled to drive any 50 Ω loads. It can also drive the I-H50 inputs through differential direct coupling. Note: all unused outputs should be terminated with 50 Ω to ground.
I-H50	Input with internal 50 Ω terminations. Input is diode level shifted so that it can swing around ground. Can be driven with single-end configuration. Commonly used with input single-end AC coupling from an O-BLL driver or another 50 Ω source, or differential direct coupling from an O-BLL driver.
C	Filter capacitor node.
S	Power supply or ground.

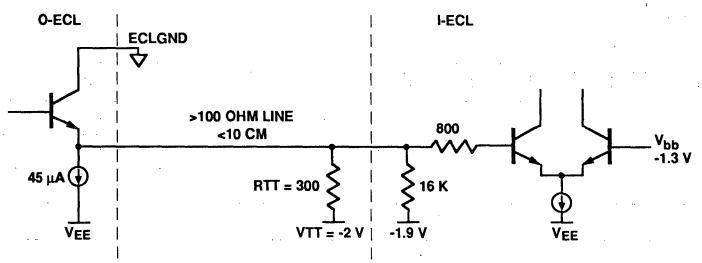


Figure 2. O-ECL and I-ECL Simplified Circuit Schematic.

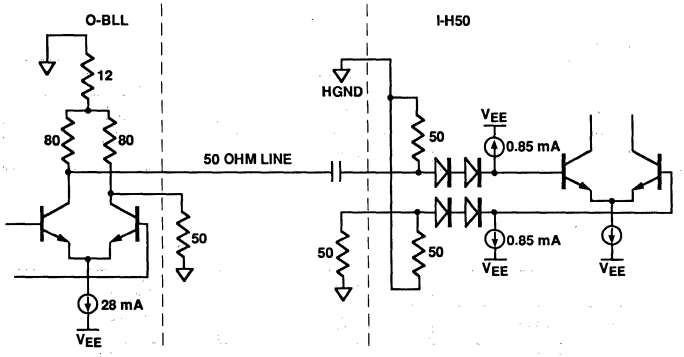


Figure 3. O-BLL and I-H50 Simplified Circuit Schematic.

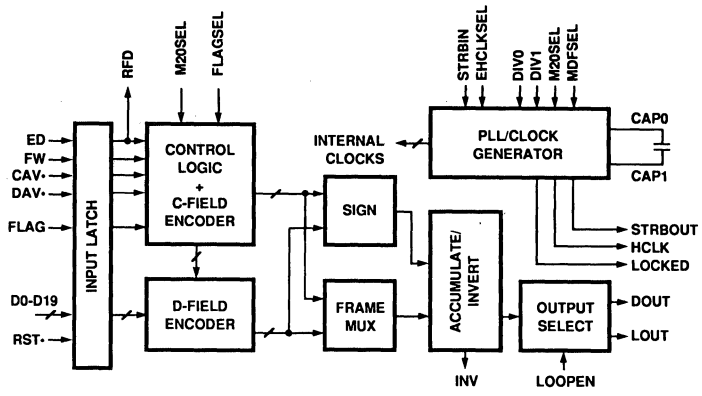


Figure 4. HDMP-1002 (Transmitter) Block Diagram.

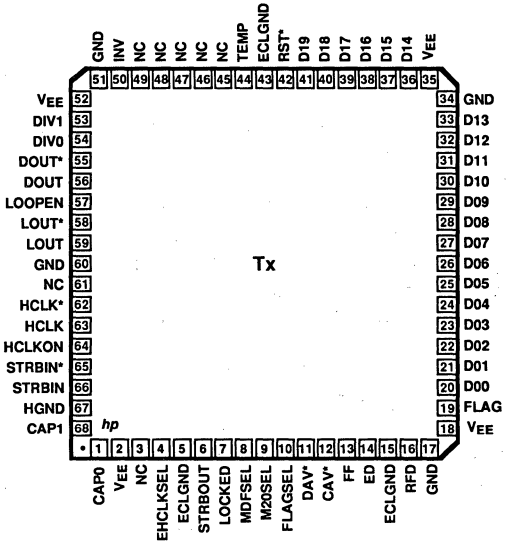


Figure 5. HDMP-1002 Package Layout, Pin View.

Tx I/O Definition

Name	Pin	Type	Signal
D00 D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19	20 21 22 23 24 25 26 27 28 29 30 31 32 33 36 37 38 39 40 41	I-ECL	**Data Inputs:** 20 Bit data is encoded and transmitted when M20SEL is active; otherwise the 16 least significant bits are encoded and transmitted. The encoded bits are transmitted LSB first, e.g.: D0 is sent first, through to either D15 or D19, followed by the 4 coding bits C0-C3.
FLAG	19	I-ECL	**Extra Flag Bit:** When FLAGSEL is active, this input is sent as an extra data bit in addition to the normal Data inputs. When FLAGSEL is not Asserted, this input is ignored and the transmitted Flag bit is internally alternated to allow the Rx chip to perform enhanced frame error detection.
DAV*	11	I-ECL	**Data Available Input:** This active-low input tells the chip that the user has valid data to be transmitted. This pin should be asserted only after the user has determined that the RFD line is active for a given frame cycle. When this pin is asserted, the information on the Data and Flag inputs is encoded and sent as a Data frame.
CAV*	12	I-ECL	**Control Word Available Input:** This active-low input tells the chip that the user is requesting a control word be transmitted. This pin should only be asserted after the user has determined the RFD line is active for a given frame cycle. When this pin is asserted, the information on the Data inputs is sent as a control frame. If CAV and DAV are asserted simultaneously, CAV takes precedence.
RFD	16	O-ECL	**Ready for Data:** Output to tell the user the Link is ready to transmit data. This pin is a retimed version of the ED input, which is driven by the Rx chip state machine controller.
STRBIN STRBIN*	66 65	I-H50	**Data Clock Input:** When EHCLKSEL is low, this input is phase locked and multiplied to generate the high speed serial clock. The chip expects a clock frequency which is equal to the input frame rate if MDFSEL (double frame mode) is low, and 1/2 the frame rate if MDFSEL is high. When EHCLKSEL is high, the PLL is bypassed, and STRBIN directly becomes the high speed serial clock. In all cases, STRBOUT is derived from the high speed serial clock, and the input data is latched in on the rising edge of STRBOUT.

Tx I/O Definition (cont'd.)

Name	Pin	Type	Signal
STRBOUT	6	O-ECL	**Frame-rate Data Clock Output:** This output is always a frame rate clock derived from STRBIN. Input data is latched on the rising edge of STRBOUT. With a buffer or pulled down with a 1 K resistor to V_{EE} and ac-coupled, this output is ideal for triggering an oscilloscope for examining the serial output eye pattern DOUT or LOUT.
DOUT DOUT*	56 55	O-BLL	**Normal Serial Data Output:** Output used when LOOPEN is not active. This output is a special *buffer line logic* driver which is a 50 Ω back-terminated ECL compatible output.
LOUT LOUT*	59 58	O-BLL	**Loop Back Serial Data Output:** Output used when LOOPEN is active. Typically, this output will be used to drive the LIN, LIN* inputs of the Rx chip.
LOOPEN	57	I-ECL	**Loop Back Control:** Input which controls whether the DOUT, DOUT* or the LOUT, LOUT* outputs are currently enabled. If active, LOUT, LOUT* are enabled. The unused output is powered down to reduce dissipation.
FLAGSEL	10	I-ECL	**Flat Bit Mode Select:** When this input is high, the extra FLAG bit input is sent as an extra transparent data bit. Otherwise, the FLAG input is ignored and the transmitted flag bit is internally alternated by the transmitter. The Rx chip can provide enhanced frame error detection by checking for strict alternation of the flag bit during data frames. The FLAGSEL input on the Rx chip should be set to the same value as the Tx FLAGSEL input.
M20SEL	9	I-ECL	**16 or 20 Bit Word Select:** When this signal is high, the link operates in 20 Bit data transmission mode. Otherwise, the link operates in 16 Bit mode.
MDFSEL	8	I-ECL	**Select Double Frame Mode:** When this signal is high, the PLL expects a 1/2 speed parallel clock at STRBIN. The chip then internally multiplies this clock and produces a full-rate parallel clock at STRBOUT. This feature is provided so that either a 40 bit or 32 bit word can be easily transmitted as two 20, or two 16 bit words. When MDFSEL is low, the PLL expects a full-rate parallel clock at STRBIN, and returns a locked replica of STRBIN on the STRBOUT pin. In both modes Data is latched on the rising edge of STRBOUT.
DIV0 DIV1	54 53	ECL	**VCO Divider Select:** These two pins program the VCO divider chain to operate at full speed, half speed, quarter speed, or one-eighth speed.
RST*	42	I-ECL	**Chip Reset:** This active-low pin initializes the internal chip registers. It should be asserted during power up for a minimum of 5 parallel-rate clock cycles to ensure a complete reset.
ED	14	I-ECL	**Enable Data:** This signal comes from the Rx chip state machine and is used to control the RFD output of the Tx chip. The state machine only allows data to be enabled when both sides of the link have established stable lock.

Tx I/O Definition (cont'd.)

Name	Pin	Type	Signal
FF	13	I-ECL	**Fill Frame Select:** When neither CAV or DAV is asserted, or when ED is false, fill frames are automatically transmitted to allow the Rx chip to maintain lock. The type of fill frame sent is determined by the state of this pin. FF0s are sent if low, and either FF1a or FF1b is sent if FF is high. The choice of FF1a or FF1b is determined by the state of the cumulative line DC balance.
LOCKED	7	O-ECL	**Loop In-lock Indication:** This signal indicates the lock status of the Tx PLL. A high value indicates lock. This signal is normally connected to the SMTRST1 reset input of the Rx state machine to force the link into the start-up state until the Tx PLL has locked. This signal may give multiple false-lock indications during the acquisition process, so should be debounced if it is used for any other purpose than to drive the Rx chip.
CAP0D CAP0S CAP1D CAP1S	1 1 68 68	C	**Loop Filter Capacitor:** A loop filter capacitor may be connected across the CAP0 and CAP1 inputs to increase the loop time constant. The packaged part contains a nominal capacitance internally so that under normal conditions no external capacitor is required.
INV	50	O-ECL	**Invert Signal:** A high value of INV implies that the current frame is being sent inverted to maintain long-term DC balance. With a buffer, or pulled down with a 1K resistor to V_{EE} and ac coupled, this signal is useful as an aid to analyzing the serial output stream with an oscilloscope.
TEMP	44	T	**Temperature Sense Diode:** Used during wafer and package test only. It should be left open otherwise.
HCLKON	64	I-ECL	**HCLK Power-down Control:** When this pin is de-asserted, the HCLK, HCLK* outputs are powered down to reduce power dissipation.
HCLK HCLK*	63 62	O-BLL	**High Speed Clock Monitor:** Used to monitor actual clock signal used to transmit the serial data. This signal will either be the divided VCO output, or the divided external clock input, depending on the value of the EHCLKSEL input.
EHCLKSEL	4	I-ECL	**EHCLK Enable:** When active, this input causes the STRBIN inputs to be used for the transmit serial clock, rather than the internal VCO clock. This is useful for generating extremely low jitter test signals, or for operating the link at speeds that are not within the VCO range. When the EHCLKSEL is active, it is necessary for the data source to take its clock from the link rather than the usual operation where the Link phase-locks onto the data source clock.
GND	60 51 34 17	S	**Ground:** Normally 0 volts. This ground is used for everything other than the noisy ECL outputs

Tx I/O Definition (cont'd.)

Name	Pin	Type	Signal
HGND	67	S	**High Speed Ground:** Normally 0 volts. This ground is used to provide a clean reference for STRBIN and STRBIN* inputs. For optimum impedance matching, it is suggested that the physical distance between this pin and the ground plane be minimized.
ECLGND	43 15 5	S	**ECL Ground:** Normally 0 volts. This ground is used for the ECL pad drivers. For best performance it is suggested that coupling of the noisy ECLGND to the clean GND and HGND grounds be minimized.
V_{EE}	52 35 18 2	S	**Power:** Normally -5 V ± 10%.

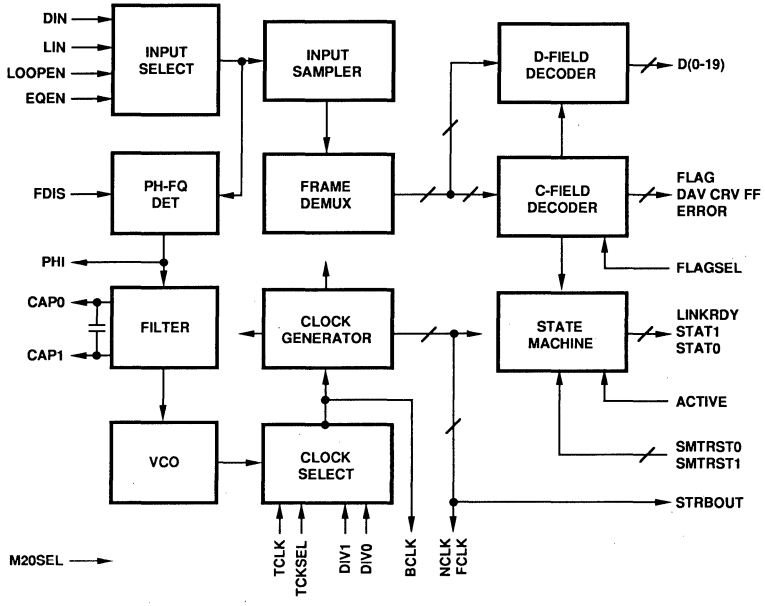


Figure 6. HDMP-1004 (Receiver) Block Diagram.

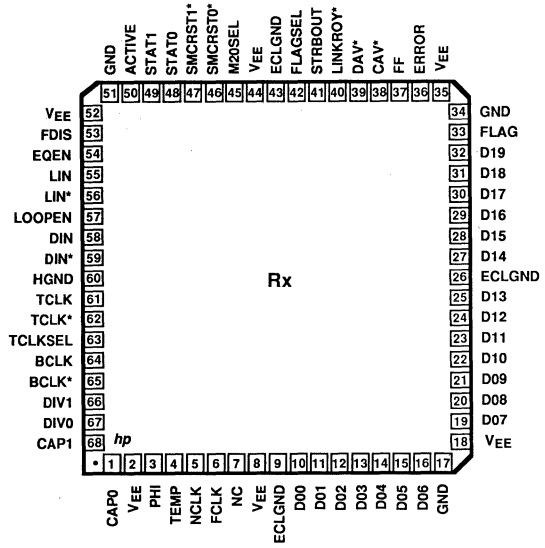


Figure 7. HDMP-1004 (Rx) Package Layout, Pin View.

Rx I/O Definition

Name	Pin	Type	Signal
DIN DIN*	58 59	I-H50	**Normal Serial Data Input:** This is the input used when LOOPEN is not active. When LOOPEN is high, the loop back data inputs LIN, LIN* are used instead. An optional cable equalizer may be enabled for the DIN, DIN* inputs by asserting EQEN.
LIN LIN*	55 56	I-H50	**Loop Back Serial Data Input:** Use this input when LOOPEN is active. Unlike the DIN, DIN* inputs, this input does not have a cable equalizer. In normal usage, this input will be connected to the Tx chip LOUT, LOUT* outputs. This allows the user to check the near-end functionality of the Tx and Rx pair independent of the transmission medium.
LOOPEN	57	I-ECL	**Loop Back Control:** When asserted, this signal causes the loop back inputs LIN, LIN* to be used instead of the normal data inputs DIN, DIN*.
EQEN	54	I-ECL	**Enable Input for Cable Equalization:** When asserted, this signal activates the cable equalization amplifier on the DIN, DIN* serial data inputs.

Rx I/O Definition (cont'd.)

Name	Pin	Type	Signal
D00 D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19	10 11 12 13 14 15 16 19 20 21 22 23 24 25 27 28 29 30 31 32	O-ECL	**Data Outputs:** 20 Bit data is received and decoded when M20SEL is active; otherwise 16 bit data is decoded and the D16-D19 bits are undefined.
FLAG	33	O-ECL	**Flag Bit:** If both Tx and Rx have FLAGSEL asserted, this output indicates the value of the transmitted flag bit, then this received bit can be treated just like an extra data bit. If both Tx and Rx have FLAGSEL set to low, FLAG is used to differentiate the even frame from the odd frame in the line code.
LINKRDY*	40	O-ECL	**Link Ready Indicator:** This active-low output is a retimed version of the ACTIVE input. ACTIVE is normally driven by the Rx state machine output. LINKRDY then indicates that the startup sequence is complete and that the data and control indications are valid.
DAV*	39	O-ECL	**Data Available Output:** This active-low output indicates that the Rx chip data outputs are received Data frames. Data should be latched on the rising edge of STRBOUT. Note that during link startup, false data indications may be given. If the user is concerned about this possibility, then the DAV indication should be combined with the LINKRDY output before being used.
CAV*	38	O-ECL	**Control Frame Available Output:** This active-low output indicates that the Rx chip data outputs are receiving Control Frames. False CAV indications may be generated during link startup.
FF	37	O-ECL	**Fill Frame Status:** During a given STRBOUT clock cycle, if neither DAV, CAV, or ERROR are active, then the currently received frame is a Fill frame. The type of Fill frame received is indicated by the FF pin. If FF is low, then FF0 has been received. If FF is high, then either FF1a or FF1b has been received.
ERROR	36	O-ECL	**Received Data Error:** Asserted when a frame is received that does not correspond to either a *valid* Data, Control, or Fill frame encoding.When FLAGSEL is not active, the Rx chip also tests for strict alternation of flag bits during data frames. A flag bit alternation error will also cause an ERROR indication.

Rx I/O Definition (cont'd.)

Name	Pin	Type	Signal
STRBOUT	41	O-ECL	**Recovered Frame-rate Data Clock Output:** This output is the PLL recovered frame rate clock. D0-D19, FLAG, DAV CAV, FF, LINKRDY, and ERROR should all be latched on the rising edge of STRBOUT.
FLAGSEL	42	I-ECL	**Flag Bit Mode Select:** When this input is high, the extra FLAG bit output is effectively an extra transparent data bit. Otherwise, the FLAG bit is checked for alternation during data frames. Any break in strict alternation results in an ERROR indication to the user.
M20SEL	45	I-ECL	**16 or 20 Bit Word Select:** When this signal is high, the link operates in 20 Bit data reception mode. Otherwise, the link operates in 16 Bit mode and data outputs D16-D19 are undefined.
DIV0 DIV1	67 66	I-ECL	**VCO Divider Select:** These two pins program the VCO divider chain to operate at full speed, half speed, quarter speed or one-eighth speed.
FDIS	53	I-ECL	**Frequency Detector Disable Input:** When active, this input disables the Rx PLL Frequency detector and enables a phase detector. The Frequency detector is used during the start-up sequence to acquire wide-band lock on Fill Frames, but must be disabled prior to sending data patterns. This input is normally controlled by the Rx state machine.
ACTIVE	50	I-ECL	**Chip Enable:** This input is normally driven by the Rx state machine output. The ACTIVE signal is internally retimed by STRBOUT and presented to the user as the LINKRKDY signal. This is how the Rx state machine signals the user that the start-up sequence is complete.
SMCRST0* SMCRST1*	46 47	I-ECL	**State Machine Reset Inputs:** Each of these active-low input pins reset the Rx state machine to the initial start-up state. This initiates a complete PLL restart and handshake at both ends of the duplex link. Normally, SMCRST0* is connected to a power-up reset circuit or a host system reset signal. The SMCRST1* input is normally connected to the Tx LOCKED output. The LOCKED signal holds the state-machine in the start-up state until the Tx PLL is locked.
STAT0 STAT1	48 49	O-ECL	**State Machine Status Outputs:** These outputs indicate the current state-machine state. They are used to directly control the Tx ED, Tx FF, Rx FDIS, and Rx ACTIVE lines.
CAP0D CAP0S CAP1D CAP1S	1 1 68 68	C	**Loop Filter Capacitor:** A loop filter capacitor may be connected across the CAP0 and CAP1 inputs to increase the loop time constant. The packaged part contains a nominal capacitance internally so that under normal conditions no external capacitor is required. Each package pin is split into two die pads: suffixed "D" for drive and "S" for sense. This enables a four-point probe arrangement to be used to reduce noise in the loop.

Rx I/O Definition (cont'd.)

Name	Pin	Type	Signal
PHI	3	O-ECL	**Phase Detector Test Output:** The output from the phase/ frequency detector in the Rx PLL. When PHI is high, the VCO should increase frequency. If low, the VCO should decrease frequency.
NCLK	5	O-ECL	**Nibble Clock Monitor:** Leave unterminated in normal use.
FCLK	6	O-ECL	**Frame Clock Monitor:** Leave unterminated in normal use.
TEMP	4	T	**Temperature Sense Diode:** Used during wafer and package test only. It should be left open otherwise.
BCLK BCLK*	64 65	O-BLL	**VCO Monitor Output:** These pins provide access to the internal VCO clock.
TCLKSEL	63	I-ECL	**Enable Test Clock Input:** When this input is active, the TCLK, TCLK* inputs are used in place of the normal VCO signal. This feature is useful both for synchronous systems and for chip testing.
TCLK TCLK*	61 62	I-H50	**External VCO Replacement Test Clock:** When TCLKSEL is enabled, this input is used in place of the normal VCO signal, effectively disabling the PLL and allowing the user to provide an external retiming clock for testing.
GND	17 34 51	S	**Ground:** Normally 0 volts. This ground is used for all the core logic other than the output drivers.
HGND	60	S	**High Speed Ground:** Normally 0 volts. This ground is used to provide clean references for the high speed DIN, DIN*, LIN, LIN*, TCLK, TCLK* inputs.
ECLGND	9 26 43	S	**ECL Ground:** Normally 0 volts. This ground is used for the ECL pad drivers. For best performance it is suggested that coupling of the noisy ECLGND to the clean GND and HGND grounds be minimized.
V_{EE}	2 8 18 35 44 52	S	**Power:** Normally -5 V ± 10%
NC	5 6 7	B	**Pins Not Connected:** Pins that are not used, or are reserved for future use. No connection should be made to any of these signals to ensure compatibility with future releases.

HDMP-1002 (Tx) Timing

Figure 8 shows the Tx timing diagram. Under normal operation, the Tx PLL locks to the STRBIN input with an internal frame clock. This frame clock is buffered to form STRBOUT with a delay of ΔT_{strb}. For the case when MDFSEL is low, INFRMCLK is a phase locked version of STRBIN. If MDFSEL is high, it is assumed that STRBIN is a one half frame rate clock and INFRMCLK is twice the frequency of STRBIN. If EHCLKSEL is high, the Tx uses the external high-speed clock from STRBIN instead of its internal VCO, and generates the appropriate INFRMCLK from the STRBIN inputs. When M20SEL is high, INFRMCLK is 1/24th the frequency of HCLK. When M20SEL is low, INFRMCLK is 1/20th the frequency of HCLK.

The input signals, D0-D19, ED, FF, CAV*, DAV*, and FLAG are latched on the rising edge of INFRMCLK. These inputs must be valid for the set-up time (t_s) before the rising edge and for the hold time (t_h) after the rising edge of INFRMCLK.

The start of a frame in the high speed serial output occurs after a delay of (t_d) after the rising edge of INFRMCLK.

The LOCKED output will stay low for at least 2 frame rate clock cycles when lock is lost.

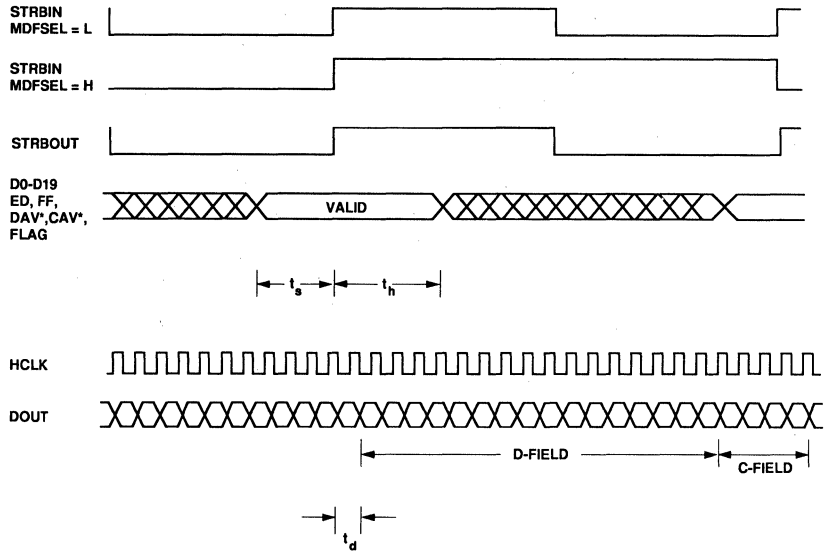


Figure 8. HDMP-1002 (Tx) Timing Diagram.

HDMP-1004 (Rx) Timing

Figure 9 is the Rx timing diagram when the internal phase-locked loop is in synchronization with the incoming serial data. When the PLL is locked, the BCLK's frequency is the same as the input data rate. The nibble clock, NCLK, is derived from the BCLK and a divide-by-4 divider. The size of the input data frame can be either 24 bits (6 nibbles) or 20 bits (5 nibbles), depending on the setting of M20SEL. Whatever the frame size, the FCLK rising edge is located at the frame's boundary, while the falling edge is at the frame's center. STRBOUT is an inverted version of FCLK.

In Figure 9, the Synchronous Outputs are the Rx's output signals clocked by STRBOUT. They are LINKRDY*, FLAG, DAV, CAV, FF, ERROR, and D00-D19. The Synchronous Outputs are updated for every data frame, and changed at the falling edge of STRBOUT. There is a delay of two frames between the serial input and the Synchronous Outputs. As for the state machine status outputs, STATI and STATO, they are also changed upon the STRBOUT's falling edge, but are only updated once in 128 frames.

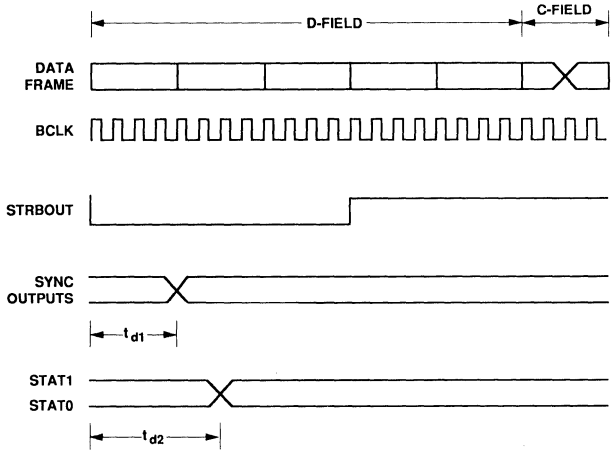


Figure 9. HDMP-1004 (Rx) Timing Diagram.

Line Code Description

The HDMP-1000 line code, Conditional Invert Master Transition (CIMT), is illustrated in Figure 10. The CIMT line code uses three types of frames; Data frames, Control frames, and Fill frames. Fill frames are internally generated by the Tx chip for use during link start up and when there is no input from the user. Each frame consists of a Data Field (D-Field) followed by a Coding Field (C-Field). The D-Field can be either 16 bit or 20-bits wide, depending on link configuration. The C-Field has a master transition which serves as a fixed timing reference for the receivers clock recovery circuit. Users can send arbitrary data carried by Data or Control Frames. The dc balance of the line code is automatically enforced by the Tx. Fill frames have a single rising edge at the master transition which is used for clock recovery and frame synchronization at the receiver.

Detailed coding schemes are described in the following subsections. All the tables given in this section show data bits in the same configuration as a scope display. In other words, the leftmost bit in each table is the first bit to be transmitted in time, while the rightmost bit is the last bit to be transmitted.

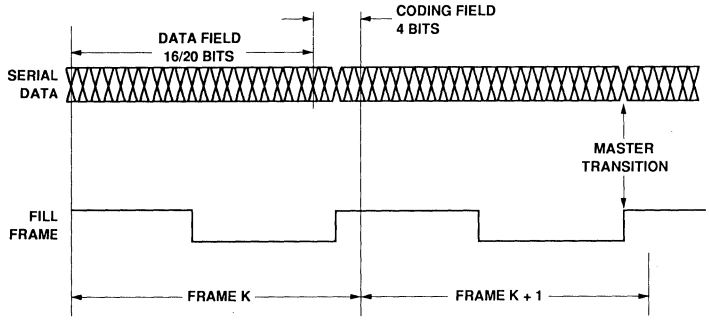


Figure 10. HDMP-1000 (Tx/Rx Pair) Line Code.

Data Frame Codes

When not in FLAGSEL mode, the FLAG bit is not user controllable and is alternately sent as 0 and 1 by the Tx chip during data frames to provide enhanced error detection. Control and Fill frames do not cause toggling between even and odd frames to occur (The FLAG bit is not available during control frames). The receiver performs a differential detection to make sure that every data frame received is the opposite pattern from the previous frame. If a break in the strict alternation is observed, a frame error is flagged by asserting the Rx ERROR output. This pattern detection makes it impossible for a static input data pattern to generate an undetectable false lock point in the transmitted data stream. The detection also reduces the probability that the loop could lock onto random data at a point away from the true master transition for any significant time before it would be detected as a false lock. This mode can detect all single-bit errors in the C-field (non-data bit fields) of the frame.

When the chip is in FLAGSEL mode, the extra FLAG bit is freely user definable as an extra data bit. This provides a 17th bit in 16 bit mode, and a 21st bit in 20 bit mode. The probability of undetected false lock is higher, but the users (e.g., SCI-FI) that need the extra bit can detect false lock at a higher level of the network protocol with CRCs, etc. If the higher level protocols consistently receive wrong data, they can initiate a link restart by resetting the Rx state machine.

HDMP-1002 (Tx), HDMP-1004 (Rx)

Operating Modes

M20SEL	FLAGSEL	Description
0	0	16 bit data plus EO checking
0	1	16 bit data plus FLAG
1	0	20 bit data plus EO checking
1	1	20 bit data plus FLAG

HDMP-1002 (Tx), HDMP-1004 (Rx)

Data Frame Structure
M20SEL Not Asserted (16 bit data mode)

Data Status	Flag Bit	D-Field	C-Field
True	0	$D_0 - D_{15}$	1101
Inverted	0	$\overline{D_0 - D_{15}}$	0010
True	1	$D_0 - D_{15}$	1011
Inverted	1	$\overline{D_0 - D_{15}}$	0100

HDMP-1002 (Tx), HDMP-1004 (Rx)

Data Frame Structure
M20SEL Asserted (20 bit data mode)

Data Status	Flag Bit	D-Field	C-Field
True	0	$D_0 - D_{19}$	1101
Inverted	0	$\overline{D_0 - D_{19}}$	0010
True	1	$D_0 - D_{19}$	1011
Inverted	1	$\overline{D_0 - D_{19}}$	0100

Control Frame Codes

There are 2^{18} control words provided in 20 bit mode. If the user desires to send a control word, his lower 9 bits (D_0-D_8) are sent as bits D0-D8 of the D-Field. The user's next 9 bits (D_9-D_{17}) are sent as bits D11-D19 of the D-Field. The control frame is either inverted or not inverted as needed to maintain balance, with the coding bits 0011 used to indicate true control, and the bits 1100 used to indicate complement control. The bits D9 and D10 are always forced to 0 1 for true control frames and 1 0 for complement control frames. These middle bits are used to distinguish true control frames from fill frames, which always have the middle bits set to either 00, 11, or 10. Similarly, there are 2^{14} control words provided in 16 bit mode.

HDMP-1002 (Tx), HDMP-1004 (Rx)

Control Frame Structure
M20SEL Not Asserted (16 bit mode)

D-Field				C-Field			
D0 - D6	D7	D8	D9 - D15	C0	C1	C2	C3
$D_0 - D_6$	0	1	$D_7 - D_{13}$	0	0	1	1
$\overline{D_0 - D_6}$	1	0	$\overline{D_7 - D_{13}}$	1	1	0	0

HDMP-1002 (Tx), HDMP-1004 (Rx)

Control Frame Structure
M20SEL Asserted (20 bit mode)

D-Field				C-Field			
D0 - D8	D9	D10	D11 - D19	C0	C1	C2	C3
$D_0 - D_8$	0	1	$D_9 - D_{17}$	0	0	1	1
$\overline{D_0 - D_8}$	1	0	$\overline{D_9 - D_{17}}$	1	1	0	0

Fill Frame Codes

Two logical fill frames are provided: FF0 and FF1. FF0 is physically a 50% duty cycle wave form with its sole rising edge occurring between C1 and C2. Logical FF1 toggles between two different physical codes, the first of which advances the falling edge of FF0 by one bit, the second of which retards the falling edge of FF0 by one bit. Two logical fill frame types are required for link start up in duplex mode.

HDMP-1002 (Tx), HDMP-1004 (Rx)

Fill Frame Structure
M20SEL Not Asserted (16 bit mode)

Fill Frame	D-Field			C-Field
0	1111111	10	0000000	0011
1a	1111111	11	0000000	0011
1b	1111111	00	0000000	0011

HDMP-1002 (Tx), HDMP-1004 (Rx)

Fill Frame Structure
M20SEL Asserted (20 bit mode)

Fill Frame	D-Field			C-Field
0	111111111	10	000000000	0011
1a	111111111	11	000000000	0011
1b	111111111	00	000000000	0011

HDMP-1004 (Rx)

Detectable Error States
M20SEL Not Asserted (16 bit mode)

D-Field			C-Field
xxxxxxx	xx	xxxxxxx	x00x
xxxxxxx	xx	xxxxxxx	x11x
xxxxxxx	0x	xxxxxxx	1100
xxxxxxx	11	xxxxxxx	1100
xxxxxxx	xx	xxxxxxx	1010
xxxxxxx	xx	xxxxxxx	0101

HDMP-1004 (Rx)

Detectable Error States
M20SEL Asserted (20 bit mode)

D-Field			C-Field
xxxxxxxxx	xx	xxxxxxxxx	x00x
xxxxxxxxx	xx	xxxxxxxxx	x11x
xxxxxxxxx	0x	xxxxxxxxx	1100
xxxxxxxxx	11	xxxxxxxxx	1100
xxxxxxxxx	xx	xxxxxxxxx	1010
xxxxxxxxx	xx	xxxxxxxxx	0101

Tx Operation Principles

The HDMP-1002 (Tx) is implemented in a high performance silicon bipolar process. The Tx performs the following functions for link operation:

- Phase lock to frame rate clock
- Clock multiplication
- Frame Encoding
- Multiplexing

In normal operation, the Tx phase locks to a user supplied frame rate clock and multiplies the frequency to produce the high speed serial clock. When locked, the Tx indicates that it is locked by asserting the LOCKED output. When the ED input is asserted, the Tx asserts the RFD signal indicating that it is now ready to transmit data or control frames.

The Tx can accept either 16 or 17 bit data and produce a 20 bit frame. It also can accept 20 or 21 bit data and produce a 24 bit frame. Similarly, either 14 bit or 18 bit control words can be transmitted in a 20 bit or 24 bit frame respectively.

Tx Encoding

A simplified block diagram of the transmitter is shown in Figure 4. The PLL/Clock Generator Block locks onto the incoming frame rate (or one-half frame rate) clock and multiplies it up to the serial clock rate. It also generates all the internal clock signals required on the Tx chip.

The data inputs, D0-D19, as well as the control signals; ED, FF, DAV*, CAV*, and FLAG are latched in on the rising edge of the frame rate clock. The data field is then encoded depending on the state of the control signals. At the same time, the coding field is generated. At this point, the entire frame has been constructed in parallel form and its sign is determined. This frame sign is compared with the accumulated sign of previously transmitted bits to decide whether to invert the frame. If the sign of the current frame is the same as the sign of the previously transmitted bits, then the frame is inverted. If the signs are opposite, the frame is not inverted. No inversion is performed if the frame is a fill frame.

The Output Select block allows the user to select between two sets of differential high speed serial outputs. This is useful for loop back testing. If LOOPEN is high, LOUT is enabled and DOUT is disabled. If LOOPEN is low, DOUT is enabled and LOUT is disabled.

The active-low RST* input resets the internal registers to a balanced state. This pin should be held low for at least five frame rate clock cycles to ensure a complete reset.

The Data Field and Control Field are encoded depending on ED, FF, DAV*, CAV*, FLAG, FLAGSEL, M20SEL as well as two internally generated signals, O/E and ACCMSB.

When FLAGSEL is high, O/E is equivalent to FLAG. This is equivalent to adding an additional bit to the data field. When FLAGSEL is low, O/E alternates between high and low for data frames. This allows the link to perform more extensive error detection when the extra bit is unused.

ACCMSB is the sign of the previously transmitted data. This is used to determine which type of FF1 should be sent. When ACCMSB is low, FF1a is sent and when ACCMSB is high, FF1b is sent. This effectively drives the accumulated offset of transmitted bits back toward the balanced state.

Tx Phase-Locked Loop

The block diagram of the transmitter phase-locked loop is shown in Figure 11. It consists of a sequential frequency detector, loop filter, VCO, clock generation circuitry and a lock indicator. The outputs of the frequency detector pass through a charge pump filter that controls the center frequency of the VCO. These outputs also go to the VCO directly to effectively add a zero in the loop response. An external high-speed clock can be used instead of the VCO clock. This is accomplished by applying a high signal to EHCLKSEL and a differential clock to STRBIN.

One of four frequency bands may be selected by applying appropriate inputs to DIV0 and DIV1. The VCO or STRBIN frequency is divided by N, where N is 1, 2, 4 or 8 corresponding to the binary number represented by DIV1, DIV0. This divided version of the VCO clock or STRBIN is used as the serial rate clock and is available as a differential signal at the HCLK output.

A clock generator block creates all the clock signals required for the chip. Depending on M20SEL, STRBOUT is either HCLK/20 or HCLK/24. If MDFSEL is low, then

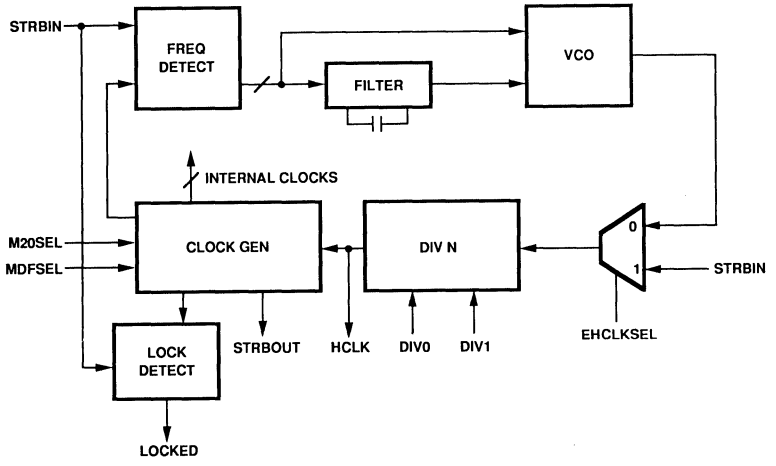


Figure 11. HDMP-1002 (Tx) Phase-Locked Loop.

STRBOUT is a phase-locked version of STRBIN. If MDFSEL is high, STRBOUT is twice the frequency of STRBIN.

The lock detect circuit samples STRBIN with phase shifted versions of STRBOUT. If the samples are not the proper values, the LOCKED signal goes low and stays low for at least two frames.

Rx Operation Principles

The HDMP-1004 (Rx) is monolithically implemented in a high performance 25 GHz f_t bipolar process. When properly configured, the Rx can accept 20B/24B CIMT line code frames, and then output parallel 16B/17B/20B/21B Data Words or 14B/18B Control Words. The Rx provides the following functions for link operation:

- Clock recovery
- Frame synchronization
- Data recovery
- Demultiplexing
- Frame decoding
- Frame error detection
- Link state control

Rx Encoding

Figure 6 shows a simplified block diagram of the receiver. The data path consists of an Input Select, an Input Sampler, a Frame Demultiplexer, a Coding Field (C-Field) Decoder, and a Data Field (D-Field) Decoder. An on-chip phase-locked loop (PLL) is used to extract timing reference from the serial input (DIN or LIN). The PLL includes a Phase-Frequency Detector, a Loop Filter, and a variable-frequency oscillator (VCO). All the Rx internal clock signals are generated from a Clock Generator. The Clock Generator can be driven either by the internal VCO or an external signal, TCLK, depending on the Clock Select configuration.

Integrated on the chip is a Link-Control State Machine for link status monitoring and link startup. Figure 12 shows the details of the Input Selector. The Input Selector chooses either the nominal serial data (DIN) or the loop back (LIN) signal for the Input Sampler's input. If loop back enable (LOOPEN) is asserted, the LIN input is selected. Included in the Input Selector is cable equalization circuitry. When coaxial cable is used as the transmission media, by setting EQEN=1 (enable equalization), the equalization circuitry is in the DIN signal path and provides fixed compensation for high-frequency cable loss.

The Data Field of the CIMT line code can be either 16-bits or 20-bits wide. The width selection for the Rx is made by setting the input pin M20SEL (Figure 6). If M20SEL = 1, then the Rx is configured to accept serial input with 20-bit data field (24 bits per frame). When M20SEL = 0, 16-bit data field is selected.

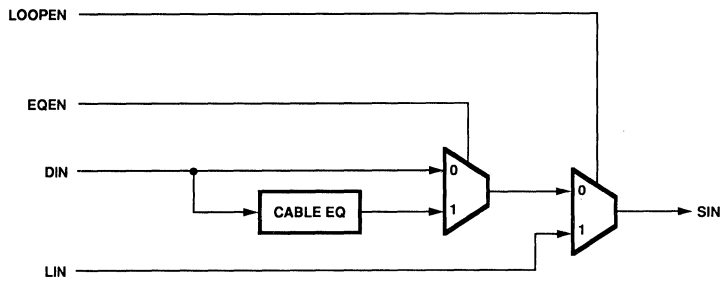


Figure 12. HDMP-1004 (Rx) Input Selector.

HDMP-1004 (Rx) Phase-Locked Loop

A more detailed block diagram for the Rx phase-locked loop (PLL) is shown in Figure 13. In the PLL, the phase of the serial input, SIN, is compared with synchronizing signals from the internal clock generator, using either a phase detector or a frequency detector. The frequency detector disable signal, FDIS, selects which detector to use. If synchronization in a link has yet to be established, the HDMP-1002 (Tx) should send out Fill Frame 0 (FF0) or Fill Frame 1 (FF1) to the remote Rx. By setting FDIS=0, the Rx uses the frequency detector to align its internal clock with the rising edge of FF0/FF1. Once this is accomplished, FDIS can be set to 1, then the PLL uses only the phase detector for synchronization adjustment and the Rx is ready to accept data. Due to the narrow frequency acquisition range of the phase detector, the frequency detector is used for internal frequency acquisition. The frequency detector, however, can only work with FF0 and FF1 and it then is necessary for the PLL to select the phase detector (by setting FDIS=1) before receiving any random data.

The output of the phase-frequency detector is externally available through pin PHI. An external clock source can also be used (through pin TCLK) by setting TCLKSEL=1. To broaden the usable frequency range of the chip, there is a programmable divider before the clock generator. The VCO or TCLK frequency can be divided by 1, 2, 4, 8 by setting DIV1, DIV0 = 00, 01, 10, 11 (see Operating Rate Tables).

HDMP-1004 (Rx) Decoding

In Figure 6, the frame demultiplexer de-serializes the recovered serial data from the Input Sampler, and outputs the resulting parallel data one frame at a time. Every frame is composed of a 16-bit or 20-bit

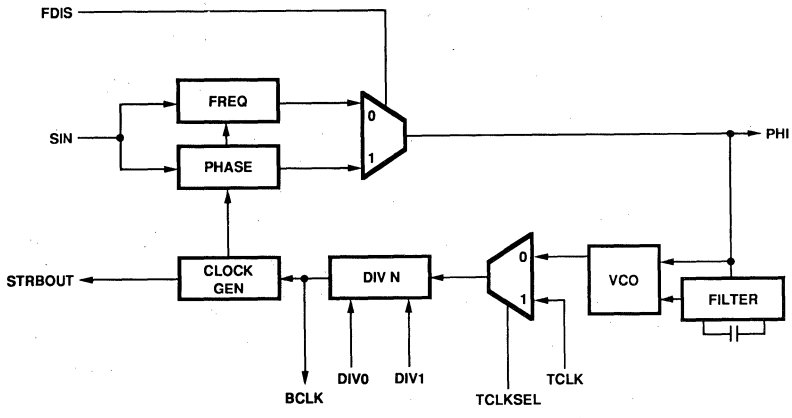


Figure 13. HDMP-1004 (Rx) Phase-Locked Loop.

Data Field (D-Field) and a 4-bit Coding Field (C-Field). The C-Field, C0-C3, together with the two center bits of the D-Field (D9 and D10 for 20 bit mode, D7 and D8 for 16 bit mode) are then decoded by the C-Field decoder to determine the content of the frame. The D-Field decoder is controlled by the outputs of the C-Field decoder. If an inverted Data Frame or Control Frame is detected, the D-Field decoder will automatically invert the D-Field data. If a Control Frame is detected, the D-Field decoder will shift the bottom half of the D-Field so that the outputs are at pin D_0 - D_{17} (if M20SEL = 1) or at pin D_0 - D_{13} (if M20SEL = 0). A data Frame is detected by the receiver when DAV = 1. A control Frame is detected by the receiver if CAV = 1. A Fill Frame is detected by the receiver if DAV = 0 and CAV = 0.

The C-Field decoder will set iERR = 1 when it detects an error. The internal error bit (iERR) is combined with the internal flag bit (iFLAG) and the flag-bit mode-select signal (FLAGSEL) to produce the externally available error (ERROR) and flag (FLAG) bits. If FLAGSEL = 1, the FLAG bit can be used as an extra data bit.

- ERROR=iERR.
- FLAG=iFLAG.
- If a Fill Frame is detected, then FLAG=0.
- If a Control Frame is detected, FLAG should be ignored.

If FLAGSEL = 0, the serial input is assumed to consist of alternating even frames (iFLAG = 0) and odd frames (iFLAG = 1).

- If iERR=1, then ERROR=1.
- If a Fill Frame is detected, then FLAG=0.
- If a Data Frame is detected, then FLAG=iFLAG, and iFLAG should alternate between 0 and 1, starting with 0 and ending with 1; otherwise, ERROR=1.
- If a Control Frame is detected, then FLAG automatically alternates between 0 and 1, starting with 0.

The even or odd feature allows a 32/40-bit wide data word to be transmitted through the link. A 2:1 multiplexer and a 1:2 demultiplexer are required. FLAG is used to synchronize the even and odd frames. Note, both Data and Control Frames can be transmitted as even/odd pairs, but only Data Frames can be detected for out of order errors.

HDMP-1004 (Rx) Link-Control State Machine Operation Principle

The link-control state machine (SMC) on the Rx chip provides a link handshake protocol enabling the duplex link to transition from frequency acquisition and training mode into data mode.

The HDMP-1000 Tx/Rx link uses an explicit frequency acquisition mode at startup that operates on a square-wave training sequence. This makes it possible to use a VCO with a very wide tuning range yet avoid the harmonic false lock problems associated with other circuits of this type.

Using the SMC, a full duplex data channel can be implemented without additional controller or hardware.

The State Machine Handshake Protocol

Figure 1 shows a simplified block diagram of the HDMP-1000 data channel configured for full duplex operation. Two HDMP-1000 chipsets are required to perform the handshake in parallel. There are three states that the link must go through to complete the link startup process:

State 0: Frequency Acquisition

State 1: Waiting for Peer

State 2: Sending Data

Each side of the link decides which of the three states that it should be in. The decision is based on its own memory and the type of frame that it is currently receiving from the other side of the link.

Considering only the local port of the link, we have a transmitter (Tx), a receiver (Rx), and a state machine controller (SMC). In practice, the SMC entity, although logically distinct, is implemented on the same die as the Rx chip. The SMC monitors the data frame status indicators (ERROR, DAV, CAV, FF) from the Rx, and is able to force (or

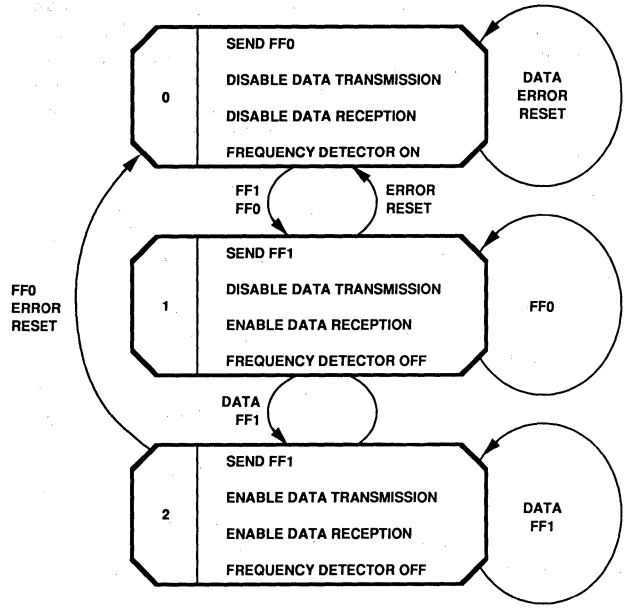


Figure 14. HDMP-1004 (Rx) State Machine State Diagram.

control) various characteristics of the Tx and the Rx chips. The Tx chip has the following controllable features:

- It can be forced to send a Fill Frame using the ED input.
- The type of Fill Frame sent can be controlled using the FF input.

The Rx Chip has the following controllable features:

- It can be in Frequency acquisition or Phase-lock/Data reception mode depending on the state of the FDIS input.
- It can be enabled for data reception or set in a mode in which data frames are ignored depending on the ACTIVE input.

The Rx chip can distinguish between the various types of frames. It can communicate the frame type to the SMC. The various frame types are:

- Fill Frame 0, (FF0)
- Fill Frame 1 a/b, (FF1)
- Data/Control frames (Data)
- Error frames (ERROR)

The SMC can be reset by either the SMCRST0* or SMCRST1* inputs. Usually one of these inputs is used for power-on reset, and the other is connected to the Tx LOCKED output.

This holds the SMC in state 0 until the transmitter PLL has locked.

Figure 14 shows the state diagram of the SMC. The SMC is debounced by allowing state transitions to be made only after at least 2 consecutive frames give the same indication. This prevents single bit errors from causing false state transitions. In addition to this debouncing mechanism, when two consecutive ERROR or Resets occur, a timer is enabled forcing the SMC into state zero for 128 frames. Any transition out of this initial state can only occur after the link has been error-free for 128 frames. This prevents false transitions from being made during the bit-slipping that occurs in the initial frequency acquisition of both the Tx and Rx PLLs.

When the local port is in State 0, it is in the reset state. Both local Tx and Rx parallel interfaces are disabled. The local Tx transmits FF0 continuously, and the Rx PLL is in the frequency detection mode. When the local Rx is phase-locked to the remote Tx it transitions to State 1. The local Tx transmits FF1 to acknowledge the phase-locked condition (its parallel input is still disabled). The local Rx PLL is in the phase detection mode and its parallel output is enabled. When in State 2, the two-way synchronization between the local port and the remote port is established. Both the local Tx and Rx parallel interfaces are enabled, and the local Rx PLL is in the phase detection mode. Parallel data can be sent by the local Tx, and at the same time, received by the local Rx.

The Rx chip has the state machine logic built in. The SMC has two status outputs, STAT0 and STAT1, that control the various features of the two chips depending on the current state.

SMC Output (STAT0 and STAT1) at Current Link State

State	STAT0	STAT1
0	0	0
1	0	1
2	1	1

The Tx inputs that need to be controlled are FF and ED. The Rx inputs that need to be controlled are FDIS and ACTIVE. To control the chips as shown in the state diagram of Figure 14, these inputs need to be driven as follows:

State	Tx FF	Tx ED	Rx FDIS	Rx ACTIVE
0	0	0	0	0
1	1	0	1	1
2	1	1	1	1

To control the link as shown above the following interchip connections must be made (Figure 15):

- Tx FF is driven by STAT1
- Tx ED is driven by STAT0
- Rx FDIS is driven by STAT1
- Rx ACTIVE is driven by STAT1
- Tx RST and Rx SMCRST0 are driven by a power-on, or user, reset circuit.

Link Configuration Examples

This section shows some application examples using the HDMP-1000 chipset. Refer to Section 2 (I/O Definition) for detailed circuit-level interconnection. For example, the chipset's ECL output drivers have weak driving power; hence, external buffers are required for large loading.

Figure 15 is the schematic for a full-duplex port. The network start-up protocol is provided by the Rx internal state-machine controller, and is transparent to the host. The handshaking between the host and the chipset is provided by the RFD and LINKRDY* signals. The host interface registers are clocked by the falling edges of the STRBOUT from the Tx and the Rx. The user has to make sure that M20SEL, FLAGSEL, DIV0, and DIV1 have the same setting on both the Tx and Rx. The word width of the parallel data from the host can be either 16 bits if M20SEL = 0, or 20 bits if M20SEL=1. Also, the FLAG bit can be used as an additional bit by setting FLAGSEL = 1. In the last case, the parallel data word width is either 17 bits or 21 bits. The local loopback test can be enabled by setting LOOPEN high.

Figure 16 shows how to use the FLAG bit and MDFSEL to transfer parallel data with 36-bit or 40-bit word width. Each data word is multiplexed and carried by two consecutive CIMT frames called even and odd frames. The FLAGSEL is set to high, and the FLAG bit is used to designate the even/odd frame. For the Tx, the MDFSEL is set to high so that the frequency of STRBOUT is twice that of STRBIN. The flag signal to the Tx is generated from STRBIN and STRBOUT. The Tx interface registers are clocked by the Tx FLAG signal. On the Rx side, the FLAG output is retimed by STRBOUT to generate RCLK, which is used to demultiplex the data output. Note that the Rx interface registers for LINKRDY*, ERROR, DAV*, CAV*, and FF are clocked by STRBOUT instead of RCLK; this is due to the fact that the FLAG is reset to "0" when receiving FF0.

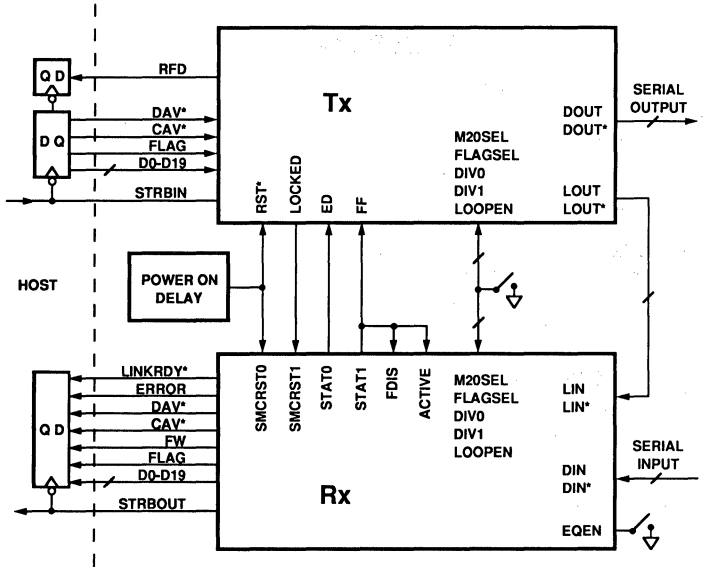


Figure 15. A Full-Duplex Port.

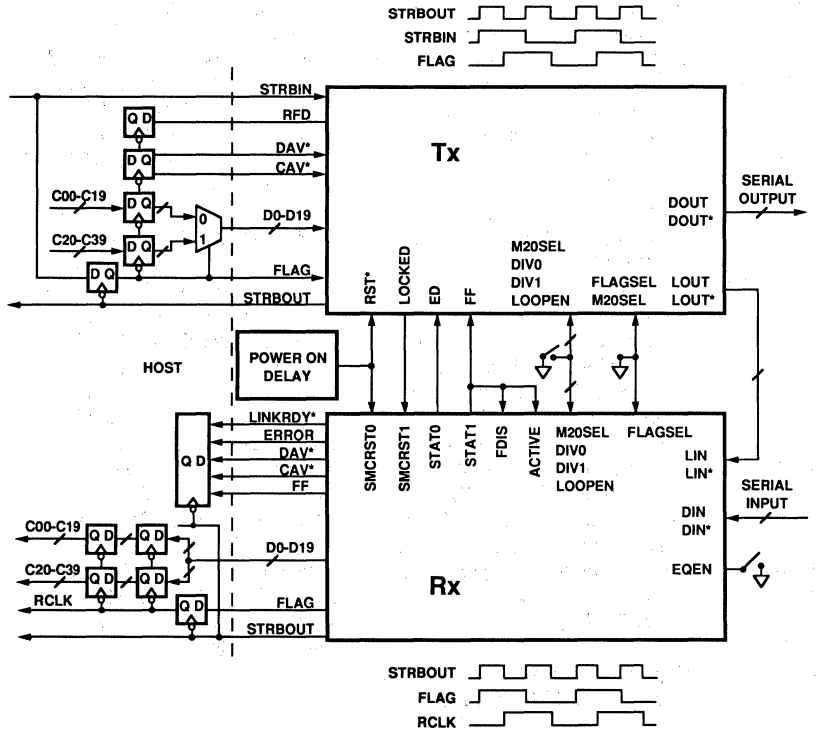


Figure 16. A Full-Duplex Double-Frame Port.

Although the HDMP-1000 chipset is designed for full-duplex applications, it is possible to configure the chipset for simplex applications as shown in Figure 17. Although the Tx has no knowledge of the status of the remote Rx, the Tx host can periodically allocate a time slot to transmit FF1. This is shown as a negative pulse to the Tx ED input in Figure 17. If the remote Rx is unlocked, it can wait for the next sequence of FF1 to regain synchronization. The length of each FF1 sequence must be longer than the Rx frequency acquisition time (approximately 2 msec). Note that the Rx internal state-machine controller can also be used in this simplex application; no additional controller is necessary.

Surface Mount Assembly Recommendations

The package is designed to be surface mounted with the lid facing the board (lid acts as bottom of the package or pin view facing the board). It is recommended that the leads be formed into a "Gull-Wing" configuration prior to surface mounting. The recommended package stand-off (distance between "bottom" of package to the board surface) is 30 mils. It is also recommended that the leads be solder (Sn/Pb) coated prior to surface mounting. The lead material is Alloy 42. Note: Packages are shipped with unformed leads in carriers.

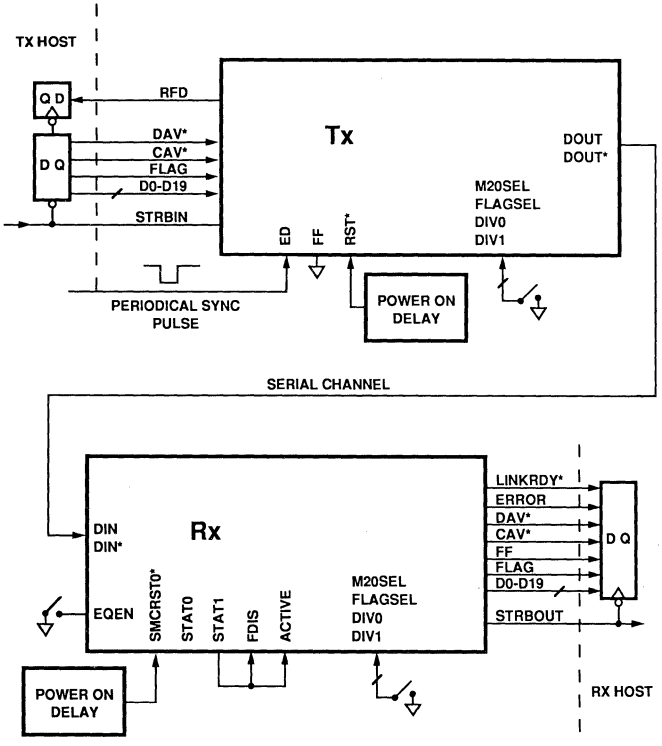
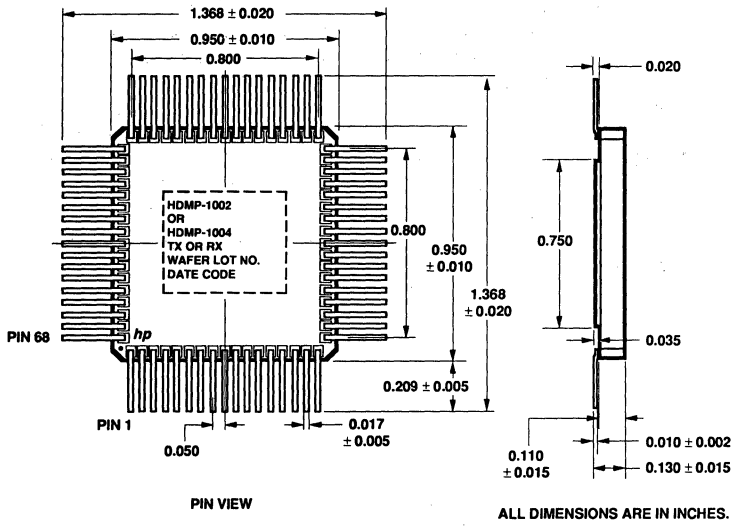


Figure 17. Simplex Configuration.

Outline

68 Lead Ceramic Quad Flatpack



Evaluation Board Ordering Information

A Gigabit Rate Transmit Receive Chipset Evaluation Board may be ordered through your local HP Components Representative or authorized HP Components distributor.

Designer Kit

Part Number	Kit Description
HDMP-100K	Evaluation board for the Gigabit Rate Transmit Receive Chipset, and literature

HEWLETT PACKARD

Decision Circuit (Comparator/D-FF)

Technical Data

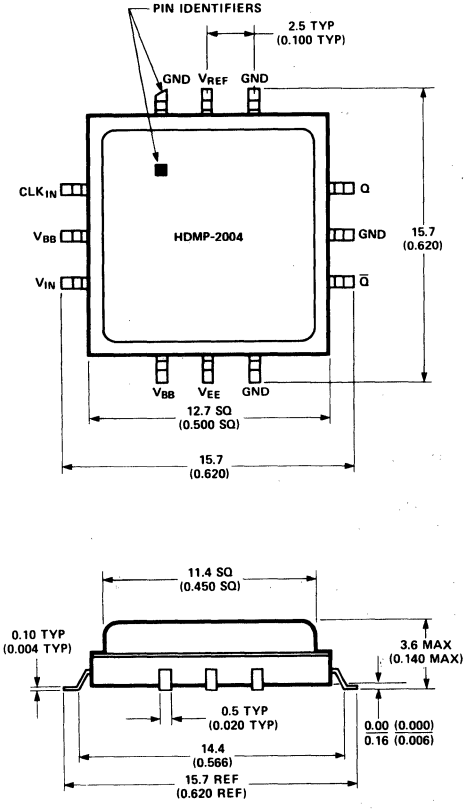
HDMP-2003
HDMP-2004

Features

- **Silicon Bipolar Technology**
- **ECL Levels**
- **Operational to 1.5 GBit Input Rates**
- **Single -5.2 V Power Supply**
- **Operational over Full Temperature Range -55°C to +125°C**
- **Highly Reliable HBIC Hermetic Surface Mount Package**
- **Low Power Dissipation ≤0.5 W**

Description/Applications

The HDMP-2003, and -2004 Decision Circuits are high speed/high sensitivity digital waveform regeneration modules consisting of a comparator, an edge-triggered D-flip-flop, and a 50 ohm output driver. They sample GBit data in both time and amplitude, and decide whether a "1" or a "0" exists relative to an internal V_{BB} or external DC reference voltage, thus regenerating a retimed, less noisy digital waveform. They are recommended for use as the data regeneration circuits in high speed fiber optics communication receivers. Other applications include Digital Radio communications systems, High Speed Computer Interconnect Systems, Instrumentation, and other Data Recovery Systems.



NOTE: BOTTOM OF PACKAGE IS PRIMARY GROUND CONTACT.
ALL DIMENSIONS IN MILLIMETERS (INCHES).

OUTLINE HBIC-0512
WEIGHT (TYPICAL): 1.15 GRAMS
(HDMP-2003, HDMP-2004)

Absolute Maximum Ratings

Symbols	Parameters	Units	Ratings
V_{EE}	Supply Voltage	V	-6.0
T_{STG}	Storage Temperature	°C	-60 to +150
T_C	Operating Case Temperature	°C	-55 to +125
V_{IN}	Input Voltage	V	+2 pk-pk

Operation in excess of these conditions may result in permanent damage to the device.

Operating Specifications

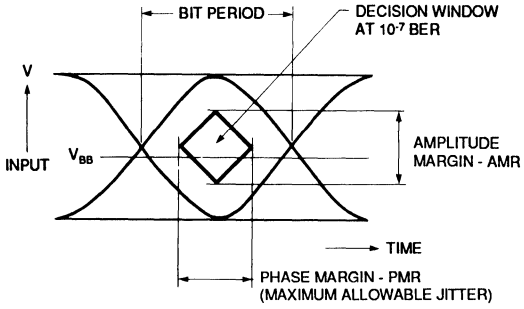
Symbols	Parameters	Units	HDMP-2003		HDMP-2004	
			Min.	Typ.	Min.	Typ.
DR	Input Data Rate	GBits/sec	2.0	2.4	2.8	
AMR[1]	Amplitude Margin	mV	100	120	70	130
PMR[1]	Phase Margin	psec	250	300	170	240
VTM	Threshold Margin	mV		40		40
t_r[2]	Rise Time	psec		110		120
t_f[2]	Fall Time	psec		110		90
V_O	pk-pk Output Voltage	Volts		0.6		0.6
I_{EE}	Supply Current	mA		70		60

Test Conditions:
V_{EE} = -5.2 V
CLK: HDMP-2003 = 2.0 GHz, 400 mV pk-pk
HDMP-2004 = 2.8 GHz, 400 mV pk-pk

V_{IN} : HDMP-2003 = 2.0 GHz, 200 mV pk-pk
HDMP-2004 = 2.8 GHz, 200 mV pk-pk

2^{15}-1 Pseudo Random Bit Sequence (PRBS)
CLK, V_{IN}, and Output are at 50 Ohms AC coupled
T_A = 25°C

Notes:
1. See Figure 1A.
2. 10% to 90% (see Figure B).



NOTE:
VTM = THE MINIMUM DIFFERENCE BETWEEN THE INTERNAL REFERENCE VOLTAGE AND THE NEAREST EDGE OF THE AMPLITUDE MARGIN WINDOW.

Figure 1a. Decision Window Definition.

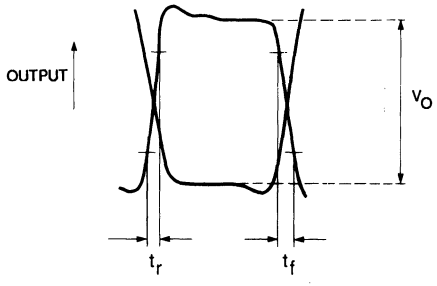


Figure 1b. Output Waveform Definition.

TYPICAL RETURN LOSS AT T = 25°C FOR HDMP-2003

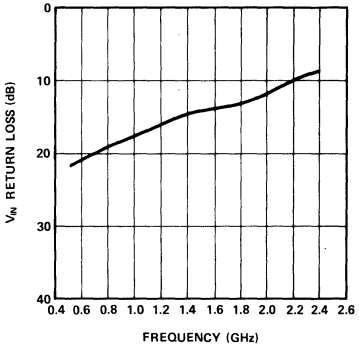


Figure 2a.

TYPICAL CASE TEMPERATURE PERFORMANCE FOR HDMP-2003

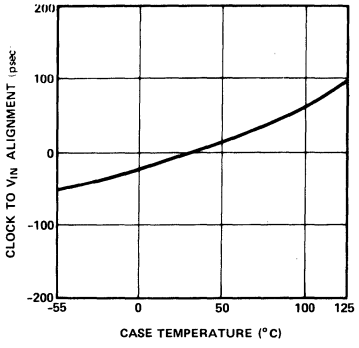


Figure 2b.

TYPICAL RETURN LOSS AT T = 25°C
FOR HDMP-2003

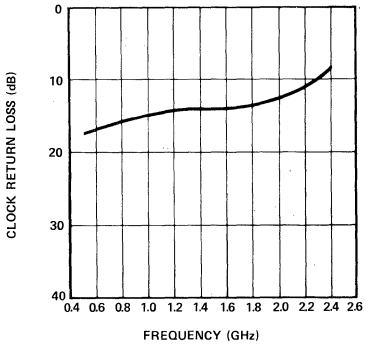


Figure 2c.

TYPICAL CASE TEMPERATURE PERFORMANCE
FOR HDMP-2003

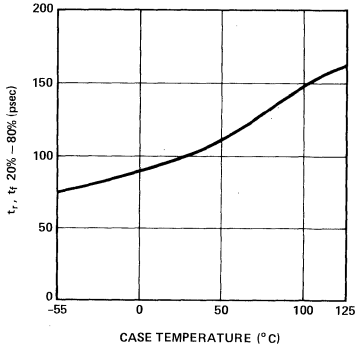


Figure 2d.

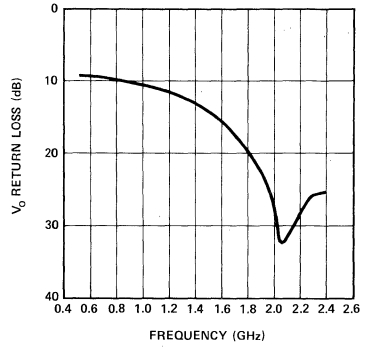


Figure 2e.

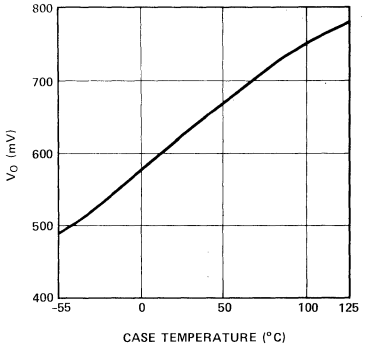


Figure 2f.

TYPICAL RETURN LOSS AT T = 25°C
FOR HDMP-2004

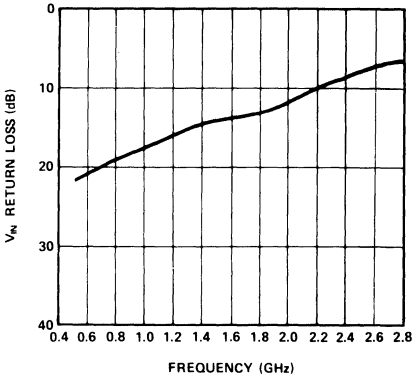


Figure 3a.

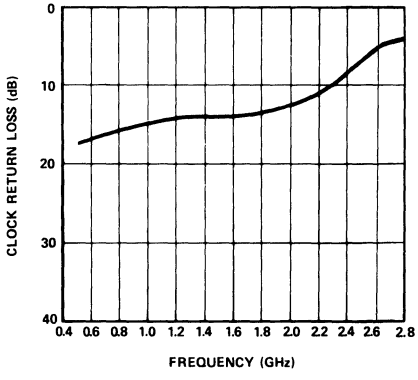


Figure 3b.

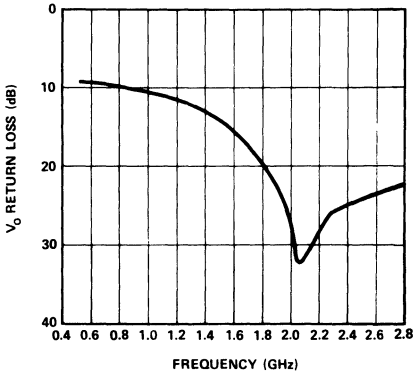


Figure 3c.

TYPICAL CASE TEMPERATURE PERFORMANCE
FOR HDMP-2004

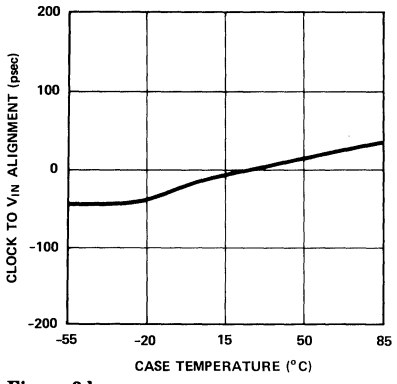


Figure 3d.

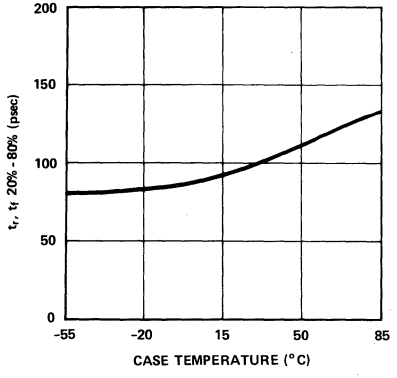


Figure 3e.

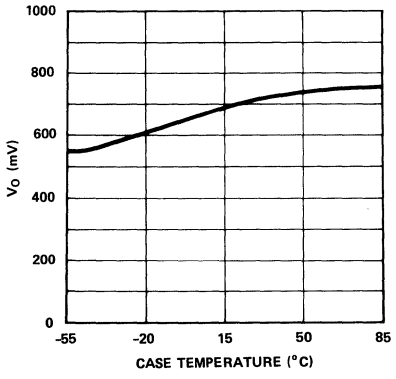


Figure 3f.

FIBER OPTICS

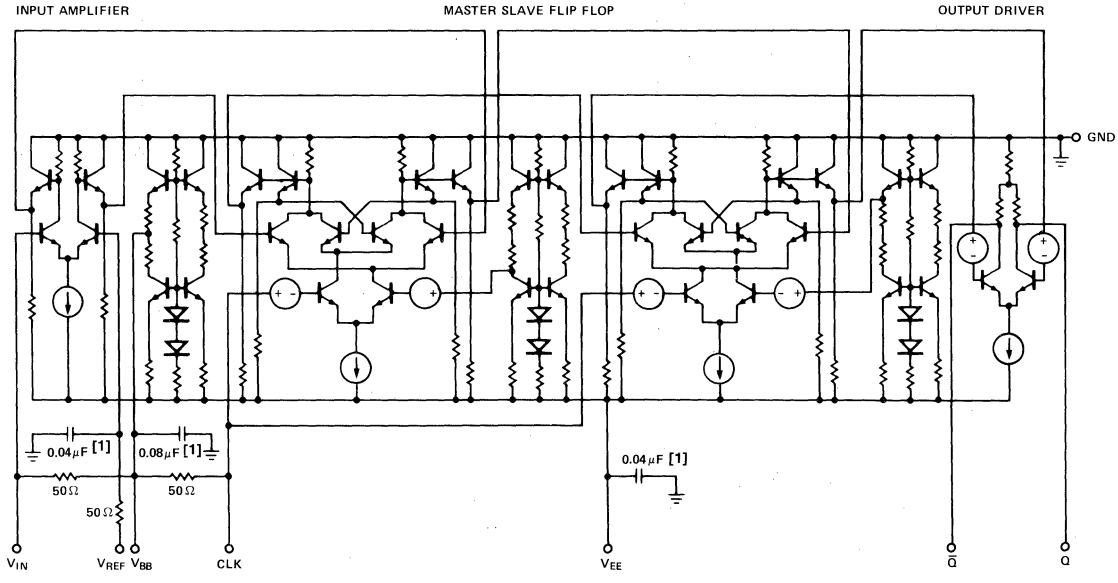
Theory of Operation

The HDMP-2003 and -2004 consist of three major sections – an input comparator amplifier, a master-slave flip-flop, and an output driver (see Figure 4). During operations, a distorted waveform enters the comparator via V_{IN}, and is compared to a reference DC voltage supplied at V_{REF}. The output of the D-flip-flop is next fed into the D-flip-flop section where a clock input triggers the master/slave action that synchronizes the signal with the rising edge of the clock. The amplified and retimed signal then exits the module through the driver section.

Under normal operating conditions, V_{REF} is connected to V_{BB}, and V_{IN} and CLK are externally capacitively coupled (see Figure 4). The internal termination resistors also form a biasing network which eliminate the need for additional external biasing. The integrity of the input amplifier is determined by the Amplitude Margin (AMR), which is defined by the range of V_{REF} at which the Bit Error Rate (BER) is less than 10^{-7}. For values inside this range, the BER falls sharply to produce virtually error free operation (see Figures 6 and 8).

The performance of the retiming flip-flop is determined by the Phase Margin (PMR) which is defined by the range of deviation of clock alignment relative to the input signal at a BER less than 10^{-7}. Again, the BER falls sharply inside this range (see Figure 7 and 9). Once the clock to data alignment is set, the internal compensation circuitry will track this alignment over temperature (see Figures 2d and 3d).

The output driver section is characterized by the peak-to-peak output voltage and the 10% to 90% rise and fall times relative to the levels at the center of the output bit. This driver also has the advantage of driving directly into 50 ohms with or without a coupling capacitor, or directly into ECL (see Figure 10). The excellent line matching also dampens pulse reflections typical for many high frequency circuit interconnections.



[1]HDMP-2004 only.

Figure 4. Circuit Schematic, HDMP-2003 and HDMP-2004.

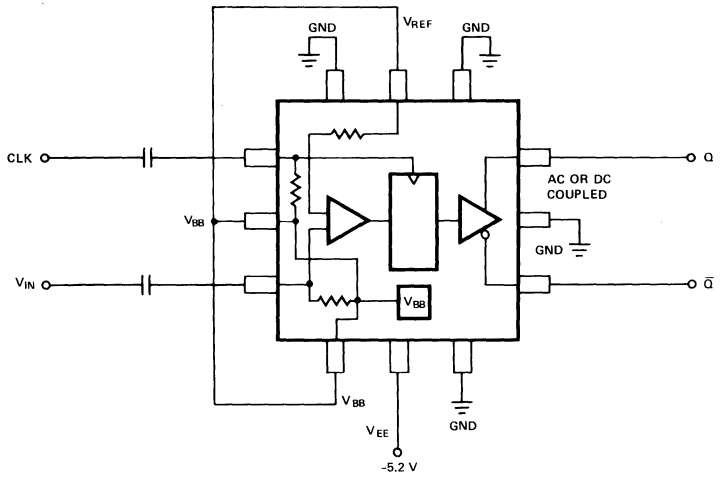


Figure 5. Typical Interfacing Diagram (Top View); HDMP-2003, HDMP-2004.

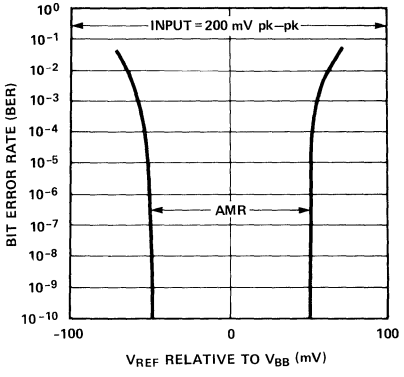


Figure 6. Amplitude Margin (AMR), HDMP-2003.

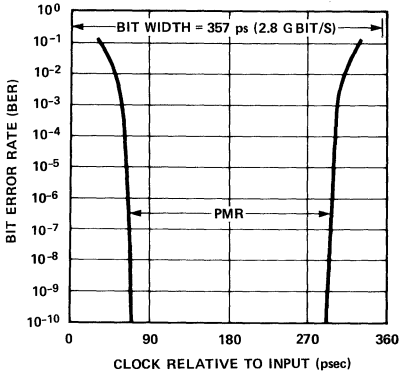


Figure 7. Phase Margin (PMR), HDMP-2003.

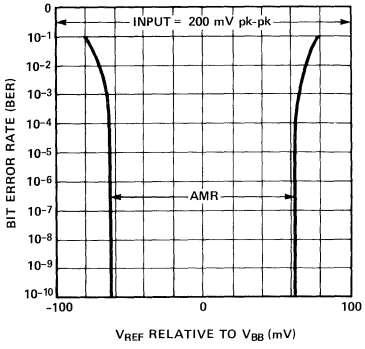


Figure 8. Amplitude Margin (AMR), HDMP-2004.

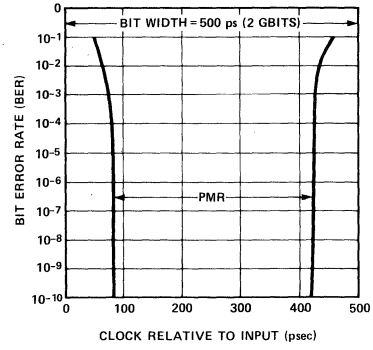


Figure 9. Phase Margin (PMR), HDMP-2004.

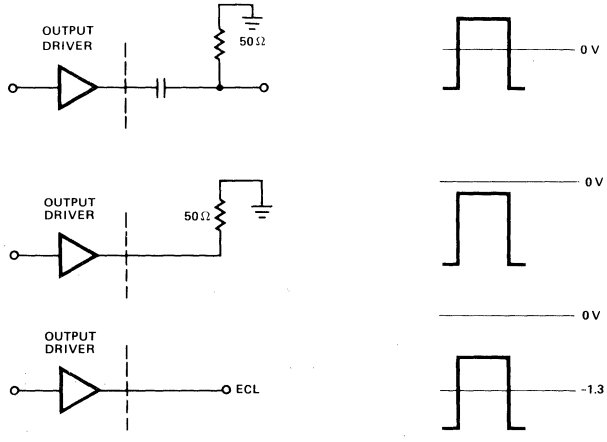


Figure 10. Output with Various Loading Conditions, HDMP-2003, HDMP-2004.

Testing

The characterization test set-up for the HDMP-2003 and -2004 is shown in Figure 11. The input signal is provided by a pseudo random bit sequence (PRBS) generator set at the operating frequency. To insure that the DUT is correctly evaluated, the square wave output from the generator (A) is fed into a high performance AGC amplifier (HAMP-5001), which emulates a typical system. The AGC amplifier output (B), and the sinusoidal clock signals (C) are applied to the DUT. The outputs Q and $\overline{Q}$ are measured with the BER receiver and a sampling scope (D).

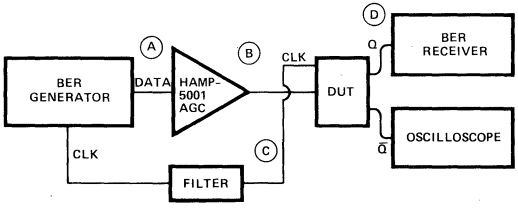
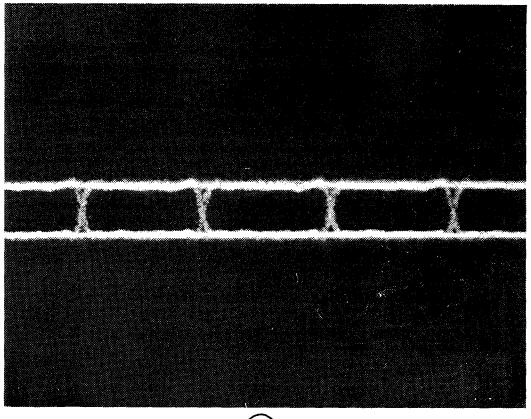
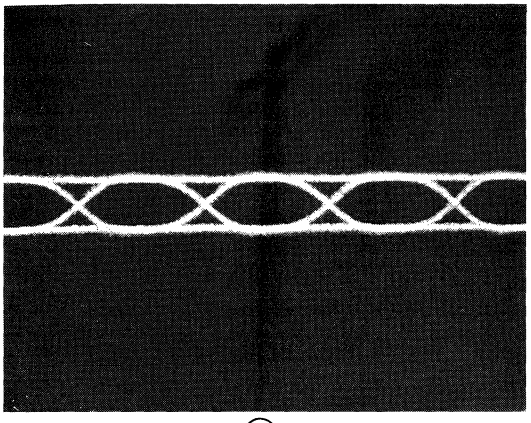


Figure 11. Test Setup

HDMP-2003

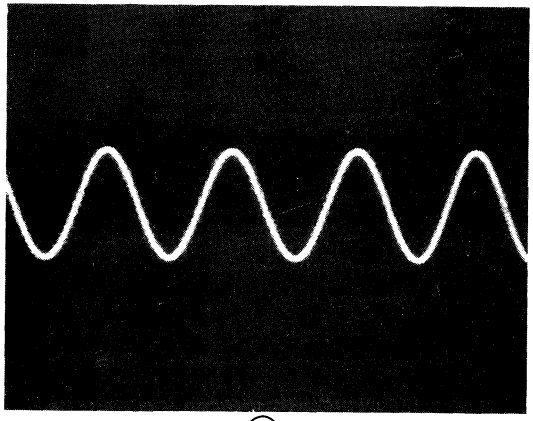


(A)

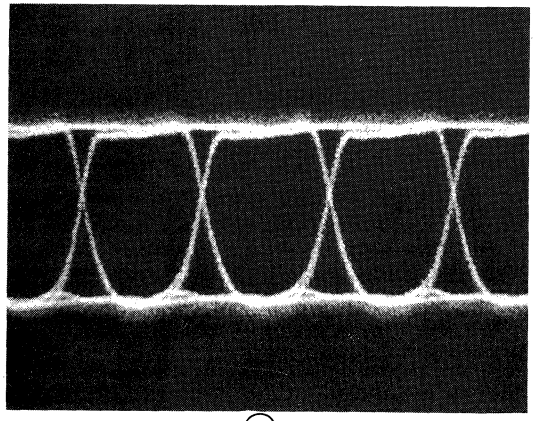


(B)

HDMP-2003 continued

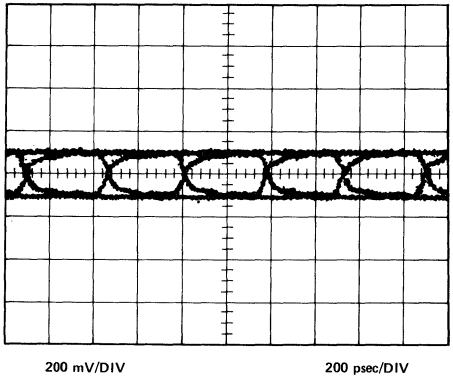


C

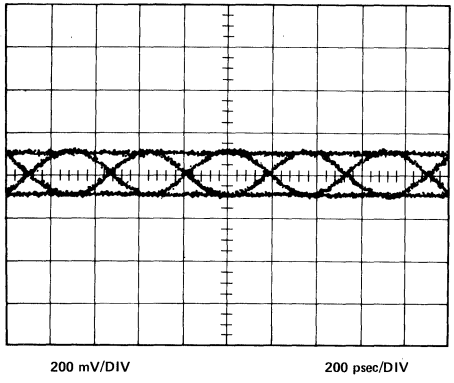


D

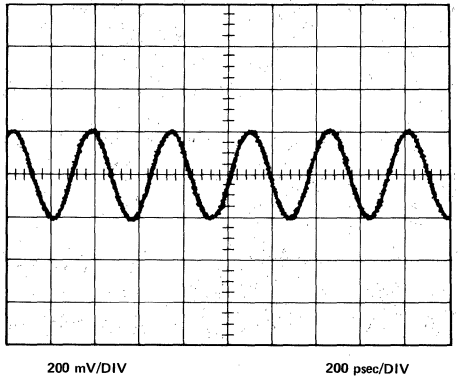
HDMP-2004



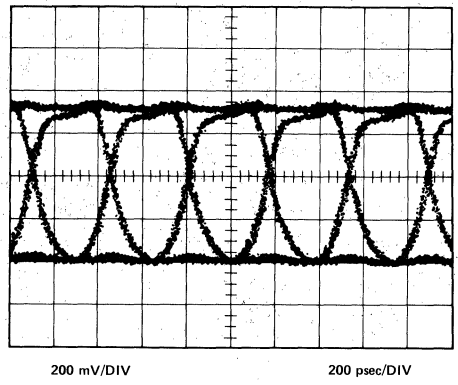
A



B



C



D

Figure 12. Characterization Test Set-up.

Handling and Mounting Procedures for Hermetic, Base is Circuit (HBIC-0512 Packages

1. Storage

Under normal circumstances, storage of the HBIC packages in HP supplied containers is sufficient. However, in particularly dusty or chemically hazardous environments, storage in a clean, inert atmosphere is advised to maintain solderability.

2. Handling

As with any multi-leaded surface mount package, care must be taken during handling of the HBIC package not to cause deformation of the leads. The planarity of the leads to each other and to the bottom of the package must be maintained for successful mounting.

The HBIC package can be handled with tweezers or other tools by clamping the package around the lid, or with vacuum systems on the top of the lid.

3. Grounding

The prime ground contact of the HBIC package is its bottom (with unused leads and the lid as secondary ground points). For optimum circuit performance, the bottom of the package must be soldered to a ground pad on the substrate (PC board or ceramic). This ground pad should be the size of the package bottom and have several plated thru holes to the substrate's ground plane, giving the package a low inductance contact to system ground.

4. Mounting

Solder reflow is the suggested method of attaching HBIC packages onto substrates. The recommended solder is 62% Sn, 36% Pb, 2% Ag, with an RMA flux. This solder paste can be dispensed (for packages with wide lead spacing) or screen printed onto the substrate. The use of a solder mask on the substrate is also recommended. Solder reflow can then be achieved by infrared heating or vapor-phase heating. The packages must not be exposed to more than 260°C for 20 seconds.

Conductive epoxy could be used for mounting the HBIC packages, however, care must be taken due to the potential problem of silver migration between the leads and the ground pad under the package.

Wave soldering is not recommended due to the metal lid and the need for solder under the package base.

HEWLETT PACKARD

Silicon Bipolar High Speed Decision Circuit with 1.5 GBit Operation (Comparator/D-FF)

Technical Data

HDMP-2006

Features

- **High Performance Low Bit Error Rate (BER)**
- **Operational to >1.5 Gbit Data Rates**
- **ECL Compatible I/O**
- **Requires only a 100 mV Minimum Input Signal**
- **Single -5.2 V Power Supply**
- **Hermetic Glass Metal SOIC Package**
- **Low Power Dissipation < 0.5W**

Applications

- **SONET Fiber Optic Systems**
- **Provides Excellent 622 Mb OC-12 Performance**
- **High Speed Digital Telecom Systems**
- **High Speed Datacomm and Computer Interconnect to 1.5 Gb**
- **Digital Television Studio Systems**
- **Instrumentation-- Comparator, DFF**

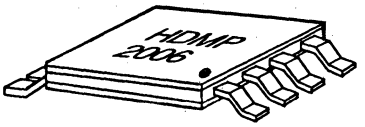
Description

The HDMP-2006 Decision Circuit is a high speed/ high sensitivity digital waveform regenerator IC consisting of a comparator, an edge triggered D-type flip-flop, and a 50 Ohm output driver. The device is fabricated on Hewlett-Packard's >13 GHz f_T silicon bipolar IC process. The HDMP-2006 samples input data at rates up to 1.5 Gb/sec in both time and amplitude, and decides whether data is a "1" or "0" relative to the sampling level V_{REF} which can be tied to the internally generated V_{BB} or externally supplied .

The HDMP-2006 is ideally suited for data regeneration applications in high speed fiber optic communication systems such as SONET standard systems.

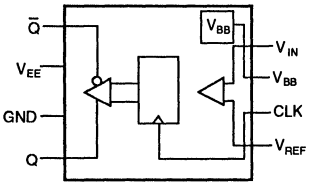
The HDMP-2006 is supplied in an 8 lead hermetic package with gold plated Kovar (ASTM F-15 alloy) cover, base, and leads.

SOIC8 Package Outline



Functional Block Diagram

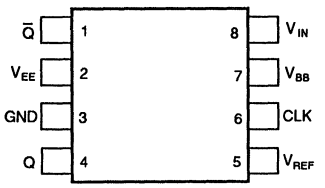
Top View



NOTE:
BOTTOM OF PACKAGE IS AT V_{EE} POTENTIAL (-5.2 V NOMINAL). TOP OF PACKAGE IS ISOLATED AND MAY BE GROUNDED BY USER.

Package Lead Code Identification

Top View



Absolute Maximum Ratings, T_A = 25 °C*

Symbol	Parameter	Units	Max.
V_{EE}	Supply Voltage	Volts	-6.0
V_{IN}	Signal Input Voltage	Volts DC Pk to Pk	2
T_{op}	Ambient Operating Temperature	°C	+100
T_{stg}	Storage Temperature	°C	-60 to +150
T_{max}	Maximum Assembly Temperature (for 60 seconds maximum)	°C	+300

* Operation in excess of any of these conditions may result in permanent damage to this device.

ESD Sensitivity
These high performance devices are ESD sensitive (Class 2).
Proper precautions should be used when handling these devices

DC Electrical Specifications, T_A = 25 °C

Symbol	Parameter	Units	HDMP-2006		
			Min.	Typ.	Max.
V_{EE}	Supply Voltage	V	-5.46	-5.2	-4.94
I_{EE}	Supply Current	mA		70	90
V_{BB}	Reference Voltage	V		-1.3	
θ_{JC}	Thermal Resistance (Die to Case)	°C/W		50	

AC Electrical Specifications, T_A = 25 °C

CLK = 1 GHz 400 mV p-p, V_{IN} = 200 mV p-p @ 1 GHz @ V_{EE} = -5.2V
Input data test sequence = PRBS @ 2^{23}-1
When tested per Test Circuit (Figures 1 and 2) in test board per layout of Figure 3.

Symbol	Parameter	Units	HDMP-2006		
			Min.	Typ.	Max.
AMR	Amplitude Margin [1]	mV	100	130	
PMR	Phase Margin [1]	ps	700	800	
V_{TM}	Threshold Voltage	mV		55	
t_r	Rise time (10% to 90%) [2]	ps			200
t_f	Fall time (90% to 10%) [2]	ps			200
V_{OUT}	Output Voltage Swing (pk to pk)	V	0.6	0.8	

Notes: 1 AMR is measured by varying V_{REF} relative to V_{IN}. PMR is measured similarly by varying the clock phase relative to the data. AMR and PMR are defined in Figure 6.
2. t_r and t_f are defined in Figure 7.

Test Circuits

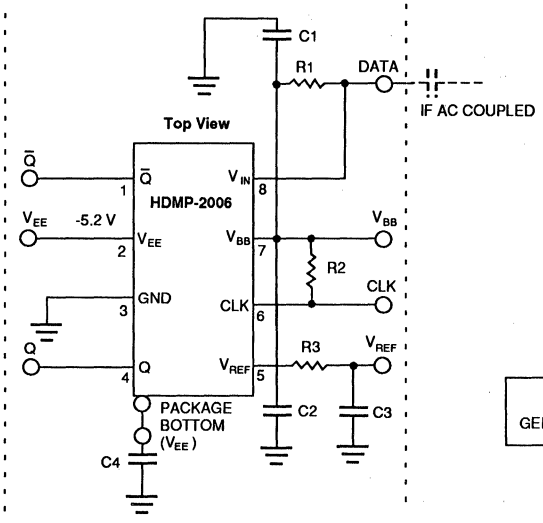


Figure 1. DUT Interface Circuitry

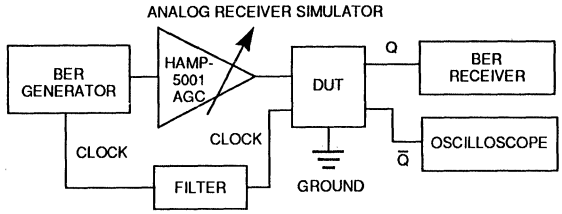
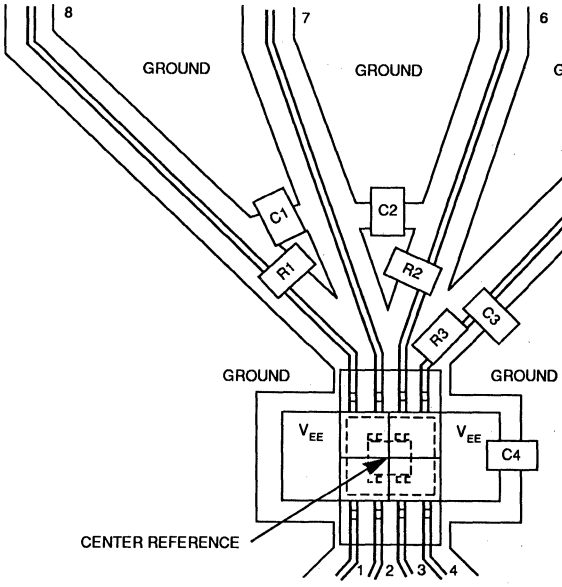


Figure 2. Device Test Setup



Component Values and Relative Positions for Chip Resistors and Capacitors in Test Circuit of Figure 3.

Component	Value	Units	Relative X [1]	Relative Y[1]
C1	39	nF	-0.22	0.49
C2	39	nF	-0.01	0.48
R1	51	Ohms	-0.20	0.33
R2	51	Ohms	0.04	0.35
C3	39	nF	0.18	0.31
R3	51	Ohms	0.07	0.22
C4	39	nF	0.22	0.00

Note 1: (Inches) relative to device center

Figure 3. Physical Test Circuit Layout and Component Information

Performance Curves

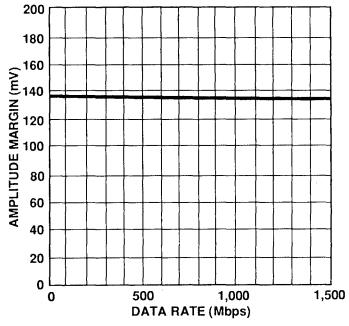


Figure 4. Input Eye Amplitude Margin

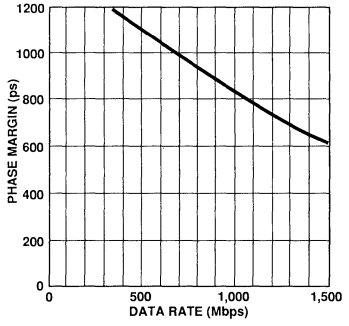
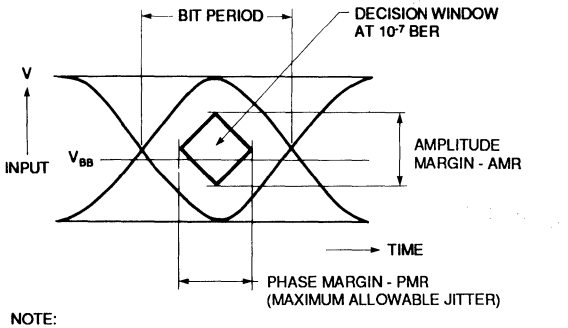


Figure 5. Input Eye Phase Margin



NOTE:
VTM = THE MINIMUM DIFFERENCE BETWEEN THE INTERNAL REFERENCE VOLTAGE AND THE NEAREST EDGE OF THE AMPLITUDE MARGIN WINDOW.

Figure 6. Eye Diagram Performance Measures

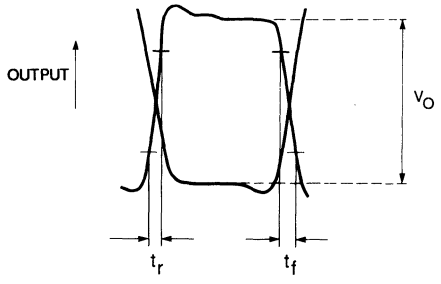


Figure 7. Output Waveform Definitions

Eye Performance Measures

HP specifies the performance of this decision circuit by measuring the input Amplitude Margin (AMR) and input Phase Margin (PMR) which will produce a Bit Error Rate (BER) of 1E-07 or less.This is accomplished (see Figure 2) by setting the input psuedorandom signal amplitude from the BER Test Set (BERT)at a constant level and varying the reference signal V_{REF} (externallly connected). In a similar manner the clock to data phase is varied. The input signal from the BERT is band limited by the HAMP-5001 which is an AGC circuit simulating the analog performance of a fiber optic receiver. The measurements are made independently; first by varying phase and second amplitude. In this way the center useable portion of the eye (Figure 6) is determined. The vertices of the diamond pattern are the values of amplitude and phase at which the BER exceeds 1E-07. This measurement simulates typical system conditions and provides both the amplitude and phase (timing) limits. The measurement provides an accurate determination of Gaussian noise superimposed on the data signal and is minimally effected by switching noise.

Ambiguity level can also be used to accurately measure the amplitude window of the eye diagram for this class of devices. A full ambiguity level test uses the PRBS output signal of the BERT with a precision attenuator (or AGC) in series with the input of the device. This requires a precision attenuator which has a constant level of noise independent of attenuation level and bandwidth.

Because of the difficulty in accurately doing the ambiguity test and since the AMR and PMR tests provide more operationally relevant data, HP does not specify ambiguity level.

Circuit Schematic

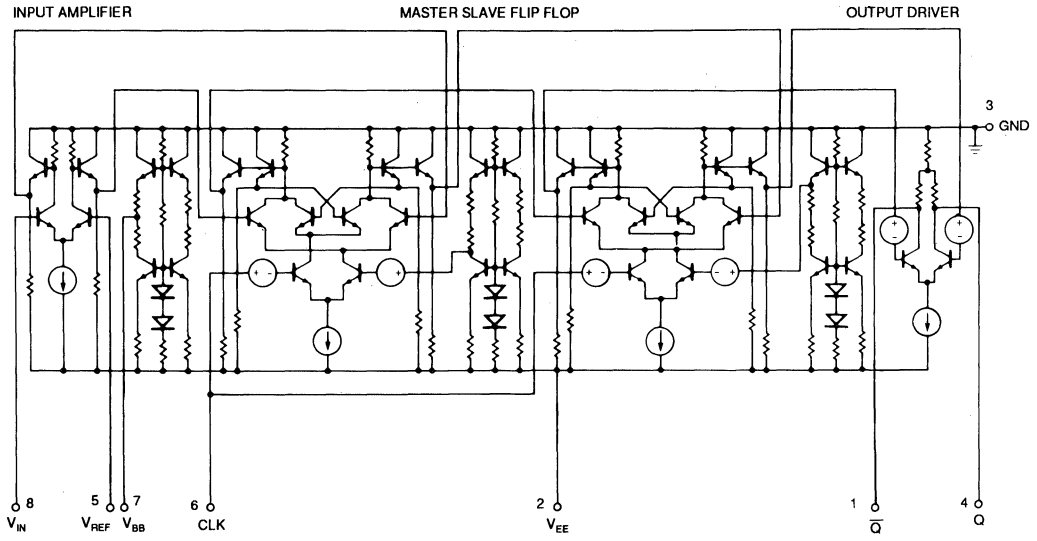


Figure 8. HDMP-2006 Circuit Schematic

Theory of Operation

The HDMP-2006 consists of three major sections - an input comparator amplifier, a master slave flip-flop, and an output driver (see Figure 8). During operation, a distorted waveform enters the comparator via V_{IN}, and is compared to a reference voltage V_{REF}. The output of the comparator is next fed to a D-type flip-flop section where the clock input triggers the master-slave action that synchronizes the signal with the rising edge of the clock. The amplified and retimed signal then exits the module through the driver section. Direct coupled inputs will work with ECL levels.

The output driver section provides the peak-to-peak voltage with the 10 to 90 % rise and fall times relative to the levels at the center of the output waveform (Figure 7). Typical interface circuit diagrams for the HDMP-2006 are given in Figure 9 and 10 which show both AC and DC input and output options.

The HDMP-2006 can interface the output directly into a 50 Ohm load with or without a coupling capacitor, or directly into an ECL gate (see Figure 10). The excellent line matching, when terminated externally, also dampens the pulse reflections that typically occur in high frequency applications.

Application Interface Circuits

There are three recommended application configurations for the HDMP-2006, wherein the user either AC or DC couples the DATA and/or supplies the V_{IN} and V_{REF} DC bias. In addition, there is a possible but non-recommended case where the user also supplies the DC clock bias externally, or DC couples the clock.

For AC coupled applications, the configuration shown in Figures 9a and 10a is recommended. Here, both the clock and data, as well as the V_{REF}, utilize the internal V_{BB} generator. This is suitable for inputs with 50% average mark ratio such as PRBS.

AC coupled applications can also employ an externally supplied DC bias for V_{IN} and V_{REF} as shown in Figure 9b. The bias level should be close to -1.3 V. For temperature compensation reasons, the V_{IN} and V_{REF} biasing should be supplied from the same source as indicated in Figure 9b. If separate biasing is used for V_{IN} and V_{REF}, care should be taken to ensure that the biasing from the different sources tracks identically as possible over temperature excursions.

For DC coupled applications, the configuration shown in Figures 9c and 10b is recommended. Here the clock is biased from V_{BB}; V_{IN} and V_{REF} are directly DC coupled externally. For temperature compensation reasons, the quiescent DC level of the DATA and DATA should temperature track and be set to approximately -1.3V as in standard ECL levels. For single-ended DC coupling, V_{REF} can be tied to an external -1.3V or a voltage (near -1.3 V) that matches and tracks the data quiescent voltage (see Figure 9c). This configuration is necessary for data with mark ratios much different than 50%.

For all three recommended configurations above, the bias of the clock by the internal V_{BB} is necessary for temperature compensation of the sampling of the decision circuit relative to the input data.

The user can separately bias the clock input if desired (Figure 9d). In this case the relative levels and temperature tracking of the DC bias signals need to be carefully considered. Experimental testing by user is strongly recommended.

Interfacing Cases

Case	Figure	Data In	V_{REF} DC Bias	V_{IN} DC Bias	Clock Bias
1	9a	AC	$=V_{BB}$	$=V_{BB}$	$=V_{BB}$
2	9b	AC	External	External	$=V_{BB}$
3	9c	DC	External	External	$=V_{BB}$
4	9d	AC or DC	External or = V_{BB}	External or = V_{BB}	External

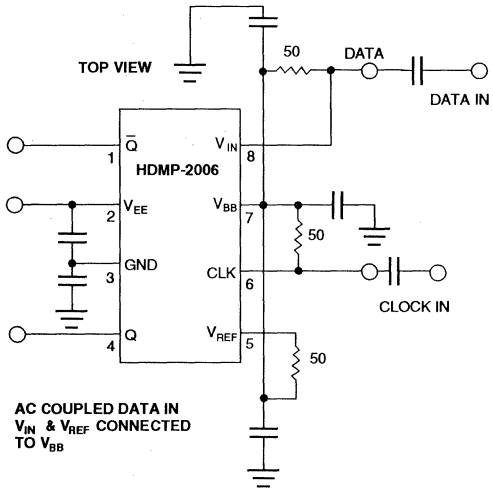


Figure 9a. AC Interface Circuit

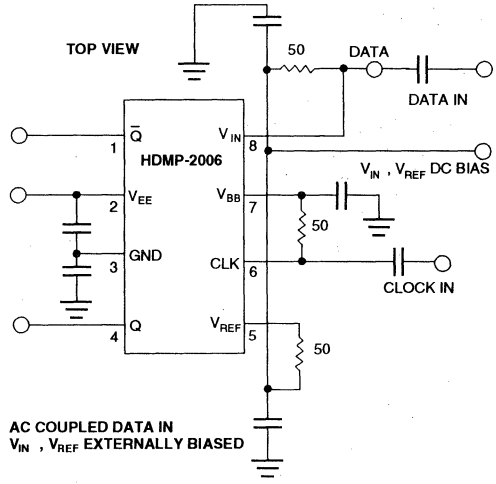


Figure 9b. AC Interface with DC V_{IN} and V_{REF} Bias

ALL CAPACITORS ARE 39000 pF
ALL RESISTORS ARE 50 Ohms

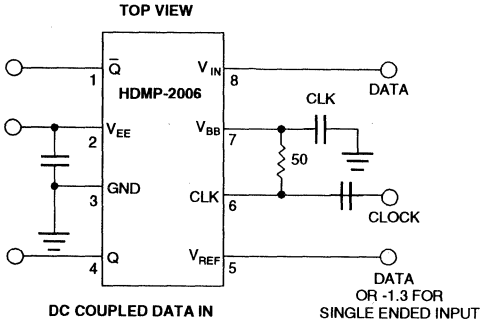


Figure 9c. DC Interface Circuit

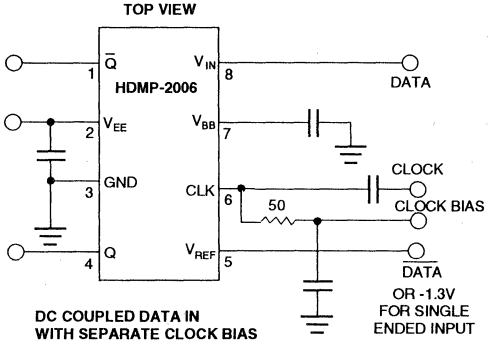


Figure 9d. DC Interface with External CLOCK Bias

Output Drive Level

The output driver is designed to deliver 0.8 V into 50 Ohms AC, or DC coupled, as shown in Figures 10a and 10b.

The V_{OH} and V_{OL} levels of the driver are such that the peak-to-peak voltage is approximately 1.2 V unloaded centered around V_{BB} = -1.3 V. For driving ECL, the line can be terminated with a parallel combination of resistors as shown in Figure 10c. The equivalent termination of 50 Ω shrinks the pk- to-pk voltage down to approximately 0.8 V centered about -1.3V. The output impedance of the driver is matched to 50 Ω. The amplitude can be increased with larger termination resistance with minimal VSWR penalty. Nominal values for a 50 Ω interface are: R_1 = 140 Ω; R_2= 77 Ω.

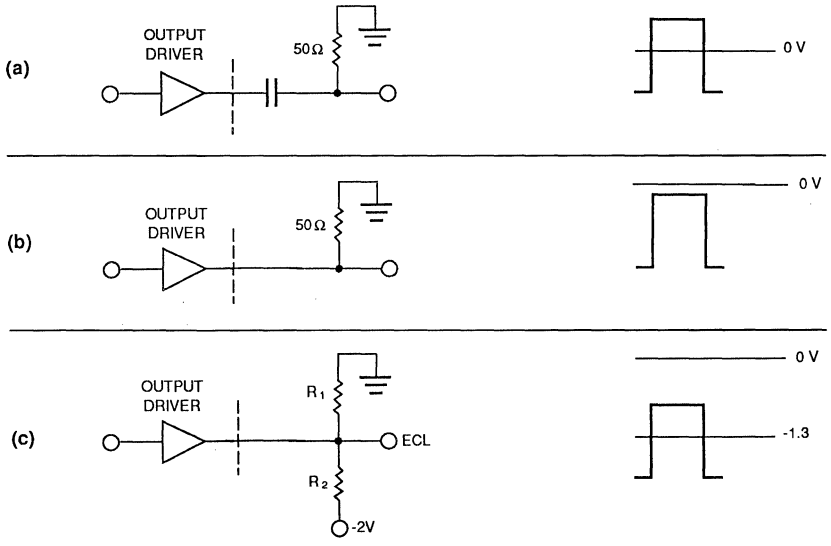
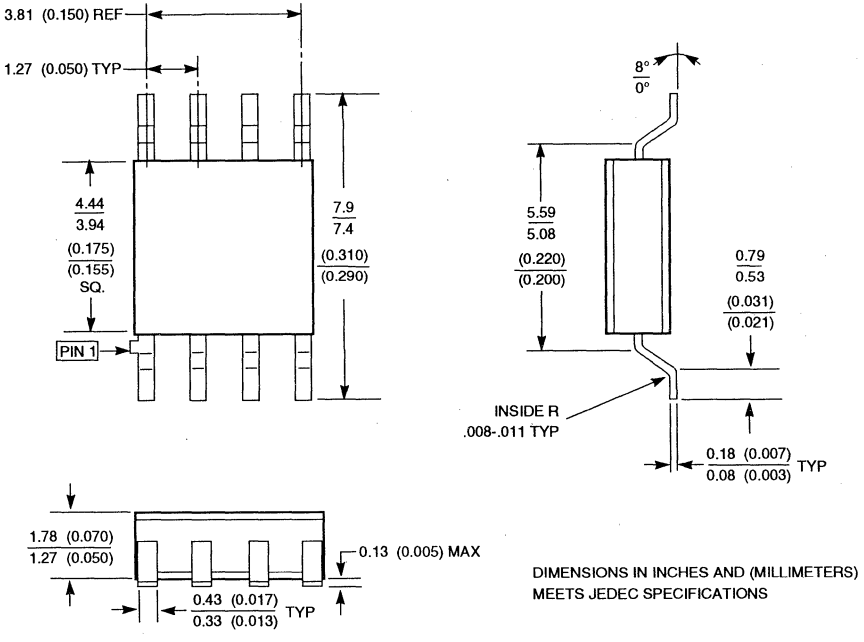


Figure 10. Output with Various Loading Conditions



NOTE: MAXIMUM STATIC PRESSURE ON PACKAGE <30 PSI (MIL-STD-883, METHOD 1014). CARE SHOULD BE TAKEN IN HANDLING AND MOUNTING SO THE PRESSURE LIMIT IS NOT EXCEEDED.

Figure 11. Package Outline Dimensions

HEWLETT PACKARD

High Speed Silicon Bipolar 622 Mb/s Serial Data and Clock Recovery Circuit

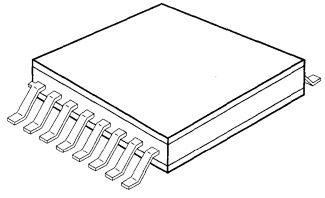
Technical Data

HDMP-2501

Features

- Single Chip Clock Extraction and Data Retiming
- Designed for 622 Mb/s Applications
- Easy to Apply, Cost Effective
- Operational with Data Patterns Pseudorandom to 2^{23}-1
- Lock Time < 2.5 ms
- Low Jitter Generation < 1.7 Degrees at 622 Mb/s
- Auto Adjusting – No Board Level Adjustment Needed
- Autotracks Temperature and Voltage Changes
- 0 to 65°C Case Temperature Range
- ECL Compatible I/O
- 50 mV Minimum Signal Input Required
- Standard ECL -5.2V & -2.0V Power Supply
- Low Power Dissipation (1.4W)
- Hermetic Glass Metal Surface Mount Package

HDMP-2501



Applications

- Telecom and Datacom Switching Systems
- Computer Back Plane Interconnect
- Board to Board High Speed Data Links

Description

The HDMP-2501 is a 622 Mb/s serial data and clock recovery circuit which is based on a Phase Locked Loop (PLL) approach for clock extraction. This chip includes a phase/frequency detector, integrator (external capacitor required), and a voltage controlled oscillator (VCO), see Figure 1. A self contained decision circuit automatically aligns the data relative to the recovered clock. Both recovered clock and retimed data outputs are available.

The digital phase detector generates a correction to the VCO ramp after each transition of the input serial data stream.

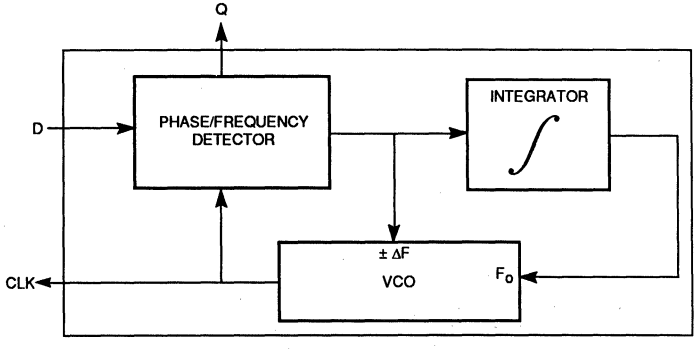
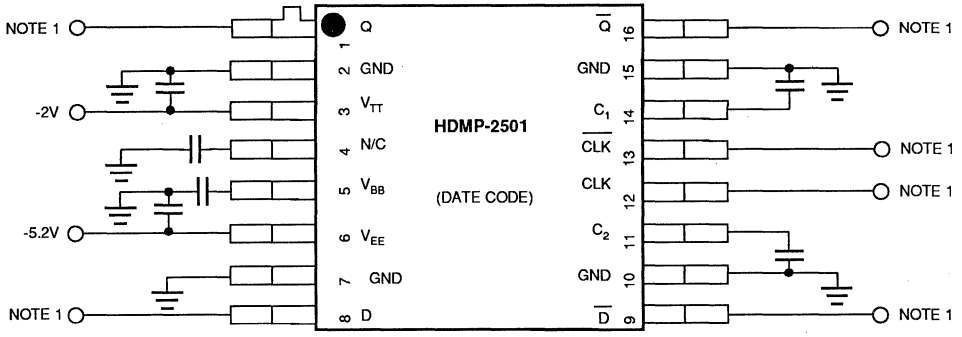


Figure 1. Functional Block Diagram

The design insures clock capture over the entire range of the VCO, and provides for fast lock-up and autotracking of the recovered clock over temperature and supply voltage changes. No external adjustment is required.

The PLL approach integrated in this design eliminates the temperature and phase variation conditions normally found with multiple device and diverse technology approaches such as surface acoustic wave devices.



NOTES:
1. PINS 1 AND 16 (Q AND $\overline{Q}$); 8 AND 9 (D AND $\overline{D}$); 12 AND 13 (CLK AND $\overline{CLK}$) **MUST** BE TERMINATED TO AC OR DC 50 Ω (SEE FIGURE 11).
2. CAPACITORS SHOWN ARE 0.1 µF CERAMIC CHIP TYPE AND ARE REQUIRED FOR ALL OPERATING CONDITIONS.

Figure 2. Package Connection

Table 1. HDMP-2501 Pin Connections Description

Label	Pin	Description
C_1	14	Charge pump capacitor connection. 0.1 µF typical, ground other end.
C_2	11	Charge pump capacitor connection. 0.1 µF typical, ground other end.
CLK	12	Retimed clock output AC or DC couple to 50 ohms, or DC couple to ECL.
$\overline{CLK}$	13	Retimed clock output (complimentary) AC or DC couple to 50 ohms, or DC couple to ECL.
D	8	Serial data input. ECL bias or AC couple with 0.1 µF.
$\overline{D}$	9	Serial data input (complimentary). ECL bias or AC couple with 0.1 µF
GND	2, 7, 10, 15	Ground
N/C	4	No connection to chip
Q	1	Retimed data output.
$\overline{Q}$	16	Retimed data output (compliment) AC or DC couple to 50 ohms, or DC couple to ECL.
V_{BB}	5	Internally generated bias reference voltage, typically -1.3 volts. Use bypass capacitor.
V_{EE}	6	Main power supply pin, typically -5.2 volts. Use bypass capacitor.
V_{TT}	3	Secondary power supply pin, typically -2.0 volts. Use bypass capacitor.

Absolute Maximum Ratings

T_C = 25°C, except as specified. Operation in excess of these may result in permanent damage to this device.

Symbol	Parameter	Units	Min.	Max.
V_{EE}	Supply Voltage	Volts	-6.0	
V_D	Data Input Voltage	Volts Pk to Pk		2.0
T_{op}	Case Operating Temperature	°C		+105
T_{stg}	Storage Temperature	°C	-60	+150
T_{max}	Maximum Assembly Temperature (for 60 seconds maximum)	°C		+300

Thermal Specifications

Symbol	Parameters	Units	Typical
θjc	Thermal Resistance (Die to Case)	°C/W	10
P_D	Power Dissipation at V_{EE} = -5.2V	Watts	1.4

DC Electrical Specifications

Symbol	Parameters	Units	Min	Typ.	Max.
V_{EE}	Supply Voltage	V	-5.46	-5.2	-4.94
I_{EE}	Supply Current	mA		230	
V_{TT}	Second Supply Voltage	V	-2.05	-2	-1.95
I_{TT}	Second Supply Current	mA		75	

AC Electrical Specifications

T_C = 25°C; V_{in} = 200 mV p-p @ 622 Mbp/s @ V_{EE} = -5.2V; V_{TT} = -2 V
Input data test sequence = PRBS @ 2^{23}-1; D and $\overline{D}$ are AC coupled (0.1 µF), 50Ω termination.
Integrating capacitors C_1 and C_2 are 0.1 µF (refer to Figure 2).

Symbol	Parameters	Units	Min.	Typ.
V_D	Minimum Data Input Voltage (pk - pk) (Ambiguity @ 10^{-7} BER)	mV		50
t_{acq}	Acquisition Lock Time	ms		2.3
t_r, t_f	Rise Time, Fall Time; Data and Clock See Figures 7 and 8	ps		200
J_g	Jitter Generation	ps (rms)		7.5
V_{CLK}	Recovered Clock Output (pk to pk)	V	0.6	0.7
V_Q	Output Voltage Swing (pk to pk) See Figure 7	V	0.6	0.7
VSWR	Data In and Out; Clock out	—		< 2:1

Theory of Operation

The retiming circuit is based on a PLL approach to timing extraction[1]. The functional block diagram is shown in Figure 1. A phase/frequency detector samples the incoming data, and generates an error signal which controls a dual input VCO. the VCO is realized as a ring oscillator in order to be integrated on the same chip.

The VCO frequency, F_0, is adjusted by feedback to a frequency approximately equal to the incoming data bit rate. The fine adjustment $\pm\Delta F$, is made by a bang-bang delay element as shown in Figure 3. The bang-bang element tracks the small variations of the incoming bit rate. The ring oscillator has a nominal delay of 800 ps with a typical usable range of ± 10%. The bang-bang fine control delay time is approximately 3 ps. The response time of the bang-bang element is about 700 ps for a full VCO update or much less than one clock cycle at 622 Mb/s.

The integrator (Figure 1) is achieved by a balanced charge-pump configuration with two off chip capacitors (pins 11 and 14).

[1]B. Lai and R. Walker, "A Monolithic 622 Mb/s Clock Extraction and Retiming Circuit", ISSCC91 Paper TPM 8.7.

Phase/Frequency Detector

The phase/frequency detector is shown in Figure 4. In the sampling pattern of Figure 4, the input data is sampled at three points: the bit prior to the transition, in the vicinity of the transition, and the bit following the transition. At each transition encountered, the clock can be deduced as either fast or slow compared to the incoming data. This information is used to generate a pulse train which updates the integrator and drives the bang-bang delay element.

The phase tracking of clock to data behaves as shown in Figure 5. Each correction in the faster direction (clock phase increasing with respect to data phase) has slope $+\Delta F$, and each correction in the slower direction has slope $-\Delta F$. Over time, the VCO phase tracks the phase changes in the incoming data. Flip-flop A (Figure 4) samples at the center of the data eye and provides the decision circuit function.

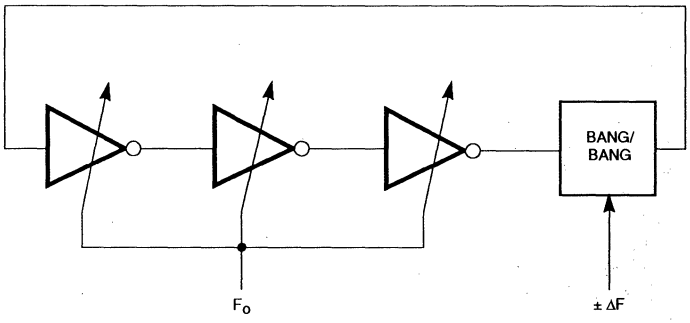
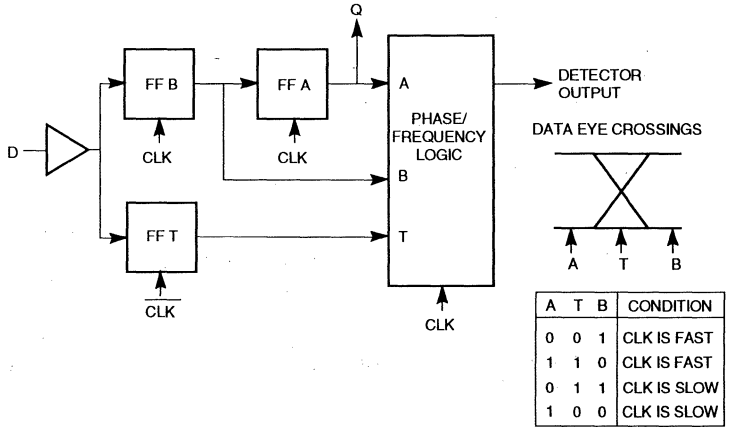


Figure 3. Ring Oscillator and Control Elements



A	T	B	CONDITION
0	0	1	CLK IS FAST
1	1	0	CLK IS FAST
0	1	1	CLK IS SLOW
1	0	0	CLK IS SLOW

Figure 4. Block Diagram of the Phase/Frequency Detector.

Lock Capture

Initial lock acquisition behavior is highly complex and works best with high transition densities typical of pseudorandom bit patterns. Due to the phase frequency detector architecture, the acquisition behavior is different from a typical PLL.

Lock capture of repetitive data patterns becomes increasingly difficult as transition density decreases. This can cause lock acquisition times to be

significantly longer than expected or sub-harmonic false locks to occur.

The fact that false lock is weaker than true lock is essential to eliminating it. When both true and false phase locks occur, a slight displacement of the data phase relative to clock phase produces an error signal in the bang-bang detector which tends to restore it back to the original lock condition. This restoring force is represented at the integrating capacitor by a change in capacitor voltage which is in turn applied to the VCO to adjust the frequency. A simple idea to eliminate false lock is to connect a current source to the integrating capacitor (Figure 6). Its immediate effect is to ramp the capacitor voltage,

$$I_{CS} = \frac{dQ}{dt} = C\frac{dV}{dt},$$

which causes the VCO to sweep. If the capacitor charging rate is high enough to cancel out the "restoring force" current due to false lock, then false lock will be suppressed. However, the ramp current must not be so large it will suppress true lock. An estimate of true lock current can be obtained through acquisition lock time t_{acq}. For example, the HDMP-2501 with 0.1 μF integrating capacitors has a t_{acq} of approximately 2.3 mS. During this time the VCO control voltage changes about 1 Volt. Thus

$$I = C\frac{dV}{dt}(0.1\ \mu F)(\frac{1\ Volt}{2.3\ mS}) = 43\ \mu A$$

is an estimate of the ramp current.

A simple and inexpensive lock enhancement circuit is shown in Figure 7. The circuit consists of a very low frequency oscillator built from an inexpensive 555 timer chip, 3 resistors and 1 capacitor (plus a supply bypass capacitor). The time output is a 100 Hz TTL square wave applied via a large (15 kΩ) resistor to one side of the balanced HDMP-2501 integrator. Since the balanced integrator circuit uses differential pairs, the signal can be applied to only one side while the other side responds by symmetry.

To assist correct lock capture, the VCO can be forced to its center frequency by momentarily equalizing the two integration capacitor voltages (pins 11 and 14) as shown in Figure 6. The VCO then begins its lock capture from the center frequency which, by design, is close to the data frequency.

Input/Output Impedance Match

The input and output are closely matched to 50 ohms impedance. This allows easy interconnection to other circuits with minimum reflection of signals. The return loss performance is shown in Figures 10 and 11.

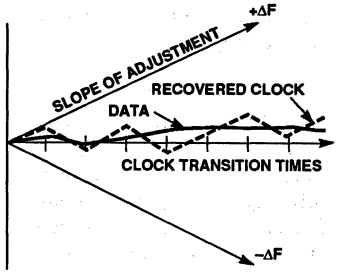


Figure 5. Clock Tracking of Data Phase.

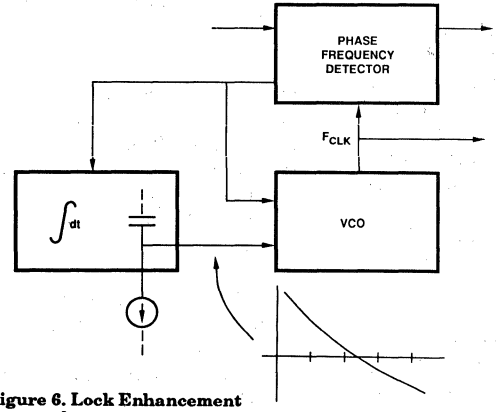


Figure 6. Lock Enhancement Approach.

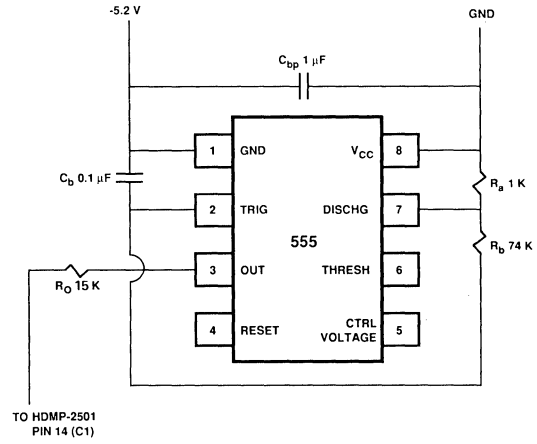


Figure 7. Practical Lock Enhancement Circuit.

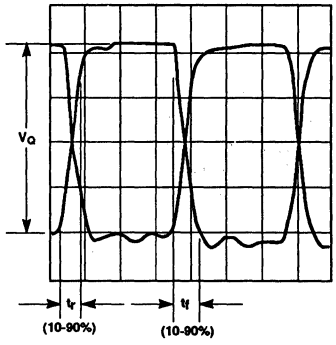


Figure 8. Typical Data Output Waveform.

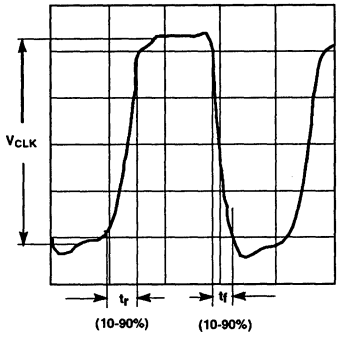


Figure 9. Typical Clock Output Waveform.

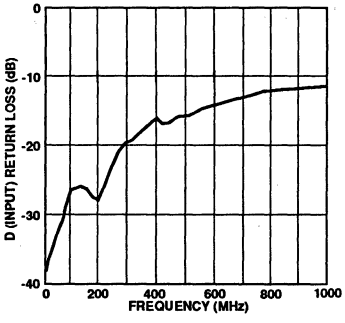


Figure 10. Typical Input Return Loss vs. Frequency.

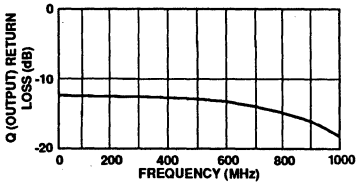


Figure 11. Typical Output Return Loss vs. Frequency.

Output Drive Level

The output driver is designed to deliver 0.8 V into 50 ohms, AC or DC coupled, as shown in Figures 12a and 12b.

The V_{OH} and V_{OL} levels of the driver are such that the peak-to-peak voltage is approximately 1.2 V unloaded centered around -1.3 V.

For driving ECL, the line can be terminated with a parallel combination of resistors as shown in Figure 12c. The equivalent termination of 50 Ω shrinks the peak-to-peak voltage down to approximately 0.8 V centered about -1.3 V. The output impedance of the driver is matched to 50 Ω. The amplitude can be increased with a larger termination resistance with minimal VSWR penalty. Nominal values for a 50 Ω interface are R_1 = 140 Ω, R_2 = 77 Ω.

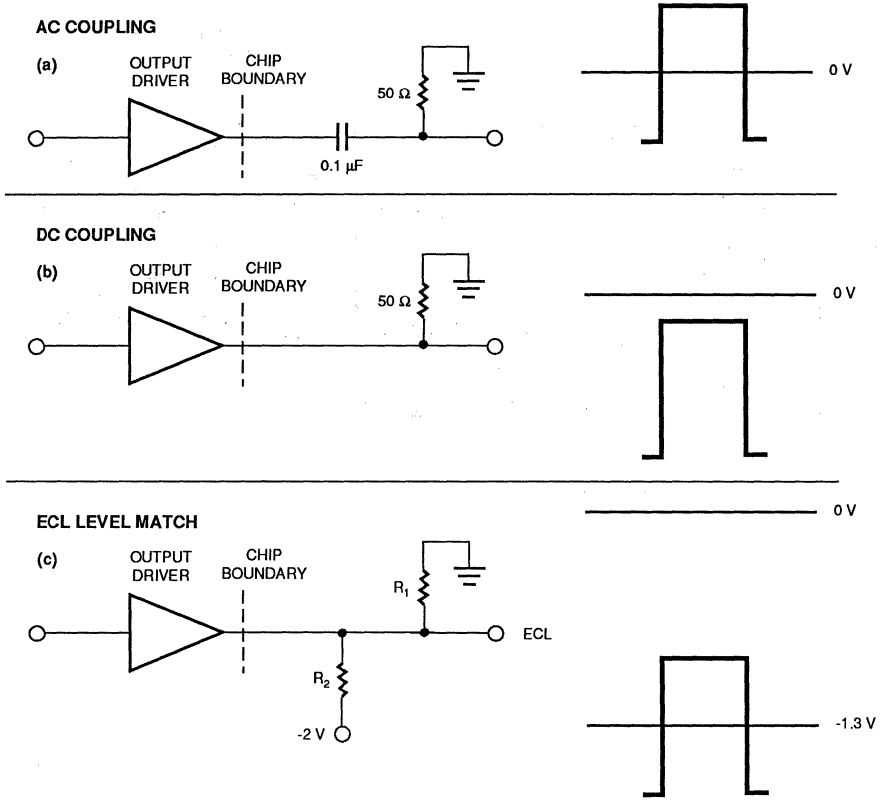


Figure 12. Output with Various Loading Conditions.

Performance vs. Supply Voltage V_{EE} Variation

The performance of the output voltage is shown in Figure 13. A 600 mV level for ECL compatibility is maintained.

VCO lock range is relatively insensitive to V_{EE} changes. The typical behavior is shown in Figure 14.

Temperature Performance

The VCO range of the HDMP-2501 is designed to accommodate variation over temperature. Figures 15 through 19 show typical performance over temperature.

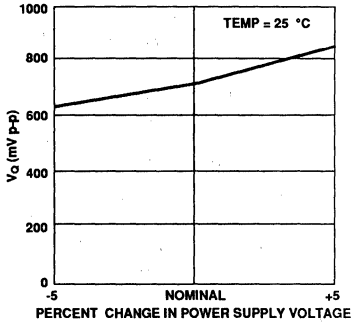


Figure 13. Output Voltage, V_Q vs. Power Supply, V_{EE}, Change.

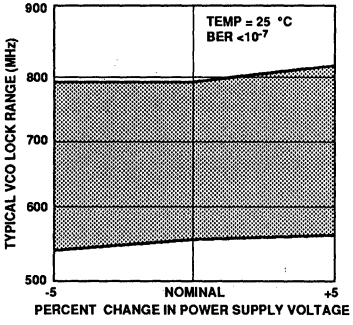


Figure 14. VCO Lock Range Variation vs. Supply Voltage, V_{EE}.

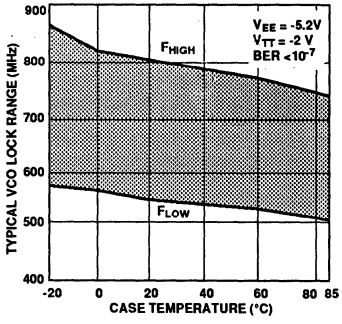


Figure 15. Typical VCO Lock Range Variation vs. Temperature.

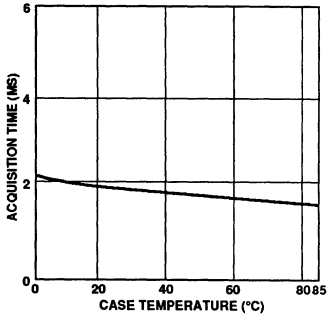


Figure 16. Typical Acquisition Time Variation vs. Temperature.

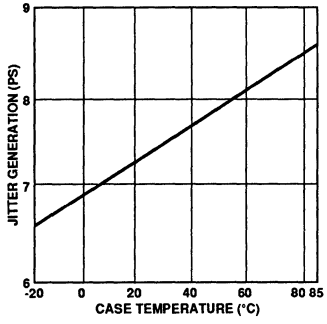


Figure 17. Typical RMS Value Jitter Generation Variation vs. Temperature with 3.5 ps Test Set Jitter.

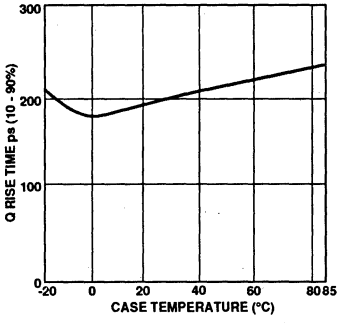


Figure 18. Typical Output Rise Time Variation vs. Temperature.

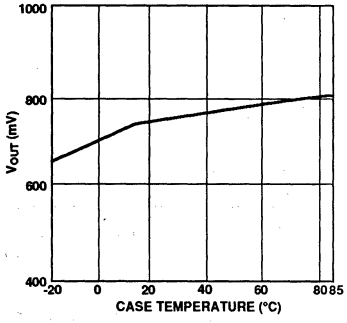


Figure 19. Typical Output Voltage Variation vs. Temperature.

FIBER OPTICS

Heat Sinking

Heat sinks are recommended for this part, especially for high temperature operation. When solder mounted on a board designed with the features shown in Figure 20, the thermal test card provides a thermal resistance (junction to air) θ_{JA} of approximately 40°C/W when measured in still air. The via holes shown are for thermal conduction between front side and back side metallization.

Package and Mechanical Considerations

The package is a glass metal construction designed for excellent high frequency electrical performance. The cover, base, and leads are gold plated Kovar (ASTM F-15 alloy). The mechanical outline is shown in Figure 21.

The base and cover of the package are electrically isolated and may be grounded. The base may be soldered to a printed circuit board.

NOTE: Maximum static pressure on package <30 PSI (MIL-STD-883, METHOD 1014). Care should be taken in handling and mounting so the pressure limit is not exceeded.

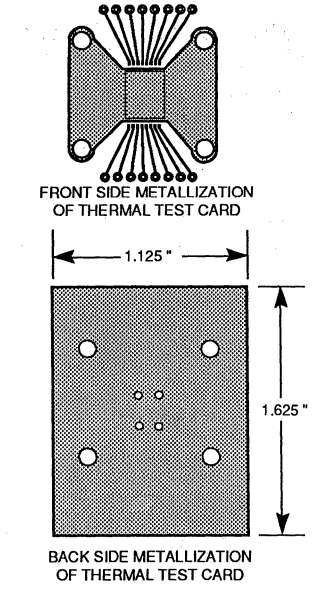


Figure 20. Circuit Mounting Configuration for Thermal Resistance Test.

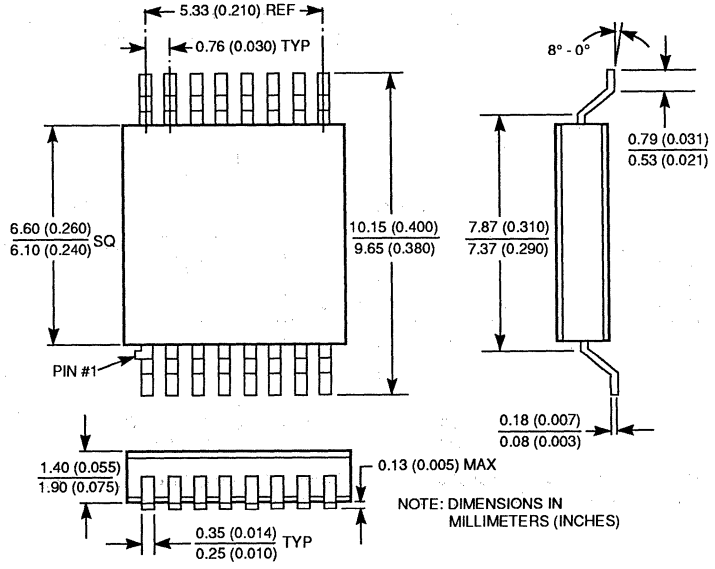


Figure 21. Outline F6.

HEWLETT PACKARD

Fiber Channel 266 MBaud Optical Link Card

Technical Data

HOLC-0266

Features

- **Conforms to ANSI X3T9.3 Fiber Channel Standard (25-M5-SL-I) (FC-0 Layer)**
- **Supports Link Lengths to 2 km at 266 MBaud**
- **Multi-Sourced Package/ Footprint**
- **Highly Reliable Multi-Mode Laser for High Performance at Low Cost**
- **Certified for Worldwide Class 1 Laser Safety Standards**
- **Industry Standard SC Connectors**
- **Highly Integrated Surface Mount Construction**
- **Industry Standard TTL Level Interface**

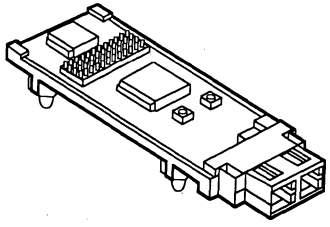
Applications

- **CPU to CPU**
- **CPU to Disk/Disk Array**
- **CPU to Peripheral**
- **Backplane Extender**
- **High Speed Data Switching**
- **Proprietary Point-to-Point Links**

Description

The HOLC-0266 optical link card (OLC) is a highly integrated fiber optic transmitter and receiver that provides a high speed serial link operating at a signaling rate of 265.625 MBaud implementing the fiber channel FC-0 specification for Short Wavelength (SWL) operation. This compact, double-sided, surface mount card conforms to Fiber Channel (25-M5-SL-I), a task group of the ANSI X3T9.3, Version 2.2 Standards Committee. The optical link card is designed to connect to a user's system card and communicates through a 10-bit wide encoded data (8B/10B) interface at industry standard TTL levels.

The OLC uses self-pulsating, SWL multimode lasers which are produced in high volumes, with proven high reliability, and low cost, for data transmission at low bit error rate (BER) levels. The OLC has on board all the functions necessary for sending 10-bit wide encoded data serially. These functions include the serializer, deserializer, clock recovery, laser driver,



SIZE:
HEIGHT: 0.547 INCHES (13.9 mm)
WIDTH: 1.559 INCHES (39.6 mm)
LENGTH: 4.508 INCHES (114.5 mm)

and automatic power control. All of these functions are implemented in silicon bipolar technology. In addition, the OLC uses an innovative open loop fiber control scheme that certifies the OLC for Class 1 laser safety limits. The OLC conforms to U.S. regulation DHHS 21 CFR(J), and internationally to IEC 825.

The optical portion of the OLC interfaces to multimode optical fiber, (recommended 50/125 µm, 62.5 µm can also be used), through low loss, easy to use, push-pull SC connectors.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Reference
Storage Temperature	T_S	-40		+75	°C	Still Air
Relative Humidity - Storage	RH_S	5		95	%	
Ambient Operating Temperature	T_{OP}	0		60	°C	
Relative Humidity Operating	RH_{OP}	8		80	%	
Supply Voltage	V_{CC}	4.0	5.0	6.0	V	
Data Input Voltage	V_I	0		V_{CC}	V	

Caution: It is advised that normal static precautions be taken in handling and assembly of the OLC to prevent damage and/or degradation which may be induced by electrostatic discharge (ESD).
(ESD to 48 pin connector: 1000 V maximum per MIL-STD-883C HBM) (see Figure 1).

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Reference
Ambient Operating Temperature	T_{OP}	10		50	°C	Still Air
Supply Voltage	V_{CC}	4.75	5.0	5.5	V	
Low Data Input Voltage	V_{IL}	0		0.4	V	
High Data Input Voltage	V_{IH}	2.4		5.5	V	
Signaling Rate*	f_S	262.969	265.625	268.281	MBaud	

*For fiber channel compatibility, must be within ±0.01% of 265.625 MBaud.

Physical and Mechanical Description

The layout of the HOLC-0266 is shown in Figure 1. The transmit and receive circuits are mounted on opposite sides of a multi-layer, surface mount card. The card has a top and bottom signal plane and four internal power planes with the transmitter and receiver sides of the card electrically isolated. A 48-pin connector with 100-mil pin spacing is mounted on the receiver side of the OLC for connection to the user's system card. The laser is mounted in a receptacle with a graded index lens and an SC fiber optic connector. The receiver is a PIN photodiode also mounted in a receptable and an SC fiber optic connector, with a trans-impedance amplifier mounted in an SOIC package under a metal shield. The connector ports are keyed and color coded to prevent misplugging. The receiver port is colored yellow, the transmitter port is black.

Electrical connection to the users system card is through the 48-pin connector (see note 17 on page 16). The OLC also uses a molded plastic frame with J-clips for precisely and securely mounting the OLC to the user's system card. A detailed outline drawing showing the dimensions of the card and mounting bracket is given in Figure 2.

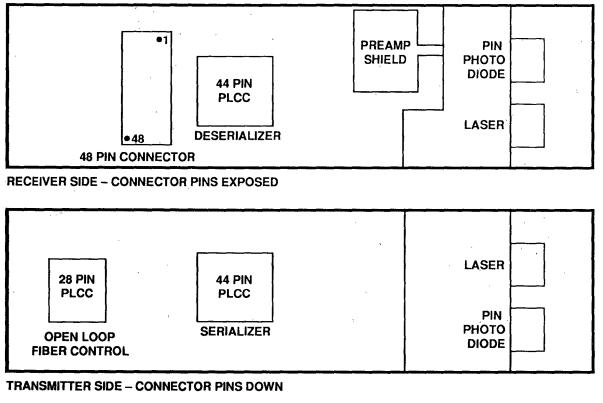


Figure 1. OLC Layout.

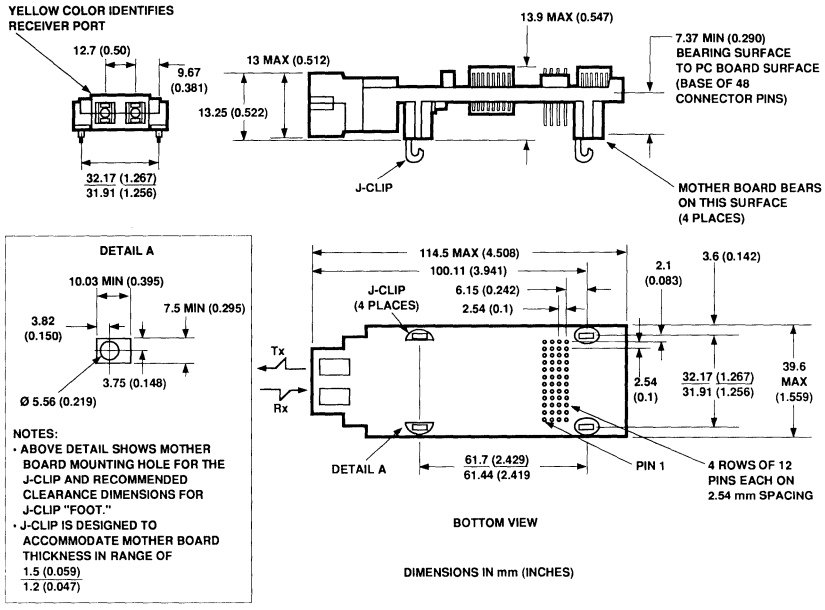


Figure 2. Optical Link Card Dimensions and Recommended Mounting Dimensions.

Electrical Description

Figure 3 is a block diagram of the transmitter, receiver and open loop fiber control portions of the HOLC-0266.

Transmitter:

10-bit wide encoded TTL level transmit data enters the shift register portion of the 44-pin PLCC serializer chip. This data is shifted out using an internal VCO at 265.625 Mb/s to the AC drive. A phase locked loop (PLL) generates the 265.625 MHz clock for the shift register, and the clock is phase locked to the user supplied 26.5625 MHz transmit clock. The AC drive modulates the 780 nm semiconductor laser with the serialized data. The DC section of the serializer controls the laser bias, keeping the laser at a correct preset power level. The DC drive also includes safety circuits that will disable the laser if an on-card fault occurs that could produce an unsafe laser power level. A multiplexer is used to provide the serialized data to the deserializer for operation of the OLC in the loopback mode.

Receiver:

The incoming laser light is received by a silicon PIN photodiode. This signal is amplified by the transimpedance amplifier which is contained in a 14-pin SOIC under the preamplifier shield. The PLL phase locks a 265.625 MHz clock to the incoming data and sends the data and the clock to the shift register of the 44-pin deserializer chip to be deserialized. The shift register uses a byte sync detector that detects the first seven bits of one polarity of the K28.5 character to enable complete bytes to be unloaded from the shift register without being fragmented. The deserializer recovers the clock and drives the 10-bit wide receive encoded data on the bus at TTL levels. Low speed Receive Clock 0 and Receive Clock 1 are output for use (see Figure 7).

Open Loop Fiber Control (OFC):

Two complementary phases of the 265.625 MHz clock are generated. The transition detector and the DC detector detect a minimum AC and DC level entering the PIN photodiode. These redundant signals are used by the open fiber control chip, a 28-pin PLCC module, as a safety interlock to shut down the link in the event of an open optical fiber. If the fiber is open, the OFC module pulses the laser at a low duty cycle. This produces Class 1 optical power in the open fiber. When the fibers are reconnected, the OFC returns the laser to continuous power. See the "Open Loop Fiber Control" section of this data sheet (page 10) for further information.

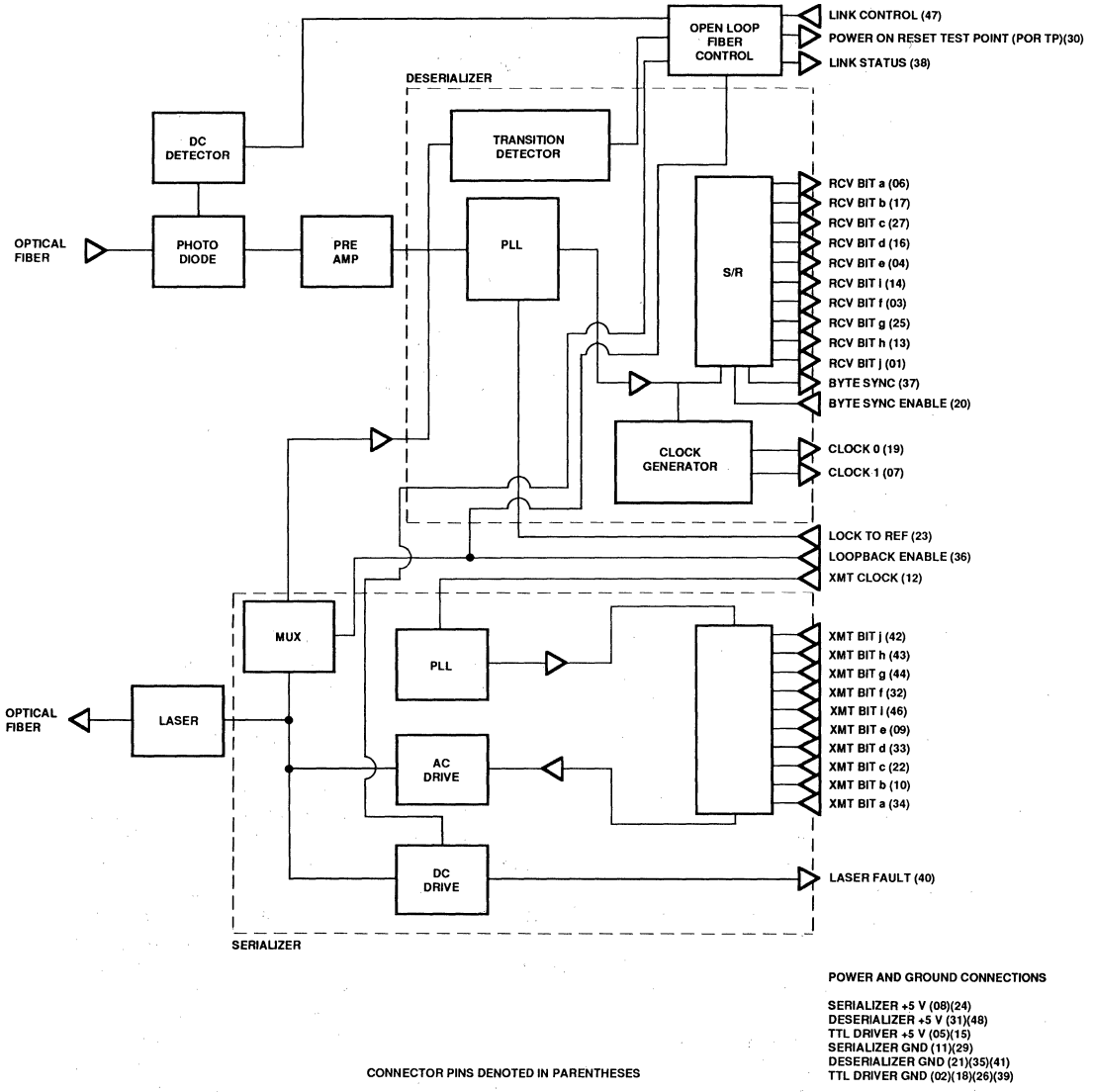


Figure 3. HOLC-0266 Functional Block Diagram.

Electrical Interface

Figure 4 defines the functions of the 48 connector pins. The pin functions and pin numbers are as viewed on the HOLC-0266 with the connector pins pointing up toward the viewer. These functions will be discussed in detail in the "OLC Input Definitions" (page 6) and "OLC Output Definitions" (page 6) sections of this specification.

Figure 5 represents the interface between the OLC and the user's system. The OLC interfaces directly with the encode/decode logic of the user's system.

37 • Byte Sync	25 • RCV bit g	13 • RCV bit h	1 • RCV bit j
38 • Link Status	26 • TTL Gnd	14 • RCV bit i	2 • TTL Gnd
39 • TTL Gnd	27 • RCV bit c	15 • TTL +5V	3 • RCV bit f
40 • Laser Fault	28 • No Connect	16 • RCV bit d	4 • RCV bit e
41 • Deserializer Gnd	29 • Serializer Gnd	17 • RCV bit b	5 • TTL +5V
42 • Xmt bit j	30 • POR TP	18 • TTL Gnd	6 • RCV bit a
43 • Xmt bit h	31 • Deserializer +5V	19 • RCV Clock 0	7 • RCV Clock 1
44 • Xmt bit g	32 • Xmt bit f	20 • Byte Sync Enable	8 • Serializer +5V
45 • No Connect	33 • Xmt bit d	21 • Deserializer Gnd	9 • Xmt bit e
46 • Xmt bit i	34 • Xmt bit a	22 • Xmt bit c	10 • Xmt bit b
47 • Link Control	35 • Deserializer Gnd	23 • Lock to Reference	11 • Serializer Gnd
48 • Deserializer +5V	36 • Loopback Enable	24 • Serializer +5V	12 • Xmt Clock

Figure 4. Connector Pin Definition (Pins Up)

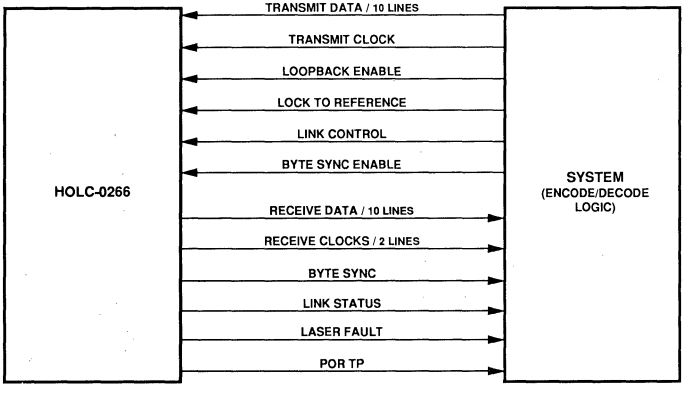


Figure 5. OLC/System Interface Signals.

OLC Input Definitions

Transmit Data:
Ten transmission lines carry 10-bit wide encoded data from the systems encode logic to the OLC to be received by the shift register of the serializer. The data will be serialized and launched onto the fiber starting with bit "a" and ending with bit "j" (see Note 8).

Transmit Clock:
The serializer uses the Transmit Clock to synthesize the 265.625 MHz clock (see Note 9). Figure 8 shows the relationship between the Transmit Clock and the Transmit Data. A minimum duty cycle of 40% is required for this clock to operate properly. A maximum of 10 ns jitter (peak to peak) is allowed on the rising edge of this clock.

Loopback Enable:
This active high signal wraps the Transmit Data from the Serializer to the Deserializer (see Note 10). The laser is disabled while Loopback Enable is active. Once Loopback Enable is deactivated one of two events will occur. If the link was active and operating prior to Loopback Enable being activated, the laser will be activated and will stabilize within 1.8 µs. If the link was not active prior to Loopback Enable being activated, the laser will pulse after 10.1 seconds and continue to pulse until the fiber is connected. See the section entitled "Open Loop Fiber Control" (page 10) for a complete description of the safety interlock.

Lock to Reference:
This is an active low signal that synchronizes the Deserializer phase locked loop to the Transmit Clock (see Note 11). This signal should stay on for approximately 8 µs. The Deserializer will be locked to the incoming serial data in less than 8 µs after Lock to Reference is deactivated. The 8 µs time period is approximate and is intended to represent the correct order of magnitude.

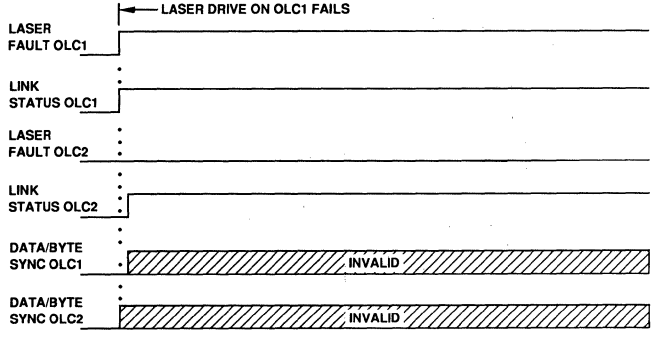


Figure 6. Laser Fault Sequence.

Link Control:
This active high signal turns the laser off (see Note 12). When this line is deactivated, the Open Loop Fiber Control Module will connect the link within 10.1 seconds.

Byte Sync Enable:
Asserting the active high signal makes the Deserializer reset the Receive Clocks when a comma character (see Byte Sync) is detected (see Note 11). When this signal is low, the comma character is treated as normal data.

OLC Output Definitions

Receive Data:
Ten lines are used by the Deserializer to send 10-bit wide encoded data to the system's decode logic (see Note 6). These signals are clocked by the systems receive clocks inside the decode logic. The relationship between Receive Clocks and Receive Data is shown in Figure 7. If no light is received by the PIN photodiode, or the PLL is out of lock for some other reason, the Receive Data lines will be random. A Loopback Enable mode initiated on an upstream OLC will cause the Open Loop Fiber Control module on that OLC to turn its laser off. Under these conditions, data at the output of the downstream deserializer will be invalid. In addition, if the Deserializer is in the Lock to Reference mode, the Receive Data will be invalid.

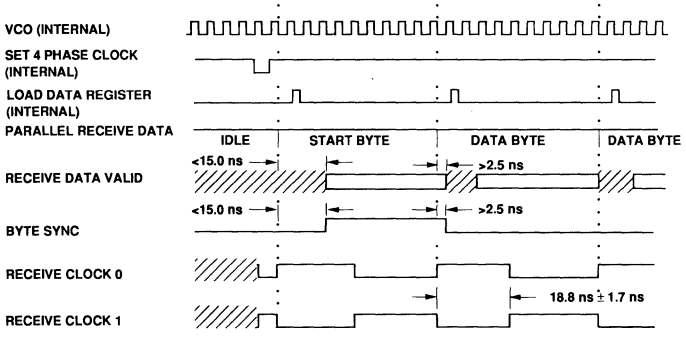
Receive Clocks:
The Deserializer generates two complementary clocks for use by the system's decode logic to clock the Receive Data into an elastic buffer (see Note 6). These

clocks will be reset anytime a Byte Sync word is received. If a Byte Sync word is received asynchronously (see Figure 7), the Receive Clocks will immediately be reset. The worst case duty cycle of the Receive Clocks is 30%. If no light is received by the PIN photodiode, or the PLL is out of lock for some other reason, the Receive Clocks will be operating at a frequency between 17 MHz and 33 MHz.

Byte Sync:
This active high signal is driven by the Deserializer (see Note 6). When the Deserializer detects a comma character, it sets the Byte Sync high for one cycle indicating the start of a frame. The Receive Clocks are reset according to Figure 7. The comma detect function detects the first seven bits of one polarity of the K28.5 character (0011111010) as defined in the IBM Journal of Research and Development, Vol. 25, No. 5, September 1983, 8B/10B Transmission Code. Bit a is launched on the fiber first, bit j is last. If no light is detected by the PIN photodiode, or the PLL is out of lock for some other reason, the Byte Sync line will pulse randomly.

a	b	c	d	e	i	f	g	h	j
0	0	1	1	1	1	1	X	X	X

Link Status:
This active high signal is driven by the Open Loop Fiber Control circuitry (see Note 7). Link Status high indicates an open fiber connection. In this mode, the Open Loop Fiber Control will be pulsing the laser at a low power level, meeting Class 1 safety requirements. Once the fiber is reconnected, the link will be re-established in less than 10.1 seconds. It takes several milliseconds for Link Status to go high after the fiber is disconnected. Invalid Receive Data and Byte Sync will occur prior to the Link Status being activated high.



NOTE: ALL CRITICAL TIMINGS ARE REFERENCED TO THE POSITIVE EDGE OF THE CLOCKS, ASSUMING 30 pF OUTPUT LOADS ON CLOCK AND DATA LINES.

Figure 7. Deserializer Interface Receive Timings.

Laser Fault:
This active high signal is driven by the Serializer (see Note 7). Once an improper power level in the laser driver is detected, the Serializer activates the Laser Fault and the laser is turned off in approximately 1 ms. During power up, the laser control loop will stabilize in less than 100 ms after the supply reaches 4.0 V. When the Laser Fault is activated, the Open Loop Fiber Control shuts down the laser through two independent paths so a single malfunction cannot prevent the laser from being turned off. The OLC receiver connected to this laser will detect a loss of light (no light at the PIN photodiode), and Link Status will be activated. Figure 6 shows the sequence of events during a laser driver hardware malfunction.

Power On Reset Test Point (POR TP):
This signal is used to test the OLC (see Note 7). POR TP is at an undetermined level when the +5 V supply is below 3.6 V. POR TP is low when the supply is between 3.6 V and 4.75 V, and it is high when the supply is greater than 4.75 V.

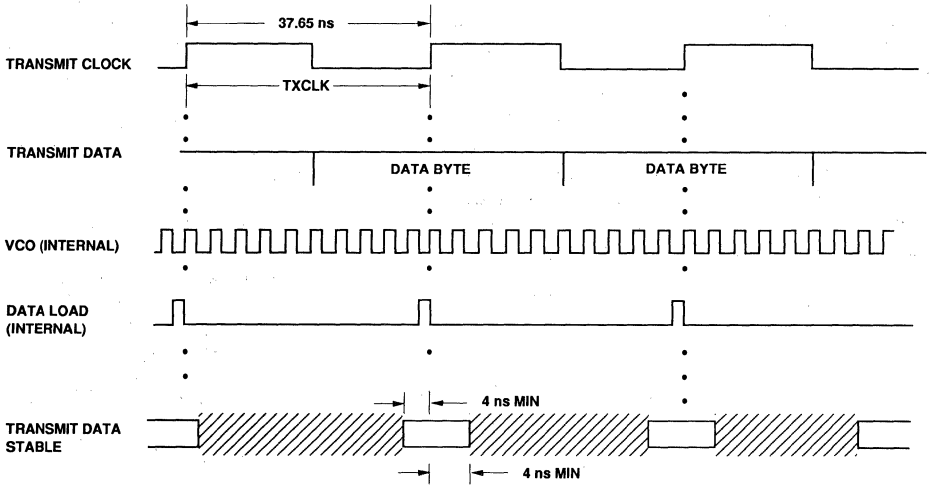
Link Operation

Serial Link Receive Operation: The Deserializer generates two complementary clocks for use in clocking the parallel data coming from the Deserializer. Each of the Receive Clocks has a nominal 37.65 ns period. Figure 7 shows the relationship of the Start Byte, the Receive Data, the Byte Sync Pulse, and the two Receive Clocks generated by the Deserializer.

Serial Link Transmit Operation:
The Serializer uses a single-phase 37.65 ns Transmit Clock for transmit operations. Figure 8 shows the timing relationship of the Transmit Clock and the Transmit Data.

Link Acquisition Sequence:
The following sequence and conditions are required for proper OLC operation. The receive PLL will not self-lock to the incoming data stream. For example, when the card is powered up or the fiber is connected, the receive PLL will be out of bit sync. Random data will be on the 10 receive data lines, the Byte Sync line will pulse randomly, and the Receive Clocks will not be at 26.5625 MHz. To acquire bit sync, the link acquisition sequence must be followed. This has no effect on the transmit data.

- Bring Lock to Reference low for at least 8 µs after the Link Status line is low.
- The upstream station should transmit valid 8B/10B encoded data. The transmitting station clock and the receiving station clock frequencies must be within 0.5% of each other for phase lock to be assured.
- Bring Lock to Reference high (wait at least 8 µs).
- The OLC will now be in bit sync. The data on the receive lines will be correct.



NOTE: ALL CRITICAL TIMINGS ARE REFERENCED TO THE POSITIVE EDGE OF THE TRANSMIT CLOCK. JITTER OF THE POSITIVE EDGE MUST BE LESS THAN 1.0 ns.

Figure 8. Serializer/Deserializer Interface Transmit Timings.

Electrical/Optical Characteristics (T_A = 10°C to 50°C, V_{CC} = 4.75 V to 5.50 V)

Transmitter Section

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Voltage	V_{CC}	4.75	5.0	5.50	V	
Supply Current	I_{CC}	190		320	mA	
Power Dissipation	P_D	0.9		1.80	W	
Data Input Voltage - Low	V_{IL}	0		0.4	V	Note 6
Data Input Voltage - High	V_{IH}	2.4		4.0	V	Note 6
Spectral Center Wavelength	λ	770	780	850	nm	
Spectral Width	FWHM			4	nm	RMS value
Launched Optical Power	P_T	-5.0		0	dBm (avg.)	Note 1
Optical Extinction Ratio		6			dB	Note 2
Relative Intensity Noise	RIN_{12}			-112	dB/Hz	Note 3
Eye Opening		61			% (pk-pk)	Note 4
Random Jitter @ ±7 sigma limit points	RJ		19		% (pk-pk)	Note 5
Numerical Aperture	NA		0.20			

Receiver Section

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Voltage	V_{CC}	4.75	5.0	5.5	V	
Supply Current	I_{CC}	200		240	mA	
Power Dissipation	P_D	0.95		1.32	W	
Data Output Voltage - Low	V_{OL}	0		0.8	V	Note 8
Data Output Voltage - High	V_{OH}	2.0		V_{cc}	V	Note 8
Return Loss of Receiver	RL	12			dB	
Receiver Sensitivity		-17		0	dBm (avg.)	Note 13
Numerical Aperture	NA		0.20			

Optical System Performance

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Signaling Rate*	f_S	262.969	265.625	268.281	MBaud	
Link Length 50/125 µm NA = 0.20		0.002		2.0	km	Note 14
Link Length 62.5/125 µm NA = 0.275		0.002		0.70	km	Note 15
Optical Power Budget	OPB			12	dB	Notes 14,15
Bit Error Rate	BER			10^{-12}		
SC Optical Connector Attenuation			0.25		dB	Note 16
Attenuation (EOL)				0.5	dB	Note 16
Connects/Disconnects				250		Note 16

*For fiber channel compatibility, must be within ±0.01% of 265.625 MBaud.

Open Loop Fiber Control

A safety interlock is provided by the Optical Fiber Control (OFC) module on the OLC. When the OLCs are connected as in Figure 9 (below), the OFC module detects when a fiber is opened. This sequence is shown in Figure 10. If Path A is opened, the OFC on OLC2 detects it and pulses its laser at a low duty cycle. The OFC on OLC1 detects this pulse signal and also pulses its laser at a low duty cycle. This provides Class 1 optical power in Path A, the open path. OLC1 launches a pulse synchronously with the pulse it receives on Path B. OLC2, however, receives no pulse and continues in inactive mode, launching pulses. When Path A is restored, OLC2 receives pulses synchronously with its transmit pulses. OLC2 then turns off its laser and confirms that its receive pulse disappears in 1.23 ms. If it does, OLC2 then turns on the laser and confirms that it receives light in 671 µs. If it does, it keeps the laser on. This confirms that the first synchronous pulse actually came from another OLC. The OFC goes to Active Mode and the laser is on continuously. Continuous power is now restored to both paths. The longest time that this reconnect sequence will take is 10.1 seconds. Note that the term synchronous used in the above discussion is valid since the delays on the OLC and the time of flight on the fiber are insignificant compared to 617 µs.

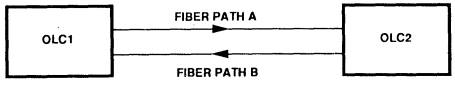


Figure 9. OLC Fiber Connection.

Laser Safety Compliance Requirements

This product is designed and certified as Class 1. It is to be used only with another Hewlett-Packard HOLC-0266 or a certified equivalent OLC to ensure Class 1 performance. This equivalent OLC must contain the Open Fiber Control system as described in the "Open Loop Fiber Control" section (above) of this specification. This is a requirement for proper operation of the HOLC-0266. Figure 10 contains a description of the open loop fiber control sequence.

The functional power supply range is specified at 4.75 V to 5.5 V. Operation outside this range may degrade performance and lifetime of the OLC. The system using the OLC must provide power supply protection that guarantees a voltage of 5.0 V ± 20% to maintain Class 1 operation.

Connection of an OLC to a non-approved optical source or operating the power supply below 4.0 V or above 6.0 V may result in hazardous radiation exposure, and may be considered an act of modifying or new manufacturing of a laser product under US regulations contained in 21 CFR(J) or CENELEC regulations contained in HD 482 S1. The person(s) performing such an act are required by law to re-certify and re-identify the product in accordance with the provisions of 21 CFR(J) for distribution within the U.S.A., and in accordance with provisions of CENELEC HD 482 S1 (or successive regulations) for distribution within the CENELEC countries or countries using the IEC 825 standard per VDE Reg. Nr. 3642.

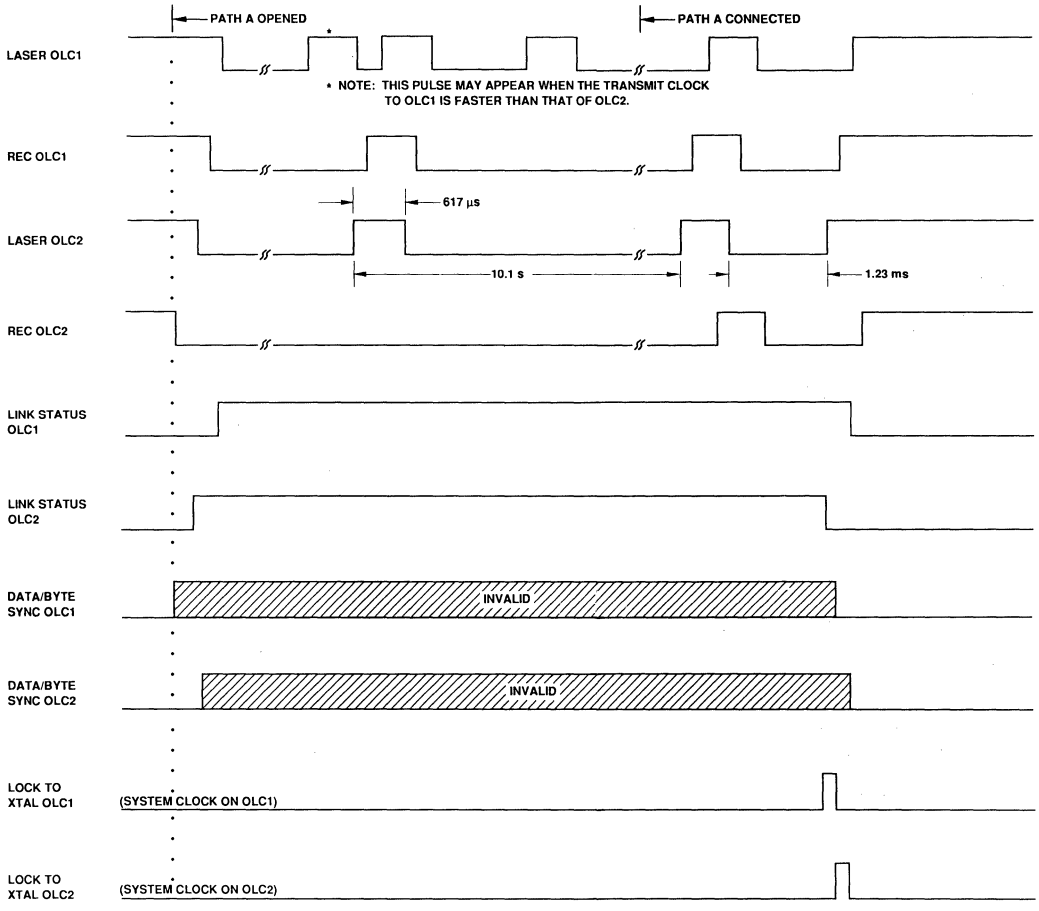


Figure 10. Open Loop Fiber Control Sequence.

Notes:

1. Launched optical power is measured at the end of a 2 m section of a 50/125 μm fiber with a nominal NA = 0.20. The maximum and minimum of the allowed range of average transmitter power coupled into the fiber are worst case values to account for manufacturing variances, drift due to temperature variations, and aging effects; and operation within the specified minimum value of extinction ratio.
2. Extinction Ratio is the minimum acceptable value of the ratio of the average optical energy in a logic level one to the average optical energy in a log level zero measured under fully modulated conditions in the presence of worst case reflections.
3. RIN_{12} is the laser noise measured relative to average optical power with 12 dB return loss.
4. Eye opening is the portion of the bit time which is error free for a given bit error rate (BER). The Fiber Channel standard for BER is $< 10^{-12}$. The general laser transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram. These characteristics include rise time, fall time, pulse overshoot, pulse undershoot, and ringing, all of which should be controlled to prevent excessive degradation of the receiver sensitivity. For the purpose of an assessment of the transmit signal, it is important to consider not only the eye opening, but also the overshoot and undershoot limitations. The parameters specifying the mask of the transmitter eye diagram are shown in Figure 11.
5. Random Jitter (RJ) is due to thermal noise which may be modeled as a Gaussian process. The peak-to-peak value of RJ is of a probabilistic nature and thus any specific value requires an associated probability.

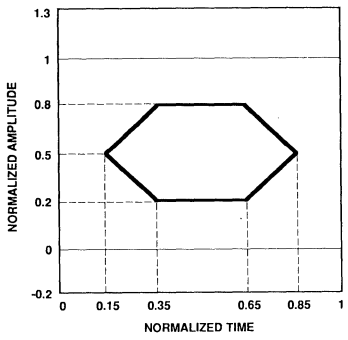


Figure 11. Eye Diagram.

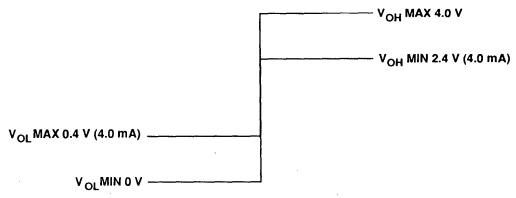


Figure 12. Receive Clock, Data and Byte Sync Driver Levels.

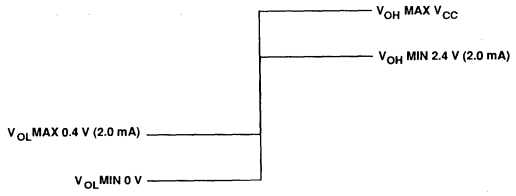


Figure 13. Link Status, Laser Fault and POR TP Driver Levels.

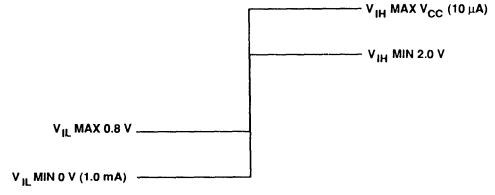


Figure 14. Transmit Data Receiver Levels.

6. The drive levels given are appropriate for Receive Data, Receiver Clock, and Byte Sync signals. The Receive Data, Receive Clock, and Byte Sync TTL drivers are push-pull totem pole drivers with a 25 Ω series resistor to dampen transmission line reflections (see Figure 12).
7. The Link Status, Laser Fault, and POR TP lines are control signals that should be treated as asynchronous lines. The drive levels for Link Status, Laser Fault, and POR TP are shown in Figure 13.
8. Figure 14 shows the receive levels for the Transmit Data lines.
9. Figure 15 shows the receive levels for the Transmit Clock.
10. Figure 16 shows the receive levels for the Loopback Enable.
11. Figure 17 shows the receive levels for the Lock to Reference and Byte Sync Enable lines.
12. Figure 18 shows the receive levels for the Link Control line.
13. The minimum and maximum values of the average received power in dBm give the input power range to maintain a BER < 10^{-12}. These values take into account power penalities caused by the use of a transmitter with worst-case combination of transmitter spectral, extinction ratio and pulse shape characteristics.
14. Optical Fiber with core diameter of 50 µm and cladding diameter of 125 µm, and a nominal Numerical Aperture of 0.20 is recommended. The modal bandwidth (-3 dB optical minimum) of the 50/125 µm fiber should be 500 MHz * km at a wavelength of 850 nm. This allows for a modal bandwidth of 400 MHz * km at 780 nm. Fiber attenuation should be 3.0 dB/km maximum at 850 nm. This allows for a fiber attenuation of 4.0 dB/km maximum at 780 nm.
15. Optical fiber with a core diameter of 62.5 µm, and a nominal Numerical Aperture of 0.275 can also be used with the HOLC-0266 OLCs. The modal

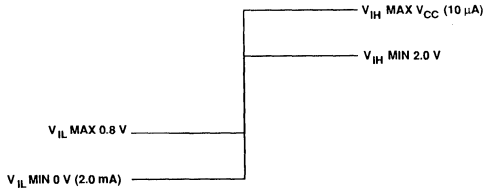


Figure 15. Transmit Clock Receiver Levels.

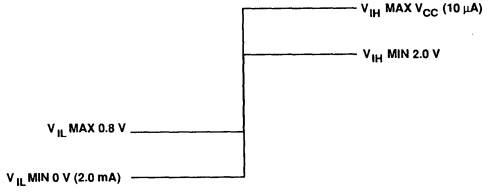


Figure 16. Loopback Enable Receiver Levels.

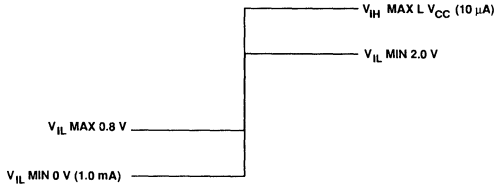


Figure 17. Lock to Reference and Byte Sync Enable Receiver Levels.

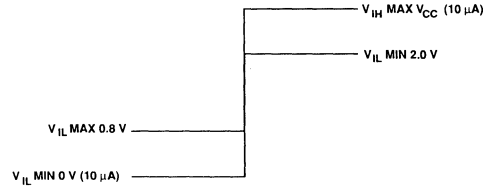


Figure 18. Link Control Receiver Levels.

bandwidth (-3dB optical minimum) should be 160 MHz * km at a wavelength of 850 nm. The length limit of 0.70 km is due to the restricted fiber bandwidth.

16. The optical interface connector dimensionally conforms to the industry standard SC type connector documented in JIS-5973. A dual keyed SC receptacle serves to align the optical transmission fiber mechanically to the OLC. The transmit side of the receptacle is color coded black, the receiver side of the receptacle is color coded yellow. See Figure 19 for a drawing of the duplex SC receptacle that is part of the OLC.

17. A possible source of the SC Duplex Cable Assembly is:
    Alcoa Fujikara Ltd.
    Telecommunications Division
    P.O. Box 5831
    Spartanburg, South Carolina 29304
    Phone# (803) 439-5160
    Fax# (803) 433-5353
    Product: SC Duplex Cable Assembly with HP Clip
    P/N: C020818

A possible source of the 48 pin connector product is:
3M Company
Electronics Product Division
P.O. Box 2963
Austin, TX 78763
Phone#: (800) 225-5373
Fax#: (800) 325-5329
Product: 48 Position, 4 Row, 100 mil Spaced Board Mount Socket Connector P/N: 962456-01-12-30

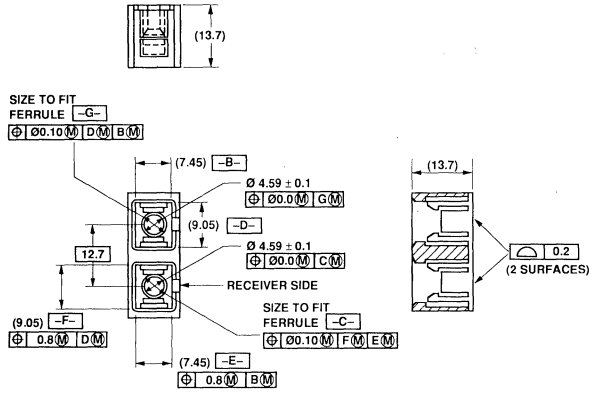


Figure 19. Duplex SC Receptacle.

Designer Kit Ordering Information

Fiber Channel 266 MBaud Optical Link Card Designer's Kits may be ordered through your local HP Components Representative or authorized HP Components distributor.

Designer Kit

Part Number	Kit Description
HOLC-K266	Two HOLC-0266 cards, 4m SC Duplex Cable Assembly, Two 48-pin electrical connectors, and literature

HEWLETT PACKARD

Silicon Bipolar Monolithic Variable Gain Amplifier

Technical Data

HPVA-0180

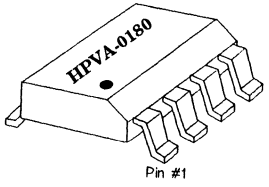
Features

- **3 dB Bandwidth: DC to 2.5 GHz**
- **Temperature Compensated Bias**
- **Single Ended or Differential Operation**
- **Low Cost Plastic Surface Mount Package**
- **Linearized Gain Control (S_{21} Magnitude)**

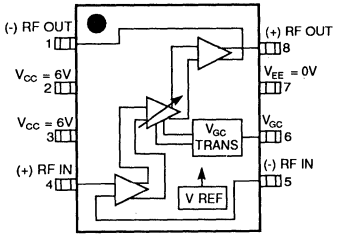
Applications

- **VHF/UHF Transceivers**
- **RF Data Links**
- **Broadband LAN's**

Plastic SO-8 Package



Functional Block Diagram and Pin Configuration



HPVA-0180
Absolute Maximum Ratings, T_A = 25°C*

Device Voltage, V_{CC} ..... 7 Volts
RF Input Power, P_{in} ..... +10 dBm
Gain Control Voltage, V_{GC} ..... 0 Volts to V_{CC}
Junction Temperature, T_j ..... +150°C
Storage Temperature, T_{stg} ..... -55° to +150°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

Care should be taken to prevent Electro Static Discharge (ESD) that could permanently damage the device. (Class II sensitivity)

Notes:
1. A θ_{JA} of 200°C/W should be used for derating and junction temperature calculations: $T_J = (P_D \times \theta_{JA}) + T_A$
2. Maximum soldering temperature is 260°C for 5 seconds.

Description

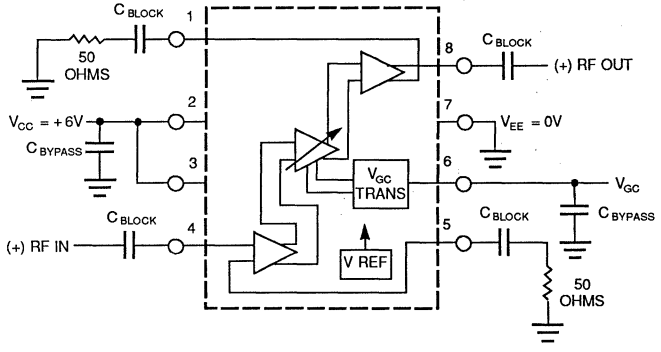
The HPVA-0180 is a silicon monolithic variable gain amplifier in a plastic surface mount SO-8 package. It is designed for wide or narrow bandwidth applications from DC to 2.5 GHz. The amplifier provides 20 dB gain (26 dB in differential operation) with 20 dB gain control over its entire DC to 2.5 GHz bandwidth, and dissipates only 250 mW from a single 6 volt power supply. The device may be operated in any combination of single-ended or differential input/output configurations.

The internal signal path of the amplifier is fully differential to achieve the highest possible immunity against transition noise. The HPVA-0180 also features a band-gap voltage reference to stabilize the bias against temperature variations and a gain control linearizer for linear gain change with gain control voltage variation.

The device is manufactured using Hewlett-Packard's 13 GHz F_t, 25 GHz F_{max} silicon bipolar integrated circuit process.

Electrical Specifications, T_A = 25°C

Symbol	Parameters / Test Conditions: V_{CC} = 6 V, Z_o = 50 Ohms, Single Ended Operation, Gain Set = +20 dB	Units	Min.	Typ.	Max.
G	Small Signal Gain $\|S_{21}\|^2$, V_{GC} = 5 Volts, f = 300 MHz	dB		21	
F_{3dB}	3 dB Bandwidth	GHz		2.5	
V_{GC}	Gain Control Range f = 300 MHz, V_{GC} = 3 to 5 Volts	dB		20	
P_{1dB}	Output Power at 1 dB Gain Comp. f = 300 MHz	dBm		-3	
IP_3	Output 3rd Order Intercept Point, F1 = 300 MHz, F2 = 305 MHz	dBm		7	
NF	50 Ohm Noise Figure f = 300 MHz	dB		16	
VSWR	Input VSWR V_{GC} = 3 to 5 Volts, f = 10 MHz to 2,000 MHz			1.8	
	Output VSWR V_{GC} = 3 to 5 Volts, f = 10 MHz to 2,000 MHz			1.8	
$\|S_{12}\|^2$	Isolation, $\|S_{12}\|^2$, f = 300 MHz	dB		32	
ΔG	Gain Flatness f = 10 MHz to 2,000 MHz	dB		±0.8	
I_{CC}	Supply Current	mA	30	41	60
I_{GC}	Gain Control Supply Current	mA		0.1	



Transmission lines (50 ohms) are recommended for all RF input and output connections. The use of chip capacitors and chip resistors will minimize unwanted parasitics.

Typical Biasing Configuration

HPVA-0180 Typical S-Parameters

Z_O = 50 Ohms, T_A = 25° C, V_{CC} = 6 V, V_{GC} Set for Nominal +20 dB Gain.

Frequency	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
10	0.23	0	20.3	10.38	-2	-44.3	0.007	-34	0.09	2
50	0.24	-4	20.2	10.23	-9	-39.3	0.011	-113	0.10	7
100	0.21	-3	20.3	10.31	-17	-40.9	0.009	68	0.12	29
200	0.23	-3	20.2	10.25	-35	-33.7	0.021	56	0.16	26
300	0.19	-9	20.1	10.05	-53	-32.0	0.025	38	0.20	23
400	0.14	-1	19.8	9.75	-70	-27.0	0.045	23	0.20	17
500	0.15	18	19.4	9.32	-87	-27.7	0.041	15	0.24	16
600	0.18	29	19.0	8.94	-102	-26.5	0.047	3	0.29	0
700	0.25	31	18.7	8.65	-116	-27.7	0.041	-30	0.28	-21
800	0.28	23	18.8	8.66	-130	-29.2	0.035	-31	0.27	-43
900	0.30	11	19.0	9.88	-145	-31.8	0.026	-61	0.24	-66
1,000	0.28	-3	19.0	8.91	-161	-30.7	0.029	-76	0.21	-90
1,100	0.27	-15	19.3	9.24	-178	-40.9	0.009	-47	0.16	-109
1,200	0.23	-25	19.4	9.33	166	-37.3	0.014	-21	0.14	-110
1,300	0.20	-32	19.4	9.35	149	-36.3	0.015	3	0.15	-125
1,400	0.14	-34	19.6	9.59	132	-31.1	0.028	10	0.16	-142
1,500	0.12	-42	19.5	9.45	115	-30.1	0.031	-13	0.15	-156
1,600	0.09	-37	19.5	9.40	97	-28.3	0.039	0	0.15	-168
1,700	0.10	-10	19.3	9.21	79	-28.2	0.039	-16	0.14	-168
1,800	0.10	-14	19.5	9.45	62	-25.9	0.051	-32	0.11	-179
1,900	0.11	-21	19.4	9.29	45	-24.7	0.058	-46	0.16	174
2,000	0.12	-54	19.6	9.58	28	-24.1	0.062	-62	0.17	167
2,100	0.10	-68	19.9	9.85	9	-25.6	0.053	-49	0.21	159
2,200	0.10	-83	20.0	10.00	-12	-24.3	0.061	-60	0.28	139
2,300	0.06	-163	19.8	9.79	-33	-22.7	0.073	-71	0.34	122
2,400	0.08	158	19.5	9.43	-56	-23.6	0.066	-84	0.40	105
2,500	0.11	126	18.7	8.57	-76	-25.1	0.055	-90	0.43	90
2,600	0.17	103	17.7	7.89	-95	-24.6	0.059	-101	0.44	80
2,700	0.20	84	16.7	6.80	-115	-22.8	0.072	-99	0.46	66
2,800	0.24	69	15.6	6.00	-134	-23.7	0.065	-101	0.48	61
2,900	0.29	48	14.8	5.50	-153	-21.6	0.083	-115	0.45	56
3,000	0.36	45	14.0	5.03	-169	-23.0	0.071	-125	0.42	52
3,100	0.35	27	13.1	4.50	178	-23.7	0.065	-115	0.44	52
3,200	0.38	31	12.0	4.00	162	-21.0	0.089	-119	0.39	48
3,300	0.43	27	11.3	3.67	147	-20.9	0.091	-135	0.33	47
3,400	0.48	24	10.3	3.28	130	-20.6	0.094	-144	0.32	42
3,500	0.47	23	9.2	2.88	115	-20.2	0.098	155	0.24	43
4,000	0.40	15	5.1	1.81	44	-19.0	0.112	-166	0.18	90

HPVA-0180 Typical Performance Parameters

Z_O = 50 Ohms, T_A = 25° C, V_{CC} = 6 V, V_{GC} Set for Nominal +20 dB Gain.

Frequency MHz	Linear Phase Deviation (Deg.)	Relative Phase (Deg.)	Gain Deviation (dB)	Group Delay (ns)	Input VSWR	Output VSWR
10	-0.3	0.0	0.0	0.52	1.6	1.2
50	-0.7	-10.7	-0.01	0.46	1.6	1.2
100	-1.1	-19.5	0.00	0.49	1.6	1.3
200	-2.2	-37.0	-0.01	0.49	1.6	1.4
300	-3.0	-50.9	-0.02	0.48	1.5	1.5
400	-4.0	-72.1	-0.54	0.49	1.4	1.5
500	-4.0	-88.5	-0.93	0.46	1.4	1.7
600	-2.4	-103.5	-1.30	0.42	1.5	1.8
700	0.1	-117.6	-1.58	0.39	1.7	1.8
800	2.4	-131.7	-1.57	0.39	1.8	1.7
900	3.6	-147.1	-1.35	0.43	1.8	1.6
1,000	4.0	-163.1	-1.32	0.45	1.8	1.5
1,100	3.8	-180.0	-1.00	0.47	1.8	1.4
1,200	4.3	-196.1	-0.92	0.44	1.5	1.4
1,300	4.5	-212.4	-0.91	0.46	1.5	1.4
1,400	3.6	-229.7	-0.68	0.48	1.3	1.4
1,500	2.9	-247.1	-0.82	0.48	1.3	1.4
1,600	1.8	-264.7	0.85	0.49	1.2	1.4
1,700	0.6	-282.4	-1.04	0.50	1.3	1.3
1,800	0.1	-299.4	-0.82	0.48	1.2	1.3
1,900	-0.8	-317.0	-0.96	0.48	1.2	1.4
2,000	-1.2	-334.0	-0.69	0.47	1.3	1.4
2,100	-3.8	-353.0	-0.45	0.53	1.2	1.6
2,200	-7.5	-373.4	-0.29	0.56	1.2	1.8
2,300	-13.0	-395.2	-0.51	0.61	1.1	2.1
2,400	-18.8	-417.6	-0.83	0.62	1.2	2.4
2,500	-22.0	-437.4	-1.66	0.55	1.3	2.6
2,600	-24.8	-456.7	-2.46	0.53	1.4	2.5
2,700	-27.9	-476.5	-3.67	0.55	1.5	2.8
2,800	-31.0	-495.9	-4.75	0.55	1.7	2.8
2,900	-33.5	-514.9	-5.51	0.52	1.8	2.6
3,000	-32.4	-530.5	-6.29	0.43	2.2	2.4
3,100	-29.1	543.9	-7.26	0.37	2.1	2.5
3,200	-28.6	-559.9	-8.29	0.44	2.3	2.2
3,300	-26.7	-574.8	-9.29	0.43	2.6	2.1
3,400	-27.9	-591.8	-10.01	0.46	2.8	1.8
3,500	-25.5	-606.4	-11.12	0.42	3.0	1.7
4,000	-14.0	-677.5	-15.18	0.37	2.3	1.4

HPVA-0180 Typical Parameters

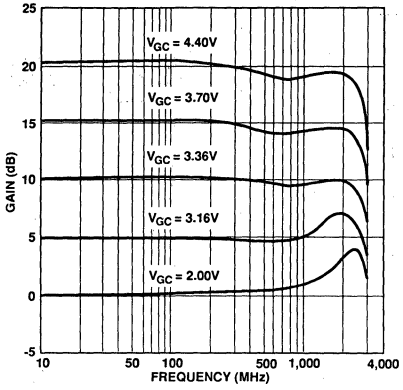


Figure 1. Typical Gain vs. Frequency over Gain Control Range at 25° C

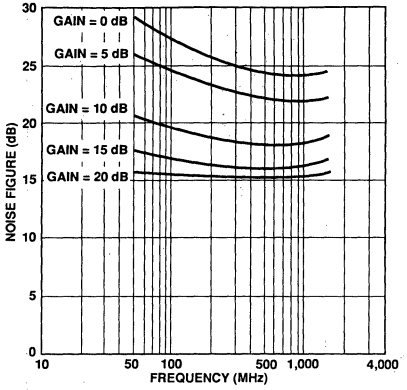


Figure 2. Typical Noise Figure vs. Frequency over Gain Control Range at 25° C

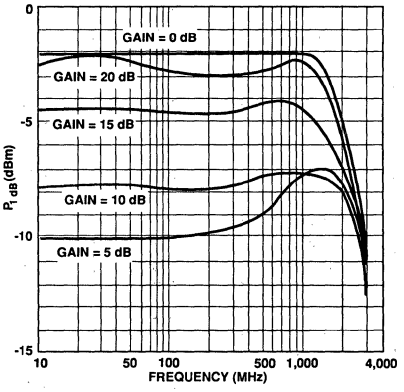


Figure 3. Typical $P_{1\ dB}$ vs. Frequency over Gain Control Range at 25° C

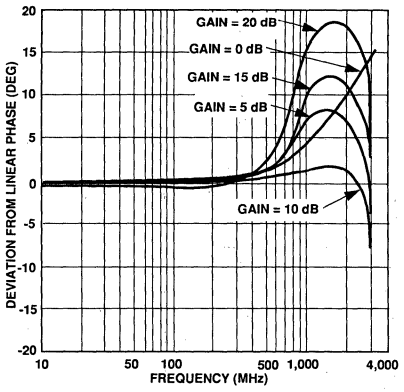


Figure 4. Typical Linear Phase vs. Frequency over Gain Control Range at 25° C

(continued)

HPVA-0180 Typical Parameters

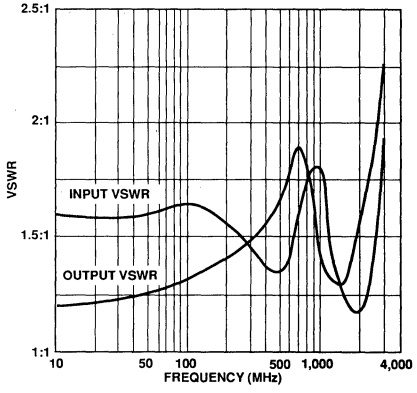


Figure 5. Typical Input and Output VSWR vs. Frequency Gain = 20 dB at 25° C

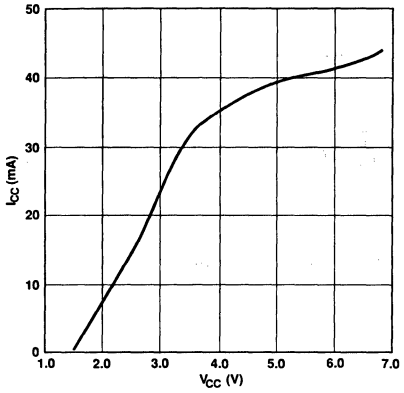


Figure 6. Typical I_{CC} vs. V_{CC} at 25°C

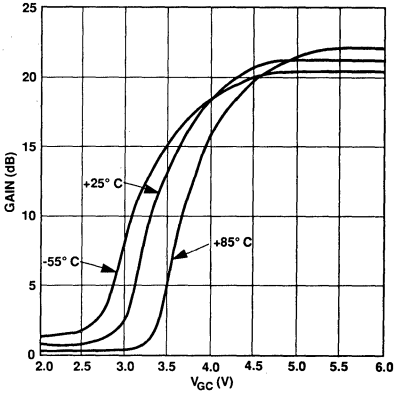


Figure 7. Typical Gain vs. V_{GC} at 300 MHz at Three Temperatures

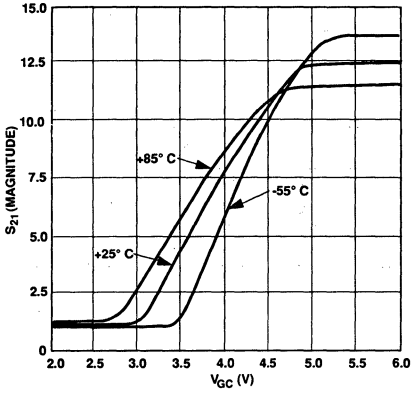


Figure 8. Typical S_{21} vs. V_{GC} at 300 MHz at Three Temperatures

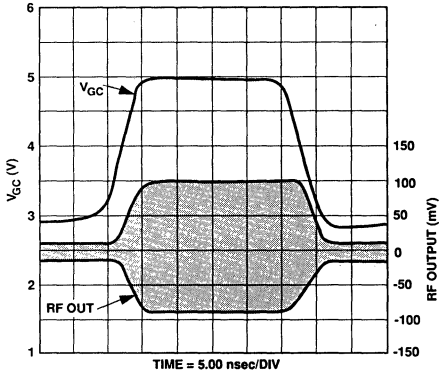


Figure 9. Typical Pulsed V_{GC} Response with RF Frequency of 100 MHz at 25°C

Theory of Operation

Figure 10 shows the simplified schematic for the HPVA-0180. The signal path is a cascade of an input buffer, a variable-gain stage, and an output buffer. The input buffer provides 50 Ω input impedance and proper bias voltage for the variable-gain stage. The variable-gain stage is the main amplifier, whose voltage gain can be adjusted by the gain-controlling voltage, V_{GC}. The output buffer has 50 Ohm output impedance and is designed to drive 50 Ohm loads. The HPVA-0180 also contains a V_{GC} translator and a band-gap voltage reference. The V_{GC} translator takes the external gain-controlling voltage, V_{GC}, and generates V_{GC1} and V_{GC2} to control the variable-gain stage. The V_{GC} translator also linearizes the HPVA-0180's gain with respect to V_{GC}. The band-gap voltage reference generates a bias voltage, V_{bias}, to drive all of the current sources in the circuit. The voltage V_{bias} is temperature compensated so that the output current of all of the current sources will remain stable over a wide temperature range.

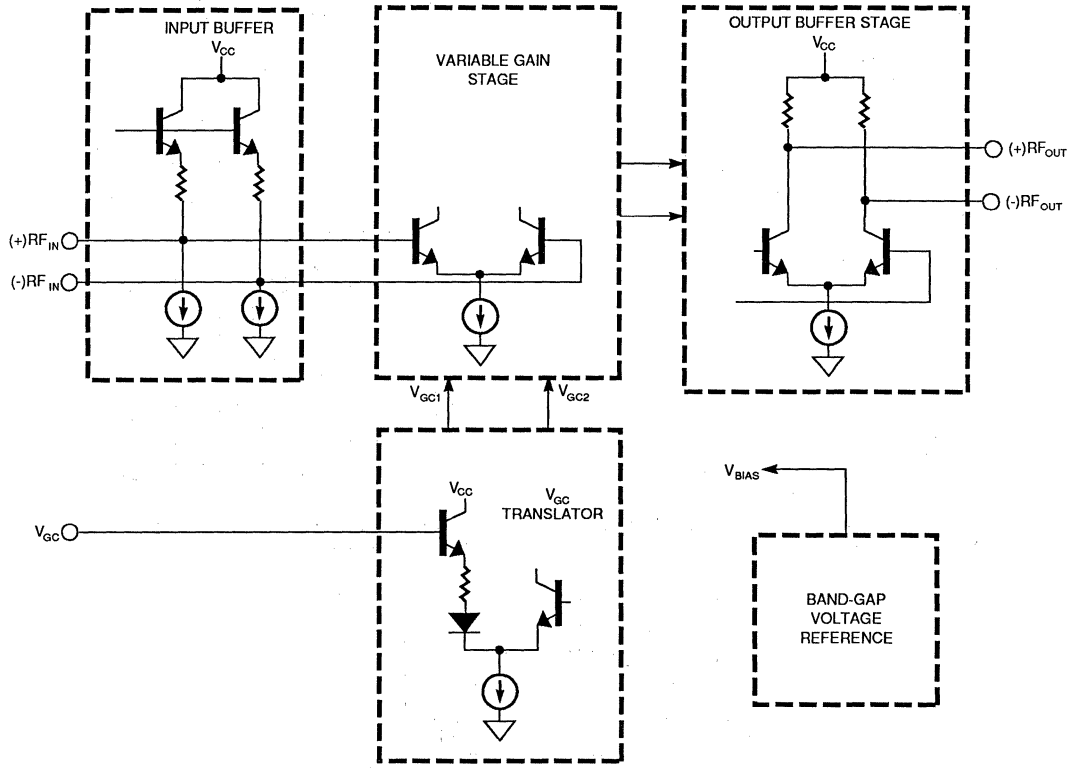
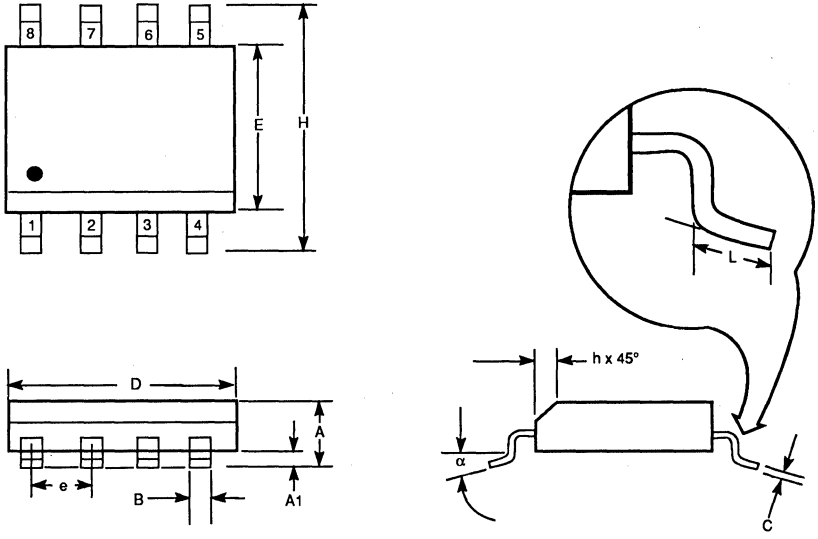


Figure 10. HPVA-0180 Simplified Schematic

Package Dimensions

Plastic SO-8 Package



Symbol	Dimensions	
	Min.	Max.
A	1.35 (0.053)	1.75 (0.068)
A1	0.10 (0.004)	0.25 (0.0098)
B	0.35 (0.0138)	0.49 (0.0192)
C	0.19 (0.007)	0.25 (0.0098)
D	4.80 (0.189)	5.00 (0.197)
E	3.80 (0.150)	4.00 (0.157)
e	1.27 BSC (0.050)	
H	5.80 (0.228)	6.20 (0.244)
h	0.25 (0.010)	0.50 (0.020)
L	0.40 (0.016)	1.27 (0.050)
α	0°	8°

Meets JEDEC outline dimensions.
Dimensions are in millimeters (inches)

HEWLETT PACKARD

IDA-07318
MagIC™ Silicon Bipolar MMIC
1.5 Gb/s Laser Diode Driver

Features

- **High Data Rates: 1.5 Gb/s NRZ**
- **High Modulation Current: 50 mA**
- **High Prebias Current: 50 mA**
- **Low VSWR 50 Ω Input, ECL Level Compatible**
- **Differential or Single-ended Inputs**
- **Separate Modulation and Prebias Controls**
- **Single Power Supply: +5 V or -5.2 V**
- **Hermetic Glass-metal Surface Mount Package**

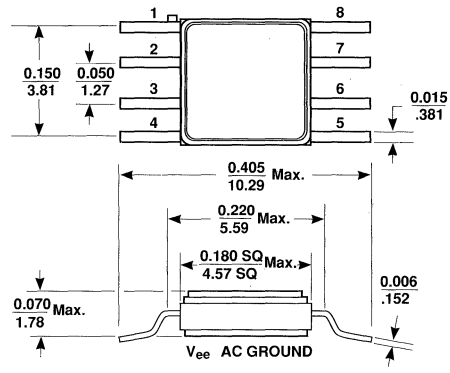
Description

The IDA-07318 is a wideband silicon bipolar Monolithic Microwave Integrated Circuit (MMIC), Laser Diode (LD) driver, housed in a miniature glass-metal hermetic surface mount package. It is designed to provide high speed current drive for laser diodes or light emitting diodes (LEDs). On-chip termination resistors and flexible prebias and modulation control inputs simplify your design.

Typical applications include fiber optic data communications (e.g., FDDI, serial HIPPI) and telecommunications (e.g., SONET) systems where high speed laser diodes are used with data rates up to 1.5 Gb/s. In addition, instrumentation and communication circuits can use the high speed current modulation feature of the IDA-07138.

The IDA series of laser diode drivers is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} ISOSAT™-1 silicon bipolar process that uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metalization, and polyimide inter-metal dielectric and scratch protection to achieve excellent performance uniformity, and reliability.

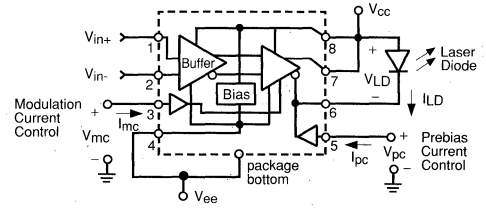
180 mil Package

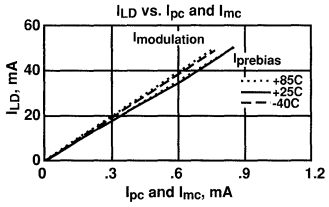


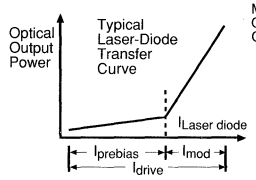
PIN DESCRIPTION	
1 V_{in+}	8 V_{CC}
2 V_{in-}	7 Output Current-
3 Mod, Input	6 Output Current+ (to LD)
4 V_{ee}	5 Prebias Input
Bottom of Package is V_{ee}	

Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
in .xxx = ±.005
mm .xx = ±.13

Functional Block Diagram







Guaranteed Electrical Specifications, T_A = 25°C, V_{cc} = 0 V, V_{ee} = -5.2 V, Z Load = 12 Ω (see Test Configuration)

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
t_r	Output Rise Time, 20% to 80% (Pin 6)	I_{mod} = 25 mA, I_{pb} = 50 mA	ps		220	300
t_f	Output Fall Time, 20% to 80% (Pin 6)	I_{mod} = 25 mA, I_{pb} = 50 mA	ps		240	320
I_{pb}	Laser Diode Prebias Current Set Range		mA	0-50		
I_{mod}	Laser Diode Modulation Current Set Range[1]		mA	5-50		
I_d	Device Current	V_{cc} - V_{cc} = 5 V, I_{mod} = 0 mA, I_{pb} = 0 mA		30	40	50

Notes: 1. Recommended operating range for Modulation Current Set is 10 to 50 mA.

Design Information, T_A = 25°C, V_{cc} = 0 V, V_{ee} = -5.2 V, Z Load = 12 Ω (see Test Configuration)

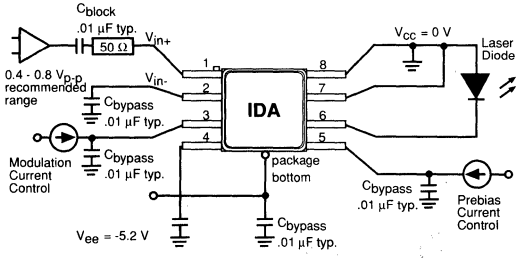
Symbol	Parameters and Test Conditions		Units	Typ.
τ_p	Propagation Delay Time, Input to Output	I_{mod} = 25 mA	ps	300
BW	Small Signal -3 dB Bandwidth	I_{mod} = 25 mA	GHz	1.0
VSWR	V_{in}+, V_{in}- VSWR	f = 0.1 to 2 GHz		2:1
$t_{r\,pb}$, $t_{r\,mod}$	Modulation or Prebias Current Output Rise Time (Inputs Pin 3 or 5)		ns	6

Absolute Maximum Ratings

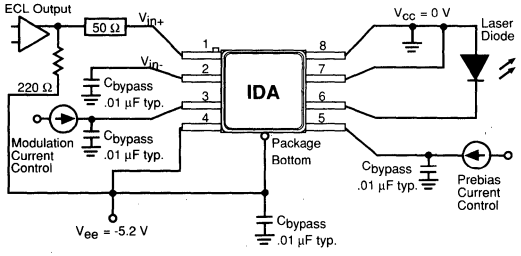
Parameter	Absolute Maximum[1]
Device Voltage	10 V
Power Dissipation[2, 3]	2.5 W
I_{mod} or I_{pb}	150 mA rms
Junction Temperature	200°C
Storage Temperature	-65 to 200°C
Thermal Resistance[2]: θ_{jc}	50°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{case} = 25°C
3. Derate at 20 mW/°C for T_C > 75°C

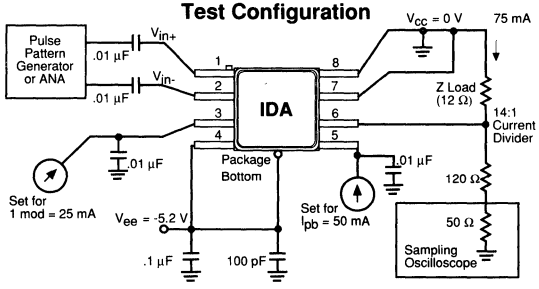
Typical Use: AC Coupled, Single-ended 50Ω Input



Typical Use: DC Coupled, Single-ended ECL Input

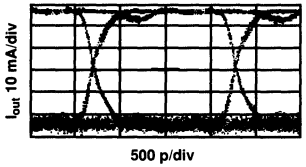


Test Configuration

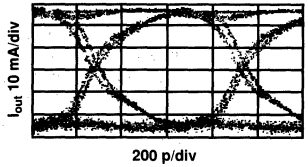


Typical Performance, T_A = 25°C
V_{CC} = 0 V, V_{EE} = 5.2 V, R_L = 12 Ω
(unless otherwise noted)

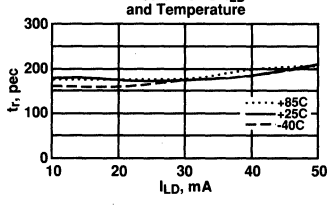
Eye Diagram, 622 Mb/s



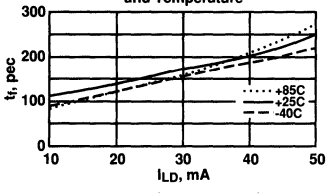
Eye Diagram, 1.5 Gb/s



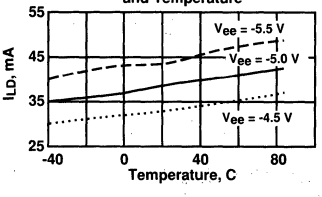
Rise Time vs. I_{LD} and Temperature



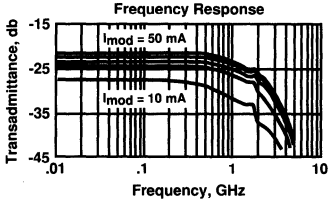
Fall Time vs. I_{LD} and Temperature



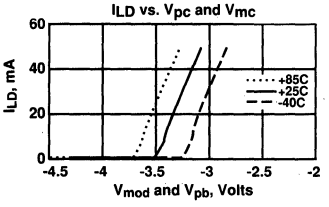
I_{device} vs. Power Supply and Temperature



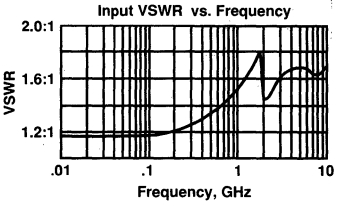
Frequency Response



I_{LD} vs. V_{pc} and V_{mc}



Input VSWR vs. Frequency



FIBER OPTICS

HEWLETT PACKARD

IDC-51418
MagIC™ Silicon Bipolar MMIC
1.5 Gb/s Decision Circuit

Features

- **High Data Rates: 1.5 Gb/s NRZ**
- **Input Sensitivity < 20 mVpp Typical**
- **ECL Voltage Swing Compatible C-Input and Q-Outputs**
- **Single Ended or Differential C and D Inputs**
- **Single Power Supply: +5 V or -5.2 V**
- **Low Power: 450 mW Typical Dissipation**
- **Hermetic Glass-metal Surface Mount Package**

Description

The IDC-51418 is a high speed silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) decision circuit, housed in a miniature glass-metal hermetic, surface mount package. It is designed for data communications and LAN applications. Other uses include wide bandwidth communications and digital circuits, such as comparators and D type flip-flops. The IDC-51418 is a master-slave D type flip-flop with a high gain data preamplifier for increased sensitivity. Both the data and clock inputs can be driven differentially or single ended. The bias and input matching circuits are included on-chip.

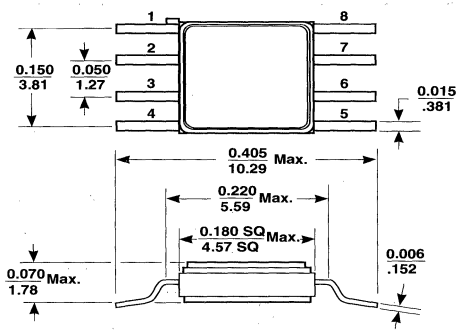
The IDC series of high speed decision circuits is fabricated using HP's 10 GHz, f_T, 25 GHz f_{MAX} ISOSAT™-1 silicon bipolar process that uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization, and polyimide inter-metal dielectric and scratch protection to achieve excellent performance uniformity, and reliability.

Truth Table

Input		Output	
Cn	Dn	Qn +1	$\overline{Qn+1}$
⎍	x	Qn	$\overline{Qn}$
⎎	0	0	1
⎎	1	1	0

Cn: Clock State at t = n
Dn: Data State at t = n
Qn: Output state at t = n
Qn +1: Output state at t = n +1

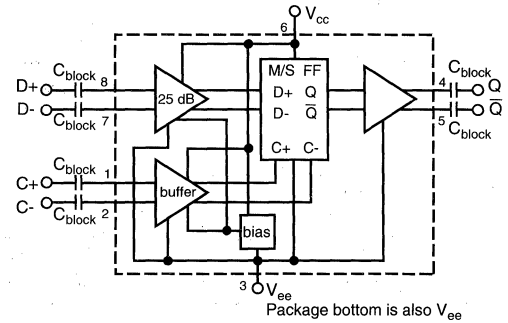
180 mil Package



PIN DESCRIPTION	
1 C+	8 D+
2 C-	7 D-
3 V_{ee}	6 V_{cc}
4 Q	5 $\overline{Q}$
Bottom of Package is V_{ee}	

Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
in .xxx = ±.005
mm .xx = ±.13

Functional Block Diagram



Package bottom is also V_{ee}

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions: V_{cc} = 5 V, V_{ee} = 0 V, R_L = 50 Ω		Units	Min.	Typ.	Max.
t_r	Q Output Rise Time, 10% to 90%	1.5 Gb/s	ps		200	
t_f	Q Output Fall Time, 90% to 10%	1.5 Gb/s	ps		190	
V_{in} (D+,D-)	Minimum Data Input Amplitude (single ended), BER = 10^{-9}	1.5 Gb/s	mVpp		20	40
CPM	Clock Phase Margin	1.5 Gb/s	deg		335	
F_b max	Maximum Data Rate (NRZ Operation)	V_{in} = 40 mV_{pp}	Gb/s	1.2	1.5	
V_{ck}(C+,C-)	Clock Input Amplitude (single ended)		mVpp		600	
V_o(Q, $\overline{Q}$)	Output Voltage		mVpp	650	800	
t_{pd}	Propagation Delay Time, Falling Clock Edge to Q Output		ps		500	
t_{setup}	Setup Time (see Timing Diagram)		ps		-25	
t_{hold}	Hold TIme (see Timing Diagram)		ps		60	
VSWR	Clock and Data Input VSWR	f = .01-1.5 GHz			1.3:1	
VSWR	Q, $\overline{Q}$ Output VSWR	f = .01-1.5 GHz			2.0:1	
I_d	Quiescent Device Current		mA	75	95	115

The recommended Power Supply Voltage range ($V_{cc} - V_{ee}$) for this device is 4.5 to 5.5 V.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	8 V
Power Dissipation[2, 3]	800 mW
C or D Input	2 Vpp
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

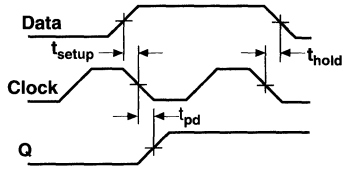
Thermal Resistance[2]: θ_{jc} = 55°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. Derate at 18 mW/°C for T_{case} > 156°C

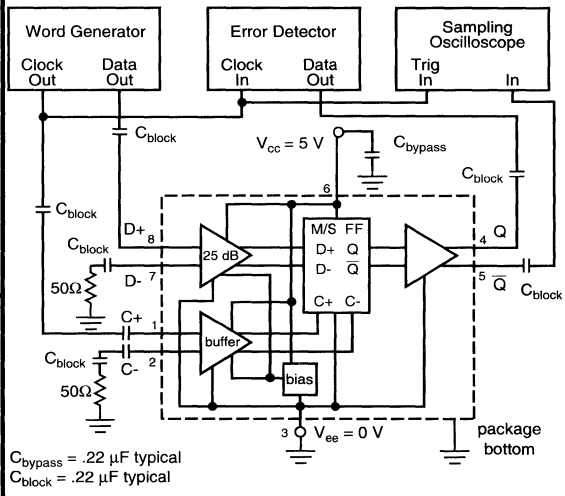
Typical Performance, T_A = 25°C, V_{cc} = 5 V, V_{ee} = 0 V, R_L = 50 Ω

(unless otherwise noted)

Timing Diagram



Test Configuration
Single Ended Input/Single Ended Output

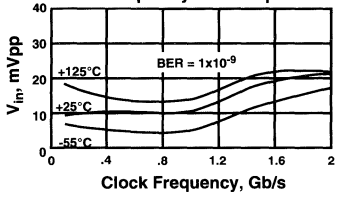


Notes: For transparent (non-latched comparator) operation, AC couple pins 1, 2 (C+, C-) to ground.

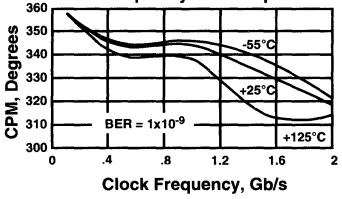
Good RF ground of Pin 3 and package bottom is critical for proper operation and good VSWR performance of this part.

FIBER OPTICS

Data Input Sensitivity vs. Clock Frequency and Temperature



Input Clock Phase Margin vs. Clock Frequency and Temperature



Quiescent Input/Output Voltages (Inputs terminated, offset voltages = 0 V)

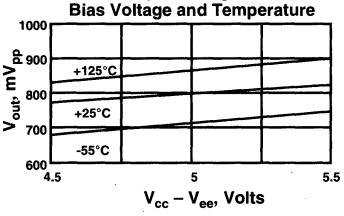
$V_{cc} - V_{ee}$	D	C	Q
5.0 V	5.0 V	3.8 V	3.4 V
-5.2 V	0.0 V	-1.2 V	-1.6 V

Note: Small offset voltages between D+ and D- will cause Q ($\overline{Q}$) to go to a high (Vcc -.2 V) or low (Vcc -1.2 V) state.

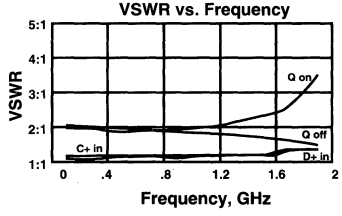
Output Voltages in the Latched (on/off) State

$V_{cc} - V_{ee}$	Q (V_{OH})	$\overline{Q}$ (V_{OL})
5.0 V	4.8 V	3.8 V
-5.2 V	-.2 V	-1.2 V

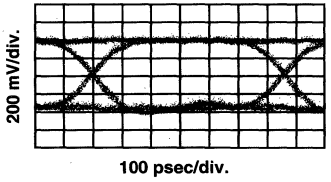
Output Voltage vs. Bias Voltage and Temperature



VSWR vs. Frequency



Output Eye Diagram at 1.5 Gb/s (Pseudorandom pattern = 2^{23} -1)



HEWLETT PACKARD

ITA-12300, ITA-12318
MagIC™ Silicon Bipolar MMIC
0.8 Gb/s Transimpedance Amplifier

Features

- **High Transimpedance Gain: A_Z = 4200 Ω (72.5 dB)**
- **High Data Rates: 0.8 Gb/s NRZ**
- **Wide Band width: 900 MHz (Chip)**
  750 MHz (Packaged)
- **Low Noise: 2.8 pA/√Hz at 100 MHz**
- **Single Power Supply: +5 V or -5.2 V**
- **Low Power Consumption: 210 mW**
- **Available in Chip Form and Hermetic Glass–Metal Surface Mount Package**

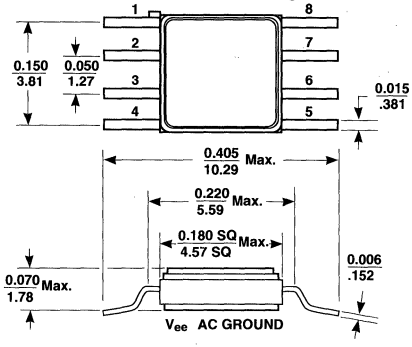
Description

The ITA-123 series of high-performance transimpedance amplifiers is available in either chip form, ITA-12300 or housed in a miniature glass-metal hermetic surface-mount package, ITA-12318. These devices are designed for use in fiber-optic receivers that require high transimpedance gain, wide bandwidth, reduced power consumption, and low noise.

Typical applications include fiber-optic systems such as high-speed data communications, point to point (Fiber Channel), networks (LAN, MAN), and telecommunications (SONET) with data rates up to 0.8 Gb/s.

The ITA series of transimpedance amplifiers is fabricated using HP's 10 GHz f_T, 25 GHz f_{max} ISOSAT™-1 silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metalization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability. The recommended assembly procedure for the ITA-12300 chip is gold eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil. gold wire.[1]

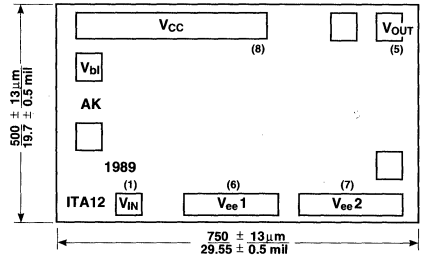
180 mil Package



PIN DESCRIPTION			
1	Input	8	V_{CC}
2	V_{ee}, AC Ground	7	V_{ee}
3	V_{ee}, AC Ground	6	V_{ee}
4	NC	5	V_{out}
Bottom of Package is V_{ee} (AC Ground)			

Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
   in .xxx = ±.005
   mm .xx = ±.13

ITA-12300 Chip Outline



Chip Thickness is 140 µm / 5.5 mil. (nominal)
Bond Pads are 50 µm / 1.97 mil. (nominal)

Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: V_{CC} = 5V, V_{ee} = 0V, Z_L = 50 Ω		Units	ITA-12318 180 mil. Min.	Typ.	Max.	ITA-12300[3] 00 (Chip) Min.	Typ.	Max.
A_Z	Transimpedance Gain	f = 100 MHz	ohms	3800	4200			4200	
F_{3dB}	Small Signal -3 dB Bandwidth[4, 5]		MHz	600	750			900	
ΔA_Z	Frequency Response Gain Peak[4, 5]		dB		0.2	0.7		0.2	
I_n	Input Current Noise Spectral Density[4]	f = 100 MHz	pA/√Hz		2.8			2.8	
V_{op-p}	Output Voltage Swing (peak to peak)	f = 50 MHz	V_{p-p}		1.2			1.2	
VSWR	Output VSWR	f = 50 to 1000 MHz			2:1			2:1	
I_{MAX}	Maximum Input Current Before Input Overload[6]	f = 50 MHz	μA_{p-p}		400			400	
I_d	Device Quiescent Current		mA	30	43	55	30	43	55
V_{in}	Input Quiescent Voltage (Pin 1)		Vdc		2.2			2.2	
V_{OUT}	Output Quiescent Voltage (Pin 5)		Vdc		2.2			2.2	

Notes:
1. See Application Note, "AN-A005: Transistor Chip Use" for additional information.
2. The recommended operating voltage range for this device is 4.75 to 5.5 V.
3. RF performance of chip is determined by testing 10 devices per wafer in a 180 mil package.
4. Assumes photodiode capacitance, C_{PD},<0.5 pF.
5. Referenced from 100 MHz.
6. Input overload is defined as output duty cycle distortion ≥ ±10%.

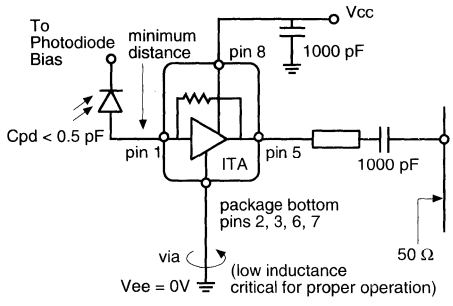
Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	8 V
Power Dissipation[2, 3]	700 mW
V_{in}-V_{ee}	3.0 V
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

Thermal Resistance: θ_{jc} = 50°C/W (ITA-12318)
θ_{jc} = 25°C/W (ITA-12300)

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{case} = 25°C (ITA-12318), $T_{mounting\ surface}$ = 25°C (ITA-12300)
3. Derate at 20 mW/°C for T_{case} > 165°C (ITA-12318)
   Derate at 40 mW/°C for $T_{mounting\ surface}$ > 182°C (ITA-12300)

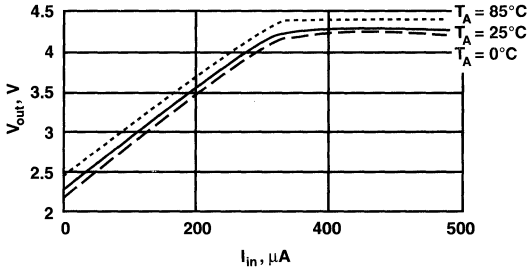
ITA-12318 Typical Biasing Configuration and Functional Block Diagram



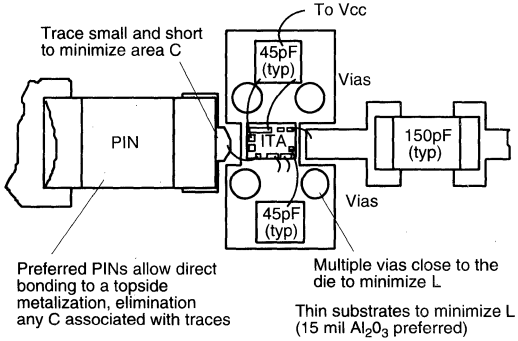
Typical Performance, T_A = 25°C, V_{cc} = 5V, V_{ee} = 0V, Z_L = 50 Ω, C_{PD} < 0.5 pF

(Unless otherwise noted)

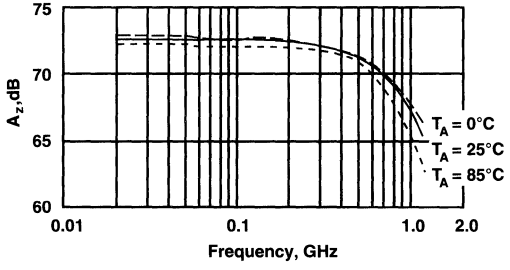
ITA-12300/ITA-12318 DC Input/Output Characteristics No Load



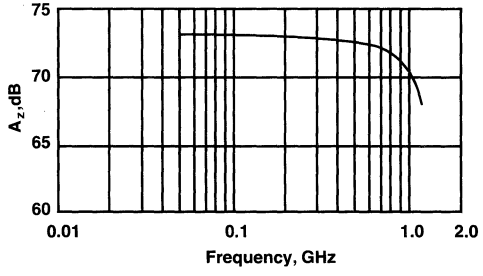
ITA-12300 Circuit Layout



ITA-12318 Typical Transimpedance Gain vs. Frequency

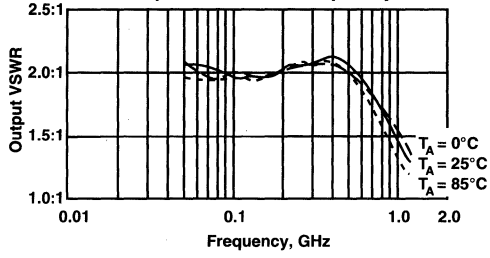


ITA-12300 Typical Transimpedance Gain vs. Frequency

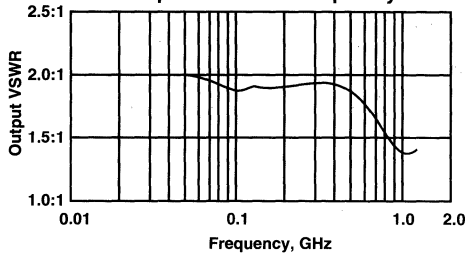


FIBER OPTICS

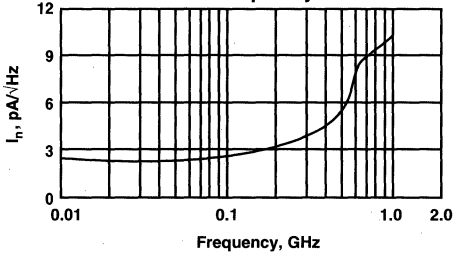
ITA-12318
Output VSWR vs. Frequency



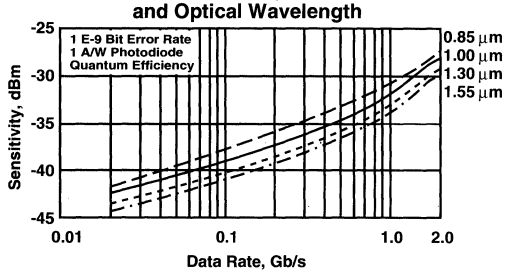
ITA-12300
Output VSWR vs. Frequency



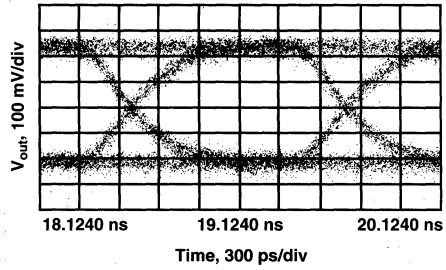
ITA-12300/ITA-12318
Equivalent Input Current Noise vs. Frequency



ITA-12300/ITA-12318
Calculated Sensitivity vs. Data Rate and Optical Wavelength



ITA-12318
Eye Diagram, 622 Mb/s
Photo current = 100 µA P-P, PRBS = 2^{31} - 1



Typical ITA-12318 Scattering Parameters: $Z_O = 50\ \Omega$

$T_A = 25°C$, Vcc = 5 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
50	.57	-1.0	31.70	38.57	-10.0	-49.50	.003	-131.0	.36	164.0	2.23
100	.57	1.0	31.50	37.60	-22.0	-49.60	.003	18.0	.33	160.0	2.65
150	.59	2.0	31.20	36.14	-32.0	-55.00	.002	-59.0	.33	157.0	4.68
200	.60	2.0	30.70	34.32	-41.0	-64.00	.001	148.0	.34	151.0	12.92
250	.62	1.0	30.40	32.91	-50.0	-55.50	.002	-32.0	.34	144.0	5.15
300	.63	0.0	30.00	31.58	-59.0	-56.80	.002	-83.0	.35	137.0	5.37
350	.63	-2.0	29.60	30.29	-66.0	-55.80	.002	-26.0	.35	129.0	5.55
400	.64	-3.0	29.30	29.21	-74.0	-57.10	.001	74.0	.35	122.0	6.47
450	.65	-4.0	29.00	28.25	-81.0	-54.80	.002	-135.0	.35	115.0	4.84
500	.65	-5.0	28.80	27.52	-89.0	-66.60	0.000	145.0	.35	106.0	9.06
550	.65	-7.0	28.60	26.85	-96.0	-57.50	.001	20.0	.35	98.0	7.30
600	.65	-8.0	28.40	26.26	-104.0	-52.40	.002	114.0	.33	90.0	4.03
650	.65	-9.0	28.20	25.52	-112.0	-61.30	.001	-56.0	.33	83.0	11.82
700	.65	-10.0	27.90	24.91	-120.0	-53.40	.002	-169.0	.31	72.0	4.73
750	.65	-11.0	27.70	24.17	-128.0	-62.70	.001	-117.0	.29	63.0	15.10
800	.65	-12.0	27.50	23.57	-136.0	-54.90	.002	155.0	.27	52.0	6.21
850	.65	-13.0	27.20	22.78	-144.0	-47.40	.004	177.0	.25	40.0	2.69
900	.65	-14.0	26.90	22.05	-153.0	-64.50	.001	-168.0	.23	28.0	20.61
950	.65	-15.0	26.40	20.86	-161.0	-49.60	.003	131.0	.21	15.0	3.96
1000	.65	-15.0	26.10	20.15	-169.0	-61.40	.001	-167.0	.18	4.0	16.16
1050	.65	-16.0	25.60	19.07	-177.0	-55.40	.002	-176.0	.17	-12.0	8.57
1100	.65	-16.0	25.10	18.04	175.0	-50.10	.003	144.0	.15	-24.0	4.96
1150	.65	-17.0	24.60	17.06	168.0	-44.80	.006	157.0	.14	-41.0	2.82
1200	.65	-18.0	24.10	16.05	160.0	-47.20	.004	163.0	.12	-58.0	4.01

Typical ITA-12300 Scattering Parameters: $Z_O = 50\ \Omega$

$T_A = 25°C$, Vcc = 5 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
50	.52	-2.0	32.40	41.51	-9.0	-48.00	.004	1.0	.35	171.0	2.20
100	.53	2.0	32.20	40.62	-19.0	-69.80	0.000	-159.0	.34	169.0	7.67
150	.54	4.0	31.90	39.43	-28.0	-52.20	.002	-97.0	.35	166.0	3.19
200	.55	4.0	31.60	38.21	-37.0	-57.60	.001	86.0	.35	162.0	6.18
250	.56	4.0	31.30	36.65	-45.0	-62.20	.001	29.0	.35	157.0	10.77
300	.58	4.0	31.00	35.31	-52.0	-54.60	.002	48.0	.35	151.0	4.65
350	.58	4.0	31.00	34.26	-60.0	-53.20	.002	43.0	.35	145.0	4.10
400	.59	3.0	30.40	33.17	-67.0	-67.00	0.000	95.0	.34	138.0	8.79
450	.60	2.0	30.20	32.16	-74.0	-60.90	.001	-96.0	.33	132.0	9.69
500	.61	2.0	29.90	31.31	-81.0	-53.70	.002	164.0	.32	125.0	4.28
550	.61	2.0	29.70	30.57	-88.0	-58.70	.001	-175.0	.31	117.0	7.82
600	.62	1.0	29.50	29.77	-95.0	-58.90	.001	-7.0	.29	110.0	8.54
650	.62	0.0	29.20	28.93	-103.0	-48.10	.004	-139.0	.27	101.0	2.37
700	.63	0.0	29.00	28.20	-110.0	-49.70	.003	159.0	.25	92.0	3.02
750	.63	-1.0	28.70	27.36	-117.0	-55.00	.002	41.0	.23	82.0	5.99
800	.63	-1.0	28.40	26.30	-125.0	-46.40	.005	136.0	.20	72.0	2.27
850	.64	-2.0	28.10	25.26	-133.0	-47.30	.004	164.0	.18	59.0	2.60
900	.64	-3.0	27.70	24.21	-140.0	-52.20	.002	179.0	.15	47.0	4.76
950	.64	-3.0	27.30	23.20	-147.0	-45.60	.005	161.0	.13	31.0	2.37
1000	.64	-4.0	26.80	21.81	-155.0	-45.50	.005	-178.0	.11	12.0	2.48
1050	.65	-4.0	26.40	20.85	-161.0	-43.20	.007	125.0	.10	-6.0	2.01
1100	.65	-5.0	25.90	19.64	-169.0	-45.20	.006	157.0	.10	-32.0	2.64
1150	.65	-5.0	25.30	18.45	-175.0	-45.60	.005	166.0	.10	-52.0	2.96
1200	.65	-6.0	24.80	17.30	178.0	-44.50	.006	153.0	.11	-65.0	2.75

HEWLETT PACKARD

ITA-06300
MagIC™ Silicon Bipolar MMIC
1.5 Gb/s Transimpedance Amplifier Chip

Features

- **High Transimpedance Gain: A_Z = 2800 Ω (69 dB)**
- **High Data Rates: 1.5 Gb/s NRZ**
- **Wide Bandwidth: 1.5 GHz**
- **Low Noise: 3.5 pA/√Hz at 100 MHz**
- **Single Power Supply: +5 V or -5.2 V**
- **Low Power Consumption: 170 mW**

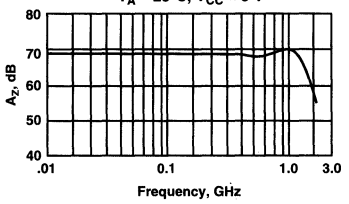
Description

The ITA-06300 series of high-performance transimpedance amplifier chip. It is designed for use in fiber-optic receivers that require high transimpedance gain, wide bandwidth, reduced power consumption, and low noise.

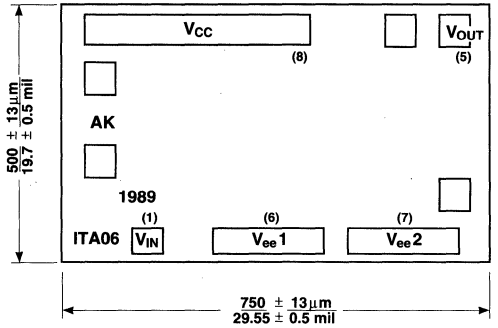
Typical applications include fiber-optic systems such as high-speed data communications, point to point (Fiber Channel), networks (LAN, MAN), and telecommunications (SONET) with data rates up to 1.8 Gb/s.

The ITA series of transimpedance amplifiers is fabricated using HP's 10 GHz f_T, 25 GHz f_{max} ISOSAT™-1 silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metalization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability. The recommended assembly procedure is gold eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil. gold wire.[1]

Typical Transimpedance Gain vs. Frequency
T_A = 25°C, V_{CC} = 5 V

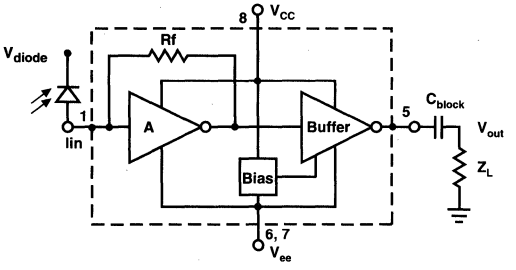


Chip Outline



Chip Thickness is 140µm / 5.5 mil.
Bond Pads are 50µm / 1.97 mil.

Typical Biasing Configuration[8]



Electrical Specifications[2,3], T_A = 25°C

Symbol	Parameters and Test Conditions[4]: V_{cc} = 5 V, V_{ee} = 0 V, Z_L = 50 Ω		Units	Min.	Typ.	Max.
A_Z	Transimpedance Gain	f = 100 MHz	ohms		2800	
F_{3dB}	Small Signal -3 dB Bandwidth[5, 6]		GHz		1.5	
ΔA_Z	Frequency Response Gain Peak[5, 6]		dB	0.0	1.0	
I_n	Input Current Noise Spectral Density[5]	f = 100 MHz	pA/√Hz		3.5	
V_{op-p}	Output V_o Swing (peak to peak)	f = 50 MHz	V_{p-p}		0.95	
VSWR	Output VSWR	f = 100 MHz			2.2:1	
I_{MAX}	Maximum Input Current Before Input Overload[7]	f = 50 MHz	μA_{p-p}		450	
I_d	Device Quiescent Current		mA		34	
V_{in}	Input Quiescent Voltage		Vdc		1.5	
V_{OUT}	Output Quiescent Voltage		Vdc		2.5	

Notes:
1. See Application Note, "AN-005: Transistor Chip Use" for additional information.
2. The recommended operating voltage range for this device is 4.5 to 5.5 V.
3. Tested in HP 180 mil package.
4. RF performance of chip is determined by packaging and testing 10 devices per wafer.
5. Assumes photodiode capacitance, C_{PD}, <0.3 pF.
6. Referenced from 100 MHz.
7. Output duty cycle distortion ≤ ±10%.
8. See Data Sheet, "ITA-06318, MagIC™ Silicon Bipolar MMIC"

Absolute Maximum Ratings

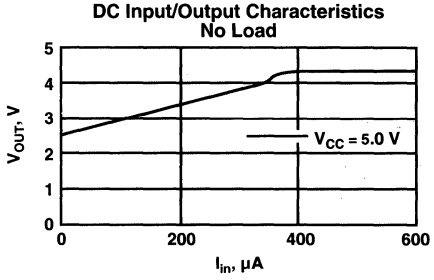
Parameter	Absolute Maximum[1]
Device Voltage	8 V
Power Dissipation[2, 3]	700 mW
V_{in}-V_{ee}	2.0 V
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

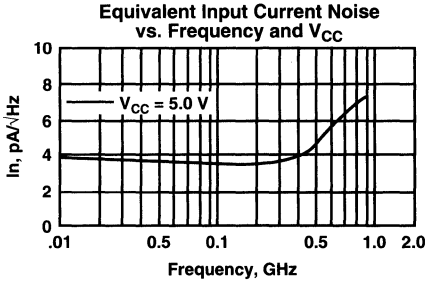
Thermal Resistance: θ_{jc} = 25°C/W

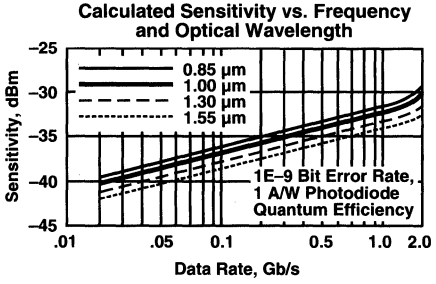
Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{mounting\ surface}$ (T_{ms}) = 25°C.
3. Derate at 40 mW/°C for T_{ms} > 182°C.

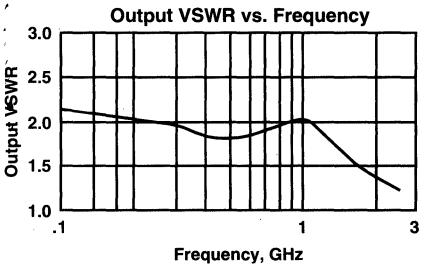
Typical Performance, T_A = 25°C, V_{cc} = 5 V, V_{ee} = 0 V, Z_L = 50 Ω, C_{PD} < 0.3 pF

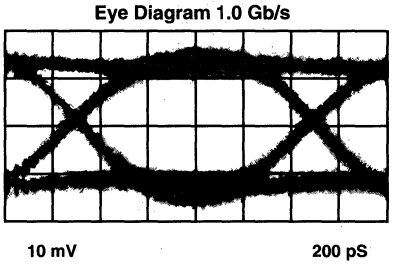
(Unless otherwise noted)











HEWLETT PACKARD

ITA-06318
MagIC™ Silicon Bipolar MMIC
1.5 Gb/s Transimpedance Amplifier

Features

- **High Transimpedance Gain: A_Z = 2800 Ω (69 dB)**
- **High Data Rates: 1.5 Gb/s NRZ**
- **Wide Bandwidth: 1.3 GHz**
- **Low Noise: 3.5 pA/√Hz at 100 MHz**
- **Single Power Supply: +5 V or -5.2 V**
- **Low Power Consumption: 170 mW**
- **Hermetic Glass Metal Surface Mount Package**

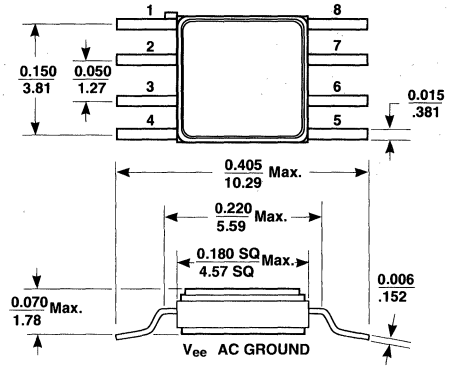
Description

The ITA-06318 is a high-performance transimpedance amplifier housed in a minature glass-metal hermetic surface- mount package. It is designed for use in fiber-optic receivers that require high transimpedance gain, wide bandwidth, reduced power consumption, and low noise.

Typical applications include fiber-optic systems such as high-speed data communications, point to point (Fiber Channel), networks (LAN, MAN), and telecommunications (SONET) with data rates up to 1.8 Gb/s.

The ITA series of transimpedance amplifiers is fabricated using HP's 10 GHz f_T, 25 GHz f_{max} ISOSAT™-1 silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metalization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

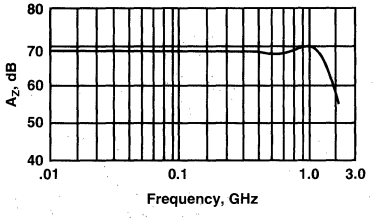
180 mil Package



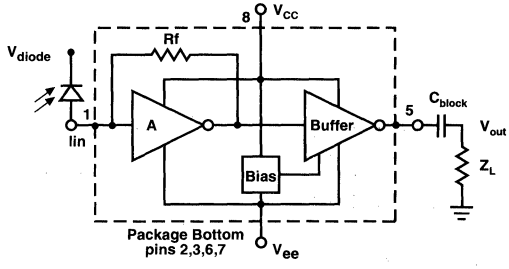
PIN DESCRIPTION	
1 Input	8 V_{cc}
2 V_{ee}, AC Ground	7 V_{ee}
3 V_{ee}, AC Ground	6 V_{ee}
4 NC	5 V_{out}
Bottom of Package is V_{ee} (AC Ground)	

Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
   in .xxx = ±.005
   mm .xx = ±.13

Typical Transimpedance Gain vs. Frequency
T_A = 25°C, V_{CC} = 5 V



Typical Biasing Configuration[8]



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: V_{cc} = 5 V, V_{ee} = 0 V, Z_L = 50 Ω		Units	Min.	Typ.	Max.
A_Z	Transimpedance Gain	f = 100 MHz	ohms	2200	2800	
F_{3dB}	Small Signal -3 dB Bandwidth[2, 4]		GHz	0.9	1.3	
ΔA_Z	Frequency Response Gain Peak[2, 4]		dB	0.0	1.1	2.0
I_n	Input Current Noise Spectral Density[2]	f = 100 MHz	pA/√Hz		3.5	
V_{op-p}	Output Vo Swing (peak to peak)	f = 50 MHz	V_{p-p}		0.95	
VSWR	Output VSWR	f = 100 MHz			1.5:1	
I_{MAX}	Maximum Input Current Before Input Overload[3]	f = 50 MHz	μA_{p-p}		450	
I_d	Device Quiescent Current		mA		34	
V_{in}	Input Quiescent Voltage		Vdc		1.5	
V_{OUT}	Output Quiescent Voltage		Vdc		2.5	

Notes:
1. The recommended operating voltage range for this device is 4.5 to 5.5 V.
2. Assumes photodiode capacitance, C_{PD},<0.3 pF.
3. Output duty cycle distortion ≤ ±10%.
4. Referenced from 100 MHz.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	8 V
Power Dissipation[2, 3]	700 mW
V_{in}-V_{ee}	2.0 V
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

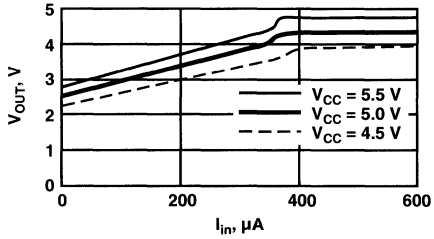
Thermal Resistance: θ_{jc} = 50°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{case} = 25°C.
3. Derate at 20 mW/°C for T_{case} > 165°C.

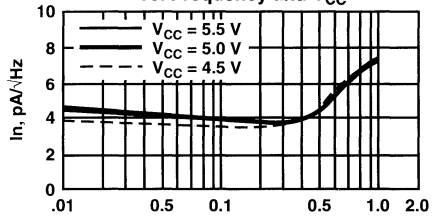
Typical Performance, T_A = 25°C, V_{cc} = 5 V, V_{ee} = 0 V, Z_L = 50 Ω, C_{PD} < 0.3 pF

(Unless otherwise noted)

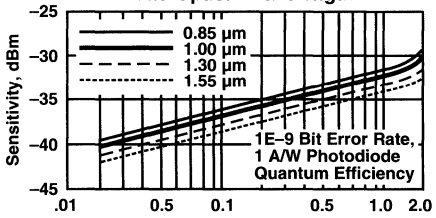
DC Input/Output Characteristics
No Load



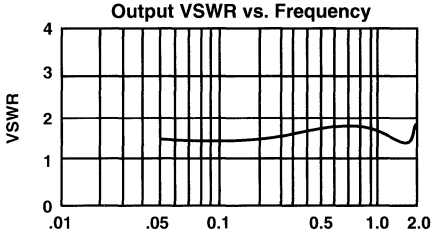
Equivalent Input Current Noise vs. Frequency and V_{CC}



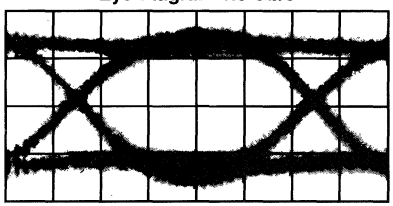
Calculated Sensitivity vs. Frequency and Optical Wavelength



Output VSWR vs. Frequency



Eye Diagram 1.0 Gb/s



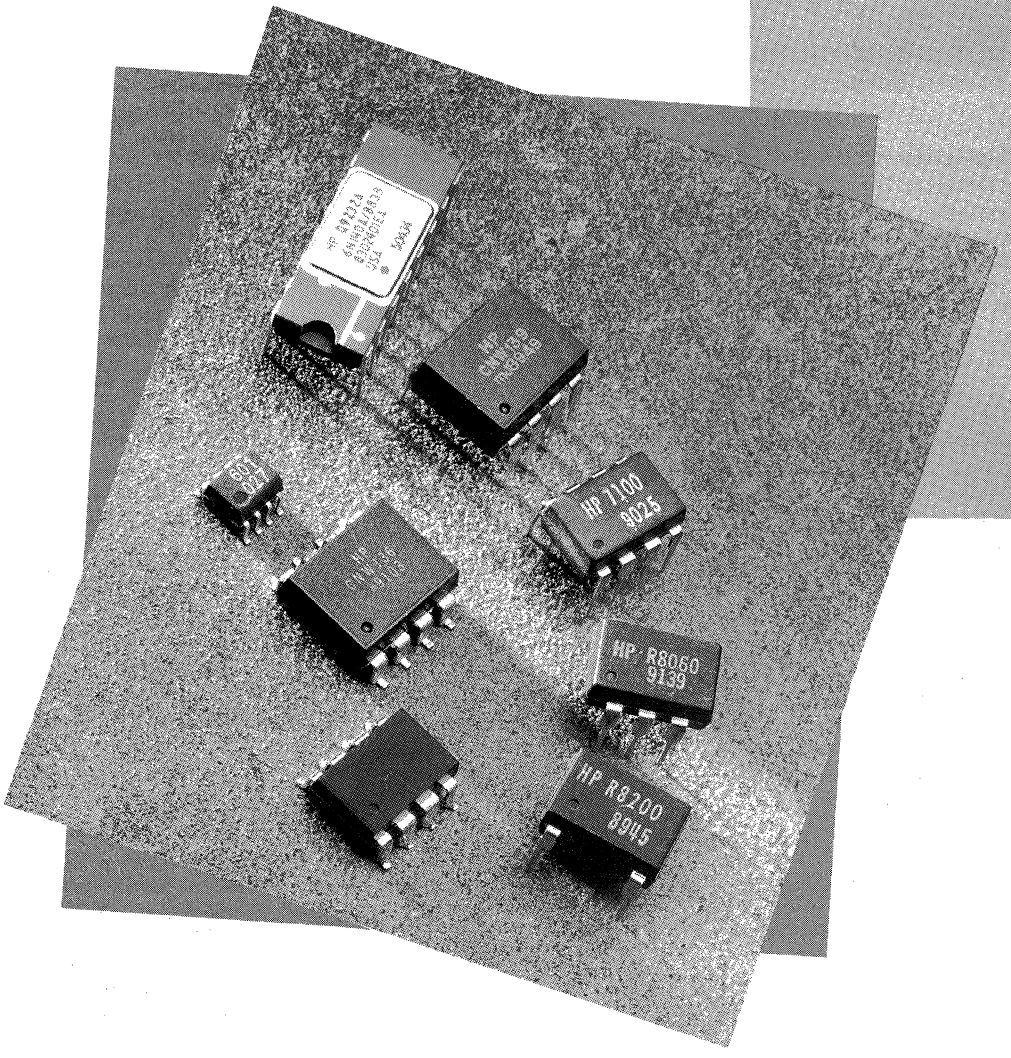
ITA-06318 Scattering Parameters: VCC - Vee = 5V

Freq.	S_{11}		S_{21}		S_{12}		S_{22}	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.05	.10	-24	62.0	-6	.002	-104	.38	168
0.10	.07	-21	63.3	-14	.003	-86	.35	166
0.20	.04	39	64.3	-30	.003	-75	.33	165
0.30	.08	90	66.1	-45	.003	-63	.33	161
0.40	.17	92	67.4	-67	.003	-57	.33	155
0.50	.28	84	67.0	-86	.003	-44	.32	147
0.60	.38	74	64.1	-107	.002	-30	.32	139
0.70	.48	61	58.6	-128	.002	-14	.29	129
0.80	.55	50	51.8	-147	.002	0	.28	122
0.90	.60	39	44.7	-165	.002	16	.26	110
1.00	.64	31	38.3	179	.002	27	.25	103
1.25	.69	16	25.6	146	.003	61	.21	86
1.50	.71	6	17.9	118	.004	93	.21	73
1.75	.71	-2	12.9	94	.006	141	.21	66
2.00	.71	-9	9.8	70	.007	164	.20	63
2.50	.69	-25	6.3	28	.015	178	.14	69

HEWLETT PACKARD

Optocouplers

- Plastic Optocouplers
- Isolation Amplifiers
- Solid State Relays
- Hermetic Optocouplers



HEWLETT PACKARD

Optocouplers

Plastic Optocouplers

Put an end to erroneous data, false control signals, and damaged circuits with HP's line of high-performance plastic optocouplers. There are six basic families of optocouplers to choose from: high-speed logic gate, high-speed transistor output, high-gain, high-speed CMOS logic-to-logic, AC/DC-to-logic interface, and 20 mA current loop. All plastic optocouplers are UL approved and have a withstand voltage of 2500 Vrms/1 minute as a standard feature. A 5000 Vrms/1 minute option is available on selected families. Also available is a surface mount option for our standard package.

A true surface mount SO-8 package is available for all 6N series optocouplers, the HCPL-2601/11, the HCPL-4502/3, and the HCPL-2201/11.

A VDE 0884 approved version of the 6N135/6, 6N138/9, HCPL-4562, and HCPL-4502/3 optocouplers has been designed to meet safety requirements worldwide. These optocouplers feature a "widebody" package to ensure conformance to stringent creepage and clearance requirements.

The HCPL-7100/01 uses an optimized light coupling system to achieve outstanding speed performance with very low power consumption.

Common mode noise rejection has been improved on several of our optocouplers. Enhanced performance up to 15 kV/μs and a Vcm of 1500 volts are available.

In addition to the HSSR-8200, Hewlett-Packard offers two new miniature solid-state relays featuring withstand voltages of 400 V and 60 V. These relays offer the reliability and long life required in instrumentation, telecommunication, and industrial control applications. They can replace electromechanical relays now used in signal and low power switching applications.

Furthermore, with Hewlett-Packard's solid-state relays you get lower power dissipation. For example, the HSSR-8200 features an output with very low leakage current, offset voltage, and capacitance which permits the design of multiplexers that require greater measurement accuracy.

Hewlett-Packard also offers optocoupler solutions to drive power transistors used in motor control inverter applications. The *HCPL-3000* drives power bipolar transistors and the *HCPL-3100/01* drives power MOSFET/IGBT transistors.

New this year is the *HCPL-7800* – a high CMR isolation amplifier. This 8 pin DIP product paves the way for a smaller, lighter, easier to produce, high noise rejection, low cost solution to motor current sensing.

A Selection Flowchart has been added immediately following this introduction to facilitate selection of the correct optocoupler or solid state relay for your application.

Product Safety Regulations and Optocouplers

Optocouplers are frequently used to optically connect a signal line to a circuit in electrical equipment. Besides providing signal isolation, optocouplers are often used to provide high voltage insulation. This is done by preventing voltage transients on a signal line from affecting the equipment, and by protecting

the user/operator from high voltage which may be present inside the equipment.

Because optocouplers perform this safety function, they are regulated by many country safety agencies, both at the component level and the equipment level. Table I lists the detailed regulations associated with each country approval.

It would be ideal for the design engineer to first determine the working voltage at the circuit location where the optocoupler is to be used. After determining the working voltage, the designer asks which optocouplers can meet the creepage, clearance, CTI (comparative tracking index), material group, dielectric withstand voltage, pollution degree, etc. to provide insulation for safety compliance. Based on these known parameters, the designer chooses an optocoupler to fit the need based on tables found in equipment specifications.

Our current data sheets should provide sufficient information to determine the suitability of Hewlett-Packard optocouplers for your applications. Our engineers are also available to assist you in determining which optocoupler best fits your need.

Common Definitions

Clearance — The shortest distance in air between two conductive parts (input metal and output metal), measured through air.

Creepage — The shortest distance measured along the surface of an insulating between two conductive parts (from input metal output metal).

Comparative Tracking Index (CTI) — This is a test designed to compare the performance of various insulating materials in the presence of aqueous contaminants. The higher the CTI, the more resistant the material is to electrical arc tracking. CTI is often used with creepage by safety agencies to determine working voltage.

Dielectric Voltage – Withstand — Capability of a device to withstand without breakdown for 60 seconds, a potential equal to the dielectric insulation voltage applied between the input and output leads of an optocoupler.

Material Group — Material Group is based on CTI and is used in conjunction with Pollution Degree, Creepage Distance and Working Voltage tables in some equipment specifications (e.g. IEC 950, IEC 664):

Material Group I	$600 \leq CTI$
Material Group II	$400 \leq CTI$
Material Group IIIa	$175 \leq CTI < 600$
Material Group IIIb	$100 \leq CTI < 175$

Pollution Degree — Pollution Degree comes from the end-use application and corresponds to the conductivity of dust, dirt, water, etc. to which an optocoupler may be exposed. A higher pollution degree indicates a "dirtier" environment.

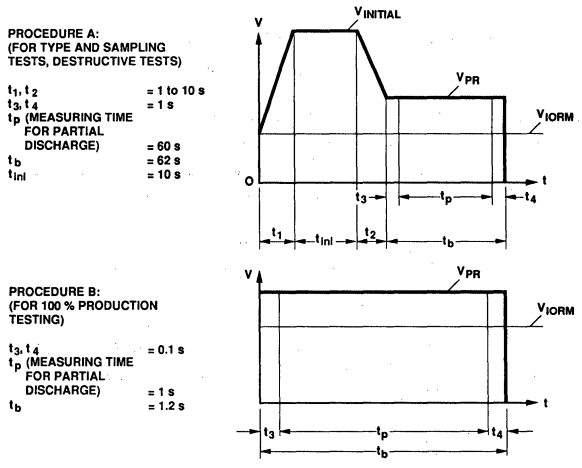
Working Voltage — In general, Working Voltage is the maximum continuous voltage which may be applied to the insulation of an optocoupler under normal operating conditions. Working Voltage is not the same as the one minute Dielectric Withstand-Voltage safety test. Working Voltage is determined by numerous factors such as creepage, clearance, mains voltage, application, pollution degree, CTI, etc.

Optocouplers for Safe Electrical Separation per VDE 0884

Optocouplers providing safe electrical separation per VDE 0884 do so only within the safety-limiting values to which they are qualified. Protective cut-out switches must be used to ensure that the safety limits are not exceeded.

Partial discharge measurements per VDE 0884 are a technique to evaluate the insulation integrity of optocouplers. VDE's philosophy is that partial discharge testing replaces the common dielectric voltage withstand test, because any dielectric voltage test may predamage the insulation of an optocoupler. The profiles below describe the partial discharge test for type and sampling (Procedure A) and for 100% production (Procedure B) testing:

TIME – TEST VOLTAGE DIAGRAM IN ACC. WITH VDE 0884



Determining $V_{INITIAL}$

$V_{INITIAL}$ is the maximum transient overvoltage occurring in the mains voltage of equipment associated with a specific service (or application) class. $V_{INITIAL}$ also equals V_{TR}. Application classes are defined on the following page.

Table I shows the Preferred Insulation Test Voltages for Service Classes. The Mains Voltage and Service (also referred to as Application) Class desired determine the required $V_{INITIAL}$ voltages for Procedures A and B. For example, if the mains voltage is 300 V and the Application Class is III, $V_{INITIAL}$ is 4,000 V peak (2828 Vrms). V_{PR} is derived from 1.2 X V_{IORM} for Procedure A and 1.6 X V_{IORM} for Procedure B.

Definitions of Terms Used in VDE 0884 Partial Discharge Testing

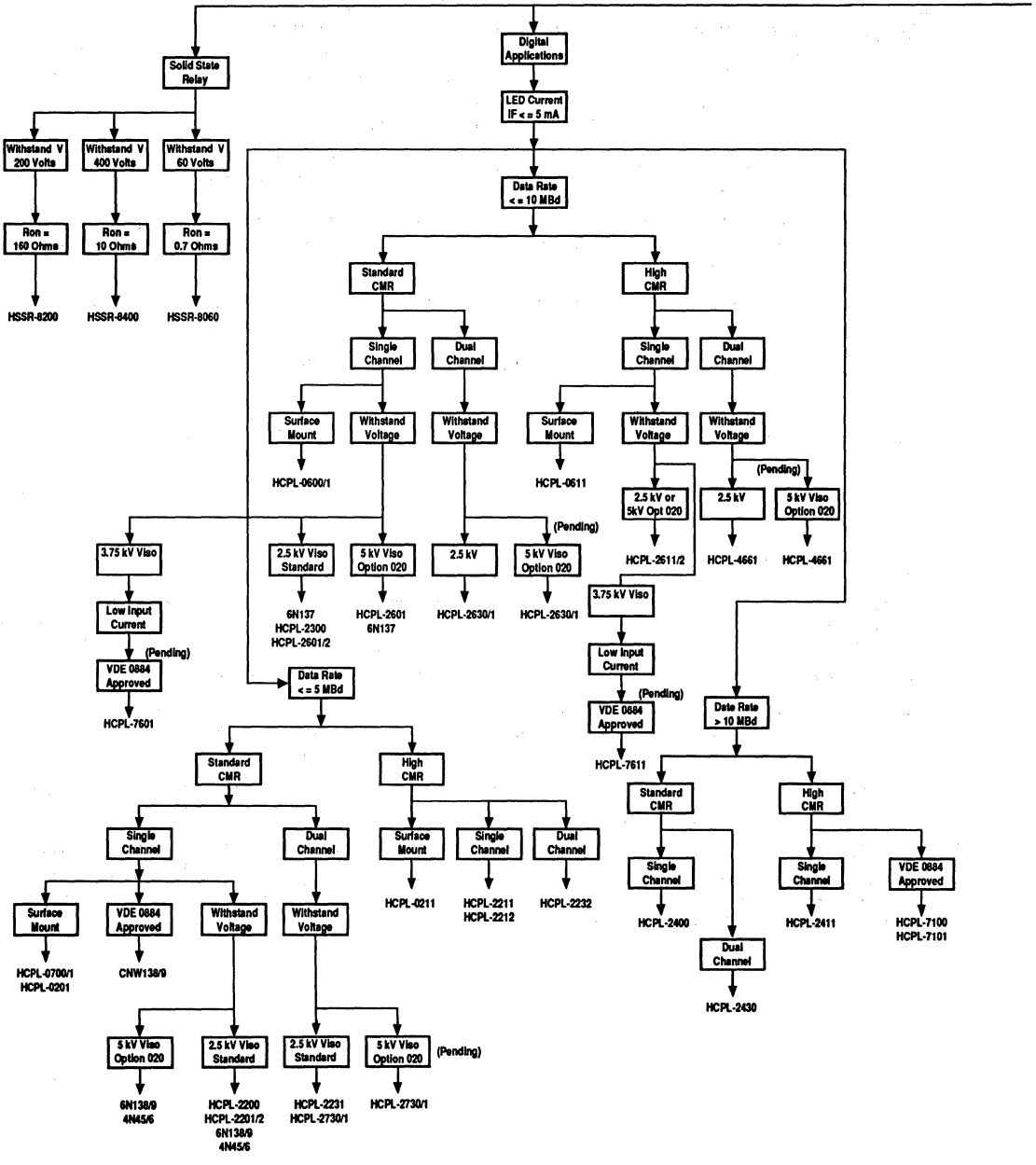
Term	Definition
$V_{INITIAL}$	Maximum test voltage for the partial discharge test. It is also the maximum transient overvoltage occurring in a rated mains voltage and service class. See Table II for preferred values for insulation test voltages. At this initial voltage, partial discharge (but no breakdown) may occur. $V_{INITIAL}$ also equals V_{TR} (transient overvoltage) which is listed in the applicable VDE safety data sections of this catalog.
V_{PR}	Test voltage applied to the device to verify its isolation capacity. V_{PR} = 1.2 X V_{IORM} for Procedure A and 1.6 X V_{IORM} for Procedure B. (Per VDE 0884/08.87)
V_{IORM}	Insulation voltage – this the maximum continuous permitted voltage which may be applied to the optocoupler. This value is specified by VDE in the safety data sections of this catalog.
t_P	Test time for partial discharge and equals 60 seconds for Procedure A, 1 second for Procedure B.
$t_{(ini)}$	Time beginning at $V_{INITIAL}$ test voltage and equals 10 seconds.
t_1, t_2, t_3, t_4	Test voltage initialization times.
Pass/Fail Criteria	No leakage failures and no unit to have more than 5 pC Partial Discharge during the partial discharge test time t_P.

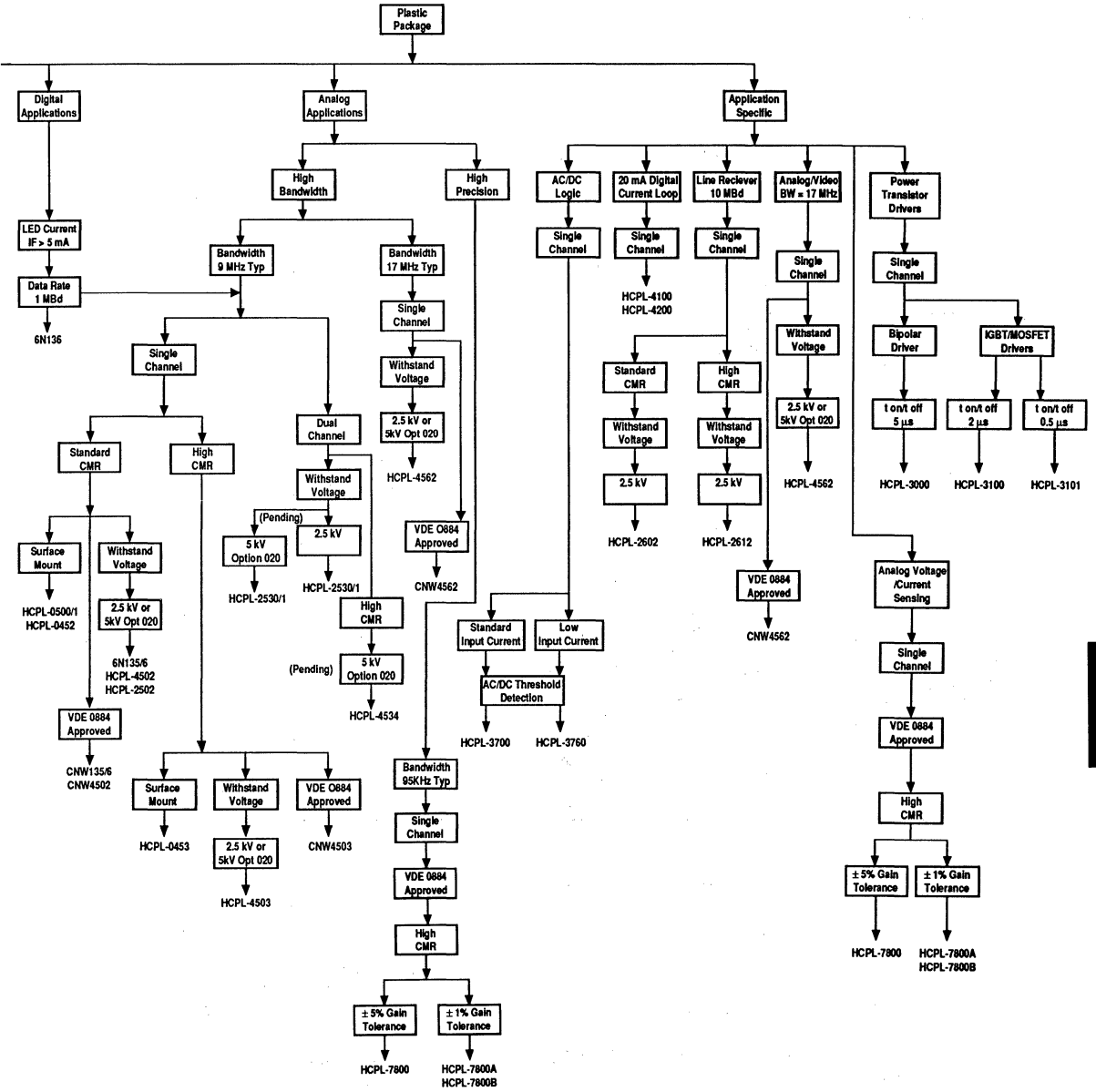
Table I – (from VDE 0884)

Rated Mains Voltages up to and including Vrms or Vdc	Preferred Insulation Test voltages for Service Class ($V_{INITIAL}$)							
	I		II		III		IV	
	PEAK (VAC)	RMS	PEAK (VAC)	RMS	PEAK (VAC)	RMS	PEAK (VAC)	RMS
50	330	233	500	353	800	565	1500	1060
100	500	353	800	565	1500	1060	2500	1767
150	800	656	1500	1060	2500	1767	4000	2828
300	1500	1060	2500	1767	4000	2828	6000	4242
600	2500	1767	4000	2828	6000	4242	8000	5656
1000	4000	2828	6000	4242	8000	5656	12000	8484

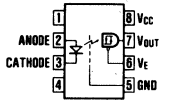
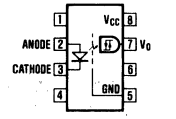
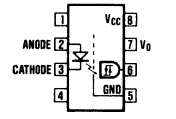
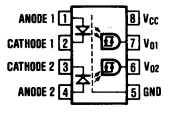
Either the peak AC or the RMS ac test voltage can be used in this test.

Optocoupler and Solid State Relay Selection Flowchart

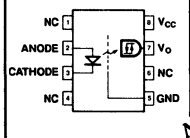



Plastic Package
Digital Applications
Analog Applications
Application Specific
LED Current IF > 5 mA
Data Rate 1 MBd
6N136
High Bandwidth
High Precision
Bandwidth 9 MHz Typ
Bandwidth 17 MHz Typ
Single Channel
Withstand Voltage
2.5 kV or 5kV Opt 020
HCPL-4562
Single Channel
Standard CMR
High CMR
Surface Mount
Withstand Voltage
2.5 kV or 5kV Opt 020
HCPL-0500/1
HCPL-0452
6N135/6
HCPL-4502
HCPL-2502
VDE 0884 Approved
CNW135/6
CNW4502
Dual Channel
Withstand Voltage
(Pending)
5 kV Option 020
HCPL-2530/1
2.5 kV
HCPL-2530/1
High CMR
(Pending)
5 kV Option 020
HCPL-4534
VDE 0884 Approved
CNW4562
Surface Mount
Withstand Voltage
2.5 kV or 5kV Opt 020
HCPL-0453
HCPL-4503
VDE 0884 Approved
CNW4503
Bandwidth 95KHz Typ
Single Channel
VDE 0884 Approved
High CMR
± 5% Gain Tolerance
± 1% Gain Tolerance
HCPL-7800
HCPL-7800A
HCPL-7800B
AC/DC Logic
Single Channel
Standard Input Current
Low Input Current
AC/DC Threshold Detection
HCPL-3700
HCPL-3760
20 mA Digital Current Loop
Single Channel
HCPL-4100
HCPL-4200
Line Reciever 10 MBd
Single Channel
Standard CMR
High CMR
Withstand Voltage
Withstand Voltage
2.5 kV
2.5 kV
HCPL-2602
HCPL-2612
Analog/Video BW = 17 MHz
Single Channel
Withstand Voltage
2.5 kV or 5kV Opt 020
HCPL-4562
VDE 0884 Approved
CNW4562
Power Transistor Drivers
Single Channel
Bipolar Driver
IGBT/MOSFET Drivers
t on/t off 5 µs
t on/t off 2 µs
t on/t off 0.5 µs
HCPL-3000
HCPL-3100
HCPL-3101
Analog Voltage /Current Sensing
Single Channel
VDE 0884 Approved
High CMR
± 5% Gain Tolerance
± 1% Gain Tolerance
HCPL-7800
HCPL-7800A
HCPL-7800B

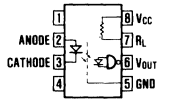
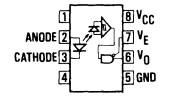
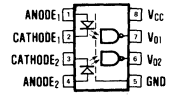
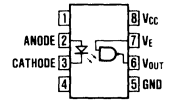
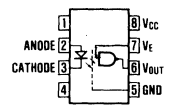
High-Speed Logic Gate Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Guaranteed CMR	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	HCPL-2200	3 State Output Low Input Current Optically Coupled Logic Gate V_{CC} = 20 V Max.	High Speed Logic Ground Isolation, LSTTL, TTL, CMOS Logic Interface	5 MBd	1000 V/µs @ V_{CM} = 50 V	1.6 mA	2500 Vac/ 1 min. UL1577 CSA	6-20
	HCPL-2219				2500 V/µs @ V_{CM} = 400 V			
	HCPL-2201	Low Input Current Optically Coupled Logic Gate V_{CC} = 20 V Max.			1000 V/µs @ V_{CM} = 50 V			6-25
	HCPL-2211				10,000 V/µs @ V_{CM} = 1000 V			
	HCPL-2202		Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments		1000 V/µs @ V_{CM} = 50 V			
	HCPL-2212				10,000 V/µs @ V_{CM} = 1000 V			
	HCPL-2231	Dual Channel Low Input Current Optically Coupled Logic Gate V_{CC} = 20 V Max.	High Speed Logic Ground Isolation, LSTTL, TTL, CMOS Logic Interface	5 MBd	1000 V/µs @ V_{CM} = 50 V	1.8 mA	2500 Vac/ 1 min. UL1577 CSA	6-31
	HCPL-2232		Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments		10 KV/µs @ V_{CM} = 1000 V			

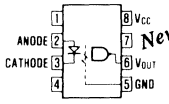
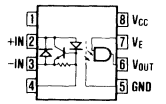
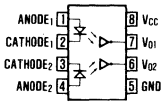
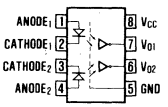
Small Outline High-Speed Logic Gate Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Guaranteed CMR	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
New  New	HCPL-0201	Very High CMR Wide V_{CC} Logic Gate V_{CC} = 20 V Max.	High Speed Logic Ground Isolation, Motor Controls, Switch-mode Power Supplies	5 MBd	1000 V/µs @ V_{CM} = 50 V	1.6 mA	2500 Vac/ 1 min. UL1577	6-36
	HCPL-0211				10,000 V/µs @ V_{CM} = 1000 V			

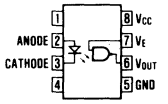
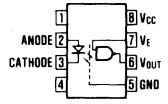
High-Speed Logic Gate Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Guaranteed CMR	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	HCPL-2300	Very Low Input Current, High Speed Optocoupler	High Speed, Long Distance Line Receiver, Computer Peripheral Interfaces, CMOS Logic Interface	8 MBd	100 V/µs @ V_{CM} = 50 V	0.5 mA	2500 Vac/ 1 min. UL1577 CSA	6-42
	HCPL-2400	20 MBaud, High Common Mode Rejection, Optically Coupled Logic Gate 3 State Output	Very High Speed Logic Isolation, I/O and Parallel-to-Serial Conversion	40 MBd	1000 V/µs @ V_{CM} = 50 V	4.0 mA	2500 Vac/ 1 min. UL1577 CSA	6-49
	HCPL-2411		Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments		1000 V/µs @ V_{CM} = 300 V			
	HCPL-2430	Dual Channel, 20 MBd High Common Mode Rejection	Very High Speed Logic Isolation, I/O and Parallel-to-Serial Conversion	40 MBd	1000 V/µs @ V_{CM} = 50 V	4.0 mA	2500 Vac/ 1 min. UL1577 CSA	6-59
	6N137	Optically Coupled Logic Gate	Line Receiver, High Speed Ground Isolation	10 MBd	10 K V/µs V_{CM} = 10 V (Typical)	5.0 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) UL1577 CSA	6-66
	HCPL-2601	High Common Mode Rejection, Optically Coupled Logic Gate	High Speed Logic Ground Isolation	10 MBd	5000 V/µs @ V_{CM} = 50 V	5.0 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) UL1577 CSA	
	HCPL-2611		Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments		10 K V/µs @ V_{CM} = 1000 V			

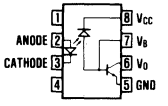
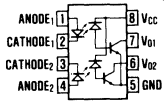
High-Speed Logic Gate Optocouplers (contd.)

Device		Description	Application	Typical Data Rate [NRZ]	Guaranteed CMR	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	New HCPL-7601	CMOS/TTL Compatible, Low Input Current, High CMR Logic Gate	High Speed Logic Ground Isolation	10 MBd	5000 V/µs @ V_{CM} = 50 V	2.0 mA	2500 Vac/ 1 min. 3750 Vac/ 1 min. UL1577 CSA VDE (Pending)	6-75
	New HCPL-7611		Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments Programmable Logic Controllers		10 K V/µs @ V_{CM} = 1000 V			
	HCPL-2602	Optically Coupled Line Receiver	Replace Conventional Line Receivers	10 MBd	1000 V/µs @ V_{CM} = 50 V	5.0 mA	2500 Vac/ 1 min. UL1577 CSA	6-86
	HCPL-2612		Electrically Noisy Environments		3500 V/µs @ V_{CM} = 300 V			
	HCPL-2630	Dual Channel Optically Coupled Gate	Line Receiver, High Speed Logic Ground Isolation	10 MBd	10 K V/µs V_{CM} = 10 V (Typical)	5.0 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) (Pending) UL1577 CSA	6-96
	HCPL-2631	Dual Channel, High Common Mode Rejection, Optically Coupled Logic Gate	High Speed Logic Ground Isolation	10 MBd	5000 V/µs @ V_{CM} = 50 V	5.0 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) (Pending) UL1577 CSA	
	HCPL-4661		Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments		10 K V/µs @ V_{CM} = 1000 V			

Small Outline High-Speed Logic Gate Optocouplers

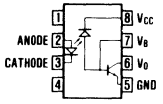
Device		Description	Application	Typical Data Rate [NRZ]	Guaranteed CMR	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	HCPL-0600	Small Outline Optically Coupled Logic Gate	Line Receiver, High Speed Ground Isolation	10 MBd	10 K V/μs @ V_{CM} = 10 V (Typical)	5.0 mA	2500 Vac/ 1 min. UL1577	6-104
	HCPL-0601	Small Outline High CMR, Optically Coupled Logic Gate	High Speed Logic Ground Isolation		5000 V/μs @ V_{CM} = 50 V			
	HCPL-0611		Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments		10 K V/μs @ V_{CM} = 1000 V			

High-Speed Transistor Output Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	6N135	Transistor Output	Line Receiver, Analog Circuits, TTL/CMOS, TTL/LSTTL Ground Isolation	1 MBd	7% Min.	16 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) UL1577 CSA	6-113
	6N136				19% Min.			
	HCPL-4502	Pin 7 Not Connected						
	HCPL-4503	Pin 7 Not Connected, Very High CMR	Electrically Noisy Environments Motor Controls Inverter Circuits					
	New HCPL-4504*				33% Typ.			
	HCPL-2502				15-22%			
	HCPL-2530	Dual Channel Transistor Output	Line Receiver, Analog Circuits, TTL/CMOS, TTL/LSTTL Ground Isolation	1 MBd	7% Min.	16 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) (Pending) UL1577 CSA	6-120
	HCPL-2531				19% Min.			
	HCPL-4534	Very High CMR						

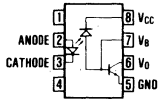
*Contact your HP Field Sales Engineer for availability.

Small Outline High-Speed Transistor Output Optocouplers

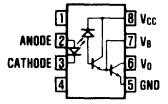
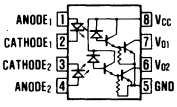
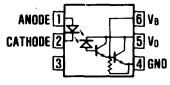
Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	HCPL-0500	Small Outline Transistor Output	Line Receiver, Analog Circuits, TTL/CMOS, TTL/LSTTL Ground Isolation	1 MBd	7% Min.	16 mA	2500 Vac/ 1 min. UL1577	6-126
	HCPL-0501				19% Min.			
	HCPL-0452	Pin 7 Not Connected						
	HCPL-0453	Small Outline Ultra High CMR Transistor Output (Pin 7 Not Connected)	Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments					

Bold Type – New Product

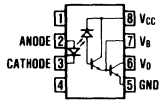
Widebody High-Speed Transistor Output Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Voltage/ Regulatory Approval	Page No.
	CNW135	Transistor Output Widebody (4e pitch) Package	High Voltage Insulation	1 MBd	7% Min.	16 mA	5000 Vac/ 1 min. UL1577 VDE 0884, BS415, 6301, 7002, SETI NEMKO DEMKO SEMKO	6-133
	CNW136		Line Receiver Feedback Element in Switch-mode Power Supplies		19% Min.			
	CNW4502	Pin 7 Not Connected	Motor Control Inverter Circuits					
	New CNW4503	Pin 7 Not Connected, Very High CMR						

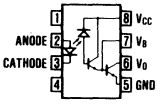
High Gain Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	6N138	Low Saturation Voltage, High Gain Output, V_{CC} = 7 V Max.	Line Receiver, Low Current Ground Isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL	100 KBd	300% Min.	1.6 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) UL1577 CSA	6-140
	6N139	Low Saturation Voltage, High Gain Output, V_{CC} = 18 V Max.	Line Receiver, Ultra Low Current Ground Isolation, CMOS/ LSTTL, CMOS/TTL, CMOS/CMOS		400% Min.	0.5 mA		
	HCPL-2730	Dual Channel, High Gain, V_{CC} = 7 V Max.	Line Receiver, Polarity Sensing, Low Current Ground Isolation	100 KBd	300% Min.	1.6 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) (Pending) UL1577 CSA	6-145
	HCPL-2731	Dual Channel, High Gain, V_{CC} = 18 V Max.			400% Min.	0.5 mA		
	4N45	Darlington Output V_{CC} = 7 V Max.	AC Isolation, Relay-Logic Isolation	3 KBd	250% Min.	1.0 mA	2500 Vac/ 1 min. UL1577	6-150
	4N46	Darlington Output, V_{CC} = 20 V Max.			350% Min.	0.5 mA		

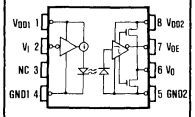
Small Outline High Gain Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	HCPL-0700	Small Outline Low Saturation Voltage, High Gain Output, V_{CC} = 7 V Max.	Line Receiver, Low Current Ground Isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL	100 KBd	300% Min.	1.6 mA	2500 Vac/ 1 min. UL1577	6-155
	HCPL-0701	Small Outline Low Saturation Voltage, High Gain Output, V_{CC} = 18 V Max.	Line Receiver, Ultra Low Current Ground Isolation, CMOS/LSTTL, CMOS/TTL, CMOS/CMOS		400% Min.	0.5 mA		

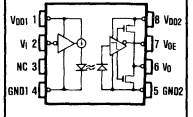
Widebody High Gain Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	CNW138	Low Saturation Voltage, High Gain Output, V_{CC} = 7 V Max. Widebody (4e pitch) Package	Line Receiver, Low Current Ground Isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL	100 KBd	300% Min.	1.6 mA	5000 Vac/ 1 min. UL1577 VDE 0884 BS415, 6301, 7002, SETI NEMKO DEMKO SEMKO	6-161
	CNW139	Low Saturation Voltage, High Gain Output, V_{CC} = 18 V Max. Widebody (4e pitch) Package	Line Receiver, Ultra Low Current Ground Isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL		400% Min.	0.5 mA		

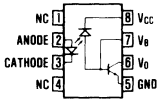
High-Speed CMOS Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Guaranteed CMR	Total Power Supply Current	Withstand Voltage/ Regulatory Approval	Page No.
	HCPL-7100	High-Speed, Low Power 3 State Output CMOS IC Technology	Computer-Peripheral Interface Digital Isolation for A/D, D/A Converters, Motor Control, Power Inverter, +5 V Compatibility CMOS and TTL Logic	15 MBd	1000 V/ms @ 50 V V_{CM}	10 mA (Typical)	3750 Vac/ 1 min. UL 1577 VDE 0884	6-168

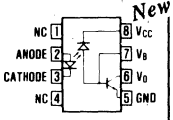
Ultra High-Speed CMOS Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Guaranteed CMR	Total Power Supply Current	Withstand Voltage/ Regulatory Approval	Page No.
	HCPL-7101	High-Speed, Low Power 3 State Output CMOS IC Technology	Computer-Peripheral Interface Digital Isolation for A/D, D/A Converters, Motor Control, Power Inverter, +5 V Compatibility CMOS and TTL Logic	65 MBd	2000 V/ms @ 200 V V_{CM}	10 mA (Typical)	3750 Vac/ 1 min. UL1577 VDE 0884	6-168

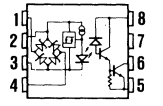
Wideband Analog/Video Optocoupler

Device		Description	Application	Typical Bandwidth	Differential Gain	Linearity	Withstand Test Voltage/ Regulatory Approval	Page No.
	HCPL-4562	Wideband Analog/ Video Optocoupler	Video Isolation, Feedback Element in Switch-mode Power Supplies	17 MHz	±1%	0.25%	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) UL1577 CSA	6-180

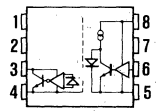
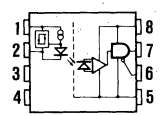
Widebody Wideband Analog/Video Optocoupler

Device		Description	Application	Typical Bandwidth	Differential Gain	Linearity	Withstand Test Voltage/ Regulatory Approval	Page No.
	CNW4562	Wideband Analog/ Video Optocoupler	Video Isolation, Feedback Element in Switch-mode Power Supplies	9.0 MHz	±0.9%	0.15%	5000 Vac/ 1 min. UL1577 VDE 0884 BS415, 6301, 7002 SETI NEMKO DEMKO SEMKO	6-186

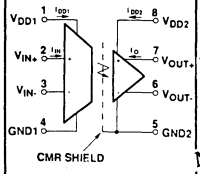
AC/DC to Logic Interface Optocouplers

Device		Description	Application	Operating Frequency	Input Threshold Current	Output Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	HCPL-3700	AC/DC to Logic Threshold Sensing Interface Optocoupler	Limit Switch Sensing, Low Voltage Detector, Relay Contact Monitor	4 KHz	2.5 mA TH+ 1.3 mA TH-	4.2 mA	2500 Vac/ 1 min. UL1577 CSA	6-195
	HCPL-3760	Low Input Current			1.2 mA TH+ 0.6 mA TH-			

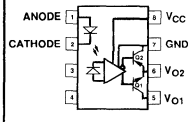
20 mA Current Loop Optocouplers

Device		Description	Application	Typical Data Rates	Input Characteristics	Output Characteristics	Withstand Test Voltage/ Regulatory Approval	Page No.
	HCPL-4100	Optically Coupled 20 mA Current Loop Transmitter	Isolated 20 mA Current Loop in: • Computer Peripherals • Industrial Control Equipment • Data Communication Equipment	20 kBd (at 400 metres)	TTL/CMOS	27 V Max. Compliance Voltage	2500 Vac/ 1 min. UL1577 CSA	6-205
	HCPL-4200	Optically Coupled 20 mA Current Loop Receiver			6.5 mA Typ. Threshold Current	3 State Output	2500 Vac/ 1 min. UL1577 CSA	6-213

High CMR Isolation Amplifier

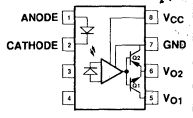
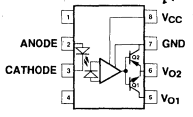
Device		Description	Application	Offset Drift	Gain Tolerance	Guaranteed Isolation Mode Rejection	Withstand Test Voltage/ Regulatory Approval	Page No.
	New HCPL-7800	High CMR Isolation Amplifier	Motor Phase Current Sensing General Purpose Industrial Current Sensing	-2.1 µV/°C	±5% Mean Gain Value = 8.00	10 K V/µs @ V_{CM} = 1000 V	3750 Vac/ 1 min. UL1577 CSA VDE 0884	6-221
	New HCPL-7800A				±1% Mean Gain Value = 7.93			
	New HCPL-7800B				±1% Mean Gain Value = 8.07			

Power Bipolar Transistor Base Drive Optocoupler

Device		Description	Application	Output Current	Guaranteed CMR	Propagation Delay	Withstand Test Voltage/ Regulatory Approval	Page No.
	New HCPL-3000	High Output Current, Wide V_{CC} Range (5.4 - 18 Volts) Isolated Power Bipolar Driver	AC/DC Motor Drive Uninterruptible Power Supply	I_{O2} 2 A Peak 0.6 A Continuous I_{O1} 1 A Peak 0.5 A Continuous	1.5 K V/µs @ V_{CM} = 600 V	2 µs	5000 Vac/ 1 min. UL1577	6-237

OPTO COUPLERS

Power MOSFET/IGBT Gate Drive Optocoupler

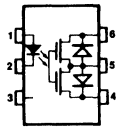
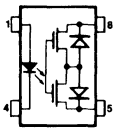
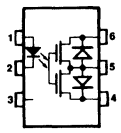
Device	Description	Application	Output Current	Guaranteed CMR	Propagation Delay	Withstand Test Voltage/ Regulatory Approval	Page No.
New HCPL-3100 	High Output Current, Wide V_{CC} Range (15 - 30 Volts) Isolated Power MOSFET/IGBT Driver	AC/DC Motor Drives Uninterruptible Power Supplies	I_{O1} and I_{O2} 0.4 A Peak, 0.1 A Continuous	1.5 K V/µs @ V_{CM} = 600 V	1 µs	5000 Vac/ 1 min. UL1577	6-245
New HCPL-3101 					0.3 µs		

Optocoupler Options

Option	Description	Eligible Optocouplers & Solid State Relays	Page No.
001	Commercial Burn-in	All 7.6 mm (300 mil) wide plastic products. Contact factory for availability.	
002	100% Screening Program	All 7.6 mm (300 mil) wide plastic products. Contact factory for availability.	
020	5000 Vac/1 min. UL Rating	See Note 1 for list of part numbers.	6-255
300	Gull Wing Surface Mount	Available on most plastic and hermetic products. Contact factory for list of part numbers.	6-257
500	Tape and Reel Packaging	Available on most plastic gull wing and small outline surface mount products. Contact factory for list of part numbers.	6-260

Notes:
1. Option 020 is available for 6N135, 6N136, 6N137, 6N138, 6N139, HCPL-2502, HCPL-2601, HCPL-2611, HCPL-4502, HCPL-4503 and HCPL-4562.
2. DESC part numbers cannot be ordered with Option 200; instead use part number designator "A" for solder dipped leads.

Plastic Solid State Relays

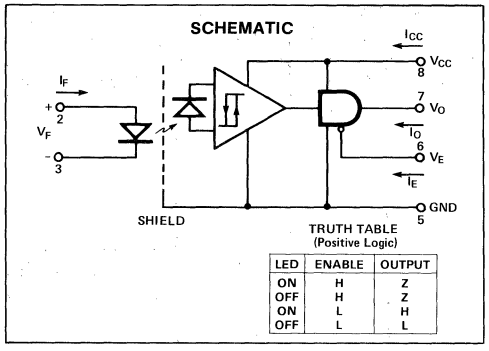
Device	Application	Output Withstand Voltage @ 25°C	Maximum Load Current @ 25°C	Typical Output On-Resistance @ 25°C	Typical Output Off-Leakage @ 25°C	Page No.
New HSSR-8060 	24 V ac/dc, 48 Vdc Load Switching; Programmable Controller Output Module; Small Signal Switching; Reed Relay Replacement; and Industrial Relay Coil Driver	60 V	0.75/1.5* Amp	0.4 Ω	0.1 nA (Vo = 60 V)	6-265
HSSR-8200 	Small Signal Switching; Data Acquisition; Analog Signal Multiplexing; Test & Measurement; Reed Relay Replacements	200 V	40 mA	125 Ω	0.02 nA (Vo = 200 V)	6-275
New HSSR-8400 	Pulse Dialing & Off-Hook Detection Telecom Circuit; Reed Relay Replacement; Small Signal Switching; 110/220 Vac Load Driver; Industrial Relay Coil Driver	400 V	150/300* mA	6 Ω	0.6 nA (Vo = 400 V)	6-283

*For applications that switch only dc signal and power, the HSSR-8060 and HSSR-8400 outputs pins can be connected in a special manner to significantly reduce the output on-resistance, and increase the output current rating. Refer to Connections A and B in the HSSR-8060 and HSSR-8400 technical data sheets.

HEWLETT PACKARD

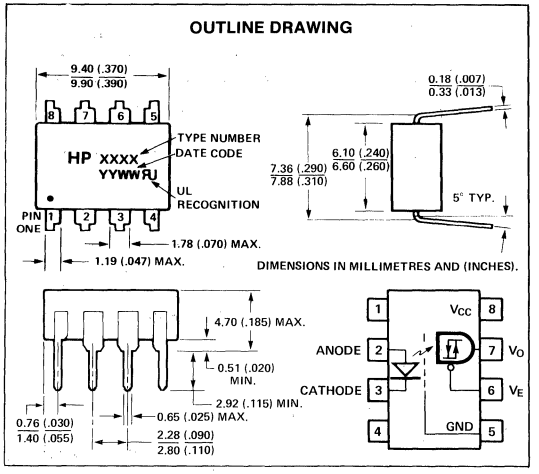
LOW INPUT CURRENT LOGIC GATE OPTOCOUPLER

HCPL-2200
HCPL-2219



TRUTH TABLE
(Positive Logic)

LED	ENABLE	OUTPUT
ON	H	Z
OFF	H	Z
ON	L	H
OFF	L	L



Features

- **VERY HIGH COMMON MODE REJECTION 2.5 KV/μs AT 400 V V_{CM} GUARANTEED (HCPL-2219)**
- **COMPATIBLE WITH LSTTL, TTL, AND CMOS LOGIC**
- **WIDE V_{CC} RANGE (4.5 TO 20 VOLTS)**
- **2.5 MBAUD GUARANTEED OVER TEMPERATURE**
- **LOW INPUT CURRENT (1.6 mA)**
- **THREE STATE OUTPUT (NO PULLUP RESISTOR REQUIRED)**
- **GUARANTEED PERFORMANCE FROM 0° C TO +85° C**
- **INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **CSA APPROVED**
- **MIL-STD-1772 VERSION AVAILABLE (HCPL-5200/1)**

Applications

- **Isolation of High Speed Logic Systems**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **Isolated Buss Driver**
- **High Speed Line Receiver**

Description

The HCPL-2200 is an optically coupled logic gate that combines a GaAsP LED and an integrated high gain photon detector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data busses. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1,000 volts/μsec. Higher CMR specifications are available upon request.

The Electrical and Switching Characteristics of the HCPL-2200 are guaranteed over the temperature range of 0° C to 85° C. The HCPL-2200 is guaranteed to operate over a V_{CC} range of 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic. Low I_F and low I_{CC} result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a typical propagation delay of 160 nsec.

The HCPL-2200 is useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Enable Voltage High	V_{EH}	2.0	20	Volts
Enable Voltage Low	V_{EL}	0	0.8	Volts
Forward Input Current	$I_{F(ON)}$	1.6*	5	mA
Forward Input Current	$I_{F(OFF)}$	—	0.1	mA
Operating Temperature	T_A	0	85[1]	°C
Fan Out	N		4	TTL Loads

*The initial switching threshold is 1.6 mA or less. It is recommended that 2.2 mA be used to permit at least a 20% CTR degradation guardband.

Recommended Circuit Design

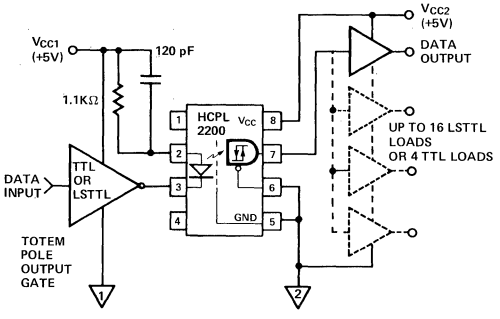


Figure 1. Recommended LSTTL to LSTTL Circuit

Absolute Maximum Ratings

(No Derating Required up to 70° C)

Storage Temperature ..... -55° C to +125° C
Operating Temperature ..... -40° C to +85° C[1]
Lead Solder Temperature ..... 260° C for 10 s
(1.6 mm below seating plane)
Average Forward Input Current — I_F ..... 10 mA
Peak Transient Input Current — I_F 1A
($\leq$1 μs Pulse Width, 300 pps)
Reverse Input Voltage 5V
Supply Voltage — V_{CC} ..... 0.0V min., 20V max.
Three State Enable Voltage
— V_E ..... -0.5V min., 20V max.
Output Voltage — V_O ..... -0.5V min., 20V max.
Total Package Power
Dissipation — P ..... 210 mW[1]
Average Output Current — I_O ..... 25 mA

Electrical Specifications

For 0°C $\leq T_A$[1] $\leq$ 85°C, 4.5 V $\leq V_{CC} \leq$ 20 V, 1.6 mA $\leq I_{F(ON)} \leq$ 5 mA, 2.0 V $\leq V_{EH} \leq$ 20 V, 0.0 V $\leq V_{EL} \leq$ 0.8 V, 0 mA $\leq I_{F(OFF)} \leq$ 0.1 mA. All Typicals at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 3 mA unless otherwise specified. See note 7.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads)		2	
Logic High Output Voltage	V_{OH}	2.4	*		Volts	I_{OH} = -2.6 mA	*$V_{OH} = V_{CC}$ - 2.1V	3	
Output Leakage Current ($V_{OUT} > V_{CC}$)	I_{OHH}			100	μA	V_O = 5.5V	I_F = 5 mA		
				500	μA	V_O = 20V	V_{CC} = 4.5V		
Logic High Enable Voltage	V_{EH}	2.0			Volts				
Logic Low Enable Voltage	V_{EL}			0.8	Volts				
Logic High Enable Current	I_{EH}			20	μA	V_{EN} = 2.7V			
				100	μA	V_{EN} = 5.5V			
			.004	250	μA	V_{EN} = 20V			
Logic Low Enable Current	I_{EL}			-0.32	mA	V_{EN} = 0.4V			
Logic Low Supply Current	I_{CCL}		4.5	6.0	mA	V_{CC} = 5.5V	I_F = 0 mA, I_O = Open, V_E = Don't Care		
			5.25	7.5	mA	V_{CC} = 20V			
Logic High Supply Current	I_{CCH}		2.7	4.5	mA	V_{CC} = 5.5V	I_F = 5 mA, I_O = Open, V_E = Don't Care		
			3.1	6.0	mA	V_{CC} = 20V			
High Impedance State Output Current	I_{OZL}			-20	μA	V_O = 0.4V	V_{EN} = 2V, I_F = 5 mA		
	I_{OZH}			20	μA	V_O = 2.4V	V_{EN} = 2V, I_F = 0		
				100	μA	V_O = 5.5V			
				500	μA	V_O = 20V			
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	$V_O = V_{CC}$ = 5.5V	I_F = 0 mA		2
		40			mA	$V_O = V_{CC}$ = 20V			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5V	I_F = 5 mA, V_O = GND		2
		-25			mA	V_{CC} = 20V			
Input Current Hysteresis	I_{HYS}		0.12		mA	V_{CC} = 5V		4	
Input Forward Voltage	V_F		1.5	1.7	Volts	T_A = 25°C	I_F = 5 mA	5	
				1.75					
Input Reverse Breakdown Voltage	BV_R	5			Volts	I_R = 10 μA			
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.7		mV/°C	I_F = 5 mA			
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH $\leq$ 50%, t = 1 min., T_A = 25°C		12	3, 8
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 VDC			3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 VDC			3
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0V, Pins 2 and 3			

Switching Specifications

For $0°C \le T_A[1] \le 85°C$, $4.5V \le V_{CC} \le 20V$, $1.6\ mA \le I_{F(ON)} \le 5\ mA$, $0.0\ mA \le I_{F(OFF)} \le 0.1\ mA$. All Typicals at $T_A = 25°C$, $V_{CC} = 5V$, $I_{F(ON)} = 3\ mA$ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		210		ns	Without Peaking Capacitor	6,7	4,5
			160	300		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		170		ns	Without Peaking Capacitor	6,7	4,5
			115	300		With Peaking Capacitor		
Output Enable Time to Logic High	t_{PZH}		25		ns		8,10	
Output Enable Time to Logic Low	t_{PZL}		28		ns		8,9	
Output Disable Time from Logic High	t_{PHZ}		105		ns		8,10	
Output Disable Time from Logic Low	t_{PLZ}		60		ns		8,9	
Output Rise Time (10-90%)	t_r		55		ns		6,11	
Output Fall Time (90-10%)	t_f		15		ns		6,11	

Parameter	Symbol	Device	Min.	Units	Test Conditions		Figure	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	HCPL-2200	1,000	V/μs	|Vcm| = 50 V	I_F = 1.6 mA, V_{CC} = 5 V, T_A = 25°C	12	6
		HCPL-2219	2,500	V/μs	|Vcm| = 400 V			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	HCPL-2200	1,000	V/μs	|Vcm| = 50 V	V_F = 0 V, V_{CC} = 5 V, T_A = 25°C	12	6
		HCPL-2219	2,500	V/μs	|Vcm| = 400 V			

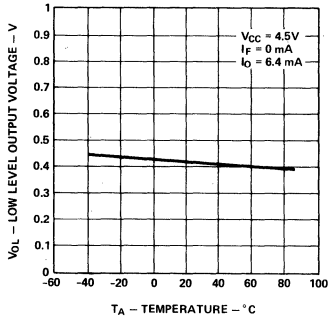


Figure 2. Typical Logic Low Output Voltage vs. Temperature

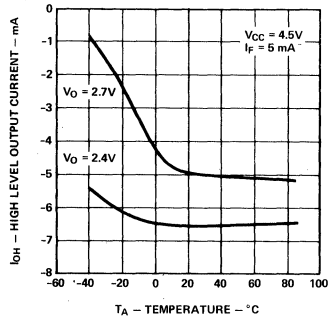


Figure 3. Typical Logic High Output Current vs. Temperature

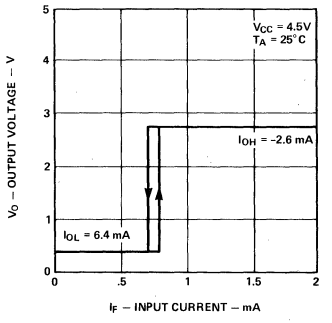


Figure 4. Output Voltage vs. Forward Input Current

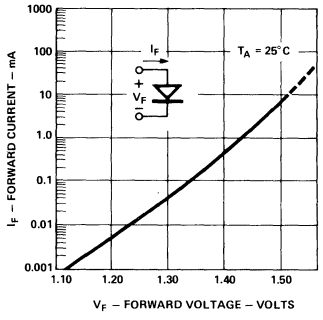


Figure 5. Typical Input Diode Forward Characteristic

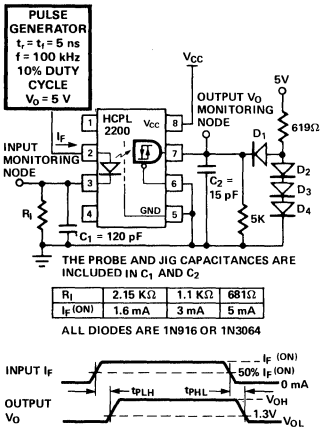


Figure 6. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

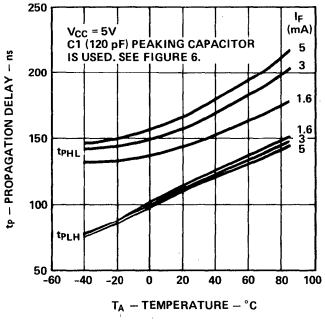


Figure 7. Typical Propagation Delays vs. Temperature

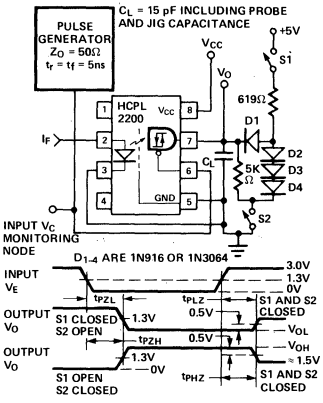


Figure 8. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}

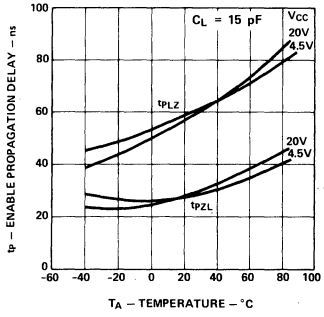


Figure 9. Typical Logic Low Enable Propagation Delay vs. Temperature

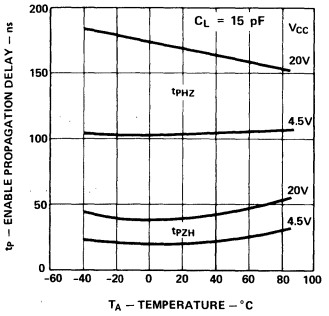


Figure 10. Typical Logic High Enable Propagation Delay vs. Temperature

OPTO COUPLERS

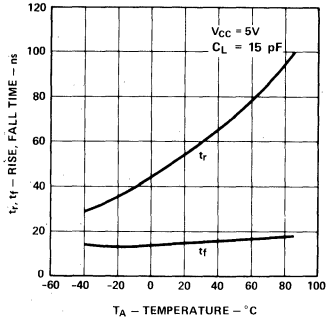


Figure 11. Typical Rise, Fall Time vs. Temperature

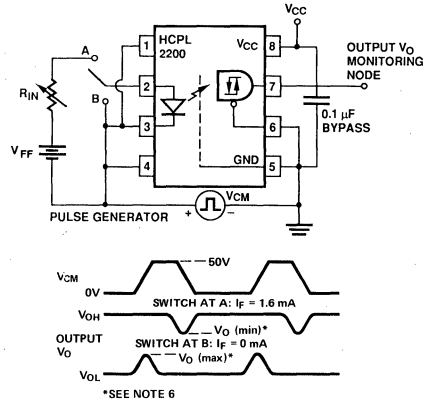


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

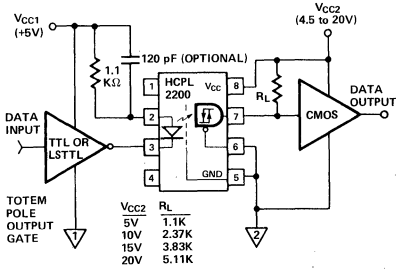


Figure 13. LSTTL to CMOS Interface Circuit

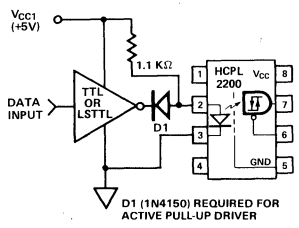


Figure 14. Recommended LED Drive Circuit

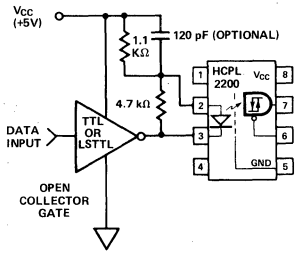


Figure 15. Series LED Drive with Open Collector Gate (4.7 kΩ Resistor Shunts I_{OH} from the LED)

The 120 pF capacitor may be omitted in applications where 500 ns propagation delay is sufficient.

Notes:

1. Derate total package power dissipation, P, linearly above 70° C free air temperature at a rate of 4.5 mW/° C.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.
5. When the peaking capacitor is omitted, propagation delay times may increase by 100 ns.
6. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0V).
7. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, I_{i-o} ≤ 5 μA).

HEWLETT PACKARD

Very High CMR, Wide V_{CC} Logic Gate Optocoupler

HCPL-2201
HCPL-2202
HCPL-2211
HCPL-2212

Features

- **Very High Common Mode Rejection, 10 kV/μs at 1000 V Guaranteed (HCPL- 2211/12)**
- **Wide V_{CC} Range (4.5 to 20 Volts)**
- **300 ns Propagation Delay Guaranteed over the Full Temperature Range**
- **5 MBd Typical Signal Rate**
- **Low Input Current (1.6 mA)**
- **Totem Pole Output (No Pullup Resistor Required)**
- **Guaranteed Performance From -40°C to +85°C**
- **Recognized under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 Vac, 1 Minute**
- **CSA Approved**

Applications

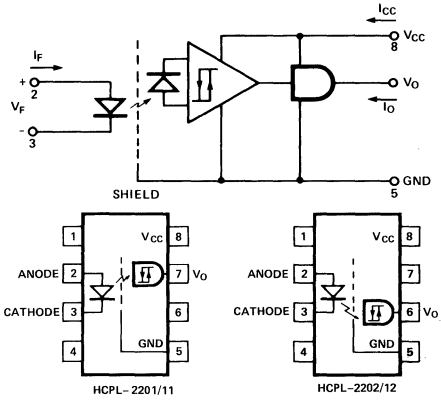
- **Isolation of High Speed Logic Systems**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **High Speed Line Receiver**

Description

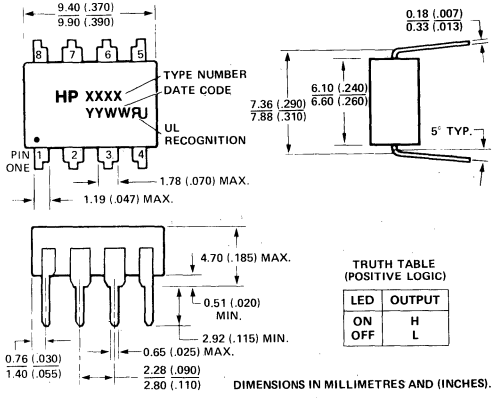
The HCPL-2201/02/11/12 are single-channel, optically-coupled logic gates. The detectors have totem pole output stages and optical receiver input stages with built-in Schmitt triggers to provide logic-compatible waveforms, eliminating the need for additional waveshaping.

OPTO COUPLERS

Schematic



Outline Drawing



TRUTH TABLE
(POSITIVE LOGIC)

LED	OUTPUT
ON	H
OFF	L

DIMENSIONS IN MILLIMETRES AND (INCHES).

A superior internal shield on the HCPL-2211/12 guarantees common mode transient immunity of 10 kV/μs at a common mode voltage of 1000 volts.

The electrical and switching characteristics of the HCPL-2201/02/11/12 are guaranteed from -40°C to +85°C and a V_{CC} from 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed couplers. Logic signals are transmitted with a typical propagation delay of 150 ns.

Recommended Circuit Design

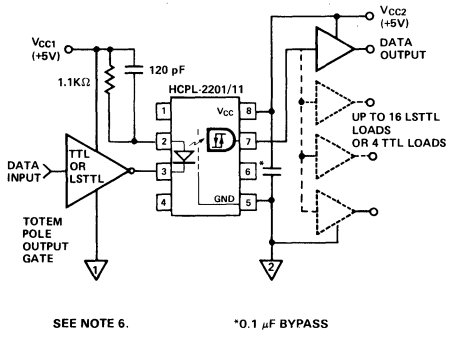


Figure 1. Recommended LSTTL to LSTTL Circuit.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Forward Input Current	$I_{F(ON)}$	1.6*	5	mA
Forward Input Voltage	$V_{F(OFF)}$	–	0.8	Volts
Operating Temperature	T_A	-40	85	°C
Fan Out	N		4	TTL Loads

*The initial switching threshold is 1.6 mA or less. It is recommended that 2.2 mA be used to permit at least a 20% CTR degradation guardband.

Absolute Maximum Ratings

(No Derating Required up to 70°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Forward Input Current – I_F ..... 10 mA
Peak Transient Input Current – I_F ..... 1 A
(≤1 μs Pulse Width, 300 pps)
Reverse Input Voltage ..... 5 V
Supply Voltage – V_{CC} ..... 0.0 V min., 20 V max.
Output Voltage – V_O ..... -0.5 V min., 20 V max.
Total Package Power Dissipation – P ..... 210 mW[1]
Average Output Current – I_O ..... 25 mA

Electrical Specifications

-40°C ≤ T_A ≤ 85°C, 4.5 V ≤ V_{CC} ≤ 20 V, 1.6 mA ≤ $I_{F(ON)}$ ≤ 5 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, unless otherwise specified. All Typicals at T_A = 25°C. See Note 7.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads)		2, 4	
Logic High Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -2.6 mA	V_{CC} = 4.5 V	3, 4, 8	
		2.7				I_{OH} = -0.4 mA			
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	µA	V_O = 5.5 V	I_F = 5 mA, V_{CC} = 4.5 V		
				500	µA	V_O = 20 V			
Logic Low Supply Current	I_{CCL}		3.7	6.0	mA	V_{CC} = 5.5 V	V_F = 0 V, I_O = Open		
			4.3	7.0	mA	V_{CC} = 20 V			
Logic High Supply Current	I_{CCH}		2.4	4.0	mA	V_{CC} = 5.5 V	I_F = 5 mA, I_O = Open		
			2.7	5.0	mA	V_{CC} = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	15			mA	V_O = V_{CC} = 5.5 V	V_F = 0 V		2
		20			mA	V_O = V_{CC} = 20 V			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5 V	I_F = 5 mA, V_O = GND		2
		-20			mA	V_{CC} = 20 V			
Input Forward Voltage	V_F		1.5	1.7	Volts	T_A = 25°C	I_F = 5 mA	5	
				1.85					
Input Reverse Breakdown Voltage	BV_R	5			Volts	I_R = 10 µA			
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.7		mV/°C	I_F = 5 mA			
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%; t = 1 min, T_A = 25°C			3, 8
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 VDC			3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 VDC			3
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V, Pins 2 and 3			

Switching Specifications $-40°C \le T_A \le 85°C$, $4.5\ V \le V_{CC} \le 20\ V$, $1.6\ mA \le I_{F(ON)} \le 5\ mA$, $0\ V \le V_{F(OFF)} \le 0.8\ V$. All typicals at $T_A = 25°C$, $V_{CC} = 5\ V$, $I_{F(ON)} = 3\ mA$ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		150		ns	Without Peaking Capacitor	6, 7	4
			150	300		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		110		ns	Without Peaking Capacitor	6, 7	4
			90	300		With Peaking Capacitor		
Output Rise Time (10-90%)	t_r		30		ns		6, 9	
Output Fall Time (90-10%)	t_f		7		ns		6, 9	

Parameter	Symbol	Device	Min.	Units	Test Conditions		Fig.	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	HCPL-2201 HCPL-2202	1,000	V/μs	$\|Vcm\| = 50\ V$	$I_F = 1.6\ mA$, $V_{CC} = 5\ V$, $T_A = 25°C$	10	5
		HCPL-2211 HCPL-2212	10,000	V/μs	$\|Vcm\| = 1\ kV$			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	HCPL-2201 HCPL-2202	1,000	V/μs	$\|Vcm\| = 50\ V$	$V_F = 0\ V$, $V_{CC} = 5\ V$, $T_A = 25°C$	10	5
		HCPL-2211 HCPL-2212	10,000	V/μs	$\|Vcm\| = 1\ kV$			

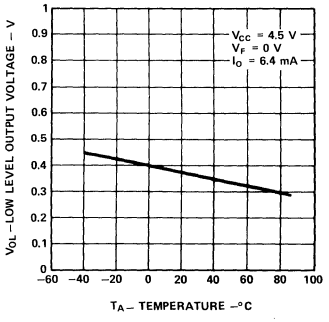


Figure 2. Typical Logic Low Output Voltage vs. Temperature.

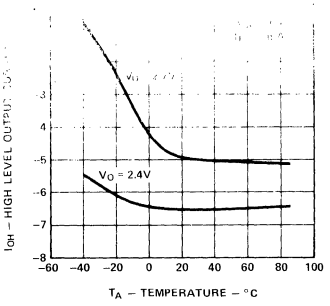


Figure 3. Typical Logic High Output Current vs. Temperature.

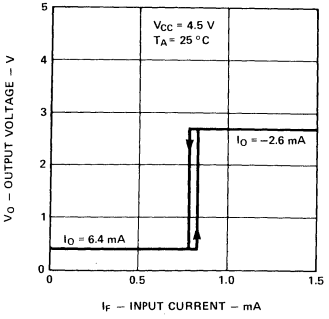


Figure 4. Output Voltage vs. Forward Input Current.

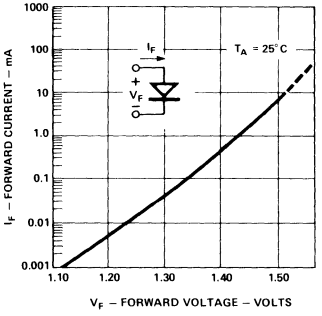
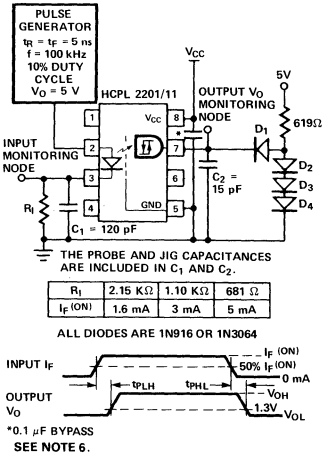


Figure 5. Typical Input Diode Forward Characteristic.



R_I	2.15 KΩ	1.10 KΩ	681 Ω
$I_{F(ON)}$	1.6 mA	3 mA	5 mA

Figure 6. Circuit for t_{PLH}, t_{PHL}, t_r, t_f.

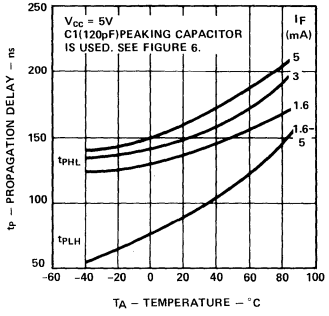


Figure 7. Typical Propagation Delays vs. Temperature.

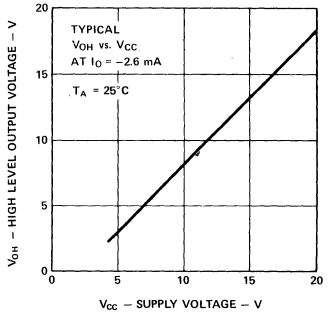


Figure 8. Typical Logic High Output Voltage vs. Supply Voltage.

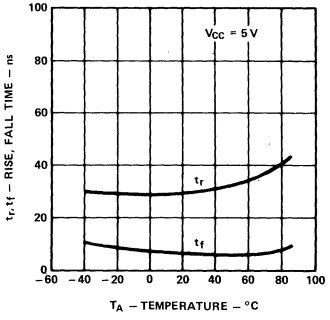


Figure 9. Typical Rise, Fall Time vs. Temperature.

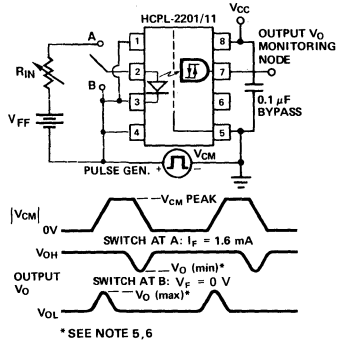


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

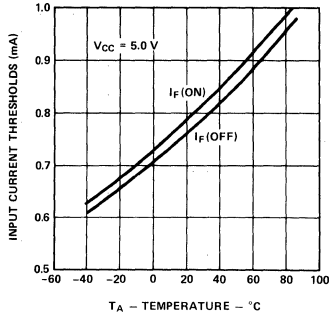


Figure 11. Typical Input Threshold Current vs. Temperature.

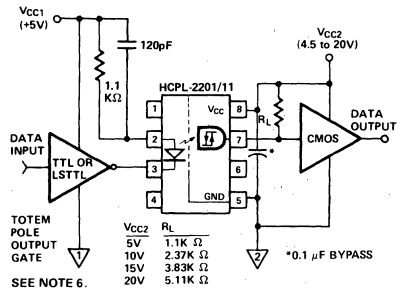


Figure 12. LSTTL to CMOS Interface Circuit.

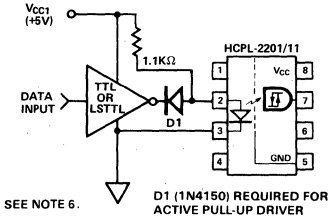


Figure 13. Alternative LED Drive Circuit.

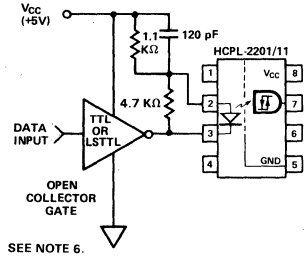


Figure 14. Series LED Drive with Open Collector Gate (4.7 kΩ Resistor Shunts I_{OH} from the LED).

Notes:

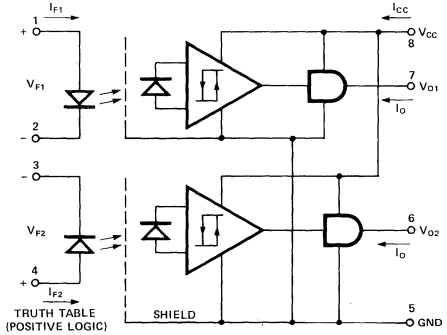
1. Derate total package power dissipation, P, linearly above 70°C free air temperature at a rate of 4.5 mW/°C.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
5. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state. $V_O < 0.8$ V. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state $V_O > 2.0$ V.
6. For HCPL-2202/12, V_O is on pin 6.
7. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
8. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 Vrms for one second (leakage detection current limit, $I_{I-O} \leq 5$ μA).

HEWLETT PACKARD

VERY HIGH CMR, WIDE V_{CC} DUAL LOGIC GATE OPTOCOUPLER

HCPL-2231
HCPL-2232

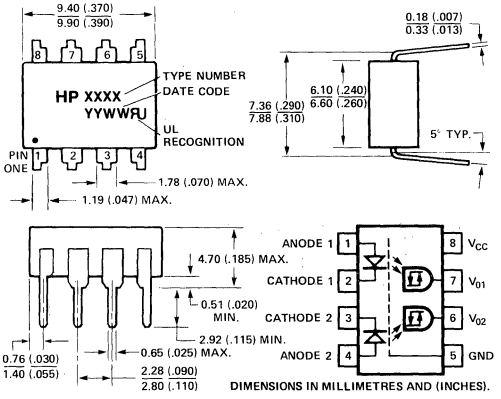
SCHEMATIC



TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	H
OFF	L

OUTLINE DRAWING



DIMENSIONS IN MILLIMETRES AND (INCHES).

Features

- **VERY HIGH COMMON MODE REJECTION 10 kV/μs AT 1000 V GUARANTEED (HCPL-2232)**
- **WIDE V_{CC} RANGE (4.5 TO 20 VOLTS)**
- **300 ns PROPAGATION DELAY GUARANTEED OVER THE FULL TEMPERATURE RANGE**
- **5 MBd TYPICAL SIGNAL RATE**
- **LOW INPUT CURRENT (1.8 mA)**
- **TOTEM POLE OUTPUT (NO PULLUP RESISTOR REQUIRED)**
- **GUARANTEED PERFORMANCE FROM -40°C TO +85°C**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **CSA APPROVED**
- **MIL-STD-1772 VERSION AVAILABLE (HCPL-5230/1)**

Applications

- **ISOLATION OF HIGH SPEED LOGIC SYSTEMS**
- **COMPUTER-PERIPHERAL INTERFACES**
- **MICROPROCESSOR SYSTEM INTERFACES**
- **GROUND LOOP ELIMINATION**
- **PULSE TRANSFORMER REPLACEMENT**
- **HIGH SPEED LINE RECEIVER**

Description

The HCPL-2231/2 are dual-channel, optically-coupled logic gates. The detectors have totem pole output stages and optical receiver input stages with built-in Schmitt triggers to provide logic compatible waveforms, eliminating the need for additional waveshaping.

A superior internal shield on the HCPL-2232 guarantees common mode transient immunity of 10,000 V/μs at a common mode voltage of 1000 V_{CM}.

The electrical and switching characteristics of the HCPL-2231/2 are guaranteed from -40°C to +85°C and a V_{CC} from 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed couplers. Logic signals are transmitted with a typical propagation delay of 150 ns.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Input Current (High)	$I_{F(ON)}$	1.8*	5	mA
Input Voltage (Low)	$V_{F(OFF)}$	—	0.8	Volts
Operating Temperature	T_A	-40	85	°C
Fan Out per Channel	N		4	TTL Loads

*The initial switching threshold is 1.8 mA or less. It is recommended that 2.5 mA be used to permit at least a 20% CTR degradation guardband.

OPTO COUPLERS

Recommended Circuit Design

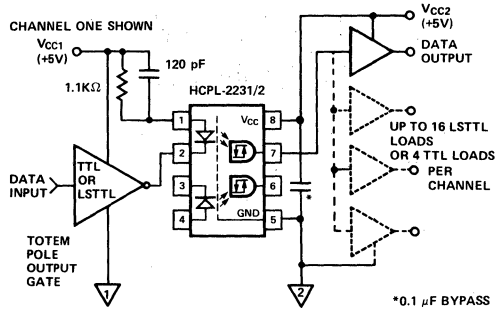


Figure 1. Recommended LSTTL to LSTTL Circuit

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Forward Input Current — I_F ..... 10 mA[1]
Peak Transient Input Current — I_F ..... 1 A[1]
(≤1 μs Pulse Width, 300 pps)
Reverse Input Voltage ..... 5 V[1]
Supply Voltage — V_{CC} ..... 0.0 V min., 20 V max.
Output Voltage — V_O ..... -0.5 V min., 20 V max.[1]
Total Package Power Dissipation ..... 294 mW
Output Power Dissipation — P_O per Channel ..... Fig. 8
Average Output Current — I_O per Channel ..... 25 mA

Electrical Specifications

-40°C ≤ T_A ≤ 85°C, 4.5 V ≤ V_{CC} ≤ 20 V, 1.8 mA ≤ $I_{F(ON)}$ ≤ 5 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, unless otherwise specified.
All Typicals at T_A = 25°C. See note 7.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads)		2, 4	1
Logic High Output Voltage	V_{OH}	2.4 2.7			Volts	I_{OH} = -2.6 mA I_{OH} = -0.4 mA	V_{CC} = 4.5 V	3, 4, 9	1
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	μA	V_O = 5.5 V	I_F = 5 mA V_{CC} = 4.5 V		1
				500	μA	V_O = 20 V			
Logic Low Supply Current	I_{CCL}		7.4	12.0	mA	V_{CC} = 5.5 V	V_F = 0 V I_O = Open		
			8.6	14.0	mA	V_{CC} = 20 V			
Logic High Supply Current	I_{CCH}		4.8	8.0	mA	V_{CC} = 5.5 V	I_F = 5 mA		
			5.4	10.0	mA	V_{CC} = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	15			mA	V_O = V_{CC} = 5.5 V	V_F = 0 V I_O = Open		1, 2
		20			mA	V_O = V_{CC} = 20 V			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5 V	I_F = 5 mA V_O = GND		1, 2
		-20			mA	V_{CC} = 20 V			
Input Forward Voltage	V_F		1.5	1.7	Volts	T_A = 25°C	I_F = 5 mA	5	1
				1.85					
Input Reverse Breakdown Voltage	BV_R	5			Volts	I_R = 10 μA			1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.7		mV/°C	I_F = 5 mA			
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C			3, 8
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 VDC			3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 VDC			3
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V			1
Input-Input Insulation Leakage Current	I_{I-I}		0.005		μA	Relative Humidity = 45% t = 5 s, V_{I-I} = 500 V			6
Resistance (Input-Input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500 V			6
Capacitance (Input-Input)	C_{I-I}		0.25		pF	f = 1 MHz			6

Switching Specifications $-40°C \le T_A \le 85°C$, $4.5\ V \le V_{CC} \le 20\ V$, $1.8\ mA \le I_{F\ (ON)} \le 5\ mA$, $0\ V \le V_{F\ (OFF)} \le 0.8\ V$. All Typicals at $T_A = 25°C$, $V_{CC} = 5\ V$, $I_{F\ (ON)} = 3\ mA$ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		150		ns	Without Peaking Capacitor	6, 7	1, 4
			150	300		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		110		ns	Without Peaking Capacitor	6, 7	1, 4
			90	300		With Peaking Capacitor		
Output Rise Time (10-90%)	t_r		30		ns		6, 10	1
Output Fall Time (90-10%)	t_f		7		ns		6, 10	1

Parameter	Symbol	Device	Min.	Units	Test Conditions		Figure	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	HCPL-2231	1,000	V/μs	$\|Vcm\| = 50\ V$	$I_F = 1.8\ mA$, $V_{CC} = 5\ V$, $T_A = 25°C$	11	1, 5
		HCPL-2232	10,000	V/μs	$\|Vcm\| = 1{,}000\ V$			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	HCPL-2231	1,000	V/μs	$\|Vcm\| = 50\ V$	$V_F = 0\ V$, $V_{CC} = 5\ V$, $T_A = 25°C$	11	1, 5
		HCPL-2232	10,000	V/μs	$\|Vcm\| = 1{,}000\ V$			

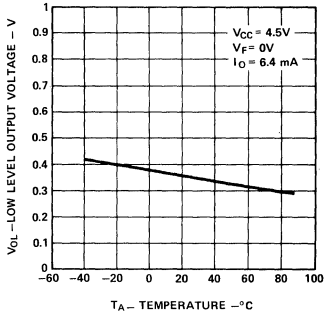


Figure 2. Typical Logic Low Output Voltage vs. Temperature

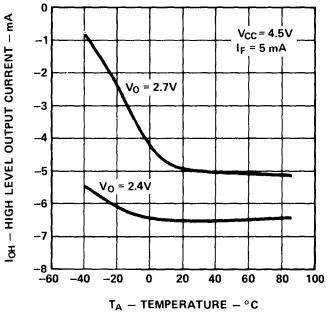


Figure 3. Typical Logic High Output Current vs. Temperature

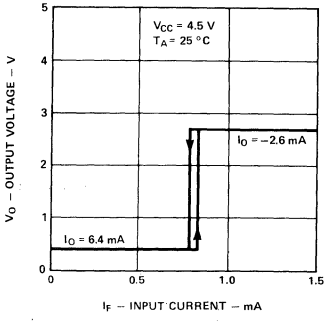


Figure 4. Output Voltage vs. Forward Input Current

OPTO COUPLERS

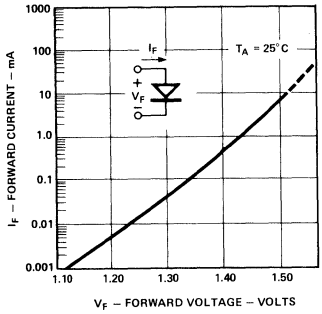
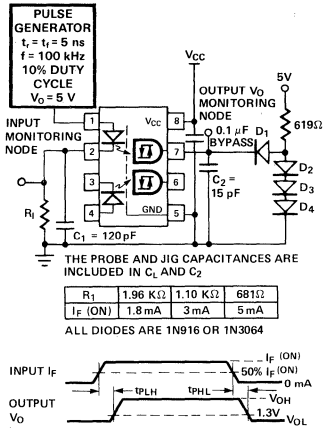


Figure 5. Typical Input Diode Forward Characteristic



Note: Channel one shown.

Figure 6. Circuit for t_{PLH}, t_{PHL}, t_r, t_f

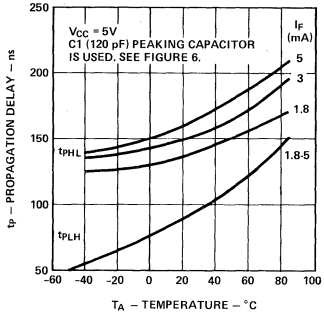


Figure 7. Typical Propagation Delays vs. Temperature

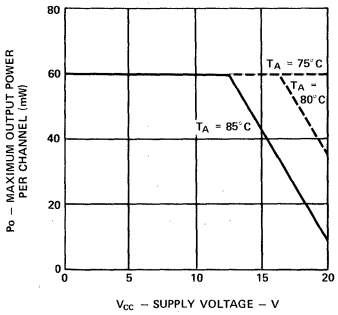


Figure 8. Maximum Output Power per Channel vs. Supply Voltage

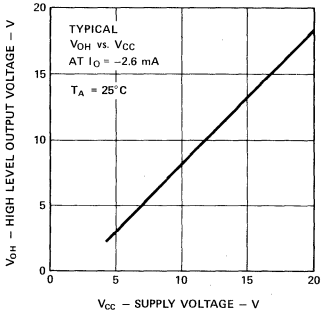


Figure 9. Typical Logic High Output Voltage vs. Supply Voltage

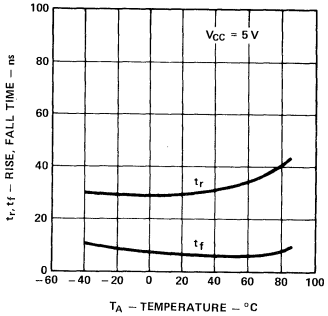


Figure 10. Typical Rise, Fall Time vs. Temperature

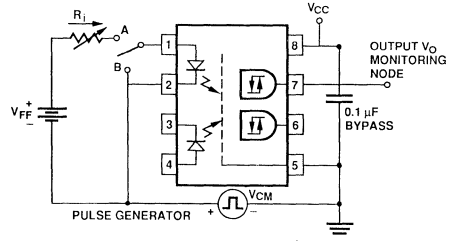


Figure 11. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

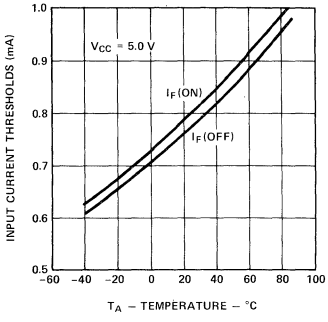


Figure 12. Typical Input Threshold Current vs. Temperature

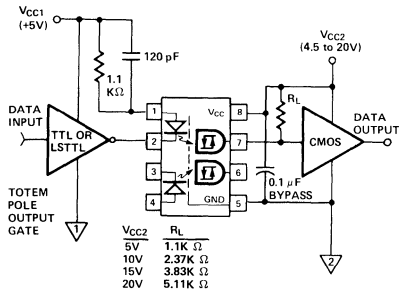


Figure 13. LSTTL to CMOS Interface Circuit

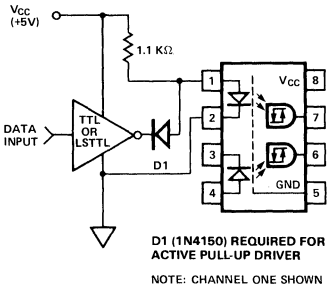


Figure 14. Alternate LED Drive Circuit

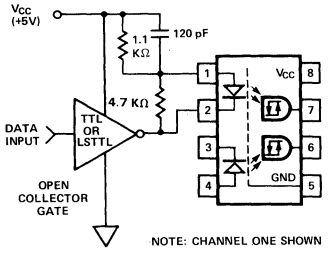


Figure 15. Series LED Drive with Open Collector Gate (4.7 kΩ Resistor Shunts I_{OH} from the LED)

Notes:

1. Each channel.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
5. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state. $V_O < 0.8$ V. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state $V_O > 2.0$ V.
6. Measured between pins 1 and 2, shorted together, and pins 3 and 4, shorted together.
7. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ μA).

HEWLETT PACKARD

New

Small Outline Very High CMR, Wide V_{CC} Logic Gate Optocoupler

Technical Data

HCPL-0201
HCPL-0211

Features

- **Surface Mountable**
- **Industry Standard SOIC-8 Footprint**
- **Compatible with Infrared Vapor Phase Reflow and Wave Soldering Processes**
- **Very High Common Mode Rejection, 10 kV/μs at Vcm = 1000 V Guaranteed (HCPL-0211) (Typical 15 kV/us)**
- **Wide V_{CC} Range (4.5 to 20 Volts)**
- **300 ns Propagation Delay Guaranteed over the Full Temperature Range**
- **5 MBd Typical Signal Rate**
- **Low Input Current (1.6 mA)**
- **Totem Pole Output (No Pullup Resistor Required)**
- **Guaranteed Performance from -40°C to +85°C**
- **Recognized under the Component Program of U.L. 1577, (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 Vac, 1 Minute**

Applications

- **Isolation of High Speed Logic Systems**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **High Speed Line Receiver**

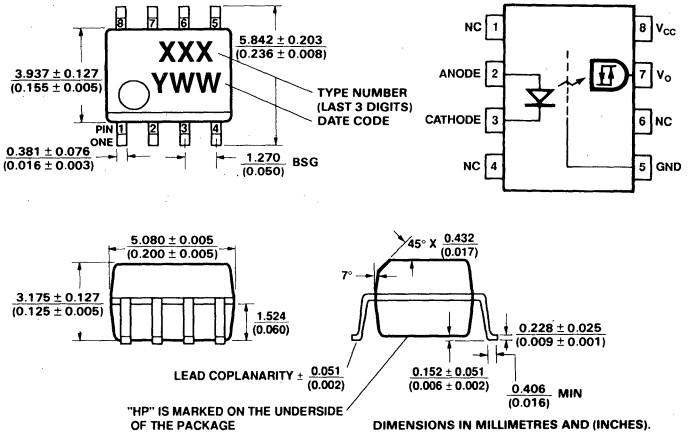
Description

These small outline very high CMR, wide V_{CC} Logic gate optocouplers are single-channel devices in an industry standard SOIC-8 footprint. They are electrically equivalent to the following HP optocouplers:

Small Outline
HCPL-0201
HCPL-0211
Standard DIP
HCPL-2201
HCPL-2211

The SOIC-8 package does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

Outline Drawing*



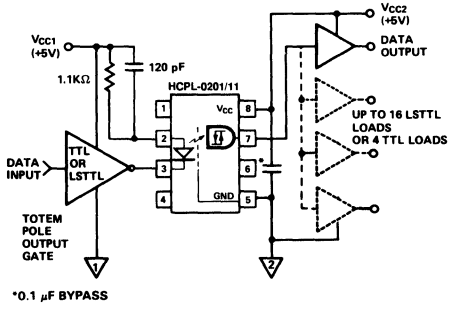
*See notes, following page.

The HCPL-0201/11 are single-channel, optically-coupled logic gates. The detectors have totem pole output stages and optical receiver input stages with built-in Schmitt triggers to provide logic-compatible waveforms, eliminating the need for additional waveshaping.

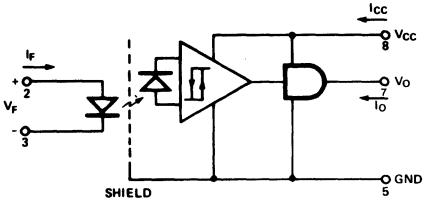
A superior internal shield on the HCPL-0211 guarantees common mode transient immunity of 10,000 V/μs at a common mode voltage of 1000 volts.

The electrical and switching characteristics of the HCPL-0201/11 are guaranteed from -40°C to +85°C and a V_{CC} from 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed couplers. Logic signals are transmitted with a typical propagation delay of 150 ns.

Recommended Circuit Design



Schematic



TRUTH TABLE (POSITIVE LOGIC)

INPUT	OUTPUT
H	H
L	L

Figure 1. Recommended LSTTL to LSTTL Circuit.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Forward Input Current	$I_{F(ON)}$	2.2*	5	mA
Forward Input Voltage	$V_{F(OFF)}$	–	0.8	Volts
Operating Temperature	T_A	-40	85	°C
Fan Out	N		4	TTL Loads

*2.2 mA condition includes an LED degradation guardband. Initial switching threshold is 1.6 mA or less. See Figure 11.

Absolute Maximum Ratings

(No Derating Required up to 70°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Reflow Temperature Profile ..... (See Figure 15)
Average Forward Input Current – I_F ..... 10 mA
Peak Transient Input Current – I_F ..... 1 A
(≤1 μs Pulse Width, 300 pps)
Reverse Input Voltage ..... 5 V
Supply Voltage – V_{CC} ..... 0.0 V min., 20 V max.
Output Voltage – V_O ..... -0.5 V min., 20 V max.
Total Package Power Dissipation – P ..... 210 mW[1]
Average Output Current – I_O ..... 25 mA

Electrical Specifications

-40°C ≤ T_A ≤ 85°C, 4.5 V ≤ V_{CC} ≤ 20 V, 1.6 mA ≤ $I_{F(ON)}$ ≤ 5 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, unless otherwise specified. All Typicals at T_A = 25°C. See Note 6.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads)		2, 4	
Logic High Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -2.6 mA	V_{CC} = 4.5 V	3, 4, 8	
		2.7			Volts	I_{OH} = -0.4 mA			
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	µA	V_O = 5.5 V	I_F = 5 mA, V_{CC} = 4.5 V		
				500	µA	V_O = 20 V			
Logic Low Supply Current	I_{CCL}		3.7	6.0	mA	V_{CC} = 5.5 V	V_F = 0 V, I_O = Open		
			4.3	7.0	mA	V_{CC} = 20 V			
Logic High Supply Current	I_{CCH}		2.4	4.0	mA	V_{CC} = 5.5 V	I_F = 5 mA, I_O = Open		
			2.7	5.0	mA	V_{CC} = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	15			mA	V_O = V_{CC} = 5.5 V	V_F = 0 V		2
		20			mA	V_O = V_{CC} = 20 V			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5 V	I_F = 5 mA, V_O = GND		2
		-20			mA	V_{CC} = 20 V			
Input Forward Voltage	V_F		1.5	1.7	Volts	T_A = 25°C	I_F = 5 mA	5	
				1.85	Volts				
Input Reverse Breakdown Voltage	BV_R	5			Volts	I_R = 10 µA			
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.7		mV/°C	I_F = 5 mA			
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%; t = 1 min., T_A = 25°C			3, 7
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 VDC			3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 VDC			3
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V, Pins 2 and 3			

Switching Specifications

$-40°C \le T_A \le 85°C$, $4.5\ V \le V_{CC} \le 20\ V$, $1.6\ mA \le I_{F(ON)} \le 5\ mA$, $0\ V \le V_{F(OFF)} \le 0.8\ V$. All Typicals at $T_A = 25°C$, $V_{CC} = 5\ V$, $I_{F(ON)} = 3\ mA$ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		150		ns	Without Peaking Capacitor	6, 7	4
			150	300		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		110		ns	Without Peaking Capacitor	6, 7	4
			90	300		With Peaking Capacitor		
Output Rise Time (10-90%)	t_r		30		ns		6, 9	
Output Fall Time (90-10%)	t_f		7		ns		6, 9	

Parameter	Symbol	Device	Min.	Units	Test Conditions		Fig.	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	HCPL-0201	1,000	V/μs	$\|Vcm\| = 50\ V$	$I_F = 1.6\ mA$, $V_{CC} = 5\ V$, $T_A = 25°C$	10	5
		HCPL-0211	10,000	V/μs	$\|Vcm\| = 1000\ V$			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	HCPL-0201	1,000	V/μs	$\|Vcm\| = 50\ V$	$V_F = 0\ V$, $V_{CC} = 5\ V$, $T_A = 25°C$	10	5
		HCPL-0211	10,000	V/μs	$\|Vcm\| = 1000\ V$			

Notes:

1. Derate total package power dissipation, P, linearly above 70°C free air temperature at a rate of 4.5 mW/°C.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
5. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state. $V_O < 0.8\ V$. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state $V_O > 2.0\ V$.
6. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
7. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\ge 3000\ V_{rms}$ for 1 second (leakage detection current limit, $I_{i-o} \le 5\ \mu A$).

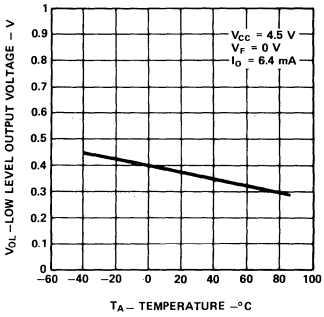


Figure 2. Typical Logic Low Output Voltage vs. Temperature.

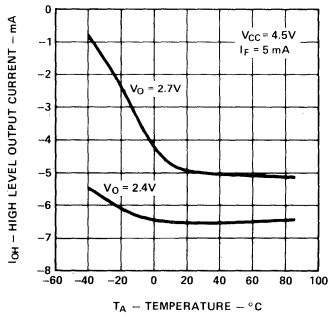


Figure 3. Typical Logic High Output Current vs. Temperature.

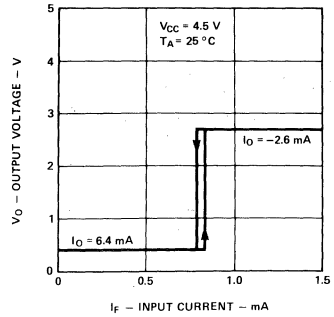


Figure 4. Output Voltage vs. Forward Input Current.

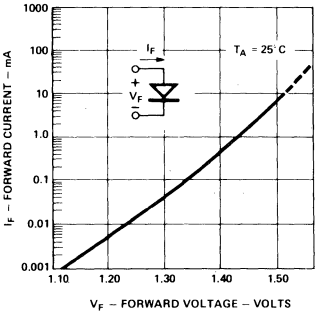
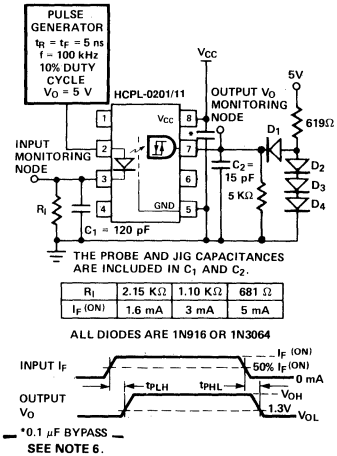


Figure 5. Typical Input Diode Forward Characteristic.



R_I	2.15 KΩ	1.10 KΩ	681 Ω
$I_{F(ON)}$	1.6 mA	3 mA	5 mA

Figure 6. Circuit for t_{PLH}, t_{PHL}, t_r, t_f.

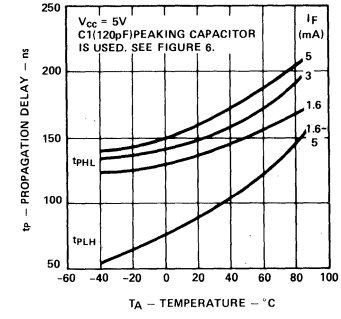


Figure 7. Typical Propagation Delays vs. Temperature.

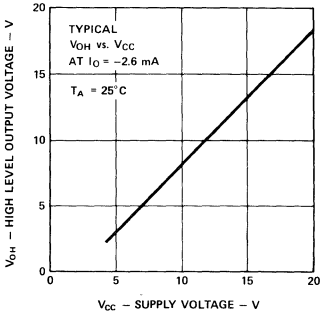


Figure 8. Typical Logic High Output Voltage vs. Supply Voltage.

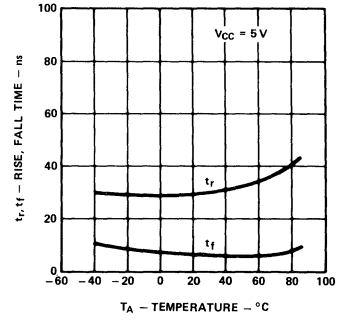


Figure 9. Typical Rise, Fall Time vs. Temperature.

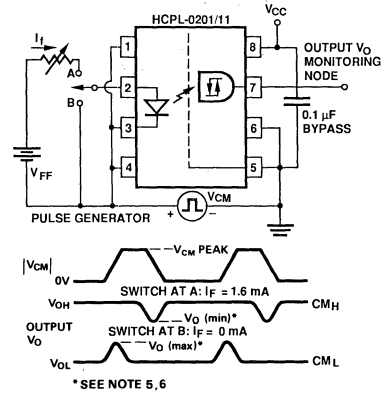


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

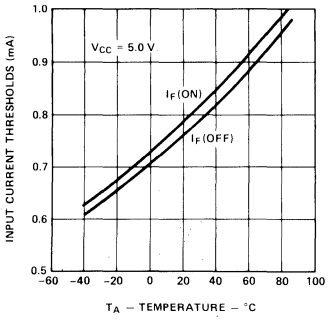


Figure 11. Typical Input Threshold Current vs. Temperature.

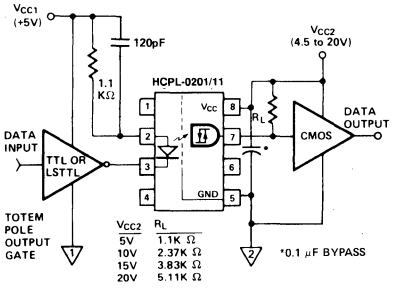


Figure 12. LSTTL to CMOS Interface Circuit.

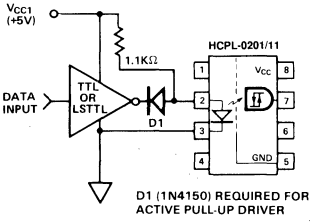


Figure 13. Alternative LED Drive Circuit.

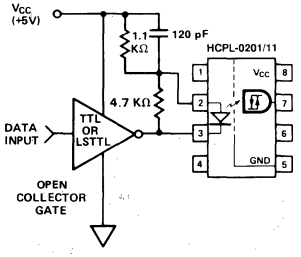


Figure 14. Series LED Drive with Open Collector Gate (4.7 kΩ Resistor Shunts I_{OH} from the LED).

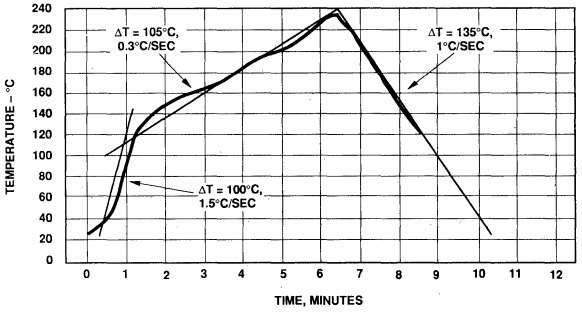
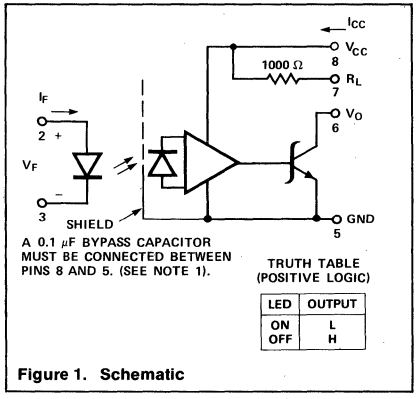


Figure 15. Maximum Solder Reflow Thermal Profile.

HEWLETT PACKARD

LOW INPUT CURRENT HIGH SPEED OPTOCOUPLER

HCPL-2300

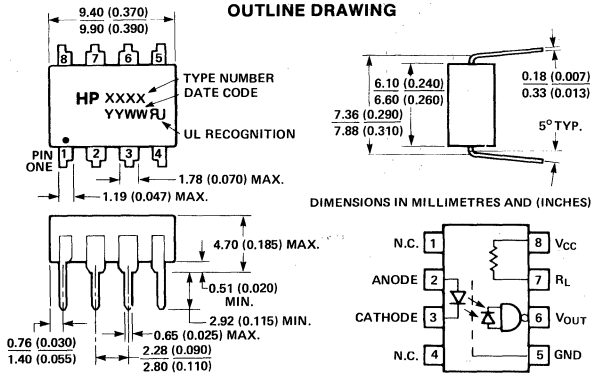


A 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5. (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

Figure 1. Schematic



Features

- **GUARANTEED LOW THRESHOLDS: I_F = 0.5 mA, $V_F \leq$ 1.5 V**
- **HIGH SPEED: GUARANTEED 5 MBd OVER TEMPERATURE**
- **VERSATILE: COMPATIBLE WITH TTL, LSTTL AND CMOS**
- **MORE EFFICIENT 820 nm AlGaAs LED**
- **INTERNAL SHIELD FOR GUARANTEED COMMON MODE REJECTION**
- **SCHOTTKY CLAMPED, OPEN COLLECTOR OUTPUT WITH OPTIONAL INTEGRATED PULL-UP RESISTOR**
- **STATIC AND DYNAMIC PERFORMANCE GUARANTEED FROM -40°C TO 85°C**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **CSA APPROVED**

Applications

- **GROUND LOOP ELIMINATION**
- **COMPUTER-PERIPHERAL INTERFACES**
- **LEVEL SHIFTING**
- **MICROPROCESSOR SYSTEM INTERFACES**
- **DIGITAL ISOLATION FOR A/D, D/A CONVERSION**
- **RS-232-C INTERFACE**
- **HIGH SPEED, LONG DISTANCE ISOLATED LINE RECEIVER**

Description

The HCPL-2300 optocoupler combines an 820 nm AlGaAs photon emitting diode with an integrated high gain photon detector. This combination of Hewlett-Packard designed and manufactured semiconductor devices brings new high performance capabilities to designers of isolated logic and data communication circuits.

The new low current, high speed AlGaAs emitter manufactured with a unique diffused junction, has the virtue of fast rise and fall times at low drive currents. Figure 6 illustrates the propagation delay vs. input current characteristic. These unique characteristics enable this device to be used in an RS-232-C interface with ground loop isolation and improved common mode rejection. As a line receiver, the HCPL-2300 will operate over longer line lengths for a given data rate because of lower I_F and V_F specifications.

The output of the shielded integrated detector circuit is an open collector Schottky clamped transistor. The shield, which shunts capacitively coupled common mode noise to ground, provides a guaranteed transient immunity specification of 100 V/μs. The output circuit includes an optional integrated 1000 Ohm pull-up resistor for the open collector. This gives designers the flexibility to use the internal resistor for pull-up to five volt logic or to use an external resistor for 18 volt CMOS logic.

The Electrical and Switching Characteristics of the HCPL-2300 are guaranteed over a temperature range of -40°C to 85°C. This enables the user to confidently design a circuit which will operate under a broad range of operating conditions.

Recommended Operating Conditions

		Sym.	Min.	Max.	Units
Input Voltage, Low Level		V_{FL}	-2.5	0.8	V
Input Current High Level	0° C to 85° C	I_{FH}	0.5	1.0	mA
	-40° C to 85° C		0.5	0.75	
Supply Voltage, Output		V_{CC}	4.75	5.25	V
Fan Out (TTL Load)		N		5	
Operating Temperature		T_A	-40	85	°C

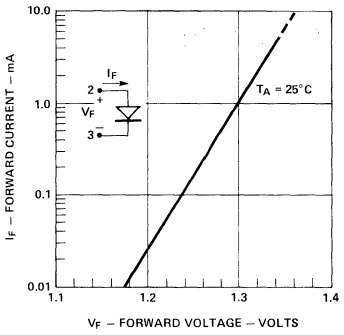


Figure 2. Typical Input Diode Forward Characteristic.

Absolute Maximum Ratings

(No derating required)

Parameter	Symbol	Min.	Max.	Units	Reference
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	85	°C	
Lead Solder Temperature	260° C for 10 s. (1.6 mm below seating plane)				
Average Forward Input Current	I_F		5	mA	See Note 2
Reverse Input Voltage	V_R		3.5	V	
Supply Voltage	V_{CC}	0.0	7.0	V	
Pull-up Resistor Voltage	V_{RL}	-0.5	V_{CC}	V	
Output Collector Current	I_O	-25	25	mA	
Input Power Dissipation	P_I		10	mW	
Output Collector Power Dissipation	P_O		40	mW	
Output Collector Voltage	V_O	-0.5	18	V	

Electrical Specifications

For $-40°C \le T_A \le 85°C$, $4.75\ V \le V_{CC} \le 5.25\ V$, $V_{FL} \le 0.8\ V$, unless otherwise specified.
All typicals at $T_A = 25°C$, $V_{CC} = 5\ V$, unless otherwise specified. See note 1.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		0.05	250	μA	$V_F = 0.8\ V$, $V_O = 18\ V$	4	
Low Level Output Voltage	V_{OL}		0.4	0.5	V	$I_F = 0.5$ mA, I_{OL} (Sinking) = 8 mA	3	
High Level Supply Current	I_{CCH}		4.0	6.3	mA	$I_F = 0$ mA, $V_{CC} = 5.25\ V$		
Low Level Supply Current	I_{CCL}		6.2	10.0	mA	$I_F = 1.0$ mA, $V_{CC} = 5.25\ V$		
Input Forward Voltage	V_F	1.0	1.3	1.5	Volts	$T_A = 25°C$, $I_F = 1.0$ mA	2	
		0.85		1.65				
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	$I_F = 1.0$ mA		
Input Reverse Breakdown Voltage	BV_R	4.5			Volts	$T_A = 25°C$, $I_R = 10\ \mu A$		
		3.5						
Input Capacitance	C_{IN}		18		pF	$V_F = 0\ V$, f = 1 MHz		
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min., $T_A = 25°C$		3, 9
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	$V_{I-O} = 500\ V$		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3
Internal Pull-up Resistor	R_L	680	1000	1700	Ohms	$T_A = 25°C$		

Switching Specifications

For -40° C ≤ T_A ≤ 85° C, 0.5 mA ≤ I_{FH} ≤ 0.75 mA;
For 0° C ≤ T_A ≤ 85° C, 0.5 mA ≤ I_{FH} ≤ 1.0 mA; With 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{FL} ≤ 0.8 V, unless otherwise specified.
All typicals at T_A = 25° C, V_{CC} = 5 V, I_{FH} = 0.625 mA, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		95		ns	C_P = 0 pF	5, 6, 8	4, 8
			85	160		C_P = 20 pF	5, 8	
Propagation Delay Time to Logic Low Output Level	t_{PHL}		110		ns	C_P = 0 pF	5, 6, 8	5, 8
			35	200		C_P = 20 pF	5, 8	
Output Rise Time (10-90%)	t_r		40		ns	C_P = 20 pF	7, 8	8
Output Fall Time (90-10%)	t_f		20		ns			
Common Mode Transient Immunity at High Output Level	$\lvert CM_H \rvert$	100	400		V/μs	V_{CM} = 50 V (peak), V_O (min.) = 2 V, R_L = 560Ω, I_F = 0 mA	9, 10	6
Common Mode Transient Immunity at Low Output Level	$\lvert CM_L \rvert$	100	400		V/μs	V_{CM} = 50 V (peak), V_O (max.) = 0.8 V, R_L = 560Ω, I_F = 0.5 mA	9, 10	7

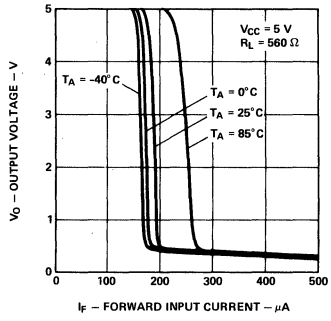


Figure 3. Typical Output Voltage vs. Forward Input Current vs. Temperature.

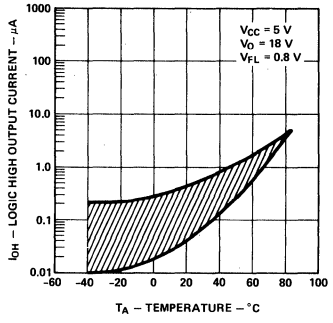


Figure 4. Typical Logic High Output Current vs. Temperature.

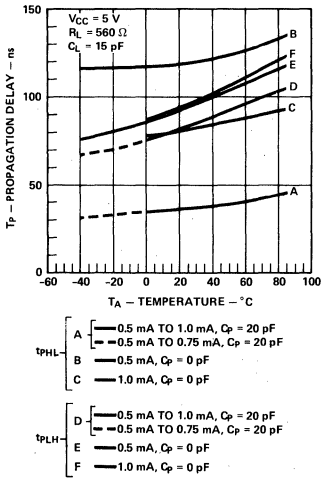


Figure 5. Typical Propagation Delay vs. Temperature and Forward Current With and Without Application of a Peaking Capacitor.

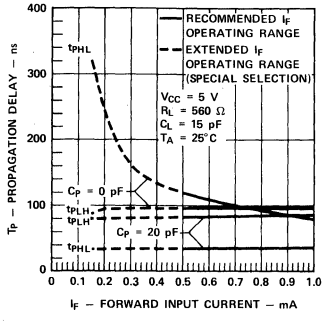


Figure 6. Typical Propagation Delay vs. Forward Current.

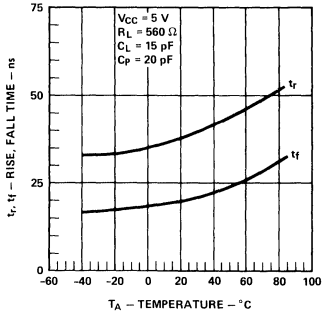


Figure 7. Typical Rise, Fall Time vs. Temperature.

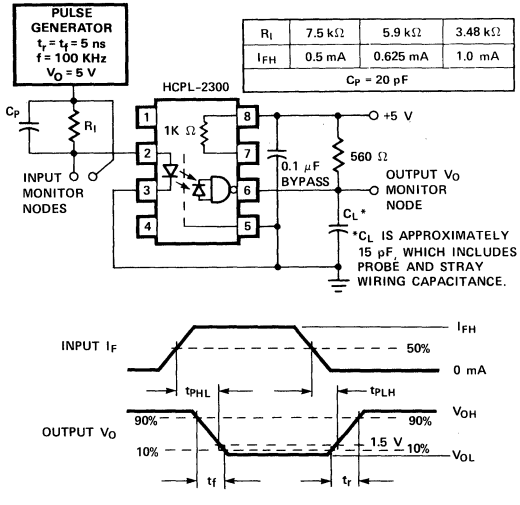


Figure 8. Test Circuit for t_{PHL}, t_{PLH}, t_r and t_f.

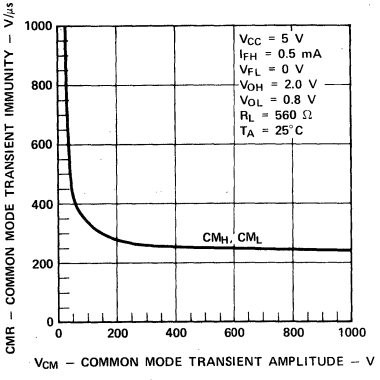
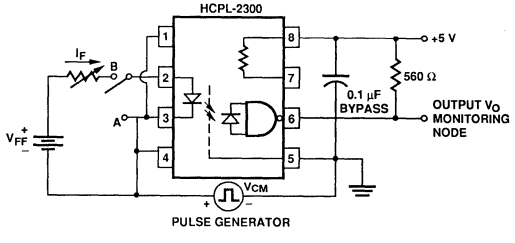
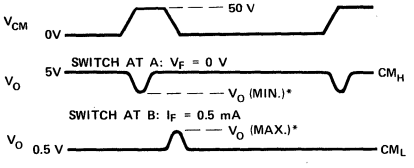


Figure 9. Typical Common Mode Transient Immunity vs. Common Mode Transient Amplitude.





*SEE NOTES 6, 7.

Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

OPTO COUPLERS

Applications

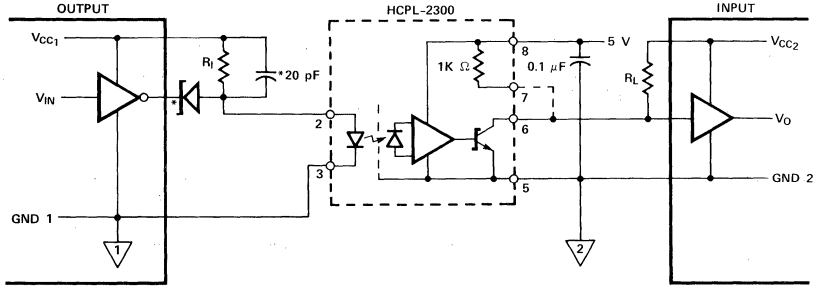
The HCPL-2300 optocoupler has the unique combination of low 0.5 mA LED operating drive current at a 5 MBd speed performance. Low power supply current requirement of 10 mA maximum and the ability to provide isolation between logic systems fulfills numerous applications ranging from logic level translations, line receiver and party line receiver applications, microprocessor I/O port isolation, etc. The open collector output allows for wired-OR arrangement. Specific interface circuits are illustrated in Figures 11 through 18 with corresponding component values, performance data and recommended layout.

For -40° C to 85° C operating temperature range, a mid range LED forward current (I_F) of 0.625 mA is recommended in order to prevent overdriving the integrated circuit detector due to increased LED efficiency at temperatures between 0° C and -40° C. For narrower temperature range of 0° C to 85° C, a suggested operating LED current of 0.75 mA is recommended for the mid range operating point and for minimal propagation delay skew. A peaking capacitance of 20 pF in parallel with the current limiting resistor for the LED shortens t_{PHL} by approximately 33% and t_{PLH} by 13%. Maintaining LED forward voltage (V_F) below 0.8 V will guarantee that the HCPL-2300 output is off.

The recommended shunt drive technique for TTL/LSTTL/CMOS of Figure 11 provides for optimal speed performance, no leakage current path through the LED, and reduced common mode influences associated with series switching of a "floating" LED. Alternate series drive techniques with either an active CMOS inverter or an open collector TTL/LSTTL inverter are illustrated in Figures 12 and 13 respectively. Open collector leakage current of 250 μA has been compensated by the 3.16K Ohms resistor (Figure 13) at the expense of twice the operating forward current.

An application of the HCPL-2300 as an unbalanced line receiver for use in long line twisted wire pair communication links is shown in Figure 14. Low LED I_F and V_F allow longer line length, higher speed and multiple stations on the line in comparison to higher I_F, V_F optocouplers. Greater speed performance along with nearly infinite common mode immunity are achieved via the balanced split phase circuit of Figure 15. Basic balanced (differential line receiver can be accomplished with one HCPL-2300 in Figure 15, but with a typical 400 V/μs common mode immunity. Data rate versus distance for both the above unbalanced and balanced line receiver applications are compared in Figure 16. The RS-232-C interface circuit of Figure 17 provides guaranteed minimum common mode immunity of 100 V/μs while maintaining the 2:1 dynamic range of I_F.

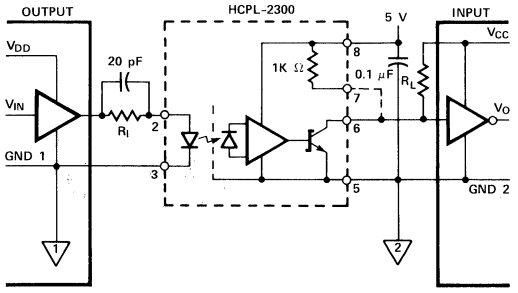
A recommended layout for use with an internal 1000 Ohms resistor or an external pull-up resistor and required V_{CC} bypass capacitor is given in Figure 18. V_{CC1} is used with an external pull-up resistor for output voltage levels (V_O) greater than or equal to 5 V. As illustrated in Figure 18, an optional V_{CC} and GND trace can be located between the input and the output leads of the HCPL-2300 to provide additional noise immunity at the compromise of insulation capability (V_{I-O}).



V_{IN} V_{DC}	V_{CC1} V_{DC}	R_I kΩ	R_L kΩ	V_{CC2} V_{DC}
5	5	6.19	1 (INTERNAL)	5
10	10	14.7	2.37	10
15	15	21.5	3.16	15

*SCHOTTKY DIODE (HP 5082-2800, OR EQUIVALENT) AND 20 pF CAPACITOR ARE NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

Figure 11. Recommended Shunt Drive Circuit for Interfacing Between TTL/LSTTL/CMOS Logic Systems.



V_{IN} V_{DC}	V_{DD} V_{DC}	R_I kΩ	R_L kΩ	V_{CC} V_{DC}
5	5	5.11	1 (INTERNAL)	5
10	10	13.3	2.37	10
15	15	19.6	3.16	15

Figure 12. Active CMOS Series Drive Circuit.

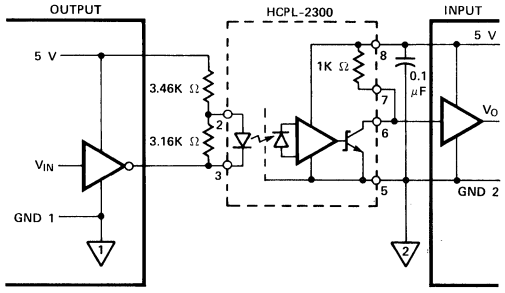
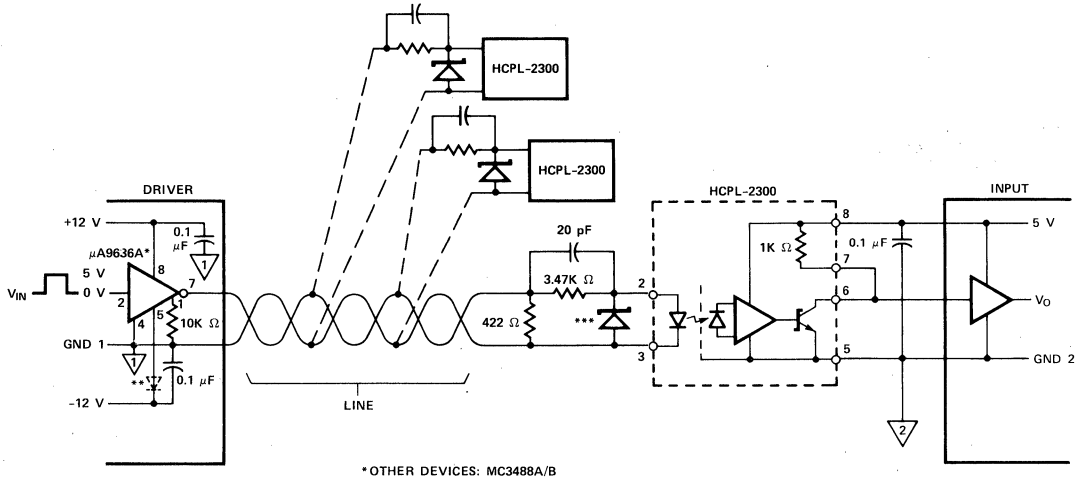


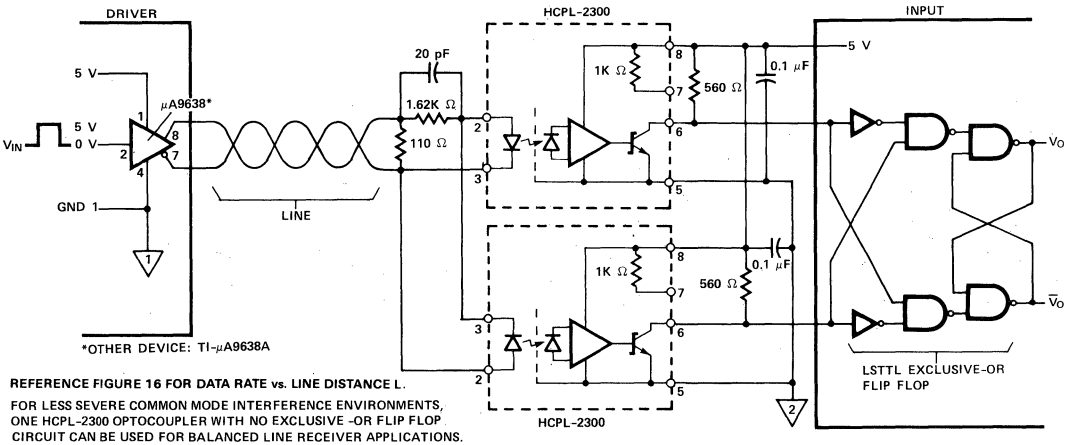
Figure 13. Series Drive from Open Collector TTL/LSTTL Units.



*OTHER DEVICES: MC3488A/B
TI-μA9636A.
**MAY BE REQUIRED ON OLDER VERSIONS OF μA9636A.
***SCHOTTKY DIODE (HP 5082-2800, OR EQUIVALENT).

REFERENCE FIGURE 16 FOR DATA RATE vs. LINE DISTANCE L.

Figure 14. Application of HCPL-2300 as Isolated, Unbalanced Line Receiver(s).



REFERENCE FIGURE 16 FOR DATA RATE vs. LINE DISTANCE L.

FOR LESS SEVERE COMMON MODE INTERFERENCE ENVIRONMENTS, ONE HCPL-2300 OPTOCOUPLER WITH NO EXCLUSIVE -OR FLIP FLOP CIRCUIT CAN BE USED FOR BALANCED LINE RECEIVER APPLICATIONS.
$V_O = V_{IN}$.

Figure 15. Application of Two HCPL-2300 Units Operating as an Isolated, High Speed, Balanced, Split Phase Line Receiver with Significantly Enhanced Common Mode Immunity.

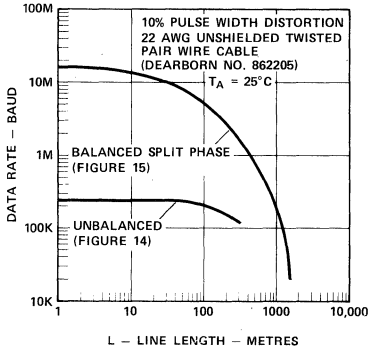


Figure 16. Typical Point to Point data Rate vs. Length of Line for Unbalanced (Figure 14) and Balanced (Figure 15) Line Receivers using HCPL-2300 Optocouplers.

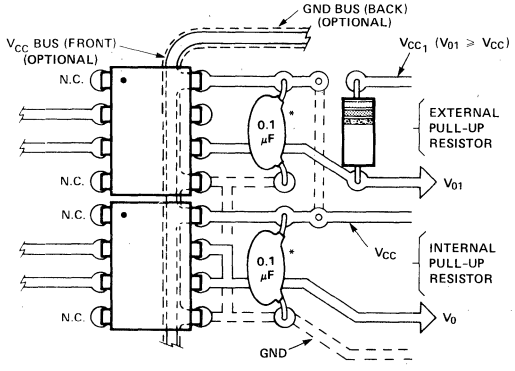


Figure 18. Recommended Printed Circuit Board Layout.

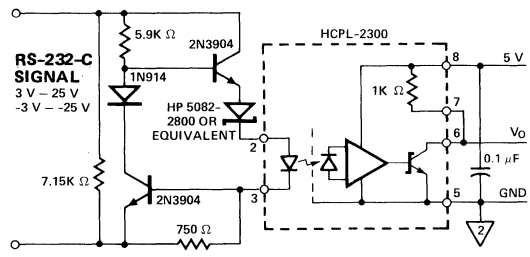


Figure 17. RS-232-C Interface Circuit with HCPL-2300. 0°C < T_A < 85°C.

NOTES:

1. Bypassing the power supply line is required with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 18. The power supply bus for the optocoupler(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.
2. Peaking circuits may produce transient input currents up to 100 mA, 500 ns maximum pulse width, provided average current does not exceed 5 mA.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
7. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} < 0.8 V).
8. C_P is the peaking capacitance. Refer to test circuit in Figure 8.
9. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ μA).

HEWLETT PACKARD

20 M Baud High CMR Logic Gate Optocoupler

HCPL-2400
HCPL-2411

Features

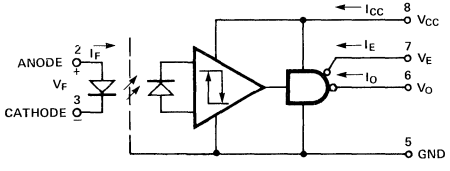
- High Speed: 40 MBd Typical Data Rate
- High Common Mode Rejection
  HCPL-2400: 10 kV/μs @ V_{CM} = 50 V (typical)
  HCPL-2411: 10 kV/μs @ V_{CM} = 300 V (typical)
- AC Performance Guaranteed over Temperature
- Compatible with TTL, STTL, LSTTL, and HCMOS Logic Families
- High Speed AlGaAs Emitter
- Three State Output (No Pull-Up Resistor Required)
- High Power Supply Noise Immunity
- Recognized under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 Vac, 1 Minute
- CSA Approved
- MIL-STD-1772 Version Available (HCPL-5400/1)

Applications

- Isolation of High Speed Logic Systems
- Computer-Peripheral Interfaces
- Isolated Bus Driver (Networking Applications)
- Switching Power Supplies
- Ground Loop Elimination
- High Speed Disk Drive I/O
- Digital Isolation for A/D, D/A Conversion
- Pulse Transformer Replacement

OPTO COUPLERS

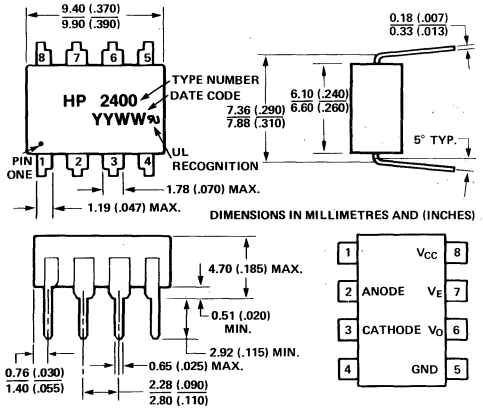
Schematic



TRUTH TABLE
(POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	L	L
OFF	L	H
ON	H	Z
OFF	H	Z

Outline Drawing



Description

The HCPL-2400/11 high speed optocouplers combine an 820 nm AlGaAs light emitting diode with a high speed photodetector. This combination results in very high data rate capability and low input current. The three state output eliminates the need for a pull-up resistor and allows for direct drive of data buses. The hysteresis provides differential mode noise immunity and minimizes the potential for output signal chatter. Improved power supply rejection minimizes the need for special power supply bypassing precautions.

The electrical and switching characteristics of the HCPL-2400/11 are guaranteed over the temperature range of 0°C to 70°C.

The HCPL-2400/11 are compatible with TTL, STTL, LSTTL, and HCMOS logic families. When Schottky type TTL devices (STTL) are used, a data rate performance of 20 MBd over temperature is guaranteed when using the application circuit of Figure 12. Typical data rates are 40 MBd.

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Power Supply Voltage	V_{CC}	4.75	5.25	Volts
Input Current (High)	$I_{F(ON)}$	4	8	mA
Input Voltage (Low)	$V_{F(OFF)}$	–	0.8	Volts
Enable Voltage (Low)	V_{EL}	0	0.8	Volts
Enable Voltage (High)	V_{EH}	2.0	V_{CC}	Volts
Operating Temperature	T_A	0	70°	°C
Fan Out	N		5	TTL Loads

Absolute Maximum Ratings

(No derating required up to 85°C)

Parameter	Symbol	Minimum	Maximum	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	85	°C	
Lead Solder Temperature	260°C for 10 s. (1.6 mm below seating plane)				
Average Forward Input Current	I_F		10.0	mA	
Peak Forward Input Current	I_{FPK}		20.0	mA	9
Reverse Input Voltage	V_R	2.0		V	
Supply Voltage	V_{CC}	0	7.0	V	
Three State Enable Voltage	V_E	-0.5	10.0	V	
Average Output Collector Current	I_O	-25.0	25.0	mA	
Output Collector Voltage	V_O	-0.5	10.0	V	
Output Collector Power Dissipation	P_O		40.0	mW	

Electrical Specifications

For $0°C \le T_A \le 70°C$, $4.75\ V \le V_{CC} \le 5.25\ V$, $4\ mA \le I_{F(ON)} \le 8\ mA$, $2.0\ V \le V_{EH} \le 5.25$, $0\ V \le V_{EL} \le 0.8\ V$, $0\ V \le V_{F(OFF)} \le 0.8\ V$ except where noted. All typicals at $T_A = 25°C$, $V_{CC} = 5\ V$, $I_{F(ON)} = 6.0\ mA$, $V_{F(OFF)} = 0\ V$ except where noted. See Note 9.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	$I_{OL} = 8.0\ mA$ (5 TTL Loads)	1	
Logic High Output Voltage	V_{OH}	2.4			Volts	$I_{OH} = -4.0\ mA$	2	
Output Leakage Current	I_{OHH}			100	μA	$V_O = 5.25\ V$, $V_F = 0.8\ V$		
Logic High Enable Voltage	V_{EH}	2.0			Volts			
Logic Low Enable Voltage	V_{EL}			0.8	Volts			
Logic High Enable Current	I_{EH}			20	μA	$V_E = 2.4\ V$		
				100	μA	$V_E = 5.25\ V$		
Logic Low Enable Current	I_{EL}		-0.28	-0.4	mA	$V_E = 0.4\ V$		
Logic Low Supply Current	I_{CCL}		19	26	mA	$V_{CC} = 5.25\ V$		
Logic High Supply Current	I_{CCH}		17	26	mA	$V_E = 0\ V$, I_O = Open		
High Impedance State Supply Current	I_{CCZ}		22	28	mA	$V_{CC} = 5.25\ V$, $V_E = 5.25\ V$		
High Impedance State Output Current	I_{OZL}			20	μA	$V_O = 0.4\ V$, $V_E = 2\ V$		
	I_{OZH}			20	μA	$V_O = 2.4\ V$		
	I_{OZH}			100	μA	$V_O = 5.25\ V$		
Logic Low Short Circuit Output Current	I_{OSL}		52		mA	$V_O = V_{CC} = 5.25\ V$, $I_F = 8\ mA$		1
Logic High Short Circuit Output Current	I_{OSH}		-45		mA	$V_{CC} = 5.25\ V$, $I_F = 0\ mA$, V_O = GND		1
Input Current Hysteresis	I_{HYS}		0.25		mA	$V_{CC} = 5\ V$	3	
Input Forward Voltage	V_F	1.1	1.3	1.5	Volts	$T_A = 25°C$, $I_F = 8\ mA$	4	
		1.0		1.55				
Input Reverse Breakdown Voltage	BV_R	3.0	5.0		Volts	$T_A = 25°C$, $I_R = 10\ μA$		
		2.0						
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.44		mV/°C	$I_F = 6\ mA$	4	
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min, $T_A = 25°C$		2, 10
Input-Output Resistance	R_{I-O}		10^{12}		Ω	$V_{I-O} = 500$ VDC		2
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, $V_{I-O} = 0$ VDC		2
Input Capacitance	C_{IN}		20		pF	f = 1 MHz, $V_F = 0\ V$, Pins 2 and 3		

Switching Specifications

$0°C \le T_A \le 70°C$, $4.75\ V \le V_{CC} \le 5.25\ V$, $0.0\ V \le V_{EN} \le 0.8\ V$, $4\ mA \le I_F \le 8.0\ mA$. All typicals $V_{CC} = 5\ V$, $T_A = 25°C$, $I_F = 6.0\ mA$ except where noted.

Parameter	Symbol		Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}				55	ns	$I_{F(ON)} = 7.0\ mA$		5, 6, 7	4
			15	33	60	ns			5, 6, 7	3
Propagation Delay Time to Logic High Output Level	t_{PLH}				55	ns	$I_{F(ON)} = 7.0\ mA$		5, 6, 7	4
			15	30	60	ns			5, 6, 7	3
Pulse Width Distortion	$\lvert t_{PHL}-t_{PLH} \rvert$			2	15	ns	$I_{F(ON)} = 7.0\ mA$		5, 8	4
				3	25	ns			5, 8	
Propagation Delay Skew	t_{PSK}				35	ns	Per Notes & Text		14, 15	5
Output Rise Time	t_r			20		ns			5	
Output Fall Time	t_f			10		ns			5	
Output Enable Time to Logic High	t_{PZH}			15		ns			9, 10	
Output Enable Time to Logic Low	t_{PZL}			30		ns			9, 10	
Output Disable Time from Logic High	t_{PHZ}			20		ns			9, 10	
Output Disable Time from Logic Low	t_{PLZ}			15		ns			9, 10	
Logic High Common Mode Transient Immunity	$\lvert CM_H \rvert$	2400	1000	10,000		V/μs	$V_{CM} = 50\ V$	$T_A = 25°C$, $I_F = 0\ mA$	11	6
		2411	1000	10,000		V/μs	$V_{CM} = 300\ V$			
Logic Low Common Mode Transient Immunity	$\lvert CM_L \rvert$	2400	1000	10,000		V/μs	$V_{CM} = 50\ V$	$T_A = 25°C$, $I_F = 4\ mA$	11	6
		2411	1000	10,000		V/μs	$V_{CM} = 300\ V$			
Power Supply Noise Immunity	PSNI			0.5		V_{p-p}	$V_{CC} = 5.0\ V$, $48\ Hz \le F_{AC} \le 50\ MHz$			7

Notes:

1. Duration of output short circuit time not to exceed 10 ms.
2. Device considered a two terminal device: pins 1-4 shorted together, and pins 5-8 shorted together.
3. t_{PHL} propagation delay is measured from the 50% level on the rising edge of the input current pulse to the 1.5 V level on the falling edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% level on the falling edge of the input current pulse to the 1.5 V level on the rising edge of the output pulse.
4. This specification simulates the worst case operating conditions of the HCPL-2400/11 over the recommended operating temperature and V_{CC} range with the suggested applications circuit of Figure 12.
5. Propagation delay skew is discussed later in this data sheet.
6. CM_H is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic high state ($V_{O(MIN)} > 2.0$ V). CM_L is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic low state ($V_{O(MAX)} < 0.8$ V).
7. Power Supply Noise Immunity is the peak to peak amplitude of the ac ripple voltage on the V_{CC} line that the device will withstand and still remain in the desired logic state. For desired logic high state, $V_{OH(MIN)} > 2.0$ V, and for desired logic low state, $V_{OL(MAX)} < 0.8$ volts.
8. Peak Forward Input Current pulse width < 50 μs at 1 KHz maximum repetition rate.
9. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
10. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 Vrms for one second (leakage detection current limit, $I_{I-O} \leq 5$ μA).

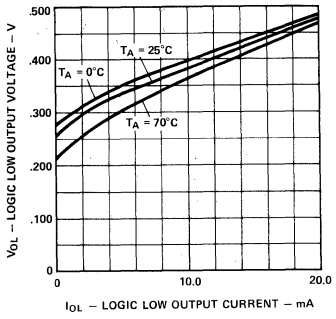


Figure 1. Typical Logic Low Output Voltage vs. Logic Low Output Current.

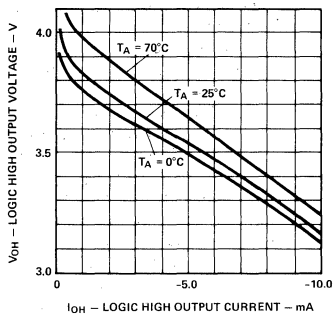


Figure 2. Typical Logic High Output Voltage vs. Logic High Output Current.

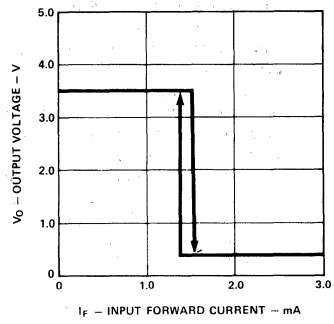


Figure 3. Typical Output Voltage vs. Input Forward Current.

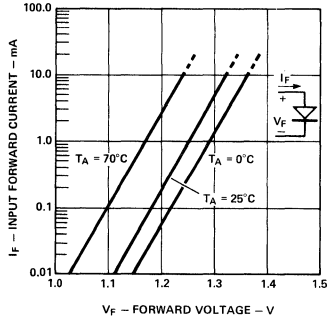


Figure 4. Typical Diode Input Forward Current Characteristic.

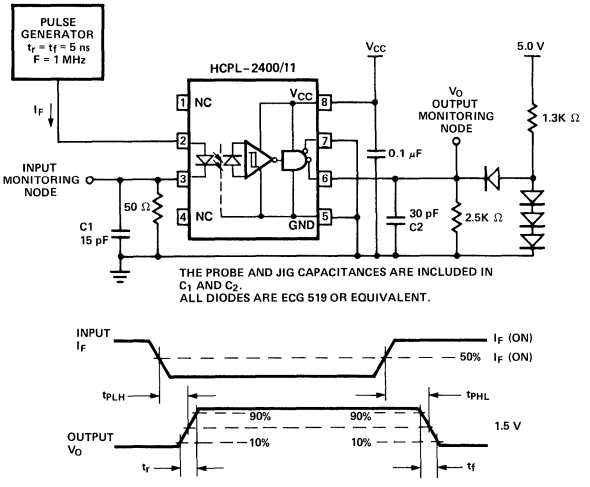


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f.

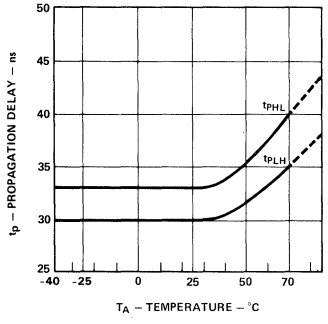


Figure 6. Typical Propagation Delay vs. Ambient Temperature.

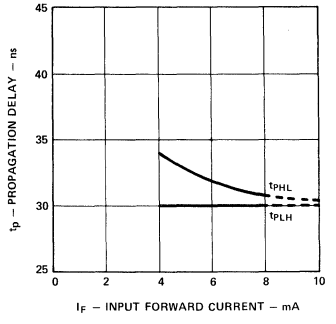


Figure 7. Typical Propagation Delay vs. Input Forward Current.

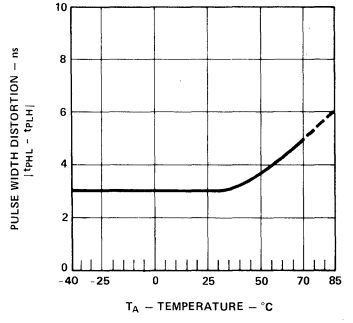
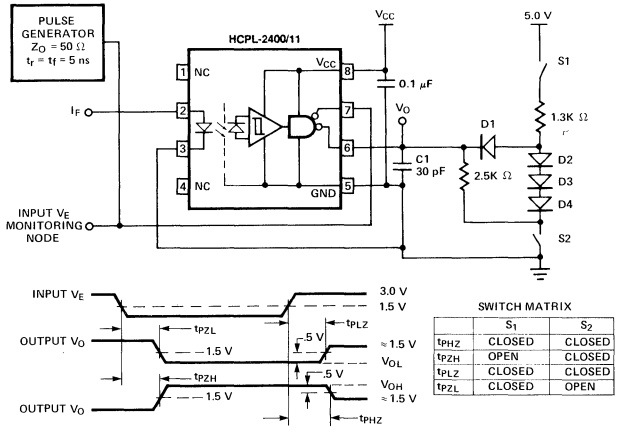


Figure 8. Typical Pulse Width Distortion vs. Ambient Temperature.



	S_1	S_2
t_{PHZ}	CLOSED	CLOSED
t_{PZH}	OPEN	CLOSED
t_{PLZ}	CLOSED	CLOSED
t_{PZL}	CLOSED	OPEN

Figure 9. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ} and t_{PZL}.

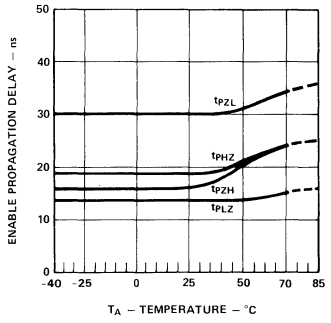
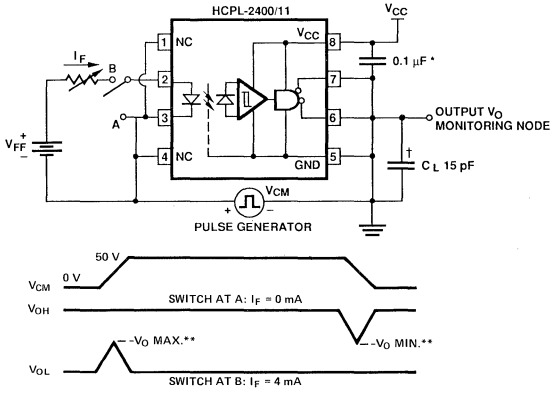


Figure 10. Typical Enable Propagation Delay vs. Ambient Temperature.



*MUST BE LOCATED < 1 cm FROM DEVICE UNDER TEST.
**SEE NOTE 6.
† C_L IS APPROXIMATELY 15 pF, WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

Figure 11. Test Diagram for Common Mode Transient Immunity and Typical Waveforms.

Applications

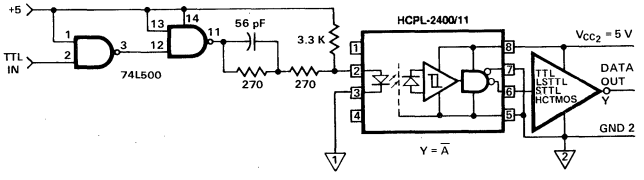


Figure 12. Recommended 20 MBd HCPL-2400/11 Interface Circuit.

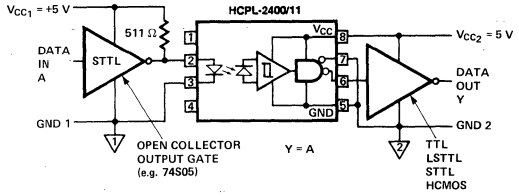


Figure 13. Alternative HCPL-2400/11 Interface Circuit.

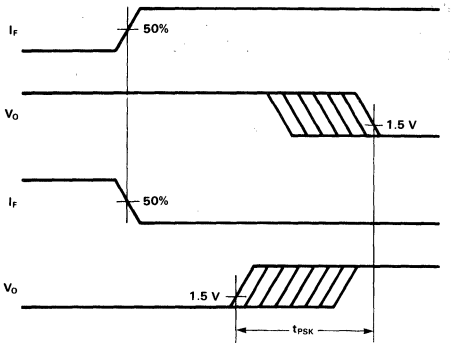


Figure 14. Illustration of Propagation Delay Skew – t_{PSK}.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 5).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 14, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 15 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 15 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might

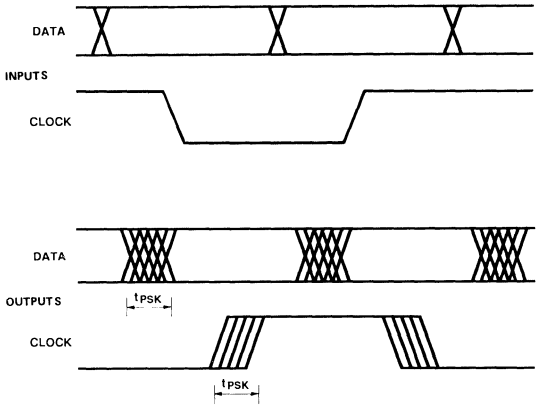


Figure 15. Parallel Data Transmission Example.

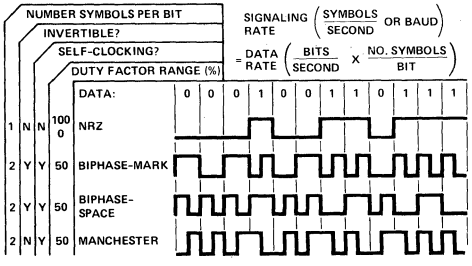


Figure 16. Modulation Code Selections.

arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The HCPL-2400/11 optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion, and propagation delay skew over the recommended temperature, input current, and power supply ranges.

Application Circuit

A recommended LED drive circuit is shown in Figure 12. This circuit utilizes several techniques to minimize the total pulse-width distortion at the output of the optocoupler. By using two inverting TTL gates connected in series, the inherent pulse-width distortion of each gate cancels the distortion of the other gate. For best results, the two series-connected gates should be from the same package.

The circuit in Figure 12 also uses techniques known as prebias and peaking to enhance the performance of the optocoupler LED. Prebias is a small forward voltage applied to the LED when the LED is off. This small prebias voltage partially charges the junction capacitance of the LED, allowing the LED to turn on more quickly. The speed of the LED is further increased by applying momentary current peaks to the LED during the turn-on and turn-off transitions of the drive current. These peak currents help to charge and discharge the capacitances of the LED more quickly, shortening the time required for the LED to turn on and off.

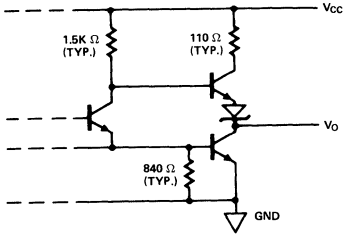


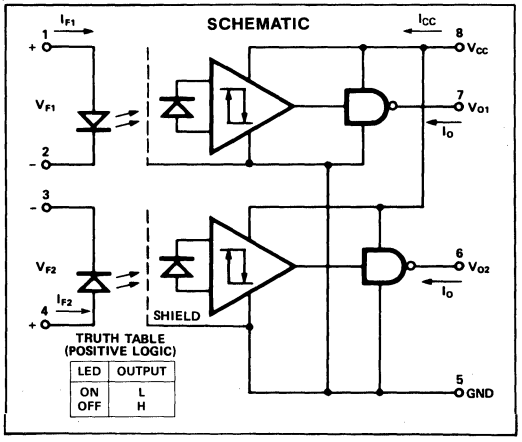
Figure 17. Typical HCPL-2400/11 Output Schematic.

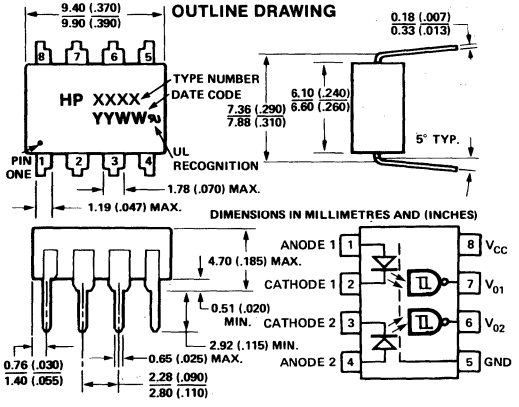
Switching performance of the HCPL-2400/11 optocouplers is not sensitive to the TTL logic family used in the recommended drive circuit. The typical and worst-case switching parameters given in the data sheet can be met using common 74LS TTL inverting gates or buffers. Use of faster TTL families will slightly reduce the overall propagation delays from the input of the drive circuit to the output of the optocoupler, but will not necessarily result in lower pulse-width distortion or propagation delay skew. This reduction in overall propagation delays is due to shorter delays in the drive circuit, not to changes in the propagation delays of the optocoupler; optocoupler propagation delays are not affected by the speed of the logic used in the drive circuit.

HEWLETT PACKARD

DUAL CHANNEL, 20 M BAUD HIGH CMR LOGIC GATE OPTOCOUPLER

HCPL-2430





Features

- CSA APPROVED
- HIGH SPEED: 40 MBd TYPICAL DATA RATE
- HIGH COMMON MODE REJECTION — 1000 V/μs GUARANTEED MINIMUM COMMON MODE TRANSIENT IMMUNITY
- AC PERFORMANCE GUARANTEED OVER TEMPERATURE
- COMPATIBLE WITH TTL, STTL, LSTTL, AND HCMOS LOGIC FAMILIES
- HIGH SPEED AlGaAs EMITTER
- TOTEM POLE OUTPUT (NO PULLUP RESISTOR REQUIRED)
- HIGH POWER SUPPLY NOISE IMMUNITY
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE
- MIL-STD-1772 VERSION AVAILABLE (HCPL-5430/1)

Applications

- ISOLATION OF HIGH SPEED LOGIC SYSTEMS
- COMPUTER-PERIPHERAL INTERFACES
- SWITCHING POWER SUPPLIES
- GROUND LOOP ELIMINATION
- HIGH SPEED DISK DRIVE I/O
- DIGITAL ISOLATION FOR A/D, D/A CONVERSION
- PULSE TRANSFORMER REPLACEMENT

Description

The HCPL-2430 high speed optocoupler combines an 820 nm AlGaAs LED with a high speed photo detector. This combination results in very high data rate capability and low input current. The totem pole output eliminates the need for a pull-up resistor.

The detectors have totem pole output stages and optical receiver input stages with built-in Schmitt triggers to provide logic compatible waveforms, eliminating the need for additional waveshaping. Improved power supply rejection minimizes the need for special power supply bypassing precautions; however, it is still recommended as good design practice.

The electrical and switching characteristics of the HCPL-2430 are guaranteed over the temperature range of 0°C to 70°C.

The HCPL-2430 is compatible with TTL, STTL, LSTTL and HCMOS logic families. A data rate performance of 20 MBd over temperature is guaranteed when using the application circuit of Figure 10. Typical data rates are 40 MBd.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.75	5.25	Volts
Input Current (High)	$I_{F(ON)}$	4	8	mA
Input Voltage (Low)	$V_{F(OFF)}$	—	0.8	Volts
Operating Temperature	T_A	0	70°	°C
Fan Out	N		5	TTL Loads

OPTO COUPLERS

Absolute Maximum Ratings (No derating required up to 70°C)

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	85	°C	
Lead Solder Temperature	260°C for 10 s. (1.6 mm below seating plane)				
Average Forward Input Current	I_F		10.0	mA	
Peak Forward Input Current	I_{FPK}		20.0	mA	10
Reverse Input Voltage	V_R		3.0	V	
Supply Voltage	V_{CC}	0	7.0	V	
Total Package Power Dissipation	P		350	mW	11
Average Output Collector Current	I_O	-25.0	25.0	mA	
Output Collector Voltage	V_O	-0.5	10.0	V	
Output Collector Power Dissipation	P_O		40.0	mW	

Electrical Specifications

For 0°C ≤ T_A ≤ 70°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, 4 mA ≤ $I_{F(ON)}$ ≤ 8 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V except where noted.
All Typicals at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 6.0 mA, $V_{F(OFF)}$ = 0 V except where noted. See note 12.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Notes
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 8.0 mA (5 TTL Loads)	1,3	1
Logic High Output Voltage	V_{OH}	2.4 2.7			Volts	I_{OH} = -4.0 mA I_{OH} = -0.4 mA	2,3	1
Output Leakage Current	I_{OHH}			100	μA	V_O = 5.25 V; V_F = 0.8 V		1
Logic Low Supply Current	I_{CCL}		34	46	mA	V_{CC} = 5.25 V, I_O = OPEN		12
Logic High Supply Current	I_{CCH}		32	42	mA			
Logic Low Short Circuit Output Current	I_{OSL}		60		mA	V_O = V_{CC} = 5.25 V; I_F = 8 mA		1,2
Logic High Short Circuit Output Current	I_{OSH}		-51		mA	V_{CC} = 5.25 V; I_F = 0 mA, V_O = GND		1,2
Input Forward Voltage	V_F	1.10 1.0	1.3	1.50 1.55	Volts	T_A = 25°C; I_F = 8 mA	4	1
Input Reverse Breakdown Voltage	BV_R	3.0 2.0	5		Volts	T_A = 25°C; I_R = 10 μA		1
Input Diode Forward Voltage Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.34		mV/°C	I_F = 6 mA	4	
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min. T_A = 25°C		3, 13
Resistance Input-Output	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 Vdc		3
Capacitance Input-Output	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 Vdc		3
Input Capacitance	C_{IN}		20		pF	f = 1 MHz, V_F = 0 V, Pins 2 and 3		
Input-Input Insulation Leakage Current	I_{I-I}		0.005		μA	Relative Humidity = 45% t = 5 s, V_{I-I} = 500 V		11
Resistance (Input-Input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500 V		11
Capacitance (Input-Input)	C_{I-I}		0.25		pF	f = 1 MHz		11

Switching Specifications

$0°C \leq T_A \leq 70°C$, $4.75\ V \leq V_{CC} \leq 5.25\ V$, $4\ mA \leq I_F \leq 8.0\ mA$. All Typicals $V_{CC} = 5\ V$, $T_A = 25°C$, $I_F = 6.0\ mA$ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		33	60	ns		5, 6, 7	1, 4
Propagation Delay Time to Logic High Output Level	t_{PLH}		30	60	ns		5, 6, 7	1, 4
Pulse Width Distortion	$\lvert t_{PHL}-t_{PLH}\rvert$		5	25	ns		5, 8	
Propagation Delay Skew	t_{PSK}			35	ns	Per notes & text	11, 12	
Output Rise Time	t_r		12		ns		5	
Output Fall Time	t_f		10		ns		5	
Logic High Common Mode Transient Immunity	$\lvert CM_H\rvert$	1000	10,000		V/μs	$T_A = 25°C$, $I_F = 0$, $V_{CM} = 50\ V$	9	7
Logic Low Common Mode Transient Immunity	$\lvert CM_L\rvert$	1000	10,000		V/μs	$T_A = 25°C$, $I_F = 4\ mA$, $V_{CM} = 50\ V$	9	7
Power Supply Noise Immunity	PSNI		0.5		V_{p-p}	$V_{CC} = 5.0\ V$, $48\ Hz \leq F_{AC} \leq 50\ MHz$		8

Notes:

1. Each channel.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
5. The typical data shown is indicative of what can be expected using the application circuit in Figure 11.
6. Propagation delay skew is discussed later in this data sheet.
7. CM_H is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic high state ($V_{O(MIN)} > 2.0\ V$). CM_L is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic low state ($V_{O(MAX)} < 0.8\ V$).
8. Power Supply Noise Immunity is the peak to peak amplitude of the ac ripple voltage on the V_{CC} line that the device will withstand and still remain in the desired logic state. For desired logic high state, $V_{OH(MIN)} > 2.0\ V$, and for desired logic low state, ($V_{OL(MAX)} < 0.8\ V$).
9. Peak Forward Input Current pulse width < 50 μs at 1 KHz maximum repetition rate.
10. Derate power dissipation above 70°C at 6.0 mW/°C.
11. Measured between pins 1 and 2, shorted together, and pins 3 and 4, shorted together.
12. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
13. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5\ \mu A$).

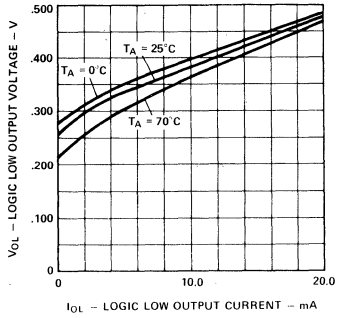


Figure 1. Typical Logic Low Output Voltage vs. Logic Low Output Current

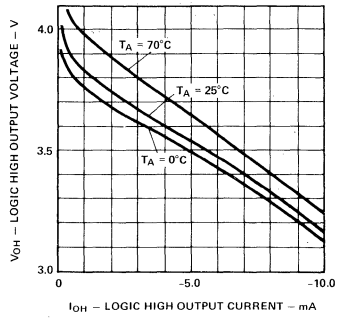


Figure 2. Typical Logic High Output Voltage vs. Logic High Output Current

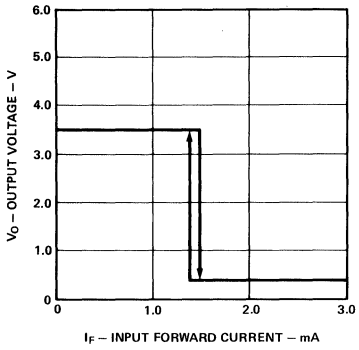


Figure 3. Typical Output Voltage vs. Input Forward Current

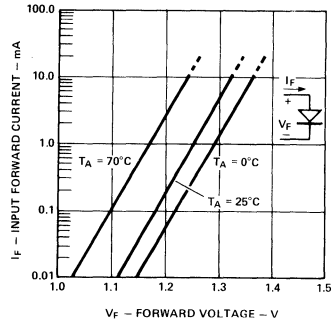


Figure 4. Typical Diode Input Forward Current Characteristic

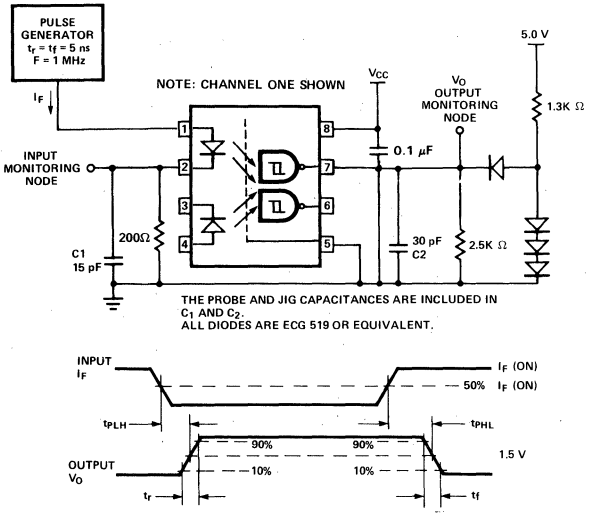


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r and t_f

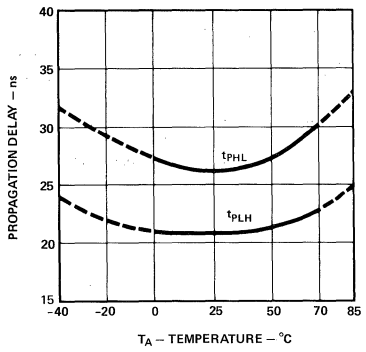


Figure 6. Typical Propagation Delay vs. Ambient Temperature

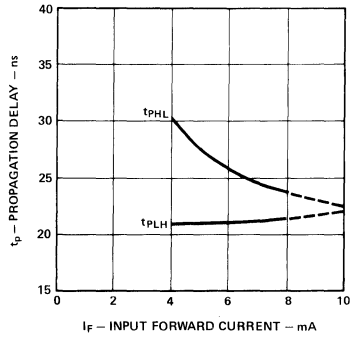


Figure 7. Typical Propagation Delay vs. Input Forward Current

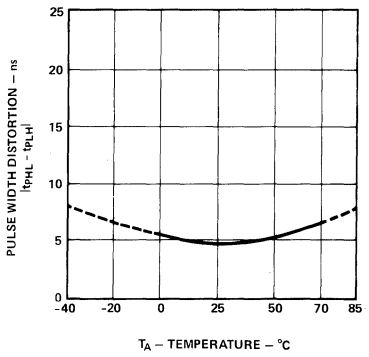
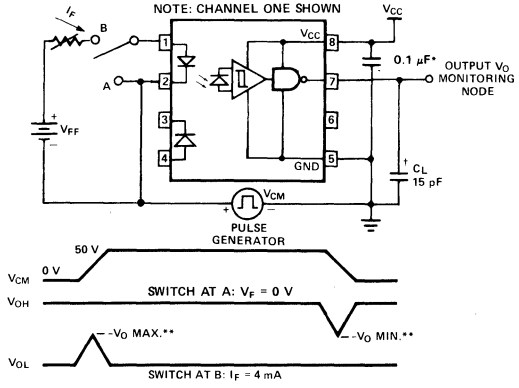


Figure 8. Typical Pulse Width Distortion vs. Ambient Temperature



*MUST BE LOCATED < 1 cm FROM DEVICE UNDER TEST.
**SEE NOTE 7.
† C_L IS APPROXIMATELY 15 pF, WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

Figure 9. Test Diagram for Common Mode Transient Immunity and Typical Waveforms

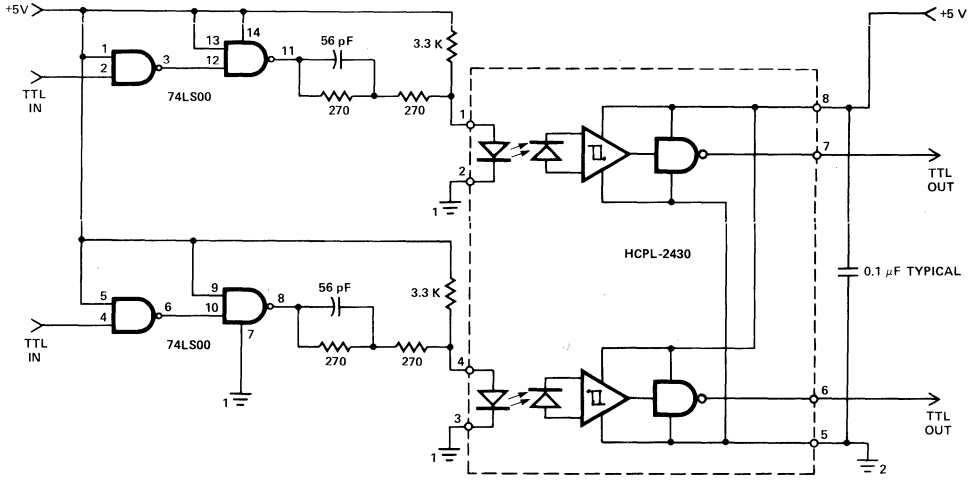


Figure 10. Recommended 20 Mbd HCPL-2430 Interface Circuit.

OPTO COUPLERS

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 5).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20–30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 11, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 12 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 12 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The HCPL-2430 optocoupler offers the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, input current, and power supply ranges.

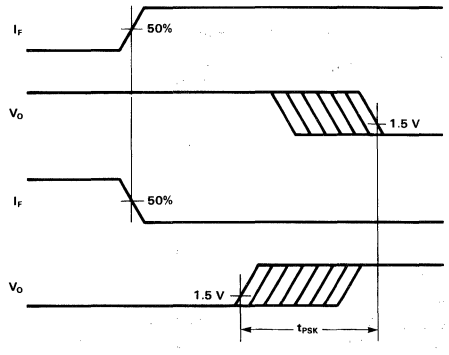


Figure 11. Illustration of Propagation Delay Skew — t_{PSK}.

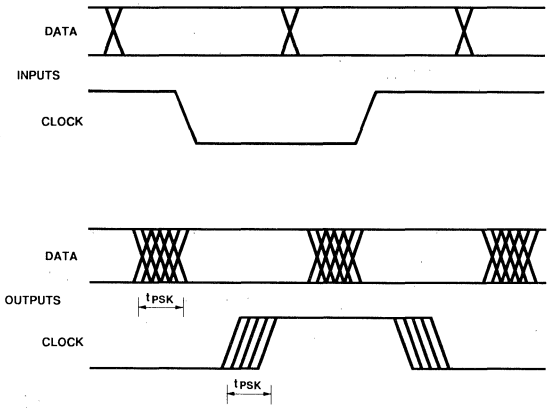


Figure 12. Parallel Data Transmission Example.

Application Circuit

A recommended LED drive circuit is shown in Figure 10. This circuit utilizes several techniques to minimize the total pulse-width distortion at the output of the optocoupler. By using two inverting TTL gates connected in series, the inherent pulse-width distortion of each gate cancels the distortion of the other gate. For best results, the two series-connected gates should be from the same package.

The circuit in Figure 10 also uses techniques known as prebias and peaking to enhance the performance of the optocoupler LED. Prebias is a small forward voltage applied to the LED when the LED is off. This small prebias voltage partially charges the junction capacitance of the LED, allowing the LED to turn on more quickly. The speed of the LED is further increased by applying momentary current peaks to the LED during the turn-on and turn-off transistions of the drive current. These peak currents help to charge and discharge the capacitances of the LED more quickly, shortening the time required for the LED to turn on and off.

Switching performance of the HCPL-2430 optocoupler is not sensitive to the TTL logic family used in the recommended drive circuit. The typical and worst-case switching parameters given in the data sheet can be met using common 74LS TTL inverting gates or buffers. Use of faster TTL families will slightly reduce the overall propagation delays from the input of the drive circuit to the output of the optocoupler, but will not necessarily result in lower pulse-width distortion or propagation delay skew. This reduction in overall propagation delays is due to shorter delays in the drive circuit, not to changes in the propagation delays of the optocoupler; optocoupler propagation delays are not affected by the speed of the logic used in the drive circuit.

HEWLETT PACKARD

High CMR, High Speed TTL Compatible Optocoupler

Technical Data

6N137
HCPL-2601
HCPL-2611

Features

- **Internal Shield for High Common Mode Rejection (CMR)**
  HCPL-2601: 10,000 V/μs at V_{CM} = 50 V (Typical)
  HCPL-2611: 15,000 V/μs at V_{CM} = 1000 V (Typical)
- **High Speed: 10 MBd Typical**
- **LSTTL/TTL Compatible**
- **Low Input Current Capability: 5 mA**
- **Guaranteed ac and dc Performance over Temperature: -40°C to +85°C**
- **Strobable Output**
- **Recognized under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 Vac, 1 Minute and 5000 Vac, 1 Minute (Option 020)**
- **CSA Approved under Component Acceptance Notice No. 5 (File No. LR 88324)**
- **Hermetic Equivalent Device Available (HCPL-5600/1)**

*JEDEC Registered Data (The HCPL-2601 and HCPL-2611 are not registered.)

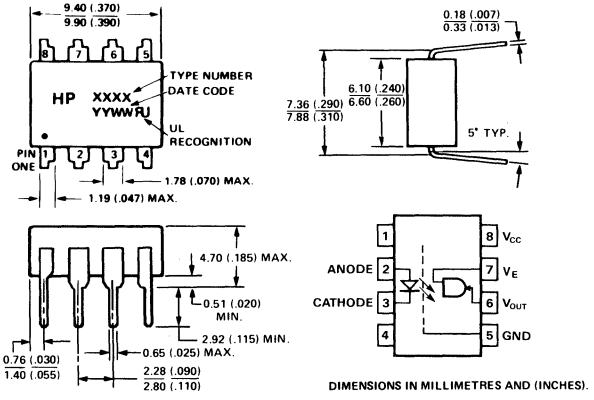
Description

The 6N137/HCPL-2601/11 optically coupled gates combine a GaAsP light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed. The output of the detector I.C. is an open collector Schottky clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 5000 V/μs for the 2601, and 10,000 V/μs for the 2611.

This unique design provides maximum ac and dc circuit isolation while achieving TTL compatibility. The optocoupler ac and dc operational parameters are guaranteed from -40°C to +85°C allowing troublefree system performance.

The 6N137/HCPL-2601/11 are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Outline Drawing*



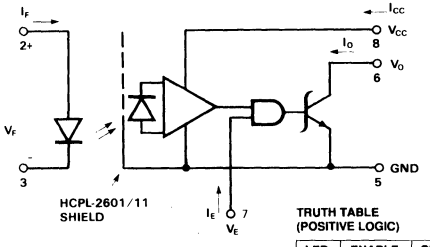
DIMENSIONS IN MILLIMETRES AND (INCHES).

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Applications

- **Isolated Line Receiver**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Switching Power Supply**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **Power Transistor Isolation in Motor Drives**

Schematic



USE OF A 0.1 μF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS REQUIRED (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	H
OFF	NC	H

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}*	0	250	μA
Input Current, High Level	I_{FH}**	5	15	mA
Supply Voltage Power	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (at R_L = 1 kΩ)	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 K	Ω
Operating Temperature	T_A	-40	85	°C

*The off condition can also be guaranteed by ensuring that $V_{FI} \leq 0.8$ volts.
**The initial switching threshold is 5 mA or less. It is recommended that 6.3 mA to 10 mA be used for best performance and to permit at least a 20% CTR degradation guardband.

Absolute Maximum Ratings*

(No Derating Required up to 85°C)
Storage Temperature ..... -55°C to +125°C
Operating Temperature** ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Forward Input Current – I_F (see Note 2) ..... 20 mA
Reverse Input Voltage ..... 5 V
Supply Voltage – V_{CC} ..... 7 V (1 Minute Maximum)
Enable Input Voltage – V_E ..... 5.5 V
(Not to exceed V_{CC} by more than 500 mV)
Output Collector Current – I_O ..... 50 mA
Output Collector Power Dissipation ..... 85 mW
Output Collector Voltage – V_O ..... 7 V
(Selection for higher output voltages up to 20 V is available.)

*JEDEC Registered Data.
**0°C to 70°C on JEDEC Registration.

Electrical Characteristics

Over recommended temperature (T_A = -40°C to +85°C) unless otherwise specified. (See note 1.)

Parameter	Sym.	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}*		5.5	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 µA, V_E = 2.0 V	1	14
Low Level Output Voltage	V_{OL}*		0.35	0.6	V	V_{CC} = 5.5 V, I_F = 5 mA, V_E = 2.0 V, I_{OL} (Sinking) = 13 mA	2, 4, 5, 15	
High Level Supply Current	I_{CCH}		7.0	10.0*	mA	V_E = 0.5 V; V_{CC} = 5.5 V, I_F = 0		15
			6.5			V_E = V_{CC}; V_{CC} = 5.5 V, I_F = 0		
Low Level Supply Current	I_{CCL}		9.0	13.0*	mA	V_E = 0.5 V; V_{CC} = 5.5 V, I_F = 10 mA		16
			8.5			V_E = V_{CC}; V_{CC} = 5.5 V, I_F = 10 mA		
High Level Enable Current	I_{EH}		-0.7	-1.6	mA	V_{CC} = 5.5 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}*		-0.9	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5 V		17
High Level Enable Voltage	V_{EH}	2.0			V			12
Low Level Enable Voltage	V_{EL}			0.8	V			
Input Forward Voltage	V_F	1.4	1.5	1.75*	V	T_A = 25°C; I_F = 10 mA	3, 14	
		1.3		1.80		I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R = 10 µA		
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz		
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 10 mA	14	
Input-Output Insulation	I_{I-O}*			1	µA	45% RH, t = 5 s, V_{I-O} = 3 kVdc, T_A = 25°C		3, 18
	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min		3, 18
OPT 020	V_{ISO}	5000						3, 19
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

*JEDEC registered data for the 6N137. The JEDEC Registration specifies 0°C to +70°C. HP specifies -40°C to +85°C.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = -40°C to +85°C), V_{CC} = 5 V, I_F = 7.5 mA unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.**	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		20	48	75*	ns	T_A = 25°C		6, 7	4
					100	ns				
Propagation Delay Time to Low Output Level	t_{PHL}		25	50	75*	ns	T_A = 25°C		6, 7	5
					100	ns				
Pulse Width Distortion	$\|t_{PHL}-t_{PLH}\|$			3.5	35	ns	R_L = 350 Ω, C_L = 15 pF		9	13
Propagation Delay Skew	t_{PSK}				40	ns				6, 13
Output Rise Time (10-90%)	t_r			24		ns			12	
Output Fall Time (90-10%)	t_f			10		ns			12	
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}			30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V		10, 11	7
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}			20		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V		10, 11	8
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	6N137		10,000		V/μs	V_{CM} = 10 V	$V_{O(MIN)}$ = 2 V, R_L = 350 Ω, I_F = 0 mA, T_A = 25°C	13	9, 11, 12
		HCPL-2601	5000	10,000			V_{CM} = 50 V			
		HCPL-2611	10,000	15,000			V_{CM} = 1000 V			
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	6N137		10,000		V/μs	V_{CM} = 10 V	$V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, I_F = 7.5 mA T_A = 25°C	13	10, 11, 12
		HCPL-2601	5000	10,000			V_{CM} = 50 V			
		HCPL-2611	10,000	15,000			V_{CM} = 1000 V			

*JEDEC registered data for the 6N137.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Notes:

1. Bypassing of the power supply line is required, with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 16. Total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the operating condition range.
7. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
8. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
9. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
10. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} < 0.8 V).
11. For sinusoidal voltages,

$$\left(\frac{|dv_{CM}|}{dt}\right)_{max} = \pi f_{CM} V_{CM}\,(p\text{-}p)$$

Notes: (Continued)

12. No external pull up is required for a high logic state on the enable input. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance.
13. See the last 2 pages of this data sheet for more information.
14. The JEDEC registration for the 6N137 specifies a maximum I_{OH} of 250 μA. HP guarantees a maximum I_{OH} of 100 μA.
15. The JEDEC registration for the 6N137 specifies a maximum I_{CCH} of 15 mA. HP guarantees a maximum I_{CCH} of 10 mA.
16. The JEDEC registration for the 6N137 specifies a maximum I_{CCL} of 18 mA. HP guarantees a maximum I_{CCL} of 13 mA.
17. The JEDEC registration for the 6N137 specifies a maximum I_{EL} of −2.0 mA. HP guarantees a maximum I_{EL} of −1.6 mA.
18. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 Vrms for one second (leakage detection current limit, $I_{I-O} \leq 5$ μA).
19. In accordance with UL 1577, each option 020 optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for one second (leakage detection current limit, $I_{i-o} \leq 5$ μA).

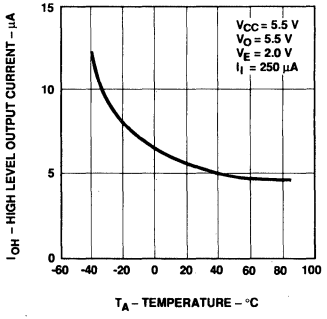


Figure 1. High Level Output Current vs. Temperature.

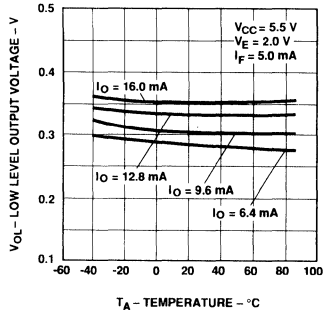


Figure 2. Low Level Output Voltage vs. Temperature.

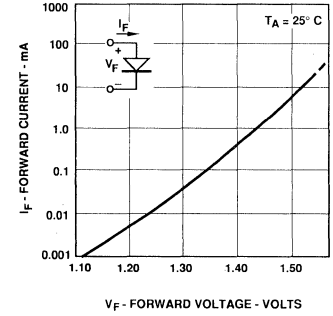


Figure 3. Input Diode Forward Characteristic.

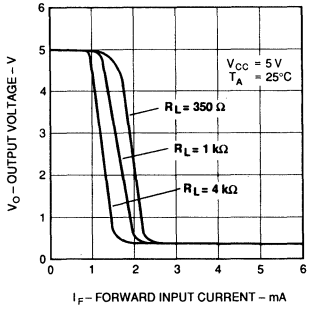


Figure 4. Output Voltage vs. Forward Input Current.

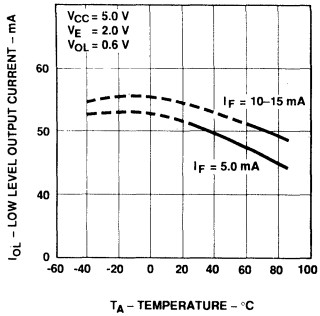


Figure 5. Low Level Output Current vs. Temperature.

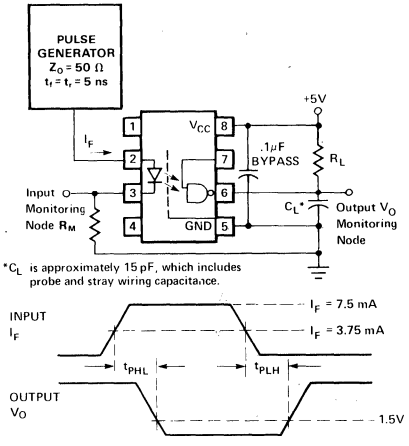


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.****

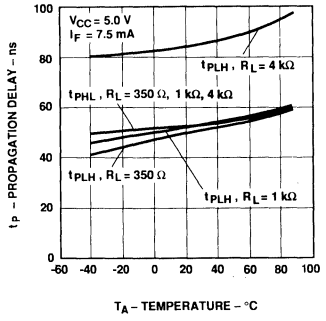


Figure 7. Propagation Delay vs. Temperature.

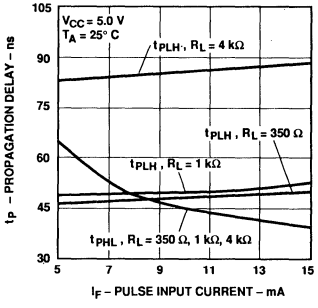


Figure 8. Propagation Delay vs. Pulse Input Current.

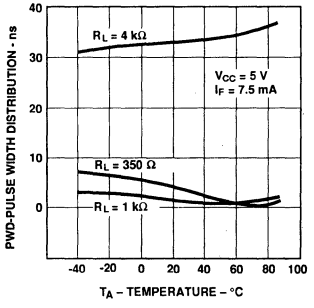


Figure 9. Pulse Width Distortion vs. Temperature.

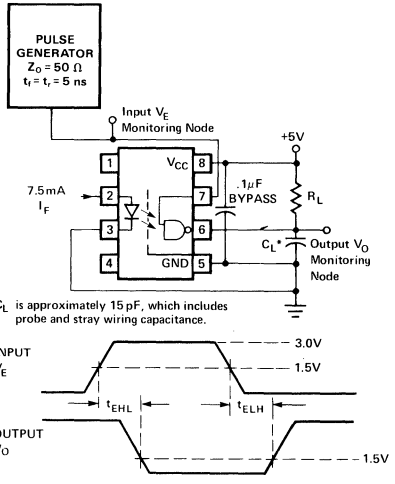


Figure 10. Test Circuit for t_{EHL} and t_{ELH}.

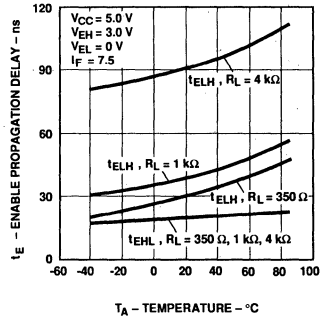


Figure 11. Enable Propagation Delay vs. Temperature.

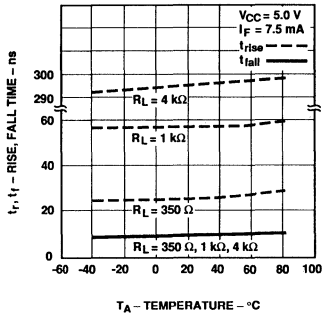


Figure 12. Rise and Fall Time vs. Temperature.

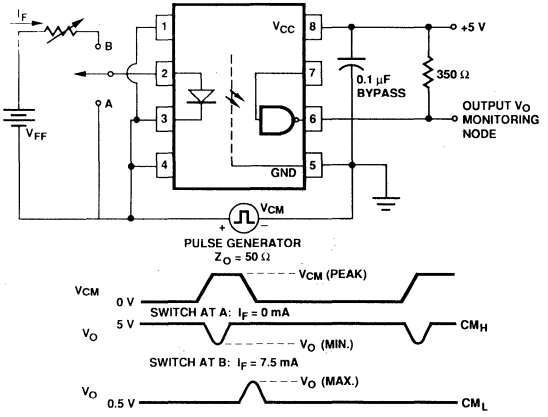


Figure 13. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

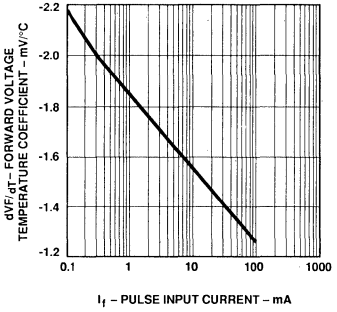


Figure 14. Temperature Coefficient for Forward Voltage vs. Input Current.

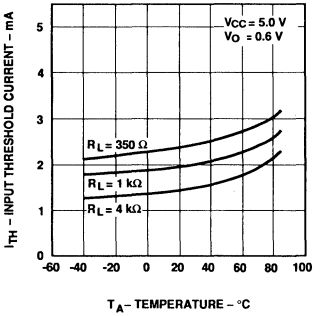


Figure 15. Input Threshold Current vs. Temperature.

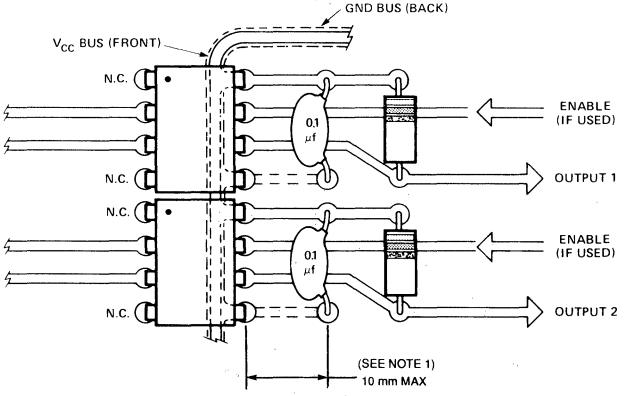


Figure 16. Recommended Printed Circuit Board Layout.

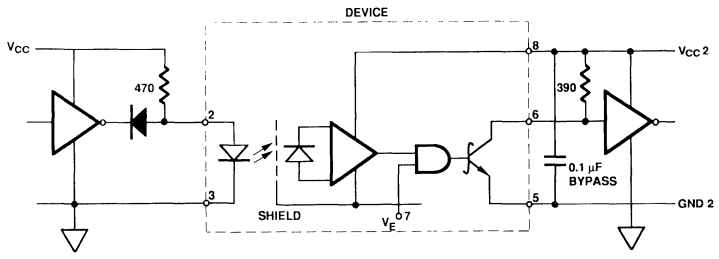


Figure 17. Recommended TTL/LSTTL to TTL/LSTTL Interface Circuit.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output causing the output to change from high to low (see Figure 6).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232. RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PLH}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 18, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 19 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 19 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{psk} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulsewidth distortion and propagation delay skew over the recommended temperature, input current, and power supply ranges.

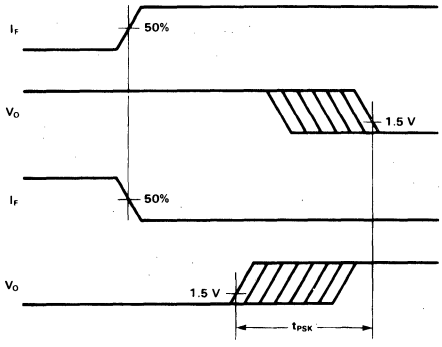


Figure 18. Illustration of Propagation Delay Skew—t_{PSK}.

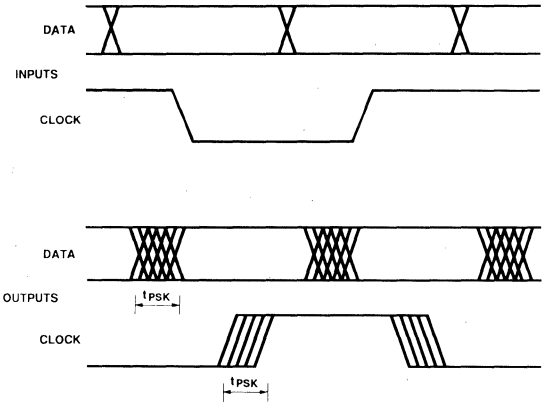


Figure 19. Parallel Data Transmission Example.

HEWLETT PACKARD

New

CMOS/TTL Compatible, Low Input Current, High Speed, High CMR Optocoupler

Technical Data

HCPL-7601
HCPL-7611

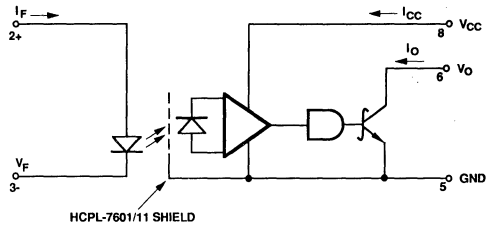
Features

- **Low Input Current Version of HCPL-2601/11 and 6N137**
- **Wide Input Current Range: I_F = 2 mA to 10 mA**
- **CMOS/TTL Compatible**
- **Guaranteed Switching Threshold: I_F = 2 mA (max.)**
- **Internal Shield for High Common Mode Rejection (CMR)**
  HCPL-7601: 5,000 V/µs (Typical) at V_{CM} = 50 V, I_F = 4 mA
  HCPL-7611: 15,000 V/µs (Typical) at V_{CM} = 1000 V, I_F = 4 mA
- **High Speed: 10 Mbd Typical**
- **Guaranteed ac and dc Performance Over Temperature: -40°C to 85°C**
- **VDE 0884 Approval: V_{IORM} = 600 V_{RMS}**
- **UL Recognized: 3750 V_{RMS}, 1 minute**
- **CSA Accepted**
- **Low Supply Current Requirement**
- **Low T_{PSK}: 40 ns Guaranteed**

Applications

- **Isolated Line Receiver**
- **Simplex/Multiplex Data Transmission**
- **Programmable Logic Controllers**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Switching Power Supply**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**

Schematic



USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS REQUIRED (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

OPTO COUPLERS

CAUTION: The small device geometries inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Description

The HCPL-7601/11 is a low input current version of the HCPL-2601/11 and 6N137 (without enable). The optically coupled gates combine an AlGaAs high-efficiency light emitting diode and an integrated high gain photon detector to create a low input current device for low power applications. The output of the detector IC is an open collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 10,000 V/μs (HCPL-7611).

This unique design provides maximum ac and dc circuit isolation while achieving CMOS and TTL compatibility. The optocoupler ac and dc operational parameters are guaranteed from -40°C to 85°C with no derating required allowing trouble free system performance. This product is suitable for high speed logic interfacing, input/output buffering, and applications that require low input-current switching levels.

The HCPL-7601/11 family offers many features that are especially beneficial to system designers. The low input current requirements and guaranteed switching threshold (2 mA max.) allows the LED to be driven directly by any standard high-speed CMOS gate (e.g. 74HC/HCT). This will simplify designs by eliminating the need for special driver circuits and result in lower part counts and greater system reliability while freeing up valuable printed circuit board space.

The wide current input range of 2 mA to 10 mA and guaranteed ac and dc performance over a wide temperature range will also simplify designs. Low supply current requirements mean lower power dissipation allowing for the use of a smaller, less expensive power supply. The high speed (10 Mbd typ.) and low propagation delay skew ($T_{psk} \leq 40$ ns guaranteed) allow for easier design of high speed parallel applications. The world-wide regulatory approval (UL/CSA/VDE 0884) will facilitate the acceptance of the end product in international markets.

Regulatory Information

The HCPL-7601 and HCPL-7611 have been approved by the following organizations:

UL–Approved under UL 1577, component recognition FILE E55361).

VDE–Approved according to VDE0884/08.87. This optocoupler is suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Can be used for safe electrical separation between ac mains and SELV (safety extra-low voltage) in equipment according to the following specifications:
DIN VDE 0804/05.89
DIN VDE 0160/05.88

Reference voltage (VDE 011b Tab 4): 630 Vac.

CSA–Approved under CSA22.2 No. 0 - General Requirements, Canadian Electrical Code, Part II; and CSA Component Acceptance Notice #5, File CA 88324.

Absolute Maximum Ratings

(No Derating Required up to 85°C)
Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Input Current - I_F (See Note 2.) ..... 20 mA
Reverse Input Voltage - V_R ..... 3 V
Supply Voltage - V_{CC} ..... 7V (1 Minute Maximum)
Output Collector Current - I_O ..... 50 mA
Output Collector Power Dissipation ..... 85 mW
Output Collector Voltage - V_O* ..... 7 V
Total Package Power Dissipation ..... 250 mW

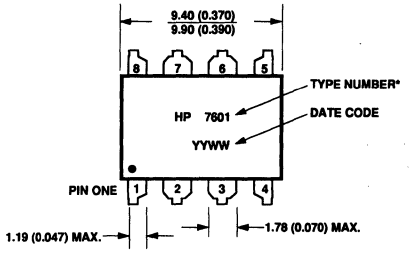
*Selection for higher output voltage up to 20 V is available.

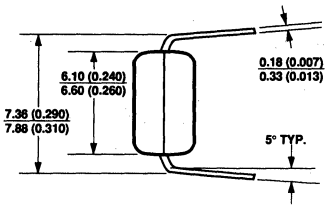
Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Voltage, Low Level	V_{FL}	0	0.8	V
Input Current, High Level	I_{FH}	2	10	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out @ R_L= 1 kΩ	N		5	TTL Loads
Operating Temperature	T_A	-40	85	°C
Output Pull-up Resistor	R_L	330	4 k	Ω

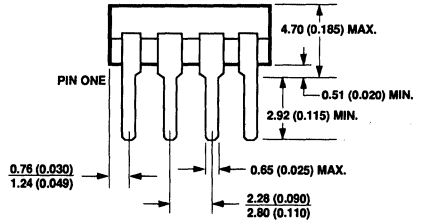
Package Outline Drawing

Standard DIP Package

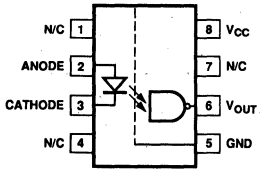




DIMENSIONS IN MILLIMETERS AND (INCHES).

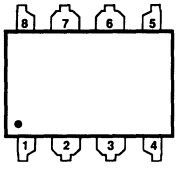


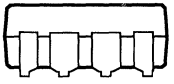
PINOUT DIAGRAM



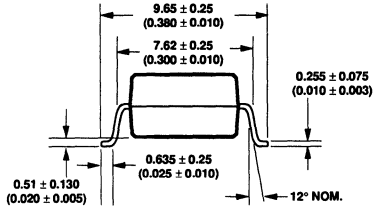
*TYPE NUMBER FOR : HCPL-7601 = 7601
HCPL-7611 = 7611

Gull Wing Surface Mount Option 300*





DIMENSIONS IDENTICAL TO
STANDARD DIP EXCEPT AS NOTED.



* REFER TO OPTION 300 DATA SHEET
FOR MORE INFORMATION.

VDE 0884 Insulation Characteristics

Description	Symbol	Characteristics	Unit
Installation classification per DIN VDE 0109*/12.83, Table 1 for rated mains voltage ≤300V_{RMS} for rated mains voltage ≤600V_{RMS}		 I-IV I-III	
Climatic Classification		40/85/21	
Pollution Degree (DIN VDE 0109/12.83)*		2	
Maximum Working Insulation Voltage	V_{IORM}	600	V_{RMS}
		848	V_{peak}
Input to Output Test Voltage, Method b** V_{PR} = 1.6 X V_{IORM} Production test with t_P = 1 sec, Partial discharge < 5 pC	V_{PR}	960	V_{RMS}
		1357	V_{peak}
Input to Output Test Voltage, Method a** V_{PR} = 1.2 X V_{IORM} Production test with t_P = 60 sec, Partial discharge < 5 pC	V_{PR}	720	V_{RMS}
		1018	V_{peak}
Highest Allowable Overvoltage** (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	6000	V_{peak}
Safety-limiting values (Maximum values allowed in the event of a failure, also see Figure 16) Case Temperature Input Power Output Power	 T_{SI} $P_{SI,Input}$ $P_{SI,Output}$	 175 80 250	 °C mW mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V	R_{IS}	$\geq 10^{11}$	Ω

* This part may also be used in Pollution Degree 3 environments where the rated mains voltage is ≤ 300 V_{RMS} (per DIN VDE 0190/12.83).
**Refer to the front of the optocoupler section of the current Optoelectronics Designers Catalog for a more detailed description of VDE 0884 and other product safety regulations.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Clearance (External Air Gap)	L (IO1)	7.0	mm	Measured from input terminals to output terminals
Minimum External Creepage (External Tracking)	L (IO2)	8.0	mm	Measured from input terminals to output terminals
Minimum Internal Clearance (Internal Plastic Gap)		0.5	mm	Through insulation distance from conductor to conductor
Comparitive Tracking Index	CTI	175	V	DIN IEC 112/VDE 303 P1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group

Electrical Specifications

Over recommended temperature (T_A = -40°C to 85°C) unless otherwise specified. (See note 1.)

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input Threshold Current	I_{TH}		1	2	mA	V_{CC} = 5.5V, $I_O \geq$ 13 mA, V_O = 0.6 V	5	
High Level Output Current	I_{OH}		3	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V V_{FL} = 0.8 V	1	
Low Level Output Voltage	V_{OL}		0.35	0.6	V	V_{CC} = 5.5 V, I_F = 2 mA, I_{OL} (Sinking) = 13 mA	2, 4, 6	
High Level Supply Current	I_{CCH}		4.75	7	mA	V_{CC} = 5.5 V, I_F = 0 mA		
Low Level Supply Current	I_{CCL}		6	10	mA	V_{CC} = 5.5 V, I_F = 4 mA		
Input Forward Voltage	V_F	1.2	1.5	1.85	V	I_F = 4 mA	3	
Input Reverse Breakdown Voltage	BV_R	3			V	I_R = 100 µA		
Input Capacitance	C_{IN}		72		pF	V_F = 0, f = 1 MHz		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$		-1.6		mV/°C	I_F = 4 mA	3	
Input-Output Insulation	V_{ISO}	3750			V_{RMS}	RH ≤ 50%, t = 1 min. T_A = 25°C		3, 9
Resistance (Input-Output)	R_{I-O}	10^{12}	10^{13}		Ω	T_A = 25°C, V_{I-O} = 500 V		3
		10^{11}				T_A = 100°C		
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 V_{dc}		3

*All typicals at T_A = 25°C, V_{CC} = 5 V.

Switching Specifications

Over recommended temperature (T_A = -40°C to 85°C), V_{CC} = 5 V, C_L = 15 pF

Parameter	Symbol	Device	Min.	Typ.*	Max	Unit	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		25	58	75		T_A = 25°C	I_F = 2 mA, R_L = 1 kΩ	7, 8, 10	4, 10
					100					
			25	55	75	ns	T_A = 25°C	I_F = 4 mA R_L = 350 Ω		
					100					
Propagation Delay Time to Low Output Level	t_{PHL}		35	73	100		T_A = 25°C	I_F = 2 mA R_L = 1 kΩ	7, 9, 10	5, 10
					120					
			25	57	75		T_A = 25°C	I_F = 4 mA R_L = 350 Ω		
					100					
Pulse Width Distortion	$\lvert t_{PHL}-t_{PLH} \rvert$			16	55		I_F = 2 mA	R_L = 1 kΩ	11, 12	4, 5
				4	40		I_F = 4 mA	R_L = 350 Ω		
Propagation Delay Skew	t_{PSK}				75		I_F = 2 mA	R_L = 1 kΩ		6, 10
					40		I_F = 4 mA	R_L = 350 Ω		
Output Rise Time (10% - 90%)	t_{rise}			58			I_F = 2 mA	R_L = 1 kΩ	13	
				24			I_F = 4 mA	R_L = 350 Ω		
Output Fall Time (10% - 90%)	t_{fall}			10			I_F = 2 - 4 mA	R_L = 350 - 1 kΩ	13	
Common Mode Transient Immunity at High Output Level	CM_H	HCPL-7601	1,000	5,000		V/µs	V_{CM} = 50 V	I_F = 0 mA $V_{o(min)}$ = 2 V R_L = 350 - 1 kΩ T_A = 25°C	14	7
		HCPL-7611	10,000	15,000			V_{CM} = 1000 V			
Common Mode Transient Immunity at Low Output Level	CM_L	HCPL-7601	1,000	5,000			I_F = 2 - 4 mA R_L = 350 - 1 kΩ V_{CM} = 50 V	$V_{o(max)}$ = 0.8V T_A = 25°C	14	8
		HCPL-7611	2,000	5,000			I_F = 2 mA R_L = 1 kΩ V_{CM} = 1000 V			
			10,000	15,000			I_F = 4 mA R_L = 350 Ω V_{CM} = 1000 V			

*All typicals at T_A = 25°C, V_{CC} = 5 V.

Notes:

1. Bypassing of the power supply line is required with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler, as illustrated in Figure 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Device considered a two terminal device: pins 1 , 2, 3 and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the operating condition range.
7. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., $V_{OUT} > 2.0$ V).
8. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., $V_{OUT} < 0.8$ V). This specification assumes that good board layout procedures were followed to reduce the effective input/output capacitance as shown in Figure 15.
9. In accordance with UL and CSA requirements, each optocoupler is proof tested by applying an insulation test voltage ≥ 5000 Vrms for one second (leakage detection current limit, $I_{I-O} \leq 5$ μA).
10. AC performance at $I_F = 4$ mA is approximately equivalent to the HCPL-2601/11 at $I_F = 7.5$ mA for comparison purposes.

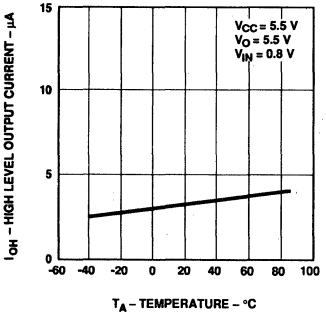


Figure 1. High Level Output Current vs. Temperature.

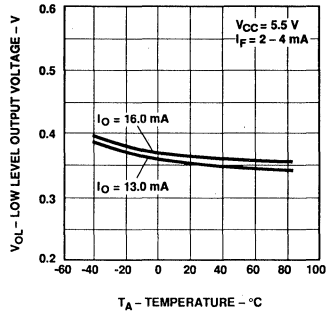


Figure 2. Low Level Output Voltage vs. Temperature.

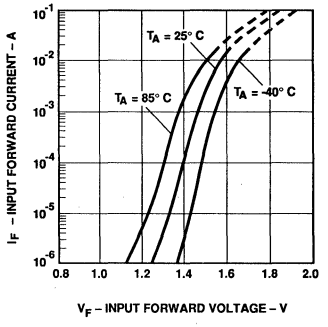


Figure 3. Typical Input Forward Current vs. Input Forward Voltage.

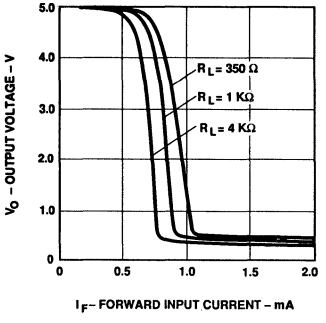


Figure 4. Output Voltage vs. Forward Input Current.

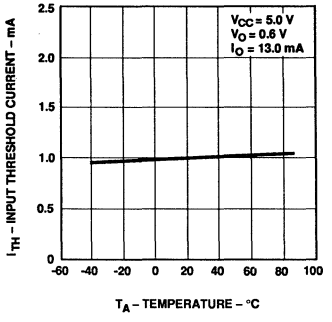


Figure 5. Input Threshold Current vs. Temperature.

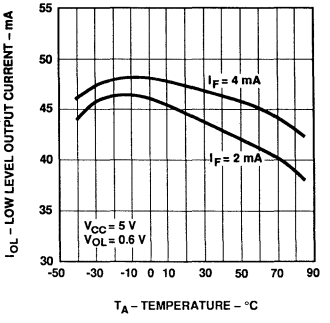


Figure 6. Low Level Output Current vs. Temperature.

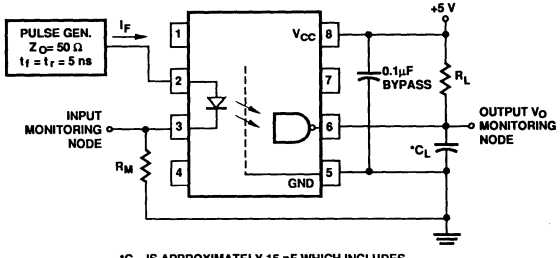


Figure 7. Test Circuit for t_{PHL} and t_{PLH}.

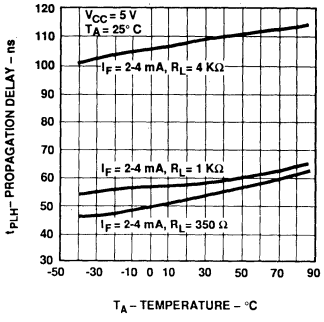


Figure 8. t_{PLH} – Propagation Delay vs. Temperature.

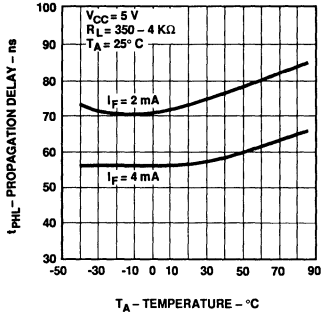


Figure 9. t_{PHL} – Propagation Delay vs. Temperature.

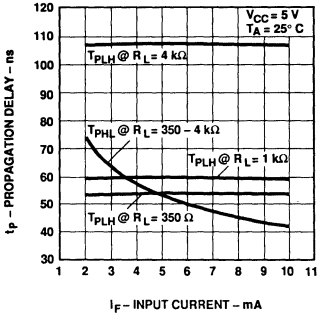


Figure 10. Propagation Delay vs. Input Current.

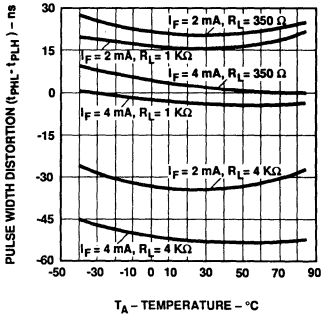


Figure 11. Pulse Width Distortion vs. Temperature.

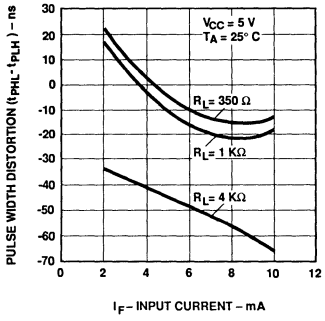


Figure 12. Pulse Width Distortion vs. Input Current.

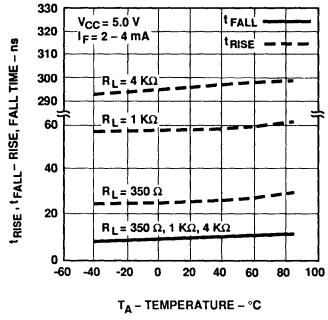


Figure 13. Rise and Fall Time vs. Temperature.

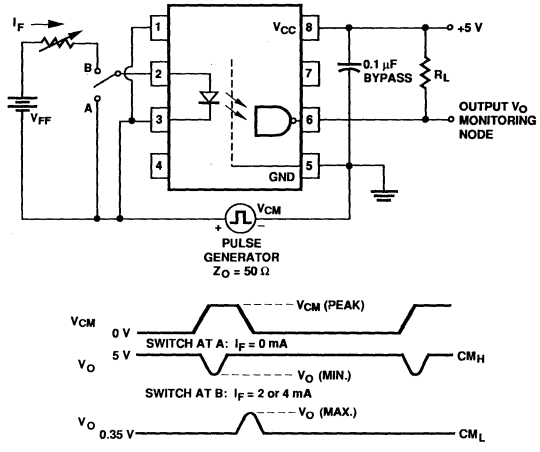


Figure 14. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

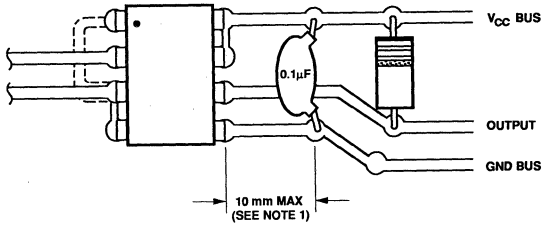


Figure 15. Recommended Printed Circuit Board Layout.

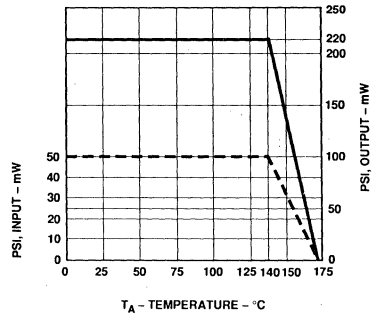
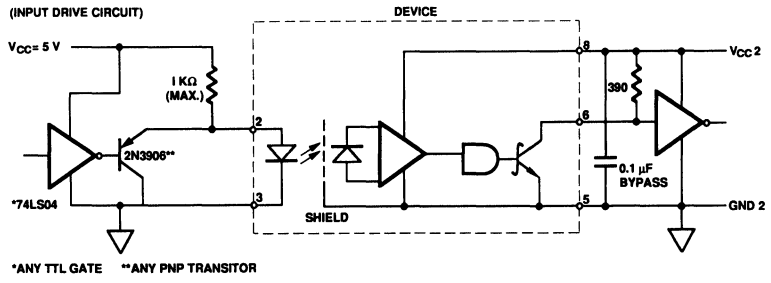
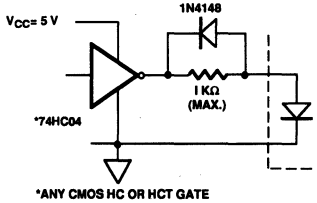


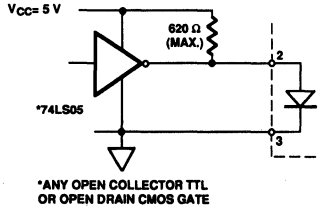
Figure 16. Dependence of Safety-Limiting Data on Ambient



CMOS OR TTL INTERFACE CIRCUIT



CMOS DRIVE CIRCUIT FOR
LOW POWER APPLICATIONS



INPUT DRIVE CIRCUIT
FOR HIGH CMR APPLICATIONS

Figure 17. Recommended Interface Circuits.

HEWLETT PACKARD

High CMR Line Receiver Optocoupler

Technical Data

HCPL-2602
HCPL-2612

Features

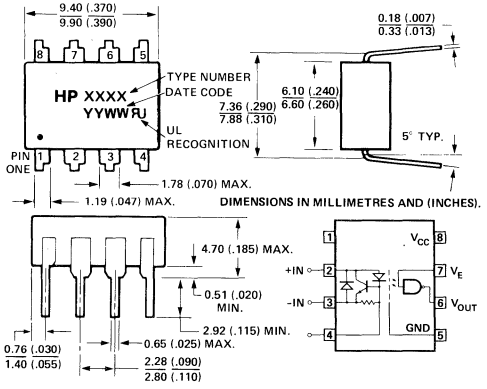
- **Internal Shield for High Common Mode Rejection (CMR)**
  HCPL-2602: 10,000 V/μs at V_{CM} = 50 V (Typical)
  HCPL-2612: 15,000 V/μs at V_{CM} = 300 V (Typical)
- **Line Termination Included – No Extra Circuitry Required**
- **Accepts a Broad Range of Drive Conditions**
- **LED Protection Minimizes LED Efficiency Degradation**
- **High Speed: 10 MBd (Limited by Transmission Line in Many Applications)**
- **Guaranteed ac and dc Performance Over Temperature: 0°C to 70°C**
- **External Base Lead Allows "LED Peaking" and LED Current Adjustment**
- **Recognized Under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 VAC.**
- **CSA Approved under Component Acceptance Notice No. 5 (File No. LR 88324)**
- **Hermetic Equivalent Device Available (HCPL-1930/1)**

Description

The HCPL-2602/12 optically coupled line receivers combine a GaAsP light emitting diode, an input current regulator and an integrated high gain photo detector. The input regulator serves as a line termination for line receiver applications. It clamps the line voltage and regulates the LED current so line reflections do not interfere with circuit performance.

The regulator allows a typical LED current of 8.5 mA before it starts to shunt excess current. The output of the detector IC is an open collector Schottky clamped transistor. An enable input gates the detector. The internal detector shield provides a guaranteed common mode transient immunity specification of 1000 V/μs for the 2602, and 3500 V/μs for the 2612.

Outline Drawing



CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

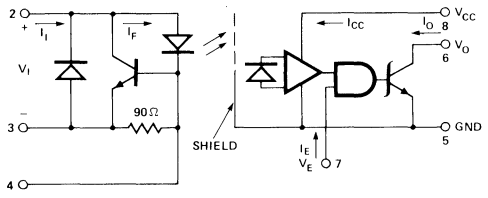
DC specifications are defined similar to TTL logic. The optocoupler ac and dc operational parameters are guaranteed from 0°C to 70°C allowing trouble-free interfacing with digital logic circuits. An input current of 5 mA will sink an eight gate fan-out (TTL) at the output.

The HCPL-2602/12 are useful as line receivers in high noise environments that conventional line receivers cannot tolerate. The higher LED threshold voltage provides improved immunity to differential noise and the internally shielded detector provides orders of magnitude improvement in common mode rejection with little or no sacrifice in speed.

Applications

- **Isolated Line Receiver**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Current Sensing**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **Power Transistor Isolation in Motor Drives**

Schematic



USE OF A 0.1 μF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS REQUIRED (SEE NOTE 1).

TRUTH TABLE (POSTIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	H
OFF	NC	H

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_L	0	250	μA
Input Current, High Level	I_{IH}	5*	60	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (@ R_L = 1 kΩ)	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 K	Ω
Operating Temperature	T_A	0	70	°C

*The initial switching threshold is 5 mA or less. It is recommended that an input current between 6.3 mA and 10 mA be used to obtain best performance and to provide at least 20% LED degradation guardband.

Absolute Maximum Ratings

(No derating required up to 85°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to 85°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Forward Input Current – I_I ..... 60 mA
Reverse Input Current ..... 60 mA
Supply Voltage – V_{CC} (1 Minute Maximum) ..... 7 V
Enable Input Voltage – V_E ..... 5.5 V
(Not to exceed V_{CC} by more than 500 mV)
Output Collector Current – I_O ..... 25 mA
Output Collector Power Dissipation ..... 40 mW
Output Collector Voltage – V_O** ..... 7 V
Input Current, Pin 4 ..... ±10 mA

**Selection for higher output voltages up to 20 V is available.

Electrical Characteristics

Over recommended temperature (T_A = 0°C to +70°C) unless otherwise specified. See note 1.

Parameter	Sym.	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}		5.5	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_I = 250 µA, V_E = 2.0 V	1	
Low Level Output Voltage	V_{OL}		0.35	0.6	V	V_{CC} = 5.5 V, I_I = 5 mA, V_E = 2.0 V, I_{OL} (Sinking) = 13 mA	2, 4, 5, 14	
High Level Supply Current	I_{CCH}		7.5	10	mA	V_{CC} = 5.5 V, I_I = 0 mA, V_E = 0.5 V		
Low Level Supply Current	I_{CCL}		10	13	mA	V_{CC} = 5.5 V, I_I = 60 mA, V_E = 0.5 V		
High Level Enable Current	I_{EH}		-0.7	-1.6	mA	V_{CC} = 5.5 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}		-0.9	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5 V		
High Level Enable Voltage	V_{EH}	2.0			V			11
Low Level Enable Voltage	V_{EL}			0.8	V			
Input Voltage	V_I		2.0	2.4	V	I_I = 5 mA	3	
			2.3	2.7		I_I = 60 mA		
Input Reverse Voltage	V_R		0.75	0.95	V	I_R = 5 mA		
Input Capacitance	C_{IN}		90		pF	V_I = 0, f = 1 MHz		
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min T_A = 25°C		2, 11
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		2
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		2

*All typicals at V_{CC} = 5 V, T_A = 25°C.

Notes:

1. Bypassing of the power supply line is required, with a 0.1 µf ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.
2. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
3. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
4. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
5. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.

Switching Specifications

Over recommended temperature (T_A = 0°C to +70°C), V_{CC} = 5 V, I_I = 7.5 mA, unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		20	48	75	ns	T_A = 25°C		6, 7, 8	3
					100	ns				
Propagation Delay Time to Low Output Level	t_{PHL}		25	50	75	ns	T_A = 25°C		6, 7, 8	4
					100	ns				
Pulse Width Distortion	$\lvert t_{PHL}-t_{PLH} \rvert$			3.5	35	ns	R_L = 350 Ω, C_L = 15 pF		9	13
Propagation Delay Skew	t_{PSK}				40	ns				12, 13
Output Rise Time (10-90%)	t_r			24		ns			12	
Output Fall Time (90-10%)	t_f			10		ns			12	
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}			30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V		10, 11	5
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}			20		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V		10, 11	6
Common Mode Transient Immunity at High Output Level	$\lvert CM_H \rvert$	HCPL-2602	1000	10,000		V/μs	V_{CM} = 50 V	$V_{O(MIN)}$ = 2 V, R_L = 350 Ω, I_F = 0 mA, T_A = 25°C	13	7, 9, 10
		HCPL-2612	3500	15,000			V_{CM} = 300 V			
Common Mode Transient Immunity at Low Output Level	$\lvert CM_L \rvert$	HCPL-2602	1000	10,000		V/μs	V_{CM} = 50 V	$V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, I_F = 7.5 mA, T_A = 25°C	13	8, 9 10
		HCPL-2612	3500	15,000			V_{CM} = 300 V			

*All typicals at V_{CC} = 5 V, T_A = 25°C.

7. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
8. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} < 0.8 V).
9. For sinusoidal voltages,
$$\left|\frac{dv_{CM}}{dt}\right|_{max} = \pi f_{CM} V_{CM} \text{ (p-p)}$$
10. No external pull up is required for a high logic state on the enable input. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance.
11. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage of ≥ 3000 for one second (leakage detection current limit, I_{i-o} ≤ 5 μA).
12. t_{PSK} is qual to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the operating condition range.
13. See the last 2 pages of this data sheet for more information.

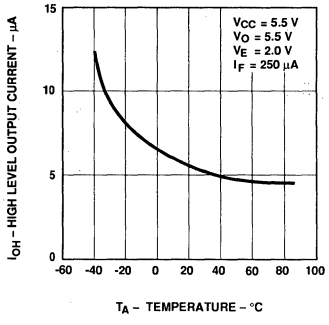


Figure 1. High Level Output Current vs. Temperature.

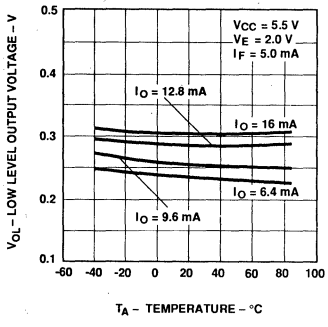


Figure 2. Low Level Output Voltage vs. Temperature.

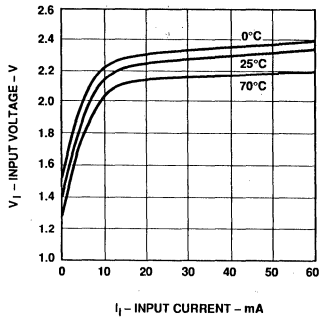


Figure 3. Input Characteristics.

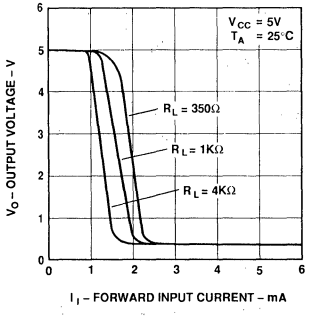


Figure 4. Output Voltage vs. Forward Input Current.

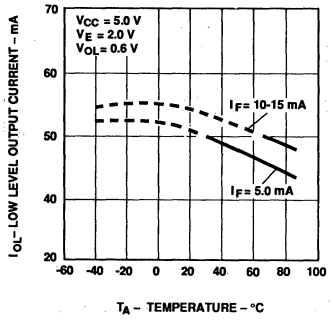


Figure 5. Low Level Output Current vs. Temperature.

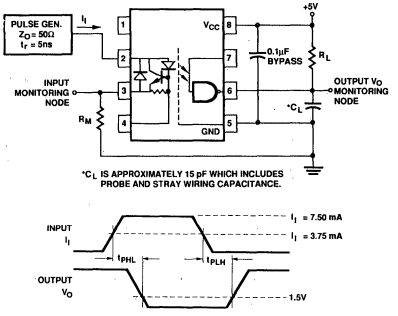


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

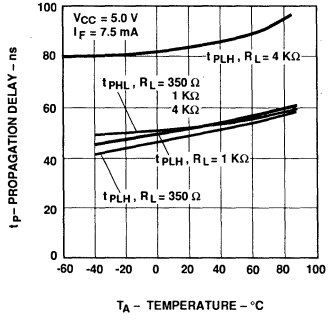


Figure 7. Propagation Delay vs. Temperature.

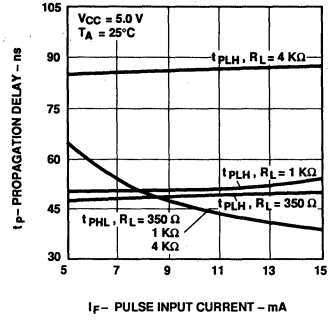


Figure 8. Propagation Delay vs. Pulse Input Current.

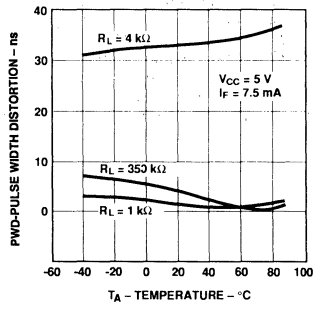


Figure 9. Pulse Width Distortion vs. Temperature.

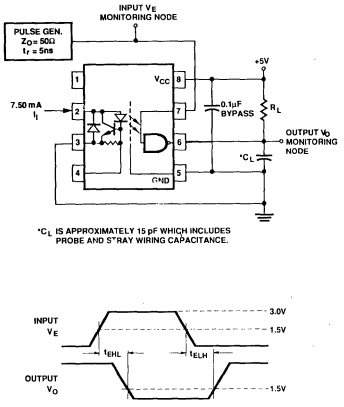


Figure 10. Test Circuit for t_{EHL} and t_{ELH}.

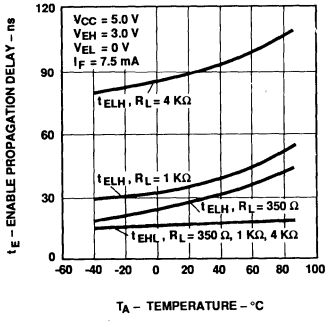


Figure 11. Enable Propagation Delay vs. Temperature.

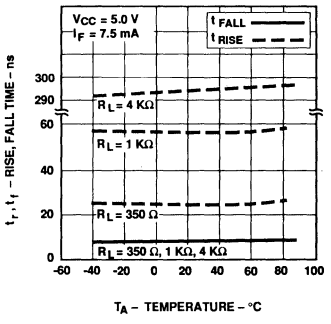


Figure 12. Rise and Fall Time vs. Temperature.

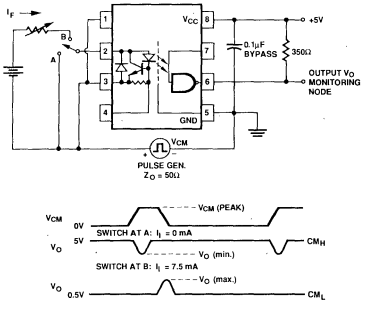


Figure 13. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

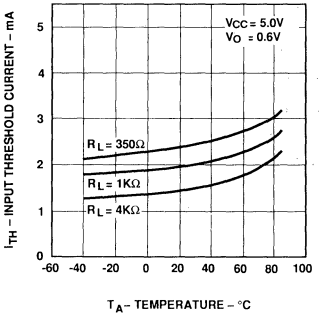


Figure 14. Input Threshold Current vs. Temperature.

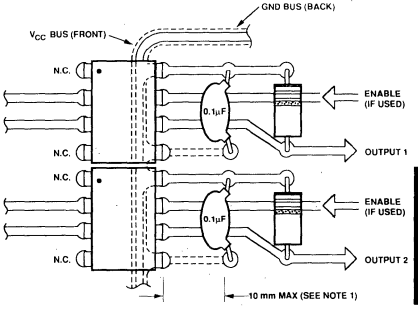


Figure 15. Recommended Printed Circuit Board Layout.

Using the HCPL-2602/12 Line Receiver Optocouplers

The primary objectives to fulfill when connecting an optocoupler to a transmission line are to provide a minimum, but not excessive, LED current and to properly terminate the line. The internal regulator in the HCPL-2602/12 simplifies this task. Excess current from variable drive conditions such as line length variations, line driver differences and power supply fluctuations are shunted by the regulator. In fact, with the LED current regulated, the line current can be increased to improve the immunity of the system to differential-mode-noise and to enhance the data rate capability. The designer must keep in mind the 60 mA input current maximum rating of the HCPL-2602/12 in such cases, and may need to use series limiting or shunting to prevent overstress.

Design of the termination circuit is also simplified; in most cases the transmission line can simply be connected directly to the input terminals of the HCPL-2602/12 without the need for additional series or shunt resistors. If reversing line drive is used it may be desirable to use two HCPL-2602/12 or an external Schottky diode to optimize data rate.

Polarity Non-Reversing Drive

High data rates can be obtained with the HCPL-2602/12 with polarity non-reversing drive. Figure (a) illustrates how a 74S140 line driver can be used with the HCPL-2602/12 and shielded, twisted pair or coax cable without any additional components. There are some reflections due to the "active termination" but they do not interfere with circuit performance because the regulator clamps the line voltage. At longer line lengths t_{PLH} increases faster than t_{PHL} since the switching threshold is not exactly halfway between asymptotic line conditions. If optimum data rate is desired, a series resistor and peaking capacitor can be used to equalize t_{PLH} and t_{PHL}. In general, the peaking capacitance should be as large as possible; however, if it is too large it may keep the regulator from achieving turn-off during the negative (or zero) excursions of the input signal. A safe rule:

make $C \leq 16t$

where:
C = peaking capacitance in picofarads
t = data bit interval in nanoseconds

Polarity Reversing Drive

A single HCPL-2602/12 can also be used with polarity reversing drive (Figure b). Current reversal is obtained by way of the substrate isolation diode (substrate to collector). Some reduction of data rate occurs, however, because the substrate diode stores charge, which must be removed when the current changes to the forward direction. The effect of this is a longer t_{PHL}. This effect can be eliminated and data rate improved considerably by use of a Schottky diode on the input of the HCPL-2602/12.

For optimum noise rejection as well as balanced delays a split-phase termination should be used along with a flip-flop at the output (Figure c). The result of current reversal in split-phase operation is seen in Figure (c) with switches A and B both OPEN. The coupler inputs are then connected in ANTI-SERIES; however, because of the higher steady-state termination voltage, in comparison to the single HCPL-2602/12 termination, the forward current in the substrate diode is lower and consequently there is less junction charge to deal with when switching.

Closing switch B with A open is done mainly to enhance common mode rejection, but also reduces propagation delay slightly because line-to-line capacitance offers a slight peaking effect. With switches A and B both CLOSED, the shield acts as a current return path which prevents either input substrate diode from becoming reversed biased. Thus the data rate is optimized as shown in Figure (c).

Improved Noise Rejection

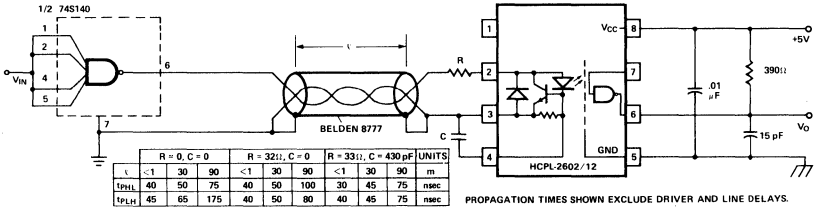
Use of additional logic at the output of two HCPL-2602/12s, operated in the split phase termination, will greatly improve system noise rejection in addition to balancing propagation delays as discussed earlier.

A NAND flip-flop offers infinite common mode rejection (CMR) for NEGATIVELY sloped common mode transients but requires $t_{PHL} > t_{PLH}$ for proper operation. A NOR flip-flop has infinite CMR for POSITIVELY sloped transients but requires $t_{PHL} < t_{PLH}$ for proper operation. An exclusive-OR flip-flop has infinite CMR for common mode transients of EITHER polarity and operates with either $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$.

With the line driver and transmission line shown in Figure (c), $t_{PHL} > t_{PLH}$, so NAND gates are preferred in the R-S flip-flop. A higher drive amplitude or different circuit configuration could make $t_{PHL} < t_{PLH}$, in which case NOR gates would be preferred. If it is not known whether $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$, or if the drive conditions may vary over the boundary for these conditions, the exclusive-OR flip-flop of Figure (d) should be used.

RS-422 and RS-423

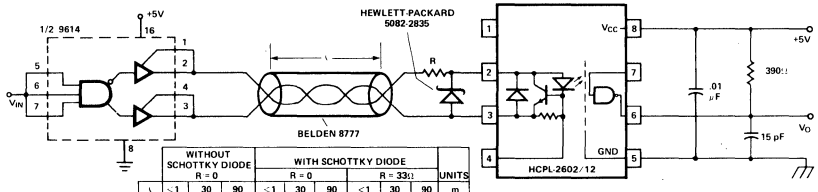
Line drivers designed for RS-422 and RS-423 generally provide adequate voltage and current for operating the HCPL-2602/12. Most drivers also have characteristics allowing the HCPL-2602/12 to be connected directly to the driver terminals. Worst case drive conditions, however, would require current shunting to prevent overstress of the HCPL-2602/12.



	R = 0, C = 0			R = 32Ω, C = 0			R = 33Ω, C = 430 pF			UNITS
ℓ	<1	30	90	<1	30	90	<1	30	90	m
t_{PHL}	40	50	75	40	50	100	30	45	75	nsec
t_{PLH}	45	65	175	40	50	80	40	45	75	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

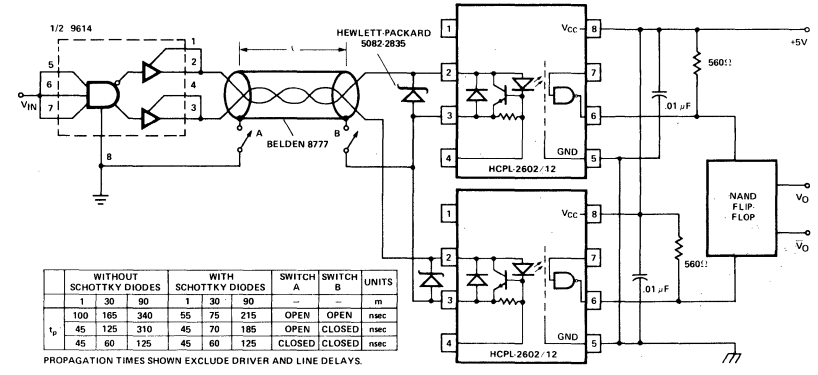
Figure a. Polarity Non-Reversing.



	WITHOUT SCHOTTKY DIODE R = 0			WITH SCHOTTKY DIODE R = 0			WITH SCHOTTKY DIODE R = 33Ω			UNITS
ℓ	<1	30	90	<1	30	90	<1	30	90	m
t_{PHL}	210	365	450	50	80	235	50	70	200	nsec
t_{PLH}	35	45	60	35	45	60	35	45	60	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

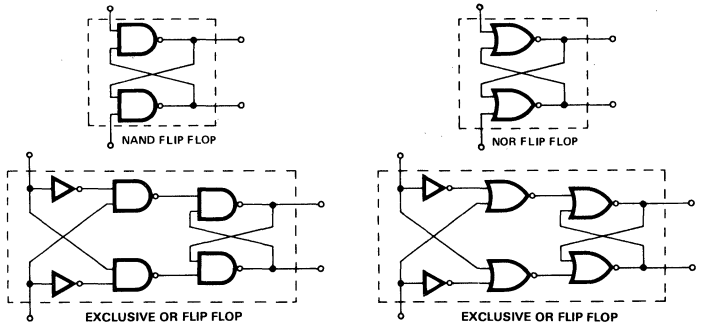
Figure b. Polarity Reversing, Single Ended.



	WITHOUT SCHOTTKY DIODES			WITH SCHOTTKY DIODES			SWITCH A	SWITCH B	UNITS
	1	30	90	1	30	90	—	—	m
t_p	100	165	340	55	75	215	OPEN	OPEN	nsec
	45	125	310	45	70	185	OPEN	CLOSED	nsec
	45	60	125	45	60	125	CLOSED	CLOSED	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

Figure c. Polarity Reversing, Split Phase.



NAND flip flop tolerates simultaneously HIGH inputs; NOR flip flop tolerates simultaneously LOW inputs; EXCLUSIVE-OR flip flop tolerates simultaneously HIGH OR LOW inputs without causing either of the outputs to change.

Figure d. Flip-Flop Configurations.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 6).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 16, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PHL} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 17 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 17 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, input current, and power supply ranges.

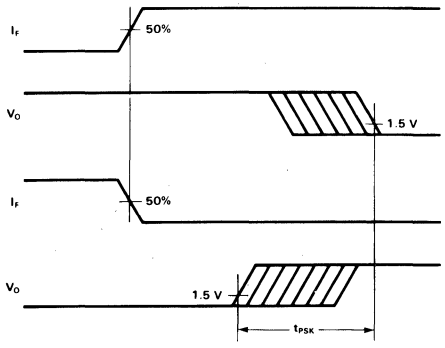


Figure 16. Illustration of Propagation Delay Skew - t_{PSK}.

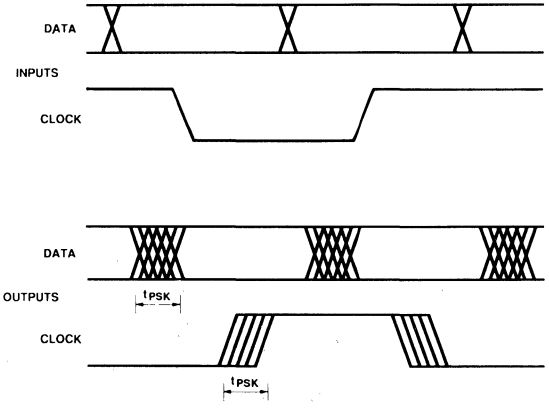


Figure 17. Parallel Data Transmission Example.

HEWLETT PACKARD

Dual Channel High CMR High Speed TTL Compatible Optocoupler

Technical Data

HCPL-2630
HCPL-2631
HCPL-4661

Features

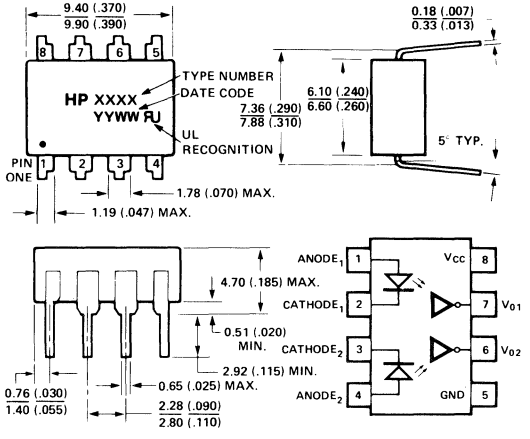
- **Internal Shield for High Common Mode Rejection (CMR)**
  HCPL-2631: 10,000 V/μs @ V_{CM} = 50 V (Typical)
  HCPL-4661: 15,000 V/μs @ V_{CM} = 1000 V (Typical)
- **High Density Packaging**
- **Low Input Current Capability: 5 mA**
- **High Speed: 10 MBd Typical**
- **LSTTL and TTL Compatible**
- **Guaranteed AC and DC Performance Over Temperature: -40°C to 85°C**
- **Recognized Under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 VAC, 1 Minute and 5000 VAC, 1 Minute (Option 020) Pending Approval.**
- **CSA Approved under Component Acceptance Notice No. 5 (File No. LR 88324)**
- **Hermetic Equivalent Device Available (HCPL-5630/31)**

Description

The HCPL-2630/HCPL-2631/4661 are dual channel optically coupled logic gates that combine GaAsP light emitting diodes and integrated high gain photodetectors. The photons are collected in the detector by a photodiode and the current is amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. Each circuit is temperature, current and voltage compensated. The internal shield provides a guaranteed common mode transient immunity specification of 5000 V/μs for the 2631, and 10,000 V/μs for the HCPL-4661.

The unique design provides maximum AC and DC circuit isolation while achieving LSTTL and TTL compatibility. The optocoupler AC and DC operational parameters are guaranteed from -40°C to +85°C. The dual channel design minimizes space and results in increased convenience.

Outline Drawing



DIMENSIONS IN MILLIMETRES AND (INCHES).

The HCPL-2630/2631/4661 are recommended for high speed logic interfacing, input/output buffering, and for use as line receivers in environments that conventional line receivers cannot tolerate. The HCPL-2630/2631/4661 can be used for the digital programming of machine control systems, motors and floating power supplies. The internal shield makes the HCPL-2631/4661 ideal for use in extremely high ground or induced noise environments.

Applications

- **Isolation of High Speed Logic Systems**
- **Microprocessor System Interfaces**
- **Isolated Line Receiver**
- **Computer-Peripheral Interfaces**
- **Ground Loop Elimination**
- **Digital Isolation for A/D, D/A Conversion**
- **Power Transistor Isolation in Motor Drives**

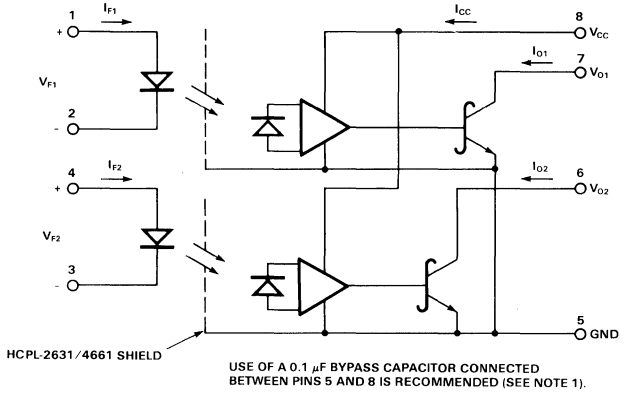


Figure 1. Schematic.

Recommended Operation Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}*	5	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (@ R_L = 1 kΩ) Each Channel	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 K	Ω
Operating Temperature	T_A	-40	85	°C

*The initial switching threshold is 5 mA or less. It is recommended that input current between 6.3 mA and 10 mA be used to obtain best performance and to provide at least a 20% LED degradation guardband.

Absolute Maximum Ratings

(No Derating Required up to 85°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Forward
Input Current (each channel, See note 2) ..... 15 mA
Reverse Input Voltage (each channel) ..... 5 V
Supply Voltage – V_{CC} (1 Minute Maximum) ..... 7 V
Output Collector Current – I_O (each channel) ..... 16 mA
Output Collector Voltage – V_O (each channel)** ..... 7 V
Output Collector Power Dissipation (each channel) ..... 60 mW

**Selection for higher output voltages up to 20 V is available.

Electrical Characteristics

Over recommended temperature (T_A = -40°C to +85°C) unless otherwise specified. (See note 1.)

Parameter	Sym.	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}		5.5	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 µA	2	3
Low Level Output Voltage	V_{OL}		0.35	0.6	V	V_{CC} = 5.5 V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	3, 5, 6, 15	3
High Level Supply Current	I_{CCH}		10	15	mA	V_{CC} = 5.5 V, I_F = 0 mA (Both Channels)		
Low Level Supply Current	I_{CCL}		13	21	mA	V_{CC} = 5.5 V, I_F = 10 mA (Both Channels)		
Input Forward Voltage	V_F	1.4	1.5	1.75	V	T_A = 25°C, I_F = 10 mA	4	3
		1.3		1.80				
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA,		3
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz		3
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 10 mA	13	
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 Min T_A = 25°C		12
Opt. 020 (Pending)	V_{ISO}	5000						15
Input-Input Leakage Current	I_{I-I}		0.005		µA	Relative Humidity = 45% t = 5 s, V_{I-I} = 500 V		5
Resistance (Input-Input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500 V		5
Capacitance (Input-Input)	C_{I-I}		0.25		pF	f = 1 MHz		
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		4
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = -40°C to +85°C), V_{CC} = 5 V, I_F = 7.5 mA, unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		20	48	75	ns	T_A = 25°C		8, 9	3, 6
					100	ns				
Propagation Delay Time to Low Output Level	t_{PHL}		25	50	75	ns	T_A = 25°C		8, 9	3, 7
					100	ns				
Pulse Width Distortion	$\|t_{PHL}-t_{PLH}\|$			3.5	35	ns	R_L = 350 Ω, C_L = 15 pF		10	13
Propagation Delay Skew	t_{PSK}				40	ns				13,14
Output Rise Time (10-90%)	t_r			24		ns			11	3
Output Fall Time (90-10%)	t_f			10		ns			11	3
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	HCPL-2630		10,000		V/μs	V_{CM} = 10 V	$V_{O(MIN)}$ = 2 V, R_L = 350 Ω, I_F = 0 mA, T_A = 25°C	12	3, 8, 10
		HCPL-2631	5,000	10,000			V_{CM} = 50 V			
		HCPL-4661	10,000	15,000			V_{CM} = 1000 V			
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	HCPL-2630		10,000		V/μs	V_{CM} = 10 V	$V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, I_F = 7.5 mA T_A = 25°C	12	3, 9, 10
		HCPL-2631	5,000	10,000			V_{CM} = 50 V			
		HCPL-4661	10,000	15,000			V_{CM} = 1000 V			

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Notes:

1. Bypassing of the power supply line is required, with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 15 mA.
3. Each channel.
4. Measured between pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
5. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
6. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
7. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
8. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
9. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} > 0.8 V).
10. For sinusoidal voltages,

$$\left(\frac{|dv_{CM}|}{dt}\right)_{max} = \pi f_{CM} V_{CM} \text{ (p-p)}$$

11. As illustrated in Figure 15 the V_{CC} and GND traces can be located between the input and the output leads of the HCPL-2630/2631/4661 to provide additional noise immunity at the compromise of insulation capability.
12. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 Vrms for one second (leakage detection current limit, $I_{i-o} \leq 5$ μA).
13. See the last 2 pages of this data sheet for more information.
14. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the operating condition range.
15. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for one second (leakage detection current limit, $I_{i-o} \leq 5$ μA).

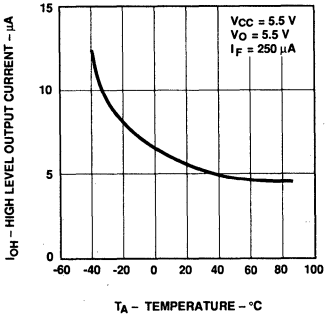


Figure 2. High Level Output Current vs. Temperature.

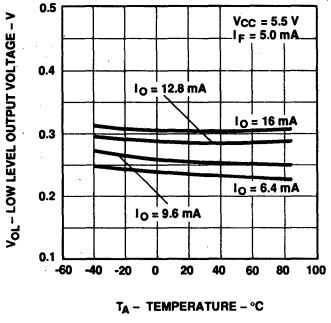


Figure 3. Low Level Output Voltage vs. Temperature.

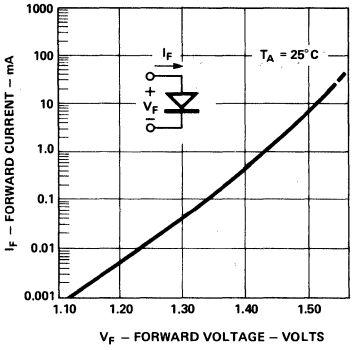


Figure 4. Input Diode Forward Characteristic.

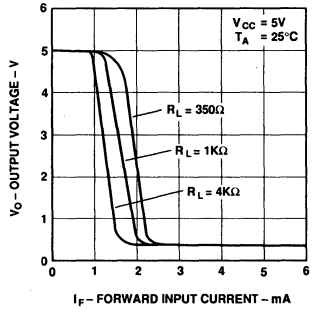


Figure 5. Output Voltage vs. Forward Input Current.

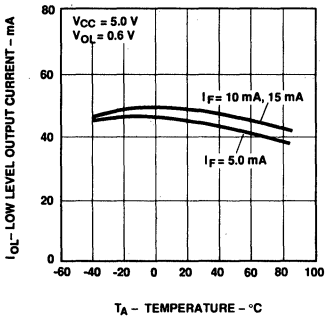


Figure 6. Low Level Output Current vs. Temperature.

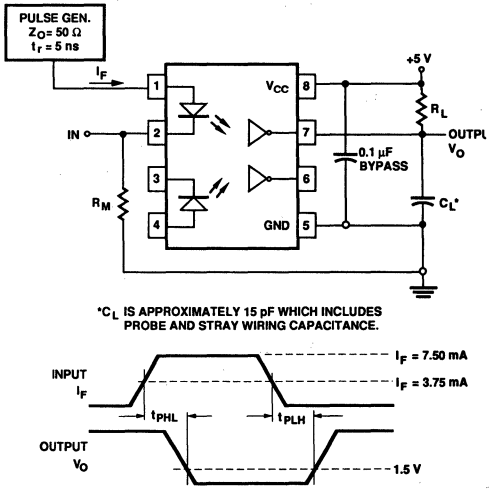


Figure 7. Test Circuit for t_{PHL} and t_{PLH} (See Note 3).

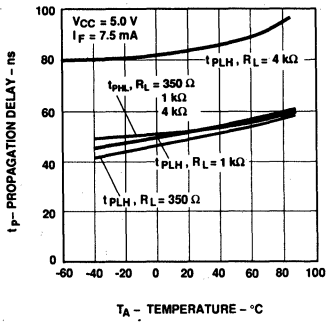


Figure 8. Propagation Delay vs. Temperature.

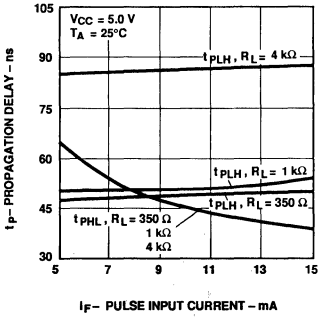


Figure 9. Propagation Delay vs. Pulse Input Current.

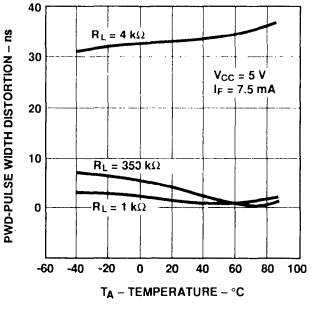


Figure 10. Pulse Width Distortion vs. Temperature.

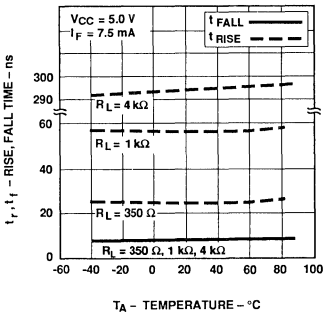


Figure 11. Rise and Fall Time vs. Temperature.

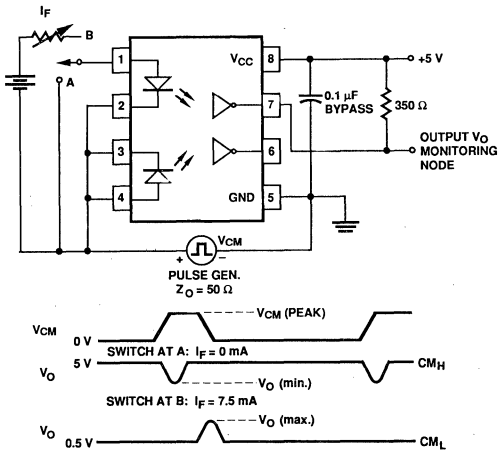


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

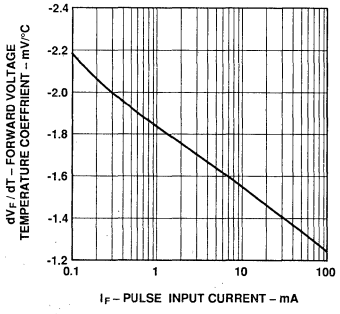
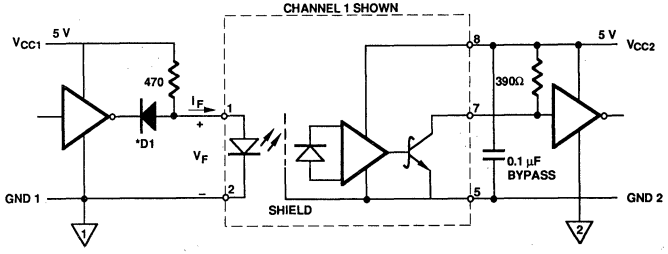


Figure 13. Temperature Coefficient of Forward Voltage vs. Input Current.



*DIODE D1 (1N916 OR EQUIVALENT) IS NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

Figure 14. Recommended TTL/ LSTTL to TTL/LSTTL Interface Circuit.

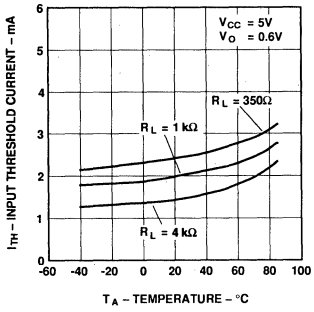


Figure 15. Input Threshold Current vs. Temperature.

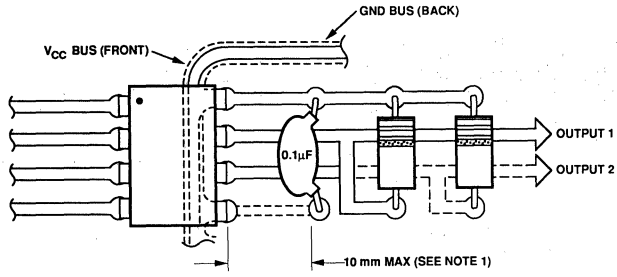


Figure 16. Recommended Printed Circuit Board Layout.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 7).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 17, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PHL} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, tPSK can determine the maximum parallel data transmission rate. Figure 18 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 18 shows

that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offers the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, input current, and power supply ranges.

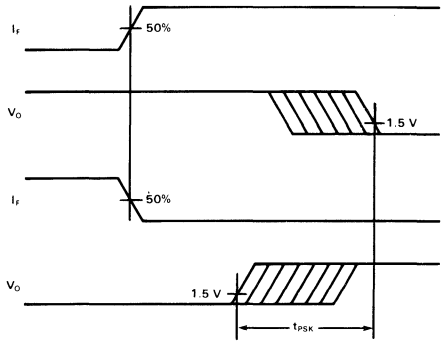


Figure 17. Illustration of Propagation Delay Skew - t_{PSK}.

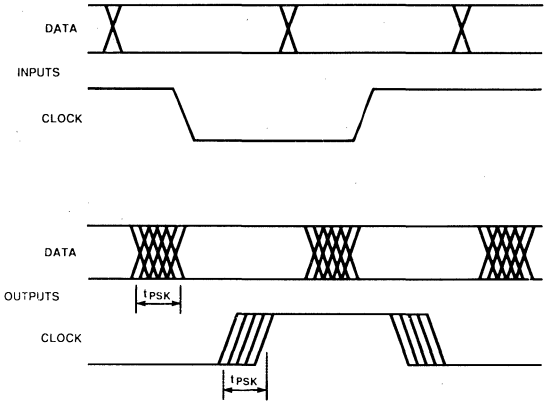


Figure 18. Parallel Data Transmission Example.

HEWLETT PACKARD

Small Outline High CMR, High Speed, Logic Gate Optocouplers

Technical Data

HCPL-0600
HCPL-0601
HCPL-0611

Features

- **Surface Mountable**
- **Industry Standard SOIC-8 Footprint**
- **Compatible with Infrared Vapor Phase Reflow and Wave Soldering Processes**
- **Internal Shield for High Common Mode Rejection (CMR)**
  HCPL-0601: 10,000 V/μs at V_{CM} = 50 V (Typical)
  HCPL-0611: 15,000 V/μs at V_{CM} = 1000 V (Typical)
- **High Speed: 10 Mbd Typical**
- **LSTTL/TTL Compatible**
- **Low Input Current Required: 5 mA**
- **Guaranteed ac and dc Performance Over Temperature: -40°C to +85°C**
- **Strobable Output**
- **CSA Approved under Component Acceptance Notice No. 5 (File No. LR 88324)**
- **Recognized under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltage of 2500 Vac, 1 Minute**

Description

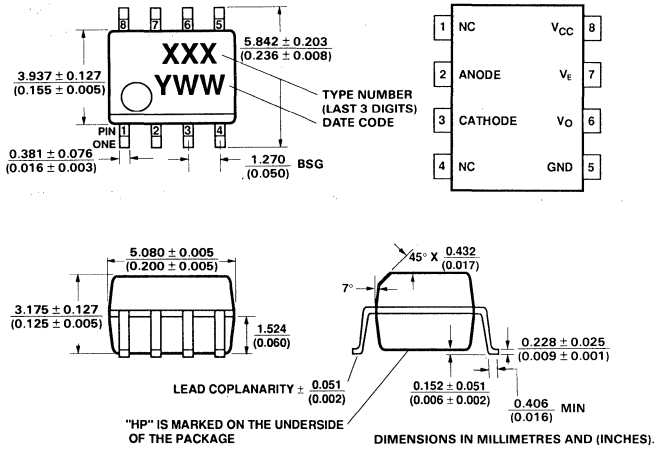
These small outline high CMR, high speed, logic gate optocouplers are single channel devices in an industry standard SOIC-8 footprint. They are electrically equivalent to the following HP optocouplers:

Small Outline	Standard DIP
HCPL-0600	6N137
HCPL-0601	HCPL-2601
HCPL-0611	HCPL-2611

The SOIC-8 package does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

The HCPL-0600/01/11 optically coupled gates combine a GaAsP light emitting diode and an

Outline Drawing*



*See notes, following page.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

integrated high gain photon detector. An enable input allows the detector to be strobed. The output of the detector I.C. is an open-collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 5000 V/μs for the HCPL–0601, and 10,000 V/μs for the HCPL-0611.

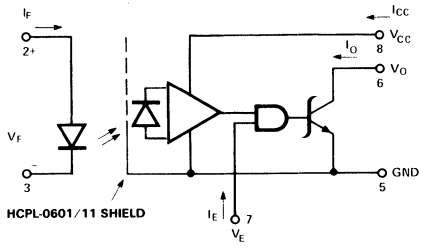
This unique design provides maximum ac and dc circuit isolation while achieving TTL compatibility. The optocoupler ac and dc operational parameters are guaranteed from -40°C to 85°C allowing trouble free system performance.

The HCPL-0600/01/11 are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate, and are recommended for use in extremely high ground or induced noise environments.

Applications

- Isolated Line Receiver
- Computer-Peripheral Interface
- Microprocessor System Interface
- Digital Isolation for A/D, D/A Conversion
- Switching Power Supply
- Instrument Input/Output Isolation
- Ground Loop Elimination
- Pulse Transformer Replacement
- Power Transistor Isolation in Motor Drives

Schematic



A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5 (See Note 1).

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}*	0	250	μA
Input Current, High Level	I_{FH}**	5	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (TTL Load)	N		10	
Output Pull-up Resistor	R_L	330	4 K	Ω
Operating Temperature	T_A	-40	+85	°C

*The off condition can also be guaranteed by ensuring that VF(off) ≤ 0.8 volts.
**The initial switching threshold is 5 mA or less. It is recommended that 6.3 mA and 10 mA be used for best performance and to permit at least 20% CTR degradation guardband.

Absolute Maximum Ratings

(No Derating Required up to 85°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to 85°C
Infrared and Vapor Phase Reflow Temperature ..... 215°C for 90 s
Forward Input Current – I_F (see Note 2) ..... 20 mA
Reverse Input Voltage ..... 5 V
Supply Voltage – V_{CC} ..... 7 V (1 Minute Maximum)
Enable Input Voltage – V_E ..... 5.5 V
(Not to exceed V_{CC} by more than 500 mV)
Output Collector Current – I_O ..... 50 mA
Output Collector Power Dissipation ..... 85 mW
Output Collector Voltage – V_O (see Note 12) ..... 7 V

Electrical Characteristics

Over recommended temperature (T_A = -40°C to +85°C) unless otherwise specified. (See note 1.)

Parameter	Symbol	Min.	Typ.*	Max.	Units	Conditions	Fig.	Note
High Level Output Current	I_{OH}		5.5	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 µA, V_E = 2.0 V	1	12
Low Level Output Voltage	V_{OL}		0.35	0.6	V	V_{CC} = 5.5 V, I_F = 5 mA, V_E = 2.0 V, I_{OL} (Sinking) = 16 mA	2, 4, 5, 15	
High Level Supply Current	I_{CCH}		7.0	10.0*	mA	V_E = 0.5 V; V_{CC} = 5.5 V, I_F = 0		
			6.5			V_E = V_{CC}; V_{CC} = 5.5 V, I_F = 0		
Low Level Supply Current	I_{CCL}		9.0	13.0*	mA	V_E = 0.5 V; V_{CC} = 5.5 V, I_F = 10 mA		
			8.5			V_E = V_{CC}; V_{CC} = 5.5 V, I_F = 10 mA		
High Level Enable Current	I_{EH}		-0.7	-1.6	mA	V_{CC} = 5.5 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}		-0.9	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5 V		
High Level Enable Voltage	V_{EH}	2.0			V			12
Low Level Enable Voltage	V_{EL}			0.8	V			
Input Forward Voltage	V_F	1.4	1.5	1.75*	V	T_A = 25°C	3, 14	
		1.3		1.80		I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA		
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz		
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 10 mA	14	
Input-Output Insulation	I_{I-O}			1	µA	45% RH, t = 5 s, V_{I-O} = 3 kVdc, T_A = 25°C		3, 15
	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 MIN		3, 15
OPT 020	V_{ISO}	5000						16
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

*All typicals at T_A = 25°C, V_{CC} = 5 V.

Switching Specifications

Over recommended temperature (T_A = -40°C to +85°C), V_{CC} = 5 V, I_F = 7.5 mA unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		20	48	75	ns	T_A = 25°C	6, 7	4
					100	ns			
Propagation Delay Time to Low Output Level	t_{PHL}		25	50	75	ns	T_A = 25°C	6, 7	5
					100	ns			
Pulse Width Distortion	$\lvert t_{PHL}-t_{PLH} \rvert$			3.5	35	ns	R_L = 350 Ω	9	14
Propagation Delay Skew	t_{PSK}			40		ns			6, 14
Output Rise Time (10-90%)	t_r			24		ns	C_L = 15 pF	12	
Output Fall Time (90-10%)	t_f			10		ns		12	
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}			30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	10, 11	7
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}			25		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	10, 11	8
Common Mode Transient Immunity at High Output Level	$\lvert CM_H \rvert$	HCPL-0600		10,000		V/μs	V_{CM} = 10 V; $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, I_F = 0 mA, T_A = 25°C	13	9, 11, 12
		HCPL-0601	5000	10,000			V_{CM} = 50 V		
		HCPL-0611	10,000	15,000			V_{CM} = 1000 V		
Common Mode Transient Immunity at Low Output Level	$\lvert CM_L \rvert$	HCPL-0600		10,000		V/μs	V_{CM} = 10 V; $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, I_F = 7.5 mA, T_A = 25°C	13	10, 11, 12
		HCPL-0601	5000	10,000			V_{CM} = 50 V		
		HCPL-0611	10,000	15,000			V_{CM} = 1000 V		

*All typicals are at V_{CC} = 5 V, T_A = 25°C

Notes:

1. Bypassing of the power supply line is required with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler as illustrated in Fig. 16. Total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. T_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the operating condition range.
7. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
8. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
9. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
10. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} < 0.8 V).
11. For sinusoidal voltages,

$$\left(\frac{\lvert dv_{CM} \rvert}{dt}\right)_{max} = \pi f_{CM} V_{CM\,(p\text{-}p)}$$

12. No external pull up is required for a high logic state on the enable input. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance.
13. Selection for higher output voltages up to 20 V is available.
14. See the last two pages of this data sheet for more information.
15. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{RMS} for one second (leakage detection current limit, $I_{I-O} \leq 5\ \mu A$).
16. In accordance with UL1577, each option 020 optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for one second (leakage detection current limit, $I_{I-O} \leq 5\ \mu A$).

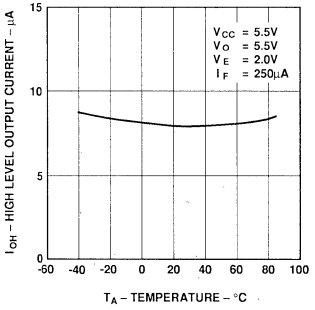


Figure 1. High Level Output Current vs. Temperature.

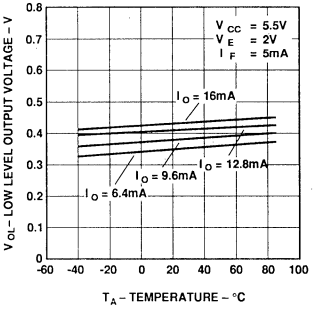


Figure 2. Low Level Output Voltage vs. Temperature.

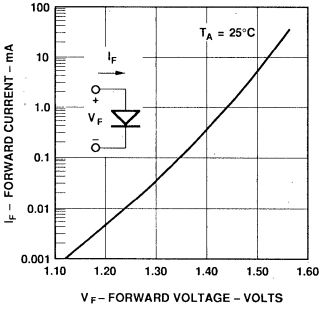


Figure 3. Input Diode Forward Characteristic.

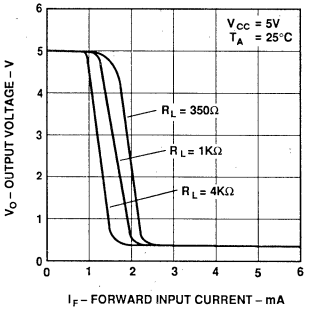


Figure 4. Output Voltage vs. Forward Input Current.

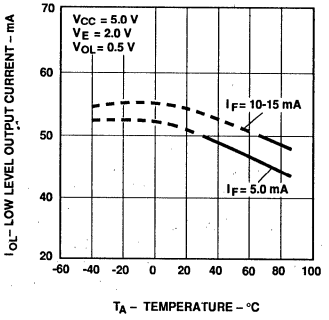


Figure 5. Low Level Output Current vs. Temperature.

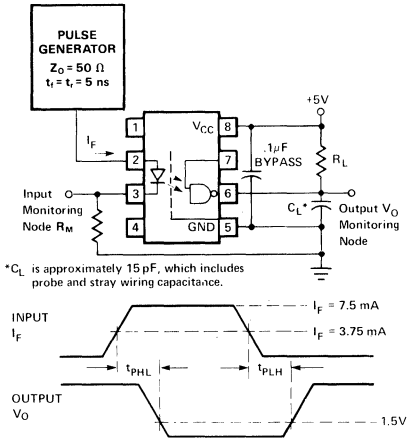


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.**

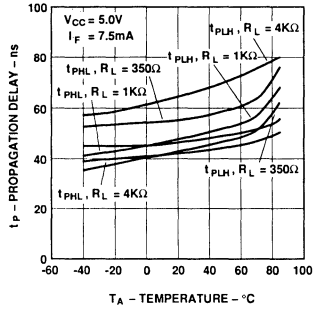


Figure 7. Propagation Delay vs. Temperature.

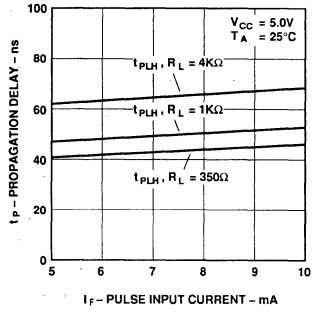


Figure 8. Propagation Delay vs. Pulse Input Current.

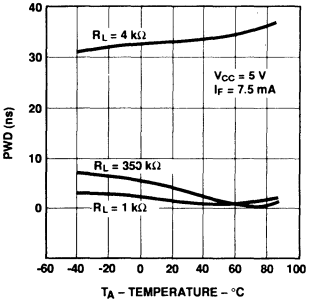


Figure 9. Pulse Width Distortion vs. Temperature.

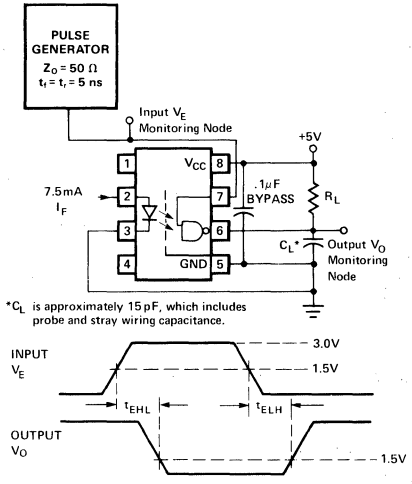


Figure 10. Test Circuit for t_{EHL} and t_{ELH}.

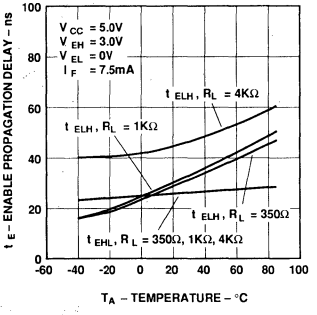


Figure 11. Enable Propagation Delay vs. Temperature.

OPTO COUPLERS

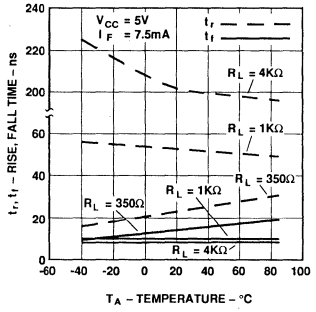


Figure 12. Rise and Fall Time vs. Temperature.

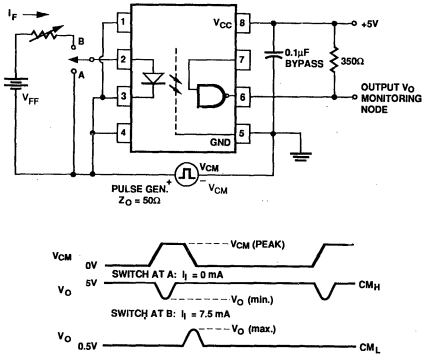


Figure 13. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

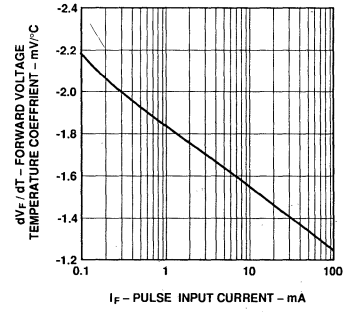


Figure 14. Temperature Coefficient of Forward Voltage vs. Input Current.

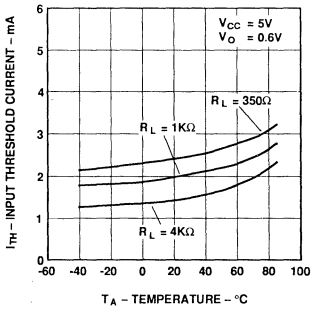


Figure 15. Input Threshold Current vs. Temperature.

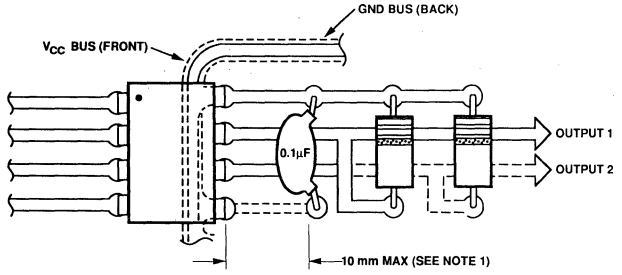


Figure 16. Recommended Printed Circuit Board Layout.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 6).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

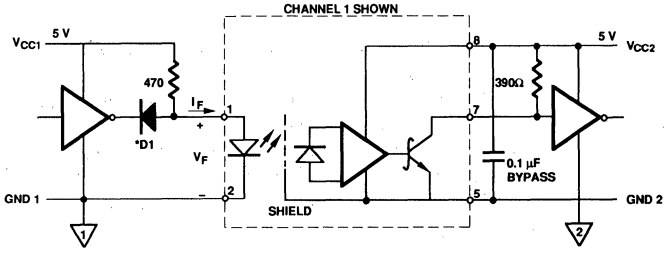
Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 18, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PHL} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 19 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 19 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, input current, and power supply ranges.



*DIODE D1 (1N916 OR EQUIVALENT) IS NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

Figure 17. Recommended TTL/LSTTL to TTL/LSTTL Interface Circuit.

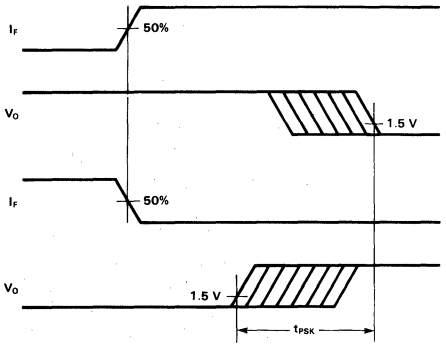


Figure 18. Illustration of Propagation Delay Skew - t_{PSK}.

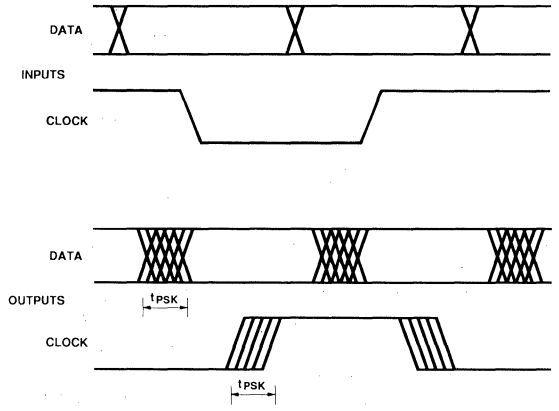


Figure 19. Parallel Data Transmission Example.

HEWLETT PACKARD

High Speed Optocouplers

Technical Data

6N135
6N136
HCPL-2502
HCPL-4502
HCPL-4503

Features

- **Very High Common Mode Transient Immunity: 15000 V/μs at V_{CM} = 1500 V Guaranteed (HCPL-4503)**
- **High Speed: 1 Mb/s**
- **TTL Compatible**
- **Guaranteed ac and dc Performance Over Temperature: 0°C to 70°C**
- **Open Collector Output**
- **Recognized under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 Vac, 1 Minute and 5000 Vac, 1 Minute (Option 020).**
- **CSA Approved under Component Acceptance Notice No. 5 (File No. LR 88324)**

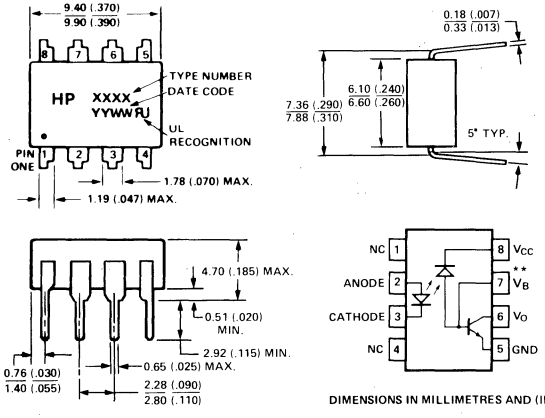
Description

These diode-transistor opto-couplers use an insulating layer between the light emitting diode and an integrated photon detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

The 6N135 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the 6N135 is 7% minimum at I_F = 16 mA.

The 6N136 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the 6N136 is 19% minimum at I_F = 16 mA.

Outline Drawing



DIMENSIONS IN MILLIMETRES AND (INCHES).

*See notes, following page.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

OPTO COUPLERS

The HCPL-2502 is suitable for use in applications where matched or known CTR is desired such as in the feedback path of switch-mode power supplies. CTR is 15 to 22% at I_F = 16mA.

The HCPL-4502 provides the electrical and switching performance of the 6N136 with increased ESD protection.

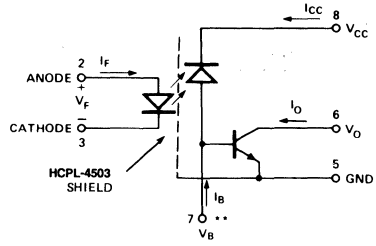
The HCPL-4503 is an HCPL-4502 with increased common mode transient immunity of 15000 V/μs minimum at V_{CM} = 1500 guaranteed.

The HCPL-4504 is recommended for IPM (Intelligent Power Module) interfacing. The HCPL-4504 is similar to the HCPL-4503, but with increased speed and CTR (See HP sales representatives for details).

Applications

- **Video Signal Isolation**
- **Line Receivers** – High common mode transient immunity (>1000 V/μs) and low input-output capacitance (0.6 pF).
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Slow Phototransistor Isolators** – Pins 2-7 of the 6N135/6 series conform to pins 1-6 of 6 pin phototransistor couplers. Pin 8 can be tied to any available bias voltage of 1.5 V to 30 V for high speed operation.
- **Replace Pulse Transformers** – Save board space and weight
- **Analog Signal Ground Isolation** – Integrated photon detector provides improved linearity over phototransistor type.

Schematic



**NOTE: FOR HCPL-4502/-3, PIN 7 IS NOT CONNECTED.

Absolute Maximum Ratings

Storage Temperature* ..... -55°C to +125°C
Operating Temperature* ..... -55°C to 100°C
Lead Solder Temperature* ..... 260°C for 10s
(1.6 mm below seating plane)
Average Input Current – I_F* .....25 mA[1]
Peak Input Current – I_F* ..... 50 mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F* ..... 1.0 A
(≤1 μs pulse width, 300 pps)
Reverse Input Voltage – V_R* (Pin 3-2) ..... 5 V
Input Power Dissipation* ..... 45 mW[3]
Average Output Current – I_O* (Pin 6) ..... 8 mA
Peak Output Current* ..... 16 mA
Emitter-Base Reverse Voltage* .....5 V
(Pin 5-7, except HCPL-4502/3)
Output Voltage* – V_O (Pin 6-5) .....-0.5 V to 15 V
Supply Voltage* – V_{CC} (Pin 8-5) ..... -0.5 V to 15 V
Output Voltage – V_O (Pin 6-5) .....-0.5 V to 20 V
Supply Voltage – V_{CC} (Pin 8-5) ..... -0.5 V to 30 V
Base Current – I_B* (Pin 7, except HCPL-4502/3) ..... 5 mA
Output Power Dissipation* .....100 mW[4]

*JEDEC Registered Data (The HCPL-2502 and HCPL-4502/3 are not registered.)

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. See note 13.

Parameter	Symbol	Device	Min.	Typ.**	Max.	Units	Test Conditions			Fig.	Note
Current Transfer Ratio	CTR*	6N135	7	18	50	%	T_A = 25°C	V_O = 0.4 V	I_F = 16 mA, V_{CC} = 4.5 V	1, 2 4	5, 11
			5	19				V_O = 0.5 V			
		6N136 HCPL-4502	19	24	50	%	T_A = 25°C	V_O = 0.4 V			
		HCPL-4503	15	25				V_O = 0.5 V			
		HCPL-2502	15	18	22	%	T_A = 25°C	V_O = 0.4 V			
Logic Low Output Voltage	V_{OL}	6N135		0.1	0.4	V	T_A = 25°C	I_O = 1.1 mA	I_F = 16 mA V_{CC} = 4.5 V		
					0.5			I_O = 0.8 mA			
		6N136 HCPL-2502 HCPL-4502 HCPL-4503		0.1	0.4	V	T_A = 25°C	I_O = 3.0 mA			
					0.5			I_O = 2.4 mA			
Logic High Output Current	I_{OH}*			0.003	0.5	µA	T_A = 25°C	V_O = V_{CC} = 5.5 V			
				0.01	1		T_A = 25°C	V_O = V_{CC} = 15.0 V	I_F = 0 mA	6	
					50						
Logic Low Supply Current	I_{CCL}			50	200	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V				13
Logic High Supply Current	I_{CCH}*			0.02	1	µA	T_A = 25°C	I_F = 0 mA, V_O = Open, V_{CC} = 15 V			13
					2						
Input Forward Voltage	V_F*			1.5	1.7	V	T_A = 25°C	I_F = 16 mA		3	
					1.8						
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10 mA				
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/ °C	I_F = 16 mA				
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0 V				
Input-Output Insulation Voltage	I_{I-O}				1	µA	45% RH, t = 5 s, V_{I-O} = 3 kVdc, T_A = 25°C				6, 16
	V_{ISO}		2500			V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C				6, 14, 15
		OPT. 020	5000			V_{RMS}					
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc				6
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz				6
Transistor DC Current Gain	h_{FE}			150			V_O = 5 V, I_O = 3 mA				
				130			V_O = 0.4 V, Ib = 20 µA				

*For JEDEC registered parts. **All typicals at T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}*	6N135		0.2	1.5	µs	T_A = 25°C, R_L = 4.1 kΩ	5, 9, 11	8, 9
					2.0				
		6N136 HCPL-2502 HCPL-4502 HCPL-4503		0.2	0.8		T_A = 25°C, R_L = 1.9 kΩ		
					1.0				
Propagation Delay Time to Logic High at Output	t_{PLH}*	6N135		1.3	1.5	µs	T_A = 25°C, R_L = 4.1 kΩ 11	5, 9,	8, 9
					2.0				
		6N136 HCPL-2502 HCPL-4502 HCPL-4503		0.6	0.8		T_A = 25°C, R_L = 1.9 kΩ		
					1.0				
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	6N135		1		kV/µs	R_L = 4.1 kΩ, I_F = 0 mA, T_A = 25°C, V_{CM} = 10 V_{p-p}	10	7, 8, 9
		6N136 HCPL-2502 HCPL-4502		1			R_L = 1.9 kΩ, C_L = 15 pF		
		HCPL-4503	15	30			R_L = 1.9 kΩ, I_F = 0 mA, T_A = 25°C, V_{CM} = 1500 V_{p-p}, C_L = 15 pF		
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	6N135		1		kV/µs	R_L = 4.1 kΩ, I_F = 16 mA, T_A = 25°C, V_{CM} = 10 V_{p-p}	10	7, 8, 9
		6N136 HCPL-2502 HCPL-4502		1			R_L = 1.9 kΩ, C_L = 15 pF		
		HCPL-4503	15	30			R_L = 1.9 kΩ, I_F = 16 mA, T_A = 25°C, V_{CM} = 1500 V_{p-p}, C_L = 15 pF		
Bandwidth	BW	6N135/6 HCPL-2502		9		MHz	See Test Circuit	7, 8	10

*JEDEC registered specification for 6N135/6. **All typicals at T_A = 25°C.

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C.
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_o, to the forward LED input current, I_F, times 100.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_o > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_o < 0.8 V).
8. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
9. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull-up resistor.
10. The frequency at which the ac output voltage is 3 dB below its mid-frequency value.
11. The JEDEC registration for the 6N136 specifies a minimum CTR of 15%. HP guarantees a minimum CTR of 19%.
12. See Option 020 data sheet for more information.
13. Use of a 0.1 µf bypass capacitor connected between pins 5 and 8 is recommended.
14. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, I_{i-o} ≤ 5 µA.
15. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 second (leakage detection current limit, I_{i-o} ≤ 5 µA.
16. This rating is equally validated by an equivalent ac proof test.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(I01)	> 7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(I02)	> 7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Insulation thickness between emitter and detector
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (Per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

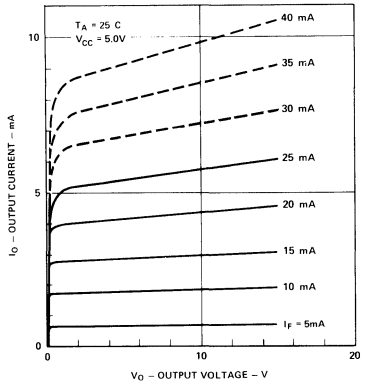


Figure 1. DC and Pulsed Transfer Characteristics.

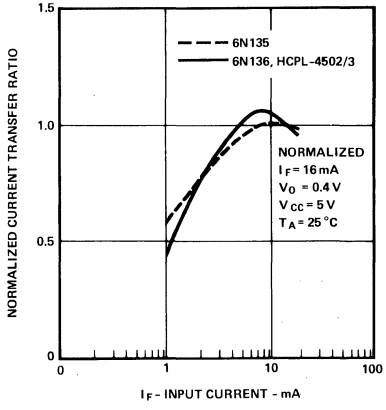


Figure 2. Current Transfer Ratio vs. Input Current.

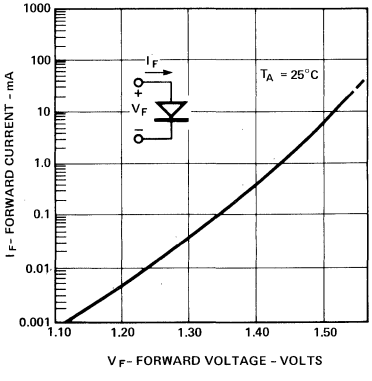


Figure 3. Input Current vs. Forward Voltage.

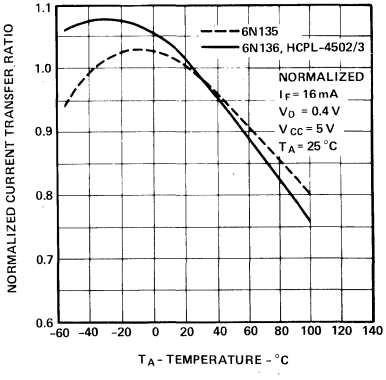


Figure 4. Current Transfer Ratio vs. Temperature.

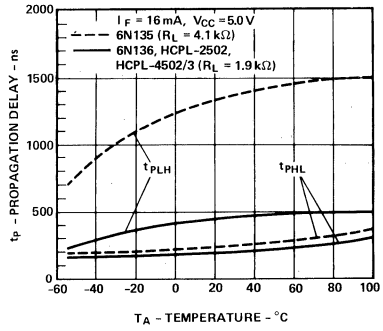


Figure 5. Propagation Delay vs. Temperature.

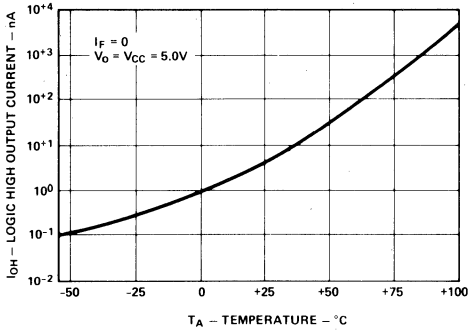


Figure 6. Logic High Output Current vs. Temperature.

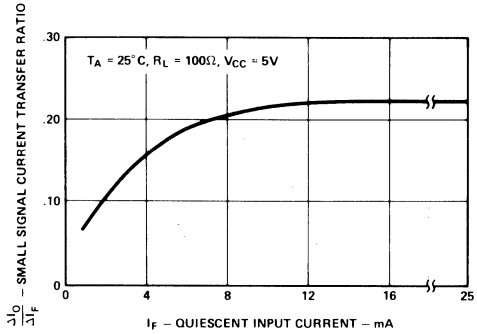
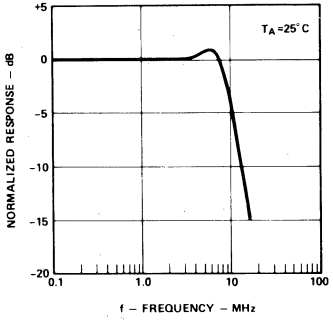


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.



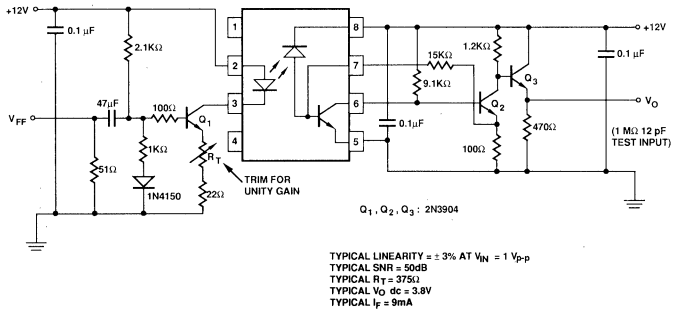


Figure 8. Frequency Response.

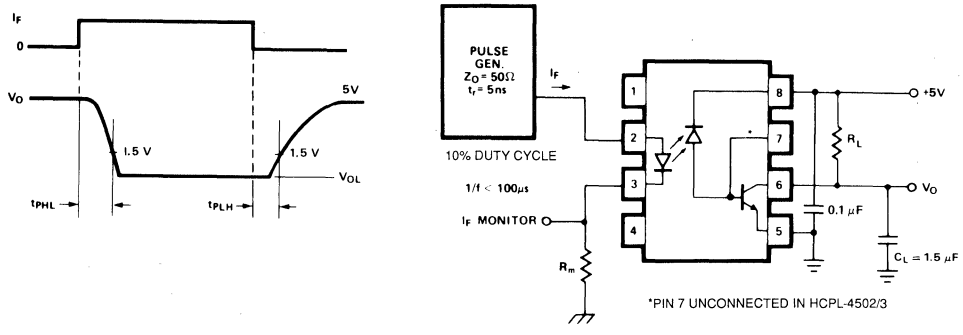


Figure 9. Switching Test Circuit.*

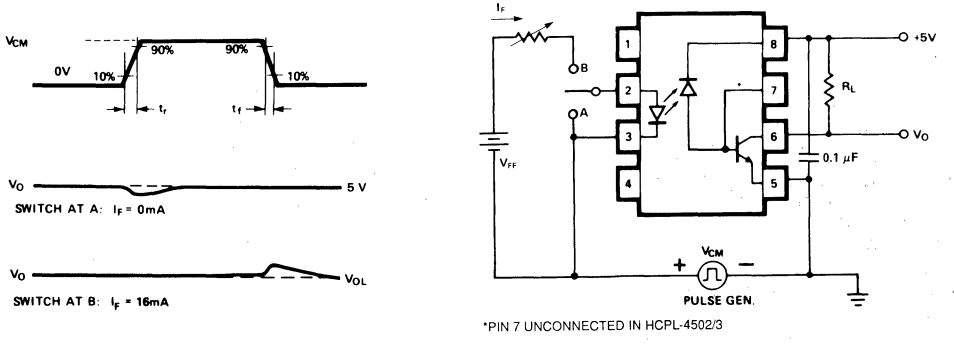


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

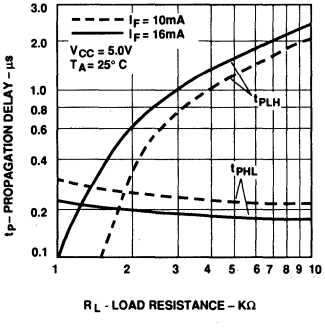


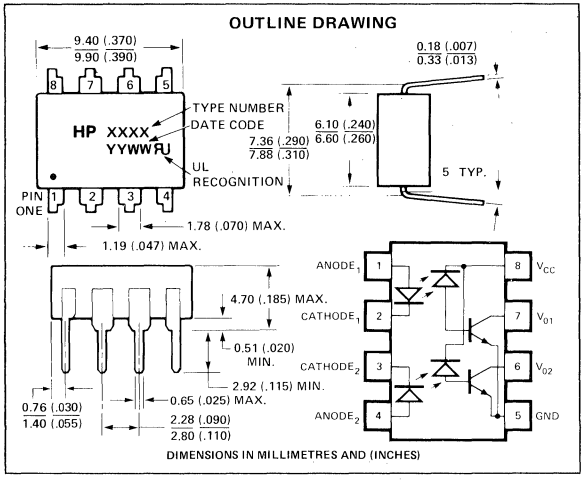
Figure 11. Propagation Delay Time vs. Load Resistance.

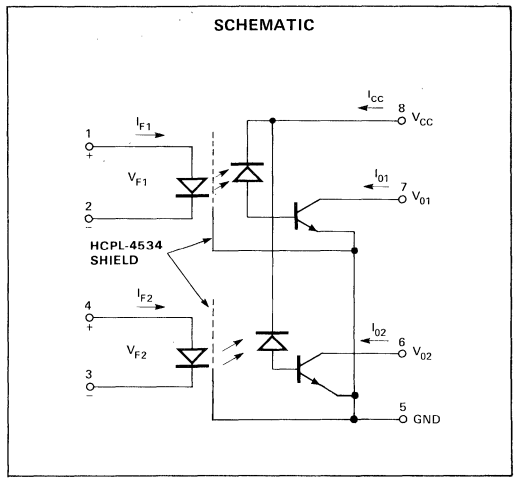
*JEDEC Registered Data

HEWLETT PACKARD

DUAL HIGH SPEED OPTOCOUPLER

HCPL-2530
HCPL-2531
HCPL-4534





Features

- **HIGH SPEED: 1 Mb/s**
- **TTL COMPATIBLE**
- **VERY HIGH COMMON MODE TRANSIENT IMMUNITY: 15000 V/μs @ V_{CM} = 1500 V GUARANTEED (HCPL-4534)**
- **HIGH DENSITY PACKAGING**
- **3 MHz BANDWIDTH**
- **OPEN COLLECTOR OUTPUTS**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE AND 5000 VAC, 1 MINUTE (OPTION 020) PENDING APPROVAL**
- **CSA APPROVED UNDER COMPONENT ACCEPTANCE NOTICE NO. 5 (FILE NO. LR88324)**
- **MIL-STD-1772 VERSION AVAILABLE (HCPL-5530/31)**

Description

These dual optocouplers contain a pair of light emitting diodes and integrated photo detectors with electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collectors increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

The HCPL-2530 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the -2530 is 7% minimum at I_F = 16 mA.

The HCPL-2531 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the -2531 is 19% minimum at I_F = 16 mA.

The HCPL-4534 is an HCPL-2531 with increased common mode transient immunity of 15000 V/μs minimum at V_{CM} = 1500 V guaranteed.

Applications

- **Line Receivers** – High common mode transient immunity (>1000V/μs) and low input-output capacitance (0.6pF).
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Pulse Transformers** – Save board space and weight.
- **Analog Signal Ground Isolation** – Integrated photon detector provides improved linearity over phototransistor type.
- **Polarity Sensing.**
- **Isolated Analog Amplifier** – Dual channel packaging enhances thermal tracking.

Absolute Maximum Ratings

Storage Temperature . . . . . -55°C to +125°C
Operating Temperature . . . . . -55°C to +100°C
Lead Solder Temperature . . . . . 260°C for 10s
(1.6mm below seating plane)
Average Input Current – I_F (each channel) . . . . . 25mA[1]
Peak Input Current – I_F (each channel) . . . . . 50mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F (each channel) . . . . 1.0 A
(≤1μs pulse width, 300pps)
Reverse Input Voltage – V_R (each channel) 5V
Input Power Dissipation (each channel) . . . . . 45mW[3]
Average Output Current – I_O (each channel) 8mA
Peak Output Current – I_O (each channel) 16mA
Supply Voltage - V_{CC} (Pin 8-5) . . . . . - 0.5V to 30V
Output Voltage - V_O (Pin 7,6-5) . . . . . - 0.5V to 20V
Output Power Dissipation (each channel) . . . . . 35mW[4]

See notes, following page.

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. See note 13.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions			Fig.	Note
Current Transfer Ratio	CTR	HCPL-2530	7	18	50	%	T_A = 25°C	V_O = 0.5 V	I_F = 16 mA, V_{CC} = 4.5 V	1, 2 4	5, 6
			5					V_O = 0.5 V			
		HCPL-2531 HCPL-4534	19	24	50	%	T_A = 25°C	V_O = 0.5 V			
			15					V_O = 0.5 V			
Logic Low Output Voltage	V_{OL}	HCPL-2530		0.1	0.4	V	T_A = 25°C	I_O = 1.1 mA	I_F = 16 mA, V_{CC} = 4.5 V	1	5
					0.5			I_O = 0.8 mA			
		HCPL-2531 HCPL-4534		0.1	0.4	V	T_A = 25°C	I_O = 3.0 mA			
					0.5			I_O = 2.4 mA			
Logic High Output Current	I_{OH}			0.003	0.5	µA	T_A = 25°C	V_O = V_{CC} = 5.5 V	I_F = 0 mA	6	5
							T_A = 25°C	V_O = V_{CC} = 15.0 V			
					50						
Logic Low Supply Current	I_{CCL}			100	400	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V				
Logic High Supply Current	I_{CCH}			0.05	4	µA	I_F = 0 mA, V_O = Open, V_{CC} = 15 V				
Input Forward Voltage	V_F			1.5	1.7	V	T_A = 25°C	I_F = 16 mA		3	5
					1.8						
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA				5
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16 mA				
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0 V				5
Input-Output Insulation Voltage	V_{ISO}		2500			V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C				7, 14
OPT 020 (PENDING)	V_{ISO}		5000								7, 15
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc				7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz				7
Input-Input Insulation Leakage Current	I_{I-I}			0.005		µA	45% Relative Humidity, t = 5 s V_{I-I} = 500 Vdc				8
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω	V_{I-I} = 500 Vdc				8
Capacitance (Input-Input)	C_{I-I}			0.25		pF	f = 1 MHz				8

*All typicals at 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA, unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	HCPL-2530		0.2	1.5	μs	T_A = 25°C	R_L = 4.1 kΩ	5, 9, 11	10, 11
					2.0					
		HCPL-2531 HCPL-4534		0.2	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Propagation Delay Time to Logic High at Output	t_{PLH}	HCPL-2530		1.3	1.5	μs	T_A = 25°C	R_L = 4.1 kΩ	5, 9, 11	10, 11
					2.0					
		HCPL-2531 HCPL-4534		0.6	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	HCPL-2530	1	10		KV/μs	R_L = 4.1 kΩ	I_F = 0 mA, T_A = 25°C, V_{CM} = 10 V_{P-P}	10	9, 10, 11
		HCPL-2531	1	10			R_L = 1.9 kΩ			
		HCPL-4534	15	30			R_L = 1.9 kΩ	I_F = 0 mA, T_A = 25°C, V_{CM} = 1500 V_{P-P}		
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	HCPL-2530	1	10		KV/μs	R_L = 4.1 kΩ	I_F = 16 mA, T_A = 25°C, V_{CM} = 10 V_{P-P}	10	9, 10, 11
		HCPL-2531	1	10			R_L = 1.9 kΩ			
		HCPL-4534	15	30			R_L = 1.9 kΩ	I_F = 16 mA, T_A = 25°C, V_{CM} = 1500 V_{P-P}		

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min.External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 1.0 mW/°C.
5. Each channel.
6. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
7. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
10. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
11. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull-up resistor.
12. The frequency at which the ac output voltage is 3 dB below the low frequency asymptote.
13. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
14. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ μA).
15. **In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ μA).**

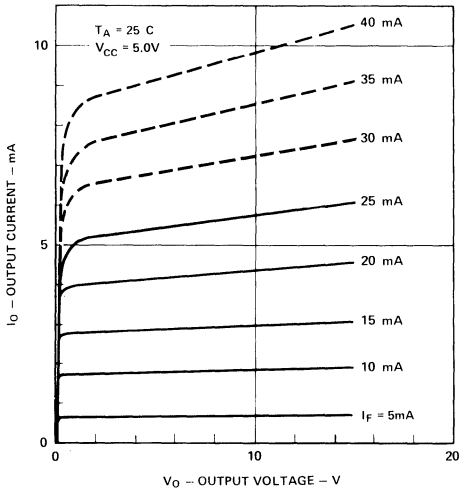


Figure 1. DC and Pulsed Transfer Characteristics.

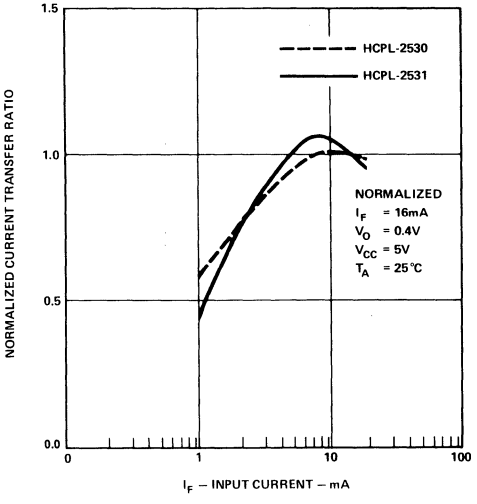


Figure 2. Current Transfer Ratio vs. Input Current.

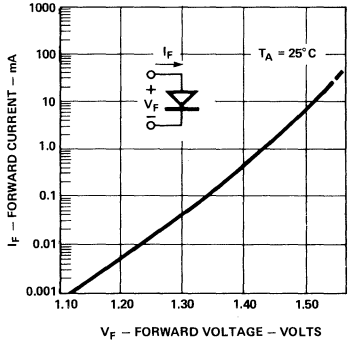


Figure 3. Input Current vs. Forward Voltage.

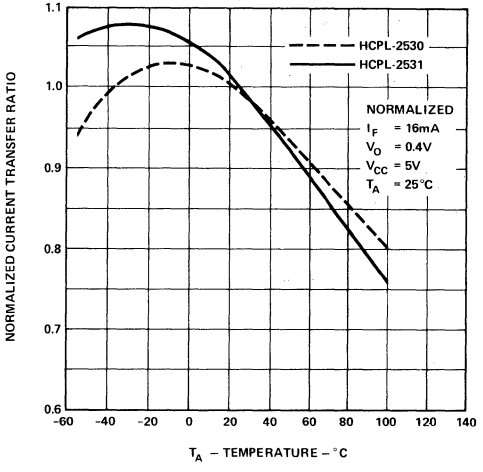


Figure 4. Current Transfer Ratio vs. Temperature.

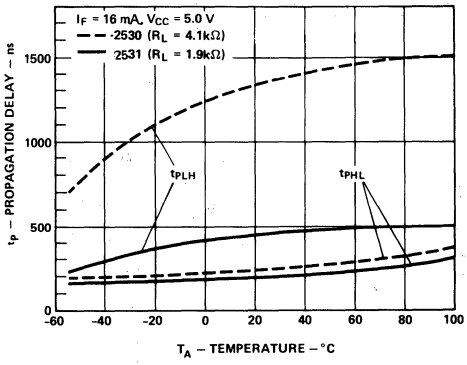


Figure 5. Propagation Delay vs. Temperature.

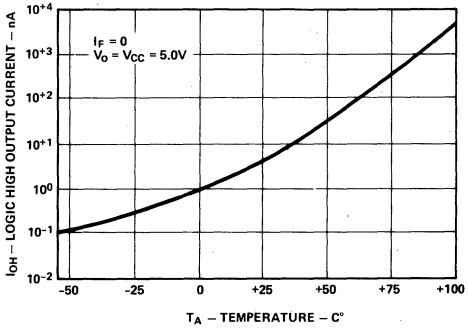


Figure 6. Logic High Output Current vs. Temperature.

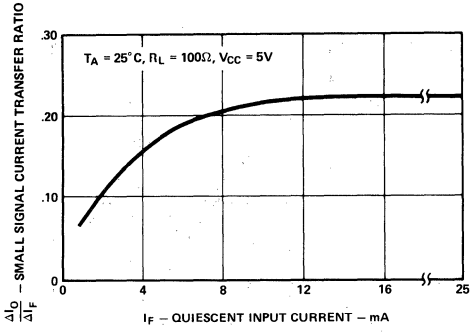
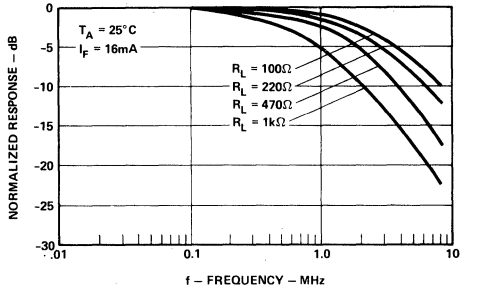


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.



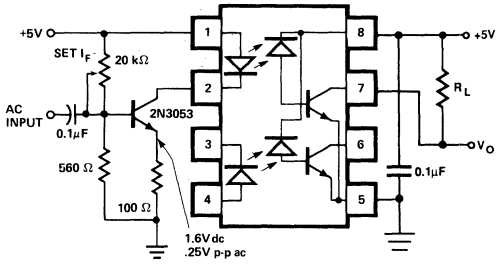


Figure 8. Frequency Response.

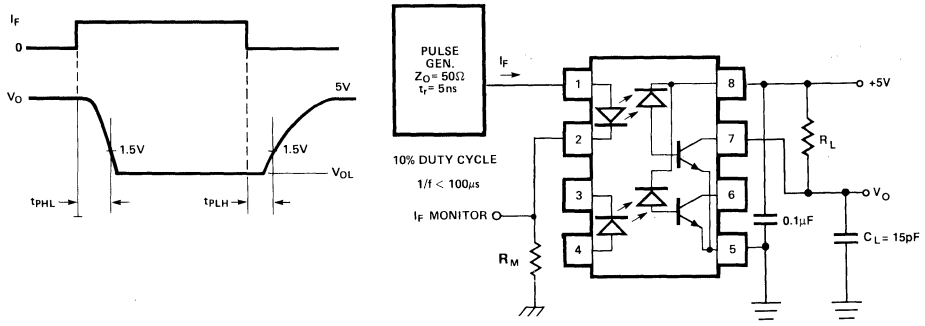


Figure 9. Switching Test Circuit.

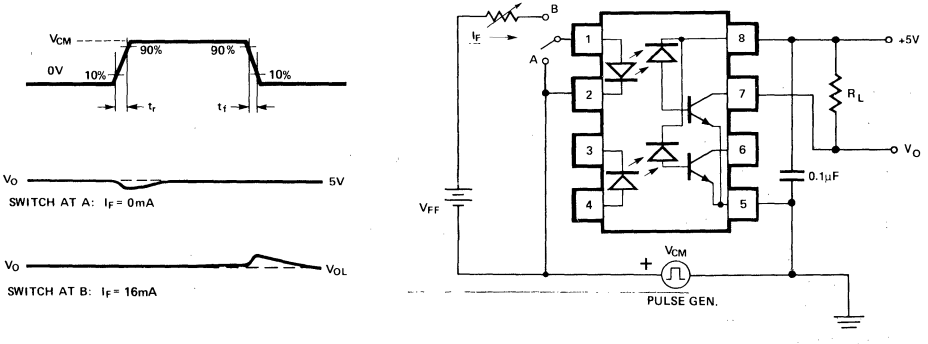


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

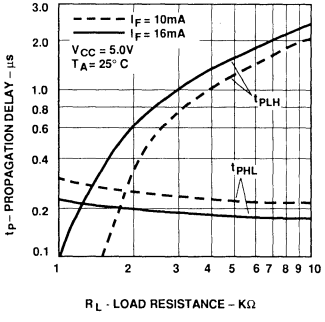


Figure 11. Propagation Delay Time vs. Load Resistance.

HEWLETT PACKARD

Small Outline High Speed Optocouplers

Technical Data

HCPL-0500
HCPL-0501
HCPL-0452
HCPL-0453

Features

- **Surface Mountable**
- **Industry Standard SOIC-8 Footprint**
- **Compatible with Infrared Vapor Phase Reflow and Wave Soldering Processes**
- **Very High Common Mode Transient Immunity: 15000 V/μs at V_{CM} = 1500 V Guaranteed (HCPL-0453)**
- **High Speed: 1 Mb/s**
- **TTL Compatible**
- **Guaranteed ac and dc Performance Over Temperature: 0°C to 70°C**
- **Open Collector Output**
- **Recognized Under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltage of 2500 VAC, 1 Minute**

Description

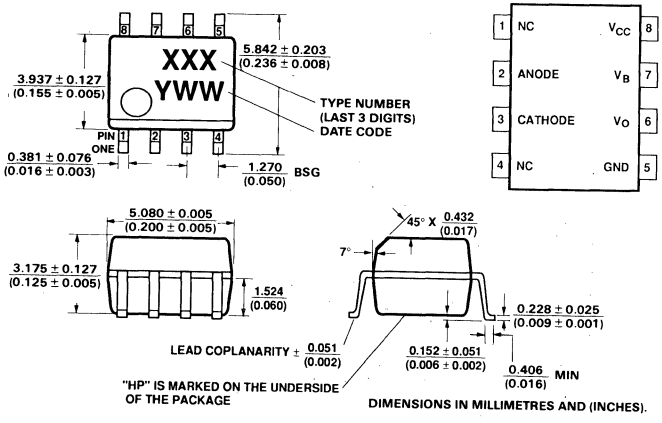
These small outline high CMR, high speed, logic gate optocouplers are single channel devices in an industry standard SOIC-8 footprint. They are electrically equivalent to the following HP optocouplers:

Small Outline	Standard DIP
HCPL-0500	6N135
HCPL-0501	6N136
HCPL-0452	HCPL-4502
HCPL-0453	HCPL-4503

The SOIC-8 package does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

These diode-transistor optocouplers use an insulating layer between the light emitting diode and an integrated photon detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

Outline Drawing*



*See notes, following page.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

The HCPL-0500 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the HCPL-0500 is 7% minimum at I_F = 16 mA.

The HCPL-0501 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the HCPL-0501 is 19% minimum at I_F = 16 mA.

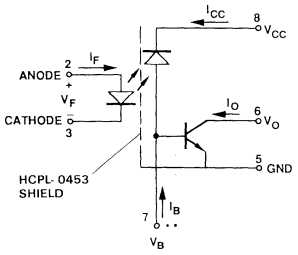
The HCPL-0452 provides the electrical and switching performance of the HCPL-0501 with increased ESD protection.

The HCPL-0453 is an HCPL–0452 with increased common mode transient immunity of 15000 V/μs minimum at V_{CM} = 1500 V guaranteed.

Applications

- **Video Signal Isolation**
- **Line Receivers** – High common mode transient immunity (>1000 V/μs) and low input-output capacitance (0.6 pF).
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Slow Phototransistor Isolators** – Pins 2-7 of the HCPL-0500/0501 series conform to pins 1-6 of 6 pin phototransistor couplers. Pin 8 can be tied to any available bias voltage of 1.5 V to 30 V for high speed operation.
- **Replace Pulse Transformers** – Save board space and weight
- **Analog Signal Ground Isolation** – Integrated photon detector provides improved linearity over phototransistor type.

Schematic



**NOTE: FOR HCPL-0452/3, PIN 7 IS NOT CONNECTED.

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -55°C to 100°C
Infrared and Vapor Phase Reflow Temperature ..... 215°C for 90 s
Average Input Current – I_F ..... 25 mA[1]
Peak Input Current – I_F ..... 50 mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F ..... 1.0 A
(≤1 μs pulse width, 300 pps)
Reverse Input Voltage – V_R (Pin 3-2) ..... 5 V
Input Power Dissipation ..... 45 mW[3]
Average Output Current – I_O (Pin 6) ..... 8 mA
Peak Output Current ..... 16 mA
Emitter-Base Reverse Voltage ..... 5 V
(Pin 5-7, except HCPL-0452/3)
Output Voltage – V_O (Pin 6-5) ..... -0.5 V to 20 V
Supply Voltage – V_{CC} (Pin 8-5) ..... -0.5 V to 30 V
Base Current – I_B (Pin 7, except HCPL-0452/3) ..... 5 mA
Output Power Dissipation ..... 100 mW[4]

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C), unless otherwise specified. (See note 11.)

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	HCPL-0500	7	18	50	%	T_A = 25°C, V_O = 0.4 V	1, 2, 4	5
			5	19			V_O = 0.5 V, I_F = 16 mA, V_{CC} = 4.5 V		
		HCPL-0501 HCPL-0452 HCPL-0453	19	24	50	%	T_A = 25°C, V_O = 0.4 V		
			15	25			V_O = 0.5 V		
Logic Low Output Voltage	V_{OL}	HCPL-0500		0.1	0.4	V	T_A = 25°C, I_O = 1.1 mA, I_F = 16 mA, V_{CC} = 4.5 V		
					0.5		I_O = 0.8 mA		
		HCPL-0501 HCPL-0452 HCPL-0453		0.1	0.4	V	T_A = 25°C, I_O = 3.0 mA		
					0.5		I_O = 2.4 mA		
Logic High Output Current	I_{OH}			0.003	0.5	µA	T_A = 25°C, V_O = V_{CC} = 5.5 V, I_F = 0 mA	7	
				0.01	1		T_A = 25°C, V_O = V_{CC} = 15.0 V, I_F = 0 mA		
					50				
Logic Low Supply Current	I_{CCL}			50	200	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V		11
Logic High Supply Current	I_{CCH}			0.02	1	µA	T_A = 25°C, I_F = 0 mA, V_O = Open, V_{CC} = 15 V		11
					2				
Input Forward Voltage	V_F			1.5	1.7	V	T_A = 25°C, I_F = 16 mA	3	
					1.8				
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16 mA		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		
Input-Output Insulation	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 MIN., T_A = 25°C		6, 12
Resistance (Input-Output)	R_{I-O}			10^{14}		Ω	V_{I-O} = 500 Vdc		6
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		6
Transistor DC Current Gain	h_{FE}			150			V_O = 5 V, I_O = 3 mA		
				130			V_O = 0.4 V, I_O = 20 mA		

*All typicals at T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	HCPL-0500		0.2	1.5	µs	T_A = 25°C	R_L = 4.1 kΩ	5, 6, 10	8, 9
					2.0					
		HCPL-0501 HCPL-0452 HCPL-0453		0.2	0.8 1.0		T_A = 25°C	R_L = 1.9 kΩ		
Propagation Delay Time to Logic High at Output	t_{PLH}	HCPL-0500		1.3	1.5	µs	T_A = 25°C	R_L = 4.1 kΩ	5, 6, 10	8, 9
					2.0					
		HCPL-0501 HCPL-0452 HCPL-0453		0.6	0.8 1.0		T_A = 25°C	R_L = 1.9 kΩ		
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	HCPL-0500		1		kV/µs	R_L = 4.1 kΩ	I_F = 0 mA, T_A = 25°C V_{CM} = 10 V_{p-p}	11	7, 8, 9
		HCPL-0501 HCPL-0452		1			R_L = 1.9 kΩ			
		HCPL-0453	15	30			R_L = 1.9 kΩ	I_F = 0 mA, T_A = 25°C, V_{CM} = 1500 V_{p-p},		
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	HCPL-0500		1		kV/µs	R_L = 4.1 kΩ	I_F = 16 mA, T_A = 25°C V_{CM} = 10 V_{p-p}	11	7, 8, 9
		HCPL-0501 HCPL-0452		1			R_L = 1.9 kΩ			
		HCPL-0453	15	30			R_L = 1.9 kΩ	I_F = 16 mA, T_A = 25°C, V_{CM} = 1500 V_{p-p},		
Bandwidth	BW			9		MHz	See Test Circuit		8, 9	10

*All typicals at T_A = 25°C.

Notes:

1. Derate linearly above 85°C free-air temperature at a rate of 0.5 mA/°C.
2. Derate linearly above 85°C free-air temperature at a rate of 1.0 mA/°C.
3. Derate linearly above 85°C free-air temperature at a rate of 1.1 mW/°C.
4. Derate linearly above 85°C free-air temperature at a rate of 2.3 mW/°C.
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together. The 2500 Vac/1 MINUTE CAPABILITY IS VALIDATED by a factory 3200 Vac/1 second dielectric voltage withstand test.
7. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
8. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
9. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull-up resistor.
10. The frequency at which the ac output voltage is 3 dB below its mid-frequency value.
11. Use of a 0.1 µf bypass capacitor connected between pins 5 and 8 is recommended.
12. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, I_{i-o} ≤ 5 µA.

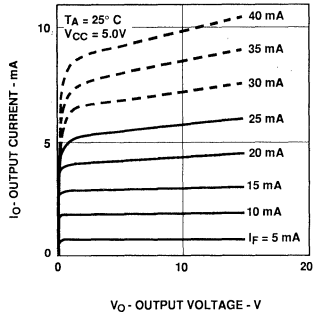


Figure 1. DC and Pulsed Transfer Characteristics.

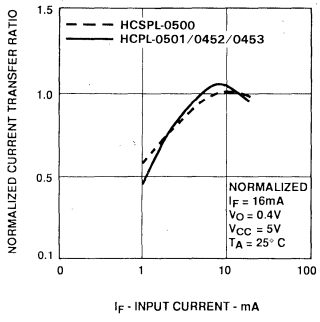


Figure 2. Current Transfer Ratio vs. Input Current.

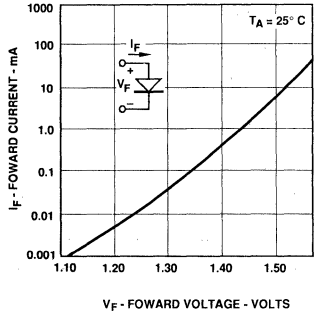


Figure 3. Input Current vs. Forward Voltage.

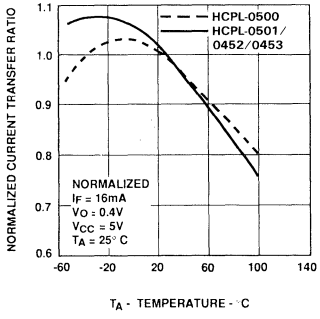


Figure 4. Current Transfer Ratio vs. Temperature.

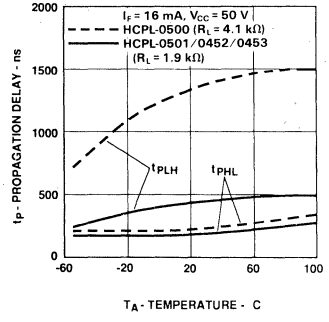


Figure 5. Propagation Delay vs. Temperature.

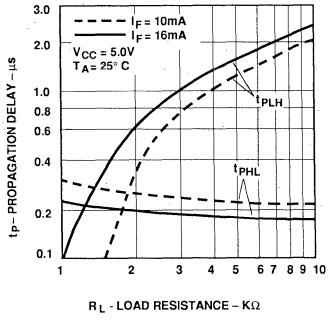


Figure 6. Propagation Delay Time vs. Load Resistance.

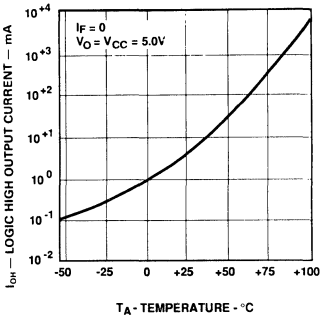


Figure 7. Logic High Output Current vs. Temperature.

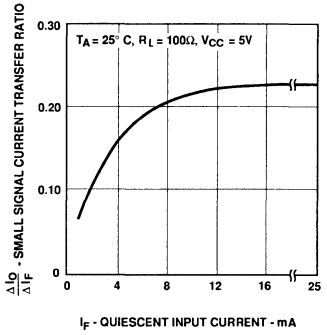
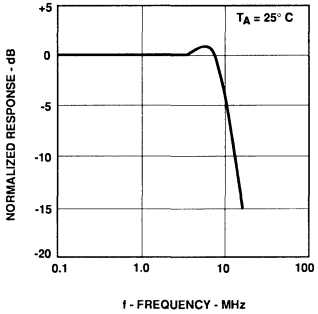


Figure 8. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.



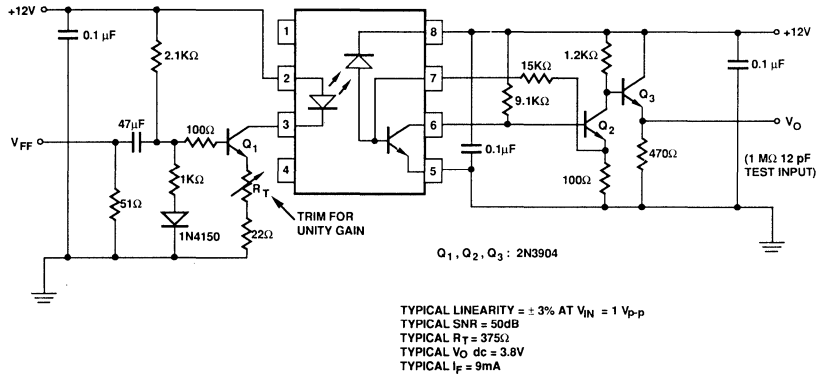


Figure 9. Frequency Response.

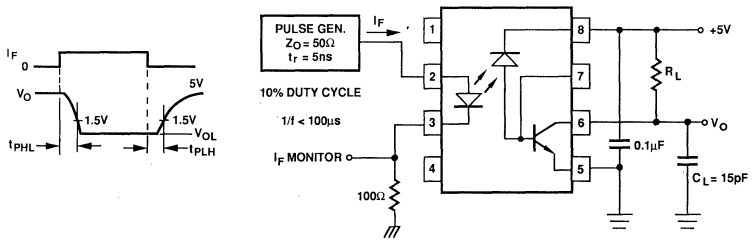


Figure 10. Switching Test Circuit.

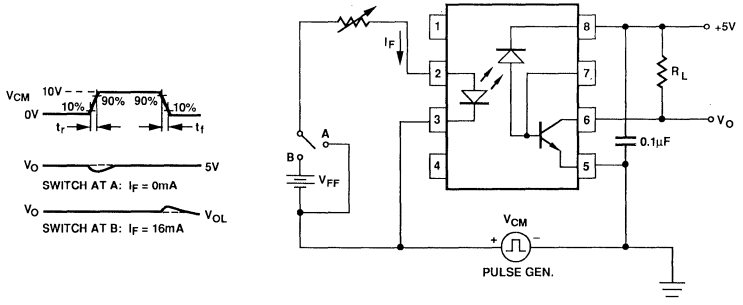


Figure 11. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

High Speed Optocouplers

Technical Data

CNW135
CNW136
CNW4502
New **CNW4503**

Features

- **5000 Vrms/1 Minute Insulation Withstand Capability**
- **Worldwide Safety Approval**
  - UL1577 (File No. E55361)
  - VDE 0884 Certification (V_{IORM} = 1 kV_{RMS})
  - VDE 860/805/806/804/750-1/IEC950
  - BSI according to BS 415/7002/6301
  - SETI-SEMKO-NEMKO DEMKO according to IEC 65/380/950/335
- **High Speed: 1 Mbit/s**
- **TTL Compatible**
- **Performance Guaranteed over Temperature 0°C to 70°C**
- **Pin Compatible with 6N135/6 and HCPL-4502/3**
- **Very High Common Mode Rejection for CNW4503**
- **Line Receivers (15 K V/μs Common Mode Transient Immunity and Low Input-Output Capacitance of 0.6 pF)**
- **Analog Signal Ground Isolation (Integrated Photon Detector Provides Improved Linearity over Phototransistor Type)**

Applications

- **High Voltage Insulation**
- **Video Signal Isolation**
- **Feedback Element in Switched Mode Power Supplies**
- **High Speed Logic Ground Isolation – TTL/TTL, TTL/CMOS, TTL/LSTTL**
- **Power Transistors Isolation in Motor Drives**
- **Replaces Pulse Transformers**
- **Replaces Slow Photo-Transistor Isolators (Pins 2-7 of the CNW135/6 Conforms to Pins 1-6 of 6 Pin Phototransistor Couplers. Pin 8 can be Tied to any Available BiasVoltage of 1.5 V to 30 V for High Speed Operation)**

Description

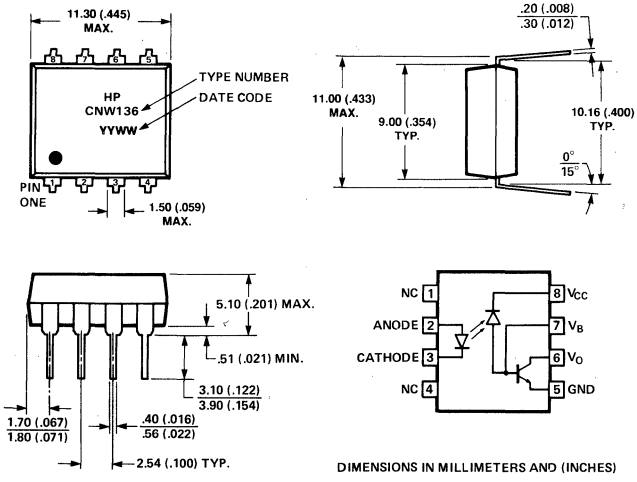
These devices are high voltage and fast switching optocouplers consisting of an AlGaAs LED and a silicon photodetector. A wide body encapsulation is used to provide creepage and clearance dimensions suitable for safety approval by regulatory agencies worldwide.

The CNW135 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications.

Current transfer ratio (CTR) for the CNW135 is 7% minimum at I_F = 16 mA.

OPTO COUPLERS

Package Outline



DIMENSIONS IN MILLIMETERS AND (INCHES)

The CNW136 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6K pullup resistor. CTR of the CNW136 is 19% minimum at I_F = 16 mA. Selection for higher CTR is available.

The CNW4502/3 provides the electrical and switching performance of the CNW136, increased ESD protection and increased transient immunity.

Regulatory Information

These products feature a wide body 8 PIN DIP. This package was specifically designed to meet regulatory requirements worldwide. The CNW135/6 and CNW4502/3* have been approved by the following organizations:

UL – Covered under UL component recognition FILE E55361

VDE – Approved according to VDE 0884 (marks License No. 70975)
Complies for reinforced insulation at 250 V AC with:
DIN IEC 380/VDE 0806
DIN IEC 435/VDE 0805 "ENTWURF"
DIN 57804/VDE 0804 (isolation group C)
DIN VDE 0860 (HD 195 S6)
DIN IEC 601 Teil 1/VDE 0750-1
DIN VDE 0160
EN 60950/IEC950

NORDIC – Tested for applications (reinforced insulation) – Class II applications for plugable apparatus in normal tight execution.
-SETI-SEMKO-NEMKO-DEMKO-According to IEC 65-IEC380-IEC950-IEC335

BSI – Certification according to BS415:1990, BS7002:1989 and BS6301: 1982 for class II applications.

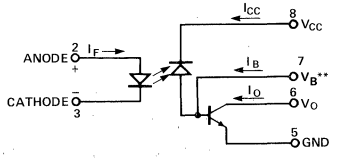
*Pending SETI and SEMKO approval

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -55°C to 85°C
Lead Solder Temperature ..... 260°C for 10s (up to seating plane)
Average Input Current – I_F ..... 100 mA
Peak Transient Input Current – I_F ..... 1.0 A (≤1 µs pulse width, 300 Hz)
Reverse Input Voltage – V_R (Pin 3-2) ..... 5 V
Input Power Dissipation (up to 70°C) ..... 250 mW*
Average Output Current – I_O (Pin 6) ..... 10 mA
Emitter-Base Reverse Voltage (Pin 5-7) ..... 5 V
Output Voltage – V_O (Pin 6-5) ..... -0.5 V to 20 V
Supply Voltage – V_{CC} (Pin 8-5) ..... -0.5 V to 30 V
Base Current – I_B (Pin 7, except HCPL-4502/3) ..... 5 mA
Output Power Dissipation ..... 100 mW

*Derate at 5.0 mW/°C for operating temperatures above 70°C.

Schematic



**Note: For CNW4502/3, Pin 7 is not connected.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assemby of this component to prevent damage and/or degradation which may be induced by ESD.

VDE 0884 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0109/12.83, Table 1 for rated mains voltage ≤ 600 V_{RMS} for rated mains voltage ≤ 1000 V_{RMS}		 I-IV I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0109/12.83)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{PEAK}
		1000	V_{RMS}
Input to Output Test Voltage, Method b* V_{PR} = 1.6 x V_{IORM}, 100% Production Test with tp = 1 sec, Partial Discharge < 5 pC	V_{PR}	2263	V_{PEAK}
		1600	V_{RMS}
Input to Output Test Voltage, Method a* V_{PR} = 1.2 x V_{IORM}, Type and sample test, tp = 60 sec, Partial Discharge < 5 pC	V_{PR}	1697	V_{PEAK}
		1200	V_{RMS}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	8000	V_{PEAK}
Safety-Limiting Values (Maximum values allowed in the event of a failure, also see Figure 9) Case Temperature Current (Input Current I_F, P_{SI} = 0) Output Power (obtained by setting pin 8 = 5.5 V, pins 7, 6, 5 = ground)	 T_{SI} I_{SI} $P_{SI, OUTPUT}$	 150 400 700	 °C mA mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V V_{IO} = 500 V	R_{IS}	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the HP Optoelectronics Designer's Catalog, under Product Safety Regulations Section, (VDE 0884) for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in the application.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Clearance (External Air Gap)	L(IO1)	9.6	mm	Measured from input terminals to output terminals
Min. External Creepage (External Tracking Path)	L(IO2)	10.0	mm	Measured from input terminals to output terminals
Min. Internal Clearance (Internal Plastic Gap)		1.0	mm	Through insulation distance conductor to conductor
Min. Internal Creepage (Internal Tracking Path)		4.0	mm	Measured from input terminals to output terminals
Comparative Tracking Index	CTI	200	volts	DIN IEC 112/VDE 0303 PART 1
Isolation Group (per DIN VDE 0109)		IIIa		Material group (DIN VDE 0109)

Electrical Specifications

Over Recommended Temperature (T_A = 0°C to 70°C) unless otherwise specified. (See note 8.)

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	CNW135	7	18	150	%	T_A = 25°C, V_O = 0.4 V, I_F = 16 mA, V_{CC} = 4.5 V	1, 2, 4	1
			5				V_O = 0.5 V, I_F = 16 mA, V_{CC} = 4.5 V		
		CNW136 CNW4502 CNW4503	19	50	150	%	T_A = 25°C, V_O = 0.4 V, I_F = 16 mA, V_{CC} = 4.5 V		
			15				V_O = 0.5 V, I_F = 16 mA, V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}	CNW135		0.1	0.4	V	T_A = 25°C, I_O = 1.1 mA, I_F = 16 mA, V_{CC} = 4.5 V		
					0.5		I_O = 0.8 mA, I_F = 16 mA, V_{CC} = 4.5 V		
		CNW136 CNW4502 CNW4503		0.1	0.4	V	T_A = 25°C, I_O = 3.0 mA, I_F = 16 mA, V_{CC} = 4.5 V		
					0.5		I_O = 2.4 mA, I_F = 16 mA, V_{CC} = 4.5 V		
Logic High Output Current	I_{OH}			0.002	0.5	µA	T_A = 25°C, V_O = V_{CC} = 5.5 V, I_F = 0 mA	6	
					1		T_A = 25°C, V_O = V_{CC} = 15 V, I_F = 0 mA		
					50				
Logic Low Supply Current	I_{CCL}			70	200	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V		
Logic High Supply Current	I_{CCH}				1	µA	T_A = 25°C, I_F = 0 mA, V_O = Open, V_{CC} = 15 V		
					2				
Input Forward Voltage	V_F		1.45	1.68	1.85	V	T_A = 25°C, I_F = 16 mA	3	
			1.35		1.95				
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA, T_A = 25°C		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			1.9		mV/°C	I_F = 16 mA		
Input Capacitance	C_{IN}			90		pF	f = 1 MHz, V_F = 0 V		
Input-Output Insulation Voltage	V_{ISO}		5000			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C		2, 7
Resistance (Input-Output)	R_{I-O}		10^{12}	10^{13}		Ω	T_A = 25°C, V_{I-O} = 500 VDC		2
			10^{11}				T_A = 100°C, V_{I-O} = 500 VDC		
Capacitance (Input-Output)	C_{I-O}			0.5	0.6	pF	f = 1 MHz		2
Transistor DC Current Gain	h_{FE}			180			V_O = 5 V, I_O = 3 mA		
				160			V_O = 0.4 V, I_B = 40 µA		

*All typicals at T_A = 25°C.

Switching Specifications

Over Recommended Temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA, unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	CNW135		0.2	1.5	µs	T_A = 25°C	R_L = 4.1 kΩ	5, 8, 11	4, 5
					2.0					
		CNW136 CNW4502		0.2	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Propagation Delay Time to Logic High at Output	t_{PLH}	CNW135		0.6	1.5	µs	T_A = 25°C	R_L = 4.1 kΩ	5, 8, 11	4, 5
					2.0					
		CNW136 CNW4502		0.35	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	CNW135	1,000			V/µs	R_L = 4.1 kΩ	I_F = 0 mA, T_A = 25°C, V_{CM} = 10 V	12	3, 4, 5
		CNW136	1,000				R_L = 1.9 kΩ			
		CNW4502	1,000	≥10,000			V_{CM} = 10 V	I_F = 0 mA, T_A = 25°C, R_L = 1.9 kΩ	12	3, 4
		CNW4503	15,000	30,000			V_{CM} = 1500 V			
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	CNW135	1,000			V/µs	R_L = 4.1 kΩ	I_F = 16 mA, T_A = 25°C, V_{CM} = 10 V	12	3, 4, 5
		CNW136	1,000				R_L = 1.9 kΩ			
		CNW4502	1,000	10,000			V_{CM} = 10 V	I_F = 16 mA, T_A = 25°C, R_L = 1.9 kΩ	12	3, 4
		CNW4503	15,000	30,000			V_{CM} = 1500 V			
Bandwidth	BW	CNW135 CNW136		11		MHz	See Test Circuit		7, 10	6

*All typicals are at T_A = 25°C.

Notes:

1. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
2. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
3. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e. V_O > 2.0 V) Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM} dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e. V_O > 0.8 V).
4. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
5. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull-up resistor.
6. The frequency at which the ac output voltage is 3 dB below the low frequency asymptote.
7. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage of ≥ 6000 Vrms for one second (leakage detection current limit, I_{I-O} ≤ 5 µA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Characteristics Table.
8. Use of a 0.1 µf bypass capacitor connected between pins 5 and 8 is recommended for operation.

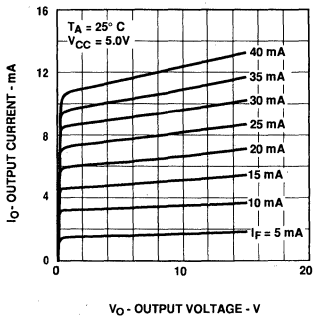


Figure 1. DC and Pulsed Transfer Characteristics.

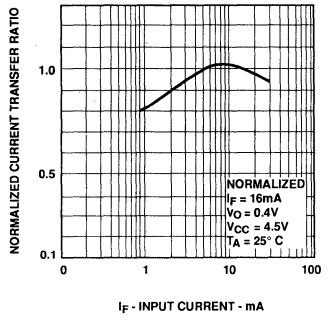


Figure 2. Current Transfer Ratio vs. Input Current

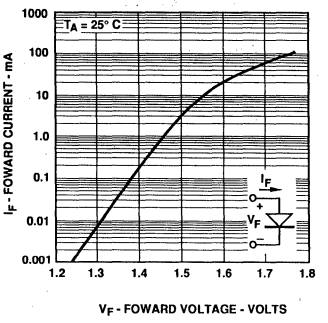


Figure 3. Input Current vs. Forward Voltage.

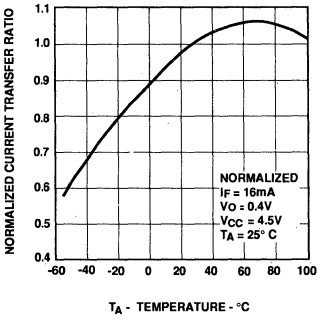


Figure 4. Current Transfer Ratio vs. Temperature.

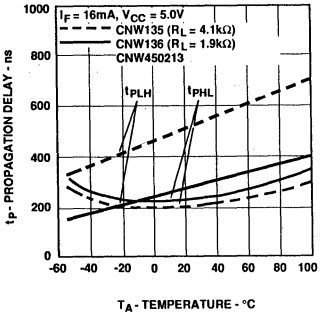


Figure 5. Propagation Delay vs. Temperature.

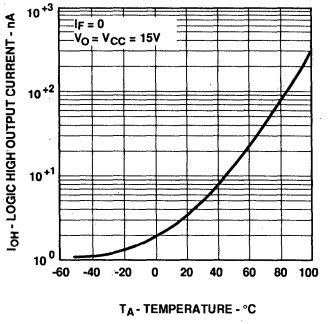


Figure 6. Logic High Output Current vs. Temperature.

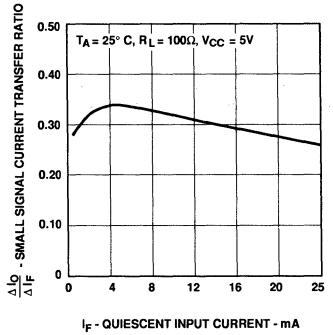


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.

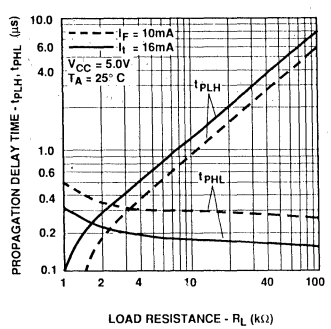


Figure 8. Propagation Delay Time vs. Load Resistance.

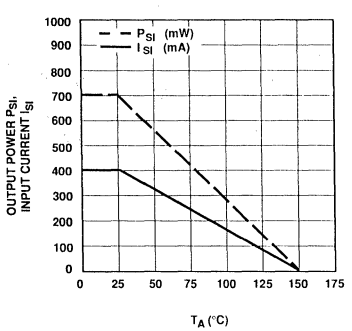


Figure 9. Dependence of Safety Maximum Ratings with Ambient Temperature.

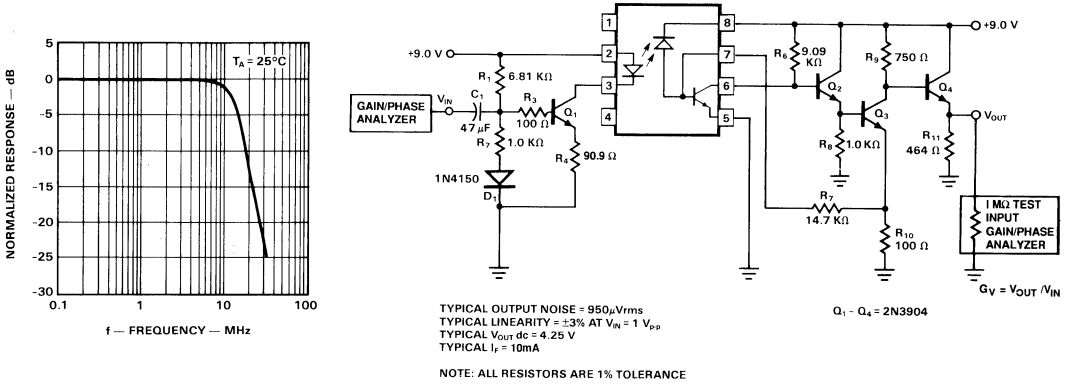


Figure 10. Frequency Response. (CNW135/6)

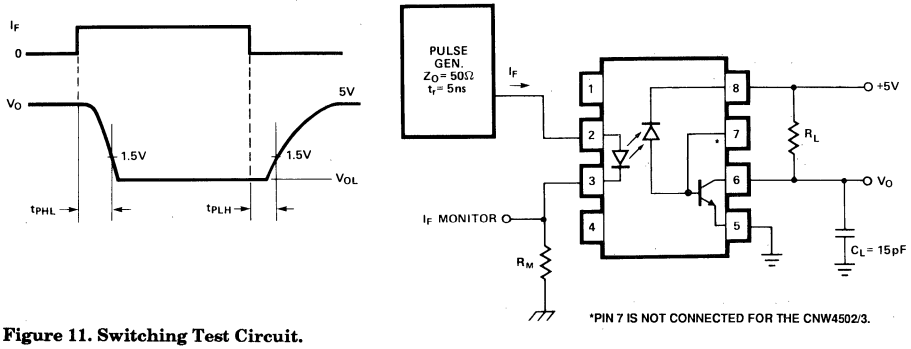


Figure 11. Switching Test Circuit.

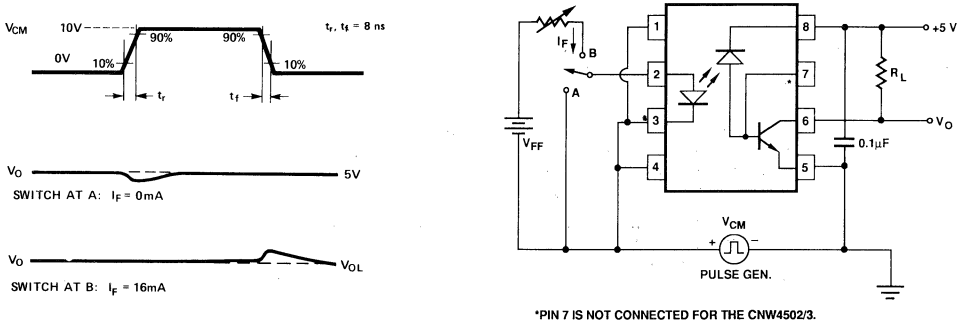
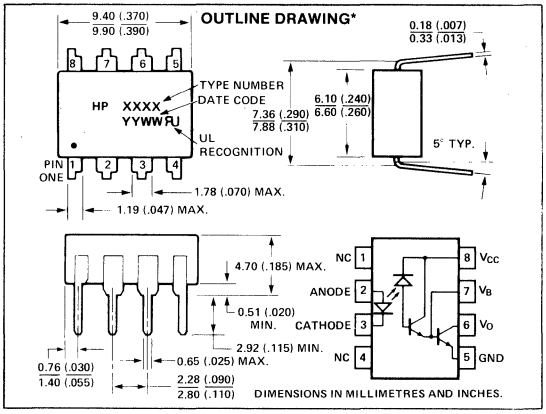


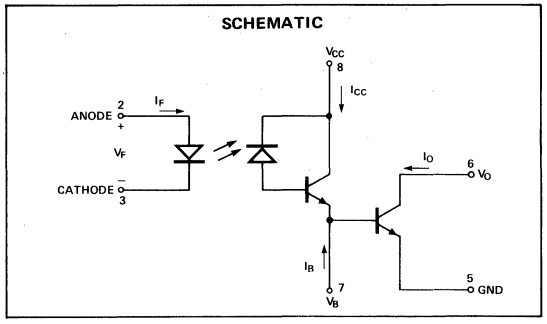
Figure 12. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

6N138
6N139





Features

- **HIGH CURRENT TRANSFER RATIO — 2000% TYPICAL**
- **LOW INPUT CURRENT REQUIREMENT — 0.5 mA**
- **TTL COMPATIBLE OUTPUT — 0.1 V V_{OL} TYPICAL**
- **PERFORMANCE GUARANTEED OVER TEMPERATURE 0°C TO 70°C**
  BASE ACCESS ALLOWS GAIN BANDWIDTH ADJUSTMENT
- **HIGH OUTPUT CURRENT — 60 mA**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE AND 5000 Vac, 1 MINUTE (OPTION 020)**
- **CSA APPROVED**
- **MIL-STD-1772 VERSION AVAILABLE (HCPL-5700/1)**

Description

These high gain series couplers use a Light Emitting Diode and an integrated high gain photo detector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

The 6N139 is for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70°C operating range for only 0.5 mA of LED current.

The 6N138 is designed for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70°C for an LED current of 1.6 mA [1 TTL Unit load (U.L.)]. A 300% minimum CTR enables operation with 1 U.L. out with a 2.2 kΩ pull-up resistor.

Selection for lower input current down to 250 μA is available upon request.

Applications

- Ground Isolate Most Logic Families – TTL/TTL, CMOS/TTL, CMOS/CMOS, LSTTL/TTL, CMOS/LSTTL
- Low Input Current Line Receiver – Long Line or Party line
- EIA RS-232C Line Receiver
- Telephone Ring Detector
- 117 V ac Line Voltage Status Indicator – Low Input Power Dissipation
- Low Power Systems – Ground Isolation

Absolute Maximum Ratings*

(No Derating Required up to 85°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature** ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10s
(1.6 mm below seating plane)
Average Input Current — I_F ..... 20 mA
Peak Input Current — I_F ..... 40 mA
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — I_F ..... 1.0 A
(≤1 μs pulse width, 300 pps)
Reverse Input Voltage — V_R ..... 5 V
Input Power Dissipation ..... 35 mW
Output Current — I_O (Pin 6) ..... 60 mA
Emitter-Base Reverse Voltage (Pin 5-7) ..... 0.5 V
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 6-5)
6N138 ..... -0.5 to 7 V
6N139 ..... -0.5 to 18 V
Output Power Dissipation ..... 100 mW

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

*JEDEC Registered Data.
**0° to 70° on JEDEC Registration.

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C), unless otherwise specified. (See note 7.)

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	6N139	400* 500*	2000 1600	3500 2600	%	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V	2, 3	1, 2, 4
		6N138	300*	1600	2600	%	I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}	6N139		0.1 0.1 0.2	0.4 0.4 0.4	V	I_F = 1.6 mA, I_O = 8 mA, V_{CC} = 4.5 V I_F = 5 mA, I_O = 15 mA, V_{CC} = 4.5 V I_F = 12 mA, I_O = 24 mA, V_{CC} = 4.5 V	1	2
		6N138		0.1	0.4	V	I_F = 1.6 mA, I_O = 4.8 mA, V_{CC} = 4.5 V		
Logic High Output Current	I_{OH}	6N139		0.05	100	μA	I_F = 0 mA, V_O = V_{CC} = 18 V		2, 4
		6N138		0.1	250	μA	I_F = 0 mA, V_O = V_{CC} = 7 V		
Logic Low Supply Current	I_{CCL}			0.4	1.5	mA	I_F = 1.6 mA, V_O = Open, V_{CC} = 18 V		2
Logic High Supply Current	I_{CCH}			0.01	10	μA	I_F = 0 mA, V_O = Open, V_{CC} = 18 V		2
Input Forward Voltage	V_F			1.4	1.7* 1.75	V	T_A = 25°C, I_F = 1.6 mA	4	
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10 μA		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.6 mA		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		
Input-Output Insulation	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C		3, 8
Option 020	V_{ISO}		5000						
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 VDC		3
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		3

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	6N139		5	25*	μs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 6, 7	2, 4
					30				
				0.2	1*		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω		
					2				
		6N138		1.6	10*		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ		
					15				
Propagation Delay Time to Logic High at Output	t_{PLH}	6N139		18	60*	μs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 6, 7	2, 4
					90				
				2	7*		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω		
					10				
		6N138		10	35*		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ		
					50				
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$		1000	10,000		V/μs	I_F = 0 mA, T_A = 25°C, R_L = 2.2 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}	8	5, 6
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$		1000	10,000		V/μs	I_F = 1.6 mA, T_A = 25°C, R_L = 2.2 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}	8	5, 6

*JEDEC registered data.
**All typicals at T_A = 25°C and V_{CC} = 5 V, unless otherwise noted.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min.External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

1. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
2. Pin 7 Open.
3. Device considered a two-terminal device. Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
4. Use of a resistor between pin 5 and 7 will decrease gain and delay time. Significant reduction in overall gain can occur when using resistor values below 47 kΩ. For more information, please contact your local HP Components representative.
5. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse. V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e. $V_O < 0.8$ V).
6. In applications where dV/dt may exceed 50,000 V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from desctructively high surge currents. The recommended value is $R_{CC} = 220\ \Omega$.
7. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ μA).

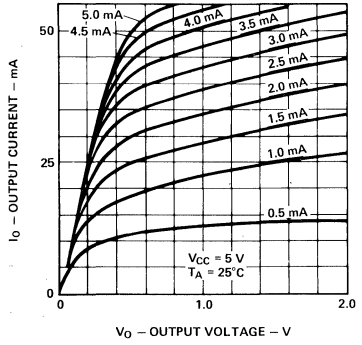


Figure 1. 6N138/6N139 DC Transfer Characteristics

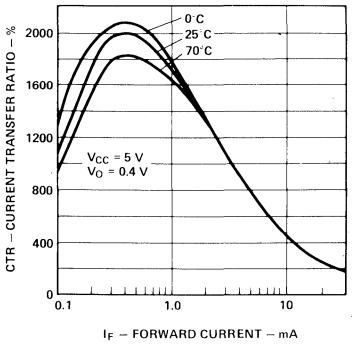


Figure 2. Current Transfer Ratio vs Forward Current 6N138/6N139

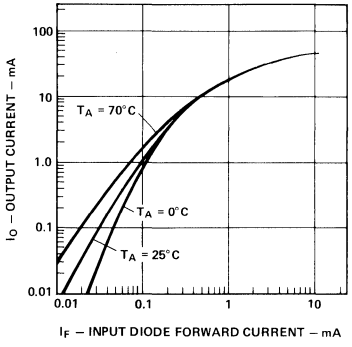


Figure 3. 6N138/6N139 Output Current vs Input Diode Forward Current

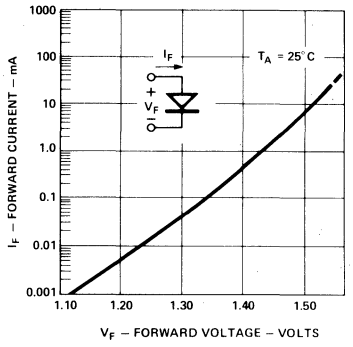


Figure 4. Input Diode Forward Current vs. Forward Voltage.

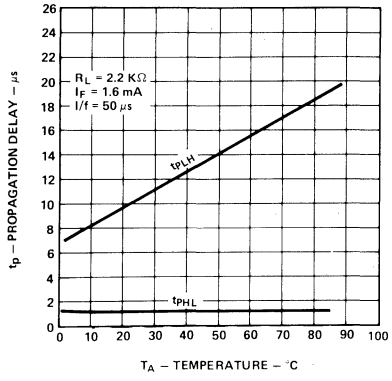


Figure 5. Propagation Delay vs. Temperature.

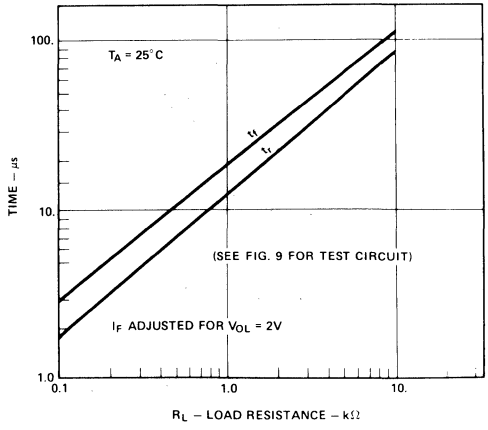


Figure 6. Non Saturated Rise and Fall Times vs. Load Resistance.

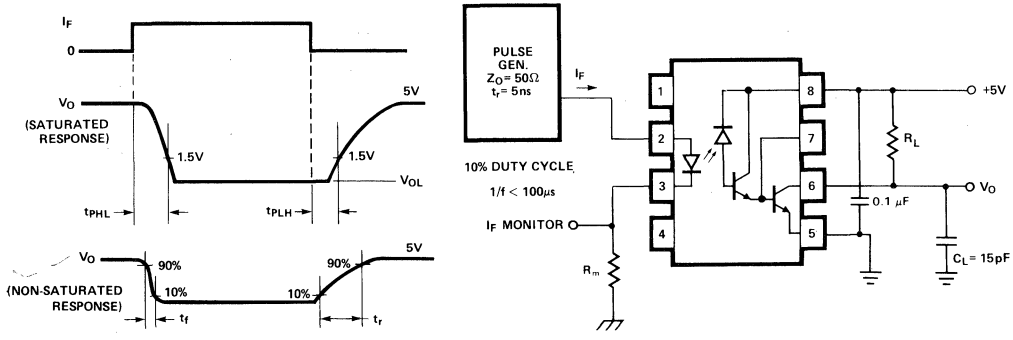


Figure 7. Switching Test Circuit.*

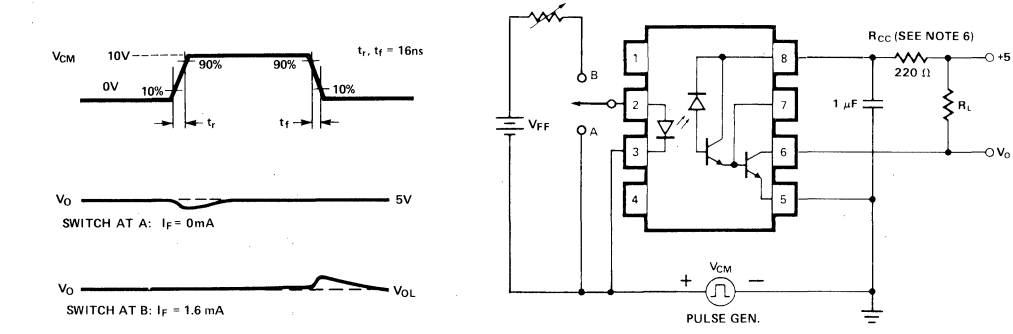


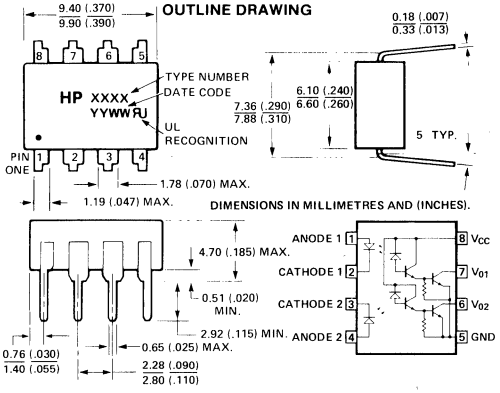
Figure 8. Test Circuit for Transient Immunity and Typical Waveforms.

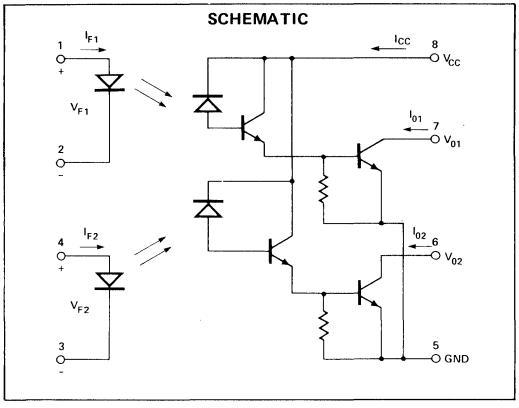
*JEDEC Registered Data.

HEWLETT PACKARD

DUAL LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

HCPL-2730
HCPL-2731





Features

- **HIGH CURRENT TRANSFER RATIO – 1800% TYPICAL**
- **LOW INPUT CURRENT REQUIREMENT – 0.5 mA**
- **LOW OUTPUT SATURATION VOLTAGE – 0.1 V TYPICAL**
- **HIGH DENSITY PACKAGING**
- **PERFORMANCE GUARANTEED OVER 0°C TO 70°C TEMPERATURE RANGE**
- **LSTTL COMPATIBLE**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE No. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE AND 5000 Vac 1 MINUTE (OPTION 020) PENDING APPROVAL**
- **CSA APPROVED UNDER COMPONENT ACCEPTANCE NOTICE NO. 5 (FILE NO. LR 88324)**
- **MIL-STD VERSION AVAILABLE (HCPL-5730/1)**

Applications

- **Digital Logic Ground Isolation**
- **Telephone Ring Detector**
- **EIA RS-232C Line Receiver**
- **Low Input Current Line Receiver — Long Line or Party Line**
- **Microprocessor Bus Isolation**
- **Current Loop Receiver**
- **Polarity Sensing**
- **Level Shifting**
- **Line Voltage Status Indicator — Low input Power Dissipation**

Description

The HCPL-2730/31 dual channel couplers contain a separated pair of GaAsP light emitting diodes optically coupled to a pair of integrated high gain photo detectors. They provide extremely high current transfer ratio and excellent input-output common mode transient immunity. A separate pin for the photodiodes and first gain stages (V_{CC}) permits lower output saturation voltage and higher speed operation than possible with conventional photodarlington type optocouplers. In addition V_{CC} may be as low as 1.6 V without adversely affecting the parametric performance.

Guaranted operation at low input currents and the high current transfer ratio (CTR) reduce the magnitude and effects of CTR degradation.

The outstanding high temperature performance of this split Darlington type output amplifier results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground.

The HCPL-2731 has a 400% minimum CTR at an input current of only 0.5 mA making it ideal for use in low input current application such as MOS, CMOS and low power logic interfacing or RS232C data transmission systems. In addition, the high CTR and high output current capability make this device extremely useful in applications where a high fanout is required. Compatibility with high voltage CMOS logic systems is guaranteed by the 18V V_{CC} and V_O specifications and by testing output high leakage (I_{OH}) at 18V.

The HCPL-2730 is specified at an input current of 1.6 mA and has a 7 V V_{CC} and V_O rating. The 300% minimum CTR allows TTL to TTL interfacing at this input current.

Important specifications such as CTR, leakage current and output saturation voltage are guaranteed over the 0°C to 70°C temperature range to allow trouble-free system operation. Selection for lower input current down to 250 μA is available upon request.

OPTO COUPLERS

Electrical Specifications

(Over recommended temperature T_A = 0°C to 70°C, unless otherwise specified.) See note 12.

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	2731	400 500	1800 1600	3500 2600	%	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V	2, 3	6, 7
		2730	300	1600	2600	%	I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}	2731		0.1 0.1 0.2	0.4 0.4 0.4	V	I_F = 1.6 mA, I_O = 8 mA, V_{CC} = 4.5 V I_F = 5 mA, I_O = 15 mA, V_{CC} = 4.5 V I_F = 12 mA, I_O = 24 mA, V_{CC} = 4.5 V	1	6
		2730		0.1	0.4	V	I_F = 1.6 mA, I_O = 4.8 mA, V_{CC} = 4.5 V		
Logic High Output Current	I_{OH}	2731		0.005	100	μA	I_F = 0 mA, V_O = V_{CC} = 18 V		6
		2730		0.01	250	μA	I_F = 0 mA, V_O = V_{CC} = 7 V		
Logic Low Supply Current	I_{CCL}	2731		1.2	3	mA	V_{CC} = 18 V; I_{F1} = I_{F2} = 1.6 mA; V_{O1} = V_{O2} = Open	5	
		2730		0.9			V_{CC} = 7 V		
Logic High Supply Current	I_{CCH}	2731		0.005	20	μA	V_{CC} = 18 V; I_{F1} = I_{F2} = 0 mA; V_{O1} = V_{O2} = Open	5	
		2730		0.004			V_{CC} = 7 V		
Input Forward Voltage	V_F			1.4	1.7 1.75	V	T_A = 25°C; I_F = 1.6 mA	4	6
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 μA		6
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.6 mA		6
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		6
Input-Output Insulation	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C		8, 13
OPT 020 (PENDING)	V_{ISO}		5000						8, 14
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 VDC		8
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		8
Input-Input Insulation Leakage Current	I_{I-I}			0.005		μA	45% Relative Humidity, t = 5 s, V_{I-I} = 500 VDC		9
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω	V_{I-I} = 500 VDC		9
Capacitance (Input-Input)	C_{I-I}			0.25		pF	f = 1 MHz		9

*All typicals at T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	2731		25	100	μs	T_A = 25°C	I_F = 0.5 mA, R_L = 4.7 kΩ	6, 7, 8, 9	6
					120					
		2730/1		5	20		T_A = 25°C	I_F = 1.6 mA, R_L = 2.2 kΩ		
					25					
				0.5	2		T_A = 25°C	I_F = 12 mA, R_L = 270 Ω		
					3					
Propagation Delay Time to Logic High at Output	t_{PLH}	2731		10	60	μs	T_A = 25°C	I_F = 0.5 mA, R_L = 4.7 kΩ	7, 8, 9	6
					90					
		2730/1		10	35		T_A = 25°C	I_F = 1.6 mA, R_L = 2.2 kΩ		
					50					
				1	10		T_A = 25°C	I_F = 12 mA, R_L = 270 Ω		
					15					
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$		1000	10,000		V/μs	I_F = 0 mA, R_L = 2.2 kΩ $\|V_{CM}\|$ = 10 V_{P-P} T_A = 25°C		10	6, 10, 11
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$		1000	10,000		V/μs	I_F = 1.6 mA, R_L = 2.2 kΩ $\|V_{CM}\|$ = 10 V_{P-P} T_A = 25°C		10	6, 10, 11

*All typicals at 25°C

NOTES:

1. Derate linearly above 50° C free-air temperature at a rate of 0.5 mA/° C.
2. Derate linearly above 50° C free-air temperature at a rate of 0.9 mW/° C.
3. Derate linearly above 35° C free-air temperature at a rate of 0.6 mA/° C.
4. Pin 5 should be the most negative voltage at the detector side.
5. Derate linearly above 35° C free-air temperature at a rate of 1.7 mW/° C. Output power is collector output power plus supply power.
6. Each channel.
7. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
8. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
9. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
10. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM} dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
11. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is R_{CC} = 110 Ω.
12. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
13. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ μA).
14. **In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ μA).**

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 sec
(1.6mm below seating plane)
Average Input Current — I_F
(each channel) ..... 20 mA[1]
Peak Input Current — I_F
(each channel) ..... 40 mA
(50% duty cycle, 1 ms pulse width)
Reverse Input Voltage — V_R
(each channel) 5V
Input Power Dissipation
(each channel) ..... 35 mW[2]
Output Current — I_O
(each channel) ..... 60 mA[3]
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 7,6-5)[4]
HCPL-2730 ..... -0.5 to 7V
HCPL-2731 ..... -0.5 to 18V
Output Power Dissipation
(each channel) ..... 100 mW[5]

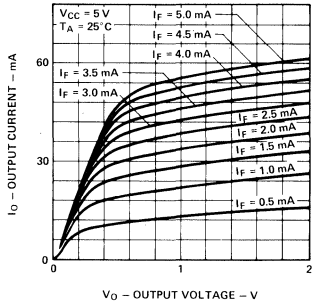


Figure 1. DC Transfer Characteristics (HCPL-2730/HCPL-2731)

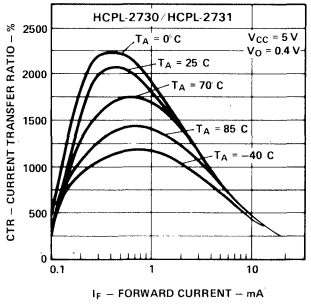


Figure 2. Current Transfer Ratio vs. Forward Current

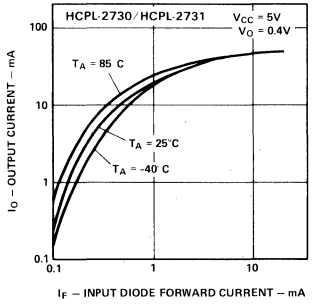


Figure 3. Output Current vs. Input Diode Forward Current

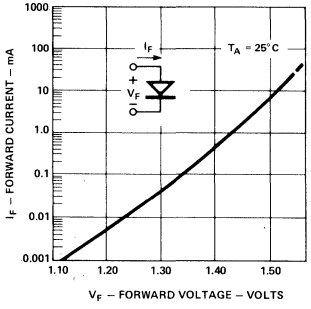


Figure 4. Input Diode Forward Current vs. Forward Voltage.

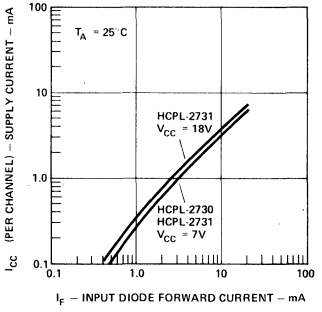


Figure 5. Supply Current Per Channel vs. Input Diode Forward Current.

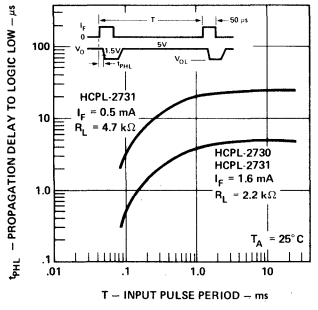


Figure 6. Propagation Delay To Logic Low vs. Pulse Period.

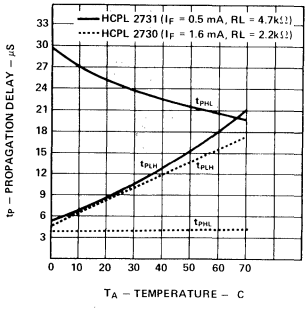


Figure 7. Propagation Delay vs. Temperature.

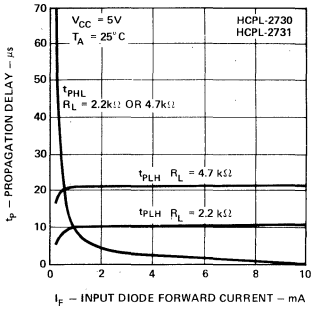


Figure 8. Propagation Delay vs. Input Diode Forward Current.

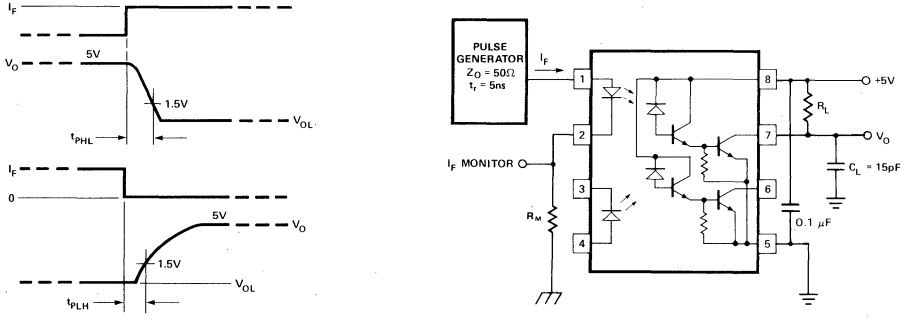


Figure 9. Switching Test Circuit.

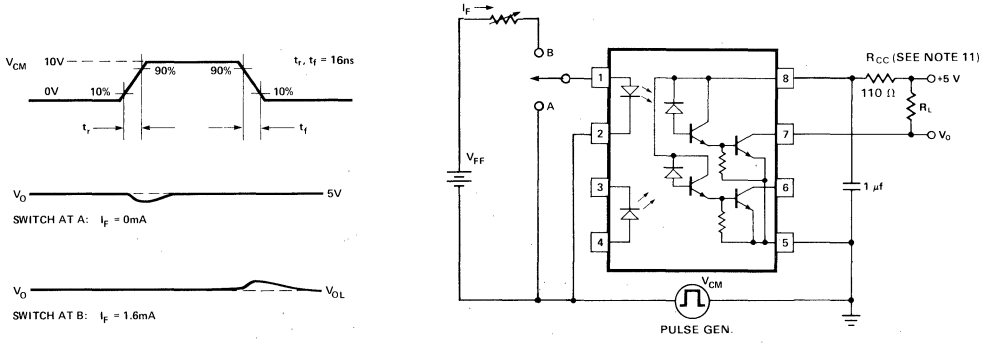


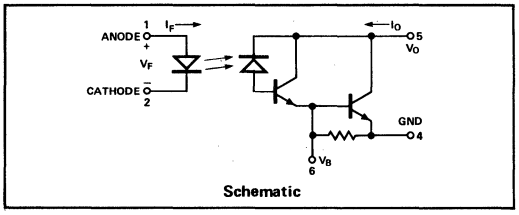
Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

OPTO COUPLERS

HEWLETT PACKARD

LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLER

4N45
4N46



Schematic

Features

- **HIGH CURRENT TRANSFER RATIO — 1500% TYPICAL**
- **LOW INPUT CURRENT REQUIREMENT — 0.5 mA**
- **PERFORMANCE GUARANTEED OVER 0°C to 70°C TEMPERATURE RANGE**
- **INTERNAL BASE-EMITTER RESISTOR MINIMIZES OUTPUT LEAKAGE**
- **GAIN-BANDWIDTH ADJUSTMENT PIN**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **CSA APPROVED**

Description

The 4N45/46 optocouplers contain a GaAsP light emitting diode optically coupled to a high gain photodetector IC.

The excellent performance over temperature results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground. External access to the second stage base provides better noise rejection than a conventional photodarlington detector. An external resistor or capacitor at the base can be added to make a gain-bandwidth or input current threshold adjustment. The base lead can also be used for feedback.

The high current transfer ratio at very low input currents permits circuit designs in which adequate margin can be allowed for the effects of CTR degradation over time.

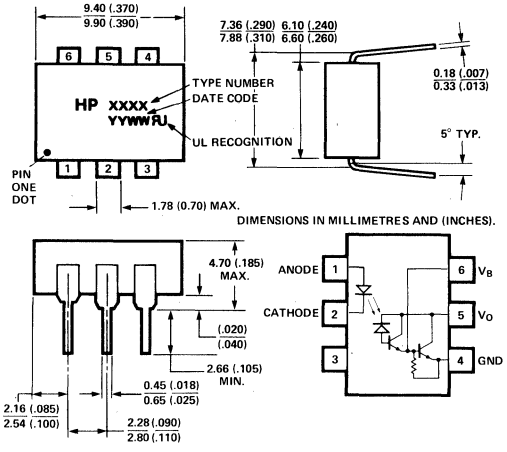
The 4N46 has a 350% minimum CTR at an input current of only 0.5mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing. Compatibility with high voltage CMOS logic systems is assured by the 20V minimum breakdown voltage of the output transistor and by the guaranteed maximum output leakage (I_{OH}) at 18V.

The 4N45 has a 250% minimum CTR at 1.0mA input current and a 7V minimum breakdown voltage rating.

Selection for lower input current down to 250 μA is available upon request.

*JEDEC Registered Data. **JEDEC Registered up to 70°C

OUTLINE DRAWING*



DIMENSIONS IN MILLIMETRES AND (INCHES).

Applications

- **Telephone Ring Detector**
- **Digital Logic Ground Isolation**
- **Low Input Current Line Receiver**
- **Line Voltage Status Indicator — Low Input Power Dissipation**
- **Logic to Reed Relay Interface**
- **Level Shifting**
- **Interface Between Logic Families**

Absolute Maximum Ratings*

Storage Temperature ..... -55°C to +125°C
Operating Temperature** ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 s.
(1.6mm below seating plane)
Average Input Current — I_F ..... 20 mA[1]
Peak Input Current — I_F ..... 40 mA
(50% duty cycle, 1ms pulse width)
Peak Transient Input Current — I_F 1.0A
(≤1 μs pulse width, 300pps)
Reverse Input Voltage — V_R 5V
Input Power Dissipation ..... 35mW[2]
Output Current — I_O (Pin 5) ..... 60 mA[3]
Emitter-Base Reverse Voltage (Pins 4-6) 0.5V
Output Voltage — V_O (Pin 5-4)
4N45 ..... -0.5 to 7V
4N46 ..... -0.5 to 20V
Output Power Dissipation ..... 100mW[4]

See notes, following page

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C), unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	4N46	350* 500* 200*	1500 1500 600	3200 2000 1000	%	I_F = 0.5 mA, V_O = 1.0 V I_F = 1.0 mA, V_O = 1.0 V I_F = 10 mA, V_O = 1.2 V	3, 4 10, 11	5, 6, 8
		4N45	250* 200*	1200 500	2000 1000	%	I_F = 1.0 mA, V_O = 1.0 V I_F = 10 mA, V_O = 1.2 V		
Logic Low Output Voltage	V_{OL}	4N46		0.90 0.92 0.95	1.0 1.0 1.2	V	I_F = 0.5 mA, I_{OL} = 1.75 mA I_F = 1.0 mA, I_{OL} = 5.0 mA I_F = 10 mA, I_{OL} = 20 mA	2	6
		4N45		0.90 0.95	1.0 1.2	V	I_F = 1.0 mA, I_{OL} = 2.5 mA I_F = 10 mA, I_{OL} = 20 mA		
Logic High Output Current	I_{OH}*	4N46		0.001	100	μA	I_F = 0 mA, V_O = 18 V		6,8
		4N45		0.001	250	μA	I_F = 0 mA, V_O = 5 V		
Input Forward Voltage	V_F			1.4	1.7* 1.75	V	T_A = 25°C, I_F = 1.0 mA	1	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.0 mA		
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10 μA		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		
Input-Output Insulation	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C		7, 10
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 VDC		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		7

Switching Specifications

(Over recommended temperature T_A = 0°C to 70°C unless otherwise specified.) V_{CC} = 5.0 V.

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		80		μs	T_A = 25°C, I_F = 0.5 mA, R_L = 10 kΩ	5, 6 7, 8 10, 12	6
	t_{PHL}		5	50*		T_A = 25°C, I_F = 10 mA, R_L = 2.2 kΩ		8
				60				
Propagation Delay Time to Logic High at Output	t_{PLH}		1500		μs	T_A = 25°C, I_F = 10 mA, R_L = 10 kΩ	5, 6 7, 8 10, 12	6
	t_{PLH}		150	500*		T_A = 25°C, I_F = 10 mA, R_L = 220 kΩ		8
				600				
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$		500		V/μs	I_F = 0 mA, R_L = 10 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}	9	9
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$		500		V/μs	I_F = 1.0 mA, R_L = 10 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}	9	9

*JEDEC Registered Data.

**All typicals at T_A = 25°C, unless otherwise noted.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

NOTES:

1. Derate linearly above 50° C free-air temperature at a rate of 0.4mA/° C.
2. Derate linearly above 50° C free-air temperature at a rate of 0.7mW/° C.
3. Derate linearly above 25° C free-air temperature at a rate of 0.8mA/° C.
4. Derate linearly above 25° C free-air temperature at a rate of 1.5mW/° C.
5. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Pin 6 Open.
7. Device considered a two-terminal device: Pins 1, 2, 3 shorted together and Pins 4, 5, and 6 shorted together.
8. Use of a resistor between pin 4 and 6 will decrease gain and delay time. (See Figures 10 and 12).
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.5V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 2.5V$).
10. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{I-O} \leq 5\ \mu A$).

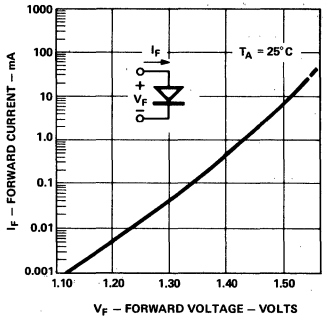


Figure 1. Input Diode Forward Current vs. Forward Voltage.

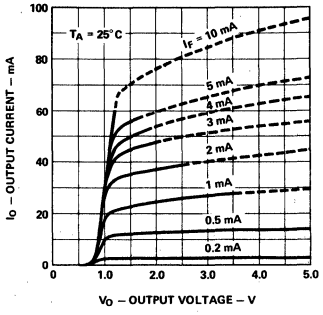


Figure 2. Typical DC Transfer Characteristics.

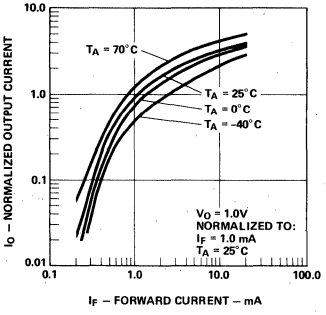


Figure 3. Output Current vs. Input Current.

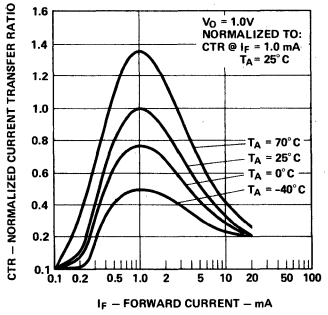


Figure 4. Current Transfer Ratio vs. Input Current.

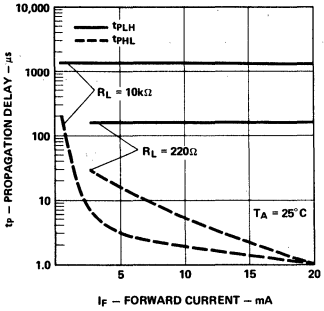


Figure 5. Propagation Delay vs. Forward Current.

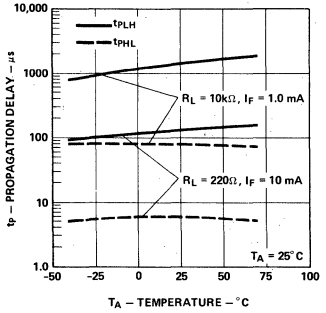


Figure 6. Propagation Delay vs. Temperature.

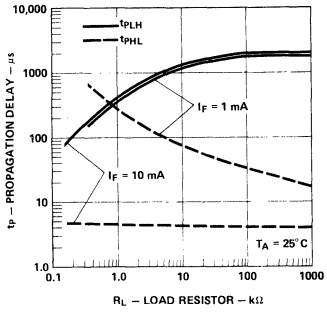


Figure 7. Propagation Delay vs Load Resistor.

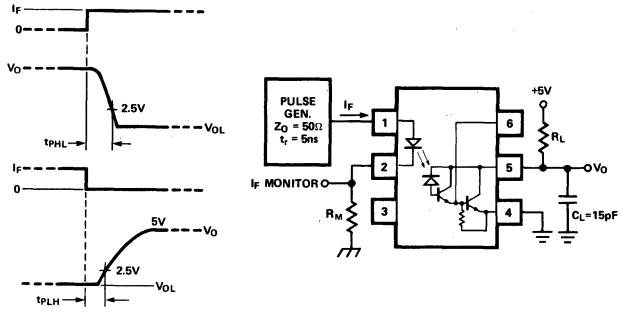


Figure 8. Switching Test Circuit

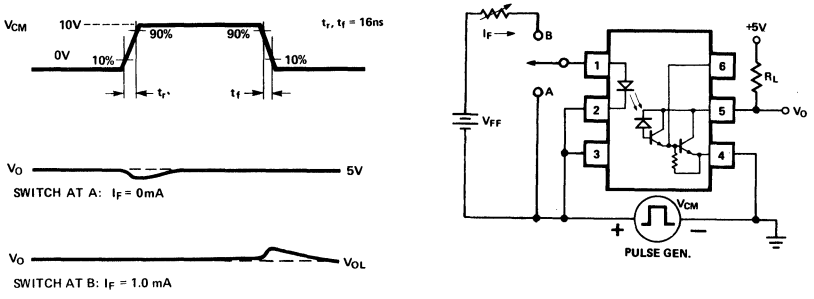


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

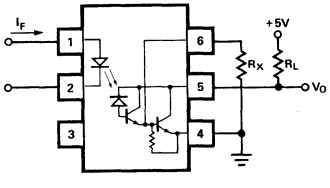


Figure 10. External Base Resistor, R_X

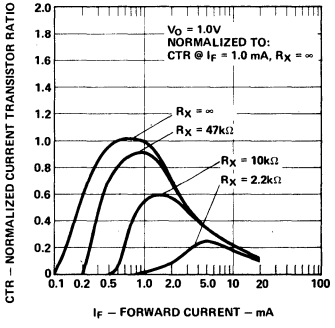


Figure 11. Effect of R_X On Current Transfer Ratio

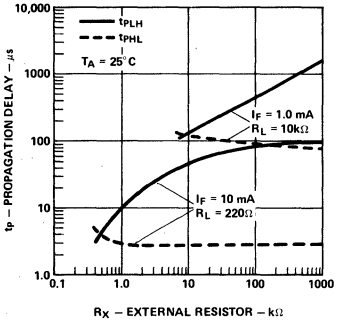
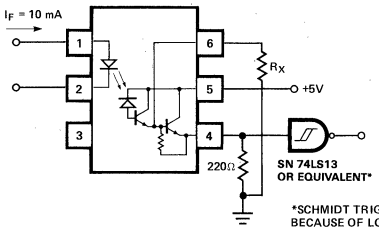


Figure 12. Effect of R_X On Propagation Delay

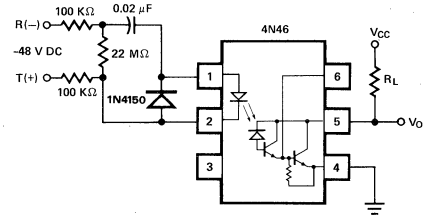
Applications



R_X (kΩ)	t_{PHL} (μs)	t_{PLH} (μs)
∞	5	320
100	5	200
47	5	140
20	6	80
10	6	45

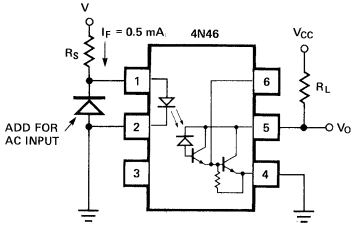
*SCHMIDT TRIGGER RECOMMENDED BECAUSE OF LONG t_r, t_f.

TTL Interface



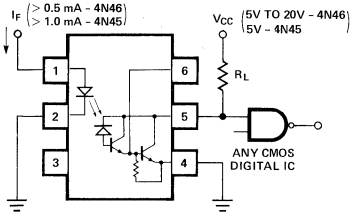
NOTE: AN INTEGRATOR MAY BE REQUIRED AT THE OUTPUT TO ELIMINATE DIALING PULSES AND LINE TRANSIENTS.

Telephone Ring Detector

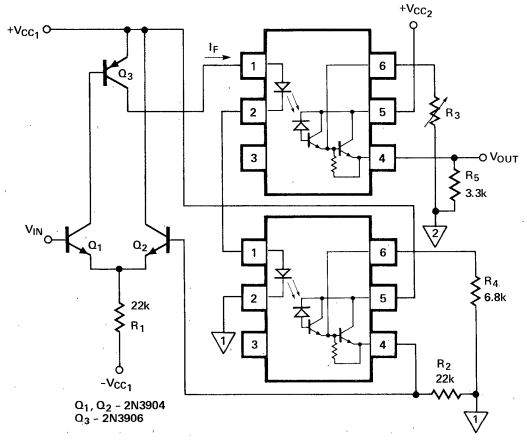


V (Vdc or Vrms)	R_S	V • I_F (mW)
24	47kΩ	11
48	100kΩ	22
115	220kΩ	62
230	470kΩ	113

Line Voltage Monitor



CMOS Interface



Analog Signal Isolation

CHARACTERISTICS

$R_{IN} \approx 30M\Omega$, $R_{OUT} \approx 50\Omega$
$V_{IN\,(MAX.)} = V_{CC_1} - 1V$, LINEARITY BETTER THAN 5%

DESIGN COMMENTS

R_1 - NOT CRITICAL $\left(\ll \frac{V_{IN\,(MAX.)} - (-V_{CC_1}) - V_{BE}}{I_{F\,(MAX.)}}\right) h_{FE}\ Q_3$

R_2 - NOT CRITICAL (OMIT IF 0.2 TO 0.3V OFFSET IS TOLERABLE)

$R_4 > \frac{V_{IN\,(MAX.)} + V_{BE}}{1\ mA}$

$R_5 > \frac{V_{IN\,(MAX.)}}{2.5\ mA}$

NOTE: ADJUST R_3 SO $V_{OUT} = V_{IN}$ AT $V_{IN} = \frac{V_{IN\,(MAX.)}}{2}$

HEWLETT PACKARD

Small Outline Low Input Current, High Gain Optocouplers

Technical Data

HCPL-0700
HCPL-0701

Features

- **Surface Mountable**
- **Industry Standard SOIC-8 Footprint**
- **Compatible With Infrared Vapor Phase Reflow and Wave Soldering Processes**
- **High Current Transfer Ratio – 2000% Typical**
- **Low Input Current Requirement – 0.5 mA**
- **TTL Compatible Output – 0.1 V V_{OL} Typical**
- **Guaranteed ac and dc Performance Over Temperature 0°C to 70°C**
- **Base Access Allows Gain Bandwidth Adjustment**
- **High Output Current – 60 mA**
- **Recognized Under The Component Program Of U.L. (File No. E55361) For Dielectric Withstand Proof Test Voltage Of 2500 VAC, 1 Minute**

Description

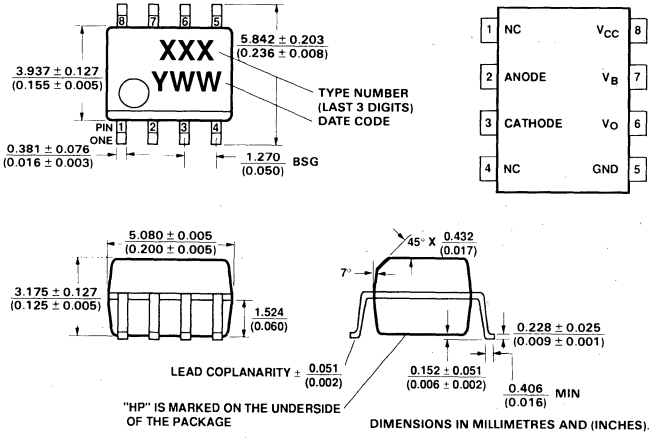
These small outline, low input current, high gain optocouplers are single channel devices in an industry standard SOIC-8 footprint. They are electrically equivalent to the following HP optocouplers:

Small Outline	Standard DIP
HCPL-0700	6N138
HCPL-0701	6N139

The SOIC-8 package does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

These high gain series couplers use a Light Emitting Diode and an integrated high gain photodetector to provide extremely high current transfer

Outline Drawing*



CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

OPTO COUPLERS

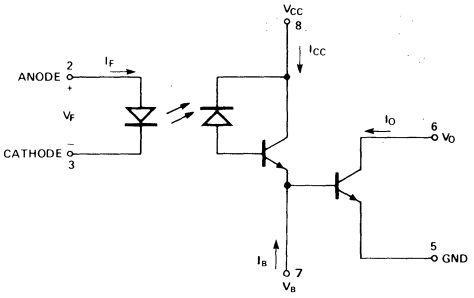
ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

The HCPL-0701 is for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70°C operating range for only 0.5 mA of LED current.

The HCPL-0700 is designed for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70°C for an LED current of 1.6 mA [1 TTL Unit Load (U.L.)]. A 300% minimum CTR enables operation with 1 U.L. out with a 2.2 kΩ pull-up resistor.

Selection for lower input currents down to 250 μA is available upon request.

Schematic



Applications

- **Ground Isolate Most Logic Families – TTL/TTL, CMOS/TTL, CMOS/CMOS, LSTTL/TTL, CMOS/LSTTL**
- **Low Input Current Line Receiver – Long Line or Party Line**
- **EIA RS-232C Line Receiver**
- **Telephone Ring Detector**
- **117 V ac Line Voltage Status Indicator – Low Input Power Dissipation**
- **Low Power Systems – Ground Isolation**

Absolute Maximum Ratings

(No Derating Required Up To 85°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Infrared and Vapor Phase Reflow Temperature ..... 215°C for 90 s
Average Input Current – I_F ..... 20 mA
Peak Input Current – I_F ..... 40 mA
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F ..... 1.0 A
(≤1 μs pulse width, 300 pps)
Reverse Input Voltage – V_R ..... 5 V
Input Power Dissipation ..... 35 mW
Output Current – I_O (Pin 6) ..... 60 mA
Emitter-Base Reverse Voltage (Pin 5-7) ..... 0.5 V
Supply and Output Voltage – V_{CC} (Pin 8-5), V_O (Pin 6-5)
HCPL-0700 ..... -0.5 V to 7 V
HCPL-0701 ..... -0.5 V to 18 V
Output Power Dissipation ..... 100 mW

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C), unless otherwise specified. (See note 7.)

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	HCPL-0701	400 500	2000 1600	3500 2600	%	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V	2, 3	1, 2, 4
		HCPL-0700	300	1600	2600	%	I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}	HCPL-0701		0.1 0.1 0.2	0.4 0.4 0.4	V	I_F = 1.6 mA, I_O = 8 mA, V_{CC} = 4.5 V I_F = 5 mA, I_O = 15 mA, V_{CC} = 4.5 V I_F = 12 mA, I_O = 24 mA, V_{CC} = 4.5 V	1	2
		HCPL-0700		0.1	0.4	V	I_F = 1.6 mA, I_O = 4.8 mA, V_{CC} = 4.5 V		
Logic High Output Current	I_{OH}	HCPL-0701		0.05	100	µA	I_F = 0 mA, V_O = V_{CC} = 18 V		2
		HCPL-0700		0.1	250	µA	I_F = 0 mA, V_O = V_{CC} = 7 V		
Logic Low Supply Current	I_{CCL}			0.4	1.5	mA	I_F = 1.6 mA, V_O = Open, V_{CC} = 18 V		2
Logic High Supply Current	I_{CCH}			0.01	10	µA	I_F = 0 mA, V_O = Open, V_{CC} = 18 V		2
Input Forward Voltage	V_F			1.4	1.7 1.75	V	T_A = 25°C; I_F = 1.6 mA	4	
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.6 mA		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		
Input-Output Insulation	V_{ISO}	2500				V_{RMS}	RH ≤ 50%, t = 1 min.		3, 8
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 V dc		3
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		3

*All typicals are at T_A = 25°C and V_{CC} = 5 V, unless otherwise noted.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	HCPL-0701		5	25	µs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 6, 7	2, 4
					30				
				0.2	1		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω		
					2				
		HCPL-0700		1.6	10		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ		
					15				
Propagation Delay Time to Logic High at Output	t_{PLH}	HCPL-0701		18	60	µs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 6, 7	2, 4
					90				
				2	7		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω		
					10				
		HCPL-0700		10	35		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ		
					50				
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$		1000	10,000		V/µs	I_F = 0 mA, R_L = 2.2 kΩ, $\|V_{CM}\|$ = 10 V_{p-p}	8	5, 6
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$		1000	10,000		V/µs	I_F = 1.6 mA, R_L = 2.2 kΩ, $\|V_{CM}\|$ = 10 V_{p-p}	8	5, 6

*All typicals are at T_A = 25°C.

Notes:

1. DC CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
2. Pin 7 open.
3. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
4. Use of a resistor between pin 5 and 7 will decrease gain and delay time. See Application Note 951-1 for more details.
5. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
6. In applications where dV/dt may exceed 50,000 V/µs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is R_{CC} = 220 Ω.
7. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 is recommended.
8. In accordance with UL 1755, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, I_{i-o} ≤ 5 µA).

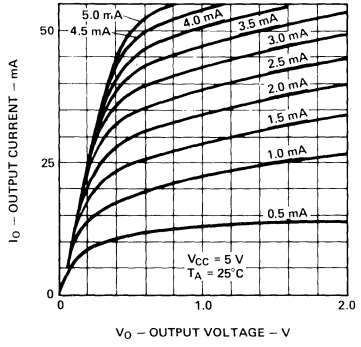


Figure 1. HCPL-0700/0701 DC Transfer Characteristics.

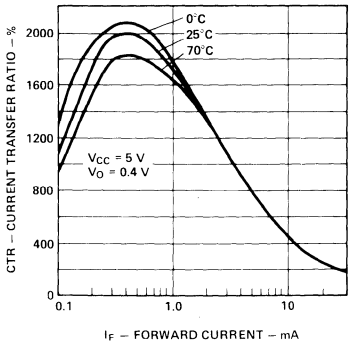


Figure 2. Current Transfer Ratio vs. Forward Current HCPL-0700/0701.

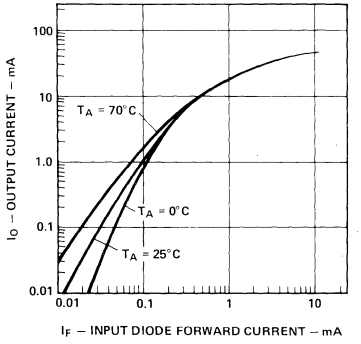


Figure 3. HCPL-0700/0701 Output Current vs. Input Diode Forward Current.

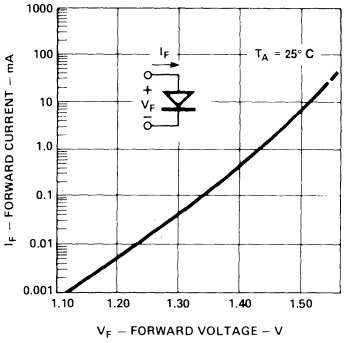


Figure 4. Input Diode Forward Current vs. Forward Voltage.

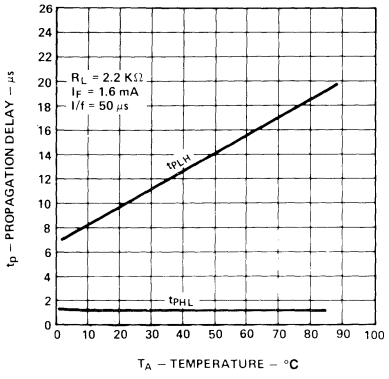


Figure 5. Propagation Delay vs. Temperature.

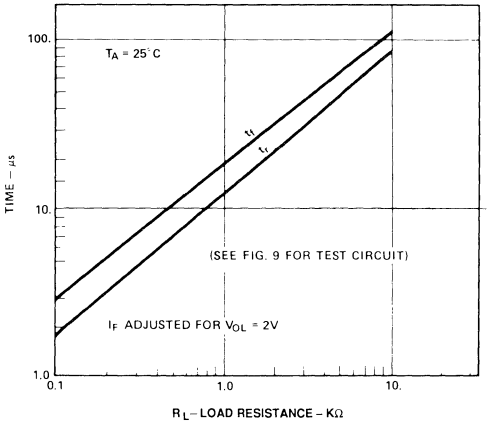


Figure 6. Non-Saturated Rise and Fall Times vs. Load Resistance.

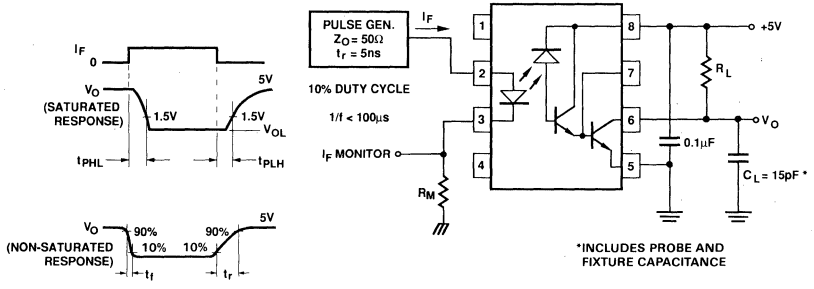


Figure 7. Switching Test Circuit.

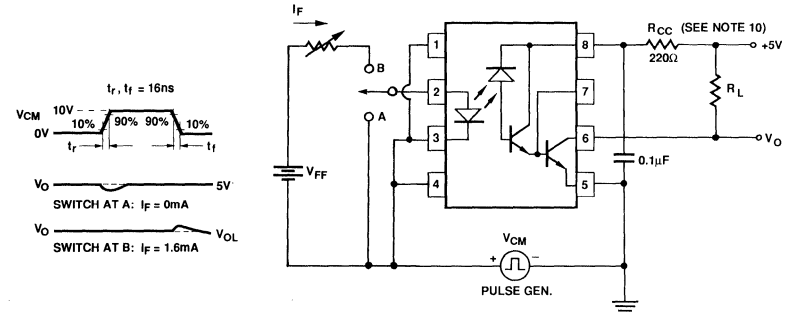


Figure 8. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

Low Input Current, High Gain Optocouplers

Technical Data

CNW138
CNW139

Features

- **5000 Vrms/1 Minute Insulation Withstand Capability**
- **Worldwide Safety Approval**
  UL1577 (File No. E55361)
  VDE 0884 Certification (V_{IORM} = 1 kV_{RMS})
  VDE 860/805/806/804/750-1/ IEC 950
  BSI According to BS 415/ 7002/6301
  SETI-SEMKO-NEMKO-DEMKO-According to IEC 65/380/950/335
- **High Current Transfer Ratio – 3000% Typical**
- **Low Input Current Requirement – 0.5 mA**
- **TTL Compatible Output – 0.1 V V_{OL} Typical**
- **Performance Guaranteed Over Temperature 0°C to 70°C**
- **Base Access Allows Gain Bandwidth Adjustment**
- **High Output Current – 60 mA**
- **Pin Compatible with 6N138/9**

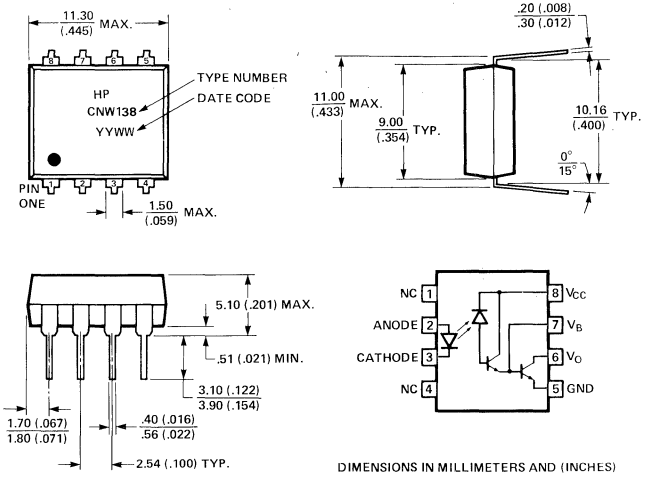
Applications

- **High Voltage Insulation**
- **Low Input Current Line Receiver**
- **Ground Isolation - TTL/ TTL, CMOS/TTL, CMOS/ CMOS, LSTTL/TTL, CMOS/ LSTTL**
- **EIA RS-232C Line Receiver**
- **Telephone Ring Detector**
- **AC Line Voltage Sensing**
- **Low Power Systems**

Description

These high-voltage, high-gain optocouplers use an AlGaAs LED and an integrated high gain photodetector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

Package Outline



DIMENSIONS IN MILLIMETERS AND (INCHES)

A widebody encapsulation is used to provide creepage and clearance dimensions suitable for safety approval by regulatory agencies worldwide.

The CNW139 is for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70°C operating range for only 0.5 mA of LED current.

The CNW138 is designed for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70°C for an LED current of 1.6 mA (1 TTL load). A 300% minimum CTR enables operation with a fanout of 1 TTL Load using a 2.2 kΩ pull-up resistor.

Regulatory Information

The CNW138/9 features a wide body DIL 8 encapsulation. This package was specifically designed to meet regulatory insulation requirements worldwide. The CNW138/9 has been approved by the following organizations:

UL – Covered under UL component recognition FILE E55361

VDE – Approved according to VDE 0884/08.87 (marks License No. 70975)
Complied for reinforced insulation at 250 V AC with:
DIN IEC 380/VDE 0806
DIN IEC 435/VDE 0805 "ENTWURF"
DIN 57804/VDE 0804 (insulation group C)
DIN VDE 0860 (HD 195 SC)
DIN IEC 601 Teil 1/VDE 0750-1
DIN VDE 0160
EN 60950/IEC 950

NORDIC – Tested for applications (reinforced insulation) – Class II applications for plugable apparatus in normal tight execution.
-SETI-SEMKO-NEMKO-DEMKO-According to IEC 65-IEC380-IEC950-IEC335

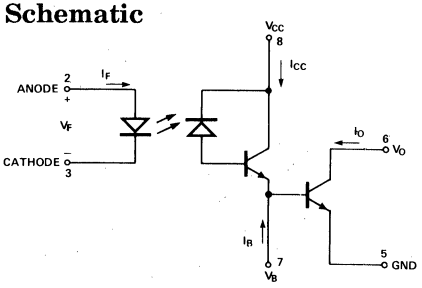
BSI – Certification according to BS415:1990, BS7002:1989 and BS6301:1982 pending

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -55°C to 85°C
Lead Solder Temperature ..... 260°C for 10 s (up to seating plane)
Average Input Current – I_F ..... 100 mA
Peak Transient Input Current – I_F ..... 1.0 A (≤1 µs pulse width, 300 pps)
Reverse Input Voltage – V_R ..... 5 V
Input Power Dissipation (up to 70°C) ..... 250 mW*
Output Current – I_O (Pin 6) ..... 60 mA
Emitter-Base Reverse Voltage (Pin 5-7) ..... 0.5 V
Supply and Output Voltage – V_{CC} (Pin 8-5), V_O (Pin 6-5)
CNW138 ..... -0.5 to 7 V
CNW139 ..... -0.5 to 18 V
Output Power Dissipation ..... 100 mW

*Derate at 5.0 mW/°C for operating temperatures above 70°C.

Schematic



CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

VDE 0884 Insulation Characteristics – Pending Approval

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0109/12.83, Table 1 for rated mains voltage ≤ 600 V_{RMS} for rated mains voltage ≤ 1000 V_{RMS}		 I-IV I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0109/12.83)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{PEAK}
		1000	V_{RMS}
Input to Output Test Voltage, Method b* V_{PR} = 1.6 x V_{IORM}, 100% Production Test with tp = 1 sec, Partial Discharge < 5 pC	V_{PR}	2263	V_{PEAK}
		1600	V_{RMS}
Input to Output Test Voltage, Method a* V_{PR} = 1.2 x V_{IORM}, Type and sample test, tp = 60 sec, Partial Discharge < 5 pC	V_{PR}	1697	V_{PEAK}
	V_{PR}	1200	V_{RMS}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	8000	V_{PK}
Safety-Limiting Values (Maximum values allowed in the event of a failure, also see Figure 10) Case Temperature Current (Input Current I_F, P_{SI} = 0) Output Power (obtained by setting pin 8 = 5.5 V, pins 7, 6, 5 = ground)	 T_{SI} I_{SI} $P_{SI, OUTPUT}$	 150 400 700	 °C mA mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V	R_{IS}	≥ 10^9	ohm

*Refer to the front of the optocoupler section of the optoelectronics Designer's Catalog, under Product Safety Regulations section, (VDE 0884) for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Clearance (External Air Gap)	L(IO1)	9.6	mm	Measured from input terminals to output terminals
Min. External Creepage (External Tracking Path)	L(IO2)	10.0	mm	Measured from input terminals to output terminals
Min. Internal Clearance (Internal Plastic Gap)		1.0	mm	Through insulation distance conductor to conductor
Min. Internal Creepage (Internal Tracking Path)		4.0	mm	Measured from input terminals to output terminals
Comparative Tracking Index	CTI	200	volts	DIN IEC 112/VDE 0303 PART 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group (DIN VDE 0109)

Electrical Specifications

Over Recommended Temperature (T_A = 0°C to 70°C) unless otherwise specified. (See note 7.)

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	CNW139	400	4500		%	I_F = 0.5 mA; V_{CC} = 4.5 V, V_O = 0.4 V	1, 2, 3	1, 2
			500	3000			I_F = 1.6 mA		
			300	1600			I_F = 5.0 mA		
			200	850			I_F = 12 mA		
		CNW138	300	1500		%	I_F = 1.6 mA; V_{CC} = 4.5 V, V_O = 0.4 V		
Logic Low Output Voltage	V_{OL}	CNW139		0.1	0.4	V	I_F = 0.5 mA, I_O = 2 mA; V_{CC} = 4.5 V	1	2
							I_F = 1.6 mA, I_O = 8 mA		
							I_F = 5.0 mA, I_O = 15 mA		
							I_F = 12 mA, I_O = 24 mA		
		CNW138		0.1	0.4	V	I_F = 1.6 mA, I_O = 4.8 mA		
Logic High Output Current	I_{OH}	CNW139		0.10	100	µA	V_O = V_{CC} = 18 V; I_F = 0 mA		2
		CNW138		0.05	250		V_O = V_{CC} = 7 V		
Logic Low Supply Current	I_{CCL}			0.5	2	mA	I_F = 1.6 mA, V_O = Open, V_{CC} = 18 V	9	2
Logic High Supply Current	I_{CCH}			0.010	1	µA	I_F = 0 mA, V_O = Open V_{CC} = 18 V		2
Input Forward Voltage	V_F		1.25	1.45	1.70	V	T_A = 25°C; I_F = 1.6 mA	4, 8	
			1.10		1.80				
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA, T_A = 25°C		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			1.9		mV/°C	I_F = 1.6 mA		
Input Capacitance	C_{IN}			90		pF	f = 1 MHz, V_F = 0 V		
Input-Output Insulation Voltage	V_{ISO}		5000			V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C		3, 8
Resistance (Input-Output)	R_{I-O}		10^{12}	10^{13}		Ω	V_{I-O} = 500 V_{DC}		3
			10^{11}				T_A = 100°C		
Capacitance (Input-Output)	C_{I-O}			0.5	0.6	pF	f = 1 MHz		3

*All typicals at T_A = 25°C.

Switching Specifications

Over Recommended Temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	CNW139		7	25	µs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 11	2, 4
					30				
				0.3	1		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω	7, 11	
					1.1				
		CNW138		2	10		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ	6, 11	
					11				
Propagation Delay Time to Logic High at Output	t_{PLH}	CNW139		40	60	µs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 11	2, 4
					115				
				3.5	7		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω	7, 11	
					11				
		CNW138		20	35		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ	6, 11	
					70				
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$		500			V/µs	I_F = 0 mA, R_L = 2.2 kΩ, R_{CC} = 0 Ω, V_{CM} = 10 V	12	5, 6
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$		500			V/µs	I_F = 1.6 mA, R_L = 2.2 kΩ, R_{CC} = 0 Ω, V_{CM} = 10 V	12	5, 6

*All typicals are at T_A = 25°C.

Notes:

1. DC CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
2. Pin 7 Open.
3. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
4. Use of a resistor between pin 5 and 7 will decrease gain and delay time. See Application Note 951-1 for more details.
5. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e. V_O > 2.0 V) Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM} dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e. V_O < 0.8 V).
6. In applications where dV/dt may exceed 50,000 V/µs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is
$$R_{CC} \approx \frac{1V}{0.15\ I_F\ (mA)}\ k\Omega.$$
7. Use of a 0.1 µF bypass capacitor connected betweens pin 5 and 8 is recommended for operation.
8. In accordance with UL 1577, each product is tested by applying an insulation test voltage of ≥ 6000 V_{rms} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA). This test is performed in addition to the tests shown in the VDE 0884 Insulation Characteristics table.

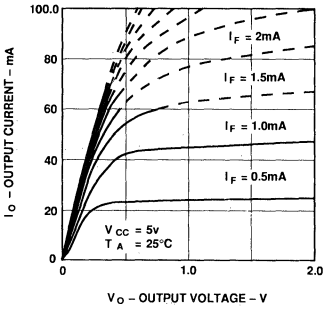


Figure 1. CNW138/9 DC Transfer Characteristics.

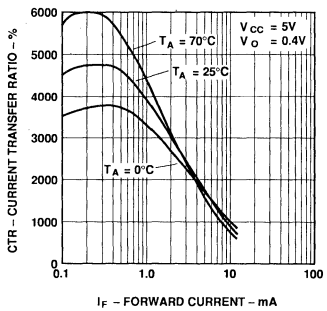


Figure 2. Current Transfer Ratio vs. Forward Current CNW138/9.

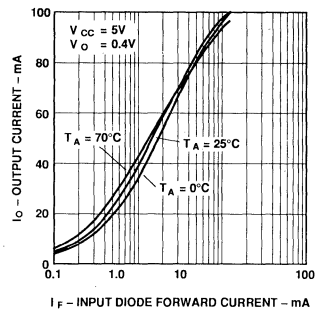


Figure 3. CNW 138/9 Output vs. Input Diode Forward Current.

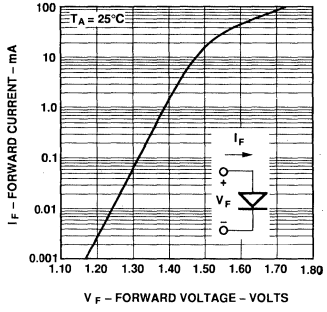


Figure 4. Input Diode Forward Current vs. Forward Voltage.

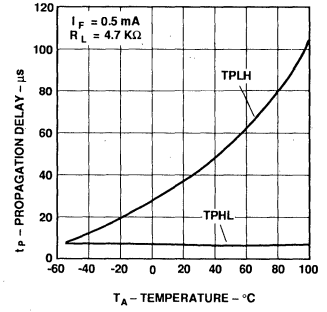


Figure 5. Propagation Delay vs. Temperature.

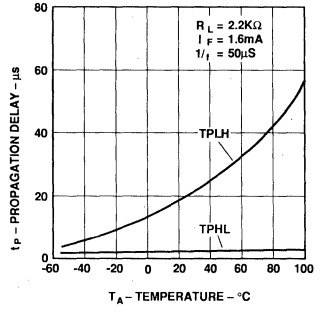


Figure 6. Propagation Delay vs. Temperature.

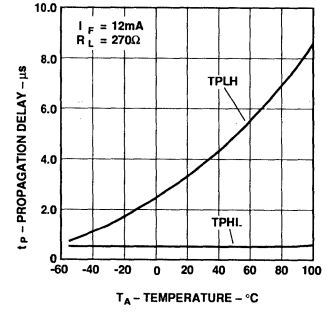


Figure 7. Propagation Delay vs. Temperature.

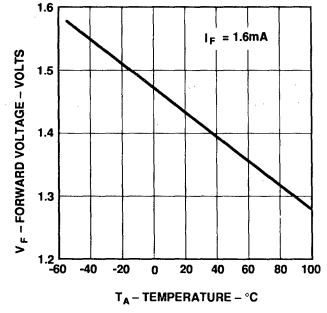


Figure 8. Forward Voltage vs. Temperature.

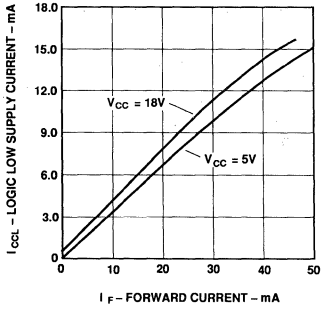


Figure 9. Logic Low Supply Current vs. Forward Current, CNW139.

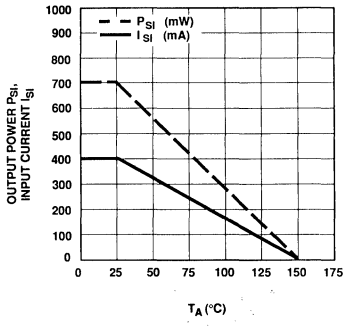


Figure 10. Dependence of Safety Maximum Ratings with Ambient Temperature.

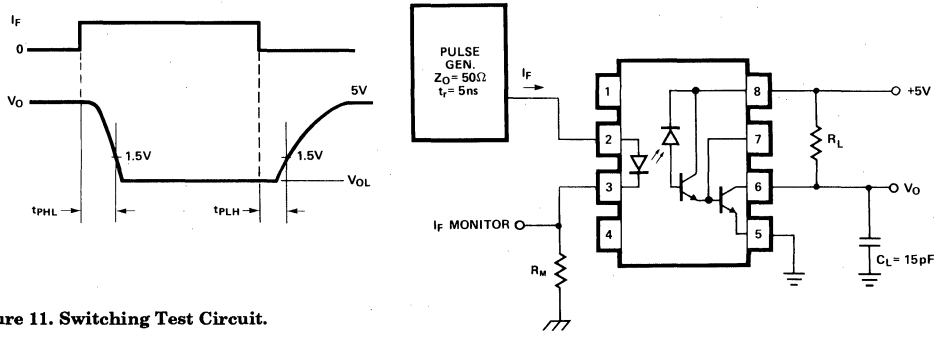


Figure 11. Switching Test Circuit.

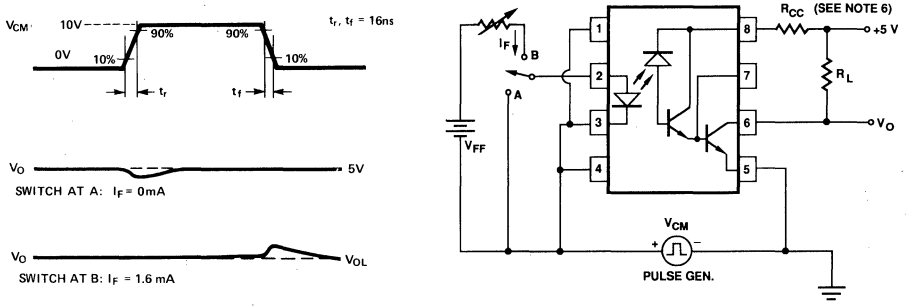


Figure 12. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

High Speed CMOS Optocoupler

Technical Data

HCPL-7100
HCPL-7101

Features

- CMOS IC Technology
- Compatibility with All +5 V CMOS and TTL Logic Families
- No External Components Required for Logic Interface
- High Speed: 15 MBd (HCPL-7100) and 50 MBd (HCPL-7101) Guaranteed
- Low Power Consumption
- World Wide Safety Approval
  UL 1577 (3750 Vac)
  VDE 0884 (V_{IORM} = 600 V_{RMS})
  CSA Approval Pending
- 3-State Output
- 3750 Vac/1 Minute Dielectric Withstand
- High Common Mode Transient Immunity

Applications

- Multiplexed Data Transmission
- Computer-Peripheral Interface
- Microprocessor System Interface
- Digital Isolation for A/D, D/A Conversion
- Instrument Input/Output Isolation
- Motor Control
- Power Inverter

Description

The HCPL-7100/7101 optocoupler combines the latest CMOS IC technology, a new high-speed high-efficiency AlGaAs LED, and an optimized light coupling system to achieve outstanding performance with very low power consumption. It requires only two bypass capacitors for complete CMOS/TTL compatibility.

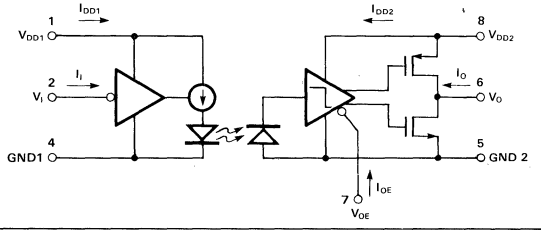
Basic building blocks of the HCPL-7100/7101 are a CMOS LED driver IC, an AlGaAs LED, and a CMOS detector IC. A CMOS or TTL logic input signal controls the LED driver IC which supplies current to the LED. The detector IC incorporates an integrated photodiode, a high-speed transimpedance amplifier and a voltage comparator with hysteresis. The 3-state output is CMOS and TTL compatible and is controlled by the output enable pin, V_{OE}.

The HCPL-7100/7101 consumes very little power, due to the CMOS IC technology and the light coupling system. The entire optocoupler typically uses only 10 mA of supply current, including the LED current.

World wide safety approval and 3750 Vac/1 minute dielectric withstand is achieved with a new packaging process.

The HCPL-7100/7101 provides the user with an easy-to-use CMOS or TTL compatible optocoupler ideally suited for a variety of applications where high speed and low power consumption are desired.

Schematic



TRUTH TABLE (POSITIVE LOGIC)

INPUT	ENABLE	OUTPUT
H	H	Z
L	H	Z
H	L	H
L	L	L

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Regulatory Information

The HCPL-7100/1 has been approved by the following organizations:

UL

Covered under UL component recognition FILE E55361

VDE

Approved according to VDE 0884/08.87(Marks License 58815)

Can be used for safe electrical separation between AC mains and SELV (safety extra-low voltage) in equipment according to the following specifications:

DIN VDE 0804/05.89
DIN VDE 0160/05.88

CSA

Approval received

VDE 0884 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0109/12.83, Table 1 for rated mains voltage ≤300 V_{RMS} for rated mains voltage ≤600 V_{RMS}		 I-IV I-III	
Climatic Classification		40/85/21	
Pollution Degree (DIN VDE 0109/12.83)**		2	
Maximum Continuous Insulation Voltage	V_{IORM}	848	V_{PEAK}
		600	V_{RMS}
Input to Output Test Voltage, Method b* V_{PR} = 1.6 x V_{IORM}, Production test with t_p = 1 sec, Partial discharge < 5 pC	V_{PR}	1,358	V_{PEAK}
		960	V_{RMS}
Input to Output Test Voltage, Method a* V_{PR} = 1.2 x V_{IORM}, Type and sample test, t_p = 60 sec, Partial discharge < 5 pC	V_{PR}	1,018	V_{PEAK}
		720	V_{RMS}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	6000	V_{PEAK}
Safety-limiting values (Maximum values allowed in the event of a failure, also see Figure 15) Case Temperature Input Power (obtained by setting pin 1 = 5.5 V, pin 2 = 0.5 V, pin 4 = gnd) Output Power (obtained by setting pin 8 = 5.5 V, pins 7, 6, 5 = ground)	 T_{SI} $P_{SI, Input}$ $P_{SI, Output}$	 175 50 220	 °C mW mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V	R_{IS}	≥10E11	Ohm

*Refer to the front of the optocoupler section in the current Optoelectronics Designer's Catalog, under regulatory information, (VDE 0884) for a detailed description.
**This part may also be used in Pollution Degree 3 environments where the rated mains voltage is ≤ 300 V_{RMS} (per DIN VDE 0109/12.83).

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External air gap (clearance)	L (IO1)	>7	mm	Measured from input terminals to output terminals
Min. External tracking path (creepage)	L (IO2)	8.0	mm	Measured from input terminals to output terminals
Min. Internal plastic gap (clearance)		0.5	mm	Through insulation distance conductor to conductor
Tracking resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		III a		Material Group DIN VDE 0109

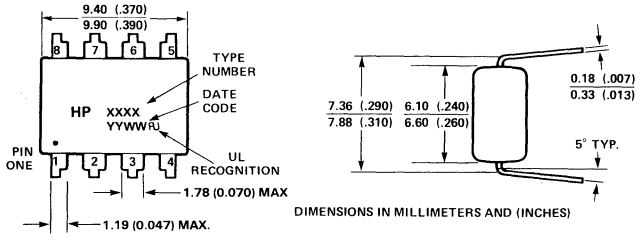
Absolute Maximum Ratings

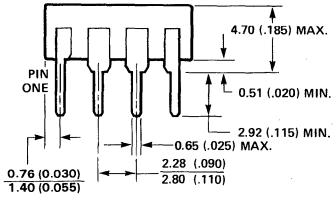
Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-55	125	°C
Supply Voltages	$V_{DD1,2}$	0.0	5.5	V
Input Voltage	V_I	-0.5	V_{DD1} + 0.5	V
Output Voltage	V_O	-0.5	V_{DD2} + 0.5	V
Output Enable Voltage	V_{OE}	-0.5	V_{DD2} + 0.5	V
Average Output Current	I_O		25	mA
Package Power Dissipation	P_{PD}		220	mW
Operating Temperature	T_A	-40	85	°C
Lead Solder Temperature	260°C for 10 s, 1.6 mm below seating plane			

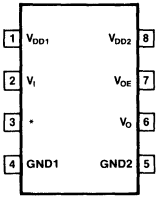
Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Operating Temperature	T_A	-40	85	°C	Ambient Temperature
Supply Voltages	$V_{DD1,2}$	4.5	5.5	V	
Logic High Input Voltage	V_{IH}	2.0	V_{DD1}	V	
Logic Low Input Voltage	V_{IL}	0.0	0.8	V	
Logic High Output Enable Voltage	V_{OEH}	2.0	V_{DD2}	V	Output in high impedance state
Logic Low Output Enable Voltage	V_{OEL}	0.0	0.8	V	Output enabled
Input Signal Rise and Fall Times	t_r, t_f		1	ms	
TTL Fanout	N		6		Standard Loads

Outline Drawing







***Pin 3 is the anode of the internal LED and must be left unconnected for guaranteed data sheet performance.**

Electrical Specifications

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Logic Low Input Supply Current	I_{DD1L}		5.2	10.0	mA	V_{DD1} = 5.5 V $V_I = V_{IL}$		1
Logic High Input Supply Current	I_{DD1H}		0.3	0.6	mA	V_I = 4.5 V, V_{DD1} = 5.5 V		1
			0.9	1.6		V_I = 2.0 V		
Logic Low Output Supply Current	I_{DD2L}		5.0	9.0	mA	V_{DD2} = 5.5 V $V_{OE} = V_{OEL}$ $V_I = V_{IL}$		
Logic High Output Supply Current	I_{DD2H}		5.2	9.0	mA	V_{DD2} = 5.5 V $V_{OE} = V_{OEL}$ I_O = 0 mA $V_I = V_{IH}$		
Tri-State Output Supply Current	I_{DD2Z}		5.1	9.0	mA	V_{OE} = 4.5 V, V_{DD2} = 5.5 V		
			5.6	10.0		V_{OE} = 2.0 V		
Input Current	I_I	-1		1	µA	$V_I = V_{DD1}$ or GND V_{DD1} = 5.5 V		
Output Enable Current	I_{OE}	-1		1	µA	$V_{OE} = V_{DD2}$ or GND V_{DD2} = 5.5 V		
Logic High Output Voltage	V_{OH}	4.4	5.0		V	V_{DD2} = 4.5 V I_O = -20 µA $V_I = V_{IH}$ $V_{OE} = V_{OEL}$	6	

Electrical Specifications (cont.)

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Logic High Output Voltage	V_{OH}	4.0	4.8		V	V_{DD2} = 4.5 V I_O = -4.0 mA V_I = V_{IH}, V_{OE} = V_{OEL}	6	
Logic High Output Voltage	V_{OH}	3.7	4.7		V	V_{DD2} = 4.5 V I_O = -6.0 mA V_I = V_{IH}, V_{OE} = V_{OEL}	6	
Logic High Output Current	I_{OH}	-7.5	-25		mA	V_{DD2} = 4.5 V V_O = 3.6 V V_I = V_{IH}, V_{OE} = V_{OEL}	6	
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	V_{DD2} = 4.5 V I_O = 20 µA V_I = V_{IL}, V_{OE} = V_{OEL}	5	
Logic Low Output Voltage	V_{OL}		0.1	0.3	V	V_{DD2} = 4.5 V I_O = 4.0 mA V_I = V_{IL}, V_{OE} = V_{OEL}	5	
Logic Low Output Voltage	V_{OL}		0.15	0.4	V	V_{DD2} = 4.5 V I_O = 6.0 mA V_I = V_{IL}, V_{OE} = V_{OEL}	5	
Logic Low Output Current	I_{OL}	10.5	23		mA	V_{DD2} = 4.5 V V_O = 0.6 V V_I = V_{IL}, V_{OE} = V_{OEL}	5	
High Impedance State Output Current	I_{OZ}	-5		5	µA	V_{DD2} = 5.5 V V_{OE} = V_{OEH}, V_O = V_{DD2} or GND		
Insulation Voltage	V_{ISO}	3750			V_{RMS}	t = 1 minute RH ≤ 50% T_A = 25°C		2, 3
Input Capacitance	C_I		4.3		pF	f = 1 MHz		4
Input-Output Resistance	R_{I-O}	10^{12}	10^{13}		Ohms	T_A = 25°C, V_{I-O} = 500 V_{dc}		2
		10^{11}				T_A = 100°C		
Input-Output Capacitance	C_{I-O}		0.7		pF	f = 1 MHz		2

Switching Specifications

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Device	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output	t_{PHL}	HCPL-7100			70	ns	C_L = 50 pF CMOS Signal Levels	7, 8	5, 6
		HCPL-7101		28	40				
		HCPL-7100			70	ns	C_L = 15 pF TTL Signal Levels		
		HCPL-7101			40				
Propagation Delay Time to Logic High Output	t_{PLH}	HCPL-7100			70	ns	C_L = 50 pF CMOS Signal Levels	7, 8	5, 6
		HCPL-7101		27	40				
		HCPL-7100			70	ns	C_L = 15 pF TTL Signal Levels		
		HCPL-7101			40				
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD	HCPL-7100			20	ns	C_L = 50 pF CMOS Signal Levels	7, 9	6, 7
		HCPL-7101		2	6				
		HCPL-7100			20	ns	C_L = 15 pF TTL Signal Levels		
		HCPL-7101			6				
Data Rate		HCPL-7100	15			MBd	% PWD < 30%		8
		HCPL-7101	50	65					
Propagation Delay Skew	t_{PSK}	HCPL-7101			10	ns		10	9
Output Rise Time (10-90%)	t_R	HCPL-7100		12		ns	C_L = 50 pF CMOS Signal Levels	7	
		HCPL-7101		10					
Output Fall Time (90-10%)	t_F	HCPL-7100		8		ns	C_L = 50 pF CMOS Signal Levels	7	
		HCPL-7101		7					
Random Jitter	RJ	HCPL-7101		50		ps rms	V_1 = 0-5 V square wave, f = 25 MHz, input rise/ fall time = 5 ns. R_L = 10 kΩ, C_L = 5 pF. TTL threshold levels.		
Propagation Delay Time From Output Enabled to Logic High Output	t_{PZH}			13		ns	C_L = 50 pF CMOS Signal Levels	12	6
				12		ns	C_L = 15 pF TTL Signal Levels		
Propagation Delay Time From Output Enabled to Logic Low Output	t_{PZL}			11		ns	C_L = 50 pF CMOS Signal Levels	12	6
				10		ns	C_L = 15 pF TTL Signal Levels		

Switching Specifications (cont.)

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Device	Min.	Typ.	Max.	Unit	Test Conditions		Fig.	Note
Propagation Delay Time From Logic High to Output Disabled	t_{PHZ}			12		ns	C_L = 50 pF CMOS Signal Levels		12	6
				12		ns	C_L = 15 pF TTL Signal Levels			
Propagation Delay Time From Logic Low to Output Disabled	t_{PLZ}			9		ns	C_L = 50 pF CMOS Signal Levels		12	6
				11		ns	C_L = 15 pF TTL Signal Levels			
Common Mode Transient Immunity at Logic High Output	$\lvert CM_H \rvert$	HCPL-7100	1000			V/µs	V_{CM} = 50 V	$V_I = V_{IH}$, $V_D > 3.2$ V	13, 14	10
		HCPL-7101	2000				V_{CM} = 200 V			
Common Mode Transient Immunity at Logic Low Output	$\lvert CM_L \rvert$	HCPL-7100	1000			V/µs	V_{CM} = 50 V	$V_I = V_{IL}$, $V_D < 0.8$ V	13, 14	10
		HCPL-7101	2000				V_{CM} = 200 V			
Input Dynamic Power Dissipation Capacitance	C_{PD1}			68		pF				11
Output Dynamic Power Dissipation Capacitance	C_{PD2}			10		pF				11

Notes:

1. The LED is OFF when the V_I is high and ON when V_I is low.
2. Device considered a two terminal device; pins 1-4 shorted together and pins 5-8 shorted together.
3. This is a proof test.
4. C_I is the capacitance measured at pin 2 (V_I).
5. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the V_I signal to the logic switching level of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the V_I signal to the logic switching level of the V_O signal.
6. The logic switching levels are 1.5 V for TTL signals (0-3 V) and 2.5 V for CMOS signals (0-5 V).
7. PWD is defined as $\lvert t_{PHL} - t_{PLH} \rvert$. %PWD (percent pulse width distortion) is equal to PWD in ns divided by symbol duration (bit length) in ns.
8. Minimum data rate is calculated as follows: %PWD/PWD where %PWD is typically chosen by the design engineer (30% is common).
9. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the operating condition range.
10. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 3.2$ V. CM_L is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
11. Unloaded dynamic power dissipation is calculated as follows: $C_{PD} \bullet V_{DD}^2 \bullet f + I_{DD} \bullet V_{DD}$ where f is switching frequency in MHz.

HCPL-7100/7101 Application Information

The HCPL-7100/7101 is extremely easy to use. Because the optocoupler uses high-speed CMOS IC technology, the inputs and output are fully compatible with all +5 V TTL and CMOS logic. TTL or CMOS logic can be connected directly to the inputs and output; no external interface circuitry is required.

As shown in Figure 1, the only external components required for proper operation are two ceramic bypass capacitors. Capacitor values should be between 0.01 μF and 0.1 μF. For each capacitor, the total lead length between both ends of the capacitor and the power-supply pins should not exceed 20 mm. Figure 2 illustrates the recommended printed circuit board layout for the HCPL-7100/7101.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 7).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same supply voltage, output load, and operating temperature). As illustrated in Figure 10, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 11 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 11 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The HCPL-7101 optocoupler offers the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, and power supply ranges.

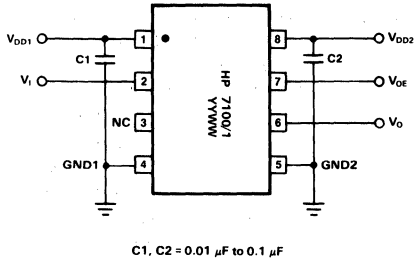


Figure 1. Recommended Application Circuit.

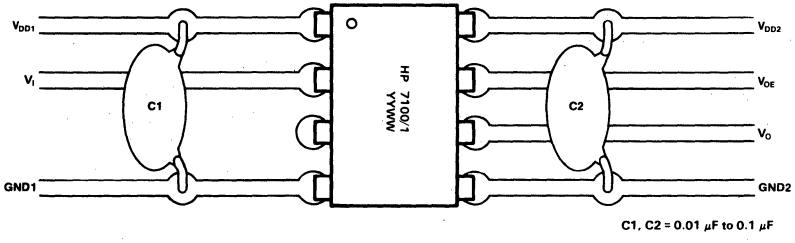


Figure 2. Recommended Printed Circuit Board Layout.

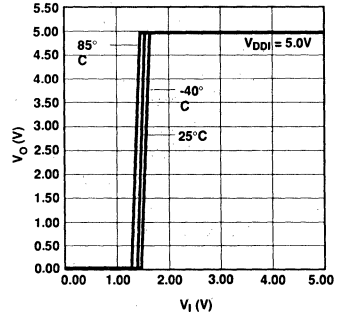


Figure 3. Typical Output Voltage vs. Input Voltage.

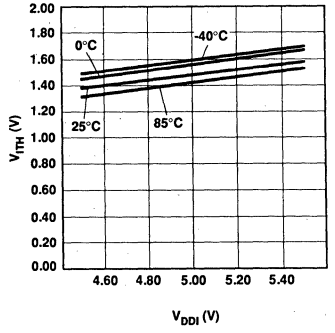


Figure 4. Typical Input Voltage Switching Threshold vs. Input Supply Voltage.

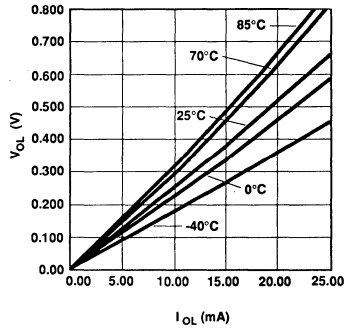


Figure 5. Typical Logic Low Output Voltage vs. Logic Low Output Current.

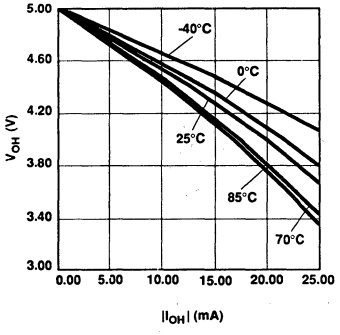


Figure 6. Typical Logic High Output Voltage vs. Logic High Output Current.

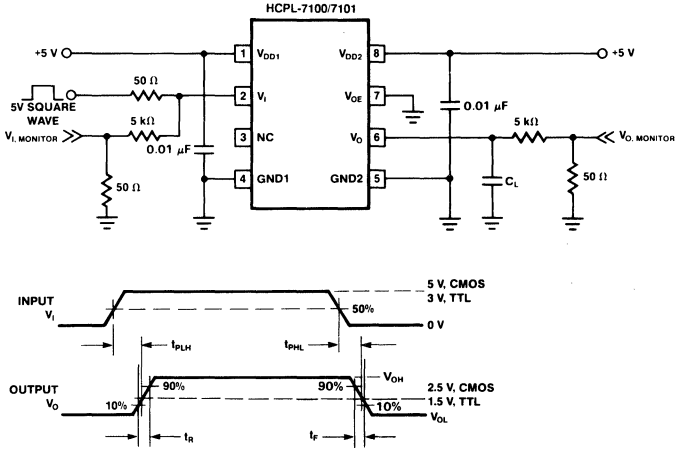


Figure 7. Test Circuit for Propagation Delay, Rise Time and Fall Time.

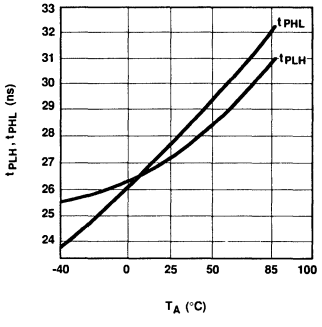


Figure 8. HCPL-7101 Typical Propagation Delay vs. Temperature.

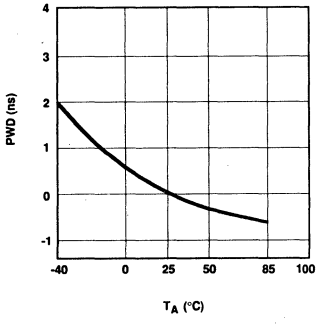


Figure 9. HCPL-7101 Typical Pulse Width Distortion vs. Temperature.

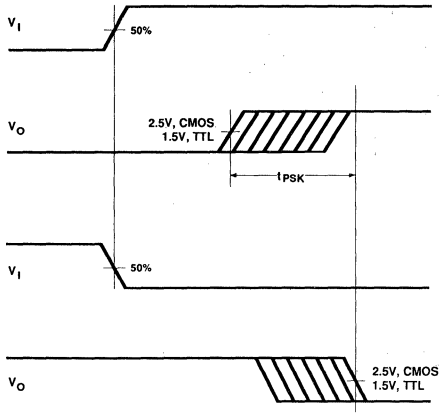


Figure 10. Propagation Delay Skew Waveform.

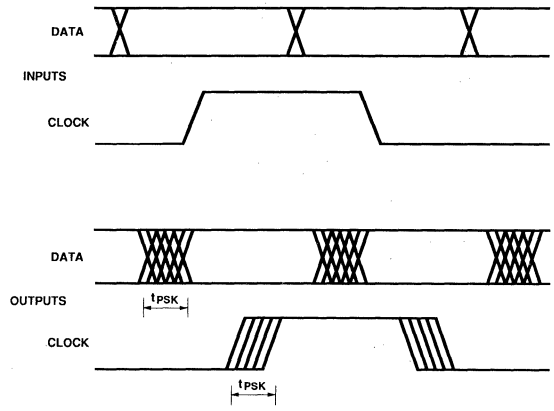


Figure 11. Parallel Data Transmission Example.

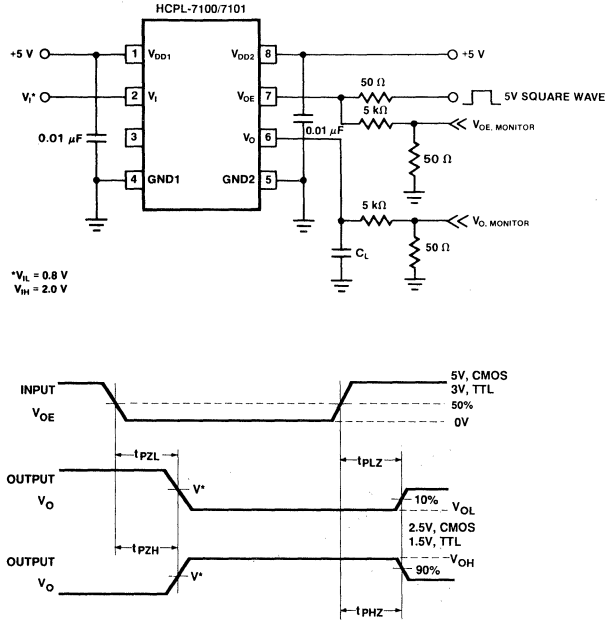


Figure 12. Test Circuit for 3-State Output Enable and Disable Propagation Delays.

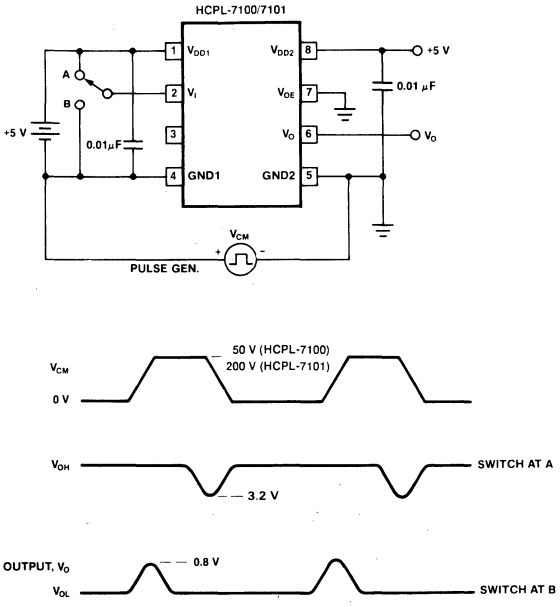


Figure 13. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

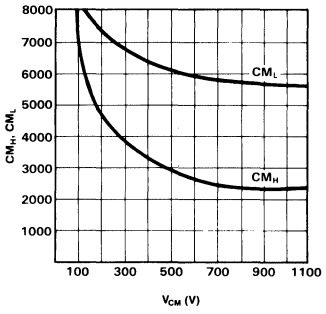


Figure 14. Typical Common Mode Transient Immunity vs. Common Mode Transient Voltage.

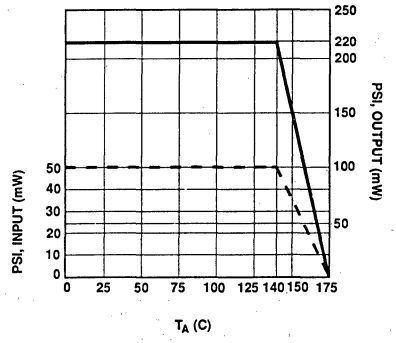
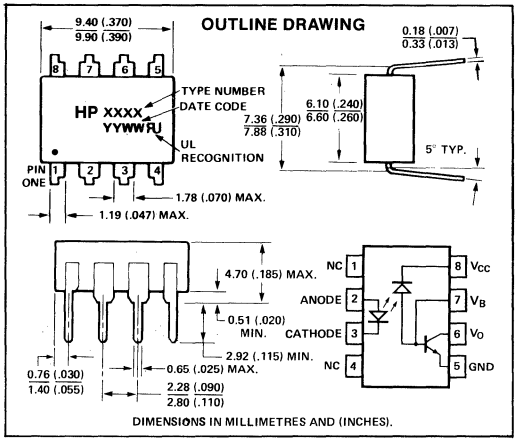


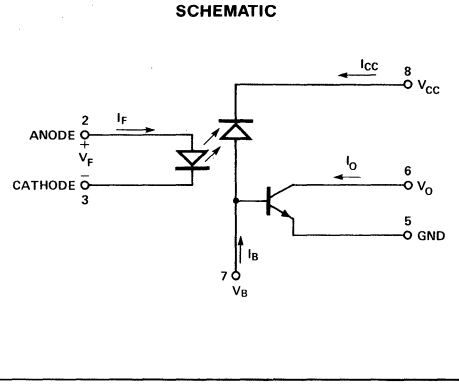
Figure 15. Dependence of Safety-Limiting Data on Ambient Temperature.

HEWLETT PACKARD

WIDEBAND ANALOG/VIDEO OPTOCOUPLER

HCPL-4562





Features

- **WIDE BANDWIDTH: 17 MHz[1]**
- **HIGH VOLTAGE GAIN: 2.0[1]**
- **LOW TEMPERATURE COEFFICIENT (G_V): -0.3% PER °C[1]**
- **HIGHLY LINEAR AT LOW DRIVE CURRENTS**
- **HIGH-SPEED AlGaAs EMITTER**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF VOLTAGES OF 2500 VAC, 1 MINUTE AND 5000 VAC, 1 MINUTE (OPTION 020).**
- **CSA APPROVED UNDER COMPONENT ACCEPTANCE NOTICE NO. 5 (FILE NO. LR 88324)**

Description

The HCPL-4562 optocoupler provides wide-bandwidth isolation for analog signals. It is ideal for video isolation when combined with its application circuit (Figure 4). High linearity and low phase shift are achieved through an 820 nm AlGaAs emitter, combined with a high-speed detector.

Applications

- **VIDEO ISOLATION FOR THE FOLLOWING STANDARDS/FORMATS: NTSC, PAL, SECAM, S-VHS, ANALOG RGB**
- **LOW-DRIVE-CURRENT FEEDBACK ELEMENT IN SWITCHING POWER SUPPLIES, *e.g.* FOR ISDN NETWORKS**
- **A/D CONVERTER SIGNAL ISOLATION**
- **ANALOG SIGNAL GROUND ISOLATION**

Recommended Operating Conditions

Operating Temperature	-10°C to +70°C
Quiescent Input Current — I_{FQ}	6 mA
Peak Input Current — I_F	10 mA

Absolute Maximum Ratings

Storage Temperature	-55°C to +125°C
Operating Temperature	-40°C to +85°C
Lead Solder Temperature	260°C for 10 s (1.6 mm below seating plane)
Average Input Current — I_F	12 mA DC
Peak Input Current — I_F	18.6 mA
Effective Input Current — I_F	12.9 mA rms
Supply Voltage — V_{CC} (Pin 8-5)	-0.3 V to 30 V
Output Voltage — V_O (Pin 6-5)	-0.3 V to 20 V
Reverse Input Voltage — V_R (Pin 3-2)	1.8 V
Emitter-Base Reverse Voltage (Pin 5-7)	5 V
Peak Output Current — I_O (Pin 6)	16 mA
Average Output Current — I_O (Pin 6)	8 mA
Base Current — I_B (Pin 7)	5 mA
Output Power Dissipation[2]	100 mW

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

DC Electrical Specifications (T_A = 25°C)

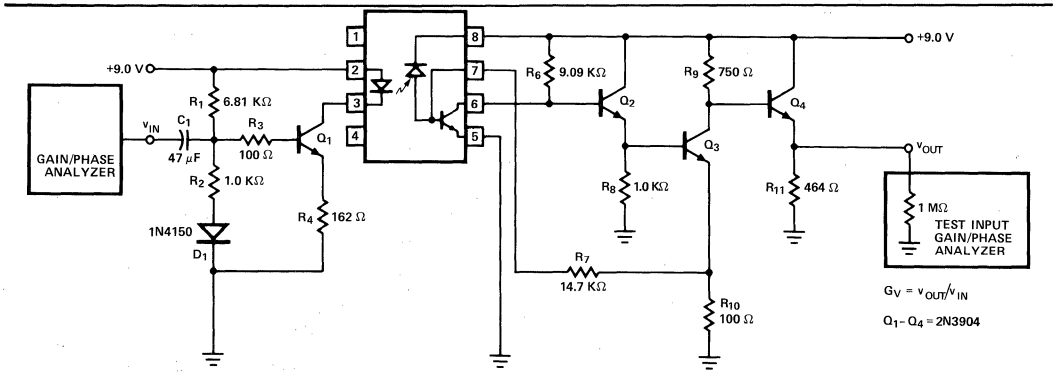
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Notes
Base Photo Current	I_{PB}	13	32 19.2	65	μA μA	I_F = 10 mA, $V_{PB} \geq$ 5 V I_F = 6 mA, $V_{PB} \geq$ 5 V	2, 6 2, 6	
I_{PB} Temperature Coefficient	$\Delta I_{PB}/\Delta T$		−0.3		%/°C	2 mA < I_F < 10 mA, $V_{PB} \geq$ 5 V	2	
I_{PB} Nonlinearity			0.25		%	2 mA < I_F < 10 mA	2, 6	3
Input Forward Voltage	V_F	1.1	1.3	1.6	V	I_F = 5 mA	5	
Input Reverse Breakdown Voltage	BV_R	1.8	5		V	I_R = 10 μA		
Transistor Current Gain	h_{FE}	60	160			I_C = 1 mA, V_{CE} = 1.25 V		
Current Transfer Ratio	CTR		45		%	I_F = 6 mA, V_{CE} = 1.25 V, $V_{PB} \geq$ 5 V	8,9	4
DC Output Voltage	V_O		4.25		V	G_V = 2, V_{CC} = 9 V	4, 15	
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		5
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz		5
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	$R_H \leq$ 50%, t = 1 min.		5, 12
OPTION 020	V_{ISO}	5000						13

Small-Signal Characteristics (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Notes
Voltage Gain	G_V(0.1 MHz)	0.8	2.0	4.2		v_{IN} = 1 V_{p-p}	1	6
G_V Temperature Coefficient	$\Delta G_V/\Delta T$		−0.3		%/°C	v_{IN} = 1 V_{p-p}, f = 0.1 MHz	1, 11	
Base Photo Current Variation	Δi_{PB} (6 MHz)		1.1	3.0	−dB	I_{FQ} = 6 mA, v_{IN} = 1 V_{p-p}, f_{REF} = 0.1 MHz	3, 10, 12	
−3 dB Frequency (i_{PB})	i_{PB} (−3 dB)	6	15		MHz	v_{IN} = 1 V_{p-p}, f_{REF} = 0.1 MHz, I_{FQ} = 6 mA	3, 10, 12	7
−3 dB Frequency (G_V)	G_V(−3 dB)	6	17		MHz	v_{IN} = 1 V_{p-p}, f_{REF} = 0.1 MHz	1, 11	7
Gain Variation	ΔG_V(6 MHz)		0.8		−dB	T_A = −10°C, v_{IN} = 1 V_{p-p}, f_{REF} = 0.1 MHz	1, 11	
			1.1	3.0	−dB	v_{IN} = 1 V_{p-p}, f_{REF} = 0.1 MHz	1, 11	
			1.5		−dB	T_A = 70°C, v_{IN} = 1 V_{p-p}, f_{REF} = 0.1 MHz	1, 11	
	ΔG_V (10 MHz)		1.15		−dB	v_{IN} = 1 V_{p-p}, f_{REF} = 0.1 MHz	1, 11	
Differential Gain			±1		%	I_{Fac} = 0.7 mA pk-pk, I_{Fdc} = 3 to 9 mA, f = 3.58 MHz	3, 7	8
Differential Phase			±1		deg.	I_{Fac} = 0.7 mA pk-pk, I_{Fdc} = 3 to 9 mA, f = 3.58 MHz	3, 7	9
Total Harmonic Distortion	THD		2.5		%	f = 3.58 MHz, G_V = 2, V_{IN} = 1 V_{p-p}, I_{FQ} = 6 mA	4	10
Output Noise Voltage	V_{ONOISE}		950		μV_{RMS}	10 Hz to 10 MHz	1	
Isolation Mode Rejection Ratio	IMRR		122		dB	f = 120 Hz, G_V = 2	14	11

Notes:

1. When used in the circuit of Figure 1 or Figure 4; $G_V = v_{OUT}/v_{IN}$.
2. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C.
3. Maximum variation from the best fit line of I_{PB} vs. I_F expressed as a percentage of the peak-to-peak full-scale output.
4. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
5. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
6. Flat-band small-signal voltage gain.
7. The frequency at which the gain is 3 dB below the flat-band gain.
8. Differential gain is the change in the small-signal gain of the optocoupler at 3.58 MHz as the bias level is varied over a given range.
9. Differential phase is the change in the small-signal phase response of the optocoupler at 3.58 MHz as the bias level is varied over a given range.
10. TOTAL HARMONIC DISTORTION is defined as the square root of the sum of the square of each harmonic distortion component.
11. ISOLATION MODE REJECTION RATIO, a measure of the optocoupler's ability to reject signals or noise that may exist between input and output terminals, is defined by $(v_{OUT}/v_{IN})/(v_{OUT}/v_{IM})$, where v_{IM} is the isolation mode voltage signal.
12. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5\ \mu A$).
13. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5\ \mu A$).



NOTE: ALL RESISTORS ARE 1% TOLERANCE; EXCEPT R_4 (162 Ω ±0.5 Ω).

Figure 1. Gain and Bandwidth Test Circuit

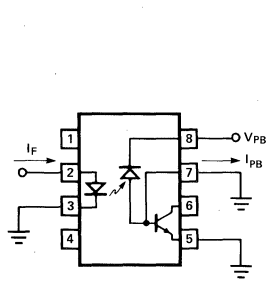


Figure 2. Base Photo Current Test Circuit

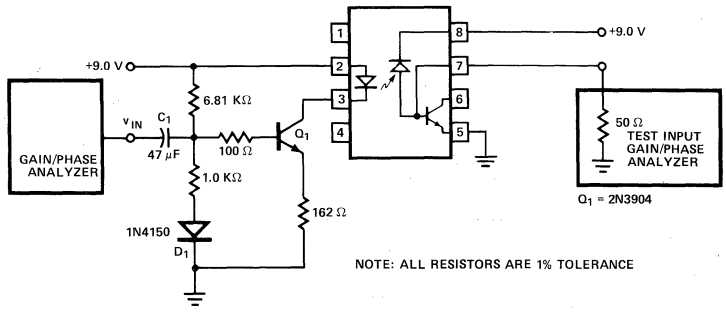


Figure 3. Base Photo Current Frequency Response Test Circuit

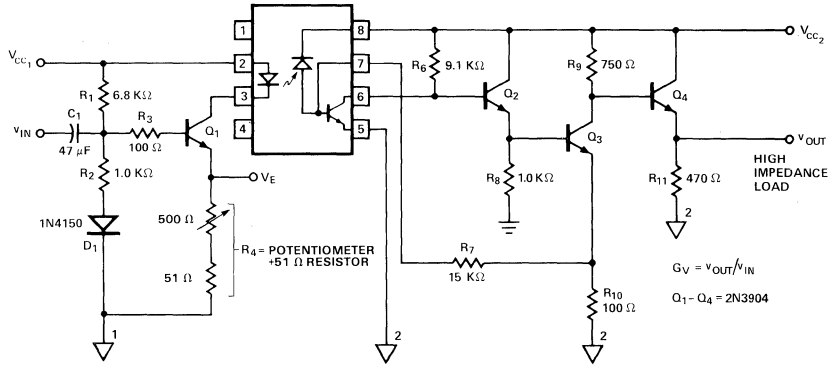


Figure 4. Recommended Isolated Video Interface Circuit

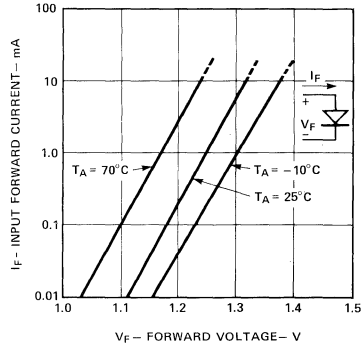


Figure 5. Input Current vs. Forward Voltage

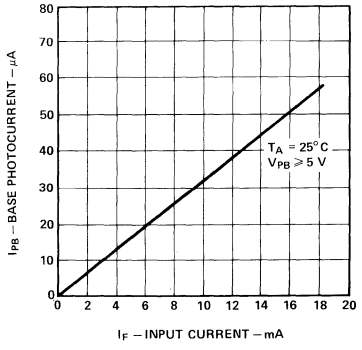


Figure 6. Base Photo Current vs. Input Current

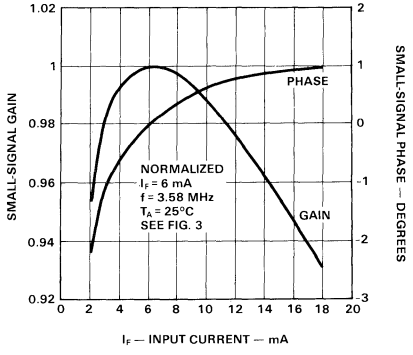


Figure 7. Small-Signal Response vs. Input Current

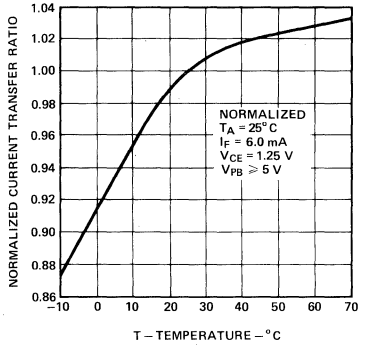


Figure 8. Current Transfer Ratio vs. Temperature

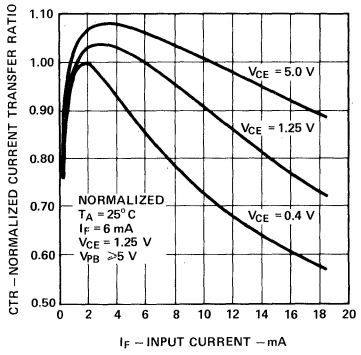


Figure 9. Current Transfer Ratio vs. Input Current

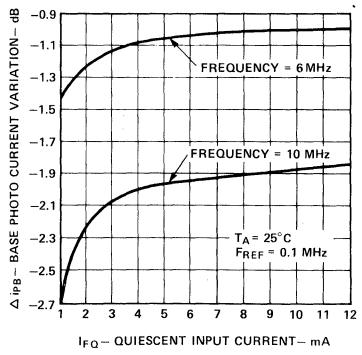


Figure 10. Base Photo Current Variation vs. Bias Conditions

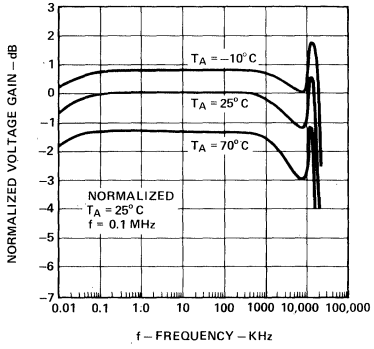


Figure 11. Normalized Voltage Gain vs. Frequency

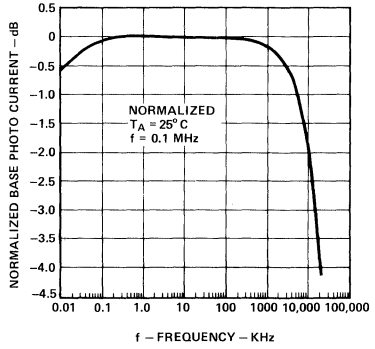


Figure 12. Normalized Base Photo Current vs. Frequency

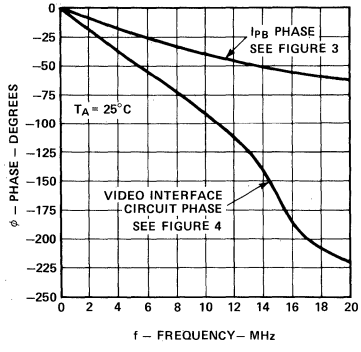


Figure 13. Phase vs. Frequency

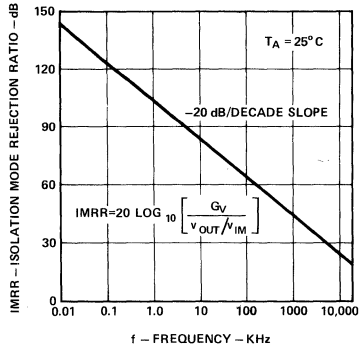


Figure 14. Isolation Mode Rejection Ratio vs. Frequency

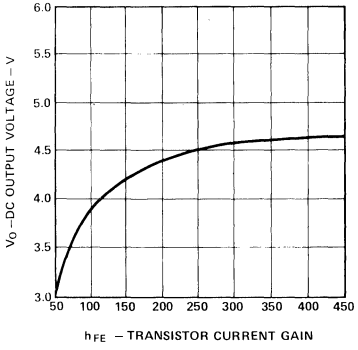


Figure 15. DC Output Voltage vs. Transistor Current Gain

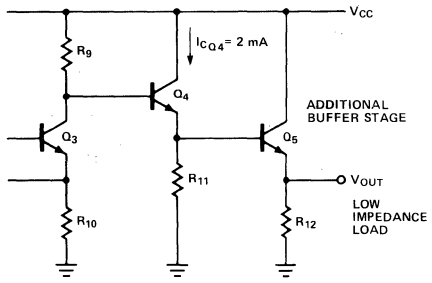


Figure 16. Output Buffer Stage for Low Impedance Loads

Design Considerations of the Application Circuit

The application circuit in Figure 4 incorporates several features that help maximize the bandwidth performance of the HCPL-4562. Most important of these features is peaked response of the detector circuit that helps extend the frequency range over which the voltage gain is relatively constant. The number of gain stages, the overall circuit topology and the choice of DC bias points are all consequences of the desire to maximize bandwidth performance.

To use the circuit, first select R_1 to set V_E for the desired LED quiescent current by:

$$I_{FQ} = \frac{V_E}{R_4} \cong \frac{G_V V_E R_{10}}{(\partial I_{PB}/\partial I_F) R_7 R_9} \quad (1)$$

For a constant value of $v_{IN_{p-p}}$, the circuit topology (adjusting the gain with R_4) preserves linearity by keeping the modulation factor (MF) dependent only on V_E.

$$i_{F_{p-p}} \cong v_{IN}/R_4 \quad (2)$$

$$\frac{i_{F_{p-p}}}{I_{FQ}} \cong \frac{i_{PB_{p-p}}}{I_{PBQ}} = \frac{v_{IN_{p-p}}}{V_E} \quad (3)$$

$$\text{Modulation Factor (MF)} \frac{i_{F_{(p-p)}}}{2 I_{FQ}} \cong \frac{v_{IN_{p-p}}}{2 V_E} \quad (4)$$

For a given G_V, V_E, and V_{CC}, DC output voltage will vary only with h_{FEX}.

$$V_O = V_{CC} - V_{BE_4} - \frac{R_9}{R_{10}} (V_{BEX} - (I_{PBQ} - I_{BXQ}) R_7) \quad (5)$$

Where:

$$I_{PBQ} \cong \frac{G_V V_E R_{10}}{R_7 R_9} \quad (6)$$

and,

$$I_{BXQ} \cong \frac{V_{CC} - 2 V_{BE}}{R_6 h_{FEX}} \quad (7)$$

Figure 15 shows the dependency of the DC output voltage on h_{FEX}.

For 9 V < V_{CC} < 12 V, select the value of R_{11} such that

$$I_{C_{Q4}} \cong \frac{V_O}{R_{11}} \leq \frac{4.25V}{470\Omega} \leq 9.0\,mA \quad (8)$$

The voltage gain of the second stage (Q_3) is approximately equal to:

$$\frac{R_9}{R_{10}} * \frac{1}{1 + s R_9 \left[C_{CQ_3} + \frac{1}{2\pi R'_{11} f_{T_4}} \right]} \quad (9)$$

Increasing R'_{11} (R'_{11} includes the parallel combination of R_{11} and the load impedance) or reducing R_9 (keeping R_9/R_{10} ratio constant) will improve the bandwidth.

If it is necessary to drive a low impedance load, bandwidth may also be preserved by adding an additional emitter following the buffer stage (Q_5 in Figure 16), in which case R_{11} can be increased to set $I_{CQ_4} \cong 2$ mA.

Finally, adjust R_4 to achieve the desired voltage gain.

$$G_V \cong \frac{v_{OUT}}{v_{IN}} \cong \frac{\partial I_{PB}}{\partial I_F} \left[\frac{R_7 R_9}{R_4 R_{10}} \right] \quad (10)$$

$$\text{where typically } \frac{\partial I_{PB}}{\partial I_F} = 0.0032$$

Definition:

G_V= Voltage Gain
I_{FQ}= Quiescent LED forward current
$i_{F_{p-p}}$= Peak-to-peak small signal LED forward current
$v_{IN_{p-p}}$= Peak-to-peak small signal input voltage
$i_{PB_{p-p}}$= Peak-to-peak small signal base photo current
I_{PBQ}= Quiescent base photo current
V_{BEX}= Base-Emitter voltage of HCPL-4562 transistor
I_{BXQ}= Quiescent base current of HCPL-4562 transistor
h_{FEX}= Current Gain (IC/IB) of HCPL-4562 transistor
V_E= Voltage across emitter degeneration resistor R_4
f_{T_4}= Unity gain frequency of Q_4
C_{CQ_3}= Effective capacitance from collector of Q_3 to ground

HEWLETT PACKARD

New

Wide Body, High Bandwidth, Analog/Video Optocoupler

Technical Data

CNW4562

Features

- **5000 V_{rms}/1 Minute Insulation Withstand Capability**
- **Worldwide Safety Approval**
  UL1577 (File No. E55361)
  VDE 0884 Certification (V_{IORM} = 1 kV_{RMS})
  VDE 860/805/806/804/750-1/ IEC 950
  BSI According to BS 415/ 7002/6301
  SETI-SEMKO-NEMKO-DEMKO-According to IEC 65/380/950/335
- **Wide Bandwidth: 9 MHz[1]**
- **High Voltage Gain: 3[1]**
- **Low Temperature Coefficient (G_V): –0.3% Per °C[1]**
- **Highly Linear at Low Drive Currents**
- **Function Compatible with HCPL-4562**

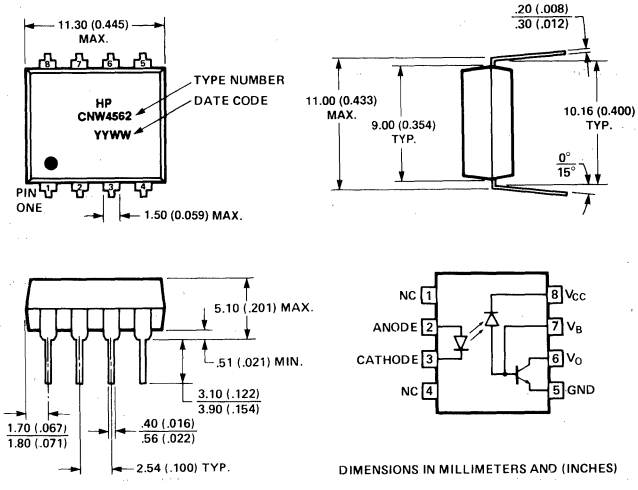
Applications

- **Video Signal Isolation for the Following Standards/ Formats: NTSC, PAL, SECAM, S-VHS, ANALOG RGB.**
- **Low-Drive-Current Feedback Element in Switching Power Supplies, e.g. for ISDN Networks**
- **A/D Converter Signal Isolation**
- **Analog Signal Ground Isolation**
- **High Voltage Insulation**

Description

The CNW4562 is a wide body optocoupler that provides wide-bandwidth isolation for analog signals. It is ideal for video isolation when combined with its application circuit (Figure 4). The wide body encapsulation provides creepage and clearance dimensions suitable for safety approval by regulatory agencies worldwide.

Package Outline



DIMENSIONS IN MILLIMETERS AND (INCHES)

Regulatory Information

The CNW4562 features a wide body eight pin DIP. This package was specifically designed to meet worldwide regulatory requirements. The CNW4562 has been approved by the following organizations:

UL	Covered under UL component recognition FILE E55361
VDE	Approved according to VDE 0884/08.87 (marks License No. 70975) Complied for reinforced insulation at 250 Vac with: DIN IEC 380/VDE 0806 DIN IEC 435/VDE 0805 "ENTWURF" DW 57804/DIN VDE 0804 (isolation group C) DIN VDE 0860 (HD 195 S6) DIN IEC 601 Teil 1/VDE 0750-1 DIN VDE 0160 EN 60950/IEC 950
NORDIC	Tested for applications (reinforced insulation) - Class II applications for plugable apparatus in normal tight execution. SETI-SEMKO-NEMKO-DEMKO-According to IEC65-IEC380-IEC950-IEC335.
BSI	Certification according to BS415:1990, BS7002:1989 & BS6301:1982 for class II applications.

*Refer to the front of the optocoupler section of the 1991/1992 Optoelectronics Designer's Catalog, under Product Safety Regulations section, (VDE 0884) for a detailed description.

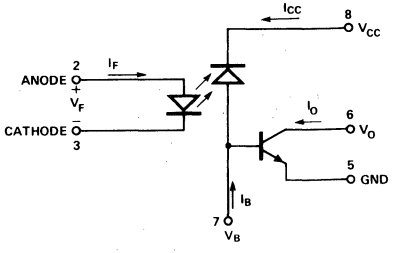
Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 s (up to seating plane)
Average Input Current - I_F ..... 100 mA
Reverse Input Voltage - V_R (Pin 3-2) ..... 5 V
Input Power Dissipation ..... 250 mW[2]
Average Output Current - I_O (Pin 6) ..... 10 mA
Emitter-Base Reverse Voltage (Pin 5-7) ..... 5 V
Output Voltage - V_O (Pin 6-5) ..... -0.3 V to 20 V
Supply Voltage - V_{CC} (Pin 8-5) ..... -0.3 V to 30 V
Base Current - I_B (Pin 7) ..... 5 mA
Output Power Dissipation ..... 100 mW

Recommended Operating Conditions

Quiescent Input Current - I_{FQ} ..... 10 mA
Peak Input Current - I_F ..... 17 mA

Schematic



CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

VDE 0884 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0109/12.83, Table 1 For rated mains voltage ≤ 600 V_{rms} For rated mains voltage ≤ 1000 V_{rms}		 I-IV I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0109/12.83)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{PEAK}
		1000	V_{rms}
Input to Output Test Voltage, Method b* V_{PR} = 1.6 x V_{IORM}, 100% Production Test with t_p = 1 sec, Partial Discharge < 5 pC	V_{PR}	2263	V_{PEAK}
		1600	V_{rms}
Input to Output Test Voltage, Method a* V_{PR} = 1.2 x V_{IORM}, Type and sample test, t_p = 60 sec, Partial Discharge < 5 pC	V_{PR}	1697	V_{PEAK}
		1200	V_{rms}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	8000	V_{PEAK}
Safety-Limiting Values (Maximum values allowed in the event of a failure, also see Figure 17)			
Case Temperature	T_{SI}	150	°C
Current (Input Current I_F, P_{SI} = 0)	I_{SI}	400	mA
Output Power (obtained by setting pin 8 = 5.5 V, pins 7,6,5 = ground)	P_{SI}, OUTPUT	700	mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V	R_{IS}	$>10^9$	Ω

*Refer to the front of the optocoupler section of the HP Optoelectronics Designer's Catalog, under Product Safety Regulations section, (VDE 0884) for a detailed description.

Note: Insulation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits in the application.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Clearance (External Air Gap)	L(IO1)	9.6	mm	Measured from input terminals to output terminals
Min. External Creepage (External Tracking Path)	L(IO2)	10.0	mm	Measured from input terminals to output terminals
Min. Internal Clearance (Internal Plastic Gap)		1.0	mm	Through insulation distance conductor to conductor
Min. Internal Creepage (Internal Tracking Path)		4.0	mm	Measured from input terminals to output terminals
Comparative Tracking Index	CTI	200	volts	DIN IEC 112/VDE 0303 PART 1
Isolation Group (per DIN VDE 0109)		IIIa		Material group (DIN VDE 0109)

Electrical Specifications (T_A = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Notes
Base Photo Current	I_{PB}	13	30	65	µA	I_F = 10 mA, $V_{PB} \geq$ 5 V	2, 6	
I_{PB} Temp. Coefficient	$\Delta I_{PB}/\Delta T$		-0.3		%/°C	2 mA < I_F < 10 mA $V_{PB} \geq$ 5 V	2	
I_{PB} Nonlinearity			0.15		%	6 mA < If < 14 mA	2, 6	3
Input Forward Voltage	V_F	1.2	1.60	1.8	V	I_F = 10 mA	5	
Input Reverse Breakdown Voltage	BV_R	5.0			V	I_R = 10 µA		
Transistor Current Gain	h_{FE}	60	170			I_C = 1 mA, V_{CE} = 1.25 V $V_{PB} \geq$ 5 V		
Current Transfer Ratio	CTR		52		%	I_F = 10 mA, V_{CE} = 1.25 V $V_{PB} \geq$ 5 V	8, 9	4
DC Output Voltage	V_{OUT}		5.0		V	I_{FQ} = 10 mA G_V = 2, V_{CC} = 9 V	4, 15	
Input-Output Capacitance	C_{I-O}		0.5	0.6	pF	f = 1 MHz		5
Resistance (Input-Output)	R_{I-O}	10^{12}	10^{13}		Ω	T_A = 25°C, V_{I-O} = 500 Vdc		5
		10^{11}				T_A = 100°C		
Input-Output Insulation Voltage	V_{ISO}	5000			V_{rms}	RH ≤ 50%, t = 1 min T_A = 25°C		5, 12

Small Signal Characteristics (T_A =25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Notes
Voltage Gain	G_V (0.1 MHz)	0.8	3.0	4.2		I_{FQ} = 10 mA V_{IN} = 1 V_{p-p}	1	6
G_V Temperature Coefficient	$\Delta G_V/\Delta T$		-0.3		%/°C	I_{FQ} = 10 mA, V_{IN} = 1 V_{p-p} f_{REF} = 0.1 MHz	1, 11	
Base Photo Current Variation	Δi_{PB} (6 MHz)		0.36	3.0	-dB	I_{FQ} = 10 mA, V_{IN} = 1 V_{p-p} f_{REF} = 0.1 MHz	3, 10, 12	
-3 dB Freq (i_{PB})	i_{PB} (-3 dB)	6	13		MHz	I_{FQ} = 10 mA, V_{IN} = 1 V_{p-p} f_{REF} = 0.1 MHz	3, 10, 12	7
-3 dB Freq (G_V)	G_V (-3 dB)	6	9.0		MHz	I_{FQ} = 10 mA, V_{IN} = 1 V_{p-p} f_{REF} = 0.1 MHz	1, 11	7
Gain Variation	ΔG_V (6 MHz)		0.54	3.0	-dB	V_{IN} = 1 V_{p-p} f_{REF} = 0.1 MHz	1, 11	
	ΔG_V (10 MHz)		2.27					
Differential Gain			±0.9		%	I_{Fac} = 1 mA pk-pk I_{Fdc} = 7 to 13 mA f = 3.58 MHz	3, 7	8
Differential Phase			±0.6		deg.	I_{Fac} = 1 mA pk-pk I_{Fdc} = 7 to 13 mA f = 3.58 MHz	3, 7	9
Total Harmonic Distortion	THD		0.75		%	f = 3.58 MHz, G_V =2, V_{IN} = 1 Vp-p I_{FQ} = 10 mA	4	10
Output Noise Voltage	V_O noise		950		μV_{rms}	10 Hz to 10 MHz	1	
Isolation Mode Rejection Ratio	IMRR		119		dB	f = 120 Hz, G_V = 2	14	11

Notes:

1. When used in the circuit of Figure 1 or Figure 4; $G_V = V_{OUT}/V_{IN}$; I_{FQ} = 10 mA.
2. Derate linearly above 65°C free-air temperature at a rate of 4.6 mW/°C to maintain $T_J \leq 125$°C.
3. Maximum variation from the best fit line of I_{PB} vs. I_F expressed as a percentage of the peak-to-peak full scale output.
4. CURRENT TRANSFER RATIO (CTR) is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
5. Device considered a two terminal device: Pins 1,2,3, and 4 shorted together and pins 5,6,7, and 8 shorted together.
6. Flat-band, small-signal voltage gain.
7. The frequency at which the gain is 3 dB below the flat-band gain.
8. Differential gain is the change in the small-signal gain of the optocoupler at 3.58 MHz as the bias level is varied over a given range.
9. Differential phase is the change in the small-signal phase response of the optocoupler at 3.58 MHz as the bias level is varied over a given range.
10. TOTAL HARMONIC DISTORTION (THD) is defined as the square root of the sum of the square of each harmonic distortion component. The THD of the isolated video circuit is measured using a 2.6 kΩ load in series with the 50 Ω input impedance of the spectrum analyzer.
11. ISOLATION MODE REJECTION RATIO (IMRR), a measure of the optocoupler's ability to reject signals or noise that may exist between input and output terminals, is defined by 20 $\log_{10}$ [$(V_{OUT}/V_{IN})/(V_{OUT}/V_{IM})$], where V_{IM} is the isolation mode voltage signal.
12. In accordance with UL 1577, each product is tested by applying an insulation test voltage of ≥ 6000 V_{rms} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA). This test is performed in addition to the tests shown in the VDE 0884 Insulation Characteristics Table.

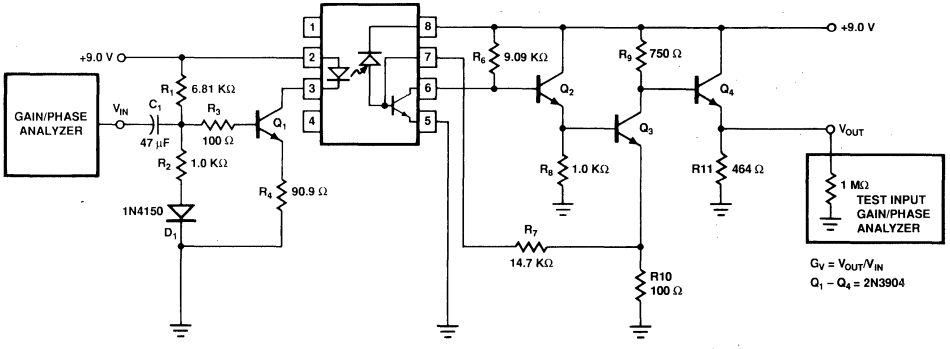


Figure 1. Gain and Bandwidth Test Circuit.

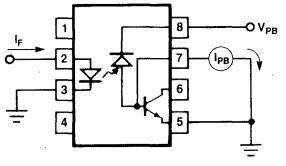


Figure 2. Base Photo Current Test Circuit.

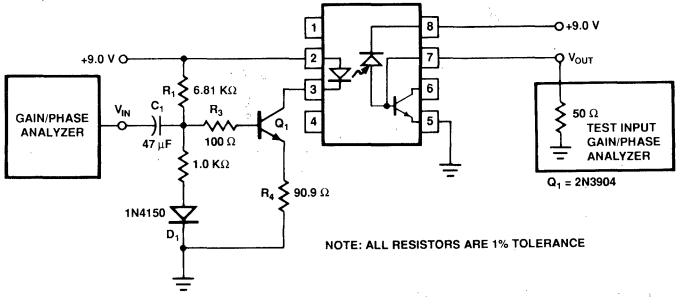


Figure 3. Base Photo Current Frequency Response Test Circuit.

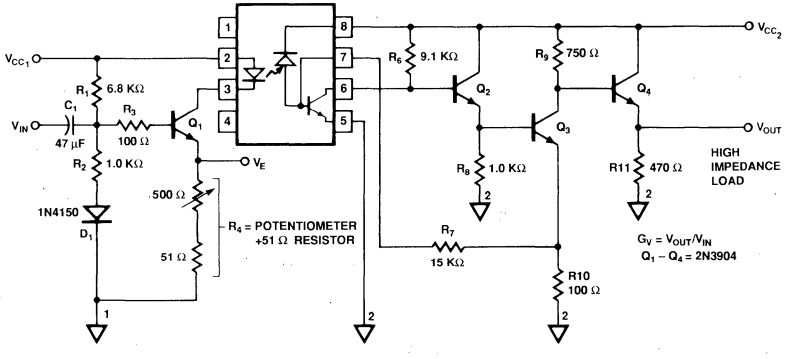


Figure 4. Recommended Isolated Video Interface Circuit.

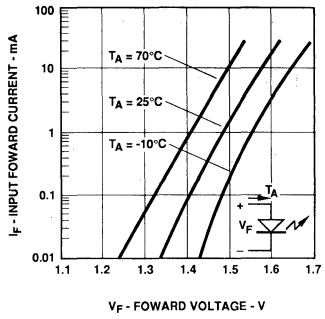


Figure 5. Input Current vs. Forward Voltage.

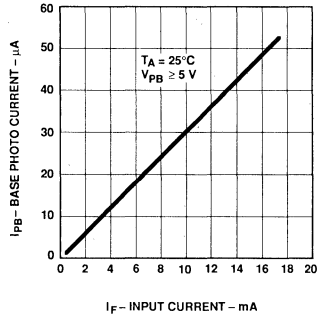


Figure 6. Base Photo Current vs. Input Current.

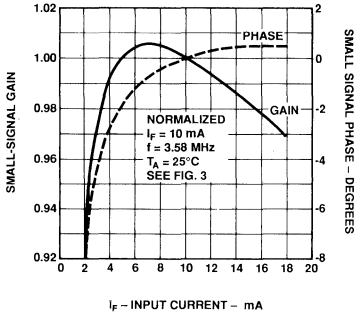


Figure 7. Small-Signal Response vs. Input Current.

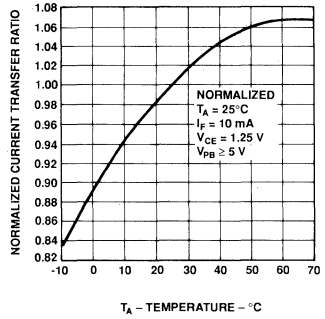


Figure 8. Current Transfer Ratio vs. Temperature.

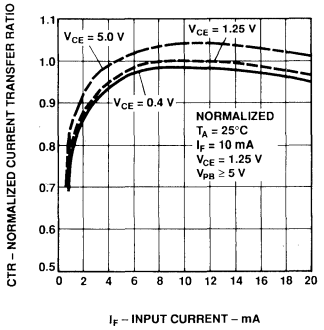


Figure 9. Current Transfer Ratio vs. Input Current.

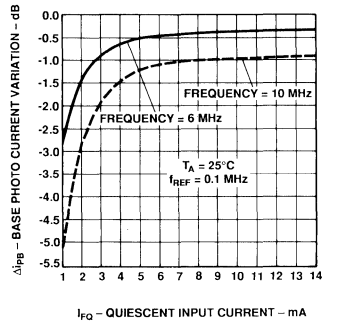


Figure 10. Base Photo Current Variation vs. Bias Conditions.

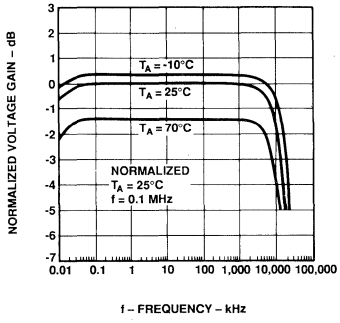


Figure 11. Normalized Voltage Gain vs. Frequency.

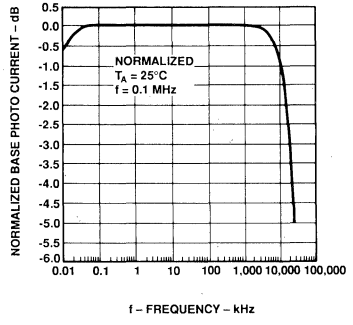


Figure 12. Normalized Base Photo Current vs. Frequency.

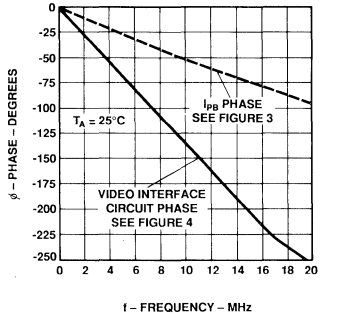


Figure 13. Phase vs. Frequency.

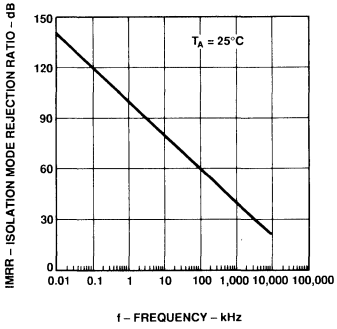


Figure 14. Isolation Mode Rejection Ratio vs. Frequency.

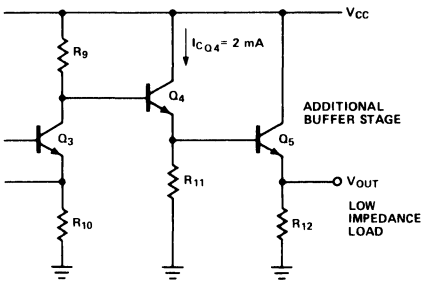


Figure 16. Output Buffer Stage for Low Impedance Loads.

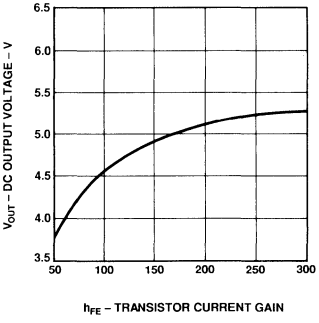


Figure 15. DC Output Voltage vs. Transistor DC Current Gain.

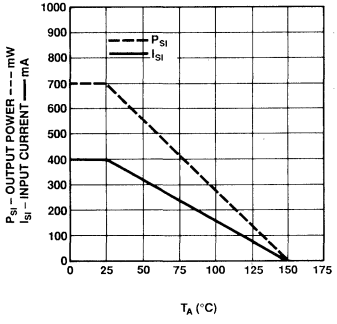


Figure 17. Dependence of Safety Maximum Ratings with Ambient Temperature.

Conversion from HCPL-4562 to CNW4562

In order to obtain similar circuit performance when converting from the HCPL-4562 to the CNW4562, it is recommended to increase the Quiescent Input Current, I_{FQ}, from 6 mA to 10 mA. If the application circuit in Figure 4 is used, then potentiometer R4 should be adjusted appropriately.

Design Considerations of the Application Circuit

The application circuit in Figure 4 incorporates several features that help maximize the bandwidth performance of the CNW4562. Most important of these features is peaked response of the detector circuit that helps extend the frequency range over which the voltage gain is relatively constant. The number of gain stages, the overall circuit topology, and the choice of DC bias points are all consequences of the desire to maximize bandwidth performance.

To use the circuit, first select R_1 to set V_E for the desired LED quiescent current by:

$$I_{FQ} = \frac{V_E}{R_4} \cong \frac{G_V V_E R_{10}}{(\partial I_{PB}/\partial I_F) R_7 R_9} \quad (1)$$

For a constant value $v_{IN_{P-P}}$, the circuit topology (adjusting the gain with R_4) preserves linearity by keeping the modulation factor (MF) dependent only on V_E.

$$i_{F_{p-p}} \cong v_{IN}/R_4 \quad (2)$$

$$\frac{i_{F_{p-p}}}{I_{FQ}} \cong \frac{i_{PB_{p-p}}}{I_{PBQ}} = \frac{v_{IN_{p-p}}}{V_E} \quad (3)$$

$$\text{Modulation Factor (MF):} \quad \frac{i_{F_{(p-p)}}}{2 I_{FQ}} \cong \frac{v_{IN_{p-p}}}{2 V_E} \quad (4)$$

For a given G_V, V_E, and V_{CC}, DC output voltage will vary only with h_{FEX}.

$$V_O = V_{CC} - V_{BE_4} - \frac{R_9}{R_{10}} (V_{BEX} - (I_{PBQ} - I_{BXQ}) R_7) \quad (5)$$

Where:

$$I_{PBQ} \cong \frac{G_V V_E R_{10}}{R_7 R_9} \quad (6)$$

and,

$$I_{BXQ} \cong \frac{V_{CC} - 2 V_{BE}}{R_6 h_{FEX}} \quad (7)$$

Figure 15 shows the dependency of the DC output voltage on h_{FEX}.

For 9 V < V_{CC} < 12 V, select the value of R_{11} such that

$$I_{C_{Q4}} \cong \frac{V_O}{R_{11}} \leq \frac{4.25V}{470\Omega} \leq 9.0\,mA \quad (8)$$

The voltage gain of the second stage (Q_3) is approximately equal to:

$$\frac{R_9}{R_{10}} * \frac{1}{1 + s R_9 \left[C_{CQ_3} + \frac{1}{2\pi R'_{11} f_{T_4}} \right]} \quad (9)$$

Increasing R'_{11} (R'_{11} includes the parallel combination of R_{11} and the load impedance) or reducing R_9 (keeping R_9/R_{10} ratio constant) will improve the bandwidth.

If it is necessary to drive a low impedance load, bandwidth may also be preserved by adding an additional emitter following the buffer stage (Q_5 in Figure 16), in which case R_{11} can be increased to set $I_{CQ4} \cong 2$ mA.

Finally, adjust R_4 to achieve the desired voltage gain.

$$G_V \cong \frac{v_{OUT}}{v_{IN}} \cong \frac{\partial I_{PB}}{\partial I_F} \left[\frac{R_7 R_9}{R_4 R_{10}} \right] \quad (10)$$

$$\text{where typically } \frac{\partial I_{PB}}{\partial I_F} = 0.0032$$

Definition:

G_V = Voltage Gain
I_{FQ} = Quiescent LED forward current
$i_{Fp\text{-}p}$ = Peak-to-peak small signal LED forward current
$v_{INp\text{-}p}$ = Peak-to-peak small signal input voltage
$i_{PBp\text{-}p}$ = Peak-to-peak small signal base photo current
I_{PBQ} = Quiescent base photo current
V_{BEX} = Base-Emitter voltage of CNW4562 transistor
I_{BXQ} = Quiescent base current of CNW4562 transistor
h_{FEX} = Current Gain (IC/IB) of CNW4562 transistor
V_E = Voltage across emitter degeneration resistor R_4
f_{T_4} = Unity gain frequency of Q_5
C_{CQ_3} = Effective capacitance from collector of Q_3 to ground

HEWLETT PACKARD

AC/DC to Logic Interface Optocoupler

Technical Data

HCPL-3700
HCPL-3760

Features

- **Standard and Low Input Current (HCPL-3760) Versions**
- **AC or DC Input**
- **Programmable Sense Voltage**
- **Hysteresis**
- **Logic Compatible Output**
- **Thresholds Guaranteed Over Temperature**
- **Thresholds Independent of LED Degradation**
- **Recognized Under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 VAC, 1 Minute**
- **CSA Approved**

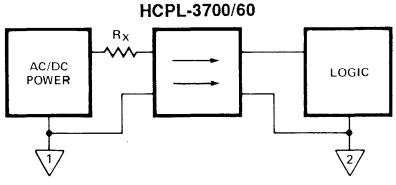
Applications

- **Limit Switch Sensing**
- **Low Voltage Detector**
- **5 V-240 V AC/DC Voltage Sensing**
- **Relay Contact Monitor**
- **Relay Coil Voltage Monitor**
- **Current Sensing**
- **Microprocessor Interfacing**

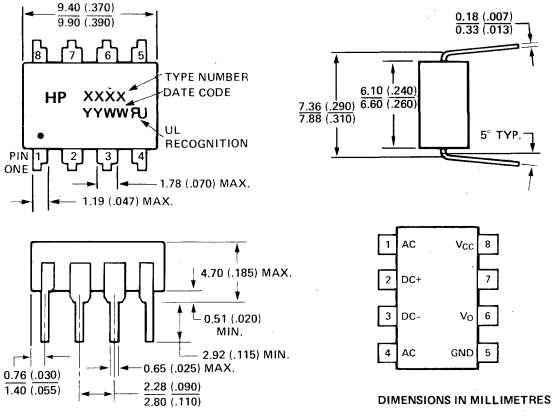
Description

The HCPL-3700 and HCPL-3760 are voltage/current threshold detection optocouplers. The HCPL-3760 is a low-current version of the HCPL-3700. To obtain lower current operation, the HCPL-3760 uses a high-efficiency AlGaAs LED which provides higher light output at lower drive currents. Both devices utilize threshold sensing input buffer ICs which permit control of threshold levels over a wide range of input voltages with a single external resistor.

The input buffer incorporates several features: hysteresis for extra noise immunity and switching immunity, a diode bridge for easy use with ac input signals, and internal clamping diodes to protect the buffer and LED from a wide range of over-voltage and over-current transients. Because



Outline Drawing



DIMENSIONS IN MILLIMETRES AND (INCHES).

OPTO COUPLERS

threshold sensing is done prior to driving the LED, variations in optical coupling from the LED to the detector will have no effect on the threshold levels.

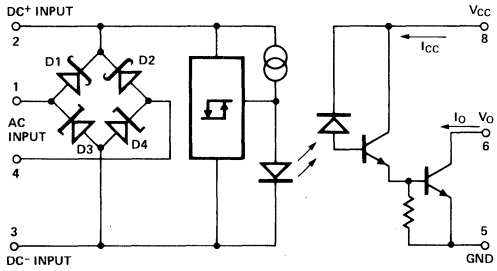
The HCPL-3700's input buffer IC has a nominal turn on threshold of 2.5 mA (I_{TH} +) and 3.7 volts (V_{TH} +).

The buffer IC for the HCPL-3760 was redesigned to permit a lower input current. The nominal turn on threshold for the HCPL-3760 is 1.2 mA (I_{TH} +) and 3.7 volts (V_{TH} +).

The high gain output stage features an open collector output providing both TTL compatible saturation voltages and CMOS compatible break-down voltages.

By combining several unique functions in a single package, the user is provided with an ideal component for industrial control computer input boards and other applications where a predetermined input threshold level is desirable.

Schematic



Absolute Maximum Ratings (No derating required up to 70°C)

Parameter		Symbol	Min.	Max.	Units	Note
Storage Temperature		T_S	-55	125	°C	
Operating Temperature		T_A	-40	85	°C	
Lead Soldering Cycle	Temperature			260	°C	1
	Time			10	sec	
Input Current	Average	I_{IN}		50	mA	2
	Surge			140		2, 3
	Transient			500		
Input Voltage (Pins 2-3)		V_{IN}	-0.5		V	
Input Power Dissipation		P_{IN}		230	mW	4
Total Package Power Dissipation		P		305	mW	5
Output Power Dissipation		P_O		210	mW	6
Output Current	Average	I_O		30	mA	7
Supply Voltage (Pins 8-5)		V_{CC}	-0.5	20	V	
Output Voltage (Pins 6-5)		V_O	-0.5	20	V	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Supply Voltage	V_{CC}	2	18	V	
Operating Temperature	T_A	0	70	°C	
Operating Frequency	f	0	4	KHz	8

Electrical Specifications

Over Recommended Temperature T_A = 0°C to 70°C, Unless Otherwise Specified.

Parameter		Sym.	Device	Min.	Typ.[9]	Max.	Units	Conditions	Fig.	Note
Input Threshold Current		I_{TH+}	HCPL-3700	1.96	2.5	3.11	mA	$V_{IN} = V_{TH+}$; V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 4.2 mA	2, 3	14
			HCPL-3760	0.87	1.2	1.56				
		I_{TH-}	HCPL-3700	1.00	1.3	1.62		$V_{IN} = V_{TH-}$; V_{CC} = 4.5 V; V_O = 2.4 V; $I_{OH} \leq$ 100 µA		
			HCPL-3760	0.43	0.6	0.80				
Input Threshold Voltage	DC (Pins 2, 3)	V_{TH+}		3.35	3.7	4.05	V	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 4.2 mA		
		V_{TH-}		2.01	2.6	2.86	V	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 100 µA		
	AC (Pins 1, 4)	V_{TH+}		4.23	4.9	5.50	V	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 4.2 mA		14, 15
		V_{TH-}		2.87	3.7	4.20	V	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 100 µA		
Hysteresis		I_{HYS}	HCPL-3700		1.2		mA	$I_{HYS} = I_{TH+} - I_{TH-}$	2	
			HCPL-3760		0.6					
		V_{HYS}			1.2		V	$V_{HYS} = V_{TH+} - V_{TH-}$		
Input Clamp Voltage		V_{IHC1}		5.4	6.0	6.6	V	$V_{IHC1} = V_2 - V_3$; V_3 = GND; I_{IN} = 10 mA; Pin 1 & 4 Connected to Pin 3	1	
		V_{IHC2}		6.1	6.7	7.3	V	$V_{IHC2} = \lvert V_1 - V_4 \rvert$; $\lvert I_{IN} \rvert$ = 10 mA; Pins 2 & 3 Open		
		V_{IHC3}			12.0	13.4	V	$V_{IHC3} = V_2 - V_3$; V_3 = GND; I_{IN} = 15 mA; Pins 1 & 4 Open		
		V_{ILC}			-0.76		V	$V_{ILC} = V_2 - V_3$; V_3 = GND; I_{IN} = -10 mA		
Input Current		I_{IN}	HCPL-3700	3.0	3.7	4.4	mA	$V_{IN} = V_2 - V_3$ = 5.0 V Pins 1 & 4 Open	5	
			HCPL-3760	1.5	1.8	2.2				
Bridge Diode Forward Voltage		$V_{D1,2}$	HCPL-3700		0.59		V	I_{IN} = 3 mA		
			HCPL-3760		0.51			I_{IN} = 1.5 mA		
		$V_{D3,4}$	HCPL-3700		0.74			I_{IN} = 3 mA		
			HCPL-3760		0.71			I_{IN} = 1.5 mA		

Electrical Specifications (Continued)

Parameter	Sym.	Device	Min.	Typ.[9]	Max.	Units	Conditions	Fig.	Note
Logic Low Output Voltage	V_{OL}			0.1	0.4	V	V_{CC} = 4.5 V; I_{OL} = 4.2 mA	5	14
Logic High Output Current	I_{OH}				100	µA	V_{OH} = V_{CC} = 18 V		14
Logic Low Supply Current	I_{CCL}	HCPL-3700		1.2	4	mA	V_2 – V_3 = 5.0 V; V_O = Open; V_{CC} = 5.0 V		
		HCPL-3760		0.7	3				
Logic High Supply Current	I_{CCH}			0.002	4	µA	V_{CC} = 18 V; V_O = Open	4	14
Input-Output Insulation	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 min; T_A = 25°C		16, 17
Input-Output Resistance	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 VDC		16
Input-Output Capacitance	C_{I-O}			0.6		pF	f = 1 MHz; V_{I-O} = 0 VDC		
Input Capacitance	C_{IN}			50		pF	f = 1 MHz; V_{IN} = 0 V, Pins 2 & 3, Pins 1 & 4 Open		

*For JEDEC registered parts.

Switching Specifications

T_A = 25°C, V_{CC} = 5.0 V Unless Otherwise Specified

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	HCPL-3700		4.0	15.0	µs	R_L = 4.7 kΩ, C_L = 30 pF	6, 9	10
		HCPL-3760		4.5					
Propagation Delay Time to Logic High at Output	t_{PLH}	HCPL-3700		10.0	40.0	µs	R_L = 4.7 kΩ, C_L = 30 pF		11
		HCPL-3760		8.0					
Output Rise Time (10-90%)	t_r	HCPL-3700		20		µs	R_L = 4.7 kΩ, C_L = 30 pF	7	
		HCPL-3760		14					
Output Fall Time (90-10%)	t_f	HCPL-3700		0.3		µs	R_L = 4.7 kΩ, C_L = 30 pF		
		HCPL-3760		0.4					
Common Mode Transient Immunity at Logic Low Output	$\|CM_H\|$			4000		V/µs	I_{IN} = 0 mA, R_L = 4.7 kΩ, $V_{O\,min}$ = 2.0 V, V_{CM} = 1400 V	8, 10	12, 13
Common Mode Transient Immunity at Logic High Output	$\|CM_L\|$	HCPL-3700		600		V/µs	I_{IN} = 3.11 mA; R_L = 4.7 kΩ, $V_{O\,max}$ = 0.8 V, V_{CM} = 140 V		
		HCPL-3760					I_{IN} = 1.56 mA; R_L = 4.7 kΩ, $V_{O\,max}$ = 0.8 V, V_{CM} = 140 V		

Notes:

1. Measured at a point 1.6 mm below seating plane.
2. Current into/out of any single lead.
3. Surge input current duration is 3 ms at 120 Hz pulse repetition rate. Transient input current duration is 10 μs at 120 Hz pulse repetition rate. Note that maximum input power, P_{IN}, must be observed.
4. Derate linearly above 70°C free-air temperature at a rate of 4.1 mW/°C. Maximum input power dissipation of 230 mW allows an input IC junction temperature of 125°C at an ambient temperature of T_A = 70°C with a typical thermal resistance from junction to ambient of θ_{JA1} = 240°C W. Excessive P_{IN} and T_J may result in IC chip degradation.
5. Derate linearly above 70°C free-air temperature at a rate of 5.4 mW/°C.
6. Derate linearly above 70°C free-air temperature at a rate of 3.9 mW/°C. Maximum output power dissipation of 210 mW allows an output IC junction temperature of 125°C at an ambient temperature of T_A = 70°C with a typical thermal resistance from junction to ambient of θ_{JA0} = 265°C/W.
7. Derate linearly above 70°C free-air temperature at a rate of 0.6 mA/°C.
8. Maximum operating frequency is defined when output waveform Pin 6 obtains only 90% of V_{CC} with R_L = 4.7 kΩ, C_L = 30 pF using a 5 V square wave input signal.
9. All typical values are at T_A = 25°C, V_{CC} = 5.0 V unless otherwise stated.
10. The t_{PHL} propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 μs rise time) to the 1.5 V level on the leading edge of the output pulse (see Figure 9).
11. The t_{PLH} propagation delay is measured from the 2.5 V level of the trailing edge of a 5.0 V input pulse (1 μs fall time) to the 1.5 V level on the trailing edge of the output pulse (see Figure 9).
12. Common mode transient immunity in Logic High level is the maximum tolerable (positive) $dV_{CM/dt}$ on the leading edge of the common mode pulse, V_{CM}, to insure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) $dV_{CM/dt}$ on the trailing edge of the common mode pulse signal, V_{CM}, to insure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V). See Figure 10.
13. In applications where $dV_{CM/dt}$ may exceed 50,000 V/μs (such as static discharge), a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value for R_{CC} is 240Ω per volt of allowable drop in V_{CC} (between Pin 8 and V_{CC}) with a minimum value of 240Ω.
14. Logic low output level at Pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH-}$ once V_{IN} has exceeded V_{TH+}. Logic high output level at Pin 6 occurs under the conditions of $V_{IN} \leq V_{TH-}$ as well as the range of $V_{IN} < V_{TH+}$ once V_{IN} has decreased below V_{TH-}.
15. AC voltage is instantaneous voltage.
16. Device considered a two terminal device: Pins 1, 2, 3, 4 connected together, and Pins 5, 6, 7, 8 connected together.
17. In accordance with UL 1755, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ μA).

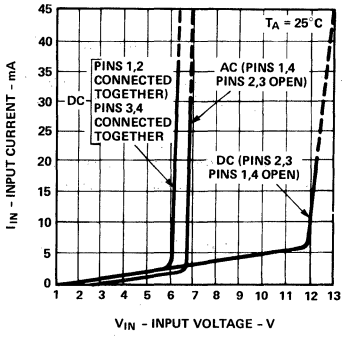
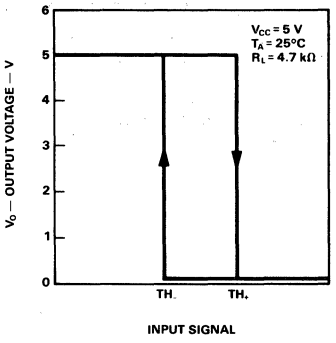
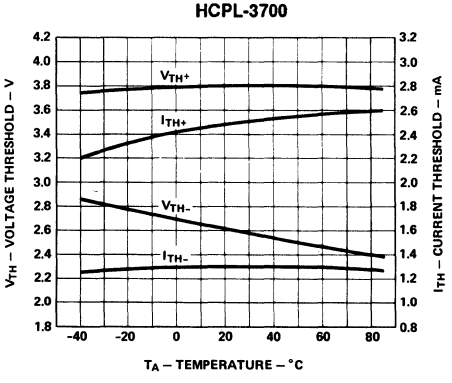


Figure 1. Typical Input Characteristics, I_{IN} vs. V_{IN} (AC Voltage is Instantaneous Value).



	DEVICE	TH_+	TH_-	INPUT CONNNECTION
I_{TH}	HCPL-3700	2.5 mA	1.3 mA	PINS 2, 3
	HCPL-3760	1.2 mA	0.6 mA	OR 1, 4
$V_{TH(dc)}$	BOTH	3.7 V	2.6 V	PINS 2, 3
$V_{TH(ac)}$	BOTH	4.9 V	3.8 V	PINS 1, 4

Figure 2. Typical Transfer Characteristics.



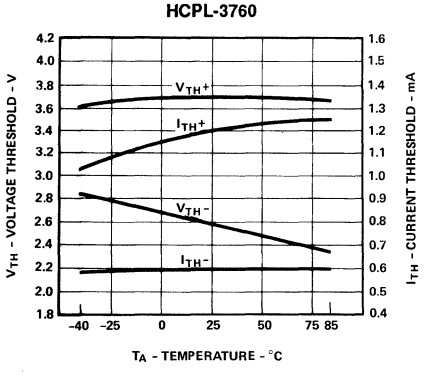


Figure 3. Typical DC Threshold Levels vs. Temperature.

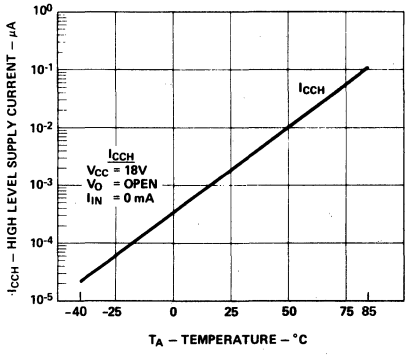


Figure 4. Typical High Level Supply Current, I_{CCH} vs. Temperature.

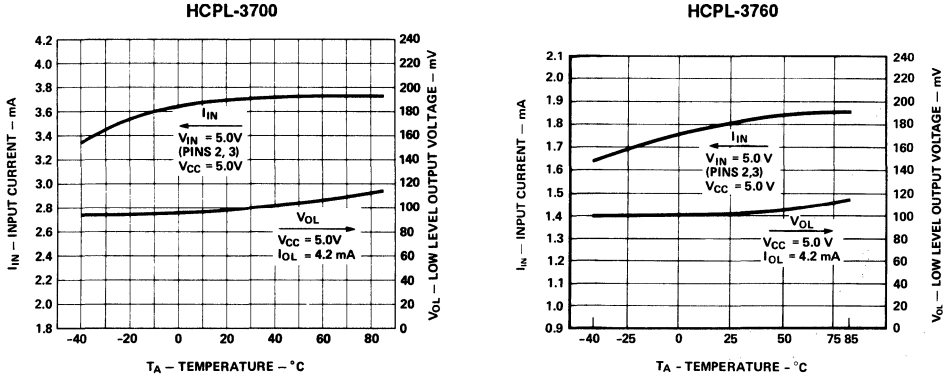


Figure 5. Typical Input Current, I_{IN}, and Low Level Output Voltage, V_{OL}, vs. Temperature.

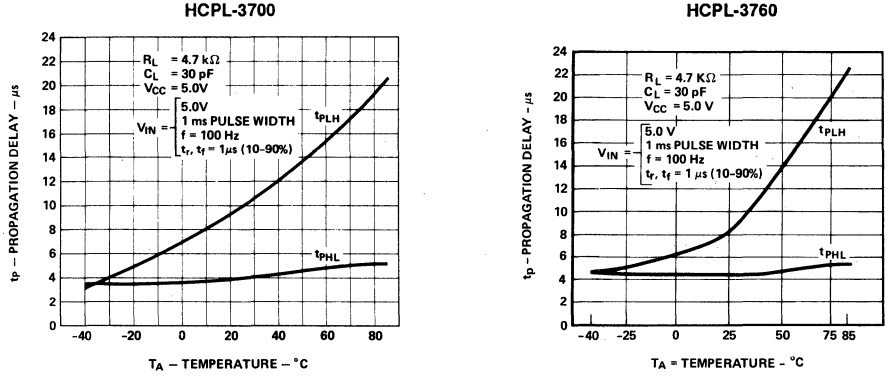


Figure 6. Typical Propagation Delay vs. Temperature.

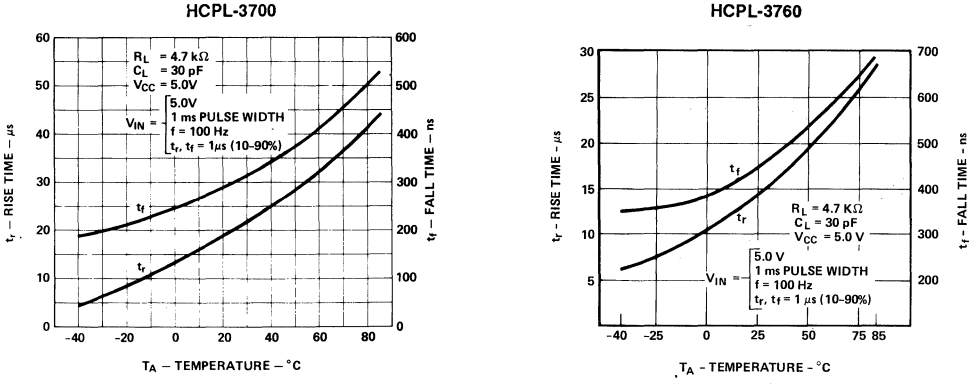


Figure 7. Typical Rise, Fall Times vs. Temperature.

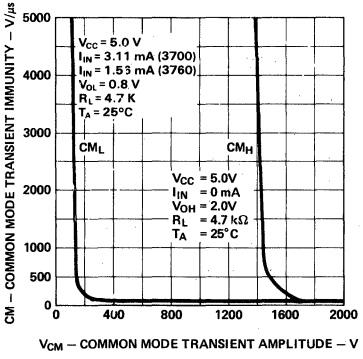


Figure 8. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

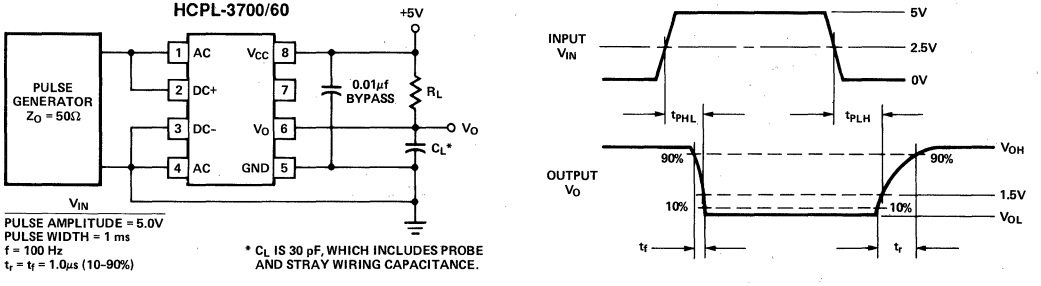


Figure 9. Switching Test Circuit.

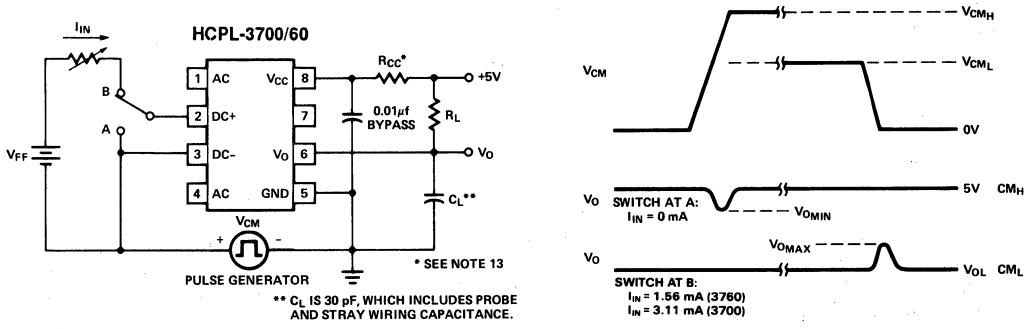


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

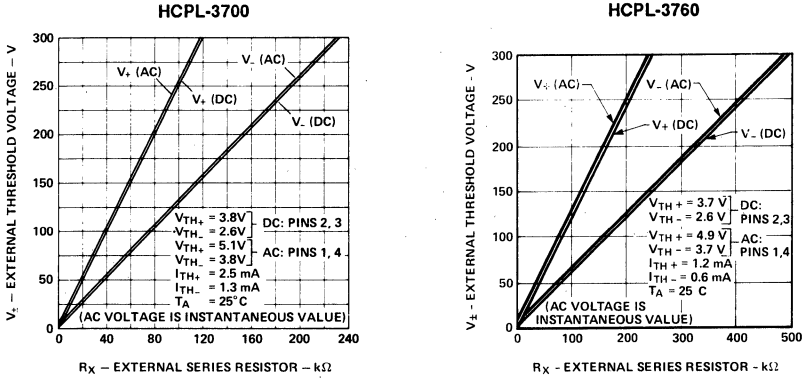


Figure 11. Typical External Threshold Characteristics, V± vs. R_X.

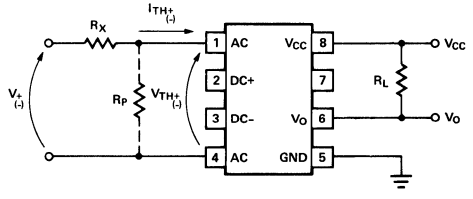


Figure 12. External Threshold Voltage Level Selection.

Electrical Considerations

The HCPL-3700/3760 optocouplers have internal temperature compensated, predictable voltage and current threshold points which allow selection of an external resistor, R_X, to determine larger external threshold voltage levels. For a desired external threshold voltage, $V_{\pm}$, a corresponding typical value of R_X can be obtained from Figure 11. Specific calculation of R_X can be obtained from Equation (1). Specification of both V_+ and V_- voltage threshold levels simultaneously can be obtained by the use of R_x and R_p as shown in Figure 12 and determined by Equations (2) and (3).

R_X can provide over-current transient protection by limiting input current during a transient condition. For monitoring contacts of a relay or switch, the HCPL-3700/3760 in combination with R_x and R_p can be used to allow a specific current to be conducted through the contacts for cleaning purposes (wetting current).

The choice of which input voltage clamp level to choose depends upon the application of this device (see Figure 1). It is recommended that the low clamp condition be used when possible. The low clamp condition in conjunction with the low input current feature will ensure extremely low input power dissipation.

In applications where $dV_{CM/dt}$ may be extremely large (such as static discharge), a series resistor, R_{CC}, should be connected in series with V_{CC} and Pin 8 to protect the detector IC from destructively high surge currents. See Note 13 for determination of R_{CC}. In addition, it is recommended that a ceramic disc bypass capacitor of 0.01 µf be placed between Pins 8 and 5 to reduce the effect of power supply noise.

For interfacing AC signals to TTL systems, output low pass filtering can be performed with a pullup resistor of 1.5 kΩ and 20 µf capacitor. This application requires a Schmitt trigger gate to avoid slow rise time chatter problems. For AC input applications, a filter capacitor can be placed across the DC input terminals for either signal or transient filtering.

Either AC (Pins 1, 4) or DC (Pins 2, 3) input can be used to determine external threshold levels.

For one specifically selected external threshold voltage level V_+ or V_-, R_x can be determined without use of R_p via

$$R_X = \frac{V_{+(-)} - V_{TH+(-)}}{I_{TH+(-)}} \quad (1)$$

For two specifically selected external threshold voltage levels, V_+ and V_-, the use of R_X and R_p will permit this selection via equations (2), (3) provided the following conditions are met. If the denominator of equation (2) is positive, then

$$\frac{V_+}{V_-} \geq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}}$$

Conversely, if the denominator of equation (2) is negative, then

$$\frac{V_+}{V_-} \leq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} > \frac{I_{TH+}}{I_{TH-}}$$

$$R_X = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_{TH-}) - I_{TH-}(V_{TH+})} \quad (2)$$

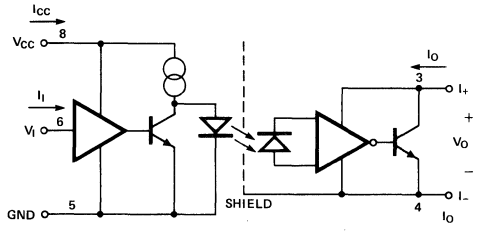
$$R_p = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_- - V_{TH-}) + I_{TH-}(V_{TH+} - V_+)} \quad (3)$$

HEWLETT PACKARD

OPTICALLY COUPLED 20 mA CURRENT LOOP TRANSMITTER

HCPL-4100

SCHEMATIC

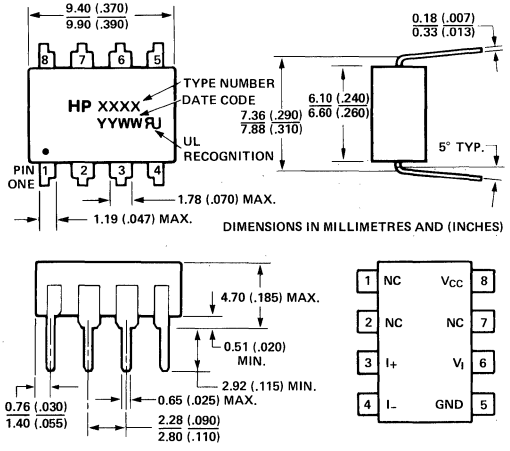


TRUTH TABLE (POSITIVE LOGIC)*

V_I	V_{CC}	I_O
H	ON	H
L	ON	L
H	OFF	H
L	OFF	H

*CURRENT LOOP CONVENTION — H = MARK: $I_O \geq 12$ mA, L = SPACE: $I_O \leq 2$ mA.

OUTLINE DRAWING*



Features

- **GUARANTEED 20 mA LOOP PARAMETERS**
- **DATA INPUT COMPATIBLE WITH LSTTL, TTL AND CMOS LOGIC**
- **GUARANTEED PERFORMANCE OVER TEMPERATURE (0°C TO 70°C)**
- **INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION**
- **20 KBaud DATA RATE AT 400 METRES LINE LENGTH**
- **GUARANTEED ON AND OFF OUTPUT CURRENT LEVELS**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **CSA APPROVED**
- **OPTICALLY COUPLED 20 mA CURRENT LOOP RECEIVER, HCPL-4200, ALSO AVAILABLE.**

Applications

- **IMPLEMENT AN ISOLATED 20 mA CURRENT LOOP TRANSMITTER IN:**
  - **Computer Peripherals**
  - **Industrial Control Equipment**
  - **Data Communications Equipment**

Description

The HCPL-4100 optocoupler is designed to operate as a transmitter in equipment using the 20 mA current loop. 20 mA current loop systems conventionally signal a logic high state by transmitting 20 mA of loop current (MARK), and signal a logic low state by allowing no more than a few milliamperes of loop current (SPACE). Optical coupling of the signal from the logic input to the 20 mA current loop breaks ground loops and provides very high immunity to common mode interference.

The HCPL-4100 data input is compatible with LSTTL, TTL, and CMOS logic gates. The input integrated circuit drives a GaAsP LED. The light emitted by the LED is sensed by a second integrated circuit that allows 20 mA to pass with a voltage drop of less than 2.7 volts when no light is emitted and allows less than 2 mA to pass when light is emitted. The transmitter output is capable of withstanding 27 volts. The input integrated circuit provides a controlled amount of LED drive current and takes into account LED light output degradation. The internal shield allows a guaranteed 1000 V/μs common mode transient immunity.

OPTO COUPLERS

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Input Voltage Low	V_{IL}	0	0.8	Volts
Input Voltage High	V_{IH}	2.0	20	Volts
Operating Temperature	T_A	0	70	°C
Output Voltage	V_O	0	27	Volts
Output Current	I_O	0	24	mA

Absolute Maximum Ratings

(No Derating Required up to 55° C)

Storage Temperature ..... -55° C to 125° C
Operating Temperature ..... -40° C to 85° C
Lead Solder Temperature ..... 260° C for 10 sec.
(1.6 mm below seating plane)
Supply Voltage — V_{CC} ..... 0 to 20 V
Average Output Current — I_O ..... -30 mA to 30 mA
Peak Output Current — I_O ..... internally limited
Output Voltage — V_O ..... -0.4 V to 27 V
Input Voltage — V_I ..... -0.5 V to 20 V
Input Power Dissipation — P_I ..... 265 mW[1]
Output Power Dissipation — P_O ..... 125 mW[2]
Total Power Dissipation — P ..... 360 mW[3]

Electrical Specifications

For 0°C ≤ T_A ≤ 70°C, 4.5 V ≤ V_{CC} ≤ 20 V, all typicals at T_A = 25°C and V_{CC} = 5 V unless otherwise noted. See note 12.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Mark State Output Voltage	V_{MO}		1.8 2.2 2.35	2.25 2.7	Volts Volts Volts	I_O = 2 mA I_O = 12 mA I_O = 20 mA	V_I = 2.0 V	1, 2	
Mark State Short Circuit Output Current	I_{SC}	30	85		mA	V_I = 2 V, V_O = 5 V to 27 V			4
Space State Output Current	I_{SO}	0.5	1.1	2.0	mA	V_I = 0.8 V, V_O = 27 V		3	
Low Level Input Current	I_{IL}		-0.12	-0.32	mA	V_{CC} = 20 V, V_I = 0.4 V			
Low Level Input Voltage	V_{IL}			0.8	Volts				
High Level Input Voltage	V_{IH}	2.0			Volts				
High Level Input Current	I_{IH}		 0.005	20 100 250	μA μA μA	V_I = 2.7 V V_I = 5.5 V V_I = 20 V			
Supply Current	I_{CC}		7.0 7.8	11.5 13	mA mA	V_{CC} = 5.5 V V_{CC} = 20 V	0 V ≤ V_I ≤ 20 V		
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	R_H ≤ 50%, t = 1 min. T_A = 25°C			5, 13
Resistance (input-output)	R_{I-O}		10^{12}		Ohms	V_{I-O} = 500 V dc			5
Capacitance (input-output)	C_{I-O}		1		pF	f = 1 MHz, V_{I-O} = 0 V dc			5

Notes:
1. Derate linearly above 55° C free air temperature at a rate of 3.8 mW/° C. Proper application of the derating factors will prevent IC junction temperatures from exceeding 125° C for ambient temperatures up to 85° C.
2. Derate linearly above a free-air temperature of 70° C at a rate of 2.3 mW/° C. A significant amount of power may be dissipated in the HCPL-4100 output circuit during the transition from the SPACE state to the MARK state when driving a data line or capacitive load (C_{OUT}). The average power dissipation during the transition can be estimated from the following equation which assumes a linear discharge of a capacitive load: $P = I_{SC}(V_{SO} + V_{MO})/2$, where V_{SO} is the output voltage in the SPACE state. The duration of this transition can be estimated as $t = C_{OUT}(V_{SO} - V_{MO})/I_{SC}$. For typical applications driving twisted pair data lines with NRZ data as shown in Figure 11, the transition time will be less than 10% of one bit time.
3. Derate linearly above 55° C free-air temperature at a rate of 5.1 mW/° C.
4. The maximum current that will flow into the output in the mark state (I_{SC}) is internally limited to protect the device. The duration of the output short circuit shall not exceed 10 ms.
5. The device is considered a two terminal device, pins 1, 2, 3, and 4 are connected together, and pins 5, 6, 7, and 8 are connected together.

Switching Specifications

for $0 \le T_A \le 70°C$, $4.5\ V \le V_{CC} \le 20\ V$, all typicals at $T_A = 25°C$ and $V_{CC} = 5\ V$ unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units	Testing Conditions	Fig.	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		0.3	1.6	μs	$C_O = 1000\ pF$, $C_L = 15\ pF$, $I_O = 20\ mA$	4, 5, 6	6
Propagation Delay Time to Logic Low Output Level	t_{PHL}		0.2	1.0	μs	$C_O = 1000\ pF$, $C_L = 15\ pF$, $I_O = 20\ mA$	4, 5, 6	7
Propagation Delay Time Skew	t_{PLH}-t_{PHL}		0.1		μs	$I_O = 20\ mA$		
Output Rise Time (10-90%)	t_r		16		ns	$I_O = 20\ mA$, $C_O = 1000\ pF$, $C_L = 15\ pF$.	5, 7	8
Output Fall Time (90-10%)	t_f		23		ns	$I_O = 20\ mA$, $C_O = 1000\ pF$, $C_L = 15\ pF$.	5, 7	9
Common Mode Transient Immunity at Logic High Output Level	$\lvert CM_H \rvert$	1,000	10,000		V/μs	$V_I = 2\ V$, $T_A = 25°C$ $V_{CM} = 50\ V$ (peak), $V_{CC} = 5\ V$ I_O (min.) = 12 mA	8, 9	10
Common Mode Transient Immunity at Logic Low Output Level	$\lvert CM_L \rvert$	1,000	10,000		V/μs	$V_I = 0.8\ V$, $T_A = 25°C$ $V_{CM} = 50\ V$ (peak), $V_{CC} = 5\ V$ I_O (max.) = 3 mA	8, 9	11

Notes:

6. The t_{PLH} propagation delay is measured from the 1.3 volt level on the leading edge of the input pulse to the 10 mA level on the leading edge of the output pulse.
7. The t_{PHL} propagation delay is measured from the 1.3 volt level on the trailing edge of the input pulse to the 10 mA level on the trailing edge of the output pulse.
8. The rise time, t_r, is measured from the 10% to the 90% level on the rising edge of the output current pulse.
9. The fall time, t_f, is measured from the 90% to the 10% level on the falling edge of the output current pulse.
10. The common mode transient immunity in the logic high level is the maximum (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, that can be sustained with the output in a Mark ("H") state (i.e., $I_O > 12\ mA$).
11. The common mode transient immunity in the logic low level is the maximum (negative) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, that can be sustained with the output in a Space ("L") state (i.e., $I_O > 3\ mA$).
12. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
13. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \le 5\ \mu A$).

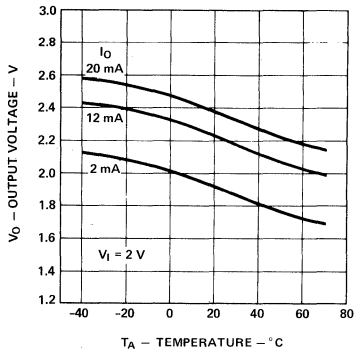


Figure 1. Typical Mark State Output Voltage vs. Temperature

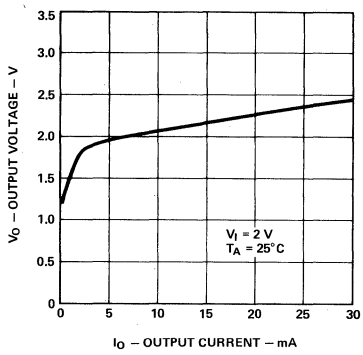


Figure 2. Typical Output Voltage vs. Output Current in Mark State

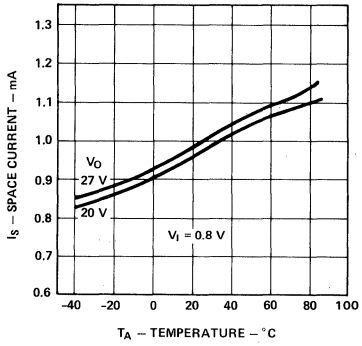


Figure 3. Typical Space State Output Current vs. Temperature

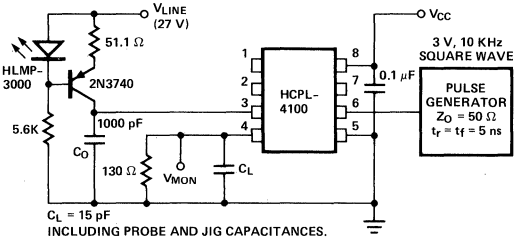


Figure 4. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

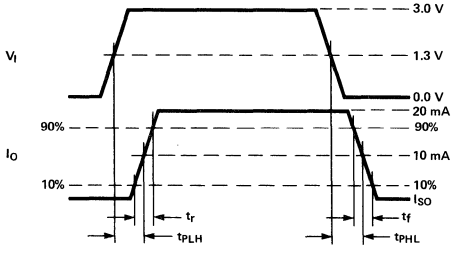


Figure 5. Waveforms for t_{PLH}, t_{PHL}, t_r, and t_f

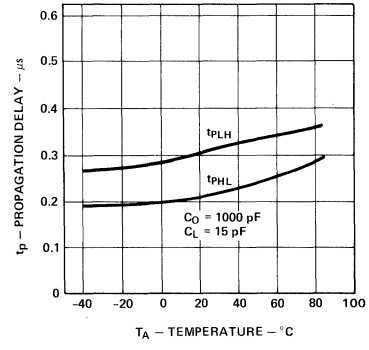


Figure 6. Typical Propagation Delay vs. Temperature

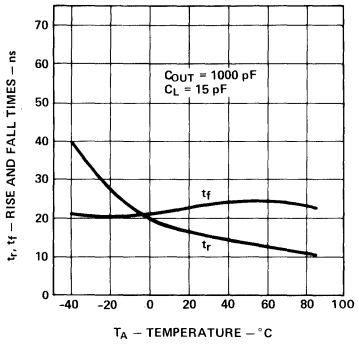


Figure 7. Typical Rise, Fall Times vs. Temperature

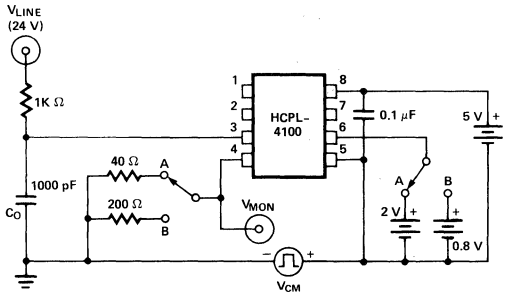


Figure 8. Test Circuit for Common Mode Transient Immunity

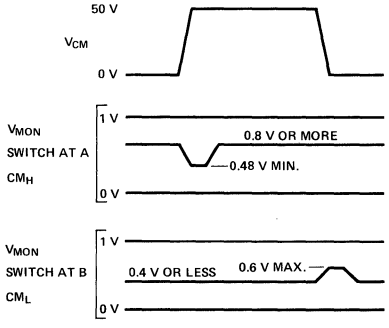


Figure 9. Typical Waveforms for Common Mode Transient Immunity

OPTO COUPLERS

Applications

Data transfer between equipment which employs current loop circuits can be accomplished via one of three configurations: simplex, half duplex or full duplex communication. With these configurations, point to point and multidrop arrangements are possible. The appropriate configuration to use depends upon data rate, number of stations, number and length of lines, direction of data flow, protocol, current source location and voltage compliance value, etc.

SIMPLEX

The simplex configuration, whether point to point or multidrop, gives unidirectional data flow from transmitter(s) to receiver. This is the simplest configuration for use in long line length (two wire), moderate data rate, and low current source compliance level applications. A block diagram of simplex point to point arrangement is given in Figure 10 for the HCPL-4100 transmitter optocoupler.

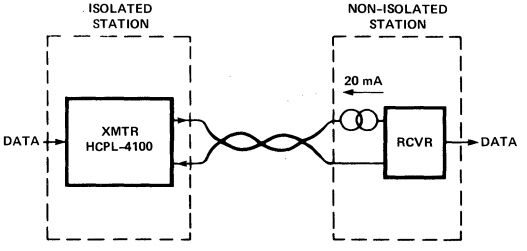


Figure 10. Simplex Point to Point Current Loop System Configuration

Major factors which limit maximum data rate performance for a simplex loop are the location and compliance voltage of the loop current source as well as the total line capacitance. Application of the HCPL-4100 transmitter in a simplex loop necessitates that a non-isolated active receiver (containing current source) be used at the opposite end of the current loop. With long line length, large line capacitance will need to be charged to the compliance voltage level of the current source before the receiver loop current decreases to zero. This effect limits upper data rate performance. Slower data rates will occur with larger compliance voltage levels. The maximum compliance level is determined by the transmitter breakdown characteristic. In addition, adequate compliance of the current source must be available for voltage drops across station(s) during the MARK state in multidrop applications for long line lengths.

In a simplex multidrop application with multiple HCPL-4100 transmitters and one non-isolated active receiver, priority of transmitters must be established.

A recommended non-isolated active receiver circuit which can be used with the HCPL-4100 in point to point or in multidrop 20 mA current loop applications is given in Figure 11. This non-isolated active receiver current threshold must be chosen properly in order to provide adequate noise immunity as well as not to detect SPACE state current (bias current) of the HCPL-4100 transmitter. The receiver input threshold current is Vth/Rth ≈ 10 mA. A simple transistor current source provides a nominal 20 mA loop current over a V_{CC} compliance range of 6 V dc to 27 V dc. A resistor can be used in place of the constant current source for simple applications where the wire loop distance and number of stations on the loop are fixed. A minimum transmitter output load capacitance of 1000 pF is required between pins 3 and 4 to ensure absolute stability.

Length of the current loop (one direction) versus minimum required DC supply voltage, V_{CC}, of the circuit in Figure 11 is graphically illustrated in Figure 12. Multidrop configurations will require larger V_{CC} than Figure 12 predicts in order to account for additional station terminal voltage drops.

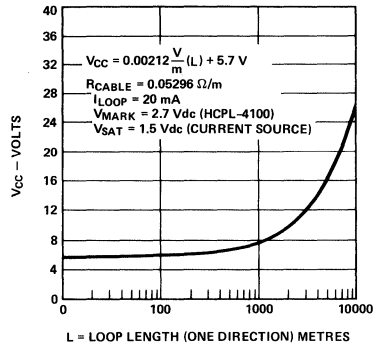


Figure 12. Miminum Required Supply Voltage, V_{CC}, vs. Loop Length for Current Loop Circuit of Figure 12

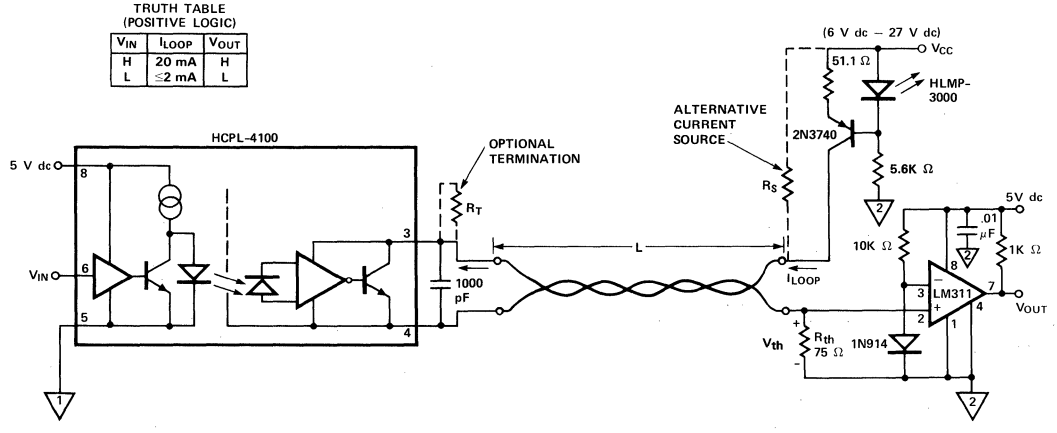


Figure 11. Recommended Non-Isolated Active Receiver with HCPL-4100 Isolated Transmitter for Simplex Point to Point 20 mA Current Loop

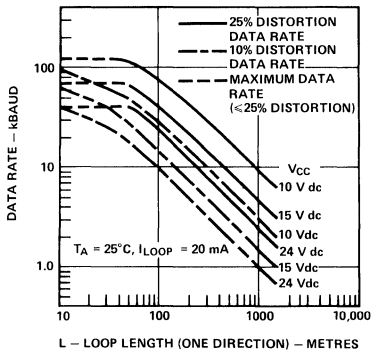


Figure 13. Typical Data Rate vs. Distance and Supply Voltage

Typical data rate performance versus distance is illustrated in Figure 13 for the combination of a non-isolated active receiver and HCPL-4100 optically coupled current loop transmitter shown in Figure 11. Curves are shown for 25% distortion data rate at different V_{CC} values. 25% distortion data rate is defined as that rate at which 25% distortion occurs to output bit interval with respect to the input bit interval. Maximum data rate (dotted line) is restricted by device characteristics. An input Non-Return-to-Zero (NRZ) test waveform of 16 bits (0000001011111101) was used for data rate distortion measurements. Enhanced speed performance of the loop system can be obtained with lower V_{CC} supply levels, as illustrated in Figure 13. In addition, when loop current is supplied through a resistor instead of by a current source, an additional series termination resistance equal to the characteristic line impedance can be used at the HCPL-4100 transmitter end to enhance speed of response by approximately 20%.

The cable used contained five pairs of unshielded, twisted, 22 AWG wire (Dearborn #862205). Loop current is 20 mA nominal. Input and output logic supply voltages are 5 V dc.

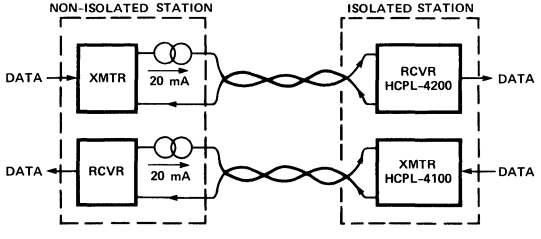


Figure 14. Full Duplex Point to Point Current Loop System Configuration

FULL DUPLEX

Full duplex point to point communication of Figure 14 uses a four wire system to provide simultaneous, bi-directional data communication between local and remote equipment. Basic application uses two simplex point to point loops which have two separate, active, non-isolated units at one common end of the loops. The other end of each loop is isolated.

As Figure 14 illustrates, the combination of Hewlett-Packard current loop optocouplers, HCPL-4100 transmitter and HCPL-4200 receiver, can be used at the isolated end of current loops. Cross talk and common mode coupling are greatly reduced when optical isolation is implemented at the same end of both loops, as shown. Full duplex data rate is limited by the non-isolated active receiver current loop. Comments mentioned under simplex configuration apply to the full duplex case. Consult the HCPL-4200 receiver optocoupler data sheet for specified device performance.

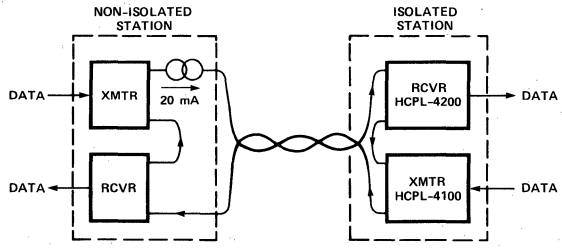
HALF DUPLEX

The half duplex configuration, whether point to point or multidrop, gives non-simultaneous bidirectional data flow from transmitters to receivers shown in Figures 15a and 15b. This configuration allows the use of two wires to carry data back and forth between local and remote units. However, protocol must be used to determine which specific transmitter can operate at any given time. Maximum data rate for a half duplex system is limited by the loop current charging time. These considerations were explained in the Simplex configuration section.

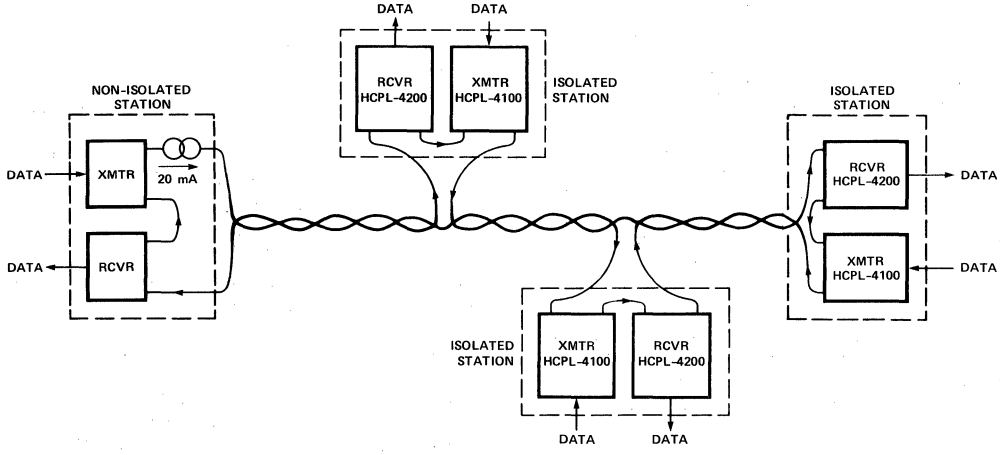
Figures 15a and 15b illustrate half duplex application for the combination of HCPL-4100/-4200 optocouplers. The unique and complementary designs of the HCPL-4100 transmitter and HCPL-4200 receiver optocouplers provide many designed-in benefits. For example, total optical isolation at one end of the current loop is easily accomplished, which results in substantial removal of common mode influences, elimination of ground potential differences and reduction of power supply requirements. With this combination of HCPL-4100/-4200 optocouplers, specific current loop noise immunity is provided, i.e., minimum SPACE state current noise immunity is 1 mA, MARK state noise immunity is 8 mA.

Voltage compliance of the current source must be of an adequate level for operating all units in the loop while not exceeding 27 V dc, the maximum breakdown voltage for the HCPL-4100. Note that the HCPL-4100 transmitter will allow output loop current to conduct when input V_{CC} power is off. Consult the HCPL-4200 receiver optocoupler data sheet for specified device performance.

For more informaton about the HCPL-4100/-4200 optocouplers, consult Application Note 1018.



(a) POINT TO POINT



(b) MULTIDROP

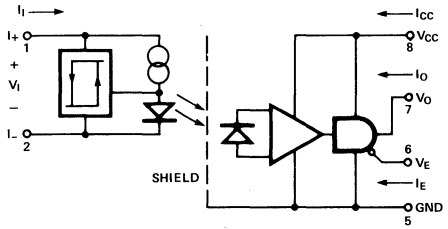
Figure 15. Half Duplex Current Loop System Configurations for (a) Point to Point, (b) Multidrop

HEWLETT PACKARD

OPTICALLY COUPLED 20 mA CURRENT LOOP RECEIVER

HCPL-4200

SCHEMATIC

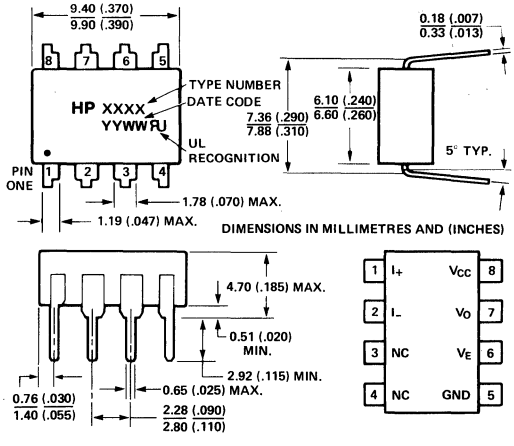


TRUTH TABLE (POSITIVE LOGIC)*

I_I	V_E	V_O
H	H	Z
L	H	Z
H	L	H
L	L	L

*CURRENT LOOP CONVENTION –
H = MARK: $I_I \geq 12$ mA,
L = SPACE: $I_I \leq 3$ mA,
Z = OFF (HIGH IMPEDANCE) STATE.

OUTLINE DRAWING*



Features

- **DATA OUTPUT COMPATIBLE WITH LSTTL, TTL AND CMOS**
- **20 K BAUD DATA RATE AT 1400 METRES LINE LENGTH**
- **GUARANTEED PERFORMANCE OVER TEMPERATURE (0°C TO 70°C)**
- **GUARANTEED ON AND OFF THRESHOLDS**
- **LED IS PROTECTED FROM EXCESS CURRENT**
- **INPUT THRESHOLD HYSTERESIS**
- **THREE-STATE OUTPUT COMPATIBLE WITH DATA BUSES**
- **INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **OPTICALLY COUPLED 20 mA CURRENT LOOP TRANSMITTER, HCPL-4100, ALSO AVAILABLE.**
- **CSA APPROVED**

Applications

- **IMPLEMENT AN ISOLATED 20 mA CURRENT LOOP RECEIVER IN:**
  - **Computer Peripherals**
  - **Industrial Control Equipment**
  - **Data Communications Equipment**

Description

The HCPL-4200 optocoupler is designed to operate as a receiver in equipment using the 20 mA Current Loop. 20 mA current loop systems conventionally signal a logic high state by transmitting 20 mA of loop current (MARK), and signal a logic low state by allowing no more than a few milliamperes of loop current (SPACE). Optical coupling of the signal from the 20 mA current loop to the logic output breaks ground loops and provides for a very high common mode rejection. The HCPL-4200 aids in the design process by providing guaranteed thresholds for logic high state and logic low state for the current loop, providing an LSTTL, TTL, or CMOS compatible logic interface, and providing guaranteed common mode rejection. The buffer circuit on the current loop side of the HCPL-4200 provides typically 0.8 mA of hysteresis which increases the immunity to common mode and differential mode noise. The buffer also provides a controlled amount of LED drive current which takes into account LED light output degradation. The internal shield allows a guaranteed 1000 V/μs common mode transient immunity.

OPTO COUPLERS

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Forward Input Current (SPACE)	I_{SI}	0	2.0	mA
Forward Input Current (MARK)	I_{MI}	14	24	mA
Operating Temperature	T_A	0	70	°C
Fan Out	N	0	4	TTL Loads
Logic Low Enable Voltage	V_{EL}	0	0.8	Volts
Logic High Enable Voltage	V_{EH}	2.0	20	Volts

Absolute Maximum Ratings

(No Derating Required up to 70° C)

Storage Temperature ..... —55° C to 125° C
Operating Temperature ..... —40° C to 85° C
Lead Solder Temperature ..... 260° C for 10 sec.
(1.6 mm below the seating plane)
Supply Voltage — V_{CC} ..... 0 V to 20 V
Average Input Current — I_I ..... —30 mA to 30 mA
Peak Transient Input Current — I_I ..... 0.5 A[1]
Enable Input Voltage — V_E ..... —0.5 V to 20 V
Output Voltage — V_O ..... —0.5 V to 20 V
Average Output Current — I_O ..... 25 mA
Input Power Dissipation — P_I ..... 90 mW[2]
Output Power Dissipation — P_O ..... 210 mW[3]
Total Power Dissipation — P ..... 255 mW[4]

Electrical Specifications

For 0°C ≤ T_A ≤ 70°C, 4.5 V ≤ V_{CC} ≤ 20 V, V_E = 0.8 V, all typicals at T_A = 25°C and V_{CC} = 5 V unless otherwise noted. See note 13.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Mark State Input Current	I_{MI}	12			mA			1, 2, 3	
Mark State Input Voltage	V_{MI}		2.52	2.75	Volts	I_I = 20 mA	V_E = Don't Care	3, 4	
Space State Input Current	I_{SI}			3	mA			1, 2, 3	
Space State Input Voltage	V_{SI}		1.6	2.2	Volts	I_I = 0.5 to 2.0 mA	V_E = Don't Care	1, 3	
Input Hysteresis Current	I_{HYS}	0.3	0.8		mA			1	
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads)	I_I = 3 mA	5	
Logic High Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -2.6 mA,	I_I = 12 mA	6	
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	μA	V_O = 5.5 V	I_I = 20 mA		
				500	μA	V_O = 20 V	V_{CC} = 4.5 V		
Logic High Enable Voltage	V_{EH}	2.0			Volts				
Logic Low Enable Voltage	V_{EL}			0.8	Volts				
Logic High Enable Current	I_{EH}			20	μA	V_E = 2.7 V			
				100	μA	V_E = 5.5 V			
			.004	250	μA	V_E = 20 V			
Logic Low Enable Current	I_{EL}			-0.32	mA	V_E = 0.4 V			
Logic Low Supply Current	I_{CCL}		4.5	6.0	mA	V_{CC} = 5.5 V	I_I = 0 mA		
			5.25	7.5	mA	V_{CC} = 20 V	V_E = Don't Care		
Logic High Supply Current	I_{CCH}		2.7	4.5	mA	V_{CC} = 5.5 V	I_I = 20 mA		
			3.1	6.0	mA	V_{CC} = 20 V	V_E = Don't Care		
High Impedance State Output Current	I_{OZL}			-20	μA	V_O = 0.4 V	V_E = 2.0 V, I_I = 20 mA		
	I_{OZH}			20	μA	V_O = 2.4 V	V_E = 2 V, I_I = 0 mA		
				100	μA	V_O = 5.5 V			
				500	μA	V_O = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	V_O = V_{CC} = 5.5 V	I_I = 0 mA		
		40			mA	V_O = V_{CC} = 20 V			5
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5 V	I_I = 20 mA		5
		-25			mA	V_{CC} = 20 V	V_O = GND		
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	R_H ≤ 50%, t = 1 min. T_A = 25°C			6, 14
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 V dc			6
Input-Output Capacitance	C_{I-O}		1.0		pF	f = 1 MHz, V_{I-O} = 0 V dc			6
Input Capacitance	C_{IN}		120		pF	f = 1 MHz, V_I = 0 V dc, Pins 1 and 2			

Switching Specifications

For $0°C \leq T_A \leq 70°C$, $4.5\ V \leq V_{CC} \leq 20\ V$, $V_E = 0.8\ V$, all typicals at $T_A = 25°C$ and $V_{CC} = 5\ V$ unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		0.23	1.6	μs	$V_E = 0\ V$, $C_L = 15\ pF$	7, 8, 9	7
Propagation Delay Time to Logic Low Output Level	t_{PHL}		0.17	1.0	μs	$V_E = 0\ V$, $C_L = 15\ pF$	7, 8, 9	8
Propagation Delay Time Skew	t_{PLH}-t_{PHL}		60		ns	$I_I = 20\ mA$, $C_L = 15\ pF$	7, 8, 9	
Output Enable Time to Logic Low Level	t_{PZL}		25		ns	$I_I = 0\ mA$, $C_L = 15\ pF$	11, 12, 14	
Output Enable Time to Logic High Level	t_{PZH}		28		ns	$I_I = 20\ mA$, $C_L = 15\ pF$	11, 12, 13	
Output Disable Time from Logic Low Level	t_{PLZ}		60		ns	$I_I = 0\ mA$, $C_L = 15\ pF$	11, 12, 14	
Output Disable Time from Logic High Level	t_{PHZ}		105		ns	$I_I = 20\ mA$, $C_L = 15\ pF$	11, 12, 13	
Output Rise Time (10-90%)	t_r		55		ns	$V_{CC} = 5\ V$, $C_L = 15\ pF$	7, 8, 10	9
Output Fall Time (90-10%)	t_f		15		ns	$V_{CC} = 5\ V$, $C_L = 15\ pF$	7, 8, 10	10
Common Mode Transient Immunity at Logic High Output Level	$\|CM_H\|$	1,000	10,000		V/μs	$V_{CM} = 50\ V$ (peak) $I_I = 12\ mA$, $T_A = 25°C$	15, 16	11
Common Mode Transient Immunity at Logic Low Output Level	$\|CM_L\|$	1,000	10,000		V/μs	$V_{CM} = 50\ V$ (peak) $I_I = 3\ mA$, $T_A = 25°C$	15, 16	12

NOTES:

1. ≤ 1 μs pulse width, 300 pps.
2. Derate linearly above 70° C free air temperature at a rate of 1.6 mW/° C. Proper application of the derating factors will prevent IC junction temperatures from exceeding 125° C for ambient temperatures up to 85° C.
3. Derate linearly above 70° C free air temperature at a rate of 3.8 mW/° C.
4. Derate linearly above 70° C free air temperature at a rate of 4.6 mW/° C.
5. Duration of output short circuit time shall not exceed 10 ms.
6. The device is considered a two terminal device, pins 1, 2, 3, and 4 are connected together and pins 5, 6, 7, and 8 are connected together.
7. The t_{PLH} propagation delay is measured from the 10 mA level on the leading edge of the input pulse to the 1.3 V level on the leading edge of the output pulse.
8. The t_{PHL} propagation delay is measured from the 10 mA level on the trailing edge of the input pulse to the 1.3 V level on the trailing edge of the output pulse.
9. The rise time, t_r, is measured from the 10% to the 90% level on the rising edge of the output logic pulse.
10. The fall time, t_f, is measured from the 90% to the 10% level on the falling edge of the output logic pulse.
11. Common mode transient immunity in the logic high level is the maximum (negative) dV_{CM}/dt on the trailing edge of the common mode pulse, V_{CM}, which can be sustained with the output voltage in the logic high state (i.e., $V_O \geq 2\ V$).
12. Common mode transient immunity in the logic low level is the maximum (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, which can be sustained with the output voltage in the logic low state (i.e., $V_O \geq 0.8\ V$).
13. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
14. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5\ \mu A$).

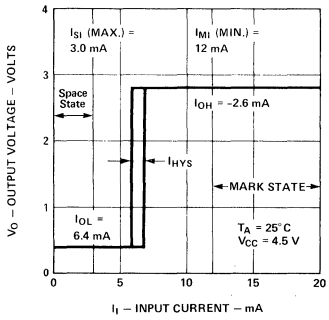


Figure 1. Typical Output Voltage vs. Loop Current

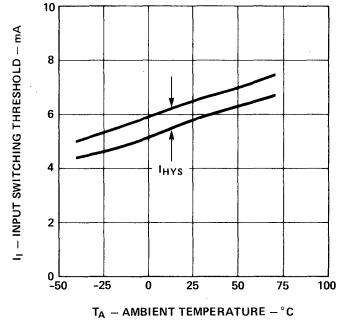


Figure 2. Typical Current Switching Threshold vs. Temperature

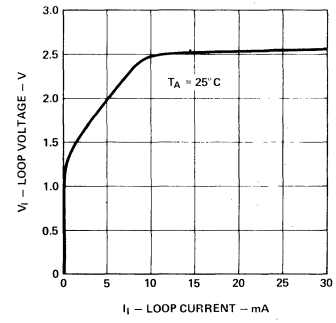


Figure 3. Typical Input Loop Voltage vs. Input Current

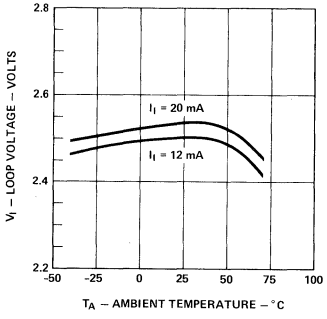


Figure 4. Typical Input Voltage vs. Temperature

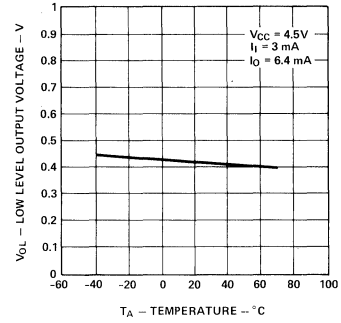


Figure 5. Typical Logic Low Output Voltage vs. Temperature

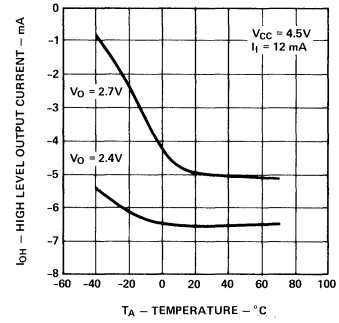
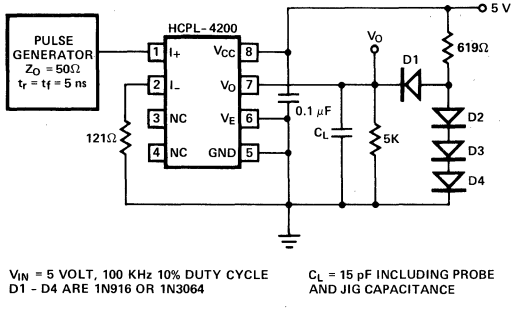


Figure 6. Typical Logic High Output Current vs. Temperature



V_{IN} = 5 VOLT, 100 KHz 10% DUTY CYCLE
D1 - D4 ARE 1N916 OR 1N3064
C_L = 15 pF INCLUDING PROBE AND JIG CAPACITANCE

Figure 7. Test Circuit for t_{PHL}, t_{PLH}, t_r, and t_f

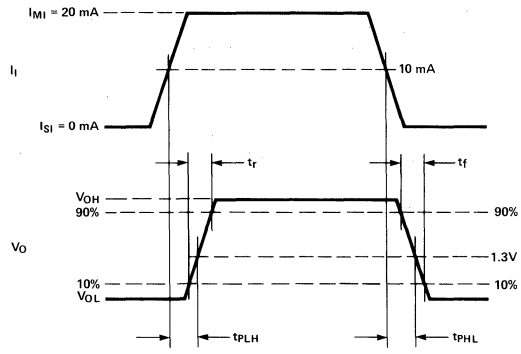


Figure 8. Waveforms for t_{PHL}, t_{PLH}, t_r, and t_f

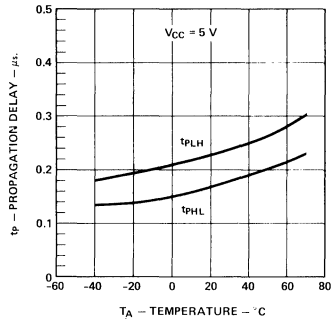


Figure 9. Typical Propagation Delay vs. Temperature

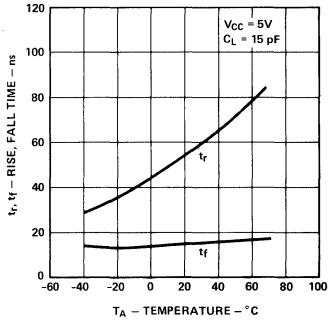


Figure 10. Typical Rise, Fall Time vs. Temperature

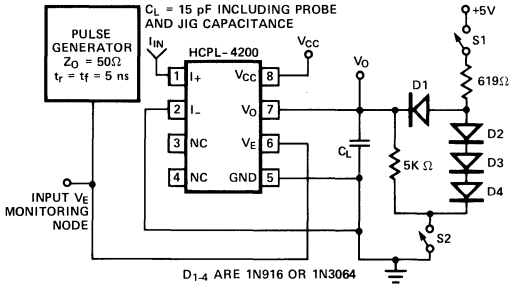


Figure 11. Test Circuit for t_{PZH}, t_{PZL}, t_{PHZ}, and t_{PLZ}

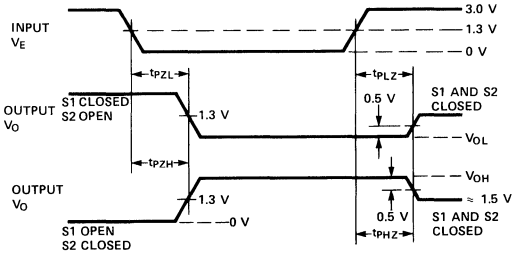


Figure 12. Waveforms for t_{PZH}, t_{PZL}, t_{PHZ}, and t_{PLZ}

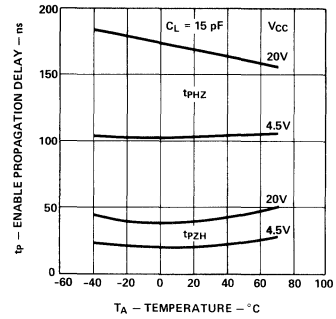


Figure 13. Typical Logic High Enable Propagation Delay vs. Temperature

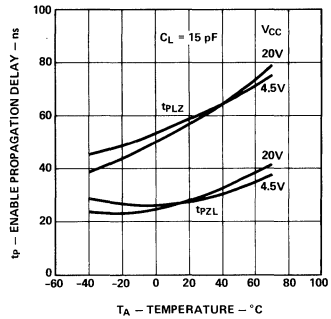


Figure 14. Typical Logic Low Enable Propagation Delay vs. Temperature

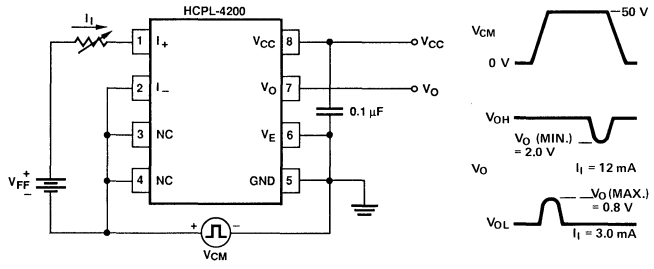


Figure 15. Test Circuit for Common Mode Transient Immunity

Applications

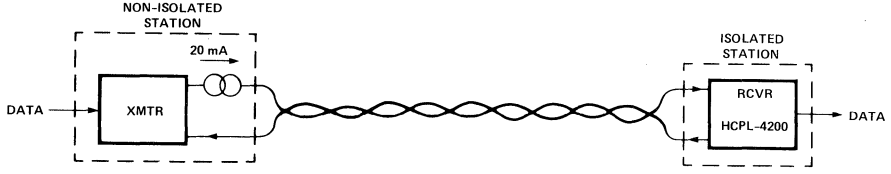
Data transfer between equipment which employs current loop circuits can be accomplished via one of three configurations: simplex, half duplex or full duplex communication. With these configurations, point-to-point and multidrop arrangements are possible. The appropriate configuration to use depends upon data rate, number of stations, number and length of lines, direction of data flow, protocol, current source location and voltage compliance value, etc.

SIMPLEX

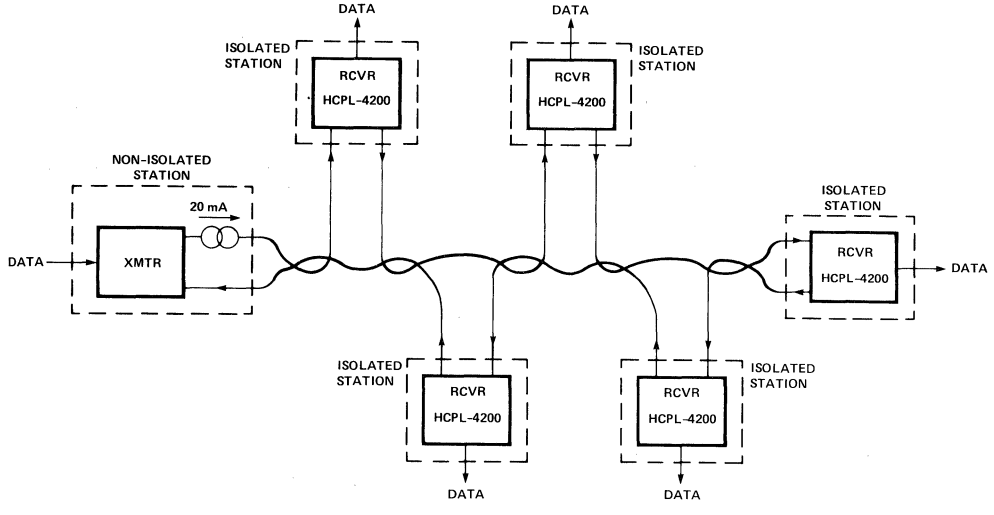
The simplex configuration, whether point to point or multidrop, gives unidirectional data flow from transmitter to receiver(s). This is the simplest configuration for use in long line length (two wire), for high data rate, and low current source compliance level applications. Block diagrams of simplex point-to-point and multidrop arrangements are given in Figures 16a and 16b respectively for the HCPL-4200 receiver optocoupler.

For the highest data rate performance in a current loop, the configuration of a non-isolated active transmitter (containing current source) transmitting data to a remote isolated receiver(s) should be used. When the current source is located at the transmitter end, the loop is charged approximately to V_{MI} (2.5 V). Alternatively, when the current source is located at the receiver end, the loop is charged to the full compliance voltage level. The lower the charged voltage level the faster the data rate will be. In the configurations of Figures 16a and 16b, data rate is independent of the current source voltage compliance level. An adequate compliance level of current source must be available for voltage drops across station(s) during the MARK state in multidrop applications or for long line length. The maximum compliance level is determined by the transmitter breakdown characteristic.

A recommended non-isolated active transmitter circuit which can be used with the HCPL-4200 in point-to-point or in multidrop 20 mA current loop applications is given in Figure 18. The current source is controlled via a standard TTL 7407 buffer to provide high output impedance of current source in both the ON and OFF states. This non-isolated active transmitter provides a nominal 20 mA loop current for the listed values of V_{CC}, R2 and R3 in Figure 17.



(a) POINT-TO-POINT



(b) MULTIDROP

Figure 16. Simplex Current Loop System Configurations for (a) Point-to-Point, (b) Multidrop

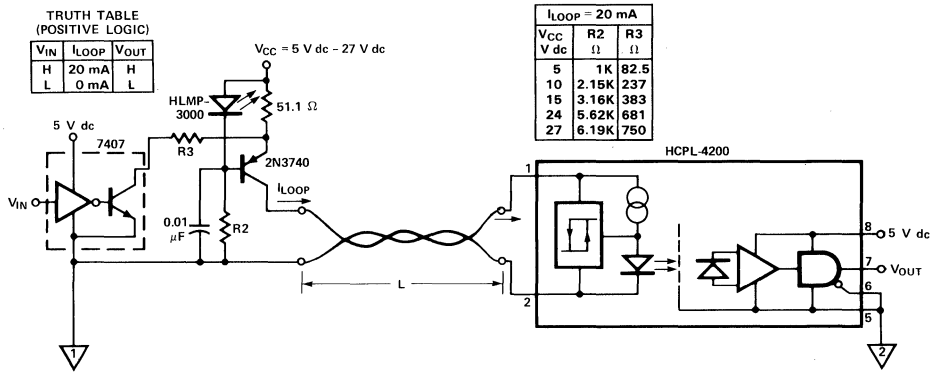


Figure 17. Recommended Non-Isolated Active Transmitter with HCPL-4200 Isolated Receiver for Simplex Point-to-Point 20 mA Current Loop

Length of current loop (one direction) versus minimum required DC supply voltage, V_{CC}, of the circuit in Figure 17 is graphically illustrated in Figure 18. Multidrop configurations will require larger V_{CC} than Figure 18 predicts in order to account for additional station terminal voltage drops.

Typical data rate performance versus distance is illustrated in Figure 19 for the combination of a non-isolated active transmitter and HCPL-4200 optically coupled current loop receiver shown in Figure 17. Curves are shown for 10% and 25% distortion data rate. 10% (25%) distortion data rate is defined as that rate at which 10% (25%) distortion occurs to output bit interval with respect to input bit interval. An input Non-Return-to-Zero (NRZ) test waveform of 16 bits (0000001011111101) was used for data rate distortion measurements. Data rate is independent of current source supply voltage, V_{CC}.

The cable used contained five pairs of unshielded, twisted, 22 AWG wire (Dearborn #862205). Loop current is 20 mA nominal. Input and output logic supply voltages are 5 V dc.

FULL DUPLEX

The full duplex point-to-point communication of Figure 20 uses a four wire system to provide simultaneous, bi-directional data communication between local and remote equipment. The basic application uses two simplex point-to-point loops which have two separate, active, non-isolated units at one common end of the loops. The other end of each loop is isolated.

As Figure 20 illustrates, the combination of Hewlett-Packard current loop optocouplers, HCPL-4100 transmitter and HCPL-4200 receiver, can be used at the isolated end of current loops. Cross talk and common mode coupling are greatly reduced when optical isolation is implemented at the same end of both loops, as shown. The full duplex data rate is limited by the non-isolated active receiver current loop. Comments mentioned under simplex configuration apply to the full duplex case. Consult the HCPL-4100 transmitter optocoupler data sheet for specified device performance.

HALF DUPLEX

The half duplex configuration, whether point-to-point or multidrop, gives non-simultaneous bidirectional data flow from transmitters to receivers shown in Figures 21a and 21b. This configuration allows the use of two wires to carry data back and forth between local and remote units. However, protocol must be used to determine which specific transmitter can operate at any given time. Maximum data rate for a half duplex system is limited by the loop current charging time. These considerations were explained in the Simplex configuration section.

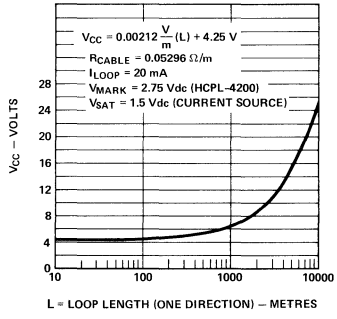


Figure 18. Minimum Required Supply Voltage, V_{CC}, vs. Loop Length for Current Loop Circuit of Figure 18

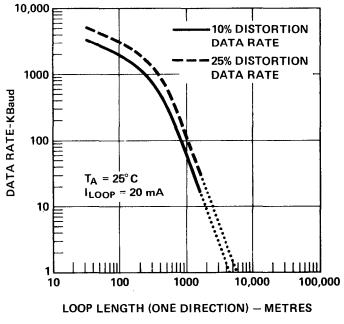


Figure 19. Typical Data Rate vs. Distance

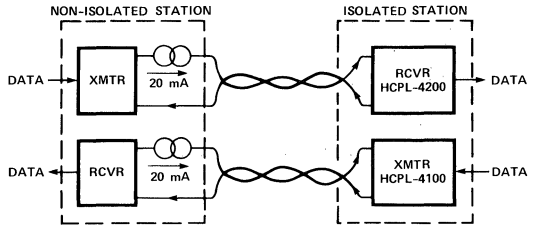
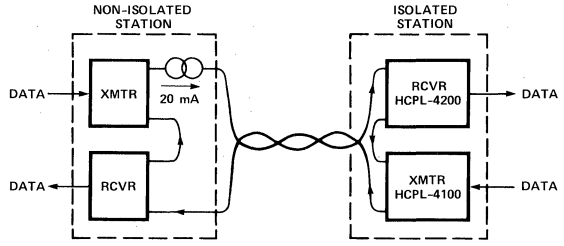


Figure 20. Full Duplex Point-to-Point Current Loop System Configuration

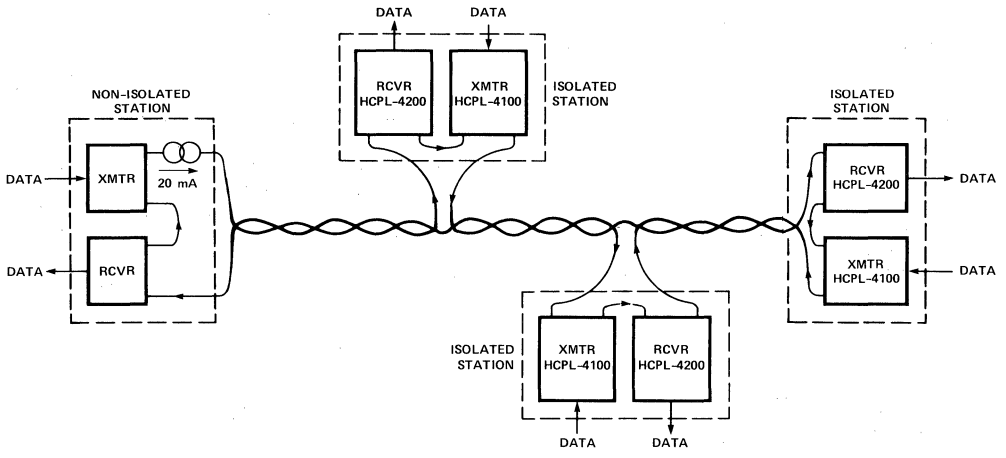
Figures 21a and 21b illustrate half duplex application for the combination of HCPL-4100/-4200 optocouplers. The unique and complementary designs of the HCPL-4100 transmitter and HCPL-4200 receiver optocouplers provide many designed-in benefits. For example, total optical isolation at one end of the current loop is easily accomplished, which results in substantial removal of common mode influences, elimination of ground potential differences and reduction of power supply requirements. With this combination of HCPL-4100/-4200 optocouplers, specific current loop noise immunity is provided, i.e., minimum SPACE state current noise immunity is 1 mA, MARK state noise immunity is 8 mA.

Voltage compliance of the current source must be of an adequate level for operating all units in the loop while not exceeding 27 V dc, the maximum breakdown voltage for the HCPL-4100. Note that the HCPL-4100 transmitter will allow loop current to conduct when input V_{CC} power is off. Consult the HCPL-4100 transmitter optocoupler data sheet for specified device performance.

For more information about the HCPL-4100/-4200 optocouplers, consult Application Note 1018.



(a) POINT-TO-POINT



(b) MULTIDROP

Figure 21. Half Duplex Current Loop System Configurations for (a) Point-to-Point, (b) Multidrop

HEWLETT PACKARD

New

High CMR Isolation Amplifier

Technical Data

HCPL-7800
HCPL-7800A
HCPL-7800B

Features

- **15 kV/μs Common-Mode Rejection at V_{CM} = 1000 V***
- **Compact, Auto-Insertable Standard 8-pin DIP Package**
- **4.6 μV/°C Offset Drift vs. Temperature**
- **0.9 mV Input Offset Voltage**
- **85 kHz Bandwidth**
- **0.1% Nonlinearity**
- **Worldwide Safety Approval: UL 1577, VDE 0884 and CSA**
- **Advanced Sigma-Delta (ΣΔ) A/D Converter Technology**
- **Fully Differential Circuit Topology**
- **1 μm CMOS IC Technology**

Applications

- **Motor Phase Current Sensing**
- **General Purpose Industrial Current Sensing**
- **High-Voltage Power Source Voltage Monitoring**
- **Switch-Mode Power Supply Signal Isolation**
- **General Purpose Analog Signal Isolation**
- **Transducer Isolation**

*The terms common-mode rejection (CMR) and isolation-mode rejection (IMR) are used interchangeably throughout this data sheet.

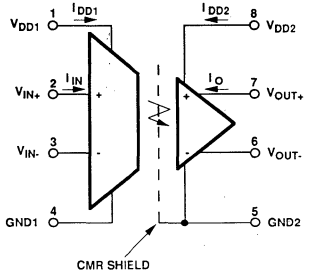
Description

The HCPL-7800 high CMR isolation amplifier provides a unique combination of features ideally suited for motor control circuit designers. The product provides the precision and stability needed to accurately monitor motor current in high-noise motor control environments, providing for smoother control (less "torque ripple") in various types of motor control applications.

This product paves the way for a smaller, lighter, easier to produce, high noise rejection, low cost solution to motor current sensing. The product can also be used for general analog signal isolation applications requiring high accuracy, stability and linearity under similarly severe noise conditions. For general applications, we recommend the HCPL-7800 which exhibits a part-to-part gain tolerance of ±5%. For precision applications, HP offers the HCPL-7800A and HCPL-7800B, each with part-to-part gain tolerances of ±1%.

The HCPL-7800 utilizes sigma-delta (ΣΔ) analog-to-digital converter technology, chopper stabilized amplifiers, and a fully differential circuit topology fabricated using HP's 1 μm standard-cell CMOS IC process. The part also couples our high-efficiency, high-speed AlGaAs LED to a high-speed, noise-

Functional Diagram



OPTO COUPLERS

CAUTION: The small device geometries inherent to the design of this CMOS component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

shielded detector using our patented "light-pipe" optocoupler packaging technology.

Together, these features deliver unequaled isolation-mode noise rejection, as well as excellent offset and gain accuracy and stability over time and temperature. All in a compact, auto-insertable, industry standard 8-pin DIP package that meets worldwide regulatory safety standards (gull-wing surface mount option #300 also available).

Regulatory Information

The HCPL-7800 has been approved by the following organizations:

UL

Approved under UL1577, component recognition FILE E55361

VDE

Approved according to VDE 0884/08.87

Can be used for safe electrical separation between AC mains and SELV (safety extra-low voltage) in equipment according to the following specifications:
DIN VDE 0804/05.89
DIN VDE 0160/05.88

Reference voltage (VDE 0110b Tab 4): 650 Vac

CSA

Approved under CSA 22.2 No. 0-General Requirements, Canadian Electrical Code, Part II; and CSA Component Acceptance Notice #5, File CA 88324.

VDE 0884 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0109/12.83, Table 1 for rated mains voltage ≤300 V_{RMS} for rated mains voltage ≤600 V_{RMS}		 I-IV I-III	
Climatic Classification		40/85/21	
Pollution Degree (DIN VDE 0109/12.83)*		2	
Maximum Working Insulation Voltage	V_{IORM}	600	V_{RMS}
Input to Output Test Voltage, Method b** V_{PR} = 1.6 x V_{IORM}, Production test with t_p = 1 sec, Partial discharge < 5 pC	V_{PR}	960	V_{RMS}
Input to Output Test Voltage, Method a** V_{PR} = 1.2 x V_{IORM}, Type and sample test, t_p = 60 sec, Partial discharge < 5 pC	V_{PR}	720	V_{RMS}
Highest Allowable Overvoltage** (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	6000	V_{PEAK}
Safety-limiting values (Maximum values allowed in the event of a failure, also see Figure 27) Case Temperature Input Power Output Power	 T_{SI} $P_{SI, Input}$ $P_{SI, Output}$	 175 80 250	 °C mW mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V	R_{IS}	≥10E11	Ohm

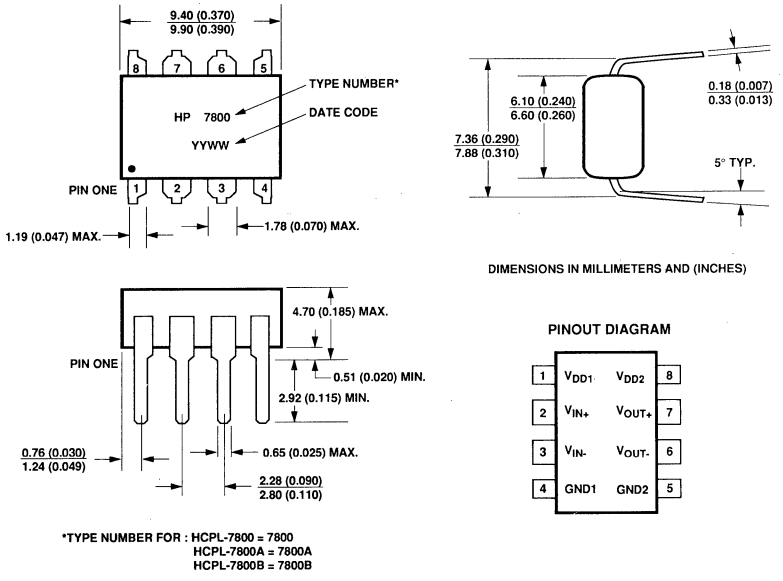
*This part may also be used in Pollution Degree 3 environments where the rated mains voltage is ≤ 300 V_{RMS} (per DIN VDE 0109/12.83).
**Refer to the front of the optocoupler section of the current Optoelectronics Designer's Catalog for a more detailed description of VDE 0884 and other product safety regulations.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External air gap (clearance)	L (IO1)	>7	mm	Measured from input terminals to output terminals
Min. External tracking path (creepage)	L (IO2)	8.0	mm	Measured from input terminals to output terminals
Min. Internal plastic gap (clearance)		0.5	mm	Through insulation distance conductor to conductor
Tracking resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		III a		Material Group DIN VDE 0109

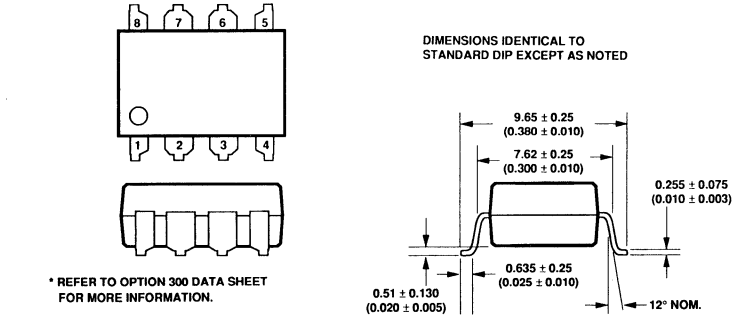
Package Outline Drawings

Standard DIP Package



*TYPE NUMBER FOR : HCPL-7800 = 7800
HCPL-7800A = 7800A
HCPL-7800B = 7800B

Gull Wing Surface Mount Option 300*



* REFER TO OPTION 300 DATA SHEET FOR MORE INFORMATION.

Ordering Information:

HCPL-7800 x

No Specifier = ±5% Gain Tol.; Mean Gain Value = 8.00
A = ±1% Gain Tol.; Mean Gain Value = 7.93
B = ±1% Gain Tol.; Mean Gain Value = 8.07

Option yyy

300 = Gull Wing Surface Mount Lead Option
500 = Tape/Reel Package Option (1k min.)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-55	125	°C	
Ambient Operating Temperature	T_A	-40	100	°C	
Supply Voltages	V_{DD1}, V_{DD2}	0	5.5	V	
Steady-State Input Voltage	V_{IN+}, V_{IN-}	-2.0	V_{DD1}+0.5	V	
2 Second Transient Input Voltage		-6.0			
Output Voltages	V_{OUT+}, V_{OUT-}	-0.5	V_{DD2}+0.5	V	
Lead Solder Temperature (1.6 mm below seating plane, 10 sec.)	T_{LS}		260	°C	1

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Ambient Operating Temperature	T_A	-40	85	°C	2
Supply Voltages	V_{DD1}, V_{DD2}	4.5	5.5	V	3
Input Voltage	V_{IN+}, V_{IN-}	-200	200	mV	4
Output Current	$\|Io\|$		1	mA	5

DC Electrical Specifications

All specifications and figures are at the nominal operating condition of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 5.0 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input Offset Voltage	V_{OS}	-1.8	-0.9	0.0	mV		1	
Input Offset Drift vs. Temperature	dV_{OS}/dT		-2.1		µV/°C		1, 2	6
Abs. Value of Input Offset Drift vs. Temperature	$\lvert dV_{OS}/dT \rvert$		4.6		µV/°C		1	7
Input Offset Drift vs. V_{DD1}	dV_{OS}/dV_{DD1}		30		µV/V		1, 3	8
Input Offset Drift vs. V_{DD2}	dV_{OS}/dV_{DD2}		-40		µV/V		1, 4	9
Gain (±5% Tol.)	G	7.61	8.00	8.40		-200 < V_{IN+} < 200 mV	1, 5	10
Gain - A Version (±1% Tol.)	G_A	7.85	7.93	8.01				
Gain - B Version (±1% Tol.)	G_B	7.99	8.07	8.15				
Gain Drift vs. Temperature	dG/dT		0.001		%/°C		5, 6	11
Abs. Value of Gain Drift vs. Temperature	$\lvert dG/dT \rvert$		0.001		%/°C		5	12
Gain Drift vs. V_{DD1}	dG/dV_{DD1}		0.21		%/V		5, 7	13
Gain Drift vs. V_{DD2}	dG/dV_{DD2}		-0.06		%/V		5, 8	14
200 mV Nonlinearity	NL_{200}		0.2	0.35	%		5, 9	15
200 mV Nonlinearity Drift vs. Temperature	dNL_{200}/dT		-0.001		% pts/°C		5, 10	16
200 mV Nonlinearity Drift vs. V_{DD1}	dNL_{200}/dV_{DD1}		-0.005		% pts/V		5, 11	17
200 mV Nonlinearity Drift vs. V_{DD2}	dNL_{200}/dV_{DD2}		-0.007		% pts/V		5, 12	18
100 mV Nonlinearity	NL_{100}		0.1	0.25	%	-100 < V_{IN+} < 100 mV	5, 13	19
Maximum Input Voltage Before Output Clipping	$\lvert V_{IN+} \rvert_{max}$		300		mV		14	
Average Input Bias Current	I_{IN}		-670		nA		15, 16	20
Input Bias Current Temperature Coefficient	dI_{IN}/dT		3		nA/°C			
Average Input Resistance	R_{IN}		530		kΩ		15	20
Input Resistance Temperature Coefficient	dR_{IN}/dT		0.38		%/°C			
Input DC Common-Mode Rejection Ratio	$CMRR_{IN}$		72		dB			21
Output Resistance	R_O		11		Ω			5
Output Resistance Temperature Coefficient	dR_O/dT		0.6		%/°C			
Output Low Voltage	V_{OL}		1.18		V	$\lvert V_{IN+} \rvert$ = 500 mV	14	22
Output High Voltage	V_{OH}		3.61		V			
Output Common-Mode Voltage	V_{OCM}	2.20	2.39	2.60	V	-40°C < T_A < 85°C 4.5 V < V_{DD1} < 5.5 V	14	
Input Supply Current	I_{DD1}		10.7	13.5	mA		17	23
Output Supply Current	I_{DD2}		11.6	14.5	mA	V_{IN+} = 200 mV, -40°C < T_A < 85°C 4.5 V < V_{DD2} < 5.5 V	18	24
Output Short-Circuit Current	$\lvert I_{OSC} \rvert$		9.3		mA	V_{OUT} = 0 V or V_{DD2}		25

AC Electrical Specifications

All specifications and figures are at the nominal operating condition of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 5.0 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Rising Edge Isolation Mode Rejection	IMR_R	10	25		kV/µs	V_{IM} = 1 kV	19, 20	26
Falling Edge Isolation Mode Rejection	IMR_F	10	15		kV/µs			
Isolation Mode Rejection Ratio at 60 Hz	IMRR		>140		dB		19	27
Propagation Delay to 10%	t_{PD10}		2.0	3.3	µs	-40°C < T_A < 85°C	21, 22	
Propagation Delay to 50%	t_{PD50}		3.4	5.6	µs			
Propagation Delay to 90%	t_{PD90}		6.3	9.9	µs			
Rise/Fall Time (10%-90%)	$t_{R/F}$		4.3	6.6	µs			
Bandwidth (-3 dB)	f_{-3dB}	50	85		kHz		23, 24	
Bandwidth (-45°)	$f_{-45°}$		35		kHz			
RMS Input-Referred Noise	V_N		300		μV_{rms}	Bandwidth = 100 kHz	25, 26	28
Power Supply Rejection	PSR		5		mV_{pk-pk}			29

Package Characteristics

All specifications and figures are at the nominal operating condition of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 5.0 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions		Fig.	Note
Input-Output Insulation Voltage	V_{ISO}	3750			V_{rms}	t = 1 min., RH ≤ 50%			30, 31
Input-Output Resistance	R_{I-O}	10^{12}	10^{13}		Ω	T_A = 25°C	V_{I-O} = 500 V_{dc}		30
		10^{11}				T_A = 100°C			
Input-Output Capacitance	C_{I-O}		0.7		pF	f = 1 MHz			30
Input IC Junction-to-Case Thermal Resistance	θ_{jci}		96		°C/W				32
Output IC Junction-to-Case Thermal Resistance	θ_{jco}		114		°C/W				
Case-to-Ambient Thermal Resistance	θ_{ca}		86		°C/W				

Notes:

General Note: Typical values represent the mean value of all characterization units at the nominal operating conditions. Typical drift specifications are determined by calculating the rate of change of the specified parameter versus the drift parameter (at nominal operating conditions) for each characterization unit, and then averaging the individual unit rates. The corresponding drift figures are normalized to the nominal operating conditions and show how much drift occurs as the particular drift parameter is varied from its nominal value, with all other parameters held at their nominal operating values. Figures show the mean drift of all characterization units as a group, as well as the ±2-sigma statistical limits. Note that the typical drift specifications in the tables below may differ from the slopes of the mean curves shown in the corresponding figures.

1. HP recommends the use of non-chlorine activated fluxes.
2. The HCPL-7800 will operate properly at ambient temperatures up to 100°C but may not meet published specifications under these conditions.
3. DC performance can be best maintained by keeping V_{DD1} and V_{DD2} as close as possible to 5 V. See application section for circuit recommendations.
4. HP recommends operation with V_{IN-} = 0 V (tied to GND1). Limiting V_{IN+} to 100 mV will improve DC nonlinearity and nonlinearity drift. If V_{IN-} is brought above 800 mV with respect to GND1, an internal test mode may be activated. This test mode is not intended for customer use.
5. Although, statistically, the average difference in the output resistance of pins 6 and 7 is near zero, the standard deviation of the difference is 1.3 Ω due to normal process variations. Consequently, keeping the output current below 1 mA will ensure the best offset performance.
6. Data sheet value is the average change in offset voltage versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the change in offset voltage per °C change in temperature.
7. Data sheet value is the average magnitude of the change in offset voltage versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the change in magnitude per °C change in temperature.
8. Data sheet value is the average change in offset voltage versus input supply voltage at V_{DD1} = 5 V, with all other parameters held constant. This value is expressed as the change in offset voltage per volt change of the input supply voltage.
9. Data sheet value is the average change in offset voltage versus output supply voltage at V_{DD2} = 5 V, with all other parameters held constant. This value is expressed as the change in offset voltage per volt change of the output supply voltage.
10. Gain is defined as the slope of the best-fit line of differential output voltage (V_{OUT+} - V_{OUT-}) versus differential input voltage (V_{IN+} -V_{IN-}) over the specified input range.
11. Data sheet value is the average change in gain versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the percentage change in gain per °C change in temperature.
12. Data sheet value is the average magnitude of the change in gain versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the percentage change in magnitude per °C change in temperature.
13. Data sheet value is the average change in gain versus input supply voltage at V_{DD1} = 5 V, with all other parameters held constant. This value is expressed as the percentage change in gain per volt change of the input supply voltage.
14. Data sheet value is the average change in gain versus output supply voltage at V_{DD2} = 5 V, with all other parameters held constant. This value is expressed as the percentage change in gain per volt change of the output supply voltage.
15. Nonlinearity is defined as the maximum deviation of the output voltage from the best-fit gain line (see Note 10), expressed as a percentage of the full-scale differential output voltage range. For example, an input range of ±200 mV generates a full-scale differential output range of 3.2 V (±1.6 V); a maximum output deviation of 6.4 mV would therefore correspond to a nonlinearity of 0.2%.
16. Data sheet value is the average change in nonlinearity versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the number of percentage points that the nonlinearity will change per °C change in temperature. For example, if the temperature is increased from 25°C to 35°C, the nonlinearity typically will decrease by 0.01 percentage points (10°C times -0.001 % pts/°C) from 0.2% to 0.19%.
17. Data sheet value is the average change in nonlinearity versus input supply voltage at V_{DD1} = 5 V, with all other parameters held constant. This value is expressed as the number of percentage points that the nonlinearity will change per volt change of the input supply voltage.
18. Data sheet value is the average change in nonlinearity versus output supply voltage at V_{DD2} = 5 V, with all other parameters held constant. This value is expressed as the number of percentage points that the nonlinearity will change per volt change of the output supply voltage.
19. NL_{100} is the nonlinearity specified over an input voltage range of ±100 mV.
20. Because of the switched-capacitor nature of the input sigma-delta converter, time-averaged values are shown.
21. This parameter is defined as the ratio of the differential signal gain (signal applied differentially between pins 2 and 3) to the common-mode gain (input pins tied together and the signal applied to both inputs at the same time), expressed in dB.
22. When the differential input signal exceeds approximately 300 mV, the outputs will limit at the typical values shown.
23. The maximum specified input supply current occurs when the differential input voltage (V_{IN+} - V_{IN-}) = 0 V. The input supply current decreases approximately 1.3 mA per 1 V decrease in V_{DD1}.
24. The maximum specified output supply current occurs when the differential input voltage (V_{IN+} - V_{IN-}) = 200 mV, the maximum recommended operating input voltage. However, the output supply current will continue to rise for differential input voltages up to approximately 300 mV, beyond

which the output supply current remains constant.

25. Short circuit current is the amount of output current generated when either output is shorted to V_{DD2} or ground.
26. IMR (also known as CMR or Common Mode Rejection) specifies the minimum rate of rise of an isolation mode noise signal at which small output perturbations begin to appear. These output perturbations can occur with both the rising and falling edges of the isolation-mode wave form and may be of either polarity. When the perturbations first appear, they occur only occasionally and with relatively small peak amplitudes (typically 20-30 mV at the output of the recommended application circuit). As the magnitude of the isolation mode transients increase, the regularity and amplitude of the perturbations also increase. See applications section for more information.
27. IMRR is defined as the ratio of differential signal gain (signal applied differentially between pins 2 and 3) to the isolation mode gain (input pins tied to pin 4 and the signal applied between the input and the output of the isolation amplifier) at 60 Hz, expressed in dB.
28. Output noise comes from two primary sources: chopper noise and sigma-delta quantization noise. Chopper noise results from chopper stabilization of the output op-amps. It occurs at a specific frequency (typically 200 kHz at room temperature), and is not attenuated by the internal output filter. A filter circuit can be easily added to the external post-amplifier to reduce the total rms output noise. The internal output filter does eliminate most, but not all, of the sigma-delta quantization noise. The magnitude of the output quantization noise is very small at lower frequencies (below 10 kHz) and increases with increasing frequency. See applications section for more information.
29. Data sheet value is the differential amplitude of the transient at the output of the HCPL-7800 when a 1 V_{pk-pk}, 1 MHz square wave with 5 ns rise and fall times is applied to both V_{DD1} and V_{DD2}.
30. This is a two-terminal measurement: pins 1-4 are shorted together and pins 5-8 are shorted together.
31. In accordance with UL1577, for devices with minimum V_{ISO} specified at 3750 V_{rms}, each optocoupler is proof-tested by applying an insulation test voltage greater-than-or-equal-to 4500 V_{rms} for one second (leak current detection limit, I_{I-O} < 5 μA). This test is performed before the method b, 100% production test for partial discharge shown in the VDE 0884 Insulation Characteristics Table.
32. Thermal resistance values were measured on a 3"x3" printed circuit board in still air at room temperature with the device in a socket. Case temperature was measured with a thermocouple located in the center of the underside of the package.

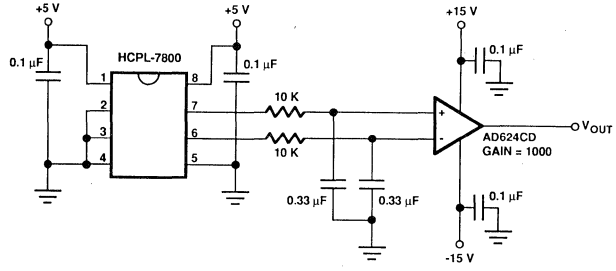


Figure 1. Input Offset Voltage Test Circuit.

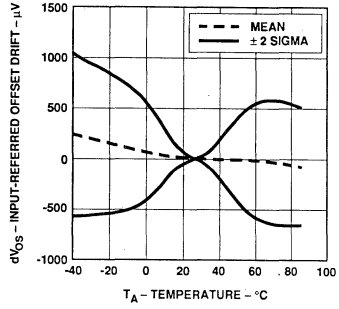


Figure 2. Input-Referred Offset Drift vs. Temperature.

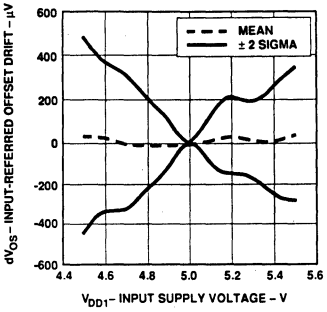


Figure 3. Input-Referred Offset Drift vs. V_{DD1} (V_{DD2} = 5 V).

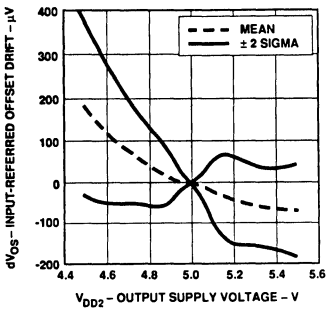


Figure 4. Input-Referred Offset Drift vs. V_{DD2} (V_{DD1} = 5 V).

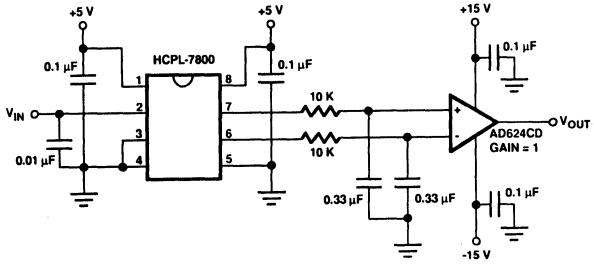


Figure 5. Gain and Nonlinearity Test Circuit.

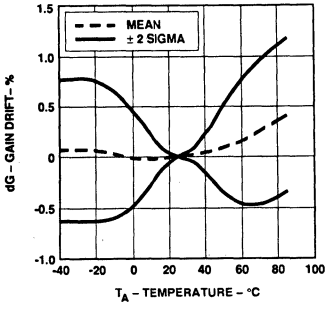


Figure 6. Gain Drift vs. Temperature.

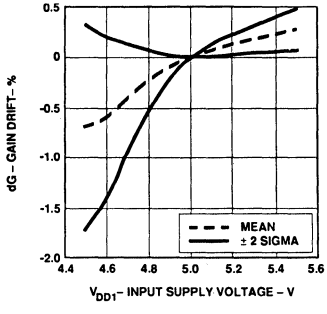


Figure 7. Gain Drift vs. V_{DD1} (V_{DD2} = 5 V).

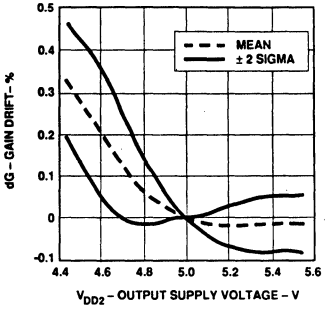


Figure 8. Gain Drift vs. V_{DD2} (V_{DD1} = 5 V).

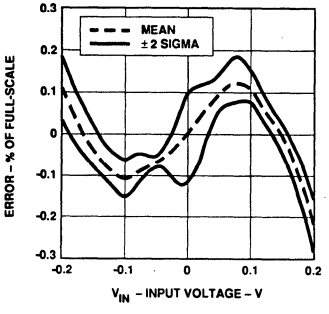


Figure 9. 200 mV Nonlinearity Error Plot.

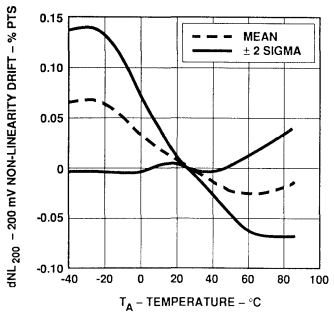


Figure 10. 200 mV Nonlinearity Drift vs. Temperature.

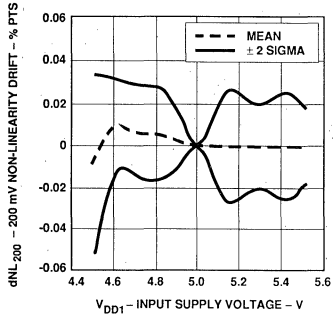


Figure 11. 200 mV Nonlinearity Drift vs. V_{DD1} (V_{DD2} = 5 V).

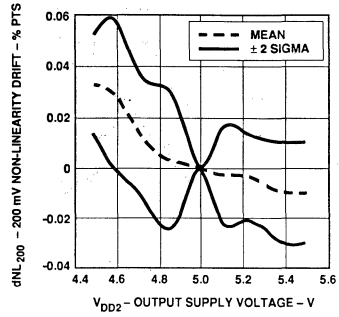


Figure 12. 200 mV Nonlinearity Drift vs. V_{DD2} (V_{DD1} = 5 V).

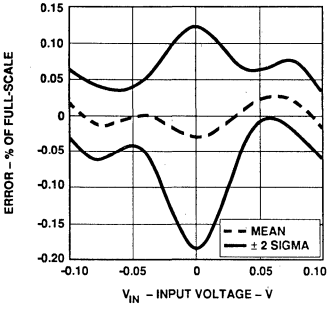


Figure 13. 100 mV Nonlinearity Error Plot.

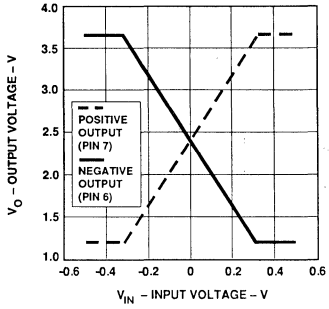


Figure 14. Typical Output Voltages vs. Input Voltage.

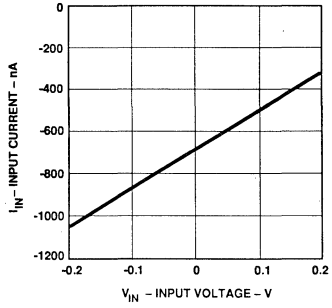


Figure 15. Typical Input Current vs. Input Voltage.

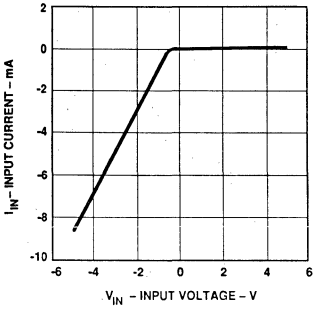


Figure 16. Typical Input Current vs. Input Voltage.

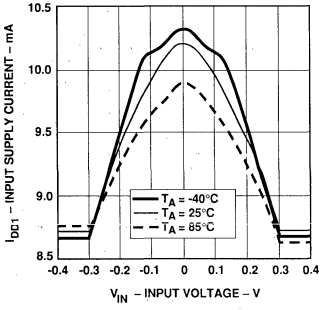


Figure 17. Typical Input Supply Current vs. Input Voltage.

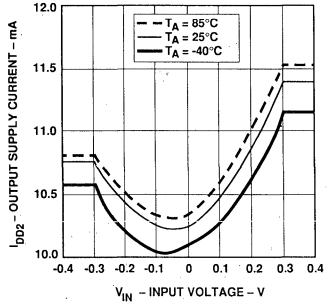


Figure 18. Typical Output Supply Current vs. Input Voltage.

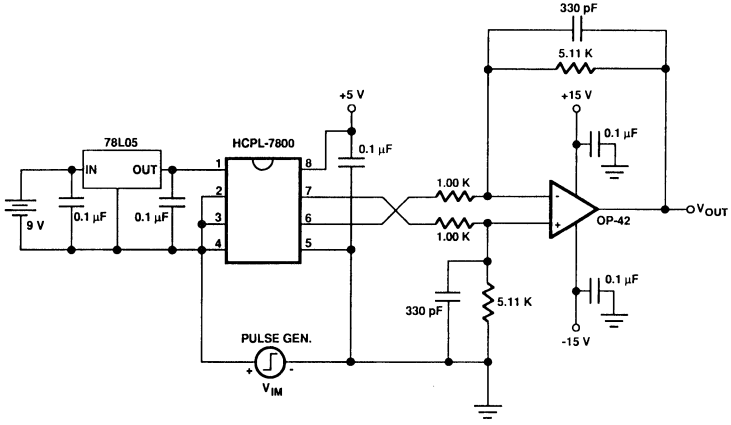


Figure 19. Isolation Mode Rejection Test Circuit.

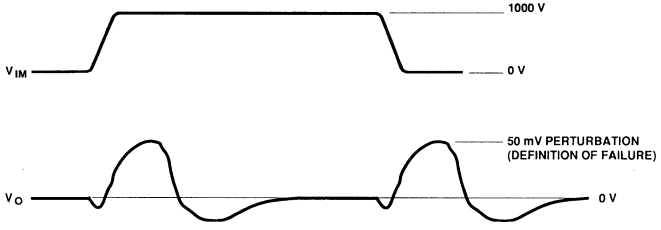


Figure 20. Typical IMR Failure Waveform.

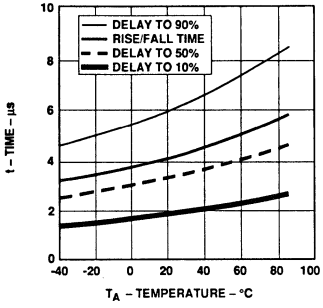


Figure 21. Typical Propagation Delays and Rise/Fall Time vs. Temperature.

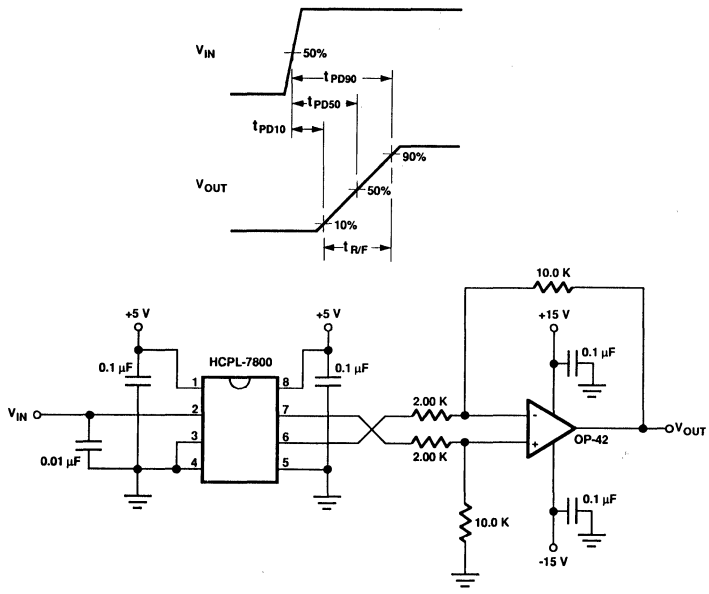


Figure 22. Propagation Delay and Rise/Fall Time Test Circuit.

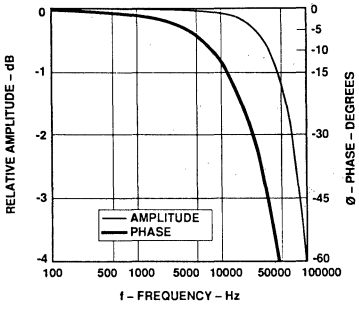


Figure 23. Typical Amplitude and Phase Response vs. Frequency.

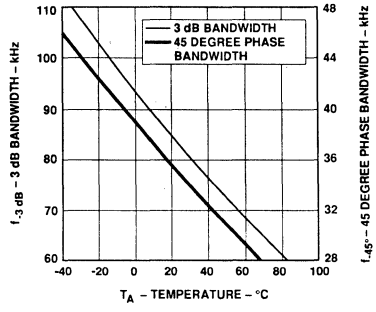


Figure 24. Typical 3 dB and 45° Bandwidths vs. Temperature.

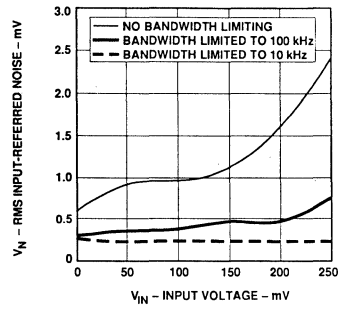


Figure 25. Typical RMS Input-Referred Noise vs. Input Voltage.

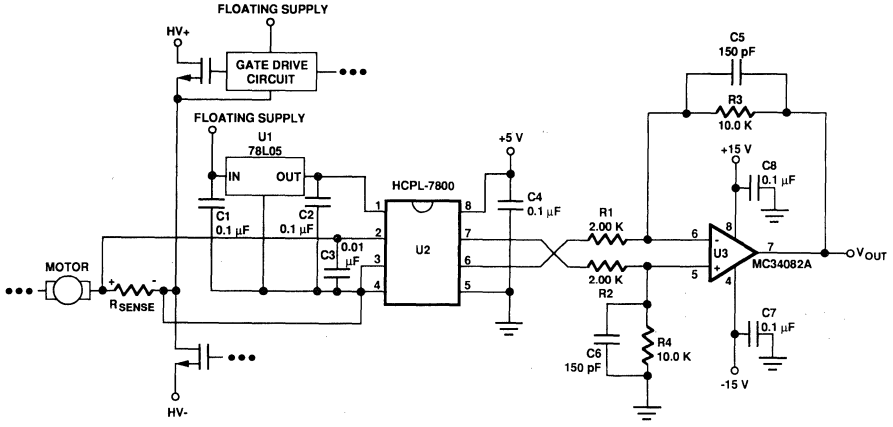


Figure 26. Recommended Application Circuit.

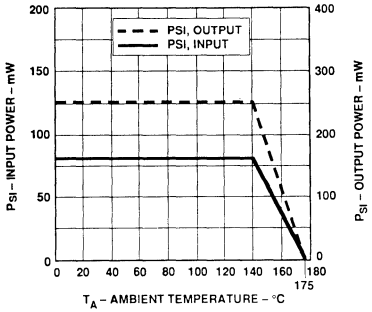


Figure 27. Dependence of Safety-Limiting Parameters on Ambient Temperature.

Applications Information

Functional Description

Figure 28 shows the primary functional blocks of the HCPL-7800. In operation, the sigma-delta analog-to-digital converter converts the analog input signal into a high-speed serial bit stream, the time average of which is directly proportional to the input signal. This high speed stream of digital data is encoded and optically transmitted to the detector circuit. The detected signal is decoded and converted into accurate analog voltage levels, which are then filtered to produce the final output signal.

To help maintain device accuracy over time and temperature, internal amplifiers are chopper-stabilized. Additionally, the encoder circuit eliminates the effects of pulse-width distortion of the optically transmitted data by generating one pulse for every edge (both rising and falling) of the converter data to be transmitted, essentially converting the *widths* of the sigma-delta output pulses into the *positions* of the encoder output pulses. A significant benefit of this coding scheme is that any non-ideal characteristics of the LED (such as non-linearity and drift over time and temperature) have little, if any, effect on the performance of the HCPL-7800.

Circuit Information

The recommended application circuit is shown in Figure 26. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple three-terminal voltage regulator. The input of the HCPL-7800 is connected directly to the current sensing resistor. The differential output of the isolation amplifier is converted to a ground-referenced single-ended output voltage with a simple differential amplifier circuit. Although the application circuit is relatively simple, a few general recommendations should be followed to ensure optimal performance.

As shown in Figure 26, 0.1 µF bypass capacitors should be located as close as possible to the input and output power supply pins of the HCPL-7800. Notice that pin 2 (V_{IN+}) is bypassed with a 0.01 µF capacitor to reduce input offset voltage that can be caused by the combination of long input leads and the switched-capacitor nature of the input circuit.

With pin 3 (V_{IN-}) tied directly to pin 4 (GND1), the power-supply return line also functions as the sense line for the negative side of the current-sensing resistor; this allows a single twisted pair of wire to connect the isolation amplifier to the sense resistor. In some applications, however, better performance may be obtained by connecting pins 2 and 3 (V_{IN+} and V_{IN-}) directly across the sense resistor with twisted pair wire and using a separate wire for the power supply return line. Both input pins should be bypassed with 0.01 µF capacitors close to the isolation amplifier. In either case, it is recommended that twisted-pair wire be used to connect the isolation amplifier to the current-sensing resistor to minimize electro-magnetic interference of the sense signal.

To obtain optimal CMR performance, the layout of the printed circuit board (PCB) should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground plane on the PCB does not pass directly below the HCPL-7800. An example single-sided PCB layout for the recommended application circuit is shown in Figure 29. The trace pattern is shown in "X-ray" view as it would be seen from the top of the PCB; a mirror image of this layout can be used to generate a PCB.

An inexpensive 78L05 three-terminal regulator is shown in the recommended application circuit. Because the performance of the isolation amplifier can be affected by changes in the power supply voltages, using regulators with tighter output voltage tolerances will result in better overall circuit performance. Many different regulators that provide tighter output voltage tolerances than the 78L05 can be used, including: TL780-05 (Texas Instruments), LM340LAZ-5.0 and LP2950CZ-5.0 (National Semiconductor).

The op-amp used in the external post-amplifier circuit should be of sufficiently high precision so that it does not contribute a significant amount of offset or offset drift relative to the contribution from the isolation amplifier. Generally, op-amps with bipolar input stages exhibit better offset performance than op-amps with JFET or MOSFET input stages.

In addition, the op-amp should also have enough bandwidth and slew rate so that it does not adversely affect the response speed of the overall circuit. The post-amplifier circuit includes a pair of capacitors (C5 and C6) that form a single-pole low-pass filter; these capacitors allow the bandwidth of the post-amp to be adjusted independently of the gain and are useful for reducing the output noise from the isolation amplifier. Many different op-amps could be used in the circuit, including: MC34082A (Motorola), TL032A, TLO52A, and TLC277 (Texas Instruments), LF412A (National Semiconductor).

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate CMRR and adequate gain tolerance for the overall circuit. Resistor networks can be used that have much better ratio tolerances than can be achieved using discrete resistors. A resistor network also reduces the total number of components for the circuit as well as the required board space.

The current-sensing resistor should have a relatively low value of resistance to minimize power dissipation, a fairly low inductance to accurately reflect high-frequency signal compo-

nents, and a reasonably tight tolerance to maintain overall circuit accuracy. Although decreasing the value of the sense resistor decreases power dissipation, it also decreases the full-scale input voltage making iso-amp offset voltage effects more significant. These two conflicting considerations, therefore, must be weighed against each other in selecting an appropriate sense resistor for a particular application. To maintain circuit accuracy, it is recommended that the sense resistor and the isolation amplifier circuit be located as close as possible to one another. Although it is possible to buy current-sensing resistors from established vendors (e.g., the LVR-1, -3 and -5 resistors from Dale), it is also possible to make a sense resistor using a short piece of wire or even a trace on a PC board.

Figures 30 and 31 illustrate the response of the overall isolation amplifier circuit shown in Figure 26. Figure 30 shows the response of the circuit to a ±200 mV 20 kHz sine wave input and Figure 31 the response of the circuit to a ±200 mV 20 kHz square wave input. Both figures demonstrate the fast, well-behaved response of the HCPL-7800.

Figure 32 shows how quickly the isolation amplifier recovers from an overdrive condition generated by a 2 kHz square wave swinging between 0 and 500 mV (note that the time scale is different from the previous figures). The first wave form is the output of the application circuit with the filter capacitors removed to show the actual response of the isolation amplifier. The second wave form is the response of the same circuit with the capacitors installed. The recovery time and overshoot are relatively independent of the amplitude and polarity of the overdrive signal, as well as its duration.

For more information, refer to Application Note 1059.

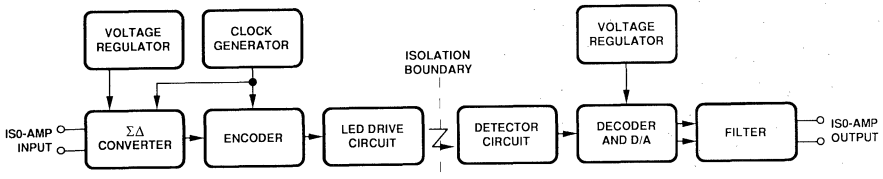


Figure 28. HCPL-7800 Block Diagram.

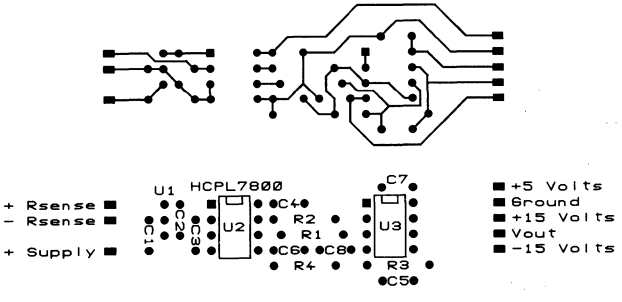


Figure 29. PC Board Trace Pattern and Loading Diagram Example.

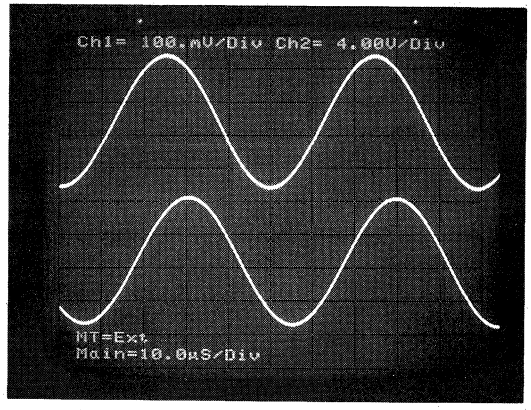


Figure 30. Application Circuit Sine Wave Response.

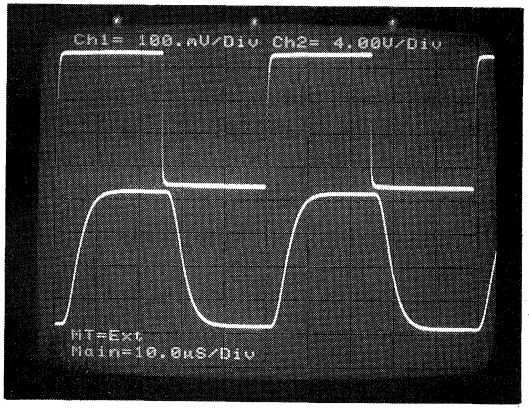


Figure 31. Application Circuit Square Wave Response.

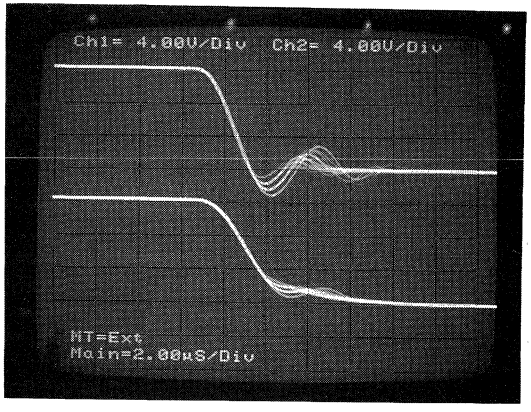


Figure 32. Application Circuit Overload Recovery Waveform.

HEWLETT PACKARD

New

Power Bipolar Transistor Base Drive Optocoupler

Technical Data

HCPL-3000

Features

- **High Output Current**
  I_{O2} (2.0 A Peak, 0.6 A Continuous)
  I_{O1} (1.0 A Peak, 0.5 A Continuous)
- **Guaranteed High Common Mode Rejection (CMR): 1.5 kV/μs at V_{CM} = 600 V**
- **Wide V_{CC} Range (5.4 to 18 Volts)**
- **2 μs Propagation Delay**
- **Recognized Under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 5000 VAC, 1 Minute**

Applications

- **Isolated Bipolar Transistor Base Drive**
- **AC and DC Motor Drives**
- **General Purpose Industrial Inverters**
- **Uninterruptable Power Supply**

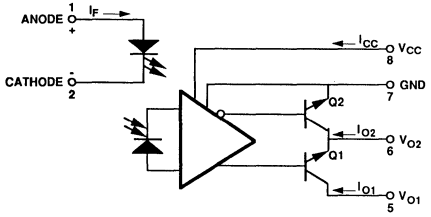
Description

The HCPL-3000 consists of a Silicon-doped GaAs LED optically coupled to an integrated circuit with a power output stage. This optocoupler is suited for driving power bipolar transistors and power Darlington devices used in motor control inverter applications. The high peak and steady state current capabilities of the output stage allow for direct interfacing to the power device without the need for an intermediate amplifier stage. With a CMR rating of 1.5 kV/μs this optocoupler readily rejects transients found in inverter applications.

The LED controls the state of the output stage. Transistor Q2 in the output stage is on with the LED off, allowing the base of the power device to be held low. Turning on the LED turns off transistor Q2 and switches on transistor Q1 in the output stage which provides current to drive the base of a power bipolar device.

OPTO COUPLERS

Schematic



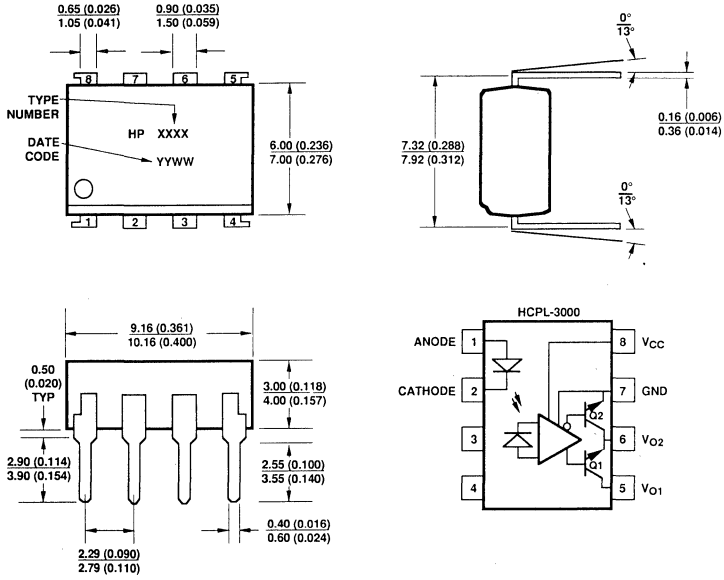
TRUTH TABLE

LED	OUTPUT	Q1	Q2
ON	HIGH LEVEL	ON	OFF
OFF	LOW LEVEL	OFF	ON

THE USE OF A 0.1μF BYPASS CAPACITOR CONNECTED BETWEEN PINS 8 AND 7 IS RECOMMENDED. ALSO, CURRENT LIMITING RESISTORS ARE RECOMMENDED (SEE FIGURE 1, NOTE 2, AND NOTE 7).

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Outline Drawing



Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (clearance)	L(IO1)	6.0	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	6.0	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.15	mm	Through insulation distance conductor to conductor

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Conditions	Fig.	Note
Storage Temperature		T_S	-55	125	°C			
Operating Temperature		T_A	-20	80	°C			
Input	Continuous Current	I_F		25	mA		9	1
	Reverse Voltage	V_R		6	V	T_A = 25°C		
Supply Voltage		V_{CC}		18	V			
Output 1	Continuous Current	I_{O1}		0.5	A		10,11	1
	Peak Current			1.0	A	Pulse Width < 5 µs, Duty cycle = 1%		1
	Voltage	V_{O1}		18	V			
Output 2	Continuous Current	I_{O2}		0.6	A		10,11,12	1
	Peak Current			2.0	A	Pulse Width < 5 µs, Duty cycle = 1%	12	1
Output Power Dissipation		P_O		500	mW		10	1
Total Power Dissipation		P_T		550	mW		11	1
Lead Solder Temperature		260°C for 10 s, 1.0 mm below seating plane						

Thermal Resistance

Typical Output IC Junction to Ambient: θ_{JA}* = 200°C/W

*The value of θ_{JA} was derived with the optocoupler suspended in free air.

Demonstrated ESD Performance

Human Body Model: MIL-STD-883 Method 3015.7: Class 2

Machine Model: EIAJ IC-121-1988 (1988.3.28 Version 2), Test Method 20, Condition C: 1200 V

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	5.4	13	Volts
Input Current (ON)	$I_{F(ON)}$	8*	20	mA
Input Current (OFF)	$I_{F(OFF)}$	-	0.2	mA
Operating Temperature	T_A	-20	80	°C

*The initial switching threshold is 5 mA or less.

Recommended Protection For Output Transistors

During switching transitions, the output transistors Q1 and Q2 of the HCPL-3000 can conduct large amounts of current. Figure 1 describes a recommended circuit design showing current limiting resistors R1 and R2 which are necessary in order to prevent damage to the output transistors Q1 and Q2 (see Note 7). A bypass capacitor C1 is also recommended to reduce power supply noise.

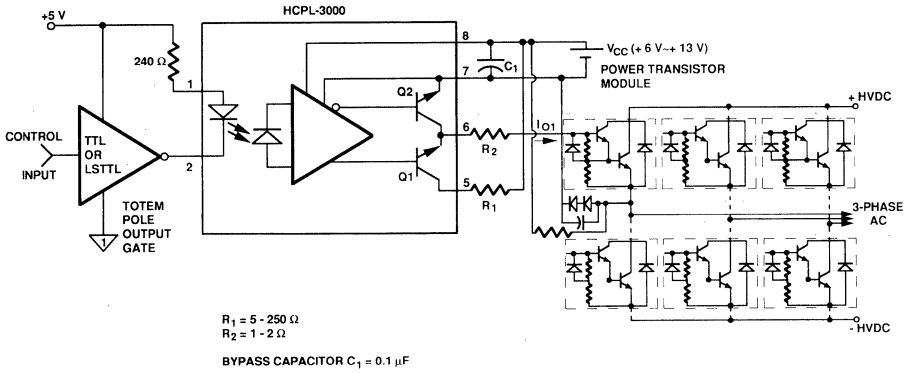


Figure 1. Recommended Output Transistor Protection and Typical Application Circuit.

Electrical Specifications

Over recommended temperature (T_A = -20°C to +80°C) unless otherwise specified.

Parameter		Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input Forward Voltage		V_F	-	1.1	1.4	V	I_F = 5 mA, T_A = 25°C	13	
			0.6	0.9	-	V	I_F = 0.2 mA, T_A = 25°C		
Input Reverse Current		I_R	-	-	10	μA	V_R = 3 V, T_A = 25°C		
Input Capacitance		C_{IN}	-	30	250	pF	V_F = 0 V, f = 1 kHz, T_A = 25°C		
Output 1	Low Level Voltage	V_{O1L}	-	0.2	0.4	V	V_{CC} = 6 V, I_{O1} = 0.4 A, R_{L2} = 10 Ω, I_F = 5 mA	2, 16, 17	2
	Leakage Current	I_{O1L}	-	-	200	μA	V_{CC} = 13 V, I_F = 0	4	
Output 2	High Level Voltage	V_{O2H}	4.5	5.0	-	V	V_{CC} = 6 V, I_{O2} = -0.4 A I_F = 5 mA	3, 18, 19	2
	Low Level Voltage	V_{O2L}	-	0.2	0.4	V	V_{CC} = 6 V, I_{O2} = 0.5 A, I_F = 0	20, 21	
	Leakage Current	I_{O2L}	-	-	200	μA	V_{CC} = 13 V, I_F = 5 mA	5	
Supply Current	High Level	I_{CCH}	-	9	13	mA	T_A = 25°C	22	2
			-	-	17		V_{CC} = 6 V, I_F = 5 mA		
	Low Level	I_{CCL}	-	11	15	mA	T_A = 25°C	23	
			-	-	20		V_{CC} = 6 V, I_F = 0		
Low to High Threshold Input Current		I_{FLH}	0.3	1.5	3.0	mA	T_A = 25°C	6, 14, 15	3
			0.2	-	5.0	mA	V_{CC} = 6 V, R_{L1} = 5 Ω, R_{L2} = 10 Ω		
Input-Output Insulation		V_{ISO}	5000			V_{RMS}	RH = 40% to 60%, t = 1 MIN, T_A = 25°C		4, 5
Resistance (Input - Output)		R_{I-O}	$5x10^{10}$	10^{11}	-	Ω	V_{I-O} = 500 V, T_A = 25°C, RH = 40%to 60%		4
Capacitance (Input-Output)		C_{I-O}	-	1.2	-	pF	f = 1 MHz		4

Switching Specifications

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	-	2	5	µs	V_{CC} = 6 V, I_F = 5 mA, R_{L1} = 5 Ω, R_{L2} = 10 Ω, T_A = 25°C	7, 24, 25	2, 6
Propagation Delay Time to Low Output Level	t_{PHL}	-	2	5				
Rise Time	t_R	-	0.2	1				
Fall Time	t_F	-	0.1	1				
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	1500	-	-	V/µs	V_{CM} = 600 V (peak), I_F = 5mA, R_{L1} = 470 Ω, R_{L2} = 1 kΩ, ΔV_{02H} = 0.5 V, T_A = 25°C	8	2
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	1500	-	-	V/µs	V_{CM} = 600 V (peak), I_F = 0, R_{L1} = 470 Ω, R_{L2} = 1 kΩ, ΔV_{02L} = 0.5 V, T_A = 25°C		

Notes:
1. Derate absolute maximum ratings with ambient temperatures as shown in Figures 9, 10 and 11.
2. A bypass capacitor of 0.01 µF or more is needed near the device between V_{CC} and GND when measuring output and transfer characteristics.
3. I_{FLH} represents the forward current when the output goes from low to high.
4. Device considered a two terminal device; pins 1-4 are shorted together and pins 5-8 are shorted together.
5. For devices with minimum V_{ISO} specified at 5000 V_{RMS}, in accordance with UL1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V_{RMS} for one second (leakage current detection limit, $I_{I-O} \leq 200$ µA).
6. The t_{PLH} and t_{PHL} propagation delays are measured from the 50% level of the input pulse to the 50% level of the output pulse.
7. R1 sets the base current (I_{01} in Figure 1) supplied to the power bipolar device. R2 limits the peak current seen by Q2 when the device is turning off. For more applications and circuit design information see Application Note "Power Transistor Gate/Base Drive Optocouplers."

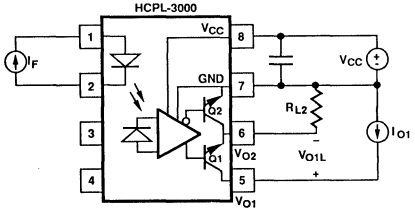


Figure 2. Test Circuit for Low Level Output Voltage V_{O1L}.

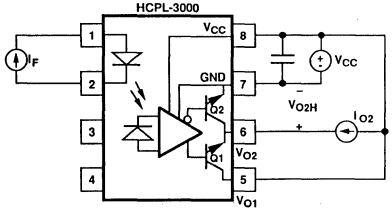


Figure 3. Test Circuit for High Level Output Voltage V_{O2H}.

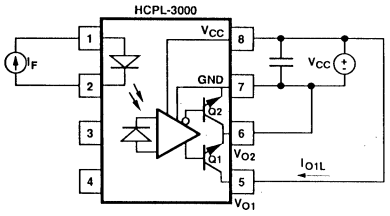


Figure 4. Test Circuit for Leakage Current I_{O1}.

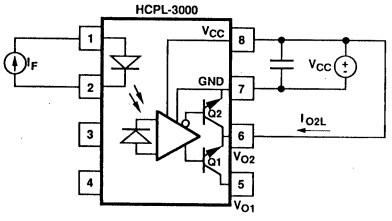


Figure 5. Test Circuit for Leakage Current I_{O2L}.

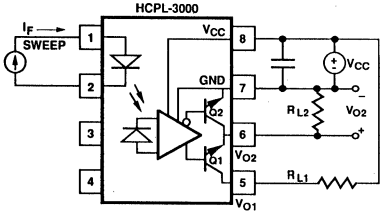


Figure 6. Test Circuit for Threshold Input Current I_{FLH}.

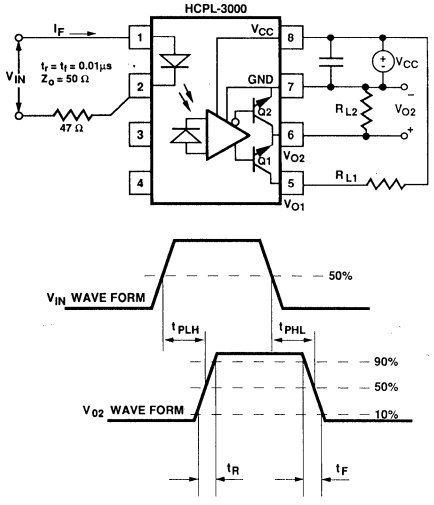


Figure 7. Test Circuit for t_{PLH}, t_{PHL}, t_R and t_F.

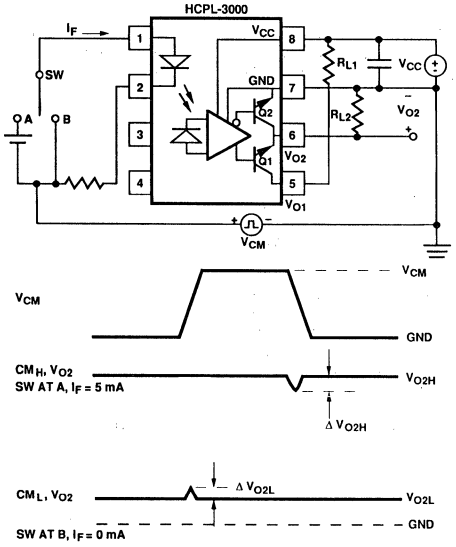


Figure 8. Test Circuit for CM_H and CM_L.

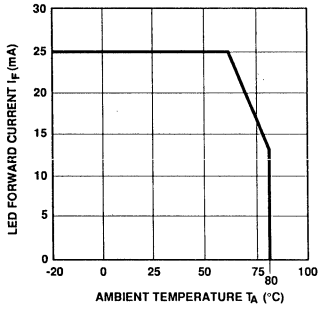


Figure 9. LED Forward Current vs. Ambient Temperature.

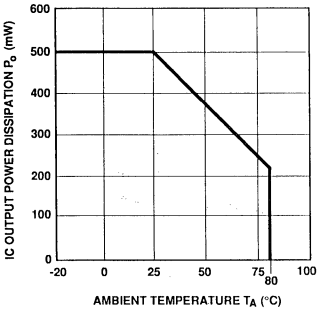


Figure 10. IC Output Power Dissipation vs. Ambient Temperature.

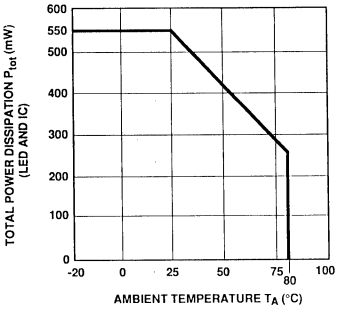


Figure 11. Total Power Dissipation vs. Ambient Temperature.

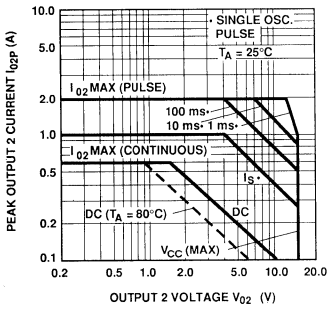


Figure 12. Typical Peak Output 2 Current vs. Output 2 Voltage (Safe Operating Area Q2).

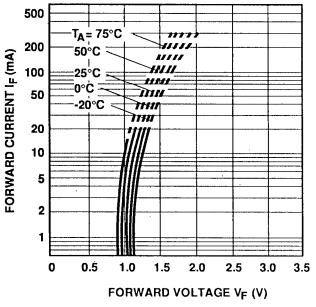


Figure 13. Typical Forward Current vs. Forward Voltage.

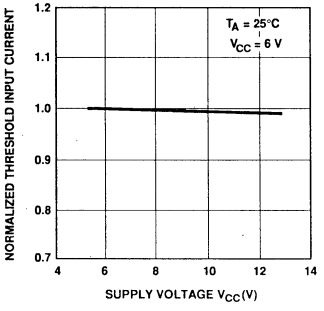


Figure 14. Normalized Low to High Threshold Input Current vs. Supply Voltage.

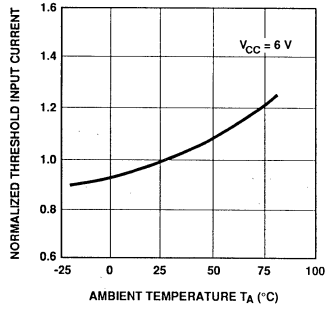


Figure 15. Normalized Low to High Threshold Input Current vs. Ambient Temperature.

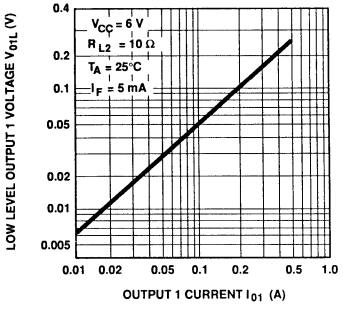


Figure 16. Typical Low Level Output 1 Voltage vs. Output 1 Current.

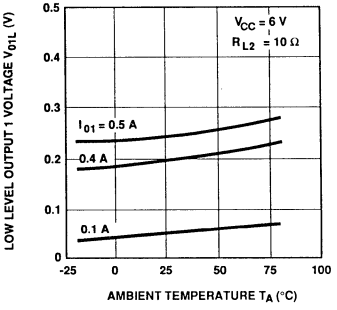


Figure 17. Typical Low Level Output 1 Voltage vs. Ambient Temperature.

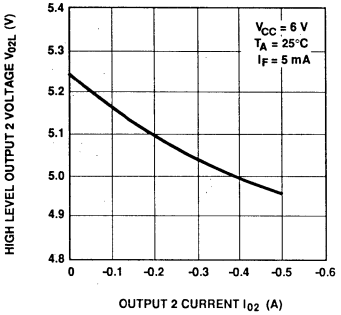


Figure 18. Typical High Level Output 2 Voltage vs. Output 2 Current.

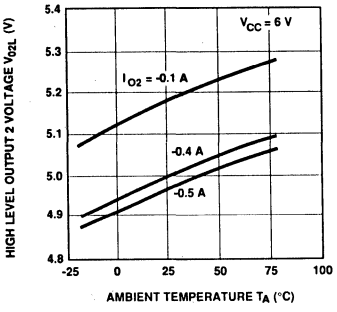


Figure 19. Typical High Level Output 2 Voltage vs. Ambient Temperature.

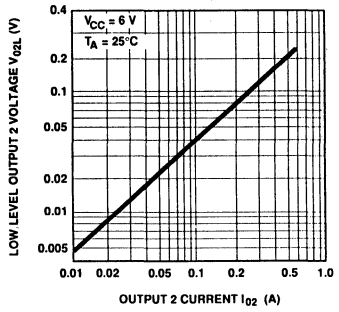


Figure 20. Typical Low Level Output 2 Voltage vs. Output 2 Current.

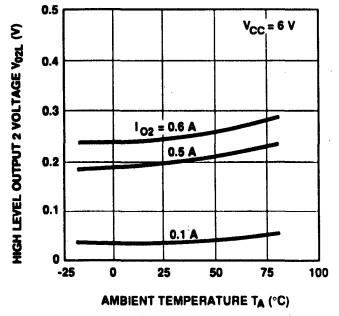


Figure 21. Typical Low Level Output 2 Voltage vs. Ambient Temperature.

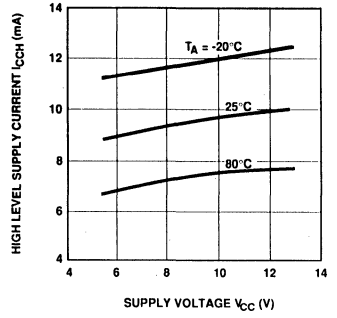


Figure 22. Typical High Level Supply Current vs. Supply Voltage.

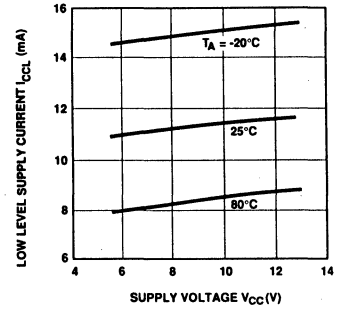


Figure 23. Typical Low Level Supply Current vs. Supply Voltage.

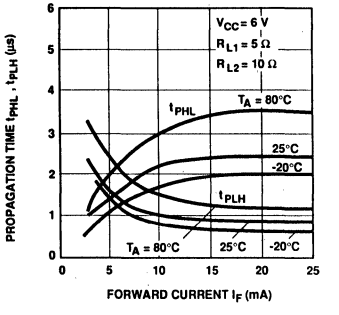


Figure 24. Typical Propagation Delay Time vs. Forward Current.

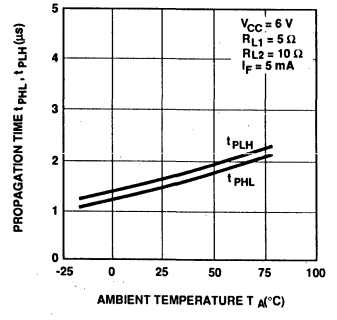


Figure 25. Typical Propagation Delay Time vs. Ambient Temperature.

HEWLETT PACKARD

New

Power MOSFET/IGBT Gate Drive Optocouplers

Technical Data

HCPL-3100
HCPL-3101

Features

- **High Output Current**
  I_{O1} and I_{O2} (0.4 A Peak, 0.1 A Continuous)
- **High Common Mode Rejection (CMR): 5 kV/µs at V_{CM} = 600 V**
- **Wide Operating V_{CC} Range (15 to 30 Volts)**
- **High Speed**
  1 µs Propagation Delay (HCPL-3100)
  0.3 µs Propagation Delay (HCPL-3101)
- **Recognized Under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 5000 VAC, 1 Minute**

Applications

- **Isolated MOSFET/IGBT Gate Drive**
- **AC and DC Motor Drives**
- **General Purpose Industrial Inverters**
- **Uninterruptable Power Supply**

Description

The HCPL-3100/3101 consists of an LED* optically coupled to an integrated circuit with a power output stage. These optocouplers are suited for driving power MOSFETs and IGBTs used in motor control inverter applications. The high operating voltage range of the output stage provides the voltage drives required by gate controlled devices. The voltage and current supplied by these optocouplers allow for direct interfacing to the power device without the need for an intermediate amplifier stage.

The HCPL-3100 switches a 3000 pF load in 2 µs and the HCPL-3101, using a higher speed LED, switches a 3000 pF load in 0.5 µs. With a CMR rating of 5 kV/µs typical these optocouplers readily reject transients found in inverter applications.

The LED controls the state of the output stage. Transistor Q2 in the output stage is on with the LED off, allowing the gate of the power device to be held low. Turning on the LED turns off transistor Q2 and switches on transistor Q1 in the output stage which provides current and voltage to drive the gate of the power device.

OPTO COUPLERS

*HCPL-3100 LED contains Silicon-doped GaAs and HCPL-3101 LED contains AlGaAs.

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Thermal Resistance

Typical Output IC Junction to Ambient: θ_{JA}* = 180°C/W

*The value of θ_{JA} was derived with the optocoupler suspended in free air.

Demonstrated ESD Performance

Human Body Model: MIL-STD-883 Method 3015.7: Class 2

Machine Model: EIAJ IC-121-1988 (1988.3.28 Version 2), Test Method 20, Condition C: 1200 V

Recommended Operating Conditions

Parameter	Symbol	Device	Min.	Max.	Units
Power Supply Voltage	V_{CC}		15	30*	Volts
			15	24	Volts
Input Current (ON)	$I_{F(ON)}$	HCPL-3100	12**	24	mA
		HCPL-3101	8**	16	mA
Input Current (OFF)	$I_{F(OFF)}$	HCPL-3100	-	0.6	mA
		HCPL-3101	-	0.2	mA
Operating Temperature	T_A		-25	80	°C

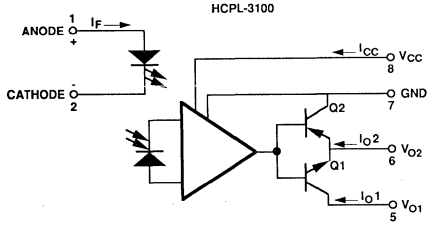
*For T_A = -10°C to 60°C.

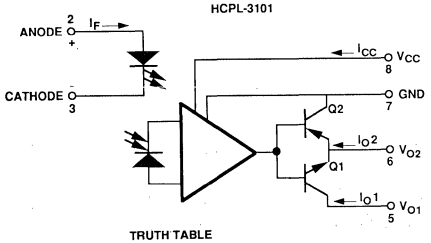
**The initial switching threshold is 10 mA or less for the HCPL-3100 and 5 mA or less for the HCPL-3101.

Recommended Protection For Output Transistors

During switching transitions, the output transistors Q1 and Q2 of the HCPL-3100/3101 can conduct large amounts of current. Figure 1 describes a recommended circuit design showing a current limiting resistor R2 which is necessary in order to prevent damage to the output transistors Q1 and Q2. (See Note 7.) A bypass capacitor C1 is also recommended to reduce power supply noise.

Schematic



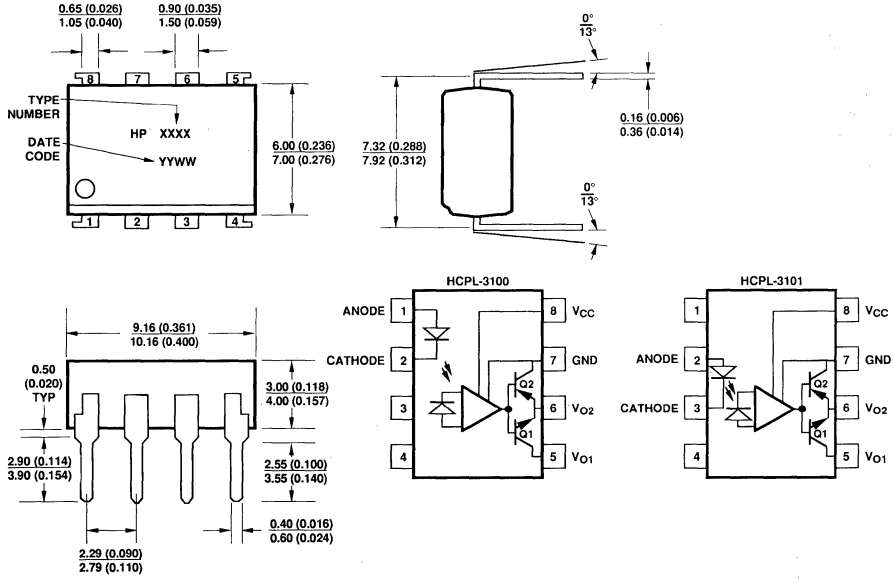


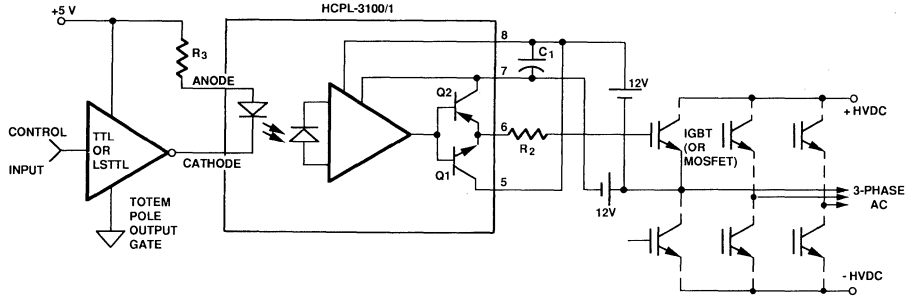
THE USE OF A 0.1 μF BYPASS CAPACITOR CONNECTED BETWEEN PINS 8 AND 7 IS RECOMMENDED. ALSO CURRENT LIMITING RESISTOR IS RECOMMENDED (SEE FIGURE 1, AND NOTE 2 AND NOTE 7).

TRUTH TABLE

LED	OUTPUT	Q1	Q2
ON	HIGH LEVEL	ON	OFF
OFF	LOW LEVEL	OFF	ON

Outline Drawing





R_2 = 25 - 100 Ω
R_3 = 180 Ω (HCPL-3100)
240 Ω (HCPL-3101)

BYPASS CAPACITOR C_1 = 0.1 μF

Figure 1. Recommended Output Transistor Protection and Typical Application Circuit.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	6.0	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	6.0	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.15	mm	Through insulation distance conductor to conductor

Absolute Maximum Ratings

Parameter		Symbol	Device	Min.	Max.	Unit	Conditions	Fig.	Note
Storage Temperature		T_S		-55	125	°C			
Operating Temperature		T_A		-25	80	°C			
Input	Continuous Current	I_F	HCPL-3100		25	mA		11	1
			HCPL-3101		20	mA		11	1
	Reverse Voltage	V_R			6	V	T_A = 25°C		
Supply Voltage		V_{CC}			35	V			
Output 1	Continuous Current	I_{O1}			0.1	A			1
	Peak Current				0.4	A	Pulse Width < 0.15 µs, Duty cycle = 1%		1
	Voltage	V_{O1}			35	V			
Output 2	Continuous Current	I_{O2}			0.1	A			1
	Peak Current				0.4	A	Pulse Width < 0.15 µs, Duty cycle = 1%		1
Output Power Dissipation		P_O			500	mW		12	1
Total Power Dissipation		P_T			550	mW		12	1
Lead Solder Temperature		260°C for 10 s, 1.0 mm below seating plane							

Electrical Specifications

Over recommended temperature (T_A = -25°C to +80°C) unless otherwise specified.

Parameter		Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Input Forward Voltage		V_F	HCPL-3100	-	1.2	1.4	V	I_F = 20 mA	T_A = 25°C	13	
				0.6	0.9	-	V	I_F = 0.2 mA			
			HCPL-3101	-	1.6	1.75	V	I_F = 10 mA		14	
				1.2	1.5	-	V	I_F = 0.2 mA			
Input Reverse Current		I_R	HCPL-3100	-	-	10	µA	V_R = 4 V	T_A = 25°C		
			HCPL-3101					V_F = 5 V			
Input Capacitance		C_{IN}		-	30	250	pF	V_F = 0 V, f = 1 kHz, T_A = 25°C			
Output 1	Low Level Voltage	V_{O1L}	HCPL-3100	-	0.2	0.4	V	I_F = 10 mA	V_{CC1} = 12 V, I_{O1} = 0.1 A, V_{CC2} = -12 V	2, 17, 18	2
			HCPL-3101					I_F = 5 mA			
	Leakage Current	I_{O1L}		-	-	500	µA	V_{CC} = V_{O1} = 35 V, I_F = 0, T_A = 25°C		5	
Output 2	High Level Voltage	V_{O2H}	HCPL-3100	18	21	-	V	I_F = 10 mA	V_{CC} = 24 V, V_{O1} = 24 V, I_{O2} = -0.1 A	3, 19, 20	2
			HCPL-3101					I_F = 5 mA			
	Low Level Voltage	V_{O2L}		-	1.2	2.0	V	V_{CC} = 24 V, I_{O2} = 0.1 A, I_F = 0		4, 21, 22	
	Leakage Current	I_{O2L}	HCPL-3100	-	-	500	µA	I_F = 10 mA	V_{CC} = 35 V, V_{O1} = 35 V, T_A = 25°C	6	
			HCPL-3101					I_F = 5 mA			
Supply Current	High Level	I_{CCH}	HCPL-3100	-	6	10	mA	T_A = 25°C		7, 23	2
				-	-	14	mA	V_{CC} = 24 V, I_F = 10 mA			
			HCPL-3101	-	6	10	mA	T_A = 25°C			
				-	-	14	mA	V_{CC} = 24 V, I_F = 5 mA			
	Low Level	I_{CCL}		-	8	13	mA	T_A = 25°C	V_{CC} = 24 V, I_F = 0 mA	7, 24	
				-	-	17	mA				
Low to High Threshold Input		I_{FLH}	HCPL-3100	1.0	4.0	7.0	mA	T_A = 25°C		8, 15, 16	2, 3
				0.6	-	10.0	mA	V_{CC} = 24 V			
			HCPL-3101	0.3	1.5	3.0	mA	T_A = 25°C			
				0.2	-	5.0	mA	V_{CC} = 24 V			
Input-Output Insulation		V_{ISO}		5000			V_{RMS}	RH = 40% to 60%, t = 1 MIN, T_A = 25°C			4, 5
Resistance (Input - Output)		R_{I-O}		$5x10^{10}$	10^{11}	-	Ω	V_{I-O} = 500 V, T_A = 25°C, RH = 40%to 60%			4
Capacitance (Input-Output)		C_{I-O}		-	1.2	-	pF	f = 1 MHz			4

Switching Specifications

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	HCPL-3100	-	1	2	µs	I_F = 10 mA	V_{CC} = 24 V, R_G = 47 Ω, C_G = 3000 pF, T_A = 25°C	9, 25, 26, 27	2, 6
		HCPL-3101	-	0.3	0.5	µs	I_F = 5 mA			
Propagation Delay Time to Low Output Level	t_{PHL}	HCPL-3100	-	1	2	µs	I_F = 10 mA			
		HCPL-3101	-	0.3	0.5	µs	I_F = 5 mA			
Rise Time	t_R	HCPL-3100	-	0.2	0.5	µs	I_F = 10 mA			
		HCPL-3101					I_F = 5 mA			
Fall Time	t_F	HCPL-3100	-	0.2	0.5	µs	I_F = 10 mA			
		HCPL-3101					I_F = 5 mA			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	HCPL-3100	1500	5000	-	V/µs	I_F = 10 mA	V_{CM} = 600 V (peak), V_{CC} = 24 V $\Delta V_{02H} = \Delta V_{02L}$ = 2.0 V, T_A = 25°C	10	2
		HCPL-3101					I_F = 5mA			
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$		1500	5000	-	V/µs	I_F = 0			

Notes:

1. Derate absolute maximum ratings with ambient temperatures as shown in Figures 11 and 12.
2. A bypass capacitor of 0.01 µF or more is needed near the device between V_{CC} and GND when measuring output and transfer characteristics.
3. I_{FLH} represents the forward current when the output goes from low to high.
4. Device considered a two terminal device; pins 1-4 are shorted together and pins 5-8 are shorted together.
5. For devices with minimum V_{ISO} specified at 5000 V_{RMS}, in accordance with UL1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V_{RMS} for one second (leakage current detection limit, $I_{I-O} \leq 200$ µA).
6. The t_{PLH} and t_{PHL} propagation delays are measured from the 50% level of the input pulse to the 50% level of the output pulse.
7. R2 limits the Q1 and Q2 peak currents. For more applications and circuit design information see Application Note "Power Transistor Gate/Base Drive Optocouplers."

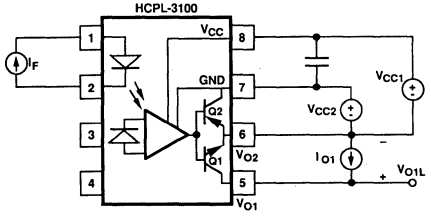


Figure 2. Test Circuit for Low Level Output Voltage V_{O1L}.

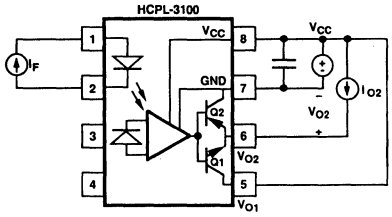


Figure 3. Test Circuit for High Level Output Voltage V_{O2H}.

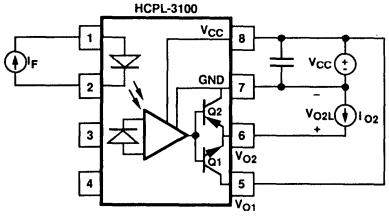


Figure 4. Test Circuit for Low Level Output Voltage V_{O2L}.

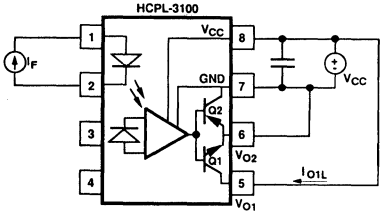


Figure 5. Test Circuit for Leakage Current I_{O1}.

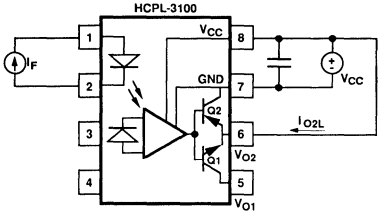


Figure 6. Test Circuit for Leakage Current I_{O2L}.

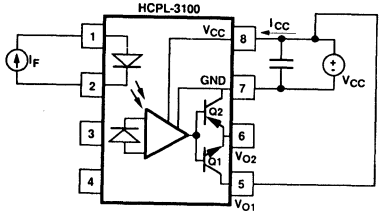


Figure 7. Test Circuit for I_{CCH} and I_{CCL}.

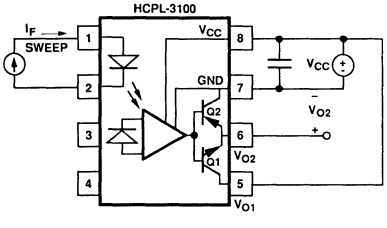


Figure 8. Test Circuit for Threshold Input Current I_{FLH}.

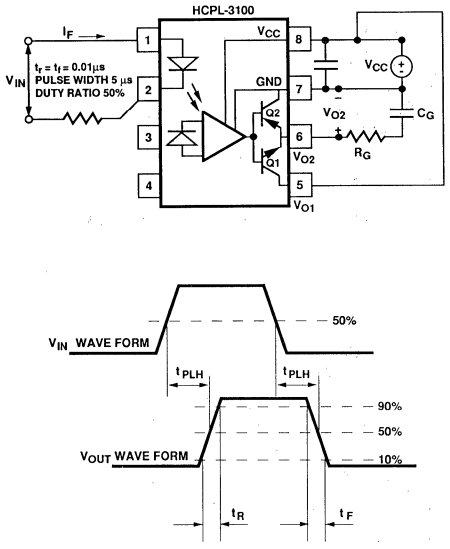


Figure 9. Test Circuit for t_{PLH}, t_{PHL}, t_R, and t_F.

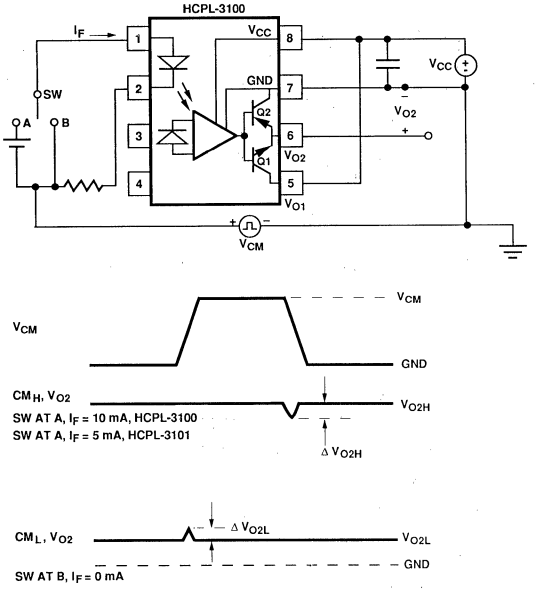


Figure 10. Test Circuit for CM_H and CM_L.

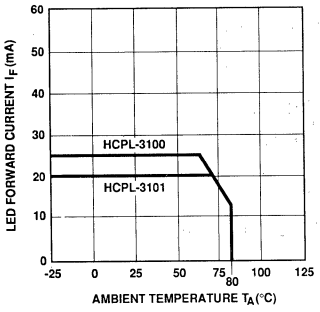


Figure 11. LED Forward Current vs. Ambient Temperature.

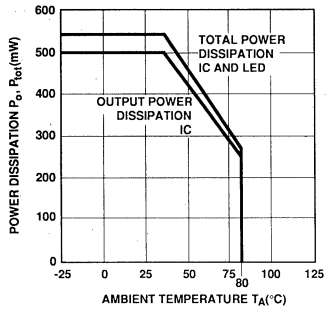


Figure 12. Power Dissipation vs. Ambient Temperature.

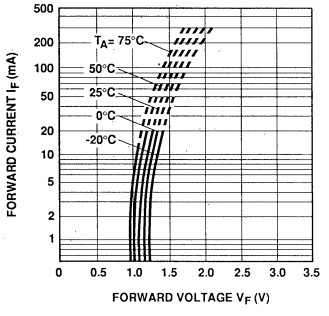


Figure 13. Typical Forward Current vs. Forward Voltage, HCPL-3100.

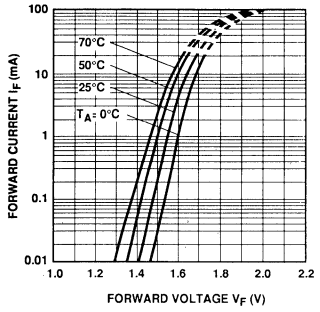


Figure 14. Typical Forward Current vs. Forward Voltage, HCPL-3101.

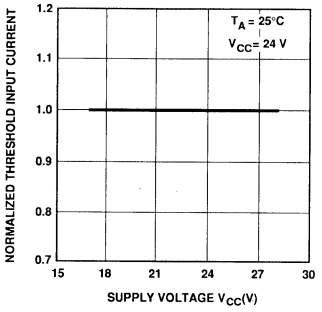


Figure 15. Normalized Low to High Threshold Input Current vs. Supply Voltage.

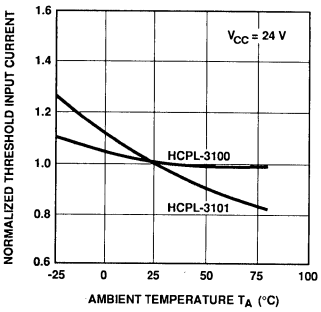


Figure 16. Normalized Low to High Threshold Input Current vs. Ambient Temperature.

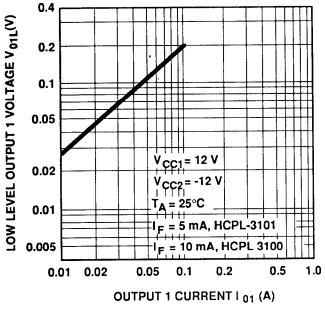


Figure 17. Typical Low Level Output 1 Voltage vs. Output 1 Current.

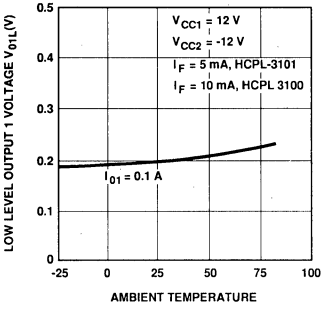


Figure 18. Typical Low Level Output 1 Voltage vs. Ambient Temperature.

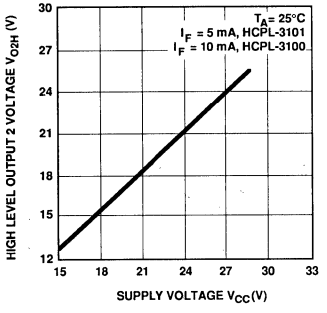


Figure 19. Typical High Level Output 2 Voltage vs. Supply Voltage.

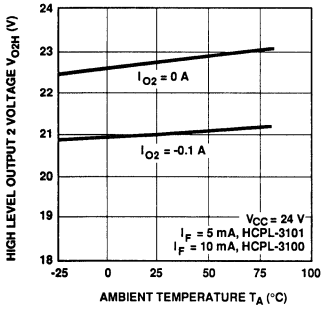


Figure 20. Typical High Level Output 2 Voltage vs. Ambient Temperature.

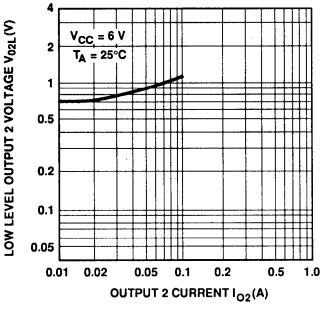


Figure 21. Typical Low Level Output 2 Voltage vs. Output 2 Current.

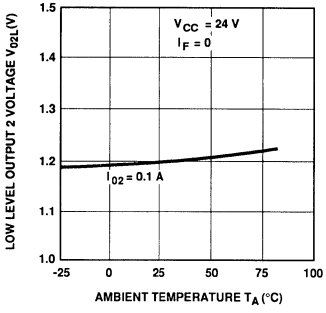


Figure 22. Typical Low Level Output 2 Voltage vs. Ambient Temperature.

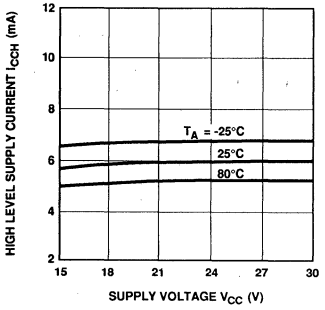


Figure 23. Typical High Level Supply Current vs. Supply Voltage.

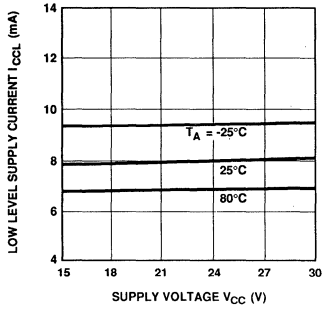


Figure 24. Typical Low Level Supply Current vs. Supply Voltage.

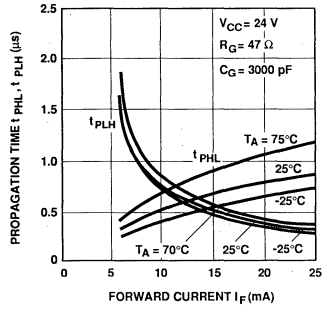


Figure 25. Typical Propagation Delay Time vs. Forward Current, HCPL-3100.

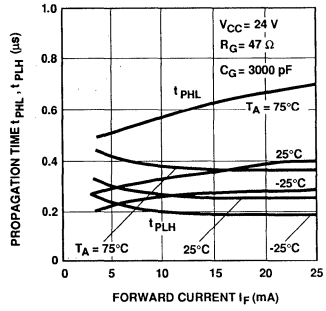


Figure 26. Typical Propagation Delay Time vs. Forward Current, HCPL-3101.

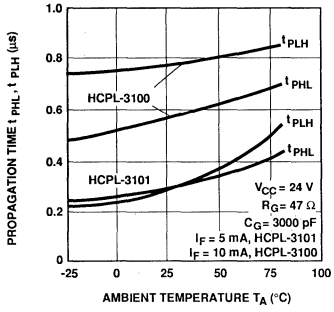


Figure 27. Typical Propagation Delay Time vs. Ambient Temperature.

HEWLETT PACKARD

Optocoupler Option for 5000 Vac/1 Minute Requirement

Technical Data

OPTION 020

Features

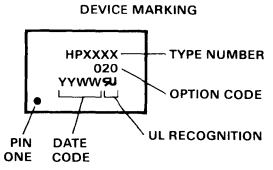
- **Special Construction and Testing**
- **UL Recognition for 5000 Vac/1 Minute Requirement (File No. E55361)**

Description

Option 020 consists of special construction on a wide range of Hewlett-Packard plastic optocouplers. After assembly, each unit is subjected to an equivalent electrical performance test to ensure its capability to withstand 5000 Vac input to output for one minute. This test is recognized by Underwriters Laboratory as proof that these components may be used in many high voltage applications.

Applications

Dielectric withstand voltage ratings are required by Underwriters Laboratory when components are used in certain types of electronic equipment. The voltage rating depends on the type of electronic equipment and the specific application within the equipment. The 5000 Vac/1 Minute dielectric withstand voltage rating provided by Option 020 offers excellent high voltage input to output protection. Some applicable UL documents are listed below.



UL Spec Number	Specification Title
114	Appliance and Business Equipment
347	High Voltage Industrial Control Equipment
508	Industrial Control Equipment
544	Medical and Dental Equipment
773	Plug-in, Locking Type Photocontrols
916	Standard for Energy Management Equipment
1012	Power Supplies
1244	Electrical and Electronic Measuring and Testing Equipment
1410	Television and Video Products
1950	Information Technology Equipment Including Electrical Business Equipment

Specifications

All specifications for optocouplers remain unchanged when this option is ordered. The 5000 VAC/1 Minute capability is validated by a factory 6200 VAC/1 Second dielectric voltage withstand test.

Ordering Information

To obtain this high voltage capability on plastic optocouplers order the standard part number and Option 020.

Examples:

6N135	HCPL-2601
Option 020	Option 020

This option is currently available on the following plastic optocouplers.

6N135/6
6N137
6N138/9
HCPL-2601/11
HCPL-4562
HCPL-4502/3
HCPL-2530/1, -4534 (pending)
HCPL-2630/1, -4661 (pending)
HCPL-2730/1 (pending)

Contact your local HP Sales Representative concerning availability of this option for optocouplers not listed.

HEWLETT PACKARD

Gull Wing Surface Mount Option for Optocouplers and Solid State Relays

Technical Data

Option 300

Description

Option 300 is available on most optocouplers and solid state relays. It consists of standard dual-in-line and 400 mil VDE approved package devices with gull wing leads. The lead profile is designed to be compatible with standard surface mount processes.

Option 300 enables electronic component assemblers to include Hewlett-Packard optocouplers and solid state relays on a PCB that utilizes surface mount processes. These options do not require "through holes" in a PCB. This reduces board costs, while potentially increasing assembly rates and component density per board. For the maximum solder reflow thermal profile, refer to Figure 4.

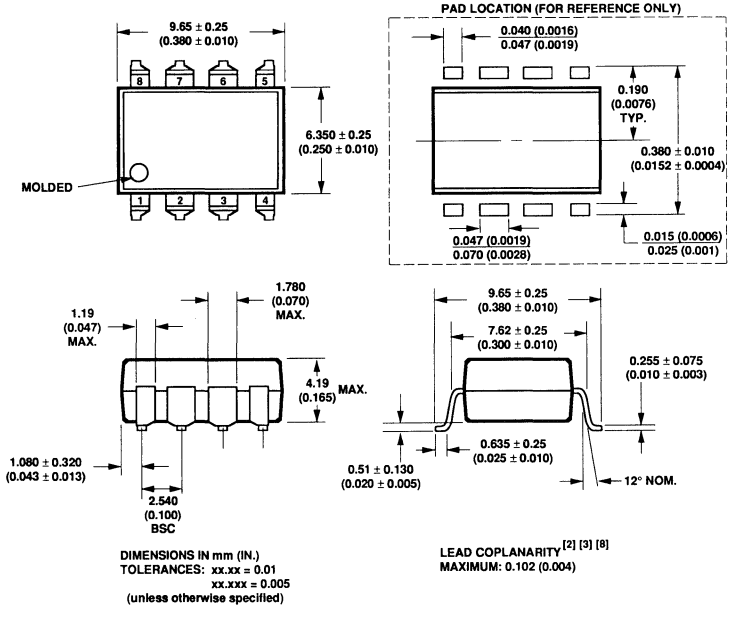


Figure 1. 8-Pin Device Outline Drawing.

Ordering Information

To obtain optocouplers and solid state relays with gull wing leads, order the standard part number and Option 300.

Example:
HCPL-2630
Option 300

Option 300 is shipped in tubes, with 50 units per tube. To obtain optocouplers and solid state relays with gull wing leads shipped in tape and reel, order Option 500[1] instead of Option 300.

OPTO COUPLERS

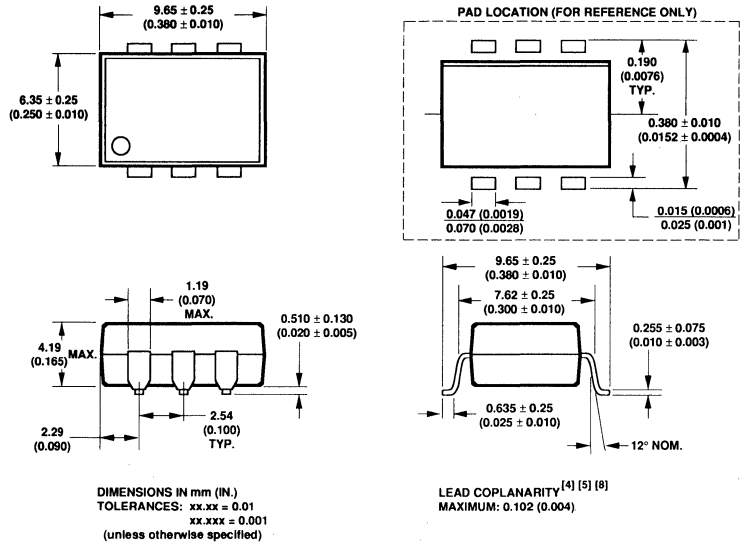


Figure 2. 6-Pin Device Outline Drawing.

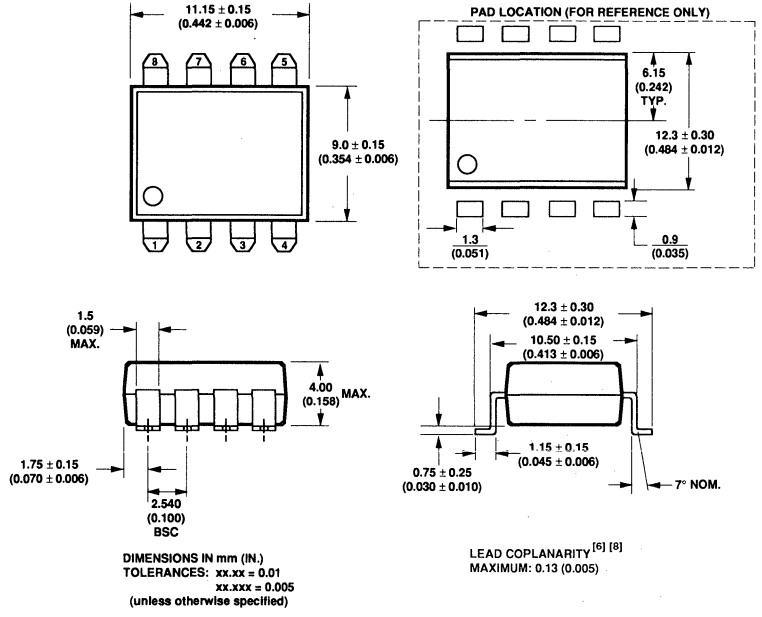


Figure 3. 8-Pin 400 mil Outline Drawing.

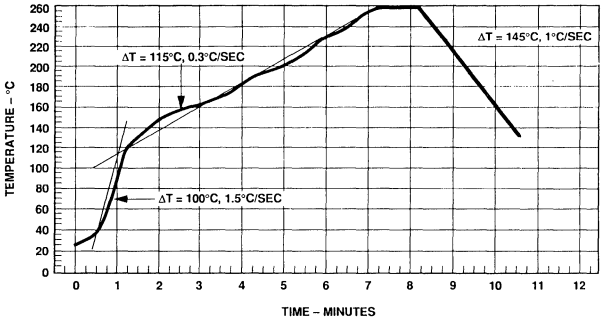


Figure 4. Maximum Solder Reflow Thermal Profile.[7]
(Note: Use of non-chlorine activated fluxes is recommended.)

Notes:
1. Tape and Reel Option 500 can also be obtained for small outline SOIC-8 optocouplers.
2. Lead coplanarity specification is valid for part numbers: 6N135/6/7/8/9, HCPL-2200/01/02/11/12/19/31/32, HCPL-2300, HCPL-2400/11/30, HCPL-2502/30/31, HCPL-2601/02/11/12/30/31, HCPL-3700/60, HCPL-4100, HCPL-4200, HCPL-4502/03/34/62, and HCPL-4661.
3. Guaranteed lead coplanarity is 6 mils for the following part numbers: HCPL-7100/1, HCPL-7601/11 and HCPL-7800/7800A/7800B.
4. Lead coplanarity specification is valid for part numbers 4N45/6.
5. Guaranteed lead coplanarity is 6 mils for HSSR-8060 and HSSR-8400.
6. Lead coplanarity specification is valid for part numbers: CNW135/6/8/9, CNW4502/3, and CNW4562.
7. Also valid for standard through hole DIP product.
8. Lead coplanarity definition: The maximum distance between the lowest and the highest pin when the package rests on a perfectly flat surface.

HEWLETT PACKARD

New

Tape and Reel Packaging Option for Optocouplers and Solid State Relays

Technical Data

Option 500

Description

Option 500 is available on most optocouplers and solid-state relays. It consists of devices with gull wing leads, shipped in a tape and reel. The following package styles and their corresponding tape and reel are available.

Style A: Small outline optocouplers with the SOIC-8 footprint, which are supplied in 12 mm wide tape on 33 cm diameter reels with 1500 units per reel.

Style B: 8-pin gull wing optocouplers and solid-state relays which are supplied in 16 mm wide tape on 33 cm diameter reels with 1000 units per reel.

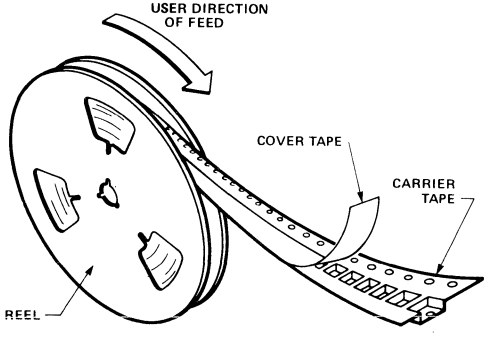
The above tape and reels conform to the EIA standard RS 481 Rev. A specifications.

Ordering Information

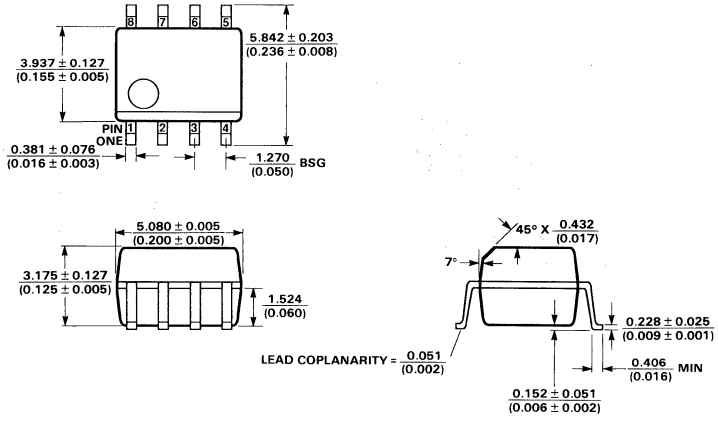
To obtain this tape and reel option for optocouplers and solid-state relays, order the standard part number with Option 500. All Option 500 units are supplied with the gull wing leads. Hence, there is no need to order Gull Wing Option 300 along with Option 500.

Example:
HCPL-2601
Option 500

The minimum order quantities are 1500 for Style A, and 1000 for Style B.

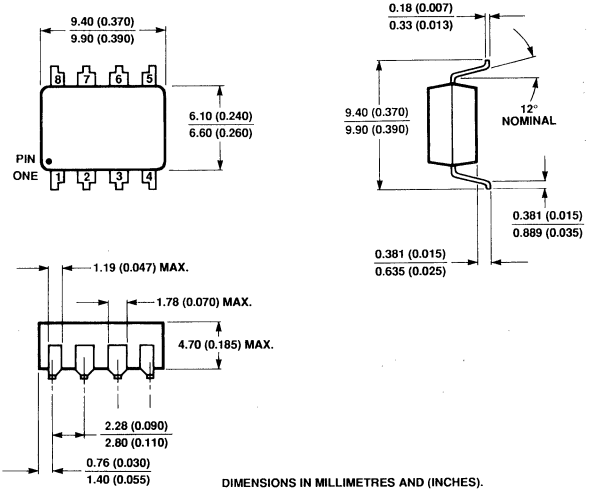


Dimensions of the Bulk Device



DIMENSIONS IN MILLIMETRES AND (INCHES)

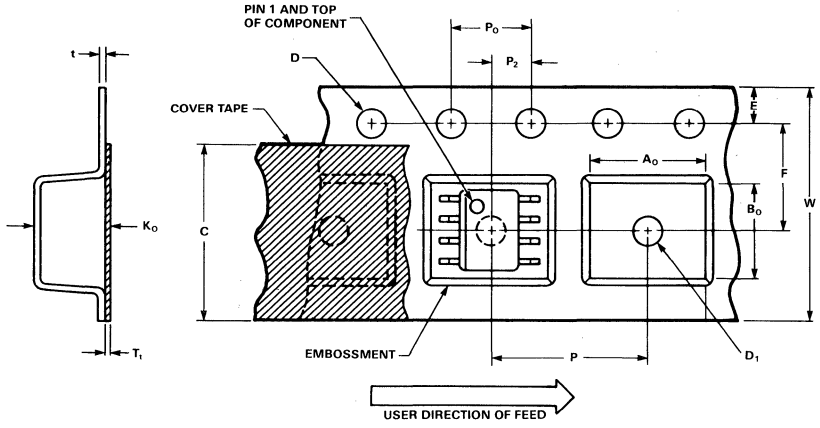
Style A: Small Outline SOIC-8 Package



DIMENSIONS IN MILLIMETRES AND (INCHES).

Style B: 8-Pin Gull Wing Package

Tape Dimensions



Item		Symbol	Size (mm)	
			Style A (SOIC-8)	Style B (8-pin Gull Wing)
Cavity	Length	A_O	6.30 ± 0.10	10.30 ± 0.10
	Width	B_O	5.35 ± 0.10	10.30 ± 0.10
	Depth	K_O	3.50 ± 0.10	4.90 ± 0.10
	Pitch	P	8.00 ± 0.10	12.00 ± 0.10
	Bottom Hole Diameter	D_1	1.50 min.	1.50 min.
	Component Rotation in Cavity (See Fig. 1)		15° max.	15° max.
Perforation	Diameter of Sprocket Holes	D	1.55 ± 0.05	1.55 ± 0.05
	Pitch	P_O	4.00 ± 0.10	4.00 ± 0.10
	Position	E	1.75 ± 0.10	1.75 ± 0.10
Cover Tape	Width	C	9.05 ± 0.10	13.05 ± 0.10
	Tape Thickness	T_t	0.065 ± 0.01	0.065 ± 0.01
Carrier Tape	Width	W	12.00 ± 0.30	16.00 ± 0.30
	Thickness	t	0.30 ± 0.05	0.30 ± 0.05
Distance Between Centerline	Cavity to Perforation (Width Direction)	F	5.50 ± 0.05	7.50 ± 0.10
	Cavity to Perforation (Length Direction)	P_2	2.00 ± 0.05	2.00 ± 0.10

Notes:
1. Drawing is not to scale.

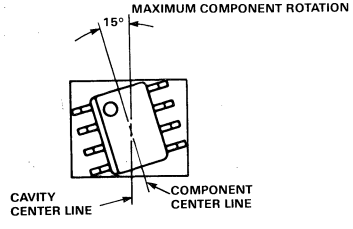
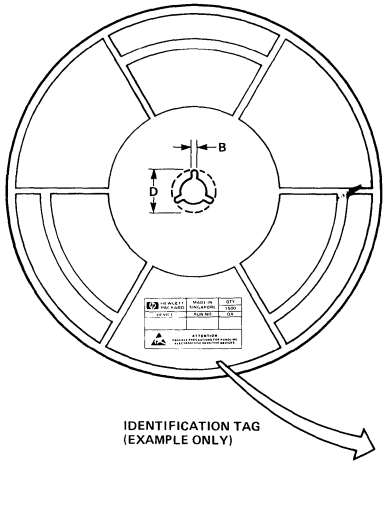
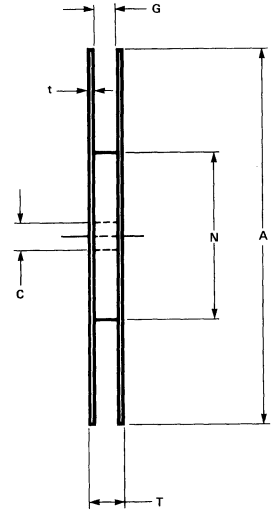


Figure 1.

Reel Dimensions



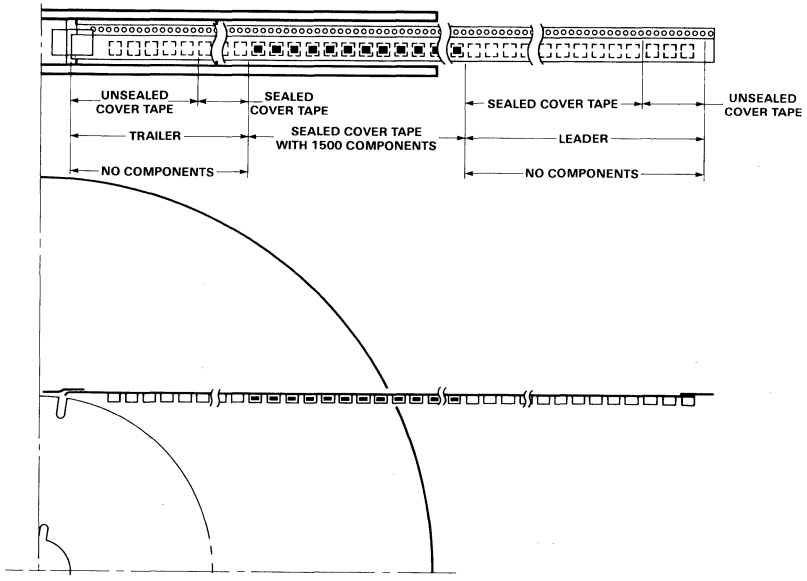
HEWLETT PACKARD	MADE IN SINGAPORE	QTY 1500
DEVICE	RUN NO.	QA
ATTENTION OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES		



Item			Symbol	Size (mm) Style A (SOIC-8)	Size (mm) Style B (8-pin Gull Wing)
Flange	Diameter		A	$330^{+0.0}_{-0.2}$	$330^{+0.0}_{-0.2}$
	Thickness (see note 2)		t	2.00	2.00
	Internal Width		G	$12.4^{+2.0}_{-0.0}$	$16.4^{+2.0}_{-0.0}$
	External Width		T	$16.4^{+2.0}_{-0.0}$	$20.4^{+2.0}_{-0.0}$
Hub	Outer Diameter		N	178.0 ± 0.1	100.0 ± 0.1
	Spindle Hole Diameter		C	13.0 ± 0.2	13.0 ± 0.2
	Key Slit	Width	B	1.9 ± 0.4	1.9 ± 0.4
		Diameter	D	$21.0^{+1.0}_{-0.0}$	$21.0^{+1.0}_{-0.0}$

Notes:
1. Drawing is not to scale.
2. Typical value only.

Packing – Leader and Trailer



Item		Size (mm)	
		Style A (SOIC-8)	**Style B (8-pin Gull Wing)**
Leader	Unsealed Cover Tape	24 (3 pockets)	24 (2 pockets)
	Sealed Cover Tape with Empty Cavities	504 (63 pockets)	480 (40 pockets)
Trailer	Unsealed Cover Tape	40 (5 pockets)	24 (2 pockets)
	Sealed Cover Tape with Empty Cavities	304 (38 pockets)	240 (20 pockets)

Materials

A. Carrier Tape:

Material: Carbon coating on both sides of polyvinyl chloride sheet.
Color: Black
Tensile strength: 530 Kgf/cm^2
Resistivity: $R_S = 10^6\ \Omega/cm^2$
$R_V = 10^{11}\ \Omega/cm^3$

B. Cover Tape:

Material: Cohesive failure type consisting of olephine-type resin. Static dissipative agent treated.
Color: Transparent
Tensile strength: 500 Kgf/cm^2
Peel-off strength: 40 ± 30 g
Resistivity: $R_S = 10^{11}\ \Omega/cm^2$

C. Reel:

Material: Plastic

HEWLETT PACKARD

New

60 V/0.7 Ω, General Purpose, 1 Form A, Solid State Relay

Technical Data

HSSR-8060

Features

- **Compact Solid-State Bidirectional Switch**
- **Normally-Off Single-Pole Relay Function (1 Form A)**
- **60 V Output Withstand Voltage in Both Polarities**
- **0.75/1.5 Amp Current Ratings (See Schematic for Connections A & B)**
- **Low Input Current; CMOS Compatibility**
- **Very Low On-resistance: 0.4 Ω Typical @ 25°C**
- **ac/dc Signal & Power Switching**
- **Input-to-Output Insulation Voltage: 2500 Vac, 1 Minute**
- **16-kV ESD Immunity: MIL-STD-883, Method 3015**
- **IEEE Surge Withstand Capability (IEEE STD 472-1974)**
- **CSA Approved**
- **UL 508 Approved**

Applications

- **Programmable Logic Controllers**
- **Telecommunication Switching Equipment**
- **Reed Relay Replacement**
- **28 Vdc, 24 Vac, 48 Vdc Load Driver**
- **Industrial Relay Coil Driver**

Description

The HSSR-8060 consists of a high-voltage circuit, optically coupled with a light emitting diode (LED). This device is a solid-state replacement for single-pole, normally-open (1 Form A) electromechanical relays used for general purpose switching of signals and low-power loads. The relay turns on (contact closes) with a minimum input current, I_F, of 5 mA through the input LED. The relay turns off (contact opens) with an input voltage, V_F, of 0.8 V or less. The detector contains a high speed photosensitive FET driver circuit and two high voltage MOSFETs.

This relay's logic level input control and very low typical output on-resistance of 0.4 Ω makes it suitable for both ac and dc loads. Connection A, as shown in the schematic, allows the relay to switch either ac or dc loads. Connection B, with the polarity and pin configuration as indicated in the schematic, allows the relay to switch dc loads only. The advantage of Connection B is that the on-resistance is significantly reduced, and the output current capability increases by a factor of two.

The electrical and switching characteristics of the HSSR-8060 are specified from -40°C to +85°C.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current (ON)	$I_{F(ON)}$	5	20	mA
Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	Volt
Operating Temperature	T_A	-40	+85	°C
Output Voltage				
Connection A	$V_{O(OFF)}$	-55	55	Volt
Connection B	$V_{O(OFF)}$	0	55	Volt

NOTE: At the time of printing this data sheet, HSSR-8200 (200 V/160 Ω) and HSSR-8400 (400 V/10 Ω) solid state relays were also available. For the most current list of solid state relays and options, you may contact your nearest Hewlett-Packard representative.

OPTO COUPLERS

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature – T_A ..... -40°C to +85°C
Case Temperature – T_C ..... +105°C[1]
Junction Temperature – T_J ..... +125°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Input Current – I_F ..... 20 mA
Repetitive Peak Input Current – I_F ..... 40 mA
(Pulse Width ≤ 1 ms; duty cycle ≤ 50%)
Transient Peak Input Current – I_F ..... 100 mA
(Pulse Width ≤ 200 μs; duty cycle ≤ 1%)
Reverse Input Voltage – V_R ..... 3 V
Input Power Dissipation ..... 40 mW
Output Voltage (T_A = 25°C)
Connection A – V_O ..... -60 to +60 V
Connection B – V_O ..... 0 to +60 V
Average Output Current – Figure 2
(T_A = 25°C, T_C ≤ 70°C)
Connection A – I_O ..... 0.75 A
Connection B – I_O ..... 1.50 A
Single Shot Peak Output Current
(100 ms pulse width, T_A = 25°C, I_F = 10 mA)
Connection A – I_O ..... 3.75 A
Connection B – I_O ..... 7.0 A
Output Power Dissipation ..... 750 mW[2]

Thermal Resistance

Typical Output MOSFET Junction to Case – θ_{JC} = 55°C/W

Demonstrated ESD Performance

Human Body Model: MIL-STD-883 Method 3015.7 – 16 kV
Machine Model: EIAJ IC-121-1988 (1988.3.28 Version 2), Test Method 20, Condition C – 1200 V

Surge Withstand Capability

IEEE STD 472-1974

CAUTION: Maximum Switching Frequency – Care should be taken during repetitive switching of loads so as not to exceed the maximum output current, maximum output power dissipation, maximum case temperature and maximum junction temperature.

Electrical Specifications

For -40°C ≤ T_A ≤ +85°C unless otherwise specified. All Typicals at T_A = 25°C.

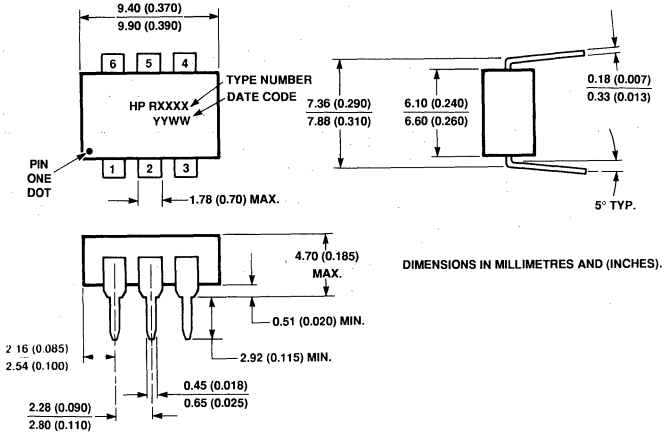
Parameter	Connection	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Output Withstand Voltage	A	$\|V_{O(OFF)}\|$	60			V	V_F = 0.8 V, I_O = 250 µA, T_A = 25°C	4	
			55				V_F = 0.8 V, I_O = 250 µA		
Output On-Resistance	A	$R_{(ON)}$		0.4	0.7	Ω	I_F = 10 mA, I_O = 750 mA (pulse duration ≤ 30 ms), T_A = 25°C	5, 6	3
	B			0.1	0.2				
	A				1.6		I_F = 10 mA, I_O = 750 mA (pulse duration ≤ 30 ms),		
	B				0.4				
Output Leakage Current	A	$I_{O(OFF)}$		10^{-4}	1.0	µA	V_F = 0.8 V, V_O = 60 V, T_A = 25°C	12	
Output Off-Capacitance	A	$C_{O(OFF)}$		135		pF	V_F = 0.8 V, V_O = 25 V, f = 1 MHz	13	
Output Offset Voltage	A	$\|V_{OS}\|$		1		µV	I_F = 5 mA, I_O = 0 mA	17	4
Input Rev. Breakdown Voltage		V_R	3			V	I_R = 100 µA		
Input Diode Temperature Coefficient		$\Delta V_F/\Delta T_A$		-1.3		mV/°C	I_F = 10 mA		
Input Forward Voltage		V_F	1.3	1.6	1.85	V	I_F = 10 mA ,T_A = 25°C	14	
Input Capacitance		C_{IN}		72		pF	V_F = 0 V, f = 1 MHz		
Input-Output Insulation Voltage		V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min, T_A = 25°C		5, 6
Input-Output Capacitance		C_{I-O}		1.0		pF	V_{I-O} = 0 V, f = 1 MHz		5
Input-Output Resistance		R_{I-O}		100		GΩ	V_{I-O} = 500 Vdc, t = 1 min, RH = 45%		5

Switching Specifications

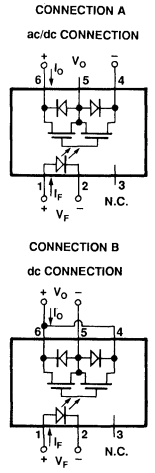
For -40°C ≤ T_A ≤ +85°C with Connection A, unless otherwise specified. All Typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Notes
Turn On Time	t_{ON}		0.93	1.4	ms	I_F = 10 mA, V_{DD} = 60 V, I_O = 750 mA, T_A = 25°C	1, 7, 8, 9	7
				1.8	ms	I_F = 10 mA, V_{DD} = 55 V, I_O = 750 mA		
Turn Off Time	t_{OFF}		0.013	0.1	ms	I_F = 10 mA, V_{DD} = 60 V, I_O = 750 mA, T_A = 25°C	1, 7, 10, 11	
				0.1	ms	I_F = 10 mA, V_{DD} = 55 V, I_O = 750 mA		
Output Transient Rejection	$\|dV_O/dt\|$	1000			V/µs	$V_{(peak)}$ = 60 V, $R_M \geq 1$ MΩ, C_M = 1000 pF, T_A = 25°C	15	
Input-Output Transient Rejection	$\|dV_{I-O}/dt\|$	2500			V/µs	V_{DD} = 5 V, $V_{I-O\ (peak)}$ = 1000 V, R_L = 1 kΩ, C_L = 25 pF, T_A = 25°C	16	

Outline Drawing

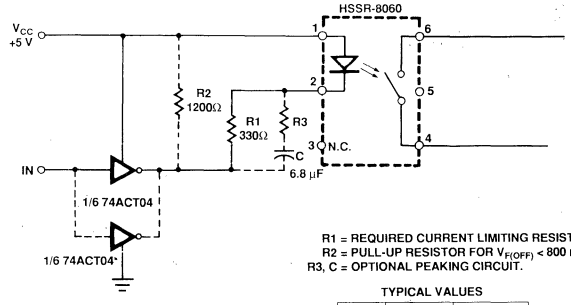


Schematic



Notes:

1. The case temperature, T_C, is measured at the center of the bottom of the package.
2. For derating, see Figure 3. The output power P_O derating curve is obtained when the part is handling the maximum average output current I_O as shown in Figure 2.
3. During the pulsed R_{ON} measurement (I_O duration ≤ 30 ms), ambient (T_A) and case temperature (T_C) are equal.
4. V_{OS} is a function of I_F, and is defined between pins 4 and 6, with pin 4 as the reference. V_{OS} must be measured in a stable ambient (free of temperature gradients).
5. Device considered a two terminal device: pins 1, 2, and 3 shorted together and pins 4, 5, and 6 shorted together.
6. This is a proof test. These parts are 100% tested in production at 3000 Vrms, one second.
7. For a faster turn-on time, the optional peaking circuit shown in Figure 1 may be implemented.



R1 = REQUIRED CURRENT LIMITING RESISTOR FOR $I_{F(ON)}$ = 10 mA.
R2 = PULL-UP RESISTOR FOR $V_{F(OFF)}$ < 800 mV; If (V_{CC} – V_{OH}) < 800 mV, OMIT R2.
R3, C = OPTIONAL PEAKING CIRCUIT.

TYPICAL VALUES

R_3 (Ω)	$I_{F(PK)}$ (mA)	HSSR-8060 t_{ON} (ms)
–	10 (no pk)	0.93
330	20	0.53
100	40	0.32
33	100	0.17

*USE SECOND GATE IF $I_{F(PK)}$ > 50 mA.

Figure 1. Recommended Input Circuit.

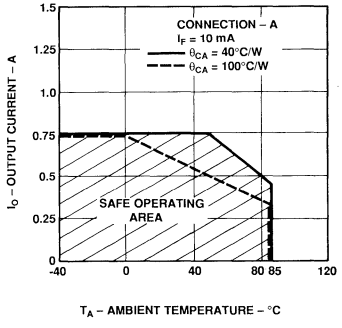


Figure 2A. Maximum Average Output Current Rating vs. Ambient Temperature.

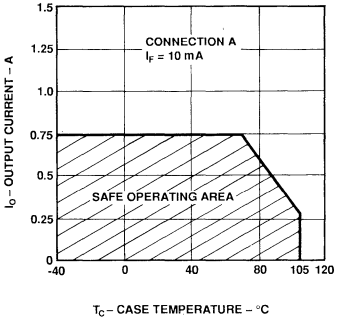


Figure 2B. Maximum Average Output Current Rating vs. Case Temperature.

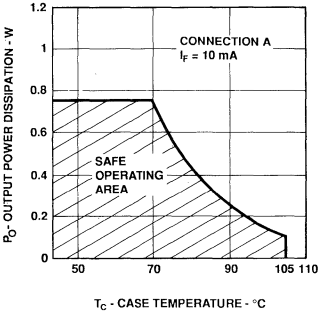


Figure 3. Output Power Derating vs. Case Temperature.

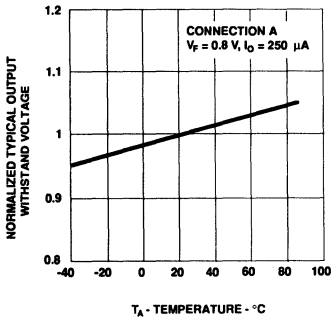


Figure 4. Normalized Typical Output Withstand Voltage vs. Temperature.

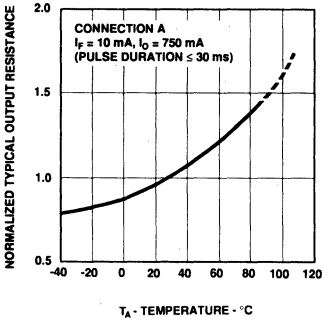


Figure 5. Normalized Typical Output Resistance vs. Temperature.

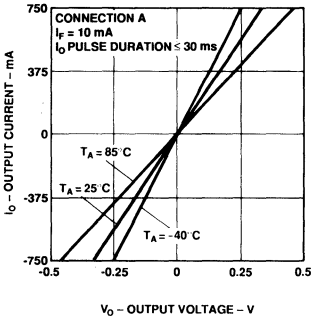
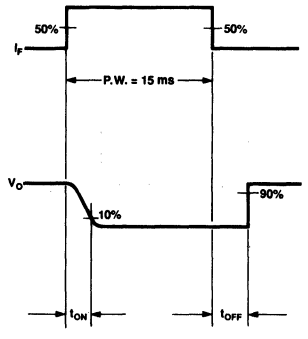


Figure 6. Typical On State Output I-V Characteristics.



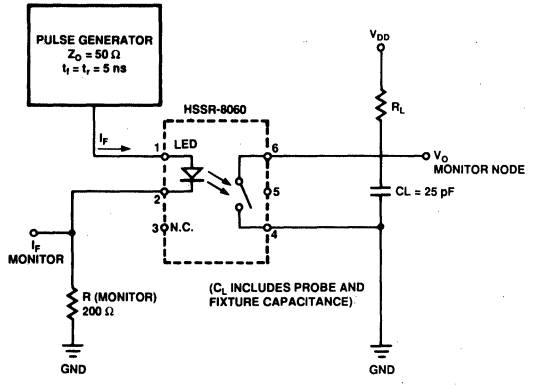


Figure 7. Switching Test Circuit for t_{ON}, t_{OFF}.

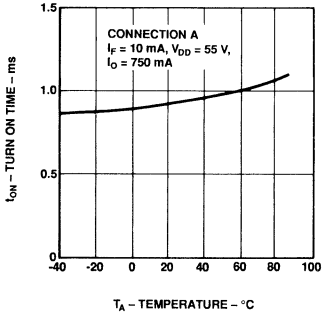


Figure 8. Typical Turn On Time vs. Temperature.

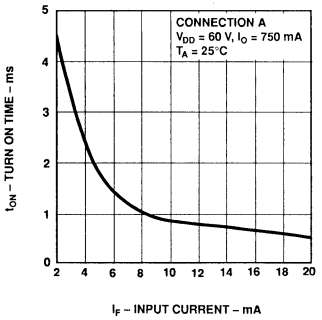


Figure 9. Typical Turn On Time vs. Input Current.

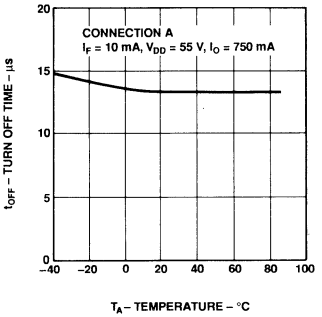


Figure 10. Typical Turn Off Time vs. Temperature.

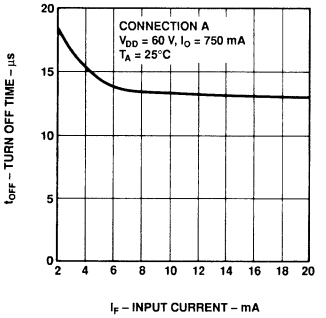


Figure 11. Typical Turn Off Time vs. Input Current.

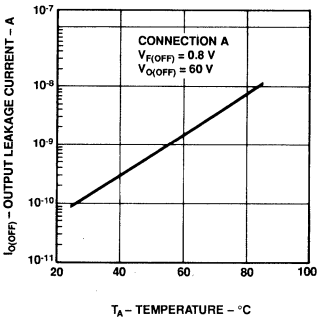


Figure 12. Typical Output Leakage Current vs. Temperature.

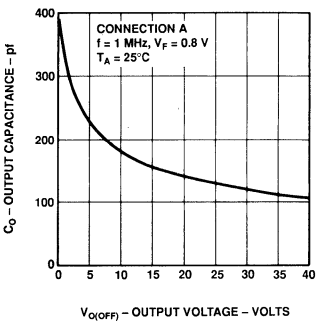


Figure 13. Typical Output Capacitance vs. Output Voltage.

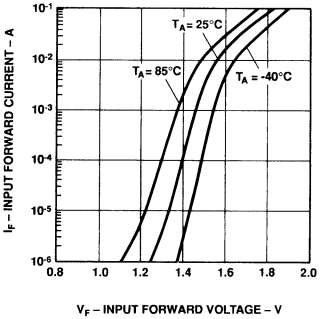


Figure 14. Typical Input Forward Current vs. Input Forward Voltage.

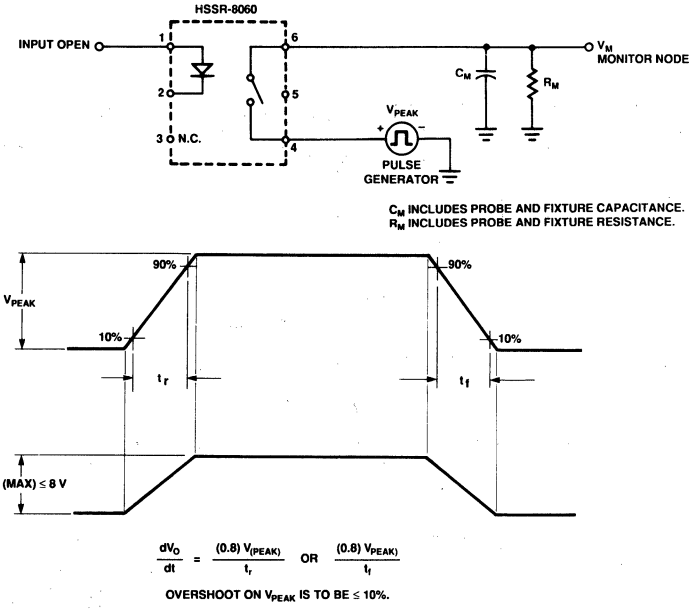


Figure 15. Output Transient Rejection Test Circuit.

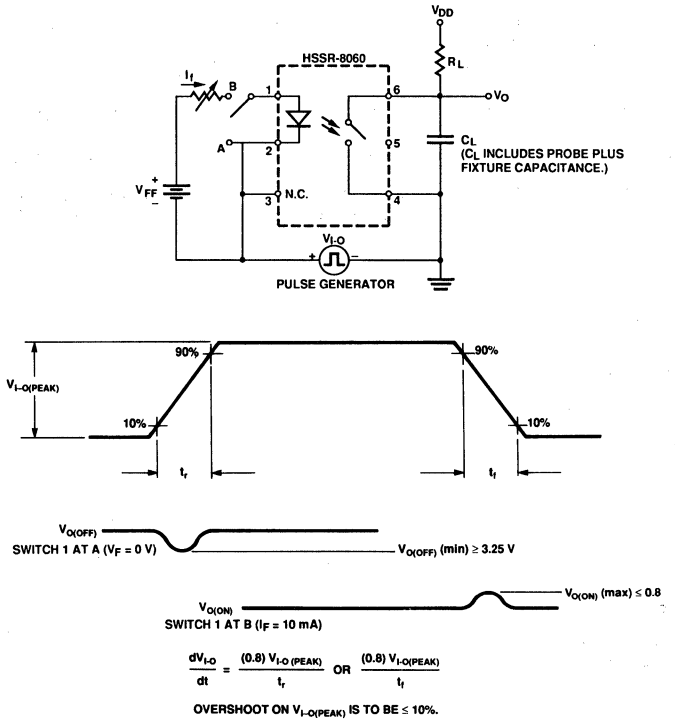


Figure 16. Input-Output Transient Rejection Test Circuit.

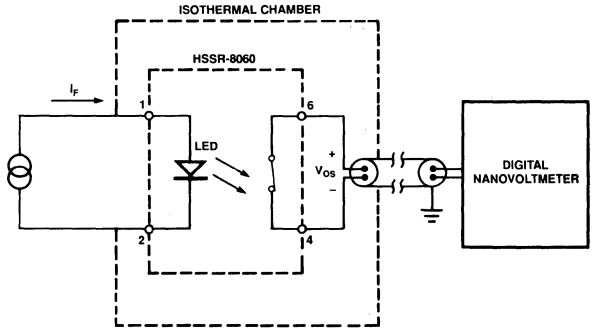


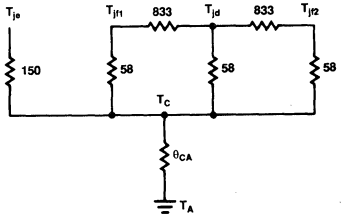
Figure 17. Voltage Offset Test Setup.

Applications Information

Thermal Model

The steady state thermal model for the HSSR-8060 is shown in Figure 18. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. The thermal resistances between the LED and other internal nodes are very large in comparison with the other terms and are omitted for simplicity. The components do, however, interact indirectly through θ_{CA}, the case-to-ambient thermal resistance. All heat generated flows through θ_{CA}, which raises the case temperature T_C accordingly. The value of θ_{CA} depends on the conditions of the board design and is, therefore, determined by the designer.

The typical value for each output MOSFET junction-to-case thermal resistance is specified as 55°C/W. This is the thermal resistance from one MOSFET junction to the case when power is dissipated equally in the MOSFETs. The power dissipation in the FET Driver is negligible in comparison to the MOSFETs.



T_{je} = LED JUNCTION TEMPERATURE
T_{jf1} = FET 1 JUNCTION TEMPERATURE
T_{jf2} = FET 2 JUNCTION TEMPERATURE
T_{jd} = FET DRIVER JUNCTION TEMPERATURE
T_C = CASE TEMPERATURE (MEASURED AT CENTER OF PACKAGE BOTTOM)
T_A = AMBIENT TEMPERATURE (MEASURED 6" AWAY FROM THE PACKAGE)
θ_{CA} = CASE-TO-AMBIENT THERMAL RESISTANCE

ALL THERMAL RESISTANCE VALUES ARE IN °C/W.

Figure 18. Thermal Model.

On-Resistance and Derating Curves

The output on-resistance, R_{ON}, specified in this data sheet, is the resistance measured across the output contact when a pulsed current signal (I_O = 750 mA) is applied to the output pins. The use of a pulsed signal (≤ 30 ms) implies that each junction temperature is equal to the ambient and case temperatures. The steady-state resistance, R_{SS}, on the other hand, is the value of the resistance measured across the output contact when a DC current signal is applied to the output pins for a duration sufficient to reach thermal equilibrium. R_{SS} includes the effects of the temperature rise of each element in the thermal model.

Derating curves are shown in Figures 2 and 3. Figure 2 specifies the maximum average output current allowable for a given ambient or case temperature. Figure 3 specifies the output power dissipation allowable for a given case temperature. Above a case temperature of 70°C, the maximum allowable output current and power dissipation are related by the expression $R_{SS} = P_O(max)/(I_O(max))^2$ from which R_{SS} can be calculated. Staying within the safe area assures that the steady state junction temperatures remain less than 125°C. As an example, for a case temperature of 80°C, Figure 3 shows that the output power dissipation should be limited to less than 0.5 watts. A check with Figure 2B shows that the output current should be limited to less than 640 mA. This yields an R_{SS} of 1.2 Ω.

Turn On Time Variation

For applications which are sensitive to turn on time, the designer should refer to Figures 19 and 20. These figures show that although there is very little variation in t_{ON} within most of the population, a portion of the distribution will vary with use. The optional peaking circuit shown in Figure 1 can be used to reduce the total turn on time and, consequently, any associated variation.

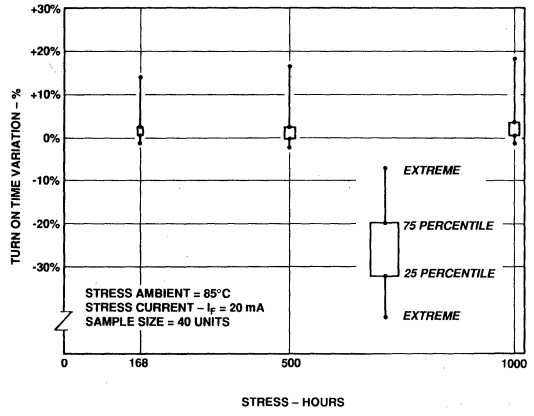


Figure 19. Turn On Time Variation with High Temperature Operating Life.

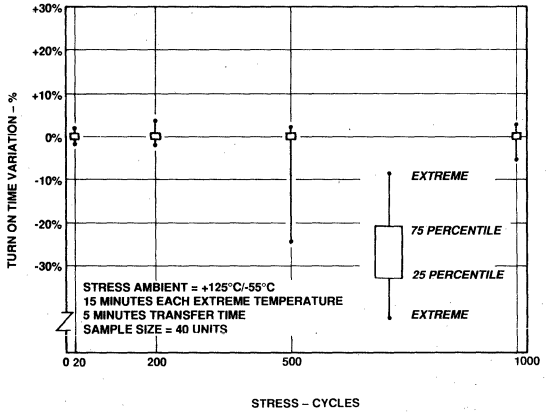


Figure 20. Turn On Time Variation with Temperature Cycling.

HEWLETT PACKARD

200-Volt/160-Ohm, 1 Form A Small-Signal Solid State Relay

Technical Data

HSSR-8200

Features

- Compact Solid-State Bi-Directional Signal Switch
- Normally-Off Single-Pole Relay Function (1 Form A)
- Very High Output Off-Impedance: 10,000 Gigaohms Typical at 25°C
- Very Low Output Offset Voltage: < 0.5 μV
- 200-Volt Output Withstand Voltage
- High-Transient Immunity: > 2000 V/μs
- Monolithic High-Voltage IC
- Operating Range: –40°C to +85C
- Very Low Input Current (1 mA); CMOS Compatibility
- High-Speed Switching: 50 μs Typical
- 160-Ohm Maximum On-Resistance at 25°C
- Surface Mount Option
- 8-kV ESD Immunity: MIL-STD-883 Method 3015
- Input-to-Output Insulation Voltage: 2500 Vac, 1 Minute
- UL Certification Pending

Applications

- Relay Scanners & Analog Input Modules of Data Acquisition Systems
- Analog Input Modules of Programmable Logic Controllers
- Relay Multiplexers of High-Performance Voltmeters
- Telecommunication Test Instruments
- Functional Tester of Board Test Equipment
- Analog Signal Multiplexer
- Flying Capacitor Multiplexer
- Reed Relay Replacement

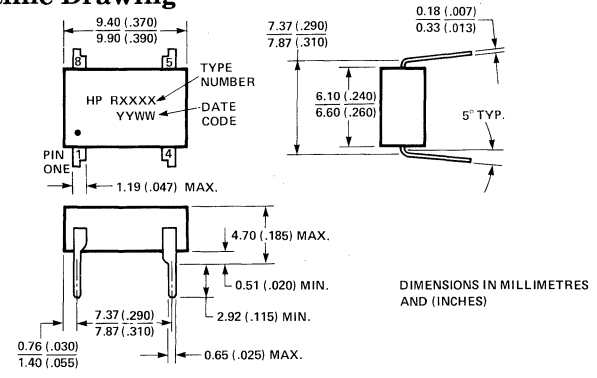
Description

The HSSR-8200 consists of a high-voltage integrated circuit optically coupled with a light emitting diode. This device is a solid-state replacement for single-pole, normally-open electromechanical relays used for general purpose switching of analog signals.

The light-emitting diode controls the ON/OFF function of the solid-state relay. The detector contains high voltage MOS transistors and a high speed photosensitive drive circuit. This relay has superior OFF impedance, very low output offset voltage and input drive current.

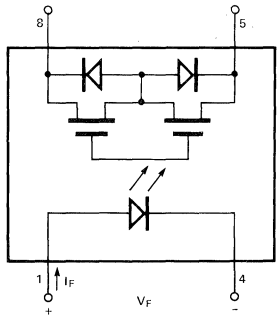
OPTO COUPLERS

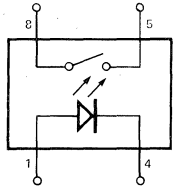
Outline Drawing



The electrical and switching characteristics of the HSSR-8200 are specified from –40°C to +85°C. The low I_F allows compatibility with TTL, LSTTL, and CMOS logic resulting in low power consumption compared to other solid state and mechanical relays.

Schematic





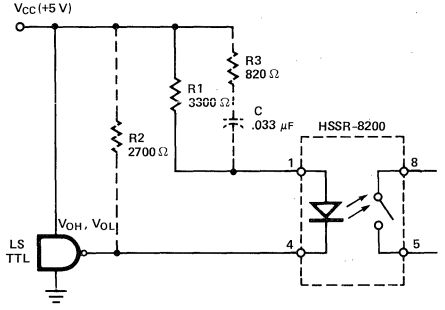
EQUIVALENT RELAY DIAGRAM

Recommended Operating Conditions

Description	Symbol	Min.	Max.	Units
Input Current (ON)	$I_{F(ON)}$	1	5	mA
Input Voltage (OFF)	$V_{F(OFF)}$	0	0.6	Volt
Operating Temperature	T_A	–40	+85	°C

Absolute Maximum Ratings

Storage Temperature ..... –55°C to 125°C
Operating Temperature ..... –40°C to +85°C
Lead Solder Temperature ..... 215°C for 30 s; Reflow Solder
260°C for 5 s; Wave Solder
Average Input Current – I_F ..... 10 mA
Repetitive Peak Input Current – I_F ..... 20 mA; 50% Duty Cycle
Transient Peak Input Current – I_F ..... 100 mA;
(≤ 1 µs pulse width; 1 kHz Pulse Repetition Rate)
Reverse Input Voltage ..... 5 V
Average Output Current – I_O ..... 40 mA[1]
Input-Output Insulation Voltage ..... 2500 VAC[6]
Output Power Dissipation ..... 320 mW[2]
Output Voltage – V_O ..... –200 V to 200 V



R1 – REQUIRED CURRENT-LIMITING RESISTOR FOR $I_{F(ON)}$ = 1 mA
R2 – PULL-UP RESISTOR FOR $V_{F(OFF)}$ < 600 mV; IF ($V_{CC} - V_{OH}$) < 600 mV, OMIT R2
R3, C – OPTIONAL PEAKING CIRCUIT FOR $I_{F(PK)}$ = 5 mA, t_{ON} < 200 µs

Figure 1. Recommended Input Circuit

Electrical Specifications

$-40°C \le T_A \le +85°C$, 1 mA $\le I_{F(ON)} \le$ 5 mA, 0 V $\le V_{F(OFF)} \le$ 0.6 V, and all Typicals at $T_A = 25°C$ unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Output Withstand Voltage	$\|V_{O(OFF)}\|$	200	245		V	$I_O = 1\ \mu A$		5
Output On-Resistance	$R_{(ON)}$	70	125	160	Ω	$T_A = 25°C$, $I_O = 1$ MA	2, 3, 4	
		40	125	250		$I_O = 1$ MA		
		30	100	200		$I_O = 40$ mA		
Output On-Current Rating	$\|I_{O(ON)}\|$			40	mA	$V_O \le 8$ V, $T_A \le 40°C$		1
Output Off-Resistance	$R_{(OFF)}$	50	10,000		GΩ	$V_O = 200$ V	5	6
Output Off-Leakage Current	$I_{O(OFF)}$		0.02	4.0	nA	$V_O = 200$ V	5	
Output Off-Capacitance	$C_{(OFF)}$			4.5	pF	$V_O = 0$ V, f = 1 MHz	6	
Output Offset Voltage	$V_{O(OS)}$	Note 3	–0.2	Note 3	μV	$I_O = 0$ A; $I_F = 1$ mA	7, 16, 17	3
			–1.3			$I_O = 0$ A; $I_F = 5$ mA		
Input Reverse Breakdown Voltage	V_R	3	10		V	$I_R = 10\ \mu A$		
Input Diode Temperature Coefficient	dV_F/dT		–1.75		mV/°C	$I_F = 1$ mA		
Input Forward Voltage	V_F		1.5	2.0	V	$I_F = 5$ mA	8	
Input Capacitance	C_{IN}		21		pF	$V_F = 0$ V; f = 1 MHz		
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH = 45%, t = 1 min; $T_A = 25°C$		4, 5
Input-Output Capacitance	C_{I-O}		0.6	1.0	pF	$V_{I-O} = 0$ V; f = 1 MHz; $T_A = 25°C$		4
Input-Output Resistance	R_{I-O}	100	100,000		GΩ	$V_{I-O} = 500$ VDC; t = 1 min; RH = 45%		4

Switching Specifications

$-40°C \le T_A \le +85°C$, 1 mA $\le I_{F(ON)} \le$ 5 mA, 0 V $\le V_{F(OFF)} \le$ 0.6 V, and all Typicals at T_A = 25°C unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Notes
Turn On Time	t_{ON}		50	200	µs	I_F = 5 mA	V_O = 50 V	9, 10, 11, 12	
			300	1500		I_F = 1 mA			
Turn Off Time	t_{OFF}		45	250	µs	I_F = 5 mA	V_O = 50 V	9, 10, 11, 12	
			75	350		I_F = 1 mA			
Output Transient Rejection	dV_O/dt		≥7000		V/µs	ΔV_O = 200 V	T_A = 25°C	13	
		2000				ΔV_O = 50 V			
Input-Output Transient Rejection	dV_{I-O}/dt		≥7000		V/µs	ΔV_{I-O} = 300 V	T_A = 25°C	14	
		2000				ΔV_{I-O} = 50 V			

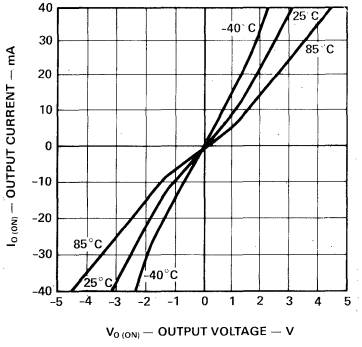


Figure 2. Typical On State I-V Characteristics.

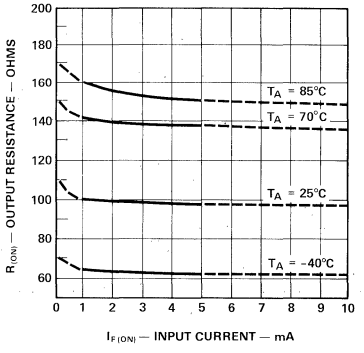


Figure 3. Typical Output Resistance vs. Input Current.

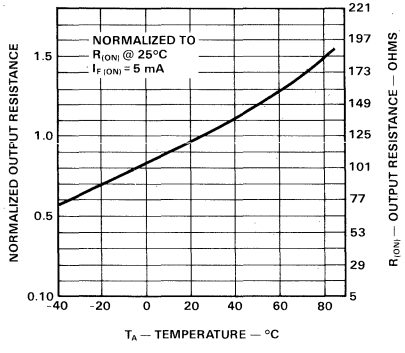


Figure 4. Typical Output Resistance vs. Temperature.

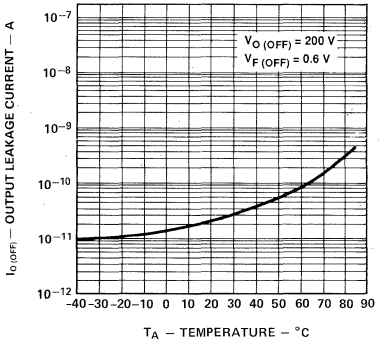


Figure 5. Typical Output Leakage vs. Temperature.

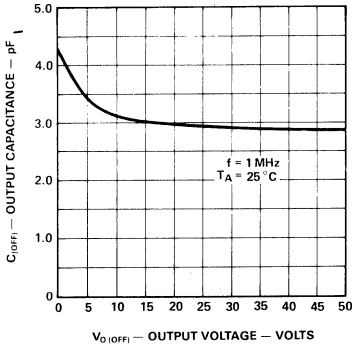


Figure 6. Typical Output Capacitance vs. Output Voltage.

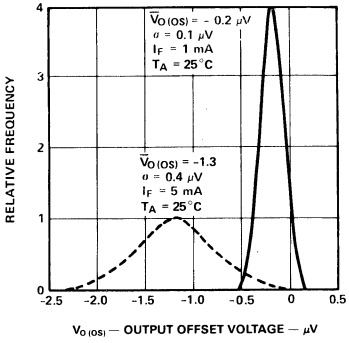


Figure 7. Output Offset Voltage Distribution.

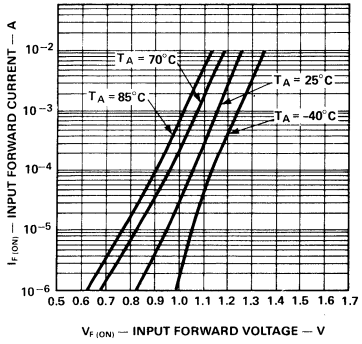


Figure 8. Typical Input Forward Current vs. Forward Voltage.

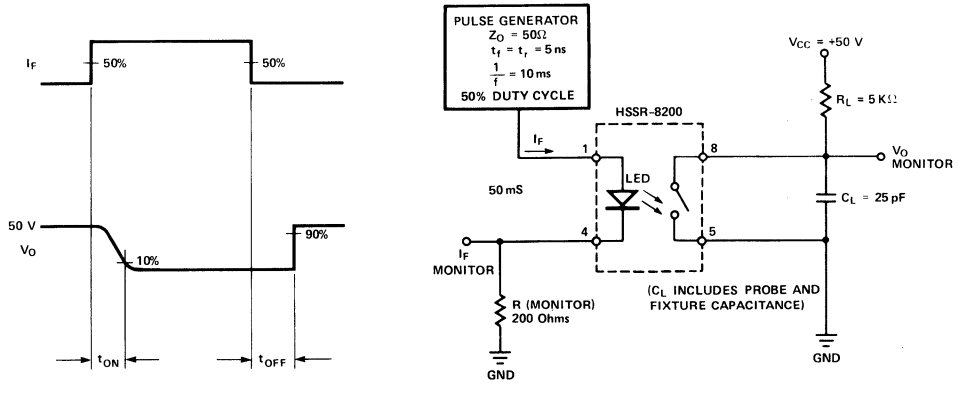


Figure 9. Switching Test Circuit for t_{ON}, t_{OFF}.

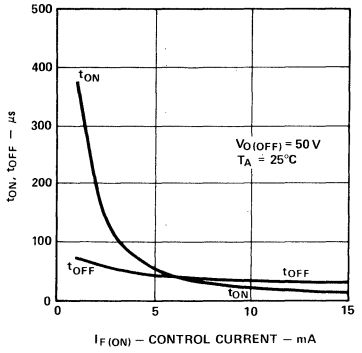


Figure 10. Typical t_{ON} and t_{OFF} vs. Input Current.

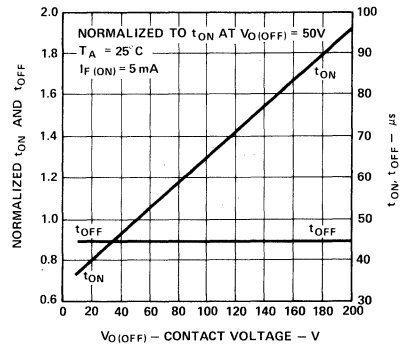


Figure 11. t_{ON} and t_{OFF} vs. Output Voltage.

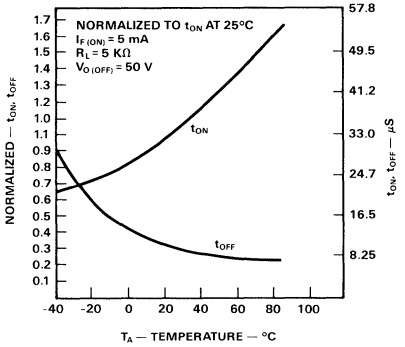


Figure 12. Normalized t_{ON} and t_{OFF} vs. Temperature.

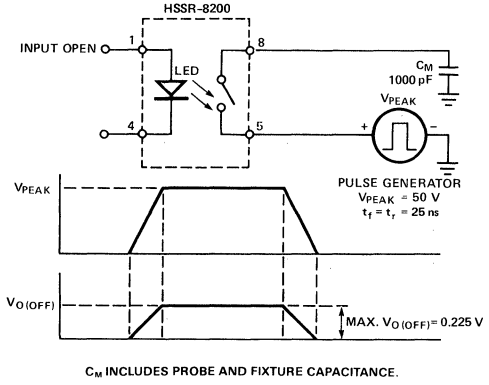


Figure 13. Output Transient Rejection Test Circuit.

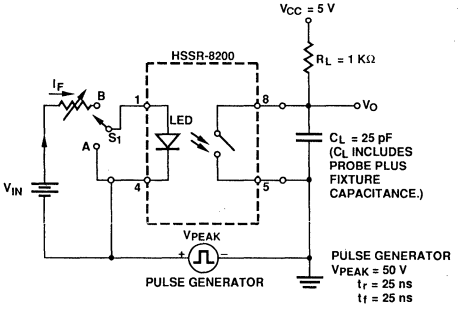
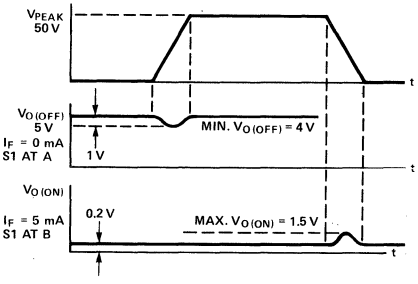


Figure 14. Input-Output Transient Rejection.



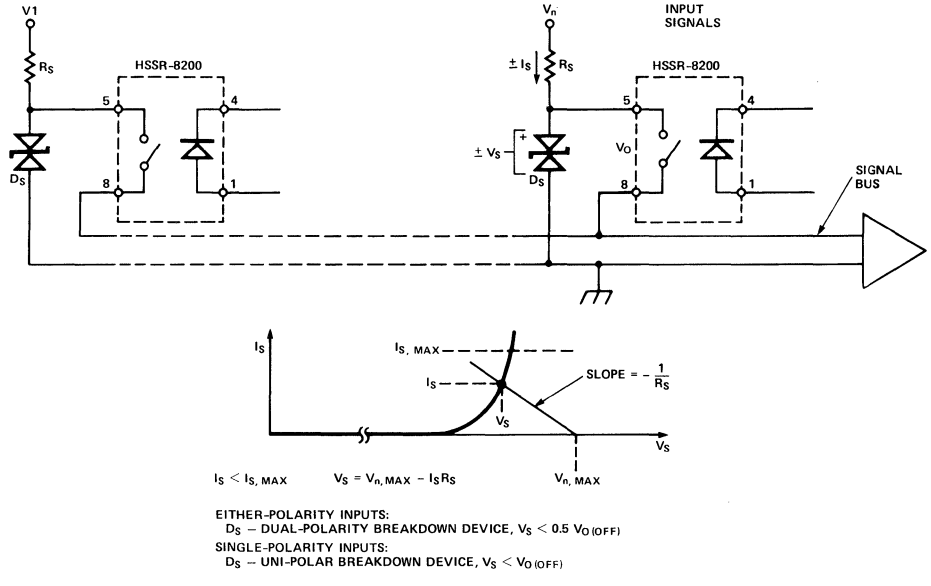


Figure 15. Over-Voltage Protection in Multiplexer Applications.

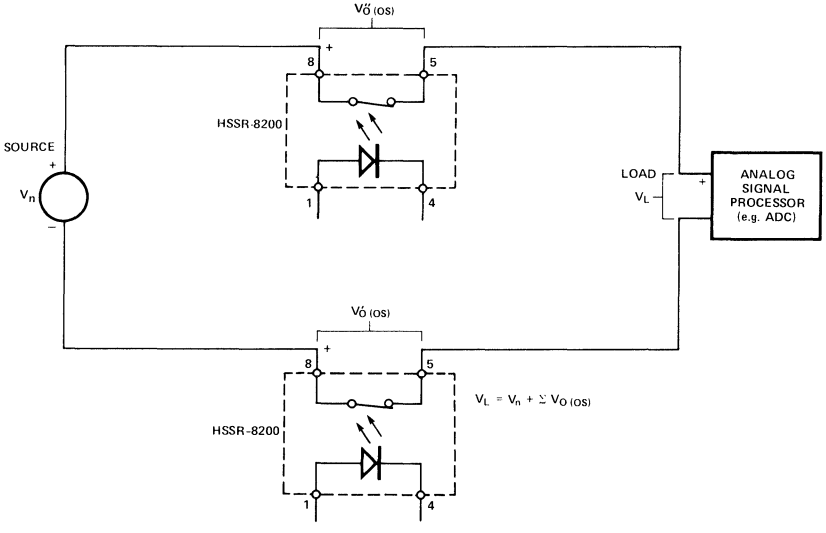


Figure 16. Differential Output Connections to Minimize Offset Voltage Effects.

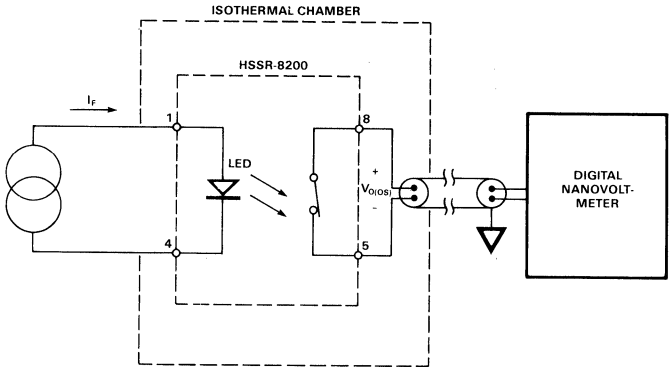


Figure 17. Voltage Offset Test Setup.

Notes:

1. Derate linearly above 40°C at a rate of 0.3 mA/°C.
2. Derate linearly above 60°C at a rate of 5 mW/°C.
3. $V_{O(OS)}$ is a function of $I_{F(ON)}$, and is defined between pins 8 and 5 with pin 5 as reference. $V_{O(OS)}$ must be measured in a stable ambient. See Figure 7 for variation of $V_{O(OS)}$ around the typical value.
4. Device considered a two terminal device: pins 1 and 4 shorted together, and pins 5 and 8 shorted together.
5. This is a proof test. These parts are 100% tested in production at 3000 V_{RMS}, one second.
6. $R_{(OFF)}$ is defined as $V_{O(OFF)}/I_{O(OFF)}$.

HEWLETT PACKARD

new

400 V/10 Ω, General Purpose, 1 Form A, Solid State Relay

Technical Data

HSSR-8400

Features

- **Compact Solid-State Bidirectional Switch**
- **Normally-Off Single-Pole Relay Function (1 Form-A)**
- **400 V Output Withstand Voltage in Both Polarities**
- **150/300 mA Current Ratings (See Schematic for Connection A & B)**
- **Low Input Current; CMOS Compatibility**
- **Very Low On-resistance: 6 Ω Typical @ 25°C**
- **ac/dc Signal & Power Switching**
- **Input-to-Output Insulation Voltage: 2500 Vac, 1 Minute**
- **16-kV ESD Immunity: MIL-STD-883, Method 3015**
- **CSA Approved**
- **UL 508 Approved**

Applications

- **Modems**
- **Telecommunication Switching Equipment**
- **Telecommunication Test Instruments**
- **Reed Relay Replacement**
- **110/220 Vac Load Driver**
- **Industrial Relay Coil Driver**

Description

The HSSR-8400 consists of a high-voltage circuit, optically coupled with a Light-Emitting Diode (LED). This device is a solid-state replacement for single-pole, normally-open (1 Form A) electromechanical relays used for general purpose switching of signals and low-power ac/dc loads. The relay turns on (contact closes) with a minimum input current, I_F, of 5 mA through the input LED. The relay turns off (contact opens) with an input voltage, V_F, of 0.8 V or less. The detector contains a high speed photo-sensitive FET driver circuit and two high voltage MOSFETs.

This relay's logic-level input control and very low typical output on-resistance of 6 Ω makes it suitable for switching of audio frequency signals in telecom applications. Connection A, as shown in the schematic, allows the relay to switch either ac or dc loads. In this configuration, the 150 mA output current rating allows it to switch small loads that are driven from 110 Vac and 220 Vac power lines. Connection B, with the polarity and pin configuration as indicated in the schematic, allows the relay to switch dc loads only. The advantage of Connection B is that the on-resistance is significantly reduced and the output current capability increases by a factor of two.

The electrical and switching characteristics of the HSSR-8400 are specified from -40°C to +85°C.

OPTO COUPLERS

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current (ON)	$I_{F(ON)}$	5	20	mA
Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	Volt
Operating Temperature	T_A	-40	+85	°C
Output Voltage				
Connection A	$V_{O(OFF)}$	-370	370	Volt
Connection B	$V_{O(OFF)}$	0	370	Volt

NOTE: At the time of printing this data sheet, HSSR-8060 (60 V/0.7 Ω) and HSSR-8200 (200 V/160 Ω) solid state relays were also available. For the most current list of solid state relays and options, you may contact your nearest Hewlett-Packard representative.

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature – T_A ..... -40°C to +85°C
Case Temperature – T_C ..... +105°C[1]
Junction Temperature – T_J ..... +125°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Input Current – I_F ..... 20 mA
Repetitive Peak Input Current – I_F ..... 40 mA
(Pulse Width ≤ 1 ms; duty cycle ≤ 50%)
Transient Peak Input Current – I_F ..... 100 mA
(Pulse Width ≤ 200 µs; duty cycle ≤ 1%)
Reverse Input Voltage – V_R ..... 3 V
Input Power Dissipation ..... 40 mW
Output Voltage (T_A = 25°C)
Connection A – V_O ..... -400 to +400 V
Connection B – V_O ..... 0 to +400 V
Average Output Current - Figure 2 (T_A = 25°C, T_C ≤ 70°C)
Connection A – I_O ..... 0.15 A
Connection B – I_O ..... 0.3 A
Single Shot Peak Output Current
(100 ms pulse width, T_A = 25°C, I_F = 10 mA)
Connection A – I_O ..... 1.0 A
Connection B – I_O ..... 2.0 A
Output Power Dissipation ..... 750 mW[2]

Thermal Resistance

Typical Output MOSFET Junction to Case – θ_{JC} = 55°C/W

Demonstrated ESD Performance

Human Body Model: MIL-STD-883 Method 3015.7 – 16 kV
Machine Model: EIAJ IC-121-1988 (1988.3.28 Version 2), Test Method 20, Condition C – 1200 V

CAUTION: Maximum Switching Frequency – Care should be taken during repetitive switching of loads so as not to exceed the maximum output current, maximum output power dissipation, maximum case temperature, and maximum junction temperature.

Electrical Specifications

For -40°C ≤ T_A ≤ +85°C unless otherwise specified. All Typicals at T_A = 25°C.

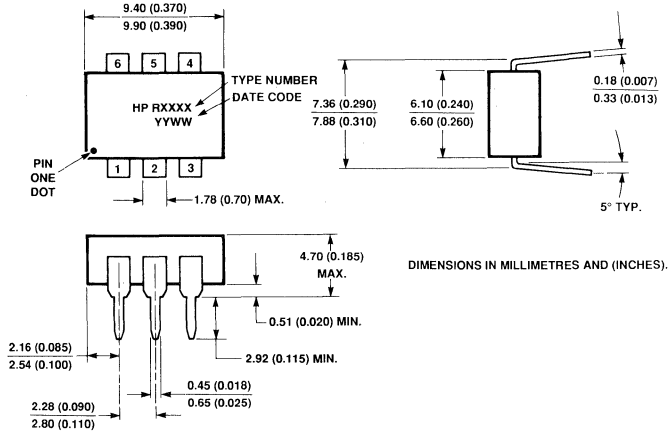
Parameter	Connection	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Output Withstand Voltage	A	$\|V_{O(OFF)}\|$	400			V	V_F = 0.8 V, I_O = 250 µA, T_A = 25°C	4	
			370				V_F = 0.8 V, I_O = 250 µA		
Output On-Resistance	A	$R_{(ON)}$		6	10	Ω	I_F = 10 mA, I_O = 150 mA (pulse duration ≤ 30 ms), T_A = 25°C	5, 6	3
	B			1.5	2.5				
	A				15		I_F = 10 mA, I_O = 150 mA (pulse duration ≤ 30 ms)		
	B				3.8				
Output Leakage Current	A	$I_{O(OFF)}$		$6x10^{-4}$	1.0	µA	V_F = 0.8 V, V_O = 400 V, T_A = 25°C	12	
Output Off-Capacitance	A	$C_{(OFF)}$		60		pF	V_F = 0.8 V, V_O = 25 V, f = 1 MHz	13	
Output Offset Voltage	A	$\|V_{OS}\|$		1		µV	I_F = 5 mA, I_O = 0 mA	17	4
Input Rev. Breakdown Voltage		V_R	3			V	I_R = 100 uA		
Input Diode Temperature Coefficient		$\Delta V_F/\Delta T_A$		–1.3		mV/°C	I_F = 10 mA		
Input Forward Voltage		V_F	1.3	1.6	1.85	V	I_F = 10 mA, T_A = 25°C	14	
Input Capacitance		C_{IN}		72		pF	V_F = 0 V, f = 1 MHz		
Input-Output Insulation Voltage		V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min, T_A = 25°C		5,6
Input-Output Capacitance		C_{I-O}		1.0		pF	V_{I-O} = 0 V, f = 1 MHz		5
Input-Output Resistance		R_{I-O}		100		GΩ	V_{I-O} = 500 Vdc, t = 1 min, RH = 45%		5

Switching Specifications

For -40°C ≤ T_A ≤ + 85°C with Connection A, unless otherwise specified. All Typicals at T_A = 25°C.

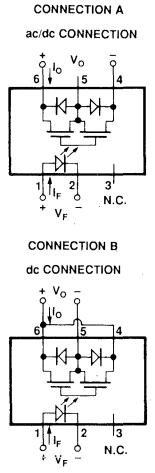
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Turn On Time	t_{ON}		0.5	0.95	ms	I_F = 10 mA, V_{DD} = 400 V, I_O = 150 mA, T_A = 25°C	1, 7, 8, 9	7
				1.2	ms	I_F = 10 mA, V_{DD} = 370 V, I_O = 150 mA		
Turn Off Time	t_{OFF}		0.013	0.1	ms	I_F = 10 mA, V_{DD} = 400 V, I_O = 150 mA, T_A = 25°C	1, 7, 10, 11	
				0.1	ms	I_F = 10 mA, V_{DD} = 370 V, I_O = 150 mA		
Output Transient Rejection	$\|dV_O/dt\|$	1000			V/μs	$V_{(peak)}$ = 100 V, $R_M \geq 1$ MΩ, C_M = 1000 pF, T_A = 25°C	15	
Input-Output Transient Rejection	$\|dV_{I\text{-}O}/dt\|$	2500			V/μs	V_{DD} = 5 V, $V_{I\text{-}O(peak)}$ = 1000 V, R_L = 1 kΩ, C_L = 25 pF, T_A = 25°C	16	

Outline Drawing



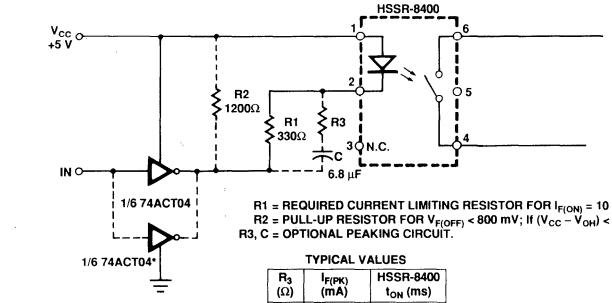
DIMENSIONS IN MILLIMETRES AND (INCHES).

Schematic



Notes:

1. The case temperature, T_C, is measured at the center of the bottom of the package.
2. For derating, see Figure 3. The output power P_O derating curve is obtained when the part is handling the maximum average output current I_O as shown in Figure 2.
3. During the pulsed R_{ON} measurement (I_O duration ≤ 30 ms), ambient (T_A) and case temperature (T_C) are equal.
4. V_{OS} is a function of I_F, and is defined between pins 4 and 6, with pin 4 as the reference. V_{OS} must be measured in a stable ambient (free of temperature gradients).
5. Device considered a two terminal device: pins 1, 2, and 3 shorted together and pins 4, 5, and 6 shorted together.
6. This is a proof test. These parts are 100% tested in production at 3000 Vrms, one second.
7. For a faster turn-on time, the optional peaking circuit shown in Figure 1 may be implemented.



R1 = REQUIRED CURRENT LIMITING RESISTOR FOR $I_{F(ON)}$ = 10 mA.
R2 = PULL-UP RESISTOR FOR $V_{F(OFF)}$ < 800 mV; If (V_{CC} – V_{OH}) < 800 mV, OMIT R2.
R3, C = OPTIONAL PEAKING CIRCUIT.

TYPICAL VALUES

R_3 (Ω)	$I_{F(PK)}$ (mA)	HSSR-8400 t_{ON} (ms)
–	10 (no pk)	0.50
330	20	0.29
100	40	0.17
33	100	0.09

*USE SECOND GATE IF $I_{F(PK)}$ > 50 mA.

Figure 1. Recommended Input Circuit.

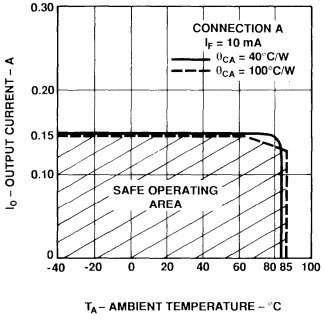


Figure 2A. Maximum Average Output Current Rating vs. Ambient Temperature.

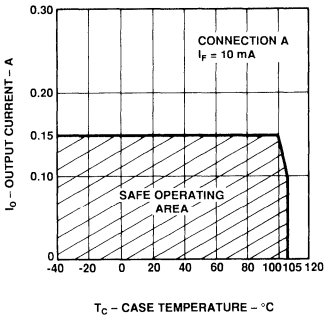


Figure 2B. Maximum Average Output Current Rating vs. Case Temperature.

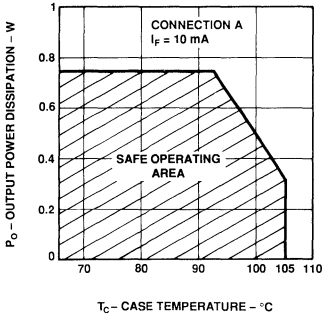


Figure 3. Output Power Derating vs. Case Temperature.

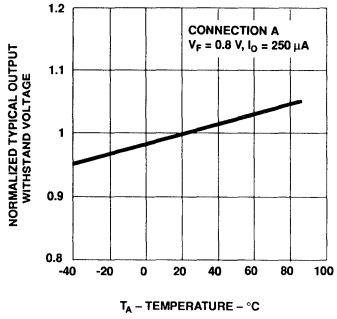


Figure 4. Normalized Typical Output Withstand Voltage vs. Temperature.

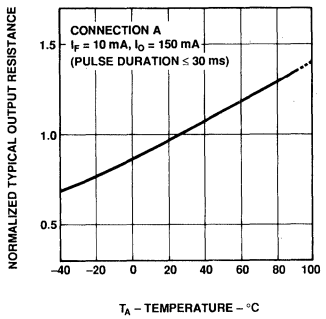


Figure 5. Normalized Typical Output Resistance vs. Temperature.

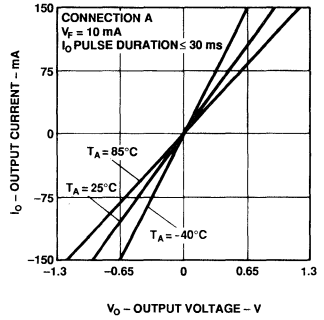


Figure 6. Typical On State Output I-V Characteristics.

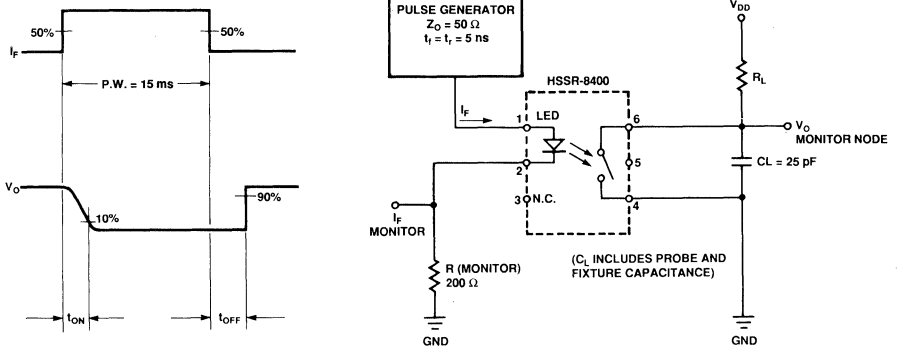


Figure 7. Switching Test Circuit for t_{ON}, t_{OFF}.

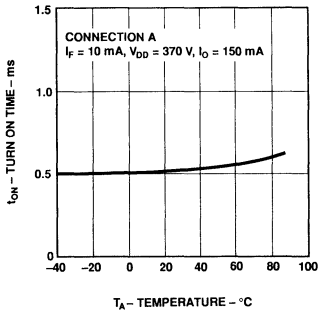


Figure 8. Typical Turn On Time vs. Temperature.

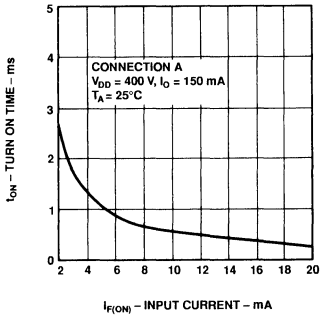


Figure 9. Typical Turn On Time vs. Input Current.

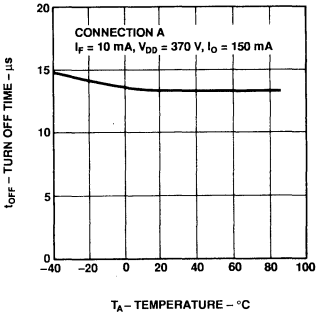


Figure 10. Typical Turn Off Time vs. Temperature.

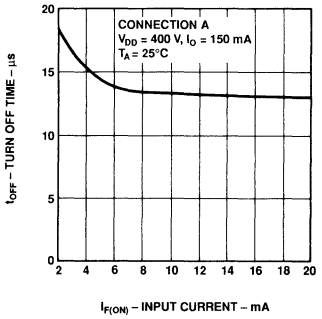


Figure 11. Typical Turn Off Time vs. Input Current.

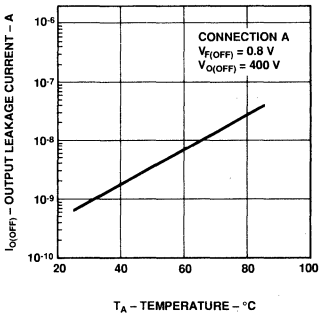


Figure 12. Typical Output Leakage vs. Temperature.

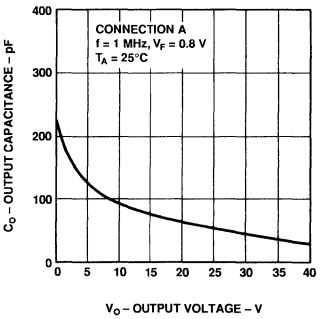


Figure 13. Typical Output Capacitance vs. Output Voltage.

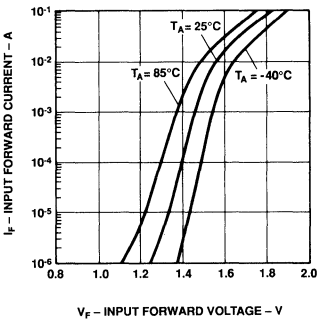


Figure 14. Typical Input Forward Current vs. Input Forward Voltage.

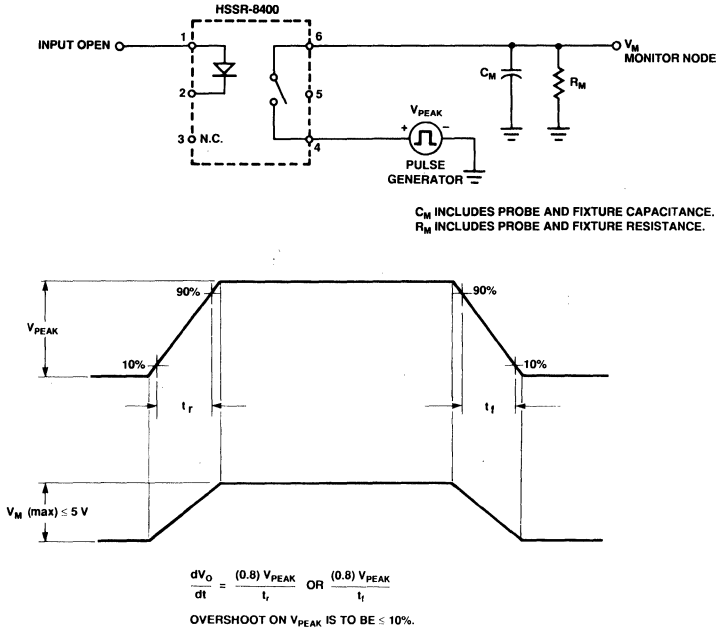


Figure 15. Output Transient Rejection Test Circuit.

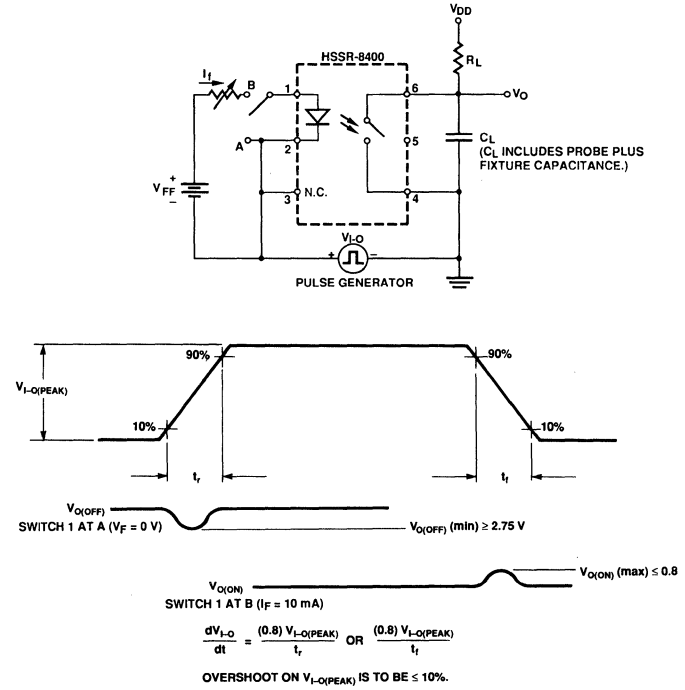


Figure 16. Input-Output Transient Rejection Test Circuit.

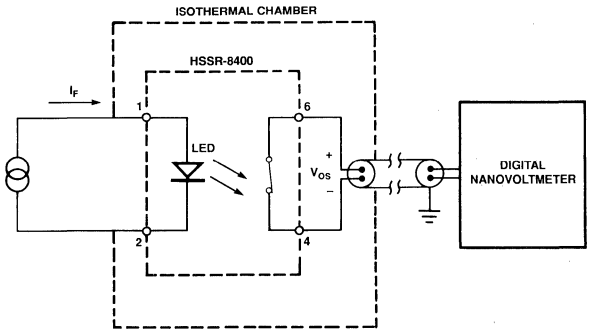


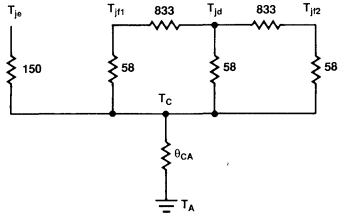
Figure 17. Voltage Offset Test Setup.

Applications Information

Thermal Model

The steady state thermal model for the HSSR-8400 is shown in Figure 18. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. The thermal resistances between the LED and other internal nodes are very large in comparison with the other terms and are omitted for simplicity. The components do, however, interact indirectly through θ_{CA}, the case-to-ambient thermal resistance. All heat generated flows through θ_{CA}, which raises the case temperature T_C accordingly. The value of θ_{CA} depends on the conditions of the board design and is, therefore, determined by the designer.

The typical value for each output MOSFET junction-to-case thermal resistance is specified as 55°C/W. This is the thermal resistance from one MOSFET junction to the case when power is dissipated equally in the MOSFETs. The power dissipation in the FET Driver is negligible in comparison to the MOSFETs.



T_{je} = LED JUNCTION TEMPERATURE
T_{jf1} = FET 1 JUNCTION TEMPERATURE
T_{jf2} = FET 2 JUNCTION TEMPERATURE
T_{jd} = FET DRIVER JUNCTION TEMPERATURE
T_C = CASE TEMPERATURE (MEASURED AT CENTER OF PACKAGE BOTTOM)
T_A = AMBIENT TEMPERATURE (MEASURED 6" AWAY FROM THE PACKAGE)
θ_{CA} = CASE-TO-AMBIENT THERMAL RESISTANCE

ALL THERMAL RESISTANCE VALUES ARE IN °C/W.

Figure 18. Thermal Model.

On-Resistance and Derating Curves

The output on-resistance, R_{ON}, specified in this data sheet, is the resistance measured across the output contact when a pulsed current signal (I_O = 150 mA) is applied to the output pins. The use of a pulsed signal (≤ 30 ms) implies that each junction temperature is equal to the ambient and case temperatures. The steady-state resistance, R_{SS}, on the other hand, is the value of the resistance measured across the output contact when a DC current signal is applied to the output pins for a duration sufficient to reach thermal equilibrium. R_{SS} includes the effects of the temperature rise of each element in the thermal model.

Derating curves are shown in Figures 2 and 3. Figure 2 specifies the maximum average output current allowable for a given ambient or case temperature. Figure 3 specifies the output power dissipation allowable for a given case temperature. Above a case temperature of 93°C, the maximum allowable output current and power dissipation are related by the expression $R_{SS} = P_O(max)/(I_O(max))^2$ from which R_{SS} can be calculated. Staying within the safe area assures that the steady state junction temperatures remain less than 125°C. As an example, for a case temperature of 100°C, Figure 3 shows that the output power dissipation should be limited to less than 0.5 watts. A check with Figure 2B shows that the output current should be limited to less than 150 mA. This yields an R_{SS} of 22 Ω.

Turn On Time Variation

For applications which are sensitive to turn on time, the designer should refer to Figures 19 and 20. These figures show that although there is very little variation in t_{ON} within most of the population, a portion of the distribution will vary with use. The optional peaking circuit shown in Figure 1 can be used to reduce the total turn on time and, consequently, any associated variation.

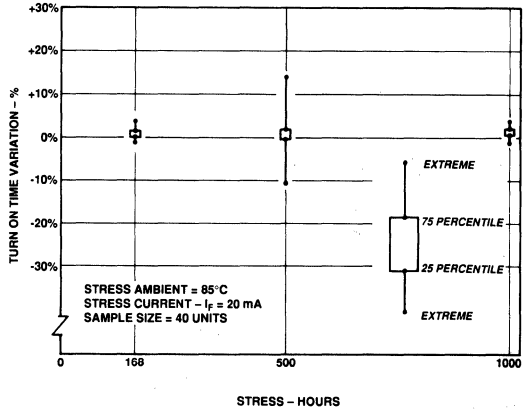


Figure 19. Turn On Time Variation with High Temperature Operating Life.

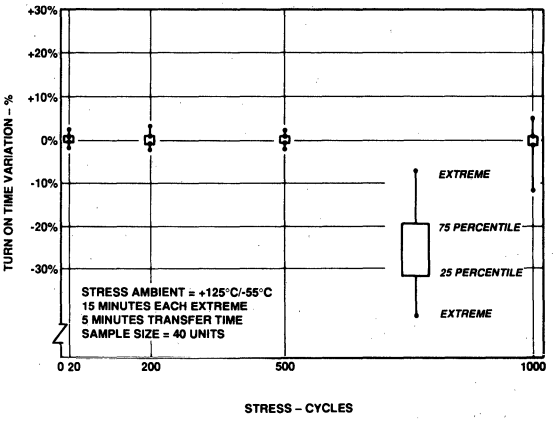


Figure 20. Turn On Time Variation with Temperature Cycling.

HEWLETT PACKARD

Hermetic Optocouplers

HEWLETT PACKARD

Hermetic and Hirel Optocouplers

For Military, Space Flight, & Life Critical Applications

Choose from Hewlett-Packard's broad line of high performance hermetic optocouplers to meet your military, aerospace, and high reliability applications. There are three ceramic package styles to choose from: 8 and 16 pin dual in-line packages, and a 20 terminal leadless chip carrier (LCC) package. Available in each package style are four basic families of optocouplers: high gain, high speed transistor, high speed logic gate, and several application specific devices. Most functional device types are offered in all three package configurations. The LCC catalog products are all two channel optocouplers.

HP's Class H hermetic optocouplers are classified by the Department of Defense as hybrid microcircuits and are manufactured and tested on a MIL-STD-1772 certified and qualified line. Our facilities and assembly processes meet MIL-H-38534 Class H, and we have listing on QML38534.

All product families are represented by standard (commercial grade) units and by high reliability tested units. The hi-rel parts are tested to MIL-STD-883 Class B. All hi-rel tested parts are also offered with recognized DESC part numbers either from DESC Drawings, Standard Military Drawings (SMDs), or from DESC's new, "One Part, One Part Numbering System." All hi-rel parts are tested and guaranteed over the full military temperature range from -55°C to +125°C.

New this year is the availability of devices with construction, screening and qualification normally required for devices used in space flight applications.

To give you more opportunities to use recognized DESC parts, we now offer 20 devices under DESC drawings.

Hermetic Optocoupler Product Screening and Quality Conformance Test Program (MIL-STD-883 Class B)

The following 100% Screening and Quality Conformance Inspection programs show in detail the capabilities of our hermetic optocouplers. MIL-H-38534 Quality assurance requirements are in accordance with Option 2 for all testing programs (Methods 5008 and 2017). Hewlett-Packard further exercises a testing option as allowed by MIL-STD-883, Method 5008, Par. 3.1a which states that "Hybrid and multichip microcircuits, which are contained in packages having an inner seal perimeter of less than 2.0 inches", may be tested in accordance with the requirements of MIL-STD-883, Methods 5004 and 5005, with a change to the internal visual from Method 2010 to Method 2017. All devices marked /883B and DESC Drawing parts have standardized test programs suitable for product used in military, aerospace, and other high reliability applications and are the preferred devices by systems contractors.

100% Screening MIL-STD-883, Method 5004 (Class H Devices)

Test	Method	Conditions
1. Precap Internal Visual	2017 & 2032	
2. Temperature Cycling	1010	Condition C, -65°C to +150°C, 10 cycles
3. Constant Acceleration	2001	Condition A, 5KG's
4. Fine Leak	1014	Condition A
5. Gross Leak	1014	Condition C
6. Interim Electrical Test	–	Optional
7. Burn-In	1015	Condition B, Time = 160 hours, min. T_A = 125°C
8. Final Electrical Test		Group A, Subgroup 1, 5% PDA
Electrical Test		Group A, Subgroups 2, 3, 9
9. External Visual	2009	

Quality Conformance Inspection

Group A electrical tests are product dependent and are given in the individual device data sheets. Group A and B testing is performed on each inspection lot

Group A Testing, MIL-STD-883, Method 5005 (Class H Devices) Quality/Acceptance Number = 116/0

Subgroup 1 Static tests at T_A = 25°C
Subgroup 2 Static tests at T_A = +125°C
Subgroup 3 Static tests at T_A = -55°C
Subgroup 4 Dynamic test at T_A = 25°C (where applicable)
Subgroups 5, 6, 7, and 8a & 8b These subgroups are non-applicable to this device type
Subgroup 9 Switching tests at T_A = 25°C
Subgroup 10 Switching tests at T_A = +125°C
Subgroup 11 Switching tests at T_A = -55°C

Group B Testing, MIL-STD-883, Method 5005 (Class H Devices)

Test	Method	Conditions	Quantity/ Accept No.
Subgroup 2 Resistance to Solvents	2015		4 Devices (no failures)
Subgroup 3 Solderability	2003	Soldering temperature of 245 ± 5 °C for 10 seconds	22/0 leads 3 devices minimum
Subgroup 5 Bond Strength Thermocompression (performed prior to seal)	2011	Test Condition D	15/0 wires

Group C testing is performed on a periodic basis from current manufacturing every three months.

Group C Testing, MIL-STD-883, Method 5005 (Class H Devices)

Test	Method	Conditions	Quantity/ Accept No.
Subgroup 1 Steady State Life Test	1005	Condition B, time = 1000 hours total T_A = +125°C	45/0
Endpoint Electricals at 1000 hours		Group A, Subgroup 1, 2, 3	

Group D testing is performed on a periodic basis from current manufacturing every six months.

Group D Testing, MIL-STD-883, Method 5005 (Class H Devices)

Test	Method	Conditions	Quantity/ Accept No.
Subgroup 1 Physical Dimensions	2016		15/0
Subgroup 2 Lead Integrity	2004	Test Cond. B2 (Test Cond. D for LCCs LTPD 15) (15/0)	45/0 leads 3 devices minimum

Group D Testing, MIL-STD-883, Method 5005 (Class H Devices) (cont.)

Test	Method	Conditions	Quantity/ Accept No.
Subgroup 3			15/0
Thermal Shock	1011	Condition B, -55°C to +125°C 15 cycles min.	
Temperature Cycling	1010	Condition C, -65°C to +150°C 100 cycles min.	
Moisture Resistance	1004		
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination		Per visual criteria of methods 1004, 1010	
Endpoint Electricals		Group A, Subgroup 1, 2, 3	
Subgroup 4			15/0
Mechanical Shock	2002	Condition B, 1500 G, t = 0.5 ms, 5 blows in each orientation	
Vibration Variable Frequency	2007	Condition A	
Constant Acceleration	2001	Condition A, 5 KGs	
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1010	Per visual criteria of Method 1010	
Endpoint Electricals		Group A, Subgroup 1, 2, 3	
Subgroup 5			15/0
Salt Atmosphere	1009	Condition A min.	
Visual Examination	1009	Per visual criteria of Method 1009	
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Subgroup 6			3/0 or 5/1
Internal Water Vapor Content	1018	5,000 ppm maximum water content at 100°C	
Subgroup 7			15/0 leads
Adhesion of Lead Finish (not required for LCCs)	2025		3 devices minimum

Class K Level Screening per MIL-H-38534

100% Screen	Method	Conditions
Nondestructive Bond Pull	2023	
Internal Visual	2017	
Temperature Cycling	1010	Cond. C, -65°C to +150°C, 10 cycles
Constant Acceleration	2001	Cond. A, 5 Kg's, Y1 & Y2 orientations
Visual Inspection	–	Visual for catastrophic failures
Particle Impact Noise Detection (PIND)	2020	Condition A
Serialization	–	
Pre Burn-in Electrical Test	–	Group A, Subgroup 1, (except Ii-o)
Burn-in Test	1015	Cond. B, time = 160 hrs. (total of 320 hrs.; 2 increments of 160 hrs.) T_A = +125°C
Interim Electrical Test (160 hrs.)	–	Group A, Subgroup 1, (except Ii-o)
Burn-in Test	1015	Cond. B, time = 160 hrs., T_A = +125°C
Post Burn-in Electrical Test	–	Group A, Subgroup 1, 2% PDA applies
Final Electrical Test	–	Group A, Subgroup 2, DC at T_A = +125°C Group A, Subgroup 3, DC at T_A = -55°C Group A, Subgroup 9, AC at T_A = +25°C
Fine Leak	1014	Cond. A1
Gross Leak	1014	Cond. C1
Radiographics	2012	
External Visual	2009	

Class K Level Group A Testing per MIL-H-38534

	Quantity (Accept Number)
Subgroup 1 Static tests at T_A = 25°C	116 (0)
Subgroup 2 Static tests at T_A = +125°C	76 (0)
Subgroup 3 Static tests at T_A = -55°C	45 (0)
Subgroup 4 Dynamic test at T_A = 25°C (where applicable)	116 (0)
Subgroup 9 Switching tests at T_A = 25°C	116 (0)
Subgroup 10 Switching tests at T_A = +125°C	76 (0)
Subgroup 11 Switching tests at T_A = -55°C	45 (0)

Class K Level Group B Testing per MIL-H-38534

Test	Method	Conditions	Quantity/Accept No.
Subgroup 1 Physical Dimensions	2016		2 (0)
Subgroup 2 Particle Impact Noise Detection (PIND)	2020	Condition A	15 (0)
Subgroup 3 Resistance to Solvents	2015		4 (0)
Subgroup 4 Internal Visual and Mechanical	2014	Performed at precap Obtained by interception	1 (0)
Subgroup 5 Bond Strength (Thermo Compression)	2011	Test condition D (Performed in-process)	2 devices (44 [0] bonds or all if less)
Subgroup 6 Die Shear Strength	2019	Per Method 2019 for the applicable die size	2 (0)
Subgroup 7 Solderability	2003	Soldering Temperature at +245 ± 5°C	2 (0) (15 [0] leads or all if less)

Class K Level Group C Testing per MIL-H-38534

Test	Method	Conditions	Quantity/Accept No.
Subgroup 1 End Point Electricals		Group A, Subgroup 1 Group A, Subgroup 2 Group A, Subgroup 3	5 (0)
External Visual	2009		
Temperature Cycling	1010	Cond. C, -65°C to +150°C, 20 cycles	
Constant Acceleration	2001	Cond. A, 5 Kg's, Y1 & Y2 orientations	
Fine Leak	1014	Cond. A1	
Gross Leak	1014	Cond. C1 or C3	
Radiographic Inspection	2012	Y axis	
Visual Examination		Per visual criteria of Method 1010	
End Point Electricals		Group A, Subgroup 1 Group A, Subgroup 2 Group A, Subgroup 3	
Subgroup 2 End Point Electricals		Group A, Subgroup 1 Group A, Subgroup 2 Group A, Subgroup 3	22 (0) or 5 (0)*
Steady State Life Test	1005	Test Cond. B, T_A = +125°C, time = 1000 hrs.	
End Point Electricals		Group A, Subgroup 1 Group A, Subgroup 2 Group A, Subgroup 3	
Subgroup 3 Internal Water-Vapor Content	1018	5000 ppm maximum water content at +100°C	3 (0)

*Maximum order quantity of 500 pieces.

Class K Level Group D Testing per MIL-H-38534

Test	Method	Conditions	Quantity/Accept No.
Thermal Shock	1011	Condition C, -65°C to +150°C, 15 cycles	5 (0)
Stabilization Bake	1008	+150°C, time = 1 hr.	5 (0)
Lead Integrity	2004	Test Condition B2 (lead fatigue)	1 (0) 15 leads min. or all if less
Fine Leak	1014	Test Condition A1	5 (0)
Gross Leak	1014	Test Condition C1	5 (0)

Controlling Government Specifications and Standards

MIL-H-38534 General Specification for Hybrid Microcircuits

All Hewlett-Packard /883B, DESC Drawing and SMD products are in full compliance with the applicable parts of MIL-H-38534, Class H.

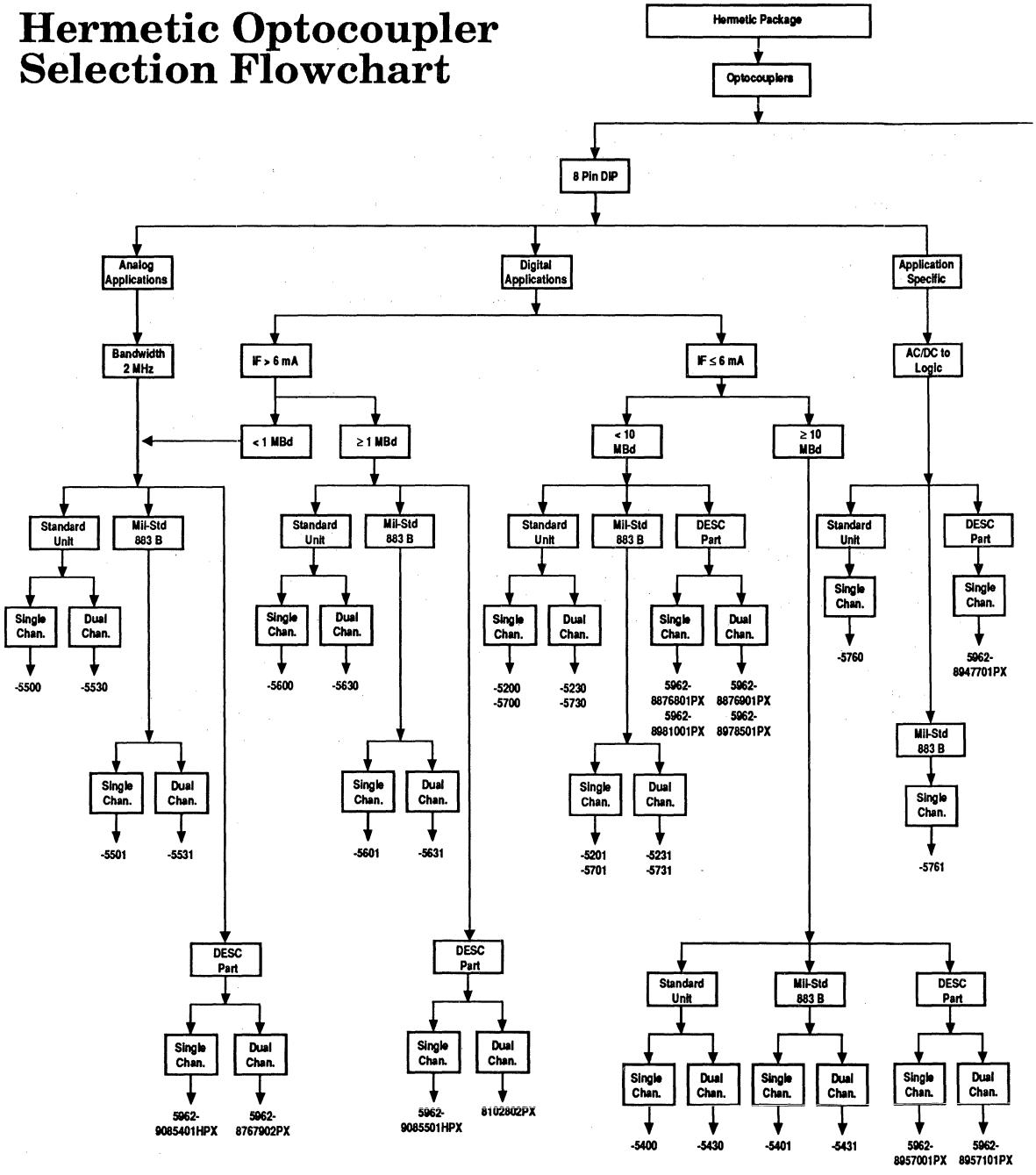
MIL-STD-883 Test Methods and Procedures for Microelectronics

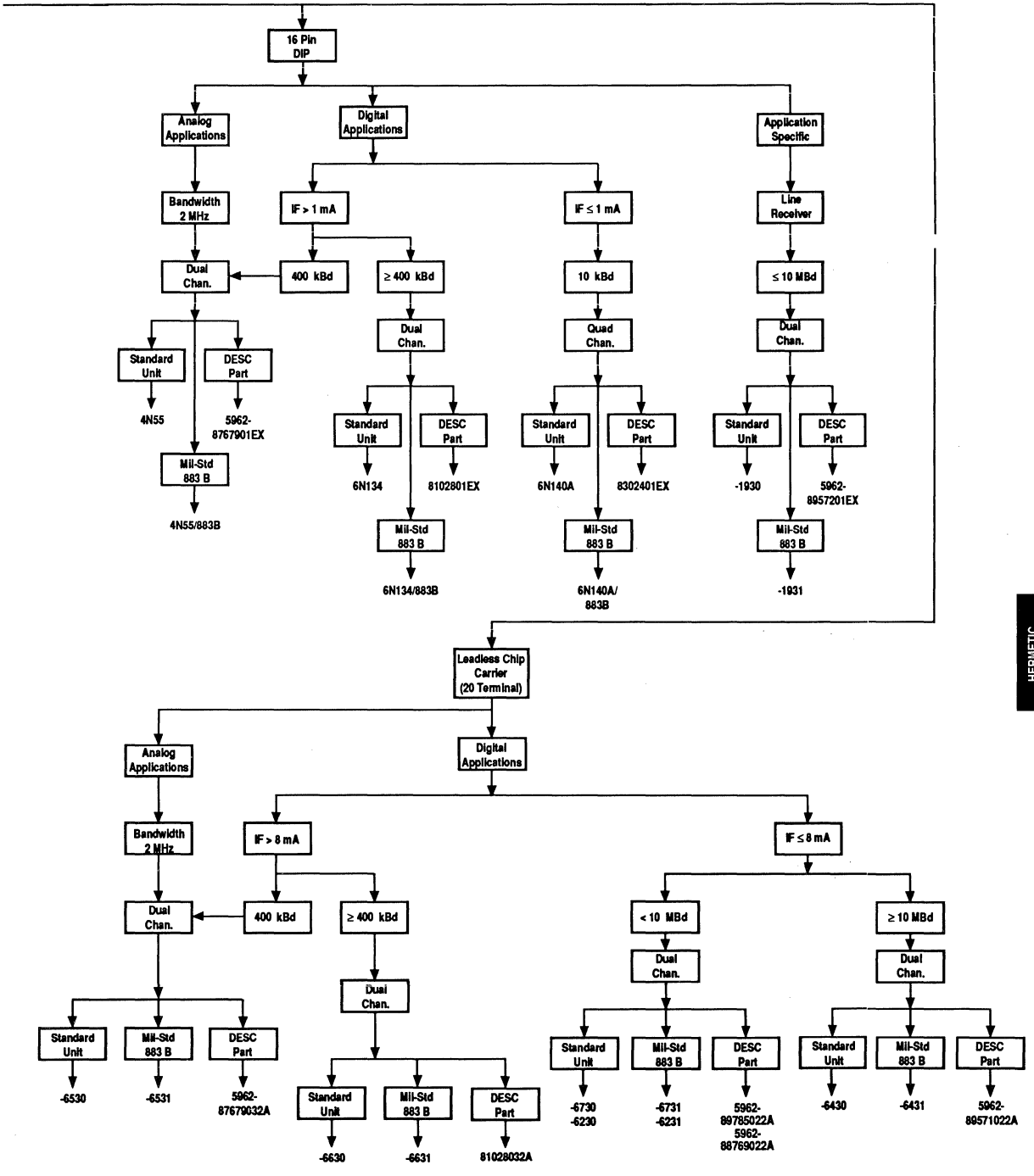
Hewlett-Packard's testing of all hermetic hybrid products is in compliance with current revisions, requirements and test methods of MIL-STD-883 Class H.

MIL-STD-1772 Certification Requirements for Hybrid Microcircuit Facilities and Lines

Our Class H hermetic optocoupler line is certified and parts are qualified to MIL-STD-1772. Certification to MIL-STD-1772 must exist before a part can be marked with 883B or with a DESC SMD number.

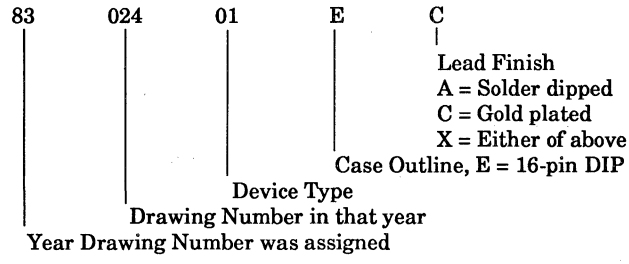
Hermetic Optocoupler Selection Flowchart



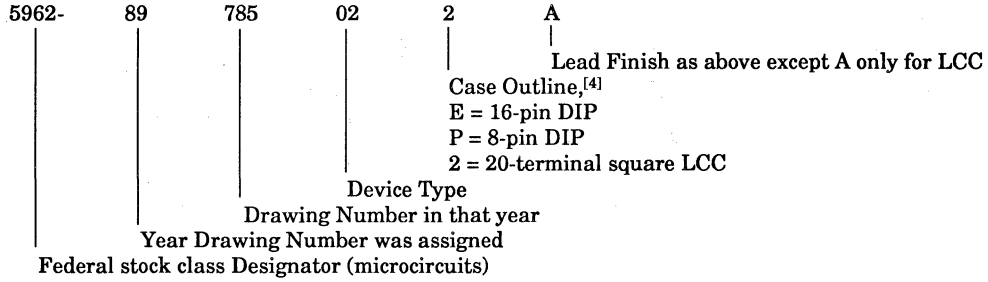

16 Pin DIP
Analog Applications
Digital Applications
Application Specific
Bandwidth 2 MHz
IF > 1 mA
IF ≤ 1 mA
Line Receiver
Dual Chan.
400 kBd
≥ 400 kBd
10 kBd
≤ 10 MBd
Dual Chan.
Quad Chan.
Dual Chan.
Standard Unit
DESC Part
4N55
5962-8767901EX
Mil-Std 883 B
4N55/883B
Standard Unit
DESC Part
6N134
8102801EX
Mil-Std 883 B
6N134/883B
Standard Unit
DESC Part
6N140A
8302401EX
Mil-Std 883 B
6N140A/883B
Standard Unit
DESC Part
-1930
5962-8957201EX
Mil-Std 883 B
-1931
Leadless Chip Carrier (20 Terminal)
Analog Applications
Digital Applications
Bandwidth 2 MHz
IF > 8 mA
IF ≤ 8 mA
Dual Chan.
400 kBd
≥ 400 kBd
< 10 MBd
≥ 10 MBd
Dual Chan.
Dual Chan.
Dual Chan.
Standard Unit
Mil-Std 883 B
DESC Part
-6530
-6531
5962-87679032A
Standard Unit
Mil-Std 883 B
DESC Part
-6630
-6631
81028032A
Standard Unit
Mil-Std 883 B
DESC Part
-6730
-6230
-6731
-6231
5962-89785022A
5962-88769022A
Standard Unit
Mil-Std 883 B
DESC Part
-6430
-6431
5962-89571022A

DESC Part Number Systems[1]

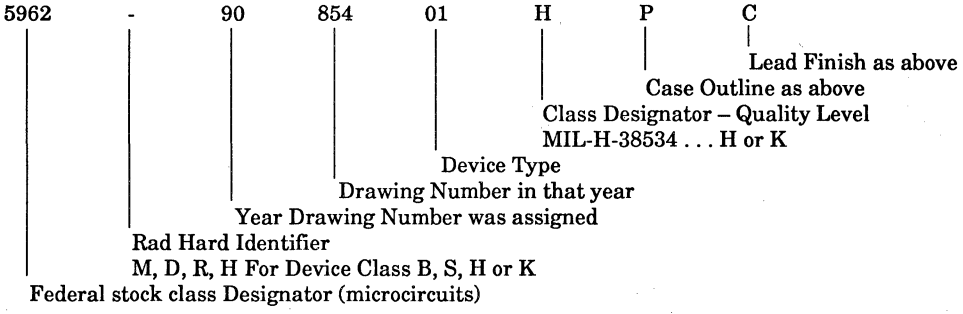
DESC Drawings[2]



Standard Military Drawings (SMD)



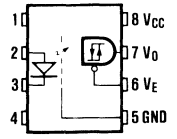
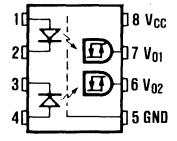
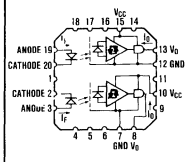
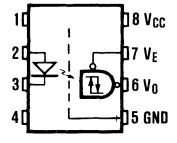
One Part – One Part Number System[3]



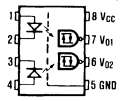
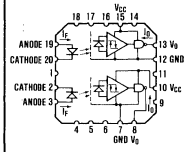
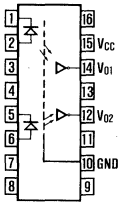
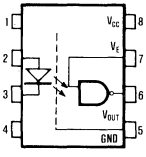
Notes:

1. The numbering system used was current when any particular part was numbered.
2. DESC Drawings do not contain the prefix 5962.
3. Class Designators H, and K of MIL-H-38534 are equivalent to class levels B and S of MIL-M-38510 respectively.
4. For additional lead form options, contact your local Hewlett-Packard field representative.

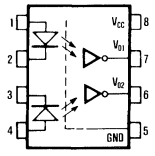
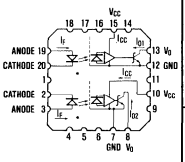
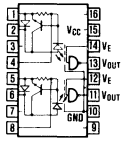
High-Speed Logic Gate Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Common Mode	Specified Input Current	Withstand Test Voltage	Page No.
 8 pin DIP	HCPL-5200	Single Channel, Hermetically Sealed Wide Supply Voltage Optocoupler	High Speed Logic Ground Isolation, LSTTL, TTL, CMOS Logic Interface	5 M bit/s	1000 V/µs at Vcm = 50 V	2-8 mA	1500 Vdc	6-313
	HCPL-5201	MIL-STD-883 Class B	Military/High Reliability					
	5962-8876801PX	DESC Approved HCPL-5201						
 8 pin DIP	HCPL-5230	Dual Channel, Hermetically Sealed Wide Supply Voltage Optocoupler	High Speed Logic Ground Isolation, LSTTL, TTL, CMOS Logic Interface					
	HCPL-5231	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-8876901PX	DESC Approved HCPL-5231						
 20 Terminal LCC	HCPL-6230	Dual Channel, Hermetically Sealed Wide Supply Voltage Optocoupler	High Speed Logic Ground Isolation, LSTTL, TTL, CMOS Logic Interface					
	HCPL-6231	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-88769022A	DESC Approved HCPL-6231						
 8 pin DIP	HCPL-5400	Single Channel, Hermetically Sealed High Speed Optocoupler	High Speed Logic Isolation, A/D and Parallel/Serial Conversion	40 M bit/s	500 V/µs at Vcm = 50 V	6-10 mA	1500 Vdc	6-328
	HCPL-5401	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-8957001PX	DESC Approved HCPL-5401						

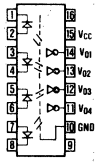
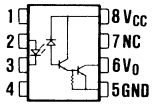
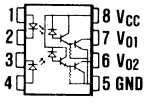
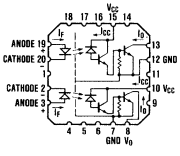
High-Speed Logic Gate Optocouplers (Continued)

Device		Description	Application	Typical Data Rate [NRZ]	Common Mode	Specified Input Current	Withstand Test Voltage	Page No.
 8 pin DIP	HCPL-5430	Dual Channel, Hermetically Sealed High Speed Optocoupler	High Speed Logic Isolation, Communications, Networks, Computers	40 Mbit/s	500 V/µs at Vcm = 50 V	6-10 mA	1500 Vdc	6-328
	HCPL-5431	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-8957101PX	DESC Approved HCPL-5431						
 20 Terminal LCC	HCPL-6430	Dual Channel, Hermetically Sealed High Speed Optocoupler	High Speed Logic Isolation, Communications, Networks, Computers					
	HCPL-6431	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-89571022A	DESC Approved HCPL-6431						
 16 pin DIP	6N134	Dual Channel, Hermetically Sealed Optically Coupled Logic Gate	Line Receiver, Ground Isolation for High Reliability Systems	10 M bit/s	1000 V/µs at Vcm = 50 V	10 mA	1500 Vdc	6-344
	6N134/883B	MIL-STD-883 Class B Part	Military/High Reliability					
	8102801EX	DESC Approved 6N134/883B						
 8 pin DIP	HCPL-5600	Single Channel, Hermetically Sealed Optically Coupled Logic Gate	Line Receiver, Ground Isolation for High Reliability Systems					6-351
	HCPL-5601	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-9085501HPX	DESC Approved HCPL-5601						

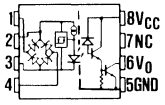
High-Speed Logic Gate Optocouplers (Continued)

Device		Description	Application	Typical Data Rate [NRZ]	Common Mode	Specified Input Current	Withstand Test Voltage	Page No.
 8 pin DIP	HCPL-5630	Dual Channel, Hermetically Sealed Optically Coupled Logic Gate	Line Receiver, Ground Isolation for High Reliability Systems	10 M bit/s	1000 V/μs at Vcm = 50 V	10 mA	1500 Vdc	6-351
	HCPL-5631	MIL-STD-883 Class B Part	Military/High Reliability					
	8102802PX	DESC Approved HCPL-5631						
 20 Terminal LCC	HCPL-6630	Dual Channel, Hermetically Sealed Optically Coupled Logic Gate	Line Receiver, Ground Isolation for High Reliability Systems					
	HCPL-6631	MIL-STD-883 Class B Part	Military/High Reliability					
	81028032A	DESC Approved HCPL-6631						
 16 pin DIP	HCPL-1930	Dual Channel, Hermetically Sealed High CMR Line Receiver Optocoupler	Line Receiver, High Speed Logic Ground Isolation in High Ground or Induced Noise Environments	10M bit/s	1000 V/μs at Vcm = 50 V	10 mA	1500 Vdc	6-360
	HCPL-1931	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-8957201EX	DESC Approved HCPL-1931						

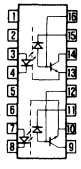
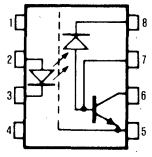
High Gain Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
 16 pin DIP	6N140A	Hermetically Sealed Package Containing 4 Low Input Current High Gain Optocouplers	Line Receiver, Low Power Ground Isolation for High Reliability Systems	100k bit/s	300% Min.	0.5 mA to 5.0 mA	1500 Vdc	6-369
	6N140A/883B	MIL-STD-883 Class B Part	Military/High Reliability					
	8302401EX	DESC Approved 6N140A/883B						
 8 pin DIP	HCPL-5700	Single Channel, Hermetically Sealed High Gain Optocoupler	Line Receiver, Low Current Ground Isolation. TTL/TTL, LSTTL/TTL, CMOS/TTL					6-377
	HCPL-5701	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-8981001PX	DESC Approved HCPL-5701						
 8 pin DIP	HCPL-5730	Dual Channel, Hermetically Sealed, High Gain Optocoupler	Line Receiver, Polarity Sensing, Low Current Ground Isolation					
	HCPL-5731	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-8978501PX	DESC Approved HCPL-5731						
 20 Terminal LCC	HCPL-6730	Dual Channel, Hermetically Sealed High Gain Optocoupler	Line Receiver, Polarity Sensing, Low Current Ground Isolation					
	HCPL-6731	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-89785022A	DESC Approved HCPL-6731						

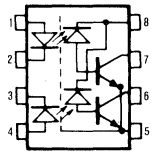
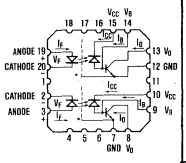
AC/DC to Logic Interface Optocoupler

Device		Description	Application	Typical Data Rate	Input Threshold Current	Output Current	Withstand Test Voltage	Page No.
	HCPL-5760	Single Channel Hermetically Sealed Threshold Sensing Optocoupler	Limit Switch Sensing, Low Voltage Detector Relay Contact Monitor	10 kHz	2.5 mA TH+ 1.3 mA TH–	2.6 mA	1500 Vdc	6-388
	HCPL-5761	MIL-STD-883 Class B Part	Military/High Reliability					
8 pin DIP	5962-8947701PX	DESC Approved HCPL-5761						

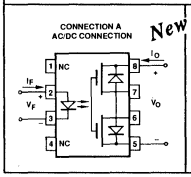
High Speed Transistor Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
	4N55	Dual Channel Hermetically Sealed Analog Optical Coupler	Line Receiver, Analog Signal Ground Isolation, Switching Power Supply Feedback Element	700k bit/s	9% Min.	16 mA	1500 Vdc	6-397
	4N55/883B	MIL-STD-883 Class B Part	Military/High Reliability					
16 pin DIP	5962-8767901EX	DESC Approved 4N55/883B						
	HCPL-5500	Single Channel Hermetically Sealed Analog Optical Coupler	Line Receiver, Analog Signal Ground Isolation, Switching Power Supply Feedback Element					6-405
	HCPL-5501	MIL-STD-883 Class B Part	Military/High Reliability					
8 pin DIP	5962-9085401HPX	DESC Approved HCPL-5501						

High Speed Transistor Optocouplers (Continued)

Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
 8 pin DIP	HCPL-5530	Dual Channel, Hermetically Sealed Analog Optical Coupler	Line Receiver, Analog Signal Ground Isolation, Switching Power Supply Feedback Element	700k bit/s	9% Min.	16 mA	1500 Vdc	6-405
	HCPL-5531	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-8767902PX	DESC Approved HCPL-5531						
 20 Terminal LCC	HCPL-6530	Dual Channel, Hermetically Sealed Analog Optical Coupler	Line Receiver, Analog Signal Ground Isolation, Switching Power Supply Feedback Element					
	HCPL-6531	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-87679032A	DESC Approved HCPL-6531						

Power MOSFET Optocouplers

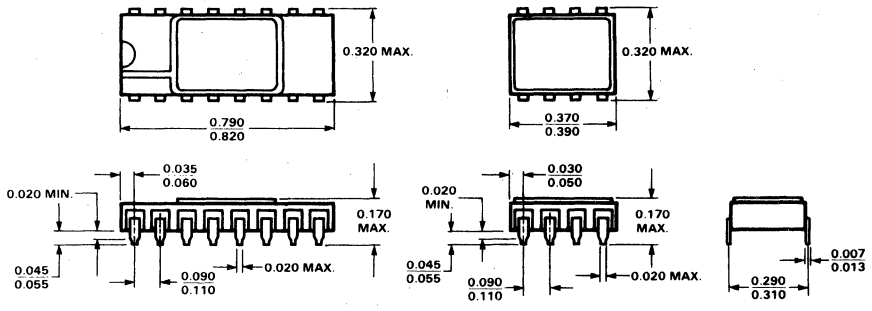
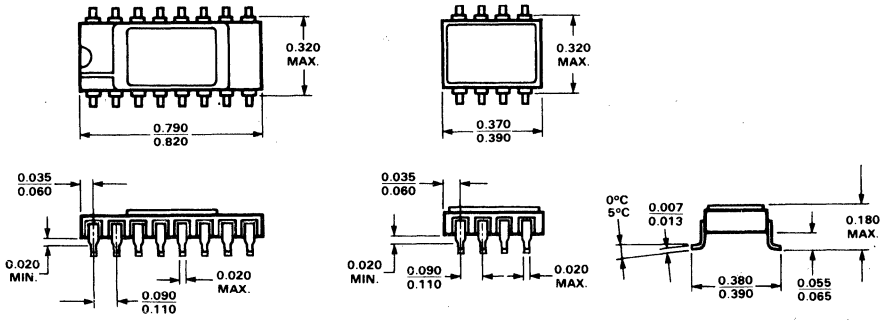
Device		Application	Output Withstand Voltage	Output On-Resistance	Maximum Load Current	Maximum Off-State Leakage	Input/ Output Insulation	Page No.
	New HSSR-7110	Military/High Reliability Systems, Standard 28 Vdc and 48 Vdc Load Driver, Standard 24 Vac Load Driver, ac/dc Electromechanical and Solid State Relay Replacement	90	1.0 Ω	0.8 A ac 1.6 A dc	250 mA	1500 Vdc	6-416

Hermetic High Performance Optocouplers
Functionally Equivalent Part Types

Package Style	16 PIN DIP		8 PIN DIP		20 Terminal LCC	Closest Equivalent Plastic
# of Channels / Function	Quad (4)	Dual (2)	Dual (2)	Single (1)	Dual (2)	Single (1)
High Gain Output, Low Input Current	6N140A **6N140A/883B** *8302401EX*		HCPL-5730 **HCPL-5731** *5962-8978501PX*	HCPL-5700 **HCPL-5701** *5962-8981001PX*	HCPL-6730 **HCPL-6731** *5962-89785022A*	6N138/9
Transistor Output		4N55 **4N55/883B** *5962-8767901EX*	HCPL-5530 **HCPL-5531** *5962-8767902PX*	HCPL-5500 **HCPL-5501** *5962-9085401HPX*	HCPL-6530 **HCPL-6531** *5962-87679032A*	6N135/6
High Speed Logic Output, 10 Mbaud	Special P/N	6N134 **6N134/883B** *8102801EX*	HCPL-5630 **HCPL-5631** *8102802PX*	HCPL-5600 **HCPL-5601** *5962-9085501HPX*	HCPL-6630 **HCPL-6631** *81028032A*	HCPL-2601
High Speed Logic, Input Regulation		HCPL-1930 **HCPL-1931** *5962-8957201EX*	Special P/N	Special P/N	Special P/N	HCPL-2602
Wide Vcc from 4.5 to 20 Volts			HCPL-5230 **HCPL-5231** *5962-8876901PX*	HCPL-5200 **HCPL-5201** *5962-8876801PX*	HCPL-6230 **HCPL-6231** *5962-88769022A*	HCPL-2200
Very High Speed Logic, 20 Mbaud			HCPL-5430 **HCPL-5431** *5962-8957101PX*	HCPL-5400 **HCPL-5401** *5962-8957001PX*	HCPL-6430 **HCPL-6431** *5962-89571022A*	HCPL-2400
AC/DC Logic Interface				HCPL-5760 **HCPL-5761** *5962-8947701PX*	Special P/N Single	HCPL-3700
Power MOSFET Optocoupler				HSSR-7110		

Standard type refers to standard parts
Bold type refers to 883B parts
Italic type refers to DESC Drawing parts

Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on standard product and /883B hi-rel product in 8 and 16 pin DIP (see drawings below for details). Contact factory for the availability of this option on DESC part types. 
200	Lead finish is solder dipped rather than gold plated. This option is available on standard product and /883B product in 8 and 16 pin DIP. DESC Drawing part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder dipped terminals as a standard feature.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on standard product and /883B product in 8 and 16 pin DIP (see drawings below for details). Contact factory for the availability of this option on DESC part types. This option has solder dipped leads. 

HEWLETT PACKARD

Wide Supply Voltage, High CMR, Hermetically Sealed Optocoupler

Technical Data

8 Pin Dual In-Line Package
- **HCPL-5200**
- **HCPL-5201 (883B)**
- **5962-8876801PX**
- **HCPL-5230**
- **HCPL-5231 (883B)**
- **5962-8876901PX**

20 Terminal Leadless Chip Carrier
- **HCPL-6230**
- **HCPL-6231 (883B)**

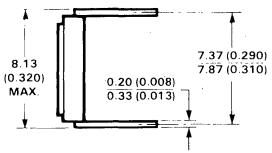
5962-88769022A

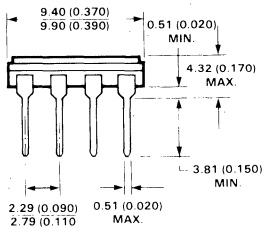
Features
- **Dual Marked with DESC Standard Military Drawing**
- **Manufactured and Tested on a MIL-STD-1772 Certified Line**
- **QML-MIL-H-38534, Class H**
- **Hermetically Sealed Packages**
- **Performance Guaranteed over -55°C to +125°C**
- **MIL-H-38534 Class H Testing**
- **Wide V_{CC} Range (4.5 to 20 V)**
- **300 ns Maximum Propagation Delay**
- **Compatible with LSTTL, TTL, and CMOS Logic**
- **High Common Mode Rejection – 1000 V/μs Guaranteed, 10 KV/μs Selection Available**
- **1500 Vdc Withstand Test Voltage**
- **Three State Output Available**
- **HCPL-2200/31 Function Compatibility**
- **Reliability Data Available**
- **Very Low CTR Degradation**

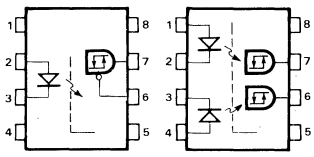
Applications
- **Military/High Reliability Systems**
- **Transportation & Life Critical Systems**
- **Space Level Processing Available**
- **Isolation of High Speed Logic Systems**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **Isolated Bus Driver (Single Channel)**
- **High Speed Line Receiver**

Outline Drawings

8 PIN CERAMIC DUAL IN-LINE PACKAGE





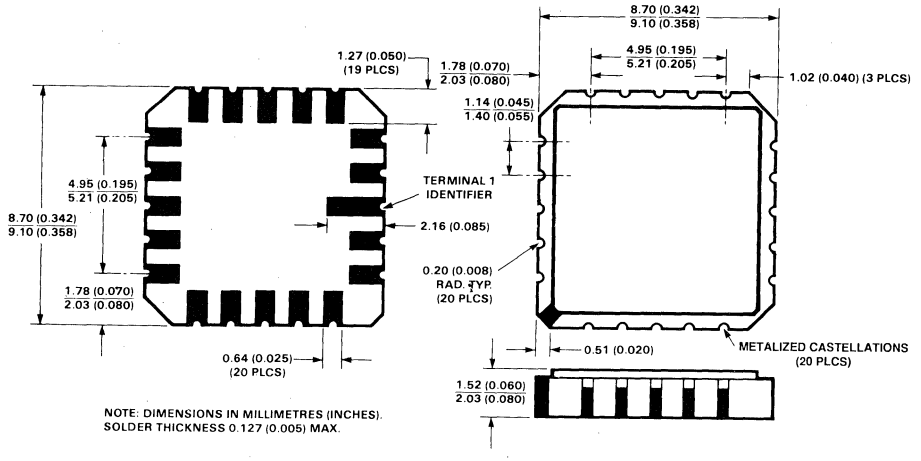


DIMENSIONS IN MILLIMETERS AND (INCHES).
*DETECTOR IC INTERNAL ELECTRICAL SHIELD

For Gull-wing or Butt-joint lead form options, contact your local Hewlett-Packard field representative.

HERMETIC OPTO COUPLERS

20 TERMINAL CERAMIC LEADLESS CHIP CARRIER



Description

The HCPL-5200, HCPL-5201, and 5962-8876801PX are single channel, logic gate optocouplers. The HCPL-5230, HCPL-5231 and 5962-8876901PX are dual channel units made from the same chip sets. All six products are in eight pin hermetic dual in-line packages. These units are capable of operation and storage over the full military temperature ranges and can be purchased as either single or dual channel standard product (HCPL-5200 and HCPL-5230 respectively), with full MIL-H-38534 Class Level H testing (HCPL-5201 and HCPL-5231 respectively), or from the DESC Standard Military Drawings (SMDs) 5962-88768 and 5962-88769 as (5962-8876801PX or 5962-8876901PX respectively). All parts are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the SMD part #, or by adding option #200 to the part number for non-SMD parts.

The HCPL-6230 and HCPL-6231 and 5962-88769022A parts are in twenty terminal hermetic, ceramic, leadless chip carriers. The standard part is HCPL-6230. The product with full MIL-H-38534 Class Level H testing is HCPL-6231. These dual channel devices are configured and function as two independent single channels. Devices are delivered with solder dipped terminals as a standard feature. Units may also be purchased with gold-plated terminals.

Each channel contains an AlGaAs light emitting diode optically coupled to an integrated high gain photon detector. The detector has a threshold with hysteresis. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter. The detector in the single channel units has a three state output stage which allows for direct connection to data buses. The output is non-inverting. The detector IC has an electric shield that provides a guaranteed common mode transient immunity of up to 10,000 V/μs. Improved power supply rejection eliminates the need for special power supply bypass precautions.

All devices are guaranteed to operate over a V_{CC} range of 4.5 Volts to 20 Volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS. Logic low I_F and low I_{CC} result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a typical propagation delay of 100 nsec when used in the circuit of Figure 11.

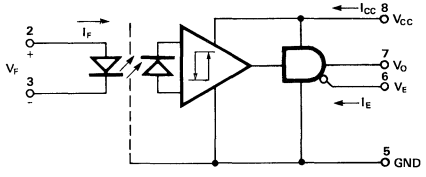
These units are useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

The test programs on the 5962-8876801PX and 5962-8876901PX are in compliance with DESC (SMDs) 5962-88768 and 5962-88769 respectively. The electrical characteristics table shows Group A Subgroup testing requirements from these drawings.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Schematics

8 PIN CERAMIC DIP SINGLE CHANNEL SCHEMATIC

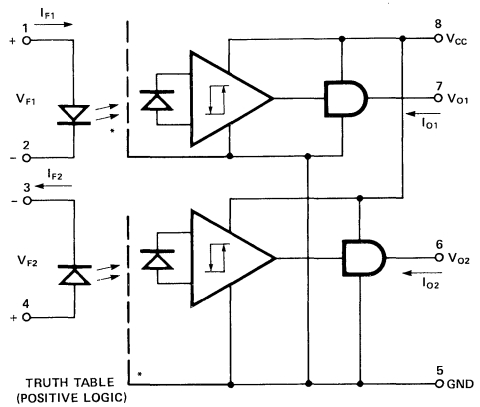


TRUTH TABLE
(POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	Z
OFF	H	Z
ON	L	H
OFF	L	L

DETECTOR IC INTERNAL ELECTRICAL SHIELD

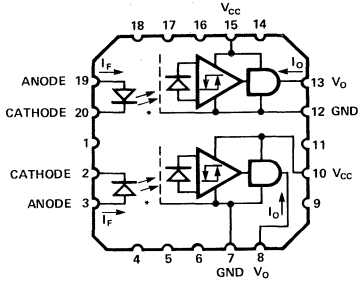
8 PIN CERAMIC DIP DUAL CHANNEL SCHEMATIC



TRUTH TABLE
(POSITIVE LOGIC)

INPUT	OUTPUT
H	H
L	L

20 TERMINAL CERAMIC LEADLESS CHIP CARRIER SCHEMATIC



TRUTH TABLE
(POSITIVE LOGIC)

INPUT	OUTPUT
ON	H
OFF	L

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Input Current (High)	$I_{F(ON)}$	2	8	mA
Input Voltage (Low)	$V_{F(OFF)}$	0	0.8	Volts
Fan Out	N		4	TTL Loads

Single Channel Product Only

Enable Voltage High	V_{EH}	2.0	20	Volts
Enable Voltage Low	V_{EL}	0	0.8	Volts

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Case Temperature – T_C ..... +170°C
Lead Solder Temperature ..... 260°C for 10 s
Junction Temperature (T_J) ..... +175°C
Average Forward Current – $I_{F\,AVG}$ ..... 8 mA
Peak Input Current – $I_{F\,PK}$ ..... 20 mA[1]
Reverse Input Voltage – V_R ..... 3 V
Supply Voltage – V_{CC} ..... 0.0 V min., 20 V max.
Average Output Current – I_O (per channel) ..... 15 mA
Output Voltage – V_O ..... 0.3 V min., 20 V max.
Total Package Power Dissipation – P_d (per channel) ..... 200 mW
Single Channel Product Only
Three State Enable Voltage – V_E ..... -0.3 V min., 20 V max.

Electrical Characteristics

T_A = -55°C to 125°C, unless otherwise specified. For 4.5 V ≤ V_{CC} ≤ 20 V, 2 mA ≤ $I_{F(ON)}$ ≤ 8 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V

Parameter		Sym.	Test Conditions		Group A Subgroups[11]	Min.	Typ.*	Max.	Units	Fig.	Notes
Logic Low Output Voltage		V_{OL}	I_{OL} = 6.4 mA (4 TTL Loads)		1, 2, 3			0.5	Volts	1, 3	2
Logic High Output Voltage		V_{OH}	I_{OH} = -2.6 mA (**V_{OH} = V_{CC} - 2.1 V)		1, 2, 3	2.4	**		Volts	2, 3	2
			I_{OH} = -0.32 mA		NA		3.1		Volts		
Output Leakage Current (V_{OUT} > V_{CC})		I_{OHH}	V_O = 5.5 V	I_F = 8 mA, V_{CC} = 4.5 V	1, 2, 3			100	µA		2
			V_O = 20 V					500	µA		
Logic Low Supply Current	Single Channel (5962-88768)	I_{CCL}	V_{CC} = 5.5 V	V_F = 0 V, V_E = Don't Care	1, 2, 3		4.5	6.0	mA		
			V_{CC} = 20 V				5.3	7.5	mA		
	Dual Channel (5962-88769)		V_{CC} = 5.5 V	V_{F1} = V_{F2} = 0 V	1, 2, 3		9.0	12.0	mA		
			V_{CC} = 20 V				10.6	15	mA		
Logic High Supply Current	Single Channel (5962-88768)	I_{CCH}	V_{CC} = 5.5 V	I_F = 8 mA, V_E = Don't Care	1, 2, 3		2.9	4.5	mA		
			V_{CC} = 20 V				3.3	6.0	mA		
	Dual Channel (5962-88769)		V_{CC} = 5.5 V	I_{F1} = I_{F2} = 8 mA	1, 2, 3		5.8	9.0	mA		
			V_{CC} = 20 V				6.6	12.0	mA		
Logic Low Short Circuit Output Current		I_{OSL}	V_O = V_{CC} = 5.5 V	V_F = 0 V	1, 2, 3	20			mA		2, 3
			V_O = V_{CC} = 20 V			35			mA		
Logic High Short Circuit Output Current		I_{OSH}	V_{CC} = 5.5 V	I_F = 8 mA, V_O = GND	1, 2, 3			-10	mA		2, 3
			V_{CC} = 20 V					-25	mA		
Input Forward Voltage		V_F	I_F = 8 mA		1, 2, 3	1.0	1.3	1.8	Volts	4	2
Input Reverse Breakdown Voltage		V_R	I_R = 10 µA		1, 2, 3	3			Volts		2
Input-Output Insulation		I_{I-O}	45% RH, t = 5 s, V_{I-O} = 1500 Vdc		1			1	µA		4, 5
Propagation Delay Time to Logic Low Output Level		t_{PHL}			9, 10, 11		173	300	ns	5, 6,	2, 6
Propagation Delay Time to Logic High Output Level		t_{PLH}			9, 10, 11		118	300	ns	5, 6,	2, 6
Logic High Common Mode Transient Immunity		$\|CM_H\|$	I_F = 2 mA, V_{CM} = 50 V_{P-P}		9	1000	10,000		V/µs	9	2, 7
Logic Low Common Mode Transient Immunity		$\|CM_L\|$	I_F = 0 mA, V_{CM} = 50 V_{P-P}		9	1000	10,000		V/µs	9	2, 7

Electrical Characteristics Single Channel Product Only

T_A = -55°C to 125°C, unless otherwise specified.
For 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, 4.5 V ≤ V_{CC} ≤ 20 V, 2 mA ≤ $I_{F(ON)}$ ≤ 8 mA, 2.0 V ≤ V_{EH} ≤ 20 V, 0 V ≤ V_{EL} ≤ 0.8 V unless otherwise specified.

Parameter	Sym.	Test Conditions		Group A Subgroups	Min.	Typ.*	Max.	Units	Fig.	Notes
High Impedance State Output Current	I_{OZL}	V_O = 0.4 V	V_{EN} = 2 V, V_F = 0 V	1, 2, 3			-20	µA		
	I_{OZH}	V_O = 2.4 V	V_{EN} = 2 V, I_F = 8 mA	1, 2, 3			20	µA		
		V_O = 5.5 V					100	µA		
		V_O = 20 V					500	µA		
Logic High Enable Voltage	V_{EH}			1, 2, 3	2.0			Volts		
Logic Low Enable Voltage	V_{EL}			1, 2, 3			0.8	Volts		
Logic High Enable Current	I_{EH}	V_{EN} = 2.7 V		1, 2, 3			20	µA		
		V_{EN} = 5.5 V					100	µA		
		V_{EN} = 20 V				0.004	250	µA		
Logic Low Enable Current	I_{EL}	V_{EN} = 0.4 V		1, 2, 3			-0.32	mA		

*All typical values are at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 5 mA unless otherwise specified.

Typical Characteristics

All typical values are at V_{CC} = 5 V, T_A = 25°C), $I_{F(ON)}$ = 5 mA unless otherwise specified.

Parameter	Symbol	Test Conditions	Typ.	Units	Fig.	Notes
Input Current Hysteresis	I_{HYS}	V_{CC} = 5 V	0.07	mA	3	2
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	I_F = 8 mA	-1.25	mV/°C		2
Input-Output Resistance	R_{I-O}	V_{I-O} = 500 Vdc	10^{13}	Ω		2, 8
Input-Output Capacitance	C_{I-O}	f = 1 MHz	2.0	pF		2, 8
Input Capacitance	C_{IN}	f = 1 MHz, V_F = 0 V	20	pF		2, 10
Output Rise Time (10-90%)	t_r		45	ns	5, 7	2
Output Fall Time (90-10%)	t_f		10	ns	5, 7	2
Single Channel Product Only						
Output Enable Time to Logic High	t_{PZH}		30	ns	8	
Output Enable Time to Logic Low	t_{PZL}		30	ns	8	
Output Disable Time from Logic High	t_{PHZ}		45	ns	8	
Output Disable Time from Logic Low	t_{PLZ}		55	ns	8	
Dual Channel Product Only						
Input-Input Insulation Leakage Current	I_{I-I}	45% Relative Humidity, V_{I-I} = 500 Vdc, T_A = 25°C, t = 5 s	0.5	nA		9
Resistance (Input-Input)	R_{I-I}	V_{I-I} = 500 Vdc	10^{13}	Ω		9
Capacitance (Input-Input)	C_{I-I}	f = 1 MHz	1.5	pF		9

Notes:

1. Peak Forward Input Current pulse width < 50 μs at 1 KHz maximum repetition rate.
2. Each channel.
3. Duration of output short circuit time not to exceed 10 ms.
4. Device considered a two terminal device: for 8 pin DIP, pins 1 through 4 are shorted together, and pins 5 through 8 are shorted together; for LCC, terminals 19, 20, 1, 2, 3 are shorted together, and terminals 7 through 15 are shorted together.
5. This is a momentary withstand test, not an operating condition.
6. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
7. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).
8. Measured between each input pair shorted together and all outputs for that channel shorted together.
9. Measured between adjacent input pairs shorted together; i.e., for 8 pin DIP, between pins 1 and 2 shorted together and pins 3 and 4 shorted together; for LCC, between terminals 19 and 20 shorted together, and terminals 2 and 3 shorted together.
10. Zero-bias capacitance measured between the LED anode and cathode.
11. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

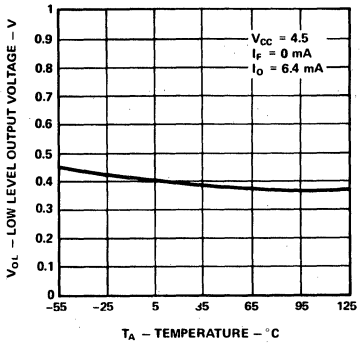


Figure 1. Typical Logic Low Output Voltage vs. Temperature

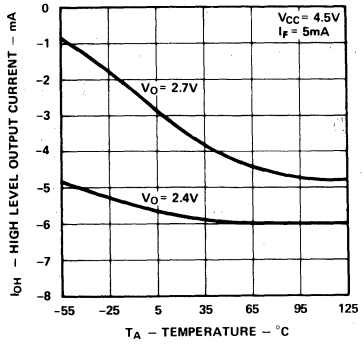


Figure 2. Typical Logic High Output Current vs. Temperature

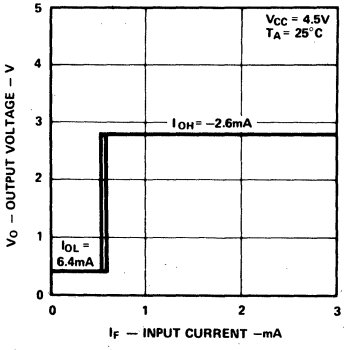


Figure 3. Output Voltage vs. Forward Input Current

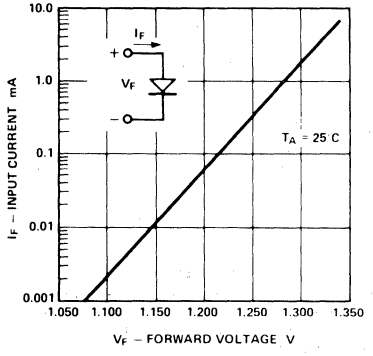


Figure 4. Typical Diode Input Forward Characteristic

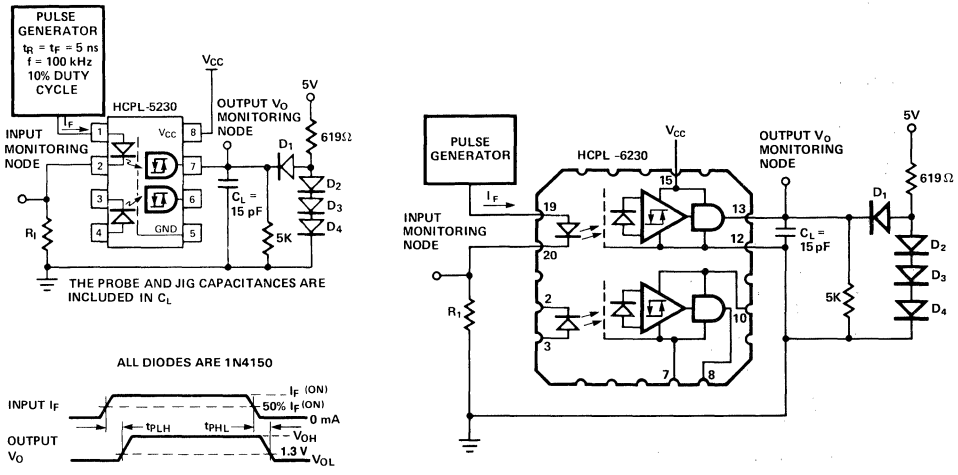


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

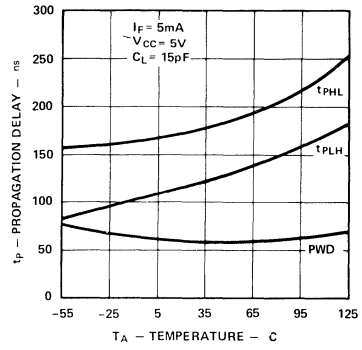


Figure 6. Typical Propagation Delay vs. Temperature

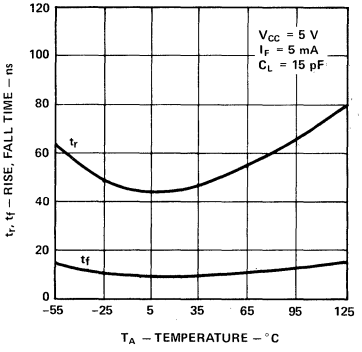


Figure 7. Typical Rise, Fall Time vs. Temperature

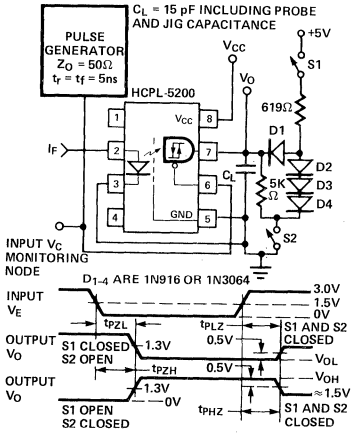


Figure 8. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}

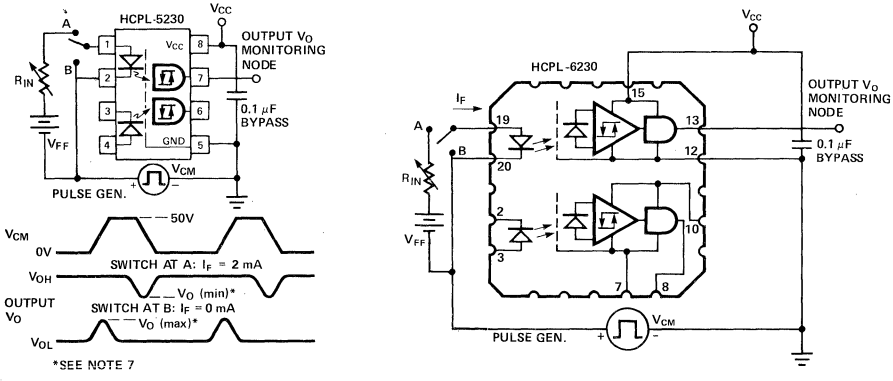


Figure 9. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

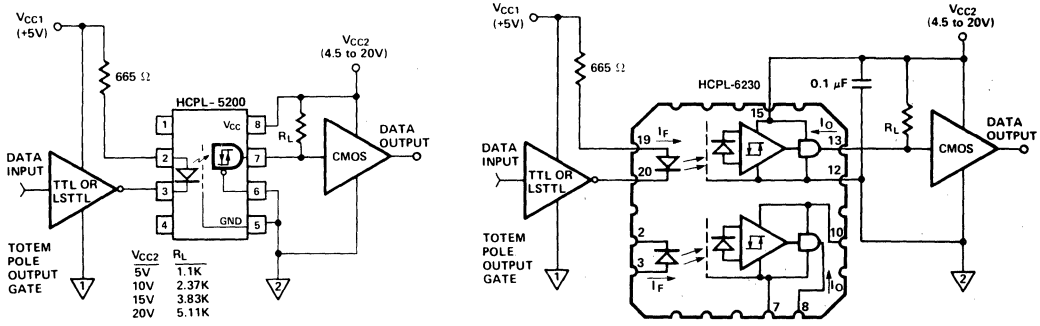


Figure 10. LSTTL to CMOS Interface Circuit.

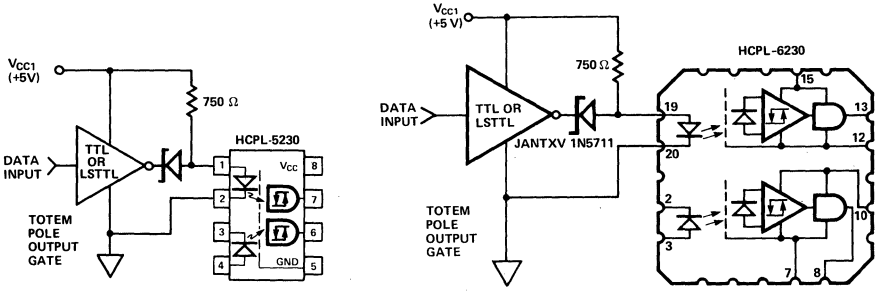


Figure 11. Recommended LED Drive Circuit.

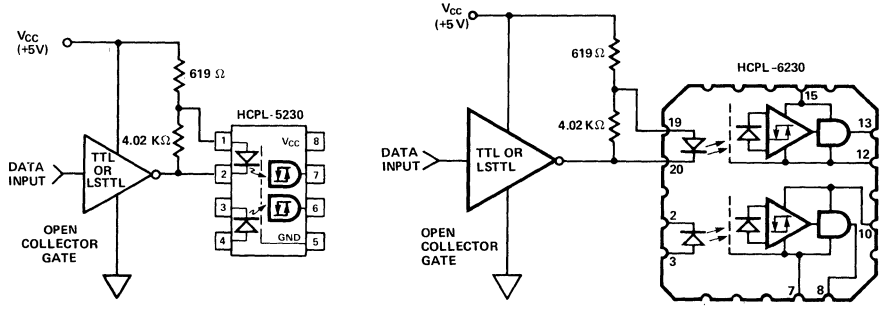


Figure 12. Series LED Drive with Open Collector Gate (4.02 kΩ Resistor Shunts I_{OH} from the LED)

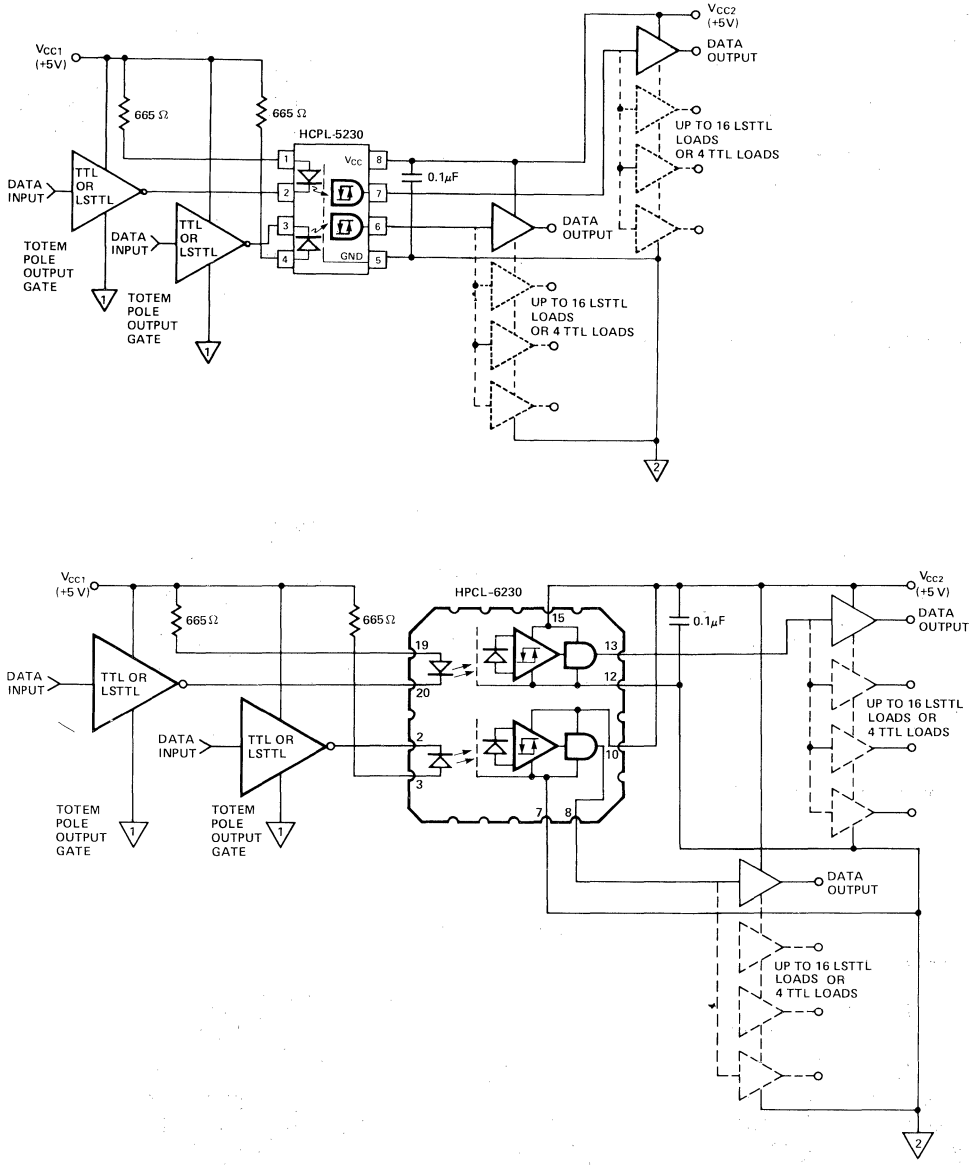


Figure 13. Recommended LSTTL to LSTTL Circuit

Part Numbering System

Commercial Product	Class H Product	DESC Product	Class K Product
HCPL-5200	HCPL-5201	5962-8876801PX	TBD
HCPL-5230	HCPL-5231	5962-8876901PX	TBD
HCPL-6230	HCPL-6231	5962-88769022A	TBD

5962-8876801PX, 5962-8876901PX, 5962-88769022A and MIL-H-38534 Class H Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-H-38534 and DESC SMD's 5962-88768 and 5962-88769.

Testing consists of 100% screening and quality conformance inspection to MIL-H-38534.

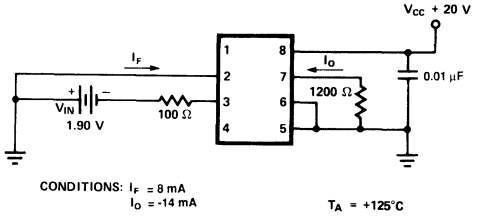


Figure 14. Single Channel Operating Circuit for Burn-in and Steady State Life Tests

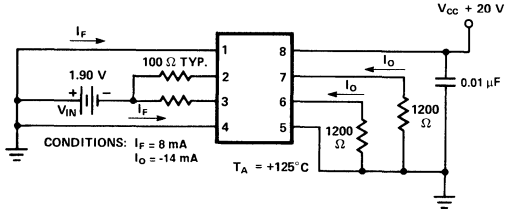


Figure 15. Dual Channel Operating Circuit for Burn-in and Steady State Life Tests

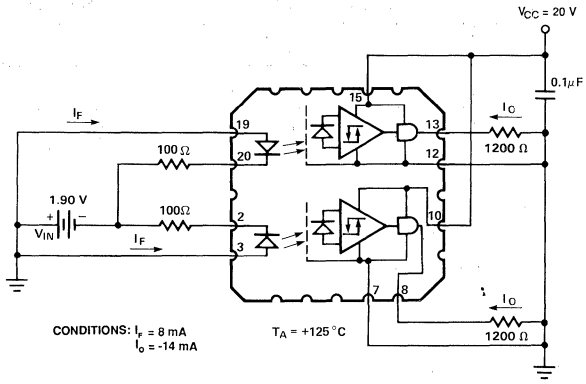
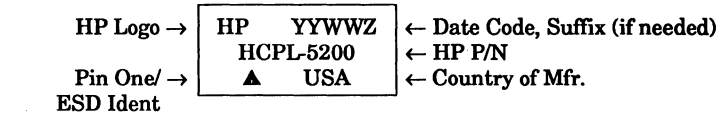


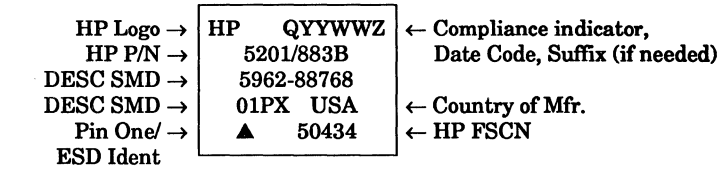
Figure 16. Operating Circuit for Burn-In and Steady State Life Tests

Part Marking Orientation for HCPL-52XX and HCPL-623X Base Product and Related DESC Productss

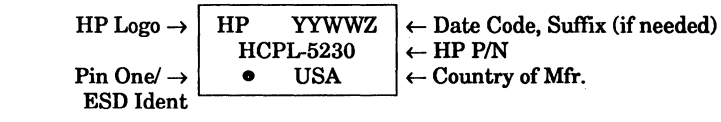
HCPL-5200
ESD Class 1



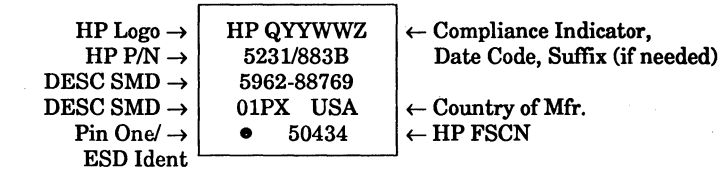
HCPL-5201
5962-8876801PX*
ESD Class 1



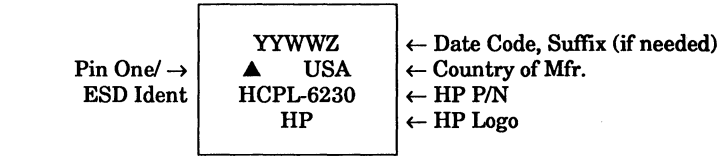
HCPL-5230
ESD Class 3



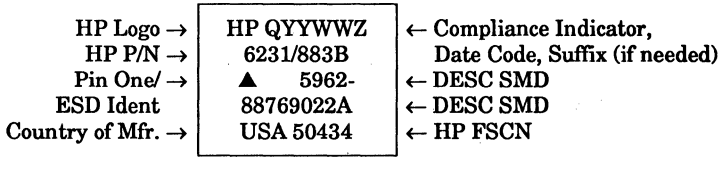
HCPL-5231
5962-8876901PX*
ESD Class 3



HCPL-6230
ESD Class 1



HCPL-6231
5962-88769022A
ESD Class 1



*"X" is not marked on device. Replace "X" with "C" for gold leads; replace "X" with "A" for solder dipped leads.

HEWLETT PACKARD

Very High Speed, Hermetically Sealed Optocoupler

Technical Data

8- pin Dual In-Line Package
HCPL-5400
HCPL-5401 (883B)
5962-8957001PX

HCPL-5430
HCPL-5431 (883B)
5962-8957101PX

20 Terminal Leadless Chip Carrier
HCPL-6430
HCPL-6431 (883B)
5962-89571022A

Features

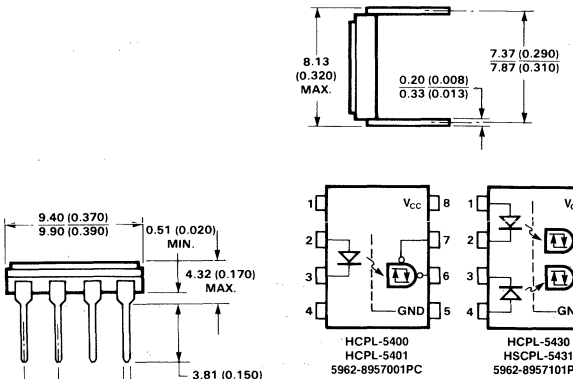
- Dual Marked with DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534
- Hermetically Sealed Packages
- Performance Guaranteed Over -55°C to +125°C
- MIL-H-38534 Class H
- High Speed Guaranteed Over Temperature
- 60 ns Maximum Propagation Delay
- 35 ns Maximum Pulse Width Distortion
- High Common Mode Rejection – 500 V/μs Guaranteed
- Compatible with TTL, STTL, LSTTL and HCMOS Logic Families
- Three State Output (No Pull-Up Resistor Required) – (5400/1 Only)
- HCPL-2400/30 Function Compatibility
- 1500 Vdc Withstand Test Voltage
- Reliability Data Available
- Very Low CTR Degradation
- Active (Totem-Pole) Outputs

Applications

- Military/High Reliability Systems
- Isolation of High Speed Logic Systems
- Computer-Peripheral Interfaces
- Isolated Bus Driver (Networking Applications) – (5400/1 Only)
- Space Level Processing Available
- Transportation and Life Critical Systems
- Switching Power Supplies
- Ground Loop Elimination
- High Speed Disk Drive I/O
- Digital Isolation for A/D, D/A Conversion
- Pulse Transformer Replacement

Outline Drawings

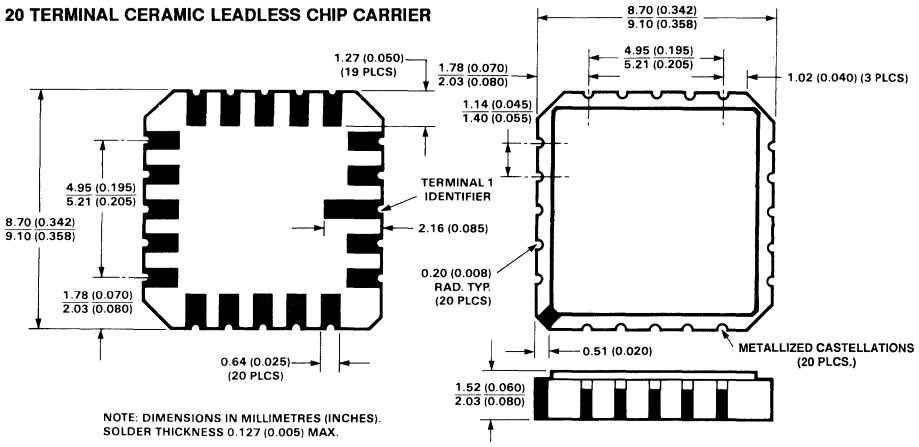
8 PIN CERAMIC DUAL-IN-LINE PACKAGE



DIMENSIONS IN MILLIMETERS AND (INCHES).
*DETECTOR IC INTERNAL ELECTRICAL SHIELD

For Gull-wing or Butt-joint lead form options, contact your local Hewlett-Packard field representative.

20 TERMINAL CERAMIC LEADLESS CHIP CARRIER



NOTE: DIMENSIONS IN MILLIMETRES (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

Description

The HCPL-5400, HCPL-5401, and 5962-8957001PC are single channel, logic gate optocouplers. The HCPL-5430, HCPL-5431, and 5962-8957101PC are dual channel units made from the same chip sets. All six products are in 8 pin hermetic dual in-line packages. These units are capable of operation and storage over the full military temperature ranges and can be purchased as either single or dual channel standard product (HCPL-5400 and HCPL-5430 respectively), with full MIL-H-38534 Class Level H testing (HCPL-5401 and HCPL-5431 respectively), or from the DESC Standard Military Drawings (SMDs) 5962-89570 and 5962-89571 as (5962-8957001PC or 5962-8957101PC respectively). All parts are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the SMD part #, or by adding option #200 to the part number for non-SMD parts.

The HCPL-6430, HCPL-6431, and 5962-89571022A are dual channel parts in twenty terminal hermetic, ceramic, leadless chip carriers. The standard part is HCPL-6430. The product with full MIL-H-38534 Class Level H testing is HCPL-6431. The DESC SMD part is 5962-89571022A. All three products are configured and function as two independent single channels without enable. Devices are delivered with solder-dipped terminals as a standard feature. Units may also be purchased with gold-plated terminals.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

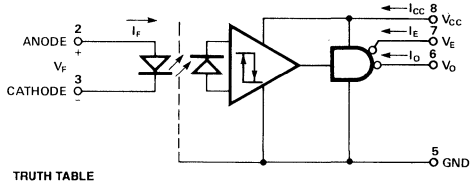
Each channel contains an AlGaAs light emitting diode which is optically coupled to an integrated high gain photon detector. This combination results in very high data rate capability. The detector has a threshold with hysteresis. The hysteresis provides typically 0.25 mA of differential mode noise immunity and minimizes the potential for output signal chatter. The detector in the single channel units has a three state output stage which eliminates the need for a pull-up resistor and allows for direct drive of a data bus.

All nine units are compatible with TTL, STTL, LSTTL, and HCMOS logic families. The 35 ns pulse width distortion specification guarantees a 10 mBaud signaling rate at +125°C with 35% pulse width distortion. Figures 11 through 16 show recommended circuits for reducing pulse width distortion and optimizing the signal rate of the product.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Schematics

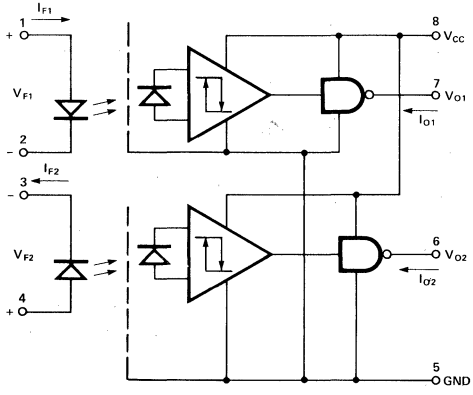
8 PIN CERAMIC DIP SINGLE CHANNEL SCHEMATIC



TRUTH TABLE
(POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	L	L
OFF	L	H
ON	H	Z
OFF	H	Z

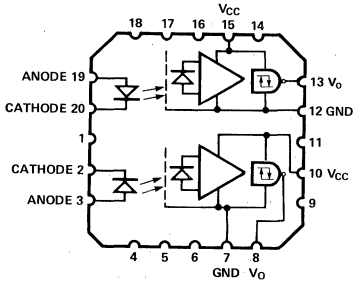
8 PIN CERAMIC DIP DUAL CHANNEL SCHEMATIC



TRUTH TABLE
(POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	L	L
OFF	L	H
ON	H	Z
OFF	H	Z

20 TERMINAL CERAMIC LEADLESS CHIP CARRIER SCHEMATIC



TRUTH TABLE
(POSITIVE LOGIC)

INPUT	OUTPUT
ON	L
OFF	H

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.75	5.25	Volts
Input Current (High)	$I_{F(ON)}$	6	10	mA
Input Voltage (Low)	$V_{F(OFF)}$	–	0.7	Volts
Fan Out (each channel)	N	–	5	TTL Loads

Single Channel Product Only

Enable Voltage (Low)	V_{EL}	0	0.8	Volts
Enable Voltage (High)	V_{EH}	2.0	V_{CC}	Volts

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Case Temperature – T_C ..... +170°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Forward Current – $I_{F\,AVG}$ ..... 10 mA
Peak Input Current – $I_{F\,PK}$ ..... 20 mA[1]
Reverse Input Voltage – V_R ..... 3 V
Supply Voltage – V_{CC} ..... 0 V min., 7.0 V max.
Average Output Current – I_O ..... -25 mA min., 25 mA max.
Output Voltage – V_O ..... -0.5 V min., 10 V max.
Output Power Dissipation – P_O (per channel) ..... 130 mW
Total Package Power Dissipation P_d ..... 400 mW
Single Channel Product Only
Three State Enable Voltage – V_E ..... -0.5 V min., 10 V max.

Electrical Characteristics

T_A = -55°C to 125°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, 6 mA ≤ $I_{F(ON)}$ ≤ 10 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.7 V, unless otherwise specified.

Parameter		Sym.	Test Conditions	Group A[10] Subgroup	Min.	Typ.*	Max.	Units	Fig.	Notes
Logic Low Output Voltage		V_{OL}	I_{OL} = 8.0 mA (5 TTL Loads)	1, 2, 3			0.5	Volts	1	9
Logic High Output Voltage		V_{OH}	I_{OH} = -4.0 mA	1, 2, 3	2.4			Volts	2	9
Output Leakage Current		I_{OHH}	V_O = 5.25 V, V_F = 0.7 V	1, 2, 3			100	µA		9
Logic Low Supply Current	Single Channel	I_{CCL}	V_{CC} = 5.25 V V_E = 0 V (Single Channel Only)	1, 2, 3		19	26	mA		
	Dual Channel					38	52			14
Logic High Supply Current	Single Channel	I_{CCH}		1, 2, 3		17	26	mA		
	Dual Channel					34	52			14
Input Forward Voltage		V_F	I_F = 10 mA	1, 2, 3	1.0	1.35	1.85	Volts	4	9
Input Reverse Breakdown Voltage		V_R	I_R = 10 µA	1, 2, 3	3.0	7.0		Volts		9
Input-Output Insulation Leakage Current		I_{I-O}	45% RH, t = 5 s, V_{I-O} = 1500 Vdc	1			1	µA		2, 3
Propagation Delay Time Logic Low Output Level		t_{PHL}		9, 10, 11		33	60	ns	5, 6, 7	4, 9
Propagation Delay Time Logic High Output Level		t_{PLH}		9, 10, 11		30	60	ns	5, 6, 7	4, 9
Pulse Width Distortion		PWD		9, 10, 11		3	35	ns	5, 6, 7	4, 9
Logic High Common Mode Transient Immunity		$\|CM_H\|$	I_F = 0 V_{CM} = 50 V_{P-P}	9, 10, 11	500	3000		V/µs	11	5, 9, 11
Logic Low Common Mode Transient Immunity		$\|CM_L\|$	I_F = 6 mA V_{CM} = 50 V_{P-P}	9, 10, 11	500	3000		V/µs	11	5, 9, 11

Guaranteed Performance

T_A = -55°C to 125°C

Propagation Delay Skew	t_{PSK}				30		ns	10	12, 13

Electrical Characteristics (continued)

T_A = -55°C to 125°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, 6 mA ≤ $I_{F\,(ON)}$ ≤ 10 mA, 0 V ≤ $V_{F\,(OFF)}$ ≤ 0.7 V, unless otherwise specified.

Single Channel Product Only

Parameter	Sym.	Test Conditions		Group A[10] Subgroup	Min.	Typ.*	Max.	Units	Fig.	Notes
Logic High Enable Voltage	V_{EH}			1, 2, 3	2.0			Volts		
Logic Low Enable Voltage	V_{EL}			1, 2, 3			0.8	Volts		
Logic High Enable Current	I_{EH}	V_E = 2.4 V		1, 2, 3			20	µA		
		V_E = 5.25 V,		1, 2, 3			100	µA		
Logic Low Enable Current	I_{EL}	V_E = 0.4 V		1, 2, 3		-0.28	-0.4	mA		
High Impedance State Supply Current	I_{CCZ}	V_{CC} = 5.25 V V_E = 5.25 V		1, 2, 3		22	28	mA		
High Impedance State Output Current	I_{OZL}	V_O = 0.4 V, V_E = 2 V		1, 2, 3			-20	µA		
	I_{OZH}	V_O = 2.4 V	V_E = 2 V	1, 2, 3			20	µA		
		V_O = 5.25 V					100	µA		

*All typical values are at V_{CC} = 5 V, T_A = 25°C, I_F = 8 mA except where noted.

Typical Characteristics

All typical values are at V_{CC} = 5 V, T_A = 25°C, I_F = 8 mA unless otherwise specified.

Parameter	Symbol	Typical	Units	Test Conditions	Figure	Note
Input Current Hysteresis	I_{HYS}	0.25	mA	V_{CC} = 5 V	3	
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	-1.11	mV/°C	I_F = 10 mA	4	
Input-Output Resistance	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 Vdc		2
Input-Output Capacitance	C_{I-O}	0.6	pF	f = 1 MHz, V_{I-O} = 0 Vdc		2
Logic Low Short Circuit Output Current	I_{OSL}	65	mA	V_O = V_{CC} = 5.25 V, I_F = 10 mA		6, 9
Logic High Short Circuit Output Current	I_{OSH}	-50	mA	V_{CC} = 5.25 V, I_F = 0 mA, V_O = GND		6, 9
Output Rise Time (10-90%)	t_r	15	ns		5	
Output Fall Time (90-10%)	t_f	10	ns		5	
Power Supply Noise Immunity	PSNI	0.5	V_{P-P}	48 Hz ≤ f_{ac} ≤ 50 MHz		7
Single Channel Product Only						
Input Capacitance	C_{IN}	15	pF	f = 1 MHz, V_F = 0 V, Pins 2 and 3		
Output Enable Time to Logic High	t_{PZH}	15	ns		8, 9	
Output Enable Time to Logic Low	t_{PZL}	30	ns		8, 9	
Output Disable Time from Logic High	t_{PHZ}	20	ns		8, 9	
Output Disable Time from Logic Low	t_{PLZ}	15	ns		8, 9	
Dual Channel Product Only						
Input Capacitance	C_{IN}	15	pF	f = 1 MHz, V_O = 0 V, Pins 1 and 2, Pins 3 and 4		
Input-Input Capacitance	C_{I-I}	1.3	pF	f = 1 MHz, V_F = 0 V		8
Input-Input Leakage Current	I_{I-I}	0.5	nA	V_{I-I} = 500 Vdc, 45% RH		8
Input-Input Resistance	R_{I-I}	10^{12}	ohms	V_{I-I} = 500 Vdc		8

Notes:

1. Not to exceed 5% duty factor, not to exceed 50 μsec pulse width.
2. Device considered a two terminal device: for 8 pin DIP, pins 1 through 4 are shorted together, and pins 5 through 8 are shorted together; for LCC, terminals 19, 20, 1, 2, 3 are shorted together, and terminals 7 through 15 are shorted together.
3. This is a momentary withstand test, not an operating condition.
4. t_{PHL} propagation delay is measured from the 50% level on the rising edge of the input current pulse to the 1.5 V level on the falling edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% level on the falling edge of the input current pulse to the 1.5 V level on the rising edge of the output pulse. Pulse width distortion, PWD = $|t_{PHL}-t_{PLH}|$.
5. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_{O(MIN)}$ > 2.0 V). CM_L is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic low state ($V_{O(MAX)}$ < 0.8 V).
6. Duration of output short circuit time not to exceed 10 ms.
7. Power Supply Noise Immunity is the peak to peak amplitude of the ac ripple voltage on the V_{CC} line that the device will withstand and still remain in the desired logic state. For desired logic high state, $V_{OH(MIN)}$ > 2.0 V, and for desired logic low state, $V_{OL(MAX)}$ < 0.8 volts.
8. Measured between adjacent input pairs shorted together; i.e., for 8 pin DIP, between pins 1 and 2 shorted together and pins 3 and 4 shorted together; for LCC, between terminals 19 and 20 shorted together, and terminals 2 and 3 shorted together.
9. Each channel.
10. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and/883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
11. Subgroups 10 and 11 shall be tested as part of device initial characterization and after design and process changes. Subgroups 10 and 11 shall be guaranteed to the limits specified for all lots not specifically tested. Subgroup 9 shall be tested with every lot.
12. Propagation delay skew is defined as the difference between the minimum and maximum propagation delays for any given group of HCPL-540X, HCPL-543X, and HCPL-643X optocouplers that are all switching at the same time under the same operating conditions. The minimum propagation delay is the shortest delay, either t_{PLH} or t_{PHL}, of any of the optocouplers; the maximum delay is the longest delay, either t_{PLH} or t_{PHL}, of any of the optocouplers. For more application information see HCPL-2430 data sheet.
13. Propagation delay skew is indirectly tested and guaranteed through guardbanding of the minimum and maximum t_{PHL} and t_{PLH} limits.
14. The HCPL-6430 and HCPL-6431 dual channel parts function as two independent single channel units. Use the single channel parameter limits.

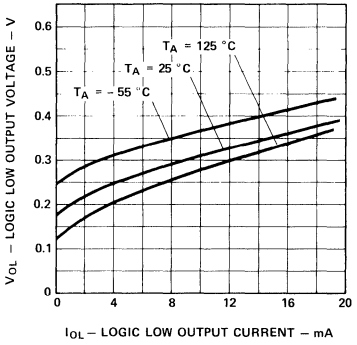


Figure 1. Typical Logic Low Output Voltage vs. Logic Low Output Current.

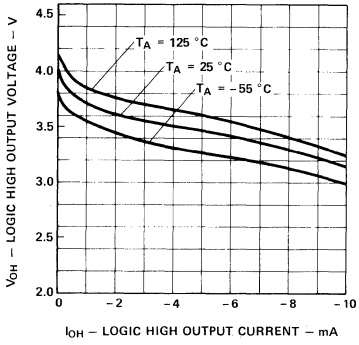


Figure 2. Typical Logic High Output Voltage vs. Logic High Output Current.

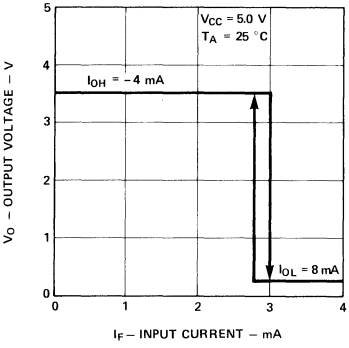


Figure 3. Typical Output Voltage vs. Input Forward Current.

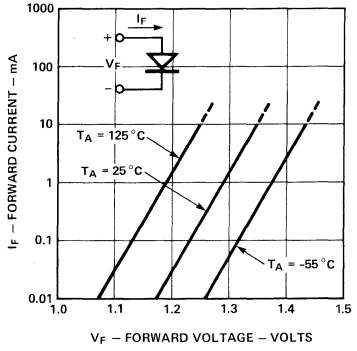


Figure 4. Typical Diode Input Forward Current Characteristic.

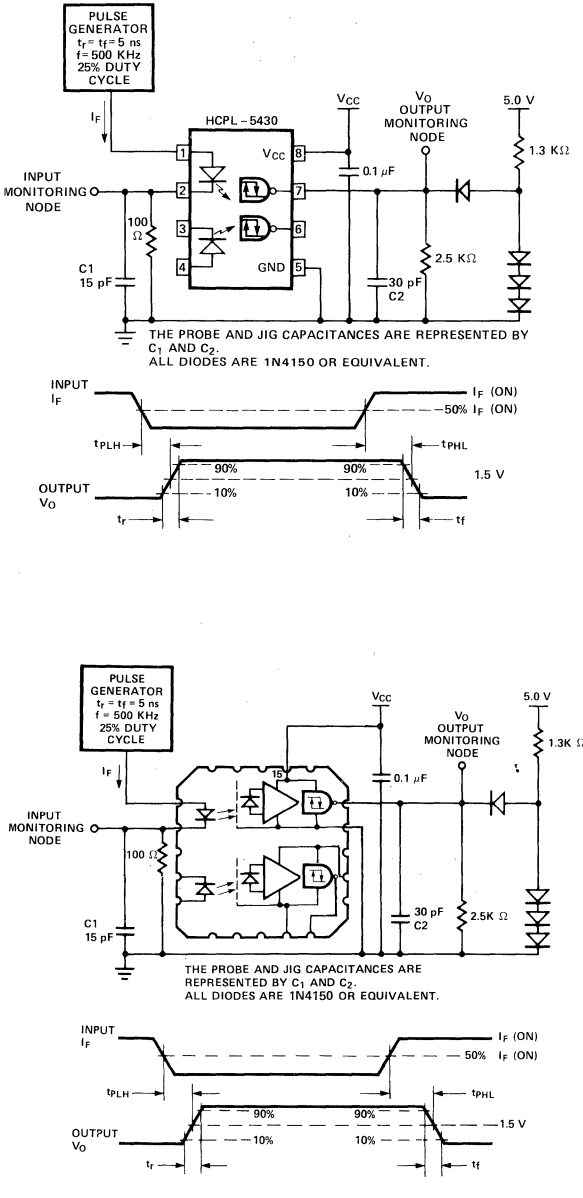


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f.

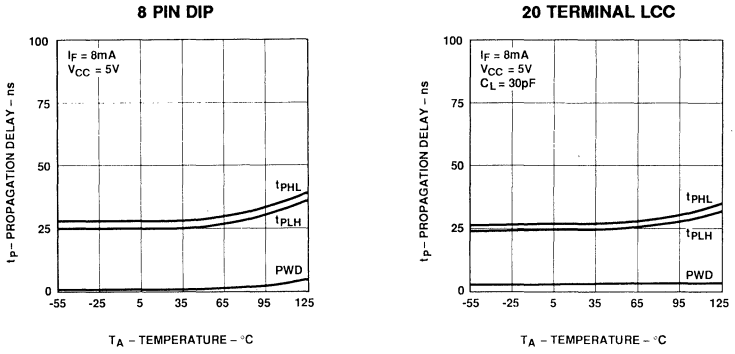


Figure 6. Typical Propagation Delay vs. Ambient Temperature.

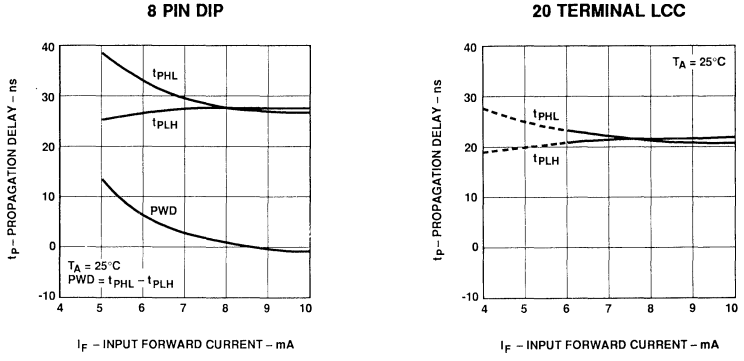
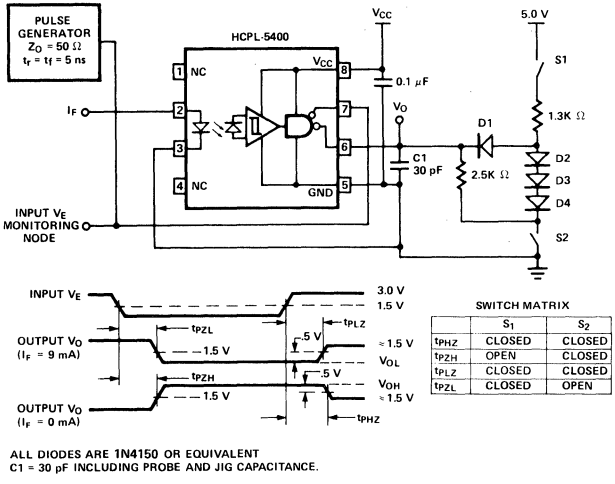


Figure 7. Typical Propagation Delay vs. Input Forward Current.



ALL DIODES ARE 1N4150 OR EQUIVALENT
C1 = 30 pF INCLUDING PROBE AND JIG CAPACITANCE.

Figure 8. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}. (Single Channel Product Only).

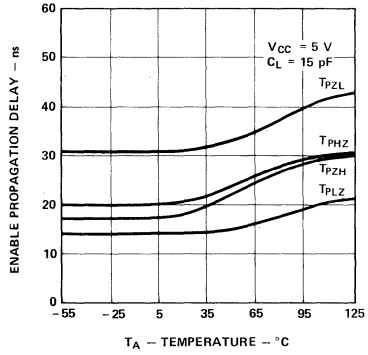


Figure 9. Typical Enable Propagation Delay vs. Ambient Temperature. (Single Channel Product Only).

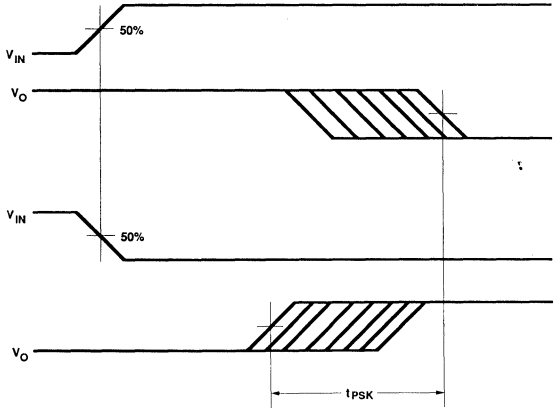
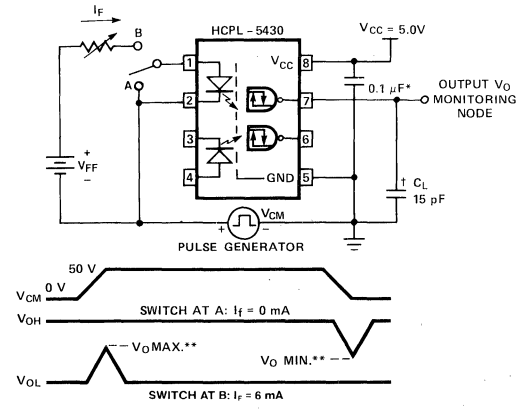
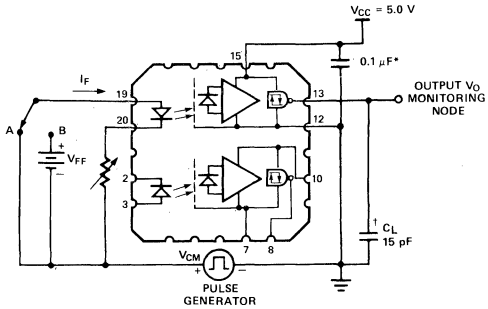


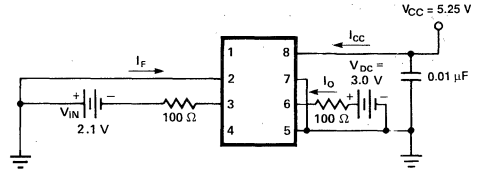
Figure 10. Propagation Delay Skew, t_{PSK}, Waveform.



*TOTAL LEAD LENGTH < 10 mm FROM DEVICE UNDER TEST.
**SEE NOTE 5.
†C_L IS APPROXIMATELY 15 pF, WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

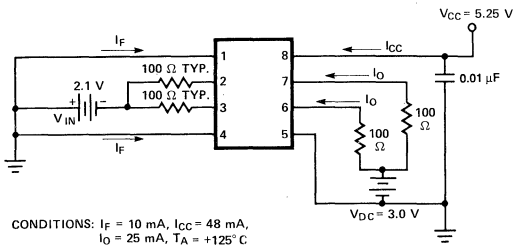
Figure 11. Test Diagram for Common Mode Transient Immunity and Typical Waveforms.





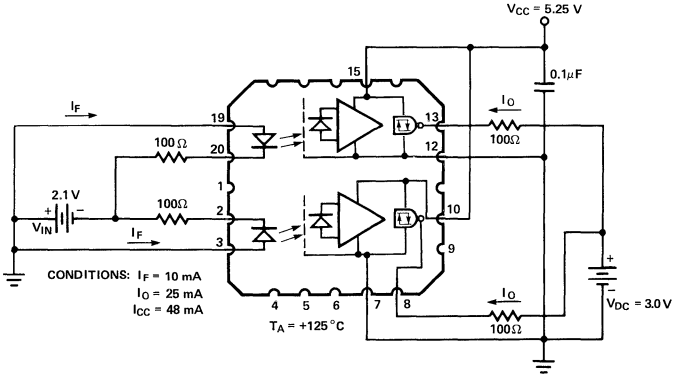
CONDITIONS:
I_F = 10 mA, I_{CC} = 25 mA,
I_O = 25 mA, T_A = +125°C

Figure 12. Single Channel Operating Circuit for Burn-In and Steady State Life Tests.



CONDITIONS: I_F = 10 mA, I_{CC} = 48 mA,
I_O = 25 mA, T_A = +125°C

Figure 13. Dual Channel Operating Circuit for Burn-In and Steady State Life Tests.



CONDITIONS: I_F = 10 mA
I_O = 25 mA
I_{CC} = 48 mA
T_A = +125°C

Figure 14. Operating Circuit for Burn-In and Steady State Life Tests.

Part Numbering System

Commercial Product	Class H Product	DESC Product	Class K Product
HCPL-5400	HCPL-5401	5962-8957001PX	TBD
HCPL-5430	HCPL-5431	5962-8957101PX	TBD
HCPL-6430	HCPL-6431	5962-89571022A	TBD

5962-8957001PC, 5962-8957101PC, 5962-89571022A, and MIL-H-38534 Class H Test Programs

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-H-38534 and DESC SMD's 5962-89570 and 5962-89571.

Testing consists of 100% screening and quality conformance inspection to MIL-H-38534.

Data Rate and Pulse-Width Distortion Definitions

Propagation delay is a figure of merit which describes the finite amount of time required for a system to translate information from input to output when shifting logic levels. Propagation delay from low to high (t_{PLH}) specifies the amount of time required for a system's output to change from a Logic 0 to a Logic 1, when given a stimulus at the input. Propagation delay from high to low (t_{PHL}) specifies the amount of time required for a system's output to change from a Logic 1 to a Logic 0, when given a stimulus at the input (see Figure 5).

When t_{PLH} and t_{PHL} differ in value, pulse width distortion results. Pulse width distortion is defined as $|t_{PHL}-t_{PLH}|$ and determines the maximum data rate capability of a distortion-limited system. Maximum pulse width distortion on the order of 25-35% is typically used when specifying the maximum data rate capabilities of systems. The exact figure depends on the particular application (RS-232, PCM, T-1, etc.).

These high performance optocouplers offer the advantages of specified propagation delay (t_{PLH}, t_{PHL}), and pulse-width distortion ($|t_{PLH} - t_{PHL}|$) over temperature and power supply voltage ranges.

Applications

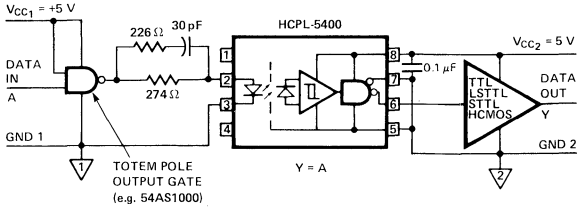


Figure 15. Recommended HCPL-5400 Interface Circuit.

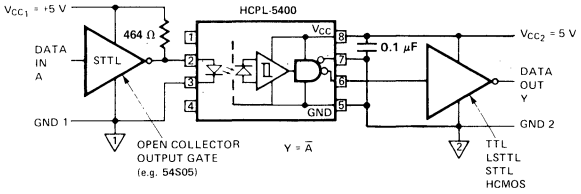


Figure 16. Alternative HCPL-5400 Interface Circuit.

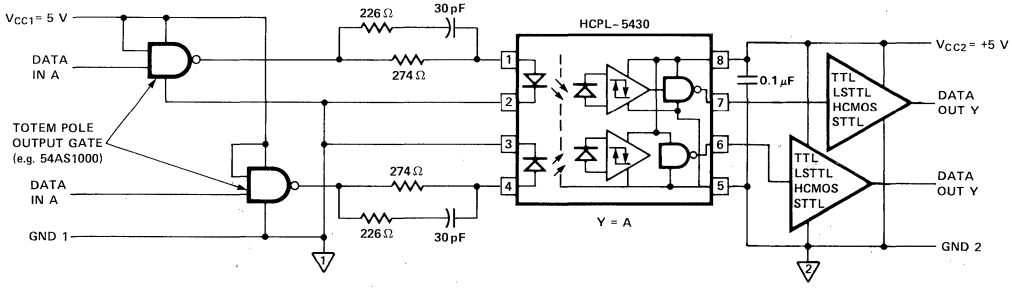


Figure 17. Recommended HCPL-5430 Interface Circuit.

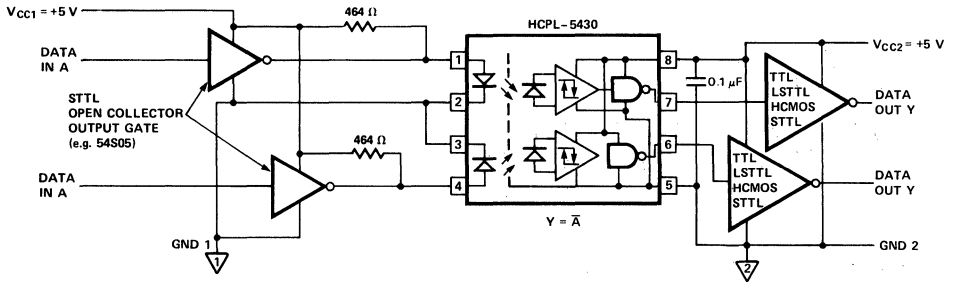


Figure 18. Alternative HCPL-5430 Interface Circuit.

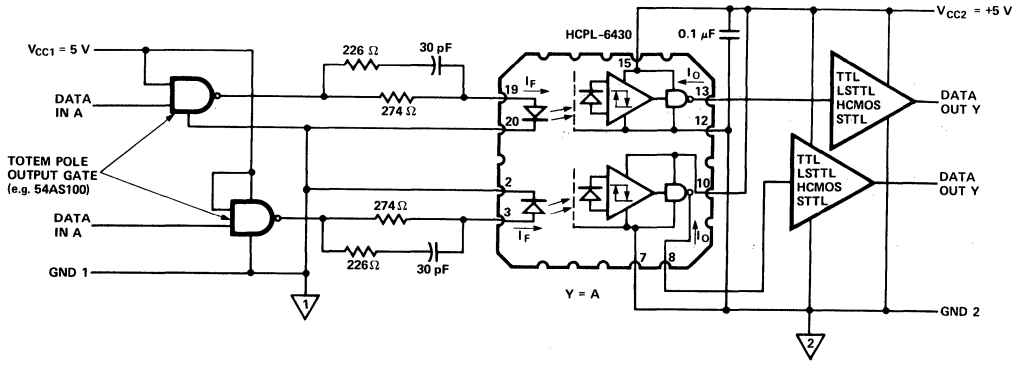


Figure 19. Recommended HCPL-6430 Interface Circuit.

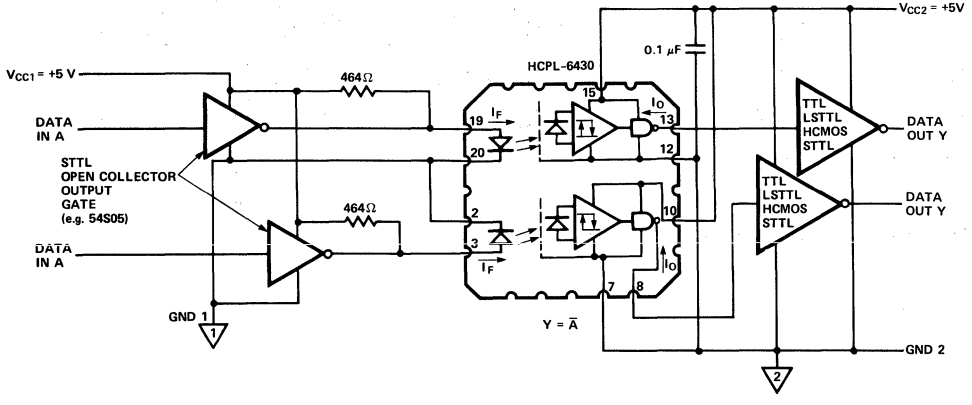
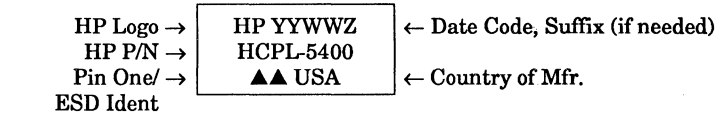


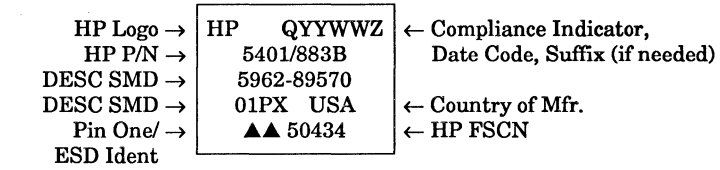
Figure 20. Alternative HCPL-6430 Interface Circuit.

Part Marking Orientation for HCPL-54XX and HCPL-643X Base Product and Related DESC Products

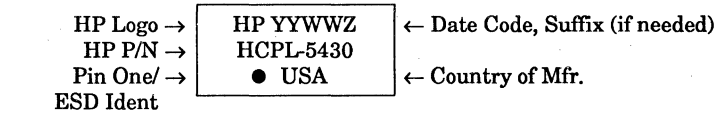
HCPL-5400
ESD Class 2



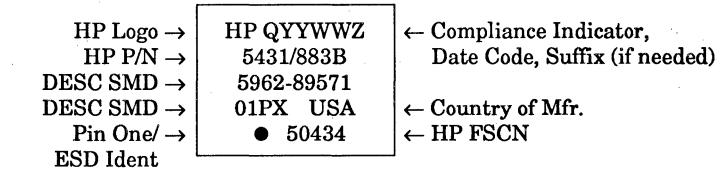
HCPL-5401
5962-8957001PX*
ESD Class 2



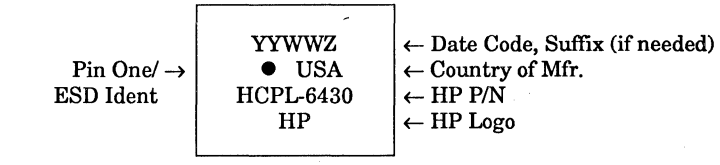
HCPL-5430
ESD Class 3



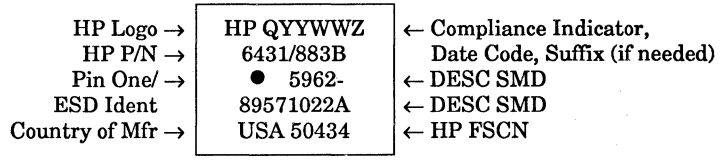
HCPL-5431
5962-8957101PX*
ESD Class 3



HCPL-6230
ESD Class 3



HCPL-6231
5962-89571022A
ESD Class 3



*"X" is not marked on device. Replace "X" with "C" for gold leads; replace "X" with "A" for solder dipped leads.

HEWLETT PACKARD

Dual Channel High CMR High Speed Hermetically Sealed Optocouplers

Technical Data

6N134
6N134/883B
8102801EX

Features

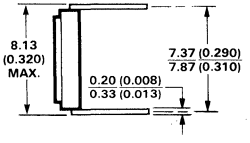
- **Dual Marked with DESC Standard Military Drawing**
- **Manufactured and Tested on a MIL-STD-1772 Certified Line**
- **QML-MIL-H-38534, Class H**
- **Hermetically Sealed 16-pin Dual In-Line Package**
- **Performance Guaranteed Over -55°C to +125°C**
- **MIL-H-38534 Class H**
- **Internal Shield for Higher CMR; Selections Available**
- **1500 Vdc Withstand Test Voltage**
- **High Radiation Immunity**
- **HCPL-2631, -56XX, -66XX Function Compatibility**
- **Reliability Data Available**
- **Space Level Processing Available**
- **Available with TXV or TXVB Part Marking**

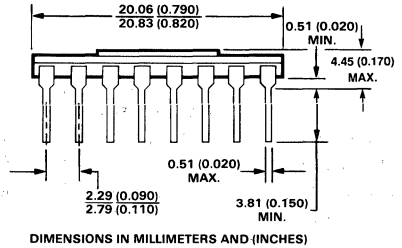
Description

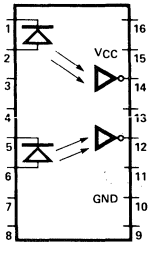
The 6N134, 6N134/883B, and 8102801EC units are hermetically sealed, high CMR, high speed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product (6N134), with full MIL-H-38534 Class Level H testing (6N134/883B) or from the DESC Drawing 81028 as (8102801EX). All three products are dual channel in sixteen pin hermetic dual in-line packages. These parts are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the DESC part #, or by adding option #200 to the part number for 883B marked parts.

Each channel contains a GaAsP light emitting diode which is optically coupled to an integrated high speed photon detector. The output of the detector is an open collector Schottky clamped transistor. Internal shields provide a guaranteed common mode transient immunity specification of 1000 V/μs. Selection for higher CMR values are available by special request.

Outline Drawing







DIMENSIONS IN MILLIMETERS AND (INCHES)

For Gull-wing or Butt-joint lead form options, contact your local Hewlett-Packard field representative.

This unique optocoupler design provides maximum dc and ac circuit isolation between each input and output while achieving TTL circuit compatibility. These optocouplers operate such that a minimum input current of 10 mA in each channel will sink a six gate fanout (10 mA) at the output with 4.5 to 5.5 V V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 55 nsec.

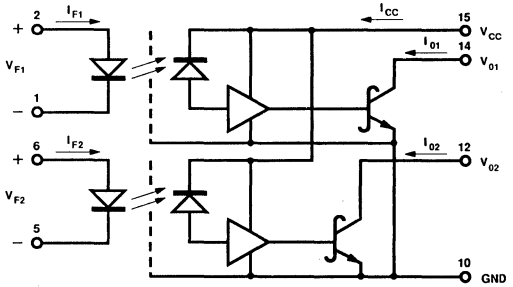
The test program performed on the 8102801EX is in compliance with DESC Drawing 81028. The electrical characteristics table shows Group A Subgroup testing requirements from this drawing.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Applications

- **Military/High Reliability Systems**
- **Transportation and Life Critical Systems**
- **Logic Ground Isolation**
- **Line Receiver**
- **Computer-Peripheral Interface**
- **Vehicle Command/Control Isolation**
- **Harsh Industrial Environments**
- **System Test Equipment Isolation**

Schematic



NOTE:
A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 15 AND 10.

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Temperature (soldering, 10 seconds) ..... +260°C
Junction Temperature (T_J) ..... +175°C
Peak Forward Input Current
(each channel) ..... 40 mA (≤1 ms Duration)
Average Input Forward Current (each channel) ..... 20 mA
Input Power Dissipation (each channel) ..... 35 mW
Reverse Input Voltage (each channel) ..... 5 V
Supply Voltage – V_{CC} ..... 7 V (1 minute max.)
Output Current – I_O (each channel) ..... 25 mA
Output Power Dissipation (each channel) ..... 40 mW
Output Voltage – V_O (each channel) ..... 7 V*
Total Power Dissipation (both channels) ..... 350 mW

*Selection for higher output voltages up to 20 V is available.

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Input Current, Low Level, Each Channel	I_{FL}	0	250	μA
Input Current, High Level, Each Channel	I_{FH}	12.5*	16	mA
Supply Voltage	V_{CC}	4.5	5.5	V
Fan Out (@ R_L = 4 kΩ), Each Channel	N		5	TTL Loads
Operating Temperature	T_A	-55	125	°C

*12.5 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 10 mA or less.

Electrical Specifications

Test	Symbol	Conditions	Group A Sub-groups[11]	Limits			Unit	Fig.	Note
				Min.	Typ.**	Max.			
Low Level Output Voltage	V_{OL}*	V_{CC} = 5.5 V; I_F = 10 mA I_{OL} = 10 mA	1, 2, 3	–	0.4	0.6	V	4	1, 9
Current Transfer Ratio	h_F CTR	V_O = 0.6 V; I_F = 10 mA V_{CC} = 5.5 V	1, 2, 3	100		–	%		1
High Level Output Current	I_{OH}*	V_{CC} = 5.5 V; V_O = 5.5 V I_F = 250 µA	1, 2, 3	–	5	250	µA dc		1
High Level Supply Current	I_{CCH}*	V_{CC} = 5.5 V; I_{F1} = I_{F2} = 0 mA	1, 2, 3	–	18	28	mA dc		
Low Level Supply Current	I_{CCL}*	V_{CC} = 5.5 V; I_{F1} = I_{F2} = 20 mA	1, 2, 3	–	26	36	mA dc		
Input Forward Voltage	V_F*	I_F = 20 mA	1, 2	–	1.55	1.75	V dc	1	1
			3	–		1.85			
Input Reverse Breakdown Voltage	V_{BR}*	I_R = 10 µA	1, 2, 3	5.0		–	V dc		1
Input to Output Insulation Leakage Current	I_{I-O}*	V_{IO} = 1500 V dc Relative Humidity = 45% t = 5 seconds	1	–		1.0	µA dc		2, 10
Capacitance Between Input/Output	C_{I-O}	f = 1 MHz; T_C = 25°C	4	–		4.0	pF		3
Propagation Delay Time, Low to High Output Level	t_{PLH}*	R_L = 510 Ω; C_L = 50 pF I_F = 13 mA	9	–		100	ns	2, 3	1, 5
			10, 11	–		140			
Propagation Delay Time, High to Low Output Level	t_{PHL}*	R_L = 510 Ω; C_L = 50 pF I_F = 13 mA	9	–		100	ns	2, 3	1, 6
			10, 11	–		120			
Output Rise Time	t_{LH}	R_L = 510 Ω C_L = 50 pF; I_F = 13 mA	9, 10, 11	–		90	ns		
Output Fall Time	t_{HL}			–		40			
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	V_{CM} = 50 V (peak); V_O = 2 V minimum; R_L = 510 Ω; I_F = 0 mA	9, 10, 11	1000	10000	–	V µs	6	1, 7, 11, 12
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	V_{CM} = 50 V (peak); V_O = 0.8 V max. R_L = 510 Ω; I_F = 10 mA	9, 10, 11	1000	10000	–	V µs	6	1, 8, 11, 12

*For JEDEC registered parts. **All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Specifications T_A = 25°C), V_{CC} = 5 V each channel

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz		1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.5		mV/°C	I_F = 20 mA		1
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Input-Input Leakage Current	I_{I-I}		0.5		nA	Relative Humidity = 45% V_{I-I} = 500 V, t = 5 s		4
Resistance (Input-Input)	R_{I-I}		10^{12}		Ω	V_{I-I} = 500 V		4
Capacitance (Input-Input)	C_{I-I}		0.55		pF	f = 1 MHz		4
Output Rise Time (10-90%)	t_r		35		ns	R_L = 510 Ω, C_L = 15 pF I_F = 13 mA		1
Output Fall Time (90-10%)	t_f		35		ns			

Notes:

1. Each channel.
2. Measured between pins 1 through 8 shorted together and pins 9 through 16 shorted together.
3. Measured between pins 1 and 2 or 5 and 6 shorted together, and pins 10, 12, 14 and 15 shorted together.
4. Measured between pins 1 and 2 shorted together, and pins 5 and 6 shorted together.
5. The t_{PLH} propagation delay is measured form the 6.5 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. The t_{PHL} propagation delay is measured from the 6.5 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
7. CM_H is the max. tolerable common mode transient to assure that the output will remain in a high logic state (i.e., V_O > 2.0 V).
8. CM_L is the max. tolerable common mode transient to assure that the output will remain in a low logic state (i.e., V_O < 0.8 V).
9. It is essential that a bypass capacitor (0.1 μF, ceramic) be connected from pin 10 to pin 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.
10. This is a momentary withstand test, not an operating condition.
11. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
12. Subgroups 10 and 11 shall be tested as part of device initial characterization and after design and process changes. Subgroups 10 and 11 shall be guaranteed to the limits specified in table I for all lots not specifically tested. Subgroup 9 shall be tested with every lot.

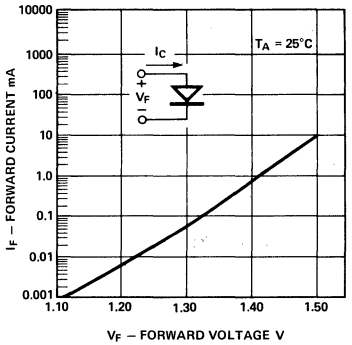


Figure 1. Input Diode Forward Current vs. Forward Voltage

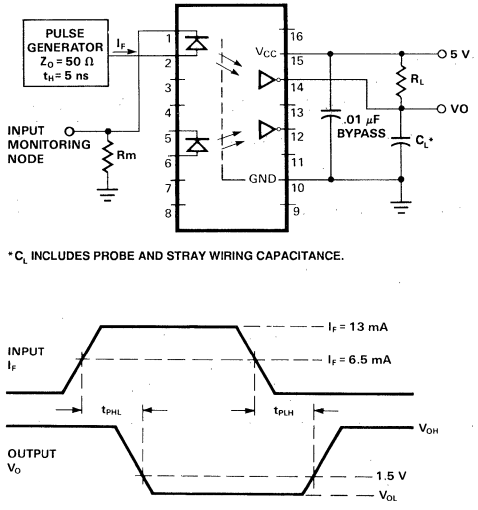


Figure 2. Test Circuit for t_{PHL} and t_{PLH}*

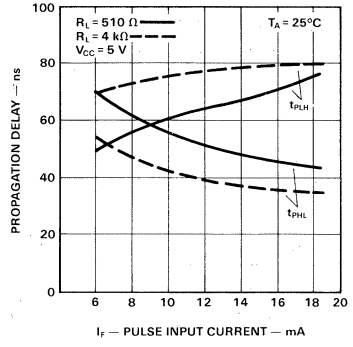
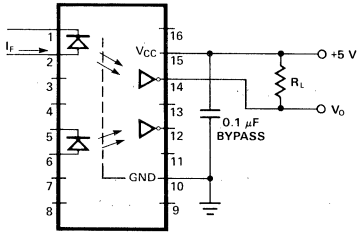


Figure 3. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}



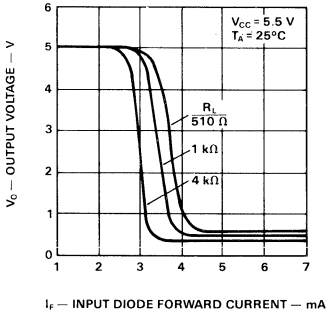


Figure 4. Input-Output Characteristics

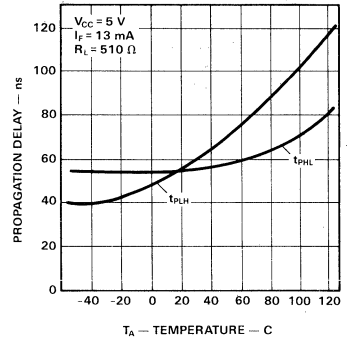


Figure 5. Propagation Delay vs. Temperature

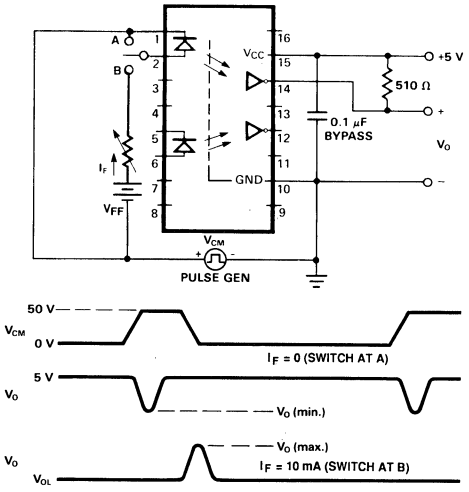


Figure 6. Typical Common Mode Rejection Characteristics/Circuit

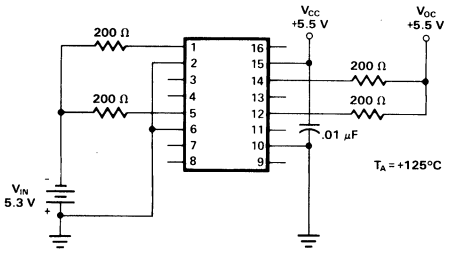


Figure 7. Operating Circuit for Burn-In and Steady State Life Tests

8102801EC and MIL-H-38534 Class H Test Program

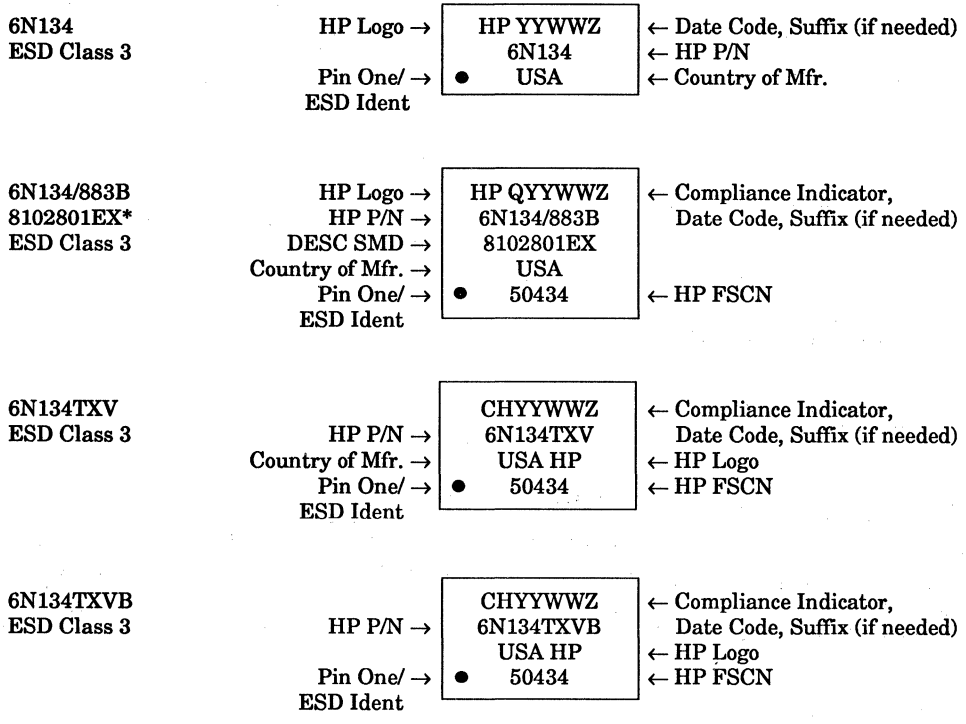
Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-H-38534 and DESC drawing 81028.

Testing consists of 100% screening and quality conformance to MIL-H-38534.

Part Numbering System

Commercial Product	Class H Product	DESC Product	Class K Product
6N134	6N134/883B	8102801EX	TBA

Part Marking Orientation for 6N134 Base Product and Related DESC Product



*"X" is not marked on device. Replace "X" with "C" for gold leads; replace "X" with "A" for solder dipped leads.

HEWLETT PACKARD

High CMR High Speed Hermetically Sealed Optocouplers

Technical Data

HCPL-5600
HCPL-5601 (883B)
5962-9085501HPX
HCPL-5630
HCPL-5631 (883B)
8102802PX
(8-pin Dual In-Line Package)
HCPL-6630
HCPL-6631 (883B)
81028032A
(20 Terminal Leadless Chip Carrier)

Features

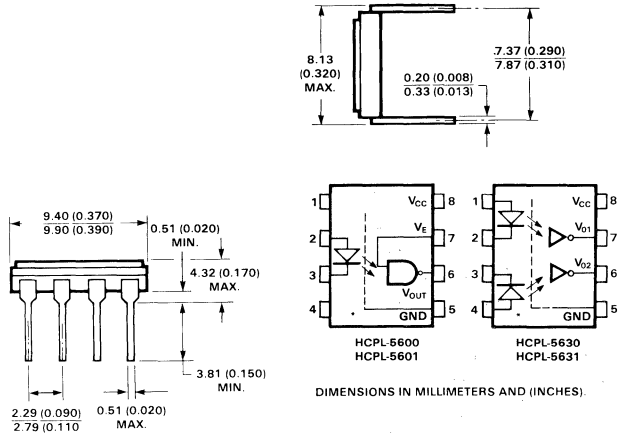
- Dual Marked with DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534, Class H
- Performance Guaranteed Over -55°C to +125°C
- MIL-H-38534 Class H
- High Speed: 10M Bit/s
- Internal Shield for High CMR, Special Selections Available
- Open Collector Outputs
- 1500 Vdc Withstand Test Voltage
- High Radiation Immunity
- 6N134, 6N137, HCPL-2601, HCPL-2630/31 Function Compatibility
- Reliability Data Available

Applications

- Military/High Reliability Systems
- Isolated Input Line Receiver
- Isolated Output Line Driver
- System Test Equipment Isolation
- Digital Logic Ground Isolation
- Computer-Peripheral Interface
- Level Shifting
- Vehicle Command/Control Isolation
- Space Level Processing Available
- Transportation and Life Critical Systems

Outline Drawings

8-pin Ceramic Dual In-Line Package



For Gull-wing or Butt-joint lead form options, contact your local Hewlett-Packard field representative.

Description

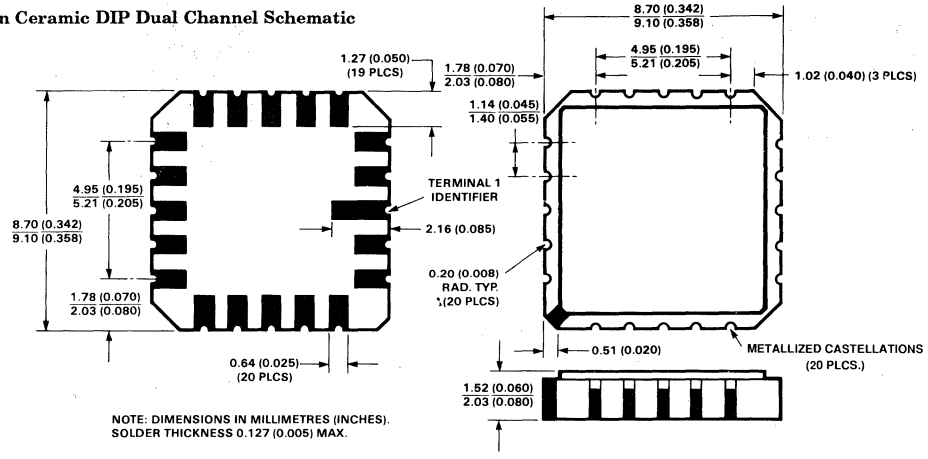
These units are single and dual channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product or with full MIL-H-38534 Class Level H testing. All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

The HCPL-5600, 5601, 5630 and 5631 are in 8 Pin ceramic DIPs configured as either single or dual channel devices. The standard products are HCPL-5600 and HCPL-5630. The products with full MIL-H-38534 Class Level H testing are HCPL-5601 and HCPL-5631.

HERMETIC OPTO COUPLERS

Outline Drawings

8 Pin Ceramic DIP Dual Channel Schematic

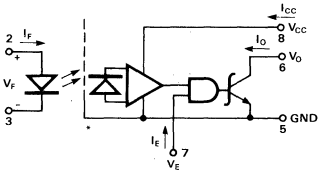


NOTE: DIMENSIONS IN MILLIMETRES (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

The HCPL-6630 and HCPL-6631 parts are in twenty terminal hermetic, ceramic, leadless chip carriers. The standard part is HCPL-6630. The product with full MIL-H-38534 Class Level H testing is HCPL-6631. These dual channel devices are configured and function as two independent single channels. Devices are delivered with solder dipped terminals as a standard feature. Units may also be purchased with gold plated terminals.

Each channel contains a light emitting diode optically coupled to an inverting gate providing 1500 Vdc electrical isolation between input and output. The output of the detector is an open collector schottky clamped transistor. Internal shields provide a guaranteed common mode transient immunity specification of 1000 V/μs at VCM = 50 V. Selection for higher CMR values are available by special request. Contact your local HP field sales engineer for ordering information.

8 Pin Ceramic DIP



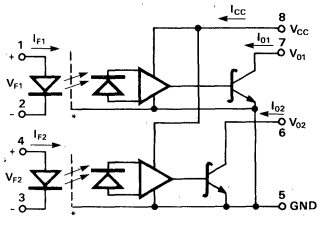
NOTE:
A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5.

SEE NOTE 10.

TRUTH TABLE
(POSITIVE LOGIC)

INPUT	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H

8 Pin Ceramic DIP

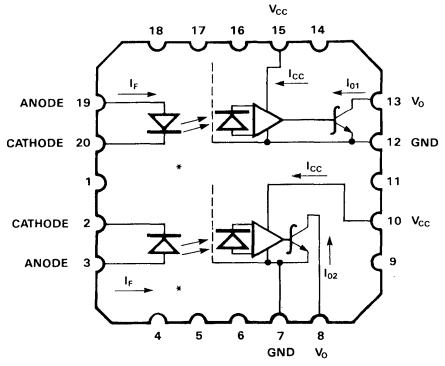


NOTE:
A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5.

This unique design provides maximum D.C. and A.C. circuit isolation while achieving TTL circuit compatibility. The optocoupler operational parameters are guaranteed from -55°C to +125°C, such that a minimum input current of 10 mA per channel will sink a six gate fanout (10 mA) at the output with 4.5 to 5.5 V V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 55 nsec.

External to the unit, a 0.01 μF bypass capacitor must be connected between V_{CC} and ground. A capacitor immediately adjacent to each optocoupler is necessary. The power supply bus for the optocoupler(s) should be separate from the bus for any active loads, otherwise a larger value of the bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.

20 Terminal Ceramic Leadless Chip Carrier Schematic



NOTE:
A .01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN TERMINALS 7 AND 10 AND BETWEEN 12 AND 15.

TRUTH TABLE (POSITIVE LOGIC)

INPUT	OUTPUT
ON	L
OFF	H

*DETECTOR IC INTERNAL ELECTRICAL SHIELD

Recommended Operating Conditions

Parameter	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	12.5†	16	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		6	

Single Channel Product Only (see note 10)

High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V

† 12.5 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 10 mA or less.

Absolute Maximum Ratings

(No derating required up to +125° C)
Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Junction Temperature ..... 175°C
Lead Solder Temperature ..... 260°C for 10s
Peak Foward Input Current
(each channel) ..... 40 mA (≤ 1 ms Duration)
Average Input Foward Current
(each channel) ..... 20 mA
Input Power Dissipation
(each channel) ..... 35 mW
Reverse Input Voltage
(each channel) ..... 5 V
Supply Voltage - V_{CC} .... 7 V (1 minute maximum)
Output Current, I_O (each channel) ..... 25 mA
Output Power Dissipation
(each channel) ..... 40 mW
Output Voltage, V_O (each channel) ..... 7 V
Total Package Power Dissipation ..... 350 mW

Single Channel Product Only
Enable Input Voltage - V_E ..... 5.5 V
ESD Classification HCPL-5600/01 ..... Class 1
HCPL-5630/31 and 6630/31
(MIL-STD-883, Method 3015) ..... Class 3

Electrical Characteristics T_A = -55°C to +125°C, unless otherwise specified

Parameter		Sym.	Test Conditions	Group A Sub-groups[13]	Limits Min.	Limits Typ.*	Limits Max.	Units	Fig.	Note
High Level Output Current		I_{OH}	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 µA	1, 2, 3		20	250	µA	3	1
Low Level Output Voltage		V_{OL}	V_{CC} = 5.5 V, I_F = 10 mA I_{OL} (Sinking) = 10 mA	1, 2, 3		0.3	0.6	V	1	1,9
Logic High Supply Current	Single Channel	I_{CCH}	V_{CC} = 5.5 V, I_F = 0	1, 2, 3		9	14	mA		1
	Dual Channel		V_{CC} = 5.5 V, I_F = 0			18	28	mA		6
Logic Low Supply Current	Single Channel	I_{CCL}	V_{CC} = 5.5 V, I_F = 20 mA;	1, 2, 3		13	18	mA		1
	Dual Channel		V_{CC} = 5.5 V, I_F = 20 mA			26	36	mA		6
Input Forward Voltage		V_F	I_F = 20 mA	1, 2, 3		1.5	1.9	V	2	1
Input Reverse Breakdown Voltage		BV_R	I_R = 10 µA	1, 2, 3	5			V		1
Input-Output Leakage Current		I_{I-O}	V_{I-O} = 1500 Vdc Relative Humidity = 45% T_A = 25°C, t = 5 s	1			1.0	µA		2,8
Propagation Delay Time to High Output Level		t_{PLH}	T_A = 25°C; R_L = 510 Ω, C_L = 50 pF, I_F = 13 mA, V_{CC} = 5 V	9		60	100	ns	4,5	1,5
			-55 to +125°C	10, 11			140			
Propagation Delay Time to Low Output Level		t_{PHL}	T_A = 25°C	9		55	100	ns		
			-55 to +125°C	10, 11			120			
Common Mode Transient Immunity at High Output Level		$\|CM_H\|$	V_{CM} = 50 V (peak), V_{CC} = 5 V T_A = 25°C, V_O (min.) = 2 V, R_L = 510 Ω, I_F = 0 mA	9	1000	>10000		V/µs	8	1, 7
Common Mode Transient Immunity at Low Output Level		$\|CM_L\|$	V_{CM} = 50 V (peak), V_{CC} = 5 V T_A = 25°C, V_O (max.) = 0.8 V, R_L = 510 Ω, I_F = 10 mA	9	1000	>10000		V/µs	8	1, 7

Single Channel Product Only

Low Level Enable Current	I_{EL}	V_{CC} = 5.5 V, V_E = 0.5 V	1, 2, 3		-1.45	-2.0	mA		
High Level Enable Voltage	V_{EH}		1, 2, 3	2.0			V		10
Low Level Enable Voltage	V_{EL}		1, 2, 3			0.8	V		

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics $T_A = 25°C$, $V_{CC} = 5$ V

Parameter	Sym.	Typ.	Units	Test Conditions	Fig.	Note
Input Capacitance	C_{IN}	60	pF	$V_F = 0$, f = 1 MHz		1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	-1.5	mV/°C	$I_F = 20$ mA		1
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	$V_{I-O} = 500$ V		2
Capacitance (Input-Output)	C_{I-O}	1.0	pF	f = 1 MHz		1, 3
Output Rise Time (10-90%)	t_r	35	ns	$R_L = 510\Omega$, $C_L = 50$ pF, $I_F = 13$ mA		1
Output Fall Time (90-10%)	t_f	35	ns			

Single Channel Product Only

Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	35	ns	$R_L = 510\Omega$, $C_L = 50$ pF, $I_F = 13$ mA, $V_{EH} = 3$ V, $V_{EL} = 0$ V	6,7	1,11
Propagation Delay time of Enable from V_{EL} to V_{EH}	t_{EHL}	35	ns		6,7	1,12

Dual Channel Products Only

Input-Input Leakage Current	I_{I-I}	0.5	nA	Relative Humidity = 45% $V_{I-I} = 500$ V, t = 5 s		4
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	$V_{I-I} = 500$ V		4
Capacitance (Input-Input)	C_{I-I}	0.55	pF	f = 1 MHz		4

Notes:

1. Each channel of a dual channel device.
2. Device considered a two-terminal device: for 8 pin DIP, pins 1 through 4 are shorted together, and pins 5 through 8 are shorted together; for LCC, terminals 19, 20, 1, 2, 3 are shorted together, and terminals 7 through 15 are shorted together.
3. Measured between each input pair shorted together and all outputs for that channel shorted together.
4. Measured between adjacent input pairs shorted together; i.e., for 8 pin DIP, between pins 1 and 2 shorted together and pins 3 and 4 shorted together; for LCC, between terminals 19 and 20 shorted together, and terminals 2 and 3 shorted together.
5. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. The HCPL-6630 and HCPL-6631 dual channel parts function as two independent single channel units. Use the single channel parameter limits.
7. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8$ V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0$ V).
8. This is a momentary withstand test, not an operating condition.
9. It is essential that a bypass capacitor (.01 to 0.1μF, ceramic) be connected from V_{CC} to ground. Total lead length between both ends of this external capacitor and the isolator pins should not exceed 20mm.
10. No external pull up is required for a high logic state on the enable input.
11. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
12. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
13. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and 883B parts receive 100% testing at 25, 125 and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

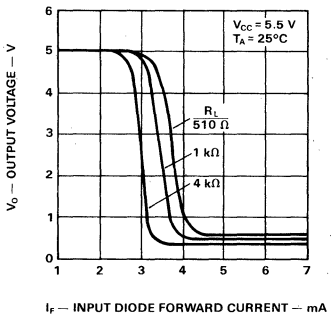


Figure 1. Input-Output Characteristics.

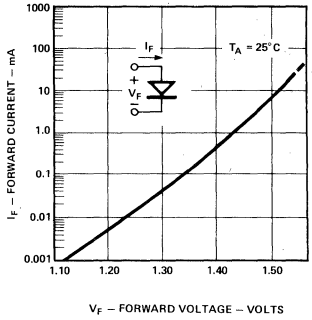


Figure 2. Input Diode Forward Characteristic.

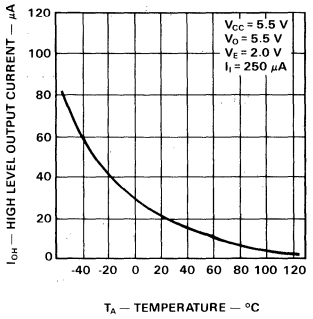


Figure 3. High Level Output Current vs. Temperature.

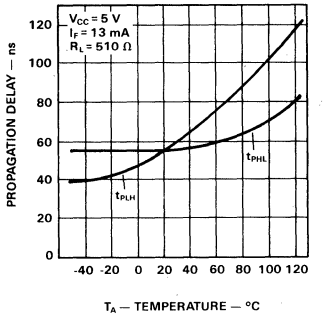
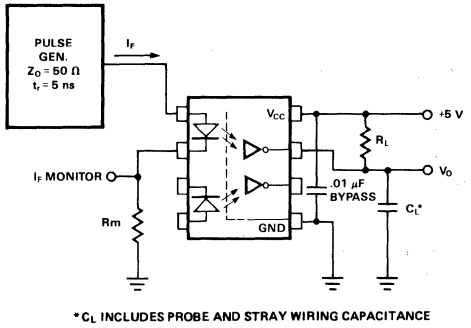


Figure 4. Propagation Delay vs. Temperature.



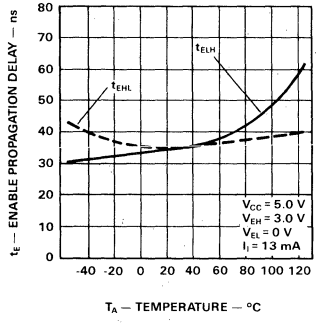


Figure 6. Enable Propagation Delay vs. Temperature.

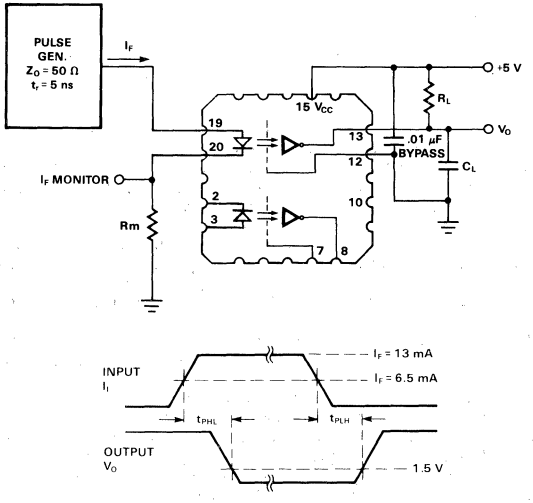
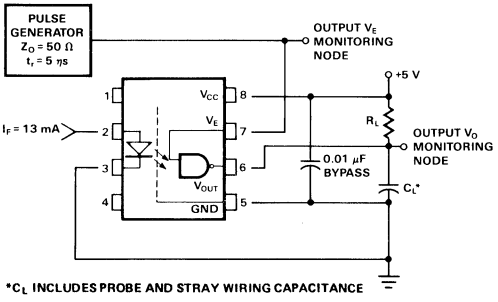


Figure 5. Test Circuit for t_{PHL} and t_{PLH}.



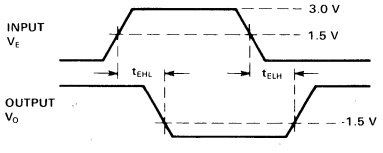


Figure 7. Test Circuit for t_{EHL} and t_{ELH}.

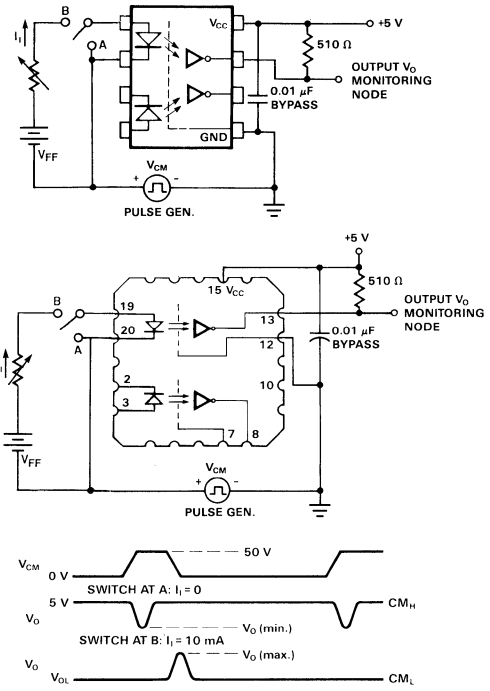


Figure 8. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

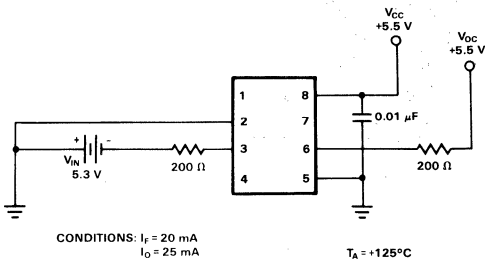


Figure 9. Single Channel Operating Circuit for Burn-In and Steady State Life Tests.

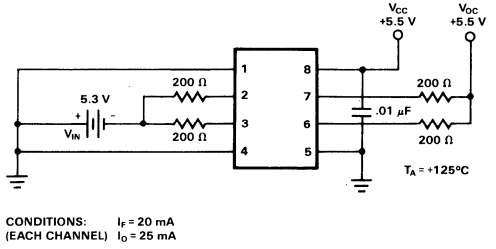


Figure 10. Dual Channel Operating Circuit for Burn-In and Steady-State Life Tests.

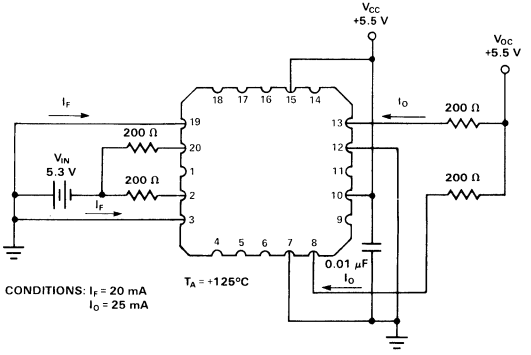


Figure 11. Operating Circuit for Burn-In and Steady State Life Tests.

5962-9085501HPX, 8102802PX, 81028032A, and MIL-H-38534 Class H Test Program

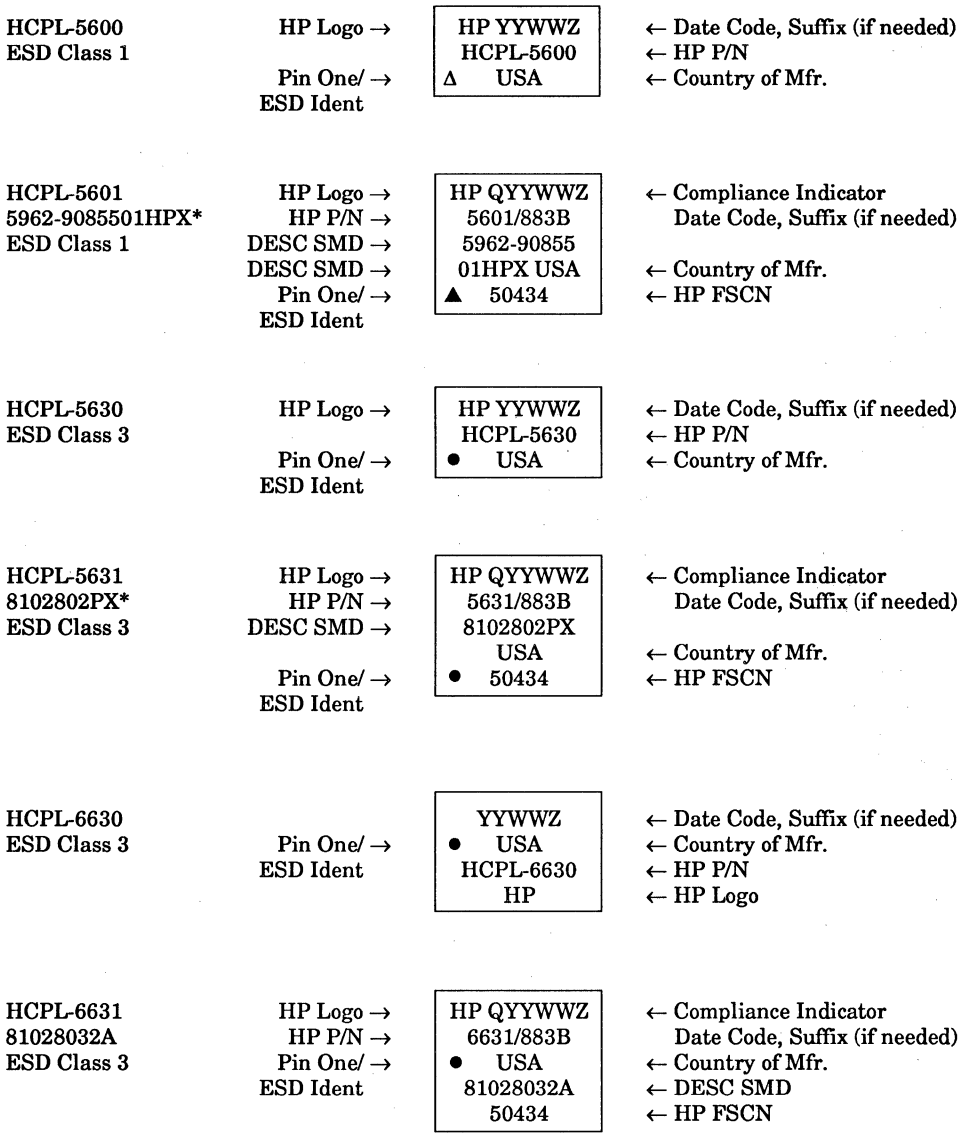
Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-H-38534 and DESC drawings 81028 and 5962-90855.

Testing consists of 100% screening and quality conformance inspection to MIL-H-38534.

Part Numbering System

Commercial Product	Class H Product	DESC Product	Class K Product
HCPL-5600	HCPL-5601	5962-9085501HPX	TBA
HCPL-5630	HCPL-5631	8102802PX	TBA
HCPL-6630	HCPL-6631	81028032A	TBA

Part Marking Orientation for HCPL-56XX and HCPL-663X Base Product and Related DESC Products



*"X" is not marked on device. Replace "X" with "C" for gold lead finish; Replace "X" with "A" for solder lead finish.

HEWLETT PACKARD

Dual Channel Line Receiver Hermetic Optocoupler

Technical Data

HCPL-1930
HCPL-1931 (883B)
5962-8957201EX

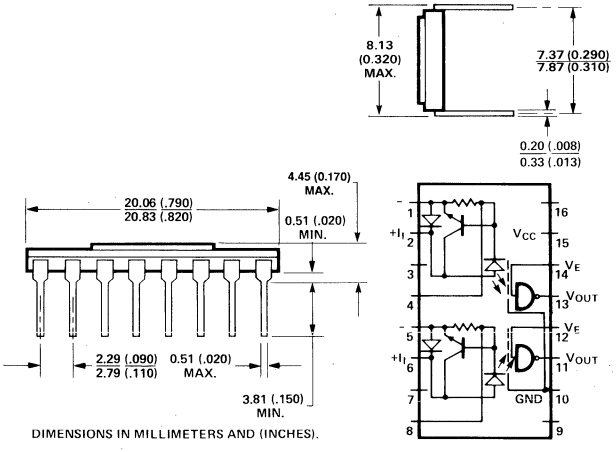
Features

- **Dual Marked with DESC Standard Military Drawing**
- **Manufactured and Tested on a MIL-STD-1772 Certified Line**
- **QML-MIL-H-38534, Class H**
- **Hermetically Sealed 16-pin Dual In-Line Package**
- **Performance Guaranteed Over -55°C to +125°C**
- **MIL-H-38534 Class H**
- **High Speed – 10 Mb/s**
- **Accepts a Broad Range of Drive Conditions**
- **Adaptive Line Termination Included**
- **Internal Shield Provides Excellent Common Mode Rejection**
- **External Base Lead Allows "LED Peaking" and LED Current Adjustment**
- **1500 Vdc Withstand Test Voltage**
- **High Radiation Immunity**
- **HCPL-2602 Function Compatibility**
- **Reliability Data Available**
- **Space Level Processing Available**

Description

The HCPL-1930, HCPL-1931, and 5962-8957201EX units are dual channel, hermetically sealed, high CMR, line receiver optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product (HCPL-1930), with full MIL-H-38534 Class Level H testing (HCPL-1931), or from the DESC Standard Military Drawing (SMD) 5962-89572 as (5962-8957201EX). All three products are sixteen pin hermetic dual in-line packages. They are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in

Outline Drawing



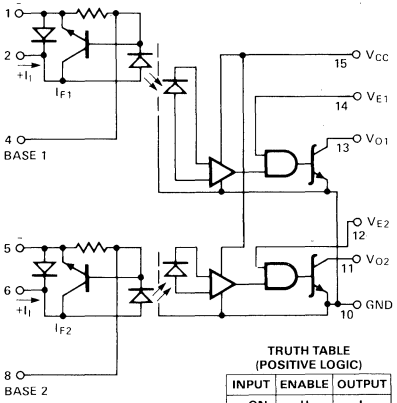
For Gull-wing or Butt-joint lead form options, contact your local Hewlett-Packard field representative.

the SMD part #, or by adding option #200 to the part number for non-DESC parts.

Each unit contains two independent channels, consisting of a GaAsP light emitting diode, an input current regulator, and an integrated high gain photon detector. The input regulator serves as a line termination for line receiver applications. It clamps the line voltage and regulates the LED current so line reflections do not interfere with circuit performance. The regulator allows a typical LED current of 12.5 mA before it starts to shunt excess current. The output of the detector IC is an open collector Schottky clamped transistor. An enable input gates the detector. The internal detector shield provides a guaranteed common mode transient immunity specification of +1000 V/μsec.

DC specifications are compatible with TTL logic and are guaranteed from -55°C to +125°C allowing trouble-free interfacing with digital logic circuits. An input current of 10 mA will sink a six gate fan-out (TTL) at the output with a typical propagation delay from input to output of only 45 nsec.

Schematic



A 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 10 AND 15 (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

INPUT	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H

The test program performed on the 5962-8957201EC is in compliance with DESC (SMD) 5962-89572. The electrical characteristics table shows Group A Subgroup testing requirements from this drawing.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Applications

- **Military/High Reliability Systems**
- **Isolated Line Receiver**
- **Simplex/Multiplex Data Transmission**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Current Sensing**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{IL}	0	250	μA
Input Current, High Level*	I_{IH}	12.5	60	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (@ R_L = 4 kΩ)	N		5	TTL Loads
Operating Temperature	T_A	-55	125	°C

*12.5 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 10 mA or less.

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10 s
1.6 mm below seating plane
Forward Input Current – I_I (each channel) ..... 60 mA[2]
Reverse Input Current ..... 60 mA
Supply Voltage – V_{CC} ..... 7 V 1 Minute Maximum
Enable Input Voltage – V_E (each channel) ..... 5.5 V
Not to exceed V_{CC} by more than 500 mV
Output Collector Current – I_O (each channel) ..... 25 mA
Output Collector Power Dissipation (each channel) ..... 40 mW
Output Collector Voltage – V_O (each channel) ..... 7 V
Total Package Power Dissipation ..... 564 mW
Input Power Dissipation (each channel) ..... 168 mW

Electrical Specifications

Parameter	Symbol	Test Conditions	Group A Sub-groups[15]	Limits			Units	Fig.	Note
				Min.	Typ.*	Max.			
High Level Output Current	I_{OH}	V_{CC} = 5.5 V, V_O = 5.5 V I_I = 250 µA, V_E = 2.0 V	1, 2, 3		20	250	µA	3	3
Low Level Output Voltage	V_{OL}	V_{CC} = 5.5 V; I_I = 10 mA V_E = 2.0 V, I_{OL} (Sinking) = 10 mA	1, 2, 3		0.3	0.6	V	1	3
Input Voltage	V_I	I_I = 10 mA	1, 2, 3		2.2	2.6	V	2	3
		I_I = 60 mA			2.35	2.75			
Input Reverse Voltage	V_R	I_R = 10 mA	1, 2, 3		0.8	1.10	V		3
Low Level Enable Current	I_{EL}	V_{CC} = 5.5 V, V_E = 0.5 V	1, 2, 3		-1.45	-2.0	mA		3
High Level Enable Voltage	V_{EH}		1, 2, 3	2.0			V		3, 12
Low Level Enable Voltage	V_{EL}		1, 2, 3			0.8	V		3
High Level Supply Current	I_{CCH}	V_{CC} = 5.5 V; I_I = 0, V_E = 0.5 V both channels	1, 2, 3		21	28	mA		
Low Level Supply Current	I_{CCL}	V_{CC} = 5.5 V; I_I = 60 mA, V_E = 0.5 V both channels	1, 2, 3		27	36	mA		
Input-Output Insulation Leakage Current	I_{I-O}	Relative Humidity = 45% t = 5 s, V_{I-O} = 1500 Vdc	1			1	µA		4
Propagation Delay Time to High Output Level	t_{PLH}	R_L = 510 Ω; C_L = 50 pF, I_I = 13 mA	9		55	100	ns	4, 5	3, 5
			10, 11			140			
Propagation Delay Time to Low Output Level	t_{PHL}	R_L = 510 Ω; C_L = 50 pF, I_I = 13 mA	9		60	100	ns	4, 5	3, 6
			10, 11			120			
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	V_{CM} = 50 V (peak), V_O (min.) = 2 V, R_L = 510 Ω; I_I = 0 mA	9, 10, 11	1000	10,000		V/µs	8, 9	3, 9, 14
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	V_{CM} = 50 V (peak), V_O (max.) = 0.8 V, R_L = 510 Ω; I_I = 10 mA	9, 10, 11	1000	10,000		V/µs	8, 9	3, 10, 14

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Specifications

$T_A = 25°C$, $V_{CC} = 5$ V

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Note
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	$V_{I-O} = 500$ V dc		3, 13
Capacitance (Input-Output)	C_{I-O}	1.7	pF	f = 1 MHz		3, 13
Input-Input Insulation Leakage Current	I_{I-I}	0.5	nA	45% Relative Humidity, $V_{I-I} = 500$ Vdc, t = 5 s		11
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	$V_{I-I} = 500$ Vdc		11
Capacitance (Input-Input)	C_{I-I}	0.55	pF	f = 1 MHz		11
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	35	ns	$R_L = 510$ Ω, $C_L = 15$ pF, $I_I = 13$ mA, $V_{EH} = 3$ V, $V_{EL} = 0$ V	6, 7	3, 7
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	35	ns		6, 7	3, 8
Output Rise Time (10-90%)	t_r	30	ns	$R_L = 510$ Ω, $C_L = 15$ pF, $I_I = 13$ mA		3
Output Fall Time (90-10%)	t_f	24	ns			3
Input Capacitance	C_I	60	pF	f = 1 MHz, $V_I = 0$, PINS 1 to 2 or 5 to 6		3

Notes:

1. Bypassing of the power supply line is required, with a 0.1 µF ceramic disc capacitor adjacent to each isolator. The power supply bus for the isolators should be separate from the bus for any active loads, otherwise additional bypass capacitance may be needed to suppress regenerative feedback via the power supply.
2. Derate linearly at 1.2 mA/°C above $T_A = 100°C$.
3. Each channel.
4. Device considered a two terminal device: pins 1 through 8 are shorted together, and pins 9 through 16 are shorted together.
5. The t_{PLH} propagation delay is measured form the 6.5 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. The t_{PHL} propagation delay is measured from the 6.5 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
7. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
8. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
9. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state, i.e. $V_{OUT} > 2.0$ V.
10. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state, i.e. $V_{OUT} < 0.8$ V.
11. Measured between adjacent input leads shorted together, i.e. between 1, 2 and 4 shorted together and pins 5, 6 and 8 shorted together.
12. No external pull up is required for a high logic state on the enable input.
13. Measured between pins 1 and 2 or 5 and 6 shorted together, and pins 10 through 15 shorted together.
14. Subgroups 10 and 11 shall be tested as part of device initial characterization and after design and process changes. Subgroup 9 shall be tested with every lot.
15. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and/883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

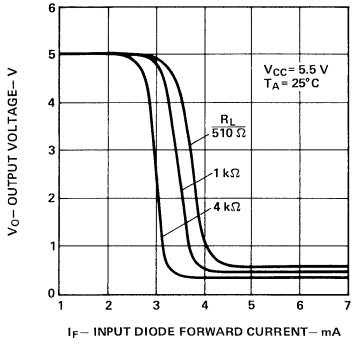


Figure 1. Input-Output Characteristics.

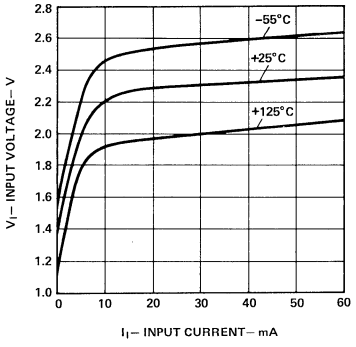


Figure 2. Input Characteristics.

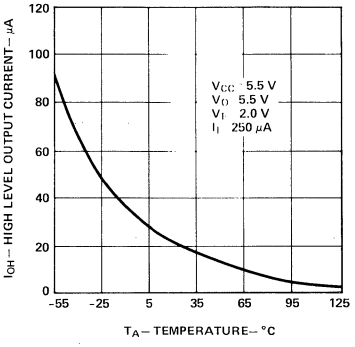


Figure 3. High Level Output Current vs. Temperature.

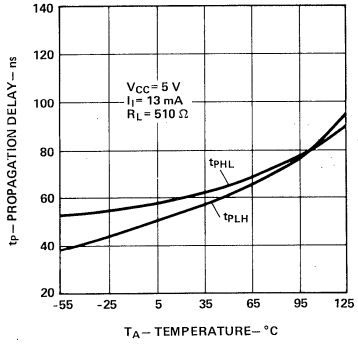


Figure 4. Propagation Delay vs. Temperature.

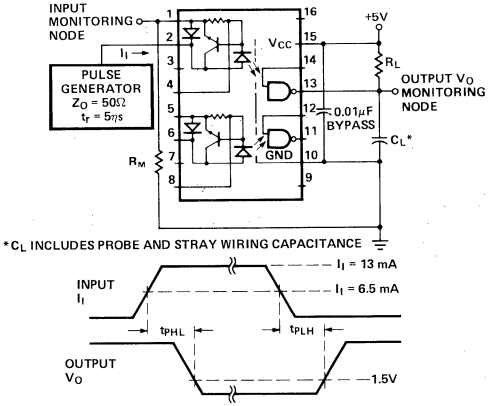


Figure 5. Test Circuit for t_{PHL} and t_{PLH}.

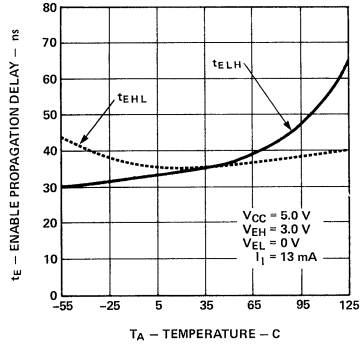


Figure 6. Enable Propagation Delay vs. Temperature.

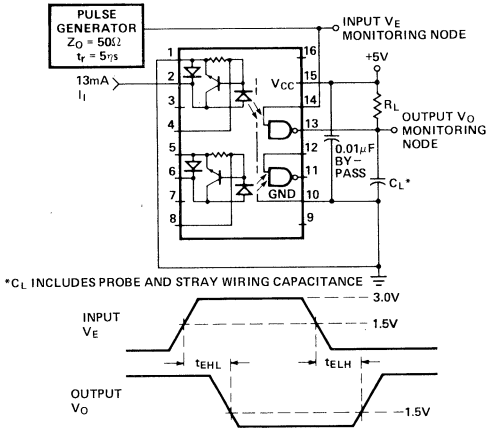


Figure 7. Test Circuit for t_{EHL} and t_{ELH}.

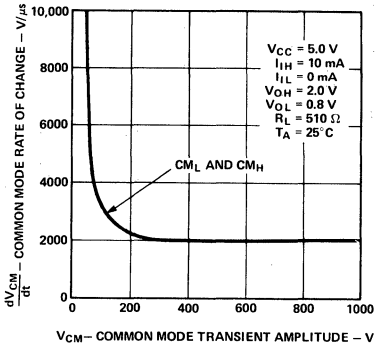


Figure 8. Typical Common Mode Transient Immunity.

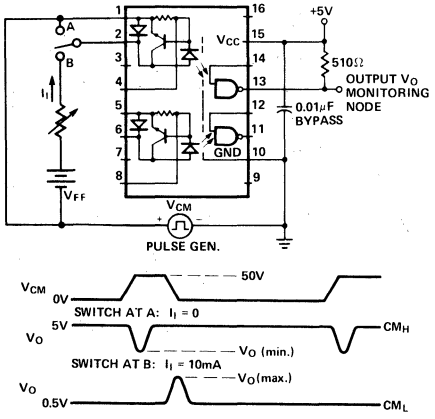


Figure 9. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

5962-8957201EX and MIL-H-38534 Class H Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-H-38534 and DESC SMD 5962-89572.

Testing consists of 100% screening and quality conformance inspection to MIL-H-38534.

Part Numbering System

Commercial Product	Class H Product	DESC Product	Class K Product
HCPL-1930	HCPL-1931	5962-8957201EX	TBA

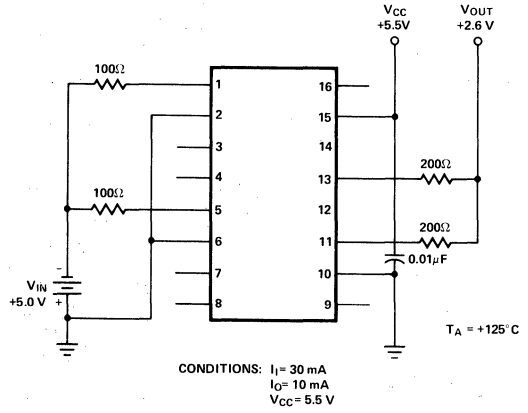
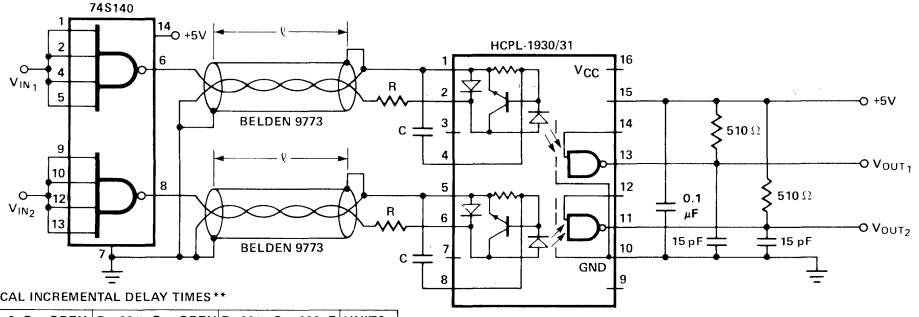


Figure 10. Burn In Circuit.

Application Circuits*

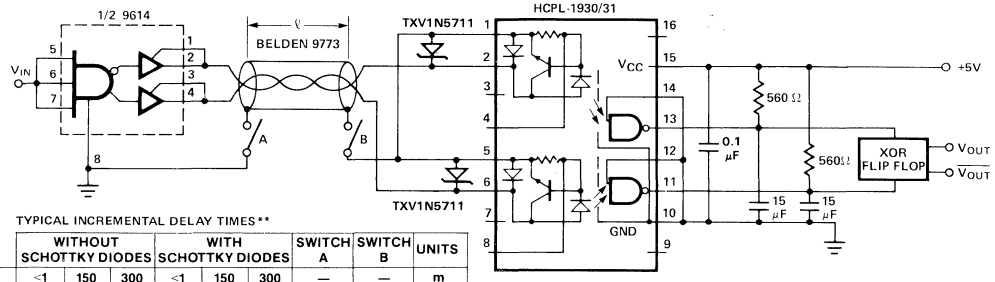


TYPICAL INCREMENTAL DELAY TIMES**

	R = 0, C = OPEN			R =33Ω, C = OPEN			R=33Ω, C = 390pF			UNITS
ℓ	<1	150	300	<1	150	300	<1	150	300	m
t_{PHL}	42	27	121	43	47	171	28	37	146	nsec
t_{PLH}	31	121	296	31	31	71	26	11	46	nsec

PROPAGATION DELAY TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

Figure A_1, Polarity Non-Reversing.

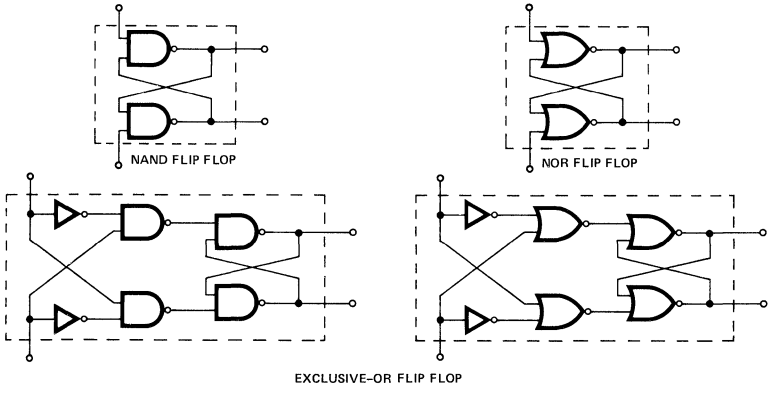


TYPICAL INCREMENTAL DELAY TIMES**

	WITHOUT SCHOTTKY DIODES			WITH SCHOTTKY DIODES			SWITCH A	SWITCH B	UNITS
ℓ	<1	150	300	<1	150	300	—	—	m
tp	112	455	820	78	365	700	OPEN	OPEN	nsec
	52	410	730	54	305	580	OPEN	CLOSED	nsec
	52	410	490	54	395	490	CLOSED	CLOSED	nsec

PROPAGATION DELAY TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS USING 1/3 74LS04 INVERTERS AND 74LS00 QUAD NAND

Figure A_2. Polarity Reversing, Split Phase.

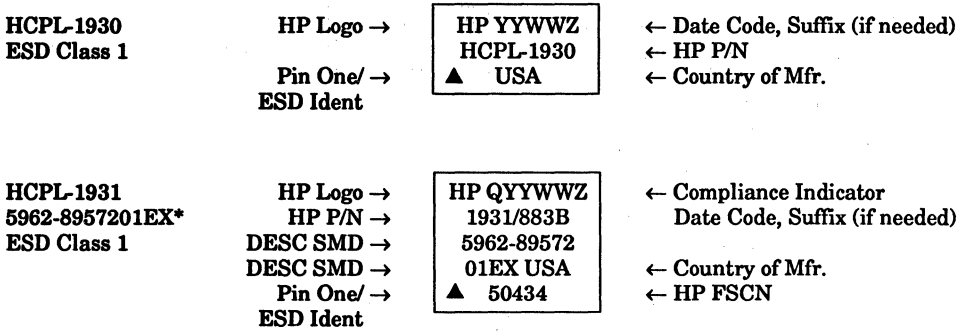


NAND flip flop tolerates simultaneously HIGH inputs; NOR flip flop tolerates simultaneously LOW inputs; EXCLUSIVE-OR flip flop tolerates simultaneously HIGH OR LOW inputs without causing either of the outputs to change.

*FOR A DESCRIPTION OF THESE CIRCUITS SEE HCPL-2602 DATA SHEET.

Figure A_3. Flop-Flop Configurations.

Part Marking Orientation for HCPL-193X Base Product and Related DESC Product



*"X" is not marked on device. Replace "X" with "C" for gold lead finish; Replace "X" with "A" for solder lead finish.

HEWLETT PACKARD

Hermetically Sealed Four Channel Low Input Current Optocoupler

Technical Data

6N140A
6N140A/883B
8302401EX

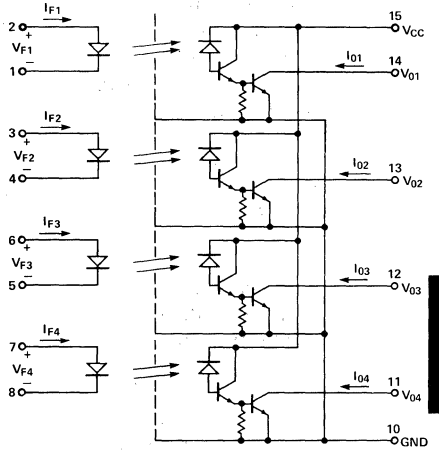
Features

- Dual Marked with DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534, Class H
- Hermetically Sealed 16-Pin Dual In-Line Package
- Performance Guaranteed Over -55°C to +125°C
- MIL-H-38534 Class H
- Internal Shield for Higher CMR
- Low Input Current Requirement: 0.5 mA
- High Current Transfer Ratio: 1500% Typical
- Low Output Saturation Voltage: 0.1 V Typical
- Low Power Consumption
- 1500 VDC Withstand Test Voltage
- High Radiation Immunity
- 6N138/9, HCPL-57XX, 67XX Function Compatibility
- Reliability Data Available
- Available with TXV and TXVB Part Marking

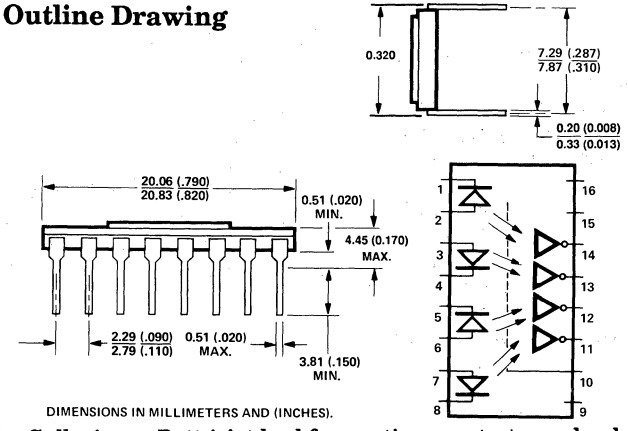
Applications

- Military/High Reliability Systems
- Transportation and Life Critical Systems
- Isolated Input Line Receiver
- Space Level Processing Available
- System Test Equipment Isolation
- Digital Logic Ground Isolation
- EIA RS-232C Line Receiver
- Microprocessor System Interface
- Current Loop Receiver
- Level Shifting
- Process Control Input/ Output Isolation

Schematic



Outline Drawing



DIMENSIONS IN MILLIMETERS AND (INCHES).

For Gull-wing or Butt-joint lead form options, contact your local Hewlett-Packard field representative.

HERMETIC OPTO COUPLERS

Description

The 6N140A is an EIA registered hybrid microcircuit which is capable of operation over the full military temperature range from -55°C to +125°C and is electrically and functionally identical to the 6N140 part. It is an advanced replacement unit for the 6N140. The better performance results from an improved integrated bypass resistor which shunts photodiode and first stage leakage currents. All products within this family have this advanced feature and can be purchased as either a standard product (6N140A), with full MIL-H-38534 Class Level H testing (6N140A/883B) or as parts compliant to DESC Drawing 83024 as (8302401EX). All parts are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the DESC part number, or by adding Option 200 to the part number for non-DESC parts.

All three products are in sixteen-pin hermetic dual in-line packages. Each part contains four GaAsP light emitting diodes, each of which is optically coupled to a corresponding integrated high gain photon detector. The high gain output stage features an open collector output providing both lower output saturation voltage and higher speed operation than possible with conventional photodarlington type optocouplers. Also, the separate V_{CC} pin can be strobed low as an output disable or operated with supply voltages as low as 2.0 V without adversely affecting the parametric performance.

The high current transfer ratio at very low input currents permits circuit designs in which adequate margin can be allowed for the effects of CTR degradation over time.

These products have a 300% minimum CTR at an input current of only 0.5 mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing or RS-232C data transmission systems. Compatibility with high voltage CMOS logic systems is assured by the 18 V V_{CC} and by the guaranteed maximum output leakage (IOH) at 18 V. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor optocouplers.

The test program performed on the 8302401EX is in compliance with DESC Drawing 83024. The electrical characteristics table shows Group A Subgroup testing requirements from this drawing.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Voltage, Low Level (Each Channel)	$V_{F,OFF}$		0.8	V
Input Current, High Level (Each Channel)	$I_{F,ON}$	0.5	5	mA
Supply Voltage	V_{CC}	2.0	18	V

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Output Current, I_O (each channel) ..... 40 mA
Output Voltage, V_O (each channel) ..... -0.5 to 20 V[1]
Supply Voltage, V_{CC} ..... -0.5 to 20 V[1]
Output Power Dissipation (each channel) ..... 50 mW[2]
Peak Input Current (each channel, ≤ 1 ms duration) ..... 20 mA
Average Input Current, I_F (each channel) ..... 10 mA[3]
Reverse Input Voltage, V_R (each channel) ..... 5 V

Electrical Characteristics

Parameter	Sym.	Test Conditions	Group A[14] Sub-groups	Limits Min.	Limits Typ.**	Limits Max.	Unit	Fig.	Note
Current Transfer Ratio	$h_{F(CTR)}$*	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1, 2, 3	300	1500		%	3	4, 5
		I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1, 2, 3	300	1000		%		4, 5
		I_F = 5 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1, 2, 3	200	500		%		4, 5
Logic Low Output Voltage	V_{OL}	I_F = 0.5 mA, I_{OL} = 1.5 mA, V_{CC} = 4.5 V	1, 2, 3		0.1	0.4	V	2	4
		I_F = 5 mA, I_{OL} = 10 mA, V_{CC} = 4.5 V	1, 2, 3		0.2	0.4	V		4
Logic High Output Current	I_{OH}*	I_F = 2 µA, V_O = V_{CC} = 18 V	1, 2, 3		0.001	250	µA		4
	I_{OHX}		1, 2, 3			250	µA		4, 6
Logic Low Supply Current	I_{CCL}*	I_{F1} = I_{F2} = I_{F3} = I_{F4} = 1.6 mA, V_{CC} = 18 V	1, 2, 3		1.7	4	mA		
Logic High Supply Current	I_{CCH}*	I_{F1} = I_{F2} = I_{F3} = I_{F4} = 0 mA, V_{CC} = 18 V	1, 2, 3		0.001	40	µA		
Input Forward Voltage	V_F*	I_F = 1.6 mA	1, 2		1.44	1.7	V	1	4
			3			1.8	V		4
Input Reverse Breakdown Voltage	BV_R*	I_R = 10 µA	1, 2, 3	5			V		4
Input-Output Insulation Leakage Current	I_{I-O}*	45% Relative Humidity, T = 25°C, t = 5 s, V_{I-O} = 1500 VDC	1			1.0	µA		7, 12
Capacitance Between Input-Output	C_{I-O}	f = 1 MHz, T_C = 25°C	4			4	pF		4, 8
Propagation Delay Time To Logic High At Output	t_{PLH}*	I_F = 0.5 mA, R_L = 4.7 kΩ, V_{CC} = 5.0 V	9, 10, 11		6	60	µs	8	4
		I_F = 5 mA, R_L = 680 Ω, V_{CC} = 5.0 V	9		4	20	µs		4
			10, 11			30	µs		4
Propagation Delay Time To Logic Low At Output	t_{PHL}*	I_F = 0.5 mA, R_L = 4.7 kΩ, V_{CC} = 5.0 V	9, 10, 11		30	100	µs	8	4
		I_F = 5 mA, R_L = 680 Ω, V_{CC} = 5.0 V	9		2	5	µs		4
			10, 11			10	µs		4
Common Mode Transient Immunity At Logic High Level Output	$\|CM_H\|$	I_F = 0, R_L = 1.5 kΩ, $\|V_{CM}\|$ = 25 V_{P-P}, V_{CC} = 5.0 V	9, 10, 11	500	1000		V/µs	9	4, 9, 11, 15
Common Mode Transient Immunity At Logic Low Level Output	$\|CM_L\|$	I_F = 1.6 mA, R_L = 1.5 kΩ, $\|V_{CM}\|$ = 25 V_{P-P}, V_{CC} = 5.0 V	9, 10, 11	500	1000		V/µs	9	4, 10, 11, 15

*JEDEC Registered Data.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics

$T_A = 25°C$, $V_{CC} = 5$ V Each Channel

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	$V_{I-O} = 500$ VDC, $T_A = 25°C$		4, 8
Input-Input Insulation Leakage Current	I_{I-I}		0.5		nA	45% Relative Humidity, $V_{I-I} = 500$ VDC $T_A = 25°C$, t = 5 s		13
Resistance (Input-Input)	R_{I-I}		10^{12}		Ω	$V_{I-I} = 500$ VDC, $T_A = 25°C$		13
Capacitance (Input-Input)	C_{I-I}		1		pF	f = 1 MHz, $T_A = 25°C$		13
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$		-1.8		mV/°C	$I_F = 1.6$ mA		4
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, $V_F = 0$, $T_A = 25°C$		4

Notes:

1. Pin 10 should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0 volts, will provide lowest total I_{OH} over temperature.
2. Output power is collector output power plus one fourth of total supply power. Derate at 1.66 mW/°C above 110°C.
3. Derate I_F at 0.33 mA/°C above 110°C.
4. Each channel.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. I_{OHX} is the leakage current resulting from channel to channel optical crosstalk. $I_F = 2$ μA for channel under test. For all other channels, $I_F = 10$ mA.
7. Device considered a two-terminal device: Pins 1 through 8 are shorted together and pins 9 through 16 are shorted together.
8. Measured between the LED anode and cathode shorted together and pins 10 through 15 shorted together.
9. CM_H is the maximum tolerable common mode transient to assure that the output will remain in a high logic state (i.e., $V_O >$ 2.0 V).
10. CM_L is the maximum tolerable common mode transient to assure that the output will remain in a low logic state (i.e., $V_O <$ 0.8 V).
11. In applications where dV/dt may exceed 50,000 V μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector ICs from destructively high surge currents. The recommended value is

$$R_{CC} \approx \frac{1\text{ V}}{0.6\ I_F\text{ (mA)}}\ \text{k}\Omega$$

12. This is a momentary withstand test, not an operating condition.
13. Measured between adjacent input pairs shorted together, i.e., between pins 1 and 2 shorted together, and pins 3 and 4 shorted together, etc.
14. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
15. Subgroups 10 and 11 shall be tested as part of device initial characterization and after design and process changes. Subgroups 10 and 11 shall be guaranteed to the limits specified in Table I for all lots not specifically tested. Subgroup 9 shall be tested with every lot.

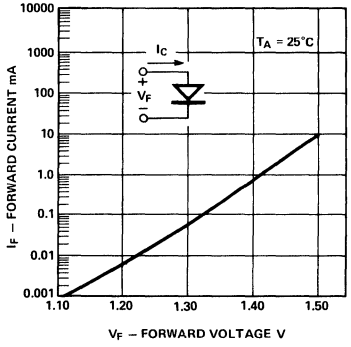


Figure 1. Input Diode Forward Current vs Forward Voltage.

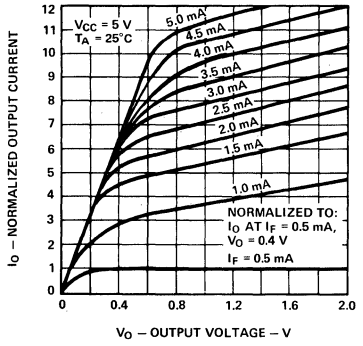


Figure 2. Normalized DC Transfer Characteristics.

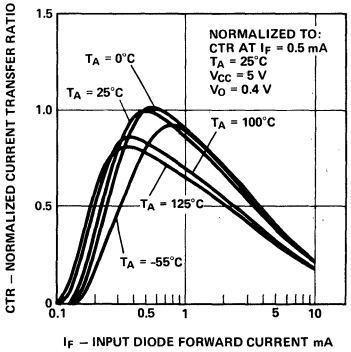


Figure 3. Normalized Current Transfer Ratio vs Input Diode Forward Current.

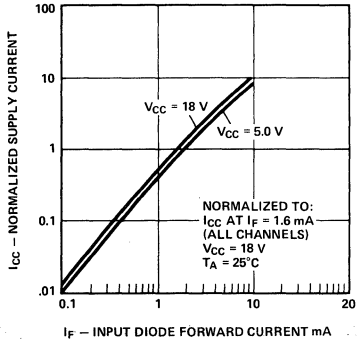


Figure 4. Normalized Supply Current vs Input Diode Forward Current.

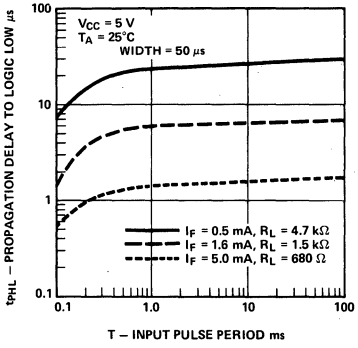


Figure 5. Propagation Delay to Logic Low vs Input Pulse Period.

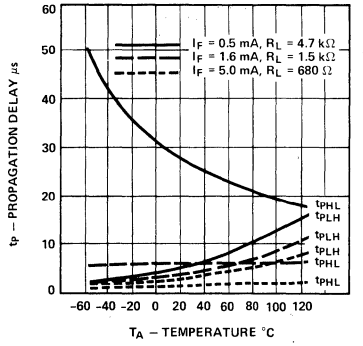


Figure 6. Propagation Delay vs Temperature.

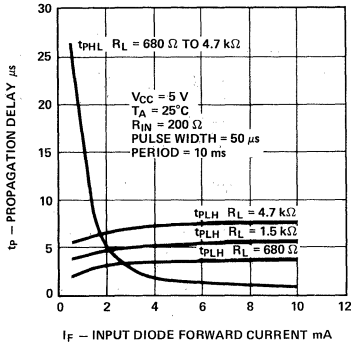


Figure 7. Propagation Delay vs Input Diode Forward Current.

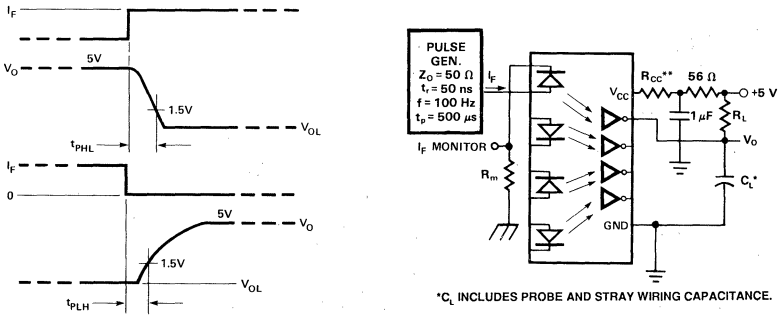


Figure 8. Switching Test Circuit (f, t_p not JEDEC registered).*

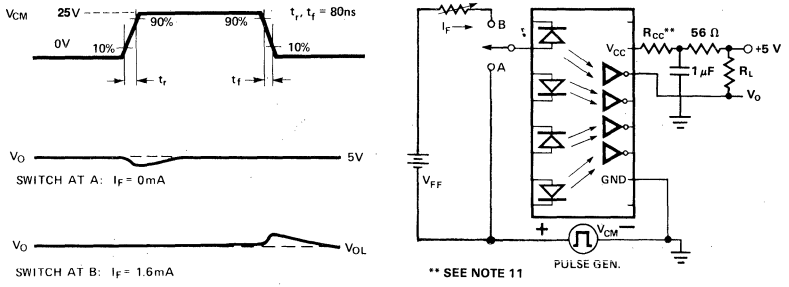


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

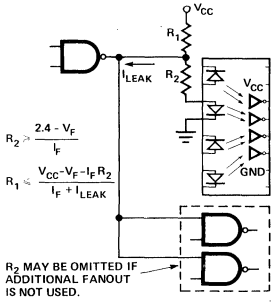


Figure 10. Recommended Drive Circuitry Using TTL Open-Collector Logic.

8302401EX and MIL-H-38534 Class H Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-H-38534 and DESC drawing 83024.

Testing consists of 100% screening and quality conformance inspection to MIL-H-38534.

Part Numbering System

Commercial Product	Class H Product	DESC Product	Class K Product
6N140A	6N140A/883B	8302401EX	TBD

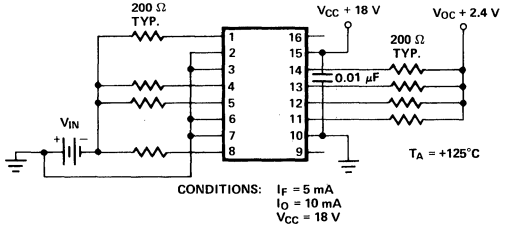
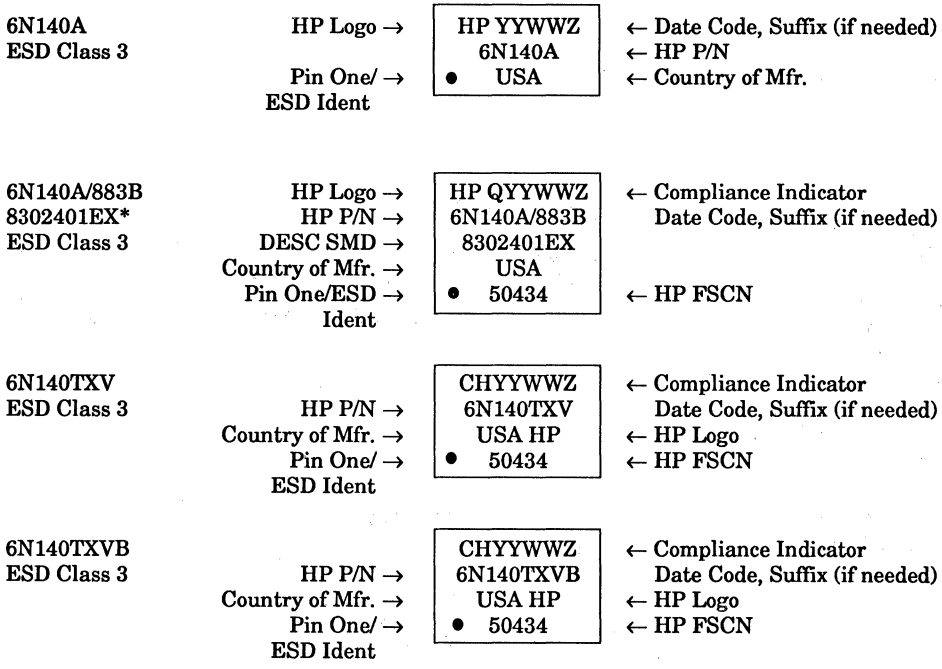


Figure 11. Operating Circuit for Burn-In and Steady State Life Tests.

Part Marking Orientation for 6N140A Base Product and Related DESC Product.



*"X" is not marked on device. Replace "X" with "C" for gold lead finish; Replace "X" with "A" for solder lead finish.

HEWLETT PACKARD

Low Input Current, High Gain, Hermetically Sealed Optocoupler

Technical Data

8-pin Dual In-Line Package
HCPL-5700
HCPL-5701 (883B)
5962-8981001PX
HCPL-5730
HCPL-5731 (883B)
5962-8978501PX
20 Terminal Leadless Chip Carrier
HCPL-6730
HCPL-6731 (883B)
5962-89785022A

Features

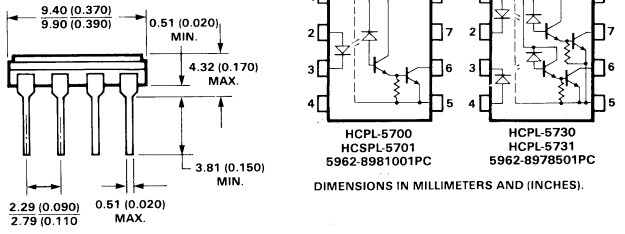
- Dual Marked with DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534, Class H
- Hermetically Sealed
- Performance Guaranteed Over -55°C to +125°C
- MIL-H-38534 Class H
- Low Input Current Requirement: 0.5 mA
- High Current Transfer Ratio: 1500% Typical
- Low Output Saturation Voltage: 0.11 V Typical
- 1500 Vdc Withstand Test Voltage
- Low Power Consumption
- High Radiation Immunity
- Function Compatibility with 6N138/9, HCPL-2730/31, and 6N140A
- 2-18 Volt V_{CC} Range
- Reliability Data Available

Applications

- Military/High Reliability Systems
- Telephone Ring Detection
- Microprocessor System Interface
- EIA RS-232-C Line Receiver
- Level Shifting
- Space Level Processing Available
- Transportation and Life Critical Systems
- Digital Logic Ground Isolation
- Current Loop Receiver
- Isolated Input Line Receiver
- System Test Equipment Isolation
- Process Control Input/Output Isolation

Outline Drawings

8-PIN CERAMIC DUAL IN-LINE PACKAGE

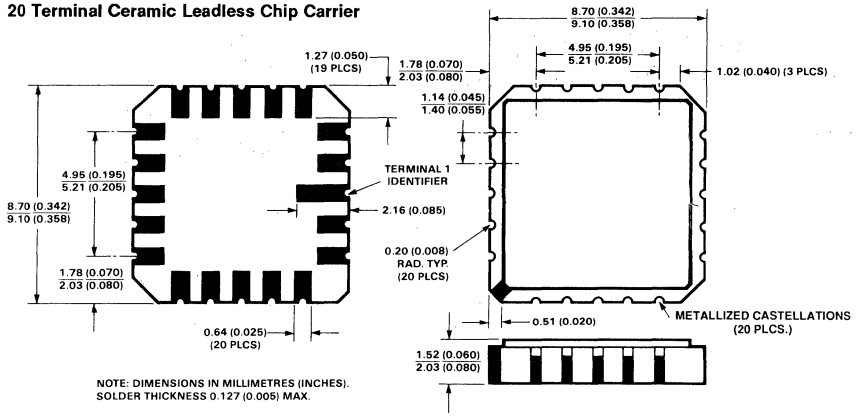


DIMENSIONS IN MILLIMETERS AND (INCHES).

For Gull-wing or Butt-joint lead form options, contact your local Hewlett-Packard field representative.

HERMETIC OPTO COUPLERS

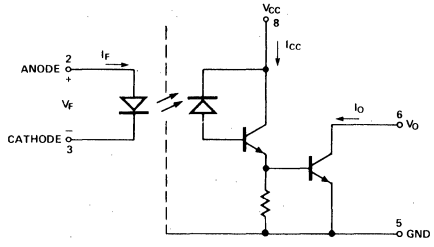
20 Terminal Ceramic Leadless Chip Carrier



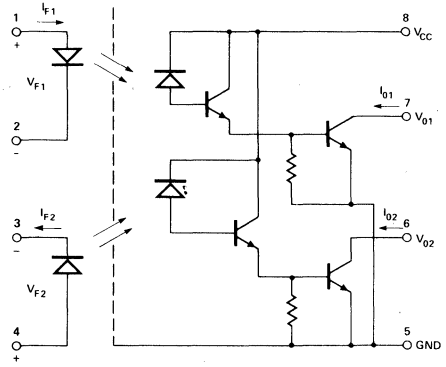
NOTE: DIMENSIONS IN MILLIMETRES (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

Description

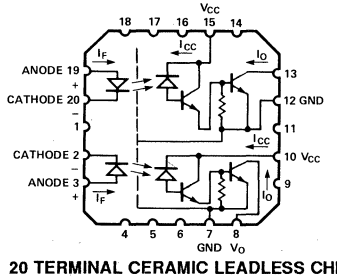
These products are 8 pin and 16 pin versions of the 6N140A family (see separate data sheet). The HCPL-5700, HCPL-5701, and 5962-8981001PX are single channel, low input current, high gain optocouplers. The HCPL-5730, HCPL-5731 and 5962-8978501PX are dual channel units made from the same chip sets. All six products are in eight pin hermetic dual in-line packages. These units are capable of operation and storage over the full military temperature ranges and can be purchased as either single or dual channel standard product (HCPL-5700 and HCPL-5730 respectively), with full MIL-H-38534 Class Level H testing (HCPL-5701 and HCPL-5731 respectively), or from the DESC Standard Military Drawings (SMDs) 5962-89810 and 5962-89785 as (5962-8981001PX or 5962-8978501PX respectively). Parts are shipped with gold plated or solder dipped leads. To order replace C for gold with A for solder dipped in the SMD part number, or add Option 200 to the part number for non-SMD parts.



8 PIN CERAMIC DIP SINGLE CHANNEL SCHEMATIC



8 PIN CERAMIC DIP DUAL CHANNEL SCHEMATIC



20 TERMINAL CERAMIC LEADLESS CHIP CARRIER SCHEMATIC

The HCPL-6730, HCPL-6731, and 8962-89785022A are dual channel parts in twenty terminal hermetic, ceramic, leadless chip carriers. The standard part is HCPL-6730. The product with full MIL-H-38534 Class Level H testing is HCPL-6731. The DESC SMD part is 5962-89785022A. All three products are configured and function as two independent single channels. Devices are delivered with solder dipped terminals as a standard feature. Units may also be purchased with gold plated terminals.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Each channel contains a GaAsP light emitting diode optically coupled to an integrated high gain photon detector. The high gain output stage features an open collector output providing both lower saturation voltage and higher signaling speed than possible with conventional photo-Darlington optocouplers.

The supply voltage can be operated as low as 2.0 V without adversely affecting the parametric performance.

These devices have a 300% minimum CTR at an input current of only 0.5 mA making them ideal for use in low input current applications such as MOS, CMOS, low power logic interfaces or line receivers.

Compatibility with high voltage CMOS logic systems is assured by the 18V VCC, VOH current and the guaranteed maximum output leakage current at 18 V. The shallow depth and small junctions offered by the IC process provides better radiation immunity than conventional phototransistor optocouplers.

Upon special request, the following device selections can be made: CTR minimum of up to 600% at 0.5 mA, lower drive currents to 0.1 mA, and lower output leakage current levels to 100 μA.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Voltage, Low Level (Each Channel)	$V_{F,OFF}$		0.8	V
Input Current, High Level (Each Channel)	$I_{F,ON}$	0.5	5	mA
Supply Voltage	V_{CC}	2.0	18	V

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10 s
Output Current, I_O (each channel) ..... 40 mA
Output Voltage, V_O (each channel) ..... -0.5 to 20 V[1]
Supply Voltage ,V_{CC} ..... -0.5 to 20 V[1]
Output Power Dissipation (each channel) ..... 50 mW[2]
Peak Input Current (each channel, ≤ 1 ms duration) ..... 20 mA
Average Input Current, I_F (each channel) ..... 10 mA[3]
Reverse Input Voltage, V_R (each channel) ..... 5 V

Electrical Characteristics T_A = -55°C to +125°C, unless otherwise specified

Parameter		Sym.	Test Conditions	Group A[14] Subgroups	Min.	Typ.*	Max.	Units	Fig.	Notes
Current Transfer Ratio		CTR	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1, 2, 3	300	1500		%	3	4, 5
			I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V		300	1000				
			I_F = 5 mA, V_O = 0.4 V, V_{CC} = 4.5 V		200	500				
Logic Low Output Voltage		V_{OL}	I_F = 0.5 mA, I_O = 1.5 mA, V_{CC} = 4.5 V	1, 2, 3		0.11	0.4	V	2	4
			I_F = 1.6 mA, I_O = 4.8 mA, V_{CC} = 4.5 V			0.13	0.4			
			I_F = 5.0 mA, I_O = 10 mA, V_{CC} = 4.5 V			0.16	0.4			
Logic High Output Current		I_{OHX}	I_F = 2 µA (Channel Under Test) I_F = 10 mA (Other Channel) V_O = V_{CC} = 18 V	1, 2, 3		0.001	250	µA		6
		I_{OH}								
Logic Low Supply Current	Single Channel and LCC	I_{CCL}	I_F = 1.6 mA, V_{CC} = 18 V	1, 2, 3		1.0	2	mA		
	Dual Channel		I_{F1} = I_{F2} = 1.6 mA, V_{CC} = 18 V				4		4	16
Logic High Supply Current	Single Channel and LCC	I_{CCH}	I_F = 0, V_{CC} = 18 V	1, 2, 3		0.001	20	µA		
	Dual Channel		I_{F1} = I_{F2} = 0, V_{CC} = 18 V				40			16
Input Forward Voltage	8 Pin DIP Devices	V_F	I_F = 1.6 mA	1	1.0	1.44	1.7	V	1	4
				2			1.7			
				3			1.8			
	20 Terminal Devices			1, 2, 3	1.0		1.8			
Input Reverse Breakdown Voltage		BV_R	I_R = 10 µA	1, 2, 3	5			V		4
Input-Output Insulation Leakage Current		I_{I-O}	45% Relative Humidity, t = 5 s, V_{I-O} = 1500 Vdc	1			1.0	µA		7, 13

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Electrical Characteristics (continued)

Parameter	Sym.	Test Conditions	Group A[14] Subgroups	Min.	Typ.*	Max.	Units	Fig.	Notes
Propagation Delay Time to Logic High at Output	t_{PLH}	I_F = 0.5 mA, R_L = 4.7 kΩ, V_{CC} = 5 V	9, 10, 11		17	60	µs	7, 8	4
		I_F = 1.6 mA, R_L = 1.5 kΩ, V_{CC} = 5 V			14	50			
		I_F = 5.0 mA, R_L = 680 Ω, V_{CC} = 5 V			8	30			
Propagation Delay Time to Logic Low at Output	t_{PHL}	I_F = 0.5 mA, R_L = 4.7 kΩ, V_{CC} = 5 V	9, 10, 11		10	100	µs	7, 8	4
		I_F = 1.6 mA, R_L = 1.5 kΩ, V_{CC} = 5 V			5	30			
		I_F = 5.0 mA, R_L = 680 Ω, V_{CC} = 5 V			2	10			
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	I_F = 0, R_L = 1.5 kΩ $\|V_{CM}\|$ = 50 V_{P-P}, V_{CC} = 5.0 V	9, 10, 11	500	≥2000		V/µs	9	4, 10, 12, 15
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	I_F = 1.6 mA, R_L = 1.5 kΩ $\|V_{CM}\|$ = 50 V_{P-P}, V_{CC} = 5.0 V	9, 10, 11	500	≥1000		V/µs	9	4, 11, 12, 15

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics

T_A = 25°C, V_{CC} = 5 V

Parameter	Symbol	Typical	Units	Test Conditions	Figure	Note
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 Vdc		4, 8
Capacitance (Input-Input)	C_{I-O}	2.0	pF	f = 1 MHz		4, 8
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	-1.8	mV/°C	I_F = 1.6 mA		4
Input Capacitance	C_{IN}	60	pF	f = 1 MHz, V_F = 0		4

Dual Channel Product Only

Input-Output Insulation Leakage Current	I_{I-I}	0.5	nA	45% Relative Humidity, V_{I-I} = 500 Vdc T_A = 25°C, t = 5 s		9
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	V_{I-I} = 500 Vdc		9
Capacitance (Input-Input)	C_{I-I}	1.0	pF	f = 1 MHz		9

Notes:

1. GND Pin should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0 V, will provide lowest total I_{OH} over temperature.
2. Output power is collector output power plus total supply power for the single channel device. For the dual channel device, output power is collector output power plus one half the total supply power. Derate at 1.66 mW/°C above 110°C.
3. Derate I_F at 0.33 mA/°C above 110°C.
4. Each channel.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. I_{OHX} is the leakage current resulting from channel to channel optical crosstalk. I_F = 2 μA for channel under test. For all other channels, I_F = 10 mA.
7. Device considered a two-terminal device: For 8 pin DIP, pins 1 through 4 are shorted together, and pins 5 through 8 are shorted together; for LCC, terminals 19, 20, 1, 2, 3 are shorted together, and terminals 7 through 15 are shorted together.
8. Measured between each input pair shorted together, and all outputs for that channel shorted together.
9. Measured between adjacent input pairs shorted together; i.e., for 8 pin DIP, between pins 1 and 2 shorted together and pins 3 and 4 shorted together; for LCC, between terminals 19 and 20 shorted together, and terminals 2 and 3 shorted together.
10. CM_H is the maximum tolerable common mode transient to assure that the output will remain in a high logic state (i.e., $V_O >$ 2.0 V).
11. CM_L is the maximum tolerable common mode transient to assure that the output will remain in a low logic state (i.e., $V_O <$ 0.8 V).
12. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector ICs from destructively high surge currents. The recommended value is

$$R_{CC} \approx \frac{1\ V}{0.15\ I_F\ (mA)}\ k\Omega$$

for single channel;

$$R_{CC} \approx \frac{1\ V}{0.3\ I_F\ (mA)}\ k\Omega$$

for dual channel.

13. This is a momentary withstand test, not an operating condition.
14. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
15. Subgroups 10 and 11 shall be tested as part of device initial characterization and after design and process changes. Subgroups 10 and 11 shall be guaranteed to the limits specified in Table I for all lots not specifically tested. Subgroup 9 shall be tested with every lot.
16. The HCPL-6730 and HCPL-6731 dual channel parts function as two independent single channel units. Use the single channel parameter limits.

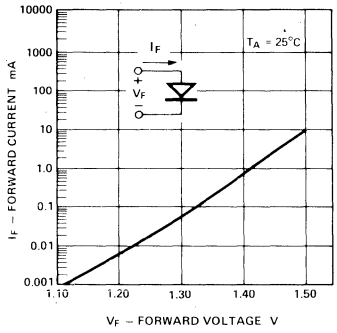


Figure 1. Input Diode Forward Current vs. Forward Voltage.

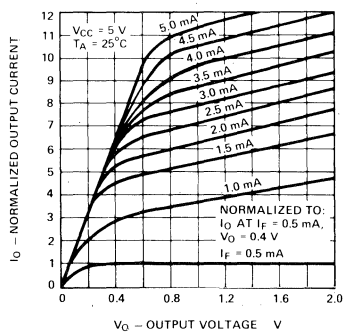


Figure 2. Normalized DC Transfer Characteristics.

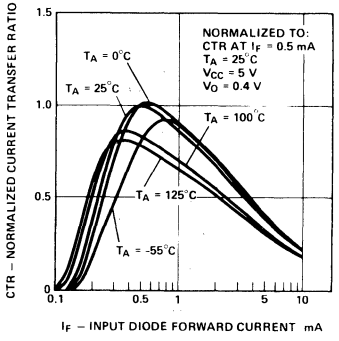


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

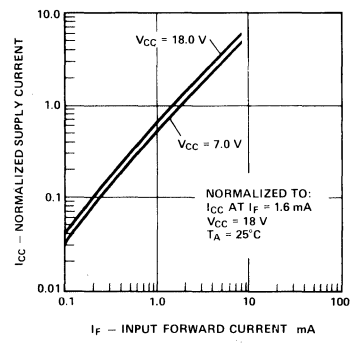


Figure 4. Normalized Supply Current vs. Input Diode Forward Current.

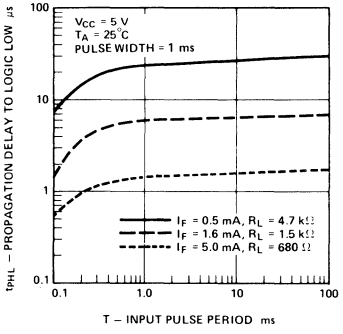


Figure 5. Propagation Delay to Logic Low vs. Input Pulse Period.

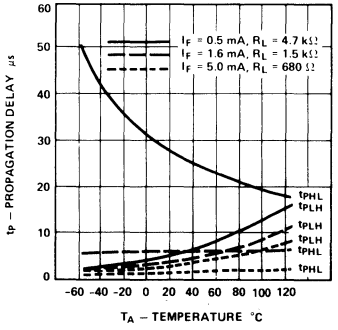


Figure 6. Propagation Delay vs. Temperature.

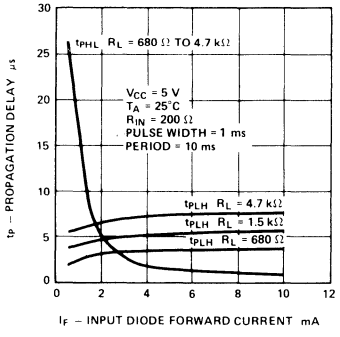


Figure 7. Propagation Delay vs. Input Diode Forward Current.

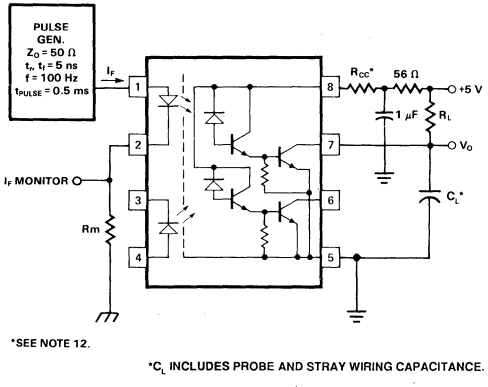
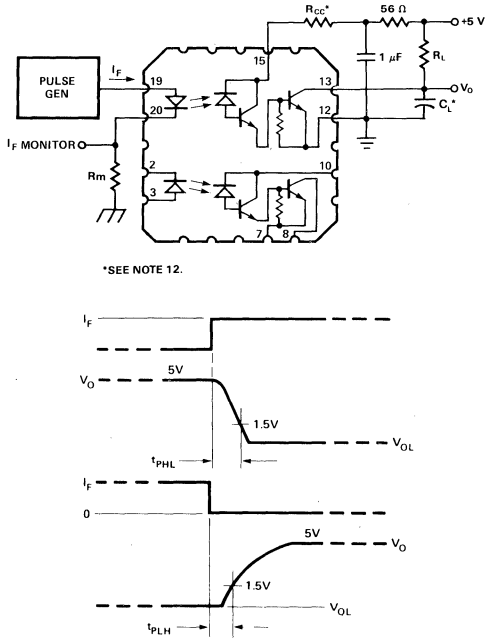
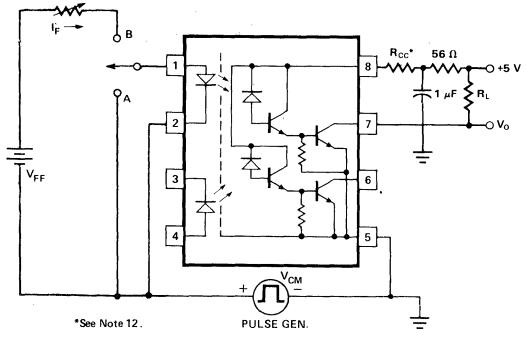
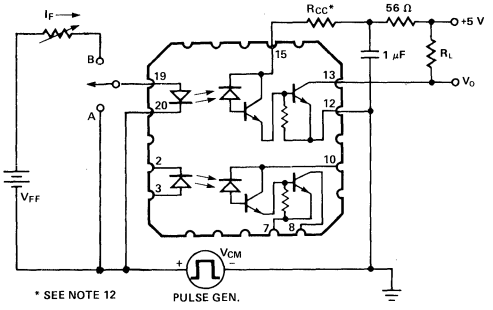


Figure 8. Switching Test Circuit.







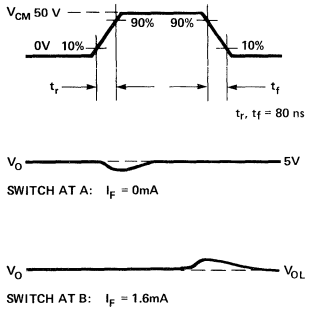


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

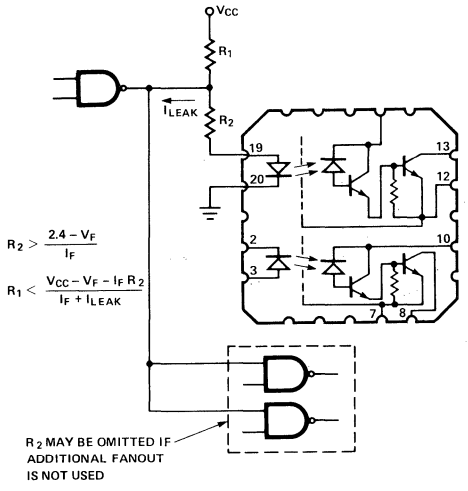


Figure 10. Recommended Drive Circuitry Using TTL Open-Collector Logic.

5962-8981001PX 5962-8978501PX 5962-89785022A and MIL-H-38534 Class H Test Programs

Hewlett-Packard's 883B Optocouplers are in compliance with MIL-H-38534 and DESC SMDs 5962-89810 and 5962-89785.

Testing consists of 100% screening and quality conformance inspection to MIL-H-38534.

Part Numbering System

Commercial Product	Class H Product	DESC Product	Class K Product
HCPL-5700	HCPL-5701	5962-8981001PX	TBD
HCPL-5730	HCPL-5731	5962-8978501PX	TBD
HCPL-6730	HCPL-6731	5962-89785022A	TBD

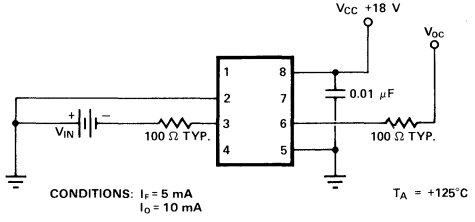


Figure 11. Single Channel Operating Circuit for Burn-In and Steady State Life Tests.

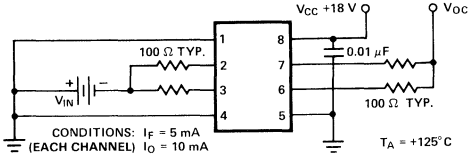


Figure 12. Dual Channel Operating Circuit for Burn-in and Steady State Life Tests.

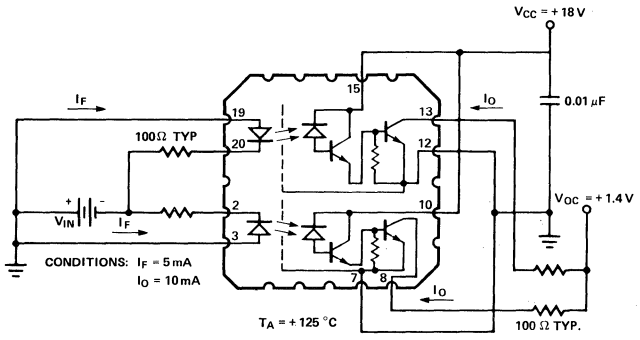


Figure 13. Operating Circuit for Burn-in and Steady State Life Tests.

Part Marking Orientation for HCPL-57XX and HCPL-673X Base Product and Related DESC Products

HCPL-5700
ESD Class 2

HP Logo →
HP P/N →
Pin One/ →
ESD Ident

HP YYWWZ ← Date Code, Suffix (if needed)
HCPL-5700
▲▲ USA ← Country of Mfr

HCPL-5701
5962-898101PX*
ESD Class 2

HP Logo →
HP P/N →
DESC SMD →
DESC SMD →
Pin One/ →
ESD Ident

HP QYYWWZ ← Compliance Indicator, Date Code, Suffix (if needed)
5701/883B
5962-89810
01PX USA ← Country of Mfr
▲▲ 50434 ← HP FSCN

HCPL-5730
ESD Class 3

HP Logo →
HP P/N →
Pin One/ →
ESD Ident

HP YYWWZ ← Date Code, Suffix (if needed)
HCPL-5730
● USA ← Country of Mfr.

HCPL-5731
5962-8978501PX*
ESD Class 3

HP Logo →
HP P/N →
DESC SMD →
DESC SMD →
Pin One/ →

HP QYYWWZ ← Compliance Indicator, Date Code, Suffix (if needed)
5731/883B
5962-89785
01PX USA ← Country of Mfr.
● 50434 ← HP FSCN

HCPL-6730
ESD Class 2

Pin One/ →
ESD Ident

YYWWZ ← Date Code, Suffix (if needed)
▲▲ USA ← Country of Mfr.
HCPL-6730 ← HP P/N
HP ← HP Logo

HCPL-6731
5962-89785022A
ESD Class 2

HP Logo →
HP P/N →
Pin One/ →
ESD Ident
Country of Mfr. →

HP QYYWWZ ← Compliance Indicator, Date Code, Suffix (if needed)
6731/883B
▲▲ 5962- ← DESC SMD
89785022A ← DESC SMD
USA 50434 ← HP FSCN

*"X" is not marked on device. Replace "X" with "C" for gold lead finish; Replace "X" with "A" for solder lead finish.

HEWLETT PACKARD

AC/DC to Logic Interface Hermetically Sealed Optocouplers

Technical Data

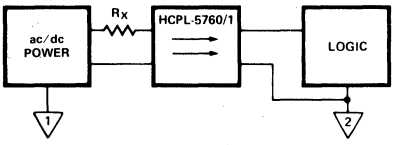
HCPL-5760
HCPL-5761 (883B)
5962 8947701PX

Features

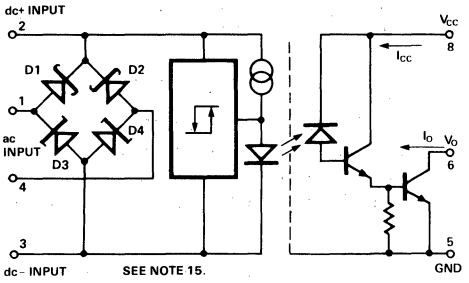
- Dual Marked with DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534, Class H
- Hermetically Sealed 8-pin Dual In-Line Packages
- Performance Guaranteed Over -55°C to +125°C
- MIL-H-38534 Class H
- ac or dc Input
- Programmable Sense Voltage
- Hysteresis
- HCPL-3700 Operating Compatibility
- Logic Compatible Output
- 1500 Vdc Withstand Test Voltage
- Thresholds Guaranteed Over Temperature
- Thresholds Independent of LED Characteristics

Applications

- Military/High Reliability/ Systems
- Limit Switch Sensing
- Low Voltage Detector
- ac/dc Voltage Sensing
- Relay Contact Monitor
- Available with Space Level Testing
- Relay Coil Voltage Monitor
- Current Sensing
- Microprocessor Interface
- Telephone Ring Detection



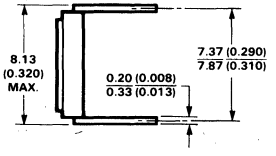
Schematic

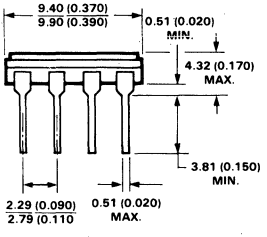


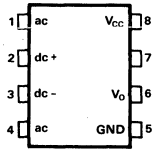
TRUTH TABLE

INPUT	OUTPUT
$H(V_{TH+} < V_{dc})$(on)	L
$L(V_{dc} < V_{TH-})$(off)	H

Outline Drawing







DIMENSIONS IN MILLIMETERS AND (INCHES).

For Gull-wing or Butt-joint lead form options, contact your local Hewlett-Packard field representative.

Description

The HCPL-5760, HCPL-5761, and 5962-8947701PX are single channel, hermetically sealed, voltage/current threshold detection optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product (HCPL-5760), with full MIL-H-38534 Class Level H testing (HCPL-5761), or from the DESC Standard Military Drawings (SMD) 5962-89477 as (5962-8947701PX). All three products are in eight pin hermetic dual in-line packages. They are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the SMD part #, or by adding option #200 to the part number for non-SMD parts.

Each unit contains a light emitting diode (LED), a threshold sensing input buffer IC, and a high gain photon detector to provide an optocoupler which permits adjustable external threshold levels. The input buffer circuit has a nominal turn on threshold of 2.5 mA (I_{TH+}) and 3.6 volts (V_{TH+}). The addition of one or more external attenuation resistors permits the use of this device over a wide range of input voltages and currents. Threshold sensing prior to the LED and detector elements minimizes effects of different optical gain and LED variations over operating life (CTR degradation). Hysteresis is also provided in the buffer for extra noise immunity and switching stability.

The buffer circuit is designed with internal clamping diodes to protect the circuitry and LED from a wide range of over-voltage and over-current transients while the diode bridge enables easy use with ac voltage input.

These units combine several unique functions in a single package, providing the user with an ideal component for computer input boards and other applications where a predetermined input threshold optocoupler level is desirable.

The high gain output stage features an open collector output providing both TTL compatible saturation voltages and CMOS compatible breakdown voltages.

The test program performed on the 5962-8947701PX is in compliance with DESC (SMD) 5962-89477. The electrical characteristics table shows Group A Subgroup testing requirements from this drawing.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply	V_{CC}	3.0	18	V
Operating Frequency[1]	f	0	10	KHz

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to 125°C
Lead Solder Temperature ..... 260°C for 10 s[2]
Average Input Current – I_{IN} ..... 15 mA[3]
Surge Input Current – $I_{IN,SG}$ ..... 140 mA[3,4]
Peak Transient Input Current – $I_{IN,PK}$ ..... 500 mA[3,4]
Input Power Dissipation – P_{IN} ..... 195 mW[5]
Total Package Power Dissipation – P_d ..... 260 mW
Output Power Dissipation – P_O ..... 65 mW
Average Output Current – I_O ..... 40 mA
Supply Voltage ,V_{CC} (Pins 8-5) ..... -0.5 min., 20 V max.
Output Voltage, V_O (Pins 6-5) ..... -0.5 min., 20 V max.

Electrical Characteristics T_A = -55°C to 125°C, unless otherwise specified.

Parameter		Symbol	Conditions	Group A[16] Subgroup	Min.	Typ.*	Max.	Units	Fig.	Note
Input Threshold Current		I_{TH+}	$V_{IN} = V_{TH+}$; V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 2.6 mA	1, 2, 3	1.75	2.5	3.20	mA	1, 2	7
		I_{TH-}	$V_{IN} = V_{TH-}$; V_{CC} = 4.5 V; V_O = 2.4 V; $I_{OH} \leq$ 250 µA	1, 2, 3	0.93	1.3	1.62	mA		
Input Threshold Voltage	dc (Pins 2, 3)	V_{TH+}	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open; V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 2.6 mA	1, 2, 3	3.18	3.6	4.10	V		
		V_{TH-}	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open; V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 250 µA	1, 2, 3	1.90	2.5	3.00	V		
	ac (Pins 1, 4)	V_{TH+}	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open; V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 2.6 mA	1, 2, 3	3.79	5.0	5.62	V		7, 8
		V_{TH-}	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open; V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 250 µA	1, 2, 3	2.57	3.7	4.52	V		
Input Clamp Voltage		V_{IHC1}	$V_{IHC1} = V_2 - V_3$; V_3 = GND; I_{IN} = 10 mA; Pin 1 & 4 Connected to Pin 3	1, 2, 3	5.3	5.9	6.7	V	3	15
		V_{IHC2}	$V_{IHC2} = \lvert V_1 - V_4 \rvert$; $\lvert I_{IN} \rvert$ = 10 mA; Pins 2 & 3 Open	1, 2, 3	6.0	6.6	7.4	V		
		V_{IHC3}	$V_{IHC3} = V_2 - V_3$; V_3 = GND; I_{IN} = 15 mA; Pins 1 & 4 Open	1, 2, 3		12.0	13.0	V		
Input Current		I_{IN}	$V_{IN} = V_2 - V_3$ = 5.0 V; Pins 1 & 4 Open	1, 2, 3	3.0	3.9	4.5	mA	4	
Logic Low Output Voltage		V_{OL}	V_{CC} = 4.5 V; I_{OL} = 2.6 mA	1, 2, 3		0.05	0.4	V	4	7
Logic High Output Current		I_{OH}	$V_{OH} = V_{CC}$ = 18 V	1, 2, 3			250	µA		
Logic Low Supply Current		I_{CCL}	$V_2 - V_3$ = 5.0 V; V_O = Open; V_{CC} = 18 V	1, 2, 3		0.8	3.0	mA		
Logic High Supply Current		I_{CCH}	V_{CC} = 18 V; V_O = Open	1, 2, 3		0.001	20	µA	5	
Input-Output Insulation		I_{I-O}	45% RH, t = 5 s; V_{I-O} = 1500 Vdc; T_A = 25°C	1			1	µA		9, 10

Electrical Characteristics T_A = -55°C to 125°C, unless otherwise specified (continued).

Parameter	Symbol	Conditions		Group A[16] Subgroup	Min.	Typ.*	Max.	Units	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}	R_L =1.8 kΩ, C_L = 15 pF		9, 10, 11		4	20	µs	6, 7	6, 11
Propagation Delay Time to Logic High Output Level	t_{PLH}	R_L =1.8 kΩ, C_L = 15 pF		9, 10, 11		8	40	µs		6, 12
Logic High Common Mode Transient Immunity	$\|CM_H\|$	V_{CM} = 50 V	T_A = 25°C, I_{IN} = 0 mA	9	1000	≥10,000		V/µs	8	13, 14
		V_{CM} = 450 V				≥10,000				
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	V_{CM} = 50 V	T_A = 25°C, I_{IN} = 4 mA	9	1000	≥5,000		V/µs		
		V_{CM} = 250 V				≥5,000				

*All typical values are at T_A = 25°C, V_{CC} = 5 V unless otherwise noted.

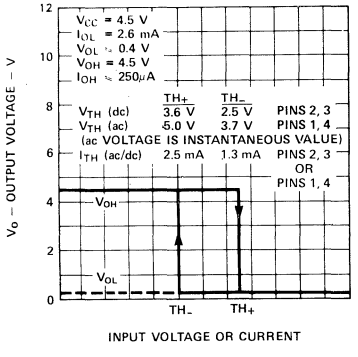


Figure 1. Typical Transfer Characteristics.

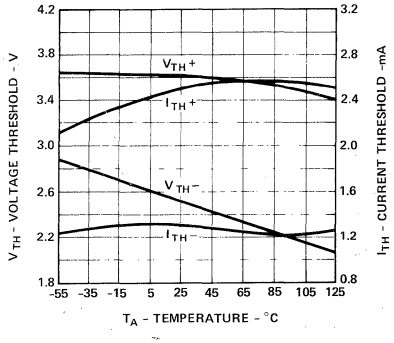


Figure 2. Typical dc Threshold Levels vs. Temperature

Typical Characteristics All typical values are at $T_A = 25°C$, $V_{CC} = 5$ V, unless otherwise specified.

Parameter	Symbol	Typ.	Units	Conditions	Fig.	Note
Hysteresis	I_{HYS}	1.2	mA	$I_{HYS} = I_{TH+} - I_{TH-}$	1	
	V_{HYS}	1.1	V	$V_{HYS} = V_{TH+} - V_{TH-}$		
Input Clamp Voltage	V_{ILC}	-0.76	V	$V_{ILC} = V_2 - V_3$; V_3 = GND; I_{IN} = -10 mA		
Bridge Diode Forward Voltage	$V_{D1,2}$	0.62		I_{IN} = 3 mA (see schematic)		
	$V_{D3,4}$	0.73				
Input-Output Resistance	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 Vdc		9
Input-Output Capacitance	C_{I-O}	2.0	pF	f = 1 MHz, V_{I-O} = 0 Vdc		
Input Capacitance	C_{IN}	50	pF	f = 1 MHz; V_{IN} = 0 V, Pins 2 & 3, Pins 1 & 4 Open		
Output Rise Time (10-90%)	t_r	10	µs		7	
Output Fall Time (90-10%)	t_f	0.5	µs		7	

Notes:

1. Maximum operating frequency is defined when output waveform (Pin 6) attains only 90% of V_{CC} with R_L = 1.8 kΩ, C_L = 15 pF using a 5 V square wave input signal.
2. Measured at a point 1.6 mm below seating plane.
3. Current into/out of any single lead.
4. Surge input current duration is 3 ms at 120 Hz pulse repetition rate. Transient input current duration is 10 µs at 120 Hz pulse repetition rate. Note that maximum input power, P_{IN}, must be observed.
5. Derate linearly above 100°C free-air temperature at a rate of 4.26 mW/°C. Maximum input power dissipation of 195 mW allows an input IC junction temperature of 150°C at an ambient temperature of T_A = 125°C with a typical thermal resistance from junction to ambient of θ_{JA} = 235°C/W. The typical thermal resistance from junction to case is equal to 170°C/W. Excessive P_{IN} and T_J may result in device degradation.
6. The 1.8 kΩ load represents 1 TTL unit load of 1.6 mA and the 4.7 kΩ pull-up resistor.
7. Logic low output level at Pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH}$ – once V_{IN} has exceeded V_{TH+}. Logic high output level at Pin 6 occurs under the conditions of $V_{IN} \leq V_{TH-}$ as well as the range of $V_{IN} < V_{TH+}$ once V_{IN} has decreased below V_{TH-}.
8. The ac voltage is instantaneous voltage.
9. Device considered a two terminal device: Pins 1, 2, 3, 4 connected together, Pins 5, 6, 7 8 connected together.
10. This is a momentary withstand test, not an operating condition.
11. The t_{PHL} propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 µs rise time) to the 1.5 V level on the leading edge of the output pulse (see Figure 7).
12. The t_{PLH} propagation delay is measured from the 2.5 V level of the trailing edge of a 5.0 V input pulse (1 µs fall time) to the 1.5 V level on the trailing edge of the output pulse (see Figure 7).
13. Common mode transient immunity in Logic High level is the maximum tolerable $dV_{CM/dt}$ of the common mode voltage, V_{CM}, to ensure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in Logic Low level is the maximum tolerable $dV_{CM/dt}$ of the common mode voltage, V_{CM}, to ensure that the output will remain in a Logic Low state (i.e., $V_O < 0.8$ V). See figure 8.
14. In applications were $dV_{CM/dt}$ may exceed 50,000 V/µs (such as static discharge), a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value for R_{CC} is 240 Ω per volt of allowable drop in V_{CC} (between Pin 8 and V_{CC}) with a minimum value of 240 Ω.
15. D_1 and D_2 are Schottky diodes; D_3 and D_4 are zener diodes.
16. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10 ,3 and 11, respectively.)

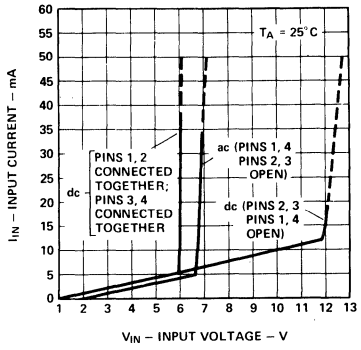


Figure 3. Typical Input Characteristics, I_{IN} vs. V_{IN}. (ac Voltage Is Instantaneous Value.)

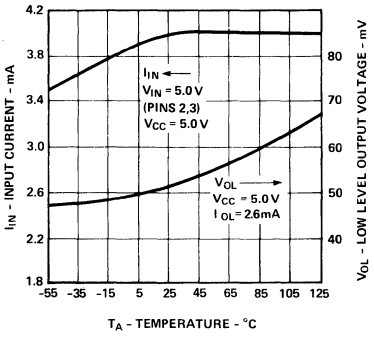


Figure 4. Typical Input Current, I_{IN}, and Low Level Output Voltage, V_{OL}, vs. Temperature.

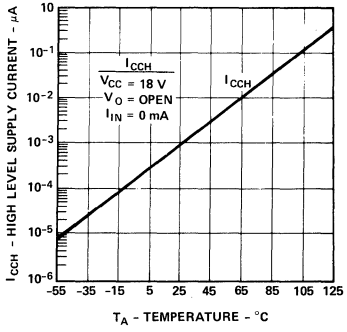


Figure 5. Typical High Level Supply Current, I_{CCH} vs. Temperature.

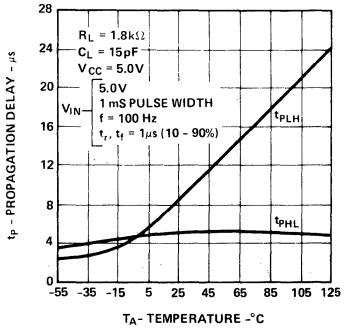


Figure 6. Typical Propagation Delay vs. Temperature.

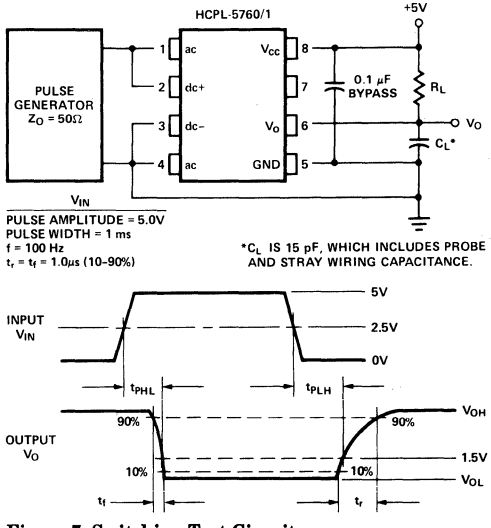


Figure 7. Switching Test Circuit.

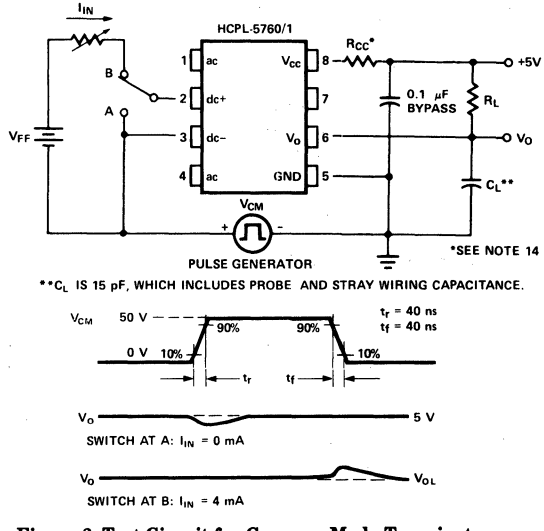


Figure 8. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

5962-8947701PC and MIL-H-38534 Class H Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-H-38534 and DESC SMD 5962-89477.

Testing consists of 100% screening and quality conformance inspection to MIL-H-38534.

Electrical Considerations

The HCPL-5760, HCPL-5761, or 5962-8947701PX optocoupler has internal temperature compensated, predictable voltage and current threshold points which allow selection of an external resistor, R_x, to determine larger external threshold voltage levels. For a desired external threshold voltage, $V_{\pm}$, a corresponding typical value of Rx can be obtained from Figure 10. Specific calculation of R_x can be obtained from Equation (1) of Figure 11. Specification of both V_+ and V_- voltage threshold levels simultaneously can be obtained by the use of R_x and R_p as shown in Figure 11 and determined by Equations (2) and (3).

Rx can provide over-current transient protection by limiting input current during a transient condition. For monitoring contacts with a relay or switch, the HCPL-5760/1, or 5962-8947701PX combination with R_x and R_p can be used to allow a specific current to be conducted through the contacts for cleaning purposes (wetting current).

The choice of which input voltage clamp level to choose depends upon the application of this device (see Figure 3). It is recommended that the low clamp condition be used when possible to lower the input power dissipation as well as the LED current, which minimizes LED degradation over time.

In applications where $dV_{CM/dt}$ may be extremely large (such as static discharge), a series resistor, R_{CC}, should be connected in series with V_{CC} and Pin 8 to protect the detector IC from destructively high surge currents. See note 14 for determination of R_{CC}. In addition, it is recommended that a ceramic disc bypass capacitor of 0.01 µF to 0.1 µF be placed between Pins 8 and 5 to reduce the effect of power supply noise.

Part Numbering System

Commercial Product	Class H Product	DESC Product	Class K Product
HCPL-5760	HCPL-5761	5962-8947701PX	TBD

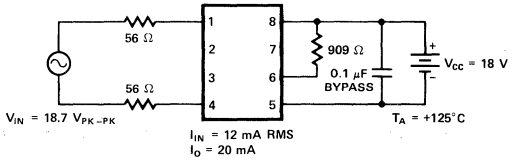


Figure 9. Operating Circuit for Burn-In and Steady State Life Tests

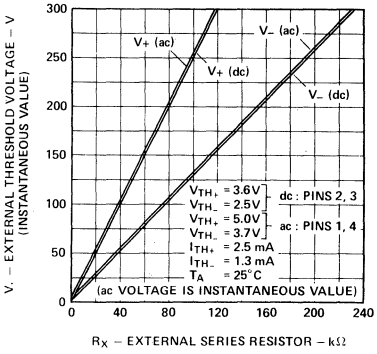


Figure 10. Typical External Threshold Characteristic, $V_{\pm}$ vs. R_x

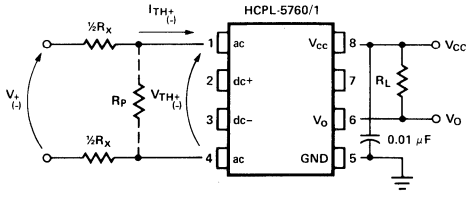


Figure 11. External Threshold Voltage Level Selection

For interfacing ac signals to TTL systems, output low pass filtering can be performed with a pullup resistor of 1.5 kΩ and 20 μF capacitor. This application requires a Schmitt trigger gate to avoid slow rise time chatter problems. For ac input applications, a filter capacitor can be placed across the dc input terminals for either signal or transient filtering.

Either ac (Pins 1, 4) or dc (Pins 2, 3) input can be used to determine external threshold levels.

For one specifically selected external threshold voltage level V_+ or V_-, R_x can be determined without use of R_p via

$$R_x = \frac{V_{+(-)} - V_{TH+(-)}}{I_{TH+(-)}} \quad (1)$$

For two specifically selected external threshold voltage levels, V_+ and V_-, the use of R_x and R_p will permit this selection via equations (2), (3) provided the following conditions are met:

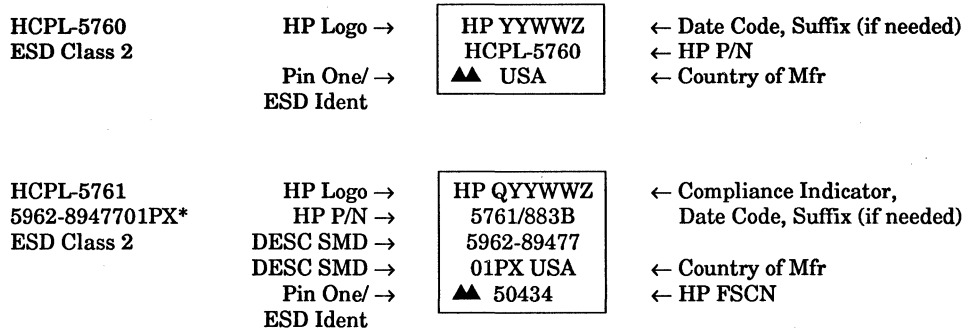
$$\frac{V_+}{V_-} \geq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}}$$

$$R_x = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_{TH-}) - I_{TH-}(V_{TH+})} \quad (2)$$

$$R_P = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_- - V_{TH-}) + I_{TH-}(V_{TH+} - V_+)} \quad (3)$$

See Application Note 1004 for more information.

Part Marking Orientation for HCPL-576X Base Product and Related DESC Product



*"X" is not marked on device. Replace "X" with "C" for gold lead finish; Replace "X" with "A" for solder lead finish.

HEWLETT PACKARD

Dual Channel Hermetically Sealed Transistor Output Optocoupler

Technical Data

4N55
4N55/883B
5962-8767901EX

Features

- Dual Marked with DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534, Class H
- Hermetically Sealed 16-pin Dual In-Line Package
- Performance Guaranteed Over -55°C to +125°C
- MIL-H-38534 Class H
- Dual Isolated Channels
- High Speed: Typically 400kBit/s
- 2-MHz Bandwidth
- Open Collector Outputs
- 2-18 Volt V_{CC} Range
- 1500 Vdc Withstand Test Voltage
- High Radiation Immunity
- HCPL-2530/2531, HCPL-55XX, 65XX Function Compatibility
- Reliability Data Available
- Available with TXV or TXVB Part Marking

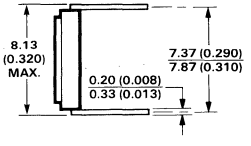
Applications

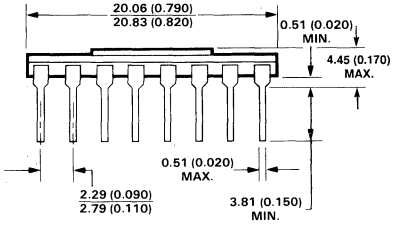
- Military/High Reliability Systems
- Line Receivers
- Digital Logic Ground Isolation
- Analog Signal Ground Isolation
- Space Level Testing Available
- Switching Power Supply Feedback Element
- Vehicle Command/Control
- System Test Equipment
- Level Shifting

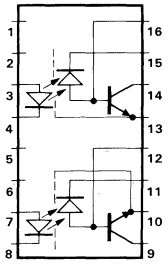
Description

The 4N55, 4N55/883B, and 5962-8767901EX units consist of two completely independent transistor output optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product (4N55), with full MIL-H-38534 Class Level H testing (4N55/883B) or from the DESC Standard Military Drawing (SMD) 5962-87679 as (5962-8767901EC). All three

Outline Drawing







DIMENSIONS IN MILLIMETERS AND (INCHES)

For Gull-wing or Butt-joint lead form options, contact your local Hewlett-Packard field representative.

products are assembled in hermetic, sixteen pin dual in-line packages. These parts are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the DESC part #, or by adding option #200 to the part number for non DESC parts.

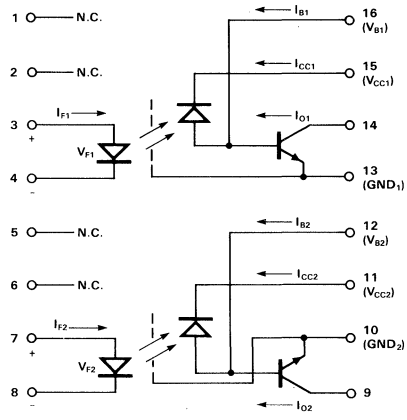
Each channel has a GaAsP light emitting diode which is optically coupled to an integrated photon detector. Separate connections for the photodiodes and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor optocoupler by reducing the base-collector capacitance.

These devices are suitable for wide bandwidth analog applications, as well as for interfacing TTL to LSTTL or CMOS. Current Transfer Ratio (CTR) is 9% minimum at I_F = 16 mA. The 18 V V_{CC} capability will enable the designer to interface any TTL family to CMOS. The availability of the base lead allows optimized gain/bandwidth adjustment in analog applications. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor couplers.

The test program performed on the 5962-8767901EX is in compliance with DESC (SMD) 5962-87679. The Electrical Characteristics Table shows Group A Subgroup testing requirements from this drawing.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Schematic



CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}		250	μA
Supply Voltage	V_{CC}	2	18	V
Operating Temperature	T_C	-55	+125	°C
Input Current, High Level	$I_{F,H}$	12	20	mA

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10 s.
(1.6 mm below seating plane)
Average Input Current – I_F (each channel) ..... 20 mA
Peak Input Current – I_F (each channel,
≤ 1 ms duration) ..... 40 mA
Reverse Input Voltage — V_R (each channel) ..... 5 V
Input Power Dissipation (each channel) ..... 36 mW
Average Output Current — I_O (each channel) ..... 8 mA
Peak Output Current — I_O (each channel) ..... 16 mA
Supply Voltage — V_{CC} (each channel) ..... -0.5 V to 20 V
Output Voltage — V_O (each channel) ..... -0.5 V to 20 V
Emitter Base Reverse Voltage – V_{EBO} ..... 3.0 V
Base Current – I_B (each channel) ..... 5 mA
Output Power Dissipation (each channel) ..... 50 mW
Derate linearly above 100°C free air temperature
at a rate of 1.4 mW/°C.

Electrical Characteristics (T_A = -55°C to 125°C, unless otherwise specified)

Parameter	Sym.	Test Conditions[5]	Group A Subgroups[10]	Limits			Units	Fig.	Note
				Min.	Typ.**	Max.			
Input Forward Voltage	V_F*	I_F = 20 mA	1, 2, 3		1.55	1.80	Vdc	1	1
Reverse Breakdown Voltage	BV_R*	I_R = 10 µA	1, 2, 3	5.0			Vdc		1
Coupled High Level Output Current	I_{OH}	I_F = 0, I_F (other channel) = 20 mA V_O = V_{CC} = 18 V	1, 2, 3		10	100	µA dc	4	1
Output Leakage Current	I_{OLEAK}*	I_F = 250 µA, I_F (other channel) = 20 mA, V_O = V_{CC} = 18 V	1, 2, 3		30	250	µA dc	4	1
Current Transfer Ratio	CTR*	V_{CC} = 4.5 V; V_O = 0.4 V; I_F = 16 mA	1, 2, 3	9	20		%	2, 3	1, 2
Input to Output Insulation Leakage Current	$I_{I/O}$*	T_C = +25°C; $V_{I/O}$ = 1500 Vdc Relative humidity = 45%; t = 5 s	1			1.0	µA dc		3, 9
Supply Current High Level	I_{CCH}*	I_F = 0 mA, I_F (other channel) = 20 mA, V_{CC} = 18 V	1, 2, 3		0.1	10	µA dc		1
Supply Current Low Level	I_{CCL}*	I_{F1} = I_{F2} = 20 mA, V_{CC} = 18 V	1, 2, 3		35	200	µA dc	5	1
Propagation Delay Time									
HIGH to LOW	t_{PHL}*	I_F = 16 mA; R_L = 8.2 kΩ V_{CC} = 5.0 V; C_L = 50 pF	9, 10, 11		0.4	2	µs	6, 9	1
LOW to HIGH	t_{PLH}*				1.0	6			

*JEDEC Registered Data.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Note
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	-1.5	mV/°C	I_F = 20 mA		1
Input Capacitance	C_{IN}	60	pF	f = 1 MHz, V_F = 0 Vdc		1
Input-Output Resistance	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 Vdc		1
Input-Output Capacitance	C_{I-O}	1.0	pF	f = 1 MHz		1, 4
Input-Input Insulation Leakage Current	I_{I-I}	1	pA	45% Relative Humidity, V_{I-I} = 500 Vdc, t = 5 s		5
Input-Input Capacitance	C_{I-I}	0.55	pF	f = 1 MHz		5
Transistor DC Current Gain	h_{FE}	150	–	V_O = 5 V, I_O = 3 mA		1
Small Signal Current Transfer Ratio	$\frac{\Delta I_O}{\Delta I_F}$	21	%	V_{CC} = 5 V, V_O = 2 V	7	1
Common Mode Transient Immunity at Logic High Level Output	$\lvert CM_H \rvert$	1000	V/µs	I_F = 0, R_L = 8.2 kΩ V_{CM} = 10 V_{p-p} V_O (min.) = 2.0 V	10	1, 6
Common Mode Transient Immunity at Logic Low Level Output	$\lvert CM_L \rvert$	1000	V/µs	I_F = 16 mA, R_L = 8.2 kΩ V_{CM} = 10 V_{p-p} V_O (max.) = 0.8 V	10	1, 7
Bandwidth	BW	9	MHz		8	8

Notes:

1. Each channel.
2. Current Transfer Ratio is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%. CTR is known to degrade slightly over the unit's lifetime as a function of input current, temperature, signal duty cycle and system on time. Refer to Application Note 1002 for more detail. In short it is recommended that designers allow at least 20-25% guardband for CTR degradation.
3. Measured between pins 1 through 8 shorted together and pins 9 through 16 shorted together.
4. Measured between each input pair shorted together and the output pins for that channel shorted together.
5. Measured between pins 3 and 4 shorted together and pins 7 and 8 shorted together.
6. CM_H is the steepest slope (dV/dt) on the leading edge of the common mode pulse, V_{CM}, for which the output will remain in the logic high state (i.e., V_O > 2.0 V).
7. CM_L is the steepest slope (dV/dt) on the trailing edge of the common mode pulse, V_{CM}, for which the output will remain in the logic low state (i.e., V_O < 0.8 V).
8. Bandwidth is the frequency at which the ac output voltage is 3 dB below the low frequency asymptote.
9. This is a momentary withstand test, not an operating condition.
10. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

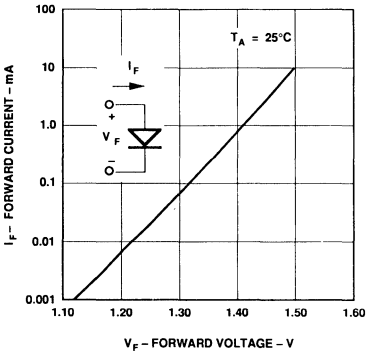


Figure 1. Input Diode Forward Current vs. Forward Voltage.

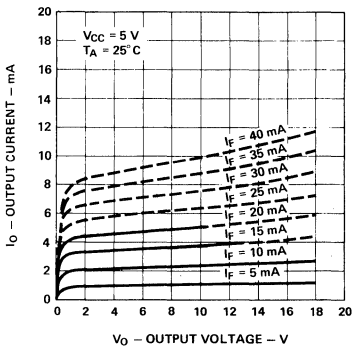


Figure 2. DC and Pulsed Transfer Characteristic.

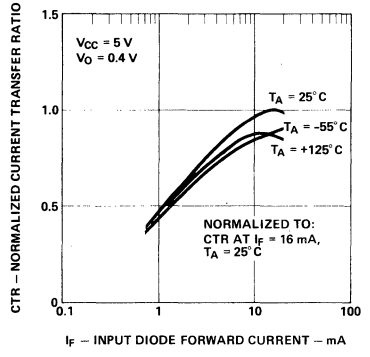


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

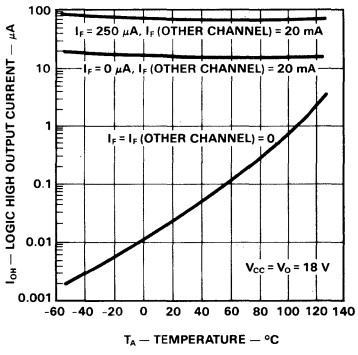


Figure 4. Logic High Output Current vs. Temperature.

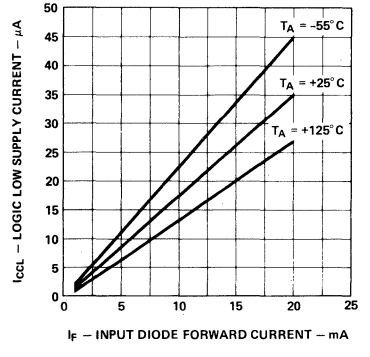


Figure 5. Logic Low Supply Current vs. Input Diode Forward Current.

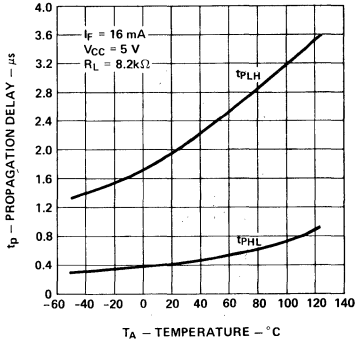


Figure 6. Propagation Delay vs. Temperature.

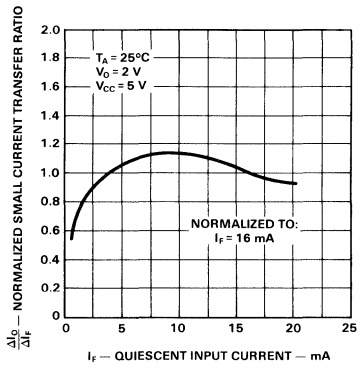


Figure 7. Normalized Small Signal Current Transfer Ratio vs. Quiescent Input Current.

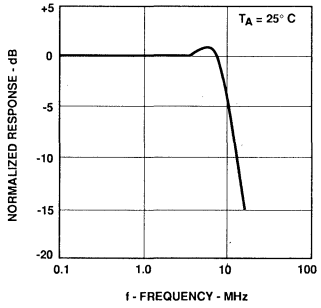


Figure 8a. Frequency Response.

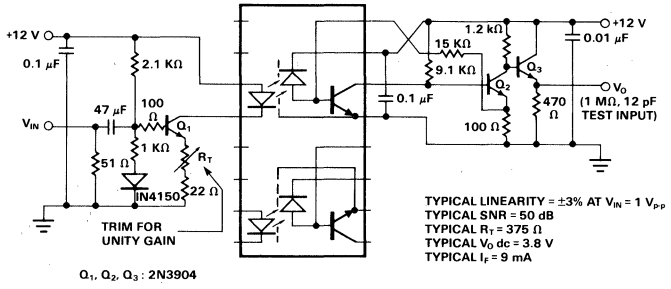


Figure 8b. Frequency Response.

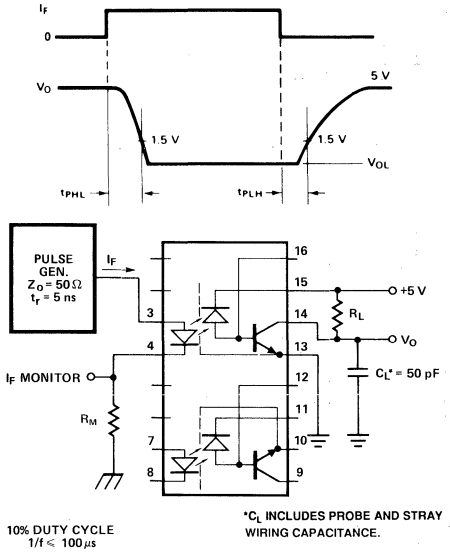


Figure 9. Switching Test Circuit.*
*JEDEC Registered Data.

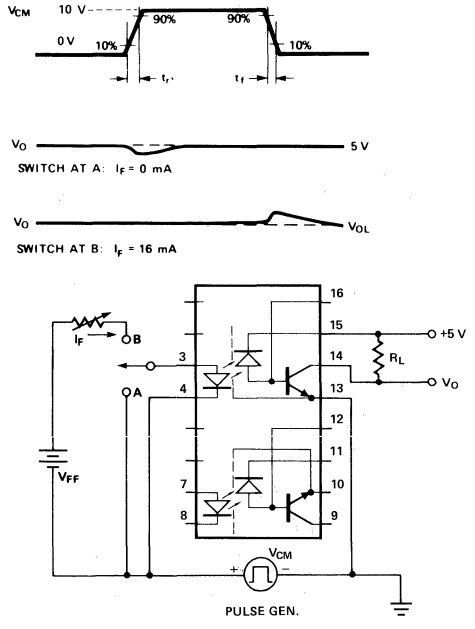
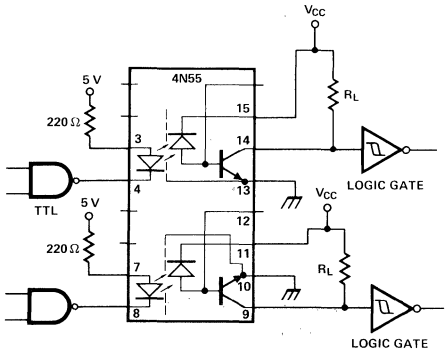


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.



LOGIC FAMILY	LSTTL	CMOS	
DEVICE NO.	54LS14	CD40106BM	
V_{cc}	5 V	5 V	15 V
R_L 5% TOLERANCE	18 kΩ*	8.2 kΩ	22 kΩ

***THE EQUIVALENT OUTPUT LOAD RESISTANCE IS AFFECTED BY THE LSTTL INPUT CURRENT AND IS APPROXIMATELY 8.2 kΩ.**

This is a worst case design which takes into account 25% degradation of CTR. See App. Note 1002 to assess actual degradation and lifetime.

Figure 11. Recommended Logic Interface.

5962-8767901EX and MIL-H-38534 Class H Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-H-38534 and DESC SMD 5962-87679.

Testing consists of 100% screening and quality conformance inspection to MIL-H-38534.

Part Numbering System

Commercial Product	Class H Product	DESC Product	Class K Product
4N55	4N55/883B	5962-8767901EX	TBD

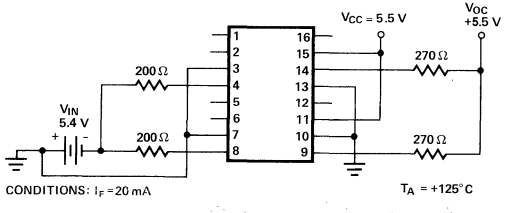
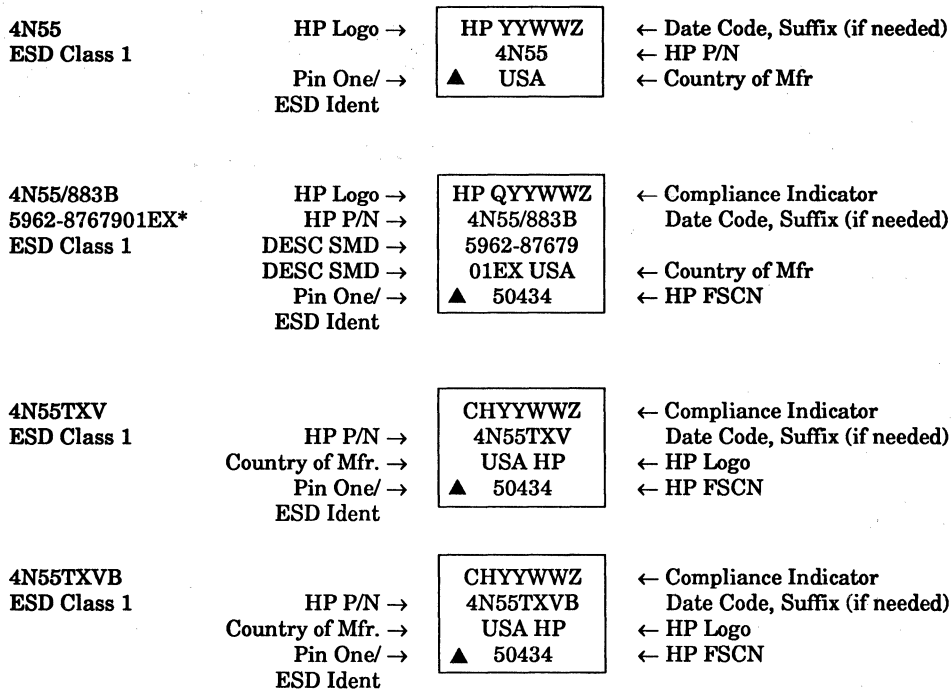


Figure 12. Operating Circuit for Burn-in and Steady State Life Tests.

Part Marking Orientation for 4N55 Base Product and Related DESC Product



*"X" is not marked on device. Replace "X" with "C" for gold lead finish; Replace "X" with "A" for solder lead finish.

HEWLETT PACKARD

Transistor Output, Hermetically Sealed Optocoupler

Technical Data

HCPL-5500
HCPL-5501 (883B)
5962-9085401HPX
HCPL-5530
HCPL-5531 (883B)
5962-8767902PX
(8-pin Dual In-Line Package)
HCPL-6530
HCPL-6531 (883B)
5962-87679032A
(20 Terminal Leadless Chip Carrier)

Features

- **Dual Marked with DESC SMD**
- **Manufactured and Tested on a MIL-STD-1772 Certified Line**
- **QML-MIL-H-38534, Class H**
- **Performance Guaranteed Over -55°C to +125°C**
- **MIL-H-38534 Class H**
- **High Speed: Typically 400 kbit/s**
- **9 MHz Bandwidth**
- **Open Collector Outputs**
- **1500 Vdc Withstand Test Voltage**
- **High Radiation Immunity**
- **4N55, 6N135/6, HCPL-2530/31 Function Compatibility**
- **2-18 Volt V_{CC} Range**
- **Reliability Data Available**
- **High Common Mode Noise Immunity; Special Testing Available for Selections with 883B and SMD**

Applications

- **Military/High Reliability Systems**
- **Isolated Input Line Receiver**
- **Isolated Output Line Driver**
- **System Test Equipment Isolation**
- **Digital Logic Ground Isolation**
- **Current Loop Receiver**
- **Level Shifting**
- **Analog Signal Ground Isolation**
- **Vehicle Command/Control**
- **Switching Power Supply Feedback Element**
- **Space Level Testing Available**

Description

These units are single and dual channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product or with full MIL-H-38534 Class Level H testing. All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

The HCPL-5500, 5501, 5530 and 5531 are in a 8 Pin ceramic DIP configured as either single or dual channel devices. The standard products are HCPL-5500 and HCPL-5530. The products with full MIL-H-38534 Class Level H testing are HCPL-5501 and HCPL-5531.

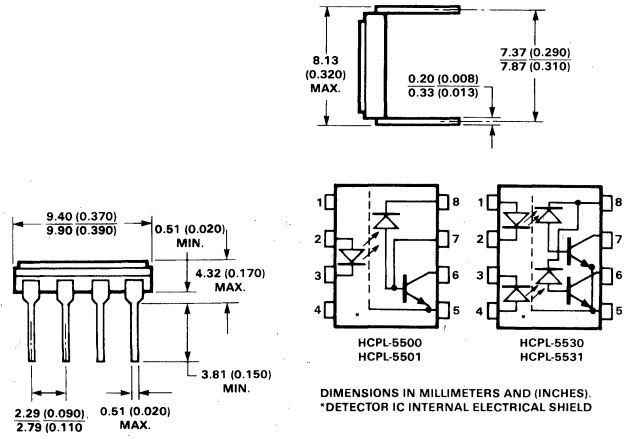
The HCPL-6530 and HCPL-6531 parts are in twenty terminal hermetic, ceramic, leadless chip carriers. The standard part is HCPL-6530. The product with full MIL-H-38534 Class Level H testing is HCPL-6531. These dual channel devices are configured and function as two independent single channels. Devices are delivered with solder dipped terminals as a standard feature. Units may also be purchased with gold plated terminals.

Each channel contains a light emitting diode optically coupled to an integrated photon detector providing 1500 Vdc electrical isolation between input and output. Separate connections for the photodiodes and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor optocoupler by reducing the base-collector capacitance. These devices are suitable for wide bandwidth analog applications, as well as for interfacing TTL to LSTTL or CMOS. Current Transfer Ratio (CTR) is 9% minimum at I_F = 16 mA over the full military operating temperature range, -55°C to +125°C. The 18 V V_{CC} capability will enable the designer to interface any TTL family to CMOS. The availability of the base lead allows optimized gain/bandwidth adjustment in analog applications. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor couplers.

These products are also available with the transistor base node unconnected to improve common mode noise immunity and ESD susceptibility. In addition, higher CTR minimums are available by special request. Contact your local HP Field Sales Engineer for ordering information.

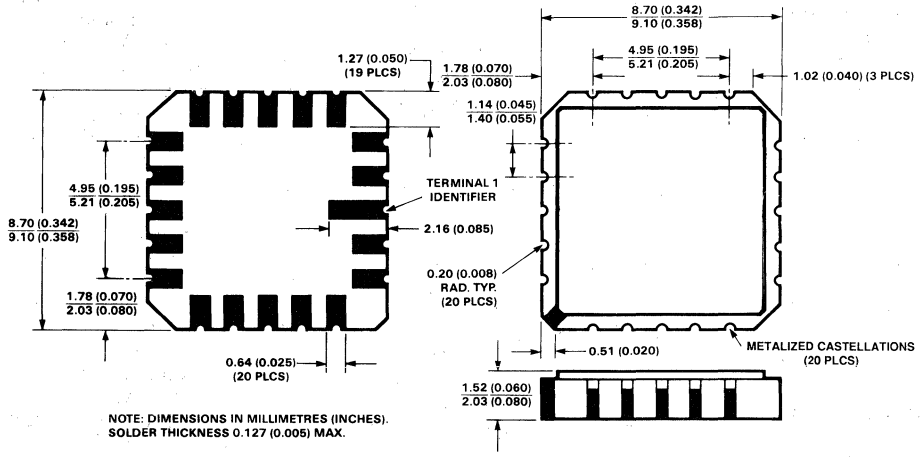
Outline Drawings

8-pin Ceramic Dual In-Line Package



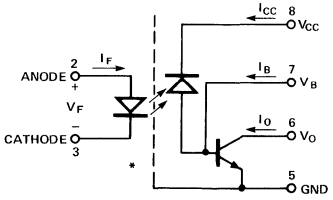
For Gull-wing or Butt-joint lead form options, contact your local Hewlett-Packard field representative.

20 Terminal Ceramic Leadless Chip Carrier



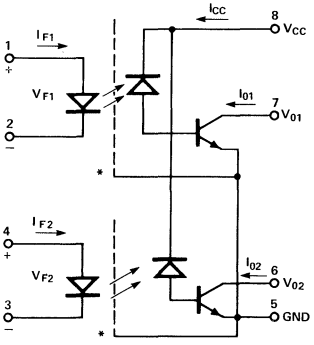
8 PIN Ceramic DIP

SINGLE CHANNEL SCHEMATIC

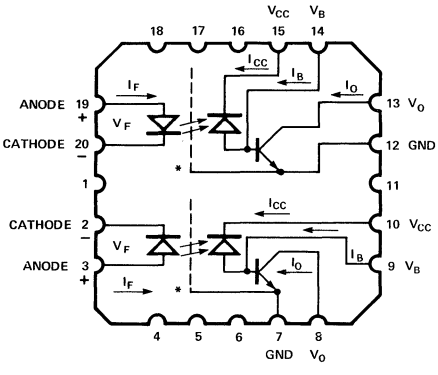


8 PIN Ceramic DIP

DUAL CHANNEL SCHEMATIC



20 Terminal Ceramic Leadless Chip Carrier Schematic



* DETECTOR IC INTERNAL ELECTRICAL SHIELD

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}		250	µA
Supply Voltage	V_{CC}	2	18	V

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10 s
Average Input Current, I_F each channel ..... 20 mA
Peak Input Current, I_F each channel,
≤1 ms duration ..... 40 mA
Reverse Input Voltage, V_R each channel ..... 3 V
Average Output Current, I_O each channel ..... 8 mA
Peak Output Current, I_O each channel ..... 16 mA
Supply Voltage, V_{CC} each channel ..... -0.5 V to 20 V
Output Voltage, V_O each channel ..... -0.5 V to 20 V
Input Power Dissipation, each channel ..... 36 mW
Output Power Dissipation, each channel ..... 50 mW
ESD Classification ..... Class 1
ESD Classification (HCPL-5530/1) ..... Class 3
(MIL-STD-883, Method 3015)

Single Channel Product Only

Emitter Base Reverse Voltage. V_{EBO} ..... 3.0 V
Base Current, I_B each channel ..... 5 mA

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and degradation which may be induced by ESD.

Electrical Characteristics T_A = -55°C to +125°C, unless otherwise specified

Parameter		Sym.	Test Conditions	Group A Sub-groups[12]	Limits			Units	Fig.	Note
					Min.	Typ.*	Max.			
Current Transfer Ratio		CTR	I_F = 16 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1, 2, 3	9	20		%	2, 3	1, 2, 10
Logic High Output Current		I_{OH}	I_F = 0, I_F (other channel) = 20 mA V_O = V_{CC} = 18 V	1, 2, 3		5	100	µA	4	1
Output Leakage Current Dual Channel		I_{OH1}	I_F = 250 µA, I_F (other channel) = 20 mA, V_O = V_{CC} = 18 V	1, 2, 3		30	250	µA	4	1
Logic Low Supply Current	Single Channel	I_{CCL}	I_F = 20 mA, V_{CC} = 18 V	1, 2, 3		35	200	µA	5	1
	Dual Channel		I_{F1} = I_{F2} = 20 mA, V_{CC} = 18 V			70	400			4
Logic High Supply Current	Single Channel	I_{CCH}	I_F = 0 mA, V_{CC} = 18 V	1, 2, 3		0.1	10	µA		1
	Dual Channel		I_F = 0 mA, I_F (other channel) = 20 mA, V_{CC} = 18 V			0.2	20			4
Input Forward Voltage		V_F	I_F = 20 mA	1, 2, 3		1.55	1.9	V	1	1
Input Reverse Breakdown Voltage		B_{VR}	I_R = 10 µA	1, 2, 3	3			V		1
Input-Output Insulation Leakage Current		I_{I-O}	45% Relative Humidity, T_A = 25°C, t = 5 s, V_{I-O} = 1500 Vdc	1			1.0	µA		3, 9
Propagation Delay Time to Logic High at Output		t_{PLH}	R_L = 8.2 kΩ, C_L = 50 pF I_F = 16 mA, V_{CC} = 5 V	9, 10, 11		1.0	6.0	µs	6, 9	1, 6
Propagation Delay Time to Logic Low at Output		t_{PHL}	R_L = 8.2 kΩ, C_L = 50 pF I_F = 16 mA, V_{CC} = 5 V	9, 10, 11		0.4	2.0	µs	6, 9	1, 6

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics $T_A = 25°C$, $V_{CC} = 5$ V

Parameter	Sym.	Typ.	Units	Test Conditions	Fig.	Note
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	-1.5	mV/°C	$I_F = 20$ mA		1
Input Capacitance	C_{in}	60	pF	f = 1 MHz, $V_F = 0$		1
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	$V_{I-O} = 500$ Vdc		3
Capacitance (Input-Output)	C_{I-O}	1.0	pF	f = 1 MHz		1, 11
Transistor DC Current Gain	h_{FE}	250	–	$V_O = 5$ V, $I_O = 3$ mA		1
Small Signal Current Transfer Ratio	$\frac{\Delta I_O}{\Delta I_F}$	21	%	$V_{CC} = 5$ V, $V_O = 2$ V	7	1
Bandwidth	BW	9	MHz		8	8
Common Mode Transient Immunity At Logic High Level Output	$\lvert CM_H \rvert$	1000	V/μs	$I_F = 0$ mA, $R_L = 8.2$ kΩ $V_{CM} = 10\ V_{p-p}$	10	1, 7
Common Mode Transient Immunity At Logic Low Level Output	$\lvert CM_L \rvert$	-1000	V/μs	$I_F = 16$ mA, $R_L = 8.2$ kΩ $V_{CM} = 10\ V_{p-p}$	10	1, 7

Dual Channel Product Only

Input-Input Insulation Leakage Current	I_{I-I}	1	pA	45% Relative Humidity, $V_{I-I} = 500$ Vdc, t = 5 s		5, 9
Capacitance (Input-Input)	C_{I-I}	0.8	pF	f = 1 MHz		5
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	$V_{I-I} = 500$ Vdc		5

Notes:
1. Each channel of a dual channel device.
2. Current Transfer Ratio is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%. CTR is known to degrade slightly over the unit's lifetime as a function of input current, temperature, signal duty cycle, and system on time. Refer to Application Note 1002 for more detail. In short, it is recommended that designers allow at least 20-25% guardband for CTR degradation.
3. Device considered a two-terminal device: for 8 pin DIP, pins 1 through 4 are shorted together, and pins 5 through 8 are shorted together; for LCC, terminals 19, 20, 1, 2, 3 are shorted together, and terminals 7 through 15 are shorted together.
4. The HCPL-6530 and HCPL-6531 dual channel parts function as two independent single channel units. Use the single channel parameter limits.
5. Measured between adjacent input pairs shorted together; i.e., for 8 pin DIP, between pins 1 and 2 shorted together and pins 3 and 4 shorted together; for LCC, between terminals 19 and 20 shorted together, and terminals 2 and 3 shorted together.
6. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.

7. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).
8. Bandwidth is the frequency at which the ac output voltage is 3 dB below the low frequency asymptote. For the HCPL-5530 the typical bandwidth is 2 MHz.
9. This is a momentary withstand test, not an operating condition.
10. Higher CTR minimums are available to support special applications.
11. Measured between each input pair shorted together and all outputs for that channel shorted together.
12. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125 and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

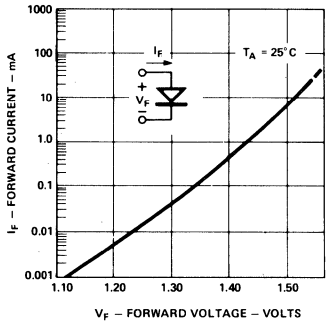


Figure 1. Input Diode Forward Characteristic.

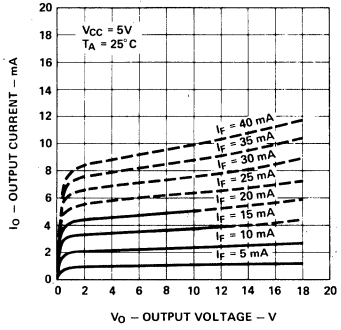


Figure 2. DC and Pulsed Transfer Characteristic.

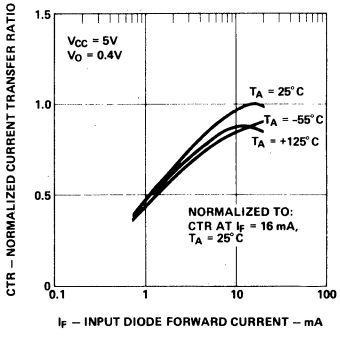


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

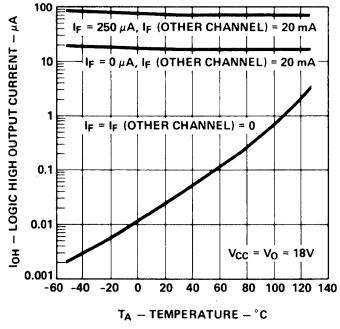


Figure 4. Logic High Output Current vs. Temperature.

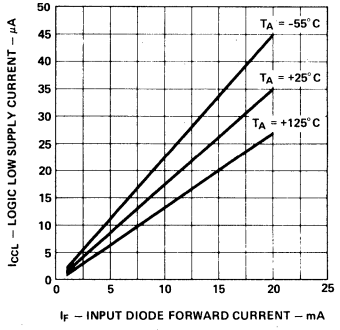


Figure 5. Logic Low Supply Current vs. Input Diode Forward Current.

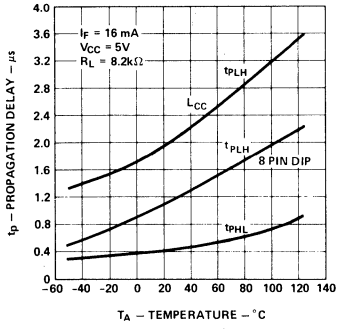


Figure 6. Propagation Delay vs. Temperature.

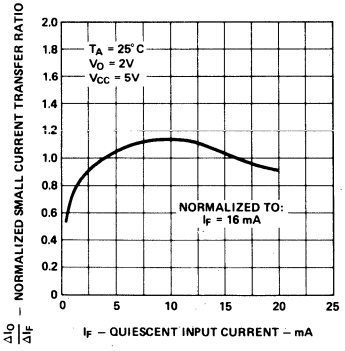


Figure 7. Normalized Small Signal Current Transfer Ratio vs. Quiescent Input Current.

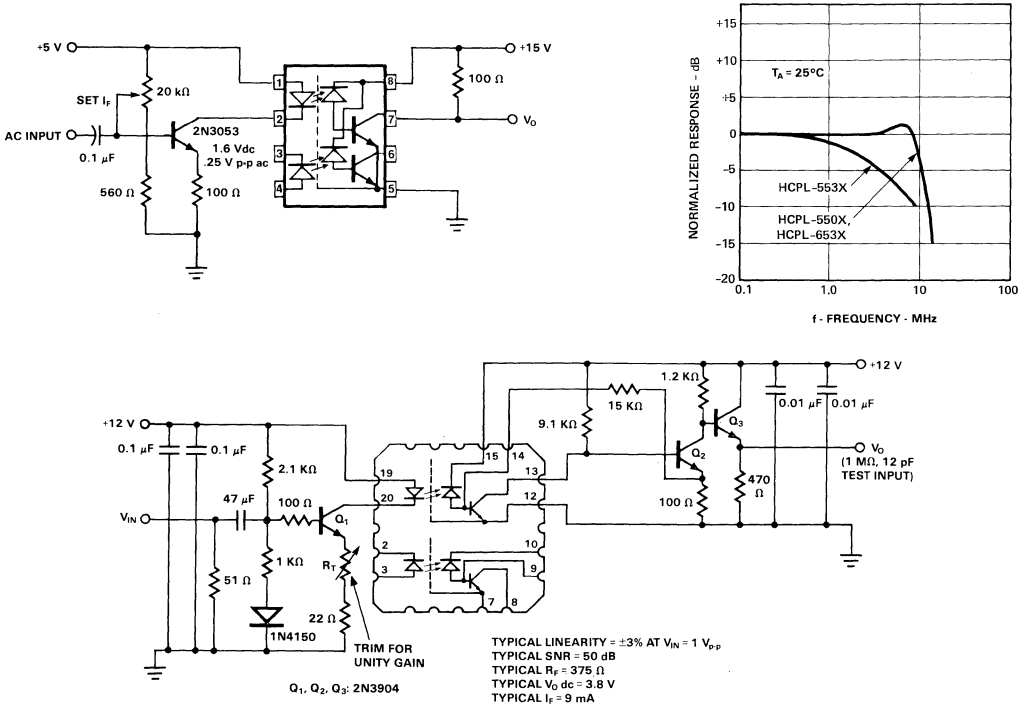


Figure 8. Frequency Response.

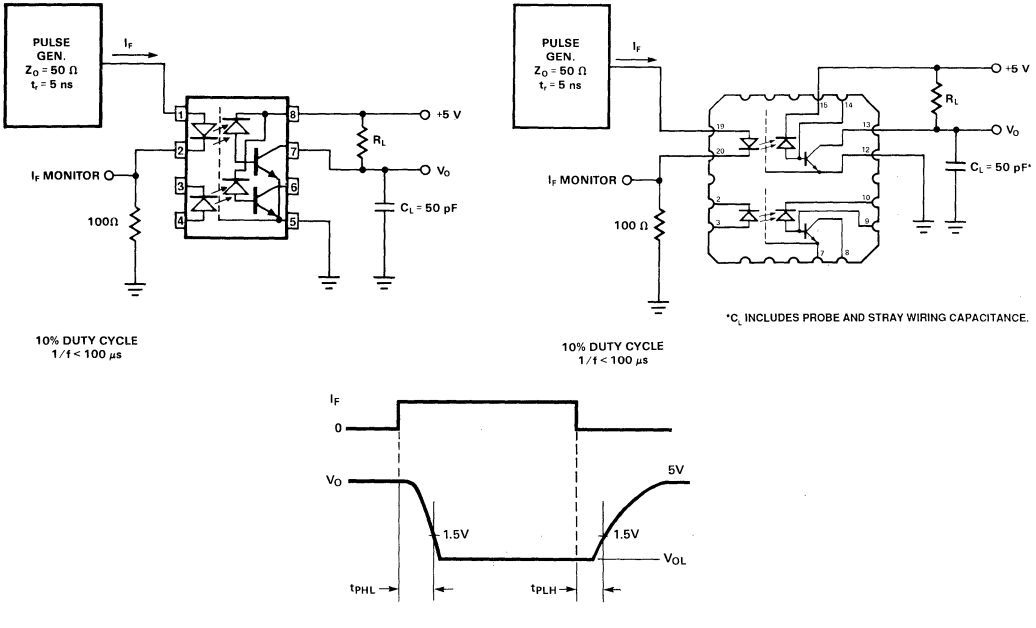


Figure 9. Switching Test Circuit.

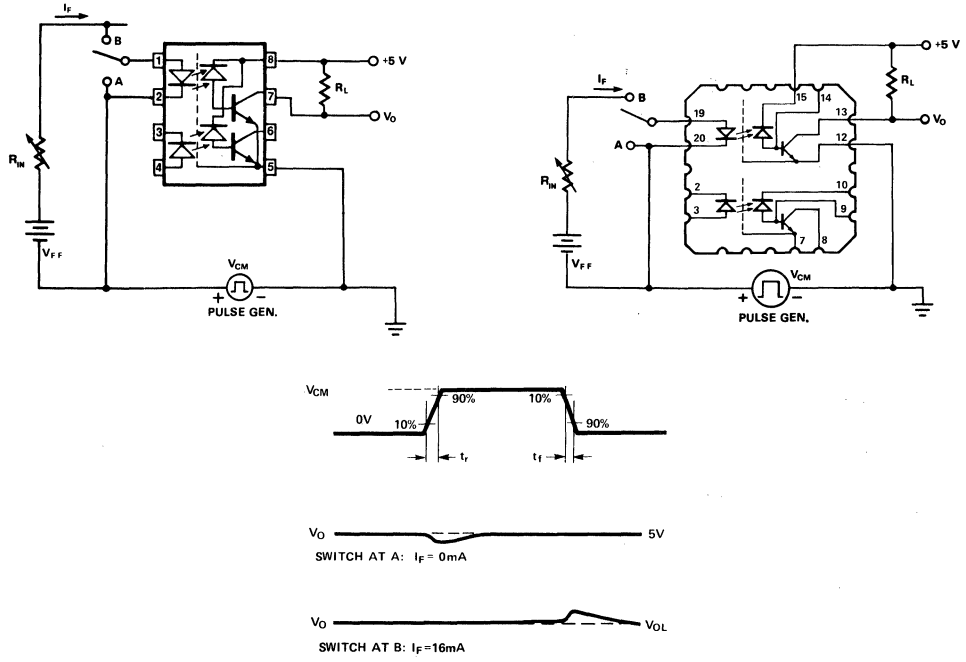
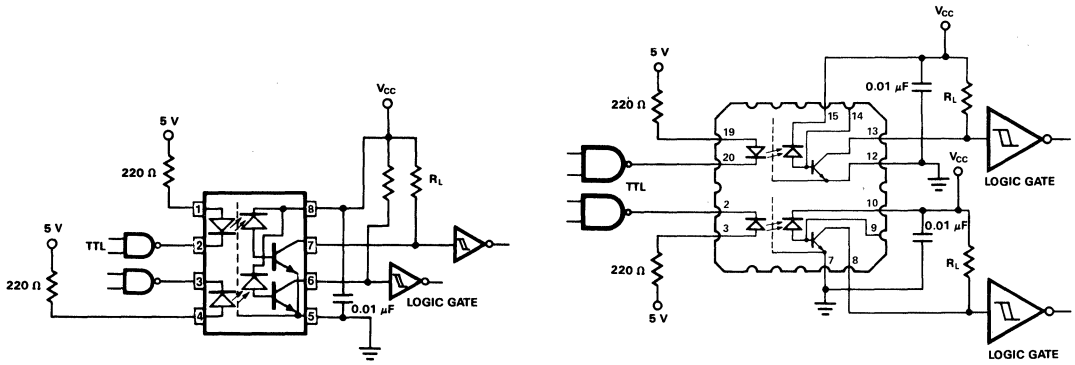


Figure. 10. Test Circuit for Transient Immunity and Typical Waveforms.



LOGIC FAMILY	LSTTL	CMOS	
DEVICE NO.	54LS14	CD40106BM	
V_{CC}	5V	5V	15 V
R_L 5% TOLERANCE	18 KΩ*	8.2 KΩ	22 KΩ

*THE EQUIVALENT OUTPUT LOAD RESISTANCE IS AFFECTED BY THE LSTTL INPUT CURRENT AND IS APPROXIMATELY 8.2 KΩ

This is a worst case design which takes into account 25% degradation of CTR. See App. Note 1002 to assess actual degradation and lifetime.

Figure 11. Recommended Logic Interface.

5962-9085401HPX 5962-8767902PX 5962-87679032A and MIL-H-38534 Class H Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-H-38534 and DESC SMD's 5962-90854 and 5962-87679.

Testing consists of 100% screening and quality conformance inspection to MIL-H-38534.

Part Numbering System

Commercial Product	Class H Product	DESC Product	Class K Product
HCPL-5500	HCPL-5501	5962-9085401HPX	TBD
HCPL-5530	HCPL-5531	5962-8767902PX	TBD
HCPL-6530	HCPL-6531	5962-87679032A	TBD

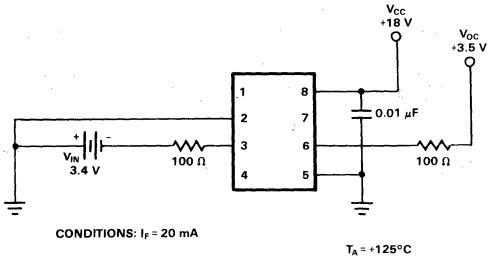


Figure 12. Single Channel Operating Circuit for Burn-In and Steady State Life Tests.

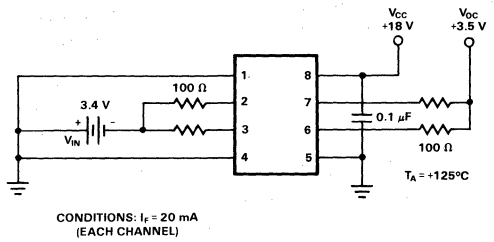


Figure 13. Dual Channel Operating Circuit for Burn-In and Steady State Life Tests.

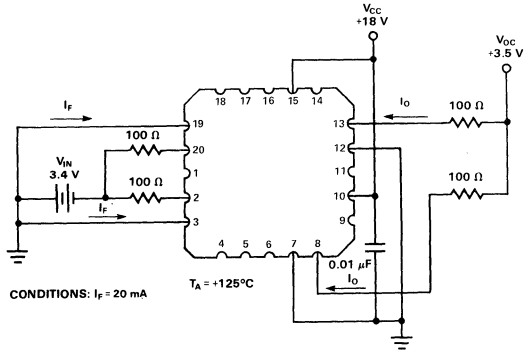


Figure 14. Operating Circuit for Burn-In and Steady State Life Tests.

Part Marking Orientation for HCPL-55XX and HCPL-65XX Base Product and Related DESC Products

HCPL-5500 ESD Class 1	HP Logo → HP P/N → Pin One/ → ESD Ident	HP YYWWZ HCPL-5500 ▲ USA	← Date Code, Suffix (if needed) ← Country of Mfr.
HCPL-5501 5962-9085401HPX* ESD Class 1	HP Logo → HP P/N → DESC SMD → DESC SMD → Pin One/ → ESD Ident	HP QYYWWZ 5501/883B 5962-90854 01HPX USA ▲ 50434	← Compliance Indicator, Date Code, Suffix (if needed) ← Country of Mfr. ← HP FSCN
HCPL-5530 ESD Class 3	HP Logo → HP P/N → Pin One/ → ESD Ident	HP YYWWZ HCPL-5530 ● USA	← Date Code, Suffix (if needed) ← Country of Mfr.
HCPL-5531 5962-8767902PX* ESD Class 3	HP Logo → HP P/N → DESC SMD → DESC SMD → Pin One/ → ESD Ident	HP QYYWWZ 5531/883B 5962-87679 02PX USA ● 50434	← Compliance Indicator, Date Code, Suffix (if needed) ← Country of Mfr. ← HP FSCN
HCPL-6530 ESD Class 1	Pin One/ → ESD Ident	YYWWZ ▲ USA HCPL-6530 HP	← Date Code, Suffix (if needed) ← Country of Mfr. ← HP P/N ← HP Logo
HCPL-6531 5962-87679032A ESD Class 1	HP Logo → HP P/N → Pin One/ → ESD Ident Country of Mfr. →	HP QYYWWZ 6531/883B ▲ 5962- 87679032A USA 50434	← Compliance Indicator, Date Code, Suffix (if needed) ← DESC SMD ← DESC SMD ← HP FSCN

*"X" is not marked on device. Replace "X" with "C" for gold lead finish; Replace "X" with "A" for solder lead finish.

HEWLETT PACKARD

New

90 V/1.0 Ω, Hermetically Sealed, Power MOSFET Optocoupler

Technical Data

HSSR-7110

Features

- **Hermetically Sealed 8-Pin Dual In-Line Package**
- **Small Size and Weight**
- **Performance Guaranteed over -55°C to +125°C Ambient Temperature Range**
- **Compact Solid-State Bidirectional Switch**
- **ac/dc Signal & Power Switching**
- **Connection A 0.8 A, 1.0 Ω**
- **Connection B 1.6 A, 0.25 Ω**
- **1500 Vdc Withstand Test Voltage**
- **High Transient Immunity**
- **5 Amp Output Surge Current**
- **Shock and Vibration Resistant**

Applications

- **Military/High Reliability Systems**
- **Standard 28 Vdc and 48 Vdc Load Driver**
- **Standard 24 Vac Load Driver**
- **Aircraft Controls**
- **ac/dc Electromechanical and Solid State Relay Replacement**
- **I/O Modules**

Description

The HSSR-7110 is a single channel, hermetically sealed, power MOSFET optocoupler. The device operates exactly like a solid-state relay. The product is capable of operation and storage over the full military temperature range and can be purchased as a standard product (HSSR-7110), or with special testing (QSSR-71XX). All products are in eight-pin, hermetic, dual in-line, ceramic packages.

As of December 1992, Hewlett-Packard has started to qualify this manufacturing line to MIL-STD-1772 and to be listed on QML-MIL-H-38534. Upon completion, a compliant part identified as HSSR-7111 will be available and will meet Class H test level of MIL-STD-883 (see note below).

The part is normally shipped with gold plated leads. Solder dipped leads are available by adding option #200 to the part number.

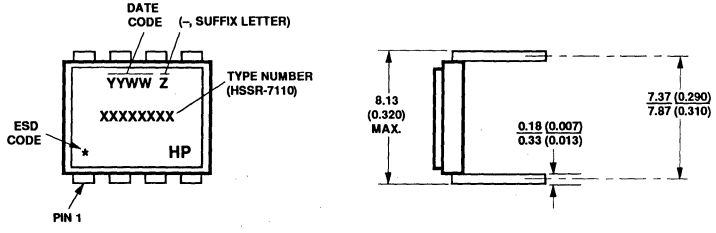
The device contains an AlGaAs light emitting diode optically coupled to a photovoltaic diode stack which drives two discrete n-channel enhancement mode power MOSFETs. The device operates as a solid-state replacement for single-pole, normally open, (1 Form A) relays used for general purpose switching of signals and loads in high reliability applications.

The part's logic level input control and very low output on-resistance makes it suitable for both ac and dc loads. Connection A, as shown in the schematic, allows the unit to switch either ac or dc loads. Connection B, with the polarity and pin configuration as indicated in the schematic, allows the device to switch dc loads only. The advantage of Connection B is that the on-resistance is significantly reduced, and the output current capability increases by a factor of two.

NOTE: Contact your local Hewlett-Packard field sales office for the availability of the HSSR-7111.

Outline Drawings and Schematic

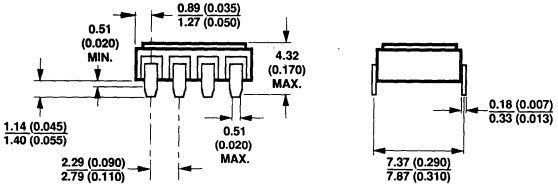
8-pin Ceramic Dual In-Line Package



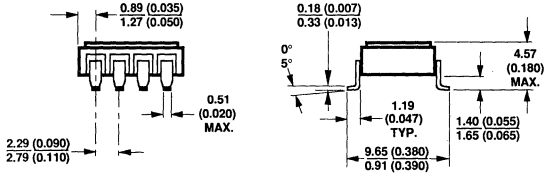
DIMENSIONS IN MILLIMETERS AND (INCHES).

8-PIN CERAMIC DUAL IN-LINE PACKAGE
TYPICAL WEIGHT: 0.7 GRAMS

Butt-Joint Surface Mount Option 100



Gull-Wing Surface Mount Option 300



The device is a convenient replacement for mechanical and solid state relays where high component reliability in standard footprint lead configuration is desirable. The eight pin dual in-line package allows easy board construction with both through hole and surface mount methods. Butt joint and gull wing lead options are available by ordering option #100 or #300 respectively (see Outline Drawings).

The HSSR-7110 is designed to switch loads on 28 Vdc power systems. It meets 80 V surge and ±600 V spike requirements. The part is suitable for military applications.

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Ambient Temperature – T_A ..... -55°C to +125°C
Junction Temperature – T_J ..... +150°C
Operating Case Temperature – T_C ..... +145°C[1]
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Input Current – I_F ..... 20 mA
Peak Repetitive Input Current – I_{FPK} ..... 40 mA
(Pulse Width < 100 ms; duty cycle < 50%)
Peak Surge Input Current – I_{FPK} surge ..... 100 mA
(Pulse Width < 0.2 ms; duty cycle < 0.1%)
Reverse Input Voltage – V_R ..... 5 V
Average Output Current – Figure 2
Connection A – I_O ..... 0.8 A
Connection B – I_O ..... 1.6 A
Single Shot Output Current – Figure 3
Connection A – I_{OPK} surge (Pulse width < 10 ms) ..... 5.0 A
Connection B – I_{OPK} surge (Pulse width < 10 ms) ..... 10.0 A
Output Voltage
Connection A – V_O ..... -90 V to +90 V
Connection B – V_O ..... 0 V to +90 V
Average Output Power Dissipation – Figure 4 ..... 800 mW[2]

Thermal Resistance

Maximum Output MOSFET Junction to Case – θ_{JC} = 15°C/W

Demonstrated ESD Performance

Human Body Model: MIL-STD-883 Method 3015.7 – Class 2

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current (on)	$I_{F(ON)}$	5	20	mA
Input Voltage (off)	$V_{F(OFF)}$	0	0.6	Volt
Operating Temperature	T_A	-55	+125	°C

Electrical Specifications

T_A =-55°C to +125°C, unless otherwise specified.

Parameter	Connection	Sym.	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Notes
Output Withstand Voltage		$\|V_{O(OFF)}\|$	90	110		V	V_F = 0.6 V, I_O = 250 µA,	5	
Output On-Resistance	A	$R_{(ON)}$		0.40	1.0	Ω	I_F = 10 mA, I_O = 800 mA, (pulse duration ≤ 30 ms)	6,7	3
	B			0.12	0.25		I_F = 10 mA, I_O = 1.6 A, (pulse duration ≤ 30 ms)		
Output Leakage Current		$I_{O(OFF)}$		10^{-4}	250	µA	V_F = 0.6 V, V_O = 90 V,	8	
Input Forward Voltage		V_F	1.0	1.24	1.7	V	I_F = 10 mA	9	
Input Reverse Breakdown Voltage		V_R	5.0			V	I_R = 10 µA		
Input-Output Insulation		I_{I-O}			1.0	µA	RH ≤ 45%, t = 5 s, V_{I-O} = 1500 Vdc, T_A = 25°C		4,5
Turn On Time		t_{ON}		1.25	6.0	ms	I_F = 10 mA, V_{DD} = 28 V, I_O = 800 mA	1,10, 11,12, 13	6
Turn On Time With Peaking		t_{ON}		0.22		ms	I_{FPK} = 100 mA, I_{FSS} = 10 mA V_{DD} = 28 V, I_O = 800 mA	1	
Turn Off Time		t_{OFF}		0.02	0.25	ms	I_F = 10 mA, V_{DD} = 28 V, I_O = 800 mA	1,10, 14,15	
Output Transient Rejection		$\left\|\frac{dVo}{dt}\right\|$	1000			V/µs	V_{PEAK} = 50 V, C_M = 1000 pF, C_L = 15 pF, $R_M \geq 1$ MΩ	17	
Input-Output Transient Rejection		$\left\|\frac{dVio}{dt}\right\|$	500			V/µs	V_{DD} = 5 V, $V_{I-O(PEAK)}$ = 50 V, R_L = 20 kΩ, C_L = 15 pF	18	

*All typical values are at T_A = 25°C, $I_{F(ON)}$ = 10 mA, $V_{F(OFF)}$ = 0.6 V unless otherwise specified.

Typical Characteristics

All typical values are at T_A = 25°C, $I_{F(ON)}$ = 10 mA, $V_{F(OFF)}$ = 0.6 V unless otherwise specified.

Parameter	Symbol	Test Conditions	Typ.	Units	Fig.	Notes
Output Off-Capacitance	$C_{O(OFF)}$	V_O = 28 V, f = 1 MHz	145	pF	16	
Output Offset Voltage	$\|V_{OS}\|$	I_F = 10 mA, I_O = 0 mA	2	µV	19	7
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	I_F = 10 mA	-1.4	mV/C		
Input Capacitance	C_{IN}	V_F = 0 V, f = 1 MHz	20	pF		8
Input-Output Capacitance	C_{I-O}	V_{I-O} = 0 V, f = 1 MHz	1.5	pF		4
Input-Output Resistance	R_{I-O}	V_{I-O} = 500 V, t = 60 s	10^{13}	Ω		4

Notes:

1. Maximum junction to case thermal resistance for the device is 15°C/W, where case temperature, T_C, is measured at the center of the package bottom.
2. For rating, see Figure 4. The output power P_O rating curve is obtained when the part is handling the maximum average output current I_O as shown in Figure 2.
3. During the pulsed R_{ON} measurement (I_O duration <30 ms), ambient (T_A) and case temperature (T_C) are equal.
4. Device considered a two terminal device: pins 1 through 4 shorted together and pins 5 through 8 shorted together.
5. This is a momentary withstand test, not an operating condition.
6. For a faster turn-on time, the optional peaking circuit shown in Figure 1 may be implemented.
7. V_{OS} is a function of I_F, and is defined between pins 5 and 8, with pin 5 as the reference. V_{OS} must be measured in a stable ambient (free of temperature gradients).
8. Zero-bias capacitance measured between the LED anode and cathode.

CAUTION: Maximum Switching Frequency – Care should be taken during repetitive switching of loads so as not to exceed the maximum output current, maximum output power dissipation, maximum case temperature, and maximum junction temperature.

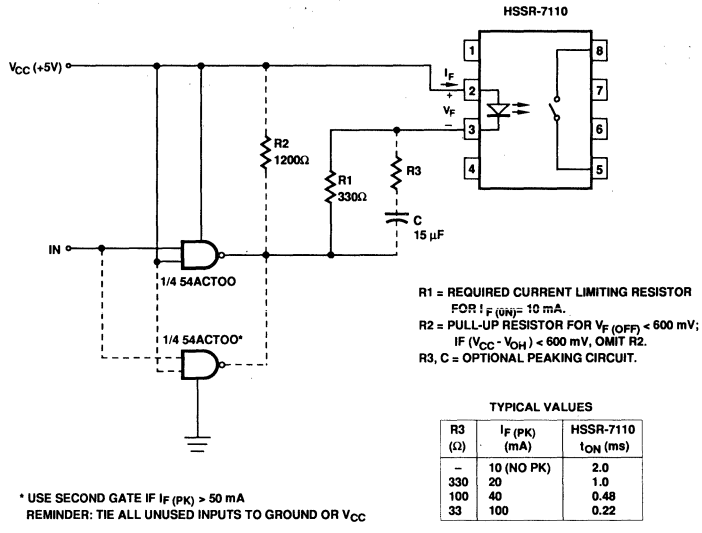


Figure 1. Recommended Input Circuit.

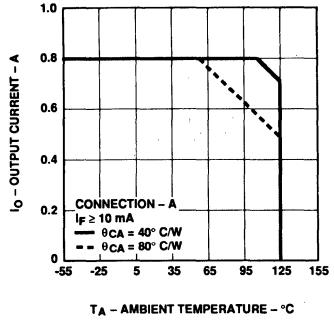


Figure 2. Maximum Average Output Current Rating vs. Ambient Temperature.

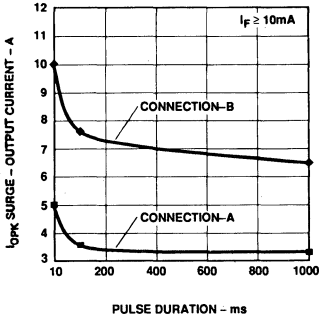


Figure 3. Single Shot (non-repetitive) Output Current vs. Pulse Duration.

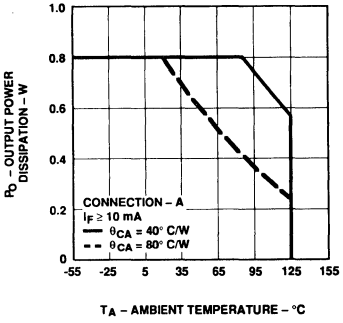


Figure 4. Output Power Rating vs. Ambient Temperature.

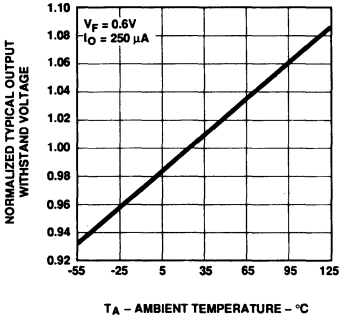


Figure 5. Normalized Typical Output Withstand Voltage vs. Temperature.

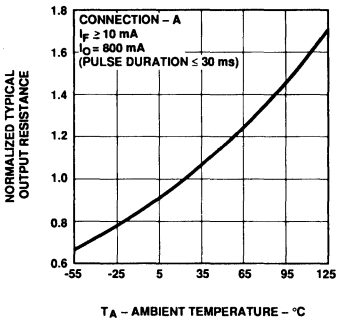


Figure 6. Normalized Typical Output Resistance vs. Temperature.

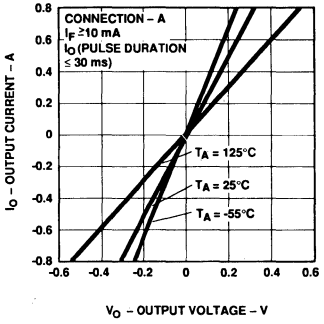


Figure 7. Typical On State Output I-V Characteristics.

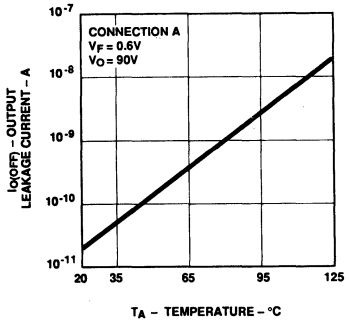


Figure 8. Typical Output Leakage Current vs. Temperature.

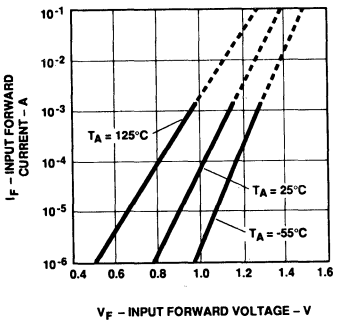


Figure 9. Typical Input Forward Current vs. Input Forward Voltage.

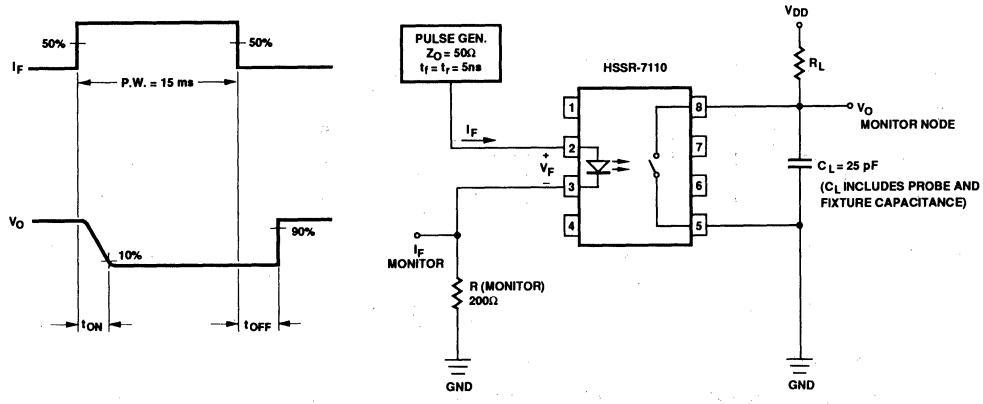


Figure 10. Switching Test Circuit for t_{ON}, t_{OFF}.

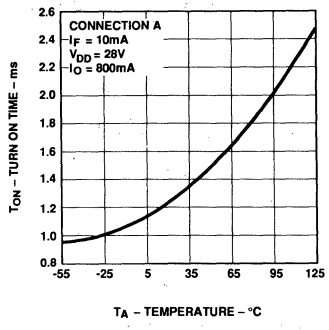


Figure 11. Typical Turn On Time vs. Temperature.

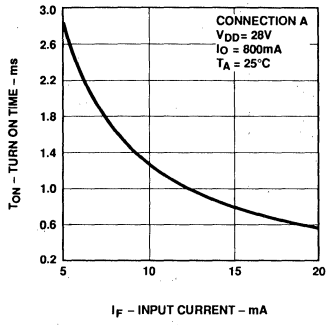


Figure 12. Typical Turn On Time vs. Input Current.

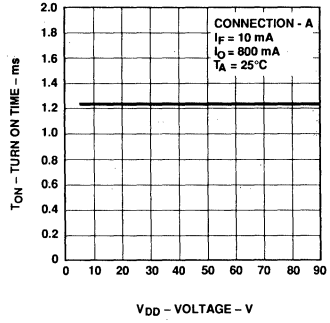


Figure 13. Typical Turn On Time vs. Voltage.

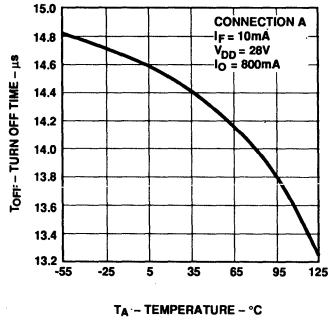


Figure 14. Typical Turn Off Time vs. Temperature.

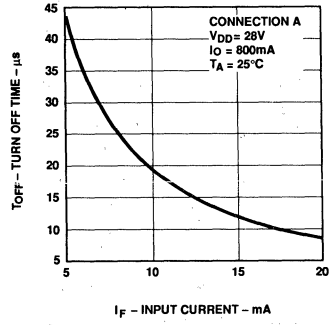


Figure 15. Typical Turn Off Time vs. Input Current.

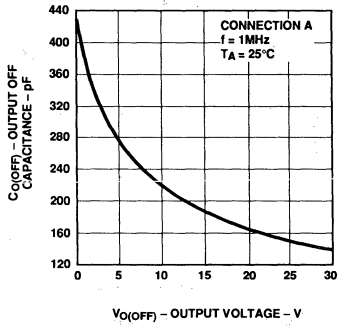
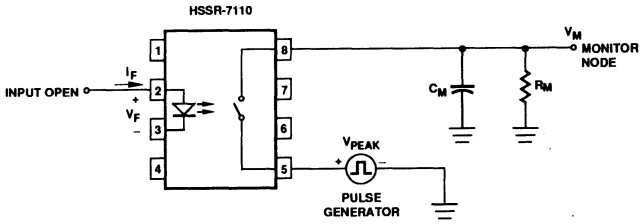
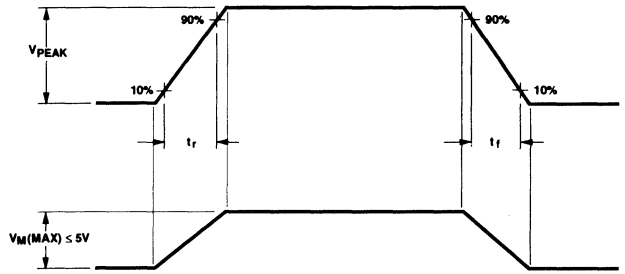


Figure 16. Typical Output Off Capacitance vs. Output Voltage.



C_M INCLUDES PROBE AND FIXTURE CAPACITANCE
R_M INCLUDES PROBE AND FIXTURE RESISTANCE



$$\frac{dV_o}{d_t} = \frac{(0.8)\,V_{(PEAK)}}{t_r} \text{ OR } \frac{(0.8)\,V_{(PEAK)}}{t_f}$$

OVERSHOOT ON V_{PEAK} IS TO BE ≤ 10%.

Figure 17. Output Transient Rejection Test Circuit.

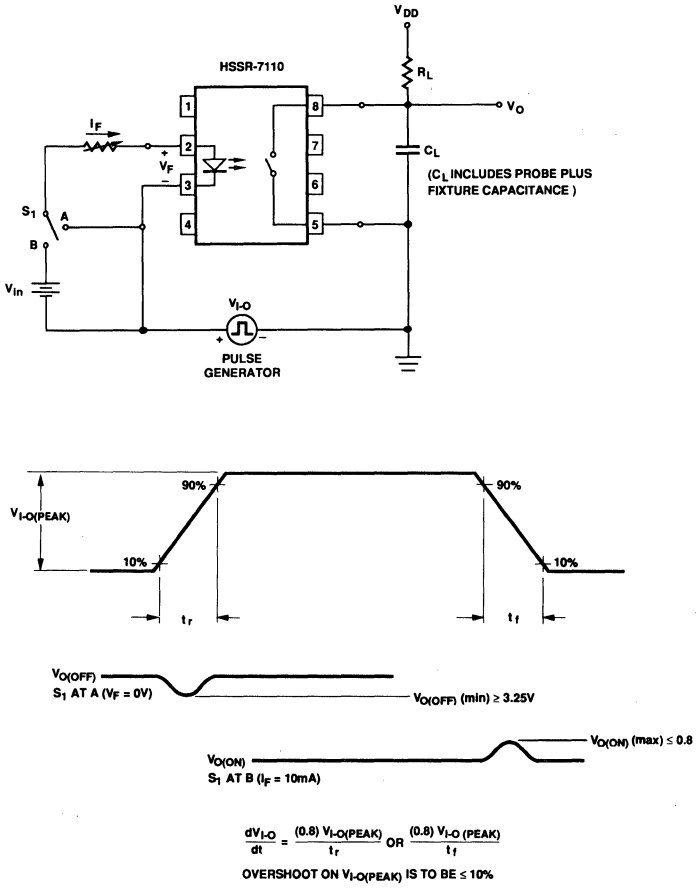


Figure 18. Input-Output Transient Rejection Test Circuit.

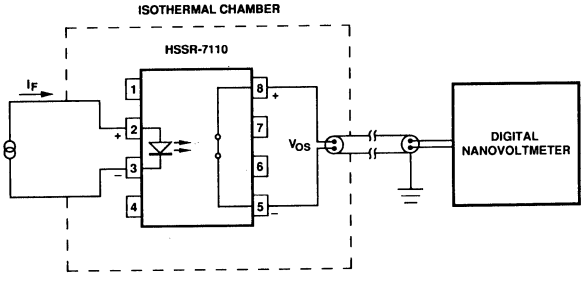


Figure 19. Voltage Offset Test Setup.

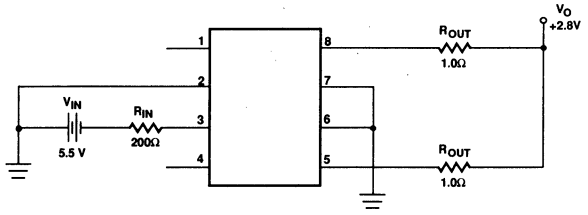
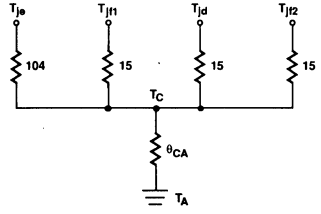


Figure 20. Burn-In Circuit.



T_{Je} = LED JUNCTION TEMPERATURE
T_{Jf1} = FET 1 JUNCTION TEMPERATURE
T_{Jf2} = FET 2 JUNCTION TEMPERATURE
T_{Jd} = FET DRIVER JUNCTION TEMPERATURE
T_C = CASE TEMPERATURE (MEASURED AT CENTER OF PACKAGE BOTTOM)
T_A = AMBIENT TEMPERATURE (MEASURED 6" AWAY FROM THE PACKAGE)
θ_{CA} = CASE-TO-AMBIENT THERMAL RESISTANCE

ALL THERMAL RESISTANCE VALUES ARE IN °C/W

Figure 21. Thermal Model.

Applications Information

Thermal Model

The steady state thermal model for the HSSR-7110 is shown in Figure 21. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. The thermal resistances between the LED and other internal nodes are very large in comparison with the other terms and are omitted for simplicity. The components do, however, interact indirectly through θ_{CA}, the case-to-ambient thermal resistance. All heat generated flows through θ_{CA}, which raises the case temperature T_C accordingly. The value of θ_{CA} depends on the conditions of the board design and is, therefore, determined by the designer.

The maximum value for each output MOSFET junction-to-case thermal resistance is specified as 15°C/W. The thermal resistance from FET driver junction-to-case is also 15°C/W. The power dissipation in the FET driver, however, is negligible in comparison to the MOSFETs.

On-Resistance and Rating Curves

The output on-resistance, R_{ON}, specified in this data sheet, is the resistance measured across the output contact when a pulsed current signal (I_O = 800 mA) is applied to the output pins. The use of a pulsed signal (≤ 30 ms) implies that each junction temperature is equal to the ambient and case temperatures. The steady-state resistance, R_{SS}, on the other hand, is the value of the resistance measured across the output contact when a DC current signal is applied to the output pins for a duration sufficient to reach thermal equilibrium. R_{SS} includes the effects of the temperature rise of each element in the thermal model.

Rating curves are shown in Figures 2 and 4. Figure 2 specifies the maximum average output current allowable for a given ambient temperature. Figure 4 specifies the output power dissipation allowable for a given ambient temperature. Above 55°C (for θ_{CA} = 80°C/W) and 107°C (for θ_{CA} = 40°C/W), the maximum allowable output current and power dissipation are related by the expression $R_{SS} = P_O(max)/(I_O(max))^2$ from which R_{SS} can be calculated. Staying within the safe area assures that the steady-state junction temperatures remain less than 150°C. As an example, for T_A = 95°C and θ_{CA} = 80°C/W, Figure 2 shows that the output current should be limited to less than 610 mA. A check with Figure 4 shows that the output power dissipation at T_A = 95°C and I_O = 610 mA, will be limited to less than 0.35 W. This yields an R_{SS} of .94 Ω.

HEWLETT PACKARD

Bar Code Components

- Digital Wands and Slot Readers
- Sensors and Sapphire Tips
- Intelligent Wands
- Digitizer and Decoder ICs

HEWLETT PACKARD

Bar Code Components

Bar Codes have gained wide acceptance in a myriad of applications where accuracy and expediency of data entry are important. Hewlett-Packard offers a broad line of quality bar code components. With an OEM focused business strategy, HP offers an extensive array of products ranging from optical reflective sensors, tips and decoder ICs to slot readers, digital bar code wands, and intelligent scanners. In essence, HP's family of bar code products are designed for ease of use, flexibility, integrity of design, and products with commitment to excellence in service, support, and reliability.

KeyWand Bar Code Readers

Package Outline Drawing	Part Number	Description	Features	Page No.
* 	HBKW-1010	HP KeyWand Bar Code Reader Wand Low Resolution (0.33mm) Compatible With: IBM PC, PC/XT, PC/AT	• Bar Code Scanning, Decoding and Keyboard-Emulated Output (For IBM PC's) Self-Contained Within Contact Scanning Wand • Automatic Recognition and Decode of 7 Standard Bar Code Symbologies • Optically Programmable Via Scanning of Bar Code Menus • Configuration Stored In Non-Volatile Memory • Rugged Polycarbonate Case • Powered From PC Keyboard Port • Automatic Recognition of Mode and Code Set for Most PC Models Kit Contains: - KeyWand Bar Code Reader Wand - Install & Operation Guide - Wand Holder	7-8
	HBKW-1015	HP KeyWand Bar Code Reader Kit		
	HBKW-1020	HP KeyWand Bar Code Reader Wand Low Resolution (0.33mm) Compatible With: IBM PS/2		
	HBKW-1025	HP KeyWand Bar Code Reader Kit		
	HBKW-1210	HP KeyWand Bar Code Reader Wand General Purpose (0.19mm) Compatible With: IBM PC, PC/XT, PC/AT HP KeyWand Bar Code Reader		
	HBKW-1215	HP KeyWand Bar Code Reader Kit		
	HBKW-1220	HP KeyWand Bar Code Reader Wand General Purpose (0.19mm) Compatible With: IBM PS/2		
	HBKW-1225	HP KeyWand Bar Code Reader Kit		
	HBKW-1410	HP KeyWand Bar Code Reader Wand High Resolution (0.13mm) Compatible With: IBM PC, PC/XT, PC/AT		
	HBKW-1415	HP KeyWand Bar Code Reader Kit		
	HBKW-1420	HP KeyWand Bar Code Reader Wand High Resolution (0.13mm) Compatible With: IBM PS/2		
	HBKW-1425	HP KeyWand Bar Code Reader Kit		

* Upgraded Intelligent Scanner with LED feedback. Available starting Fall 1993.

SmartWand Bar Code Readers

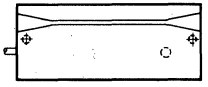
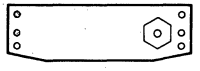
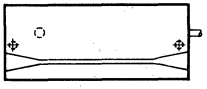
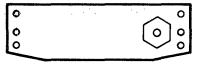
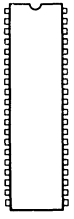
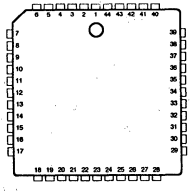
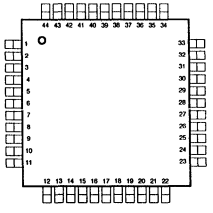
Package Outline Drawing	Part Number	Description	Features	Page No.
* 	HBSW-8000	HP SmartWand Programmable Contact Bar Code Reader Rugged Polycarbonate Case Low Resolution (0.33mm)	• Automatic Recognition and Decode of 7 Standard Bar Code Symbologies • +5V Serial Asynchronous Output • Flexible Programming Capability -Via Escape Sequences or -Optical Scanning of Bar Codes • Configuration Stored in Non-Volatile Memory • High Ambient Light Rejection (100K Lux) • Rugged Epoxy Coated Metal Case -Replaceable Tip (HBCS-4999) -25KV ESD Immunity -Force Required to Deform Case 181 Kg (400 lbs) • Rugged Polycarbonate Case -Replaceable Case (HBCS-A991) -15KV ESD Isolation -Force Required to Deform Case 100 Kg (220 lbs)	7-12
	HBSW-8100	HP SmartWand Programmable Contact Bar Code Reader Rugged Metal Case Low Resolution (0.33mm)		
* 	HBSW-8200	HP SmartWand Programmable Contact Bar Code Reader Rugged Polycarbonate Case Low Resolution (0.19mm)		
	HBSW-8300	HP SmartWand Programmable Contact Bar Code Reader Rugged Metal Case Low Resolution (0.19mm)		
* 	HBSW-8400	HP SmartWand Programmable Contact Bar Code Reader Rugged Polycarbonate Case Low Resolution (0.13mm)		
	HBSW-8500	HP SmartWand Programmable Contact Bar Code Reader Rugged Metal Case Low Resolution (0.13mm)		

* Upgraded Intelligent Scanner with LED feedback. Available starting Fall 1993.

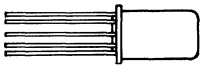
DigitalWand Bar Code Readers

Package Outline Drawing	Part Number	Description	Features	Page No.
	HBCS-A000	Low Current Digital Bar Code Wand (with Switch) Resolution 0.33mm	• Low Continuous Current Draw (Less Than 5 mA) • High Ambient Light Rejection • 0 to 45 degree Scan Angle • Push to Read Switch for Ultra Low Power Consumption • Rugged Polycarbonate Case • 15KV ESD Isolation • One Piece Case Design • Replaceable Case: -HBCS-A990 (Tool) -HBCS-A991 (Without Switch) -HBCS-A992 (With Switch) • Full Line of Options Available	7-16
	HBCS-A100	Low Current Digital Bar Code Wand (without Switch) Resolution 0.33mm		
	HBCS-A200	Low Current Digital Bar Code Wand (with Switch) Resolution 0.19mm		
	HBCS-A300	Low Current Digital Bar Code Wand (without Switch) Resolution 0.19mm		
	HBCS-A400	Low Current Digital Bar Code Wand (with Swithch) Resolution 0.13mm		
	HBCS-A500	Low Current Digital Bar Code Wand (without Switch) Resolution 0.13mm		
	HBCS-6100	Low Current Digital Bar Code Wand Resolution 0.33mm	• Low Continuous Current Draw (Less Than 5 mA) • 0 to 45 degree Scan Angle • Sealed Sapphire Tip • High Ambient Light Rejection • Sealed Sapphire Tip • Replaceable Tip (HBCS-4999) • Metal Case • 25KV ESD Immunity • Full Line of Options Available	
	HBCS-6300	Low Current Digital Bar Code Wand Resolution 0.19mm		
	HBCS-6500	Low Current Digital Bar Code Wand Resolution 0.13mm		

Slot Readers

Package Outline Drawing	Part Number	Description	Features	Page No.
	HBCS-7000	Industrial Digital Slot Reader, Visible Red (660nm) Resolution 0.19mm	•125 mil Slot Width •Epoxy Finished Metal Housing •Wide Scan Speed Range •Tamper Proof Design •Also Compatible with Low Resolution Bar Codes •Digital Output	7-23
	HBCS-7050	Optic/Electronics Module, Visible Red (660nm) Resolution 0.19mm		
	HBCS-7100	Industrial Digital Slot Reader, Infrared (880nm) Resolution 0.19mm		
	HBCS-7150	Optic/Electronics Module, Infrared (880nm) Resolution 0.19mm		
 40 Pin DIP  44 Pin PLCC  44 Pin QFP	New HBCR-1610 New HBCR-1611 New HBCR-1612	Single Chip Wand and Slot Reader (Digital Input) Bar Code Decoder IC	•Available in CMOS and either 40 Pin DIP, 44 Pin PLCC, or 44 Pin QFP Packages •Auto discriminates 5 Popular Bar Code Symbologies •Full Duplex Serial or Parallel ASCII Output •Program via Escape Sequences •Requires Single +5V Supply	7-49
	HBCR-2210 HBCR-2211	Wand and Laser Input Multi-Purpose Bar Code Decoder IC .	•Available in CMOS and either: 40 Pin Dip or 44 Pin PLCC Package. •Auto-discrimination of 7 Industry Standard Symbologies •Choice of Serial or Parallel Input/Output Capability •May be Programmed Either Optically (with a Wand) or via Escape Sequences •Input and Output Data Buffering •Requires a Single +5V Supply	7-60

Optional Reflective Sensors

Package Outline Drawing	Part Number	Description	Features	Page No.
	HBCS-1100	High Resolution Optical Reflective Sensor	• 0.19 mm (.0075 in.) Spot Size • Fully Specified and Guaranteed for Assured Performance • Visible (700 nm) Light Source Can Detect Most Colors • Photo IC Detector Optimizes Speed and Response • TO-5 Miniature Sealed Package	7-29
	New HEDS-1500	Precision Optical Reflective Sensor	• 0.178 mm (0.007 in.) Spot Size • Fully Specified and Guarenteed for Assured Performance • Visible Red (655 nm) Light Souce (Emitter) • Photodiode Output • TO-5 Miniature Sealed Package	7-43
	New HEDS-1200	Ultra High Resolution Optical Reflective Sensor	• 0.13 mm (0.005 in.) Spot Size • Fully Specified and Guarenteed for Assured Performance • Infrared (820 nm) Light Source • Photodiode Output • TO-5 Miniature Sealed Package	7-35
	New HEDS-1300	Similar to the HBCS-1100 with the Following Differences: – Different Pinout, Same as HEDS-1200 – Mechanical Baffle to Reduce Stray Light – Binned by Photocurrent	• 0.19 mm (.0075 in.) Spot Size • Fully Specified and Guaranteed for Assured Performance • Visible (700 nm) Light Source Can Detect Most Colors • Photo IC Detector Optimizes Speed and Response • TO-5 Miniature Sealed Package	

HEWLETT PACKARD

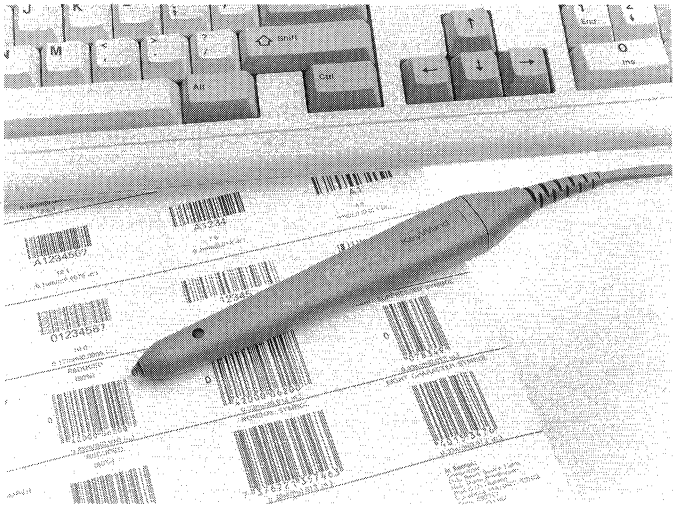
Hewlett-Packard KeyWand Bar Code Reader with Good Read LED Indicator

Technical Data

HBKW-1000 Series

Description

The HP KeyWand bar code reader lets you scan data directly into a personal computer via the keyboard interface, without hardware or software modification. All electronics are self-contained within the compact wand for clutter-free operation.



Features

- **Works with IBM Compatible Computers:**
  HP Vectra ES, RS, QS, 286, 386, 486
  IBM PC, PC/XT, PC/AT
  IBM PS/2
- **Operation With or Without the Keyboard Attached**
- **Powered from PC**
- **Bar Codes Read**
  Code 39/Extended Code 39
  Interleaved 2 of 5
  UPC A, E — EAN 8, 13
  Code 11 — Code 128
  MSI Code — Code 93
  Codabar
- **Programmable Via Bar Code Menus**
- **Rugged Polycarbonate Case**
- **15 KV ESD Case Isolation**
- **Automatic Recognition of Mode and Code Set for Most PC Models**

Applications

- **Manufacturing:**
  Work-in-process
  Inventory control
  Shipping and receiving
  Warehousing and distribution
- **Retail POS**
- **Library Circulation**
- **Office Automation:**
  Document tracking
- **Health Industry:**
  Medication dispensation
  Blood banks

Physical

Weight: 160 g (5.6 oz)
Color: Gray

Environmental

Operating Temp.: -20°C to 70°C
Storage Temp.: -40°C to 70°C

Relative humidity: 5% to 95% (non-condensing)

Ambient light: 100K lux (max)

Rain: MIL-STD-810, Method 506, Procedure II

Dust: MIL-STD-810, Method 510

Shock: Ten drops to sealed concrete (random orientation) from 1.2 meters (4 feet)

Typical Current Draw

Idle	10 mA
Operating:	20 mA
Δ LED ON	+11 mA

Wand Specifications

Tilt angle	5° to 40°
Scan speed	7.6 to 127 cm/s (3 to 50 in/s)
Min. contrast	45%

Light Wavelength

HBKW-10xx	655 nm
HBKW-12xx	655 nm
HBKW-14xx	820 nm

Caps Lock Detection

The HP KeyWand reader detects the state of the Caps Lock key and sends data in the proper case, except for original PCs and PC/XTs.

Keyboard Languages

U.S. English	Finnish
U.K. English	French Canadian
French	Latin American
German	Norwegian
Italian	Portuguese
Spanish	Swedish
Dutch	Swiss French
Belgian	Swiss German
Danish	

FCC Certification

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with these instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- **Reorient or relocate the receiving antenna**
- **Increase the separation between the equipment and the receiver**
- **Connect the equipment into an outlet on a circuit different from that to which the receiver is connected**
- **Consult the dealer or an experienced radio/television technician for help**

Model	FCC Identification
HBKW-1000 Series	FCC ID: B94KDRZ

Audible Feedback

The HP KeyWand bar code reader produces audible "good read" feedback by prompting the internal beeper resident in the host PC in one of two ways:

Method #1

The HP KeyWand reader is configured to send a beep code before transmitting its bar code data. The code is interpreted by the system BIOS as a keyboard buffer overflow condition, prompting the host personal computer to activate its own internal beeper (tone may vary). The beep code does not affect the bar code data and is removed by the BIOS.

The pitch and duration of the tone can be modified by using an uploadable TSR program that is resident in the HP KeyWand reader. This program, KWCAF.EXE, is needed for reliable beep operation with some PCs.

Method #2

The HP KeyWand reader can be configured to output a header message before the bar code data. The application software can utilize these header characters to activate feedback.

Visible Feedback

A green LED will flash to indicate good reads, successful scanning of configuration labels, successful powering up, and will flash an error code if anything fails in the KeyWand Reader.

Wand Configuration

The HP KeyWand bar code reader can be configured by scanning special bar code labels. This allows decoding options and interface protocols to be tailored to a specific application. The configuration is stored in nonvolatile memory and cannot be changed by removing power from the wand or by scanning standard bar code labels. The HP KeyWand reader may be reconfigured at any time to accommodate changing application requirements.

Configuration labels with detailed instructions on how to use them are printed in the HP KeyWand Installation and Operation Guide (Part #HBKW-1910).

```
                              CONFIGURATION DISPLAY
--- Version 14.3 ------------------------- (c) Hewlett-Packard 1986-1992
  CODE    |READ |CHECK CHAR |  LENGTH  | CODE ID  |  OTHER CONFIG. SETTINGS
          |     |verif_xmit_|min__max|xmit:[off]|-------------------------
Code 39   |[yes]|[no]  | yes |[1]  [32]|   [a]    |Extended: [no]
Int. 2/5  |[yes]|[no]  | yes |[4]  [32]|   [b]    |Length: [variable]
Codabar   |[yes]|[no]  | no  |[1]  [32]|   [d]    |Include start/stop: [yes]
Code 128  |[yes]| yes  | no  |[1]  [32]|   [e]    |
Code 11   |[yes]| [1]  | yes |[2]  [32]|   [f]    |
MSI Code  |[yes]| yes  | yes |[3]  [32]|   [g]    |
Code 93   |[yes]| yes  | no  |[1]  [32]|   [h]    |
UPC/EAN   |[yes]| yes  | yes |  fixed  |   [c]    |[+ none]
 E:[0]    |     |      |     |         |          |EAN:[yes]   ID chars:[off]
----- MESSAGE COMPONENTS ------------------------------------------------
      Ctrl character = ^ + letter       <<nn>> = Extended Key Index
Header:[<<61>>]
Trailer:[^M]
No-read:[<<61>><<61>>]
--- KEYCODES ----------OPERATOR FEEDBACK----------- MISCELLANEOUS -------
Key Delay:[1] ms  |Ready Signal:[on]          |[Wedge] (using keyboard)
[U.S. English]    |Menu Scan Responses:[on]   |No-read recognition:[off]
Code Set:[auto]->2|Good Read LED:[flashes]    |Family:[auto]->PC/AT,PS/2
ALT Sequence:[off]|                           |Cntl Chars:[ASCII]
-------------------------------------------------------------------------
```

The wand can display its current configuration on the computer's screen. See example above. All items within the square brackets [ ] are configurable.

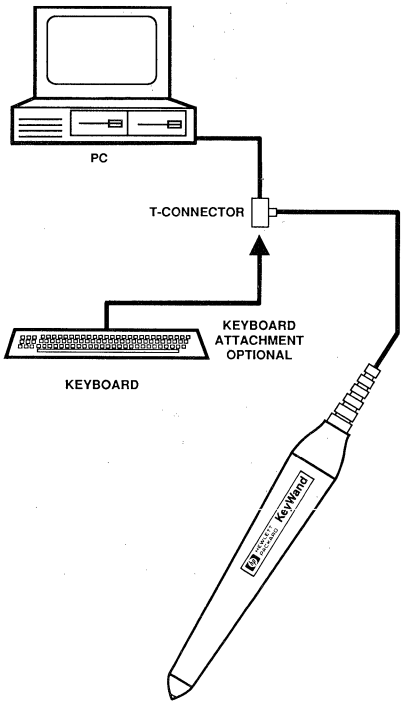
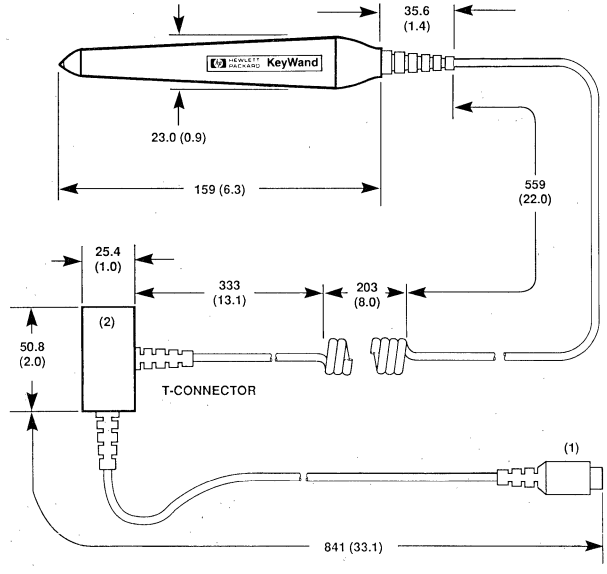


Figure 1. System Configuration



NOMINAL DIMENSIONS IN MILLIMETERS (INCHES)

HBCK-1010/1210/1410	(1)	MALE 5-PIN DIN CONNECTOR
	(2)	FEMALE 5-PIN DIN SOCKET
HBCK-1020/1220/1420	(1)	MALE 6-PIN MINI DIN CONNECTOR
	(2)	FEMALE 6-PIN MINI DIN SOCKET

Figure 2. Wand Dimensions

Selection Guide

General Purpose Wands

- Narrow Element width 0.19 mm (0.0075 in) or greater
- Label types include:
  - Dot Matrix (>9 wire)
  - Direct thermal
  - Thermal transfer
- The general purpose wand is appropriate for most bar code applications

Low Resolution Wands

- Narrow Element width 0.33 mm (0.013 in) or greater
- Label types include:
  - Dot Matrix (9 wire)
  - Small spots and voids
  - Lower contrast

High Resolution Wands

- Narrow Element width 0.13 mm (0.005 in) or greater
- Label types include:
  - High Density Labels
  - Infrared security labels
  - Thermal transfer

Warranty and Service

The Hewlett-Packard KeyWand Bar Code Reader is warranted for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Ordering Information

HP KeyWand Bar Code Reader Kit

- HP KeyWand Bar Code Reader
- Installation and Operations Guide (HBKW-1910)
- Wand Holder (HBKW-1920)

5 Pin DIN Connector	**HP Vectra ES, RS, QS IBM PC, PC/XT, PC/AT**
HBKW-1215	Kit iwth HBKW-1210 General Purpose Wand
HBKW-1015*	Kit with HBKW-1010 Low Resolution Wand
HBKW-1415*	Kit with HBKW-1410 Low Resolution Wand
6 Pin Mini-DIN Connector	**Vectra 286, 386, 486 IBM PS/2 Models**
HBKW-1225	Kit with HBKW-1220 General Purpose Wand
HBKW-1025*	Kit with HBKW-1020 Low Resolution Wand
HBKW-1425*	Kit with HBKW-1420 Low Resolution Wand
Universal KeyWand Kit	
HBKW-1240	Will work with either 5-pin or 6-pin PCs. Same as HBCK-1215 with adapter connectors (HBKW-1925)

Items Ordered Separately

HBKW-1210	General Purpose Wand, 5 Pin DIN Connector
HBKW-1220	General Purpose Wand, 6 Pin mini-DIN Connector
HBKW-1010*	Low Resolution Wand, 5 Pin DIN Connector
HBKW-1020*	Low Resolution Wand, 6 Pin mini-DIN Connector
HBKW-1410*	High Resolution Wand, 5 Pin DIN Connector
HBKW-1420*	High Resolution Wand, 6 Pin mini-DIN Connector
HBKW-1910	Installation and Operation Guide
HBKW-1920	Wand Holder
HBKW-1925	Adapter Connectors (DIN <-> Mini-DIN)
HBKW-1991	Replacement Tip/Case
HBCS-A990	Case Replacement Tool

*Note: Low and High Resolution KeyWand Readers are build to order devices.

HEWLETT PACKARD

HP Programmable Metal and Polycarbonate SmartWand Bar Code Reader (with Good Read LED Indicator)

Technical Data

Polycarbonate	Metal
HBSW-8000	HBSW-8100
HBSW-8200	HBSW-8300
HBSW-8400	HBSW-8500

Features

- **Automatically Decodes 8 Bar Code Symbologies**
- **Programmable Either by Bar Code Labels or Via Escape Sequences**
- **Program Stored in Non-Volatile Memory**
- **CMOS Interface**
  - Output 0 to 5 volts
  - Input up to ±15 volts
- **Polycarbonate SmartWand**
  - Good Read LED Indicator
  - 15 KV ESD Isolation
- **Metal SmartWand**
  - Rugged Industrial Design: 181 Kg (400 lbs) Force Required to Deform the Case
  - 25 KV ESD Immunity

Description

The Hewlett-Packard Programmable SmartWand Reader is an intelligent peripheral designed to easily add bar code scanning capability to any host system which can support a 5 volt serial asynchronous interface. A microprocessor, decoding software, optical and escape sequence programmability, non-volatile memory and a high performance contact scanner are integrated into a standard wand package. The HP SmartWand reader transmits decoded data in a serial ASCII format, freeing the host processor from the decoding task. The optics and electronics allow operation in a wide range of environments.

The HP SmartWand Reader automatically recognizes and decodes seven standard bar code symbologies. Code type identification, label length checking, and check character verification are options that when enabled ensure a high level of data integrity. There is a power on self test to ensure that the wand is operating properly.

Bar Codes Read

Code 39	Extended Code 39
Int. 2 of 5	Code 128
UPC A, E	EAN 8, 13
Codabar	Code 11
MSI Code	Code 93

Programmable Features

Bar code selection
Check character verification
Check character transmission
Serial Port baud rate
Serial Port parity
Serial Port pacing
Headers and terminators
Label length checking
No read recognition

Wand Specifications

Tilt Angle ..... 5° to 40°
Scan Speed ..... 7.6 to 127 cm/s (3 to 50 in/s)
Minimum Contrast 45%
Light Wavelength ..... 655 nm (8000, 8100, 8200, 8300 Wands)
Light Wavelength ..... 820 nm (8400, 8500 Wands)
Resolution:
8000, 8100 Wands ..... 0.33 mm (0.013 in)
8200, 8300 Wands ..... 0.19 mm (0.0075 in)
8400, 8500 Wands ..... 0.13 mm (0.005 in)

Environmental

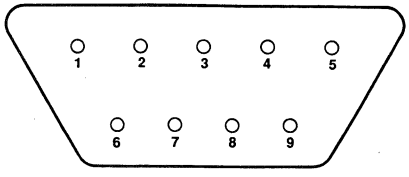
Temperature:
Operating:
-20°C to 70°C (-4°F to 158°F)
Non-operating:
-40°C to 70°C (-40°F to 158°F)

Relative Humidity:
(Non-condensing): 5% to 95%.

Ambient Light:
100,000 lux (maximum)

Pinout

Pin #	Function
2	TxD transmitted data (from the wand)
3	RxD received data (to the wand)
7	Ground
9	V_{cc}
Shell	Shield



MALE 9 PIN SUBMINIATURE D CONNECTOR

Electrical

V_{cc} Limits (V)

	Min	Max
Operating	4.5	6.0
Absolute Rating	-0.3	6.0

Typical I_{cc} (mA)

V_{cc} (V)	4.5	5.0	6.0
Idle	9	10	12
Scanning	14	16	20
Configuring	23	25	29

Visible Feedback

A green LED will flash to indicate good reads, successful scanning of configuration labels, successful powering up, and will flash an error code if anything fails in the SmartWand Reader.

FCC Certification

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with these instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and the receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/television technician for help

Model	HP SmartWand FCC Identification
HBSW-8xxx Series	FCCID: B94KDRZ

Wand Configuration

The HP SmartWand bar code reader can be configured by scanning special bar code labels. This allows decoding options and interface protocols to be tailored to a specific application. The configuration is stored in nonvolatile memory and cannot be changed by removing power from the wand or by scanning standard bar code labels. The HP SmartWand Reader may be reconfigured at any time to accommodate changing application requirements.

Configuration labels with detailed instructions on how to use them are printed in the HP SmartWand User's Manual (P/N: HBSW-8997).

CONFIGURATION DISPLAY

--- Version 12.5 ---------- (c) Hewlett-Packard 1986-1992

CODE	READ	CHECK CHAR		LENGTH		CODE ID	OTHER CONFIG. SETTINGS
		verif	xmit	min	max	xmit: [off]	
Code 39	[yes]	[no]	yes	[1]	[32]	[a]	Extended: [no]
Int. 2/5	[yes]	[no]	yes	[4]	[32]	[b]	Length: [variable]
Codabar	[yes]	[no]	no	[1]	[32]	[d]	Include start/stop: [yes]
Code 128	[yes]	yes	no	[1]	[32]	[e]	
Code 11	[yes]	[1]	yes	[2]	[32]	[f]	
MSI Code	[yes]	yes	yes	[3]	[32]	[g]	
Code 93	[yes]	yes	no	[1]	[32]	[h]	
UPC/EAN	[yes]	yes	yes	fixed		[c]	[+ none]
E: [0]							EAN: [yes] ID chars: [off]

--- MESSAGE COMPONENTS (control character = ^ + letter) ----------

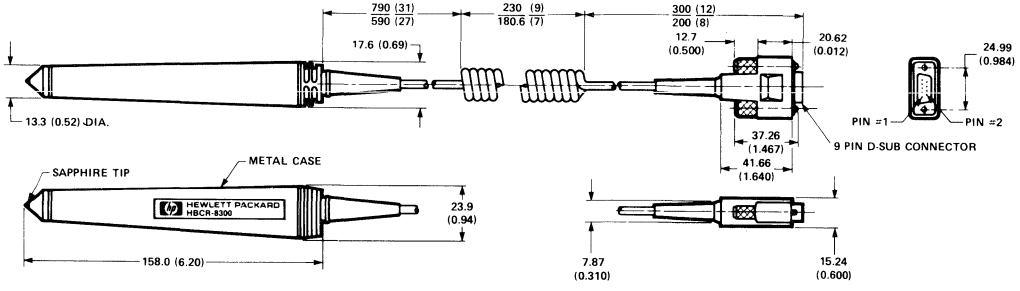
Header: []	No-read: []
Trailer: [^M^J]	Message Ready: [^F]
Reader Address: []	Message Not Ready: [^U]

-- SERIAL PORT --------- PACING ------------------- MISCELLANEOUS -------

Baud Rate: [9600]	XON/XOFF Protocol: [off]	No-Read Recognition: [off]
Parity: [0's]	Single Read Mode: [off]	Scanner: [enabled]
Stop Bits: [1]	----- FEEDBACK: [on] ------	Buffering: [None]
[20ms] Delay: [off]	LED: [flashes] Active: [high]	ROM/RAM Self Test: [off]

All items within the square brackets [ ] are configurable.

General Mechanical Specifications



NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES).

Selection Guide

General Purpose Wands

- Narrow Element width 0.19 mm (0.0075 in) or greater
- Label types include:
  - Dot Matrix (>9 wire)
  - Direct thermal
  - Thermal transfer
- The general purpose wand is appropriate for most bar code applications

Low Resolution Wands

- Narrow Element width 0.33 mm (0.013 in) or greater
- Label types include:
  - Dot Matrix (9 wire)
  - Small spots and voids
  - Lower contrast

High Resolution Wands

- Narrow Element width 0.13 mm (0.005 in) or greater
- Label types include:
  - High Density Labels
  - Infrared security labels
  - Thermal transfer

Warranty and Service

The Hewlett-Packard SmartWand is warranted for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective im material or workmanship under proper use during the warranty period.

NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Ordering Information
HP SmartWand Bar Code Reader Kit

- HP SmartWand Bar Code Reader
- User's Manual (HBSW-8997)
- Wand Holder (HBCS-2998)

Polycarbonate SmartWand Reader (with LED)

HBSW-8205	Kit with HBSW-8200 General Purpose Wand
HBSW-8005*	Kit with HBSW-8000 Low Resolution Wand
HBSW-8405*	Kit with HBSW-8400 Low Resolution Wand

Items Ordered Separately

HBSW-8200	General Purpose SmartWand with LED
HBSW-8000*	Low Resolution SmartWand with LED
HBSW-8400*	High Resolution Wand with LED
HBSW-8991	Replacement Tip/Case
HBCS-A990	Case Replacement Tool

Metal SmartWand Reader (without LED)

HBSW-8305	Kit with HBSW-8300 General Purpose Wand
HBSW-8105*	Kit with HBSW-8100 Low Resolution Wand
HBSW-8505*	Kit with HBSW-8500 Low Resolution Wand

Items Ordered Separately

HBSW-8300	General Purpose Metal SmartWand
HBSW-8100*	Low Resolution Metal SmartWand
HBSW-8500*	High Resolution Metal SmartWand
HBCS-4999	Replacement Tip

*Note: Low and High Resolution KeyWand Readers are build to order devices.

HEWLETT PACKARD

LOW CURRENT DIGITAL BAR CODE WANDS

METAL, LOW RESOLUTION	HBCS-6100
METAL, GENERAL PURPOSE RESOLUTION	HBCS-6300
METAL, HIGH RESOLUTION	HBCS-6500
POLYCARBONATE, LOW RESOLUTION	HBCS-A000/A100
POLYCARBONATE, GENERAL PURPOSE RESOLUTION	HBCS-A200/A300
POLYCARBONATE, HIGH RESOLUTION	HBCS-A400/A500

Features

- **ULTRA LOW CONTINUOUS CURRENT DRAIN**
  - **Less Than 4 mA Typical**
- **HIGH AMBIENT LIGHT REJECTION**
  - **Operates in Direct Sunlight**
- **AVAILABLE IN THREE RESOLUTIONS TO MEET A VARIETY OF SCANNING NEEDS**
- **VISIBLE RED (655 nm) AND INFRARED (820 nm) VERSIONS FOR READING A WIDE RANGE OF PRINTING TYPES AND COLORS**
- **SCAN ANGLE 0 TO 45 DEGREES TYPICAL**
- **INDUSTRIAL VERSION**
  - **Textured Metal Case**
  - **25 kV ESD Immunity**
- **COMMERCIAL VERSION**
  - **Polycarbonate Case**
  - **Switched or Unswitched**
  - **15 kV ESD Isolation**
- **OPERATING TEMPERATURE -20°C TO +65°C**
- **SEALED SAPPHIRE TIP**
  - **Provides protection from contamination due to dirt and debris**
- **DIGITAL OUTPUT**
  - **Open Collector Output Compatible with TTL and CMOS Logic**
- **SINGLE 5 VOLT SUPPLY**

Description

Hewlett-Packard's Low Current Digital Bar Code Wands are hand-held scanners optimized to provide excellent reading of all common bar code formats. The wands contain an optical sensor with a 655 nm visible red or 820 nm infrared LED; a photodetector IC; and precision aspheric optics. The internal signal conditioning circuitry converts the optical information into a logic level pulse width representation of the bars and spaces. All of the wands have a special circuit design that provides for extremely low current drain (less than 4 mA) with continuous operation. This makes them ideal for use on battery powered systems where low power drain will extend battery life. These wands also have excellent ambient light rejection, allowing full operation in direct sunlight, or brightly lit indoor environments.

Available in a choice of three resolutions, these wands have been designed to cover a wide range of bar code printing. The general purpose resolutionw ands, with their 0.19 mm (0.0075 in.) spot size, are excellent choices for reading a wide range of bar code symbols including dot matrix symbols. For reading very high density symbols, the high resolution wands with a 0.13 mm (0.005 in.) spot size, are the appropriate choice. For poorly printed low density symbols, the low resolution wands have a spot size of 0.33 mm (0.013 in.) to help reject extraneous spots and voids.

All of HP's Low Current Digital Bar Code Wands are FCC and VDE approved. They feature a shield for maximizing immunity to electrostatic discharge (ESD), electromagnetic interference (EMI) and ground loops. The unswitched polycarbonate case provides 15 kV EDS isolation, perfect for portable environments where static discharge could damage the operation of the host terminal. The shield is also designed to eliminate noise from capacitively coupled inputs.

The standard wand configuration includes a strain relieved coiled cord. The standard connector is a 5 pin, 240 degree DIN connector. On the metal wands the standard connector is the same, with the addition of a metal locking ring.

Applications

The digital bar code wand is a highly effective alternative to keyboard data entry. Bar code scanning is faster and more accurate than key entry and provides far greater throughput. In addition, bar code scanning typically has a higher first read rate and greater data accuracy than optical character recognition. When compared to magnetic stripe encoding, bar code offers significant advantages in flexibility of media, symbol placement, and immunity to electromagnetic fields.

Hewlett-Packard's Low Current Digital Bar Code Wands are especially designed for battery powered applications where low power drain is a primary concern. With continuous current draws of less than 4 mA, these wands can be used on battery powered systems without sacrificing battery life or requiring special "strobing" circuits. They are also ideal for AC powered systems where conventional wand current drains may require an increased power supply design. Switched wands are available to further reduce the power consumption. The switched wand may also be used to signal the host in a portable, one microprocessor based system.

In addition to their low current drain, these wands are also designed to work in high ambient light, such as outdoors or near large windows. This feature is extremely useful in applications such as inventory control on receiving docks, automobile tracking outdoors and check-out stands outdoors or near large store front windows.

Because the low resolution and the general purpose resolution wands use an emitter wavelength of 655 nm, they are extremely versatile in the range of printing type and colors that they will read, including thermal printing and dot matrix printing.

Available in either a light weight polycarbonate case or a rugged metal case, these wands are excellent choices for both light industrial and commercial applications, or heavy industrial and LOGMARS applications.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Nominal Narrow Element Width					
HBCS-A000/A100/6100		0.33 (0.013)		mm (in.)	
HBCS-A200/A300/6300		0.19 (0.0075)		mm (in.)	
HBCS-A400/A500/6500		0.13 (0.005)		mm (in.)	
Scan Velocity	V_{SCAN}	7.6 (3)	127 (50)	cm/sec (in/sec)	1
Contrast (Edge Contrast)	EC	40		%	2
Supply Voltage	V_S	4.5	5.5	Volts	3
Temperature	T_A	−20	+65	°C	
Ambient Light	E_V		100,000	lux	4
Orientation	(See Figure 2)				

Notes:

1. Narrow element width = 0.33 (0.013) mm (in.) and wide element width = 0.99 (0.039) mm (in.).
2. Contrast is defined as R_W-R_B where R_W is the reflectance of the white spaces and R_B is the reflectance of the black bars, measured at the emitter wavelength (655 nm or 820 nm). Contrast is related to print contrast signal (PCS) by PCS = $(R_W-R_B)/R_W$ or $R_W-R_B = PCS*R_W$.
3. Power supply ripple and noise should be less than 100 mV peak to peak.
4. Ambient light sources can be diffuse tungsten, sodium, mercury, fluorescent, sunlight, or a combination thereof.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	−40	+75	°C	
Operating Temperature	T_A	−20	+65	°C	
Supply Voltage	V_S	−0.5	+6.00	V	
Output Transistor Power	P_T		150	mW	
Output Collector Voltage	V_O	−0.5	+20	V	

Electrical Operation

The HBCS-6XXX/AXXX family of digital bar code wands consists of a precision optical sensor and an electronic circuit that creates a digital output of the bar code pattern. The open collector transistor requires only a pull-up resistor to provide a TTL compatible output from a single 4.5 V to 5.5 V DC power supply.

A non-reflecting black bar results in a logic high (1) level output, while a reflecting white space will cause a logic low (0) level output (see Figure 1). The initial state will be indeterminate. However, if no bar code is scanned, after a short period (typically less than 1 second), the wand will assume a logic low state. This feature insures that the first bar will not be missed in a normal scan, and allows for combining several wands by simple parallel wiring.

The wands provide a case, cable and connector shield which must be terminated to logic ground or, preferably, to both logic ground and earth ground. The shield is connected to the metal housing of the 5 pin DIN connector.

All standard HP Low Current Digital Bar Code wands are certified to meet FCC Class B and VDE Level B standards. The shield must be properly terminated in order to maintain these approvals and to keep the cable from acting as an antenna, injecting electrical noise into the wand circuitry. Grounding the shield will also provide a substantial improvement in EMI/ESD immunity.

The recommended logic interface for the wands is shown in Figure 5. This interconnection provides the maximum ESD protection for both the wand and the user's electronics.

Electrical Characteristics (T_A = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Notes
Supply Current	I_S		2.7	4.0	mA	V_S = 5.0 V	5, 6
High Level Output Current	I_{OH}			1.0	μA	V_{OH} = 2.4 V	
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA	
Output Rise Time	t_r		4.5	20	μs		7
Output Fall Time	t_f		0.3	20	μs		7
Switch Bounce — HBCS-A000/A200/A400	t_{sb}		0.5	5.0	ms		8
ESD Immunity — All Wands	ESD		25		kV		9
ESD Isolation — HBCS-A100/A300/A500	ESD		15		kV		10
ESD Isolation — HBCS-A000/A200/A400	ESD		8		kV		10
Wake-Up Time	t_w		50	200	ms		11

Notes:

5. Push to read switch (if applicable) is depressed.
6. Not including pull-up resistor current.
7. 10% tro 90% transistion. 1 kΩ pull-up resistor. See Figure 1.
8. Switch bounce causes a series of sub-millisecond pulses to appear at the output (V_O).
9. Shield must be properly terminated (see Figure 4). The human body is modeled by discharging a 300 pF capacitor through a 500 Ω resistor. No damage to the wand will occur at the specified discharge level.
10. No substantial discharge will occur at this level.
11. After this time, the wand is operational.

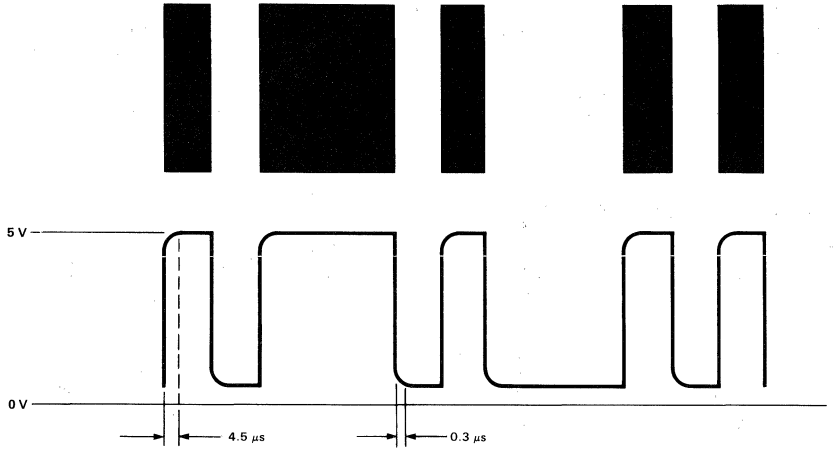


Figure 1. Typical Output Waveform

Testing

All Hewlett-Packard Digital Bar Code Wands are 100% tested for performance and digitizing accuracy after manufacture. This insures you of the consistent quality product you expect from HP. More information about our test procedures, test set-up, and test limits are available upon request. Reliability data sheet available upon request.

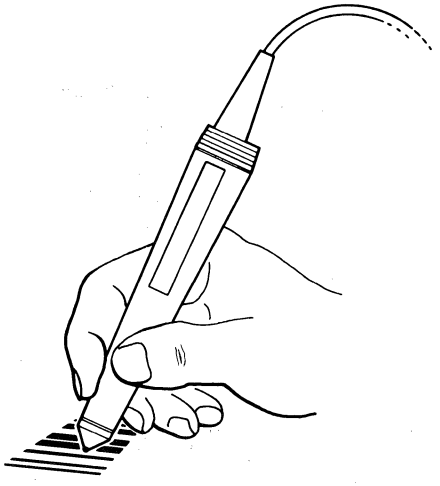


Figure 2. Preferred Orientation.

Selection and Application Guide

		Industrial			Commercial					
		HBCS 6100	**HBCS 6300**	**HBCS 6500**	**HBCS A000**	**HBCS A100**	**HBCS A200**	**HBCS A300**	**HBCS A400**	**HBCS A500**
Wavelength (nm)		655	655	820	655	655	655	655	820	820
Switch					X		X		X	
Nominal Narrow Element Width	(mm)	0.33	0.19	0.13	0.33	0.33	0.19	0.19	0.13	0.13
	(inch)	0.013	0.0075	0.005	0.013	0.013	0.0075	0.0075	0.005	0.005
Case Material	Polycarbonate				X	X	X	X	X	X
	Metal	X	X	X						
Will Read Bar Codes Printed Using	Regular Thermal Paper (Note 12)	X	X		X	X	X	X		
	Dye Based Inks (Note 12)	X	X		X	X	X	X		
	Carbon Based Inks (Notes 12, 13)	X	X	X	X	X	X	X	X	X
	Colors (Notes 12, 14)	X	X		X	X	X	X		
Best Choice For	Widest Range of Bar Code Printing		X				X	X		
	Highest Density Printing			X					X	X
	Low Density Poor Quality Printing	X			X	X				

Notes:

12. A blind spot may occur while scanning specular bar code labels with the wand at a 0 degree tilt angle.
13. For "black-on-black" security bar codes, use infrared (820 nm) wands only.
14. For color bar codes the background (spaces) should reflect red (655 nm) light, and the bars should absorb red light.

Certification

FCC Certification (USA Only)

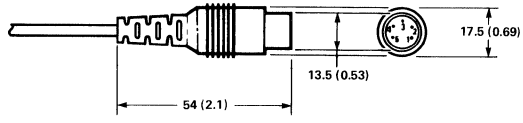
Model	FCC Identification
HBCS-6100 through -6199	FCC ID: B94600 HEWLETT-PACKARD
HBCS-6300 through -6399	FCC ID: B94600 HEWLETT-PACKARD
HBCS-6500 through -6599	FCC ID: B94600 HEWLETT-PACKARD
HBCS-A000 through -A099	FCC ID: B948JAHBCS-A000 HEWLETT-PACKARD
HBCS-A100 through -A199	FCC ID: B948JAHBCS-A100 HEWLETT-PACKARD
HBCS-A200 through -A299	FCC ID: B948JAHBCS-A200 HEWLETT-PACKARD
HBCS-A300 through -A399	FCC ID: B948JAHBCS-A300 HEWLETT-PACKARD
HBCS-A400 through -A499	FCC ID: B948JAHBCS-A400 HEWLETT-PACKARD
HBCS-A500 through -A599	FCC ID: B948JAHBCS-A500 HEWLETT-PACKARD

THIS DEVICE COMPLIES WITH PART 15 OF THE FCC RULES. OPERATION IS SUBJECT TO THE FOLLOWING TWO CONDITIONS: (1) THIS DEVICE MAY NOT CAUSE HARMFUL INTERFERENCE, AND (2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE RECEIVED, INCLUDING INTERFERENCE THAT MAY CAUSE UNDESIRED OPERATION.

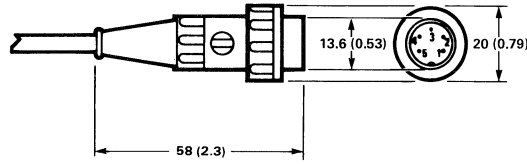
FCC Disclaimer

Hewlett-Packard products have received FCC certification for its standard configuration only. Any customer purchasing the product with stripped and tinned leads or a connector without adequate shielding has the responsibility to comply with FCC regulations. Moreover, if the Hewlett-Packard Low Current Digital Bar Code Wands are purchased without a connector, the product becomes defined as a subassembly and the FCC Identification number no longer applies. Hewlett-Packard assumes no responsibility or liability for users of the Hewlett-Packard Low Current Digital Bar Code Wands without connectors that fail to comply with FCC regulations.

Interface



HBCS-AXXX



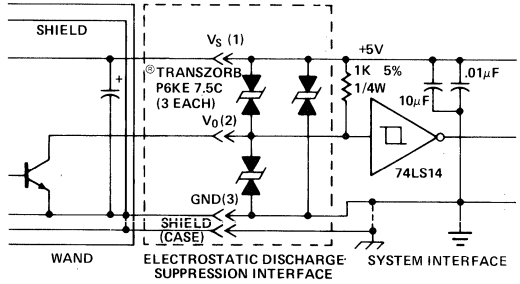
HBCS-6XXX

Note:

15. Dimensions are in millimeters and (inches).

PIN	Wire Color	Function
1	Red	V_S Power Supply
2	White	V_O Output
3	Black	Ground
4	N/A	No Connect
5	N/A	No Connect
Case	—	Shield (Must be connected)

Figure 3. Connector Specifications.



®TRANSZORB IS A REGISTERED TRADEMARK OF GENERAL SEMICONDUCTOR INDUSTRIES. TEMPE AZ.

Figure 4. Recommended Logic Interface for a fixed station host system. (When earth ground is not available, connect shield to logic ground, as shown by dotted line.) For portable devices, a larger valve pull-up resistor should be used to conserve power.

The wands include a standard 5 pin, 240° DIN connector, locking and non-locking for the HBCS-6000 series and the HBCS-A000 series, respectively. The detailed specifications and pin-outs are shown in Figure 3. Mating connectors are available from RYE Industries and SWITCHCRAFT in both 5 pin and 6 pin configurations. These connections are listed below.

Connector	Configuration
RYE MAB-5*	5 pin
SWITCHCRAFT 61GA5F*	5 Pin
SWITCHCRAFT 61HA5F	5 Pin
RYE MAB-6*	6 Pin
SWITCHCRAFT 61HA5F	6 Pin

*Suitable for non-locking connector only.

Ordering Guide

HBCS-6XXX	See "Selection and Application Guide" for part number determination.
HBCS-AXXX	See "Selection and Application Guide" for part number determination.
Opt-A01	Individually boxed wand with data sheet.
HBCS-4999	Replacement tip for the HBCS-6000 series wand family.
HBCS-A990	Disassembly tool for the HBCS-AXXX series wand family.
HBCS-A991	Replacement case kit for the HBCS-A100/A300/A500 wands.
HBCS-A992	Replacement case kit for the HBCS-A000/A200/A400 wands.

Maintenance Considerations

There are no user serviceable parts inside the wand. The tip of the 6000 series wands is designed to be easily replaceable, and if damaged, should be replaced. The part number for the replacement tip is HBCS-4999.

Like the 6000 series, the HBCS-A000 family series' case is designed for OEM replacement should damage occur to the tip or the case. A special tool has been designed to facilitate case removal (HBCS-A990). The case can be replaced with either the HBCS-A991 or HBCS-A992 case replacement kit for the unswitched or switched wand, respectively.

Before replacing the tip or the case, disconnect the wand from the system power source. The 6000 series tip, the A000 series' replacement case and disassembly tool can be ordered from any Hewlett-Packard authorized distributor.

Optional Features

For options such as special cords, connections or labels, contact your nearest Hewlett-Packard sales office or authorized representative.

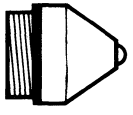


Figure 5. HBCS-4999 Sapphire Tip.

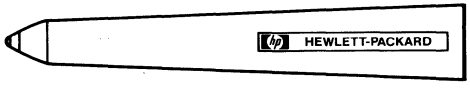


Figure 6. HBCS-A991 Replacement Case.

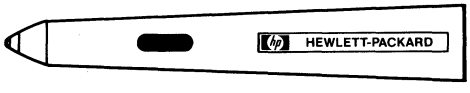


Figure 7. HBCS-A992 Replacement Case.

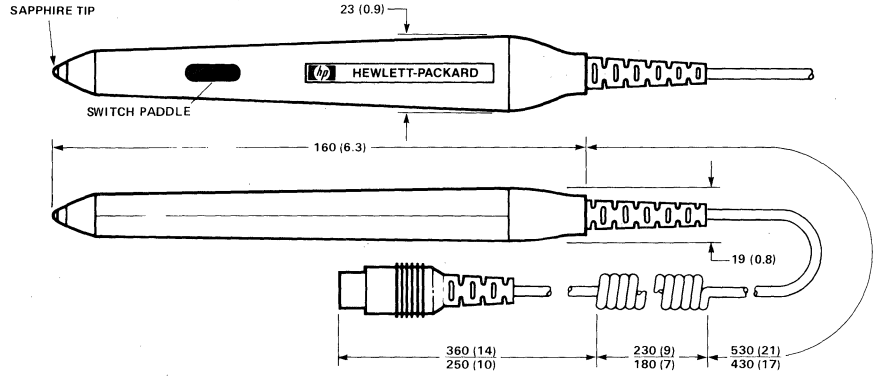
Warranty and Service

Hewlett-Packard Low Current Digital Bar Code Wands are warranteed for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair, or at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

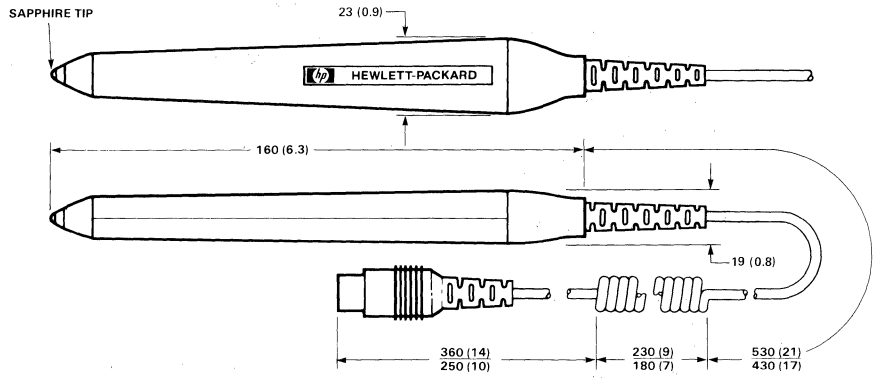
NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

For additional Warranty or service information please contact your local Hewlett-Packard sales representative or authorized distributor.

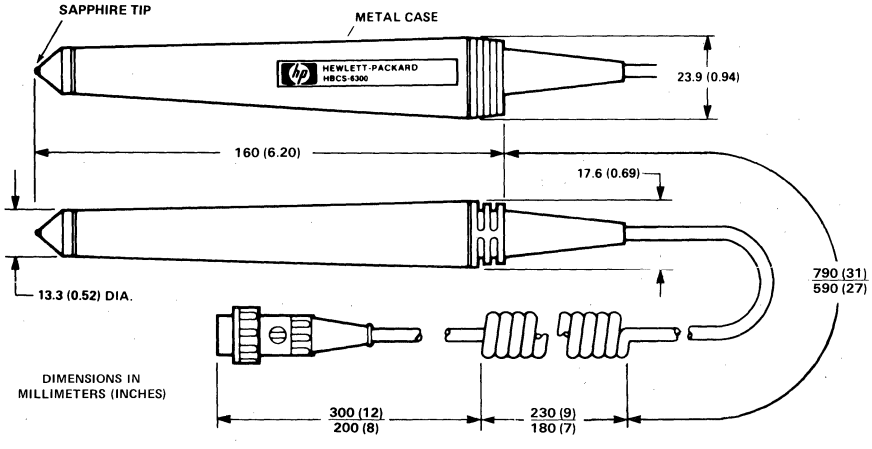
Wand Dimensions



HBCS-A000/A200/A400



HBCS-A100/A300/A500



HBCS-6100/6300/6500

Figure 8.

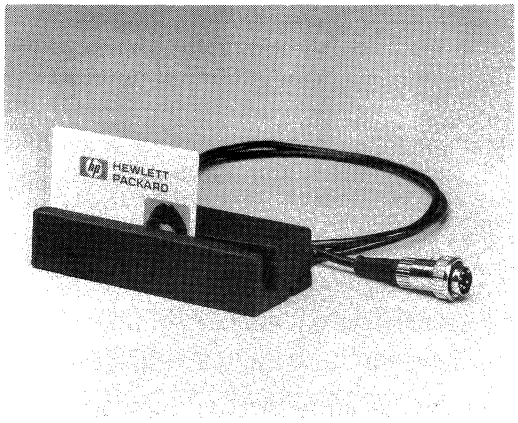
HEWLETT PACKARD

INDUSTRIAL DIGITAL BAR CODE SLOT READERS

HBCS-7000
HBCS-7050
HBCS-7100
HBCS-7150

Features

- **MULTI-RESOLUTION**
  - **— Compatible with Virtually All Bar Code Resolutions**
- **LARGE SLOT WIDTH**
  - **— Allows Reading Multiple Laminated Cards**
- **SEALED METAL CASE (IP 66/67)**
  - **— Can Be Installed Outdoors or in Wet Environments**
- **TAMPER PROOF DESIGN**
  - **— Ideal for Security Applications**
- **MINIMAL FIRST BAR DISTORTION**
  - **— Compatible with Most Decoding Software**
- **AVAILABLE IN EITHER VISIBLE 660 nm OR INFRARED 880 nm VERSIONS**
- **WIDE OPERATING TEMPERATURE RANGE**
  - **— -40 to 70° C (HBCS-7100)**
  - **— -20 to 55° C (HBCS-7000)**
- **WIDE SCAN SPEED RANGE**
- **BLACK TEXTURED EPOXY FINISH**
- **DIGITAL OUTPUT**
  - **— Open Collector Output Compatible with TTL and CMOS Logic**
- **SINGLE 5 VOLT SUPPLY**



Description

Hewlett-Packard's Industrial Digital Slot Readers are designed to provide excellent scanning performance on a wide variety of bar coded cards and badges. They contain a unique optical/electrical system that integrates over a large area of the bar/space pattern, providing a greatly improved first read rate even on poorly printed bar codes.

The HBCS-7000 has a visible red (660 nm) optical system with a resolution of 0.19 mm (0.0075 in.). The HBCS-7100 model has an infrared (880 nm) optical system with a resolution of 0.19 mm (0.0075 in.).

The extra large depth of field allows these slot readers to have a slot width of 3.2 mm (0.125 in.), thus making it possible to read even multiple laminated cards and badges. When used as a stand alone optics module, the maximum depth of field is dependent on resolution.

The optics and electronics are housed in a rugged metal case. The cases are fully gasketed and sealed, making them suitable for use in outdoor or wet environments. The black epoxy coating adds a durable, finished look to these Digital Slot Readers. When installed using the rear screw holes, the units become tamper-proof, making them excellent choices for security access control.

The optical system is centered in the slot track, allowing the user to easily scan from either direction. The wide slot width makes it easy to insert and slide the cards. The optical system is covered with a recessed window to prevent contamination and reduce the wear on the cards.

The standard slot reader comes with the optical/electrical asembly mounted on a base plate with an opposite rail. A 122 cm (48 in.) straight cord and a 5 pin, 240 degree, locking DIN connector are also standard.

The optical/electrical system is also available as a separate unit which can be integrated into other equipment or used as a stand alone sensor assembly.

Applications

The digital bar code slot reader is a highly effective alternative to keyboard data entry. Bar code scanning is faster and more accurate than key entry and provides far greater throughput. In addition, bar code scanning typically has a higher first read rate and greater data accuracy than optical character recognition. When compared to magnetic stripe encoding, bar code offers significant advantages in flexibility of media, symbol placement and immunity to electromagnetic fields.

Hewlett-Packard's Industrial Digital Slot Readers are designed for applications where high first read rate and durability are important factors. The epoxy coated metal case, with its tamper-proof mounting system, makes these slot readers ideal choices for security access control, time and attendance recording and other bar coded badge and card reading applications.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Nominal Narrow Element Width				
HBCS-7000/7050		0.19 (0.0075)		mm (in.)
HBCS-7100/7150		0.19 (0.0075)		mm (in.)
Scan Velocity[1]	V_{SCAN}	20 (8)	317 (125)	cm/sec (in. sec/)
Contrast[2]	R_W-R_B	45		%
Supply Voltage[3]	V_S	4.5	5.5	Volts
Temperature[4]				
HBCS-7000/7050	T_A	-20	+55	°C
HBCS-7100/7150	T_A	-40	+70	°C
Ambient Light[5]	E_V		100,000	lux

Notes:
1. Measured scanning a symbol with 0.19 mm (0.0075 in.) narrow elements. For larger narrow element widths, the maximum scan velocity will increase proportionately.
2. Contrast is defined as R_W-R_B where R_W is the reflectance of the white spaces and R_B is the reflectance of the black bars, measured at the emitter wavelength (660 nm or 880 nm). Contrast is related to print contrast signal (PCS) by PCS = $(R_W$-$R_B)/R_W$ or R_W-R_B = PCS x R_W.
3. Power supply ripple and noise should be less than 100 mV peak to peak.
4. Non-condensing. If there is frost or dew covering over the optics window, it should be removed for optimal scanning performance.
5. Direct sunlight at any illumination angle.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-40	+80	°C
Supply Voltage	V_S	-0.3	+7.0	Volts
Output Transistor Power	P_T		200	mW
Output Collector Voltage	V_O	-0.3	+20	Volts

WARNING:
OBSERVING THE INFRARED LIGHT SOURCE IN THE HBCS-7150 AT CLOSE DISTANCES FOR PROLONGED PERIODS OF TIME MAY CAUSE INJURY TO THE EYE. When mounted with the rail in place, the infrared output flux is radiologically safe. With the rail removed, precautions should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

Electrical Operation

The HBCS-7XXX family of digital slot readers consists of a precision optical system, an analog amplifier, a digitizing circuit, and an output transistor. These elements provide a TTL compatible output from a single 4.5 V to 5.5 V DC power supply. The open collector transistor requires a pull-up resistor for proper operation.

A non-reflecting black bar results in a logic high (1) level output, while a reflecting white space will cause a logic low (0) level output. After power-up, the slot reader will be fully operational after a period of approximately 6 seconds. During operation, the slot reader will assume a logic low state after a short period (typically 1 second) if no bar code is scanned. This feature allows multiple scanners (both slot readers and Hewlett-Packard sapphire tip wands) to be connected together with a simple OR gate.

The slot reader connector provides a shield which should be terminated to logic ground or, preferably, to both logic ground and earth ground. The shield is connected to the metal housing of the 5 pin DIN connector, the metal housing of the slot reader, and logic ground inside the slot reader.

The recommended logic interface for the slot reader is shown in Figure 1. This interface provides ESD protection for both the slot reader and the user's electronics.

The maximum recommended cable length for the slot reader's output is 25 feet.

Electrical Characteristics (V_S = 4.5 V to 5.5 V, T_A = 25° C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current						
HBCS-7000/7050	I_S		50	100	mA	V_S = 5.0 V
HBCS-7100/7150	I_S		65	100	mA	V_S = 5.0 V
High Level Output Current	I_{OH}			1.0	μA	V_{OH} = 2.4 V
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Output Rise Time	t_r		0.9	5.0	μs	10%-90% Transition R_L = 1K Ω
Output Fall Time	t_f		0.07	5.0	μs	
Electrostatic Discharge Immunity[6]	ESD		25		kV	

Notes:
6. Shield must be properly terminated (see Figure 1). The human body is modeled by discharging a 300 pF capacitor through a 500 Ω resistor. No damage to the slot reader will occur at the specified discharge level.

Interface Specifications

The slot readers include a standard 5 pin, 240°, metal, locking DIN connector. The recommended logic interface is shown in Figure 1. The mechanical specifications and wiring are shown in Figure 2. Mating connectors are available from SWITCHCRAFT in both 5 pin and 6 pin configurations. These connectors are listed on the right.

Connector	Configuration
SWITCHCRAFT 61HA5F	5 Pin
SWITCHCRAFT 13EL5F	5 Pin
SWITCHCRAFT 61HA6F	6 Pin

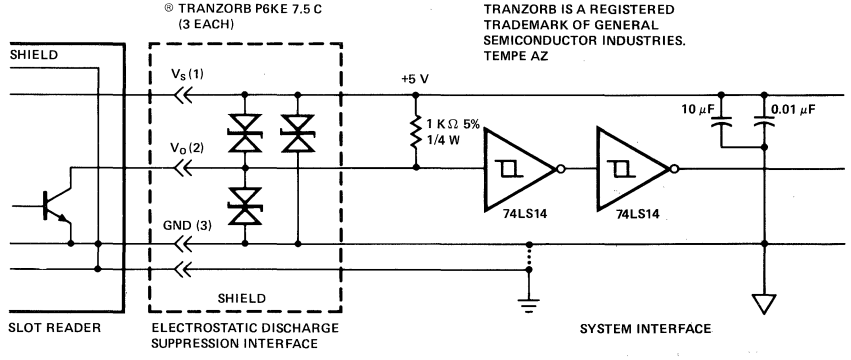
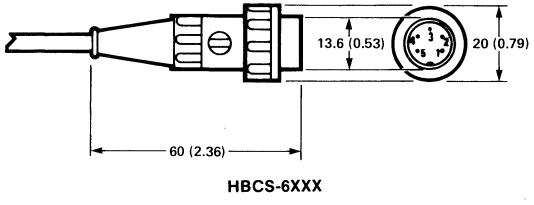


Figure 1. Recommended Logic Interface (When earth ground is not available, connect shield to logic ground, as shown by dotted line).



HBCS-6XXX

PIN	WIRE COLOR	FUNCTION
1	RED	V_S SUPPLY VOLTAGE
2	WHITE	V_O OUTPUT
3	BLACK	GROUND
4	N/A	N/C
5	N/A	N/C
CASE	-	SHIELD (MUST BE CONNECTED)

NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).

Figure 2. Connector Specifications.

Mounting Considerations

Slot Reader

The slot reader (HBCS-7000/7100) is designed to be virtually tamper-proof when mounted using the two rear mounting holes. In this case, the cable must be routed from the rear of the slot reader through the mounting surface (wall, door, etc.). For applications where a tamper-proof installation is less of a concern, an optional mounting bracket (HBCS-7999) allows for more convenient surface mounting.

When mounting the slot reader, the cable may either be routed through the mounting surface (see above), or it may be routed along grooves in the base and exit the side of the slot reader at any one of four points. This allows flexibility in the mounting orientation.

Optics/Electronics Module

The optics/electronics module (HBCS-7050/7150) is designed for applications which require a different slot width, integration into a larger housing, or a fixed-beam stationary scanner. When using the optics/electronics module, the operating distance from the front surface of the module to the symbol will vary depending on the symbol resolution. Figure 3 shows the relationship between operating range and *minimum* symbol resolution for a typical optics/electronics module. This relationship was applied in the design of the slot reader, where a slot width of 3.2 mm (0.125 in.) insures excellent performance reading bar code symbols which have a *nominal* resolution of 0.19 mm (0.0075 in.) and include printing errors.

When mounting the optics/electronics module it is important that the screws be tightened with a minimum static torque of 2.5 Nm (22 in.-lbs.). This will insure that the sealing gasket is compressed sufficiently to provide proper sealing.

Rail

The rail (HBCS-7998) is designed for use with the optics/electronics module in applications which require a different slot width. It may also be used in applications where it is preferable to mount the optics/electronics module and rail flush to the mounting surface instead of using the base provided with the slot reader.

Mounting Bracket

The mounting bracket (HBCS-7999) is designed to provide a convenient way of mounting the slot reader, optics/electronics module, and/or rail to a flat surface.

Symbol Placement

The center of the slot reader's optical system is located 12.7 mm (0.50 in.) from the bottom of the slot. Consequently, bar code symbols to be read by the slot reader must be positioned on the card(s) or document(s) at a height which insures that all bars and spaces will cross a line located 12.7 mm (0.50 in.) from the bottom edge of the card(s) or document(s). For optimal performance, all bars and spaces should cross the area between 1.14 mm (0.45 in.) and 1.40 mm (0.55 in.) from the bottom edge of the card(s) or document(s).

The bars should be perpendicular to the bottom edge of the card(s) or document(s), however, a skew of ±4 degrees from the perpendicular is acceptable.

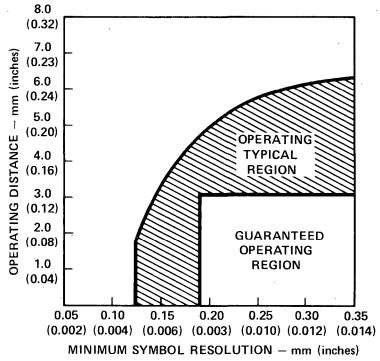


Figure 3. Typical Operating Distance vs. Minimum Symbol Resolution.

Maintenance Considerations

The slot reader and optics/electronics module include a window which is slightly recessed in order to prevent direct contact with the bar code symbol. This reduces wear on both the window and the symbol. The window may, however, become dirty over a period of time. If this occurs, clean the window with a commercial glass cleaner.

Testing

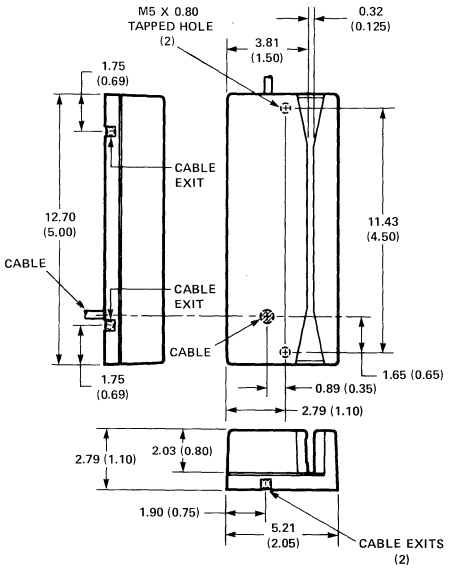
All Hewlett-Packard Digital Bar Code Slot Readers are 100% tested for performance and digitizing accuracy after manufacture. This insures a consistent quality product. More information about Hewlett-Packard's test procedures, test set-up, and test limits are available upon request.

Optional Features

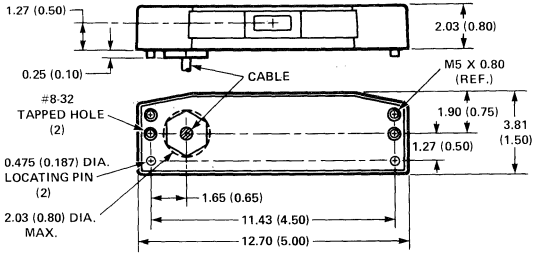
For options such as special cables or connectors, contact your nearest Hewlett-Packard sales office or authorized representative.

Dimensions

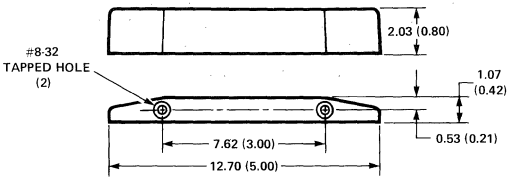
SLOT READER (HBCS-7000/7100)



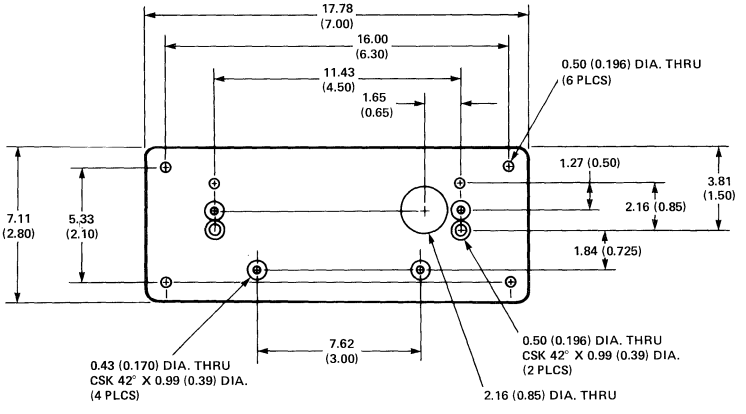
OPTICS/ELECTRONICS MODULE (HBCS-7050/7150)



RAIL (HBCS-7998)



MOUNTING BRACKET (HBCS-7999)



NOTES:
1. MOUNTING HOLES ON HBCS-7000/7100 ARE SUITABLE FOR EITHER #10-32 OR M5-0.80 SCREWS.
2. MOUNTING HOLES ON HBCS-7050/7150 ARE FOR #8-32 SCREWS.
3. MOUNTING HOLES ON HBCS-7998 ARE FOR #8-32 SCREWS.
4. THICKNESS OF THE HBCS-7999 MOUNTING BRACKET IS 3.2 mm (0.125 in.)
5. HBCS-7000/7100 SLOT READERS, HBCS-7050/7150 MODULES, AND HBCS-7998 RAILS HAVE A BLACK TEXTURED EPOXY FINISH. HBCS-7999 MOUNTING BRACKETS HAVE AN ELECTROLESS NICKEL FINISH.
6. ALL DIMENSIONS ARE NOMINAL AND ARE STATED IN MILLIMETRES AND (INCHES).

Selection Guide

Part Number	Description
HBCS-7000	Slot Reader with 660 nm visible red light source and 0.19 mm (0.0075 in.) nominal resolution.
HBCS-7100	Slot Reader with 880 nm infrared light source and 0.19 mm (0.0075 in.) nominal resolution.
HBCS-7050	Optics/Electronics Module with 660 nm visible red light source and 0.19 mm (0.0075 in.) nominal resolution.
HBCS-7150	Optics/Electronics Module with 880 nm infrared light source and 0.19 mm (0.0075 in.) nominal resolution.
HBCS-7998	Rail for use with the HBCS-7050/7150 (optional)
HBCS-7999	Mounting Bracket (optional)

Warranty and Service

HP Bar Code Slot Reader is warranted for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

For additional warranty or service information please contact your local Hewlett-Packard sales representative or authorized distributor.

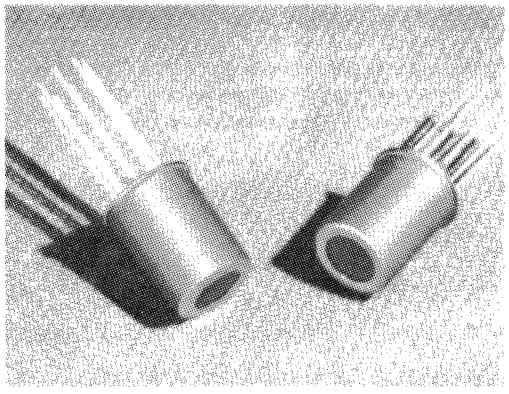
HEWLETT PACKARD

HIGH RESOLUTION OPTICAL REFLECTIVE SENSOR

HBCS-1100

Features

- **FOCUSED EMITTER AND DETECTOR IN A SINGLE PACKAGE**
- **HIGH RESOLUTION — .190mm SPOT SIZE**
- **700nm VISIBLE EMITTER**
- **LENS FILTERED TO REJECT AMBIENT LIGHT**
- **TO-5 MINIATURE SEALED PACKAGE**
- **PHOTODIODE AND TRANSISTOR OUTPUT**
- **SOLID STATE RELIABILITY**



Description

The HBCS-1100 is a fully integrated module designed for optical reflective sensing. The module contains a .178mm (.007 in.) diameter 700nm visible LED emitter and a matched I.C. photodetector. A bifurcated aspheric lens is used to image the active areas of the emitter and the detector to a single spot 4.27mm (0.168 in.) in front of the package. The reflected signal can be sensed directly from the photodiode or through an internal transistor that can be configured as a high gain amplifier.

Applications

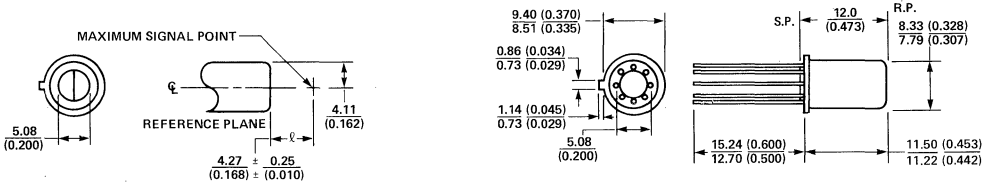
Applications include pattern recognition and verification, object sizing, optical limit switching, tachometry, textile thread counting and defect detection, dimensional monitoring, line locating, mark, and bar code scanning, and paper edge detection.

Mechanical Considerations

The HBCS-1100 is packaged in a high profile 8 pin TO-5 metal can with a glass window. The emitter and photodetector chips are mounted on the header at the base of the package. Positioned above these active elements is a bifurcated aspheric acrylic lens that focuses them to the same point.

The sensor can be rigidly secured by commercially available two piece TO-5 style heat sinks, such as Thermalloy 2205, or Aavid Engineering 3215. These fixtures provide a stable reference platform and their tapped mounting holes allow for ease of affixing this assembly to the circuit board.

Package Dimensions



NOTES:
1. ALL DIMENSIONS IN MILLIMETERS AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. THE REFERENCE PLANE IS THE TOP SURFACE OF THE PACKAGE.
4. NICKEL CAN AND GOLD PLATED LEADS.
5. S.P. SEATING PLANE.
6. THE LEAD DIAMETER IS 0.45mm (0.018in.) TYP.

BAR CODE PRODUCTS

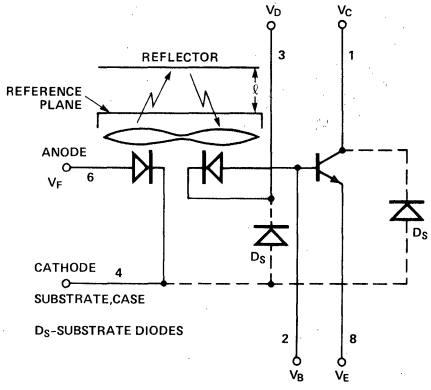
Electrical Operation

The detector section of the sensor can be connected as a single photodiode, or as a photodiode transistor amplifier. When photodiode operation is desired, it is recommended that the substrate diodes be defeated by connecting the collector of the transistor to the positive potential of the power supply and shorting the base-emitter junction of the transistor. Figure 15 shows photocurrent being supplied from the anode of the photodiode to an inverting input of the operational amplifier. The circuit is recommended to improve the reflected photocurrent to stray photocurrent ratio by keeping the substrate diodes from acting as photodiodes.

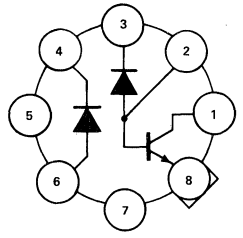
The cathode of the 700nm emitter is physically and electrically connected to the case-substrate of the device. Applications that require modulation or switching of the LED should be designed to have the cathode connected to the electrical ground of the system. This insures minimum capacitive coupling of the switching transients through the substrate diodes to the detector amplifier section.

The HBCS-1100 detector also includes an NPN transistor which can be used to increase the output current of the sensor. A current feedback amplifier as shown in Figure 6 provides moderate current gain and bias point stability.

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



TOP VIEW

PIN	FUNCTION
1	TRANSISTOR COLLECTOR
2	TRANSISTOR BASE, PHOTODIODE ANODE
3	PHOTODIODE CATHODE
4	LED CATHODE, SUBSTRATE, CASE
5	NC
6	LED ANODE
7	NC
8	TRANSISTOR EMITTER

Absolute Maximum Ratings at T_A=25°C

Parameter	Symbol	Min.	Max.	Units	Fig.	Notes
Storage Temperature	T_S	-40	+75	°C		
Operating Temperature	T_A	-20	+70	°C		
Lead Soldering Temperature 1.6mm from Seating Plane			260 for 10 sec.	°C		11
Average LED Forward Current	I_F		50	mA		2
Peak LED Forward Current	I_{FPK}		75	mA	1	1
Reverse LED Input Voltage	V_R		5	V		
Package Power Dissipation	P_P		120	mW		3
Collector Output Current	I_O		8	mA		
Supply and Output Voltage	V_D,V_C,V_E	-0.5	20	V		10
Transistor Base Current	I_B		5	mA		
Transistor Emitter Base Voltage	V_{EB}		.5	V		

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be introduced by ESD.

System Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Total Photocurrent (I_{PR}+I_{PS})	I_P			575	nA	T_A=-20°C	2,3	4
		150	250	375		T_A=25°C, I_F=35mA, V_D=V_C=5V		
		80				T_A=70°C	15	
Reflected Photocurrent (I_{PR}) to Internal Stray Photocurrent (I_{PS})	$\frac{I_{PR}}{I_{PS}}$	4	8.5			I_F=35mA, V_C=V_D=5V	3	
Transistor DC Static Current Transfer Ratio	h_{FE}	50				T_A=-20°C	4,5	
		100	200			T_A=25°C, V_{CE}=5V, I_C=10μA		
Slew Rate			.08		V/μs	R_L=100K, I_{PK}=50mA, R_F= 10M, t_{ON}=100μs, Rate = 1kHz	6	
Image Diameter	d		.17		mm	I_F=35mA, ℓ=4.27mm (0.168in.)	8,10	8,9
Maximum Signal Point	ℓ	4.01	4.27	4.52	mm	Measured from Reference Plane	9	
50% Modulation Transfer Function	MTF		2.5		$l_{npr/mm}$	I_F=35mA, ℓ =4.27mm	10,11	5,7
Depth of Focus	$\frac{\Delta\ell}{FWHM}$		1.2		mm	50% of I_P at ℓ=4.27mm	9	5
Effective Numerical Aperature	N.A.		.3					
Image Location	D		.51		mm	Diameter Reference to Centerline ℓ=4.27mm		6
Thermal Resistance	Θ_{JC}		85		°C/W			

Detector Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Dark Current	I_{PD}		5	200	pA	T_A=25°C, I_F=0, V_D=5V; Reflection=0%		
				10	nA	T_A=70°C		
Capacitance	C_D		45		pF	V_D=0V, I_P=0, f=1MHz		
Flux Responsivity	$R\phi$		.22		$\frac{A}{W}$	λ=700nm, V_D=5V	12	
Detector Area	A_D		.160		mm^2	Square, with Length=.4mm/Side		

Emitter Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Forward Voltage	V_F		1.6	1.8	V	I_F=35mA	13	
Reverse Breakdown Voltage	BV_R	5			V	I_R=100μA		
Radiant Flux	ϕ_E	5	9.0		μW	I_F=35mA, λ=700nm	14	
Peak Wavelength	λ_p	680	700	720	nm	I_F=35mA	14	
Thermal Resistance	Θ_{JC}		150		°C/W			
Temperature Coefficient of V_F	$\Delta V_F/\Delta T$		-1.2		mV/°C	I_F=35mA		

Transistor Electrical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Collector-Emitter Leakage	I_{CEO}		1		nA	V_{CE}=5V		
Base-Emitter Voltage	V_{BE}		.6		V	I_C=10μA, I_B=70nA		
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$		.4		V	I_B=1μA, I_E=10μA		
Collector-Base Capacitance	C_{CB}		.3		pF	f=1MHz, V_{CB}=5V		
Base-Emitter Capacitance	C_{BE}		.4		pF	f=1MHz, V_{BE}=0V		
Thermal Resistance	Θ_{JC}		200		°C/W			

NOTES:
1. 300μs pulse width, 1 kHz pulse rate.
2. Derate Maximum Average Current linearly from 65°C by 6mA/°C.
3. Without heat sinking from T_A = 65°C, derate Maximum Average Power linearly by 12mW/°C.
4. Measured from a reflector coated with a 99% reflective white paint (Kodak 6080) positioned 4.27mm (0.168 in.) from the reference plane.
5. Peak-to-Peak response to black and white bar patterns.
6. Center of maximum signal point image lies within a circle of diameter D relative to the center line of the package. A second emitter image (through the detector lens) is also visible. This image does not affect normal operation.
7. This measurement is made with the lens cusp parallel to the black-white transition.
8. Image size is defined as the distance for the 10%-90% response as the sensor moves over an abrupt black-white edge.
9. (+) indicates an increase in the distance from the reflector to the reference plane.
10. All voltages referenced to Pin 4.
11. CAUTION: The thermal constraints of the acrylic lens will not permit the use of conventional wave soldering procedures. The typical preheat and post cleaning temperatures and dwell times can subject the lens to thermal stresses beyond the absolute maximum ratings and can cause it to defocus.

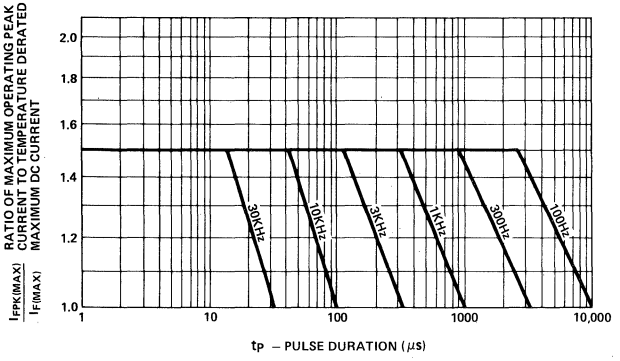


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration

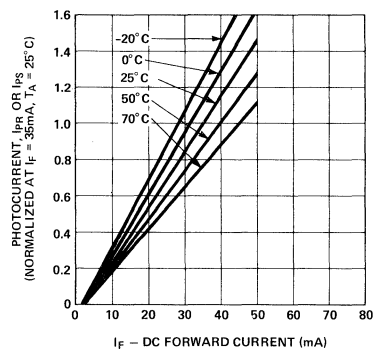


Figure 2. Relative Total Photocurrent vs. LED DC Forward Current

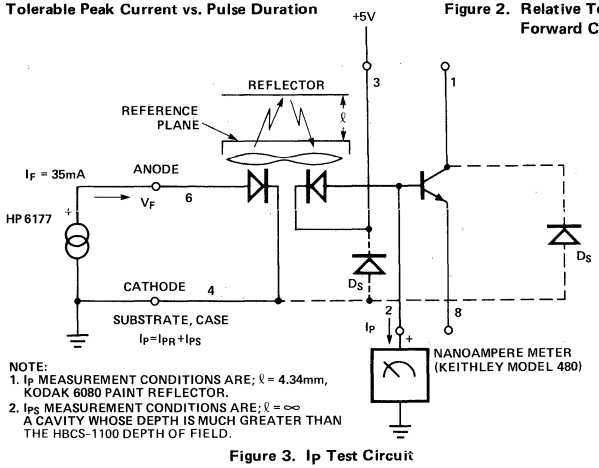


Figure 3. I_P Test Circuit

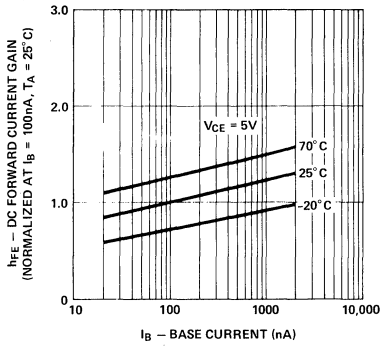


Figure 4. Normalized Transistor DC Forward Current Gain vs. Base Current at Temperature

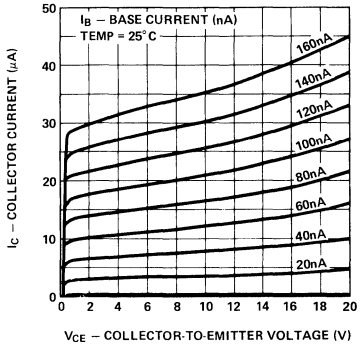


Figure 5. Common Emitter Collector Characteristics

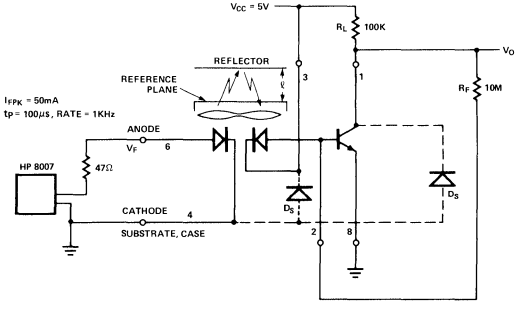


Figure 6. Slew Rate Measurement Circuit

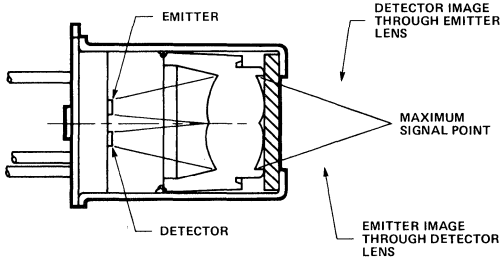


Figure 7. Image Location

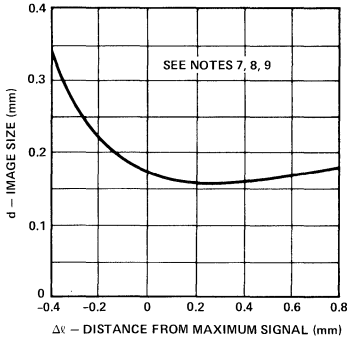


Figure 8. Image Size vs. Maximum Signal Point

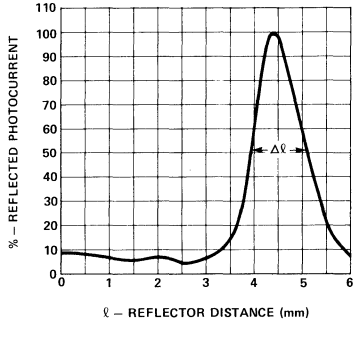


Figure 9. Reflector Distance vs. % Reflected Photocurrent

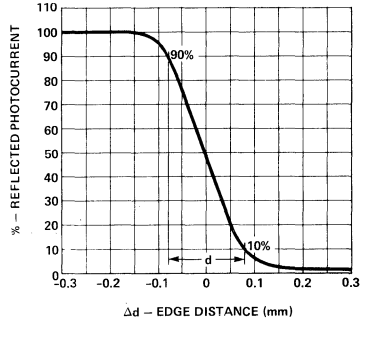


Figure 10. Step Edge Response

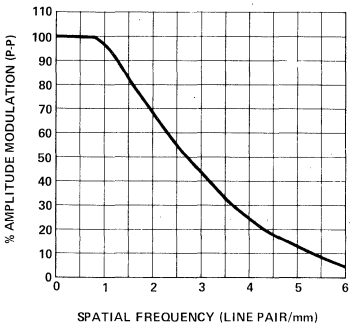


Figure 11. Modulation Transfer Function

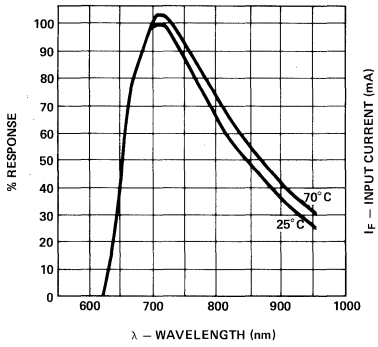


Figure 12. Detector Spectral Response

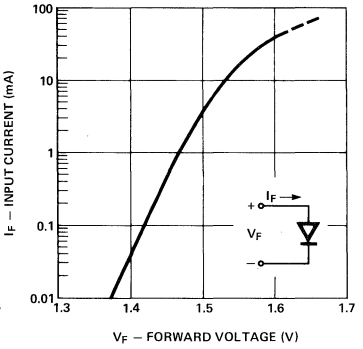


Figure 13. LED Forward Current vs. Forward Voltage Characteristics

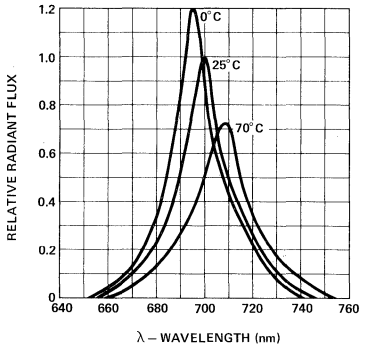


Figure 14. Relative Radiant Flux vs. Wavelength

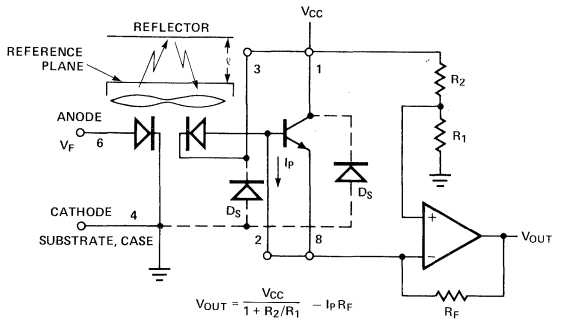


Figure 15. Photodiode Interconnection

Warranty and Service

HP Optical Reflective Sensor is warranted for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

For additional warranty or service information please contact your local Hewlett-Packard sales representative or authorized distributor.

HEWLETT PACKARD

New

Optical Reflective Sensors

Technical Data

HEDS-1200 High Resolution Infrared Sensor
HEDS-1300 Precision Resolution Sensor

Features

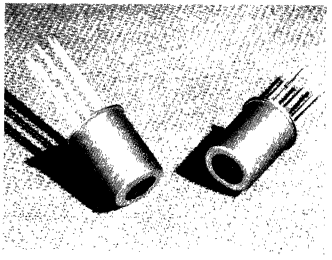
- **Focused Emitter and Detector in a Single Package**
- **TO5 Package**
- **Binning of Sensors by Photocurrent (Ipr)**

Applications

- **Bar Code Scanning**
- **Pattern Recognition and Verification**
- **Object Sizing**
- **Optical Limit Switching**
- **Optical/Surface Inspection**
- **Tachometry**
- **Edge/Line Sensing**
- **Dimensional Monitoring**

Description

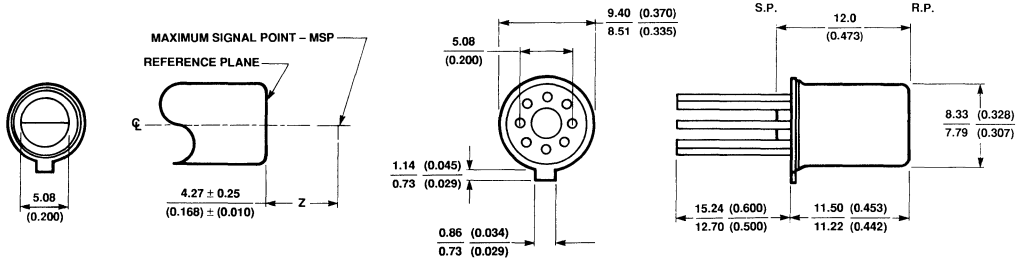
Both the HEDS-1200 and HEDS-1300 sensor are fully integrated modules designed for applications requiring optical reflective sensing. The modules contain an LED emitter (at the appropriate wavelengths) and a matched I.C. photodetector. A bifurcated aspheric lens is used to image the active areas of the emitter and the detector to a single spot that defines the resolution of the sensor. The output signal is a current generated by the photodiode.



Selection Guide

Sensor Part Number	HEDS-1200	HEDS-1300
Resolution	0.13 mm (0.005 in.)	0.19 mm (0.0075 in.)
LED Wavelength	820 nm	700 nm

Package Dimensions



NOTES:
A. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
B. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
C. THE REFERENCE PLANE (R.P.) IS THE TOP SURFACE OF THE PACKAGE.
D. NICKEL CAN AND GOLD-PLATED LEADS.
E. S.P. = SEATING PLANE.
F. THE LEAD DIAMETER IS 0.45 mm (0.018 in.) TYP.

BAR CODE PRODUCTS

Mechanical Considerations

The HEDS-1200 and HEDS-1300 sensors are packaged in a high profile 8 pin TO5 metal can with a glass window. The emitter and photodetector chips are mounted on the header at the base of the package. Positioned above these active elements is a bifurcated aspheric acrylic lens that focuses them to the same point.

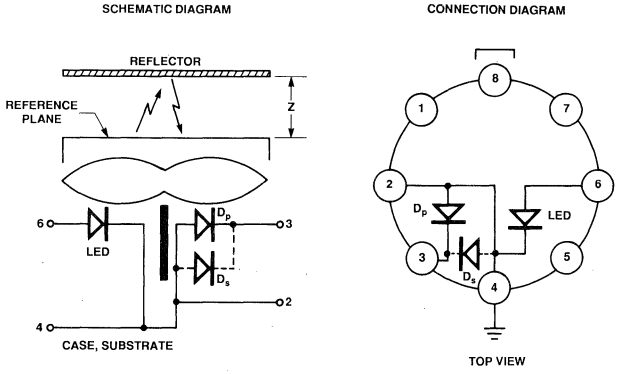
The sensors can be rigidly secured by commercially available TO5 style heat sinks, or 8 pin 0.200 inch diameter pin circle sockets. These fixtures provide a stable reference platform for affixing the sensors to a circuit board.

In applications requiring contact scanning, protective focusing tips are available. Focusing tips are available in either metal (HBCS-2999 or HBCS-4999) or polycarbonate (HBCS-A998 or HBCS-A999) packages using a rugged sapphire ball as the contact surface.

Electrical Operations

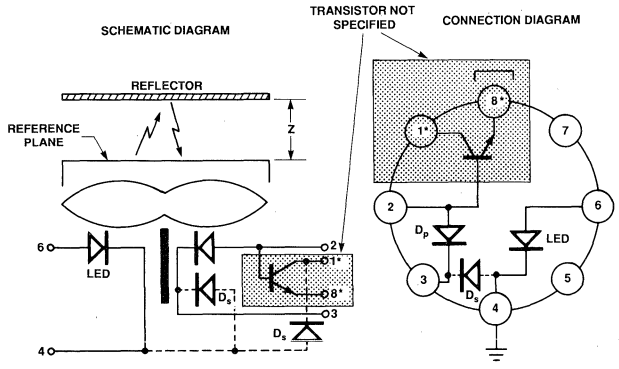
Both the HEDS-1200 and HEDS-1300 sensors have the following in common. The detector of the sensor is a single photodiode. The cathode of the emitter is physically and electrically connected to the case-substrate of the device. Applications that require modulation or switching of the LED should be designed to have the cathode connected to the electrical ground of the system. Refer to the Schematic and Connection Diagrams that follow.

HEDS-1200 Optical System



PIN #	FUNCTION (HEDS-1200)
2	PHOTODIODE ANODE, SUBSTRATE, CASE
3	PHOTODIODE CATHODE
4	LED CATHODE, SUBSTRATE, CASE
6	LED ANODE

HEDS-1300 Optical System



*NO CONNECTION TO BE MADE TO PIN 1 AND PIN 8

PIN #	FUNCTION (HEDS-1300)
2	PHOTODIODE ANODE
3	PHOTODIODE CATHODE
4	LED CATHODE, SUBSTRATE, CASE
6	LED ANODE

Absolute Maximum Ratings @ T_A = 25°C

Parameter	Symbol	HEDS-	Min.	Max.	Units	Fig.	Notes
Storage Temperature	Ts	1200	-40	+75	°C		
		1300	-40	+75	°C		
Operating Temperature	T_A	1200	-20	+70	°C		
		1300	-20	+70	°C		
Lead Soldering Temperature 1.6 mm from Seating Plane		1200		260°C for 10 sec.			1
		1300					1
Average LED Forward Current	If	1200	10	40	mA		3
		1300		50	mA		2
Peak LED Forward Current	Ifpk	1200		40	mA	7	4
		1300		75	mA	7	4
Reverse LED Input Voltage	Vr	1200		2.5	V		
		1300		5.0	V		
Photodiode Bias (Id = 100 µA max)	Vd	1200	-0.3	20	V		5
		1300	-0.3	20	V		5

Notes:
1. Caution: The thermal constraints of the acrylic lens will not permit the use of conventional wave soldering procedures. The typical preheat and post-cleaning temperatures and dwell times can subject the lens to thermal stresses beyond the absolute maximum ratings and can cause it to defocus.
2. Derate Maximum Average Current linearly from 65°C by 6 mA/°C. [HEDS-1300 only]
3. Non-linear effects make operation of the HEDS-1200 below 10 mA not advisable.
4. 1 KHz pulse rate, 300 µS pulse width.
5. All voltages referenced to Pin 4.

System Electrical/Optical Characteristics @ T_A = 25°C

Parameter	Symbol	HEDS-	Min.	Typ.	Max.	Units	Conditions	Fig.	Notes
Reflected Photocurrent	Ipr	1200	150	280	650	nA	If = 35 mA, Vd = 0	1A, 2, 6	6
		1300	150	280	650	nA	See Binning Table	1B, 2, 6	6
Quality Factor	<Q>	1200	0.82	0.95	1.0		If = 35 mA	1A	6, 7
		1300	0.82	0.95	1.0			1B	6, 7
Ipr Temperature Coefficient	Ke	1200		-0.005		1/°C	If = 35 mA		8
		1300		-0.01		1/°C			8
System Optical Step Response Size (OSR)	d	1200		0.13		mm		9A	9
		1300		0.19		mm		9B	9
Maximum Signal Point (MSP)	Zm	1200	4.01	4.27	4.62	mm	Measured from	4	
		1300	4.01	4.27	4.52	mm	Reference Plane	4	
Effective Numerical Aperture of Detector Lens	N.A.	1200		0.3					
		1300		0.3					

Notes:
6. Measured from a reflector coated with 99% diffuse reflective white paint (Kodak 6080) positioned 4.27 mm (0.168 in.) from the sensor's reference plane. Measured physically is the total photocurrent, Ipt, which consists of a signal (reflected from target) component, Ipr, and a component induced by reflections internal to the sensor (stray), Ips. Ipr = Ipt - Ips.
7. <Q> = Ipr/Ipt
8. Photocurrent variation with temperature follows a natural exponential law: Ip(T) = Ip(To)*exp[Ke(T-To)]
9. OSR size is defined as the distance for the 10%-90% "step" response of Ipr as the sensor moves over an abrupt black-white edge, or from opaque white to free space (no reflection).

Detector Electrical/Optical Characteristics @ T_A = 25°C

Parameter	Symbol	HEDS-	Min.	Typ.	Max.	Units	Conditions	Fig.	Notes
Dark Current	Id	1200		50	1000	pA	Vd = 5 V, If = 0		
		1300		50	1000	pA	Reflection = 0%		
Capacitance	Cd	1200		100		pF	Vd = 0 V, If = 0		
		1300		100		pF	f = 1 MHz		
Detector Area	Ad	1200		0.16		sq-mm	Square, with length		
		1300		0.16		sq-mm	= 0.4 mm per side		

Emitter Electrical/Optical Characteristics @ T_A = 25°C

Parameter	Symbol	HEDS-	Min.	Typ.	Max.	Units	Conditions	Fig.	Notes
Forward Voltage	Vf	1200		1.48	1.7	V	If = 35 mA	3	
		1300		1.6	1.8	V		3	
Reverse Breakdown Voltage	BVR	1200	2.5			V	Ir = 100 μA		
		1300	5.0			V			
Thermal Coefficient of Vf	ΔVf/ΔT	1200		-0.91		mV/°C	If = 35 mA		
		1300		-1.2		mV/°C			
Peak Wavelength	λ	1200	805	820	835	nm	If = 35 mA	5	
		1300	680	700	720	nm		5	
Emitting Area	Ae	1200		0.0062		sq-cm	0.0889 mm diameter junction (0.0035 in.)		
		1300		0.0285		sq-cm	0.185 mm diameter junction (0.0073 in.)		

Bin Table

Ipr Limits (nA)		
Bin #	**Min.**	**Max.**
2	150	200
3	195	245
4	240	293
5	288	355
6	350	430
7	425	520
8	515	650

Product Marking

The photocurrent binning of the sensor is included in the 8-digit code printed on the sensor can. The last digit in the code represents the bin number.

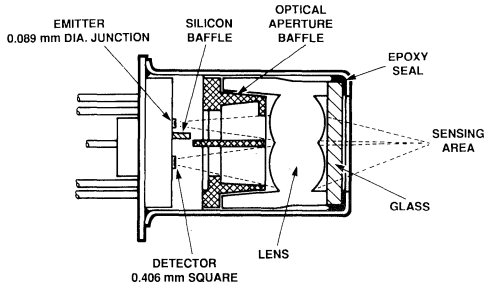
See Figure 8 for suggestions in the application of photocurrent bins.

Test algorithm bins units to the lowest bin number if a unit is in the overlap region. Such units can cross bin boundaries as temperature changes. (Ambient temperature affects LED efficiency slightly and may cause several percent changes in Ipr). Bin numbers are for "reference only" and do not constitute an absolute guarantee.

The output of all LEDs degrades with time, depending on drive conditions and temperature.

The entire available distribution of parts, appropriately marked, will be shipped. Single bin orders cannot be supplied.

HEDS-1200 Optical System



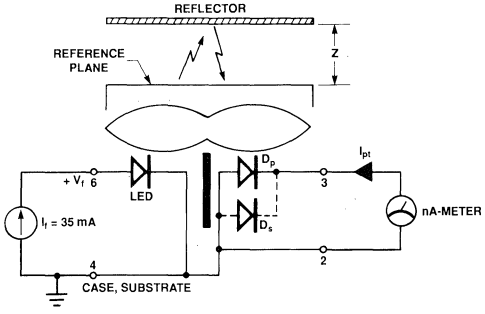
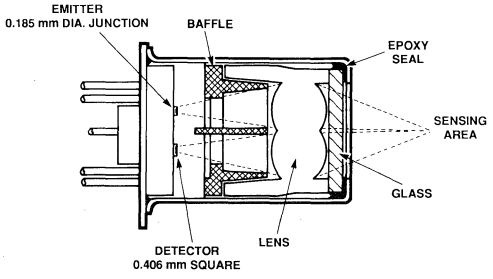
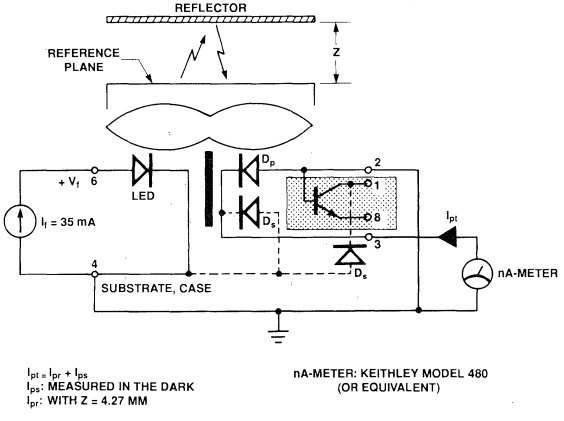


Figure 1A. HEDS-1200 Photocurrent Test Circuit.

HEDS-1300 Optical System





$I_{pt} = I_{pr} + I_{ps}$
I_{ps}: MEASURED IN THE DARK
I_{pr}: WITH Z = 4.27 MM

nA-METER: KEITHLEY MODEL 480
(OR EQUIVALENT)

Figure 1B. HEDS-1300 Photocurrent Test Circuit.

BAR CODE PRODUCTS

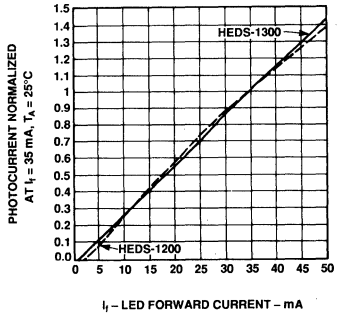


Figure 2. Relative Reflected Photocurrent.

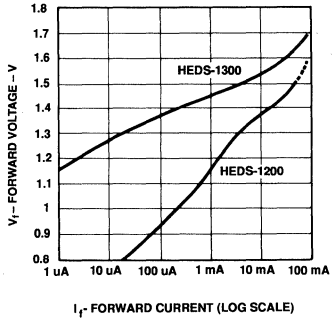


Figure 3. LED Forward Voltage vs. Forward Current.

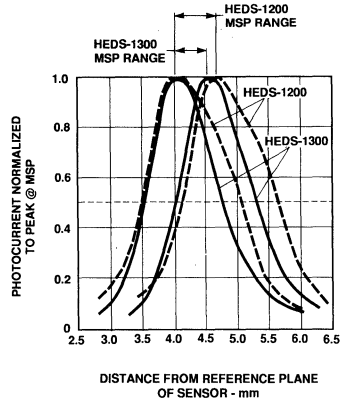


Figure 4. Photocurrent Variation with Distance.

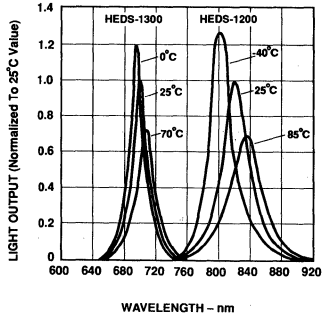


Figure 5. Typical Spectral Distribution of LEDs.

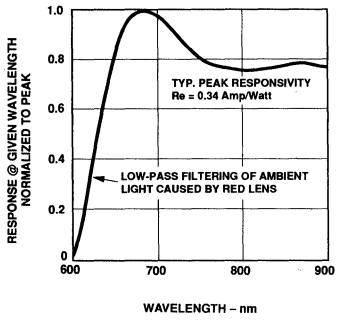


Figure 6. Relative Spectral Response of HEDS-1200 and HEDS-1300 Sensors.

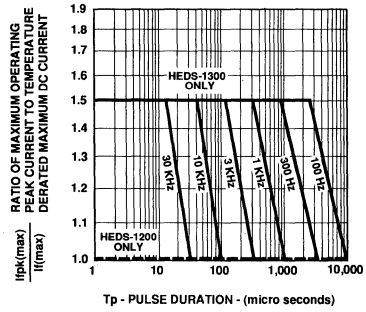
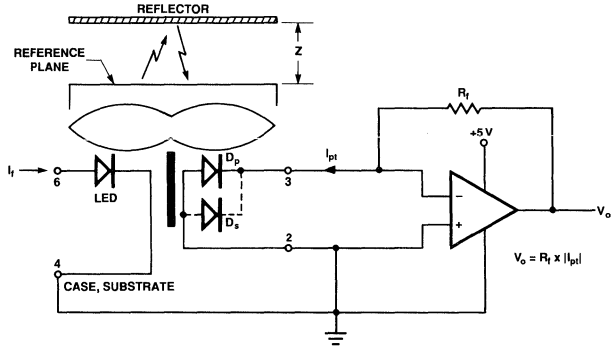


Figure 7. Sensor Pulse Drive Considerations. Max Tolerable Peak Pulse Current vs. Pulse Duration.

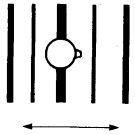


NOTE: FOR V_o (APPROX.) 1.9 – 2.4 VOLTS:

SENSOR BIN NUMBER	RECOMMEND VALUE OF R_f (OHMS)
2	15 M
3	12 M
4	10 M
5	8.2 M
6	6.8 M
7	5.6 M
8	4.7 M

Figure 8. Sensor with Transimpedance Amplifier.

Preferred Orientation



At maximum signal point (MSP) and/or when the sensor is in focus, the orientation of the sensor is unimportant. However, as one moves away from MSP and/or moves out of focus (either by distance or angle), the preferred orientation indicated above is recommended to maintain a higher resolution spot size.

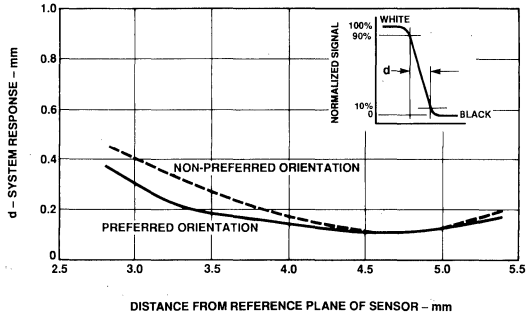


Figure 9A. HEDS-1200 System Optical Step Response Variation with Distance.

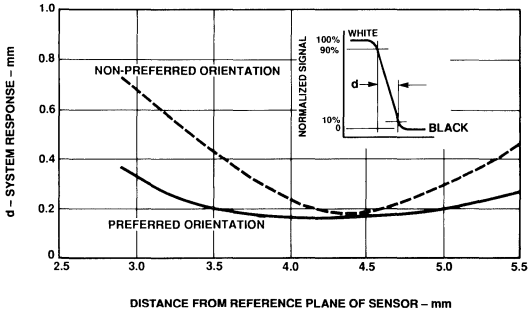


Figure 9B. HEDS-1300 System Optical Step Response Variation with Distance.

Warranty and Service

HP Optical Reflective Sensor is warranted for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

For additional warranty or service information please contact your local Hewlett-Packard sales representative or authorized distributor.

HEWLETT PACKARD

New

655 nm Precision Optical Reflective Sensor

Technical Data

HEDS-1500

Features

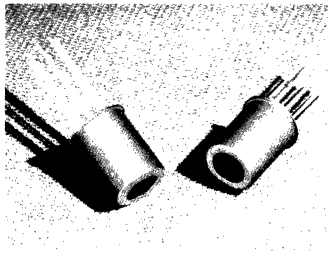
- **Focused Emitter and Detector in a Single Package**
- **655 nm Visible Emitter**
- **0.178 mm (0.007) Resolution**
- **TO-5 Miniature Sealed Package**
- **Photodiode Output**

Description

The HEDS-1500 is a fully integrated module designed for applications requiring optical reflective sensing. The module contains a 655 nm visible LED emitter and a matched I.C. photodetector. A bifurcated aspheric lens is used to image the active areas of the emitter and the detector to a single spot 4.27 mm (0.168 in.) in front of the package. The output signal is a current generated by the photodiode.

Applications

Applications for the HEDS-1500 include bar code scanning, pattern recognition and verification, object sizing, optical limit switching, tachometry, textile thread counting and defect detection, dimensional monitoring, line locating, paper edge detection, and any application where precision optical reflective sensing is desired.

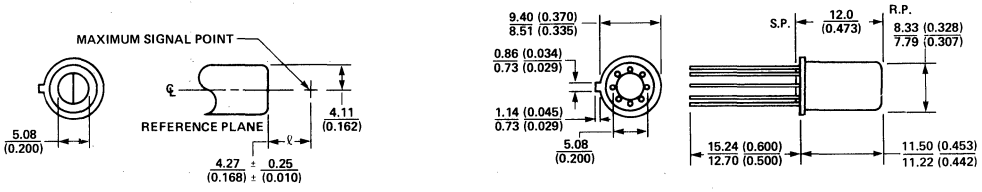


Mechanical Considerations

The HEDS-1500 is packaged in a high profile 8 pin TO-5 metal can with a glass window. The emitter and photodetector chips are mounted on the header at the base of the package. Positioned above these active elements is a

BAR CODE PRODUCTS

Package Dimensions



NOTES:
1. ALL DIMENSIONS IN MILLIMETERS AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. THE REFERENCE PLANE IS THE TOP SURFACE OF THE PACKAGE.
4. NICKEL CAN AND GOLD PLATED LEADS.
5. S.P. SEATING PLANE.
6. THE LEAD DIAMETER IS 0.45mm (0.018in.) TYP.

bifurcated aspheric acrylic lens that focuses them to the same point.

The sensors can be rigidly secured by commercially available two piece TO-5 style heat sinks, such as Thermalloy 2205, Aavid Engineering 321527, or 8 pin 0.200 inch diameter pin circle sockets. These fixtures provide a stable reference platform for affixing the HEDS-1500 to a circuit board.

In applications requiring contact scanning, protective focusing tips are available. Focusing tips are available in either metal or polycarbonate packages using a sapphire ball as the contact surface. The Hewlett-Packard part numbers are HEDS-3001, HBCS-2999, HBCS-4999, HBCS-A998 and HBCS-A999.

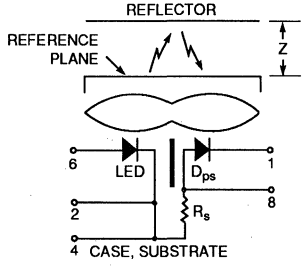
Electrical Operation

The detector of the sensor is a single photodiode. Figure 7 shows photocurrent being supplied from the cathode of the photodiode to an inverting input of the operational amplifier. The cathode of the 655 nm emitter is physically and electrically connected to the case-substrate of the device. Applications that require modulation or switching of the LED should be designed to have the cathode connected to the electrical ground of the system.

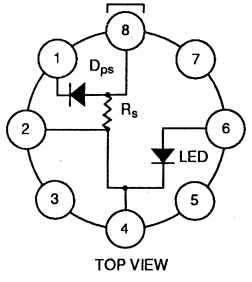
Applications where ambient light is present will require a special LED drive and recovery circuit to achieve the full resolution of the sensor. Application Note 1040 provides data and schematics to support HEDS-1500 sensor operation in ambient light conditions.

A reliability data sheet is available for the HEDS-1500 precision optical reflective sensor.

Schematic Diagram



Connection Diagram



PIN#	FUNCTION
1	PHOTODIODE CATHODE
2	HEADER GROUND
4	**
6	LED ANODE
8	PHOTODIODE ANODE

** CUSTOMER SHOULD NOT CONNECT GROUND TO PIN 4.

INTERNAL CONNECTION TO PIN 4 WILL BE DELETED IN THE FUTURE.

R_S — CHARACTERISTIC NOT DEFINED

Absolute Maximum Ratings @ T_A = 25 °C

Parameter	Symbol	Min.	Max.	Units	Note
Operating Temperature	T_A	-20	70	°C	
Storage Temperature	T_s	-40	75	°C	
Lead Soldering Temperature			260 for 10 sec.	°C	1
Average LED Forward Current	I_f		50	mA	
Peak LED Forward Current	I_{fp}		(data pending)		2
Reverse LED Input Voltage	V_r		5	V	
Photodiode Bias (-V = forward bias)	V_d	-0.3	7	V	3

(See next page for Notes.)

Electrical/Optical Characteristics at T_A = 25°C

Parameter	Symbol	Min.	Typ	Max.	Units	Conditions	Note	Figure
Reflected Photocurrent	I_{pr}	80	125	-	nA	If=35mA	4,5, 11	1,2,4, 7
Quality Factor	<Q>	0.82	0.95	1.0	--	If=35mA	4,6	
Maximum Signal Point (MSP)	Z	4.01 (.158)	4.27 (.168)	4.52 (.178)	mm (inch)		4,7	4
LED Forward Voltage	V_f	--	1.72	1.86	V	If=35mA		3
LED Reverse Breakdown Voltage	BVR	5.0	--	--	V	Ir=100µA		
Photodiode Dark Current	I_d	--	50	1000	pA	Vd=5V, If=0	8	
LED Peak Wavelength	lambda		655	670	nm	If=35mA		5
Ipr Temperature Coefficient	K_e		-0.006		1/°C		9	
System Optical Step Response Size (OSR)	d		0.154 (0.006)		mm (inch)	--	10	8

Note 1: CAUTION: The thermal constraints of the acrylic lens will not permit conventional wave soldering procedures. The typical preheat and post-soldering cleaning procedures and dwell times can subject the lens to thermal stresses beyond the absolute maximum ratings and can cause it to defocus.

Note 2: (Reliability tests are proceeding -- data not yet available.)

Note 3: I_d (max) = 100µA. Recommended operation: V_d (min) = 0V V_d(max) = 5V Exceeding maximum conditions may cause permanent damage to photodiode or to chip metallization.

Note 4: Measured from a reflector coated with 99% diffuse reflective white paint (Kodak 6080) positioned 4.27mm (0.168 in.) from the reference plane. (See "Photocurrent Test Circuit" for test connection.) Measured physically is the total photocurrent, Ipt, which consists of a signal (reflected from target) component, Ipr, and a component induced by reflection internal to the sensor (stray), Ips. Ipt = Ipr + Ips Specified is the reflected signal component, Ipr.

Note 5: See Bin Table

Note 6: <Q> = Ipr/Ipt

Note 7: Measured from the reference plane (R.P.) of the sensor.

Note 8: Leakage current of photodiode measured in the dark.

Note 9: Photocurrent variation with temperature varies with LED output which follows a natural exponential law: Ip(T) = Ip(To)*exp[Ke(T-To)]

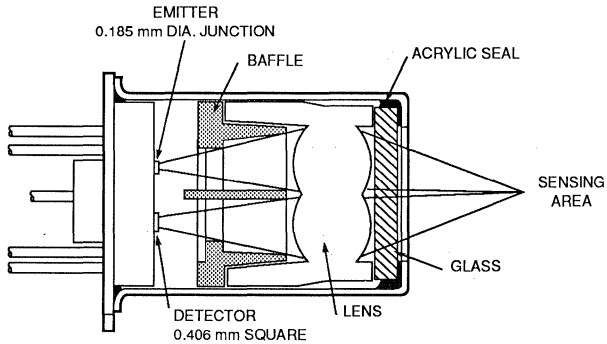
Note 10: OSR size is defined as the distance for a 10%-90% "step" response of Ipr as the sensor moves over an abrupt step from opaque white to black, or from opaque white to free space (no reflection).

Note 11: Sensor contains no ambient light filtering -- see Figure 6 for relative response of detector. In bright ambient light conditions, LED signal may be a small portion of total signal. AC coupling and additional signal processing may be necessary . Reference Application Note 1040.

BIN TABLE

I_{pr} Limits		
Bin#	**Min.**	**Max.**
1	80	110 nA
2	105	135
3	125	155
4	150	190
5	180	220
6	215	275
7	270	320

Optical System



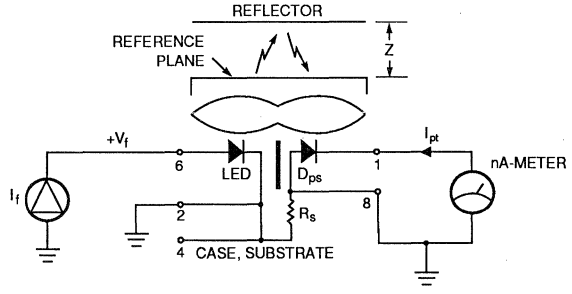


Figure 1. Photocurrent Test Circuit

Product Marking

The photocurrent binning of the sensor is incorporated as part of the date code format, assigned at time of test -- "CTYYWWan", where:

C = letter identifying country of assembly -- S = Singapore. If blank = USA.

T = tester code designation letter (single letter)

YY = last two digits of year

WW = week number in year

a = single lot code letter (A - Z), sequential assignment during week

n = bin number

See Figure 7 for suggestion in the application of photocurrent bins.

Test algorithm bins units to the lowest bin number if a unit is in the overlap region. Such units can cross bin boundaries as temperature changes. (Ambient temperature affects LED efficiency slightly and may cause several percent change in I_{pr}). Bin numbers are for "reference only" and do not constitute an absolute guarantee.

The output of all LEDs degrade with time, depending on drive conditions and temperature.

The entire available distribution of parts, appropriately marked, will be shipped. Single bin orders cannot be supplied.

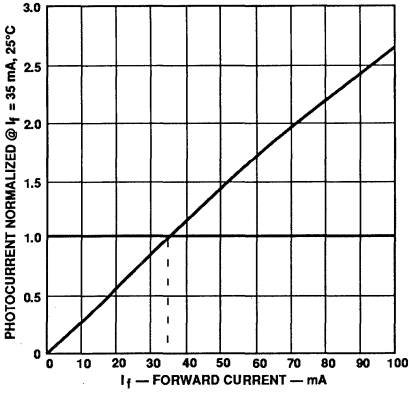


Figure 2. Relative Reflected Photocurrent

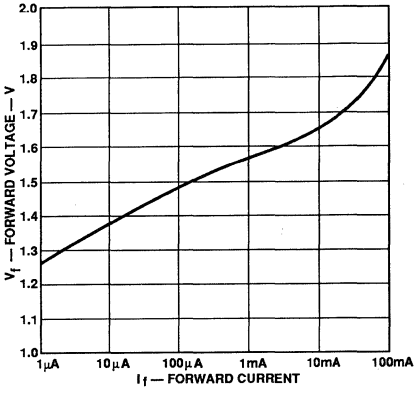


Figure 3. LED Forward Voltage vs. Forward Current

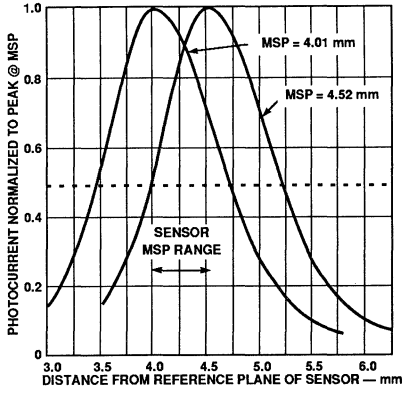


Figure 4. Photocurrent Variation with Distance

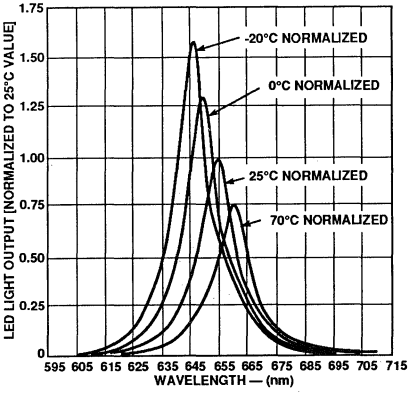


Figure 5. 655 nm Emitter Typical Spectral Distribution

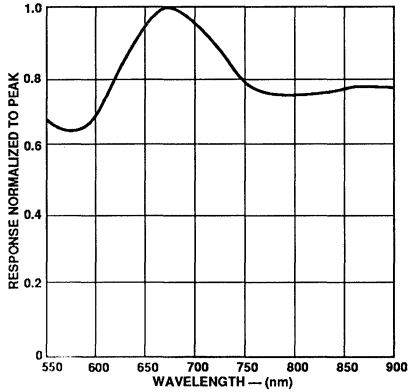


Figure 6. Relative Spectral Response of Sensor

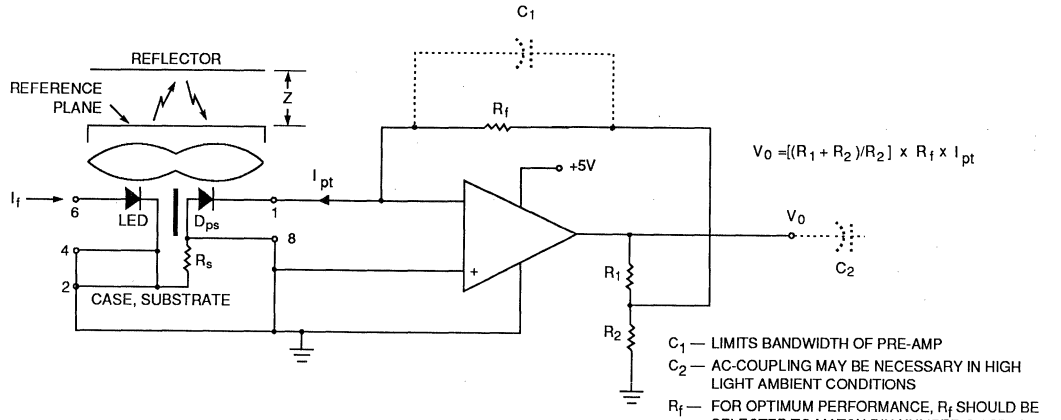


Figure 7. Sensor with Transimpedance Amplifier

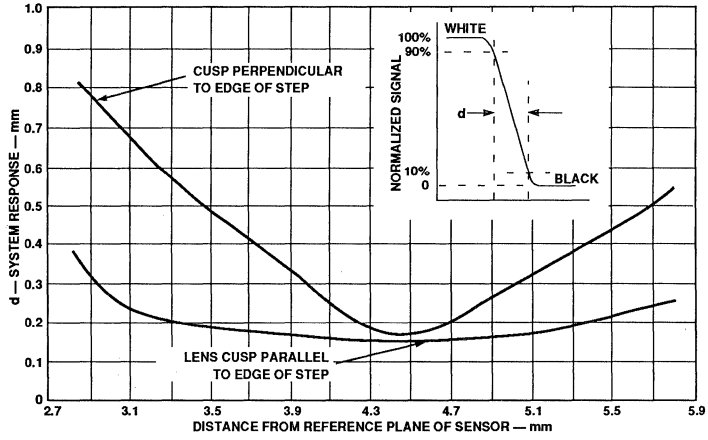


Figure 8. System Optical Step Response Variation with Distance

Warranty and Service

HP Optical Reflective Sensor is warranted for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

For additional warranty or service information please contact your local Hewlett-Packard sales representative or authorized distributor.

HEWLETT PACKARD

New

Single Chip Bar Code Decode IC

Technical Data

HBCR-1610
HBCR-1611
HBCR-1612

Features

- **Supports 5 Industry Standard Bar Code Symbologies**
- **Automatic Code Recognition**
- **Choice of Parallel or Full Duplex Serial ASCII Interface**
- **Programmable via Escape Sequences or Pin Strapping**
- **CMOS**
- **Through hole and surface mount packages**
- **Audio and Visual Feedback Control**

Description

The Hewlett-Packard Single Chip Bar Code Decoder IC offers flexible bar code decoding that is designed to give OEMs the ability to address a growing number of industry segments and applications. Flexibility is made possible through firmware that allows the IC to automatically recognize and decode the most popular bar code symbologies. User implementation is easy since only a few supporting components are required.

The HBCR-1610 series decodes the most popular bar code symbologies used in applications in government, retail, industrial and medical markets. The IC automatically discriminates and decodes the following symbologies:

- Code 39 (Standard or Extended)
- Interleaved 2 of 5
- UPC A, E0, E1
- EAN/JAN 8, 13
- Codabar
- Code 128

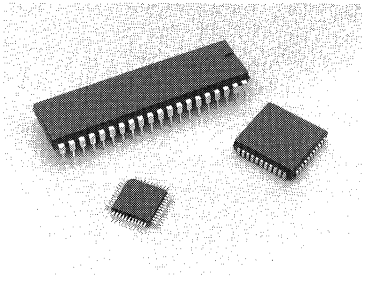
All bar codes may be scanned bidirectionally except for UPC/EAN/JAN bar codes with supplemental digits, which must be scanned so that the supplemental digits are scanned last.

Scanner Input

The HBCR-1610 decode ICs are designed to accept input from hand held digital scanners and slot readers. The maximum scan speed is 30 ips (76 cm/s).

Data Communications

The serial port supports a variety of baud rates, parity, and stop bits as described in Table 5. The IC



has a "Single Read Mode" which allows the application program to stop data input until a "Next Read" command has been received. This allows the host computer to process data transmissions before enabling subsequent reads. Control of data transmission is available using the standard XON/XOFF (D_1/D_3) handshake.

The parallel port is accomplished via an external 74HCT646 (octal bus transceiver) or two 74HCT574s (octal latches). There are handshake lines for both data and commands.

Feedback Features

Both audible and visual feedback are possible with the HBCR-1610 series. In both cases, the feedback outputs from the IC

should be buffered before driving the transducer. An LED or beeper connected to the IC is either controlled directly by the IC, with signals generated by successful decodes, or controlled by the host system. The tone of the beeper can be configured to one of 16 tones, or can be silenced.

Power Requirements

The decoder IC is operated from a +5 volt DC power supply. the maximum current draw is 24 mA. The maximum power supply ripple voltage should be less than 100 mV, peak-to-peak.

Idle Mode

The IC automatically reduces power consumption whenever there is no scanning or decoding activity, or when there is no activity on the I/O port. See Table 4.

Manual

The HBCR-1610 Series Users Manual (HBCR-1697) covers the following topics:

- Specifications and Timing Diagrams
- Pin Definitions and Schematics
- General Scanning Tips
- Configuration and Operation
- Escape Sequence Programming
- Data Output Formats
- Sample Bar Codes
- I/O and Pacing Characteristics

Table 1. Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units	Notes
Supply Voltage	V_{cc}	4.5	5.5	V	1
Ambient Temperature	T_A	-40	+85	°C	
Oscillator Frequency	F_{osc}	DC	16.000	MHz	2

Notes:
1. Maximum power supply ripple of 100 mV peak-to-peak.
2. The IC can use either an 11.059 or a 16.000 MHz crystal or ceramic resonator. The FRQ pin selects the frequency that matches the oscillator.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	- 55	+150	°C	
Supply Voltage	V_{cc}	- 0.5	+7.0	V	
Pin Voltage	V_{IN}	- 0.5	V_{cc} + 0.5	V	3

Note:
3. Voltage on any pin with respect to ground.

Table 3. Ordering Information

Part Number	Description
HBCR-1610	CMOS, 40 pin DIP, bulk shipment, no manual
HBCR-1611	CMOS, 44 pin PLCC, bulk shipment, no manual
HBCR-1612	CMOS, 40 pin QFP, bulk shipment, no manual
HBCR-1697	HBCR-1610 Series Users Manual
Option A01	IC individually bagged, no manual
Option B01	IC individually boxed with manual and data sheet

IC Configuration

The default configuration is set when the IC powers up or when a Hard Reset command is received. Default configuration of many of the options is dependent on the logic states of IC pins, as shown in Table 5. A complete description of the pins and all possible configurations is in the Users Manual. More complete and flexible configuration is achieved using escape sequence commands.

There are two pins that cause significant changes in the IC operation.

FRQ Pin

The FRQ pin is used to tell the IC what frequency oscillator is attached to the IC. Using the higher frequency allows greater maximum scan speeds, but causes the IC to draw slightly more supply current. If the state of the FRQ pin does not match the actual oscillator, beeper tones, LED flash length, parallel port timing, and serial port baud rates are adversely affected.

FRQ	Oscillator Frequency
0	16.000 MHz
1	11.059 MHz

IOM Pin

The IOM pin selects between the serial and parallel I/O mode of the IC. Depending on the state of the IOM pin, definitions of several configuration pins change or move to new positions.

IOM	I/O Mode
0	Parallel
1	Serial

Escape Sequences

The following set of escape sequences are used to control the IC and change its default configuration. Note that all configuration changes will be lost after a Hard Reset, or after power up. Detailed information on how to formulate and use escape sequences is given in the Users Manual.

Table 7. Escape Sequences

Escape Sequence	Function
^{E}C - y <n> b	Good Read Beep Tone
^{E}C - y <n> d	Serial Intercharacter Delay
^{E}C E	Hard Reset
^{E}C - y <n> f	Bar Code Symbology Selection
^{E}C - y <n> g	Check Character Options
^{E}C - y <n> h	Decoding Options
^{E}C - y <n> j	Single Read Mode
^{E}C - y <n> k	Single Read Control
^{E}C - y <n> l	LED Control
^{E}C - y <n> m	Interleaved 2 of 5 Length
^{E}C - y <n> O <n characters>	Trailer Selection
^{E}C - y <n> q	Code ID Characters
^{E}C - y <n> s	Status Request
^{E}C - y <n> t	Sound Tone
^{E}C - y <n> w	Scanner Enable

Table 4. DC Characteristics

HBCR-1610, 1611, 1612 (T_A = 0 °C to +70 °C, V_{cc} = 4.5V to 5.5V, V_{ss} = 0V)

Symbol	Parameter	1610 Pins	1611 Pins	1612 Pins	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	all	all	all	- 0.5	0.2 V_{cc} - 0.1	V	
V_{IH}	Input High Voltage	except 9,19	except 10, 21	except 4, 15	0.2 V_{cc} + 0.9	V_{cc} + 0.5	V	
V_{IH1}	Input High Voltage	9, 19	10, 21	4, 15	0.7 V_{cc}	V_{cc} + 0.5	V	
V_{OL}	Output Low Voltage	1-8, 10-17, 21-28	2-9, 11, 13-19, 24-31	1-3, 5, 7-13 18-25, 40,44		0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output Low Voltage	32-39	36-43	30-37		0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	1-8, 10-17, 21-28	2-9, 11, 13-19, 24-31	1-3, 5, 7-13 18-25, 40-44	2.4		V	I_{OH} = - 60 µA
					0.75 V_{cc}		V	I_{OH} = - 25 µA
					0.9 V_{cc}		V	I_{OH} = - 10 µA
V_{OH1}	Output High Voltage	32-39	36-43	30-37	2.4		V	I_{OH} = - 400 µA
					0.75 V_{cc}		V	I_{OH} = - 150 µA
					0.9 V_{cc}		V	I_{OH} = - 40 µA
I_{IL}	Input Low Current	1-8, 10-17, 21-28	2-9, 11, 13-19, 24-31	1-3, 5, 7-13, 18-25, 40-44		-50	µA	V_{IN} = 0.45V
I_{LI}	Input Leakage Current	32-39	36-43	30-37		±10	µA	$V_{ss} \leq V_{IN} \leq V_{cc}$
R_{RST}	Pulldown Resistor	9	10	4	50	150	KΩ	
I_{cc}	Supply Current 11.059 MHz	40	44	38		18	mA	Scanning
						4	mA	Idle
I_{cc}	Supply Current 16.000 MHz	40	44	38		24	mA	Scanning
						6	mA	Idle

Table 5. Summary of Features and Configurations – HBCR-1610 series

Feature	Function or Value	Default Setting	
		Serial Mode	Parallel Mode
Bar Code Symbology	When a symbology is enabled, bar codes of that type can be read, assuming other decoding options are satisfied.	Depends on pins: C39, I25, UPC CDB and C28.	All codes enabled
Interleaved 2 of 5 Label Length	Length variable from 4 to 32, or specific lengths from 2 to 32, or 6 or 14 only	Variable, 4-32	Variable, 4-32
Check Character Verification	For Code 39 For Interleaved 2 of 5 For Code 128 † For UPC/EAN †	Depends on pin $\overline{C3C}$ Depends on pin $\overline{I2C}$ Enabled Enabled	Depends on pin $\overline{C3C}$ Depends on pin $\overline{I2C}$ Enabled Enabled
Check Character Transmission	For Code 39 and Interleaved 2 of 5 For UPC/EAN For Code 128 †	Depends on pin $\overline{CST}$ Enabled Enabled	Depends on pin $\overline{CST}$ Enabled Enabled

† Not configurable

Table 5. Summary of Features and Configurations – HBCR-1610 series (continued)

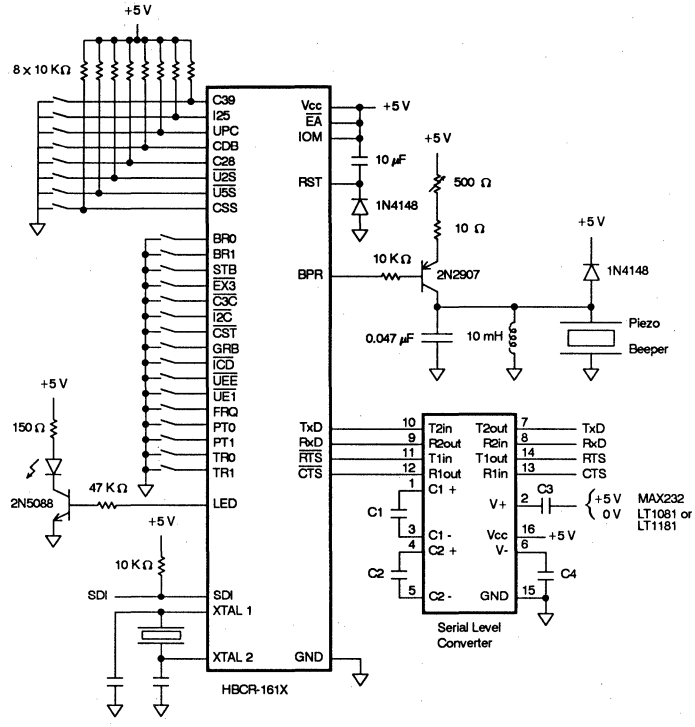
Feature	Function or Value	Default Setting	
		Serial Mode	Parallel Mode
Extended Code 39 Enable	Converts paired Code 39 data characters to Full ASCII characters	Depends on pin $\overline{EX3}$	Depends on pin $\overline{EX3}$
UPC/EAN Decoding Options	UPC vs. UPC/EAN UPC E expansion to UPC A UPC E Version 1 autodiscrimination UPC/EAN supplemental digits UPC/EAN check digit UPC/EAN output format	UPC/EAN Depends on pin $\overline{UEE}$ Depends on pin $\overline{UE1}$ Depends on pins $\overline{US2}$ and $\overline{US5}$ Transmitted Standard	UPC/EAN Depends on pin $\overline{UEE}$ Depends on pin $\overline{UE1}$ Disabled Transmitted Standard
Codabar Start/ Stop Transmission	Transmits or suppresses Codabar start/stop characters	Depends on pin CSS	Depends on pin CSS
Baud Rates	1200, 2400, 4800, 9600	Depends on pins BR0 and BR1	–
Parity	0's, 1's, even, odd	Depends on pins PT0 and PT1	0's
Stop Bits	1 or 2	Depends on pin STB	–
XON/XOFF Pacing †	Controls data flow on either port	Enabled	Enabled
Transmitted character Delay enable	Controls 10 millisecond intercharacter delay on the serial port	Depends on pin $\overline{ICD}$	–
Trailer Selection	String of characters appended to the decoded message (4 maximum)	$^{C}_{R}$, $^{C}_{R}{}^{L}_{F}$, $^{H}_{T}$, or none Depends on pins TR0 and TR1	$^{C}_{R}$
Single Read Mode	Controls when labels can be read	Disabled	Disabled
Code ID Character Enable	Controls the transmission of the Code ID characters before decoded data	Disabled	Disabled
Good Read Beep Tone Selection	Controls the tone sounded when a bar code label is read	High or low pitch Depends on pin GRB	High or low pitch Depends on pin GRB
LED Control	Controls LED function: flash or turn off after a label is read	Auto Flash Mode	Auto Flash Mode

† Not configurable

Table 6. Summary of Commands – HBCR-1610 series

Feature	Description
Scanner Enable	When enabled, scans from a wand or a slot reader are decoded; otherwise, they are ignored.
Hard Reset	Resets the IC as though it were just powered up.
Self Test Failure Message	An error message is transmitted over the serial port at 9600 baud at power up if the IC self test fails.
Status Request	Returns the version number of the software.
Sound Tone	Causes the IC to sound a tone of the selected pitch for 120 milliseconds.

Stand Alone Decoder (Serial Mode)



Notes:

1. Use the correct capacitor for either a crystal or a ceramic resonator. See Users Manual, page 2-16.
2. See the pin diagrams for the pinout of the decode IC. Pin numbers vary with package.
3. Volume of the beeper circuit is adjustable by varying the value of the 500 Ω pot.
4. The eight pull up resistors shown in the schematic are only needed if a DIP switch is used. If the pins are strapped directly to ground or Vcc, the resistors are not needed.
5. The logic levels of the SDI scanner input is as follows: black = high, white = low.

Surface Mount IC Drying

Whenever Vapor Phase or Infrared Reflow technologies are used to mount either of the surface mount packages, there is a possibility that previously absorbed moisture, heated very rapidly to the reflow temperatures, may cause the package to crack from internal stresses. There is a reliability concern that moisture may then enter the package over a period of time, and metal corrosion may take place, degrading the IC performance.

To reduce the amount of absorbed moisture and prevent cracking, all of the surface mount ICs should undergo one of the following baking cycles. The parts MUST then be mounted within 48 hours. If the parts are not mounted within 48 hours, they *must* be rebaked.

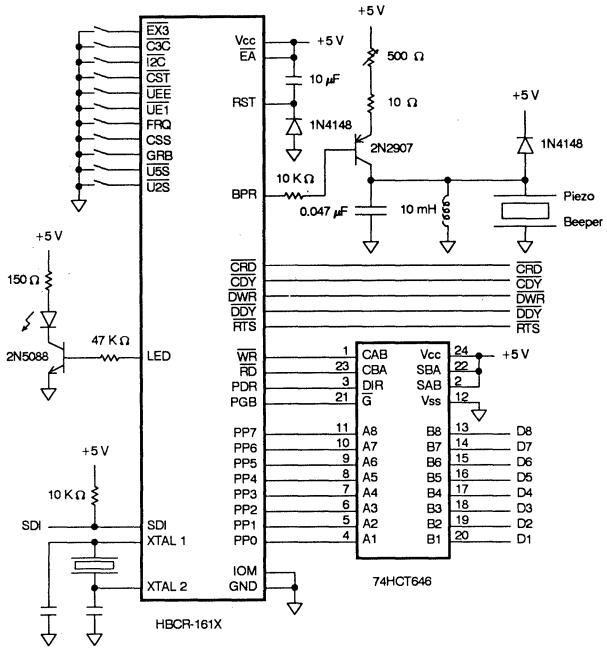
The total number of baking cycles must not exceed two (2). If the ICs are baked more than twice, Hewlett-Packard cannot guarantee the performance and reliability of the parts.

Neither bake cycle can be performed in the standard shipping tubes. The ICs must be baked in an ESD safe, mechanically stable container, such as an aluminum tube or pan.

Cycle	Temperature	Time
A	125 °C	24 Hours
B	60 °C	96 Hours

Note:
Cycle B must be done in an atmosphere of <5% relative humidity air or nitrogen.

Stand Alone Decoder (Parallel Mode)

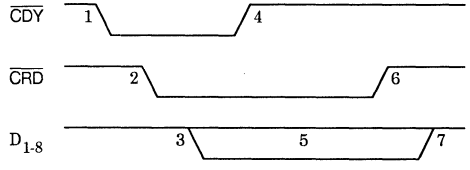


Notes:

1. Use the correct capacitor for either a crystal or a ceramic resonator. See the Users Manual.
2. See pin diagrams for the pinout of the decode IC. Pin numbers vary with package.
3. Volume of the beeper circuit is adjustable by varying the value of the 500 Ω pot.
4. An alternative circuit using two 74HCT574 octal latches instead of the 74HCT646 is in the Users Manual.
5. The logic levels of the SDI scanner input is as follows: black = high, white = low.

Parallel I/O Handshake

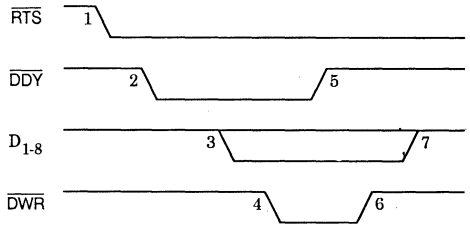
Commands received by the IC



Protocol

1. The host indicates that a command is pending by lowering CDY.
2. The IC indicates that it is ready for a command by lowering CRD.
3. The host outputs the command onto the data bus.
4. The host indicates that the data is stable by raising CDY.
5. The IC reads the command from the bus.
6. The IC indicates that the command was accepted by raising CRD.
7. The host removes the data from the data bus.

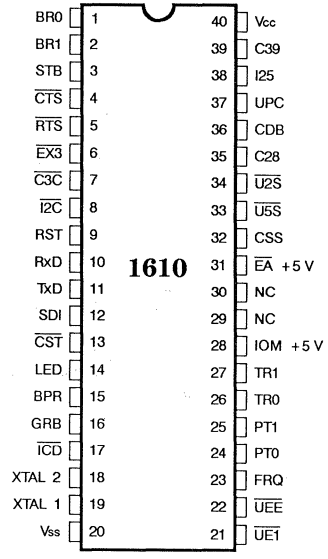
Data Transmitted from the IC

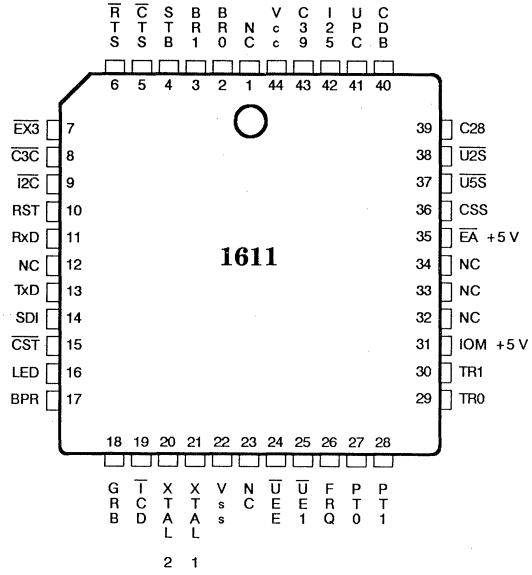


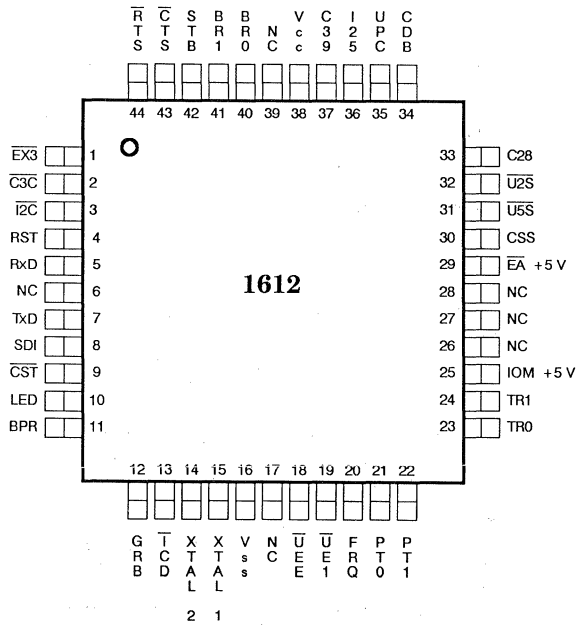
Protocol

1. The IC indicates data is ready to be transmitted by lowering RTS; RTS stays low until the last byte has been transmitted.
2. The host signals the IC that it is ready for data by lowering DDY.
3. The IC outputs data onto the bus.
4. The IC indicates that the data is stable by lowering DWR.
5. The host acknowledges that the data is received by raising DDY.
6. The IC indicates the end of the output cycle by raising DWR.
7. The IC removes data from the bus.

Serial Pinout

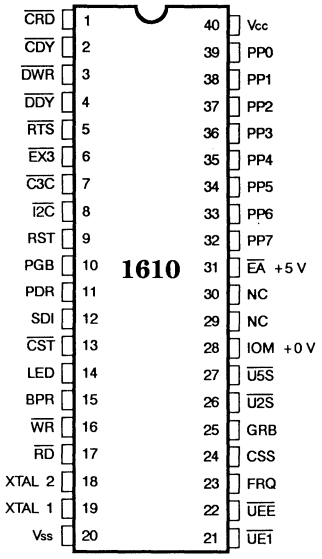


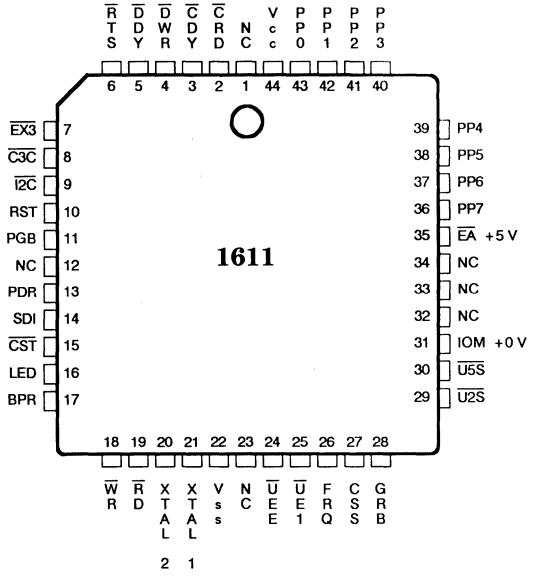


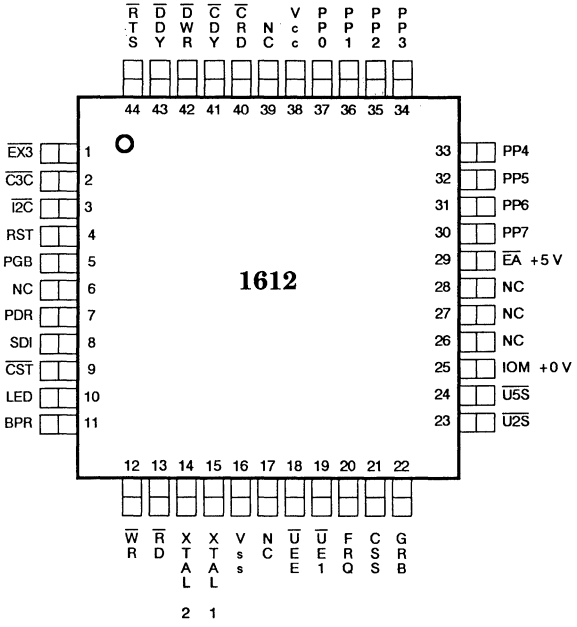


Pin Mnemonics	
RxD	Received Data
TxD	Transmitted Data
BR0-BR1	Baud Rate Select
PT0-PT1	Parity Select
TR0-TR1	Trailer Characters Select
$\overline{CTS}$	Clear to Send
$\overline{RTS}$	Request to Send
C39	Code 39 Enable
$\overline{EX3}$	Extended Code 39 Enable
I25	Interleaved 2 of 5 Enable
UPC	UPC/EAN Enable
CDB	Codabar Enable
C28	Code 128 Enable
$\overline{UEE}$	UPC E Expansion Enable
$\overline{UE1}$	UPC E Version 1 Enable
$\overline{U2S}$	UPC 2 Digit Supplementals Enable
$\overline{U5S}$	UPC 5 Digit Supplementals Enable
CSS	Codabar start/stop char. Enable
STB	Stop Bits Select
$\overline{C3C}$	Code 39 Checksum Enable
$\overline{I2C}$	Interleaved 2 of 5 Checksum Enable
$\overline{CST}$	Checksum Transmit Enable
SDI	Scanner Digital Input
IOM	I/O Mode Select
RST	IC Reset
$\overline{EA}$	External Program Memory Enable
GRB	Good Read Beep Tone Select
FRQ	Oscillator Frequency Select
LED	LED control line
BPR	Beeper control line
$\overline{ICD}$	Intercharacter Delay Enable
XTAL1	Oscillator Input
XTAL2	Oscillator Input
V_{cc}	Power
V_{ss}	Ground

Parallel Pinout

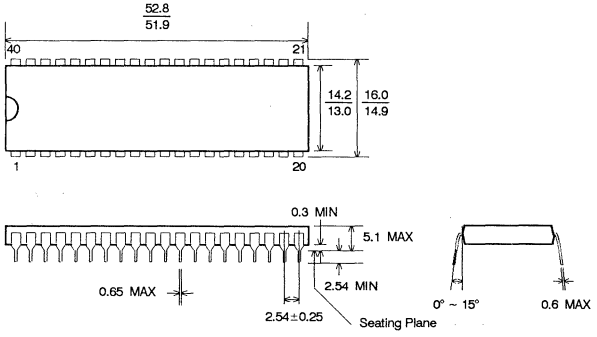




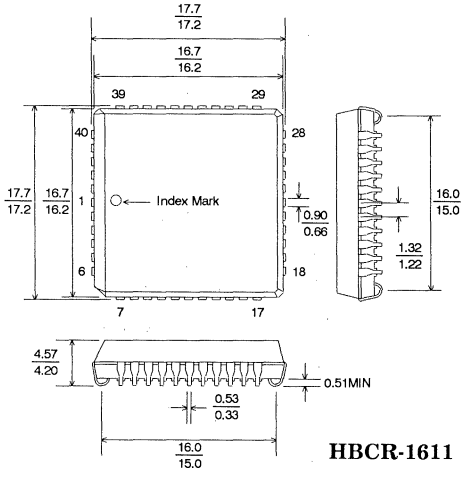


Pin Mnemonics	
PP0-PP7	Parallel Port Bus
DWR	Data Write handshake
DDY	Ready for data handshake
CRD	Command read handshake
CDY	Command ready handshake
RTS	Request to Send
C3C	Code 39 Checksum Enable
I2C	Interleaved 2 of 5 Checksum Enable
CST	Checksum Transmit Enable
EX3	Extended Code 39 Enable
WR	Data write
RD	Data read
U2S	UPC 2 Digit Supplementals Enable
U5S	UPC 5 Digit Supplementals Enable
CSS	Codabar start/stop char. Enable
PGB	Transceiver drive Enable
PDR	Transceiver direction control
UEE	UPC E Expansion Enable
UE1	UPC E Version 1 Enable
SDI	Scanner Digital Input
IOM	I/O Mode Select
RST	IC Reset
EA	External Program Memory Enable
FRQ	Oscillator Frequency Select
GRB	Good Read Beep Tone Select
LED	LED control line
BPR	Beeper control line
XTAL1	Oscillator Input
XTAL2	Oscillator Input
V_{cc}	Power
V_{ss}	Ground

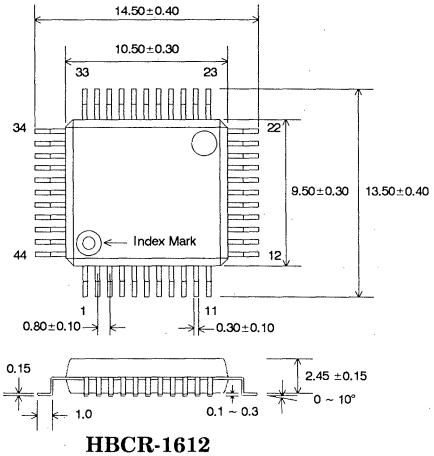
Mechanical Specifications – Units (mm)



HBCR-1610



HBCR-1611



HBCR-1612

Warranty and Service

The HP Decode IC is warranted for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

For additional warranty or service information please contact your local Hewlett-Packard sales representative or authorized distributor.

Handling Precautions

The decoder ICs are extremely sensitive to electrostatic discharge (ESD). It is important that proper anti-static procedures be observed when handling the ICs. The package should not be opened except in a static free environment.

HEWLETT PACKARD

Programmable Bar Code Decode ICs

Technical Data

HBCR-2210
HBCR-2211

Features

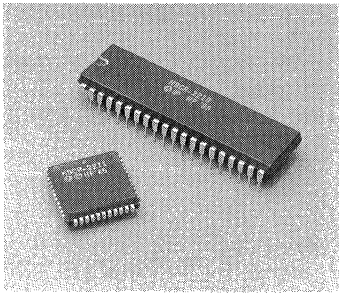
- **Ideal for Hand Scanning and Non-contact Laser Scanning Applications**
- **Supports 7 Industry Standard Bar Code Symbologies**
- **Automatic Code Recognition**
- **Choice of Parallel or Serial Interface**
- **Full Duplex ASCII Interface**
- **Extensive Configuration Control**
- **Optical and Escape Sequence Configuration**
- **Input and Output Buffering**
- **Low Current (18 mA) CMOS Technology**
- **40 Pin DIP and 44 Pin PLCC Packages**
- **Audio and Visual Feedback Control**
- **EEPROM Support For Non-volatile Configuration**
- **Single +5 Volt Supply**

Description

Hewlett-Packard's Bar Code Decoder ICs offer flexible bar code decoding capability that is designed to give OEMs the ability to address a growing number of industry segments and applications. Flexibility is made possible through sophisticated firmware which allows the ICs to accept data from a wide variety of scanners and to automatically recognize and decode the most popular bar code symbologies. User implementation of the decoder ICs is easy since it requires only a few supporting components and provides a standard I/O interface.

Manufacturers of data collection terminals, point of sale terminals, keyboards, weighing scales, medical equipment, test instrumentation, material handling equipment, and other systems having data collection needs are finding a growing demand for bar code reading capability in their products. The HBCR-2210 series decode ICs make it easy to add this capability without the need to invest in the development of bar code decoding software.

The bar code decoder ICs are compatible with most hand held scanners and some medium speed machine mounted laser heads. The HBCR-2210 series is compatible with fixed beam non-contact scanners, digital wands, and slot readers. In addition, the decoder is optimized for use with the Symbol Technologies moving beam laser scanners, but is also compatible with many other moving beam non-contact laser scanners with a similar interface protocol.



The HBCR-2210 series decoder ICs are excellent decoding solutions for a number of stationary scanning applications found in automated systems. The scan rate for moving beam applications should be similar to the scan rates for hand held laser scanners (35 to 45 scans per second). The scan speed for fixed beam applica-

tions should be similar to the scan speeds typical of wands and slot readers. For moving beam applications, it is necessary for the scanner to utilize the three laser control lines.

The HBCR-2210 series decodes the most popular bar code symbologies now in use in applications in the industrial, retail, government and medical markets:

- **Code 39 (Standard or Extended)**
- **Interleaved 2 of 5**
- **UPC A, E**
- **EAN/JAN 8, 13**
- **Codabar**
- **Code 128**
- **Code 11**
- **MSI Code**

When more than one symbology is enabled, the bar code being scanned will automatically be recognized and decoded, except for Standard versus Extended Code 39, which are mutually exclusive. Bi-directional scanning is allowed for all bar codes except UPC/EAN/JAN with supplemental digits, which must be scanned with the supplemental digits last.

The I/O for the decode IC is full duplex, 7 bit ASCII. Both serial and parallel interfacing are available. The serial interface can be converted to an RS232C interface or connected directly to another microprocessor for data processing. The parallel interface can be connected to a 74HC646 octal bus transceiver chip (or an equivalent part). Feedback to the operator is accomplished by signals for an LED and a beeper. In addition, there are many programmable functions that cover such items as code selection, good read beep tone, Header and Trailer buffers, laser scanning control, beeper tone, etc. See Table 2 for a complete list.

Performance Features

Bar Codes Supported

Code 39 is an alphanumeric code, while Extended Code 39 encodes the full 128 ASCII character set by pairing Code 39 characters. Both can be read bi-directionally with message lengths of up to 32 characters. An optional checksum character can be used with these codes, and the ICs can be configured to verify this character prior to data transmission.

Interleaved 2 of 5 code, a compact numeric only bar code, can also be read bi-directionally with message lengths from 4 to 32 characters. To enhance data accuracy, optional checksum character verification and/or message length checking can be enabled.

The following versions of UPC, EAN and JAN bar codes can be read bi-directionally: UPC-A, UPC-E, EAN-8, EAN-13, JAN-8, and JAN-13. All versions can be enabled simultaneously or decoding can be restricted to only the UPC codes. UPC, EAN, and JAN codes printed with complementary two or five digit supplemental encodations can be read in two different ways. If the codes are enabled without the supplemental encodations, then only the main part of symbols printed with supplemental encodations will be read. If the reading of supplemental encodations is enabled, then only symbols with these supplements will be read. When supplemental encodations are enabled, the bar code symbols must be read in a direction which results in the supplements being scanned last.

Codabar, a numeric only bar code with special characters, can be read bi-directionally for message lengths up to 32 characters. The decode IC can be configured to transmit or suppress the Codabar start/stop characters.

Code 128, a full ASCII symbology, can be scanned bi-directionally with message lengths of up to 32 characters.

Code 11 is a numeric, high density code with one special character, the hyphen (-). Verification of one or two check characters must be enabled, and the check character(s) are always transmitted. This code can be scanned bi-directionally.

MSI Code is a numeric, continuous code, with message lengths up to 32 characters. The check digit, a modulo 10 checksum, is always verified and transmitted. This code can be scanned bi-directionally.

Scanner Input

The HBCR-2210 decode IC is designed to accept data from hand held digital scanners or slot readers with the following logic state: black = high, white = low. The same decode IC also accepts data from hand held laser scanners with the opposite logic states: black = low, white = high. The scanner type pin (SCT) on the HBCR-2210 series must be driven prior to power up or hard reset to identify the type of scanner connected.

In the HBCR-2210 series ICs, the automatic laser shutoff feature delay time is adjustable as a configuration option. Applications which require increased accuracy may need the redundancy check feature.

Scanner input can be disabled by software command. This allows an application program to control when an operator can enter data, preventing inadvertent data entry. It also allows the program to verify each scan before enabling subsequent scans. The HBCR-2210 series also offers two Single Read Modes which allow the application program to stop bar code data entry until a "Next Read" command is received, allowing the host computer to process data transmissions before enabling subsequent reads.

Configuration Control and Non-volatile Storage

Configuration of the decoder IC is done by any of three methods. A minimal subset of key options can be "hardwired" – controlled by electrically strapping specified pins on the decoder IC itself. Which pins affect configuration depends on the selection of serial or parallel interface. Alternatively, ASCII characters in the form of HP Escape Sequences (a format common to HP decoder ICs) can be sent to the serial or parallel I/O port; these commands can be used to control all configurable options. A third method is optical configuration, which makes use of special bar code menus supplied by HP. Menu labels can be created to modify any configurable options. A summary of the decoder IC features and applicable configuration methods for each is presented in Tables 2 and 3.

Once configuration has been set, it can be stored in an optional non-volatile memory, if included in the decoder circuit. When the EEP pin is tied high, the decoder IC drives I/O lines compatible with the widely available 9346/93C46 family of serial EEPROMS. The configuration is thereby saved during power down of the system and automatically reloaded at power up. Escape sequence commands allow explicit storage and recall of configuration settings. When using optical configuration, storage is automatic. If the EEP pin is tied low, the EEPROM is not used, so only hardwired configuration options are saved through powerdown; all others are set to default values at powerup. Table 2 shows default values of all features.

Data Communications

The serial port supports a wide range of baud rates, parities, and stop bits as described in Table 2. Software control of data transmission can be accomplished with a standard Xon/Xoff (DC1/DC3) handshake. The decode IC also supports an RTS/CTS hardware handshake.

The parallel port data has configurable parity. When the SMD pin is tied low, several pins pertaining to the serial port change function to control a parallel port instead. Pins 1 through 5 on DIP packages assume the function of handshake lines for the parallel port. The port itself is an external '646 family octal bus transceiver. Processor pins 10 and 11 (TXD and RXD in serial mode) now control the transceiver chip along with pins 16 and 17, RD and WR. Alternative circuits using SSI latch chips can be substituted for the '646 implementation to customize the function of the parallel port to a particular bus configuration.

Feedback Features

Both audio and visual feedback are possible with the HBCR-2210 series. In both cases, the outputs from the ICs should be buffered before driving the actual feedback transducer. An LED or beeper connected to the decoder IC can be controlled directly by the IC, with signals generated by successful decodes, or can be controlled by the host system. In addition, the tone of the beeper can be configured to be one of 16 different frequencies, or can be silenced.

Power Requirements

The decoder IC operates from a +5 volt DC power supply. The maximum current draw is 18 mA. The maximum power supply ripple voltage should be less than 100 mV, peak-to-peak.

Handling Precautions

The decoder ICs are extremely sensitive to electrostatic discharge (ESD). It is important that proper anti-static procedures be observed when handling the ICs. The package should not be opened except in a static free environment.

Manuals

The decode IC Users Manual covers the following topics:

- Data output formats
- I/O interfaces
- Laser input timing diagrams
- Escape sequence syntax and functionality
- Example schematics
- All configurable options
- Bar code menus
- Scanner positioning and tilt
- Sample bar code symbols
- Appendices describing bar code symbologies

Table 1. Ordering Information

Part Number	Description
HBCR-2210	CMOS, 40 pin DIP, bulk ship, no manual
HBCR-2211	CMOS, 44 pin PLCC, bulk ship, no manual
OPT A01	IC individually boxed with manual and data sheet
HBCR-2297	HBCR-2210 Series Users Manual

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units	Notes
Supply Voltage	V_{CC}	4.0	6.0	V	1
Ambient Temperature	T_A	-40	+85	°C	
Crystal Frequency	XTAL	0 (DC)	11.059	MHz	2
Element Time Interval (Moving Beam)	ETI_M	13	555	µs	2,3,4
Element Time Interval (Contact Scanner)	ETI_C	50	71000	µs	3,4

Notes:
1. Maximum power supply ripple of 100 mV peak to peak.
2. The HBCR-2210 series uses a 11.059 MHz crystal. For different crystal frequencies, multiply the specified baud rate and beeper frequencies by (crystal frequency/11.059 MHz) and multiply the element time interval ranges by (11.059 MHz/crystal frequency).
3. At the specified crystal frequency.
4. Corresponds to a scan rate of 35 to 45 scans per second.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-55	+150	°C	
Supply Voltage	V_{CC}	-0.5	+7.0	V	5
Pin Voltage	V_{IN}	-0.5	V_{CC}+0.5	V	5,6

Notes:
5. T_A = 25 °C
6. Voltage on any pin with respect to ground

DC Characteristics

HBCR-2210, 2211 **(T_A = 40 °C to +85 °C, V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0 V)**

Symbol	Parameter	HBCR-2210 Pins	HBCR-2211 Pins	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	all	all	−0.5	0.2 V_{CC} −0.1	V	
V_{IH}	Input High Voltage	except 9, 18	except 10, 20	0.2 V_{CC} +0.9	V_{CC}+0.5	V	
V_{IH1}	Input High Voltage	9, 18	10, 20	0.7 V_{CC}	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	1-8, 10-17, 21-28	2-9, 11, 13-19, 24-31		0.45	V	I_{OL}= 1.6 mA
V_{OL1}	Output Low Voltage	30, 32-39	33, 36-43		0.45	V	I_{OL}= 3.2 mA
V_{OH}	Output High Voltage	1-8, 10-17, 21-28	2-9, 11, 13-19, 24-31	2.4		V	I_{OH}= − 60 μA
				0.75 V_{CC}		V	I_{OH}= −30 μA
				0.9 V_{CC}		V	I_{OH}= −10 μA
V_{OH}	Output High Voltage	30, 32-39	33, 36-43	2.4		V	I_{OH}= −400 μA
				0.75 V_{CC}		V	I_{OH}= −150 μA
				0.9 V_{CC}		V	I_{OH}= −40 μA
I_{IL}	Input Low Current	1-8, 10-17, 21-28	2-9, 11, 13-19, 24-31	−10	−200	μA	V_{IN}= 0.45 V
I_{IL2}	Input Low Current	18	20		−3.2	mA	V_{IN}= 0.45 V
I_{LI}	Input Leakage Current	32-39	36-43		±10	μA	$0.45 \le V_{IN} \le V_{CC}$
R_{RST}	Pulldown Resistor	9	10	20	125	KΩ	
I_{CC}	Power Supply Current	—	—		18	mA	All Outputs disconnected
I_{CC}	Idle Mode Power Supply Current	—	—		9	mA	Note 7.

Note:

7. Applies only to HBCR-2210 and -2211 in Wand Mode or Laser Mode with Laser Idling enabled with no scanning or I/O operation in progress.

Table 2. Summary of Features and Configurations - HBCR-2210 series

In the table below, the column entitled Selection is either:

Software	Escape Sequence and Optical Menu Programmability
Hardwire	Control of a feature by electrically strapping specified pins on the decoder IC itself
Both	Both Software and Hardwire

Feature	Function or Value	Selection	Default Setting
Code Selection	When a symbology is enabled, bar codes of that type can be read, assuming that other decoding options are satisfied.	Both	Decoding of all codes is enabled
Minimum/Maximum Label Length Selection	Code 39, Codabar, Code 128, Code 11, and MSI Code	Software	Min. = 1 Max. = 32
	Interleaved 2 of 5	Software	Min. = 4 Max. = 32

(continued)

Table 2. Summary of Features and Configurations - HBCR-2210 series (continued)

Feature	Function or Value	Selection	Default Setting
Interleaved 2 of 5 Specific Label Length Selection	Length variable from 4 to 32, or a specific even length between 2 and 32, or lengths 6 and 14 only	Software	4 to 32
Check Character Verification Enable	For Code 39 For Interleaved 2 of 5 When enabled, the check character at the end of the bar code data is verified by the decoder	Software Software	Disabled Disabled
Check Character Transmission Enable	For both Code 39 and Interleaved 2 of 5, the check characters verified by the reader are included at the end of the decoded message	Software	Disabled
Code 39 Full ASCII Conversion Enable	Extended Code 39 data will be converted to ASCII characters	Software	Disabled
UPC/EAN/JAN Decoding Options Selection	UPC/EAN/JAN vs. UPC only Enable 2 or 5 digit supplements Autodiscrimination of tags with and without supplements	Software Software	UPC/EAN/JAN Enabled Supplements Disabled Disabled
Codabar Data Start/Stop Transmission Enable	Transmit or suppress start/stop characters	Software	Transmit
Code 11 Check Digit Verification Selection	Selection of 1 or 2 check digits	Software	1 check digit
Baud Rates	150, 300, 600, 1200, 2400, 4800, 9600, 19200	Both	Depends on pins BR1, BR0,and SMD
Parity	0's, 1's, Odd, Even	Both	Depends on pins EEP, PT1 and PT0
Stop Bits	1 or 2	Both	Depends on pins SMD and STB
RTS/CTS Pacing Enable	Request-To-Send/Clear-To-Send Pacing controls serial port data transmission	Software	Enabled
Xon/Xoff Pacing Enable	Controls data transmission on serial or parallel port by means of control characters sent to decoder IC	Software	Disabled
Transmitted Character Delay Enable	Specifies whether a delay is inserted between characters transmitted on the serial port	Software	Disabled

(continued)

Table 2. Summary of Features and Configurations - HBCR-2210 series (continued)

Feature	Function or Value	Selection	Default Setting
Transmitted Character Delay Selection	Specifies the number of milliseconds to insert between completion of transmission of one character and beginning of transmission of the next (1 to 250 ms)	Software	20 msec
Header Selection	A string of characters prepended to the decoded message (10 characters, maximum)	Software	none
Trailer Selection	A string of characters appended to the decoded message (10 characters, maximum)	Software	C_R L_F
Reader Address Selection	Reader Address is transmitted at the beginning of decoded and No-Read messages for polling purposes. (1 character)	Software	none
Message Ready/Not Ready Response Selection	The Message Ready/Not Ready response is transmitted after the reader receives a status request type 3 and is used with Single Read Mode 2. (1 character each)	Software	ACK/NAK
No-Read Message Selection	The No-Read Message configured is transmitted each time there is an unsuccessful read (10 characters, maximum)	Software	none
No-Read Recognition Enable	Controls whether the decoder detects unsuccessful reads and sends the No-Read Message	Software	Disabled
Single Read Mode 1 Enable	Controls reading and automatic transmission of decoded messages	Software	Disabled
Single Read Mode 2 Enable	Controls separate reading of bar codes and triggering decoded message transmission	Software	Disabled
Output Buffering Enable	Characters to be transmitted are entered into a 256 character queue for use with a pacing protocol.	Software	Disabled
Scanner Type Selection	Determines whether a wand or laser is to be used	Hardwire	Depends on pin SCT
Laser Shutoff Delay Selection	Defines laser on time prior to automatic shutoff, from 0 to 10 seconds in 100 ms steps	Software	3 seconds
Laser Redundancy Check Enable	Enables requirement for two consecutive, identical decodes for a good read	Software	Disabled

(continued)

Table 2. Summary of Features and Configurations - HBCR-2210 series (continued)

Feature	Function or Value	Selection	Default Setting
Continuous Laser Read Mode Enable	When enabled, the laser is turned on permanently instead of waiting for the trigger to be pulled	Software	Disabled
Laser Connection Detection Enable	When enabled, the scanner type pin is ignored at powerup. Instead, the decoder tests for a laser scanner to determine scanner type	Software	Disabled
Laser Trigger Latch Mode Enable	When enabled, the laser scanner continues to scan after the trigger has been released until either the laser shutoff delay period elapses or a read occurs	Software	Disabled
Laser Idling Enable	When enabled, the processor idles while waiting for the trigger to be pulled, reducing current draw	Software	Disabled
Code ID Character Selection	Code ID character serves to identify the symbology of the decoded message	Software	Code 39 = a Int 2/5 = b UPC/EAN = c Codabar = d Code 128 = e Code 11 = f MSI Code = g
Code ID Character Transmission Enable	Code ID character can be added to the beginning of each decoded message	Software	Disabled
Bar Code Menu Scan Response Enable	Verification of individual configuration menu scans via transmission of response message	Software	Disabled
Hard Reset Message Enable	"Ready 12.4" C_R L_F will be transmitted to host upon hard reset	Software	Disabled
ROM, RAM Self Test Enable	When enabled, ROM and RAM are tested after a Hard Reset	Software	Enabled
Good Read Beep Tone Selection	Selects Good Read Beep tones (1 to 16)	Software	Tone 12
LED Control Selection	Controls the LED function: Automatic Flash Mode Automatic Feedback Mode		 Enabled Disabled
LED Active Level Selection	Defines logic level of LED ON state	Software	Active High
LED, Beeper Feedback Suppression Enable	Suppresses LED and Beeper operation for systems without those annunciators	Software	Not Suppressed

(continued)

Table 2. Summary of Features and Configurations - HBCR-2210 series (continued)

Feature	Function or Value	Selection	Default Setting
Wand Input Buffering Enable	Data from wand scans is collected continuously in an input buffer to increase throughput	Software	Disabled
Quiescent State of Address Line Selection	The quiescent state of the processor memory bus address lines A8, A9, A10 can be defined for additional I/O interfacing	Software	High

Table 3. Summary of Commands - HBCR-2210 Series

Features	Description
Scanner Enable	When enabled, scans with the wand or laser are decoded; otherwise, they are ignored
Hard Reset	Resets decoder IC as though it were just powered up
Soft Reset	Clears pacing conditions, errors
LED Control Selection	Controls the LED On/Off function
Status Requests	Cause the decoder to generate a status message • General status message showing symbology of last message read, error conditions, etc. • Message Ready/Not Ready response (for Single Read Mode 2)
Sound Tone	This command causes the reader to sound a tone at the selected pitch for approximately 100 milliseconds
Configuration Control	There are three operations that manipulate the decoder configuration as a block. • Set default configuration • Save configuration in non-volatile memory • Recall non-volatile configuration
Execute Pending Command	For use with laser scanning, this command causes immediate execution of previous commands that would otherwise be postponed until the laser scan finishes

Table 4. Summary of Other Features - HBCR-2210 Series

Power Idle Mode	Reduces current draw of processor from approximately 20 mA to 4 mA in wand mode when the wand is inactive
Laser Failure Timeout	Turns off the laser if the Scan Sync signal is missing after approximately 1 second, and sets the laser failure status bit
Self Test Failure Message	An appropriate message is transmitted at power up if the decoder Self Test fails. • ROM SELF TEST FAILED • EEPROM SELF TEST FAILED • RAM SELF TEST FAILED
EEPROM Fault Recognition	An appropriate message is transmitted at power up if the EEPROM checksum is incorrect. • EEPROM FAULT

Parallel Mode Handshake Timing

Handshake and Data Lines

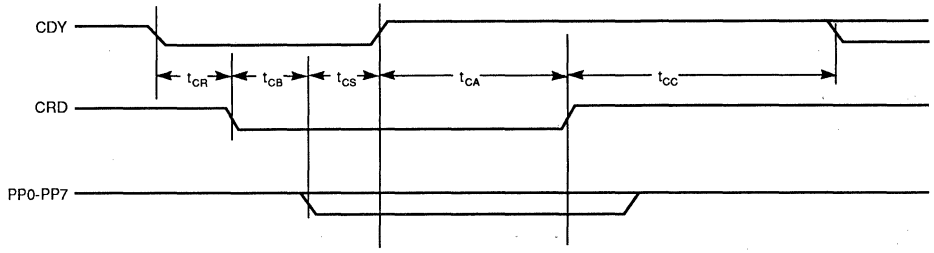


Figure 1. Host Commands Received By Decode IC (Reader)

Handshake Timing

t_{CR} = Falling edge of command ready to falling edge of command read. Max. = 30 µs for the first byte of transmission from host.

t_{CB} = Falling edge of command read to command valid. Min. = 0 µs

t_{CS} = Command valid set up to rising edge of command ready. Min. = 0 µs

t_{CA} = Rising edge of command ready to rising edge of command read. Max. = 8 µs

t_{CC} = Rising edge of command read to falling edge of command ready. Min. = 0 µs

Handshake and Data Lines

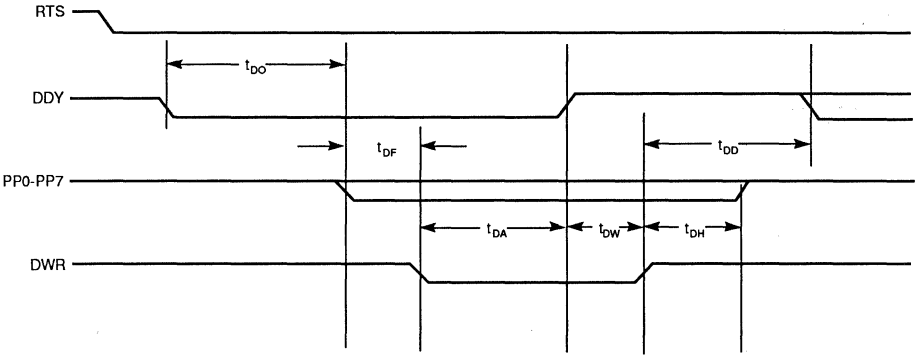


Figure 2. Decoder IC Data Sent to Host

Handshake Timing

t_{DO} = Falling edge of data ready to data output to bus. Min. = 6 µs Typical Max. = 74 µs

Note: The maximum can be infinite if there is no data to be transmitted. RTS can be used to determine when there is data. If the scanner is active or escape sequence commands are being processed, (t_{DO} + t_{DF}) can extend by an indefinite amount.

t_{DF} = Data output to bus to falling edge of data write. Max. = 6 µs

t_{DA} = Falling edge of data write to rising edge of data ready. Min. = 0 µs

t_{DW} = Rising edge of data ready to rising edge of data write. Max. = 8 µs

t_{DH} = Data hold after rising edge of data write. Max. = 4 µs

t_{DD} = Rising edge of data write to falling edge of data ready. Min. = 0 µs

PLCC Drying

Whenever Vapor Phase or Infrared Reflow Technologies are used to mount the PLCC packages, there is a possibility that previously absorbed moisture, heated very rapidly to the reflow temperatures, may cause the package to crack from the internal stresses. There is a reliability concern that moisture may then enter the package over a period of time, and metal corrosion may take place, degrading the IC performance.

To reduce the amount of absorbed moisture and prevent cracking, all of the PLCC ICs should undergo one of the following baking cycles. The parts must then be mounted within 48 hours.

If the parts are not mounted within 48 hours, they must be re-baked.

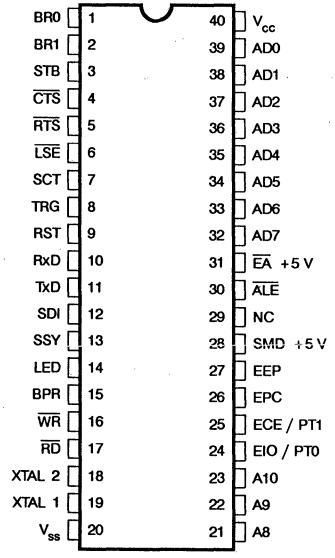
The total number of baking cycles must not exceed two. If the ICs are baked more than twice, Hewlett-Packard cannot guarantee the performance and reliability of the parts.

Neither bake cycle can be performed in the standard shipping tubes. The ICs must be baked in an ESD safe, mechanically stable container, such as an aluminum tube or pan.

Cycle	Temperature	Time	Notes
A	125°C	24 hrs	
B	60 °C	96 hrs	8

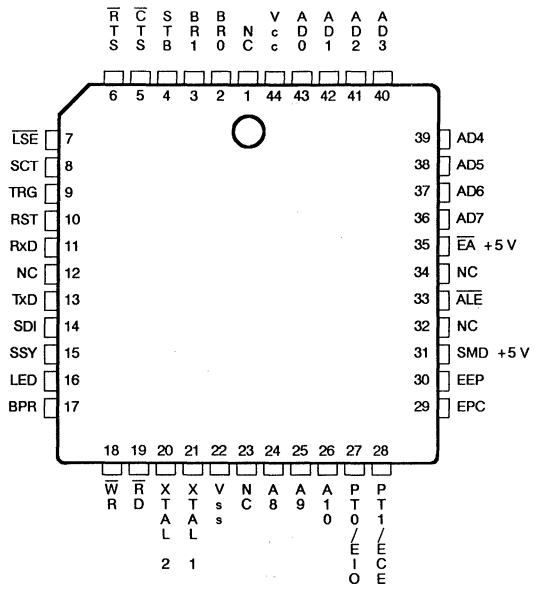
Note:
8. Cycle B must be done in atmosphere of <5% relative humidity air or nitrogen.

Pin Definitions



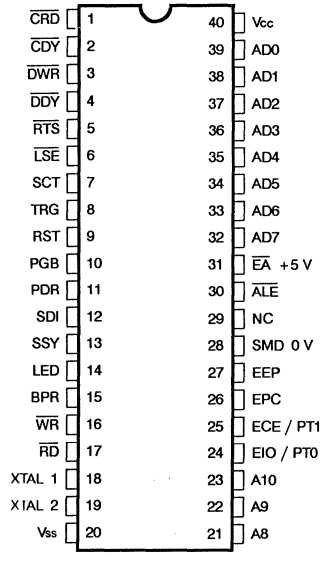
Pin Mnemonics			
AD0 - AD7	Address/Data bus	RTS	Request to send
RxD	Received Data	CTS	Clear to send
TxD	Transmitted Data	RST	IC reset
BR0 - BR1	Baud rate	EEP	EEPROM select
PT0 - PT1	Parity	EPC	EEPROM clock
STB	Stop bits	ECE	EEPROM chip enable
LSE	Laser scan enable	EIO	EEPROM I/O
SCT	Scanner type	TRG	Laser trigger line
SDI	Scanner digital input	SSY	Scanner synchronization
LED	LED control line	A8	Address line #8
BPR	Beeper control line	A9	Address line #9
WR	Data memory write	A10	Address line #10
RD	Data memory read	EA	External program enable
XTAL1	Crystal input	ALE	Address latch enable
XTAL2	Crystal input	Vcc	Power
SMD	Serial Mode Select	Vss	Ground

Figure 3. HBCR-2210 Serial Pinout



Pin Mnemonics	
AD0 - AD7	Address/Data bus
RxD	Received Data
TxD	Transmitted Data
BR0 - BR1	Baud rate
PT0 - PT1	Parity
STB	Stop bits
$\overline{LSE}$	Laser scan enable
SCT	Scanner type
SDI	Scanner digital input
LED	LED control line
BPR	Beeper control line
$\overline{WR}$	Data memory write
$\overline{RD}$	Data memory read
XTAL1	Crystal input
XTAL2	Crystal input
SMD	Serial Mode Select
$\overline{RTS}$	Request to send
$\overline{CTS}$	Clear to send
RST	IC reset
EEP	EEPROM select
EPC	EEPROM clock
ECE	EEPROM chip enable
EIO	EEPROM I/O
TRG	Laser trigger line
SSY	Scanner synchronization
A8	Address line #8
A9	Address line #9
A10	Address line #10
$\overline{EA}$	External program enable
$\overline{ALE}$	Address latch enable
V_{cc}	Power
V_{ss}	Ground

Figure 4. HBCR-2211 Serial Pinout



Pin Mnemonics			
AD0 - AD7	Address/Data bus	PGB	Tranceiver drive enable
$\overline{DWR}$	Data write handshake	PDR	Tranceiver direction control
$\overline{DDY}$	Ready for data handshake	RST	IC reset
$\overline{CRD}$	Command read handshake	EEP	EEPROM select
$\overline{CDY}$	Command ready handshake	EPC	EEPROM clock
PT0 - PT1	Parity	ECE	EEPROM chip enable
$\overline{LSE}$	Laser scan enable	EIO	EEPROM I/O
SCT	Scanner type	TRG	Laser trigger line
SDI	Scanner digital input	SSY	Scanner synchronization
LED	LED control line	A8	Address line #8
BPR	Beeper control line	A9	Address line #9
$\overline{WR}$	Data memory write	A10	Address line #10
$\overline{RD}$	Data memory read	$\overline{EA}$	External program enable
XTAL1	Crystal input	$\overline{ALE}$	Address latch enable
XTAL2	Crystal input	$\overline{RTS}$	Request to send
SMD	Serial Mode Select	V_{cc}	Power
		V_{ss}	Ground

Figure 5. HBCR-2210 Parallel Pinout

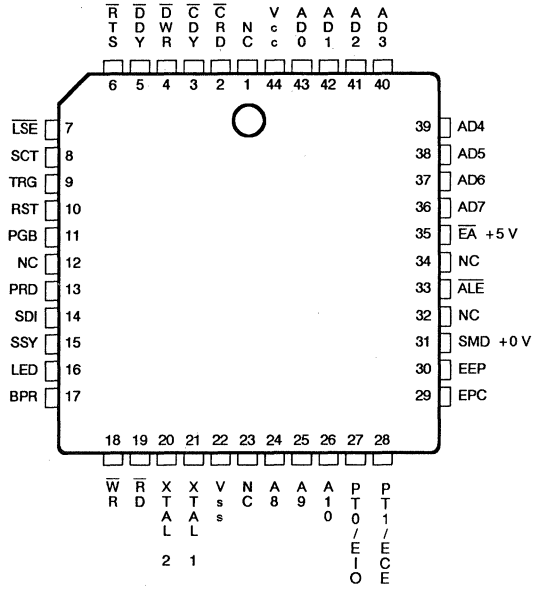


Figure 6. HBCR-2211 Parallel Pinout

Pin Mnemonics	
AD0 - AD7	Address/Data bus
$\overline{DWR}$	Data write handshake
$\overline{DDY}$	Ready for data handshake
$\overline{CRD}$	Command read handshake
$\overline{CDY}$	Command ready handshake
PT0 - PT1	Parity
$\overline{LSE}$	Laser scan enable
SCT	Scanner type
SDI	Scanner digital input
LED	LED control line
BPR	Beeper control line
$\overline{WR}$	Data memory write
$\overline{RD}$	Data memory read
XTAL1	Crystal input
XTAL2	Crystal input
SMD	Serial Mode Select
PGB	Tranceiver drive enable
PDR	Tranceiver direction control
RST	IC reset
EEP	EEPROM select
EPC	EEPROM clock
ECE	EEPROM chip enable
EIO	EEPROM I/O
TRG	Laser trigger line
SSY	Scanner synchronization
A8	Address line #8
A9	Address line #9
A10	Address line #10
$\overline{EA}$	External program enable
$\overline{ALE}$	Address latch enable
$\overline{RTS}$	Request to send
V_{cc}	Power
V_{ss}	Ground

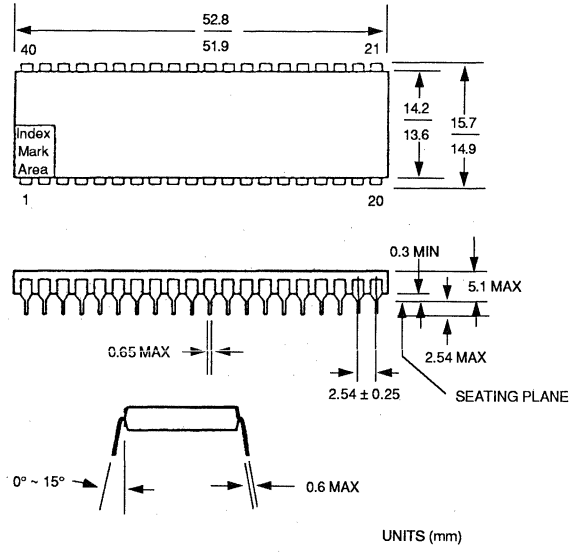


Figure 7. HBCR-2210 Mechanical Specifications

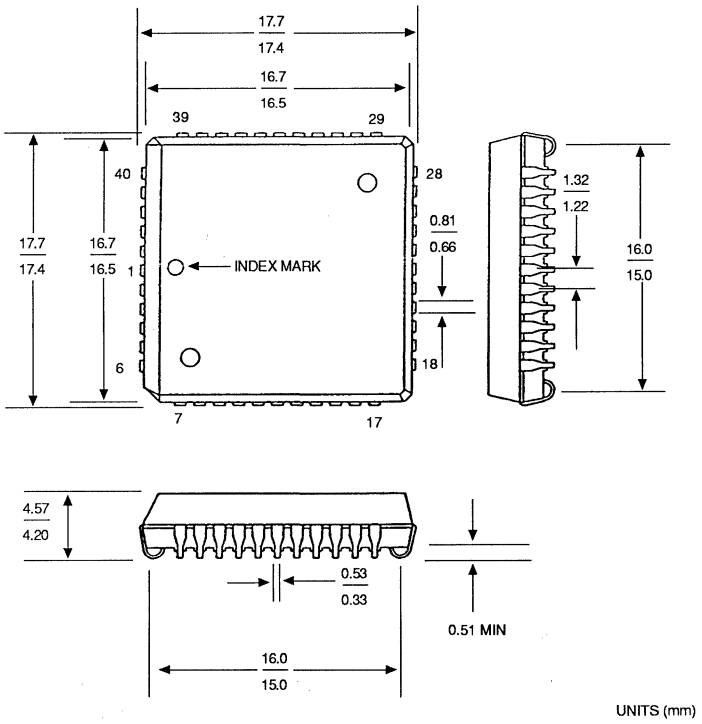


Figure 8. HBCR-2211 Mechanical Specifications

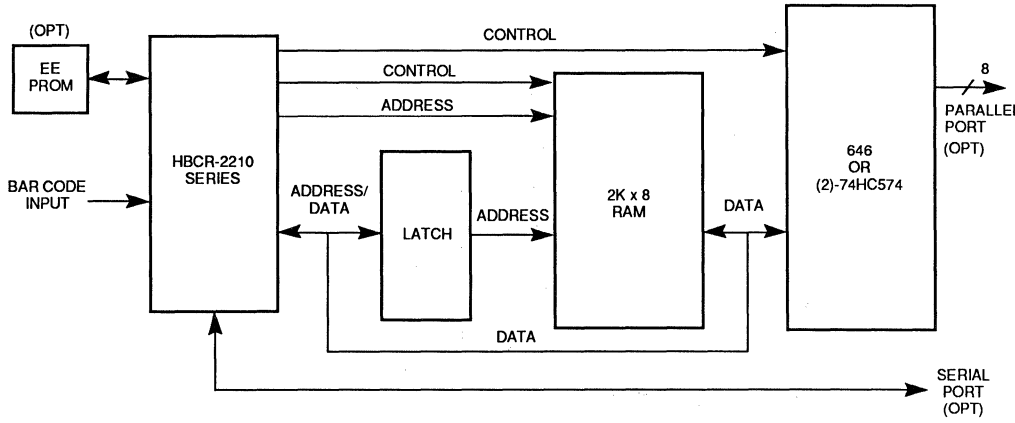


Figure 9. System Block Diagram

Warranty and Service

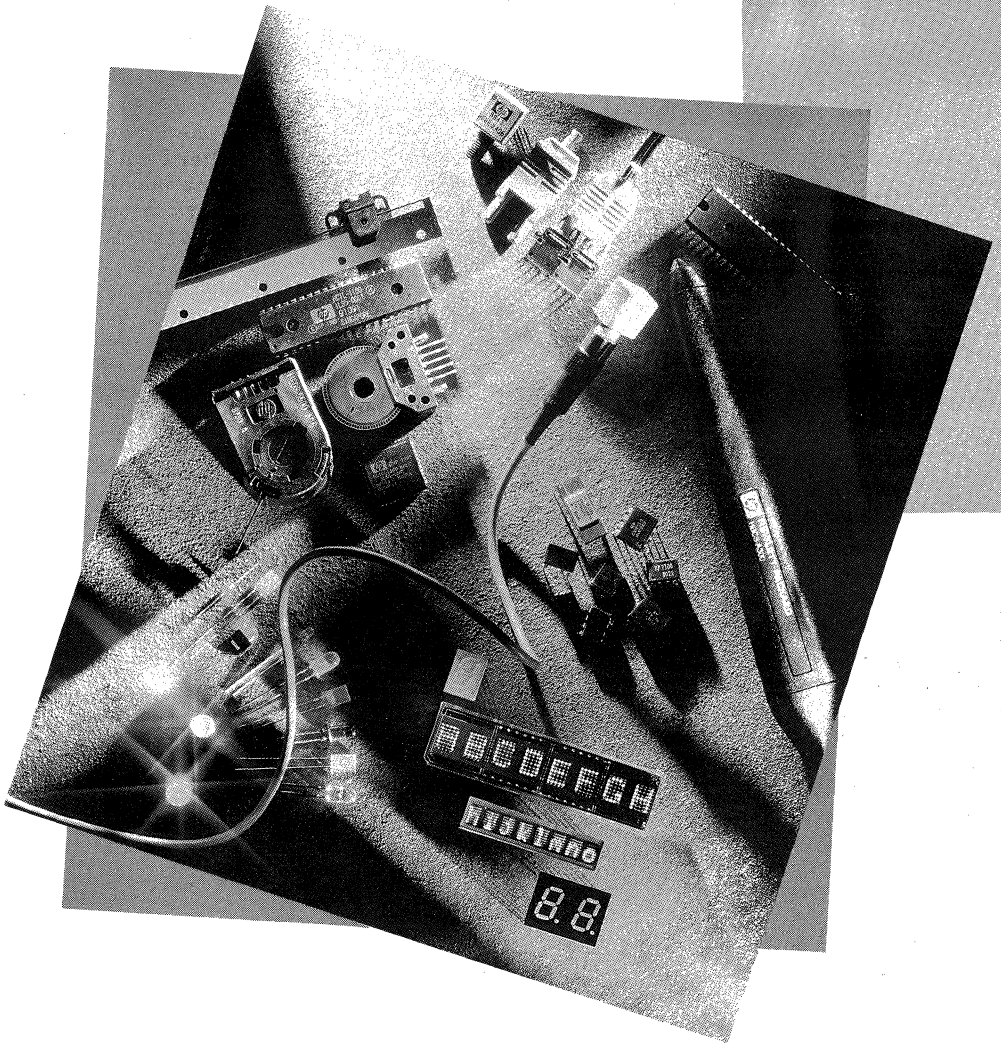
The HP Decode IC is warranted for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

For additional warranty or service information please contact your local Hewlett-Packard sales representative or authorized distributor.

HEWLETT PACKARD

Applications



HEWLETT PACKARD

Applications

Because technology is growing and changing so rapidly, HP's commitment to customers includes an extensive applications department. In an effort to anticipate design needs and answer design questions, this team of engineers has published a complete library of applications literature.

All of the Application Notes, Bulletins and Technical Briefs listed here, are available from your local HP Sales Office or nearest HP Components Authorized Distributor or Representative. In the U.S. call 1-800-537-7715 and in Canada call 1-800-387-3867.

Motion Sensing & Control Products

AN 1011
Design and Operational Considerations for the HEDS-5000 Incremental Shaft Encoder

This application note is directed toward the system designer using the HEDS-5000 and HEDS-6000 modular incremental shaft encoders. First the note briefly analyzes the theory of design and operation of the HEDS-5000 and HEDS-6000. A practical approach to design considerations and an error analysis provide an in depth treatment of the relationship between motor mechanical parameters and encoding error accumulation. Several design examples demonstrate the analysis techniques presented. Operation considerations for assembly, test, trouble shooting and repair are presented. Finally, some circuits and software concepts are introduced which will be useful in interfacing the shaft encoder to a digital or microprocessor based system.

Appendix A summarizes the uses and advantages of various encoder technologies while Appendix B provides guidance for selecting DC motors suitable for use with the HEDS-5000 and HEDS-6000.

Ordering No. 5953-9393

AN 1025
Applications and Circuit Design for the HEDS-7500 Series Digital Potentiometer
This application note demonstrates some of the uses for the Hewlett-Packard HEDS-7500 series digital potentiometer, explains how a digital potentiometer works, and explains some of the advantages of a digital potentiometer over a standard resistive potentiometer. In addition, this application note provides some examples of circuitry which will interface the digital potentiometer to a microprocessor, and provides mechanical design considerations and available options for the HEDS-7500 series digital potentiometer.

Ordering No. 5954-8485

AN 1032
Design of the HCTL-1000's Digital Filter Parameters by the Combination Method
Digital closed loop motion control systems employing a dedicated IC as a controller are becoming increasingly popular as a solution to the need for controlled velocity and positioning systems. Hewlett-Packard's HCTL-1000 is a general purpose motion control IC which has been designed for this type of closed loop systems. A digital compensator has been designed into the HCTL-1000 to provide a stable response to an input command. This application note explains how the combination method can be used for calculation of the HCTL-1000's digital compensation filter parameters to provide a stable, closed loop position control system.

Ordering No. 5954-8455

Light Bars & Bar Graph Arrays

AN 1007
Bar Graph Array Applications
This application note begins with a description of the manufacturing process used to construct the 10 element array. Next is a discussion of the package design and basic electrical configuration and how they affect designing with the bar graph array. Mechanical information including pin spacing and wave soldering recommendations are made.

Display interface techniques of two basic types are thoroughly discussed. The first of these two drive schemes is applicable in systems requiring display of analog signals in a bar graph format. The second major drive technique interfaces bar graph arrays in systems where the data is of a digital nature. Examples of microprocessor controlled bar graph arrays are presented.

Summarized for the design engineer are tables of available integrated circuits for use with bar graph arrays. Finally, a list of recommended filters is included.

Ordering No. 5953-0452

AN 1012
Methods of Legend Fabrication
Hewlett-Packard LED Light Bar Modules inscribed with fixed messages or symbols can be used as economical annunciators. Annunciators are often used in front panels to convey the status of a system, to indicate a selected mode of operation, or to indicate the next step in a sequence. This application note discusses alternative ways the message or symbols (legends) can be designed. A selection matrix is provided to assist in the selection of the most appropriate method of legend fabrication. Each fabrication method is explained in detail along with mounting and attachment techniques. Finally, prevention of cross-talk is discussed for legend areas of a multi-segmented light bar.

Ordering No. 5953-0478

Solid State Lamps

AB 74
Option 002 Tape and Reel LED Lamps
Hewlett-Packard Option 002 tape and reel LED lamps have straight leads on standard 2.54 mm (0.100 inch) center spacing. These lamps may be auto-inserted into printed circuit boards with most radial auto-insertion equipment. However, it is important to have the proper plated through hole size and spacing, in the printed circuit to assure high insertion yields.

This application bulletin details the specific information on the printed board plated through hole size, spacing, and tolerances necessary to assure high insertion yields of Option 002 LED lamps with 0.46 mm (0.018 inch) square leads.

Ordering No. 5954-8402

AN 1005
Operational Considerations for LED Lamps and Display Devices
In the design of a display system which incorporates LED lamps and display devices, the objective is to achieve an optimum between light output, power dissipation, reliability, and operating life. The performance characteristics and capabilities of each LED device must be known and understood so that an optimum design can be achieved. The primary source for this information is the LED device data sheet. The data sheet typically contains Electrical/Optical Characteristics that list the performance of the device and Absolute Maximum Ratings in conjunction with characteristic curves and other data which describe the capabilities of the device. A thorough understanding of this information and its intended use provides the basis for achieving an optimum design. This application note presents an in-depth discussion of the theory and use of the electrical and optical information contained within a data sheet. Two designs using this information in the form of numerical examples are presented, one for dc operation and one for pulsed (strobed) operation.

Ordering No. 5953-0419

AN 1017
LED Solid State Reliability
Light emitting diode display technology offers many attractive features including multiple display colors, sunlight readability, and a continuously variable intensity adjustment. One of the most common reasons that LED displays are designed into an application, however, is the high level of

reliability of the LED display. Hewlett-Packard has taken a leadership role in setting reliability standards for LED displays and documenting reliability performance.

This note explains how to use the reliability data sheets published for HP LED indicators and displays. It describes the LED indicator and display packages, defines device failures, and discusses parameters affecting useful life, failure rates, and mechanical test performance.

Ordering Number 5953-7784

AN 1021
Utilizing LED Lamps Packaged on Tape and Reel
Hewlett-Packard offers many of its LED lamps packaged on tape and reel for radial insertion by automatic equipment during high volume production of PC board assemblies.

This application note is a guide to the use of tape and reel LED lamps in the automatic insertion process. Discussed are the LED lamp tape and reel configuration, the radial lead insertion process, PC board design considerations, a method to maintain LED lamp alignment during soldering, and lamp stand-off height information.

Ordering No. 5954-0861

AN 1027
Soldering LED Components
The modern printed circuit board is assembled with a wide variety of semiconductor components. These components may include LED lamps and displays in combination with other components. The quantity of solder connections will be many times the component count. Therefore, the solder connections must be good on the first pass through the soldering process. The effectiveness of the soldering process is a function of the care and attention paid to the details of the process. It is important for display system designers and PC board assembly engineers to understand the aspects of the soldering process and how they relate to LED components to assure high yields.

This application note provides an in-depth discussion on the aspects of the soldering process and how they relate to LED lamps and display components, with the objective of being to serve as a guide towards achieving high yields for solder connections.

Ordering No. 5954-0893

AN 1060
Surface Mounting SMT LED Indicator Components
Circuit board assemblies using surface mount technology (SMT) are now common and SMT LED indicators are being used on many of these SMT board assemblies. This application note gives the Standard EIA tape and reel packaging information for SMT LED indicators. Recommended pc board pad layout designs are given for each type of SMT LED component. Automatic placement considerations, solder paste, and Type 2 pc board processing issues are discussed. Recommended temperature profiles are presented for both convective IR reflow and vapor phase (VPS) reflow soldering processes. A brief discussion of conductive attachment is included. An industry standard rework technique is described in detail.

Ordering No. 5091-6704E

AN 1061
Light Output Degradation of Emerald Green Solid State Lamps
Emerald Green material has demonstrated a different light output degradation pattern vs other II V materials. Differences include larger standard deviation within a sample and suggestions of varied performance from lot-to-lot. This application note reports the observed differences between Standard Green LEDs and Emerald Green LEDs on light output degradation vs. time. Design Engineers could utilize tis information in their applications.

Ordering No. 5091-7778E

Solid State Displays

AN 1006
Seven Segment LED Display Applications
This application note begins with a detailed explanation of the two basic product lines that Hewlett-Packard offers in the seven segment display market. This discussion includes mechanical construction techniques, character heights, and typical areas of application. The two major display drive techniques, dc and strobed, are covered. The resultant tradeoffs of cost, power, and ease of use are discussed. This is followed by several typical instrument

applications including counters, digital voltmeters, and microprocessor interface applications. Several different microprocessor based drive techniques are presented incorporating both the monolithic and the large seven segment LED displays.

The application note contains a discussion of intensity and color considerations made necessary if the devices are to be end stacked. Hewlett-Packard has made several advances in the area of sunlight viewability of LED displays. The basic theory is discussed and recommendations made for achieving viewability in direct sunlight. Information concerning display mounting, soldering, and cleaning is presented. Finally, an extensive set of tables has been compiled to aid the designer in choosing the correct hardware to match a particular application. These tables include seven segment decoder/drivers, digit drivers, LSI chips designed for use with LEDs, printed circuit board edge connectors, and filtering materials.

Ordering No. 5953-0439

AN 1015
Contrast Enhancement Techniques for LED Displays
Contrast enhancement is essential to assure readability of LED displays in a variety of indoor and outdoor ambients. Plastic filters are typically used for contrast enhancement with indoor lighting and glass circular polarized filters are typically used to achieve readability in sunlight ambients.

This application note discusses contrast enhancement technology for both indoor and outdoor ambients, the theory of Discrimination Index and provides a list of tested contrast enhancement filters and filter manufacturers.

Ordering No. 5953-7788

AN 1016
Using the HDSP-2000 Alphanumeric Display Family
The HDSP-2000 family of alphanumeric display products provides the designer with a variety of easy-to-use display modules with on board integrated circuit drivers. The HDSP-2000 family has been expanded to provide three display sizes with character heights ranging from 3.8 mm (0.15 in.) to 6.9 mm (0.27 in.), four display colors, and both commercial and military versions. These displays can be arranged to create both single line and multiple line alphanumeric panels.

This note is intended to serve as a design and application guide for users of the HDSP-2000 family of alphanumeric display devices. It covers the theory of the device design and operation, considerations for specific circuit designs, thermal management, power derating and heat sinking, and intensity modulation techniques.

Ordering No. 5953-7787

AN 1026
Designing with Hewlett-Packard's Smart Display – the HPDL-2416
The trend in LED Alphanumeric displays is to simplify a designer's job as much as possible by incorporating on board character storage, ASCII character generation, and multiplexing within the display. The HPDL-2416 is a four character alphanumeric display which incorporates a 64 character ASCII decoder and an on board CMOS IC to perform these functions. This application note is intended to serve as a design and application guide for users of the HPDL-2416. The information presented will cover electrical description, electrical design considerations, interfacing to micro-processors, preprogrammed message systems, mechanical and electrical handling, and contrast enhancement.

Ordering No. 5954-0936

AN 1029
Luminous Contrast and Sunlight Readability of the HDSP-238X Series LED Alphanumeric Displays for Military Applications
Military specifications for avionics and other kinds of electronics that require readability in sunlight use specific definitions for luminous contrast. The concept of chrominance contrast and the theory of Discrimination Index (see Hewlett-Packard Application Note 1015) are not used by the military as a means of determining readability in sunlight. Thus, the military requirements for readability in sunlight are based solely on luminous contrast measurements. This application note discusses the luminous contrasts used by military specifications, describes anti-reflection/circular polarized

filters designed for use with the HDSP-238X series sunlight viewable LED displays, and presents luminous contrast data for various HDSP-238X display/ filter combinations.

Ordering No. 5954-0923

AN1030
LED Displays and Indicators and Night Vision Imaging System Lighting
This application note introduces the concept of night vision imaging. It discusses GEN II and GEN III ANVIS and Cat's Eyes night vision goggles. NVG compatibility problems and compatible lighting objectives for aircraft cockpits are discussed. It illustrates the use of NVG filters with high performance green and yellow LEDs to obtain NVG compatibility. Various aspects of MIL-L-85762A, as they apply to LEDs, are discussed. Calculated NVIS Radiance values are presented for high performance green and yellow LED/NVG/DV filter combinations. A discussion of the U.S. Army's NVG Secure Lighting Program and the objectives of the CECOM SOW are included. Information on dimming LED displays is presented. Daylight readability with NVG/DV filters is also discussed.

Ordering No. 5954-2245

AN 1031
Front Panel Design
In many applications designers are faced with the problem of how to match the perceived brightness of an assortment of seven segment displays, light bars, linear arrays, and lamps on the same front panel. To simplify this problem Hewlett-Packard has introduced S02 option selected parts. S02 option selected parts provide a restricted range of luminous intensity for a given part number. This application note is written as a design guide to matching the perceived brightness of LED displays and lamps on a front panel. The procedure shown in the application note will enable the designer to calculate the needed display drive currents (either dc or pulsed) for a given ambient light level and specified filter. Two technques are explained. The first is how to calculate the drive currents to insure minimum acceptable brightness. The second is how to calculate the drive currents to match the display on the front panel to a known display.

Ordering No. 5954-0933

AN 1033
Designing with the HDSP-211X Smart Display Family
Hewlett-Packard's smart alphanumeric display, the HDSP-211X, is built to simplify the user's display design. Each HDSP-211X has an onboard CMOS IC which displays eight characters. All of the IC features are software driven. These features include 128 character ASCII decoder, 16 user-defined symbols, seven brightness levels, flashing characters, a self test, and all of the circuitry needed to decode, drive, and refresh eight 5 x 7 dot matrix characters.

This application note discusses how to interface the HDSP-211X display to either a Motorola 6808 or an Intel 8085 microprocessor. A 32 character display interface is explained for each microprocessor. The note includes a detailed description of the hardware and software. The software illustrates how the user-defined symbols and a string of ASCII characters are loaded into the display.

Ordering No. 5954-8424

AN 1039
Dimming HDSP-213X Displays to Meet Night Vision Lighting Levels
Abstract
For normal operation, the seven programmable dimming levels available with the HDSP-213X military grade displays are sufficient. However, the displays must be dimmed well below the lowest available on-board programmable dimming level to meet the requirements for night vision imaging system (NVIS) lighting. This application note describes a circuit that will dim HDSP-213X displays to luminance levels sufficient to meet NVIS lighting requirements.

Ordering No. 5952-0708

Fiber Optics

Application Bulletin 65
Using 50/125 μm Optical Fiber with Hewlett-Packard Components
This AB discusses the 50/125 μm cable as it relates to light losses due to attenuation, mechanical and optical limits; the tests used to determine these losses; how optical power is calculated; and how full system performance can be predicted using this data. This AB is applicable to any fiber-

optic product in the catalog.

Ordering No. 5953-9370

Application Bulletin 73
Low-Cost Fiber Optic Transmitter and Receiver Interface Circuits
This AB assists in designing circuits to interface HP HFBR-0400 low-cost miniature fiber-optic components with TTL 1/0 for applications at data rates up to 35 MBd. The TTL transistor/receiver circuits shown were designed, built, and tested; and are suitable for a wide range of applications. The HFBR-0400 fiber-optic components are compatible with either SMA or ST style connectors. The concepts illustrated here are applicable to both types of connectors.

Ordering No. 5954-8415

Application Bulletin 78
Low-Cost Fiber Optic Links for Digital Applications up to 150 MBd
This AB concentrates on a specific digital application, one of the most prevalent for the HFBR-24X6, the transmission of encoded digital signals, otherwise known as run-length limited data. Circuit diagrams illustrate the various concepts. The AB is divided into the following topics:
- The HFBR-2406/-2416 high performance components
- Applications for 820 nm LED-based fiber-optic links
- Advantages of run-limited code
- Designing with fiber-optic components
- Testing fiber-optic systems
- Testing fiber-optic systems
- TTL transmitter performance
- ECL transmitter performance
- Receiver design
- Error rate versus signal-to-noise ratio
- Advantages of hysteresis
- Low-pass filtering to enhance receiver sensitivity
- Compromises associated with high-speed 820 nm links
- High-frequency circuit design
- EMI issues
- Applications support

Ordering No. 5954-8478

AN 1035
Versatile Link
This AN describes how fiber optics can be used to solve many different types of application problems, introduces HP's Versatile Link plastic fiber optics, and shows how to design a fiber-optic link using the Versatile Link. The AN, which is applicable to the HFBR-0500 series, is divided into the following topics:
- Introduction
- Example Applications
- Versatile Link Description
- System Specifications and Link Design
- Pulse-Width Distortion
- Additional Circuit Recommendations
- Appendix

Ordering No. 5954-2191

AN 1037
Surface Mount Flatpack (HBIC-XXXX) Mounting
This application note describes appropriate techniques for RF grounding, PWB pad layout, and solder attachment of the HBIC-XXXX series of surface mount flatpacks used for RF and High Speed Digital hybrid and MMIC circuits.

Ordering No. 5954-2211

AN 1038
Low-Cost Components for IEEE 802.3 Fiber Optic Inter-Repeater Links
This AN is applicable to the HFBR-0400 family of fiber-optic products. It explains some system specifications and specifies values for the Fiber-Optic Inter-Repeater Links (FOIRL) described in the IEEE 802.3 standard. Among the topics discussed are:
- FOIRL System specifications, which list the key parameters required by the IEEE standard
- Overall circuit design
- Designs specific to the transmitter and receiver circuits
- Run-length-limited link performance, containing tables of specifications, and burst-mode applications.

Ordering No. 5954-2215

AN 1045
High-Speed Plastic, Fiber-Optic Link
This AN discusses the speed limitations of plastic optical fiber and Hewlett-Packard's new transmitter and receiver components that can transmit data through these fibers at up to 50 MBd. The paper is divided into three sections. The first one deals with understanding and using the data sheets; the second one discusses coupled power and the optical power budget; the third section explains circuit operation and the considerations involved in its design. The topics in this last section include:
- Transmitter configuration
- Receiver circuit operation
- The power supply filter
- Layout of the printed circuit

Ordering No. 5091-3024E

AN 1057
Conductive Port Receiver
This AN compares the performance of fiber-optic receivers with conductive ports to fiber-optic receivers with non-conductive ports. It explains how conductive port receivers solve specific problems encountered in some applications and how they help to improve the electromagnetic immunity of part number HFBR-24X6 XC, required by such standards as MIL 461 and IEC 801.3. The application note also presents test data that shows why HP's low-resistance conductive port has an advantage over the higher-resistance conductive ports of other manufacturers.

Ordering No. 5091-6001E

AN S011
Using Silicon MMIC Gain Blocks as Transimpedance Amplifiers
Key specifications and performance evlauation.

Ordering No. 5091-7798E

AN S015
ITA Series Transimpedance Amplifiers
Transimpedance (TZ) amplifiers are a critical element in digital fiber optic receivers. Their role is to take the current output from a photo diode, and convert it to a voltage. This application note gives an overview of Hewlett-Packard's ITA series of transimpedance amplifiers for high speed application s(100 Mb/s to 1.5 Gb/s). Tips on how to get optimum RF performance with the amplifiers are given. Recommended PC board layouts are given for ITAs in chip and package form.

Ordering No. 300455

AN 1055
Clock Recovery Using Si MMICs
One of the functions that must be performed by a fiver optic receiver is the retiming of the output data stream. This clock recovery function can be done using an active mixer (the IAM-81 or IAM-82 series) as a transition detector, a SAW filter, and a limiting amplifier (MSA, INA or IVA series). This application note discusses how these parts can be combined to construct a clock recovery circuit.

Ordering No. 5091-4917E

AN 1051
The IDA-07318 Laser Diode Driver
The IDA-07318 is a high speed silicon Monolithic Microwave Integrated Circuit (MMIC) laser diode driver (LDD) capable of operating at data rates up to 1.5 Gb/s. This application note discusses how to properly drive the IDA-07318 and how to use the modulation and prebias inputs on the laser driver. A brief overview of the theory of operation of the laser driver is covered.

Ordering No. 5091-4927E

Technical Brief 101
Fiber Optic SMA Connector Technology
This TB discusses tradeoffs between various SMA connector techniques. It cross-references manufacturers of SMA connectors with SMA connector types; and is applicable to the HFBR-2414 fiber-optic receiver.

Ordering No. 5954-1004

Technical Brief 102
Fiber/Cable Selection for LED-Based Local Communications Systems
This TB, which is applicable to the HFBR-1402/1404 fiber-optic transmitters, is intended to assist the first-time user of fiber optics with the selection of a fiber cable that best meets desired system requirements. Issues discussed in this brief include:
- Trade-offs between various fiber types
- The effect of LED emitters on fiber performance
- Coupled power versus numerical aperture
- Factors that influence cable selection

Also included is a cross-references of manufacturers of fiber cable with cable type.

Ordering No. 5954-1011

Technical Brief 104
Baseband Video Transmission with Low-Cost Fiber-Optic Components
The transmission of video signals over fiber-optic links offers several advantages compared to wire distribution systems. This TB describes simple Transistor/Resistor circuits that provide 20 MHz, 3 dB bandwidth for high-resolution analog video transmission. This TB is applicable to the HFBR-2414 fiber-optic receiver.

Ordering No. 5954-1025

Technical Brief 105
ST Connector/Cable Guide
Although developed fairly recently by AT & T, the rapid acceptance of the ST* connector

by users of fiber-optic components indicates that it may soon become a standard. This TB provides a quick comparison between the SMA and the ST-style connector. Some suppliers of the ST- style connectored cables are tabulated. This TB is applicable to the HFBR-2416 fiber-optic receiver.

Ordering No. 5954-8436

Optocouplers

Application Bulletin 69
CMOS Circuit Design Using Hewlett-Packard Optocouplers
This AB illustrates CMOS isolation interface circuits for use with the various, low input current, HCPL-2200/-2300/ -2731 and 6N139 optocouplers. Advantages of and recommendations for different input and output circuit configurations for low-power operation at various signalling rates are tabulated.

Ordering No. 5953-9384

AN 947
Digital Data Transmission Using Optically Coupled Isolators
Optocouplers make ideal line receivers for digital data transmission applications. They are especially useful for elimination of common-mode interference between two isolated data transmission systems. This AN describes design considerations and circuit techniques with special emphasis on selection of line drivers, transmission lines, and line receiver termination for optimum data rate and common-mode rejection. Both resistive and-active terminations are described for multiplexing applications, and for common-mode rejection and data rate enhancement. This AN is applicable to the 6N136 and 6N137 or any other HP digital optocoupler.

Ordering No. 5953-7759

AN 951-1
Applications for Low-Input-Current, High-Gain Optocouplers
Optocouplers are useful in line receivers, logic isolation, medical equipment, power lines, and telephone lines. This AN discusses the use of the 6N138/9 series of high-CTR optocouplers in each of these areas.

Ordering No. 5953-7794

AN 951-2
Linear Applications of Optocouplers
Although optocouplers are not inherently linear, the separate photodiodes used in HP devices provide better linearity as well as higher speed of response than phototransistor detectors.

Using paired optocouplers to enhance linearity is described with specific circuit examples offering dc-to-25 KHz response. These examples illustrate the relative merits of differential and servo techniques. A circuit with linear ac response to 10 MHz is also described for analog optocouplers having the photodiode terminals externally accessible.

The AN also discusses digital techniques of voltage-to-frequency conversion and pulse-width modulation. Their linearity is quite independent of optocoupler linearity but requires use of high-speed optocouplers for low distortion. The AN is applicable to the HCPL-2530.

Ordering No. 5954-8430

AN 1002
Consideration of CTR Variations in Optocoupler Circuit Designs
A persistent, and sometimes crucial concern of designers using optocouplers is that of the current transfer ratio, CTR, changing with time. The change, or CTR degradation, must be accounted for if long, functional lifetime of a system is to be guaranteed. This AN discusses a number of different sources for this degradation. This AN is applicable to the 4N45 and 4N46 optocouplers.

Ordering No. 5953-7799

AN 1004
Threshold Sensing for Industrial Control Systems with the HCPL-3700 Interface Optocoupler
Interfacing from industrial control systems to logic systems is a necessary operation to monitor system progress. This interfacing is found in a variety of applications, including:
- Process control systems
- Programmable controllers
- Microprocessor subsystems that monitor proximity and limit switches
- Environmental sensors and ac line status
- Switching power supplies for detection of ac power loss
- Power back-up systems that need an early warning of power loss to save special microprocessor memory information or switch to battery operation, etc.

Applications of the HCPL-3700 interface optocoupler are addressed in this note. The ability of the HCPL-3700 to detect thresholds and isolate systems, allows it to provide unique features that no other optocoupler can provide. Addressed in this note are the advantages of using this optocoupler for isolating systems as well as the device characteristics, dc/ac operational performance with and without filtering, simple calculations for setting desired thresholds, and four typical application examples.

Additional information focuses on protecting the optocoupler from power transients, considerations of thermal conditions, and electrical safety requirements of the industrial control environment.

Ordering No. 5953-0406

AN 1018
Designing with the HCPL-4100 and HCPL-4200 Current-Loop Optocoupler
Digital current loops provide unique advantages of large noise immunity and long-distance communication at low cost. Applications are wide and varied for current loops, but one of the critical concerns for designers of loop systems is to provide a predictable, reliable and isolated interface. The HCPL-4100 (transmitter) and HCPL-4200 (receiver) optocouplers provide easy interfacing to and from a current loop with minimal design effort.

This AN completely describes the HCPL-4100/4200 optocouplers and lists applications for digital, 20 mA, simplex, half-duplex and full-duplex loops. These loops can be either point-to-point or multidrop configurations. Factors that affect data performance are discussed. Circuit arrangements with specific data performance are given in graphical and tabular form.

Ordering No. 5953-9359

AN 1023
Radiation Immunity of Hewlett-Packard Optocouplers
This AN opens with a quotation from MIL-HDBK-279, which describes optocouplers that contain photodiodes as being superior to optocouplers that contain phototransistors.

The AN continues with a description of the properties of ionizing radiation (particles and photons) and how it affects the performance of optocouplers. Graphs show degradation of CTR (Current Transfer Ratio) in the 6N140 as a function of gamma total dose (up to 1000 rad (Si)) and as a function of total neutron fluence (up to 6 x 10^{12} neutrons/cm^2). A table gives radiation hardness requirements for various military applications.

Ordering No. 5954-1003

AN 1024
Ring Detection with the HCPL-3700 Optocoupler
With the increased use of modems, automatic phone answering equipment, private automatic branch exchange (PABX) systems, etc., low-cost, reliable, isolated ring detection becomes important to many electronic equipment manufacturers. This AN defines the ringing requirements (U.S.A. and Europe), and the applications of the HCPL-3700 optocoupler as a simple, but effective, ring detector.

A design example is shown with calculations to illustrate proper use of the optocoupler. Features integrated into the HCPL-3700 provide predictable detection, protection and isolation with greater ease than is possible with other optocouplers.

Ordering No. 5954-1006

AN 1036
Small-Signal Solid-State Relays
This AN introduces the solid-state relay (SSR), an alternative to the electromechanical relay; contrasts its mode of operation; describes the SSR's features and some of its applications. The AN is applicable to the HSSR-8200/8400.

Ordering No. 5954-2200

AN 1043
Common-Mode Noise: Sources and Solutions
This AN is divided into three sections. The first section defines and describes common-mode noise (CMR). The second section lists some typical sources, which can be either coupled from an external device or can be inherent in the design. The third section explains the methods that can limit the amount of CMR. The last section explains the technology of an optocoupler that allows a low-cost solution to the problem. The AN is applicable to the

HCPL-2211/2611/4503 optocouplers.

Ordering No. 5091-1866E

AN 1046
Low On-Resistance, Solid-State Relays
The on-resistance specification of a solid-state relay (SSR) is important because, in general, a lower on-resistance allows a higher contact current rating and more closely resembles an ideal switch. This application note begins with a description of the main characteristics of the HSSR-8060 and HSSR-8400, two of Hewlett-Packard's low on-resistance SSRs. A control drive circuit is recommended and suggestions for overvoltage protection are discussed. Also, this application note includes examples of the SSRs in telecommunications, multiplexing, and industrial control applications; and with various types of loads.

Ordering No. 5091-3123E

AN 1047
Low On-Resistance Solid-State Relays for High-Reliability Applications
This AN shows the main characteristic of the HSSR-7110 Power MOSFET optocoupler and how this component operates as a low on-resistance solid-state relay. Several control drive circuits are described.

Ordering No. 5091-4502E

AN 1058
Power Transistor Gate/Base Drive Optocouplers
Hewlett-Packard offers an expanded choice of optocouplers that can directly drive power MOSFETS, IGBTs, and bipolar power transistors. This application note describes the main features of the HCPL-3000, HCPL-3100 and HCPL-3101 power driver optocouplers. Also included are application guidelines for three-phase power inverters.

Ordering No. 5091-6000E

AN 1059
High-CMR Isolation Amplifier for Current-Sensing Applications
In 1992, Hewlett-Packard introduced the world's smallest isolation amplifier, the HCPL-7800. This paper describes the theory of operation for the HCPL-7800 as well as a typical application circuit for motor current sensing.

Ordering No. 5091-6315E

Technical Brief 103
High-Speed Optocouplers vs. Pulse Transformers
Pulse transformers are often used for high-speed signaling with ground loop isolation. This TB summarizes the difficulties encountered in using pulse transformers, such as rise-time, sag, and interwinding capacitance. A table summarizes the parameters of Hewlett-Packard optocouplers designed for high-speed signaling. A second table summarizes the advantages of using these optocouplers instead of pulse transformers. This TB is applicable to the following products: HCPL-2200/2300/2400/ 2430/2601/2630/2631 optocouplers.

Ordering No. 5954-1017

Bar Code Components

Application Bulletin 75
ESD Control in Portable Bar Code Readers
This AB, which is applicable to the HBCS-AXXX and HBCS-6XXX series wands, provides information to help the designer of portable barcode decoders to harden their system to electrostatic discharge (ESD).

Ordering No. 5954-2170

Application Bulletin 77
Interfacing the HP SmartWand
This AB, which is applicable to the HBCR-8XXX series, provides circuits to allow the user to interface the HP SmartWand to true RS232 connections.

Ordering No. 5954-2176

AN 1008
Optical Sensing with the HBCS-1100
This AN gives the basic optical flux coupling design for discrete emitters and detectors. It presents the concepts of modulation transfer function, depth of field, and reflective sensor design. It also discusses the optical and electrical operation of the HBCS-1100 High-Resolution optical sensor. Finally, it presents electrical design techniques that allow the HBCS-1100 to interface with popular logic families.

Ordering No. 5091-7363E

AN 1013
Elements of a Bar Code System
This AN, which is applicable to all HP digital wands, describes in detail the elements that make up most bar code systems. Included is a discussion of the fundamental system design, detailed discussion of seven popular code symbologies, a section on symbol generation, and methods of data entry. A glossary of terms and a reference section are also included. This is an excellent publication for people who are just learning about bar code or for those who need a more comprehensive understanding of the subject.

Ordering No. 5953-9387

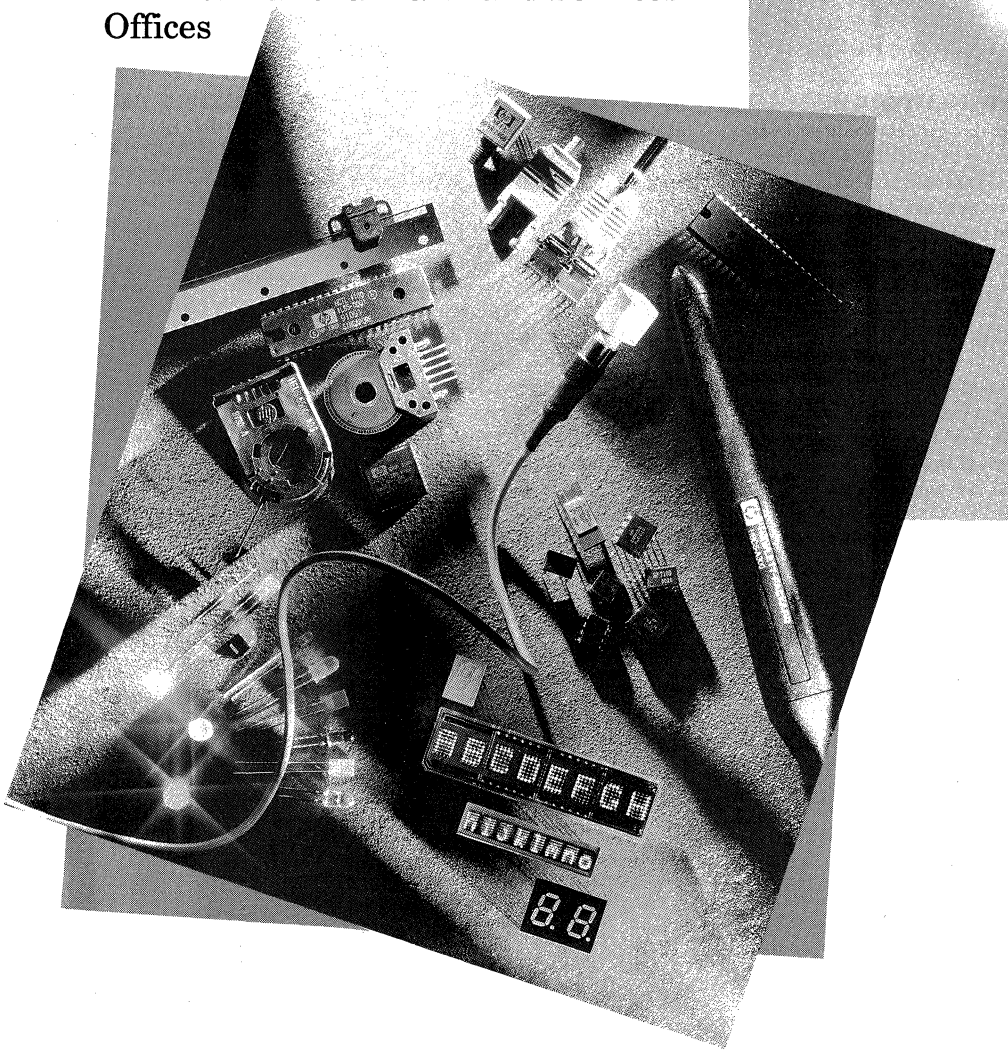
AN 1040
Ambient Light Rejection Circuit for the HED5-1500
Bright ambient light causes the resolution of the HEDS-1500 sensor to degrade when the sensor is dc driven. This AN presents a circuit schematic that allows full resolution in bright ambient light. Included are graphs showing limits of current and voltage, and frequency responses under specific conditions.

Ordering No. 5952-2228

HEWLETT PACKARD

Appendix

- Ordering Information
- HP Components Authorized Distributor and Representative Directory
- HP Components U.S. Sales and Service Offices
- HP International Sales and Services Offices



HEWLETT PACKARD

Ordering Information, After Sales Service

How to Order

To order any component in this catalog or additional applications information, call the HP office nearest you and ask for a Components representative. A complete listing of the U.S. sales offices is on page 9-10; offices located outside of the U.S. are listed on page 9-11.

A worldwide listing of HP authorized distributors is on page 9-3. These distributors can offer off-the-shelf delivery for most HP components.

Warranty

HP's Components are warranted against defects in material and workmanship for a period of one year from the date of shipment. If HP receives notice of such defects during the warranty period, HP will repair or, at its option, replace components that prove to be defective in material or workmanship under proper use during the warranty period. This warranty extends only to HP customers.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

The foregoing limitation of liability shall not apply in the event that any HP product sold hereunder is determined by a court of competent jurisdiction to be defective and to have directly caused bodily injury, death, or property damage; provided, that in no event shall HP's liability for property damage exceed the greater of $50,000 or the purchase price of the specific product that caused such damage.

HEWLETT® PACKARD

HP Components Authorized Distributor and Representative Directory

Alabama

Arrow/Schweber Electronics[1,2]
1015 Henderson Rd.
Huntsville 35816
(205) 837-6955

Hamilton Hallmark[1,2,3]
4890 University Square
Suite 1
Huntsville 35816
(205) 837-8700

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Arizona

Arrow/Schweber Electronics[1,2]
2415 W. Erie Dr.
Tempe 85282
(602) 431-0030

Hamilton Hallmark[1,2,3]
4637 S. 36th Place
Phoenix 85040
(602) 437-1200

Hamilton Hallmark[1,2]
60 S. McKemy Rd.
Chandler 85226
(602) 902-4700

Newark Electronics[1,2]
1-800-367-3573

Sertek, Inc.[2,3]
2111 East Broadway Rd.
Suite 5
Tempe 85282
(602) 894-9405

Penstock, Inc.
8260 E. Raintree Drive
Suite 206
Scottsdale 85260
(602) 998-4442

California

Arrow/Schweber Electronics[1,2]
26677 W. Agoura Rd.
Calabassas 91302
(818) 880-9686

Arrow/Schweber Electronics[1,2]
6 Cromwell St.
Suite 100
Irvine 92718
(714) 587-0404

Arrow/Schweber Electronics[1,2]
9511 Ridgehaven Ct.
San Diego 92123
(619) 565-4800

Arrow/Schweber Electronics[1,2]
48834 Kato Rd.
Suite 103
Fremont 94538
(510) 490-9477

Hamilton Hallmark[1,2,3]
580 Menlo Dr.
Suite 2
Rocklin 95677
(916) 624-9781

Hamilton Hallmark[1,2]
21150 Califa St.
Woodland Hills 91367
(818) 594-0404

Hamilton Hallmark[1,2]
3170 Pullman St.
Costa Mesa 92626
(714) 641-4100

Hamilton Hallmark[1,2]
(Corporate Office)
10950 W. Washington Blvd.
Culver City 90230
(310) 558-2000

Hamilton Hallmark[1,2]
4545 Viewridge Ave.
San Diego 92123
(619) 571-7540

Hamilton Hallmark[1,2]
2105 Lundy Ave.
San Jose 95131
(408) 435-3500

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
(Corporate Office)
520 Mercury Dr.
Sunnyvale 94086
(408) 730-0300

Penstock, Inc.[2,3]
1401 Highland Ave.
Suite 200
Manhattan Beach 90266
(310) 546-8953

Penstock, Inc.[2,3]
5850 Oberlin Dr.
Suite 208
San Diego 92121
(619) 535-3015

Sertek, Inc.[2,3]
(Corporate Office)
3481 Old Conejo Rd.
Newbury Park, CA 91320
(805) 375-6680

Zeus Electronics[1,2]
6276 San Ignacio Ave.
San Jose 95119
(408) 629-4789

Zeus Electronics[1,2]
22700 Savi Ranch Parkway
Yorba Linda 92687
(714) 921-9000

Colorado

Arrow/Schweber Electronics[1,2]
61 Invernes Dr. East
Suite 105
Englewood 80112
(303) 799-0258

Hamilton Hallmark[1,2,3]
12503 East Euclid Dr.
Suite 20
Englewood 80111
(303) 790-1662

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
(303) 421 7161

Sertek, Inc.
1-800-334-7127

Connecticut

Arrow/Schweber Electronics[1,2]
12 Beaumont Rd.
Wallingford 06492
(203) 265-7741

Hamilton Hallmark[1,2,3]
125 Commerce Ct.
Unit 6
Cheshire 06410
(203) 271-2844

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Florida

Arrow/Schweber Electronics[1,2]
37 Skyline Dr.
Suite 3101
Lake Mary 32746
(407) 333-9300

Arrow/Schweber Electronics[1,2]
400 Fairway Dr.
Deerfield Beach 33441
(305) 429-8200

Hamilton Hallmark[1,2,3]
10491 72nd St. North
Largo 34647
(813) 541-7440

Hamilton Hallmark[1,2]
7079 University Blvd.
Winter Park 32792
1-800-332-8638

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-522-2012

Notes:
1. Optoelectronics
2. RF Diodes/Transistors
3. Microwave and Avantek Products

APPENDIX

Penstock, Inc.[2,3]
700 N. Wickham Rd.
Suite 104
Melbourne 32935
(407) 242-3314

Zeus Electronics[1,2]
37 Skyline Drive, Ste. 3101
Lake Mary 32746
(407) 333-3055

Georgia

Arrow/Schweber Electronics[1,2]
4250 E. River Green Pkwy.
Duluth 30136
(404) 497-1300

Hamilton Hallmark[1,2,3]
3425 Corporate Way
Suite A & G
Duluth 30136
(404) 623-4400

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[1,2,3]
5500 Interstate North Pkwy.
Suite 475
Atlanta 30328
(404) 951-0300

Illinois

Arrow/Schweber Electronics[1,2]
1140 West Thorndale Ave.
Itasca 60143
(708) 250-0500

Hamilton Hallmark[1,2]
1130 Thorndale Ave.
Bensenville 60106
(708) 860-7780

Newark Electronics[1,2]
(Corporate Office)
4801 N. Ravenswood Ave.
Chicago 60640
1-800-367-3573

Penstock, Inc.[2,3]
1250 West Northwest Hwy
Suite 509
Palatine 60067
(708) 934-3700

Indiana

Arrow/Schweber Electronics[1,2]
7108 Lake View Pkwy West Dr.
Indianapolis 46268
(317) 299-2071

Hamilton Hallmark[1,2,3]
4275 W. 96th St.
Indianapolis 46268
(317) 872-8875

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
3304 Mallard Cove Lane
Fort Wayne 46804
(219) 432-1277

Iowa

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Kansas

Arrow/Schweber Electronics[1,2]
9801 Legler Rd.
Lenexa 66219
(913) 451-9542

Hamilton Hallmark[1,2,3]
10809 Lakeview Ave
Lenexa 66215
(913) 888-4747

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
300 S. Clairborne, Suite #A2
Olathe 66062
(913) 829-9330

Kentucky

Hamilton Hallmark[1,2]
1847 Mercer Rd.
Suite G
Lexington 40511
1-800-235-6039

Newark Electronics[1,2]
1-800-367-3573

Maryland

Arrow/Schweber Electronics[1,2]
9800 J. Patuxent Woods Dr.
Columbia 21046
(301) 596-7800

Hamilton Hallmark[1,2,3]
10240 Old Columbia Rd.
Columbia 21046
(410) 988-9800

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
9881 Broken Land Pkwy.
Suite 105
Columbia 21046
(410) 290-3746

Massachusetts

Arrow/Schweber Electronics[1,2]
25 Upton Dr.
Wilmington 01887
(508) 658-0900

Hamilton Hallmark[1,2]
10M Centennial Dr.
Peabody 01960
(508) 532-9808

Newark Electronics[1,2]
1-800-367-3573

Penstock[2,3]
5 Mount Royal Ave.
Marlborough 01752
(508) 624-7300

Zeus Electronics[1,2]
25 Upton Drive
Wilmington 01876
(508) 658-4776

Michigan

Arrow/Schweber Electronics[1,2]
19880 Haggerty Rd.
Livonia 48152
(313) 462-2290

Hamilton Hallmark[1,2,3]
44191 Plymouth Oak Blvd.
Suite 1300
Plymouth 48170
(313) 416-5800

Hamilton Hallmark[1,2]
41650 Gardenbrook
Suite 100
Novi 48375
(313) 347-4271

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Minnesota

Arrow/Schweber Electronics[1,2]
10100 Viking Dr.
Suite 100
Eden Prairie 55344
(612) 941-5280

Hamilton Hallmark[1,2,3]
9401 James Ave., South
Suite 140
Bloomington 55431
(612) 881-2600

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Missouri

Hamilton Hallmark[1,2,3]
3783 Rider Trail South
Earth City 63045
(314) 291-5350

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

New Jersey

Arrow/Schweber Electronics[1,2]
43 Route 46 East
Pine Brook 07058
(201) 227-7880

Arrow/Schweber Electronics[1,2]
4 Stow Rd.
Marlton 08053
(609) 596-8000

Hamilton Hallmark[1,2]
One Keystone Ave.
Bldg. 36
Cherry Hill 08003
(609) 424-0110

Hamilton Hallmark[1,2]
10 Lanidex Plaza West
Parisippany 07054-2715
(201) 515-5370

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.
160 Littleton Road
Suite 201
Parsippany 07754
(602) 998-4442

Notes:
1. Optoelectronics
2. RF Diodes/Transistors
3. Microwave and Avantek Products

New Mexico

Newark Electronics[1,2]
1-800-367-3573

Sertek, Inc.[2,3]
(602) 894-9405

New York

Arrow/Schweber Electronics[1,2]
20 Oser Ave.
Hauppauge 11788
(516) 231-1000

Arrow/Schweber Electronics[1,2]
3375 Brighton-Henrietta Townline Rd.
Rochester 14623
(716) 427-0300

Arrow/Schweber Electronics[1,2]
(Corporate Office)
25 Hub Dr.
Melville 11747
(516) 391-1148
(Military)

Hamilton Hallmark[1,2,3]
3075 Veterans Memorial Hwy.
Ronkonkoma 11779
(516) 737-0600

Hamilton Hallmark[1,2]
933 Motor Park Way
Hauppauge 11788
(516) 434-7470

Hamilton Hallmark[1,2]
1057 Henrietta Rd.
Rochester 14623
(716) 475-9130

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1117 Old Country Road
Suite 226
Plainview 11803
(516) 935-4785

Zeus Electronics[1,2]
100 Midland Ave.
Port Chester 10573
(914) 937-7400

North Carolina

Arrow/Schweber Electronics[1,2]
5240 Green Dairy Rd.
Raleigh 27604
(919) 876-3132

Hamilton Hallmark[1,2,3]
5234 Greens Dairy Rd.
Raleigh 27604
(919) 872-0712

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Ohio

Arrow/Schweber Electronics[1,2]
6573E Cochran Rd.
Solon 44139
(216) 248-3990

Arrow/Schweber Electronics[1,2]
8200 Washington Village Dr.
Centerville 45458
(513) 435-5563

Hamilton Hallmark[1,2,3]
5821 Harper Rd.
Solon 44139
(216) 498-1100

Hamilton Hallmark[1,2,3]
777 Dearborn Park Lane
Suite L
Worthington 43085
(614) 888-3313

Hamilton Hallmark[1,2]
7760 Washington Village Dr.
Dayton 45459
(513) 439-6735

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Oklahoma

Arrow/Schweber Electronics[1,2]
12111 E. 51st St.
Suite 101
Tulsa 74146
(918) 252-7537

Hamilton Hallmark[1,2,3]
5411 S. 125th East Ave.
Suite 305
Tulsa 74146
(918) 254-6110

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Oregon

Almac/Arrow Electronics[1,2]
1885 N.W. 169th Place
Beaverton 97006
(503) 629-8090

Hamilton Hallmark[1,2]
9750 S.W. Nimbus Ave.
Beaverton 97005
(503) 526-6200

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Pennsylvania

Arrow/Schweber Electronics[1,2]
2681 Mosside Blvd
Monroeville 15146
(412) 856-9490

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
40 Croce Lane
Coatesville 19320
(215) 383-9536

Texas

Arrow/Schweber Electronics[1,2]
11500 Metric Blvd
Suite 160
Austin 78758
(512) 835-4180

Arrow/Schweber Electronics[1,2]
3220 Commander Dr.
Carrollton 75006
(214) 380-6464

Arrow/Schweber Electronics[1,2]
10899 Kinghurst
Suite 100
Houston 77099
(713) 530-4700

Hamilton Hallmark[1,2,3]
(Corporate Office)
11333 Pagemill Rd.
Dallas 75243
(214) 343-5000

Hamilton Hallmark[1,2,3]
11420 Pagemill Rd.
Dallas 75243
(214) 553-4300

Hamilton Hallmark[1,2,3]
8000 West Glen
Houston 77063
(713) 781-6100

Hamilton Hallmark[1,2]
12211 Technology Blvd.
Austin 78727
(512) 258-8848

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
13740 Midway Rd.
Suite 601
Dallas 75244
(214) 701-9555

Zeus Electronics[1,2]
3220 Commander Dr.
Carrollton 75006
(214) 783-7010

Utah

Hamilton Hallmark[1,2]
1100 East 6600 South
Suite 120
Salt Lake City 84121
(801) 266-2022

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Sertek, Inc.[2,3]
800 334-7127

Washington

Almac/Arrow Electronics[1,2]
14360 S.E. Eastgate Way
Bellevue 98007-6458
(206) 643-9992

Hamilton Hallmark[1,2]
8630 154th Ave.
Redmond 98052
(206) 881-6697

Newark Electronics[1,2]
1-800-367-3573

Notes:
1. Optoelectronics
2. RF Diodes/Transistors
3. Microwave and Avantek Products

Penstock, Inc.[2,3]
10800 N.E. 8th St.
Suite 805
Bellevue 98004
(206) 454-2371

Penstock, Inc.[2,3]
1-800-PENSTOC

Wisconsin

Arrow/Schweber
Electronics[1,2]
200 North Patrick Blvd.
Brookfield 53045
(414) 792-0150

Hamilton Hallmark[1,2,3]
2440 South 179th St.
New Berlin 53146
(414) 797-7844

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

International

Australia

VSI Electronics (AUST) Pty. Ltd.[1,2,3]
16 Dickson Avenue
Artarmon, N.S.W. 2064
(61) 2 439 4655

Austria

BFI IBEXSA Elektronik GmbH[2,3]
Korbinianstr. 6
85386 Eching (München)
Tel: (49) 89 319 51 35

EBV[1,2]
Diefenbachgasse 35/6
1150 Vienna
Tel: (43) 1 894 1774

EURODIS Electronics[1,2]
Lamezanstrasse 10
1232 Vienna
Tel: (43) 1 61062 115

Belgium

BFI IBEXSA BV[2,3]
PO Box 3019
2130 KA Hoofddorp
Netherlands
Tel: (31) 20 65 31 350

EBV ELEKTRONIK[1,2]
Excelsiorlaan 35
Avenue Excelsior 35
1930 Zaventem
Tel: (32) 02 720 99 36

Brazil

Intertek Electronica Ltd.[1,2]
Rua Miguel Casagrande, 200
02714-000, Sao Paulo, SP
(011) 266-2922

Bulgaria

MACRO Sofia[1,2]
116 Geo Millev Str.
BL 57 AP70
1574 SOFIA
Tel/Fax:(359) 2 708140

Canada

Arrow
1093 Meyerside Dr.
Mississauga, Ontario
L5T 1M4
(416) 670-7769

Arrow
8544 Baxter Pl.
Burnaby, B.C.
V5A 4T4
(604) 421-2333

Arrow
1100 St. Regis
Dorval, Quebec
H9P 2T5
(514) 421-7411

Arrow
36 Antares Dr.
Unit 100
Nepean, Ontario
K7E 7W5
(613) 226-6903

Hamilton/Hallmark[1,2]
8610 Commerce Court
Burnaby, BC V5A 4N6
(604) 420-4101

Hamilton/Hallmark[1,2]
151 Superior Blvd.
Units 1-6
Mississauga,
Ontario L5T 2L1
(416) 564-6060

Hamilton/Hallmark[1,2]
190 Colonnade Road
Nepean, Ontario K7E 7J5
(613) 226-1700

Hamilton/Hallmark[1,2]
7575 Trans Canada Highway
Suite 600
Ville St. Laurent, Quebec
H4T 1V6
(514) 335-1000

Penstock Inc.
260 Hearst Way, #313
Kanata, Ontario K2L 3H1
(613) 592-6088

Czech Republic

GM Electronic[1,2,3]
Evropska 73
160-00 Praha 6
Tel: (42) 2 316 7202

MACRO Weil s.r.o.[1,2]
Bechynova 3
160-00 Praha 6
Tel: (42) 2 3112 182

Denmark

Avnet Nortec AS[1,2]
Transformervej 17
DK-2730 Herlev
Tel: +45 (42) 84 20 00

BFI-IBEXSA Denmark AS[2,3]
Langebjergsvenget 8A, 1.TH
DK-4000 Roskilde
Tel: +45 (46) 75 31 31

Finland

Arrow-Field Oy[1,2]
Niittyläntie 5
00620 Helsinki
Tel: 358-0-777571

Arrow-Field Oy
Ravi 18
EE0002 Tallinn
Estonia
Tel: 358-49-215172

Avnet Nortec Oy[1,2]
Itälahdenkatu 22
00210 Helsinki
Tel: 358-0-670277

BFI-IBEXSA Nordic AB[2,3]
Box 7093
(Kung Hans väg 12)
S-191 07 Sollentuna
Sweden
Tel: +46 (8) 626 99 00

France

Arrow Electronics[1,2]
73/79 rue des Solets
Silic 585
94668 Rungis Cedex
Tel: (1) 49 78 49 78

EBV Elektronik[1,2]
16, rue Gallilée
Cité Descartes
77436 Champs sur Marne
Tel: (1) 64 68 86 00

Elexience[2,3]
9, rue des Petits Ruisseaux
91370 Verriere le Buisson
Tel: (1) 60 11 94 71

RADIOSPARES Composants
Rue Norman King
BP 453
60031 Beauvais Cedex
Tel: (16) 44 84 72 72

Scie-Dimes Ibexsa SA[2,3]
1, rue Lavoisier ZI-BP 25
91430 Igny
Tel: (1) 69 33 74 00

S.C.A.I.B. S.A.[1,2]
80, rue d'Arcueil
Silic 137
94523 Rungis Cedex
Tel: (1) 46 87 23 13

Germany

BFI IBEXSA Elektronik GmbH[2,3]
Korbinianstrasse 6
85386 Eching
Tel: 089 / 3 19 51 35

EBV-Elektronik GmbH[1,2]
Hans-Pinsel-Strasse 4
85540 Haar b. München
Tel: 089 / 4 56 10-0

Farnell GmbH[1,2]
Grünwalderweg 30
82041 Deisenhofen
Tel: 089 / 6 13 39 11

Ing.-Büro K.-H. Dreyer[1,2]
Albert-Schweitzer-Ring 36
22045 Hamburg
Tel: 040 / 66 90 27-28

Jermyn GmbH[1,2]
Im Dachsstück 9
65549 Limburg
Tel: 06431 / 508-0

SASCO GmbH[1,2]
Hermann-Oberth-Str. 16
85640 Putzbrunn b. München
Tel: 089 / 46 11-0

Greece

Micronics Ltd.[1,2,3]
46, Kritis Street
16451 Argyroupolis
Athens
Tel: (30) 1 9914 786

Hong Kong

CET Ltd. (REP)[1,2,3]
22/F Chuang's Finance Centre
81-85, Lockhart Road
(852) 5200922

Semicon Products and Systems Co. Ltd.[3]
11/F Evernew House,
485 Lockhart Road
Causeway Bay
(852) 5729183

Hungary

EURODIS Electronics[1,2]
Lamezanstrasse 10
1232 Vienna
Tel: (43) 1 61062 115

MACRO Budapest Kft[1,2]
Etele ut 68
1115 Budapest
Tel:(36) 1 269 8110

India

Hinditron Services Pvt. Ltd.[2,3]
Industry House, 23-B
Mahal Industrial Estate
Mahakali Caves Road,
Andheri East,
Bombay 400093
(91) 22 8634035

Notes:
1. Optoelectronics
2. RF Diodes/Transistors
3. Microwave and Avantek Products

SKAG INDIA PVT. Ltd.[1]
22 Richmond Rd.
Bangalore 560025
(91) 80 224057/2240497

Israel

CMS[2,3]
Computation & Measurement Systems Ltd.
11, Hashlosha Street
P.O. Box 25089
67060 Tel-Aviv
(03) 538 03 18

Telsys Ltd.[1,2]
Atidim, Industrial Park, Bldg 3
Dvora Hanevia Street, Neva Sharet
61431 Tel-Aviv
(03) 49 20 01

Italy

BFI IBEXSA SPA[2,3]
Via Massena 18
20145 Milano
Tel: (02) 33 10 05 35

Dott. Ing.[1,2]
Giuseppe de Mico S.p.A.
V. le Vittorio Veneto 8
20060 Cassina de Pecchi
Tel: (02) 95 34 36 00

LASI Elettronica S.p.A.[1,2]
Viale Fulvio Test. 280
20126 Milano
Tel: (02) 66 10 1370

Silverstar Ltd.[1,2]
Viale Fulvio Testi 280
20126 Milano
Tel: (02) 66 12 51

Japan

Ryoden Trading Co., Limited[1,2,3]
3-15-15 , Higashi Ikebukuro,
Toshima-ku, Tokyo 170
(81) 3-5396-6206

Ryoden Trading Co., Limited[1,2,3]
Shin-Osaka Center Bldg.
4-1-4 Miyahara
Yodogawa-Ku
Osaka-shi, Osaka 532
(81) 6-399-3409

Ryoyo Electro Corporation[1,2,3]
Konwa Bldg.
1-12-22, Tsukiji
Chuo-ku, Tokyo 104
(81) 3-3546-5011

Ryoyo Electro Corporation[1,2,3]
Nisshin Shokuhin Bldg.
4-1-1, Nishi-Nakajima
Yodogawa-ku, Osaka 532
(81) 6-302-5371

Ryoyo Electro Corporation[1,2,3]
Nagoya AT Bldg.
1-18-22, Nishiki, Naka-ku,
Nagoya-shi, Aichi 460
(81) 52-203-0277

Tokyo Electron Limited[1,2,3]
Shinjuku Monolith Bldg.
2-3-1 Nishi Shinjuku
Shinjyuku-Ku, Tokyo 163
(81) 3-3340-8252

Tokyo Electron Limited[1,2,3]
Sumitomoseimei
Shin-Osaka-Kita Bldg.
4-1-14, Miyahara,
Yodogawa-ku,
Osaka-shi, Osaka 532
(81) 6-399-0261

Yamada Corporation[2,3]
Shin-Aoyama Bldg. East
1-1-1 Minami-Aoyama
Minato-Ku, Tokyo 107
(81) 3-3475-1121

Yamada Corporation[2,3]
Nagoya Kokusai-Center Bldg.
1-47-1, Nakono,
Nakamura-Ku
Nagoya-shi, Aichi 450
(81) 52-563-6661

Yamada Corporation[2,3]
Higobashi Shimizu Bldg.
1-3-7 Tosabori, Nishi-Ku
Osaka-shi, Osaka 550
(81) 6-449-1101

Korea

Panwest Co. (REP)[1,2]
Songnam Building
Room 213
Seocho-dong-Seocho-ku
1358-6 Seoul
(82) 2-5547176

SANGSOO Electronics Co.[2,3]
Suite 303 Kyungho Building
25-2 Yeo euido-Dong
Youngdeungpo-ku, Seoul
(82) 2-7805360

Malaysia

DCP (M) SDN BHD[1,2]
6th Floor Wisma Denko
41 Aboo Sittee Lane
10400 Penang
(604) 281860

Netherlands

EBV ELEKTRONIK[1,2]
Planetenbaan 2
3606 AK Maarssenbroek
Tel: (31) 03465 623 53

Diode Components[1,2]
Coltbaan 17
3439 NG Nieuwegein
Tel: (31) 03402 912 34

BFI IBEXSA BV[2,3]
PO Box 3019
2130 KA Hoofddorp
Tel: (31) 020 65 31 350

New Zealand

VSI Electronics (NZ) Ltd.[1,2,3]
7 Beasley Ave.
Penrose
Auckland
(64) 9 579 6603

VSI Electronics (NZ) Ltd.[1,2]
295 Cashel Street
Christchurch
(64) 3 660-928

VSI Electronics (NZ) Ltd.[1,2]
Flanders Arcade
71 High Street
Lower Hutt
(64) 4 694-560

Norway

Avnet Nortec AS[1,2]
P.O. Box 123
(Smedsvingen 4B)
N-1364 Hvalstad
Tel: +47 (66) 84 62 10

Farnell Electronic Services[1,2]
Nedre Kaldbakkvei 88
N-1081 Oslo 10
Tel: +47 (22) 32 12 70

BFI-IBEXSA Nordic AB[2,3]
Box 7093
(Kung Hans väg 12)
S-191 07 Sollentuna
Sweden
Tel: +46 (8) 626 99 00

Poland

Macropol Co. Ltd.
02-366 Warszawa
Ul. Bitwy Warszawskej 11
Tel: (48) 22 224 337

Meditronik[1,2,3]
4, Dzika Street
00-194 Warsaw
Tel: (48) 2 635 2263

Portugal

Corsisa Electronica LIMITADA[1,2]
C/ Estrada Nacional 107, No. 743
Ardegas, Aguasantos
Tel: (351) 2 973 69 57

ATD - ARROW[1,2,3]
Quinta Grande, Lote 20 r/c DTO. Alfragide
2700 Amadora, LISBOA
Tel: (351) 1 47 14 182

Russia

Arrow-Field DESAGENT SPp
2. Bodepa Square
196143 St. Petersburg
Tel: see directory

NEKLUSOVA[1,2]
ul Zamshina 15
St. Petersburg
Tel: (7) 812 545 0723

OPTONIKA[1,2,3]
PO Box 69
109542 Moscow
Tel: (7) 095 305 7738

RADIS/MTUCI[2,3]
Aviamotornaya 8a
105855 MOSCOW
Tel: (7) 095 273 8879

Singapore

Dynamar Computer Products[1,2]
PTE Ltd. (REP)
109 Defu Lane 10
Off Hougang Avenue 3
Singapore 1953
(65) 2813388

Hi-Tech Business Associate[2,3]
230, Upper Bukit Timah Road
Bukit Timah Industrial Complex #04-10
Singapore 2158
(65) 4620668

Slovak Republic

MACRO Components s.r.o.[1,2]
Vysokoskolakov 6
010-01 Zilina
Tel: (42) 89 45041/34181

Notes:
1. Optoelectronics
2. RF Diodes/Transistors
3. Microwave and Avantek Products

Slovenia
EBV[1,2]
Diefenbachgasse 35/6
1150 Vienna
Austria
Tel: (43) 1 894 1774

IR Electronic[1,2]
Ziherlova ulica 2
Ljubjana
Tel: (386) 61 222 007

So. Africa
Advanced Semiconductor Devices (PTY) Ltd.[1,2,3]
P.O. Box 3853
SA-2128 Rivonia
Tel: (27) 011 444 23 33

Spain
BFI IBEXSA[3]
Isabel Colbrand S/N
Edificio alpha III Nave 85
Poligono Industrial
Fuencarral
28049 MADRID
Tel: (34) 1 358 8516

Diode[1,2]
C/ Orense 34
28020 Madrid
Tel:(34) 1 555 3686

Sociedad De Electronica Y Componentes SA
Selco[1,2]
Paseo De La Habana 190
28036 Madrid

Sweden
Avnet Nortec AB[1,2]
Box 1830
(Englundavägen 7)
S-171 27 Solna
Tel: +46 (8) 629 14 00

BFI-IBEXSA Nordic AB[2,3]
Box 7093
(Kung Hans väg 12)
S-191 07 Sollentuna
Tel: +46 (8) 626 99 00
Farnell Electronic Services[1,2]
Box 1330
(Ankdammsgatan 32)
S-171 26 Solna
Tel: +46 (8) 83 00 20

Switzerland
Basix AG[1,2]
Hardturmstr. 181
Postfach
8010 Zürich
Tel: (41) 01 276 11 11

BFI IBEXSA Elektronik GmbH[2,3]
Korbinianstr. 6
85386 Eching (München)
Tel: (49) 89 319 51 35

EBV Elektronik AG[1,2]
Vorstadtstrasse 37
8958 Dietikon
Tel: (41) 01 740 1090

Taiwan (Republic of China)
Morrihan International Inc.[1,2]
No. 57, 8th Floor
Yang Shen Shan Yet Building
337 Fu Hsing North Road
Taipei, Taiwan
(886) 2 7522200

Thailand
Dynamar Computer Products[1,2]
2991/19 Visuthanee,
1st Floor
Ladprao Road SOI 101-103
Klongchan, Bangkapi
Bangkok 10220
(66) 2-3760132

Turkey
EMPA AS[1,2,3]
Elektronik Mamulleri
Pazarlama A.S.
Florya Is Merkezi
Besyol Londra Asfalti
34630 SEFAKOY - ISTANBUL
Tel: (90) 212 599 30 50

United Kingdom
Avnet Access Ltd.[1,2]
Jubilee House
Jubilee Road
Letchworth
Herts SG6 1QH
Tel: (44) 0462 48 08 88

BFI IBEXSA Electronics Ltd.[2,3]
Burnt Ash Road
Quarry Wood Industrial Estate
Aylesford
Kent
ME20 7NA
Tel: (44) 0622 88 24 67

Farnell Celdis[1,2]
300 Kings Road,
Reading
Berkshire RG1 4GA
Tel: (44) 0734 66 66 76

Farnell Electronic Services[1,2]
Edinburg Way
Harlow,
Essex CM20 2DF
Tel: (44) 0279 44 11 44

Farnell Electronic Components[1,2]
Canal Road
Leeds
West Yorkshire LS12 2TU
Tel: (44) 0532 63 63 11

Jermyn Distribution[1,2]
Vestry Estate
Sevenoaks,
Kent TN14 5EU
Tel: (44) 0732 74 01 00

Notes:
1. Optoelectronics
2. RF Diodes/Transistors
3. Microwave and Avantek Products

HEWLETT PACKARD

HP Components US Sales & Support

Alabama
620 Discovery Dr.
Huntsville 35806
Tel: 205-971-2000

Arizona
8080 Pointe Parkway West
Phoenix 85044
Tel: 800-235-0312

3400 E. Britannia Dr.
Bldg. C, Suite 124
Tucson 85706
Tel: 800-235-0312

California
1421 S. Manhattan Ave.
Fullerton 92631
Tel: 800-235-0312

5245 Pacific Concourse Dr.
Suite 100
Los Angeles 90045
Tel: 800-235-0312

351 E. Evelyn Ave.
Mountain View 94041
Tel: 800-235-0312

3831 N. Freeway Blvd.
Bldg. C, Suite 100
Sacramento 95834
Tel: 916-567-8500

9606 Aero Dr.
San Diego 92123
Tel: 800-235-0312

5805 Sepulveda Blvd.
Suite 800
Van Nuys 91411
Tel: 800-235-0312

Colorado
24 Inverness Place East
Englewood 80112
Tel: 800-235-0312

Connecticut
115 Glastonbury Blvd.
Glastonbury 06033
Tel: 203-633-8100

One Stamford Plaza
9th Floor
Stamford 06901
Tel: 203-324-1003

Florida
5900 N. Andrews Ave.
Suite 100
Ft. Lauderdale 33309
Tel: 305-938-9800

6177 Lake Ellenor Dr.
Orlando 32809
Tel: 407-859-2900

5550 W. Idlewild Ave.,
Suite 150
Tampa 33634
Tel: 813-884-3282

Georgia
1995 North Park Place
Atlanta 30339
Tel: 404-955-1500

Illinois
5201 Tollview Dr.
Rolling Meadows 60008
Tel: 708-342-2000

Indiana
201 W. 103rd St.
Suite 100
Indianapolis, IN 46290
Tel: 317-844-4100

Maryland
3701 Koppers St.
Baltimore 21227
Tel: 410-362-7572

Massachusetts
29 Burlington Mall Rd.
Burlington 01803
Tel: 617-270-7000

Michigan
39550 Orchard Hill Place
Novi 48376
Tel: 313-380-2100

Minnesota
2025 W. Larpenteur Avenue
St. Paul 55113
Tel: 612-644-1100

Missouri
6601 Winchester Ave.
Kansas City 64133
Tel: 816-737-0071

New Jersey
W. 120 Century Rd.
Paramus 07653
Tel: 201-599-5000

New York
290 Woodcliff Dr.
Fairport 14450
Tel: 716-264-4000

7 Old Sod Farm Rd.
Melville 11747
Tel: 516-753-0555

North Carolina
2000 Regency Pkwy.
Suite 600
Cary, NC 27511
Tel: 919-467-6600

Ohio
7887 Washington Village Dr.
Dayton 45459
Tel: 513-433-2223

15885 Sprague Rd.
Strongsville 44136
Tel: 216-243-7300

Oregon
15115 SW Sequoia Parkway, Suite 100
Portland 97224
Tel: 800-235-0312

Pennsylvania
2750 Monroe Blvd.
Valley Forge 19482
Tel: 215-666-2434

Texas
930 E. Campbell Rd.
Richardson 75081
Tel: 214-231-6101

Utah
3530 West 2100 South
Salt Lake 84119
Tel: 800-235-0312

Washington
15815 SE 37th St.
Bellevue 98006
Tel: 800-235-0312

HEWLETT PACKARD

International Sales & Support

Austria and Eastern Region
Hewlett-Packard
Lieblgasse 1
P.O. Box 72
A-1222 Vienna
Tel: (43) 1 2500 461

Belgium/Luxemburg
Hewlett-Packard Nederland B.V.
Boschdijk 137
PO Box 2342
5600 CH Eindhoven
Netherlands
Tel: (31) 40 / 32 42 18

Brazil
Edisa Hewlett-Packard S.A.
Alameda Rio Negro 750
06454 - Alphaville - Barueri - SP
Brazil
Tel: (+55 11) 725-1444

Canada
5150 Spectrum Way
Mississauga, Ontario
Canada L4W 5G1
Tel: 416-206-4725

China
Hewlett-Packard Co., Ltd.
5-6/F West Wing Office
China World Trade Center
No. 1 Jian Guo Men Wai Ave.
Beijing, 100004, PRC
Tel: 86-1-505-3888

Finland
Hewlett-Packard Oy
Piispankalliontie 17
SF-02200 Espoo
Tel: 358/0/8 87 21

France
Hewlett-Packard
Z.A. de Courtaboeuf
1, Avenue du Canada
F-91947 Les Ulis Cedex
Tel: 33/1/69 82 60 60

Germany
Hewlett-Packard GmbH
Unternehmensbereich
Elektronische Bauelemente
Hewlett-Packard-Str. 1
61352 Bad Homburg
Tel: (49) 6172 - 16-0

Greece/Turkey
Hewlett-Packard S.A.
P.O.Box
150 Route du Nant-d'Avril
CH-1217 Meyrin 2
Tel: 41/22/780 81 11

Israel
Computation & Measurement
Systems Ltd.
11 Hashlosha Street
P.O.Box 25089
IL-Tel Aviv 67060
Tel: 972/3/538 03 18

Italy
Hewlett-Packard Italiana S.p.A.
Via G. Di Vittorio 9
I-20063 Cernusco S/N (MI)
Tel: 39/2/92 121

Japan
Yokogawa Hewlett-Packard
29-21 Takaido-Higashi 3 Chome
Sugimani-Ku, Tokyo 168
Japan
Tel: 81-3-3331-8153

Korea
Samsung Hewlett-Packard
Samsung Life Bldg.
36-1 Yeoeui Do-Dong
Youngdeungpo-Ku
Seoul, 150-010, Korea
Tel: 82-2-769-0114

Mexico
Hewlett-Packard de México
S.A. de C.V.
Monte Pelvoux No. 111
Fracc. Lomas de Virreyes
11000 Mexico D.F.
Mexico
(+52 5) 326-4000

Netherlands
Hewlett-Packard Nederland B.V.
Boschdijk 137
PO Box 2342
5600 CH Eindhoven
Netherlands
Tel: (31) 40 / 32 42 18

Singapore
Hewlett-Packard Singapore
150 Beach Rd. #29-00
Gateway West Singapore 0718
Tel: 65-291-9088

Spain/Portugal
Hewlett-Packard Espanola S.A.
Corta de la Coruna km 16 500
Madrid
E-28230 Las Rozas
Tel: 34/1/626 16 00

Sweden, Denmark, Norway
Hewlett-Packard AB
Skalholtsgatan 9, Kista
Box 19
S-164 93 Kista
Tel: 46/8/7 50 20 00

Switzerland/South Africa
Hewlett-Packard (Schweiz) AG
In der Luberzen 29
CH-8902 Urdorf/Zürich
Tel: (41) 01 735 71 11

Taiwan
Hewlett-Packard Taiwan Ltd.
20, Kao Shuang Rd, Ping Chen
Tao-Yuan, Taiwan, R.O.C.
Tel: 886-3-492-9666

United/Kingdom/Ireland
Hewlett-Packard Ltd.
Amen Corner
Cain Road
Bracknell
UK-Berkshire RG12 1HN
Tel: 44/344/ 36 00 00

HEWLETT PACKARD

5091-4573E (6/93)