IBM

DRAM Module Databook

1995

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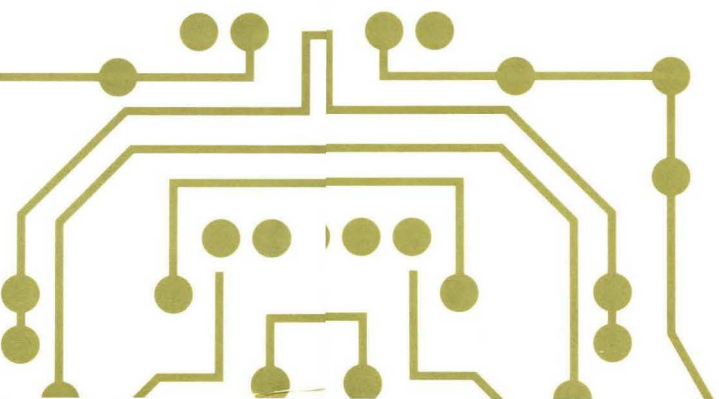

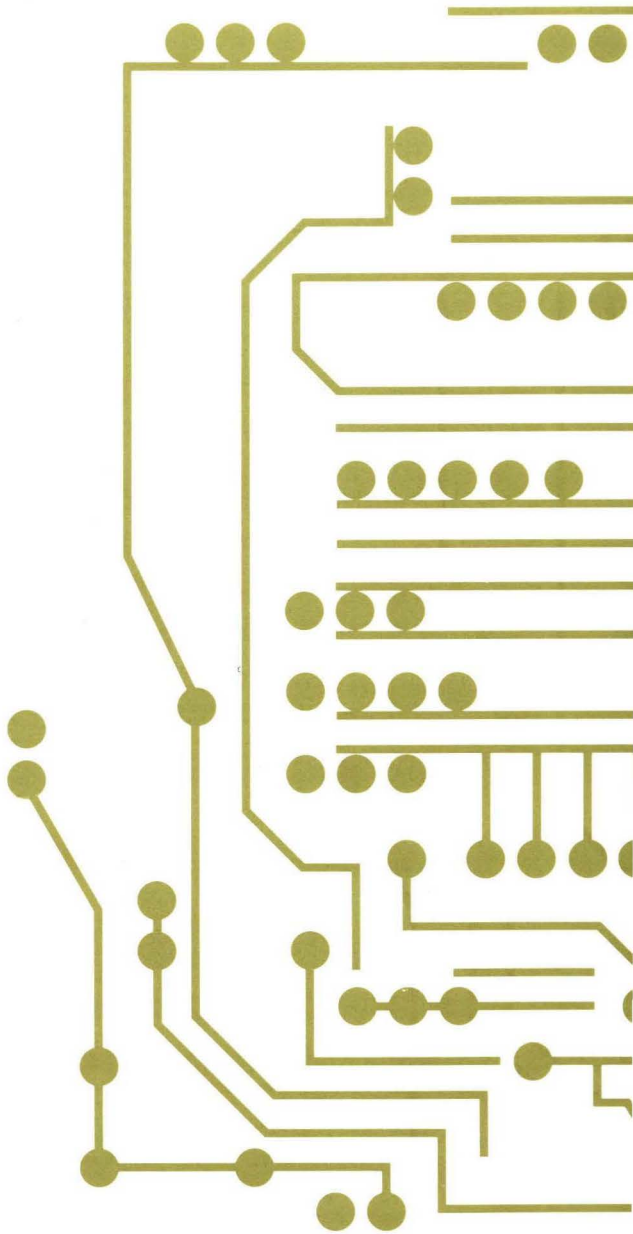

IBM

Welcome to the new Memory Databook from the IBM Microelectronics Division. Represented in this edition is a vast array of leading-edge memory products backed by the world's largest producer of integrated circuit solutions with the most extensive support network in the industry.

The IBM Microelectronics Division is a world-wide enterprise with development and manufacturing facilities in Essex Junction,VT; Essonnes, France; Sindelfingen, Germany; and Yasu, Japan. IBM semiconductor products provide world-class technology from a global company that has delivered advanced design, process, and packaging technology for over thirty years. The Essex Junction site is the largest CMOS development and manufacturing facility where 6000 employees work in 3.5 million square feet of space in over 20 buildings on a 728-acre site to develop, manufacture, and support innovative product solutions that include the industry-standard 4-Mbit DRAMs, leading-edge 0.5-micron 16-Mbit DRAMs, and an extensive family of SIMMs, 8-Byte DIMMs, Small Outline DIMMs (SO DIMMs), and IC DRAMs...all meeting the stringent ISO 9000 quality standard.

Nearly four decades of experience has resulted in a impressive string of product "firsts" (from the world's first 16-bit bipolar integrated memory chip used in IBM System/360 systems in the sixties, to today's breakthrough 64-million-bit DRAMs built upon our innovative 0.35-micron CMOS VI technology), that assure unrivaled product reliability, superiority, and lasting value. A key customer benefit is direct access to our world-class silicon, packaging, and manufacturing technologies.

Our world wide presence provides extensive product support for all memory products through application centers, system specialists, and on-site experts.

Thank you for your interest in IBM Microelectronics Division memory products. We have provided you a postage paid comment card which can be found at the end of this manual. We value your suggestions and comments.

DRAM Module Databook

IBM

Printed in Canada
November 1994

Features: Addressing; Power Supply; Special Features (LC = Low Current, SR = Self Refresh, Au = Gold Tabs, SnPb = Tin Lead Tabs)

Organization: Organization, Special Features (QC = Quad CAS, E = ECC Optimized, EOS = ECC-On-SIMM)

168 Pin DIMMs - ECC 647

72 Pin SO DIMMs 869

IC DRAM Cards 1047

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Alphanumeric Index

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IBM11J1320BN	88 Pin IC DRAM Card	1M x 32	10/10, 3.3V	1065
IBM11J1360BL	88 Pin IC DRAM Card	1M x 36	10/10, 5.0V	1257
IBM11J2320BL	88 Pin IC DRAM Card	2M x 32	10/10, 5.0V	1081
IBM11J2320BN	88 Pin IC DRAM Card	2M x 32	10/10, 3.3V	1097
IBM11J2320HL	88 Pin IC DRAM Card	2M x 32	11/10, 5.0V	1113
IBM11J2320HN	88 Pin IC DRAM Card	2M x 32	11/10, 3.3V	1129
IBM11J2360BL	88 Pin IC DRAM Card	2M x 36	10/10, 5.0V	1273
IBM11J4320BL	88 Pin IC DRAM Card	4M x 32	11/11, 5.0V	1177
IBM11J4320CL	88 Pin IC DRAM Card	4M x 32	12/10, 5.0V	1193
IBM11J4320CN	88 Pin IC DRAM Card	4M x 32	12/10, 3.3V	1209
IBM11J4320HL	88 Pin IC DRAM Card	4M x 32	11/10, 5.0V	1145
IBM11J4320HN	88 Pin IC DRAM Card	4M x 32	11/10, 3.3V	1161
IBM11J4360BL	88 Pin IC DRAM Card	4M x 36	11/11, 5.0V	1289
IBM11J4360DL	88 Pin IC DRAM Card	4M x 36	12/11, 5.0V	1305
IBM11J8320CL	88 Pin IC DRAM Card	8M x 32	12/10, 5.0V	1225
IBM11J8320CN	88 Pin IC DRAM Card	8M x 32	12/10, 3.3V	1241
IBM11J8360BL	88 Pin IC DRAM Card	8M x 36	11/11, 5.0V	1321
IBM11J8360DL	88 Pin IC DRAM Card	8M x 36	12/11, 5.0V	1337
IBM11M1640BA	168 Pin 8 Byte DIMM	1M x 64	10/10, 5.0V, Au	519
IBM11M16730CB	168 Pin 8 Byte DIMM	16M x 72 E	13/11, 3.3V, Au	847
IBM11M1720BA	168 Pin 8 Byte DIMM	1M x 72	10/10, 5.0V, Au	585
IBM11M1730BA	168 Pin 8 Byte DIMM	1M x 72 E	10/10, 5.0V, Au	649
IBM11M1730BB	168 Pin 8 Byte DIMM	1M x 72 E	10/10, 3.3V, Au	671
IBM11M2640H	168 Pin 8 Byte DIMM	2M x 64	11/10, 5.0V, Au	541
IBM11M2720L	168 Pin 8 Byte DIMM	2M x 72	10/10, 5.0V, Au	607

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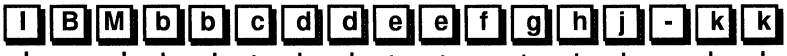
General Information

Part Numbering



Company Identification

Product Family / Quality Designator

Premium DRAM 11

Standard DRAM B1

Assembly Memory Depth
1 or 2 digits

25	256K depth
51	512K depth
1	1M depth
2	2M depth
4	4M depth
8	8M depth
16	16M depth
32	32M depth
64	64M depth
13	128M depth
26	256M depth
52	512M depth

Product Revision

Speed of Part

10	100ns (±10% V_{CC})
80	80ns (±10% V_{CC})
70	70ns (±10% V_{CC})
60	60ns (±10% V_{CC})
50	50ns (±10% V_{CC})
40	40ns (±10% V_{CC})

Product Identifier

A	30 Pin SIMM/ Sn/Pb Tab pins
B	30 Pin SIMM/ Au Tab pins
C	30 Pin SIMM/ pinned
D	72 Pin SIMM/ Sn/Pb Tab pins
E	72 Pin SIMM/ Au Tab pins
F	72 Pin SIMM/ pinned
J	88 Pin DRAM Card (Buffered inputs)
L	88 Pin Reserved
M	168 Pin DIMM/ Au Tab Pins
S	72 Pin SO DIMM/Au Tab Pins

Functions Supported:

0	Fast Page Mode
1	Nibble Mode
2	Static Column Mode
5	Hyper Page Mode

Power / Refresh Sort: 1 Digit or Blank

Blank	Standard Power, 5V, No Self Refresh
A	Standard Power, 5V, Self Refresh
B	Standard Power, 3.3V, No Self Refresh
C	Standard Power, 3.3V, Self Refresh
L	Low Power, 5V, No Self Refresh
M	Low Power, 5V, Self Refresh
N	Low Power, 3.3V, No Self Refresh
P	Low Power, 3.3V, Self Refresh
S	Super Low Power, 5V, No Self Refresh
T	Super Low Power, 5V, Self Refresh
U	Super Low Power, 3.3V No Self Refresh
V	Super Low Power, 3.3V, Self Refresh
Z	Per Datasheet

Assembly Memory Width

08	x 8
09	x 9
16	x 16
18	x 18
32	x 32
33	x 33
36	x 36 (Parity)
37	x 36 (ECC applications)
38	x 36 (Custom)
40	x 40 (ECC applications)
48	x 36 (ECC-on-board, 12/8 code)
49	x 36 (ECC-On-board,Error reporting)
64	x 64 (TBD applications)
72	x 72 (Parity applications)
73	x 72 (ECC applications)
80	x 80 (ECC applications)

DRAM Type (Organization of DRAMs used on assembly)

A	x1 DRAMs used on the assembly
B	x4 DRAMs, x1 for parity (if applicable), square addressing (i.e. 11/11)
C	x4 DRAMs, x1 for parity (if applicable), # Row Addr = # Column Addr + 2
D	x4 DRAMs, x1 for parity (if applicable), Mixed Addressing (i.e. 12/11)
E	x4 DRAMs, x4/4 CE for parity, square addressing (i.e. 11/11)
F	x4 DRAMs, x4/4 CE for parity,# Row Addr = # Column Addr + 2
G	x4 DRAMs, x4/4 CE for parity, Mixed Addressing (i.e. 12/11)
H	x8 or 9 DRAMs, # Row Addr = # Column Addr + 1 (i.e. 11/10)
J	x8 or 9 DRAMs, # Row Addr = # Column Addr + 3 (i.e. 12/9)
K	x8 or 9 DRAMs, # Row Addr = # Column Addr + 5 (i.e. 13/7)
L	x16 or x18 DRAMs, # Row Addr = # Column Addr (i.e. 10/10)
M	x16 or x18 DRAMs, # Row Addr = # Column Addr + 2 (i.e. 11/9)
N	x16 or x18 DRAMs, # Row Addr = # Column Addr + 4 (i.e. 12/8)
P	Non-standard DRAMs used on the assembly (per Datasheet)

Quality & Reliability

Introduction

Superior integrated circuit device reliability is attained when it is an integral part of process development, design and manufacturing. This section describes the methodology used by the IBM Microelectronics Division to achieve robust DRAM designs prior to market introduction, and the processes employed to ensure products of utmost quality and reliability during volume production.

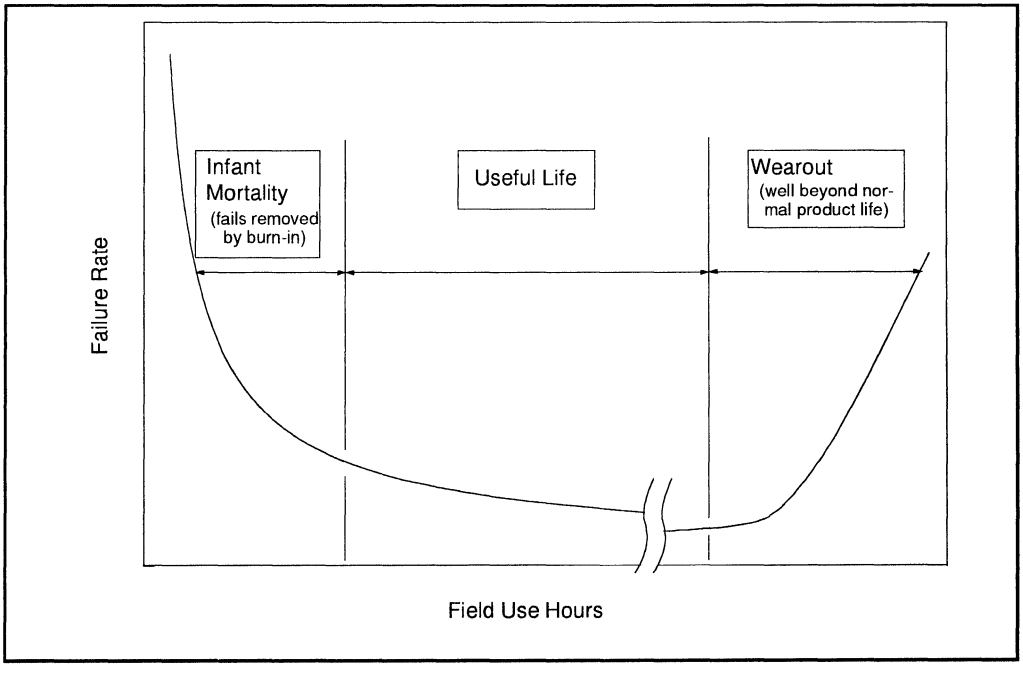
Reliability Goal

Our goal is to achieve failure rates during product life which are consistently below customer requirements. A time distribution of reliability failures is described by the "bathtub" curve depicted in Figure 1. The curve is divided into three segments: an infant mortality period marked by a rapidly decreasing failure rate; a stable, useful life period where the failure rate continues to decrease, and a period of increasing failure rate representing the onset of product wear-out. Infant mortality and useful life failures are caused by defects introduced during the manufacturing process; most of these defects are eliminated via high-efficiency reliability screens. Wear-out failures are avoided through careful technology development and product design, and by the use of effective process monitors during production.

Reliability Management System

Reliability fails are a combination of three problem types: wear-out mechanisms which shorten useful life, systematic defects caused by process variation beyond acceptable limits, and random defects created by process deficiencies. IBM Microelectronics' comprehensive development and manufacturing strategy emphasizes reliability in our designs and processes to manage all three problem types. Early design and qualification activities eliminate wear-out failure mechanisms (e.g., hot carriers and electromi-

Figure 1. Bathtub Curve

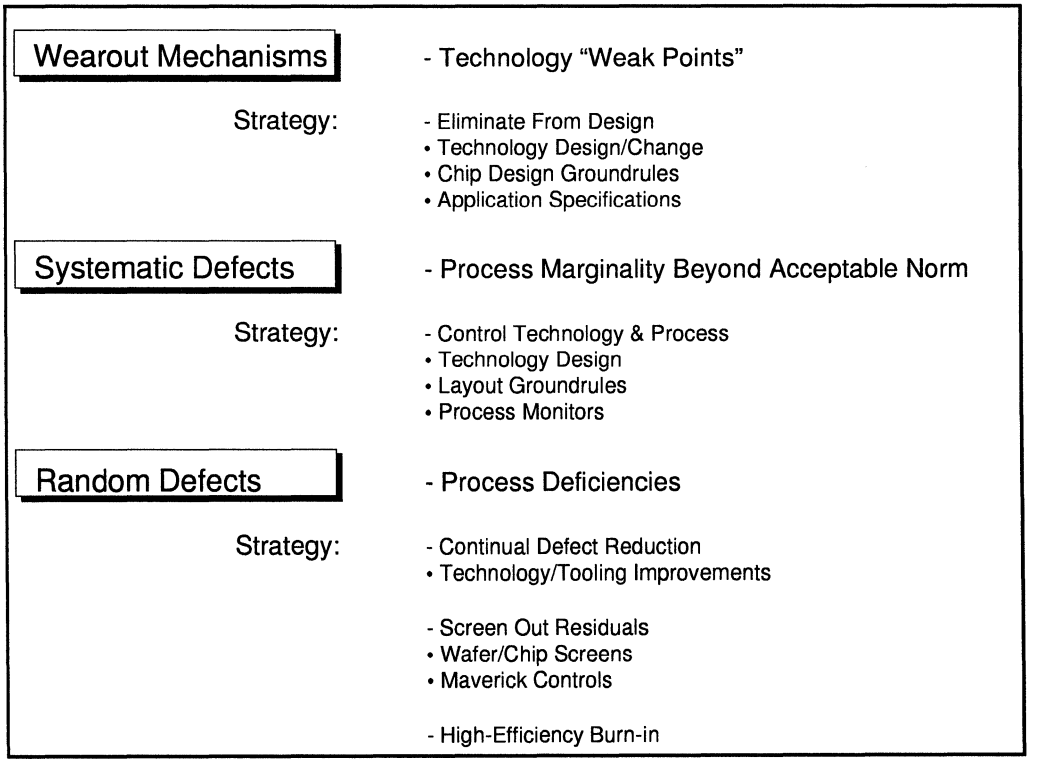


gration) during normal product life, and establish technology and process limits which minimize design sensitivity to manufacturing defects. Process control and tooling improvements, combined with high-efficiency burn-in and maverick screens, provide continuous defect reduction. Attributes of the reliability management system are summarized in Figure 2.

Qualification Process

An overview of the qualification cycle, from technology inception to full production, is given in Figure 3 on page 25. Reliability management begins with the start of a new technology, when design models are developed and used to evaluate new features, and reliability test structures are defined. Mechanism-specific accelerated tests are then performed to assess wear-out mechanisms, including hot carriers, dielectric integrity, ionics and temperature stability, mechanical stability, stress induced metal voiding, and electromigration. The qualification process establishes the control of wear-out mechanisms to well beyond intended product life. Stress results are utilized to define chip and technology design groundrules (e.g., hot carriers and electromigration), application specification limits, and process controls to avoid wear-out. Wafer screen and burn-in design requirements are verified. Upon successful completion of the technology qualification phase, early production devices are subjected to a full series of chip and assembly tests and stresses. These include functionality tests to define test margins for outgoing quality, functional stresses to measure product reliability, and temperature-humidity and thermal cycle stresses to assess package integrity. A summary of product

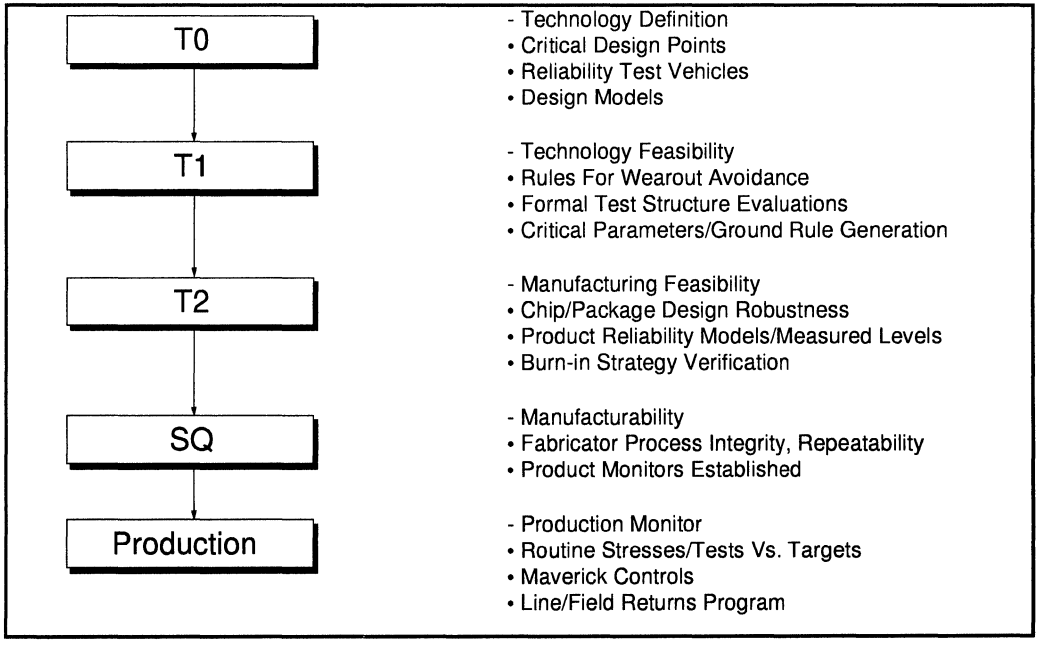
Figure 2. Reliability Management System



qualification tests and stresses is provided in Table , "DRAM Product Qualification Tests," on page 26. Failures experienced during these stresses receive complete electrical and physical failure analysis. Root cause failure information is fed back to process and design engineering with the goal of eliminating all failure mechanisms. With every new DRAM technology, product functional stresses are conducted at a minimum of three voltage and temperature conditions to develop voltage and temperature acceleration models. These models are then used to predict product reliability performance compared to program objectives. Acceleration model development is summarized in Figure 4 on page 27.

Before a product design is introduced into full scale production, it undergoes an exhaustive functional test evaluation as a key element of the overall qualification process. The objective of this evaluation is to confirm that the product exhibits adequate performance margins over the application specification limits. Issues must be resolved prior to the exit of the qualification cycle. Resolution may include a redesign, process fix, or the addition of a manufacturing test which ensures outgoing product will have sufficient margin.

Figure 3. Qualification Cycle



DRAM Product Qualification Tests

Accelerated Stress/Test		Sample Type (Table 1)	When Required (Table 2)
In-line Process Data	Wafer Test Structures	U,F	2,3
	Packaging Assembly Structures	U,F	4,5
Construction Analysis		FTM	2 - 5
Group "B" Mechanical Tests	Salt Atmosphere	FTM	4,5
	Flammability	FTM	4,5
	Marking Permanence	FTM	4,5
	Solderability	FTM	4,5
	Solvent Resistance	FTM	4,5
	Vibration	FBTM	4,5
	Solder Dip	FBTM	4,5
	Thermal Shock	FBTM	4,5
	Impact Shock	FBTM	4,5
	Bubble Leak	FTM	4,5
	Helium Leak	FTM	4,5
Kinetics HTB Evaluation		FTM	1,2,3,6
Functionality Tests	Module Level	FBTM	1-5
	Card/System Level	FBTM	1,4
Latchup Tests		FBTM	2,3
ESD Tests		FBTM	2,3
Preconditioning		FBTM	2-5
Extended Stresses	High Temperature Operating Life	FBTM	2,3
	Low Temperature Operating Life	FBTM	2,3
	Thermal Cycle	FBTM	2-5
	THB, HAST	FBTM	2-5
	Pressure Cooker Test	FBTM	2-5
	Low Temperature Storage	FBTM	4,5
	High Temperature Storage	FBTM	2-5
Soft Error Rate Tests		FBTM	1,2,3,4,6

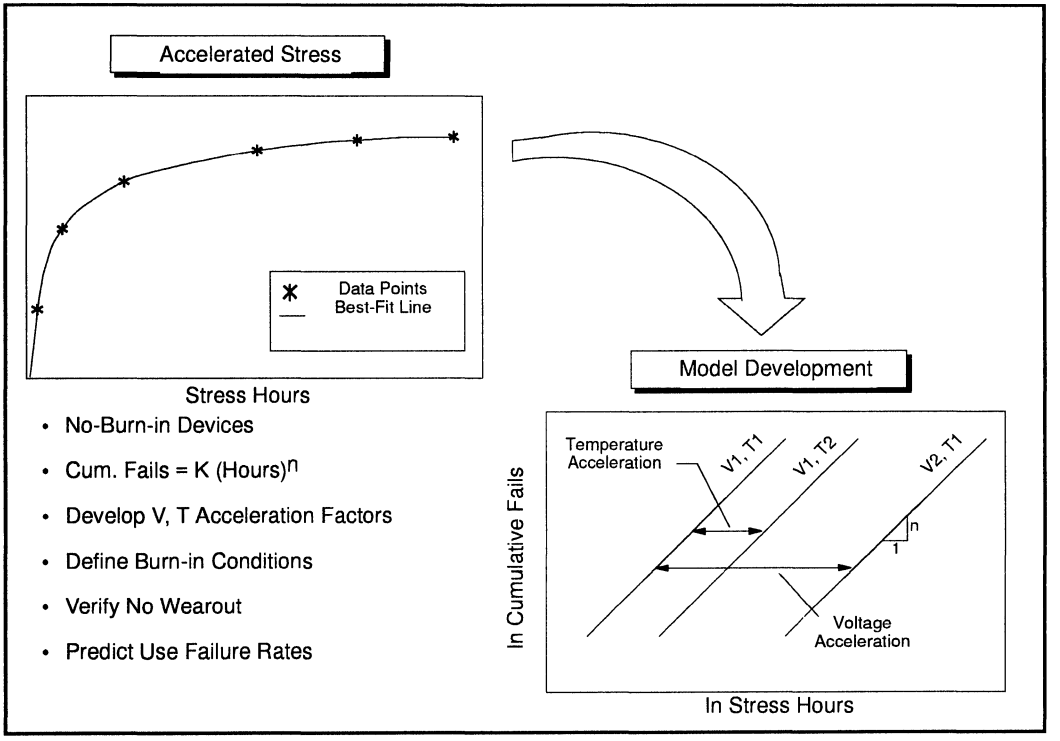
Table 1

Designation	Sample Description
U	Unfinished or Subassembly Stage
F	Finished Unit (Wafer or Device)
FTM	Finished, Tested and Marked (No Burn-in)
FBTM	Finished, Burned-in, Tested and Marked

Table 2

Designation	When Required
1	New Die Design or New Product
2	New Wafer Fabrication Technology
3	Major Change to Wafer Fabrication Process
4	New Package Type or Assembly Technology
5	Major Change to Chip Size, Leadframe Design, Packaging Materials or Assembly Process

Figure 4. Acceleration Model Development



Failure Rate Calculations

Product reliability data is typically composed of several different failure mechanisms which may contribute failures differently as a function of voltage and temperature. When projecting reliability performance at actual use conditions from accelerated test data, the contribution of individual mechanisms with unique voltage and temperature kinetics behavior must be acknowledged. This is particularly important when the accelerated stress failure mix includes mechanisms with relatively low acceleration, where it can be expected that these will contribute a disproportionate number of fails at lower use conditions. In the absence of such fails, it is common practice to use voltage and temperature acceleration factors which combine all mechanisms into a composite model. Temperature acceleration for semiconductor failure mechanisms is usually determined from the Arhennius equation:

$$AF_T = \exp[E_a/k \times (1/T_u - 1/T_s)]$$

where: k is Boltzmann's constant ($8.617e^{-5}$)

T_u and T_s are use and stress temperatures, expressed in °K

E_a is the activation energy in ev. The composite value for 4M DRAM derived from our product qualifications is 0.65ev.

From modeling evaluations conducted during our product qualifications, voltage acceleration is described by:

$$AF_V = \exp(\beta \times (V_s - V_u))$$

where: V_s and V_u are stress and use voltages, expressed in volts.

β is the voltage acceleration term (1/V). The composite value for β from our 4M DRAM qualifications is 3.5.

Failure rates at use conditions can be calculated from accelerated stress data by converting the data to equivalent use hours with the voltage and temperature acceleration factors previously described. An example of a failure rate calculation for 4M DRAM is shown in the example below.

Failure Rate Calculation Example

Inputs/Assumptions

- 1000 devices through functional stress (HTOL)
- HTOL = 5.1 Volts, 125°C, 1000 Hours, producing 2 fails
- Operating conditions = 3.6 Volts, 85°C
- E_a = 0.65ev. and $\beta = 3.5V^{-1}$
- Chi-Squared distribution with 90% confidence interval

Failure Rate Calculation

The relationship between failure rate and the Chi-Squared distribution, expressed in fits, is as follows:

$$\lambda = \chi^2 / (2 \times t) = (\chi^2 \times 10^9) / (2 \times D.H.)$$

Where: λ = Failure Rate
t = Time (Hours)
D.H = Device-hours representing equivalent Use-Hours
χ^2 = The Chi-Squared distribution for a given confidence interval = X^2 (α, d.f.), where:

α = The CHI-Squared confidence interval
d.f. = Degrees of freedom = (2r + 2), where:
r = Number of observed HTOL failures

- Device-Hours from HTOL stress are sample size multiplied by stress time and voltage & temperature acceleration factors:

  D.H. = (1000 x 1000 x 190.6 x 8.3) = 1.58 * 10^9 Device-Hours

- From Chi-Squared distribution tables, the χ^2 Value for 2 fails at 90% confidence is 10.645. Thus, the failure rate is:

$$\lambda = (10.645 \times 10^9) / (2 \times 1.58 \times 10^9) = 3.4FIT$$

Production Test Strategy

A key design feature of our DRAM product set is the ability to invoke 'test modes' which provide an efficient and cost effective means of testing at both wafer and packaged device level. This feature affords reduced test times over conventional test methods while actually providing improved test coverage, guaranteeing superior product quality. Module level testing is performed at both elevated and sub-ambient temperatures to meet customer needs over the entire temperature operating range. The test programs are designed to guarantee that shipped product meets the application specifications for input levels, A.C. and D.C. parametrics, and access and other timing parameters, including data retention. A comprehensive set of patterns is employed which subjects the modules to a variety of address, data, and timing schemes to ensure the product will perform as expected in customer environments.

High-Efficiency Burn-in

For over a decade, all IBM Microelectronics DRAMs have seen full In Situ burn-in, that is, dynamic stress with functional tests to monitor outputs while devices are undergoing burn-in. All fails experienced during burn-in, including those occurring at high voltage and temperature conditions, are identified. A typical In Situ burn-in test/stress sequence is shown in Figure 5. In Situ burn-in screen efficiency is unparalleled; it ensures full product functionality at burn-in conditions, finds equipment problems as they arise, and identifies unique fails during stress, including recoverable fails such as ionics. Because it provides reliability information for each production lot, In Situ burn-in has evolved as an important part of the maverick control strategy to improve line quality. Combined with our design and process control practices, it enables us to achieve world-class reliability levels on our DRAM products. Figure 6 on page 30 demonstrates the reliability benefit of In Situ burn-in; in the example, early life behavior is dominated by burn-in escapes (i.e., fails which, for equipment and other

Figure 5. In Situ Burn-in Stress/Test Sequence

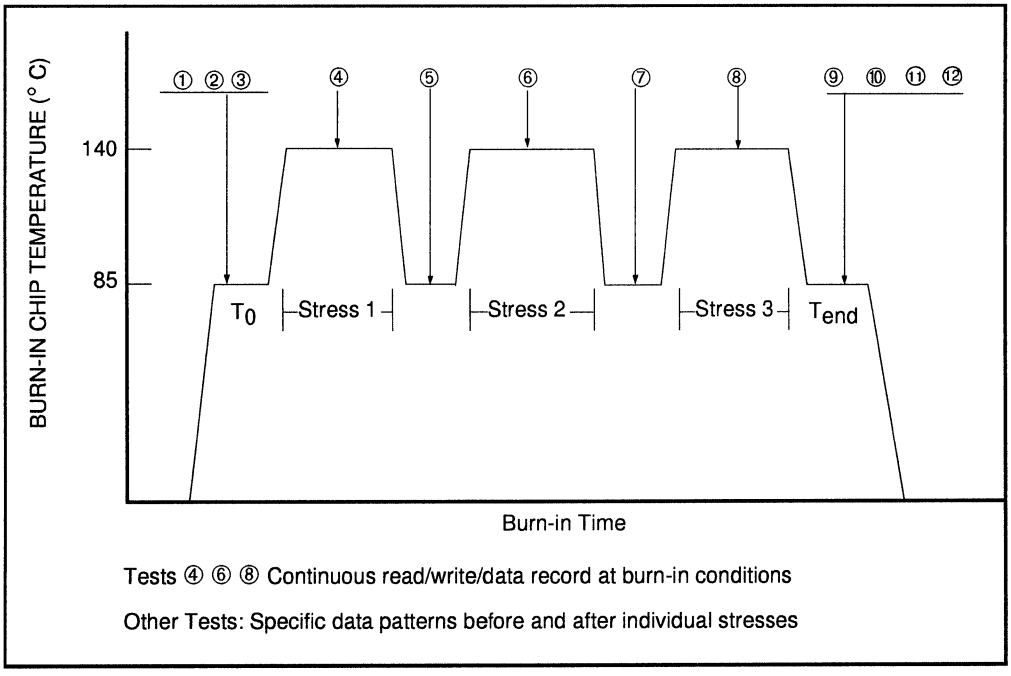
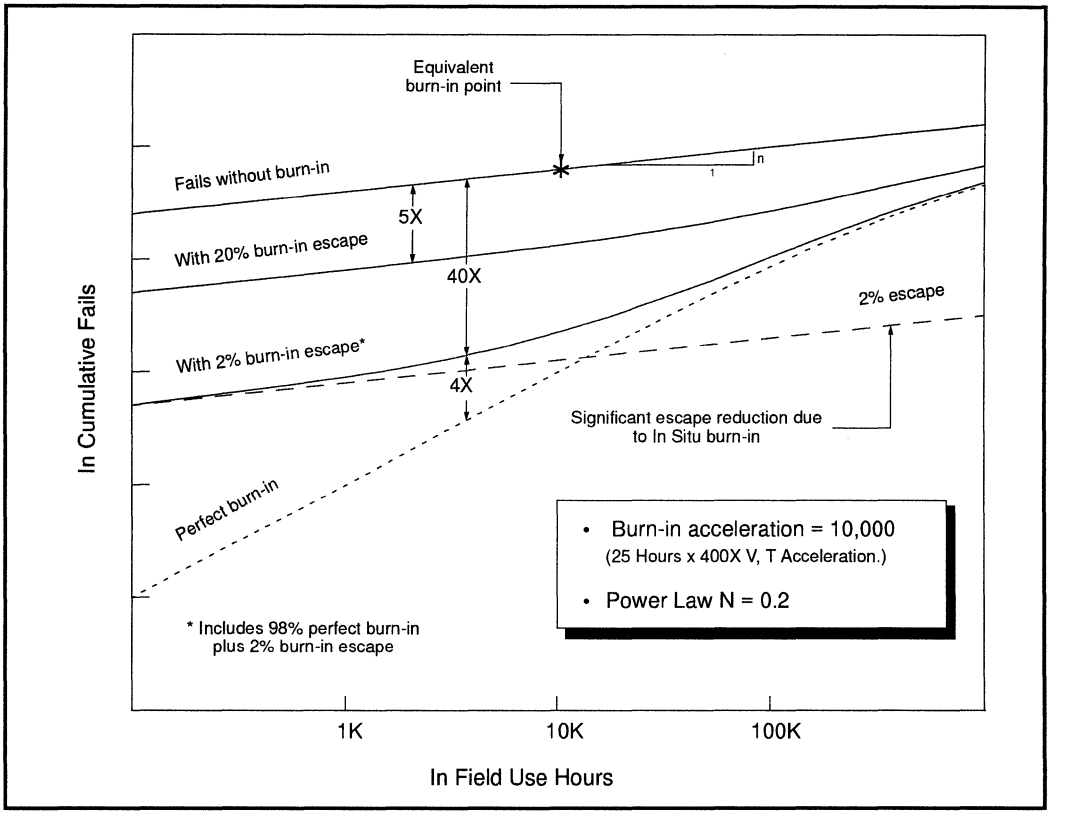


Figure 6. Example of In Situ Burn-in Reliability Benefit



reasons, escape the full burn-in process, and which are minimized by In Situ burn-in).

Quality/Reliability Monitor Program

Once in full production, product chip and assembly test and stress monitors are established to provide an ongoing measurement of line quality and reliability. Samples are drawn from products representing each major process and packaging technology. A quarterly report summarizing monitor results is available upon request. The data is used by IBM Microelectronics to measure overall product quality and reliability trends, to detect quality and reliability problems, and to verify corrective actions.

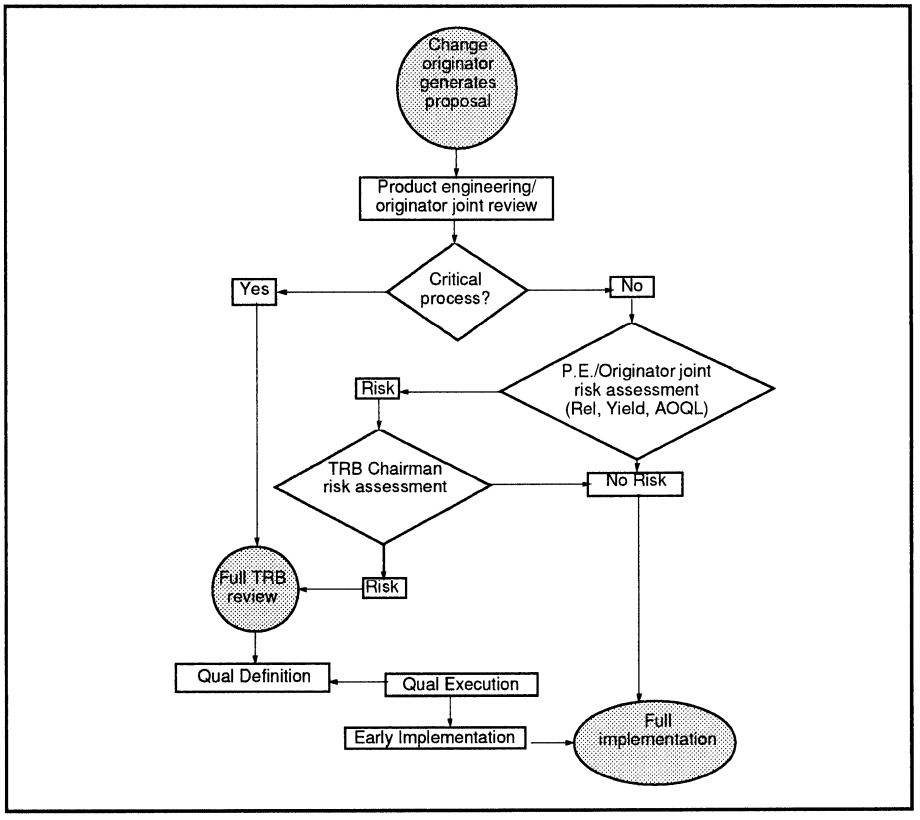
Process/Design Re-qualification

Re-qualification is required whenever major process or design changes occur, and appropriate tests and stresses are performed. Figure 7 on page 31 summarizes the re-qualification process. Changes are classified as potentially impacting form, fit, function, or reliability, as determined by the Technical Review Board (TRB).

Quality/Reliability Maintenance

In-line and end-of-line critical parameters have been established to measure and control manufacturing operations which may affect quality and reliability performance. Parametric trends are routinely monitored via statistical process control (SPC), and corrective actions are taken as required. In addition, a

Figure 7. Re-qualification Process



comprehensive system of maverick limits has been defined which detects systematic process and defect problems with known or possible adverse reliability or quality impact, and provides appropriate disposition of product containing such problems. This disposition frequently results in wafers being scrapped. These actions have resulted in improved process control and tighter process distributions, leading to better quality and reliability. The maverick control process is summarized in Figure 8 on page 32; a diagram illustrating the use of In Situ burn-in data for maverick control is shown in Figure 9 on page 33.

Quality Monitor And Customer Feedback

The customer feedback process is a key component of our quality program. Our semiconductor manufacturing facility has a long history of working very closely with card and system manufacturing sites to obtain significant product performance data. It is through such data exchange programs that IBM Microelectronics has demonstrated world class product performance, with the goal of continuous improvement for all of our customers.

Figure 8. Maverick Control Process

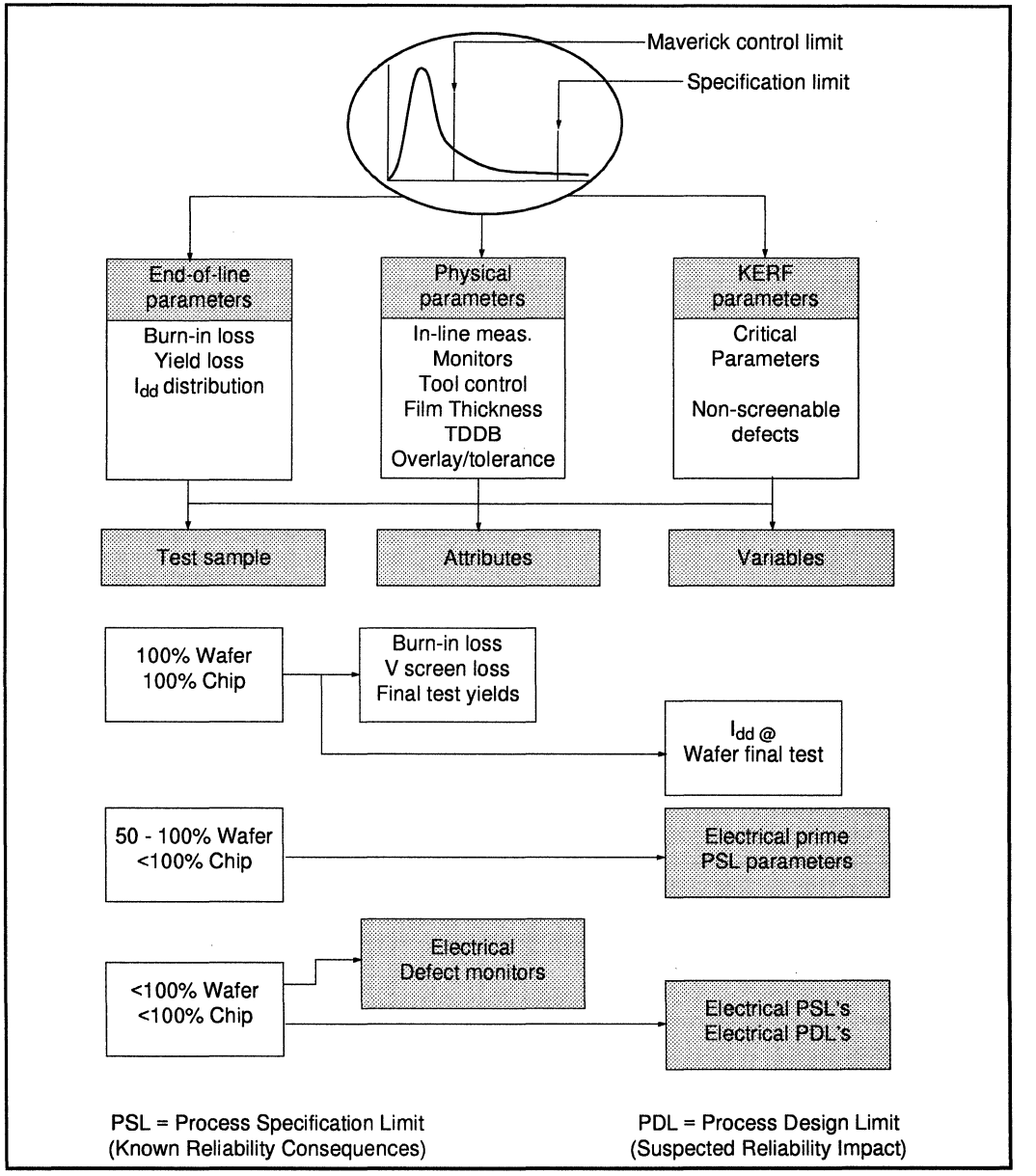
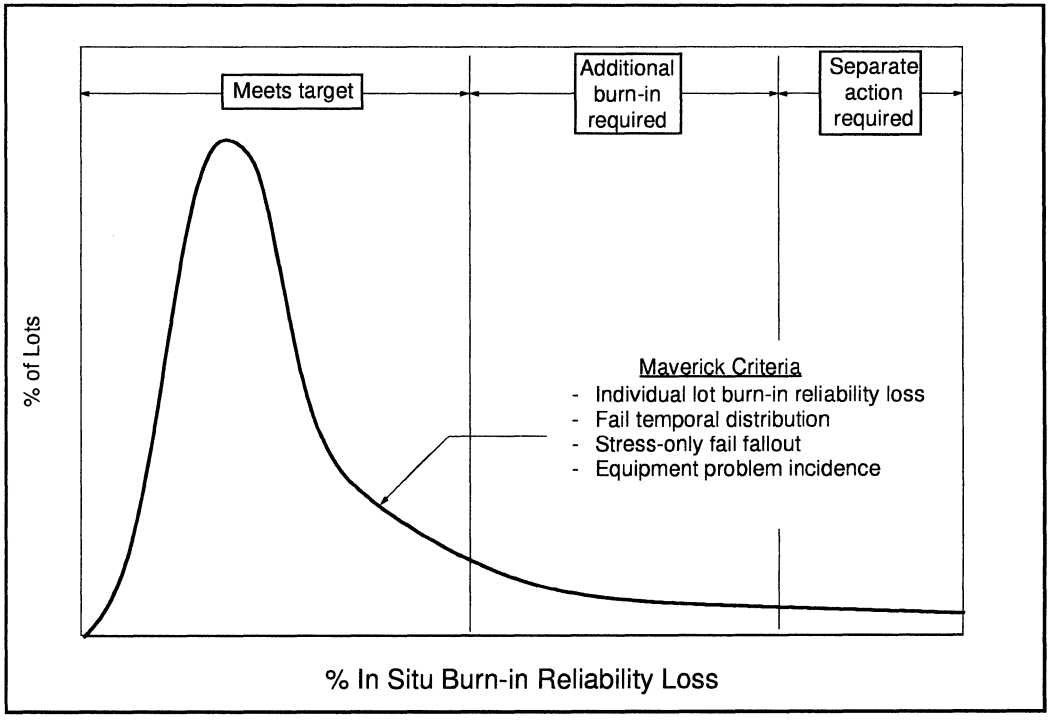


Figure 9. In Situ Maverick Control Process



72 Pin SIMMs

- Parity

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

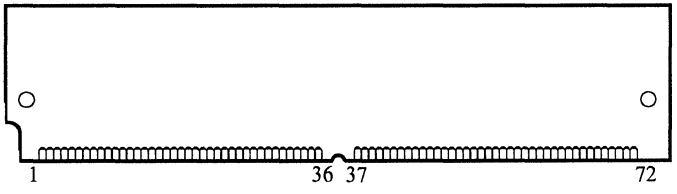
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au and Sn/Pb versions available

Description

The IBM11D1320BB/C is a 4MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 1Mx32 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 8 1Mx4 devices, each in either a 350mil or 300mil package, and is compatible with the JEDEC 72-Pin SIMM standard.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 1Mx36 parity SIMM, IBM11D1360B, as well as higher density and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	NC	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	NC	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ32	72	V_{SS}

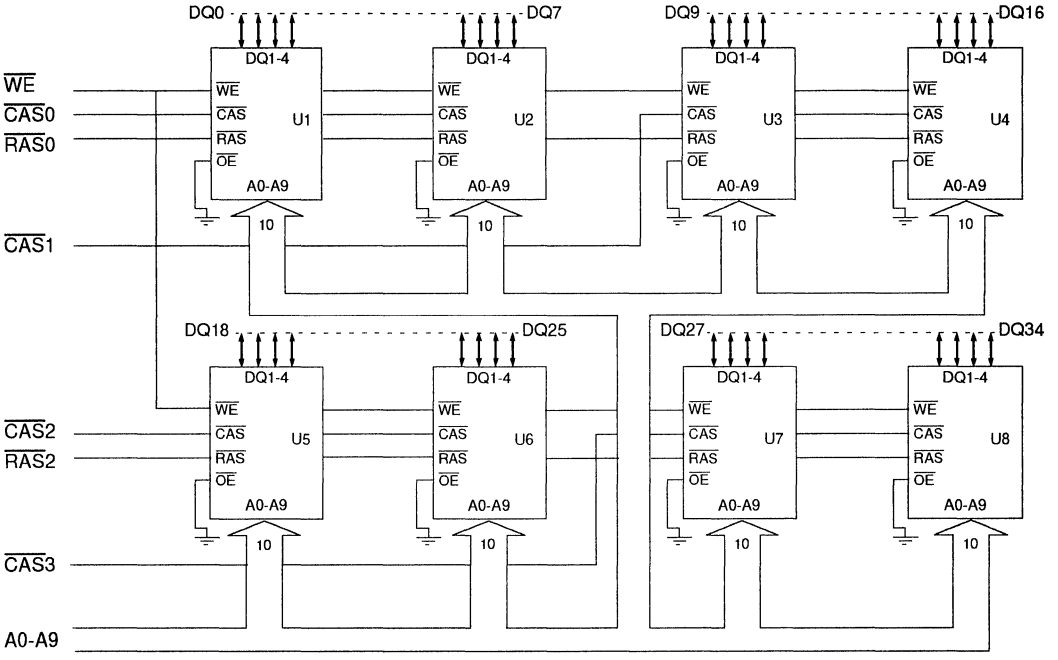
1. DQ numbering is compatible with parity (x36) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D1320BA-60	1M x 32	60ns	Sn/Pb	4.25" x 1" x .205"	
IBM11D1320BA-70	1M x 32	70ns	Sn/Pb	4.25" x 1" x .205"	
IBM11E1320BA-60	1M x 32	60ns	Au	4.25" x 1" x .205"	
IBM11E1320BA-70	1M x 32	70ns	Au	4.25" x 1" x .205"	
IBM11D1320BB-60	1M x 32	60ns	Sn/Pb	4.25" x .85" x .205"	1
IBM11D1320BB-70	1M x 32	70ns	Sn/Pb	4.25" x .85" x .205"	1
IBM11E1320BB-60	1M x 32	60ns	Au	4.25" x .85" x .205"	1
IBM11E1320BB-70	1M x 32	70ns	Au	4.25" x .85" x .205"	1
IBM11D1320BC-60	1M x 32	60ns	Sn/Pb	4.25" x 1" x .205"	2
IBM11D1320BC-70	1M x 32	70ns	Sn/Pb	4.25" x 1" x .205"	2
IBM11E1320BC-60	1M x 32	60ns	Au	4.25" x 1" x .205"	2
IBM11E1320BC-70	1M x 32	70ns	Au	4.25" x 1" x .205"	2

1. Limited availability, for height-constrained applications.
2. 'C' revision replaces 'A' revision, all specifications are identical or improved. 'C' revision uses new raw card which is common with IBM11D1360E.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 6.5	V	1
V_{IN}	Input Voltage	-0.7 to V_{CC} + 0.7	V	1
V_{OUT}	Output Voltage	-0.7 to V_{CC} + 0.7	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	5.25	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	50	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	26	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	14	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	41	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	13	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	960	mA	1, 2, 3
		-70	—	864		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	16	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	960	mA	1, 3
		-70	—	864		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	600	mA	1, 2, 3
		-70	—	560		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	16	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	960	mA	1, 3
		-70	—	864		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$	-20	+20		
		All others	-80	+80		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -4mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. The DRAM Outputs will remain disabled until these 8 cycles have occurred. This prevents data contention (excessive current) during power on. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	10	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	—	—	—	—	ns	3
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	45	—	50	—	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	10	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	10	—	15	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	10	0	15	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	2, 3

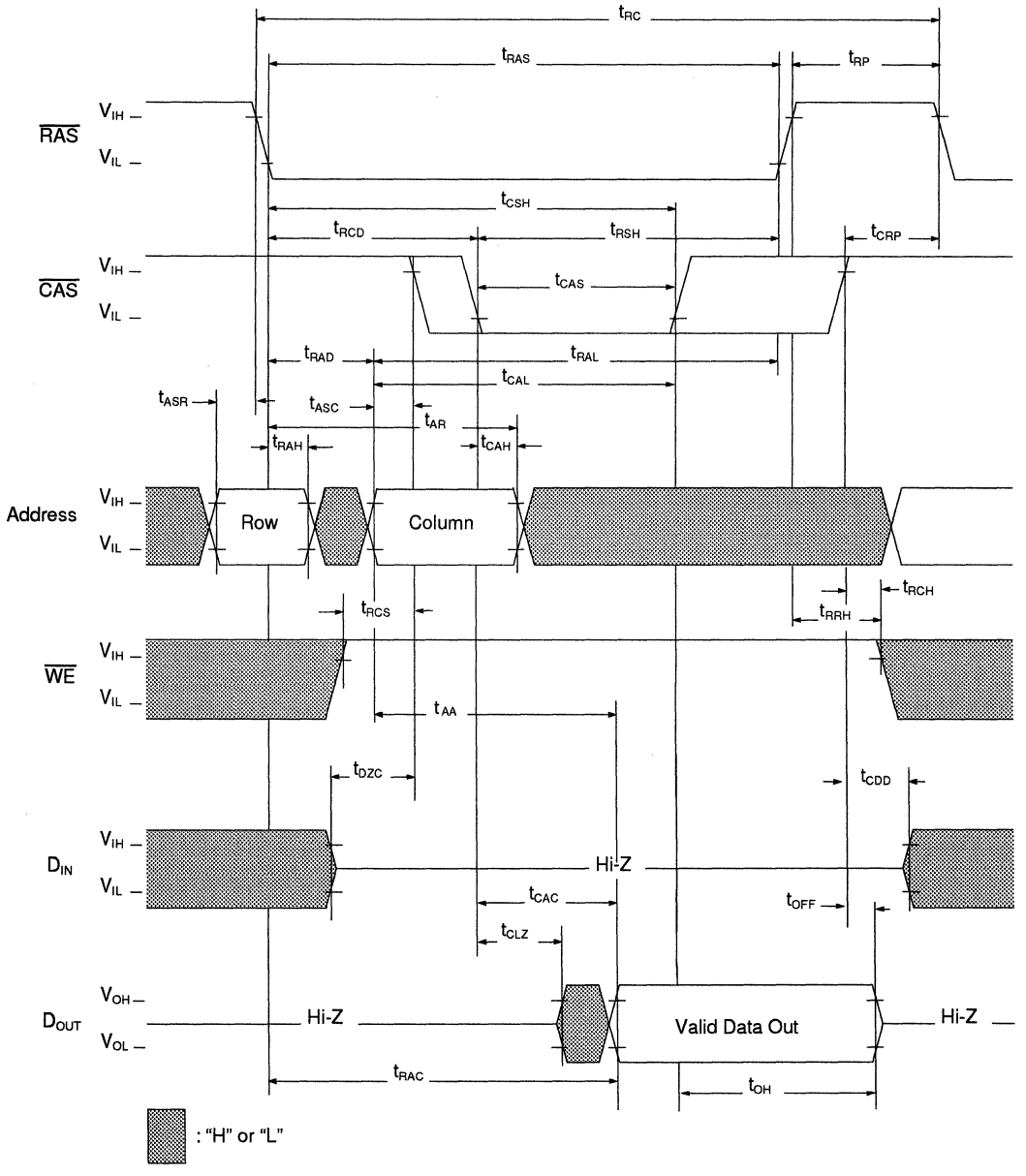
1. This timing parameter is not applicable to this product, but applies to a related product in this family.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Access time assumes a load of 100pF.

Refresh Cycle

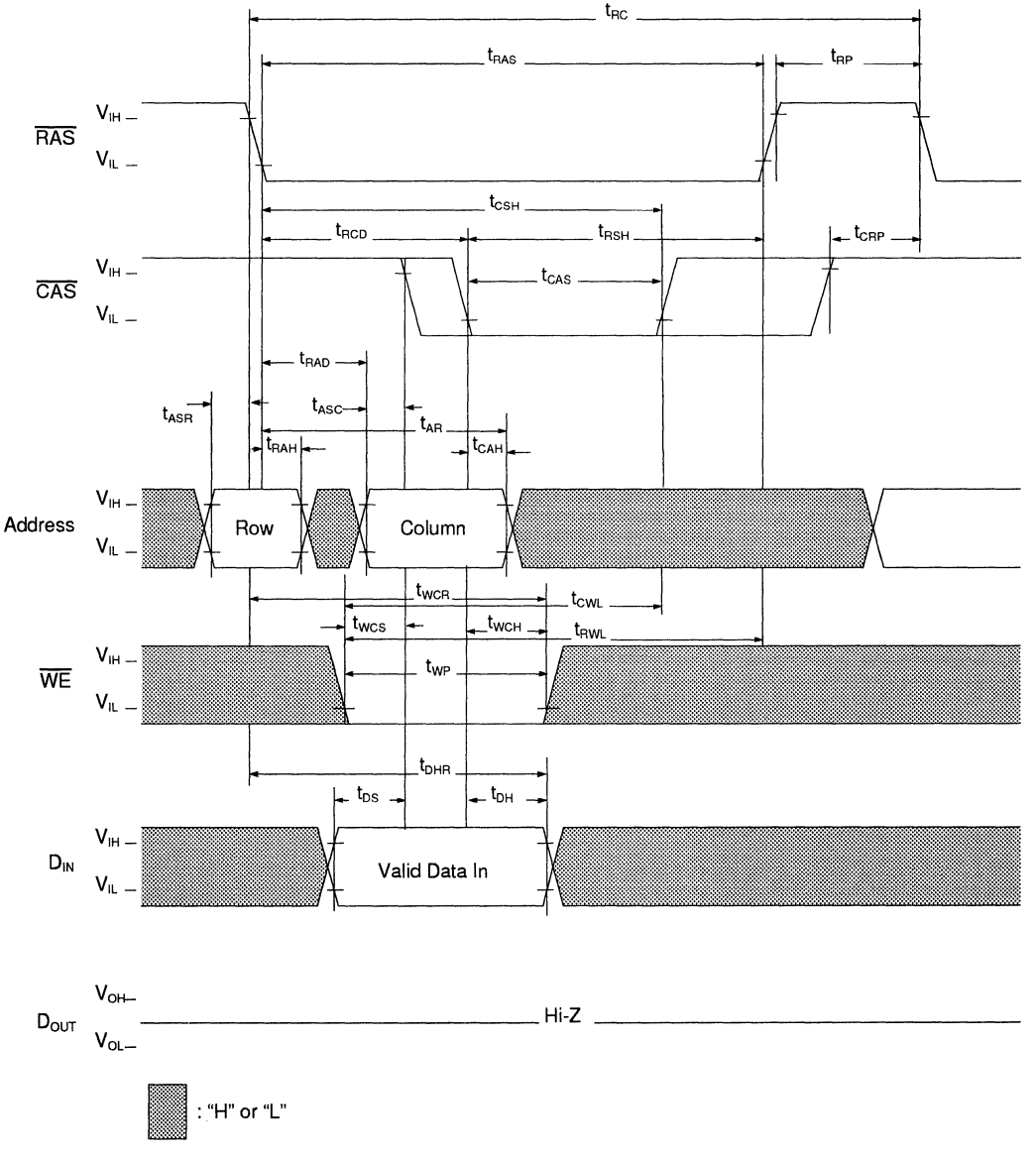
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	5	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms. The DC variation in the V_{CC} supply may not exceed 300mV within a refresh interval (16ms).

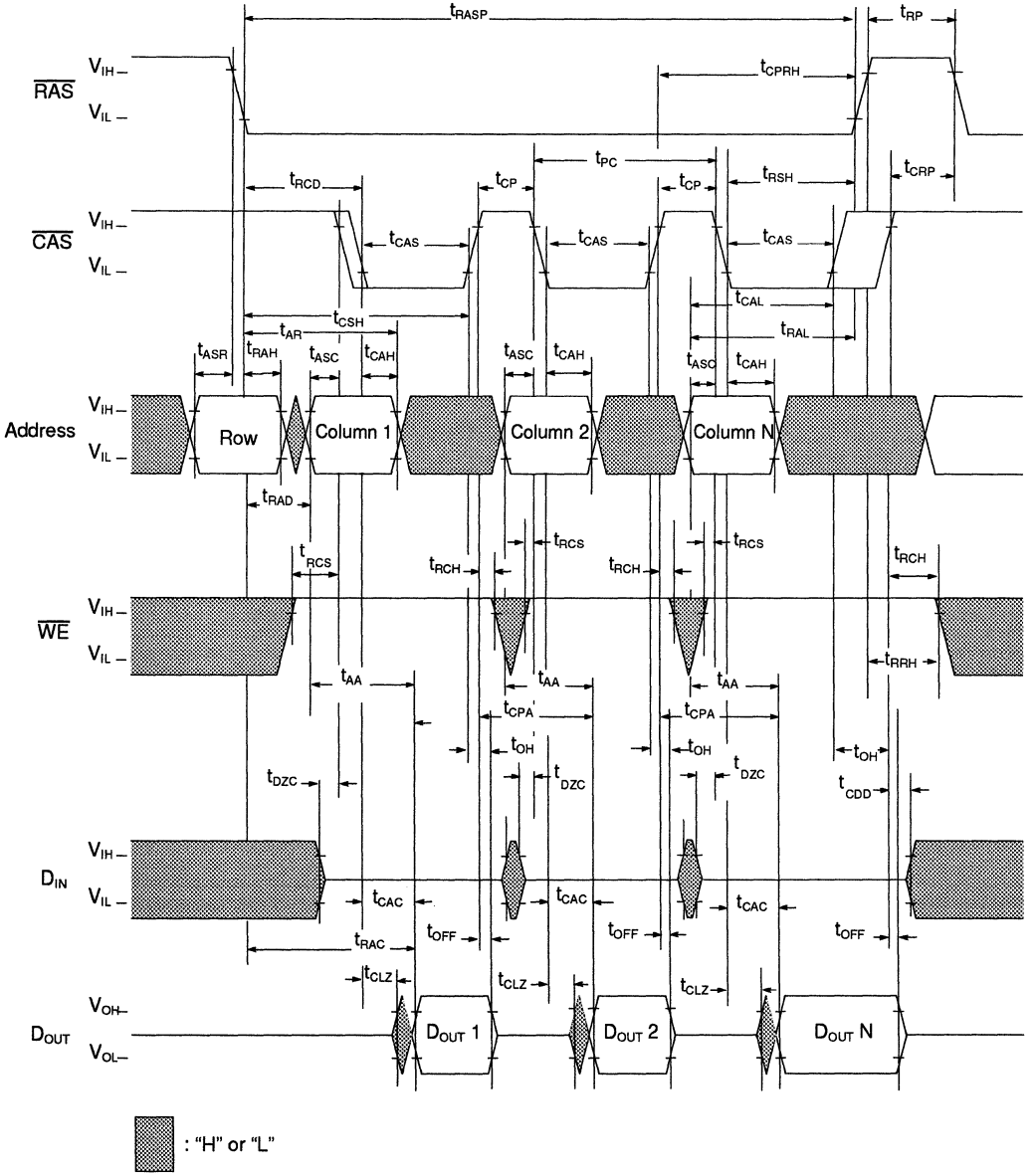
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

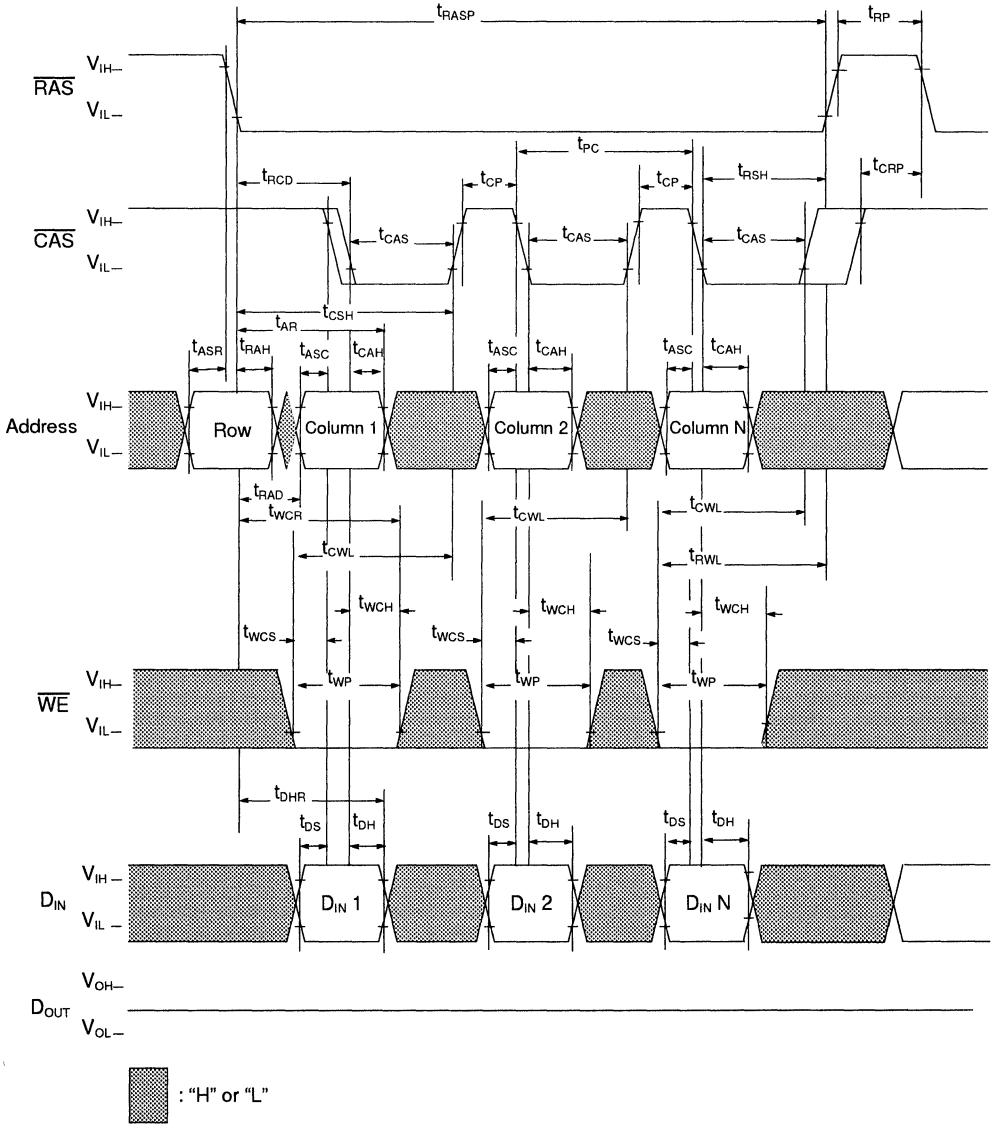
Write Cycle (Early Write)



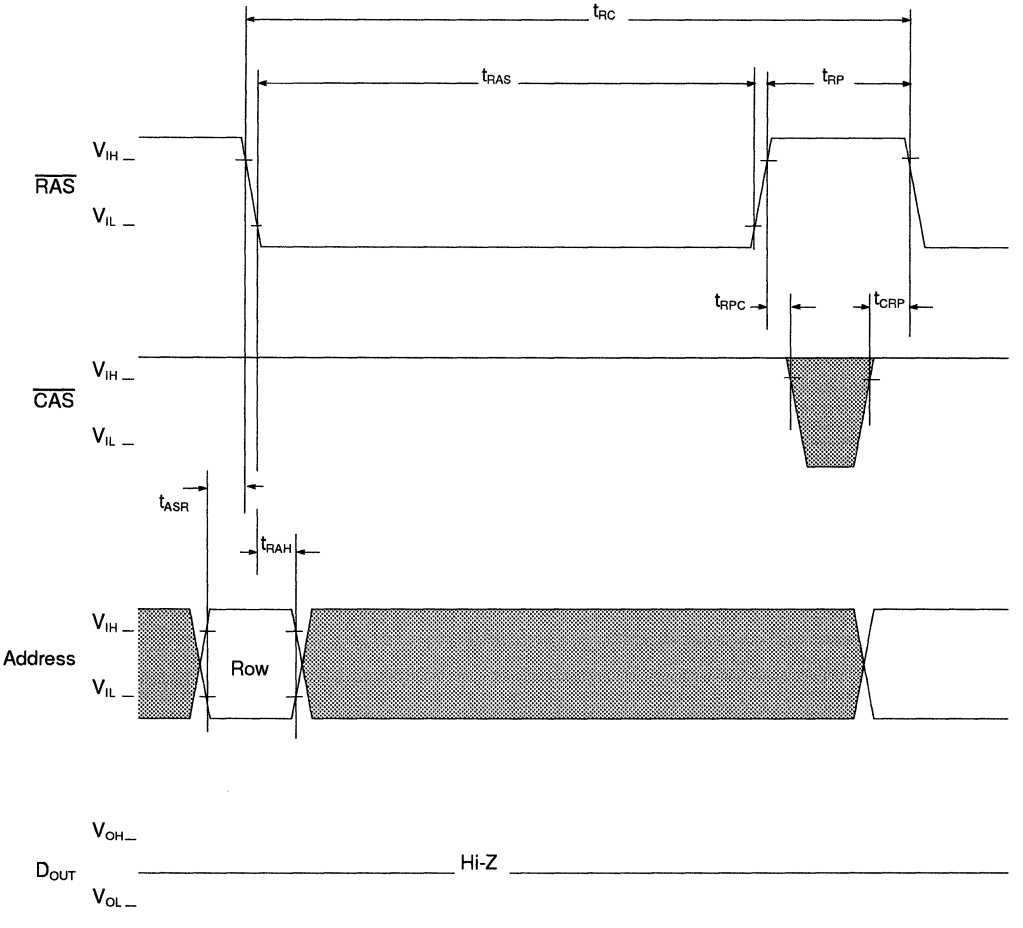
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

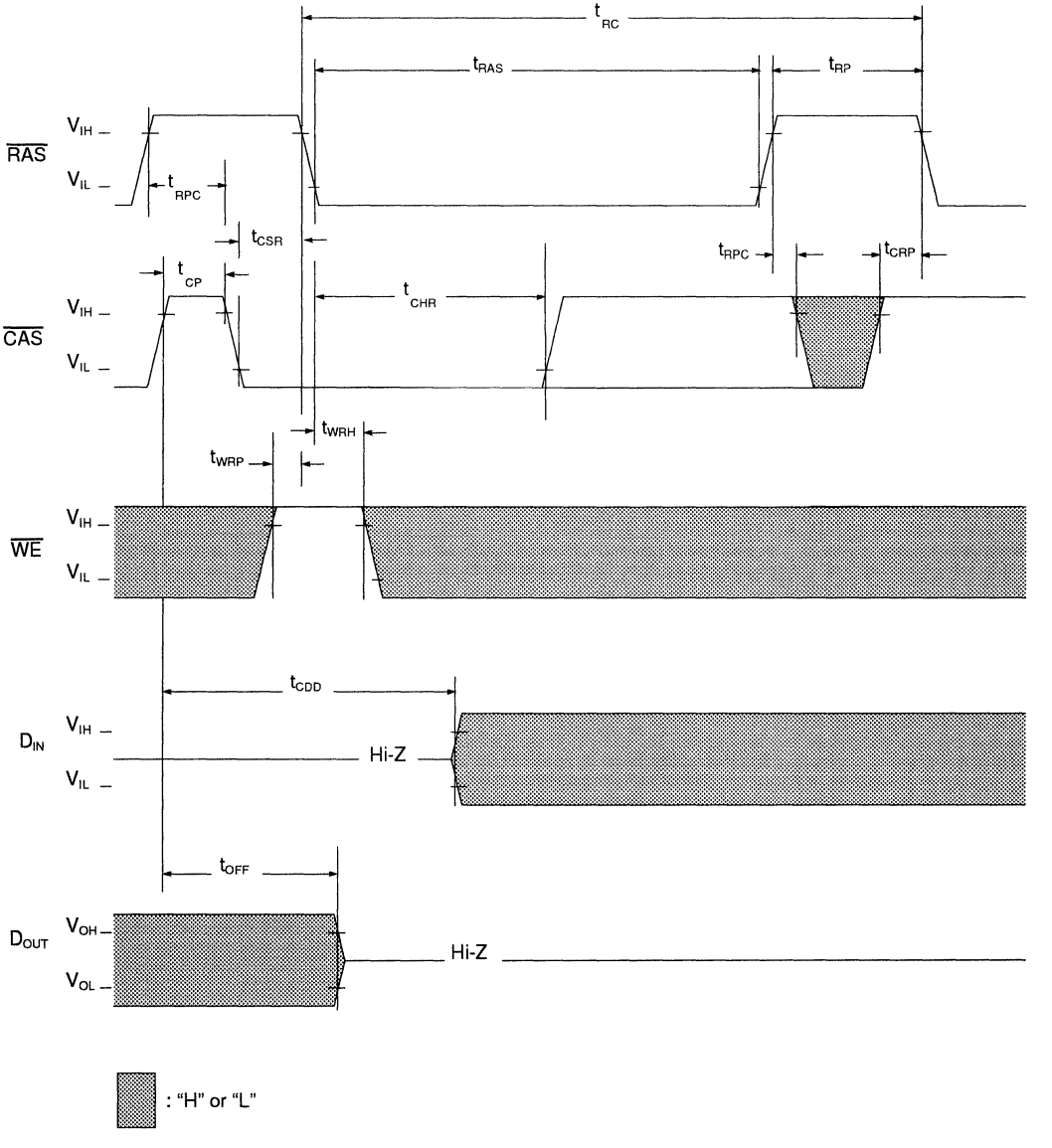


$\overline{RAS}$ Only Refresh Cycle



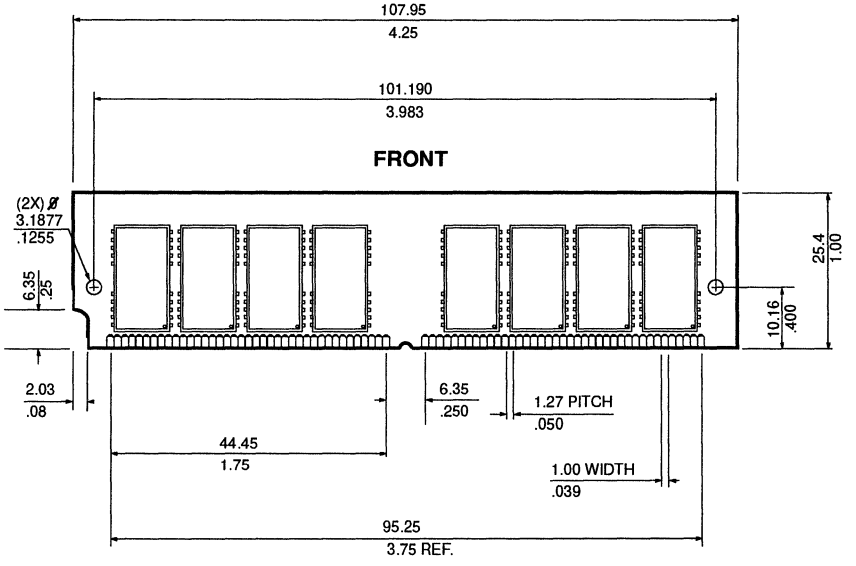
Note: $\overline{WE}$, D_{IN} are "H" or "L"

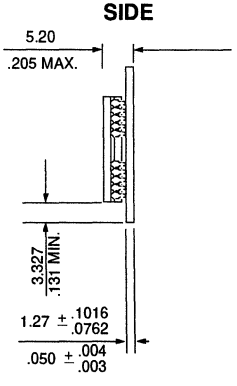
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing (IBM11E1320BB)





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	18ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	40ns

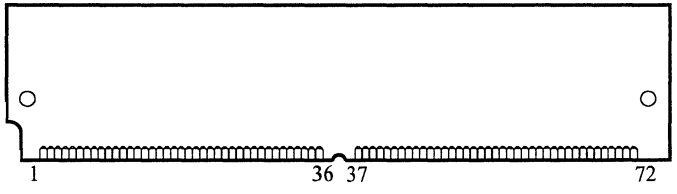
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- Low active current dissipation
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au and Sn/Pb versions available

Description

The IBM11D1320BD is a 4MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 1Mx32 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 8 1Mx4 devices, each in a 300mil package, and is compatible with the JEDEC 72-Pin SIMM standard.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 1Mx36 parity SIMM, IBM11D1360B, as well as higher density and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

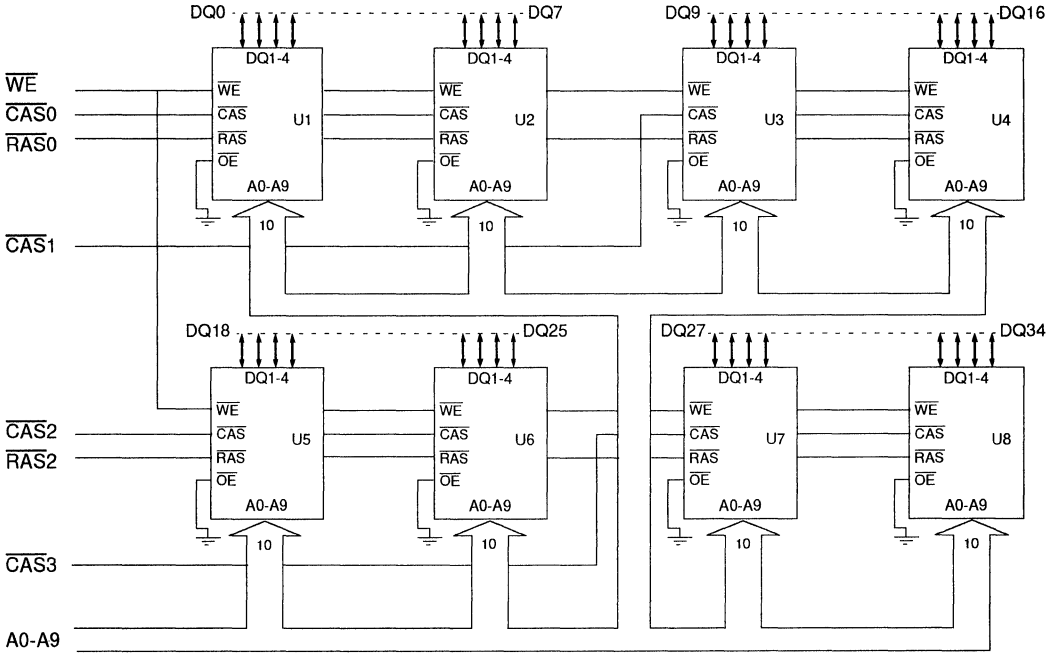
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	NC	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	NC	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with parity (x36) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D1320BD-60	1M x 32	60ns	Sn/Pb	4.25" x 1" x .205"	
IBM11D1320BD-70	1M x 32	70ns	Sn/Pb	4.25" x 1" x .205"	
IBM11E1320BD-60	1M x 32	60ns	Au	4.25" x 1" x .205"	
IBM11E1320BD-70	1M x 32	70ns	Au	4.25" x 1" x .205"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to + 6.0	V	1
V_{IN}	Input Voltage	-1.0 to + 6.0	V	1
V_{OUT}	Output Voltage	-1.0 to + 6.0	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	3.75	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	60	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	35	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	21	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	67	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	13	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	680	mA	1, 2, 3
		-70	—	560		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	16	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	680	mA	1, 3
		-70	—	560		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	480	mA	1, 2, 3
		-70	—	400		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	8	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	680	mA	1, 3
		-70	—	560		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$	-20	+20		
		All others	-80	+80		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	18	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	52	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	18	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	18	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	18	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	18	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	40	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

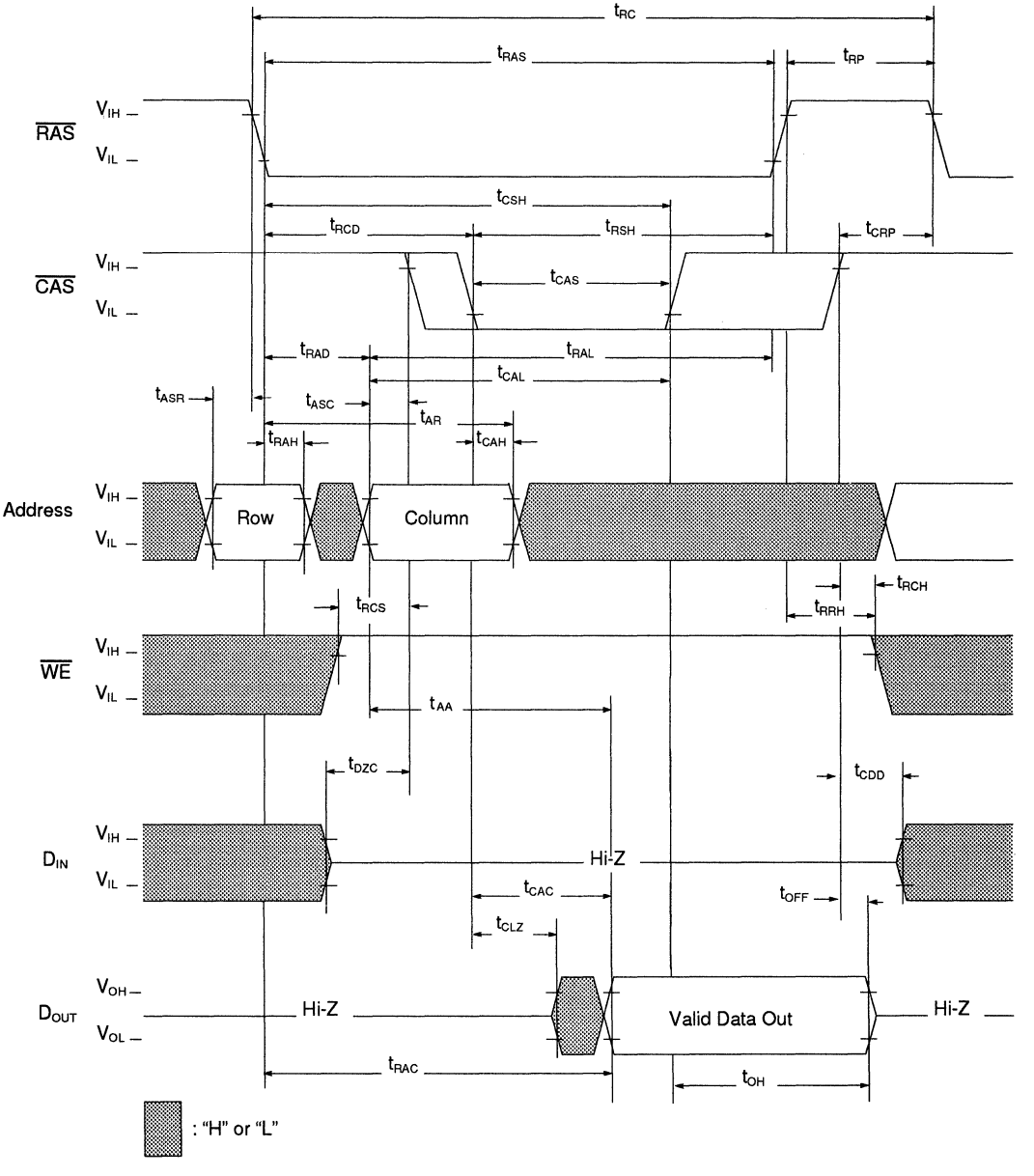
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

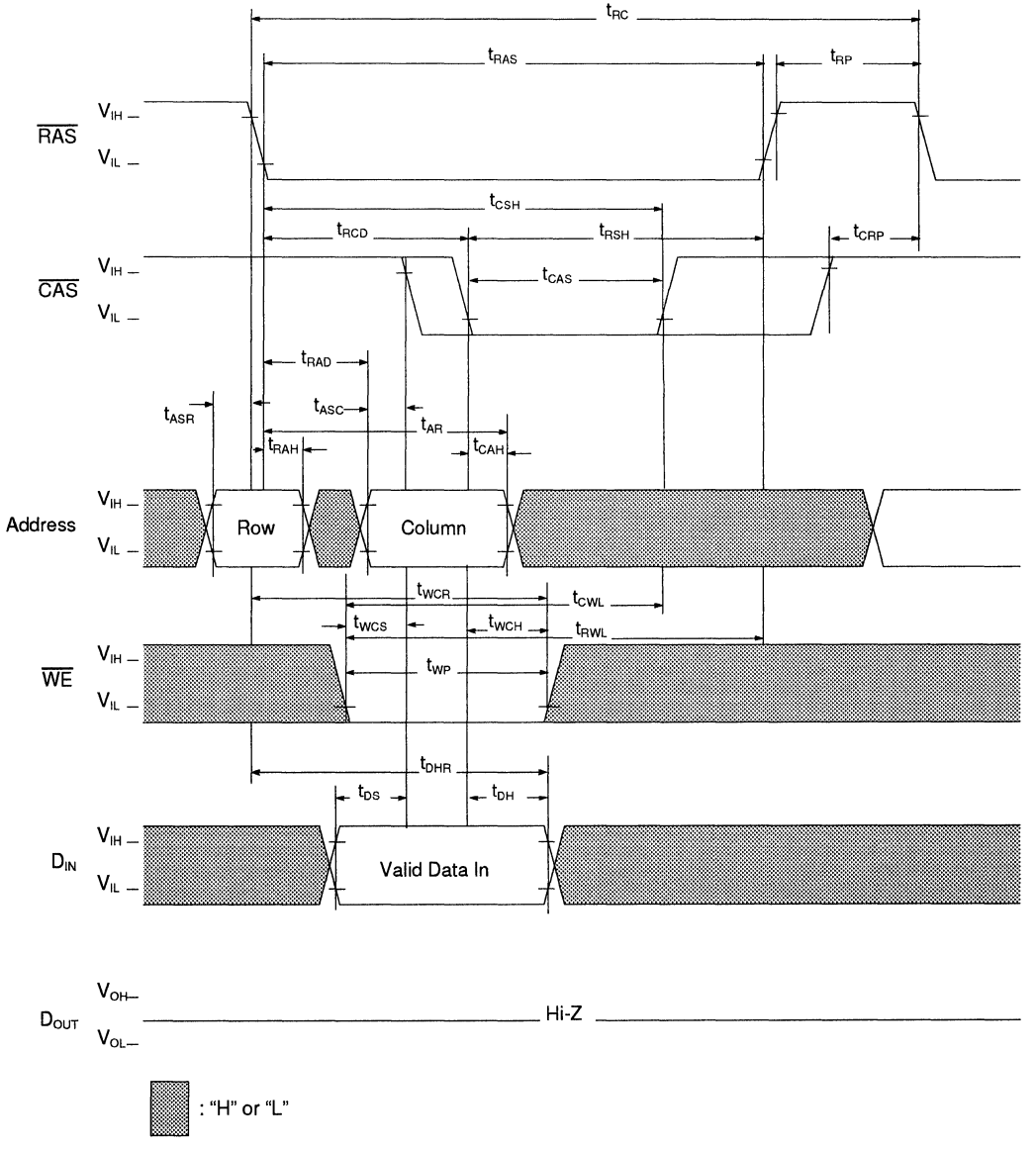
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms.

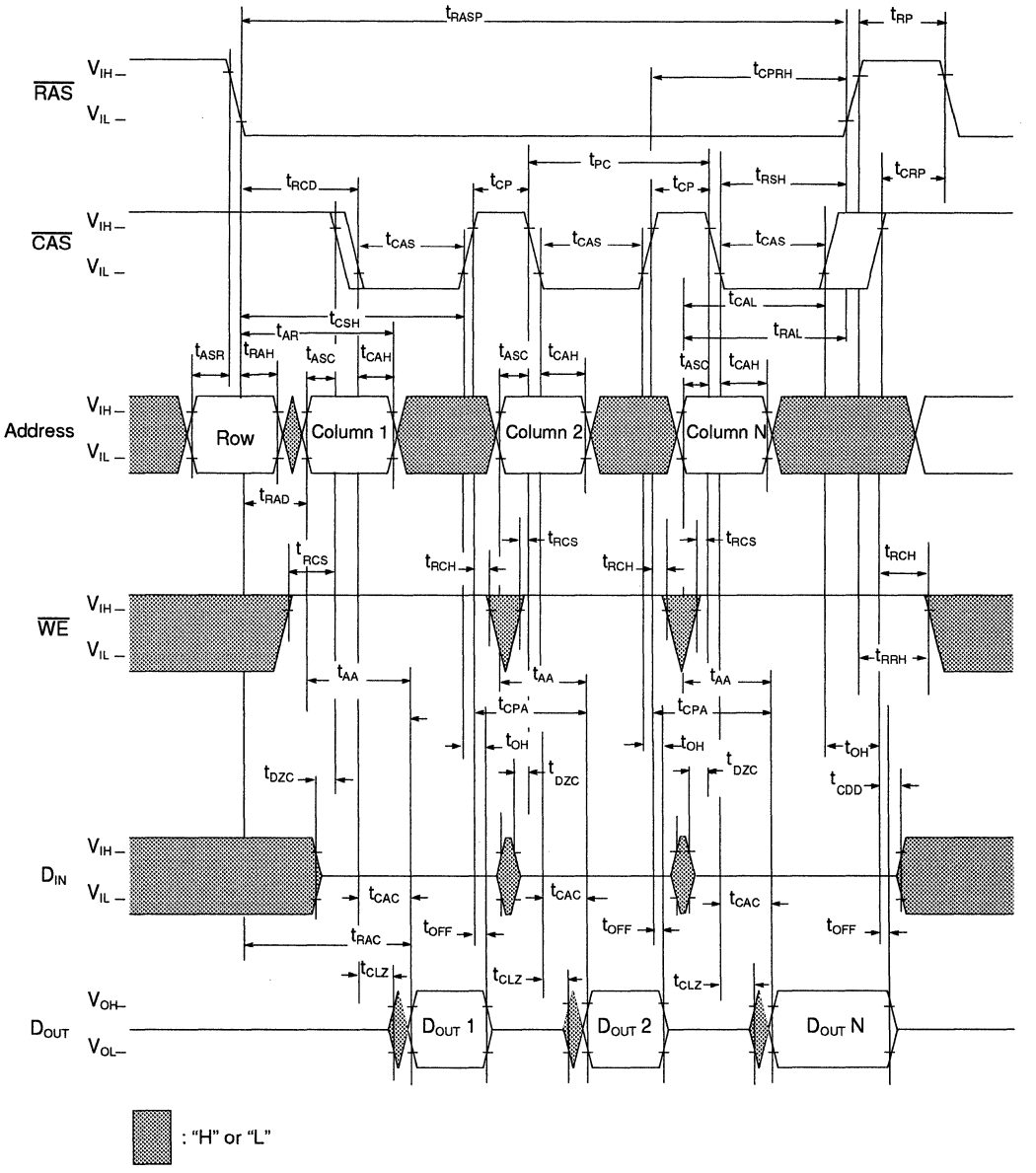
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCH
tRCS
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

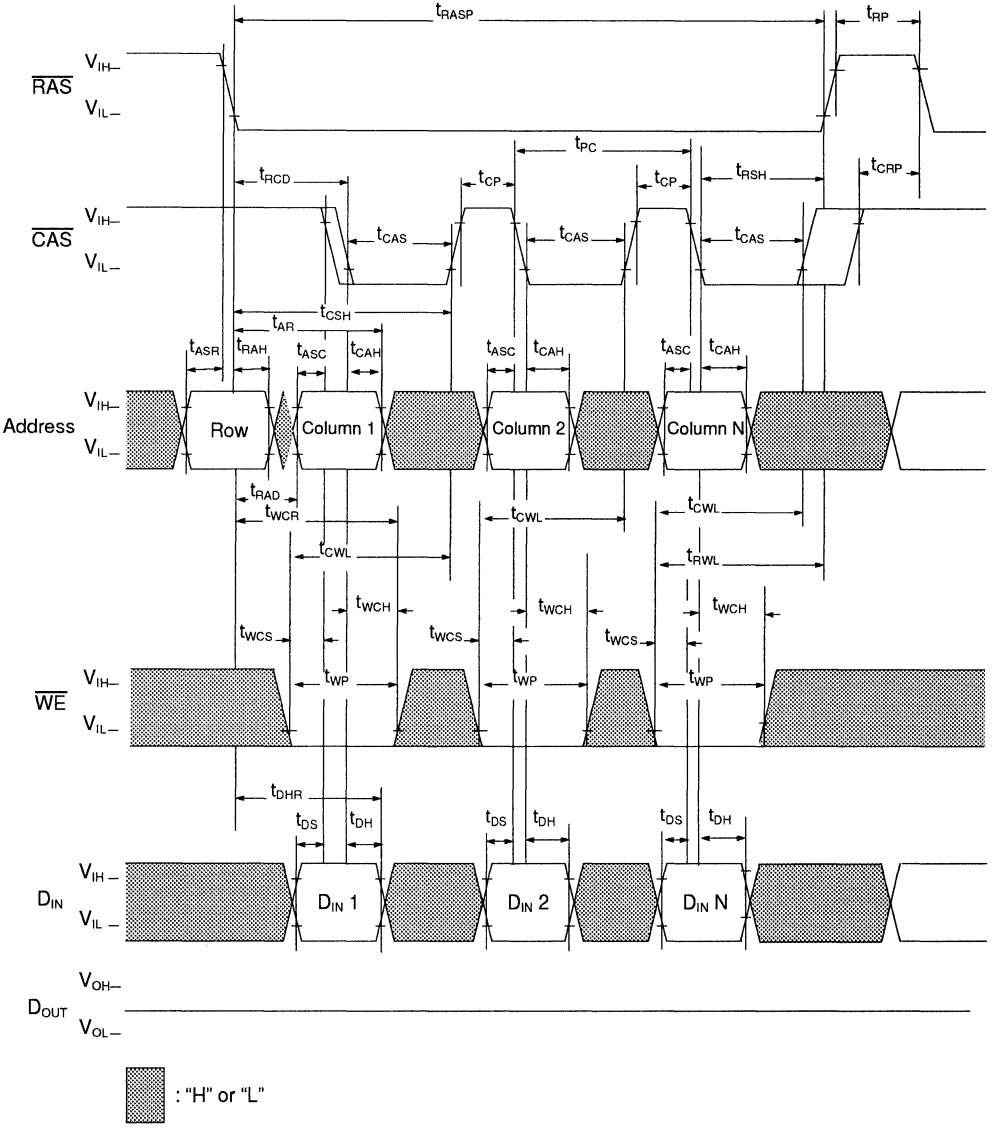
Write Cycle (Early Write)



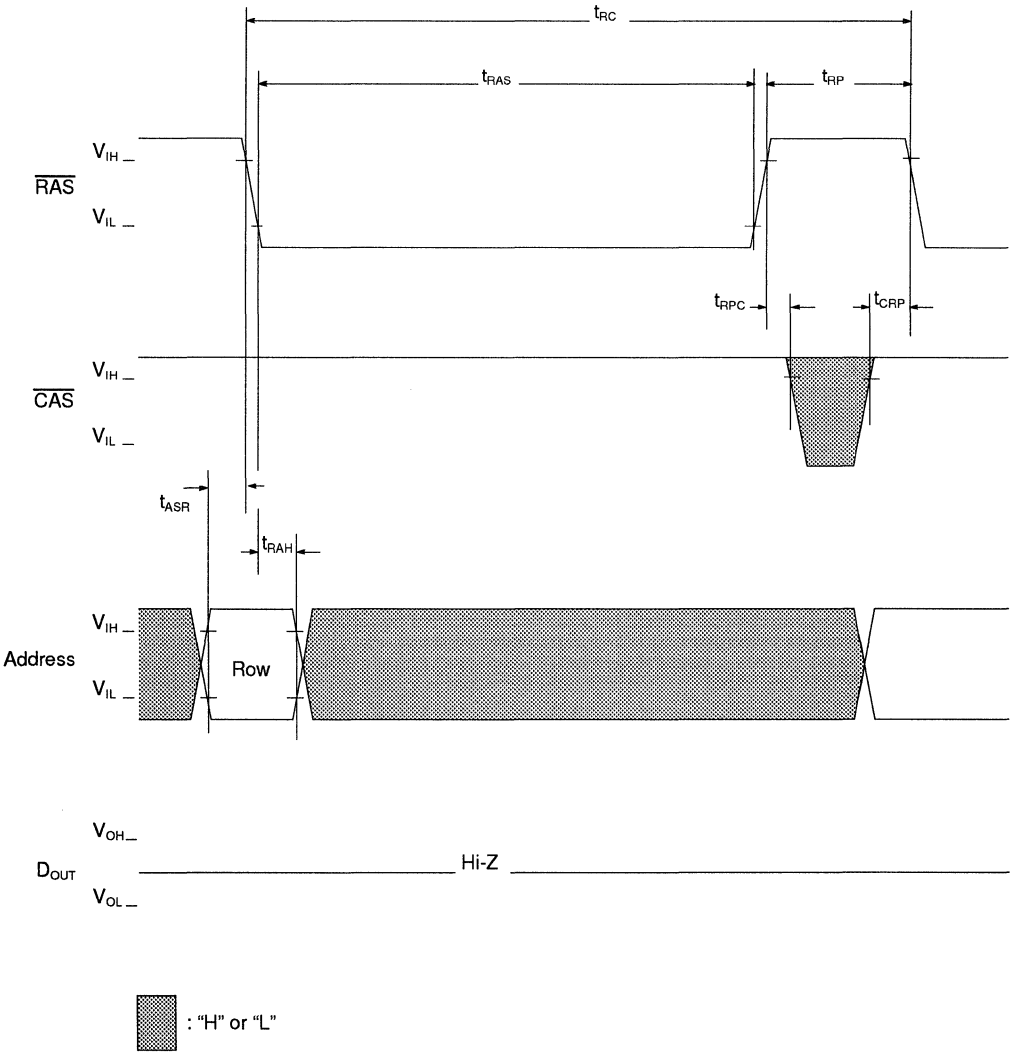
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

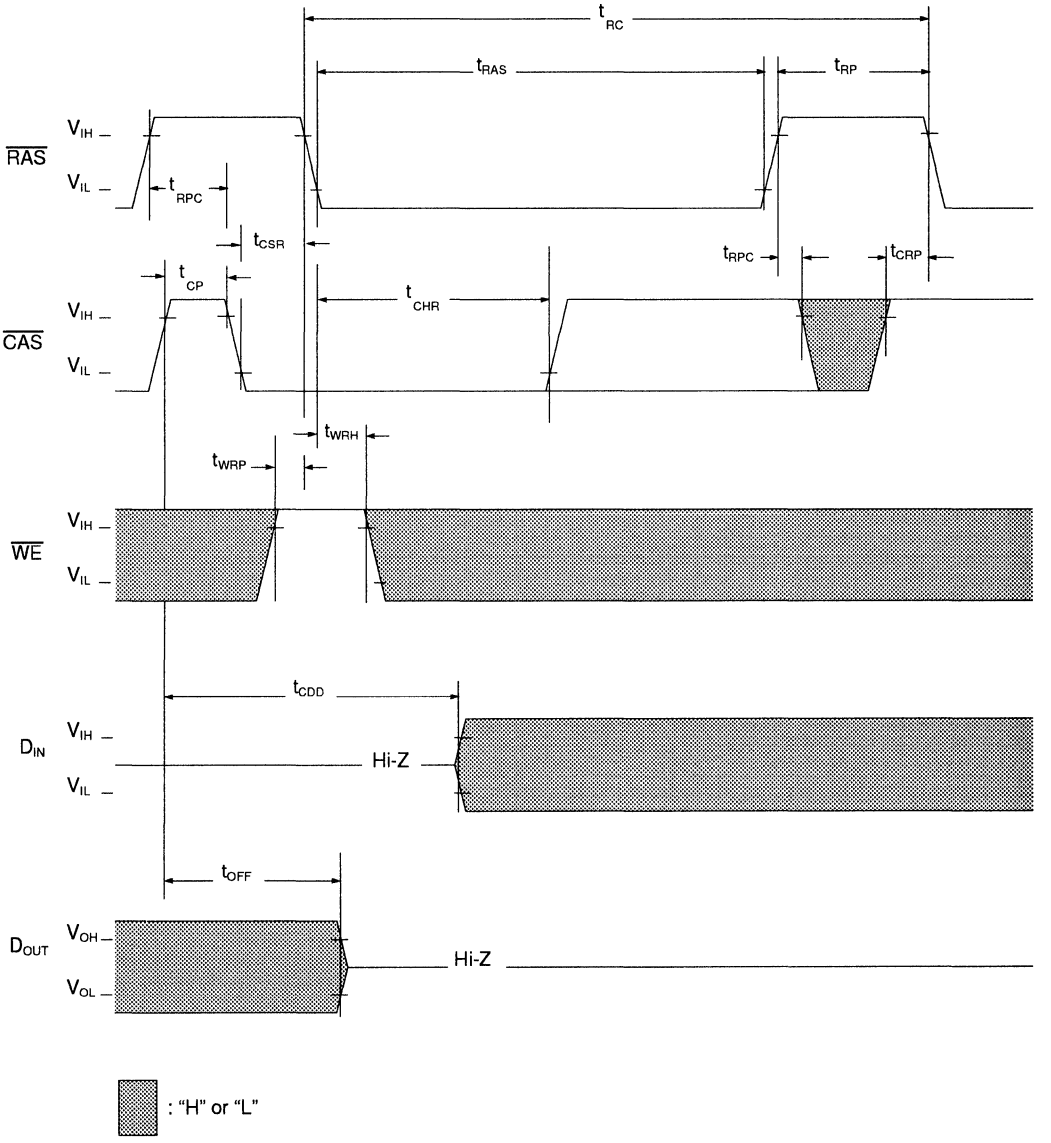


$\overline{RAS}$ Only Refresh Cycle



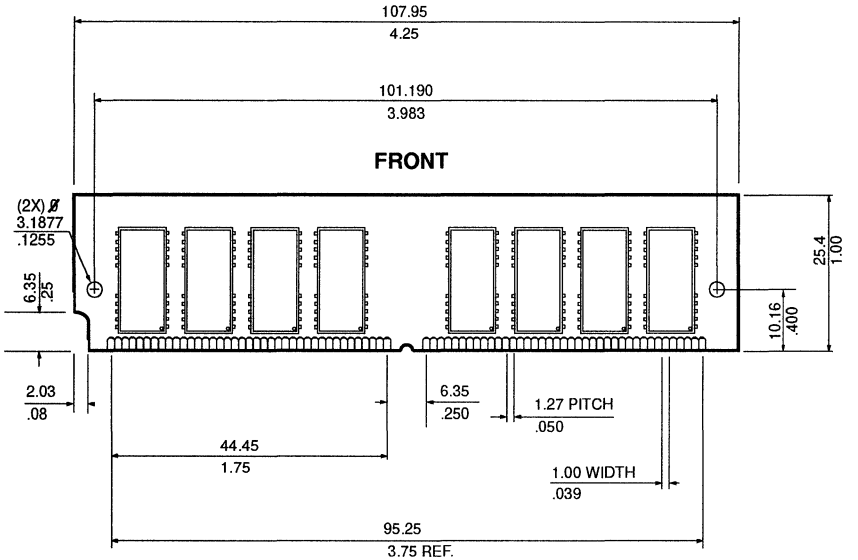
Note: $\overline{WE}$, D_{IN} are "H" or "L"

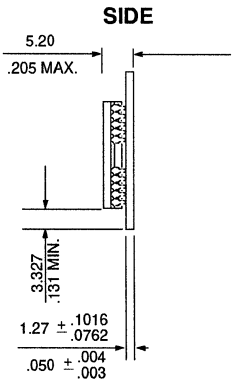
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

1M x 32 DRAM Module

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Manufactured with 16Mb DRAMS (1M x 16)
- Single 5V, ± 0.5V Power Supply
- Low current consumption
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au and Sn/Pb versions available

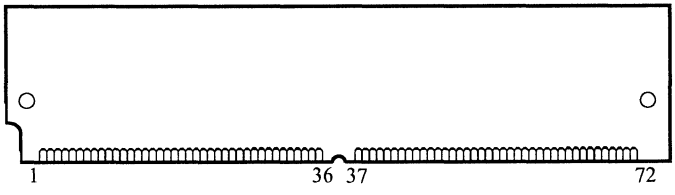
Description

The IBM11D1320L is a 4MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 1Mx32 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 2 1Mx16 devices, each in a 400mil TSOP package, and is compatible with the JEDEC 72-Pin SIMM standard.

This assembly is intended as a direct replacement for 1Mx4-based SIMMs, while significantly reducing power dissipation. The use of TSOP packages allows tighter SIMM spacing (.3" on center). Input loading is consistent with 4Mb-based assemblies due to the addition of discrete capacitors maximizing compatibility at the system-level.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 1Mx32 non-parity SIMM, IBM11D1320B, as well as higher density, parity and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

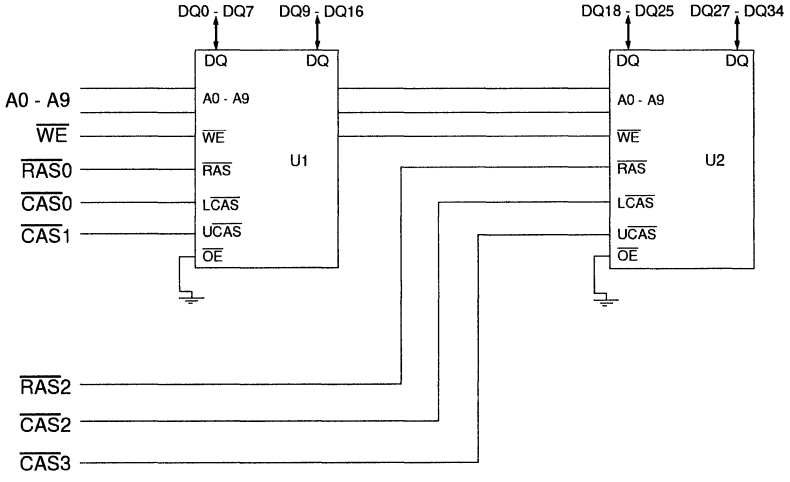
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	NC	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	NC	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with parity (x36) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D1320LA-60	1M x 32	60ns	Sn/Pb	4.25" x 1" x .104"	
IBM11D1320LA-70	1M x 32	70ns	Sn/Pb	4.25" x 1" x .104"	
IBM11E1320LA-60	1M x 32	60ns	Au	4.25" x 1" x .104"	
IBM11E1320LA-70	1M x 32	70ns	Au	4.25" x 1" x .104"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	2.1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	47	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	32	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	17	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	50	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	390	mA	1, 2, 3
		-70	—	340		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	4	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	390	mA	1, 3
		-70	—	340		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	180	mA	1, 2, 3
		-70	—	160		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	2	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	390	mA	1, 3
		-70	—	340		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-10	+10	µA	
		$\overline{CAS}$	-10	+10		
		All others	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

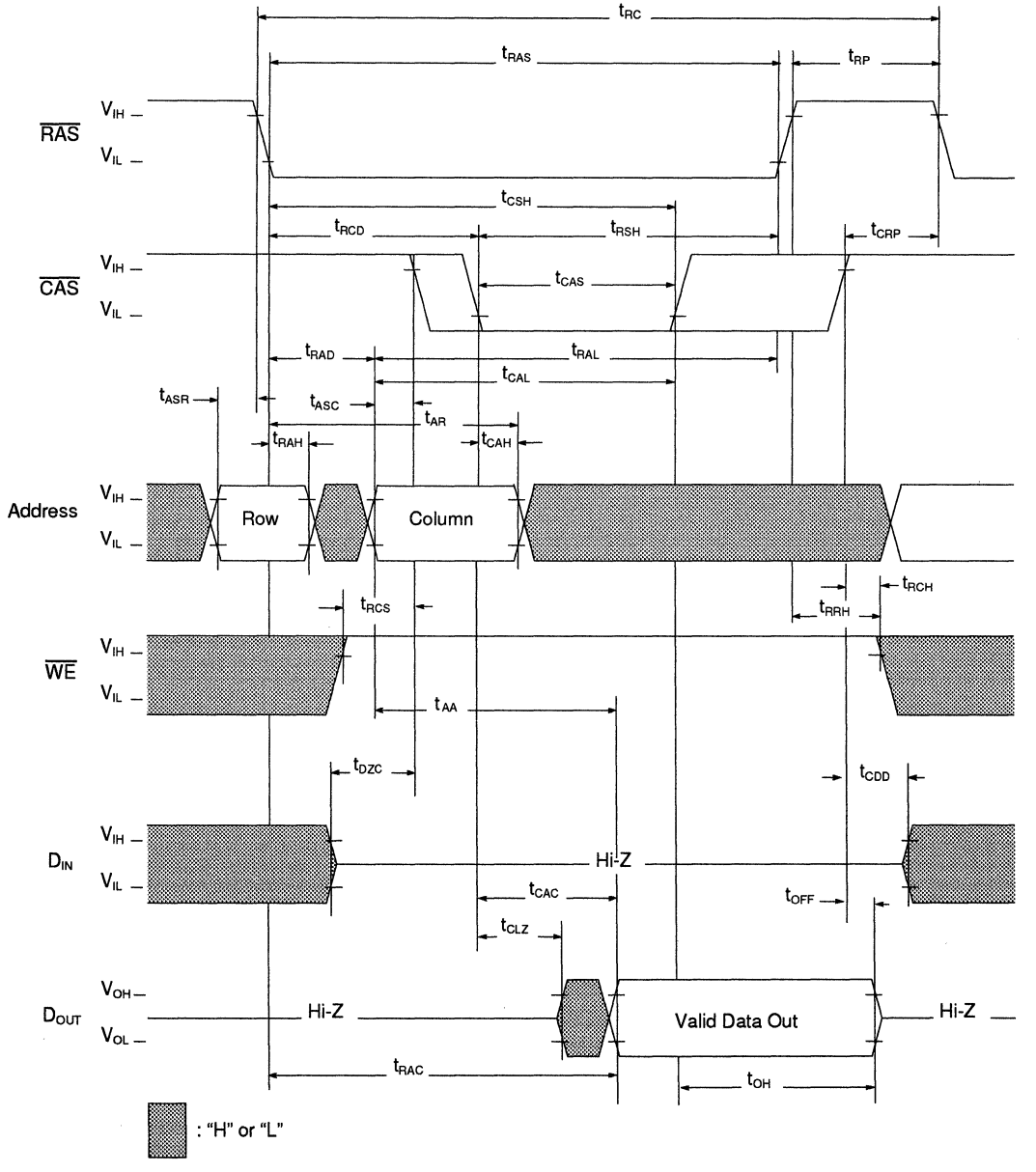
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

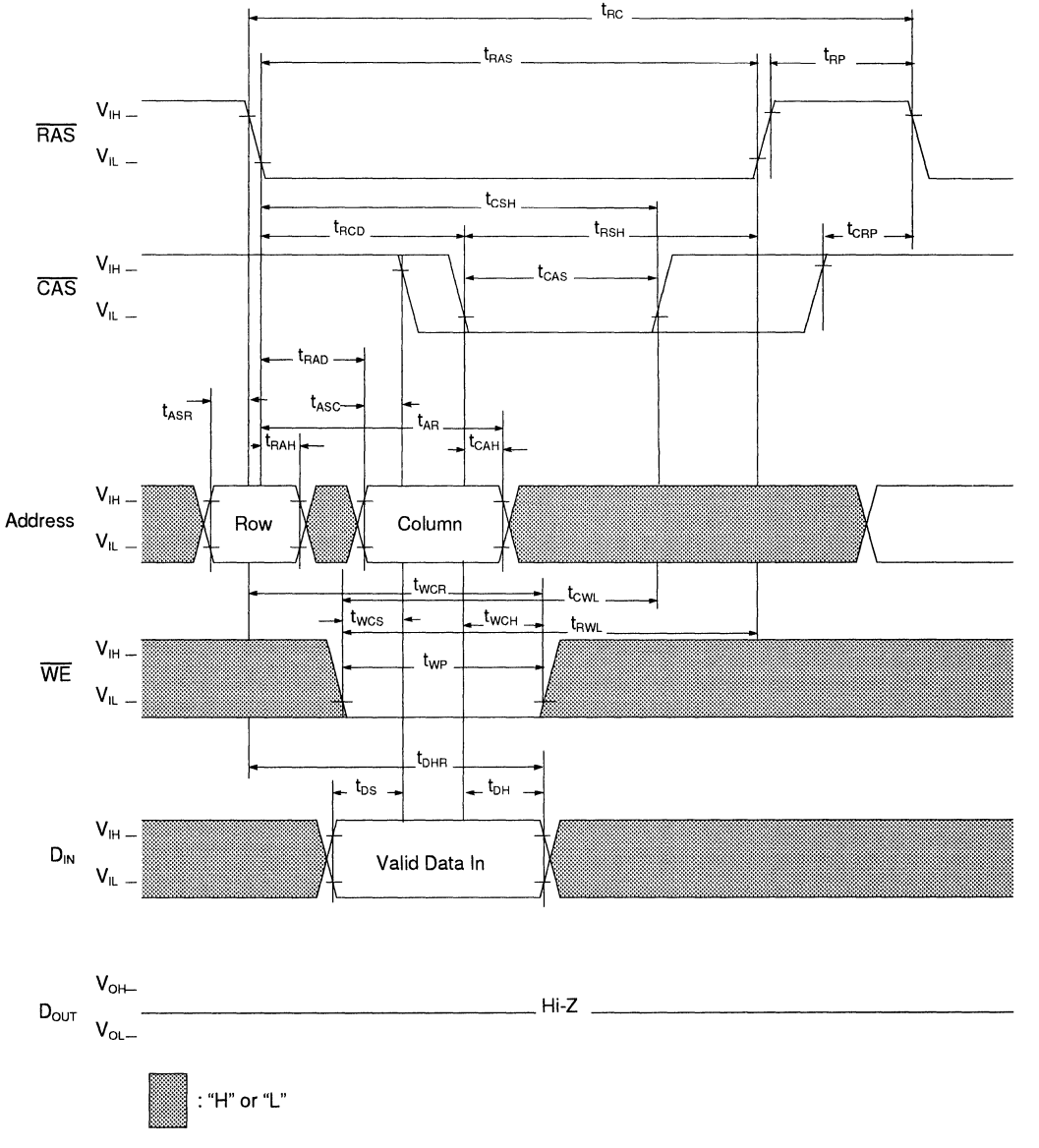
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms.

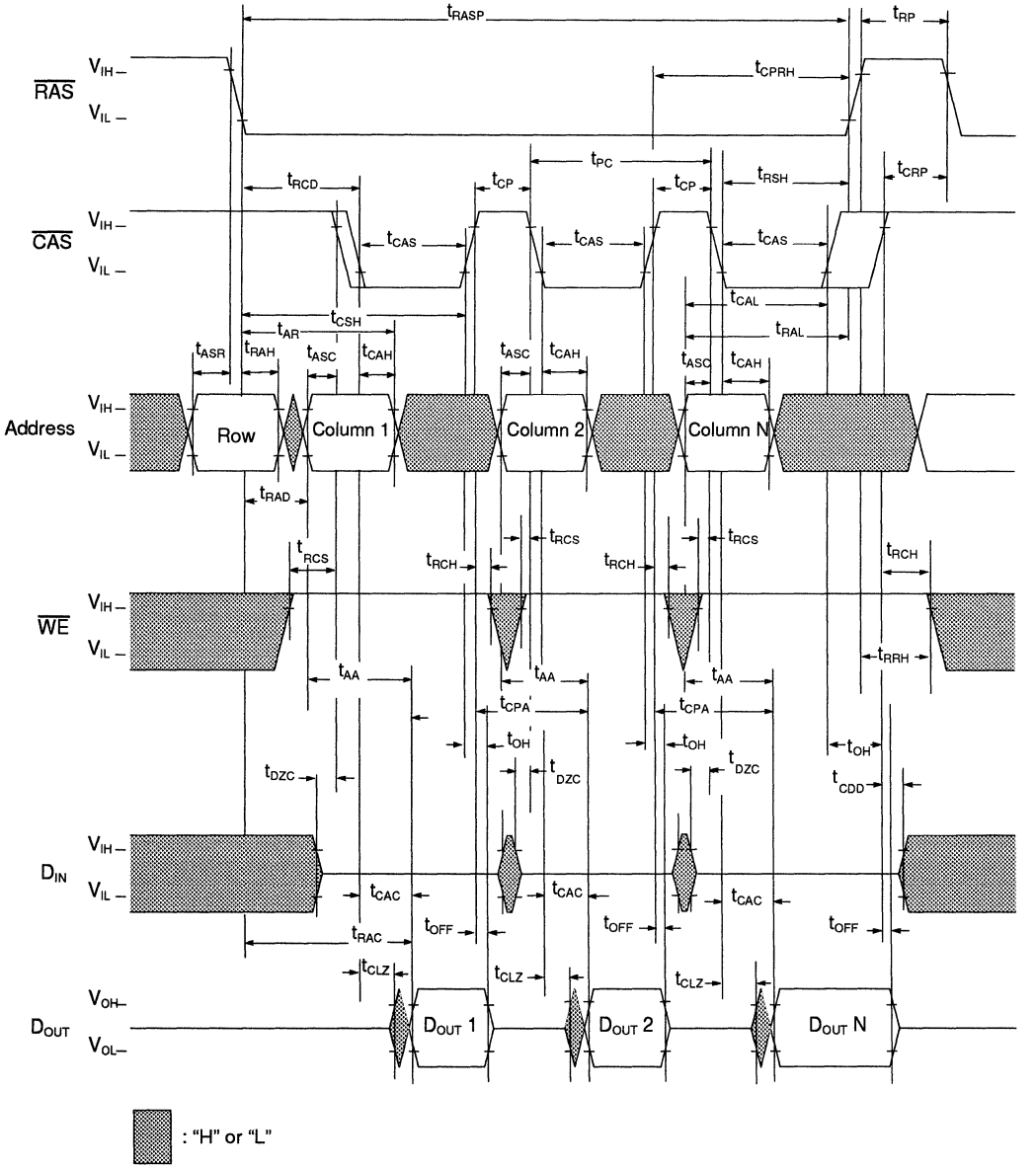
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRRH
tRCH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

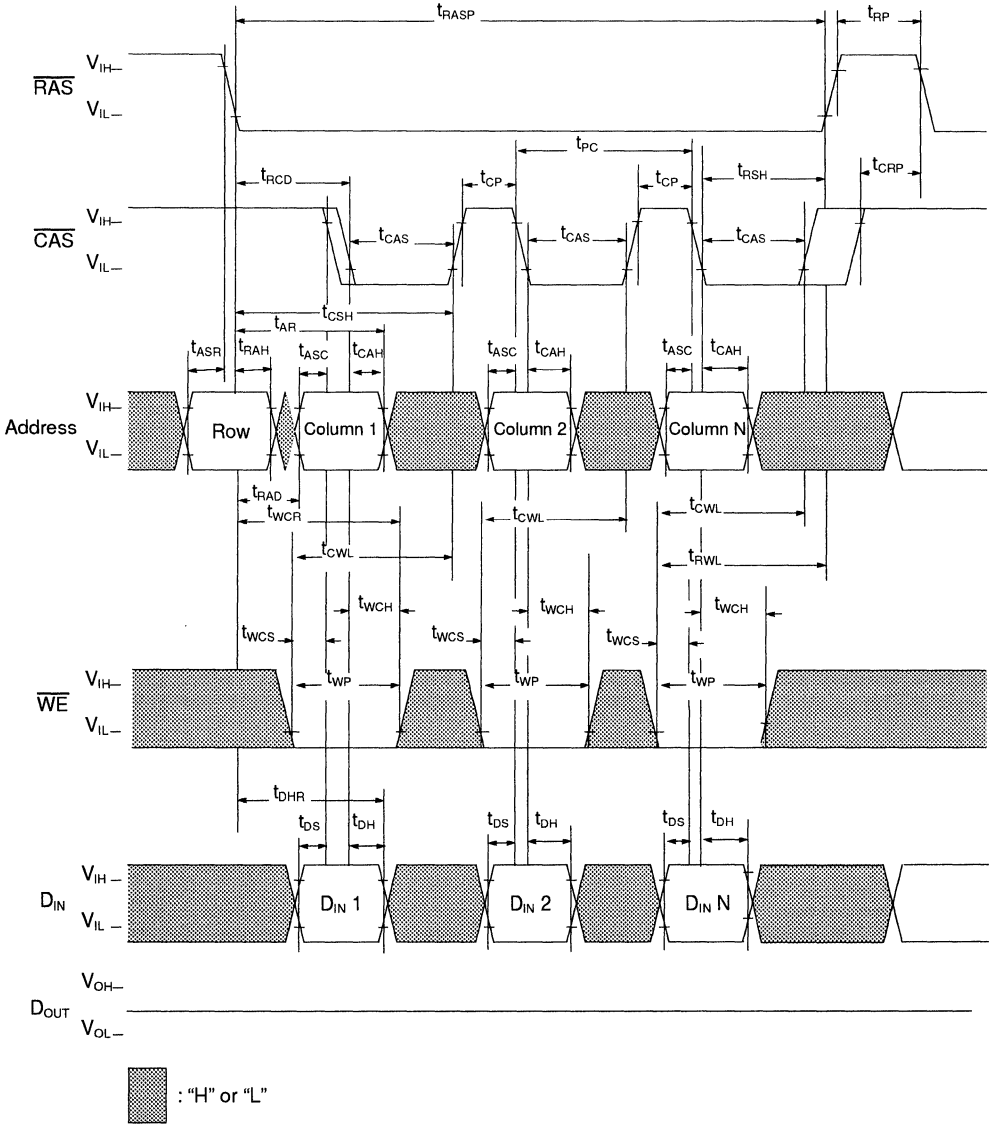
Write Cycle (Early Write)



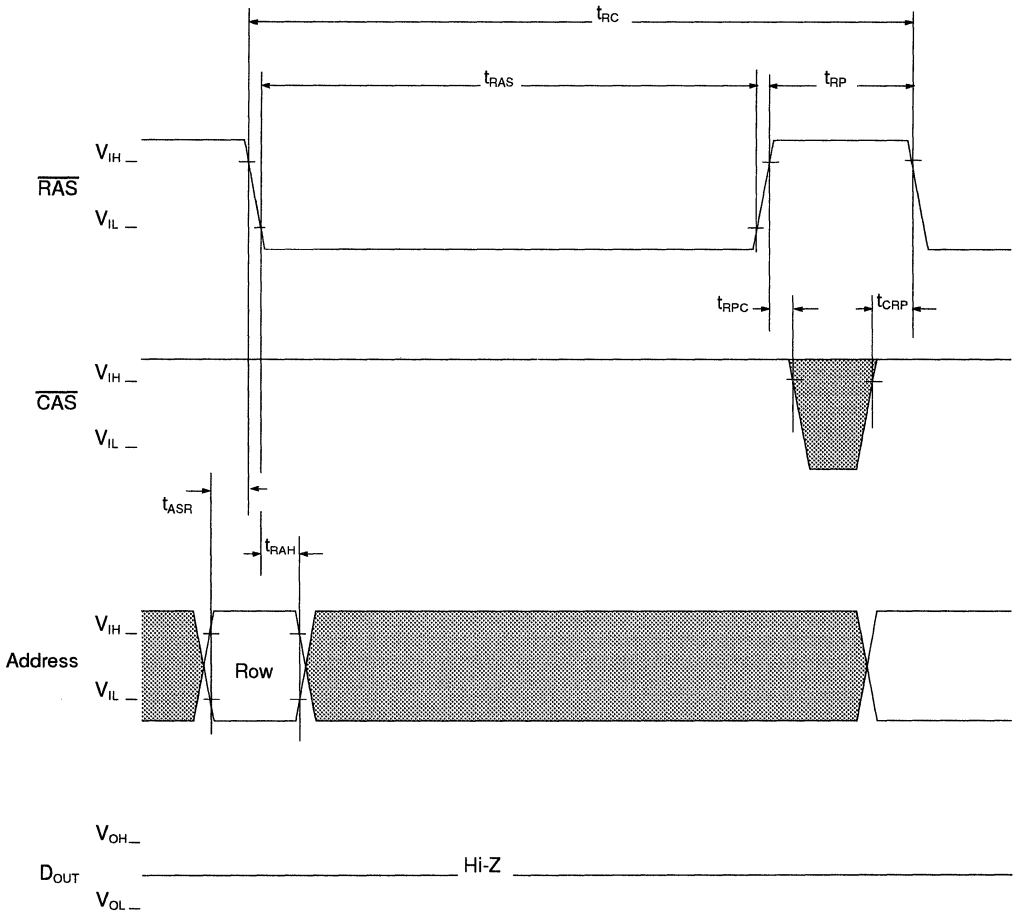
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

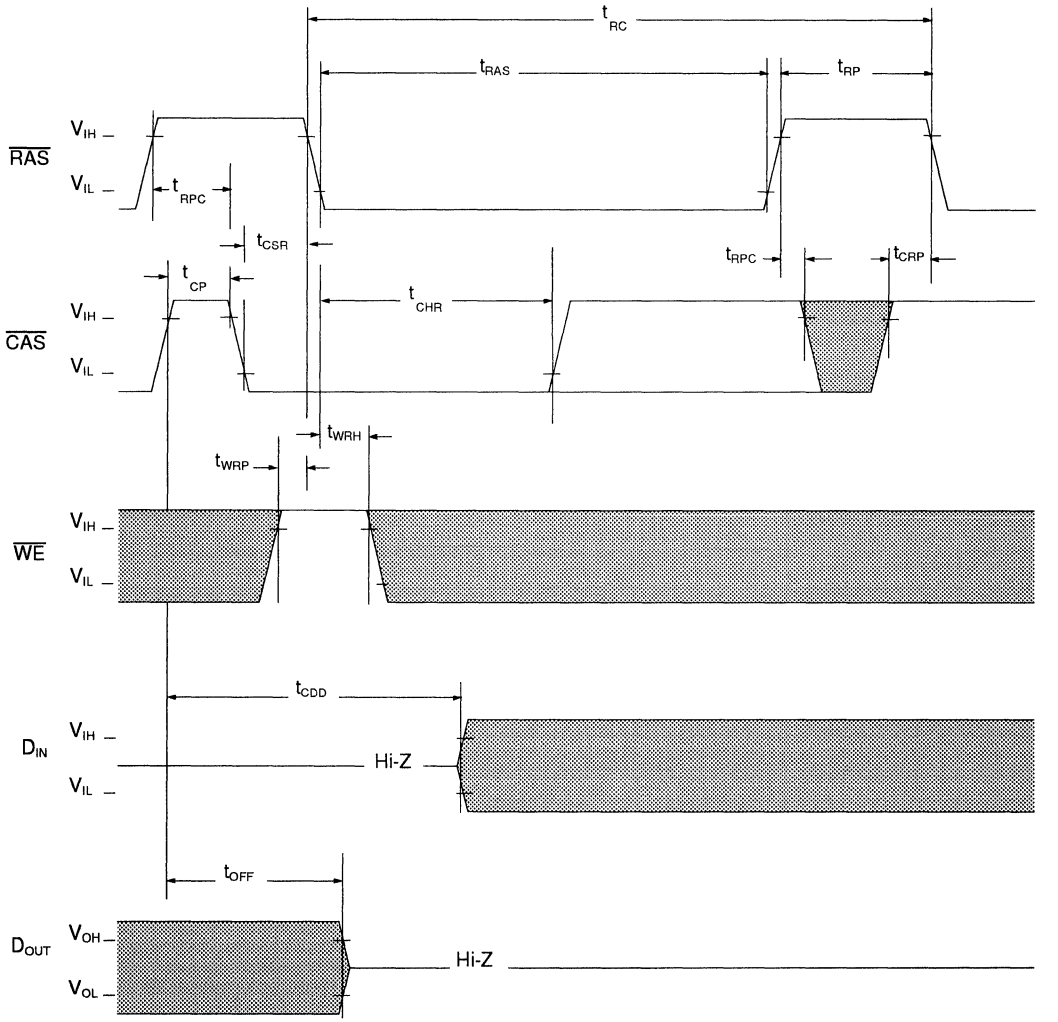


$\overline{\text{RAS}}$ Only Refresh Cycle



Note: $\overline{\text{WE}}$, D_{IN} are "H" or "L"

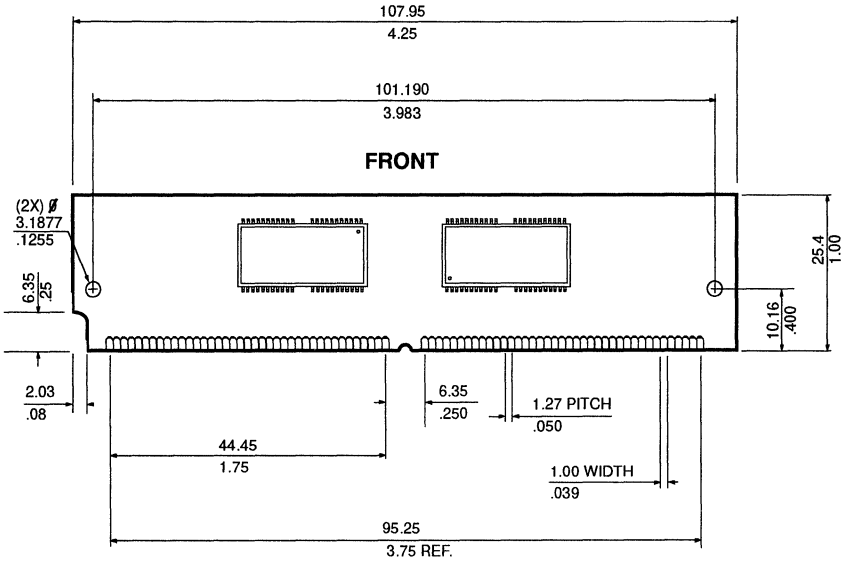
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

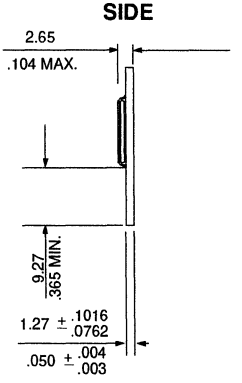


: "H" or "L"

Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 32 DRAM Module

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

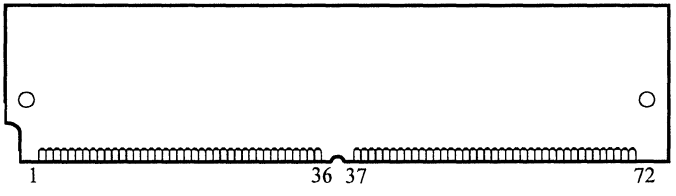
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au and Sn/Pb versions available

Description

The IBM11D2320BC is an 8MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 2Mx32 high speed memory array, and is configured as 2 1Mx32 banks - each independently selectable via unique $\overline{RAS}$ inputs. The assembly is intended for use in 16, 32 and 64 bit applications. It is manufactured with 16 1Mx4 devices, each in either a 350mil or 300mil package, and is compatible with the JEDEC 72-Pin SIMM standard.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 2Mx36 parity SIMM, IBM11D2360B, as well as other density offerings and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	V_{SS}	13	A1	25	DQ24	37	NC	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	NC	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ32	72	V_{SS}

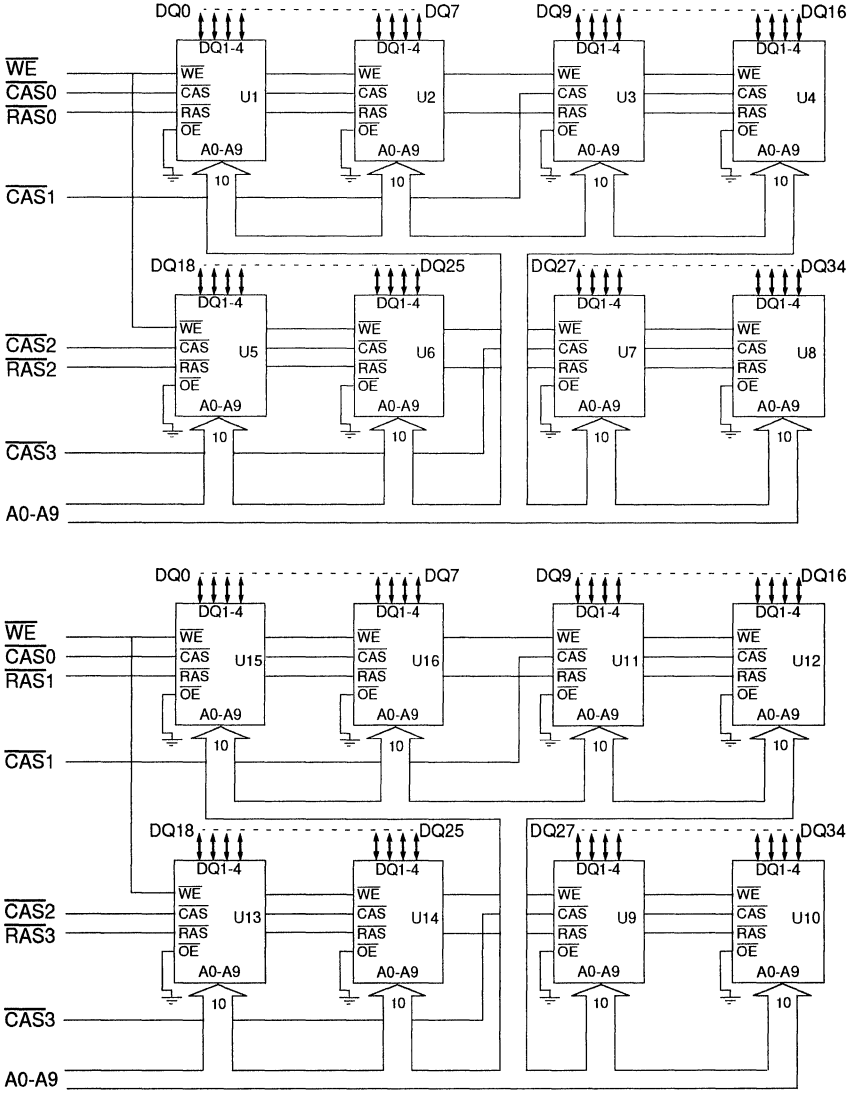
1. DQ numbering is compatible with parity (x36) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D2320BA-60	2M x 32	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D2320BA-70	2M x 32	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E2320BA-60	2M x 32	60ns	Au	4.25" x 1" x .360"	
IBM11E2320BA-70	2M x 32	70ns	Au	4.25" x 1" x .360"	
IBM11D2320BC-60	2M x 32	60ns	Sn/Pb	4.25" x 1" x .360"	1
IBM11D2320BC-70	2M x 32	70ns	Sn/Pb	4.25" x 1" x .360	1
IBM11E2320BC-60	2M x 32	60ns	Au	4.25" x 1" x .360	1
IBM11E2320BC-70	2M x 32	70ns	Au	4.25" x 1" x .360	1

1. 'C' revision replaces 'A' revision, all specifications are identical or improved. 'C' revision uses new raw card which is common with IBM11D2360E.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	NC	NC
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 6.5	V	1
V_{IN}	Input Voltage	-0.7 to V_{CC} + 0.7	V	1
V_{OUT}	Output Voltage	-0.7 to V_{CC} + 0.7	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	10.6	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	90	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	37	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	37	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	75	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	25	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	976	mA	1, 2, 3
		-70	—	880		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	32	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	976	mA	1, 3, 4
		-70	—	880		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	616	mA	1, 2, 3
		-70	—	566		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	32	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	976	mA	1, 3, 4
		-70	—	880		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$	-40	+40		
		All others	-160	+160		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -4mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for 1 bank..

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. The DRAM Outputs will remain disabled until these 8 cycles have occurred. This prevents data contention (excessive current) during power on. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	10	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	—	—	—	—	ns	3
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	45	—	50	—	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	10	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	10	—	15	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	10	0	15	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	2, 3

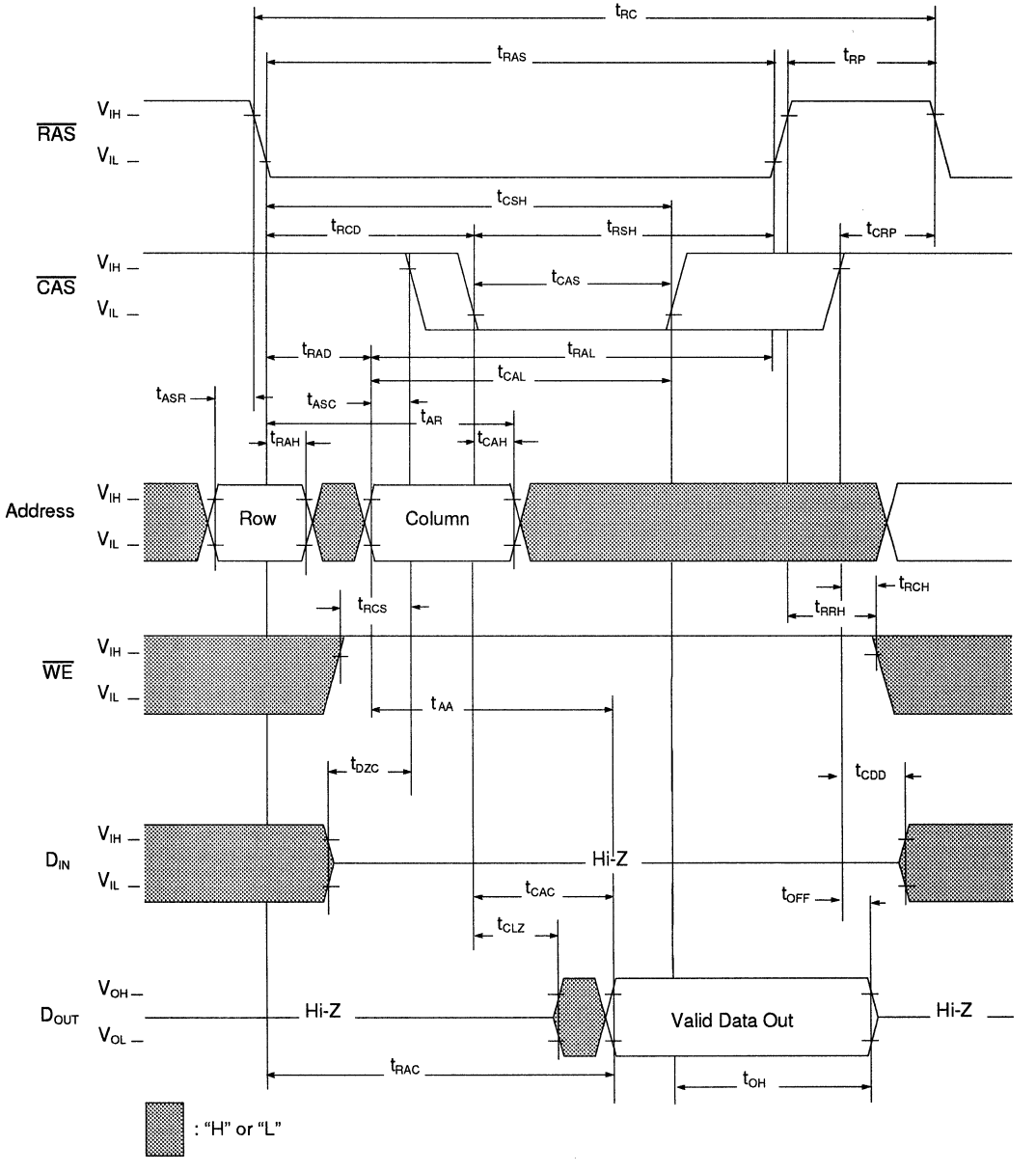
1. This timing parameter is not applicable to this product, but applies to a related product in this family.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Access time assumes a load of 100pF.

Refresh Cycle

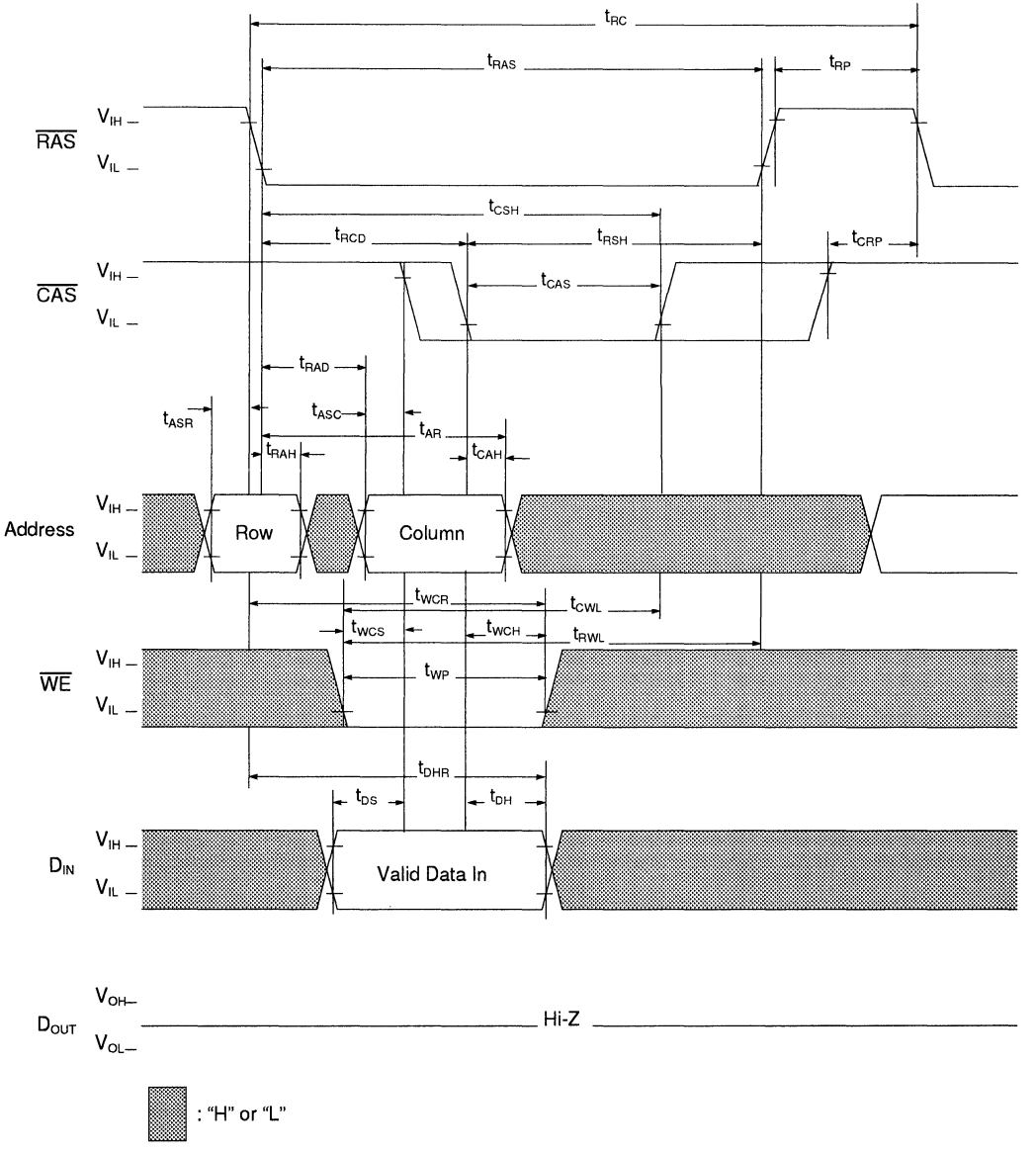
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	5	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms. The DC variation in the V_{CC} supply may not exceed 300mV within a refresh interval (16ms).

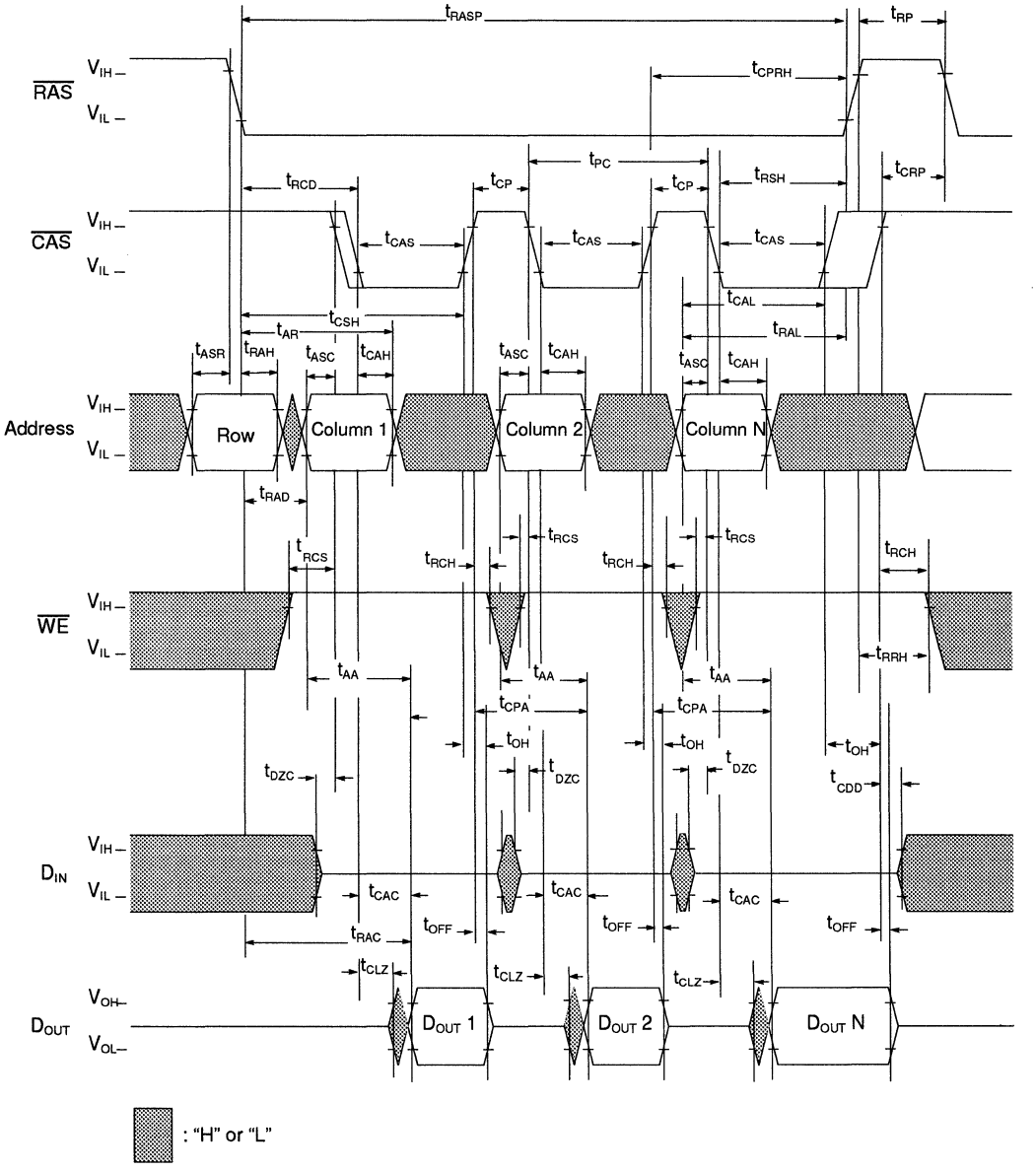
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRRH
tRCH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

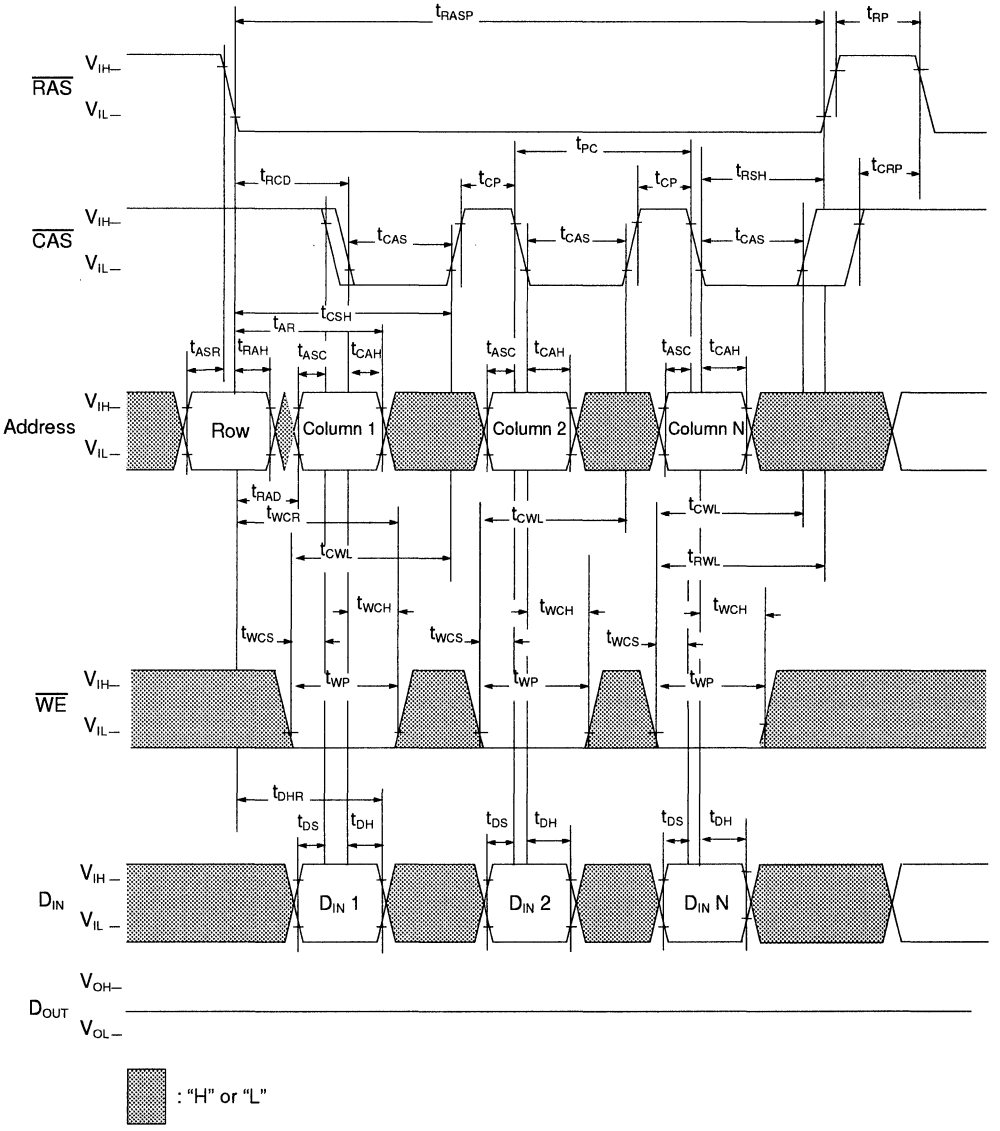
Write Cycle (Early Write)



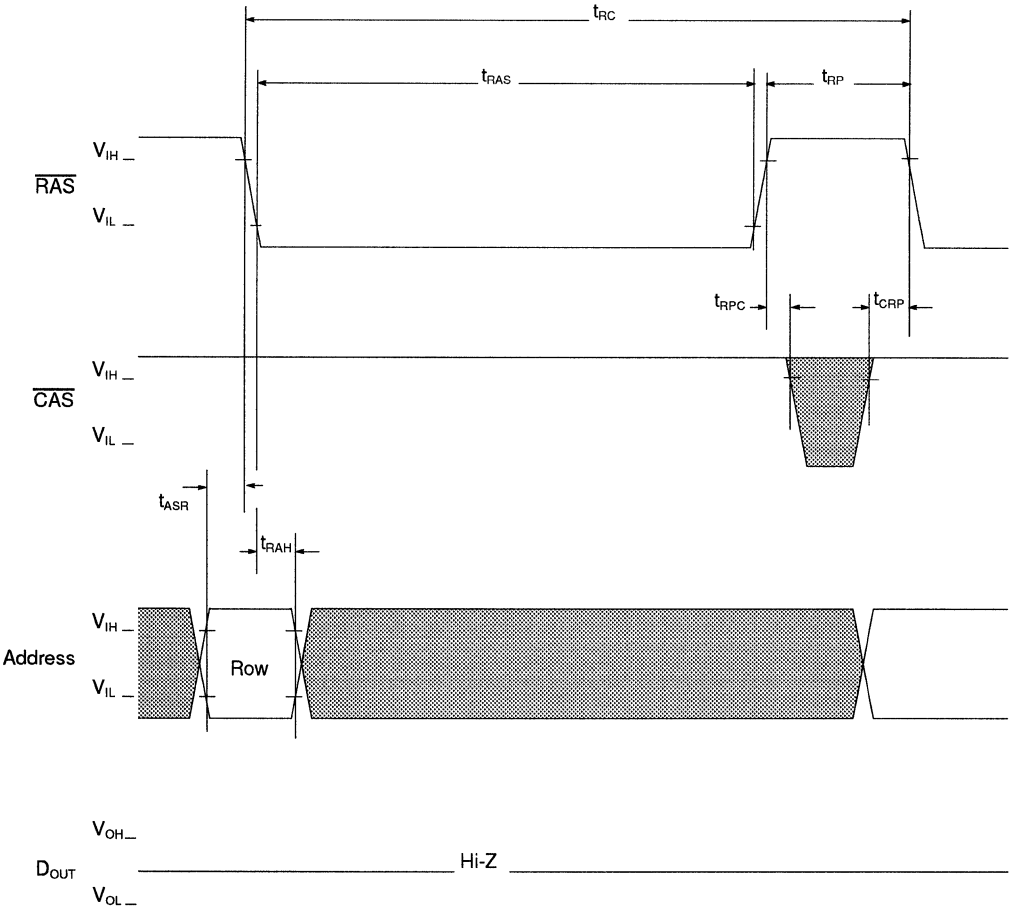
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

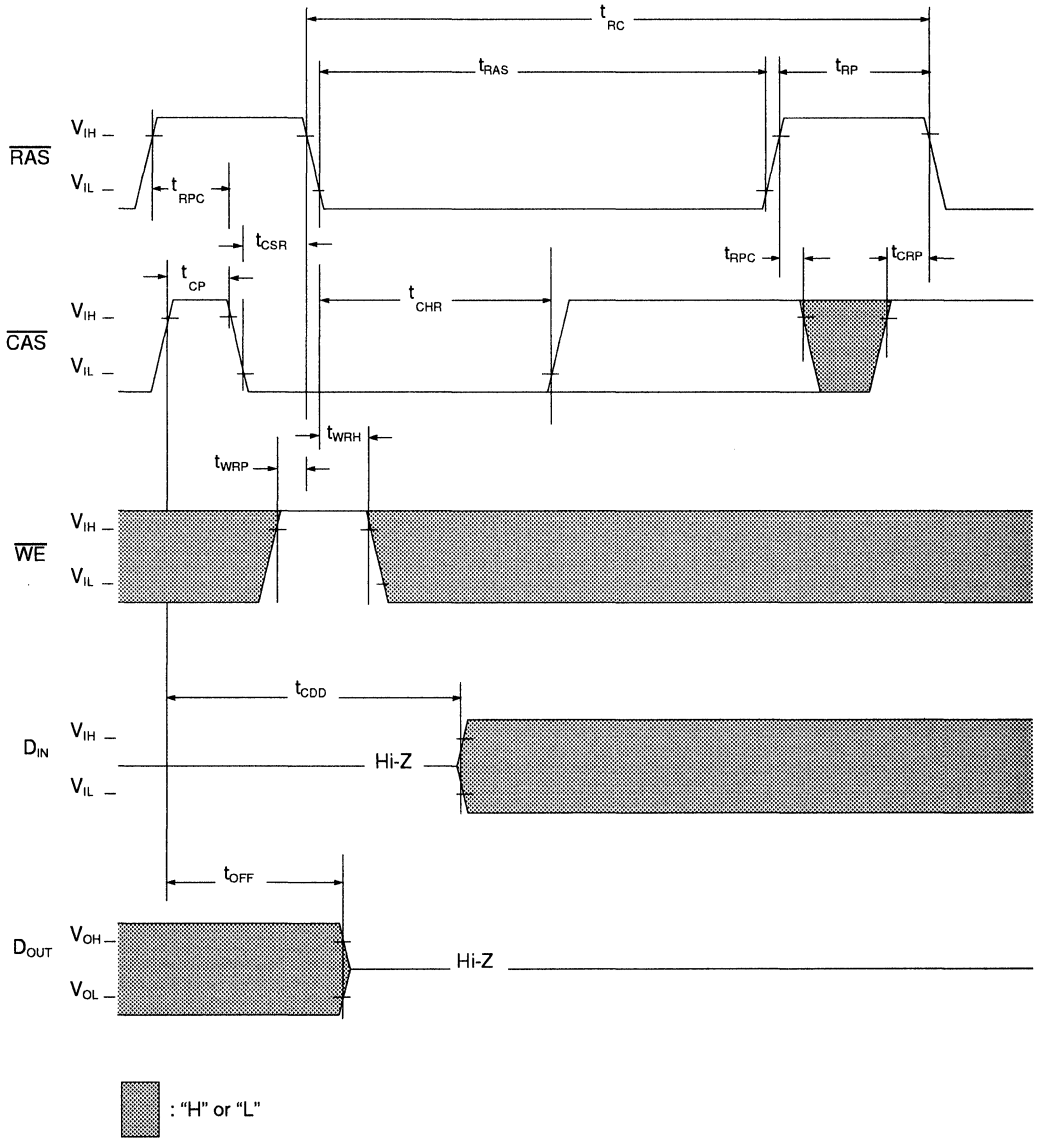


$\overline{RAS}$ Only Refresh Cycle



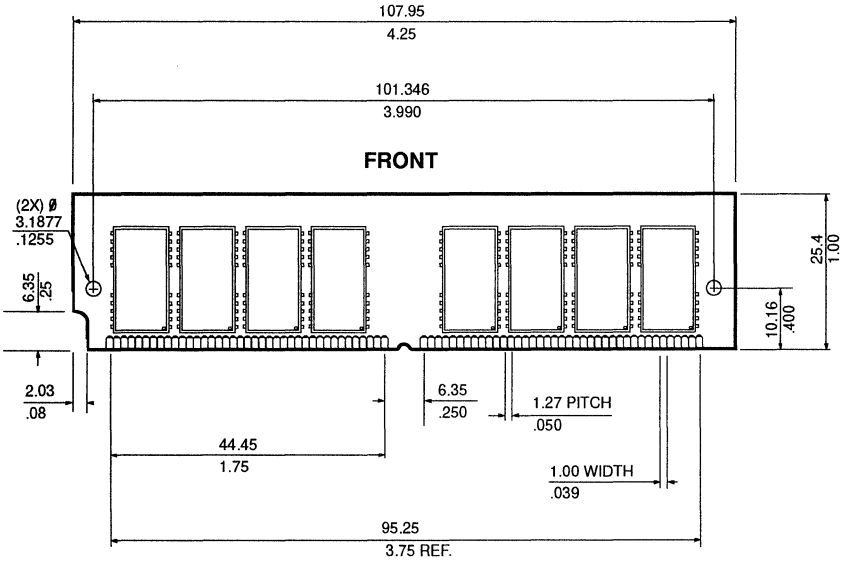
Note: $\overline{WE}$, D_{IN} are "H" or "L"

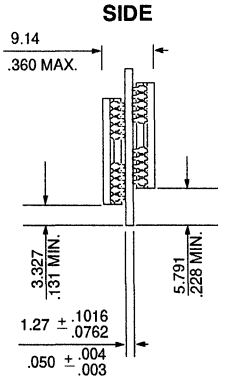
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing(IBM11D2320BC)





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 32 DRAM Module

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	18ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	40ns

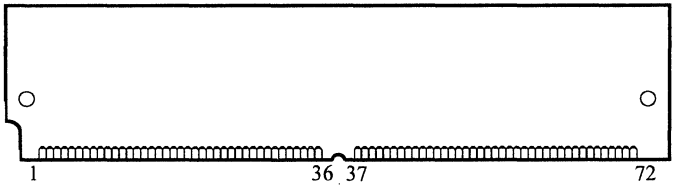
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- Low active current dissipation
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au and Sn/Pb versions available

Description

The IBM11D2320BD is an 8MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 2Mx32 high speed memory array, and is configured as 2 1Mx32 banks - each independently selectable via unique $\overline{RAS}$ inputs. The assembly is intended for use in 16, 32 and 64 bit applications. It is manufactured with 16 1Mx4 devices, each in a 300mil package, and is compatible with the JEDEC 72-Pin SIMM standard.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 2Mx36 parity SIMM, IBM11D2360B, as well as other density offerings and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

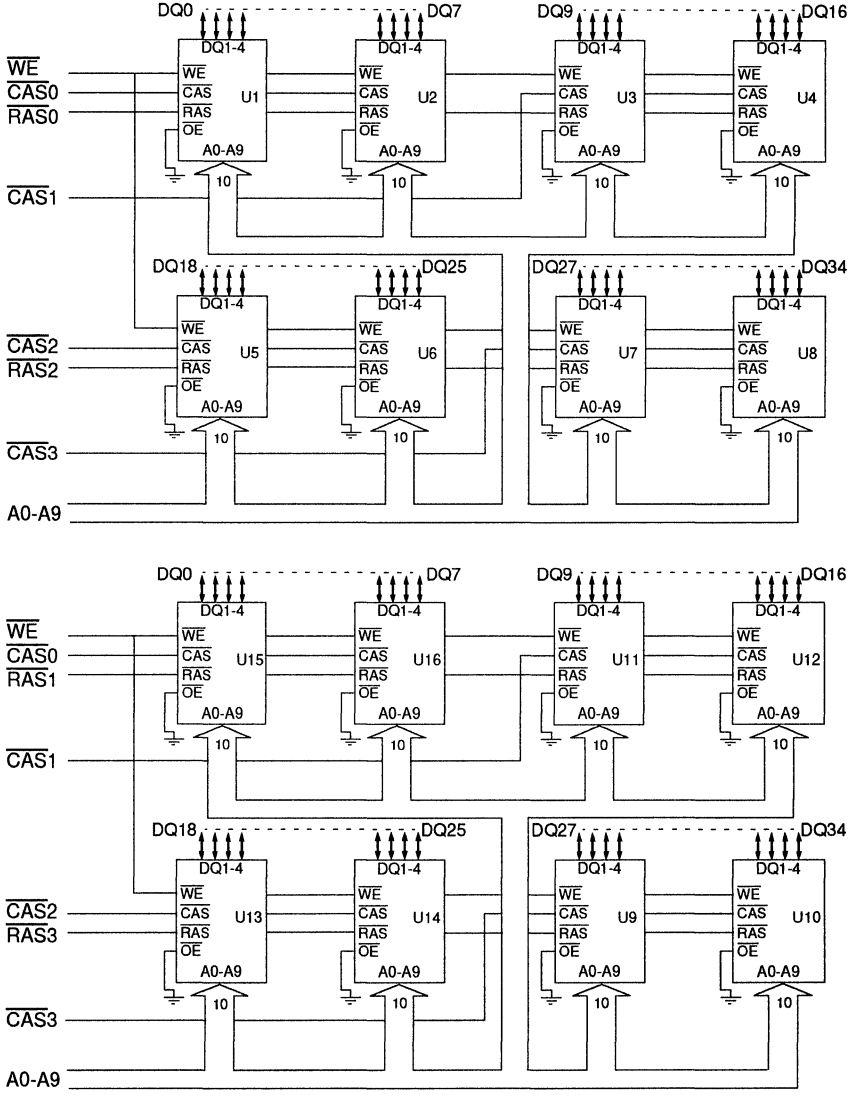
Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	V_{SS}	13	A1	25	DQ24	37	NC	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	NC	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with parity (x36) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D2320BD-60	2M x 32	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D2320BD-70	2M x 32	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E2320BD-60	2M x 32	60ns	Au	4.25" x 1" x .360"	
IBM11E2320BD-70	2M x 32	70ns	Au	4.25" x 1" x .360"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	NC	NC
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to + 6.0	V	1
V_{IN}	Input Voltage	-1.0 to + 6.0	V	1
V_{OUT}	Output Voltage	-1.0 to + 6.0	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	7.5	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	100	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	40	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	40	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	127	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	25	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	696	mA	1, 2, 3
		-70	—	576		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	32	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	696	mA	1, 3, 4
		-70	—	576		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	496	mA	1, 2, 3
		-70	—	416		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	16	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	696	mA	1, 3, 4
		-70	—	576		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$	-40	+40		
		All others	-160	+160		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for 1 bank.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	18	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	52	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	18	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	18	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	18	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	18	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	40	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

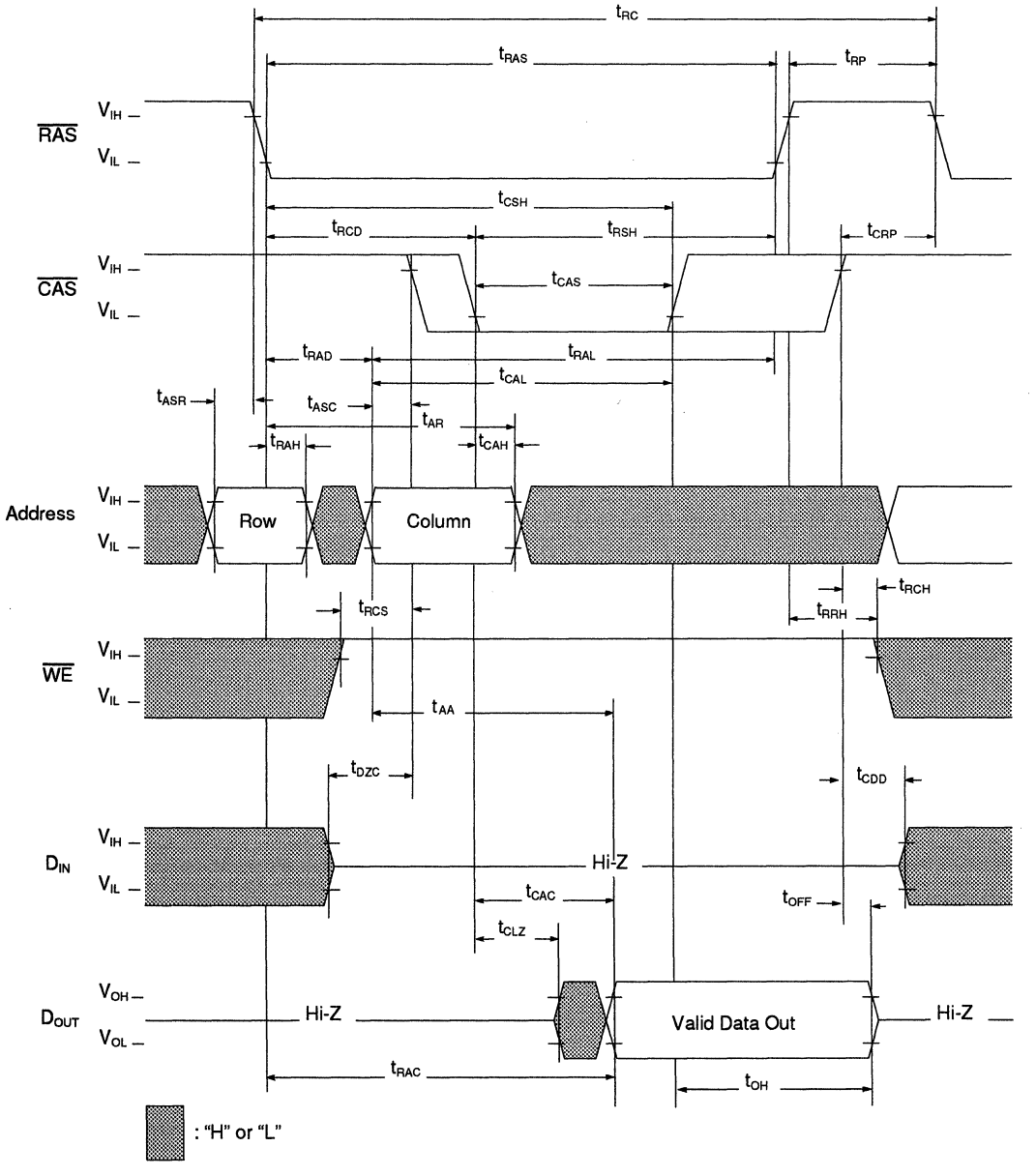
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

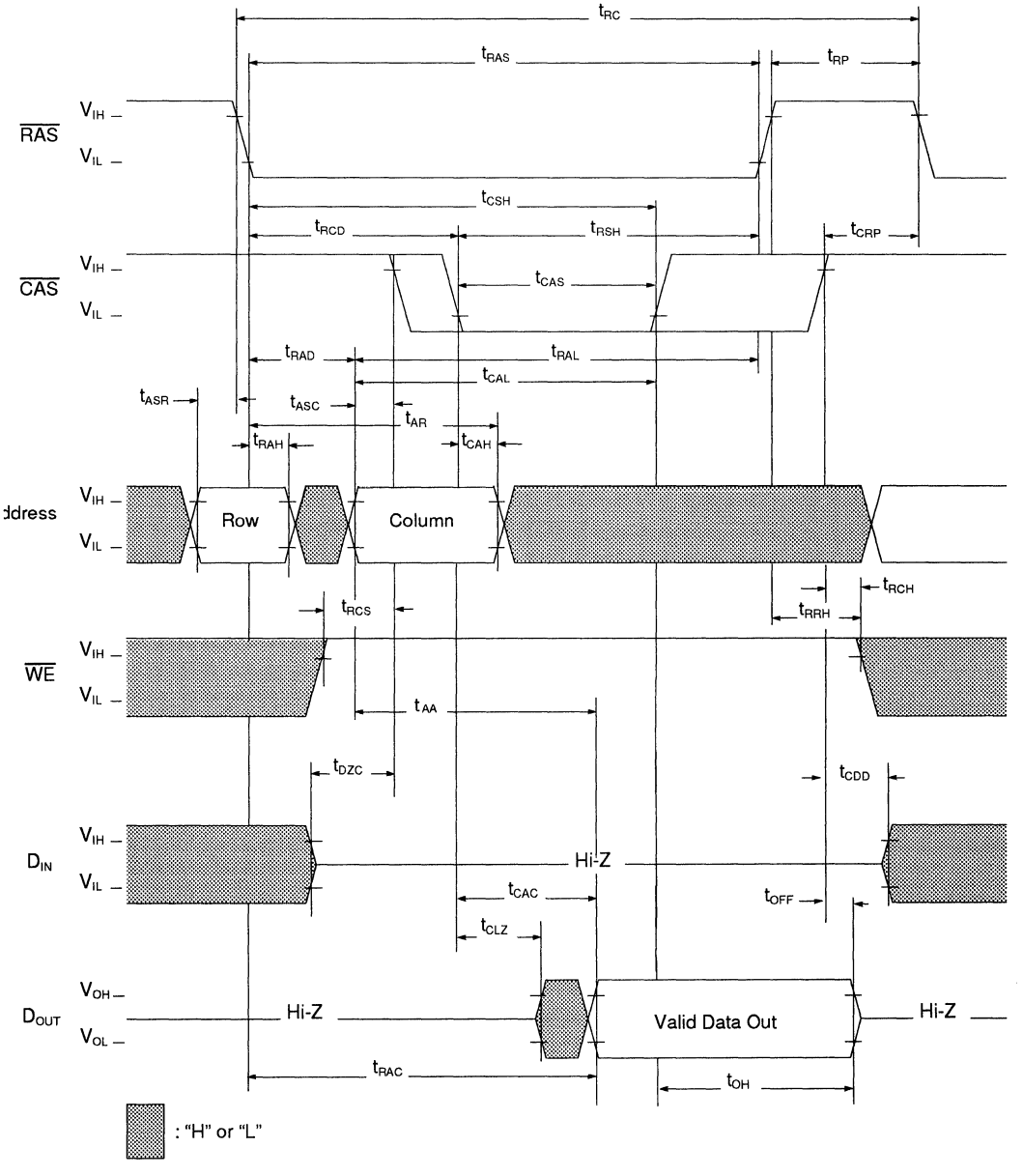
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms.

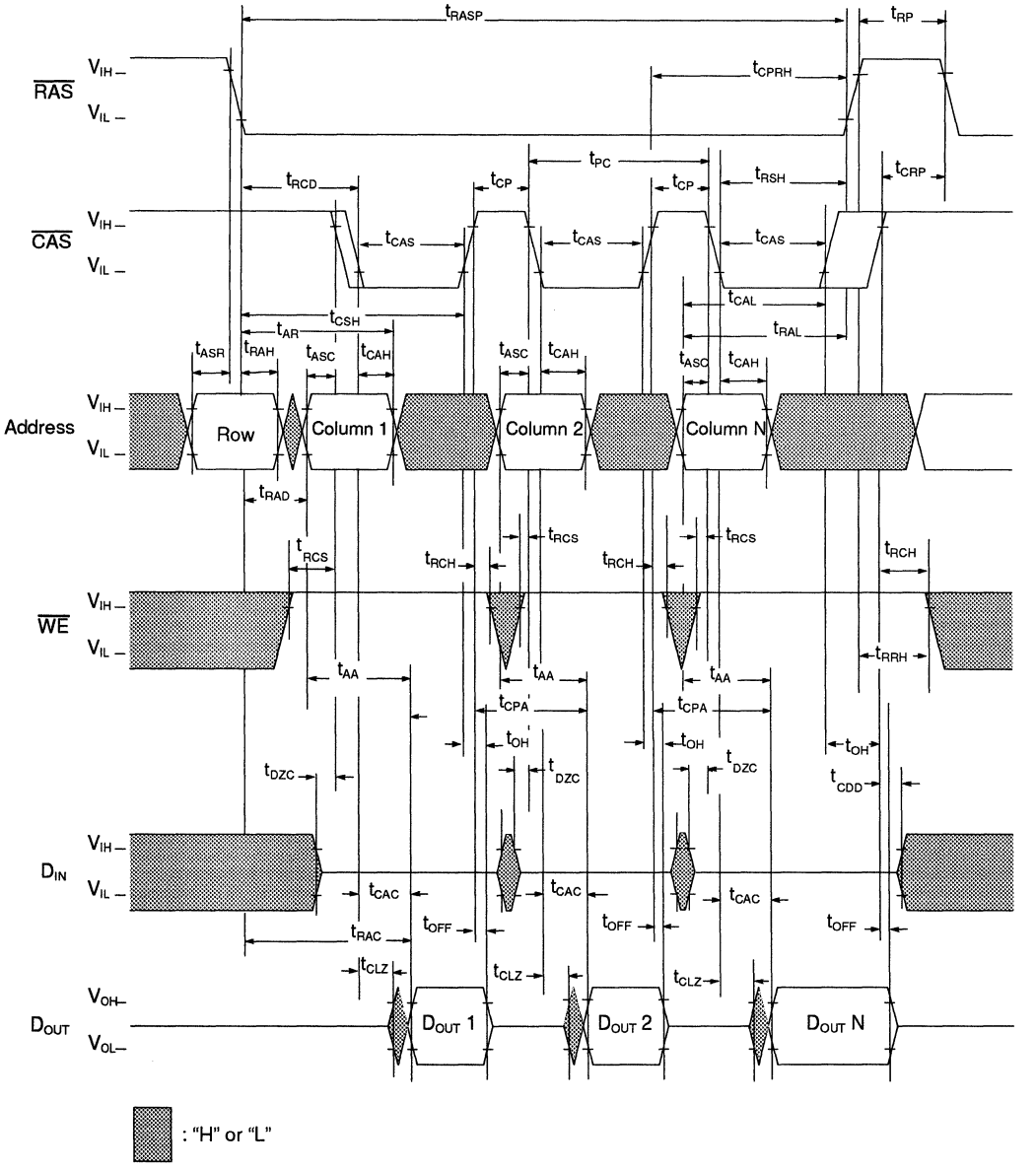
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

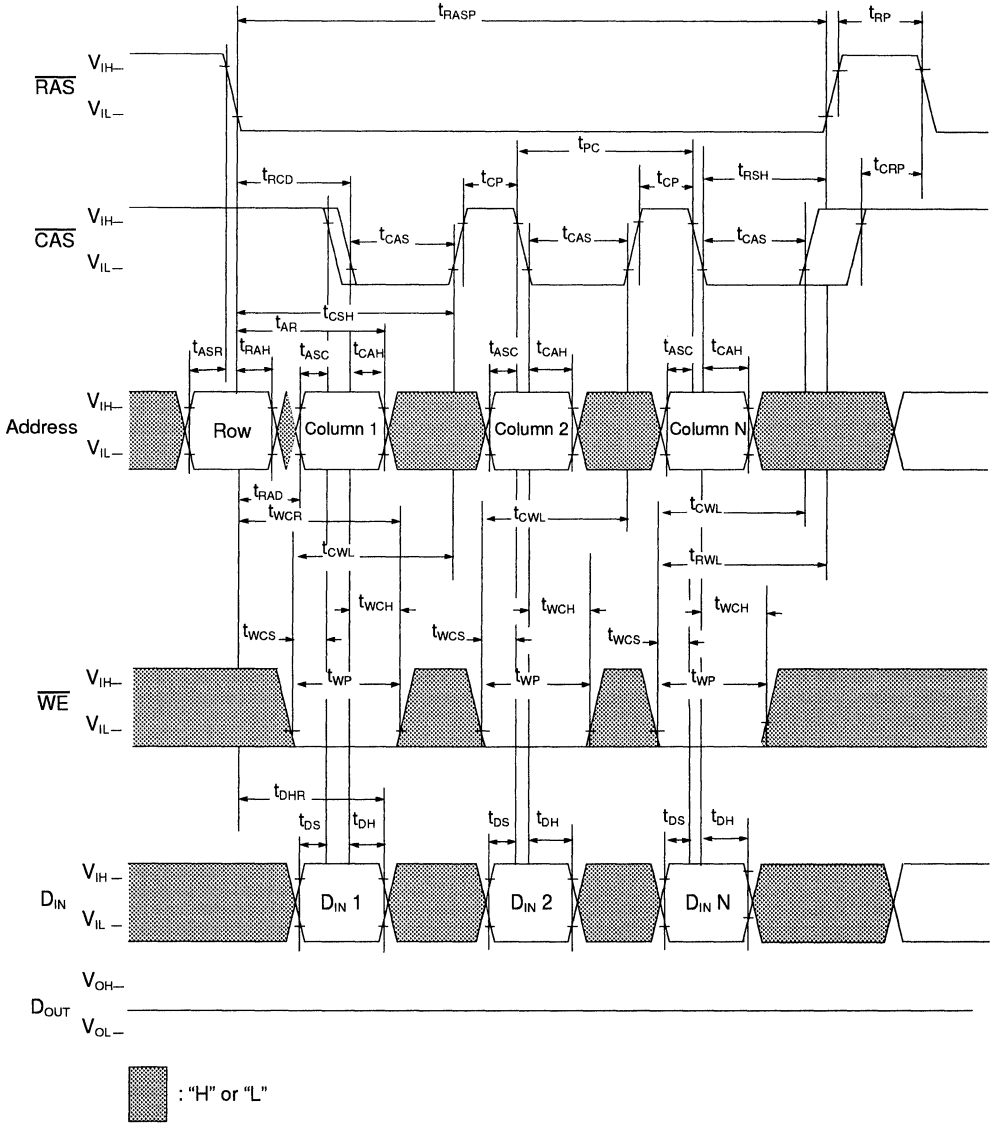
Write Cycle (Early Write)



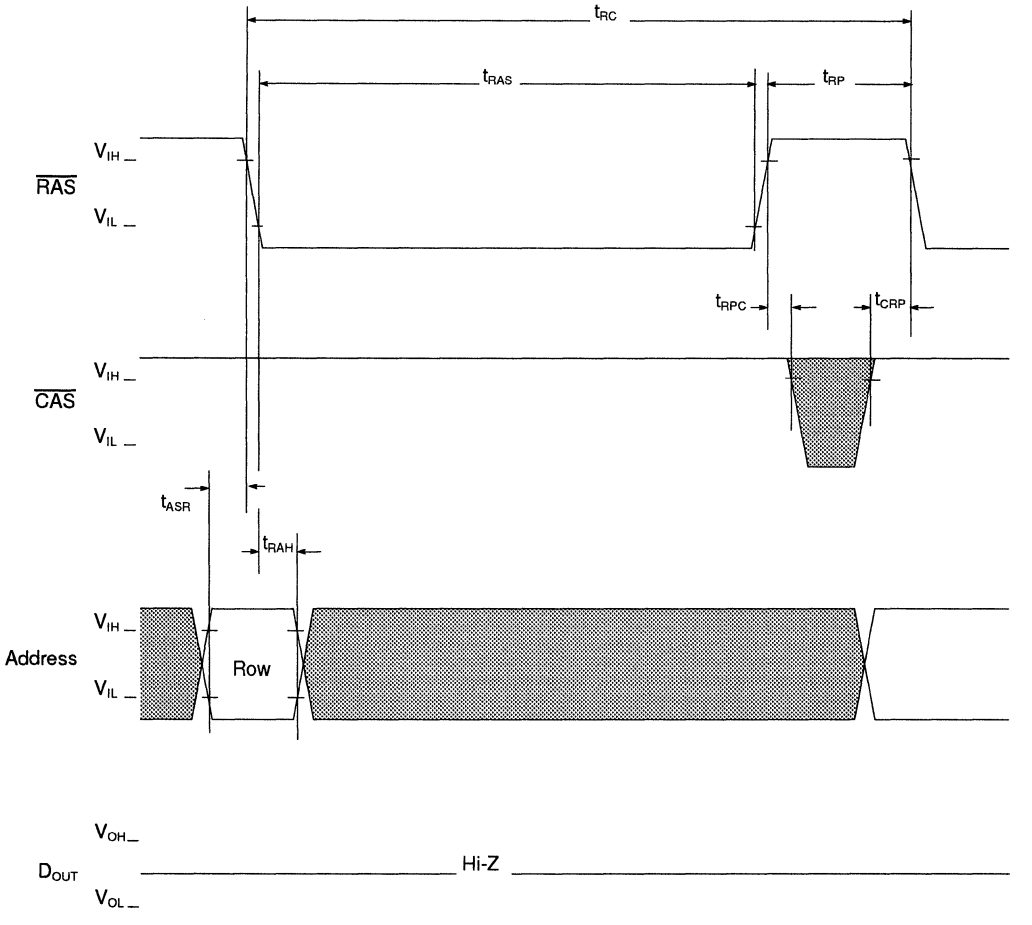
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



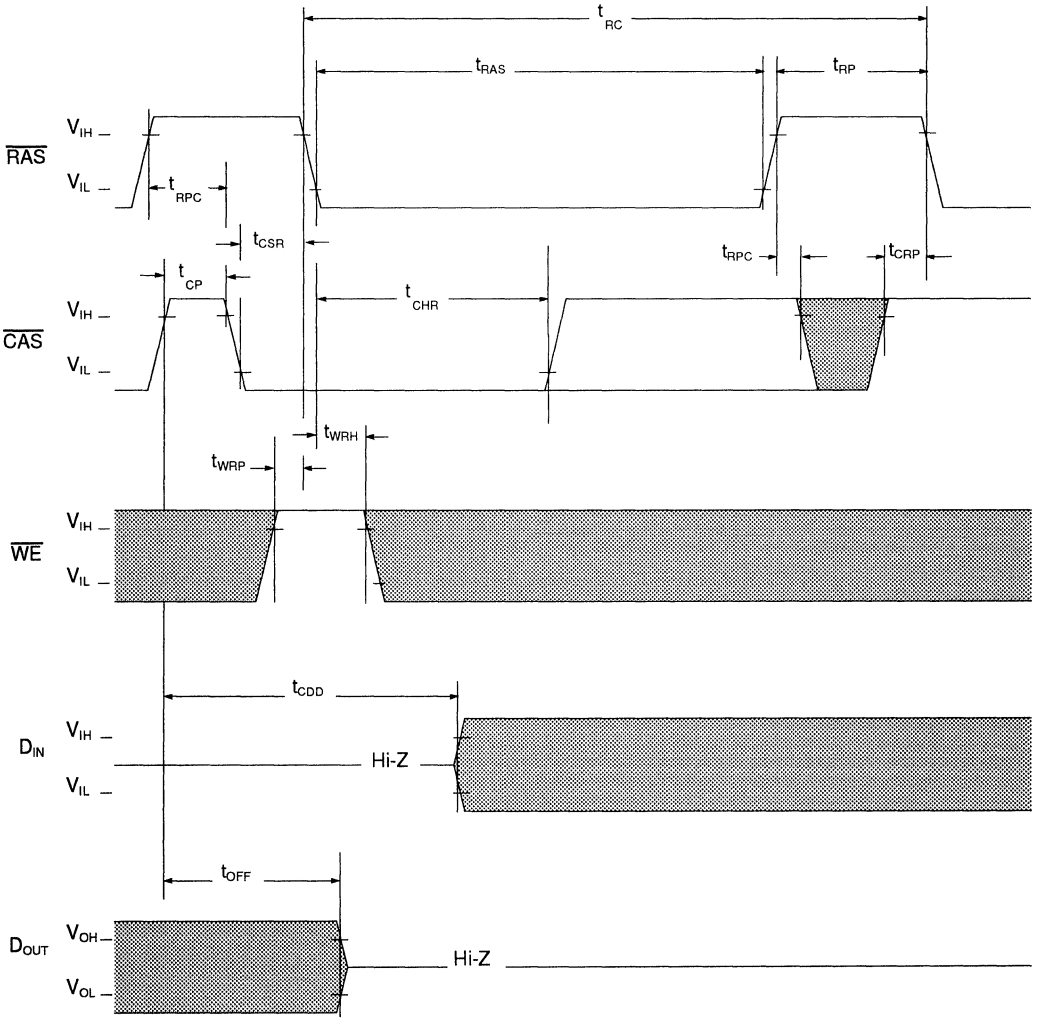
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

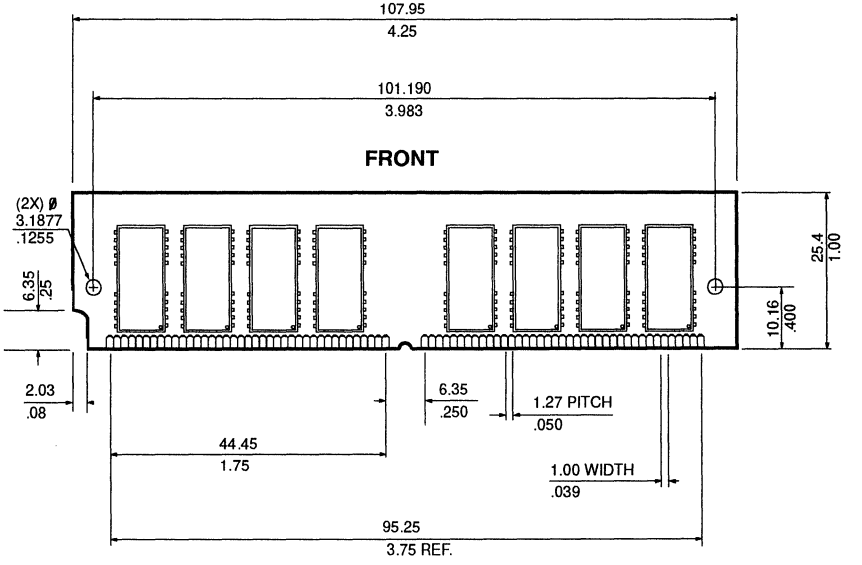
Note: $\overline{WE}$, D_{IN} are "H" or "L"

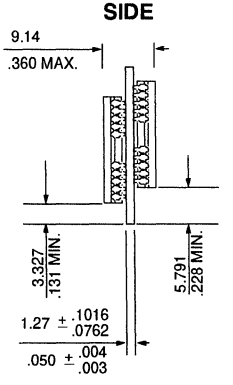
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 32 DRAM Module

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Manufactured with 16Mb DRAMS (1M x 16)
- Single 5V, ± 0.5V Power Supply
- Low current consumption
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au and Sn/Pb versions available

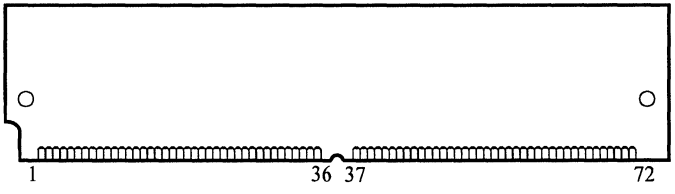
Description

The IBM11D2320L is an 8MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 2Mx32 high speed memory array, and is configured as 2 1Mx32 banks - each independently selectable via unique $\overline{RAS}$ inputs. The assembly is intended for use in 16, 32 and 64 bit applications. It is manufactured with 4 1Mx16 devices, each in a 400mil TSOP package, and is compatible with the JEDEC 72-Pin SIMM standard.

This assembly is intended as a direct replacement for 1Mx4-based SIMMs, while significantly reducing power dissipation. The use of TSOP packages allows tighter SIMM spacing (.3" on center). Input loading is consistent with 4Mb-based assemblies due to the addition of discrete capacitors maximizing compatibility at the system-level.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 2Mx32 non-parity SIMM, IBM11D2320B, as well as other density, parity and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

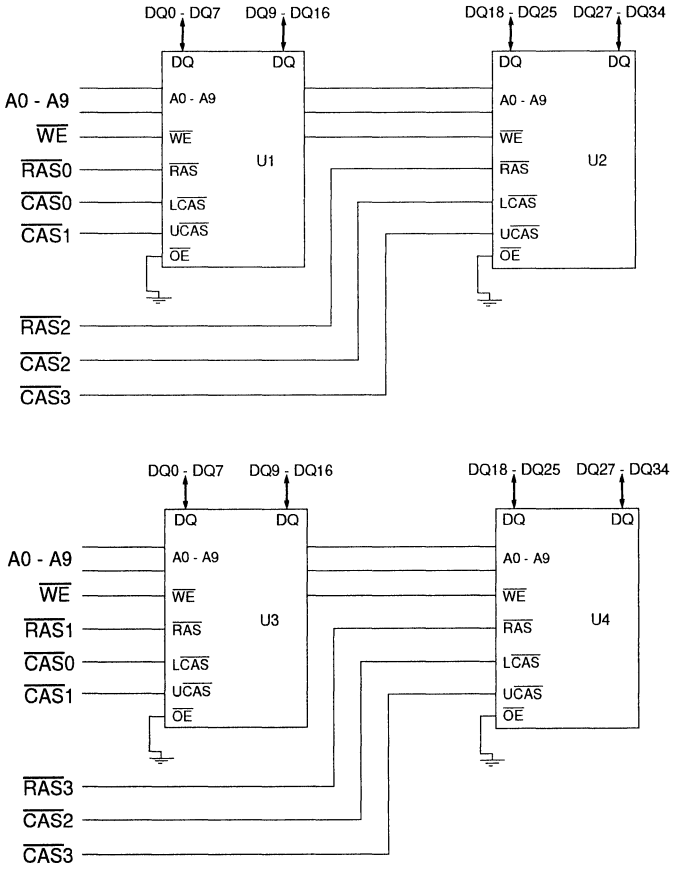
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	NC	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	NC	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with parity (x36) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D2320LA-60	2M x 32	60ns	Sn/Pb	4.25" x 1" x .154"	
IBM11D2320LA-70	2M x 32	70ns	Sn/Pb	4.25" x 1" x .154"	
IBM11E2320LA-60	2M x 32	60ns	Au	4.25" x 1" x .154"	
IBM11E2320LA-70	2M x 32	70ns	Au	4.25" x 1" x .154"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	NC	NC
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	4.3	W	1,2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	90	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	44	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	47	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	94	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	25	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	394	mA	1, 2, 3
		-70	—	344		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	8	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	394	mA	1, 3, 4
		-70	—	344		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	184	mA	1, 2, 3
		-70	—	164		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	4	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	394	mA	1, 3, 4
		-70	—	344		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-10	+10	µA	
		$\overline{CAS}$	-10	+10		
		All others	-40	+40		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. Refresh current is specified for 1 bank.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

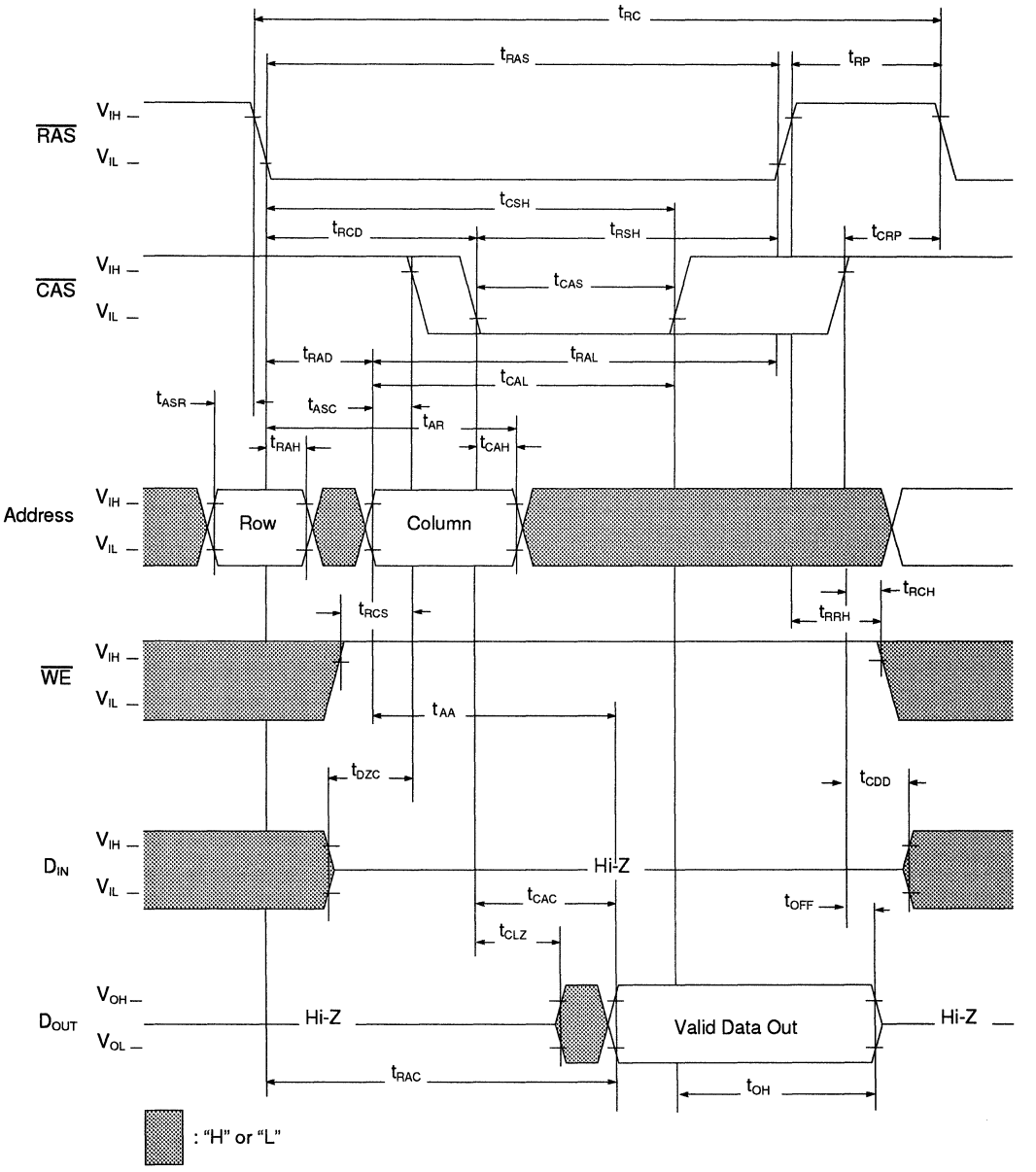
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

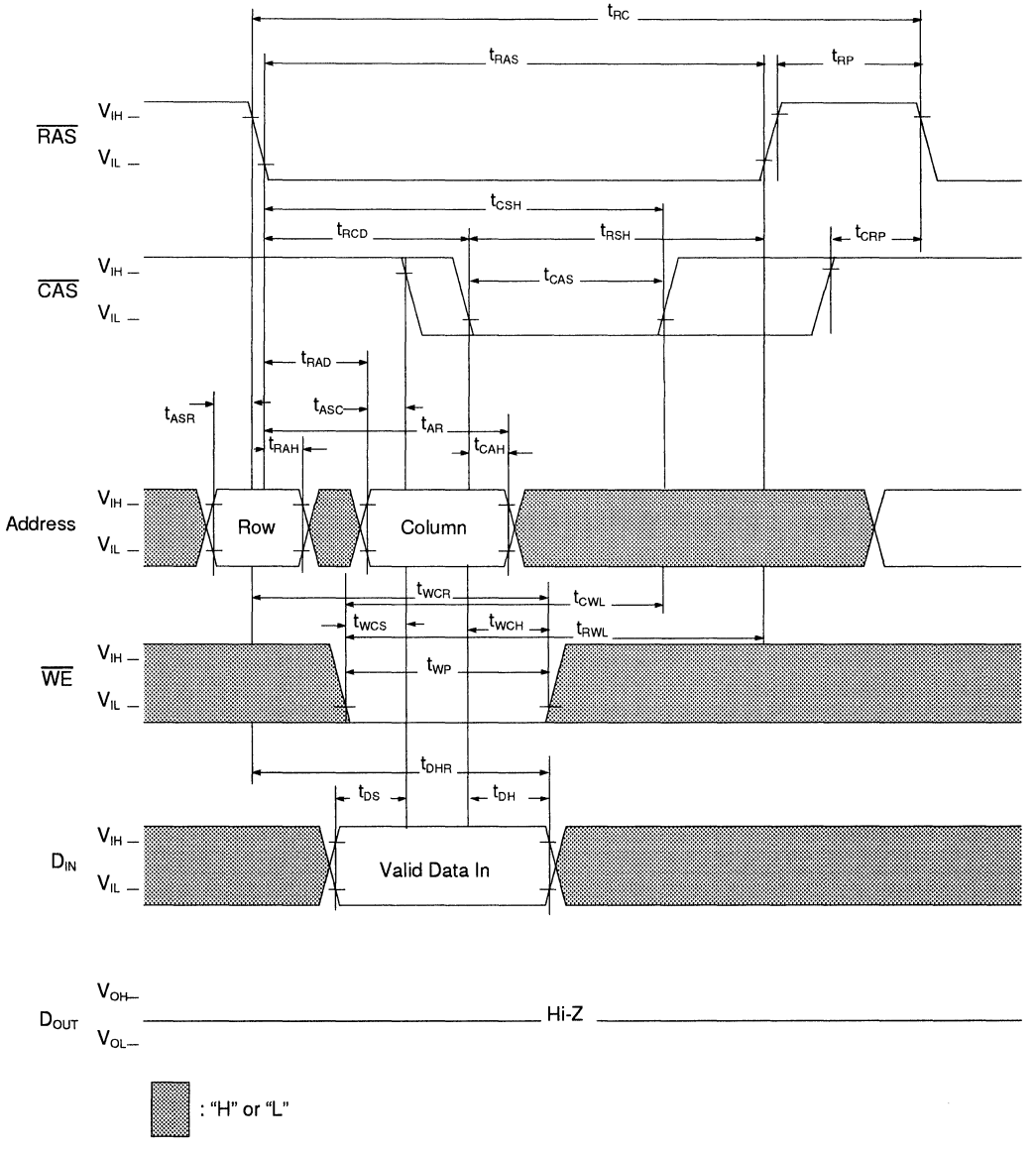
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms.

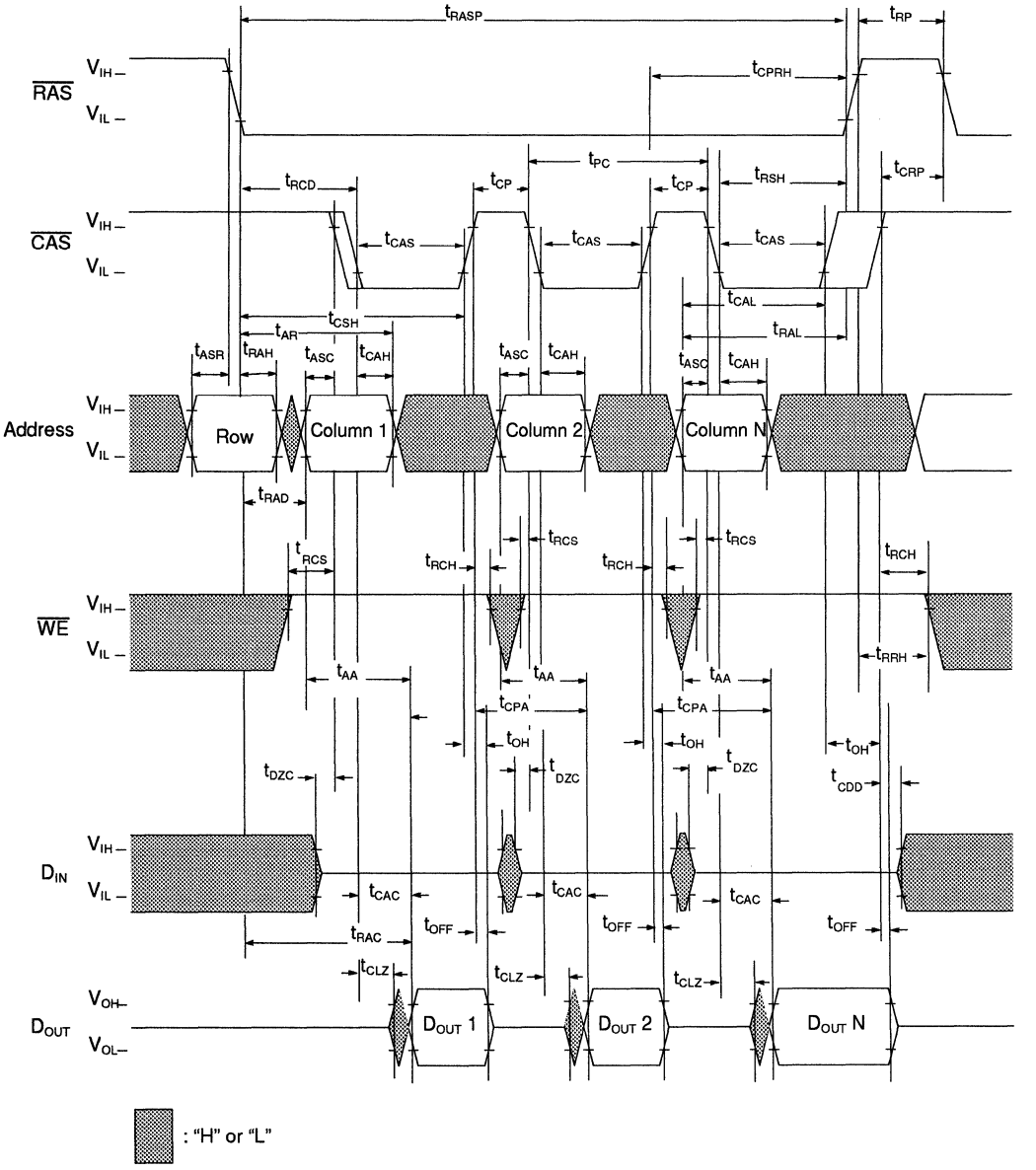
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

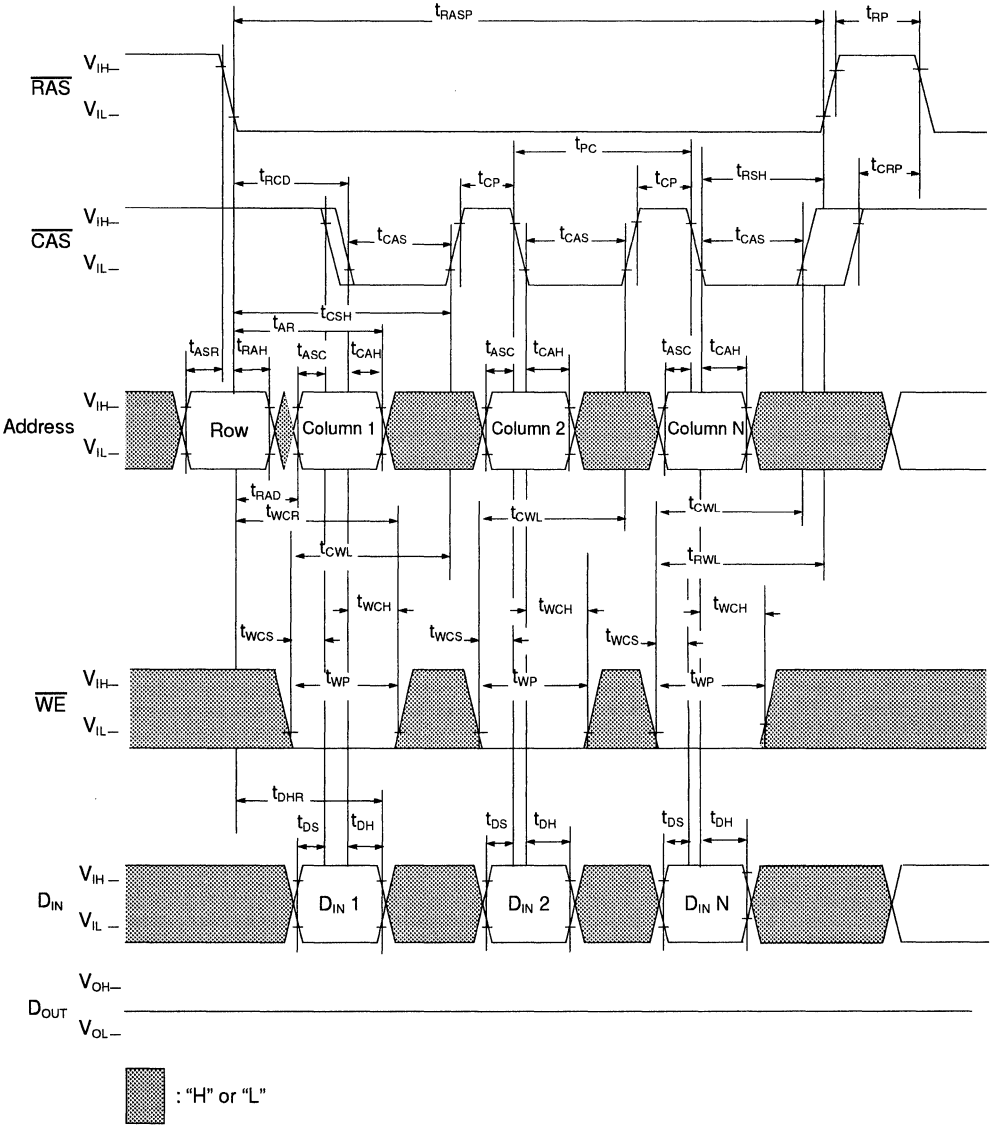
Write Cycle (Early Write)



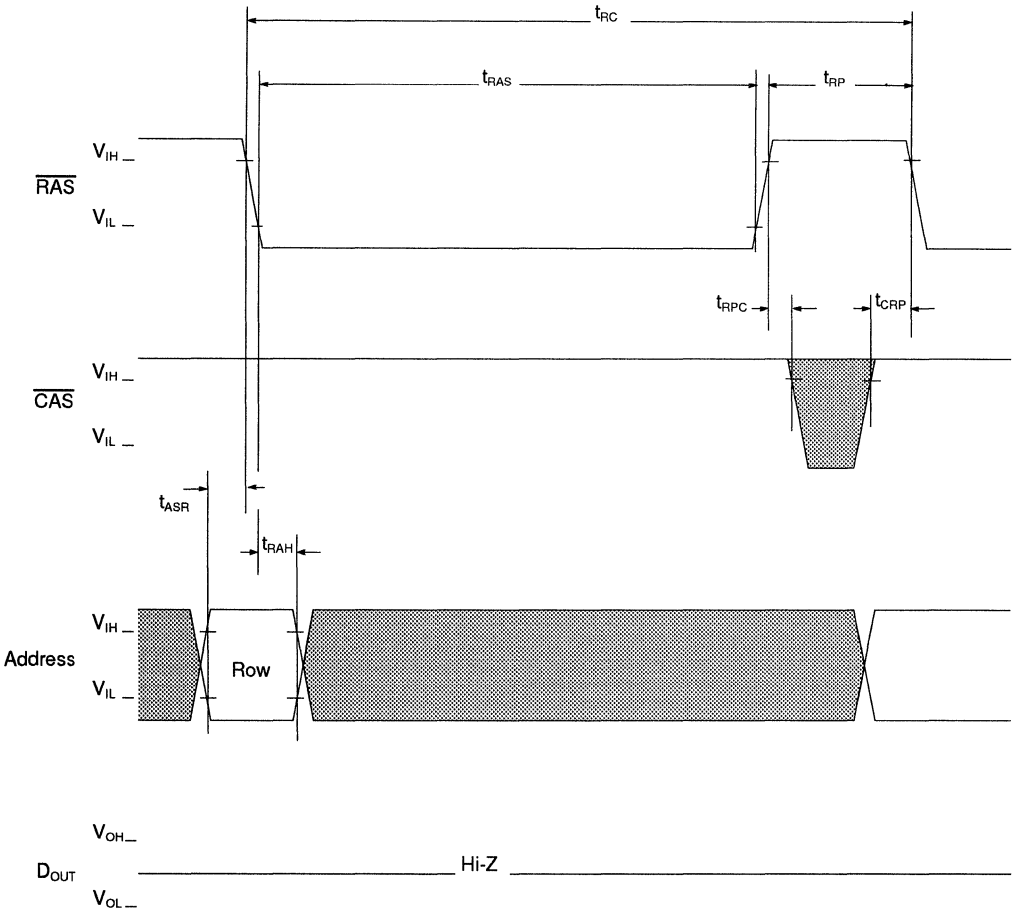
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



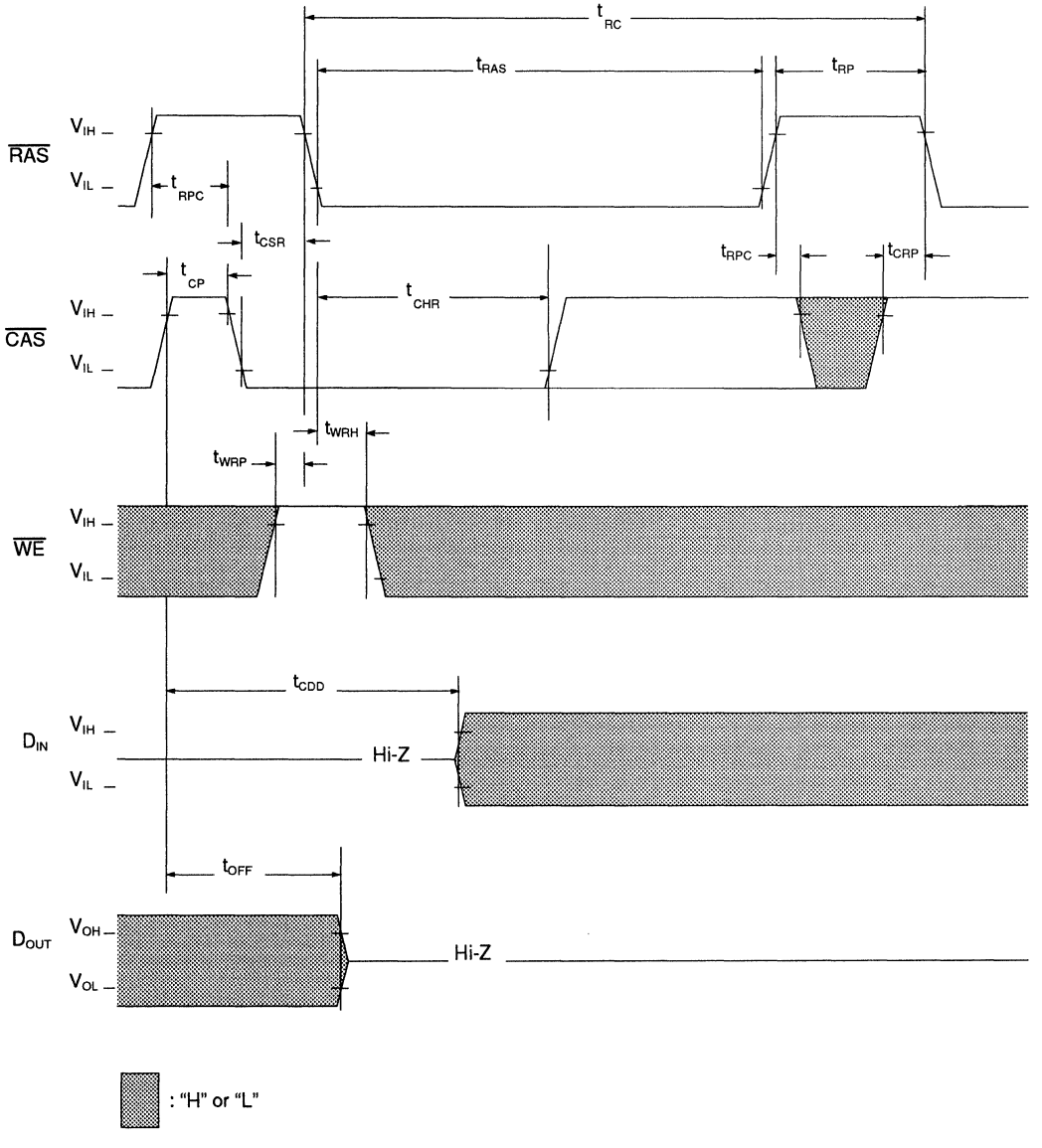
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

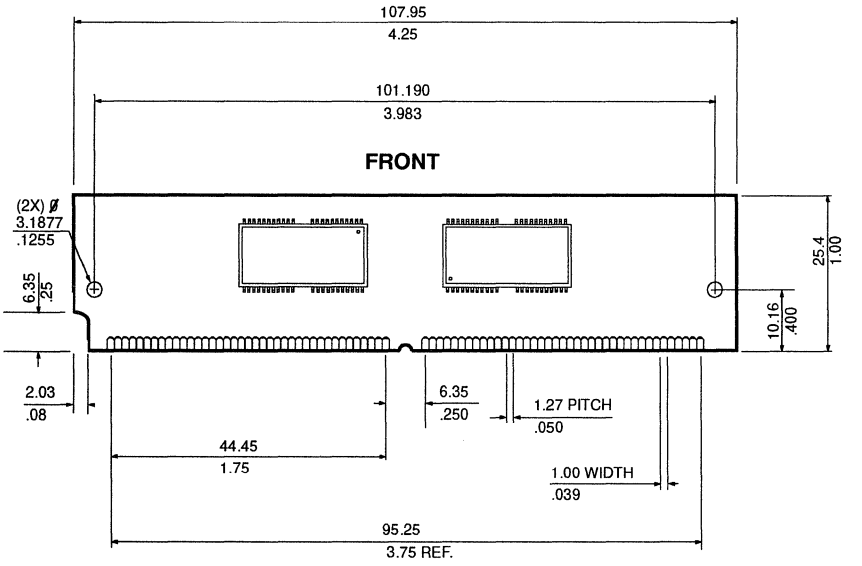
Note: $\overline{WE}$, D_{IN} are "H" or "L"

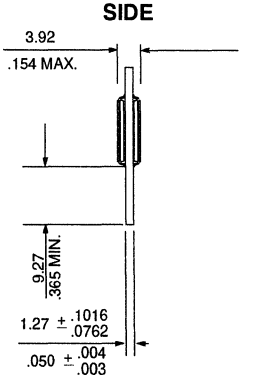
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

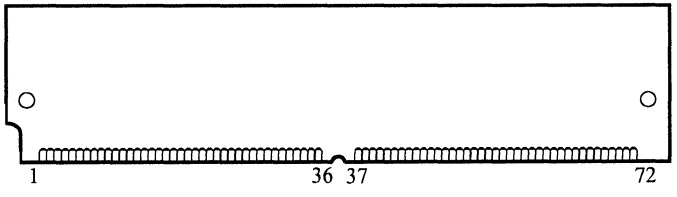
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 2048 refresh cycles distributed across 32ms
- 11/11 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au and Sn/Pb versions available

Description

The IBM11D4320B is a 16MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 4Mx32 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 8 4Mx4 devices, each in a 300mil package, and is compatible with the JEDEC 72-Pin SIMM standard.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 4Mx36 parity SIMM, IBM11D4360B, as well as other density and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

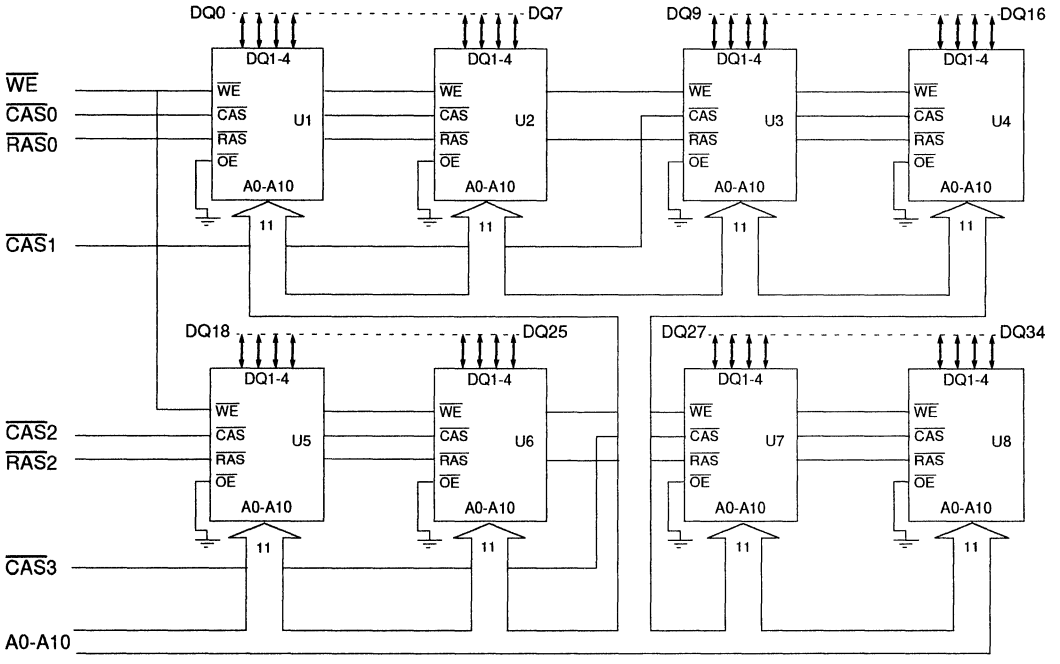
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	NC	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	A10	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	NC	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with parity (x36) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D4320BA-60	4M x 32	60ns	Sn/Pb	4.25" x 1" x .205"	
IBM11D4320BA-70	4M x 32	70ns	Sn/Pb	4.25" x 1" x .205"	
IBM11E4320BA-60	4M x 32	60ns	Au	4.25" x 1" x .205"	
IBM11E4320BA-70	4M x 32	70ns	Au	4.25" x 1" x .205"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V_{SS}	V_{SS}
PD2	NC	NC
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min(V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min(V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	5.5	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A10)	55	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	40	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	25	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	66	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	13	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1000	mA	1, 2, 3
		-70	—	880		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	16	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	1000	mA	1, 3
		-70	—	880		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	920	mA	1, 2, 3
		-70	—	800		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	8	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1000	mA	1, 3
		-70	—	880		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$	-20	+20		
		All others	-80	+80		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

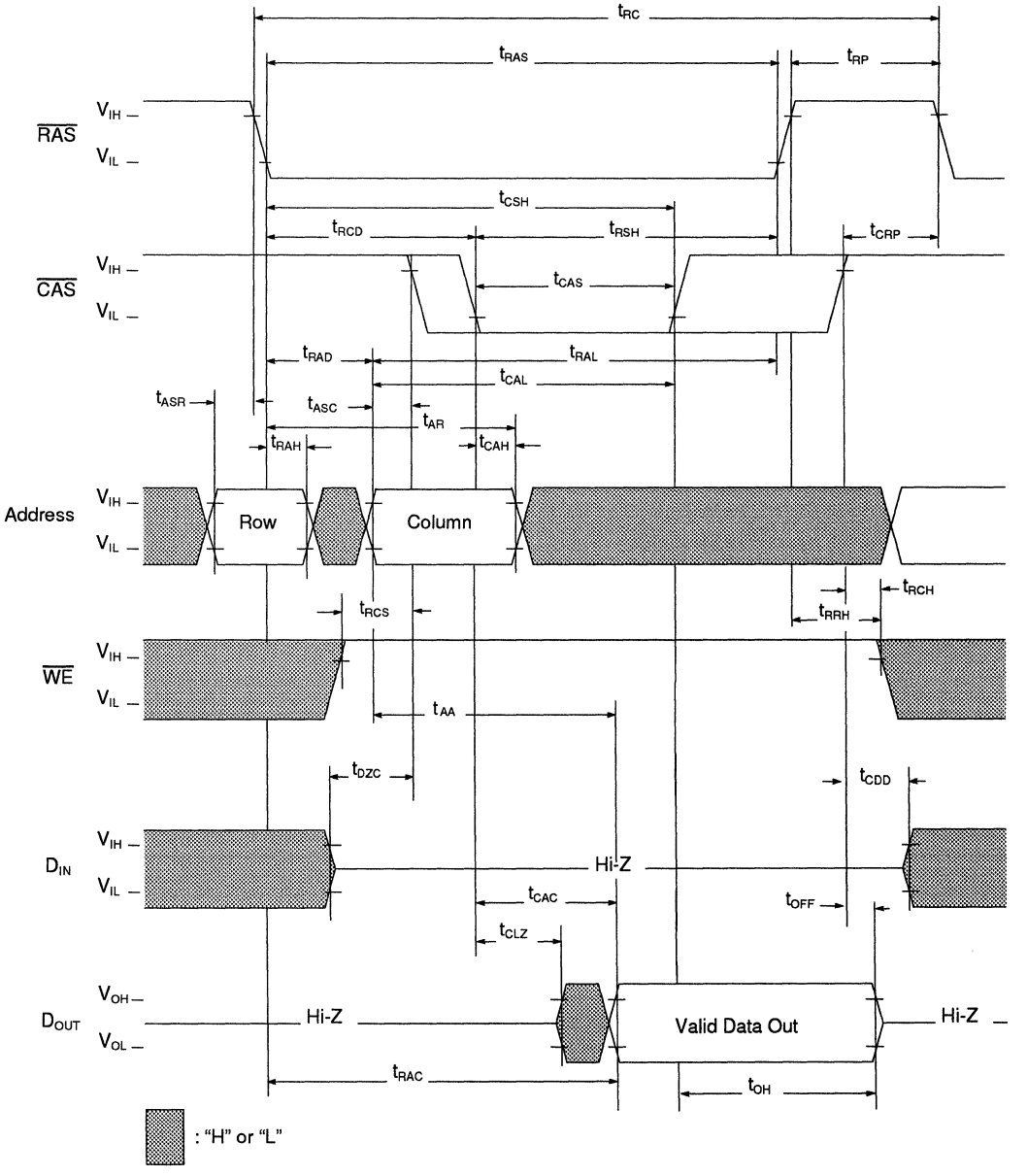
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Measured with the specified current load and 100pF..

Refresh Cycle

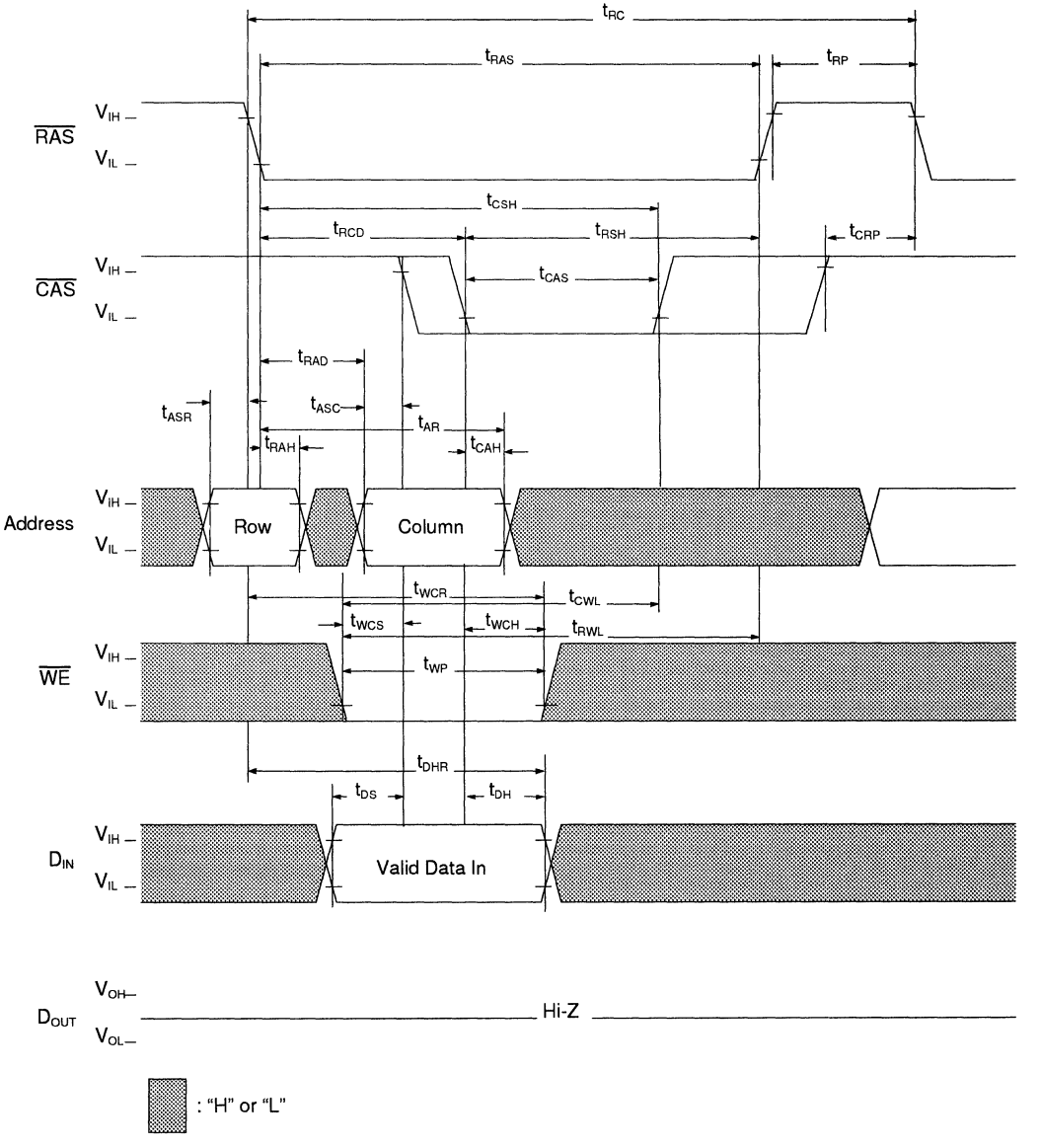
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	32	—	32	ms	1

1. 2048 refreshes are required every 32ms.

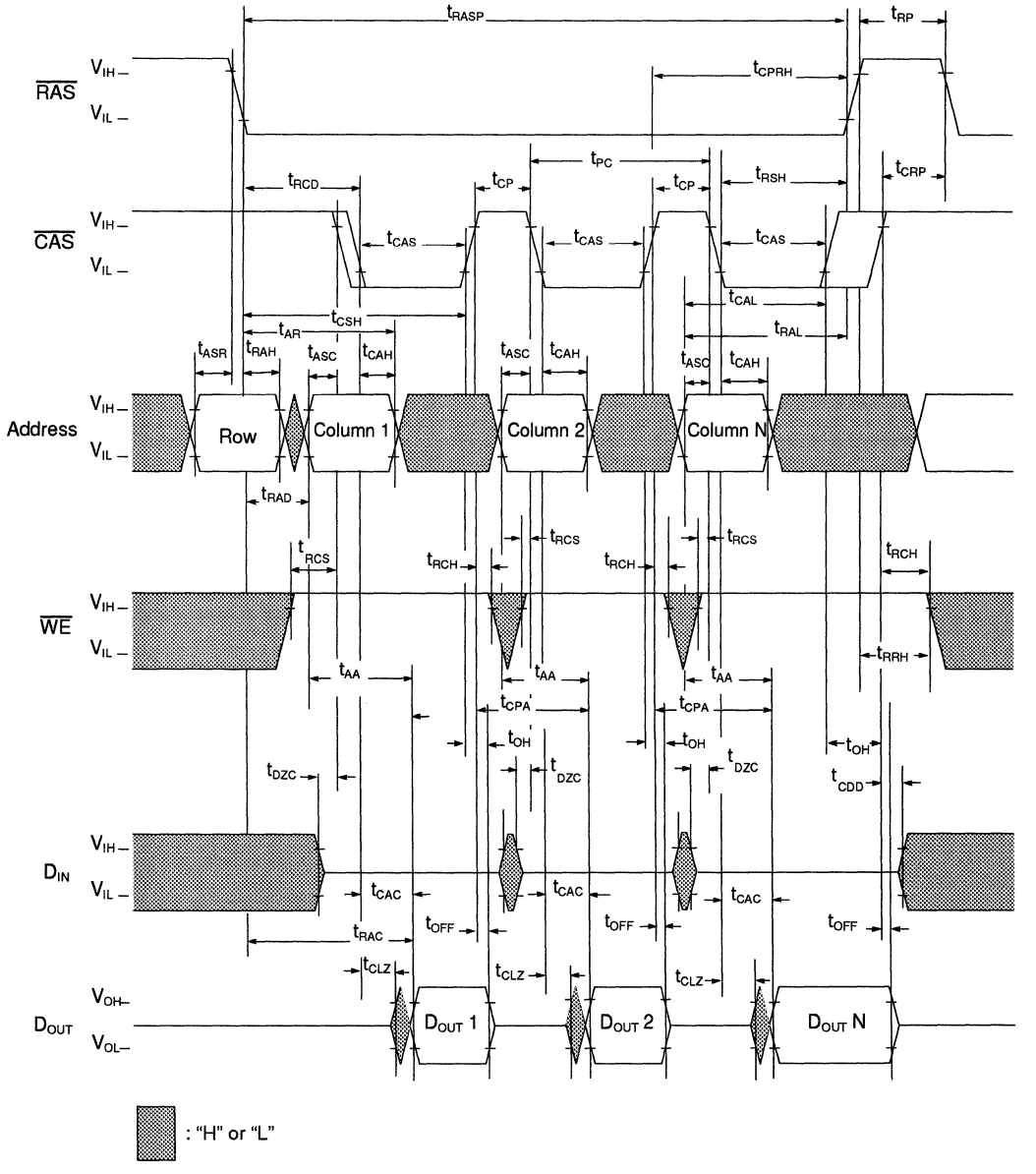
Read


tRC
tRAS
tRP
VIH
RAS
VIL
tCSH
tRCD
tRSH
tCRP
VIH
CAS
VIL
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
VIH
Address
VIL
Row
Column
tRCS
tRCH
tRRH
VIH
WE
VIL
tAA
tDZC
tCDD
VIH
DIN
VIL
Hi-Z
tCAC
tOFF
tCLZ
VOH
DOUT
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

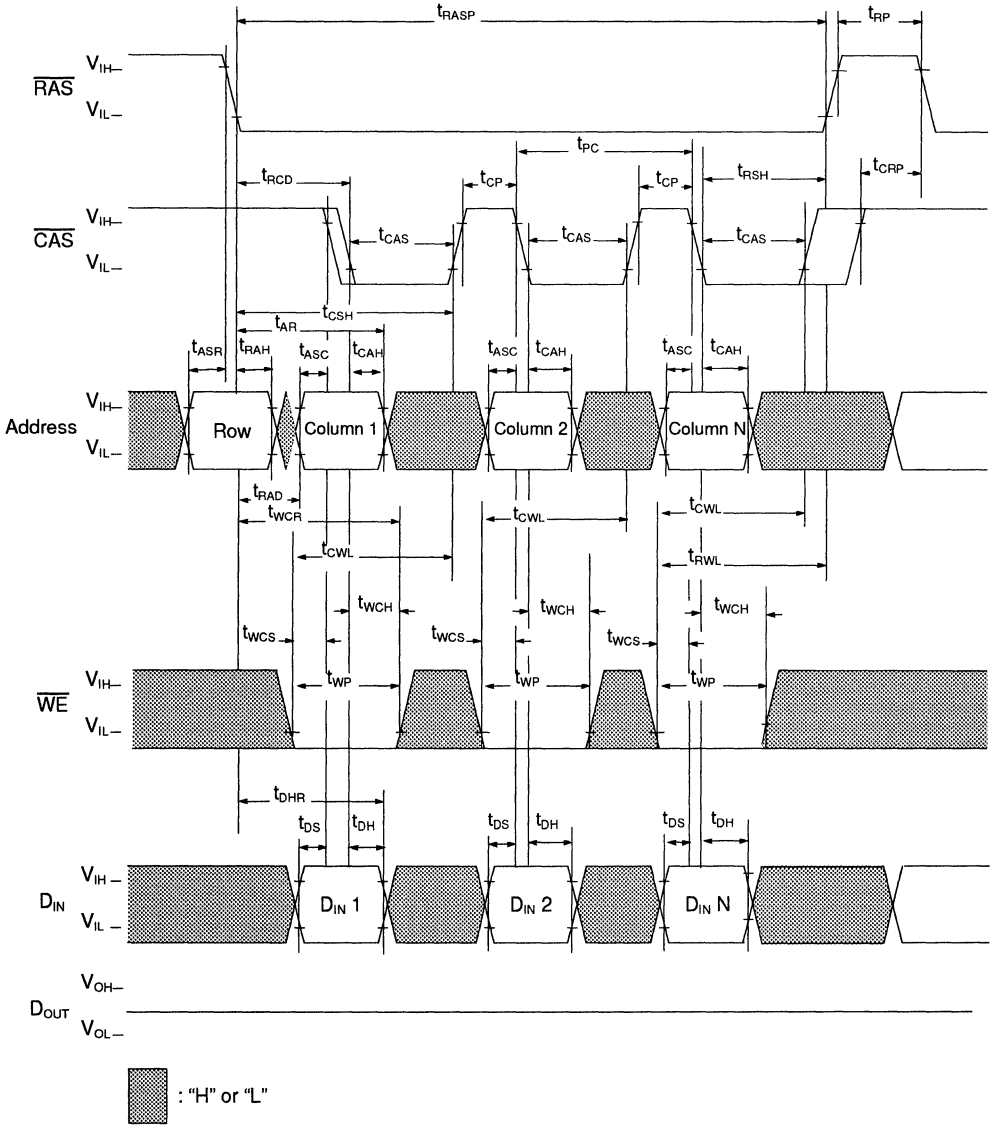
Write Cycle (Early Write)



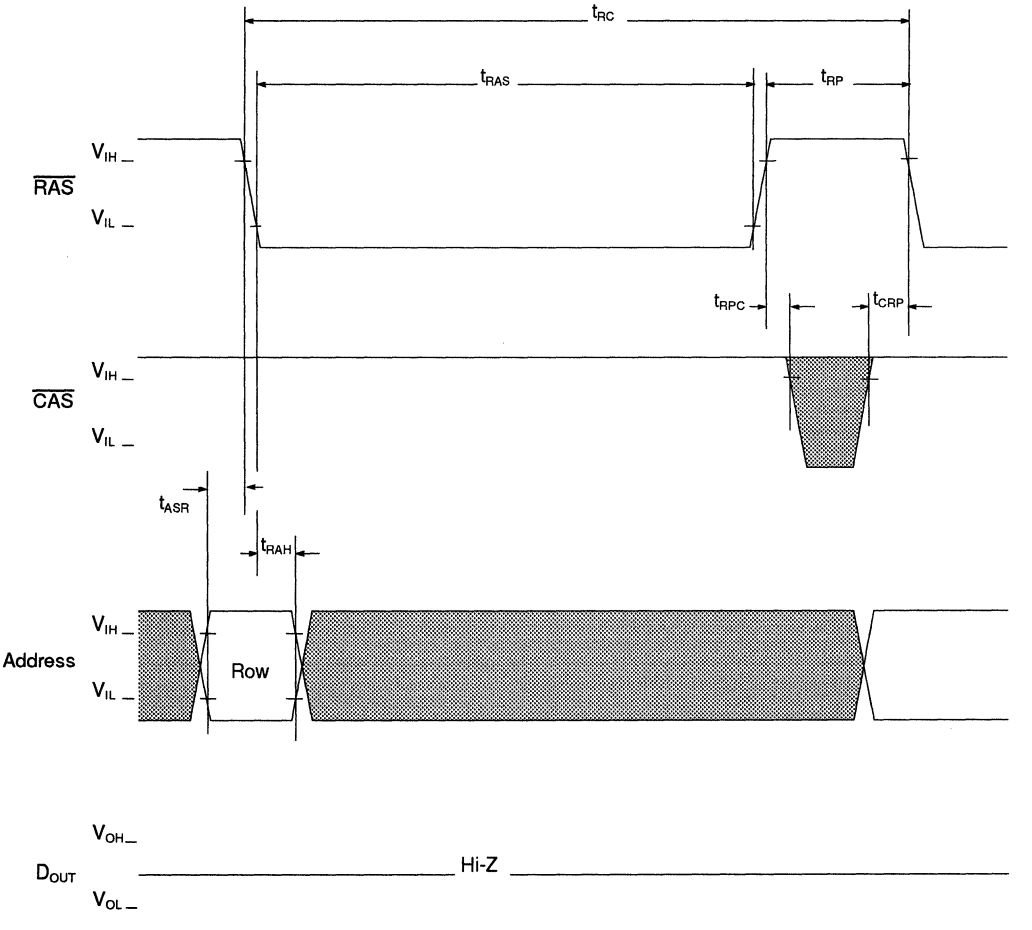
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

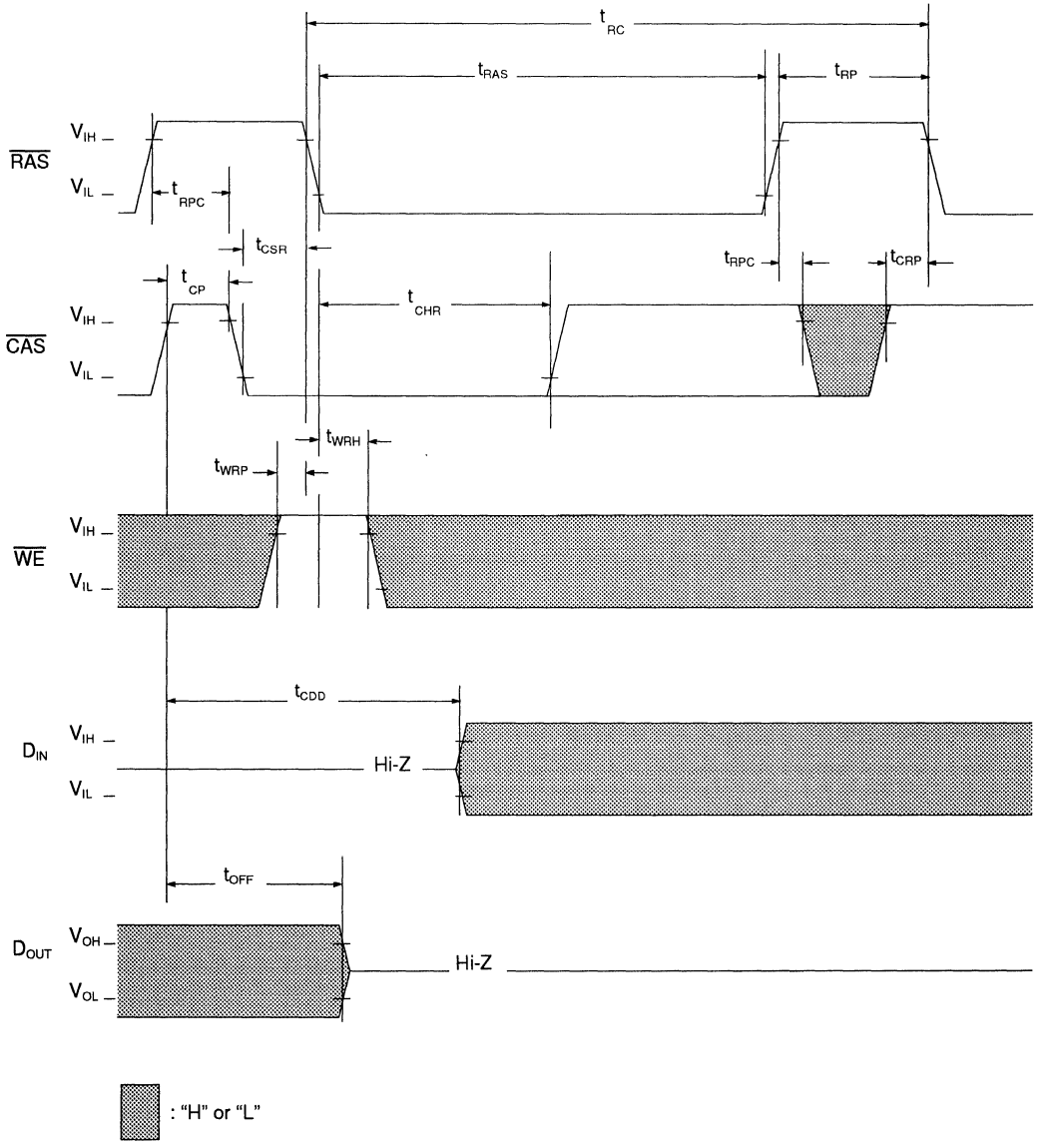


$\overline{RAS}$ Only Refresh Cycle



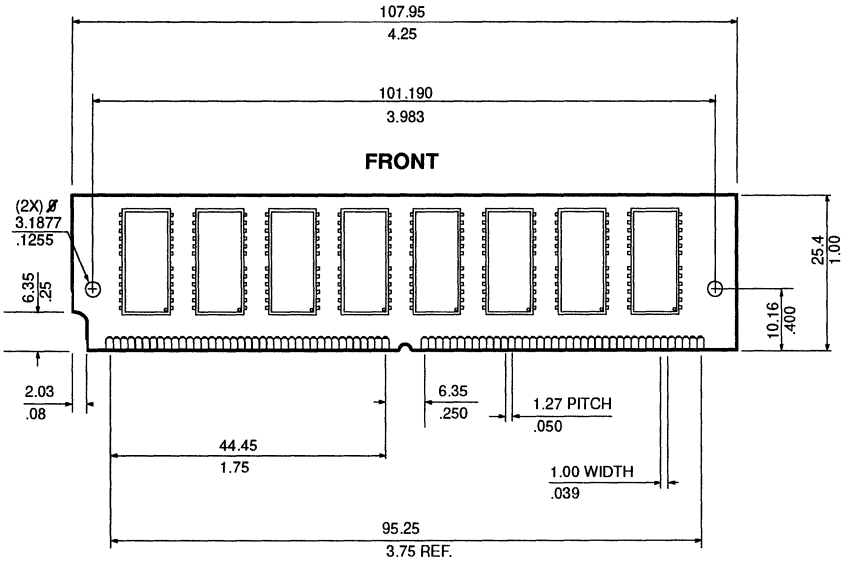
Note: $\overline{WE}$, D_{IN} are "H" or "L"

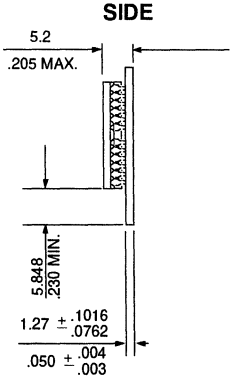
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Preliminary

8M x 32 DRAM Module

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

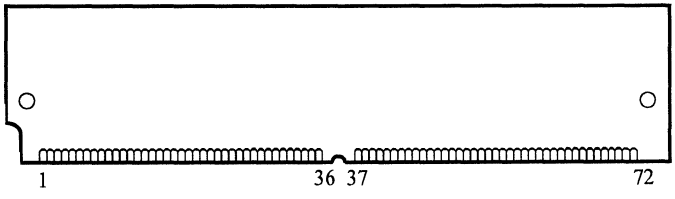
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 2048 refresh cycles distributed across 32ms
- 11/11 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au and Sn/Pb versions available

Description

The IBM11D8320B is a 32MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as an 8Mx32 high speed memory array, and is configured as 2 4Mx32 banks - each independently selectable via unique $\overline{RAS}$ inputs. The assembly is intended for use in 16, 32 and 64 bit applications. It is manufactured with 16 4Mx4 devices, each in a 300mil package, and is compatible with the JEDEC 72-Pin SIMM standard.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 8Mx36 parity SIMM, IBM11D8360B, as well as other density offerings and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

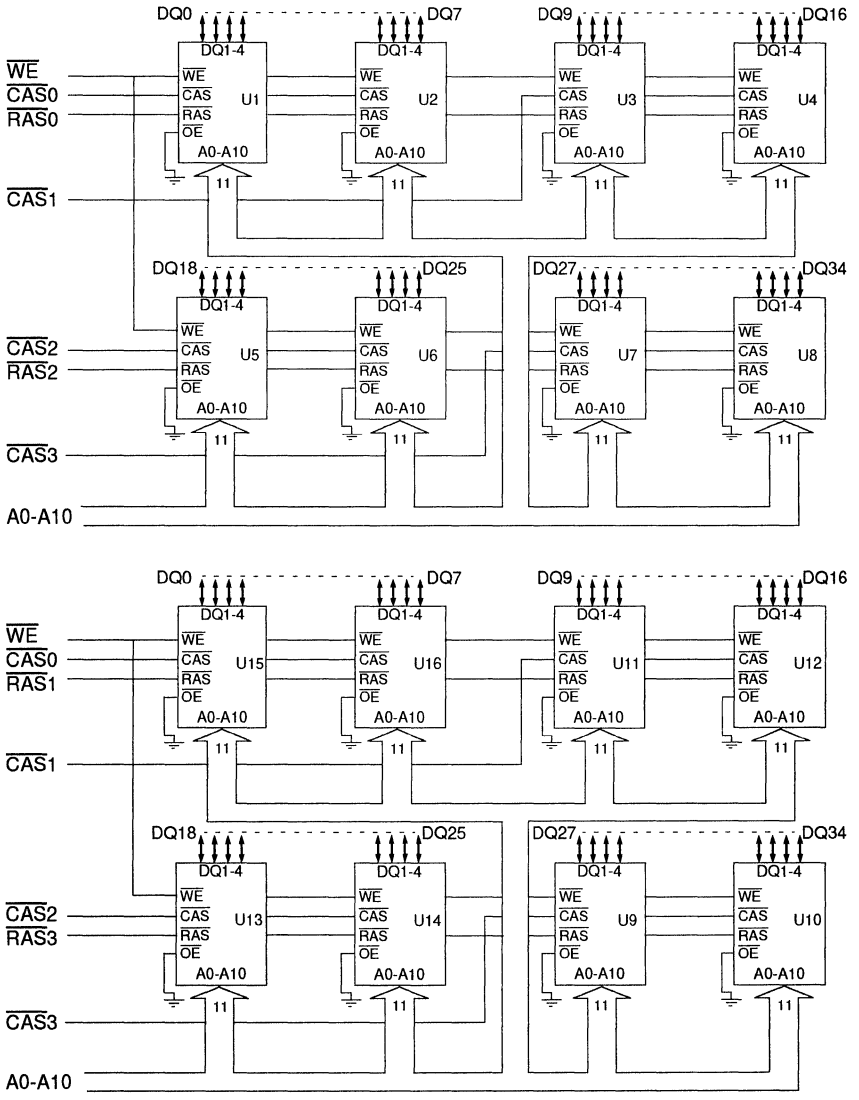
Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	V_{SS}	13	A1	25	DQ24	37	NC	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	A10	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	NC	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with parity (x36) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D8320BA-60	8M x 32	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D8320BA-70	8M x 32	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E8320BA-60	8M x 32	60ns	Au	4.25" x 1" x .360"	
IBM11E8320BA-70	8M x 32	70ns	Au	4.25" x 1" x .360"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	11	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A10)	100	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	40	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	40	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	127	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	25	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1016	mA	1, 2, 3
		-70	—	896		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	32	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1016	mA	1, 3, 4
		-70	—	896		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	936	mA	1, 2, 3
		-70	—	816		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	16	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	936	mA	1, 3, 4
		-70	—	816		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$	-40	+40		
		All others	-160	+160		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for 1 bank..

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

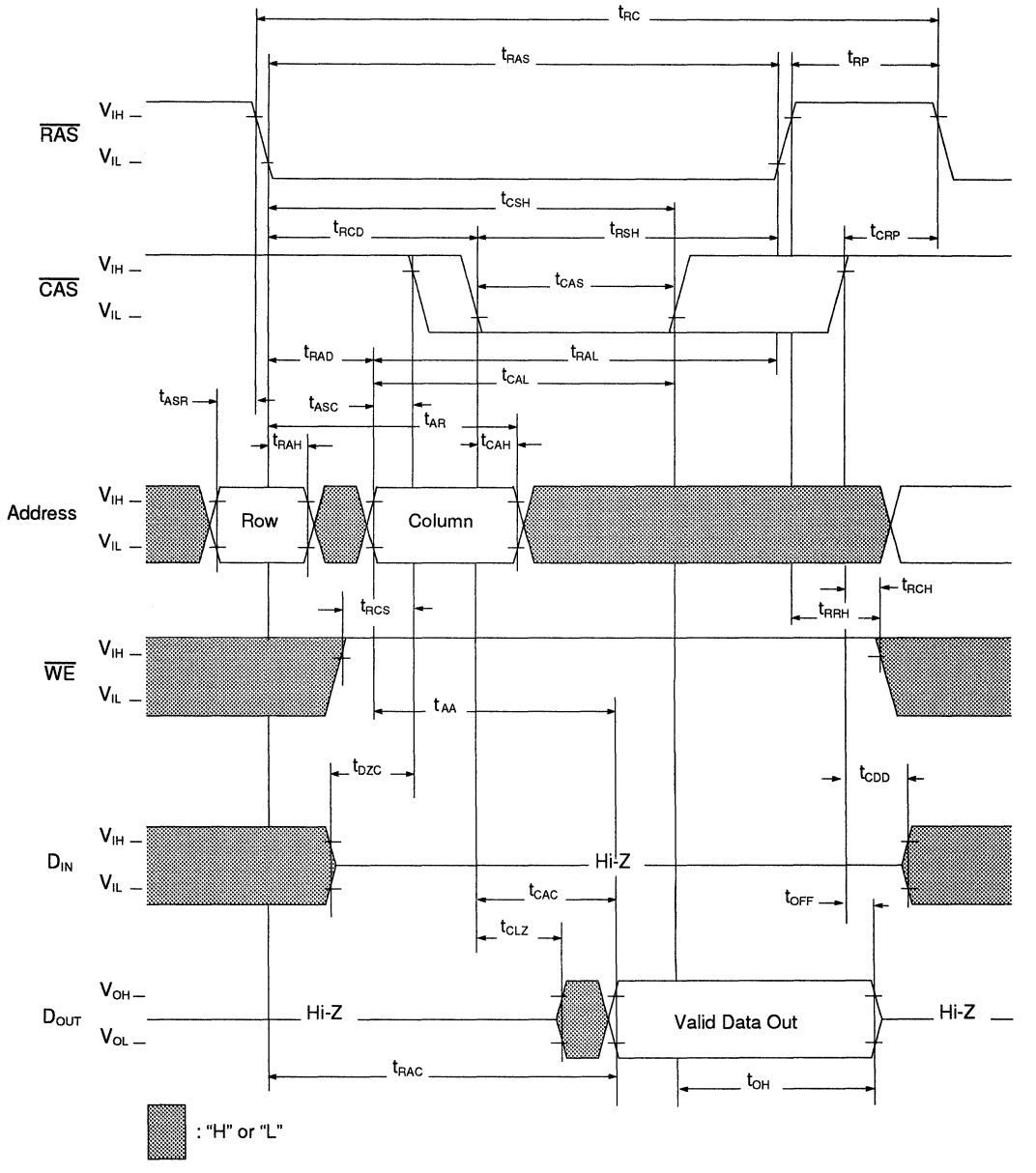
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Measured with the specified current load and 100pF.

Refresh Cycle

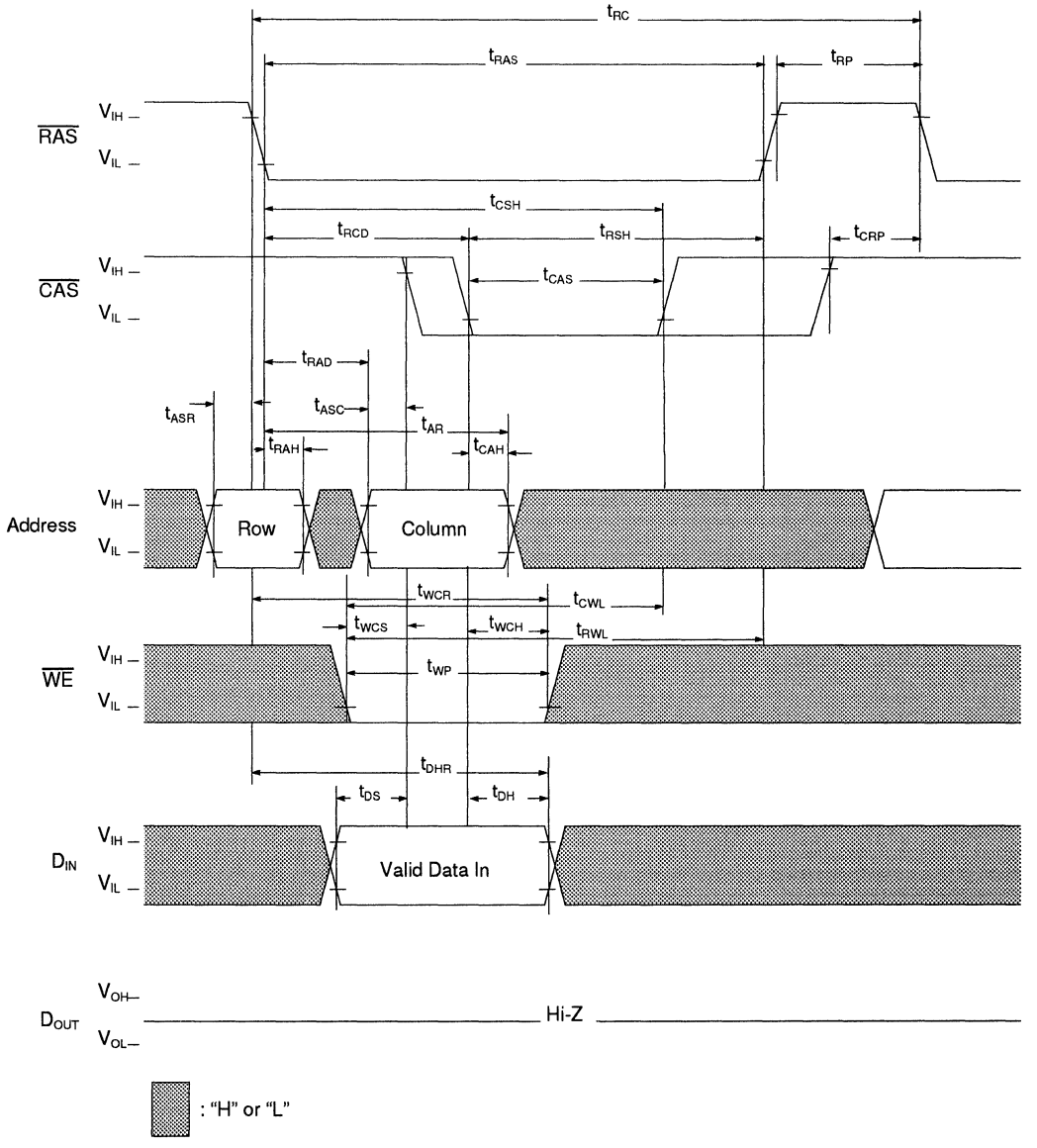
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	32	—	32	ms	1

1. 2048 refreshes are required every 32ms.

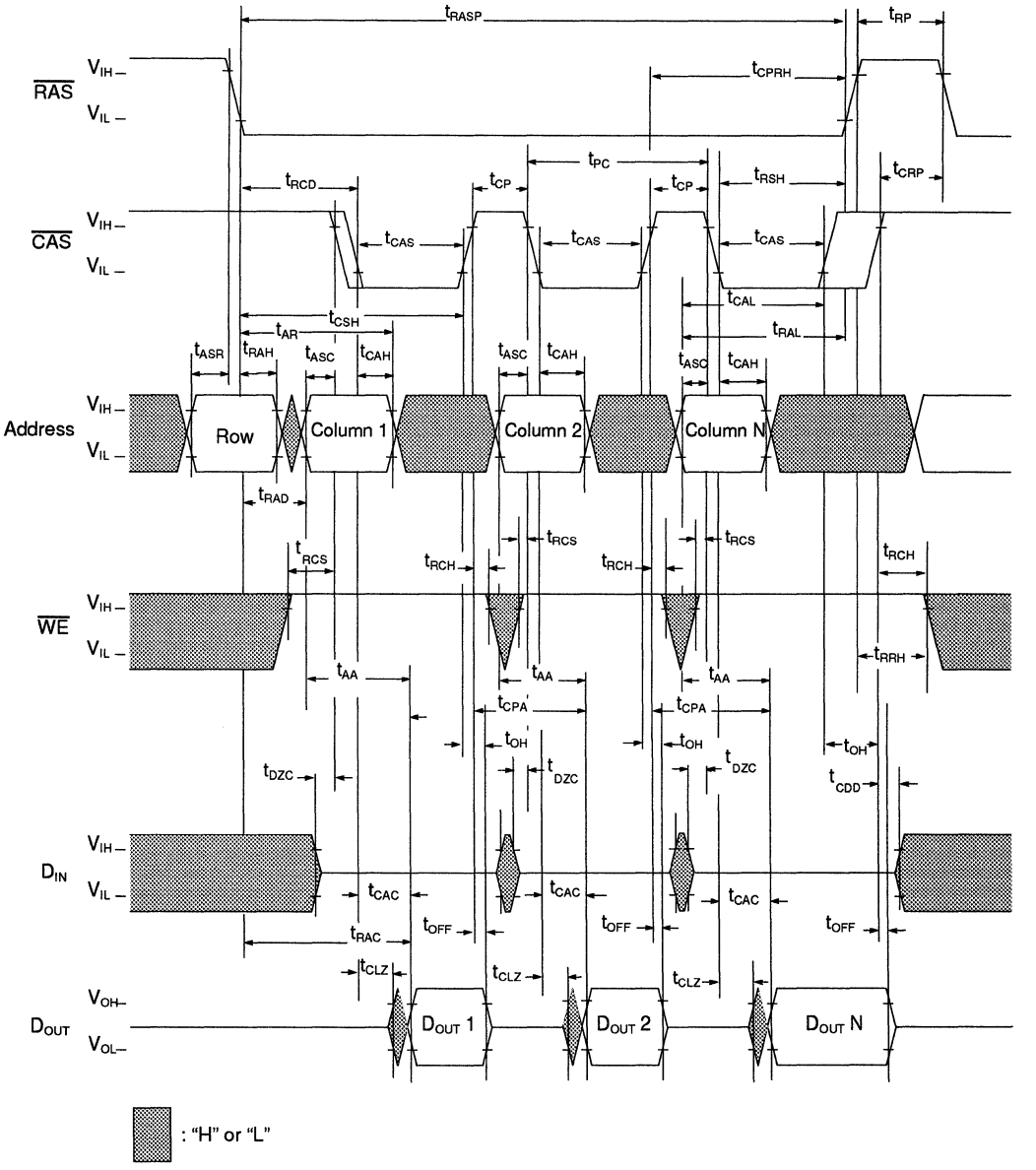
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCH
tRCS
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

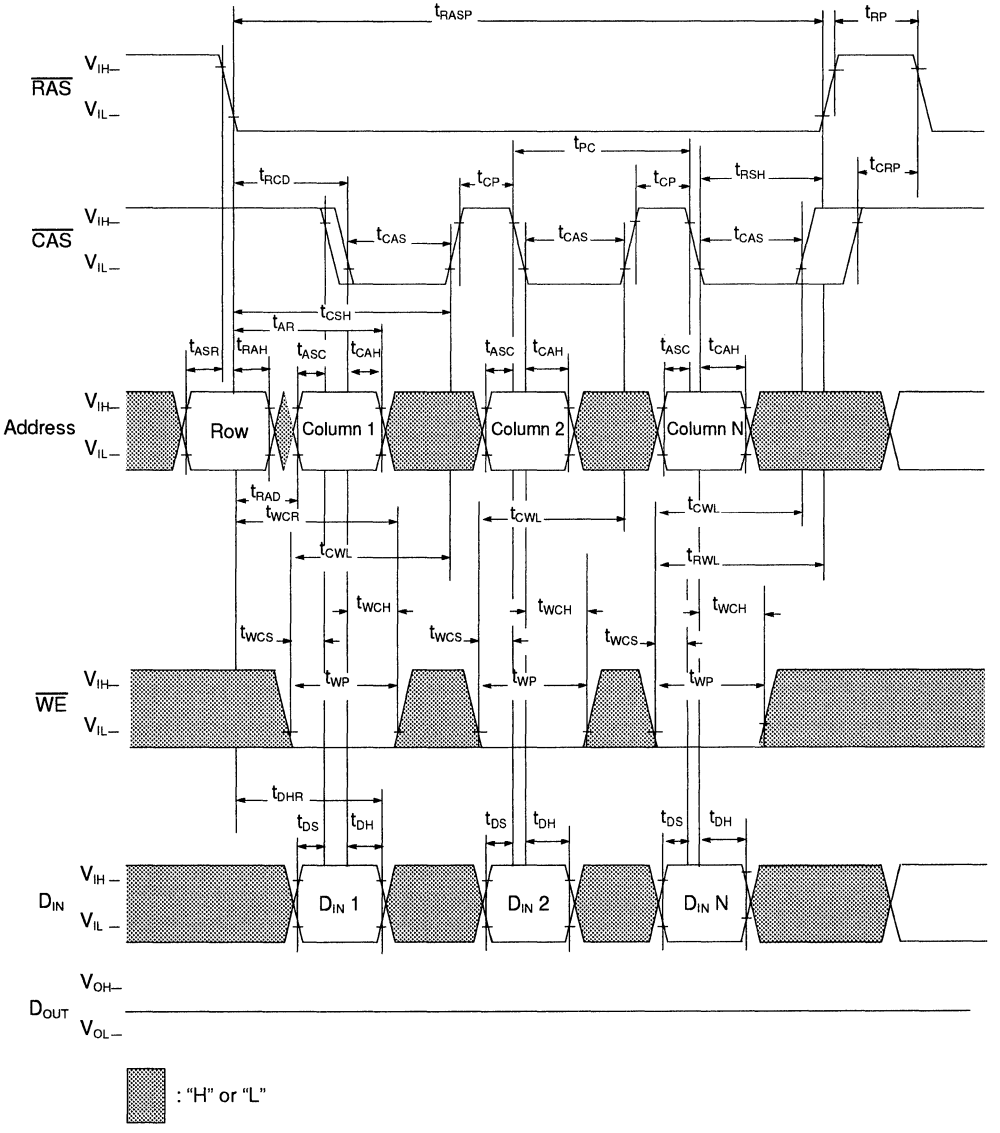
Write Cycle (Early Write)



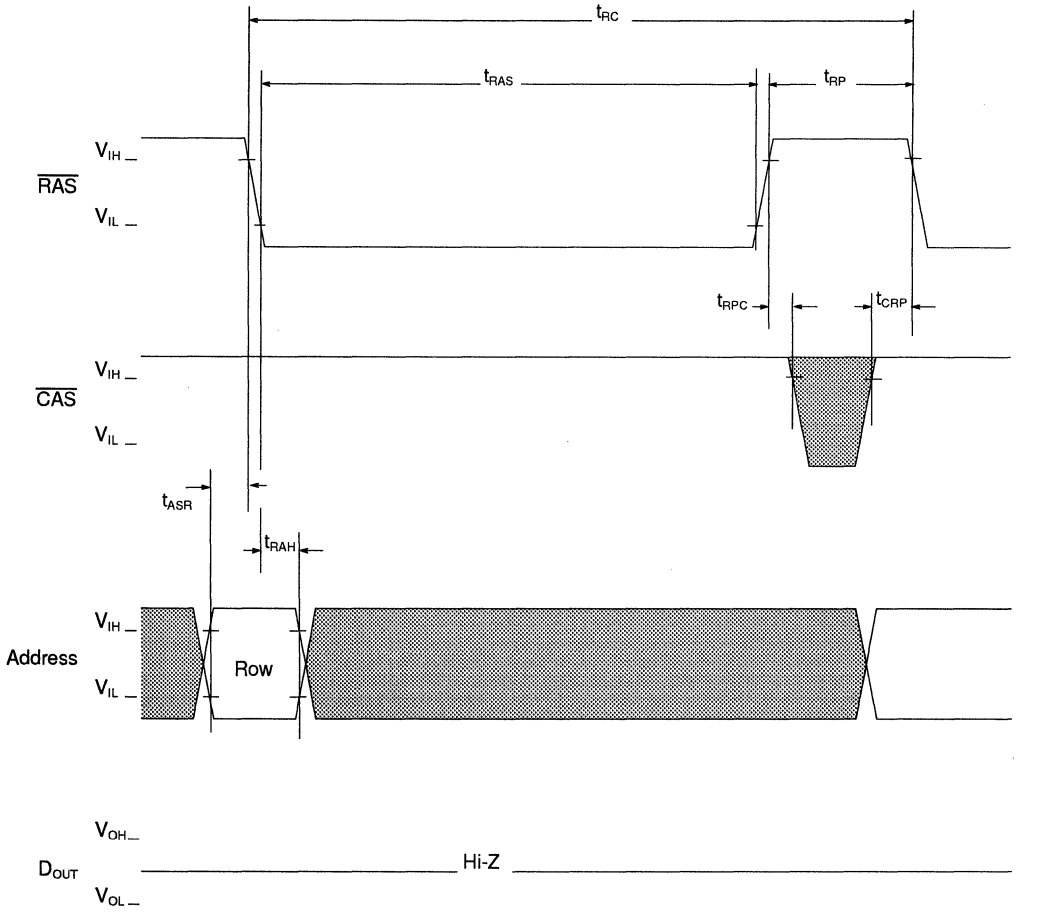
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

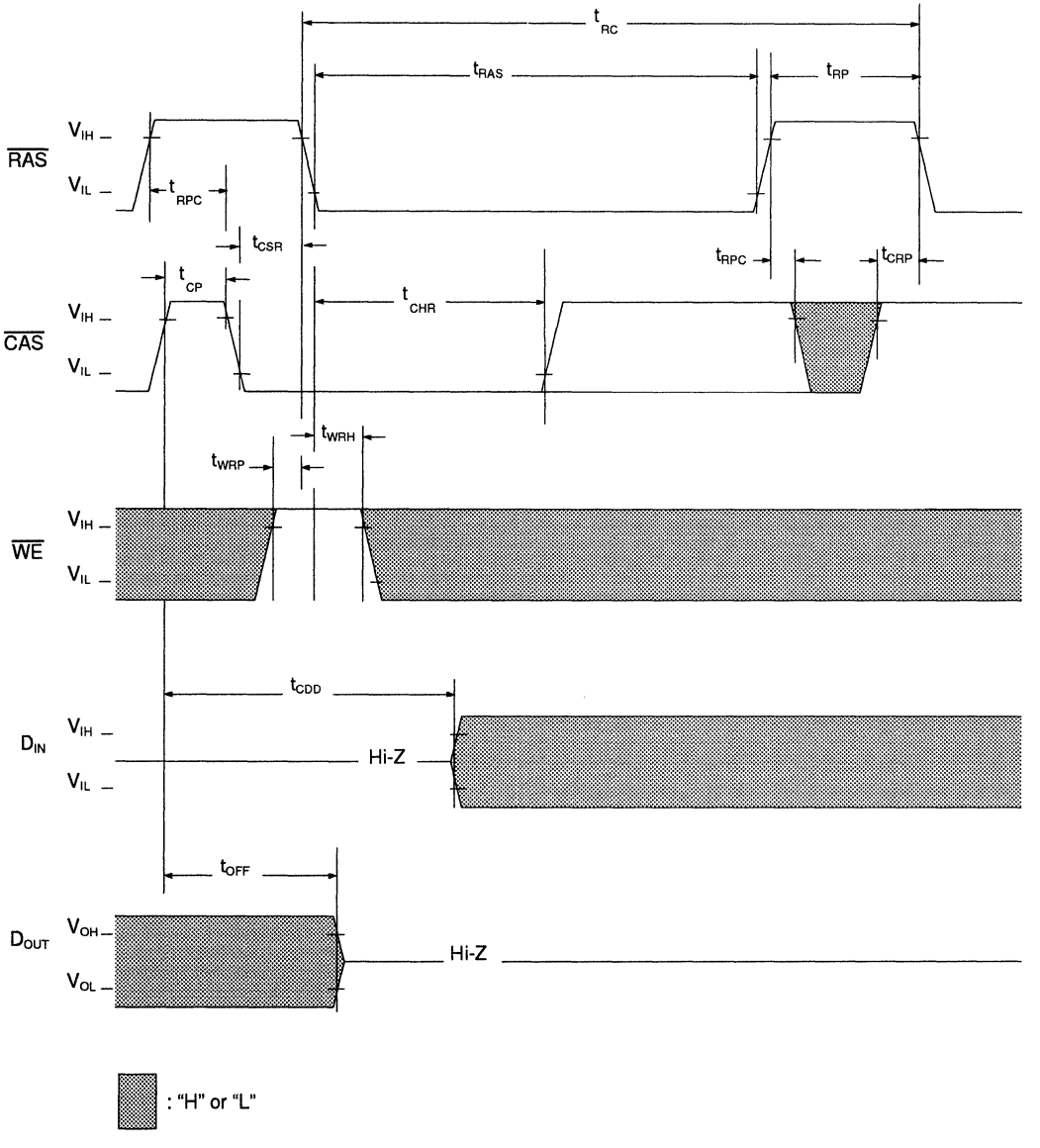


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, D_{IN} are "H" or "L"

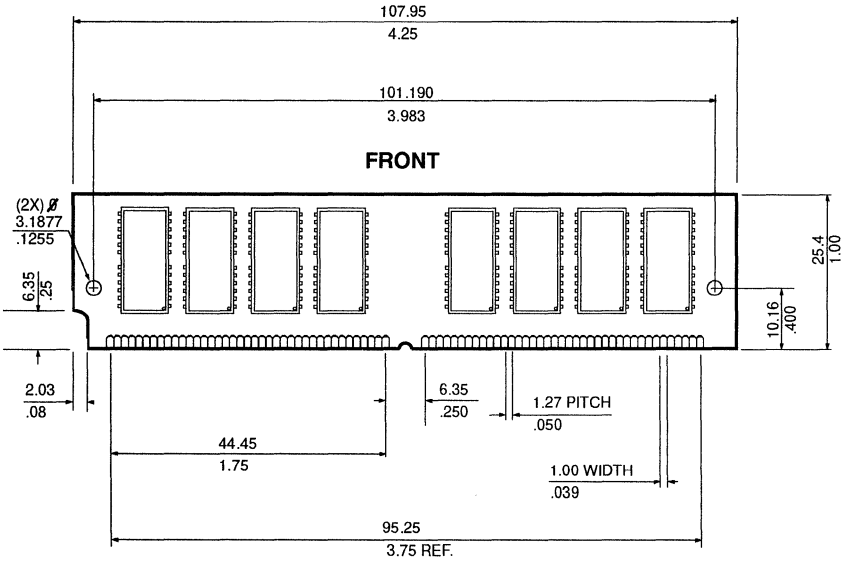
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

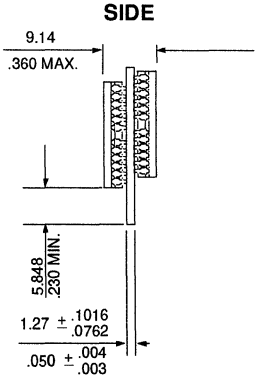


: "H" or "L"

Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

1M x 36 DRAM Module

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

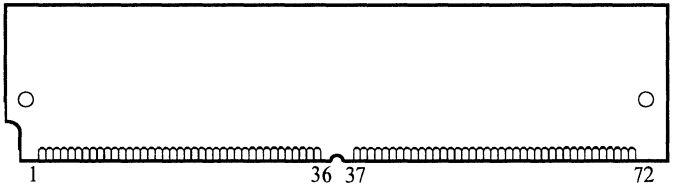
- High Performance CMOS process
- Single 5.0, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write parity applications
- Au and Sn/Pb versions available

Description

The IBM11D1360BA/B is a 4MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 1Mx36 high speed memory array that is intended for use in 18, 36, and 72 bit parity applications. It is manufactured with 8 1Mx4 devices, each in either a 350mil or 300mil package, and 4 1Mx1 devices in a 300mil package. The module is compatible with the JEDEC 72-pin SIMM standard.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 1Mx32 non-parity SIMM, IBM11D1320B, as well as higher density and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

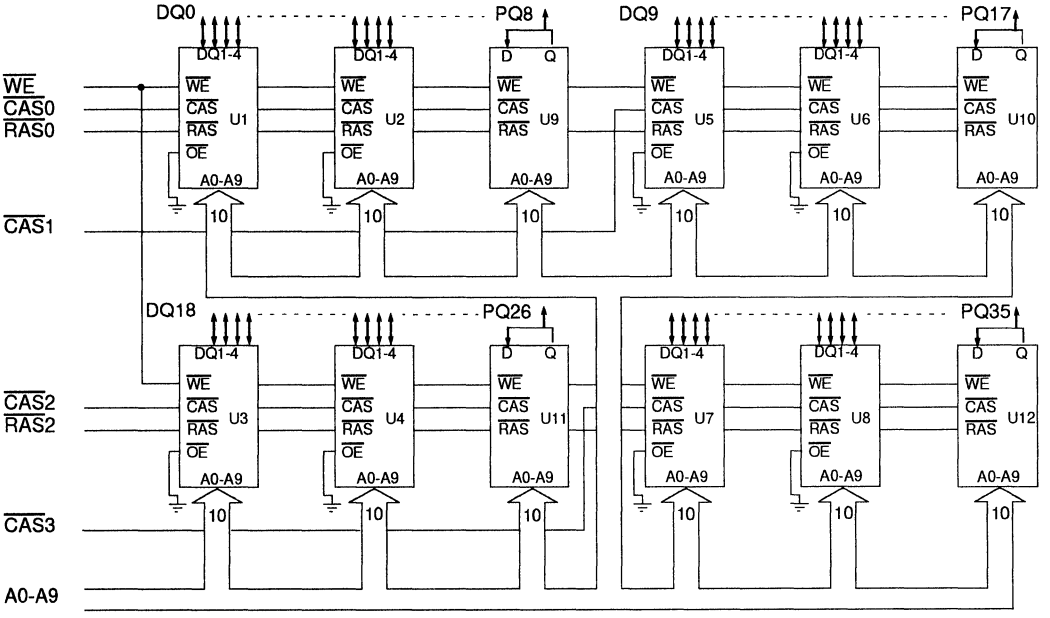
1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D1360BA-60	1M x 36	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D1360BA-70	1M x 36	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E1360BA-60	1M x 36	60ns	Au	4.25" x 1" x .360"	
IBM11E1360BA-70	1M x 36	70ns	Au	4.25" x 1" x .360"	
IBM11D1360BB-60	1M x 36	60ns	Sn/Pb	4.25" x .85" x .360"	1
IBM11D1360BB-70	1M x 36	70ns	Sn/Pb	4.25" x .85" x .360"	1
IBM11E1360BB-60	1M x 36	60ns	Au	4.25" x .85" x .360"	1
IBM11E1360BB-70	1M x 36	70ns	Au	4.25" x .85" x .360"	1

1. Limited availability, for height-constrained applications.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 6.5	V	1
V_{IN}	Input Voltage	-0.7 to V_{CC} + 0.7	V	1
V_{OUT}	Output Voltage	-0.7 to V_{CC} + 0.7	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	7.25	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	70	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	40	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	21	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	68	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	13	pF	
$C_{I/O2}$	Output Capacitance (PQ8, 17, 26, 35)	18	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1320	mA	1, 2, 3
		-70	—	1204		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	24	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	1320	mA	1, 3
		-70	—	1204		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	920	mA	1, 2, 3
		-70	—	840		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	20	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1320	mA	1, 3
		-70	—	1204		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$	-30	+30		
		All others	-120	+120		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -4mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. The 1M x 4 DRAM Outputs will remain disabled until these 8 cycles have occurred. This prevents data contention (excessive current) during power on. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	—	—	—	—	ns	3
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	30	—	40	ns	2, 3

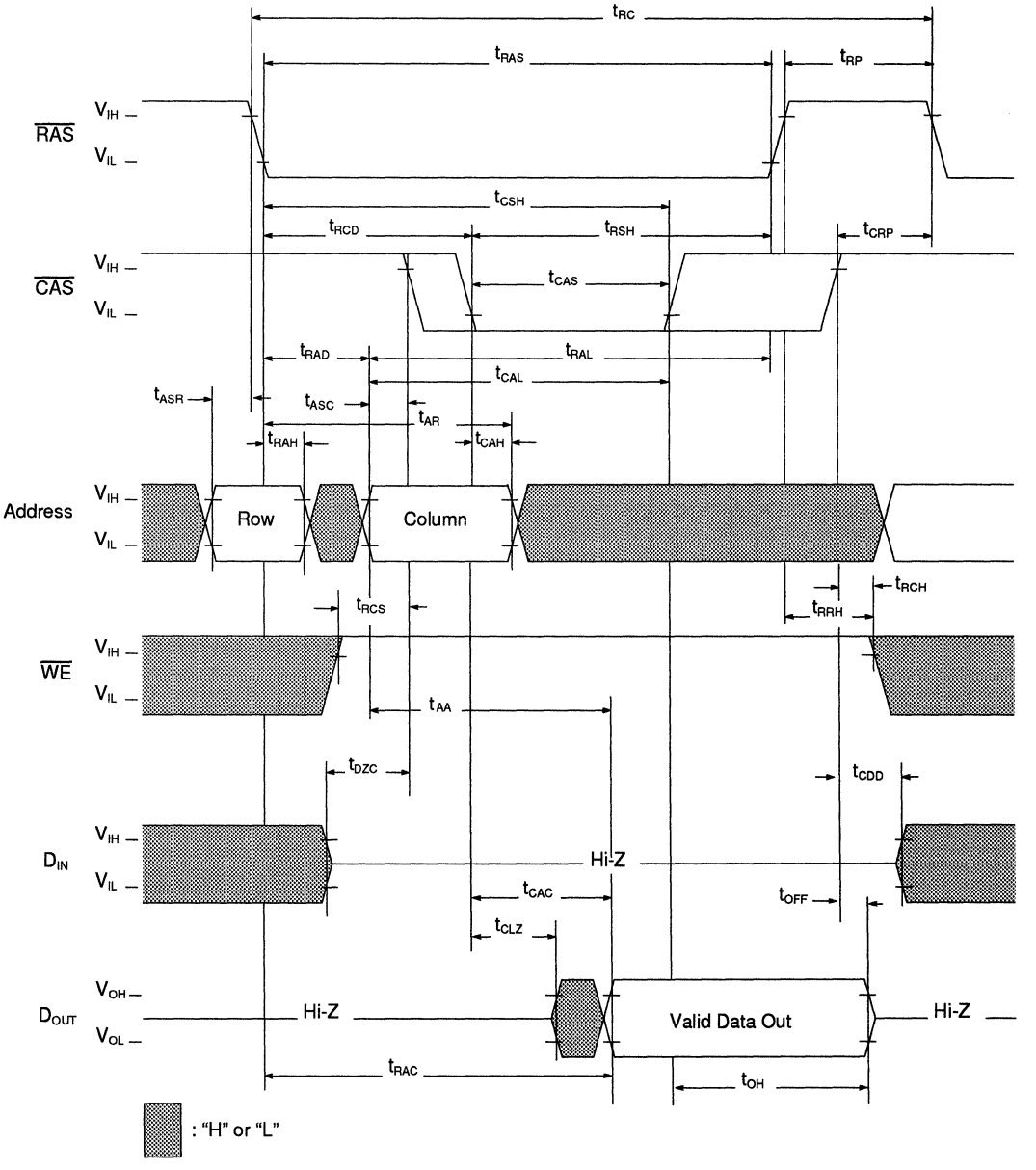
1. This timing parameter is not applicable to this product, but applies to a related product in this family.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Access time assumes a load of 100pF.

Refresh Cycle

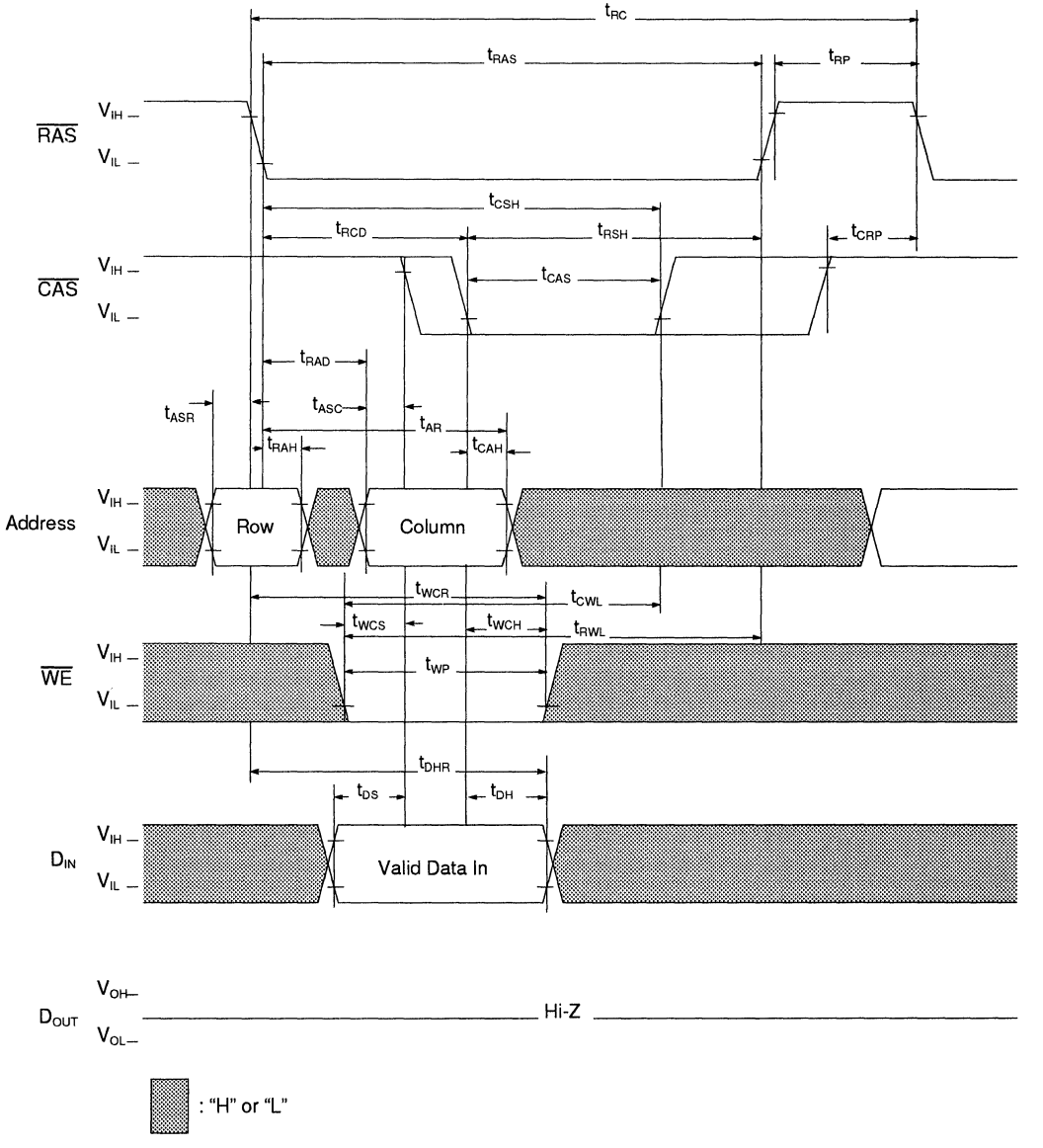
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	30	—	30	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	5	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms. The DC variation in the V_{CC} supply may not exceed 300mV within a refresh interval (16ms).

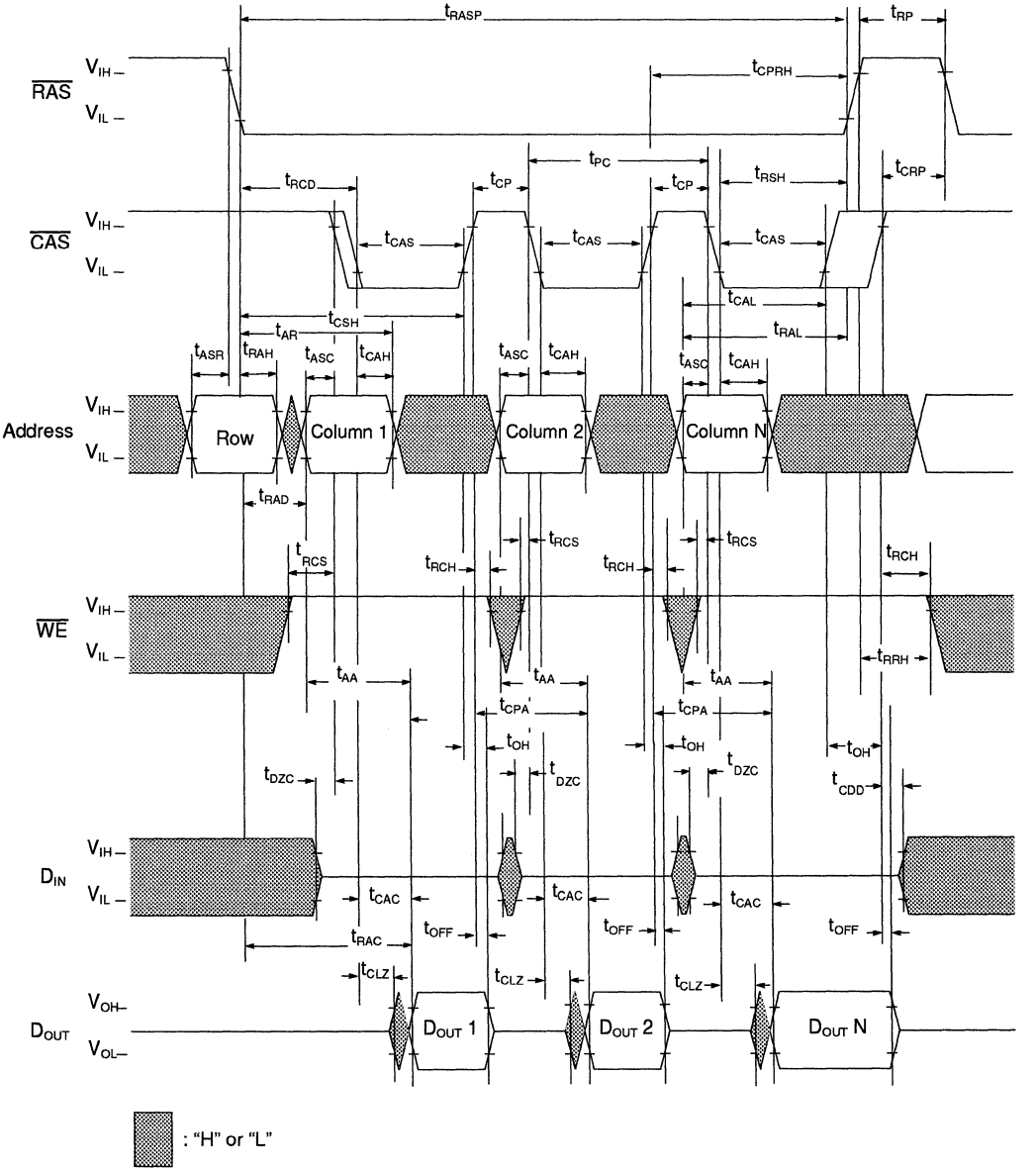
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCH
tRCS
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

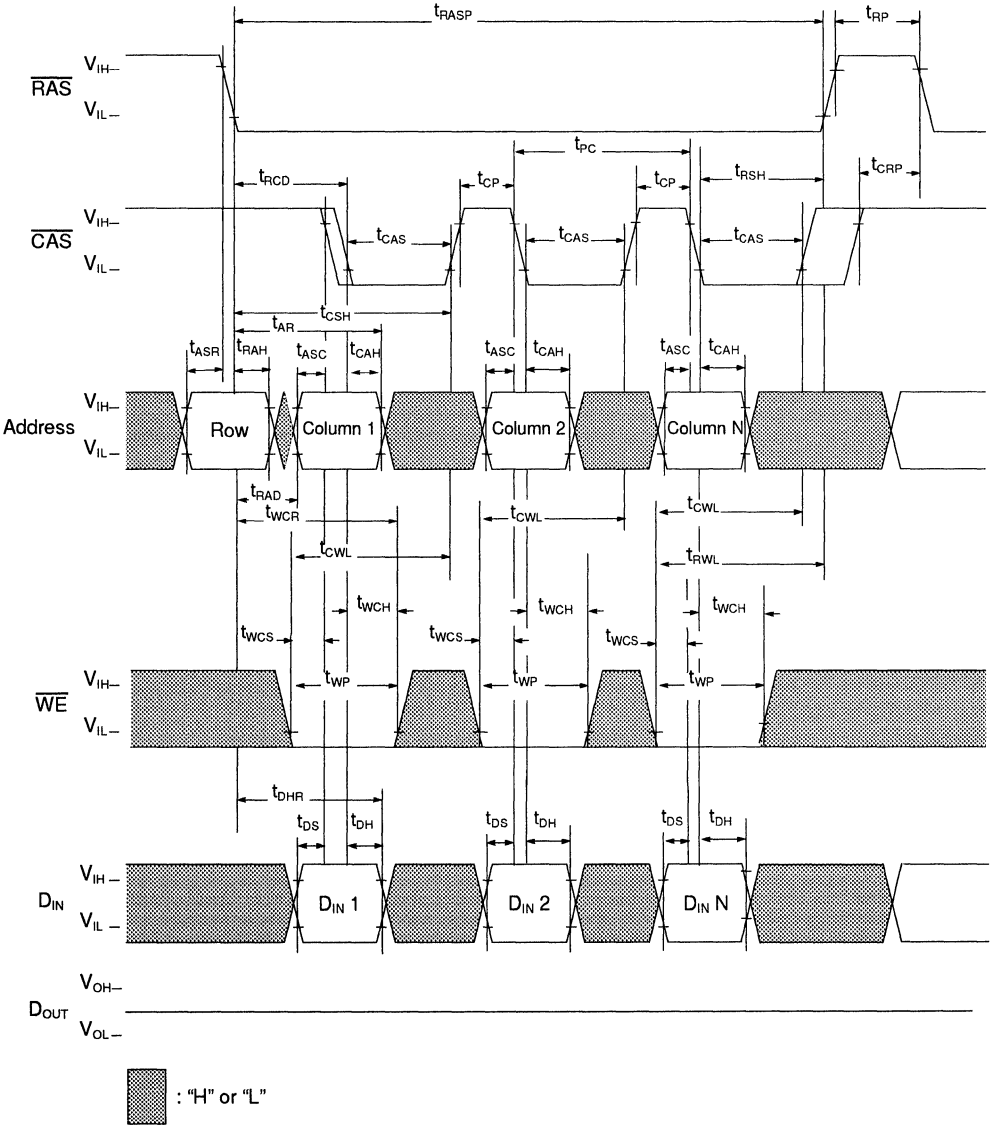
Write Cycle (Early Write)



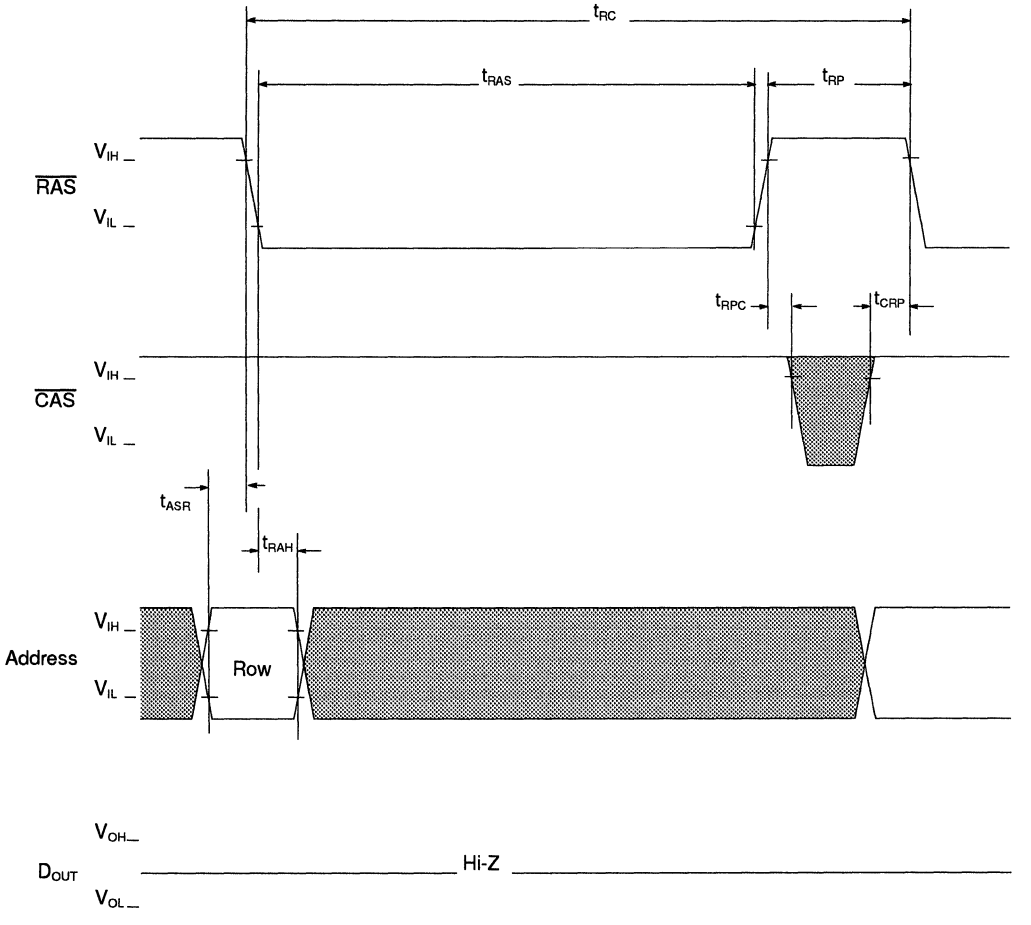
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



$\overline{RAS}$ Only Refresh Cycle



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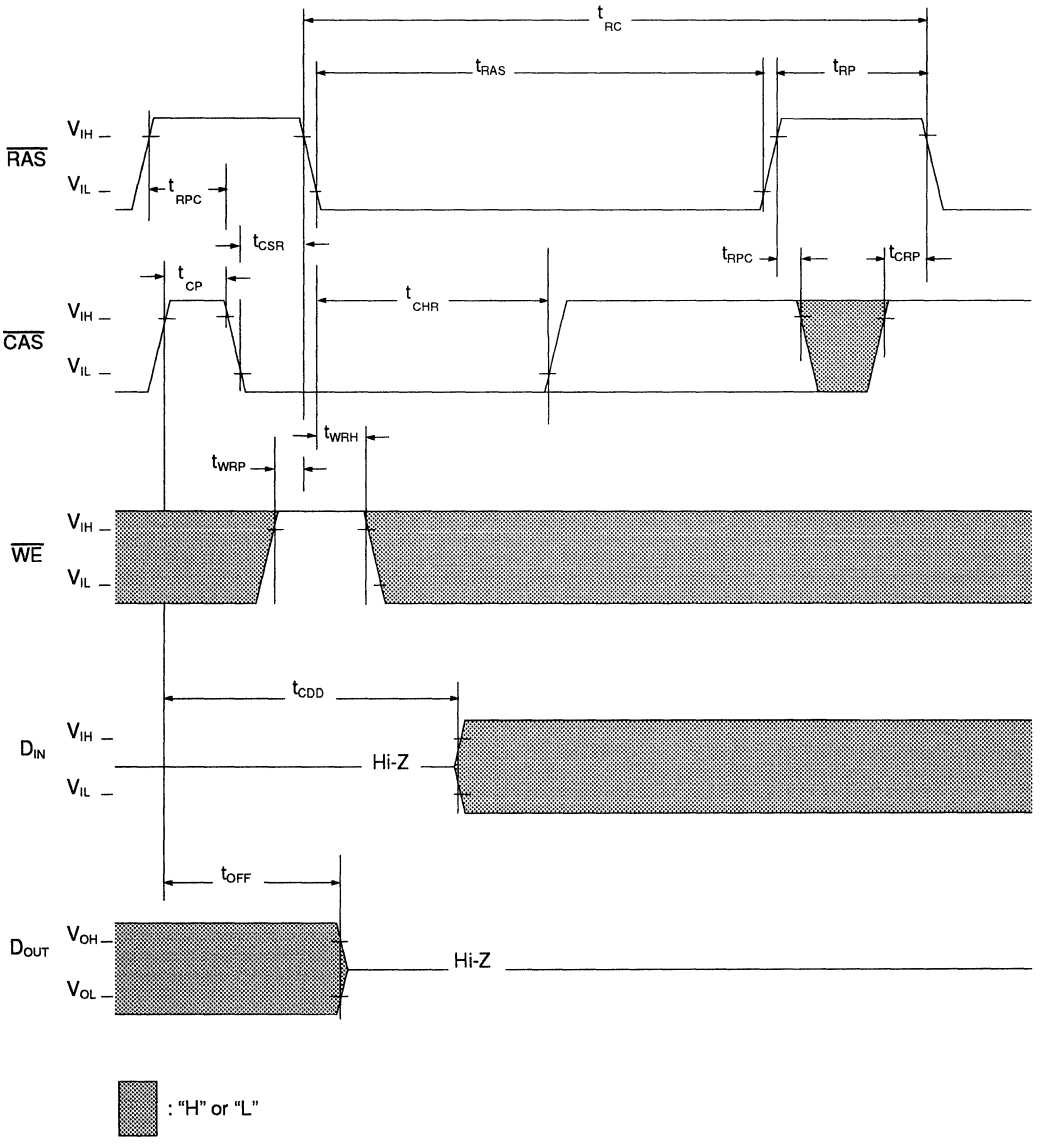
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



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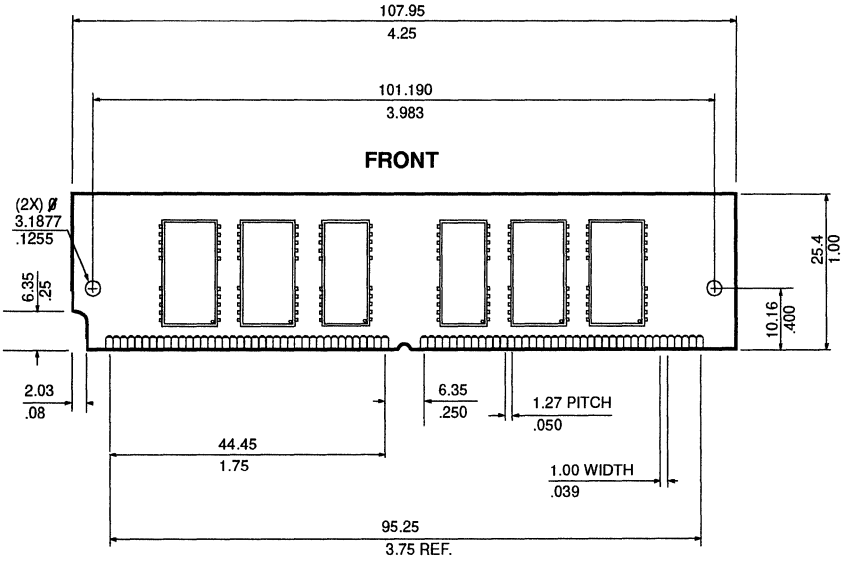
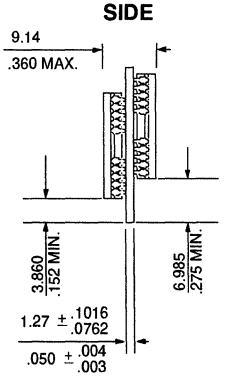
Layout Drawing (IBM11D1360BA)





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1M x 36 DRAM Module

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- Au and Sn/Pb versions available

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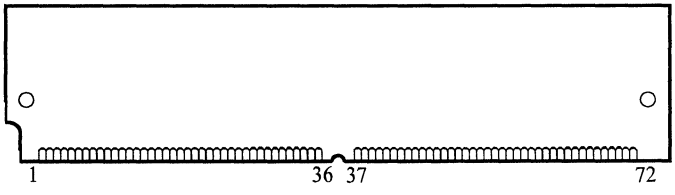


Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

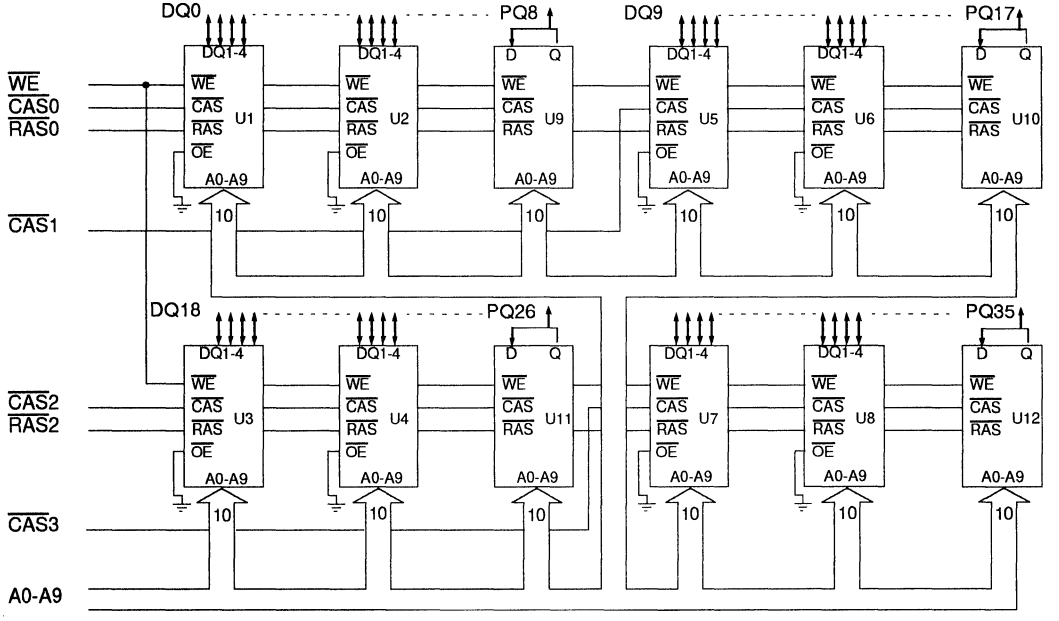
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D1360BD-60	1M x 36	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D1360BD-70	1M x 36	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E1360BD-60	1M x 36	60ns	Au	4.25" x 1" x .360"	
IBM11E1360BD-70	1M x 36	70ns	Au	4.25" x 1" x .360"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +6.0	V	1
V_{IN}	Input Voltage	-1.0 to +6.0	V	1
V_{OUT}	Output Voltage	-1.0 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	5.72	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	Vcc + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	78	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	50	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	27	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	94	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	13	pF	
$C_{I/O2}$	Output Capacitance (PQ8, 17, 26, 35)	18	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1040	mA	1, 2, 3
		-70	—	900		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	24	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	1040	mA	1, 3
		-70	—	900		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	800	mA	1, 2, 3
		-70	—	680		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	12	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1040	mA	1, 3
		-70	—	900		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$	-30	+30		
		All others	-120	+120		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	30	—	40	ns	1, 2

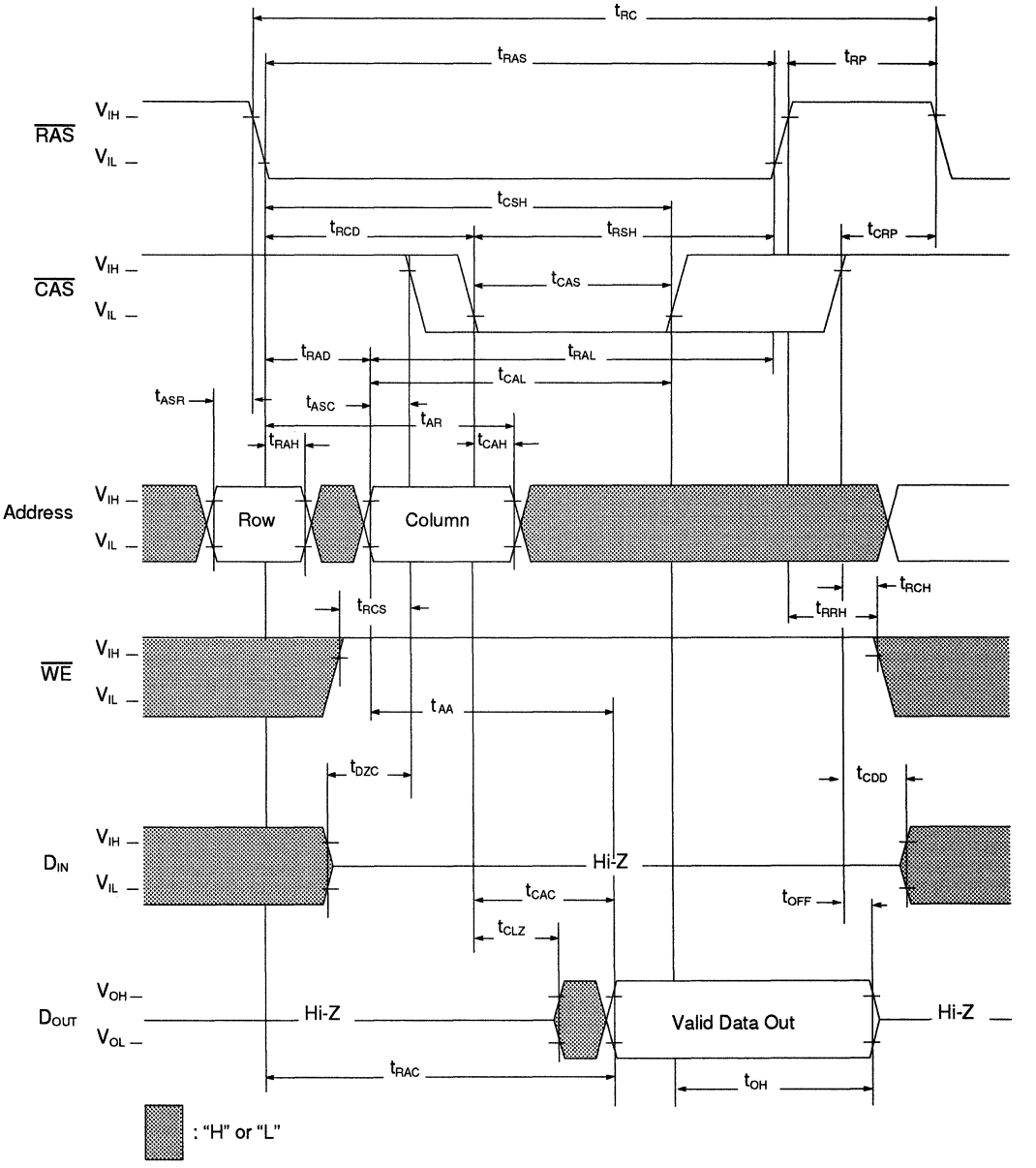
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

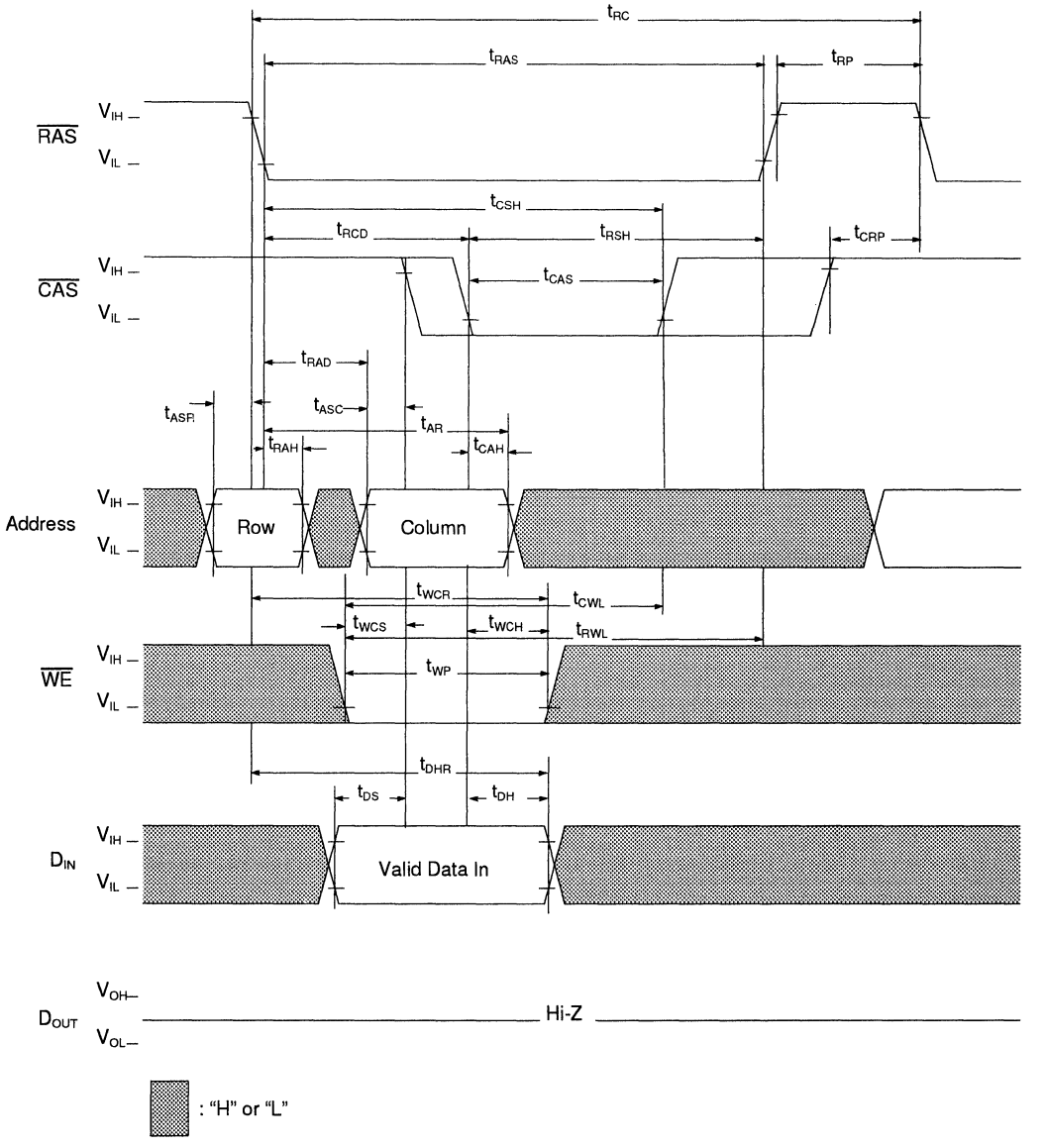
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	30	—	30	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms.

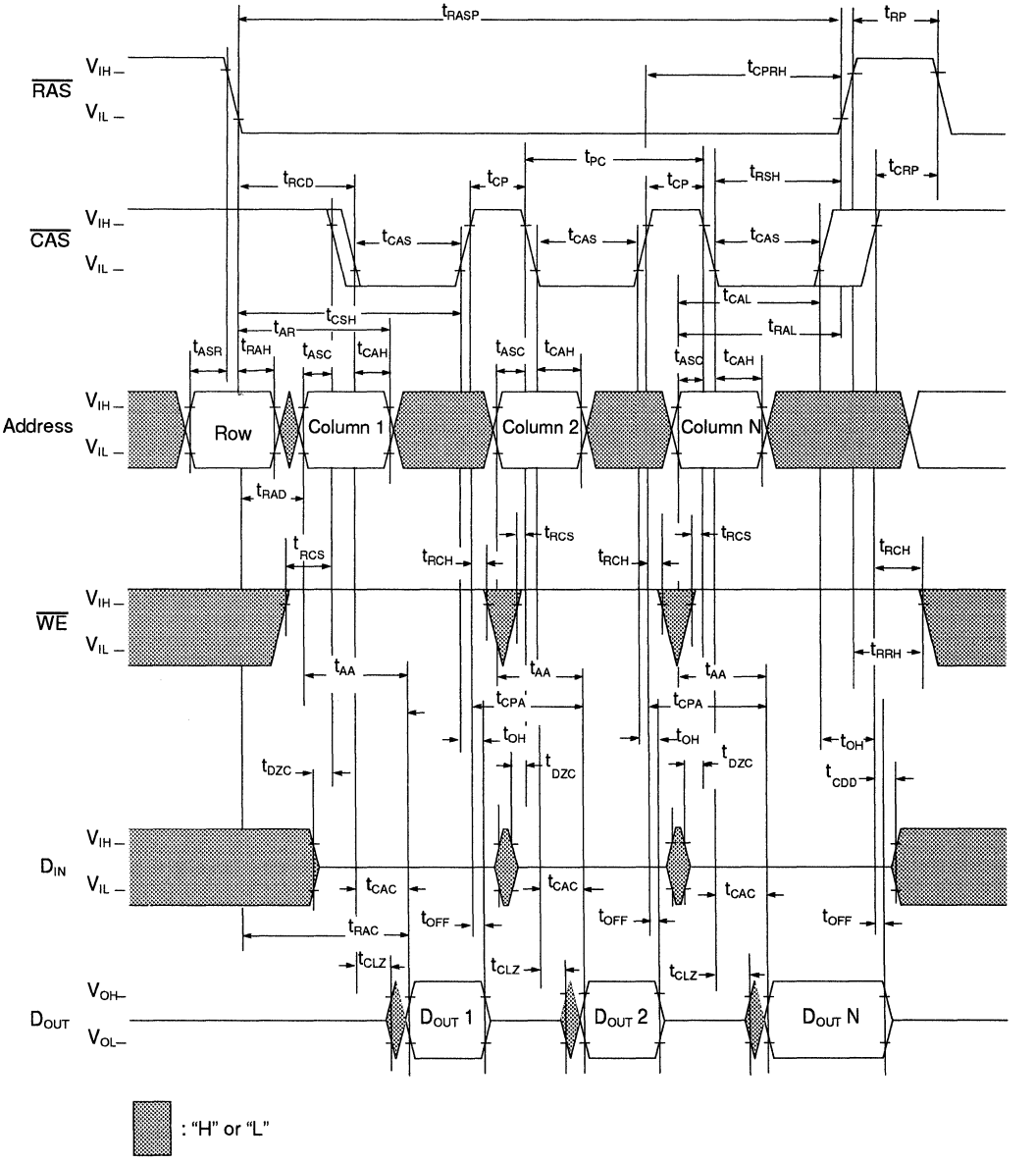
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Valid Data Out
tRAC
tOH
: "H" or "L"

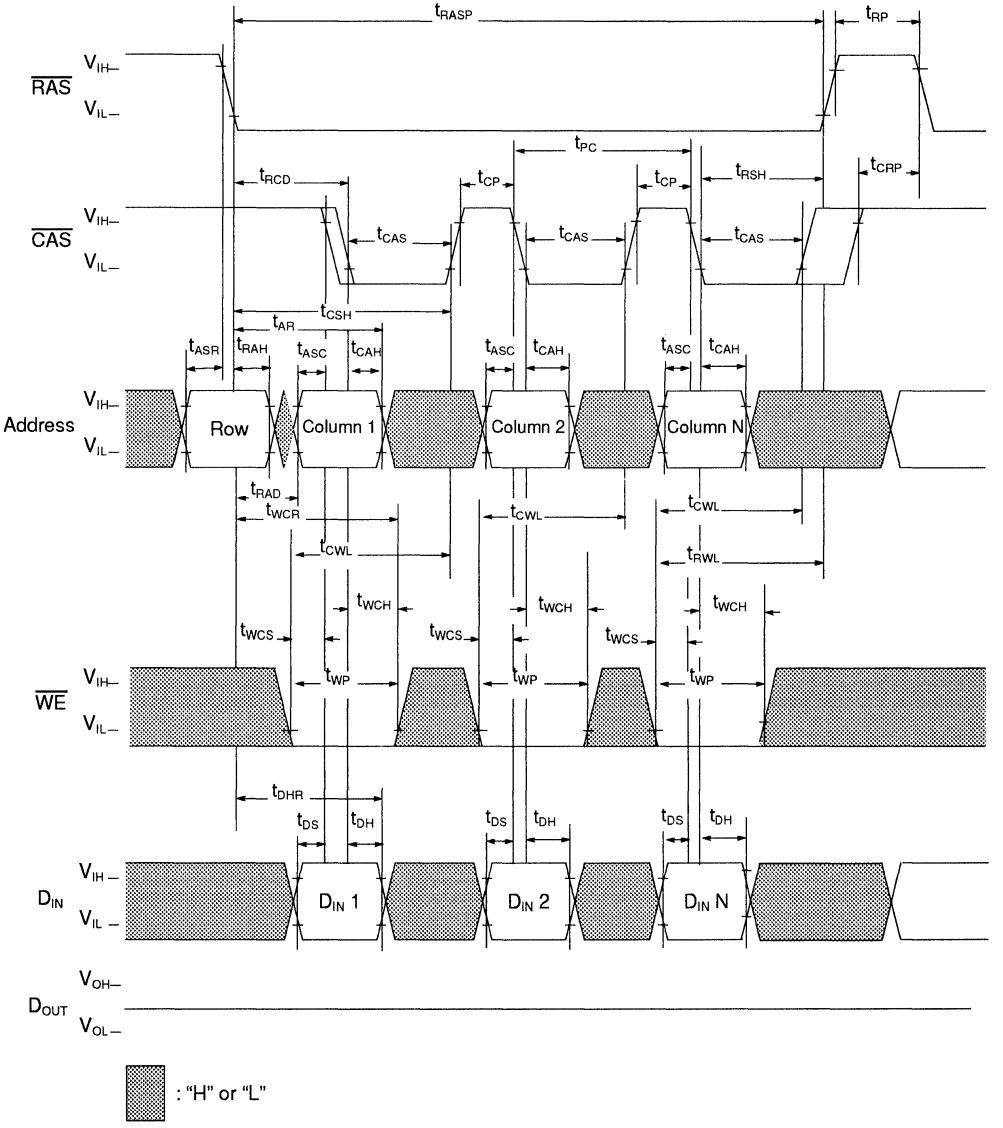
Write Cycle (Early Write)



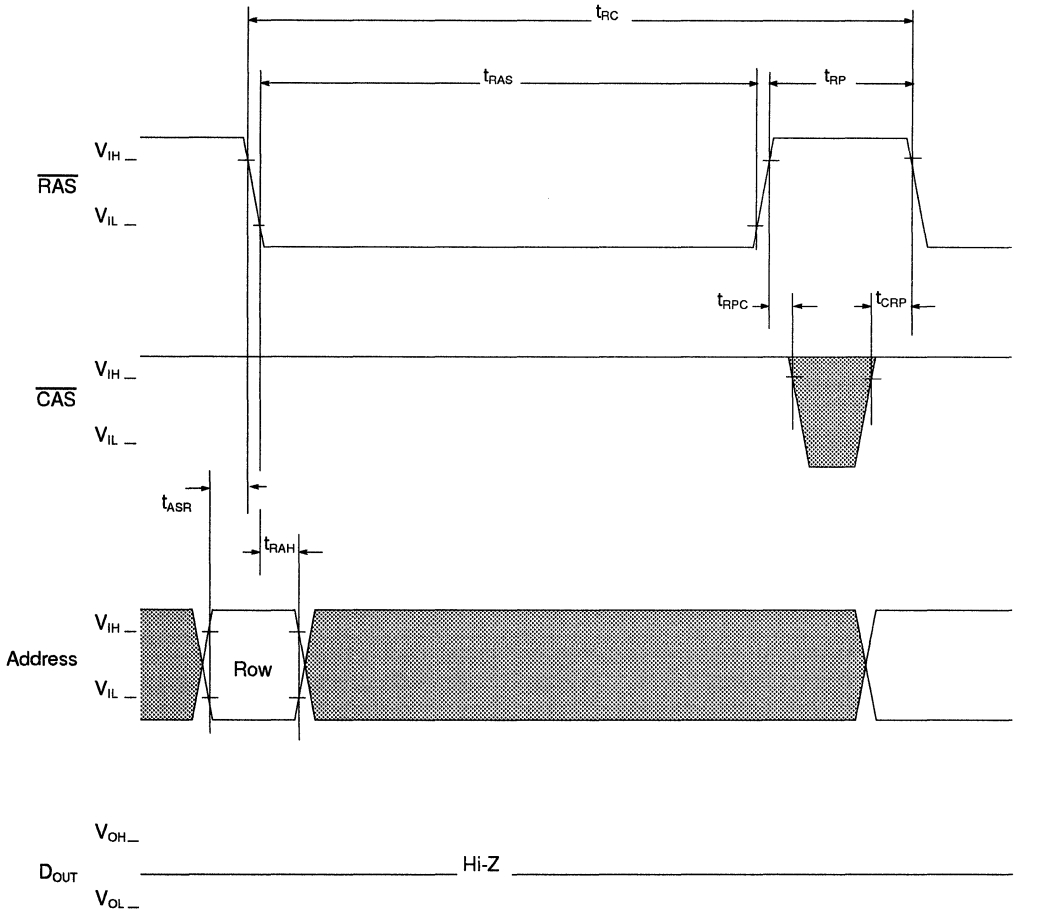
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

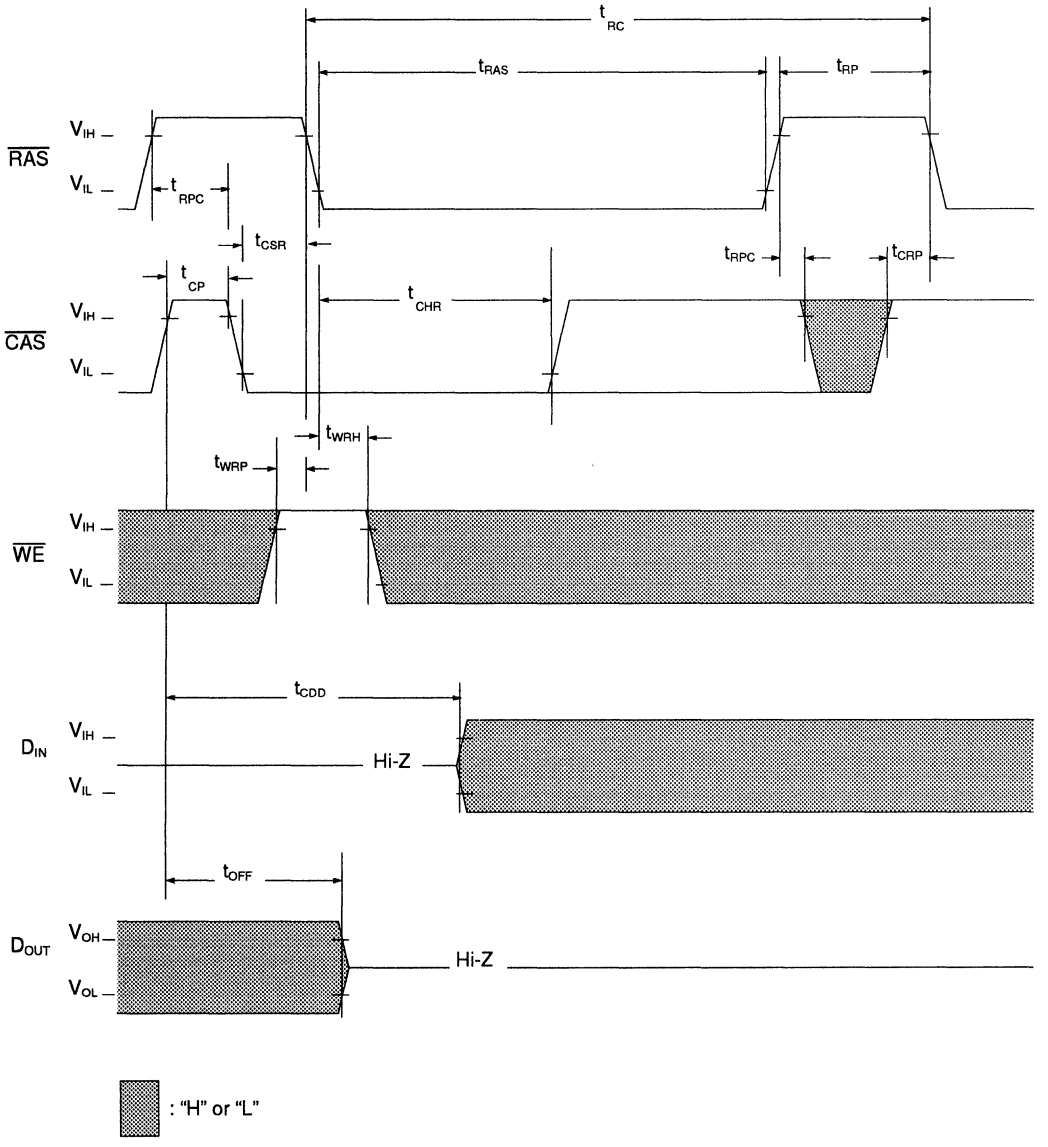


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, D_{IN} are "H" or "L"

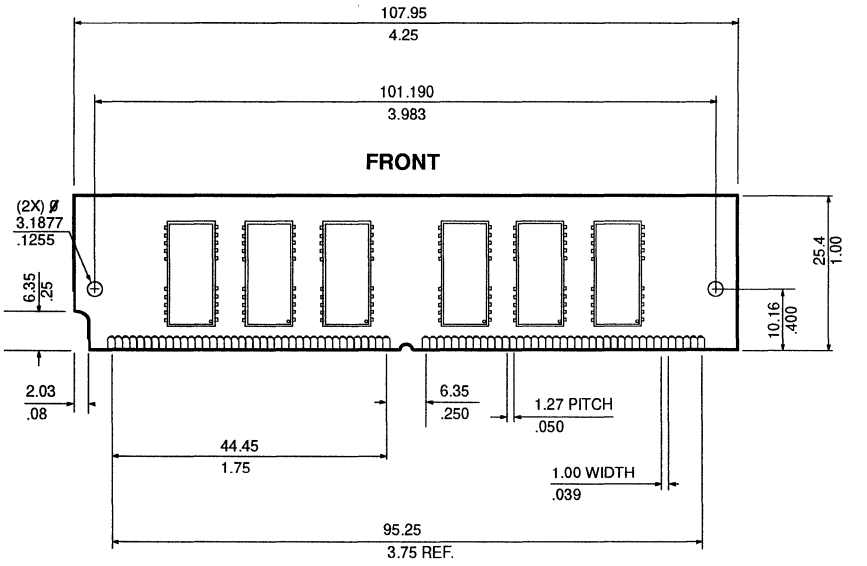
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

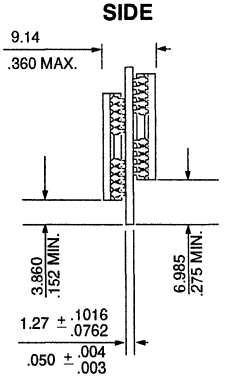


: "H" or "L"

Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

1M x 36 DRAM Module

Features

- 72-Pin Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

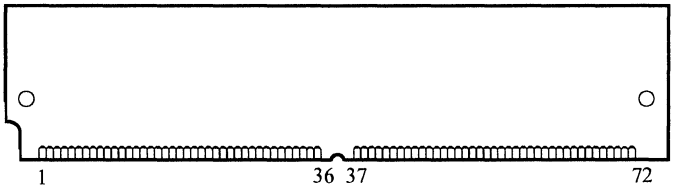
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write parity applications
- Au and Sn/Pb versions available

Description

The IBM11D1360EA is a 4MB 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 1Mx36 high speed memory array, and is intended for use in 36 and 72 bit applications where interleave of 9 or 18 bit words is not required. It is manufactured with 8 1Mx4 devices - each in either a 350mil or 300mil package, and 1 1Mx4 'Quad CAS' device for parity. The use of 'Quad CAS' devices allows the SIMM to be manufactured as a single-sided assembly, and provides reduced power dissipation.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 1Mx32 non-parity SIMM, IBM11D1320B, as well as higher density and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

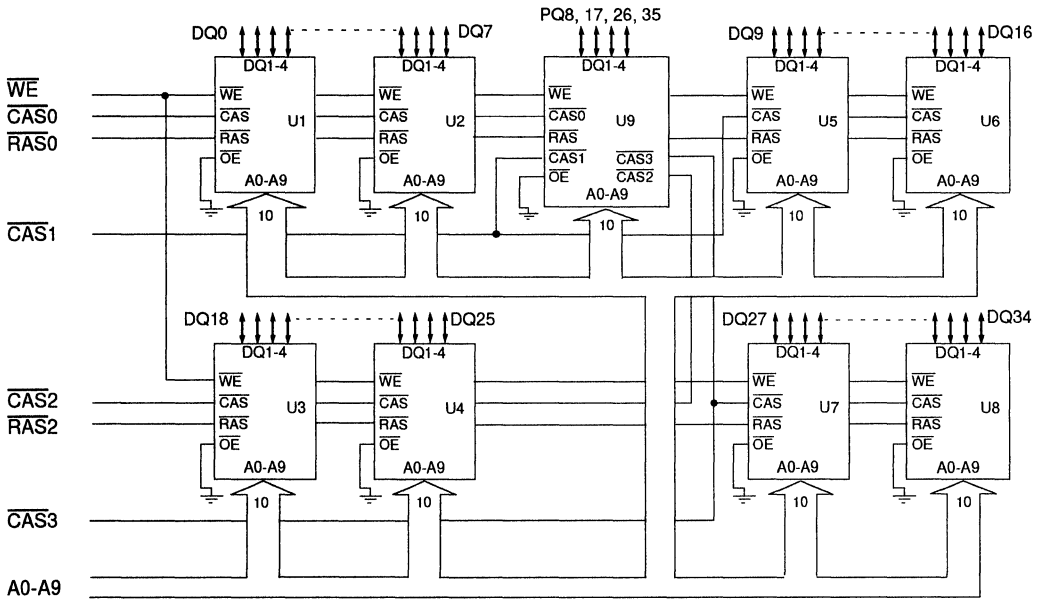
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D1360EA-60	1M x 36	60ns	Sn/Pb	4.25" x 1" x .205"	
IBM11D1360EA-70	1M x 36	70ns	Sn/Pb	4.25" x 1" x .205"	
IBM11E1360EA-60	1M x 36	60ns	Au	4.25" x 1" x .205"	
IBM11E1360EA-70	1M x 36	70ns	Au	4.25" x 1" x .205"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 6.5	V	1
V_{IN}	Input Voltage	-0.7 to V_{CC} + 0.7	V	1
V_{OUT}	Output Voltage	-0.7 to V_{CC} + 0.7	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	5.8	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	46	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$0)	40	pF	
C_{I3}	Input Capacitance ($\overline{RAS}$2)	31	pF	
C_{I4}	Input Capacitance ($\overline{CAS}$)	26	pF	
C_{I5}	Input Capacitance ($\overline{WE}$)	46	pF	
$C_{I/O}$	Output Capacitance (All DQ, PQ)	12	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1060	mA	1, 2, 3
		-70	—	954		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	18.5	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	1060	mA	1, 3
		-70	—	954		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	670	mA	1, 2, 3
		-70	—	620		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	17	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1060	mA	1, 3
		-70	—	954		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$0	-50	+50		
		$\overline{RAS}$2	-40	+40	µA	
		$\overline{CAS}$	-30	+30		
		All others	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -4mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. The 1Mx4 DRAM Outputs will remain disabled until these 8 cycles have occurred. This prevents data contention (excessive current) during power on. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	1
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	—	—	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{CLCH}	Hold Time $\overline{CAS}$ Low to $\overline{CAS}$ High	10	—	10	—	ns	5
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	

1. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	45	—	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	10	—	15	—	ns	

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

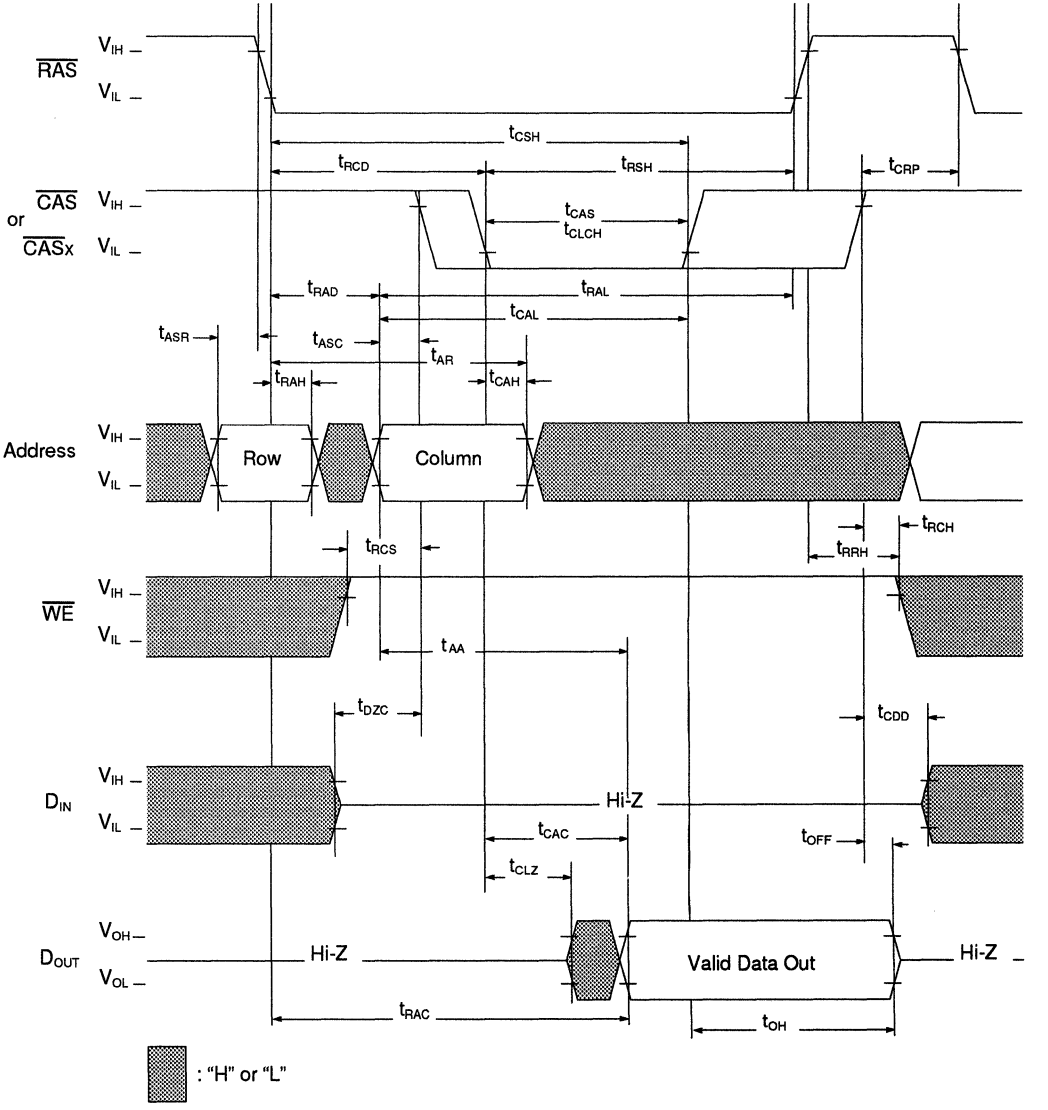
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Measured with the specified current load and 100pF.

Refresh Cycle

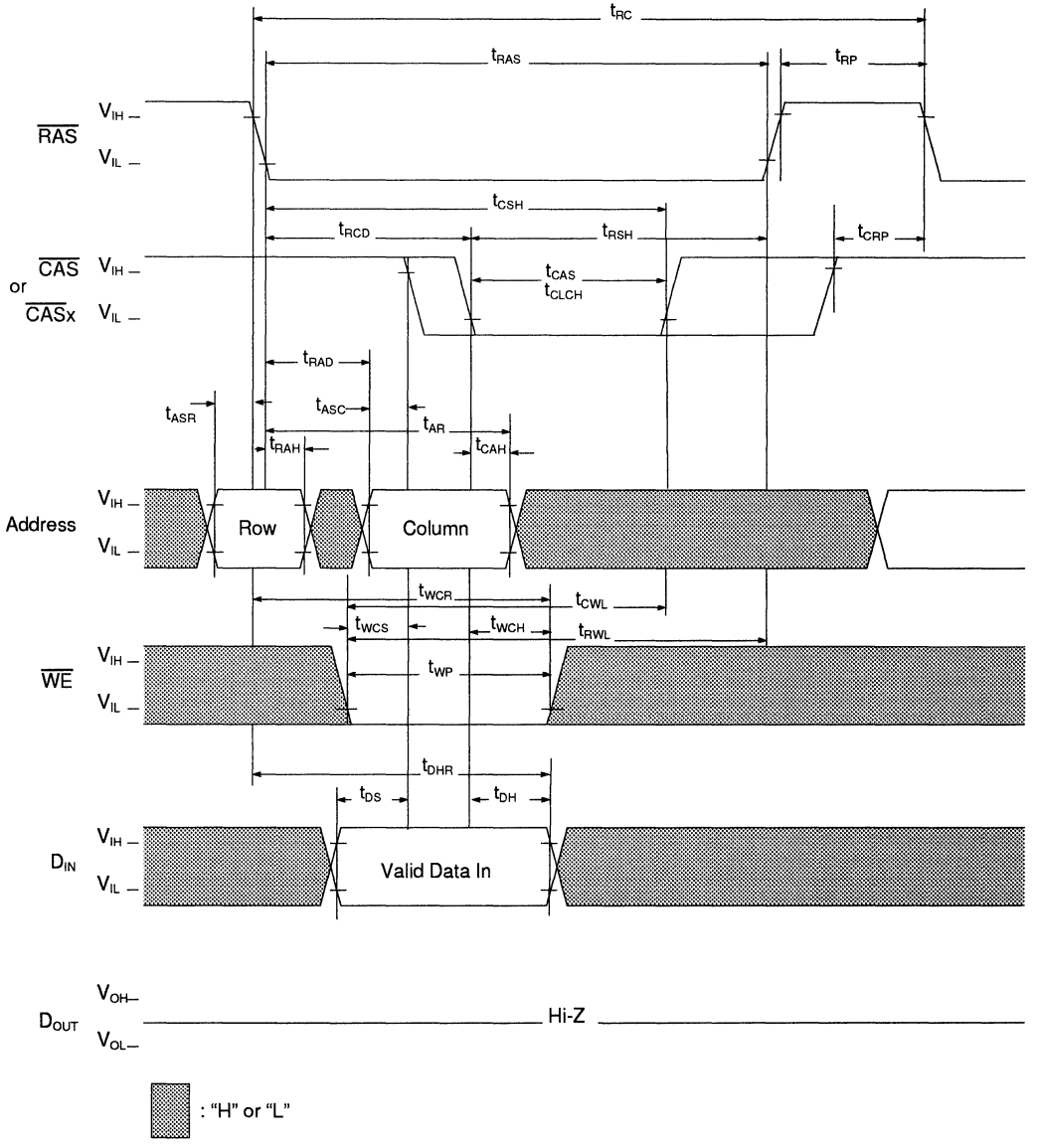
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms. The DC variation in the V_{CC} supply may not exceed 300mV within a refresh interval (16ms).

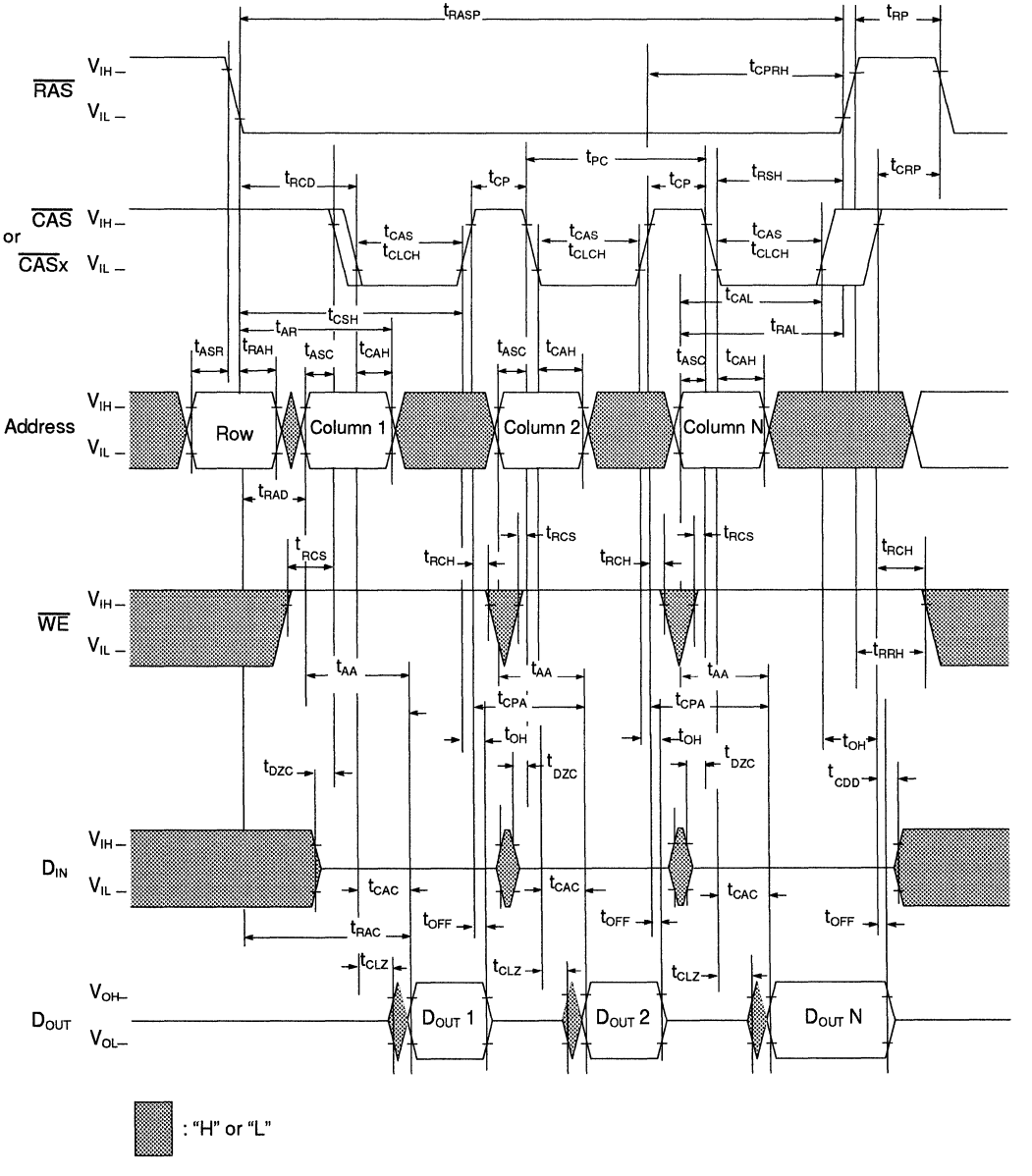
Read


RAS
CAS
or
CASx
Address
WE
DIN
DOUT
VIH
VIL
VOH
VOL
tCSH
tRCD
tRSH
tCRP
tCAS
tCLCH
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Row
Column
tRCS
tRCH
tRRH
tAA
tDZC
tCDD
Hi-Z
tCAC
tOFF
tCLZ
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

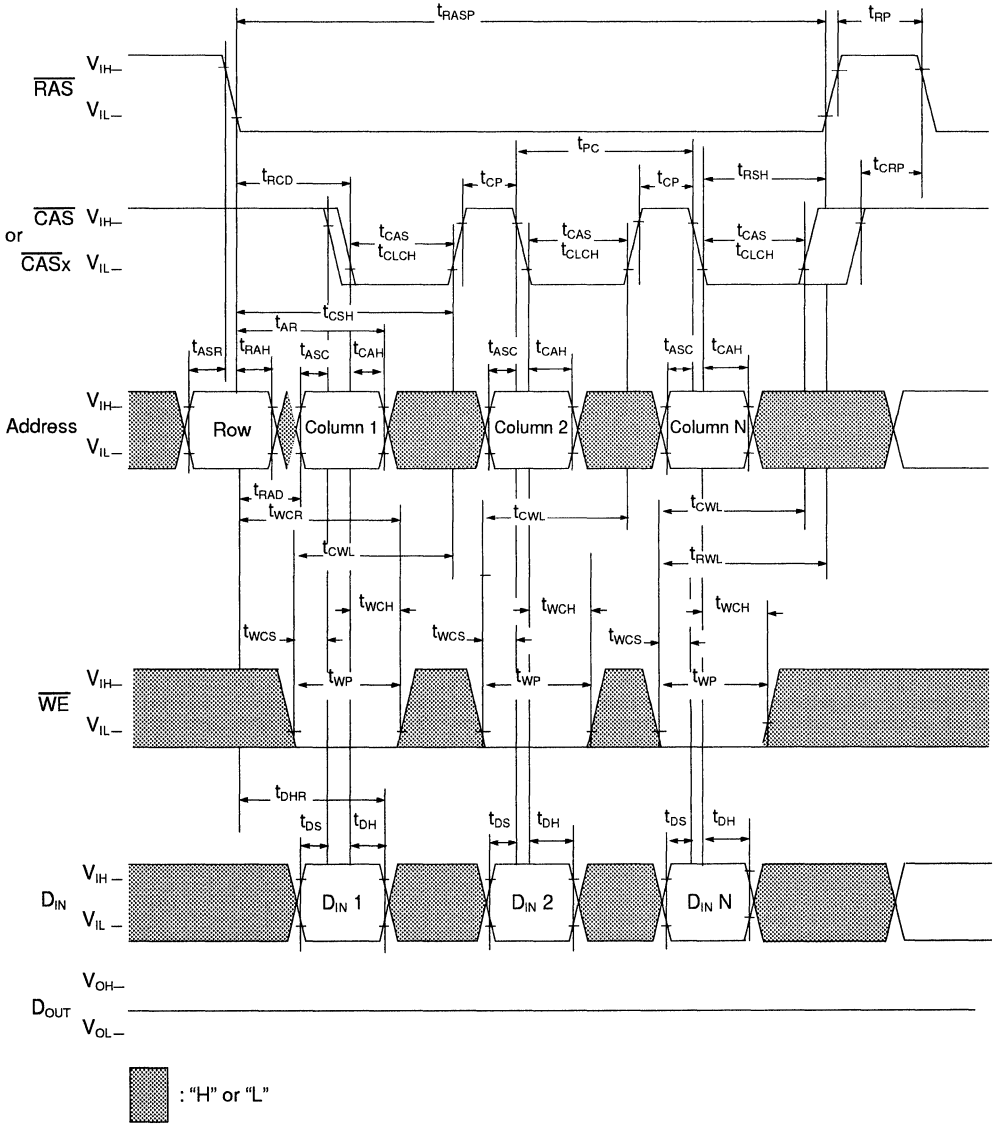
Write Cycle (Early Write)



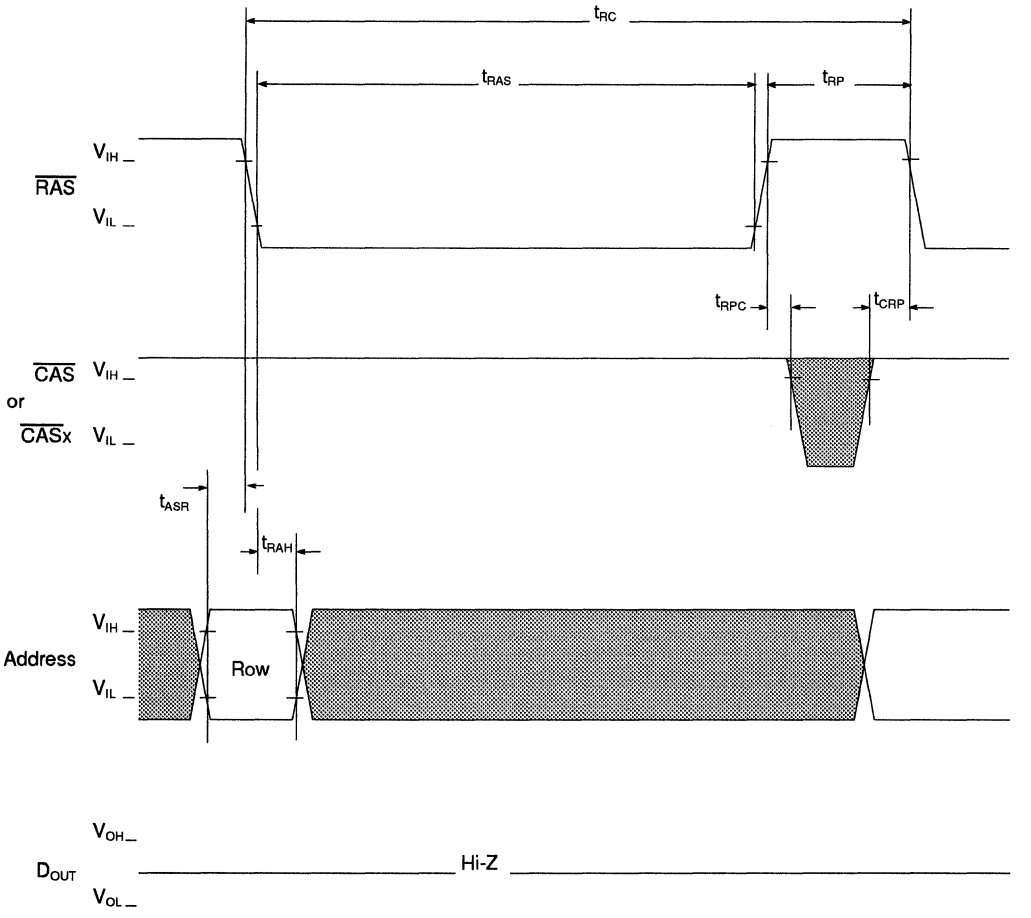
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

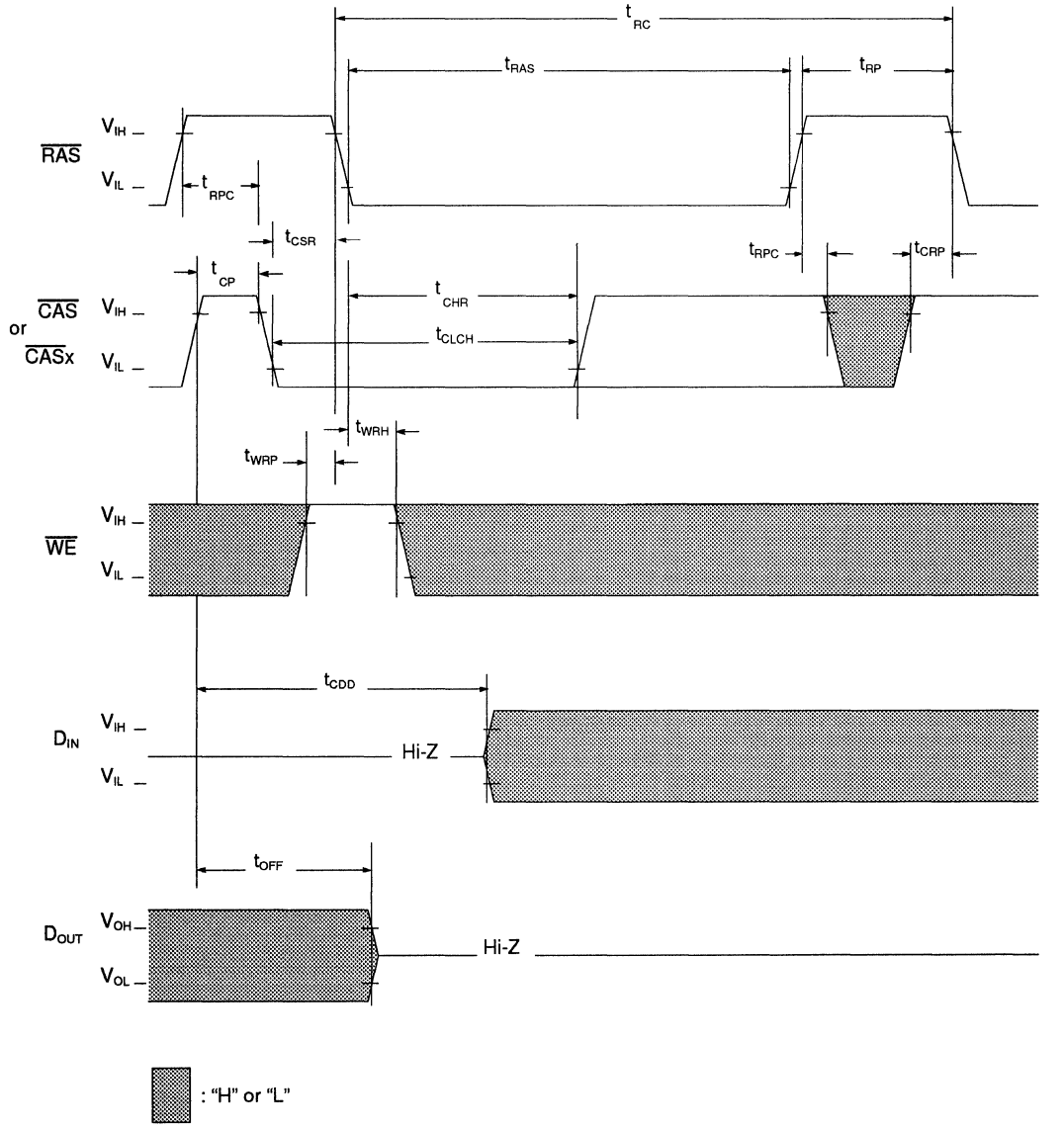


$\overline{RAS}$ Only Refresh Cycle



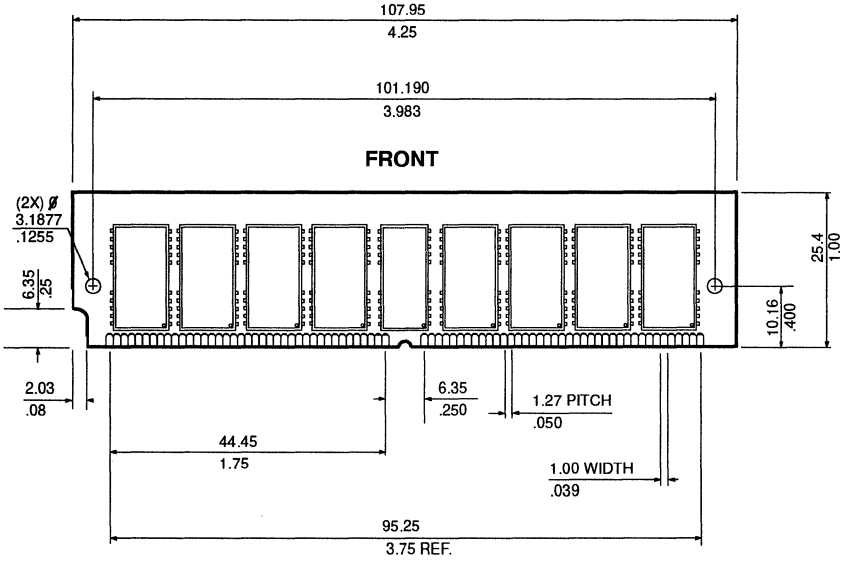
Note: $\overline{WE}$, D_{IN} are "H" or "L"

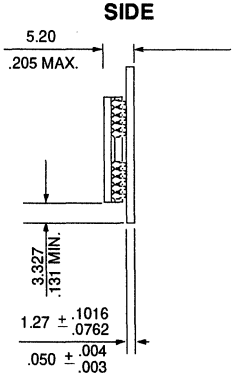
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 72-Pin Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

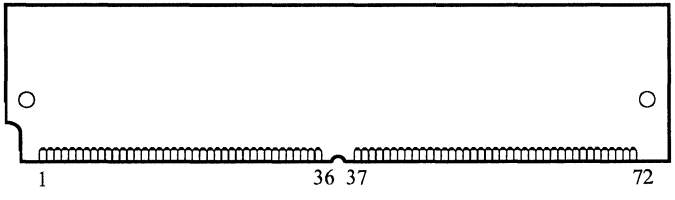
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Low active current dissipation
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write parity applications
- Au and Sn/Pb versions available

Description

The IBM11D1360EA is a 4MB 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 1Mx36 high speed memory array, and is intended for use in 36 and 72 bit applications where interleave of 9 or 18 bit words is not required. It is manufactured with 8 1Mx4 devices - each in a 300mil package, and 1 1Mx4 'Quad CAS' device for parity. The use of 'Quad CAS' devices allows the SIMM to be manufactured as a single-sided assembly, and provides reduced power dissipation.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 1Mx32 non-parity SIMM, IBM11D1320B, as well as higher density and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

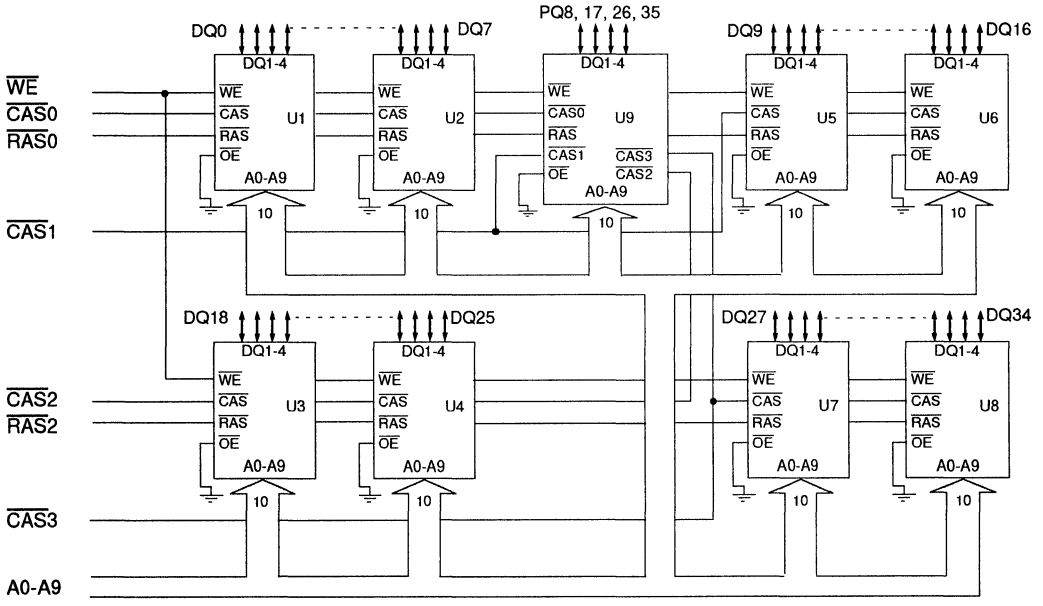
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D1360ED-60	1M x 36	60ns	Sn/Pb	4.25" x 1" x .205"	
IBM11D1360ED-70	1M x 36	70ns	Sn/Pb	4.25" x 1" x .205"	
IBM11E1360ED-60	1M x 36	60ns	Au	4.25" x 1" x .205"	
IBM11E1360ED-70	1M x 36	70ns	Au	4.25" x 1" x .205"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +6.0	V	1
V_{IN}	Input Voltage	-1.0 to +6.0	V	1
V_{OUT}	Output Voltage	-1.0 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	4.3	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	55	pF	
C_{I2}	Input Capacitance ($\overline{RAS0}$)	47	pF	
C_{I3}	Input Capacitance ($\overline{RAS2}$)	43	pF	
C_{I4}	Input Capacitance ($\overline{CAS}$)	30	pF	
C_{I5}	Input Capacitance ($\overline{WE}$)	70	pF	
$C_{I/O}$	Output Capacitance (All DQ, PQ)	12	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	780	mA	1, 2, 3
		-70	—	650		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	18	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	780	mA	1, 3
		-70	—	650		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	550	mA	1, 2, 3
		-70	—	460		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	9	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	780	mA	1, 3
		-70	—	650		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$0	-50	+50	µA	
		$\overline{RAS}$2	-40	+40		
		$\overline{CAS}$	-30	+30		
		All others	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	1
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{CLCH}	Hold Time $\overline{CAS}$ Low to $\overline{CAS}$ High	10	—	10	—	ns	4
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	

1. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	45	—	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

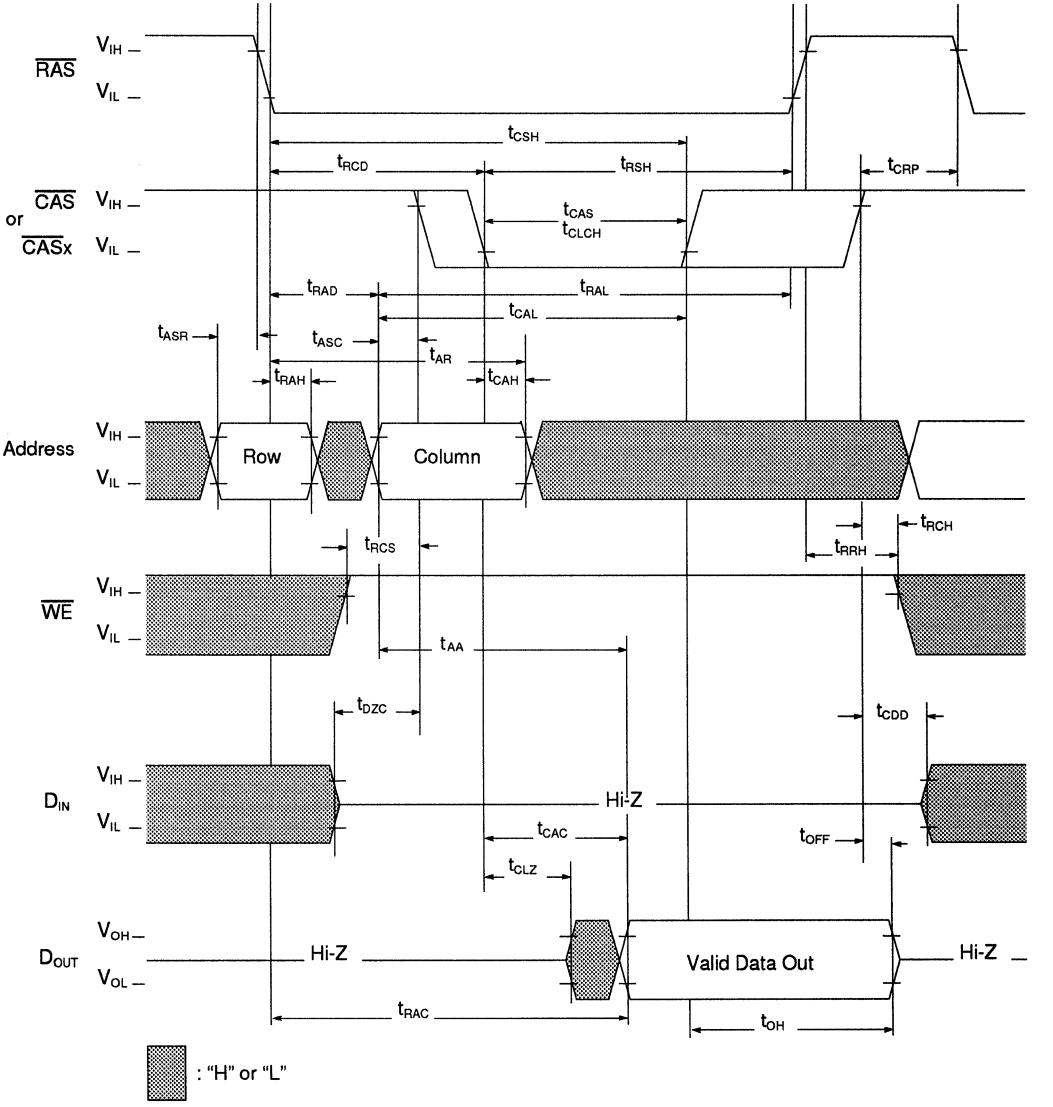
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Measured with the specified current load and 100pF.

Refresh Cycle

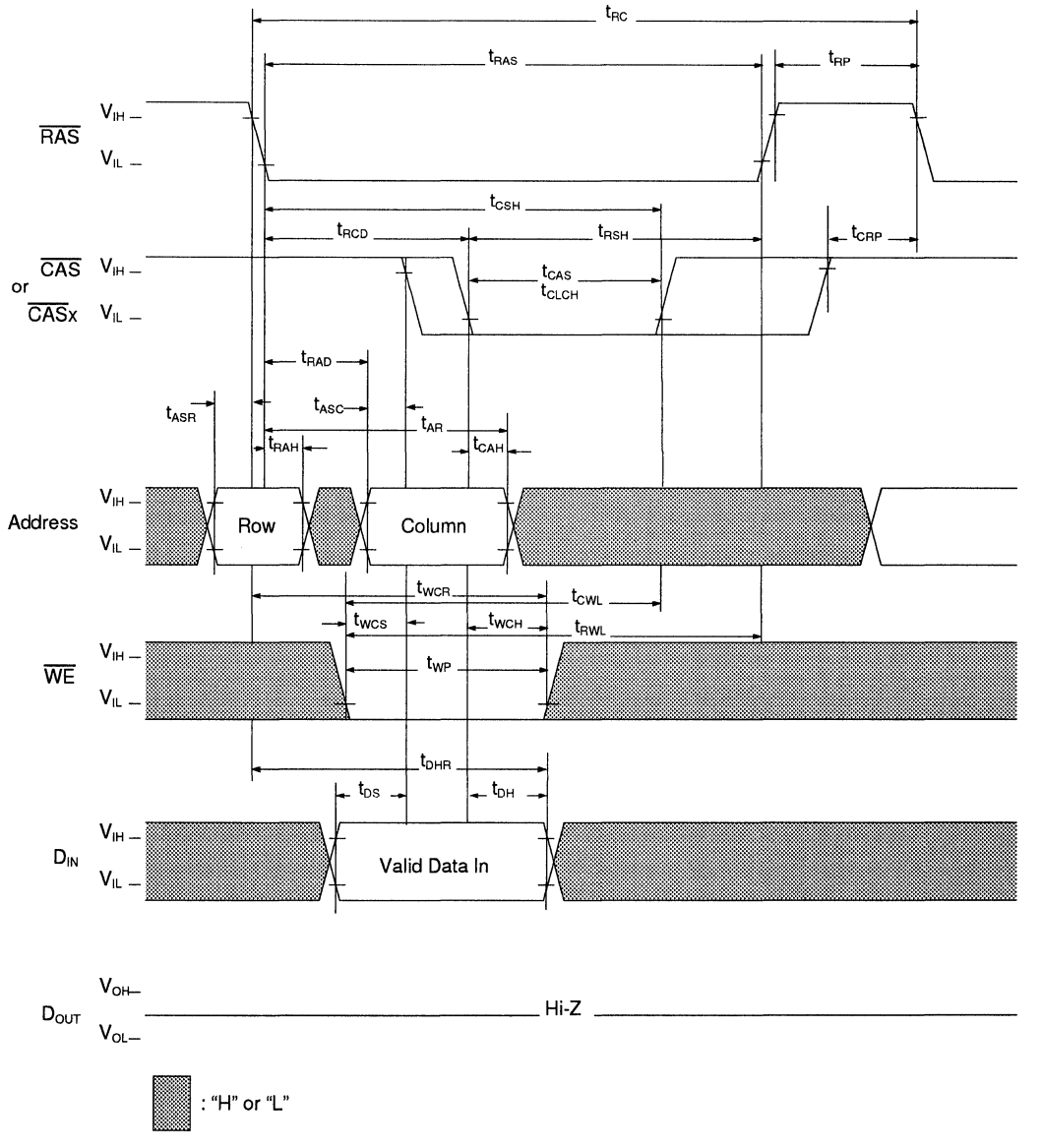
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	15	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms.

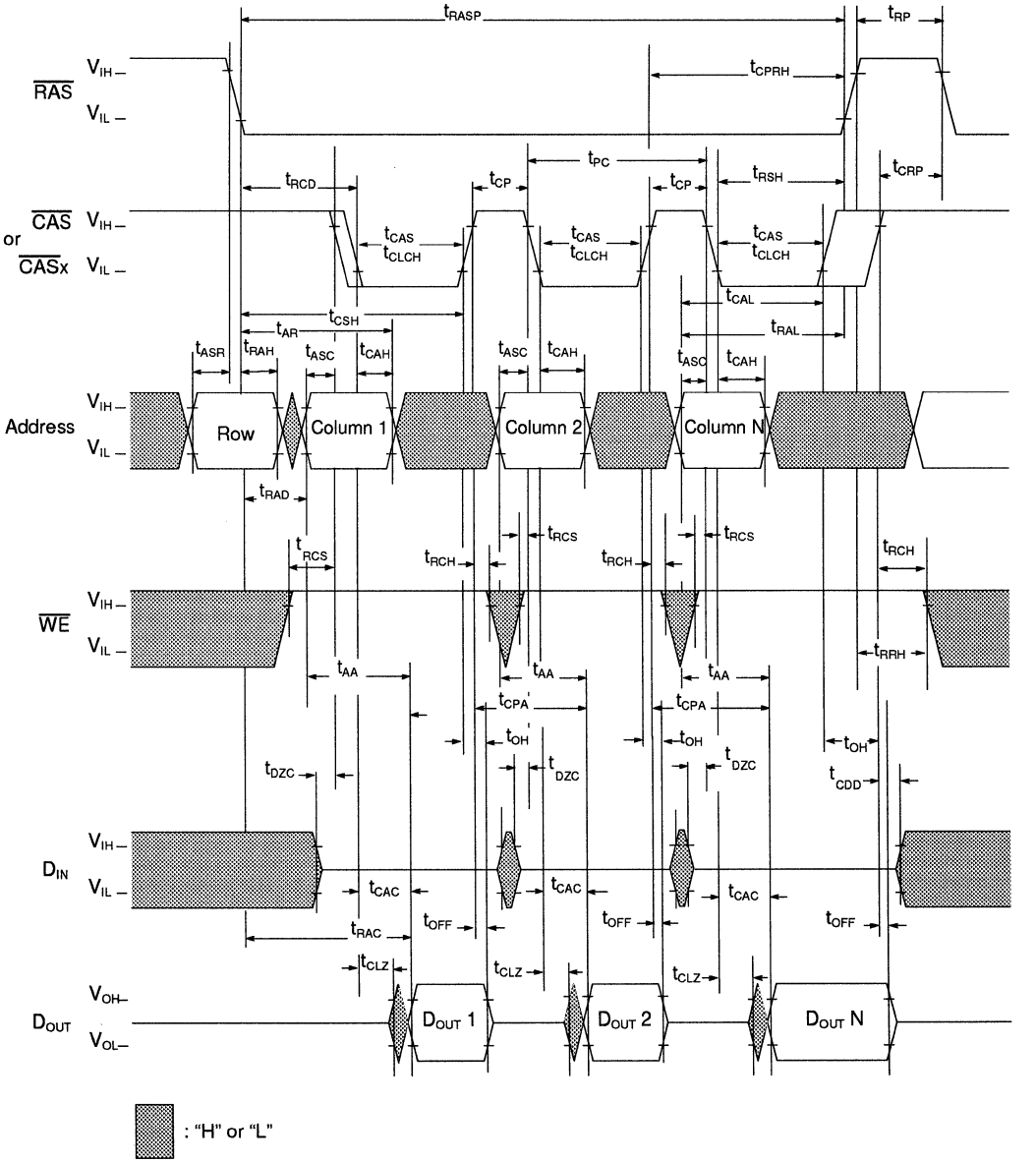
Read


RAS
CAS
or
CASx
Address
WE
DIN
DOUT
VIH
VIL
VOH
VOL
tCSH
tRCD
tRSH
tCRP
tCAS
tCLCH
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Row
Column
tRCS
tRCH
tRRH
tAA
tDZC
tCDD
Hi-Z
tCAC
tOFF
tCLZ
Valid Data Out
tRAC
tOH
: "H" or "L"

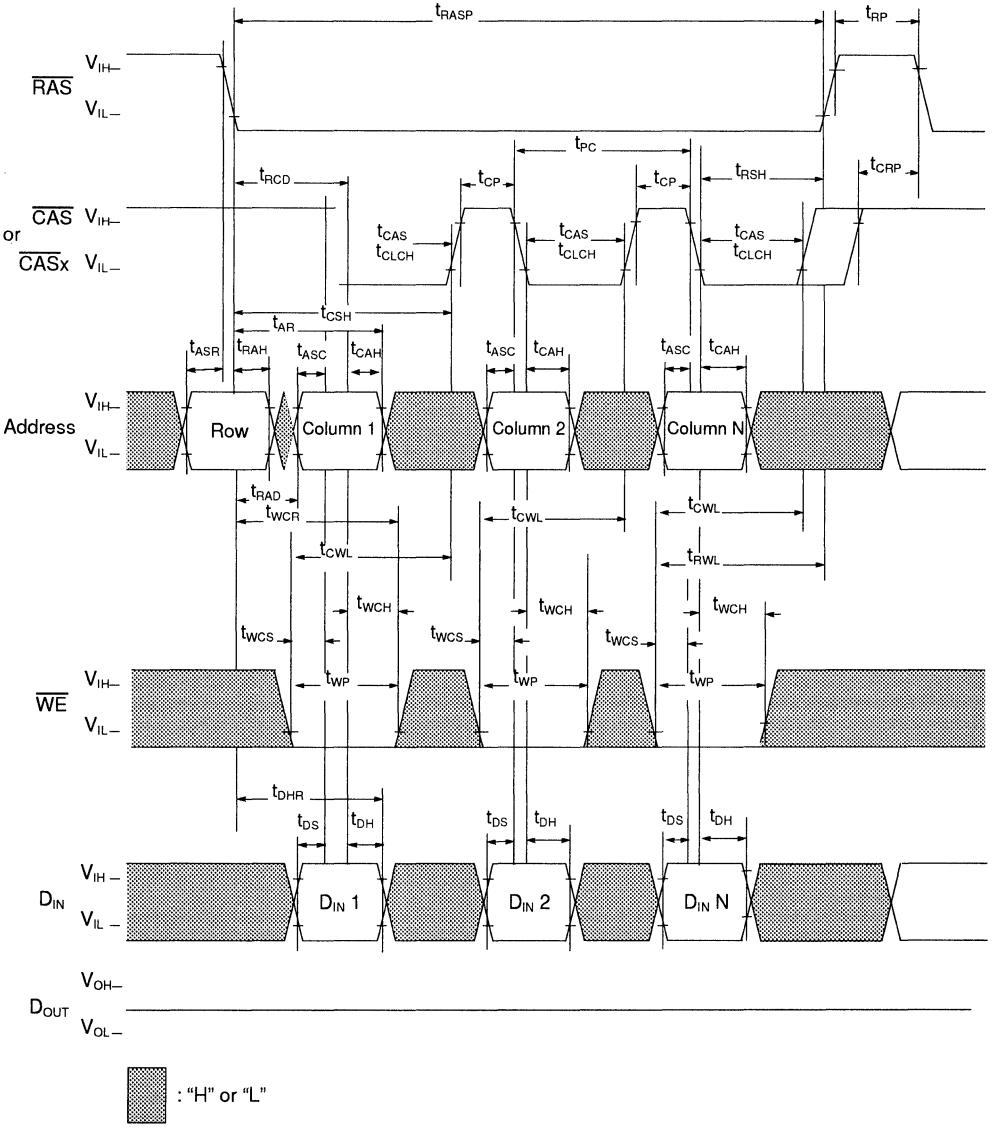
Write Cycle (Early Write)



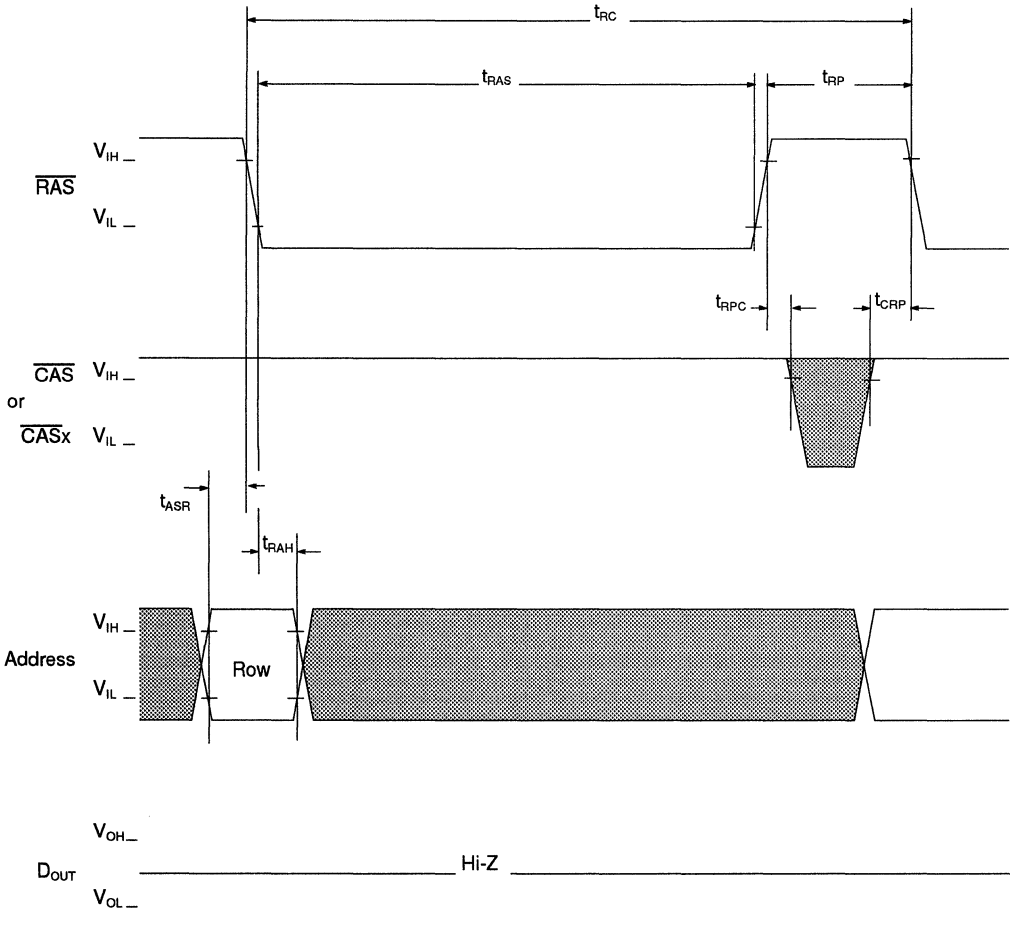
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

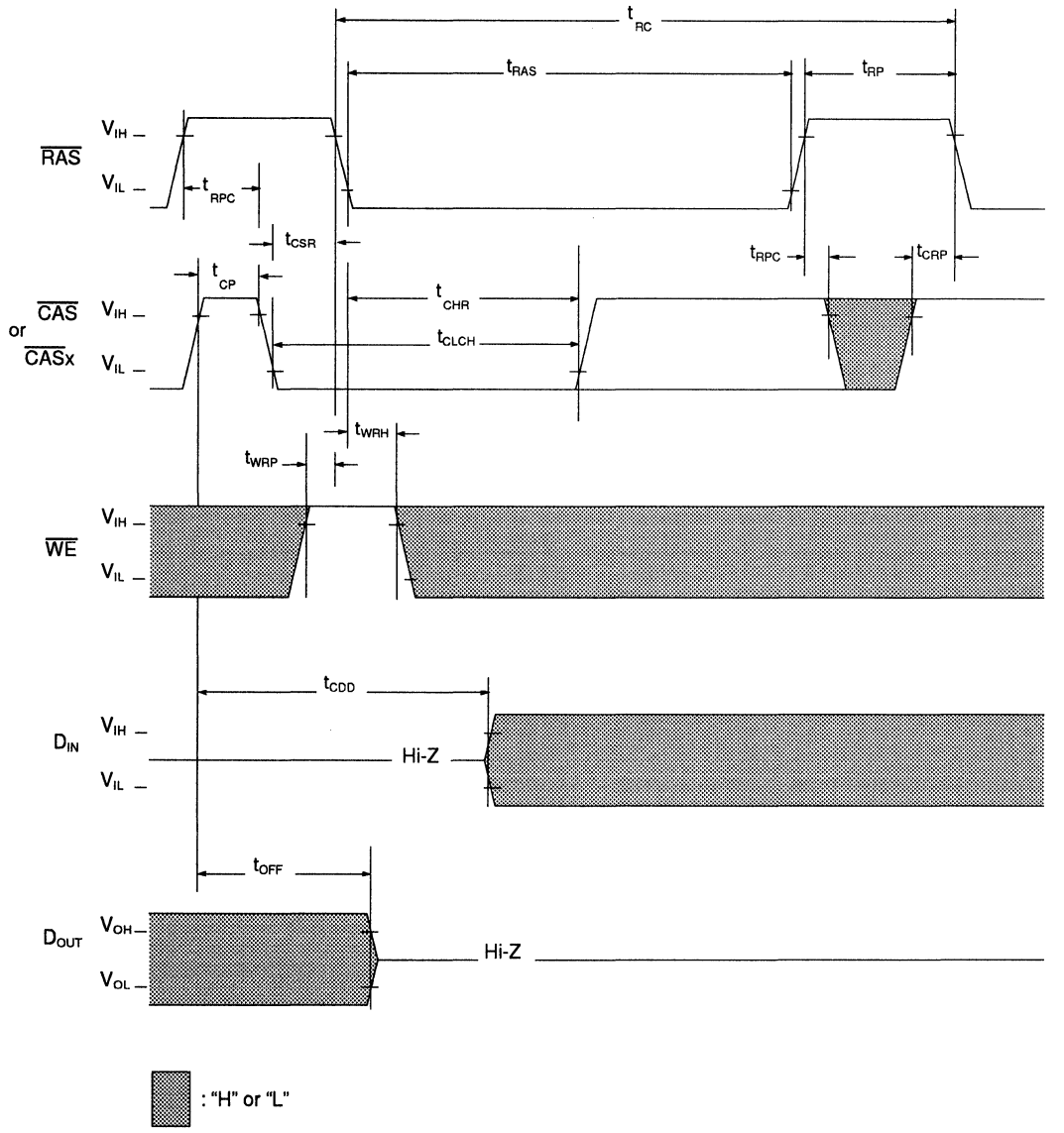


$\overline{RAS}$ Only Refresh Cycle



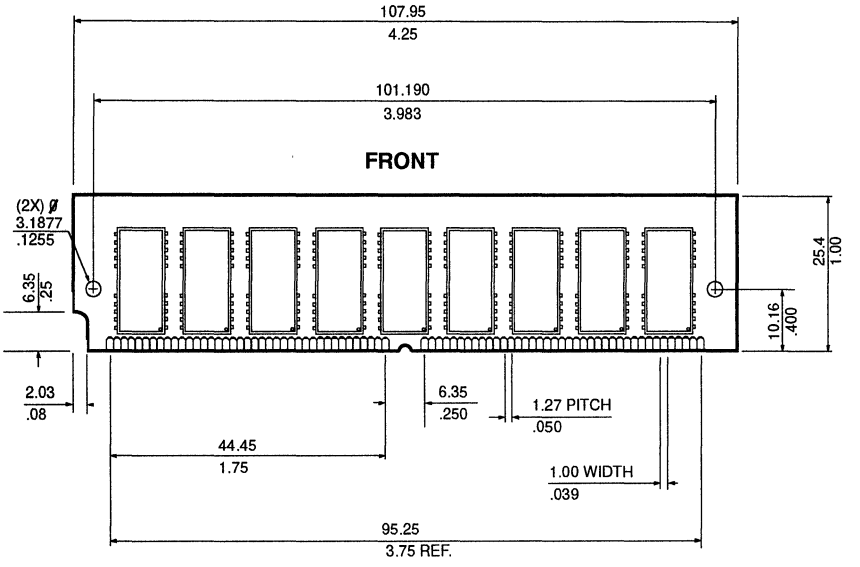
Note: $\overline{WE}$, D_{IN} are "H" or "L"

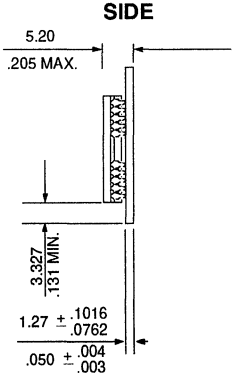
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Manufactured with 18Mb DRAMS (1M x 18)
- Single 5V, ± 0.5V Power Supply
- Low current consumption
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write parity applications.
- Au and Sn/Pb versions available

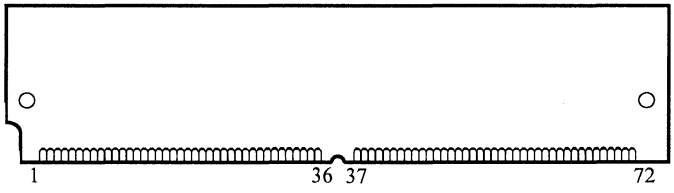
Description

The IBM11D1360L is a 4MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 1Mx36 high speed memory array that is intended for use in 18, 36 and 72 bit applications. It is manufactured with 2 1Mx18 devices, each in a 400mil TSOP package, and is compatible with the JEDEC 72-Pin SIMM standard.

This assembly is intended as a direct replacement for 1Mx4-based SIMMs, while significantly reducing power dissipation. The use of TSOP packages allows tighter SIMM spacing (.3" on center). Input loading is consistent with 4Mb-based assemblies due to the addition of discrete capacitors - maximizing compatibility at the system-level.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 1Mx36 parity SIMM, IBM11D1360B, as well as higher density, parity and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

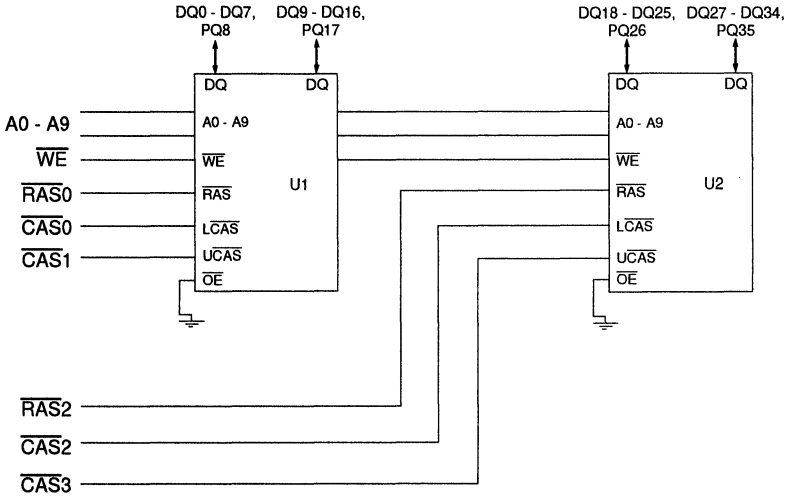
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D1360LA-60	1M x 36	60ns	Sn/Pb	4.25" x 1" x .104"	
IBM11D1360LA-70	1M x 36	70ns	Sn/Pb	4.25" x 1" x .104"	
IBM11E1360LA-60	1M x 36	60ns	Au	4.25" x 1" x .104"	
IBM11E1360LA-70	1M x 36	70ns	Au	4.25" x 1" x .104"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	2.3	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	47	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	32	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	17	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	50	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34, PQ8, PQ17, PQ26, PQ35)	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	420	mA	1, 2, 3
		-70	—	370		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	4	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	420	mA	1, 3
		-70	—	370		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	180	mA	1, 2, 3
		-70	—	160		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	2	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	420	mA	1, 3
		-70	—	370		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-10	+10	µA	
		$\overline{CAS}$	-10	+10		
		All others	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

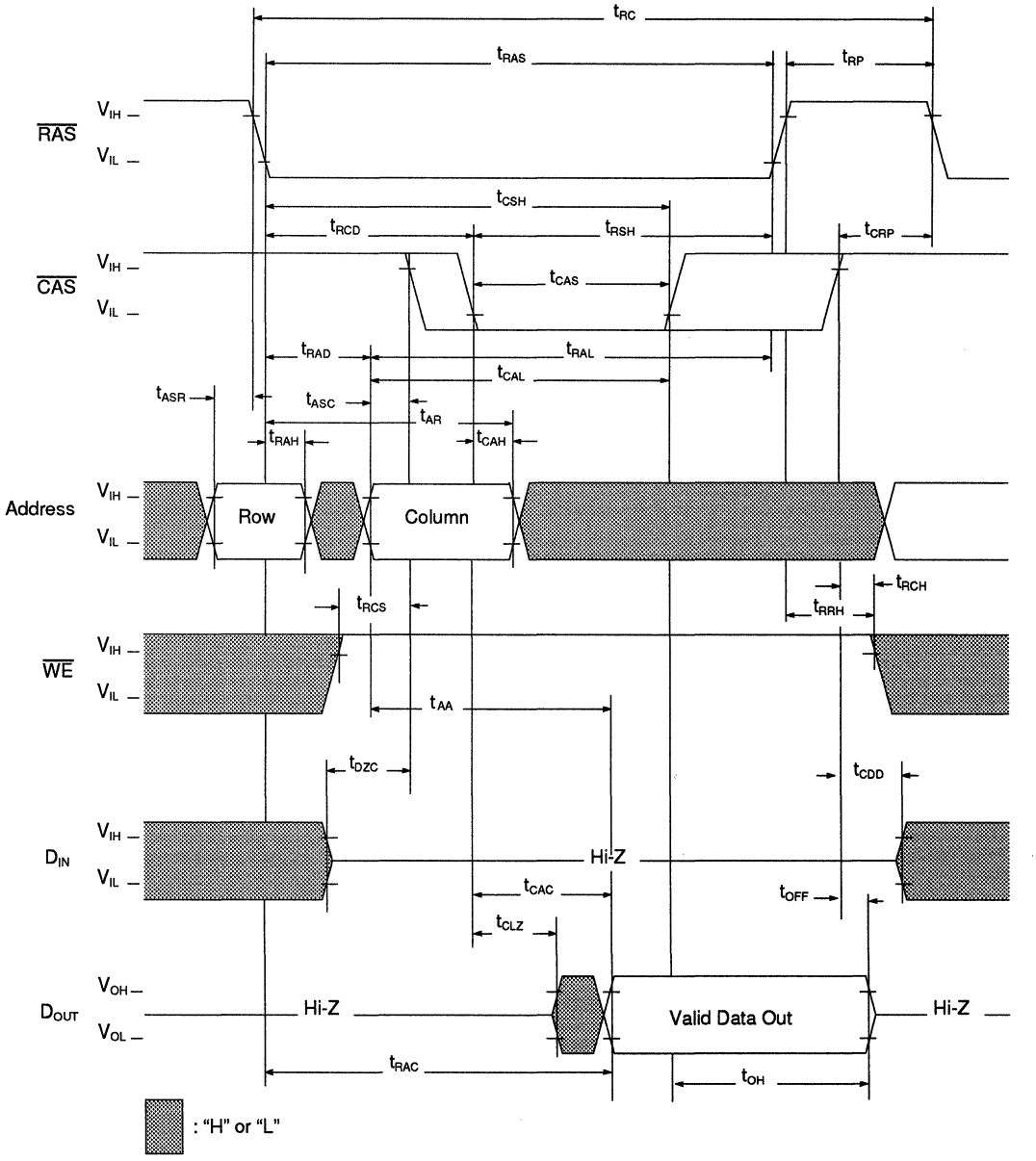
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

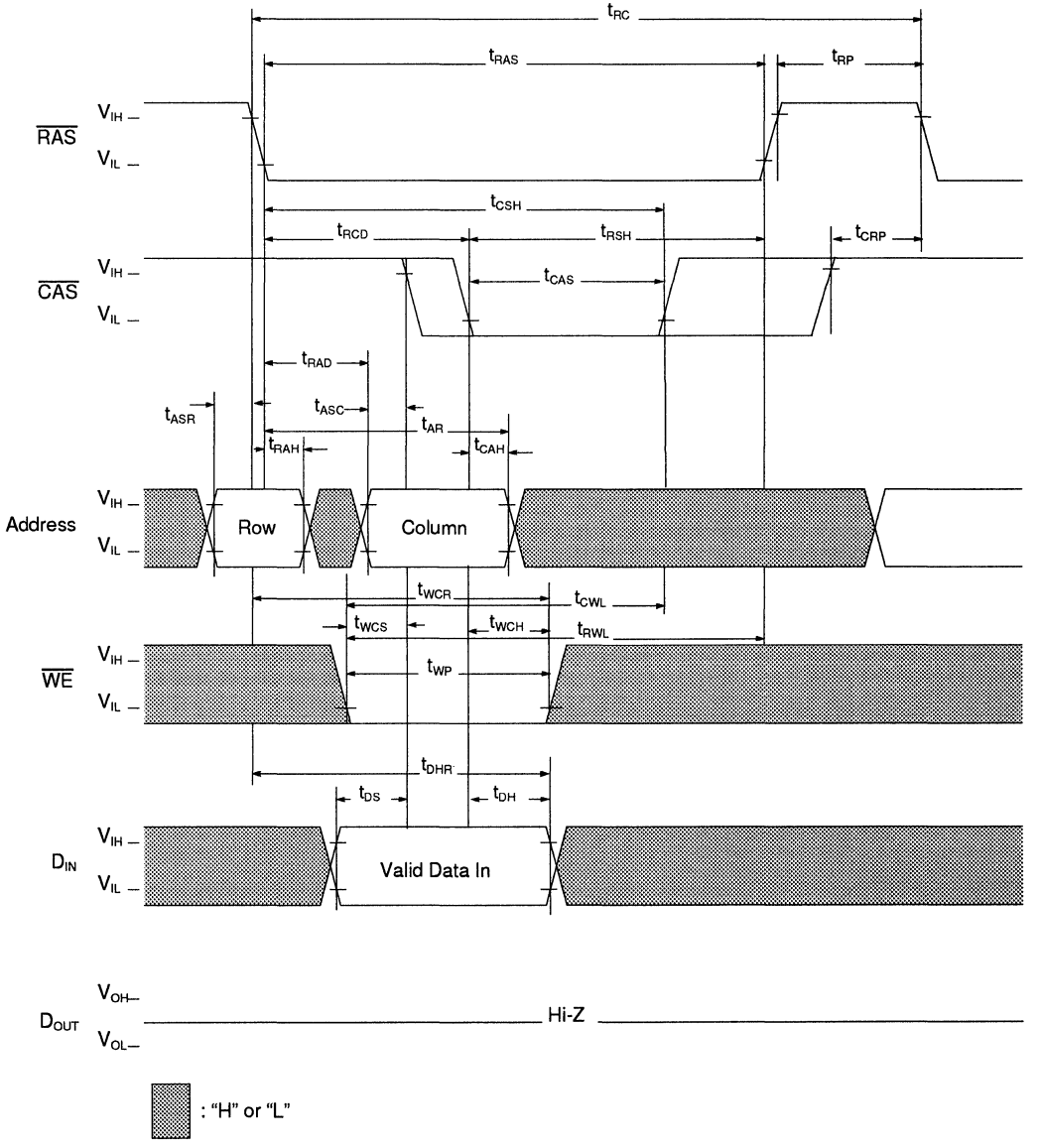
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms.

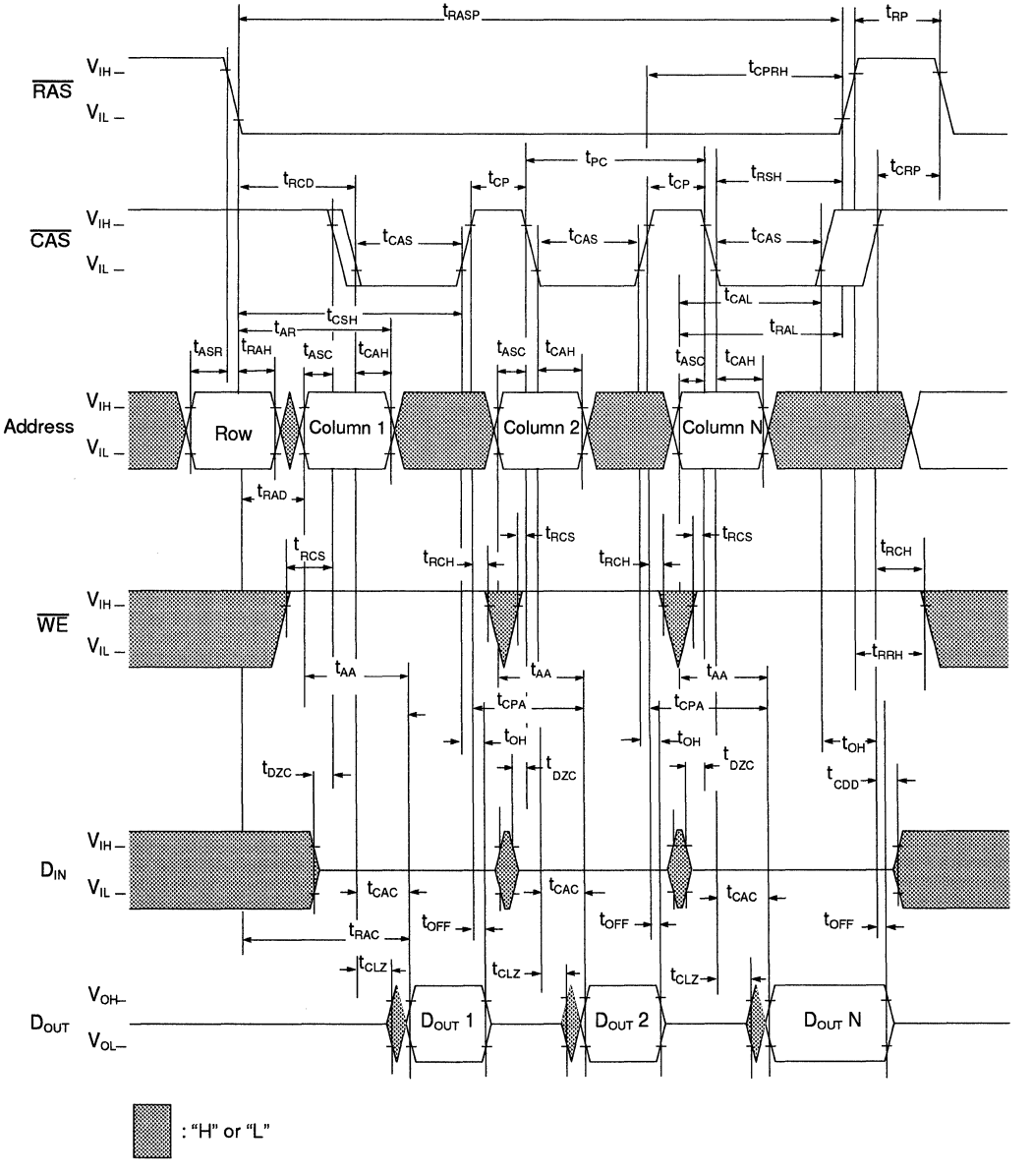
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRRH
tRCH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

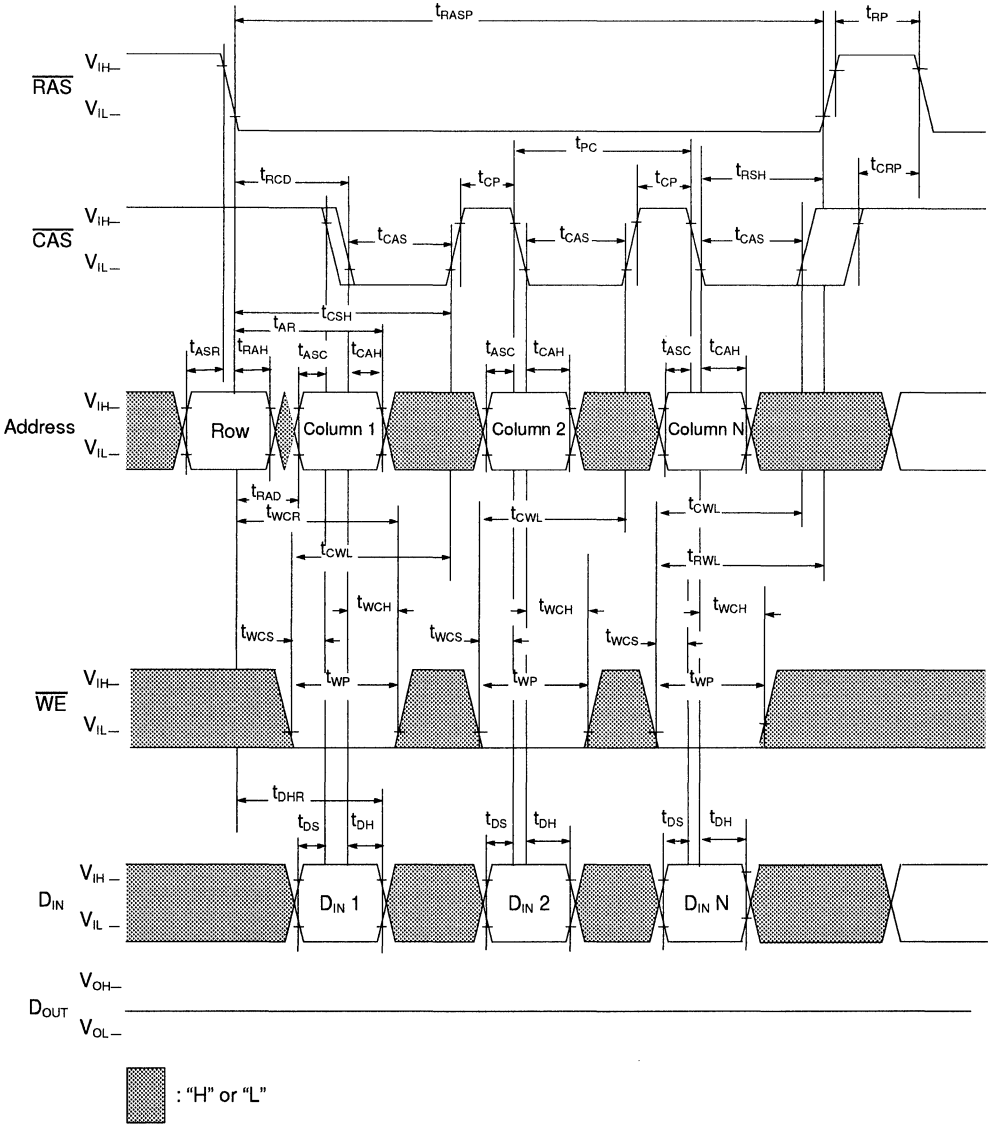
Write Cycle (Early Write)



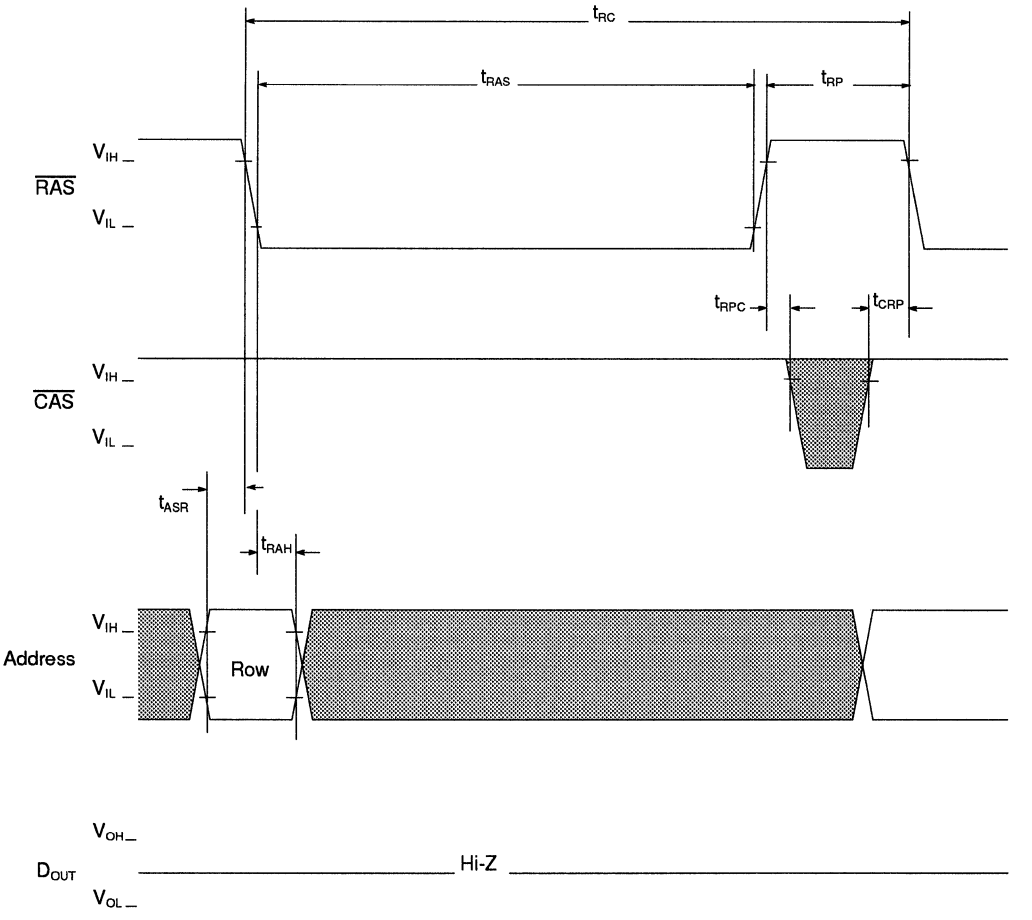
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

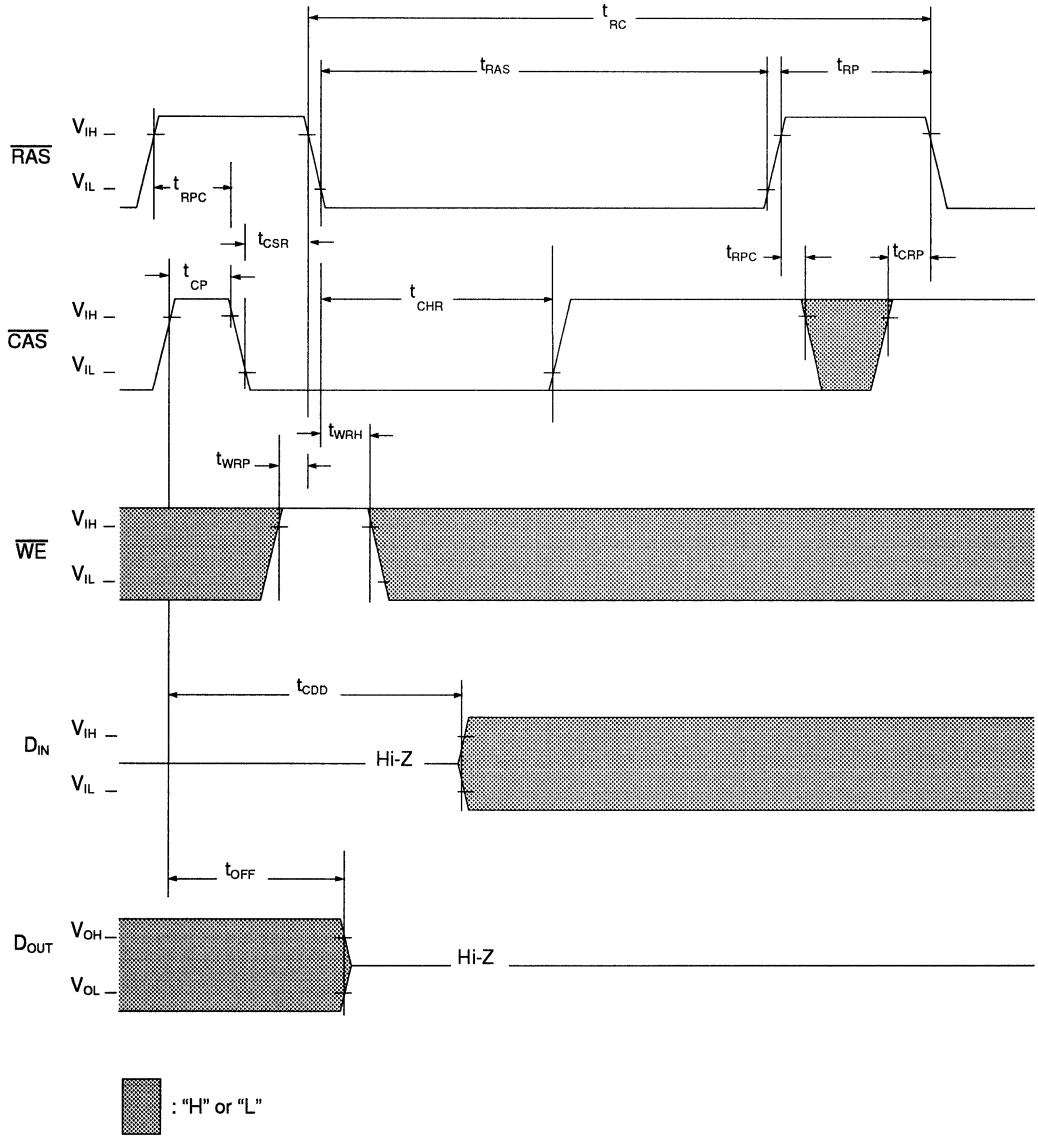


$\overline{RAS}$ Only Refresh Cycle



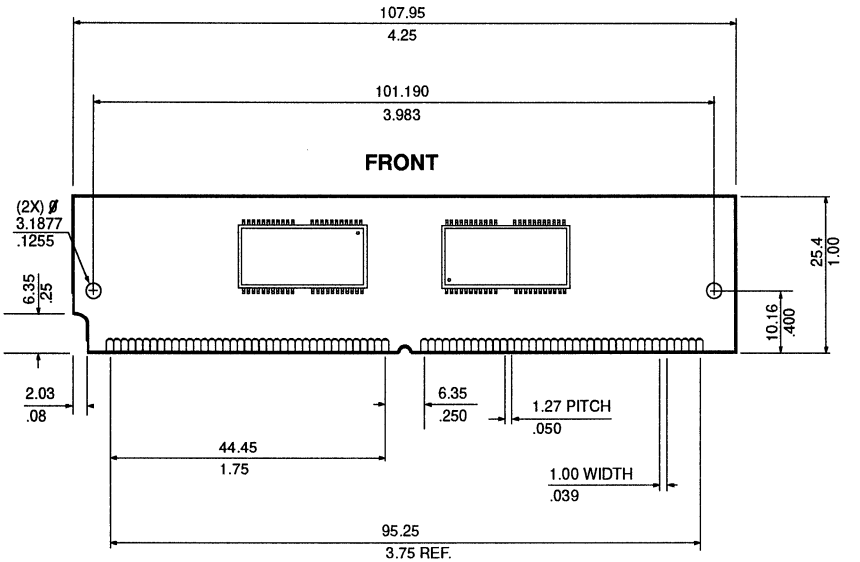
Note: $\overline{WE}$, D_{IN} are "H" or "L"

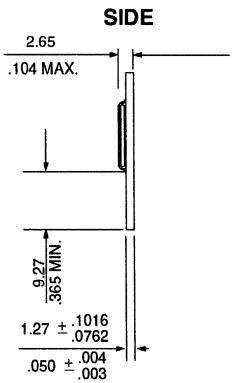
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 36 DRAM Module

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

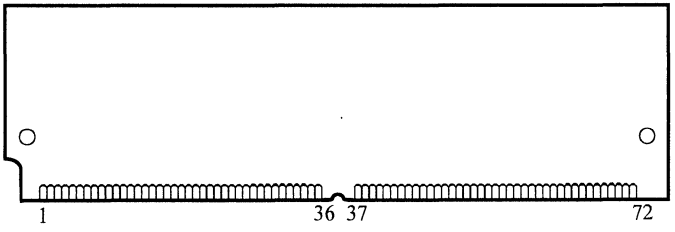
- High Performance CMOS process
- Single 5V ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write parity applications
- Au and Sn/Pb versions available

Description

The IBM11D2360BA is an 8MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 2Mx36 high speed memory array, and is configured as 2 1Mx36 banks - each independently selectable via unique $\overline{RAS}$ inputs. The assembly is intended for use in 18, 36 and 72 bit parity applications. It is manufactured with 16 1Mx4 devices, each in either a 350mil or 300mil package, and 8 1Mx1 devices in a 300mil package. The module is compatible with the JEDEC 72-Pin SIMM standard.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 2Mx32 non-parity SIMM, IBM11D2320B, as well as other density offerings and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

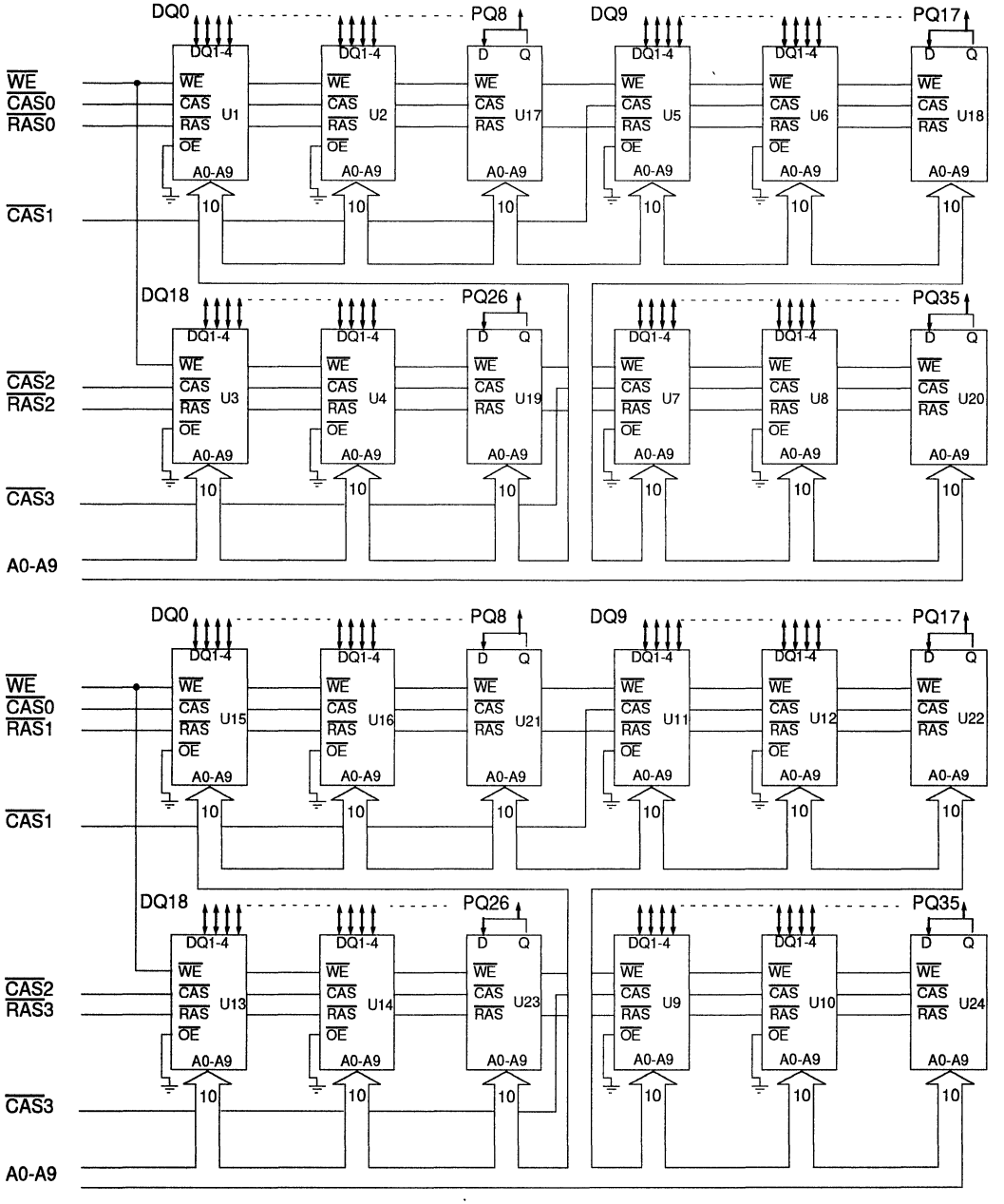
Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D2360BA-60	2M x 36	60ns	Sn/Pb	4.25" x 1.25" x .360"	
IBM11D2360BA-70	2M x 36	70ns	Sn/Pb	4.25" x 1.25" x .360"	
IBM11E2360BA-60	2M x 36	60ns	Au	4.25" x 1.25" x .360"	
IBM11E2360BA-70	2M x 36	70ns	Au	4.25" x 1.25" x .360"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	NC	NC
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 6.5	V	1
V_{IN}	Input Voltage	-0.7 to V_{CC} + 0.7	V	1
V_{OUT}	Output Voltage	-0.7 to V_{CC} + 0.7	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	14.5	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power is dissipated when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	147	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	51	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	42	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	147	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	27	pF	
$C_{I/O2}$	Output Capacitance (All PQ bits)	35	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1344	mA	1, 2, 3
		-70	—	1228		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	48	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1344	mA	1, 3, 4
		-70	—	1228		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	944	mA	1, 2, 3
		-70	—	864		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	40	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1344	mA	1, 3, 4
		-70	—	1228		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$	-60	+60		
		All others	-240	+240		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -4mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. Refresh current is specified for 1 bank.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100s is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. The 1M x 4 DRAM Outputs will remain disabled until these 8 cycles have occurred. This prevents data contention (excessive current) during power on. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	—	—	—	—	ns	3
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	30	—	40	ns	2, 3

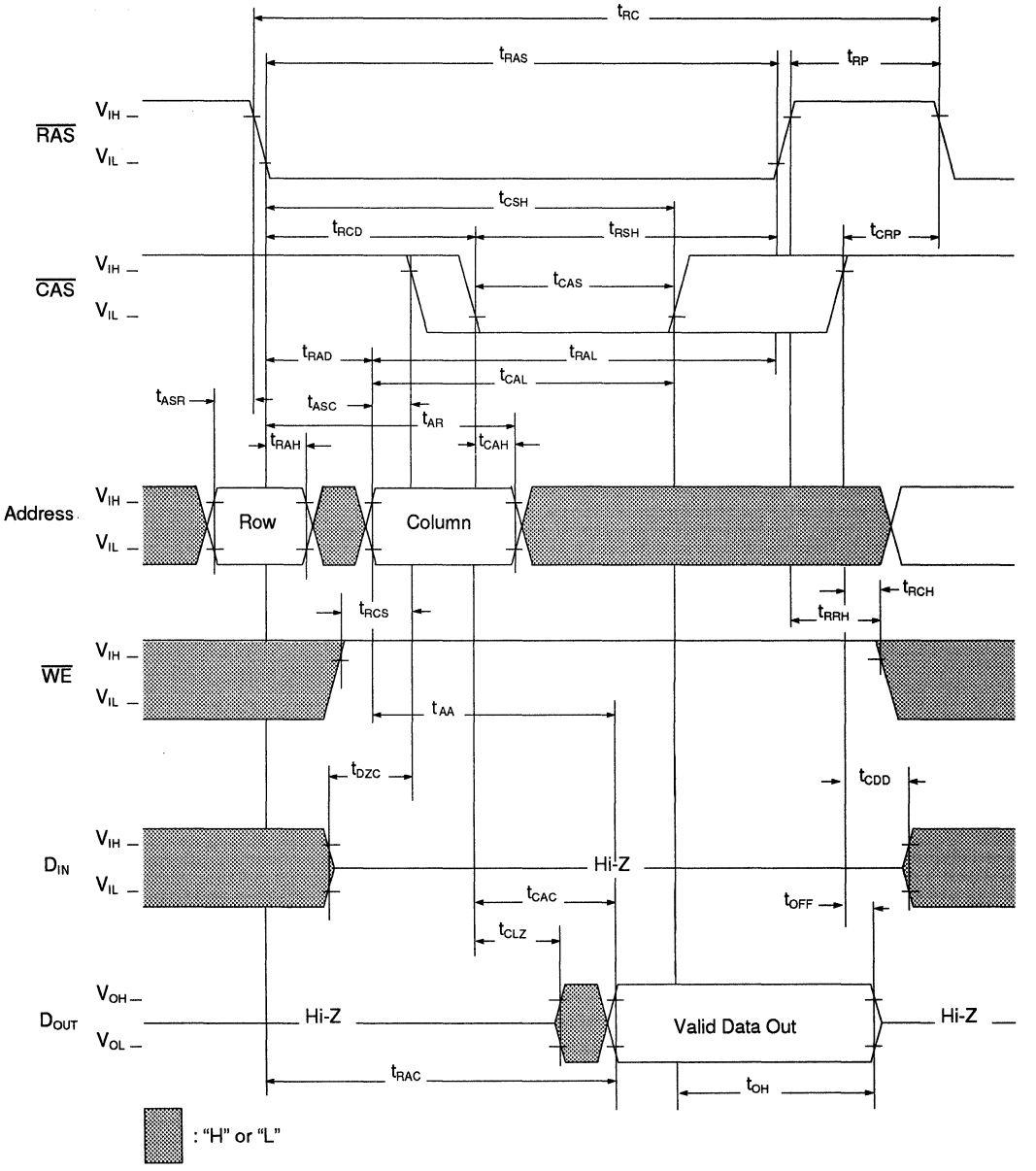
1. This timing parameter is not applicable to this product, but applies to a related product in this family.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Access time assumes a load of 100pF.

Refresh Cycle

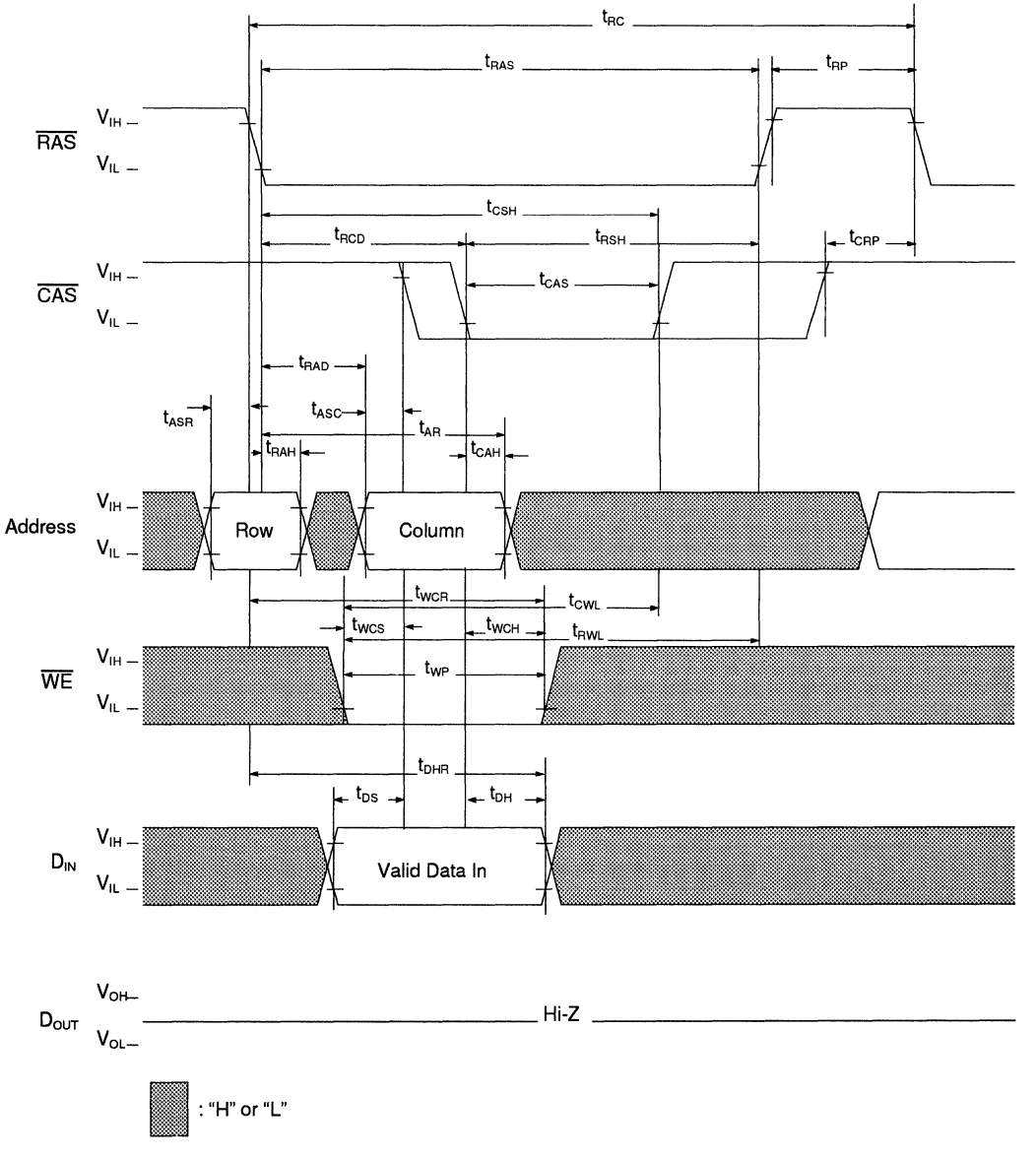
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	30	—	30	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	5	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms. The DC variation in the V_{CC} supply may not exceed 300mV within a refresh interval (16ms).

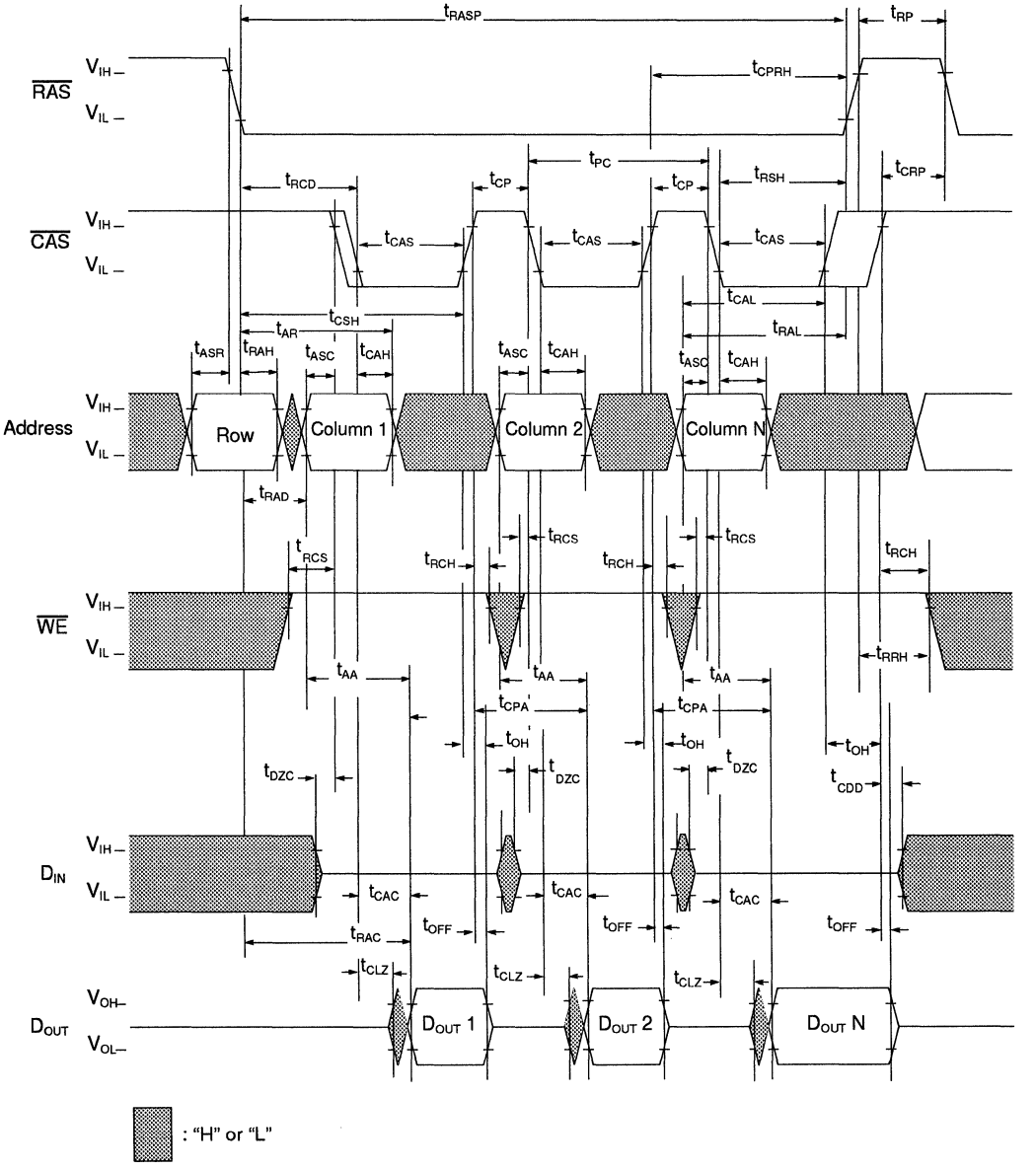
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

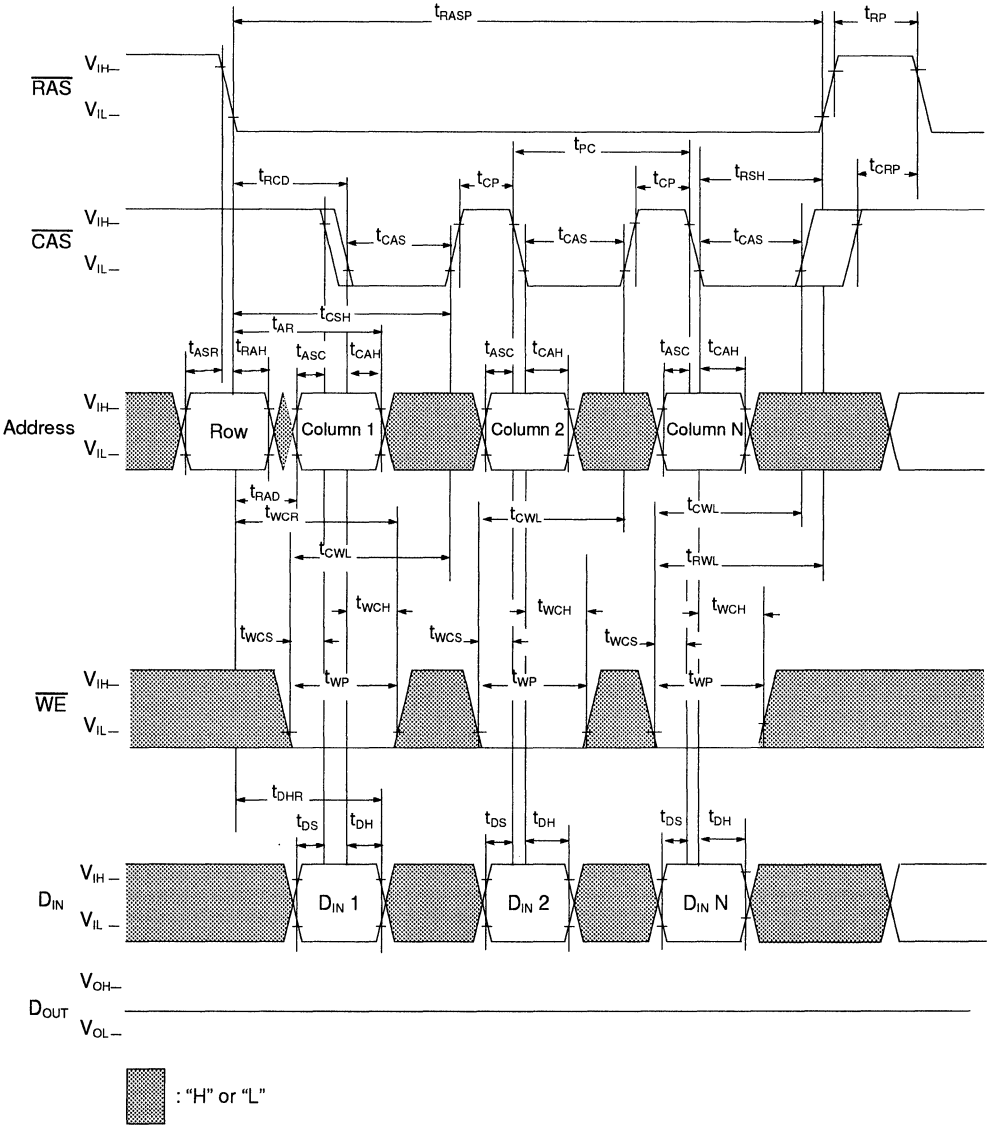
Write Cycle (Early Write)



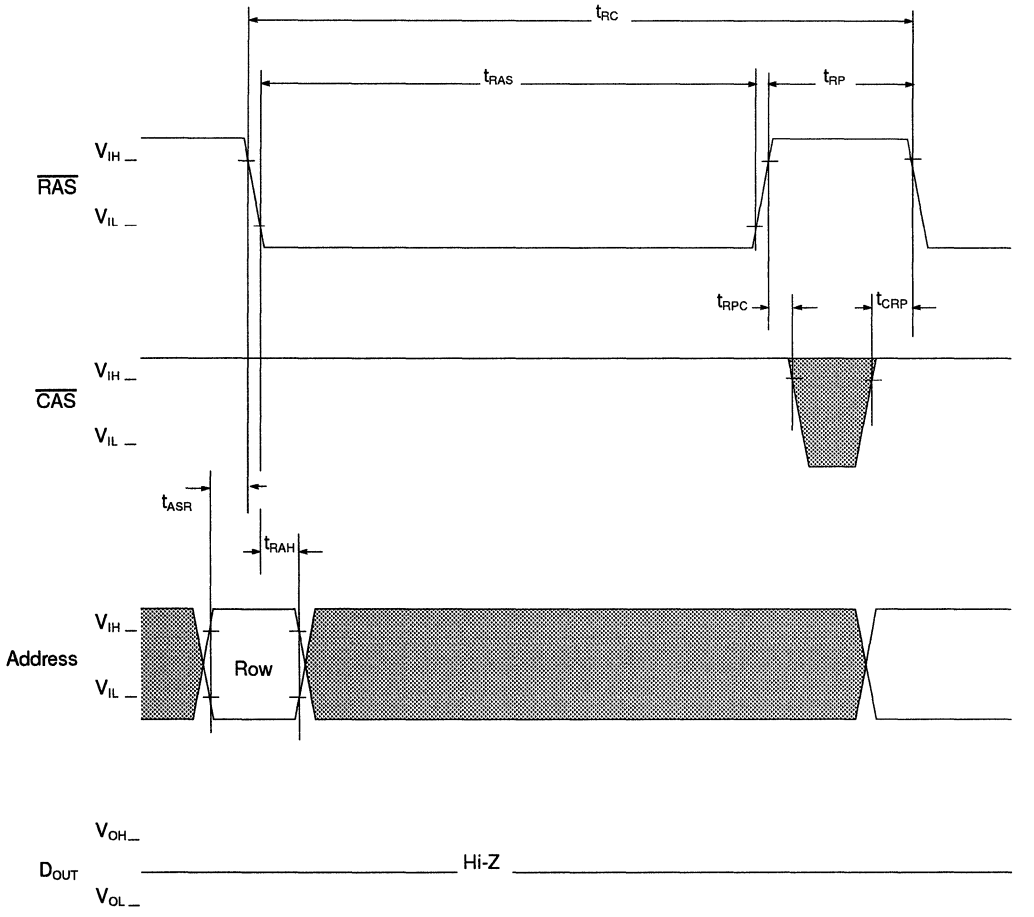
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



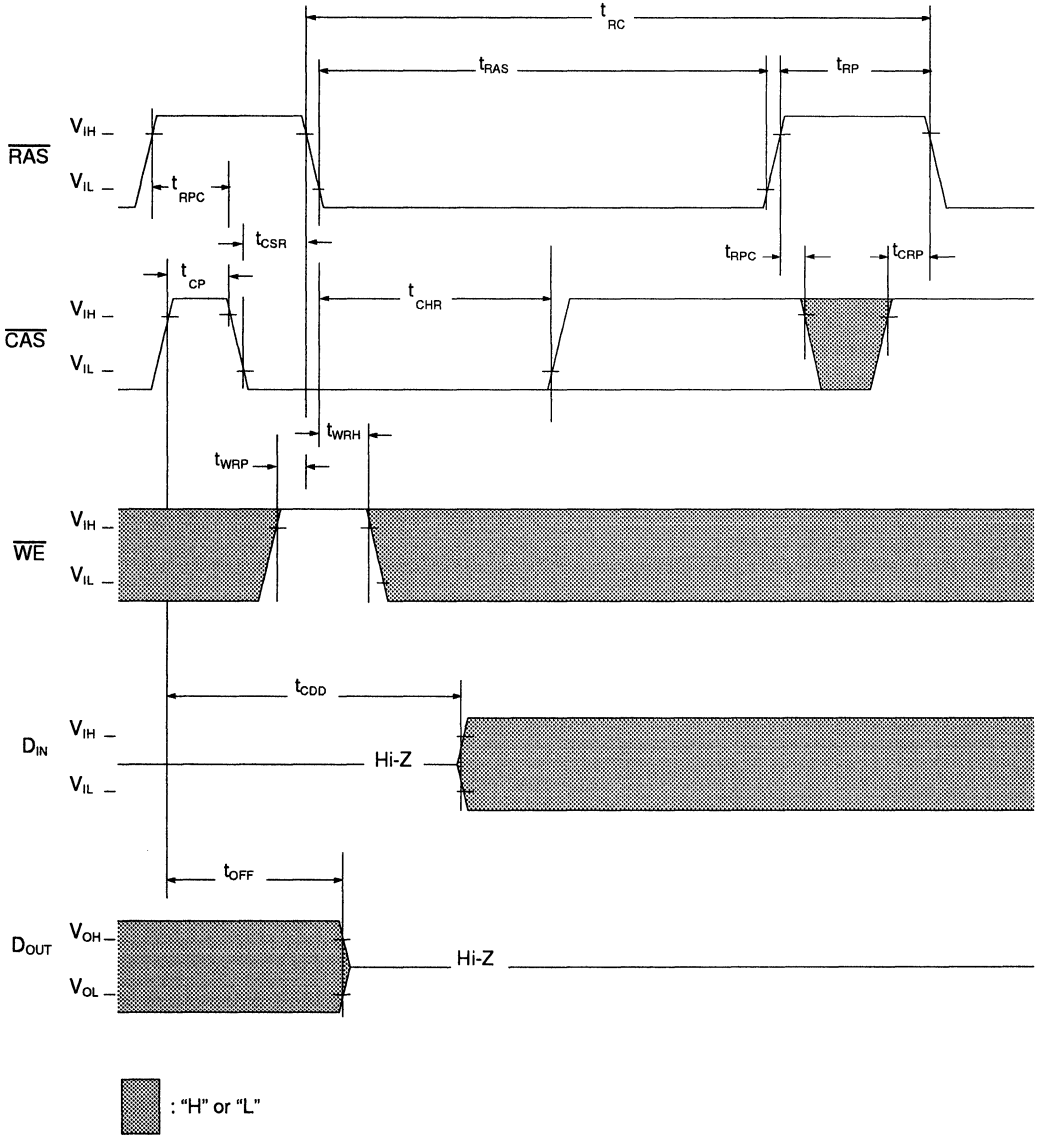
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

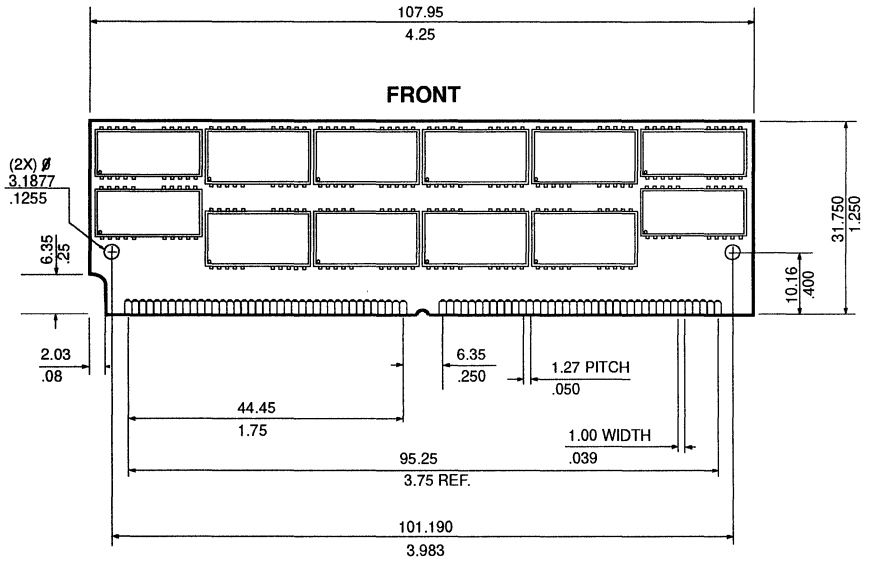
Note: $\overline{WE}$, D_{IN} are "H" or "L"

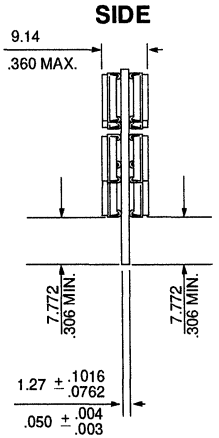
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing (IBM11D2360BA)





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 36 DRAM Module

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

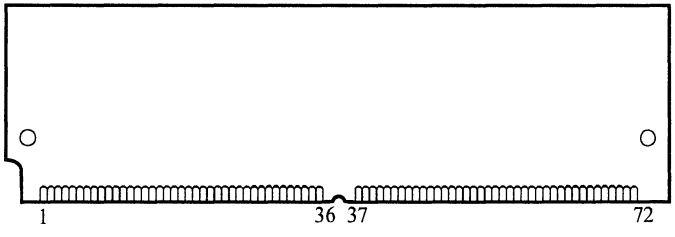
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- Low active current dissipation
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write parity applications
- Au and Sn/Pb versions available

Description

The IBM11D2360BD is an 8MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 2Mx36 high speed memory array, and is configured as 2 1Mx36 banks - each independently selectable via unique $\overline{RAS}$ inputs. The assembly is intended for use in 18, 36 and 72 bit parity applications. It is manufactured with 16 1Mx4 devices, each in a 300mil package, and 8 1Mx1 devices in a 300mil package. The module is compatible with the JEDEC 72-Pin SIMM standard.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 2Mx32 non-parity SIMM, IBM11D2320B, as well as other density offerings and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

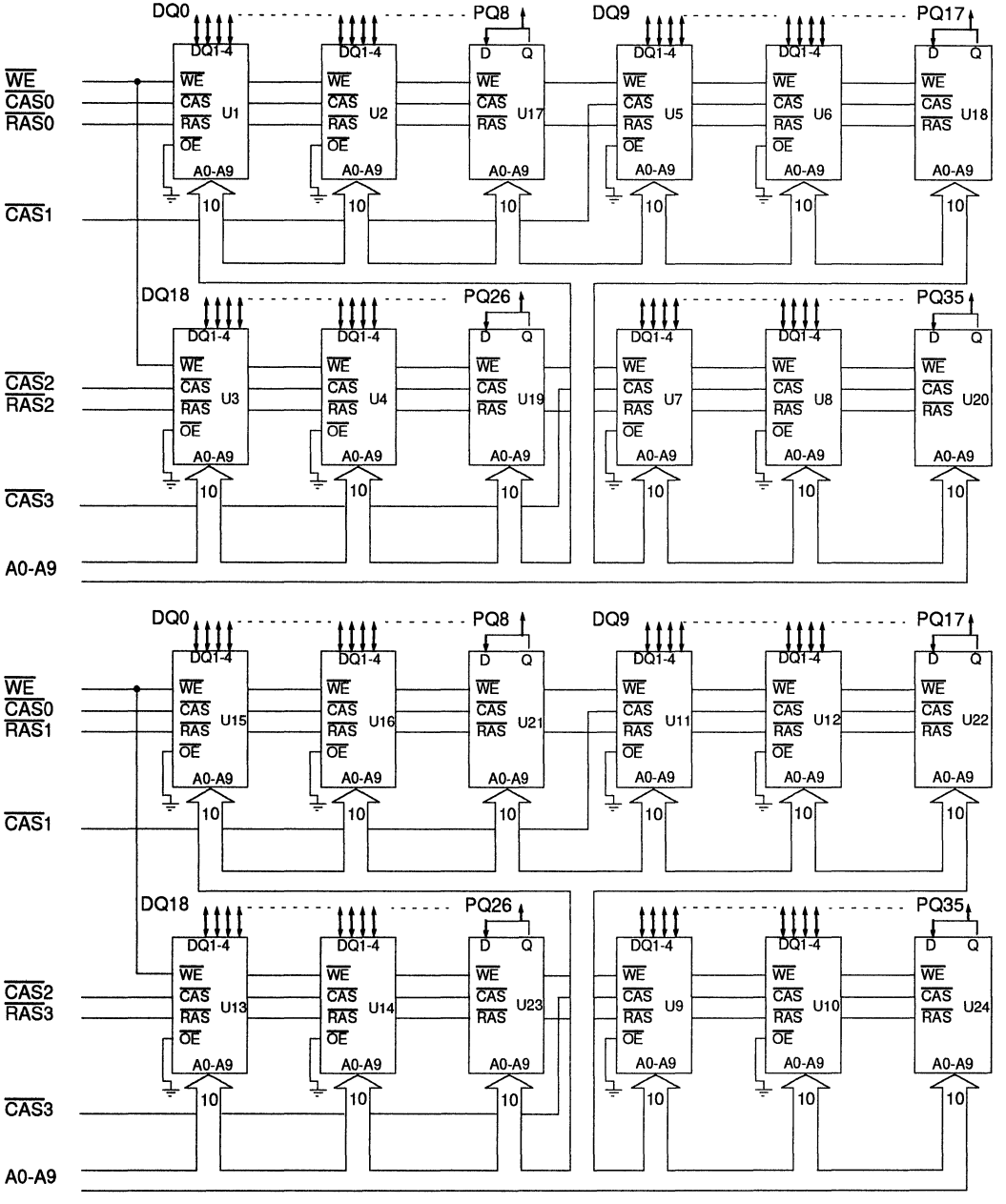
Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D2360BD-60	2M x 36	60ns	Sn/Pb	4.25" x 1.25" x .360"	
IBM11D2360BD-70	2M x 36	70ns	Sn/Pb	4.25" x 1.25" x .360"	
IBM11E2360BD-60	2M x 36	60ns	Au	4.25" x 1.25" x .360"	
IBM11E2360BD-70	2M x 36	70ns	Au	4.25" x 1.25" x .360"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	NC	NC
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to + 6.0	V	1
V_{IN}	Input Voltage	-1.0 to + 6.0	V	1
V_{OUT}	Output Voltage	-1.0 to + 6.0	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	11.5	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power is dissipated when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	161	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	55	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	52	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	188	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	27	pF	
$C_{I/O2}$	Output Capacitance (All PQ bits)	35	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1064	mA	1, 2, 3
		-70	—	924		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	48	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1064	mA	1, 3, 4
		-70	—	924		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	824	mA	1, 2, 3
		-70	—	704		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	24	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1064	mA	1, 3, 4
		-70	—	924		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$	-60	+60		
		All others	-240	+240		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. Refresh current is specified for 1 bank.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	30	—	40	ns	1, 2

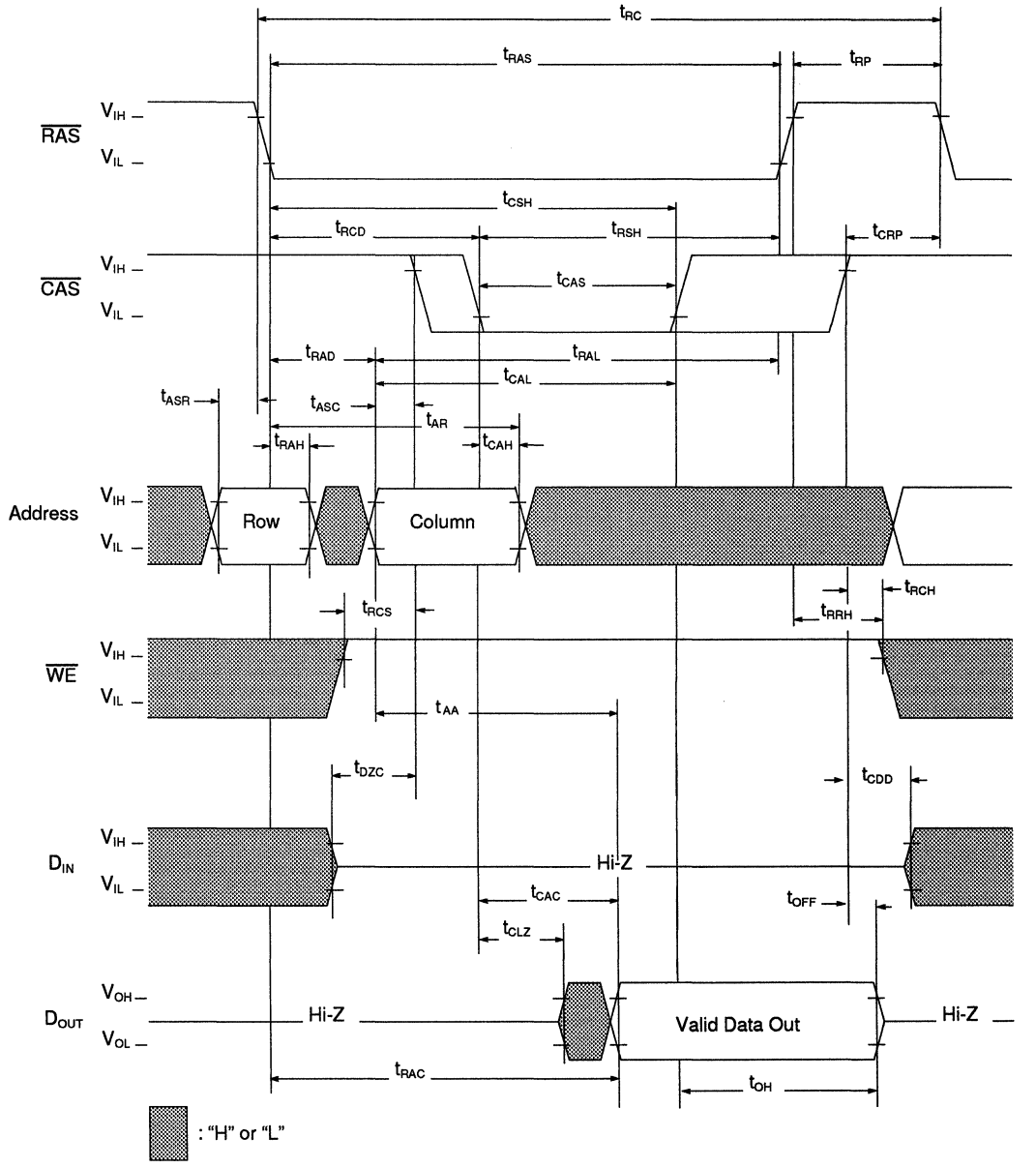
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	30	—	30	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms.

Read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VIH
VIL
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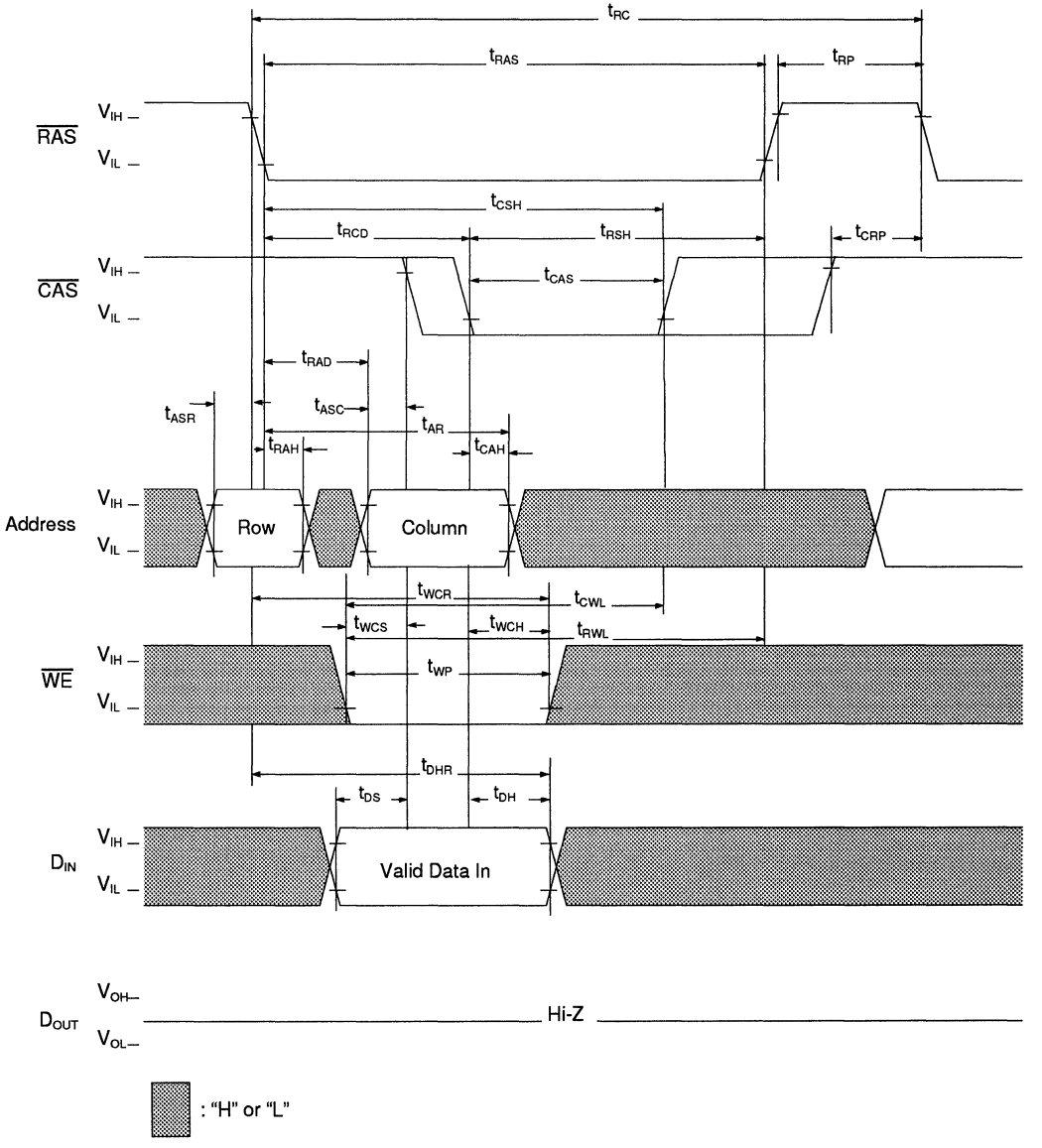
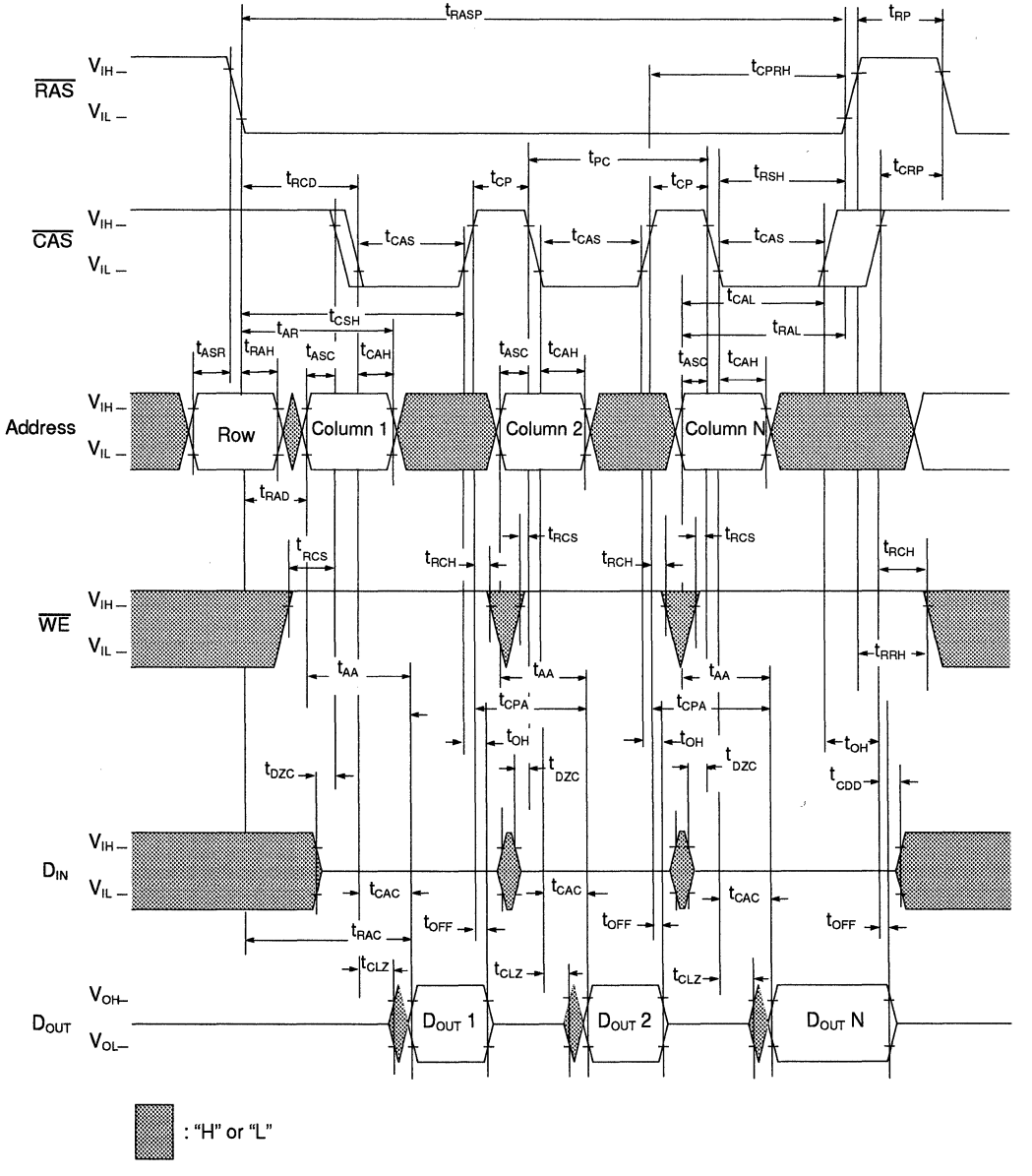
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

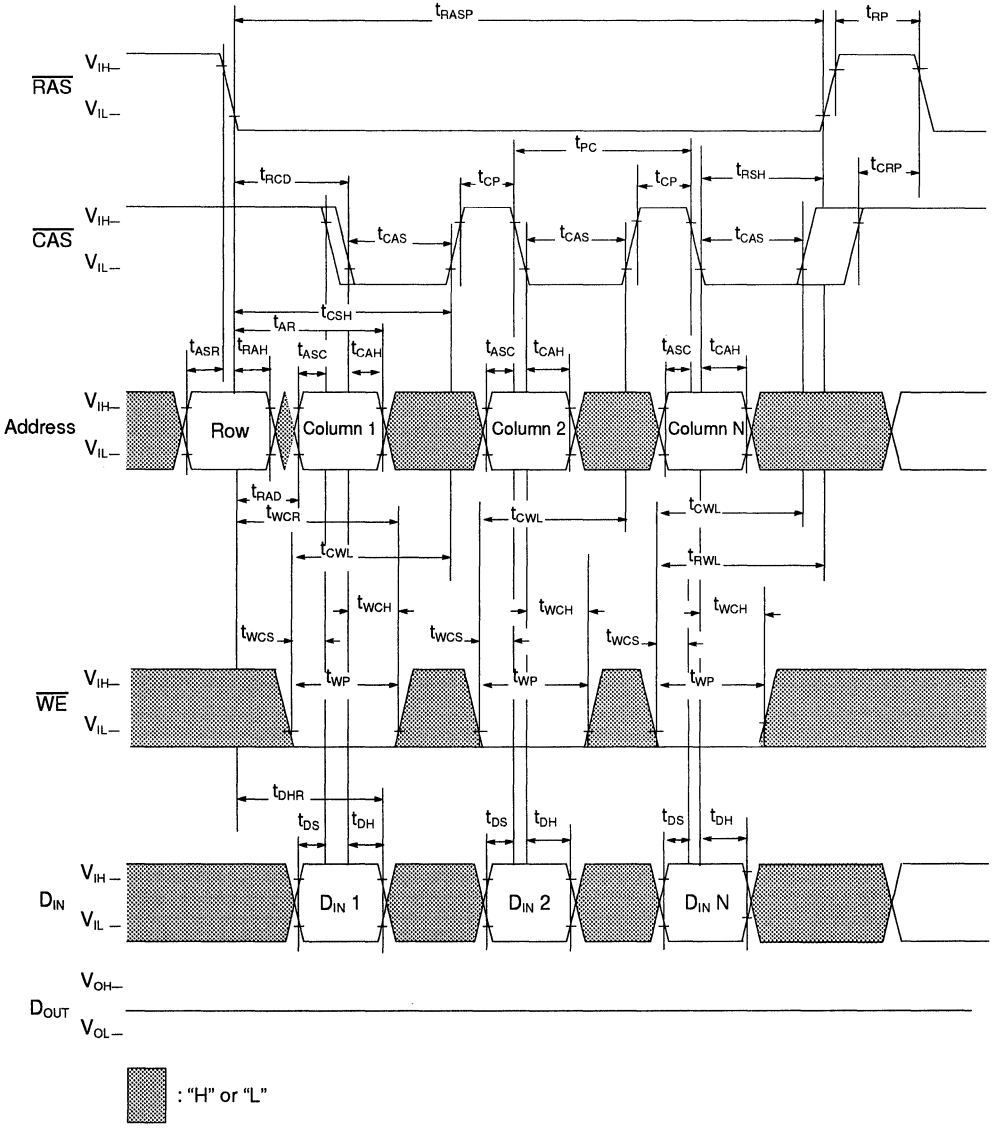
Write Cycle (Early Write)



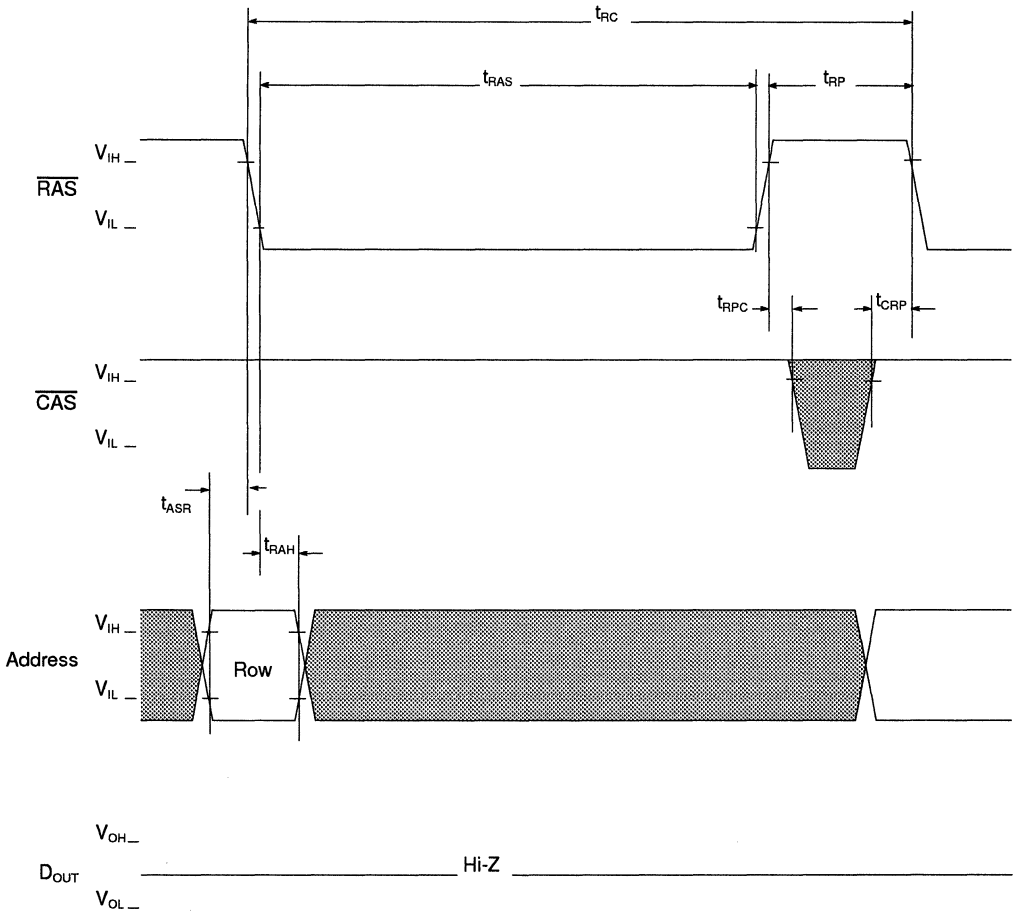
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



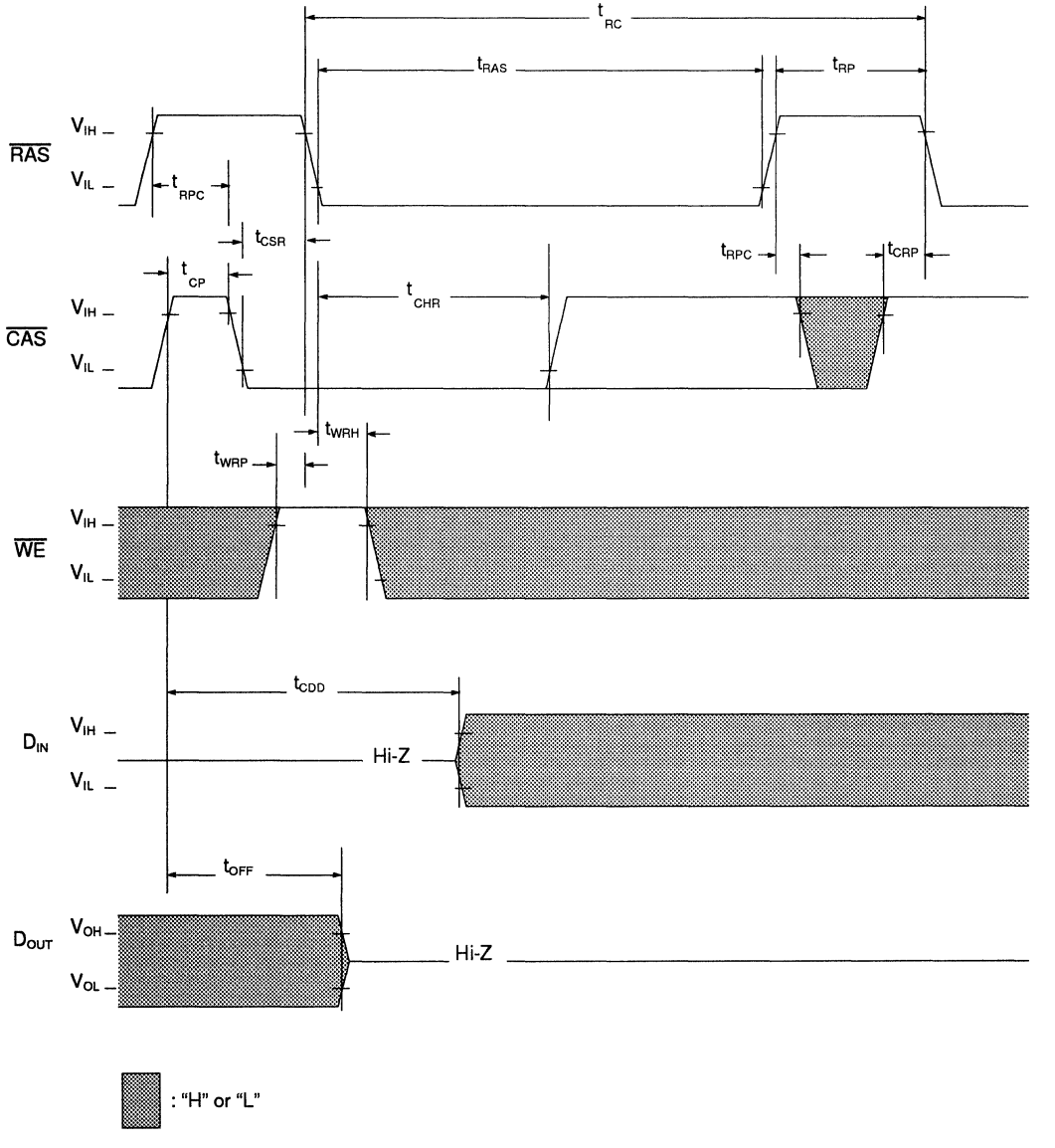
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

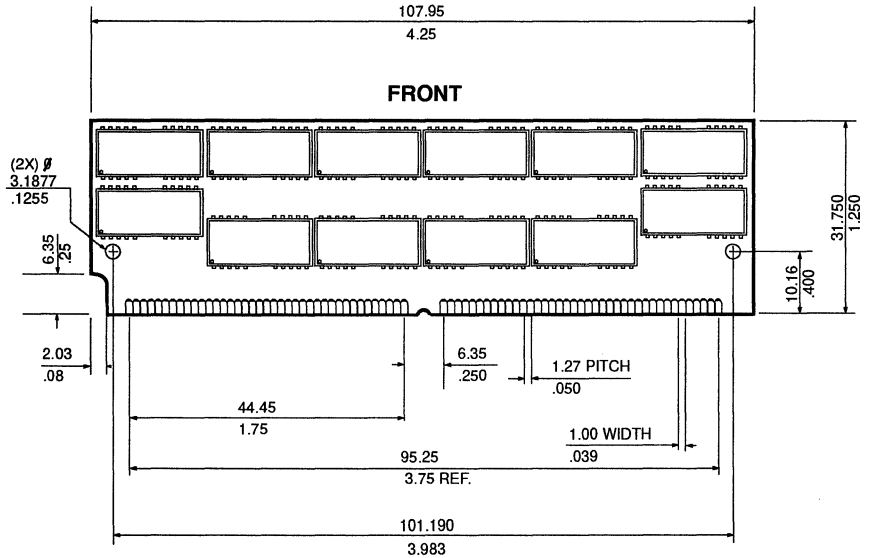
Note: $\overline{WE}$, D_{IN} are "H" or "L"

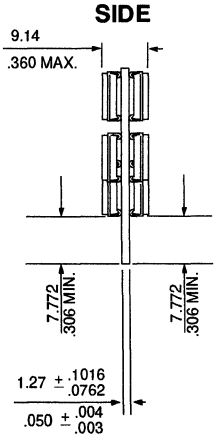
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 36 DRAM Module

Features

- 72-Pin Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

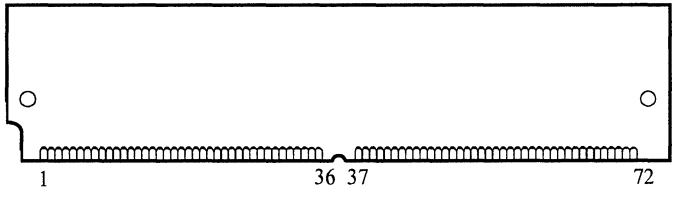
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write parity applications
- Au and Sn/Pb versions available

Description

The IBM11D2360EA is an 8MB 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 2Mx36 high speed memory array, and is configured as 2 1Mx36 banks - each independently selectable via unique $\overline{RAS}$ inputs. The assembly is intended for use in 36 and 72 bit applications where interleave of 9 or 18 bit words is not required. It is manufactured with 16 1Mx4 devices, each in either a 350mil or 300mil package, and 2 1Mx4 'Quad CAS' devices for parity. The use of 'Quad CAS' devices results in reduced SIMM height and lower power dissipation.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 2Mx32 non-parity SIMM, IBM11D2320B, as well as other density offerings and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

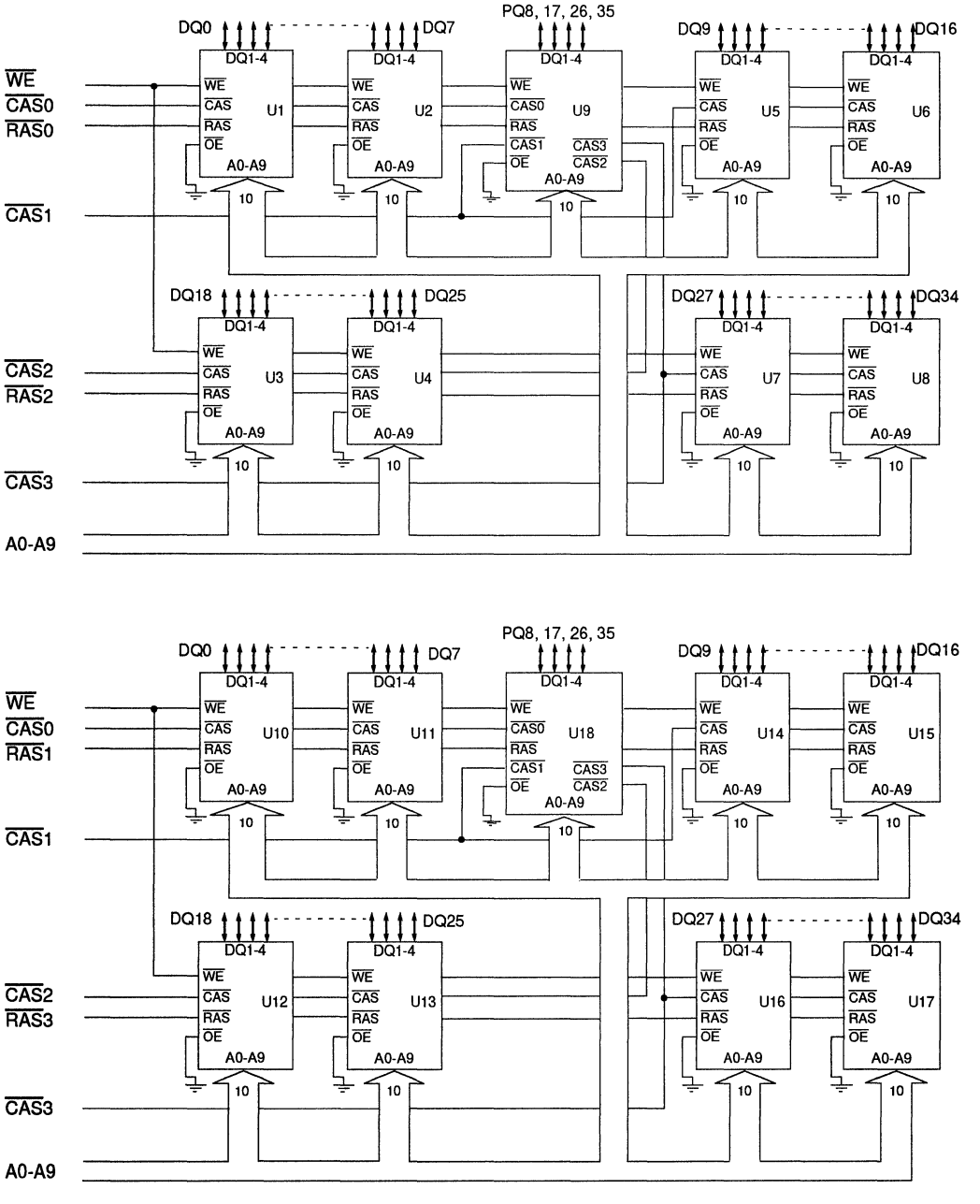
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D2360EA-60	2M x 36	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D2360EA-70	2M x 36	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E2360EA-60	2M x 36	60ns	Au	4.25" x 1" x .360"	
IBM11E2360EA-70	2M x 36	70ns	Au	4.25" x 1" x .360"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	NC	NC
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 6.5	V	1
V_{IN}	Input Voltage	-0.7 to V_{CC} + 0.7	V	1
V_{OUT}	Output Voltage	-0.7 to V_{CC} + 0.7	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	11.7	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	99	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$0, 1)	44	pF	
C_{I3}	Input Capacitance ($\overline{RAS}$2, 3)	38	pF	
C_{I4}	Input Capacitance ($\overline{CAS}$)	44	pF	
C_{I5}	Input Capacitance ($\overline{WE}$)	85	pF	
$C_{I/O}$	Output Capacitance (All DQ, PQ)	23	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1078	mA	1, 2, 3
		-70	—	972		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	37	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	1078	mA	1, 3, 4
		-70	—	972		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	688	mA	1, 2, 3
		-70	—	668		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	34	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1078	mA	1, 3, 4
		-70	—	972		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$0, 1	-50	+50	µA	
		$\overline{RAS}$2, 3	-40	+40		
		$\overline{CAS}$	-60	+60		
		All others	-180	+180		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -4mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. Refresh current is specified for 1 bank.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. The 1Mx4 DRAM Outputs will remain disabled until these 8 cycles have occurred. This prevents data contention (excessive current) during power on. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	1
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	—	—	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{CLCH}	Hold Time $\overline{CAS}$ Low to $\overline{CAS}$ High	10	—	10	—	ns	5
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	

1. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	45	—	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	10	—	15	—	ns	

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

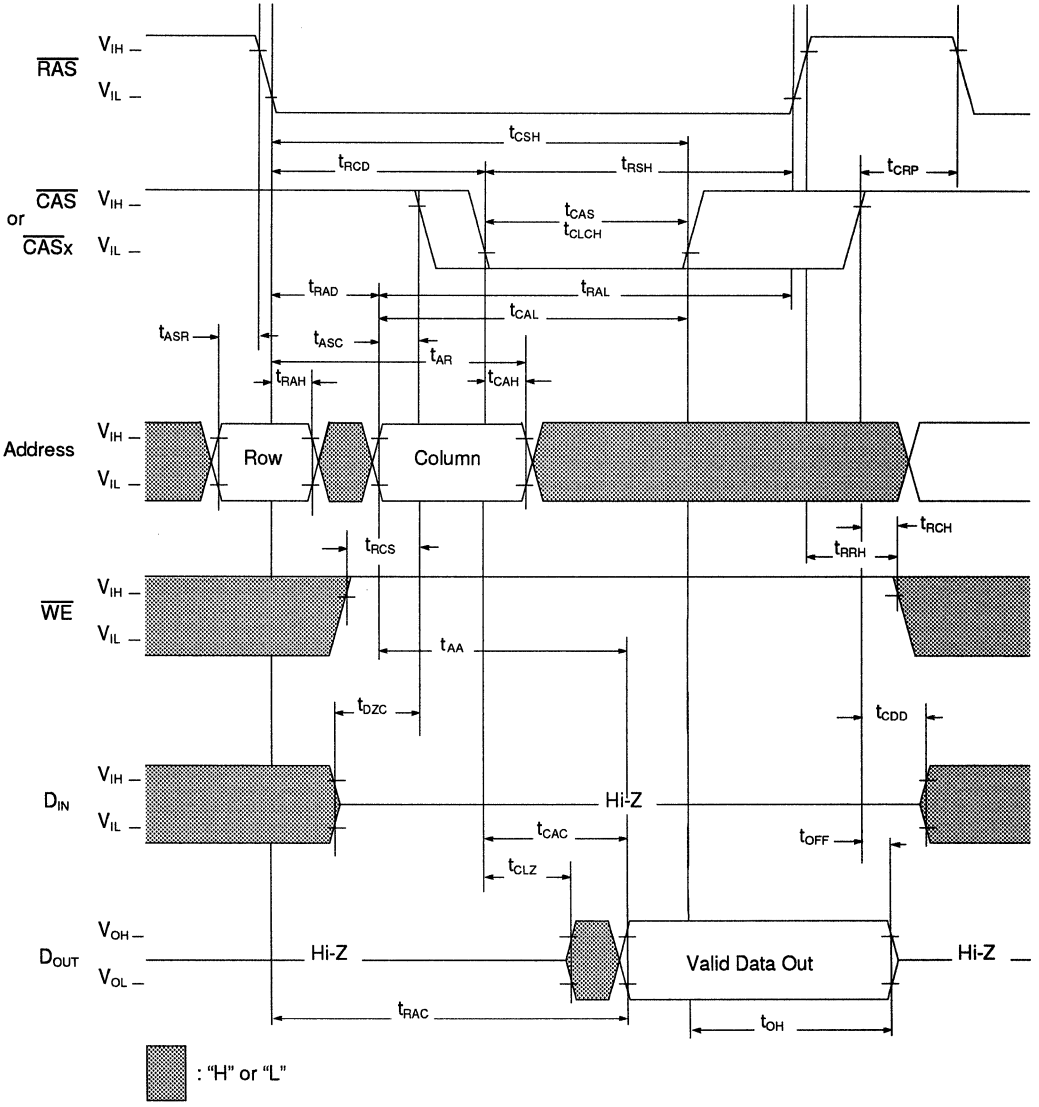
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Measured with the specified current load and 100pF.

Refresh Cycle

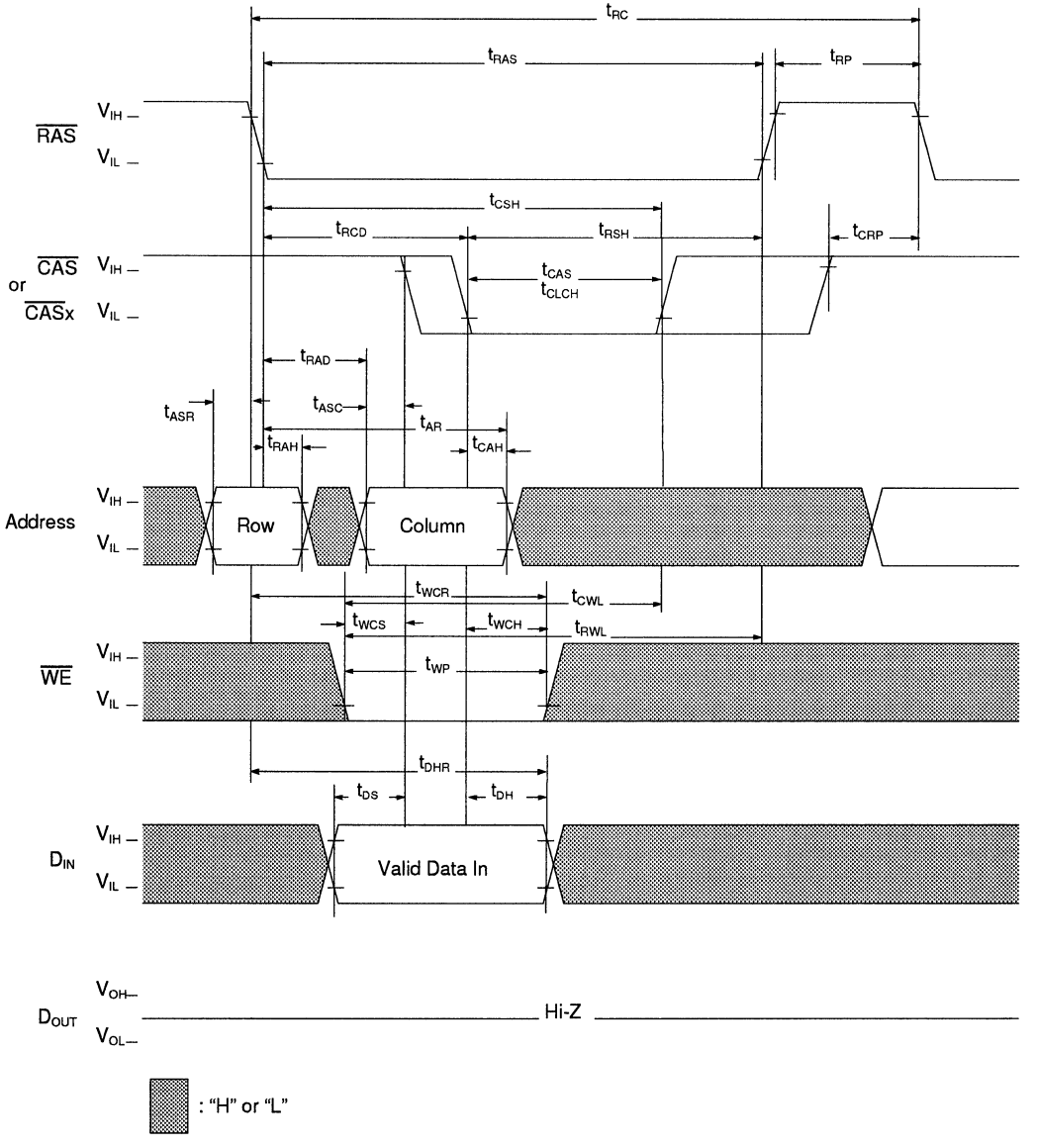
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms. The DC variation in the V_{CC} supply may not exceed 300mV within a refresh interval (16ms).

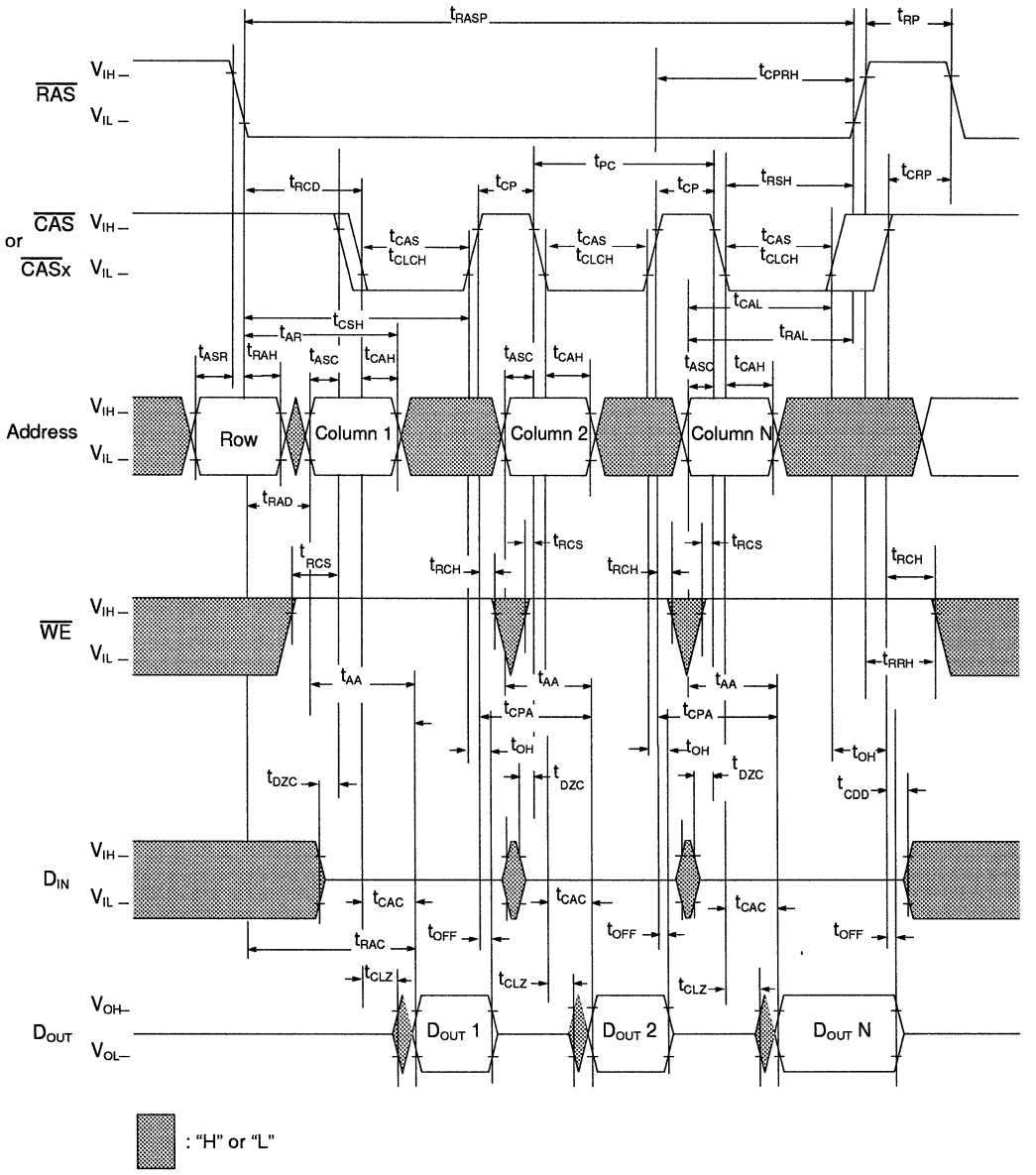
Read


RAS
CAS
or
CASx
Address
WE
DIN
DOUT
VIH
VIL
VOH
VOL
Row
Column
Hi-Z
Valid Data Out
tCSH
tRCD
tRSH
tCRP
tCAS
tCLCH
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
tRCS
tRCH
tRRH
tAA
tDZC
tCDD
tCAC
tOFF
tCLZ
tRAC
tOH
: "H" or "L"

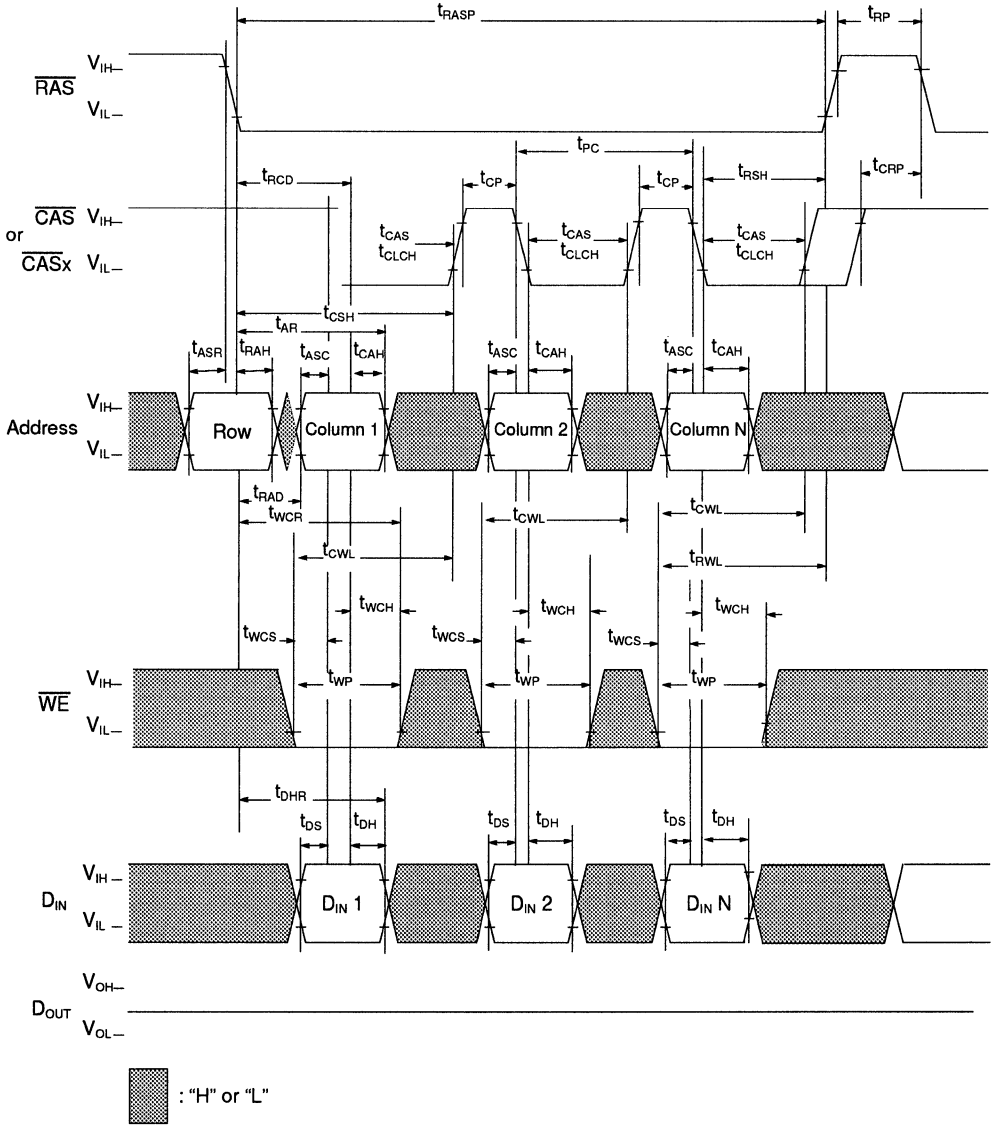
Write Cycle (Early Write)



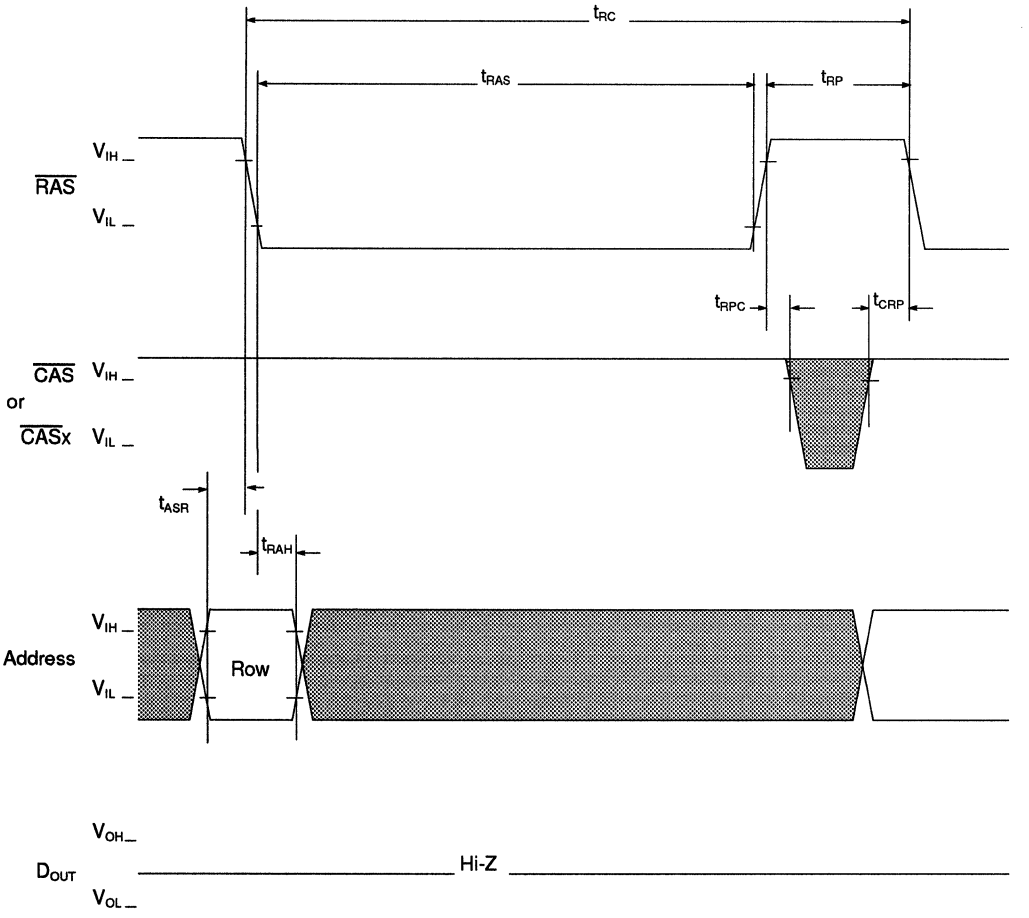
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

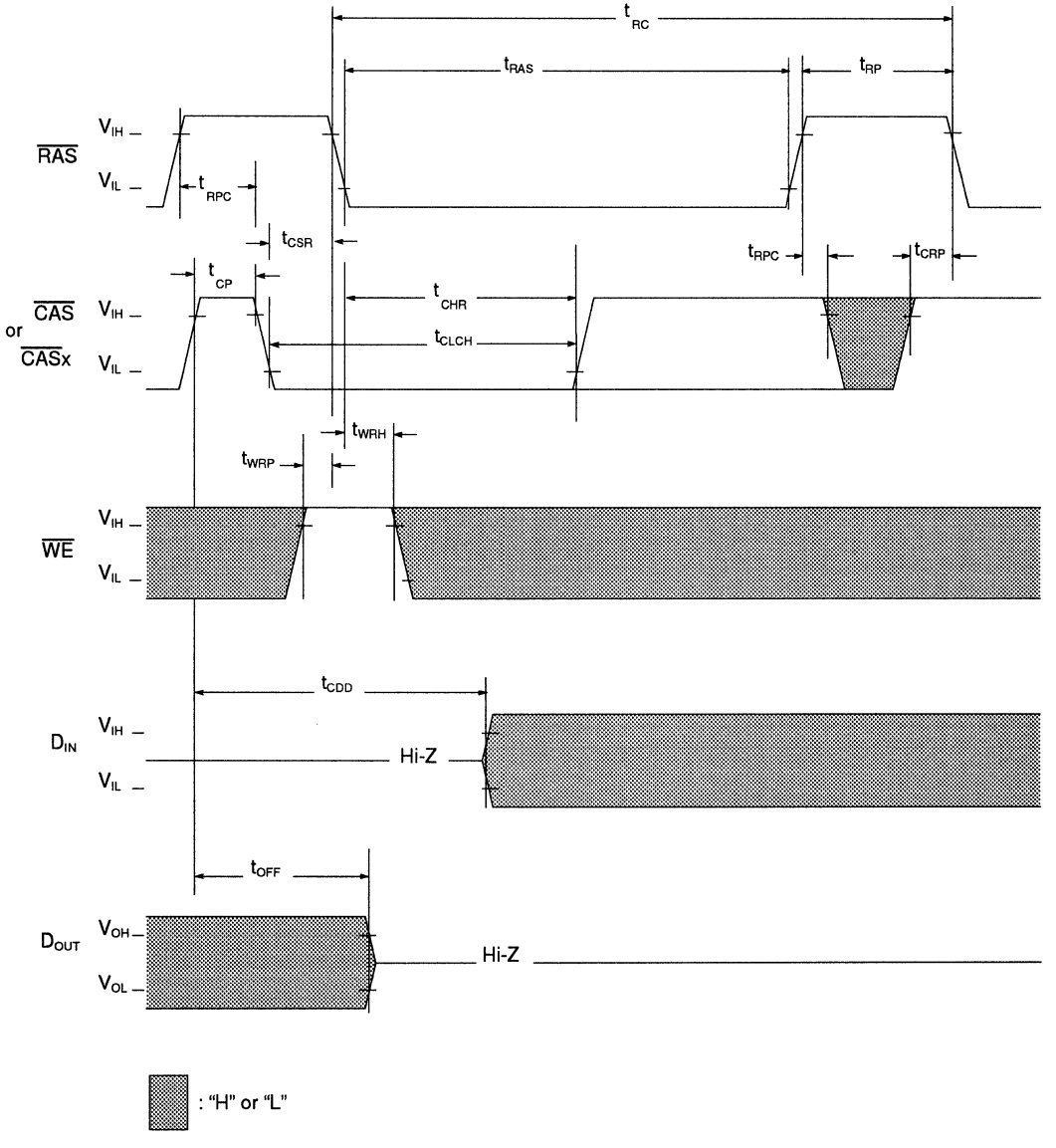


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



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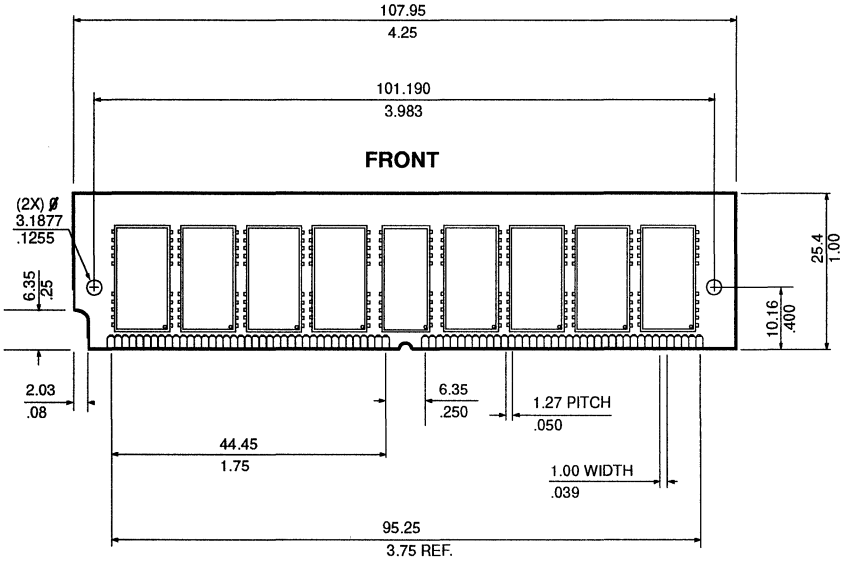

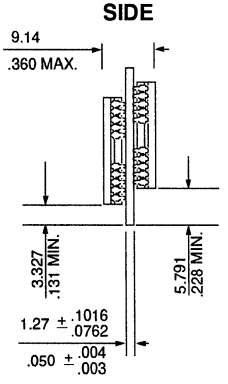

NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

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Preliminary

2M x 36 DRAM Module

Features

- 72-Pin Single-In-Line Memory Module
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- High Performance CMOS process
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- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write parity applications
- Au and Sn/Pb versions available

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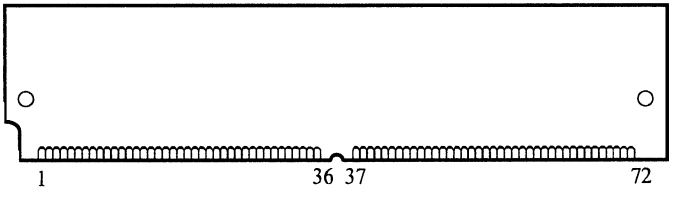
Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

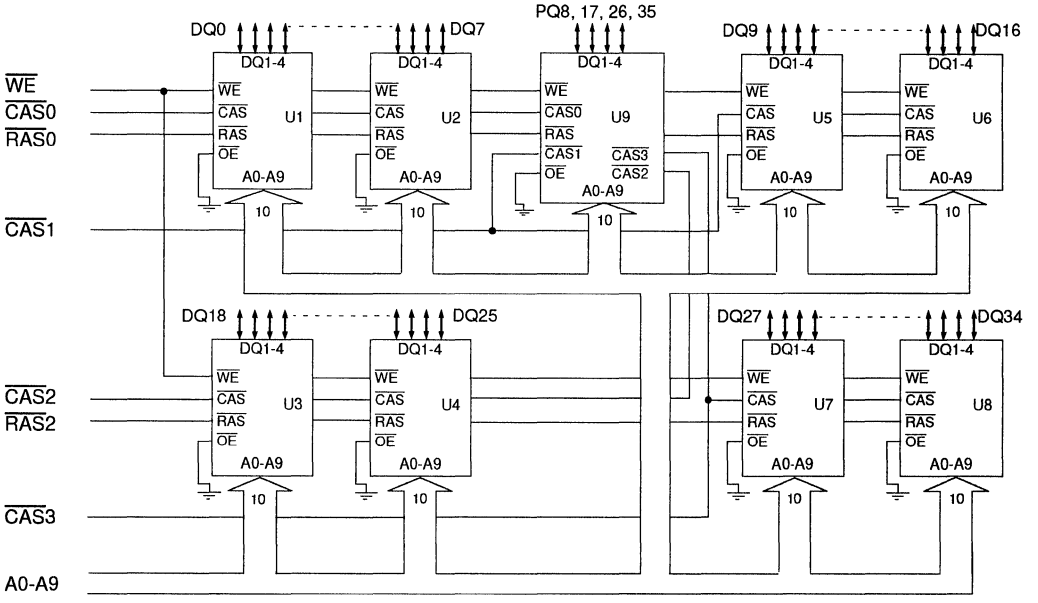
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

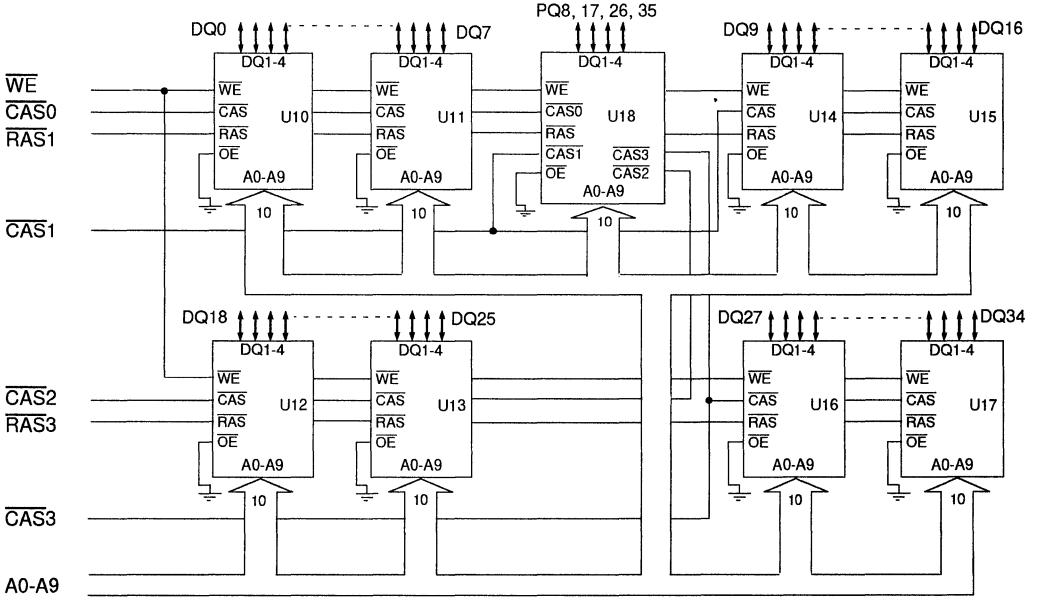
1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D2360ED-60	2M x 36	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D2360ED-70	2M x 36	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E2360ED-60	2M x 36	60ns	Au	4.25" x 1" x .360"	
IBM11E2360ED-70	2M x 36	70ns	Au	4.25" x 1" x .360"	

Block Diagram





Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	NC	NC
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +6.0	V	1
V_{IN}	Input Voltage	-1.0 to +6.0	V	1
V_{OUT}	Output Voltage	-1.0 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	8.6	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	105	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$0, 1)	48	pF	
C_{I3}	Input Capacitance ($\overline{RAS}$2, 3)	45	pF	
C_{I4}	Input Capacitance ($\overline{CAS}$)	54	pF	
C_{I5}	Input Capacitance ($\overline{WE}$)	137	pF	
$C_{I/O}$	Output Capacitance (All DQ, PQ)	25	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	798	mA	1, 2, 3
		-70	—	668		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	37	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	798	mA	1, 3, 4
		-70	—	668		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	568	mA	1, 2, 3
		-70	—	478		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	18	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	798	mA	1, 3, 4
		-70	—	668		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$0, 1	-50	+50		
		$\overline{RAS}$2, 3	-40	+40	µA	
		$\overline{CAS}$	-60	+60		
		All others	-180	+180		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. Refresh current is specified for 1 bank.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	1
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{CLCH}	Hold Time $\overline{CAS}$ Low to $\overline{CAS}$ High	10	—	10	—	ns	4
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	

1. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	45	—	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

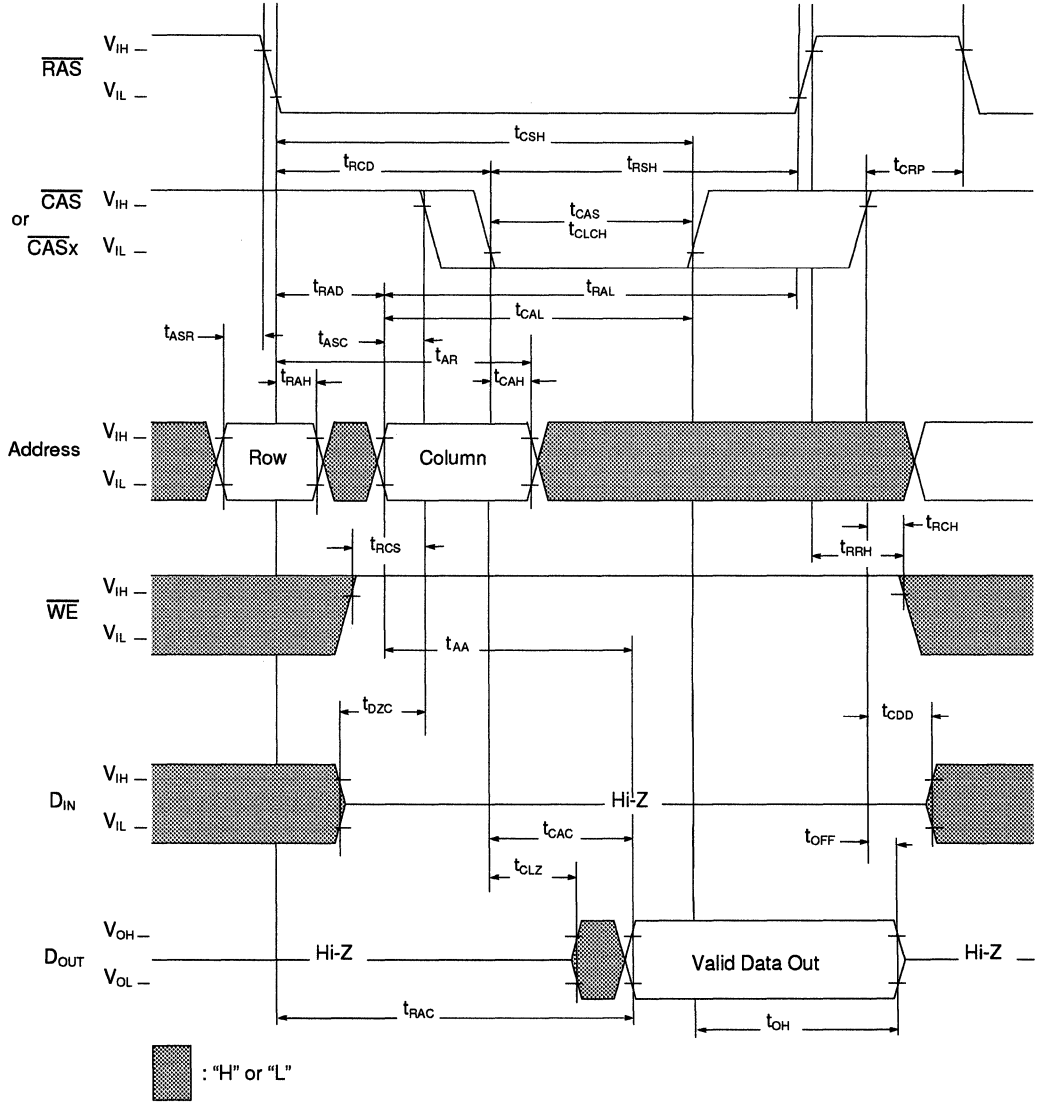
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Measured with the specified current load and 100pF.

Refresh Cycle

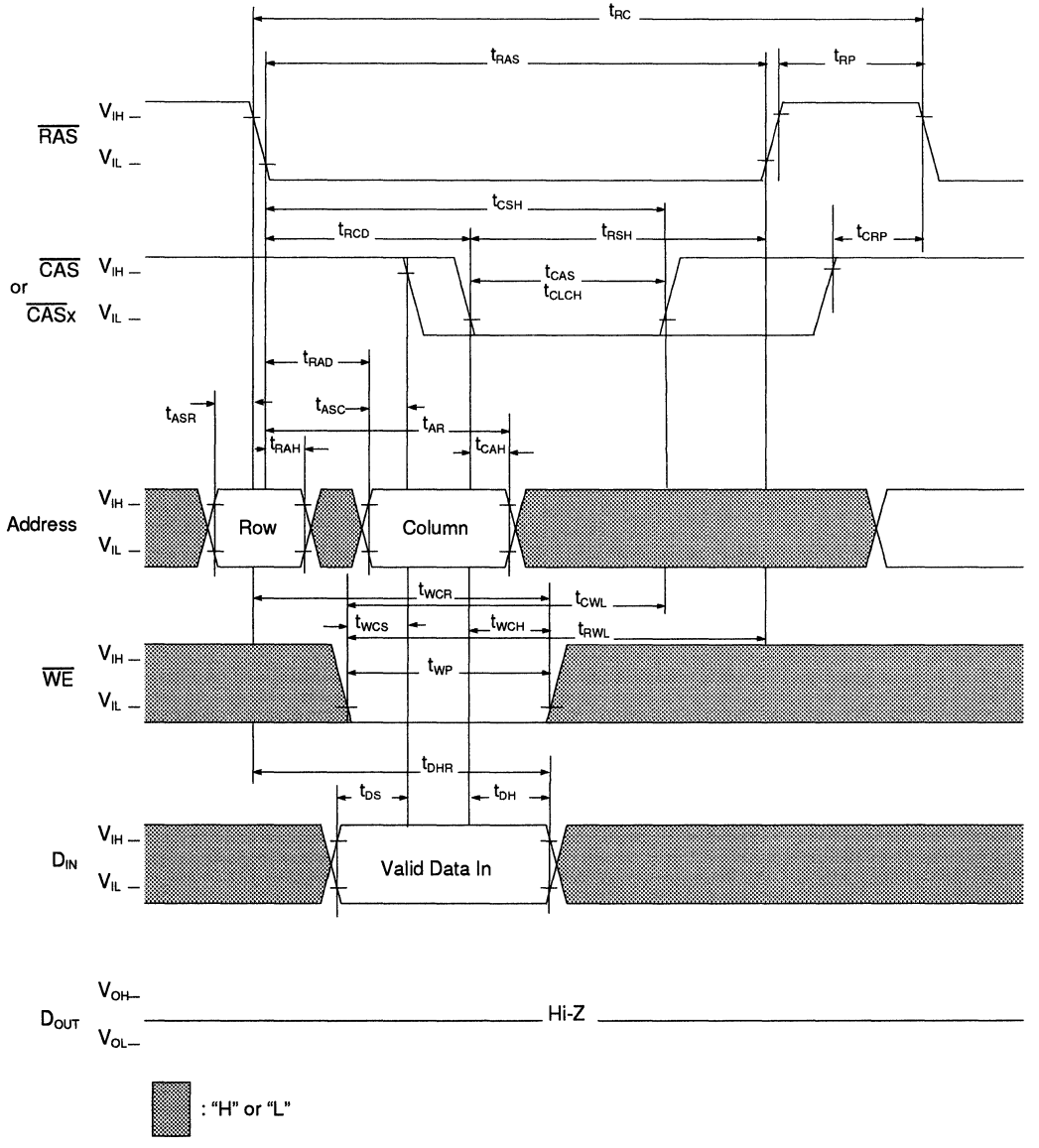
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	15	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms.

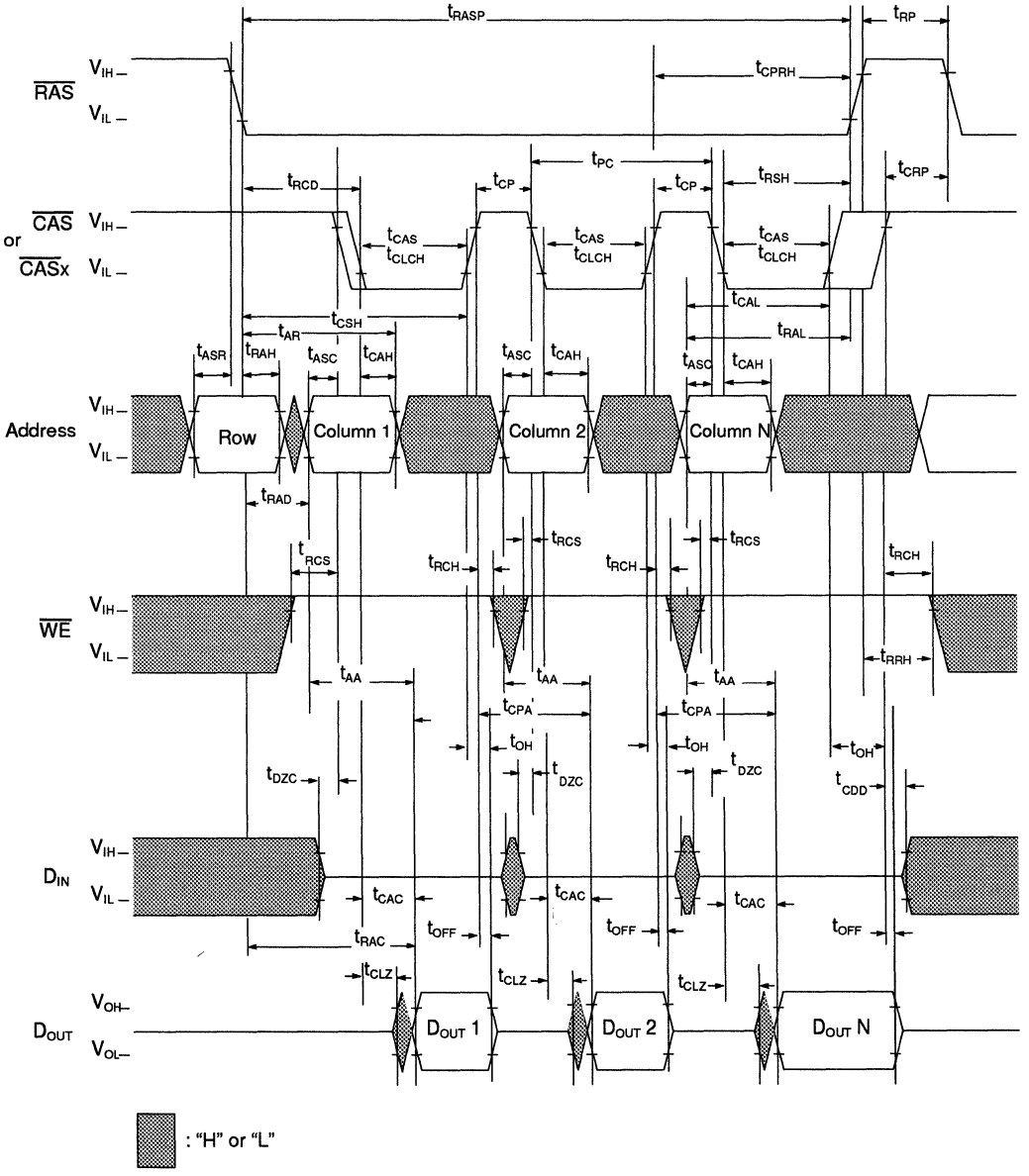
Read


RAS
CAS
or
CASx
Address
WE
DIN
DOUT
VIH
VIL
VOH
VOL
Row
Column
Hi-Z
Valid Data Out
tCSH
tRCD
tRSH
tCRP
tCAS
tCLCH
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
tRCS
tRRH
tRCH
tAA
tDZC
tCDD
tCAC
tOFF
tCLZ
tRAC
tOH
: "H" or "L"

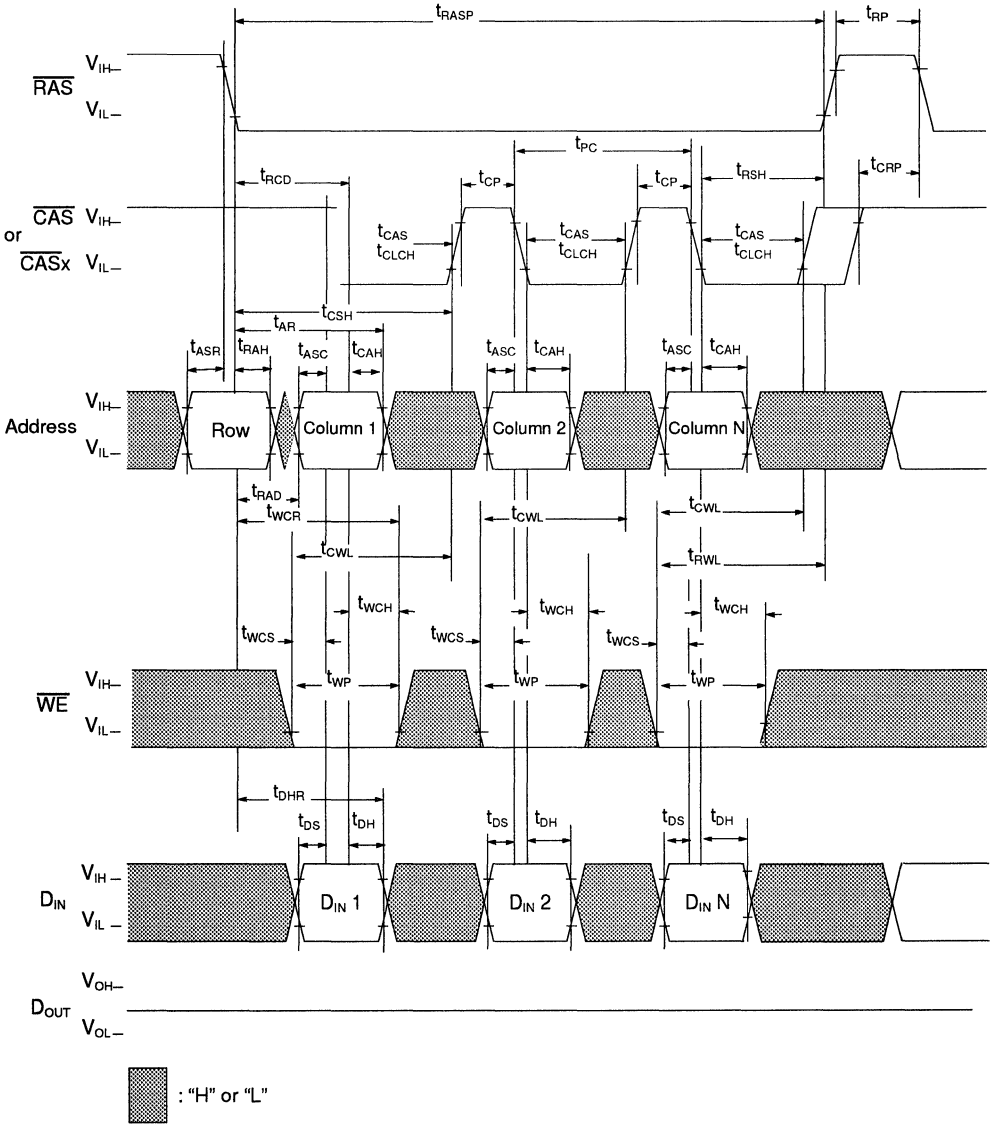
Write Cycle (Early Write)



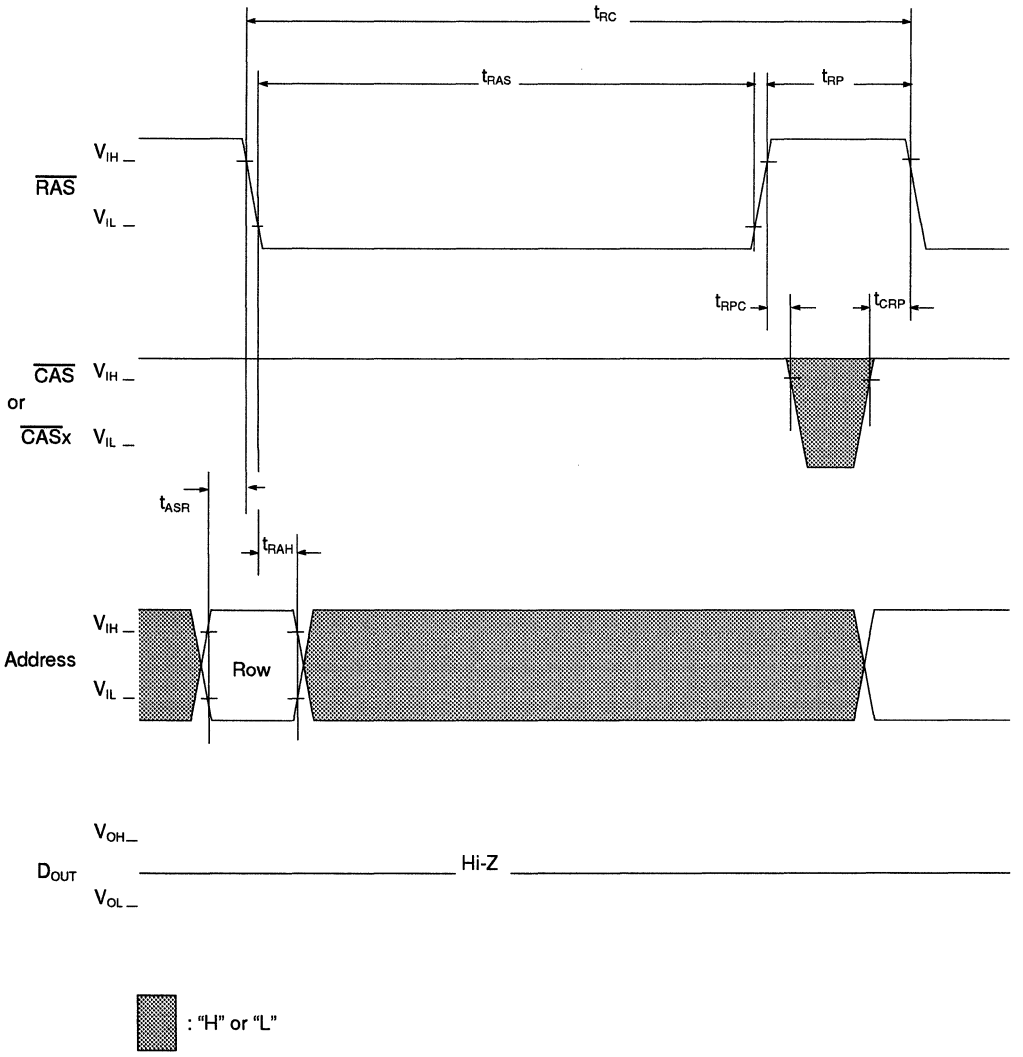
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

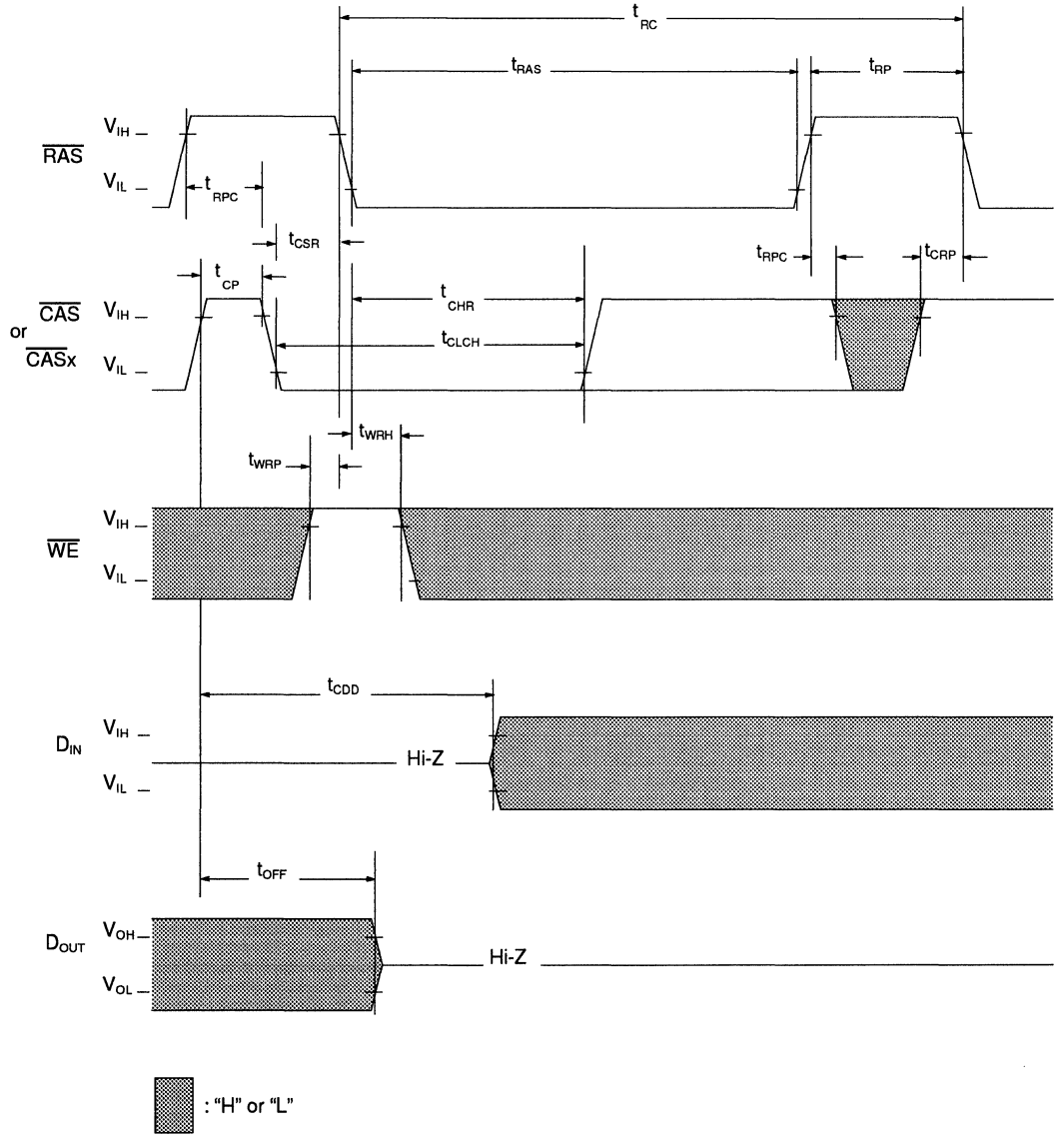


$\overline{RAS}$ Only Refresh Cycle



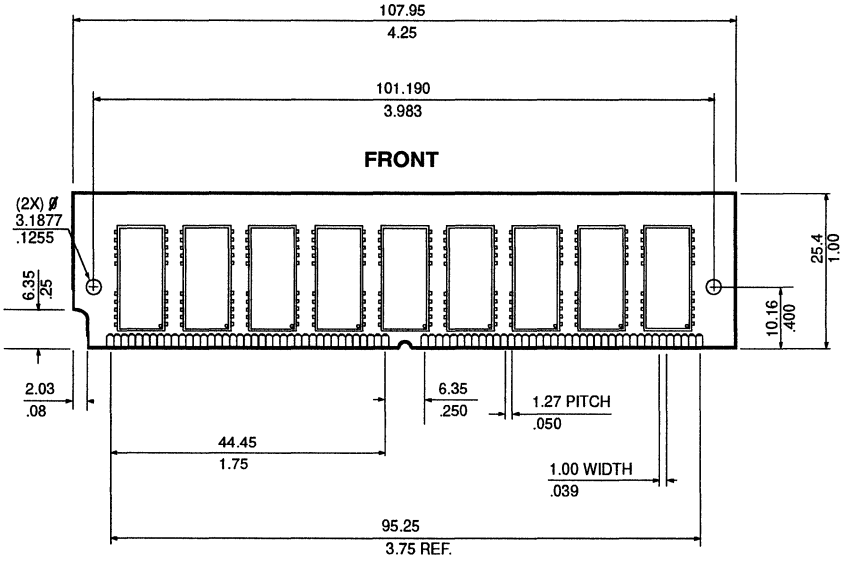
Note: $\overline{WE}$, D_{IN} are "H" or "L"

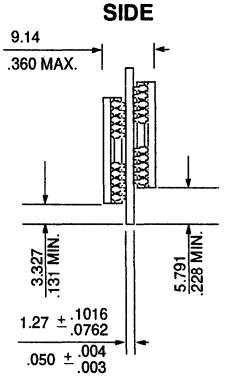
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 36 DRAM Module

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Manufactured with 18Mb DRAMS (1M x 18)
- Single 5V, ± 0.5V Power Supply
- Low current consumption
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write parity applications.
- Au and Sn/Pb versions available

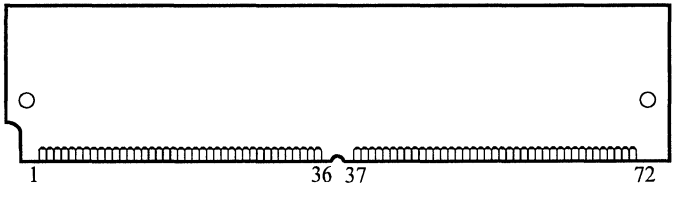
Description

The IBM11D2360L is an 8MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 2Mx36 high speed memory array, and is configured as 2 1Mx36 banks - each independently selectable via unique $\overline{RAS}$ inputs. The assembly is intended for use in 18, 36 and 72 bit applications. It is manufactured with 4 1Mx18 devices, each in a 400mil TSOP package, and is compatible with the JEDEC 72-Pin SIMM standard.

This assembly is intended as a direct replacement for 1Mx4-based SIMMs, while significantly reducing power dissipation. The use of TSOP packages allows tighter SIMM spacing (.3" on center). Input loading is consistent with 4Mb-based assemblies due to the addition of discrete capacitors - maximizing compatibility at the system-level.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 2Mx36 parity SIMM, IBM11D2360B, as well as other density, parity and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 36	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

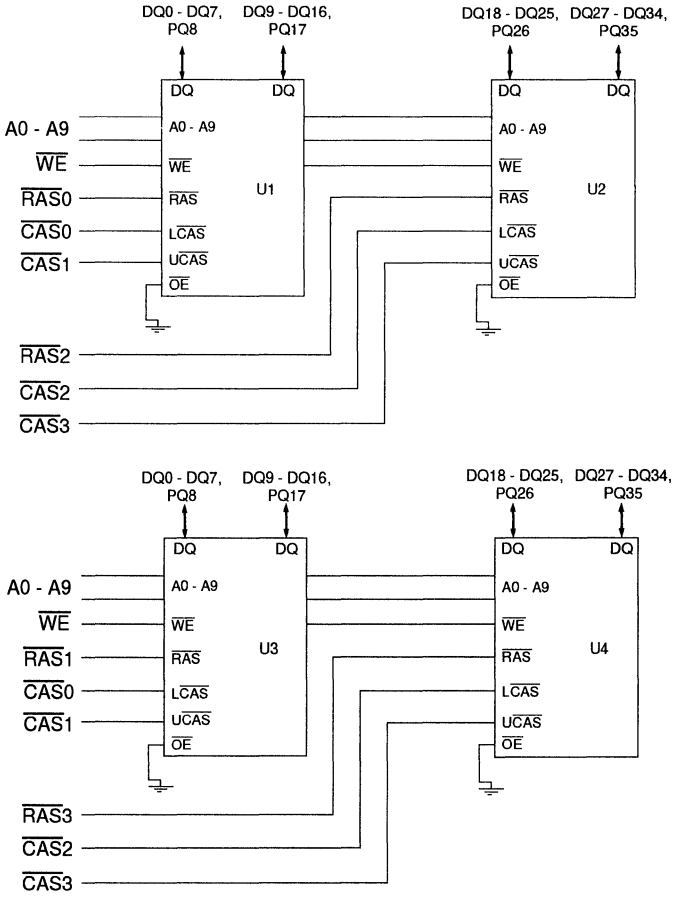
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D2360LA-60	2M x 36	60ns	Sn/Pb	4.25" x 1" x .154"	
IBM11D2360LA-70	2M x 36	70ns	Sn/Pb	4.25" x 1" x .154"	
IBM11E2360LA-60	2M x 36	60ns	Au	4.25" x 1" x .154"	
IBM11E2360LA-70	2M x 36	70ns	Au	4.25" x 1" x .154"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	NC	NC
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	4.6	W	1,2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	90	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	44	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	47	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	94	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34, PQ8, PQ17, PQ26, PQ35)	25	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	424	mA	1, 2, 3
		-70	—	374		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	8	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	424	mA	1, 3, 4
		-70	—	374		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	184	mA	1, 2, 3
		-70	—	164		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	4	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	424	mA	1, 3, 4
		-70	—	374		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-10	+10	µA	
		$\overline{CAS}$	-10	+10		
		All others	-40	+40		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. Refresh current is specified for 1 bank.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

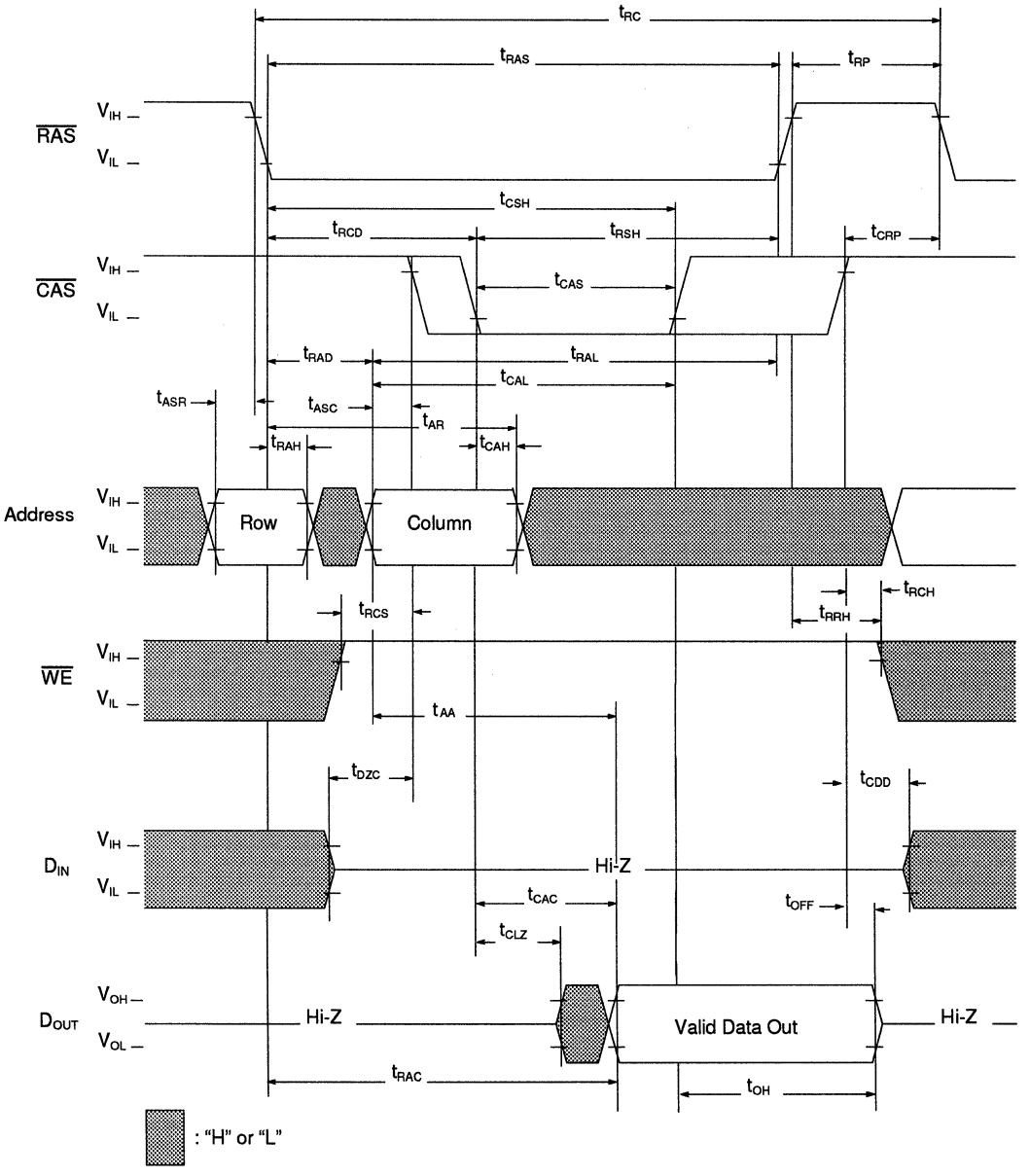
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

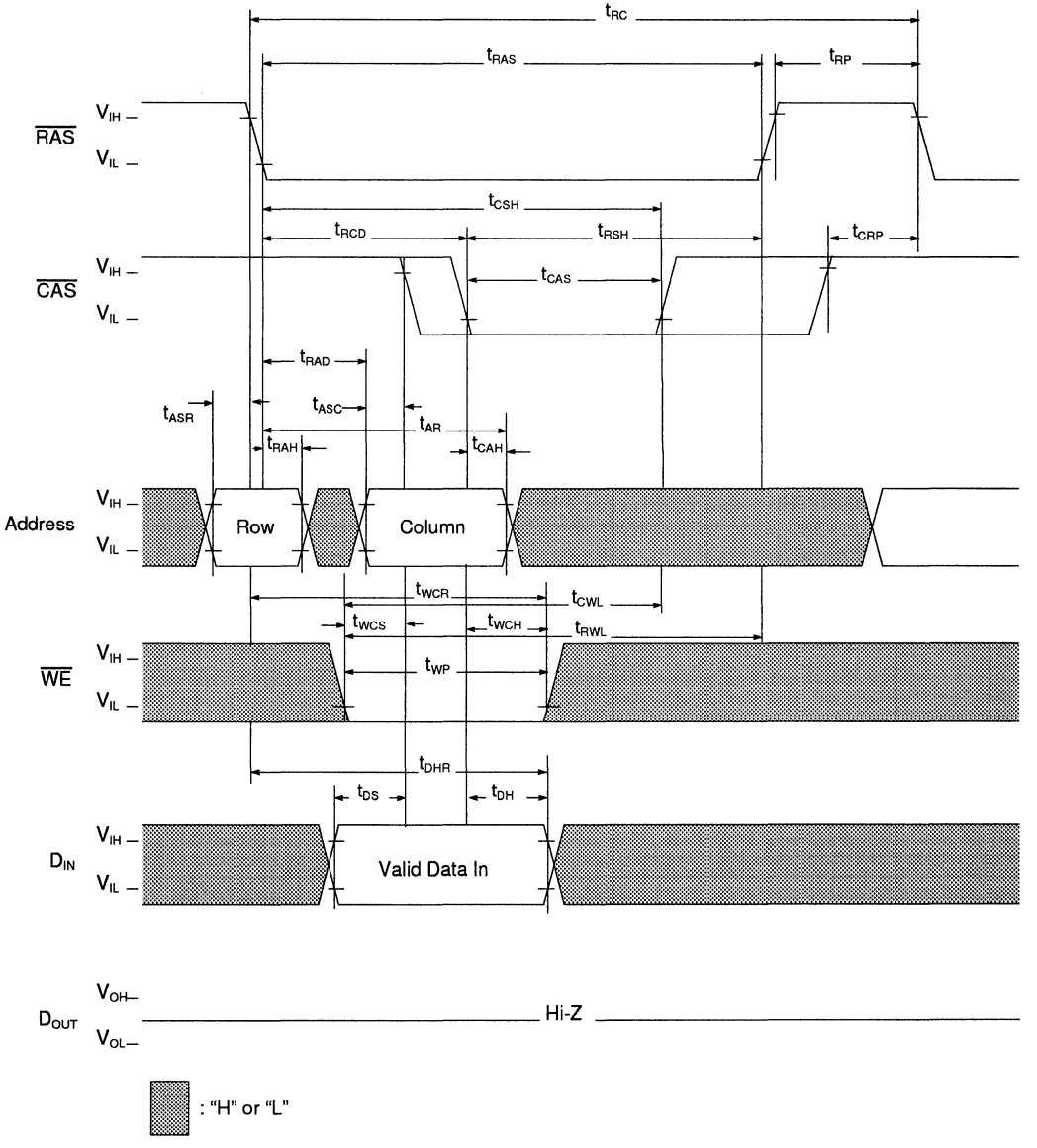
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms.

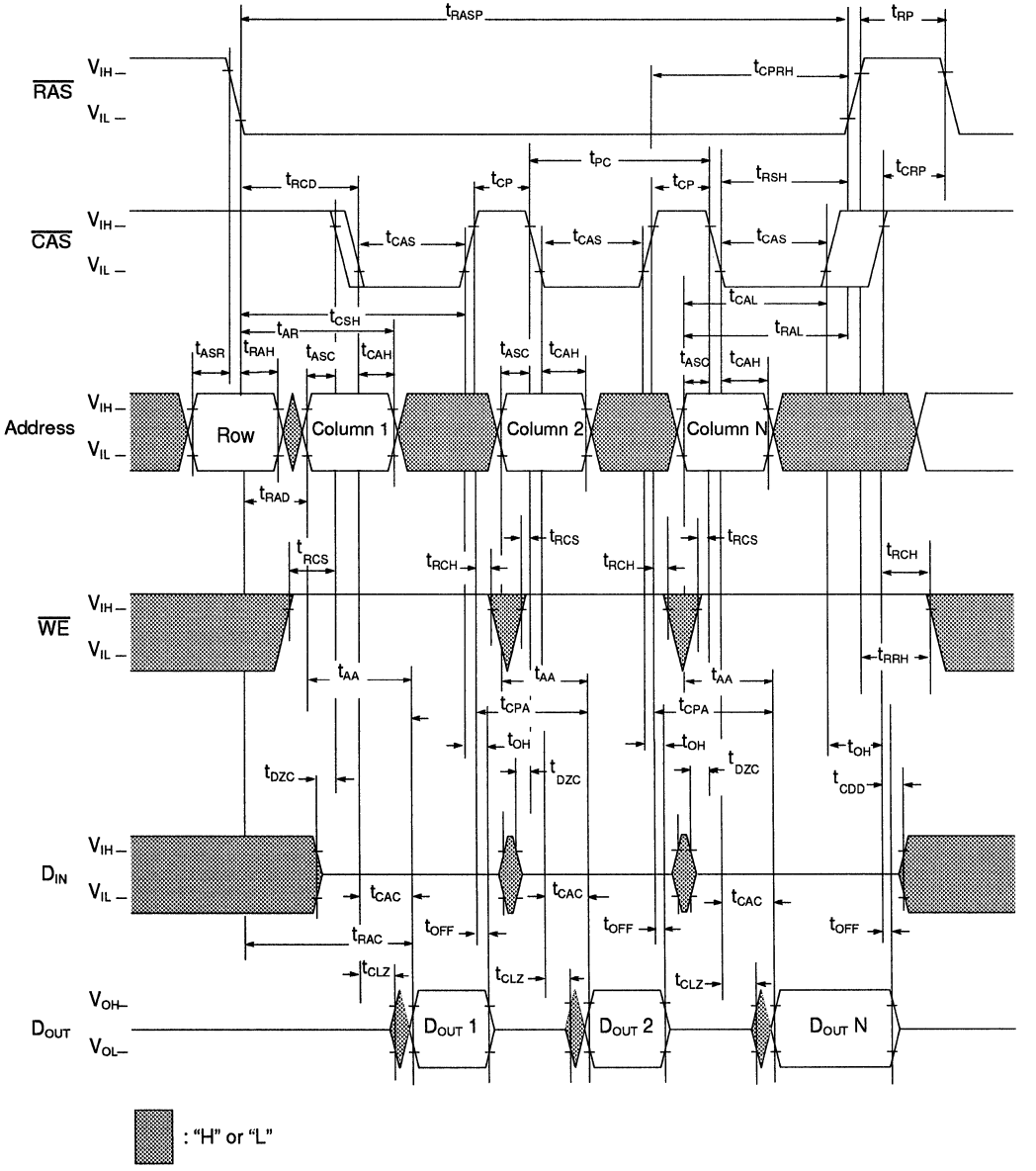
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

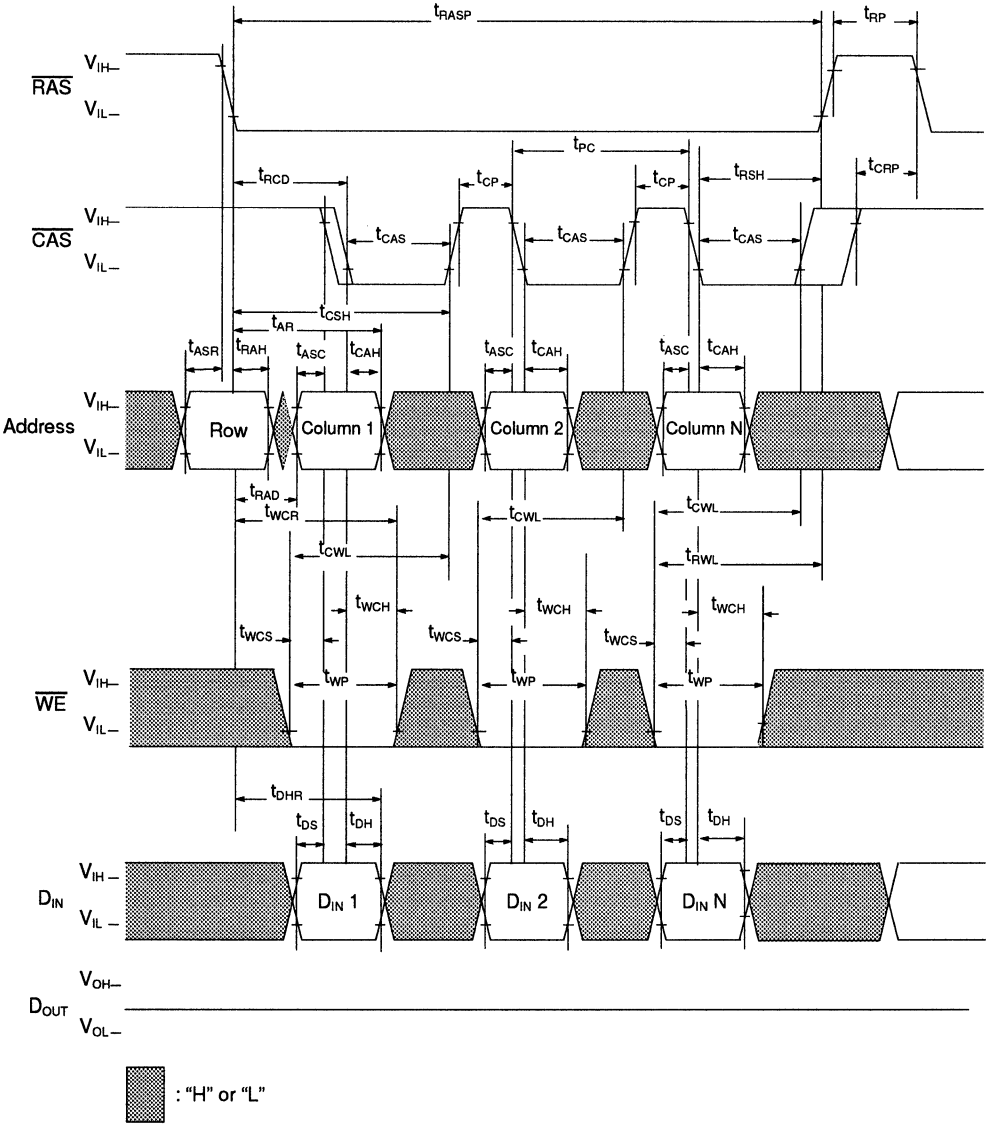
Write Cycle (Early Write)



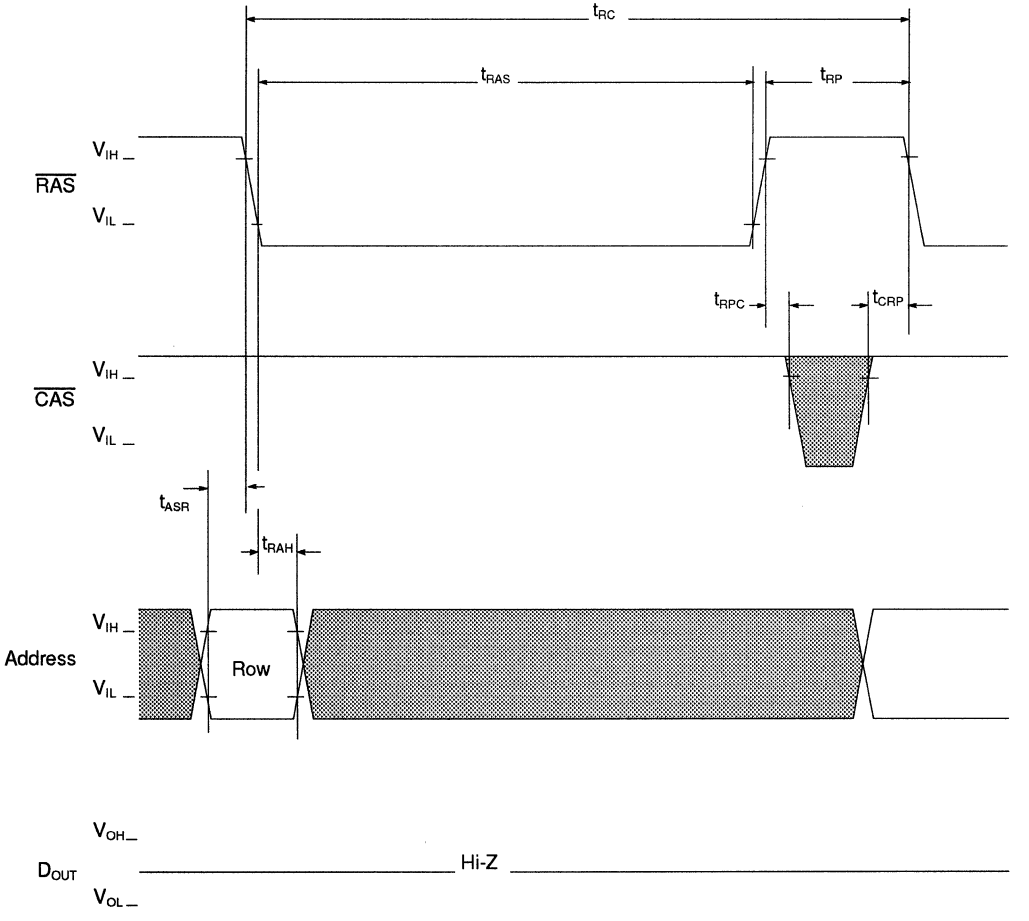
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

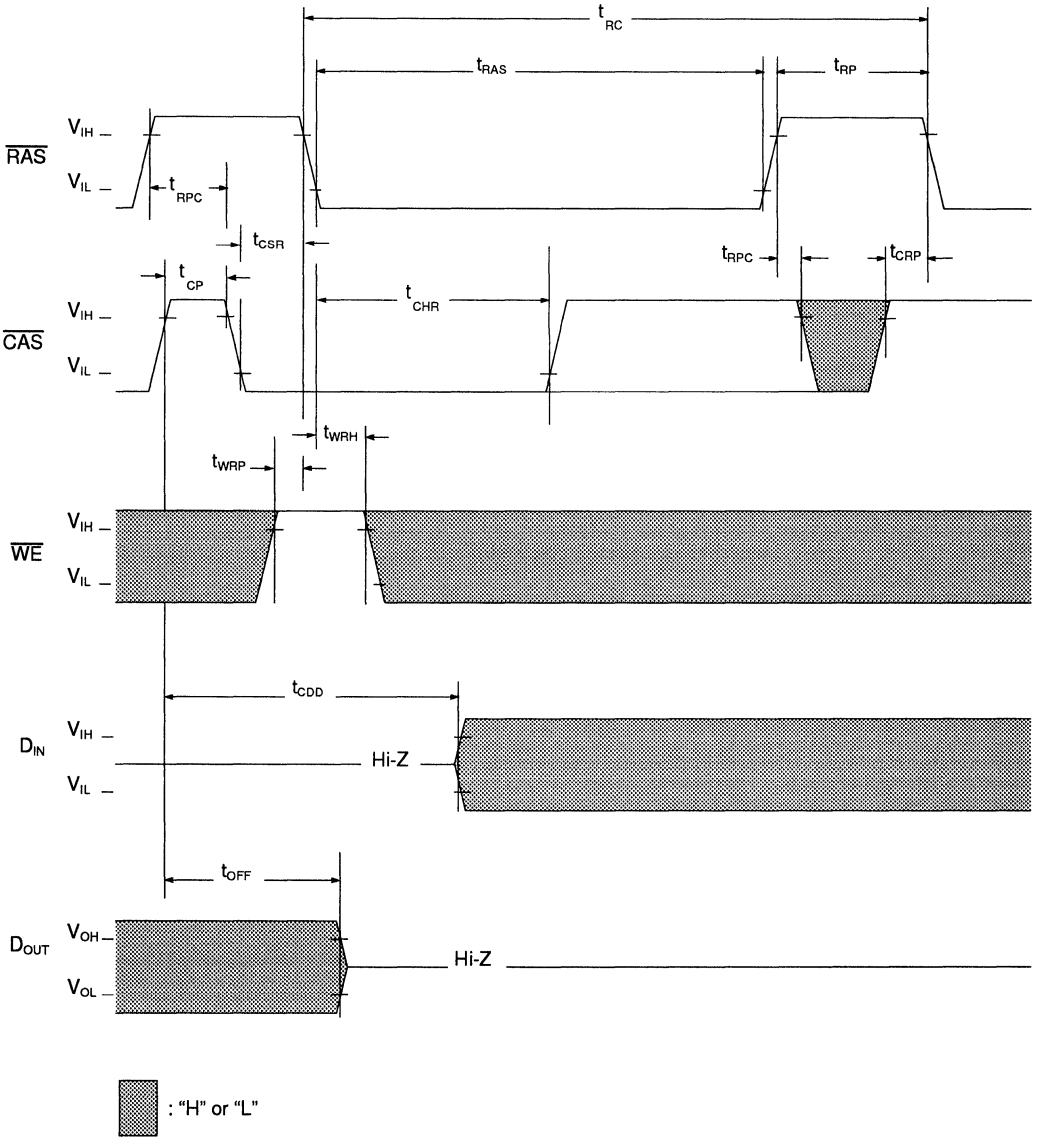


$\overline{RAS}$ Only Refresh Cycle



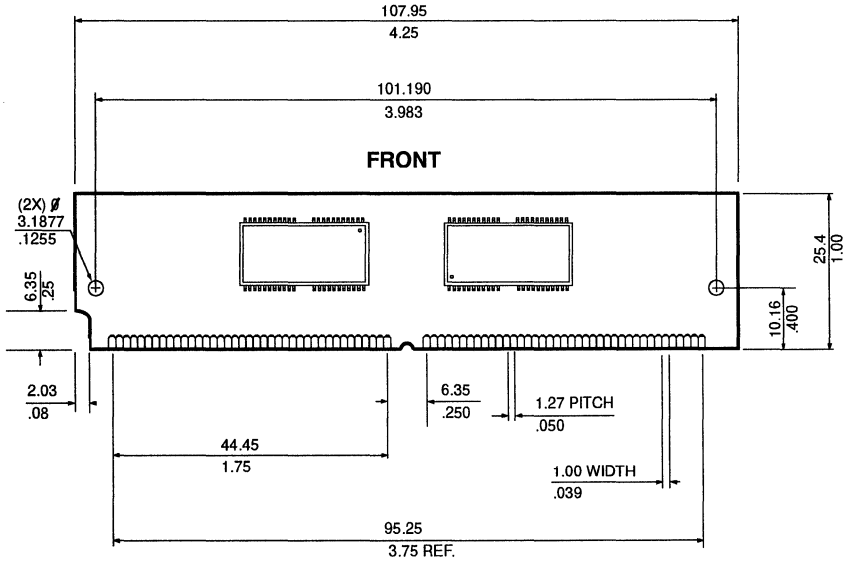
Note: $\overline{WE}$, D_{IN} are "H" or "L"

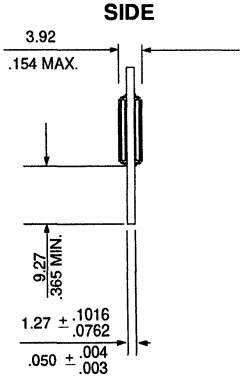
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Preliminary

4M x 36 DRAM Module

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

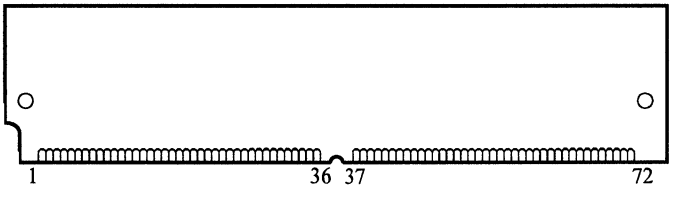
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: RAS-Only and CBR
- 2048 refresh cycles distributed across 32ms
- 11/11 Addressing (Row/Column)
- Optimized for use in byte-write parity applications
- Au and Sn/Pb versions available

Description

The IBM11D4360B is a 16MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 4Mx36 high speed memory array that is intended for use in 18, 36, and 72 bit parity applications. It is manufactured with 8 4Mx4 devices, each in a 300mil package, and 4 4Mx1 devices in a 300mil package. The module is compatible with the JEDEC 72-pin SIMM standard.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 4Mx32 non-parity SIMM, IBM11D4320B, as well as other density and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

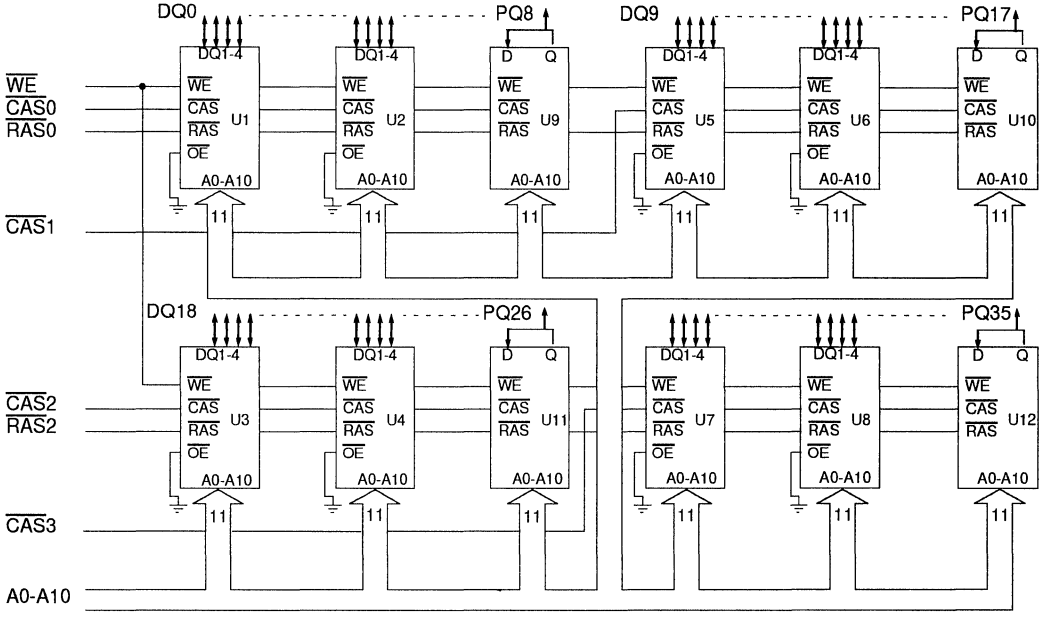
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	A10	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D4360BA-60	4M x 36	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D4360BA-70	4M x 36	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E4360BA-60	4M x 36	60ns	Au	4.25" x 1" x .360"	
IBM11E4360BA-70	4M x 36	70ns	Au	4.25" x 1" x .360"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V_{SS}	V_{SS}
PD2	NC	NC
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min(V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min(V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	7.9	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	Vcc + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A10)	78	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	50	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	31	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	94	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	13	pF	
$C_{I/O2}$	Output Capacitance (PQ8, 17, 26, 35)	18	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1440	mA	1, 2, 3
		-70	—	1280		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	24	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	1440	mA	1, 3
		-70	—	1280		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1240	mA	1, 2, 3
		-70	—	1080		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	12	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1440	mA	1, 3
		-70	—	1280		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$	-30	+30		
		All others	-120	+120		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	45	—	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	45	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

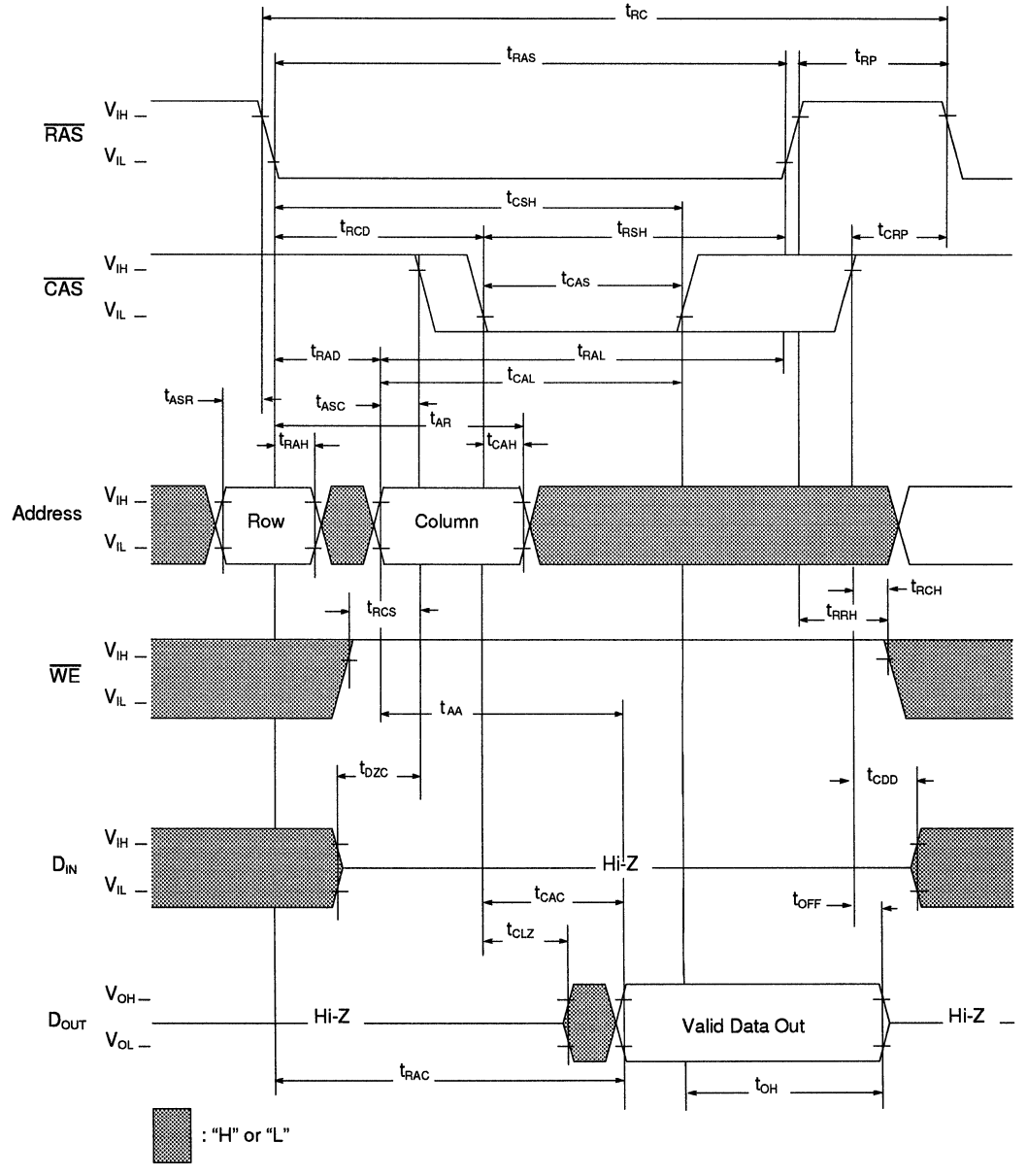
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Measured with the specified current load and 100pF.

Refresh Cycle

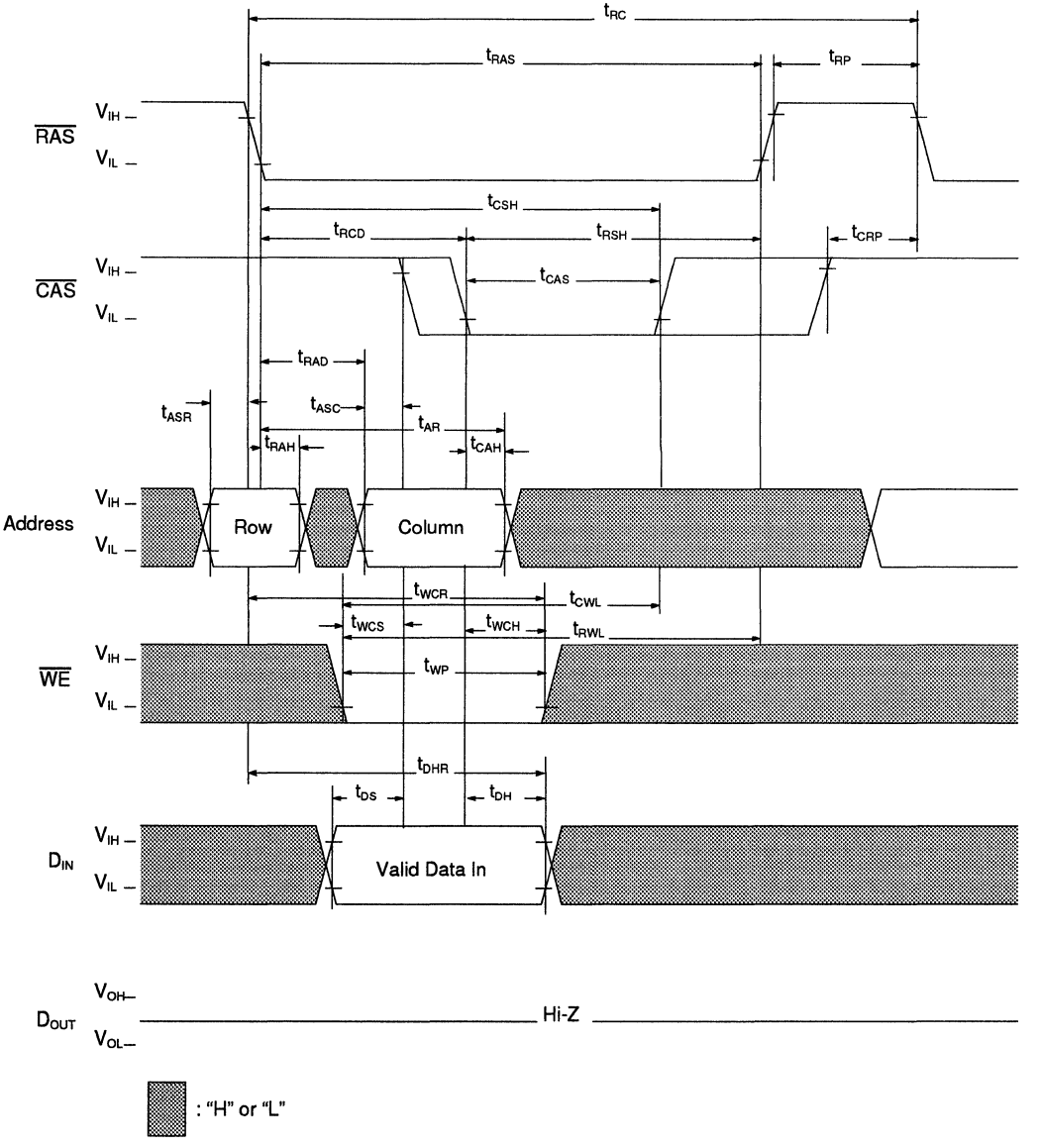
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	
t_{REF}	Refresh Period	—	32	—	32	ms	1

1. 2048 refreshes are required every 32ms.

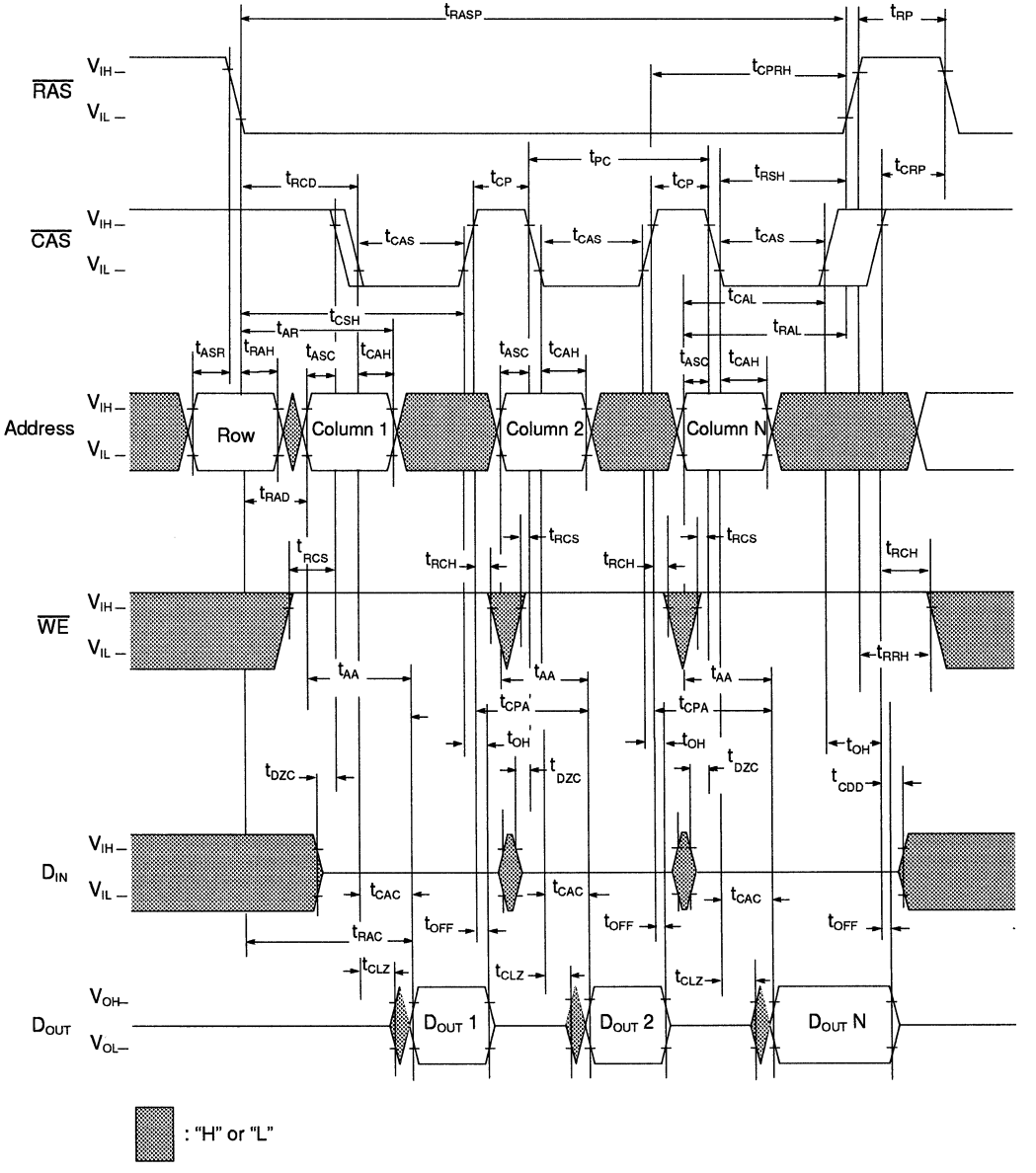
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

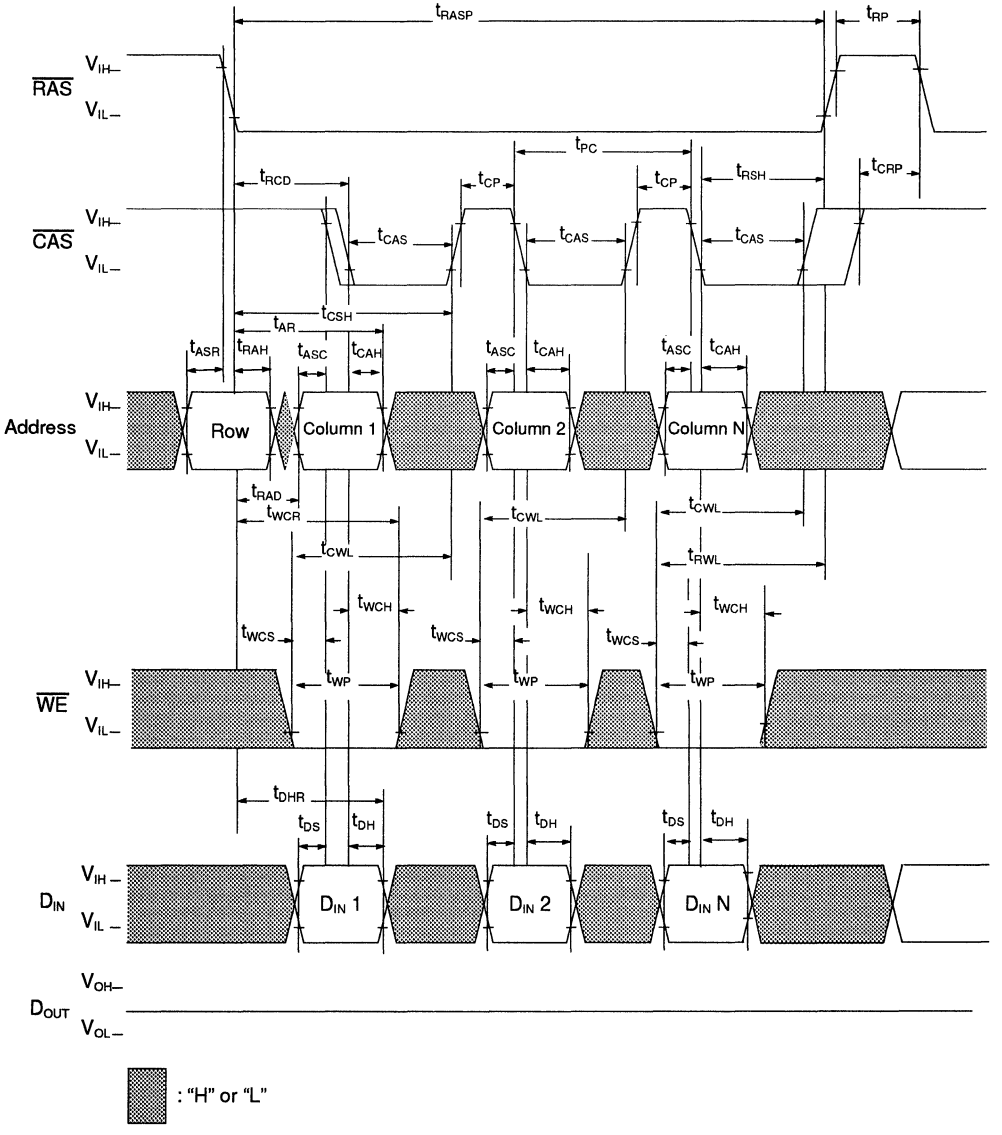
Write Cycle (Early Write)



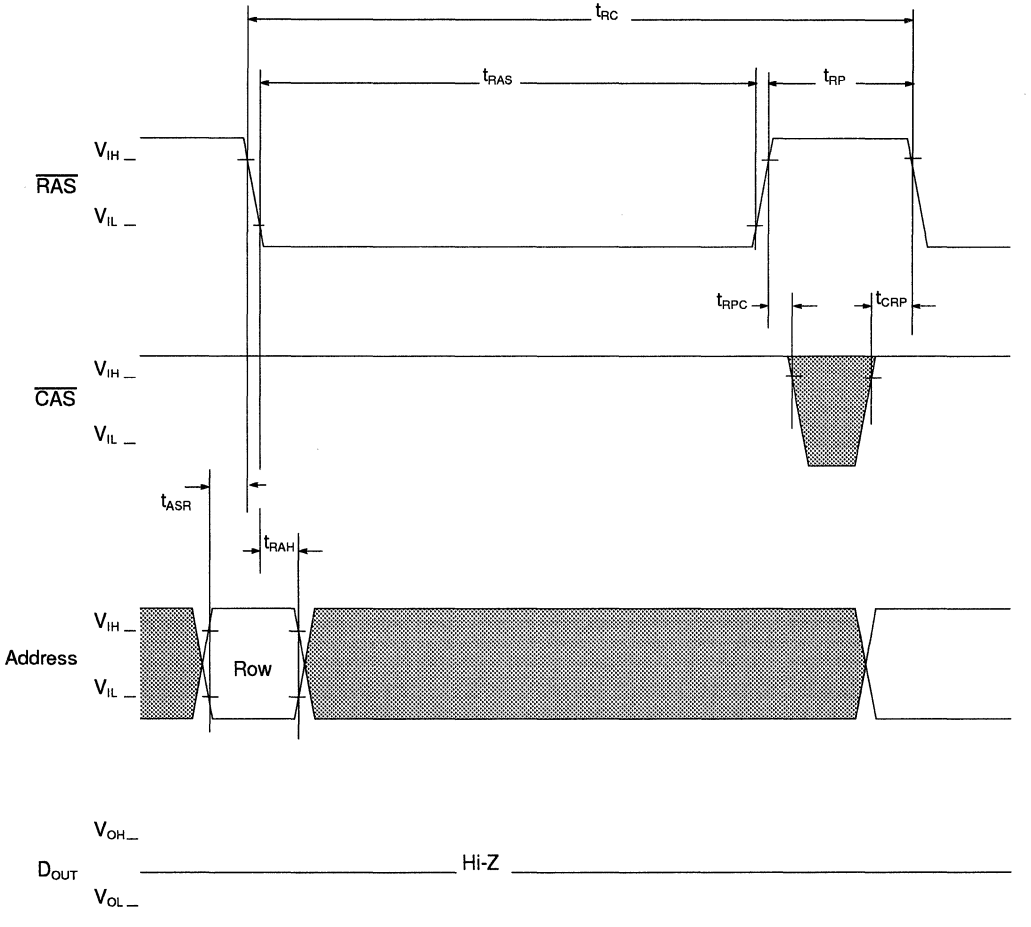
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

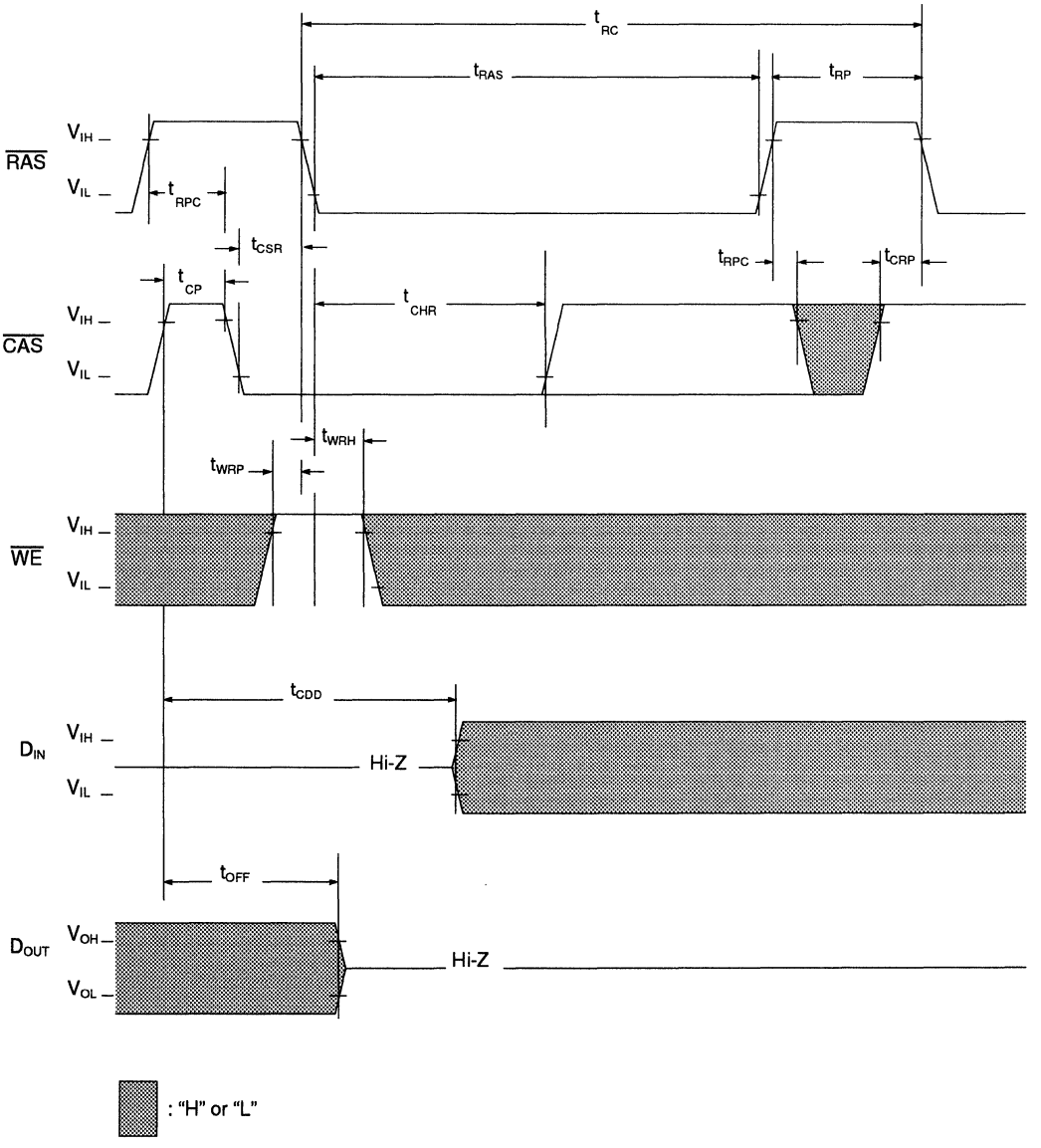


$\overline{RAS}$ Only Refresh Cycle



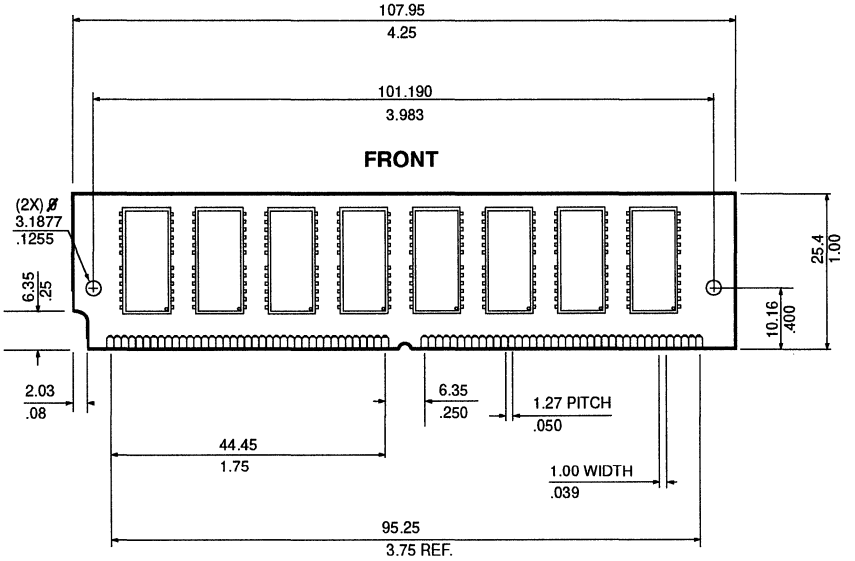
Note: $\overline{WE}$, D_{IN} are "H" or "L"

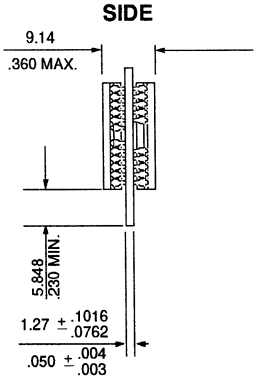
CAS Before RAS Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Preliminary

8M x 36 DRAM Module

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 2048 refresh cycles distributed across 32ms
- 11/11 Addressing (Row/Column)
- Optimized for use in byte-write parity applications
- Au and Sn/Pb versions available

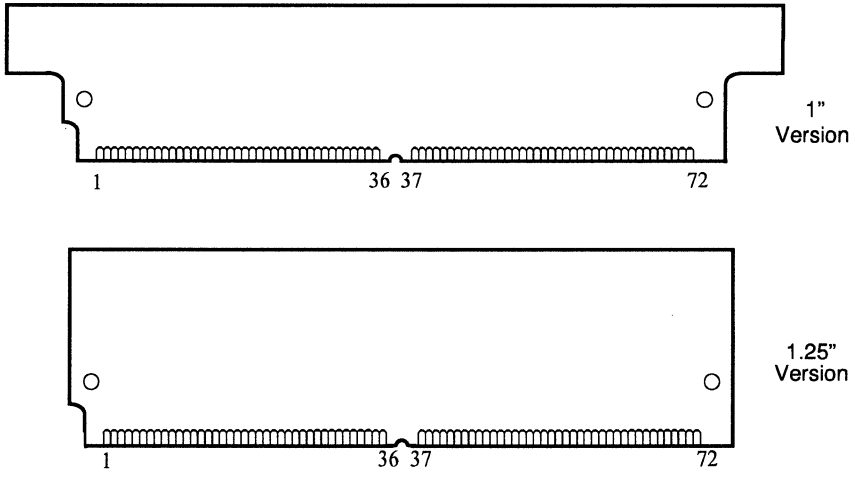
Description

The IBM11D8360B is a 32MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as an 8Mx36 high speed memory array, and is configured as 2 4Mx36 banks - each independently selectable via unique $\overline{RAS}$ inputs. The assembly is intended for use in 18, 36 and 72 bit parity applications. It is manufactured with 16 4Mx4 devices, each in a 300mil package, and 8 4Mx1 devices in a 300mil package. The module is compatible with the JEDEC 72-Pin SIMM standard.

Two package offerings are available to accomodate system spacing requirements.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 8Mx32 non-parity SIMM, IBM11D8320B, as well as other density offerings and ECC-optimized SIMMs.

Card Outlines



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

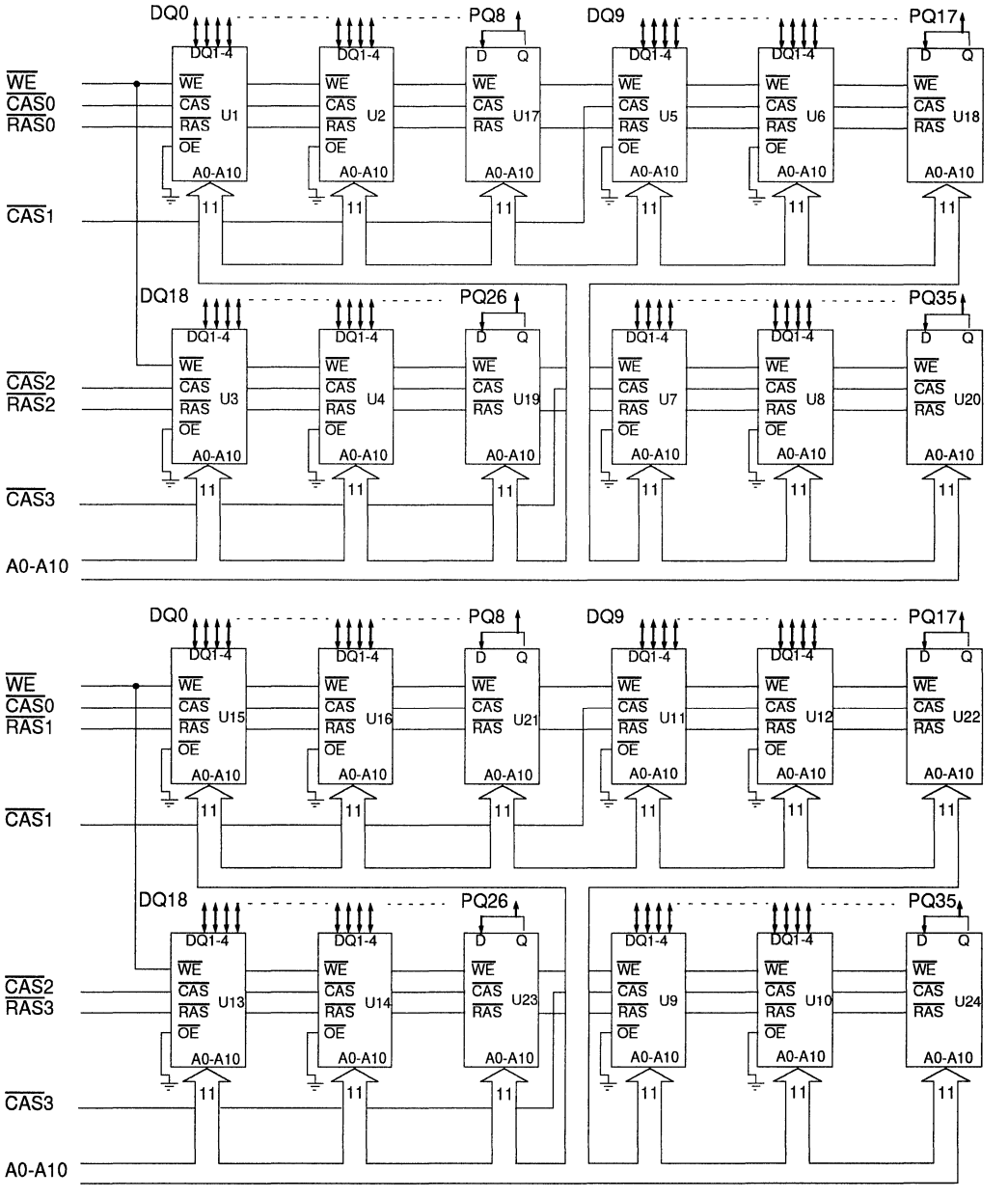
Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	A10	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D8360BA-60	8M x 36	60ns	Sn/Pb	5" x 1" x .360"	Wide
IBM11D8360BA-70	8M x 36	70ns	Sn/Pb	5" x 1" x .360"	Wide
IBM11E8360BA-60	8M x 36	60ns	Au	5" x 1" x .360"	Wide
IBM11E8360BA-70	8M x 36	70ns	Au	5" x 1" x .360"	Wide
IBM11D8360BB-60	8M x 36	60ns	Sn/Pb	4.25" x 1.25" x .360"	Tall
IBM11D8360BB-70	8M x 36	70ns	Sn/Pb	4.25" x 1.25" x .360"	Tall
IBM11E8360BB-60	8M x 36	60ns	Au	4.25" x 1.25" x .360"	Tall
IBM11E8360BB-70	8M x 36	70ns	Au	4.25" x 1.25" x .360"	Tall

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to + 70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	15.8	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A10)	161	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	57	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	57	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	188	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	27	pF	
$C_{I/O2}$	Output Capacitance (PQ8, 17, 26, 35)	37	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1464	mA	1, 2, 3
		-70	—	1304		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	48	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1464	mA	1, 3, 4
		-70	—	1304		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1264	mA	1, 2, 3
		-70	—	1104		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	24	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1464	mA	1, 3, 4
		-70	—	1304		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$	-60	+60		
		All others	-240	+240		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for 1 bank.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	45	—	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	45	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

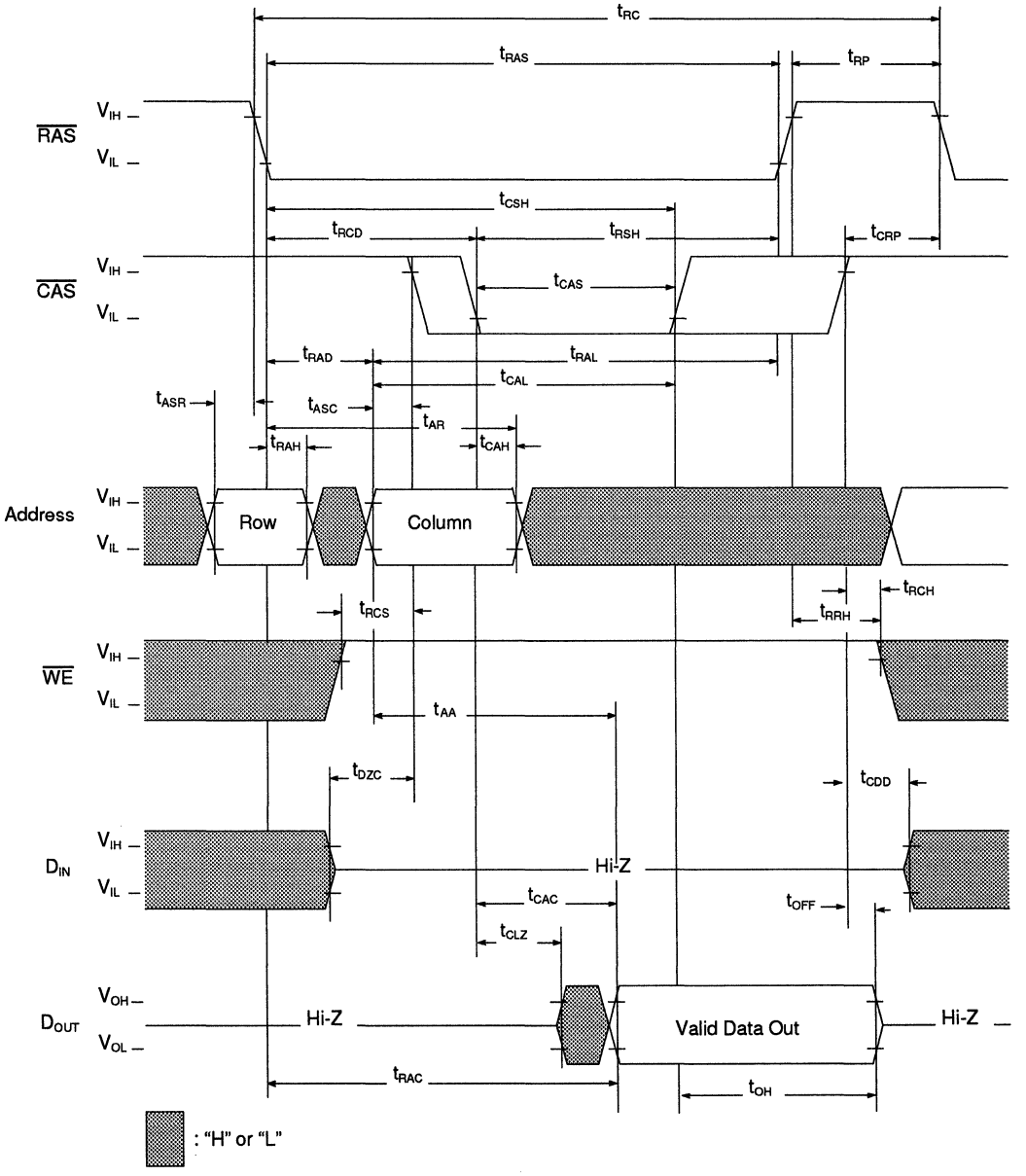
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Measured with the specified current load and 100pF.

Refresh Cycle

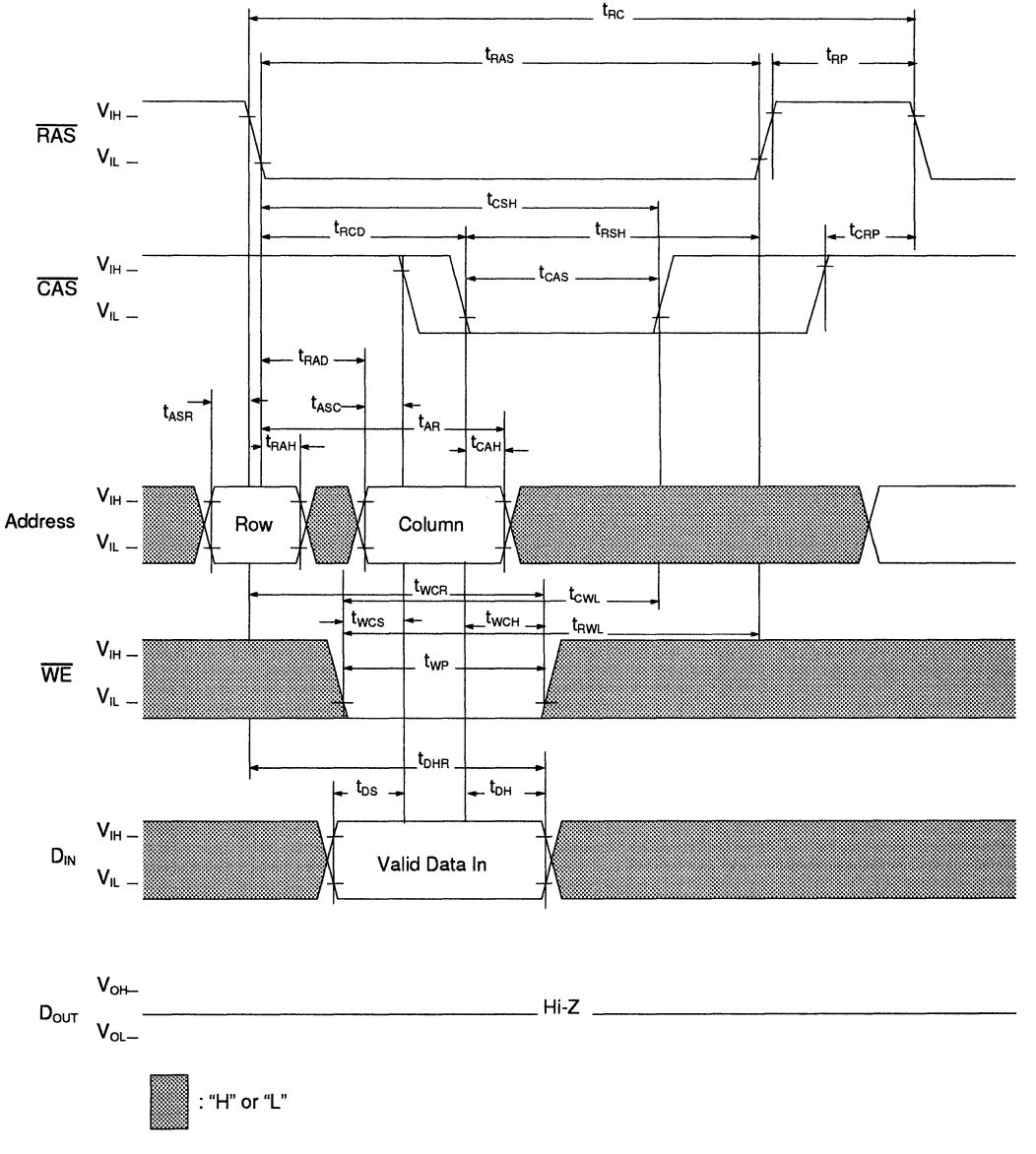
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	
t_{REF}	Refresh Period	—	32	—	32	ms	1

1. 2048 refreshes are required every 32ms.

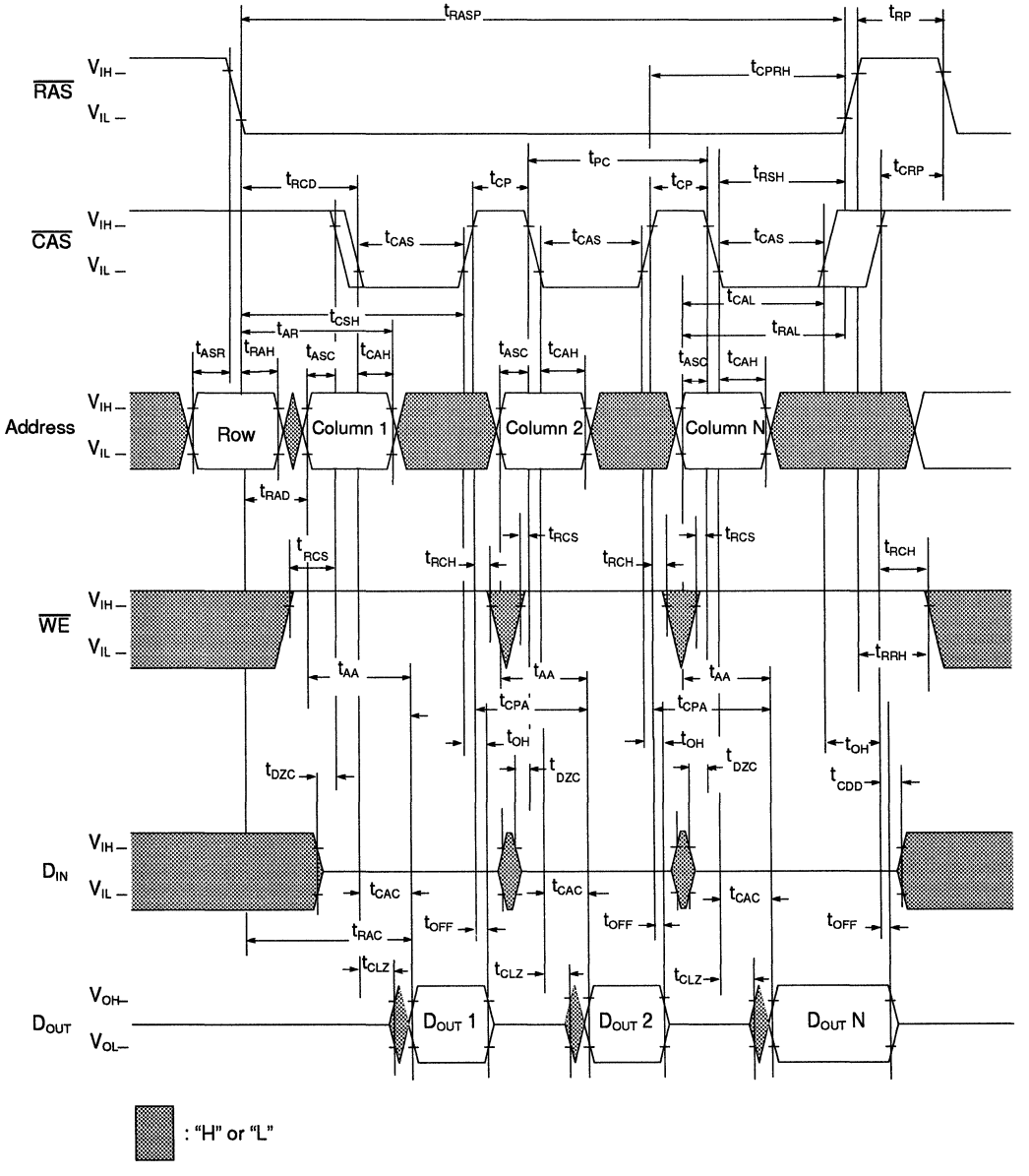
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

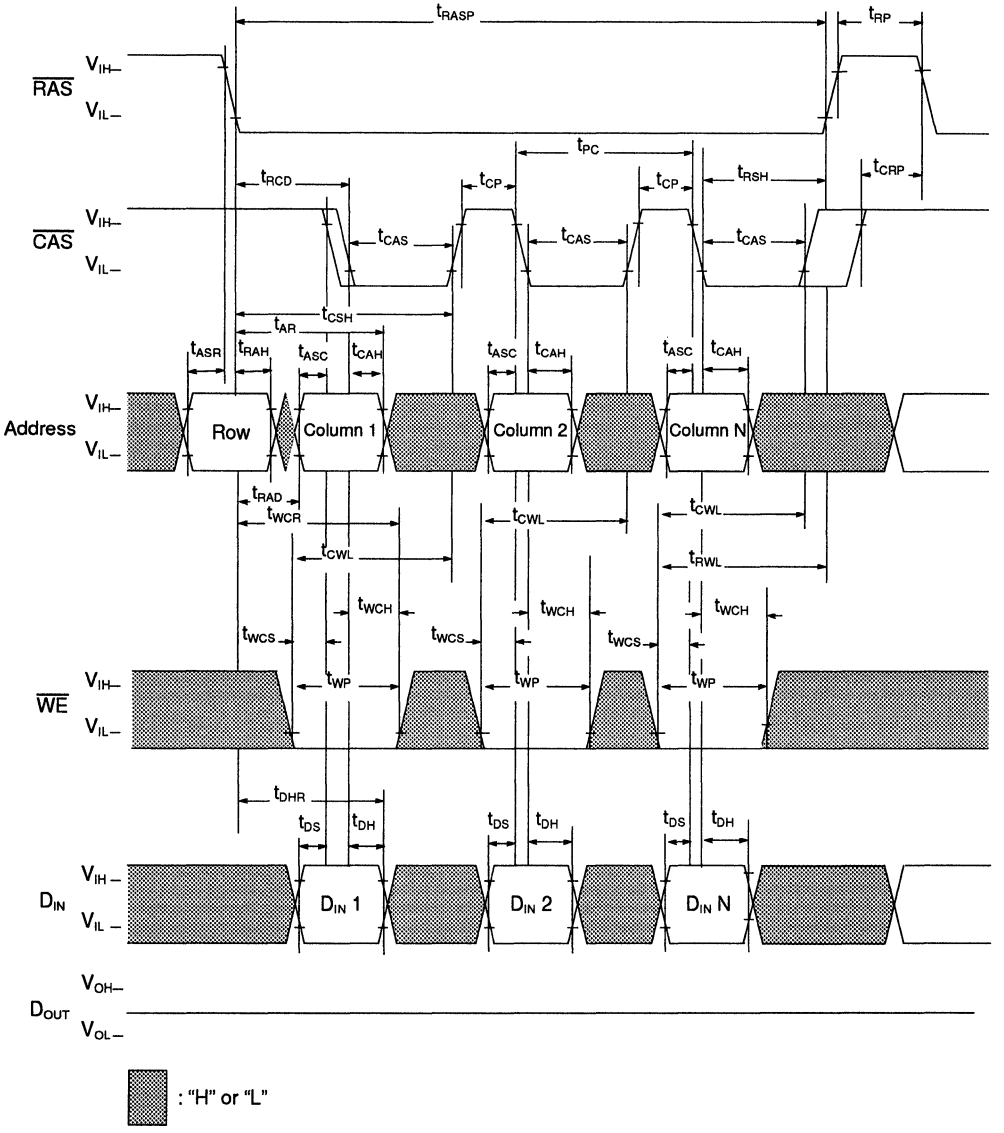
Write Cycle (Early Write)



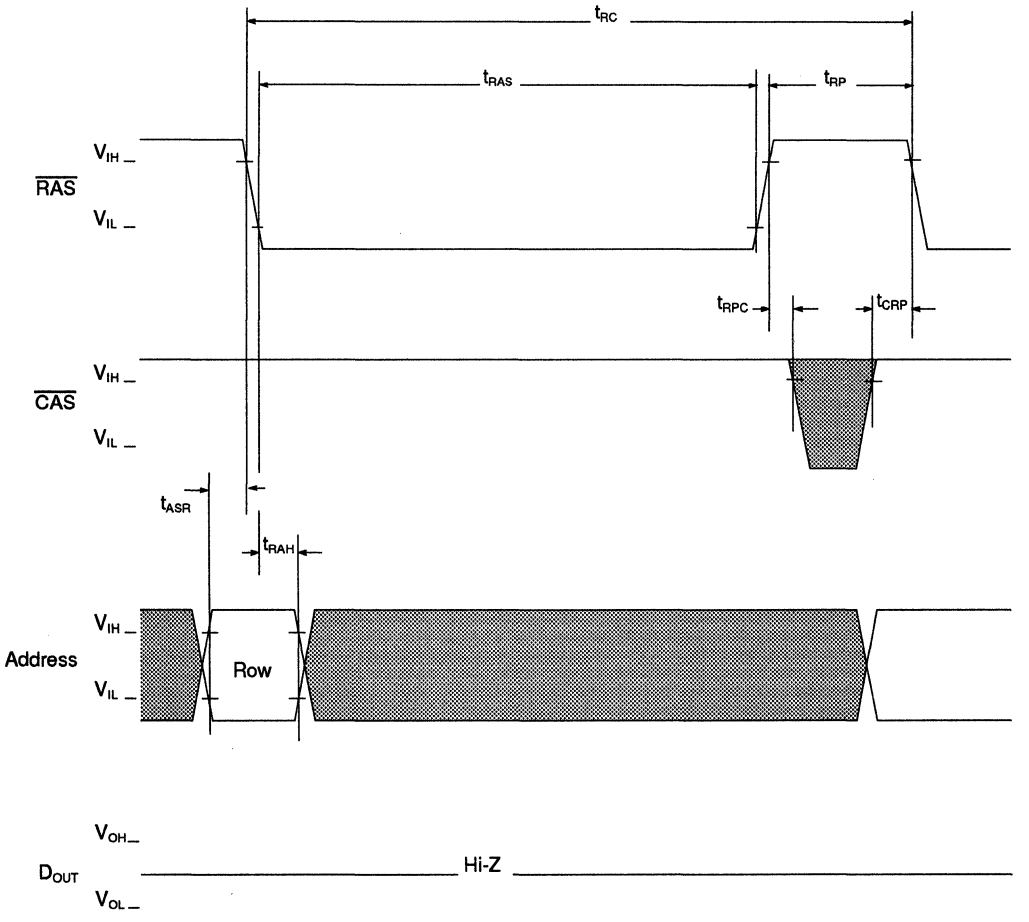
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

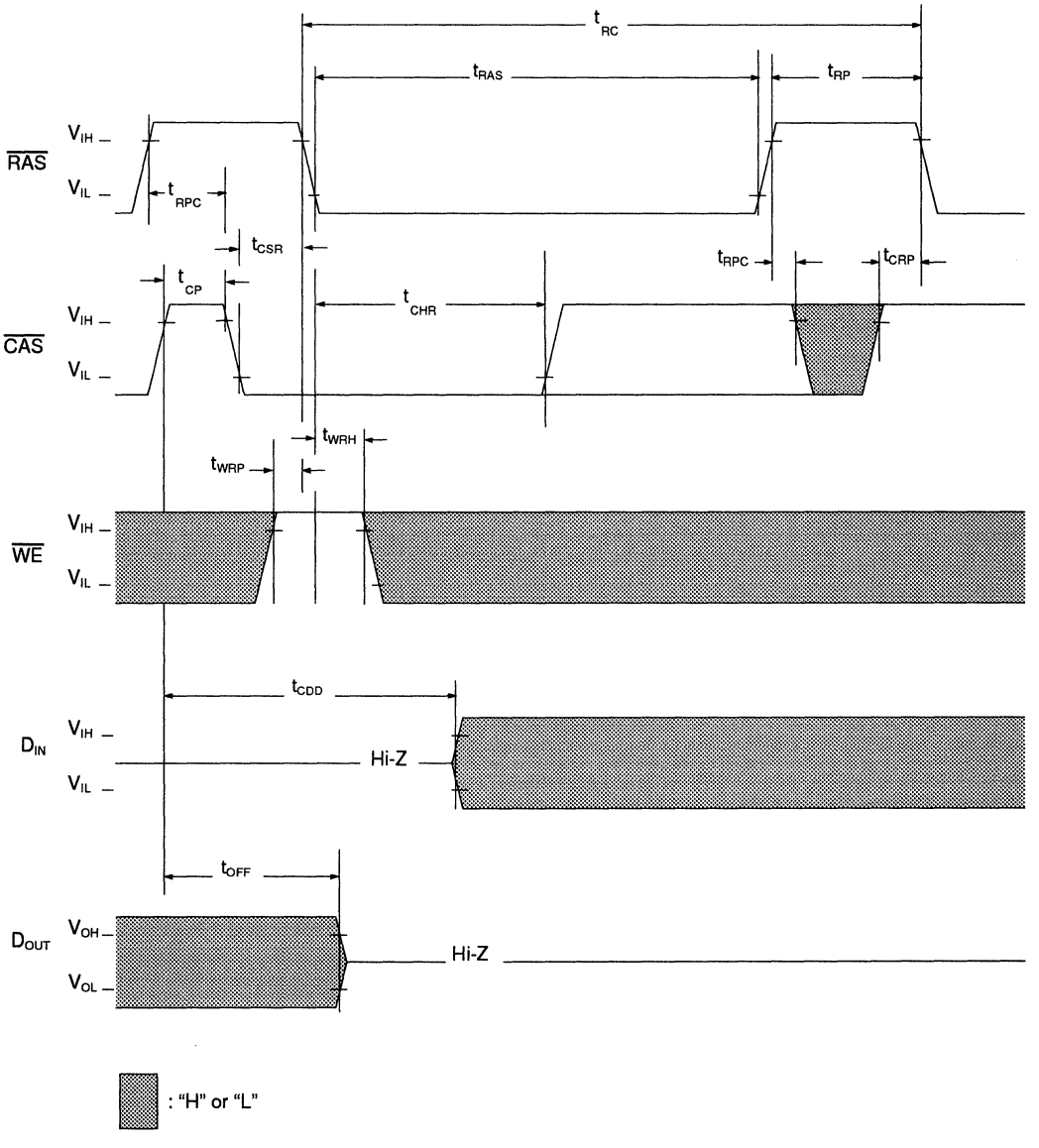


$\overline{RAS}$ Only Refresh Cycle



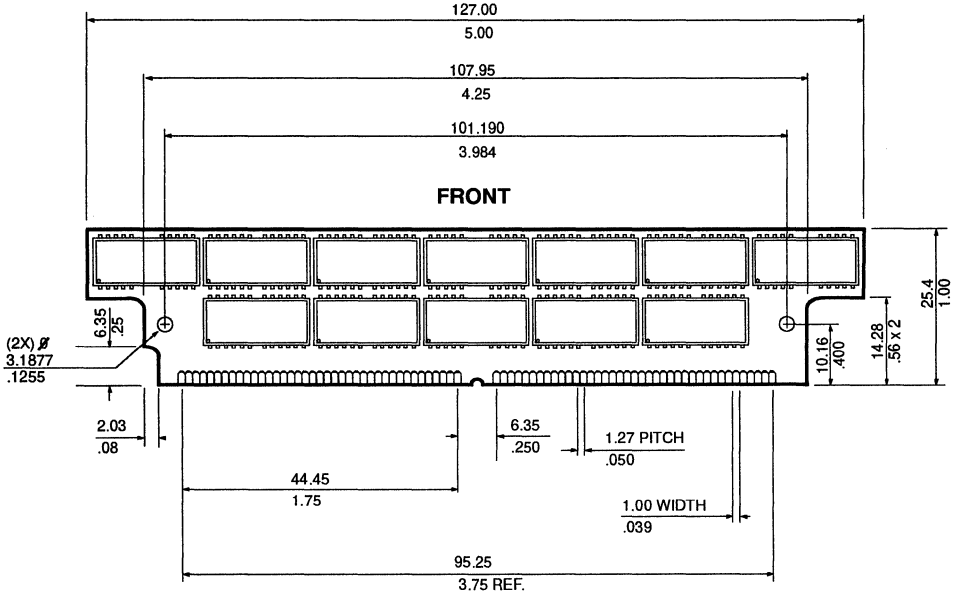
Note: $\overline{WE}$, D_{IN} are "H" or "L"

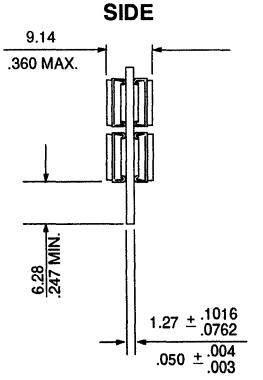
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

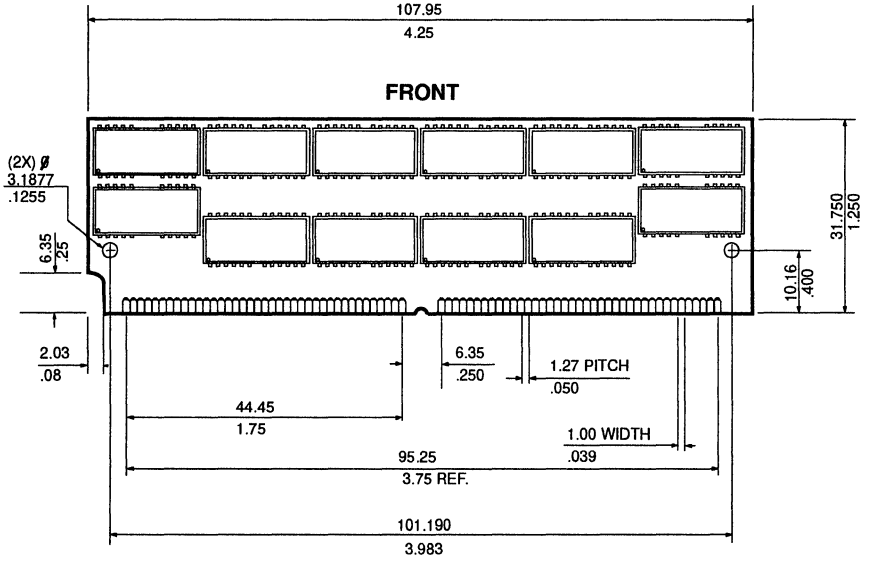
Layout Drawing (IBM11D8360BA)

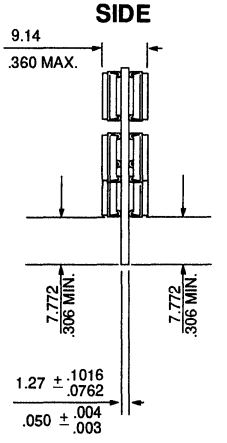




NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Layout Drawing (IBM11D8360BB)





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

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72 Pin SIMMs

- *ECC*

1M x 36/1M x 40 DRAM Modules

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

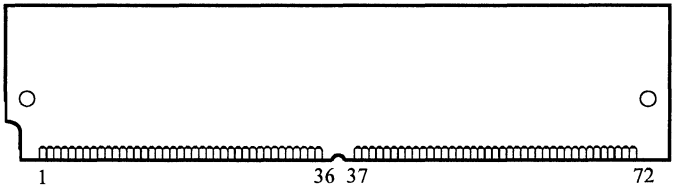
- Optimized for use in ECC applications
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode, Read-Modify-Write cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Au and Sn/Pb versions available

Description

The ECC-Optimized SIMMs, IBM11D1370BA and IBM11D1400BA are 4MB industry standard 72 pin 4-byte single inline memory modules (SIMMs). The Modules are organized as 1M x 36/40 high speed memory arrays, and are configured as a single 1M x 36/40 bank. The 1M x 36 assembly is intended for use in 8 byte applications, typically having 64 data and 8 check bits (64/72 code). The 1M x 40 assembly is applicable to 4 byte applications with 32 data and 7 or 8 check bits (32/39 code), or 8 byte applications with extended error correction capabilities. The modules are manufactured with 9 or 10 1M x 4 devices, each in a 350 mil package, and are compatible with the JEDEC 72-pin SIMM standard.

The IBM 72-pin SIMMs provide a high-performance, flexible 4-byte interface in a 4.25" long footprint. Related products include other density offerings and parity SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$	Row Address Strobe
$\overline{CAS0}$	Column Address Strobe
$\overline{WE}$	Read/write Input
$\overline{OE}$	Output Enable
A0 - A9	Address Inputs
DQ0-35 or DQ0-39	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
$\overline{ECC}$, PD1 - PD4	Presence Detects

Pinout

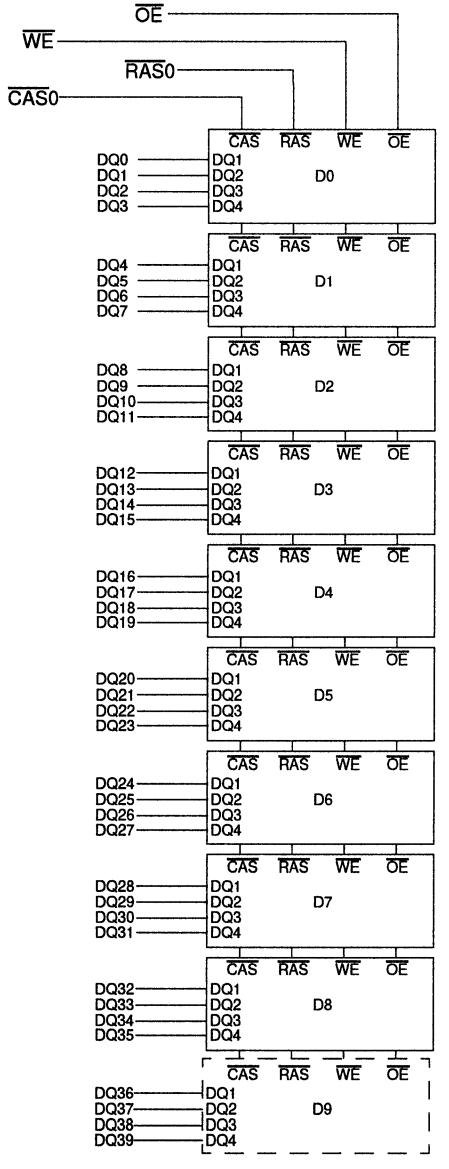
Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	NC	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{OE}$	31	A8	43	NC	55	DQ28	67	PD1
8	DQ6	20	DQ8	32	A9	44	$\overline{RAS0}$	56	DQ29	68	PD2
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ30	69	PD3
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD4
11	NC	23	DQ11	35	DQ17	47	$\overline{WE}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	$\overline{ECC}$	60	DQ32	72	V_{SS}

1. DQ36 - DQ39 are NC for x36 SIMM.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D1370BA-60	1M x 36	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D1370BA-70	1M x 36	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E1370BA-60	1M x 36	60ns	Au	4.25" x 1" x .360"	
IBM11E1370BA-70	1M x 36	70ns	Au	4.25" x 1" x .360"	
IBM11D1400BA-60	1M x 40	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D1400BA-70	1M x 40	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E1400BA-60	1M x 40	60ns	Au	4.25" x 1" x .360"	
IBM11E1400BA-70	1M x 40	70ns	Au	4.25" x 1" x .360"	

Block Diagram



NOTE: D9 IS NOT USED IN X36 SIMM

A0 - A9 → A0 - A9: DRAMS D0 - D9

VCC → D0 - D9

VSS → D0 - D9

Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Col Address	All DQ Bits
Standby	H	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	Valid Data Out
Early-Write	L	L	L	X	Row	Col	Valid Data In
Late-Write / RMW	L	L	H→L	L→H	Row	Col	Valid Data Out, Valid Data In
Fast Page Mode-Read 1st cycle	L	H→L	H	L	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	Valid Data Out
Fast Page Mode-Write 1st cycle	L	H→L	L	X	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	Valid Data In
Fast Page Mode Read-Modify-Write: 1st cycle	L	H→L	H→L	L→H	Row	Col	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	L→H	N/A	Col	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	High Impedance

Presence Detect

Pin	-60	-70
$\overline{ECC}$ (ECC Optimized SIMM)	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +6.5	V	1
V_{IN}	Input Voltage	-0.7 to V_{CC} + 0.7	V	1
V_{OUT}	Output Voltage	-0.7 to V_{CC} + 0.7	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	5.9	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	x36 Max	x40 Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	55	58	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	50	53	pF	
C_{I3}	Input Capacitance ($\overline{WE}$)	47	50	pF	
C_{I4}	Input Capacitance ($\overline{OE}$)	65	70	pF	
$C_{I/O}$	Output Capacitance (All DQ bits)	13	13	pF	

1M x 36 DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1080	mA	1, 2, 3
		-70	—	972		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	18	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1080	mA	1, 3
		-70	—	972		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	675	mA	1, 2, 3
		-70	—	630		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	18	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1080	mA	1, 3
		-70	—	972		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{OE}$, $\overline{WE}$, ADDRESS	-90	+90	µA	
		$\overline{RAS}$, $\overline{CAS}$	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}

1M x 40 DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1200	mA	1, 2, 3
		-70	—	1080		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	20	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1200	mA	1, 3
		-70	—	1080		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	750	mA	1, 2, 3
		-70	—	700		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	20	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1200	mA	1, 3
		-70	—	1080		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{OE}$, $\overline{WE}$, ADDRESS	-100	+100	µA	
		$\overline{RAS}$, $\overline{CAS}$	-100	+100		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	10	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	—	—	—	—	ns	3
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	—	—	—	—	ns	3
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	—	—	—	—	ns	3
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	45	—	50	—	—	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	1
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	3
t_{DH}	D_{IN} Hold Time	10	—	15	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	15	—	20	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OES}	$\overline{OE}$ Setup Time prior to $\overline{RAS}$	—	—	—	—	ns	4
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	0	—	0	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	10	0	15	ns	5
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	10	—	10	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	10	—	15	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$		10		15	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	2, 3

1. This timing parameter is not applicable to this product, but applies to a related product in this family.
2. Measured with the specified current load and 100pF.
3. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	160	—	180	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	90	—	95	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	45	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	55	—	60	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	10	—	15	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	85	—	90	—	ns	
t_{CPW}	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1

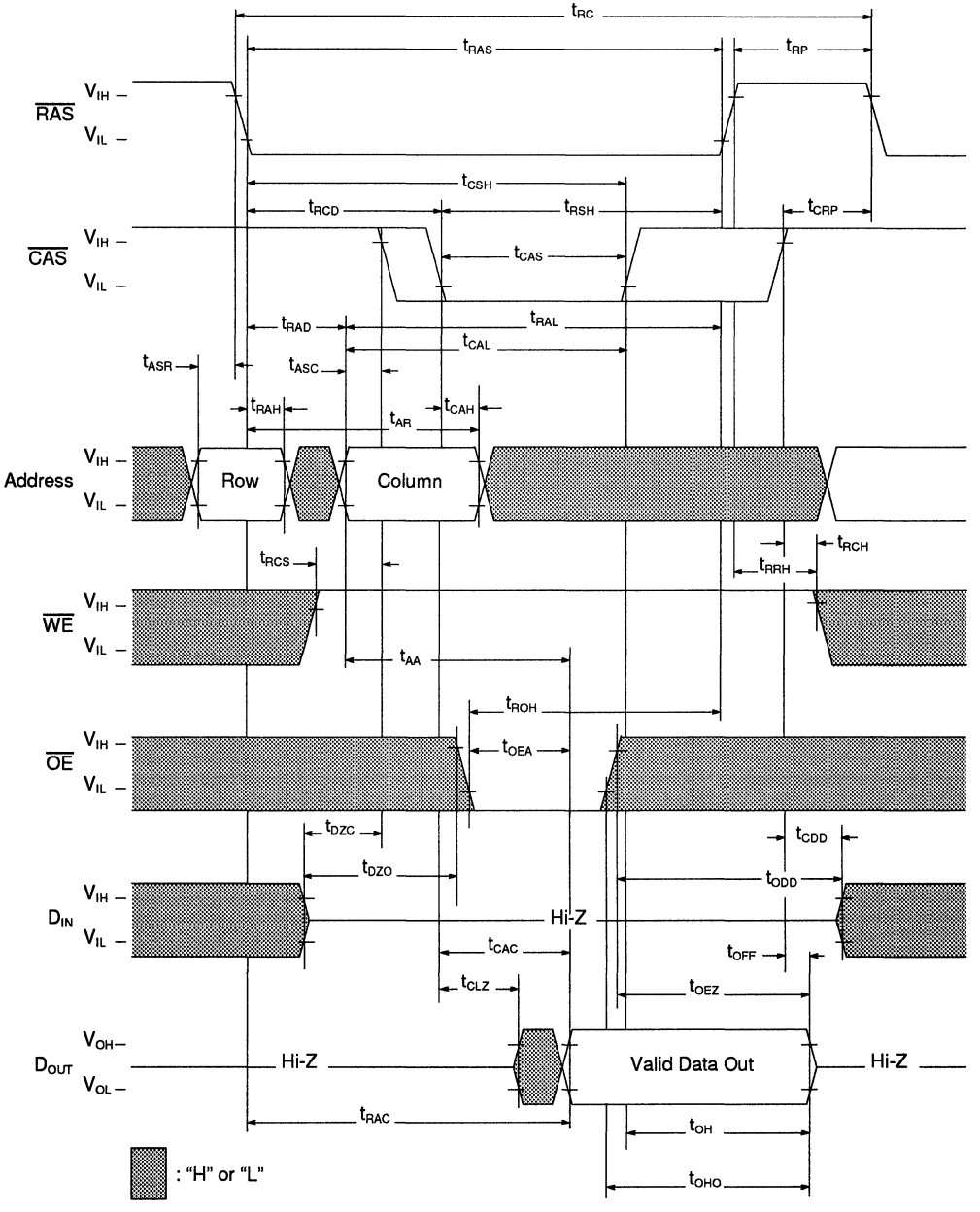
1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Refresh Cycle

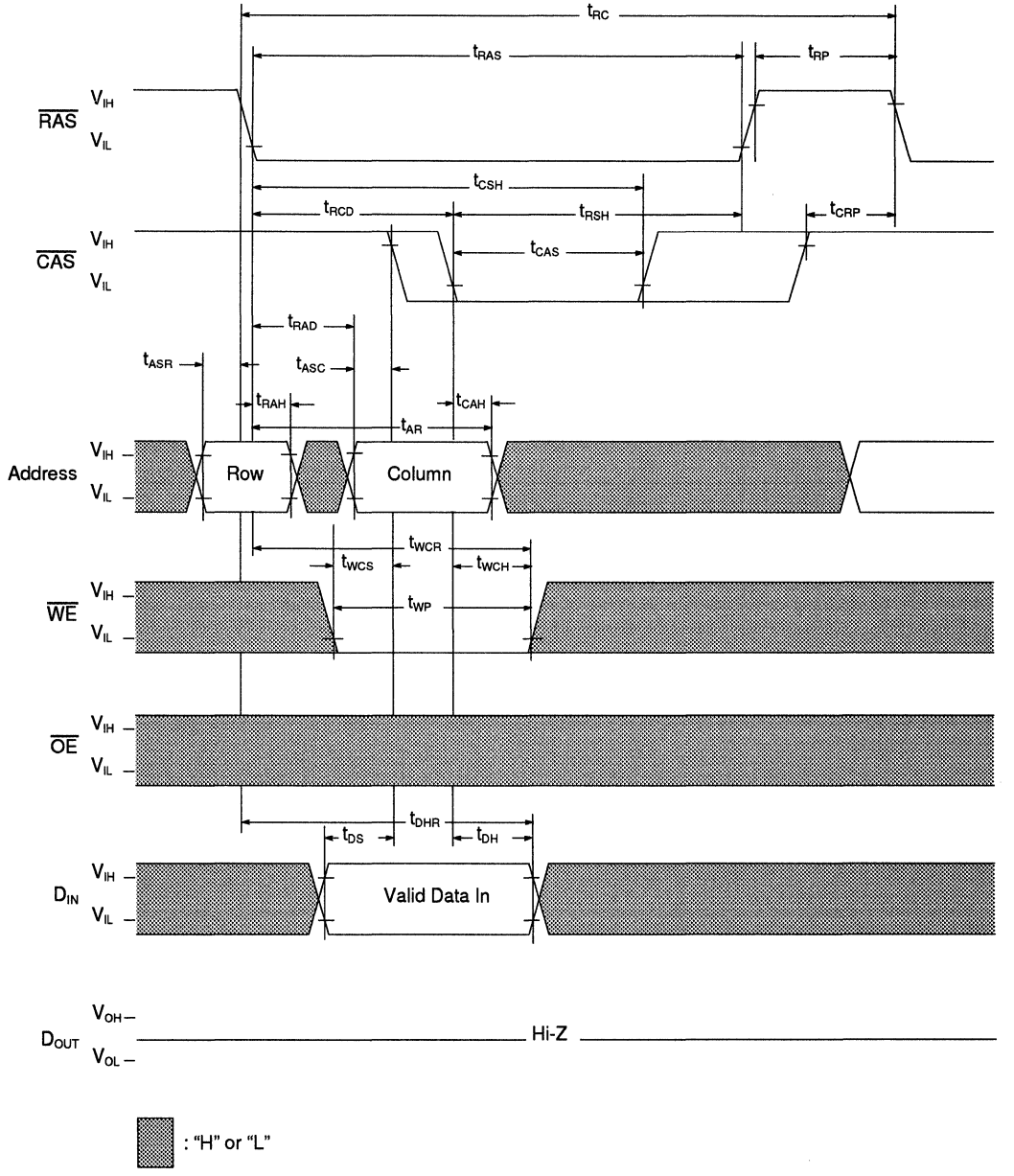
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	15	—	15	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	5	—	5	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 Refreshes are required every 16ms.

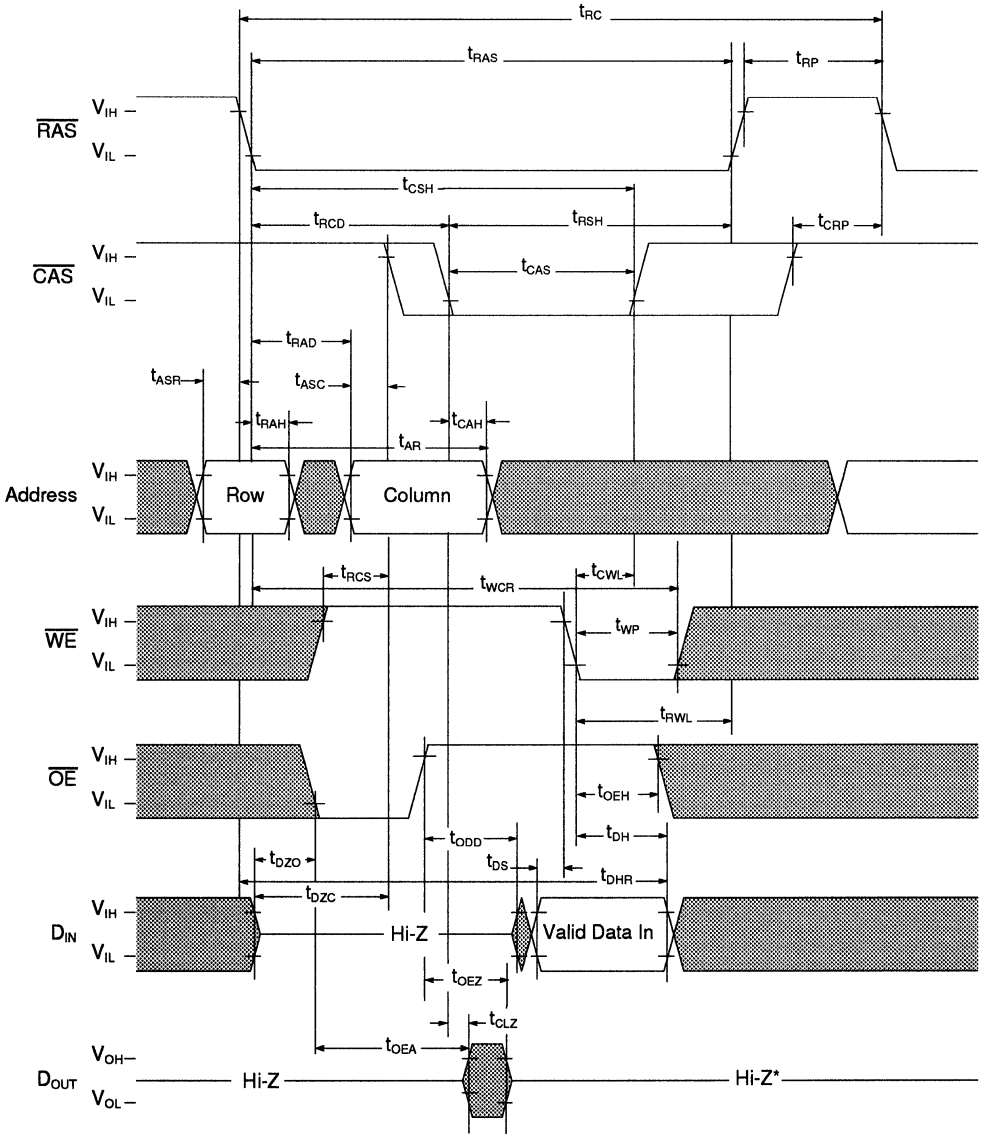
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tCAH
tAR
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tCDD
tDZO
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
VOH
VOL
DOUT
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

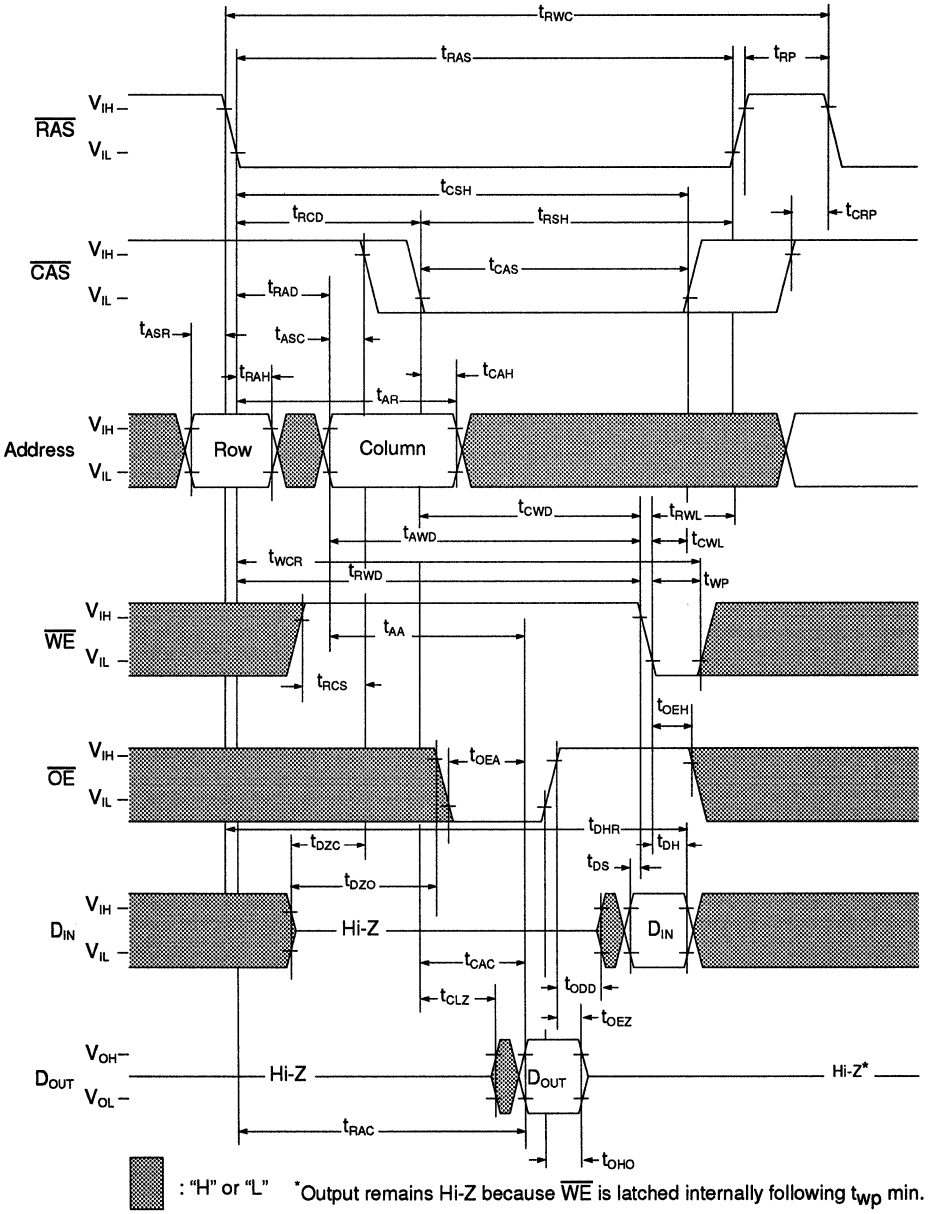


Write Cycle (Late Write)

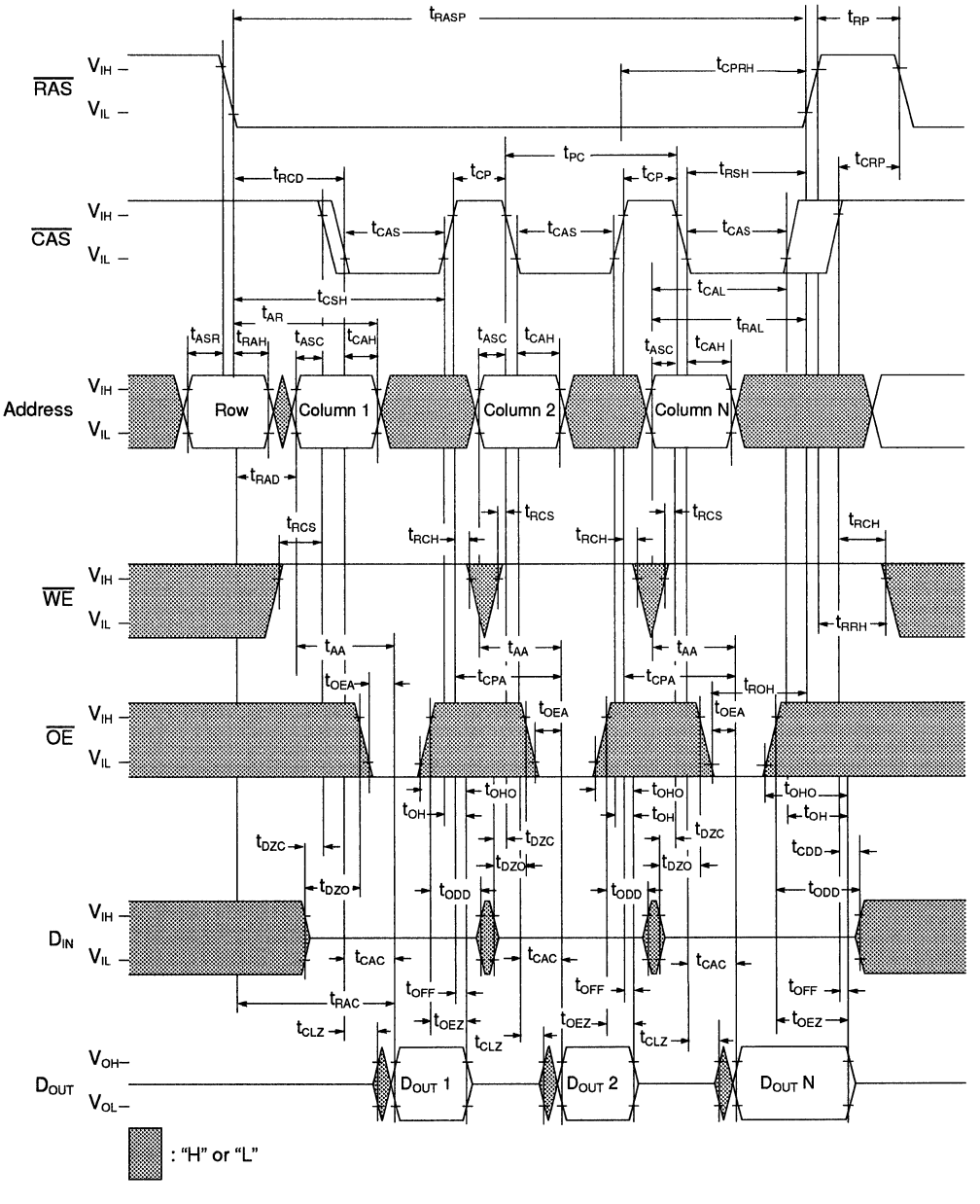


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

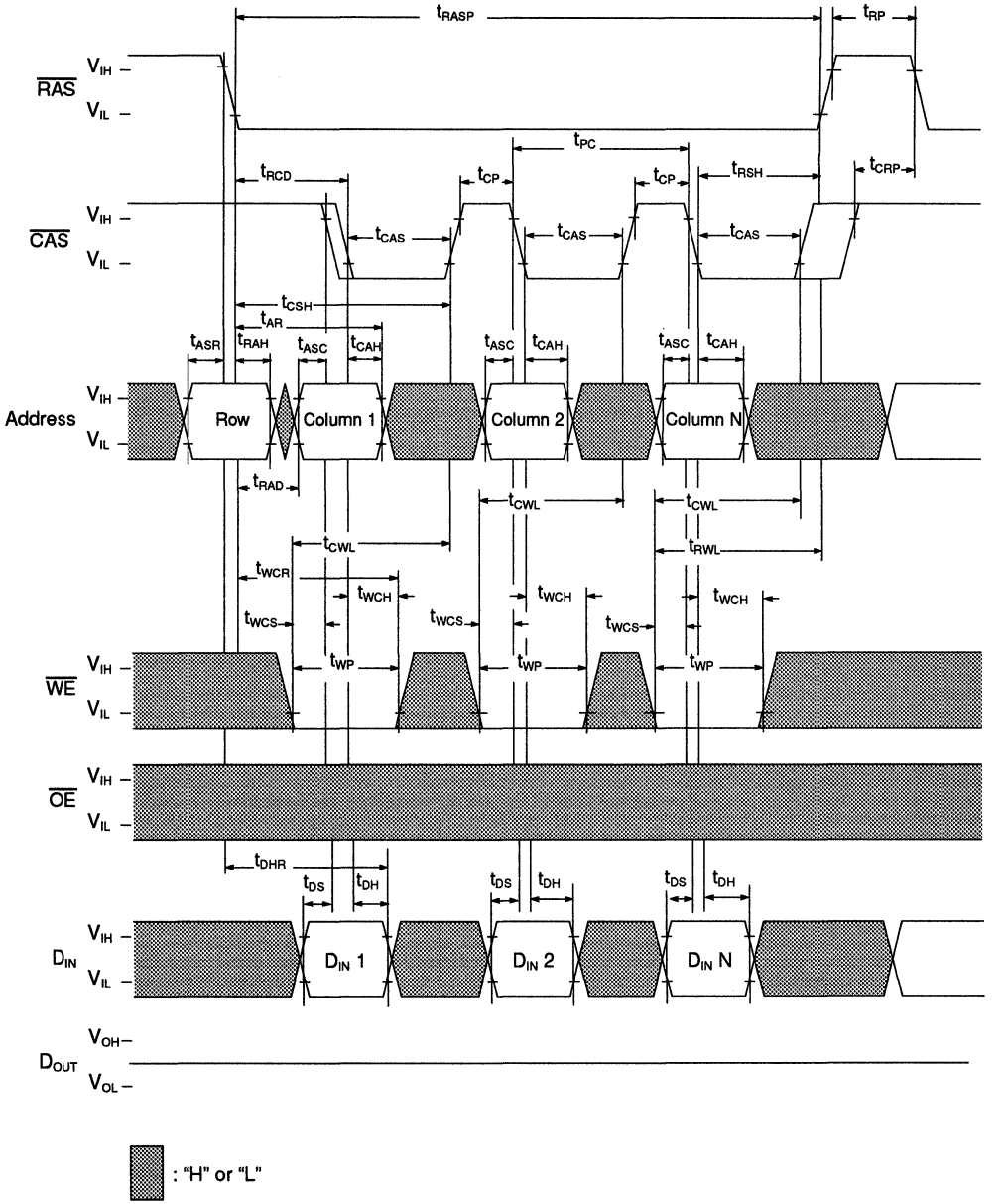
Read-Modify-Write Cycle



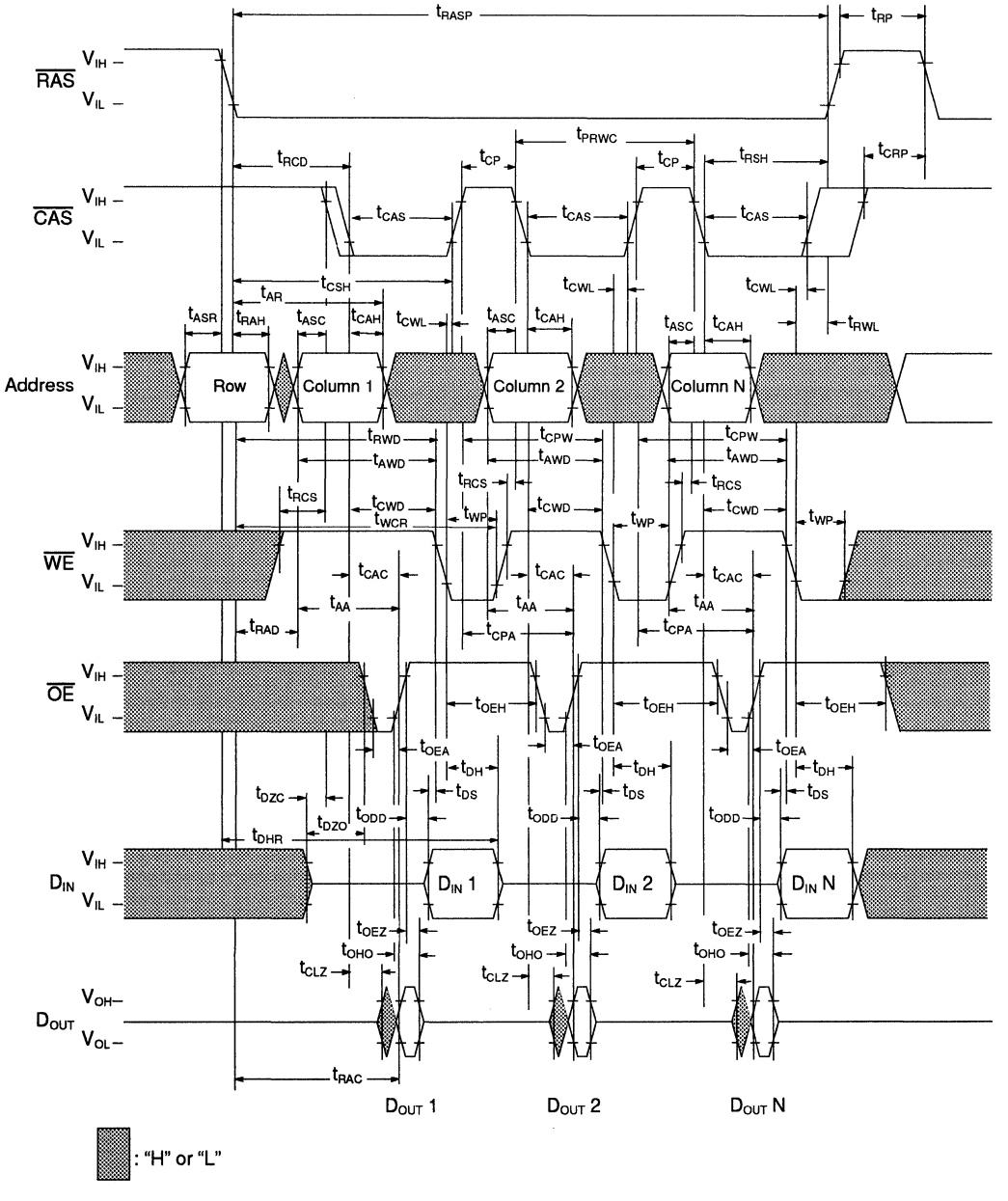
Fast Page Mode Read Cycle



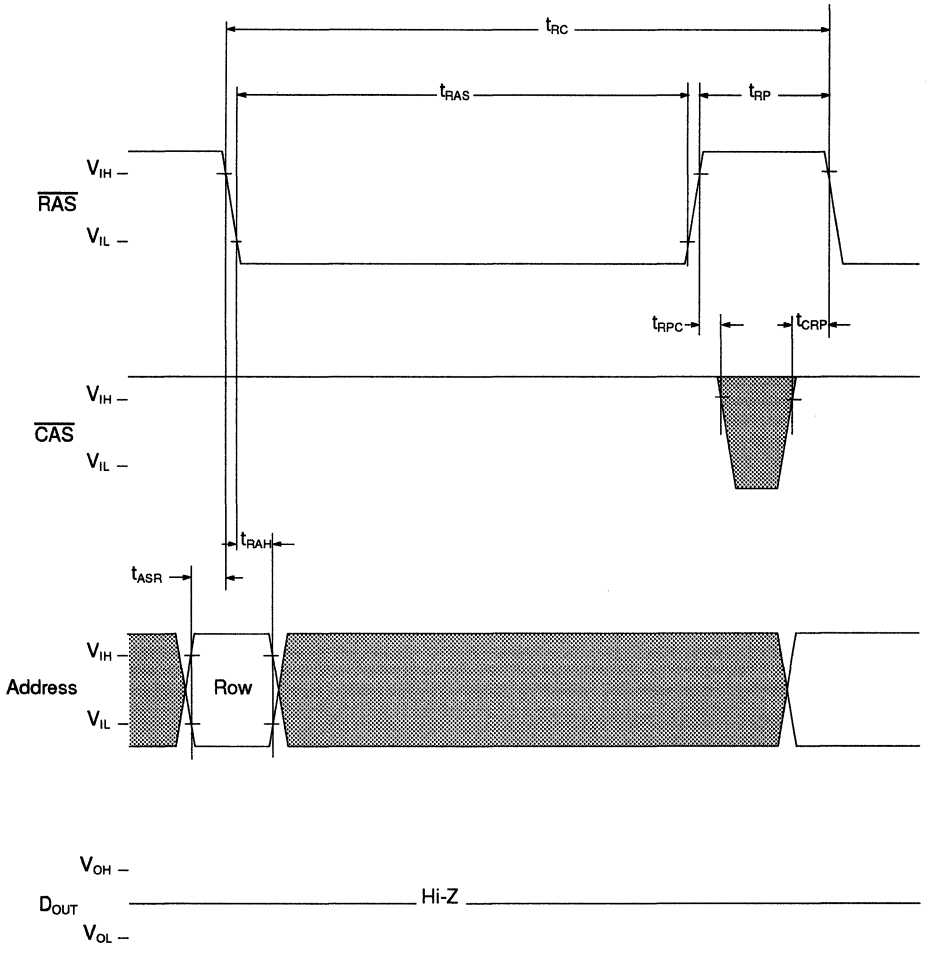
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

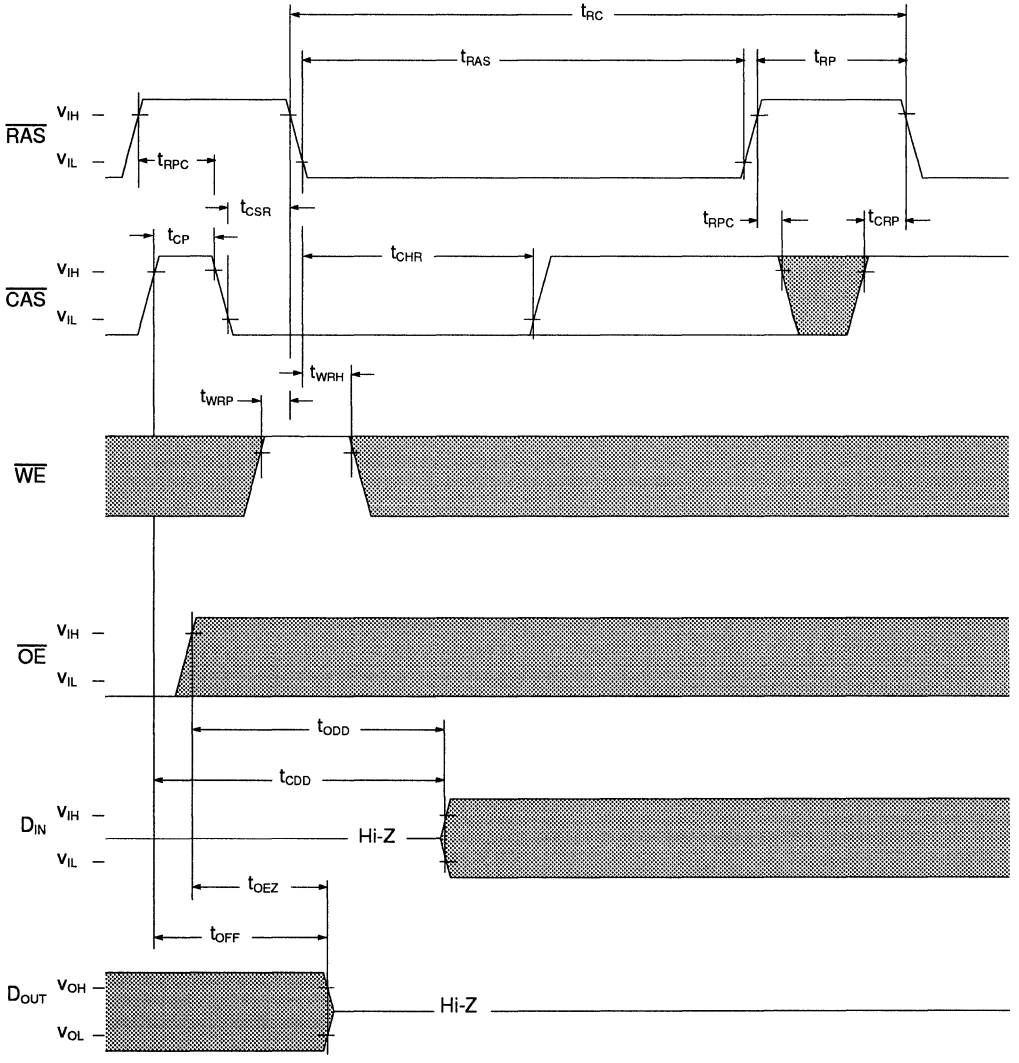


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

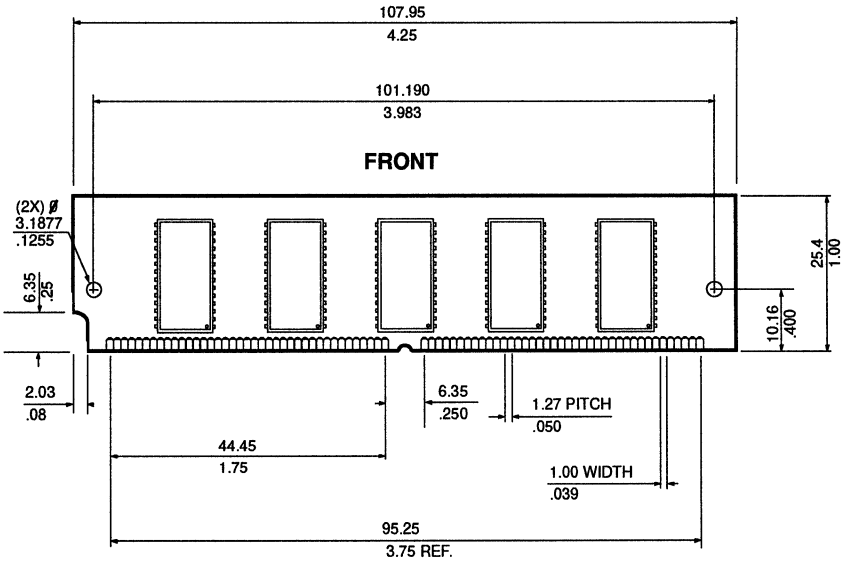
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

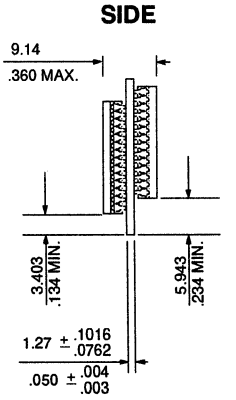


: "H" or "L"

Note: Addresses are "H" or "L"

Layout Drawing (IBM11D1400BA)





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

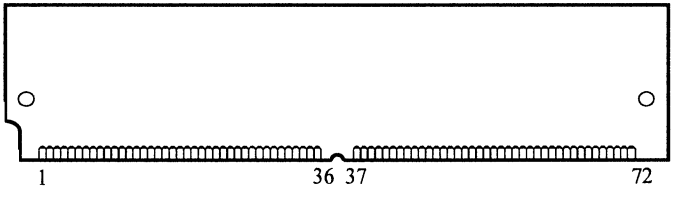
- Optimized for use in ECC applications
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode, Read-Modify-Write cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Au and Sn/Pb versions available

Description

The ECC-Optimized SIMMs, IBM11D2370BA and IBM11D2400BA are 8MB industry standard 72 pin 4-byte single inline memory modules (SIMMs). The Modules are organized as 2M x 36/40 high speed memory arrays, and are configured as 2 1M x 36/40 banks - each independently selectable via unique $\overline{RAS}$ inputs. The 2M x 36 assembly is intended for use in 8 byte applications, typically having 64 data and 8 check bits (64/72 code). The 2M x 40 assembly is applicable to 4 byte applications with 32 data and 7 or 8 check bits (32/39 code), or 8 byte applications with extended error correction capabilities. The modules are manufactured with 18 or 20 1M x 4 devices, each in a 350 mil package, and are compatible with the JEDEC 72-pin SIMM standard.

The IBM 72-pin SIMMs provide a high-performance, flexible 4-byte interface in a 4.25" long footprint. Related products include other density offerings and parity SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS1}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS1}$	Column Address Strobe
$\overline{WE}$	Read/write Input
$\overline{OE}$	Output Enable
A0 - A9	Address Inputs
DQ0-35 or DQ0-39	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
$\overline{ECC}$, PD1 - PD4	Presence Detects

Pinout

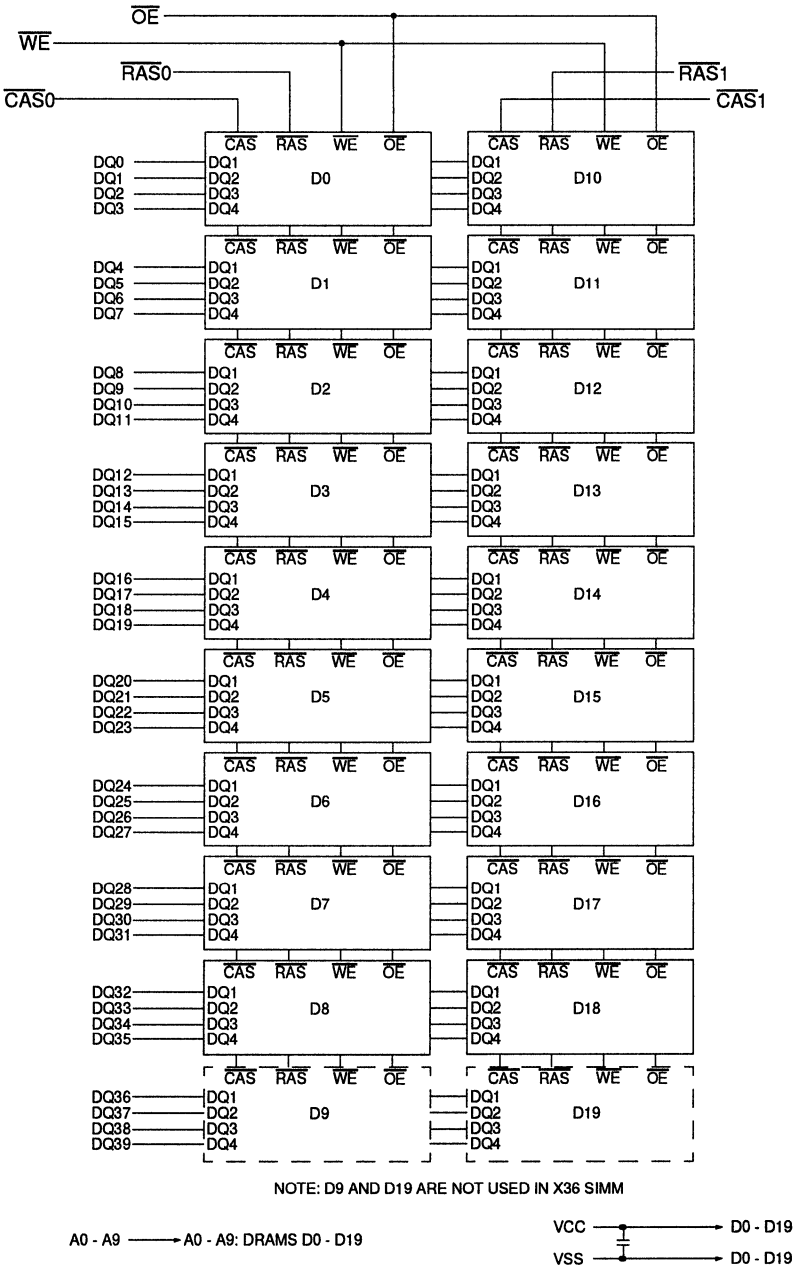
Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	NC	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{OE}$	31	A8	43	$\overline{CAS1}$	55	DQ28	67	PD1
8	DQ6	20	DQ8	32	A9	44	$\overline{RAS0}$	56	DQ29	68	PD2
9	DQ7	21	DQ9	33	NC	45	$\overline{RAS1}$	57	DQ30	69	PD3
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD4
11	NC	23	DQ11	35	DQ17	47	$\overline{WE}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	$\overline{ECC}$	60	DQ32	72	V_{SS}

1. DQ36 - DQ39 are NC for x36 SIMM.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D2370BA-60	2M x 36	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D2370BA-70	2M x 36	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E2370BA-60	2M x 36	60ns	Au	4.25" x 1" x .360"	
IBM11E2370BA-70	2M x 36	70ns	Au	4.25" x 1" x .360"	
IBM11D2400BA-60	2M x 40	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D2400BA-70	2M x 40	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E2400BA-60	2M x 40	60ns	Au	4.25" x 1" x .360"	
IBM11E2400BA-70	2M x 40	70ns	Au	4.25" x 1" x .360"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Col Address	All DQ Bits
Standby	H	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	Valid Data Out
Early-Write	L	L	L	X	Row	Col	Valid Data In
Late-Write / RMW	L	L	H→L	L→H	Row	Col	Valid Data Out, Valid Data In
Fast Page Mode-Read 1st cycle	L	H→L	H	L	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	Valid Data Out
Fast Page Mode-Write 1st cycle	L	H→L	L	X	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	Valid Data In
Fast Page Mode Read-Modify-Write: 1st cycle	L	H→L	H→L	L→H	Row	Col	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	L→H	N/A	Col	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	High Impedance

Presence Detect

Pin	-60	-70
$\overline{ECC}$ (ECC Optimized SIMM)	V_{SS}	V_{SS}
PD1	NC	NC
PD2	NC	NC
PD3	NC	V_{SS}
PD4	NC	NC

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +6.5	V	1
V_{IN}	Input Voltage	-0.7 to V_{CC} + 0.7	V	1
V_{OUT}	Output Voltage	-0.7 to V_{CC} + 0.7	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	13.2	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	x36 Max	x40 Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	100	104	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	66	70	pF	
C_{I3}	Input Capacitance ($\overline{WE}$)	112	116	pF	
C_{I4}	Input Capacitance ($\overline{OE}$)	112	116	pF	
$C_{I/O}$	Output Capacitance (All DQ bits)	25	25	pF	

2M x 36 DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1098	mA	1, 2, 3
		-70	—	990		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	36	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1098	mA	1, 3, 4
		-70	—	990		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	693	mA	1, 2, 3
		-70	—	648		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	36	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1098	mA	1, 3, 4
		-70	—	990		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{OE}$, $\overline{WE}$, ADDRESS	-180	+180	µA	
		$\overline{RAS}$, $\overline{CAS}$	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for 1 bank..

2M x 40 DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1220	mA	1, 2, 3
		-70	—	1100		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	40	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1220	mA	1, 3, 4
		-70	—	1100		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	770	mA	1, 2, 3
		-70	—	720		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	40	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1220	mA	1, 3, 4
		-70	—	1100		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{OE}$, $\overline{WE}$, ADDRESS	-200	+200	µA	
		$\overline{RAS}$, $\overline{CAS}$	-100	+100		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for 1 bank..

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	10	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	—	—	—	—	ns	3
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	—	—	—	—	ns	3
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	—	—	—	—	ns	3
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	45	—	50	—	—	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	1
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	3
t_{DH}	D_{IN} Hold Time	10	—	15	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	15	—	20	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OES}	$\overline{OE}$ Setup Time prior to $\overline{RAS}$	—	—	—	—	ns	4
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	0	—	0	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	10	0	15	ns	5
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	10	—	10	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	10	—	15	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$		10		15	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	2, 3

1. This timing parameter is not applicable to this product, but applies to a related product in this family.
2. Measured with the specified current load and 100pF.
3. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	160	—	180	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	90	—	95	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	45	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	55	—	60	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	10	—	15	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	85	—	90	—	ns	
t_{CPW}	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1

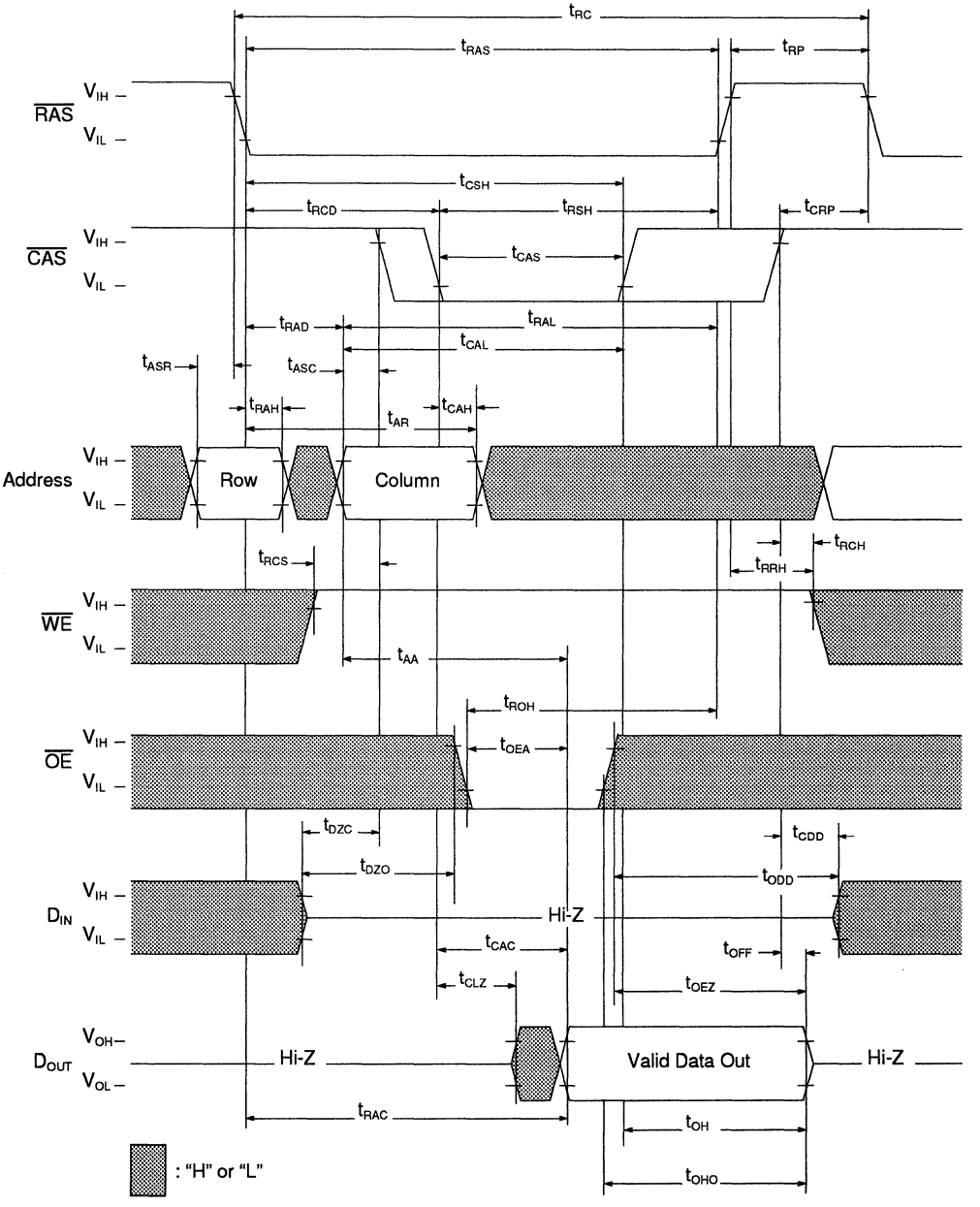
1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Refresh Cycle

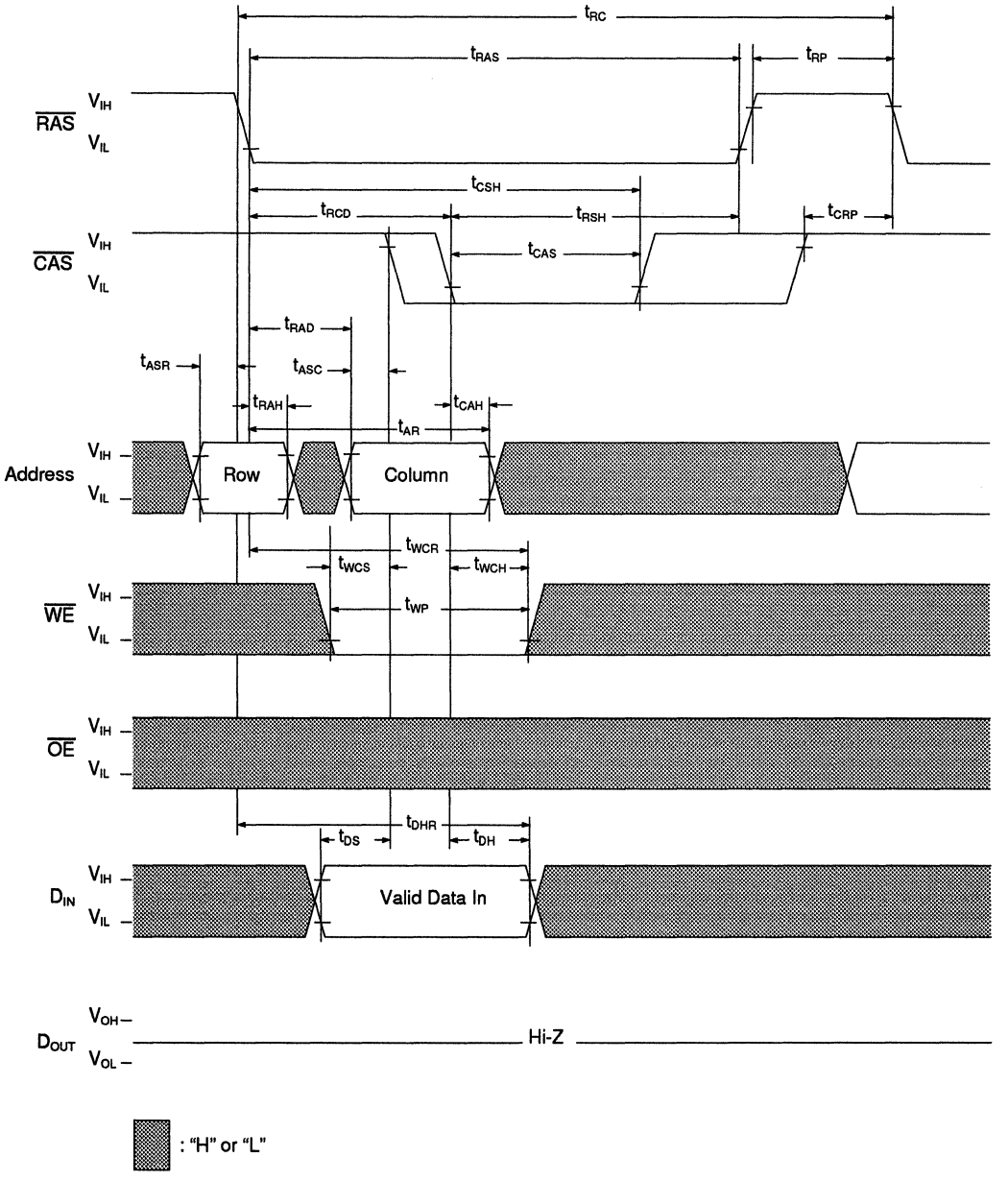
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	15	—	15	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	5	—	5	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 Refreshes are required every 16ms.

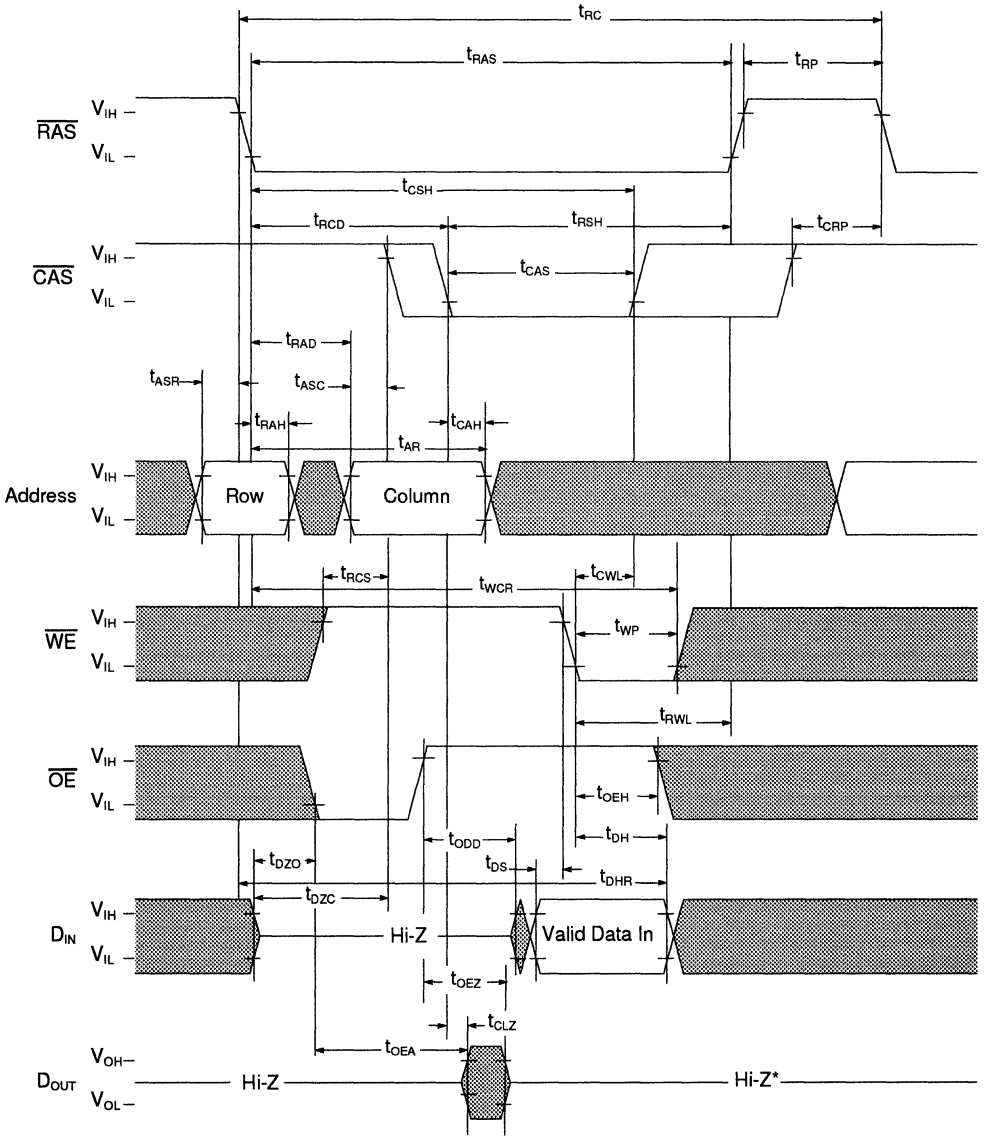
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tCAH
tAR
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tCDD
tDZO
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

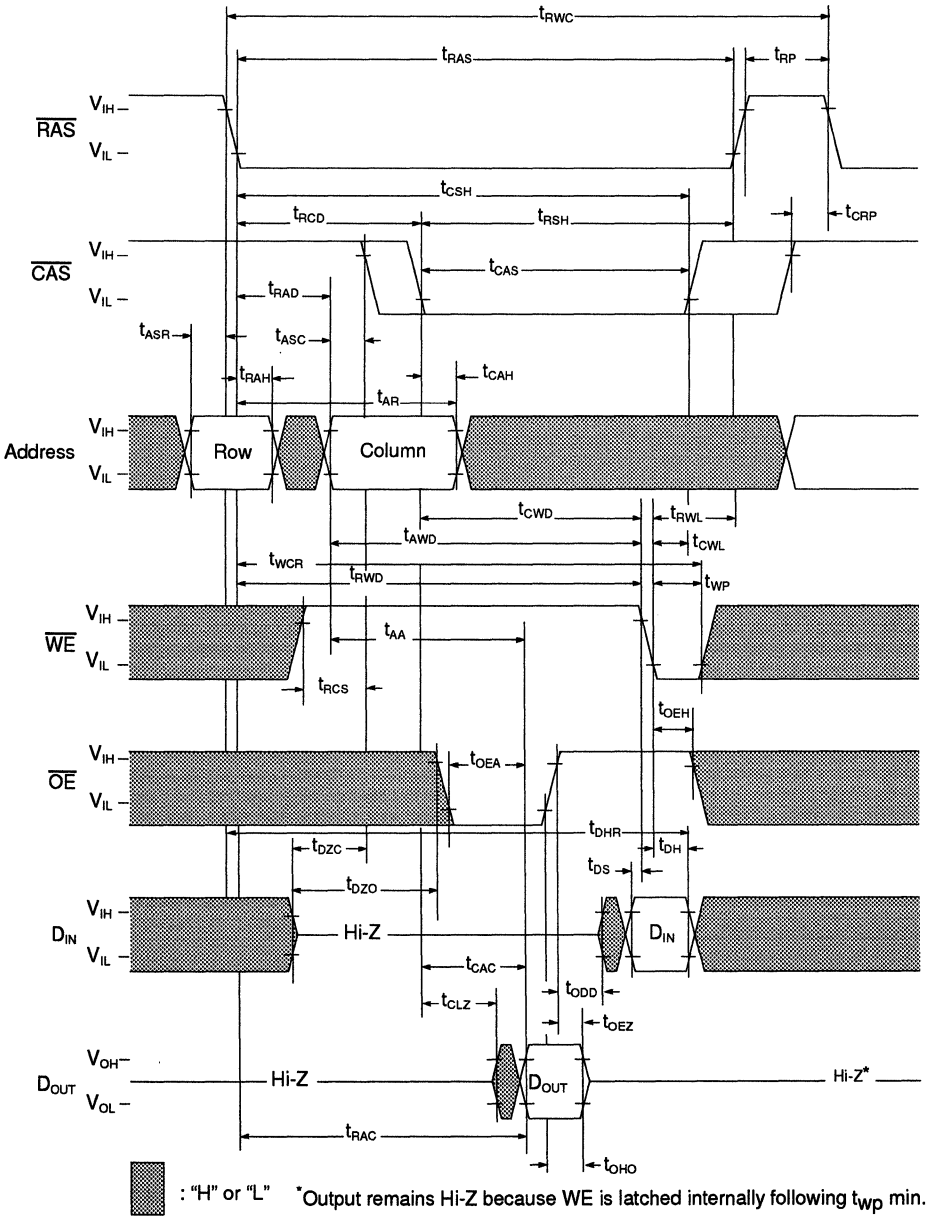


Write Cycle (Late Write)

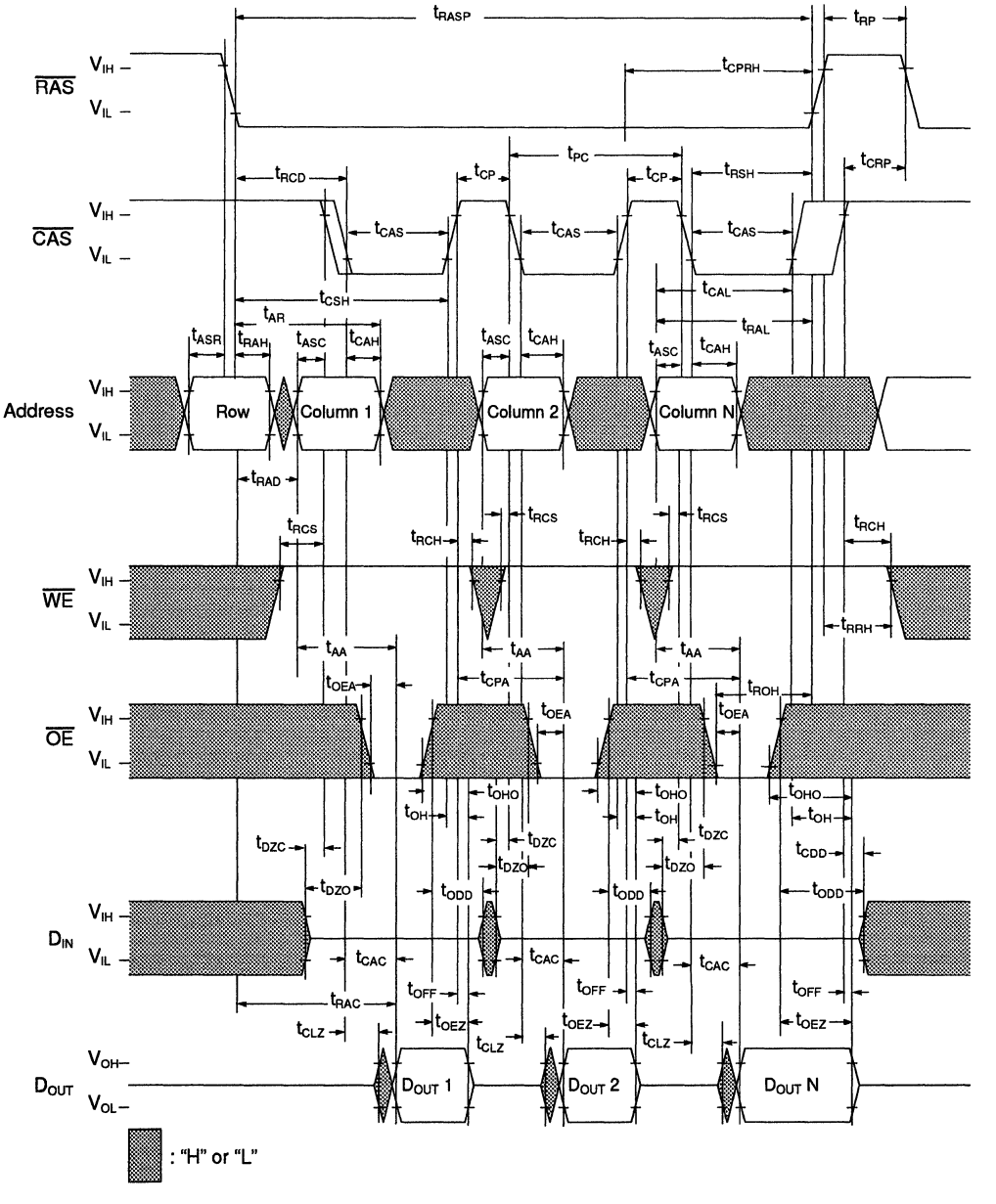


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

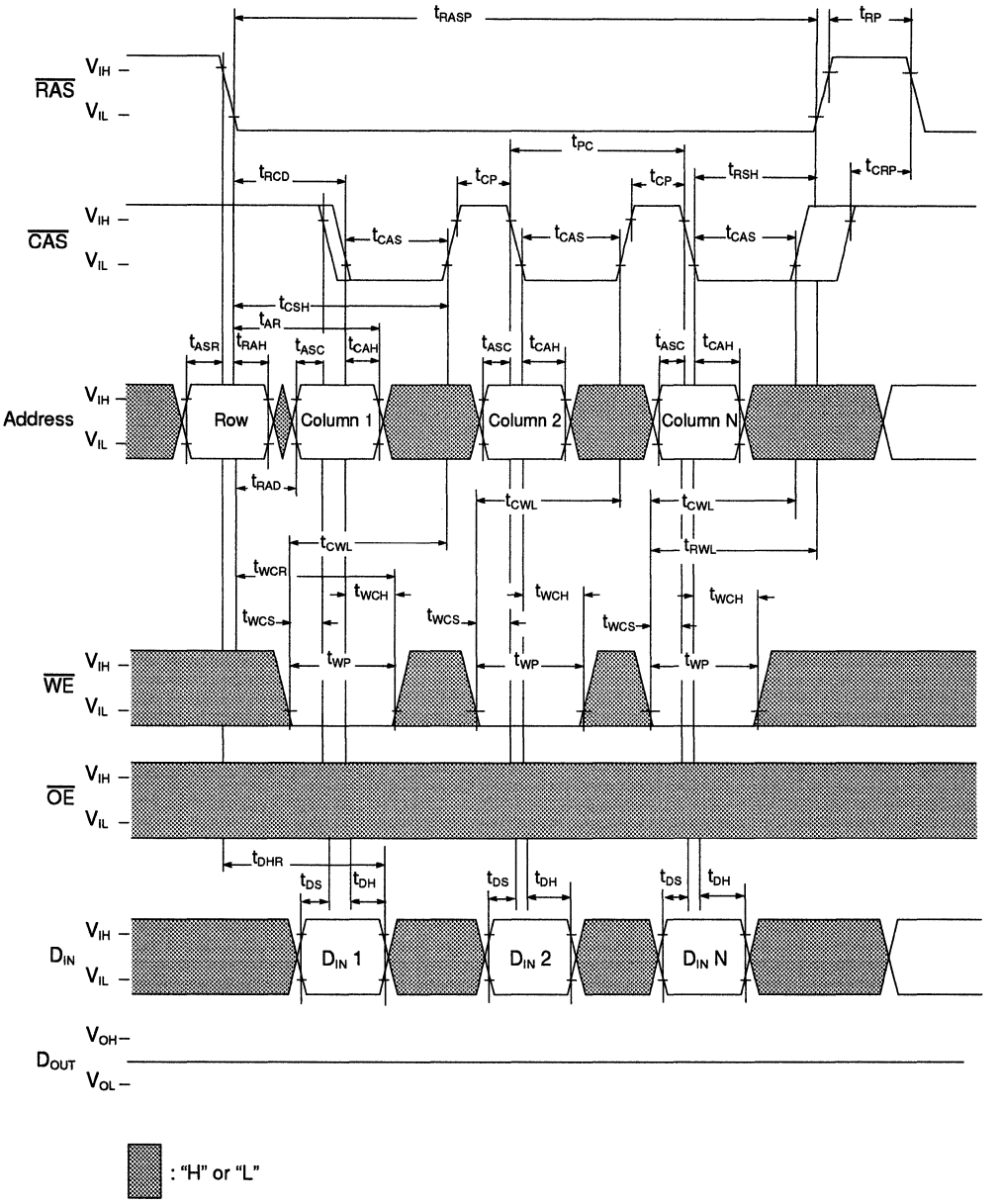
Read-Modify-Write Cycle



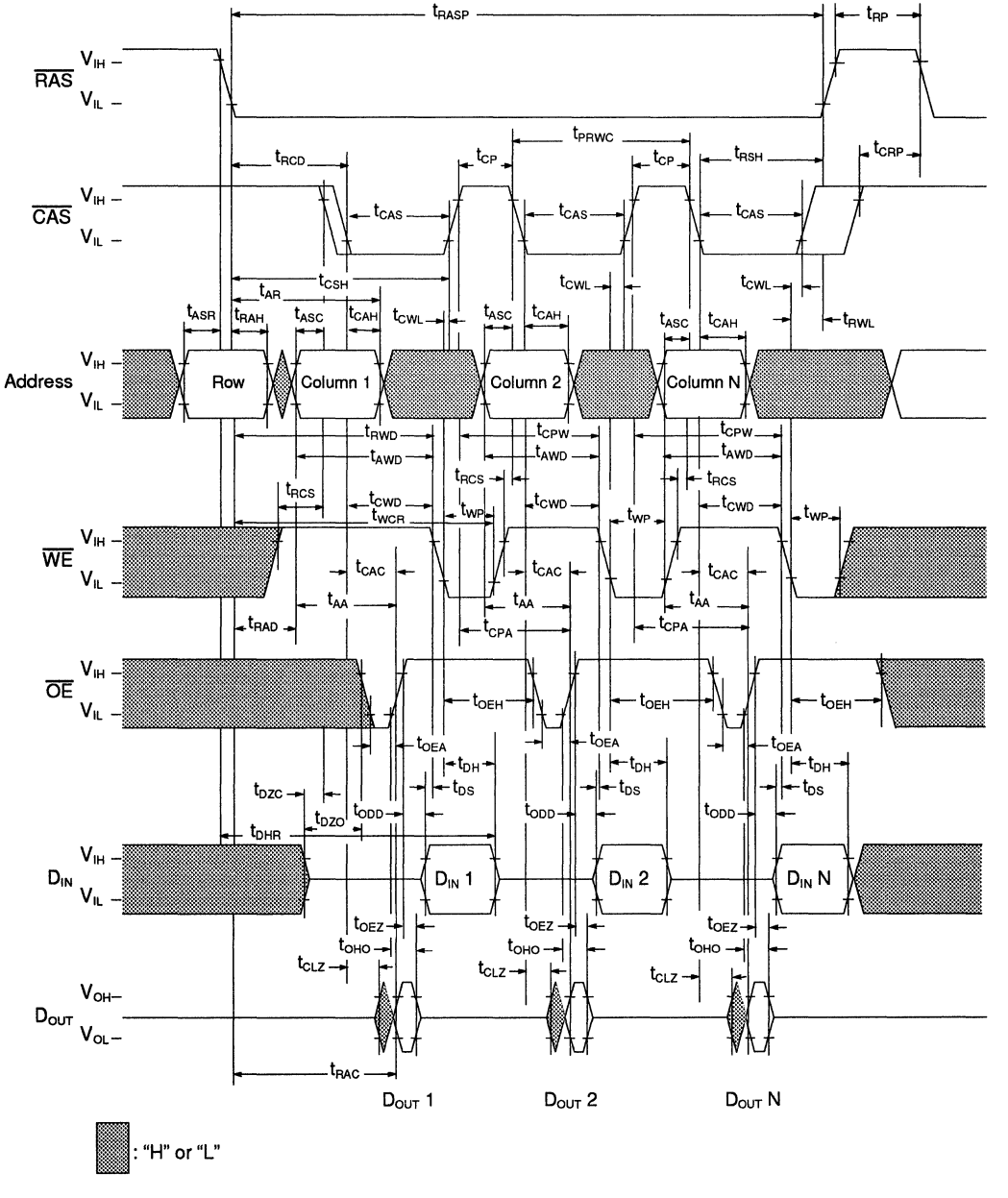
Fast Page Mode Read Cycle



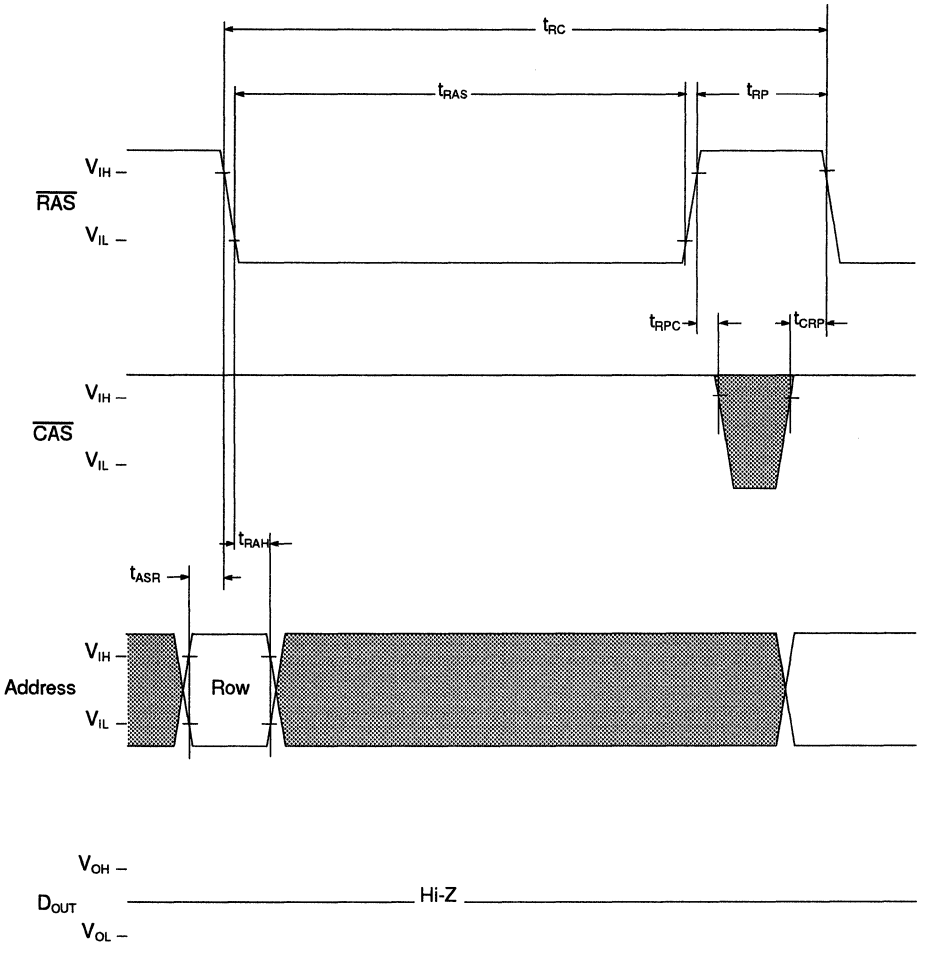
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle



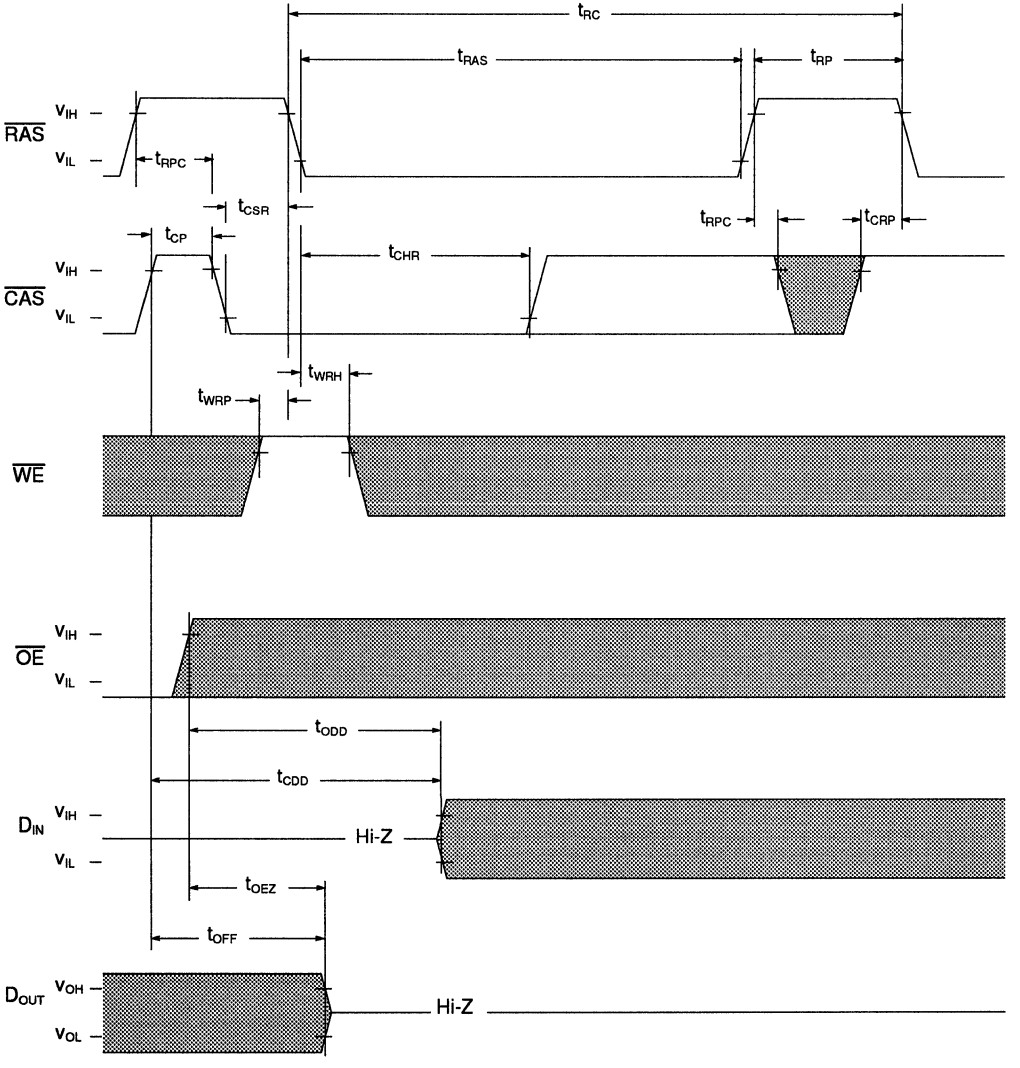
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

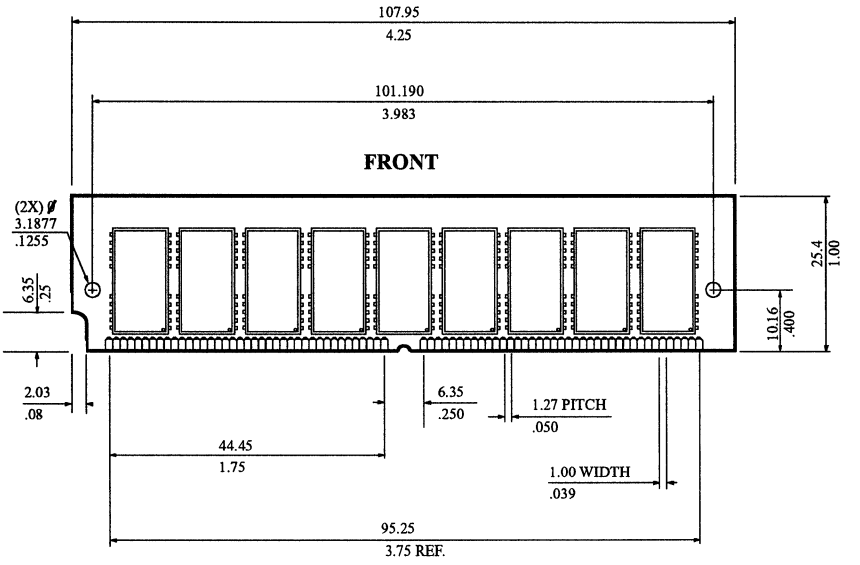
Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

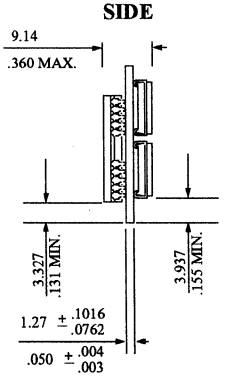
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing (IBM11D2400BA)





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

4M x 36/4M x 40 DRAM Modules

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

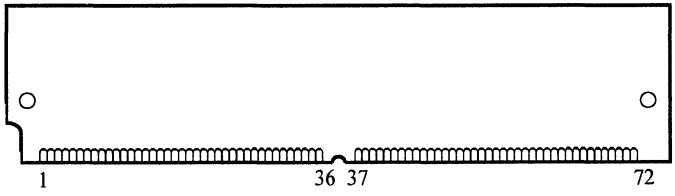
- Optimized for use in ECC applications
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode, Read-Modify-Write cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Au and Sn/Pb versions available

Description

The ECC-Optimized SIMMs, IBM11D4370C and IBM11D4400C are 16MB industry standard 72 pin 4-byte single inline memory modules (SIMMs). The Modules are organized as 4M x 36/40 high speed memory arrays, and are configured as a single 4M x 36/40 bank. The 4M x 36 assembly is intended for use in 8 byte applications, typically having 64 data and 8 check bits (64/72 code). The 4M x 40 assembly is applicable to 4 byte applications with 32 data and 7 or 8 check bits (32/39 code), or 8 byte applications with extended error correction capabilities. The modules are manufactured with 9 or 10 4M x 4 devices, each in a 400 mil package, and are compatible with the JEDEC 72-pin SIMM standard.

The IBM 72-pin SIMMs provide a high-performance, flexible 4-byte interface in a 4.25" long footprint. Related products include other density offerings and parity SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$	Row Address Strobe
$\overline{CAS0}$	Column Address Strobe
$\overline{WE}$	Read/write Input
$\overline{OE}$	Output Enable
A0 - A11	Address Inputs
DQ0-35 or DQ0-39	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
$\overline{ECC}$, PD1 - PD5	Presence Detects

Pinout

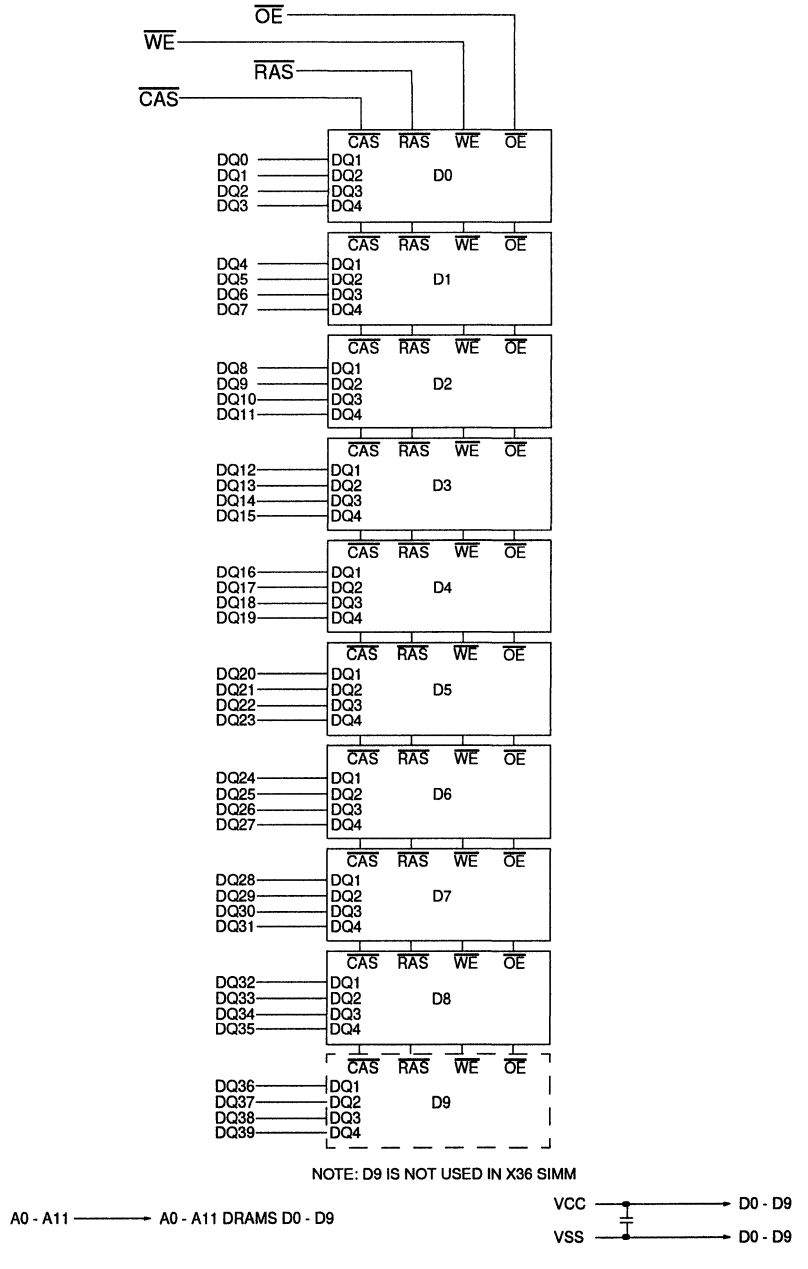
Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	A10	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	A11	54	DQ27	66	DQ38
7	DQ5	19	$\overline{OE}$	31	A8	43	NC	55	DQ28	67	PD1
8	DQ6	20	DQ8	32	A9	44	$\overline{RAS0}$	56	DQ29	68	PD2
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ30	69	PD3
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD4
11	PD5	23	DQ11	35	DQ17	47	$\overline{WE}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	$\overline{ECC}$	60	DQ32	72	V_{SS}

1. DQ36 - DQ39 are NC for x36 SIMM.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D4370CA-60	4M x 36	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D4370CA-70	4M x 36	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E4370CA-60	4M x 36	60ns	Au	4.25" x 1" x .360"	
IBM11E4370CA-70	4M x 36	70ns	Au	4.25" x 1" x .360"	
IBM11D4400CA-60	4M x 40	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D4400CA-70	4M x 40	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E4400CA-60	4M x 40	60ns	Au	4.25" x 1" x .360"	
IBM11E4400CA-70	4M x 40	70ns	Au	4.25" x 1" x .360"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Col Address	All DQ Bits
Standby	H	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	Valid Data Out
Early-Write	L	L	L	X	Row	Col	Valid Data In
Late-Write / RMW	L	L	H→L	L→H	Row	Col	Valid Data Out, Valid Data In
Fast Page Mode-Read 1st cycle	L	H→L	H	L	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	Valid Data Out
Fast Page Mode-Write 1st cycle	L	H→L	L	X	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	Valid Data In
Fast Page Mode Read-Modify-Write: 1st cycle	L	H→L	H→L	L→H	Row	Col	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	L→H	N/A	Col	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	High Impedance

Presence Detect

Pin	-60	-70
$\overline{ECC}$ (ECC Optimized SIMM)	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}
PD2	NC	NC
PD3	NC	V_{SS}
PD4	NC	NC
PD5	V_{SS}	V_{SS}

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min(V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min(V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	4.7	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 2.0V for pulse widths ≤ 4.0ns (or V_{CC} + 1.0V for ≤ 8.0ns) and V_{IL} may undershoot to -2.0V for pulse widths ≤ 4.0ns (or -1.0V for ≤ 8.0ns). Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	x36 Max	x40 Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	65	70	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	55	60	pF	
C_{I3}	Input Capacitance ($\overline{WE}$)	60	65	pF	
C_{I4}	Input Capacitance ($\overline{OE}$)	65	70	pF	
$C_{I/O}$	Output Capacitance (All DQ bits)	15	15	pF	

4M x 36 DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	765	mA	1, 2, 3
		-70	—	675		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	18	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	765	mA	1, 3
		-70	—	675		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	675	mA	1, 2, 3
		-70	—	585		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	9	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	765	mA	1, 3
		-70	—	675		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{OE}$, $\overline{WE}$, ADDRESS	-90	+90	µA	
		$\overline{RAS}$, $\overline{CAS}$	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}

4M x 40 DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	850	mA	1, 2, 3
		-70	—	750		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	20	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	850	mA	1, 3
		-70	—	750		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	750	mA	1, 2, 3
		-70	—	650		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	10	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	850	mA	1, 3
		-70	—	750		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{OE}$, $\overline{WE}$, ADDRESS	-100	+100	µA	
		$\overline{RAS}$, $\overline{CAS}$	-100	+100		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	15	—	20	—	ns	3
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	—	0	—	ns	4
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	4
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	—	5
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. Either t_{CDD} or t_{ODD} must be satisfied.
4. Either t_{DCZ} or t_{DZO} must be satisfied.
5. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	1
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	3
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	15	—	20	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OES}	$\overline{OE}$ Setup Time prior to $\overline{RAS}$	—	—	—	—	ns	4
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	3	—	3	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	6
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	—	—	—	—	ns	4
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	6
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	0	15	0	20	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	150	—	180	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80	—	95	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	35	—	45	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	50	—	60	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	80	—	95	—	ns	
t_{CPW}	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	55	—	65	—	ns	1

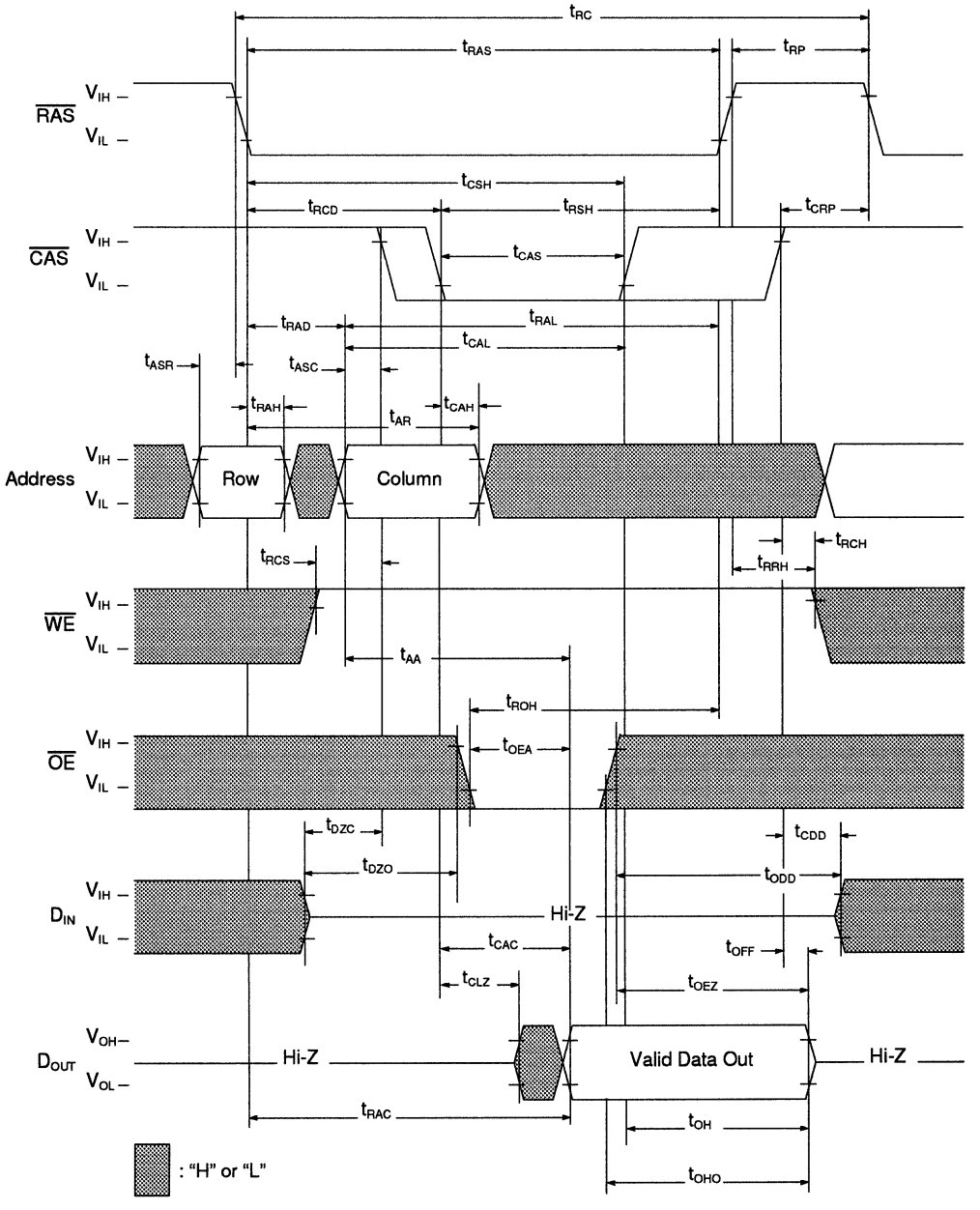
1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Refresh Cycle

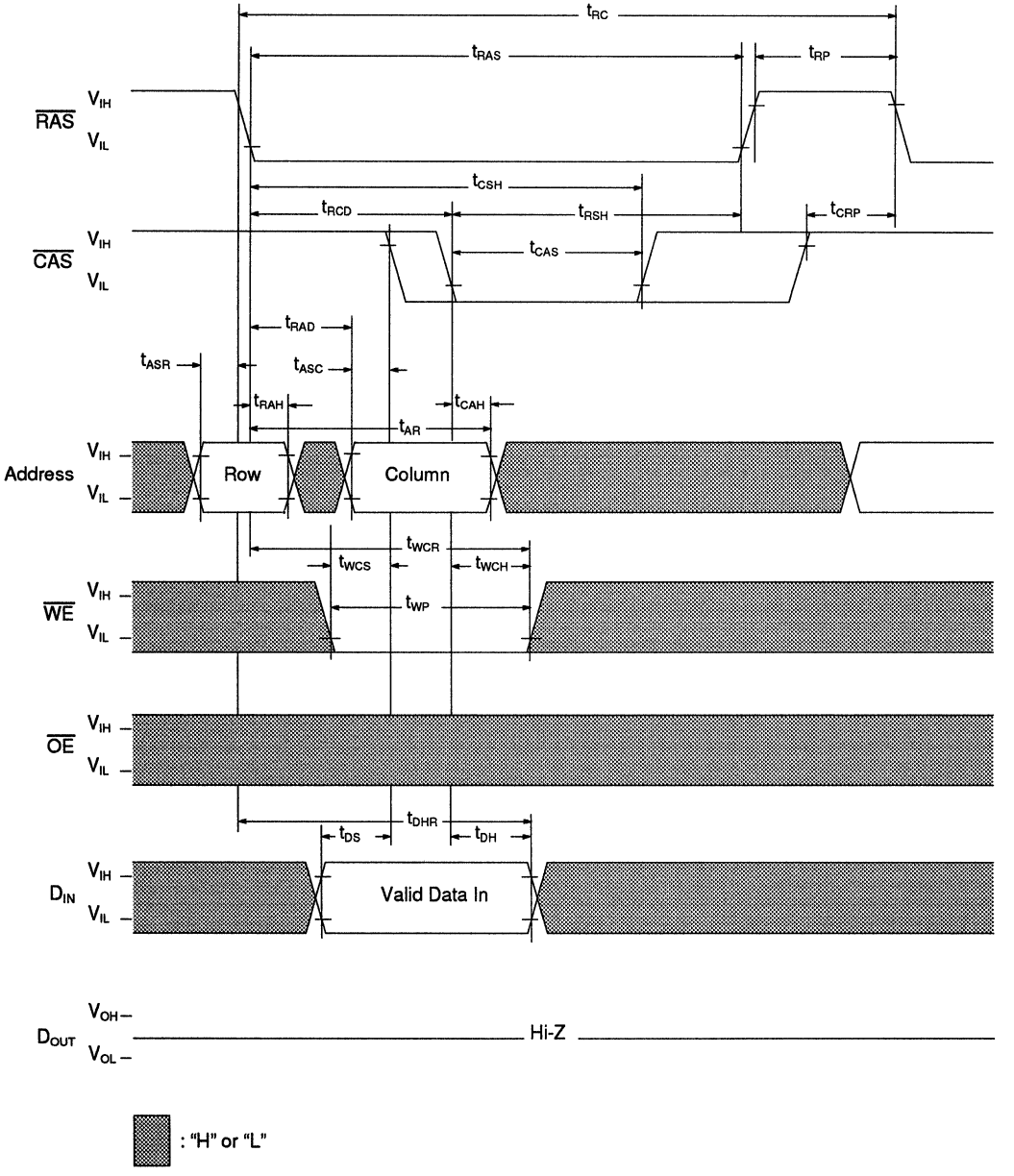
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	64	—	64	ms	1

1. 4096 Refreshes are required every 64ms.

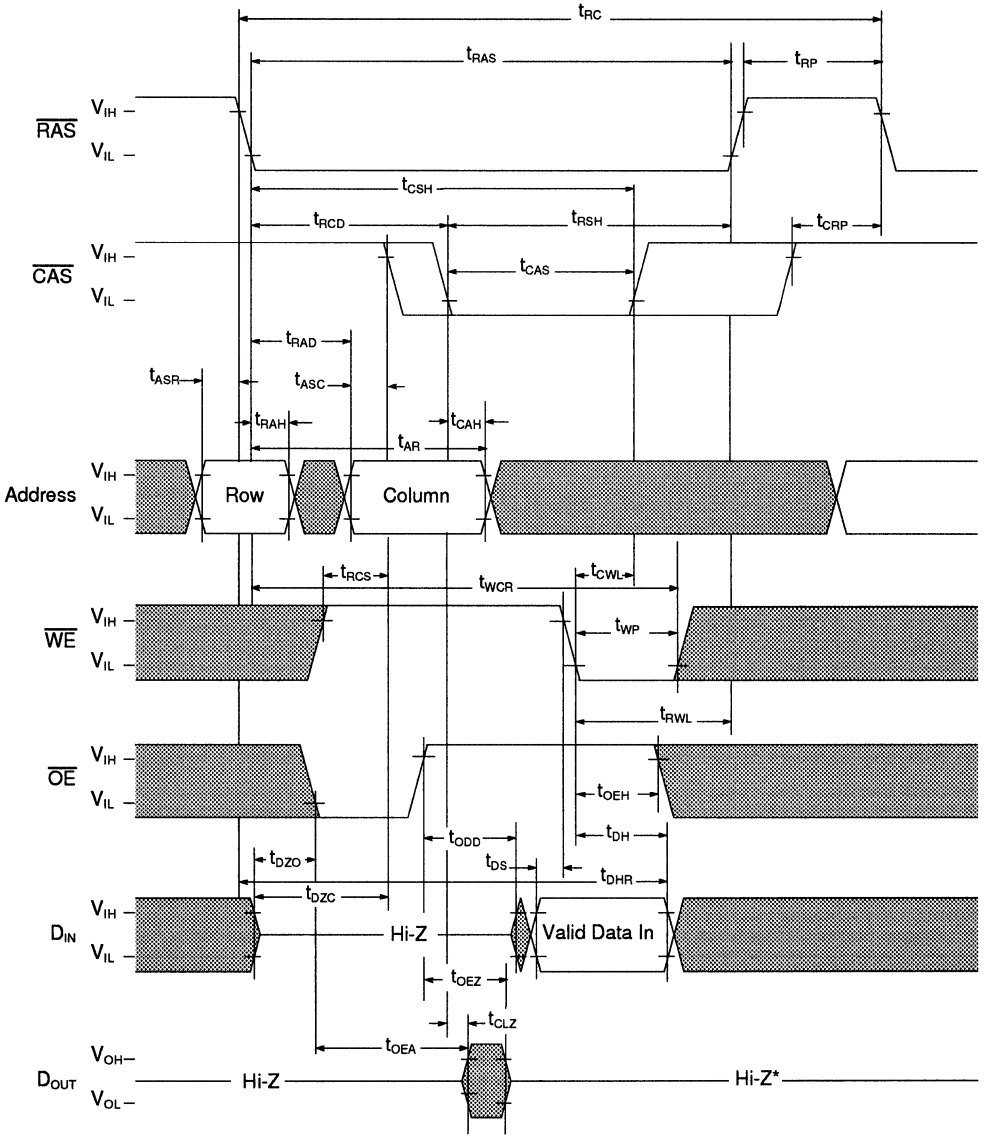
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tAR
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Valid Data Out
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

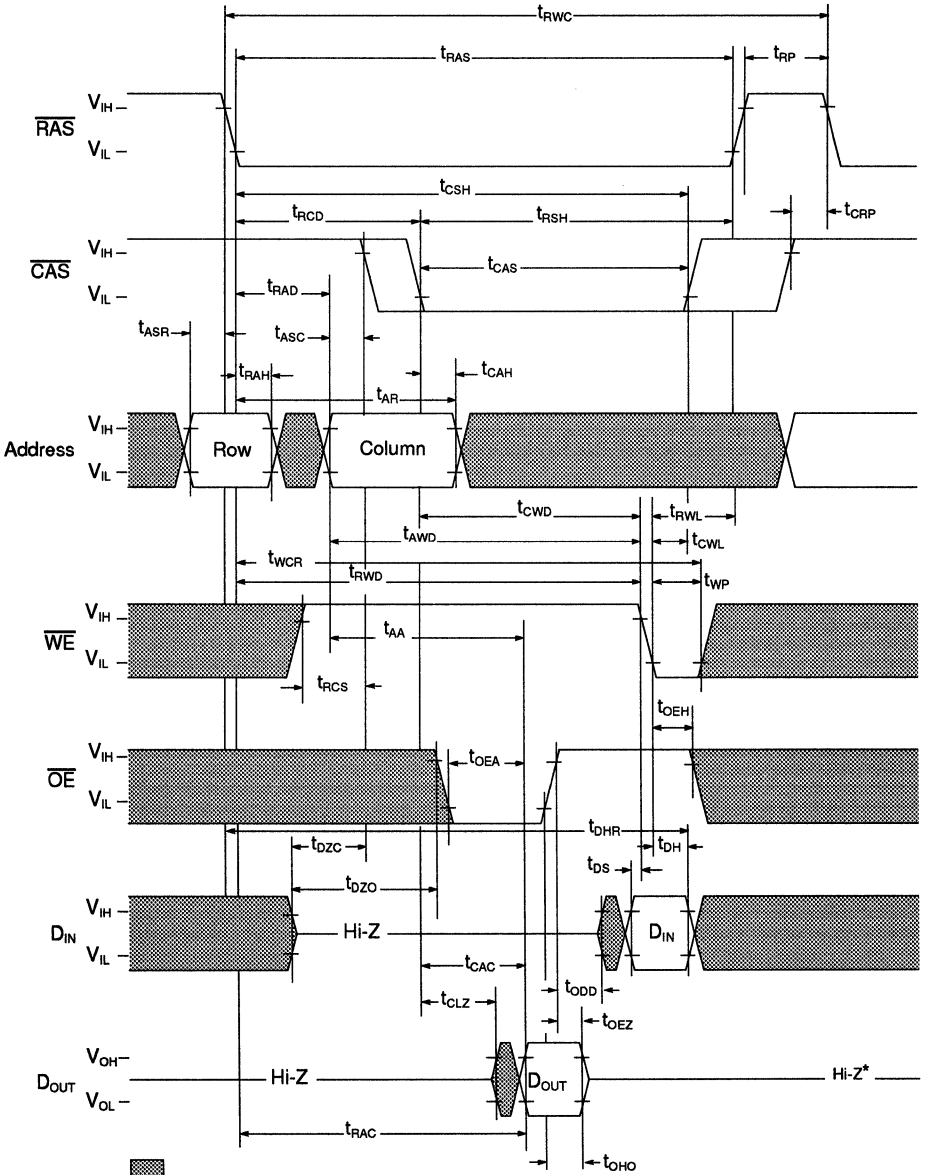


Write Cycle (Late Write)

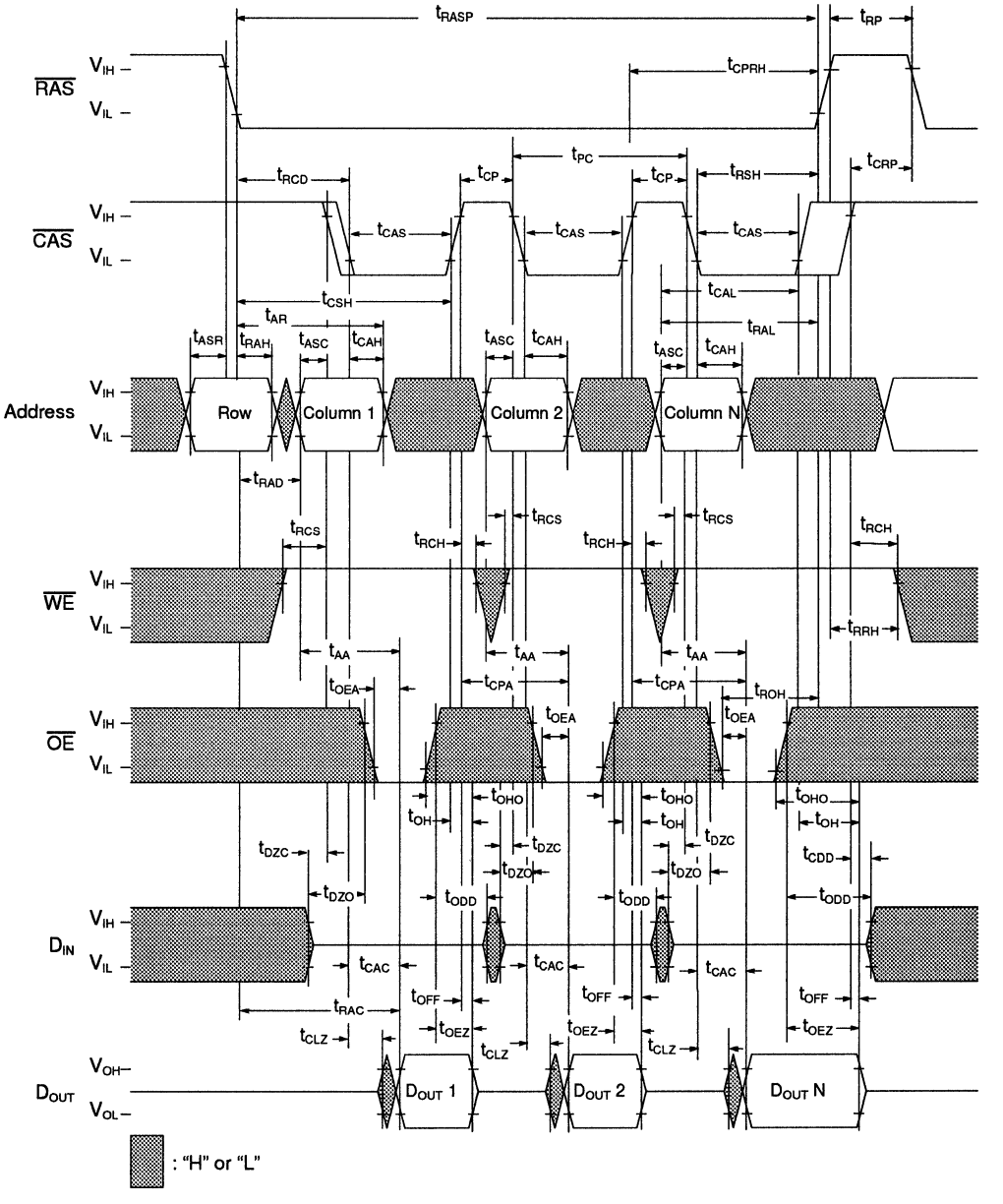


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

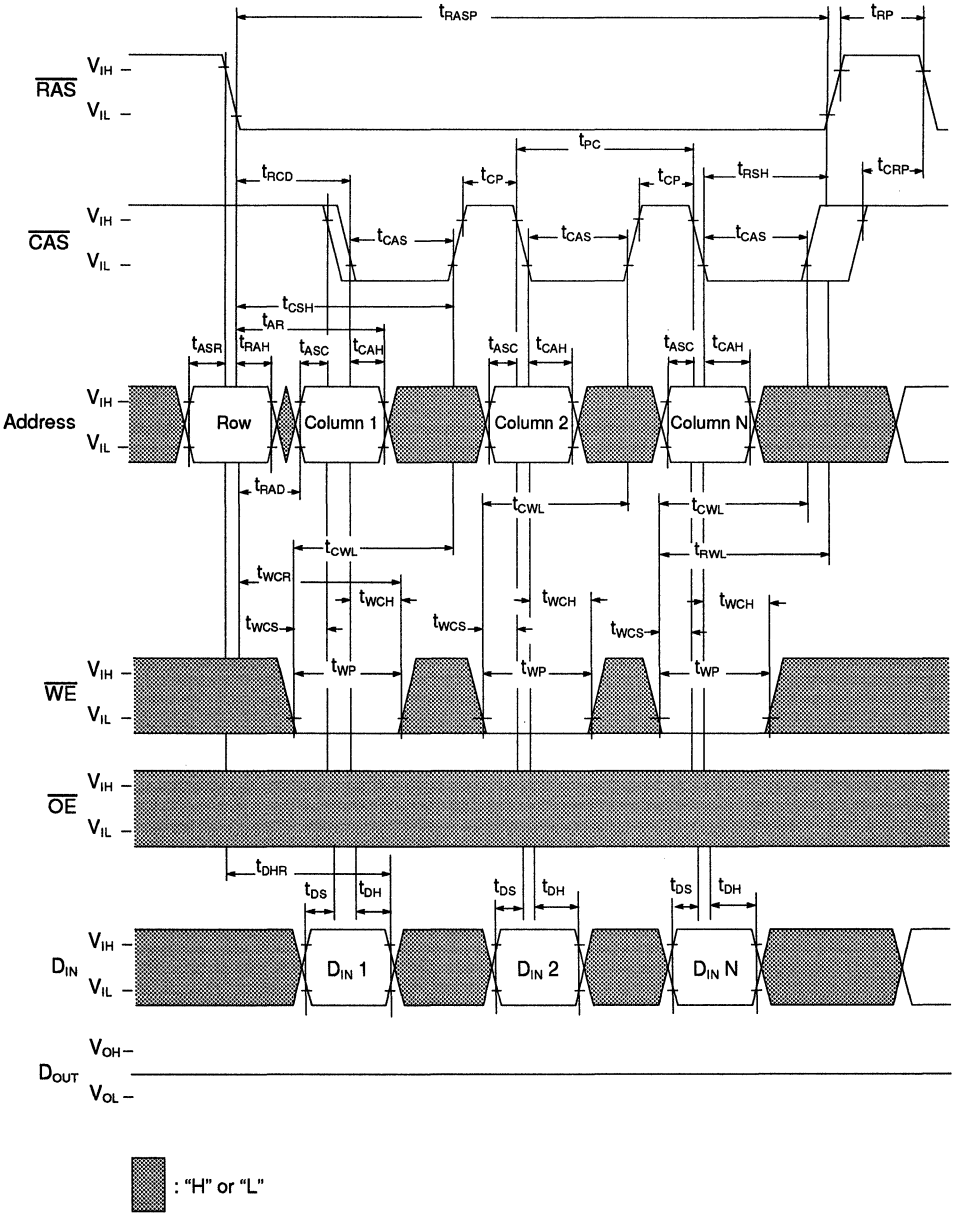
Read-Modify-Write Cycle



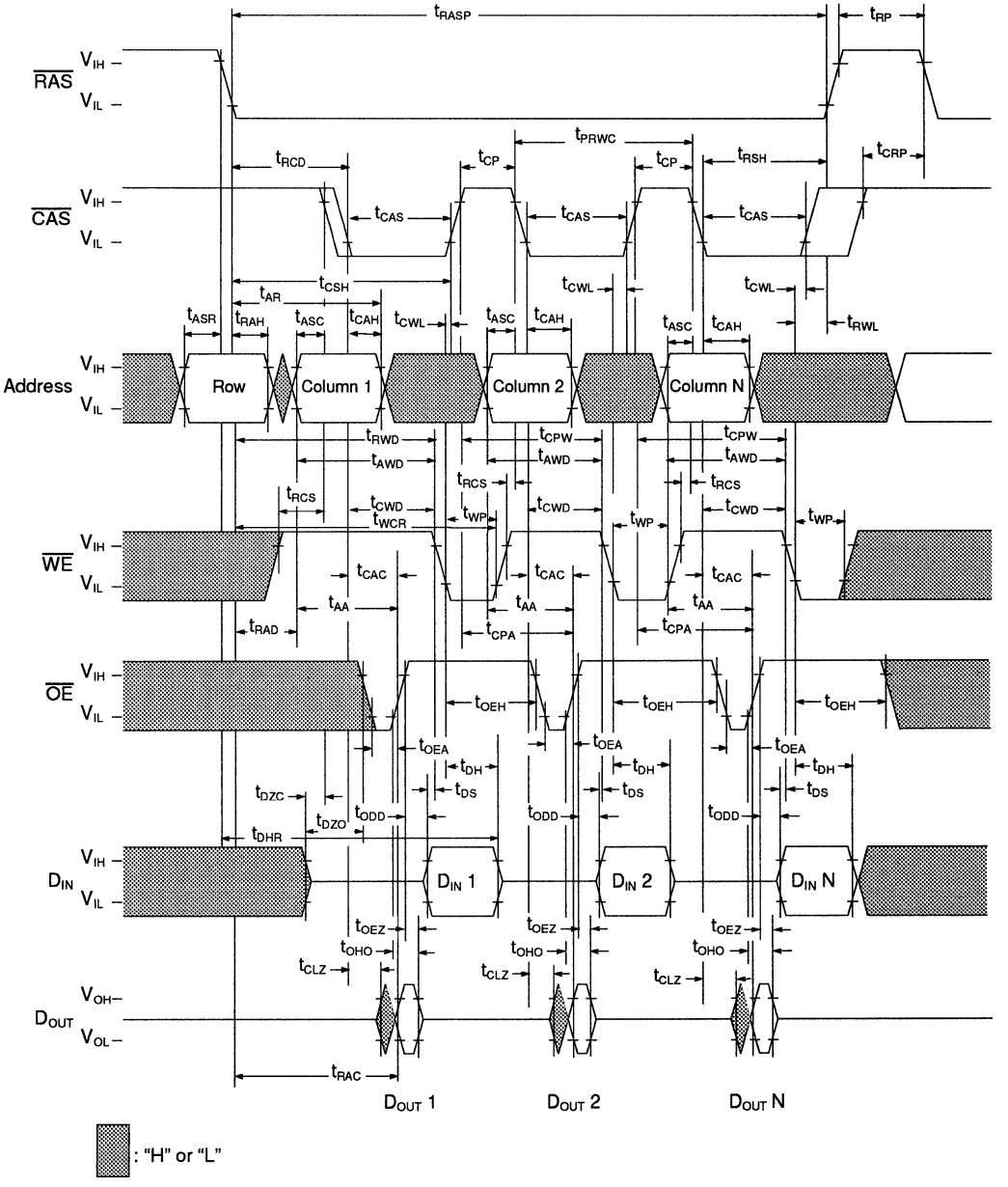
Fast Page Mode Read Cycle



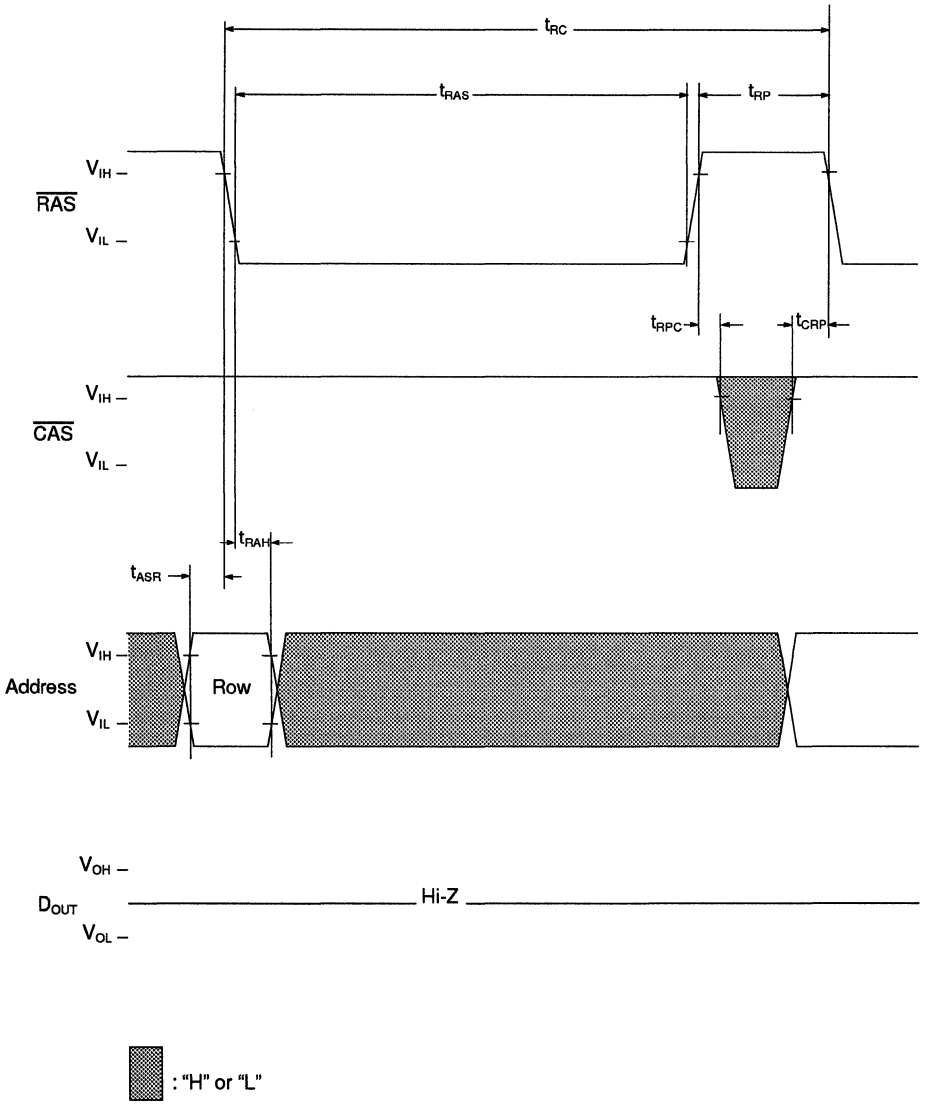
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

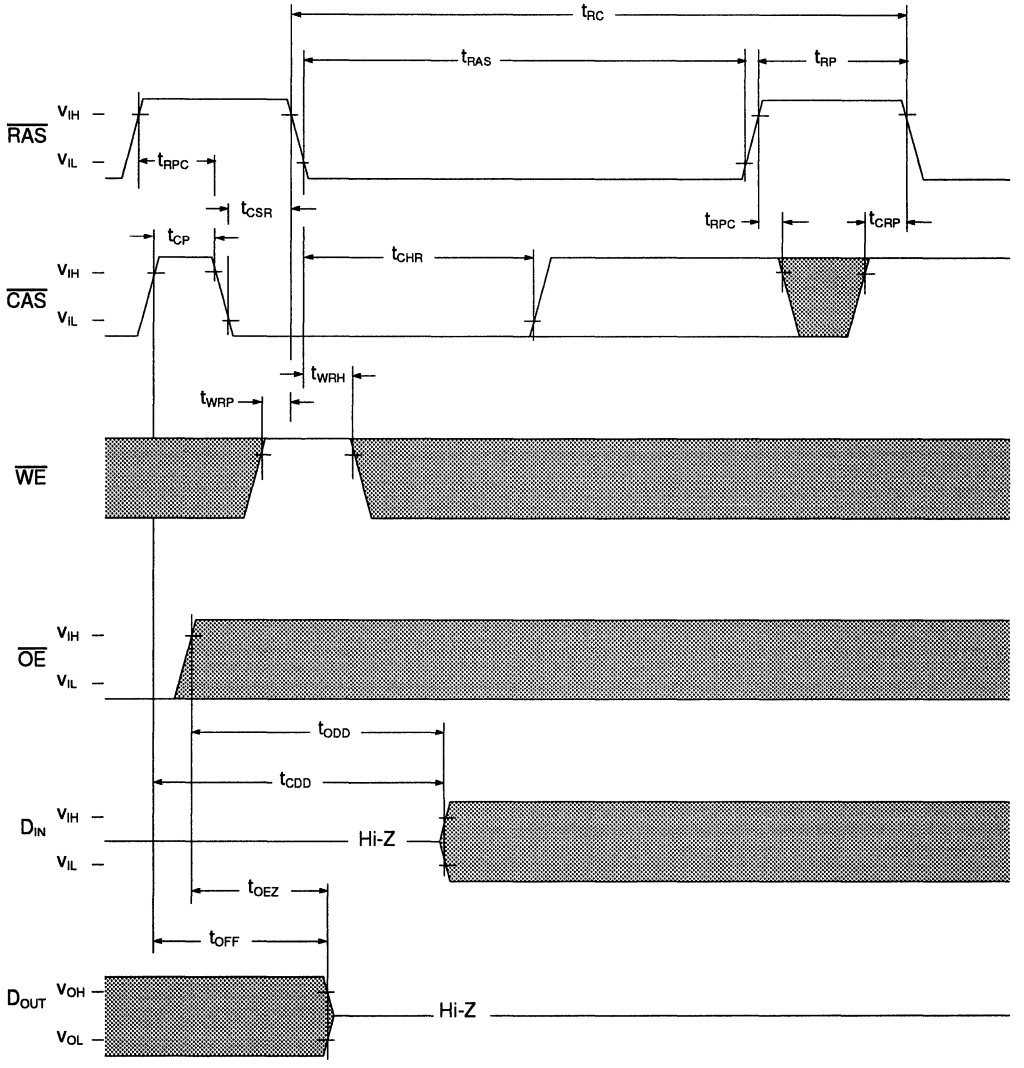


$\overline{RAS}$ Only Refresh Cycle



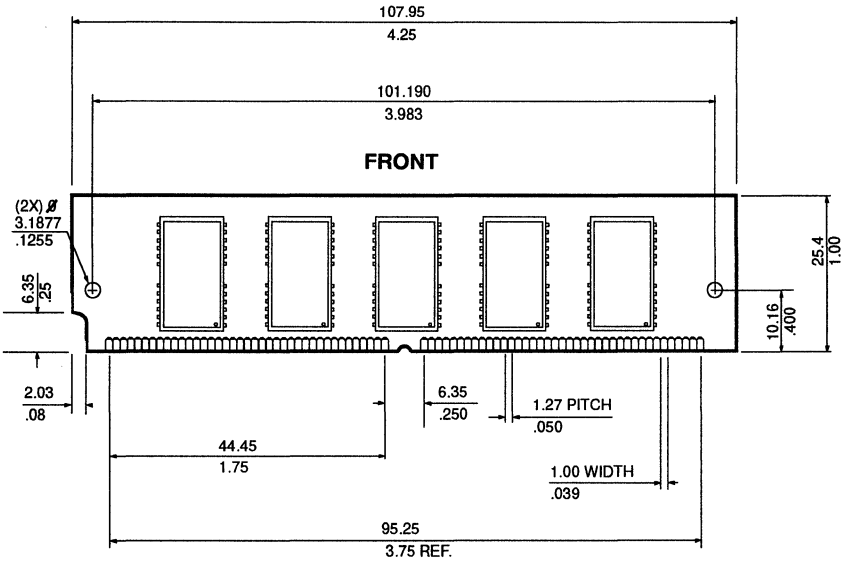
Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

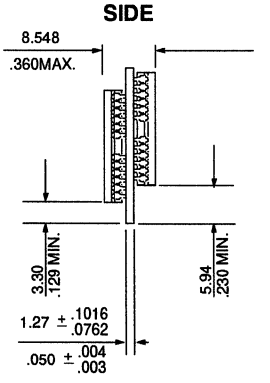
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing (IBM11D4400C)





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

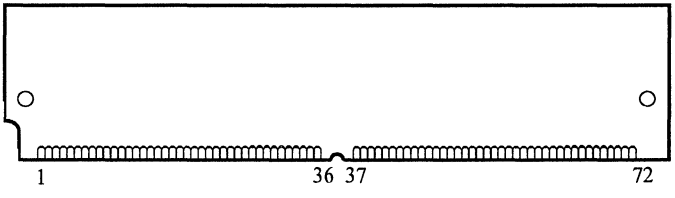
- Optimized for use in ECC applications
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode, Read-Modify-Write cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 4096 refresh cycles distributed across 64ms
- 12/10 Addressing (Row/Column)
- Au and Sn/Pb versions available

Description

The ECC-Optimized SIMMs, IBM11D8370C and IBM11D8400C are 32MB industry standard 72 pin 4-byte single inline memory modules (SIMMs). The Modules are organized as 8M x 36/40 high speed memory arrays, and are configured as 2 4M x 36/40 banks - each independently selectable via unique $\overline{RAS}$ inputs. The 8M x 36 assembly is intended for use in 8 byte applications, typically having 64 data and 8 check bits (64/72 code). The 8M x 40 assembly is applicable to 4 byte applications with 32 data and 7 or 8 check bits (32/39 code), or 8 byte applications with extended error correction capabilities. The modules are manufactured with 18 or 20 4M x 4 devices, each in a 300 mil package, and are compatible with the JEDEC 72-pin SIMM standard.

The IBM 72-pin SIMMs provide a high-performance, flexible 4-byte interface in a 4.25" long footprint. Related products include other density offerings and parity SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS1}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS1}$	Column Address Strobe
$\overline{WE}$	Read/write Input
$\overline{OE}$	Output Enable
A0 - A11	Address Inputs
DQ0-35 or DQ0-39	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
$\overline{ECC}$, PD1 - PD5	Presence Detects

Pinout

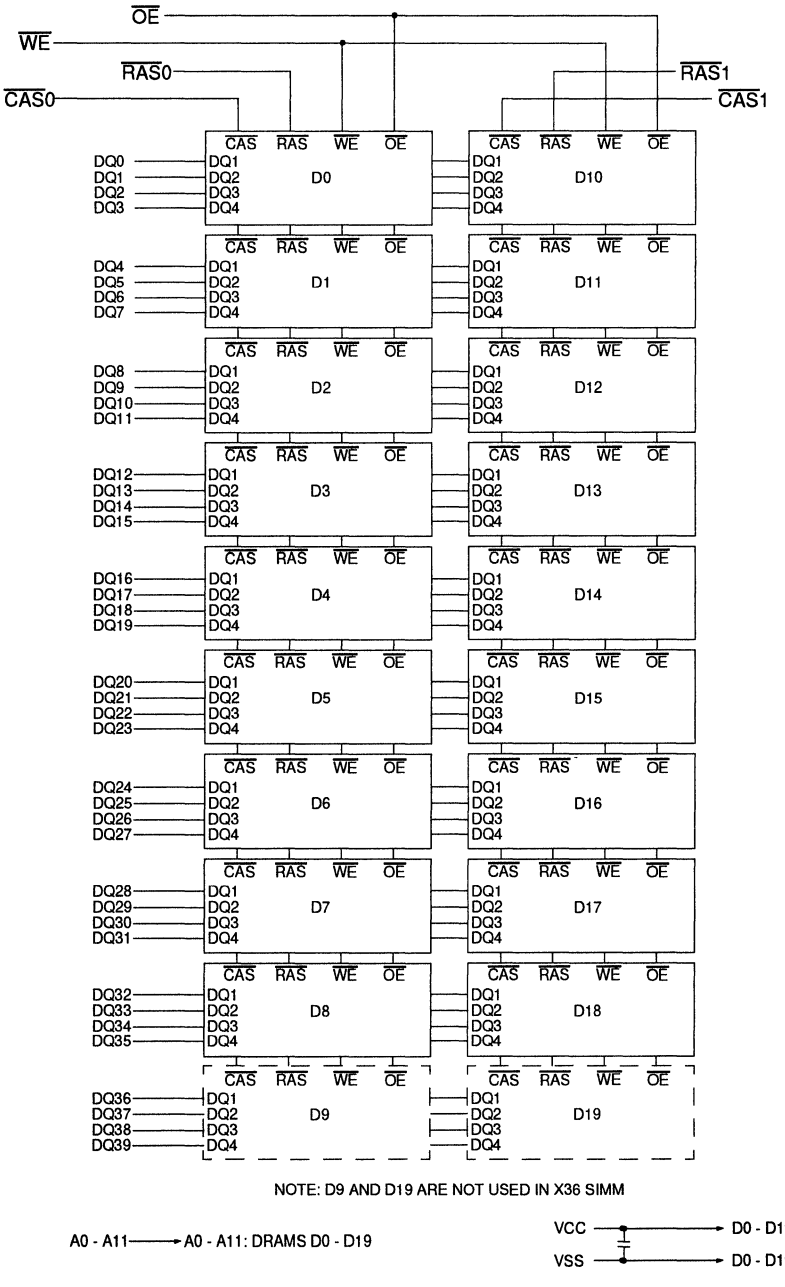
Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	A10	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	A11	54	DQ27	66	DQ38
7	DQ5	19	$\overline{OE}$	31	A8	43	$\overline{CAS1}$	55	DQ28	67	PD1
8	DQ6	20	DQ8	32	A9	44	$\overline{RAS0}$	56	DQ29	68	PD2
9	DQ7	21	DQ9	33	NC	45	$\overline{RAS1}$	57	DQ30	69	PD3
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD4
11	PD5	23	DQ11	35	DQ17	47	$\overline{WE}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	$\overline{ECC}$	60	DQ32	72	V_{SS}

1. DQ36 - DQ39 are NC for x36 SIMM.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D8370CA-60	8M x 36	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D8370CA-70	8M x 36	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E8370CA-60	8M x 36	60ns	Au	4.25" x 1" x .360"	
IBM11E8370CA-70	8M x 36	70ns	Au	4.25" x 1" x .360"	
IBM11D8400CA-60	8M x 40	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D8400CA-70	8M x 40	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E8400CA-60	8M x 40	60ns	Au	4.25" x 1" x .360"	
IBM11E8400CA-70	8M x 40	70ns	Au	4.25" x 1" x .360"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Col Address	All DQ Bits
Standby	H	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	Valid Data Out
Early-Write	L	L	L	X	Row	Col	Valid Data In
Late-Write / RMW	L	L	H→L	L→H	Row	Col	Valid Data Out, Valid Data In
Fast Page Mode-Read 1st cycle	L	H→L	H	L	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	Valid Data Out
Fast Page Mode-Write 1st cycle	L	H→L	L	X	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	Valid Data In
Fast Page Mode Read-Modify-Write: 1st cycle	L	H→L	H→L	L→H	Row	Col	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	L→H	N/A	Col	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	High Impedance

Presence Detect

Pin	-60	-70
$\overline{ECC}$ (ECC Optimized SIMM)	V_{SS}	V_{SS}
PD1	NC	NC
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC
PD5	V_{SS}	V_{SS}

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min(V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min(V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	9.35	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 2.0V for pulse widths ≤ 4.0ns (or V_{CC} + 1.0V for ≤ 8.0ns) and V_{IL} may undershoot to -2.0V for pulse widths ≤ 4.0ns (or -1.0V for ≤ 8.0ns). Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	x36 Max	x40 Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	126	130	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	74	80	pF	
C_{I3}	Input Capacitance ($\overline{WE}$)	149	155	pF	
C_{I4}	Input Capacitance ($\overline{OE}$)	168	174	pF	
$C_{I/O}$	Output Capacitance (All DQ bits)	25	25	pF	

8M x 36 DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	783	mA	1, 2, 3
		-70	—	693		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	36	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	783	mA	1, 3, 4
		-70	—	693		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	693	mA	1, 2, 3
		-70	—	603		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	18	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	783	mA	1, 3, 4
		-70	—	693		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{OE}$, $\overline{WE}$, ADDRESS	-180	+180	µA	
		$\overline{RAS}$, $\overline{CAS}$	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for 1 bank.

8M x 40 DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	870	mA	1, 2, 3
		-70	—	770		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	40	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	870	mA	1, 3, 4
		-70	—	770		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	770	mA	1, 2, 3
		-70	—	670		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	20	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	870	mA	1, 3, 4
		-70	—	770		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{OE}$, $\overline{WE}$, ADDRESS	-200	+200	µA	
		$\overline{RAS}$, $\overline{CAS}$	-100	+100		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for 1 bank.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	15	—	20	—	ns	3
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	—	0	—	ns	4
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	4
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	—	5
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. Either t_{CDD} or t_{ODD} must be satisfied.
4. Either t_{DZC} or t_{DZO} must be satisfied.
5. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	1
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	3
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	15	—	20	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OES}	$\overline{OE}$ Setup Time prior to $\overline{RAS}$	—	—	—	—	ns	4
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	3	—	3	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	5
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	—	—	—	—	ns	4
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	6
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	0	15	0	20	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	150	—	180	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80	—	95	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	35	—	45	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	50	—	60	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	80	—	95	—	ns	
t_{CPW}	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	55	—	65	—	ns	1

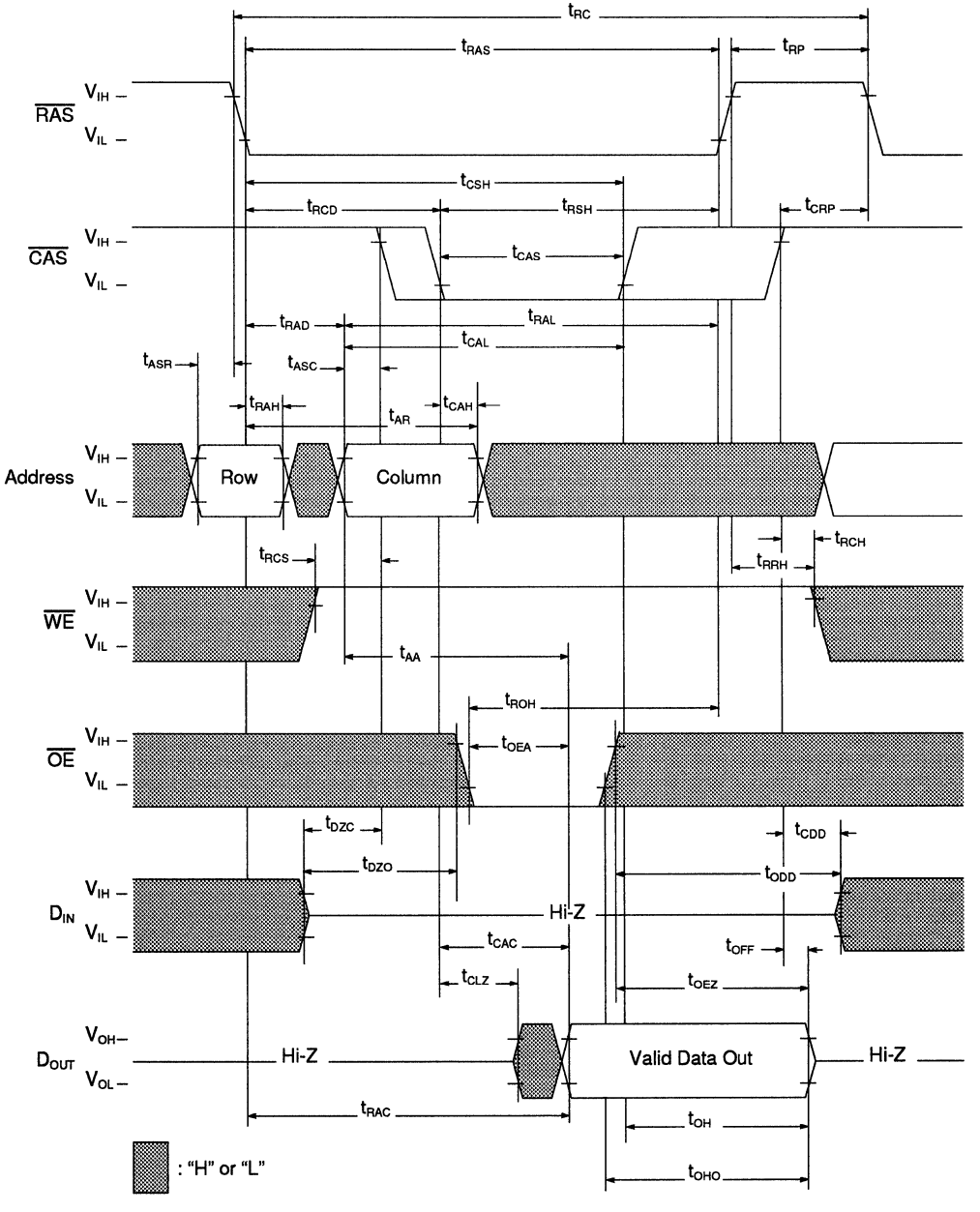
1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Refresh Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	10	—	10	—	ns	
t_{RWH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	64	—	64	ms	1

1. 4096 Refreshes are required every 64ms.

Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
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tASR
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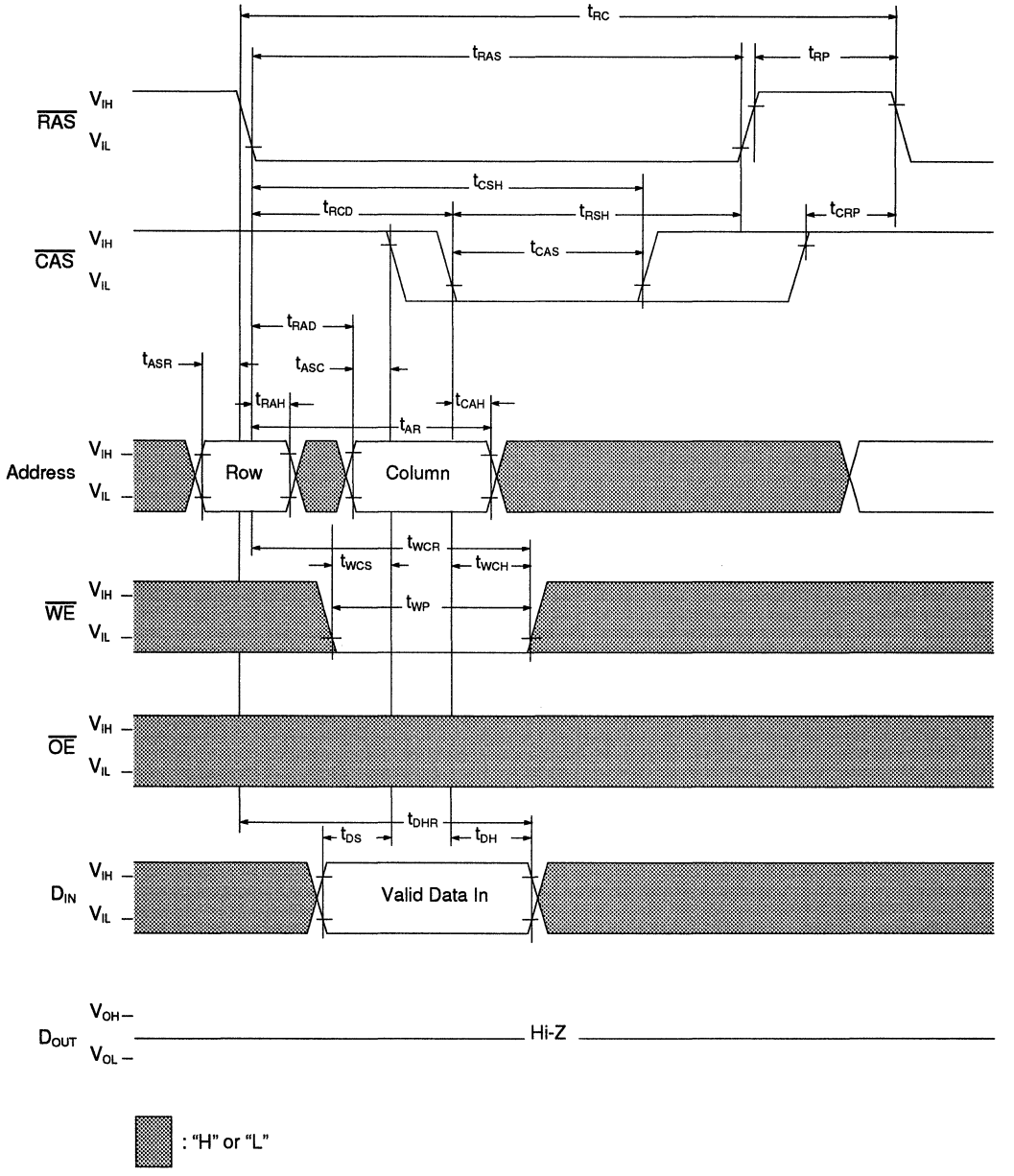
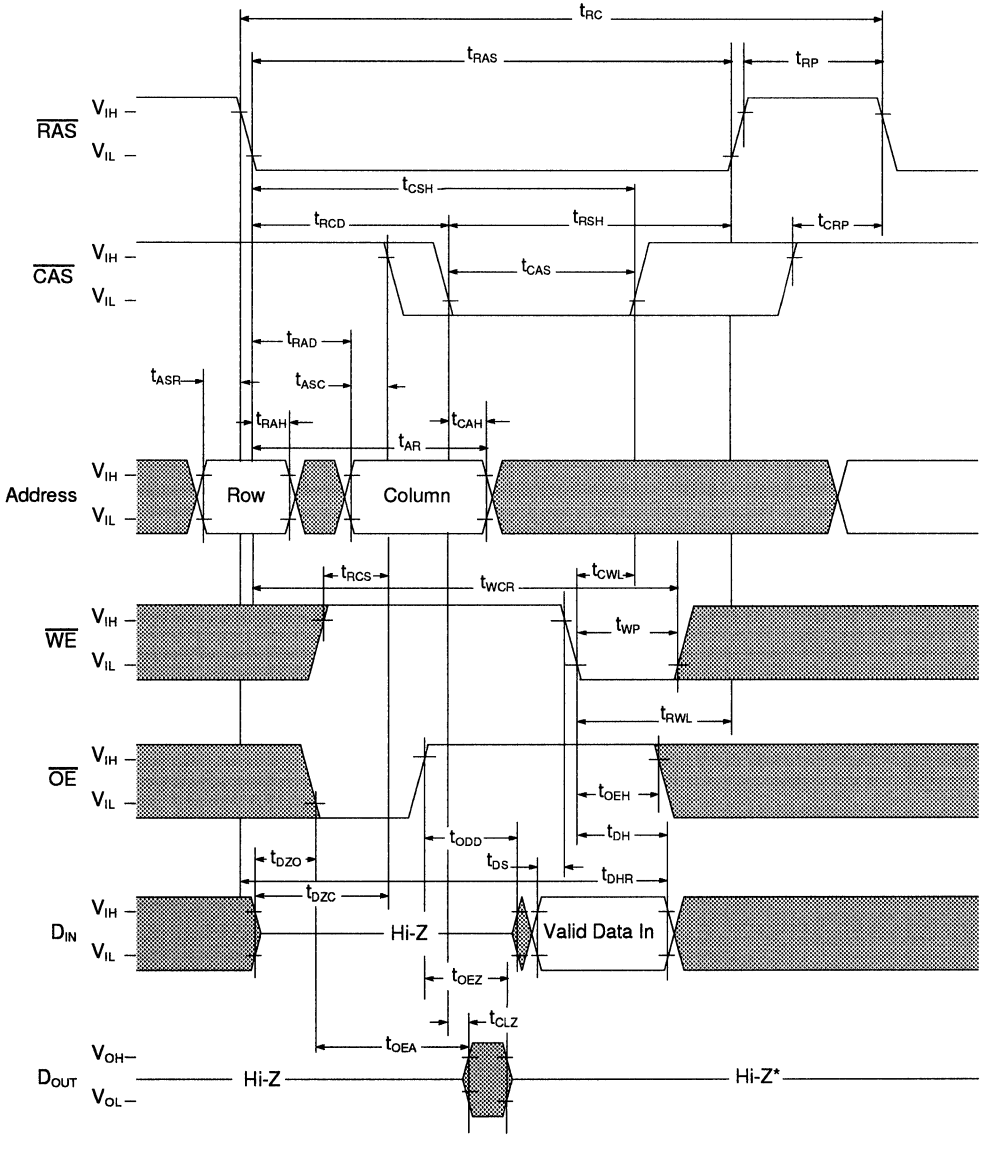
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Valid Data Out
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

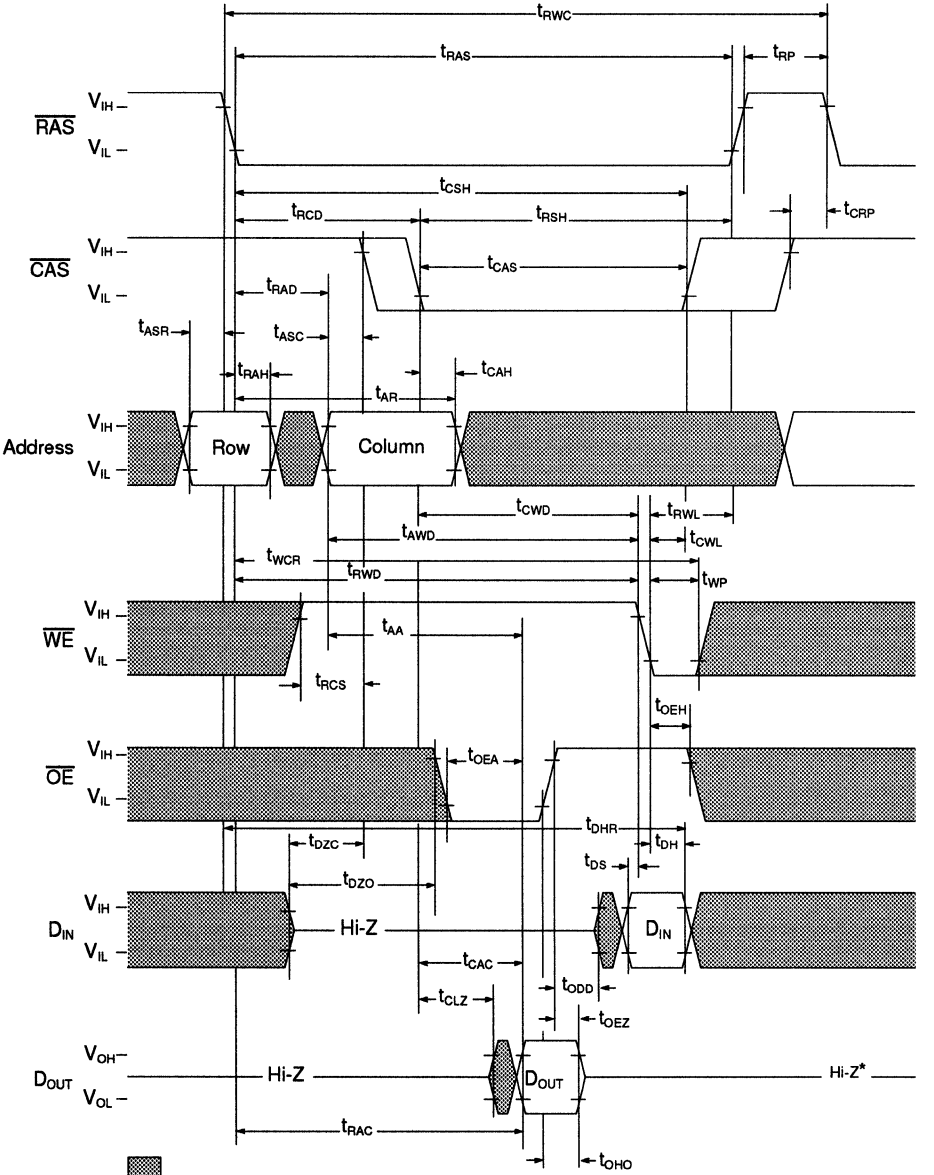


Write Cycle (Late Write)

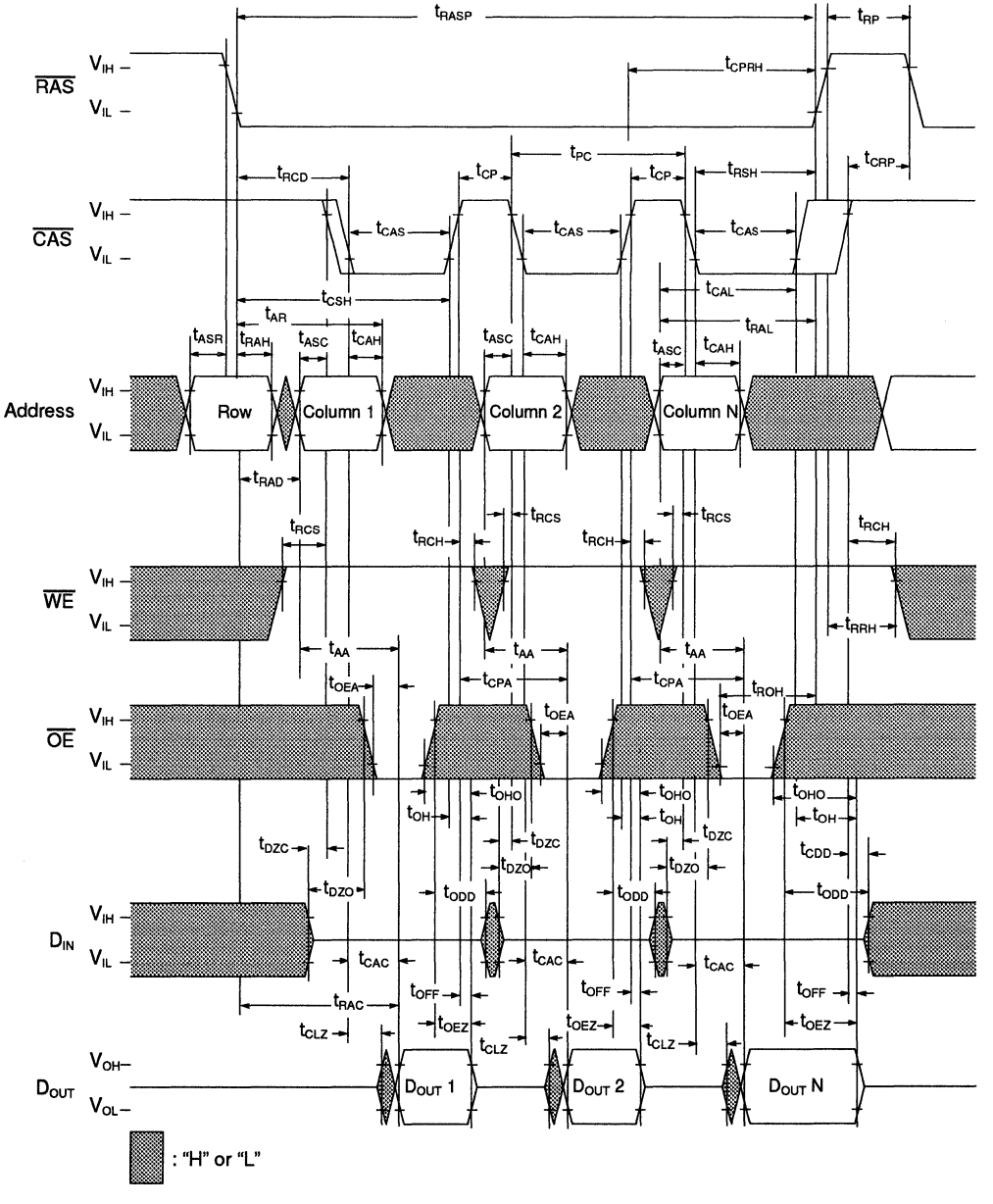


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

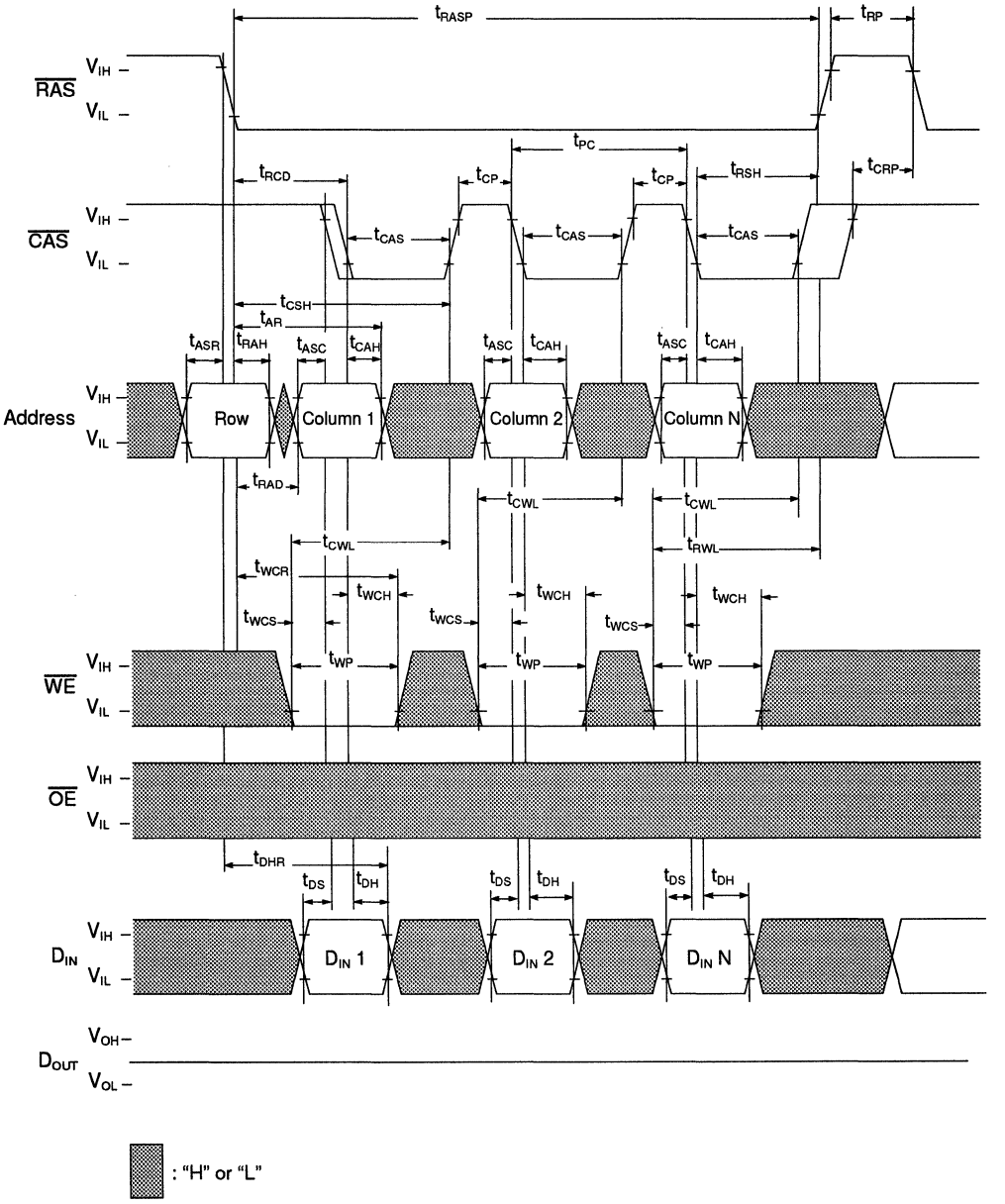
Read-Modify-Write Cycle



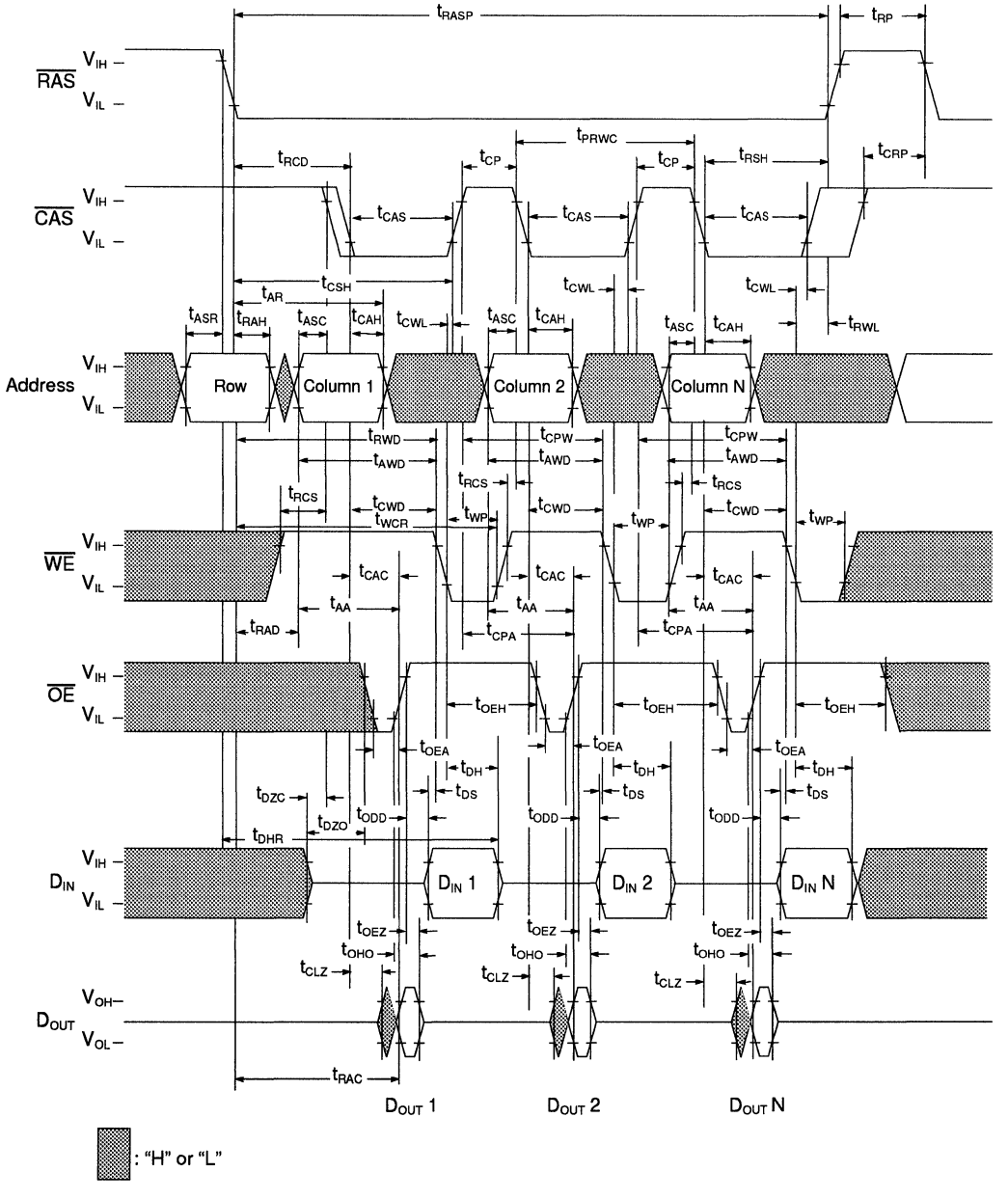
Fast Page Mode Read Cycle



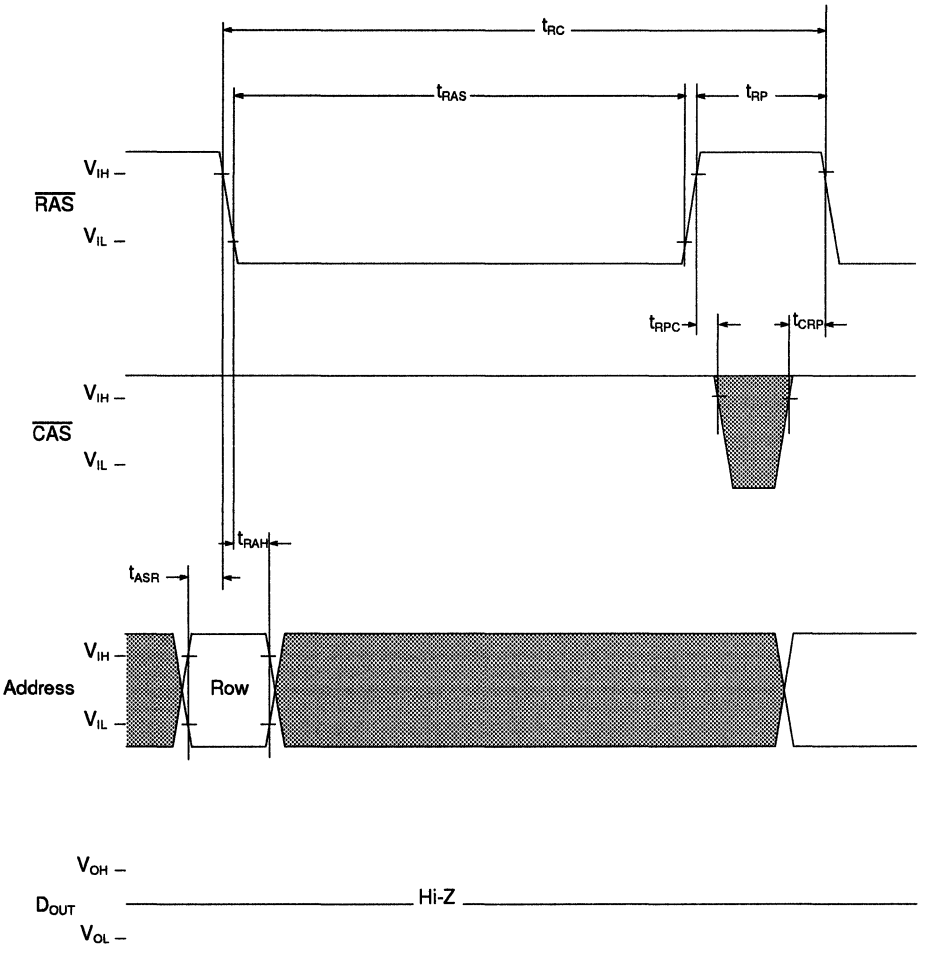
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

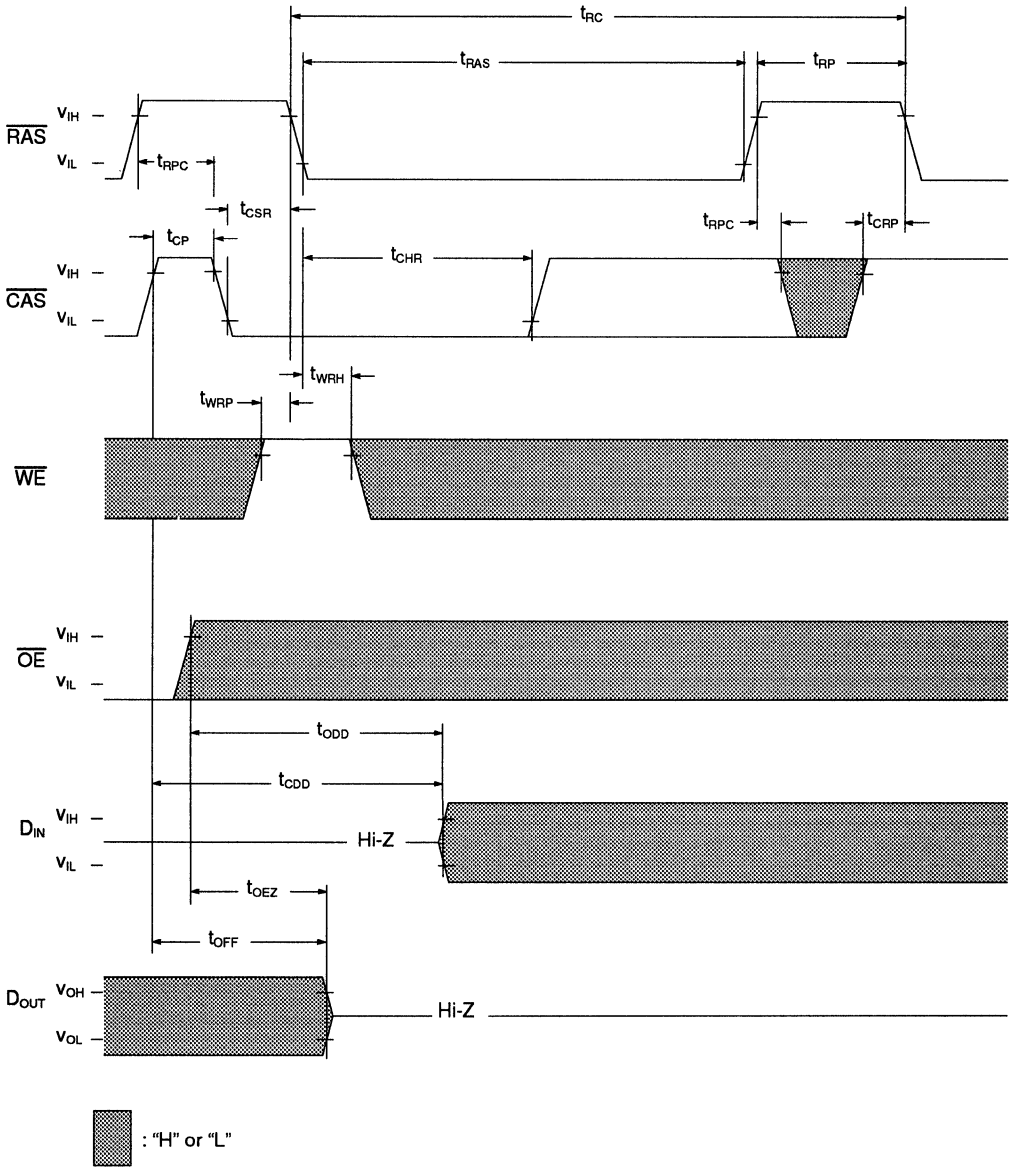


$\overline{RAS}$ Only Refresh Cycle



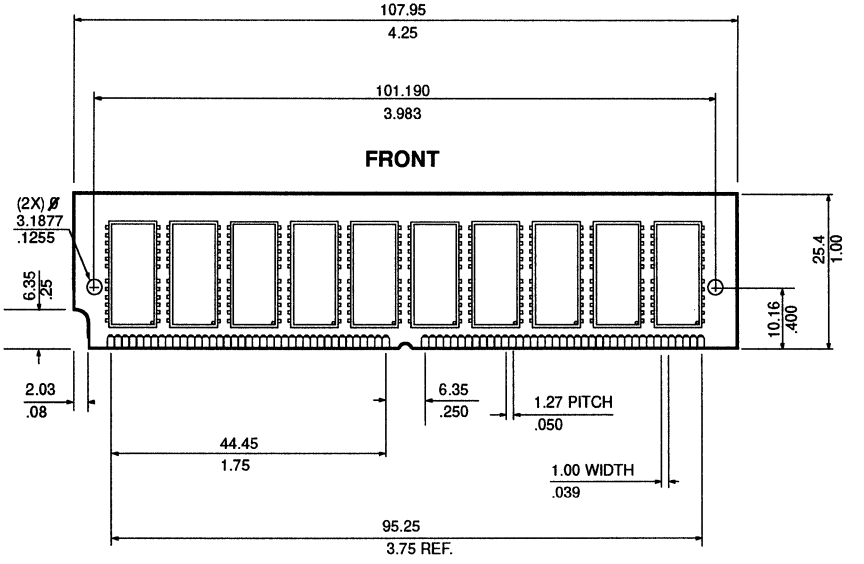
Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

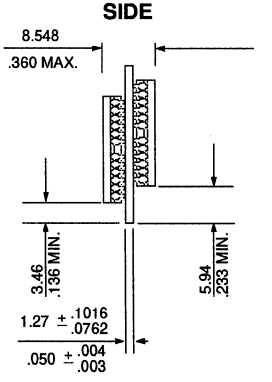
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing (IBM11D8400C)





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

72 Pin SIMMs

- ECC-On-SIMM

Features

- 72-Pin JEDEC-Standard Single In-Line Memory Module
- Performance:

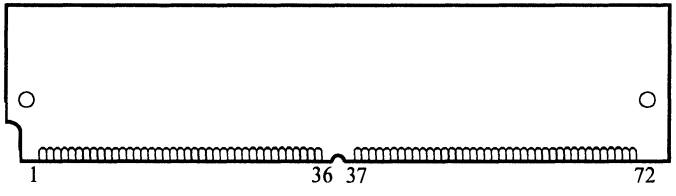
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{AA}	Access Time From Address	35ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Single-error-correct (SEC) high-speed ECC algorithm
- Single 5V ± 0.25V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Provides ECC and retrofits to standard x36 socket
- Au and Sn/Pb versions available

Description

The IBM11D1480BA is a 4MB industry standard 72-pin 4-byte single in-line memory module (SIMM) that has a fully functional, retrofittable and plug-compatible on-board error-correcting-code (ECC). The ECC function is completely self-contained and transparent to the system. The module is manufactured with 12 1M x 4 DRAMS and 4 ECC ASICs. The ECC-on-SIMM module corrects single-bit errors that may occur in any byte of SIMM data. It is recommended for systems that run critical applications but do not have native ECC. This family of SIMMs (1M x 36, 2M x 36, 4M x 36, and 8M x 36) provides the memory reliability required by these applications with no performance penalty. The outline varies per density.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

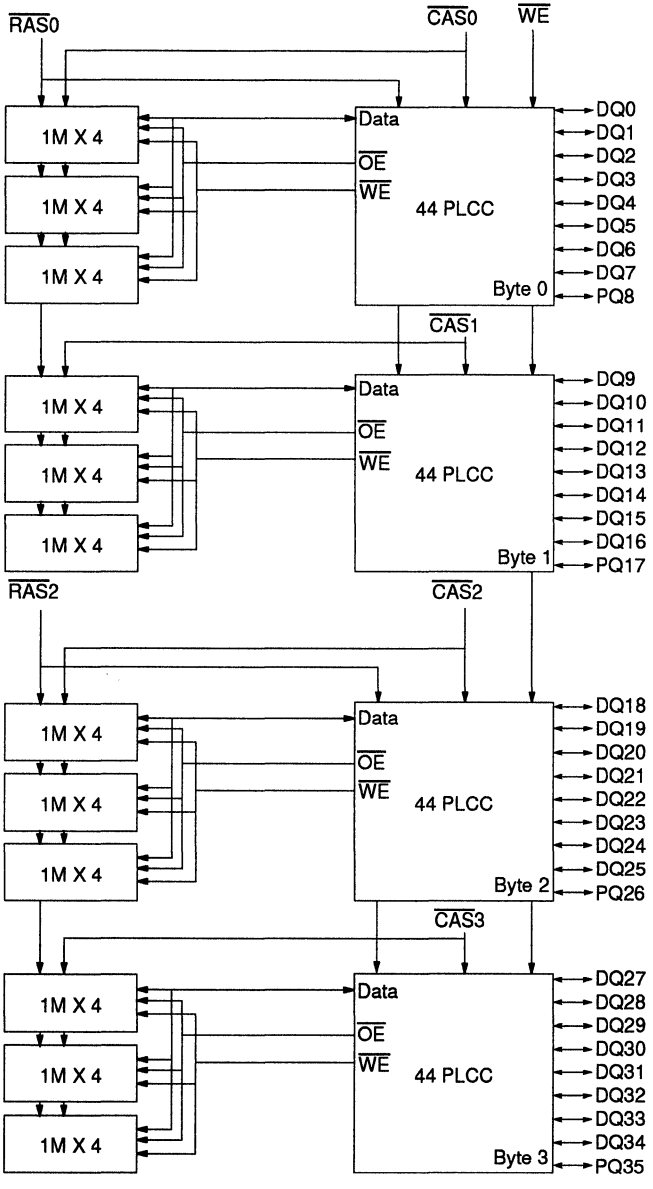
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D1480BA-70	1M x 36	70ns	Sn/Pb	4.25" x 1.04" x .397"	
IBM11E1480BA-70	1M x 36	70ns	Au	4.25" x 1.04" x .397"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	Application Specific -70	Industry Standard -70
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	V_{SS}	NC

1. NC= OPEN, V_{SS} = GND ; Application specific SIMMs have unique IBM part numbers.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.3 to 6.5	V	1
V_{IN}	Input Voltage	-0.3 to V_{CC} + 0.3	V	1
V_{OUT}	Output Voltage	-0.3 to V_{CC} + 0.3	V	1
T_C	Operating Temperature (Case)	0 to +65	°C	1
T_{STG}	Storage Temperature	-40 to +125	°C	1
P_D	Power Dissipation	12	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_C = 0 to 65°C)

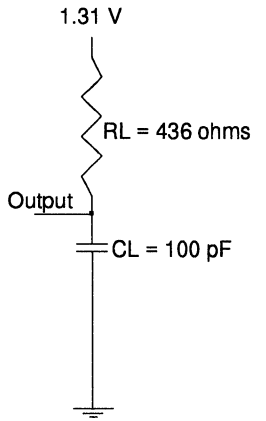
Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

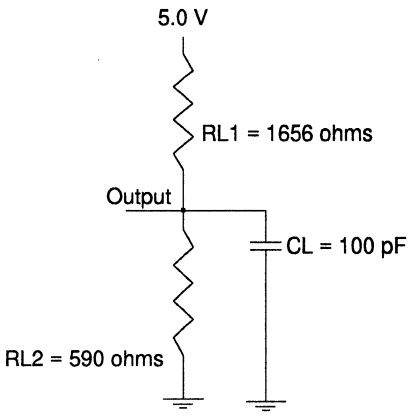
Capacitance (T_C = 0 to +65°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	65	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	50	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	30	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	35	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	12	pF	
$C_{I/O2}$	Output Capacitance (PQ8, 17, 26, 35)	12	pF	

Load Diagram



LOAD CIRCUIT



ALTERNATE LOAD CIRCUIT

DC Electrical Characteristics (Tc = 0 to +65°C, V_{CC} = 5 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	1296	mA	1, 2, 3
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	24	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	1296	mA	1, 3
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	780	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	24	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	1296	mA	1, 3
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-460	+460	µA	
		$\overline{CAS}$, $\overline{WE}$	-40	+40		
		Address	-120	+120		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -4mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_C = 0 to +65°C, V_{CC} = 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 500ms is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	—	—	ns	3
t_T	Transition Time (Rise and Fall)	3	50	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	55	—	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	20	—	ns	

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	—	—	ns	1
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	45	ns	2, 3

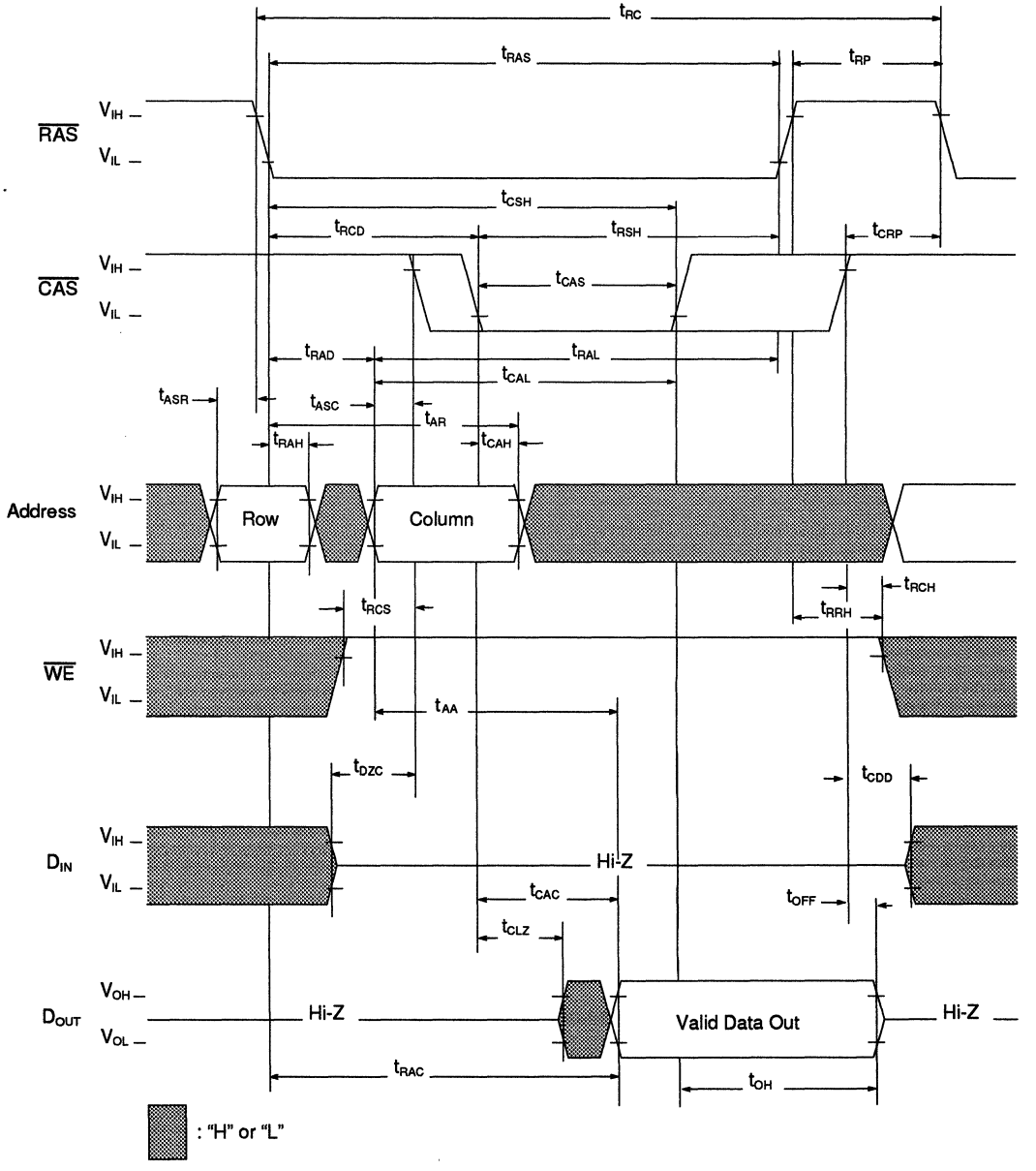
1. This timing parameter is not applicable to this product, but applies to a related product in this family.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Access time assumes a load of 100pF.

Refresh Cycle

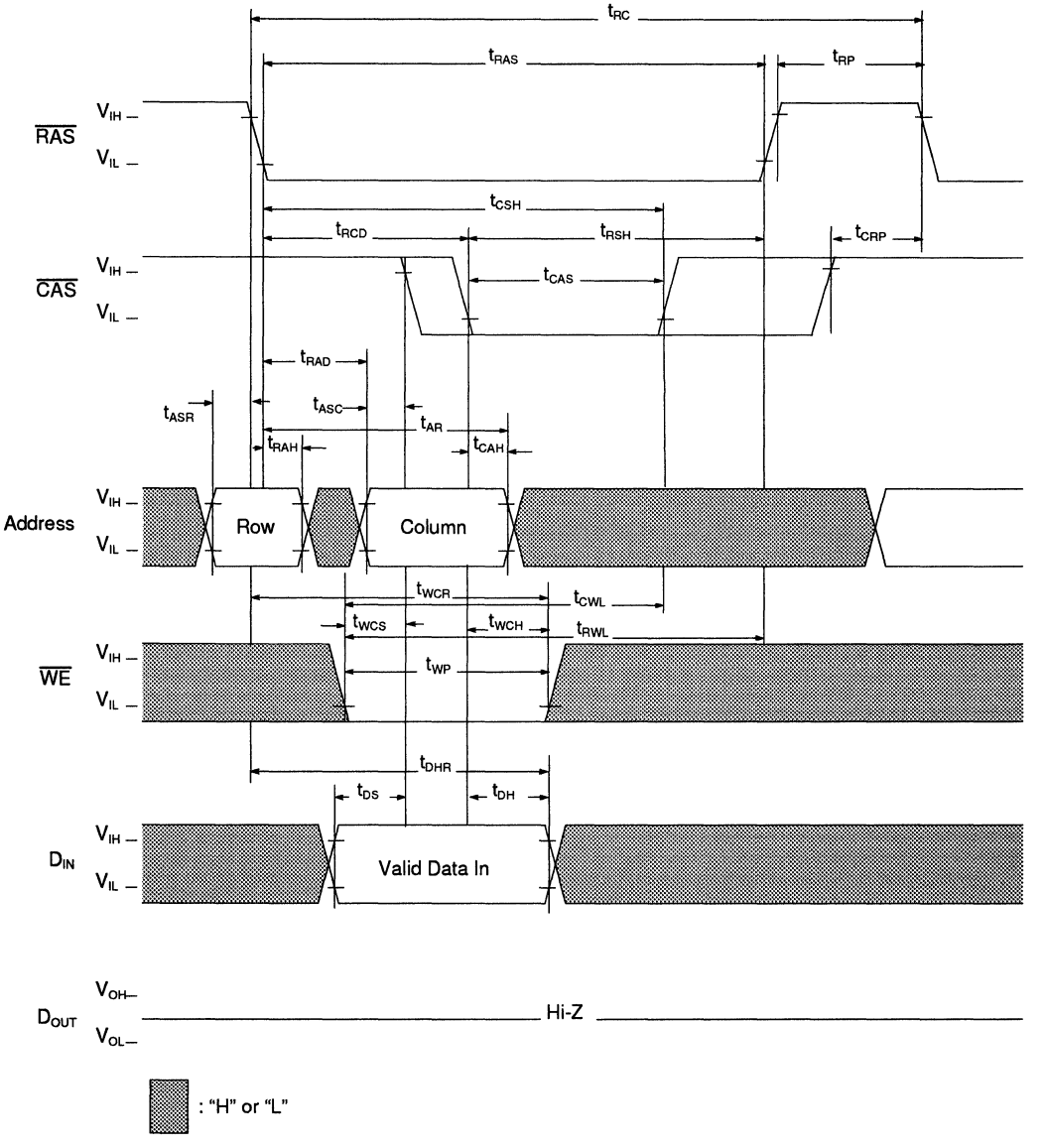
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	ns	
t_{REF}	Refresh Period	—	16	ms	1

1. 1024 refreshes are required every 16ms. The DC variation in the V_{CC} supply may not exceed 300mV within a refresh interval (16ms).

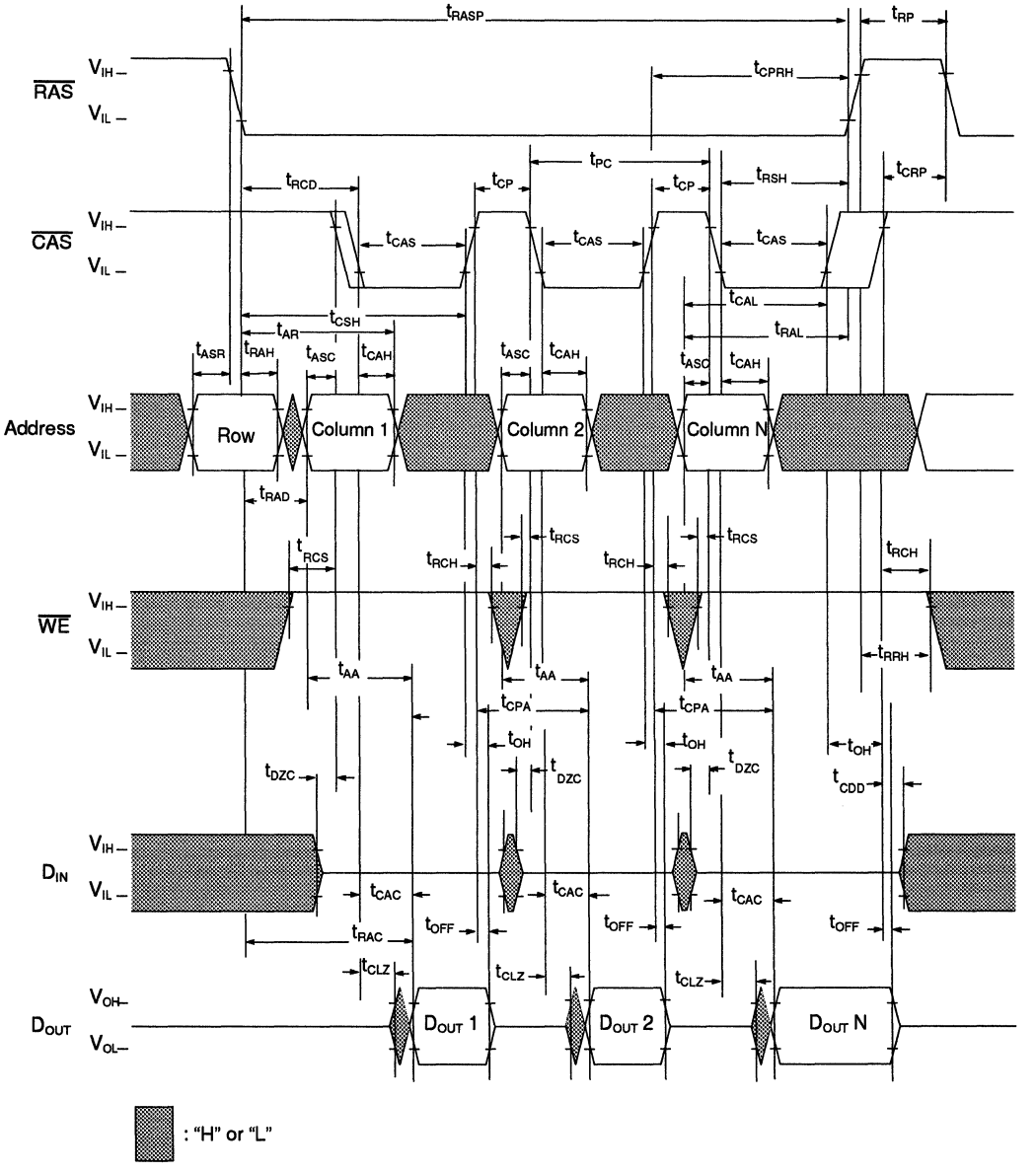
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Valid Data Out
tRAC
tOH
: "H" or "L"

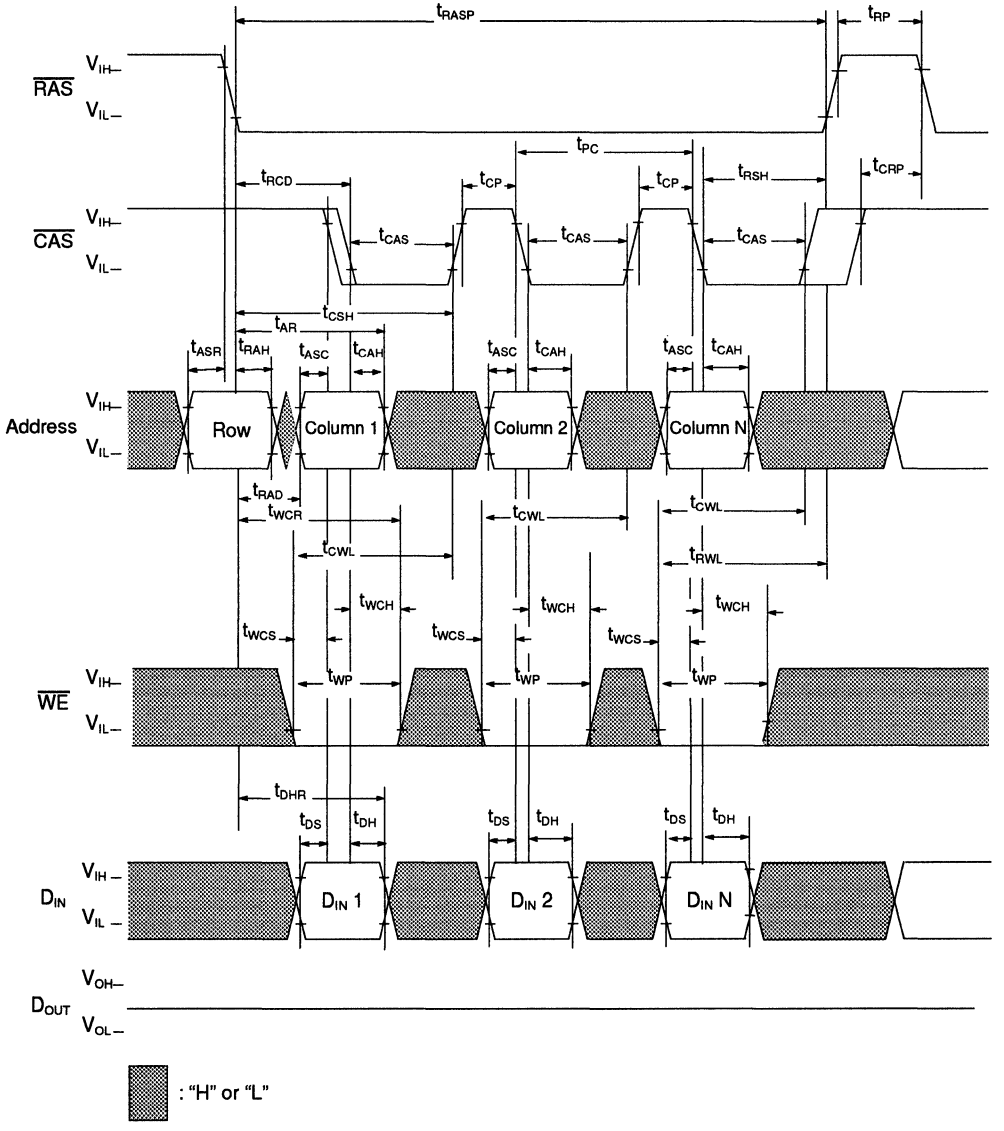
Write Cycle (Early Write)



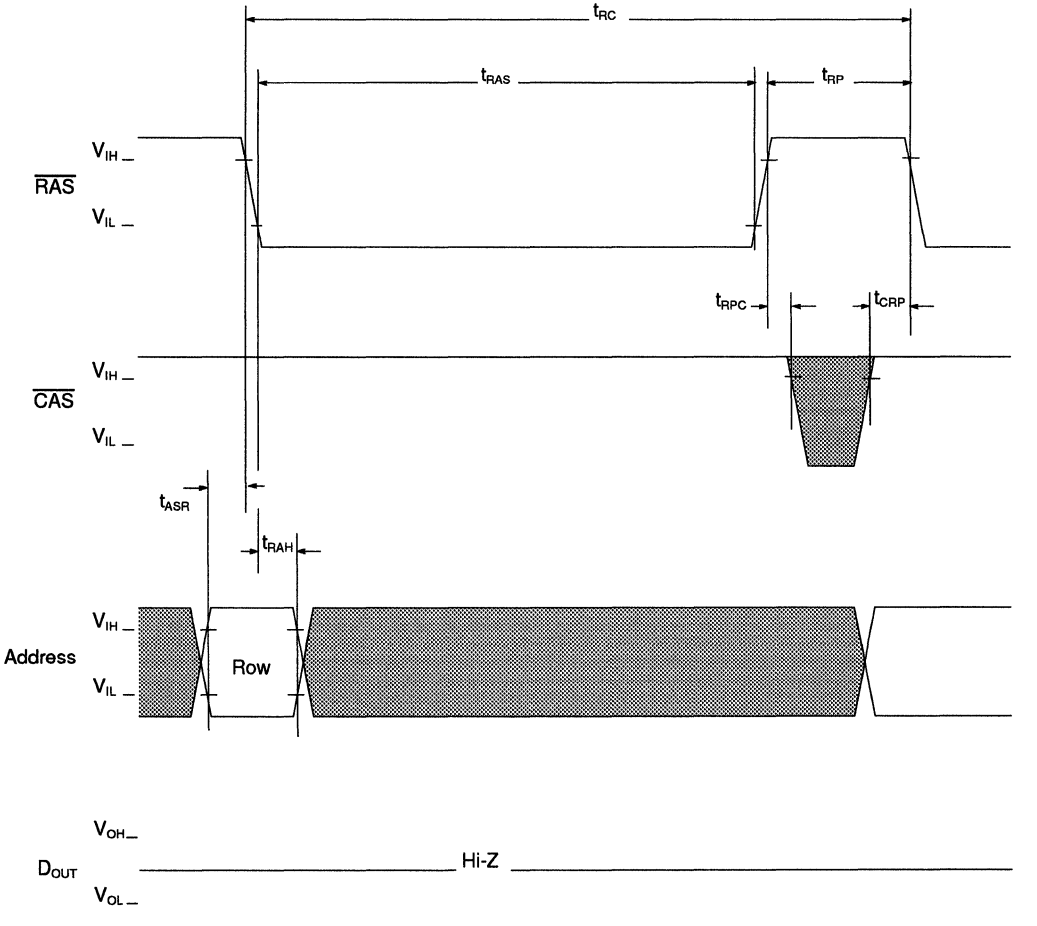
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

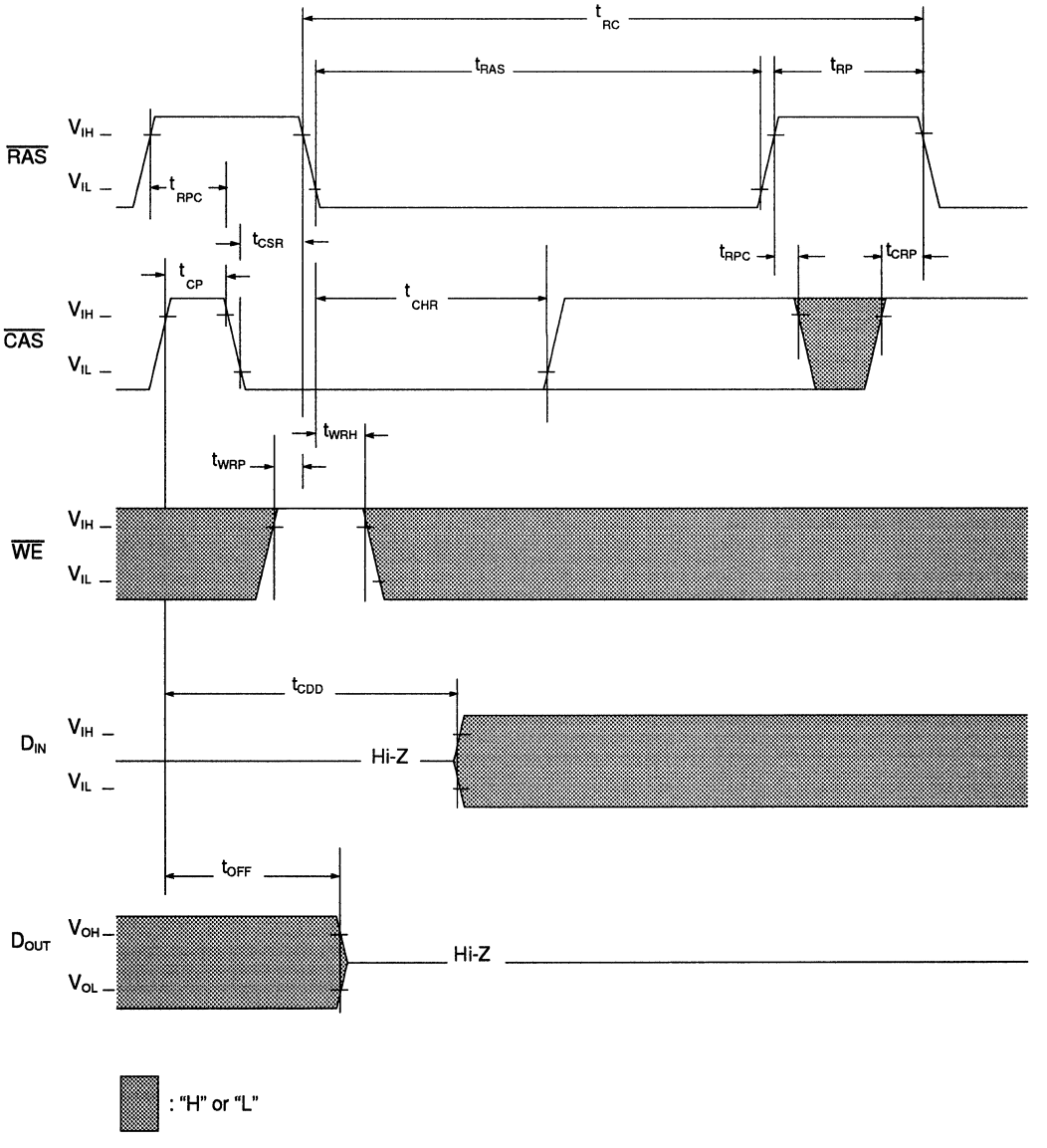


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, D_{IN} are "H" or "L"

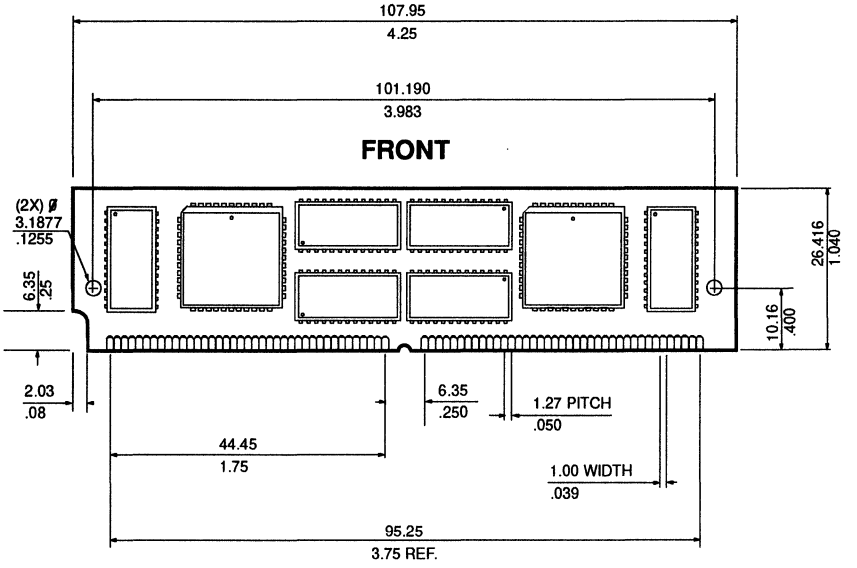
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



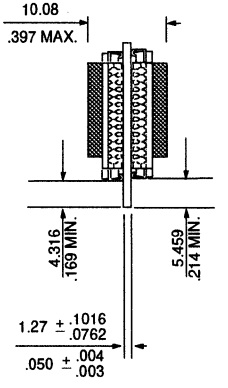
: "H" or "L"

Note: Addresses are "H" or "L"

Layout Drawing



SIDE



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

4Features

- 72-Pin JEDEC-Standard Single In-Line Memory Module
- Performance:

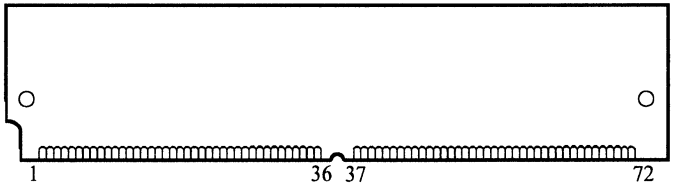
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{AA}	Access Time From Address	35ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Single-error-correct (SEC) high-speed ECC algorithm
- Single 5V 0.25V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Provides ECC and retrofits to standard x36 socket
- Au and Sn/Pb versions available

Description

The IBM11D2480BA is an 8MB industry standard 72-pin 4-byte single in-line memory module (SIMM) that has a fully functional, retrofittable and plug-compatible on-board error-correcting-code (ECC). The ECC function is completely self-contained and transparent to the system. The module is manufactured with 24 1M x 4 DRAMS and 4 ECC ASICs. The ECC-on-SIMM module corrects single-bit errors that may occur in any byte of SIMM data. It is recommended for systems that run critical applications but do not have native ECC. This family of SIMMs (1M x 36, 2M x 36, 4M x 36, and 8M x 36) provides the memory reliability required by these applications with no performance penalty. The outline varies per density.

Card Outline



Pin Description

$\overline{RAS0}$-$\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

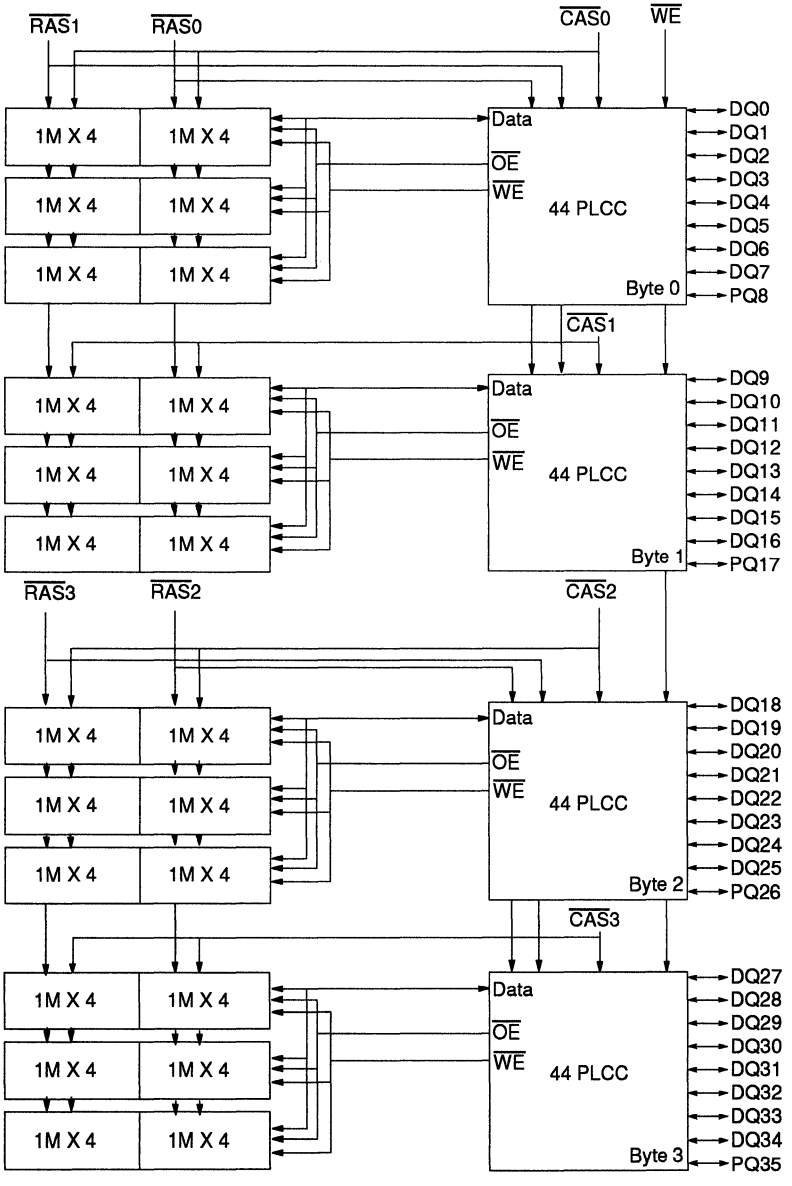
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D2480BA-70	2M x 36	70ns	Sn/Pb	4.25" x 1.04" x .559"	
IBM11E2480BA-70	2M x 36	70ns	Au	4.25" x 1.04" x .559"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	Application Specific -70	Industry Standard -70
PD1	NC	NC
PD2	NC	NC
PD3	V_{SS}	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND ; Application specific SIMMs have unique IBM part numbers.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.3 to 6.5	V	1
V_{IN}	Input Voltage	-0.3 to V_{CC} + 0.3	V	1
V_{OUT}	Output Voltage	-0.3 to V_{CC} + 0.3	V	1
T_C	Operating Temperature (Case)	0 to +65	°C	1
T_{STG}	Storage Temperature	-40 to +125	°C	1
P_D	Power Dissipation	24	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_C = 0 to 65°C)

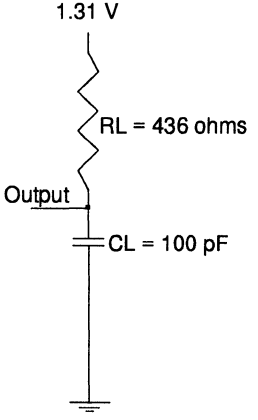
Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

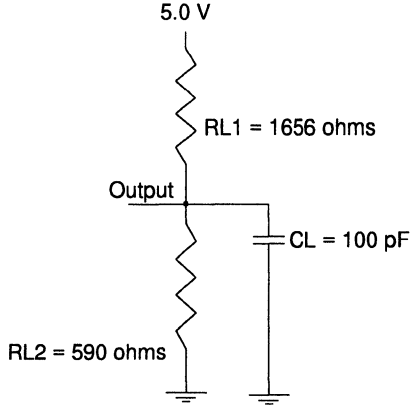
Capacitance (T_C = 0 to +65°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	140	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	50	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	45	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	35	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	12	pF	
$C_{I/O2}$	Output Capacitance (PQ8, 17, 26, 35)	12	pF	

Load Diagram



LOAD CIRCUIT



ALTERNATE LOAD CIRCUIT

DC Electrical Characteristics (Tc = 0 to +65°C, V_{CC} = 5 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	1320	mA	1, 2, 3
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	48	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	1320	mA	1, 3, 4
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	804	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	48	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	1320	mA	1, 3, 4
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-460	+460	µA	
		$\overline{CAS}$, $\overline{WE}$	-70	+70		
		Address	-240	+240		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -4mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. When refreshing both banks at once, the refresh current becomes 2592 mA.

AC Characteristics (T_C = 0 to +65°C, V_{CC} = 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 500ms is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	—	—	ns	3
t_T	Transition Time (Rise and Fall)	3	50	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	55	—	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	20	—	ns	

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	—	—	ns	1
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	45	ns	2, 3

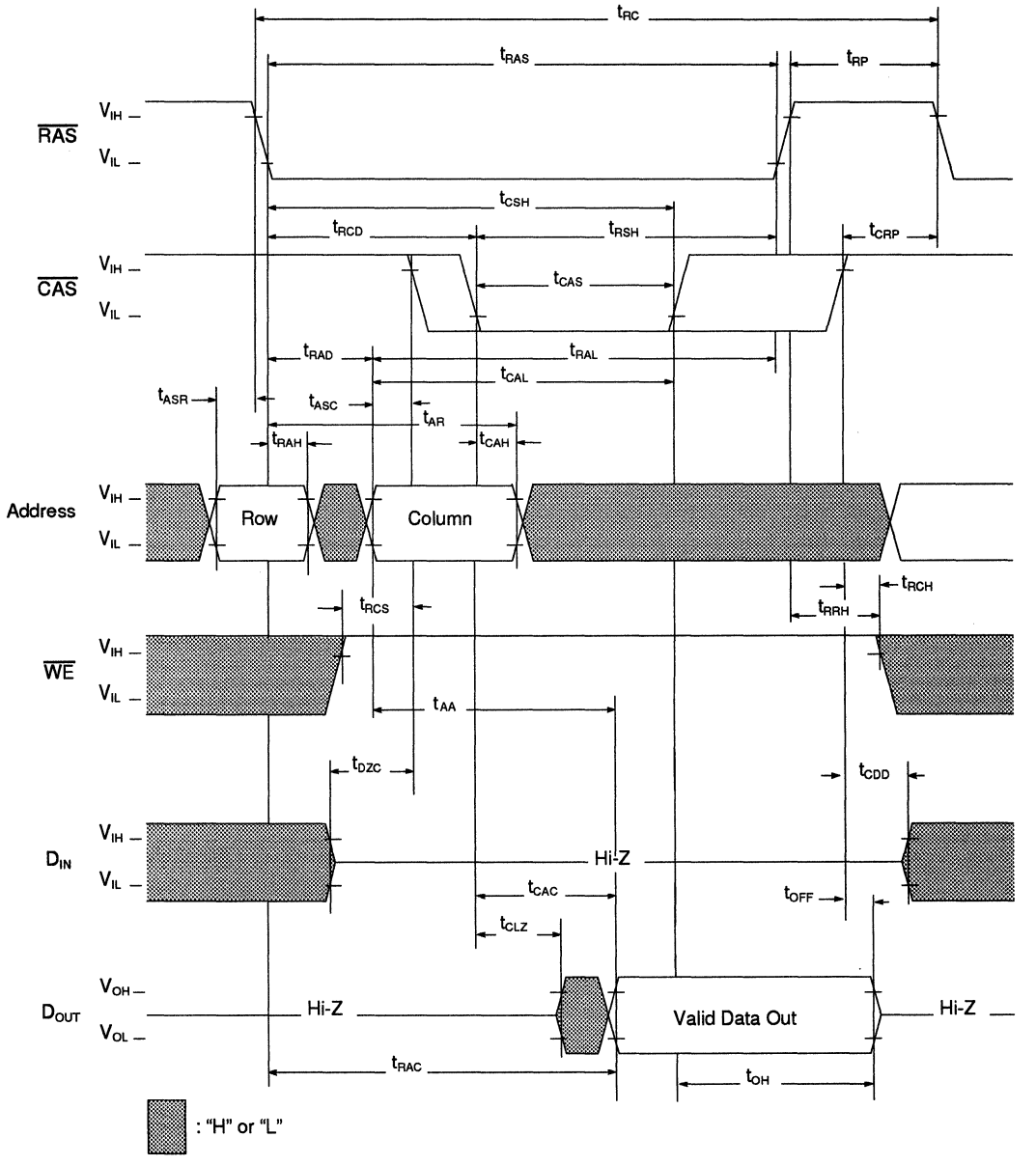
1. This timing parameter is not applicable to this product, but applies to a related product in this family.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Access time assumes a load of 100pF.

Refresh Cycle

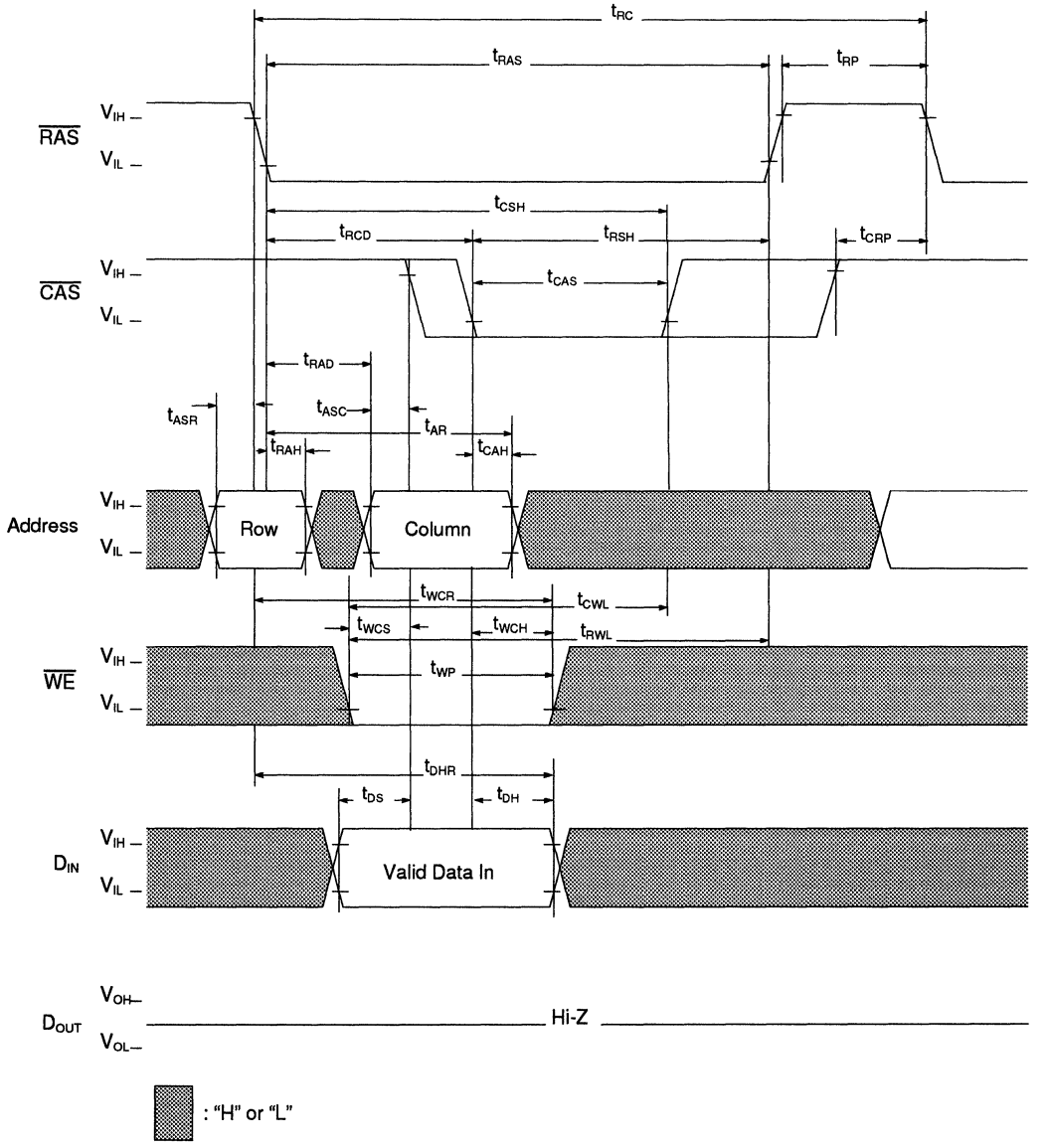
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	ns	
t_{REF}	Refresh Period	—	16	ms	1

1. 1024 refreshes are required every 16ms. The DC variation in the V_{CC} supply may not exceed 300mV within a refresh interval (16ms).

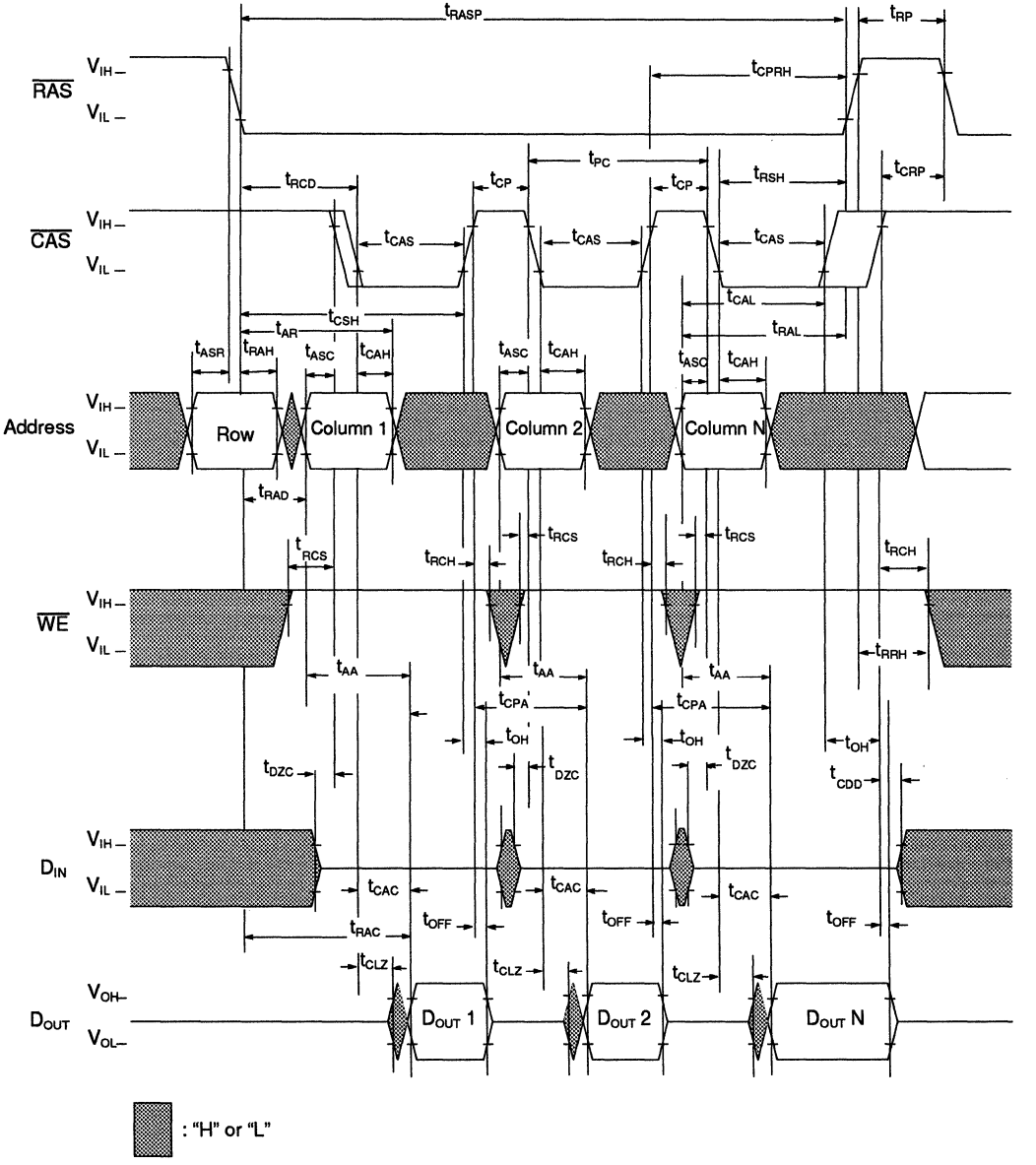
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

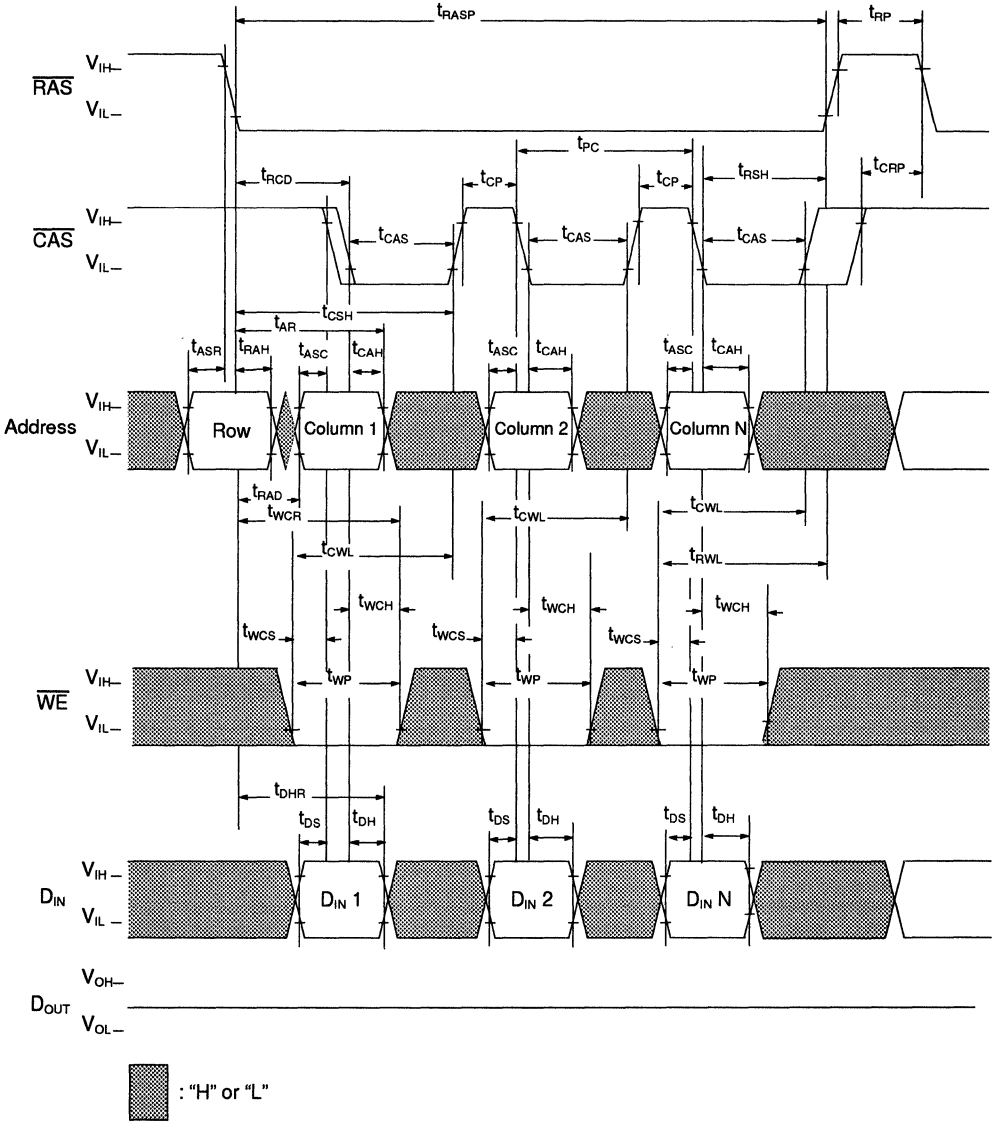
Write Cycle (Early Write)



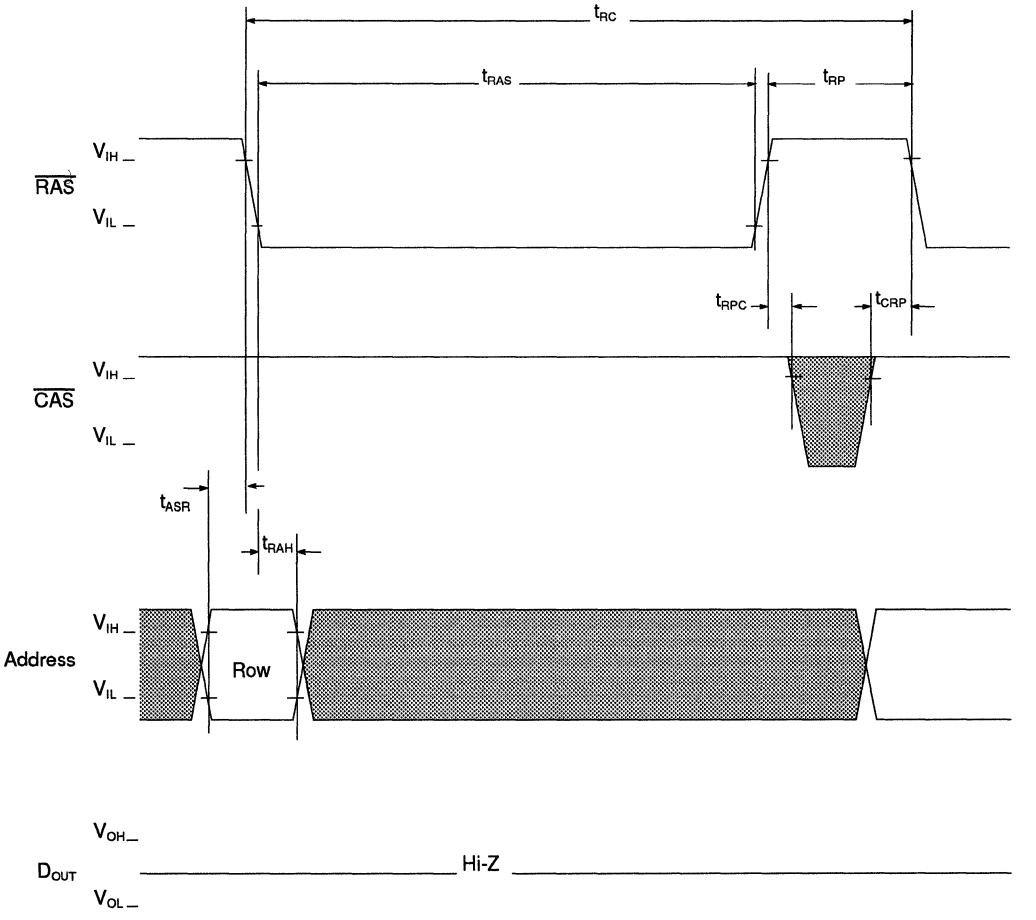
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



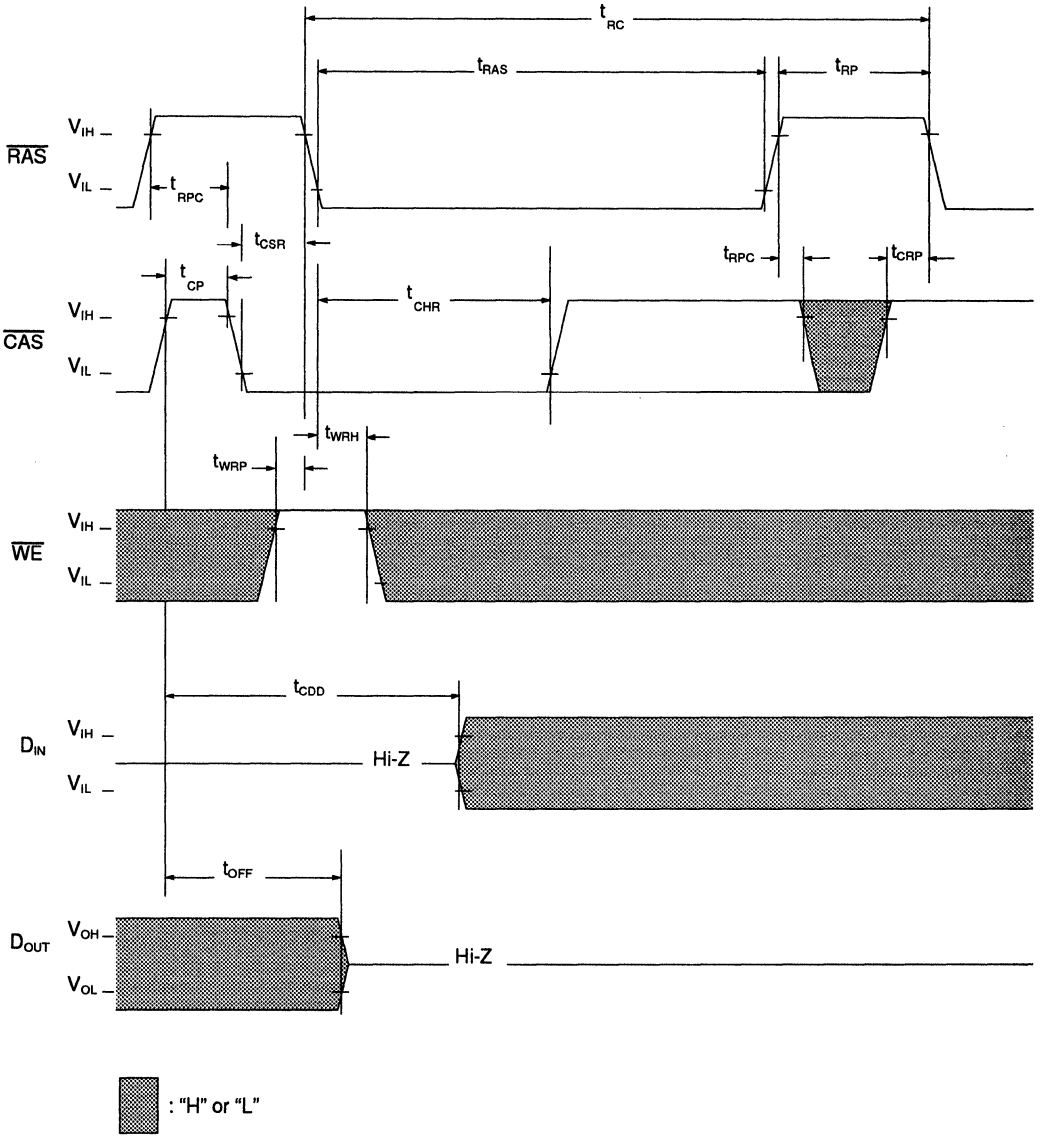
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

Note: $\overline{WE}$, D_{IN} are "H" or "L"

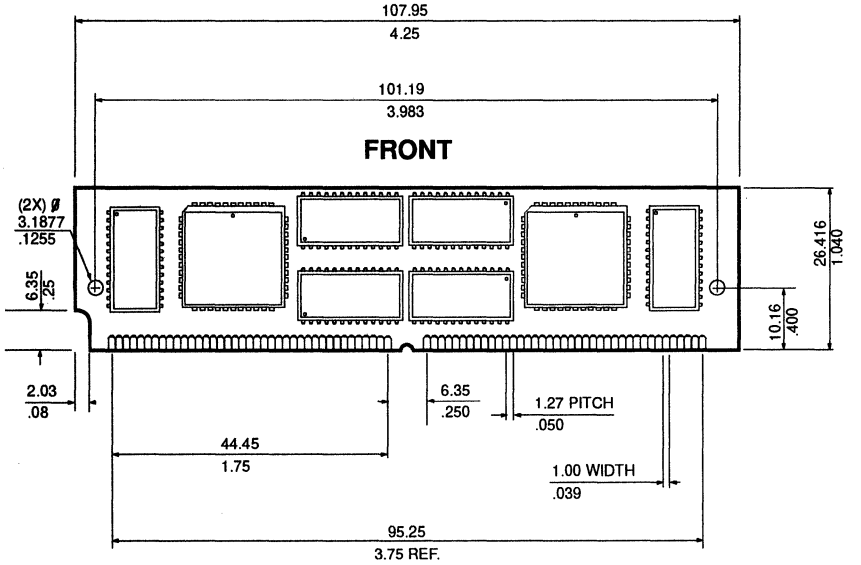
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



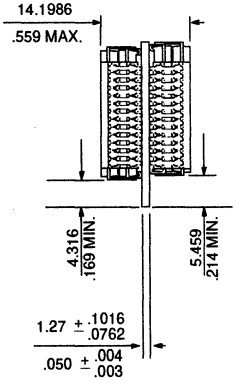
: "H" or "L"

Note: Addresses are "H" or "L"

Layout Drawing



SIDE



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

4M x 36 ECC-on-SIMM

Features

- 72-Pin JEDEC-Standard Single In-Line Memory Module
- Performance:

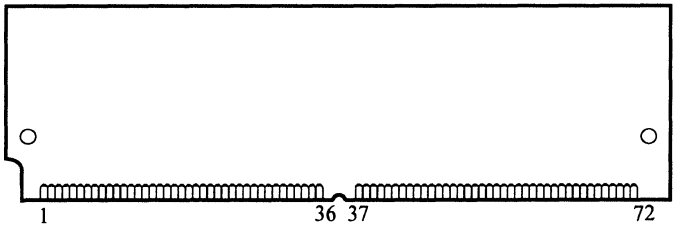
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{AA}	Access Time From Address	35ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Single-error-correct (SEC) high-speed ECC algorithm
- Single 5V ± 0.25V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 2048 refresh cycles distributed across 32ms
- 11/11 Addressing (Row/Column)
- Provides ECC and retrofits to standard x36 socket
- Au and Sn/Pb versions available

Description

The IBM11D4480BA is a 16MB industry standard 72-pin 4-byte single in-line memory module (SIMM) that has a fully functional, retrofittable and plug-compatible on-board error-correcting-code (ECC). The ECC function is completely self-contained and transparent to the system. The module is manufactured with 12 4M x 4 DRAMS and 4 ECC ASICs. The ECC-on-SIMM module corrects single-bit errors that may occur in any byte of SIMM data. It is recommended for systems that run critical applications but do not have native ECC. This family of SIMMs (1M x 36, 2M x 36, 4M x 36, and 8M x 36) provides the memory reliability required by these applications with no performance penalty. The outline varies per density.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

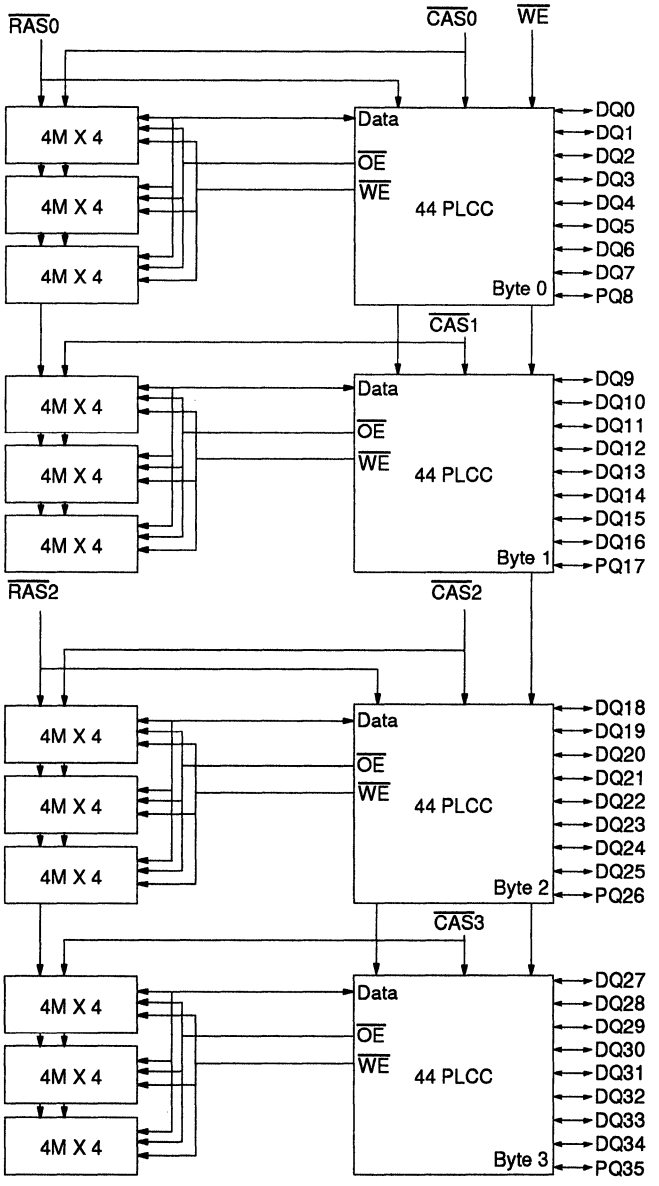
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	A10	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D4480BA-70	4M x 36	70ns	Sn/Pb	4.25" x 1.20" x .397"	
IBM11E4480BA-70	4M x 36	70ns	Au	4.25" x 1.20" x .397"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	Industry Standard -70
PD1	V_{SS}
PD2	NC
PD3	V_{SS}
PD4	NC

1. NC= OPEN, V_{SS} = GND.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.3 to 6.5	V	1
V_{IN}	Input Voltage	-0.3 to V_{CC} + 0.3	V	1
V_{OUT}	Output Voltage	-0.3 to V_{CC} + 0.3	V	1
T_C	Operating Temperature (Case)	0 to +65	°C	1
T_{STG}	Storage Temperature	-40 to +125	°C	1
P_D	Power Dissipation	12	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_C = 0 to 65°C)

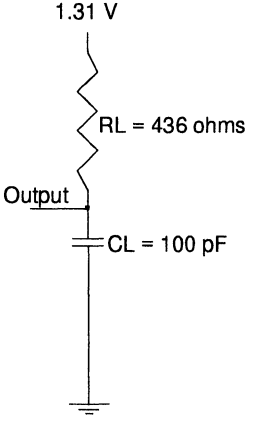
Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

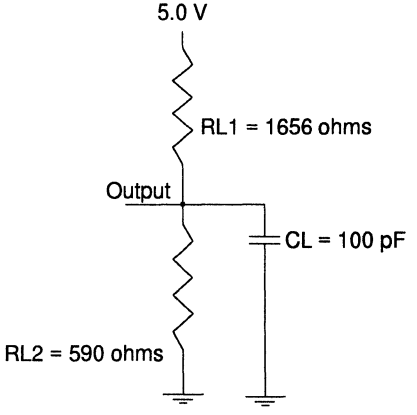
Capacitance (T_C = 0 to +65°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A10)	100	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	70	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	50	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	35	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	12	pF	
$C_{I/O2}$	Output Capacitance (PQ8, 17, 26, 35)	12	pF	

Load Diagram



LOAD CIRCUIT



ALTERNATE LOAD CIRCUIT

DC Electrical Characteristics (Tc = 0 to +65°C, V_{CC} = 5 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	1080	mA	1, 2, 3
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	24	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	1080	mA	1, 3
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	960	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	12	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	1080	mA	1, 3
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-460	+460	µA	
		$\overline{CAS}$, $\overline{WE}$	-40	+40		
		Address	-120	+120		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -4mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_C = 0 to +65°C, V_{CC} = 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 500ms is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	55	—	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	20	—	ns	

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	45	ns	1, 2

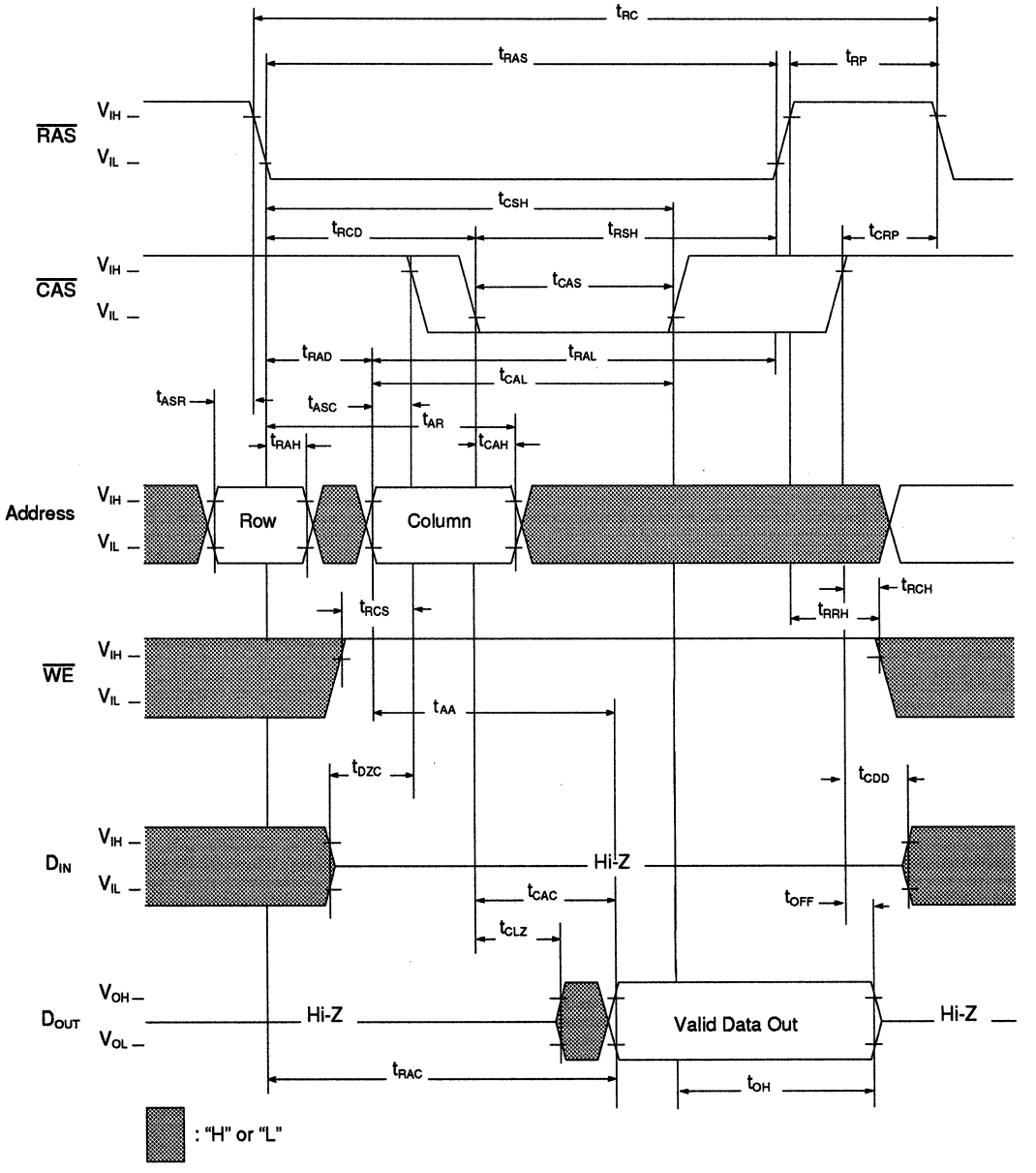
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	ns	
t_{REF}	Refresh Period	—	32	ms	1

1. 2048 refreshes are required every 32ms. The DC variation in the V_{CC} supply may not exceed 300mV within a refresh interval (32ms).

Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
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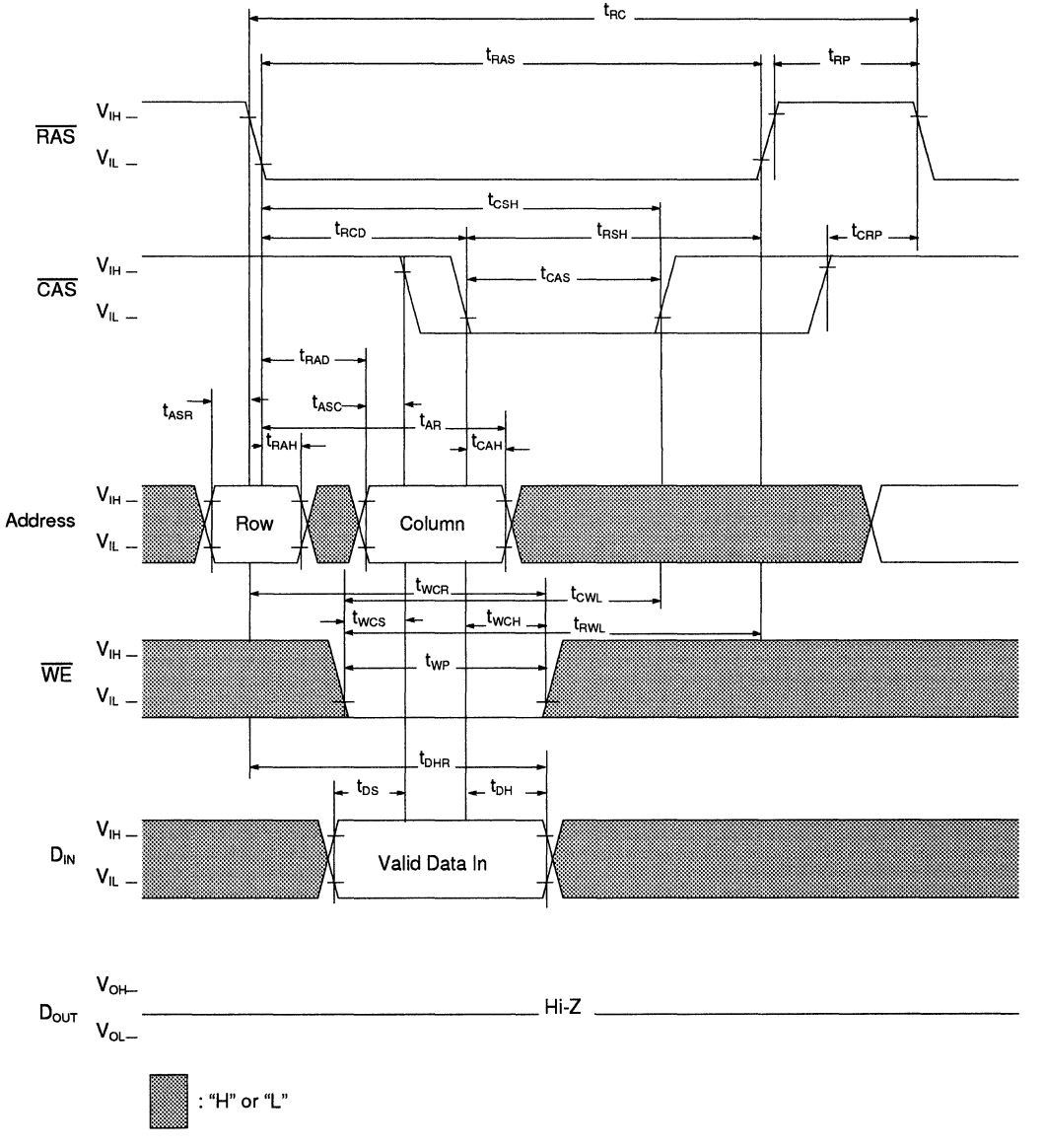
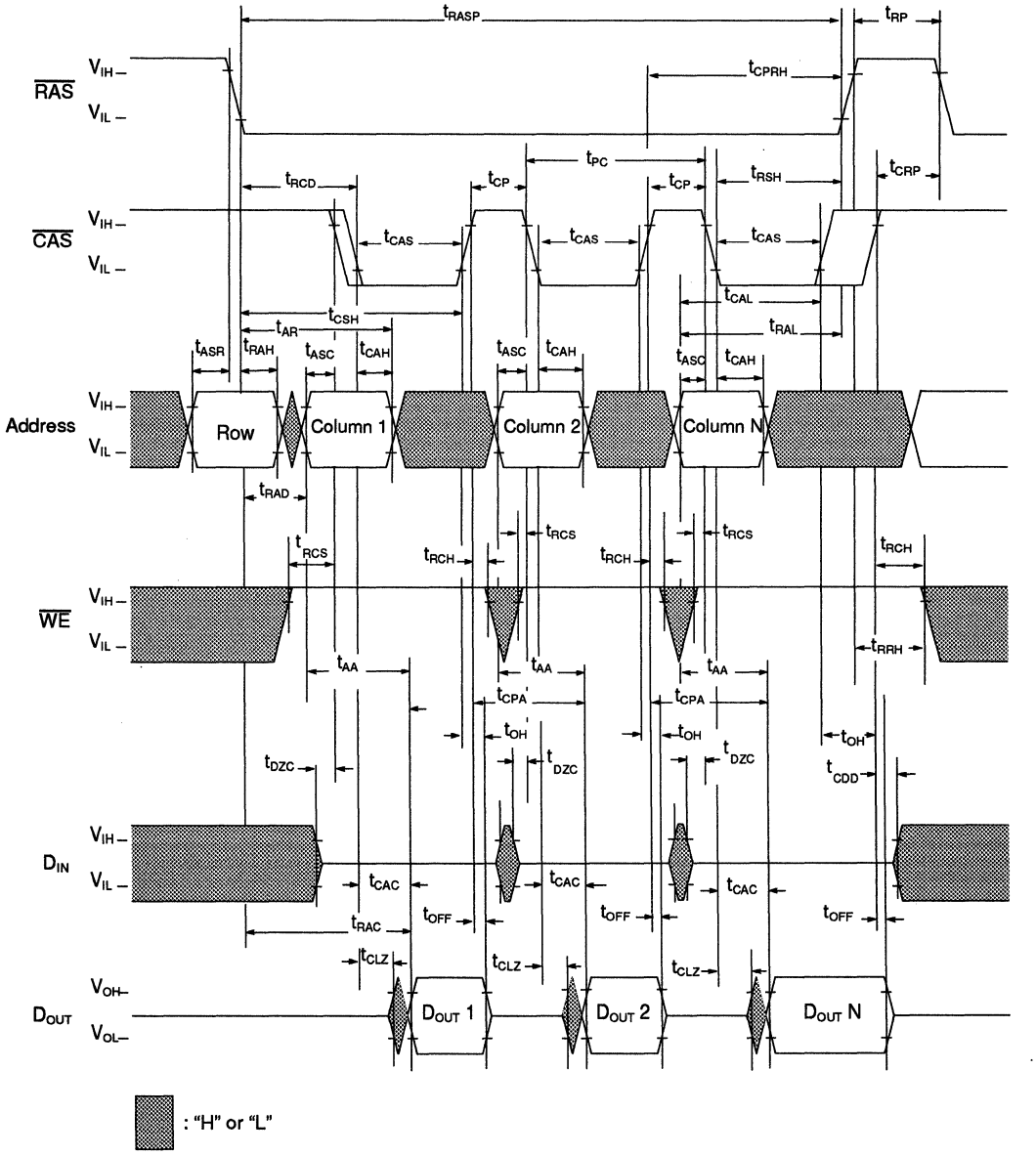
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRRH
tRCH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

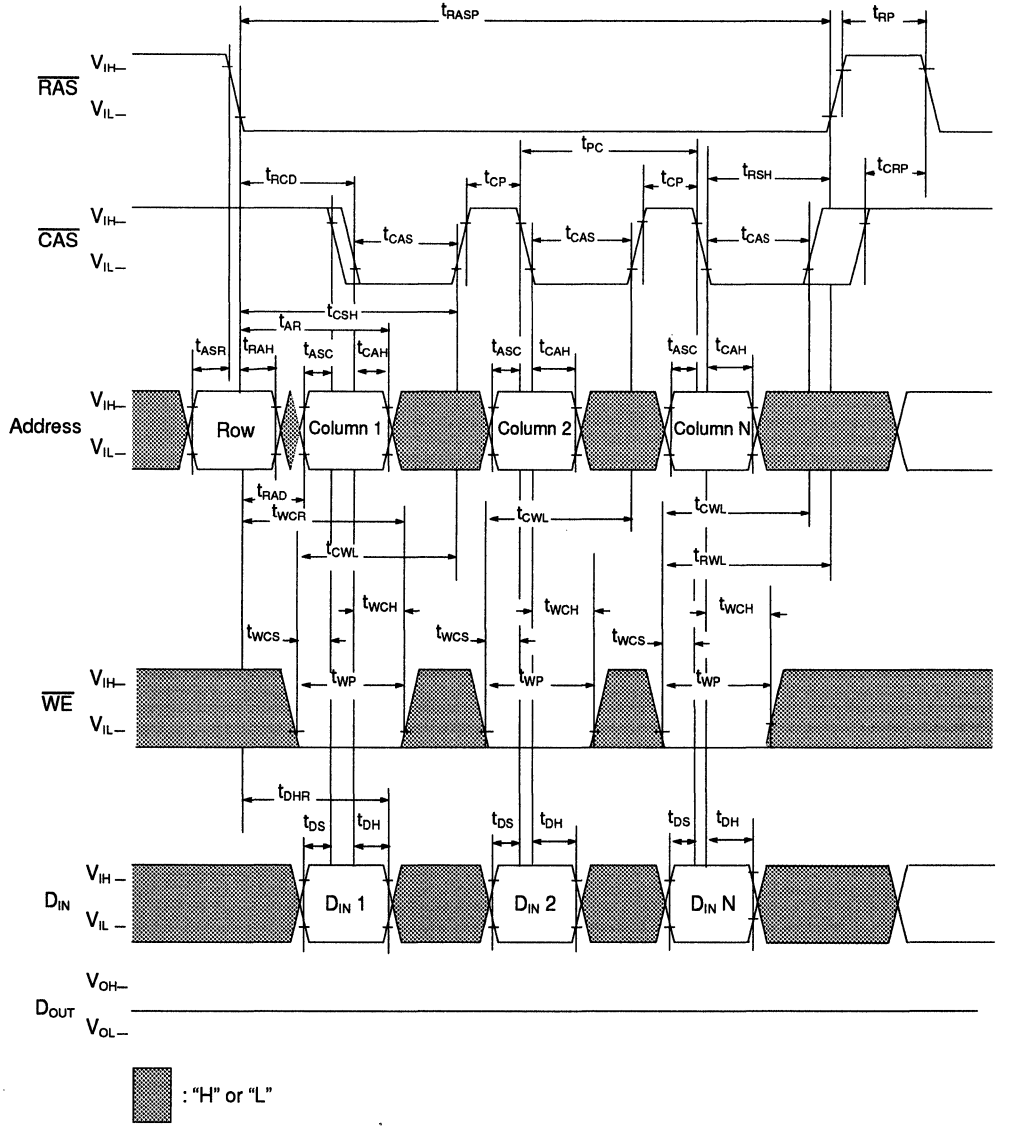
Write Cycle (Early Write)



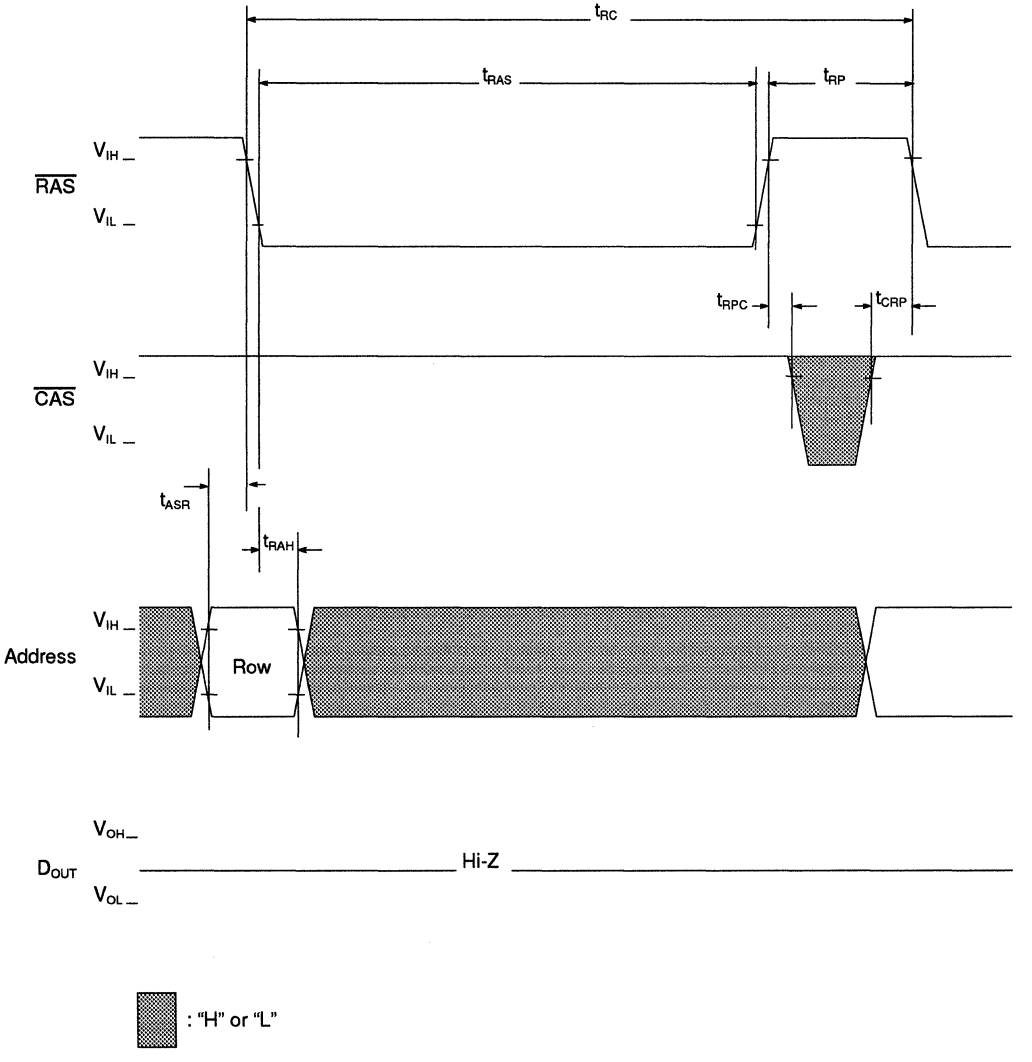
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

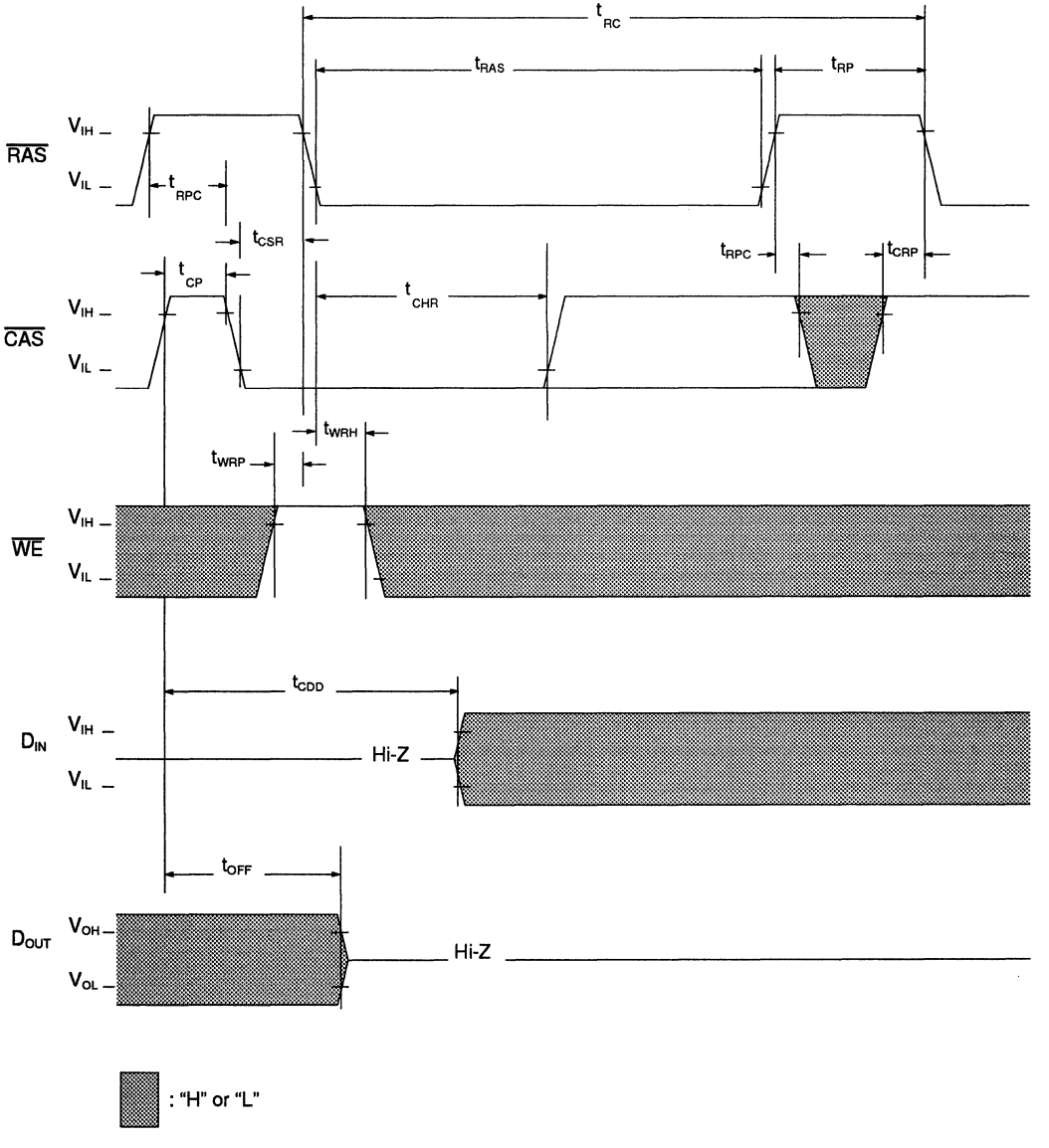


$\overline{RAS}$ Only Refresh Cycle



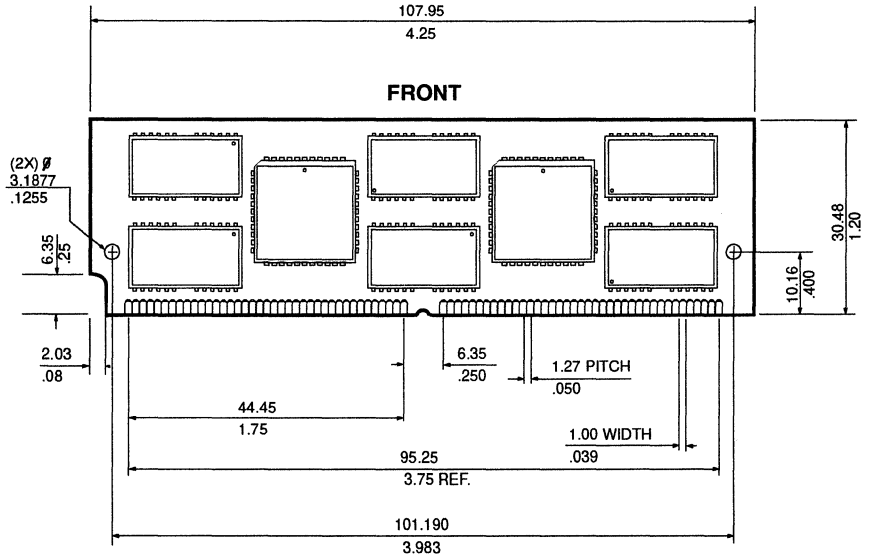
Note: $\overline{WE}$, D_{IN} are "H" or "L"

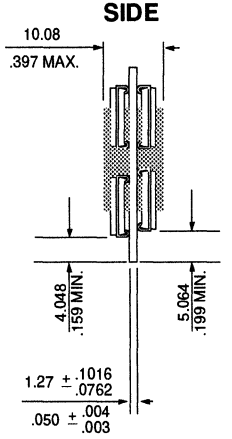
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

8M x 36 ECC-on-SIMM

Features

- 72-Pin JEDEC-Standard Single In-Line Memory Module
- Performance:

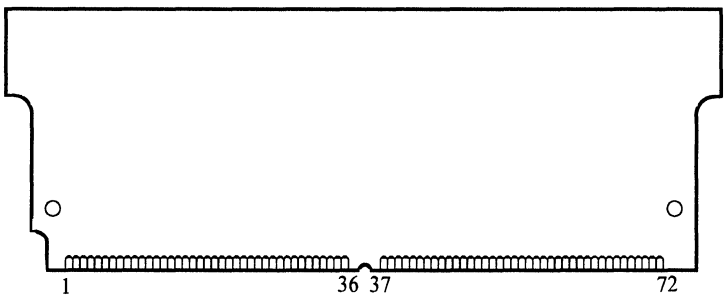
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{AA}	Access Time From Address	35ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Single-error-correct (SEC) high-speed ECC algorithm
- Single 5V ± 0.25V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 2048 refresh cycles distributed across 32ms
- 11/11 Addressing (Row/Column)
- Provides ECC and retrofits to standard x36 socket
- Au and Sn/Pb versions available

Description

The IBM11D8480BA is a 32MB industry standard 72-pin 4-byte single in-line memory module (SIMM) that has a fully functional, retrofittable and plug-compatible on-board error-correcting-code (ECC). The ECC function is completely self-contained and transparent to the system. The module is manufactured with 24 4M x 4 DRAMS and 4 ECC ASICs. The ECC-on-SIMM module corrects single-bit errors that may occur in any byte of SIMM data. It is recommended for systems that run critical applications but do not have native ECC. This family of SIMMs (1M x 36, 2M x 36, 4M x 36, and 8M x 36) provides the memory reliability required by these applications with no performance penalty. The outline varies per density.

Card Outline



Pin Description

$\overline{RAS0}$-$\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

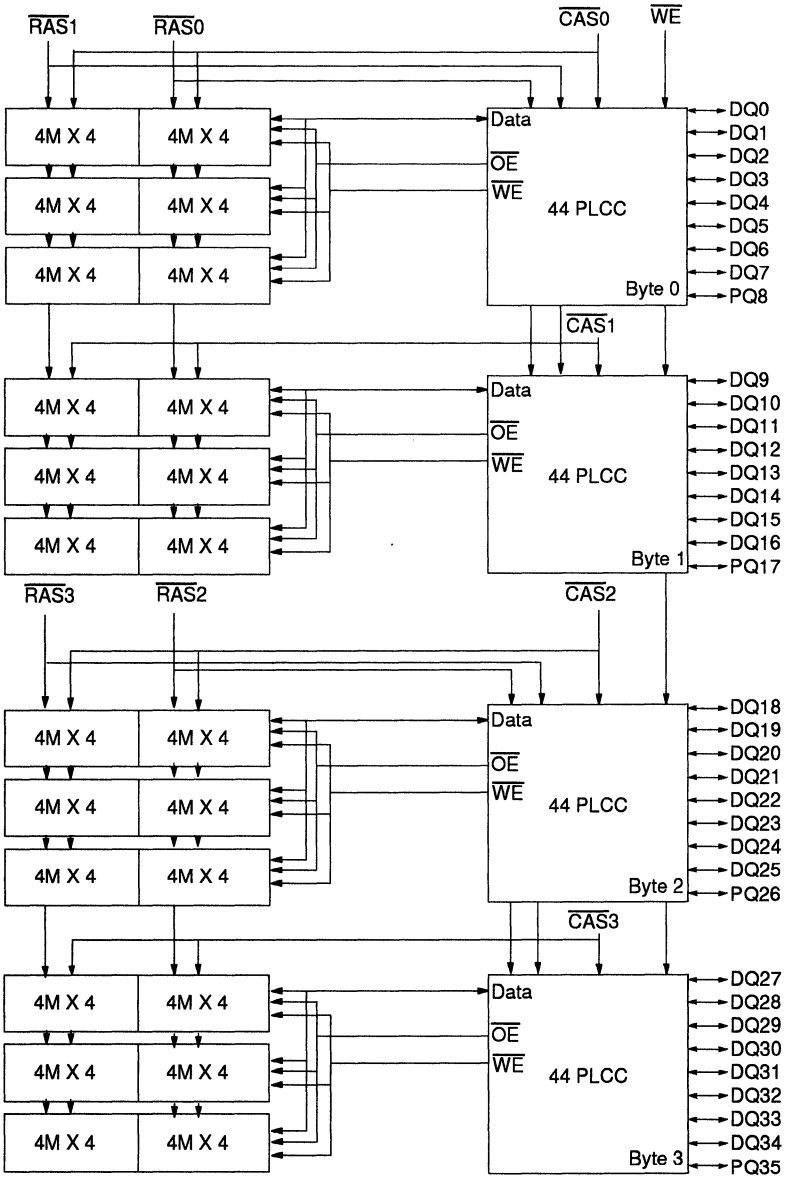
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	A10	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D8480BA-70	8M x 36	70ns	Sn/Pb	4.25" x 1.67" x .397"	
IBM11E8480BA-70	8M x 36	70ns	Au	4.25" x 1.67" x .397"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	Industry Standard -70
PD1	NC
PD2	Vss
PD3	V_{SS}
PD4	NC
1. NC= OPEN, V_{SS} = GND.	

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.3 to 6.5	V	1
V_{IN}	Input Voltage	-0.3 to V_{CC} + 0.3	V	1
V_{OUT}	Output Voltage	-0.3 to V_{CC} + 0.3	V	1
T_C	Operating Temperature (Case)	0 to +65	°C	1
T_{STG}	Storage Temperature	-40 to +125	°C	1
P_D	Power Dissipation	24	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_C = 0 to 65°C)

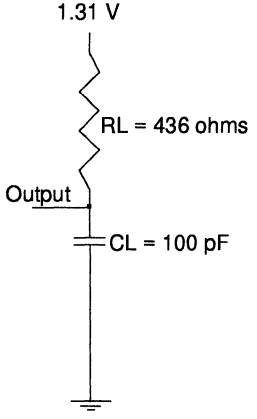
Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

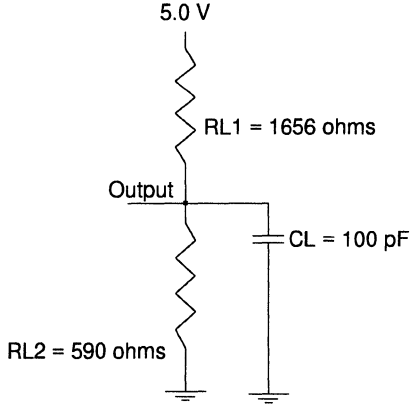
Capacitance (T_C = 0 to +65°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A10)	150	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	70	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	70	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	35	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	12	pF	
$C_{I/O2}$	Output Capacitance (PQ8, 17, 26, 35)	12	pF	

Load Diagram



LOAD CIRCUIT



ALTERNATE LOAD CIRCUIT

DC Electrical Characteristics (Tc = 0 to +65°C, V_{CC} = 5 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	1104	mA	1, 2, 3
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	48	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	1104	mA	1, 3, 4
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	984	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	24	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	1104	mA	1, 3, 4
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-460	+460	µA	
		$\overline{CAS}$, $\overline{WE}$	-70	+70		
		Address	-240	+240		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -4mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. When refreshing both banks at once, the refresh current becomes 2160mA.

AC Characteristics (T_C = 0 to +65°C, V_{CC} = 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 500ms is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	55	—	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	20	—	ns	

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	45	ns	1, 2

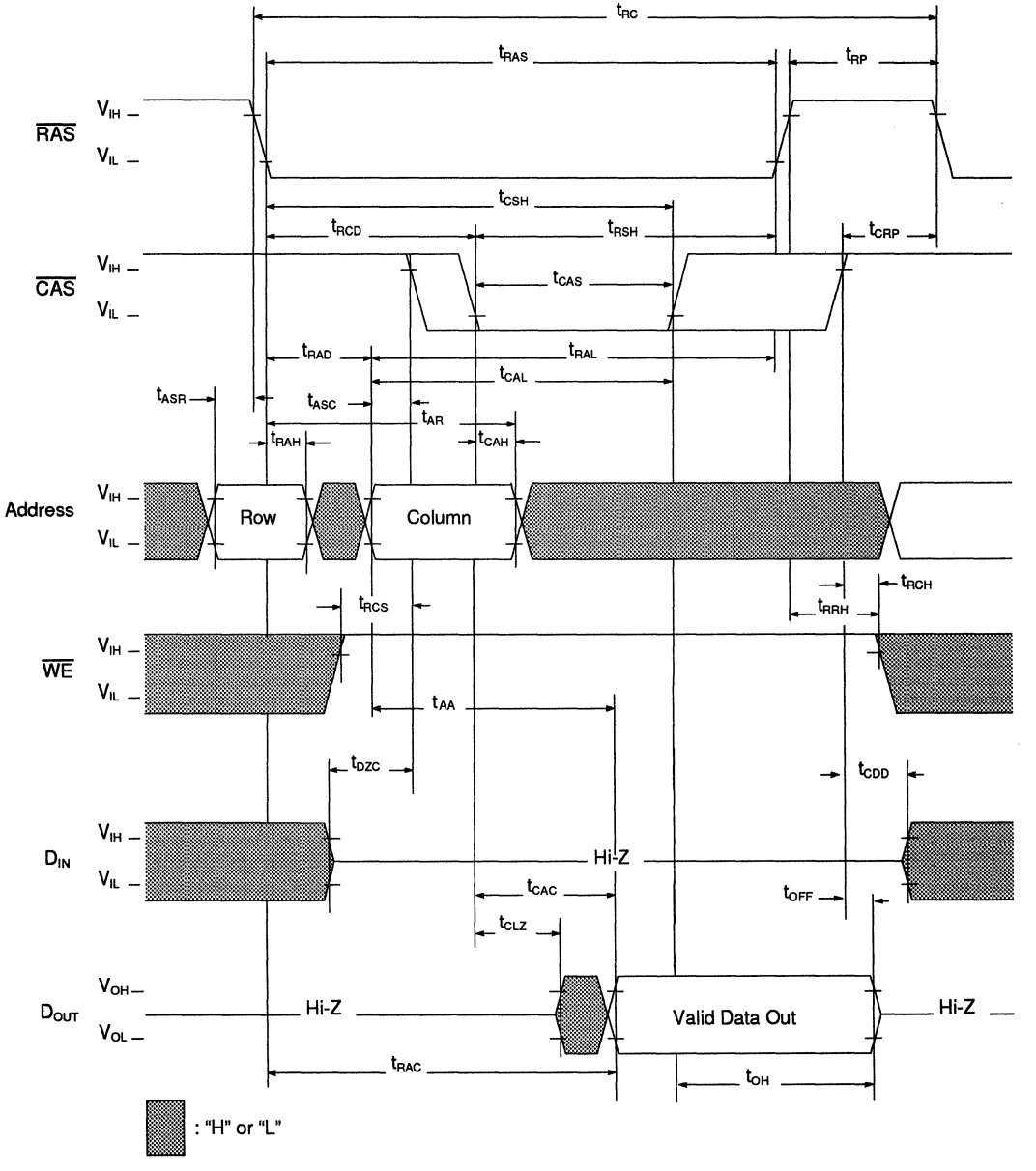
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

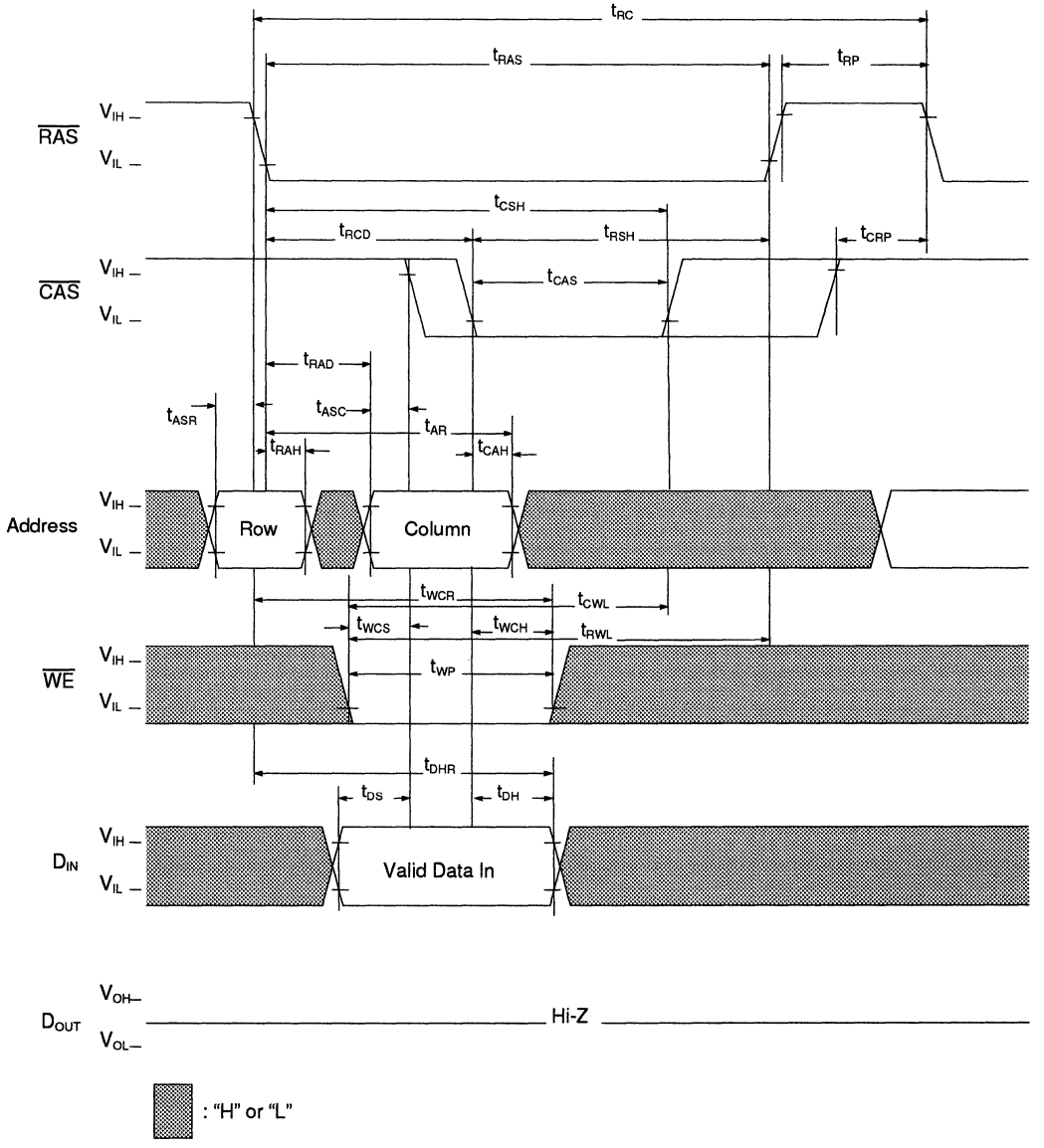
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	ns	
t_{REF}	Refresh Period	—	32	ms	1

1. 2048 refreshes are required every 32ms. The DC variation in the V_{CC} supply may not exceed 300mV within a refresh interval (32ms).

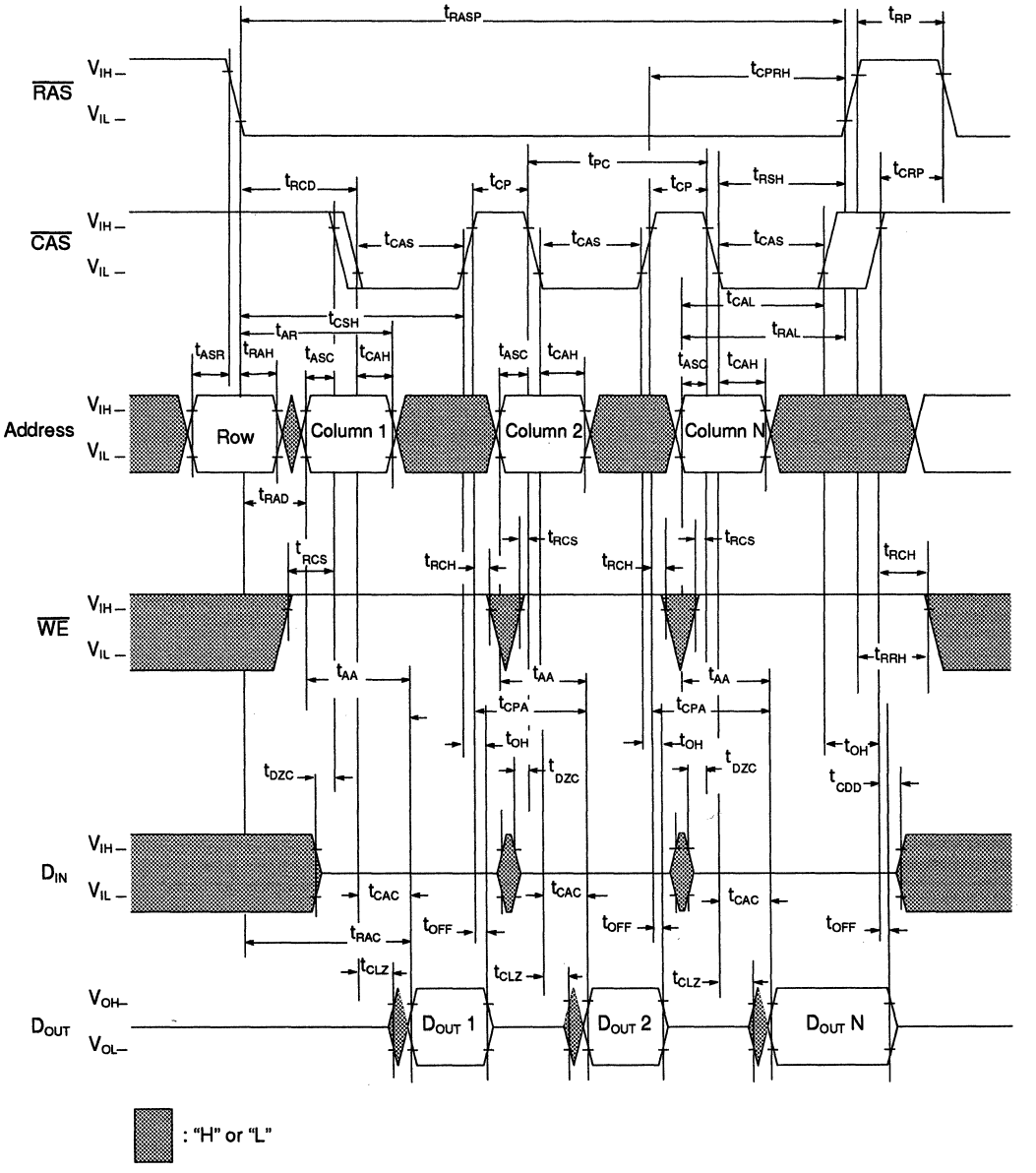
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Valid Data Out
tRAC
tOH
: "H" or "L"

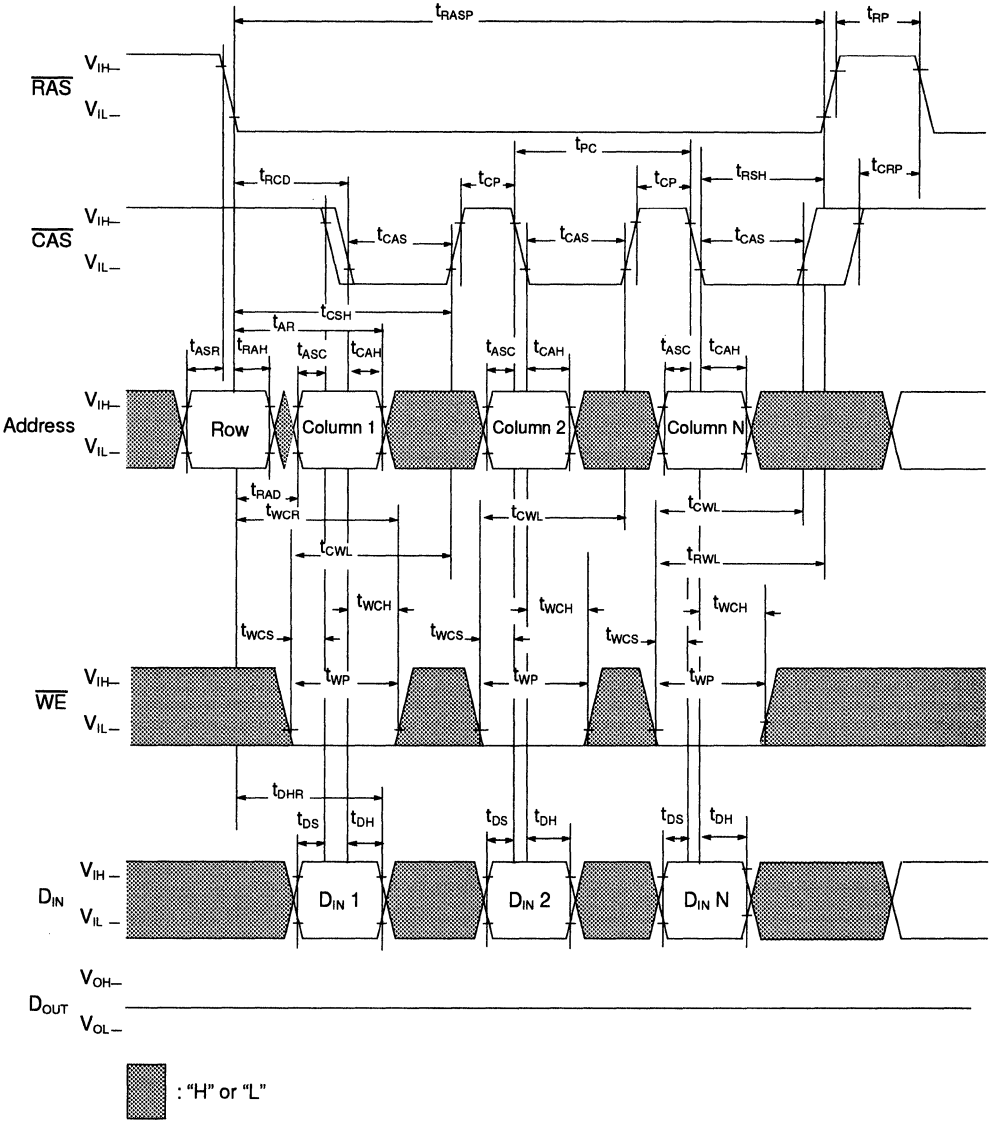
Write Cycle (Early Write)



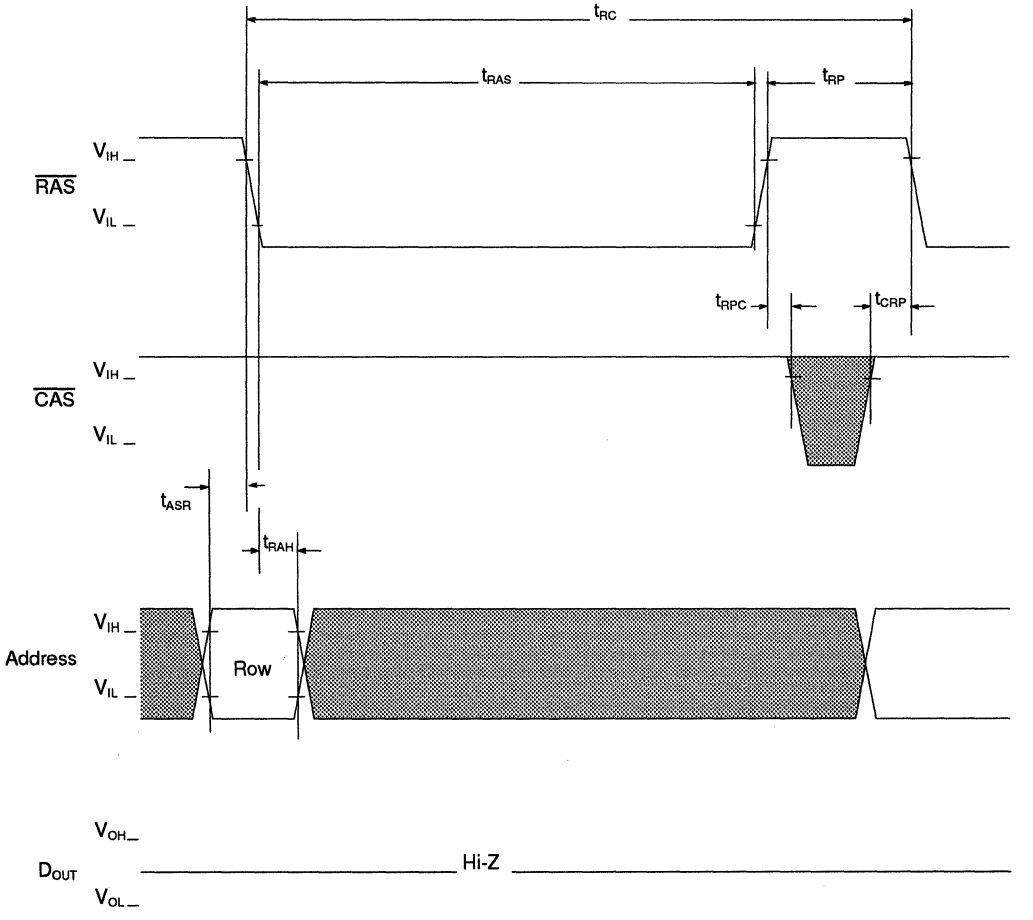
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



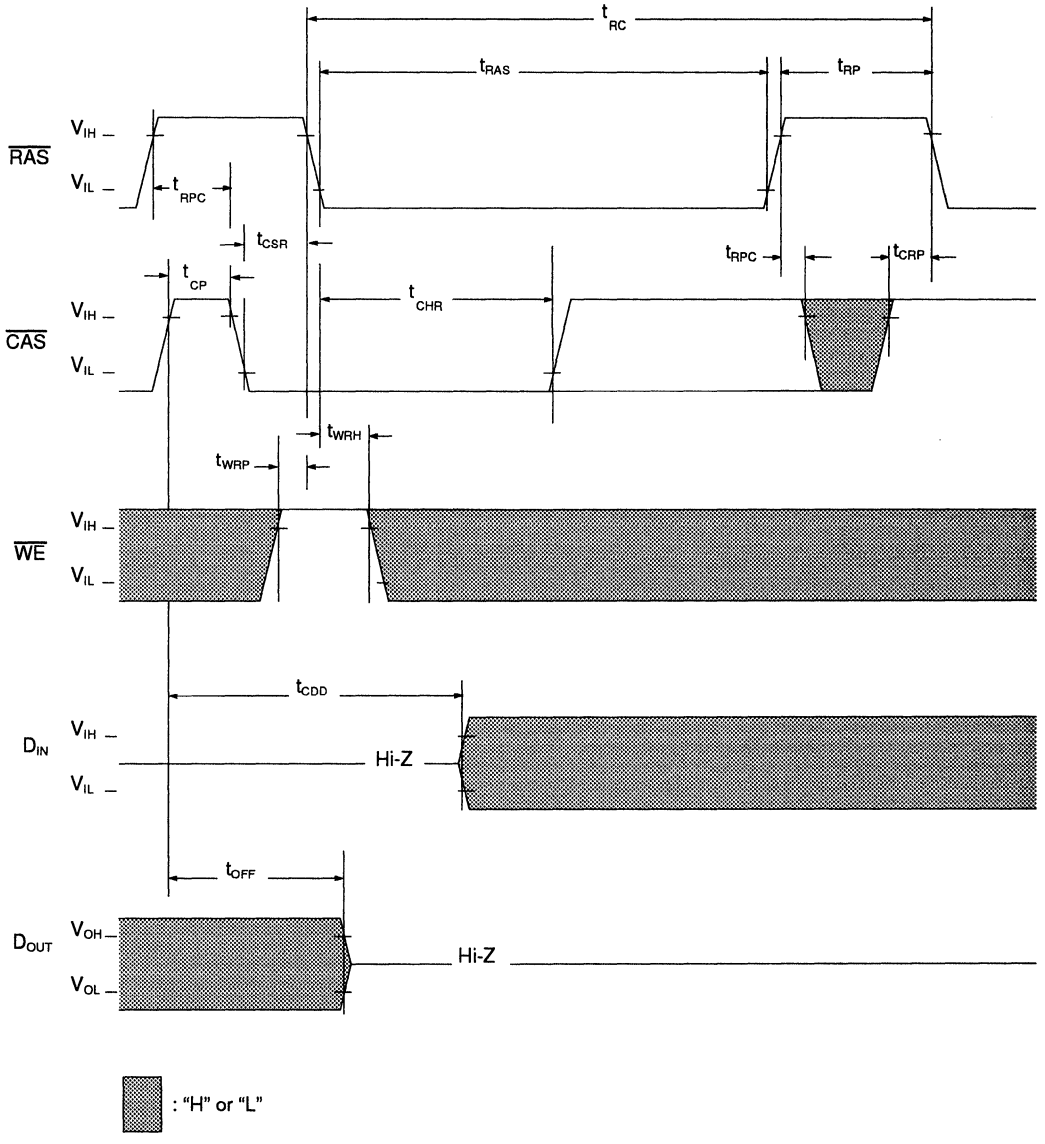
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

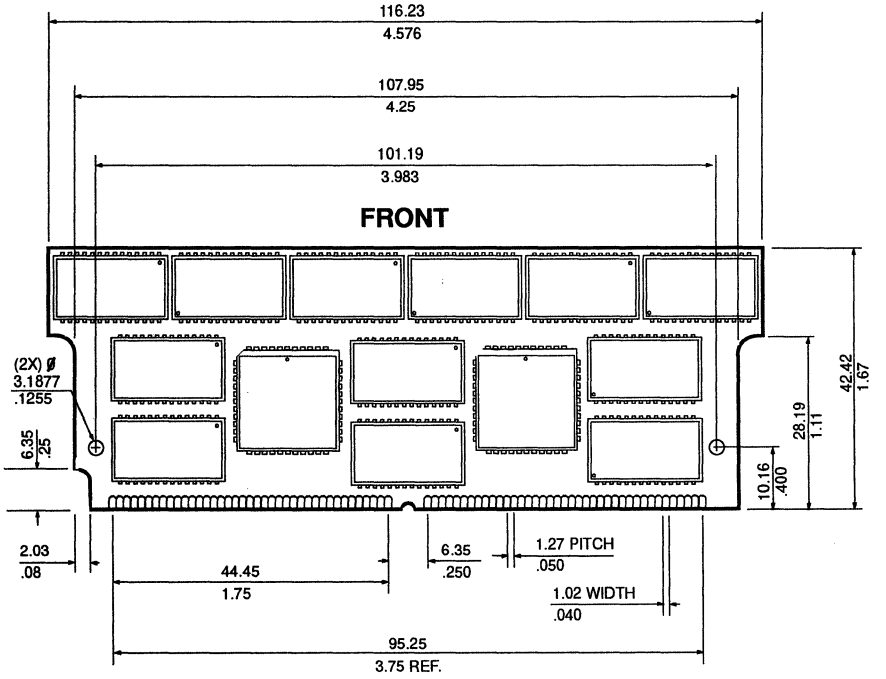
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

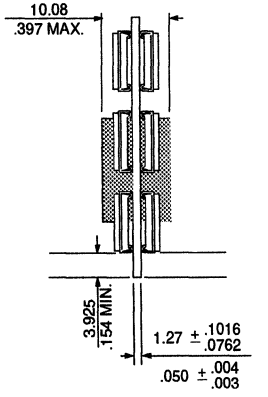


Note: Addresses are "H" or "L"

Layout Drawing



SIDE



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

168 Pin DIMMs

- Parity

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 1Mx64 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are fully TTL and CMOS compatible
- Single 5V, ± 0.5V Power Supply
- Au contacts
- Optimized for byte-write non-parity applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - 4 Byte Interleave enabled
  - Byte write, byte read accesses
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 addressing (Row/Column)
- Card size: 5.25" x 1.0" x 0.354"
- DRAMS in SOJ Package

Description

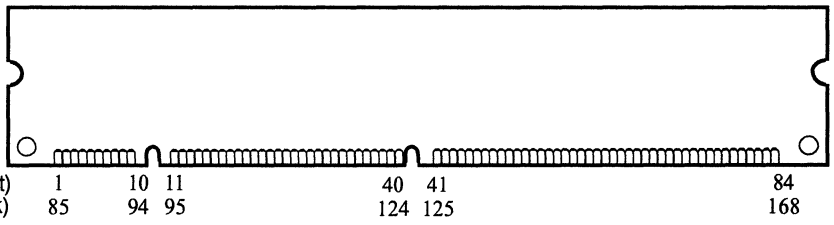
IBM11M1640BA is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 1Mx64 high speed memory array for non-parity applications. The DIMM uses 16 1Mx4 DRAMs in SOJ packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, if a x64 parity DIMM were inserted into a bank of x72 parity DIMMs, ID0 (grounded) would indicate that at least one DIMM in that memory bank is x64, and if the memory controller is designed to do so, all DIMMs in that memory bank will function as x64s.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x72 parity (5V) and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A9	Address Inputs (Buffered)
DQx	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

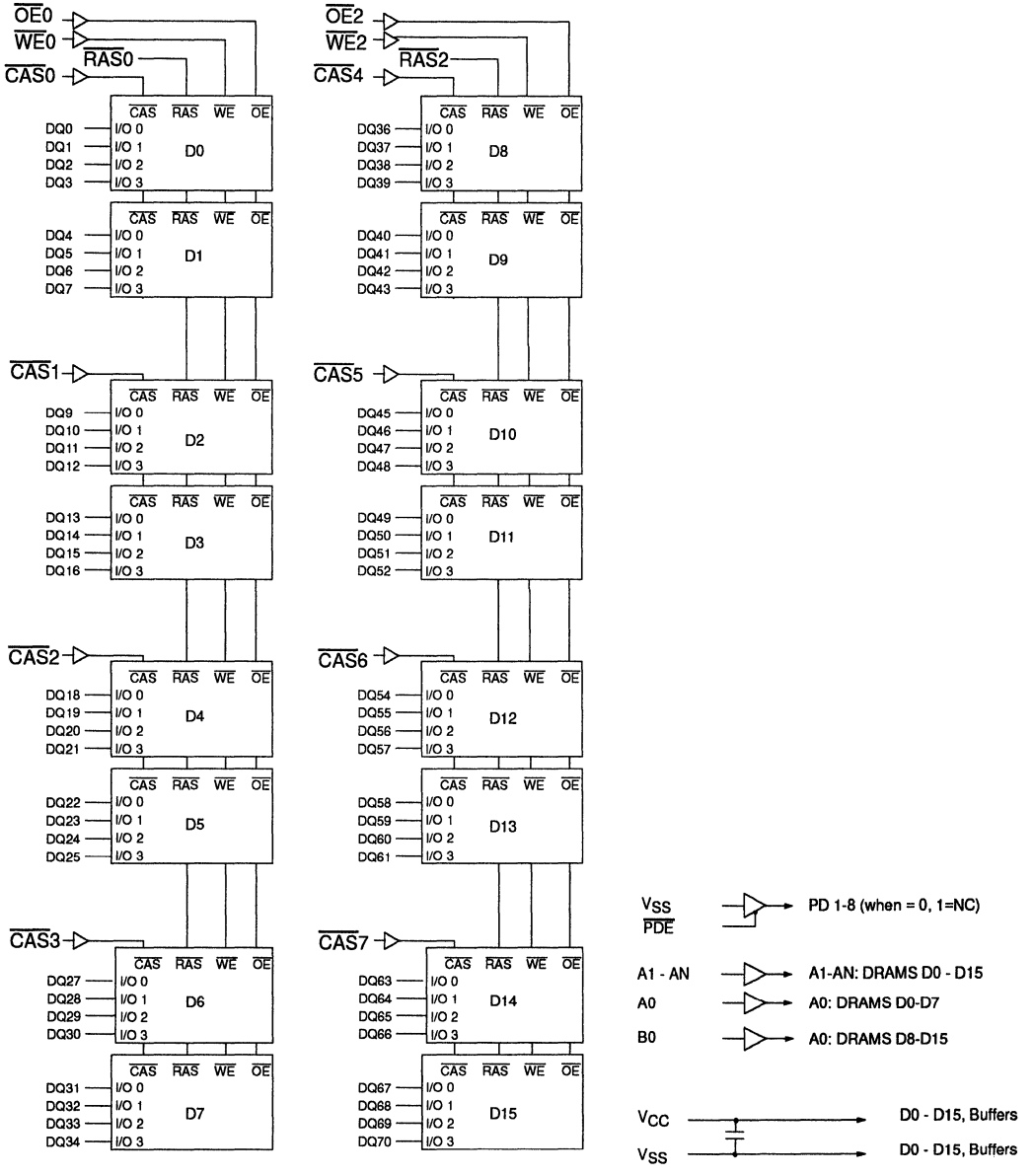
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	NC
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	$\overline{CAS5}$
5	DQ3	89	DQ39	47	$\overline{CAS6}$	131	$\overline{CAS7}$
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	NC	95	NC	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	NC	106	NC	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	NC	150	NC
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	$\overline{CAS1}$	70	DQ29	154	DQ65
29	$\overline{CAS2}$	113	$\overline{CAS3}$	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	NC	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	NC	161	NC
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	NC	122	NC	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M1640BA-60	1Mx64	60ns	Au	5.25"x1.0"x 0.354"	
IBM11M1640BA-70	1Mx64	70ns	Au	5.25"x1.0"x 0.354"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	0	0
PD2	0	0
PD3	1	1
PD4	0	0
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	1	1
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 6.5	V	1
V_{IN}	Input Voltage	-0.7 to V_{CC} +0.7	V	1
V_{OUT}	Output Voltage	-0.7 to V_{CC} +0.7	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	10.6	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to Vss.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ±0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A9)	13	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	60	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF	
C_{I4}	DQ_X Capacitance	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1920	mA	1,2,3
		-70	—	1728		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	32	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1920	mA	1,3
		-70	—	1728		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1200	mA	1,2,3
		-70	—	1120		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	32	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1920	mA	1,3
		-70	—	1728		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-80	+80		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1},I_{CC3},I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1},I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. The 1Mx4 DRAM outputs will remain disabled until these 8 cycles have occurred. This prevents data contention (excessive current) during power on. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the DRAM device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	1
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	4
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	57	—	62	—	—	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
2. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	2	—	ns	1
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	3
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	36	—	41	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	15	—	15	—	ns	
t_{OH}	Output Data Hold Time	2	—	2	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	2, 3

1. This timing parameter is not applicable to this product, but applies to a related product in this family.
2. Measured with the specified current load and 100pF.
3. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

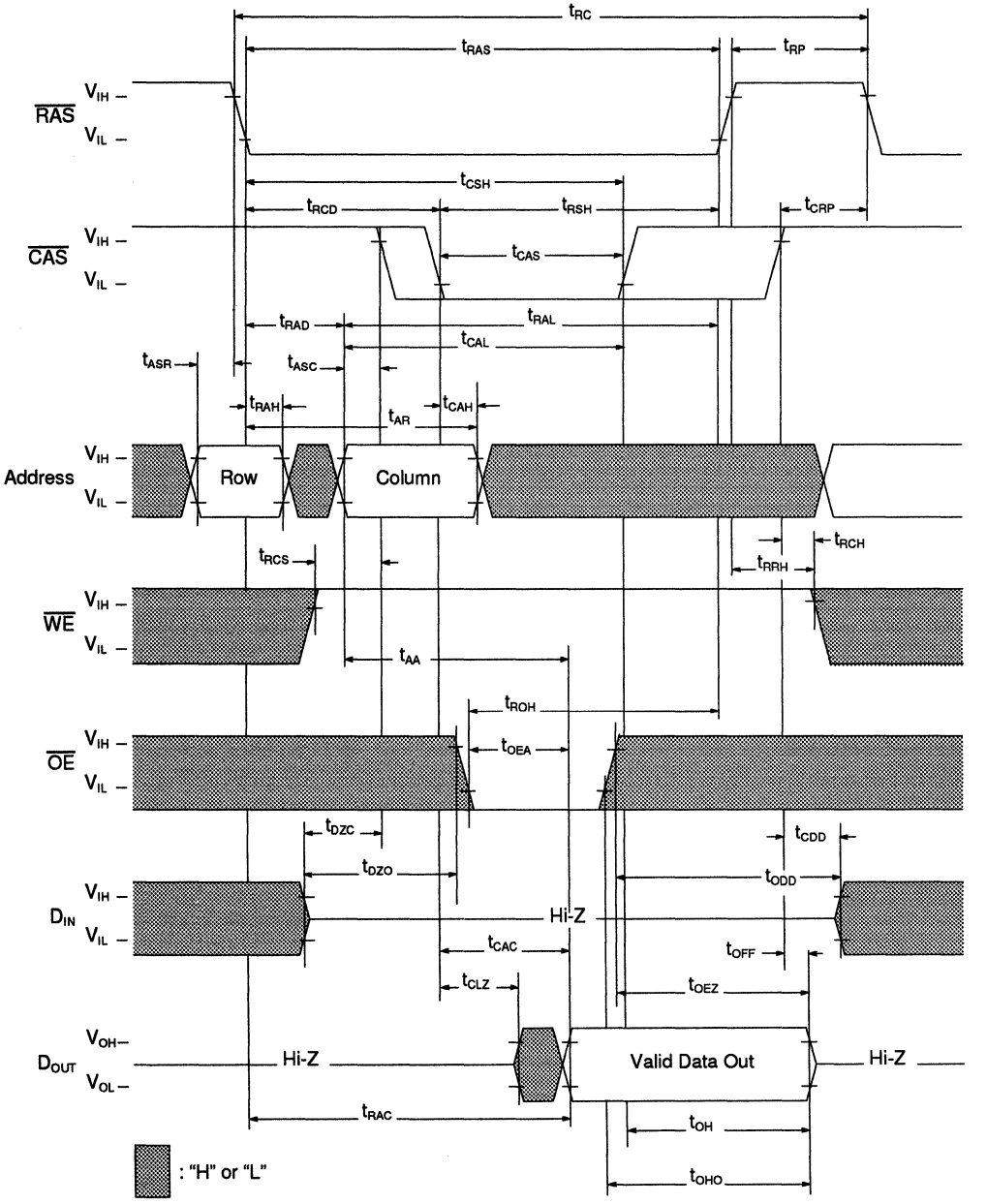
1. 1024 refreshes are required every 16ms.

Presence Detect Read Cycle

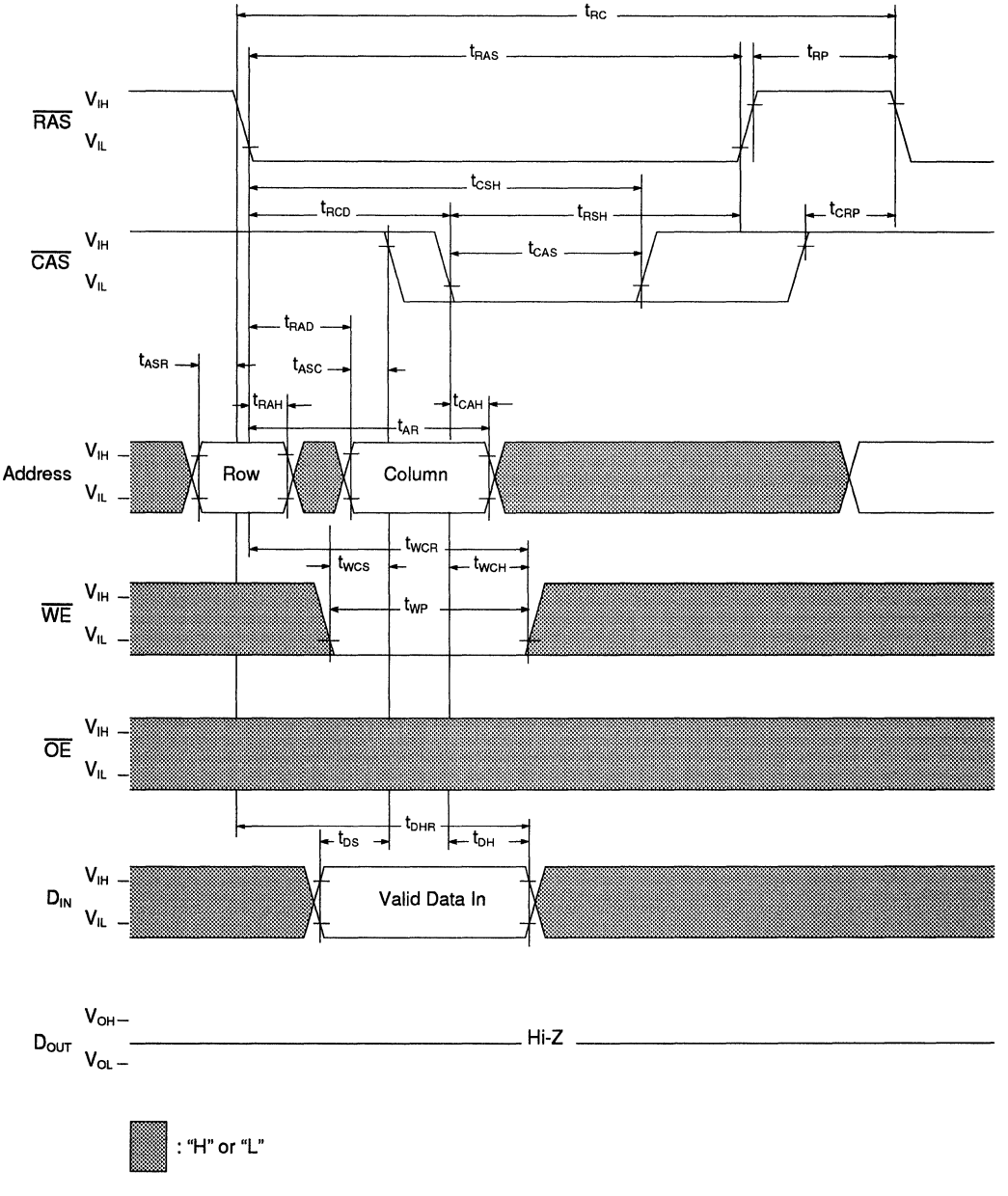
Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

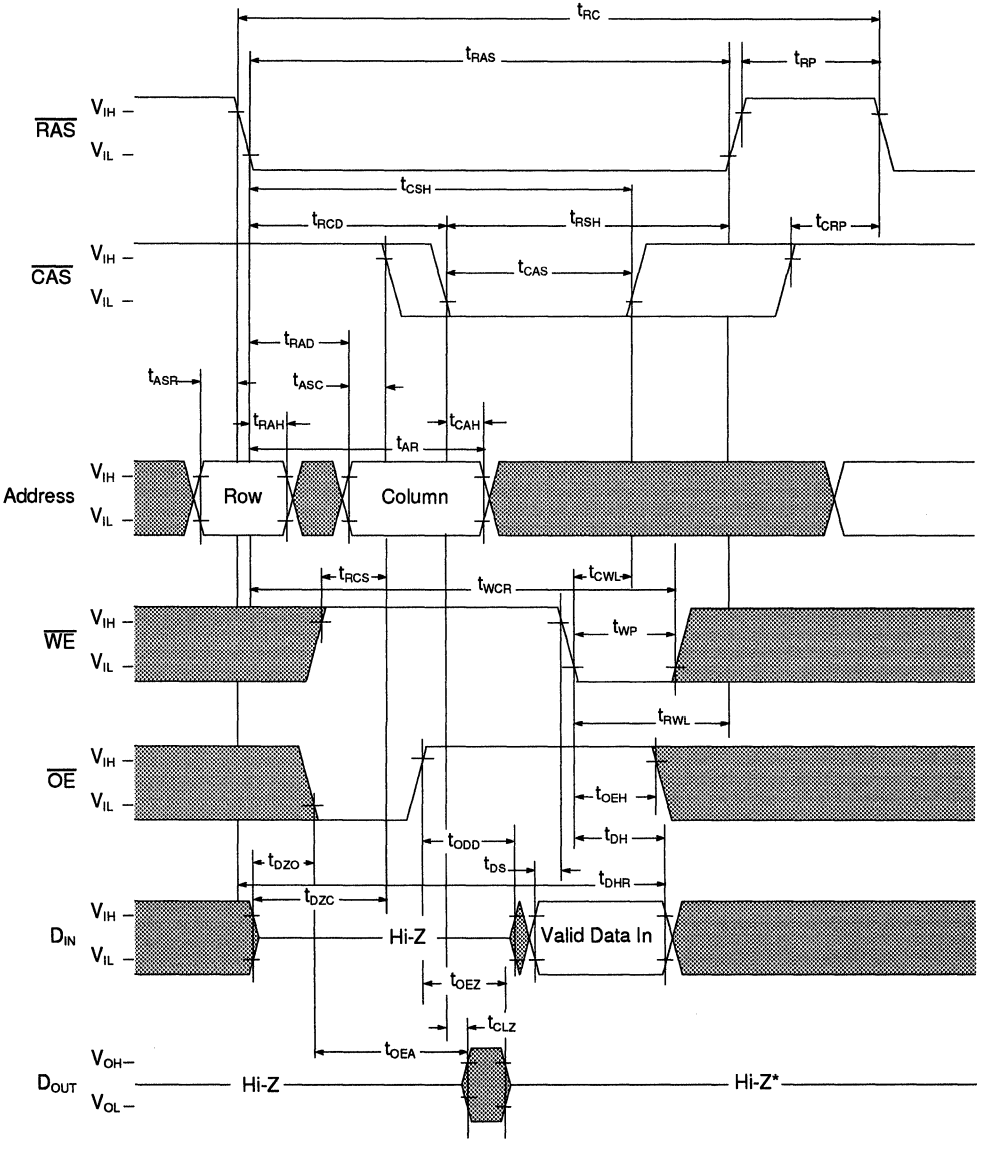
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tCAH
tAR
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tCDD
tDZO
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Valid Data Out
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

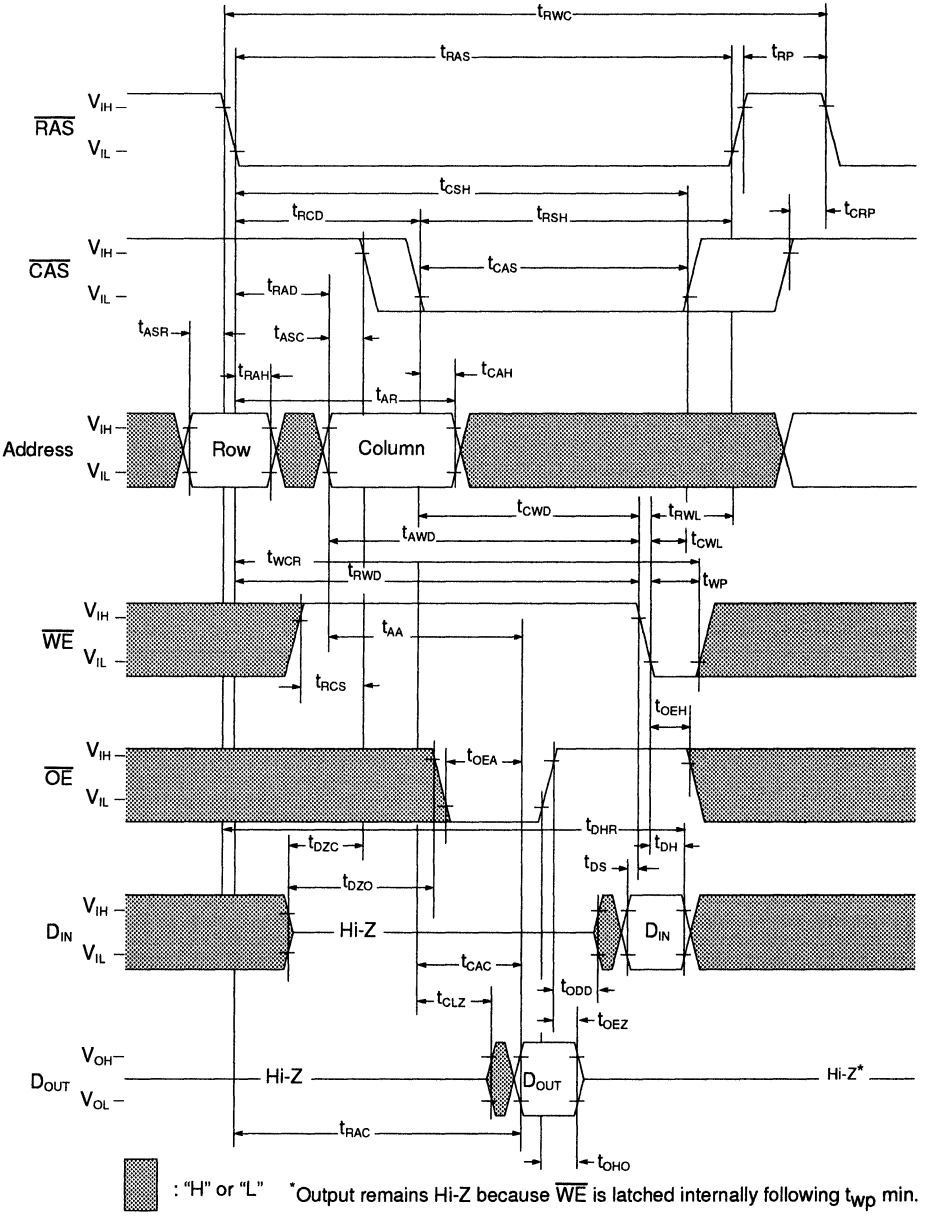


Write Cycle (Late Write)

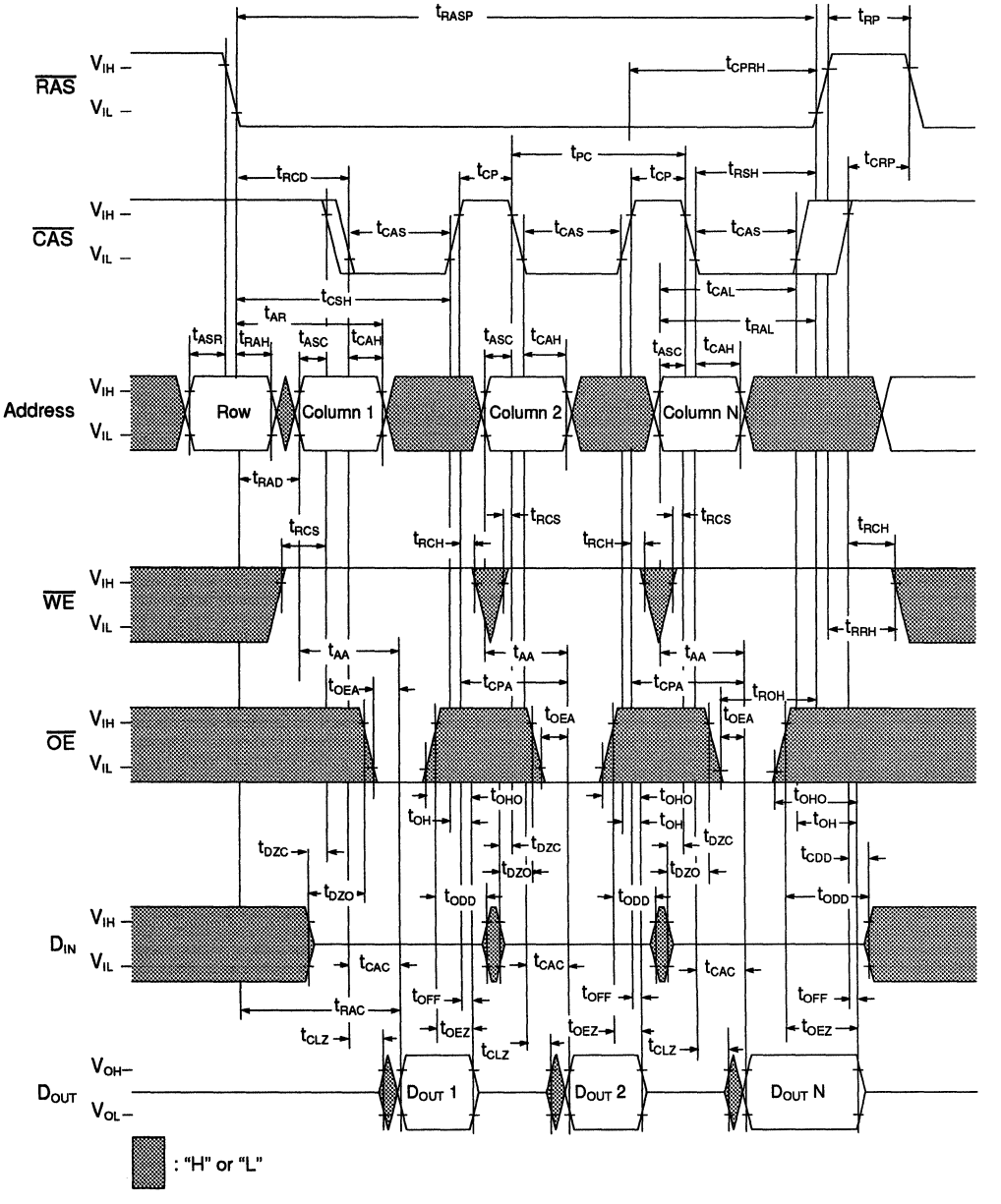


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

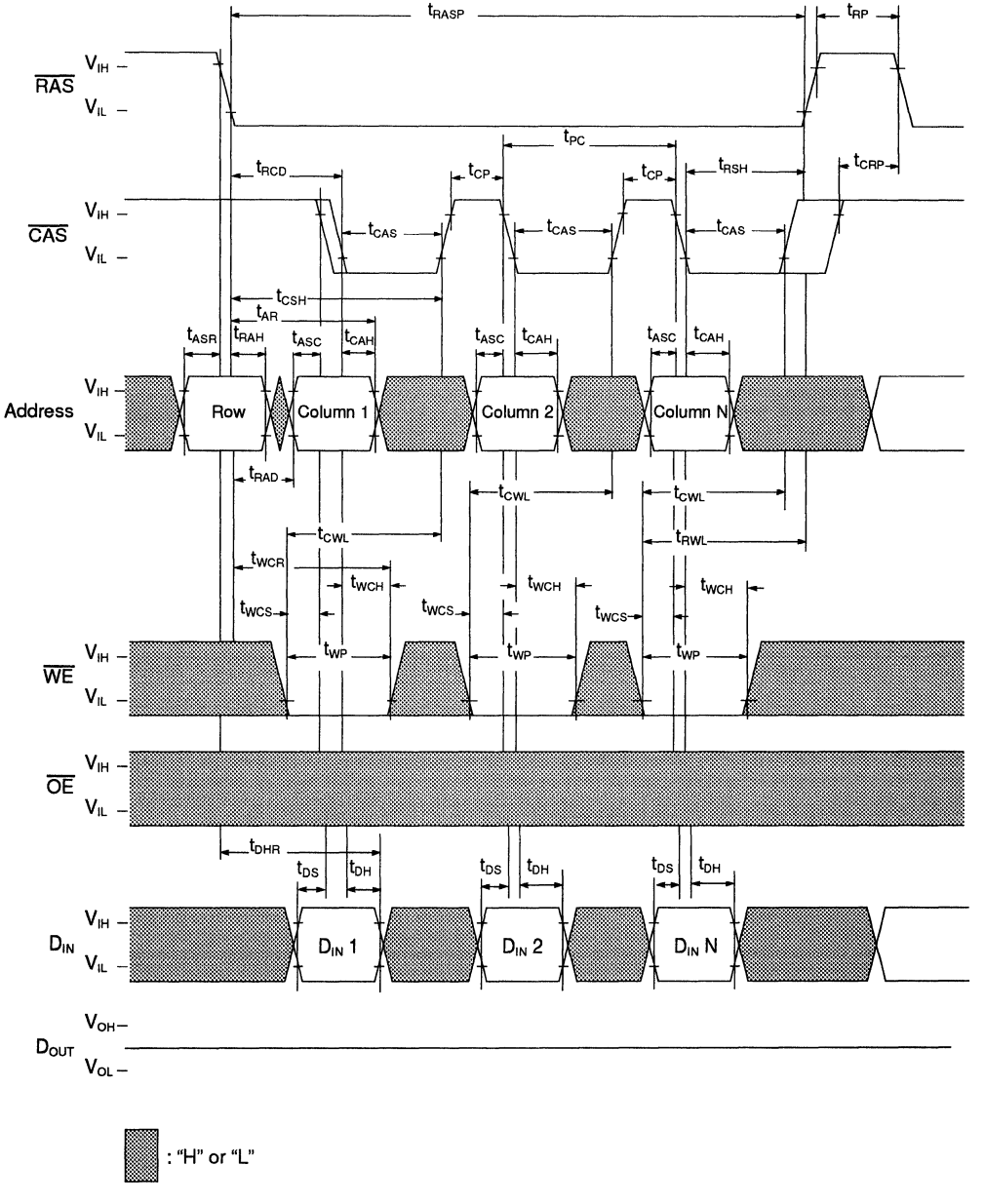
Read-Modify-Write-Cycle



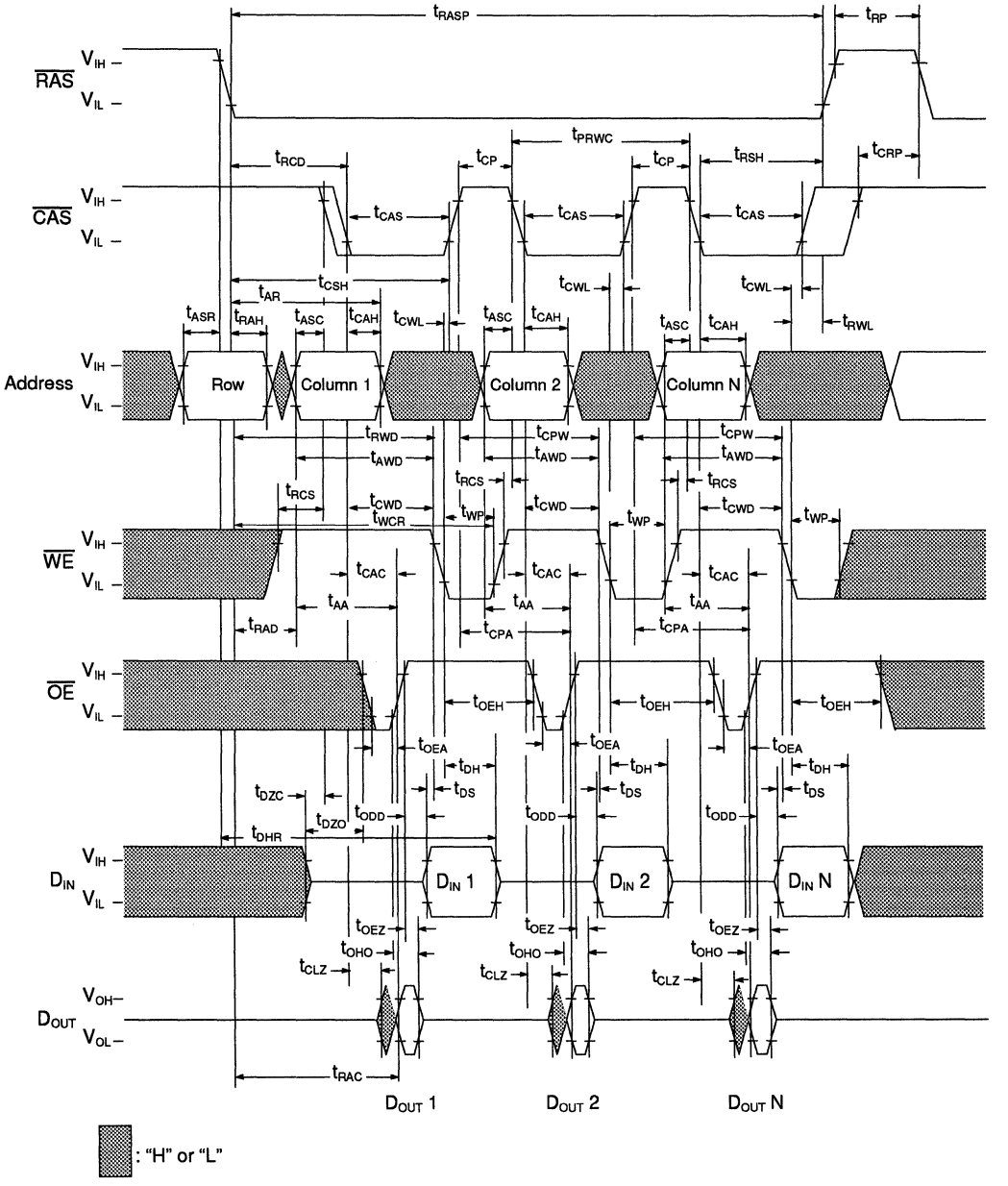
Fast Page Mode Read Cycle



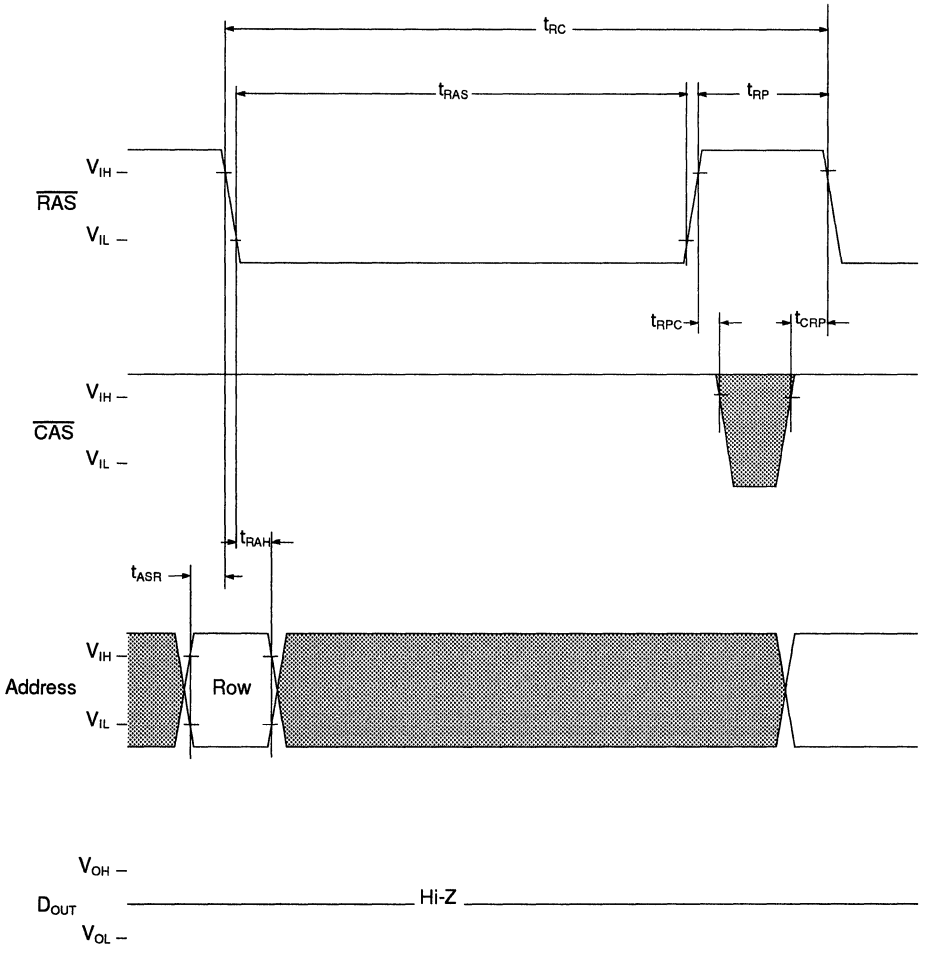
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

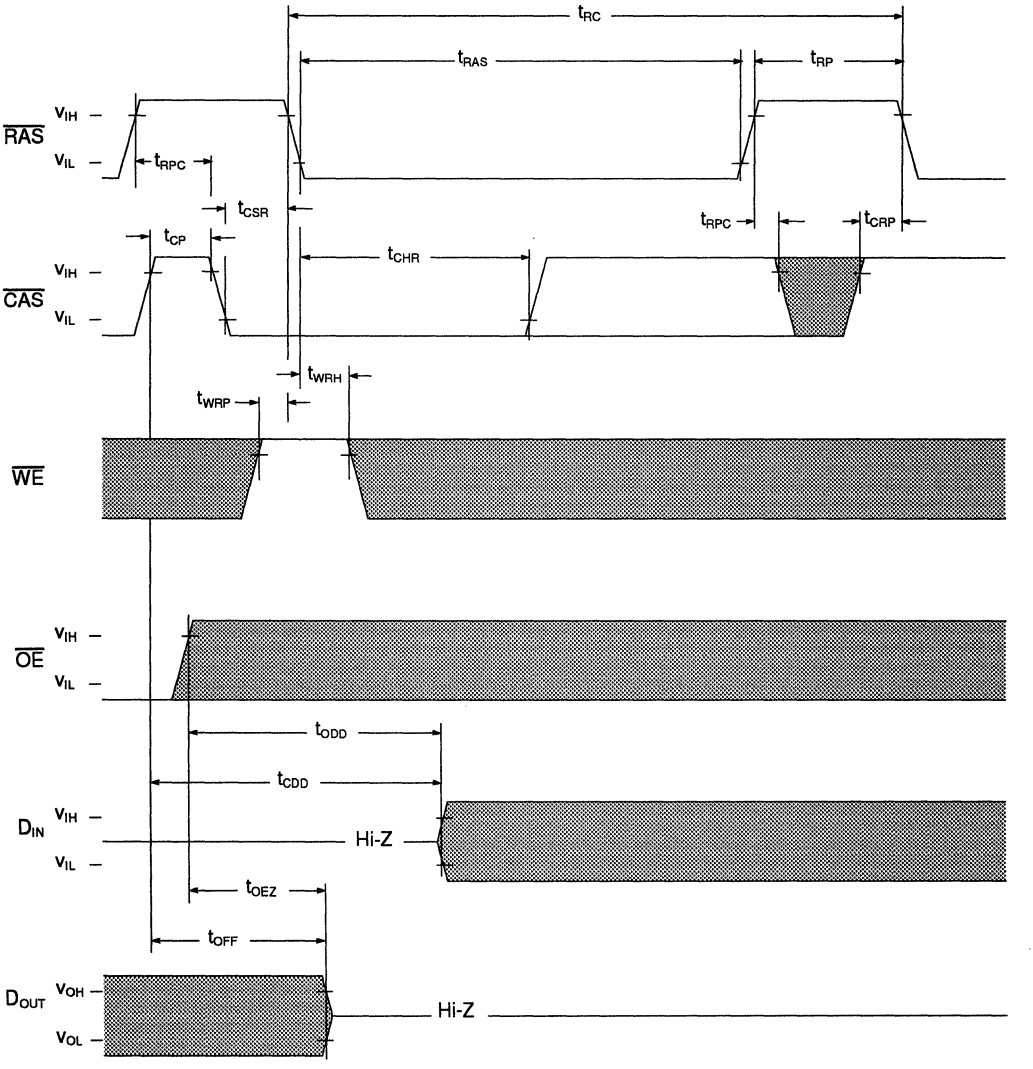


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

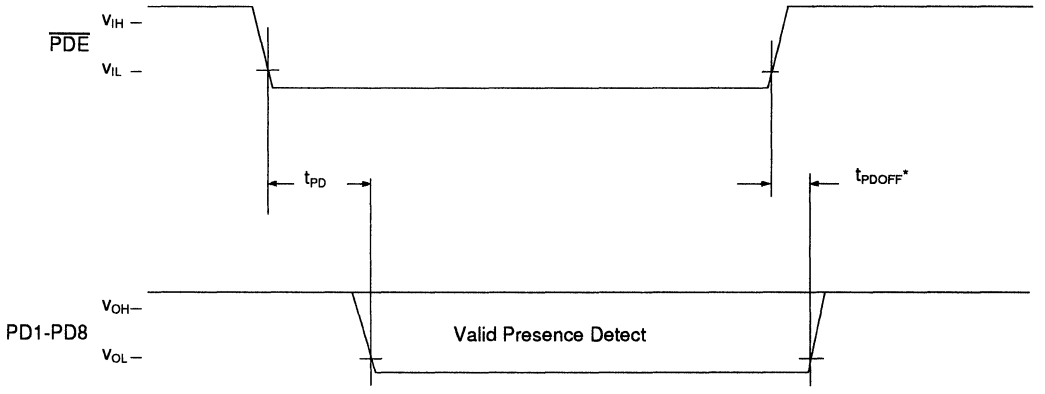
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



: "H" or "L"

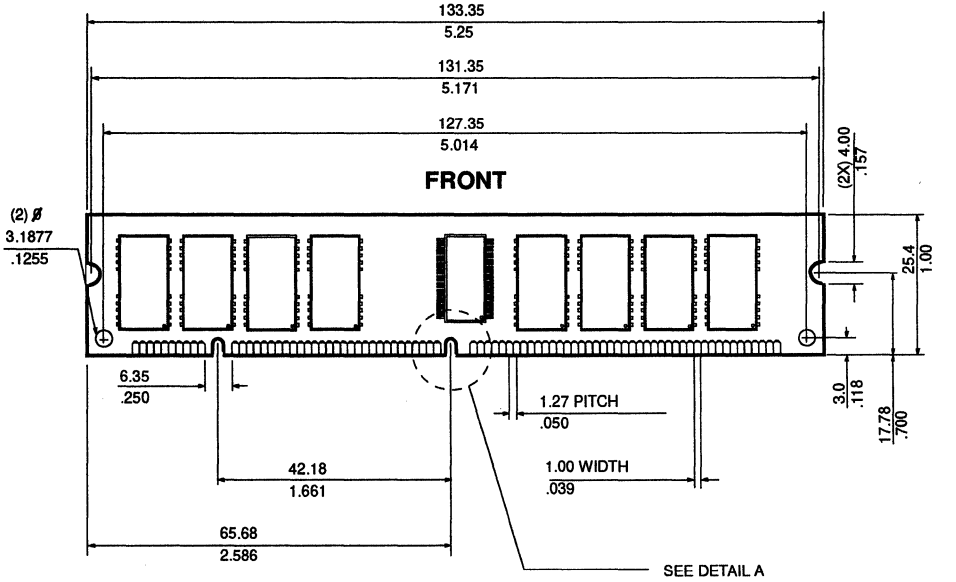
Note: Addresses are "H" or "L"

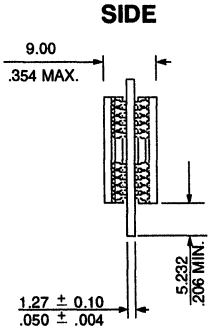
Presence Detect Read Cycle

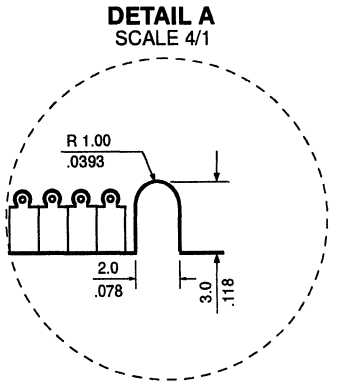


*PD pins must be pulled high at next level of assembly

Layout Drawing







NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 64 DRAM MODULE

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 2Mx64 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are fully TTL and CMOS compatible
- Single 5V, ± 0.5V Power Supply
- Au contacts
- Optimized for byte-write non-parity applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - 4 Byte Interleave enabled
  - Byte write, byte read accesses
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 2048 refresh cycles distributed across 32ms
- 11/10 addressing (Row/Column)
- Card size: 5.25" x 1.0" x 0.157"
- DRAMS in TSOP Package

Description

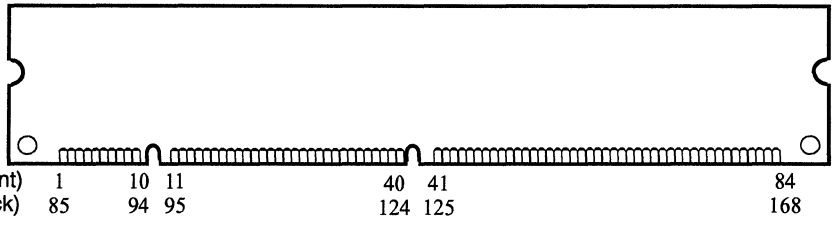
IBM11M2640H is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 2Mx64 high speed memory array for non-parity applications. The DIMM uses 8 2Mx8 DRAMs in TSOP packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, if a x64 parity DIMM were inserted into a bank of x72 parity DIMMs, ID0 (grounded) would indicate that at least one DIMM in that memory bank is x64, and if the memory controller is designed to do so, all DIMMs in that memory bank will function as x64s.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x72 parity (5V) and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A10	Address Inputs (Buffered)
DQx	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

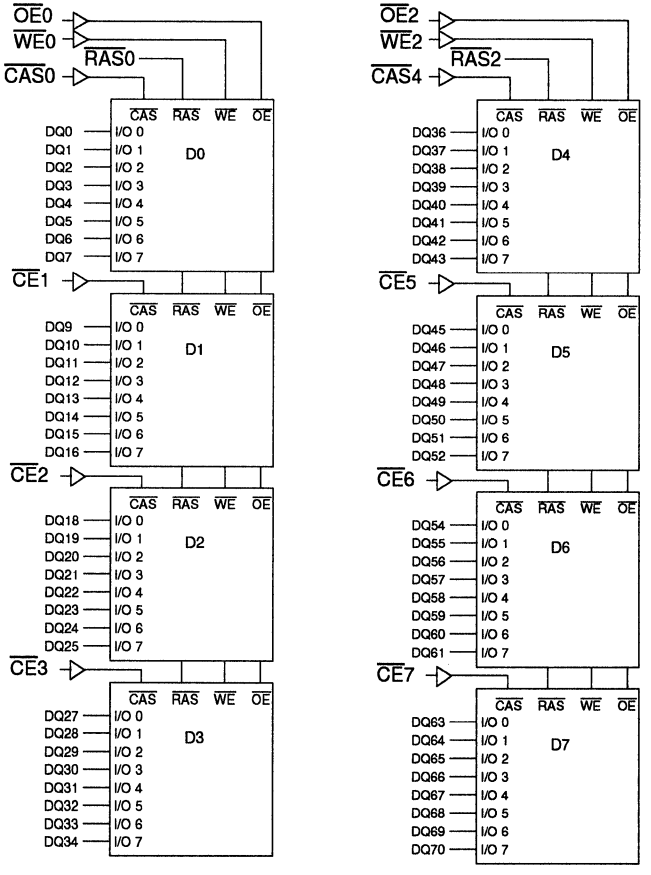
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	NC
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	$\overline{CAS5}$
5	DQ3	89	DQ39	47	$\overline{CAS6}$	131	$\overline{CAS7}$
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	NC	95	NC	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	NC	106	NC	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	NC	150	NC
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	$\overline{CAS1}$	70	DQ29	154	DQ65
29	$\overline{CAS2}$	113	$\overline{CAS3}$	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	NC	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	NC	161	NC
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	A10	122	NC	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

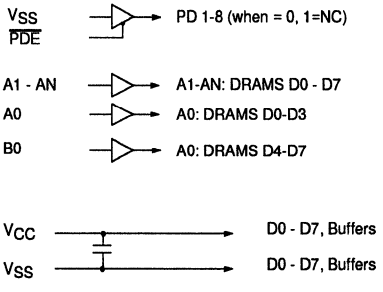
Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M2640HA-60	2Mx64	60ns	Au	5.25"x1.0"x0.157"	
IBM11M2640HA-70	2Mx64	70ns	Au	5.25"x1.0"x0.157"	

Block Diagram





Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	1	1
PD2	0	0
PD3	0	0
PD4	1	1
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	1	1
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} +0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} +0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	5.3	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A10)	13	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	35	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF	
C_{I4}	DQ_X Capacitance	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	960	mA	1,2,3
		-70	—	800		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	16	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	960	mA	1,3
		-70	—	800		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	600	mA	1,2,3
		-70	—	520		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	8	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	960	mA	1,3
		-70	—	800		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-40	+40		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1},I_{CC3},I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1},I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the Dram device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	1
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	4
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	—	5
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
2. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.
5. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	2	—	2	—	ns	3
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	3
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1,2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1,2
t_{AA}	Access Time from Address	—	36	—	41	ns	1,2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1,2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Access to $\overline{CAS}$ Lead Time	36	—	41	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	—	—	—	—	ns	4
t_{OH}	Output Data Hold tIme	2	—	2	—	ns	
t_{OHO}	Output Data Hold from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1,2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	63	—	73	—	ns	1

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	32	—	32	ms	1

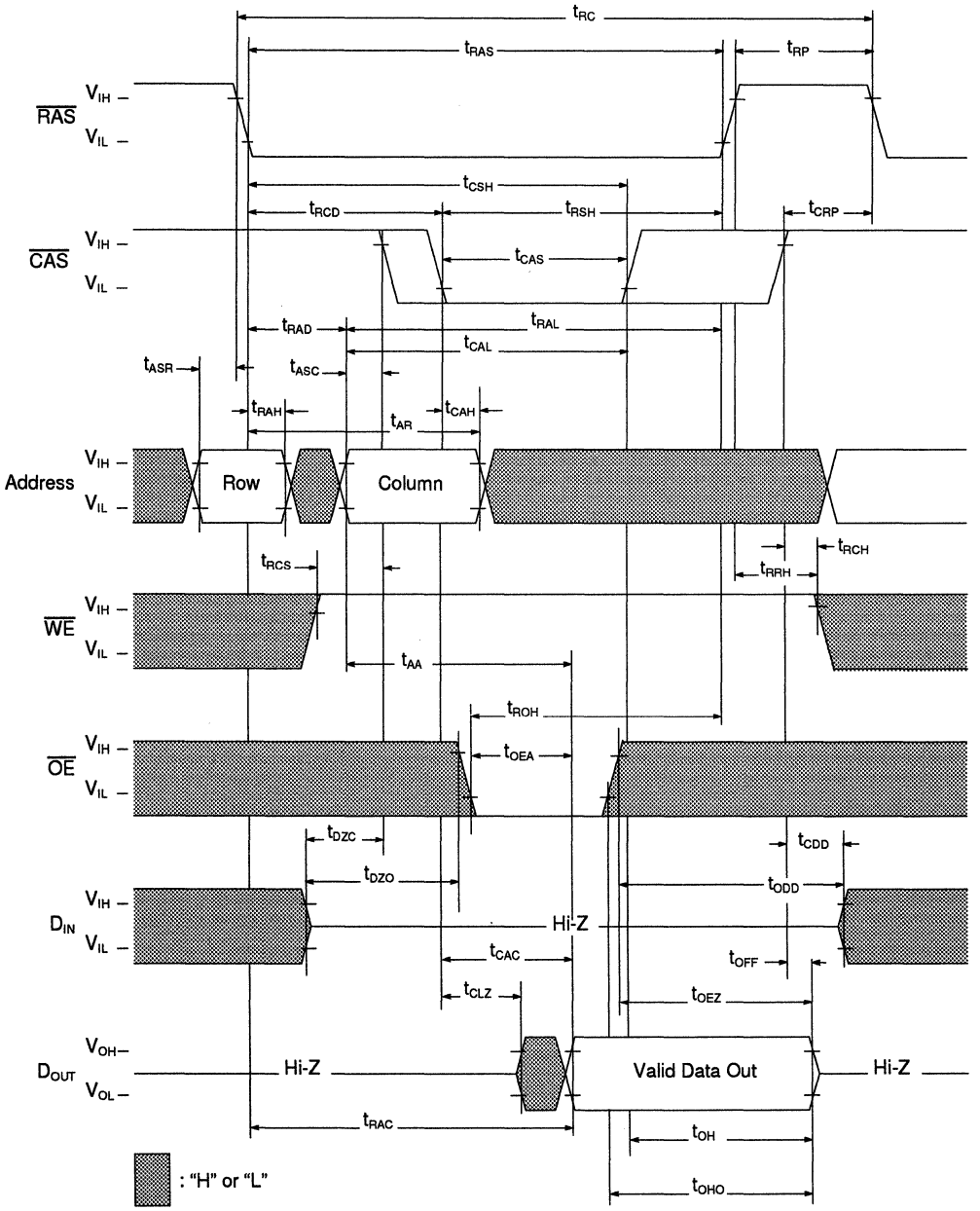
1. 2048 refreshes are required every 32ms.

Presence Detect Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
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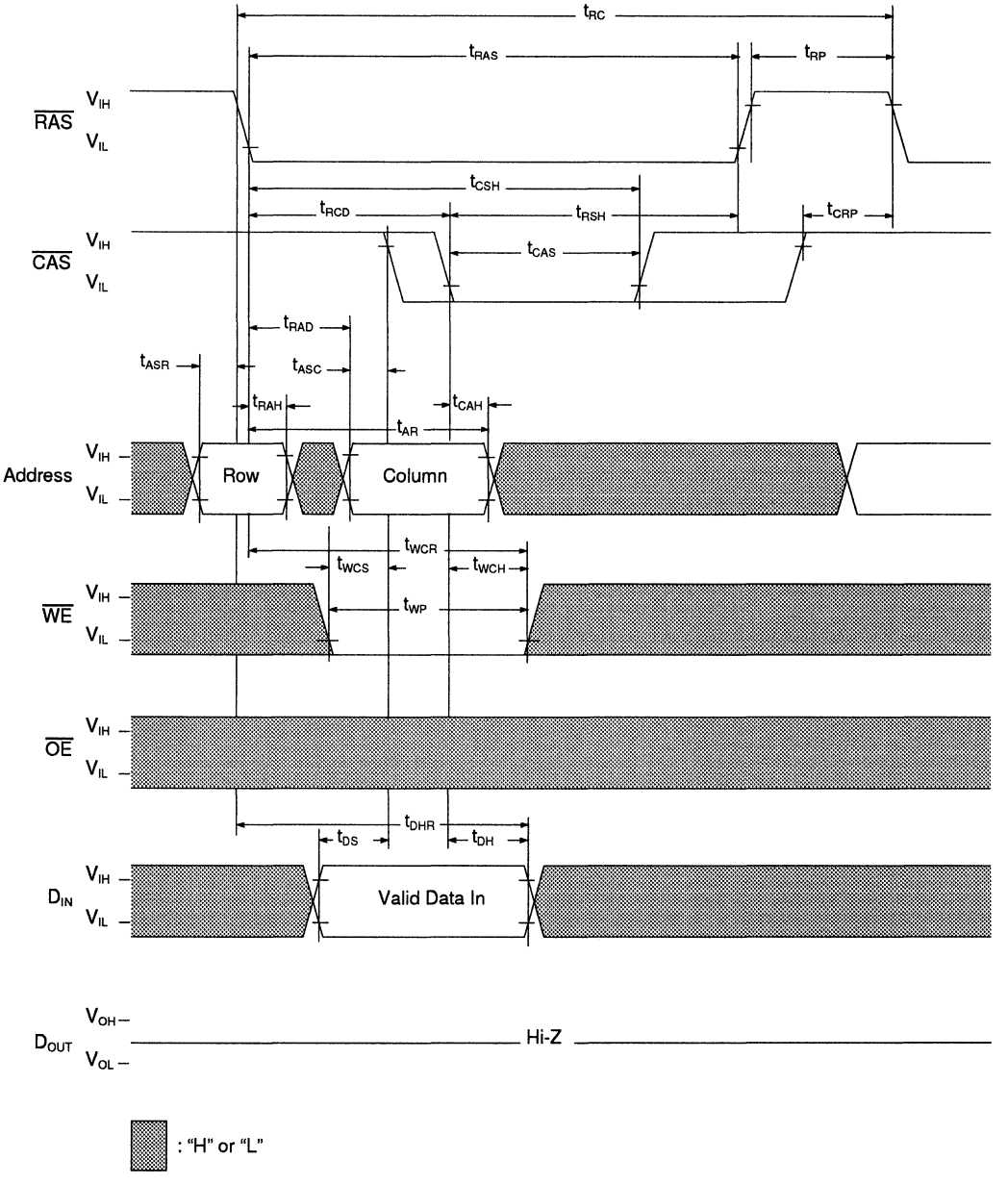
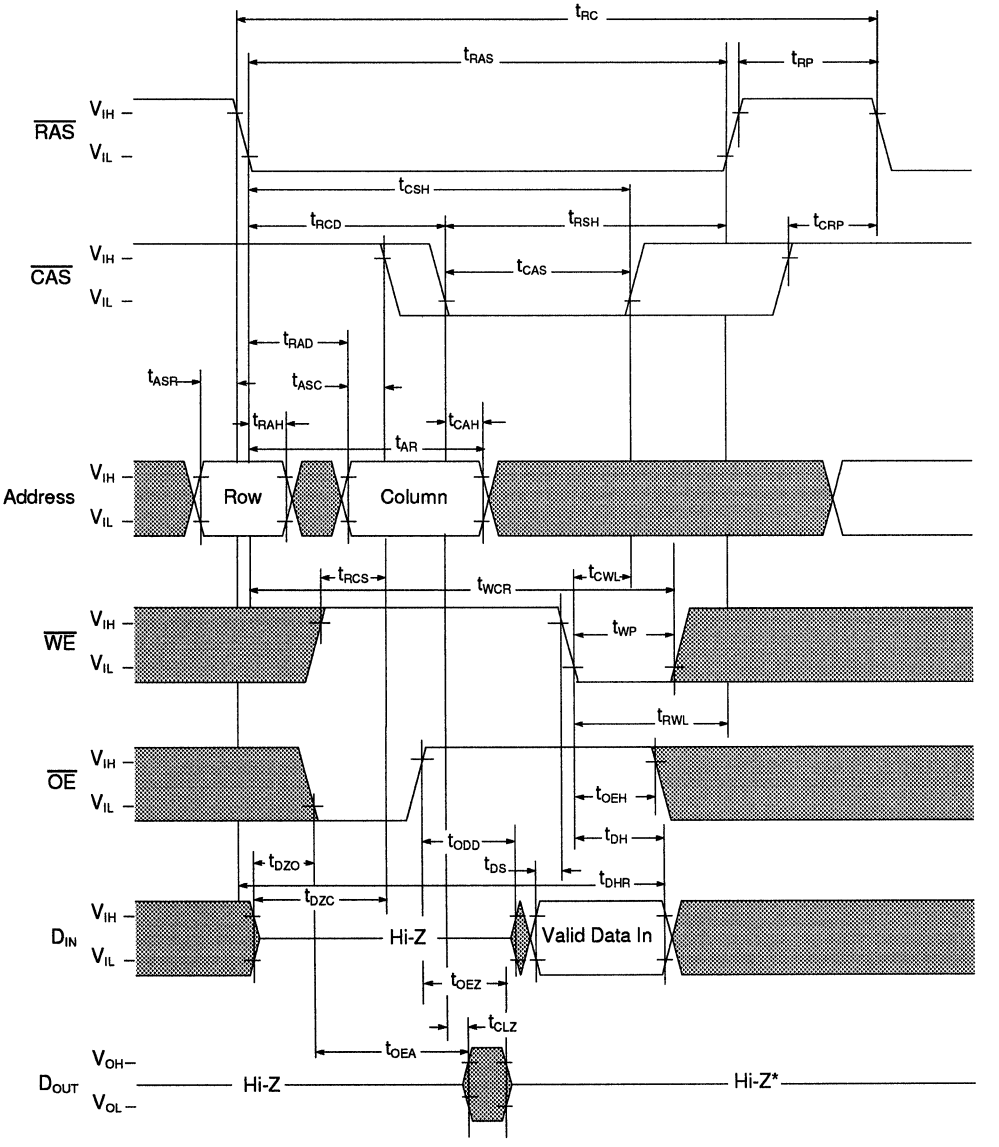
tASC
tRAH
tAR
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

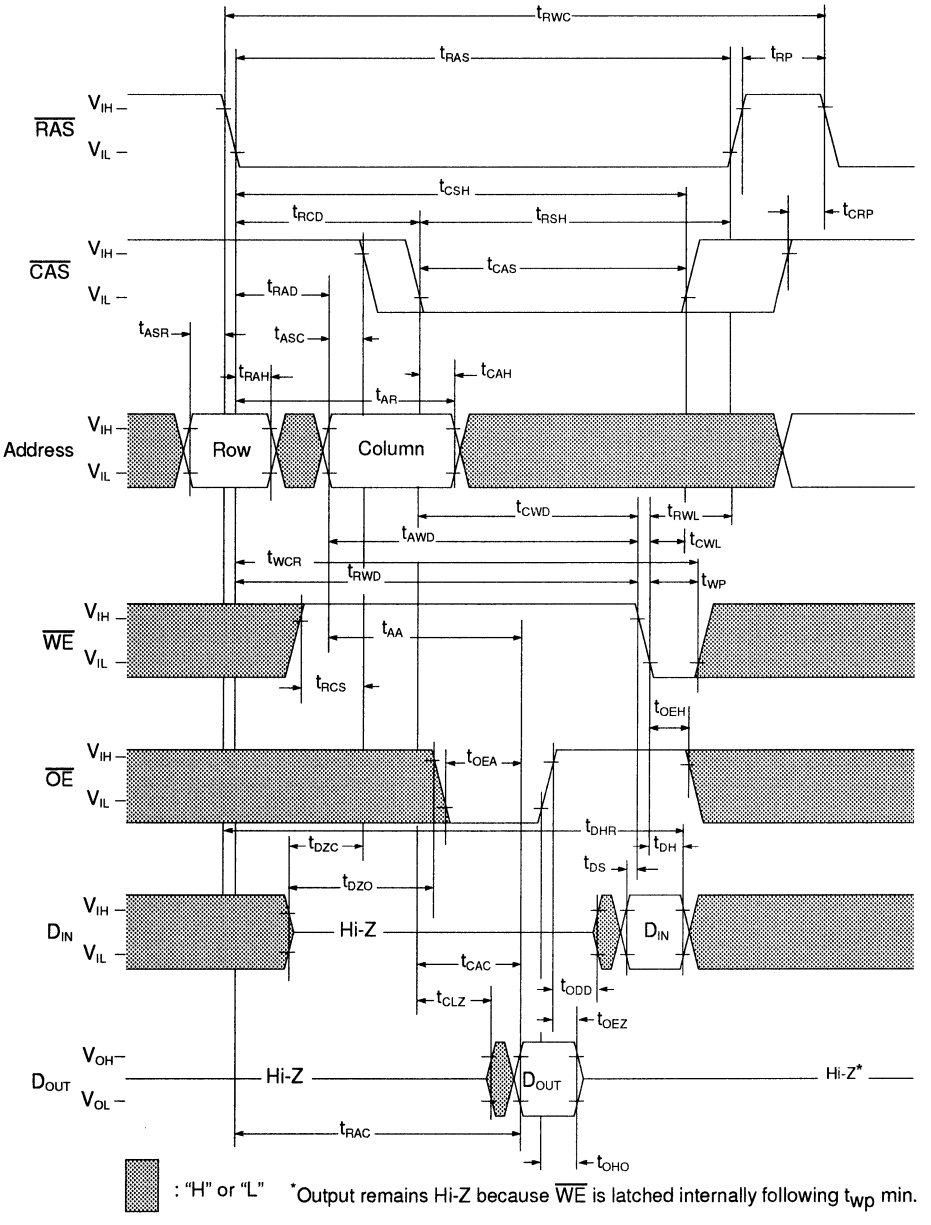


Write Cycle (Late Write)

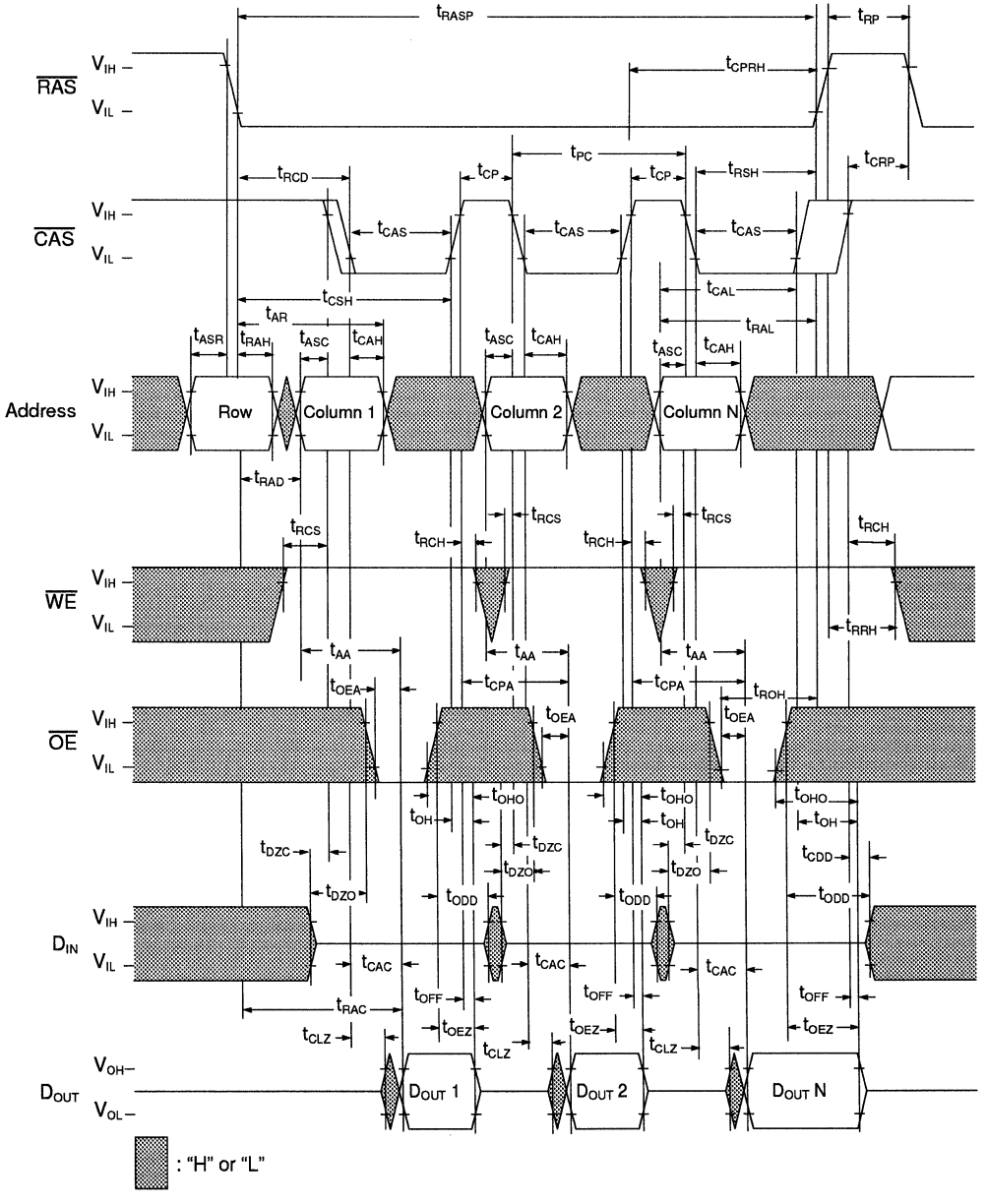


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

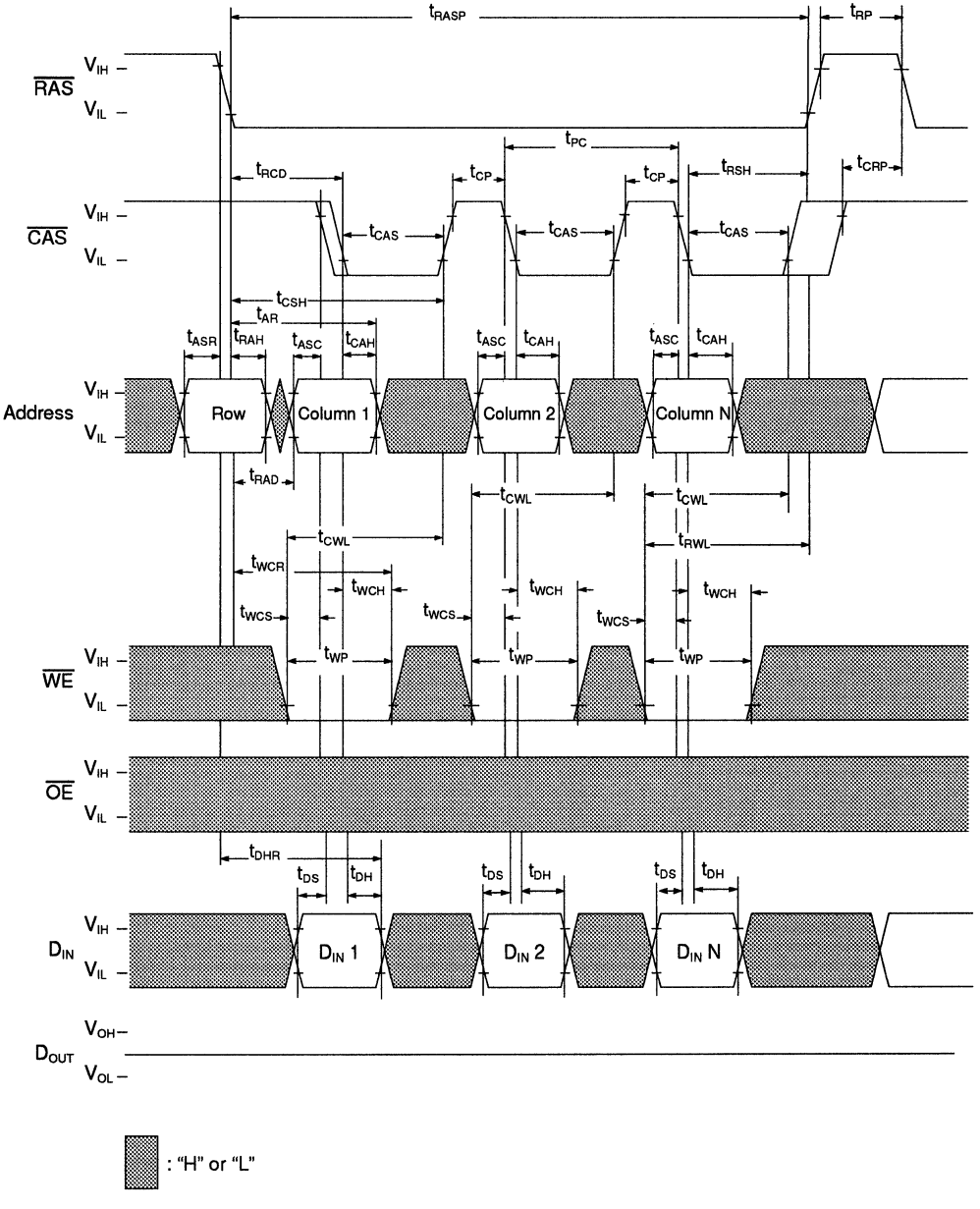
Read-Modify-Write-Cycle



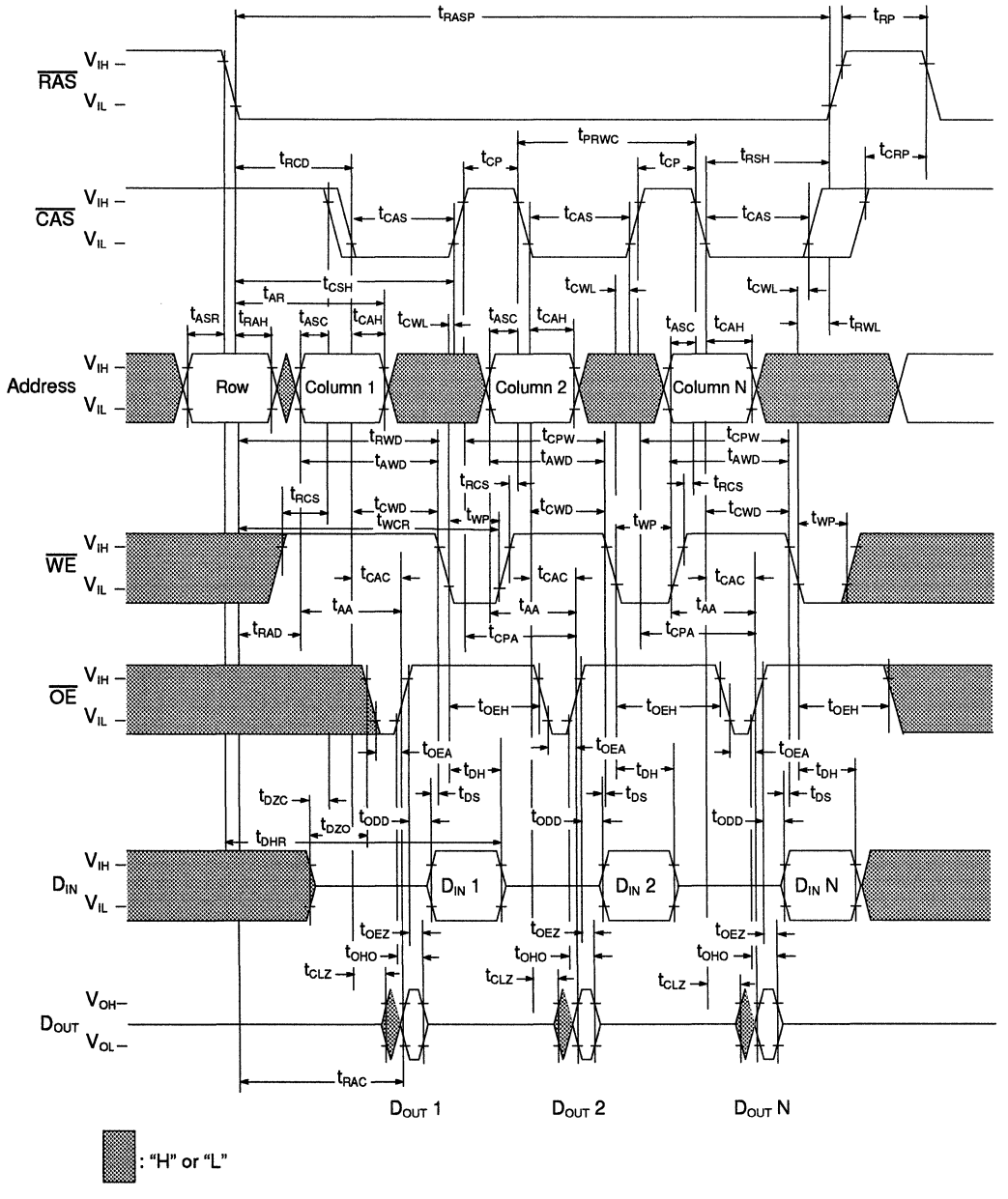
Fast Page Mode Read Cycle



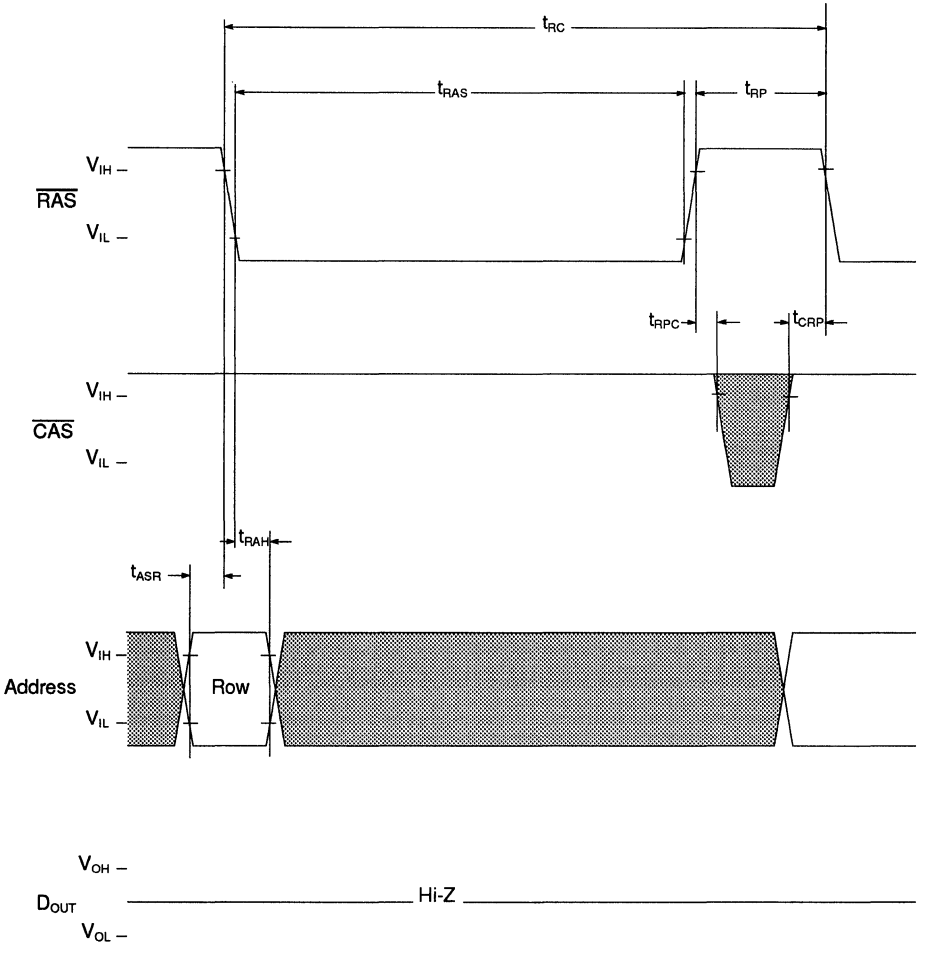
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

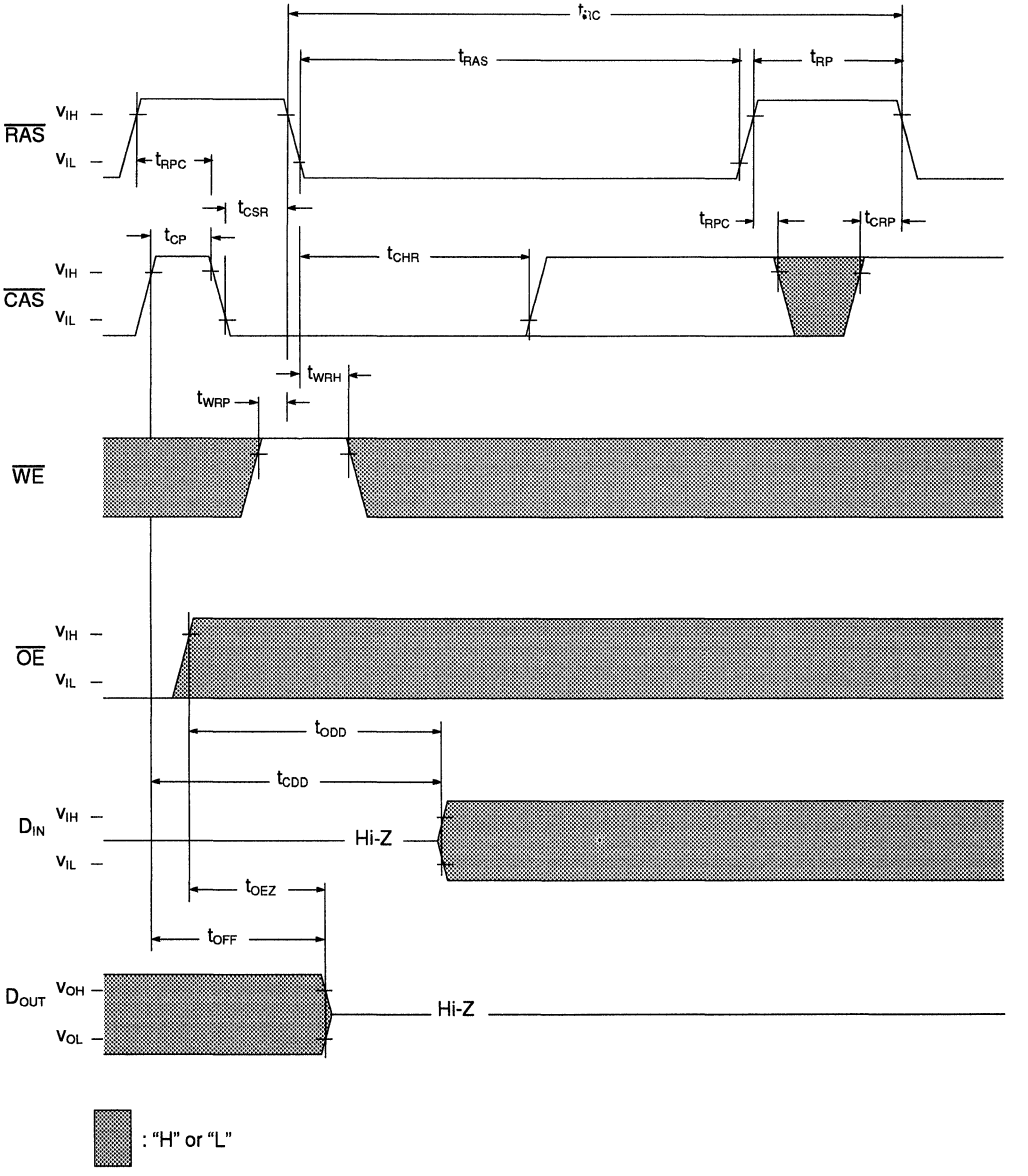


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

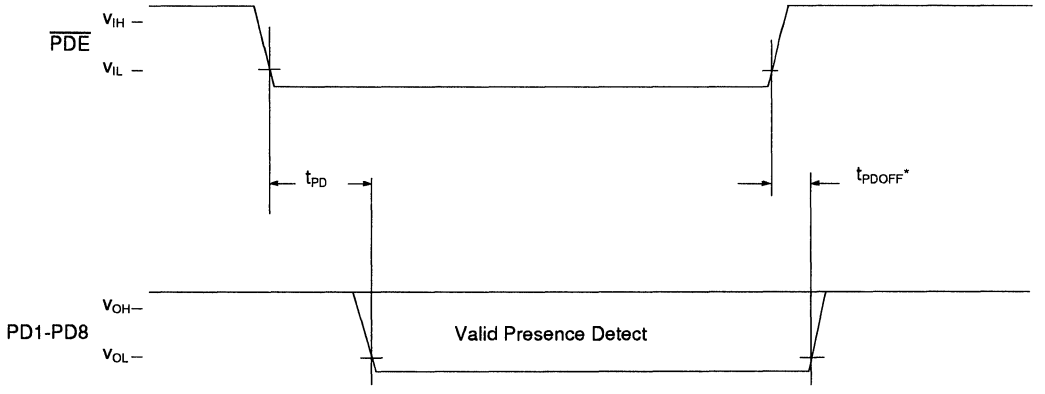
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



: "H" or "L"

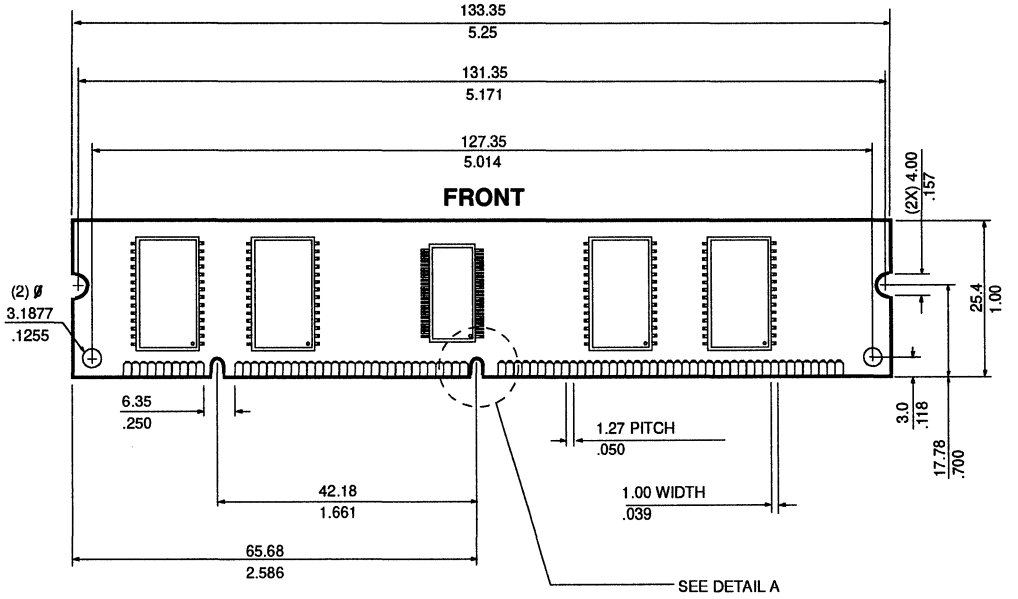
Note: Addresses are "H" or "L"

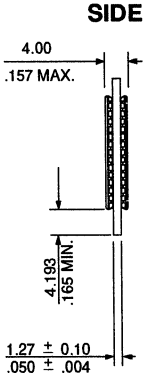
Presence Detect Read Cycle

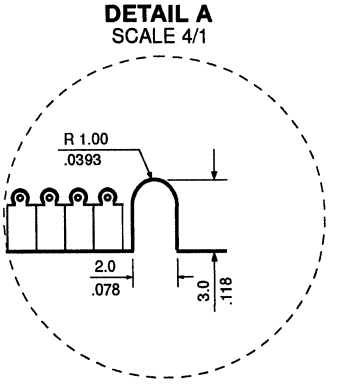


*PD pins must be pulled high at next level of assembly

Layout Drawing







NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

4M x 64 DRAM MODULE

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 4Mx64 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are fully TTL and CMOS compatible
- Single 5V, ± 0.5V Power Supply
- Au contacts
- Optimized for byte-write non-parity applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - 4 Byte Interleave enabled
  - Byte write, byte read accesses
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 4096 refresh cycles distributed across 64ms
- 12/10 addressing (Row/Column)
- Card size: 5.25" x 1.2" x 0.354"
- DRAMS in SOJ Package

Description

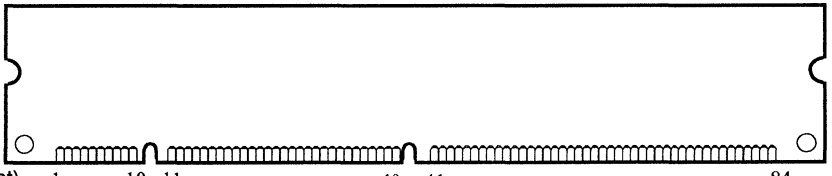
IBM11M4640C is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 4Mx64 high speed memory array for non-parity applications. The DIMM uses 16 4Mx4 DRAMs in SOJ packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, if a x64 parity DIMM were inserted into a bank of x72 parity DIMMs, ID0 (grounded) would indicate that at least one DIMM in that memory bank is x64, and if the memory controller is designed to do so, all DIMMs in that memory bank will function as x64s.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x72 parity (5V) and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A11	Address Inputs (Buffered)
DQx	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

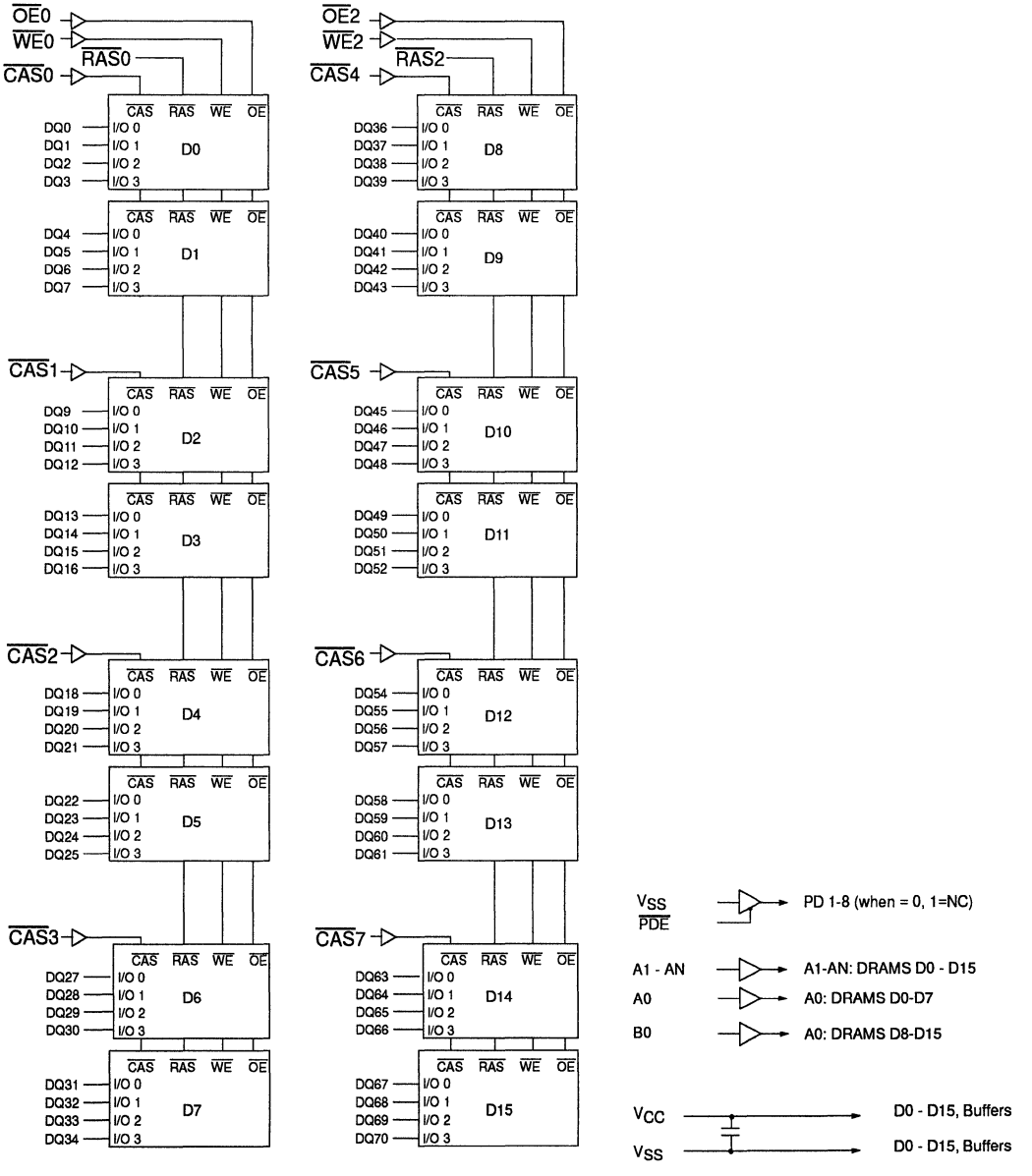
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	NC
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	$\overline{CAS5}$
5	DQ3	89	DQ39	47	$\overline{CAS6}$	131	$\overline{CAS7}$
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	NC	95	NC	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	NC	106	NC	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	NC	150	NC
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	$\overline{CAS1}$	70	DQ29	154	DQ65
29	$\overline{CAS2}$	113	$\overline{CAS3}$	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	NC	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	NC	161	NC
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	A10	122	A11	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M4640CA-60	4Mx64	60ns	Au	5.25"x1.2"x0.354"	
IBM11M4640CA-70	4Mx64	70ns	Au	5.25"x1.2"x0.354"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	1	1
PD2	1	1
PD3	0	0
PD4	1	1
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	1	1
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} +0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} +0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	7.5	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A0-A11)	13	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	60	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF	
C_{I4}	DQ_X Capacitance	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1360	mA	1,2,3
		-70	—	1200		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	32	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1360	mA	1,3
		-70	—	1200		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1200	mA	1,2,3
		-70	—	1040		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	16	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1360	mA	1,3
		-70	—	1200		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-80	+80		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the Dram device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	1
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	4
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	—	5
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
2. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.
5. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	2	—	2	—	ns	3
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	3
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1,2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1,2
t_{AA}	Access Time from Address	—	36	—	41	ns	1,2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1,2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Access to $\overline{CAS}$ Lead Time	36	—	41	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	—	—	—	—	ns	4
t_{OH}	Output Data Hold tIme	2	—	2	—	ns	
t_{OHO}	Output Data Hold from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1,2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	63	—	73	—	ns	1

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	64	—	64	ms	1

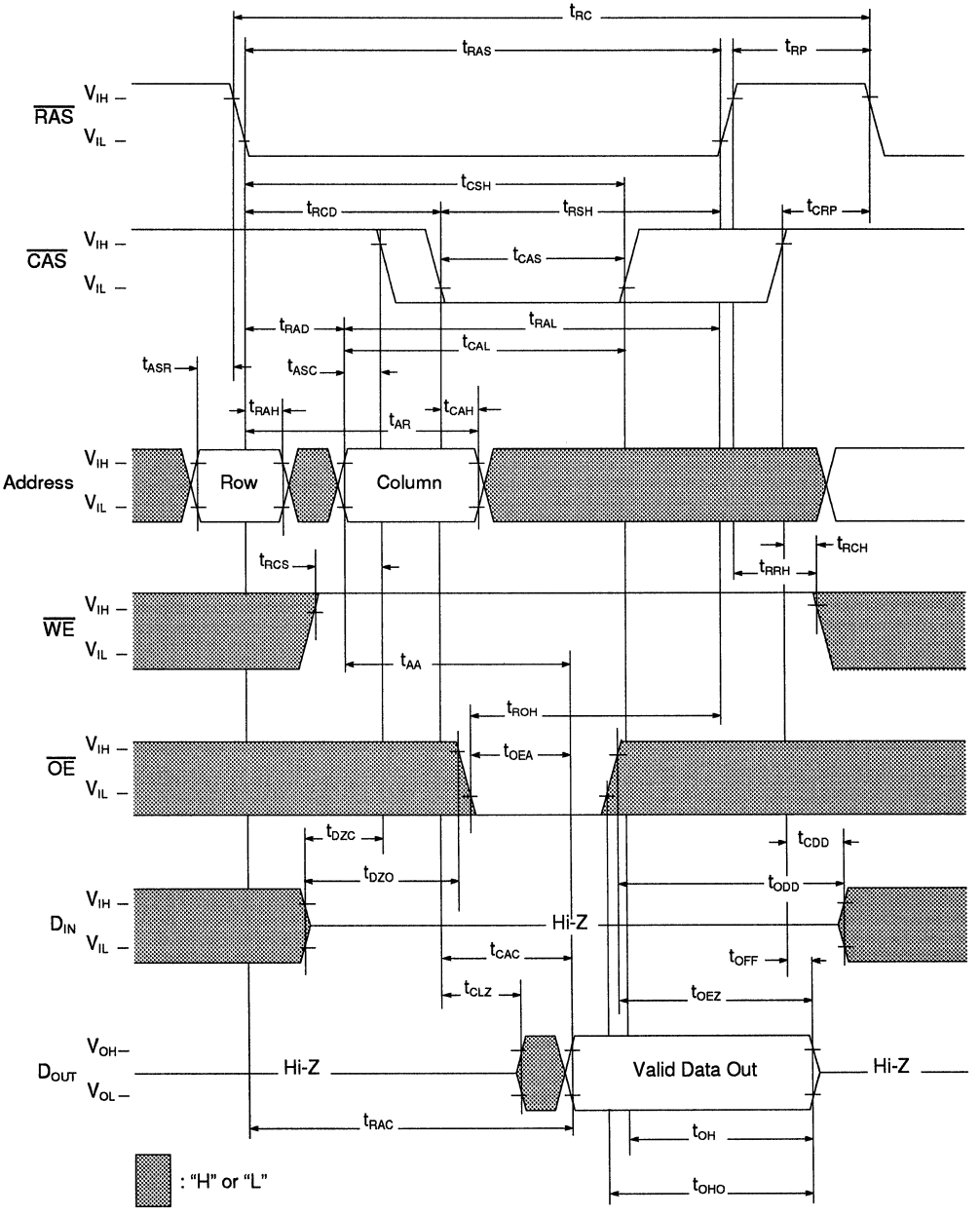
1. 4096 refreshes are required every 64ms.

Presence Detect Read Cycle

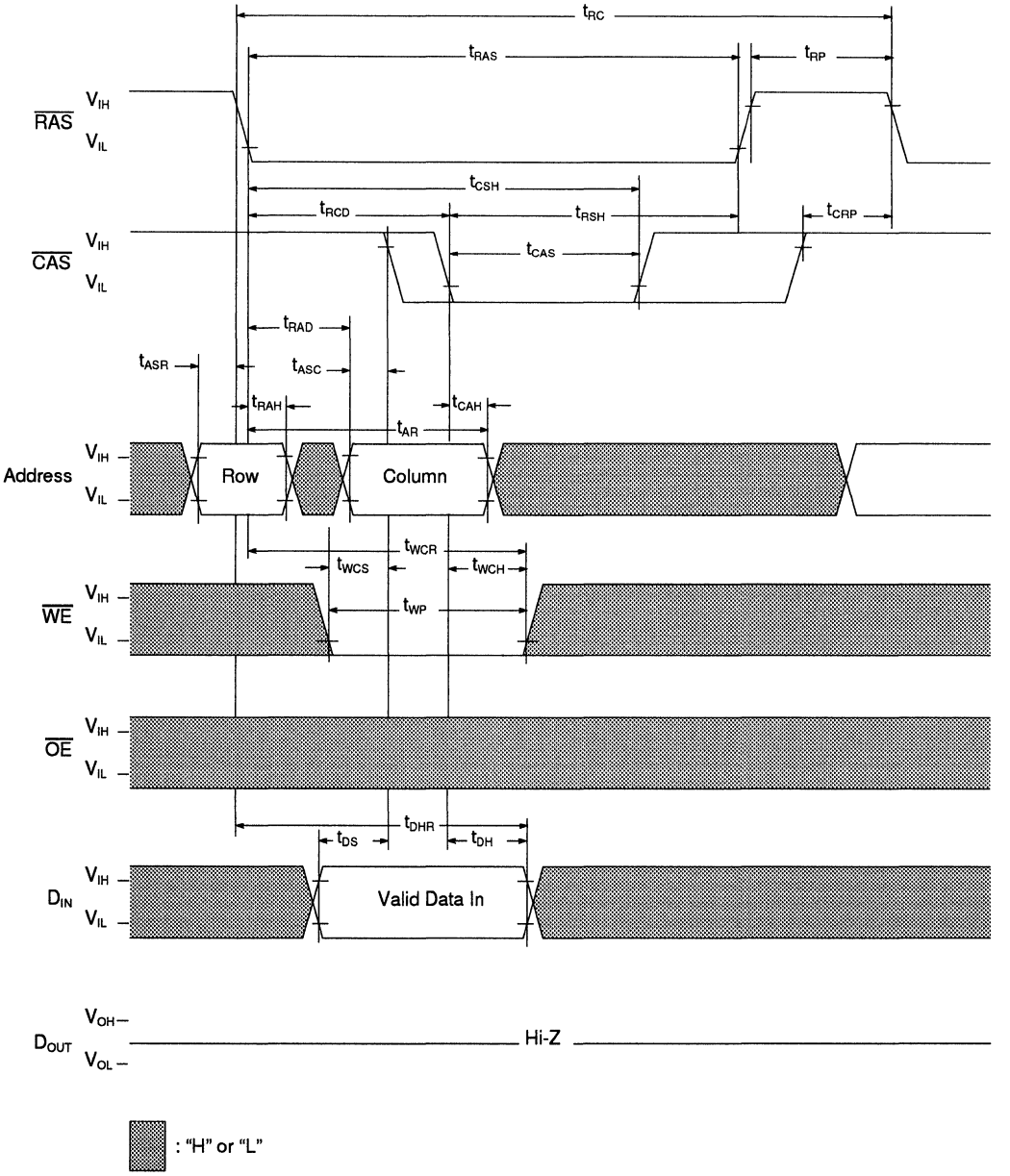
Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

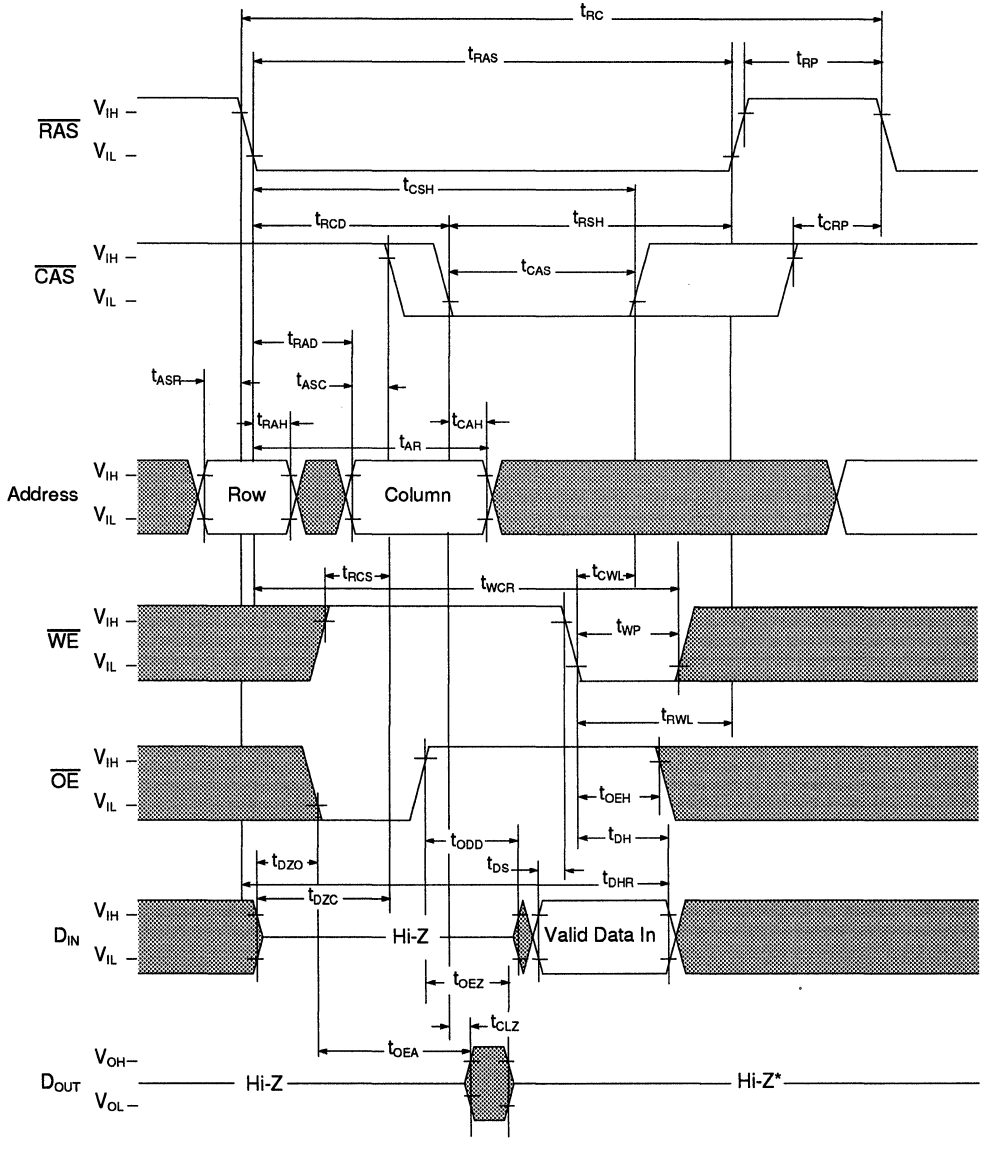
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tAR
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

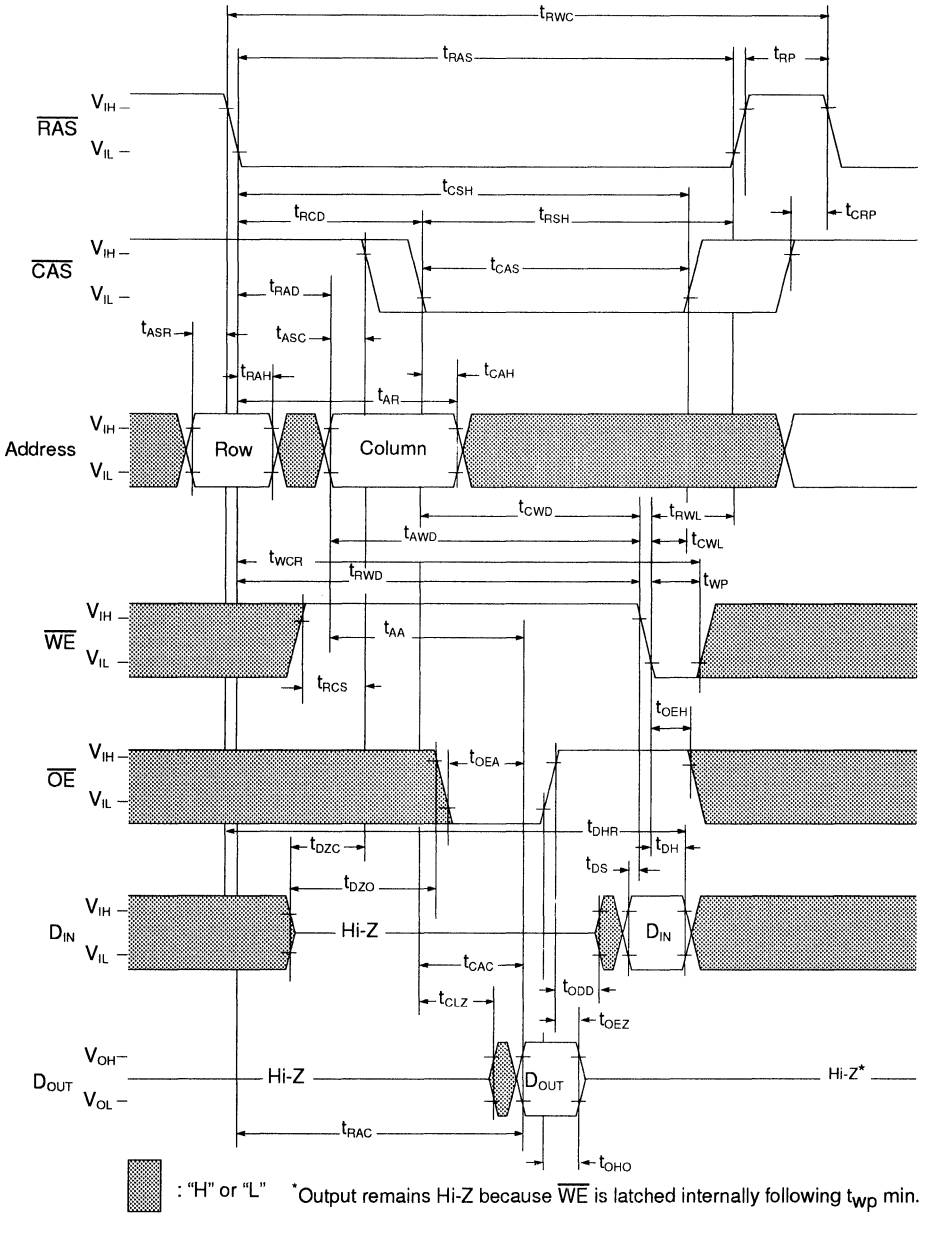


Write Cycle (Late Write)

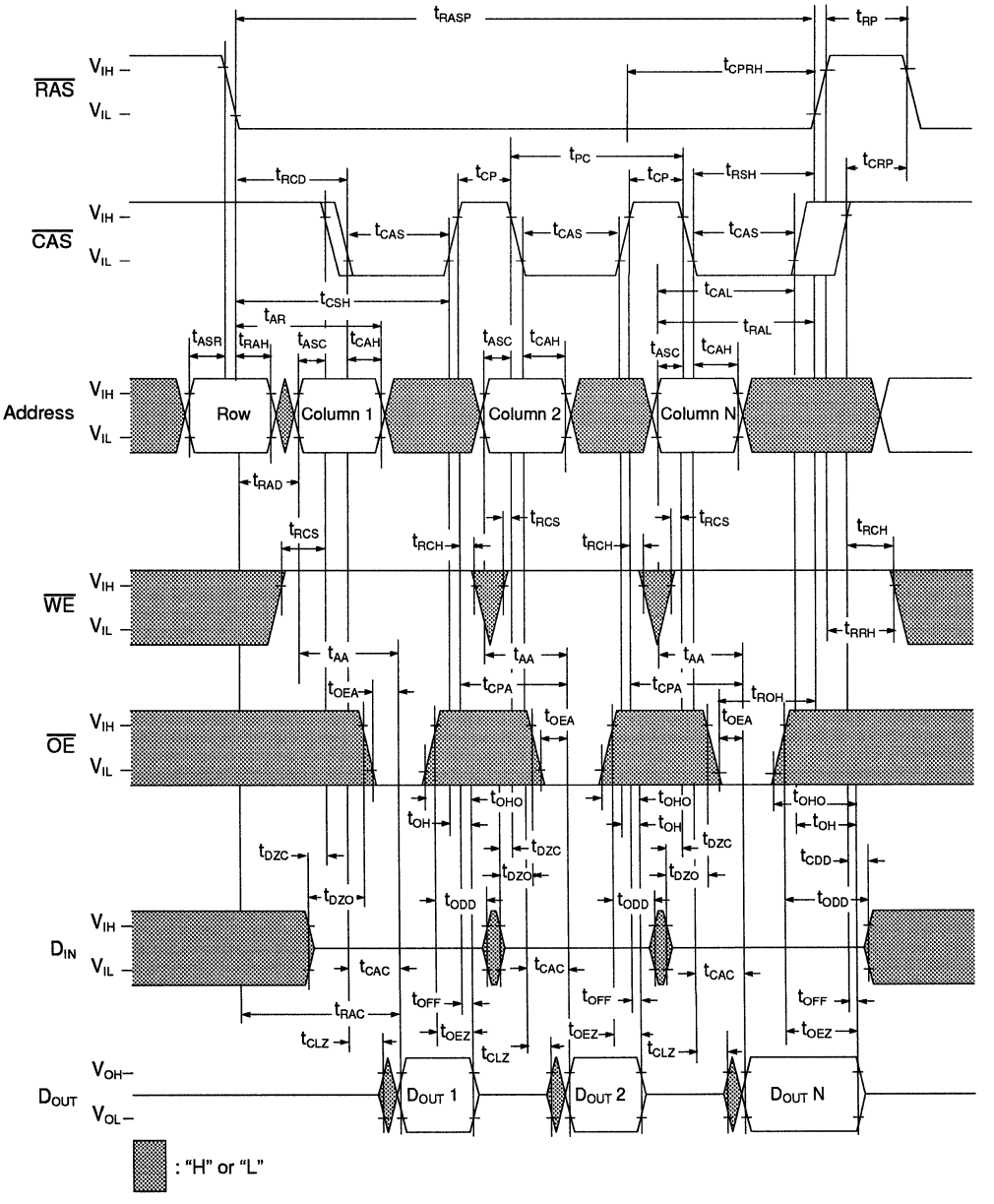


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

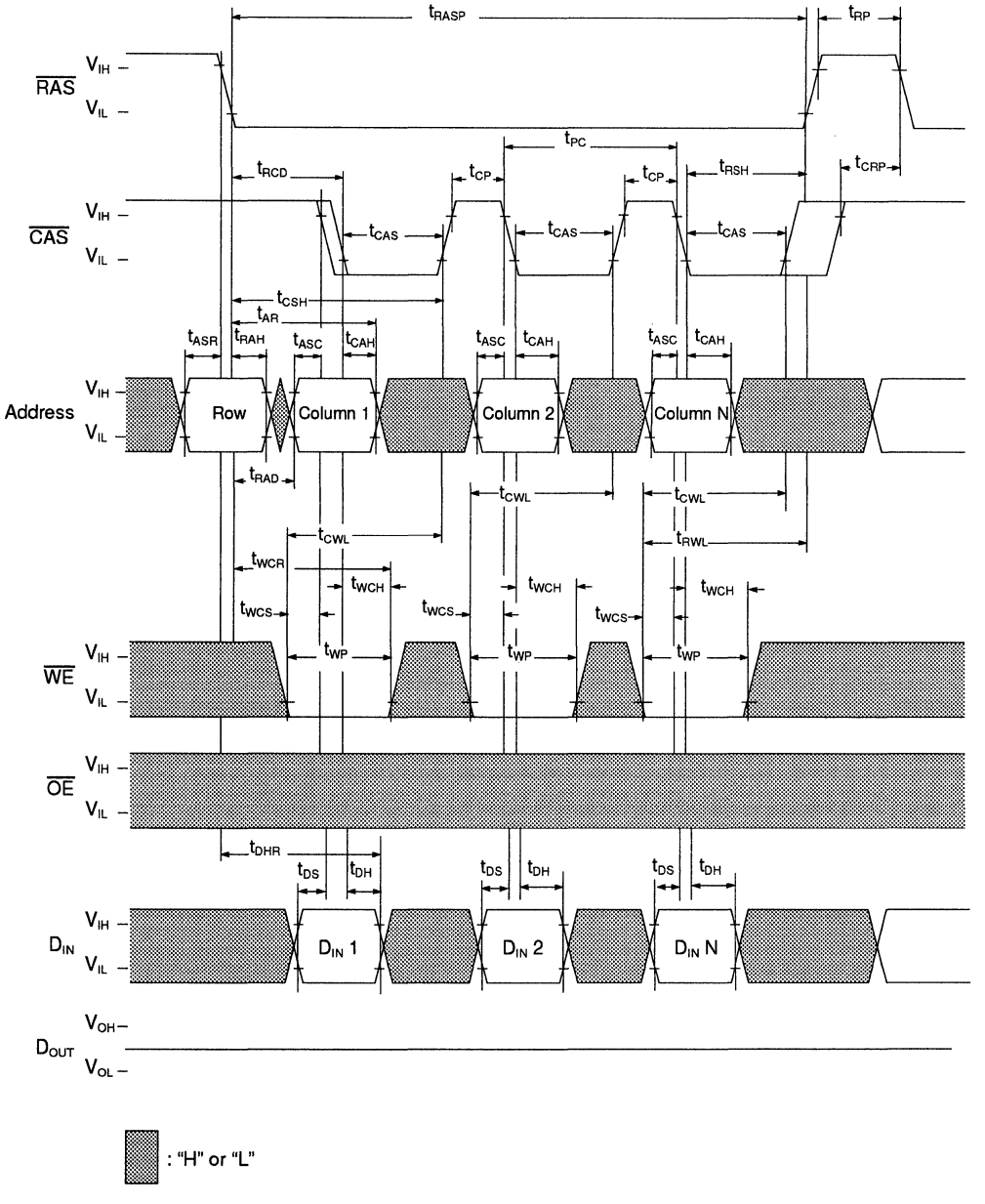
Read-Modify-Write-Cycle



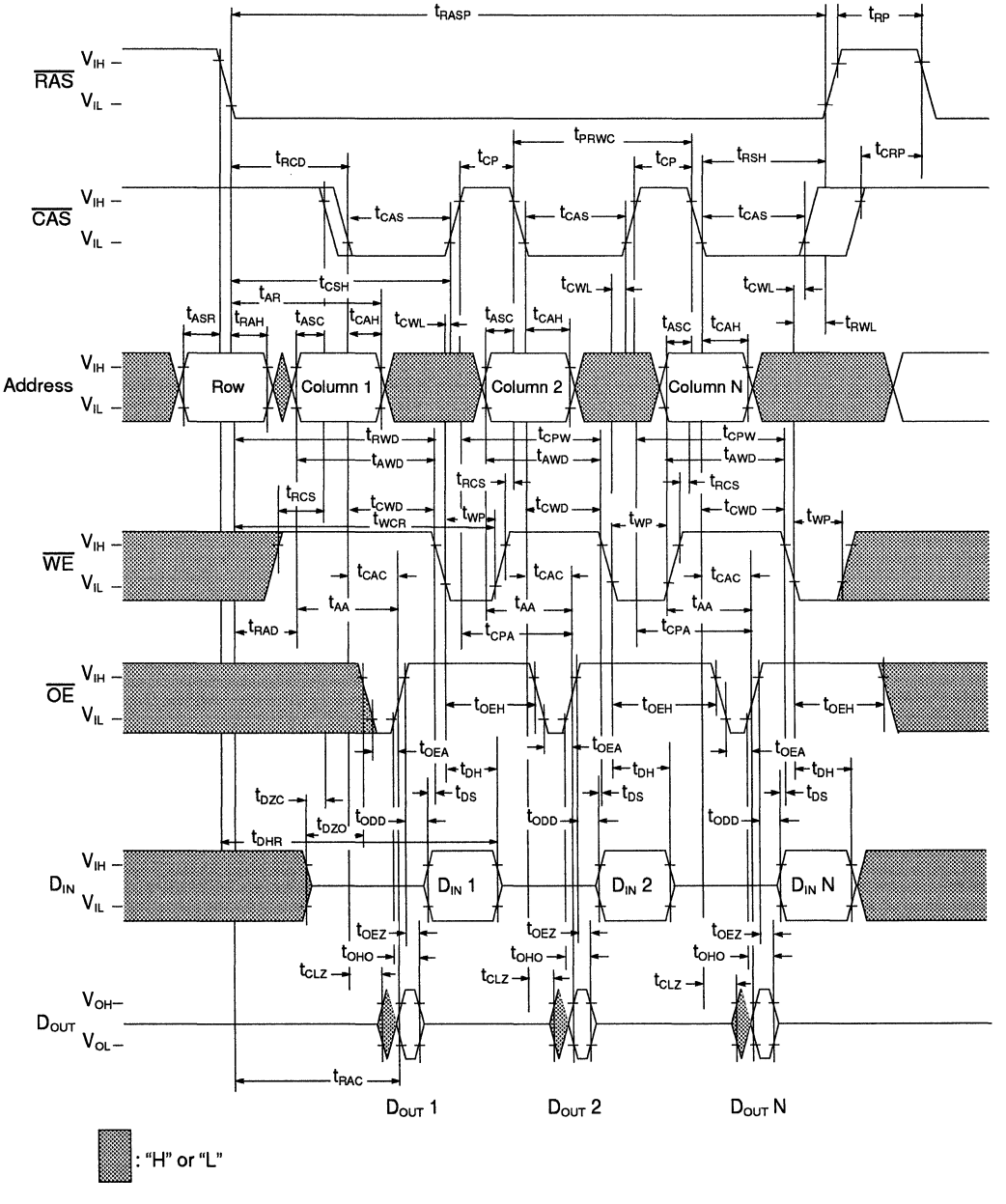
Fast Page Mode Read Cycle



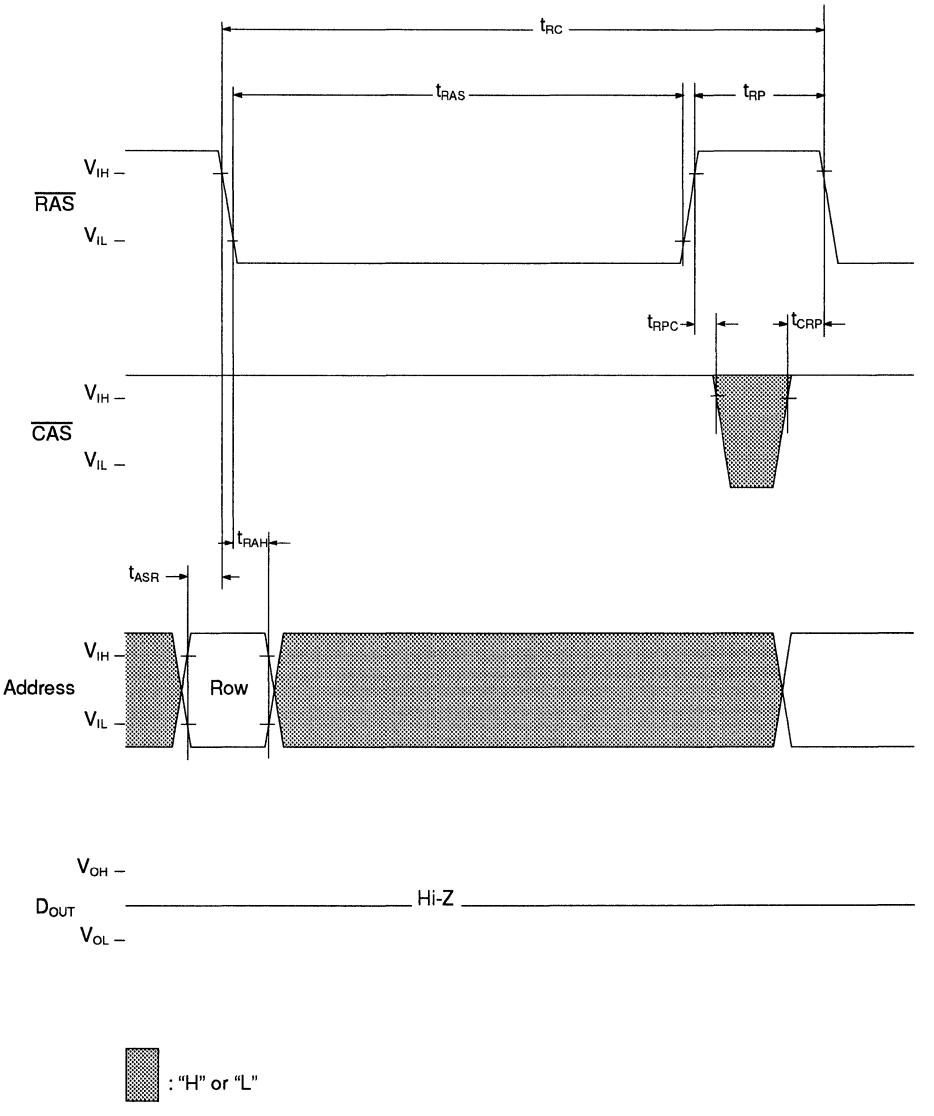
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

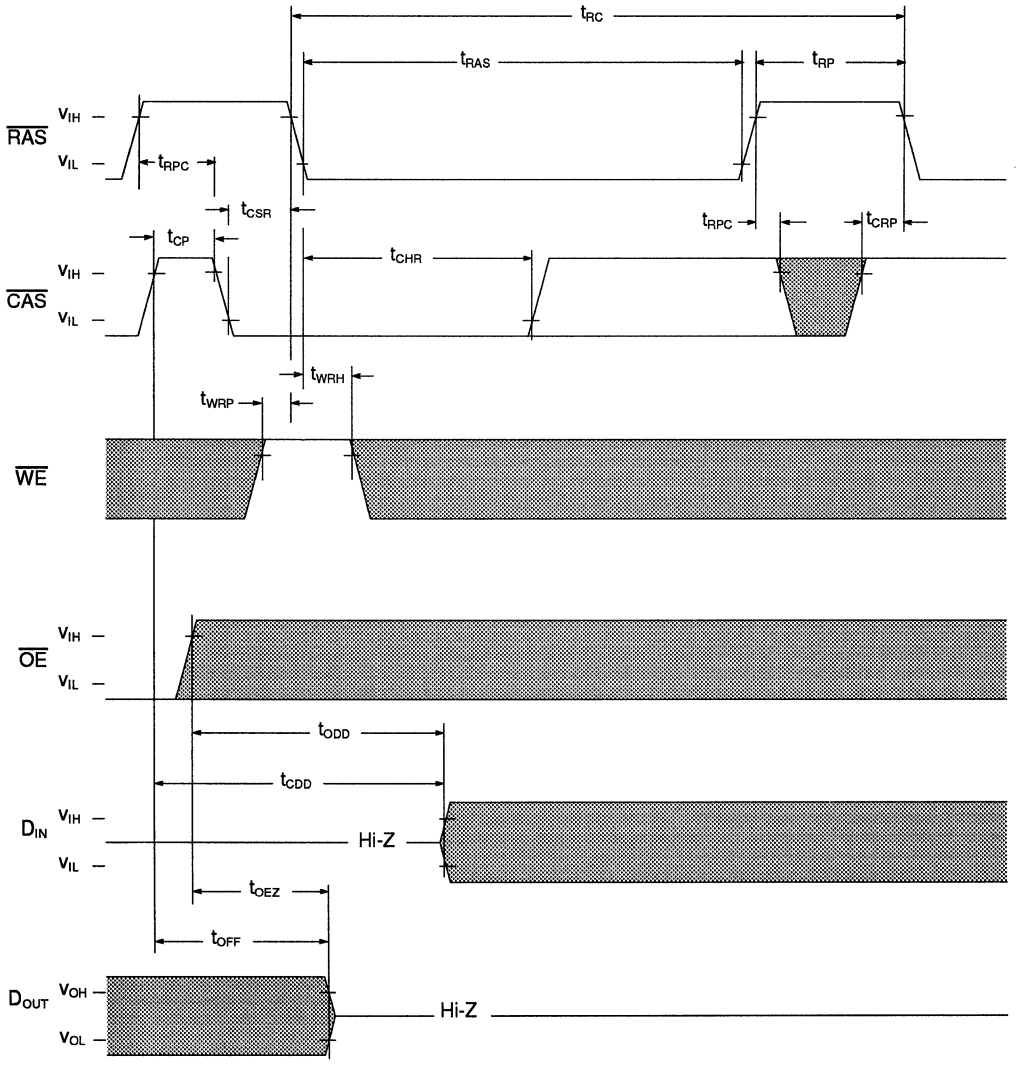


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

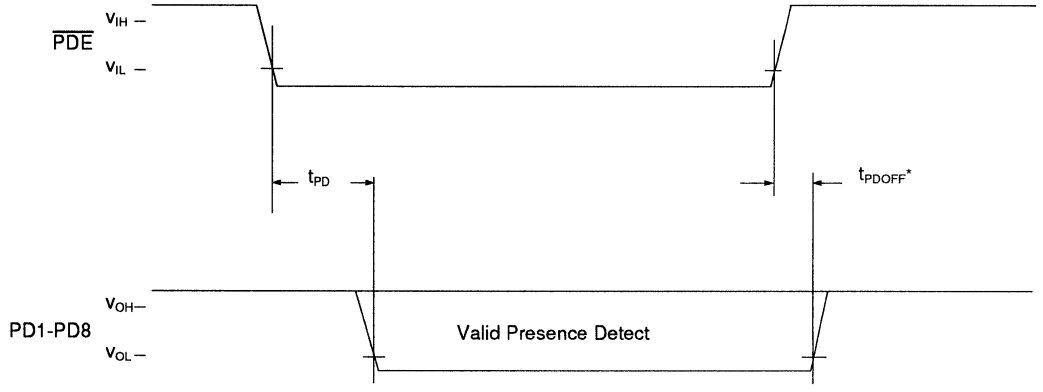
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



: "H" or "L"

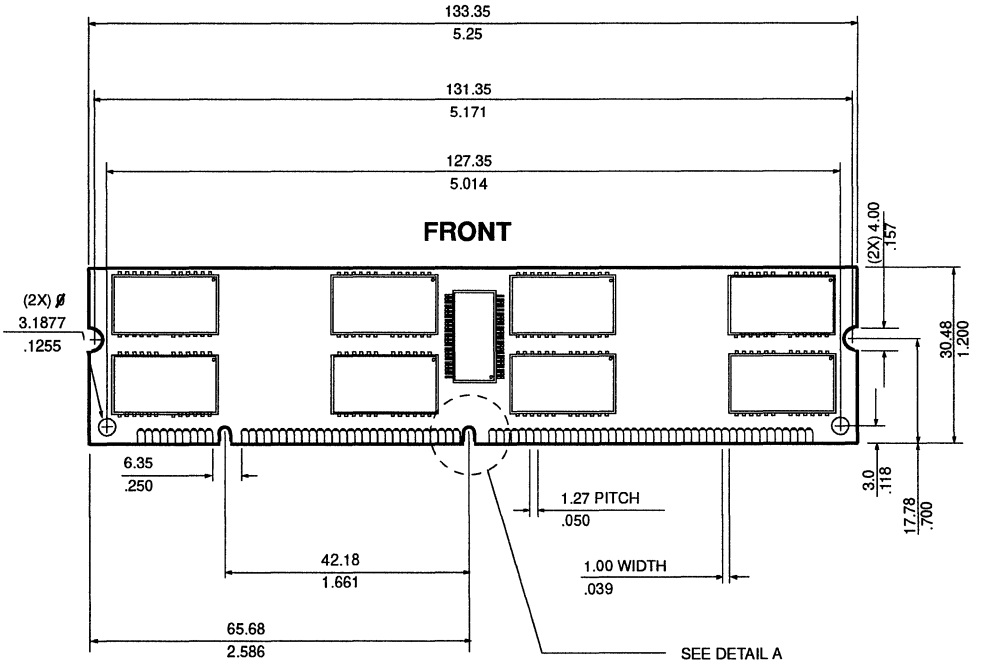
Note: Addresses are "H" or "L"

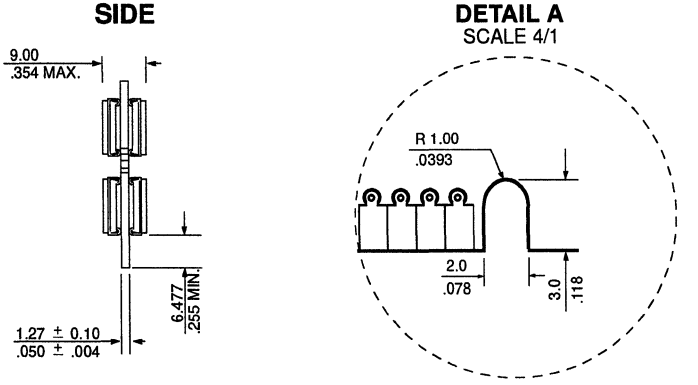
Presence Detect Read Cycle



*PD pins must be pulled high at next level of assembly

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

1M x 72 DRAM MODULE

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 1Mx72 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are fully TTL and CMOS compatible
- Single 5V, ± 0.5V Power Supply
- Au contacts
- Optimized for byte-write parity applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - 4 Byte Interleave Enabled
  - Byte write, byte read accesses
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 addressing (Row/Column)
- Card size: 5.25" x 1.0" x 0.354"
- DRAMS in SOJ Package

Description

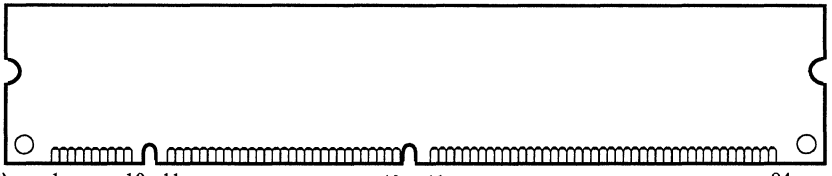
IBM11M1720BA is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 1Mx72 high speed memory array for parity applications. The DIMM uses 16 1Mx4 DRAMs and 2 1Mx4 Quad CAS DRAMs in SOJ packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, if a x64 or x72 (ECC) DIMM were inserted into a bank of x72 parity DIMMs, IDO (grounded) would indicate that at least one DIMM in that memory bank will not function properly. PD8 would indicate what positions, if any, contained an ECC DIMM.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 non-parity (5V) and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A9	Address Inputs (Buffered)
DQx	Data Input/Output
PQx	Parity Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

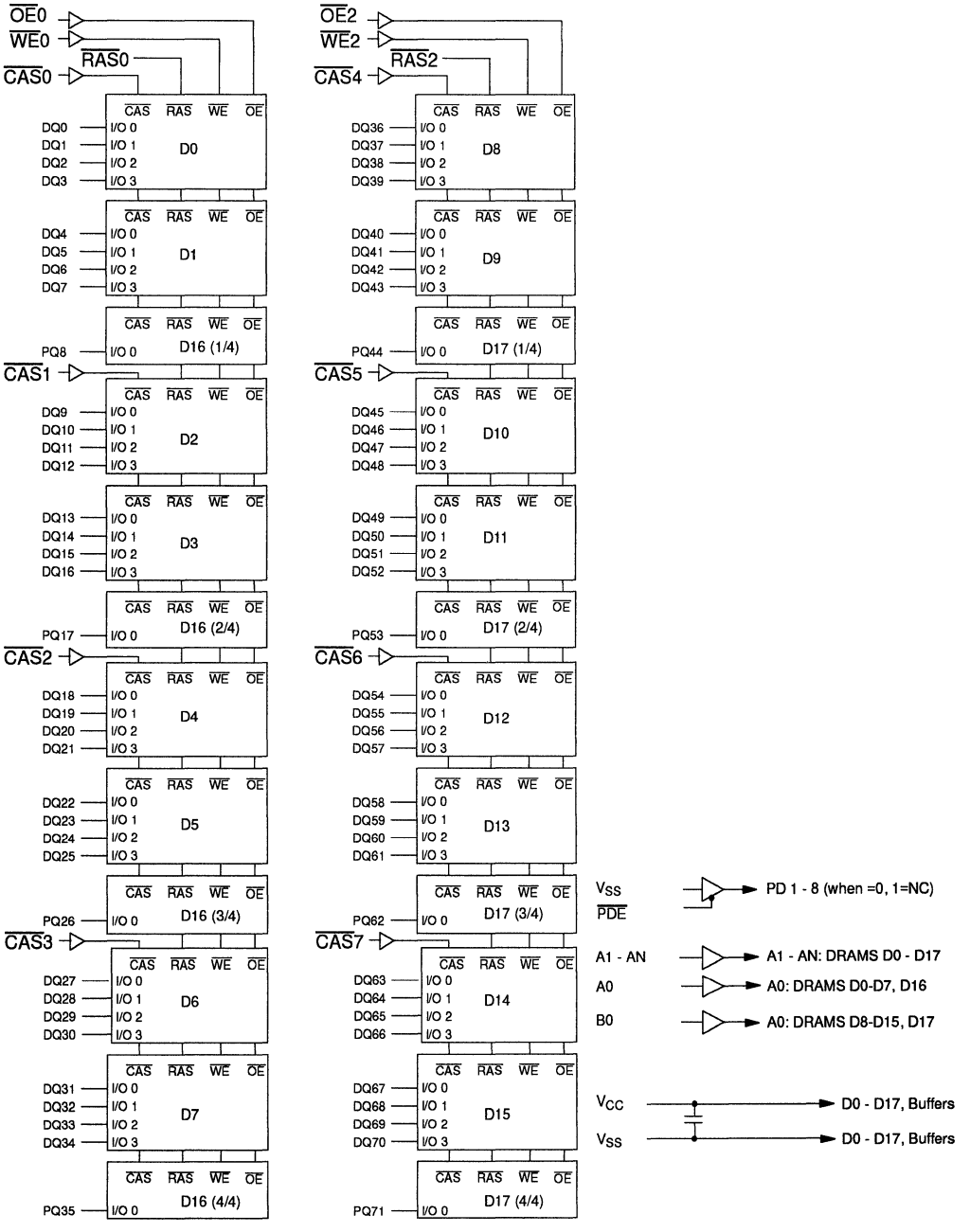
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	NC
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	$\overline{CAS5}$
5	DQ3	89	DQ39	47	$\overline{CAS6}$	131	$\overline{CAS7}$
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	PQ8	95	PQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	PQ17	106	PQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	PQ26	150	PQ62
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	$\overline{CAS1}$	70	DQ29	154	DQ65
29	$\overline{CAS2}$	113	$\overline{CAS3}$	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	NC	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	PQ35	161	PQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	NC	122	NC	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M1720BA-60	1Mx72	60ns	Au	5.25"x1.0"x 0.354"	
IBM11M1720BA-70	1Mx72	70ns	Au	5.25"x1.0"x 0.354"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx, PQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	0	0
PD2	0	0
PD3	1	1
PD4	0	0
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	1	1
ID0 (DIMM Type/Width)	1	1
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 6.5	V	1
V_{IN}	Input Voltage	-0.7 to V_{CC} +0.7	V	1
V_{OUT}	Output Voltage	-0.7 to V_{CC} +0.7	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	11.7	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ±0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A9)	13	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	70	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF	
C_{I4}	DQ_X Capacitance	15	pF	
C_{I5}	PQ_X Capacitance	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	2120	mA	1,2,3
		-70	—	1908		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	37	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	2120	mA	1,3
		-70	—	1908		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1340	mA	1,2,3
		-70	—	1240		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	34	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	2120	mA	1,3
		-70	—	1908		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1},I_{CC3},I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1},I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. The 1Mx4 DRAM outputs will remain disabled until these 8 cycles have occurred. This prevents data contention (excessive current) during power on. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the DRAM device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	1
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	2
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	3
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	4
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	5
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	57	—	62	—	—	
t_{CLCH}	Hold Time $\overline{CAS}$ Low to $\overline{CAS}$ High	10	—	10	—	ns	6
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	

1. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
2. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
3. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
4. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
5. Either t_{CDD} or t_{ODD} must be satisfied.
6. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	2	—	ns	1
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	47	—	57	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	2
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	2

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	36	—	41	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	15	—	15	—	ns	
t_{OH}	Output Data Hold Time	2	—	2	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1, 2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

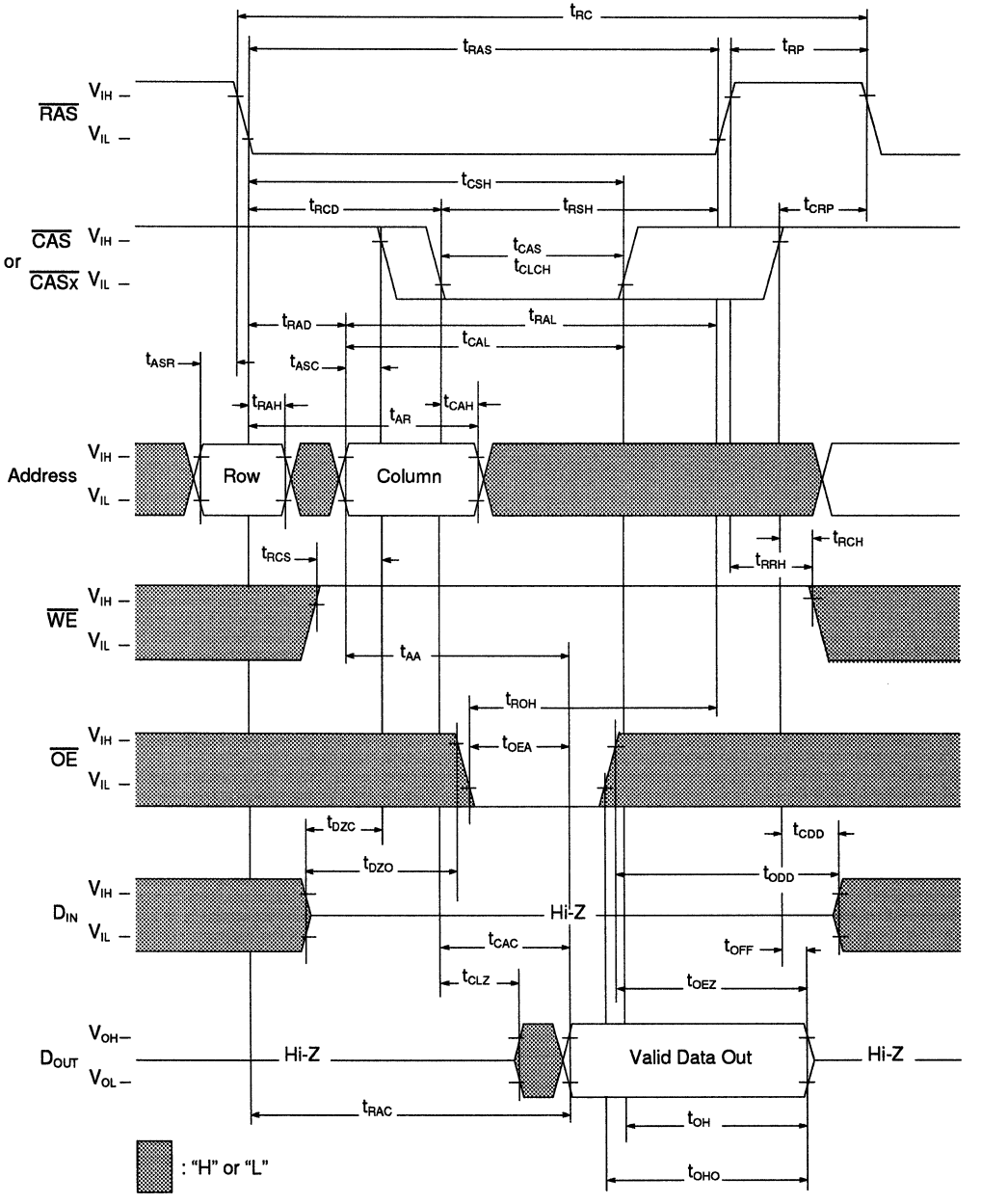
1. 1024 refreshes are required every 16ms.

Presence Detect Read Cycle

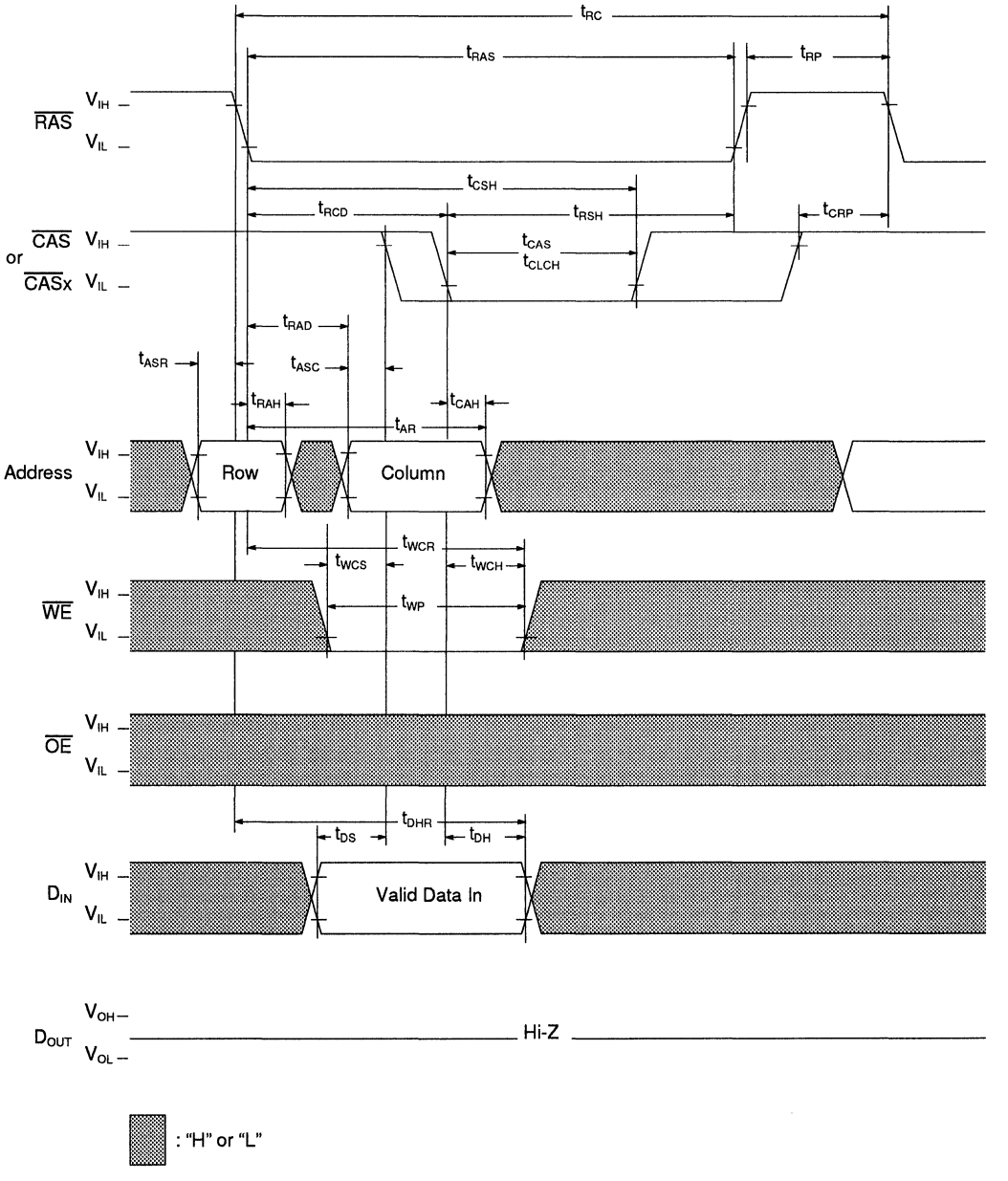
Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

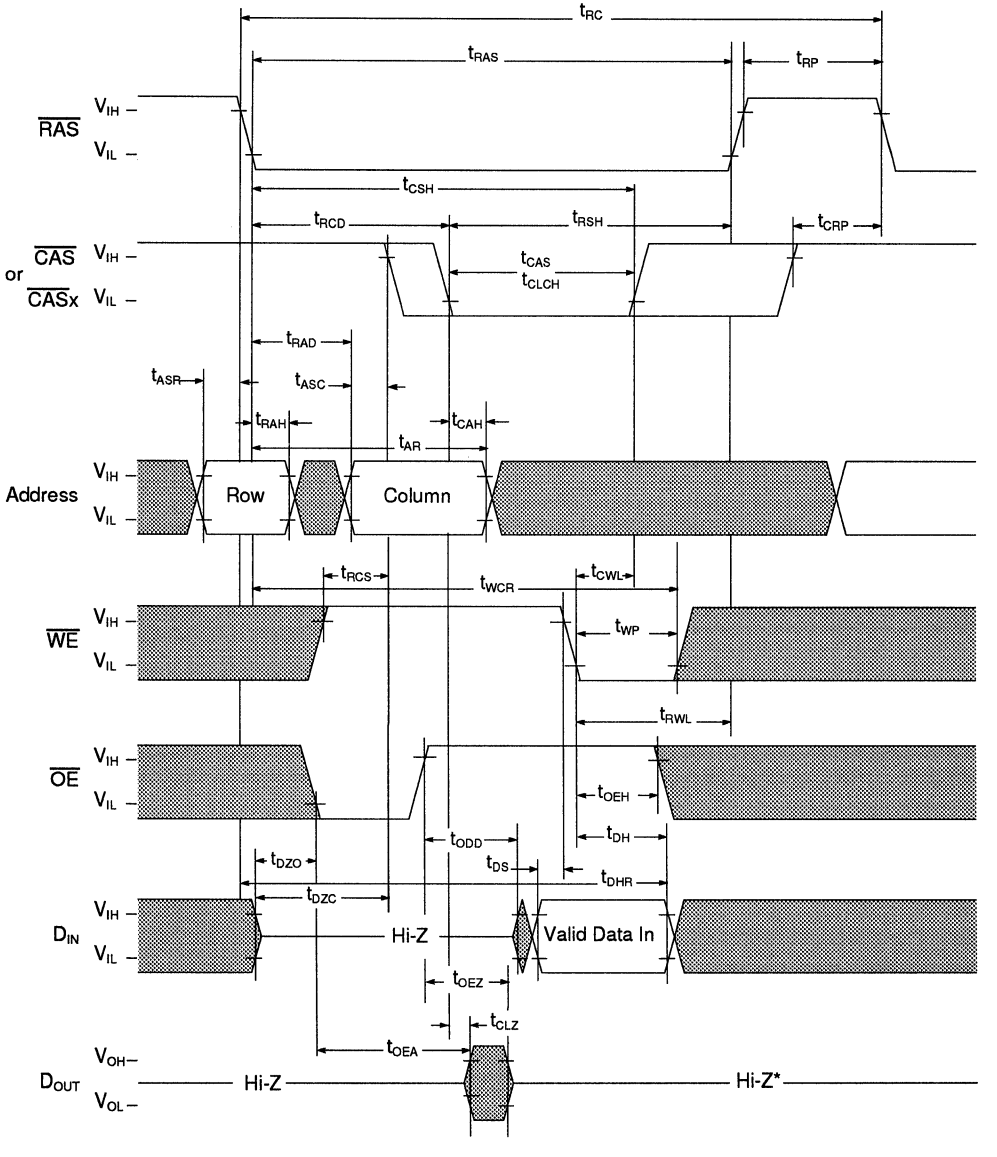
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
or
CASx
tCAS
tCLCH
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tAR
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
VOH
VOL
DOUT
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

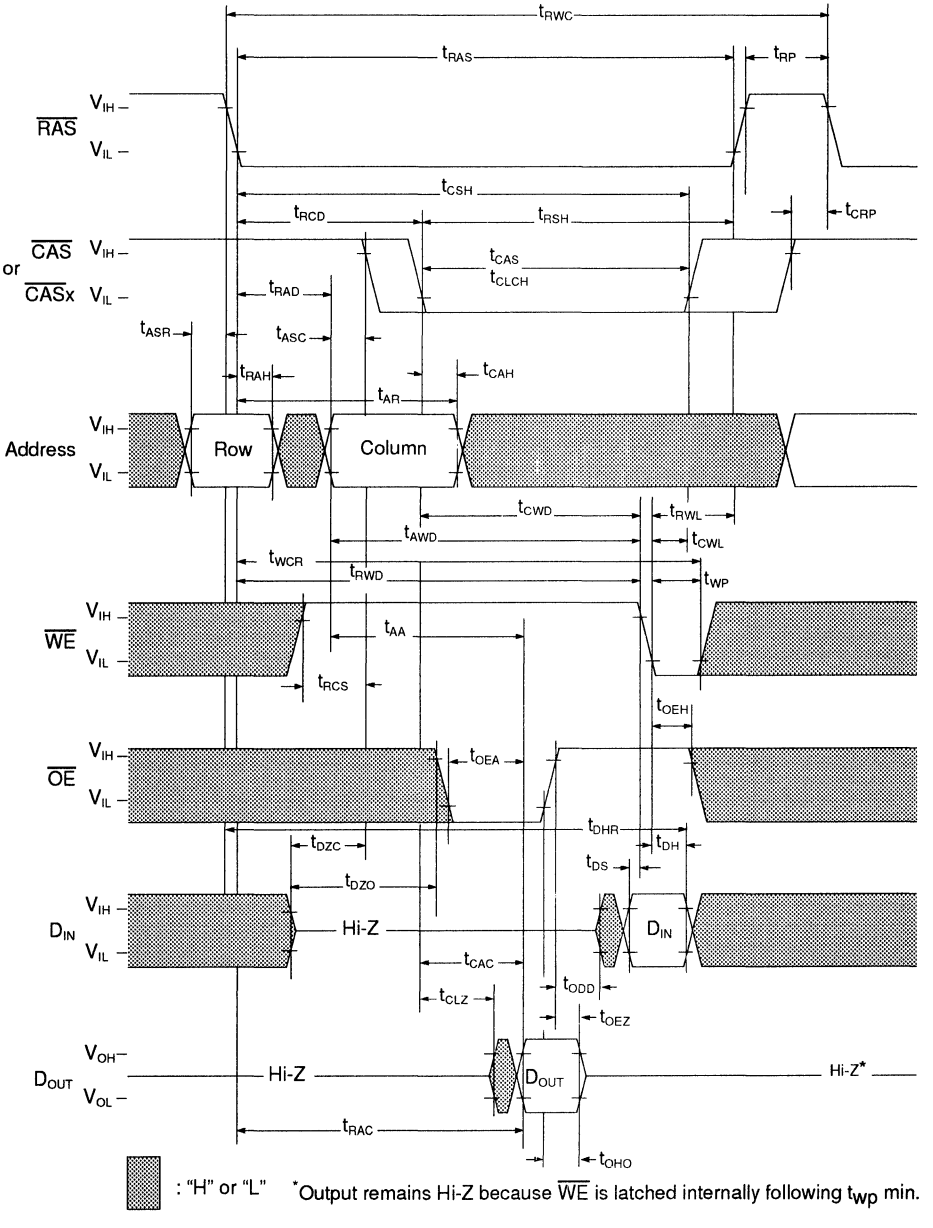


Write Cycle (Late Write)

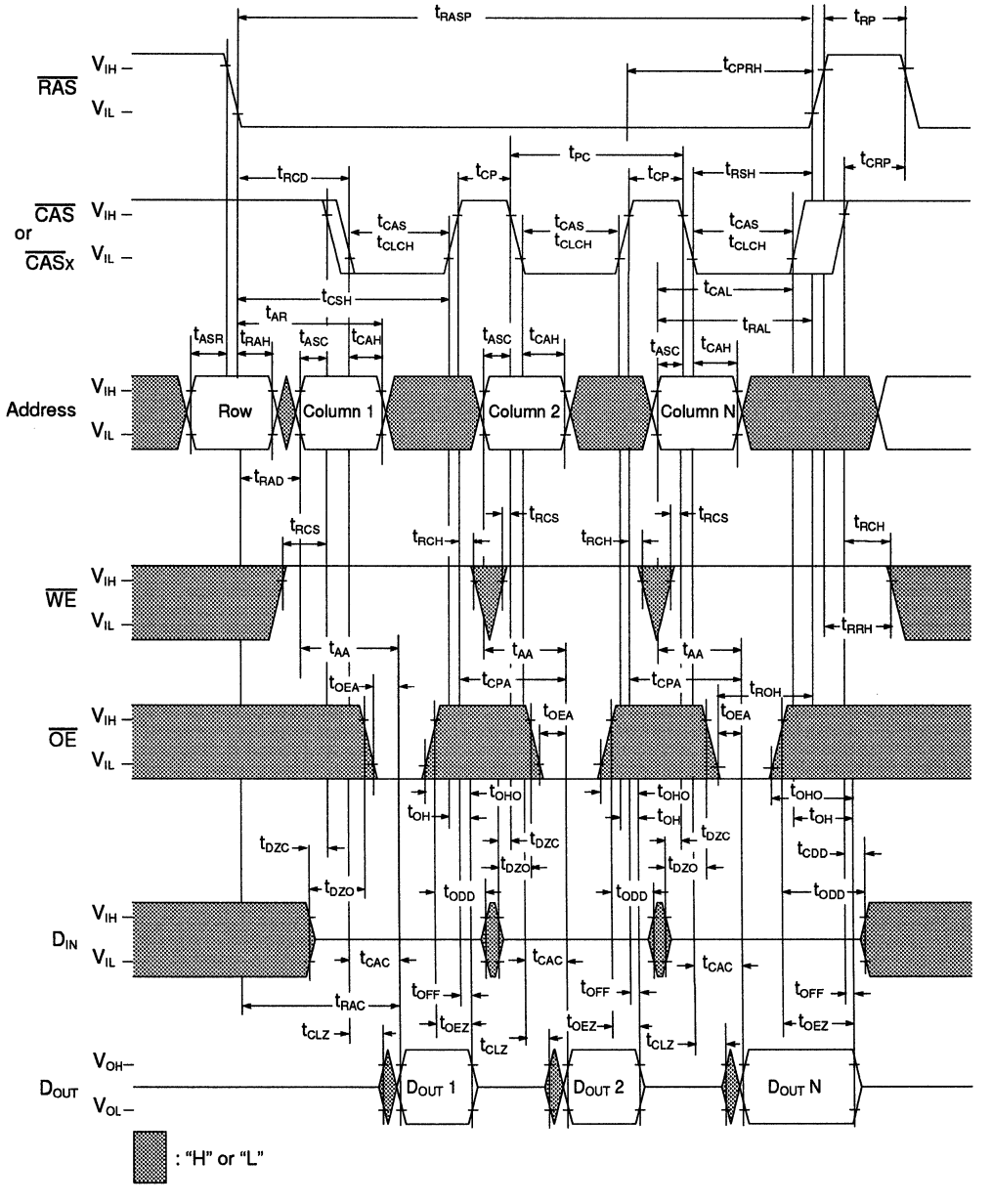


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

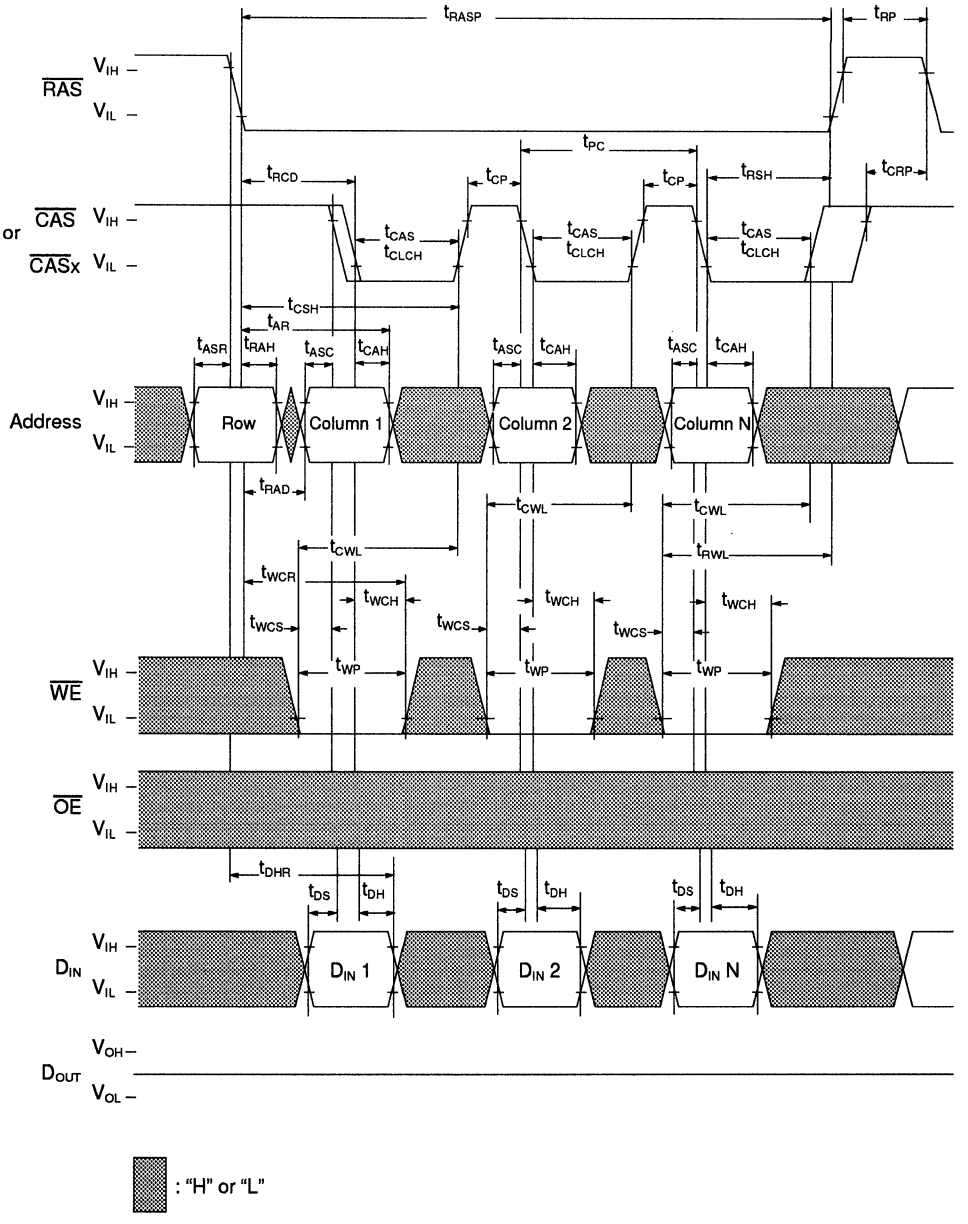
Read-Modify-Write-Cycle



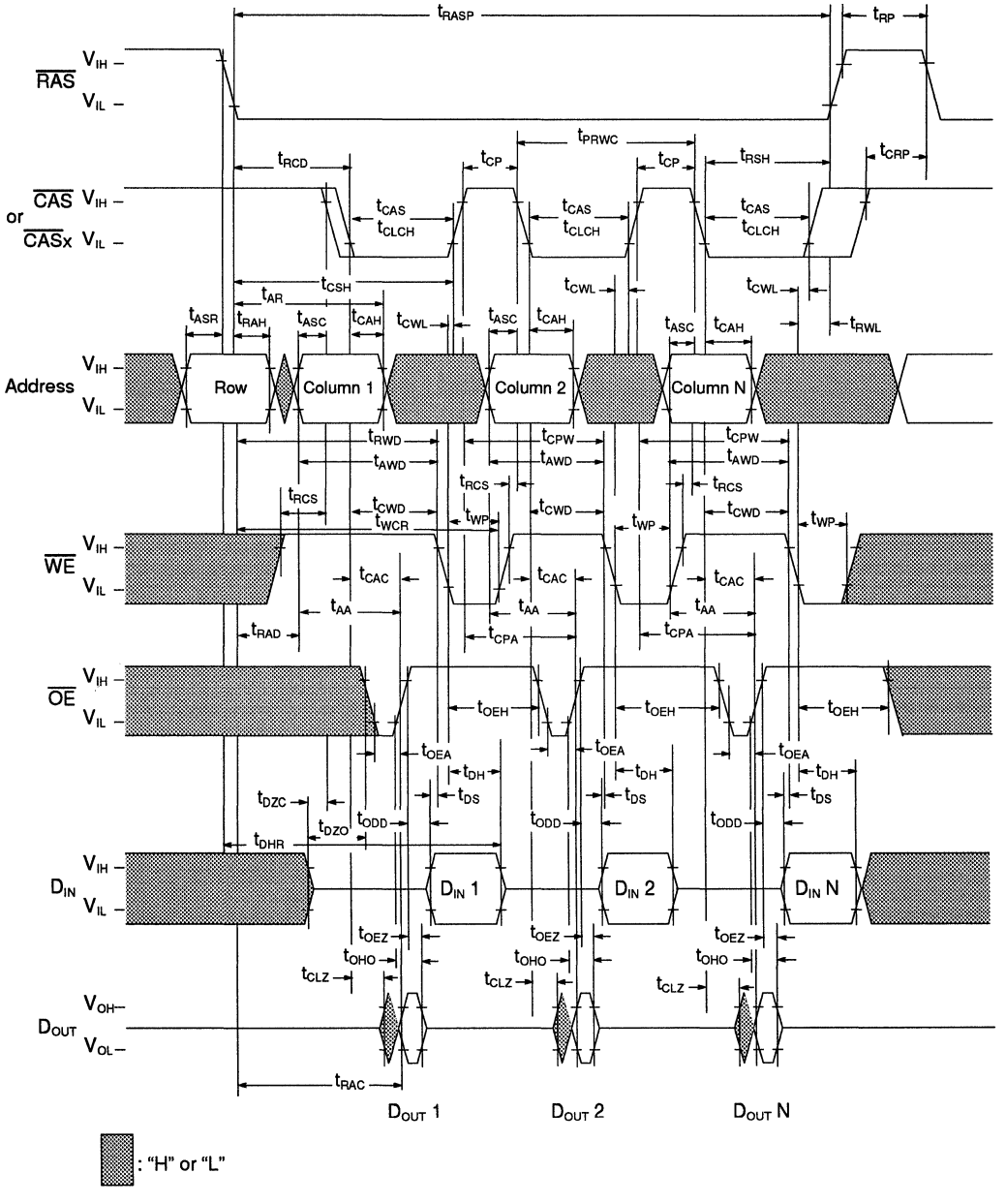
Fast Page Mode Read Cycle



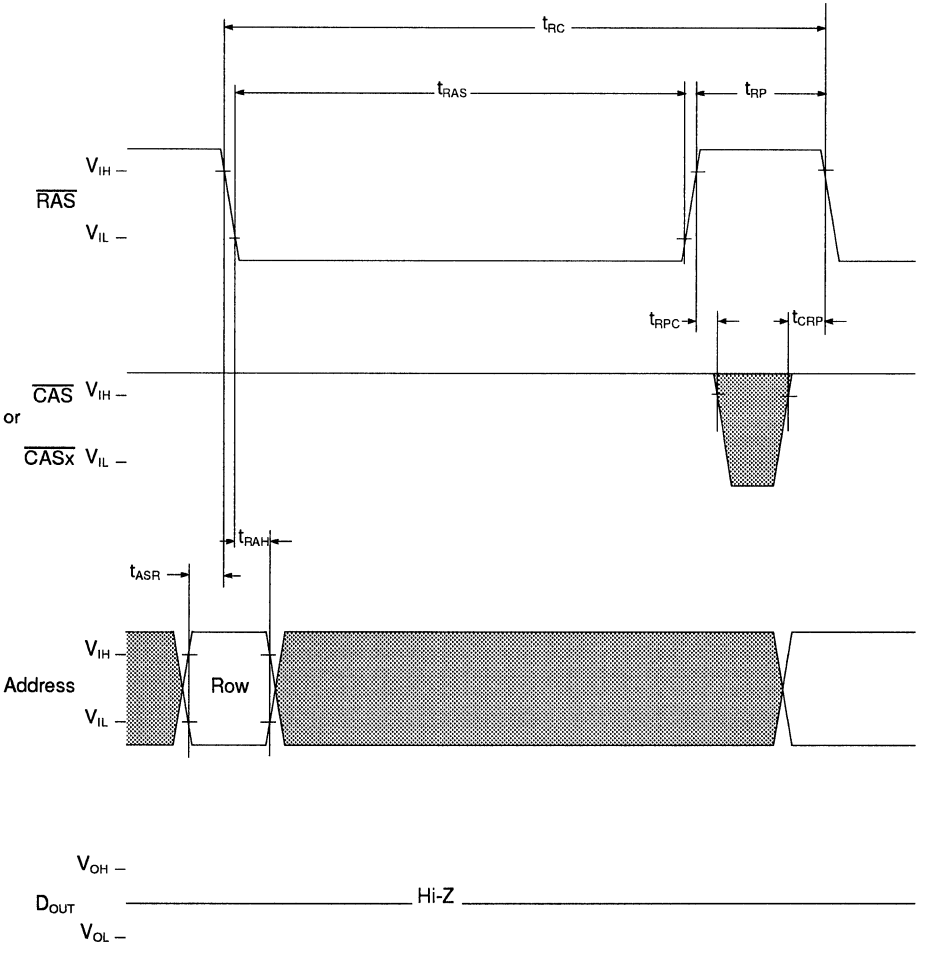
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

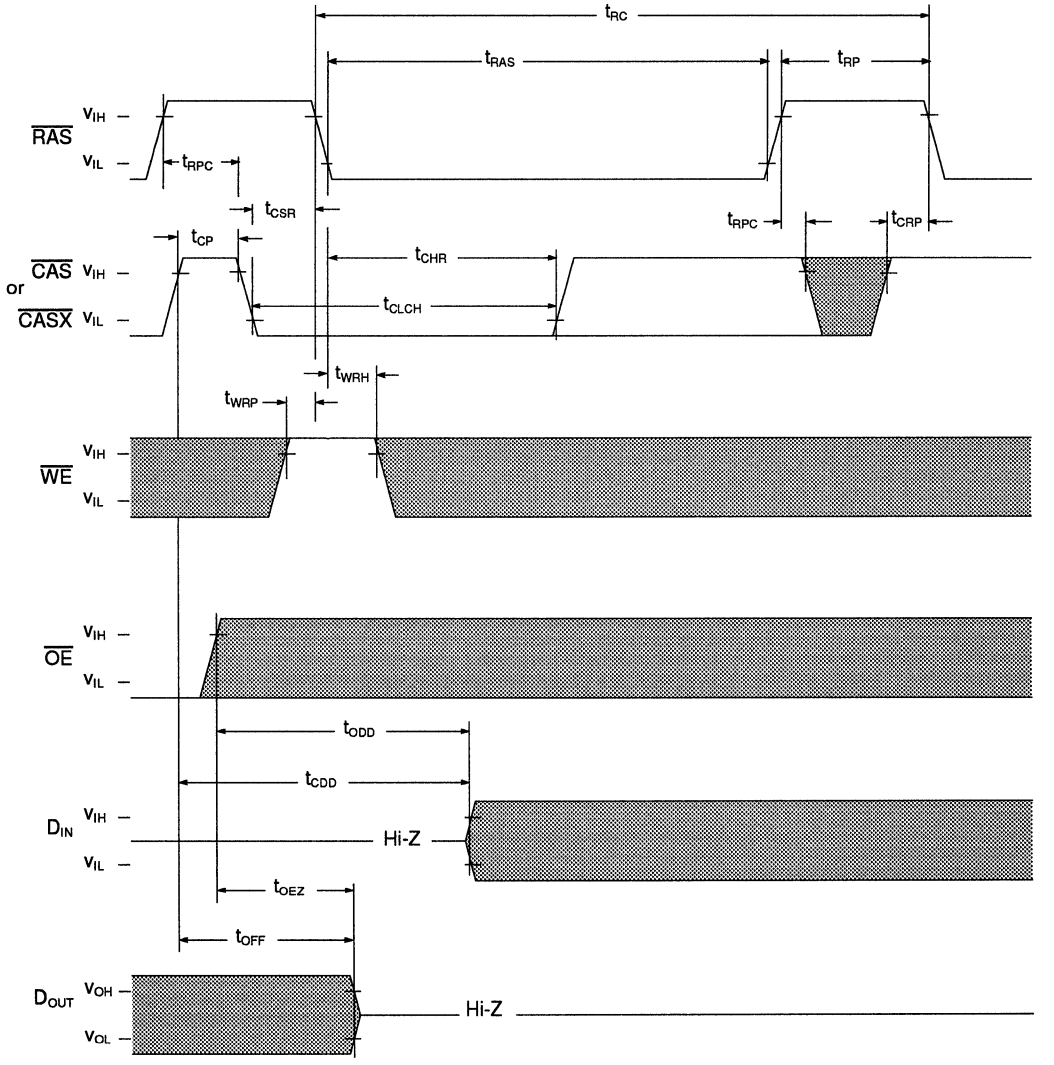


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

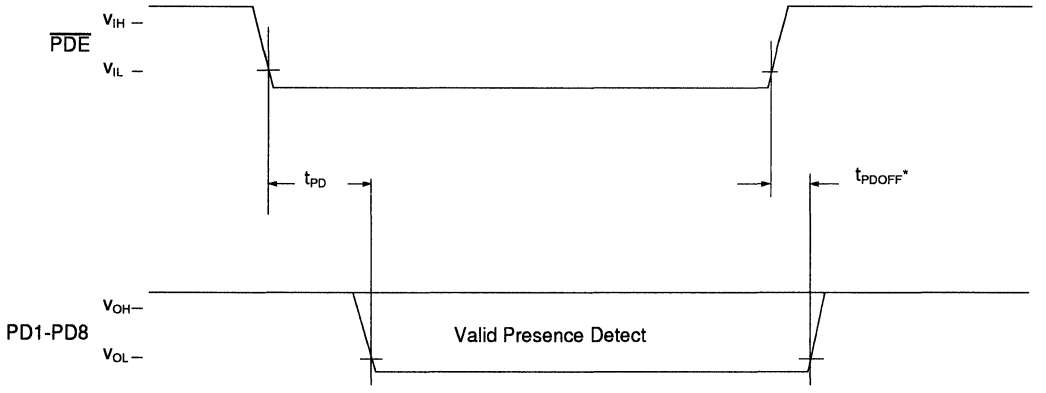
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



: "H" or "L"

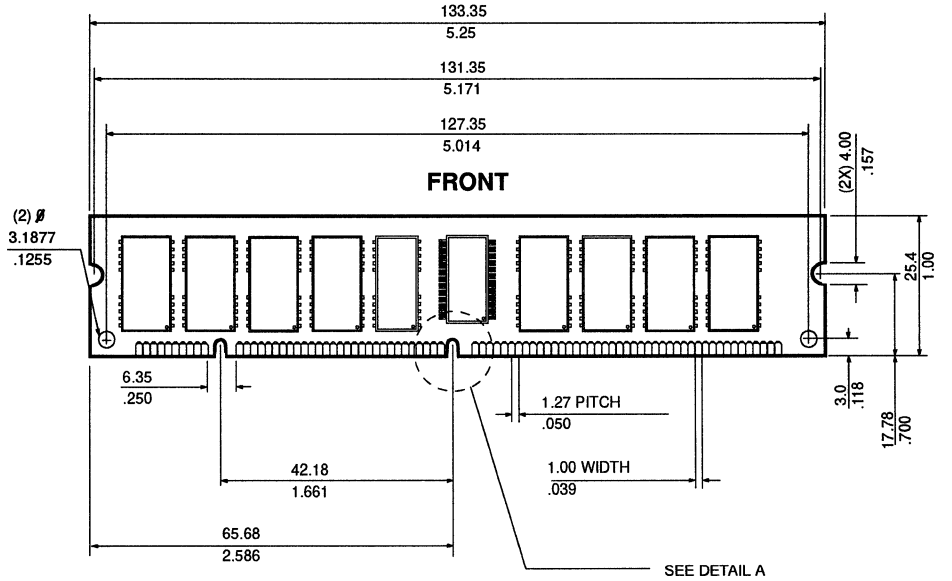
Note: Addresses are "H" or "L"

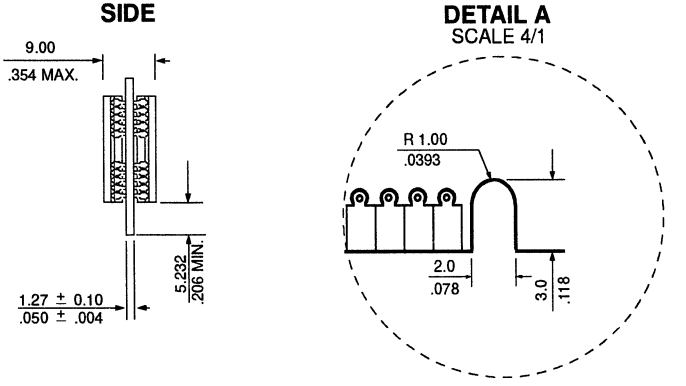
Presence Detect Read Cycle



*PD pins must be pulled high at next level of assembly

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 72 DRAM MODULE

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 2Mx72 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are fully TTL and CMOS compatible
- Single 5V, ± 0.5V Power Supply
- Au contacts
- Optimized for byte-write parity applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced Noise (32 V_{SS}/V_{CC} pins)
  - 4 Byte Interleave enabled
  - Byte write, byte read accesses
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 addressing (Row/Column)
- Card size: 5.25" x 1.0" x 0.157"
- DRAMS in TSOP Package

Description

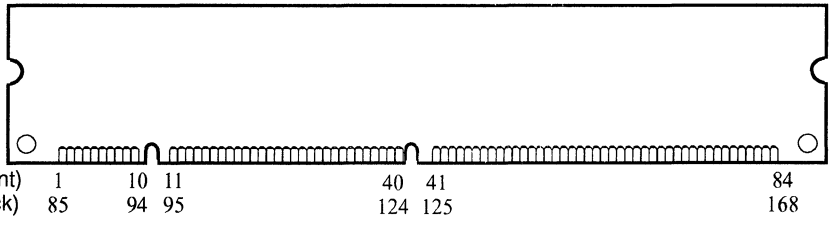
IBM11M2720L is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 2Mx72 high speed memory array and is configured as 2 1Mx72 banks. The DIMM uses 8 1Mx18 DRAMs in TSOP packages, and is intended for parity applications.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, if a x64 or x72 (ECC) DIMM were inserted into a bank of x72 parity DIMMs, IDO (grounded) would indicate that at least one DIMM in that memory bank will not function properly. PD8 would indicate what positions, if any, contained an ECC DIMM.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 non-parity (5V) and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A9	Address Inputs (Buffered)
DQx	Data Input/output
PQx	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

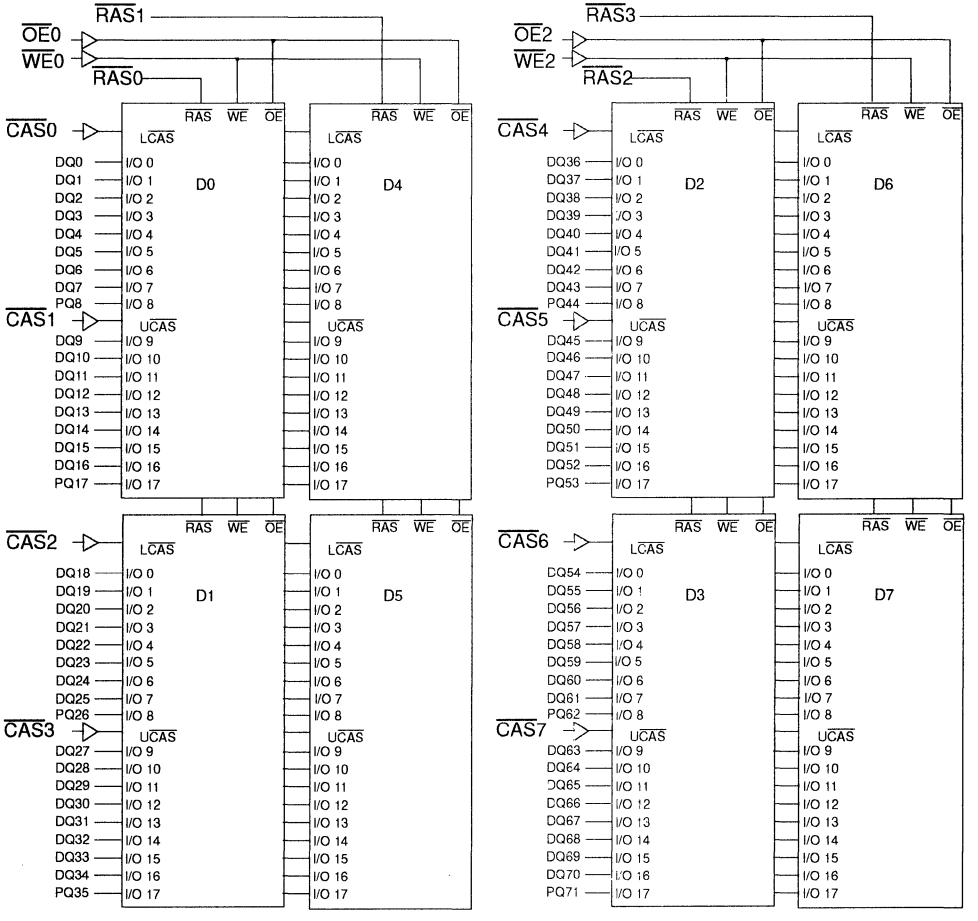
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	$\overline{RAS3}$
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	$\overline{CAS5}$
5	DQ3	89	DQ39	47	$\overline{CAS6}$	131	$\overline{CAS7}$
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	PQ8	95	PQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	PQ17	106	PQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	PQ26	150	PQ62
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	$\overline{CAS1}$	70	DQ29	154	DQ65
29	$\overline{CAS2}$	113	$\overline{CAS3}$	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	$\overline{RAS1}$	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	PQ35	161	PQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	NC	122	NC	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M2720LA-60	2Mx72	60ns	Au	5.25"x1.0"x0.157"	
IBM11M2720LA-70	2Mx72	70ns	Au	5.25"x1.0"x0.157"	

Block Diagram



V_{SS} / $\overline{PDE}$ → PD 1-8
(when = 0, 1=NC)

A1 - AN → A1-AN: DRAMS D0 - D7
A0 → A0: DRAMS D0,D1,D4,D5
B0 → A0: DRAMS D2,D3,D6,D7

V_{CC} → D0 - D7, Buffers
V_{SS} → D0 - D7, Buffers

Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx, PQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	1	1
PD2	0	0
PD3	1	1
PD4	0	0
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	1	1
ID0 (DIMM Type/Width)	1	1
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} +0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} +0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	9.25	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A9)	13	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	25	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF	
C_{I4}	DQ_X Capacitance	22	pF	
C_{I5}	PQ_X Capacitance	22	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	848	mA	1, 2, 3
		-70	—	748		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	16	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	848	mA	1, 3, 4
		-70	—	748		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	368	mA	1, 2, 3
		-70	—	328		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	8	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	848	mA	1, 3, 4
		-70	—	748		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. Refresh current is specified for 1 bank.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the Dram device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	1
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	2
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	3
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	4
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	5
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	—	6
t_{CLCH}	Hold Time from $\overline{CAS}$ Low to $\overline{CAS}$ High	10	—	10	—	ns	7
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
2. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
3. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
4. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
5. Either t_{CDD} or t_{ODD} must be satisfied.
6. This timing parameter is not applicable to this product, but applies to a related product in this family.
7. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	2	—	2	—	ns	3
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	3
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1,2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1,2
t_{AA}	Access Time from Address	—	36	—	41	ns	1,2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1,2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Access to $\overline{CAS}$ Lead Time	36	—	41	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	—	—	—	—	ns	4
t_{OH}	Output Data Hold tIme	2	—	2	—	ns	
t_{OHO}	Output Data Hold from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1,2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	63	—	73	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

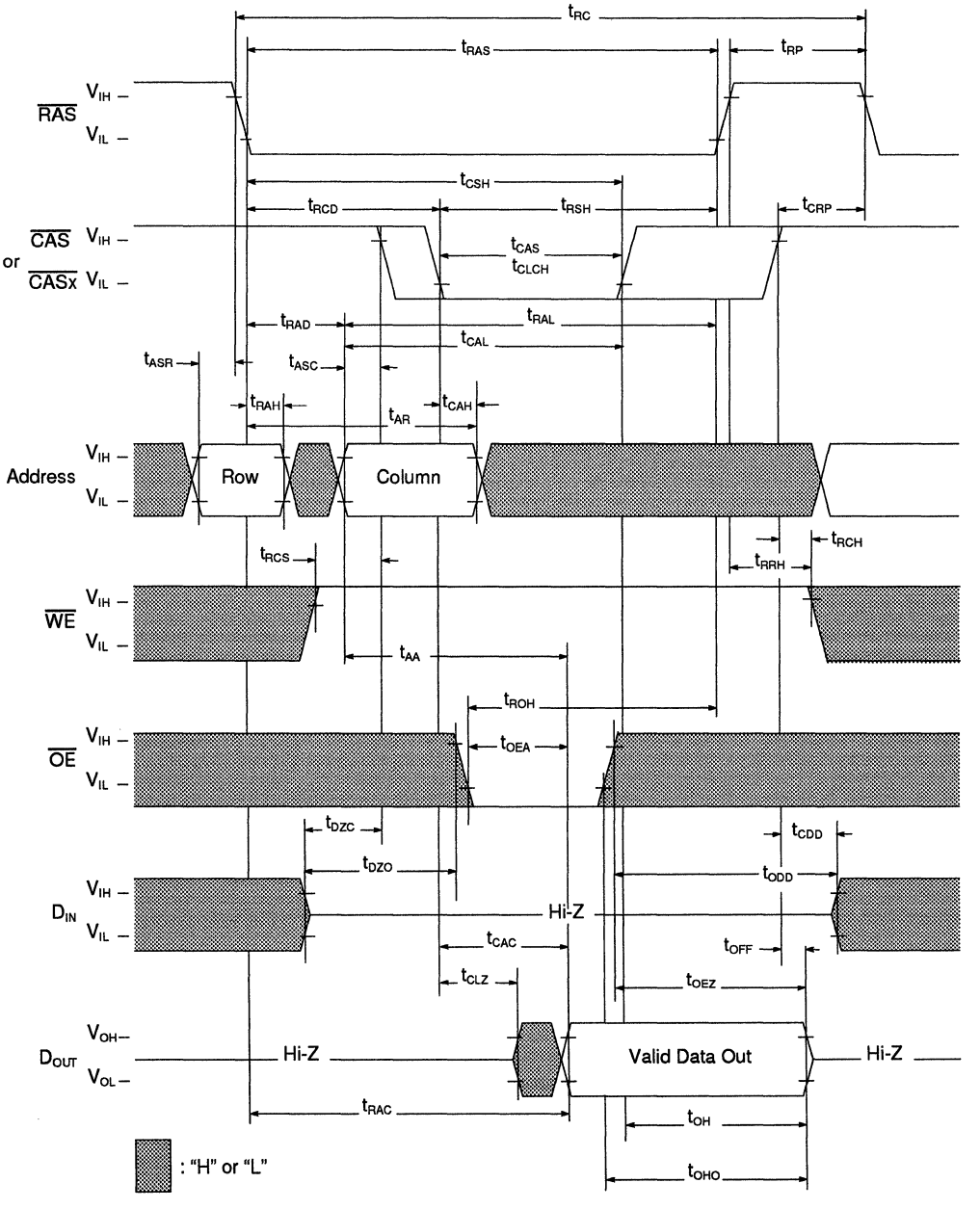
1. 1024 refreshes are required every 16ms.

Presence Detect Read Cycle

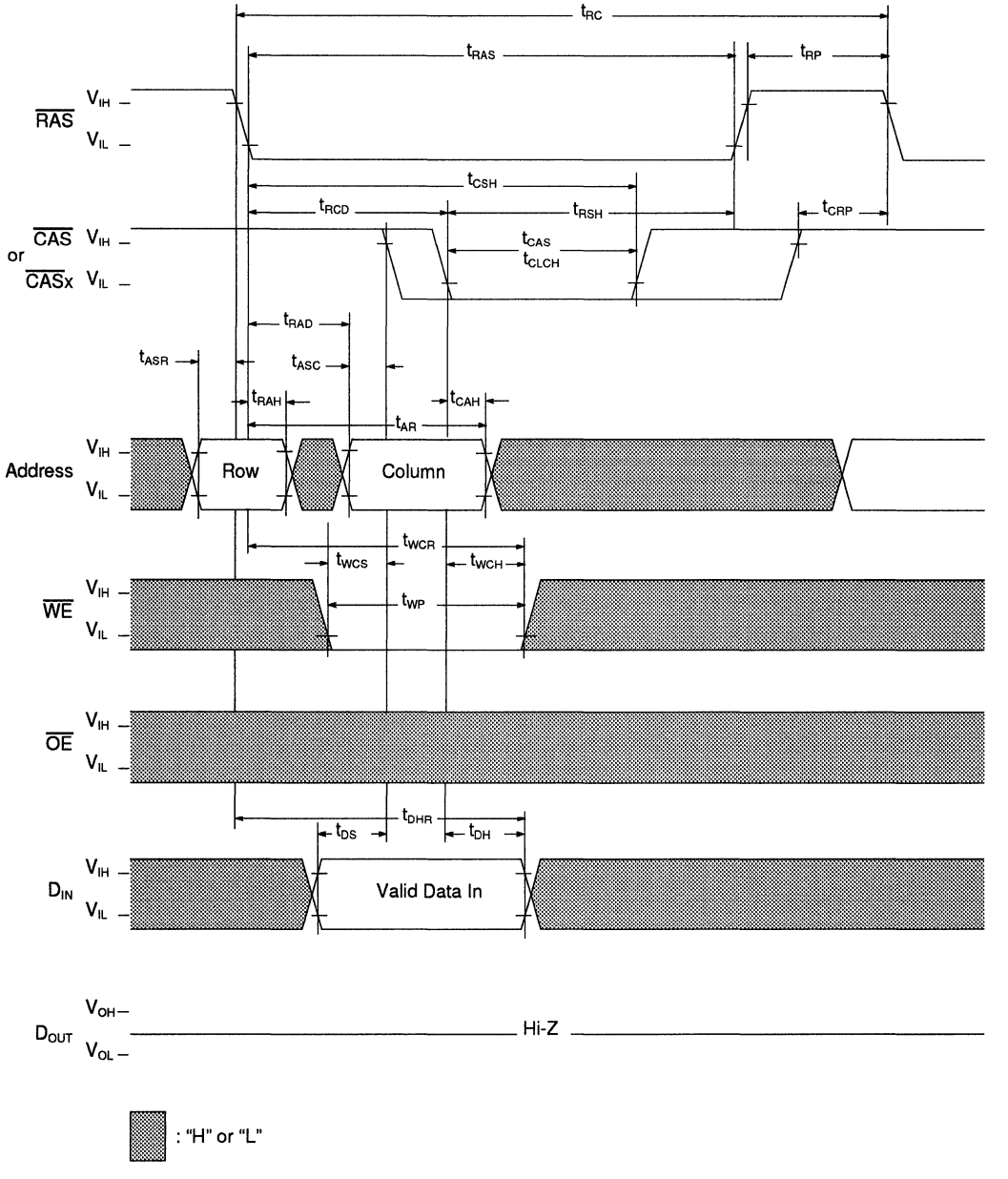
Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

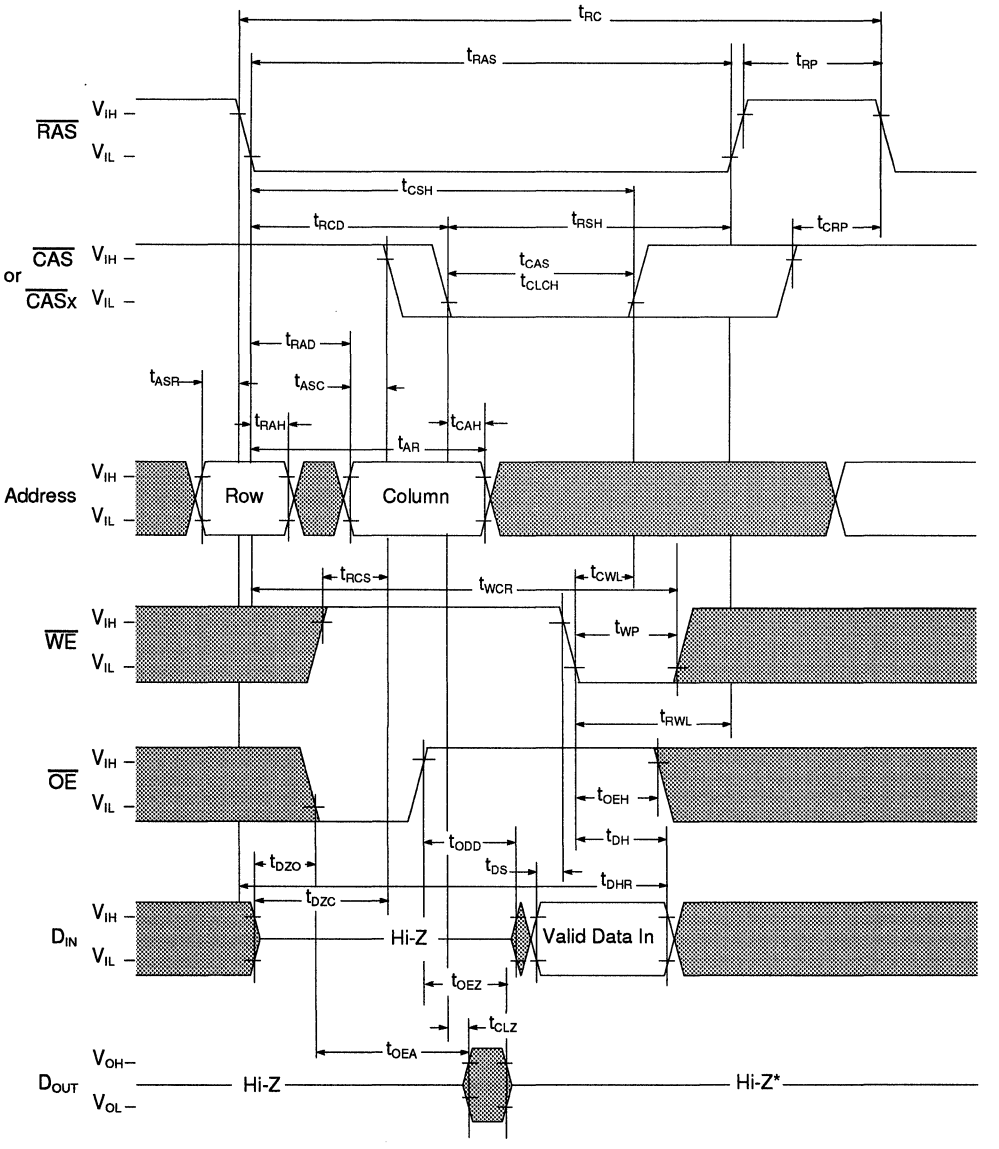
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
or
CASx
tCAS
tCLCH
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tCAH
tAR
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
VOH
VOL
DOUT
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

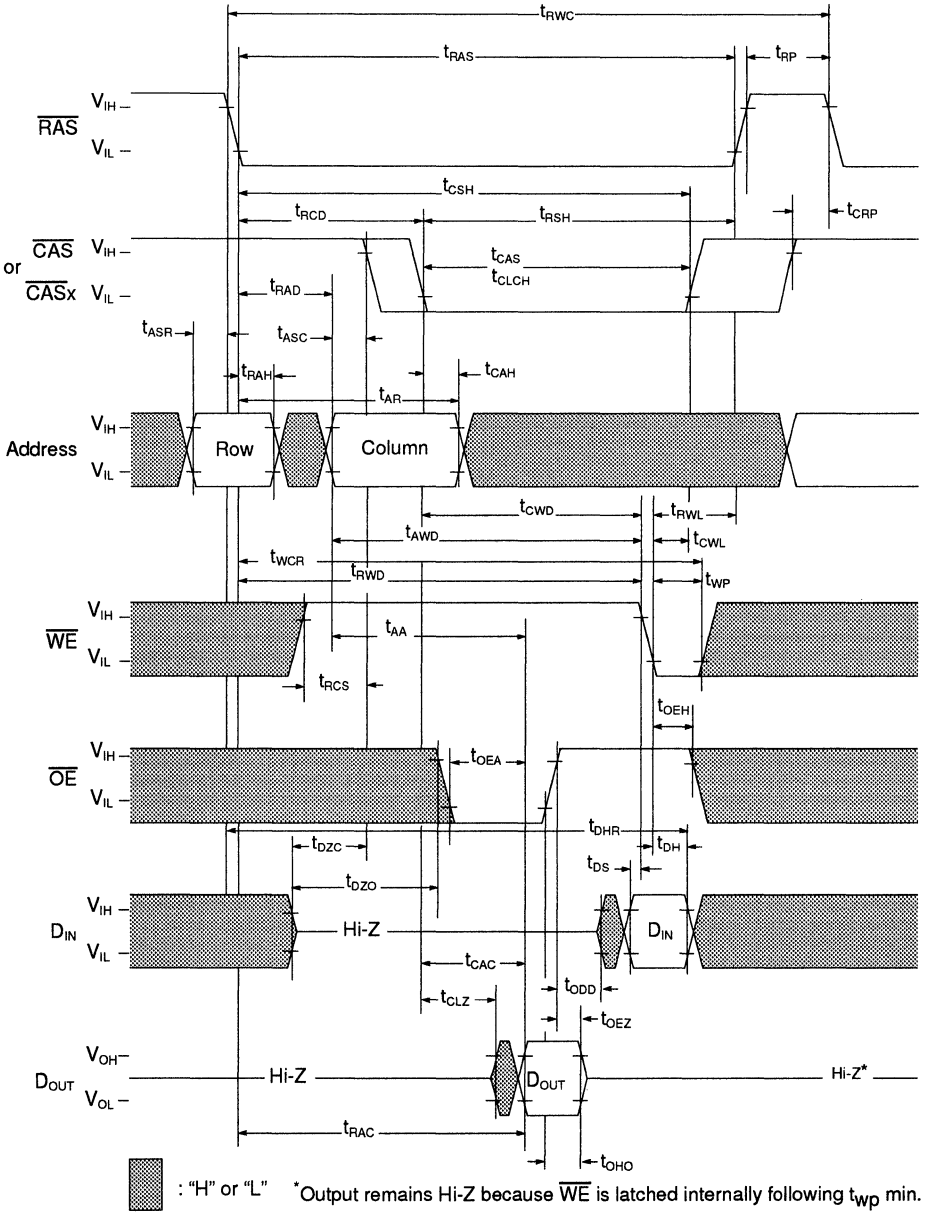


Write Cycle (Late Write)

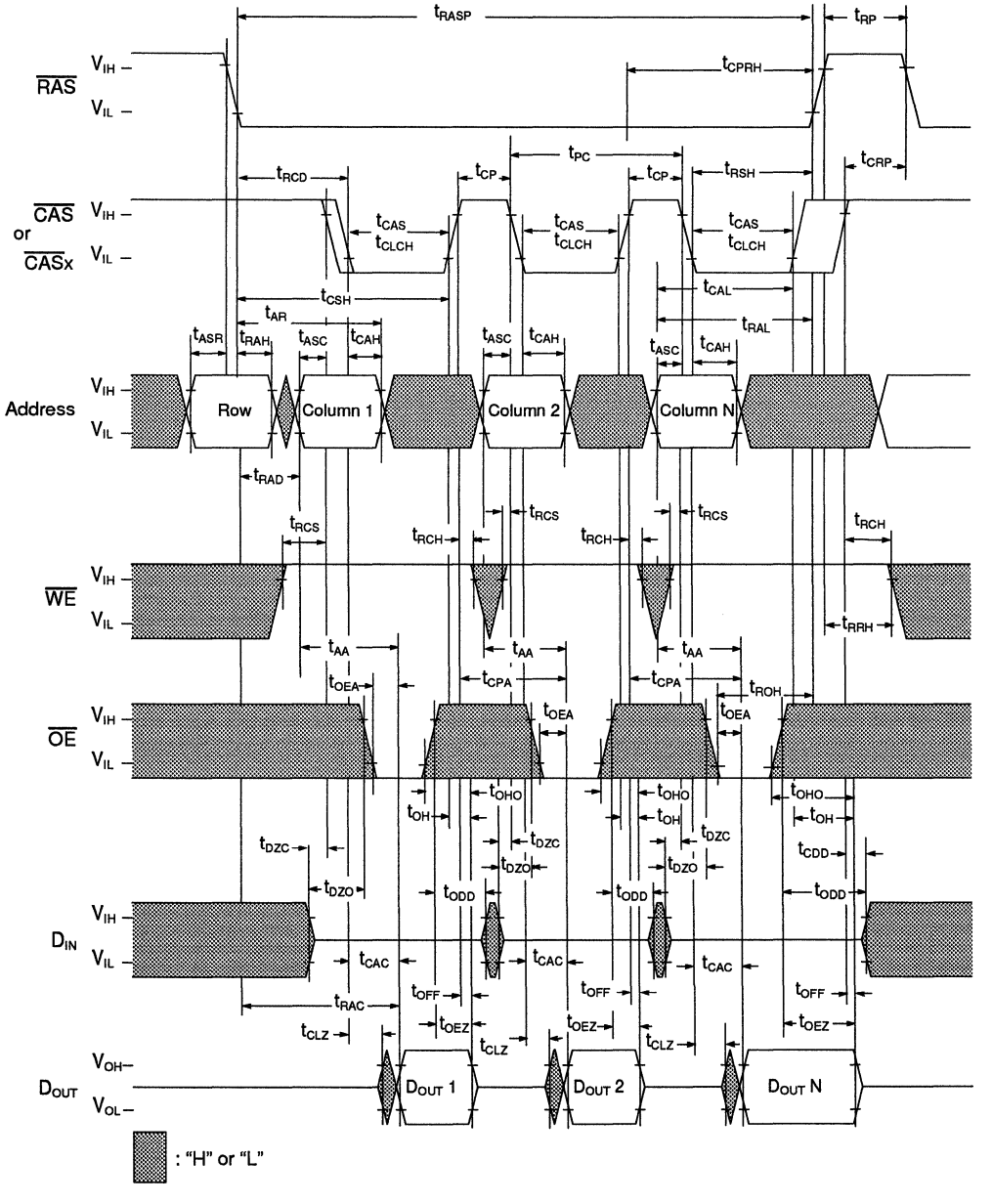


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

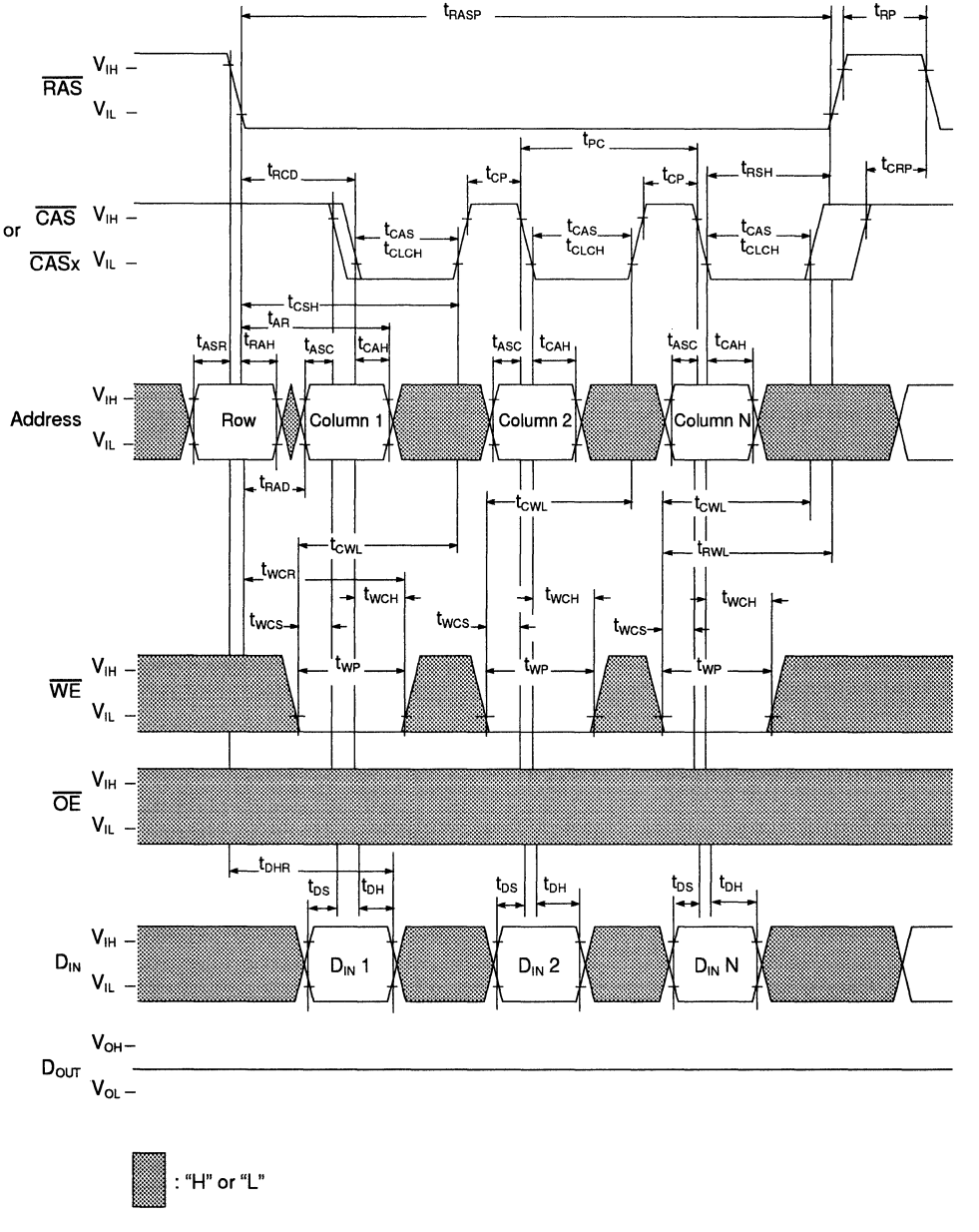
Read-Modify-Write-Cycle



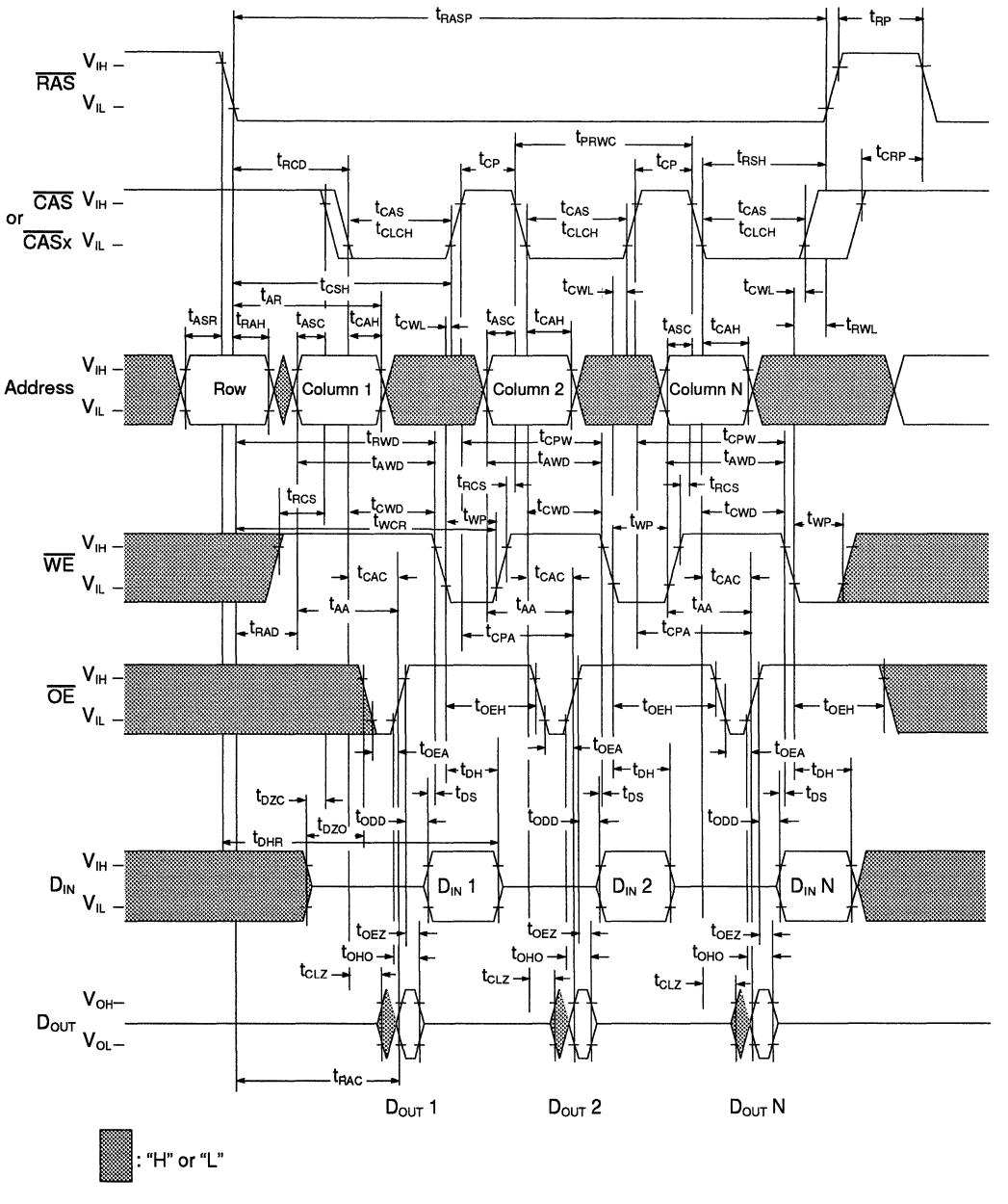
Fast Page Mode Read Cycle



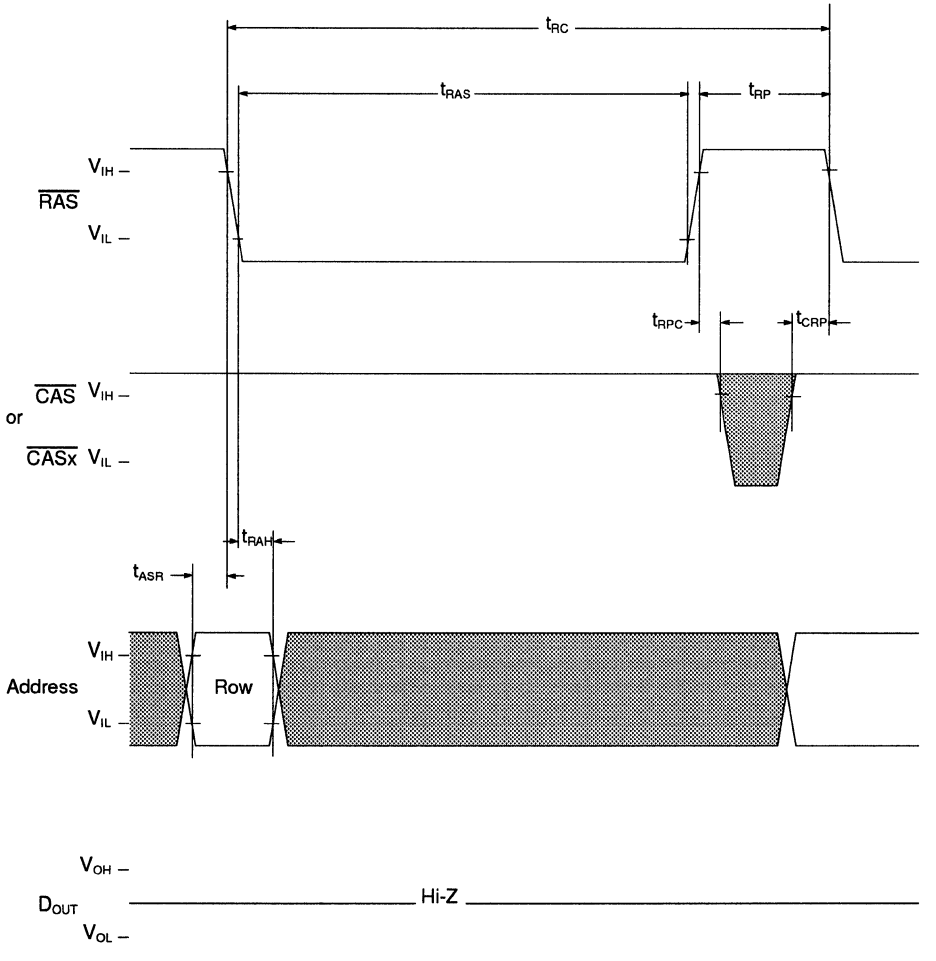
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

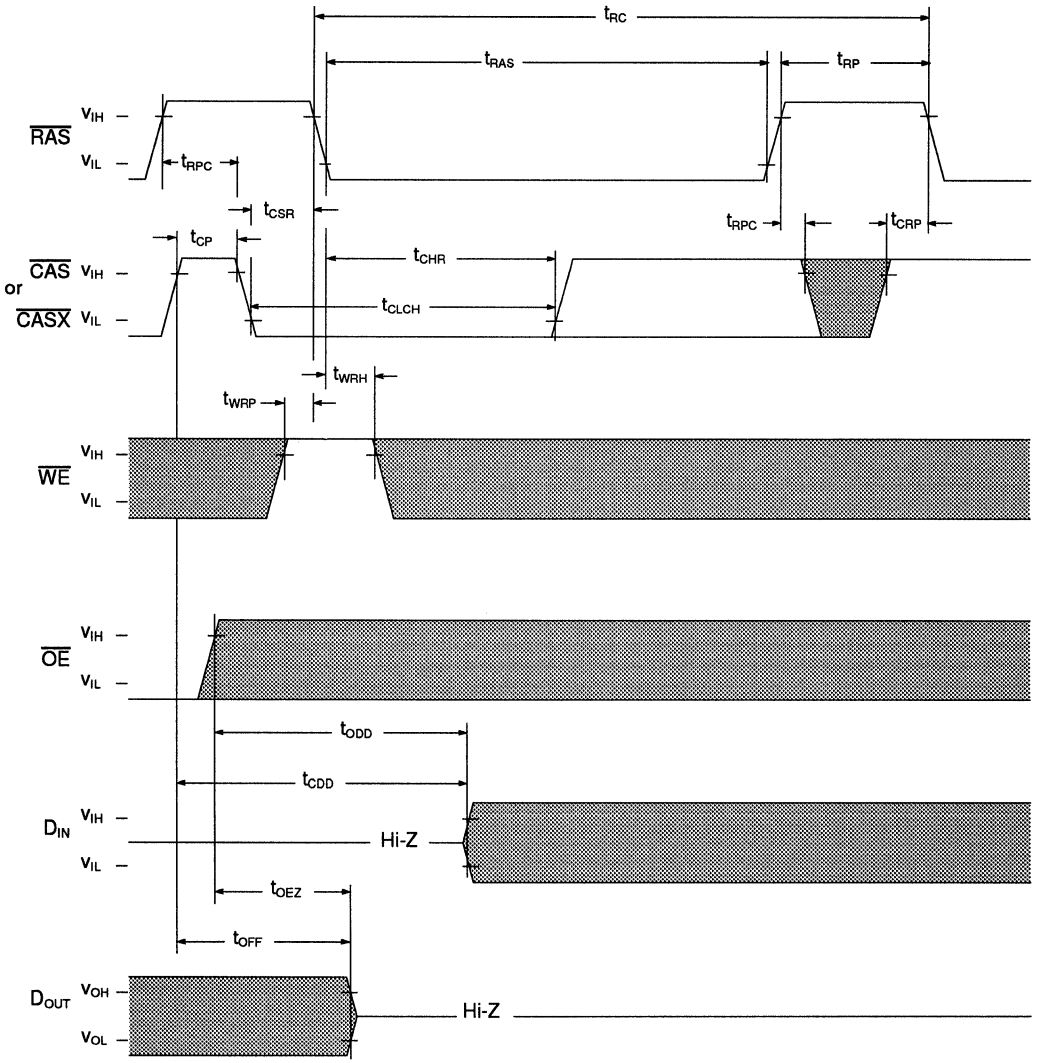


$\overline{RAS}$ Only Refresh Cycle



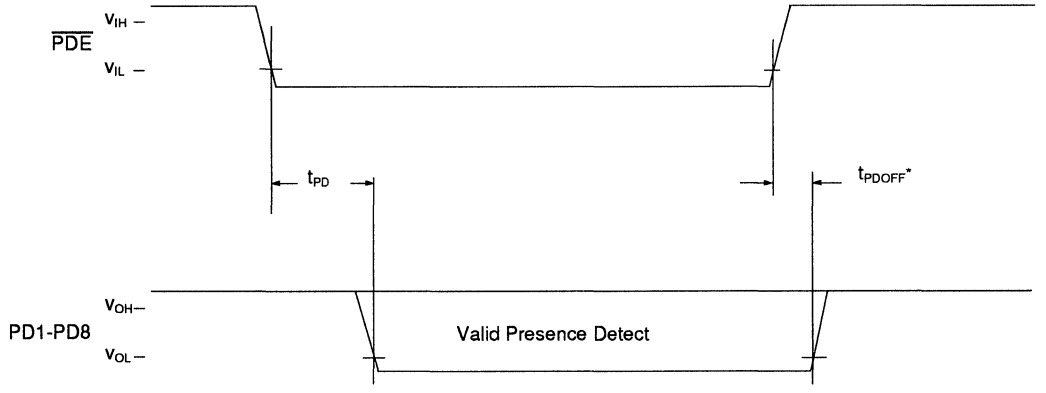
Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



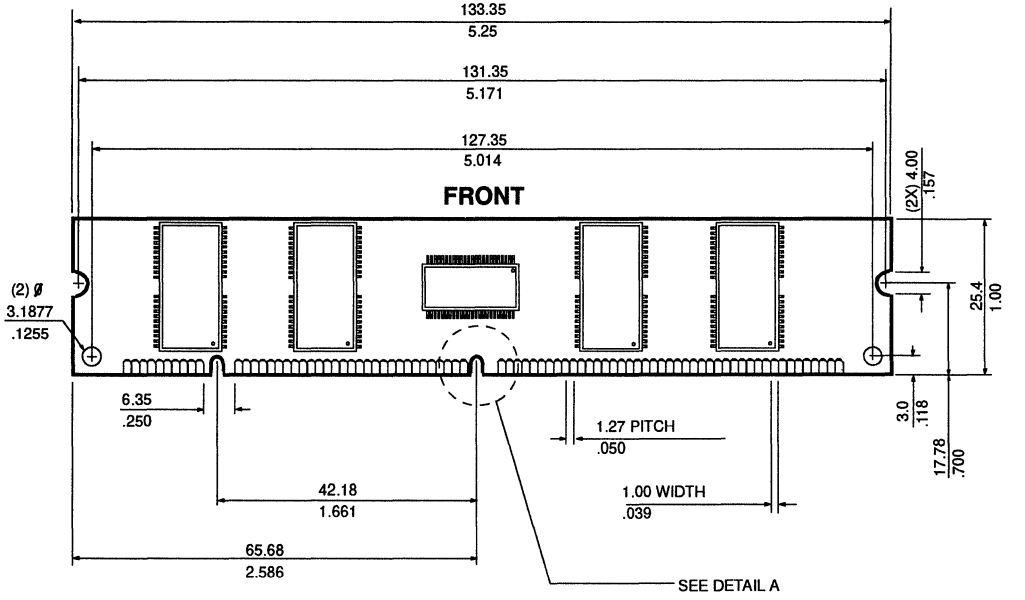
Note: Addresses are "H" or "L"

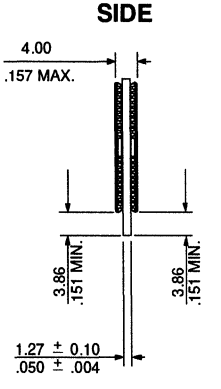
Presence Detect Read Cycle

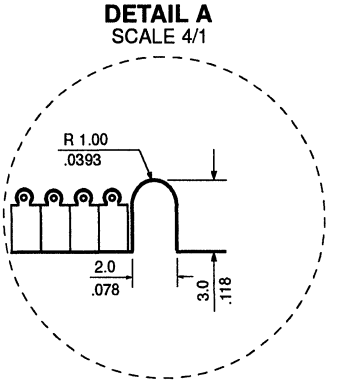


*PD pins must be pulled high at next level of assembly

Layout Drawing







NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

4M x 72 DRAM MODULE

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 4Mx72 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are fully TTL and CMOS compatible
- Single 5V, ± 0.5V Power Supply
- Au contacts
- Optimized for byte-write parity applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - 4 Byte Interleave enabled
  - Byte write, byte read accesses
  - Buffered PDs
- Fast Page Mode
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 4096 refresh cycles distributed across 64ms
- 12/11 (redundant) addressing (Row/Column)
- Card size: 5.25" x 1.2" x 0.354"
- DRAMS in SOJ Package

Description

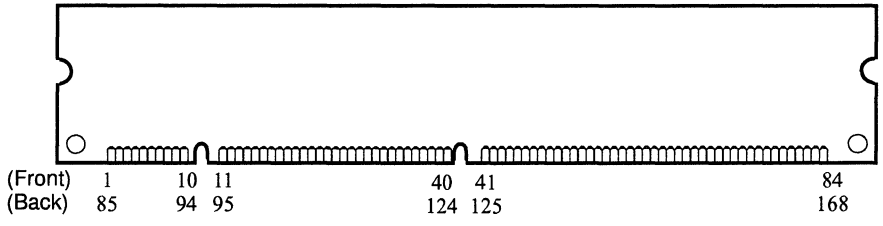
IBM11M4720D is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 4Mx72 high speed memory array for parity applications. The DIMM uses 16 4Mx4 (12/10 addressed) DRAMs and 8 4Mx1 (11/11 addressed) DRAMs in SOJ packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, if a x64 or x72 (ECC) DIMM were inserted into a bank of x72 parity DIMMs, IDO (grounded) would indicate that at least one DIMM in that memory bank will not function properly. PD8 would indicate what positions, if any, contained an ECC DIMM.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 non-parity (5V) and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS}0$, $\overline{RAS}2$	Row Address Strobe
$\overline{CAS}0$ - $\overline{CAS}7$	Column Address Strobe (Buffered)
$\overline{WE}0$, $\overline{WE}2$	Read/write Input (Buffered)
$\overline{OE}0$, $\overline{OE}2$	Output Enable (Buffered)
A0, B0, A1 - A11	Address Inputs (Buffered)
DQx	Data Input/output
PQx	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

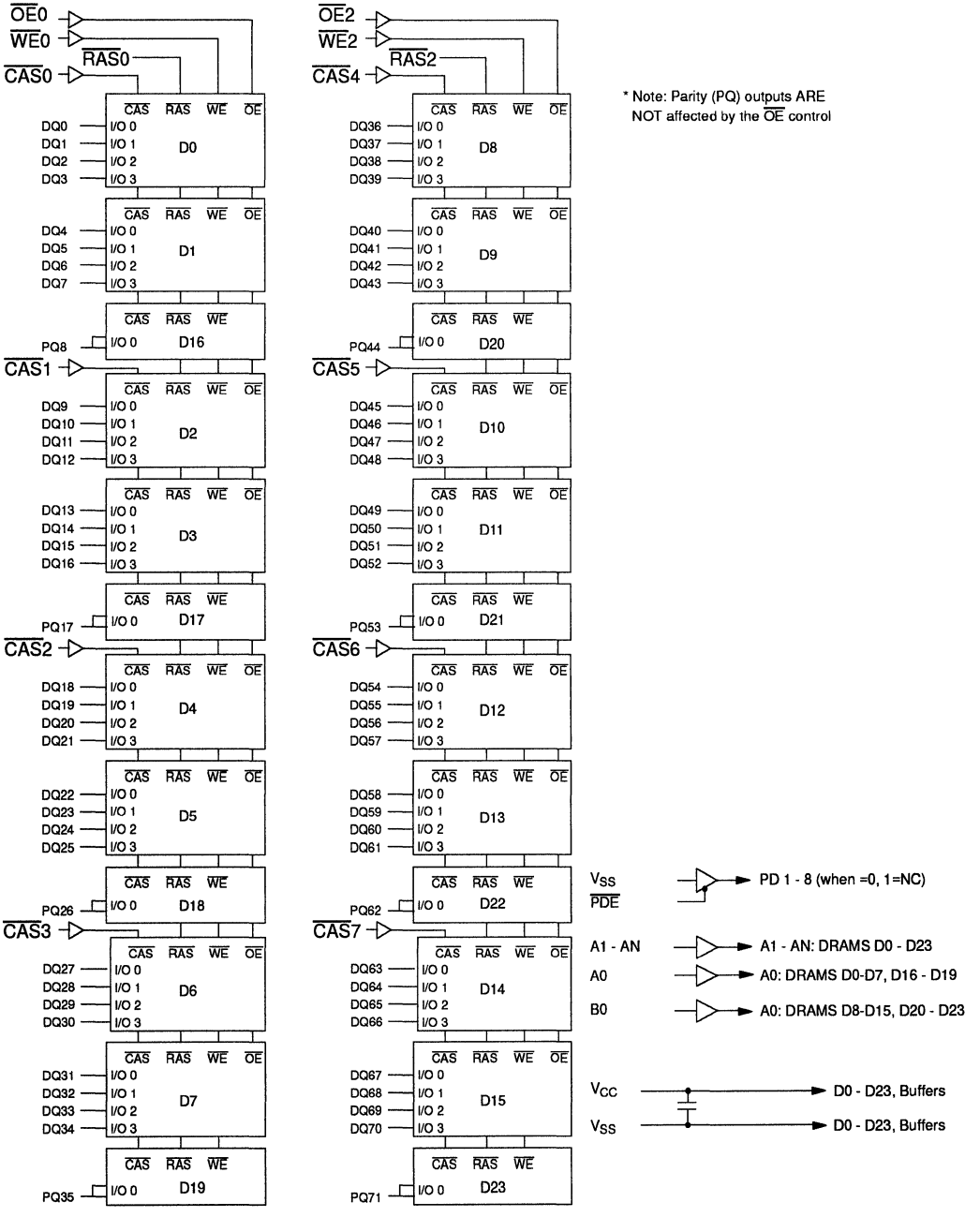
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE}2$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS}2$	129	NC
4	DQ2	88	DQ38	46	$\overline{CAS}4$	130	$\overline{CAS}5$
5	DQ3	89	DQ39	47	$\overline{CAS}6$	131	$\overline{CAS}7$
6	V_{CC}	90	V_{CC}	48	$\overline{WE}2$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	PQ8	95	PQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	PQ17	106	PQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	PQ26	150	PQ62
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE}0$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS}0$	112	$\overline{CAS}1$	70	DQ29	154	DQ65
29	$\overline{CAS}2$	113	$\overline{CAS}3$	71	DQ30	155	DQ66
30	$\overline{RAS}0$	114	NC	72	DQ31	156	DQ67
31	$\overline{OE}0$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	PQ35	161	PQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	A10	122	A11	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M4720DA-60	4Mx72	60ns	Au	5.25"x1.2"x0.354"	
IBM11M4720DA-70	4Mx72	70ns	Au	5.25"x1.2"x0.354"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx, PQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	1	1
PD2	1	1
PD3	0	0
PD4	1	1
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	1	1
ID0 (DIMM Type/Width)	1	1
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} +0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} +0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	12.3	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A11)	13	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	90	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF	
C_{I4}	DQ_X Capacitance	15	pF	
C_{I5}	PQ_X Capacitance	20	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	2240	mA	1,2,3
		-70	—	2000		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	48	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	2240	mA	1,3
		-70	—	2000		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1840	mA	1,2,3
		-70	—	1600		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	24	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	2240	mA	1,3
		-70	—	2000		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-120	+120		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the Dram device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	1
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	4, 5
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	5
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	57	—	62	—	—	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
2. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.
5. $\overline{OE}$ has no effect on Parity (PQx) bits.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	2	—	2	—	ns	2
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	47	—	57	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	2
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	2

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	36	—	41	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1, 2, 3
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	4
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	4
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Access to $\overline{CAS}$ Lead Time	36	—	41	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	—	—	—	—	ns	5
t_{OH}	Output Data Hold tIme	2	—	2	—	ns	
t_{OHO}	Output Data Hold from $\overline{OE}$	2	—	2	—	ns	3
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	3, 6
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	7
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	6

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. $\overline{OE}$ has no effect on Parity (PQx) bits.
4. Either t_{RCH} or t_{RRH} must be satisfied.
5. This timing parameter is not applicable to this product, but applies to a related product in this family.
6. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1,2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	64	—	64	ms	1

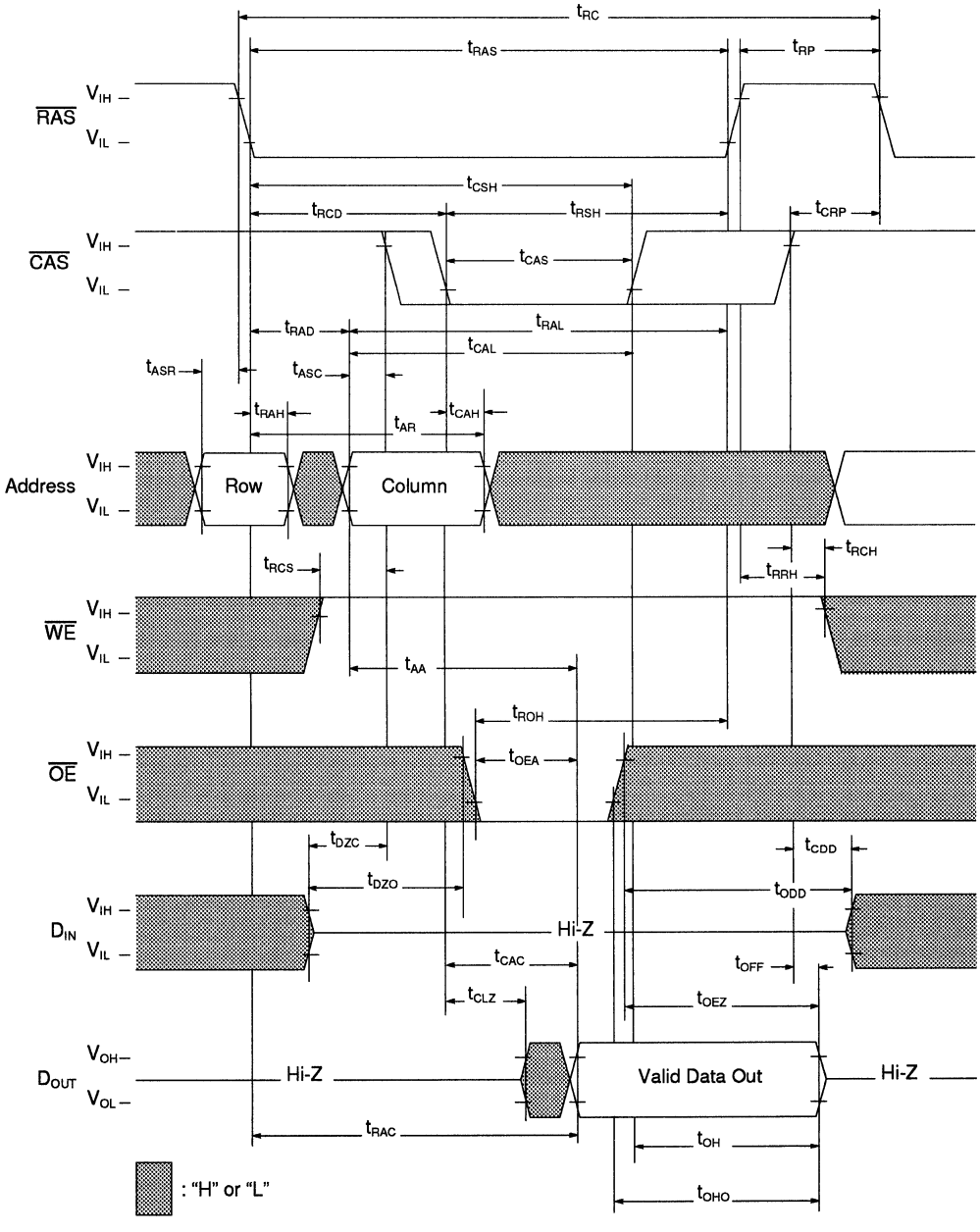
1. 4096 refreshes are required every 64ms.

Presence Detect Read Cycle

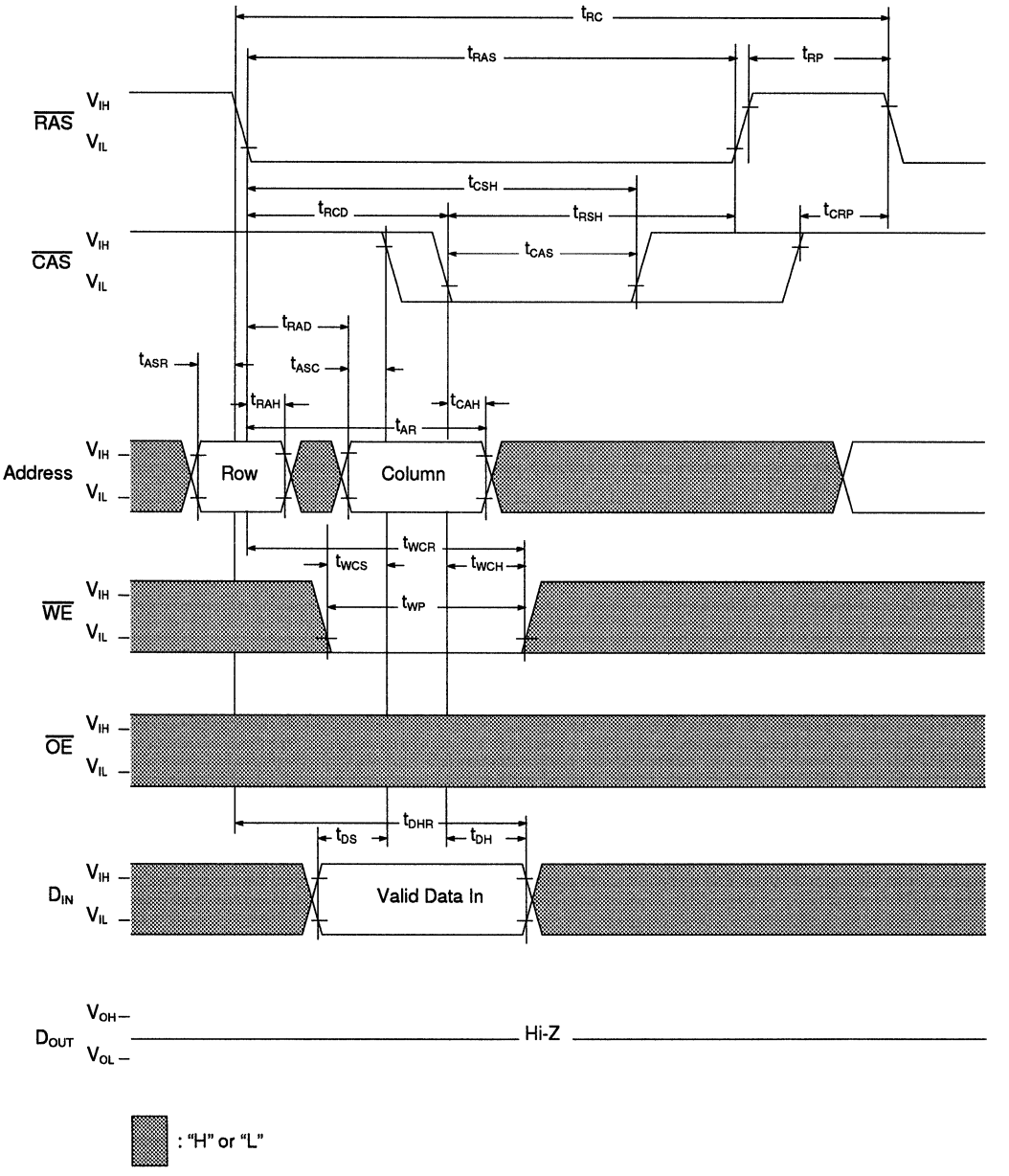
Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

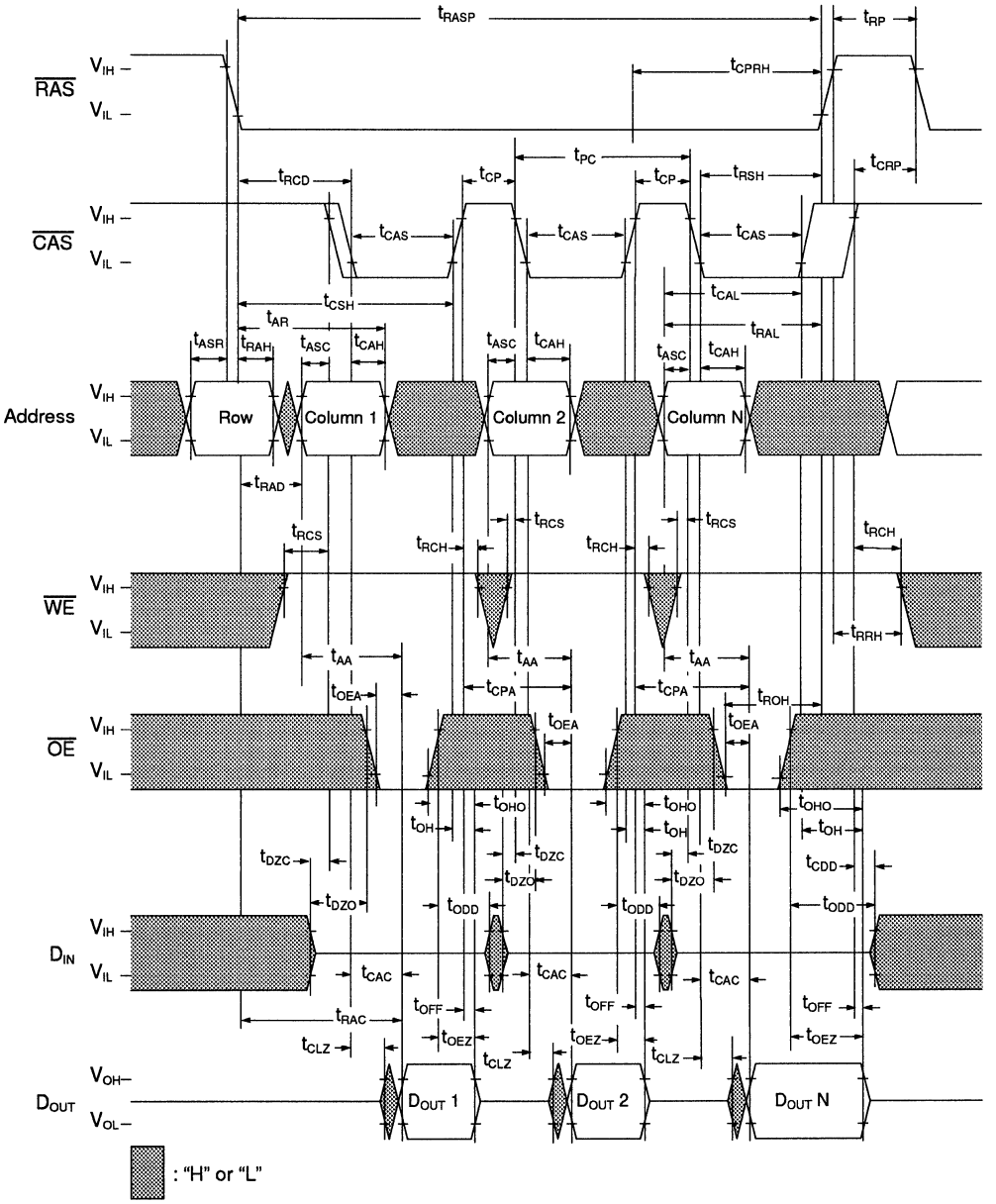
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tAR
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tCDD
tDZO
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
tOHO
: "H" or "L"

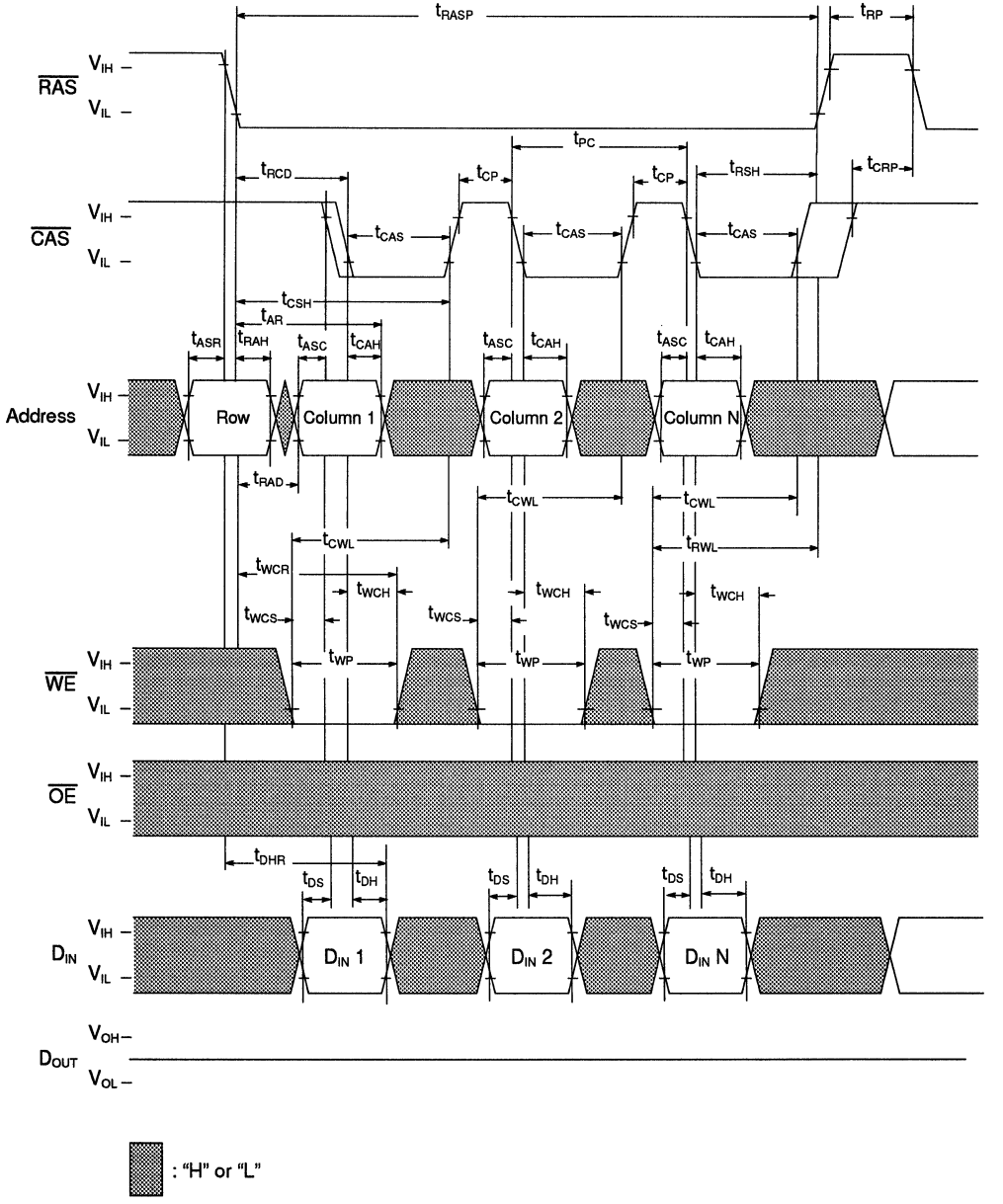
Write Cycle (Early Write)



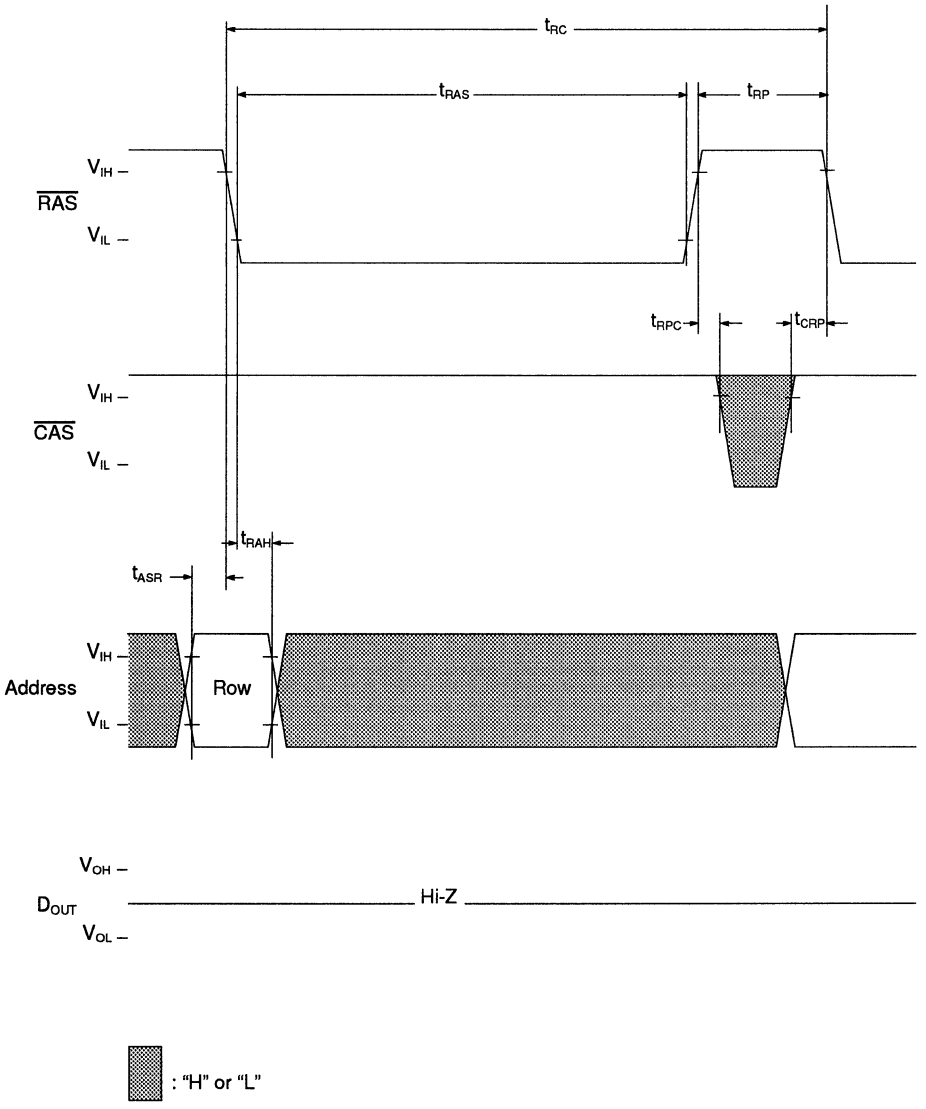
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

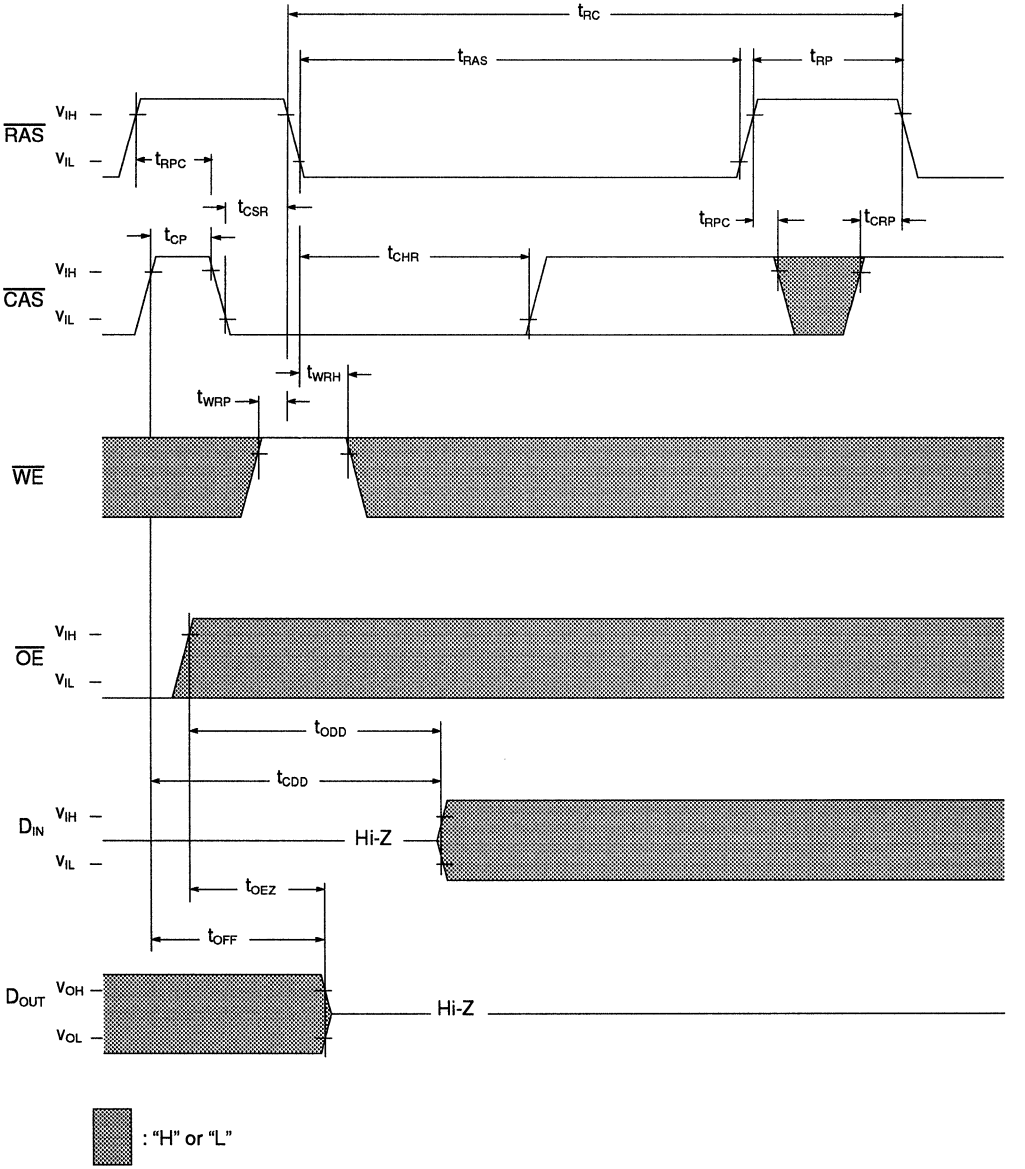


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

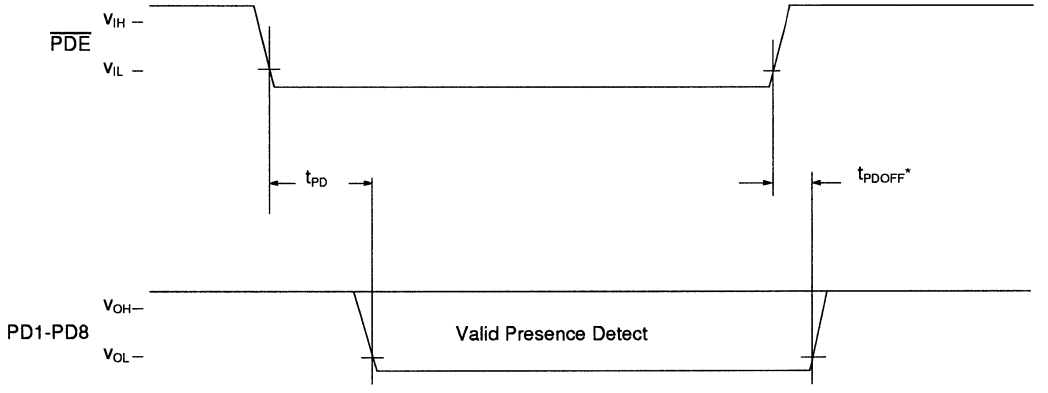
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



: "H" or "L"

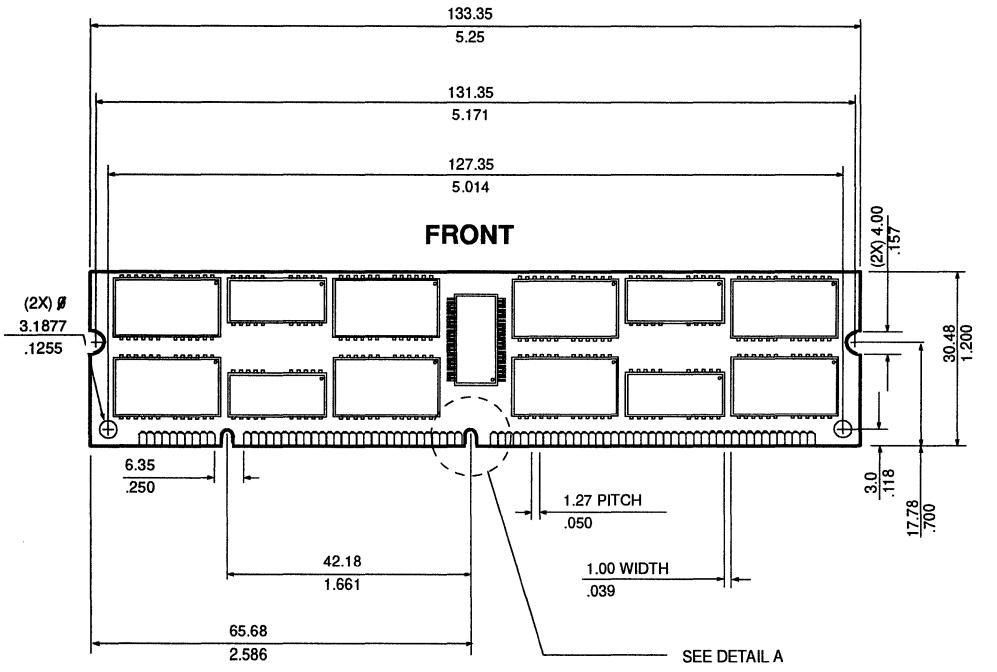
Note: Addresses are "H" or "L"

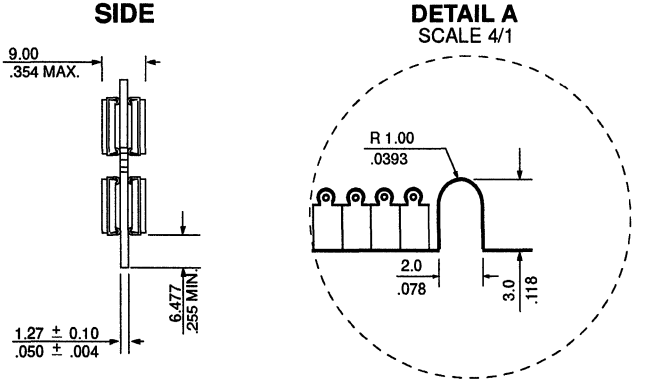
Presence Detect Read Cycle



*PD pins must be pulled high at next level of assembly

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

168 Pin DIMMs

-ECC

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 1Mx72 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are fully TTL and CMOS compatible
- Single 5V, ± 0.5V Power Supply
- Au contacts
- Optimized for ECC applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - 4 Byte Interleave enabled
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 addressing (Row/Column)
- Card size = 5.25" x 1.0" x 0.354"
- DRAMS in SOJ Package

Description

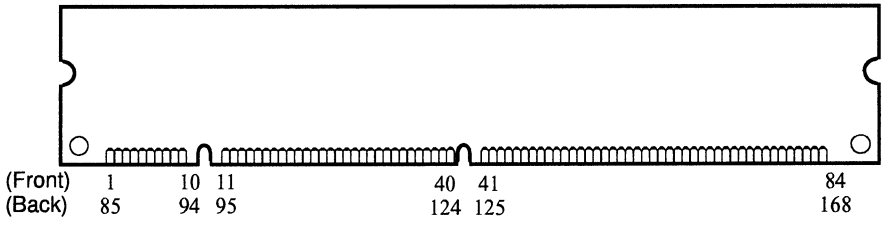
IBM11M1730BA is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 1Mx72 high speed memory array for ECC applications. The DIMM uses 18 1Mx4 DRAMs in SOJ packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, the system will determine that ECC DIMMs are installed if PD8 is low (0). ID0 need not be sensed since both x72 and x80 ECC DIMMs will function in a x72 bank.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 and x72 parity (5V) DIMMs and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A9	Address Inputs (Buffered)
DQx	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

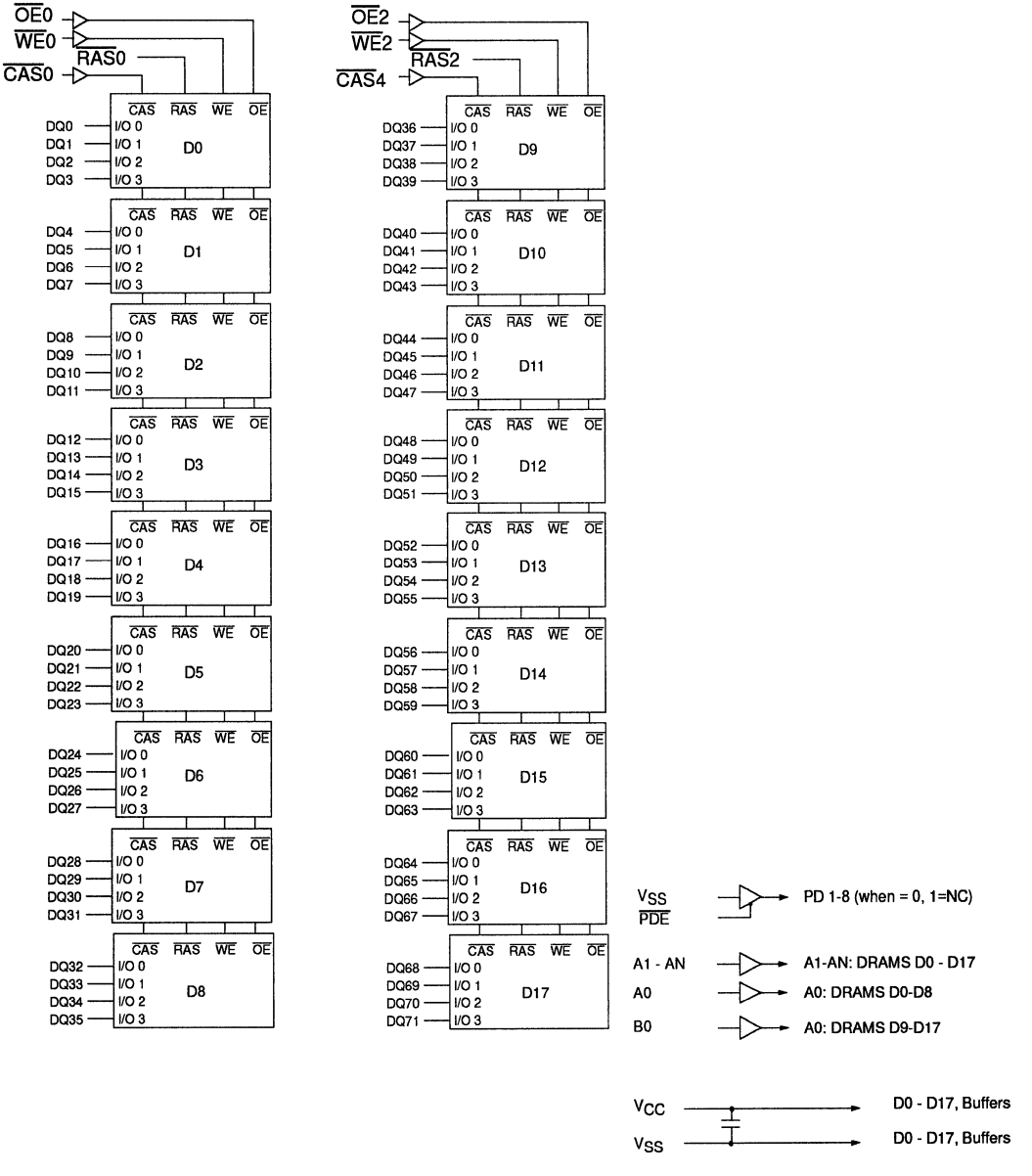
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	NC
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	NC
5	DQ3	89	DQ39	47	NC	131	NC
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	DQ8	95	DQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	DQ17	106	DQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	DQ26	150	DQ62
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	NC	70	DQ29	154	DQ65
29	NC	113	NC	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	NC	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	DQ35	161	DQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	NC	122	NC	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M1730BA-60	1Mx72	60ns	Au	5.25"x1.0"x 0.354"	
IBM11M1730BA-70	1Mx72	70ns	Au	5.25"x1.0"x 0.354"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	0	0
PD2	0	0
PD3	1	1
PD4	0	0
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	0	0
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 6.5	V	1
V_{IN}	Input Voltage	-0.7 to V_{CC} +0.7	V	1
V_{OUT}	Output Voltage	-0.7 to V_{CC} +0.7	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	11.9	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A9)	13	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	70	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF	
C_{I4}	DQ_X Capacitance	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	2160	mA	1,2,3
		-70	—	1944		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	36	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	2160	mA	1,3
		-70	—	1944		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1350	mA	1,2,3
		-70	—	1260		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	36	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	2160	mA	1,3
		-70	—	1944		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 4.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1},I_{CC3},I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1},I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. The 1Mx4 DRAM Outputs will remain disabled until these 8 cycles have occurred. This prevents data contention (excessive current) during power on. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the Dram device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	1
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	4
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	57	—	62	—	—	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
2. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	2	—	ns	1
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	3
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	36	—	41	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	15	—	15	—	ns	
t_{OH}	Output Data Hold Time	2	—	2	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	2, 3

1. This timing parameter is not applicable to this product, but applies to a related product in this family.
2. Measured with the specified current load and 100pF.
3. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

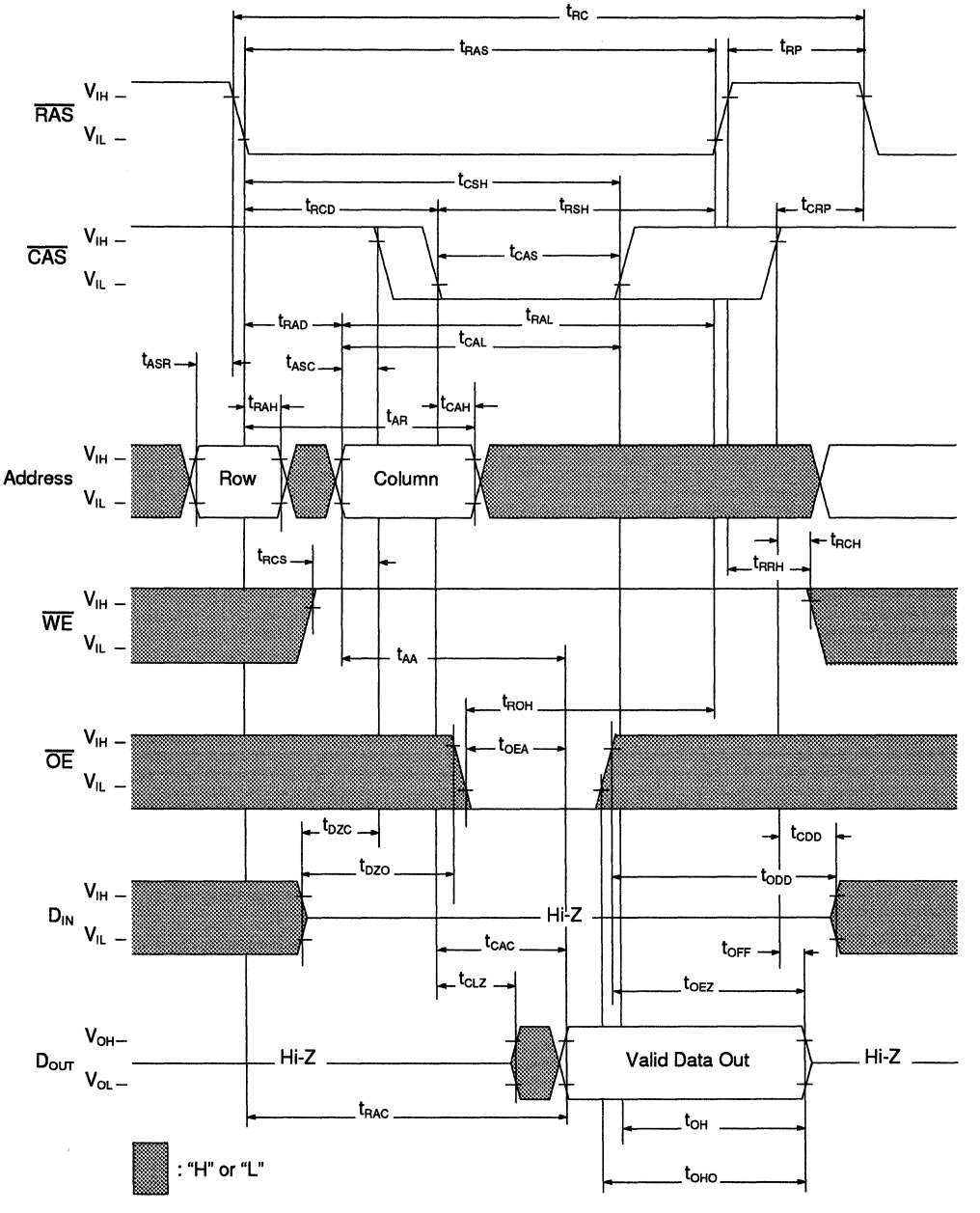
1. 1024 refreshes are required every 16ms.

Presence Detect Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Read Cycle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tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
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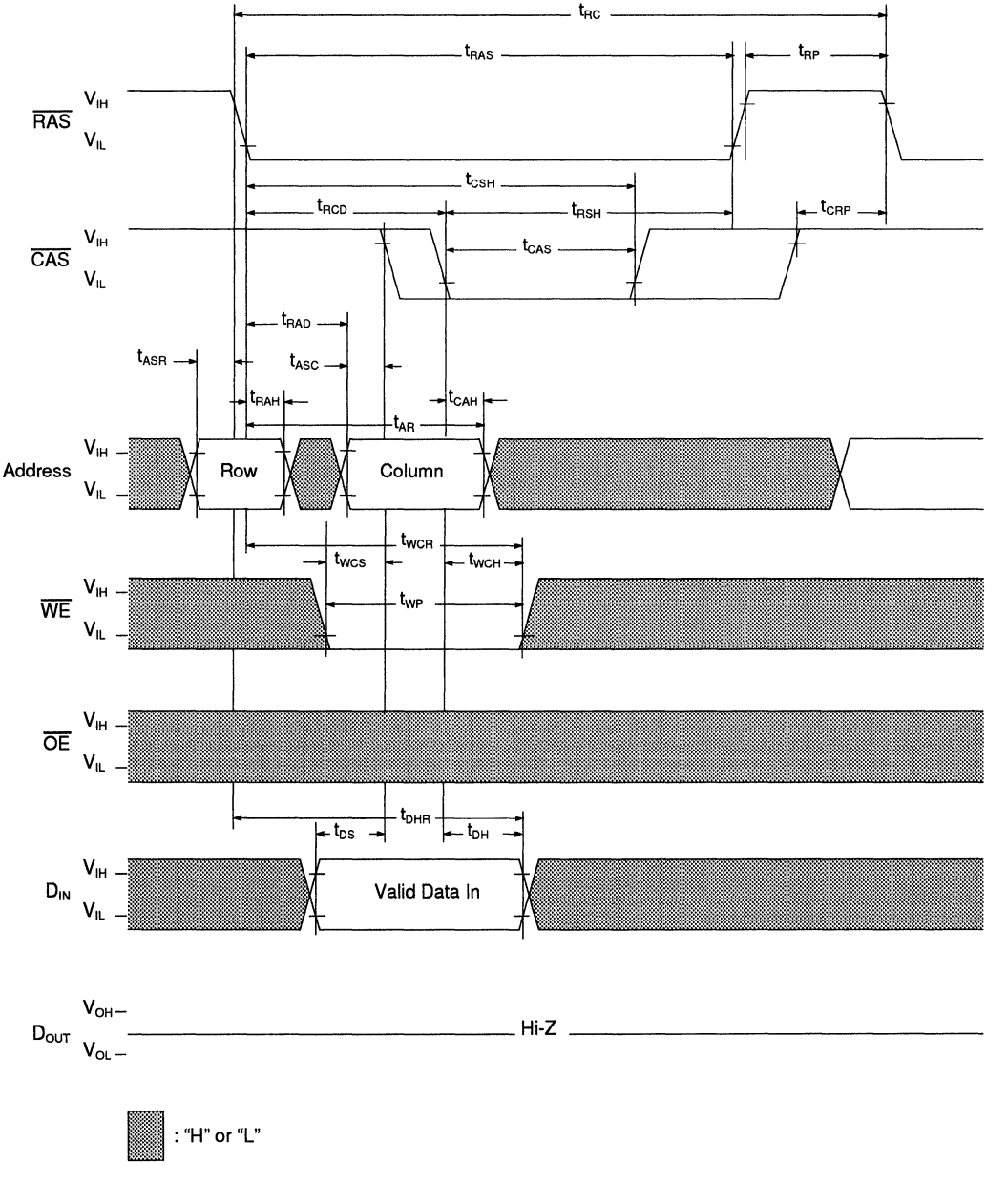
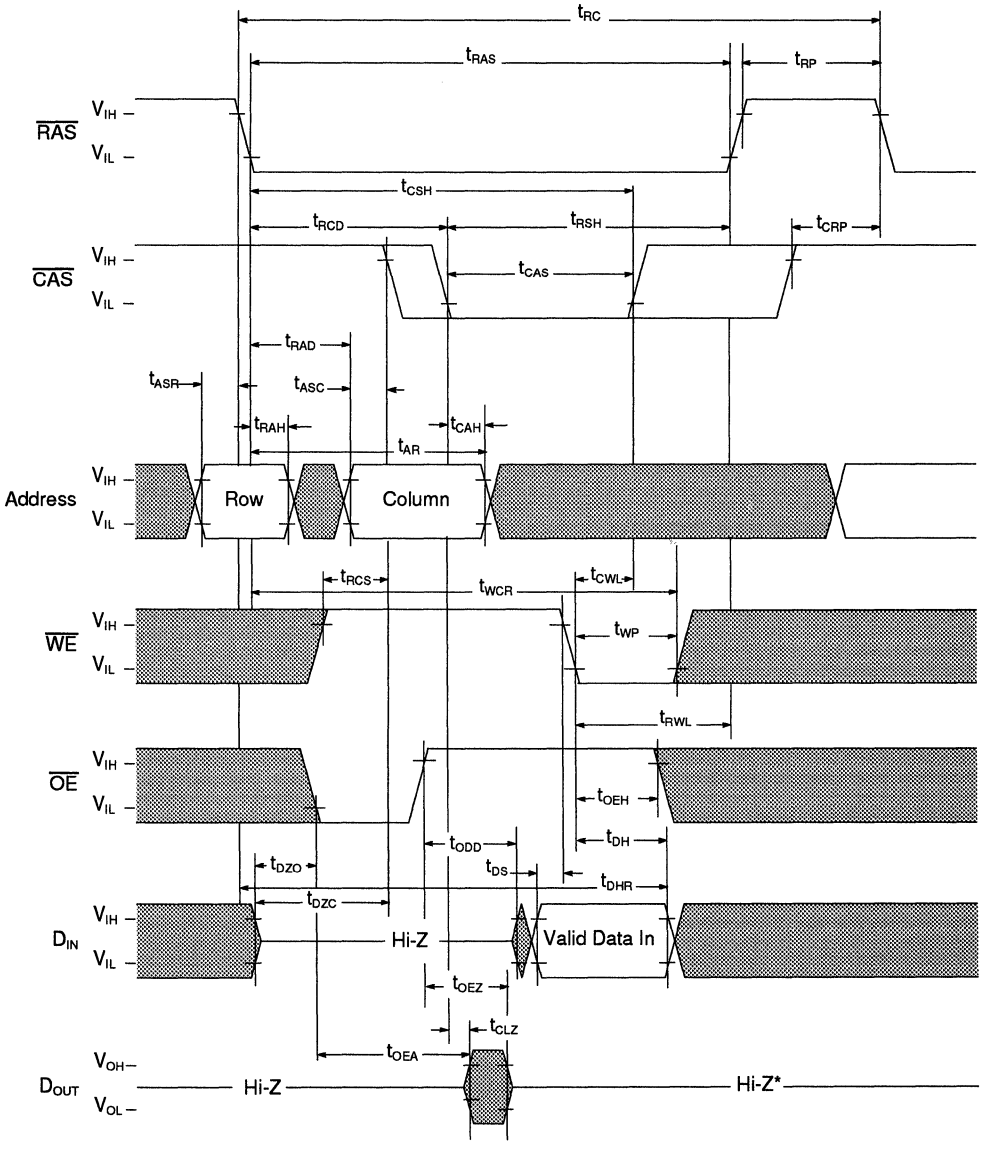
tASR
tASC
tRAH
tAR
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Valid Data Out
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

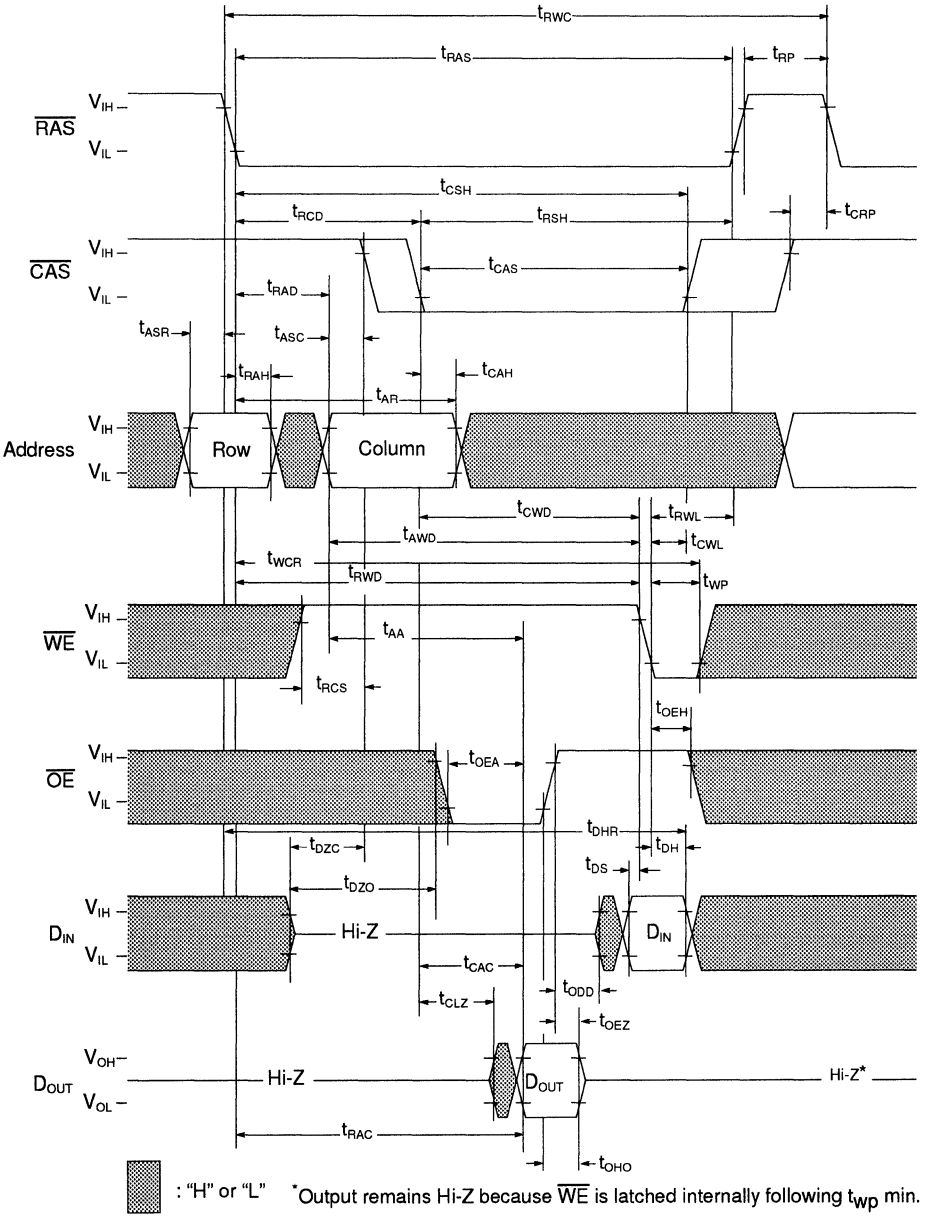


Write Cycle (Late Write)

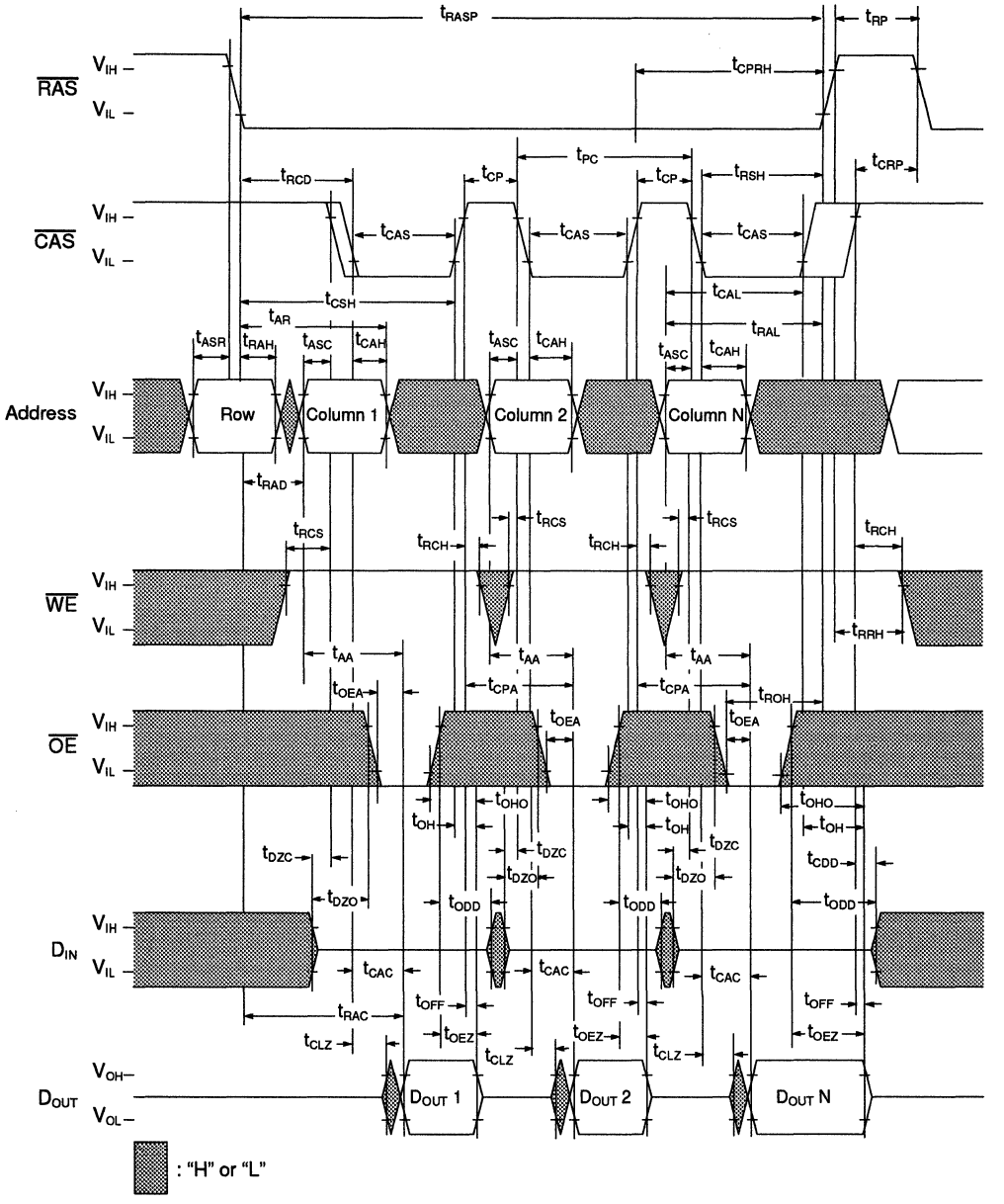


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

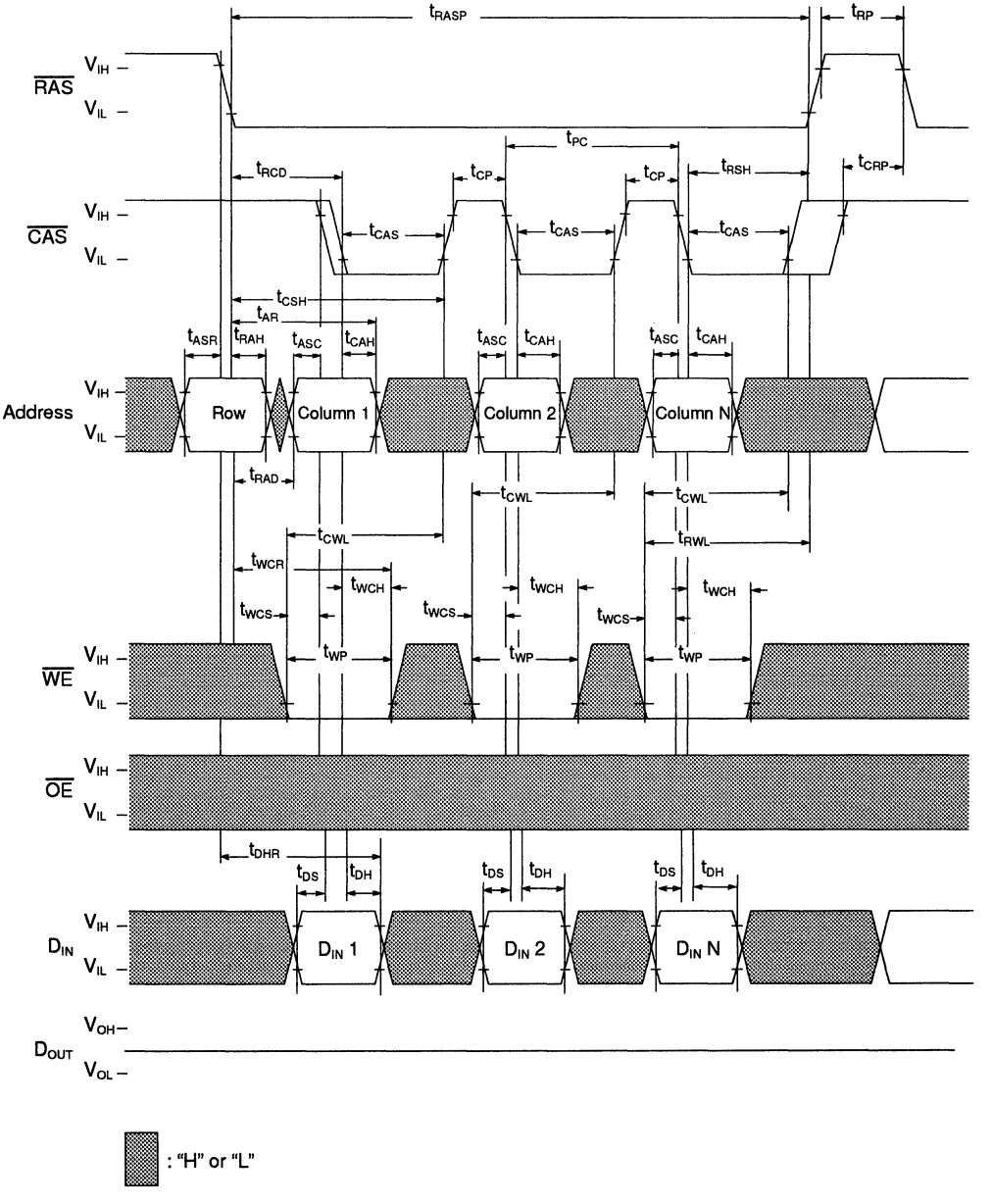
Read-Modify-Write-Cycle



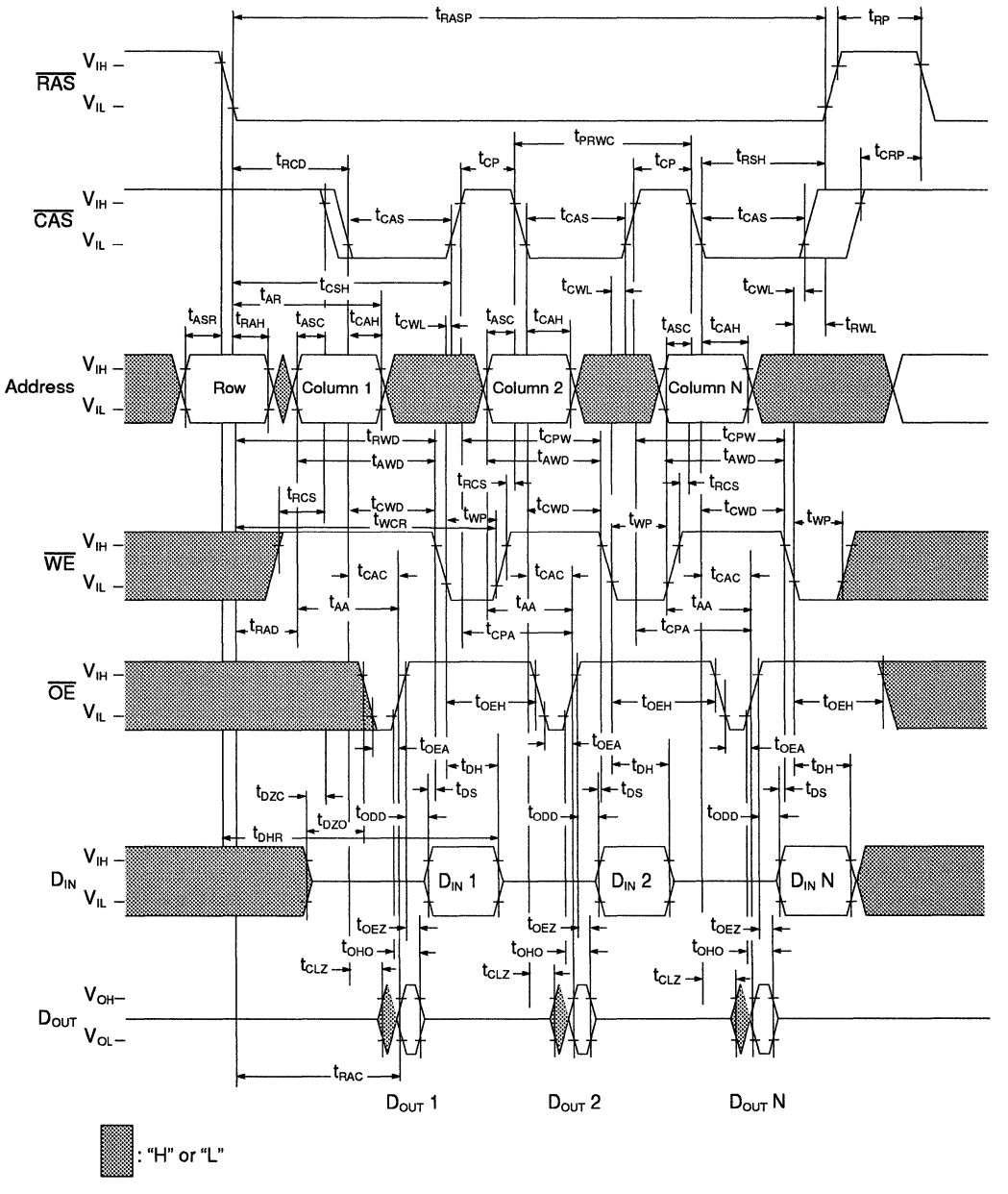
Fast Page Mode Read Cycle



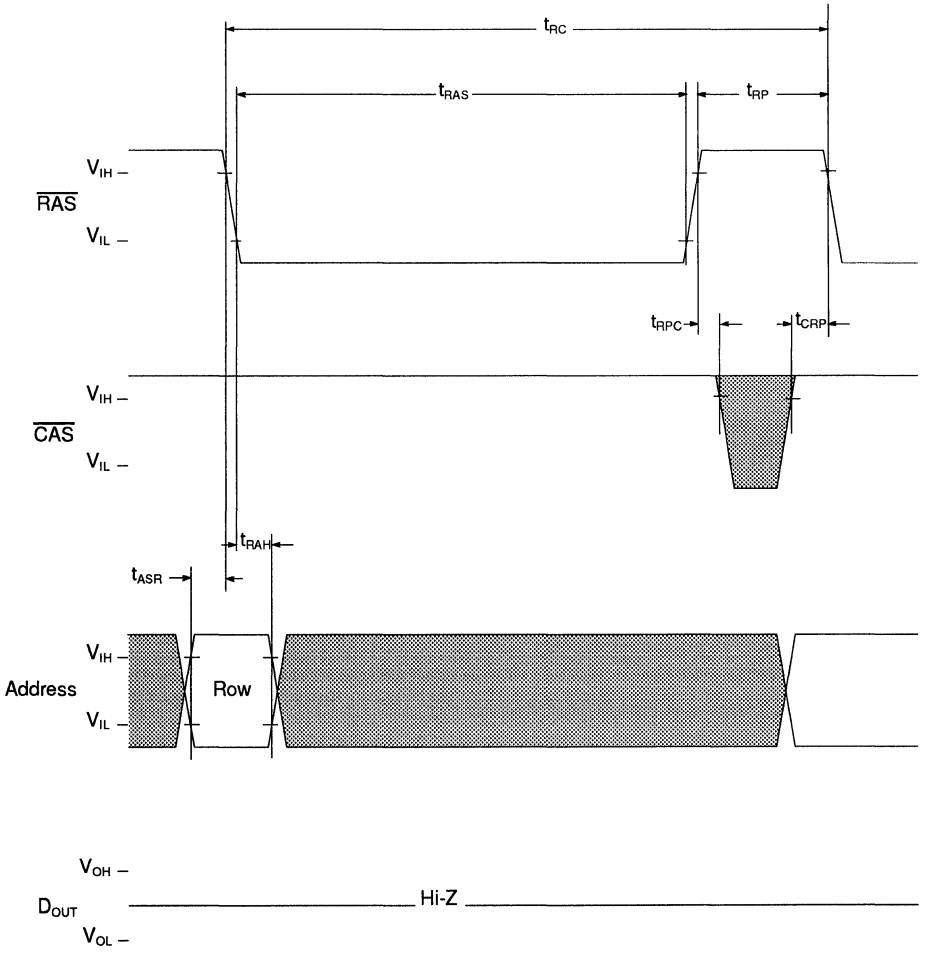
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

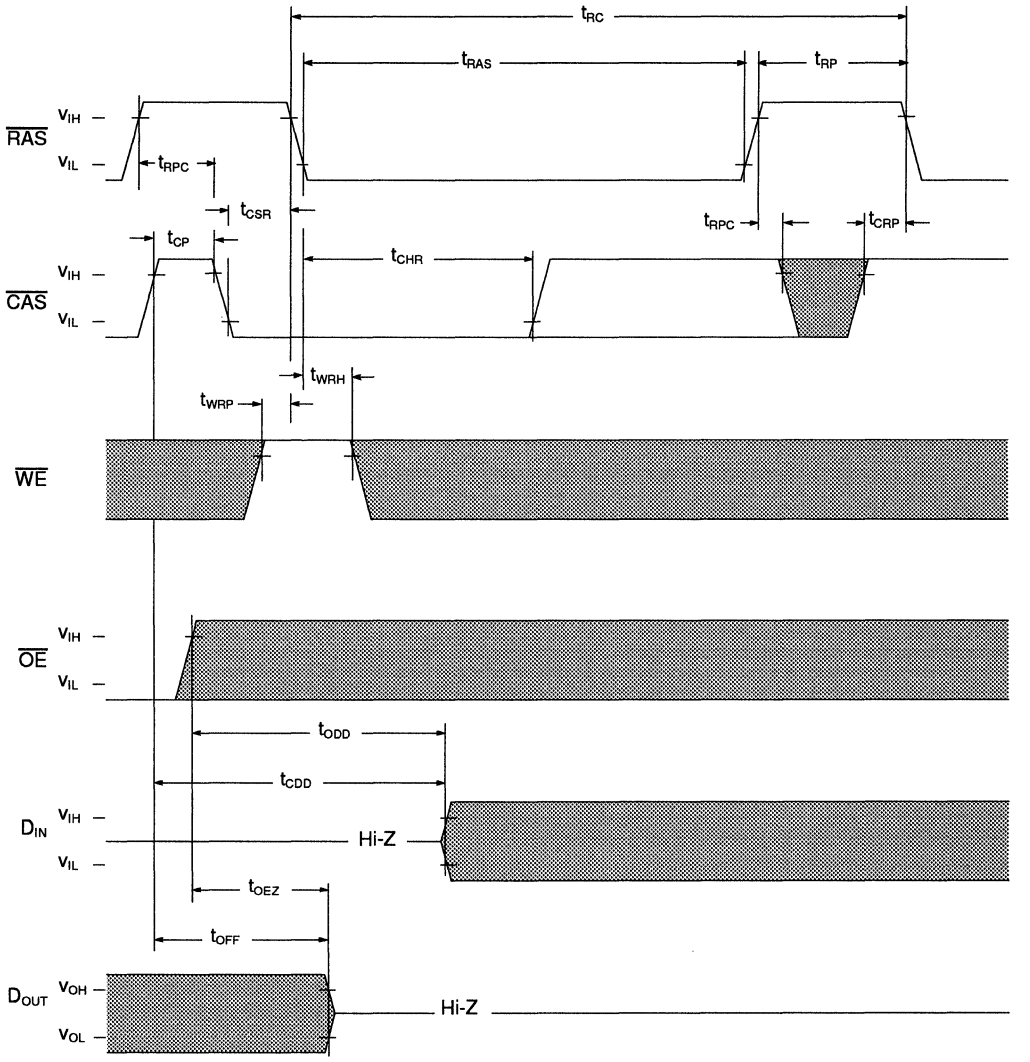


$\overline{\text{RAS}}$ Only Refresh Cycle



Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$, D_{IN} are "H" or "L"

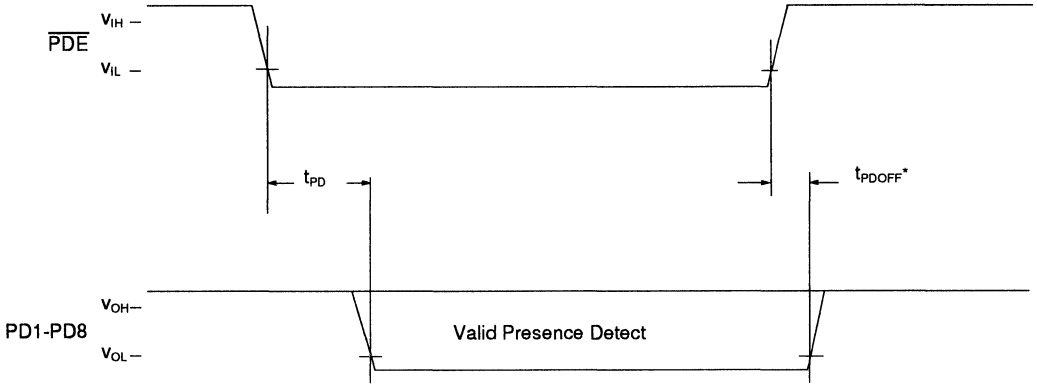
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



: "H" or "L"

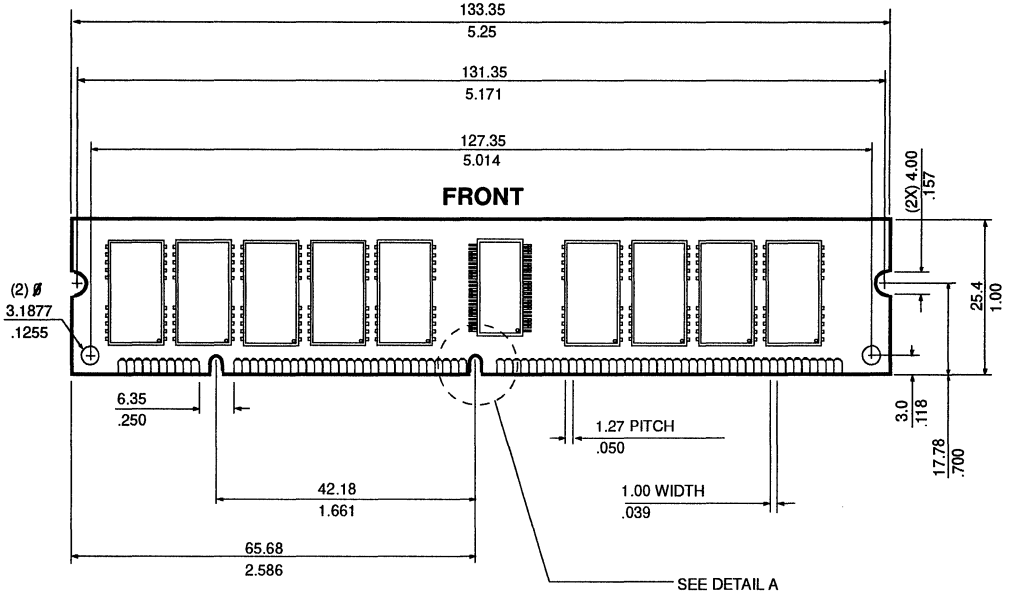
Note: Addresses are "H" or "L"

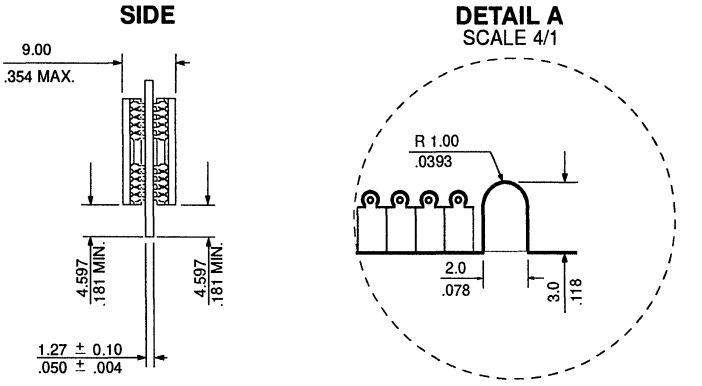
Presence Detect Read Cycle



*PD pins must be pulled high at next level of assembly

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 1Mx72 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are LVTTL and LVCMOS compatible
- Single 3.3V, ± 0.3V Power Supply
- Au contacts
- Optimized for ECC applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - 4 Byte Interleave enabled
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 addressing (Row/Column)
- Card size: 5.25" x 1.0" x 0.354"
- DRAMS in SOJ Package

Description

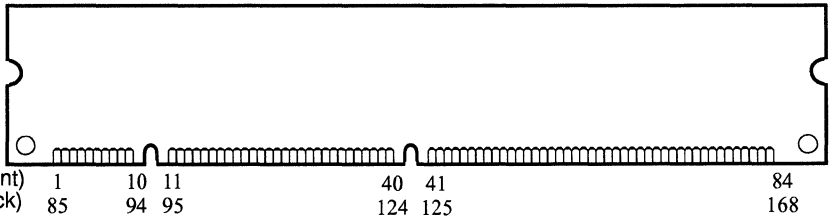
IBM11M1730BB is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 1Mx72 high speed memory array for ECC applications. The DIMM uses 18 1Mx4 DRAMs in SOJ packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, the system will determine that ECC DIMMs are installed if PD8 is low (0). ID0 need not be sensed since both x72 and x80 ECC DIMMs will function in a x72 bank.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 and x72 parity (5V) DIMMs and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A9	Address Inputs (Buffered)
DQx	Data Input/Output
V_{CC}	Power (3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

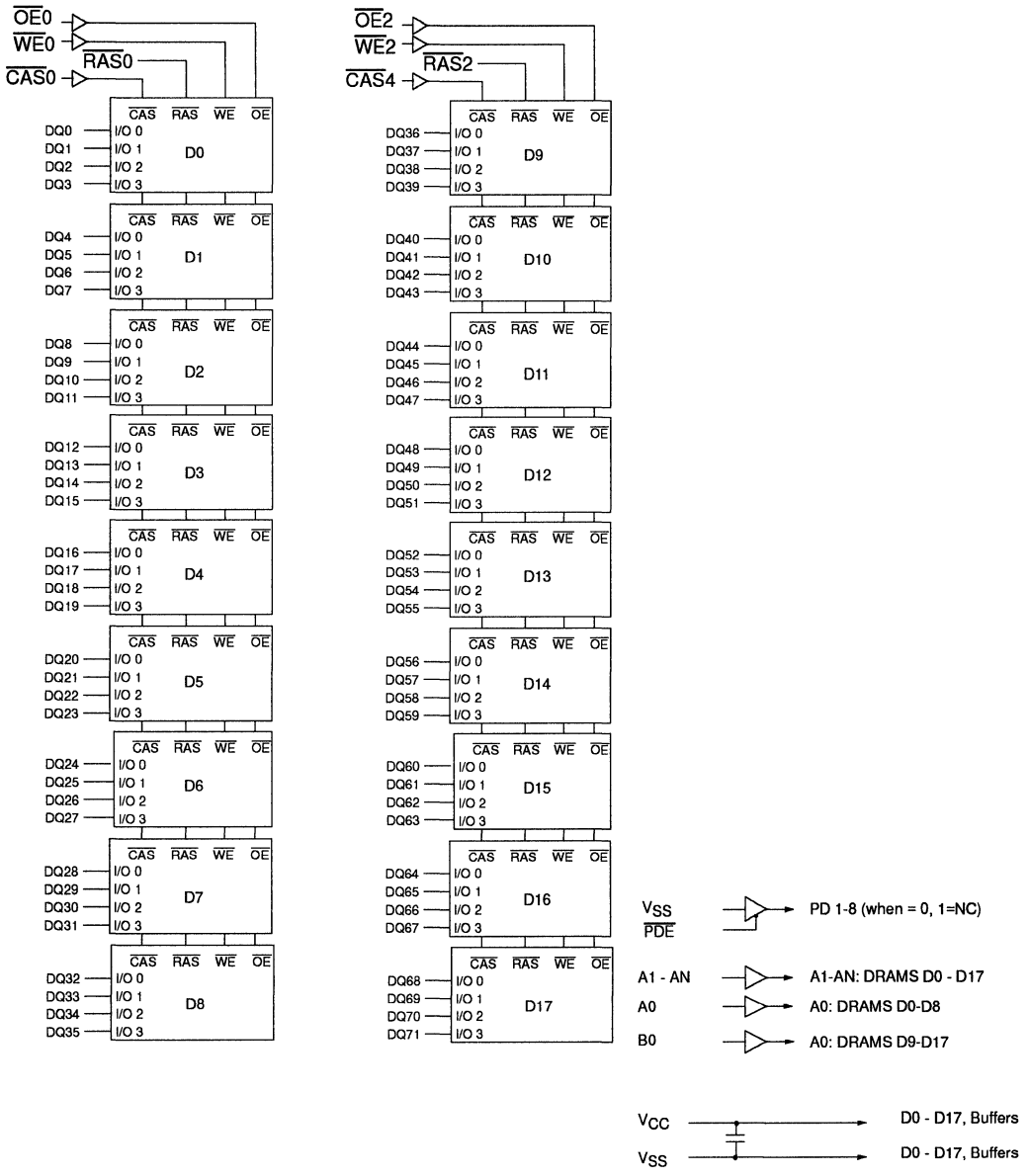
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	NC
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	NC
5	DQ3	89	DQ39	47	NC	131	NC
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	DQ8	95	DQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	DQ17	106	DQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	DQ26	150	DQ62
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	NC	70	DQ29	154	DQ65
29	NC	113	NC	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	NC	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	DQ35	161	DQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	NC	122	NC	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M1730BBA-60	1Mx72	60ns	Au	5.25"x1.0"x 0.354"	
IBM11M1730BBA-70	1Mx72	70ns	Au	5.25"x1.0"x 0.354"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	0	0
PD2	0	0
PD3	1	1
PD4	0	0
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	0	0
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

3. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
4. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 4.1	V	1
V_{IN}	Input Voltage	-0.5 to 4.1	V	1
V_{OUT}	Output Voltage	-0.5 to 4.1	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	5.5	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.3	V	1
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1

1. All voltages referenced to Vss.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A9)	13	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	70	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF	
C_{I4}	DQ_X Capacitance	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1530	mA	1,2,3
		-70	—	1260		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	36	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1530	mA	1,3
		-70	—	1260		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1080	mA	1,2,3
		-70	—	900		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	18	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1530	mA	1,3
		-70	—	1260		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the Dram device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	1
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	4
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	—	5
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
2. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.
5. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	2	—	ns	1
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	3
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	36	—	41	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	15	—	15	—	ns	
t_{OH}	Output Data Hold Time	2	—	2	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off delay	2	20	2	25	ns	

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RHC} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1, 2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

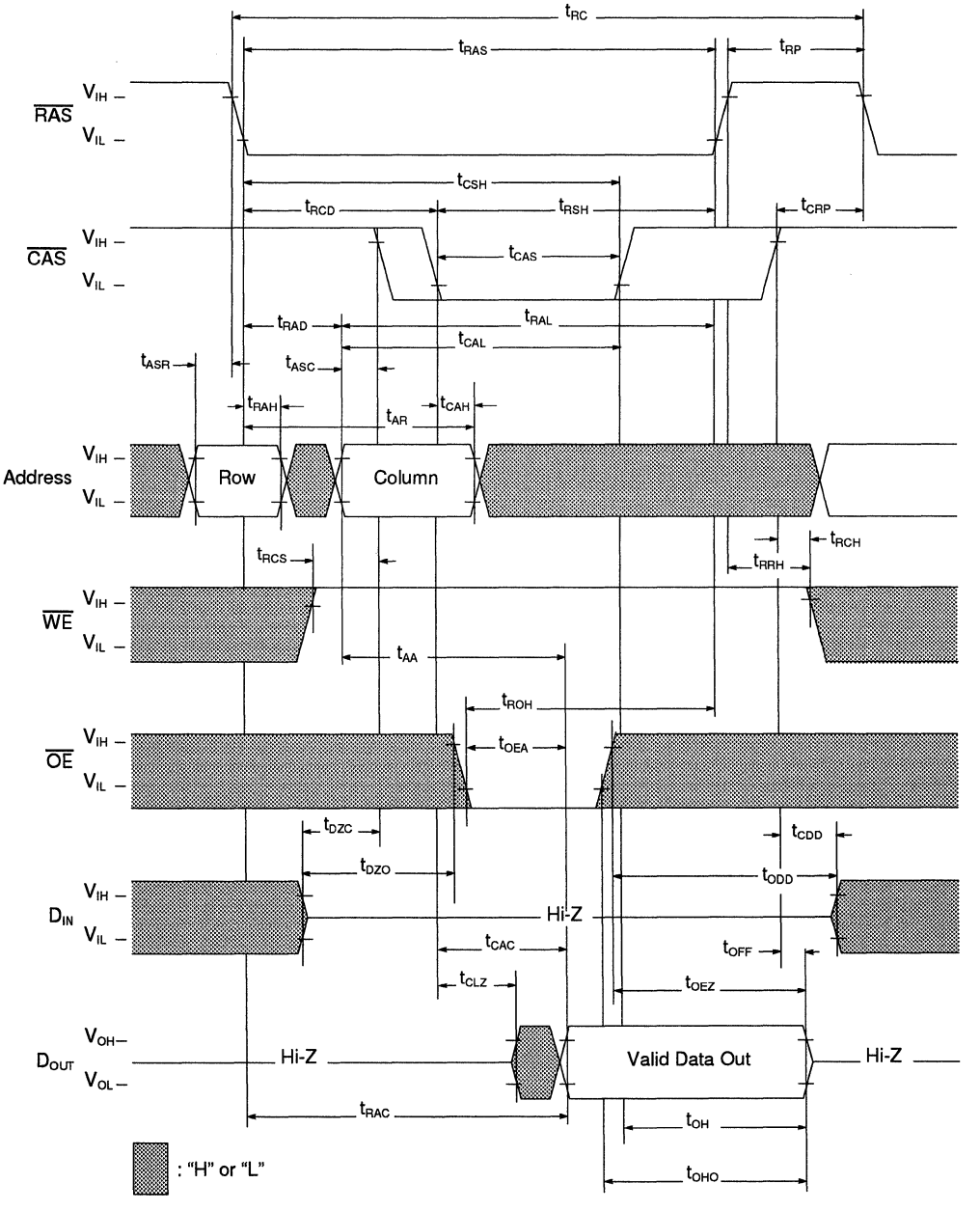
1. 1024 refreshes are required every 16ms.

Presence Detect Read Cycle

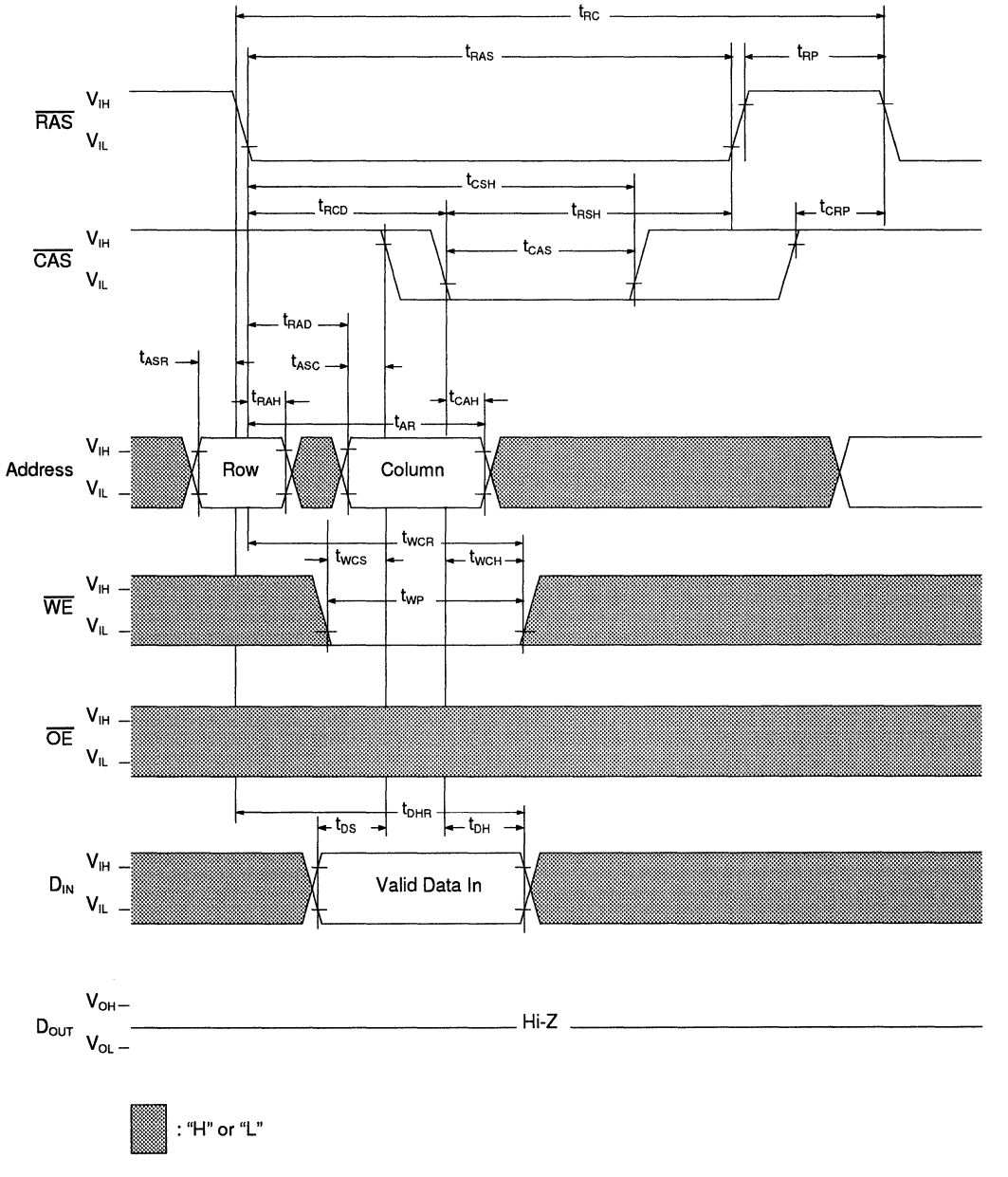
Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

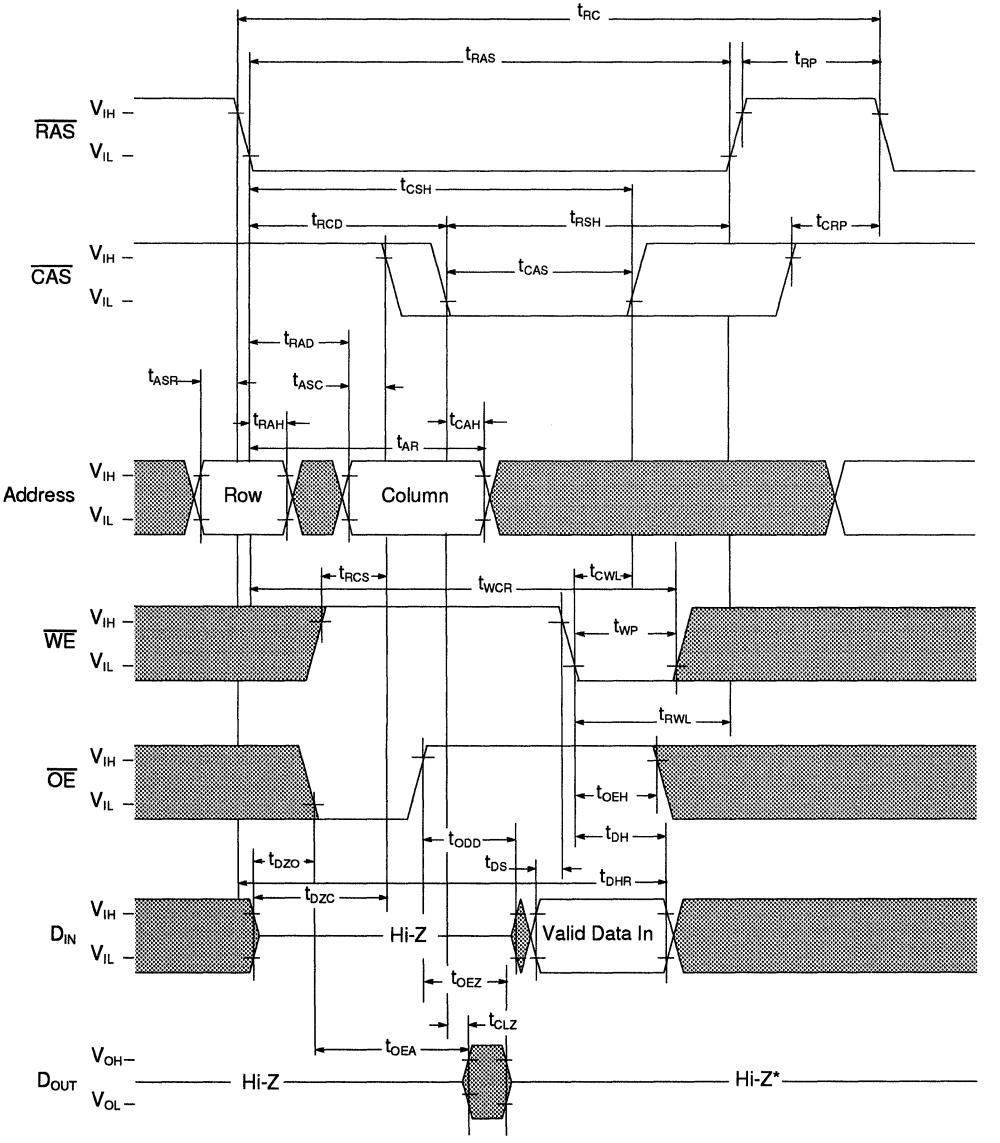
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tAR
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Valid Data Out
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

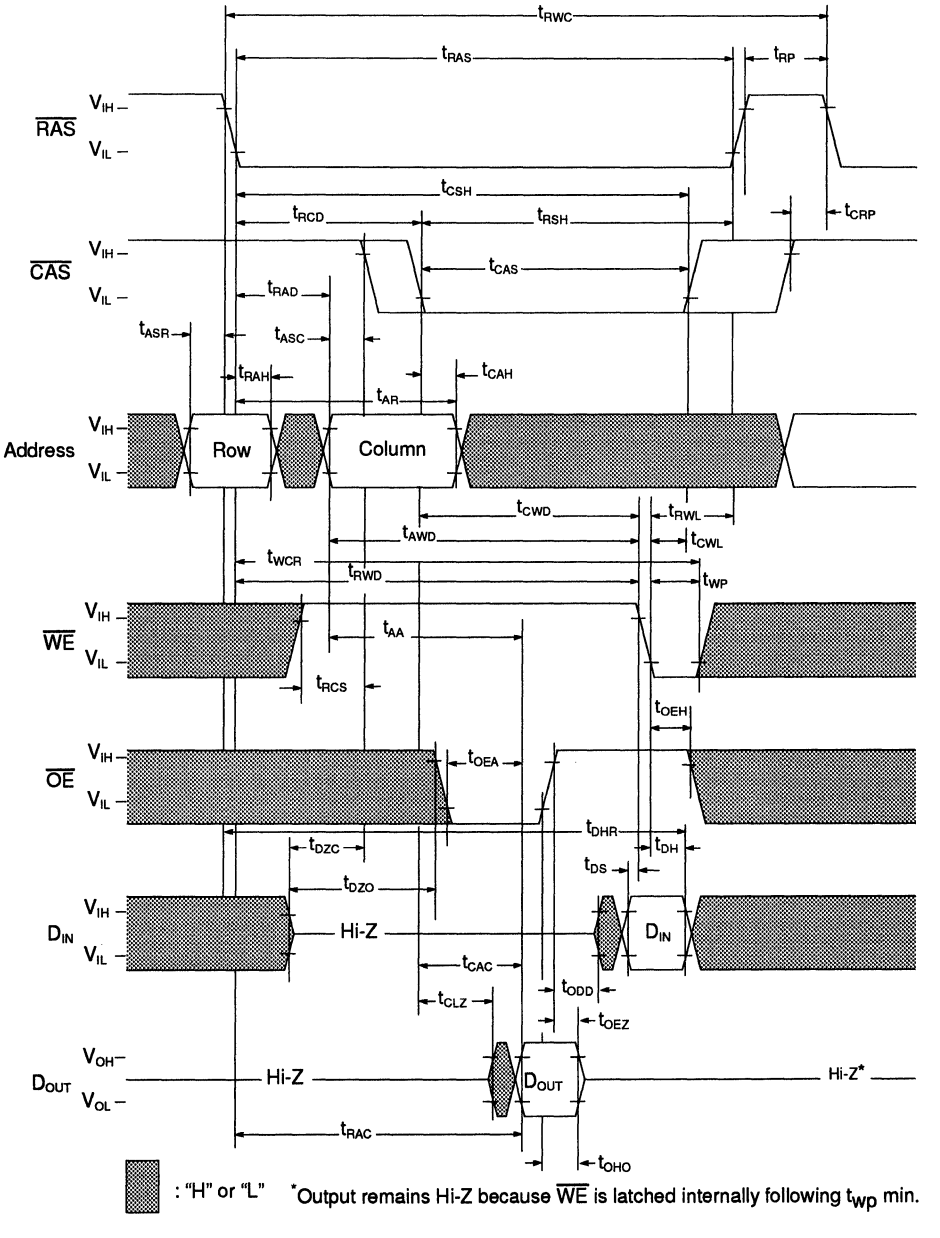


Write Cycle (Late Write)

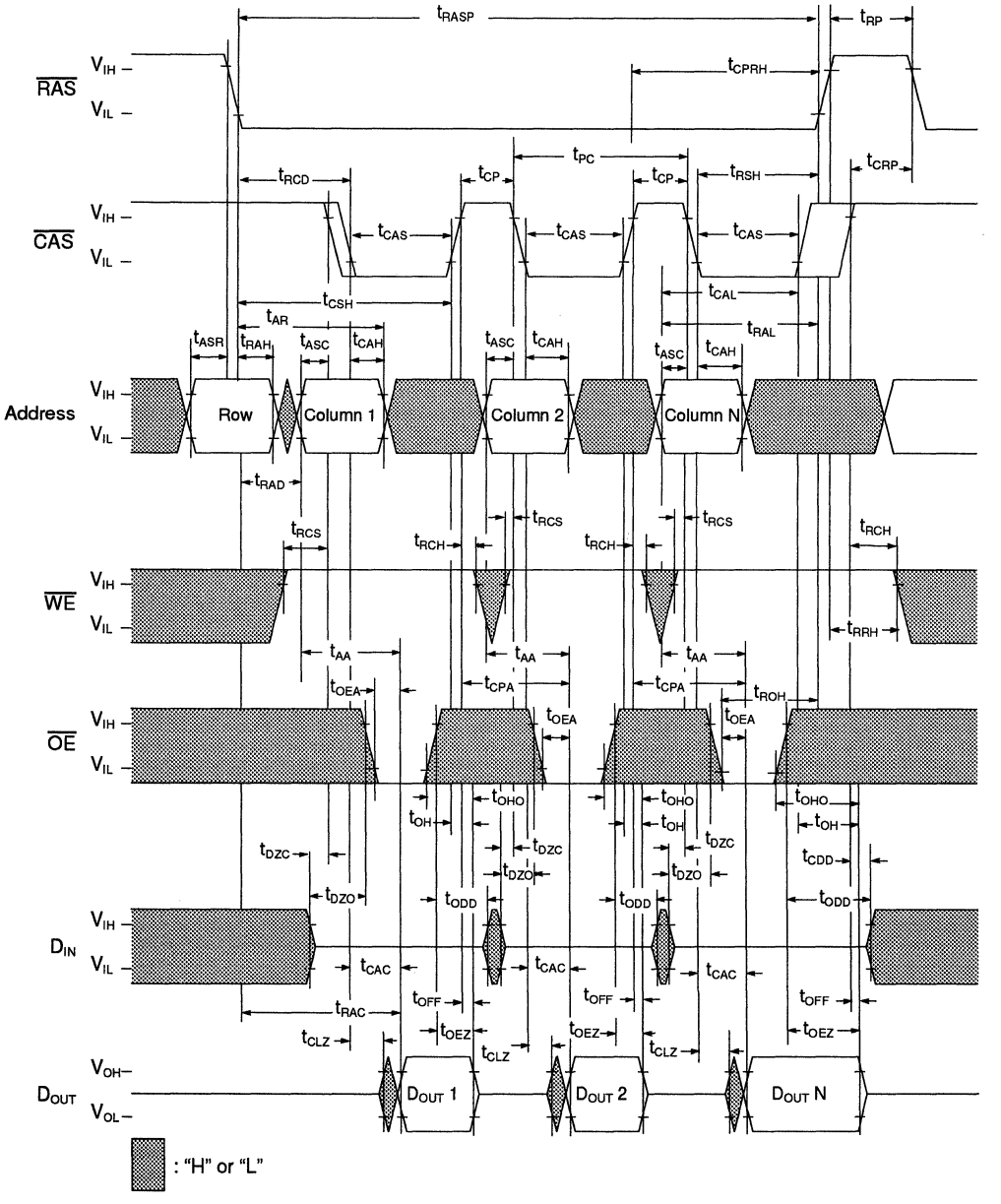


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

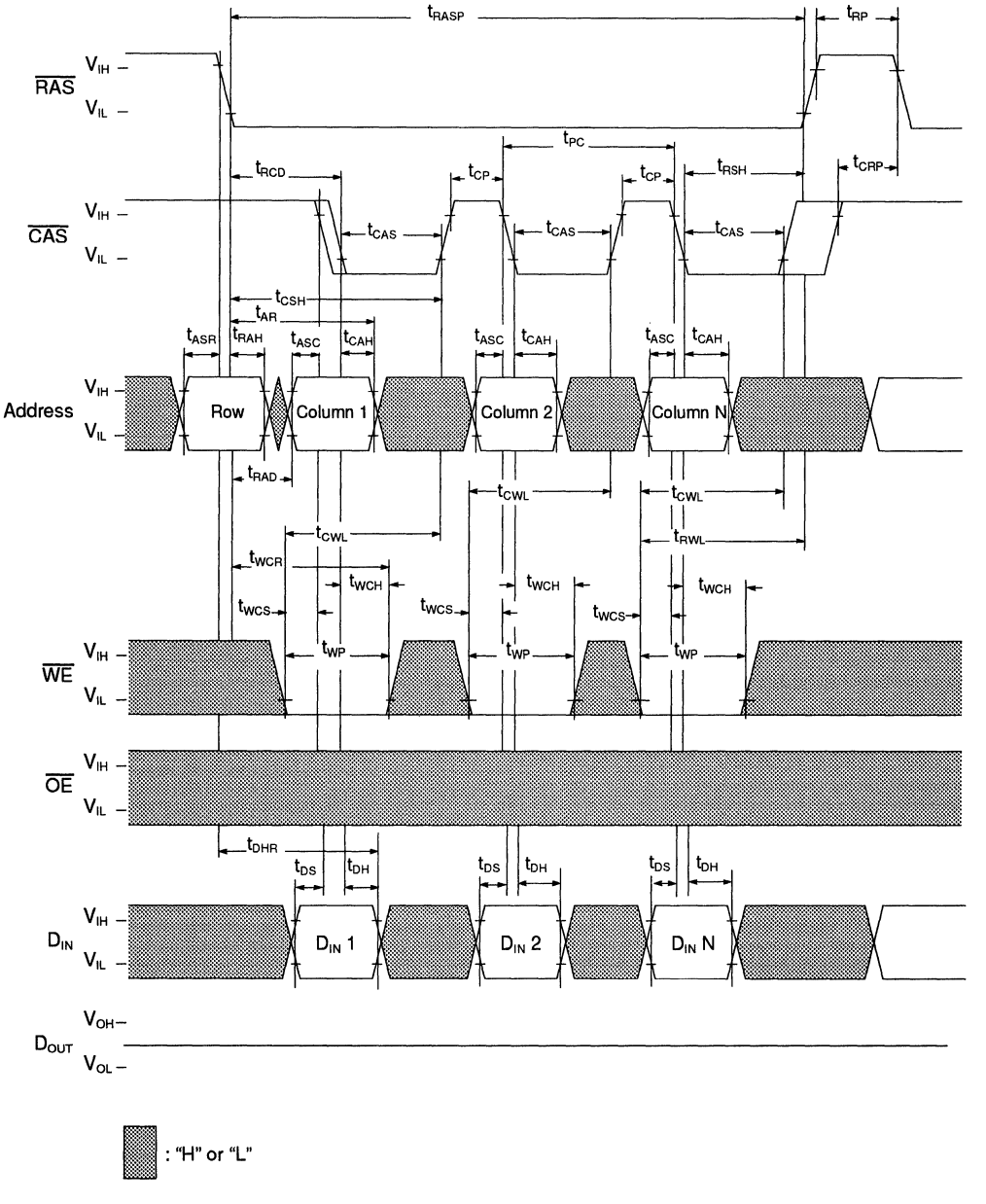
Read-Modify-Write-Cycle



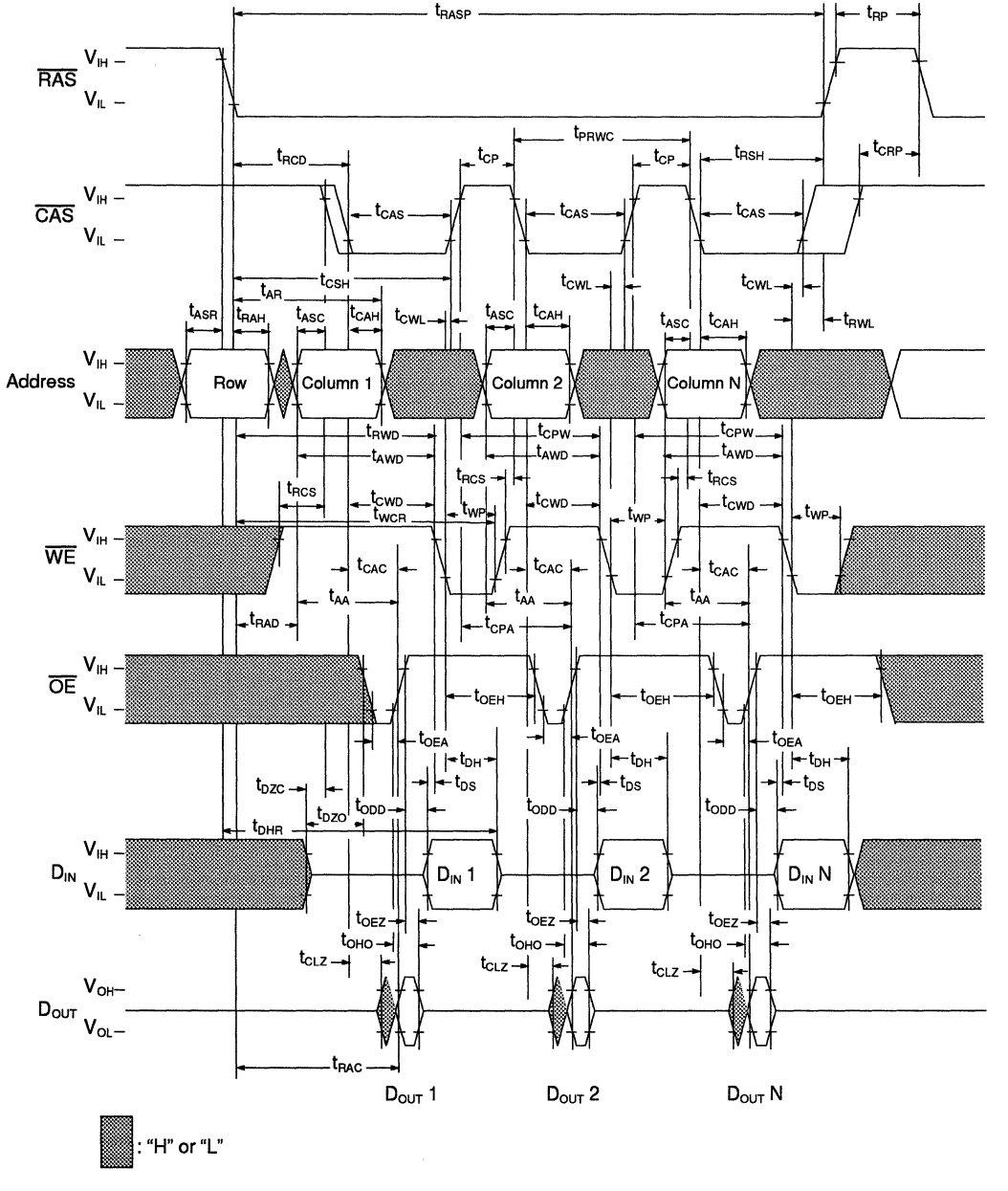
Fast Page Mode Read Cycle



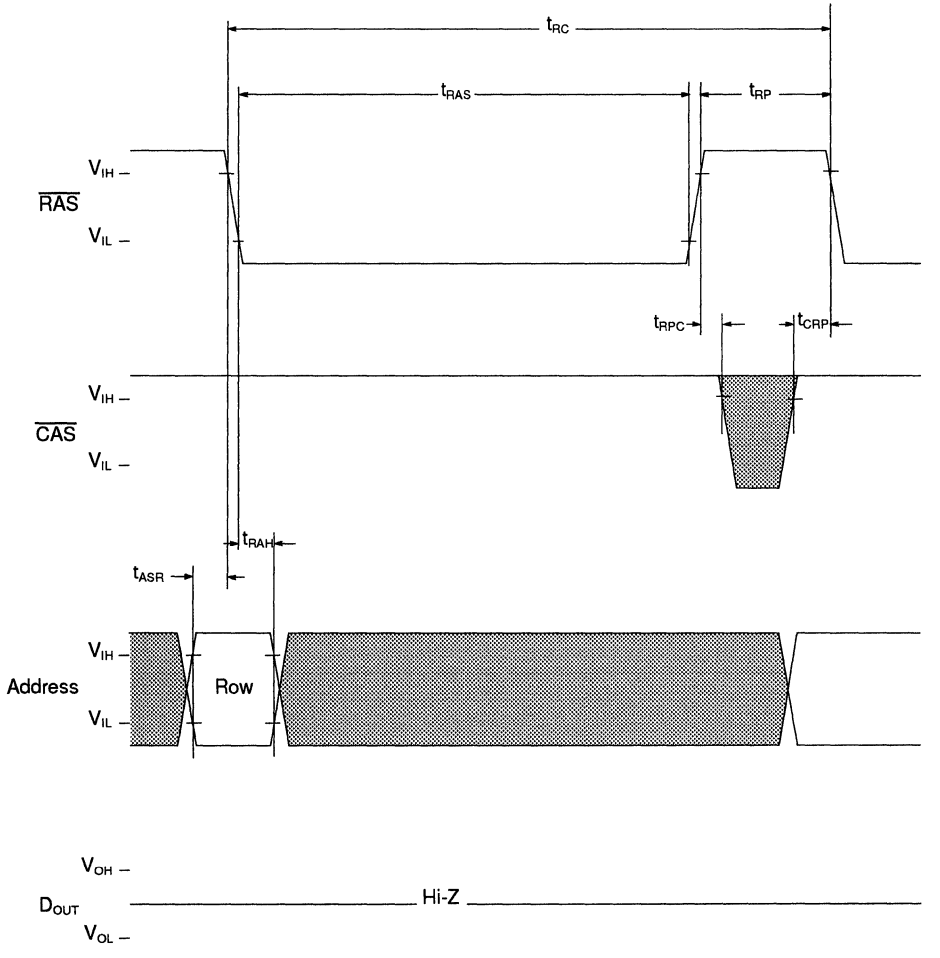
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

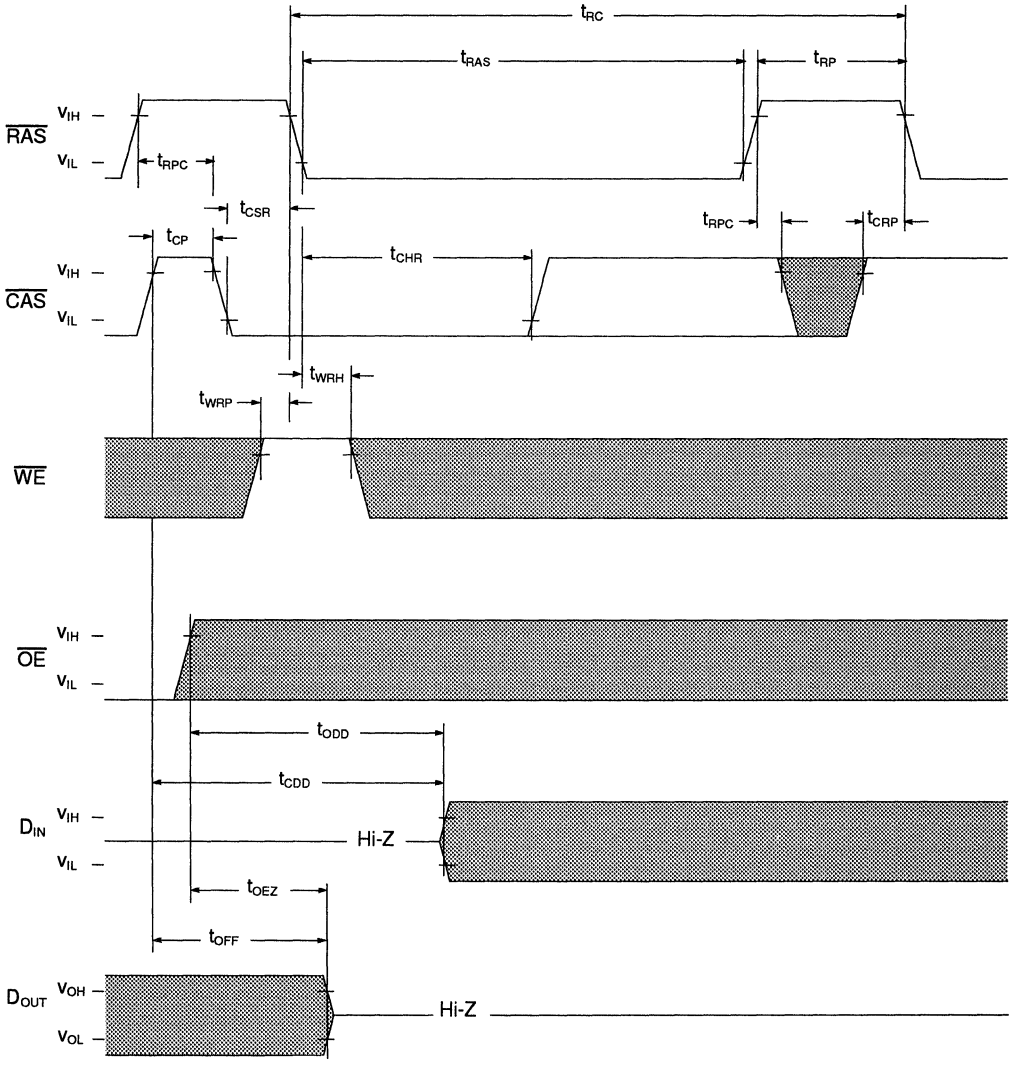


$\overline{RAS}$ Only Refresh Cycle



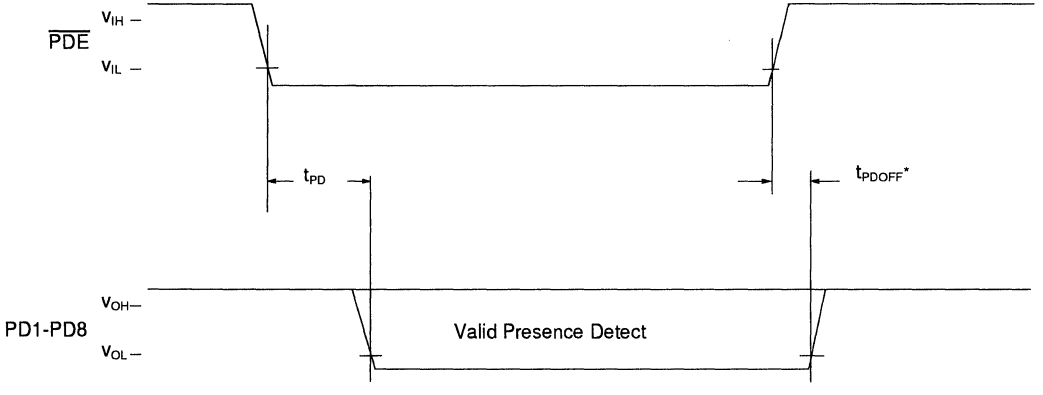
Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



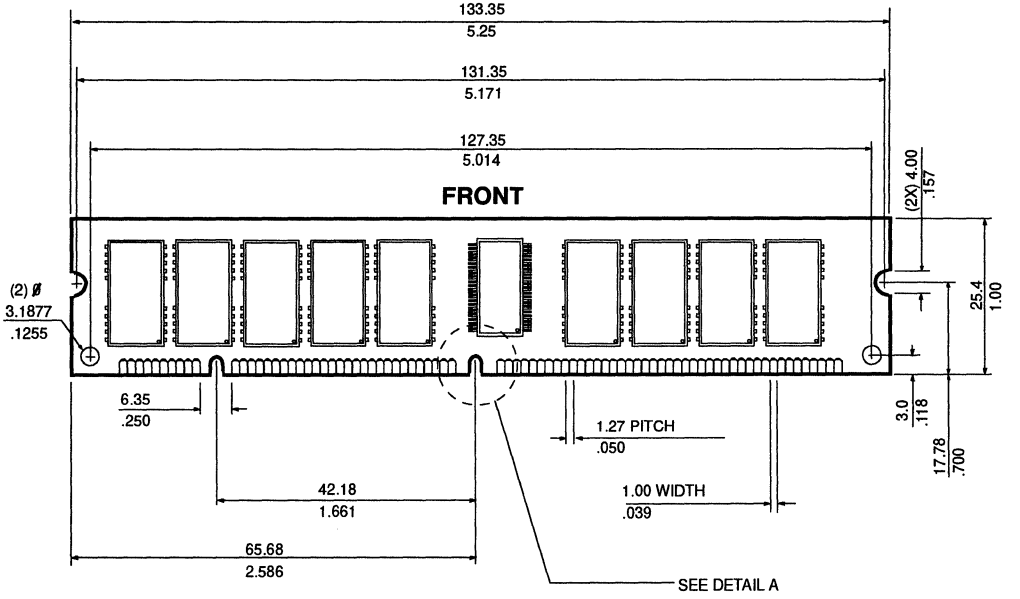
Note: Addresses are "H" or "L"

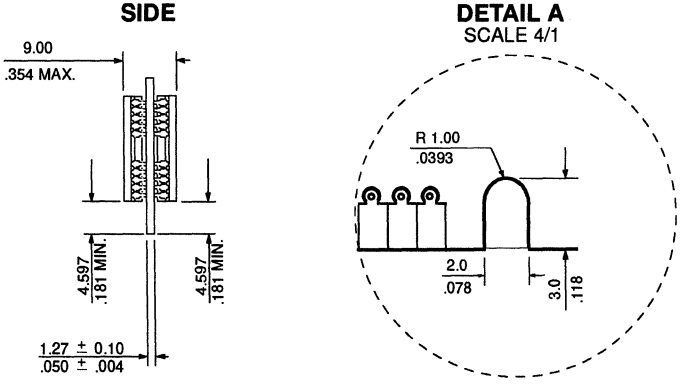
Presence Detect Read Cycle



*PD pins must be pulled high at next level of assembly

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 2Mx72 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are TTL and CMOS compatible
- Single 5.0V, ± 0.5V Power Supply
- Au contacts
- Optimized for ECC applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 2048 refresh cycles distributed across 32ms
- 11/10 addressing (Row/Column)
- Card size: 5.25" x 1.0" x 0.157"
- DRAMS in TSOP Package

Description

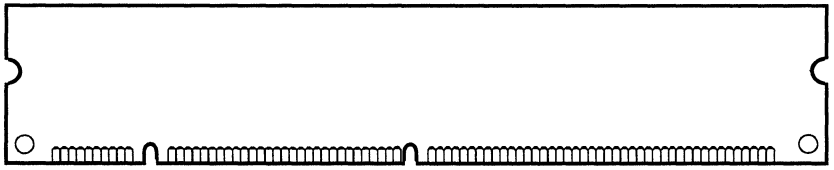
IBM11M2730H is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 2Mx72 high speed memory array for ECC applications. The DIMM uses 9 2Mx8 DRAMs in TSOP packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, the system will determine that ECC DIMMs are installed if PD8 is low (0). ID0 need not be sensed since both x72 and x80 ECC DIMMs will function in a x72 bank.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 and x72 parity (5V) DIMMs and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A10	Address Inputs (Buffered)
DQx	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

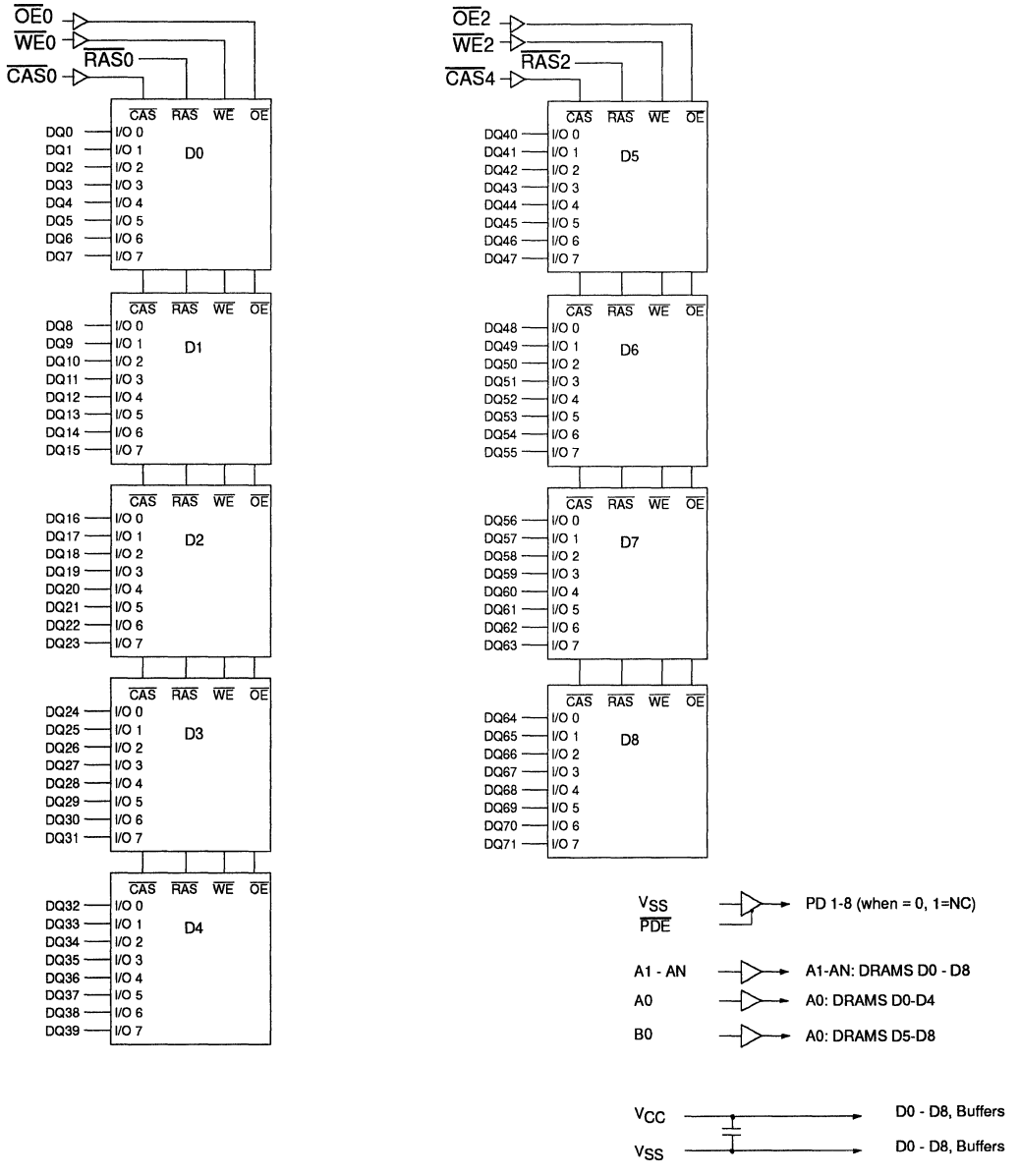
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	NC
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	NC
5	DQ3	89	DQ39	47	NC	131	NC
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	DQ8	95	DQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	DQ17	106	DQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	DQ26	150	DQ62
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	NC	70	DQ29	154	DQ65
29	NC	113	NC	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	NC	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	DQ35	161	DQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	A10	122	NC	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M2730HA-60	2Mx72	60ns	Au	5.25"x1.0"x 0.157"	
IBM11M2730HA-70	2Mx72	70ns	Au	5.25"x1.0"x 0.157"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	1	1
PD2	0	0
PD3	0	0
PD4	1	1
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	0	0
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	5.95	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to Vss.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A10)	13	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	40	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF	
C_{I4}	DQ_X Capacitance	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1080	mA	1,2,3
		-70	—	900		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	18	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1080	mA	1,3
		-70	—	900		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	675	mA	1,2,3
		-70	—	585		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	9	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1080	mA	1,3
		-70	—	900		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-50	+50		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the Dram device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	1
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	4
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	—	5
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
2. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.
5. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	2	—	ns	1
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	3
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	36	—	41	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	36	—	41	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	—	—	—	—	ns	4
t_{OH}	Output Data Hold Time	2	—	2	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1, 2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	63	—	73	—	ns	1

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	32	—	32	ms	1

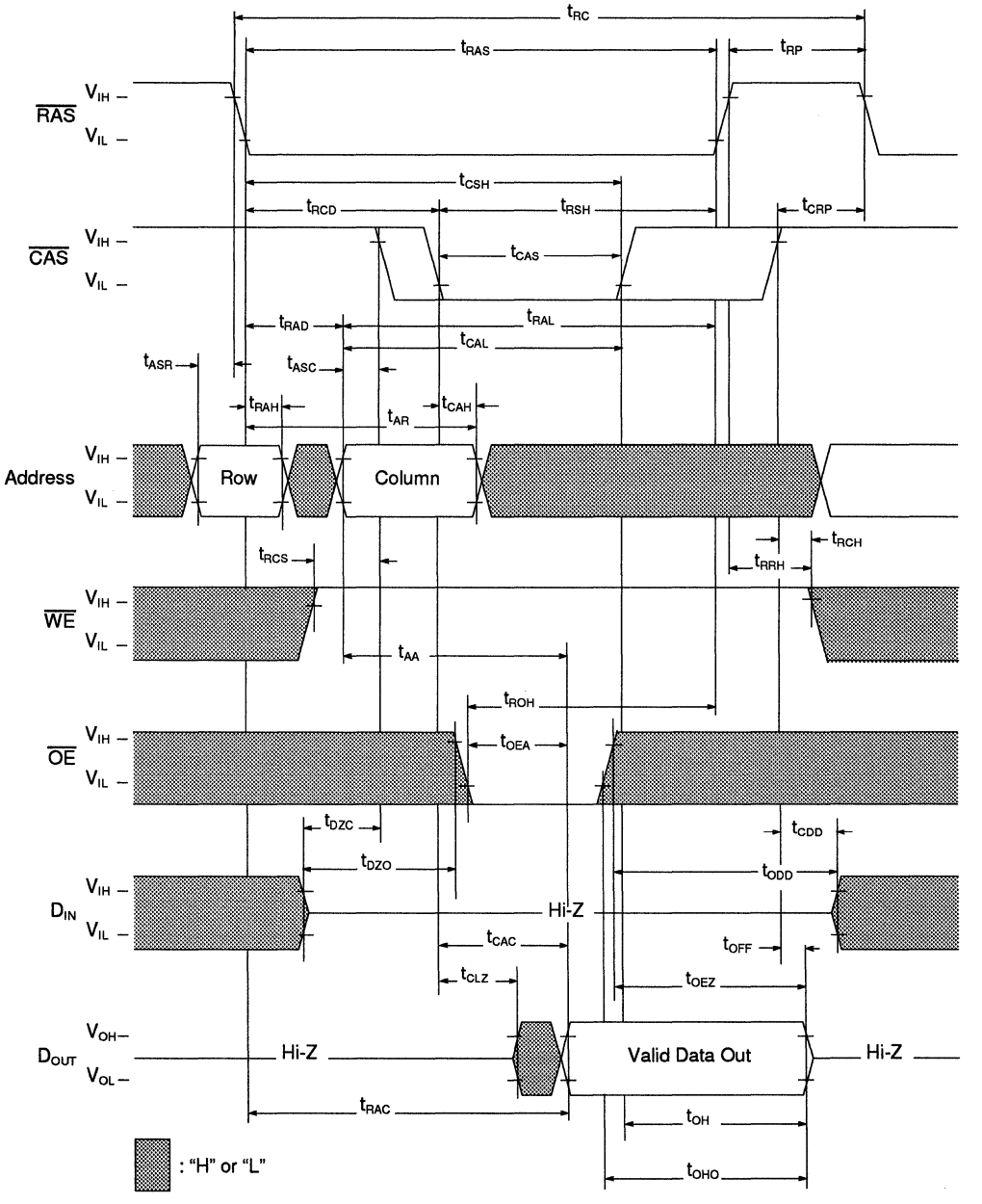
1. 2048 refreshes are required every 32ms.

Presence Detect Read Cycle

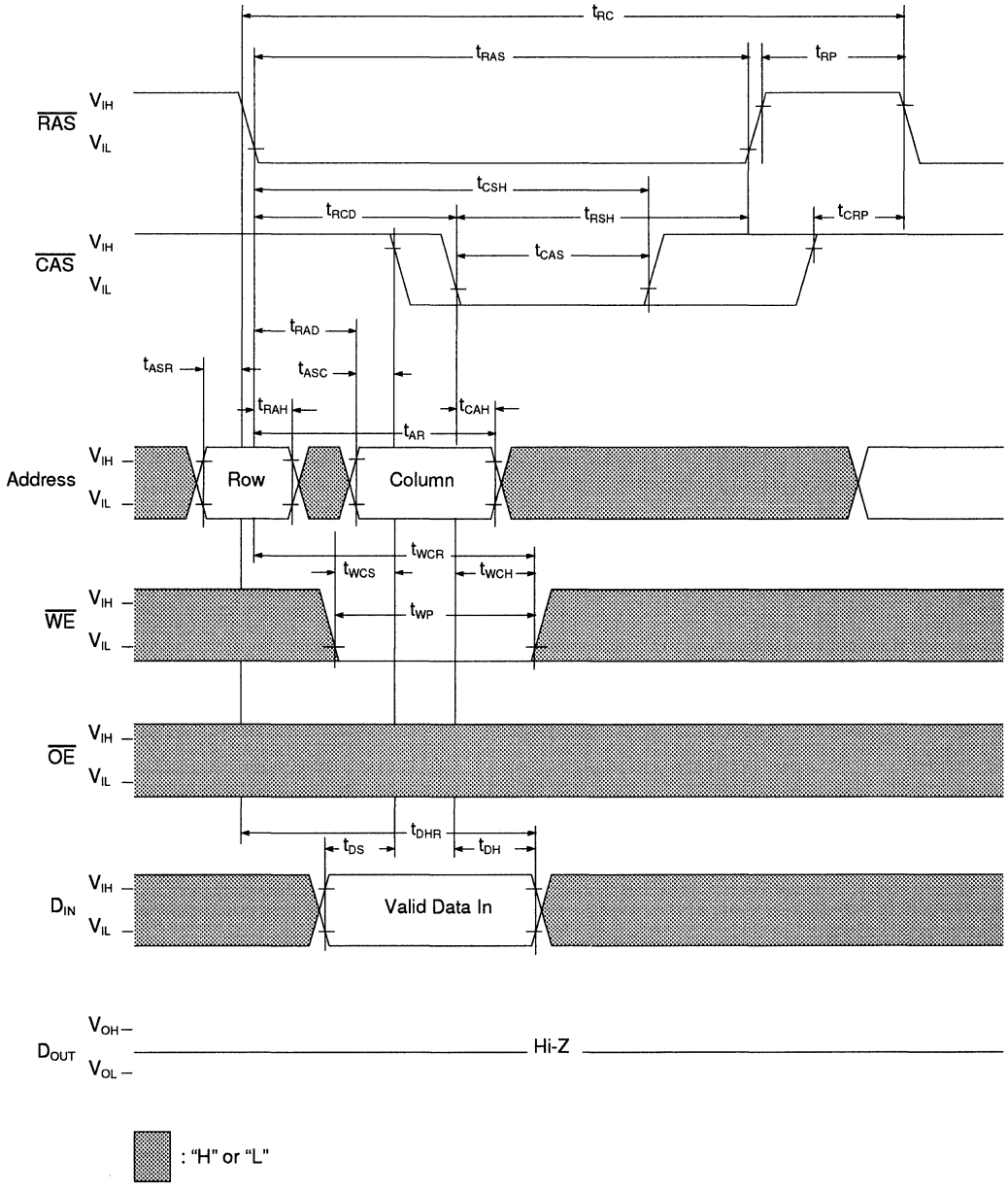
Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

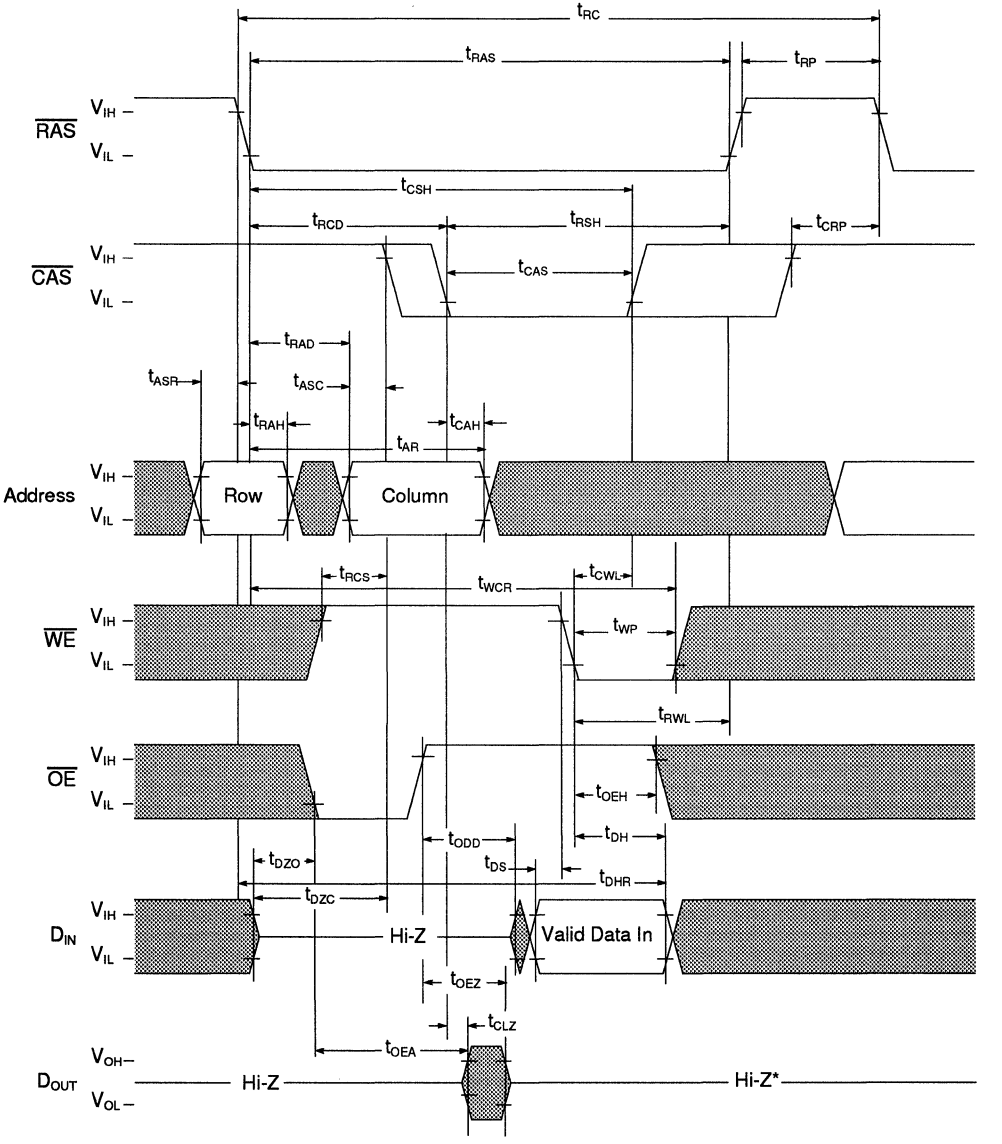
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tAR
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Valid Data Out
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

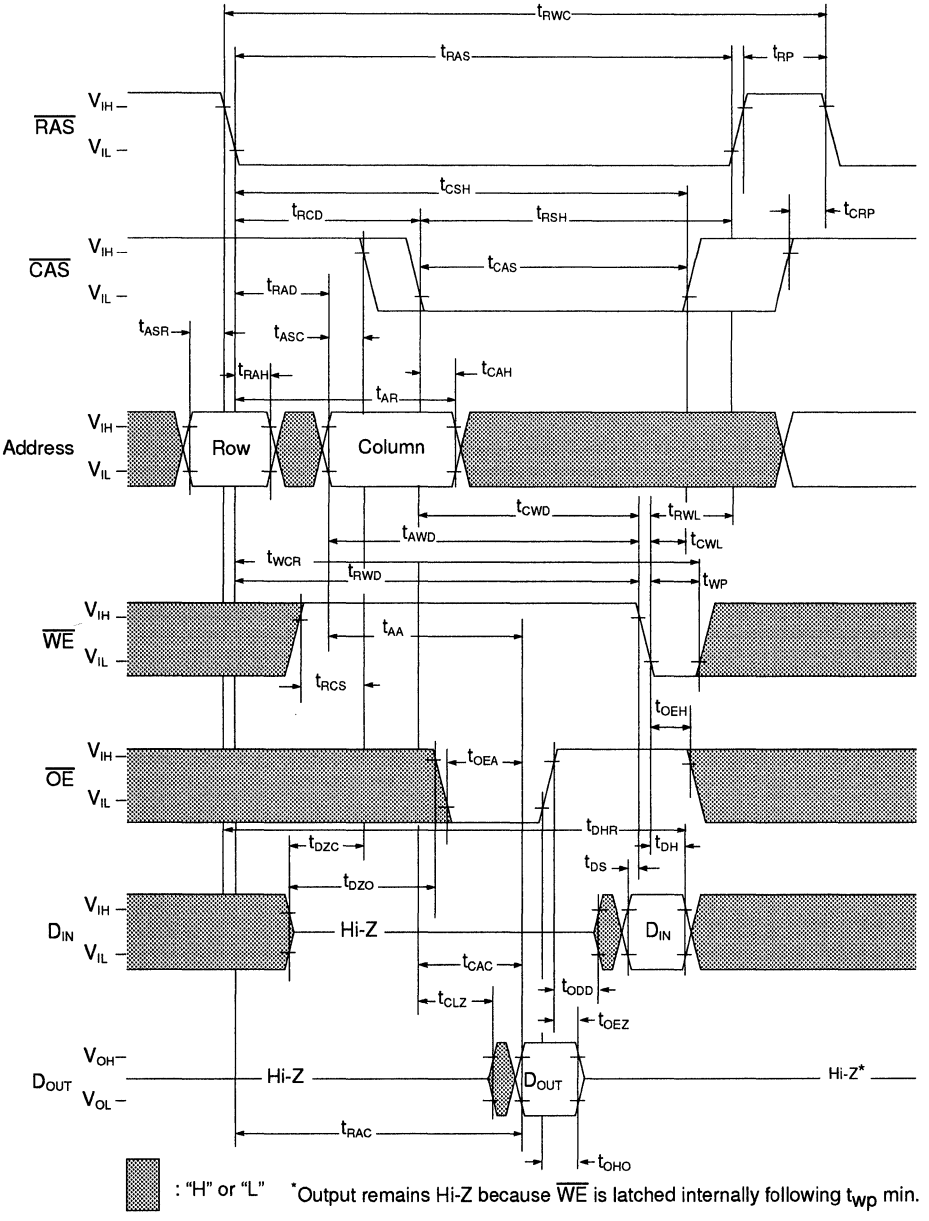


Write Cycle (Late Write)

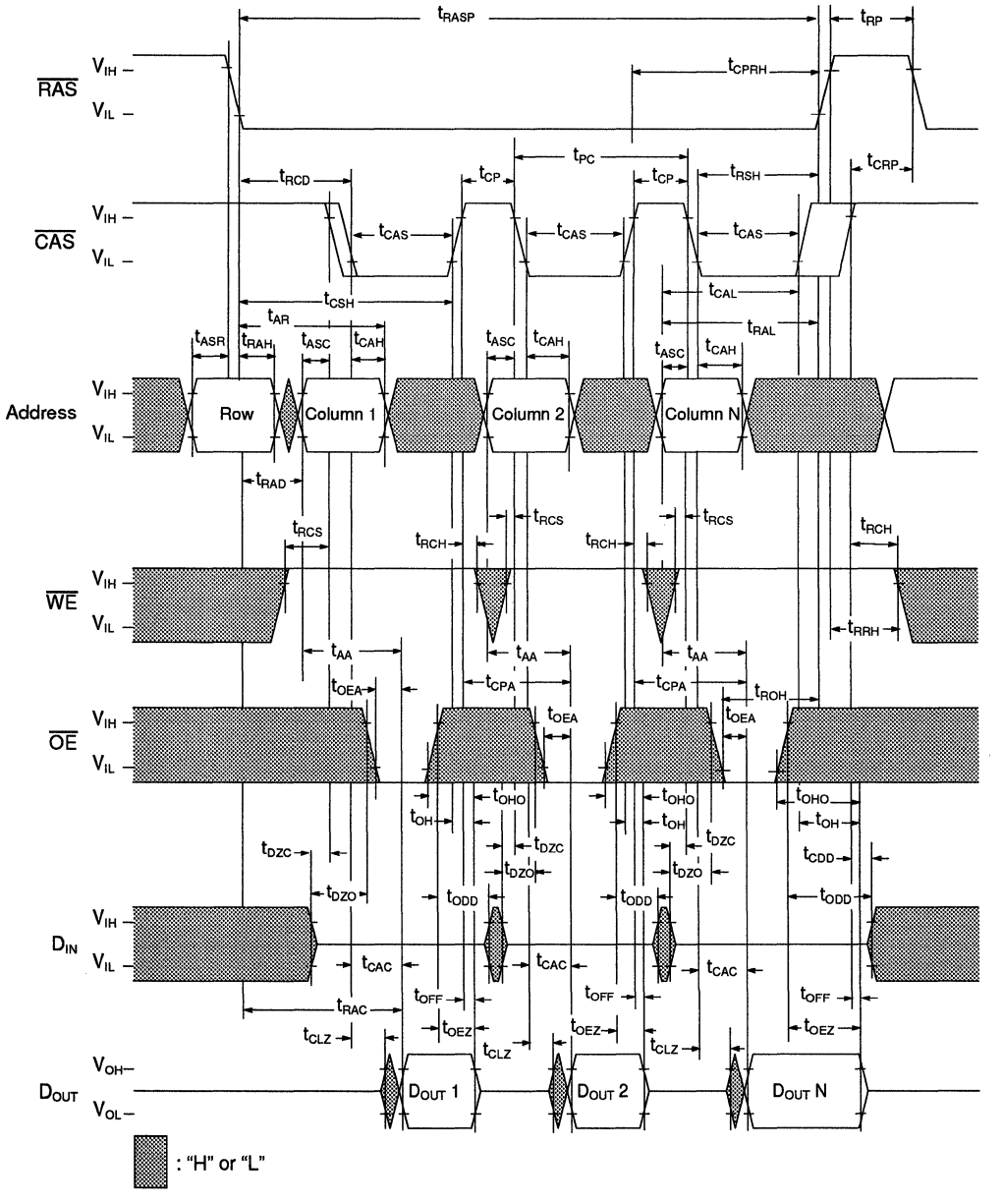


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

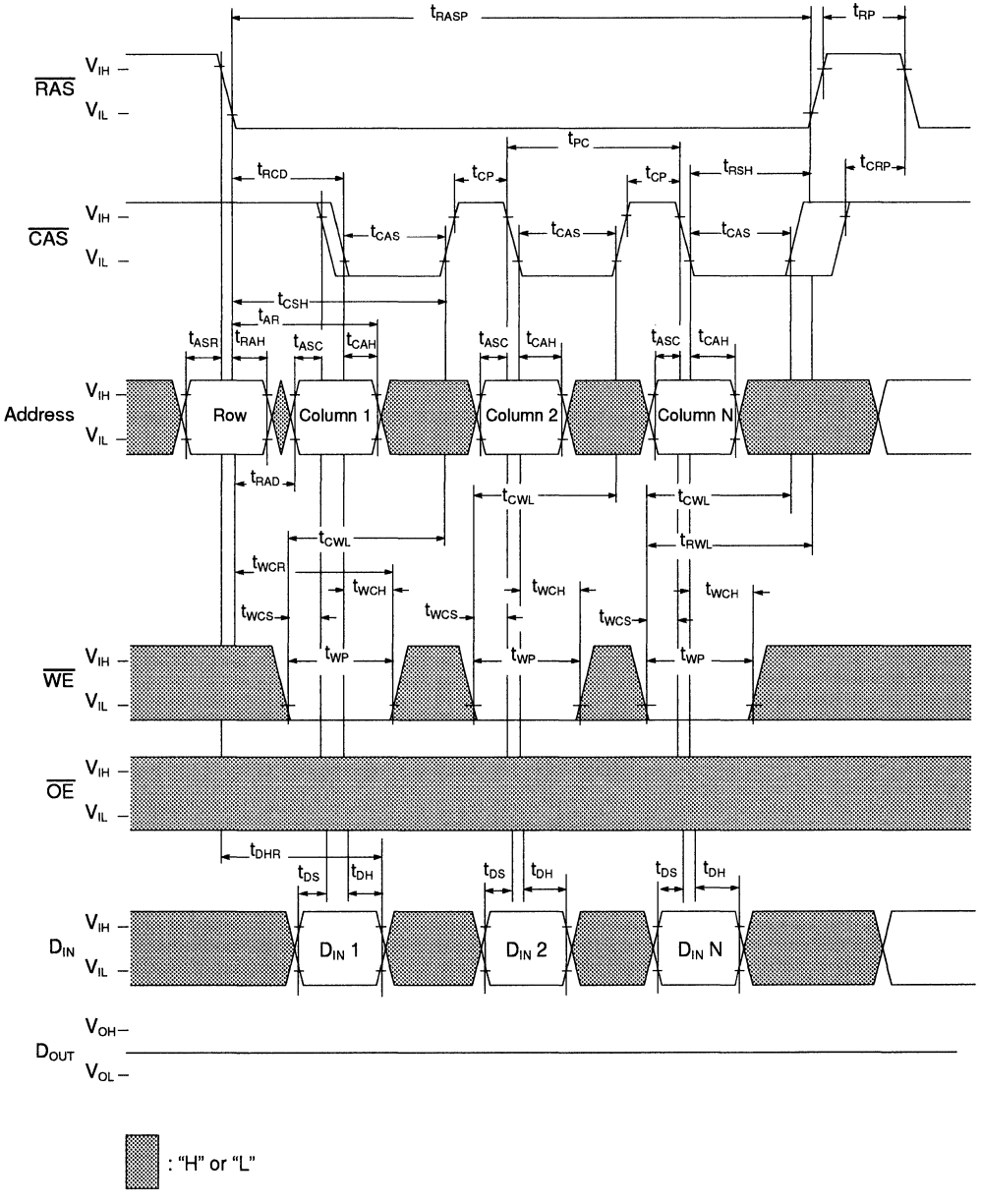
Read-Modify-Write-Cycle



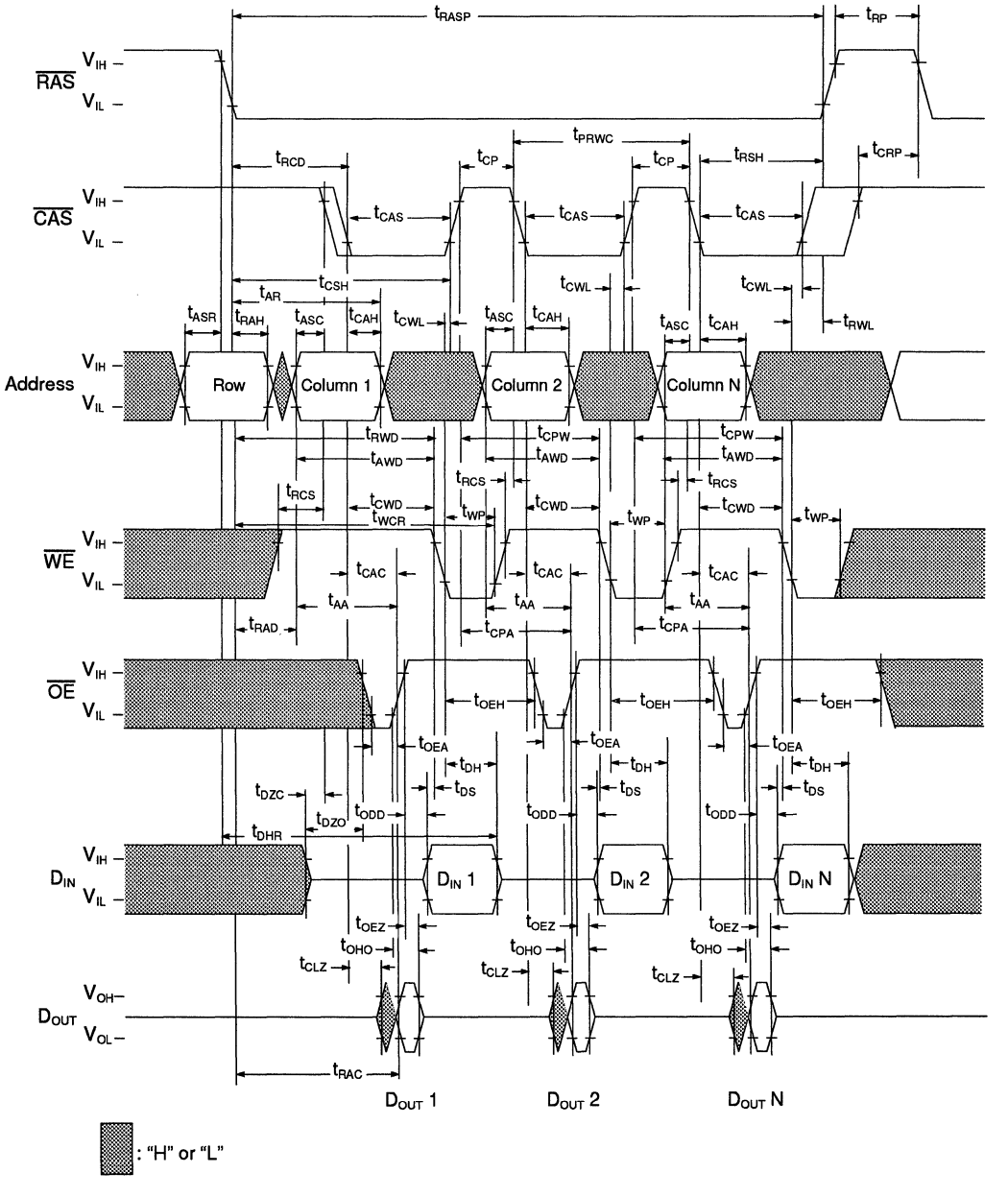
Fast Page Mode Read Cycle



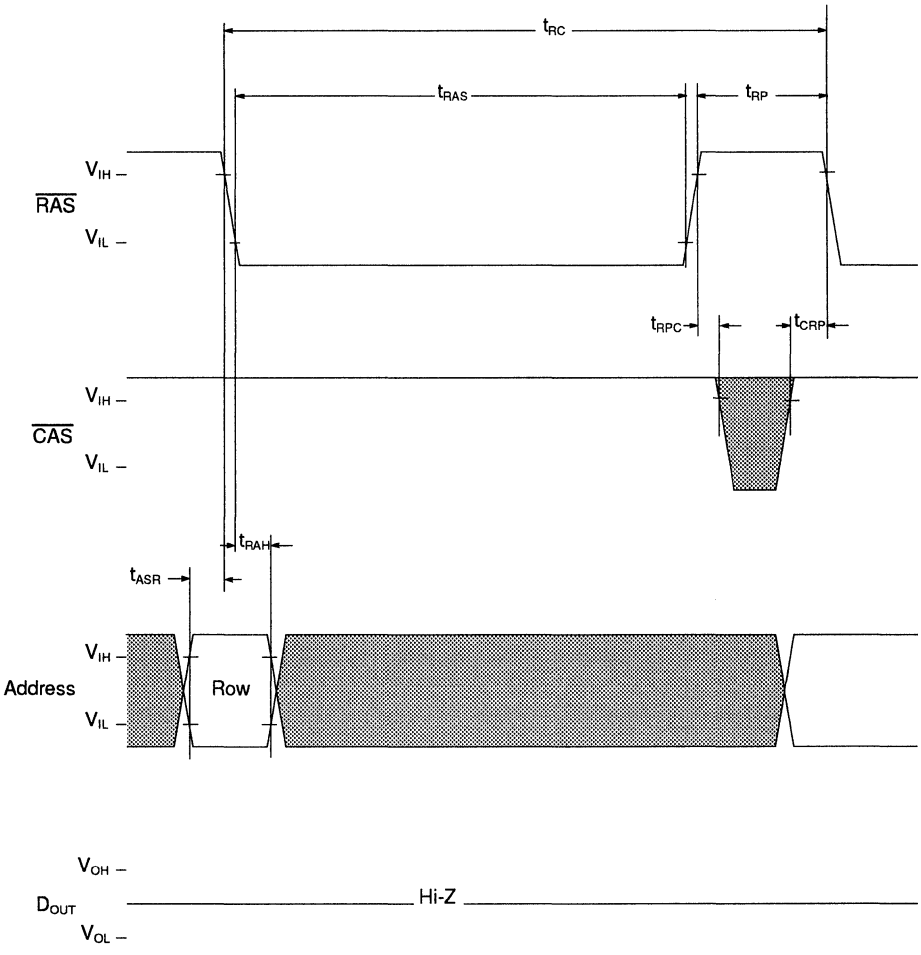
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

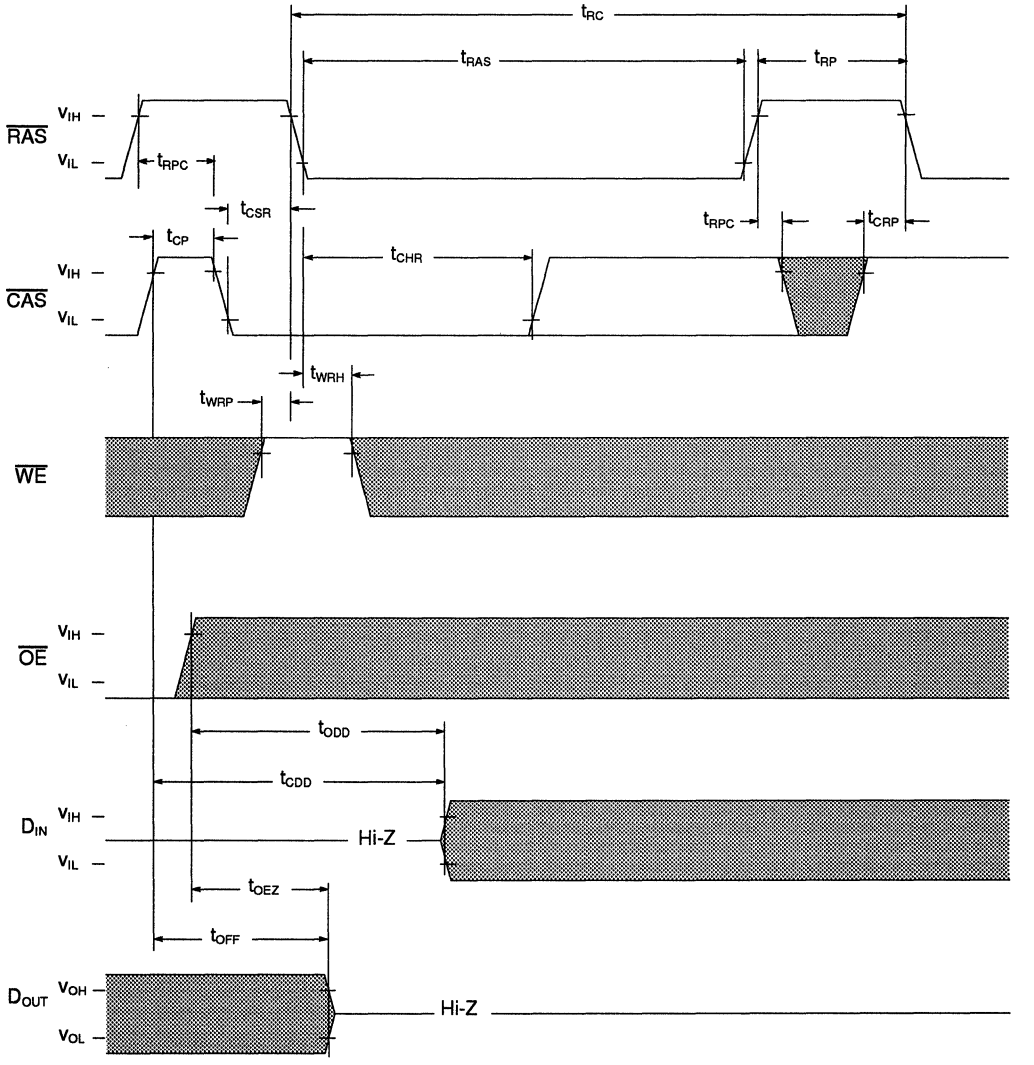


$\overline{\text{RAS}}$ Only Refresh Cycle



Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$, D_{IN} are "H" or "L"

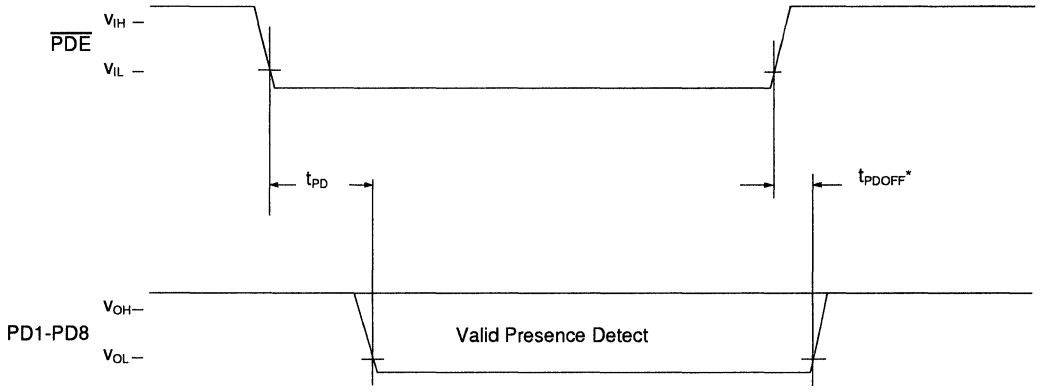
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



: "H" or "L"

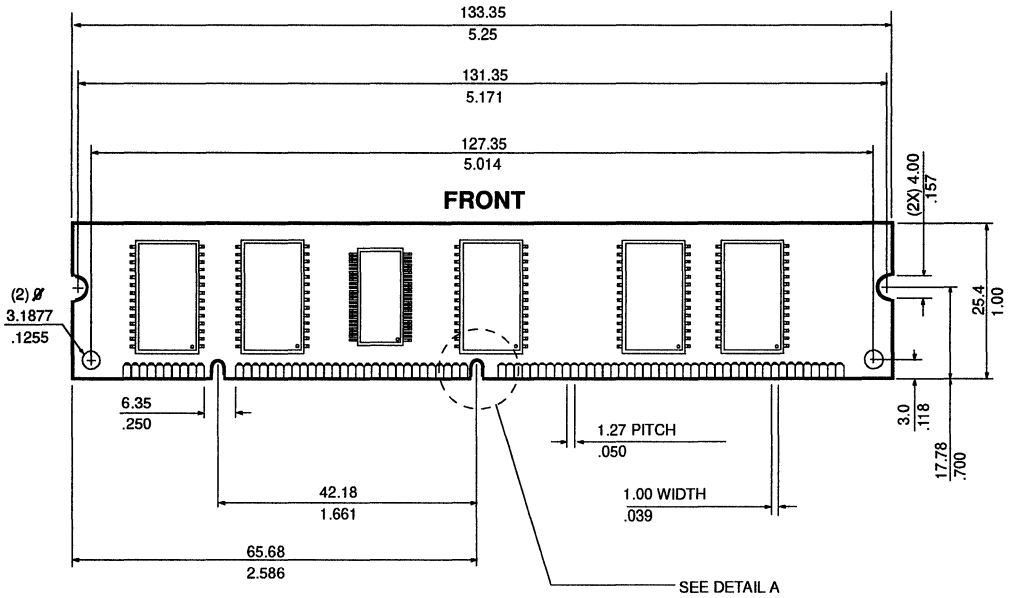
Note: Addresses are "H" or "L"

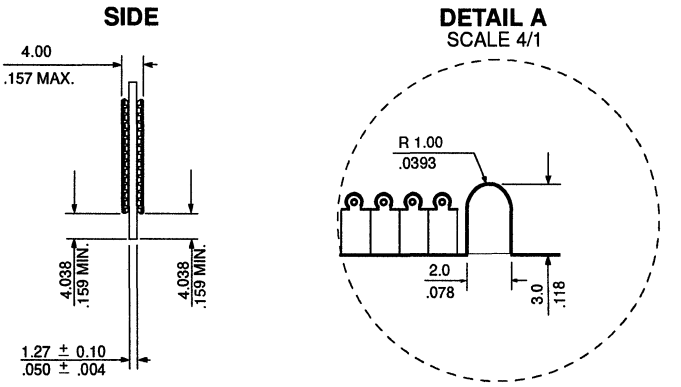
Presence Detect Read Cycle



*PD pins must be pulled high at next level of assembly

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 2Mx72 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are LVTTL and LVCMOS compatible
- Single 3.3V, ± 0.3V Power Supply
- Au contacts
- Optimized for ECC applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 2048 refresh cycles distributed across 32ms
- 11/10 addressing (Row/Column)
- Card size: 5.25" x 1.0" x 0.157"
- DRAMS in TSOP Package

Description

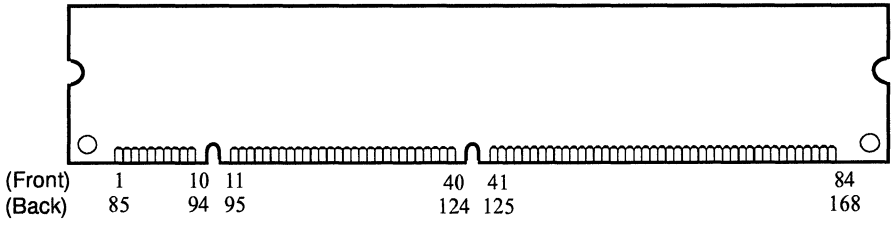
IBM11M2730HB is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 2Mx72 high speed memory array for ECC applications. The DIMM uses 9 2Mx8 DRAMs in TSOP packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, the system will determine that ECC DIMMs are installed if PD8 is low (0). ID0 need not be sensed since both x72 and x80 ECC DIMMs will function in a x72 bank.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 and x72 parity (5V) DIMMs and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A10	Address Inputs (Buffered)
DQx	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

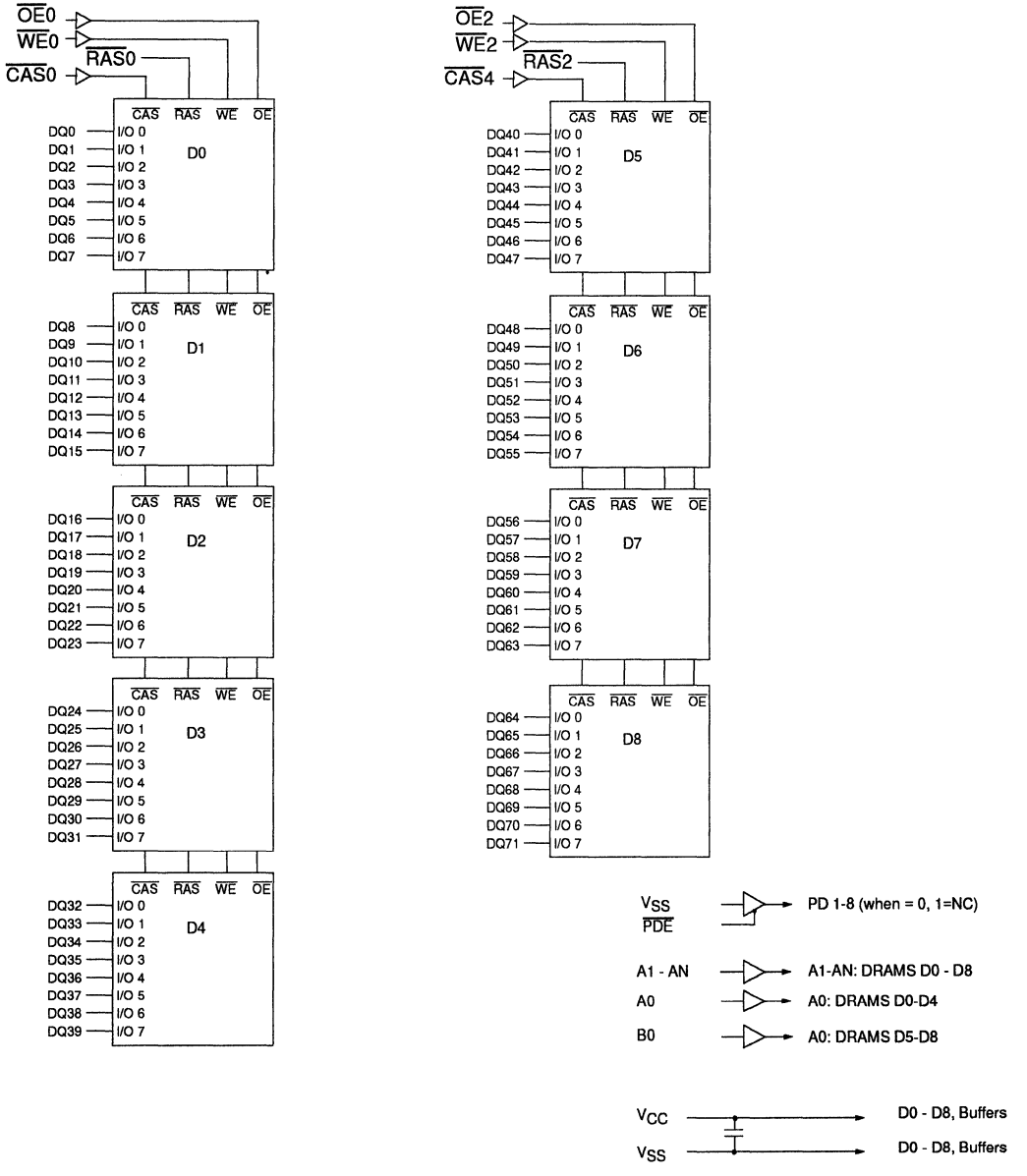
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	NC
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	NC
5	DQ3	89	DQ39	47	NC	131	NC
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	DQ8	95	DQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	DQ17	106	DQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	DQ26	150	DQ62
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	NC	70	DQ29	154	DQ65
29	NC	113	NC	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	NC	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	DQ35	161	DQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	A10	122	NC	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M2730HBA-60	2Mx72	60ns	Au	5.25"x1.0"x 0.157"	
IBM11M2730HBA-70	2Mx72	70ns	Au	5.25"x1.0"x 0.157"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	1	1
PD2	0	0
PD3	0	0
PD4	1	1
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	0	0
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +4.6	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	3.9	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A10)	13	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	40	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF	
C_{I4}	DQ_X Capacitance	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1080	mA	1,2,3
		-70	—	900		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	18	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1080	mA	1,3
		-70	—	900		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	675	mA	1,2,3
		-70	—	585		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	9	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1080	mA	1,3
		-70	—	900		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-50	+50		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	

1. I_{CC1},I_{CC3},I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1},I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the Dram device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	1
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	4
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	—	5
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
2. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.
5. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	2	—	ns	1
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	3
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	36	—	41	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	36	—	41	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	—	—	—	—	ns	4
t_{OH}	Output Data Hold Time	2	—	2	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1, 2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	63	—	73	—	ns	1

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	32	—	32	ms	1

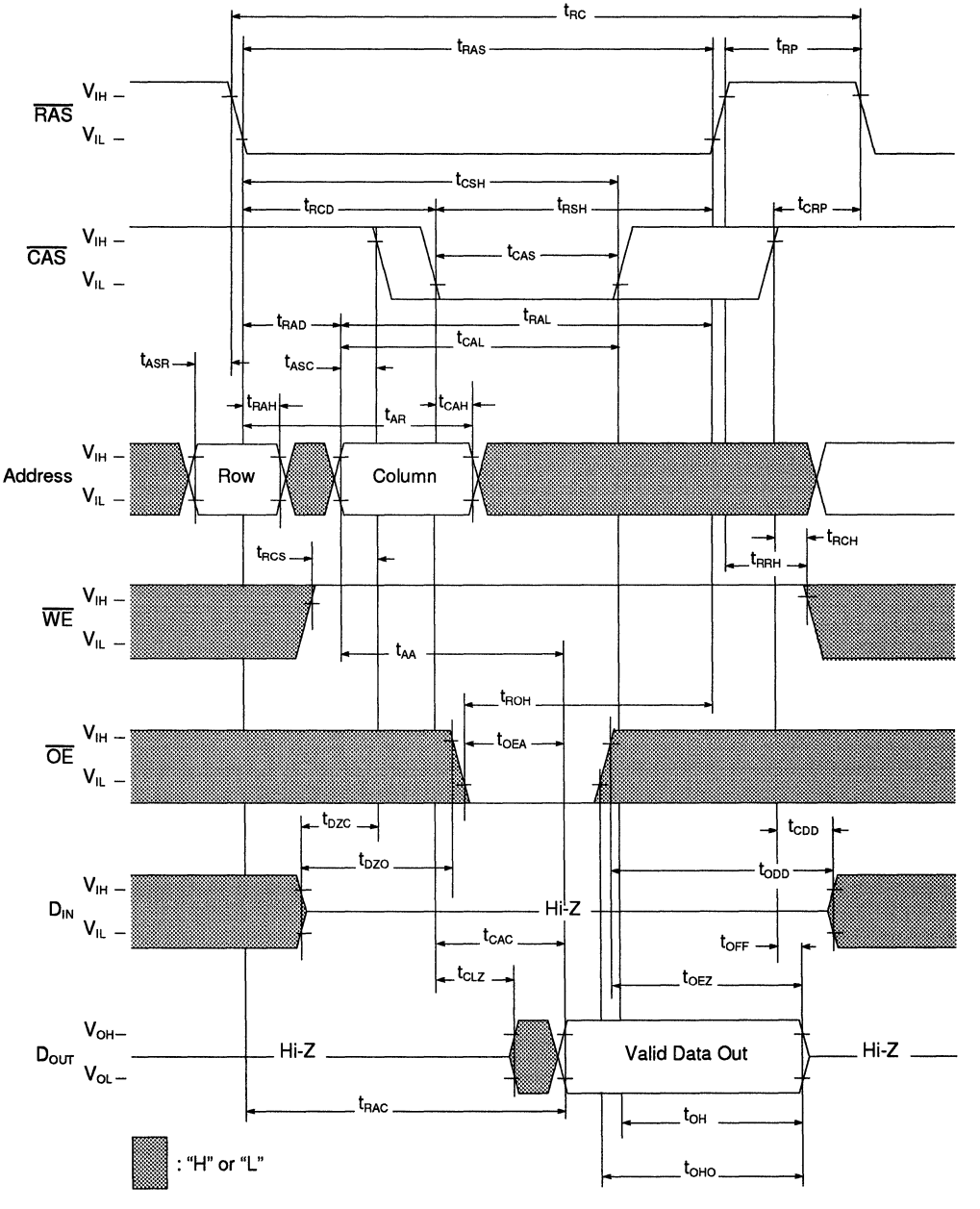
1. 2048 refreshes are required every 32ms.

Presence Detect Read Cycle

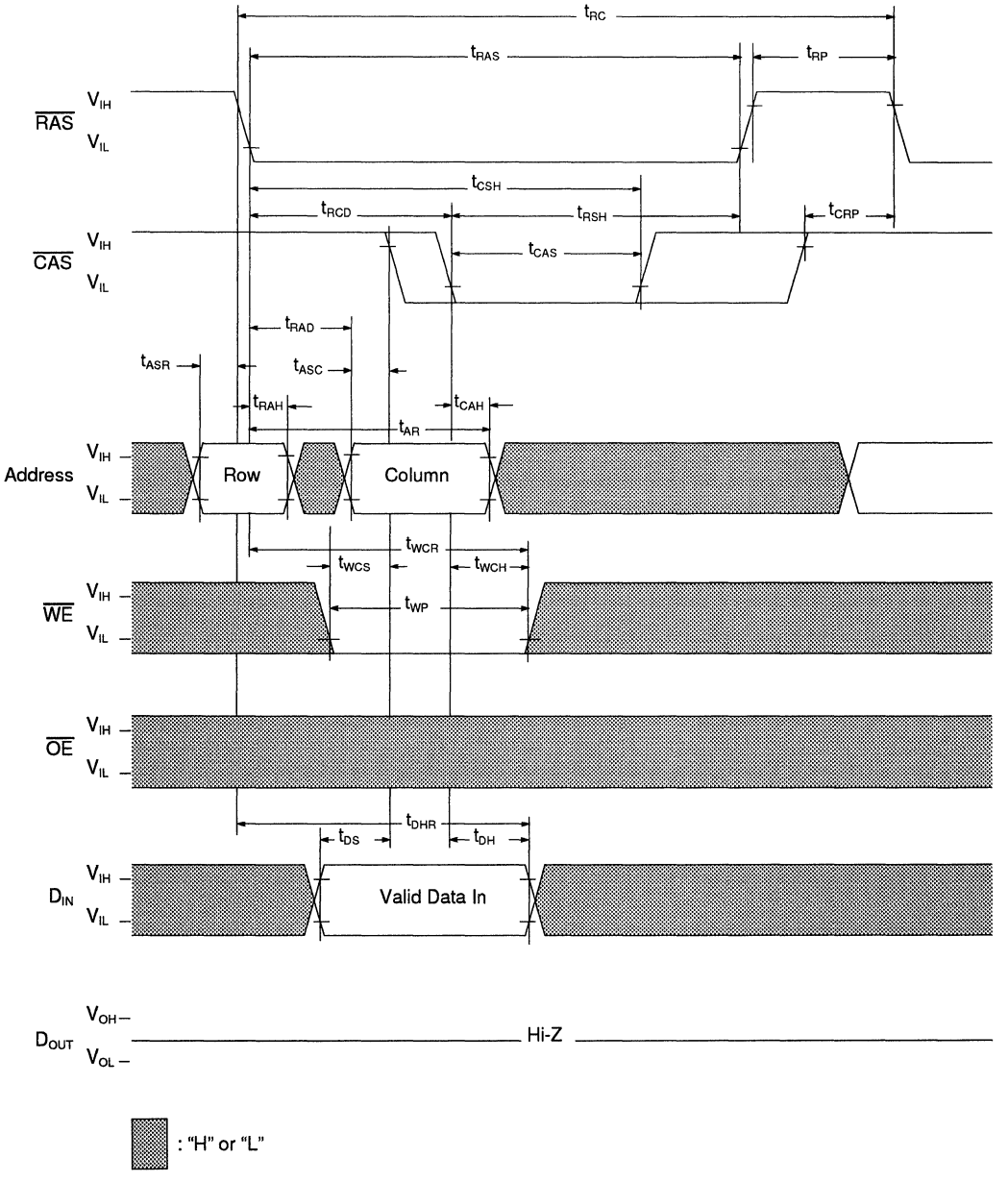
Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

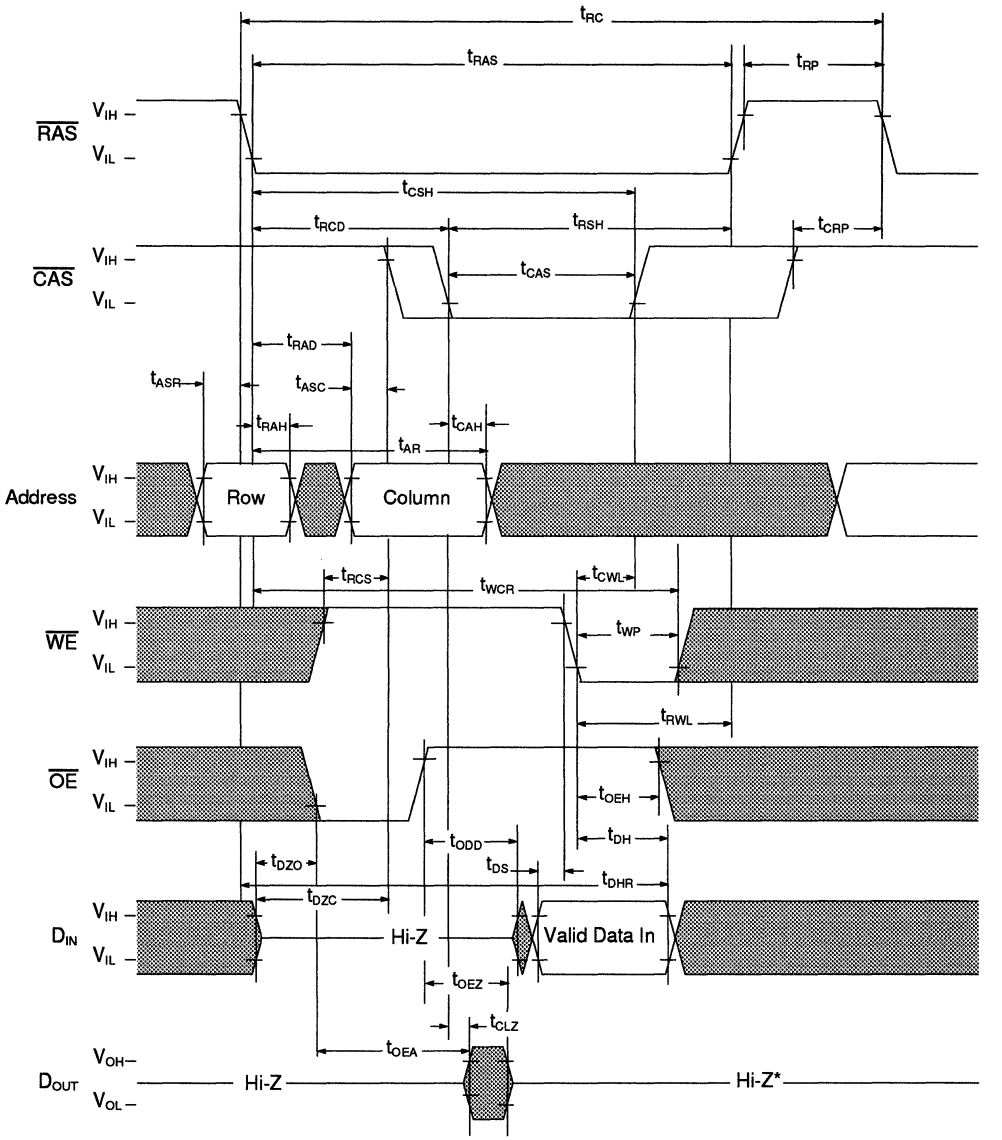
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tAR
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

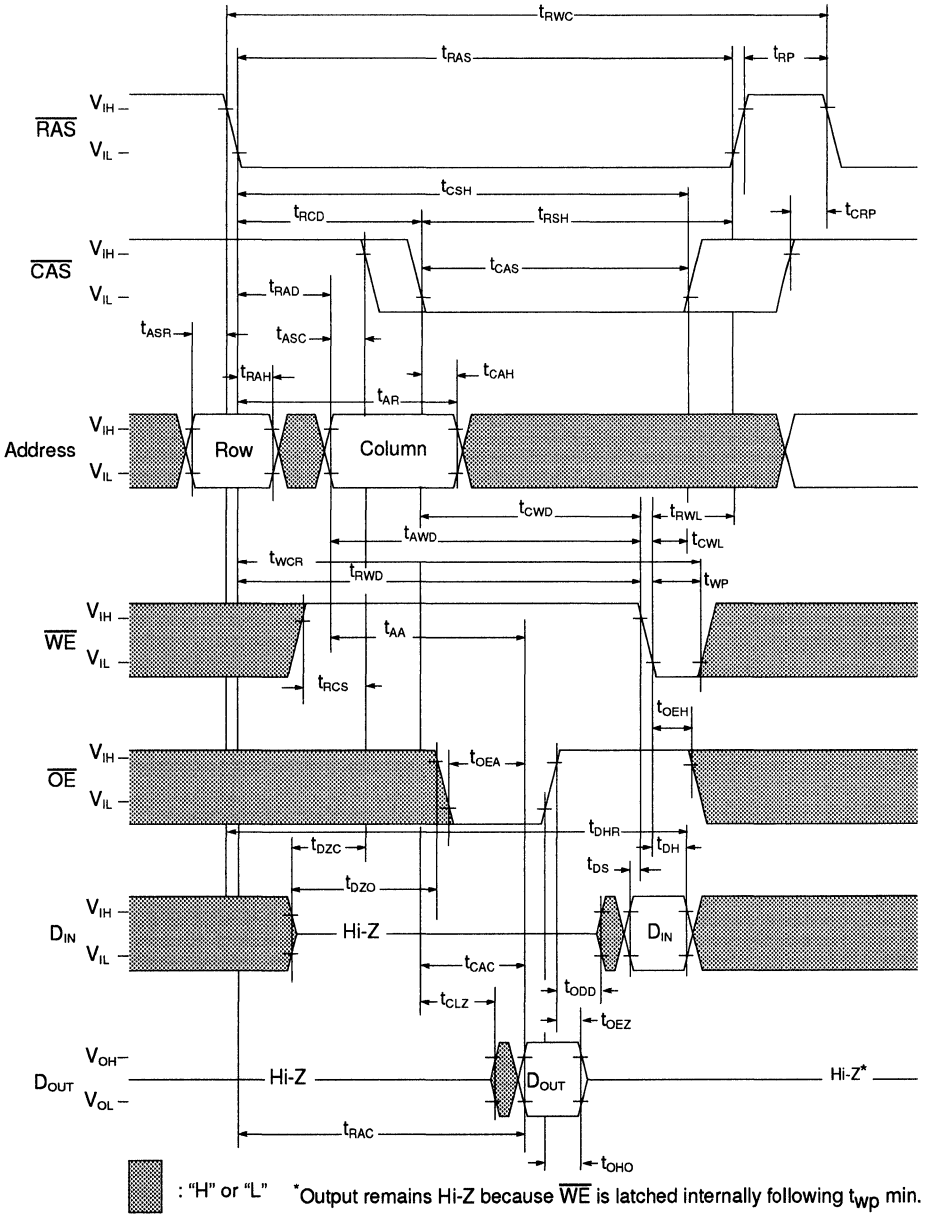


Write Cycle (Late Write)

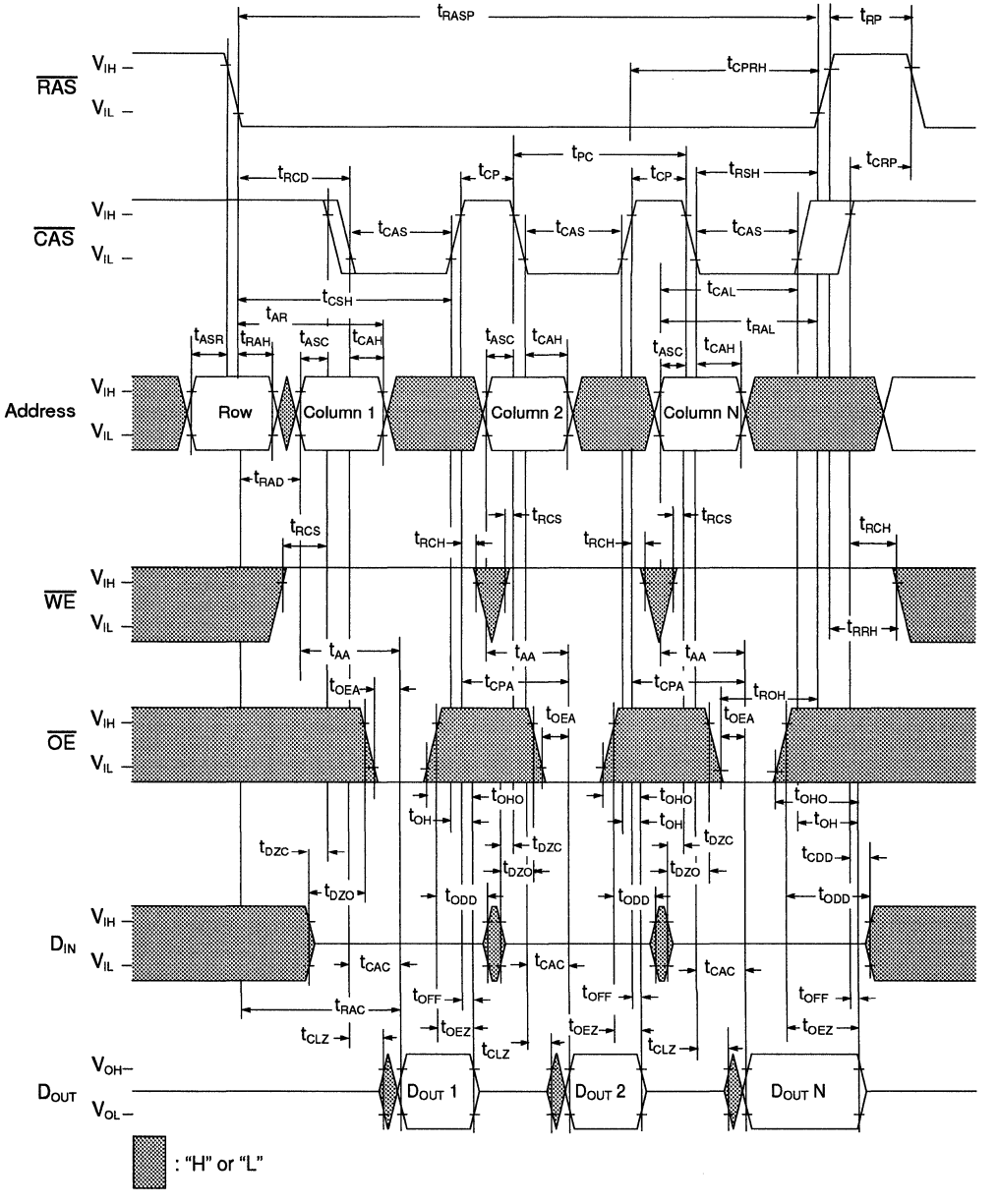


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{wp} min.

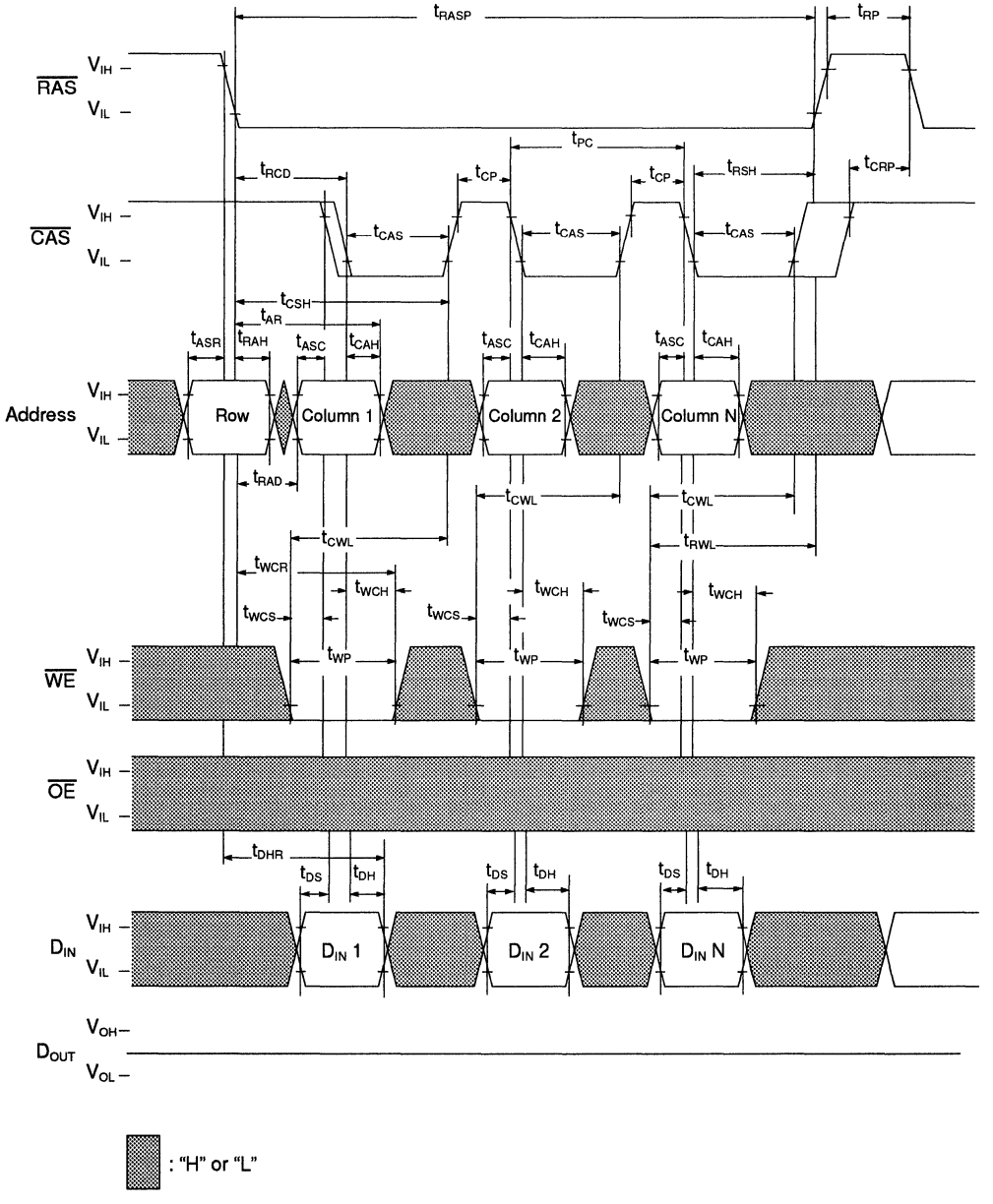
Read-Modify-Write-Cycle



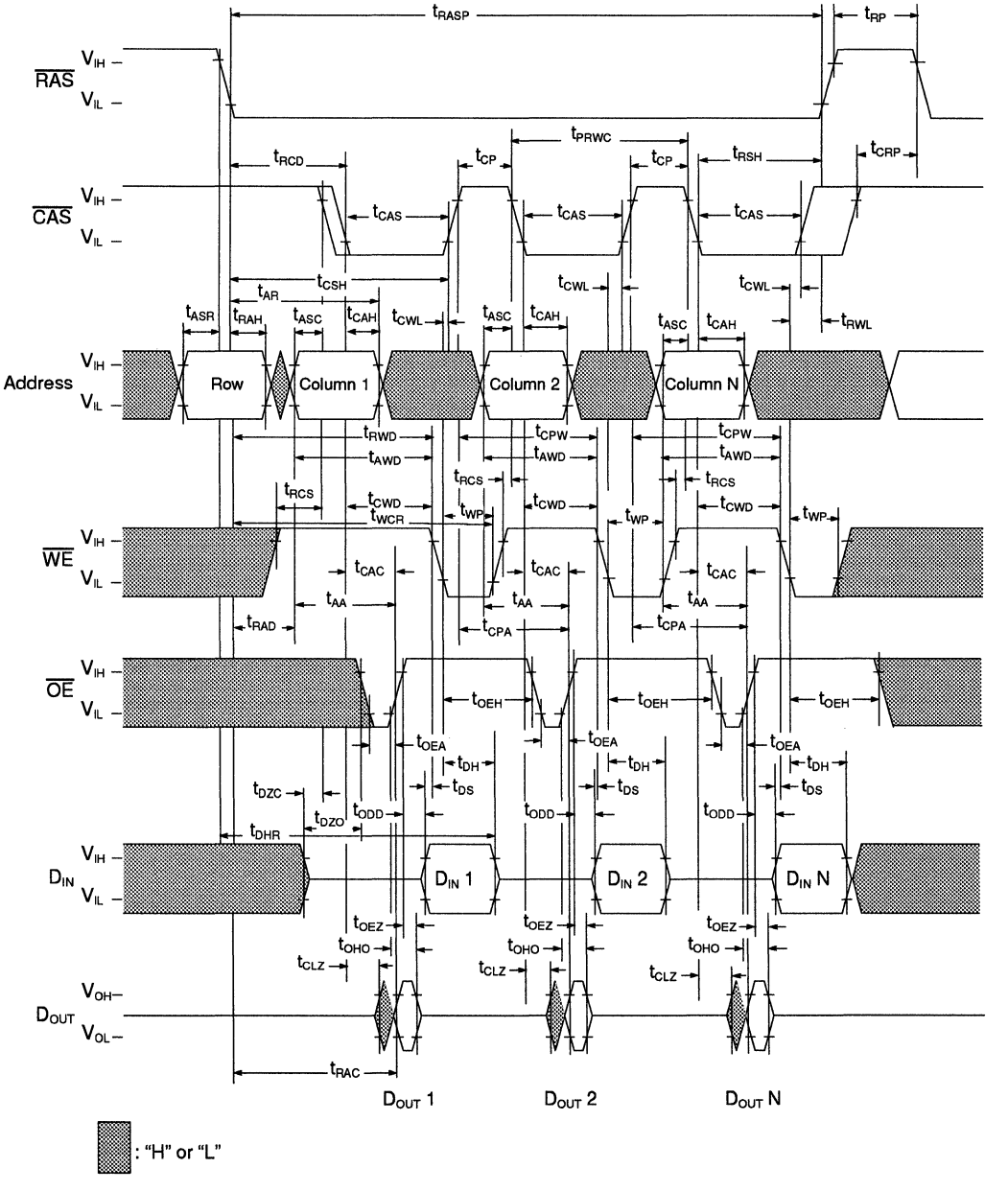
Fast Page Mode Read Cycle



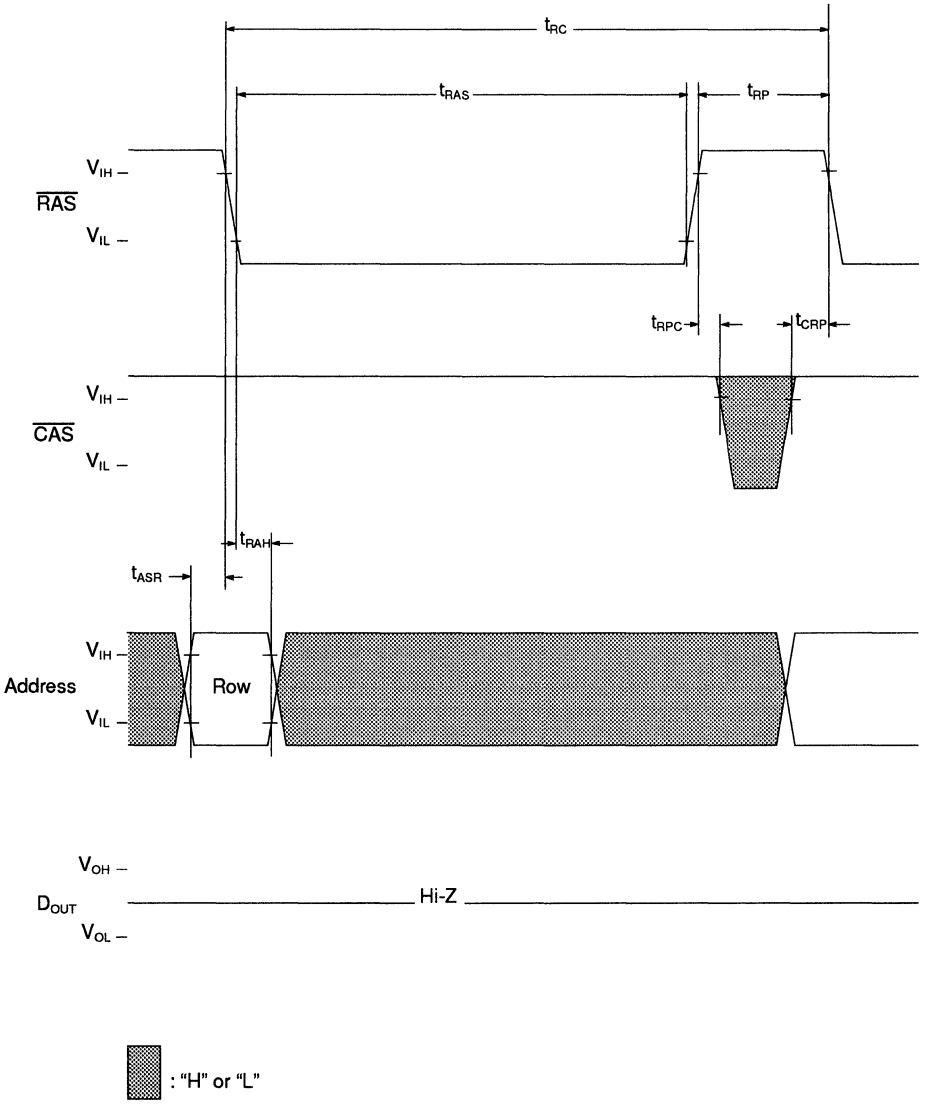
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

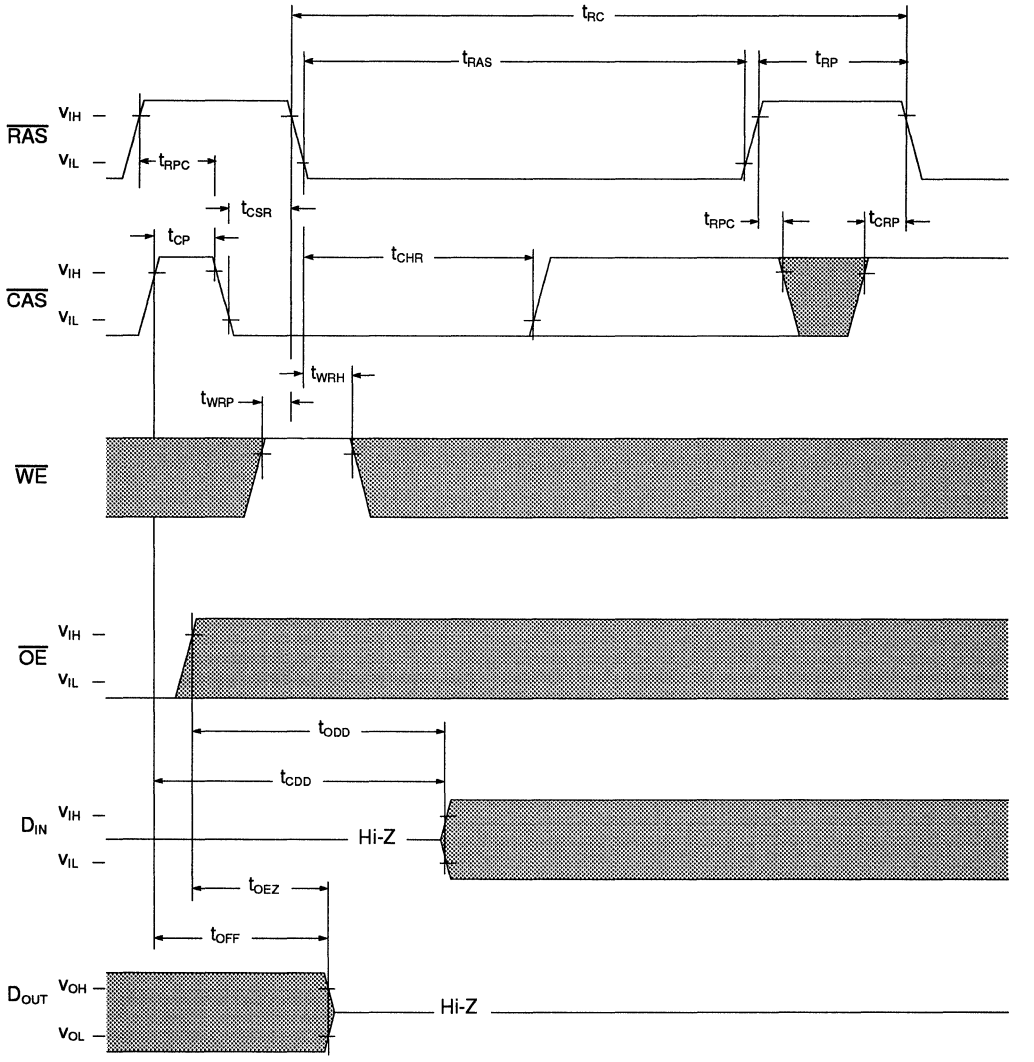


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

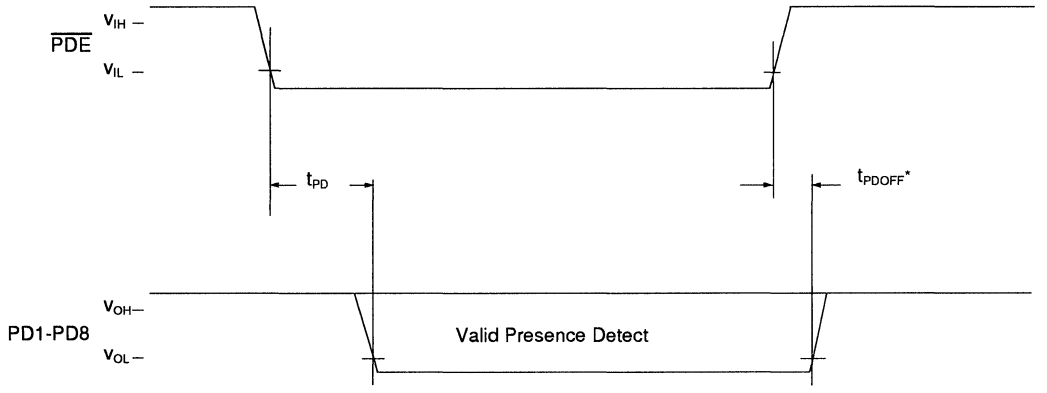
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



: "H" or "L"

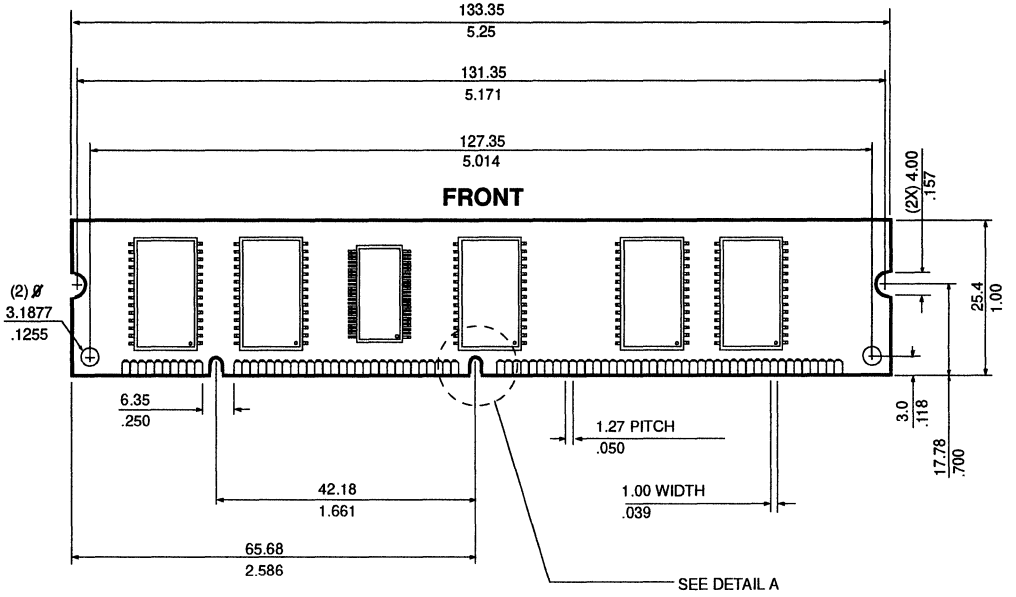
Note: Addresses are "H" or "L"

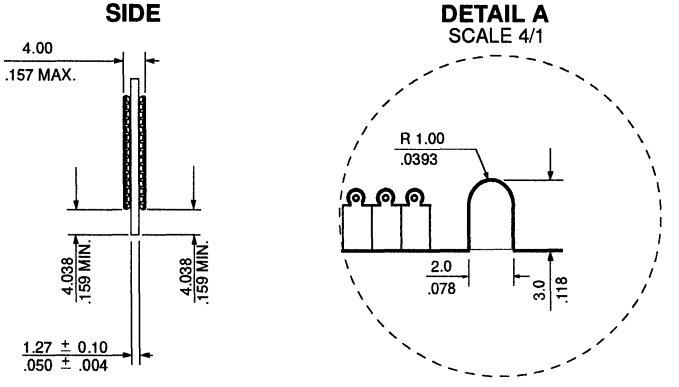
Presence Detect Read Cycle



*PD pins must be pulled high at next level of assembly

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 4Mx72 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are TTL and CMOS compatible
- Single 5.0V, ± 0.5V Power Supply
- Au contacts
- Optimized for ECC applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - 4 Byte Interleave enabled
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 4096 refresh cycles distributed across 64ms
- 12/10 addressing (Row/Column)
- Card size: 5.25" x 1.0" x 0.354"
- DRAMS in SOJ Package

Description

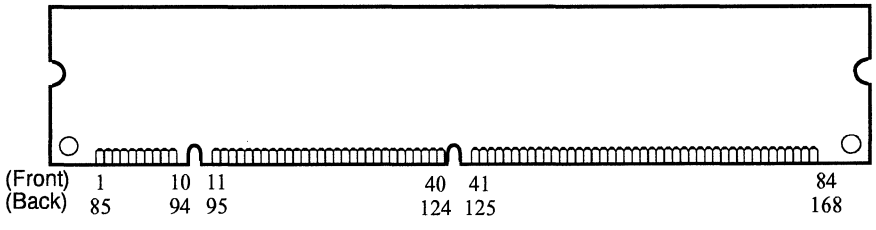
IBM11M4730C is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 4Mx72 high speed memory array for ECC applications. The DIMM uses 18 4Mx4 DRAMs in SOJ packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, the system will determine that ECC DIMMs are installed if PD8 is low (0). ID0 need not be sensed since both x72 and x80 ECC DIMMs will function in a x72 bank.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 and x72 parity (5V) DIMMs and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A11	Address Inputs (Buffered)
DQx	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

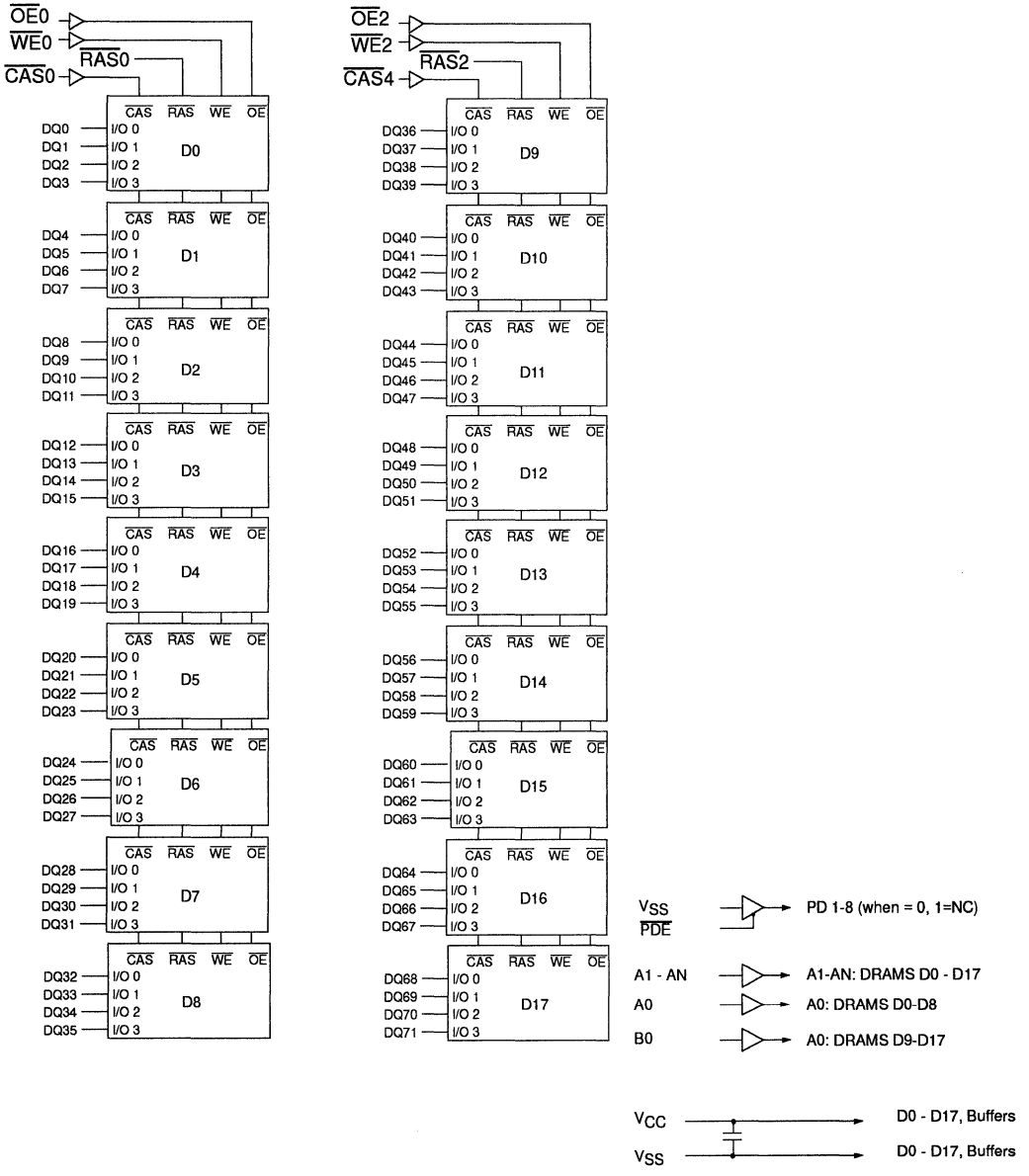
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	NC
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	NC
5	DQ3	89	DQ39	47	NC	131	NC
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	DQ8	95	DQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	DQ17	106	DQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	DQ26	150	DQ62
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	NC	70	DQ29	154	DQ65
29	NC	113	NC	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	NC	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	DQ35	161	DQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	A10	122	A11	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M4730CA-60	4Mx72	60ns	Au	5.25"x1.0"x 0.354"	
IBM11M4730CA-70	4Mx72	70ns	Au	5.25"x1.0"x 0.354"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	1	1
PD2	1	1
PD3	0	0
PD4	1	1
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	0	0
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	8.4	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A11)	13	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	70	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF	
C_{I4}	DQ_X Capacitance	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1530	mA	1,2,3
		-70	—	1350		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	36	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1530	mA	1,3
		-70	—	1350		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1350	mA	1,2,3
		-70	—	1170		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	18	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1530	mA	1,3
		-70	—	1350		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1},I_{CC3},I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1},I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required..
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the Dram device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	1
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	4
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	5
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
2. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.
5. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	2	—	ns	1
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	3
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	36	—	41	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	36	—	41	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	—	—	—	—	ns	4
t_{OH}	Output Data Hold Time	2	—	2	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1, 2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	63	—	73	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	64	—	64	ms	1

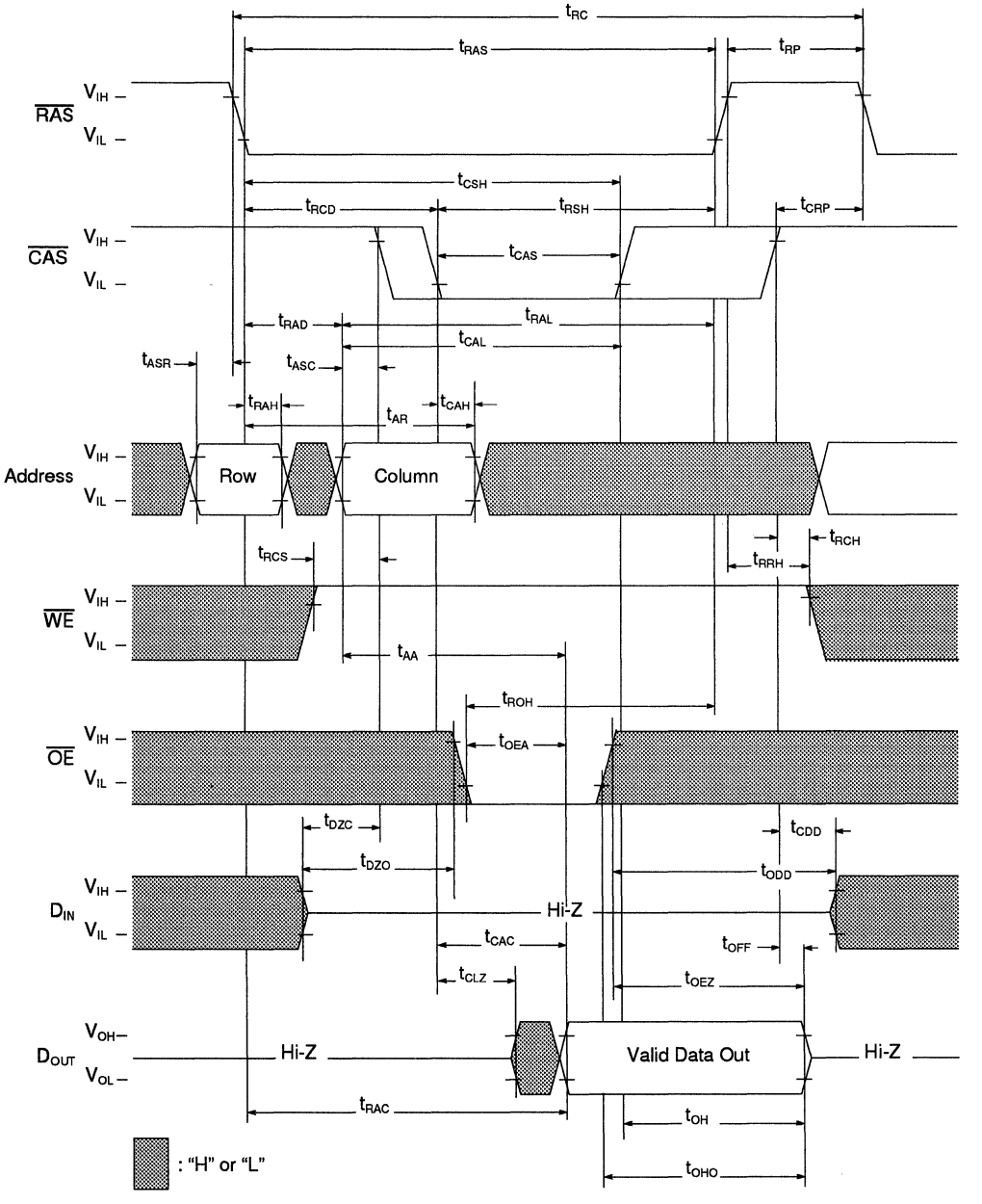
1. 4096 refreshes are required every 64ms.

Presence Detect Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Read Cycle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tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
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CAS
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Column
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tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
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Valid Data Out
tRAC
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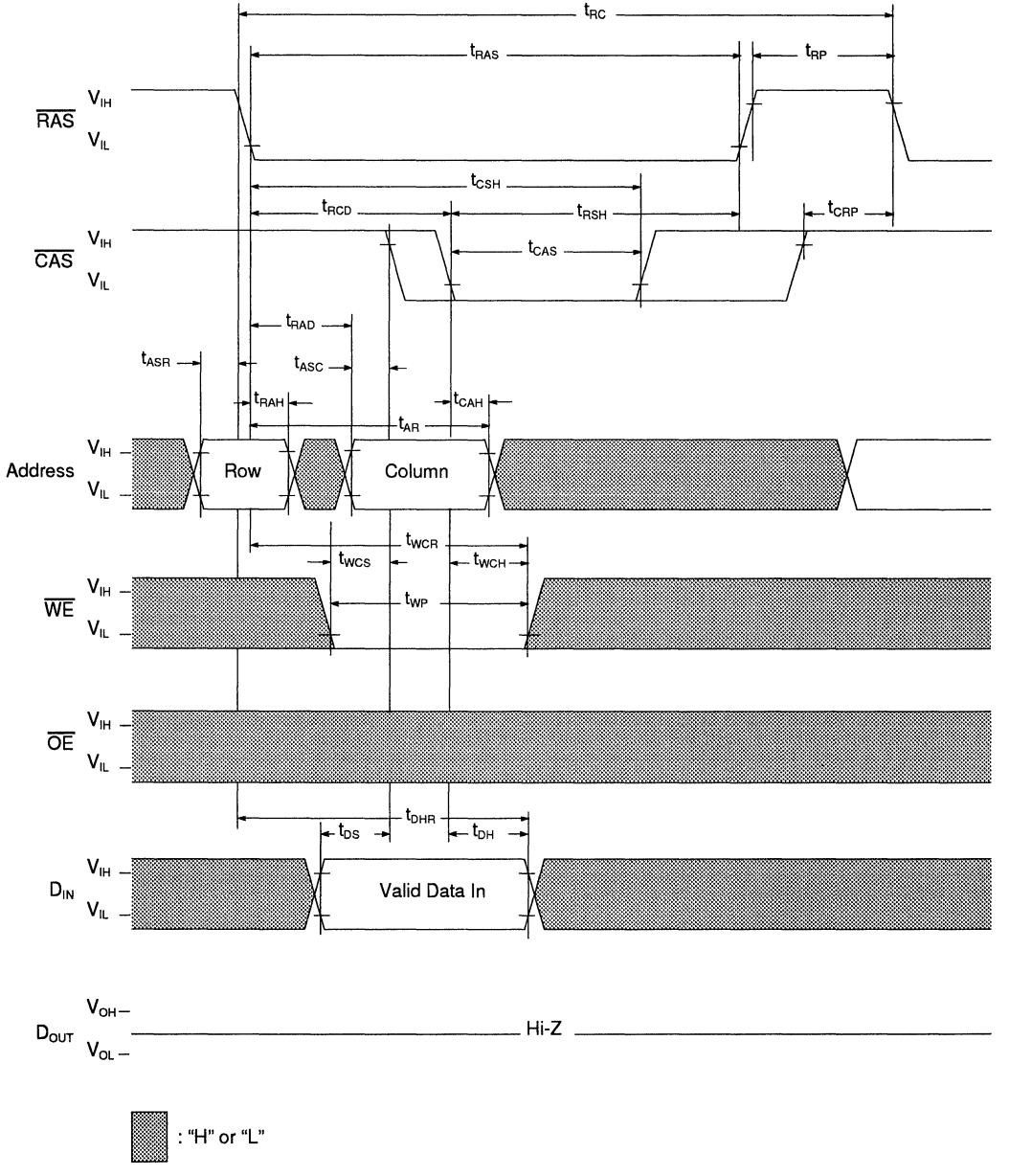
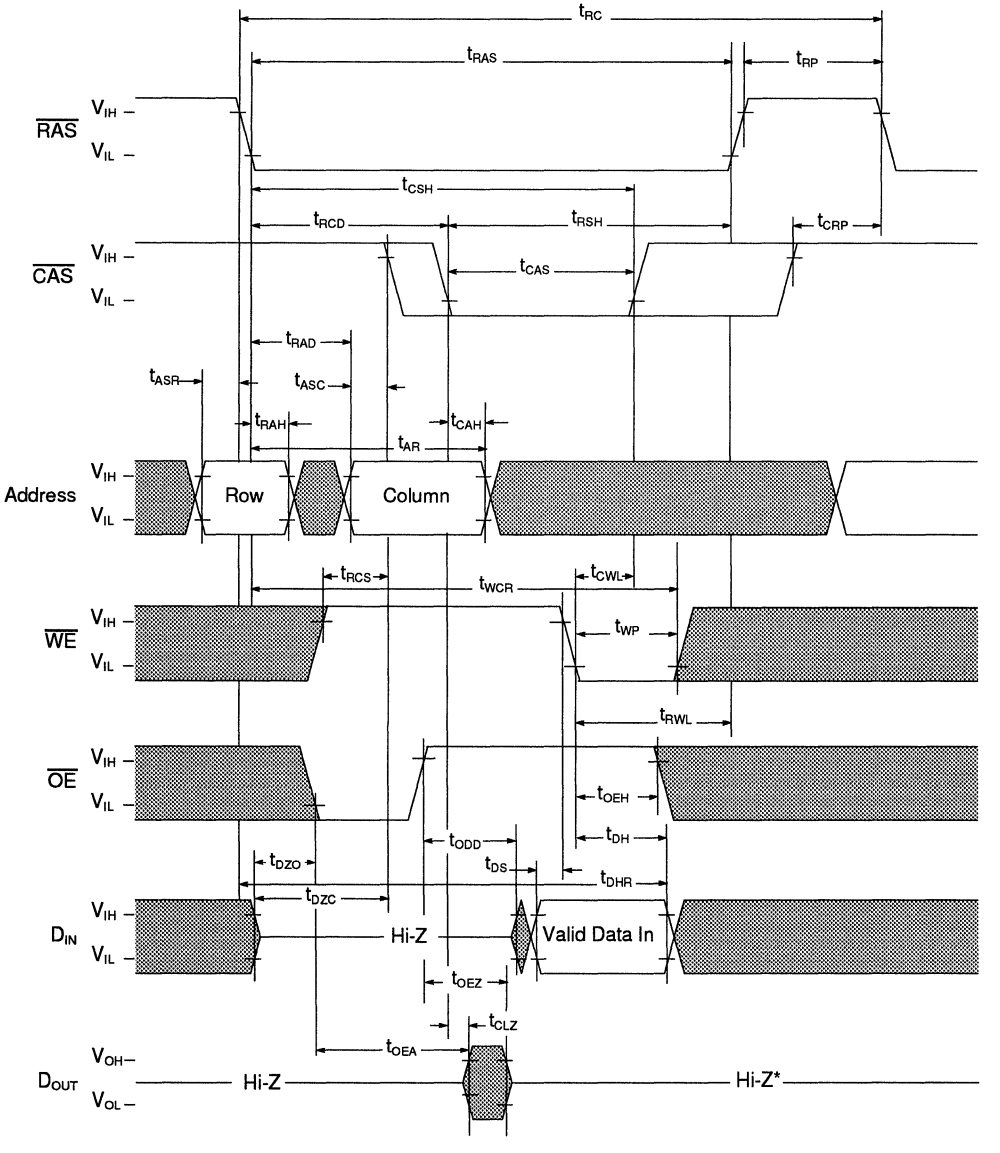
Write Cycle (Early Write)

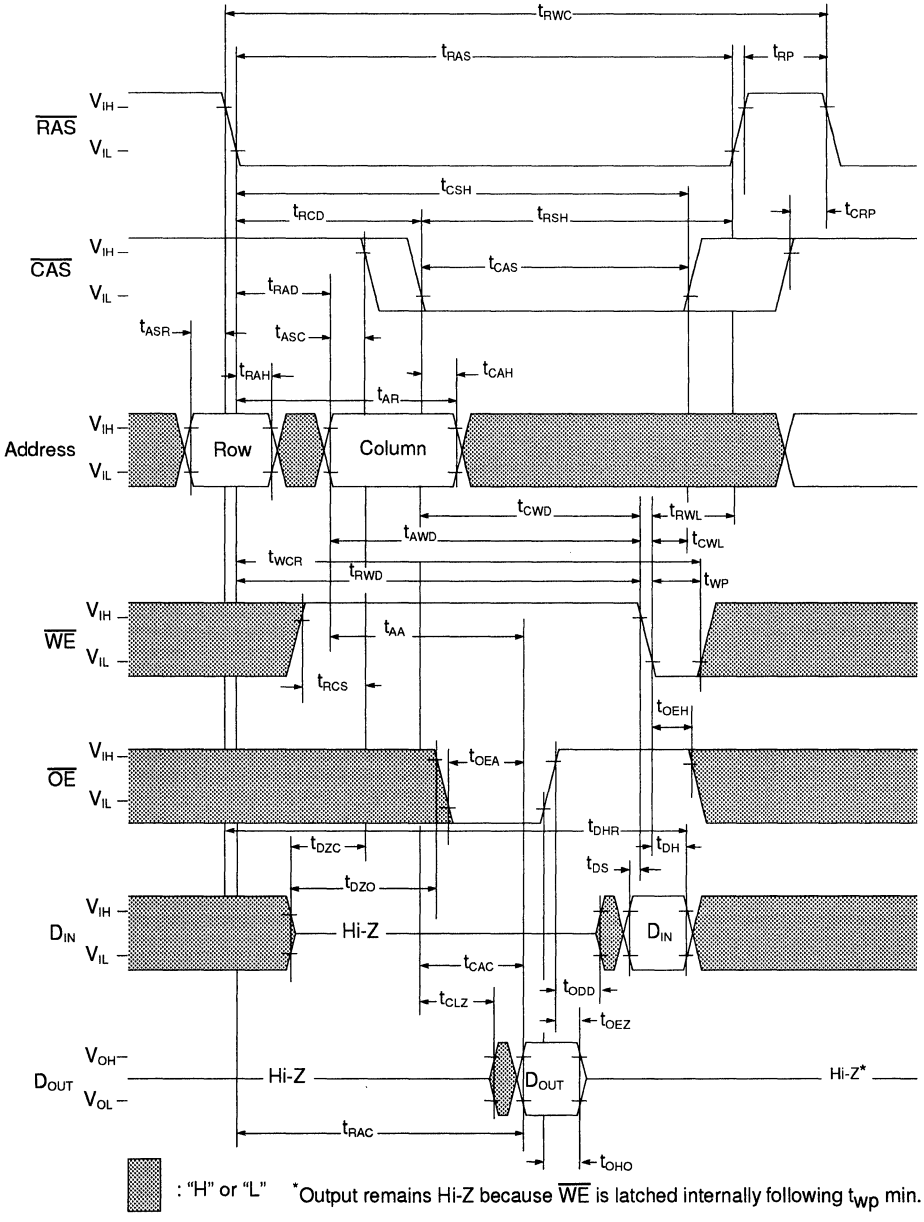


Write Cycle (Late Write)

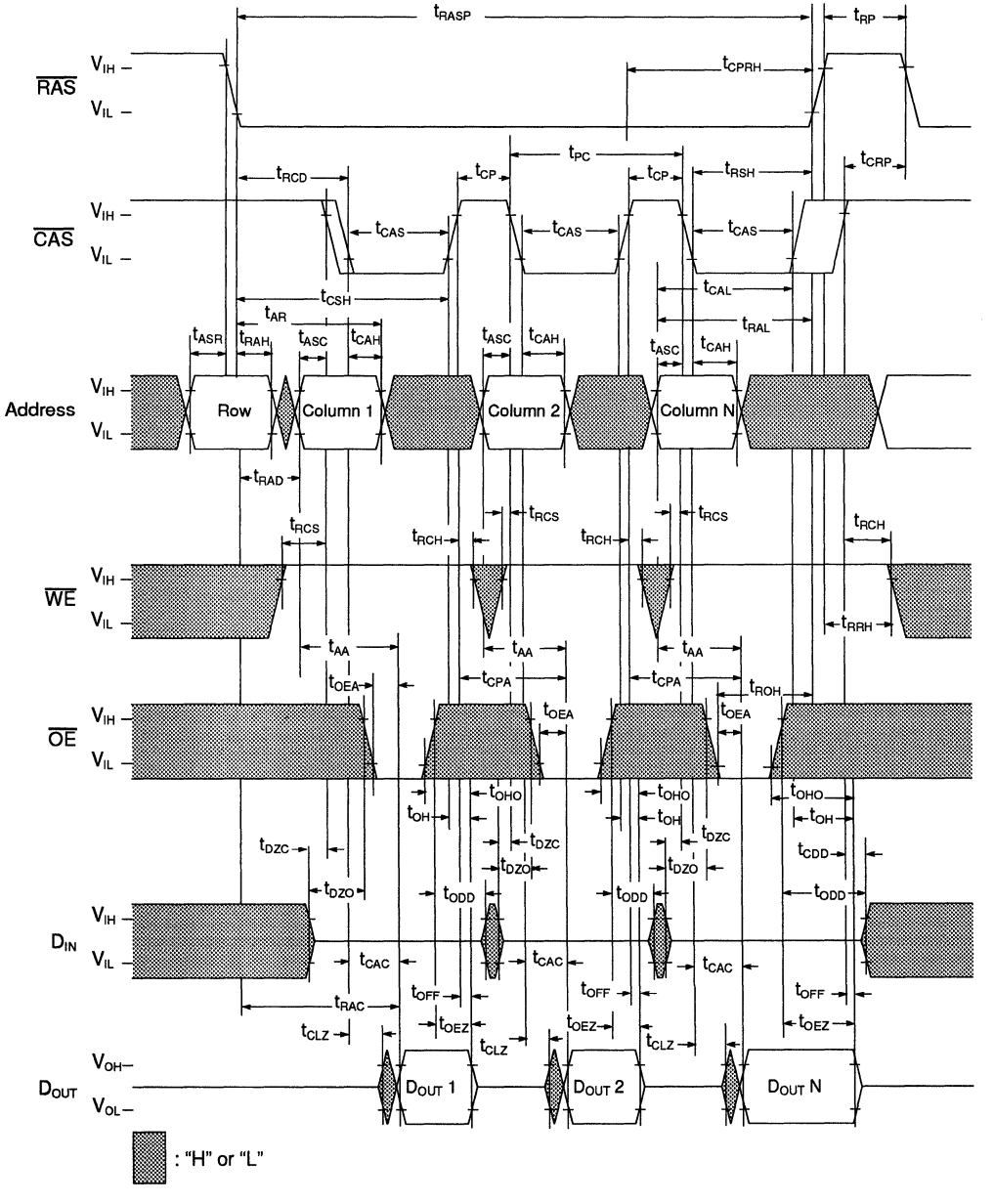


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{wp} min.

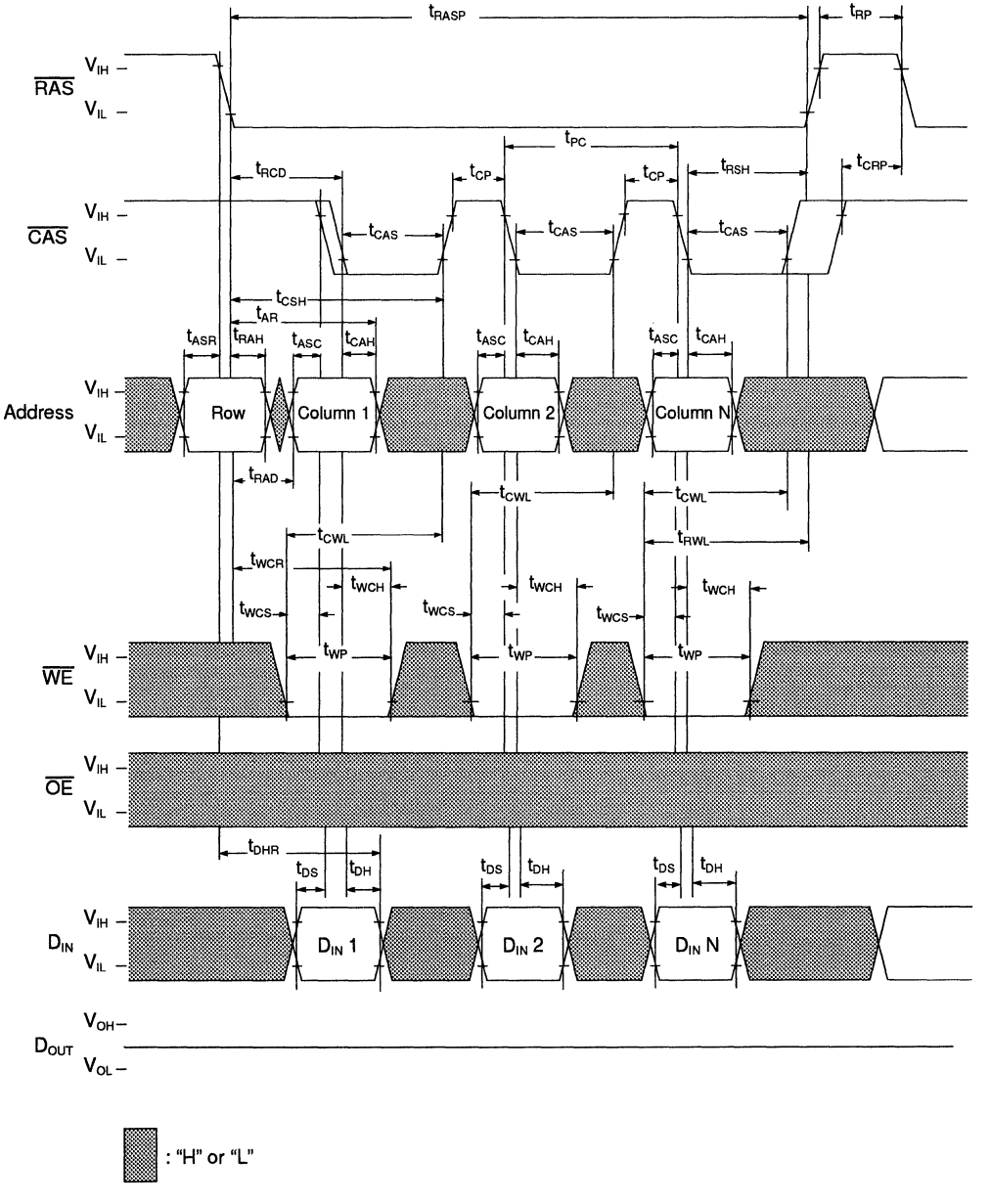
Read-Modify-Write-Cycle



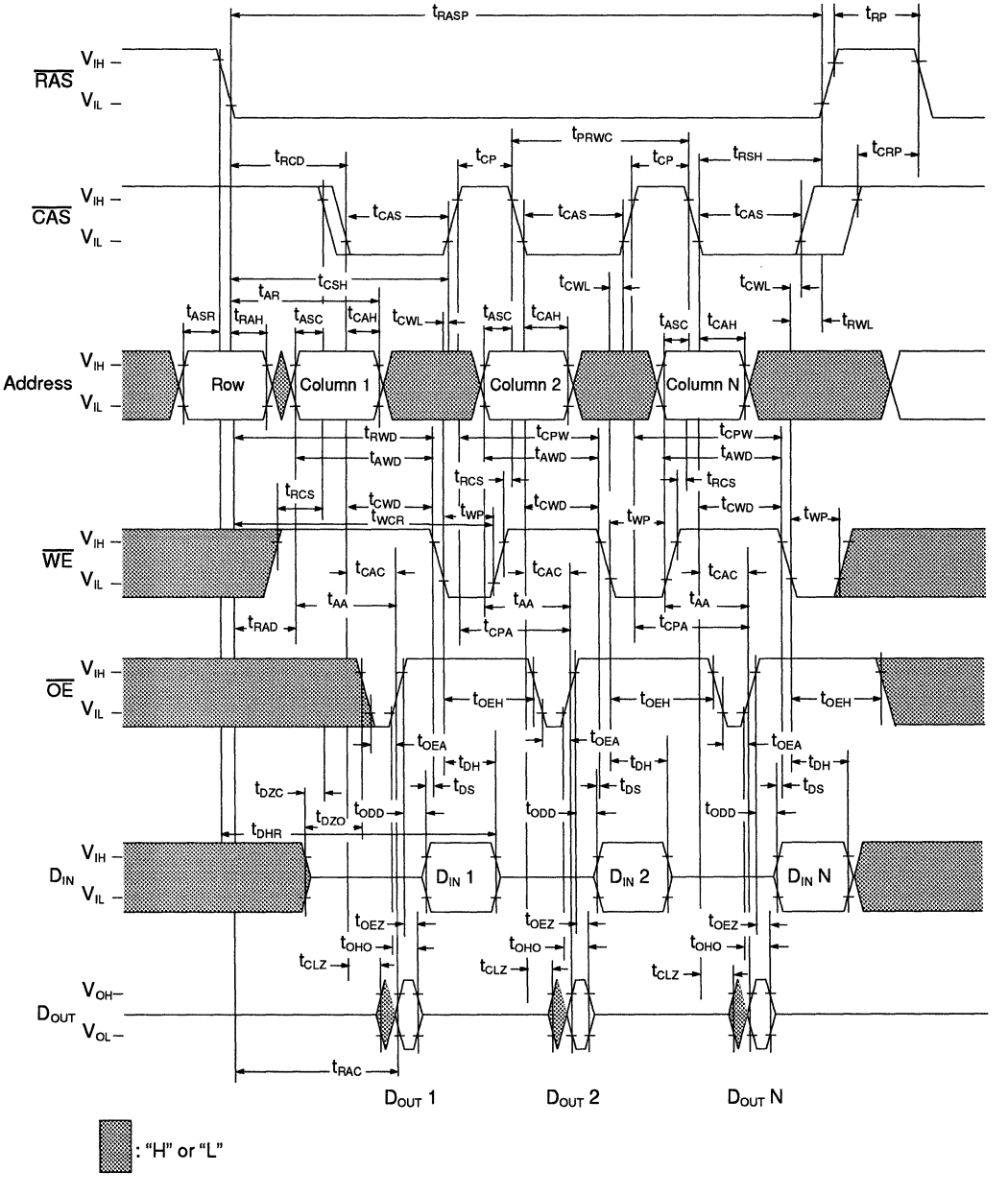
Fast Page Mode Read Cycle



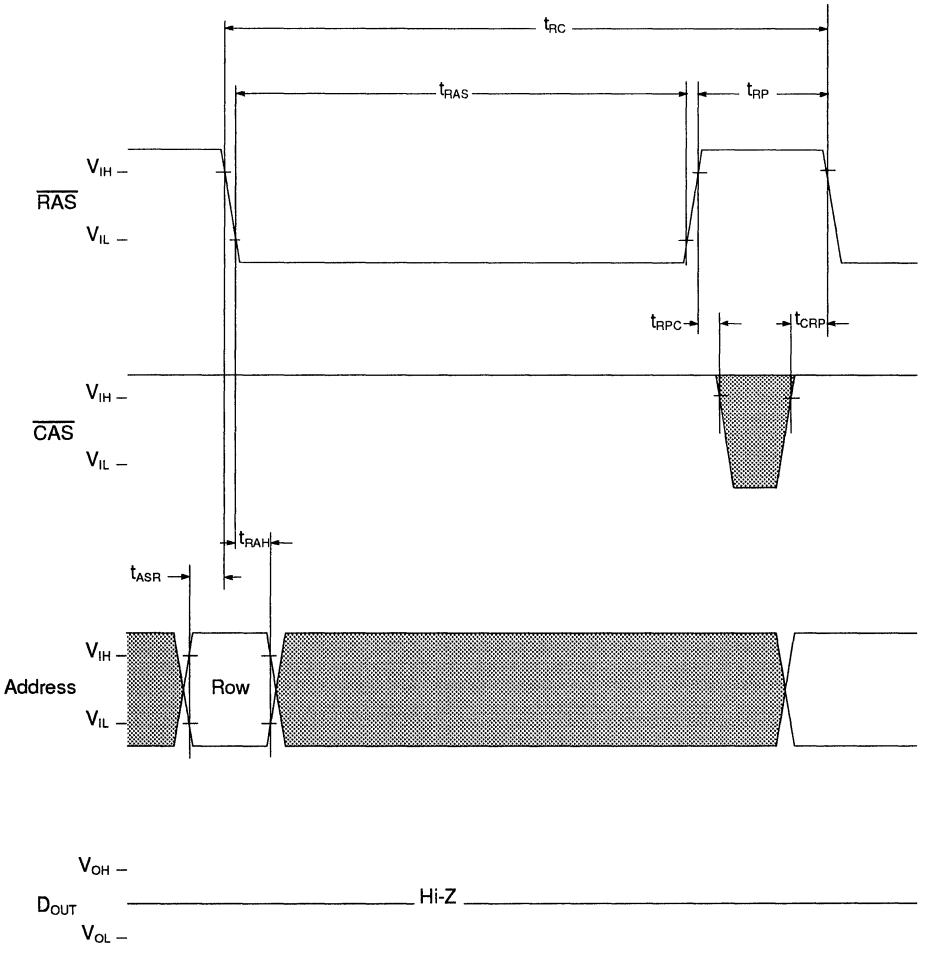
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

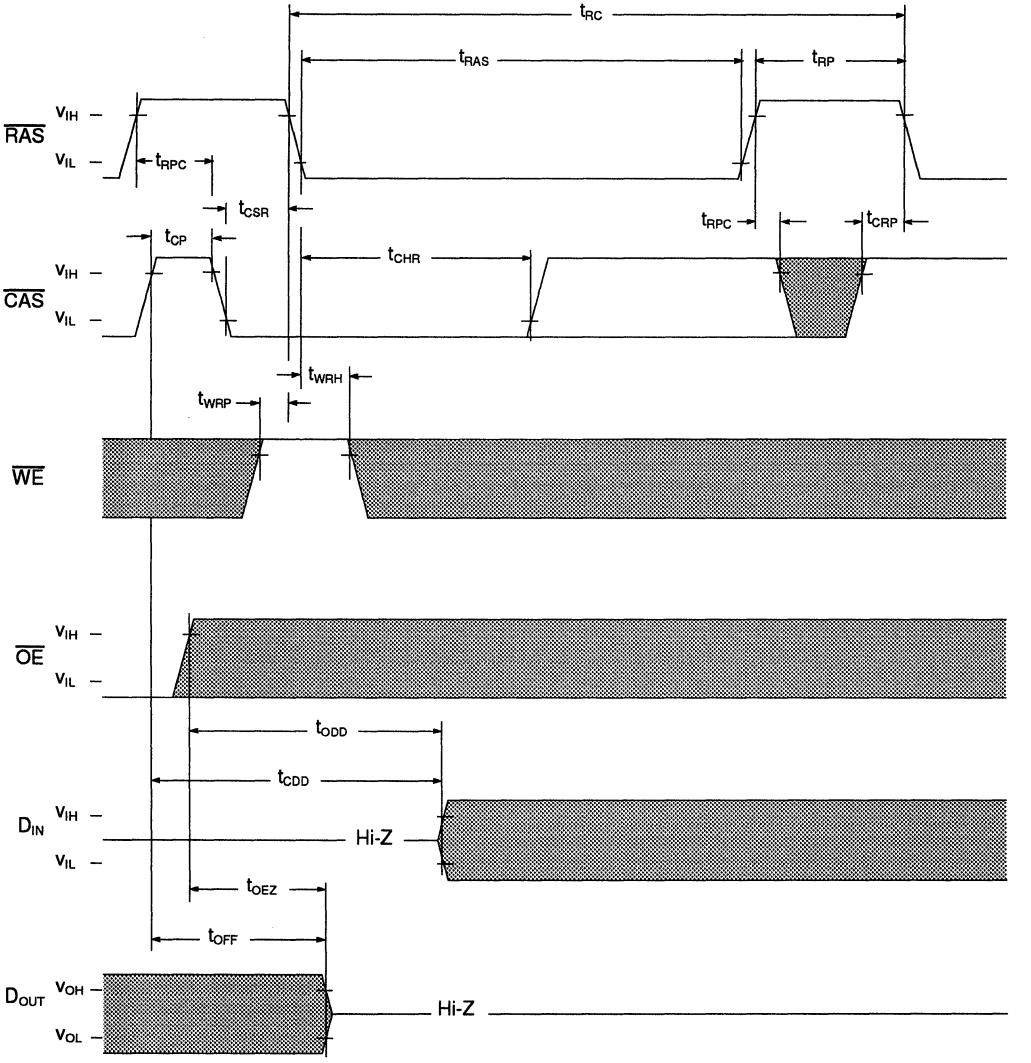


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

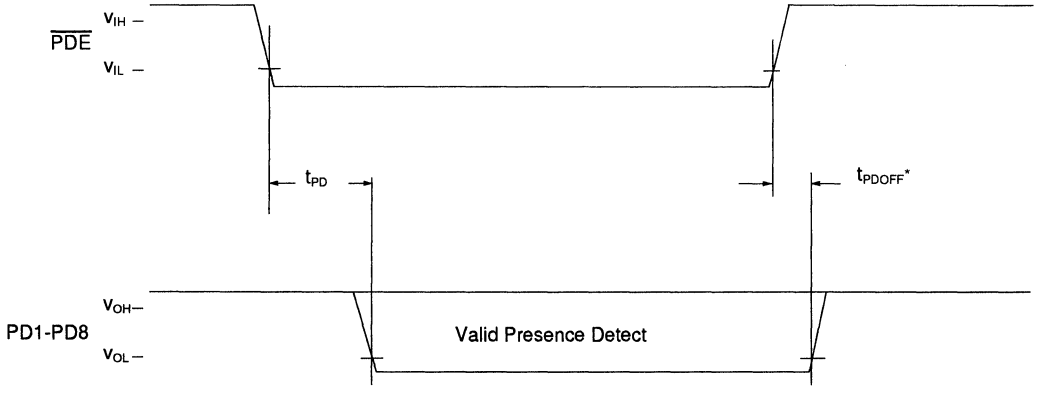
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



: "H" or "L"

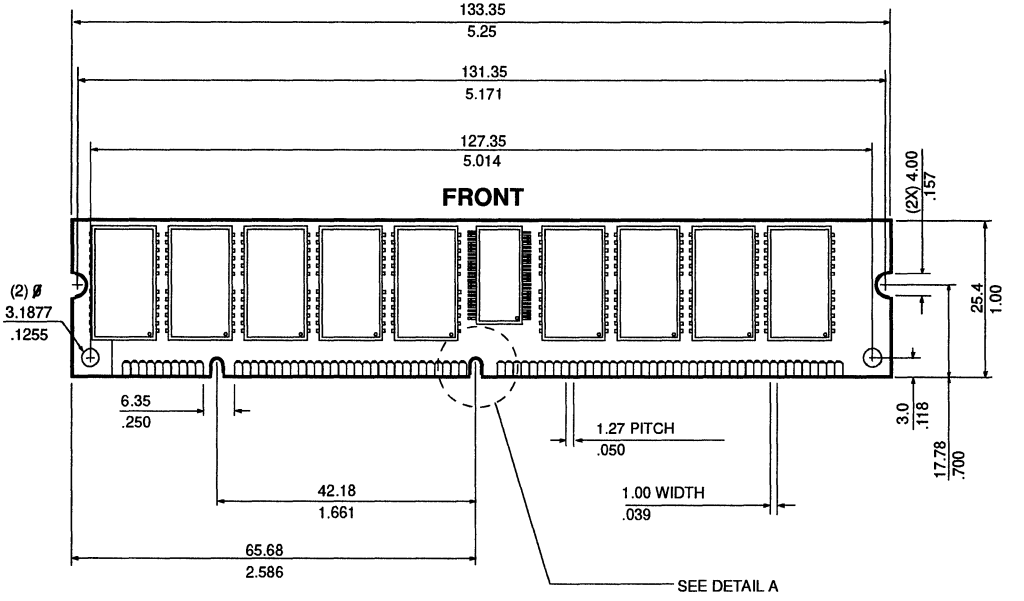
Note: Addresses are "H" or "L"

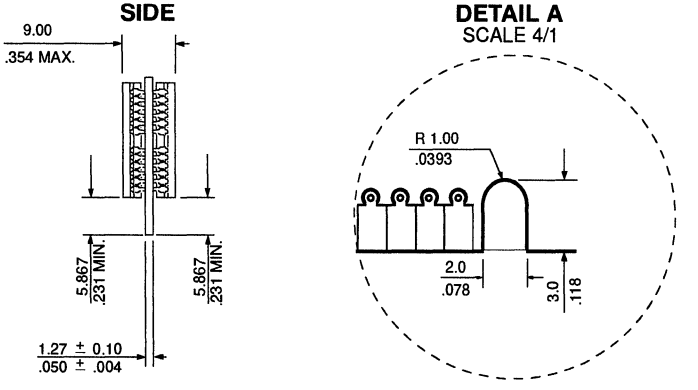
Presence Detect Read Cycle



*PD pins must be pulled high at next level of assembly

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 4Mx72 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are LVTTL and LVCMOS compatible
- Single 3.3V, ± 0.3V Power Supply
- Au contacts
- Optimized for ECC applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - 4 Byte Interleave enabled
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 4096 refresh cycles distributed across 64ms
- 12/10 addressing (Row/Column)
- Card size: 5.25" x 1.0" x 0.354"
- DRAMS in SOJ Package

Description

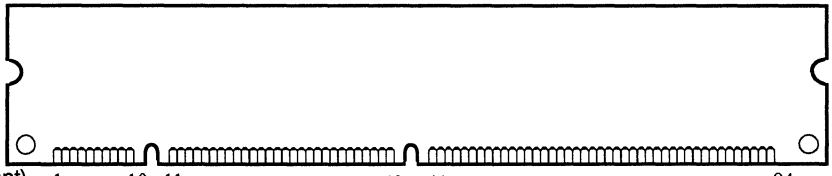
IBM11M4730CB is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 4Mx72 high speed memory array for ECC applications. The DIMM uses 18 4Mx4 DRAMs in SOJ packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, the system will determine that ECC DIMMs are installed if PD8 is low (0). ID0 need not be sensed since both x72 and x80 ECC DIMMs will function in a x72 bank.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 and x72 parity (5V) DIMMs and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A11	Address Inputs (Buffered)
DQx	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

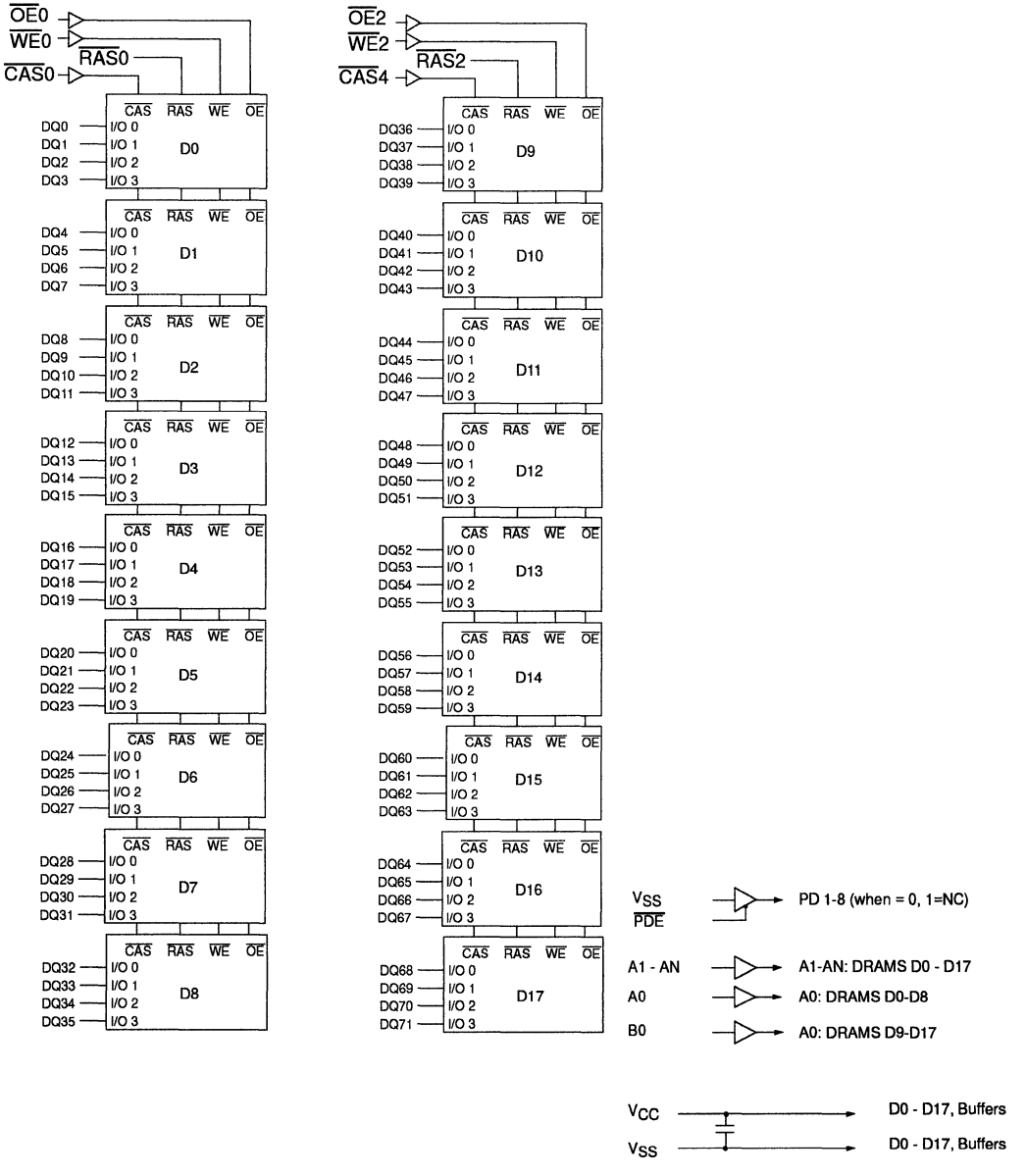
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	NC
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	NC
5	DQ3	89	DQ39	47	NC	131	NC
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	DQ8	95	DQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	DQ17	106	DQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	DQ26	150	DQ62
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	NC	70	DQ29	154	DQ65
29	NC	113	NC	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	NC	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	DQ35	161	DQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	A10	122	A11	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M4730CBA-60	4Mx72	60ns	Au	5.25"x1.0"x 0.354"	
IBM11M4730CBA-70	4Mx72	70ns	Au	5.25"x1.0"x 0.354"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	1	1
PD2	1	1
PD3	0	0
PD4	1	1
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	0	0
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 4.6	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	5.5	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A11)	13	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	70	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF	
C_{I4}	DQ_X Capacitance	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1530	mA	1,2,3
		-70	—	1350		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	36	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1530	mA	1,3
		-70	—	1350		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1350	mA	1,2,3
		-70	—	1170		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	18	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1530	mA	1,3
		-70	—	1350		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	

1. I_{CC1},I_{CC3},I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1},I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required..
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the Dram device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	1
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	4
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	5
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
2. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.
5. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	2	—	ns	1
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	3
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	36	—	41	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	36	—	41	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	—	—	—	—	ns	4
t_{OH}	Output Data Hold Time	2	—	2	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1, 2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	63	—	73	—	ns	1

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	64	—	64	ms	1

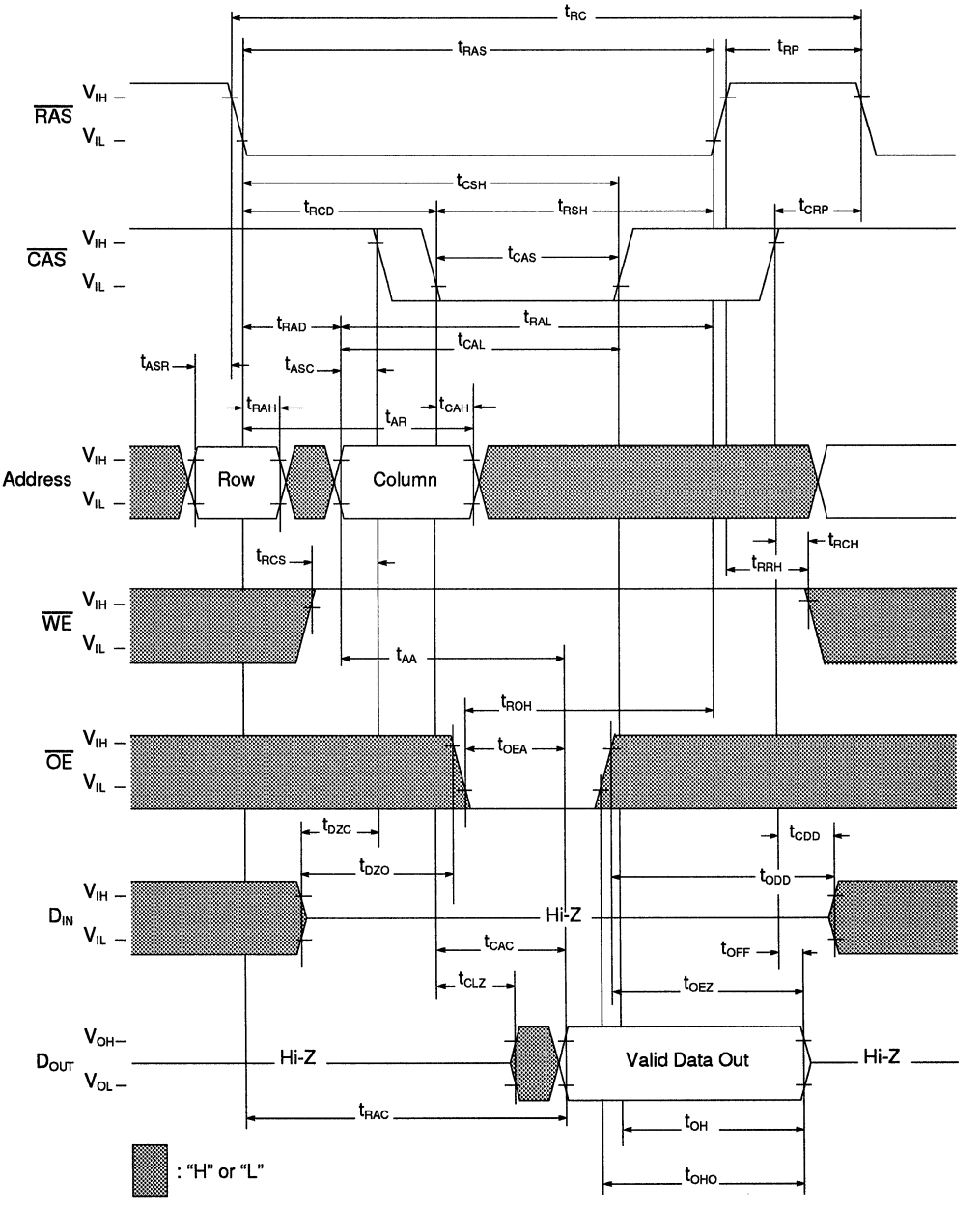
1. 4096 refreshes are required every 64ms.

Presence Detect Read Cycle

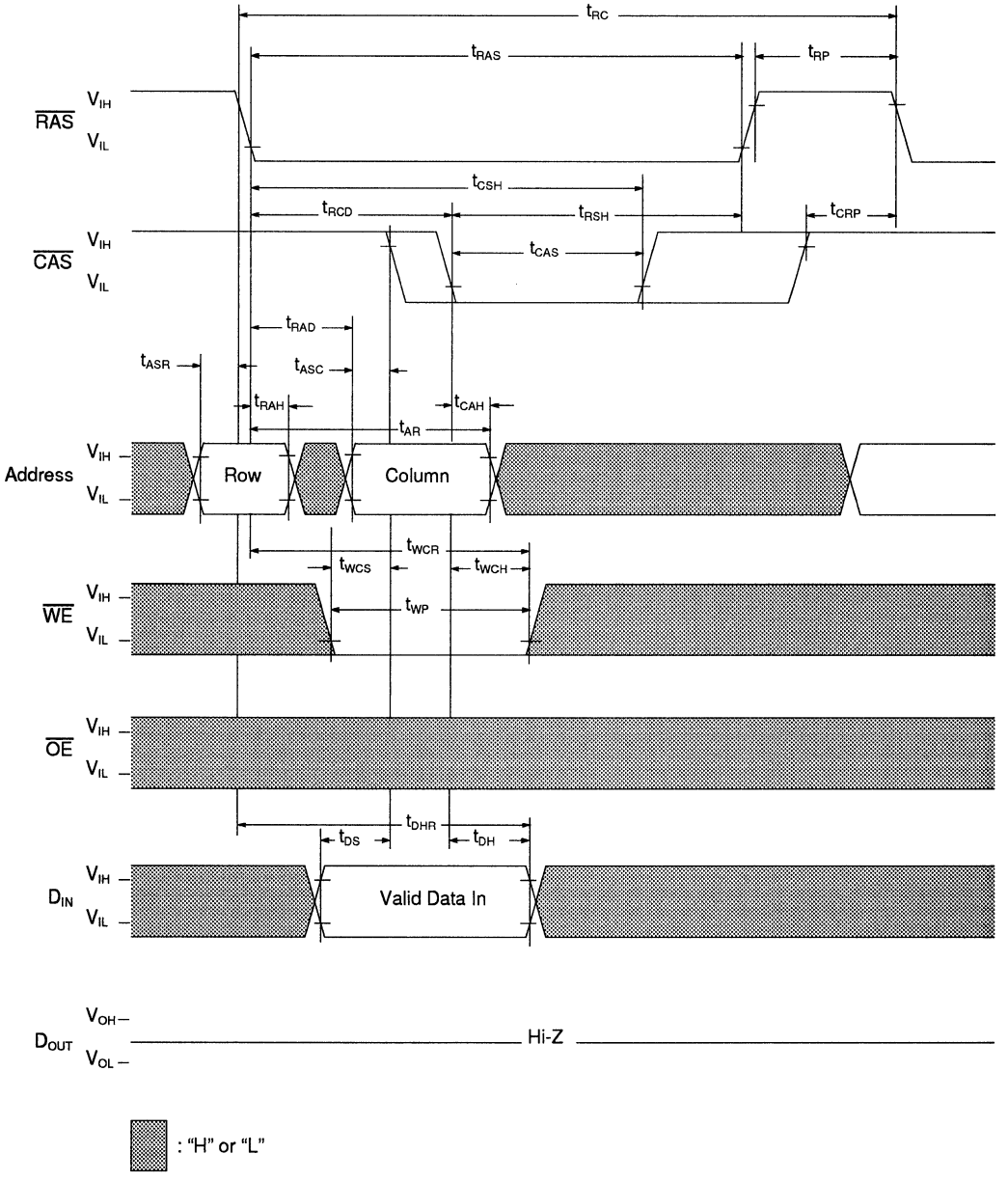
Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

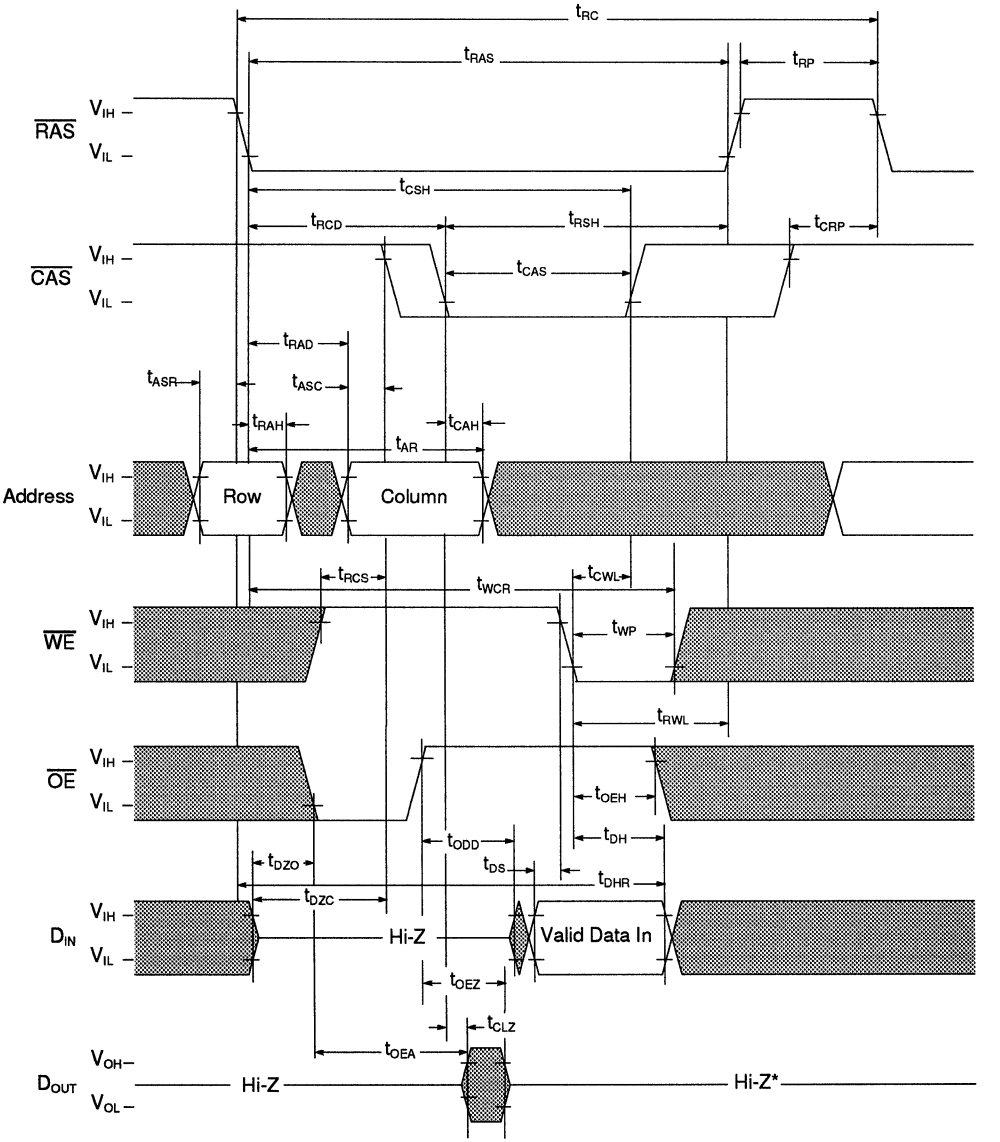
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tAR
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tCDD
tDZO
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

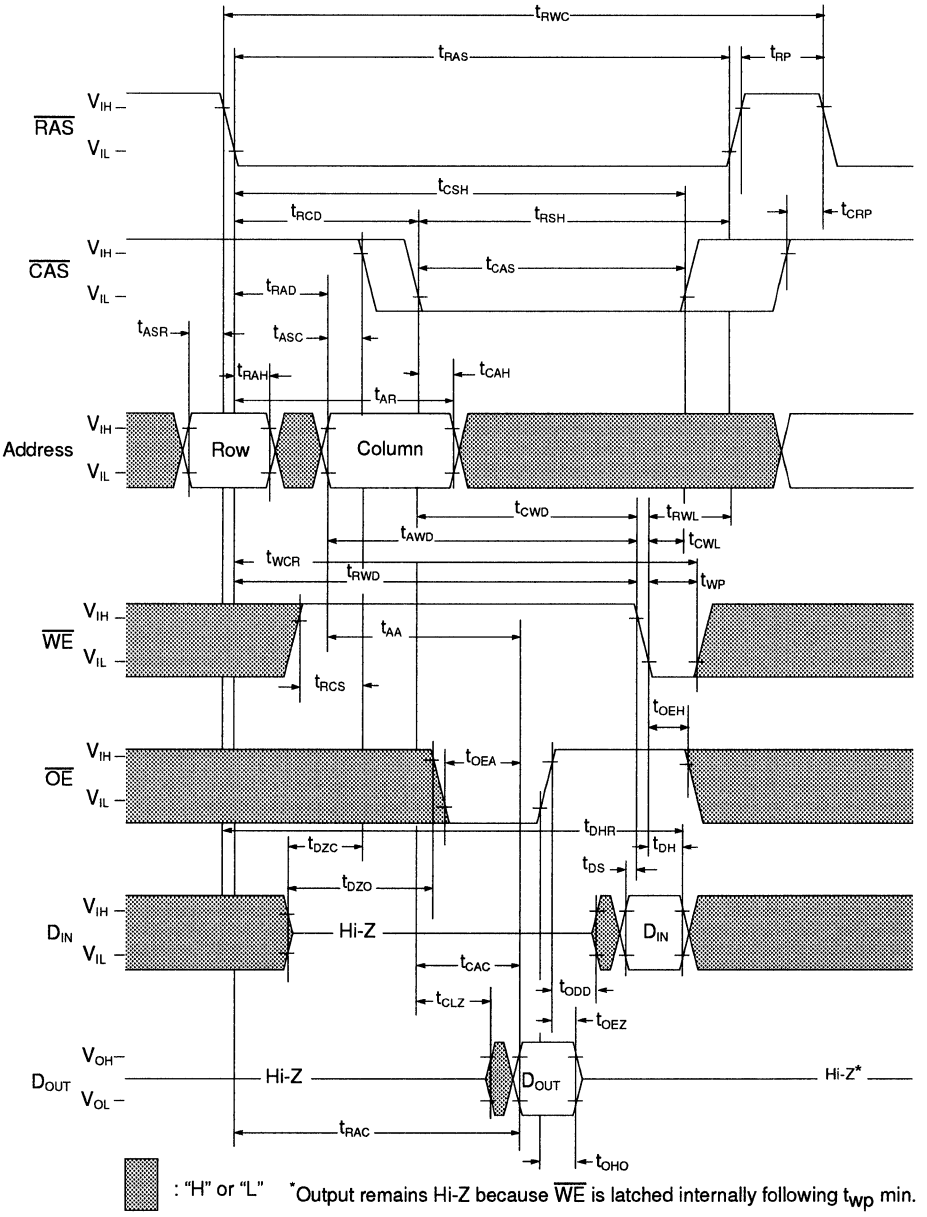


Write Cycle (Late Write)

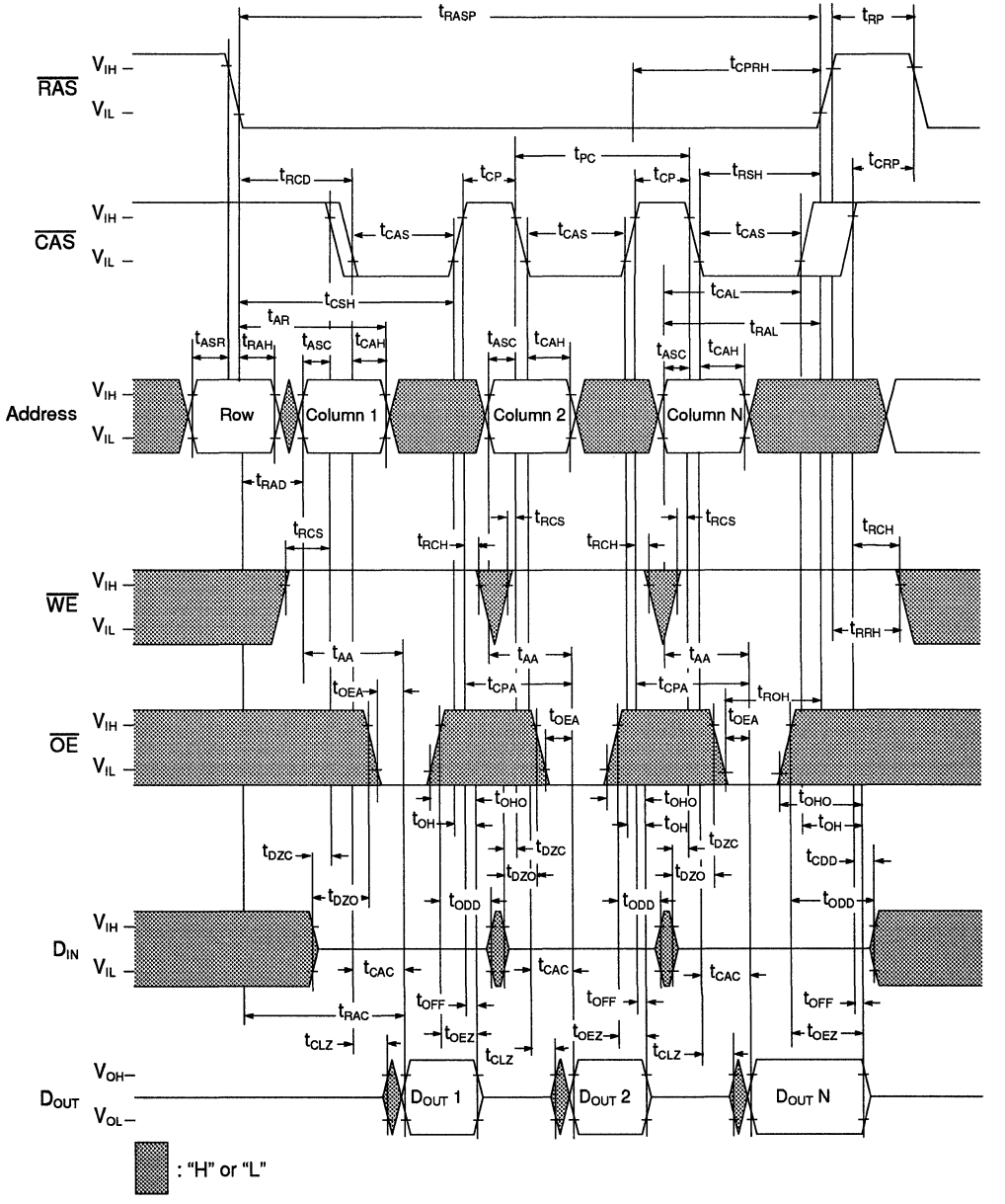


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

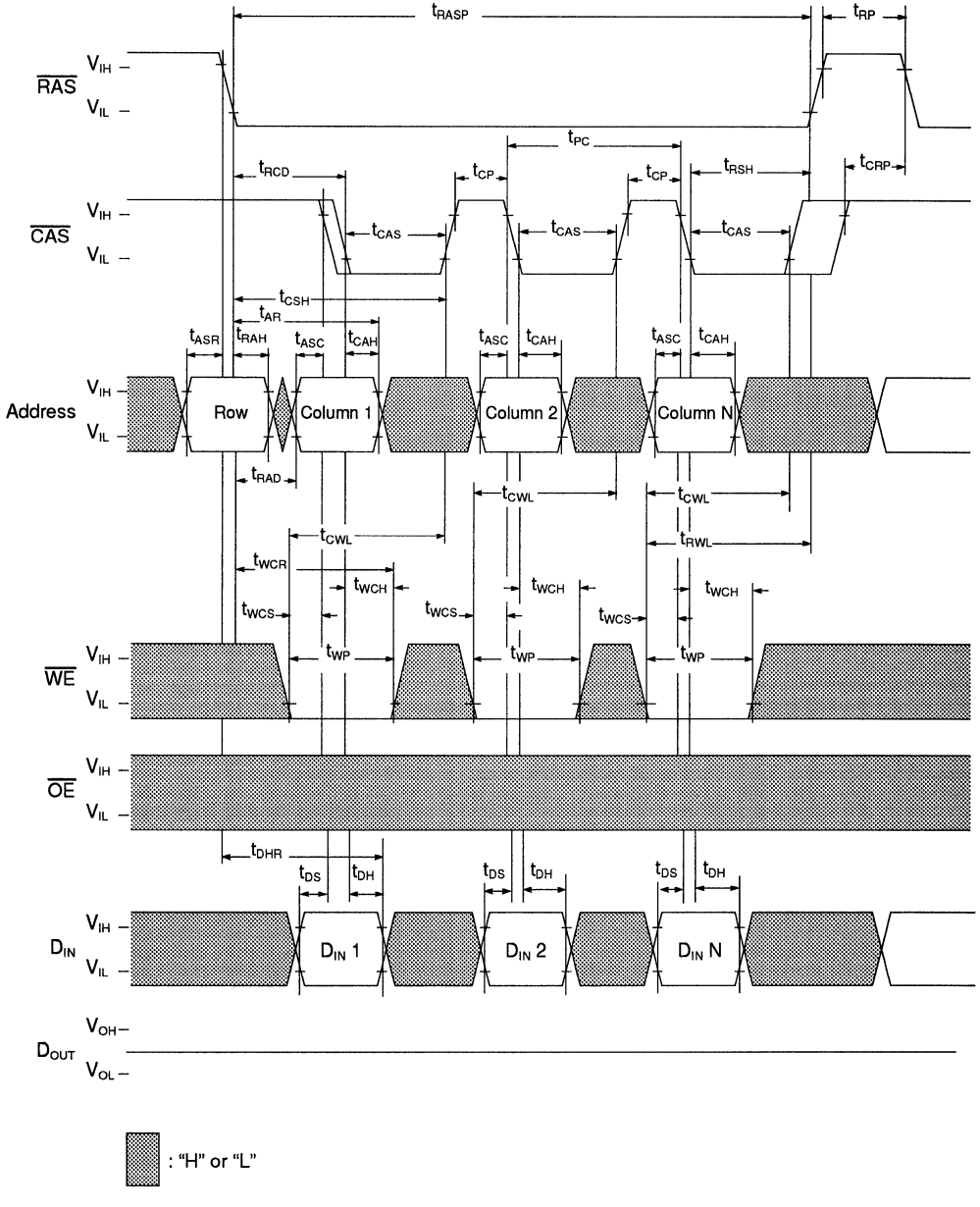
Read-Modify-Write-Cycle



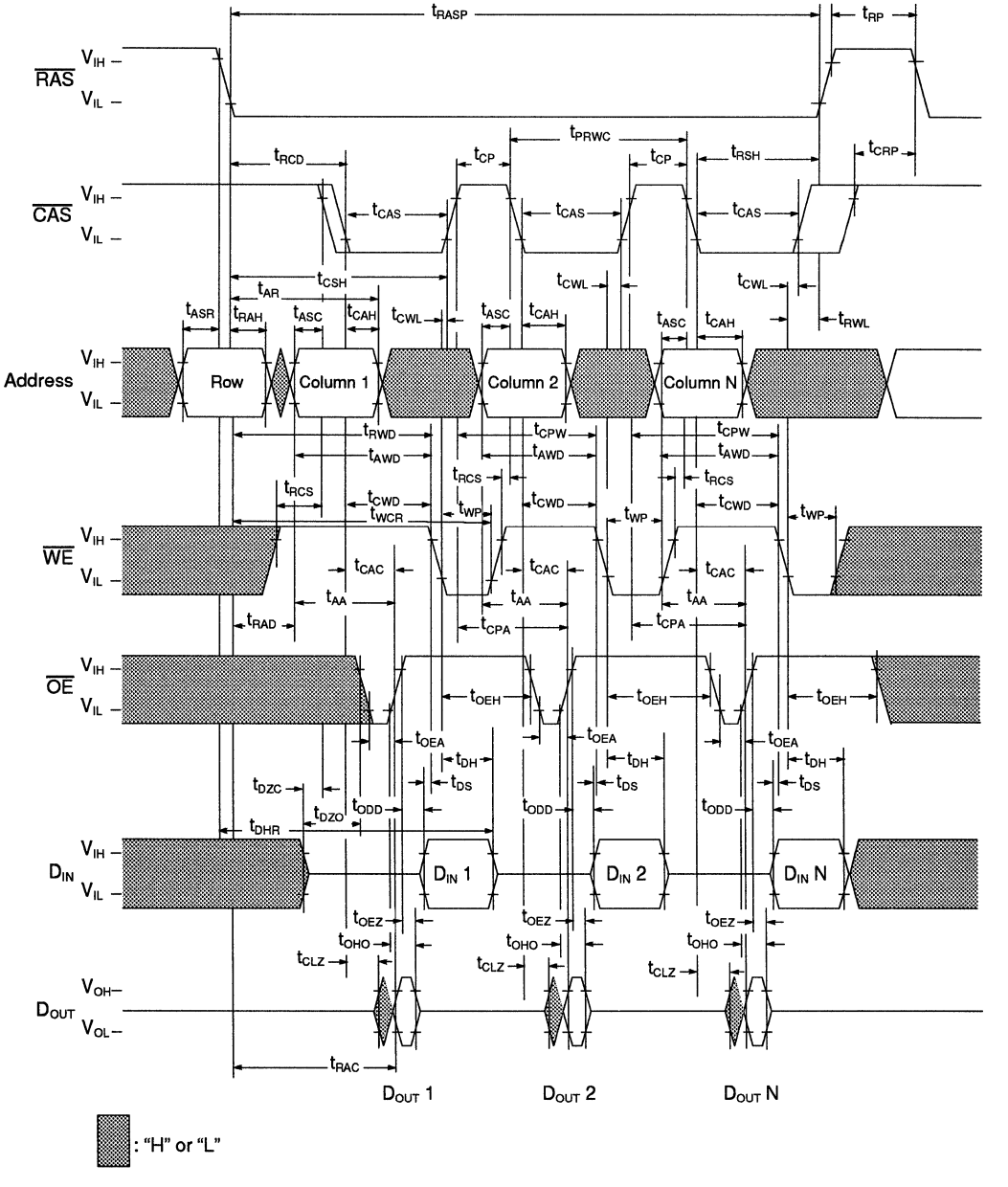
Fast Page Mode Read Cycle



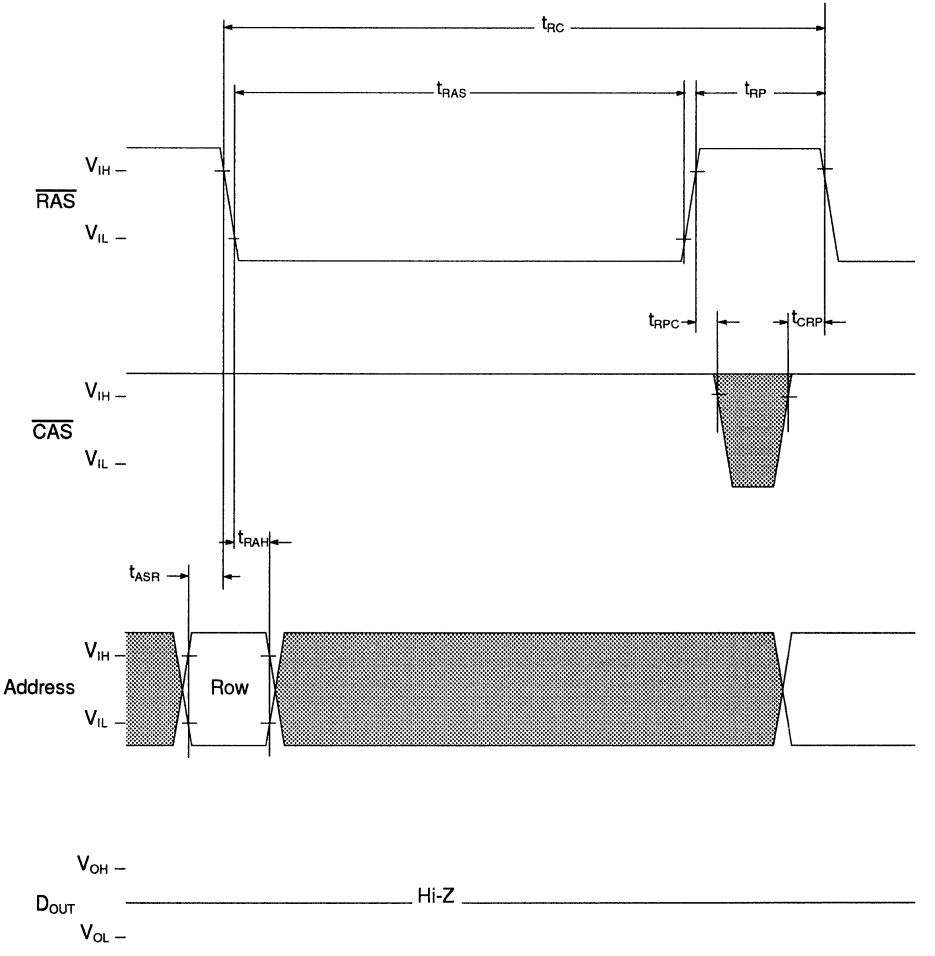
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

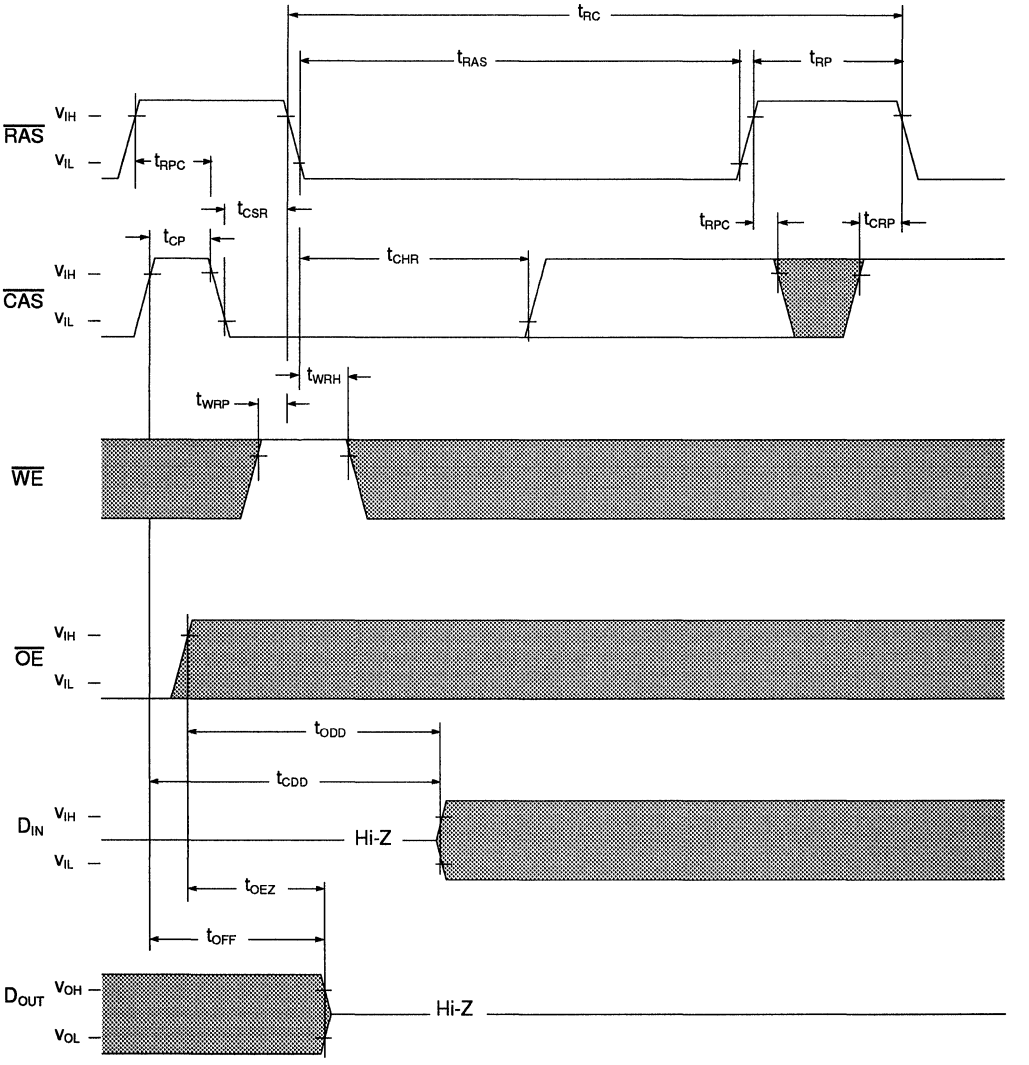


$\overline{\text{RAS}}$ Only Refresh Cycle



Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$, D_{IN} are "H" or "L"

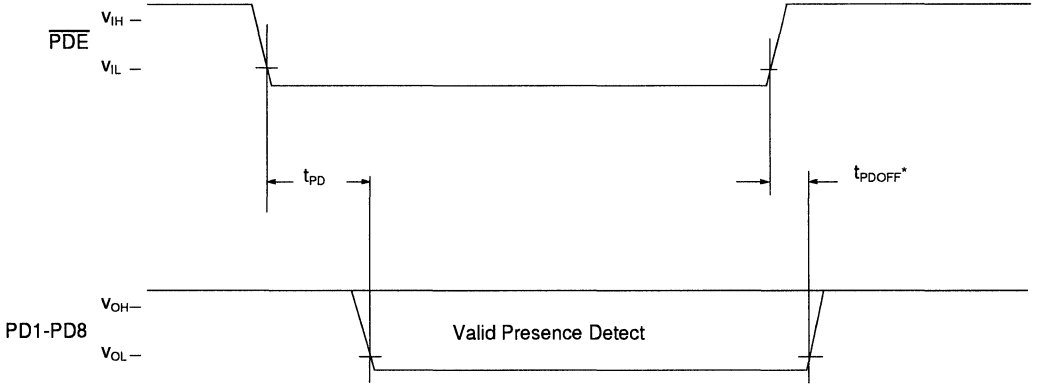
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



: "H" or "L"

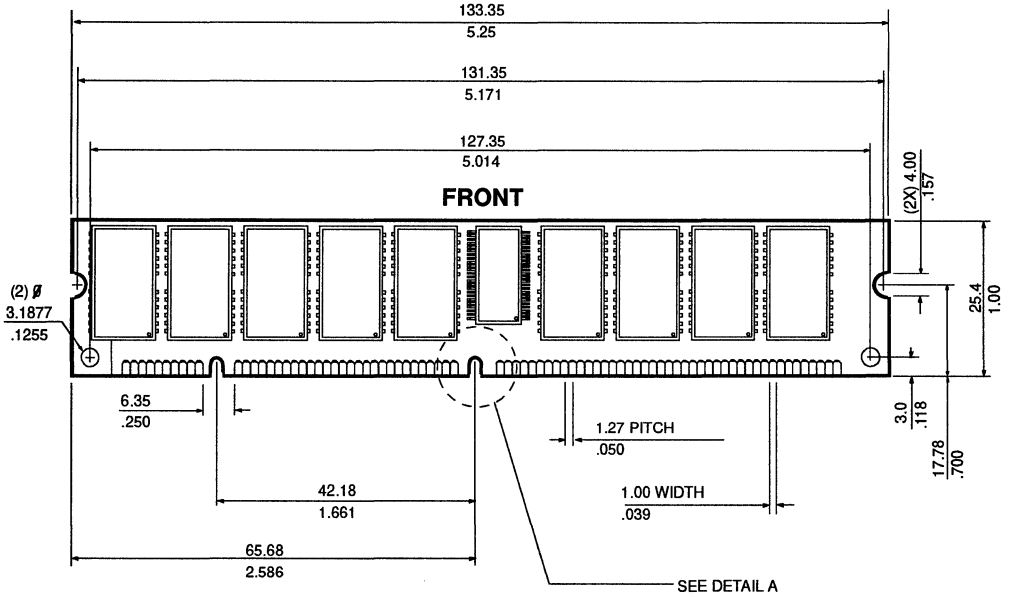
Note: Addresses are "H" or "L"

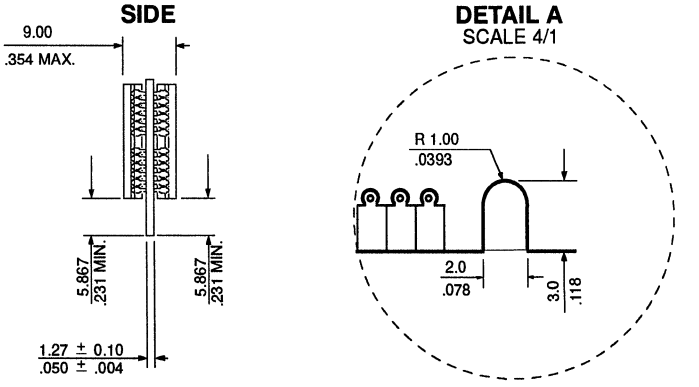
Presence Detect Read Cycle



*PD pins must be pulled high at next level of assembly

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 8Mx72 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are TTL and CMOS compatible
- Single 5.0V, ± 0.5V Power Supply
- Au contacts
- Optimized for ECC applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - 4 Byte Interleave enabled
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 4096 refresh cycles distributed across 64ms
- 12/10 addressing (Row/Column)
- Card size: 5.25" x 1.5" x 0.320"
- DRAMS in Stacked TSOP Package

Description

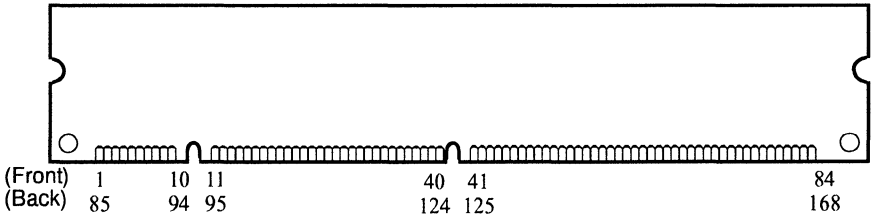
IBM11M8730P is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as an 8Mx72 high speed memory array, and is configured as 2 4Mx72 banks. The DIMM uses 36 4Mx4 DRAMs assembled as 18 stacked TSOP packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, the system will determine that ECC DIMMs are installed if PD8 is low (0). ID0 need not be sensed since both x72 and x80 ECC DIMMs will function in a x72 bank.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 and x72 parity (5V) DIMMs and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A11	Address Inputs (Buffered)
DQx	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

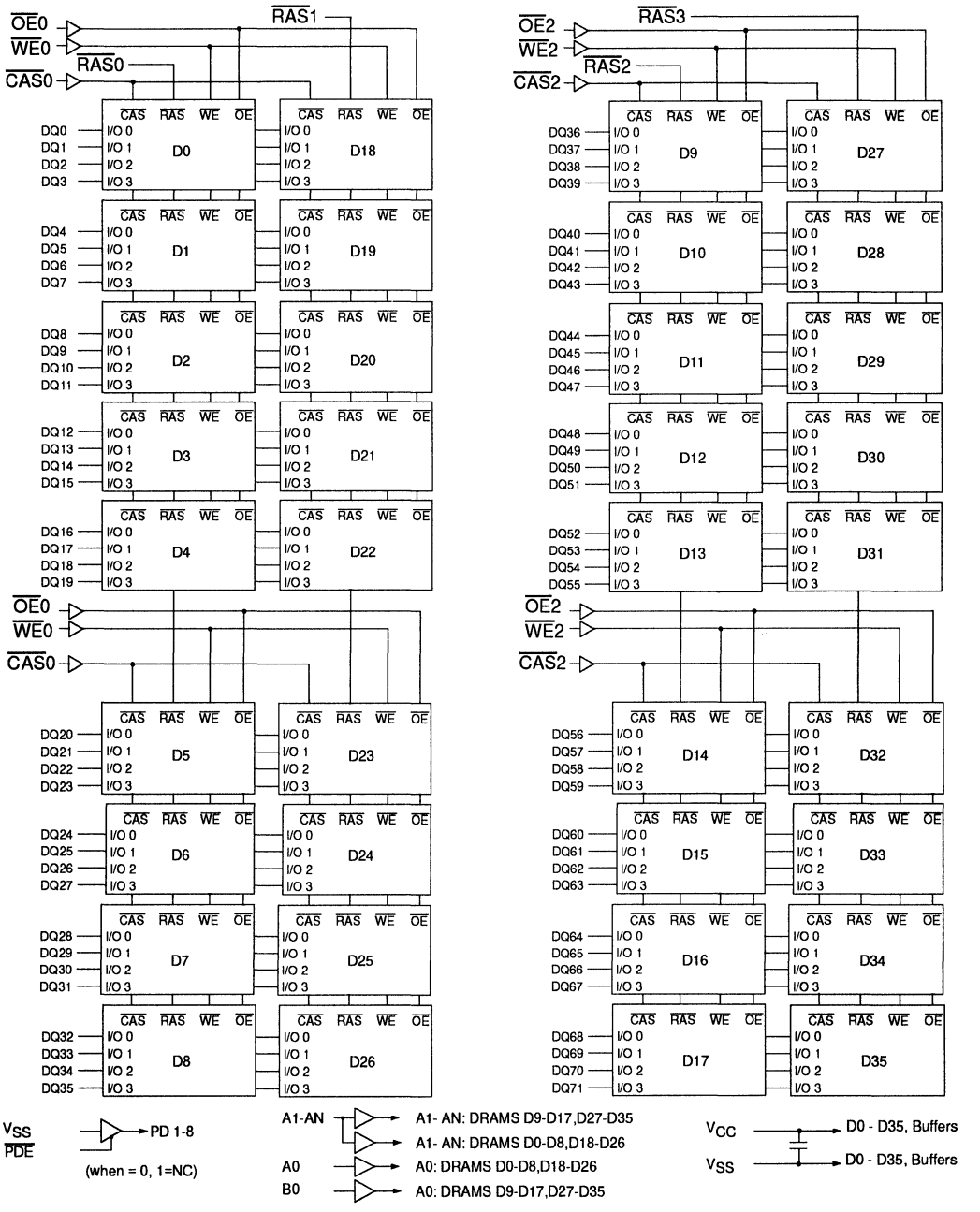
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	$\overline{RAS3}$
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	NC
5	DQ3	89	DQ39	47	NC	131	NC
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	DQ8	95	DQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	DQ17	106	DQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	DQ26	150	DQ62
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	NC	70	DQ29	154	DQ65
29	NC	113	NC	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	$\overline{RAS1}$	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	DQ35	161	DQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	A10	122	A11	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M8730PA-60	8Mx72	60ns	Au	5.25"x1.5"x 0.320"	
IBM11M8730PA-70	8Mx72	70ns	Au	5.25"x1.5"x 0.320"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	0	0
PD2	0	0
PD3	1	1
PD4	1	1
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	0	0
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	16.8	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to Vss.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A11)	18	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	80	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	18	pF	
C_{I4}	DQ_X Capacitance	22	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1566	mA	1, 2, 3
		-70	—	1386		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	72	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1566	mA	1, 3, 4
		-70	—	1386		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1386	mA	1, 2, 3
		-70	—	1206		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	36	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1566	mA	1, 3, 4
		-70	—	1386		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-20	+20	µA	
		$\overline{RAS}$	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1},I_{CC3},I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1},I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. Refresh current is specified for 1 bank.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required..
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the Dram device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	1
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	4
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	5
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
2. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.
5. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	2	—	ns	1
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	3
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	36	—	41	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	36	—	41	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	—	—	—	—	ns	4
t_{OH}	Output Data Hold Time	2	—	2	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1, 2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	63	—	73	—	ns	1

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	64	—	64	ms	1

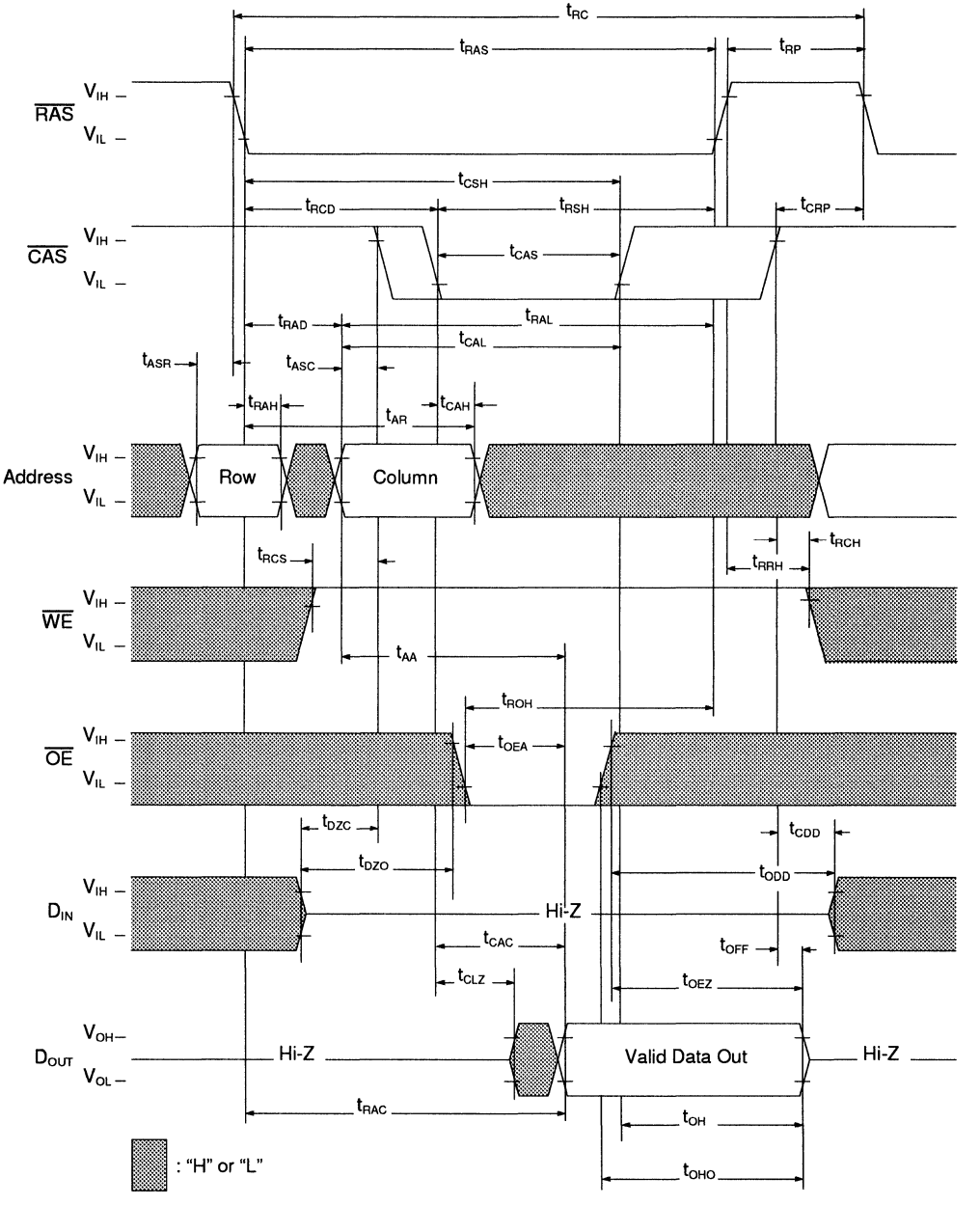
1. 4096 refreshes are required every 64ms.

Presence Detect Read Cycle

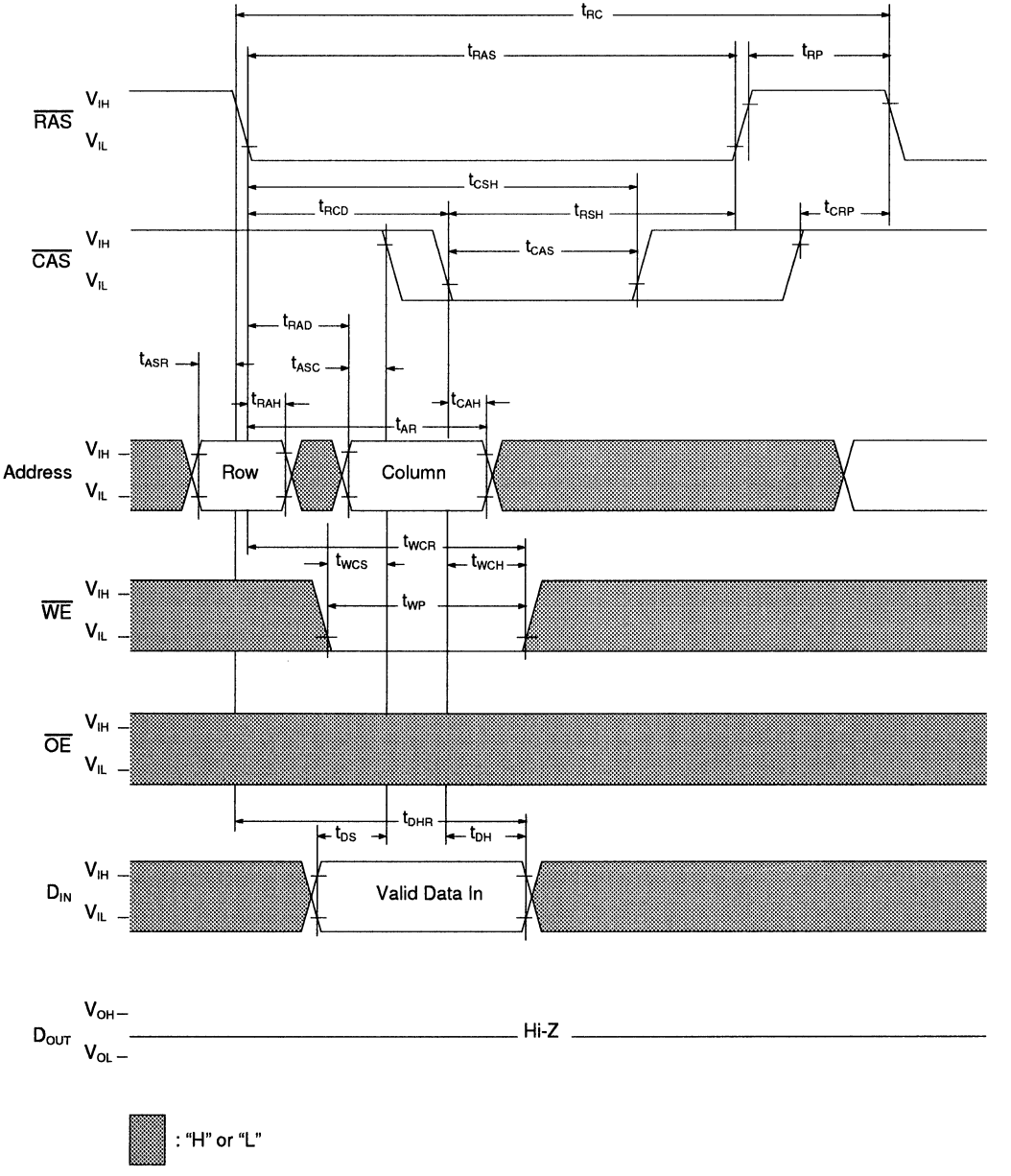
Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

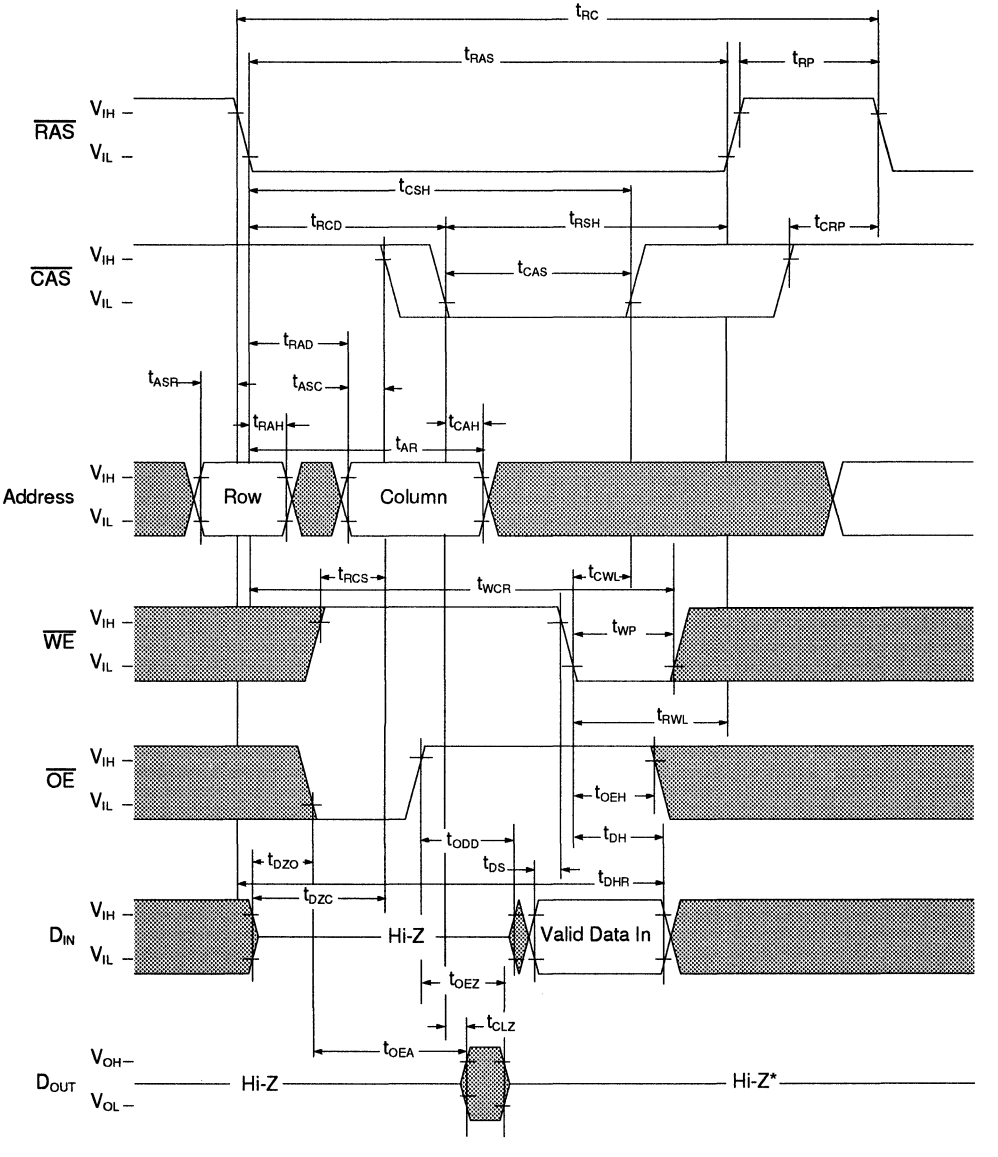
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tCAH
tAR
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tCDD
tDZO
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Valid Data Out
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

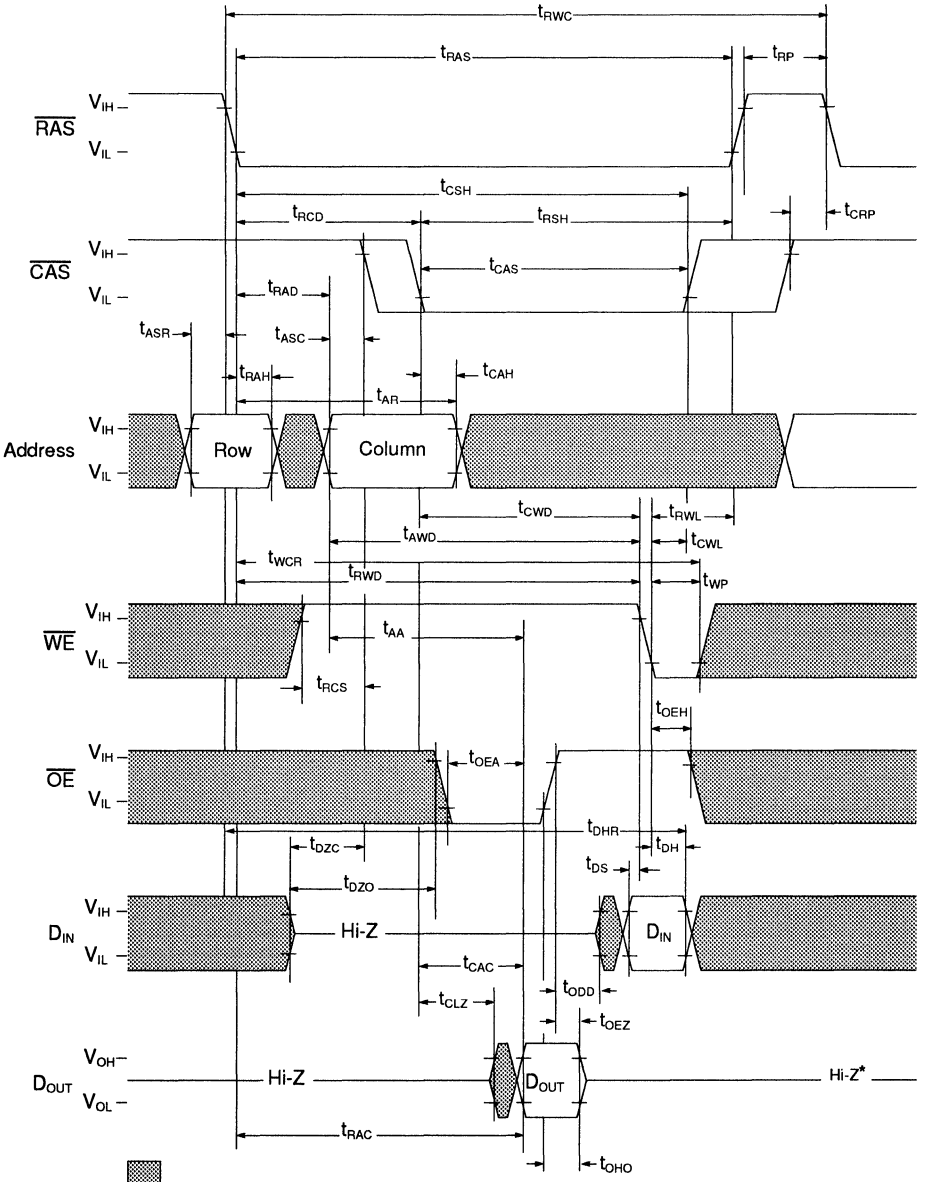


Write Cycle (Late Write)

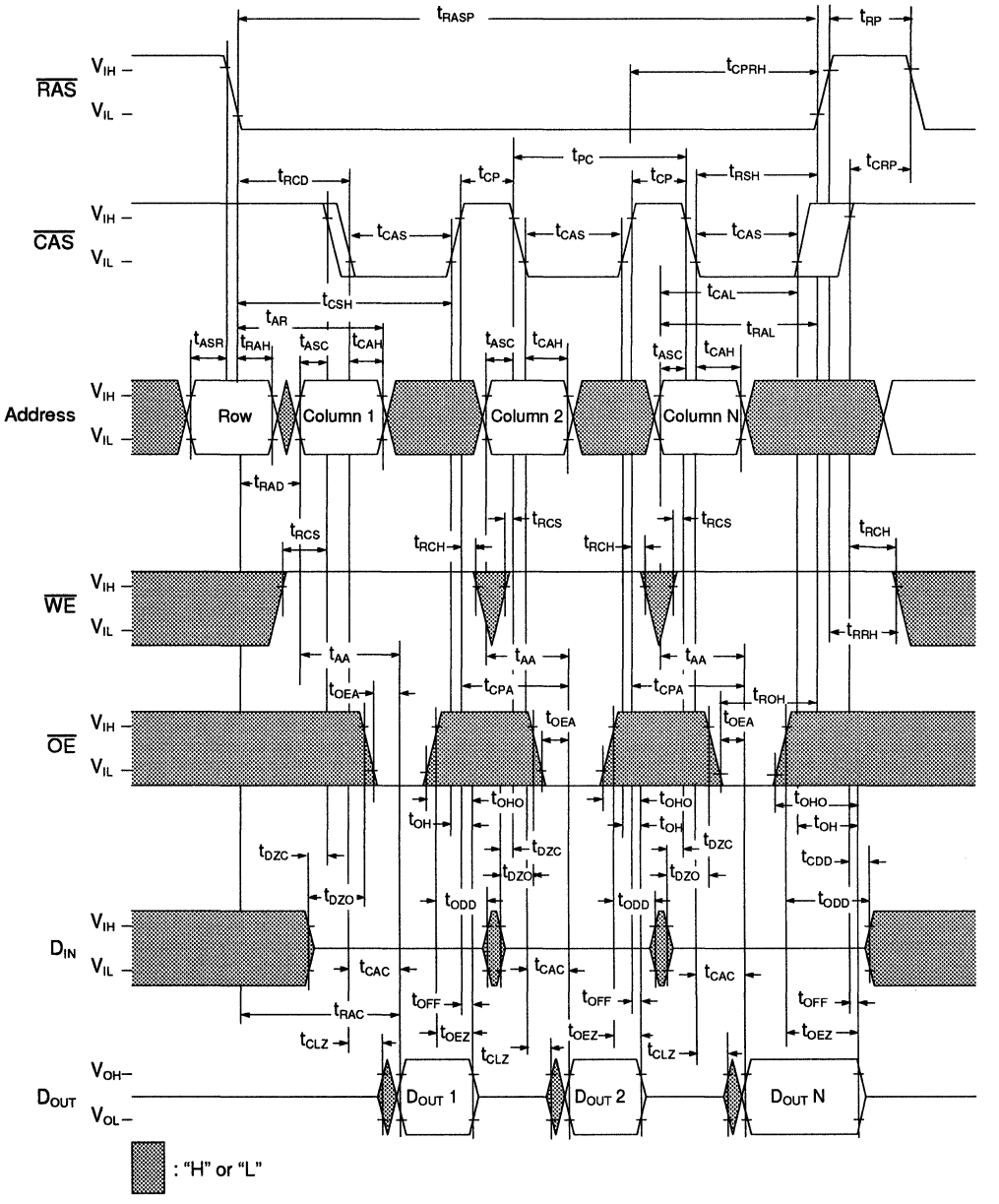


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

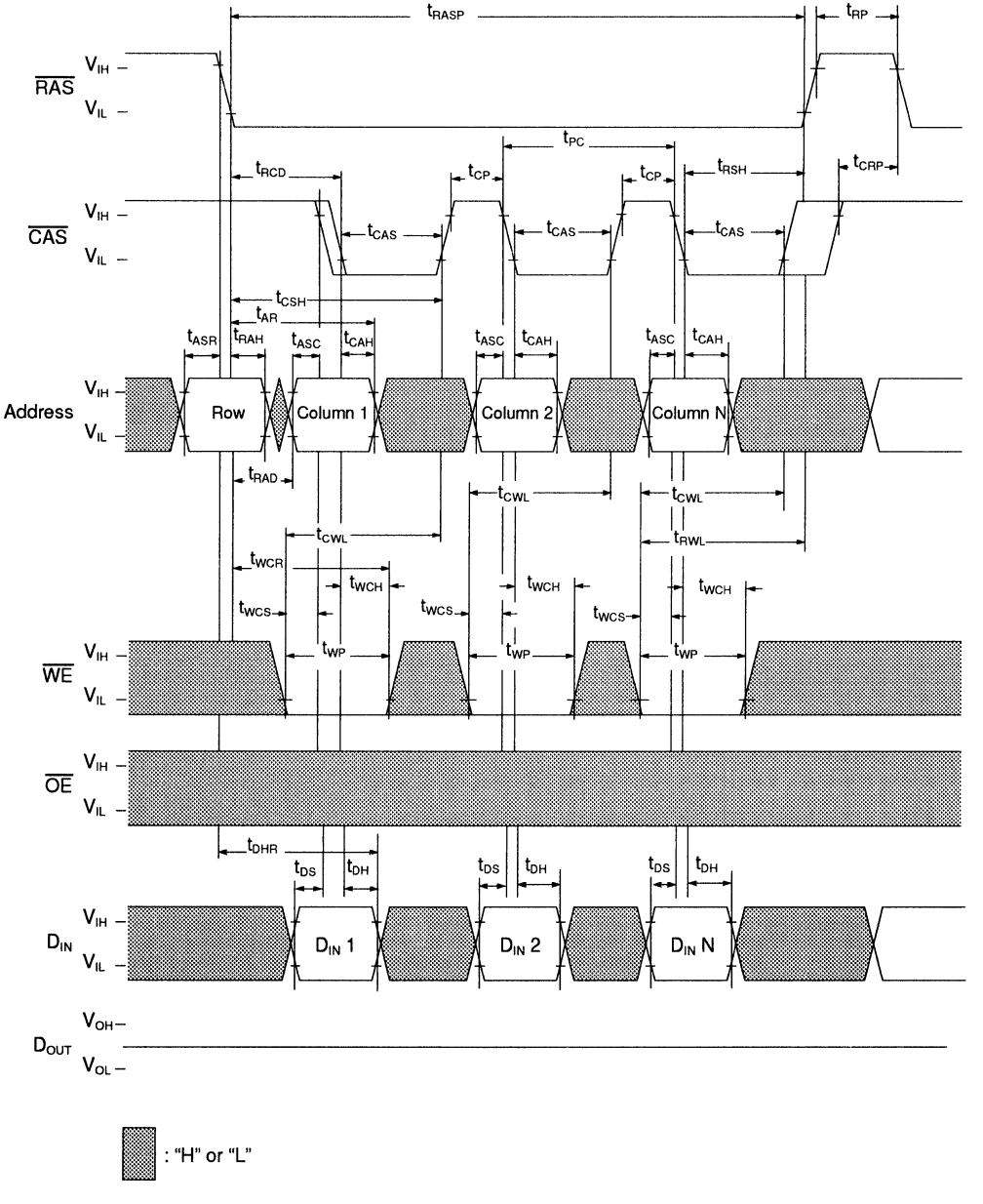
Read-Modify-Write-Cycle



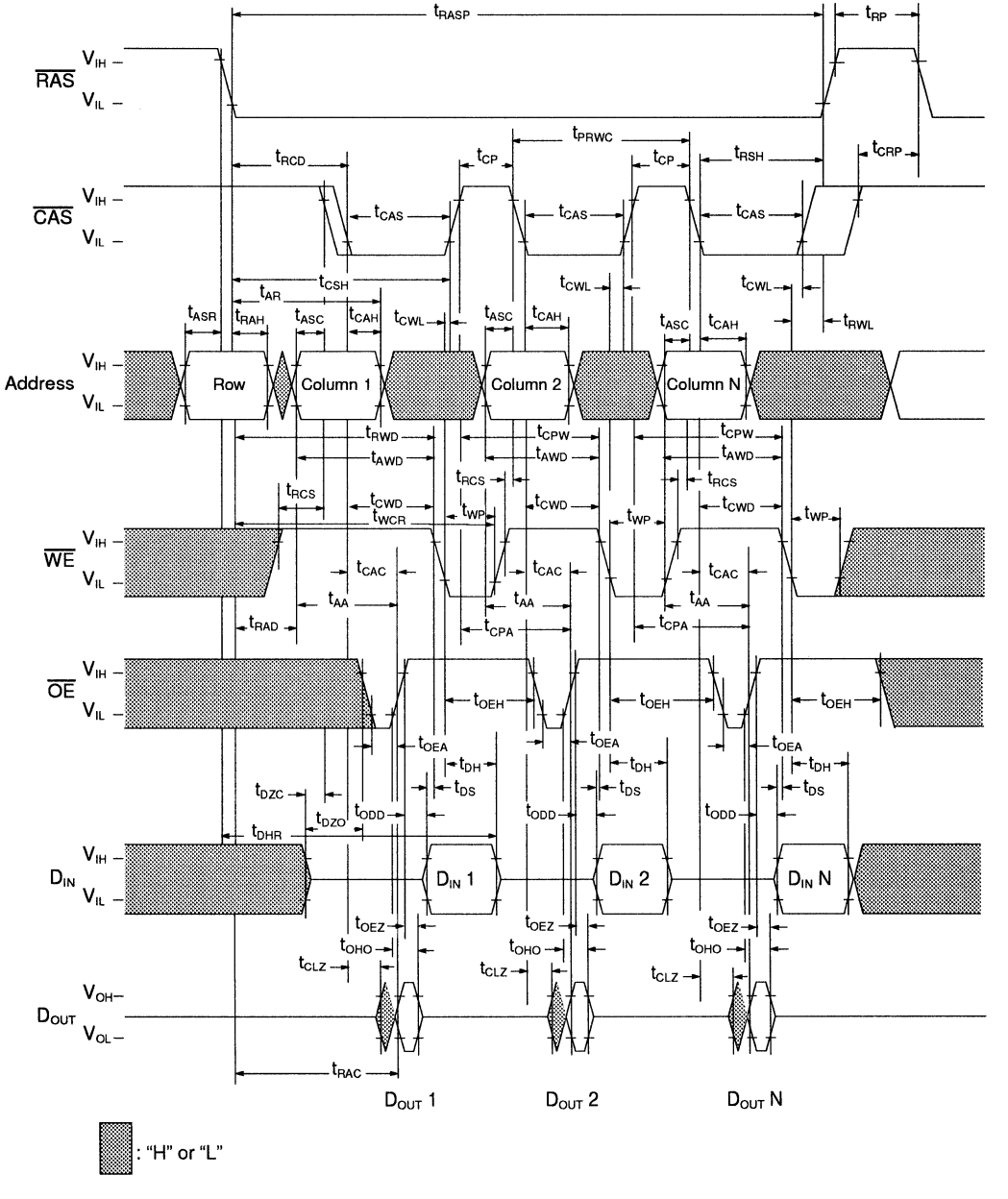
Fast Page Mode Read Cycle



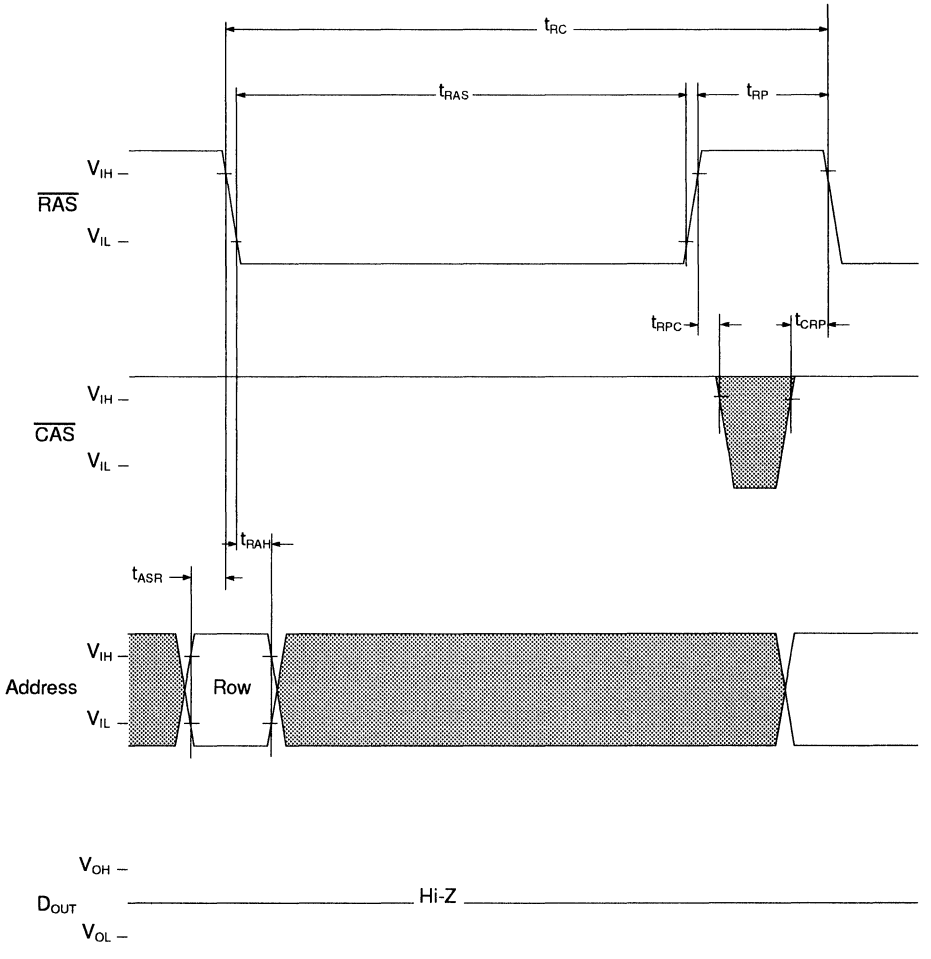
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

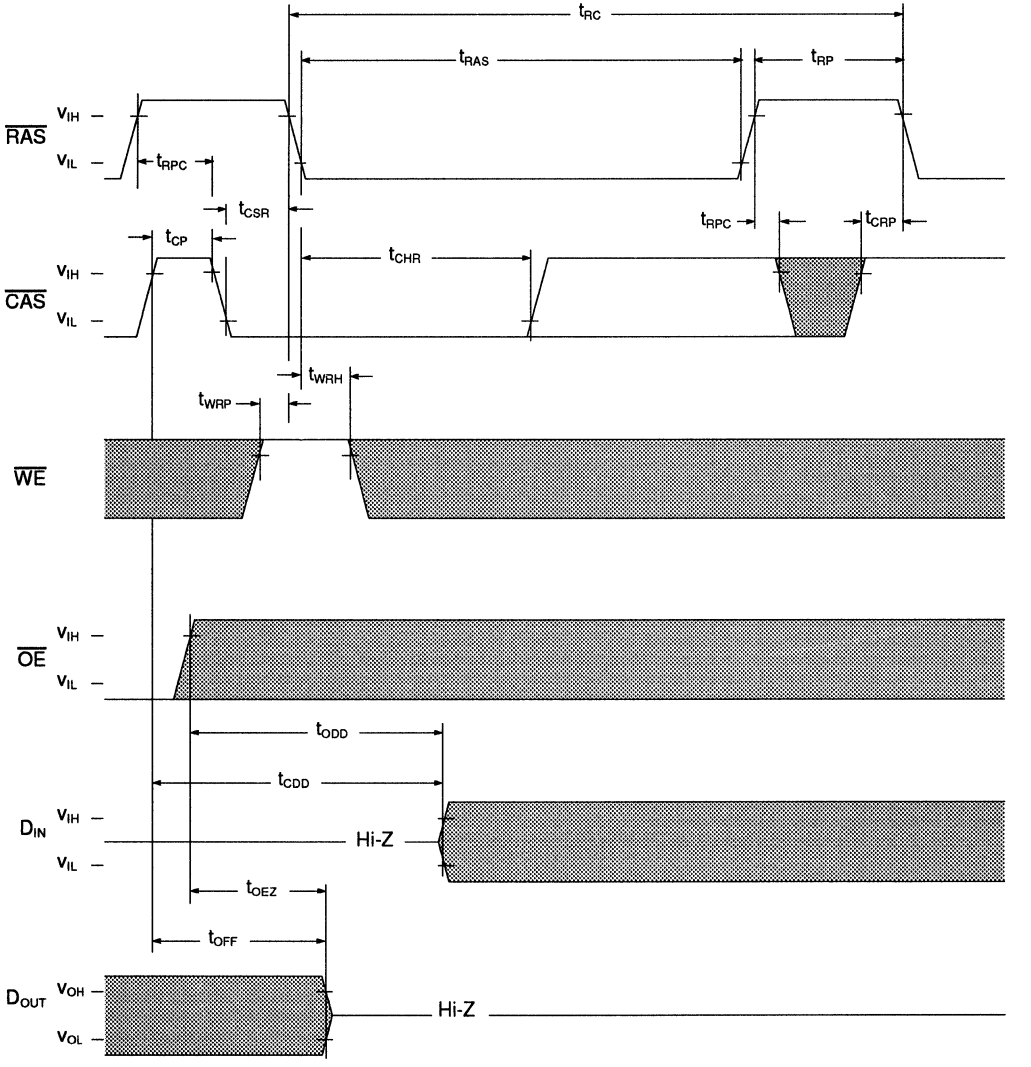


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

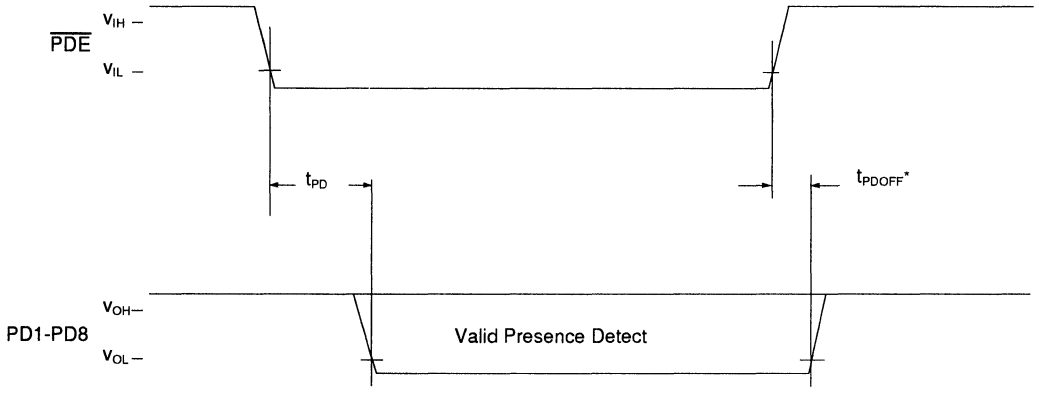
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



: "H" or "L"

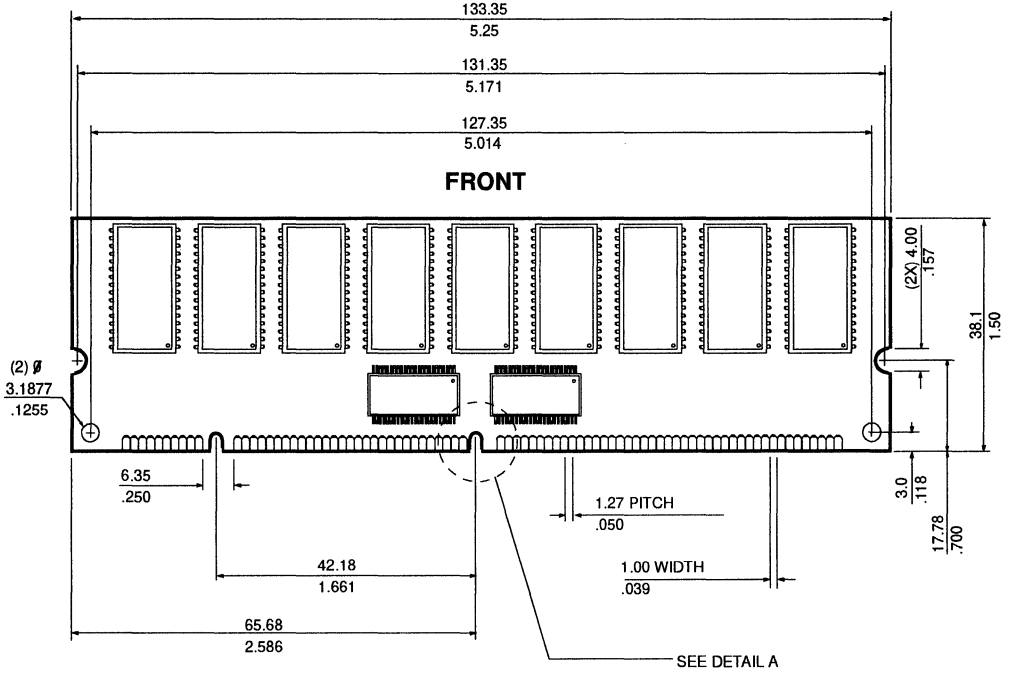
Note: Addresses are "H" or "L"

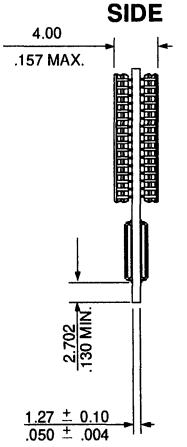
Presence Detect Read Cycle

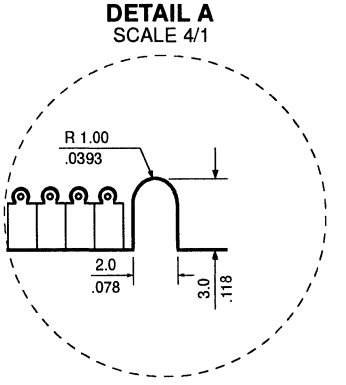


*PD pins must be pulled high at next level of assembly

Layout Drawing







NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 8Mx72 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are LVTTL and LVCMOS compatible
- Single 3.3V, ± 0.3V Power Supply
- Au contacts
- Optimized for ECC applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - 4 Byte Interleave enabled
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 4096 refresh cycles distributed across 64ms
- 12/10 addressing (Row/Column)
- Card size: 5.25" x 1.5" x 0.320"
- DRAMS in stacked TSOP Package

Description

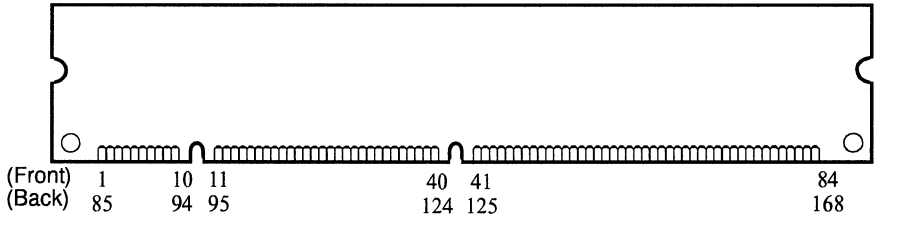
IBM11M8730PB is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as an 8Mx72 high speed memory array, and is configured as 2 4Mx72 banks. The DIMM uses 36 4Mx4 DRAMs, which are assembled as 18 stacked TSOP packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, the system will determine that ECC DIMMs are installed if PD8 is low (0). ID0 need not be sensed since both x72 and x80 ECC DIMMs will function in a x72 bank.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 and x72 parity (5V) DIMMs and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A11	Address Inputs (Buffered)
DQx	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

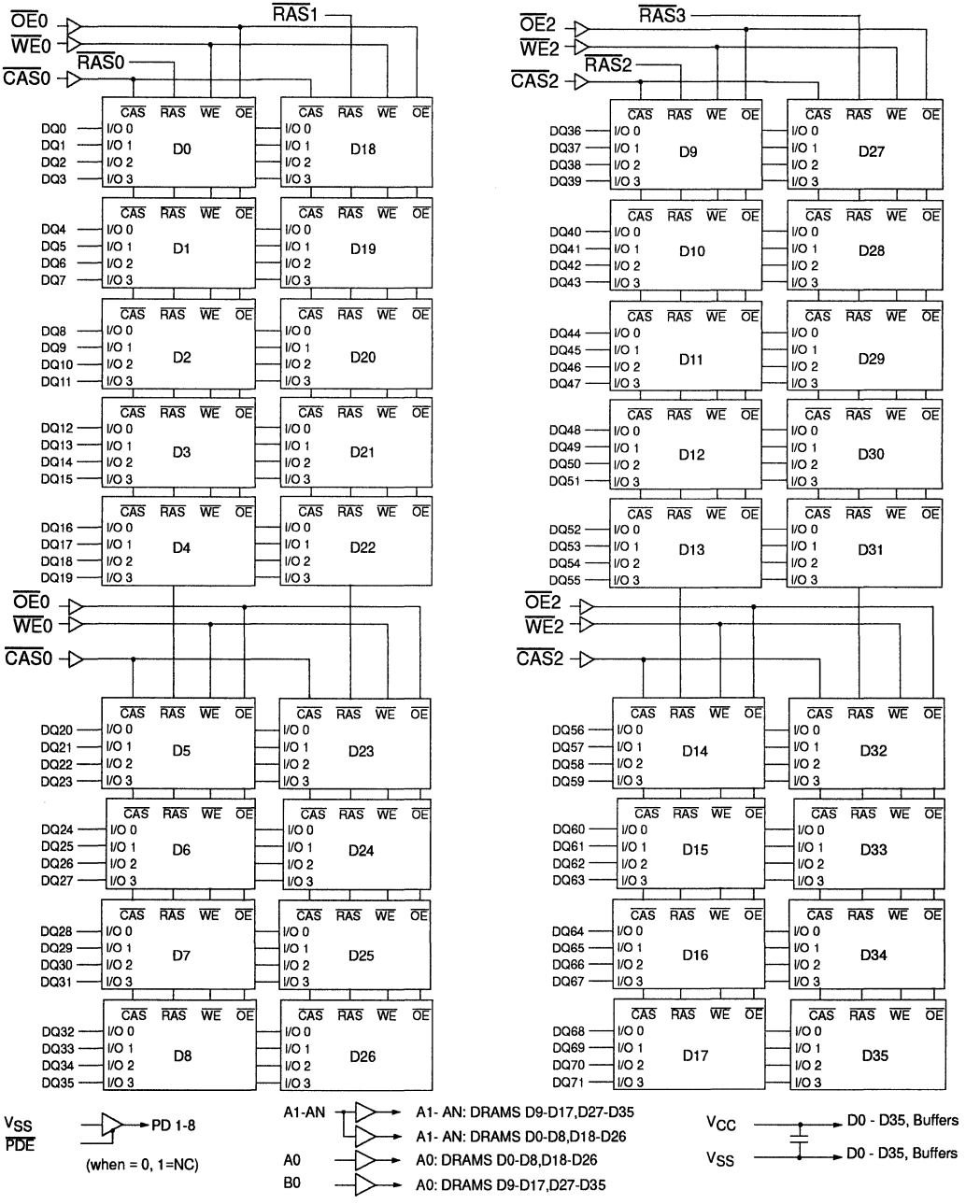
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	$\overline{RAS3}$
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	NC
5	DQ3	89	DQ39	47	NC	131	NC
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	DQ8	95	DQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	DQ17	106	DQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	DQ26	150	DQ62
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	NC	70	DQ29	154	DQ65
29	NC	113	NC	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	$\overline{RAS1}$	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	DQ35	161	DQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	A10	122	A11	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M8730PBA-60	8Mx72	60ns	Au	5.25"x1.5"x 0.320"	
IBM11M8730PBA-70	8Mx72	70ns	Au	5.25"x1.5"x 0.320"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	0	0
PD2	0	0
PD3	1	1
PD4	1	1
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	0	0
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 4.6	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	11	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A11)	18	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	80	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	18	pF	
C_{I4}	DQ_X Capacitance	22	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1566	mA	1, 2, 3
		-70	—	1386		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	72	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1566	mA	1, 3, 4
		-70	—	1386		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1386	mA	1, 2, 3
		-70	—	1206		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	36	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1566	mA	1, 3, 4
		-70	—	1386		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-20	+20	µA	
		$\overline{RAS}$	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. Refresh current is specified for 1 bank.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required..
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the Dram device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	1
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	4
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	5
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
2. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.
5. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	2	—	ns	1
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	3
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	36	—	41	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	36	—	41	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	—	—	—	—	ns	4
t_{OH}	Output Data Hold Time	2	—	2	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1, 2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	63	—	73	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	64	—	64	ms	1

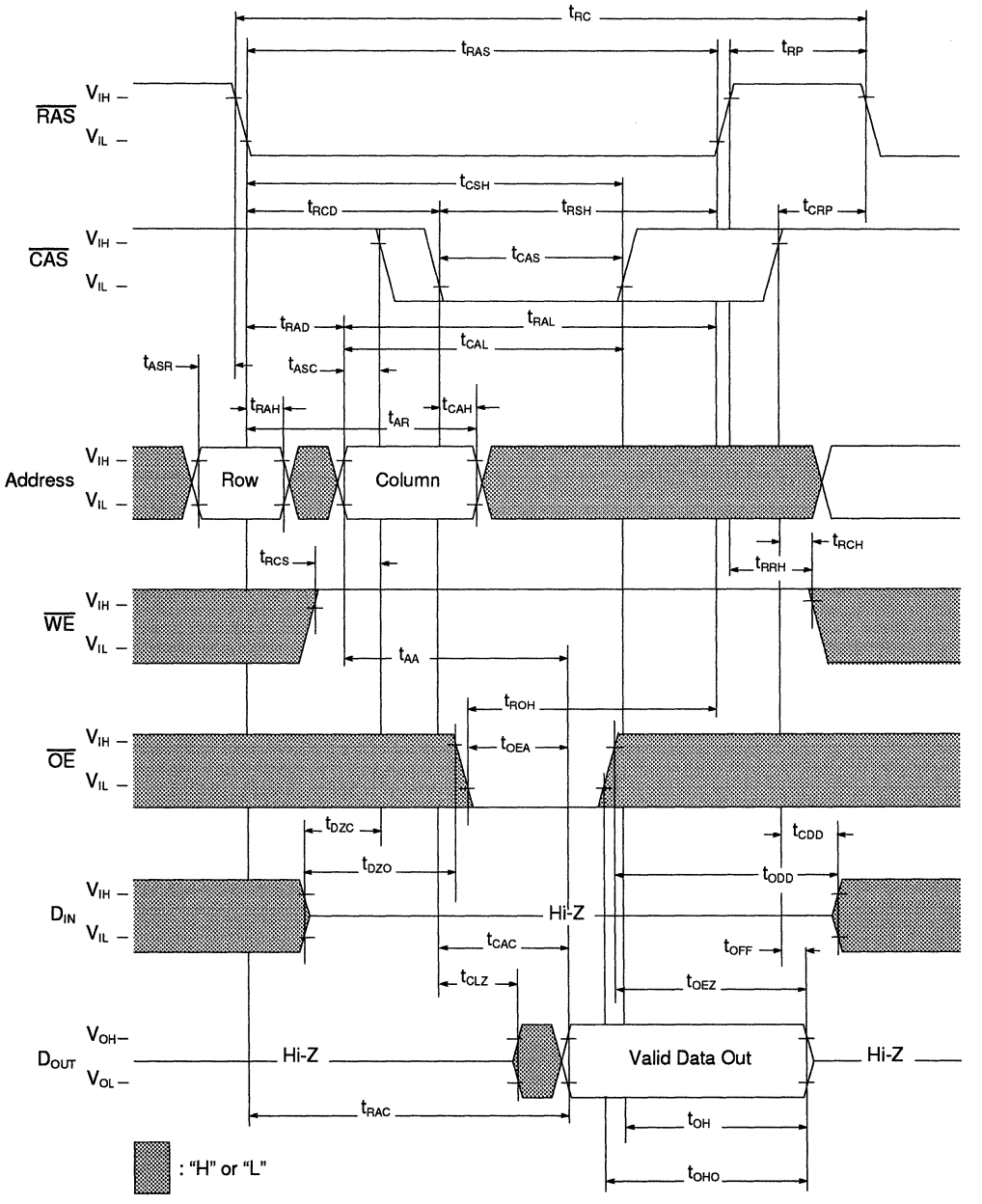
1. 4096 refreshes are required every 64ms.

Presence Detect Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
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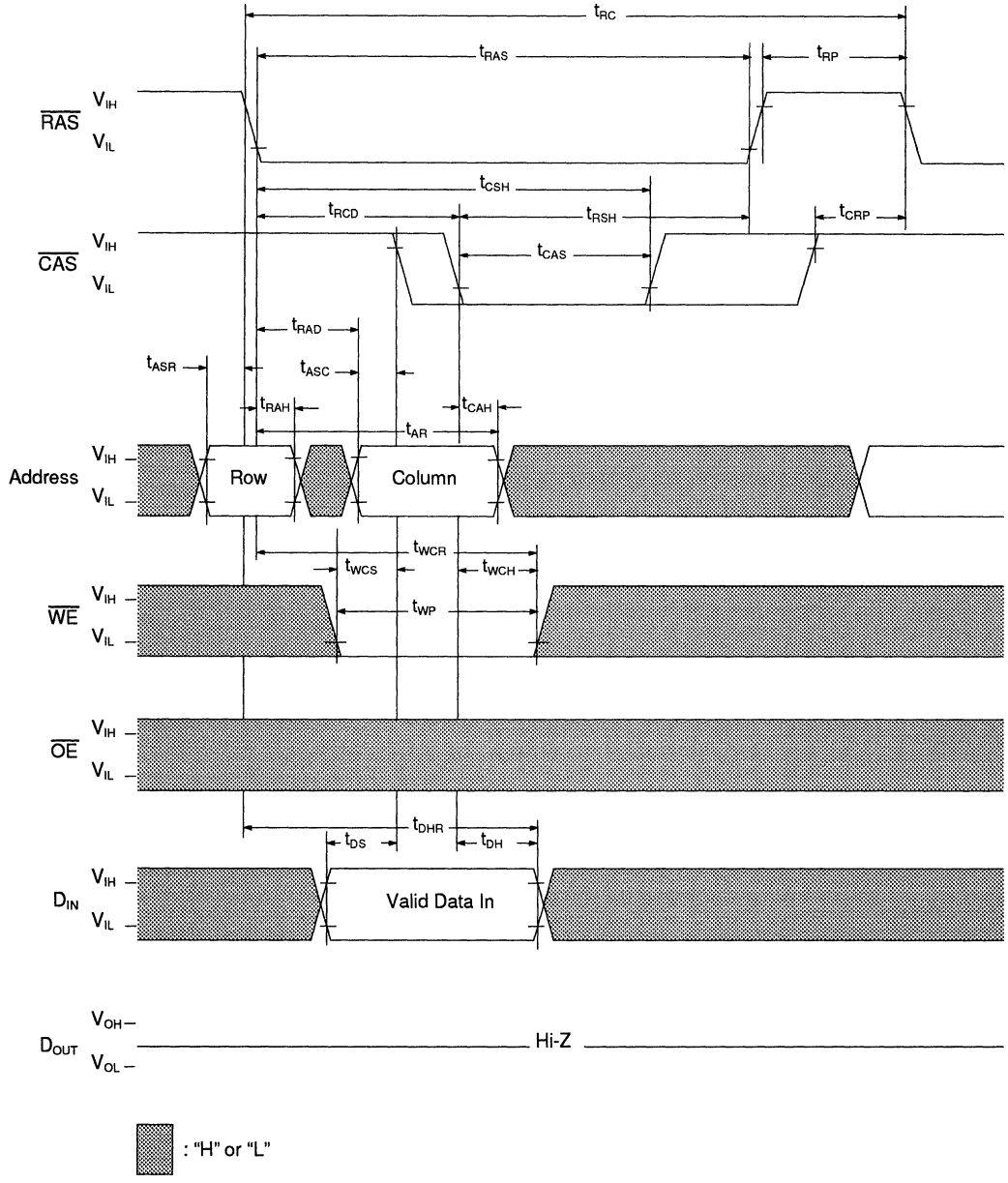
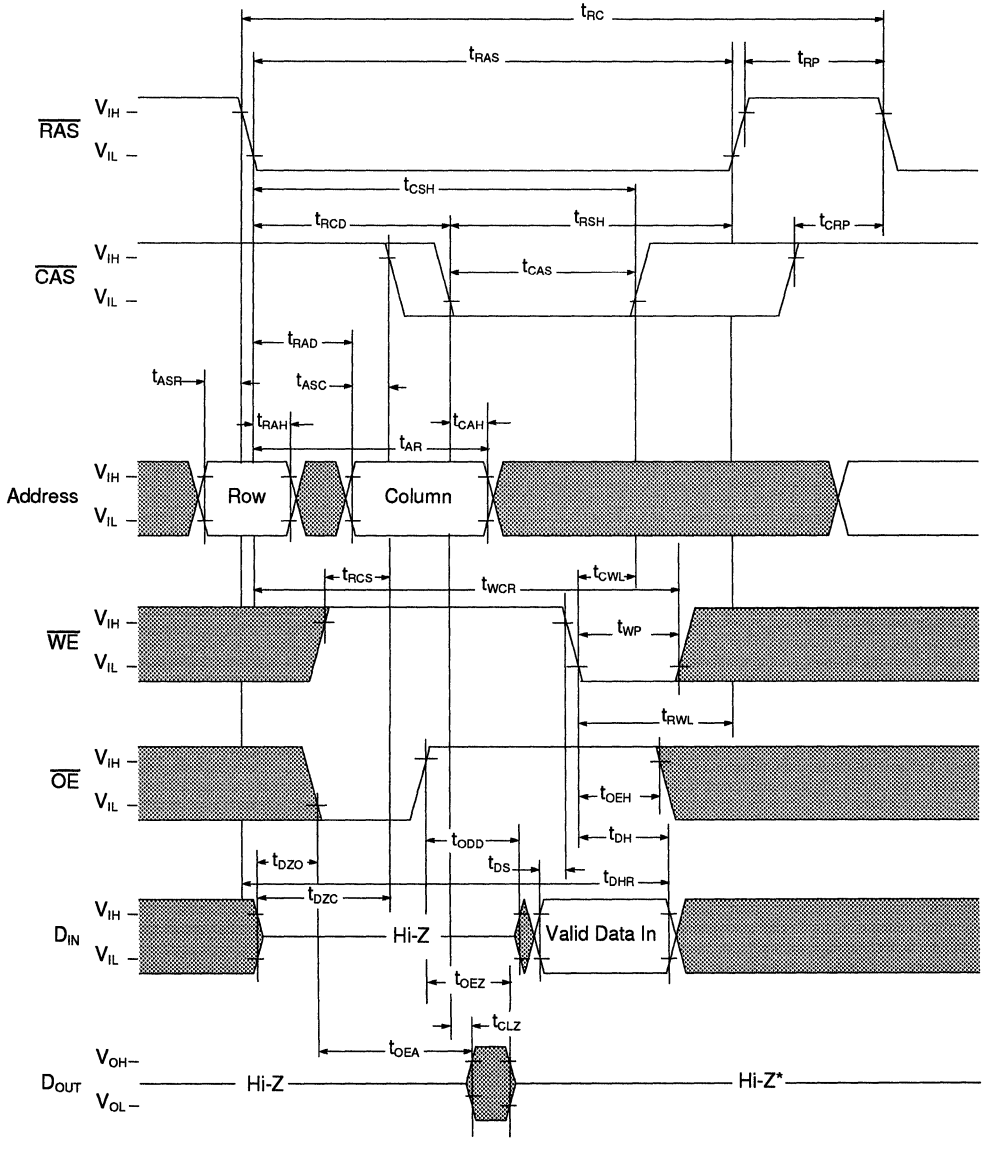
tCAL
tASR
tASC
tRAH
tCAH
tAR
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

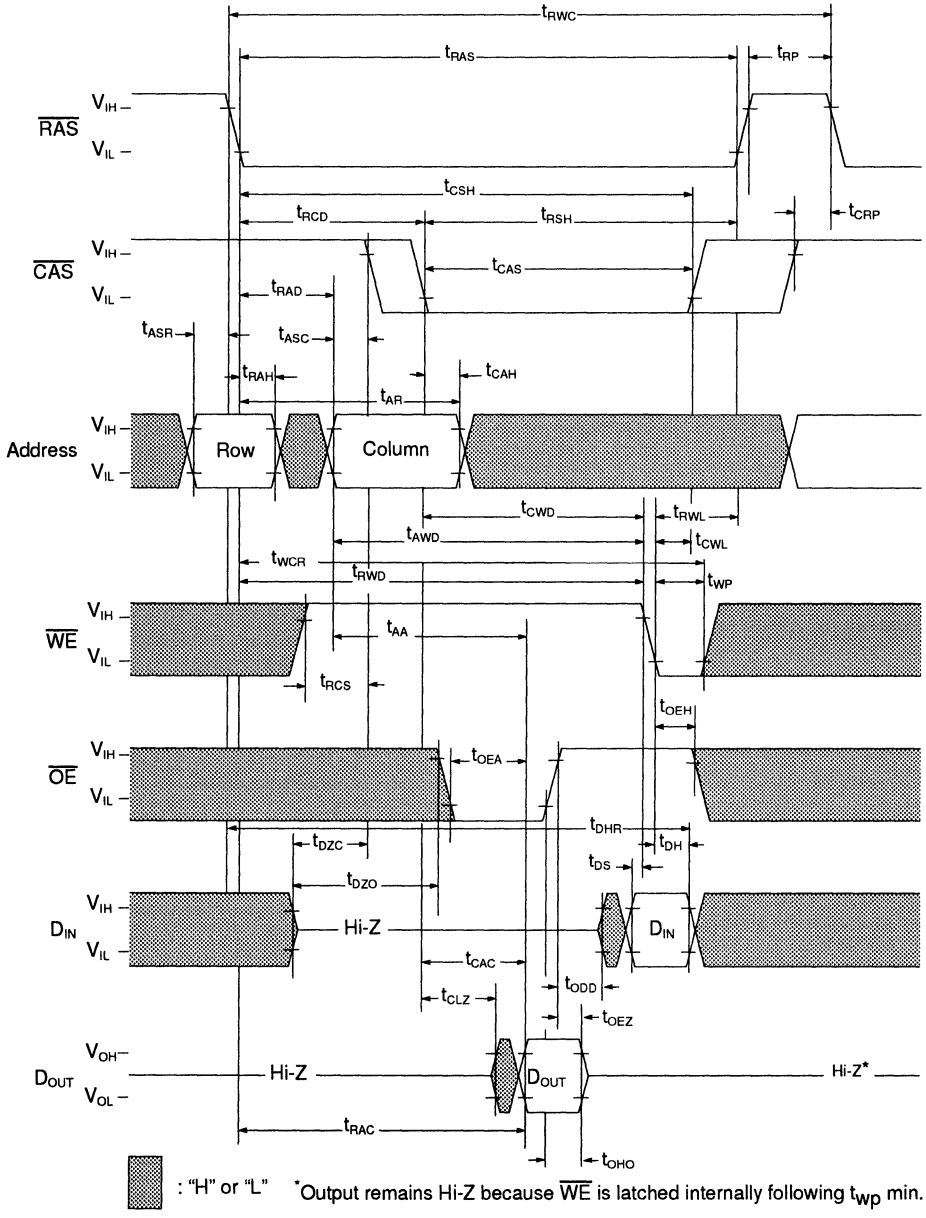


Write Cycle (Late Write)

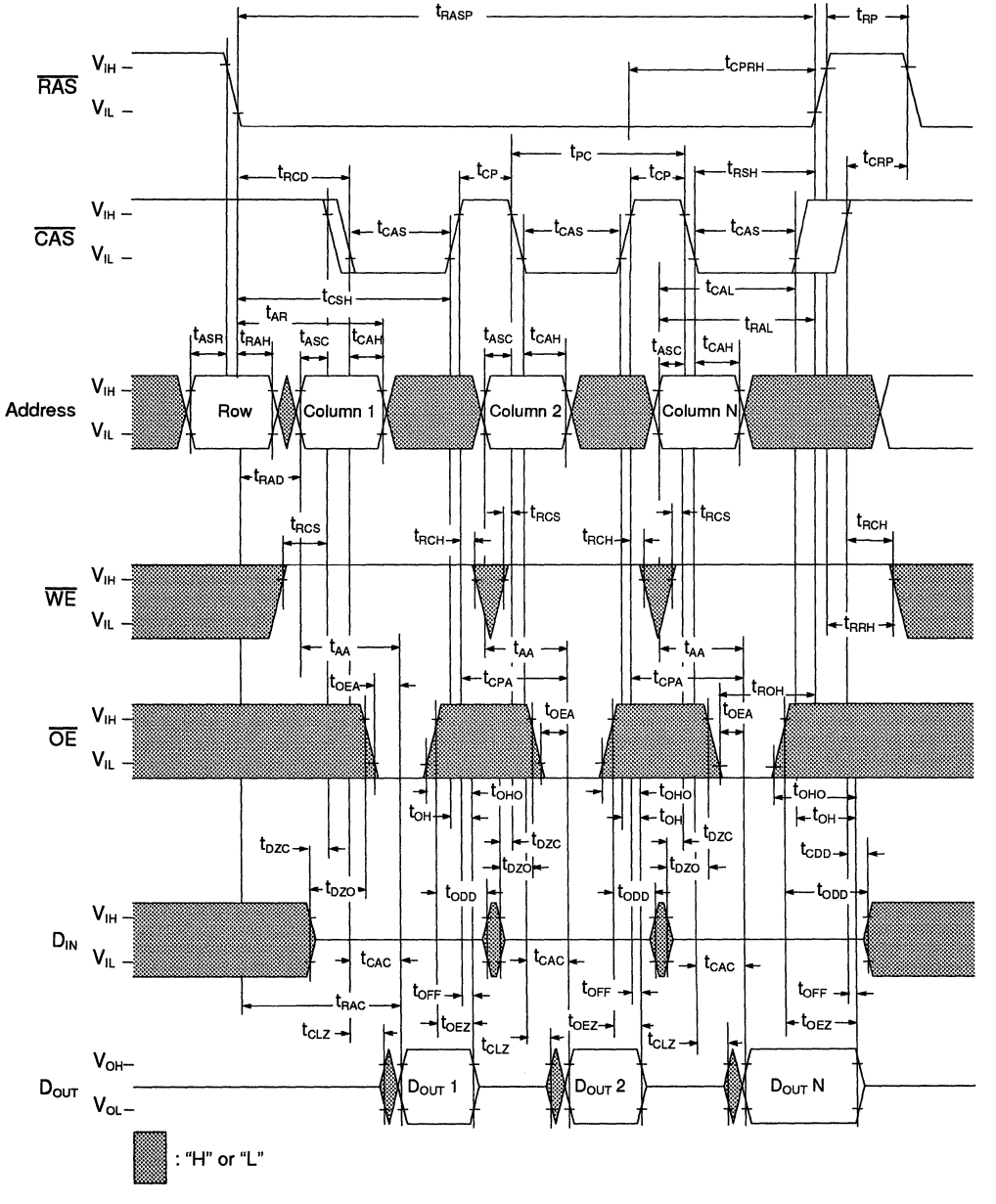


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{wp} min.

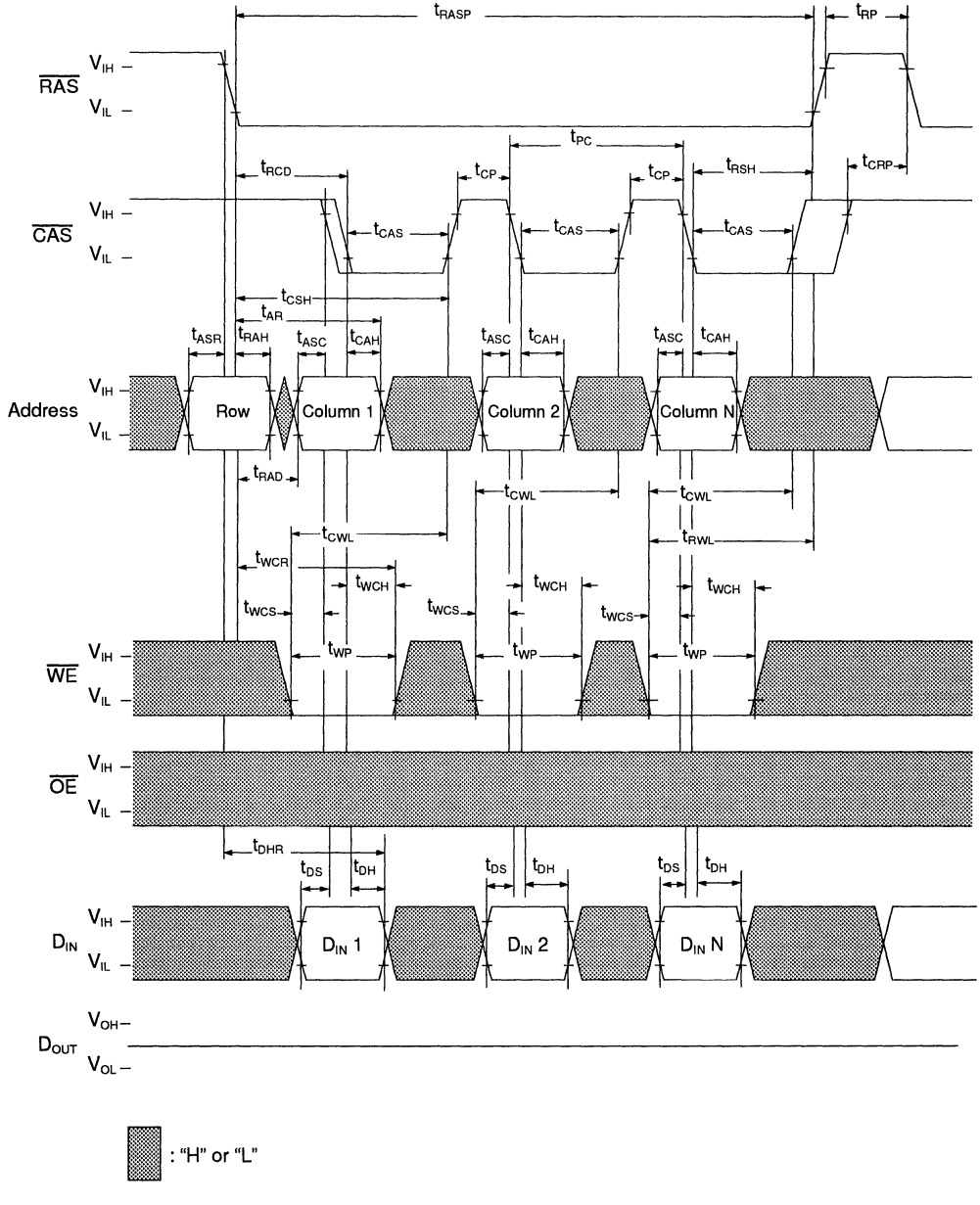
Read-Modify-Write-Cycle



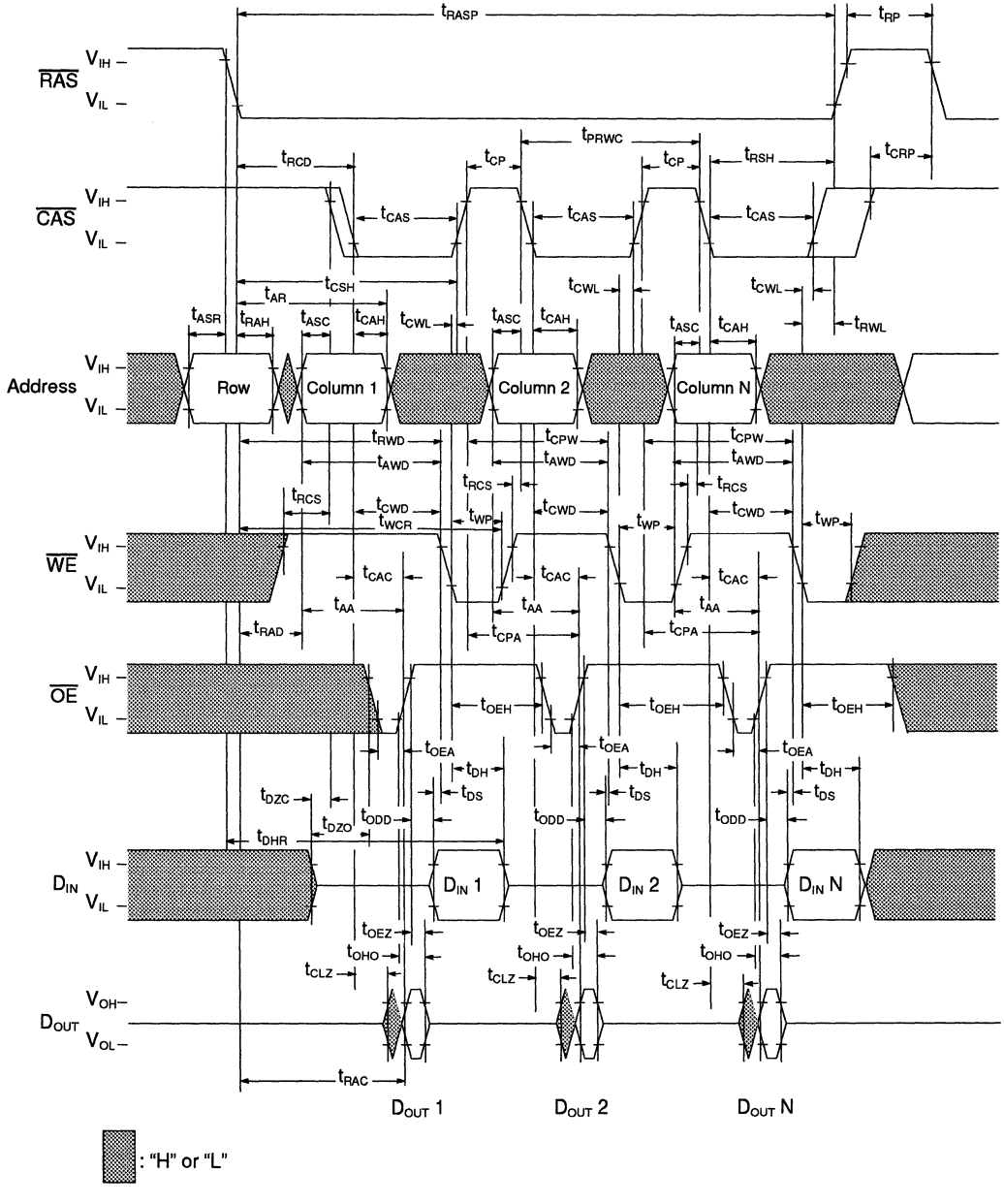
Fast Page Mode Read Cycle



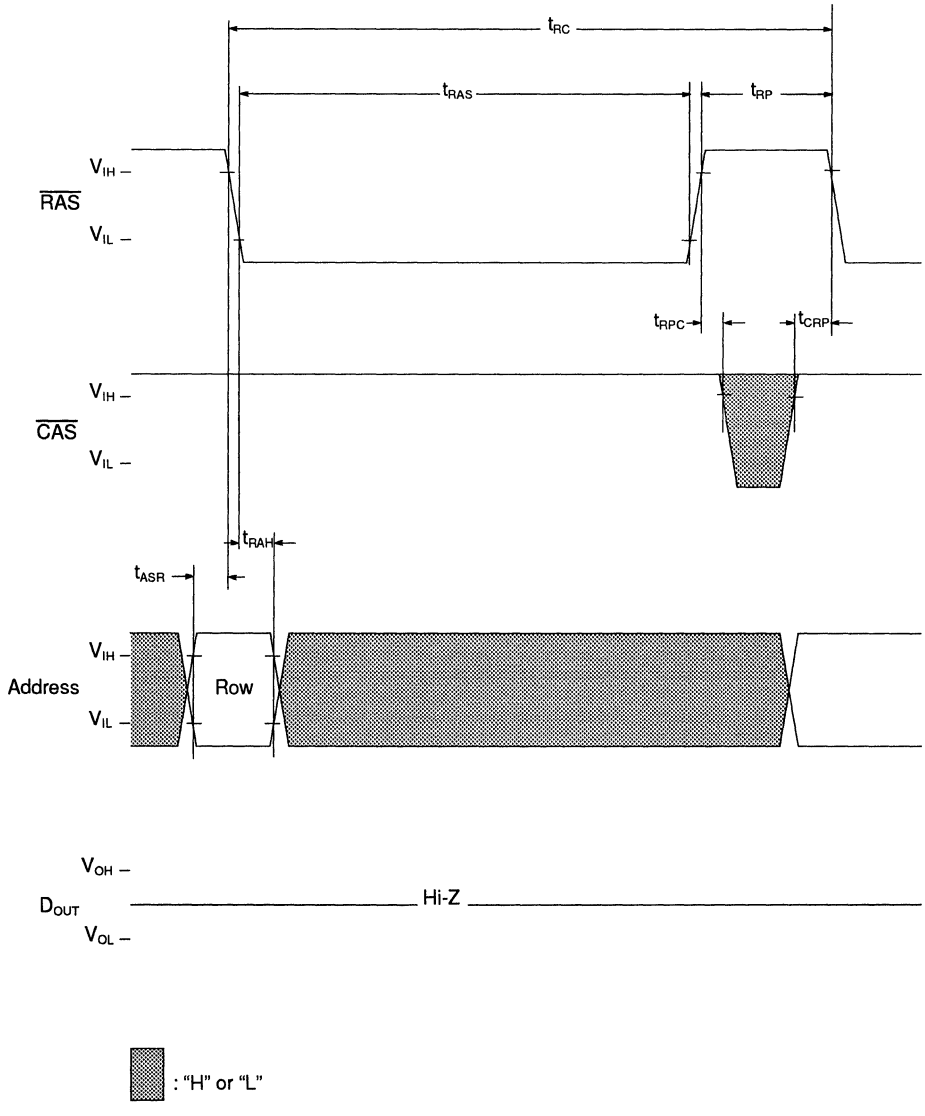
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

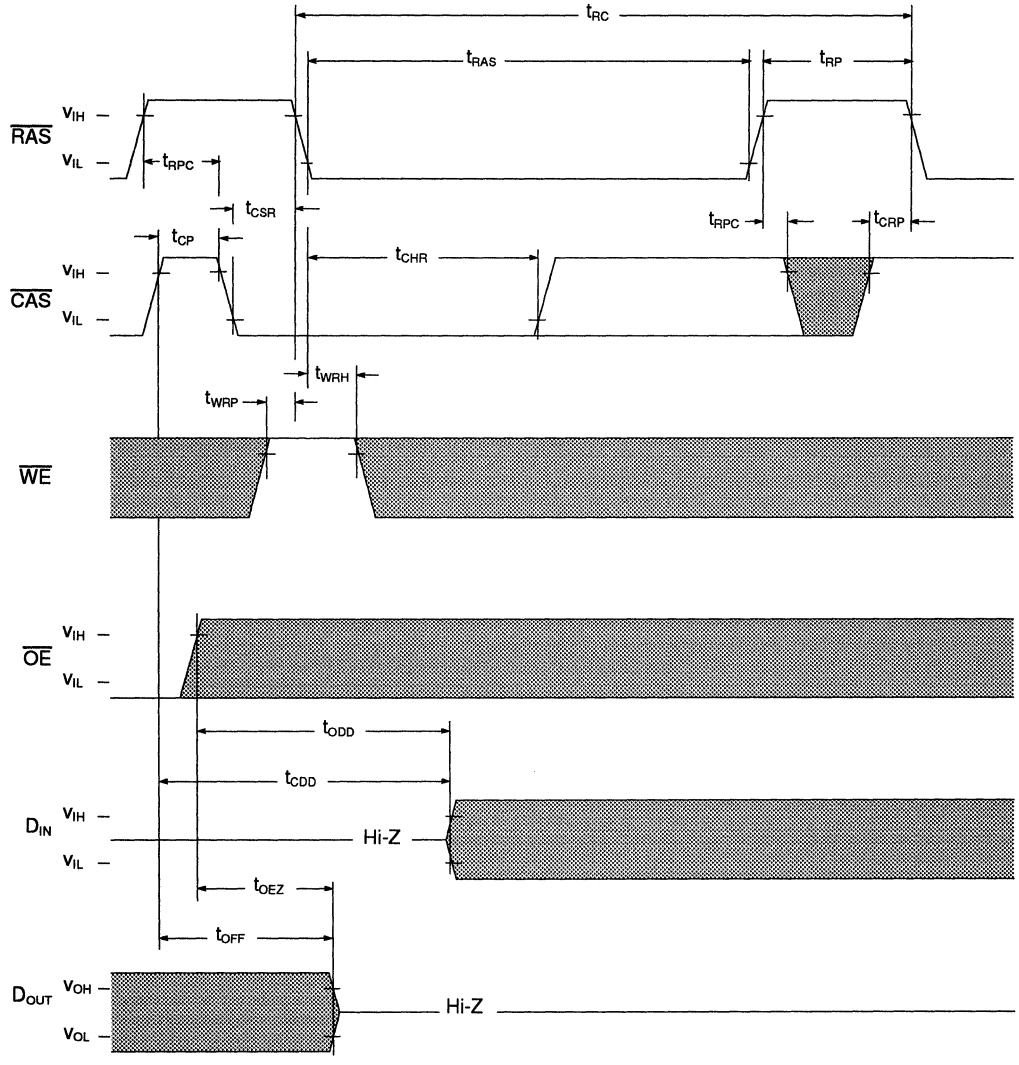


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

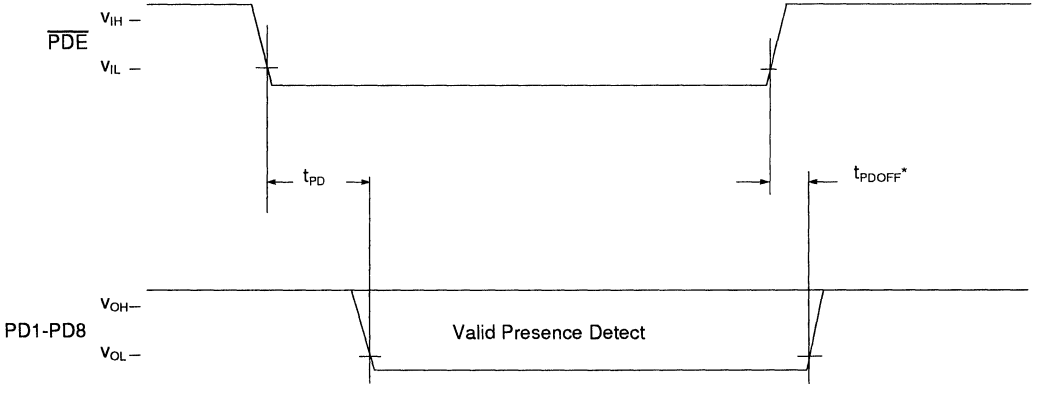
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



: "H" or "L"

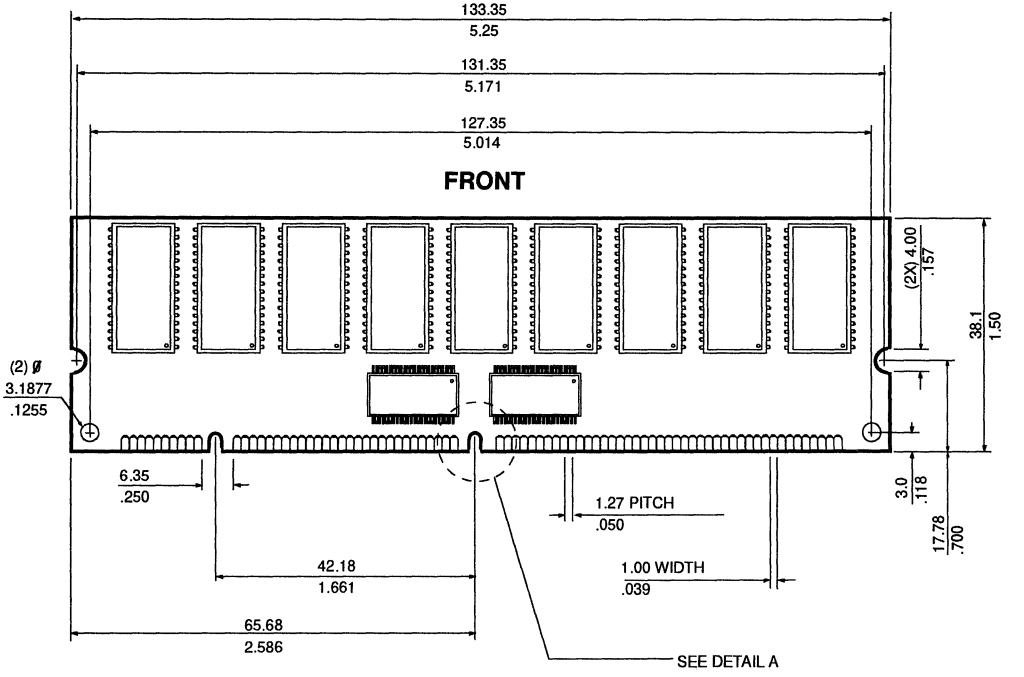
Note: Addresses are "H" or "L"

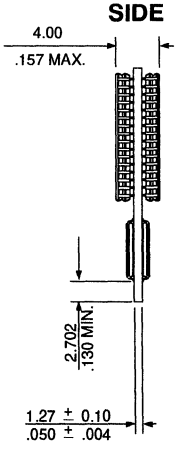
Presence Detect Read Cycle

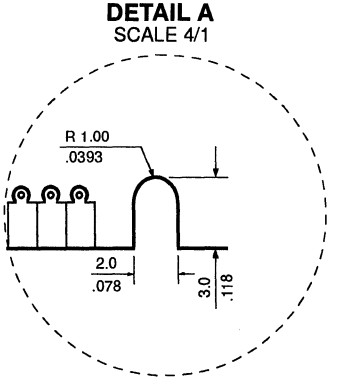


*PD pins must be pulled high at next level of assembly

Layout Drawing







NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 8Mx72 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are LVTTL and LVCMOS compatible
- Single 3.3V, ± 0.3V Power Supply
- Au contacts
- Optimized for ECC applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 4096 refresh cycles distributed across 64ms
- 12/11 addressing (Row/Column)
- Card size: 5.25" x 1.2" x 0.157"
- DRAMS in TSOP Package

Description

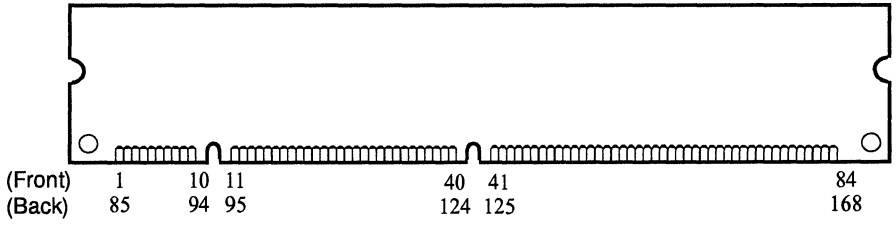
IBM11M8730HB is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as an 8Mx72 high speed memory array for ECC applications. The DIMM uses 9 8Mx8 DRAMs in TSOP packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, the system will determine that ECC DIMMs are installed if PD8 is low (0). ID0 need not be sensed since both x72 and x80 ECC DIMMs will function in a x72 bank.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 and x72 parity (5V) DIMMs and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A11	Address Inputs (Buffered)
DQx	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

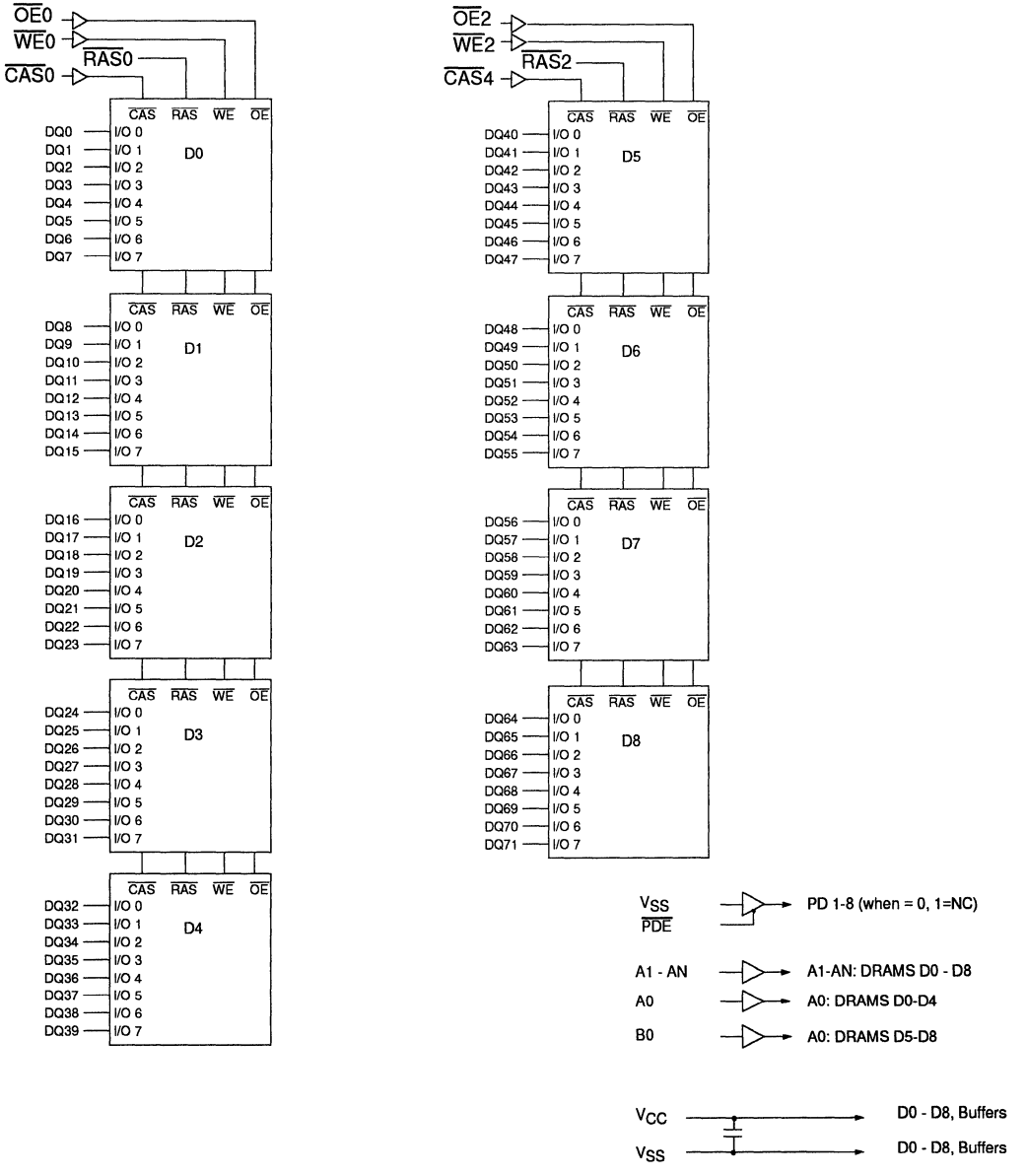
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	NC
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	NC
5	DQ3	89	DQ39	47	NC	131	NC
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	DQ8	95	DQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	DQ17	106	DQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	DQ26	150	DQ62
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	NC	70	DQ29	154	DQ65
29	NC	113	NC	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	NC	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	DQ35	161	DQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	A10	122	A11	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M8730HBA-60	8Mx72	60ns	Au	5.25"x1.2"x 0.157"	
IBM11M8730HBA-70	8Mx72	70ns	Au	5.25"x1.2"x 0.157"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	1	1
PD2	0	0
PD3	1	1
PD4	1	1
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	0	0
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +4.6	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	3.9	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to Vss.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A11)	13	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	40	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF	
C_{I4}	DQ_X Capacitance	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1080	mA	1,2,3
		-70	—	990		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	18	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1080	mA	1,3
		-70	—	990		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	675	mA	1,2,3
		-70	—	585		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	1.8	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1080	mA	1,3
		-70	—	990		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-50	+50		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the Dram device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	1
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	4
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	—	5
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
2. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.
5. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	2	—	ns	1
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	3
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	36	—	41	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	36	—	41	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	—	—	—	—	ns	4
t_{OH}	Output Data Hold Time	2	—	2	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1, 2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	63	—	73	—	ns	1

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	64	—	64	ms	1

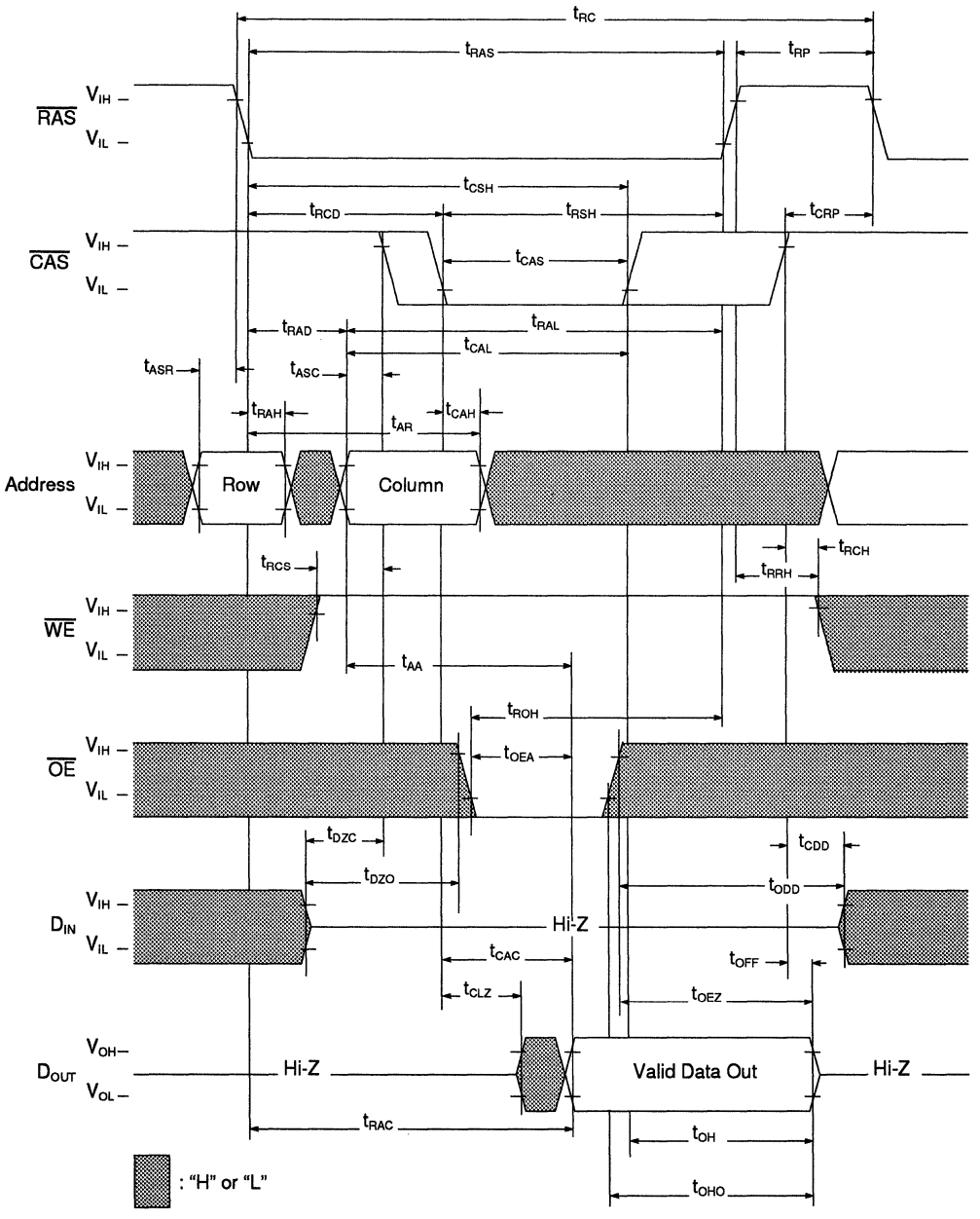
1. 4096 refreshes are required every 64ms.

Presence Detect Read Cycle

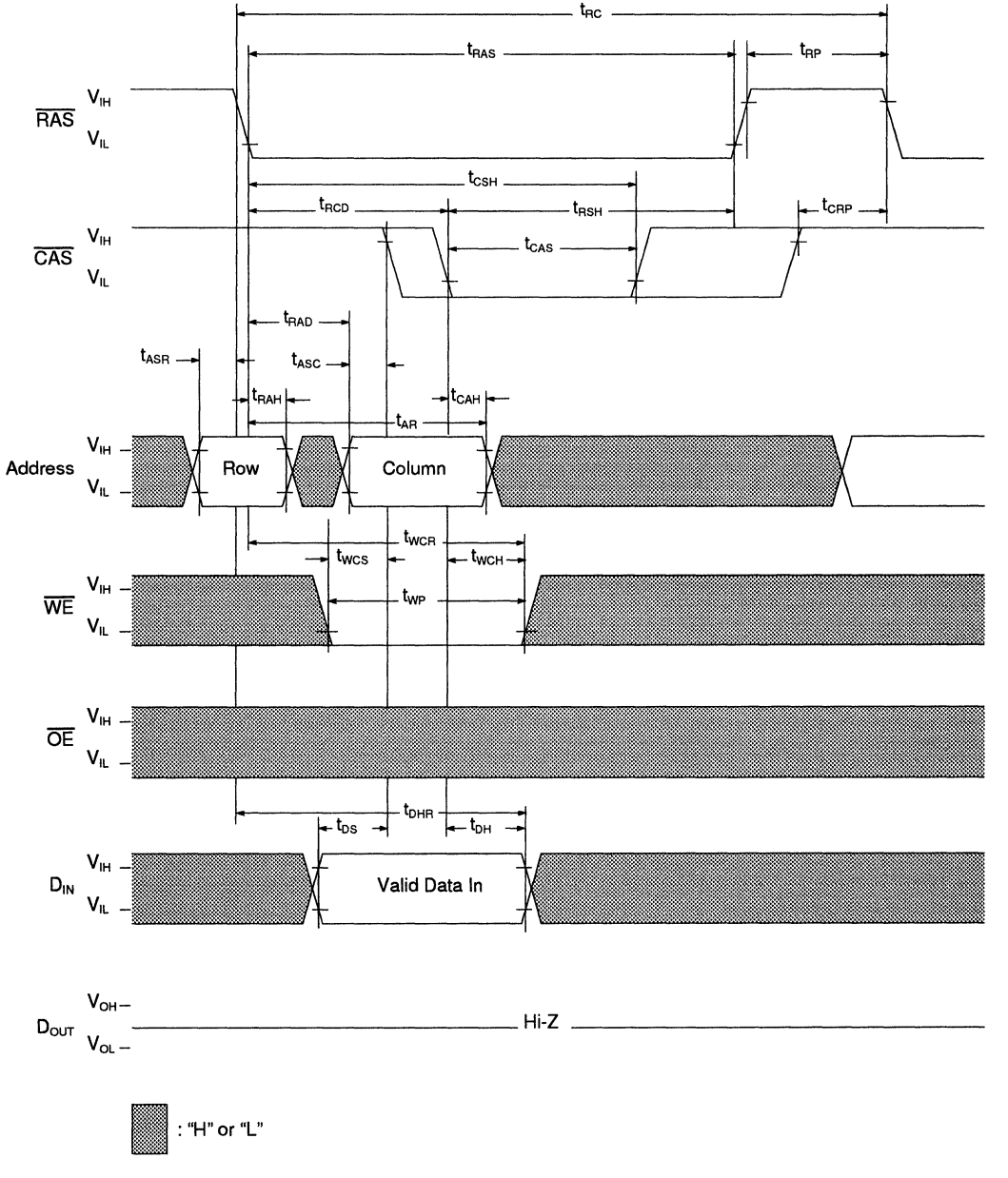
Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

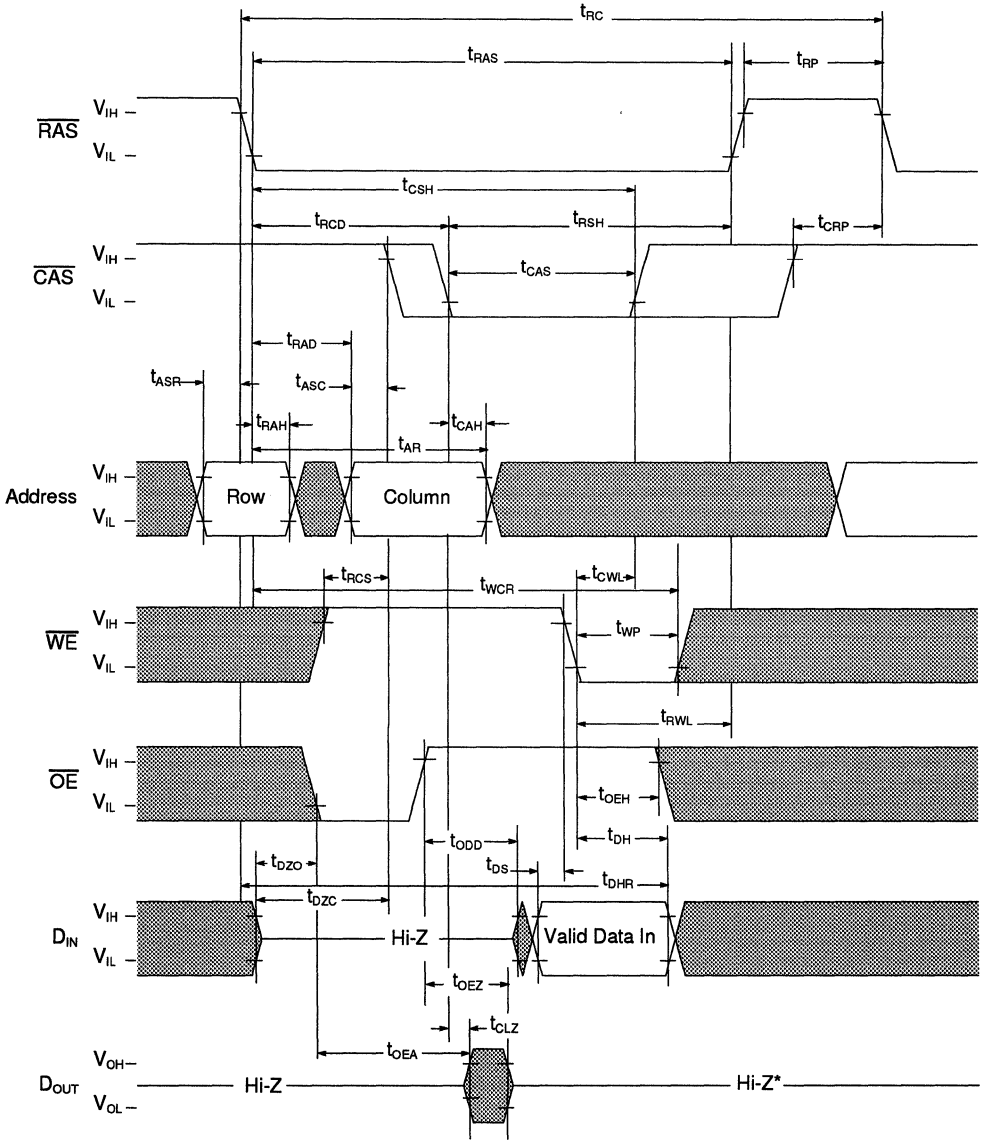
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tAR
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

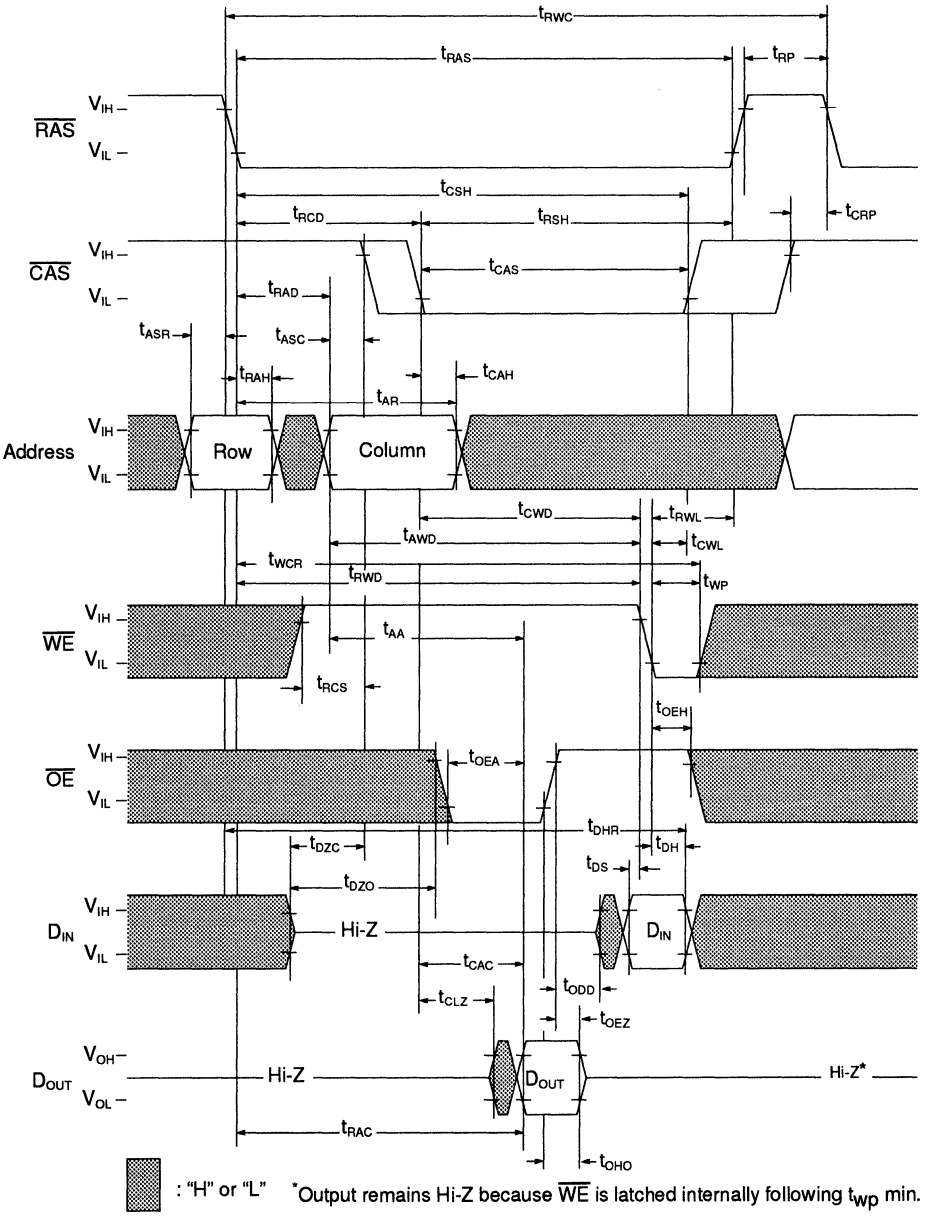


Write Cycle (Late Write)

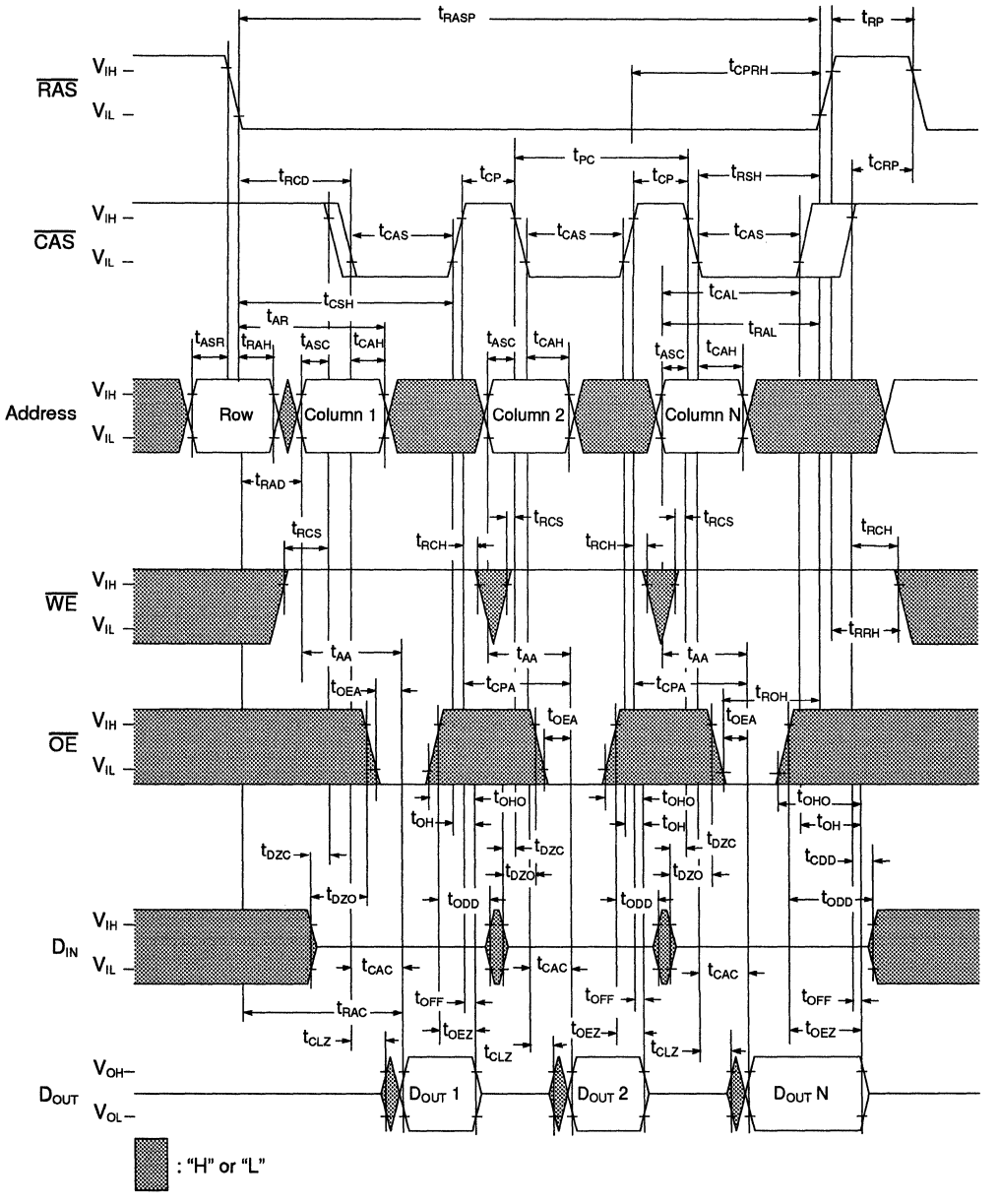


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{wp} min.

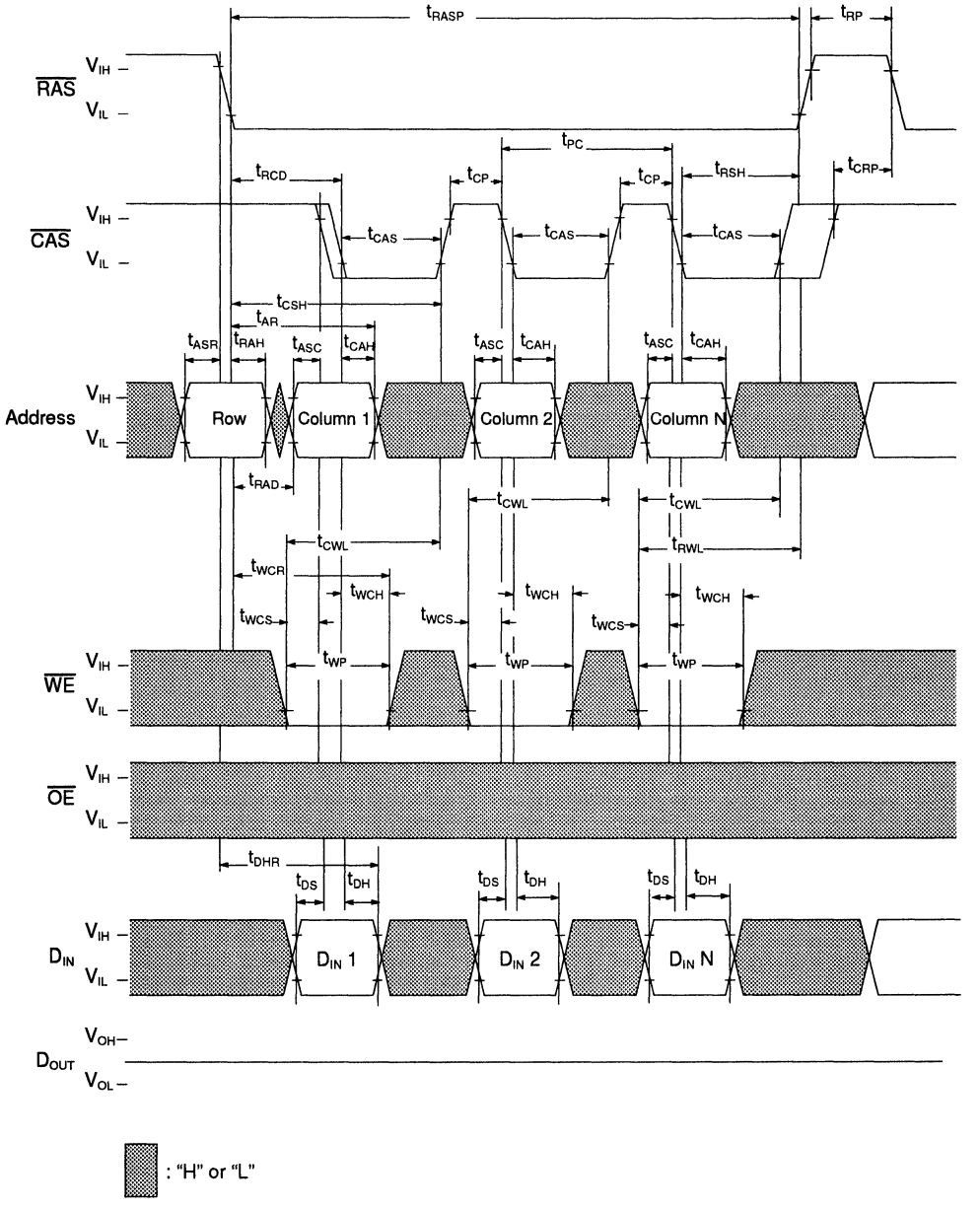
Read-Modify-Write-Cycle



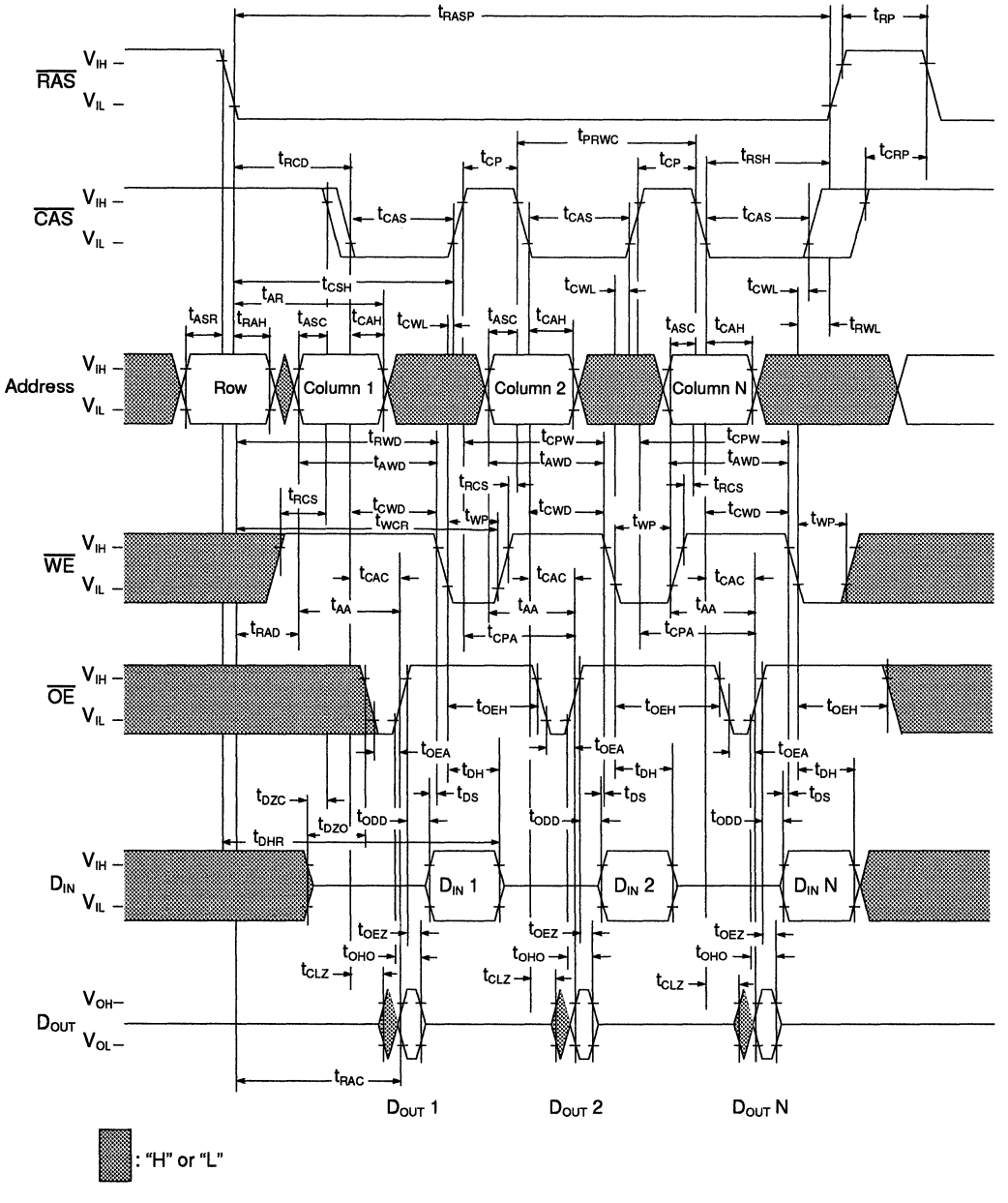
Fast Page Mode Read Cycle



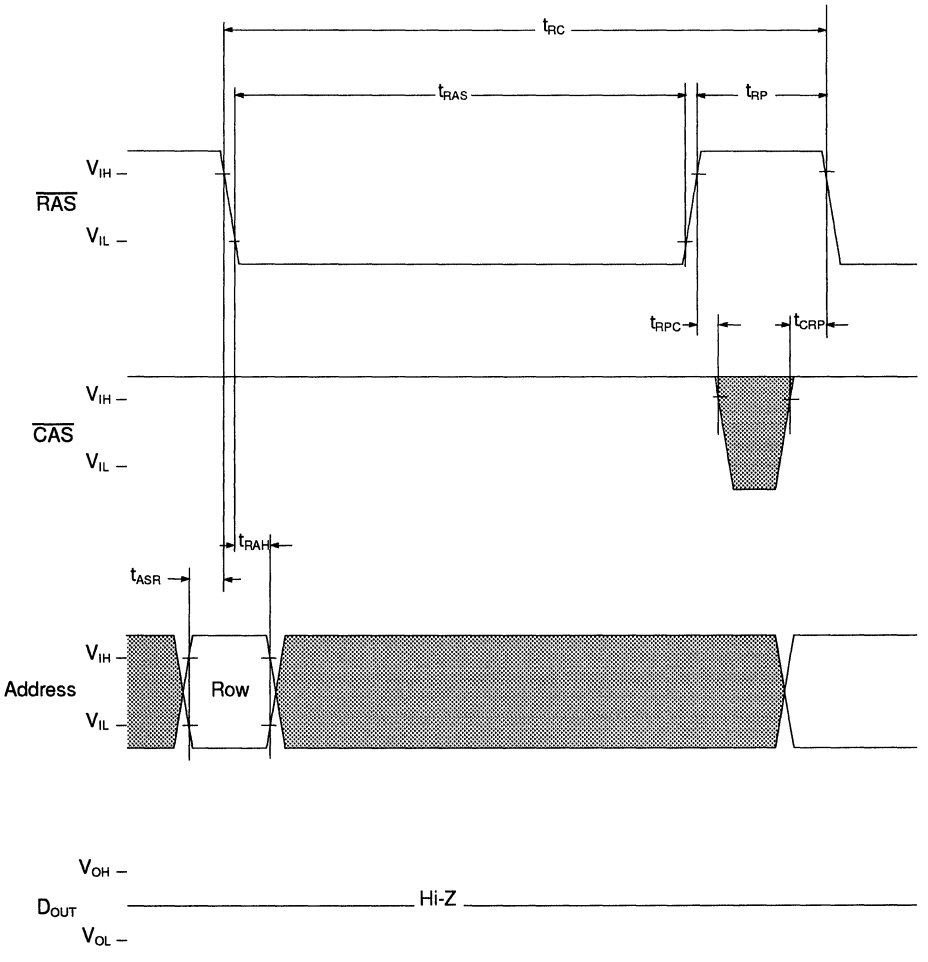
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

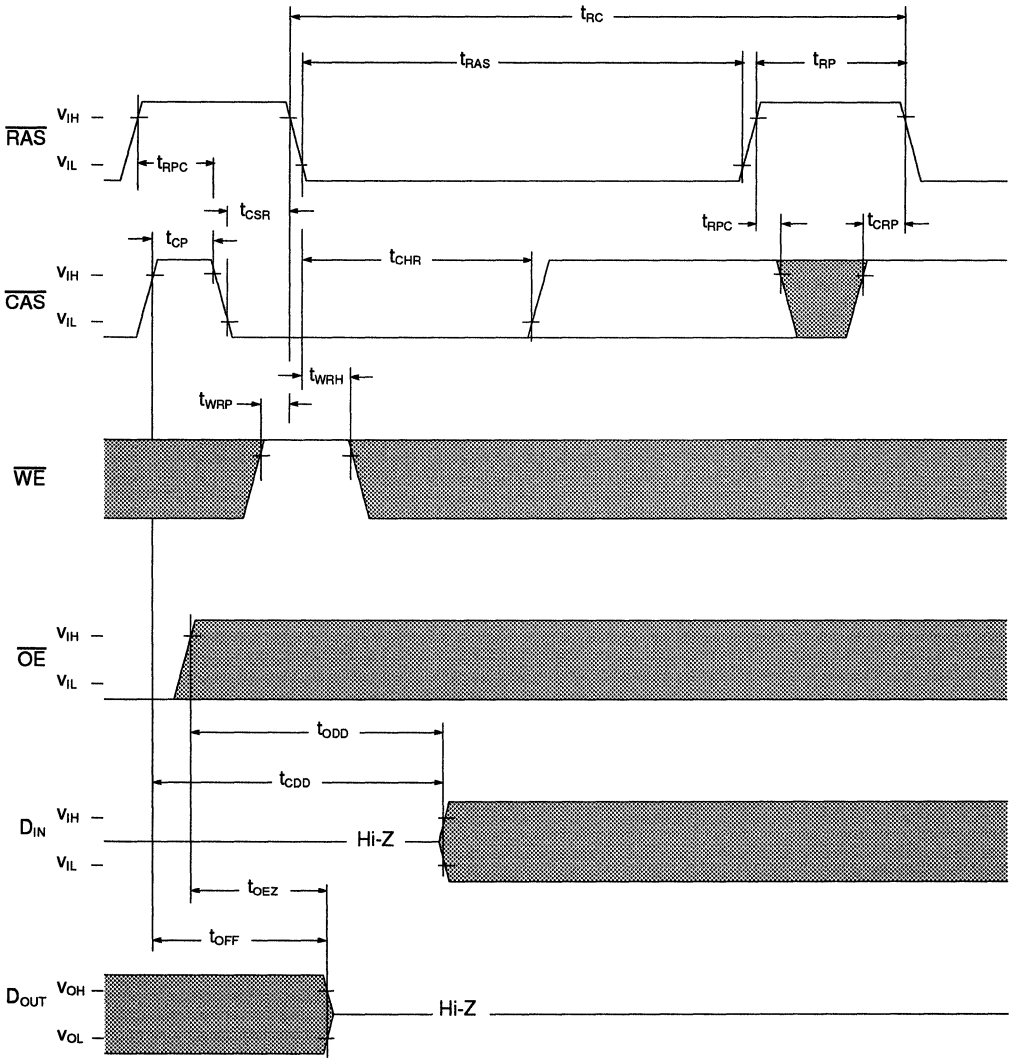


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

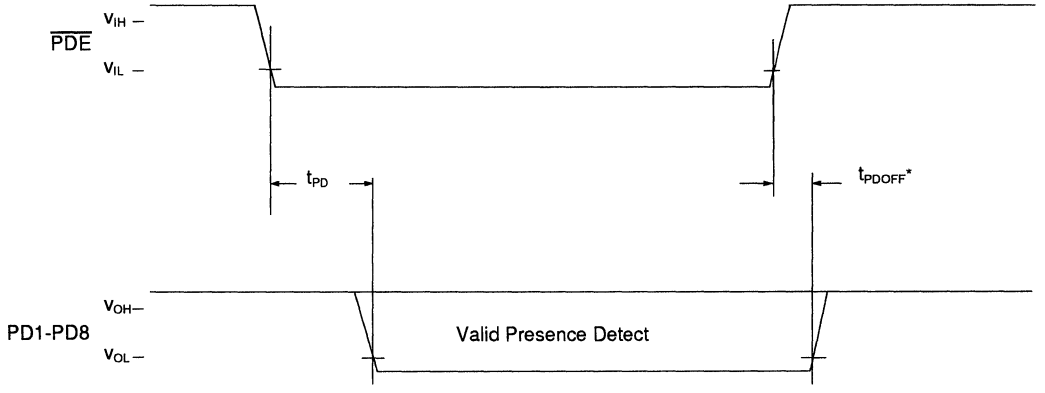
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



: "H" or "L"

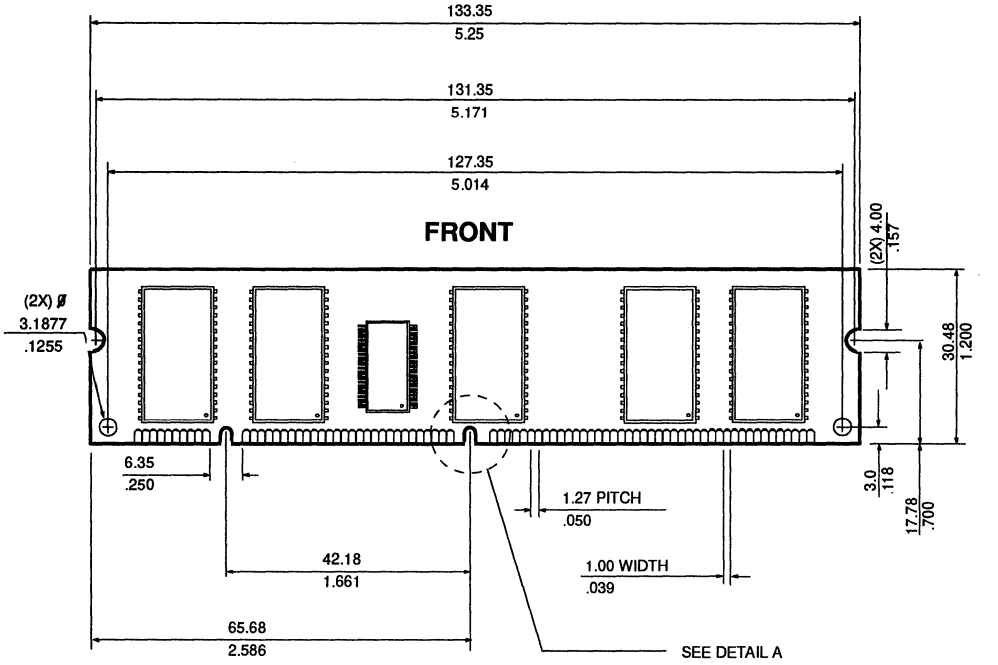
Note: Addresses are "H" or "L"

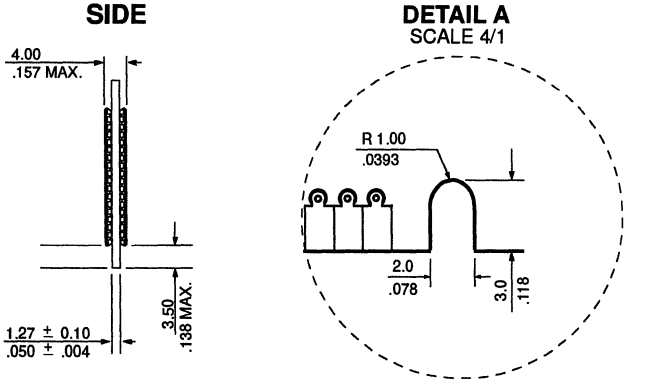
Presence Detect Read Cycle



*PD pins must be pulled high at next level of assembly

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 16Mx72 Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	36ns	41ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are LVTTL and LVCMOS compatible
- Single 3.3V, ± 0.3V Power Supply
- Au contacts
- Optimized for ECC applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced noise (32 V_{SS}/V_{CC} pins)
  - 4 Byte Interleave enabled
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 8192 refresh cycles distributed across 128ms
- 13/11 addressing (Row/Column)
- Card size: 5.25" x 1.5" x 0.157"
- DRAMS in TSOP Package

Description

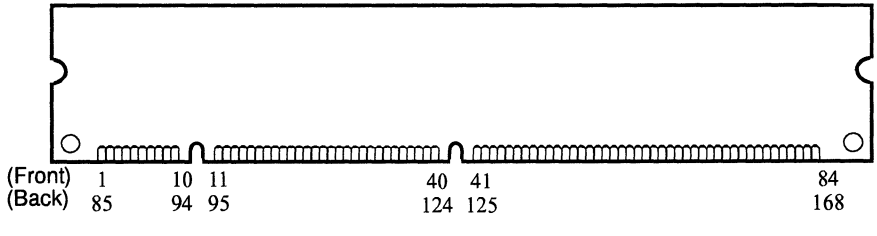
IBM11M16730CB is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 16Mx72 high speed memory array for ECC applications. The DIMM uses 18 16Mx4 DRAMs in TSOP packages.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, the system will determine that ECC DIMMs are installed if PD8 is low (0). ID0 need not be sensed since both x72 and x80 ECC DIMMs will function in a x72 bank.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 and x72 parity (5V) DIMMs and ECC DIMMs (5V and 3.3V).

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A12	Address Inputs (Buffered)
DQx	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

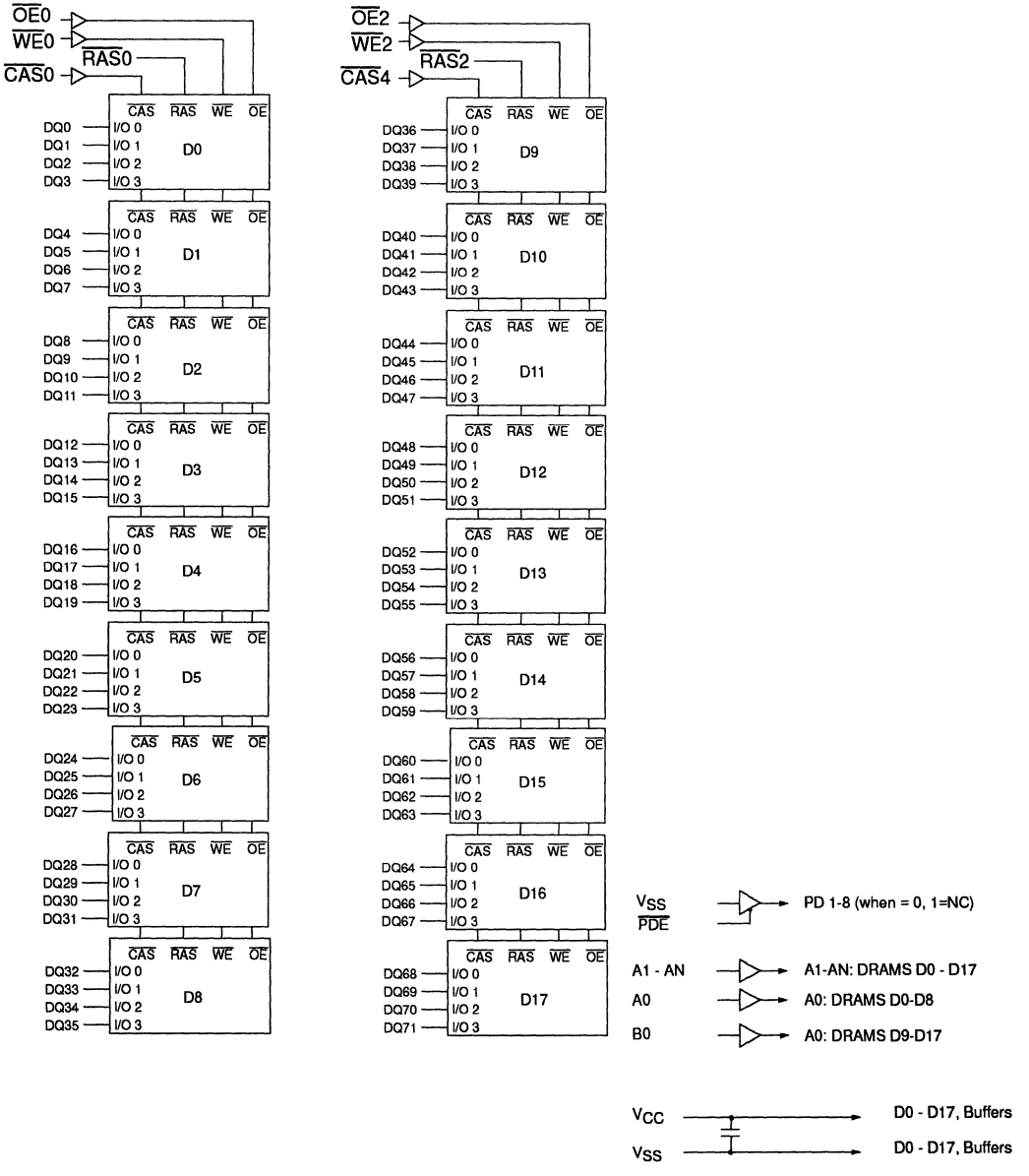
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE2}$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS2}$	129	NC
4	DQ2	88	DQ38	46	$\overline{CAS4}$	130	NC
5	DQ3	89	DQ39	47	NC	131	NC
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	DQ8	95	DQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	DQ17	106	DQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	DQ26	150	DQ62
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE0}$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS0}$	112	NC	70	DQ29	154	DQ65
29	NC	113	NC	71	DQ30	155	DQ66
30	$\overline{RAS0}$	114	NC	72	DQ31	156	DQ67
31	$\overline{OE0}$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	DQ35	161	DQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	A10	122	A11	80	PD3	164	PD4
39	A12	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Notes
IBM11M16730CBA-60	16Mx72	60ns	Au	5.25"x1.5"x 0.157"	
IBM11M16730CBA-70	16Mx72	70ns	Au	5.25"x1.5"x 0.157"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby	H	X	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	X	Valid Data Out
Early-Write	L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW	L	L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle	L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle	L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle	L	H→L	H→L	H→L	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	H→L	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	X	High Impedance
Read Presence Detects	X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD5: Addressing/Density)	1	1
PD2	1	1
PD3	1	1
PD4	1	1
PD5	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	0	0
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 4.6	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	3.6	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0, B0, A1-A12)	13	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	80	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF	
C_{I4}	DQ_X Capacitance	17	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1980	mA	1,2,3
		-70	—	1620		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	36	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1980	mA	1,3
		-70	—	1620		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1350	mA	1,2,3
		-70	—	1170		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	3.6	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1980	mA	1,3
		-70	—	1620		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	

1. I_{CC1},I_{CC3},I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1},I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required..
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the Dram device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	1
t_{ASR}	Row Address Setup Time	6	—	6	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	4	—	4	—	ns	
t_{CAH}	Column Address Hold Time	17	—	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	13	29	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	4
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	5
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
2. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{ODD} must be satisfied.
5. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	2	—	ns	1
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	3
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	36	—	41	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	3	—	3	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	36	—	41	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	36	—	41	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	—	—	—	—	ns	4
t_{OH}	Output Data Hold Time	2	—	2	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	25	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	6
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	25	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1, 2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	59	—	69	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	20	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	63	—	73	—	ns	1

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	128	—	128	ms	1

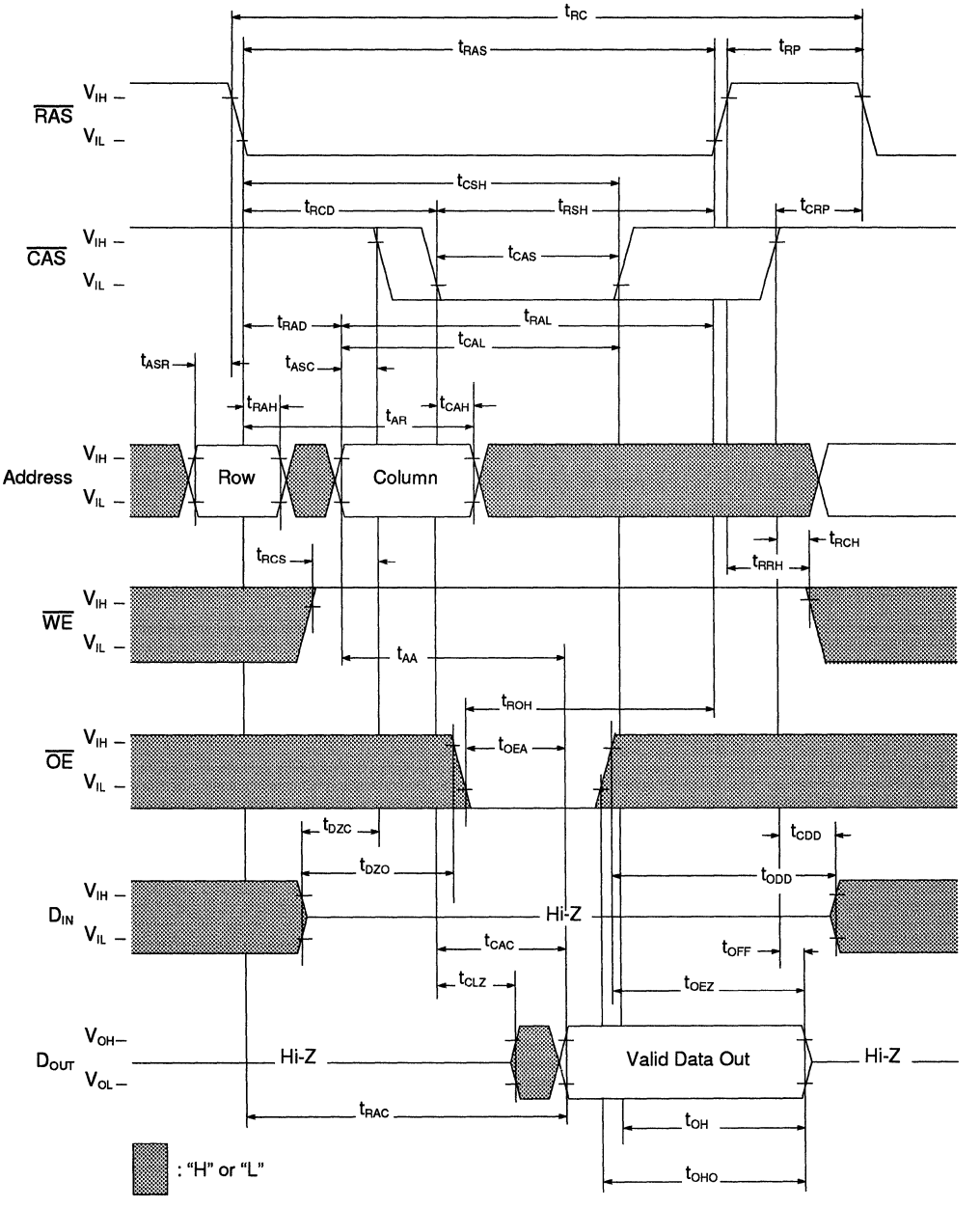
1. 8192 refreshes are required every 128ms.

Presence Detect Read Cycle

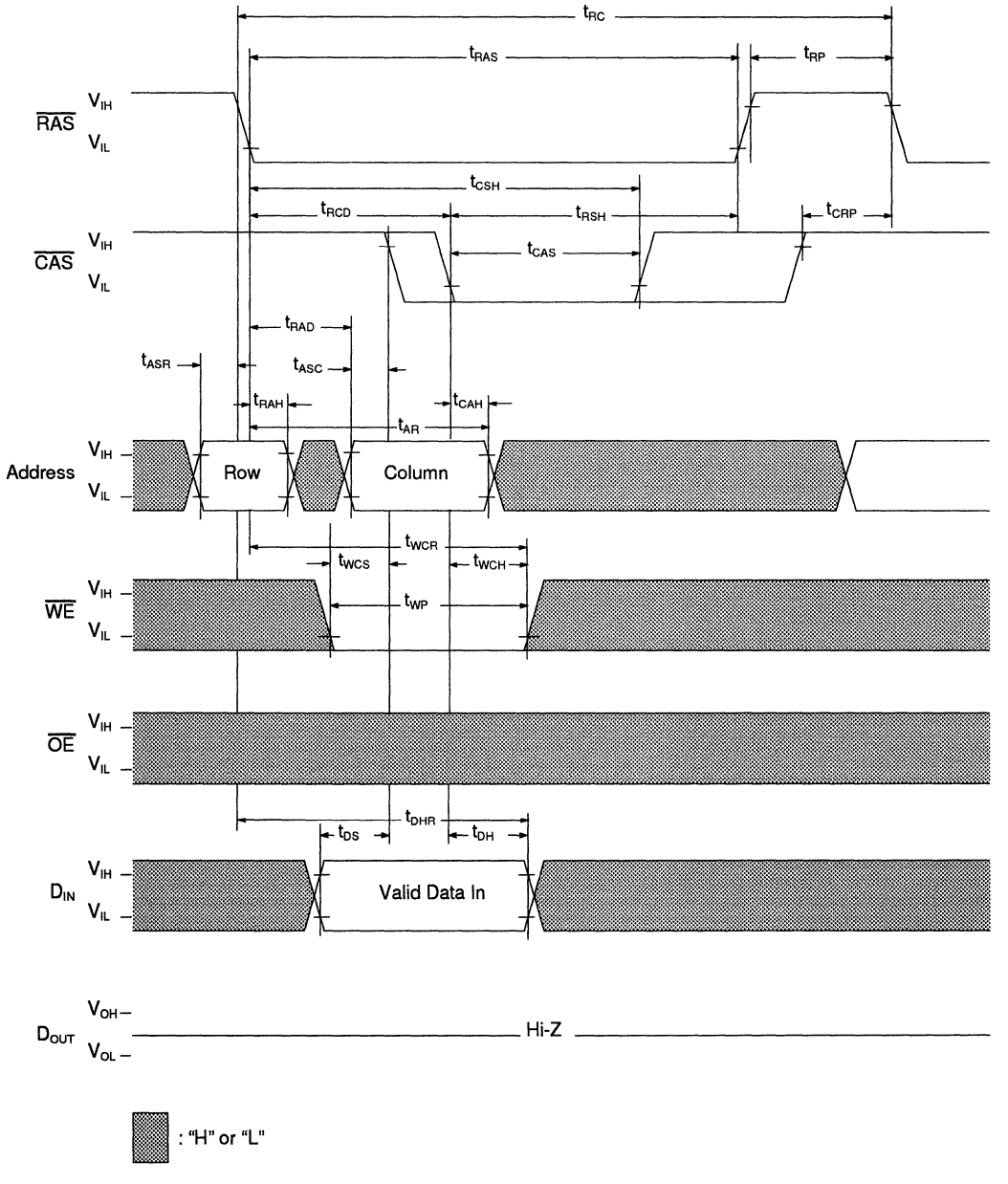
Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

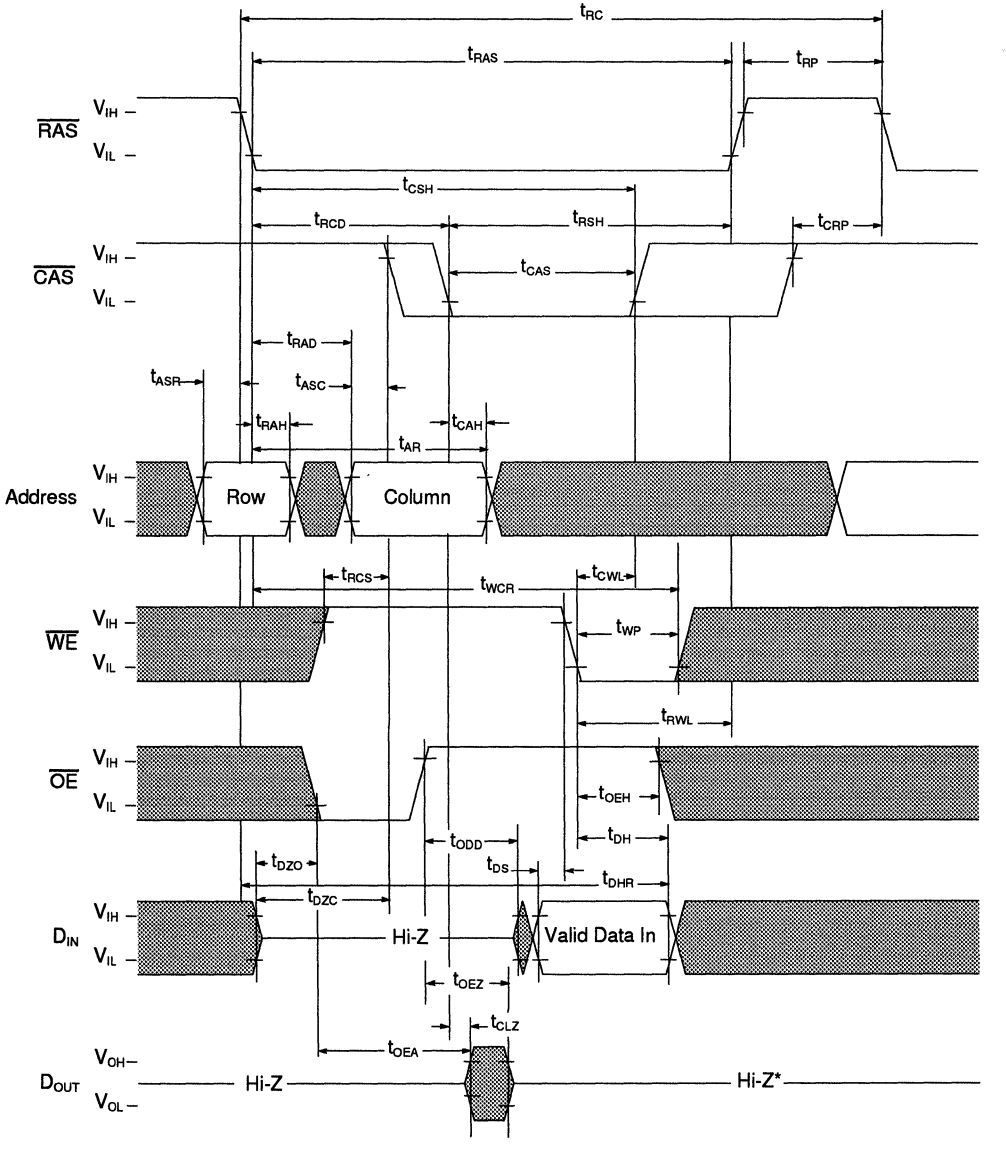
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tAR
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Valid Data Out
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

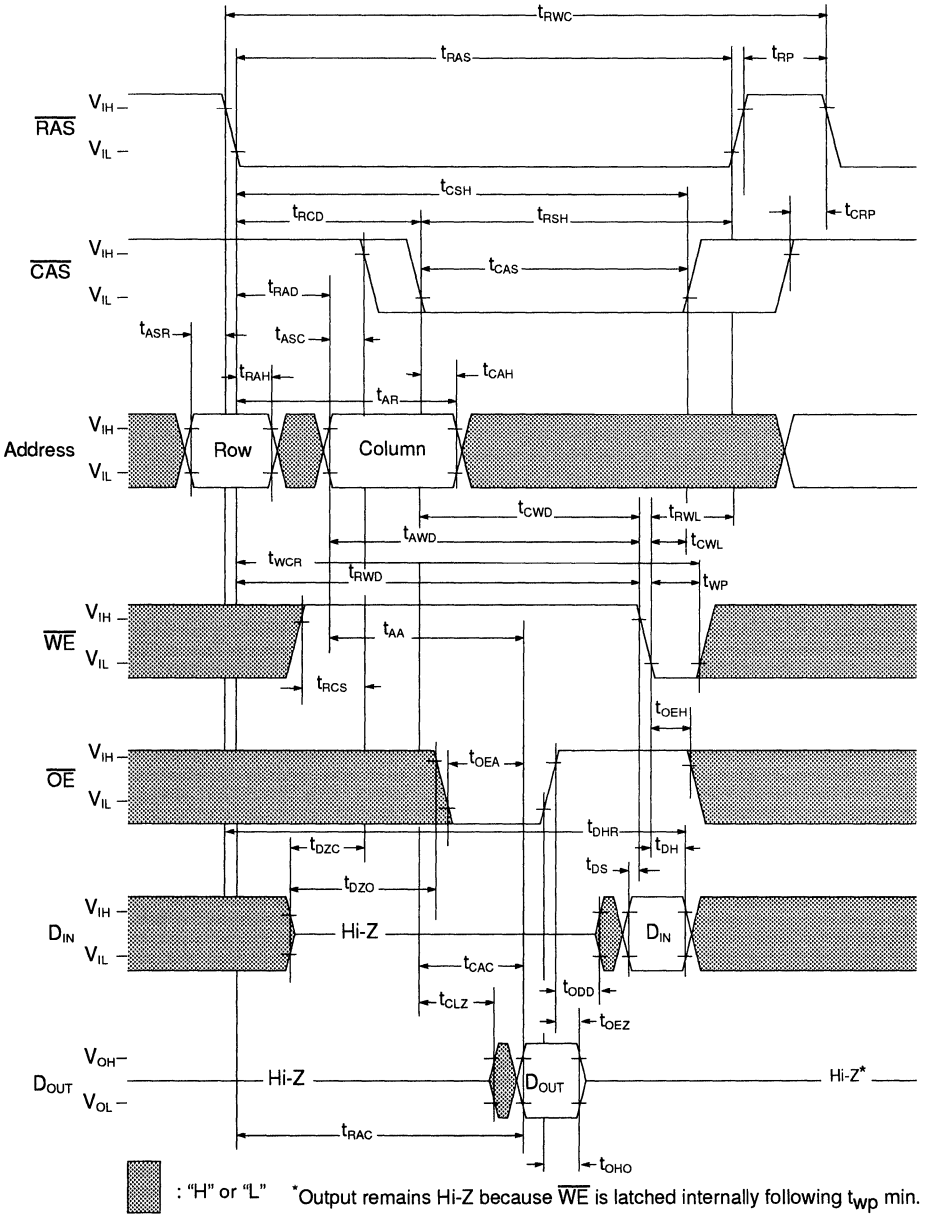


Write Cycle (Late Write)

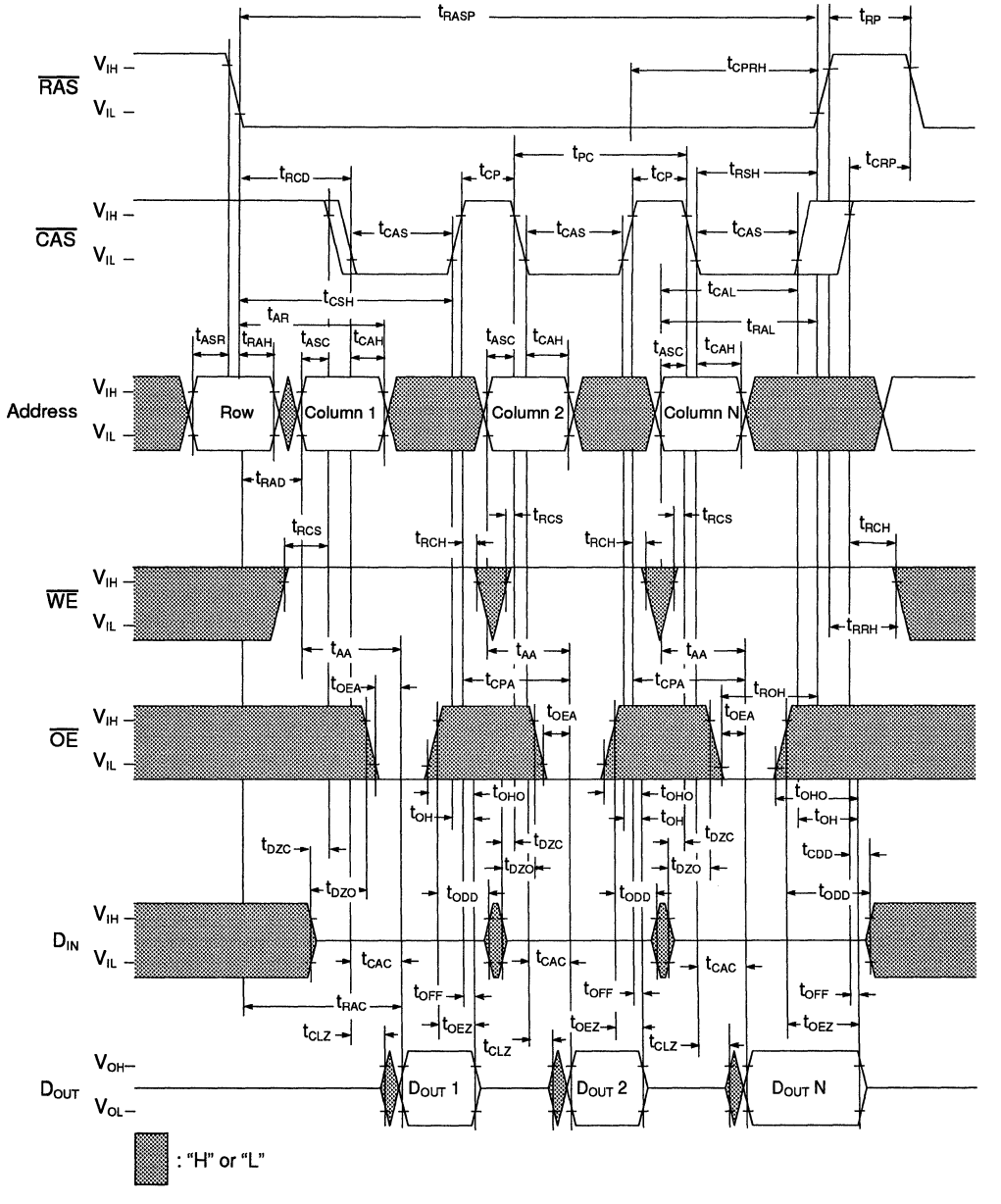


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

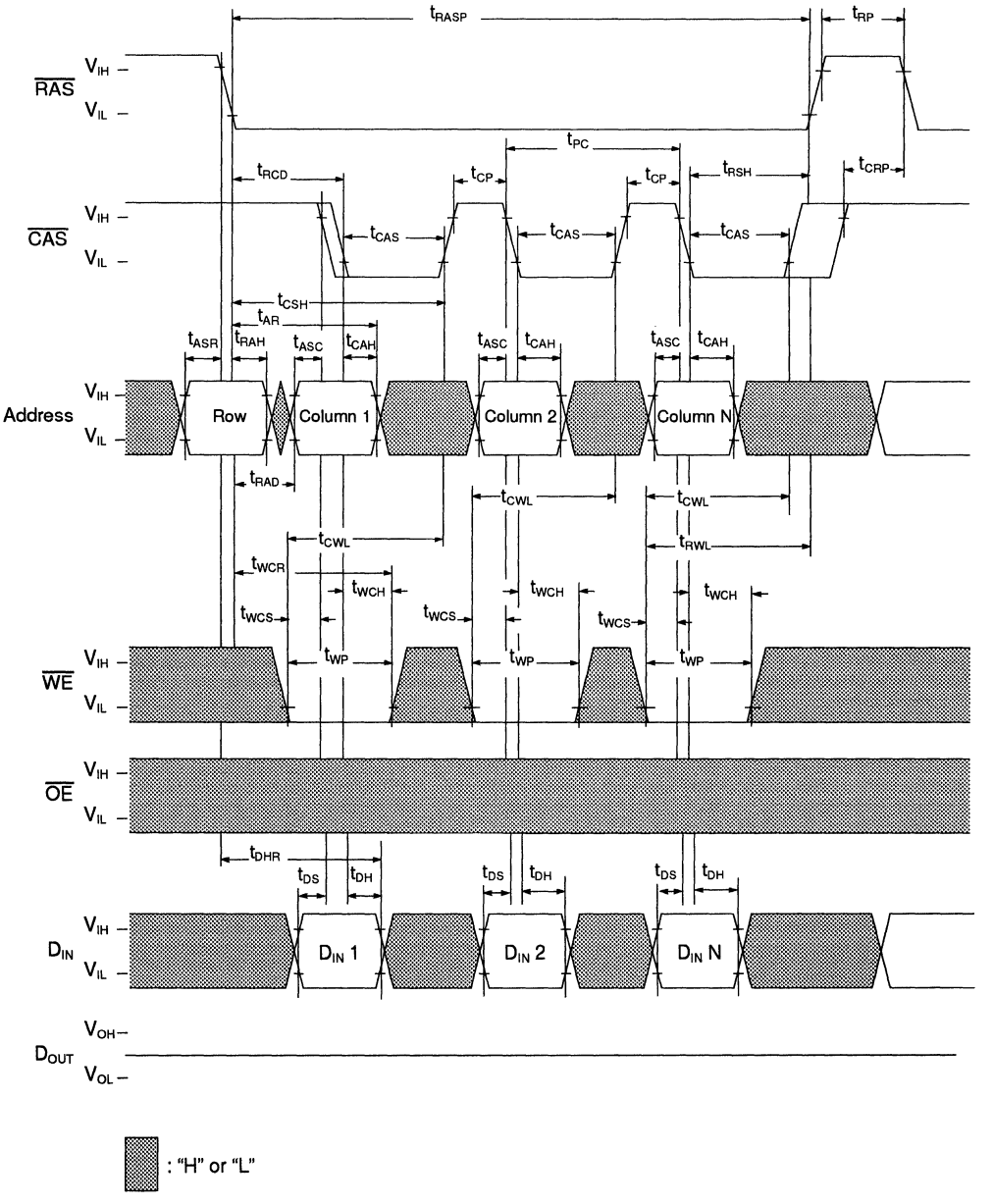
Read-Modify-Write-Cycle



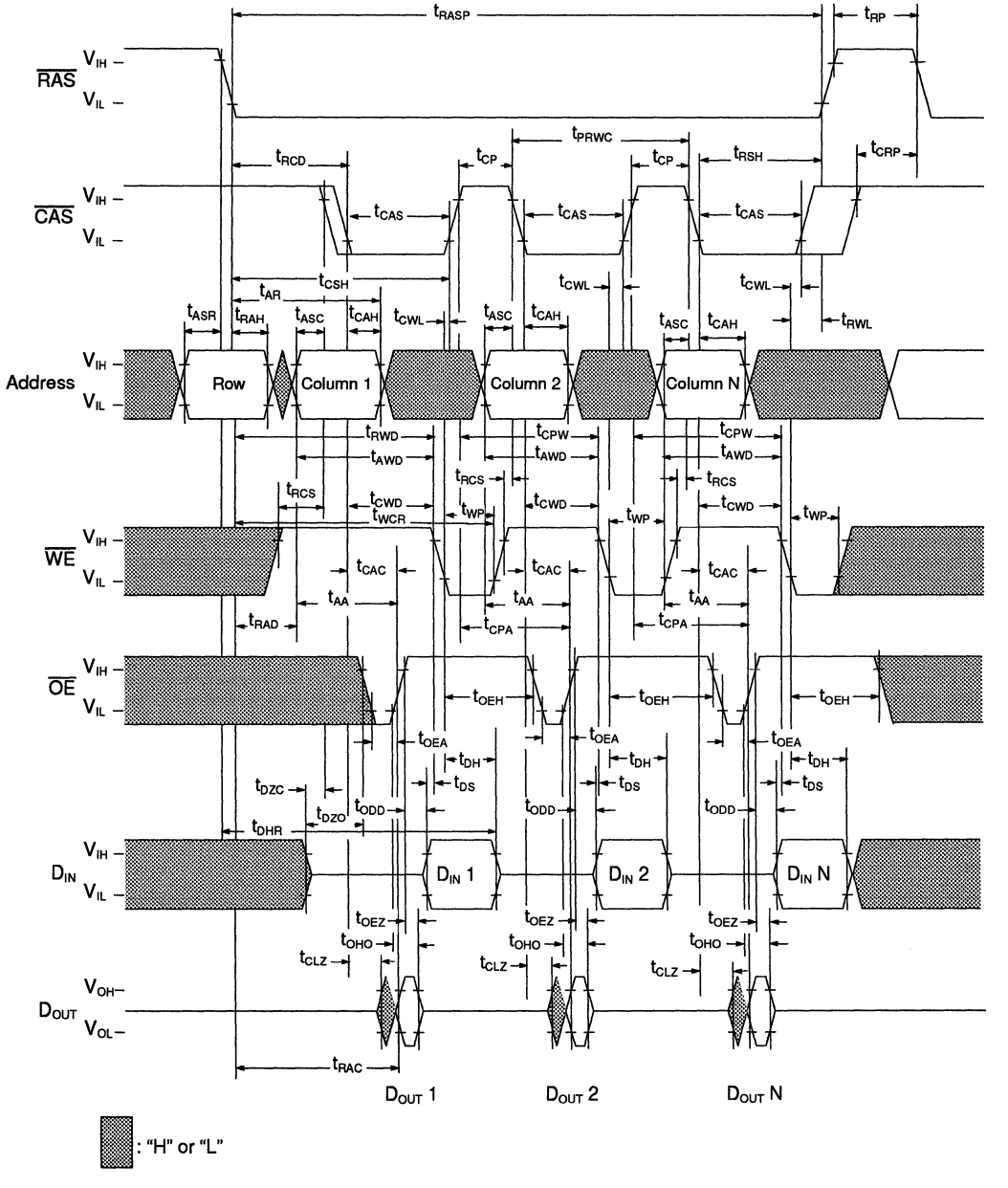
Fast Page Mode Read Cycle



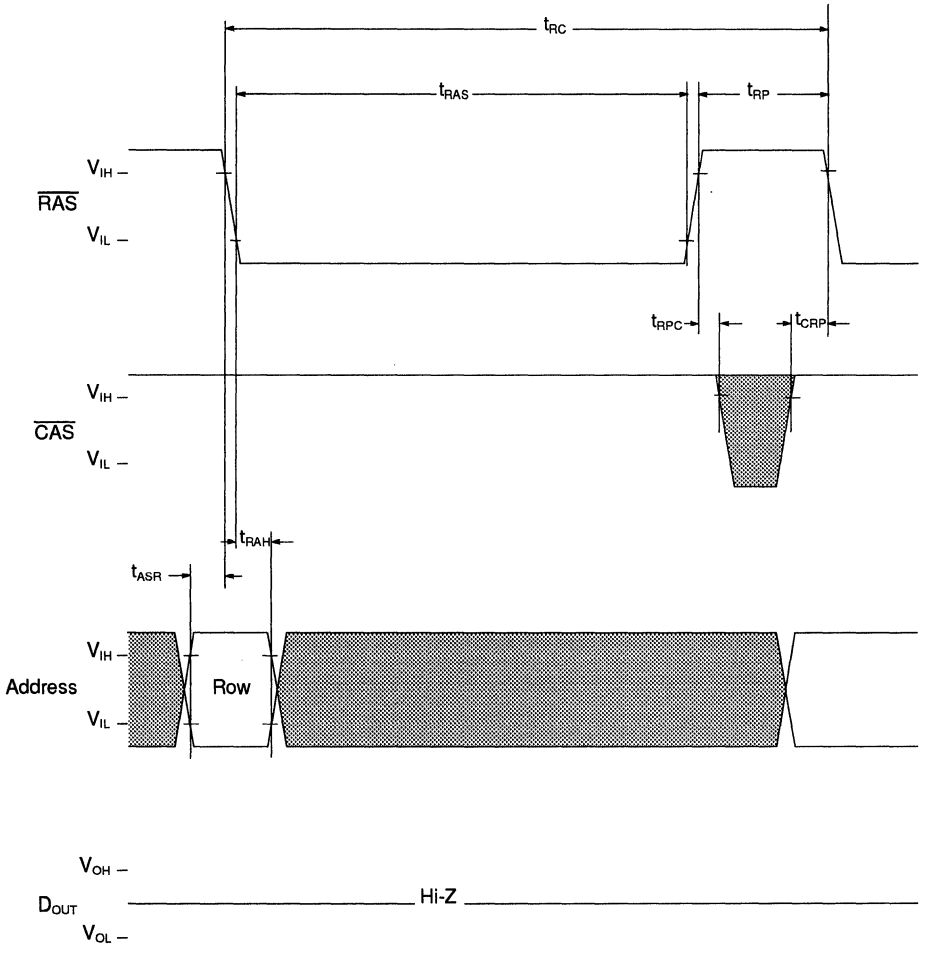
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

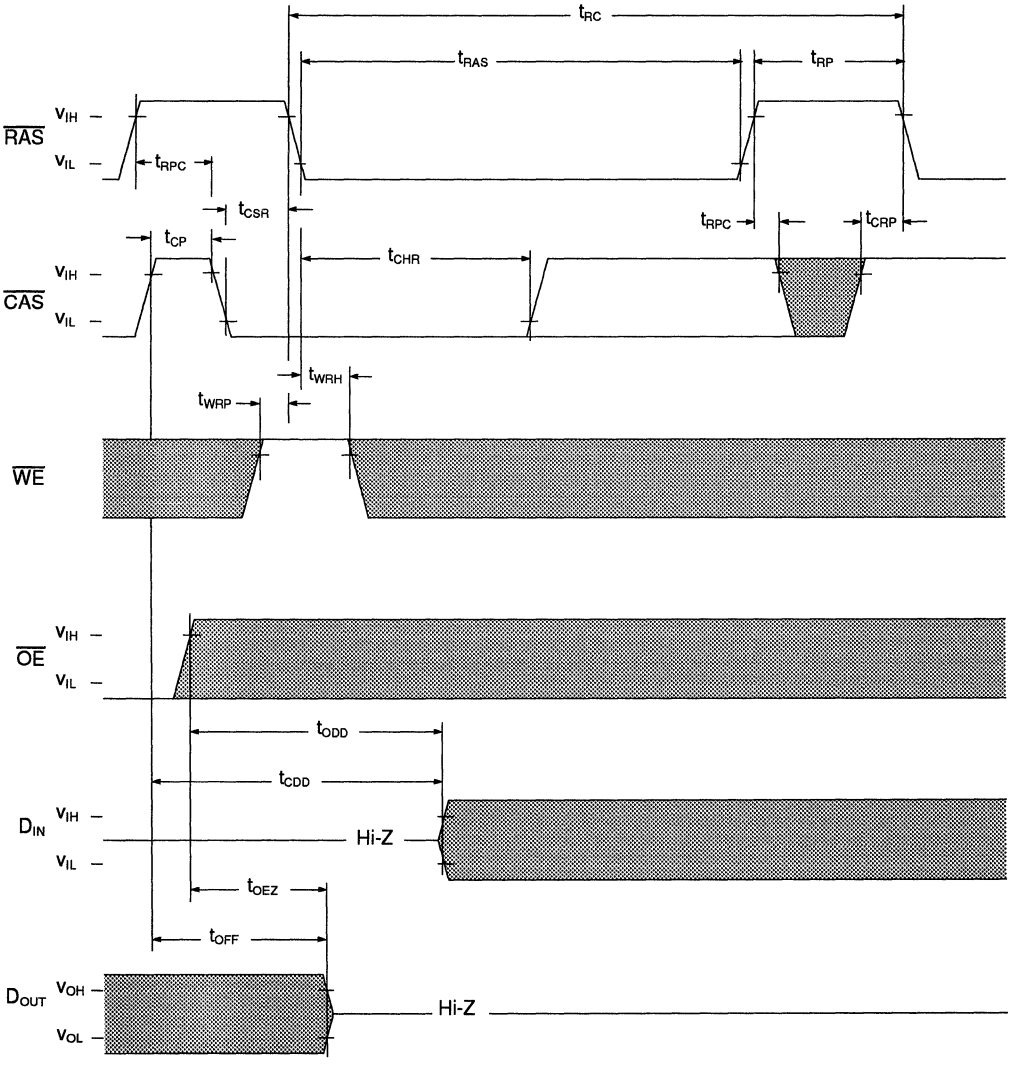


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

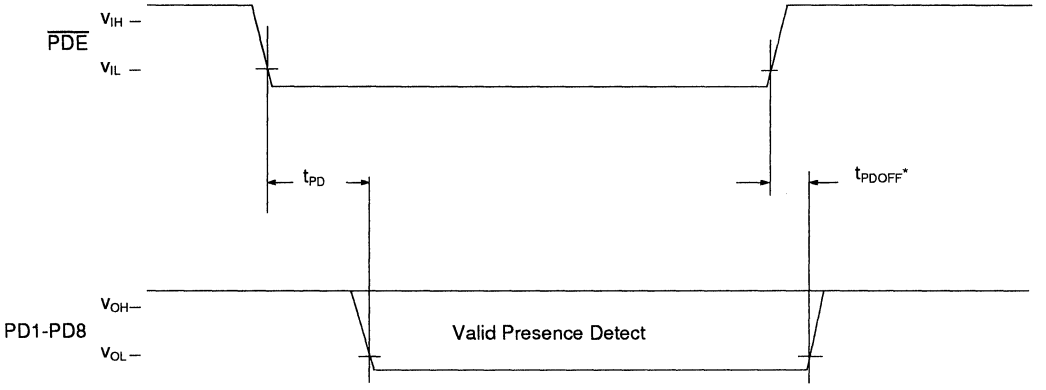
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



: "H" or "L"

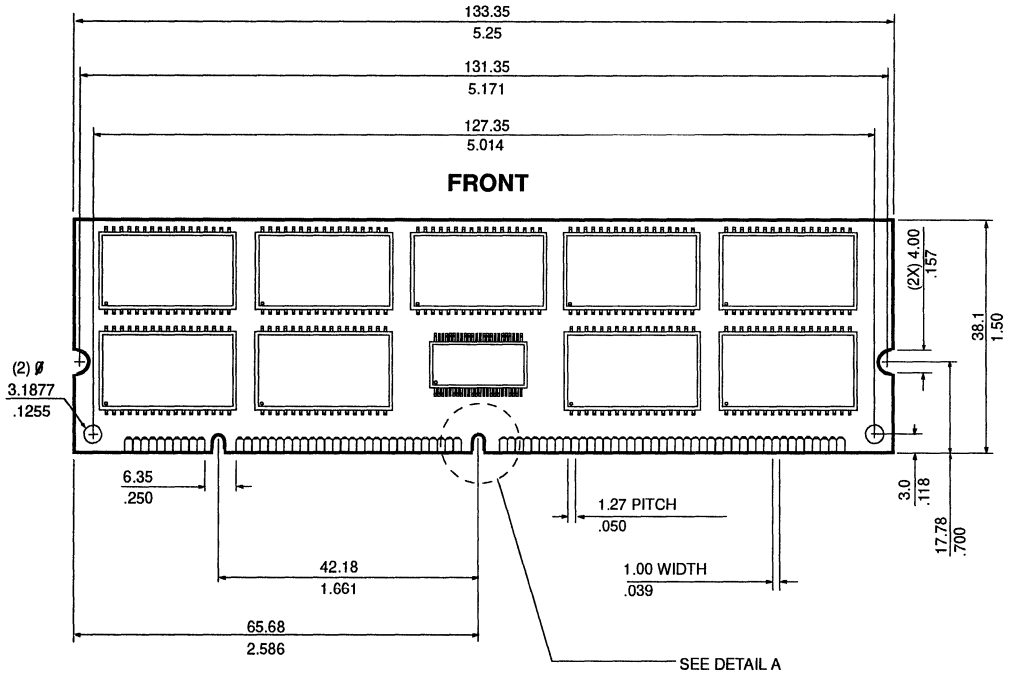
Note: Addresses are "H" or "L"

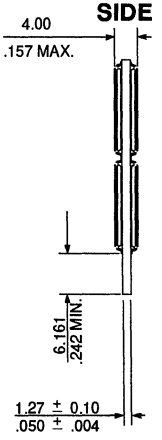
Presence Detect Read Cycle

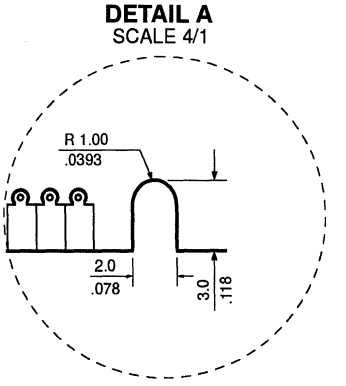


*PD pins must be pulled high at next level of assembly

Layout Drawing







NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

72 Pin SO DIMMs

1M x 32 SODIMM Module

Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns	45ns

- High Performance CMOS process
- Single 3.3, ± 0.3V or 5.0, ± 0.25V Power Supply
- Low active current consumption
- All inputs & outputs are TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 128ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au contacts

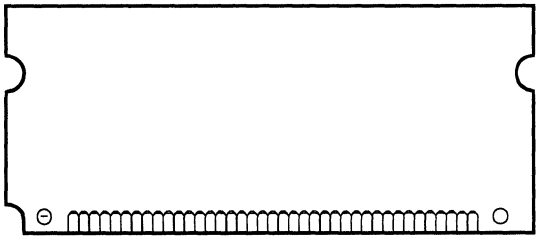
Description

The IBM11S1320BN/L are 4MB industry standard 72-pin 4-byte small outline dual in-line memory modules (SODIMM's). The module is organized as a 1Mx32 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 8 1Mx4 TSOP devices, each in a 300mil package

This assembly is intended for use in space constrained and or low power applications.

The IBM 72-Pin SODIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint. Related products include the 1Mx32 version with 12/8 addressing IBM11S1320NN/L as well as a 1Mx36 parity version IBM11S1360NN/L.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V or +5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

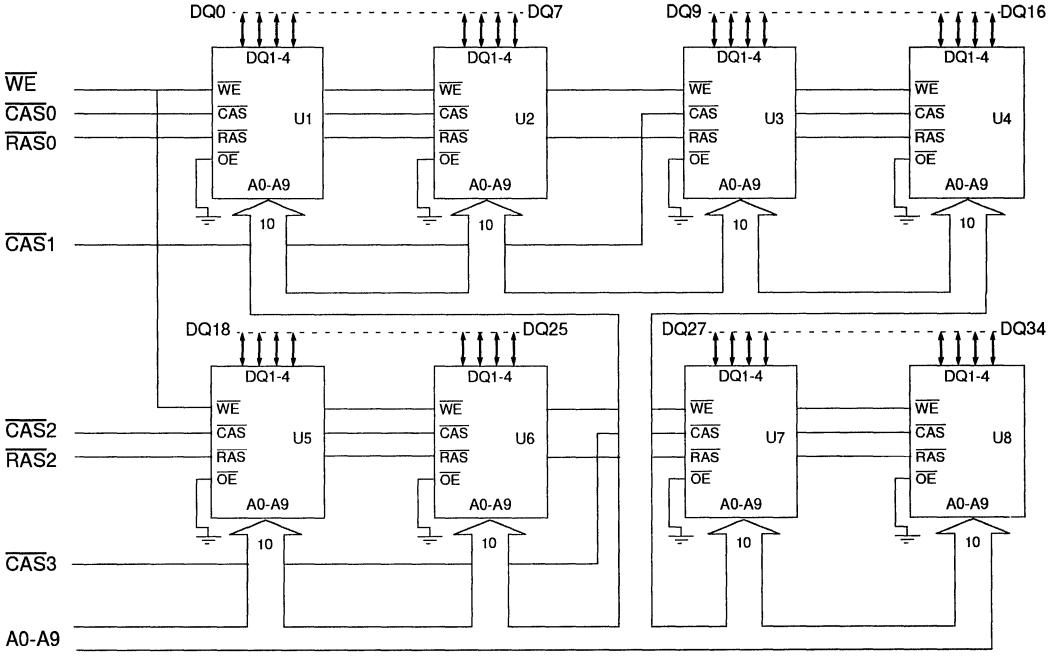
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ23	64	DQ34
5	DQ3	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ24	65	NC
6	DQ4	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ25	66	PD2
7	DQ5	19	NC	31	A8	43	$\overline{CAS1}$	55	NC	67	PD3
8	DQ6	20	NC	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{RAS2}$	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{WE}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	NC	48	NC	60	DQ30	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Power
IBM11S1320BNA-60	1M x 32	60ns	Au	2.35" x 1" x .15"	3.3V
IBM11S1320BNA-70	1M x 32	70ns	Au	2.35" x 1" x .15"	3.3V
IBM11S1320BLA-60	1M x 32	60ns	Au	2.35" x 1" x .15"	5.0V
IBM11S1320BLA-70	1M x 32	70ns	Au	2.35" x 1" x .15"	5.0V

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	V_{SS}	V_{SS}
PD3	V_{SS}	V_{SS}
PD4	NC	NC
PD5	NC	V_{SS}
PD6	NC	NC
PD7	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt	5.0 Volt		
V_{CC}	Power Supply Voltage	-0.5 to + 4.6	-1.0 to + 6.0	V	1
V_{IN}	Input Voltage	-0.7 to V_{CC} + 0.5	-1.0 to + 6.0	V	1
V_{OUT}	Output Voltage	-0.5 to V_{CC} + 0.5	-1.0 to + 6.0	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	-55 to +125	°C	1
P_D	Power Dissipation	3.75	3.75	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3 Volt			5.0 Volt			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3± 0.3V or 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	50	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	35	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	20	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	67	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V or 5.0± 0.25V)

Symbol	Parameter		3.3 Volt Min	3.3 Volt Max	5.0 Volt Min	5.0 Volt Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	760		960	mA	1, 2, 3
		-70	—	640		800		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	16		16	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	760		960	mA	1, 3
		-70	—	640		800		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	520		880	mA	1, 2, 3
		-70	—	520		800		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	1.6			mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	760		960	mA	1, 3
		-70	—	640		800		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	-40	+40	µA	
		$\overline{CAS}$	-20	+20	-20	+20		
		All others	-80	+80	-80	+80		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	52	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	—	15	35	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

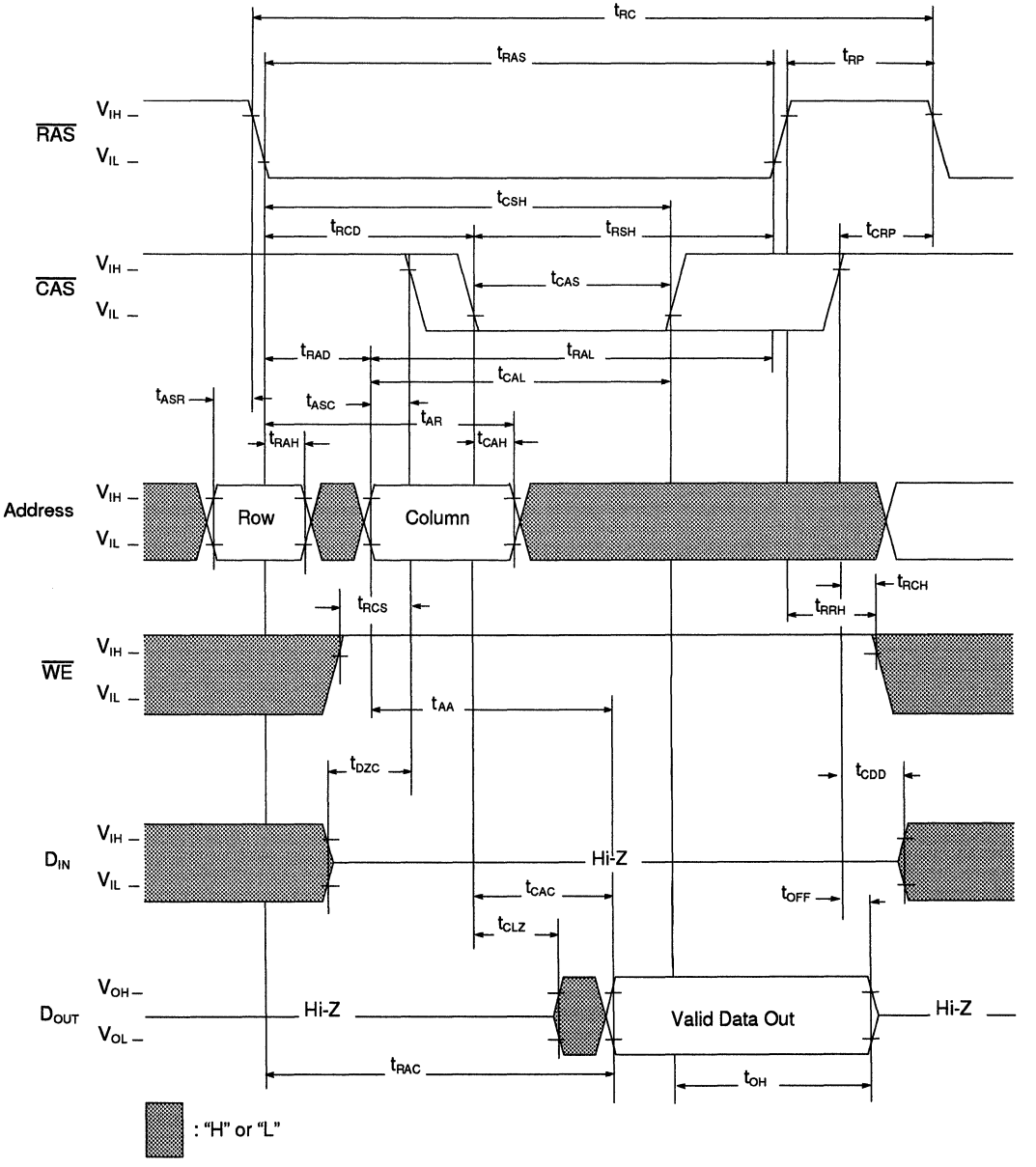
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

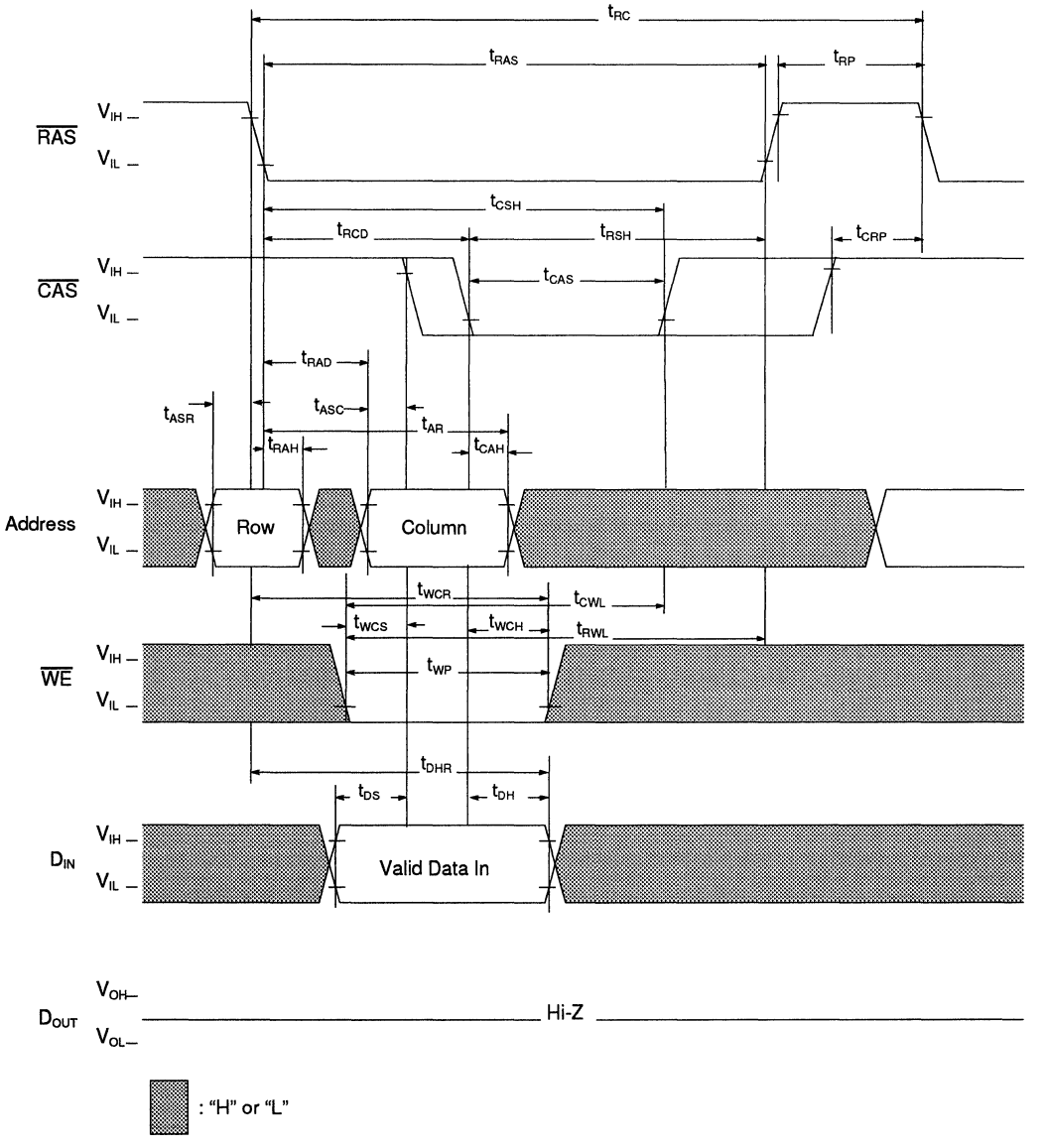
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	128	—	128	ms	1

1. 1024 refreshes are required every 128ms.

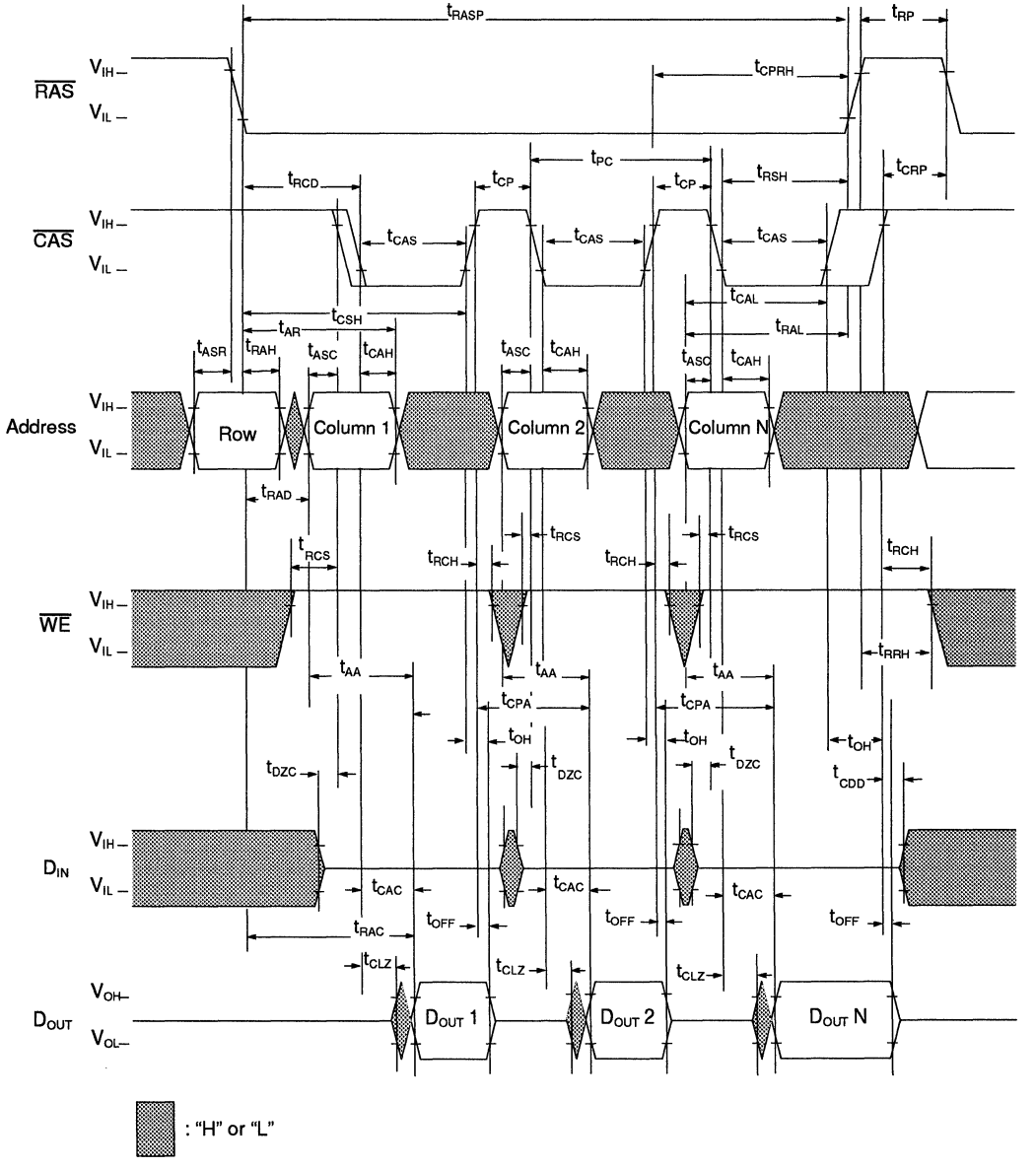
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRRH
tRCH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

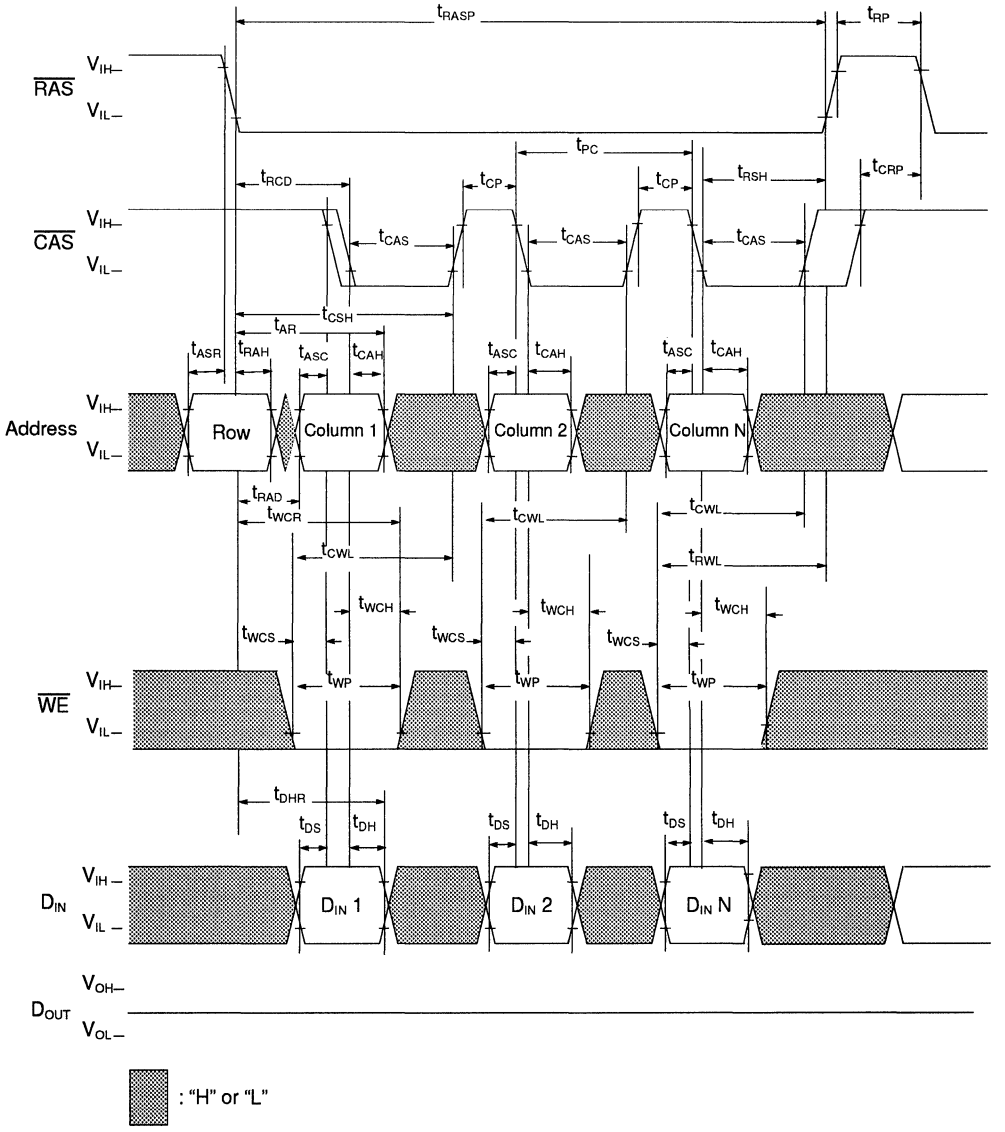
Write Cycle (Early Write)



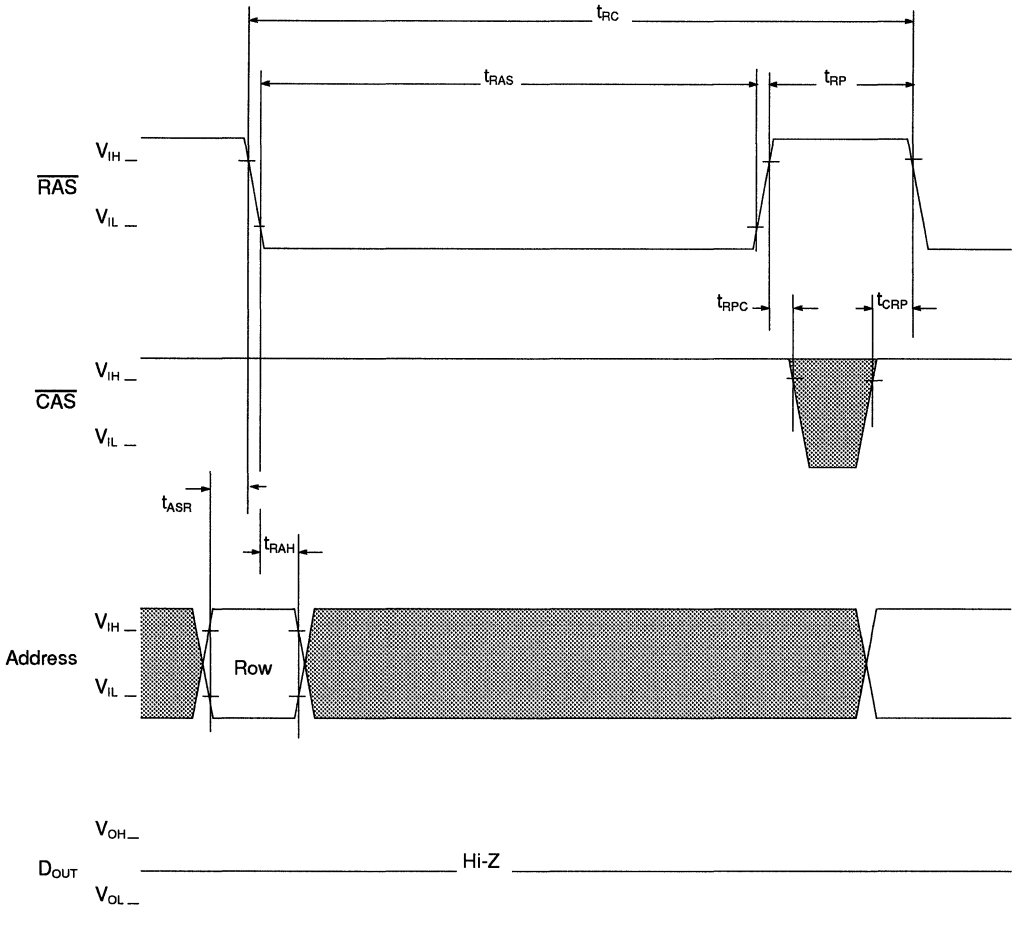
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



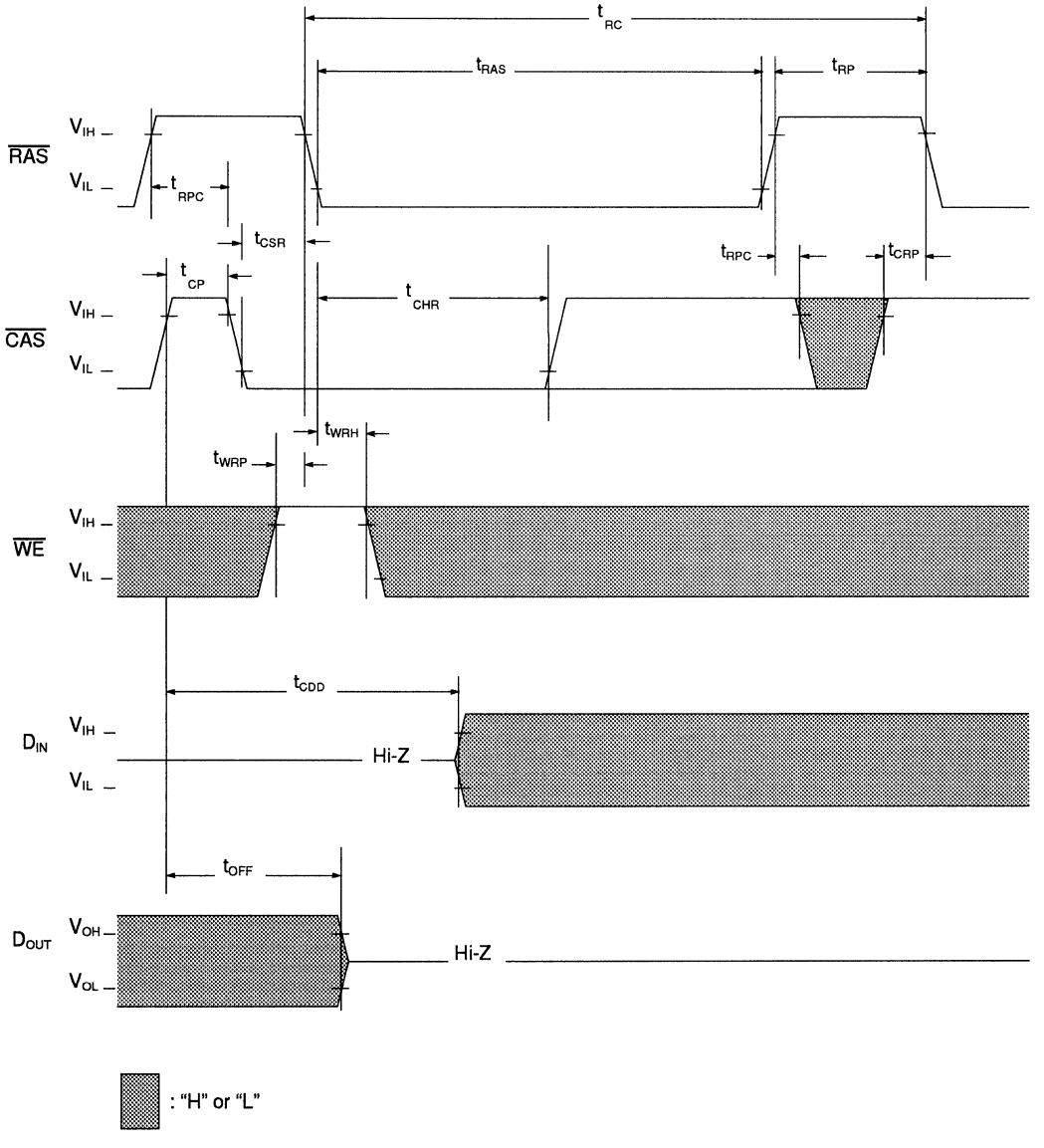
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

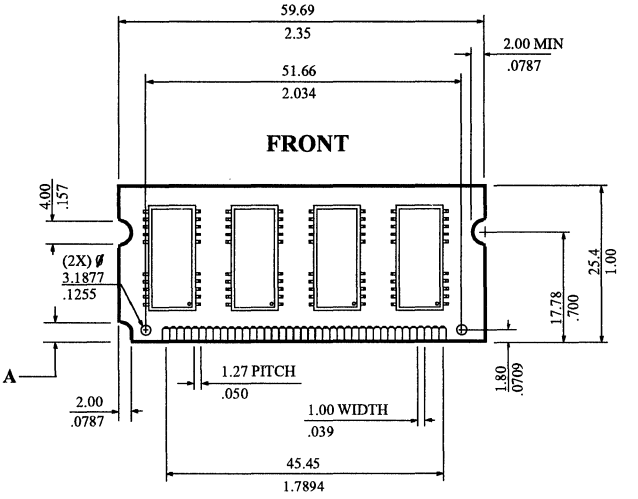
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

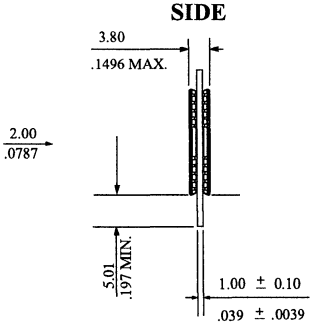


Note: Addresses are "H" or "L"

Layout Drawing



A =	3.3V	5.0V
	3.175 / .125	6.35 / .246



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

1M x 32 SODIMM Module

Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Single 3.3, ± 0.3V or 5.0, ± 0.25V Power Supply
- Low active current consumption
- All inputs & outputs are TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 4096 refresh cycles distributed across 256ms
- 12/8 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au contacts

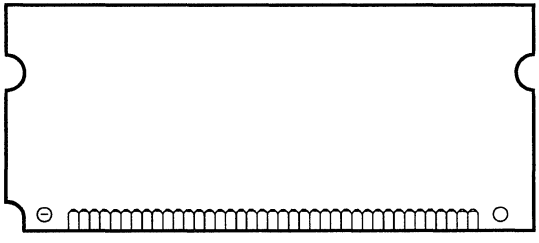
Description

The IBM11S1320NN/L are 4MB industry standard 72-pin 4-byte small outline dual in-line memory modules (SODIMM's). The module is organized as a 1Mx32 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 2 1Mx16 TSOP devices, each in a 400mil package

This assembly is intended for use in space constrained and or low power applications. It utilizes 12/8 address 16m bit technology to further reduce power consumption.

The IBM 72-Pin SODIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint. Related products include the 1Mx32 version with 10/10 addressing IBM11S1320BN/L as well as a 1Mx36 parity version IBM11S1360NN/L.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A11	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V or +5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

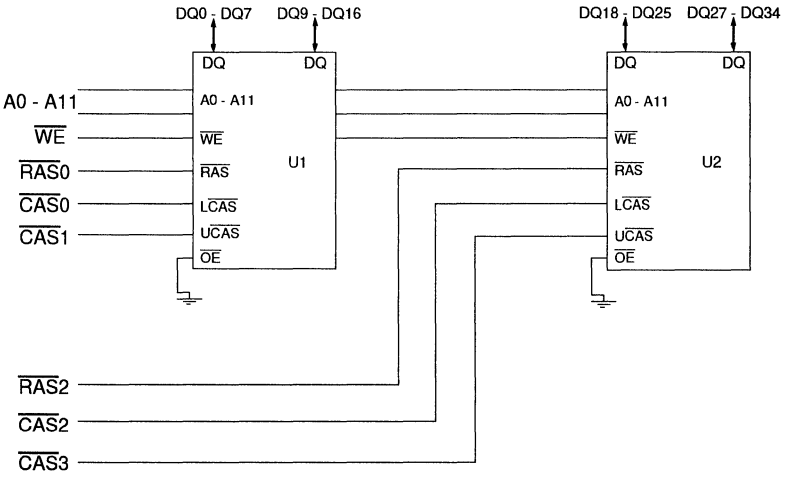
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ23	64	DQ34
5	DQ3	17	A5	29	A11	41	$\overline{CAS2}$	53	DQ24	65	NC
6	DQ4	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ25	66	PD2
7	DQ5	19	A10	31	A8	43	$\overline{CAS1}$	55	NC	67	PD3
8	DQ6	20	NC	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{RAS2}$	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{WE}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	NC	48	NC	60	DQ30	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Power
IBM11S1320NNA-60	1M x 32	60ns	Au	2.35" x 1" x .0965"	3.3V
IBM11S1320NNA-70	1M x 32	70ns	Au	2.35" x 1" x .0965"	3.3V
IBM11S1320NLA-60	1M x 32	60ns	Au	2.35" x 1" x .0965"	5.0V
IBM11S1320NLA-70	1M x 32	70ns	Au	2.35" x 1" x .0965"	5.0V

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	V_{SS}	V_{SS}
PD3	NC	NC
PD4	NC	NC
PD5	NC	V_{SS}
PD6	NC	NC
PD7	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt	5.0 Volt		
V_{CC}	Power Supply Voltage	-0.5 to + 4.6	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.7 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	-55 to +125	°C	1
P_D	Power Dissipation	0.6	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3 Volt			5.0 Volt			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3± 0.3V or 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	28	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	16	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	28	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	16	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V or 5.0± 0.25V)

Symbol	Parameter		3.3 Volt		5.0 Volt		Units	Notes
			Min	Max	Min	Max		
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	190	—	190	mA	1, 2, 3
		-70	—	170	—	170		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	4	—	4	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	190	—	190	mA	1, 3
		-70	—	170	—	170		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	150	—	150	mA	1, 2, 3
		-70	—	130	—	130		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	0.4	—	0.4	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	190	—	190	mA	1, 3
		-70	—	170	—	170		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-10	+10	-10	+10	µA	
		$\overline{CAS}$	-10	+10	-10	+10		
		All others	-20	+20	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

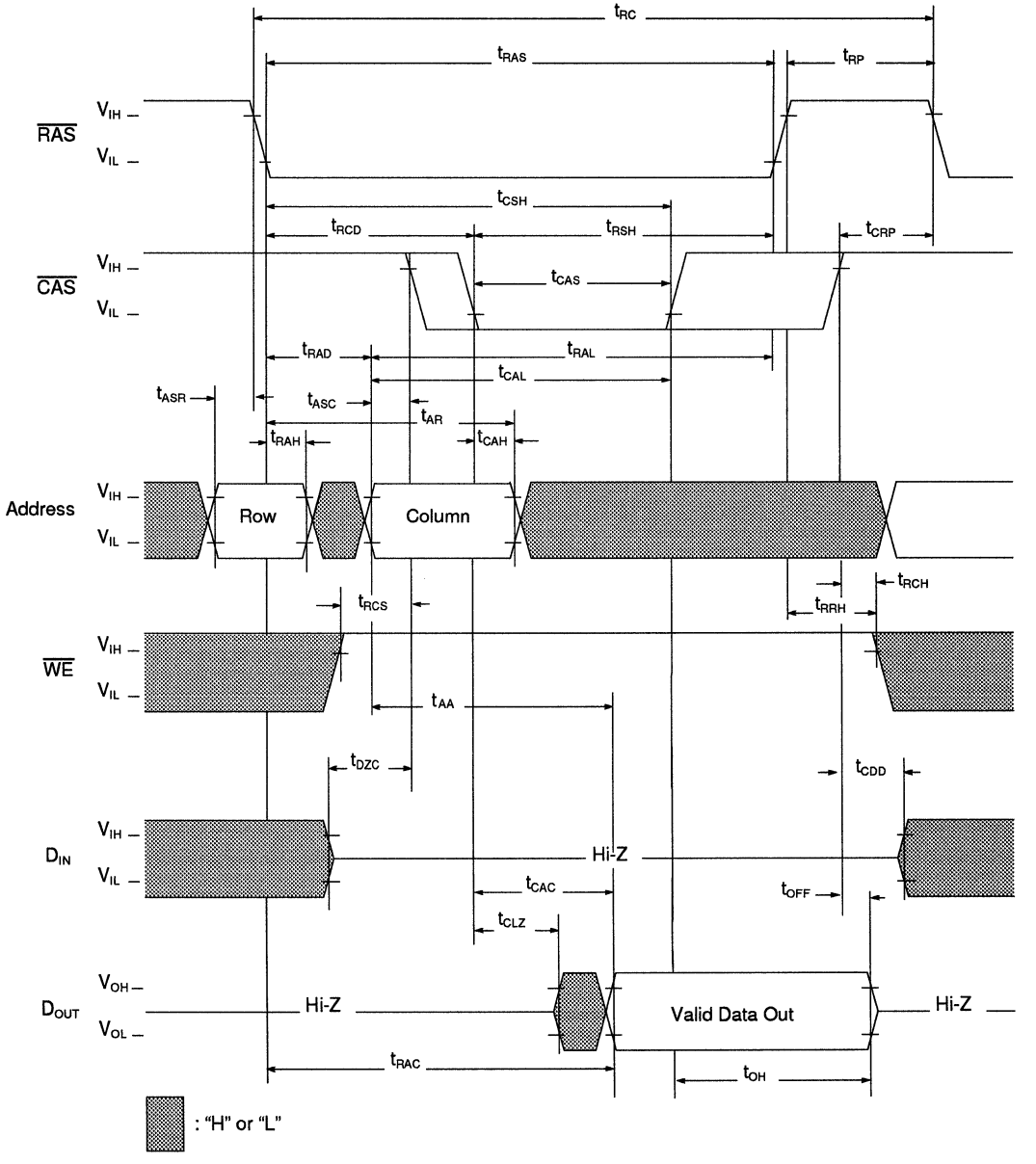
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

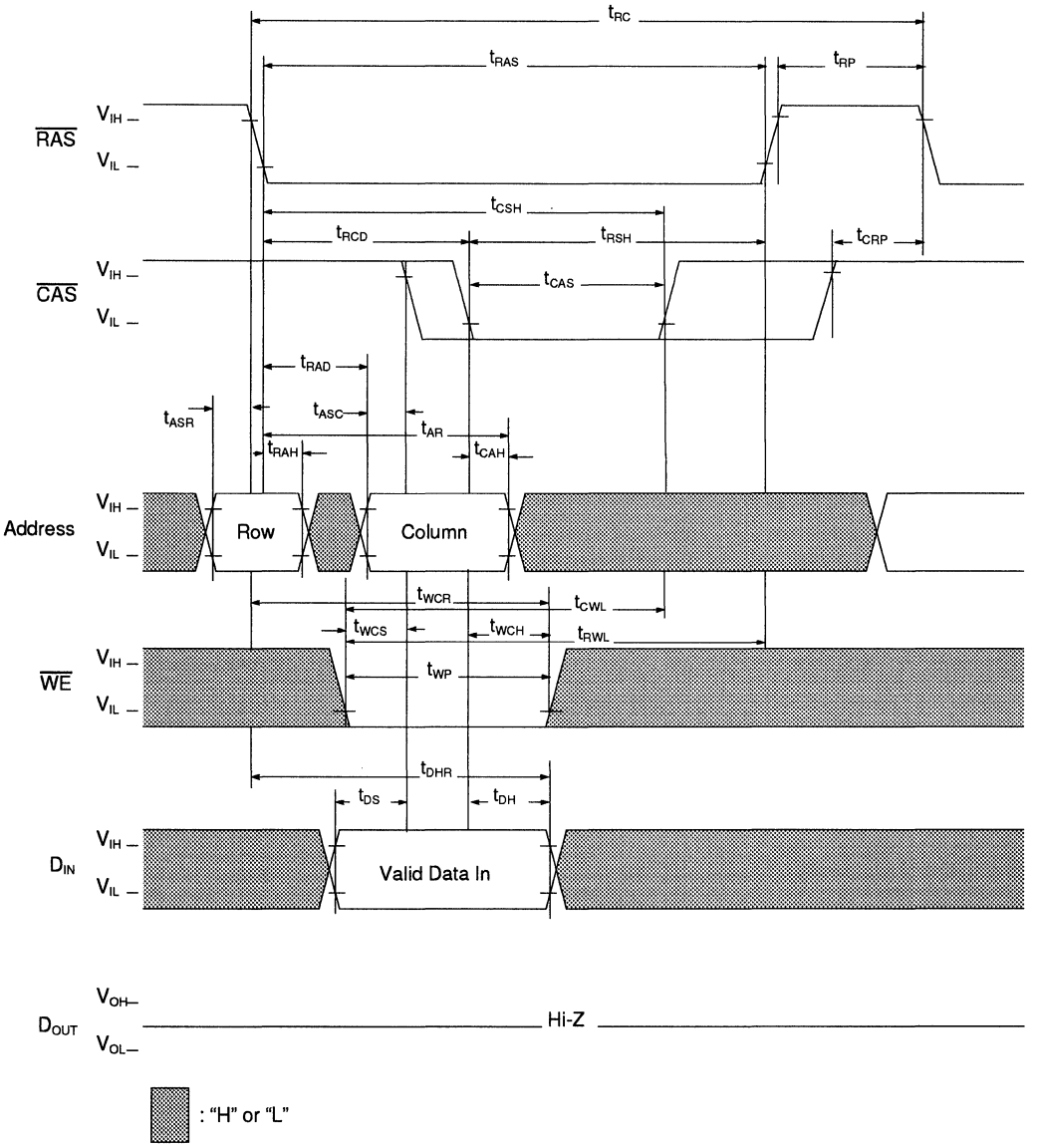
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	256	—	256	ms	1

1. 4096 refreshes are required every 256ms.

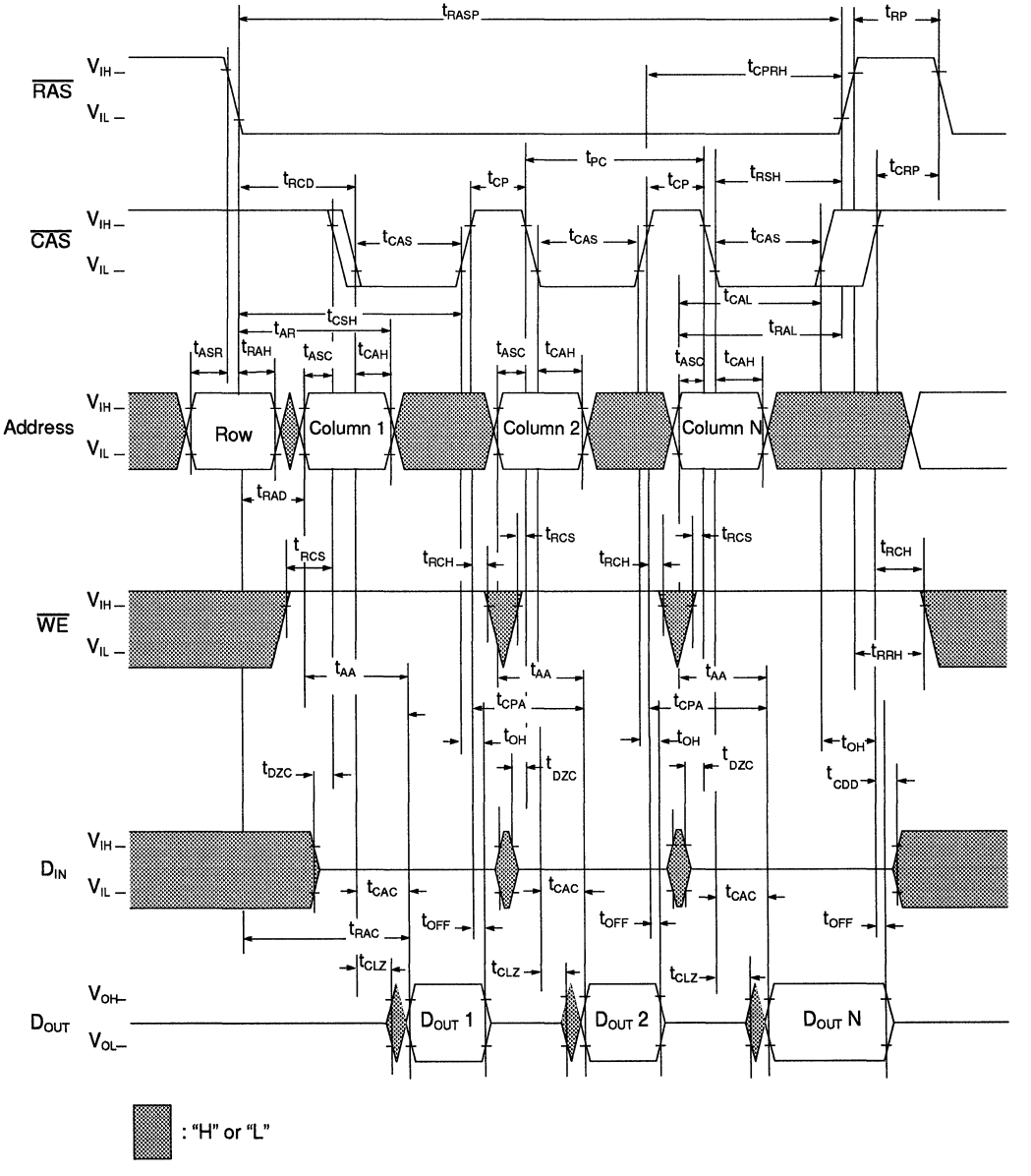
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

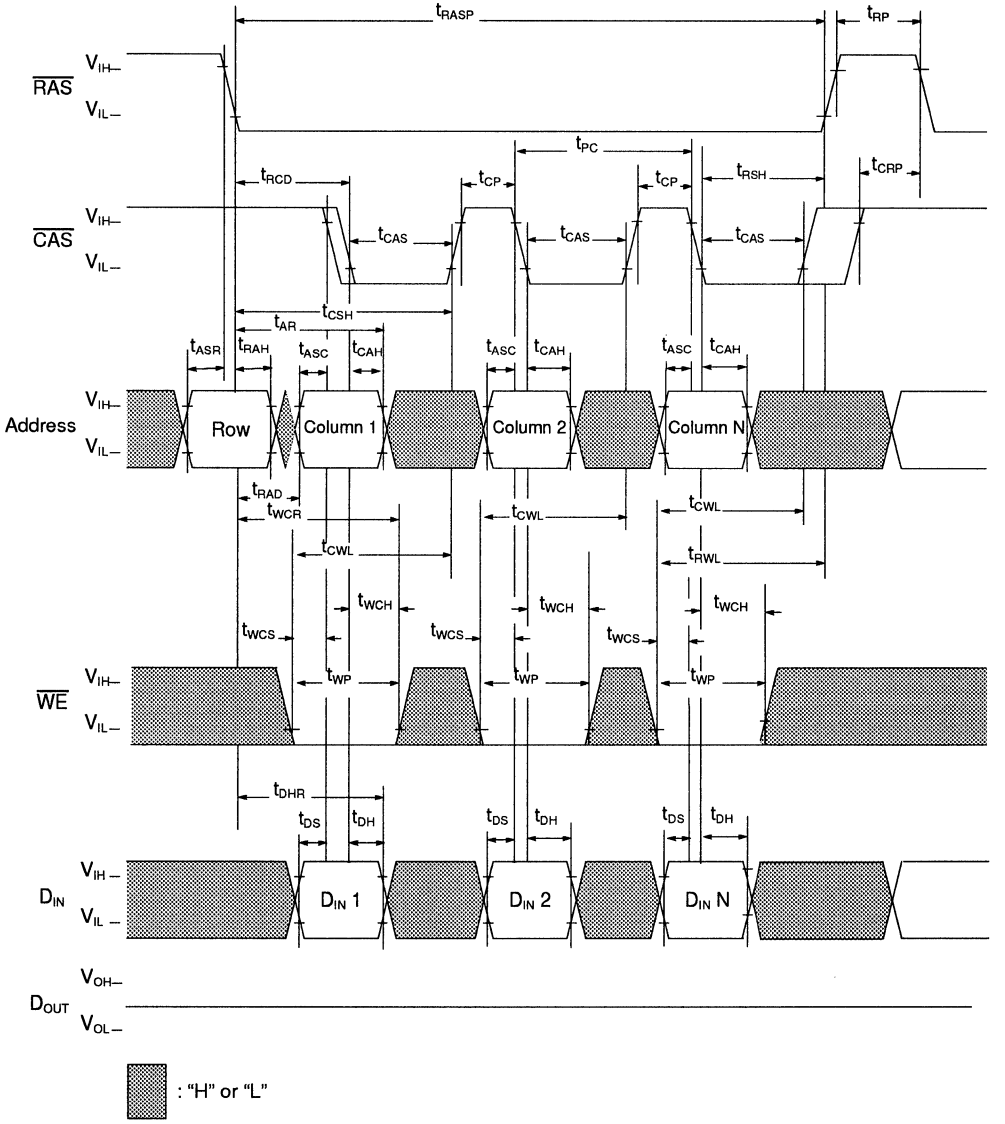
Write Cycle (Early Write)



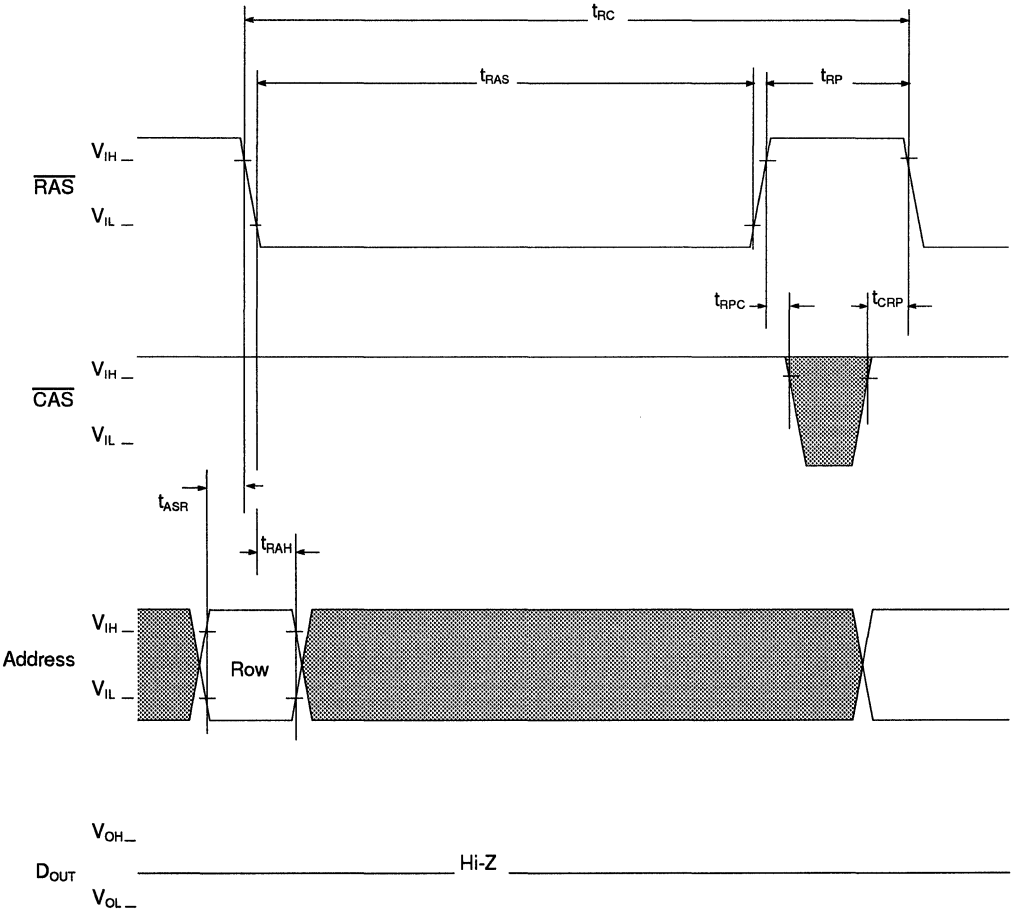
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

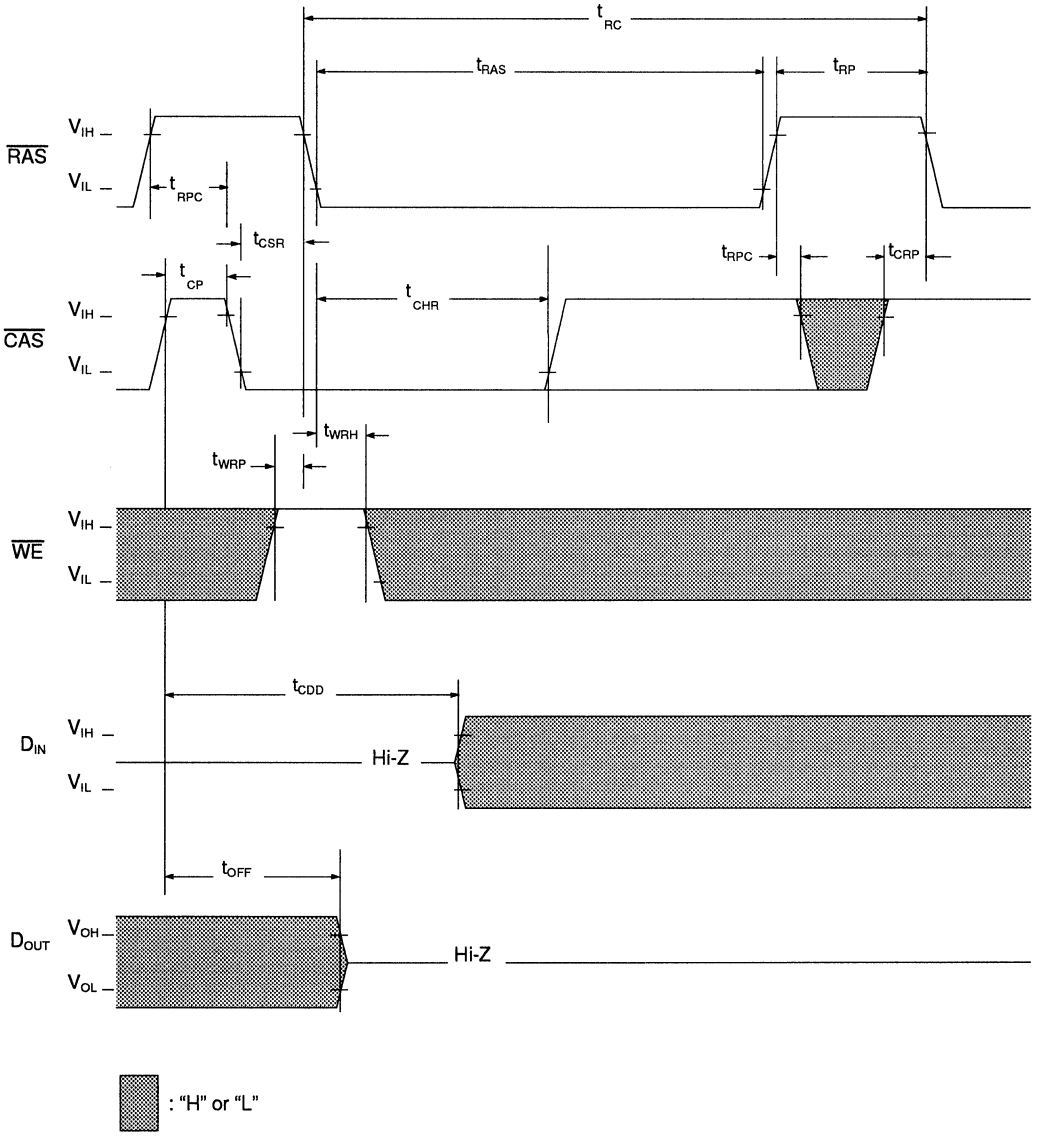


$\overline{RAS}$ Only Refresh Cycle



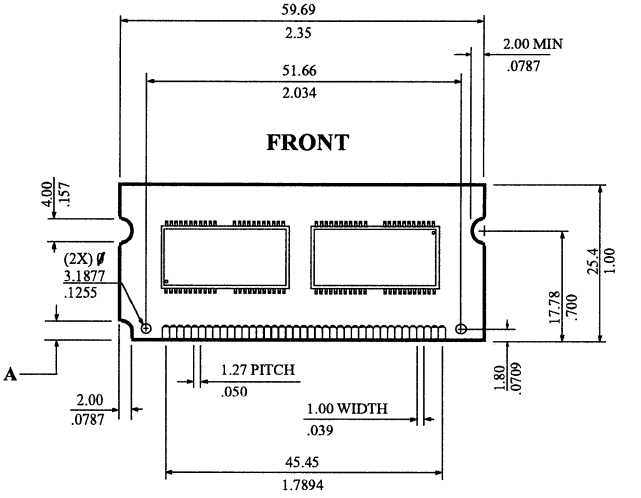
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

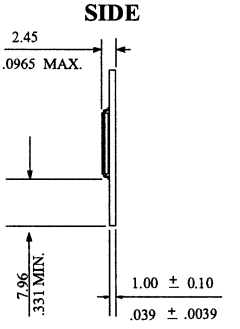


Note: Addresses are "H" or "L"

Layout Drawing



A =	3.3V	5.0V
	3.175	6.35
	.125	.246



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 32 SODIMM Module

Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Single 3.3, ± 0.3V or 5.0, ± 0.25V Power Supply
- Low active current consumption
- All inputs & outputs are TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 2048 refresh cycles distributed across 256ms
- 11/10 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au contacts

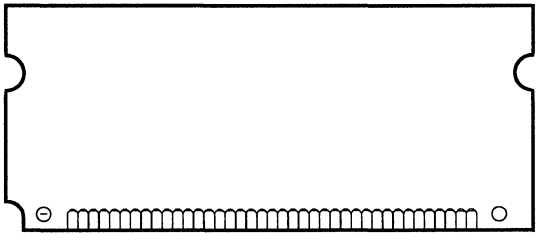
Description

The IBM11S2320HN/L are 8MB 72-pin 4-byte small outline dual in-line memory modules (SODIMM's). The module is organized as a 2Mx32 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 4 2Mx8 TSOP devices, each in a 400mil package

This assembly is intended for use in space constrained and or low power applications.

The IBM 72-Pin SODIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint. Related products include the 2Mx32 version with 12/8 addressing IBM11S2320NN/L as well as a 2Mx36 parity version IBM11S2360NN/L.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V or +5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

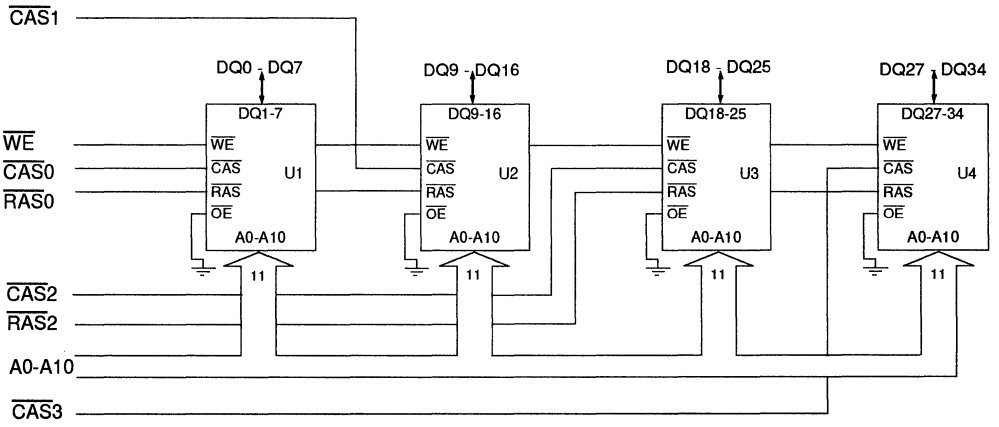
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ23	64	DQ34
5	DQ3	17	A5	29	A11	41	$\overline{CAS2}$	53	DQ24	65	NC
6	DQ4	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ25	66	PD2
7	DQ5	19	A10	31	A8	43	$\overline{CAS1}$	55	NC	67	PD3
8	DQ6	20	NC	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{RAS2}$	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{WE}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	NC	48	NC	60	DQ30	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Power
IBM11S2320HNA-60	2M x 32	60ns	Au	2.35" x 1" x .083"	3.3V
IBM11S2320HNA-70	2M x 32	70ns	Au	2.35" x 1" x .083"	3.3V
IBM11S2320HLA-60	2M x 32	60ns	Au	2.35" x 1" x .083"	5.0V
IBM11S2320HLA-70	2M x 32	70ns	Au	2.35" x 1" x .083"	5.0V

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V_{SS}	V_{SS}
PD2	NC	NC
PD3	V_{SS}	V_{SS}
PD4	NC	NC
PD5	NC	V_{SS}
PD6	NC	NC
PD7	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt	5.0 Volt		
V_{CC}	Power Supply Voltage	-0.5 to + 4.6	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.7 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	-55 to +125	°C	1
P_D	Power Dissipation	0.6	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3 Volt			5.0 Volt			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3± 0.3V or 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	38	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	24	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	14	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	40	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V or 5.0± 0.25V)

Symbol	Parameter		3.3 Volt Min	3.3 Volt Max	5.0 Volt Min	5.0 Volt Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	480	—	480	mA	1, 2, 3
		-70	—	400	—	400		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	8	—	8	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	480	—	480	mA	1, 3
		-70	—	400	—	400		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	300	—	300	mA	1, 2, 3
		-70	—	260	—	260		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	0.8	—	0.8	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	480	—	480	mA	1, 3
		-70	—	400	—	400		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-10	+10	-10	+10	µA	
		$\overline{CAS}$	-20	+20	-20	+20		
		All others	-40	+40	-40	+40		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

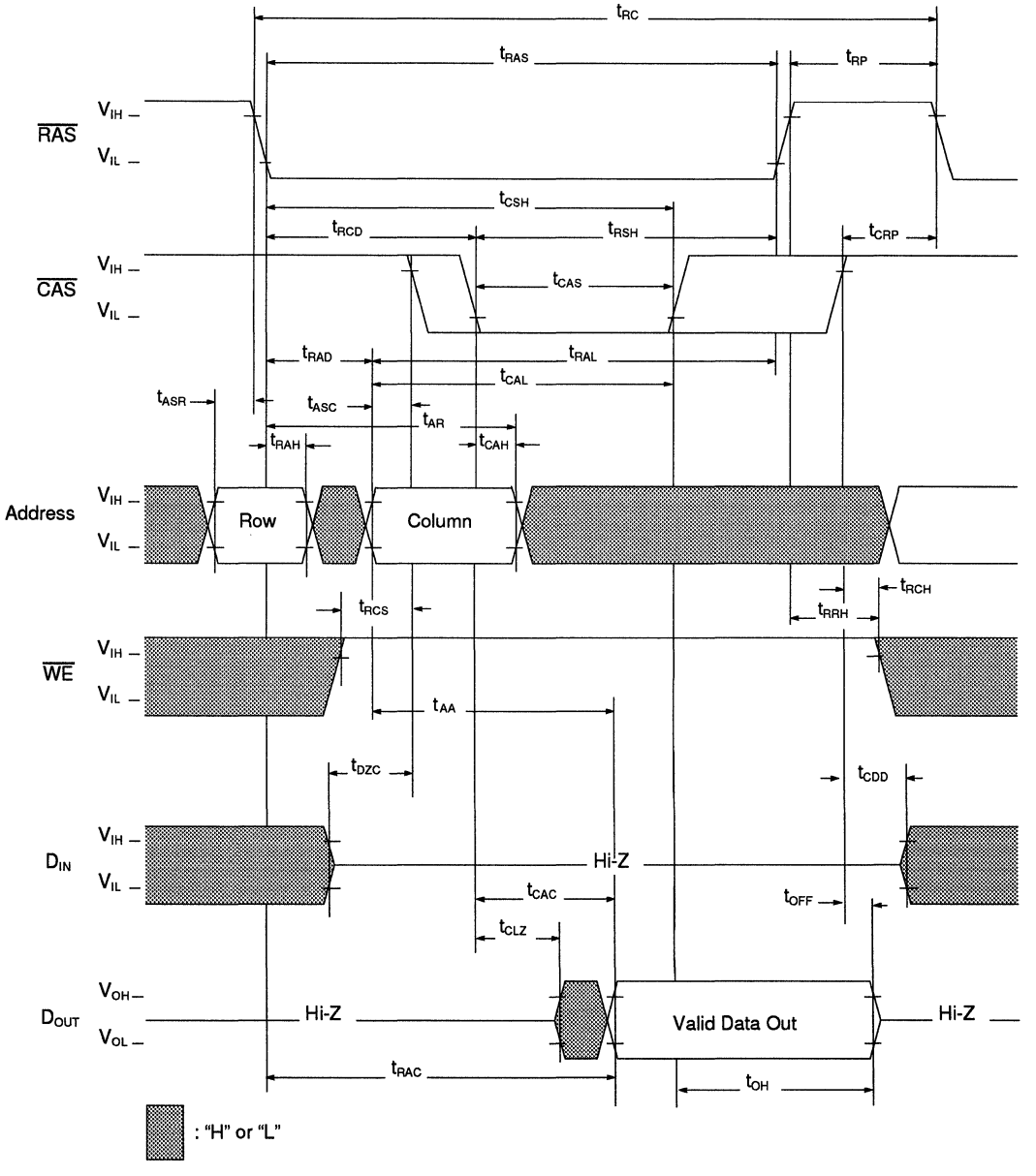
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

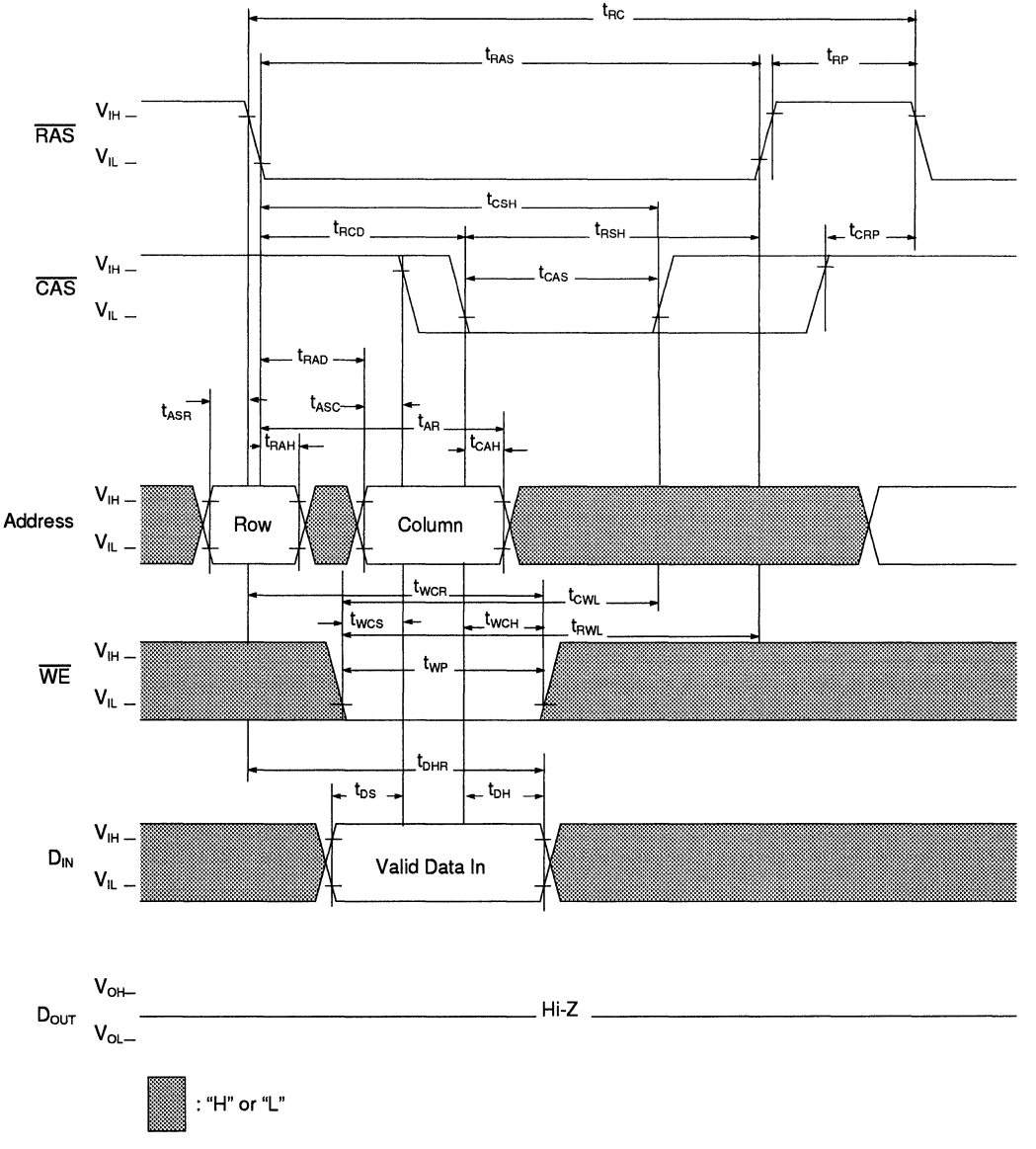
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	256	—	256	ms	1

1. 2048 refreshes are required every 256ms.

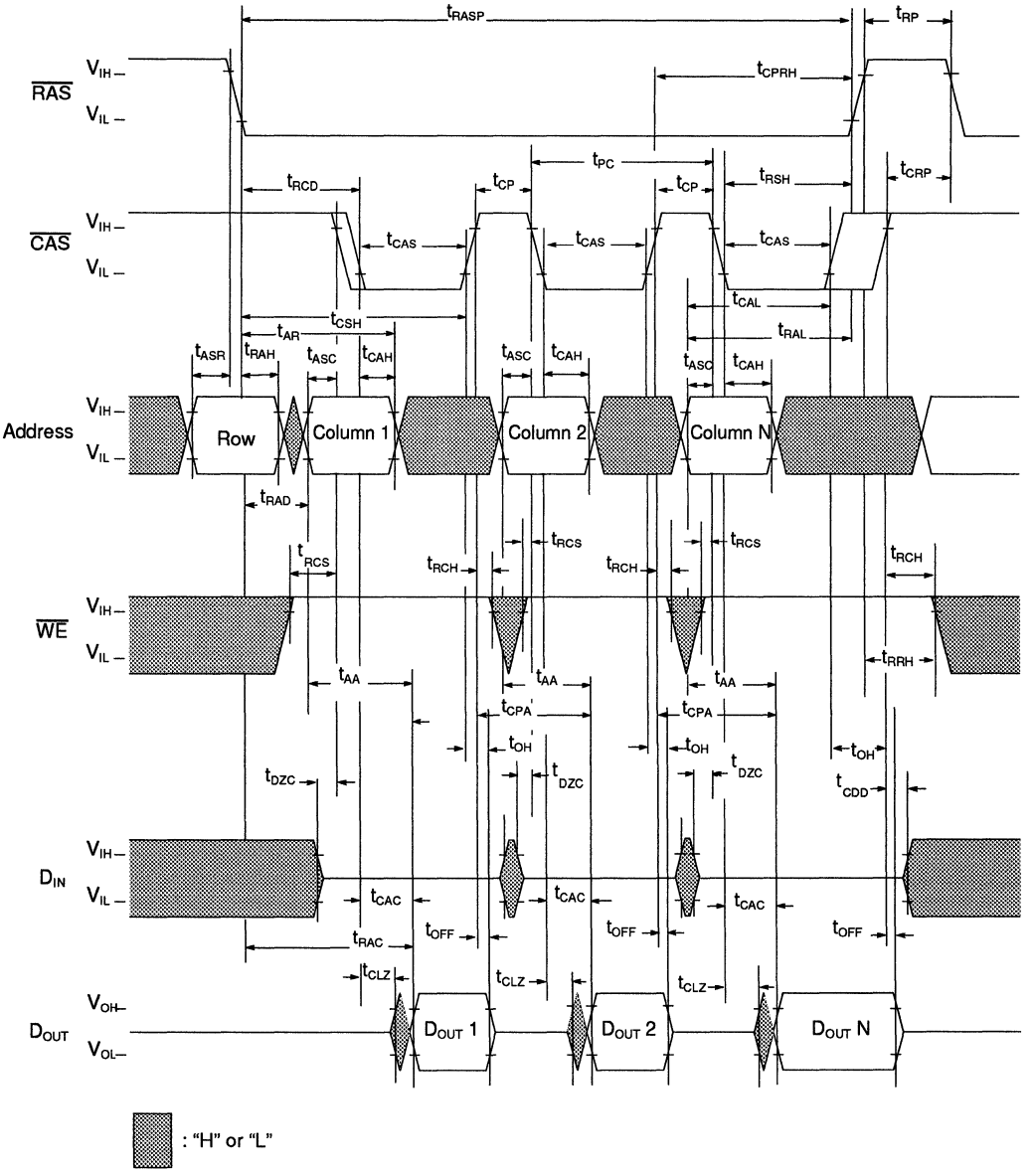
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

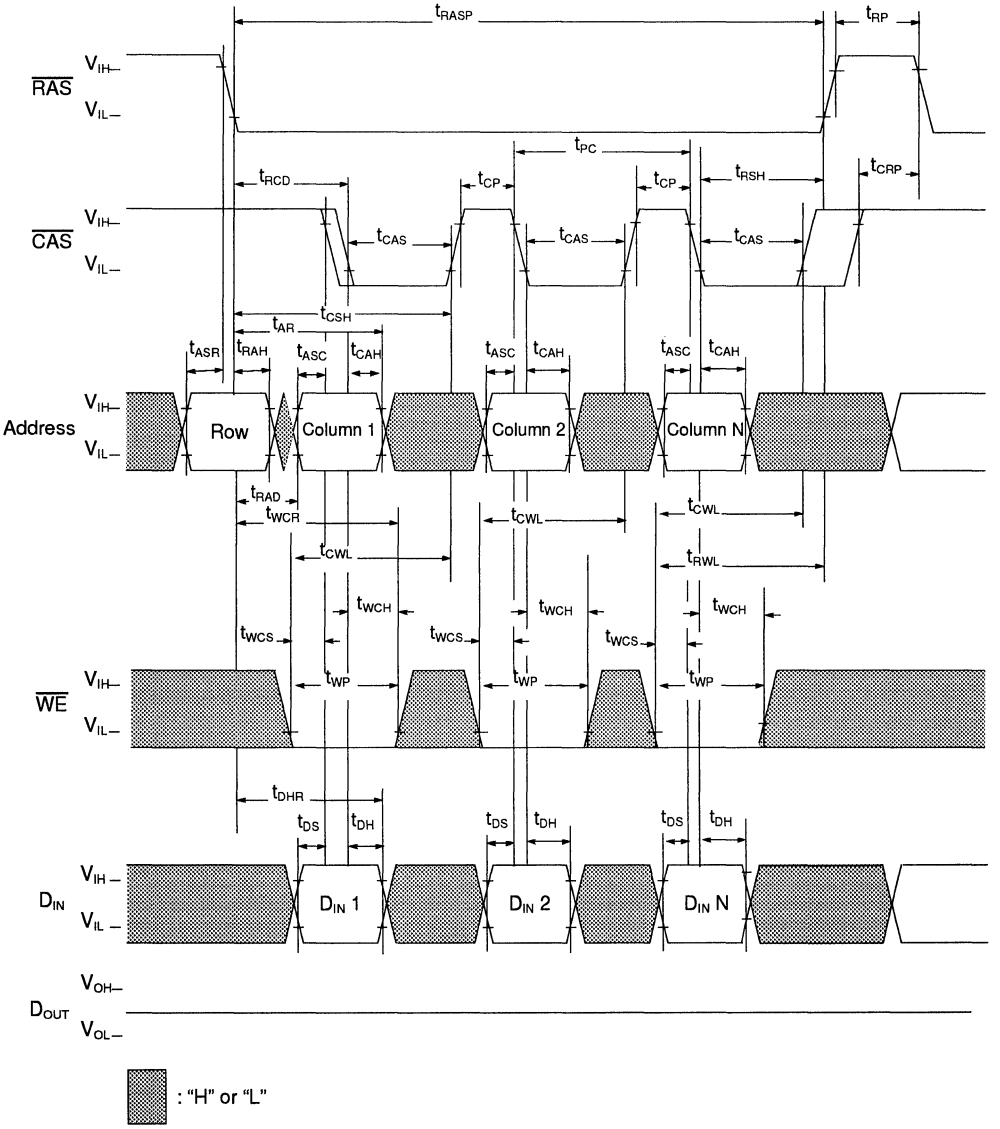
Write Cycle (Early Write)



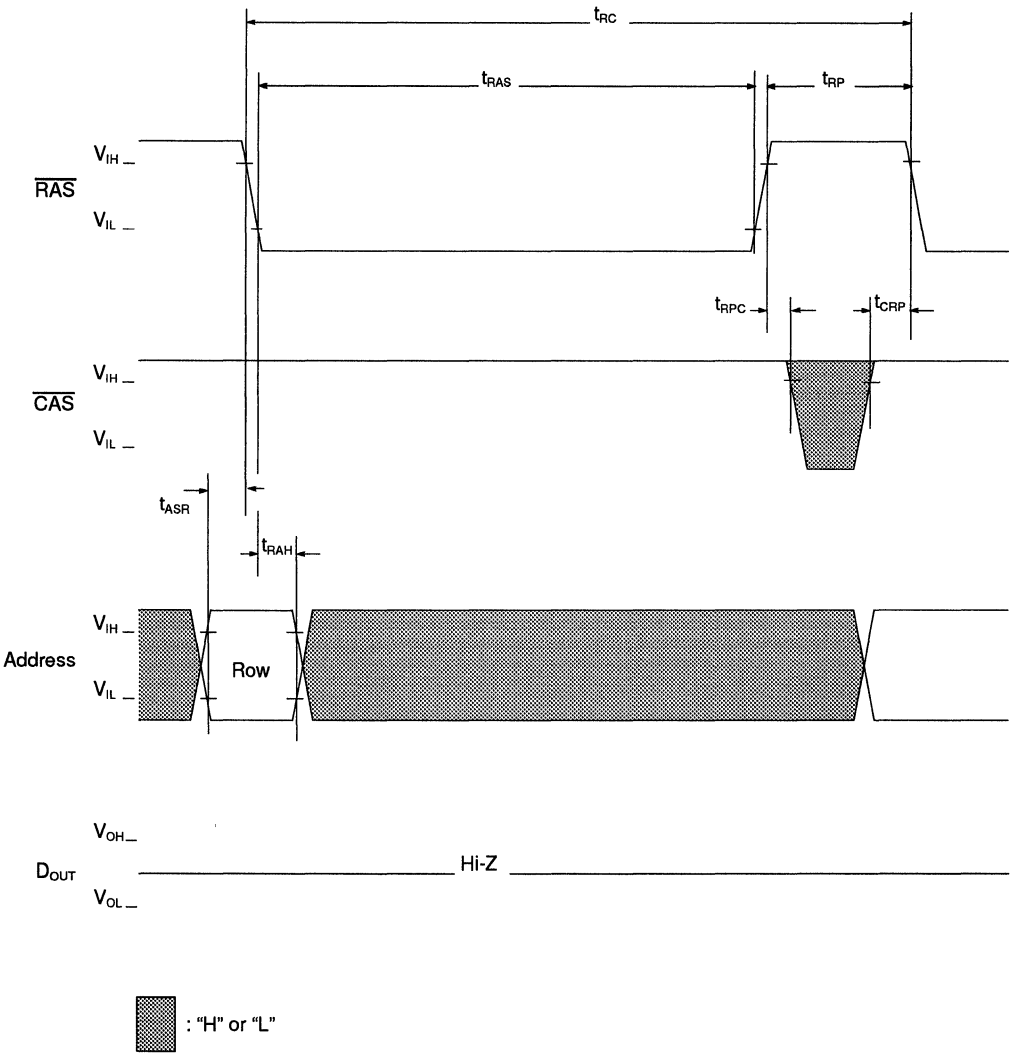
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

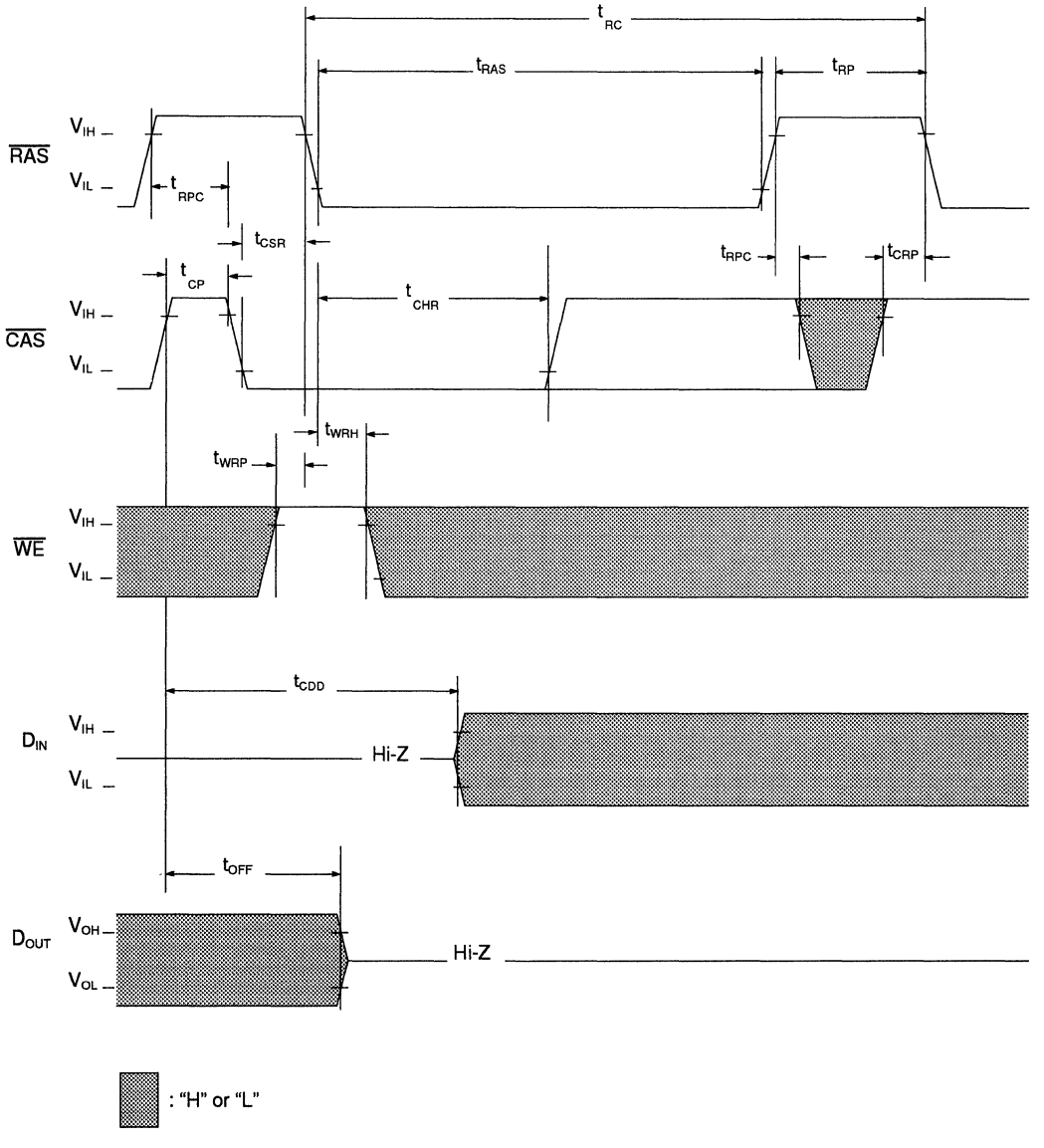


$\overline{RAS}$ Only Refresh Cycle



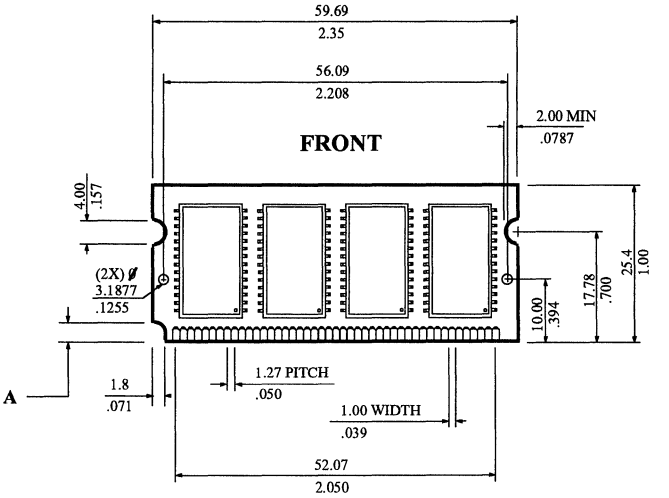
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

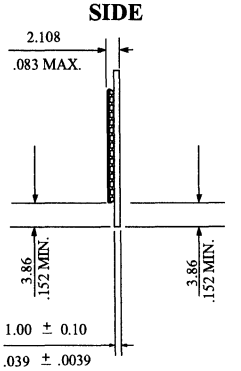


Note: Addresses are "H" or "L"

Layout Drawing



A =	3.3V	5.0V
	3.175 .125	6.35 .246



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Single 3.3, ± 0.3V or 5.0, ± 0.25V Power Supply
- Low active current consumption
- All inputs & outputs are TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 4096 refresh cycles distributed across 256ms
- 12/8 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au contacts

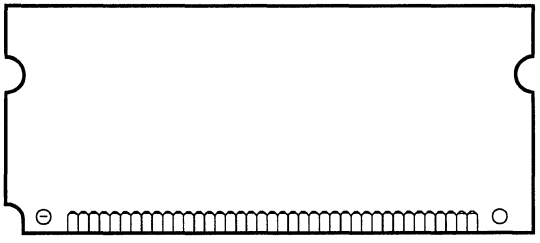
Description

The IBM11S2320NN/L are 8MB industry standard 72-pin 4-byte small outline dual in-line memory modules (SODIMM's). The module is organized as a 2Mx32 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 4 1Mx16 TSOP devices, each in a 400mil package

This assembly is intended for use in space constrained and or low power applications. It utilizes 12/8 address 16m bit technology to further reduce power consumption.

The IBM 72-Pin SODIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint. Related products include the 2Mx36 parity version IBM11S2360NN/L as well as a 2Mx32 version with 11/10 addressing IBM11S2320HN/L

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A11	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V or +5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

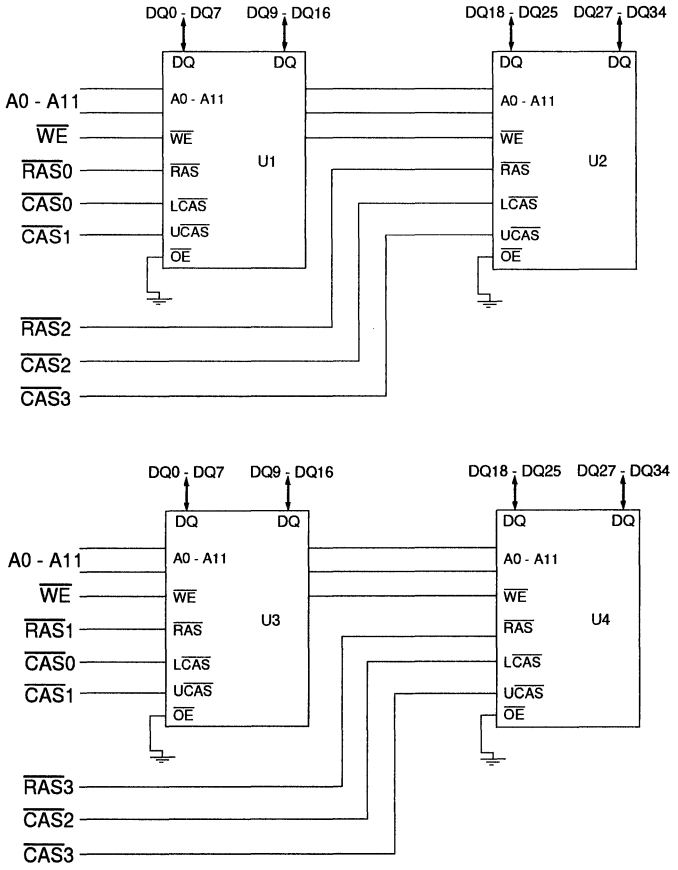
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ23	64	DQ34
5	DQ3	17	A5	29	A11	41	$\overline{CAS2}$	53	DQ24	65	NC
6	DQ4	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ25	66	PD2
7	DQ5	19	A10	31	A8	43	$\overline{CAS1}$	55	NC	67	PD3
8	DQ6	20	NC	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{RAS2}$	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{WE}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	NC	48	NC	60	DQ30	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Power
IBM11S2320NNA-60	2M x 32	60ns	Au	2.35" x 1" x .1496"	3.3V
IBM11S2320NNA-70	2M x 32	70ns	Au	2.35" x 1" x .1496"	3.3V
IBM11S2320NLA-60	2M x 32	60ns	Au	2.35" x 1" x .1496"	5.0V
IBM11S2320NLA-70	2M x 32	70ns	Au	2.35" x 1" x .1496"	5.0V

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	V_{SS}	V_{SS}
PD3	NC	NC
PD4	V_{SS}	V_{SS}
PD5	NC	V_{SS}
PD6	NC	NC
PD7	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt	5.0 Volt		
V_{CC}	Power Supply Voltage	-0.5 to + 4.6	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.7 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	-55 to +125	°C	1
P_D	Power Dissipation	0.6	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3 Volt			5.0 Volt			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3± 0.3V or 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	38	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	16	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	22	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	42	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	23	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V or 5.0± 0.25V)

Symbol	Parameter		3.3 Volt		5.0 Volt		Units	Notes
			Min	Max	Min	Max		
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	190	—	190	mA	1, 2, 3
		-70	—	170	—	170		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	8	—	8	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	190	—	190	mA	1, 3
		-70	—	170	—	170		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	150	—	150	mA	1, 2, 3
		-70	—	130	—	130		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	0.8	—	0.8	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	190	—	190	mA	1, 3
		-70	—	170	—	170		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-10	+10	-10	+10	µA	
		$\overline{CAS}$	-20	+20	-20	+20		
		All others	-40	+40	-40	+40		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

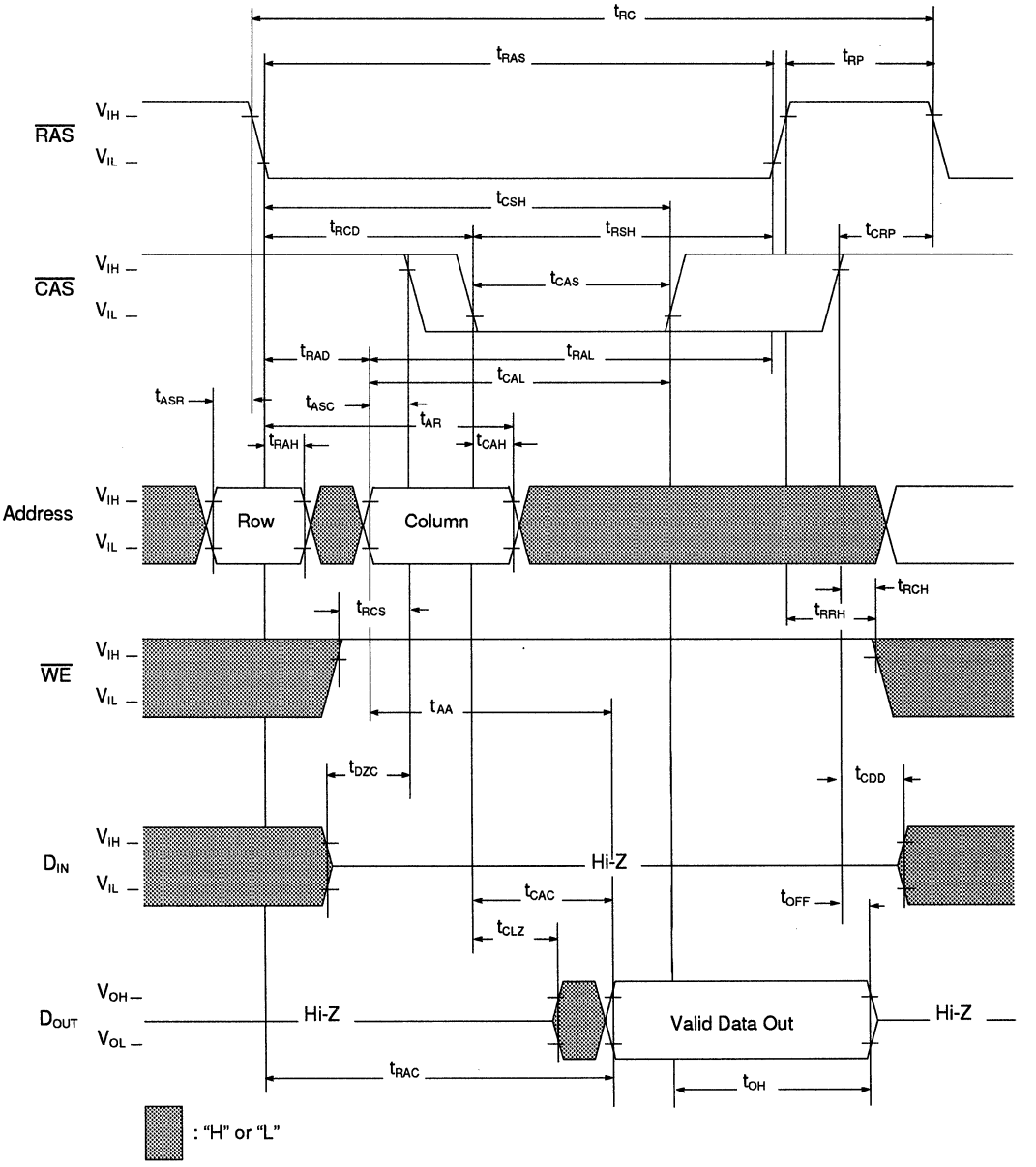
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

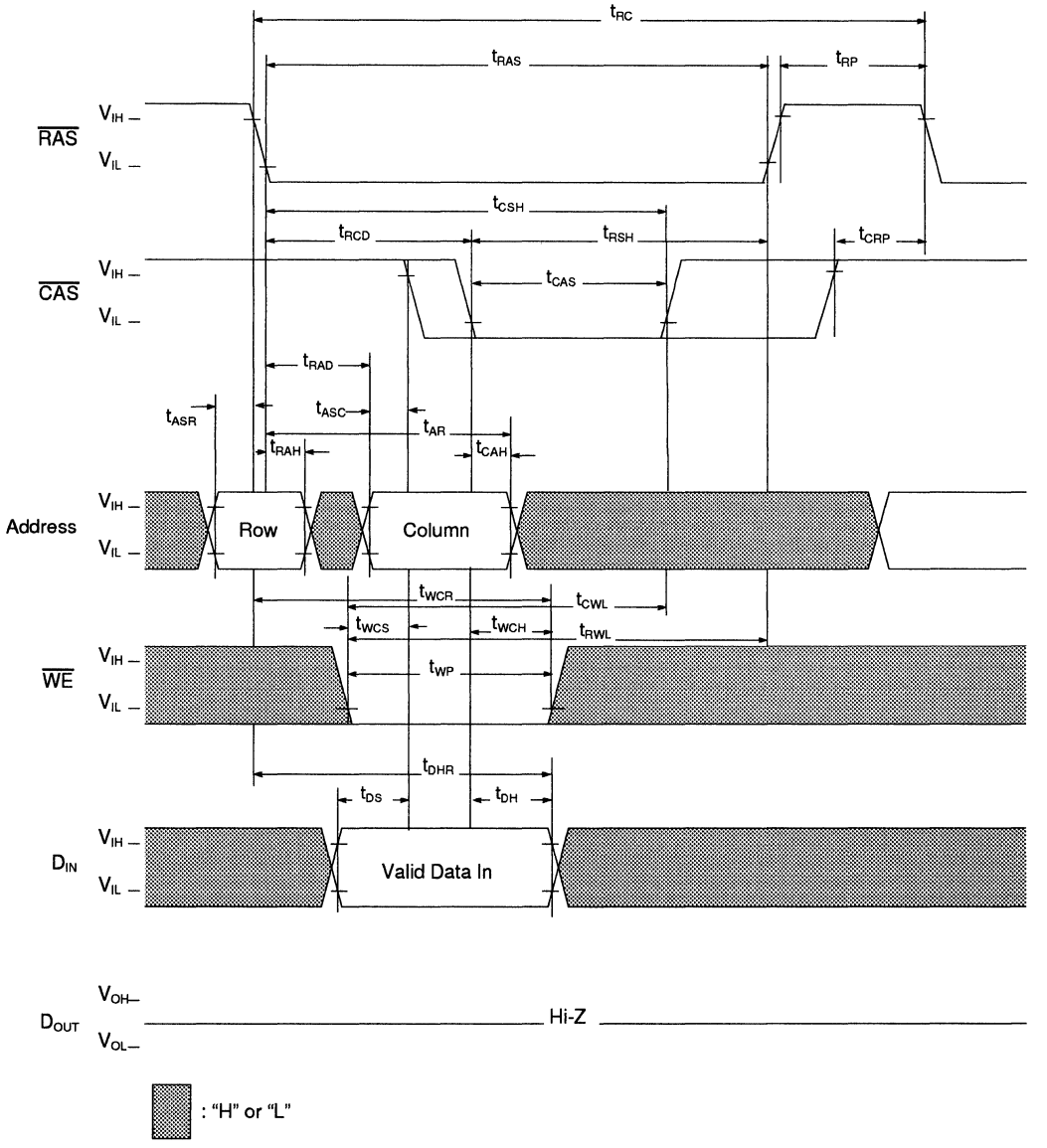
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	256	—	256	ms	1

1. 4096 refreshes are required every 256ms.

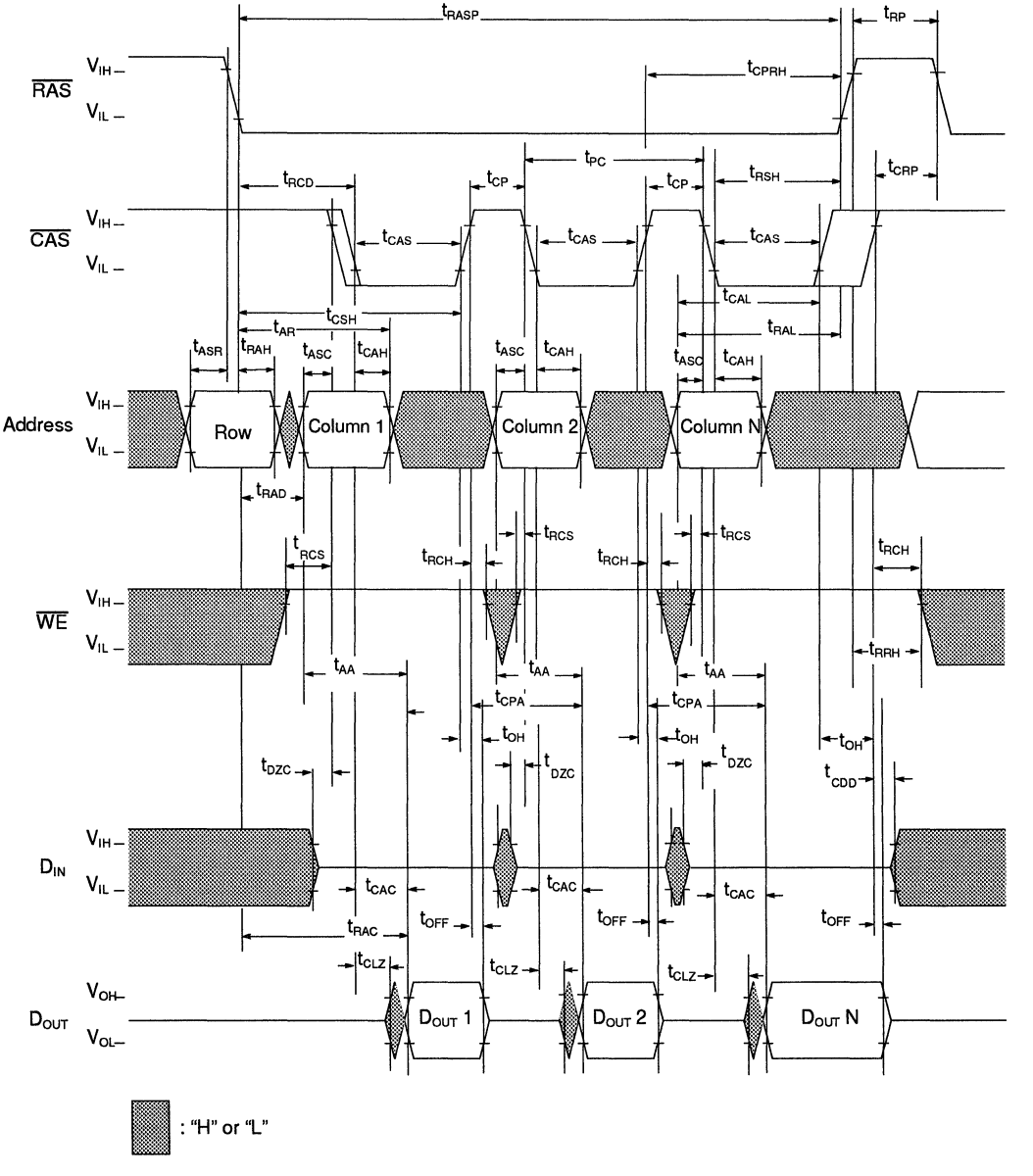
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCH
tRRH
tRCS
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

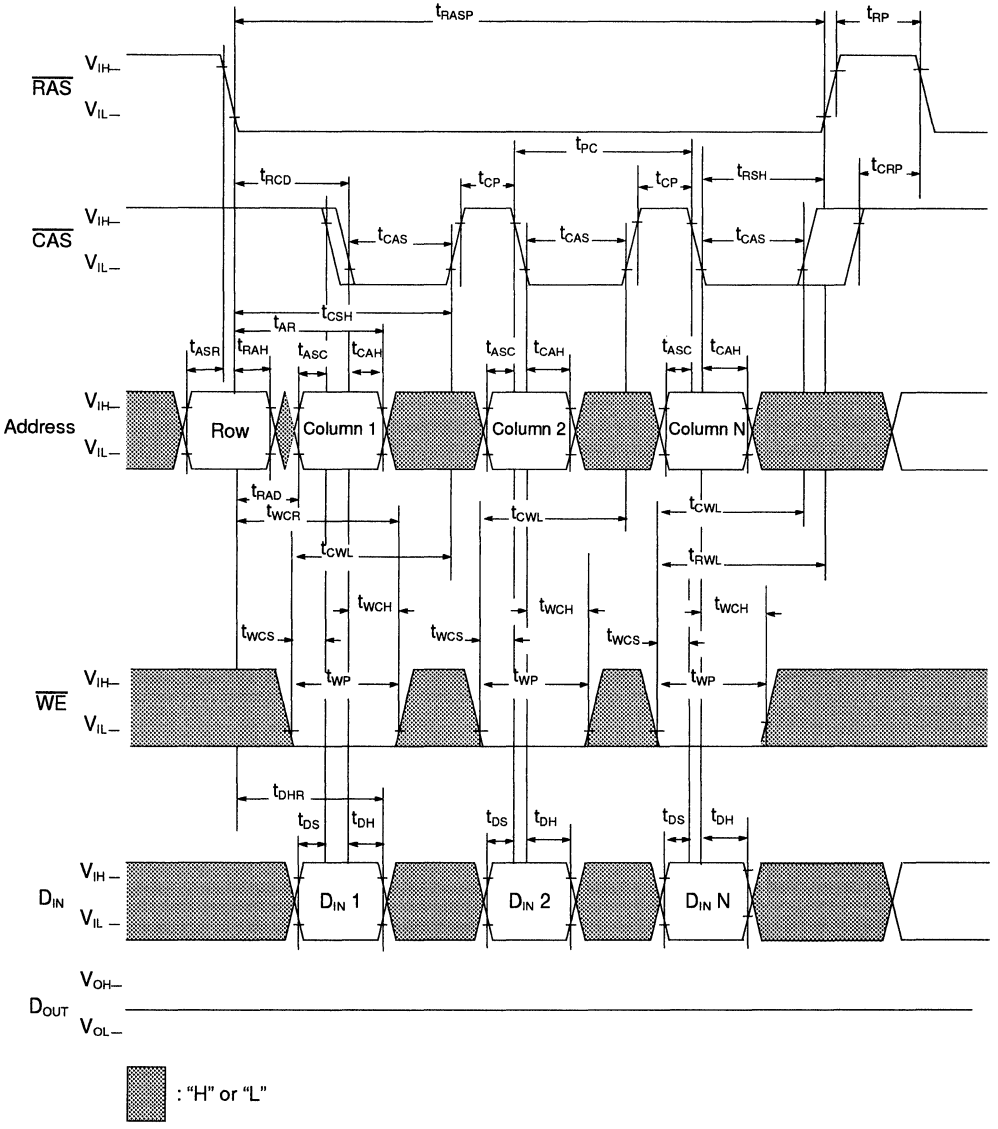
Write Cycle (Early Write)



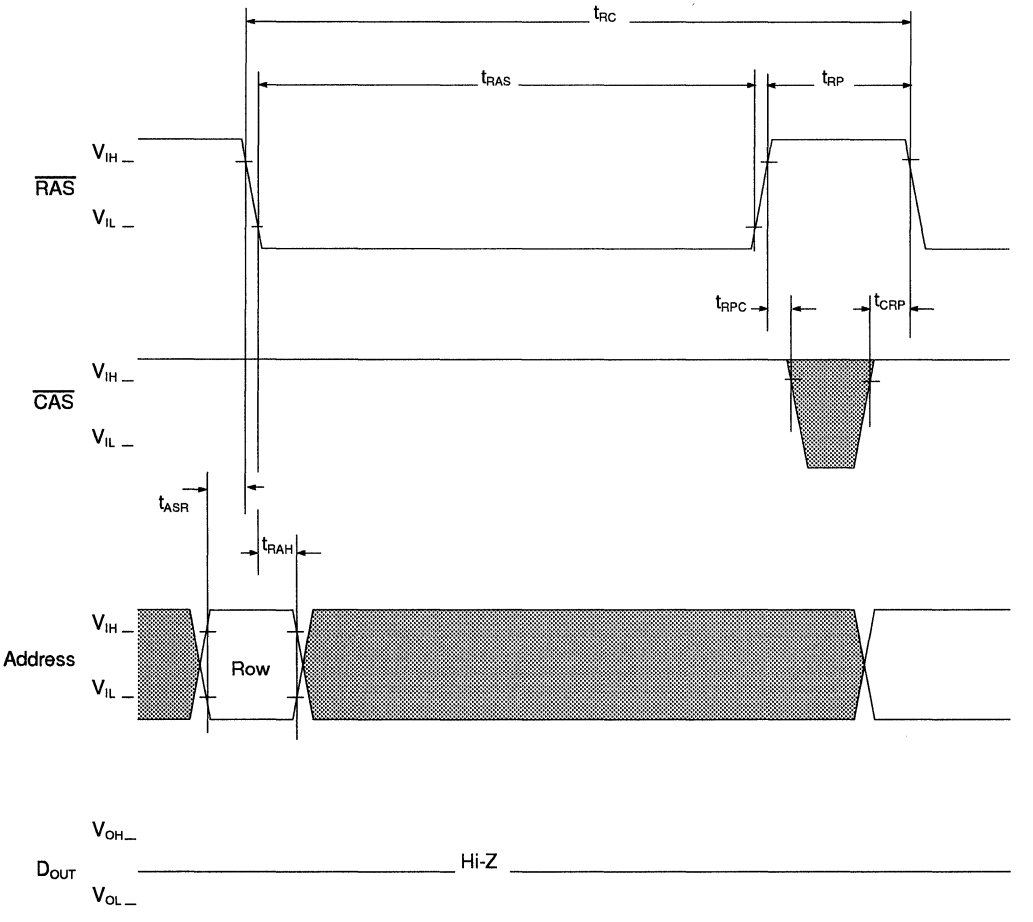
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

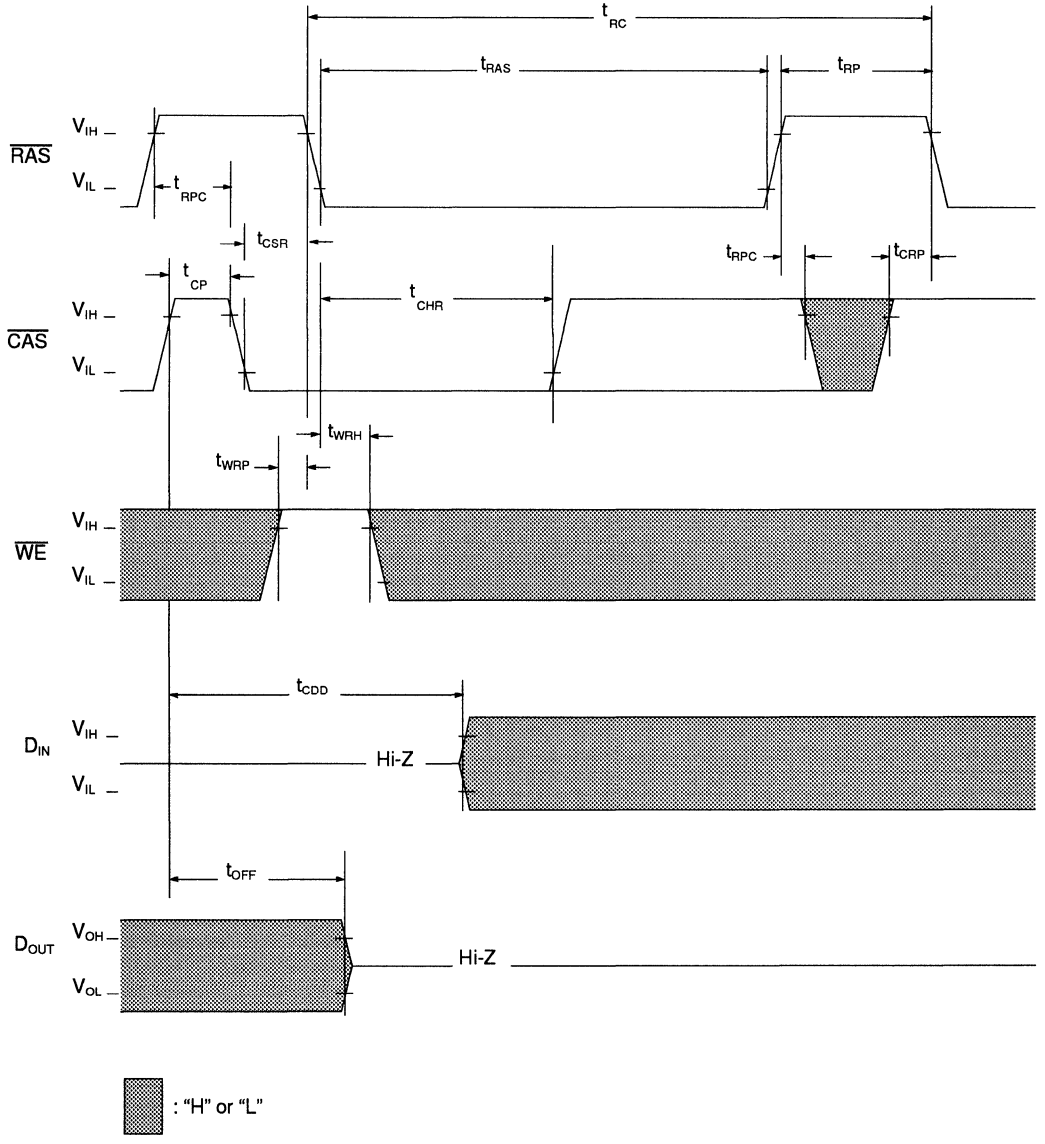


$\overline{RAS}$ Only Refresh Cycle



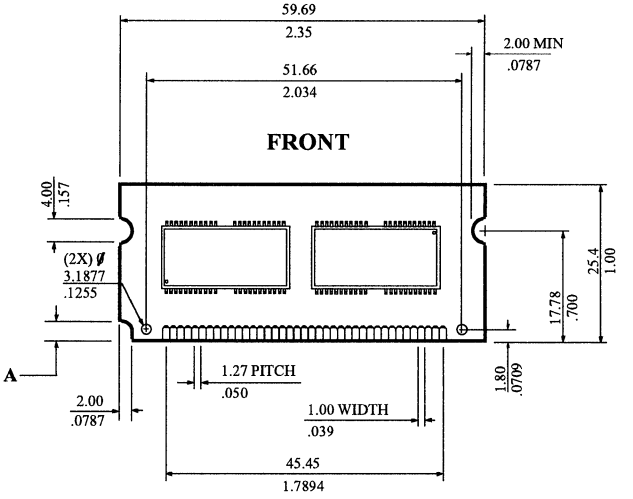
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

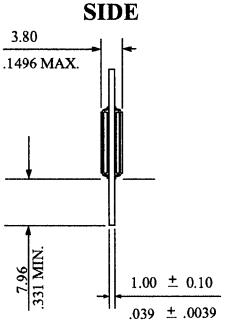


Note: Addresses are "H" or "L"

Layout Drawing



A =	3.3V	5.0V
	3.175 / .125	6.35 / .246



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Single 3.3, ± 0.3V or 5.0, ± 0.25V Power Supply
- Low active current consumption
- All inputs & outputs are TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 2048 refresh cycles distributed across 256ms
- 11/10 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au contacts

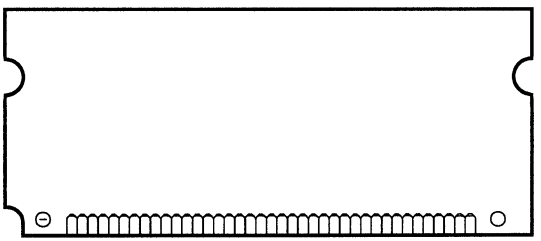
Description

The IBM11S4320HN/L are 16MB 72-pin 4-byte small outline dual in-line memory modules (SODIMM's). The module is organized as a 4Mx32 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 8 2Mx8 TSOP devices, each in a 400mil package

This assembly is intended for use in space constrained and or low power applications.

The IBM 72-Pin SODIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint. Related products include the 4Mx32 version with 12/10 addressing IBM11S4320CN/L as well as a 4Mx36 parity version IBM11S4360DN/L.

Card Outline



(Front) 1 71
(Back) 2 72

Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V or +5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

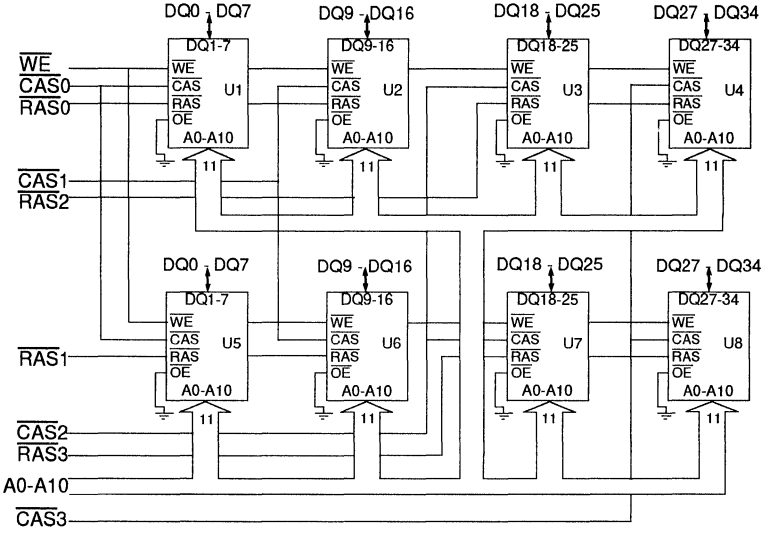
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ23	64	DQ34
5	DQ3	17	A5	29	A11	41	$\overline{CAS2}$	53	DQ24	65	NC
6	DQ4	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ25	66	PD2
7	DQ5	19	A10	31	A8	43	$\overline{CAS1}$	55	NC	67	PD3
8	DQ6	20	NC	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{RAS2}$	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{WE}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	NC	48	NC	60	DQ30	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Power
IBM11S4320HNA-60	4M x 32	60ns	Au	2.35" x 1" x .127"	3.3V
IBM11S4320HNA-70	4M x 32	70ns	Au	2.35" x 1" x .127"	3.3V
IBM11S4320HLA-60	4M x 32	60ns	Au	2.35" x 1" x .127"	5.0V
IBM11S4320HLA-70	4M x 32	70ns	Au	2.35" x 1" x .127"	5.0V

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V_{SS}	V_{SS}
PD2	NC	NC
PD3	V_{SS}	V_{SS}
PD4	V_{SS}	V_{SS}
PD5	NC	V_{SS}
PD6	NC	NC
PD7	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt	5.0 Volt		
V_{CC}	Power Supply Voltage	-0.5 to + 4.6	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.7 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	-55 to +125	°C	1
P_D	Power Dissipation	0.6	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3 Volt			5.0 Volt			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3± 0.3V or 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	58	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	24	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	21	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	68	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	24	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V or 5.0± 0.25V)

Symbol	Parameter		3.3 Volt		5.0 Volt		Units	Notes
			Min	Max	Min	Max		
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	480	—	480	mA	1, 2, 3
		-70	—	400	—	400		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	8	—	8	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	480	—	480	mA	1, 3
		-70	—	400	—	400		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	300	—	300	mA	1, 2, 3
		-70	—	260	—	260		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	0.8	—	0.8	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	480	—	480	mA	1, 3
		-70	—	400	—	400		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-10	+10	-10	+10	µA	
		$\overline{CAS}$	-20	+20	-20	+20		
		All others	-80	+80	-80	+40		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

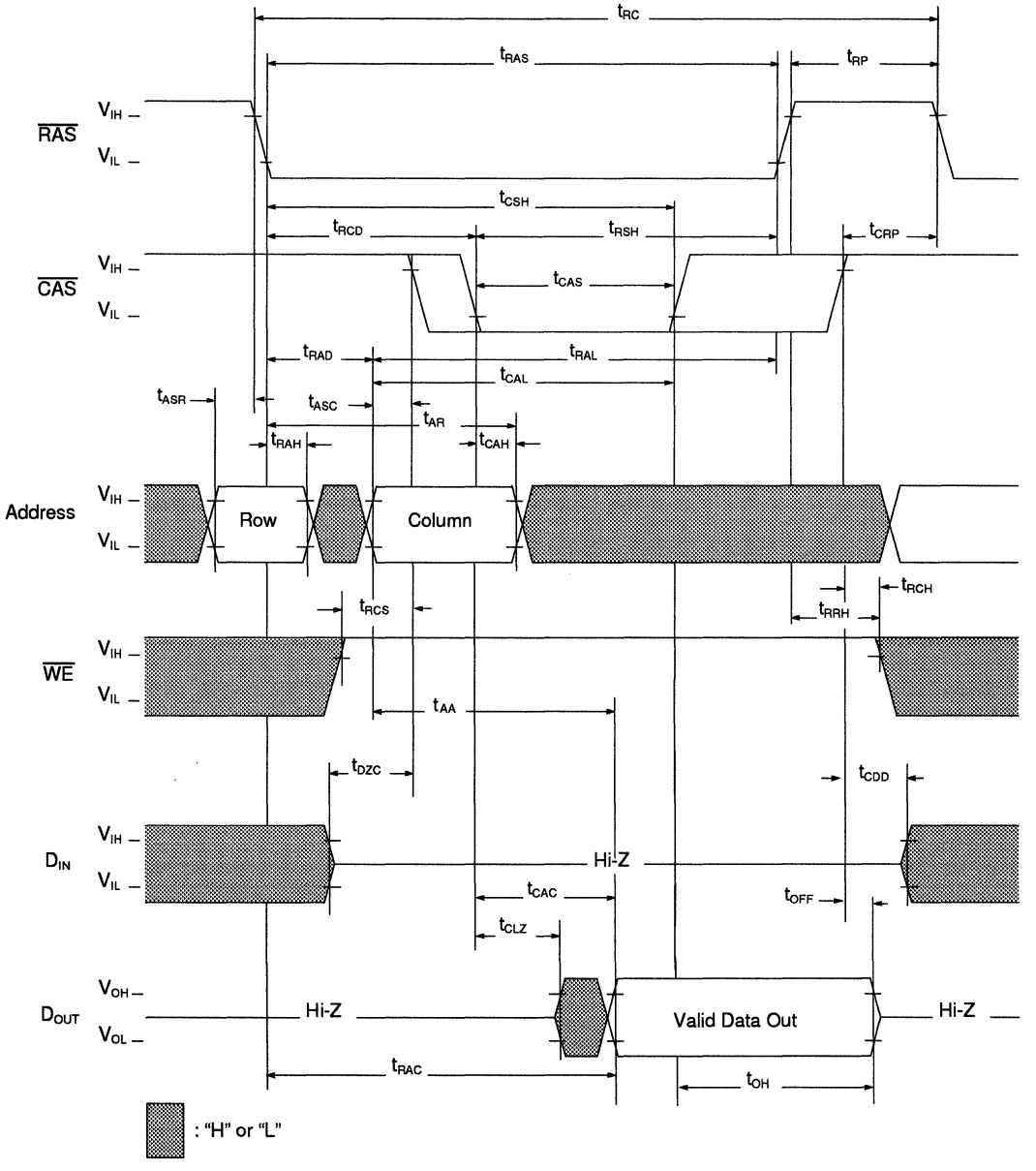
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

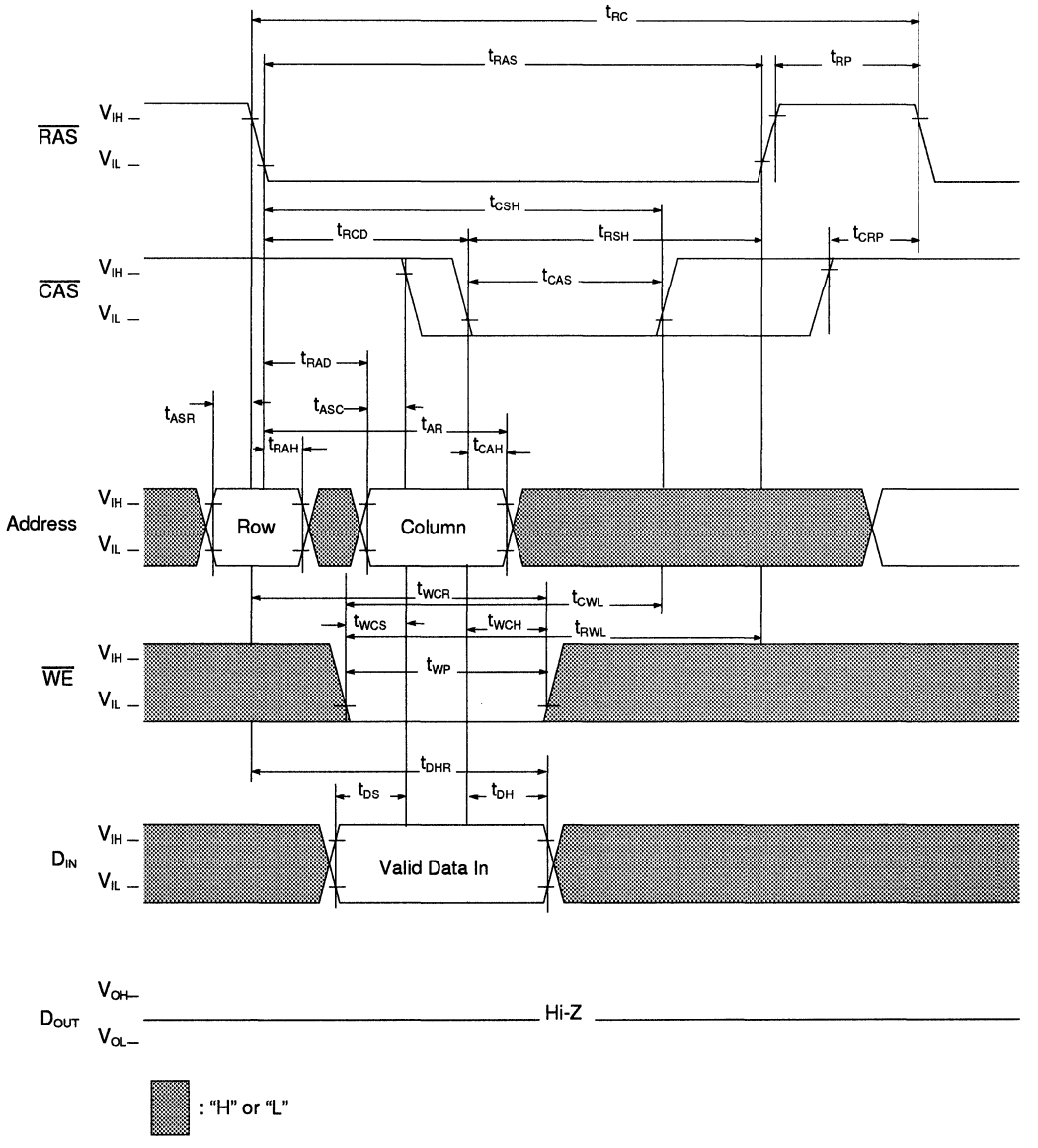
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	256	—	256	ms	1

1. 2048 refreshes are required every 256ms.

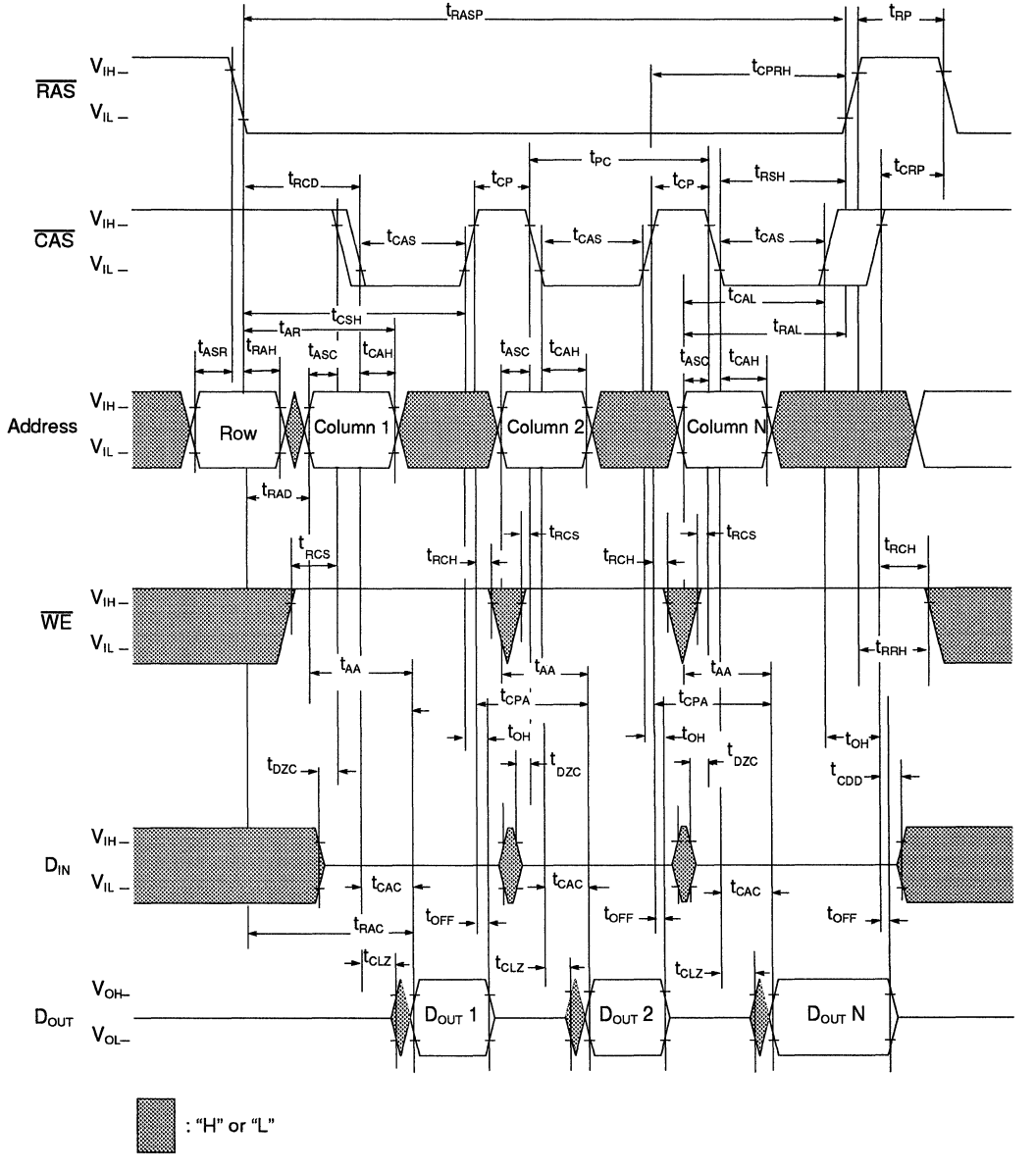
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

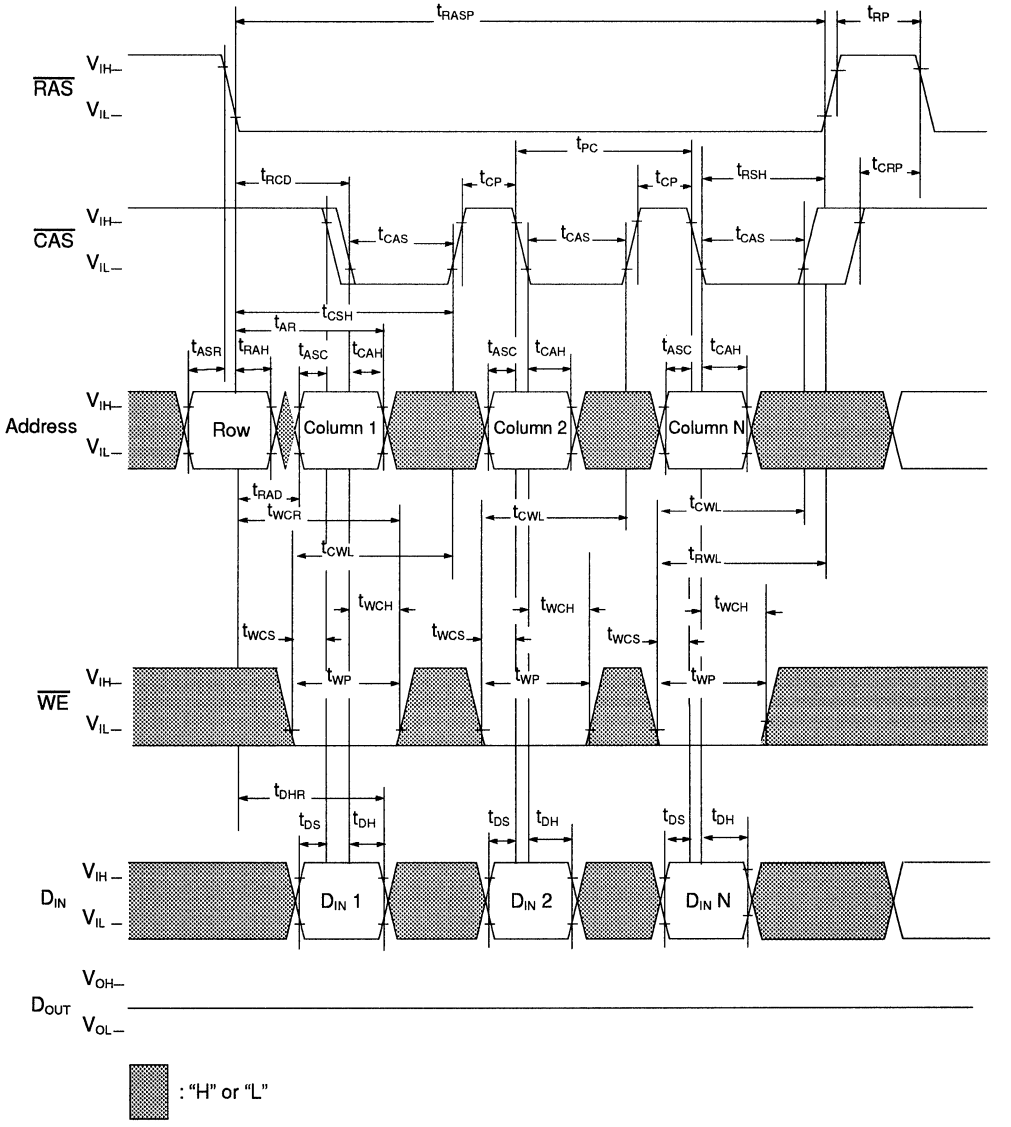
Write Cycle (Early Write)



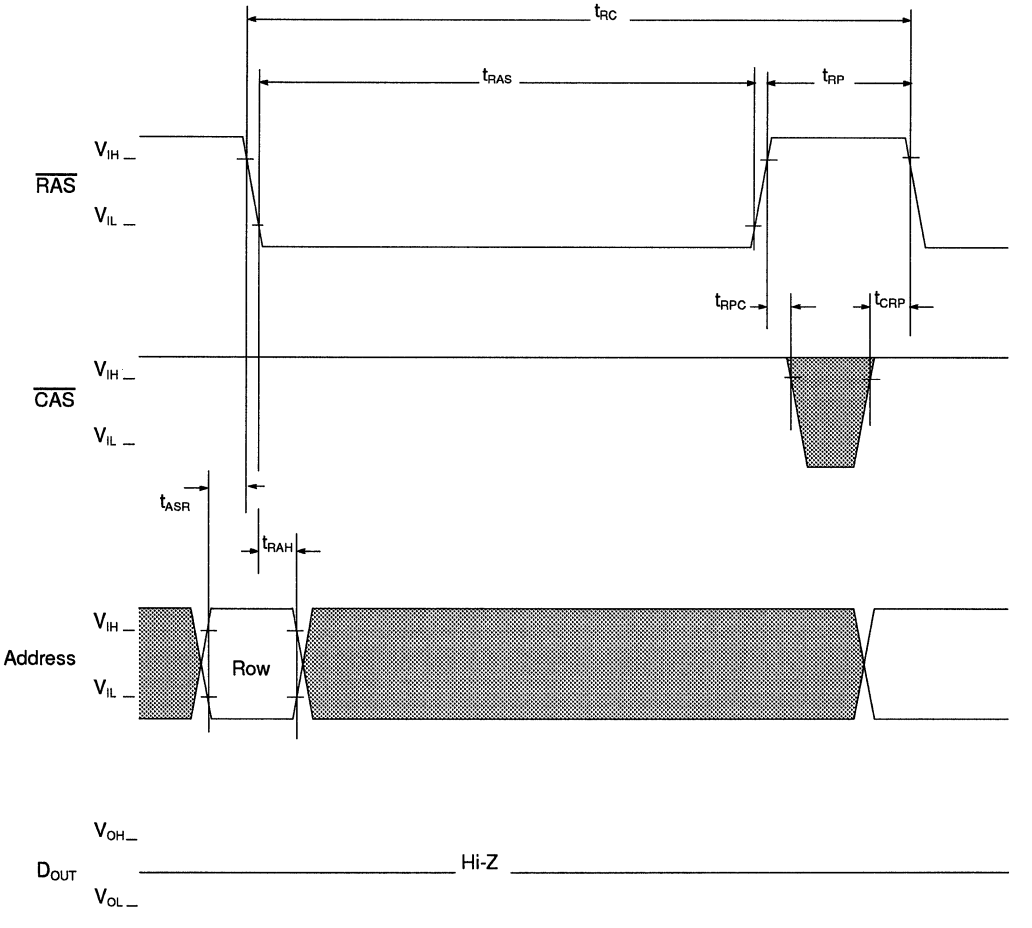
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



$\overline{RAS}$ Only Refresh Cycle



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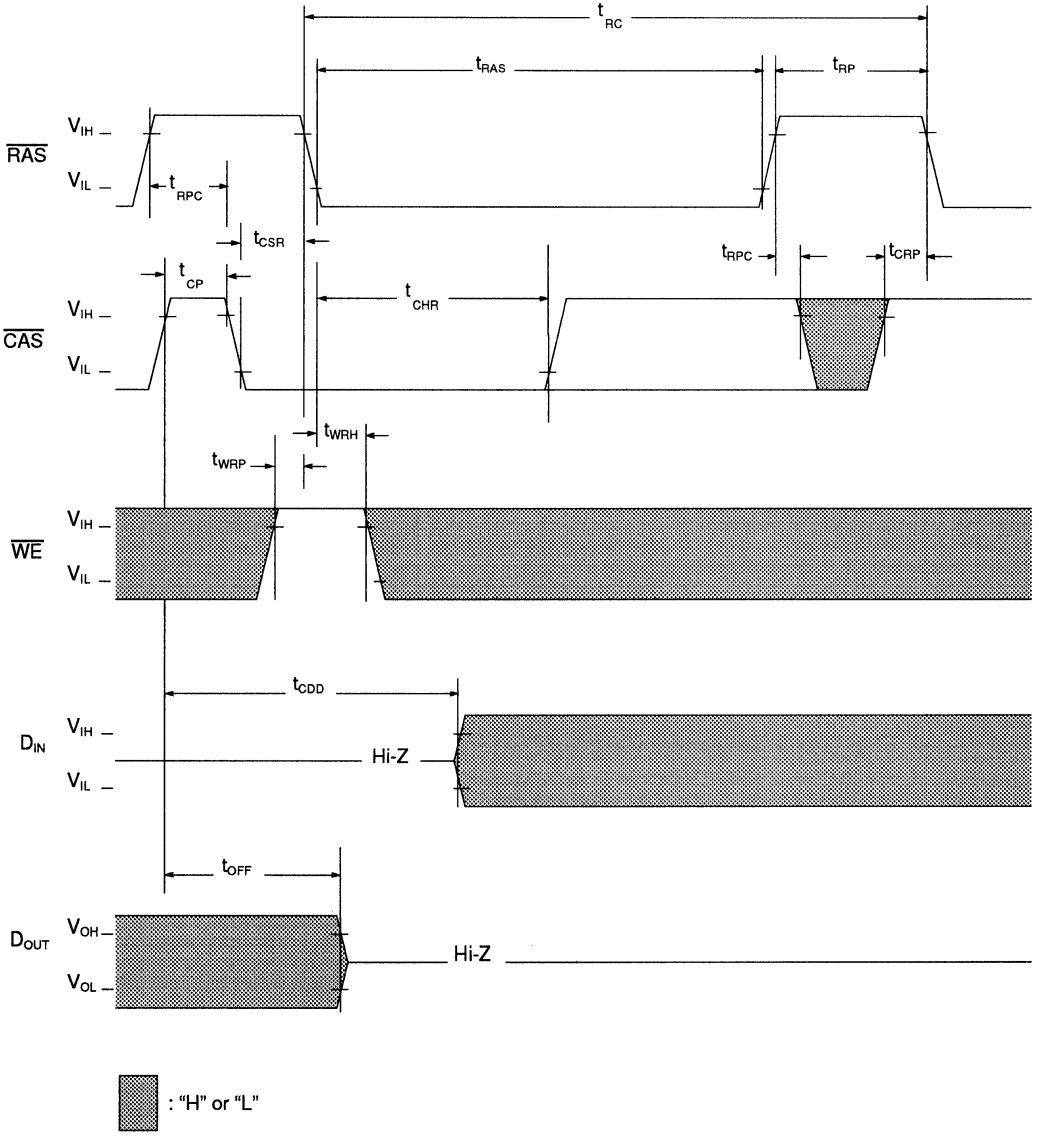
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



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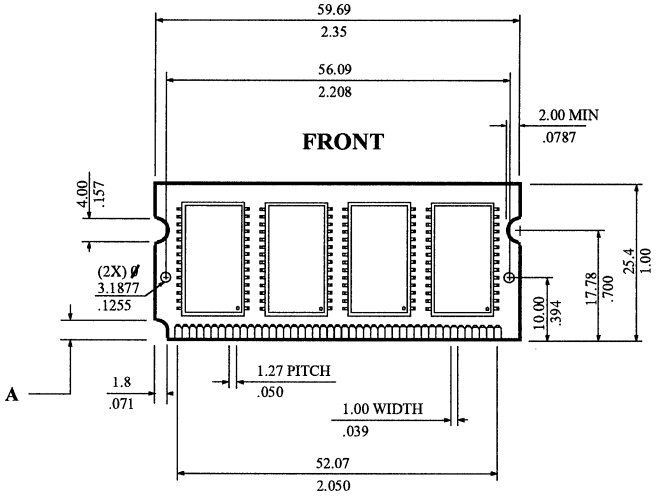

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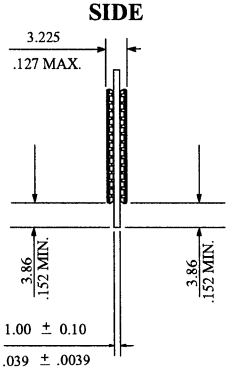

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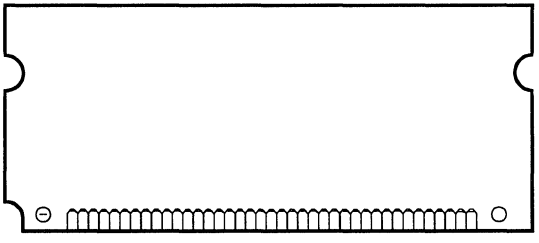
The IBM 72-Pin SODIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint. Related products include the 4Mx32 version with 11/10 addressing IBM11S4320HN/L as well as a 4Mx36 parity version IBM11S4360DN/L.

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A11	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V or +5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

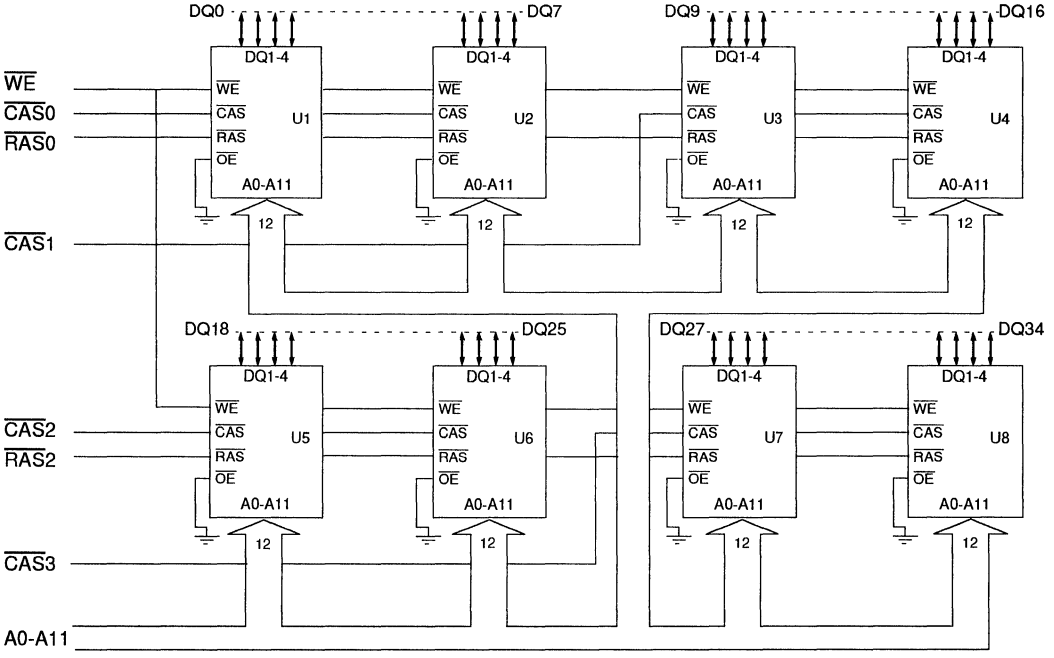
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ23	64	DQ34
5	DQ3	17	A5	29	A11	41	$\overline{CAS2}$	53	DQ24	65	NC
6	DQ4	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ25	66	PD2
7	DQ5	19	A10	31	A8	43	$\overline{CAS1}$	55	NC	67	PD3
8	DQ6	20	NC	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{RAS2}$	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{WE}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	NC	48	NC	60	DQ30	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Power
IBM11S4320CNA-60	4M x 32	60ns	Au	2.35" x 1" x .1496"	3.3V
IBM11S4320CNA-70	4M x 32	70ns	Au	2.35" x 1" x .1496"	3.3V
IBM11S4320CLA-60	4M x 32	60ns	Au	2.35" x 1" x .1496"	5.0V
IBM11S4320CLA-70	4M x 32	70ns	Au	2.35" x 1" x .1496"	5.0V

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	NC	NC
PD3	V_{SS}	V_{SS}
PD4	NC	NC
PD5	NC	V_{SS}
PD6	NC	NC
PD7	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt	5.0 Volt		
V_{CC}	Power Supply Voltage	-0.5 to + 4.6	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.7 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	-55 to +125	°C	1
P_D	Power Dissipation	0.6	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3 Volt			5.0 Volt			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3± 0.3V or 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	53	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	38.9	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	23	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	67	pF	
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	15	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V or 5.0± 0.25V)

Symbol	Parameter		3.3 Volt		5.0 Volt		Units	Notes
			Min	Max	Min	Max		
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	680	—	680	mA	1, 2, 3
		-70	—	600	—	600		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	16	—	16	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	680	—	680	mA	1, 3
		-70	—	600	—	600		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	600	—	600	mA	1, 2, 3
		-70	—	520	—	520		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	1.6	—	1.6	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	680	—	680	mA	1, 3
		-70	—	600	—	600		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	-40	+40	µA	
		$\overline{CAS}$	-20	+20	-20	+20		
		All others	-80	+80	-80	+40		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

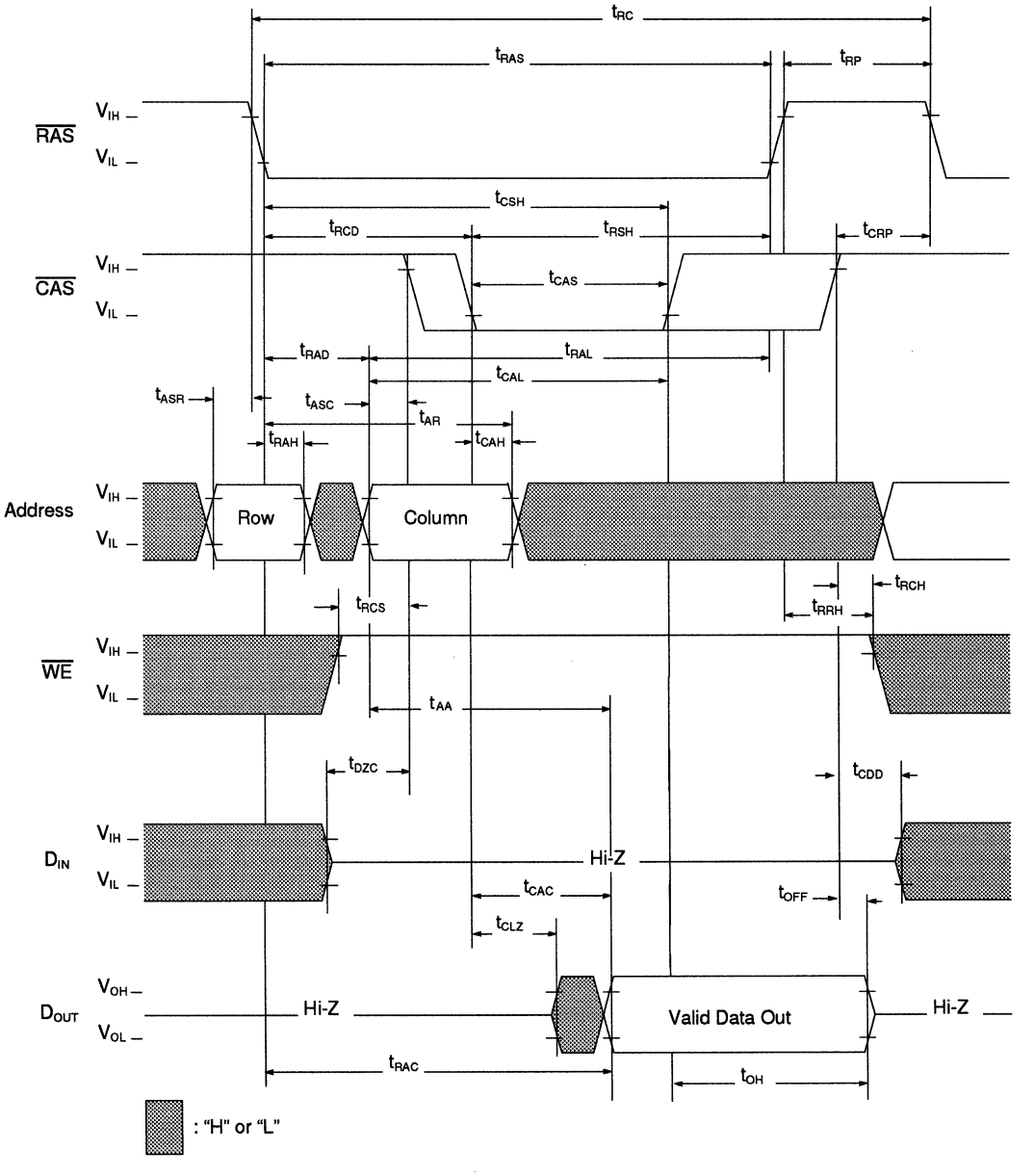
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

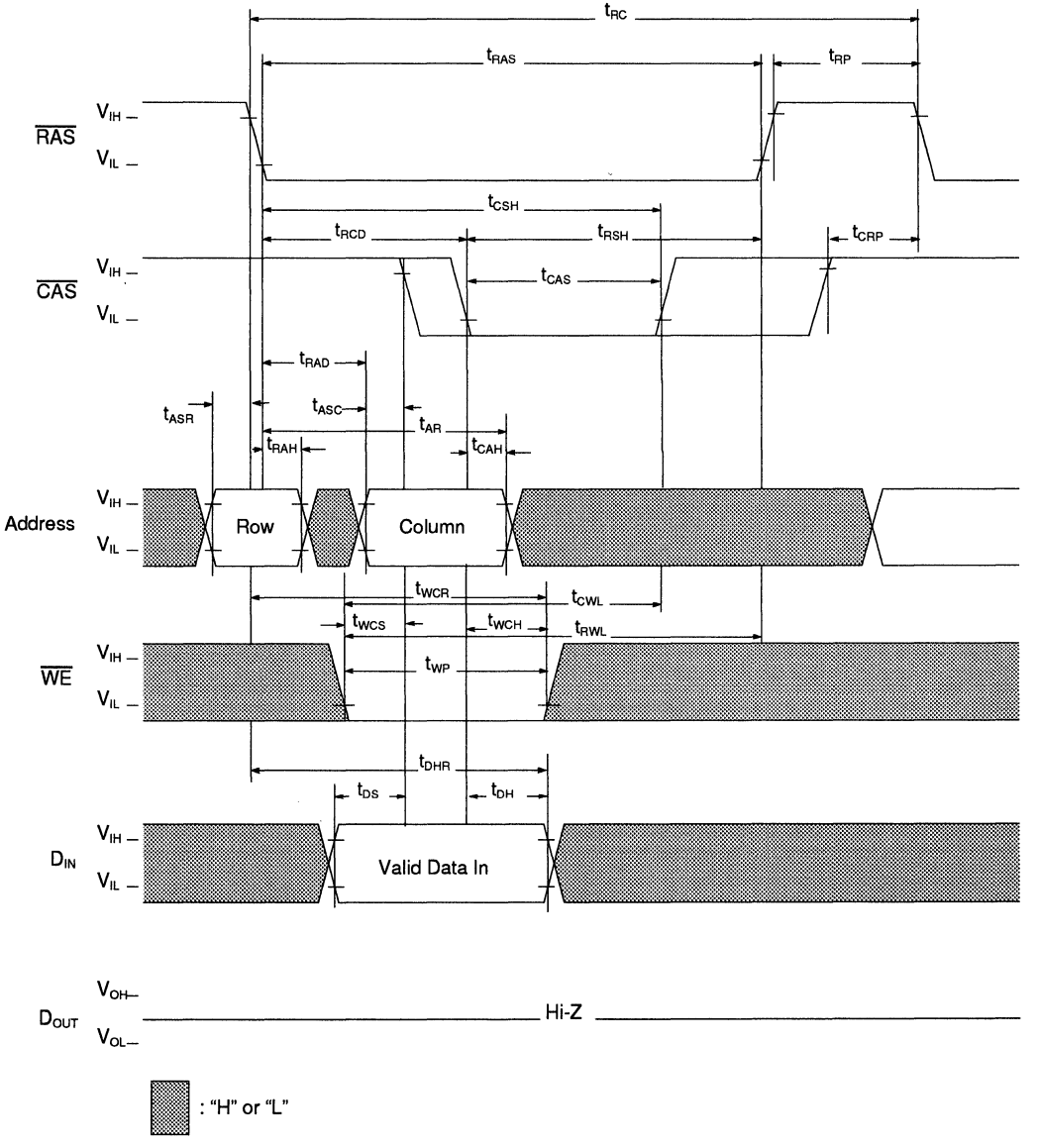
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	256	—	256	ms	1

1. 4096 refreshes are required every 256ms.

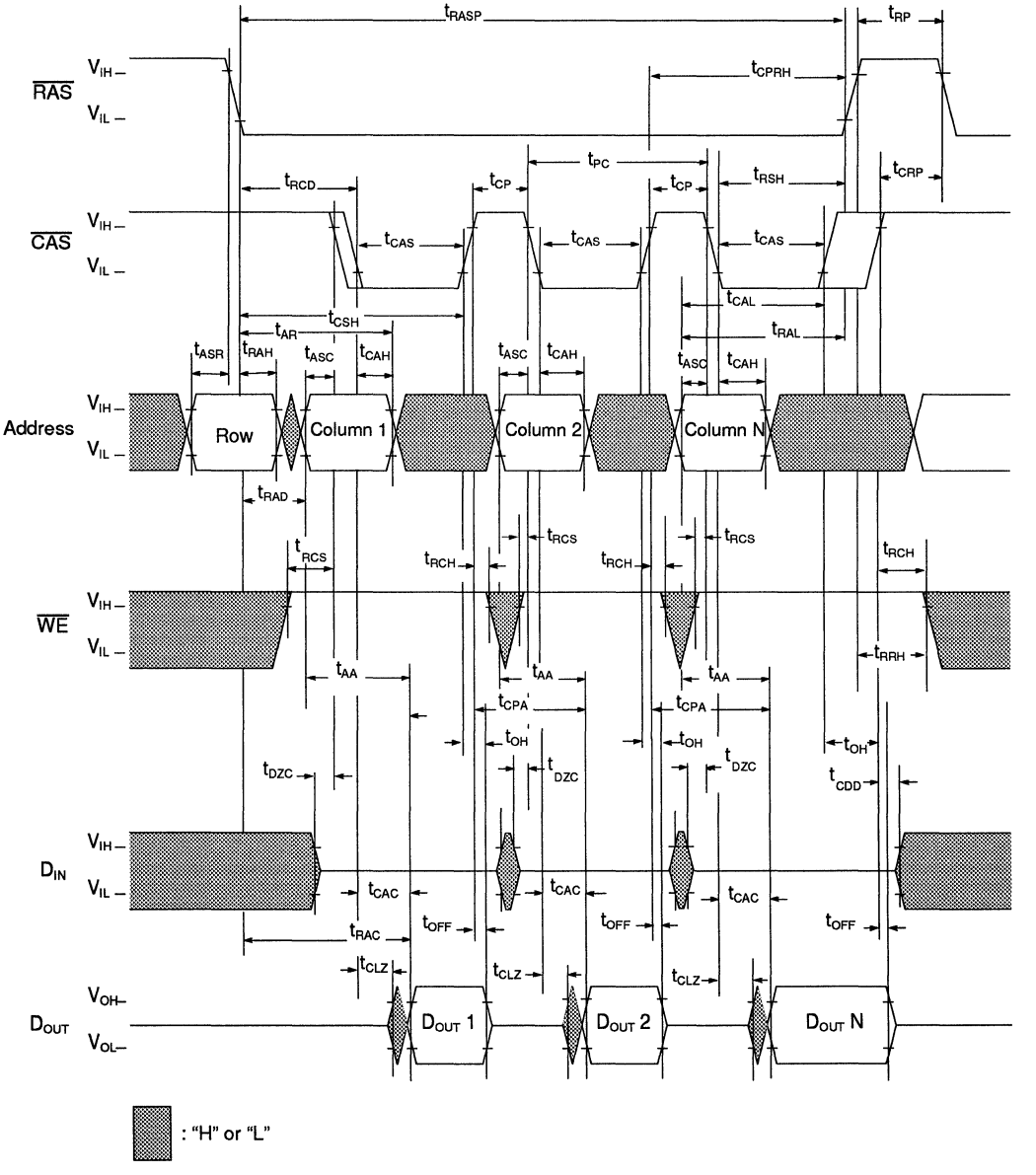
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

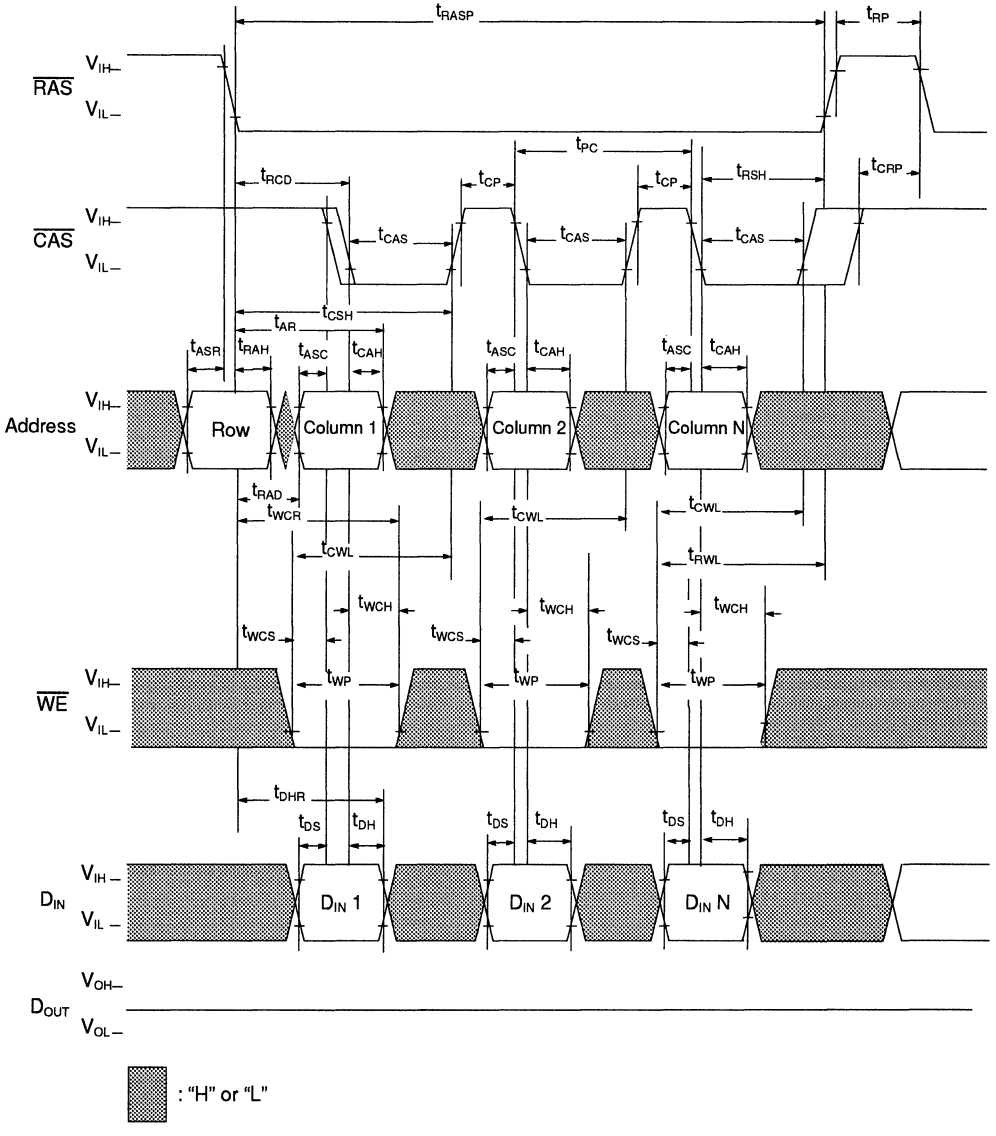
Write Cycle (Early Write)



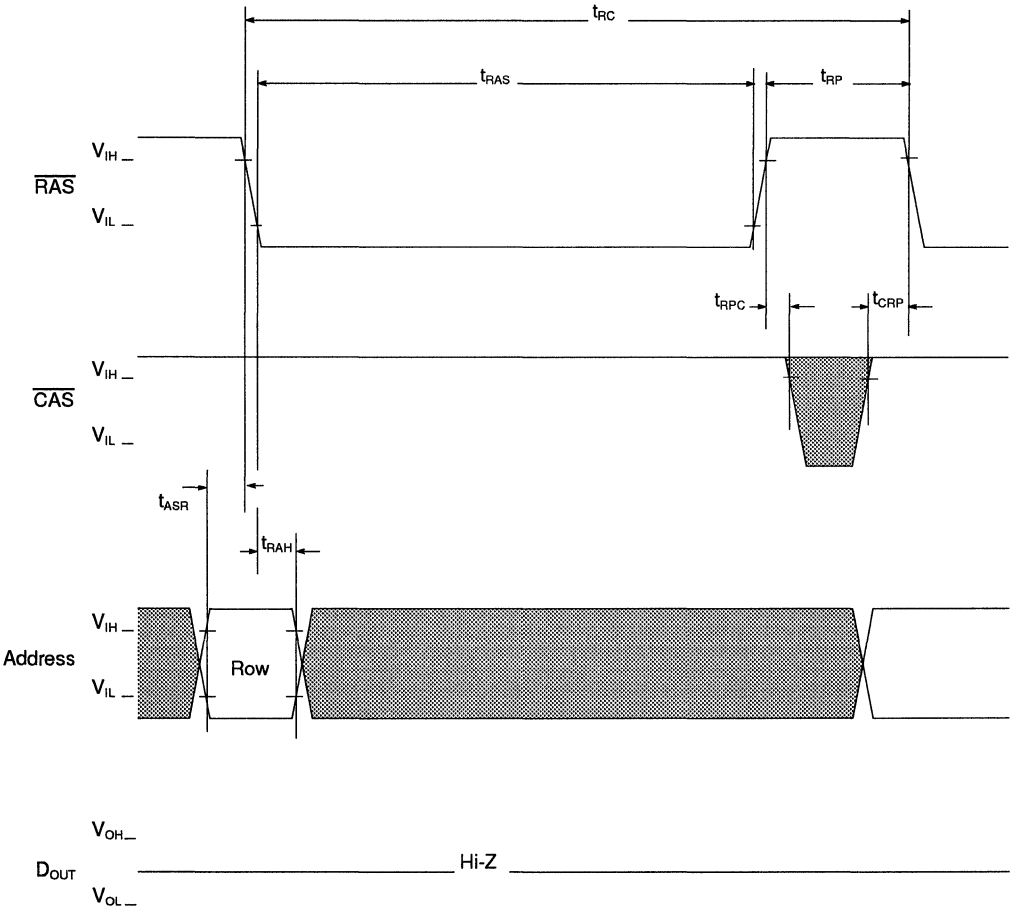
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

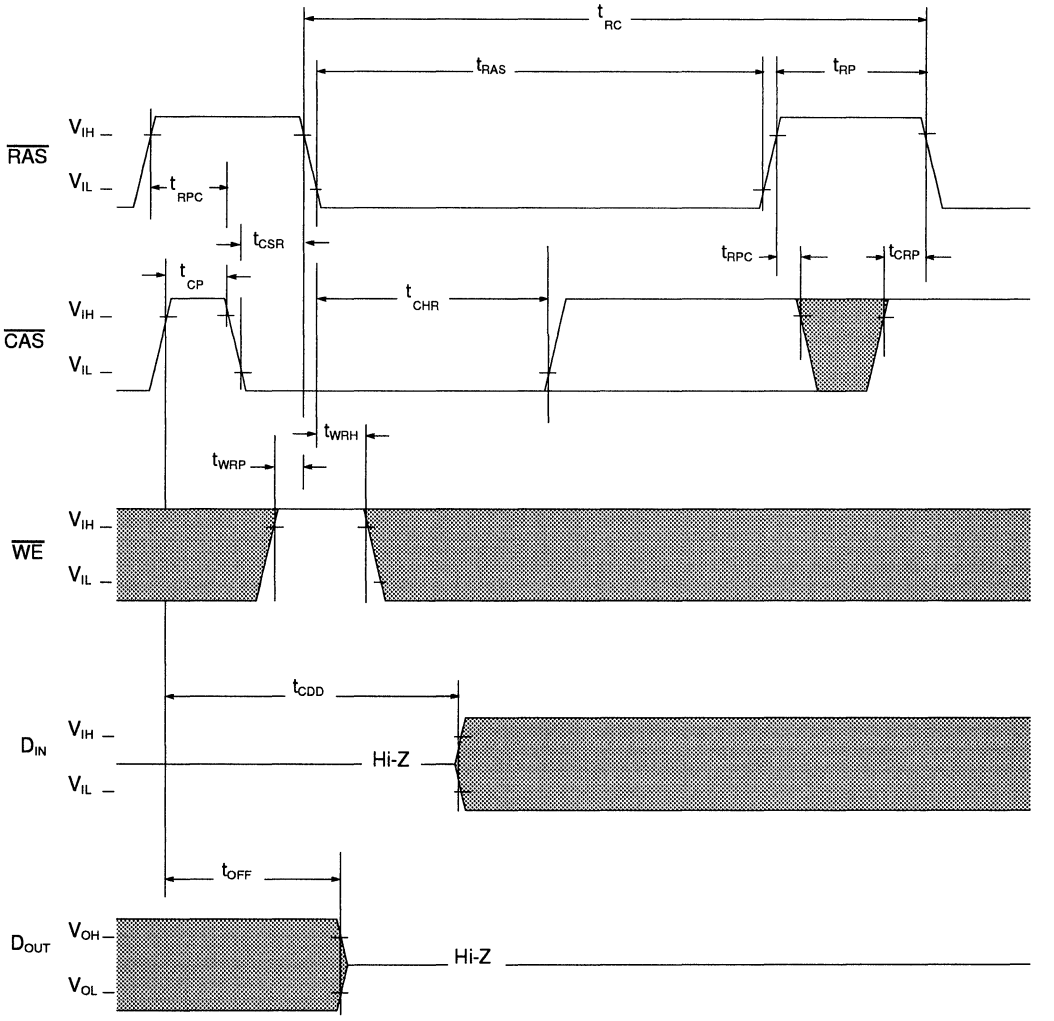


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, D_{IN} are "H" or "L"

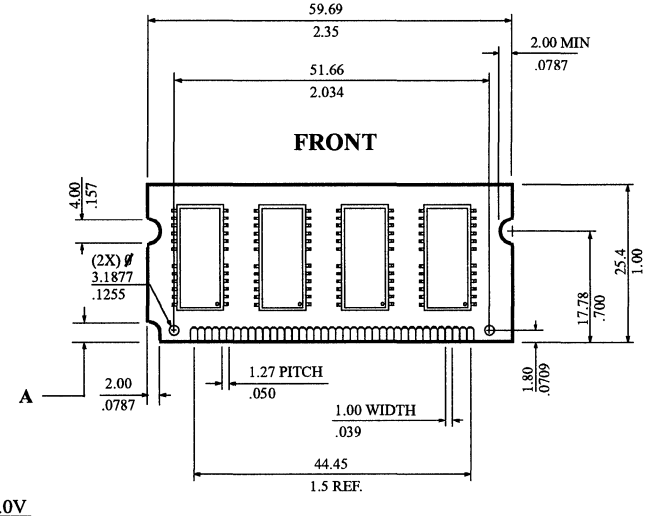
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



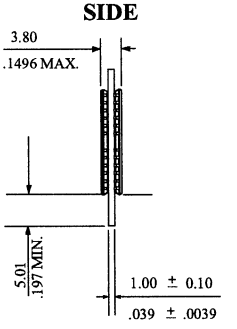
: "H" or "L"

Note: Addresses are "H" or "L"

Layout Drawing



A =	3.3V	5.0V
	3.175 .125	6.35 .246



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

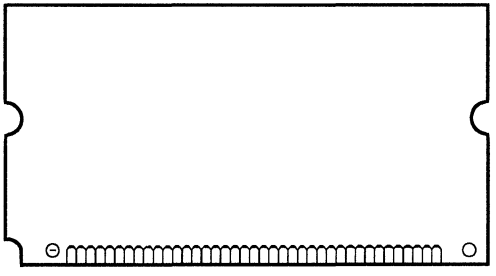
- High Performance CMOS process
- Single 5.0, ± 0.25V Power Supply
- Low active current consumption
- All inputs & outputs are TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, CBR
- 1024 refresh cycles distributed across 128ms
- 10/10 (Redundant Addressing) Addressing (Row/Column)
- Optimized for use in byte-write parity applications.
- Au contacts

Description

The IBM11S1360BL are 4MB 72-pin 4-byte small outline dual in-line memory modules (SODIMM's). The module is organized as a 1Mx36 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 8 1Mx4 and 4 1Mx1 TSOP devices each in a 300mil package. Each bit is uniquely addressed via 20 address bits. This assembly is intended for use in space constrained and or low power applications.

The IBM 72-Pin SODIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint. A related product is the 1Mx32 version with 10/10 addressing IBM11S1320BL.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, PQ17, PQ26, PQ35	Parity Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

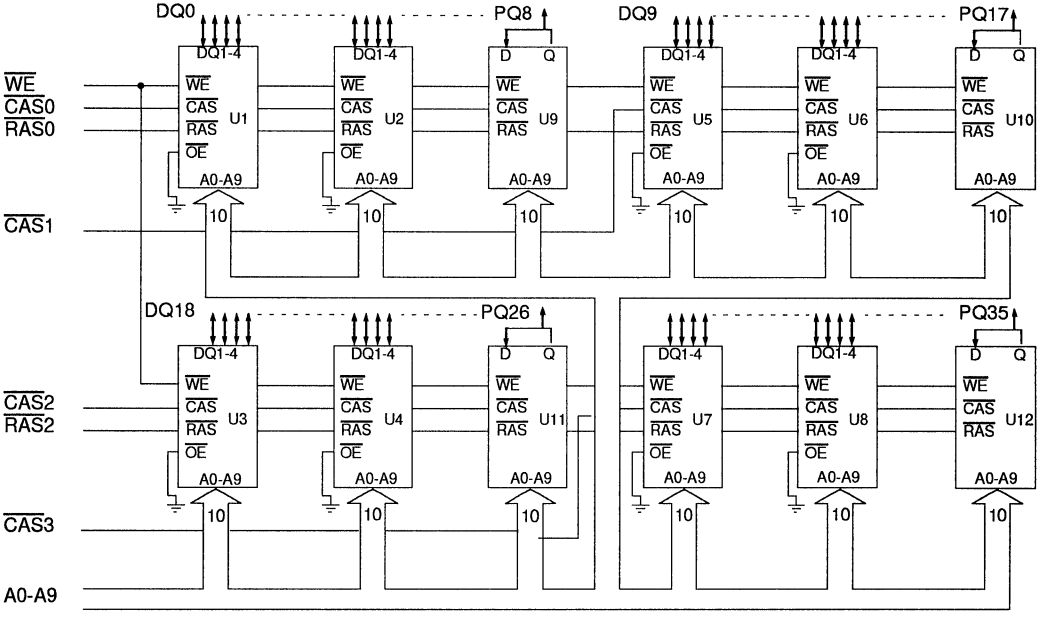
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ23	64	DQ34
5	DQ3	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ24	65	PQ35
6	DQ4	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ25	66	PD2
7	DQ5	19	NC	31	A8	43	$\overline{CAS1}$	55	PQ26	67	PD3
8	DQ6	20	PQ8	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{RAS2}$	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{WE}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	PQ17	48	NC	60	DQ30	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Power
IBM11S1360BLA-60	1M x 36	60ns	Au	2.35" x 1.25" x .1496"	5.0V
IBM11S1360BLA-70	1M x 36	70ns	Au	2.35" x 1.25" x .1496"	5.0V

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	V_{SS}	V_{SS}
PD3	V_{SS}	V_{SS}
PD4	NC	NC
PD5	NC	V_{SS}
PD6	NC	NC
PD7	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt	5.0 Volt		
V_{CC}	Power Supply Voltage	-0.5 to + 4.6	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.7 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	-55 to +125	°C	1
P_D	Power Dissipation	0.6	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3 Volt			5.0 Volt			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3± 0.3V or 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	82	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	57	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	32	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	80	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	13	pF	
$C_{I/O2}$	Parity Output Capacitance (PQ0, PQ17, PQ26, PQ35)	21	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V or 5.0± 0.25V)

Symbol	Parameter		3.3 Volt Min	3.3 Volt Max	5.0 Volt Min	5.0 Volt Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1880	—	1440	mA	1, 2, 3
		-70	—	1680	—	1280		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	24	—	24	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	1880	—	1440	mA	1, 3
		-70	—	1680	—	1280		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1560	—	1240	mA	1, 2, 3
		-70	—	1360	—	1080		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	2.4	—	2.4	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1040	—	1440	mA	1, 3
		-70	—	920	—	1280		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	-60	+60	µA	
		$\overline{CAS}$	-30	+30	-30	+30		
		All others	-120	+120	-120	+120		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V or 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

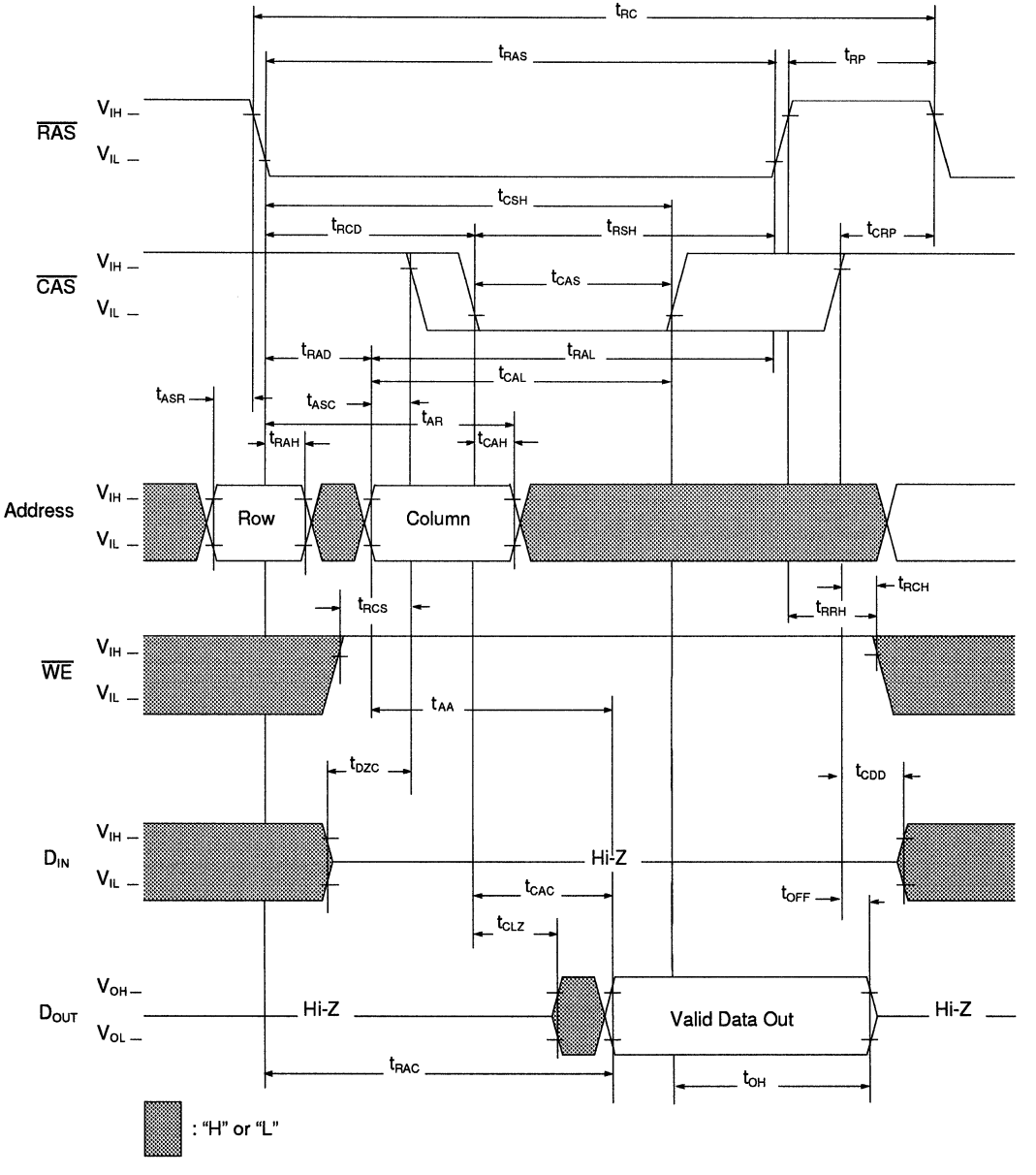
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	256	—	256	ms	1

1. 1024 refreshes are required every 128ms.

Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
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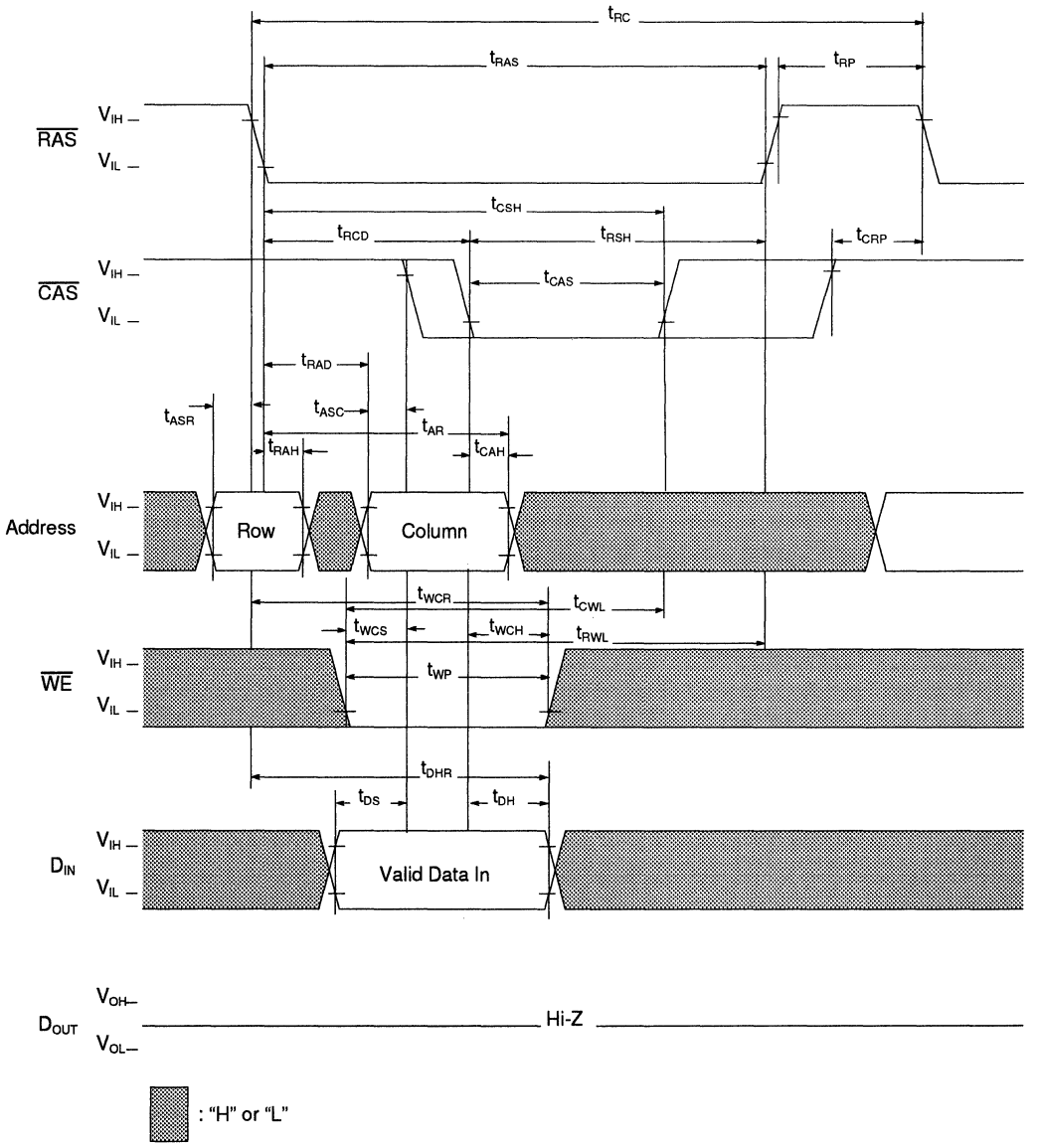
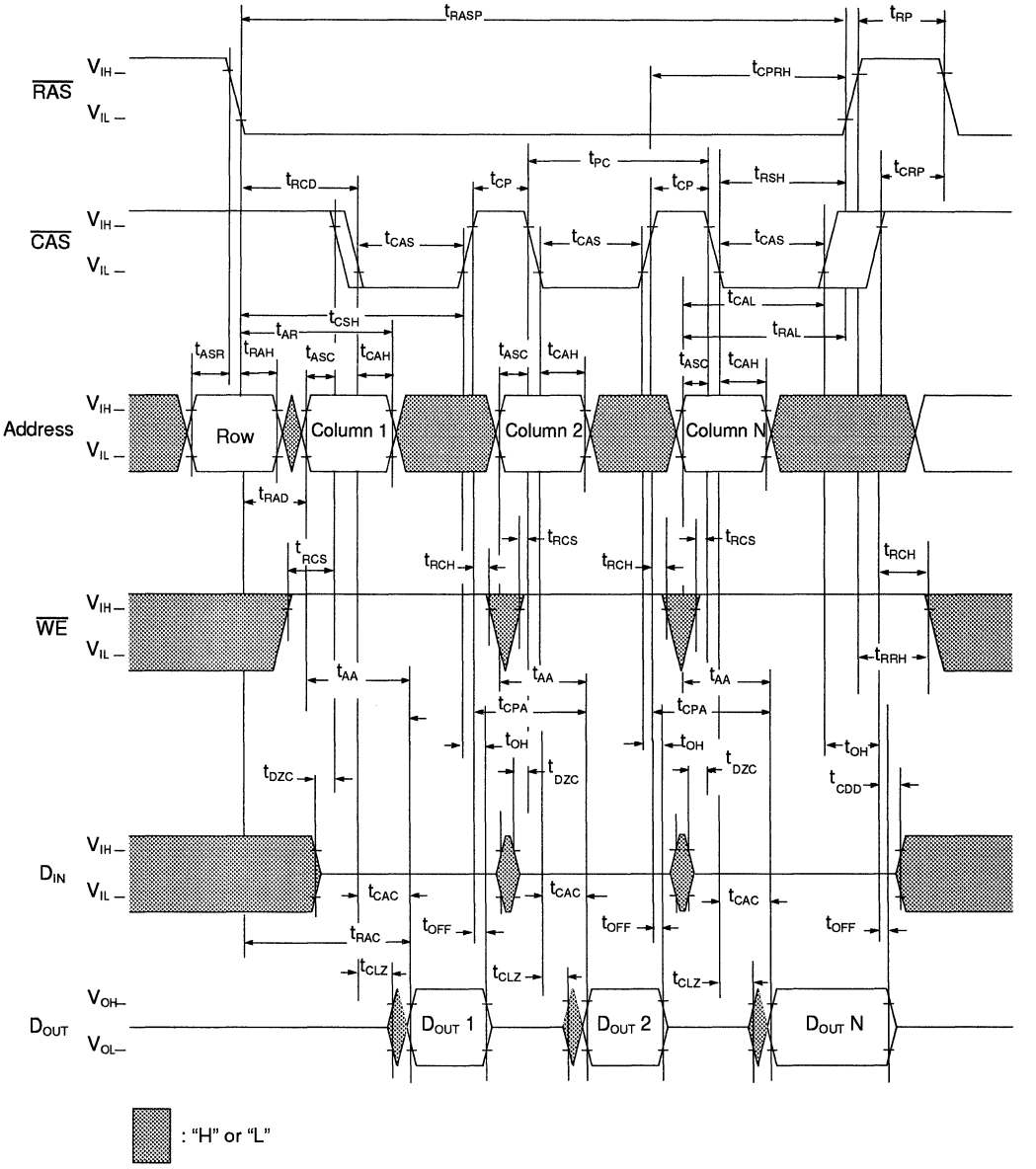
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCH
tRCS
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

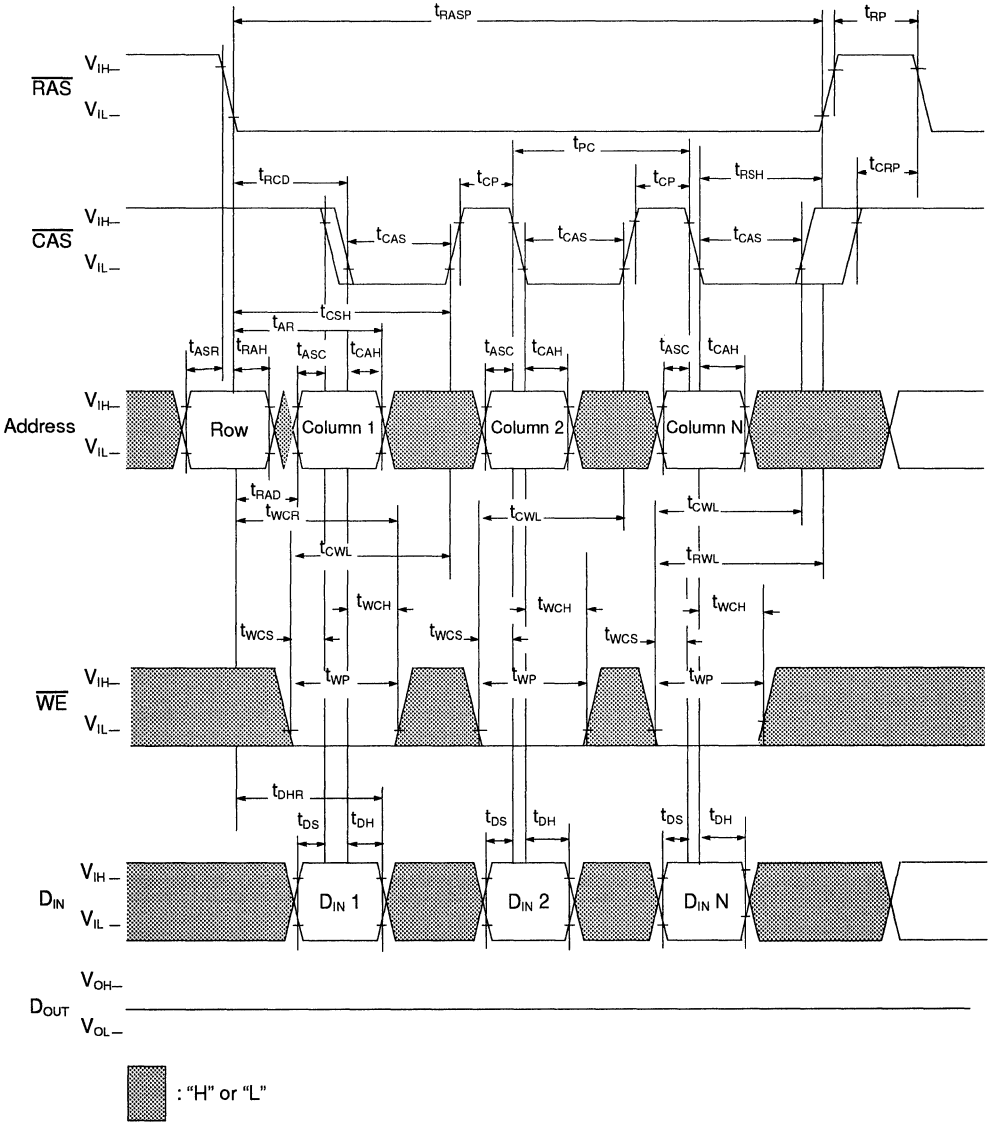
Write Cycle (Early Write)



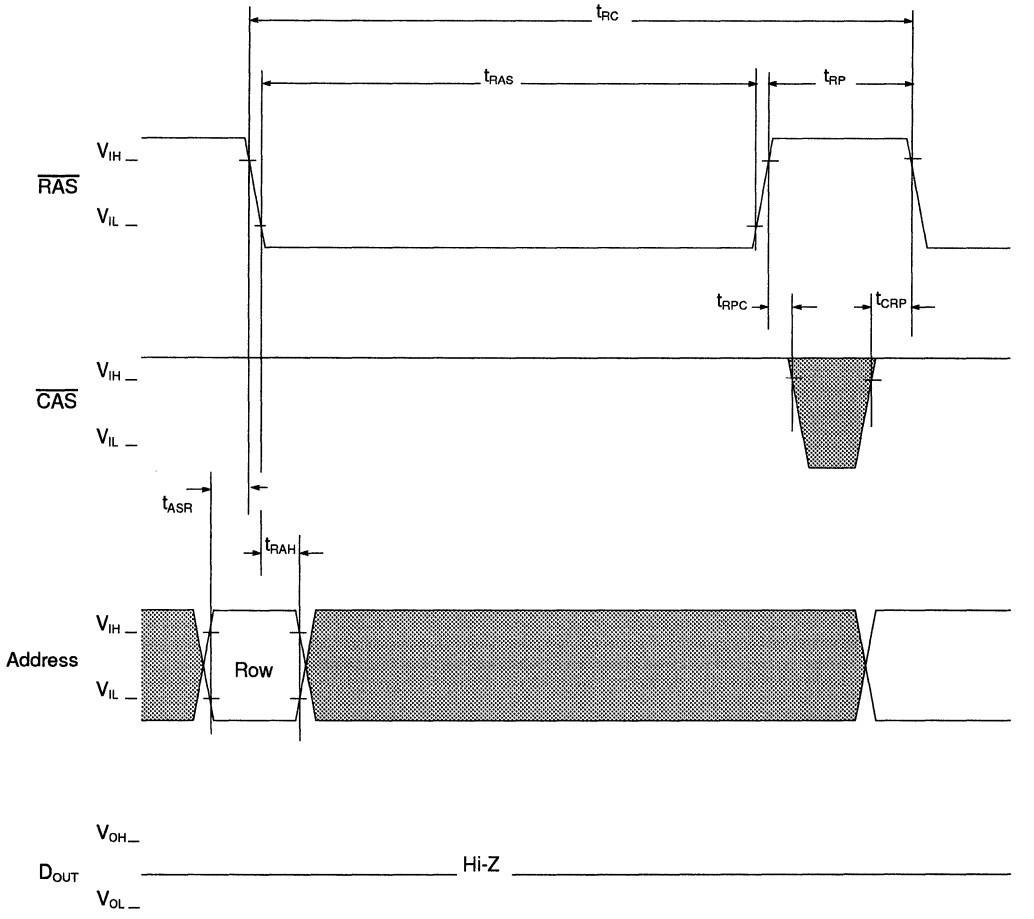
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

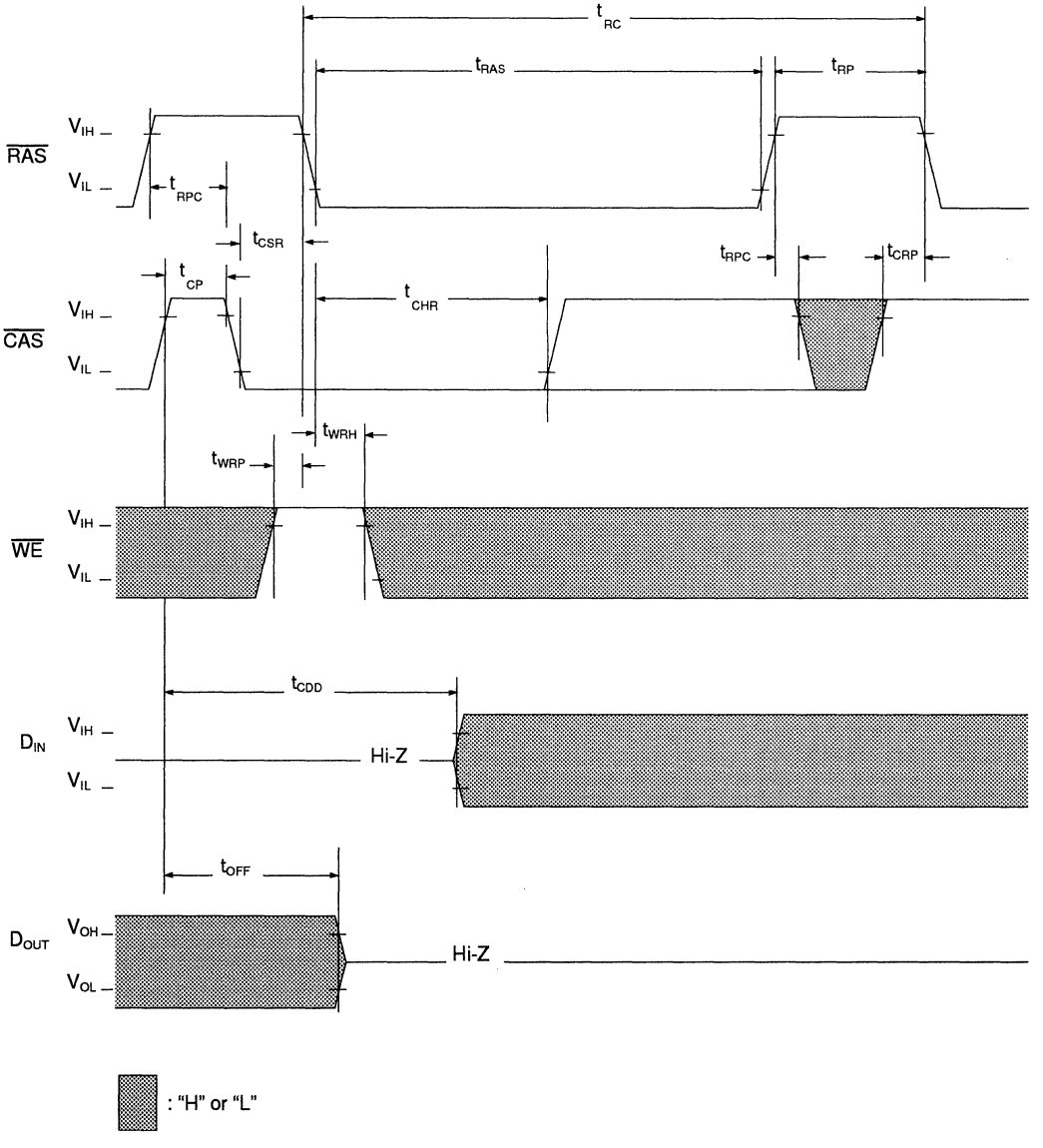


$\overline{RAS}$ Only Refresh Cycle



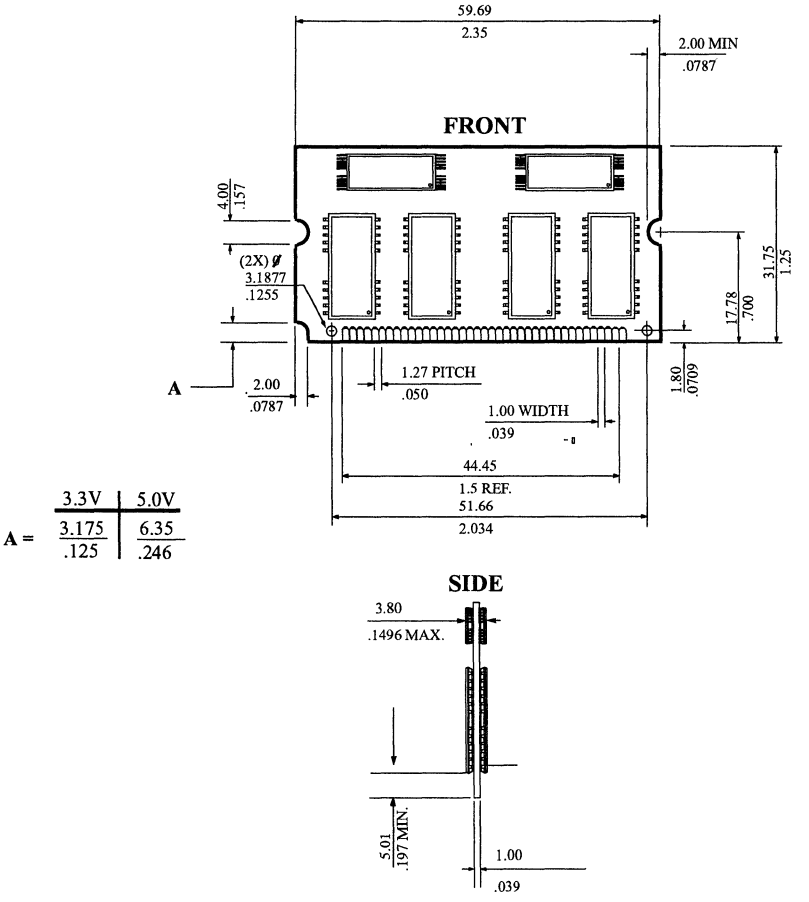
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



A =	3.3V	5.0V
	3.175 / .125	6.35 / .246

NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Single 3.3, ± 0.3V or 5.0, ± 0.25V Power Supply
- Low active current consumption
- All inputs & outputs are TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 4096 refresh cycles distributed across 256ms
- 12/8 Addressing (Row/Column)
- Optimized for use in byte-write parity applications.
- Au contacts

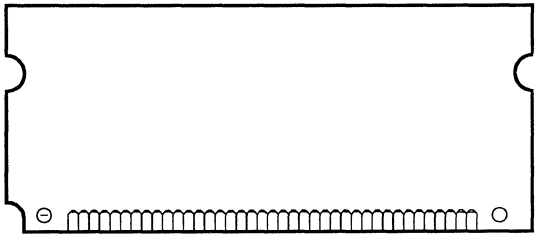
Description

The IBM11S1360NN/L are 4MB industry standard 72-pin 4-byte small outline dual in-line memory modules (SODIMM's). The module is organized as a 1Mx36 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 2 1Mx18 TSOP devices, each in a 400mil package

This assembly is intended for use in space constrained and or low power applications. It utilizes 12/8 address 16m bit technology to further reduce power consumption.

The IBM 72-Pin SODIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint. Related products include the 1Mx32 version with 12/8 addressing IBM11S1320NN/L as well as a 1Mx32 version with 10/10 addressing IBM11S1320BN/L.

Card Outline



(Front) 1 71
(Back) 2 72

Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A12	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, PQ17,PQ26,PQ35	Parity Data Input/output
V_{CC}	Power (+3.3V or +5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

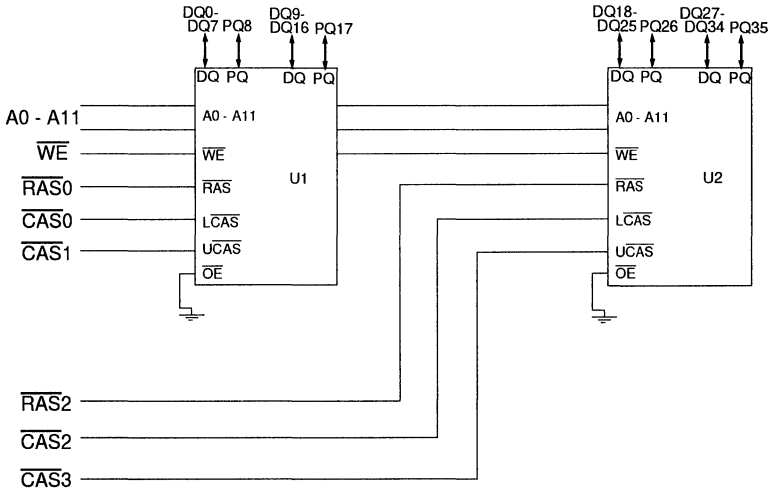
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ23	64	DQ34
5	DQ3	17	A5	29	A11	41	$\overline{CAS2}$	53	DQ24	65	PQ35
6	DQ4	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ25	66	PD2
7	DQ5	19	A10	31	A8	43	$\overline{CAS1}$	55	PQ26	67	PD3
8	DQ6	20	PQ8	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{RAS2}$	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{WE}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	PQ17	48	NC	60	DQ30	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Power
IBM11S1360NNA-60	1M x 36	60ns	Au	2.35" x 1" x .0965"	3.3V
IBM11S1360NNA-70	1M x 36	70ns	Au	2.35" x 1" x .0965"	3.3V
IBM11S1360NLA-60	1M x 36	60ns	Au	2.35" x 1" x .0965"	5.0V
IBM11S1360NLA-70	1M x 36	70ns	Au	2.35" x 1" x .0965"	5.0V

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	V_{SS}	V_{SS}
PD3	NC	NC
PD4	NC	NC
PD5	NC	V_{SS}
PD6	NC	NC
PD7	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt	5.0 Volt		
V_{CC}	Power Supply Voltage	-0.5 to + 4.6	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.7 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	-55 to +125	°C	1
P_D	Power Dissipation	0.6	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3 Volt			5.0 Volt			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3± 0.3V or 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	28	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	16	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	28	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	16	pF	
$C_{I/O2}$	Parity Output Capacitance (PQ8, PQ17, PQ26, PQ35)	16	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V or 5.0± 0.25V)

Symbol	Parameter		3.3 Volt		5.0 Volt		Units	Notes
			Min	Max	Min	Max		
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	190	—	190	mA	1, 2, 3
		-70	—	170	—	170		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	4	—	4	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	190	—	190	mA	1, 3
		-70	—	170	—	170		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	150	—	150	mA	1, 2, 3
		-70	—	130	—	130		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	0.4	—	0.4	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	190	—	190	mA	1, 3
		-70	—	170	—	170		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-10	+10	-10	+10	µA	
		$\overline{CAS}$	-10	+10	-10	+10		
		All others	-20	+20	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

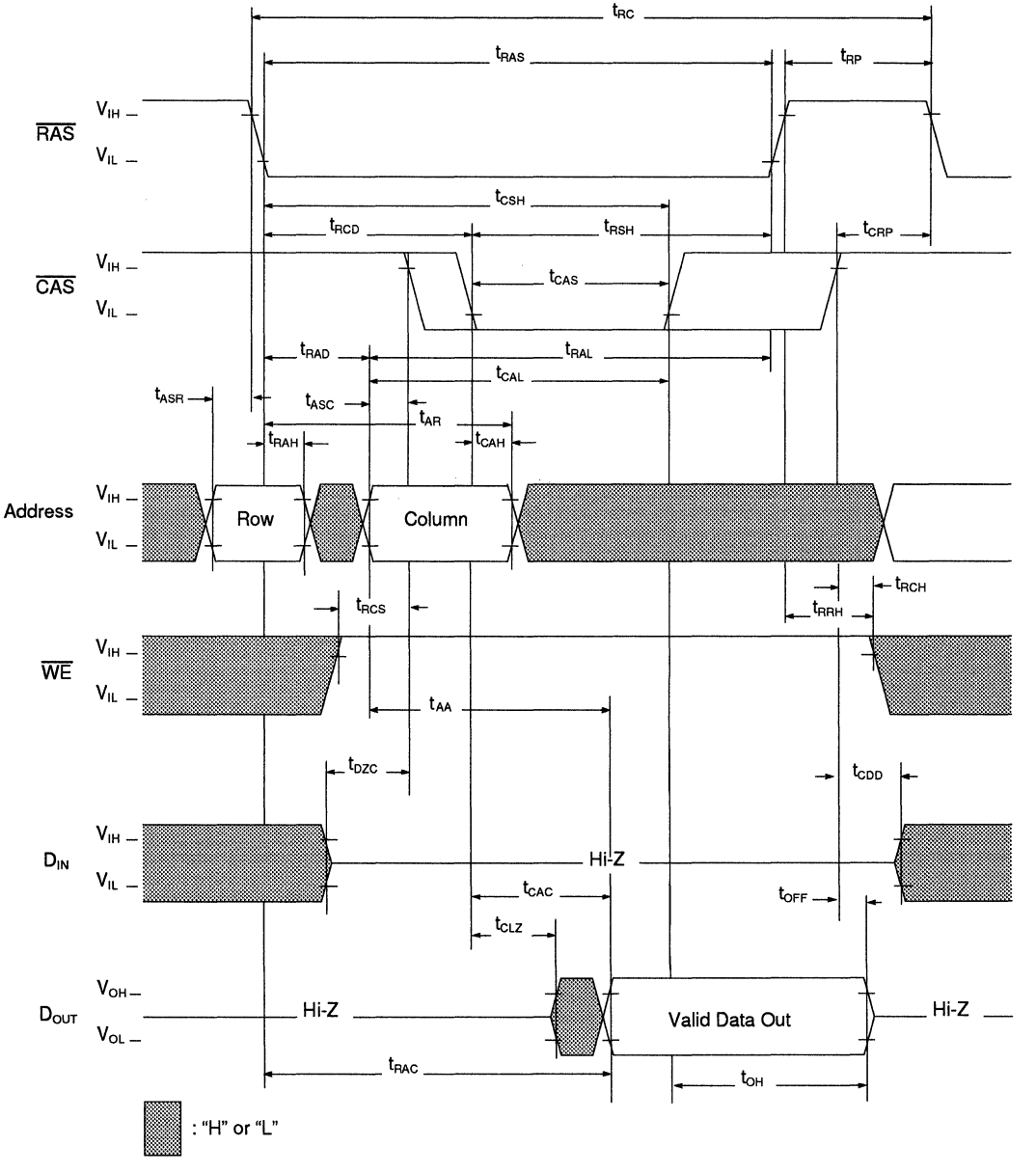
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

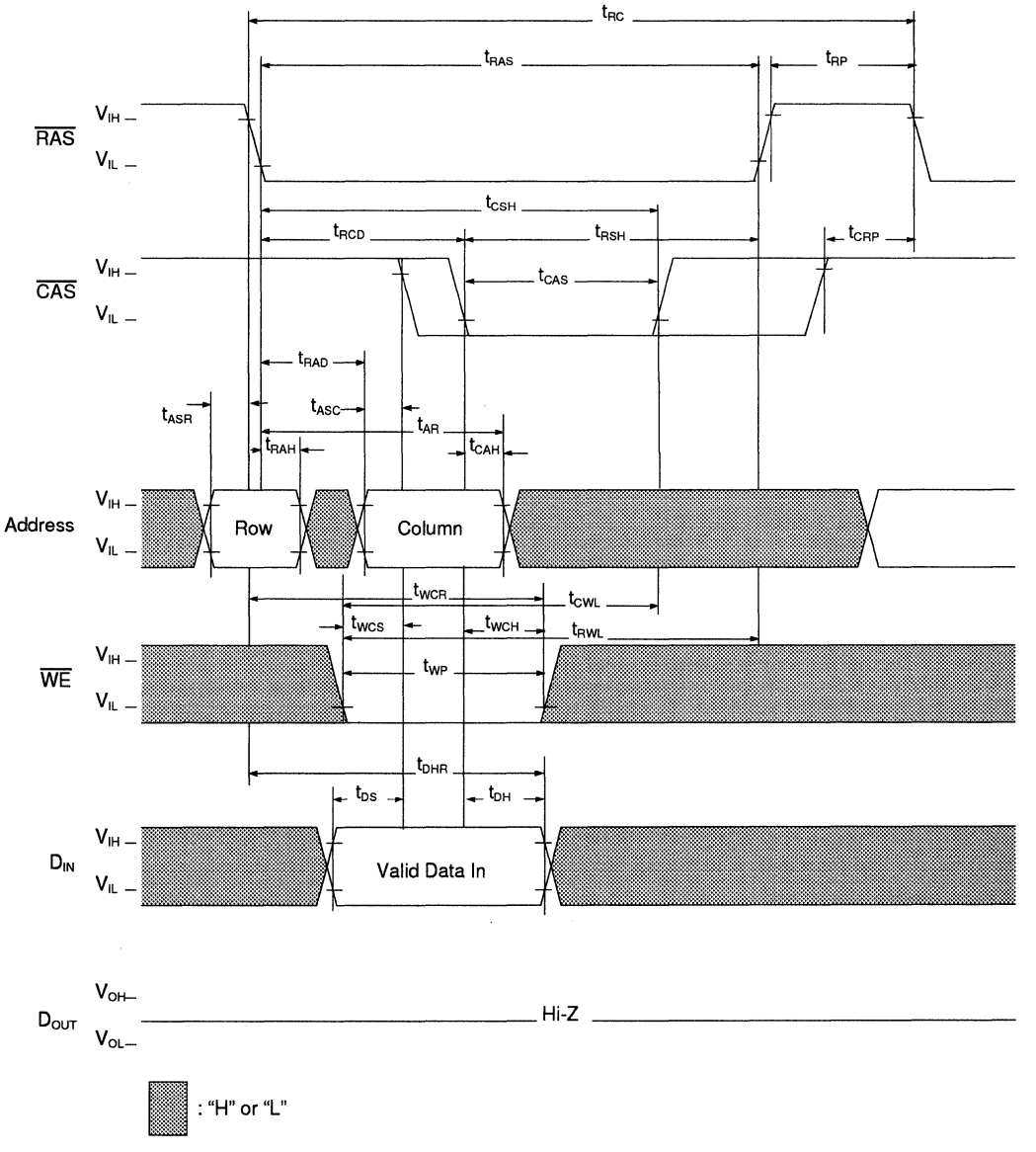
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	256	—	256	ms	1

1. 4096 refreshes are required every 256ms.

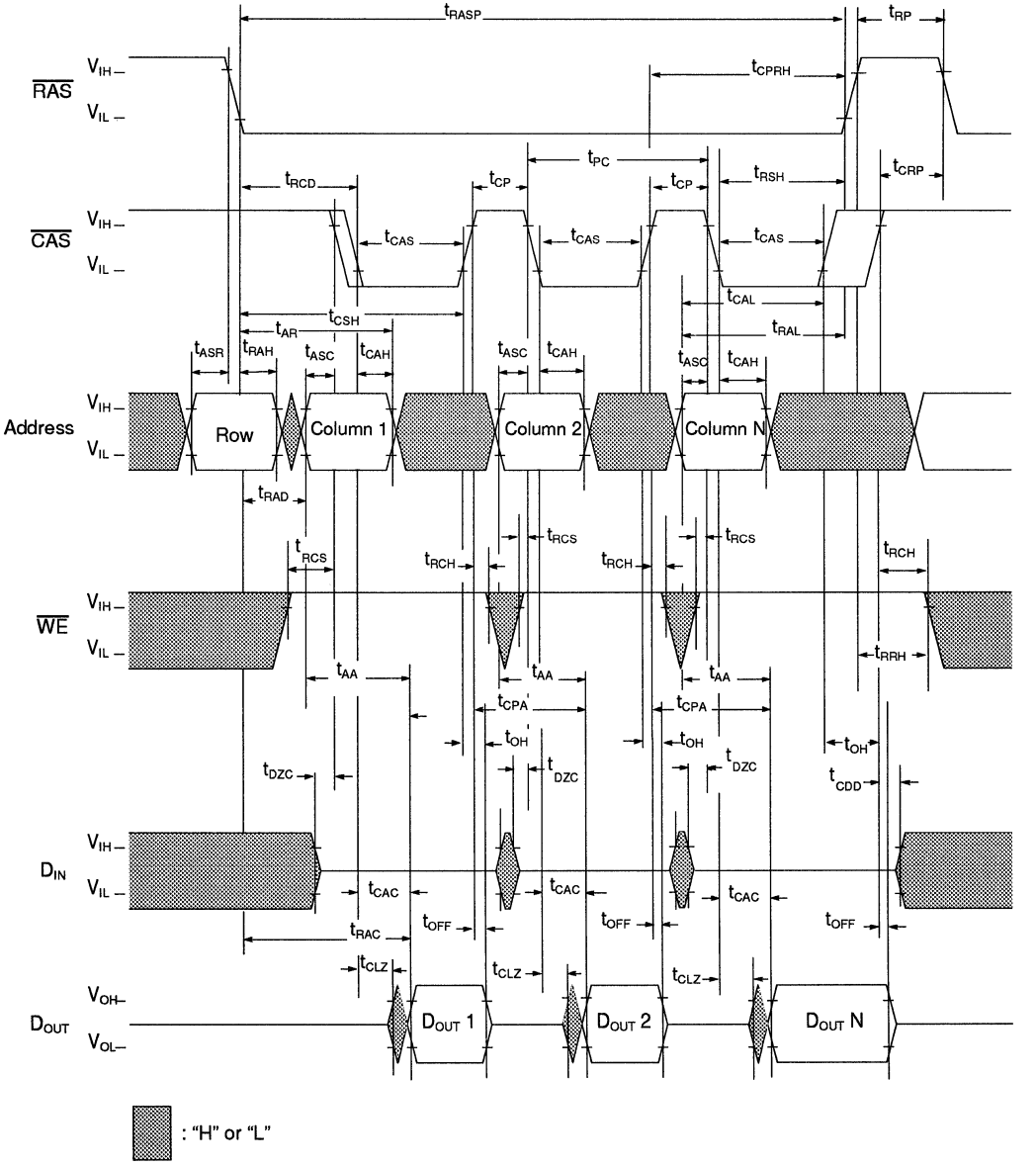
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

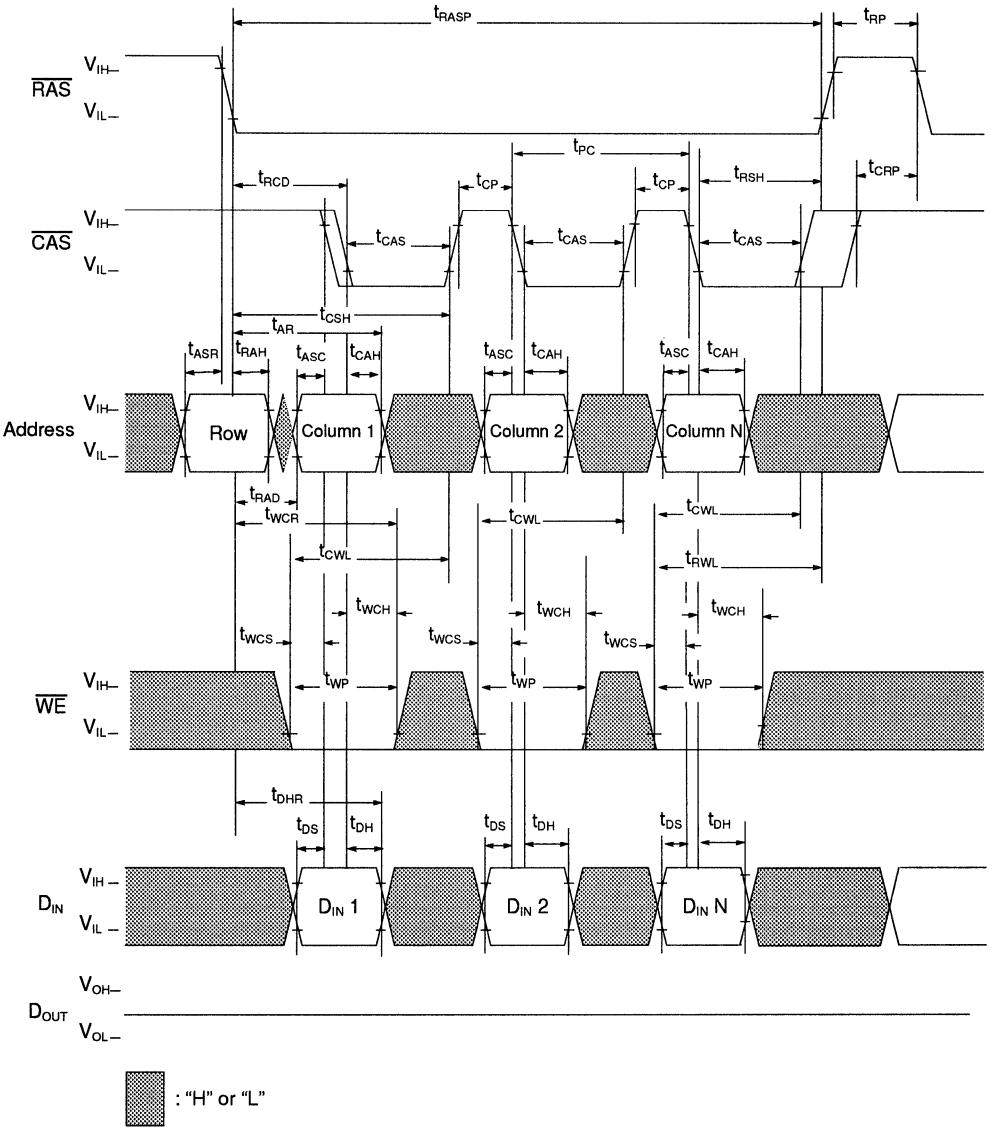
Write Cycle (Early Write)



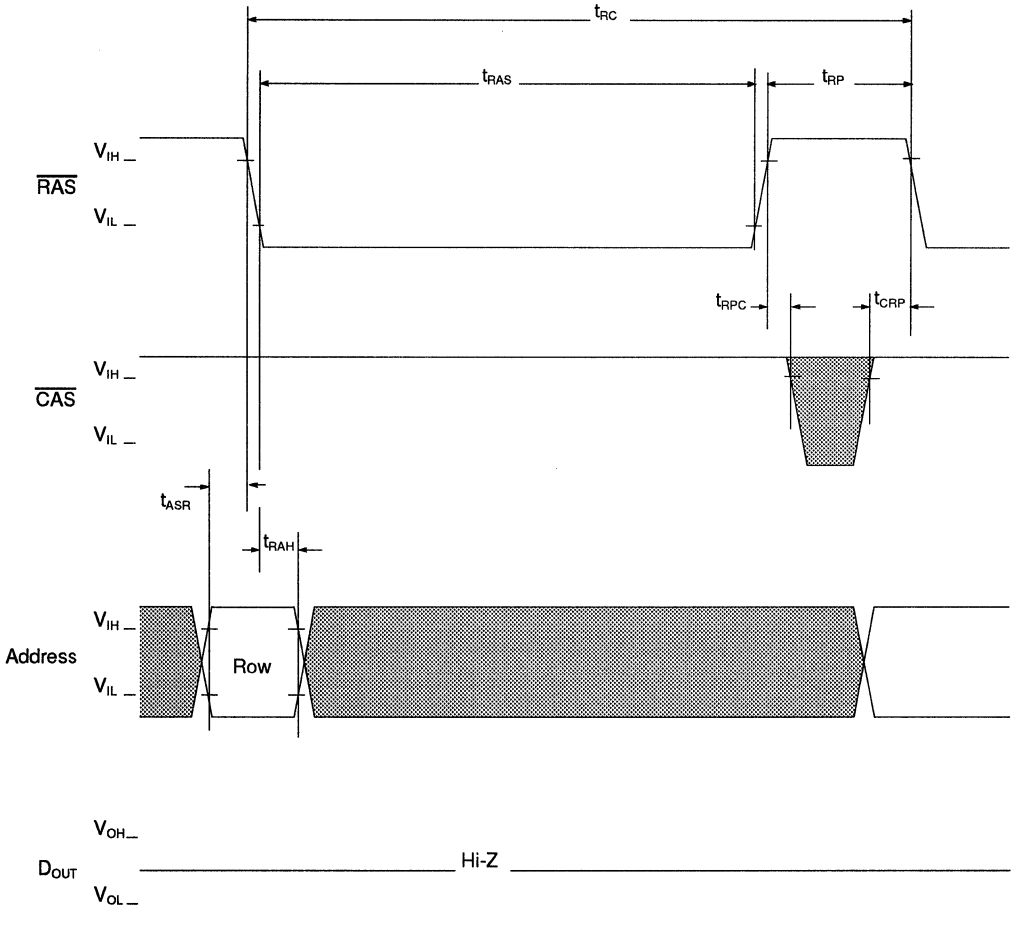
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

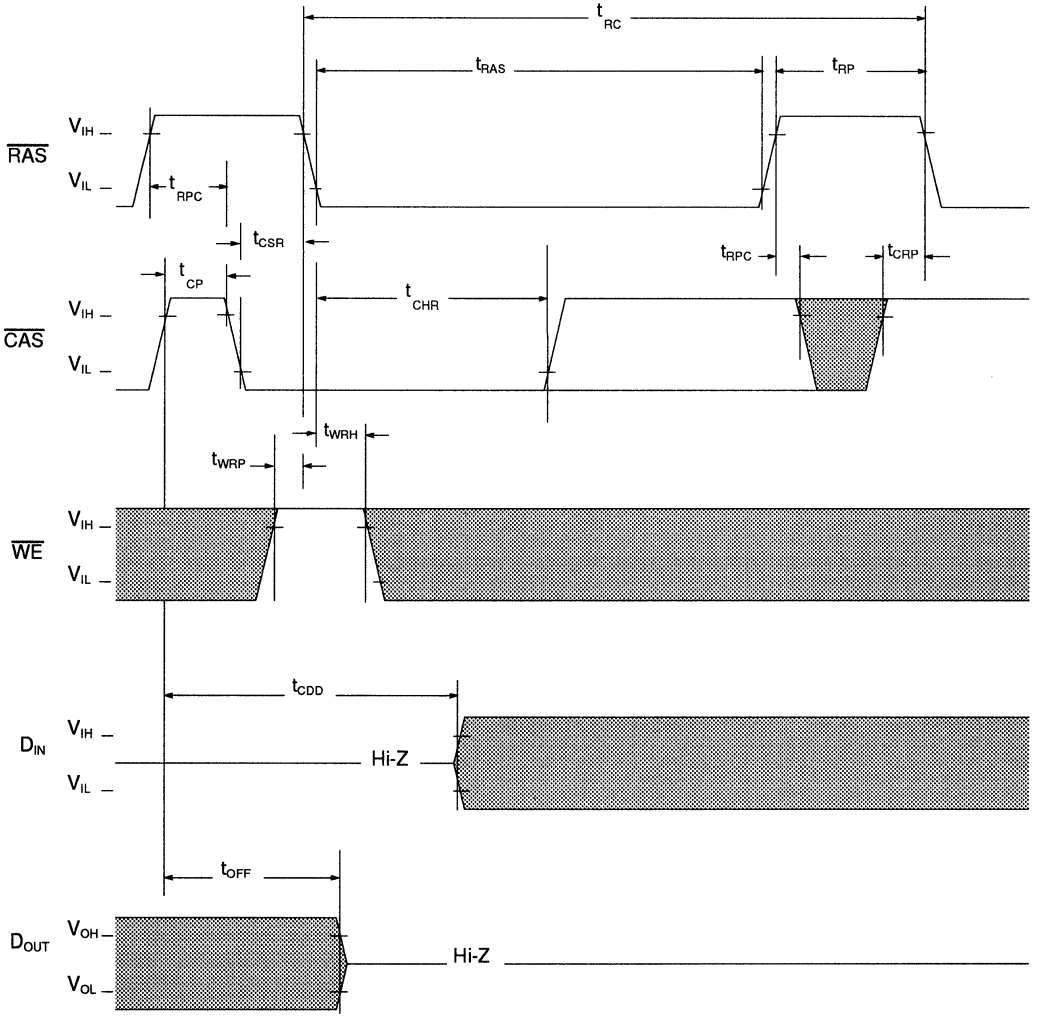


$\overline{RAS}$ Only Refresh Cycle



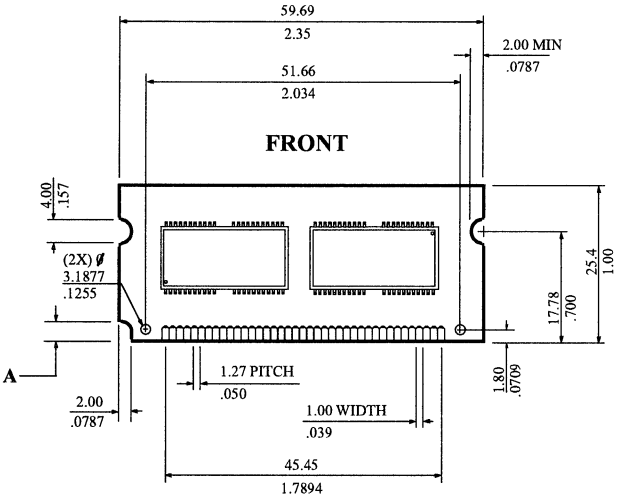
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



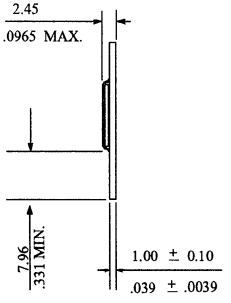
Note: Addresses are "H" or "L"

Layout Drawing



A =	3.3V	5.0V
	3.175 .125	6.35 .246

SIDE



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 36 SODIMM Module

Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Single 3.3, ± 0.3V or 5.0, ± 0.25V Power Supply
- Low active current consumption
- All inputs & outputs are TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 4096 refresh cycles distributed across 256ms
- 12/8 Addressing (Row/Column)
- Optimized for use in byte-write parity applications.
- Au contacts

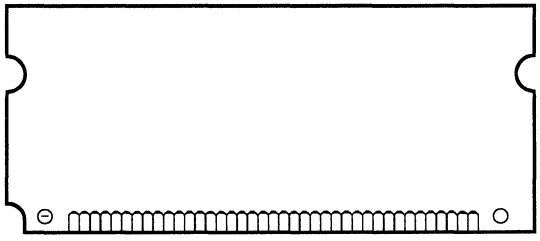
Description

The IBM11S2360NN/L are 8MB industry standard 72-pin 4-byte small outline dual in-line memory modules (SODIMM's). The module is organized as a 2Mx36 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 4 1Mx18 TSOP devices, each in a 400mil package

This assembly is intended for use in space constrained and or low power applications. It utilizes 12/8 address 16m bit technology to further reduce power consumption.

The IBM 72-Pin SODIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint. Related products include the 2Mx32 version with 12/8 addressing IBM11S2320NN/L as well as a 2Mx32 version with 11/10 addressing IBM11S2320HN/L

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A12	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, PQ17,PQ26,PQ35	Parity Data Input/output
V_{CC}	Power (+3.3V or +5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

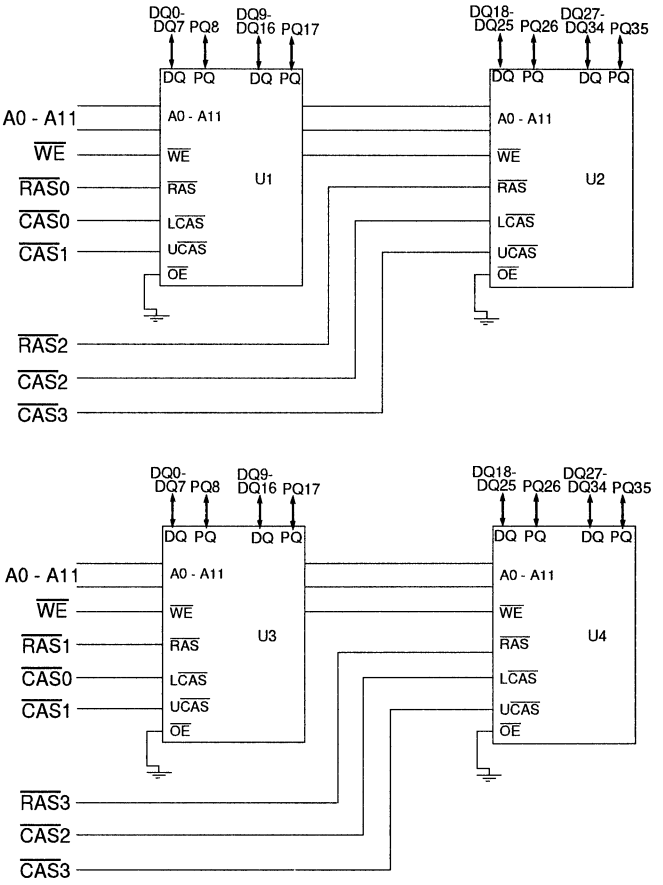
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ23	64	DQ34
5	DQ3	17	A5	29	A11	41	$\overline{CAS2}$	53	DQ24	65	PQ35
6	DQ4	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ25	66	PD2
7	DQ5	19	A10	31	A8	43	$\overline{CAS1}$	55	PQ26	67	PD3
8	DQ6	20	PQ8	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{RAS2}$	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{WE}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	PQ17	48	NC	60	DQ30	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Power
IBM11S2360NNA-60	2M x 36	60ns	Au	2.35" x 1" x .1496"	3.3V
IBM11S2360NNA-70	2M x 36	70ns	Au	2.35" x 1" x .1496"	3.3V
IBM11S2360NLA-60	2M x 36	60ns	Au	2.35" x 1" x .1496"	5.0V
IBM11S2360NLA-70	2M x 36	70ns	Au	2.35" x 1" x .1496"	5.0V

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	V_{SS}	V_{SS}
PD3	NC	NC
PD4	V_{SS}	V_{SS}
PD5	NC	V_{SS}
PD6	NC	NC
PD7	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt	5.0 Volt		
V_{CC}	Power Supply Voltage	-0.5 to + 4.6	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.7 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	-55 to +125	°C	1
P_D	Power Dissipation	0.6	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3 Volt			5.0 Volt			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3± 0.3V or 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	38	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	16	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	22	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	42	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	23	pF	
$C_{I/O2}$	Parity Output Capacitance (PQ8, PQ17, PQ26, PQ35)	23	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V or 5.0± 0.25V)

Symbol	Parameter		3.3 Volt		5.0 Volt		Units	Notes
			Min	Max	Min	Max		
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	190	—	190	mA	1, 2, 3
		-70	—	170	—	170		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	8	—	8	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	190	—	190	mA	1, 3
		-70	—	170	—	170		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	150	—	150	mA	1, 2, 3
		-70	—	130	—	130		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	0.8	—	0.8	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	190	—	190	mA	1, 3
		-70	—	170	—	170		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-10	+10	-10	+10	µA	
		$\overline{CAS}$	-20	+20	-20	+20		
		All others	-40	+40	-40	+40		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

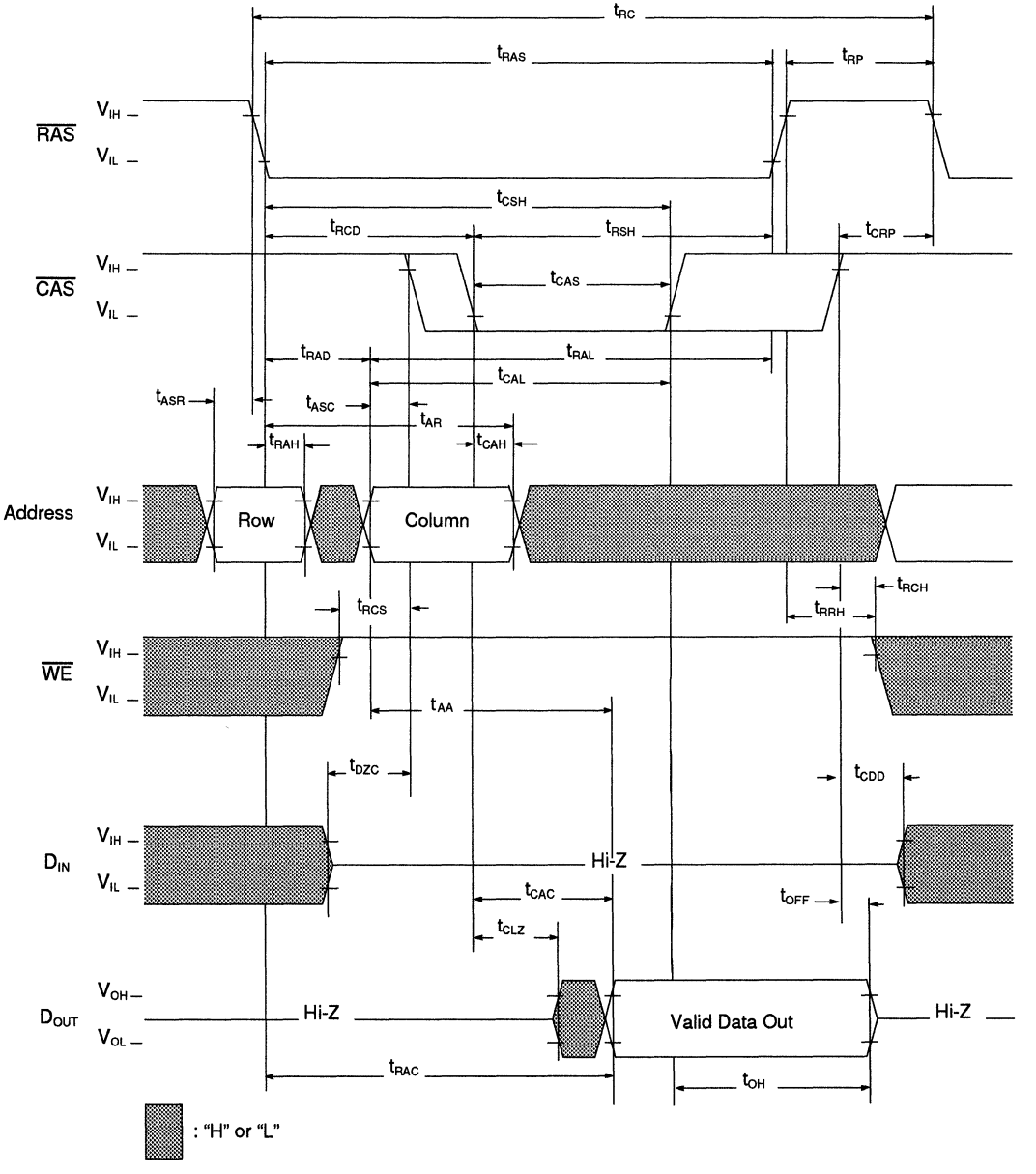
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

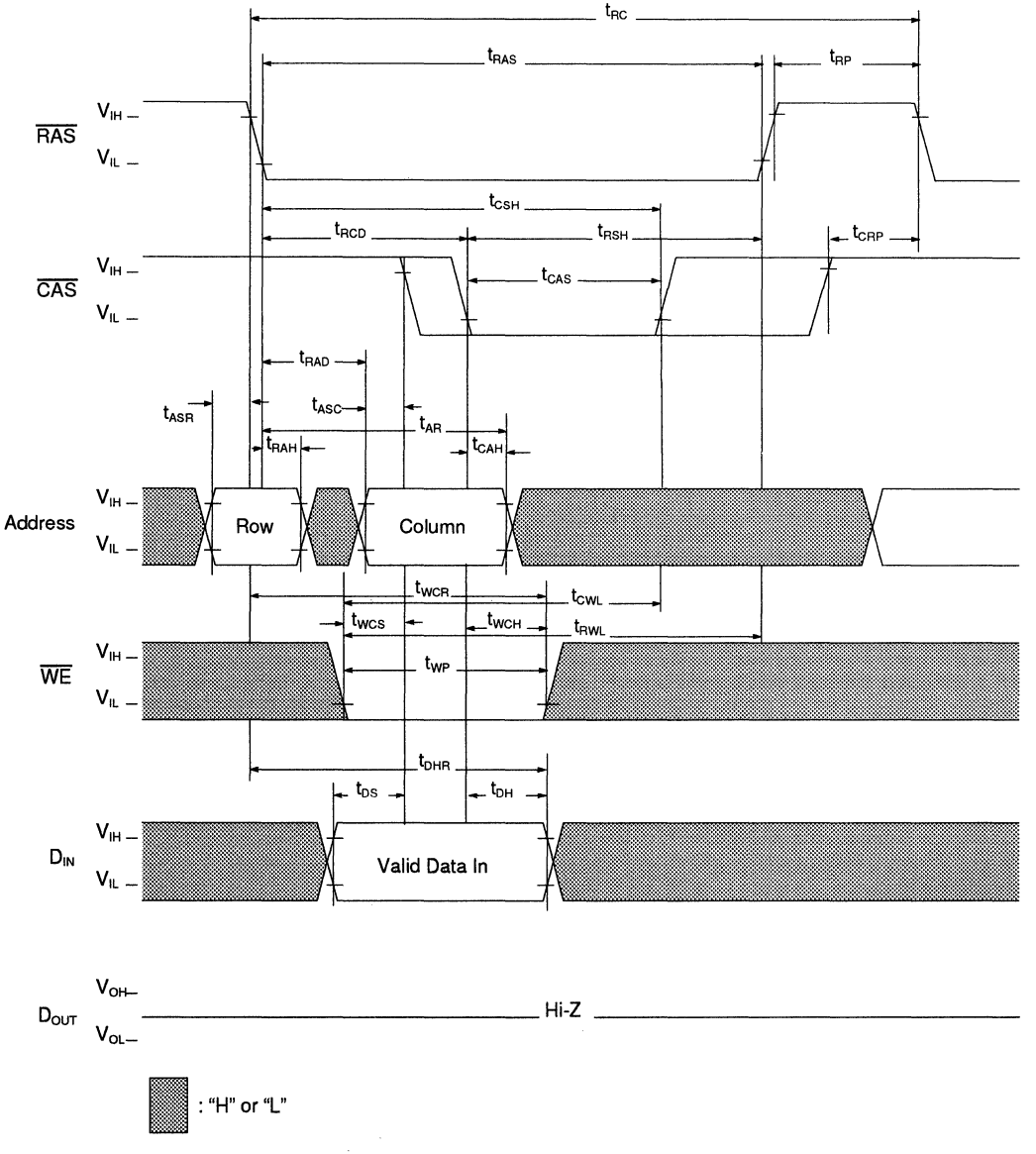
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	256	—	256	ms	1

1. 4096 refreshes are required every 256ms.

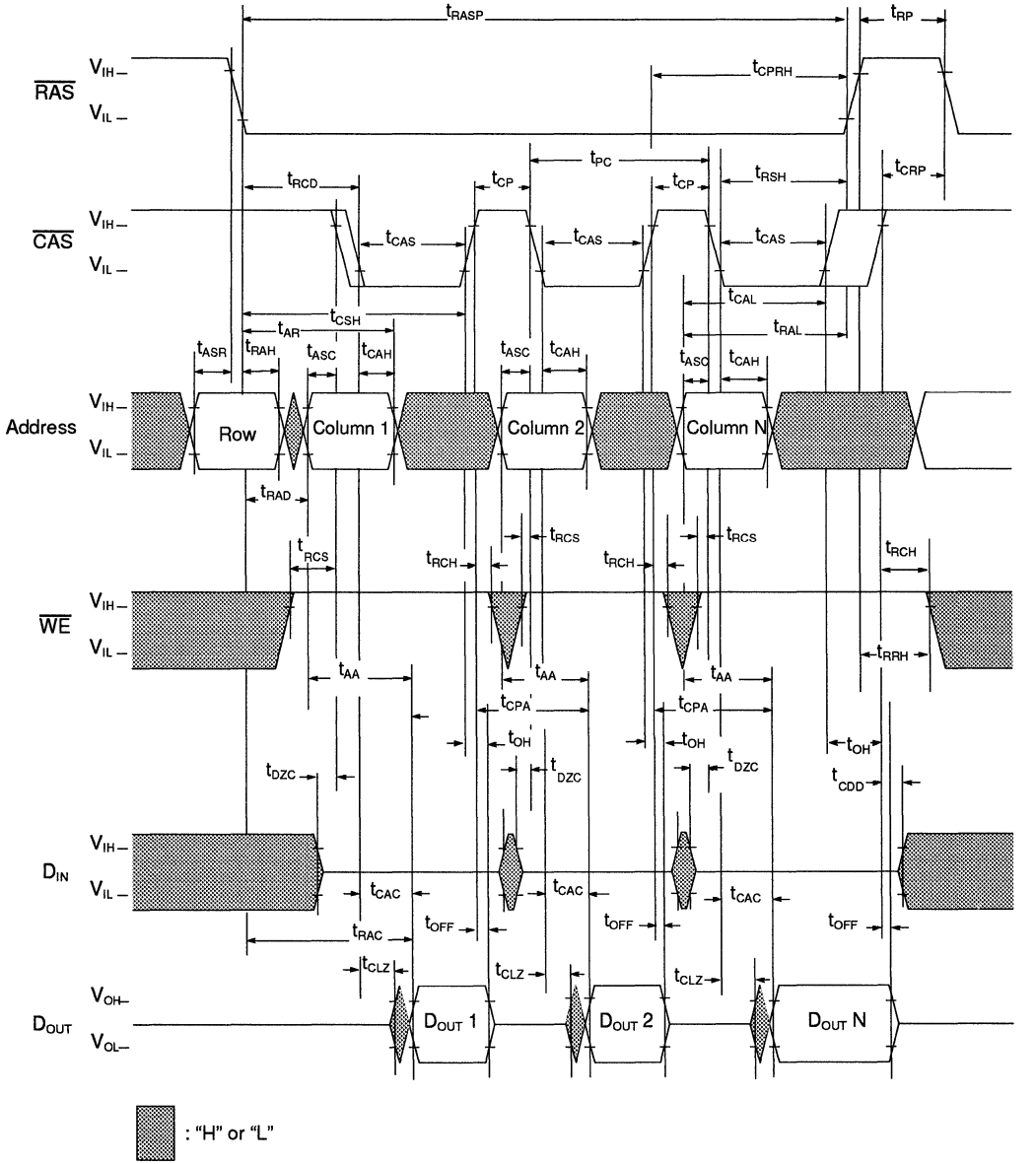
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

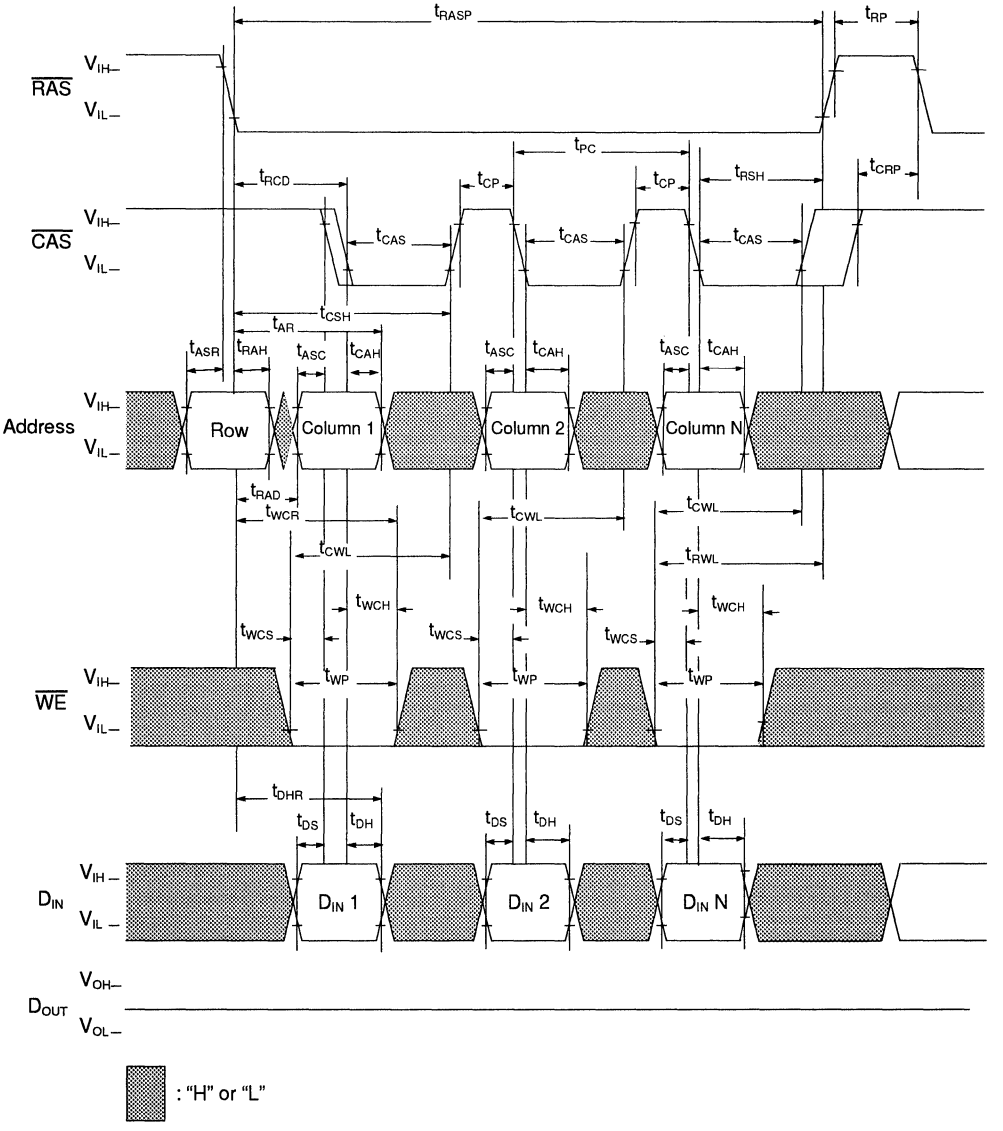
Write Cycle (Early Write)



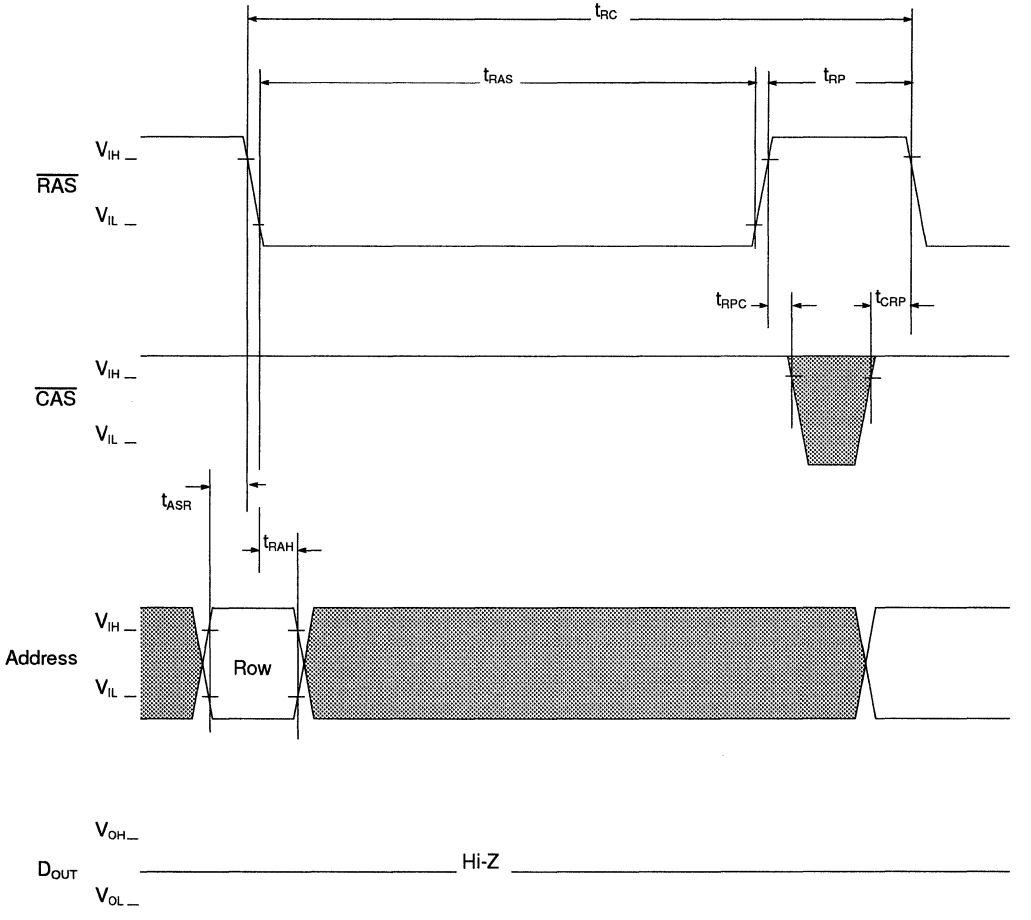
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

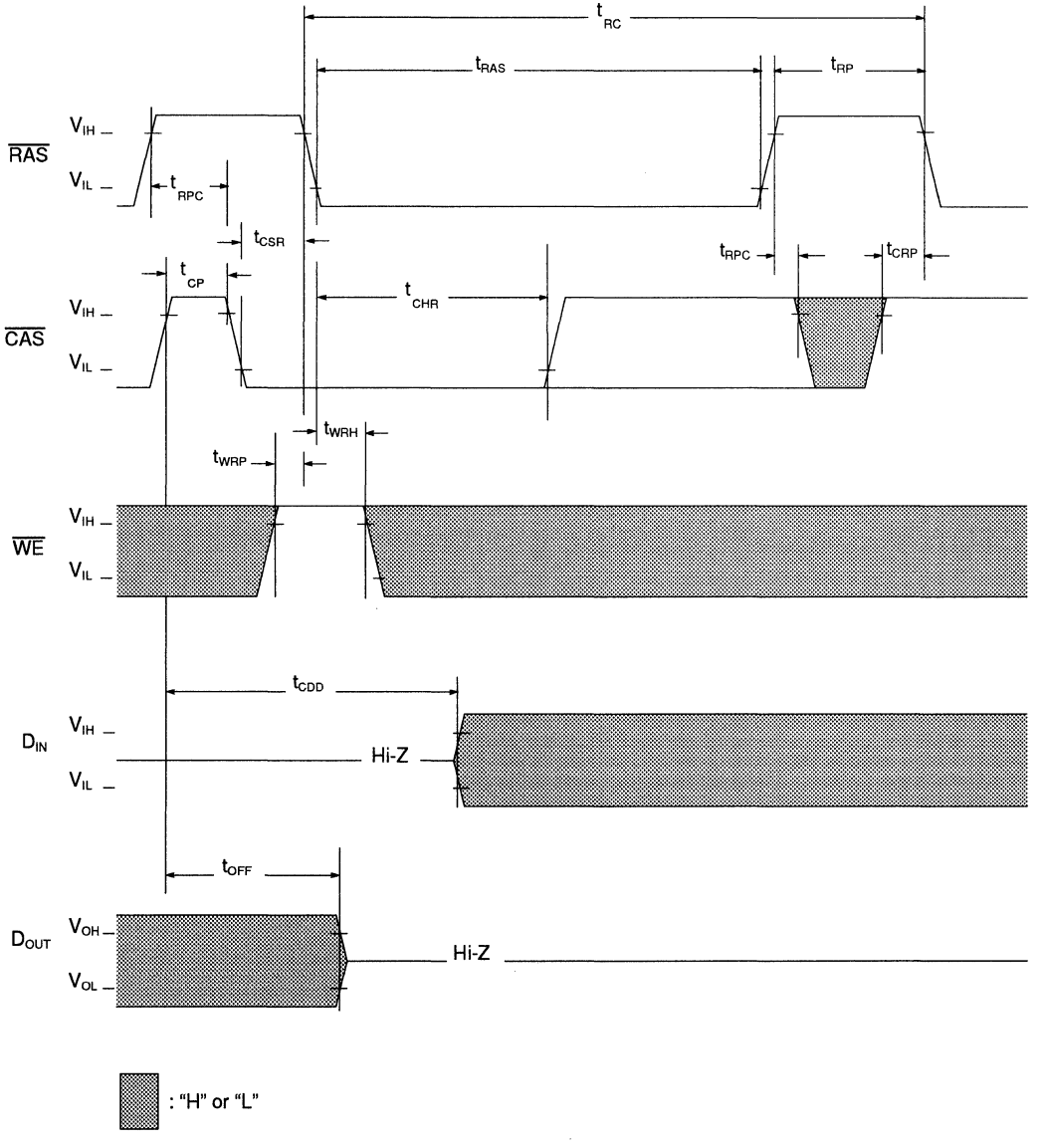


$\overline{RAS}$ Only Refresh Cycle



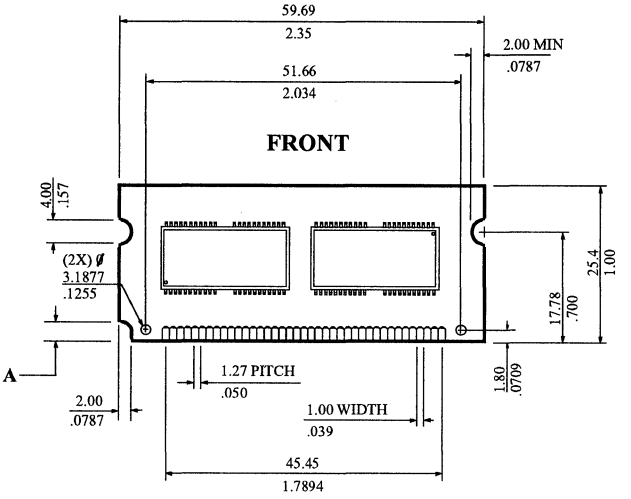
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

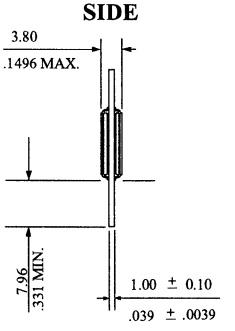


Note: Addresses are "H" or "L"

Layout Drawing



A =	3.3V	5.0V
	3.175	6.35
	.125	.246



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

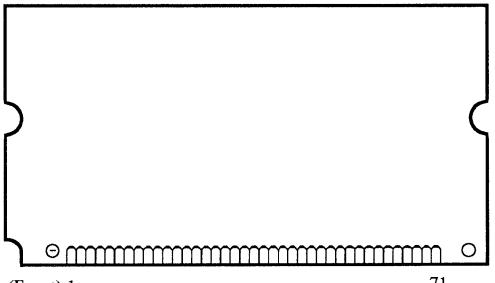
- High Performance CMOS process
- Single 3.3, ± 0.3V or 5.0, ± 0.25V Power Supply
- Low active current consumption
- All inputs & outputs are TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, CBR
- 2048 refresh cycles distributed across 256ms
- 11/11 (Redundant Addressing) Addressing (Row/Column)
- Optimized for use in byte-write parity applications.
- Au contacts

Description

The IBM11S4360BN/L are 16MB 72-pin 4-byte small outline dual in-line memory modules (SODIMM's). The module is organized as a 4Mx36 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 8 4Mx4 and 4 4Mx1 TSOP devices each in a 300mil package. Each bit is uniquely addressed via 22 address bits. This assembly is intended for use in space constrained and or low power applications.

The IBM 72-Pin SODIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint. Related products include the 4Mx32 version with 12/10 addressing IBM11S4320CN/L as well as the 4Mx36 version with 12/11 addressing IBM11S4360DN/L.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, PQ17, PQ26, PQ35	Parity Data Input/output
V_{CC}	Power (+3.3V or +5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

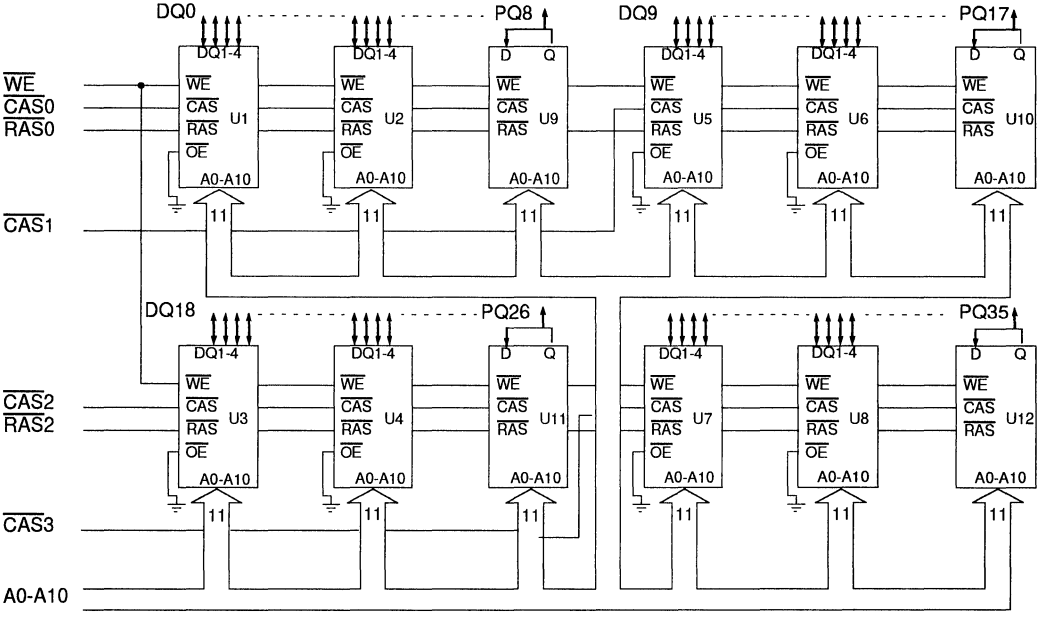
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ23	64	DQ34
5	DQ3	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ24	65	PQ35
6	DQ4	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ25	66	PD2
7	DQ5	19	A10	31	A8	43	$\overline{CAS1}$	55	PQ26	67	PD3
8	DQ6	20	PQ8	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{RAS2}$	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{WE}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	PQ17	48	NC	60	DQ30	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Power
IBM11S4360BNA-60	4M x 36	60ns	Au	2.35" x 1.25" x .1496"	3.3V
IBM11S4360BNA-70	4M x 36	70ns	Au	2.35" x 1.25" x .1496"	3.3V
IBM11S4360BLA-60	4M x 36	60ns	Au	2.35" x 1.25" x .1496"	5.0V
IBM11S4360BLA-70	4M x 36	70ns	Au	2.35" x 1.25" x .1496"	5.0V

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	NC	NC
PD3	V_{SS}	V_{SS}
PD4	NC	NC
PD5	NC	V_{SS}
PD6	NC	NC
PD7	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
		5.0 Volt		
V_{CC}	Power Supply Voltage	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	5.0 Volt			Units	Notes
		Min	Typ	Max		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	82	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	57	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	32	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	80	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	13	pF	
$C_{I/O2}$	Parity Output Capacitance (PQ8, PQ17, PQ26, PQ35)	21	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0± 0.25V)

Symbol	Parameter		5.0 Volt Min	5.0 Volt Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1440	mA	1, 2, 3
		-70	—	1280		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})	24	—	24	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	1440	mA	1, 3
		-70	—	1280		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1240	mA	1, 2, 3
		-70	—	1080		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)	2.4	—	2.4	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1440	mA	1, 3
		-70	—	1280		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$	-30	+30		
		All others	-120	+120		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})	-10	-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)	2.4	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)	—	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

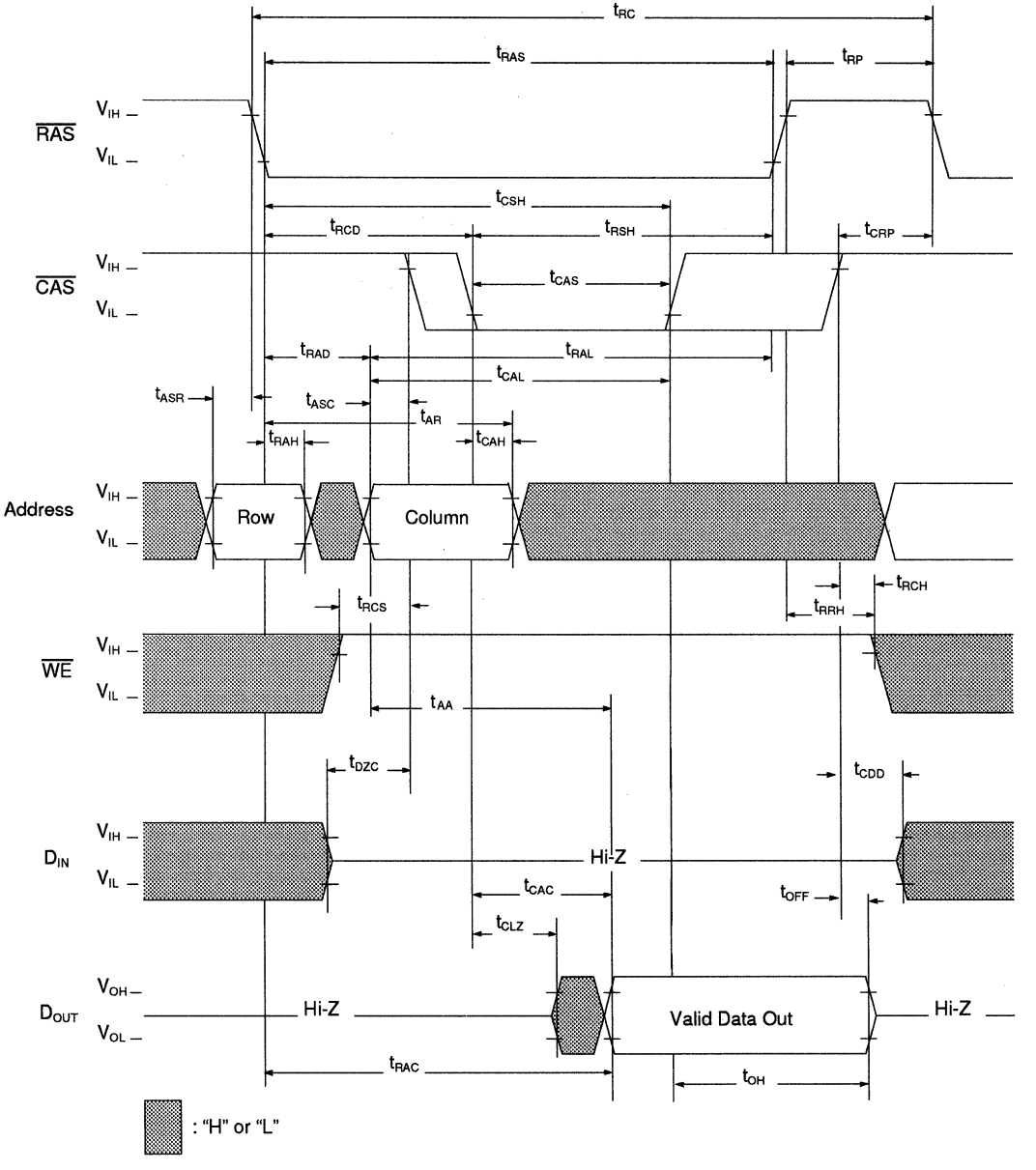
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

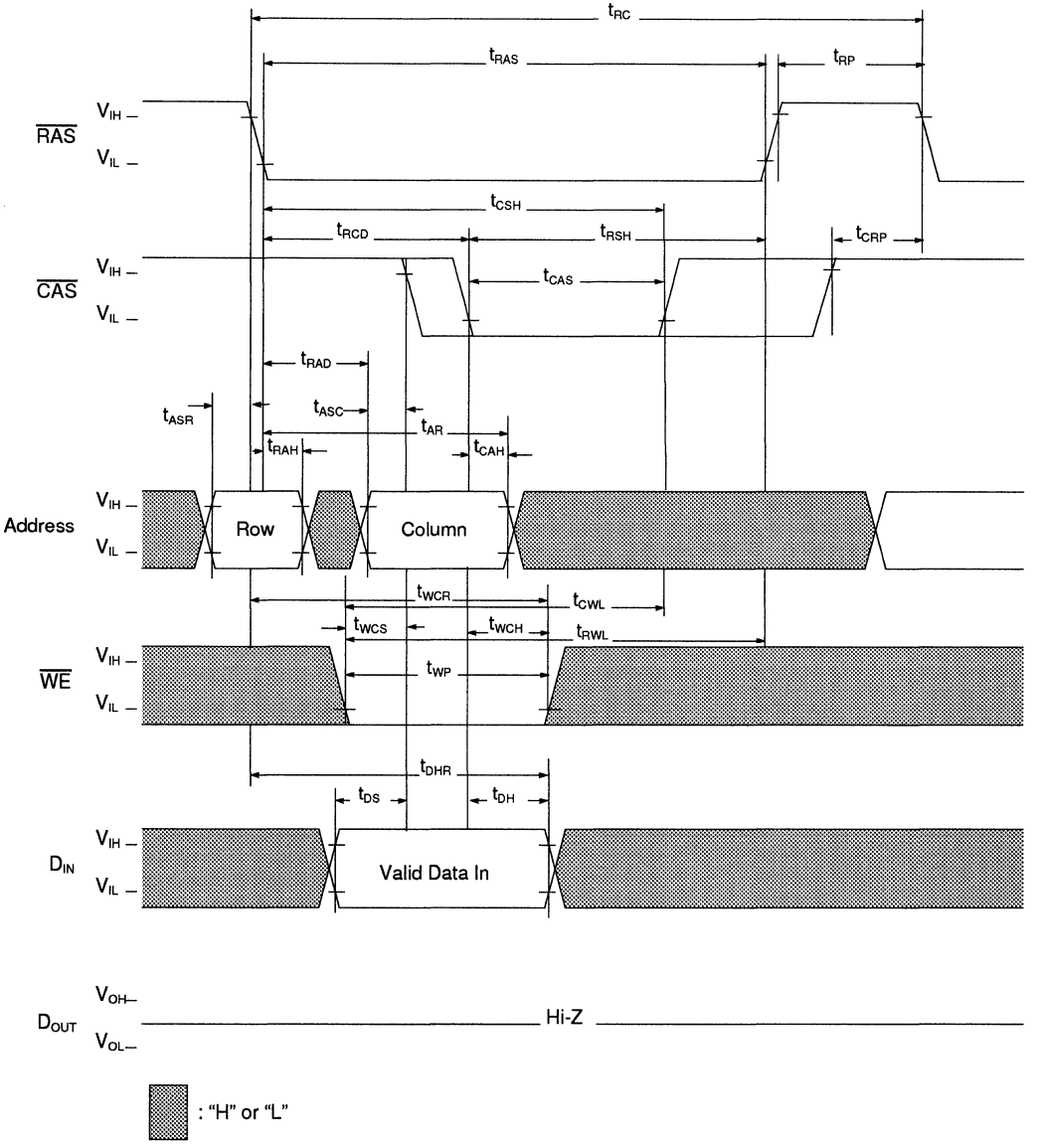
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	256	—	256	ms	1

1. 2048 refreshes are required every 256ms.

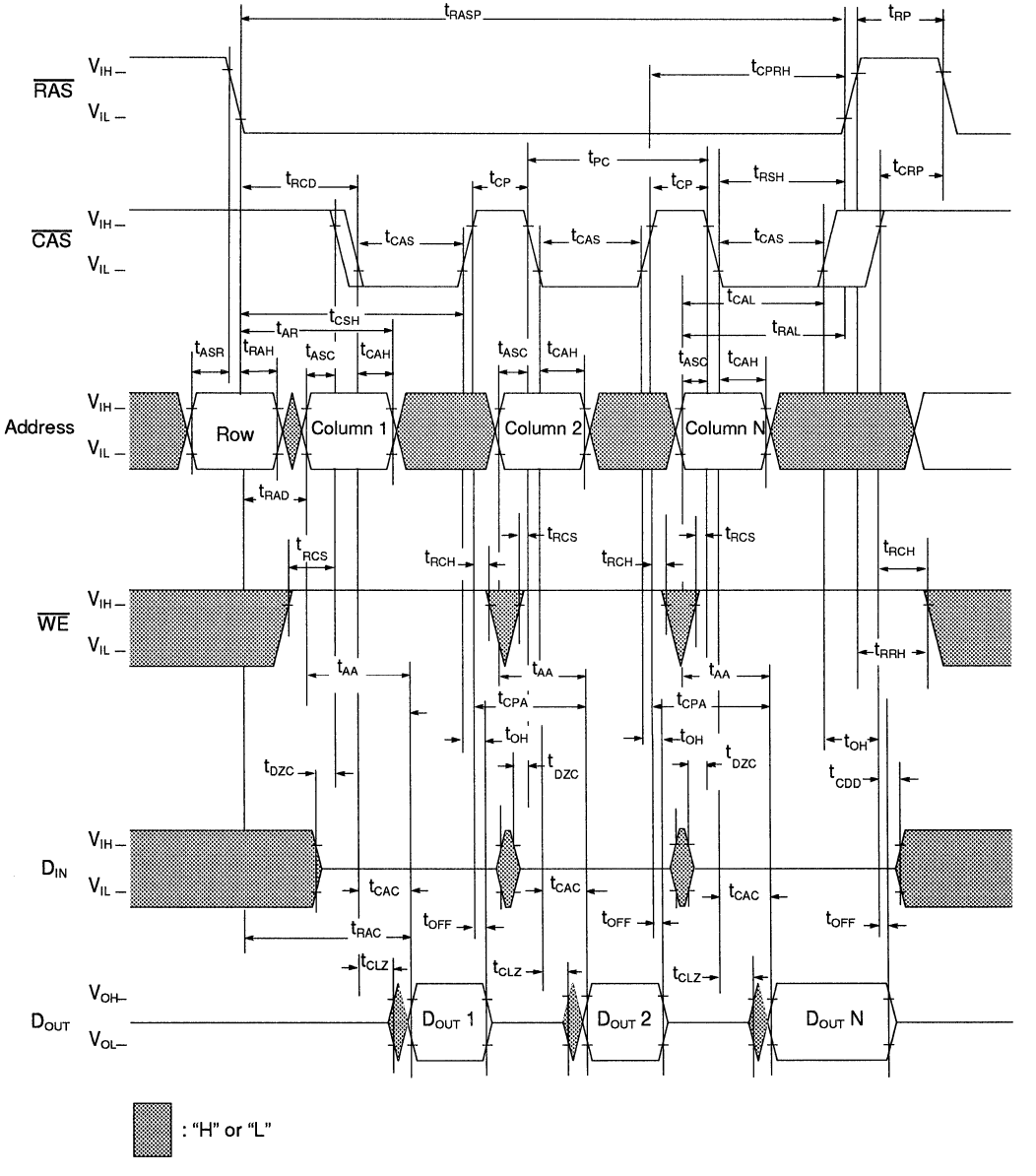
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

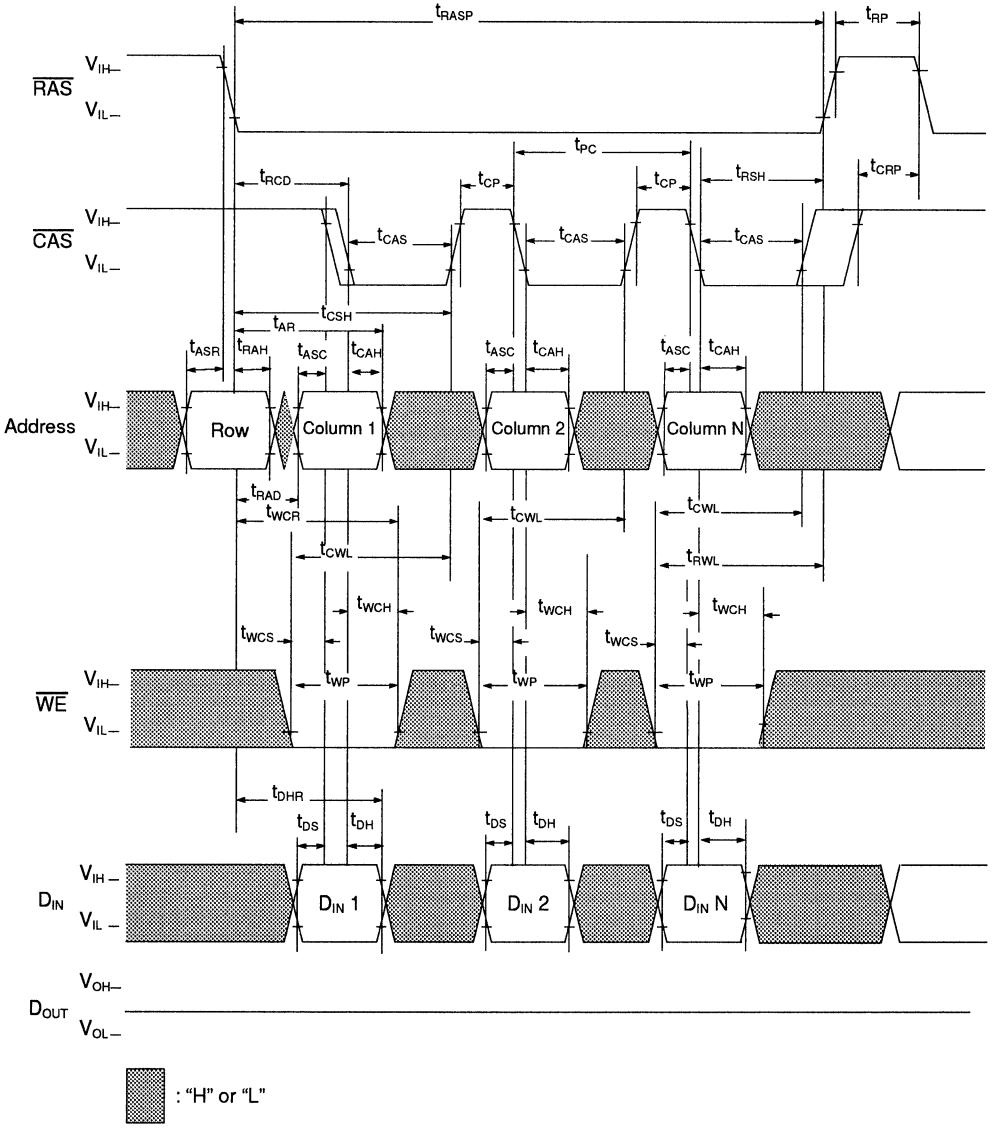
Write Cycle (Early Write)



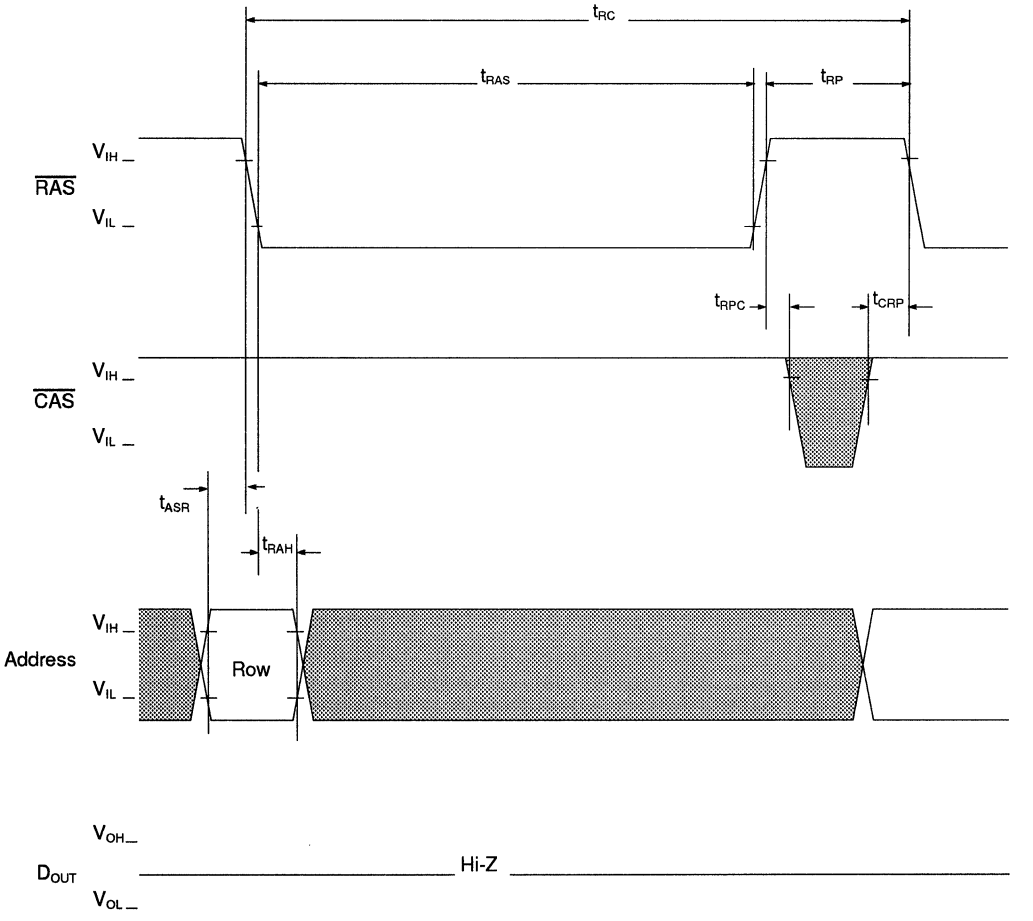
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

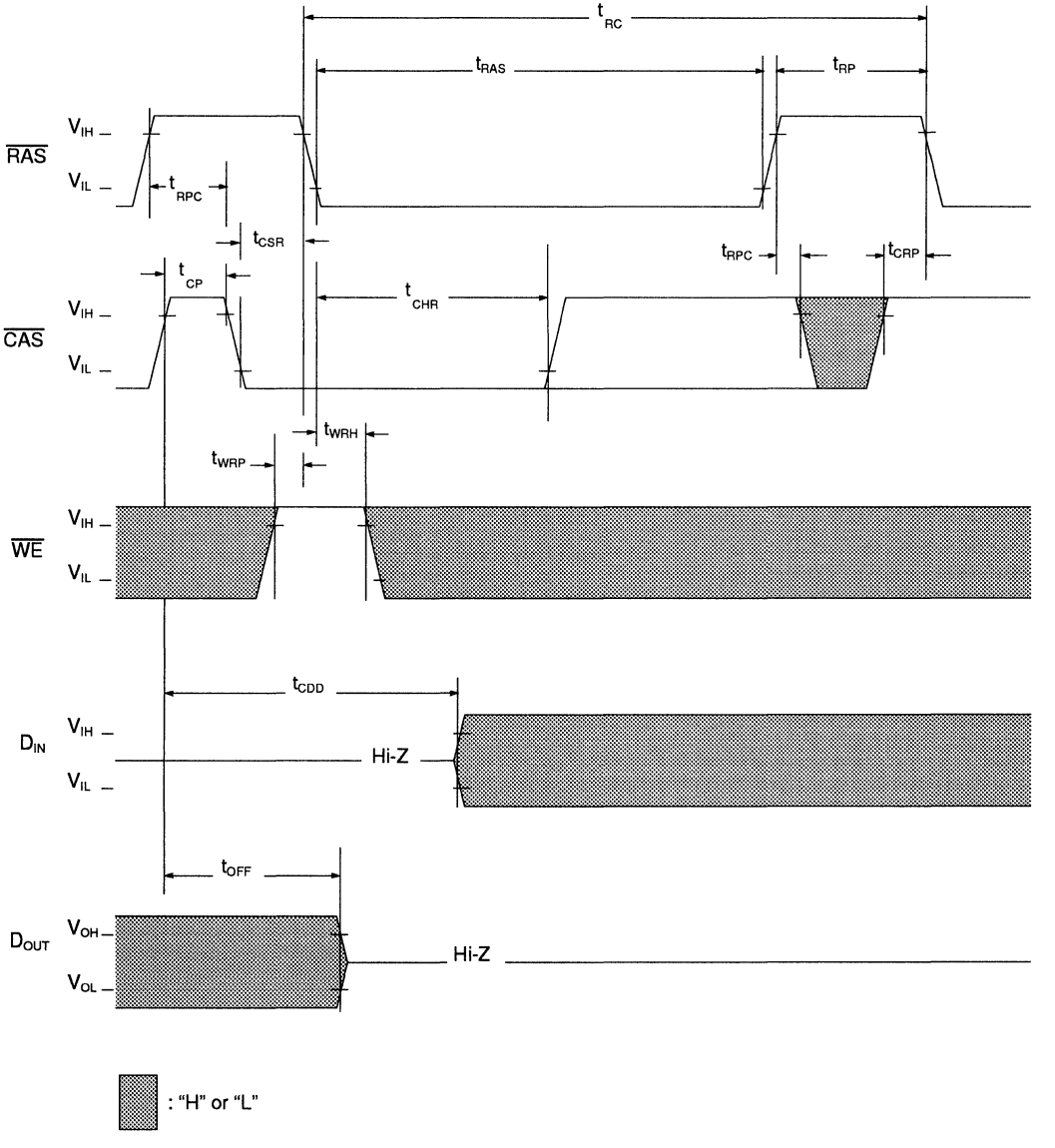


$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, D_{IN} are "H" or "L"

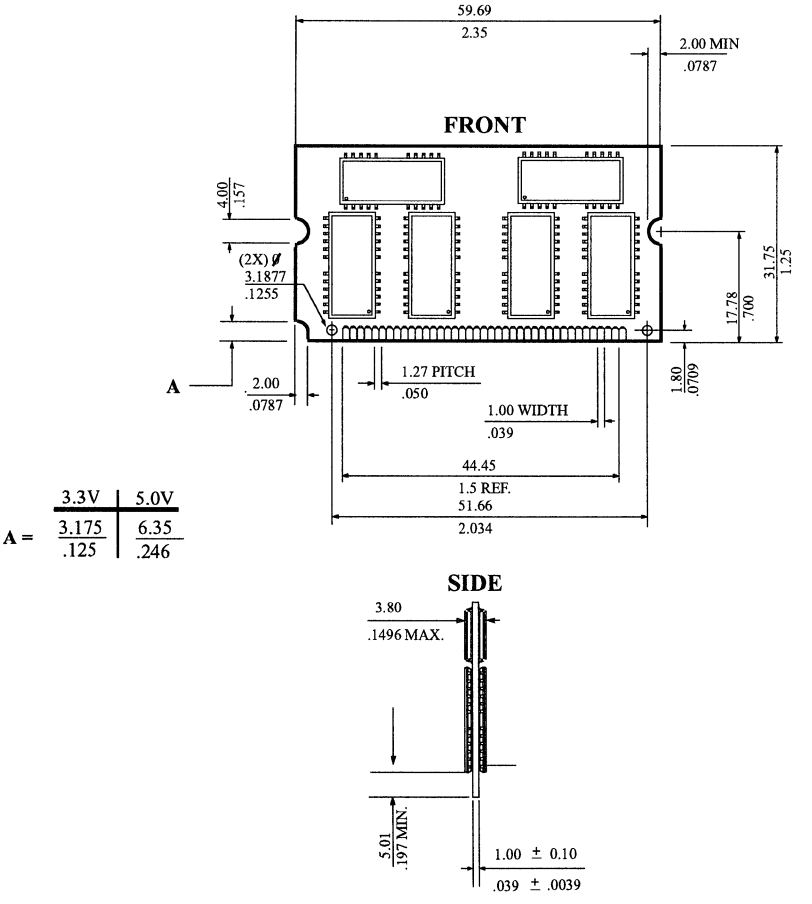
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



: "H" or "L"

Note: Addresses are "H" or "L"

Layout Drawing



A =	3.3V	5.0V
	3.175 / .125	6.35 / .246

NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

4M x 36 SODIMM Module

Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

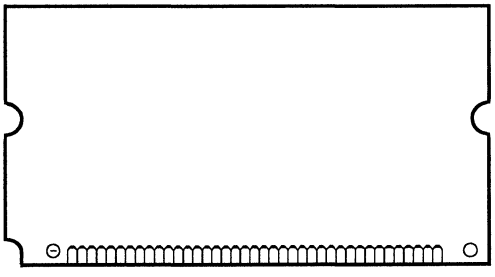
- High Performance CMOS process
- Single 3.3, ± 0.3V or 5.0, ± 0.25V Power Supply
- Low active current consumption
- All inputs & outputs are TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 4096 refresh cycles distributed across 256ms
- 12/11 (Redundant Addressing) Addressing (Row/Column)
- Optimized for use in byte-write parity applications.
- Au contacts

Description

The IBM11S4360DN/L are 16MB 72-pin 4-byte small outline dual in-line memory modules (SODIMM's). The module is organized as a 4Mx36 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 8 4Mx4 and 4 4Mx1 TSOP devices each in a 300mil package. Each bit is uniquely addressed via 22 address bits. The x4 Drams require 12 ROW/10 Column addresses and the x1 Drams require 11 ROW/11 COLUMN addresses. The highest order ROW addresses must be sent as the highest order COLUMN address to satisfy both DRAM requirements.This assembly is intended for use in space constrained and or low power applications.

The IBM 72-Pin SODIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint. Related products include the 4Mx32 version with 11/10 addressing IBM11S4320HN/L as well as the 4Mx32 version with 12/10 addressing IBM11S4320CN/L.

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A11	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, PQ17, PQ26, PQ35	Parity Data Input/output
V_{CC}	Power (+3.3V or +5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

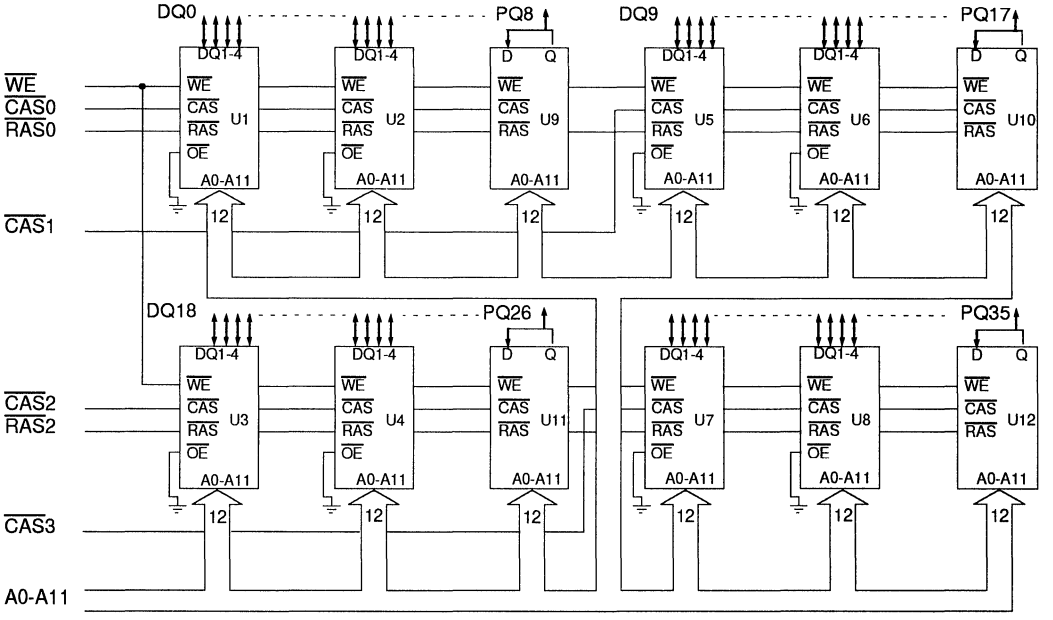
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ23	64	DQ34
5	DQ3	17	A5	29	A11	41	$\overline{CAS2}$	53	DQ24	65	PQ35
6	DQ4	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ25	66	PD2
7	DQ5	19	A10	31	A8	43	$\overline{CAS1}$	55	PQ26	67	PD3
8	DQ6	20	PQ8	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{RAS2}$	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{WE}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	PQ17	48	NC	60	DQ30	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Power
IBM11S4360DNA-60	4M x 36	60ns	Au	2.35" x 1.25" x .1496"	3.3V
IBM11S4360DNA-70	4M x 36	70ns	Au	2.35" x 1.25" x .1496"	3.3V
IBM11S4360DLA-60	4M x 36	60ns	Au	2.35" x 1.25" x .1496"	5.0V
IBM11S4360DLA-70	4M x 36	70ns	Au	2.35" x 1.25" x .1496"	5.0V

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	NC	NC
PD3	V_{SS}	V_{SS}
PD4	NC	NC
PD5	NC	V_{SS}
PD6	NC	NC
PD7	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt	5.0 Volt		
V_{CC}	Power Supply Voltage	-0.5 to + 4.6	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.7 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	-55 to +125	°C	1
P_D	Power Dissipation	0.6	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3 Volt			5.0 Volt			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	2.4	—	V_{CC} + 0.5	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3± 0.3V or 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	82	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	57	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	32	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	80	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	13	pF	
$C_{I/O2}$	Parity Output Capacitance (PQ8, PQ17, PQ26, PQ35)	21	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V or 5.0± 0.25V)

Symbol	Parameter		3.3 Volt Min	3.3 Volt Max	5.0 Volt Min	5.0 Volt Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1040	—	1040	mA	1, 2, 3
		-70	—	920	—	920		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	24	—	24	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	1040	—	1040	mA	1, 3
		-70	—	920	—	920		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	920	—	920	mA	1, 2, 3
		-70	—	800	—	800		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	2.4	—	2.4	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1040	—	1040	mA	1, 3
		-70	—	920	—	920		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	-60	+60	µA	
		$\overline{CAS}$	-30	+30	-30	+30		
		All others	-120	+120	-120	+120		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

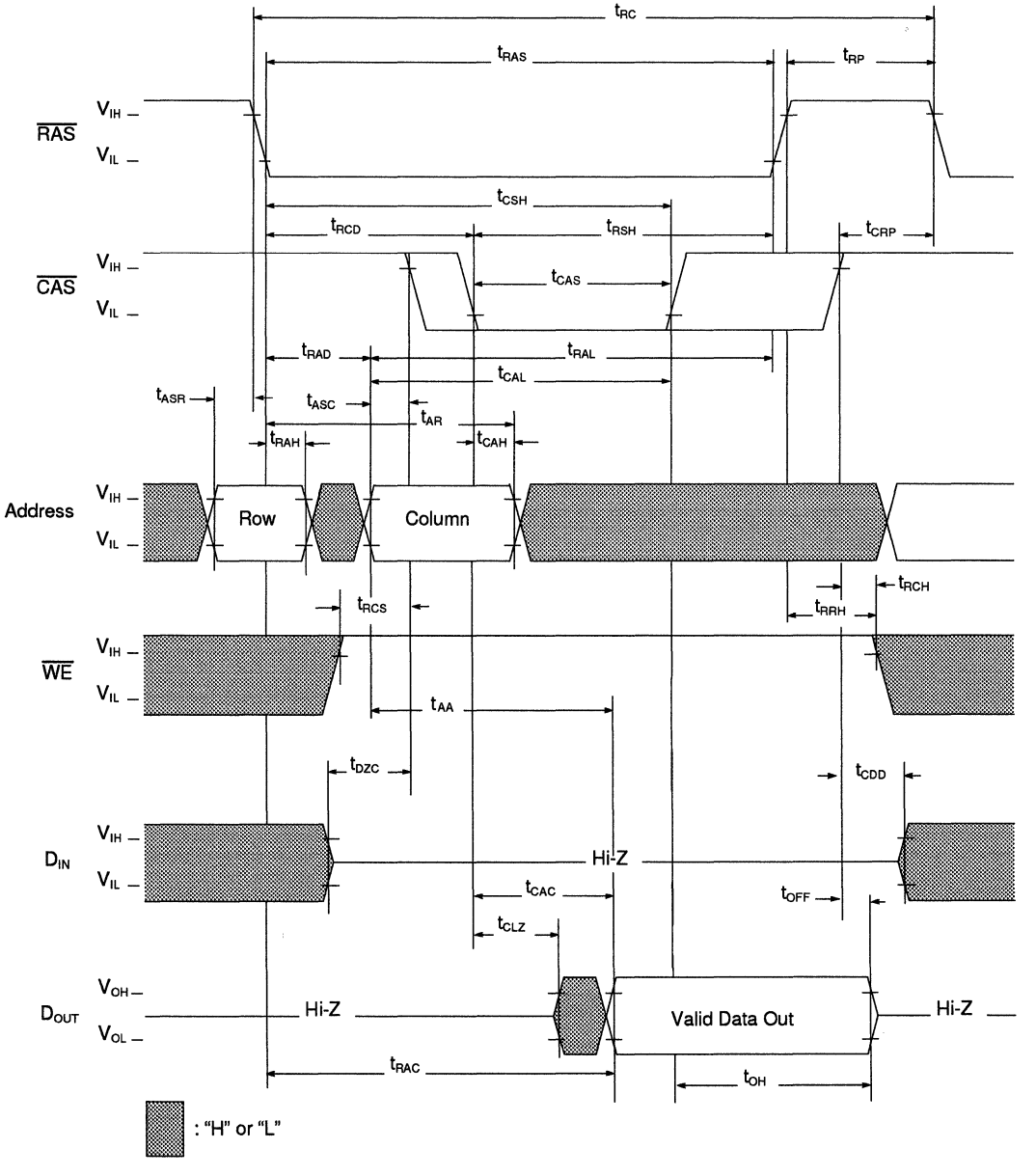
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

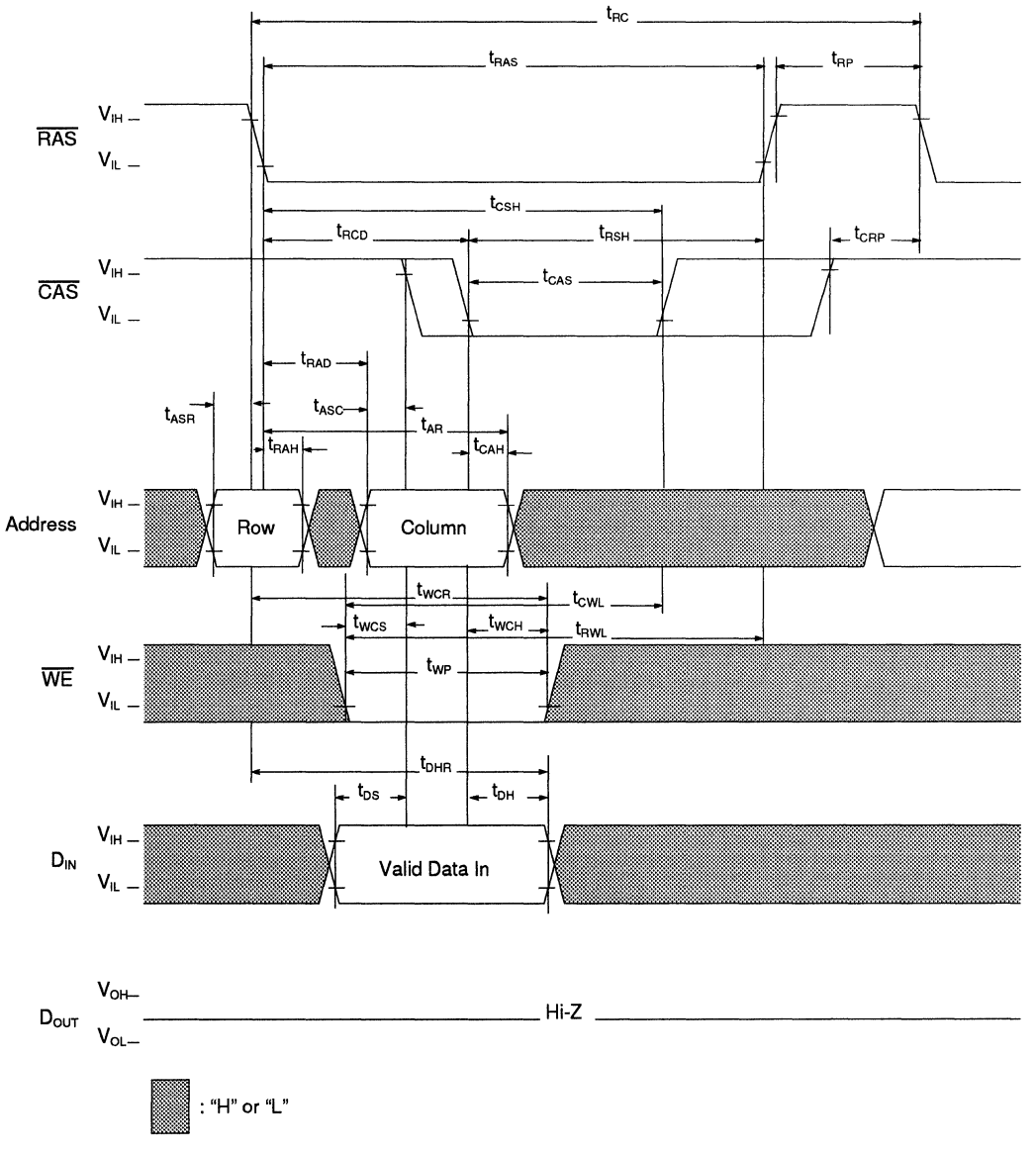
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	256	—	256	ms	1

1. 4096 refreshes are required every 256ms.

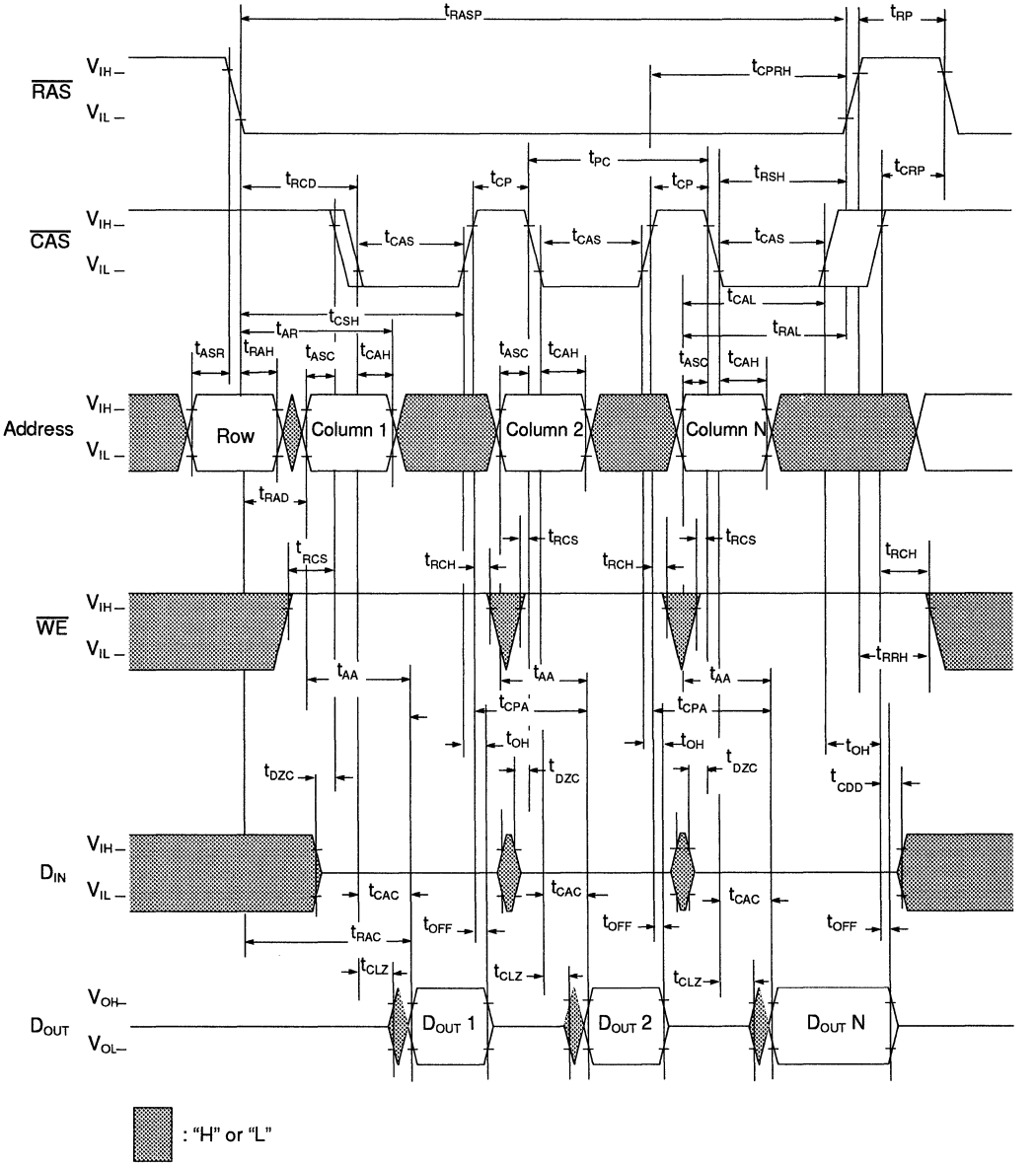
Read


tRC
tRAS
tRP
VIH
RAS
VIL
tCSH
tRCD
tRSH
tCRP
VIH
CAS
VIL
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
VIH
Address
VIL
Row
Column
tRCS
tRCH
tRRH
VIH
WE
VIL
tAA
tDZC
tCDD
VIH
DIN
VIL
Hi-Z
tCAC
tOFF
tCLZ
VOH
DOUT
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

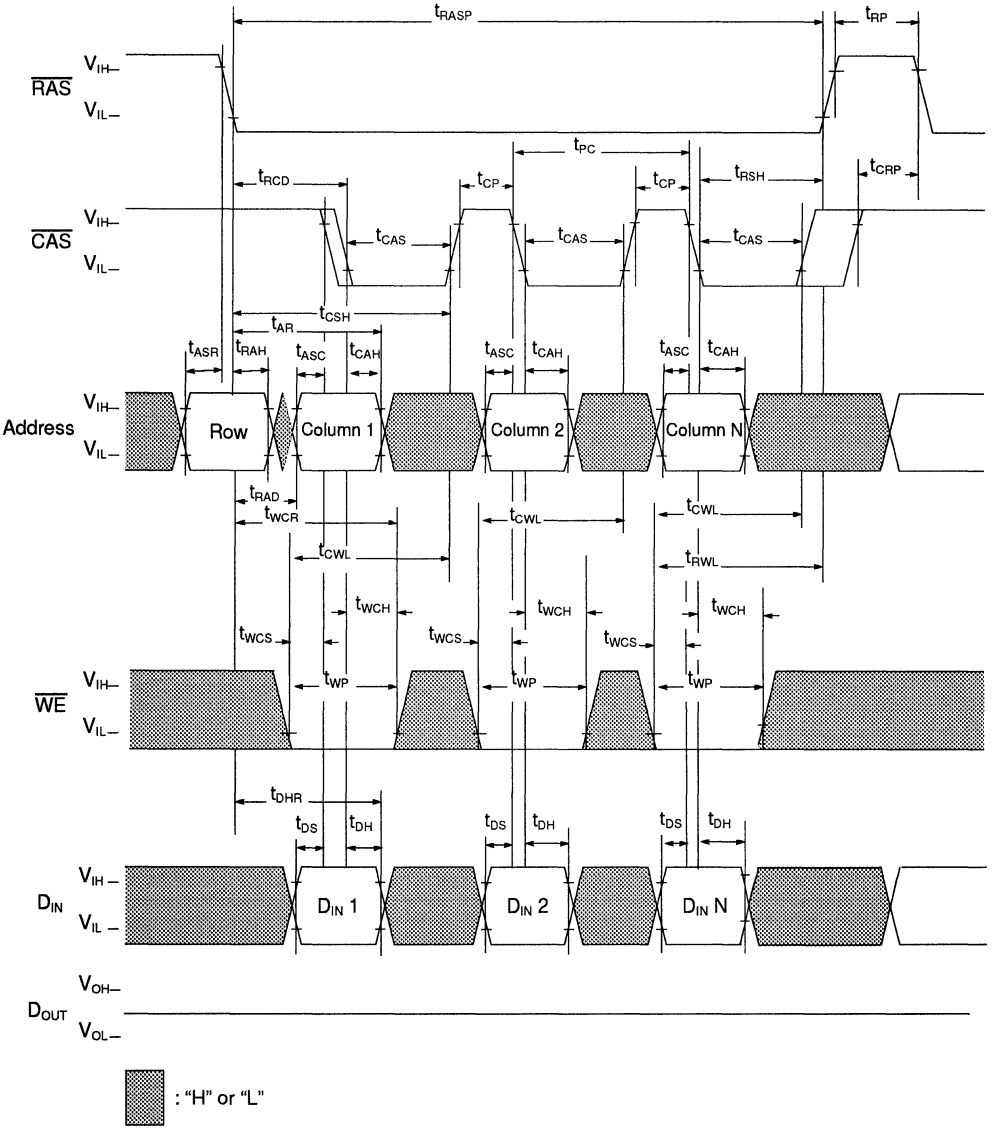
Write Cycle (Early Write)



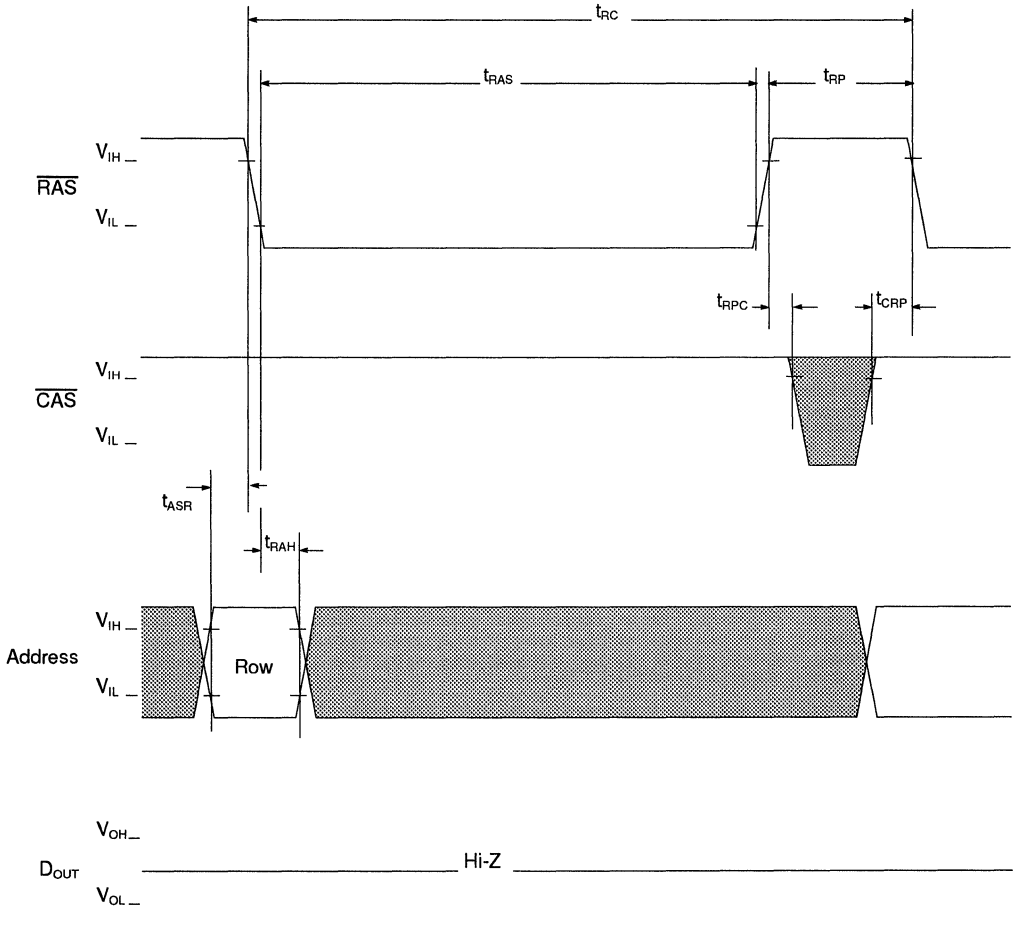
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

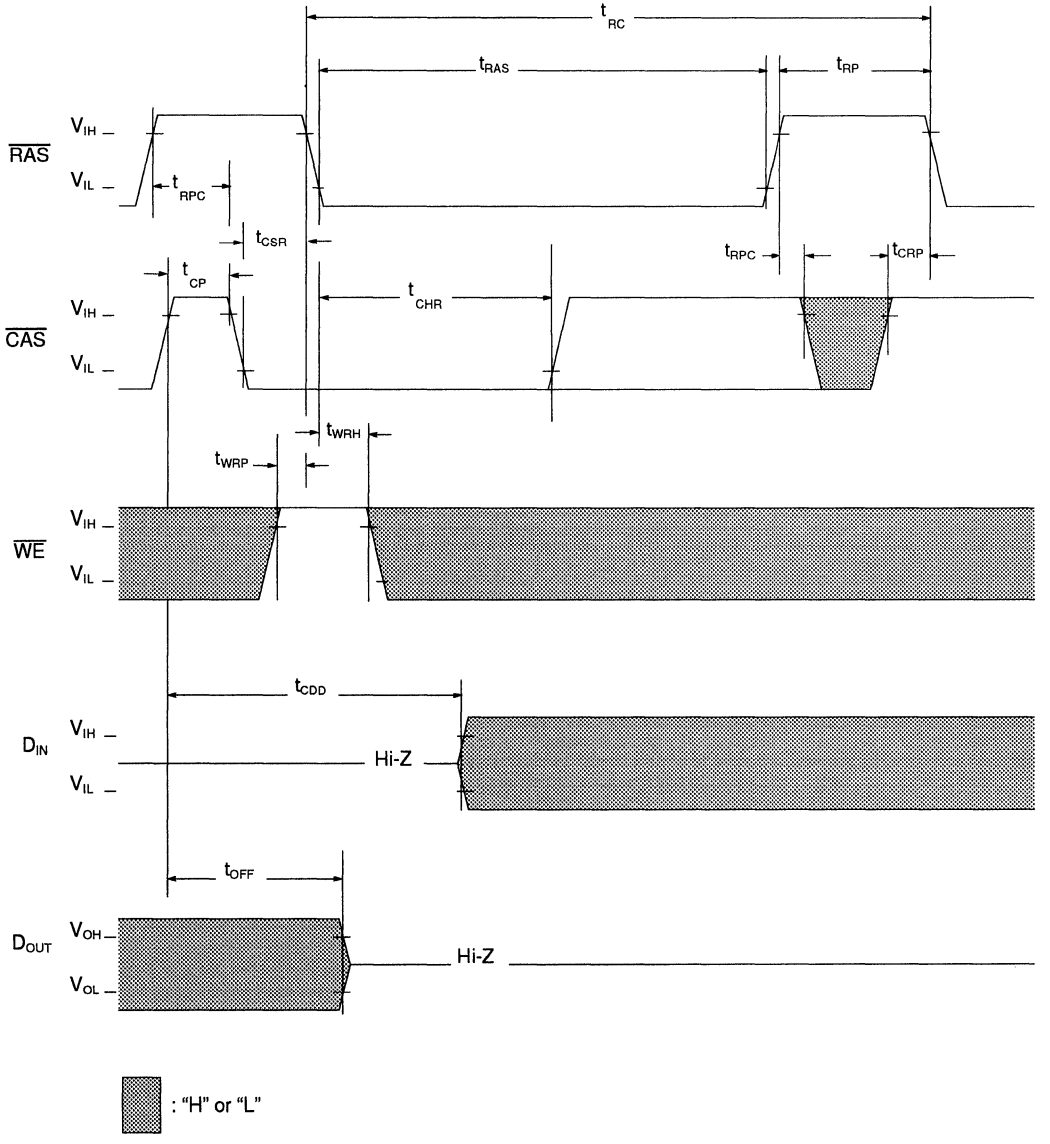


$\overline{RAS}$ Only Refresh Cycle



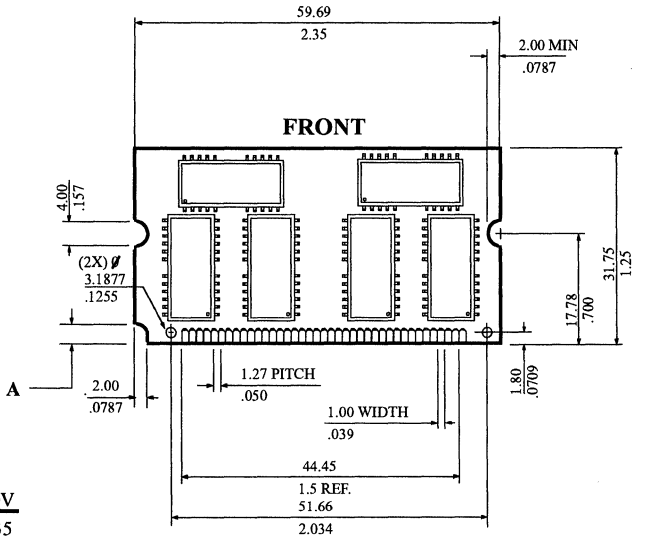
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

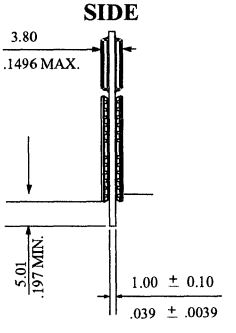


Note: Addresses are "H" or "L"

Layout Drawing



A =	3.3V	5.0V
	3.175	6.35
	.125	.246



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

IC DRAM Cards

1M x 32 5.0V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

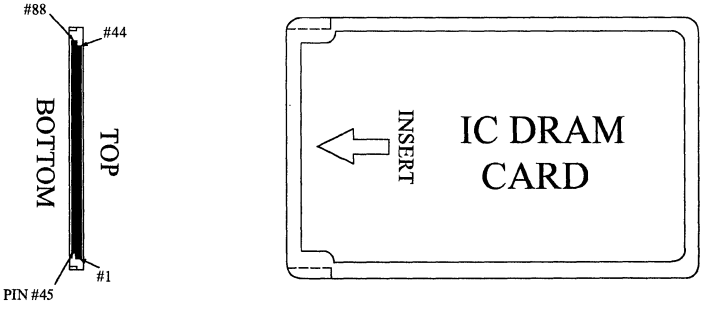
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	29ns
t_{AA}	Access Time From Address	46ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 5.0, ± 0.25V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- 10/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 1024 refresh cycles distributed across 128ms
- Polarized Connector

Description

The IBM11J1320BL is a 4MB industry standard 88-pin IC DRAM card. It is organized as a 1M x 32 high speed memory array. It is built using 8 1Mx4 devices and is compatible to the JEDEC/PCMCIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x32 configuration the memory is a single bank, having four unique bytes. The x16 configuration may be utilized as two banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other bank in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. The related 1M x 36 versions of these ICDRAM cards is IBM11J1360BLA.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

Pinout

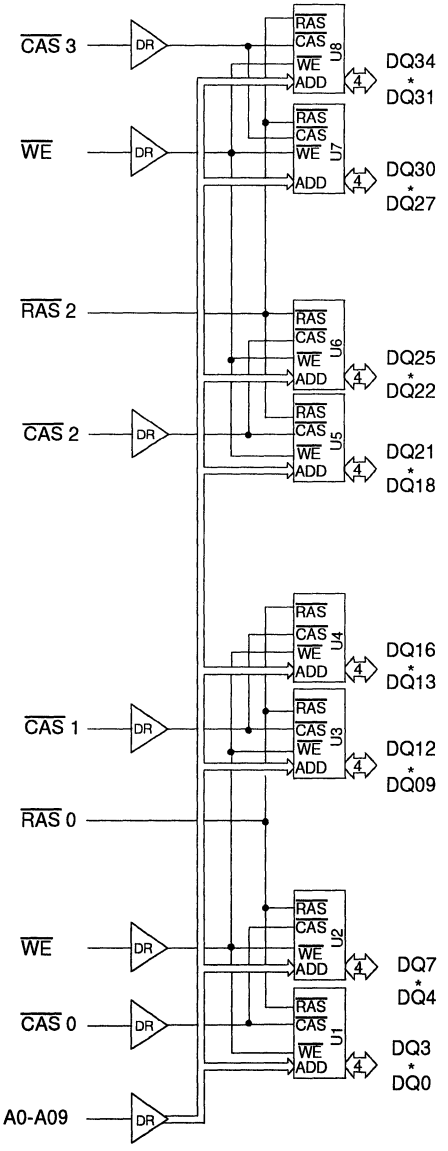
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	NC	47	DQ19	69	NC
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	V_{CC}	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	V_{CC}	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	NC	76	PD8
11	NC	33	NC	55	NC	77	NC
12	NC	34	DQ9	56	V_{SS}	78	NC
13	A0	35	NC	57	A1	79	NC
14	A2	36	DQ10	58	A3	80	DQ27
15	V_{CC}	37	V_{CC}	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	NC	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	NC	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	NC	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	NC	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

1. DQ numbering is compatible with parity (x36) version)

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J1320BLA-70	1M x 32	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	NC
PD3	V_{SS}
PD4	V_{SS}
PD5 (Number of Banks/Organization)	NC
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +6.0	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-1.0 to +6.0	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-1.0 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	4.2	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.4	—	V_{CC}+0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	43	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O}$	Output Capacitance (DQ0~DQ34)	25	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	800	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	16	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	800	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	800	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	1.6	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	800	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			2.4	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 10ns ($\overline{CAS}$, $\overline{WE}$) or 11ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	11	—	ns	
t_{RAH}	Row Address Hold Time	10	—	ns	
t_{ASC}	Column Address Setup Time	3	—	ns	
t_{CAH}	Column Address Hold Time	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	42	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	24	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	29	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	20	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 19ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 21ns (7ns before max t_{CAC} of 28ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	15	—	ns	
t_{WP}	Write Command Pulse Width	16	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	25	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	29	ns	1, 2
t_{AA}	Access Time from Address	—	46	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	46	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	29	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	49	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	49	ns	1, 2

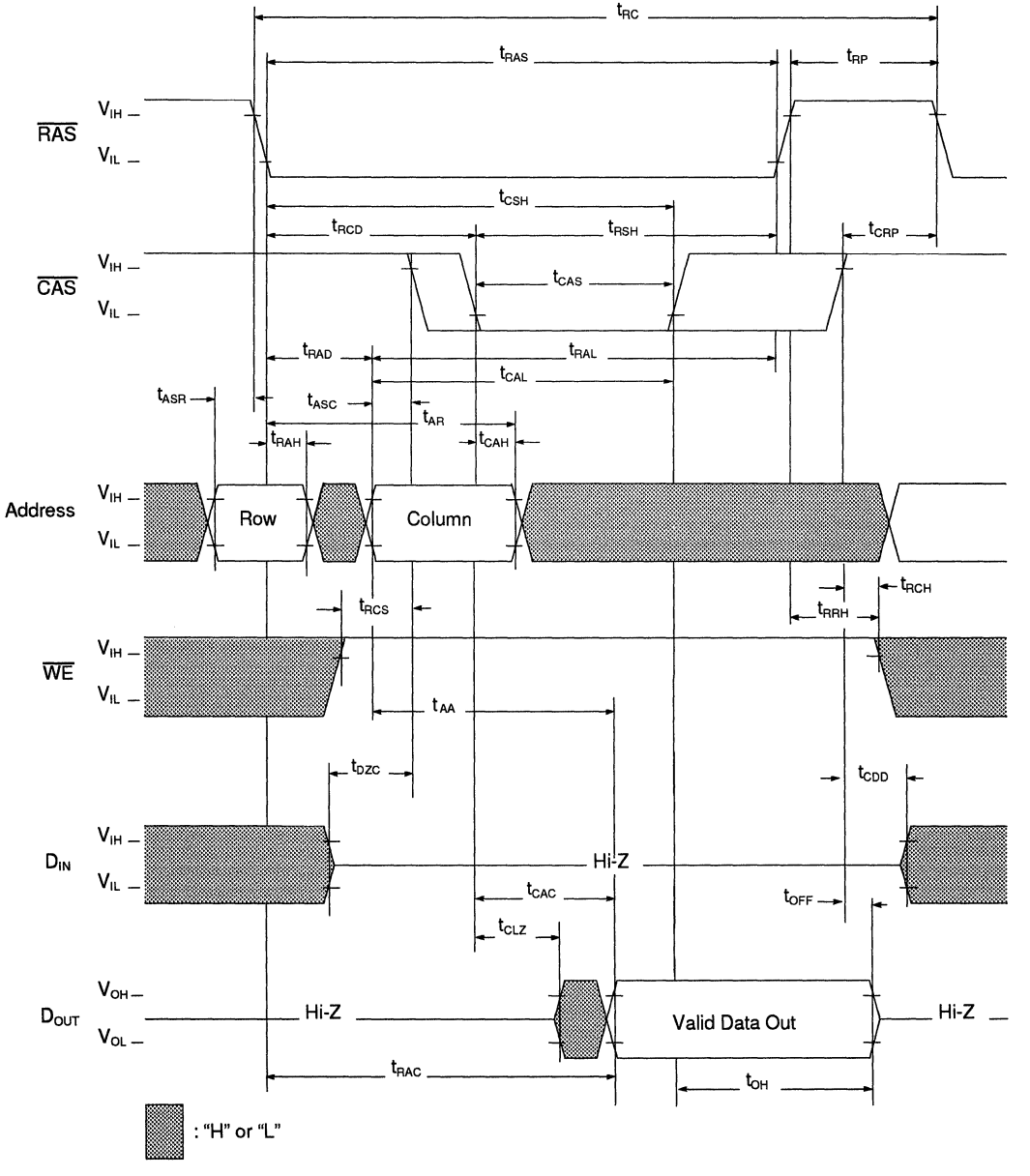
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

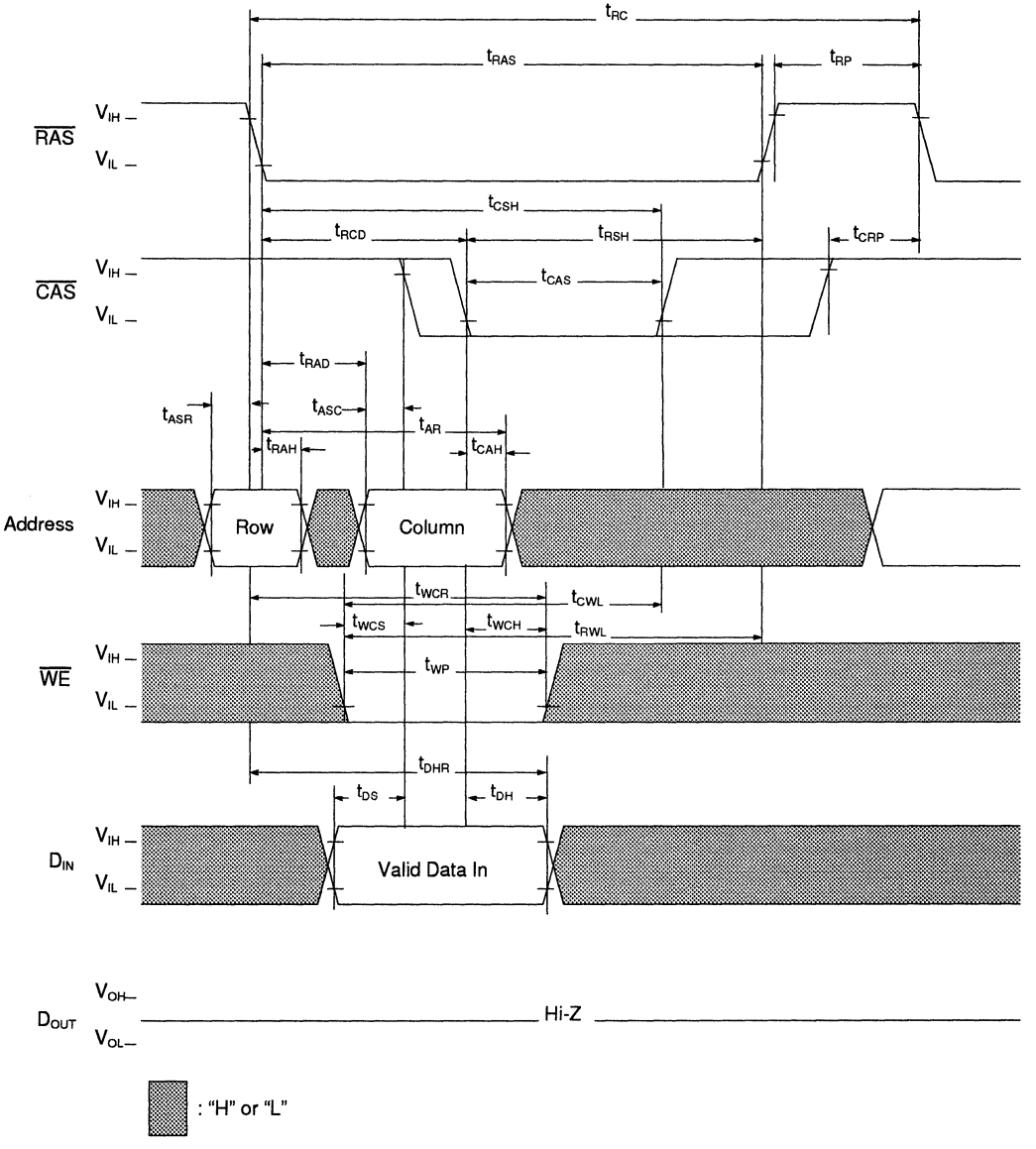
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	13	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	8	—	ns	
t_{REF}	Refresh Period	—	128	ms	1

1. 1024 refreshes are required every 128ms.

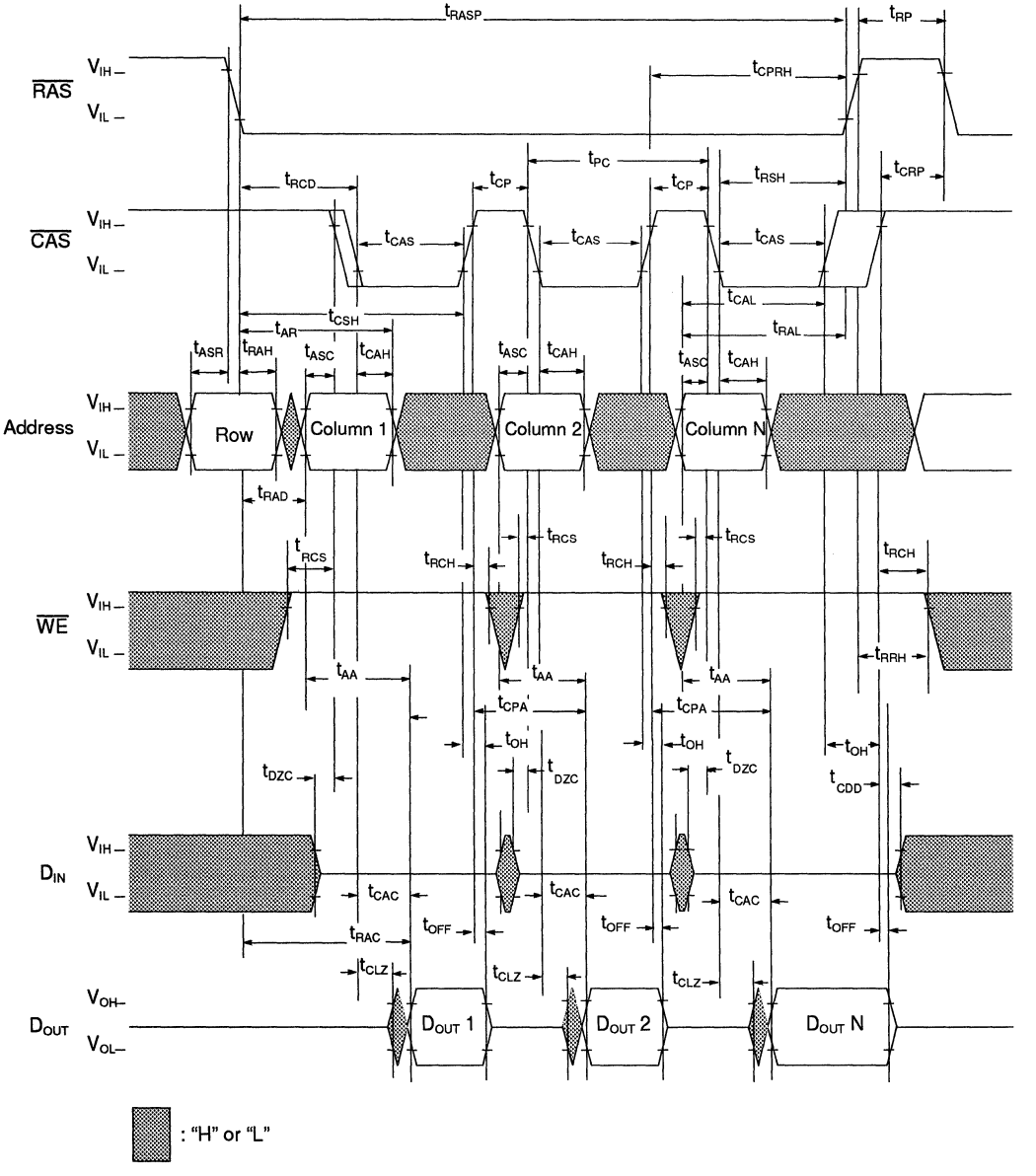
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Valid Data Out
tRAC
tOH
: "H" or "L"

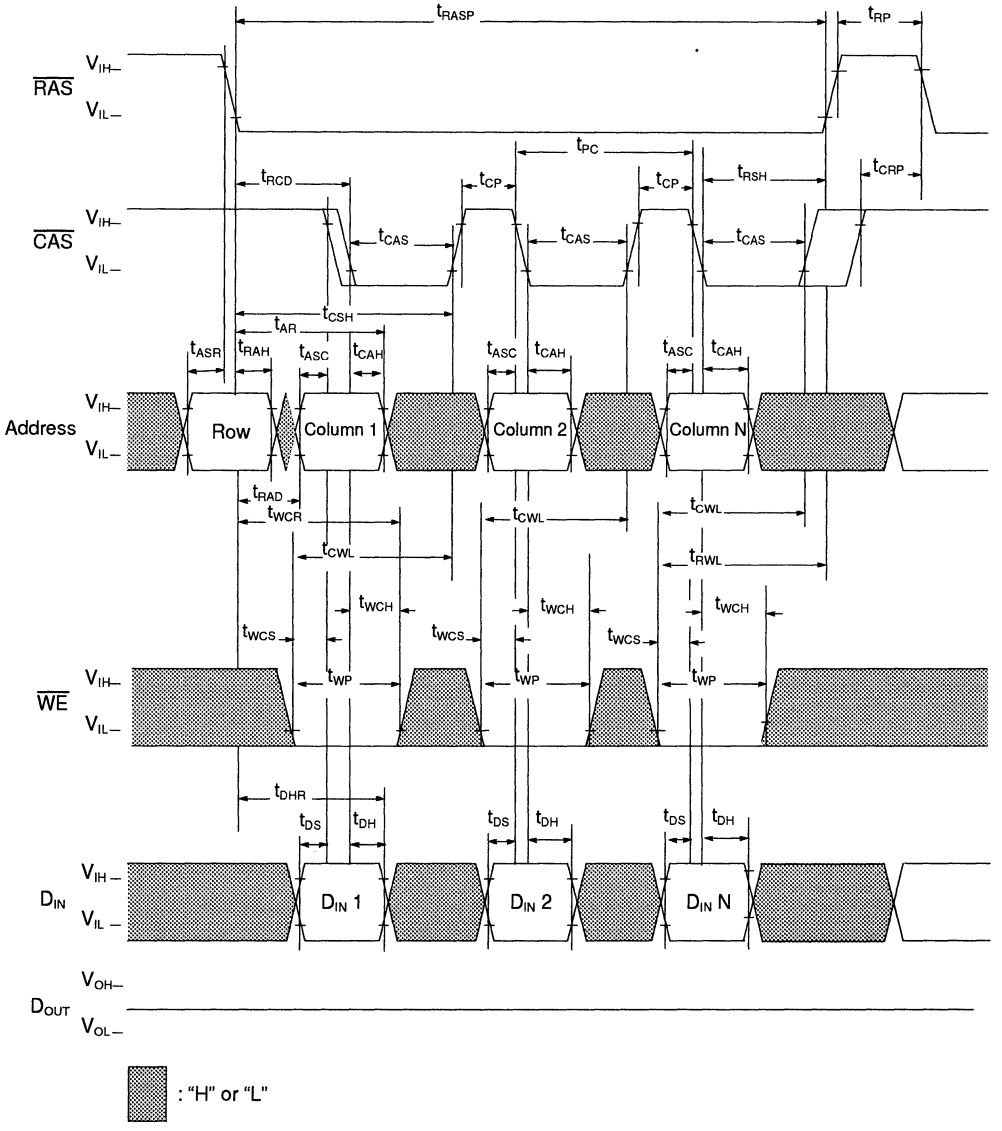
Write Cycle (Early Write)



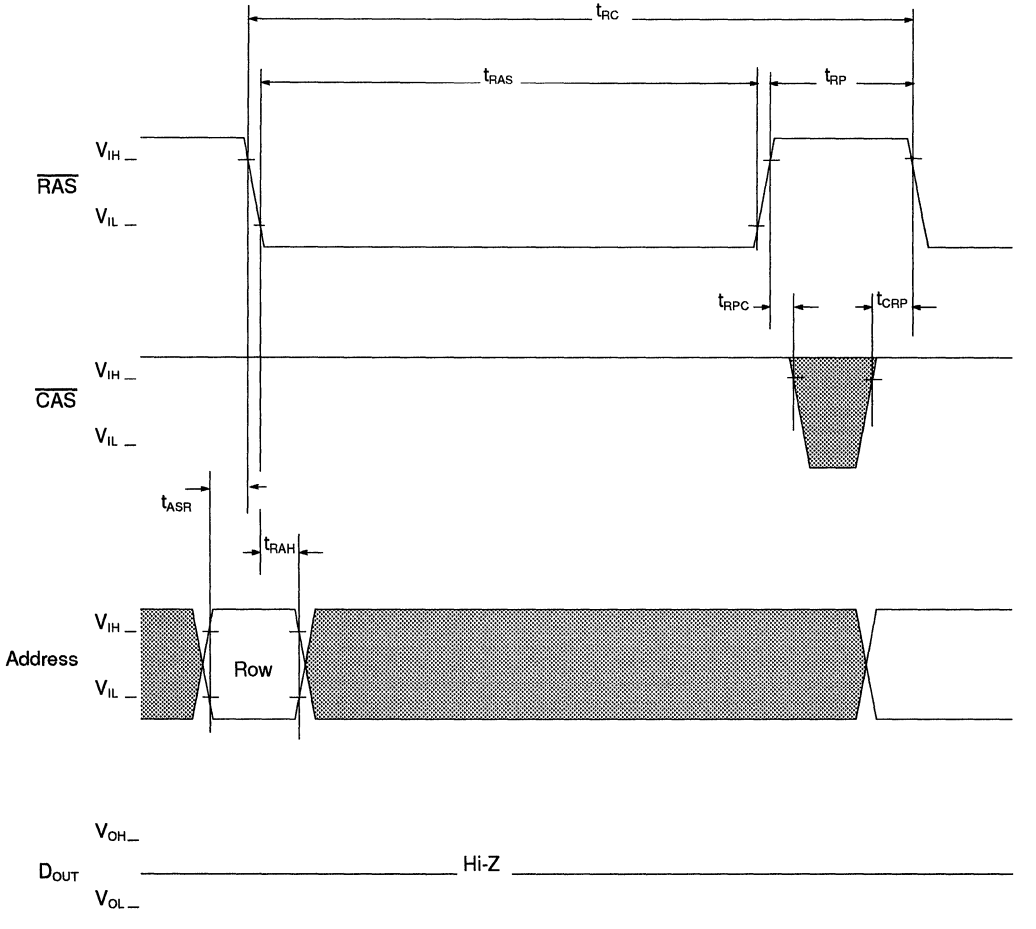
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

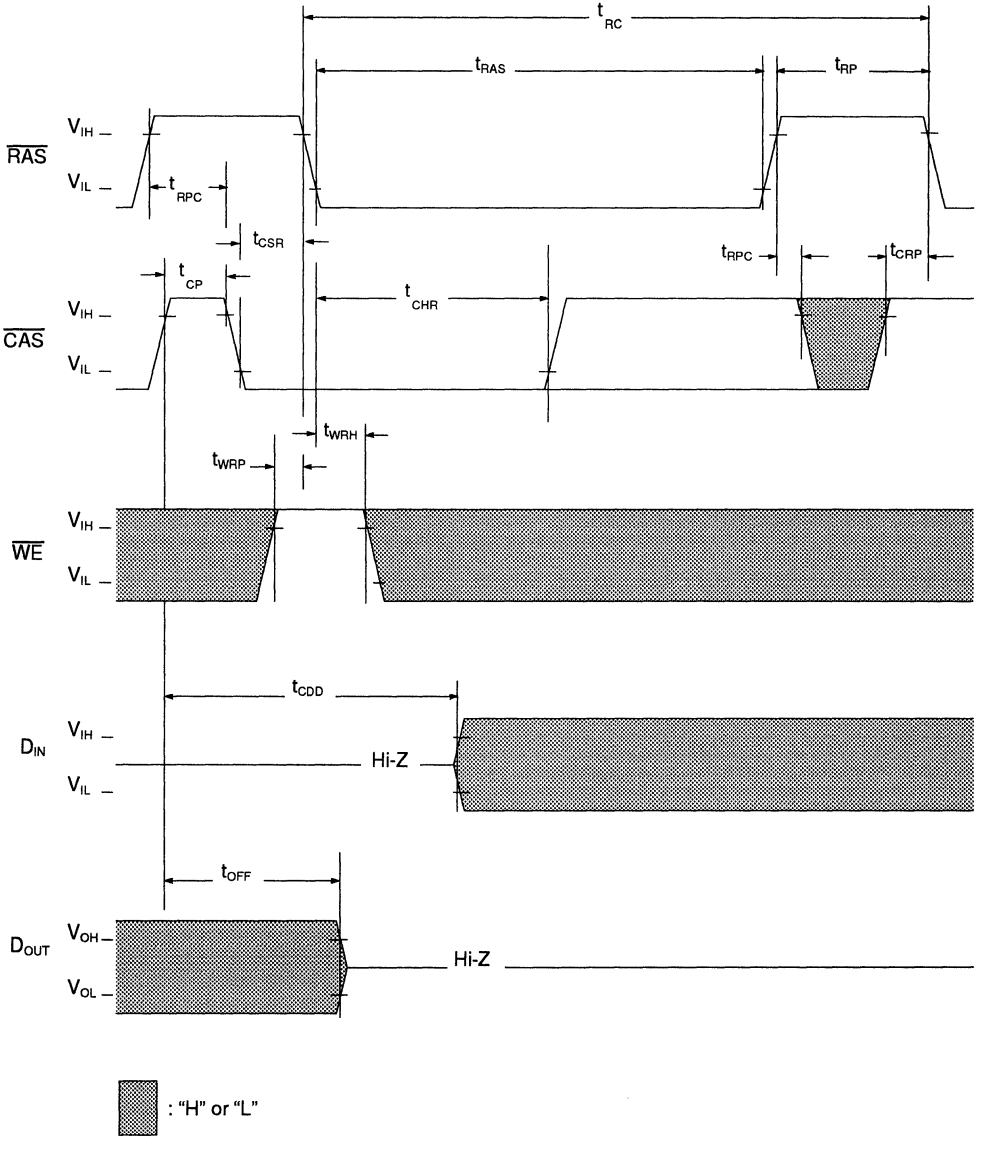


$\overline{RAS}$ Only Refresh Cycle



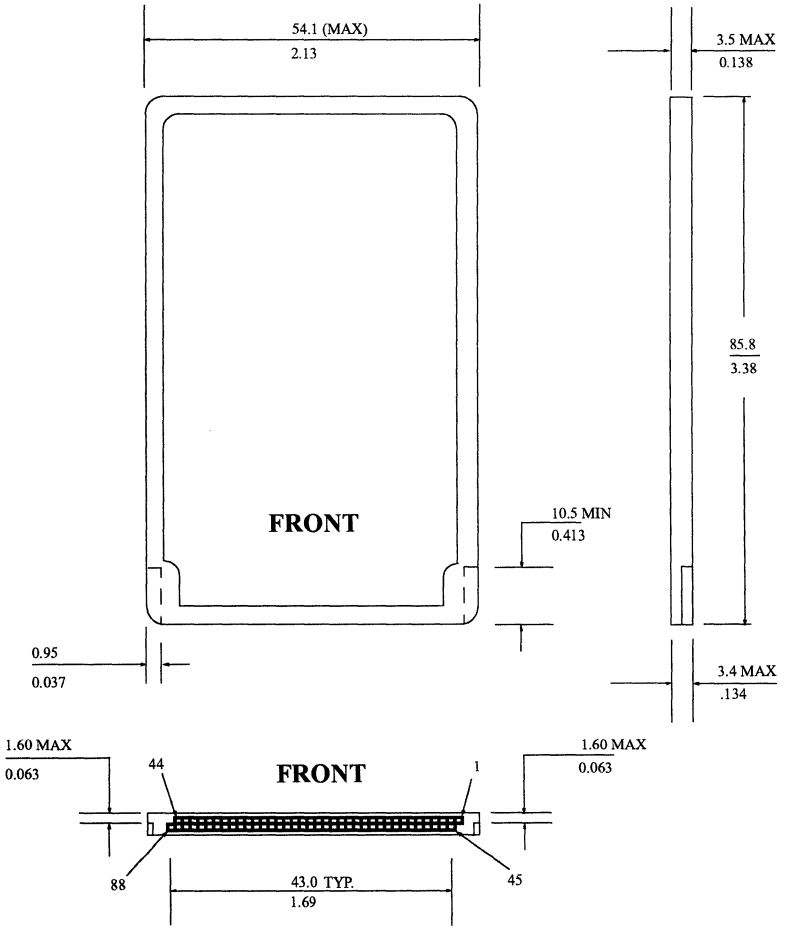
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

1M x 32 3.3V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

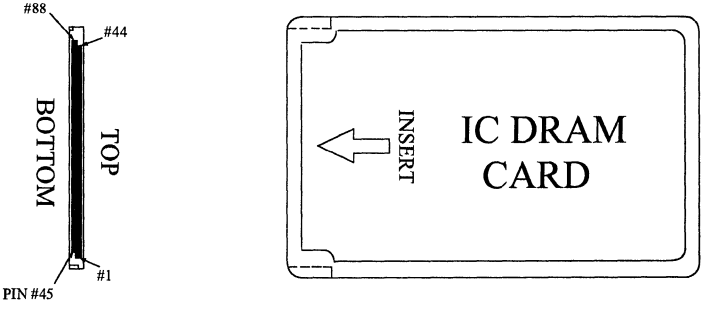
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	24ns
t_{AA}	Access Time From Address	40ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 3.3 ± 0.3V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- 10/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 1024 refresh cycles distributed across 128ms
- Polarized Connector

Description

The IBM11J1320BN is a 4MB industry standard 88-pin IC DRAM card. It is organized as a 1M x 32 high speed memory array. It is built using 8 1Mx4 devices and is compatible to the JEDEC/PCM-CIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x32 configuration the memory is a single bank, having four unique bytes. The x16 configuration may be utilized as two banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other bank in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. **Caution must be used to prevent insertion into a 5.0V application.**

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

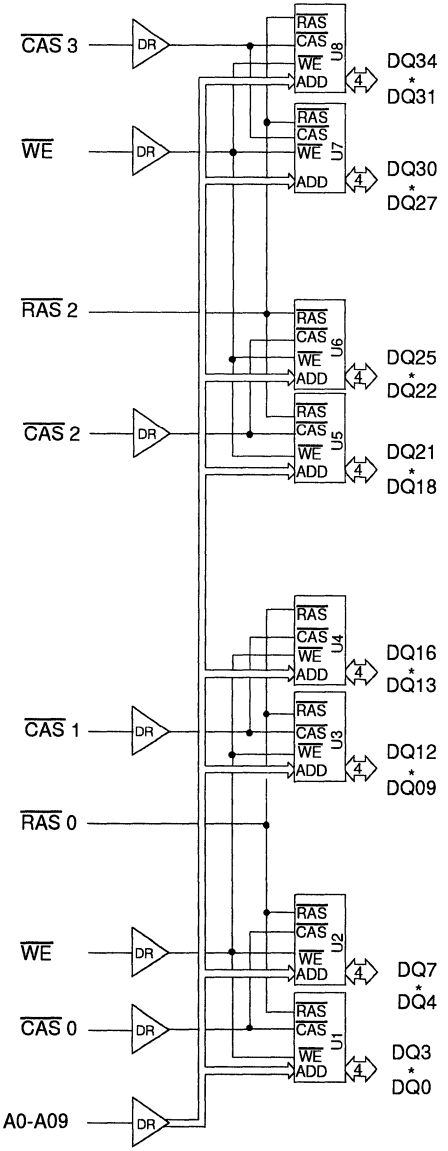
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	V_{CC}	47	DQ19	69	NC
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	NC	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	NC	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	NC	76	PD8
11	V_{CC}	33	NC	55	NC	77	NC
12	NC	34	DQ9	56	V_{SS}	78	NC
13	A0	35	V_{CC}	57	A1	79	NC
14	A2	36	DQ10	58	A3	80	DQ27
15	NC	37	NC	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	V_{CC}	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	NC	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	NC	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	NC	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J1320BNA-70	1M x 32	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	NC
PD3	V_{SS}
PD4	V_{SS}
PD5 (Number of Banks/Organization)	NC
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +4.1	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to +4.1	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to +4.1	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	2.3	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.0	—	V_{CC}+0.3	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.3	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	43	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O}$	Output Capacitance (DQ0~DQ34)	25	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	640	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	8	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	640	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	520	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	2.0	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	640	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			2.4	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.0	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 3.3 ± 0.3V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 1ns minimum, 4ns ($\overline{CAS}$, $\overline{WE}$) or 5ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specification of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	—	ns	2
t_{ASR}	Row Address Setup Time	5	—	ns	
t_{RAH}	Row Address Hold Time	9	—	ns	
t_{ASC}	Column Address Setup Time	2	—	ns	
t_{CAH}	Column Address Hold Time	16	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	19	46	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	14	30	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	24	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	69	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	14	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 20ns plus a minimum t_{OH} of 1ns would result in turning data out of the card at 21ns (3ns before max t_{CAC} of 24ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	19	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	24	ns	1, 2
t_{AA}	Access Time from Address	—	40	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	1	—	ns	
t_{OH}	Output Data Hold Time	1	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	24	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	1	24	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	44	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	44	ns	1, 2

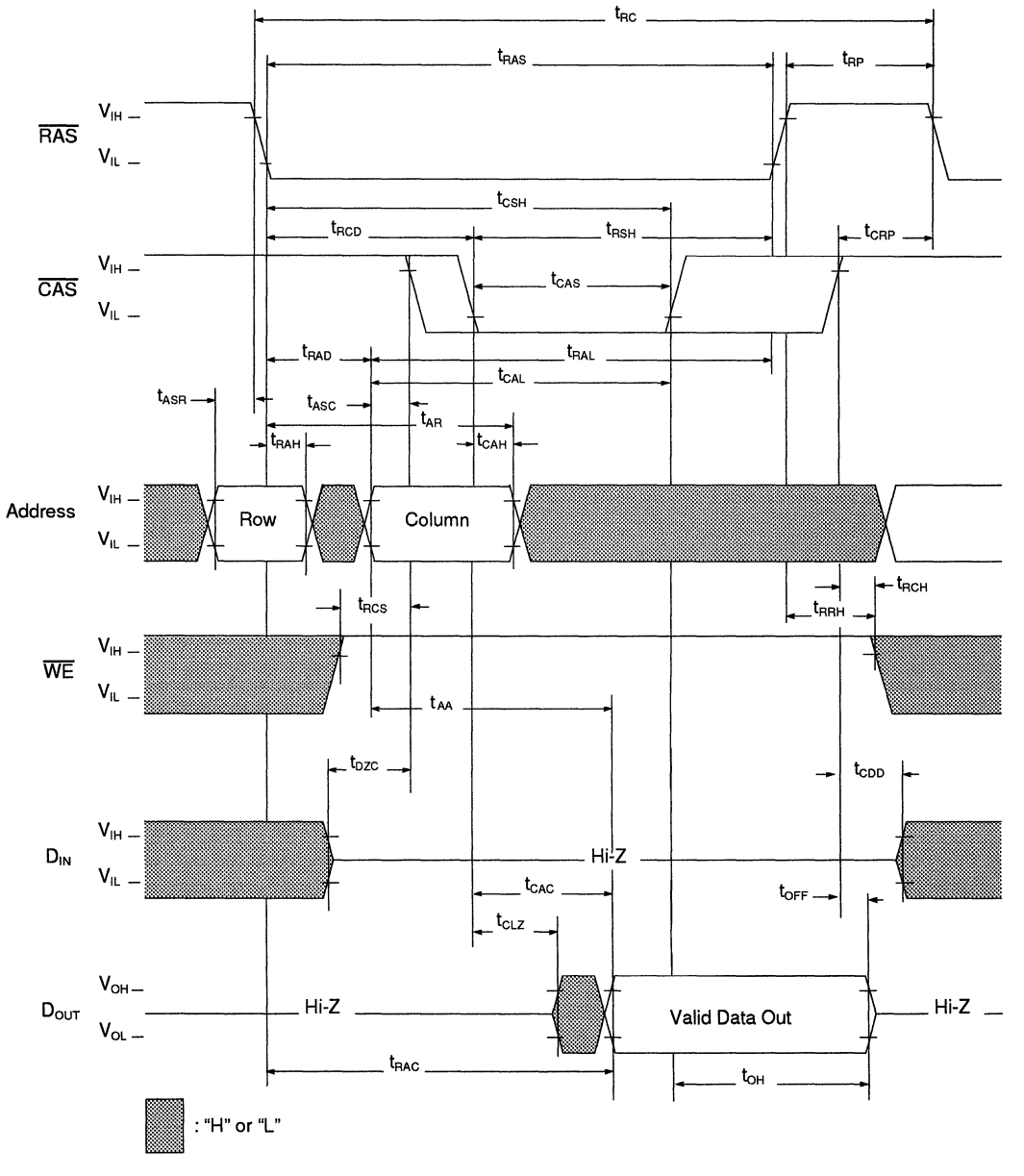
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

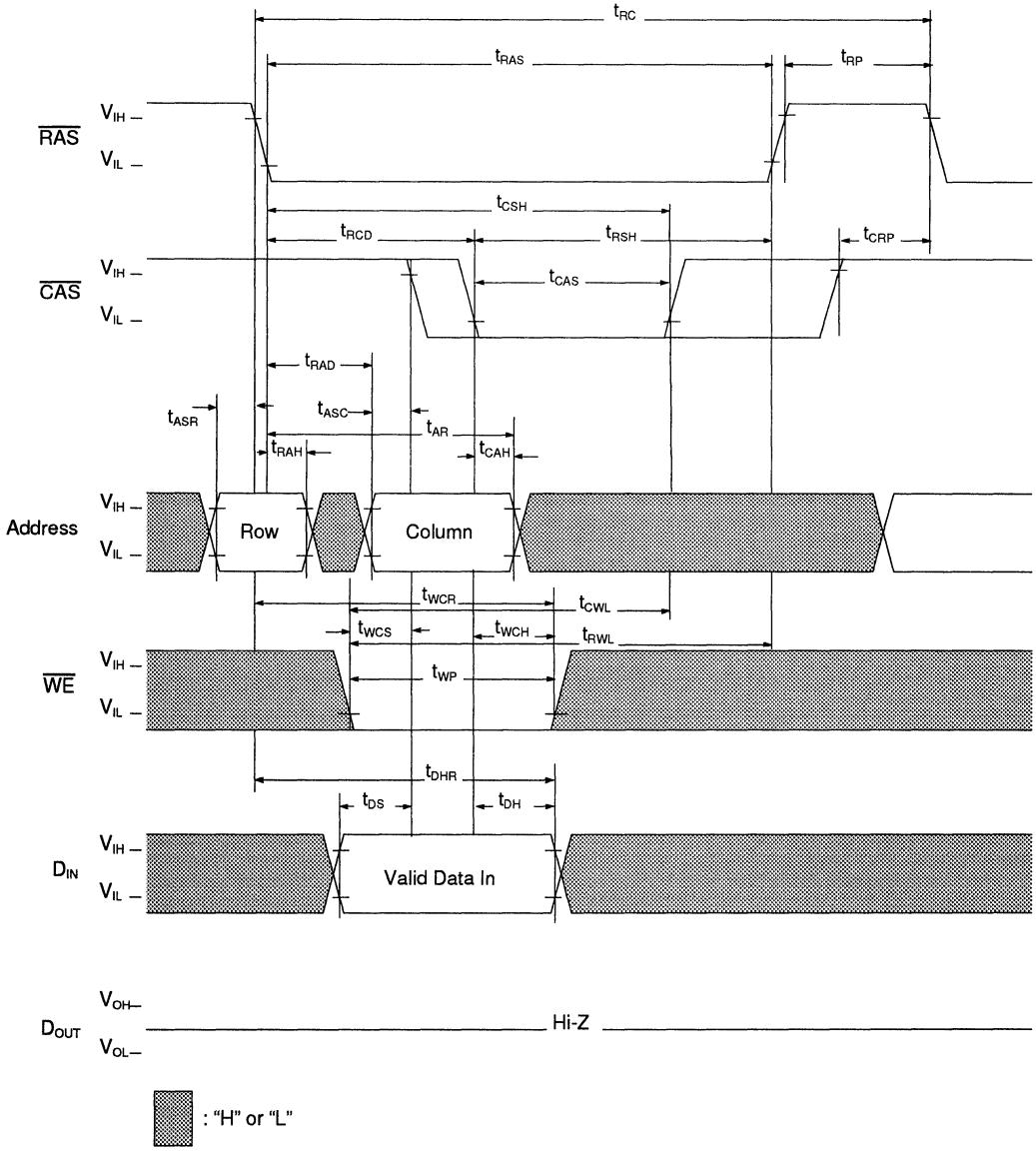
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	9	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	14	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	9	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	9	—	ns	
t_{REF}	Refresh Period	—	128	ms	1

1. 1024 refreshes are required every 128ms.

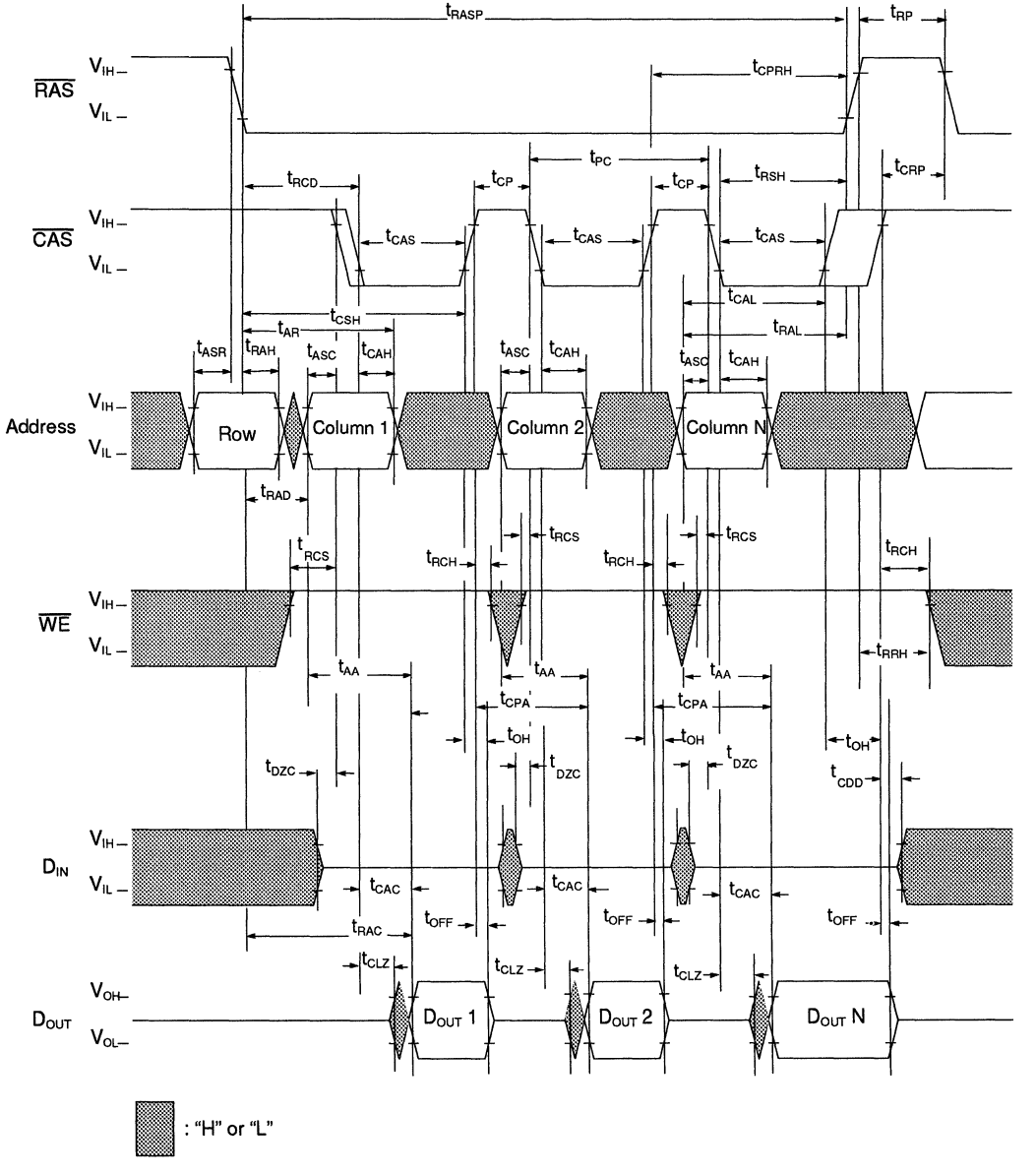
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

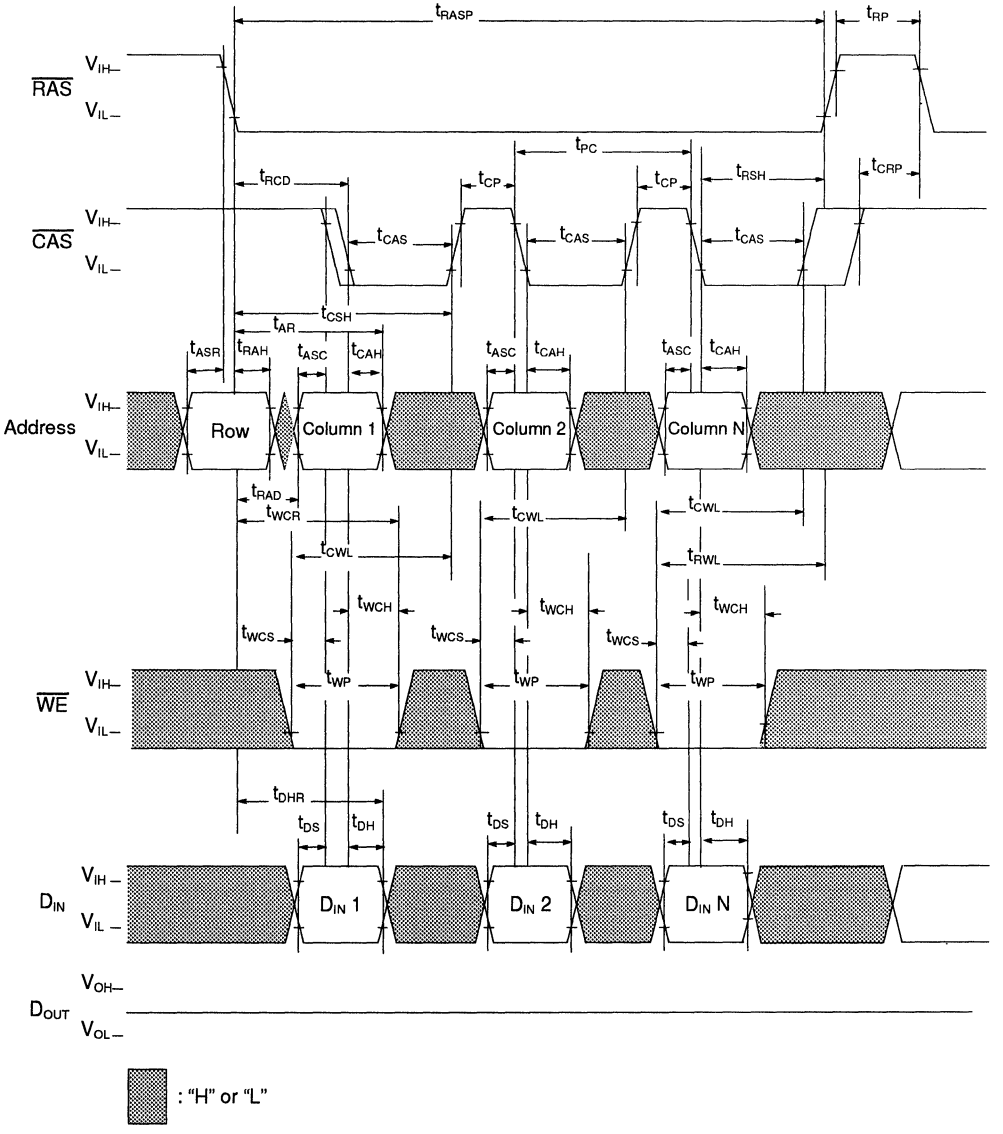
Write Cycle (Early Write)



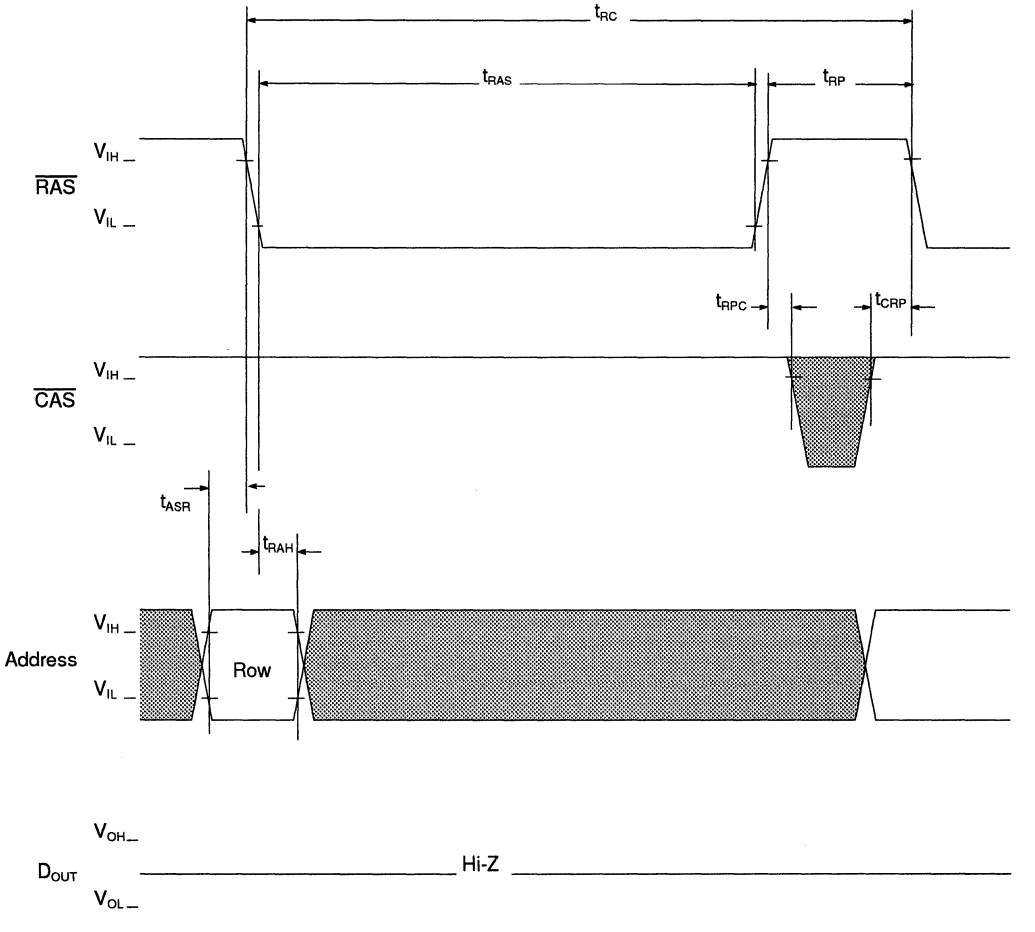
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



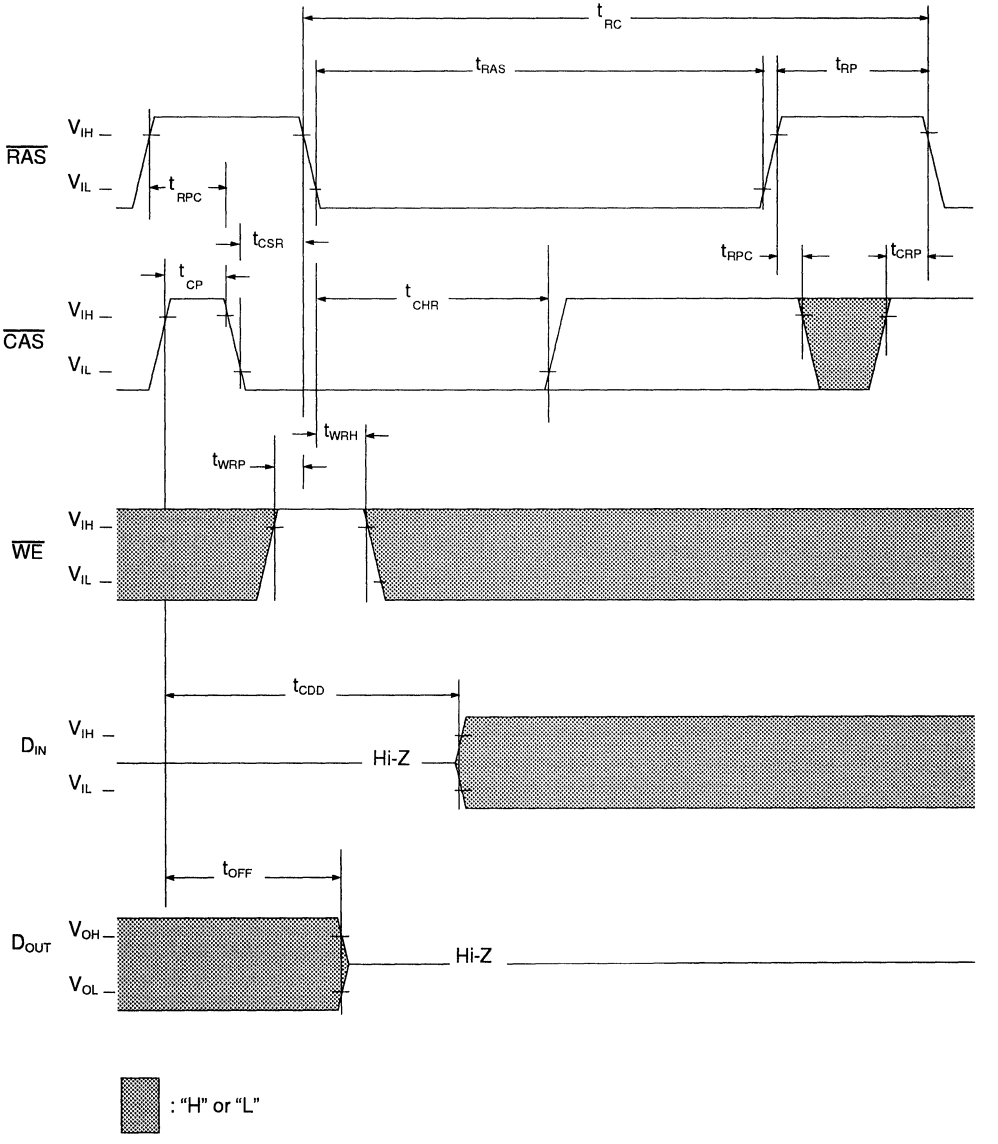
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

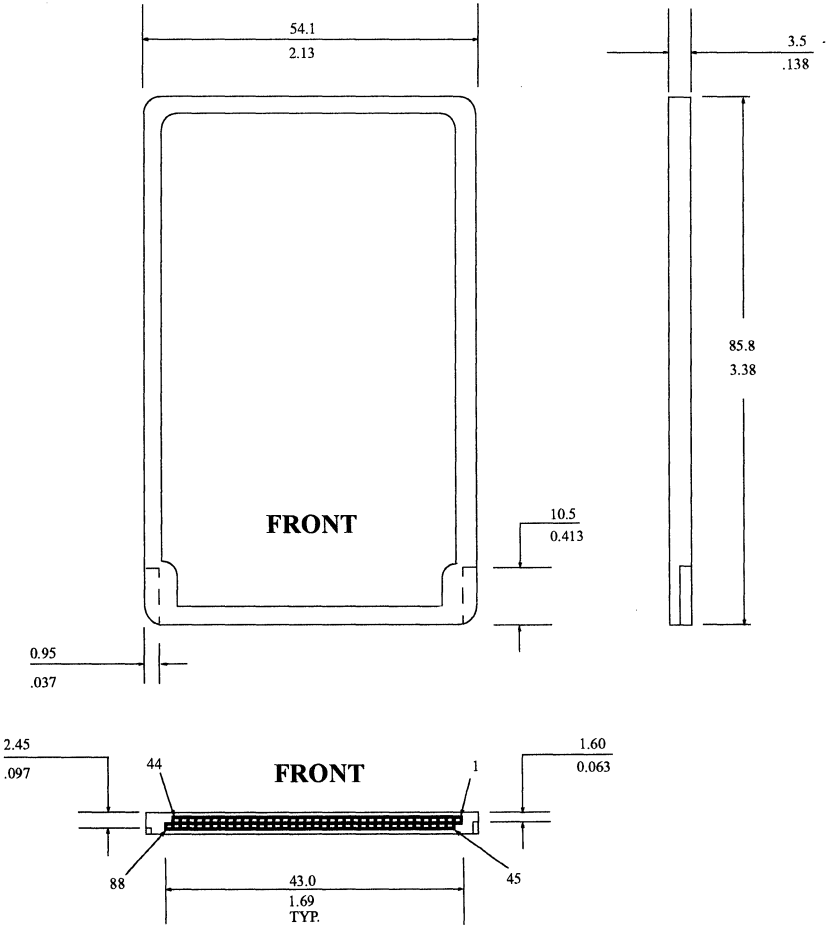
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 32 5.0V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

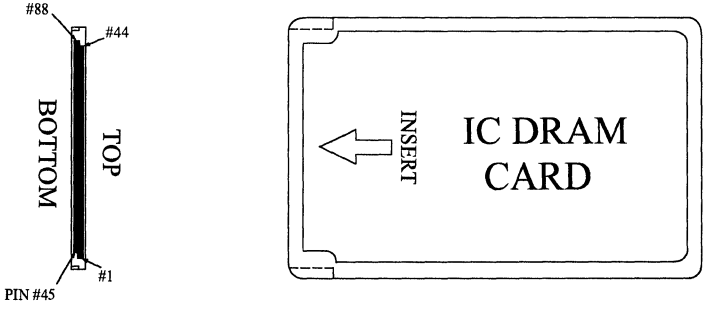
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	29ns
t_{AA}	Access Time From Address	46ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	50ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 5.0V, ± 0.25V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- 10/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 1024 refresh cycles distributed across 128ms
- Polarized Connector

Description

The IBM11J2320BL is a 8MB industry standard 88-pin IC DRAM card. It is organized as a 2M x 32 high speed memory array. It is built using 16 - 1Mx4 devices and is compatible to the JEDEC/PCMCIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x32 configuration the memory may be utilized as two banks, each having four unique bytes. The x16 configuration may be utilized as four banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other banks in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. The related 2M x 36 version of this ICDRAM card is IBM11J2360BLA

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

Pinout

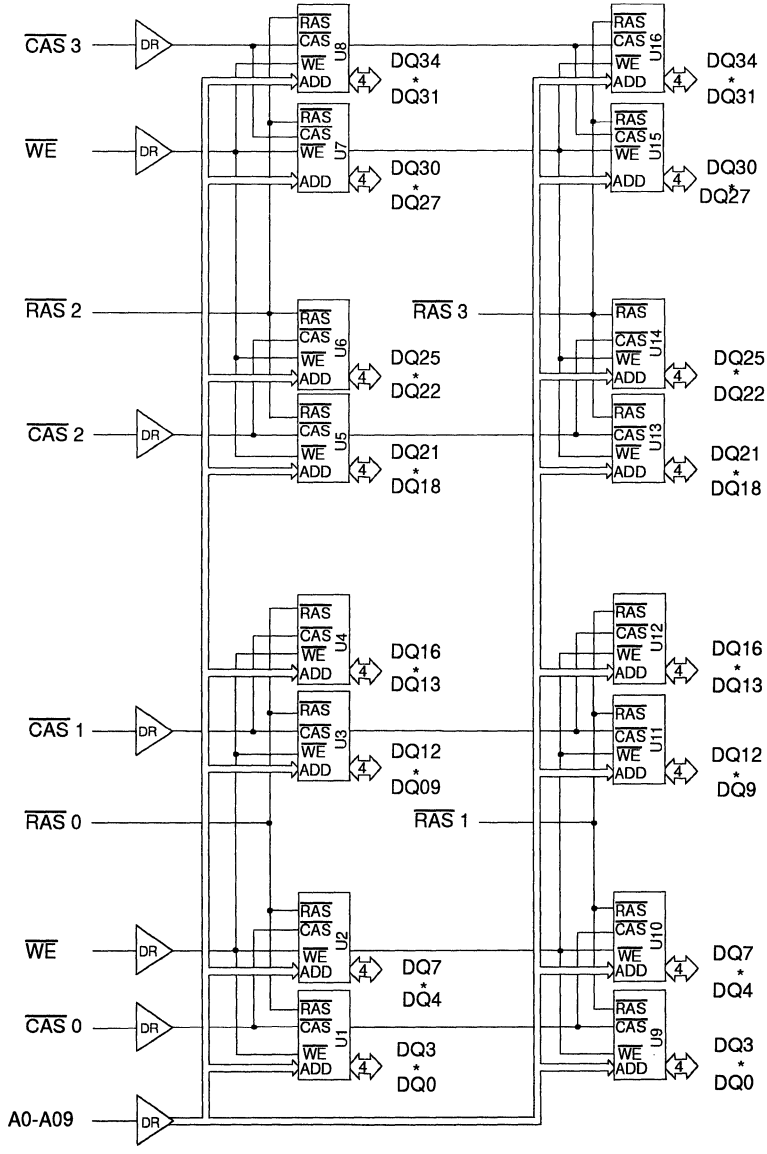
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	NC	47	DQ19	69	$\overline{RAS3}$
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	V_{CC}	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	V_{CC}	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	NC	76	PD8
11	NC	33	NC	55	NC	77	NC
12	NC	34	DQ9	56	V_{SS}	78	NC
13	A0	35	NC	57	A1	79	NC
14	A2	36	DQ10	58	A3	80	DQ27
15	V_{CC}	37	V_{CC}	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	NC	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	NC	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	NC	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	$\overline{RAS1}$	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

1. DQ numbering is compatible with parity (x36) version)

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J2320BLA-70	2M x 32	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	NC
PD3	V_{SS}
PD4	V_{SS}
PD5 (Number of Banks/Organization)	V_{SS}
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +6.0	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-1.0 to +6.0	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-1.0 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	11.8	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.4	—	V_{CC} + 0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	57	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O}$	Output Capacitance (DQ0~DQ34)	32	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	800	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	32	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	800	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	800	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	3.2	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	800	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			4.8	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 10ns ($\overline{CAS}$, $\overline{WE}$) or 11ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	11	—	ns	
t_{RAH}	Row Address Hold Time	10	—	ns	
t_{ASC}	Column Address Setup Time	3	—	ns	
t_{CAH}	Column Address Hold Time	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	42	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	24	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	29	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	20	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 21ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 23ns (6ns before max t_{CAC} of 29ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	15	—	ns	
t_{WP}	Write Command Pulse Width	16	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	25	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	29	ns	1, 2
t_{AA}	Access Time from Address	—	46	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	46	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	29	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	50	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	49	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	49	ns	1, 2

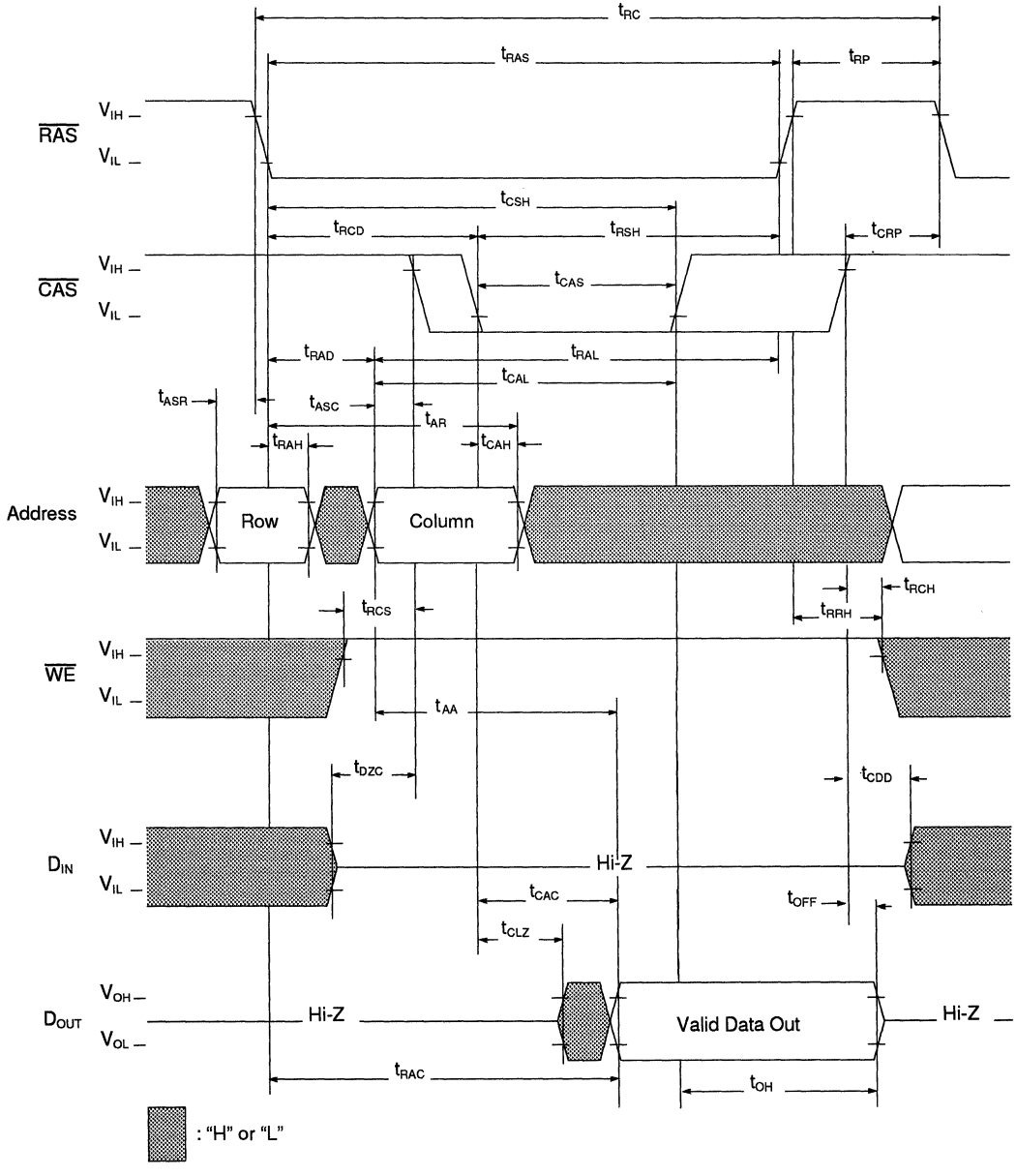
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

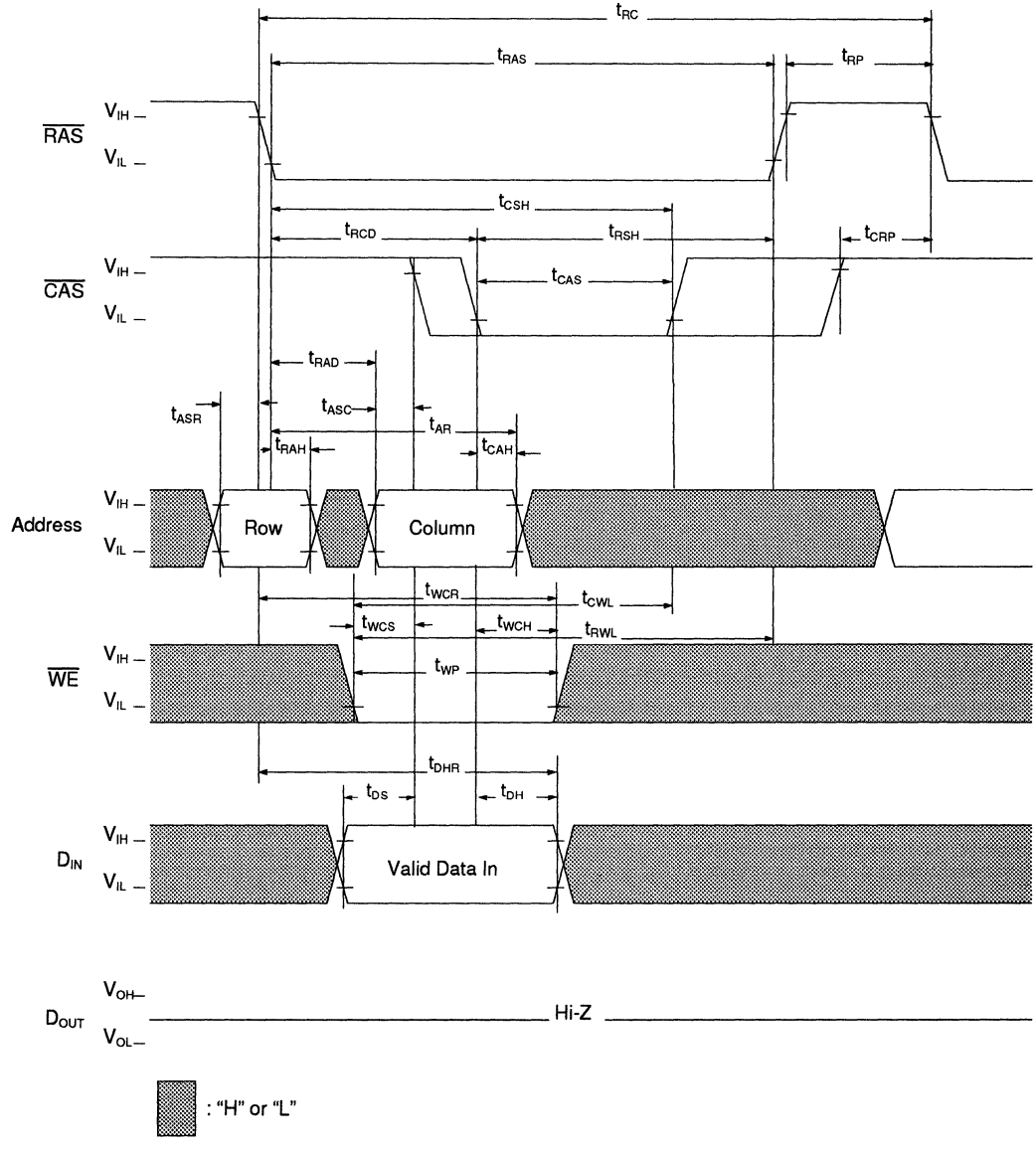
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	13	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	8	—	ns	
t_{REF}	Refresh Period	—	128	ms	1

1. 1024 refreshes are required every 128ms.

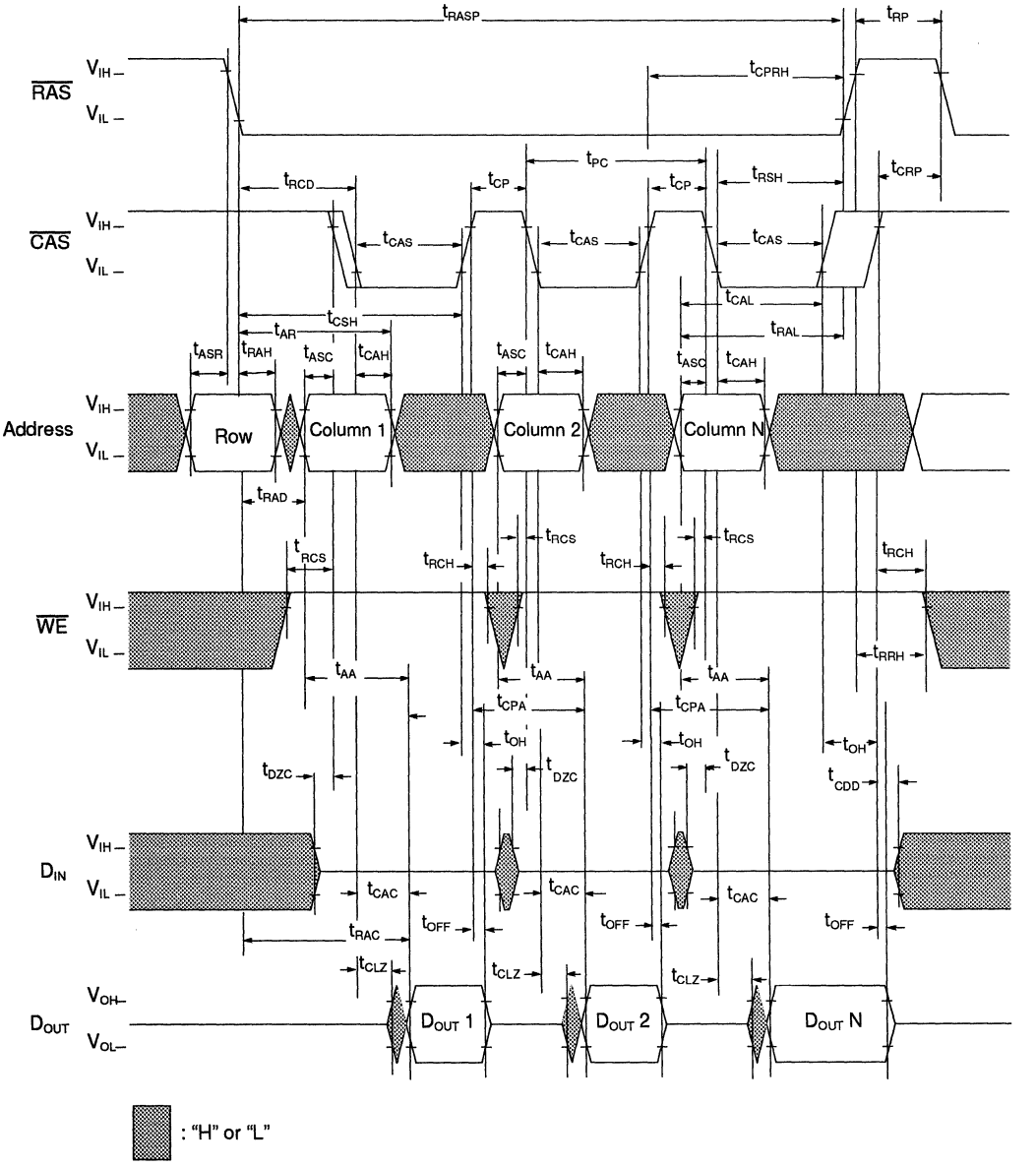
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

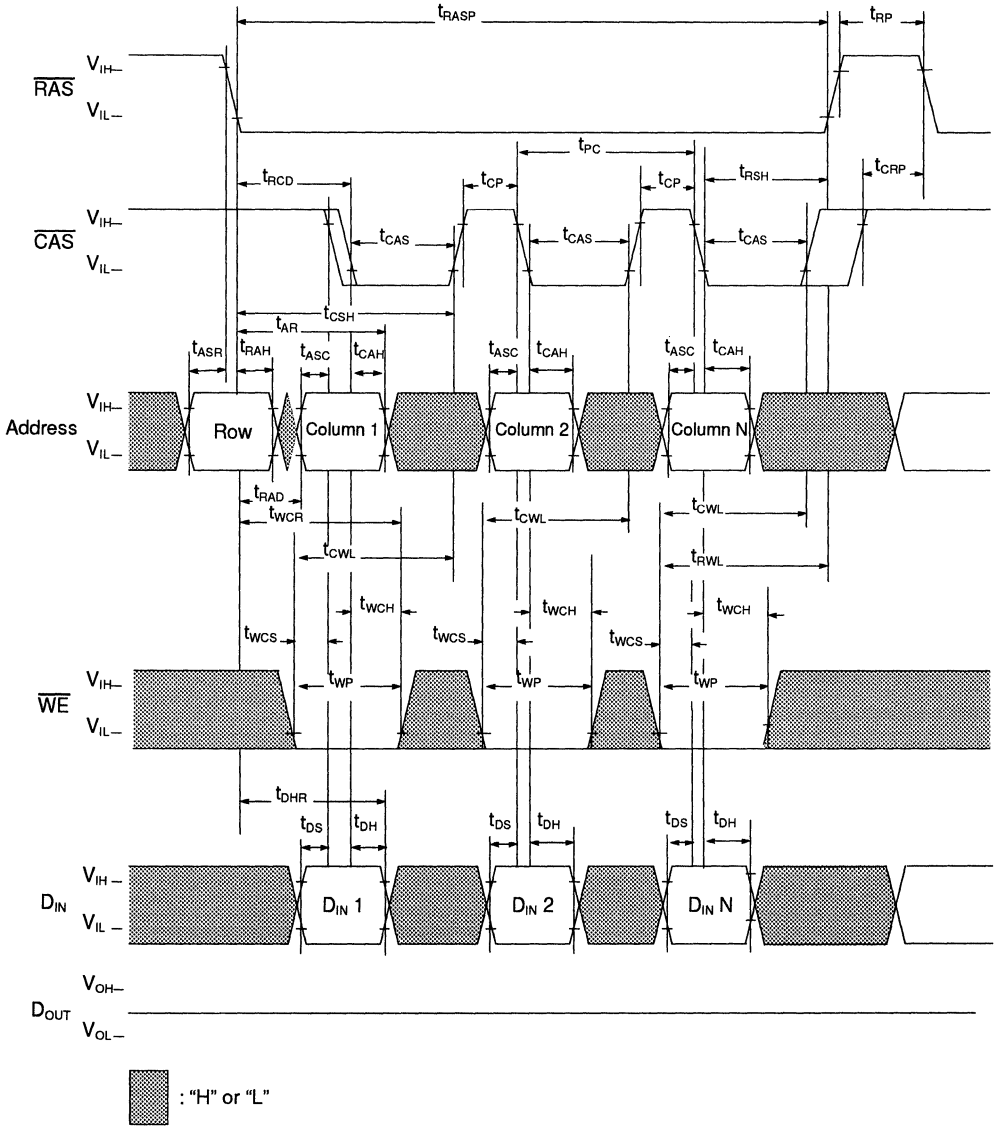
Write Cycle (Early Write)



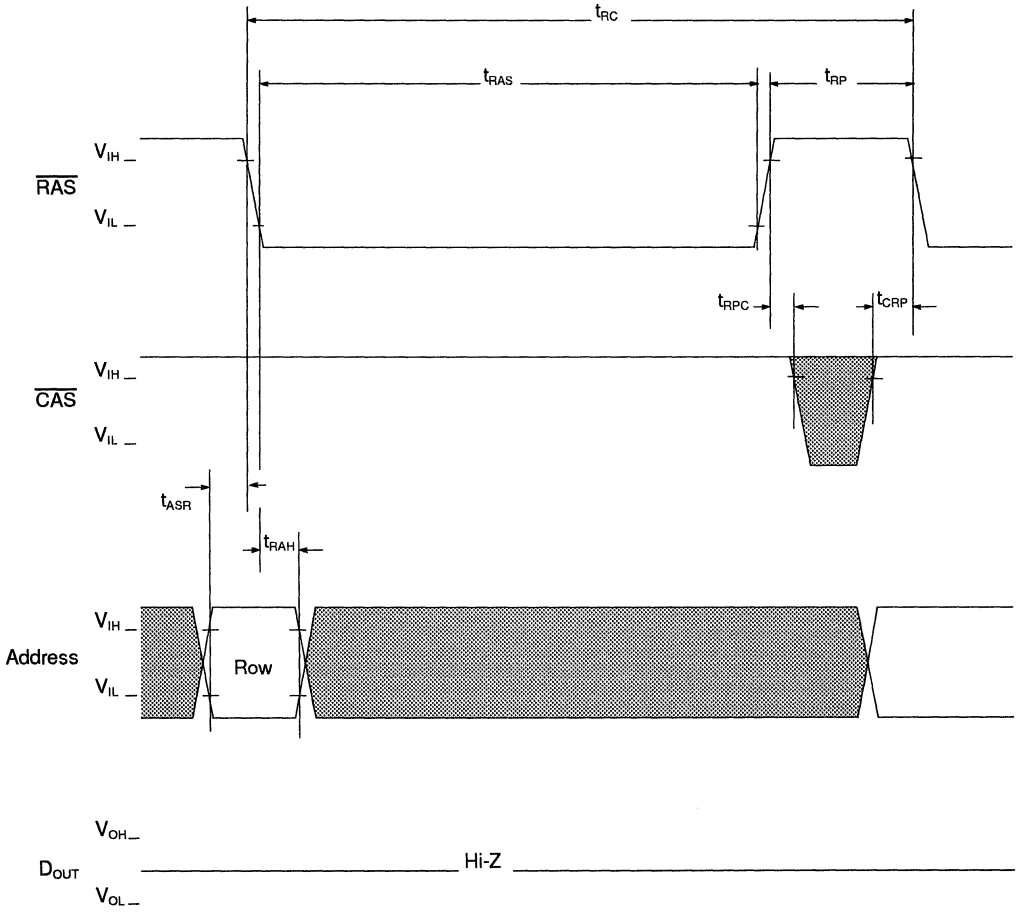
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

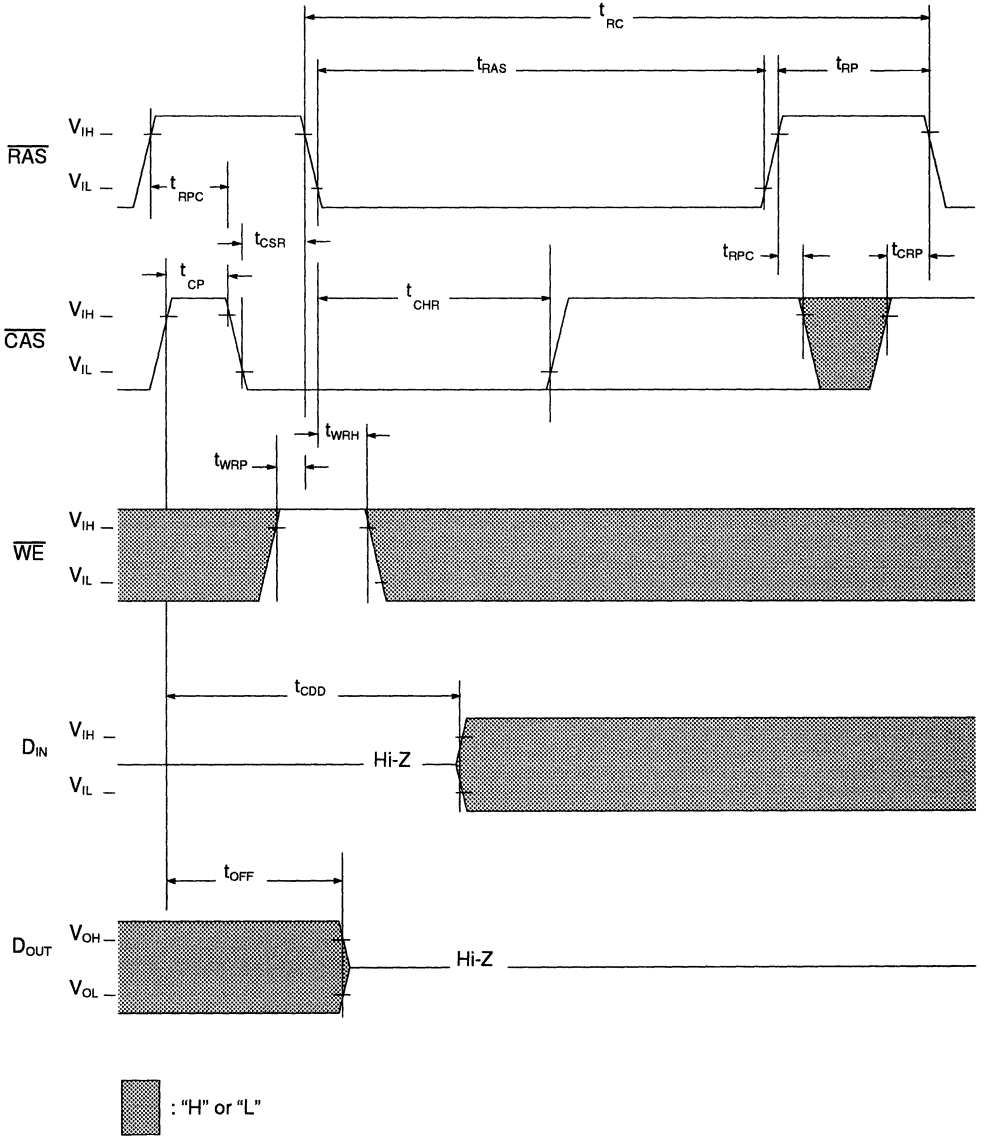


$\overline{RAS}$ Only Refresh Cycle



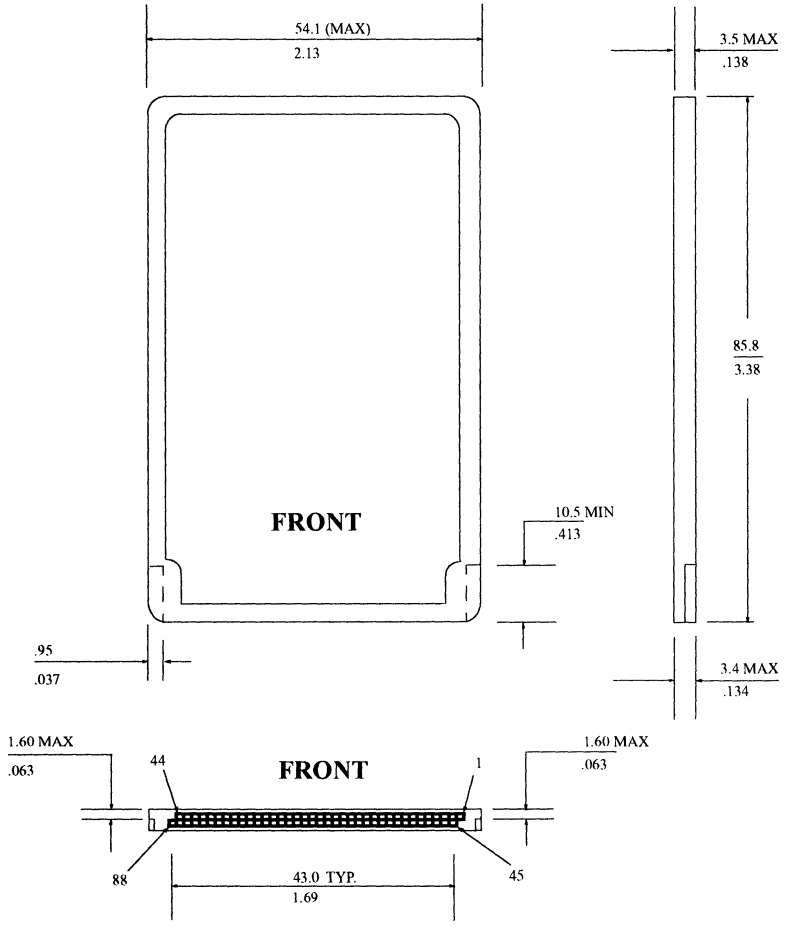
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 32 3.3V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

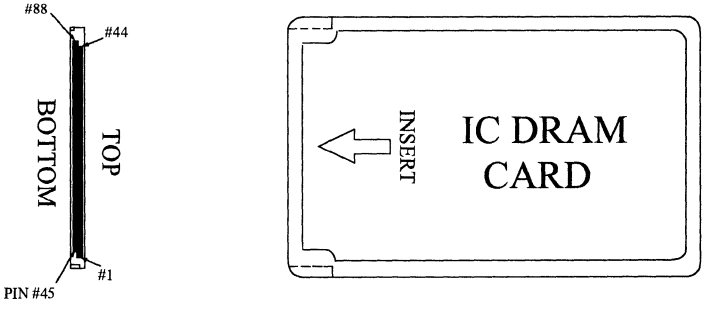
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	24ns
t_{AA}	Access Time From Address	40ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 3.3V, ± 0.3V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- 10/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 1024 refresh cycles distributed across 128ms
- Polarized Connector

Description

The IBM11J2320BN is a 8MB industry standard 88-pin IC DRAM card. It is organized as a 2M x 32 high speed memory array. It is built using 16 1Mx4 devices and is compatible to the JEDEC/PCM-CIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x32 configuration the memory may be utilized as two banks, each having four unique bytes. The x16 configuration may be utilized as four banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other banks in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. **Caution must be used to prevent insertion into a 5.0V application.**

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

Pinout

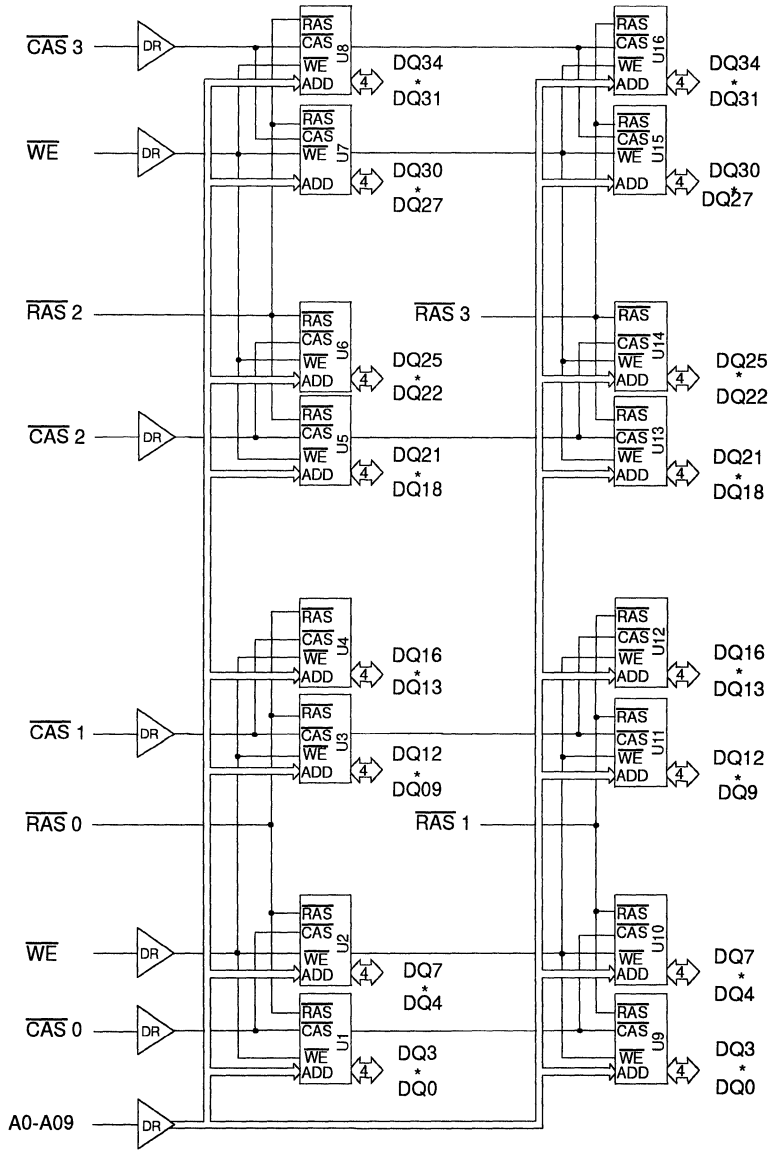
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	V_{CC}	47	DQ19	69	$\overline{RAS3}$
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	NC	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	NC	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	NC	76	PD8
11	V_{CC}	33	NC	55	NC	77	NC
12	NC	34	DQ9	56	V_{SS}	78	NC
13	A0	35	V_{CC}	57	A1	79	NC
14	A2	36	DQ10	58	A3	80	DQ27
15	NC	37	NC	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	V_{CC}	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	NC	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	NC	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	$\overline{RAS1}$	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

1. DQ numbering is compatible with parity (x36) version)

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J2320BNA-70	2M x 32	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	NC
PD3	V_{SS}
PD4	V_{SS}
PD5 (Number of Banks/Organization)	V_{SS}
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +4.1	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to +4.1	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to +4.1	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	4.6	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.0	—	V_{CC} + 0.3	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.3	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	43	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O}$	Output Capacitance (DQ0~DQ34)	32	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 3.3± 0.3V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	640	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	16	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	640	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	520	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	4.0	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	640	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			4.8	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 3.3± 0.3V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays:1ns minimum, 4ns ($\overline{CAS}$, $\overline{WE}$) or 5ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	—	ns	2
t_{ASR}	Row Address Setup Time	5	—	ns	
t_{RAH}	Row Address Hold Time	9	—	ns	
t_{ASC}	Column Address Setup Time	2	—	ns	
t_{CAH}	Column Address Hold Time	16	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	19	46	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	14	30	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	24	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	69	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	14	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 20ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 21ns (3ns before max t_{CAC} of 24ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	19	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	24	ns	1, 2
t_{AA}	Access Time from Address	—	40	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	1	—	ns	
t_{OH}	Output Data Hold Time	1	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	24	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	1	24	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	44	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	44	ns	1, 2

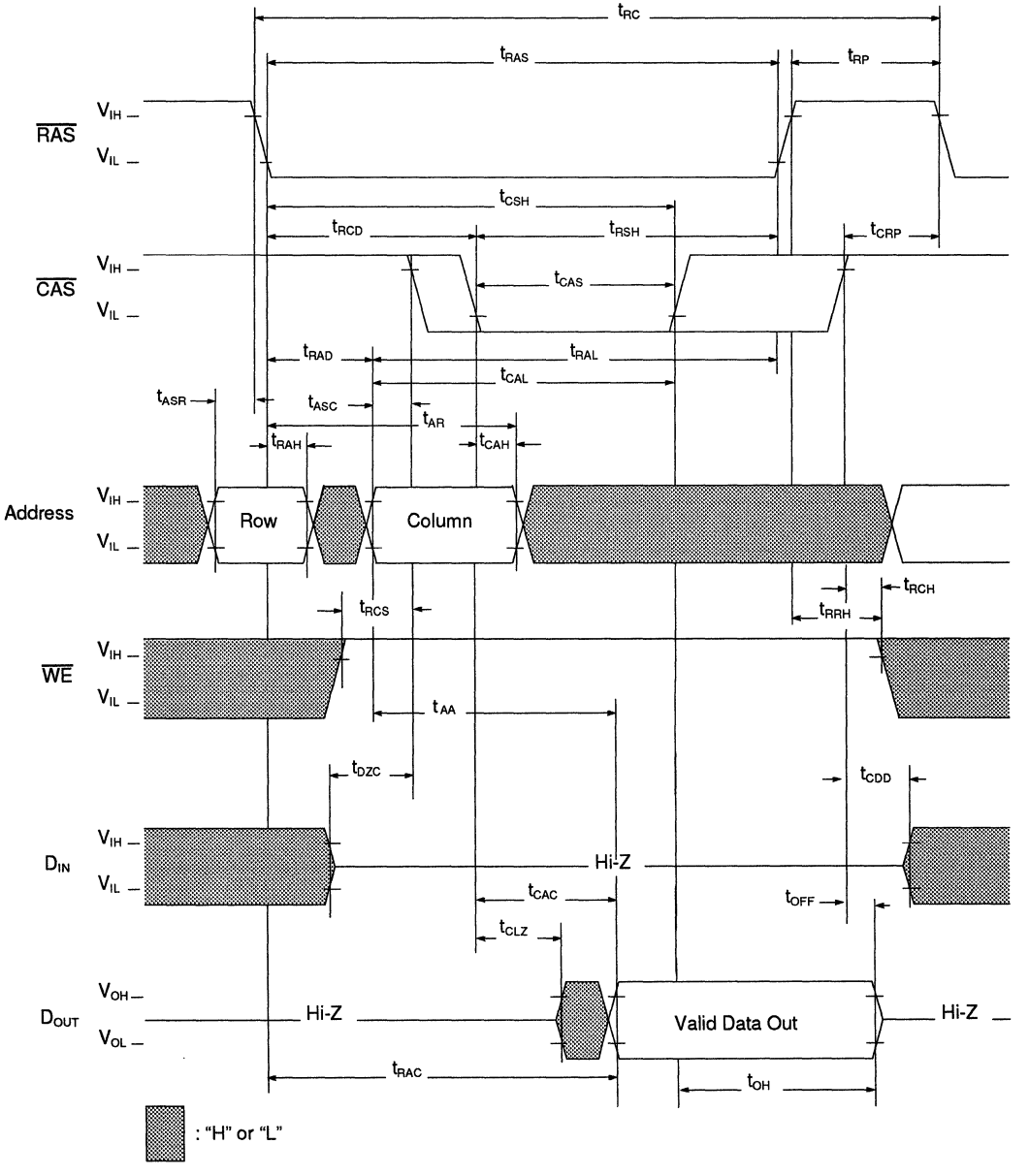
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

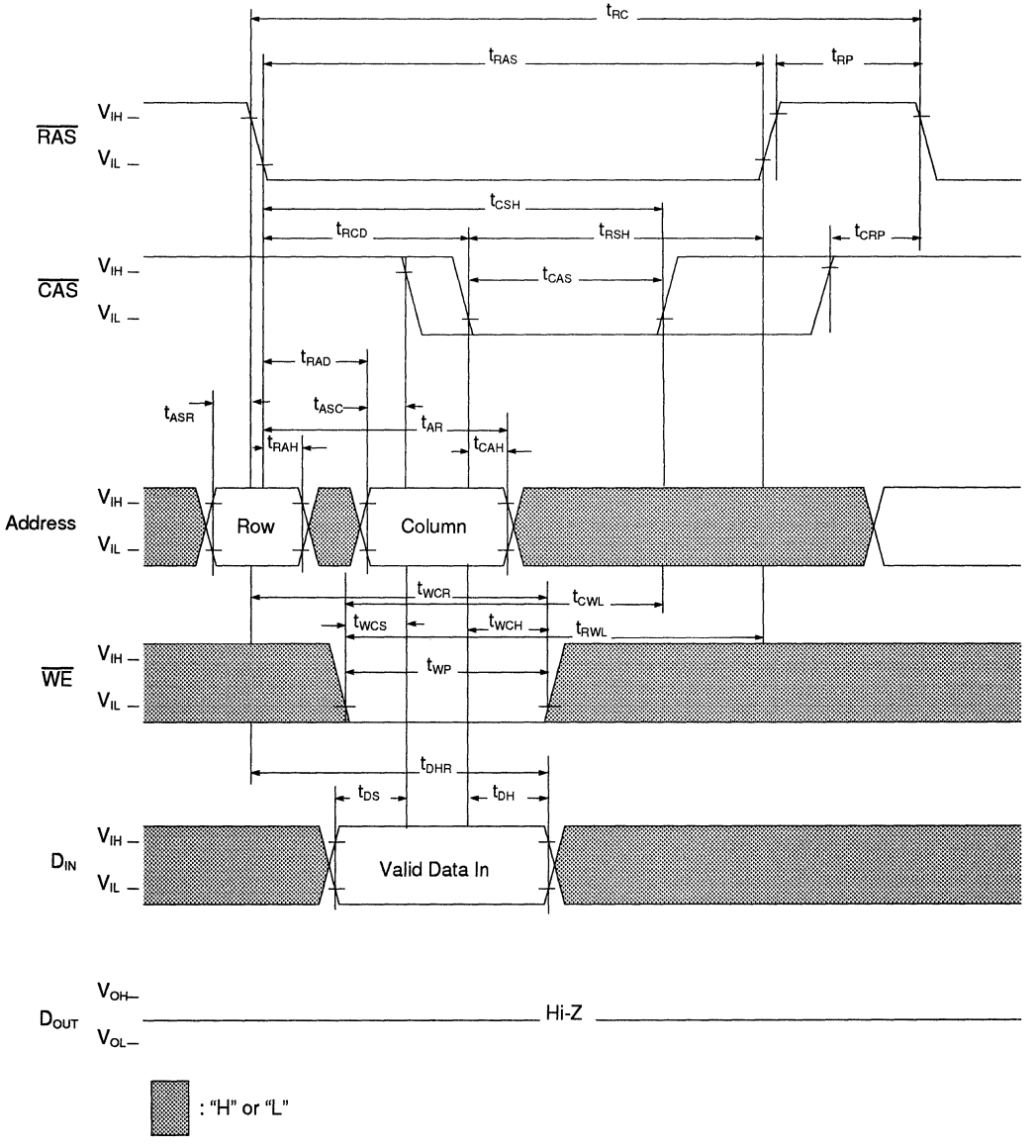
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	9	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	14	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	9	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	9	—	ns	
t_{REF}	Refresh Period	—	128	ms	1

1. 1024 refreshes are required every 128ms.

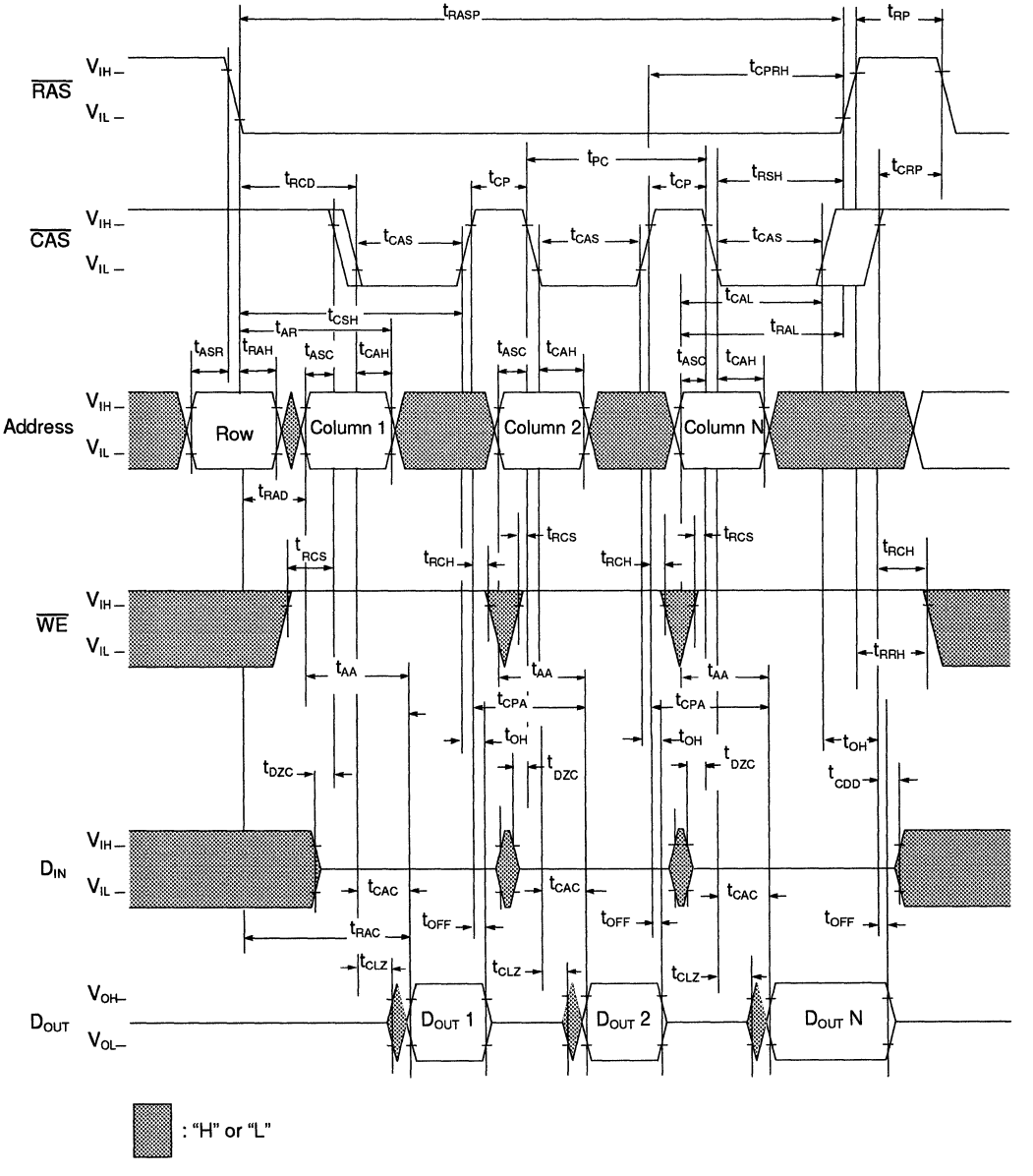
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

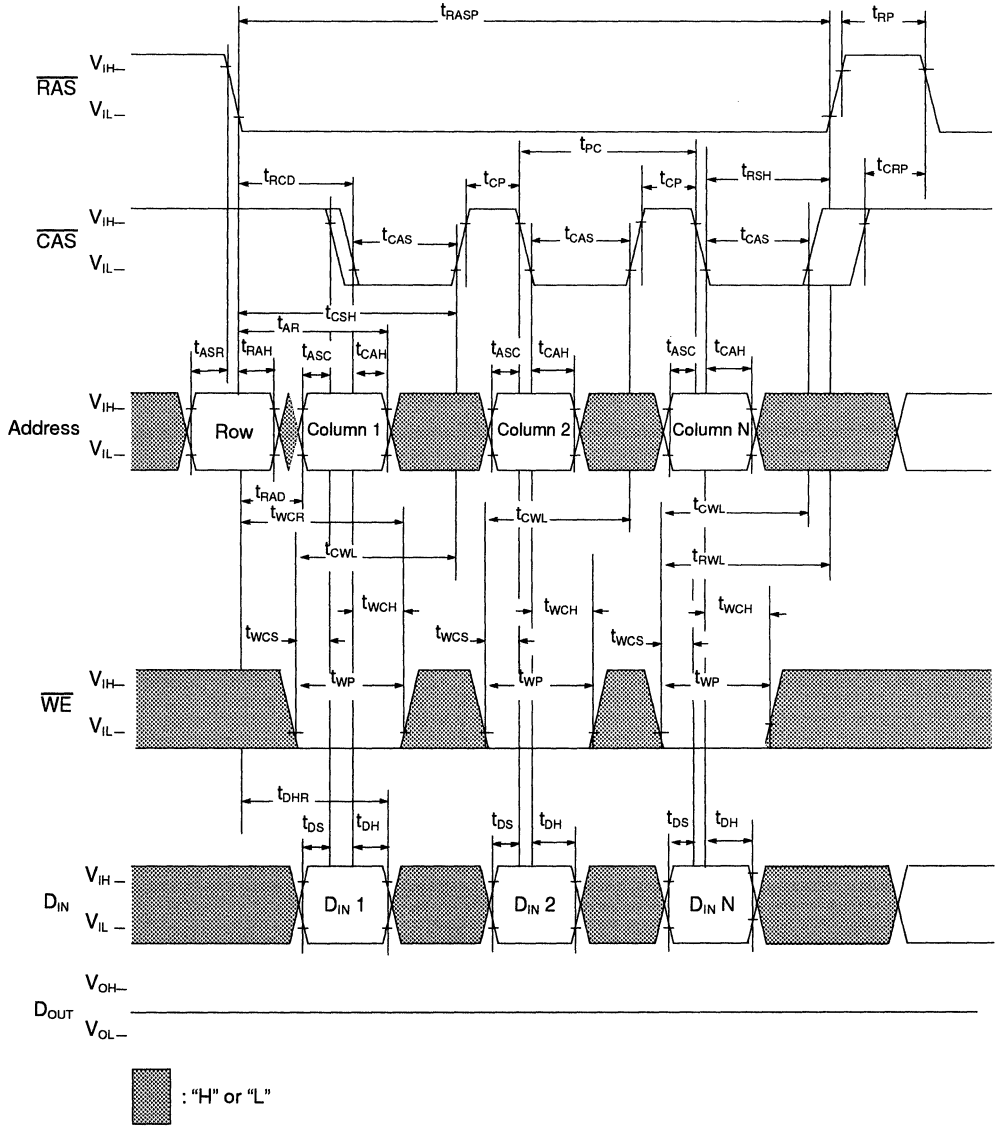
Write Cycle (Early Write)



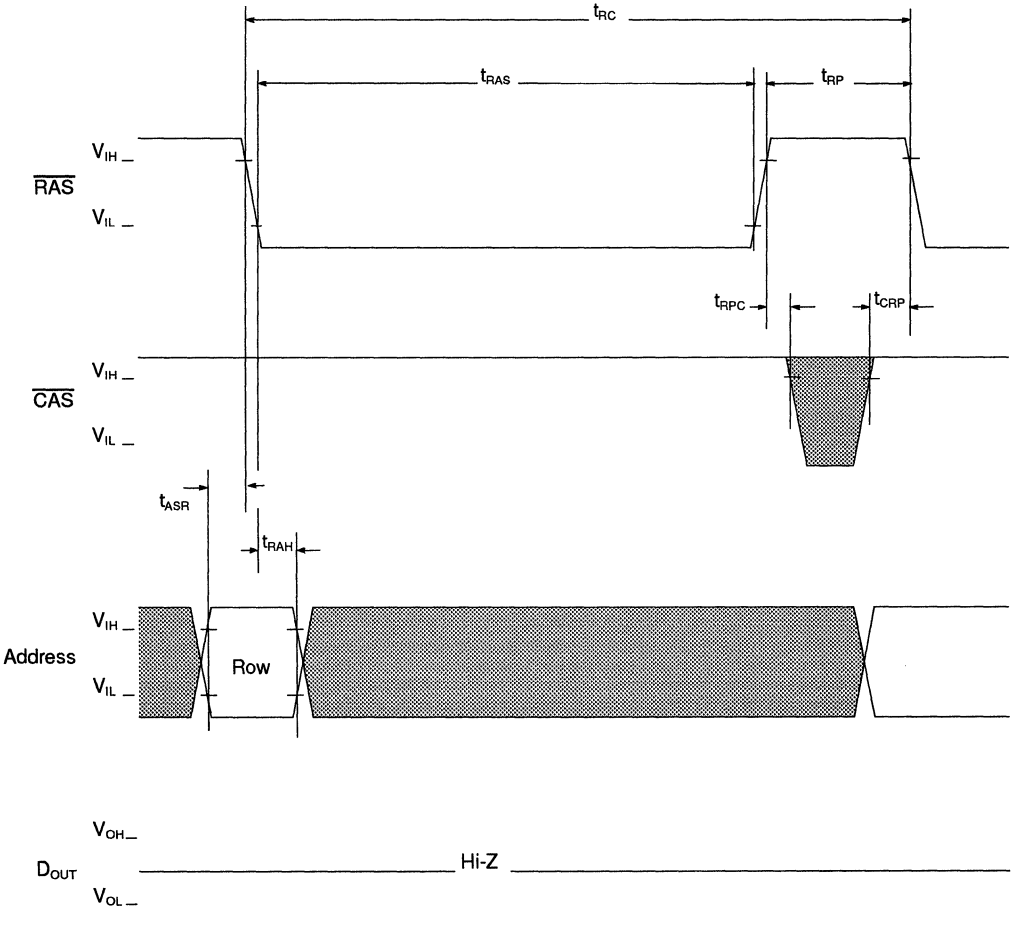
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



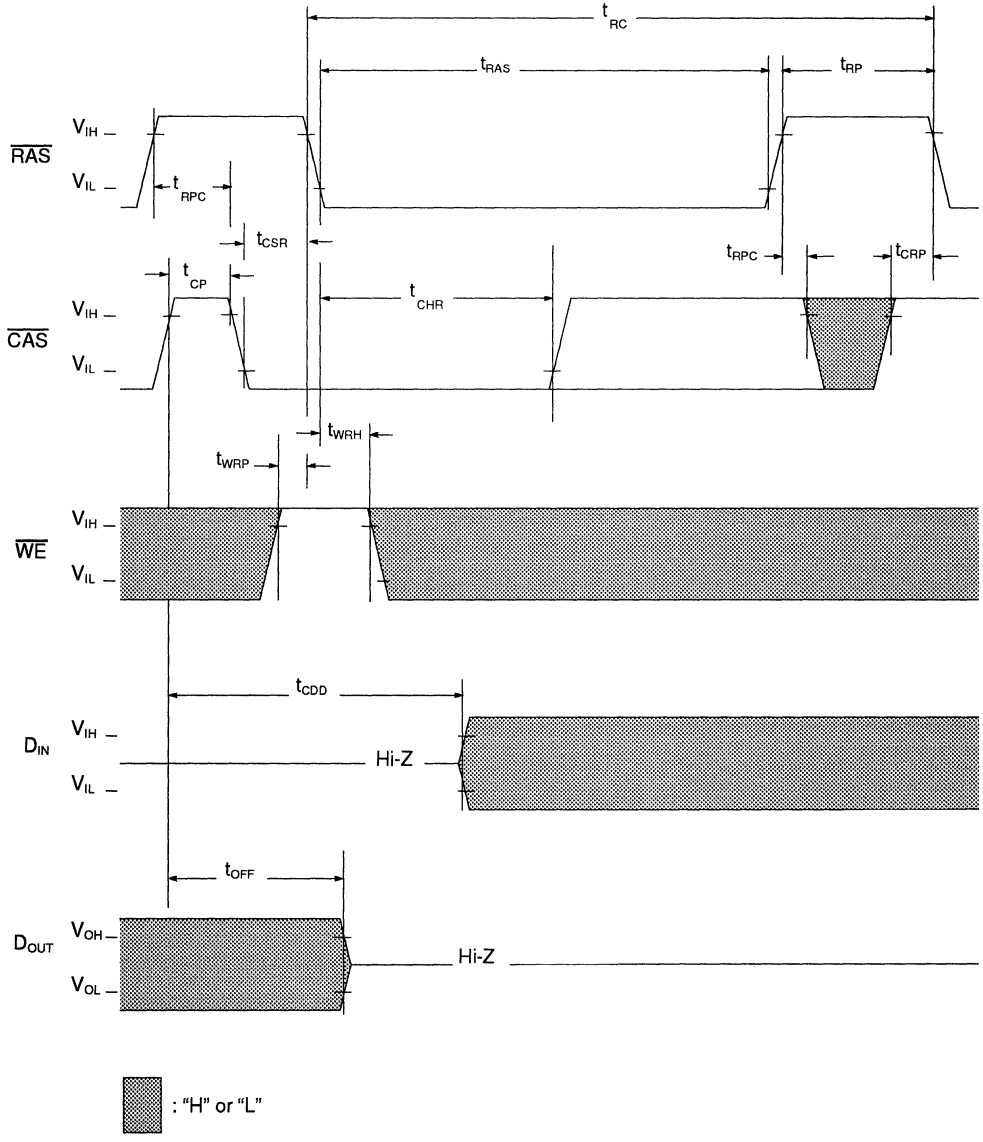
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

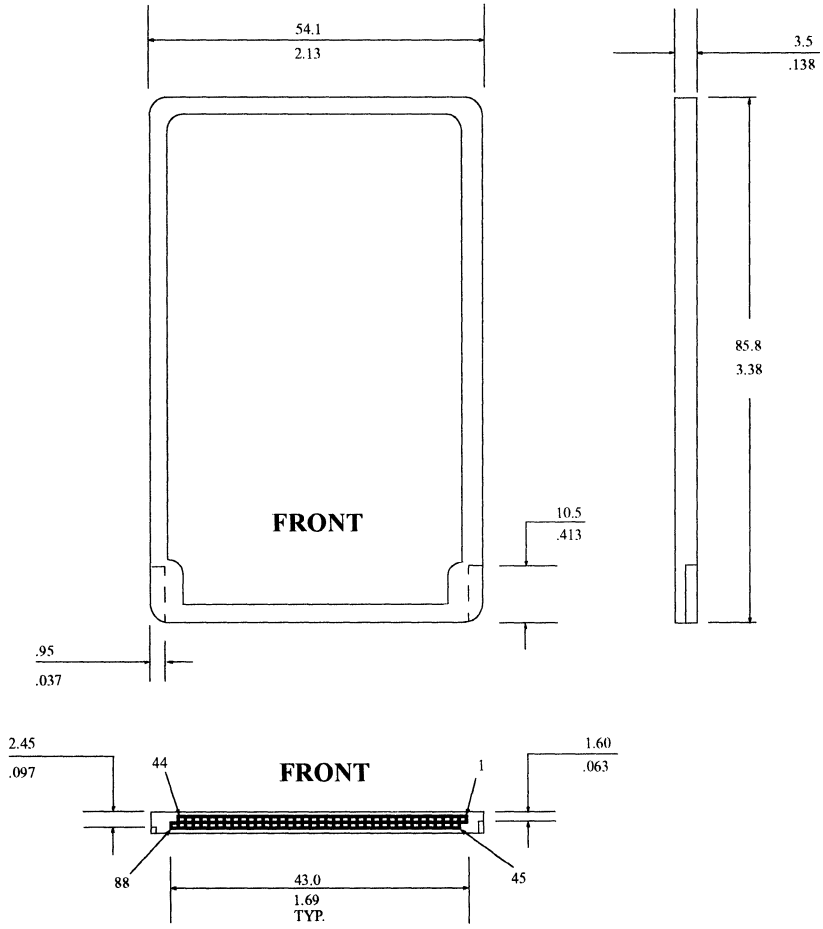
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 32 5.0V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

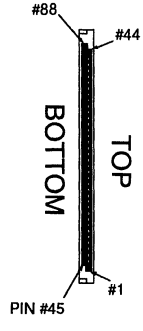
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns
t_{AA}	Access Time From Address	46ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

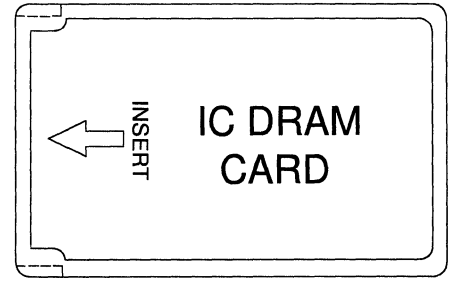
- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 5.0V, ± 0.25V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- 11/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 2048 refresh cycles distributed across 256ms
- Polarized Connector

Description

The IBM11J2320HL is a 8MB industry standard 88-pin IC DRAM card. It is organized as a 2M x 32 high speed memory array. It is built using 4- 2Mx8 devices and is compatible to the JEDEC/PCM-CIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x32 configuration the memory is a single bank, having four unique bytes. The x16 configuration may be utilized as two banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other bank in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications.

Card Outline





Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

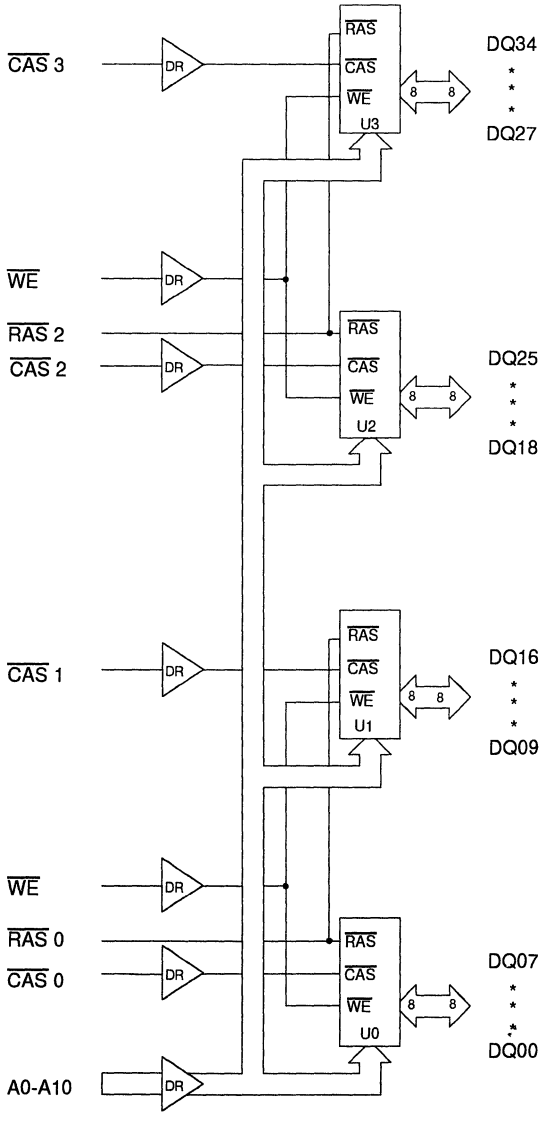
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	NC	47	DQ19	69	$\overline{NC}$
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	V_{CC}	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	V_{CC}	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	NC	76	PD8
11	NC	33	NC	55	NC	77	NC
12	NC	34	DQ9	56	V_{SS}	78	NC
13	A0	35	NC	57	A1	79	NC
14	A2	36	DQ10	58	A3	80	DQ27
15	V_{CC}	37	V_{CC}	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	NC	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	NC	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	A10	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	$\overline{NC}$	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J2320HLA-70	2M x 32	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	NC
PD2	NC
PD3	V_{SS}
PD4	V_{SS}
PD5 (Number of Banks/Organization)	NC
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +7.0	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to V_{CC} + 0.5, 7.0	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	2.1	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.4	—	V_{CC} + 0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	35	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O}$	Output Capacitance (DQ0~DQ34)	23	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	400	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	8	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	400	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	260	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	0.8	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	400	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			2.4	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 10ns ($\overline{CAS}$, $\overline{WE}$) or 11ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	11	—	ns	
t_{RAH}	Row Address Hold Time	8	—	ns	
t_{ASC}	Column Address Setup Time	3	—	ns	
t_{CAH}	Column Address Hold Time	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	42	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	30	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 21ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 23ns (7ns before max t_{CAC} of 30ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	16	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	25	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	30	ns	1, 2
t_{AA}	Access Time from Address	—	46	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	46	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	29	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	49	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	54	ns	1, 2

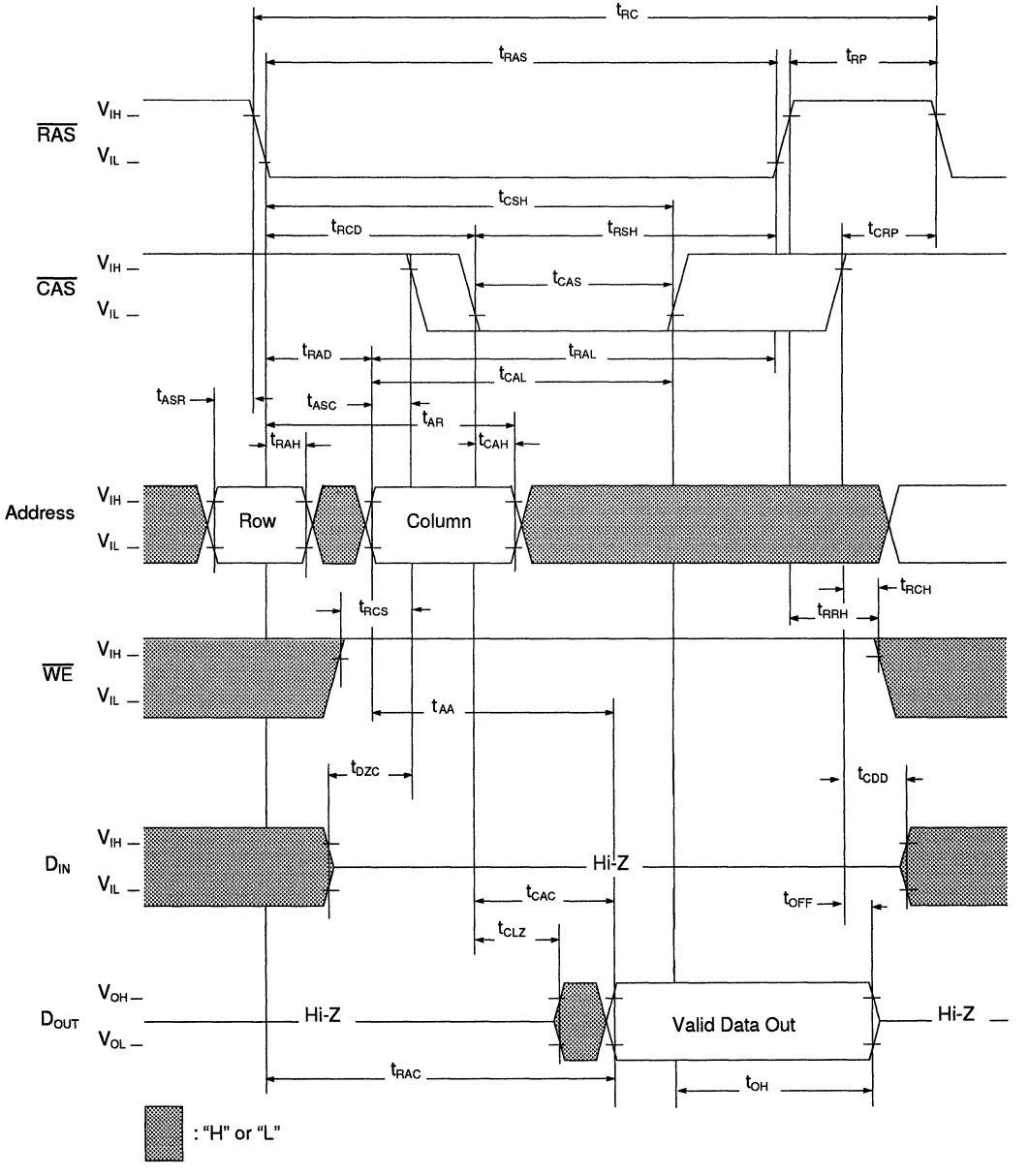
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

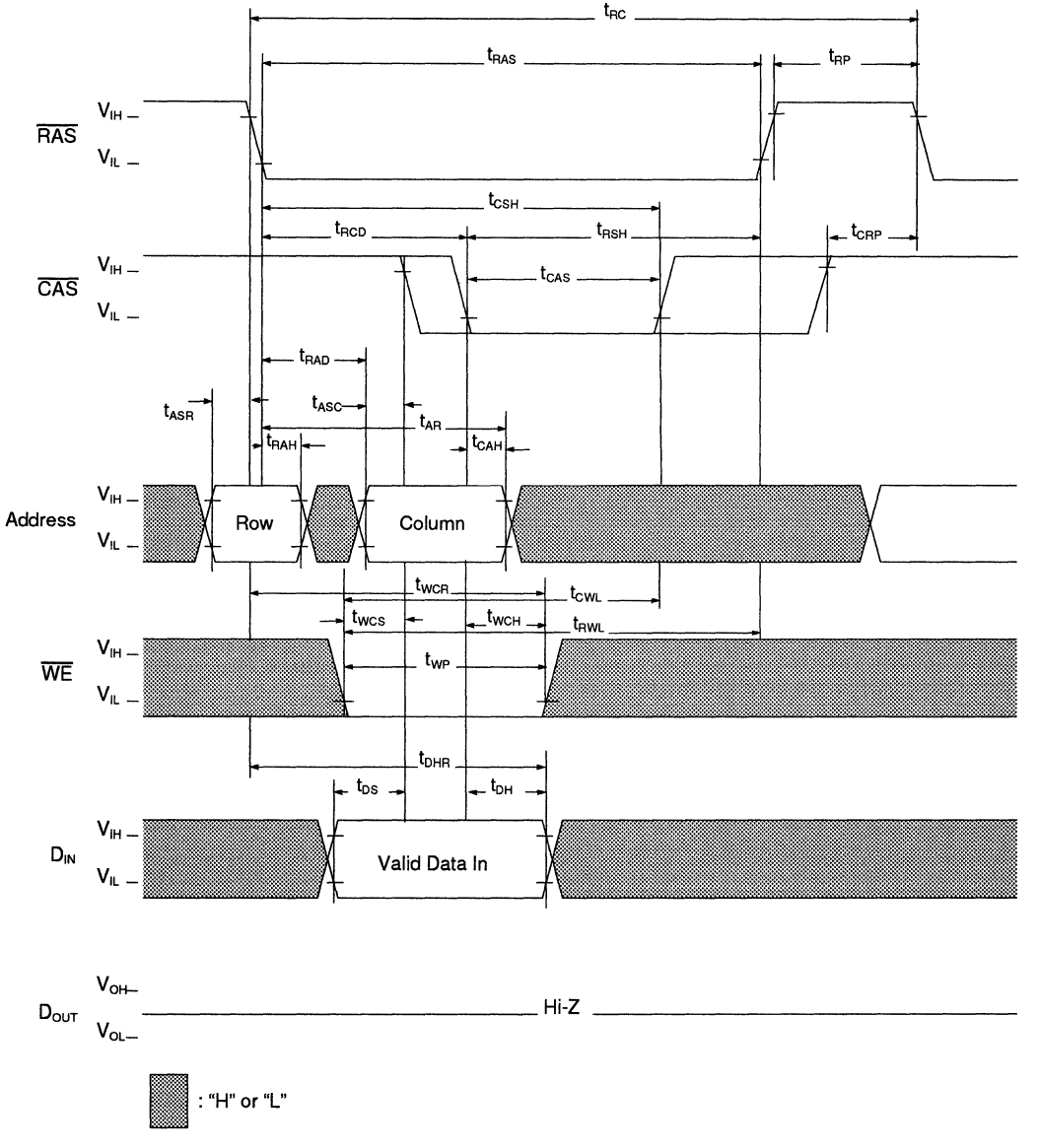
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	19	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	ns	
t_{REF}	Refresh Period	—	256	ns	1

1. 2048 refreshes are required every 256ms.

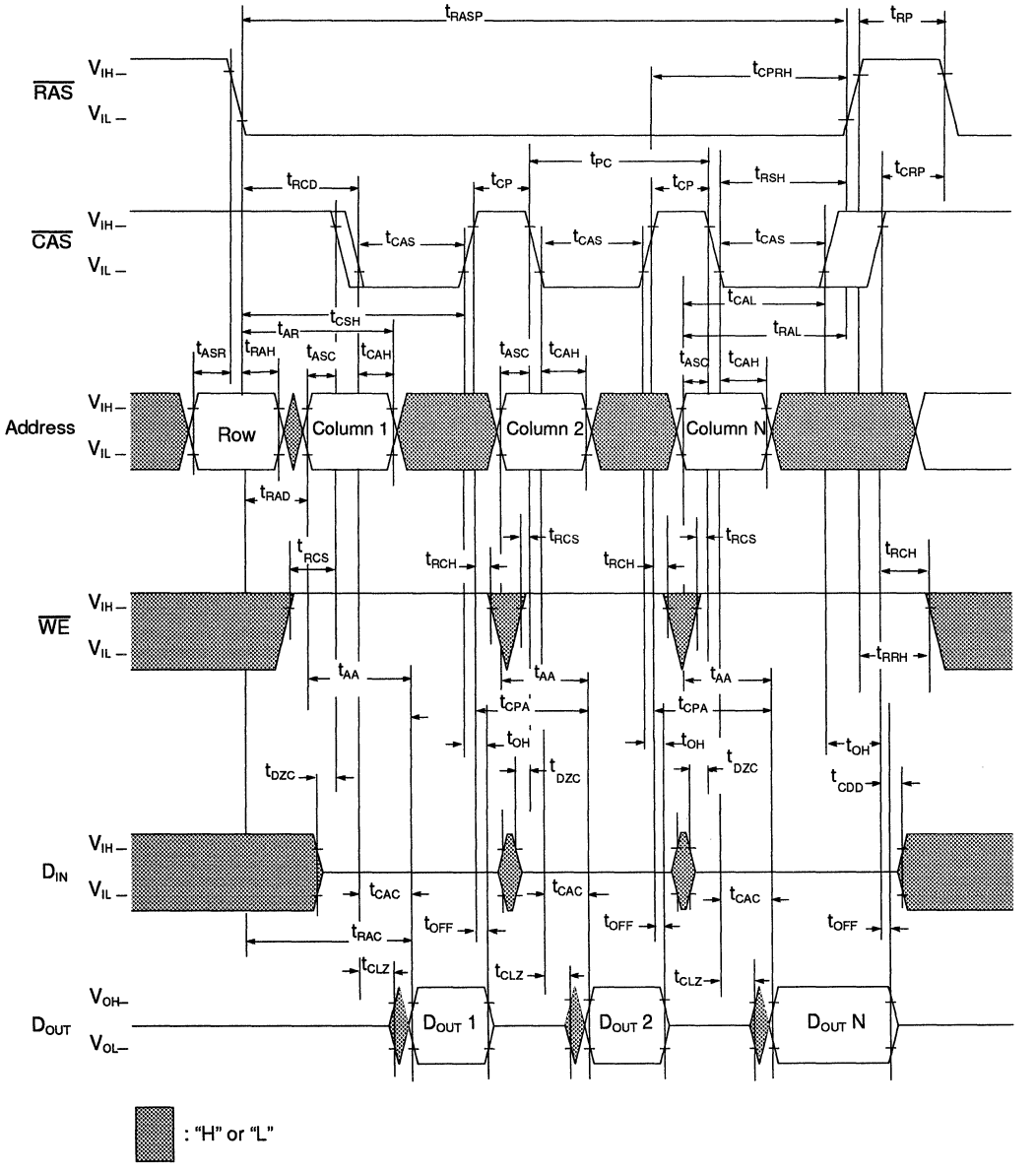
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCH
tRCS
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

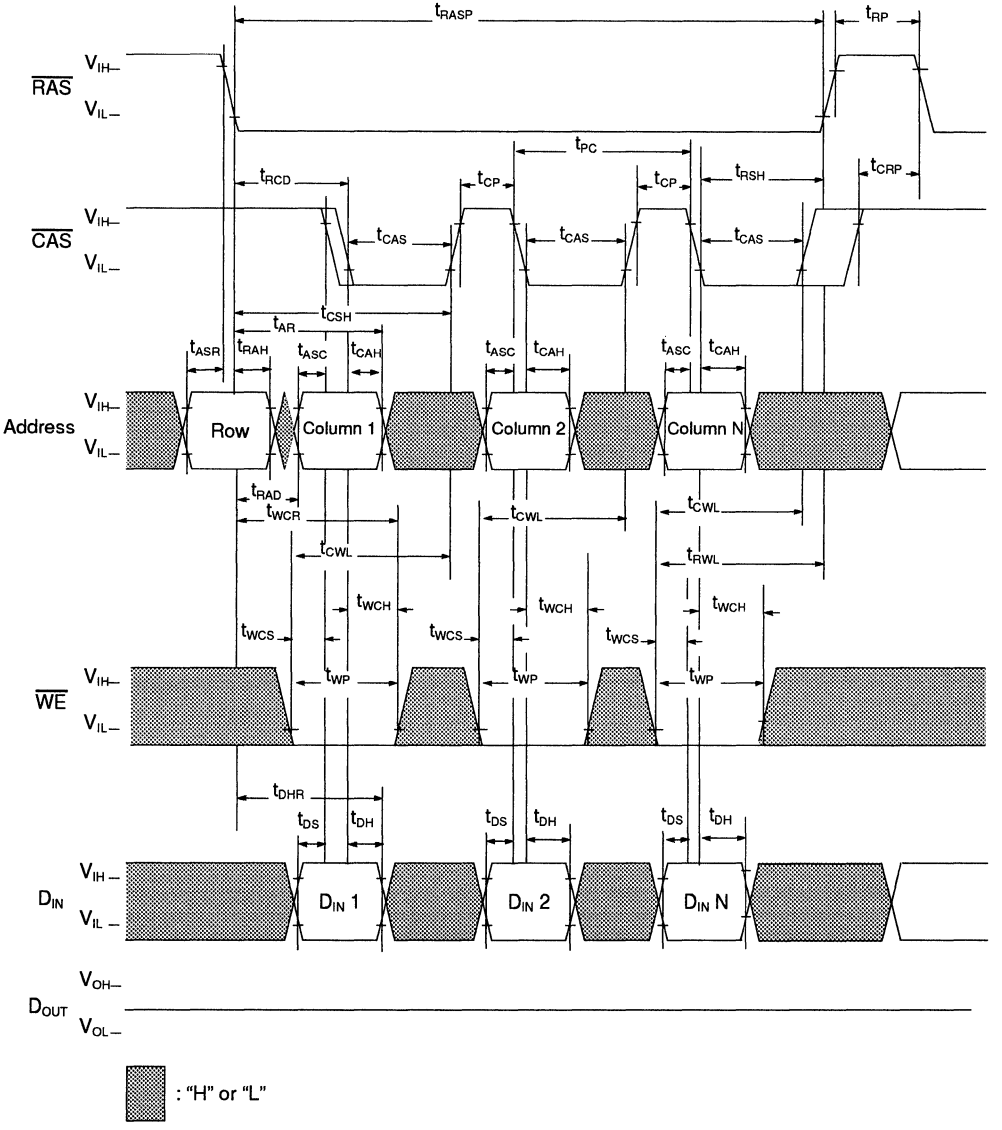
Write Cycle (Early Write)



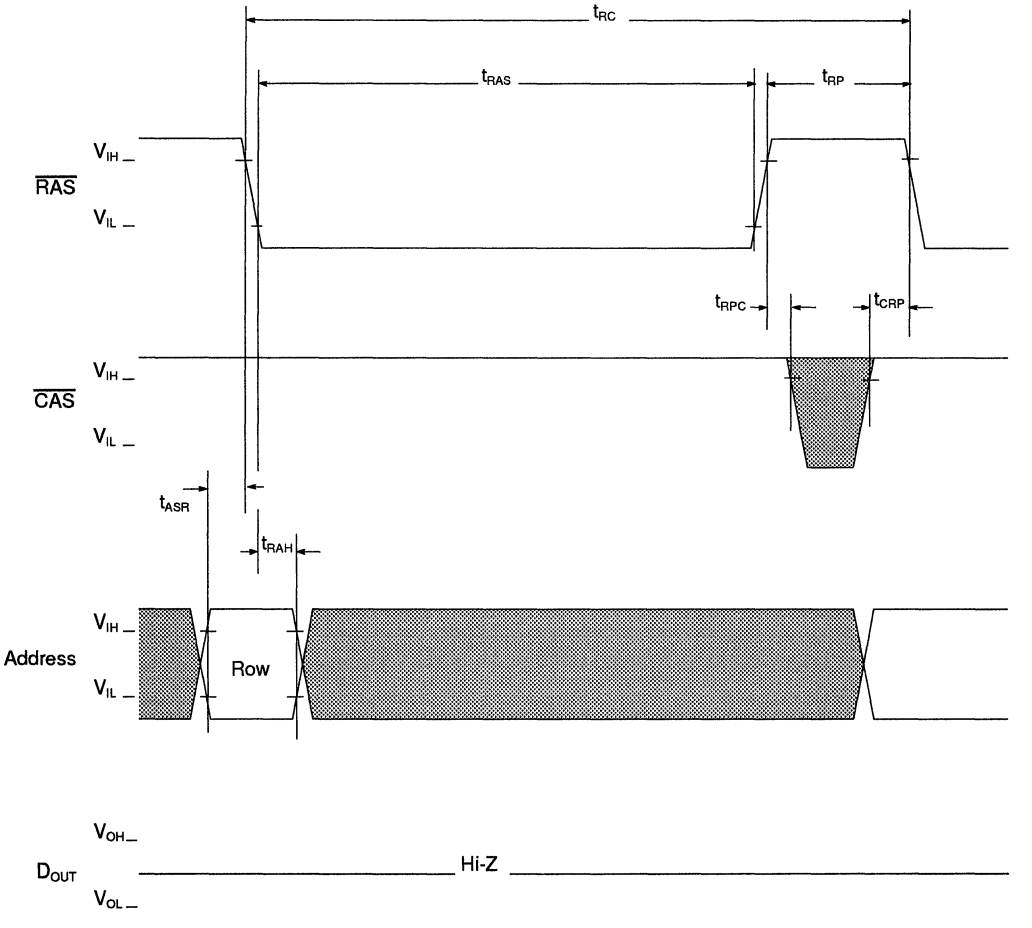
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



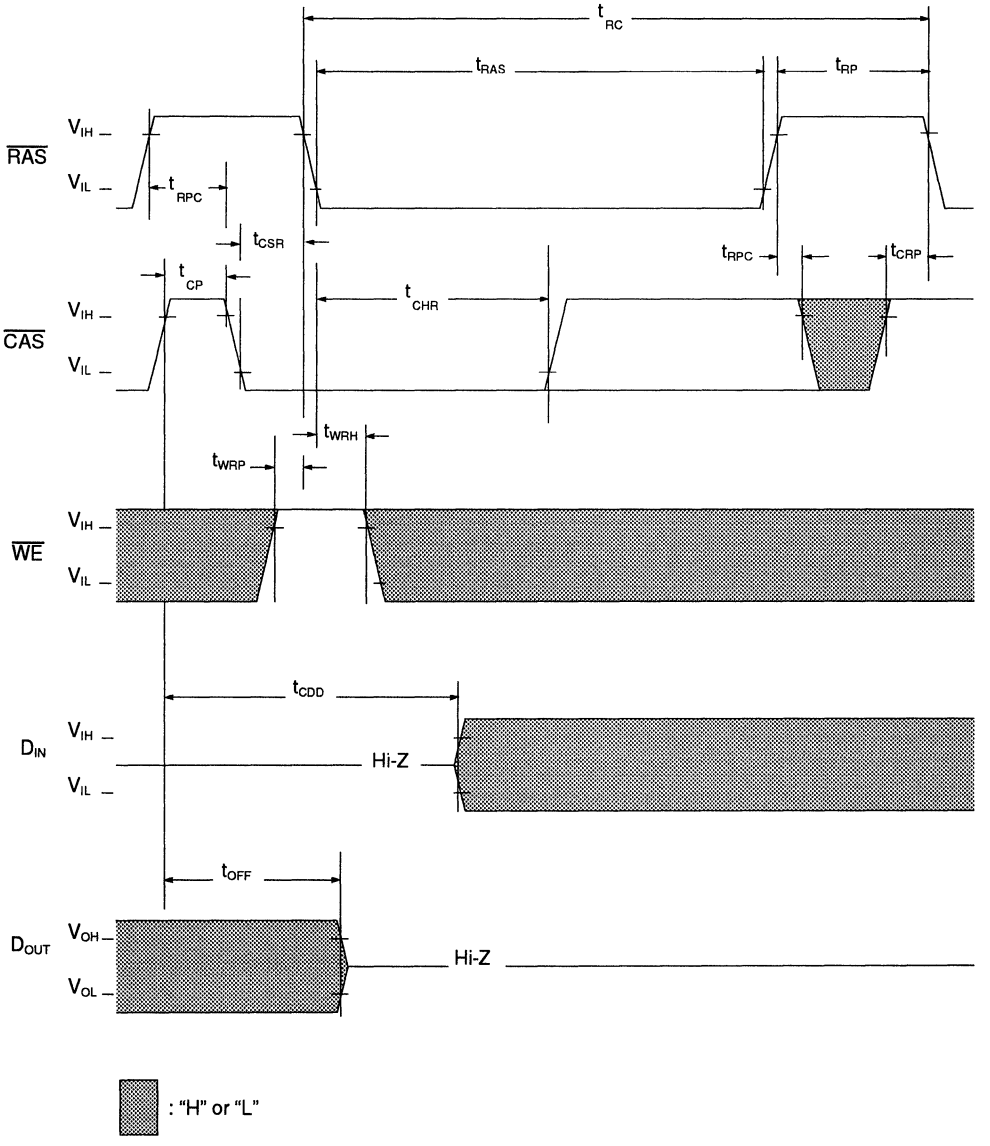
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

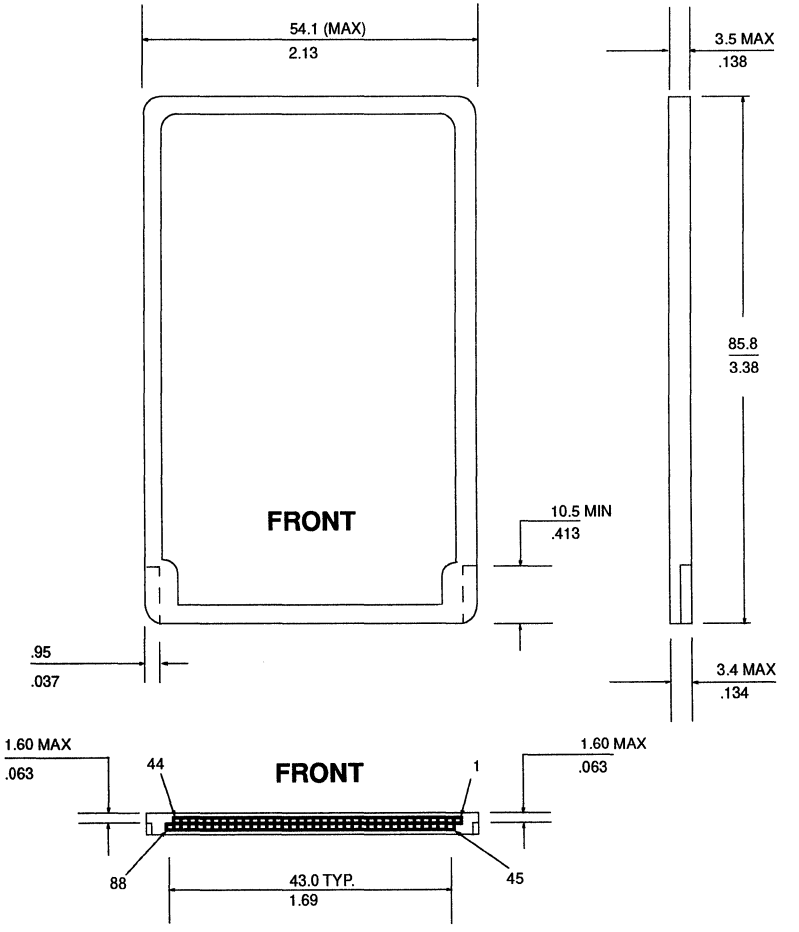
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 32 3.3V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

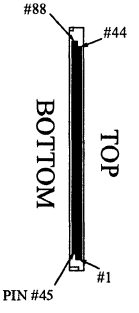
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	24ns
t_{AA}	Access Time From Address	40ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

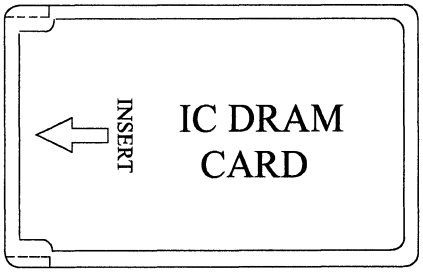
- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 3.3V, ± 0.3V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- 11/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 2048 refresh cycles distributed across 256ms
- Polarized Connector

Description

The IBM11J2320HN is a 8MB industry standard 88-pin IC DRAM card. It is organized as a 2M x 32 high speed memory array. It is built using 4- 2Mx8 devices and is compatible to the JEDEC/PCM-CIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x32 configuration the memory is a single bank, having four unique bytes. The x16 configuration may be utilized as two banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other bank in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications.

Card Outline





Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

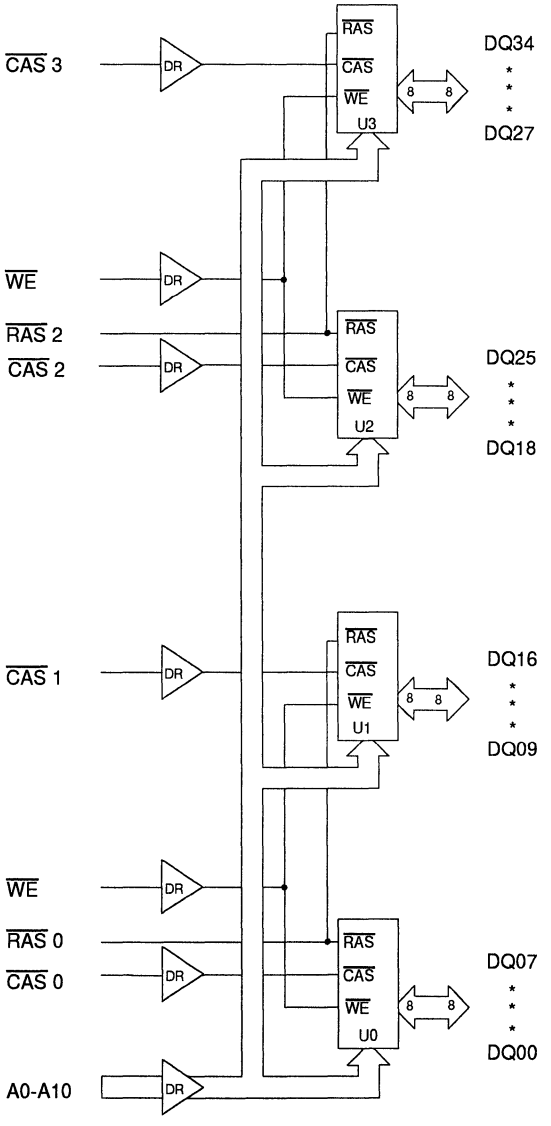
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	V_{CC}	47	DQ19	69	NC
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	NC	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	NC	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	NC	76	PD8
11	V_{CC}	33	NC	55	NC	77	NC
12	NC	34	DQ9	56	V_{SS}	78	NC
13	A0	35	V_{CC}	57	A1	79	NC
14	A2	36	DQ10	58	A3	80	DQ27
15	NC	37	NC	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	V_{CC}	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	NC	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	A10	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	NC	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J2320HNA-70	2M x 32	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	NC
PD2	NC
PD3	V_{SS}
PD4	V_{SS}
PD5 (Number of Banks/Organization)	NC
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +4.1	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to +4.1	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to +4.1	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	1.44	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.0	—	V_{CC}+0.3	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.3	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 3.3± 0.3V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	35	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O}$	Output Capacitance (DQ0~DQ34)	23	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 3.3± 0.3V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	400	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	8	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	400	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	260	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	0.8	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	400	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			2.4	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 3.3± 0.3V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 1ns minimum, 4ns ($\overline{CAS}$, $\overline{WE}$) or 5ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	11	—	ns	
t_{RAH}	Row Address Hold Time	8	—	ns	
t_{ASC}	Column Address Setup Time	3	—	ns	
t_{CAH}	Column Address Hold Time	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	42	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	30	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 21ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 23ns (7ns before max t_{CAC} of 30ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	25	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	24	ns	1, 2
t_{AA}	Access Time from Address	—	40	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	1	—	ns	
t_{OH}	Output Data Hold Time	1	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	24	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	1	24	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	44	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	44	ns	1, 2

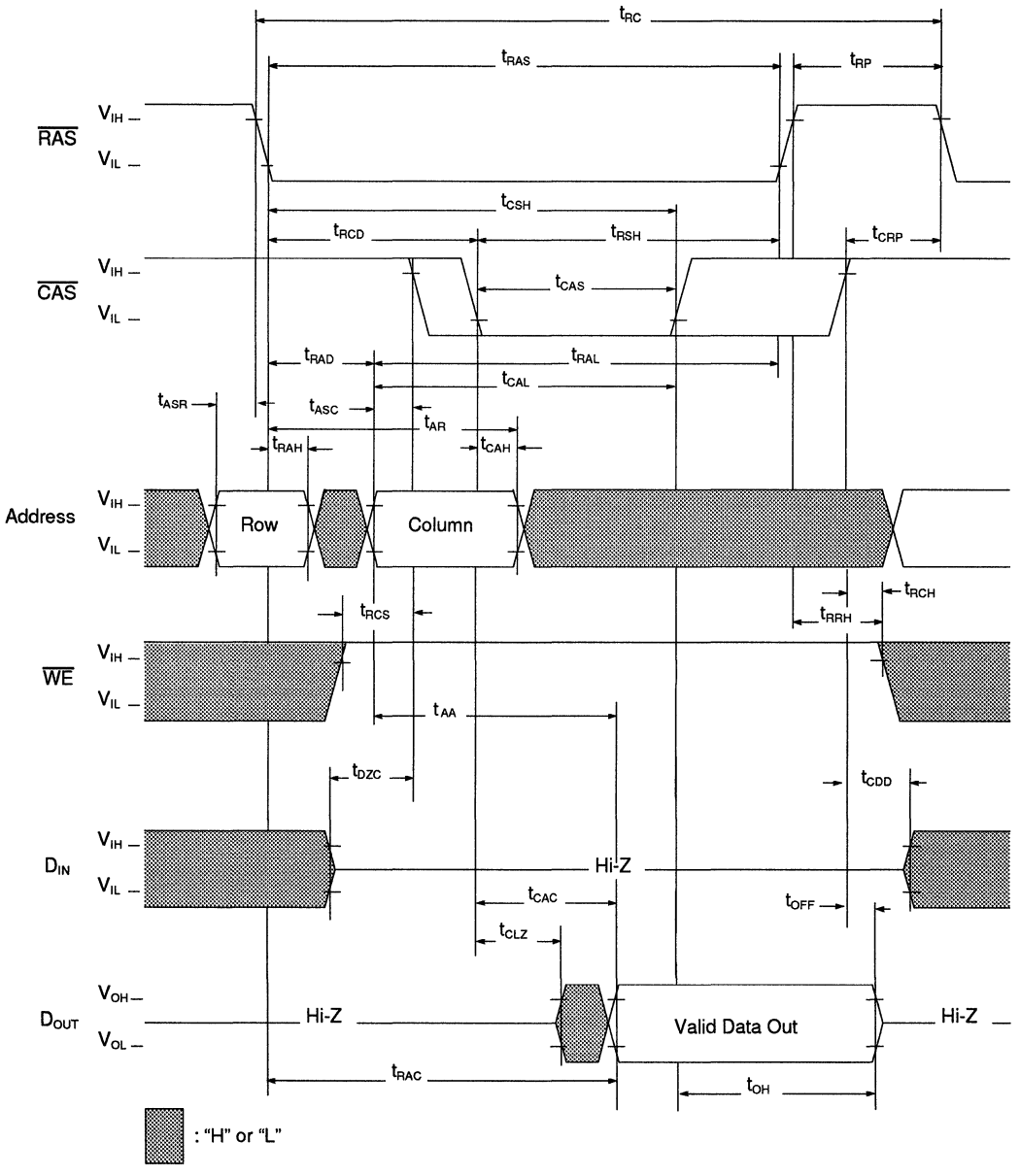
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

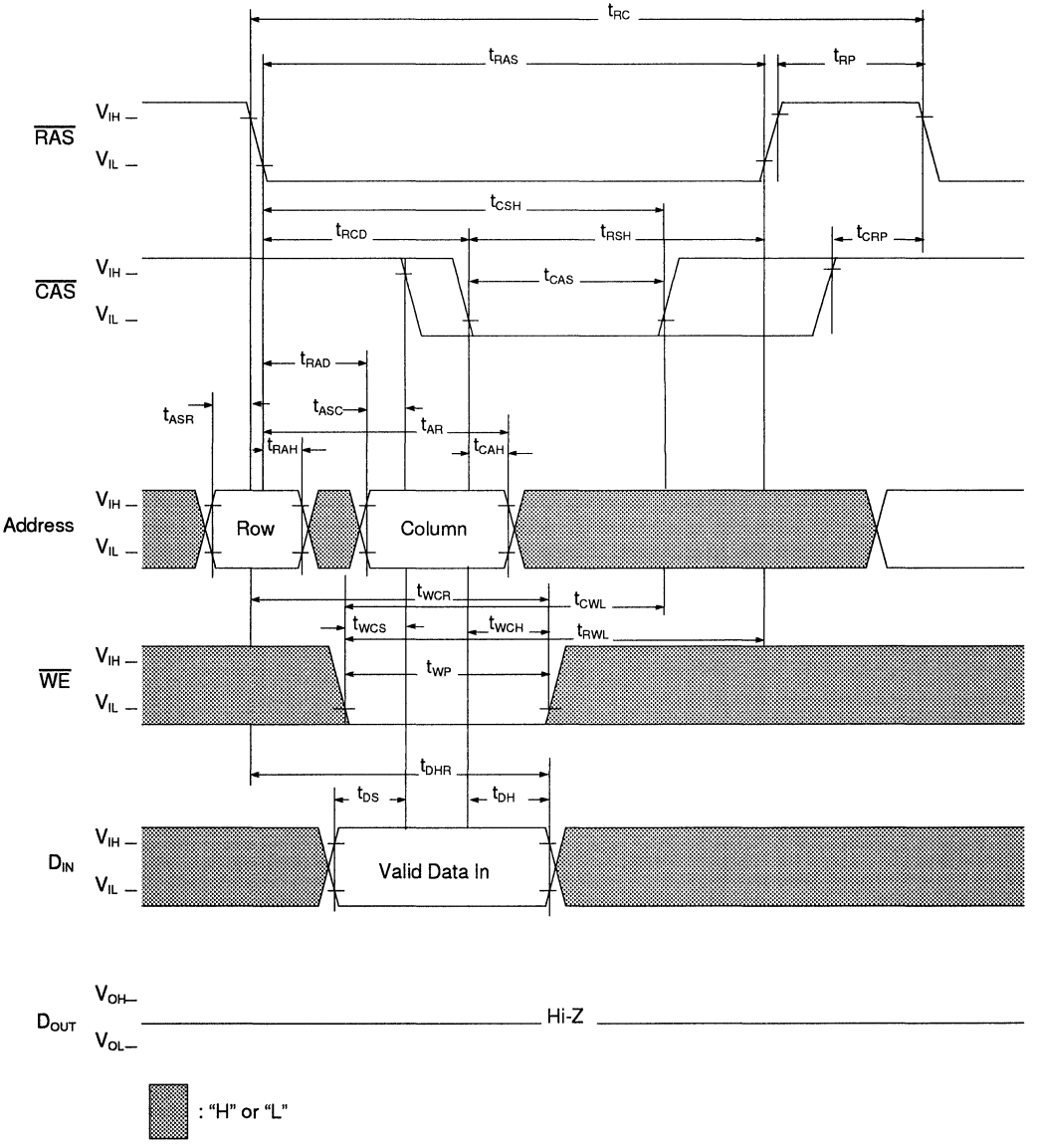
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	9	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	14	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	9	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	9	—	ns	
t_{REF}	Refresh Period	—	256	ns	1

1. 2048 refreshes are required every 256ms.

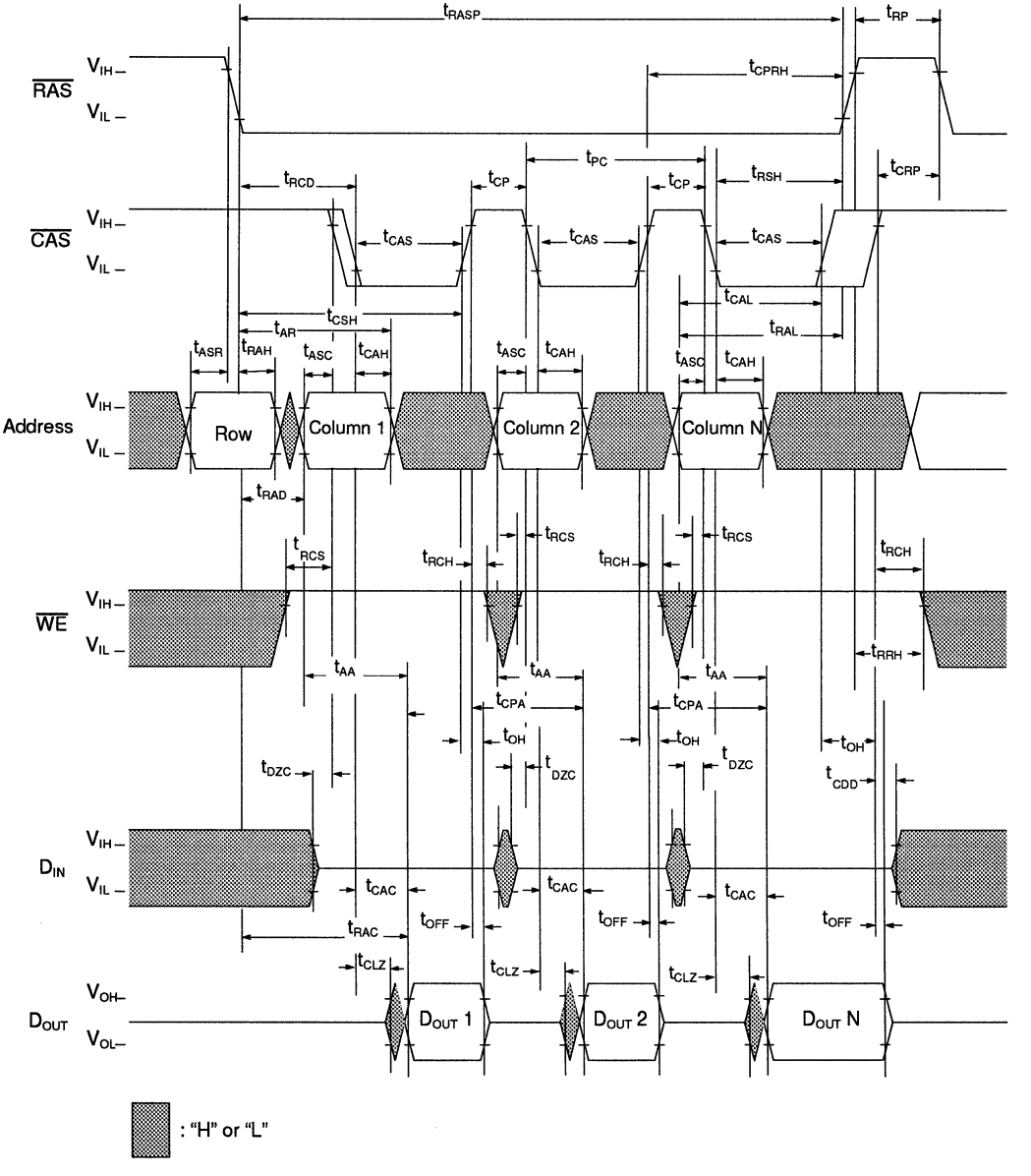
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

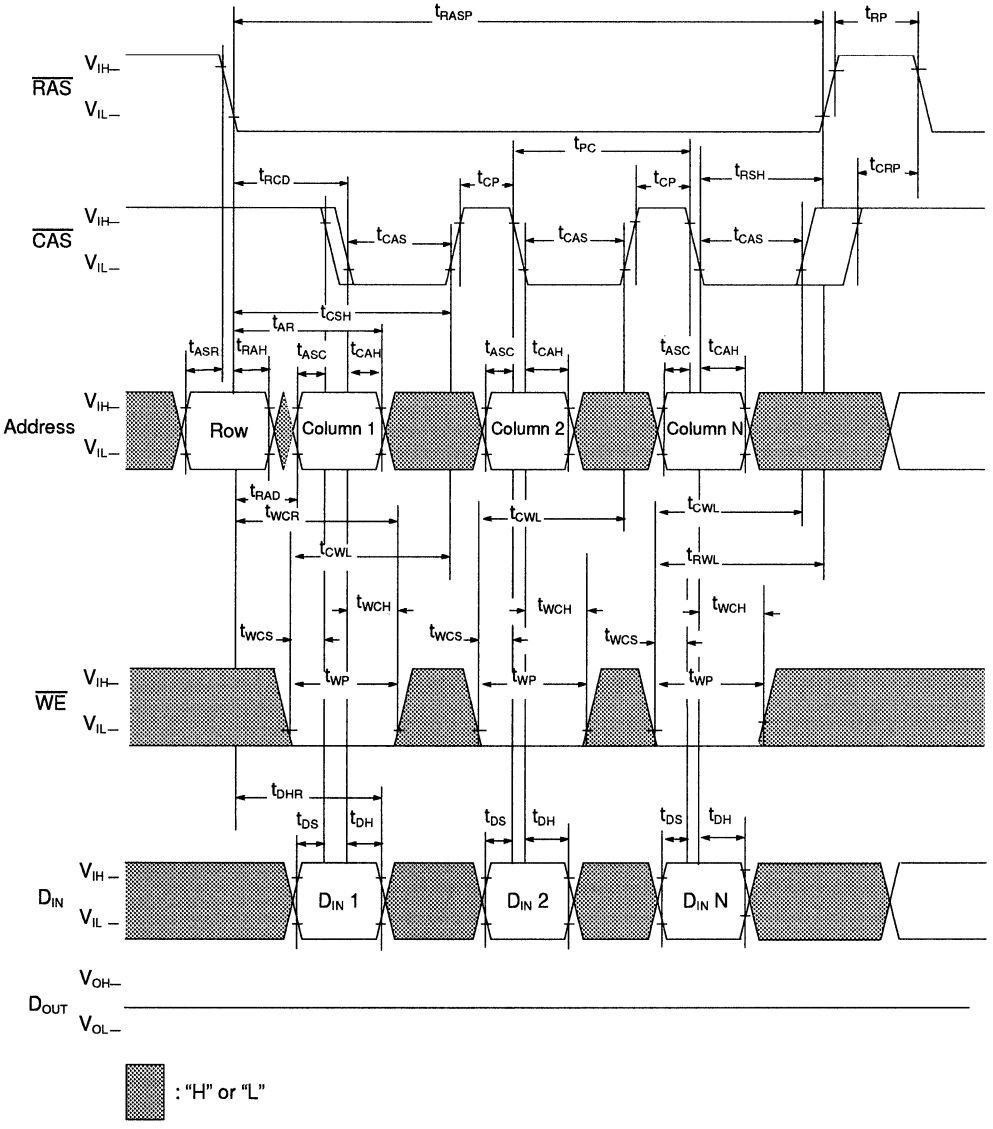
Write Cycle (Early Write)



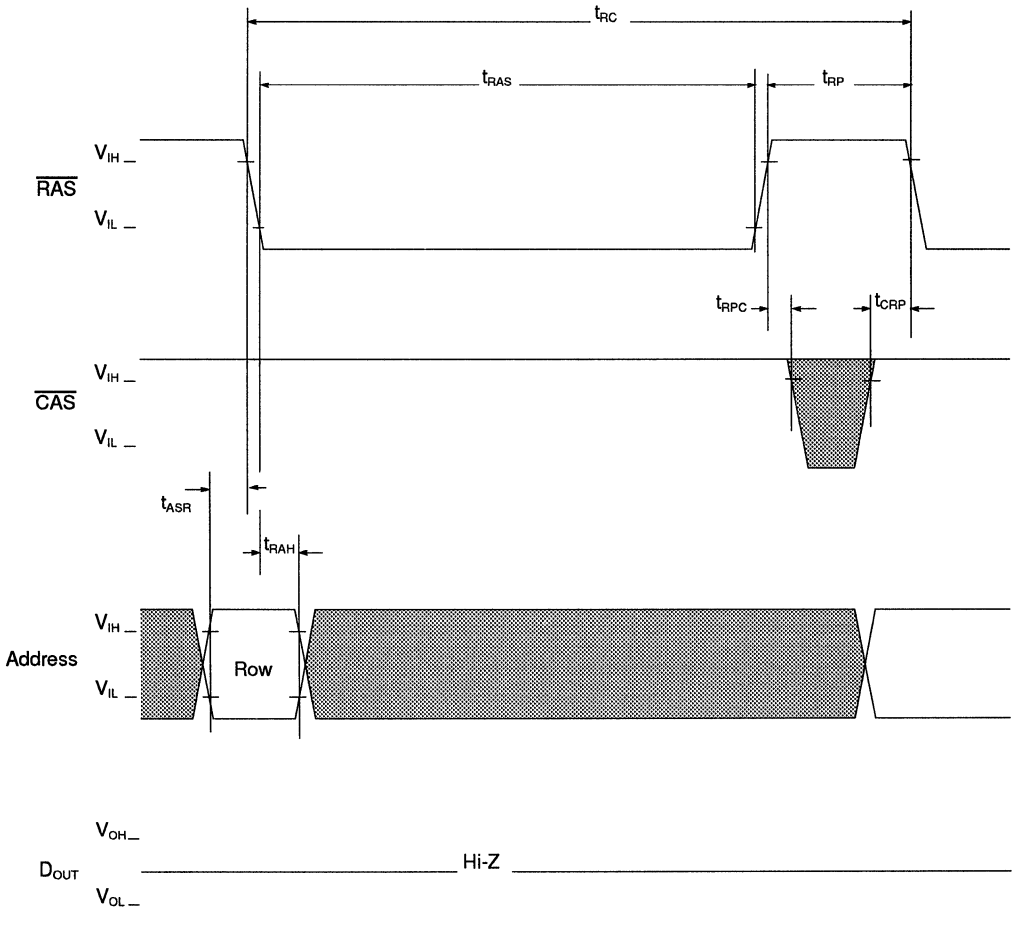
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



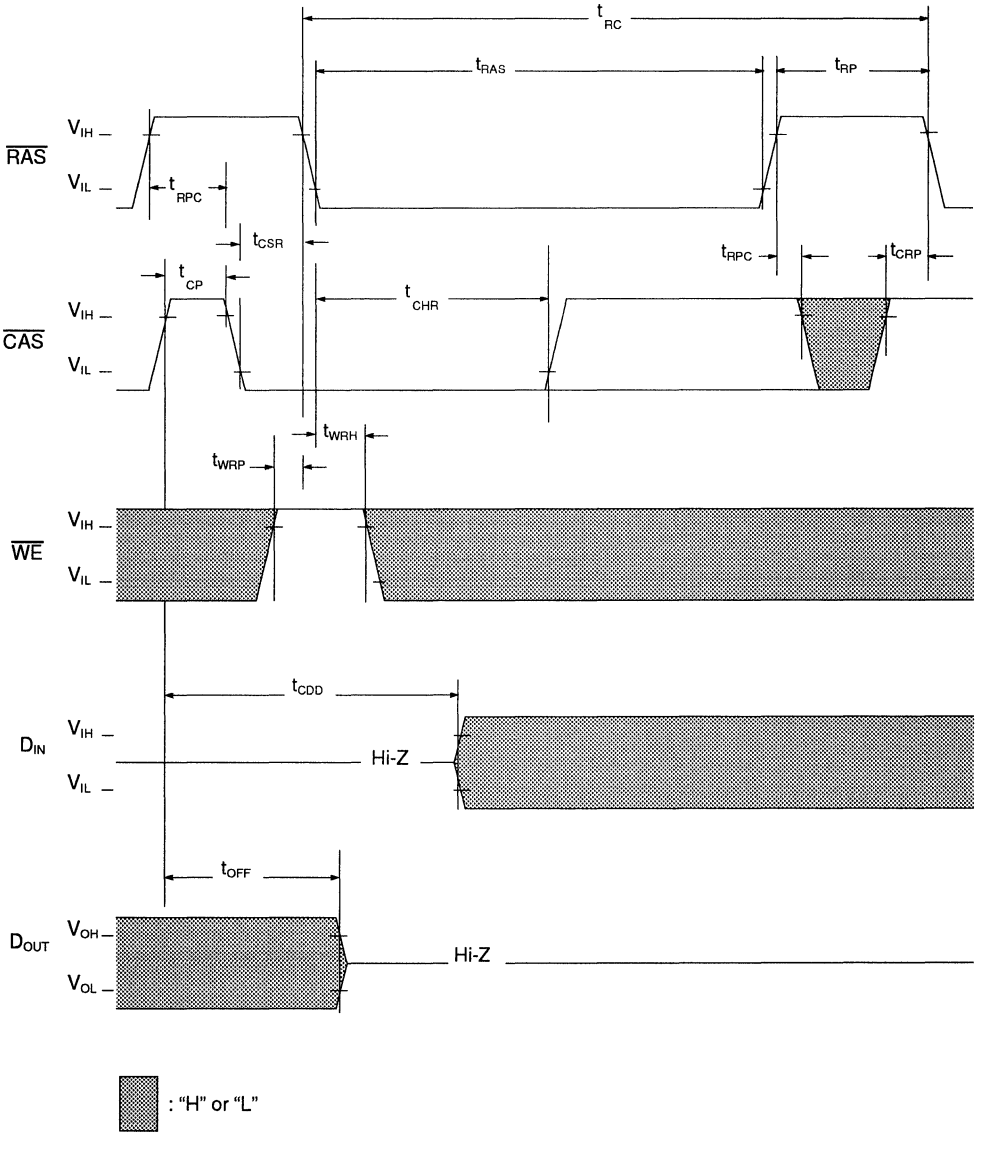
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

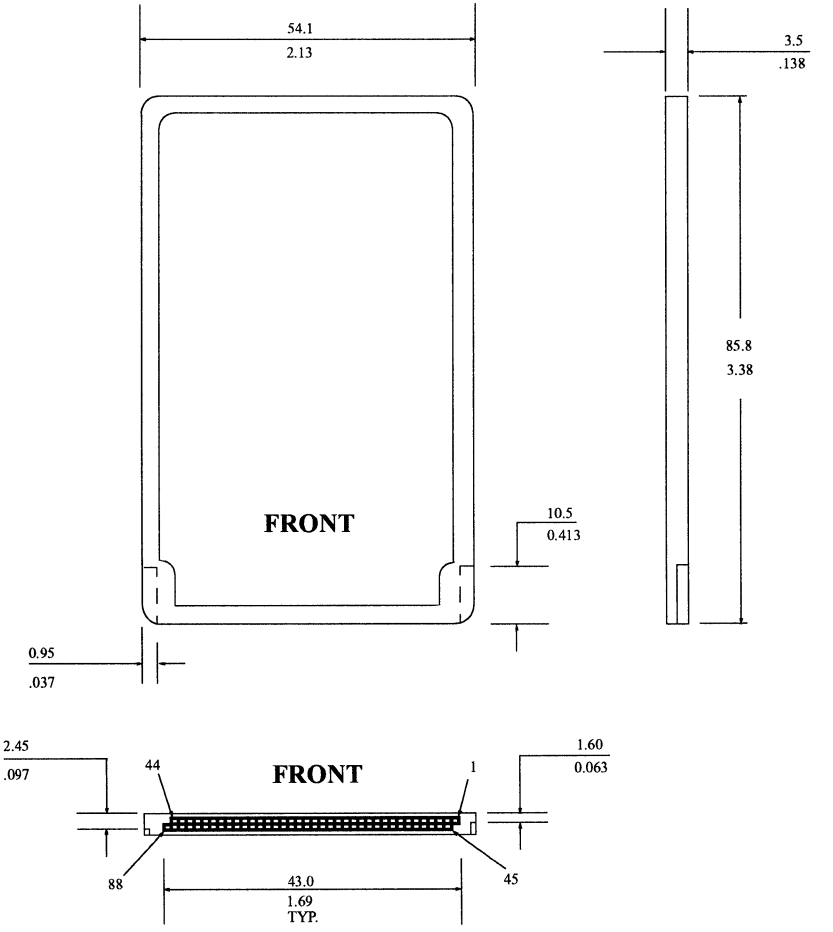
Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

4M x 32 5.0V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

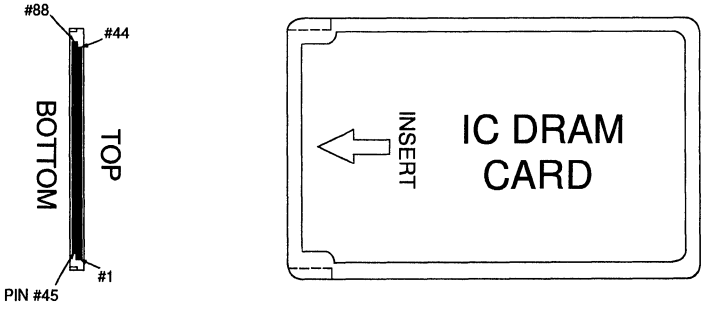
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns
t_{AA}	Access Time From Address	46ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 5.0V, ± 0.25V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- 11/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 2048refresh cycles distributed across 256ms
- Polarized Connector

Description

The IBM11J4320HL is a 16MB industry standard 88-pin IC DRAM card. It is organized as a 4M x 32 high speed memory array. It is built using 8- 2Mx8 devices and is compatible to the JEDEC/PCM-CIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x32 configuration the memory may be utilized as two banks, each having four unique bytes. The x16 configuration may be utilized as four banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other banks in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications.

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

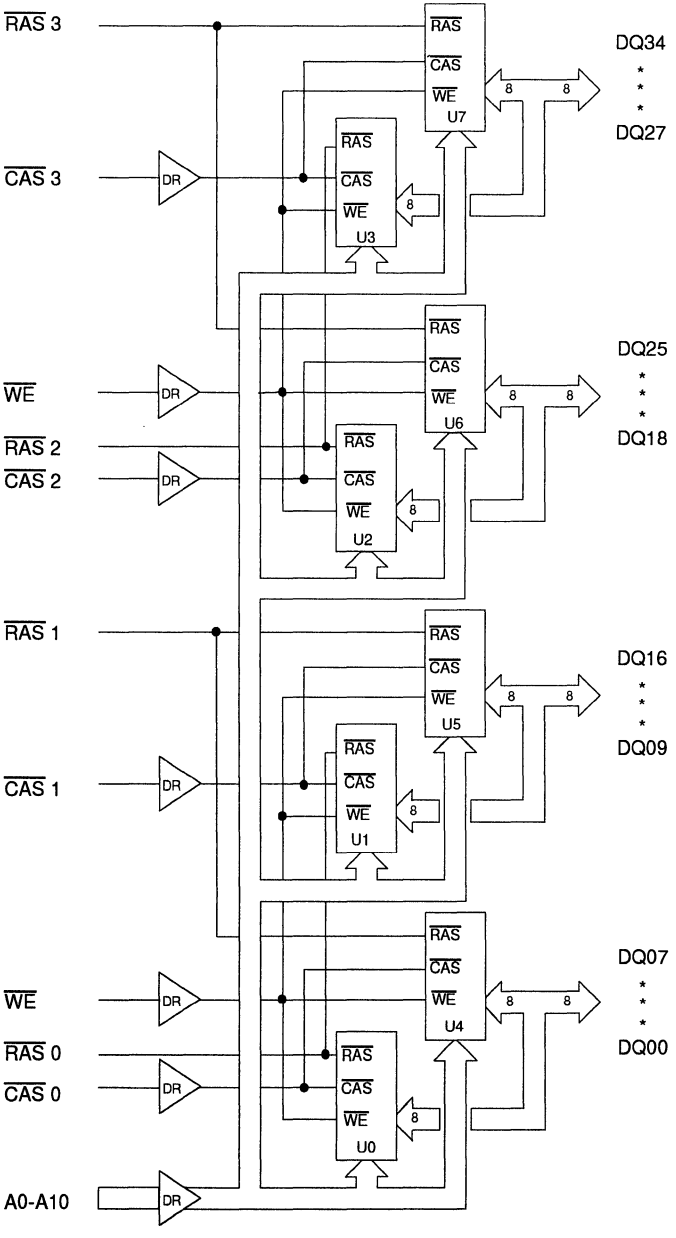
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	NC	47	DQ19	69	$\overline{RAS3}$
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	V_{CC}	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	V_{CC}	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	NC	76	PD8
11	NC	33	NC	55	NC	77	NC
12	NC	34	DQ9	56	V_{SS}	78	NC
13	A0	35	NC	57	A1	79	NC
14	A2	36	DQ10	58	A3	80	DQ27
15	V_{CC}	37	V_{CC}	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	NC	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	A11	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	A10	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	$\overline{RAS1}$	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J4320HLA-70	4M x 32	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type) NC= OPEN, V_{SS} = GND	NC
PD2	NC
PD3	V_{SS}
PD4	V_{SS}
PD5 (Number of Banks/Organization)	V_{SS}
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +7.0	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to V_{CC} + 0.5, 7.0	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	4.2	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.4	—	V_{CC} + 0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	35	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O}$	Output Capacitance (DQ0~DQ34)	30	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	400	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	16	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	400	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	260	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	1.6	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	400	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			2.4	mA	1, 2
$I_{I(L)}$	Input Leakage Current	$\overline{RAS}$	-20	+20	µA	
	Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V))	$\overline{CAS}$,ADD	-10	+10		
	All Other Pins Not Under Test = 0V	$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 10s ($\overline{CAS}$, $\overline{WE}$) or 11ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	11	—	ns	
t_{RAH}	Row Address Hold Time	8	—	ns	
t_{ASC}	Column Address Setup Time	3	—	ns	
t_{CAH}	Column Address Hold Time	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	42	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	30	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 21ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 23ns (7ns before max t_{CAC} of 30ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	16	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	25	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	30	ns	1, 2
t_{AA}	Access Time from Address	—	46	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	46	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	29	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	49	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	54	ns	1, 2

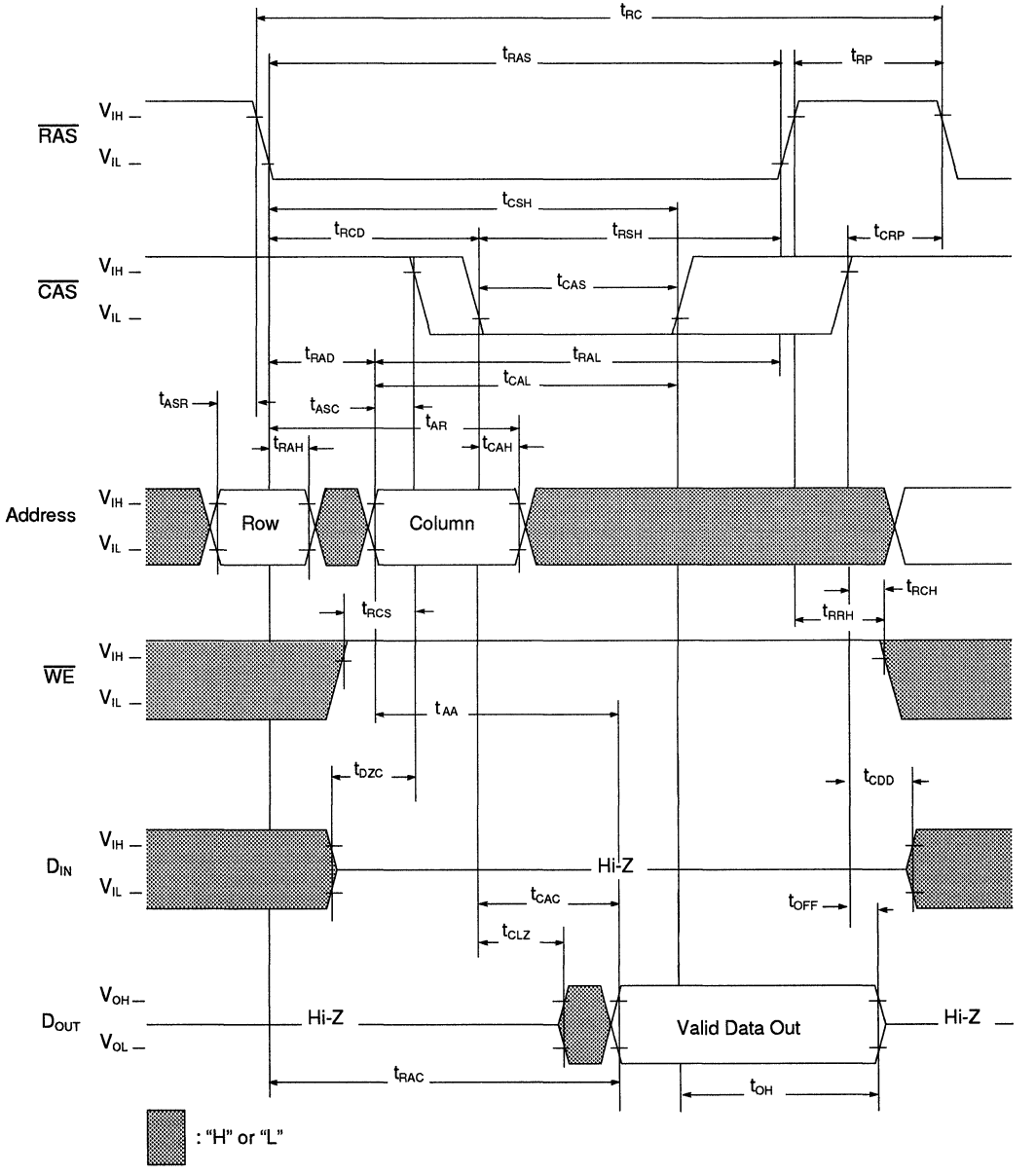
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

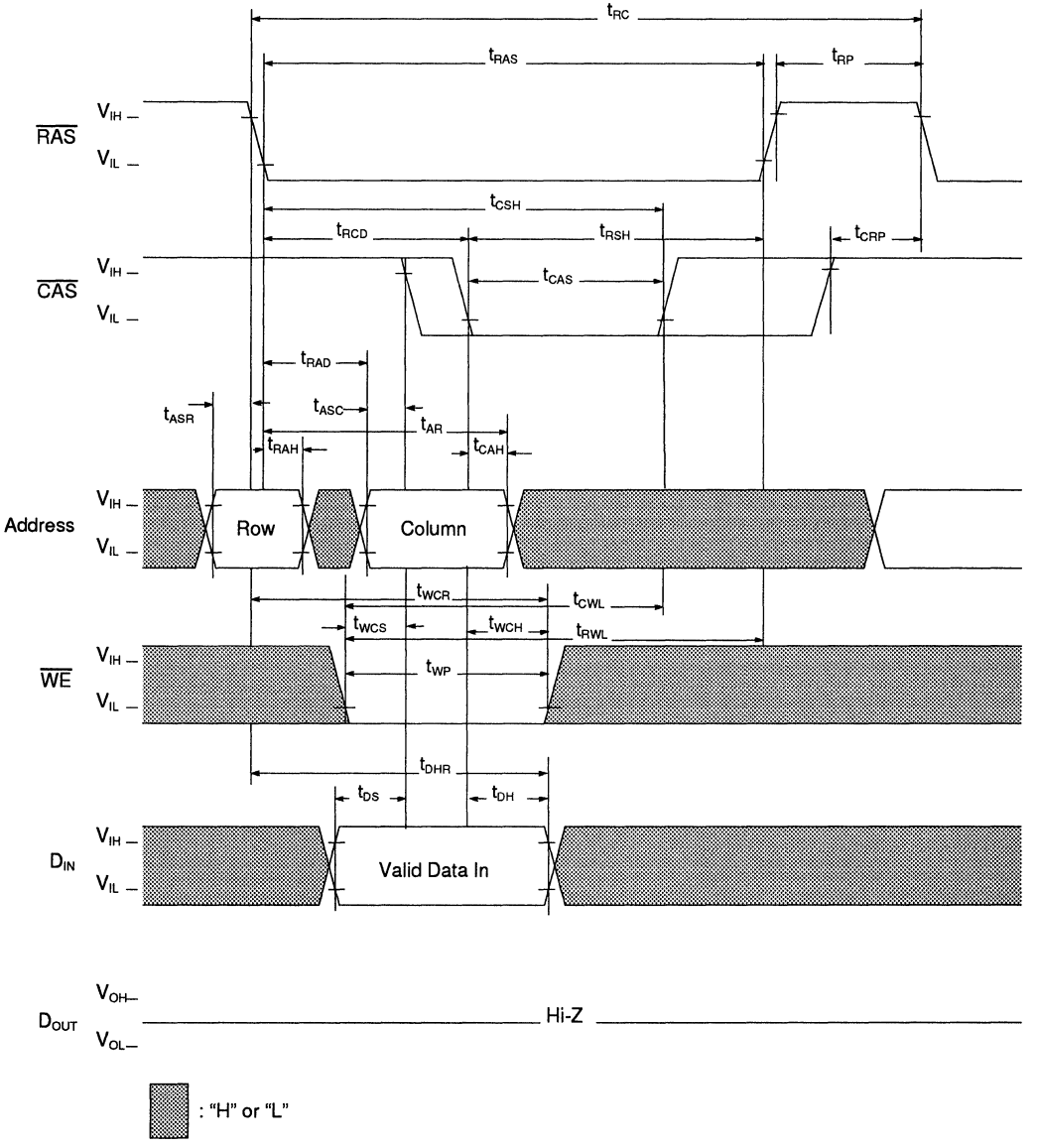
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	19	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	ns	
t_{REF}	Refresh Period	—	256	ms	1

1. 2048 refreshes are required every 256ms.

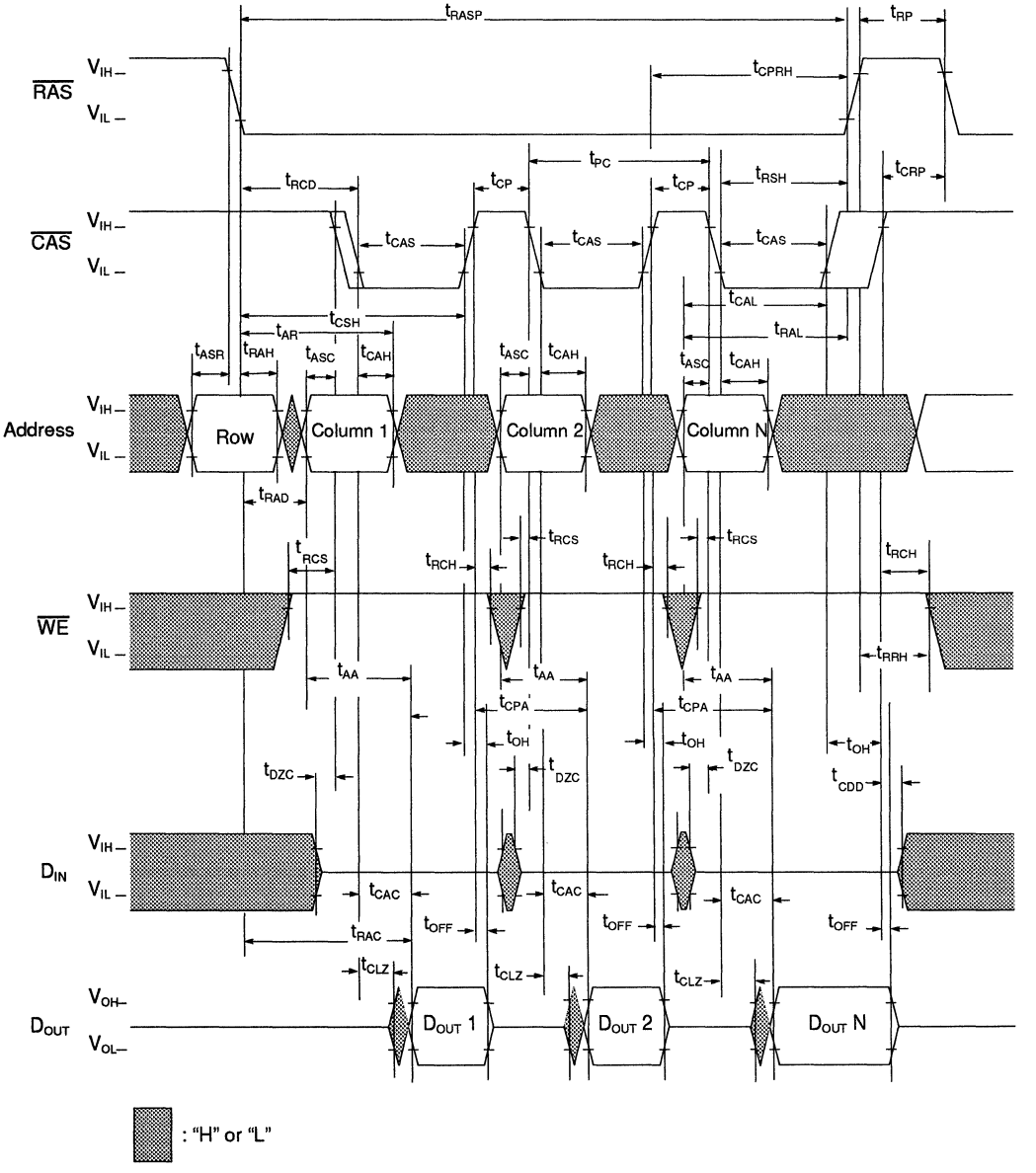
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCH
tRCS
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

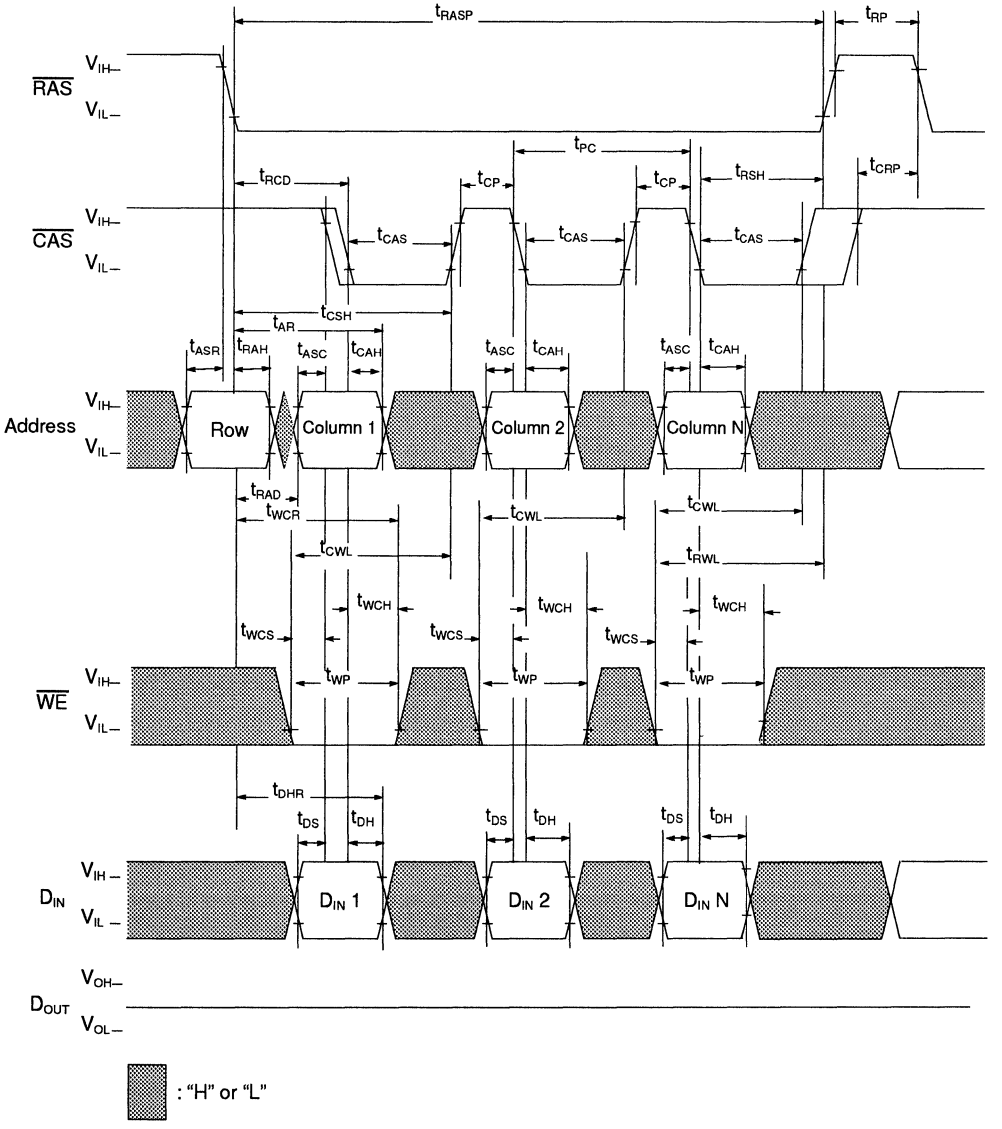
Write Cycle (Early Write)



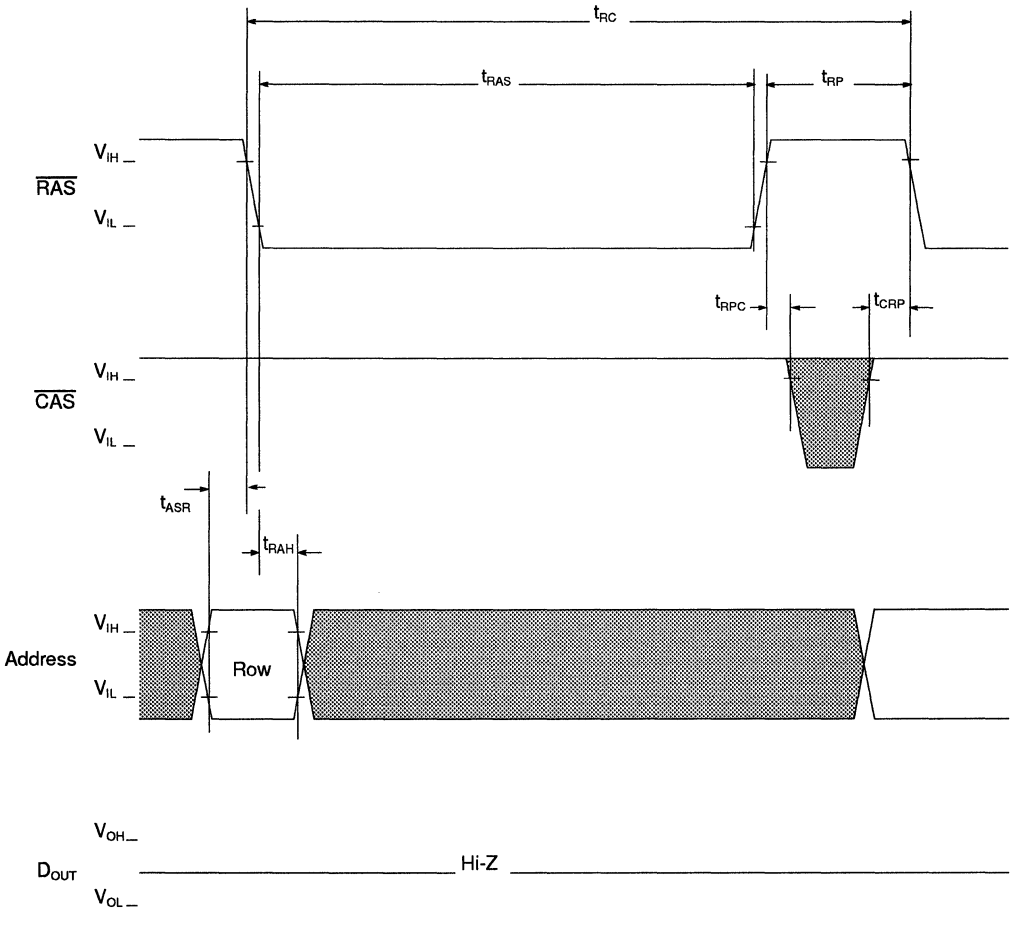
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



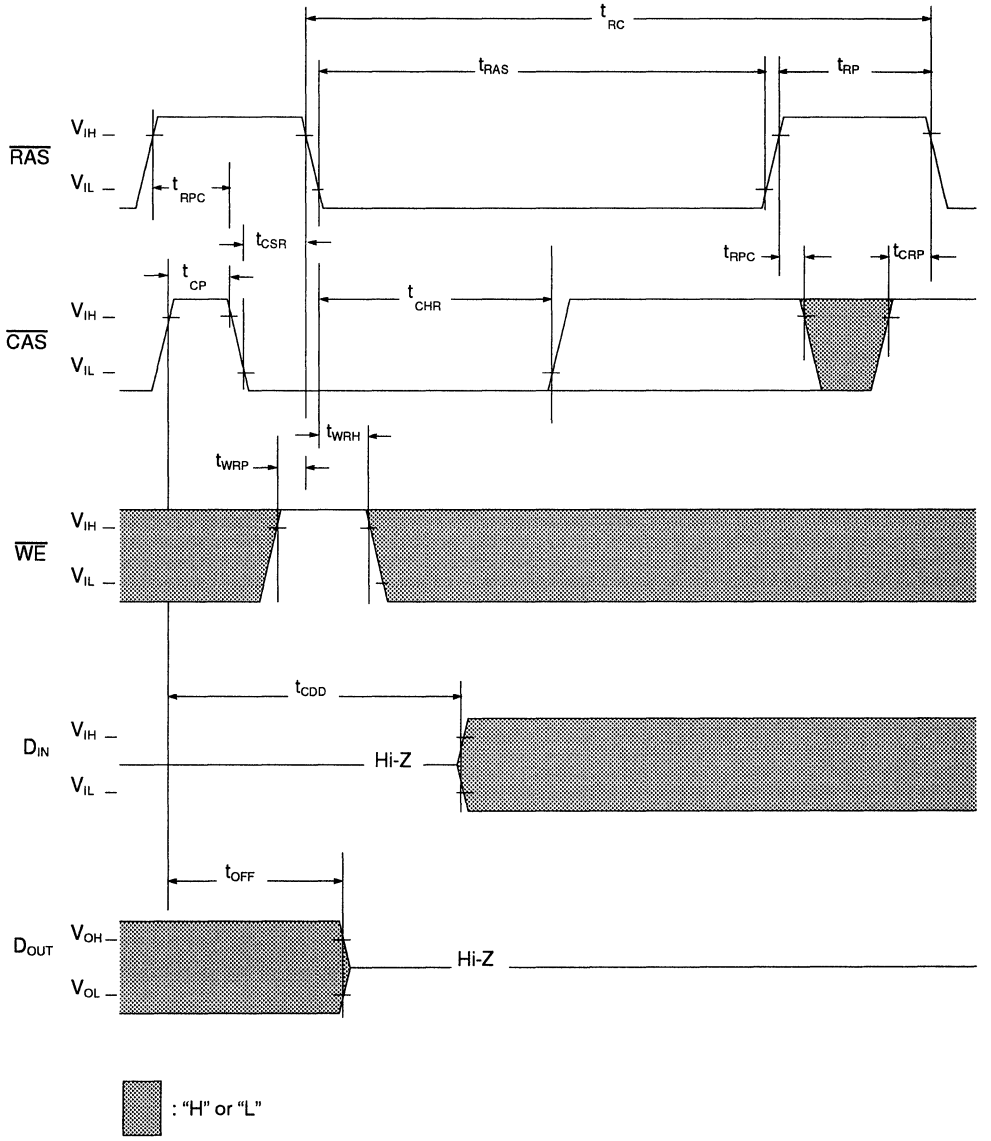
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

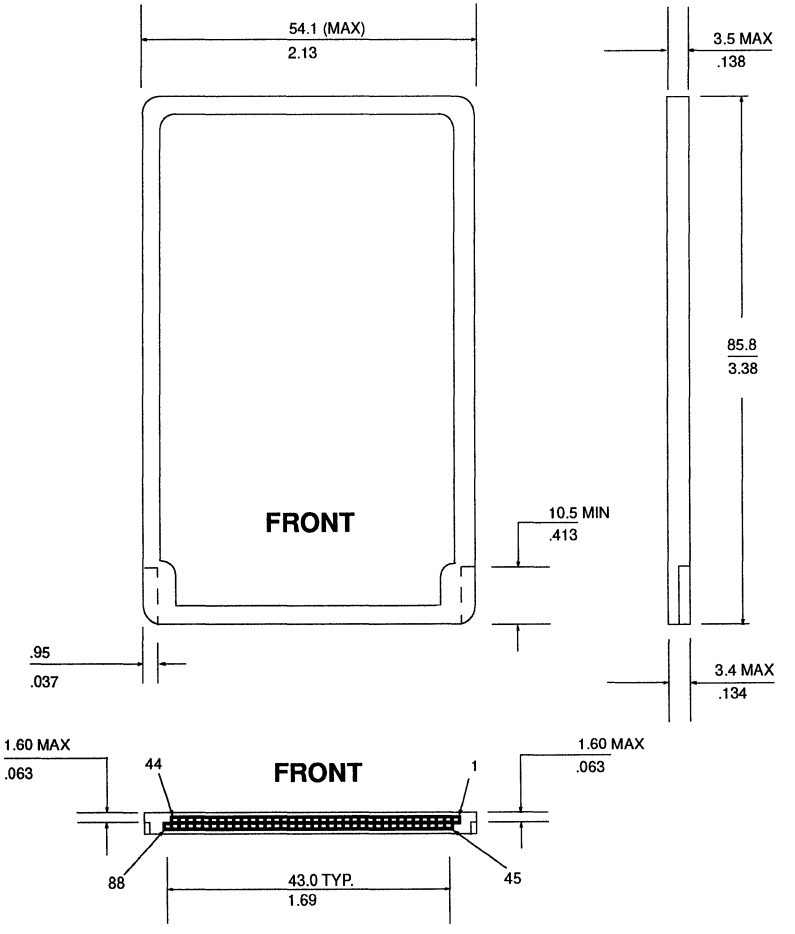
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

4M x 32 3.3V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

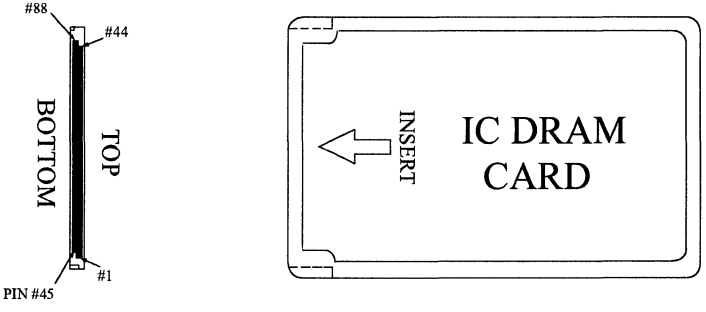
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	24ns
t_{AA}	Access Time From Address	40ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 3.3V, ± 0.3V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- 11/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 2048refresh cycles distributed across 256ms
- Polarized Connector

Description

The IBM11J4320HN is a 16MB industry standard 88-pin IC DRAM card. It is organized as a 4M x 32 high speed memory array. It is built using 8- 2Mx8 devices and is compatible to the JEDEC/PCMCIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x32 configuration the memory may be utilized as two banks, each having four unique bytes. The x16 configuration may be utilized as four banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other banks in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. **Caution must be used to prevent insertion into a 5.0V application.**

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

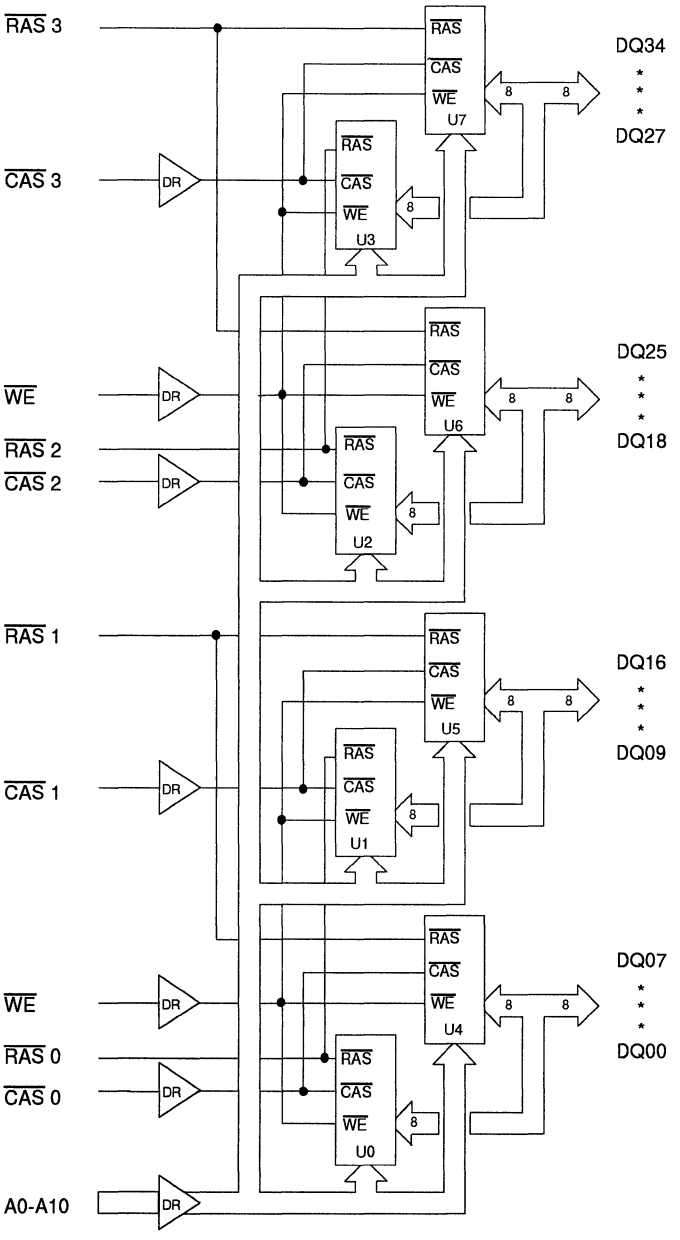
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	V_{CC}	47	DQ19	69	NC
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	NC	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	NC	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	NC	76	PD8
11	V_{CC}	33	NC	55	NC	77	NC
12	NC	34	DQ9	56	V_{SS}	78	NC
13	A0	35	V_{CC}	57	A1	79	NC
14	A2	36	DQ10	58	A3	80	DQ27
15	NC	37	NC	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	V_{CC}	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	NC	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	A10	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	NC	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J4320HNA-70	4M x 32	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type) NC= OPEN, V_{SS} = GND	NC
PD2	NC
PD3	V_{SS}
PD4	V_{SS}
PD5 (Number of Banks/Organization)	V_{SS}
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +4.1	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to +4.1	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to +4.1	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	2.88	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.0	—	V_{CC}+0.3	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.3	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 3.3± 0.3V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	35	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O}$	Output Capacitance (DQ0~DQ34)	30	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 3.3± 0.3V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	400	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	16	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	400	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	260	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	1.6	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	400	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			2.4	mA	1, 2
$I_{I(L)}$	Input Leakage Current	$\overline{RAS}$	-20	+20	µA	
	Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V))	$\overline{CAS}$,ADD	-10	+10		
	All Other Pins Not Under Test = 0V	$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 3.3 ± 0.3V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 1ns minimum, 4ns ($\overline{CAS}$, $\overline{WE}$) or 5ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	11	—	ns	
t_{RAH}	Row Address Hold Time	8	—	ns	
t_{ASC}	Column Address Setup Time	3	—	ns	
t_{CAH}	Column Address Hold Time	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	42	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	24	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	30	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 21ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 23ns (7ns before max t_{CAC} of 30ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	25	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	24	ns	1, 2
t_{AA}	Access Time from Address	—	40	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	1	—	ns	
t_{OH}	Output Data Hold Time	1	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	24	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	1	24	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	44	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	44	ns	1, 2

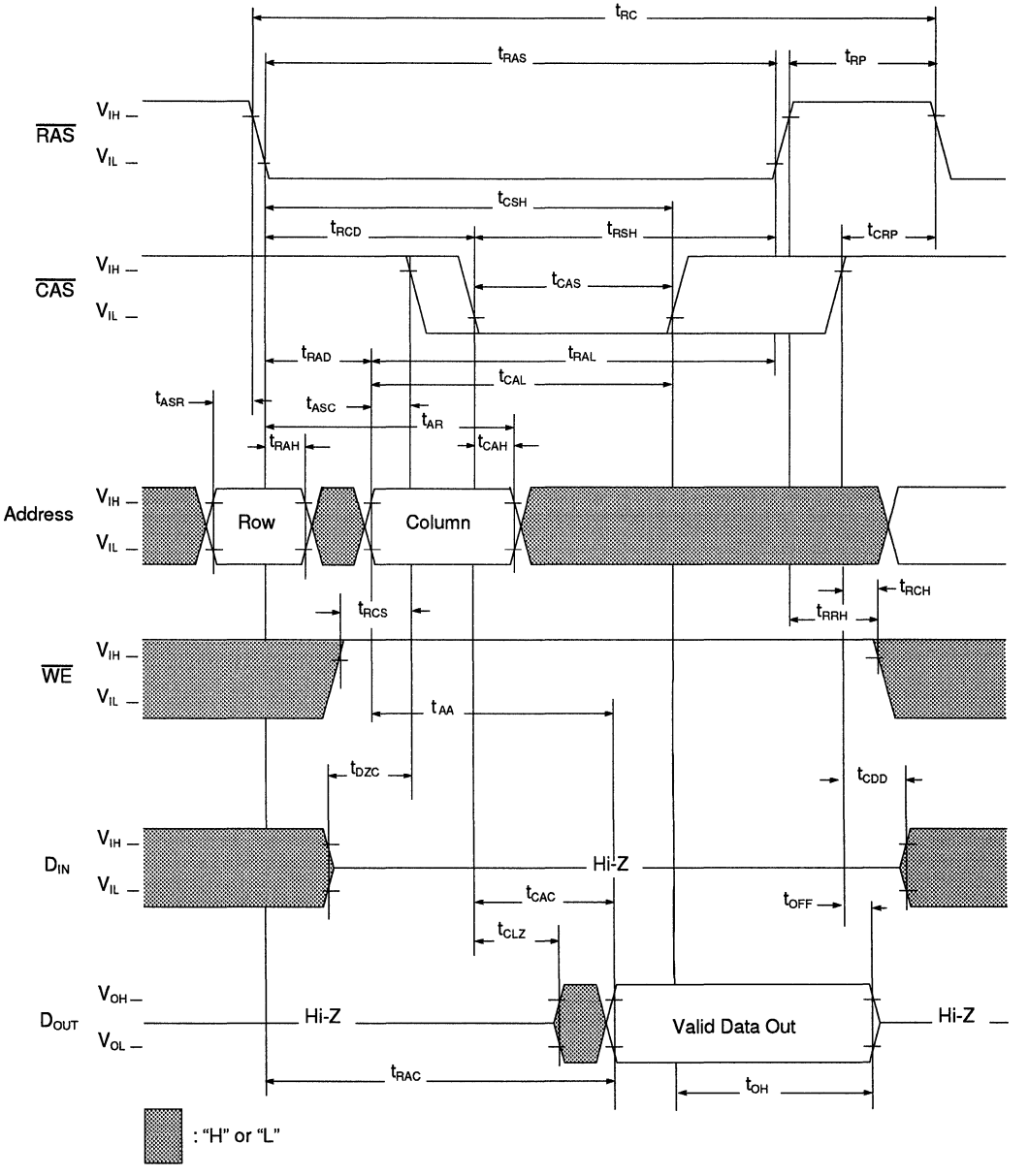
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

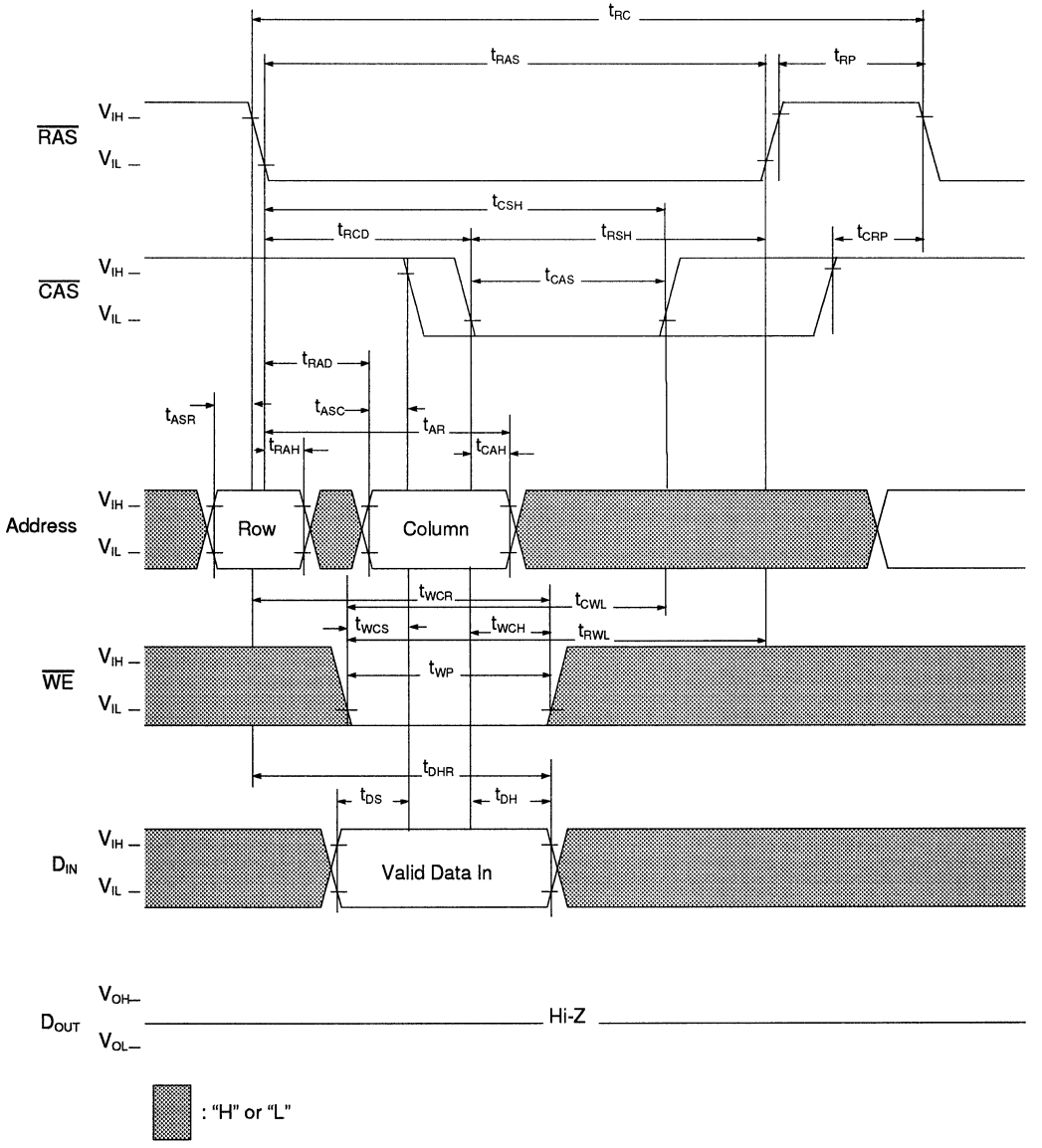
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	9	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	14	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	9	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	9	—	ns	
t_{REF}	Refresh Period	—	256	ms	1

1. 2048 refreshes are required every 256ms.

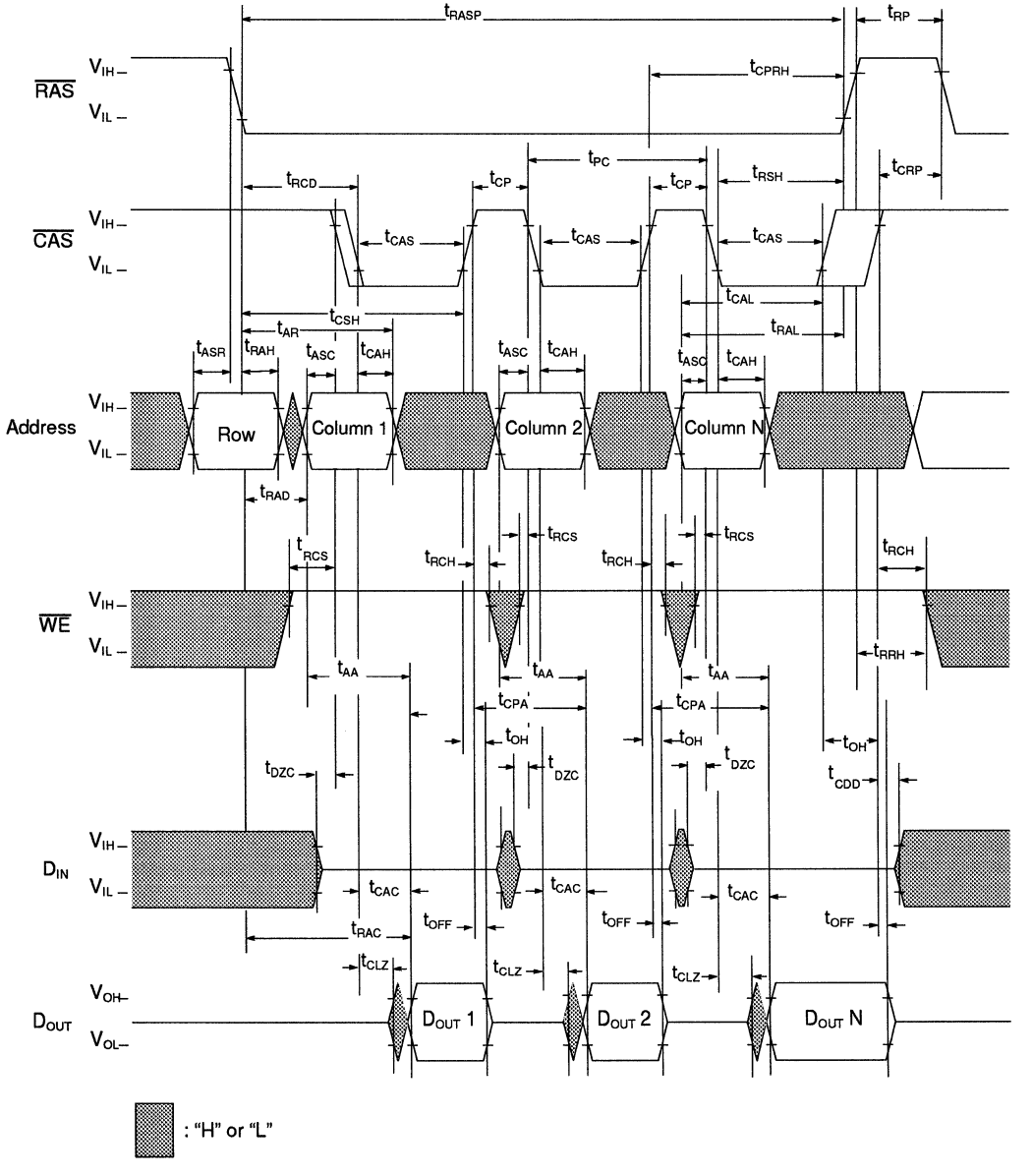
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

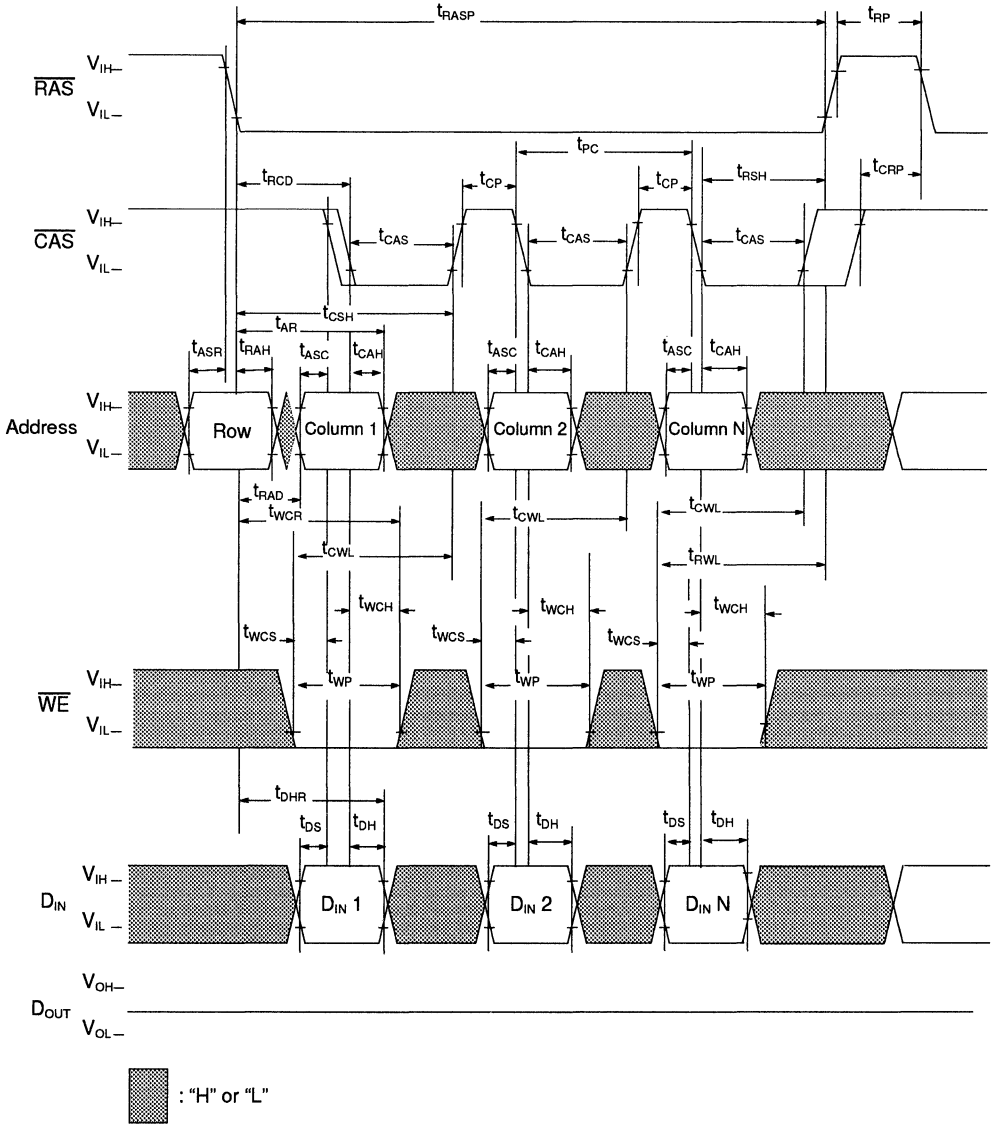
Write Cycle (Early Write)



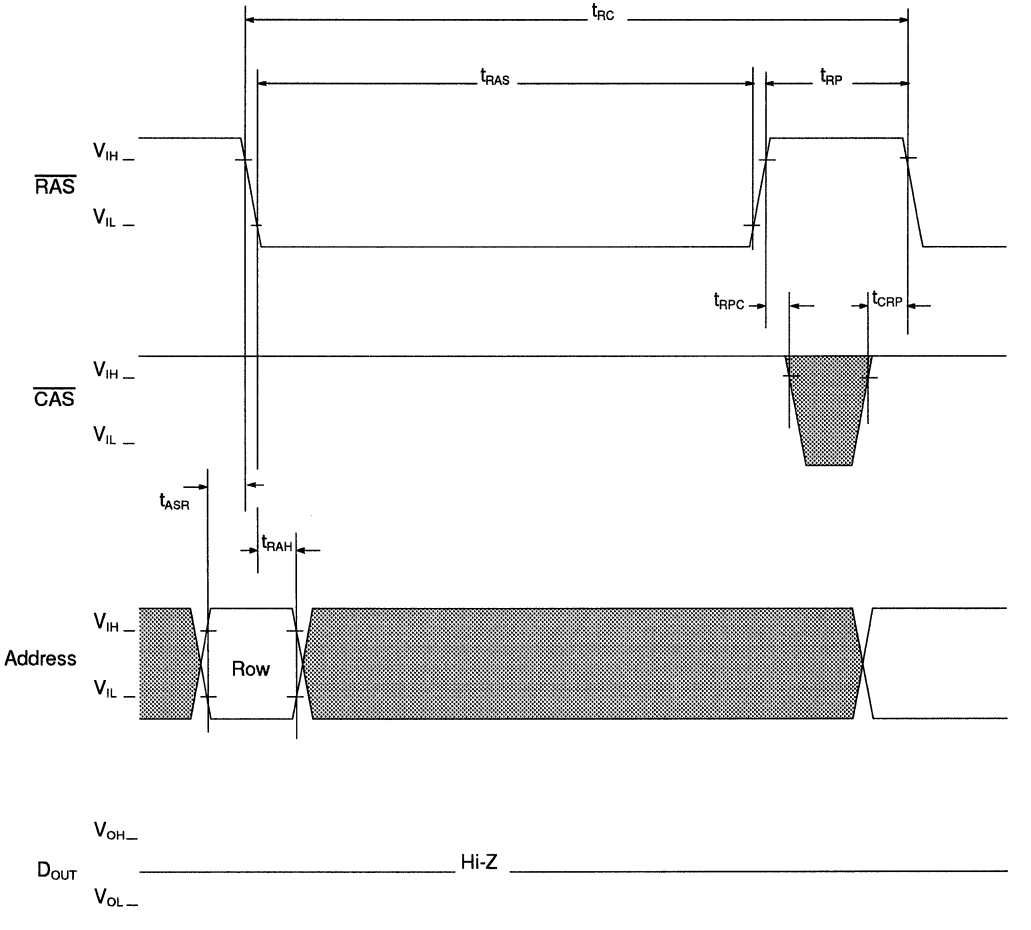
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

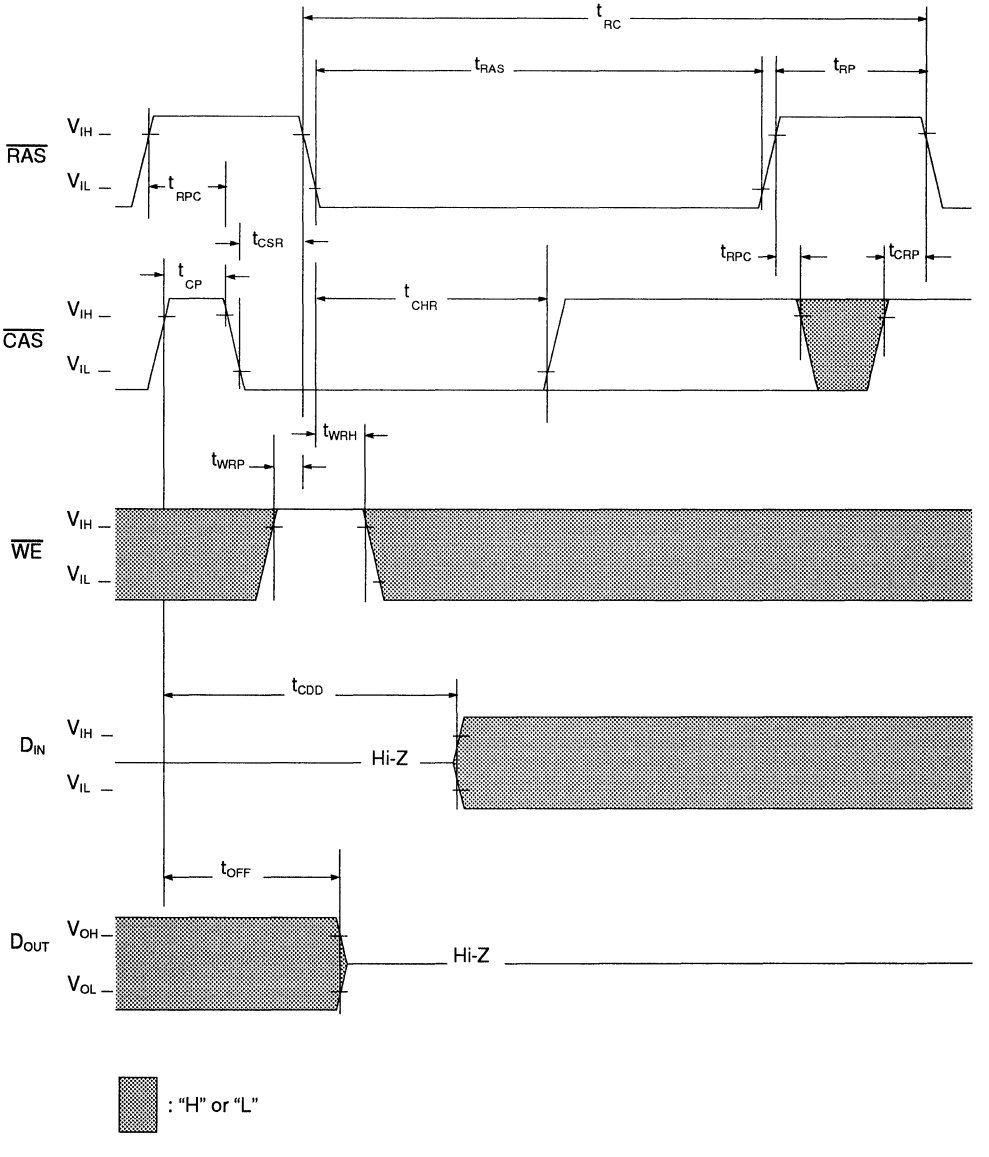


$\overline{RAS}$ Only Refresh Cycle



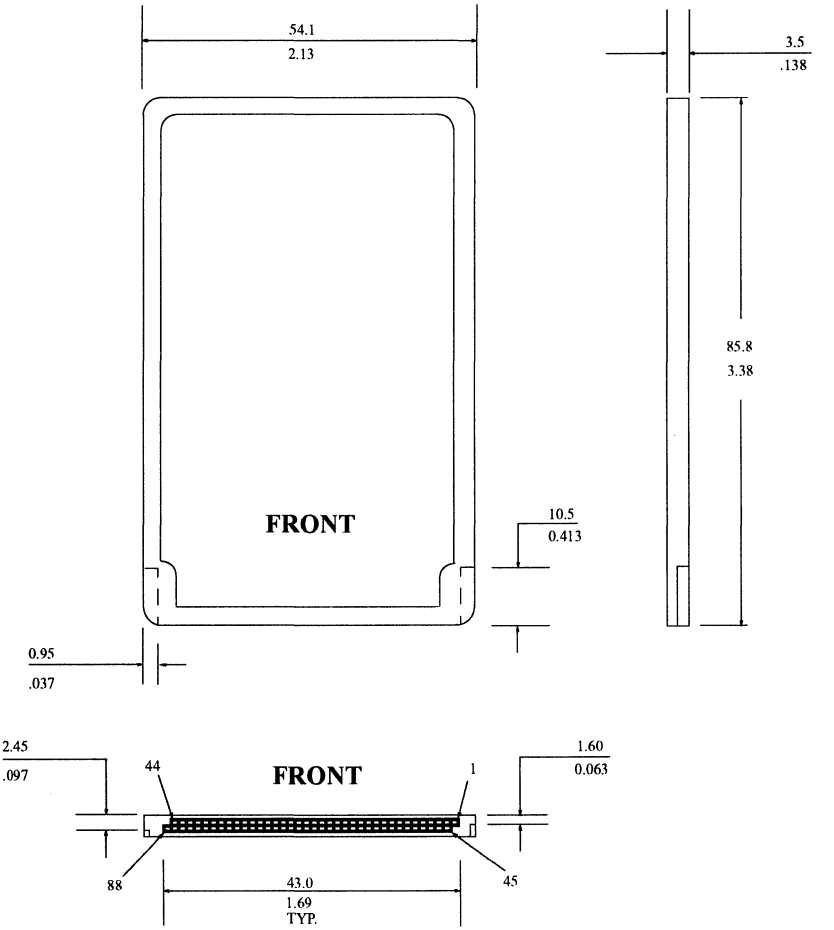
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Preliminary

4M x 32 5.0V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
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- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 5.0V, ± 0.25V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- 11/11 Addressing (Row/Column)
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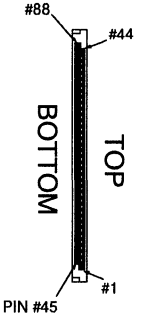
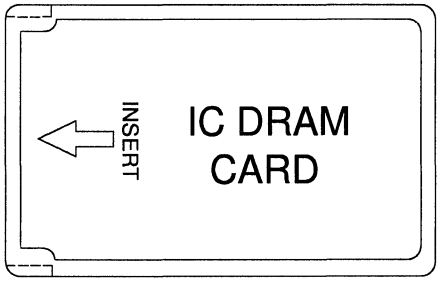
- 2048 refresh cycles distributed across 256ms
- Polarized Connector

Description

The IBM11J4320BL is a 16MB industry standard 88-pin IC DRAM card. It is organized as a 4M x 32 high speed memory array. It is built using 8- 4Mx4 devices and is compatible to the JEDEC/PCMCIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x32 configuration the memory is a single bank, having four unique bytes. The x16 configuration may be utilized as two banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other bank in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. The related 4M x 36 version of this ICDRAM card is IBM11J4360BLA

Card Outline





Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

Pinout

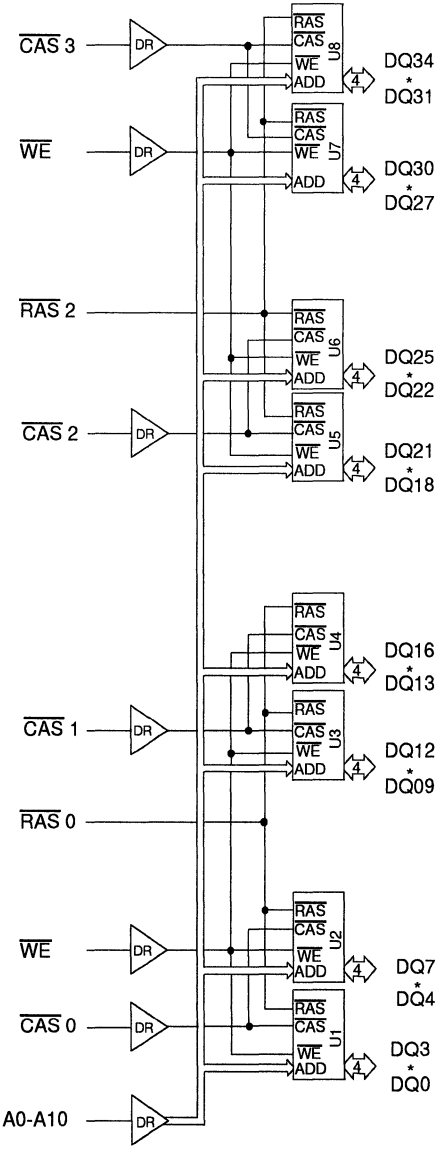
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	NC	47	DQ19	69	$\overline{NC}$
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	V_{CC}	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	V_{CC}	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	NC	76	PD8
11	NC	33	NC	55	NC	77	NC
12	NC	34	DQ9	56	V_{SS}	78	NC
13	A0	35	NC	57	A1	79	NC
14	A2	36	DQ10	58	A3	80	DQ27
15	V_{CC}	37	V_{CC}	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	NC	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	NC	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	A10	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	$\overline{NC}$	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

1. DQ numbering is compatible with parity (x36) version)

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J4320BLA-70	4M x 32	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	V_{SS}
PD3	NC
PD4	V_{SS}
PD5 (Number of Banks/Organization)	NC
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +7.0	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to V_{CC} + 0.5, 7.0	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	6.3	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.4	—	V_{CC} + 0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	43	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O}$	Output Capacitance (DQ0~DQ34)	25	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	880	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	16	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	880	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	520	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	1.6	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	800	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			2.4	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$) or 6ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	7	—	ns	
t_{RAH}	Row Address Hold Time	8	—	ns	
t_{ASC}	Column Address Setup Time	2	—	ns	
t_{CAH}	Column Address Hold Time	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	28	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 21ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 23ns (6ns before max t_{CAC} of 29ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	16	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	20	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	42	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	42	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	25	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	50	ns	1, 2

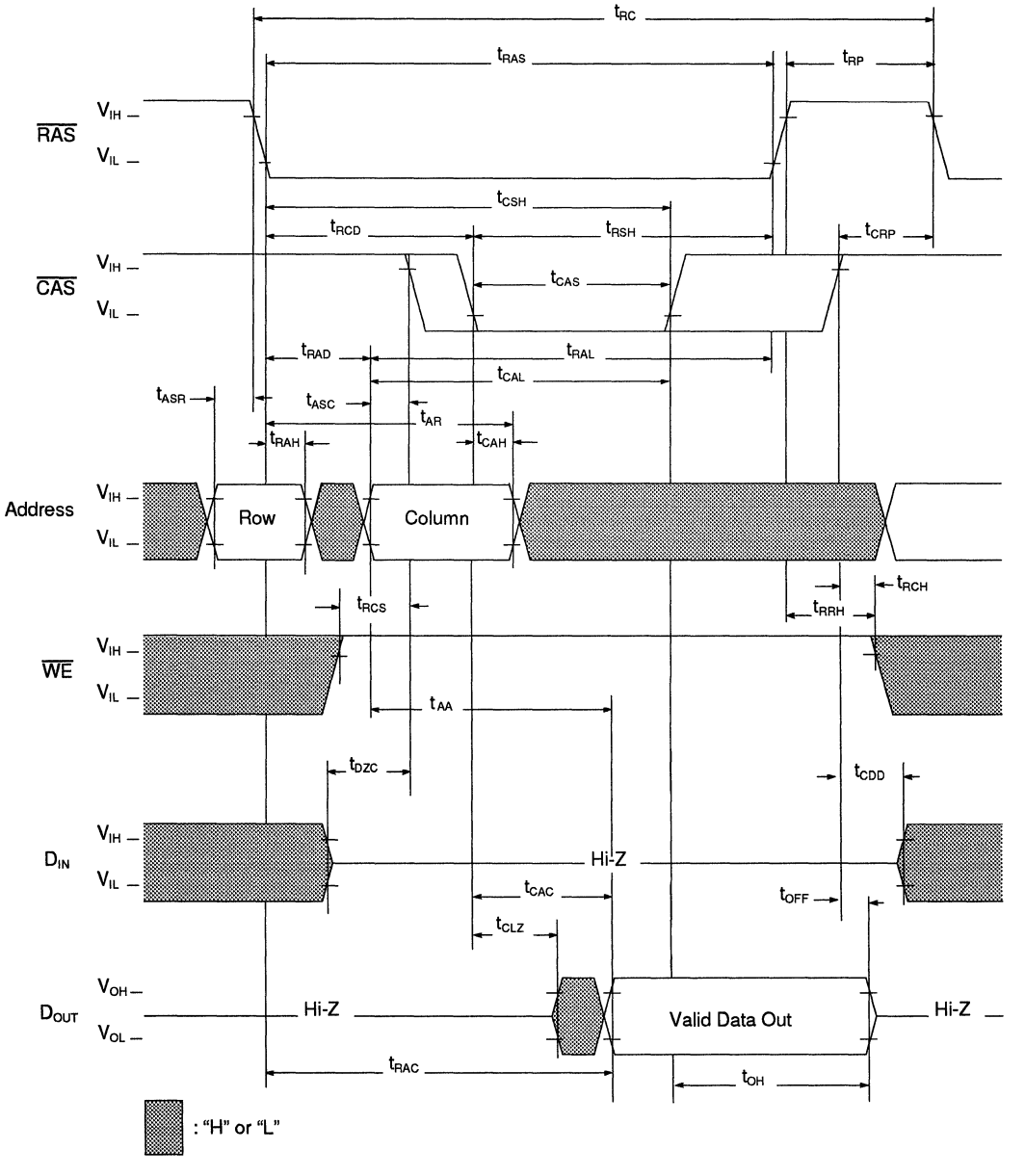
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

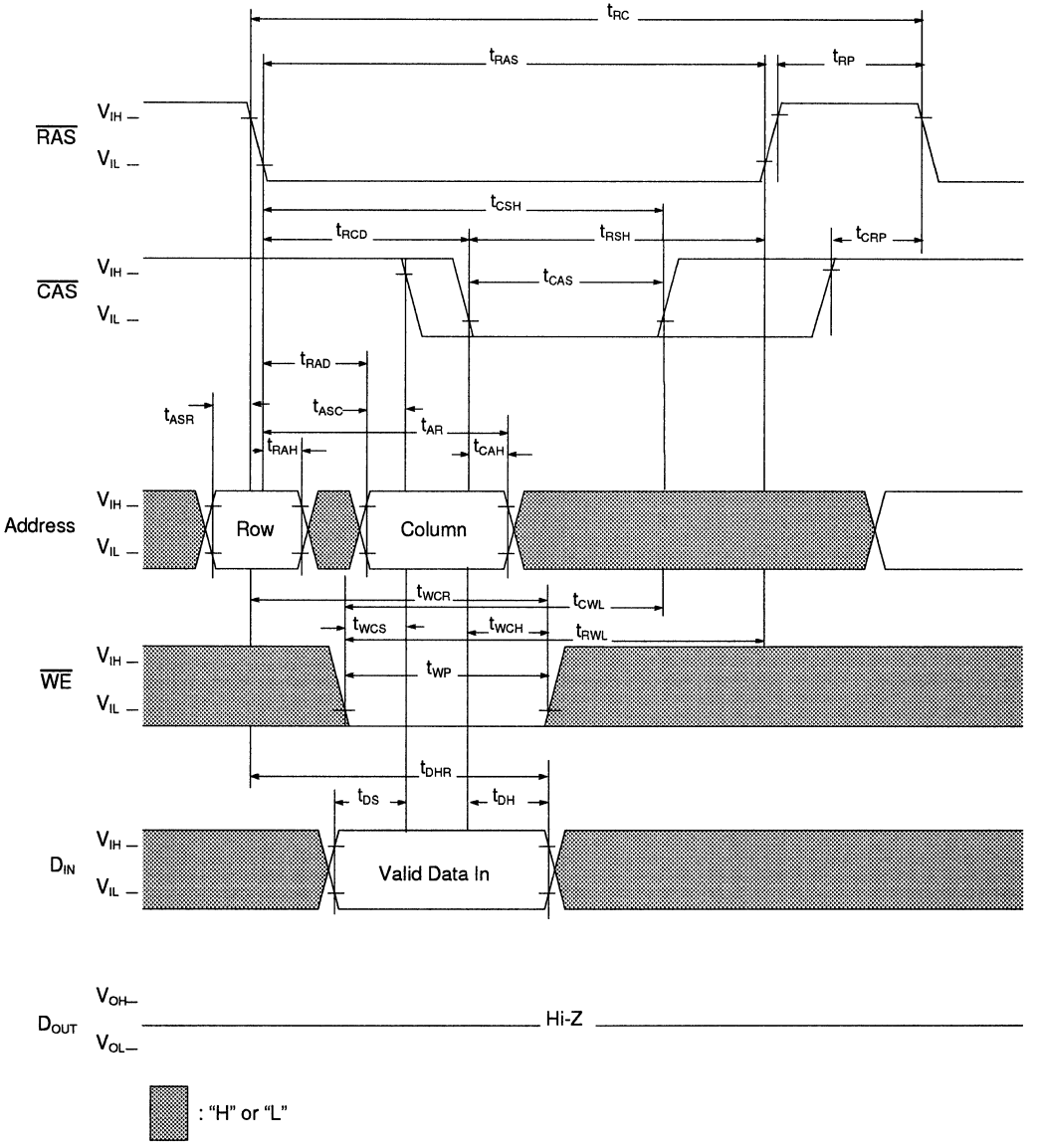
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	16	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	8	—	ns	
t_{REF}	Refresh Period	—	256	ns	1

1. 2048 refreshes are required every 256ms.

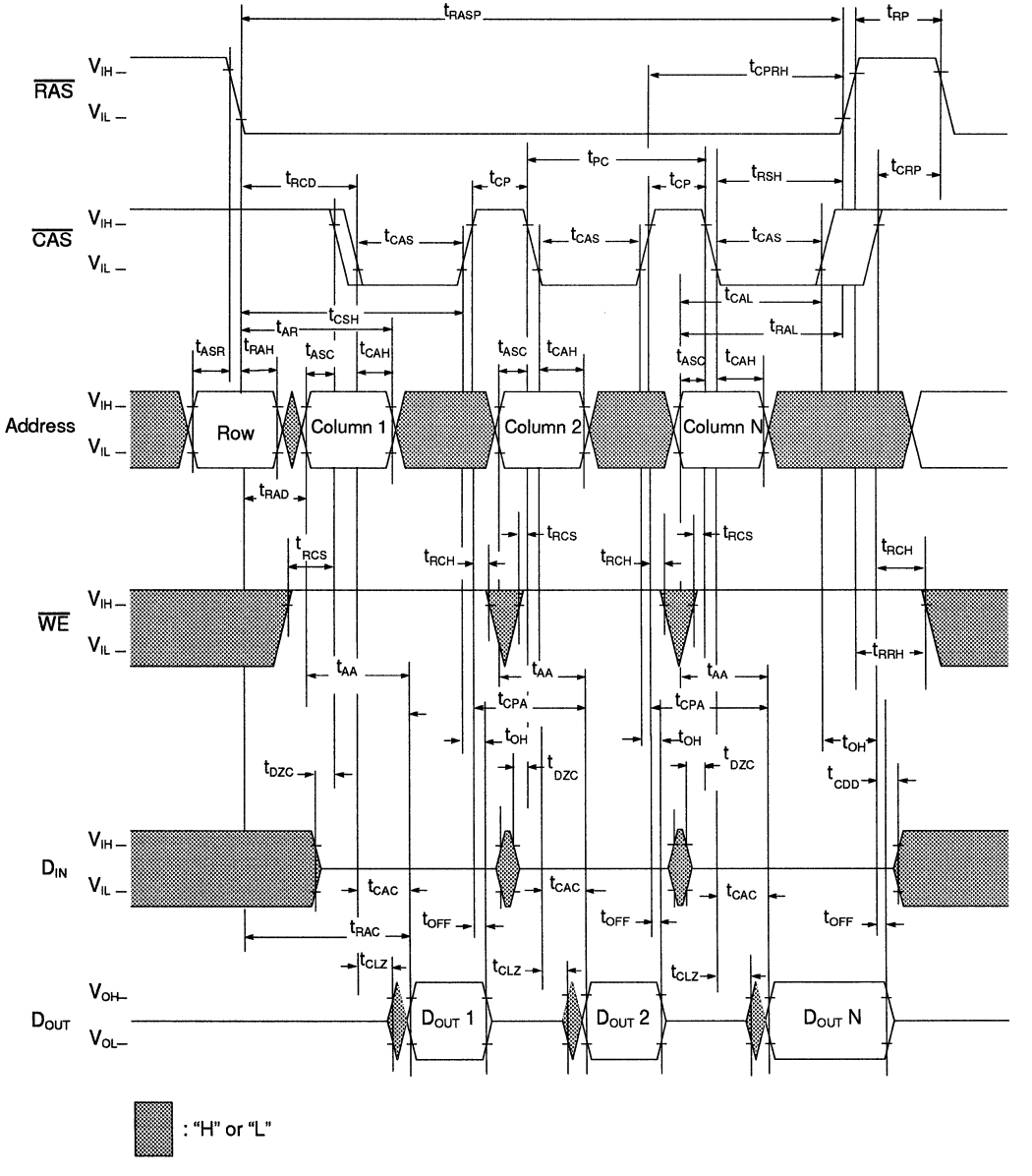
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRRH
tRCH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

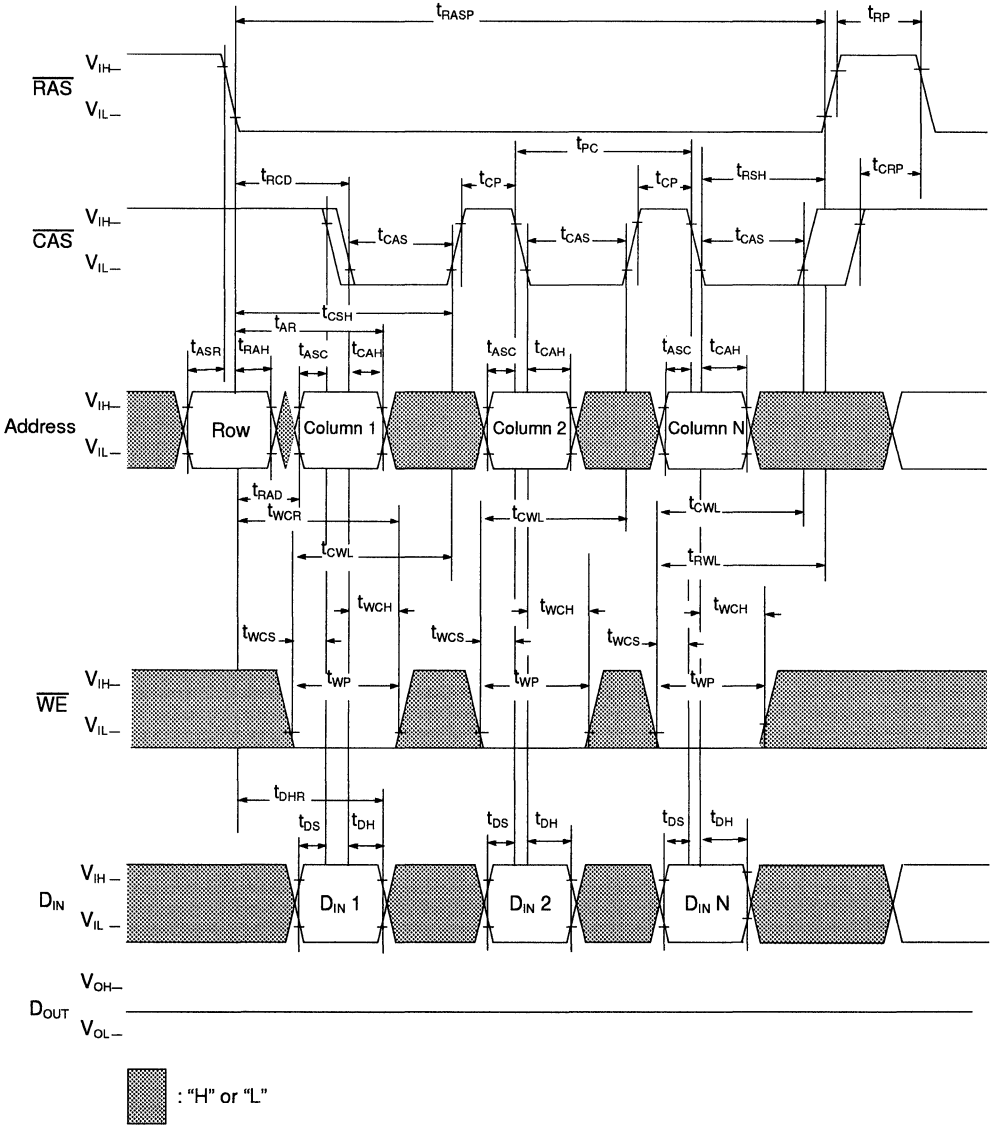
Write Cycle (Early Write)



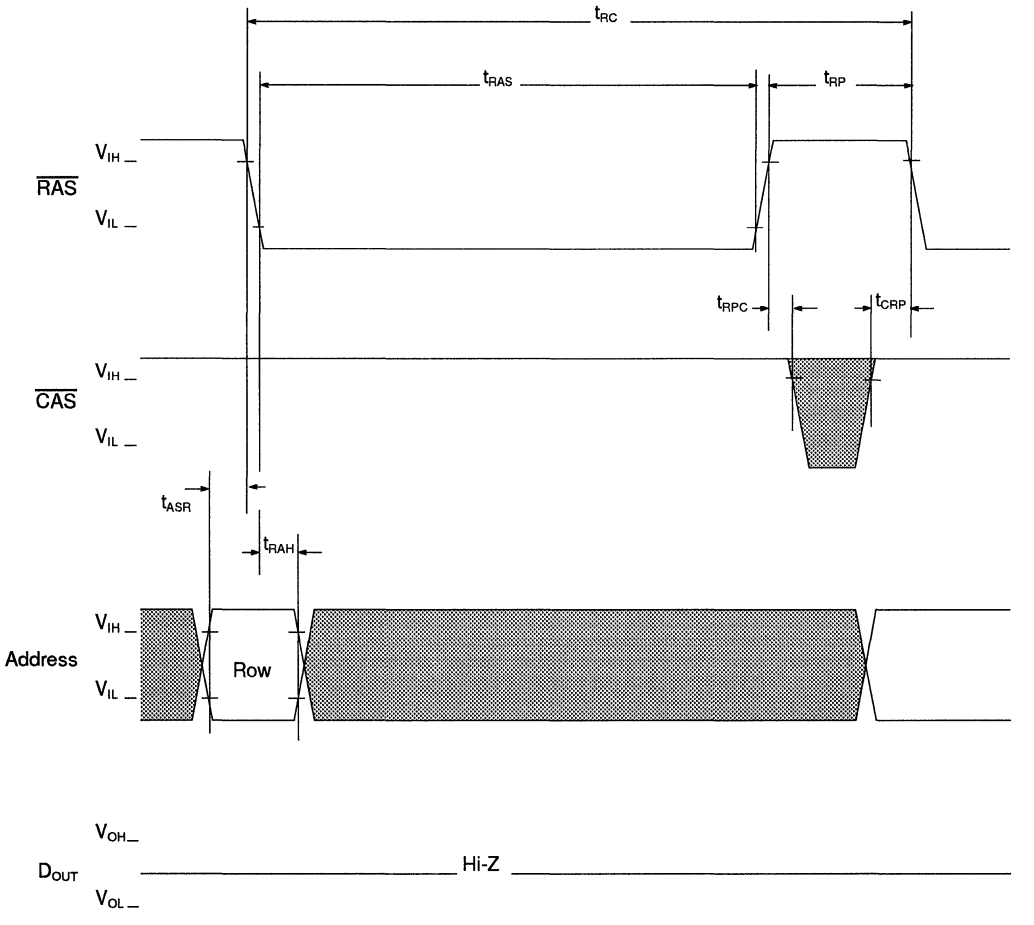
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



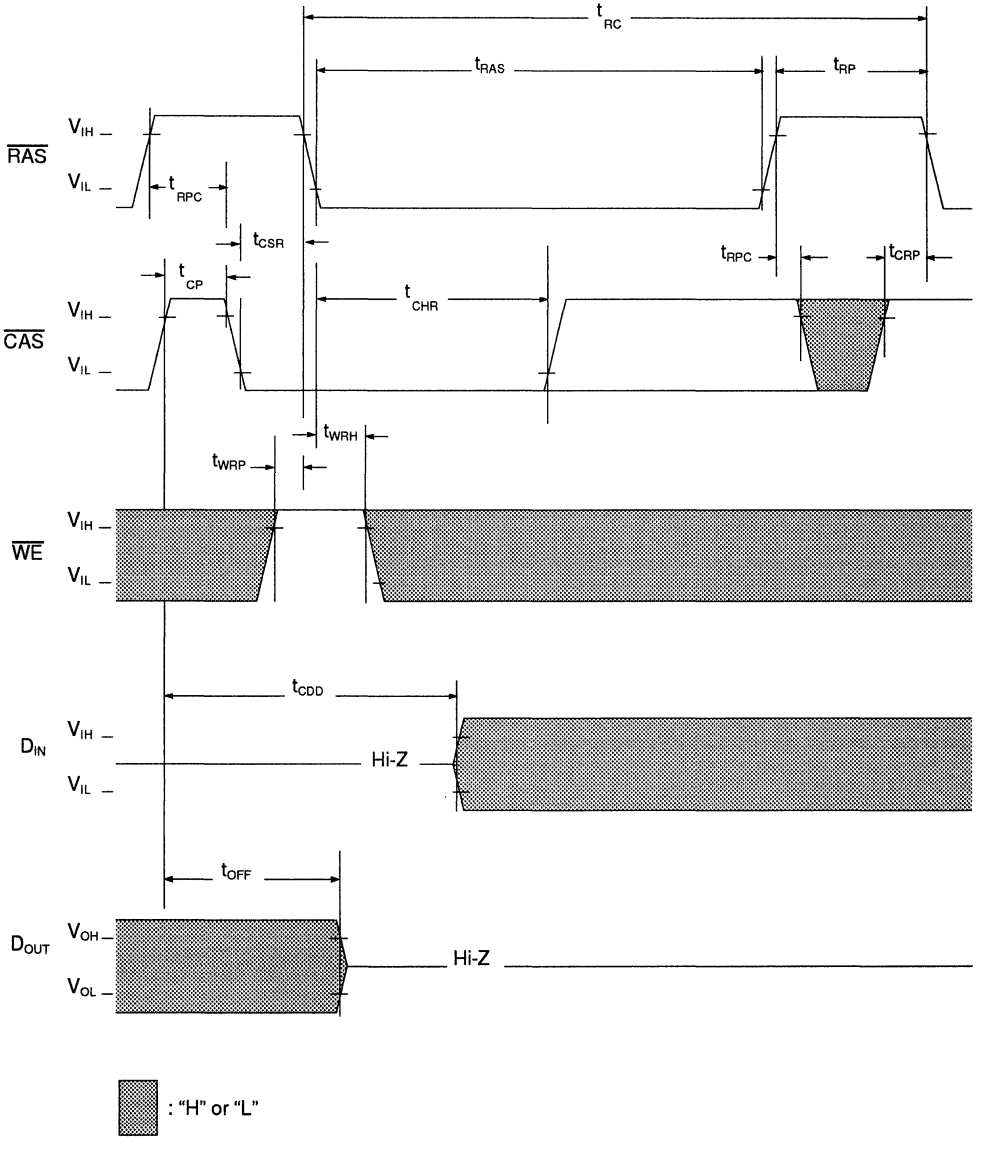
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

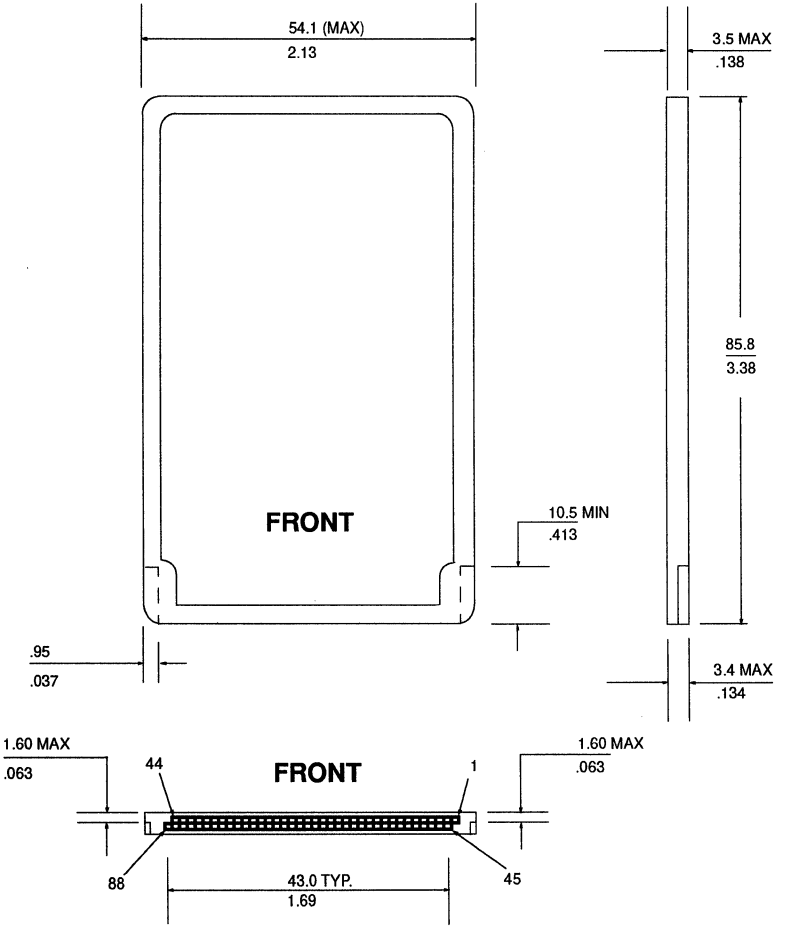
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

4M x 32 5.0V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

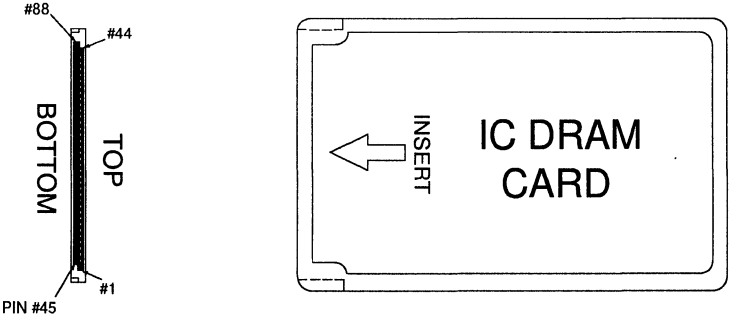
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns
t_{AA}	Access Time From Address	42ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 5.0V, ± 0.25V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- 12/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 4096 refresh cycles distributed across 256ms
- Polarized Connector

Description

The IBM11J4320CL is a 16MB industry standard 88-pin IC DRAM card. It is organized as a 4M x 32 high speed memory array. It is built using 8- 4Mx4 devices and is compatible to the JEDEC/PCMCIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x32 configuration the memory is a single bank, having four unique bytes. The x16 configuration may be utilized as two banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other bank in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. The related 4M x 36 version of this ICDRAM card is IBM11J4360DLA

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A11	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

Pinout

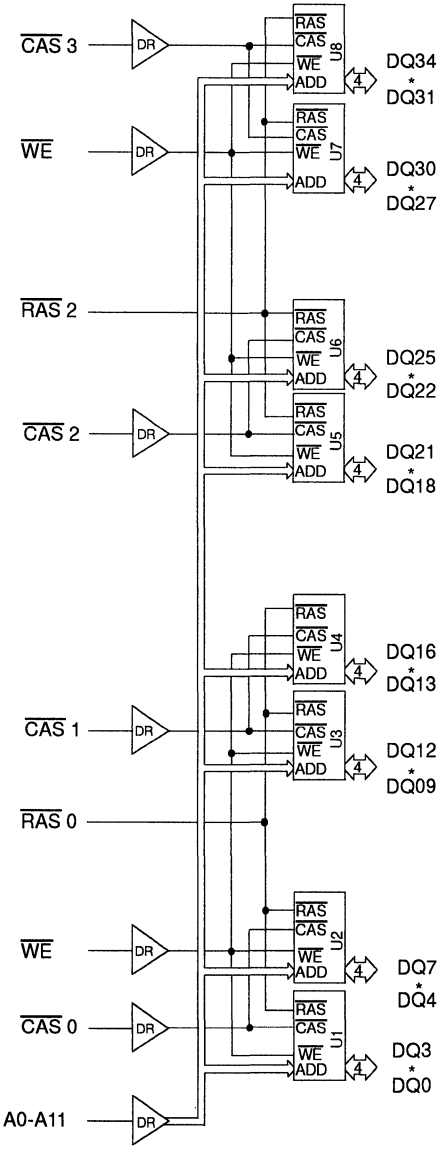
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	NC	47	DQ19	69	$\overline{NC}$
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	V_{CC}	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	V_{CC}	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	NC	76	PD8
11	NC	33	NC	55	NC	77	NC
12	NC	34	DQ9	56	V_{SS}	78	NC
13	A0	35	NC	57	A1	79	NC
14	A2	36	DQ10	58	A3	80	DQ27
15	V_{CC}	37	V_{CC}	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	NC	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	A11	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	A10	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	$\overline{NC}$	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

1. DQ numbering is compatible with parity (x36) version)

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J4320CLA-70	4M x 32	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	V_{SS}
PD3	NC
PD4	V_{SS}
PD5 (Number of Banks/Organization)	NC
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +7.0	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to V_{CC} + 0.5, 7.0	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	6.3	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.4	—	V_{CC} + 0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	43	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O}$	Output Capacitance (DQ0~DQ34)	25	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	600	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	16	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	600	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	520	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	1.6	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	600	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			2.4	mA	1, 2
$I_{I(L)}$	Input Leakage Current	$\overline{RAS}$	-40	+40	µA	
	Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V))	$\overline{CAS}$,ADD	-10	+10		
	All Other Pins Not Under Test = 0V	$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$) or 6ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	7	—	ns	
t_{RAH}	Row Address Hold Time	8	—	ns	
t_{ASC}	Column Address Setup Time	2	—	ns	
t_{CAH}	Column Address Hold Time	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	28	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 21ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 23ns (6ns before max t_{CAC} of 29ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	16	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	20	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	42	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	42	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	25	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	50	ns	1, 2

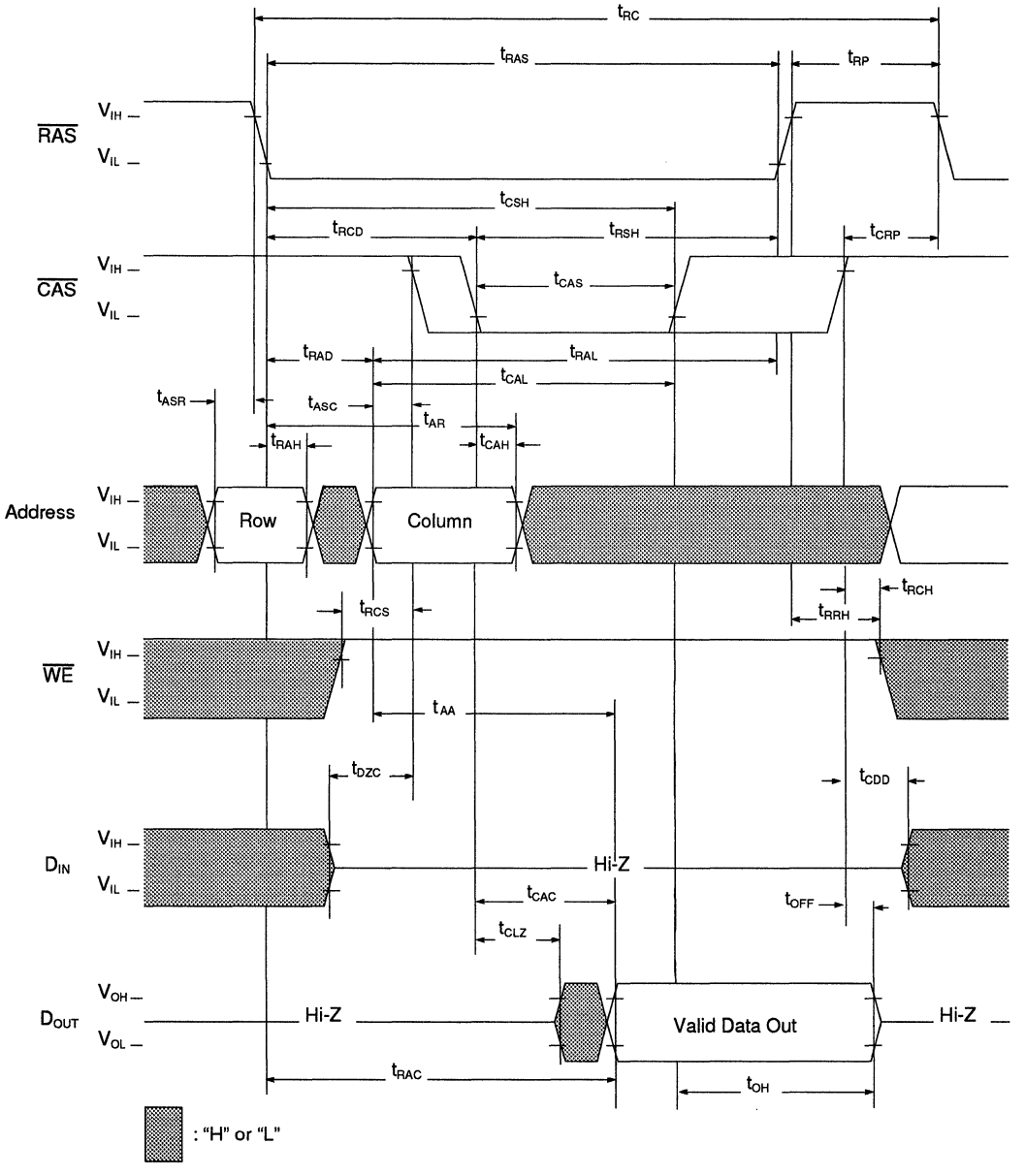
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

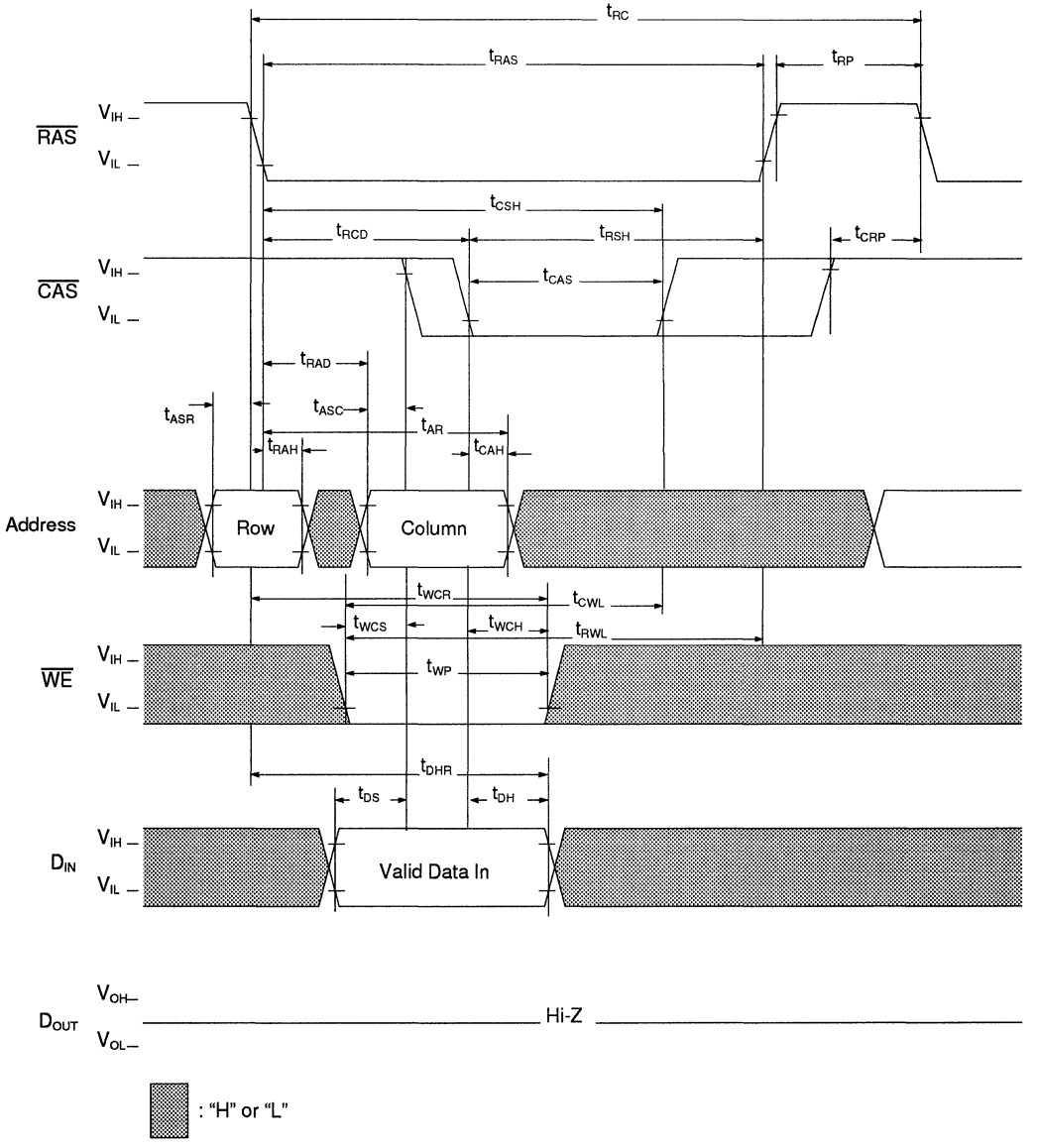
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	16	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	8	—	ns	
t_{REF}	Refresh Period	—	256	ns	1

1. 4096 refreshes are required every 256ms.

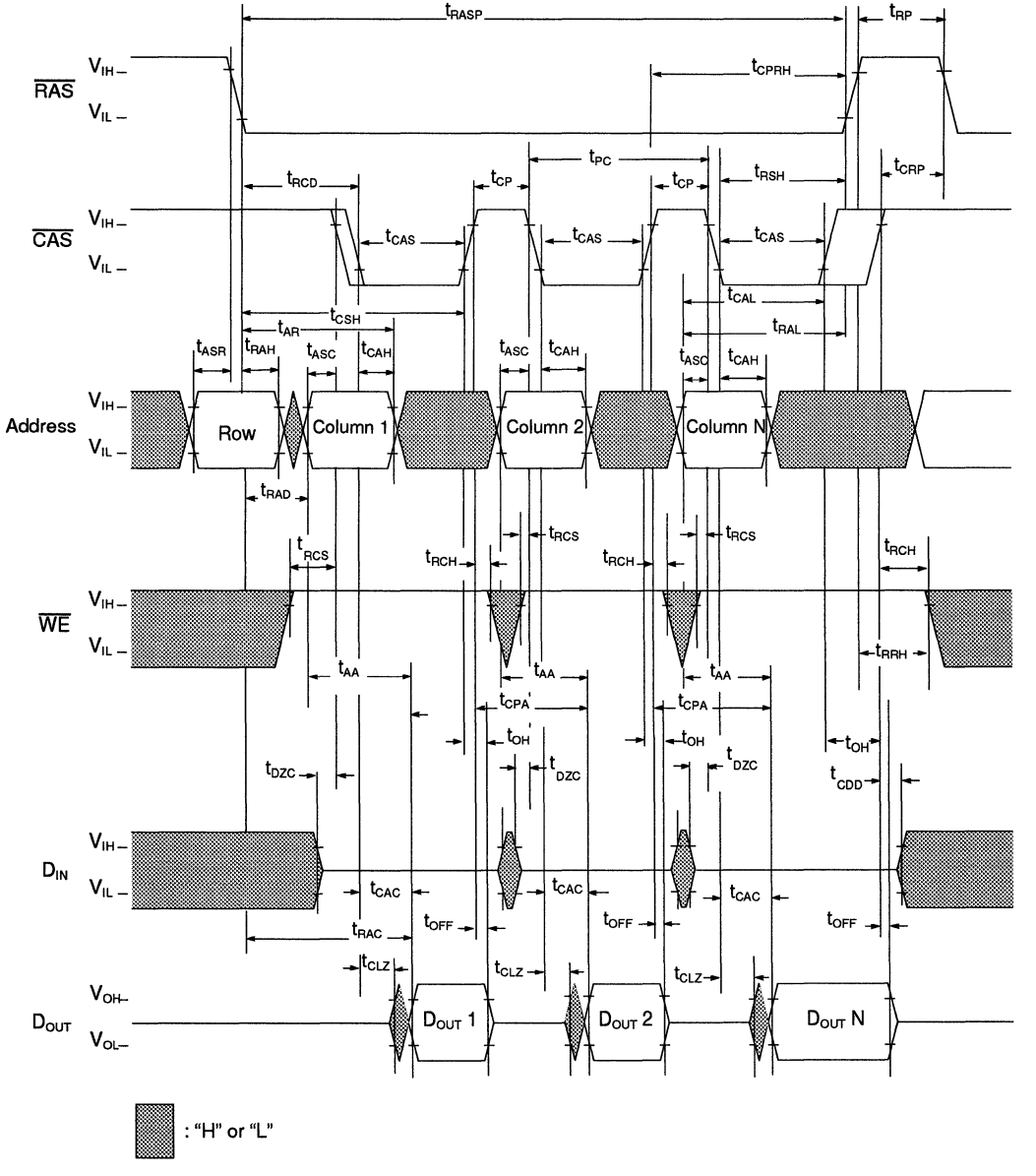
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

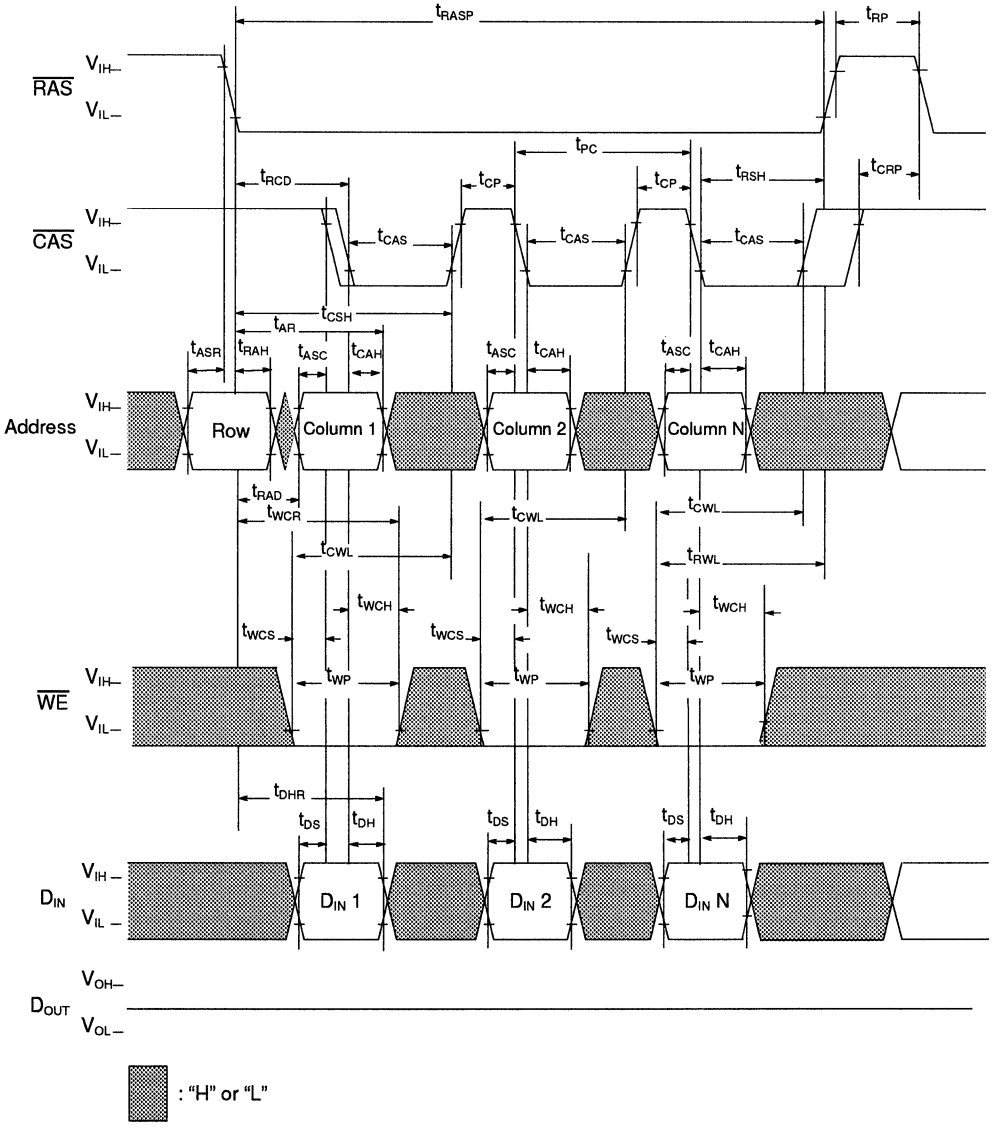
Write Cycle (Early Write)



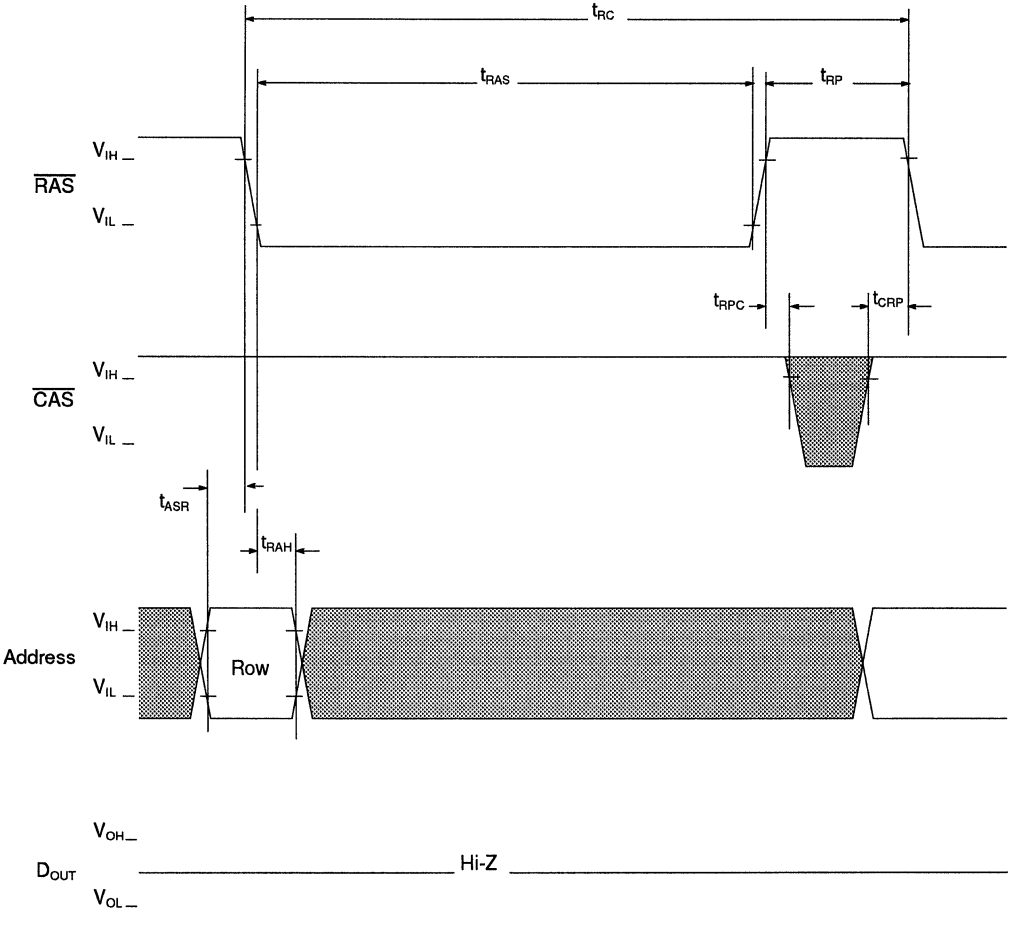
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



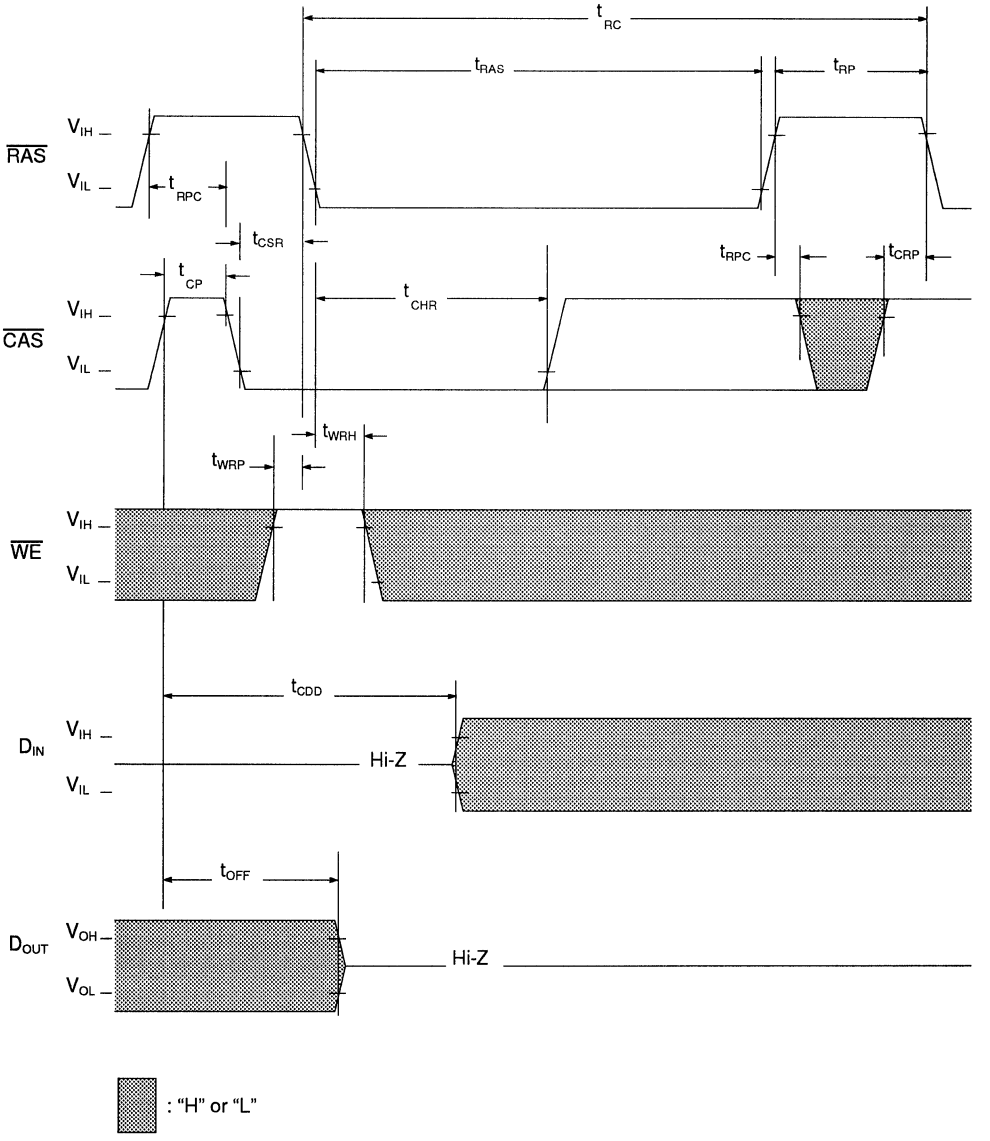
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

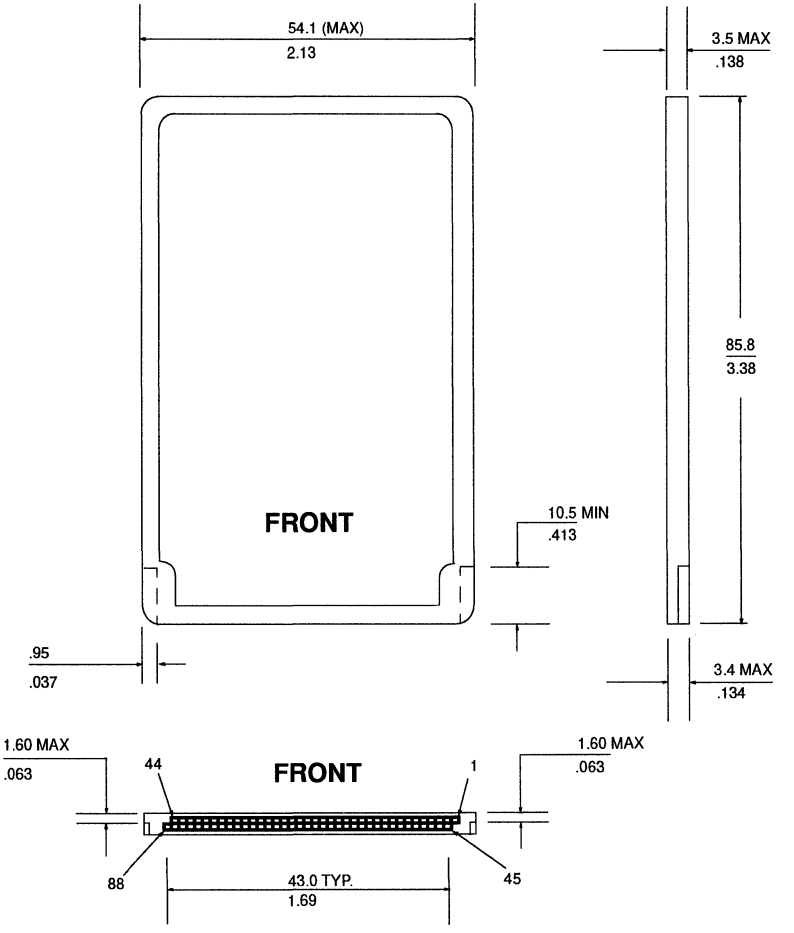
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

4M x 32 3.3V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

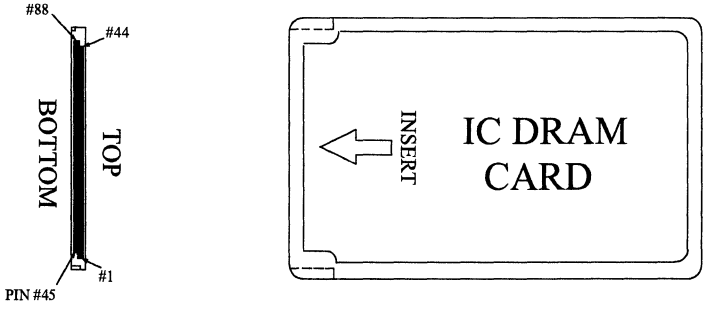
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns
t_{AA}	Access Time From Address	42ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 3.3V, ± 0.3V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- 12/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 4096 refresh cycles distributed across 256ms
- Polarized Connector

Description

The IBM11J4320CN is a 16MB industry standard 88-pin IC DRAM card. It is organized as a 4M x 32 high speed memory array. It is built using 8- 4Mx4 devices and is compatible to the JEDEC/PCMCIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x32 configuration the memory is a single bank, having four unique bytes. The x16 configuration may be utilized as two banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other bank in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. **Caution must be used to prevent insertion into a 5.0V application.**

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A11	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

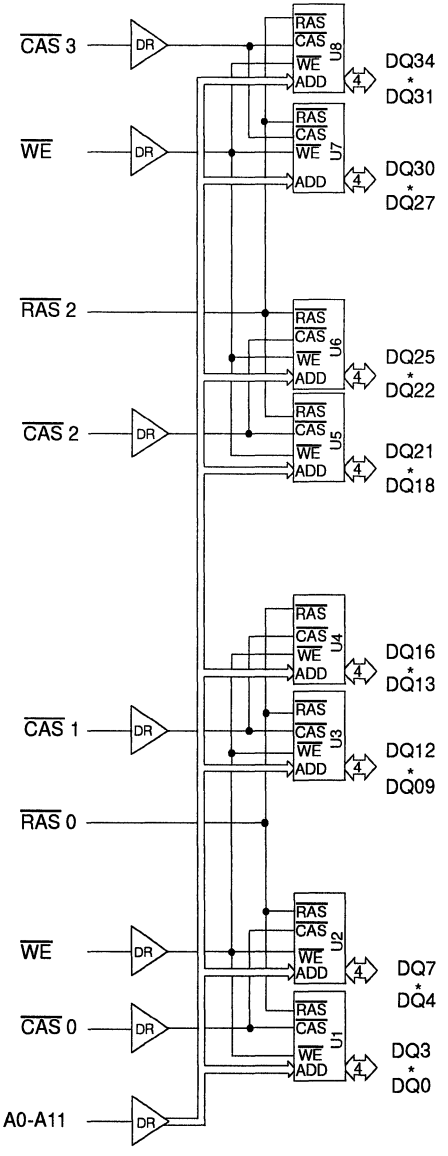
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	V_{CC}	47	DQ19	69	$\overline{NC}$
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	NC	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	NC	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	NC	76	PD8
11	V_{CC}	33	NC	55	NC	77	NC
12	NC	34	DQ9	56	V_{SS}	78	NC
13	A0	35	V_{CC}	57	A1	79	NC
14	A2	36	DQ10	58	A3	80	DQ27
15	NC	37	NC	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	V_{CC}	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	A11	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	A10	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	$\overline{NC}$	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J4320CNA-70	4M x 32	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	V_{SS}
PD3	NC
PD4	V_{SS}
PD5 (Number of Banks/Organization)	NC
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +4.6	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to min(V_{CC} + 0.5, 4.6)	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to min(V_{CC} + 0.5, 4.6)	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation		W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.0	—	V_{CC} + 0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 3.3± 0.3V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	43	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O}$	Output Capacitance (DQ0~DQ34)	25	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	600	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	16	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	600	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	520	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	1.6	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	600	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			2.4	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 3.3± 0.3V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$) or 6ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	7	—	ns	
t_{RAH}	Row Address Hold Time	8	—	ns	
t_{ASC}	Column Address Setup Time	2	—	ns	
t_{CAH}	Column Address Hold Time	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	28	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 20ns plus a minimum t_{OH} of 1ns would result in turning data out of the card at 21ns (3ns before max t_{CAC} of 24ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	16	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	20	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	42	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	42	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	25	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	50	ns	1, 2

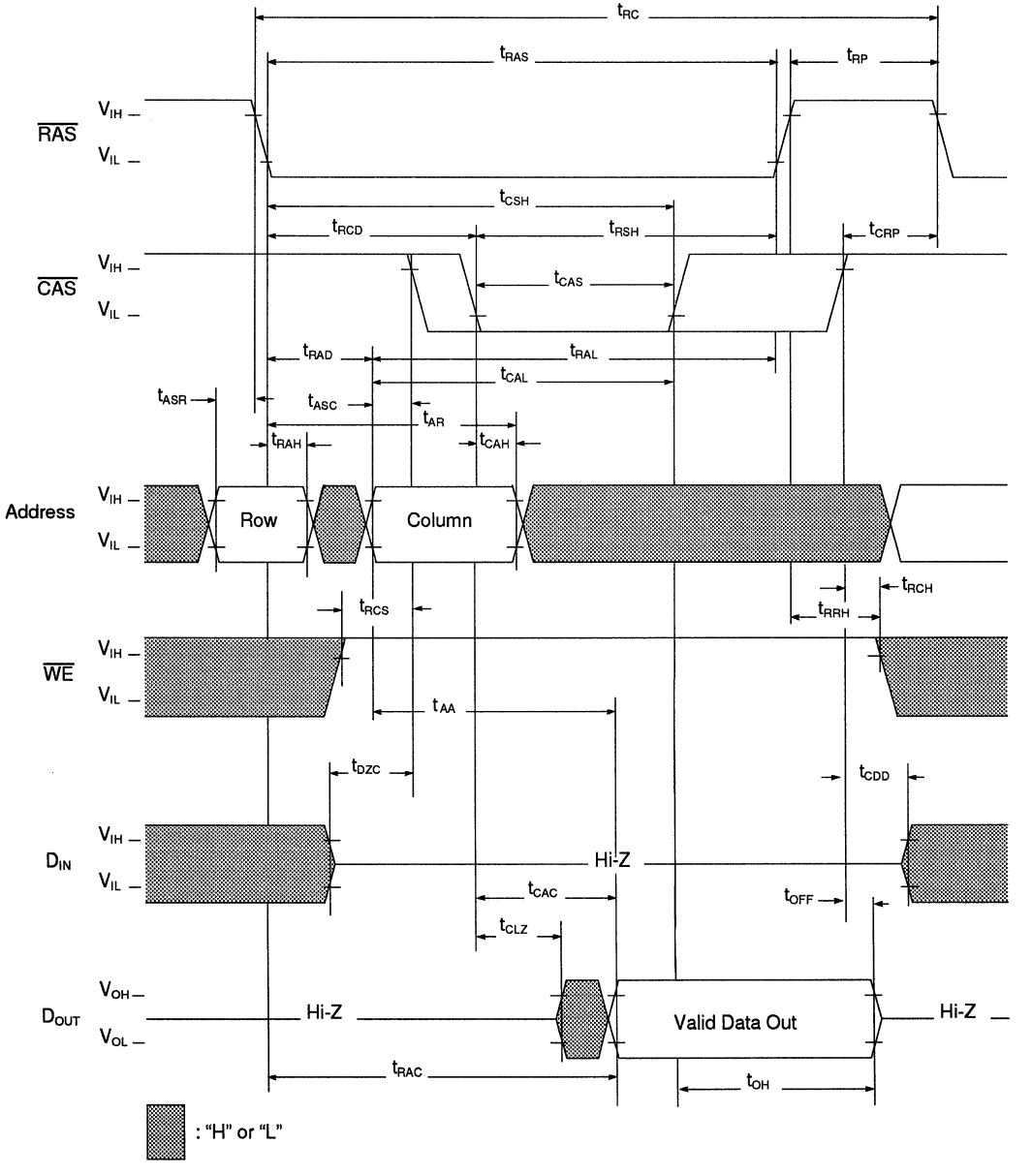
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

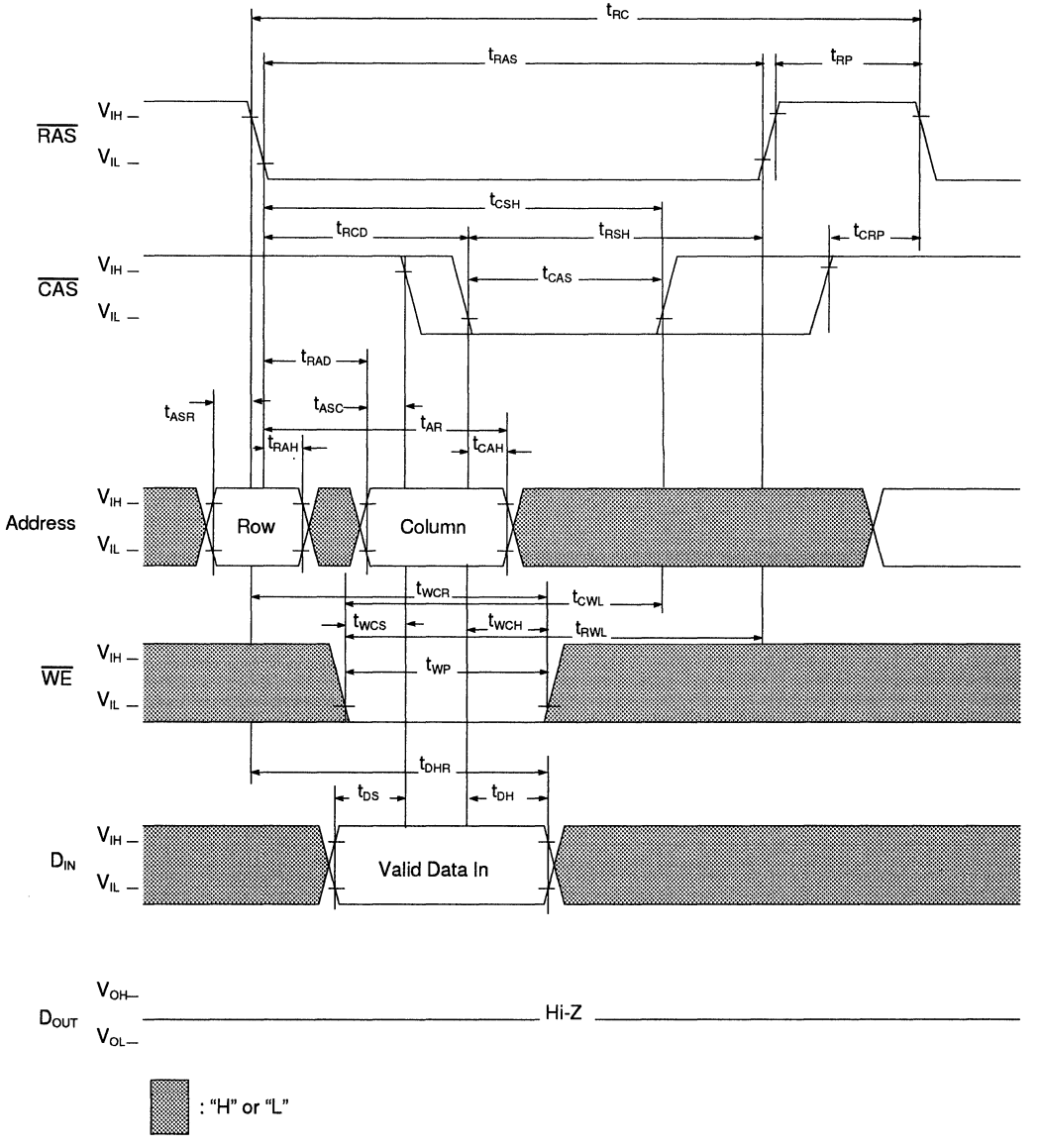
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	16	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	8	—	ns	
t_{REF}	Refresh Period	—	256	ns	1

1. 4096 refreshes are required every 256ms.

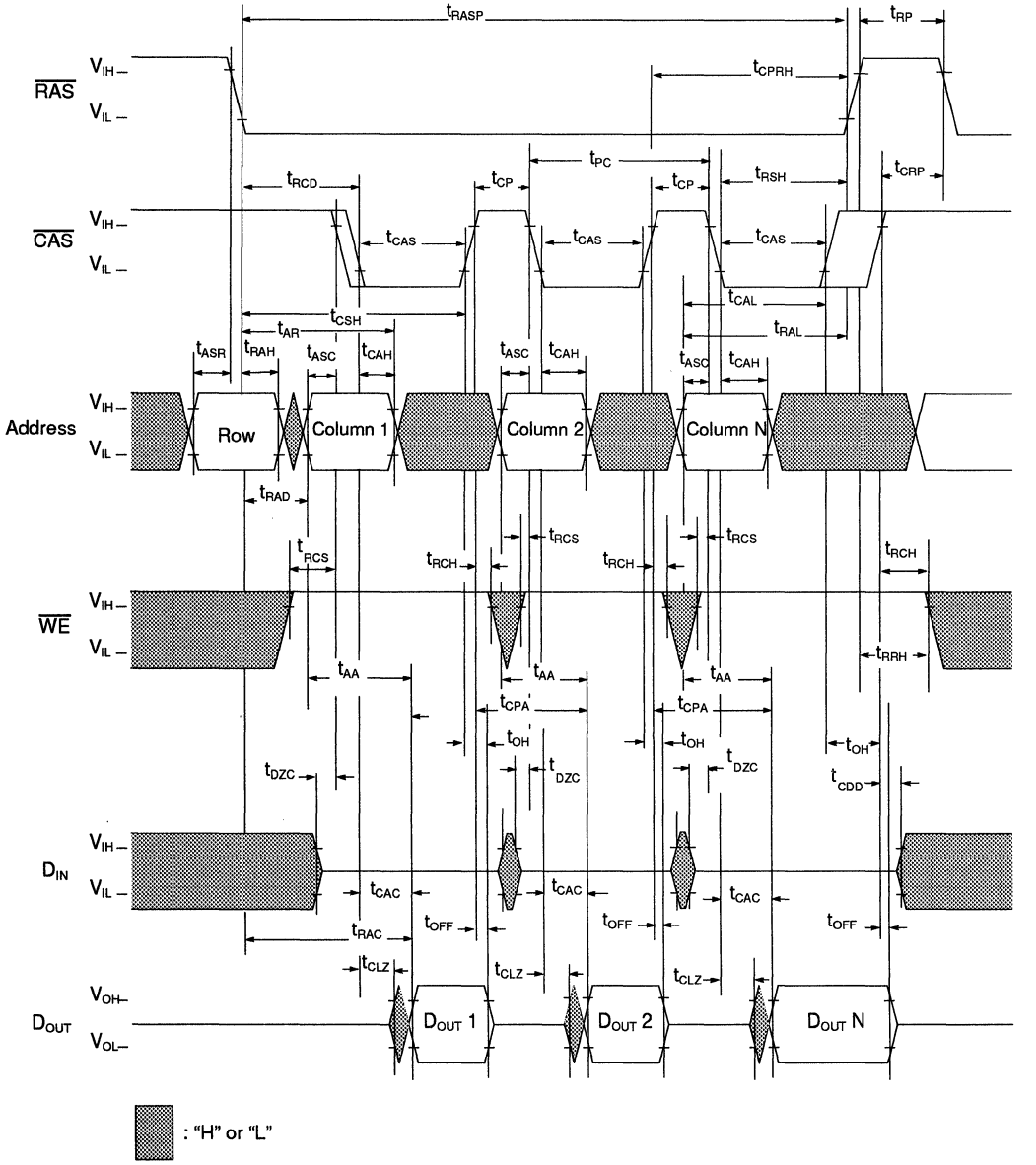
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

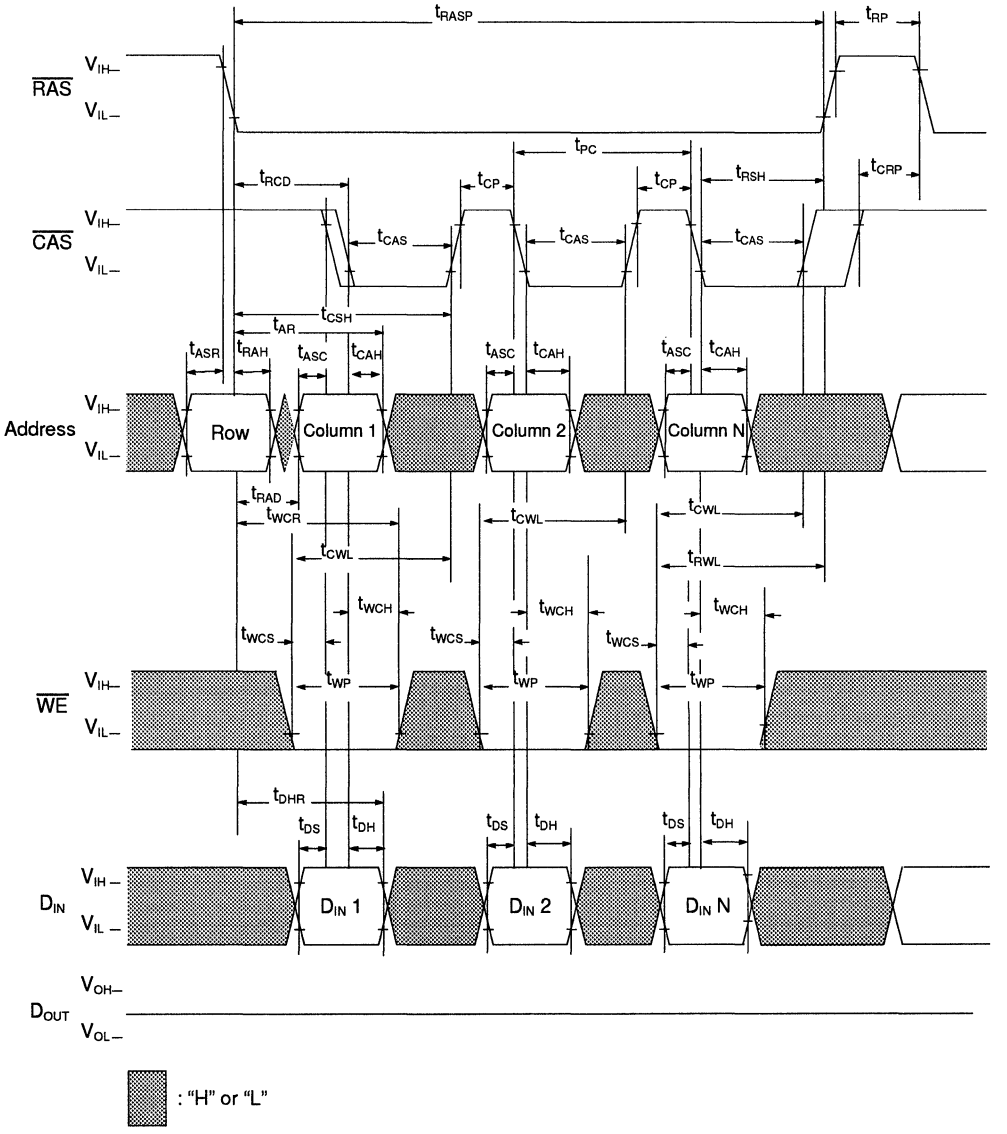
Write Cycle (Early Write)



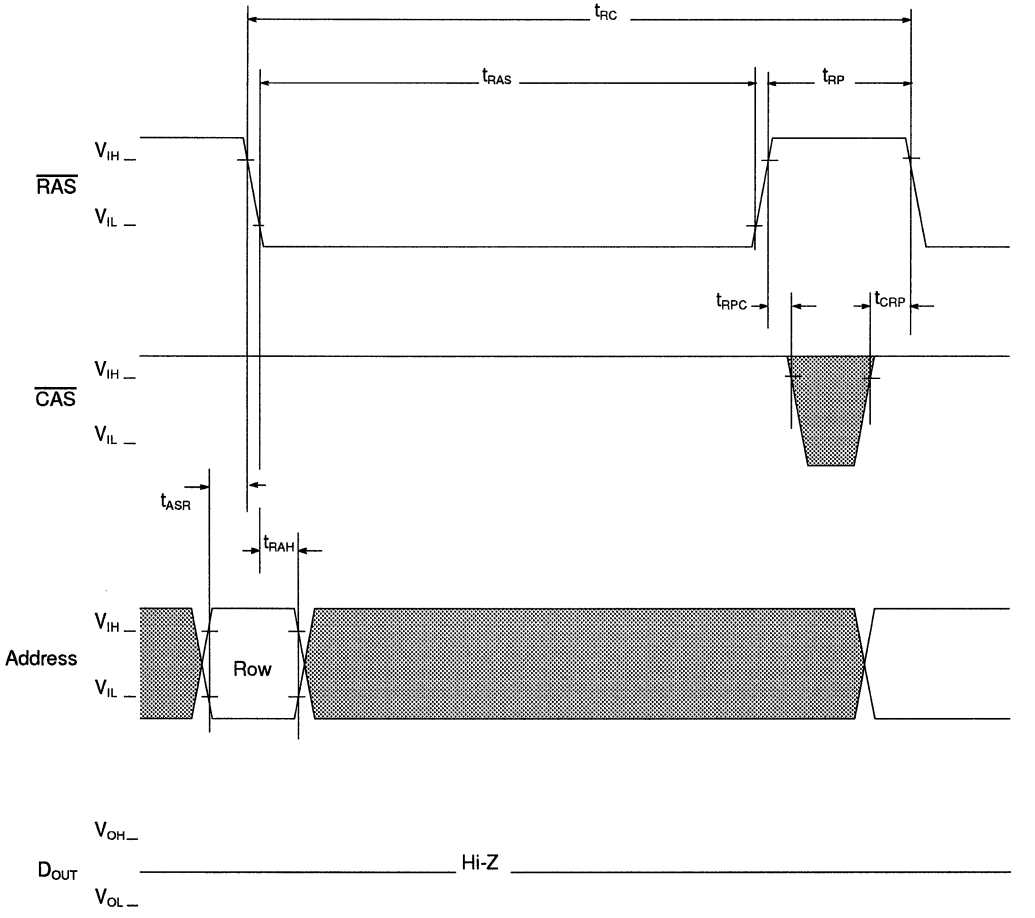
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



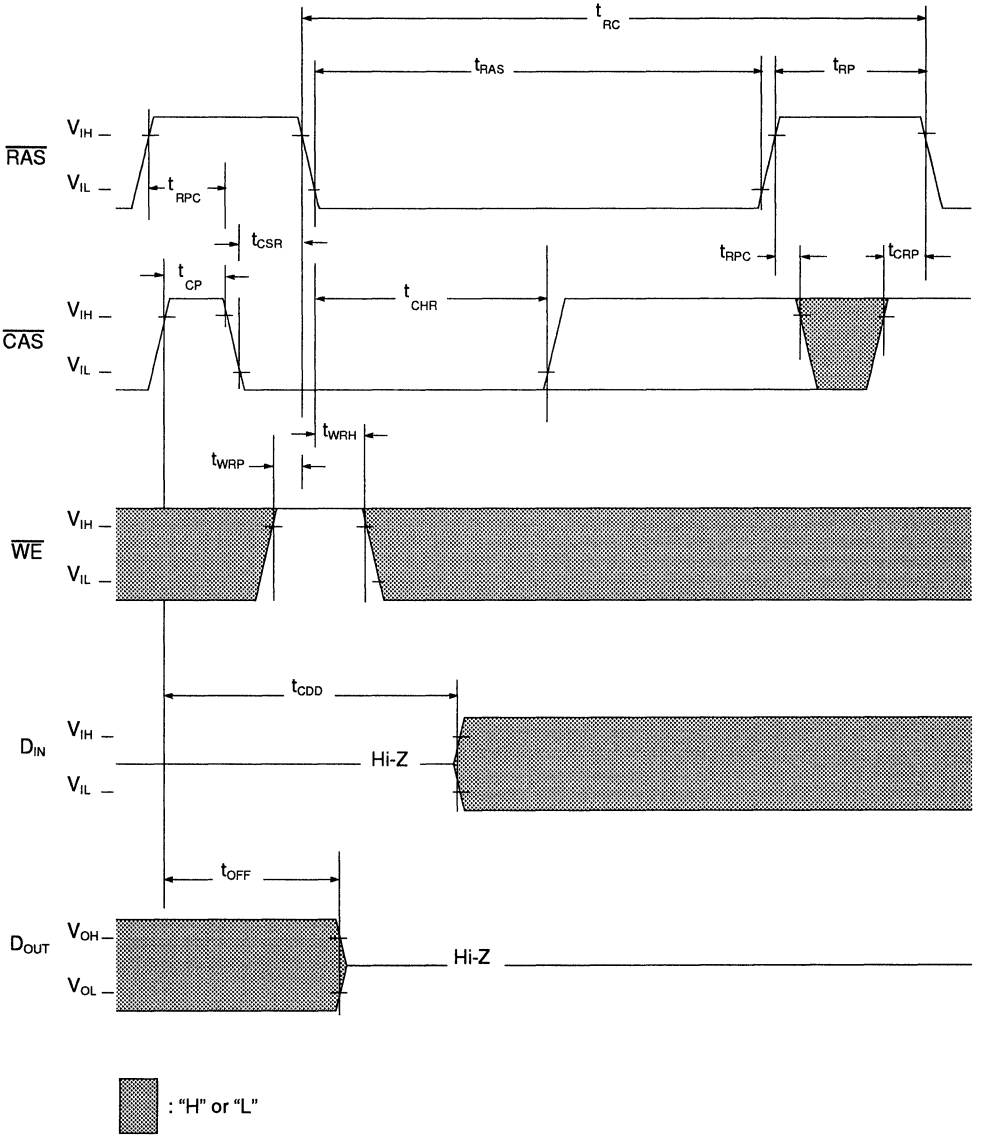
$\overline{\text{RAS}}$ Only Refresh Cycle



: "H" or "L"

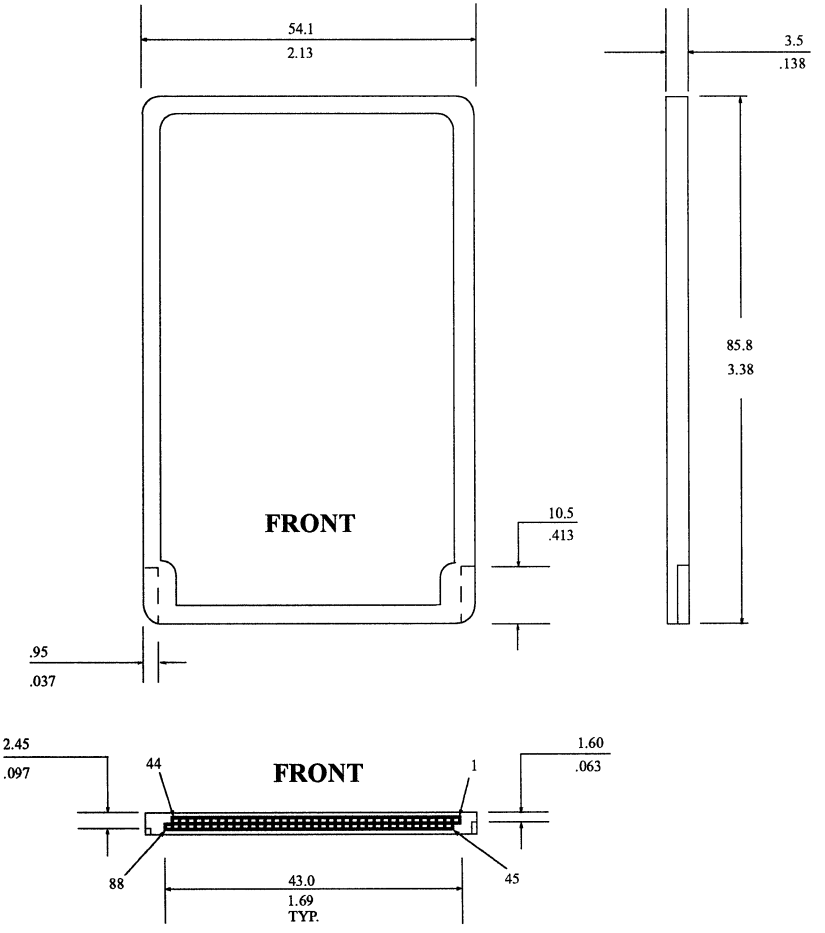
Note: $\overline{\text{WE}}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

8M x 32 5.0V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

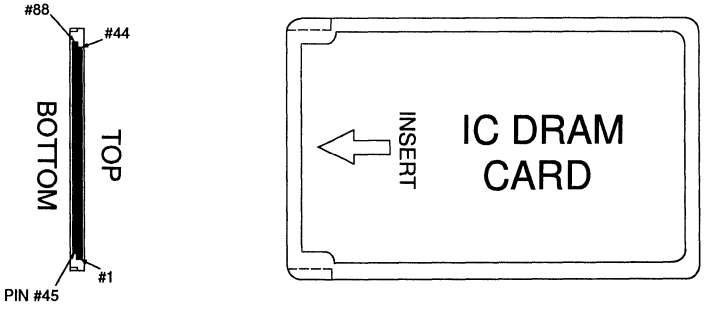
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns
t_{AA}	Access Time From Address	42ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 5.0V, ± 0.25V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- 12/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 4096 refresh cycles distributed across 256ms
- Polarized Connector

Description

The IBM11J8320CL is a 32MB industry standard 88-pin IC DRAM card. It is organized as a 8M x 32 high speed memory array. It is built using 16 - 4Mx4 devices and is compatible to the JEDEC/PCM-CIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x32 configuration the memory may be utilized as two banks, each having four unique bytes. The x16 configuration may be utilized as four banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other banks in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. The related 8M x 36 version of this ICDRAM card is IBM11J8360DLA

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A11	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

Pinout

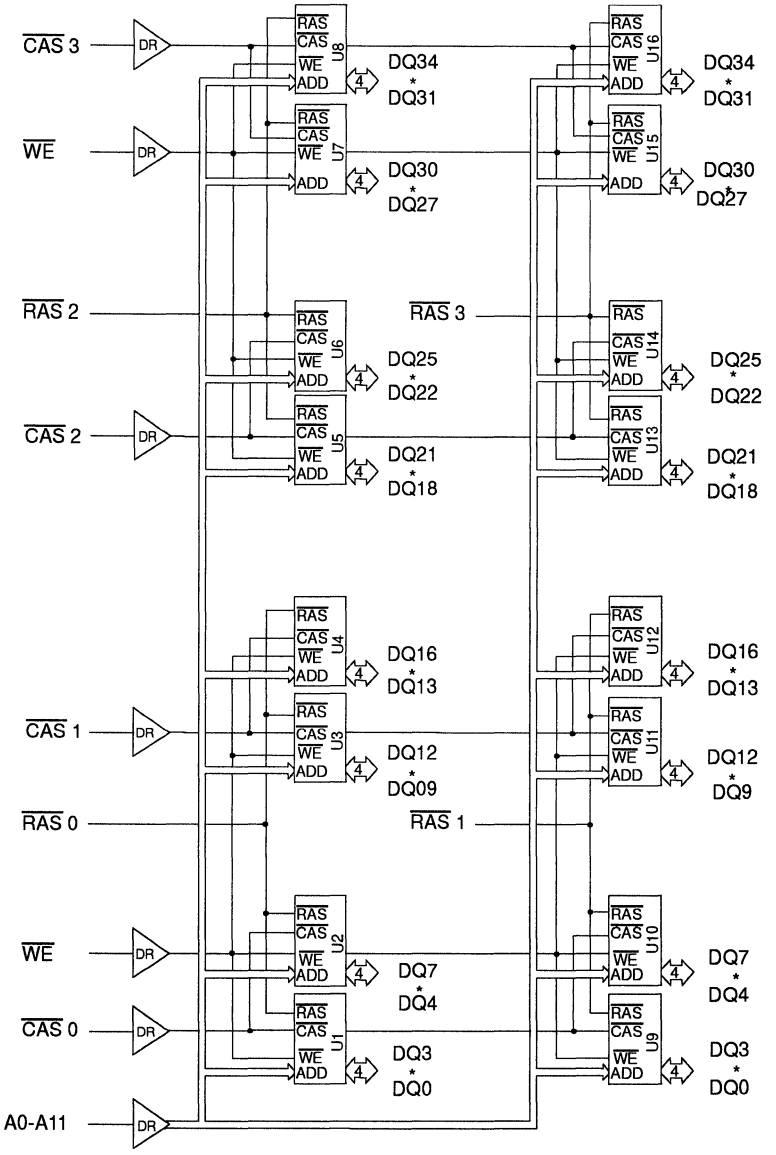
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	NC	47	DQ19	69	$\overline{RAS3}$
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	V_{CC}	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	V_{CC}	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	NC	76	PD8
11	NC	33	NC	55	NC	77	NC
12	NC	34	DQ9	56	V_{SS}	78	NC
13	A0	35	NC	57	A1	79	NC
14	A2	36	DQ10	58	A3	80	DQ27
15	V_{CC}	37	V_{CC}	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	NC	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	A11	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	A10	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	$\overline{RAS1}$	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

1. DQ numbering is compatible with parity (x36) version)

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J8320CLA-70	8M x 32	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	V_{SS}
PD3	NC
PD4	V_{SS}
PD5 (Number of Banks/Organization)	V_{SS}
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +7.0	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to V_{CC} + 0.5, 7.0	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	11.8	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.4	—	V_{CC} + 0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	43	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O}$	Output Capacitance (DQ0~DQ34)	32	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	600	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	32	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	600	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	520	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	3.2	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	600	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			4.8	mA	1, 2
$I_{I(L)}$	Input Leakage Current	$\overline{RAS}$	-40	+40	µA	
	Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V))	$\overline{CAS}$,ADD	-10	+10		
	All Other Pins Not Under Test = 0V	$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 10s ($\overline{CAS}$, $\overline{WE}$) or 11ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	7	—	ns	
t_{RAH}	Row Address Hold Time	8	—	ns	
t_{ASC}	Column Address Setup Time	2	—	ns	
t_{CAH}	Column Address Hold Time	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	28	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 21ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 23ns (6ns before max t_{CAC} of 29ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	16	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	20	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	42	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	42	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	25	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	50	ns	1, 2

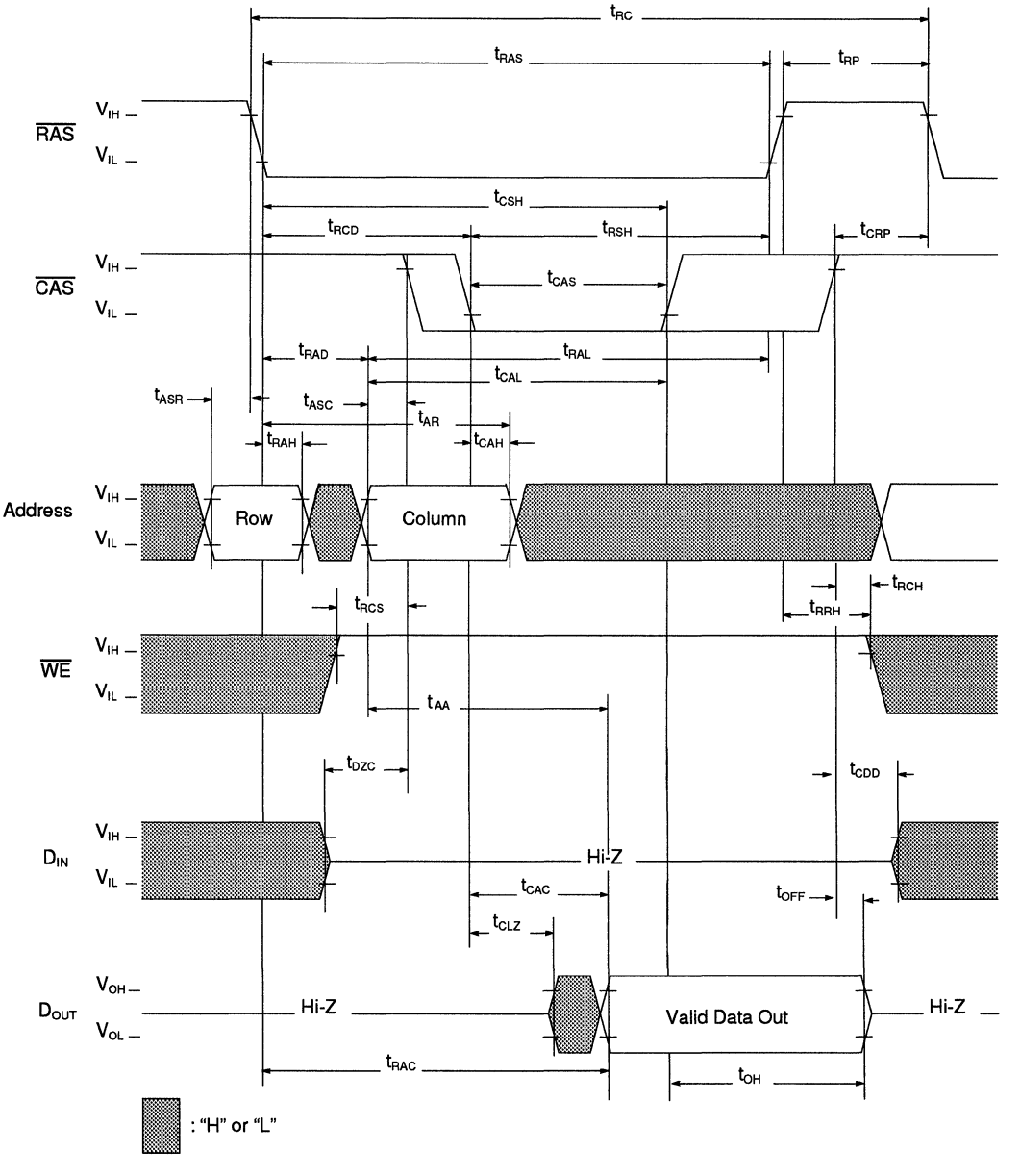
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

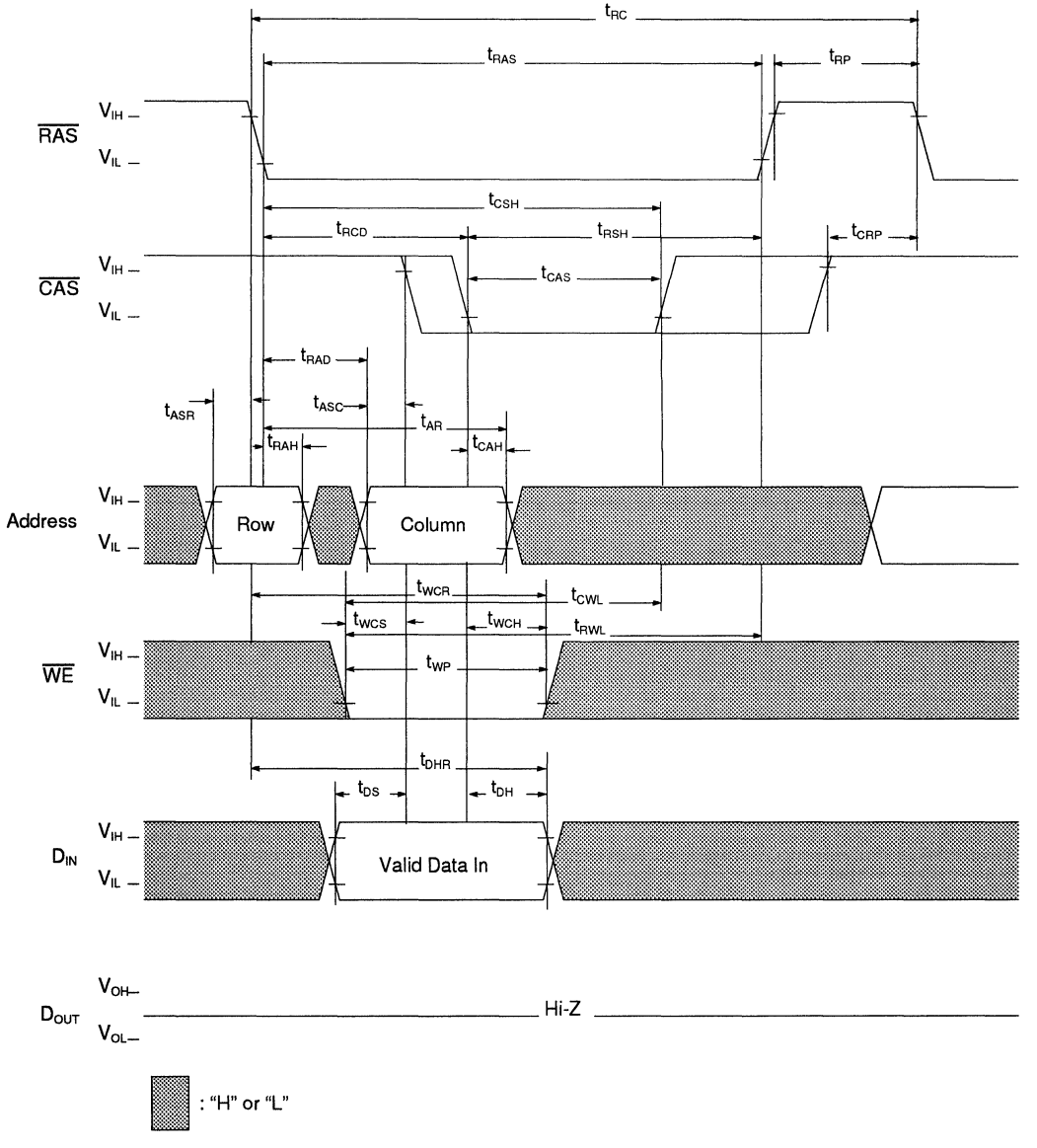
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	16	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	8	—	ns	
t_{REF}	Refresh Period	—	256	ns	1

1. 4096 refreshes are required every 256ms.

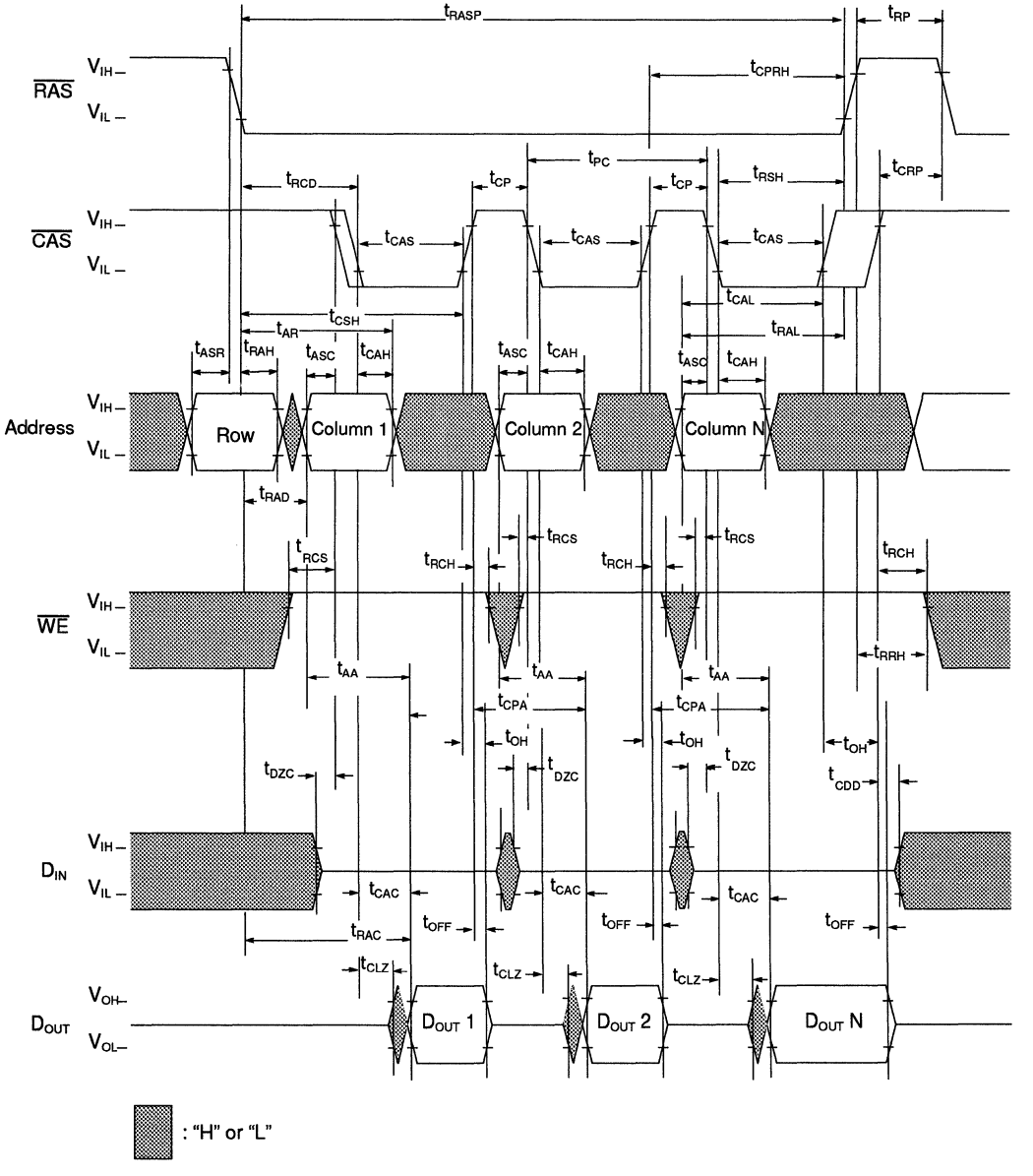
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCH
tRRH
tRCS
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

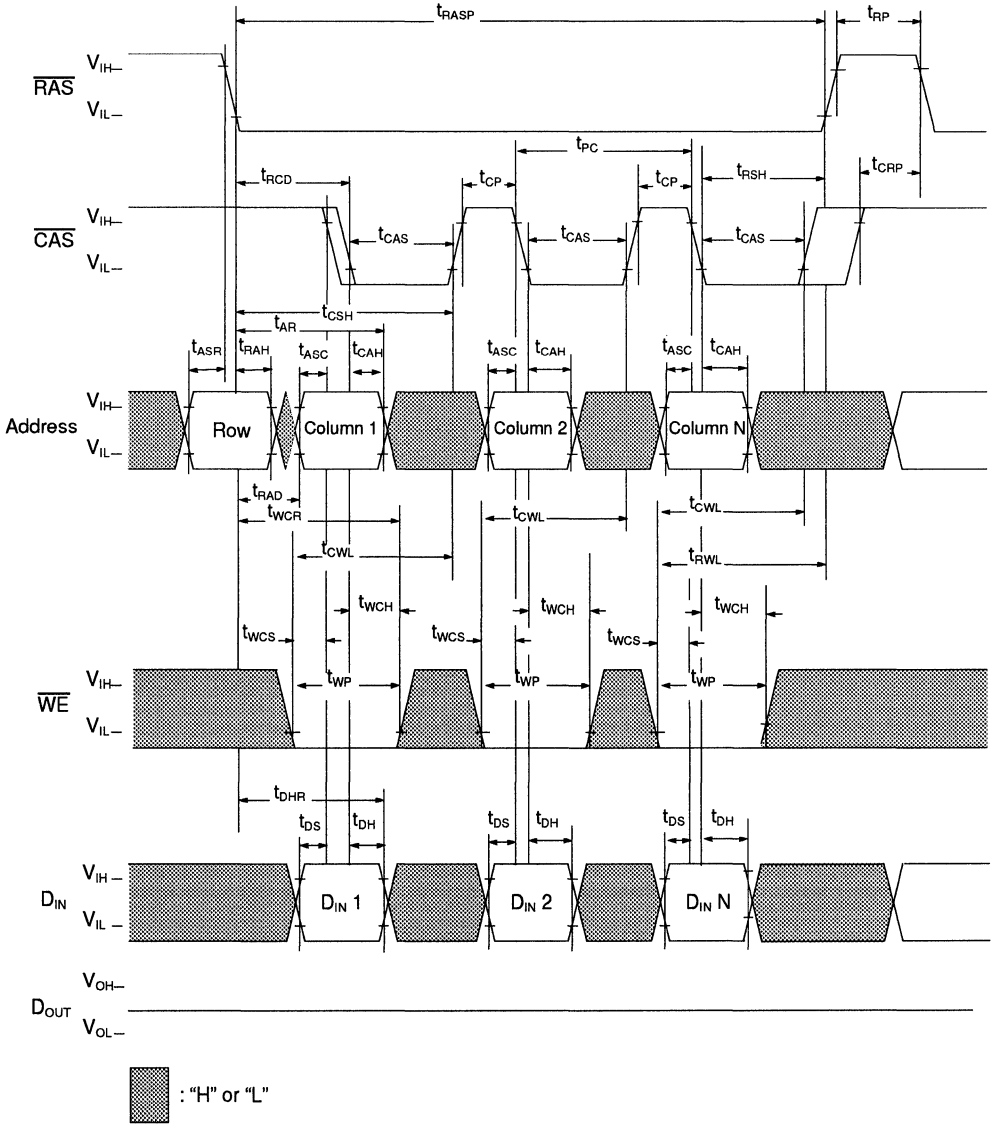
Write Cycle (Early Write)



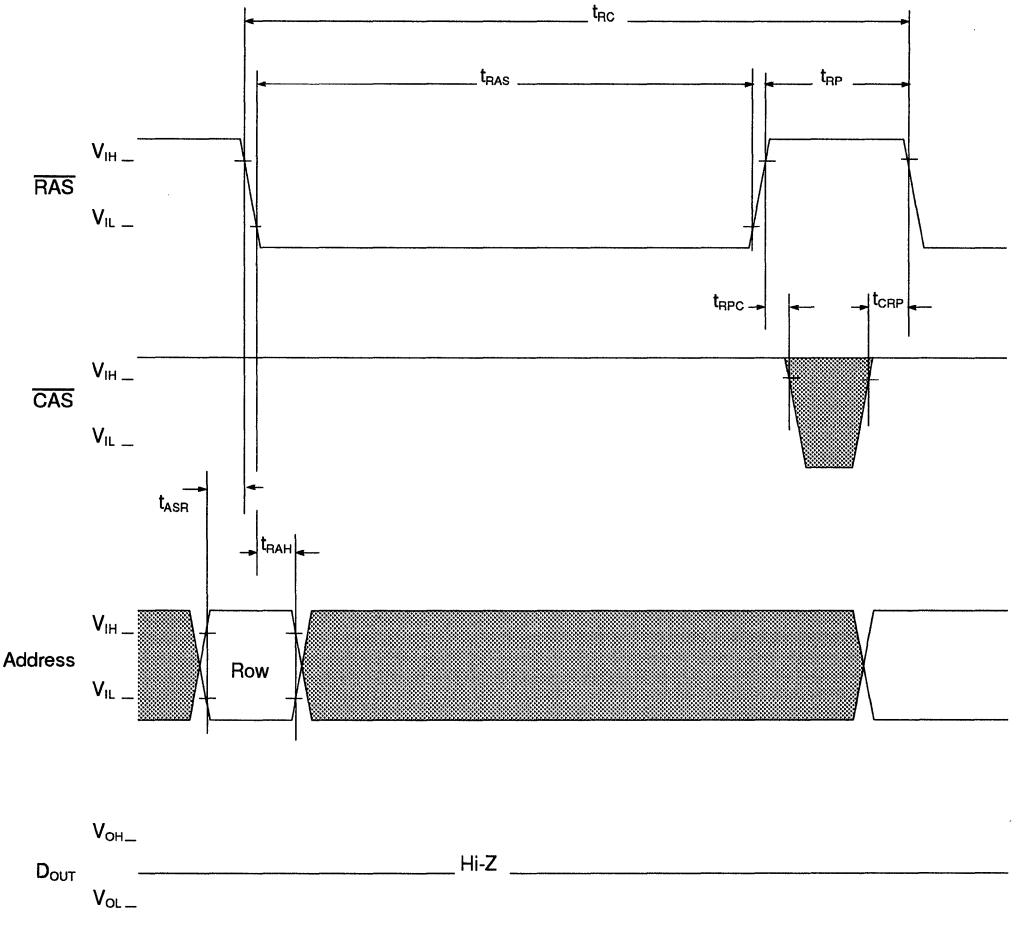
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



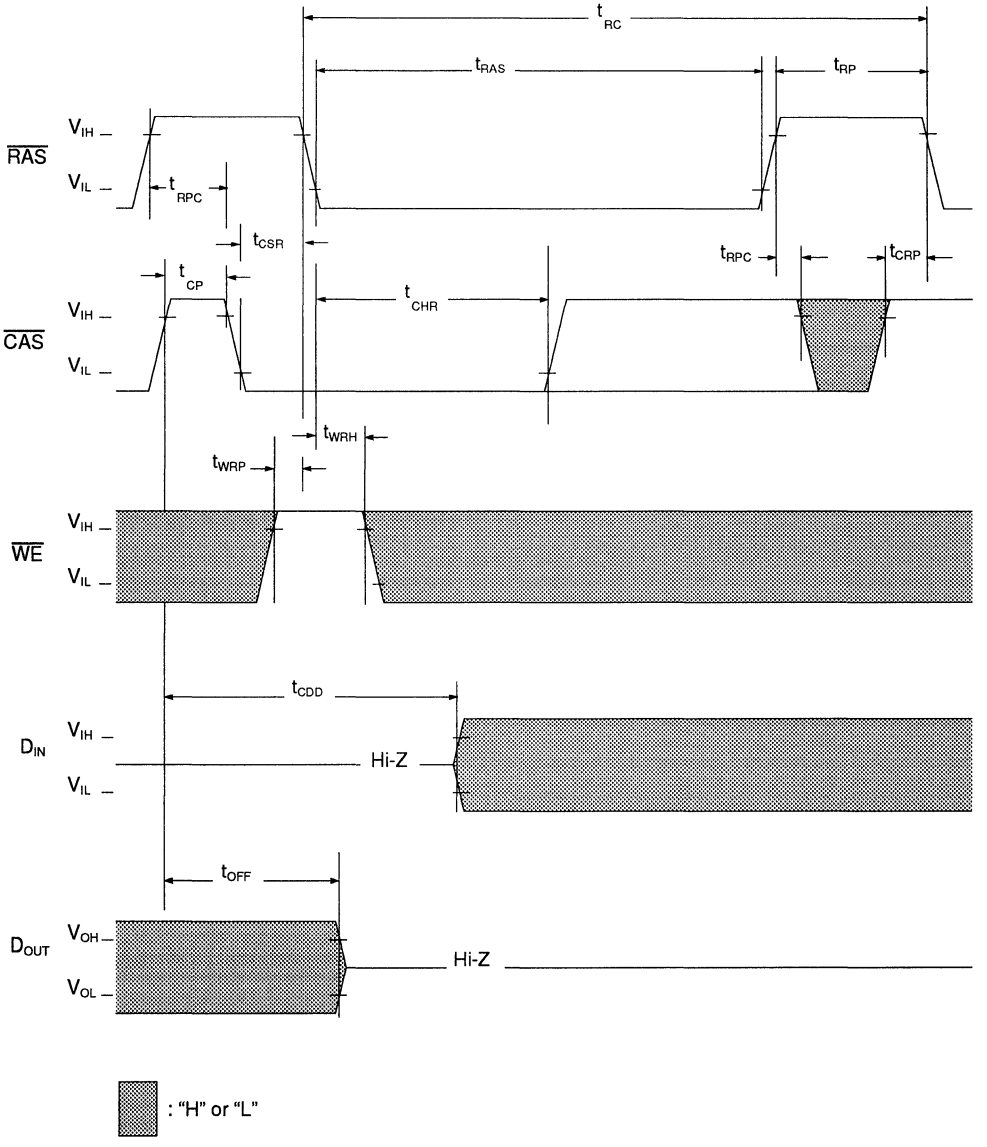
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

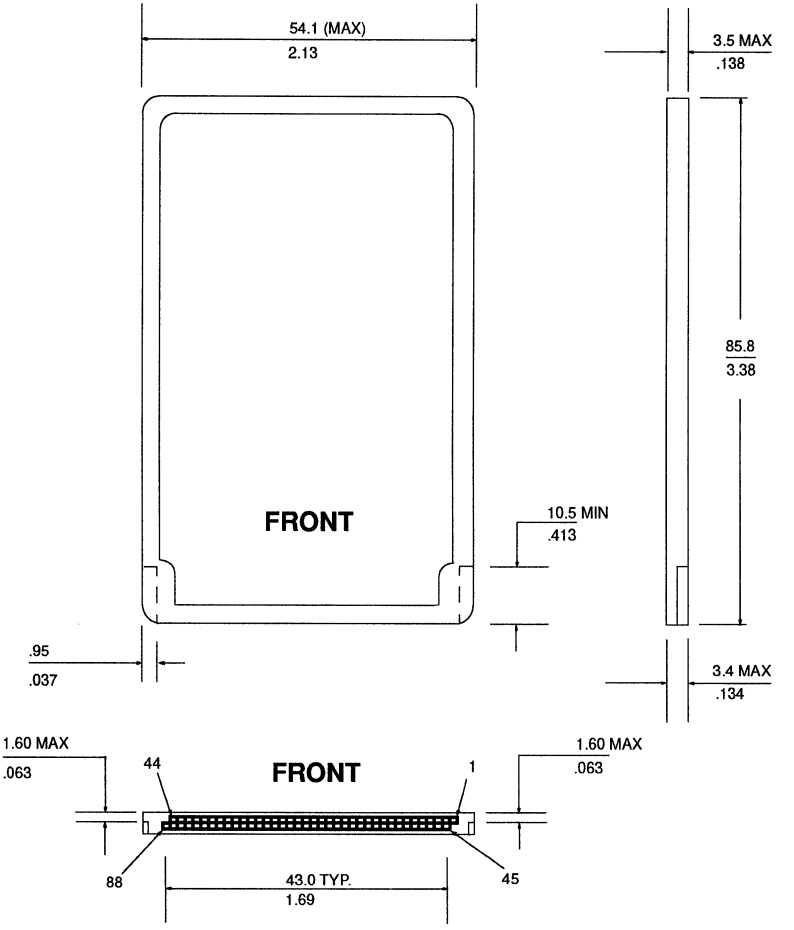
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

8M x 32 3.3V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

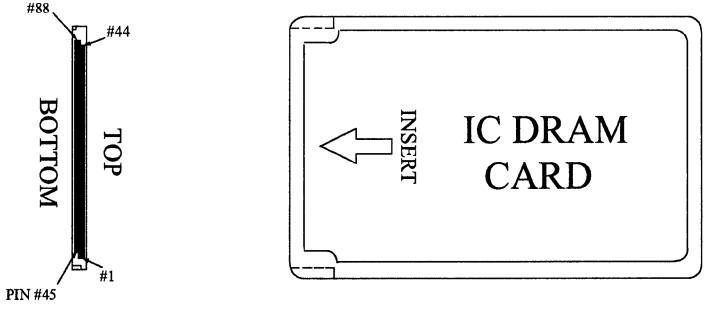
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns
t_{AA}	Access Time From Address	42ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 3.3V, ± 0.3V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- 12/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 4096 refresh cycles distributed across 256ms
- Polarized Connector

Description

The IBM11J8320CN is a 32MB industry standard 88-pin IC DRAM card. It is organized as a 8M x 32 high speed memory array. It is built using 16- 4Mx4 devices and is compatible to the JEDEC/PCMCIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x32 configuration the memory may be utilized as two banks, each having four unique bytes. The x16 configuration may be utilized as frour banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other banks in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. **Caution must be used to prevent insertion into a 5.0V application.**

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A11	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

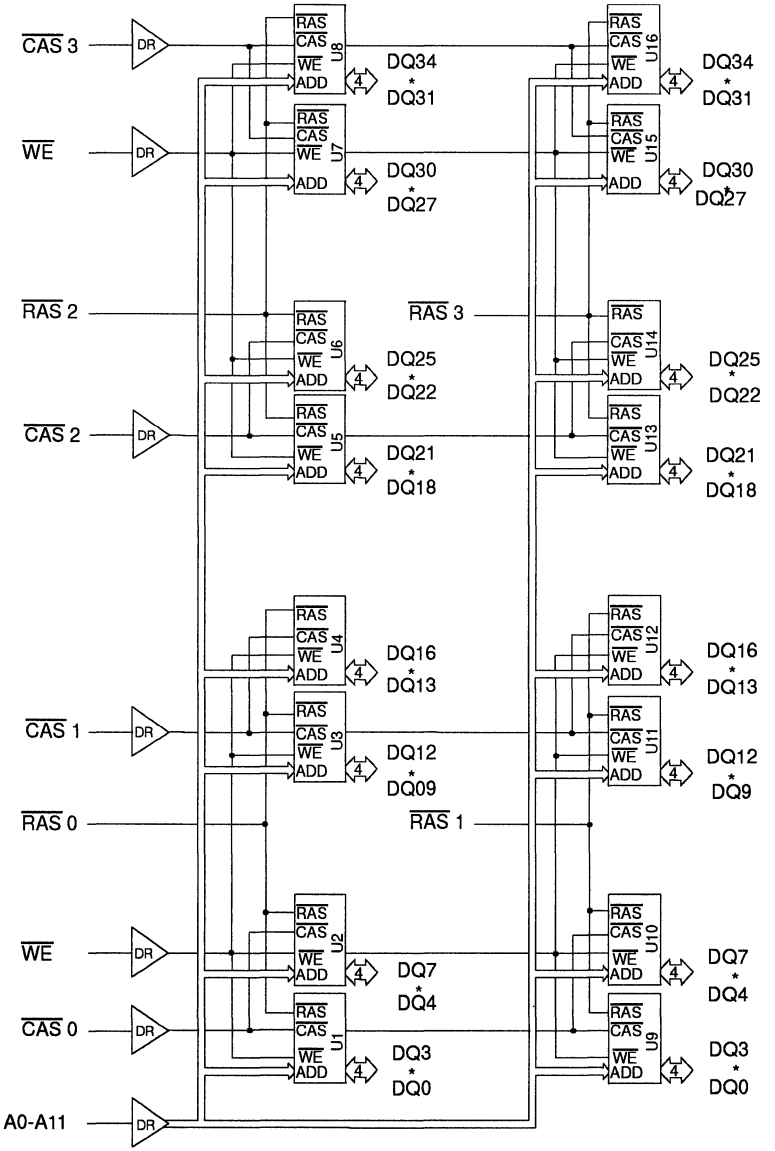
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	V_{CC}	47	DQ19	69	$\overline{RAS3}$
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	NC	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	NC	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	NC	76	PD8
11	V_{CC}	33	NC	55	NC	77	NC
12	NC	34	DQ9	56	V_{SS}	78	NC
13	A0	35	V_{CC}	57	A1	79	NC
14	A2	36	DQ10	58	A3	80	DQ27
15	NC	37	NC	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	V_{CC}	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	A11	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	A10	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	$\overline{RAS1}$	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J8320CNA-70	8M x 32	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	V_{SS}
PD3	NC
PD4	V_{SS}
PD5 (Number of Banks/Organization)	V_{SS}
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +4.6	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to min(V_{CC} + 0.5, 4.6)	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to min(V_{CC} + 0.5, 4.6)	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation		W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.0	—	V_{CC} + 0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 3.3± 0.3V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	43	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O}$	Output Capacitance (DQ0~DQ34)	32	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 3.3± 0.3V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	600	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	32	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	600	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	520	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	3.2	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	600	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			4.8	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 3.3± 0.3V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$) or 6ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	7	—	ns	
t_{RAH}	Row Address Hold Time	8	—	ns	
t_{ASC}	Column Address Setup Time	2	—	ns	
t_{CAH}	Column Address Hold Time	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	28	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 20ns plus a minimum t_{OH} of 1ns would result in turning data out of the card at 21ns (3ns before max t_{CAC} of 24ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	16	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	20	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	42	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	42	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	25	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	50	ns	1, 2

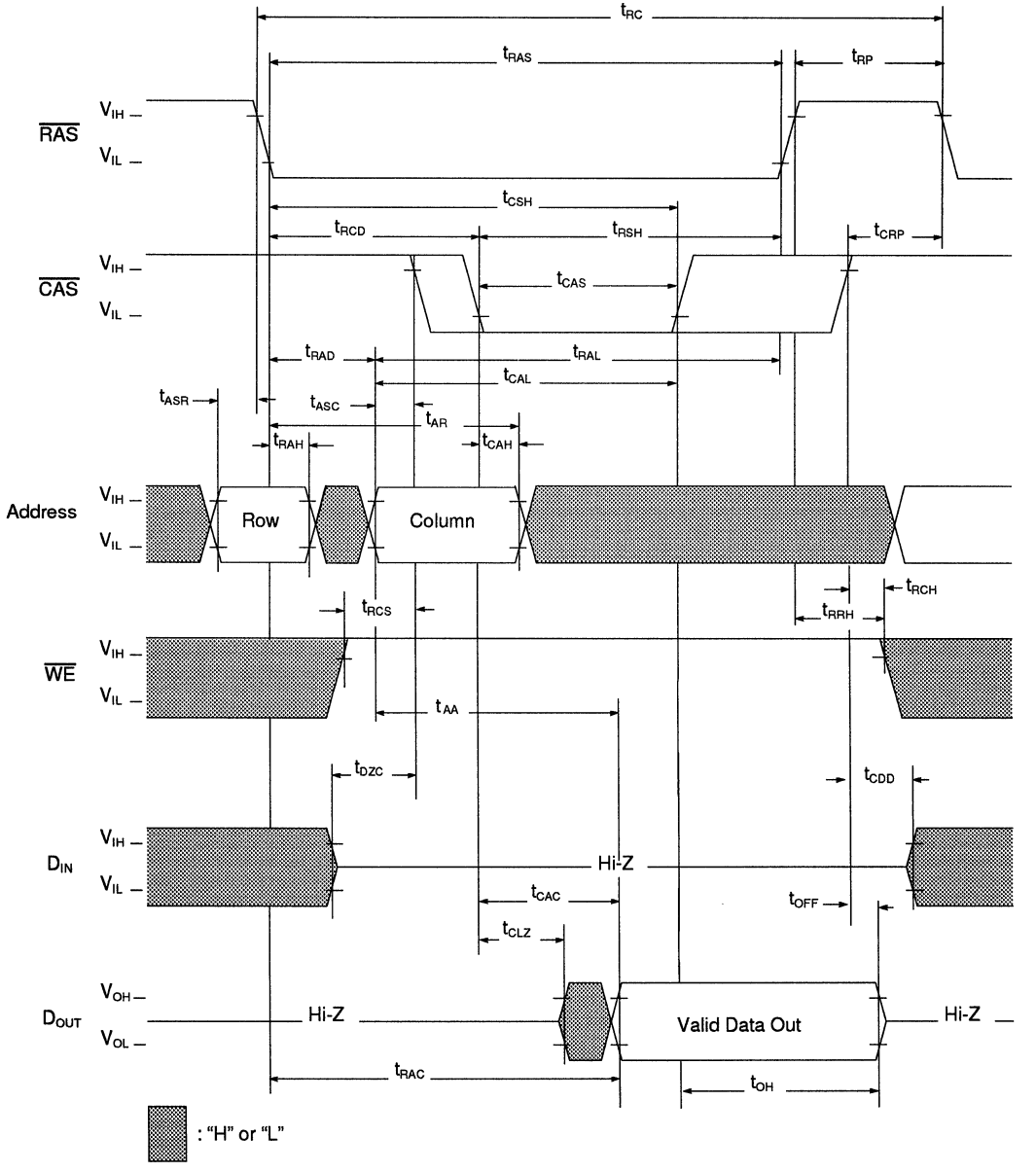
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

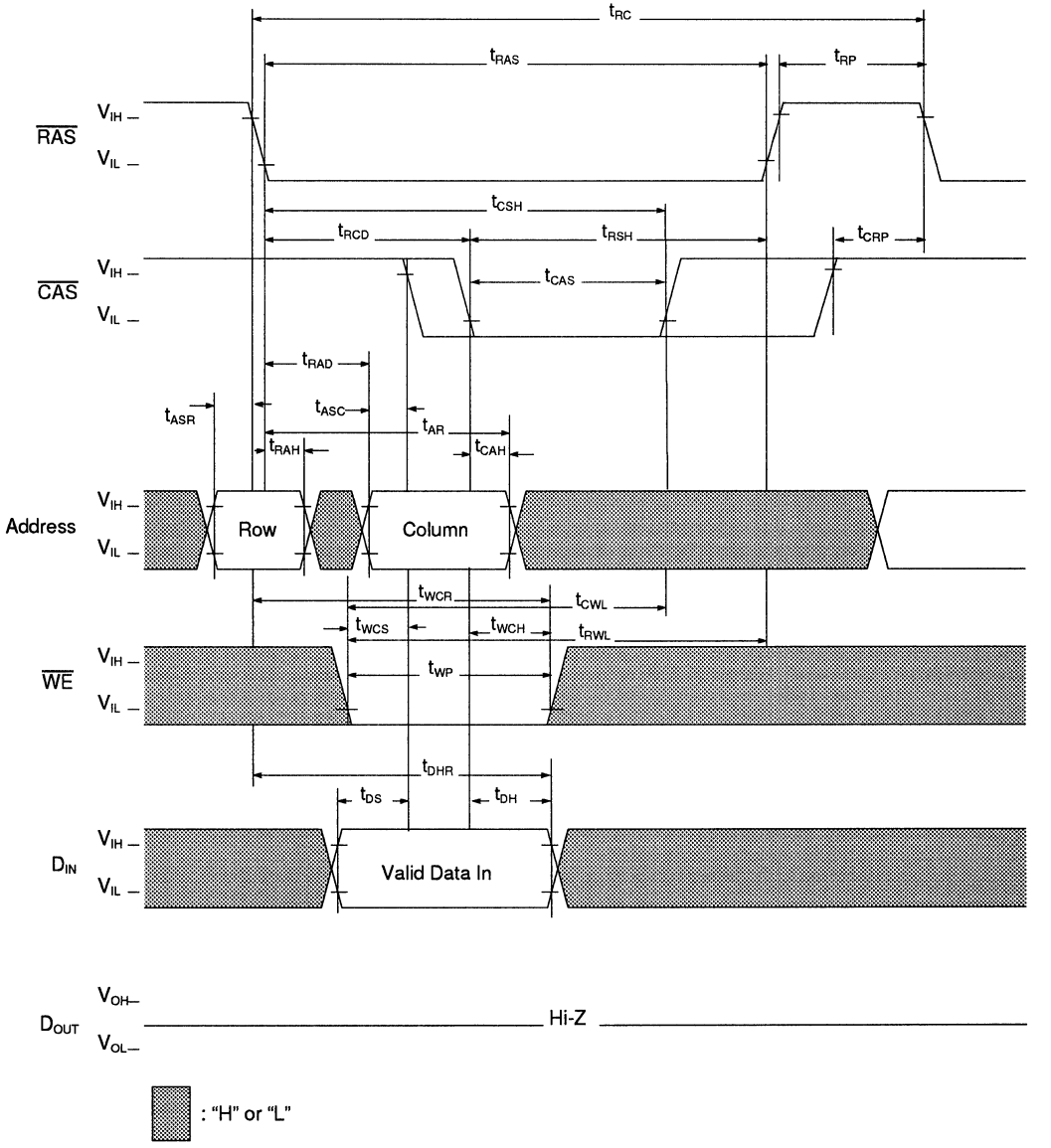
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	16	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	8	—	ns	
t_{REF}	Refresh Period	—	256	ns	1

1. 4096 refreshes are required every 256ms.

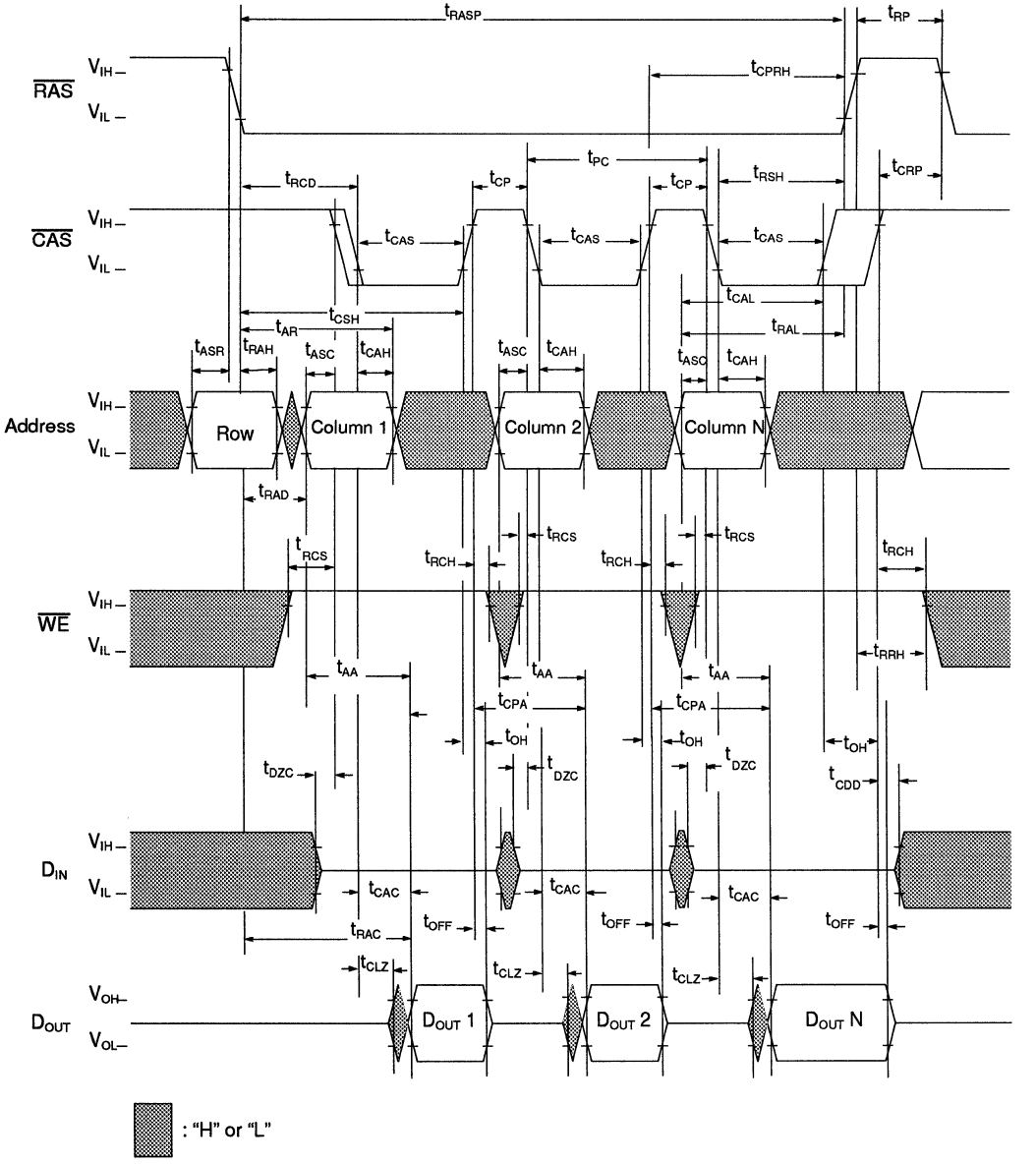
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

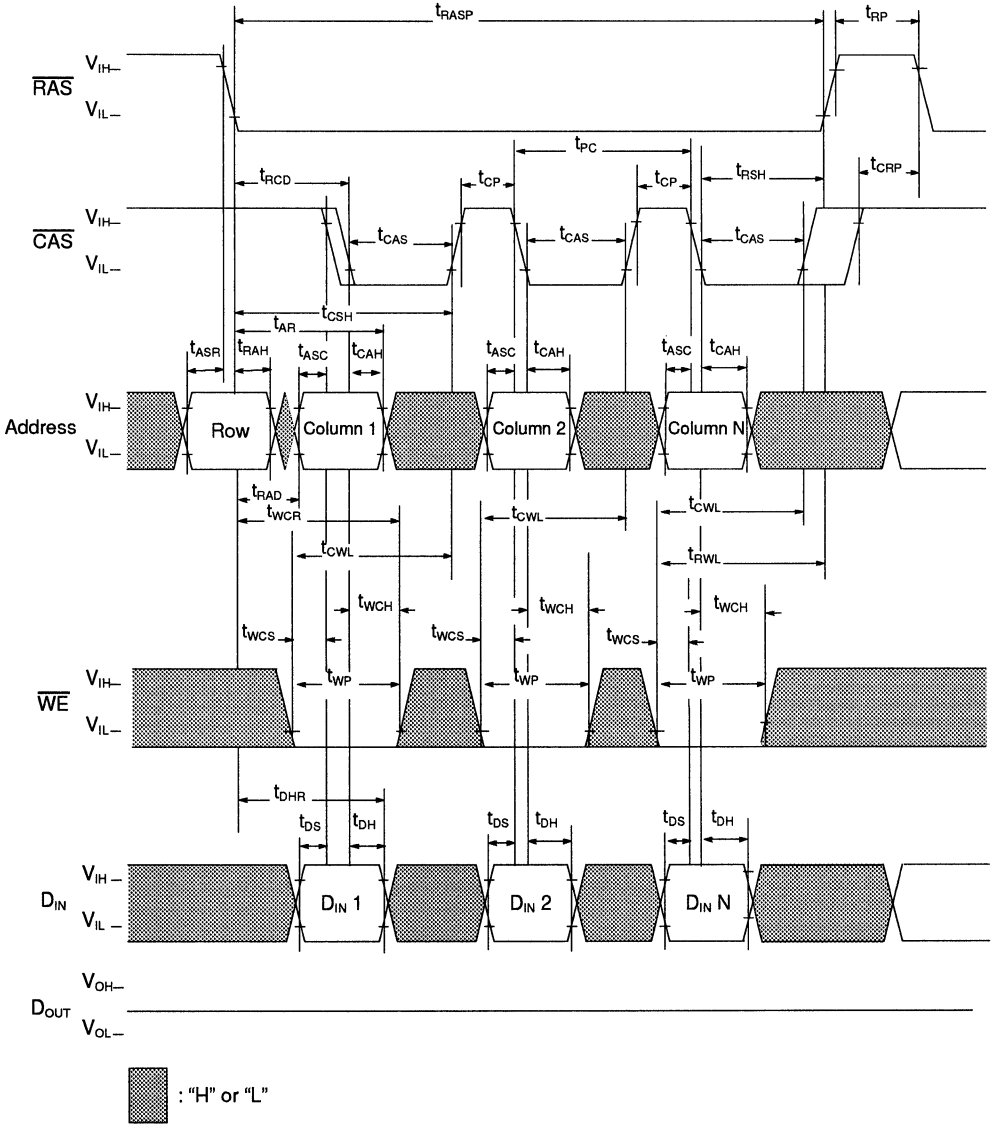
Write Cycle (Early Write)



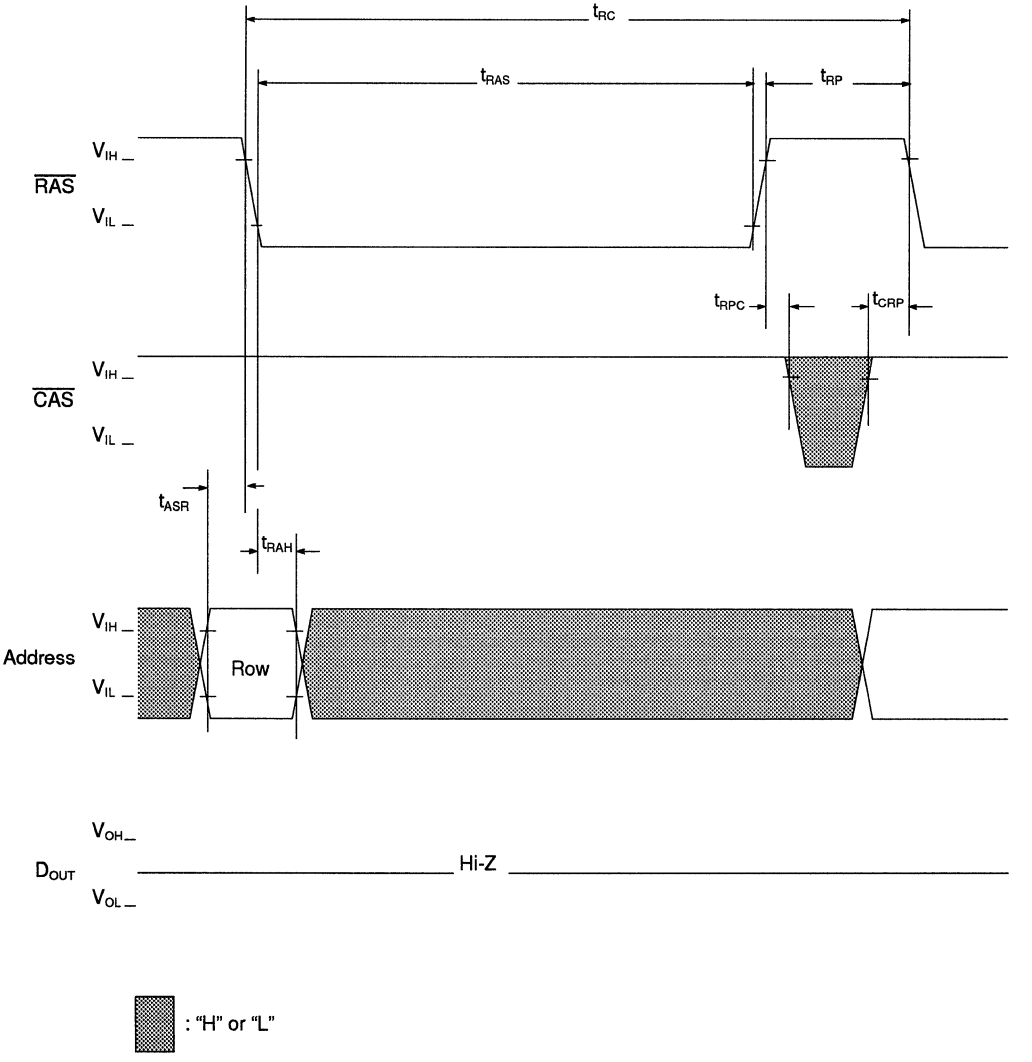
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

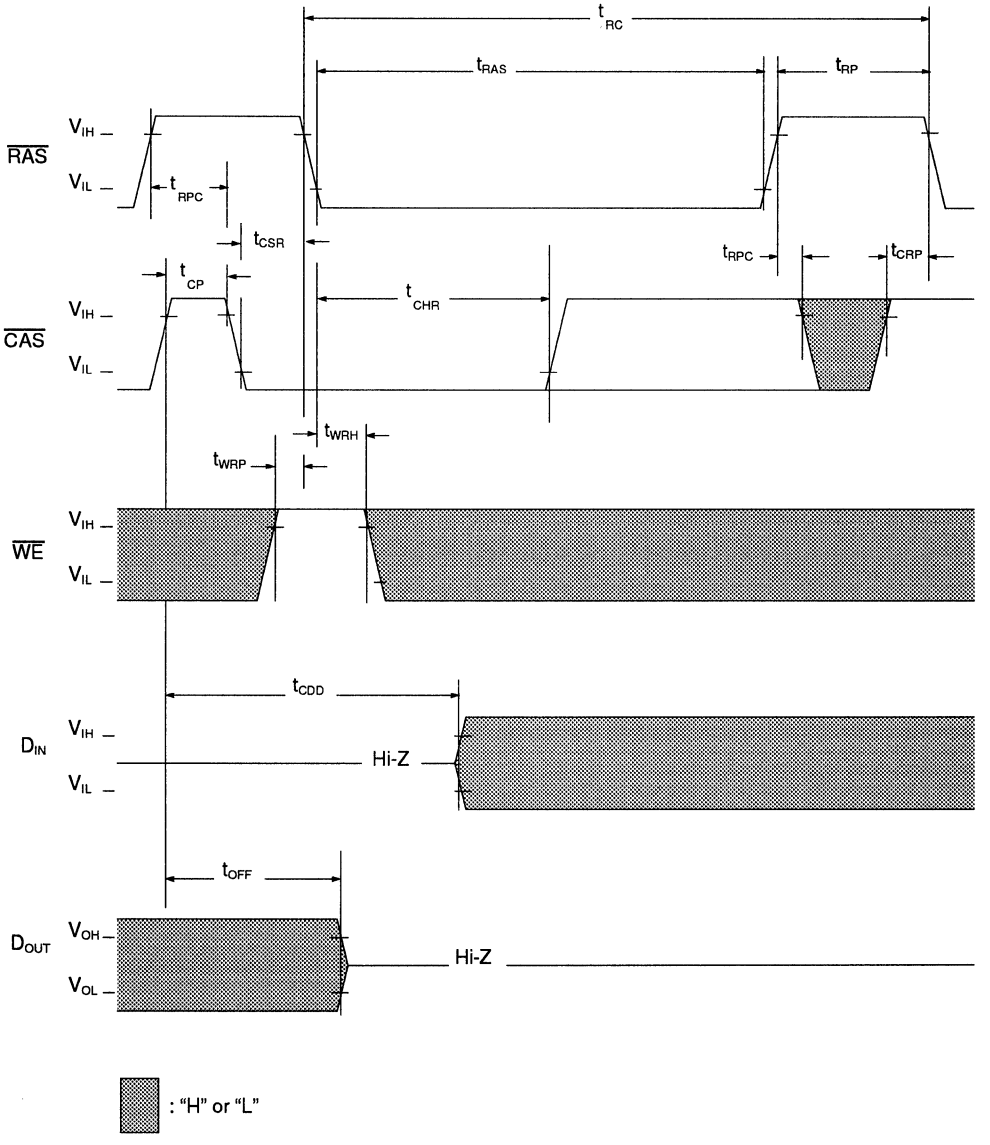


$\overline{\text{RAS}}$ Only Refresh Cycle



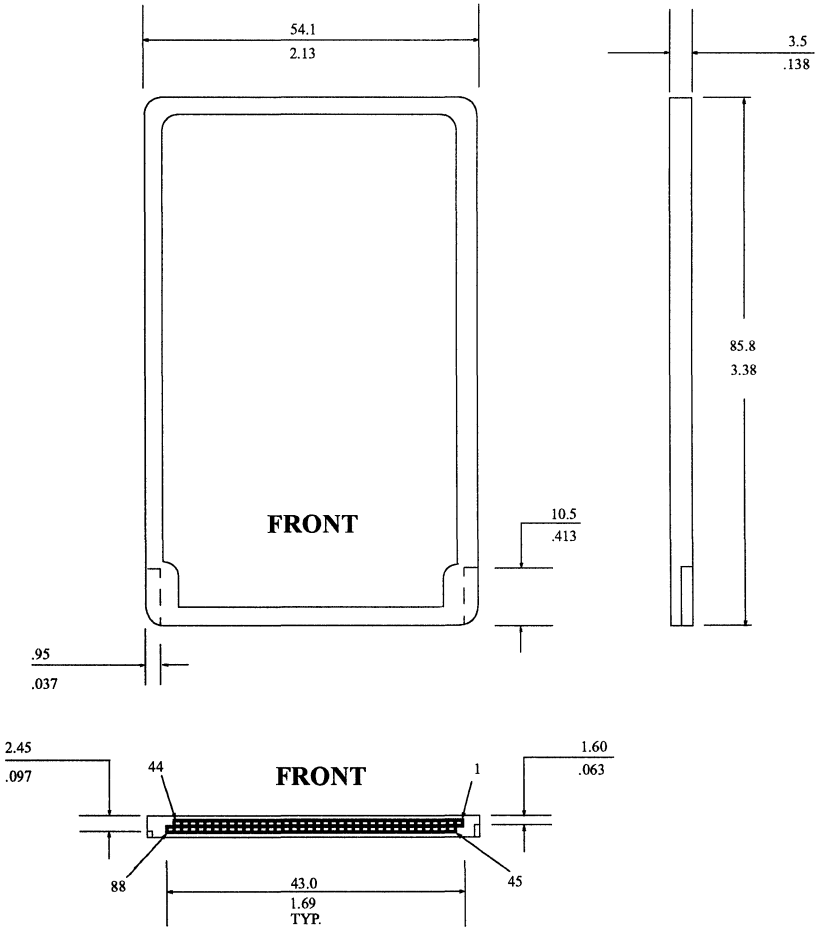
Note: $\overline{\text{WE}}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

1M x 36 5.0V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

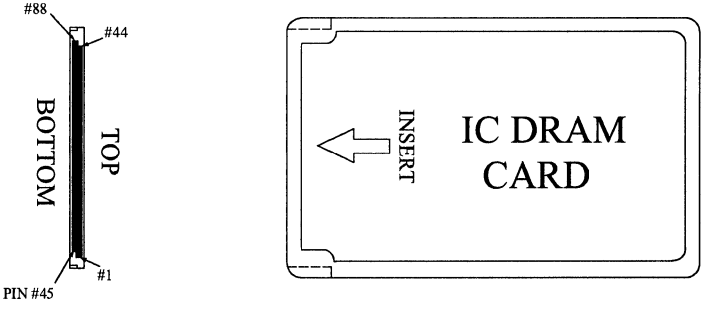
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	29ns
t_{AA}	Access Time From Address	46ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 5.0, ± 0.25V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x18 or x36 selectability
- 10/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 1024 refresh cycles distributed across 128ms
- Polarized Connector

Description

The IBM11J1360BL is a 4MB industry standard 88-pin IC DRAM card. It is organized as a 1M x 36 high speed memory array. It is built using 8 - 1M x 4, 4 - 1M x 1 devices and is compatible to the JEDEC/PCMCIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x36 configuration the memory is a single bank, having four unique bytes. The x18 configuration may be utilized as two banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other bank in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. The related 1M x 32 versions of these ICDRAM cards is IBM11J1320BLA.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

Pinout

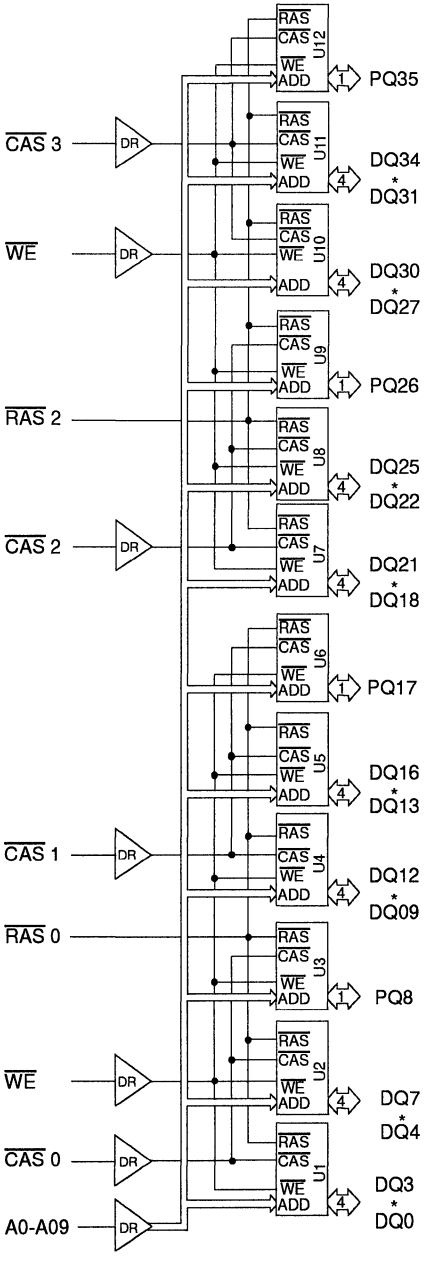
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	NC	47	DQ19	69	NC
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	V_{CC}	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	V_{CC}	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	PQ26	76	PD8
11	NC	33	PQ17	55	NC	77	NC
12	PQ8	34	DQ9	56	V_{SS}	78	NC
13	A0	35	NC	57	A1	79	PQ35
14	A2	36	DQ10	58	A3	80	DQ27
15	V_{CC}	37	V_{CC}	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	NC	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	NC	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	NC	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	NC	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

1. DQ numbering is compatible with parity (x36) version)

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J1360BLA-70	1M x 36	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	NC
PD3	V_{SS}
PD4	V_{SS}
PD5 (Number of Banks/Organization)	NC
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +6.0	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-1.0 to +6.0	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-1.0 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	4.2	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.4	—	V_{CC}+0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	57	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O1}$	Output Capacitance (DQ0~DQ34)	25	pF	
$C_{I/O2}$	Parity Output Capacitance (PQ8, PQ17, PQ26, PQ35)	30	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	1120	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	24	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	1120	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	1040	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	2.4	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	1120	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)		—	3.6	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 10ns ($\overline{CAS}$, $\overline{WE}$) or 11ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	11	—	ns	
t_{RAH}	Row Address Hold Time	10	—	ns	
t_{ASC}	Column Address Setup Time	3	—	ns	
t_{CAH}	Column Address Hold Time	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	42	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	24	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	29	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 19ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 21ns (7ns before max t_{CAC} of 28ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	15	—	ns	
t_{WP}	Write Command Pulse Width	16	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	25	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	29	ns	1, 2
t_{AA}	Access Time from Address	—	46	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	46	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	29	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	49	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	49	ns	1, 2

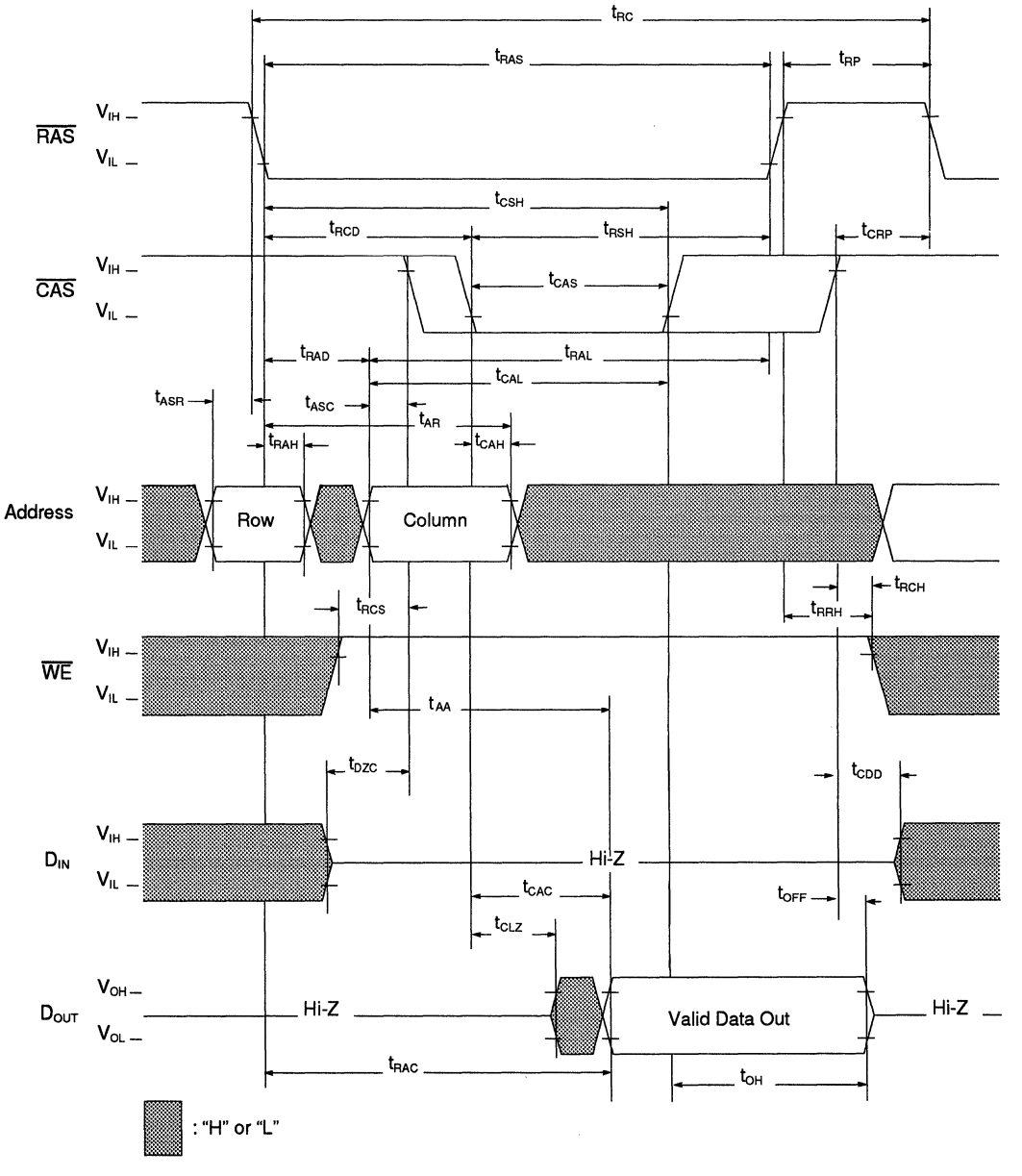
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	13	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	8	—	ns	
t_{REF}	Refresh Period	—	128	ms	1

1. 1024 refreshes are required every 128ms.

Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
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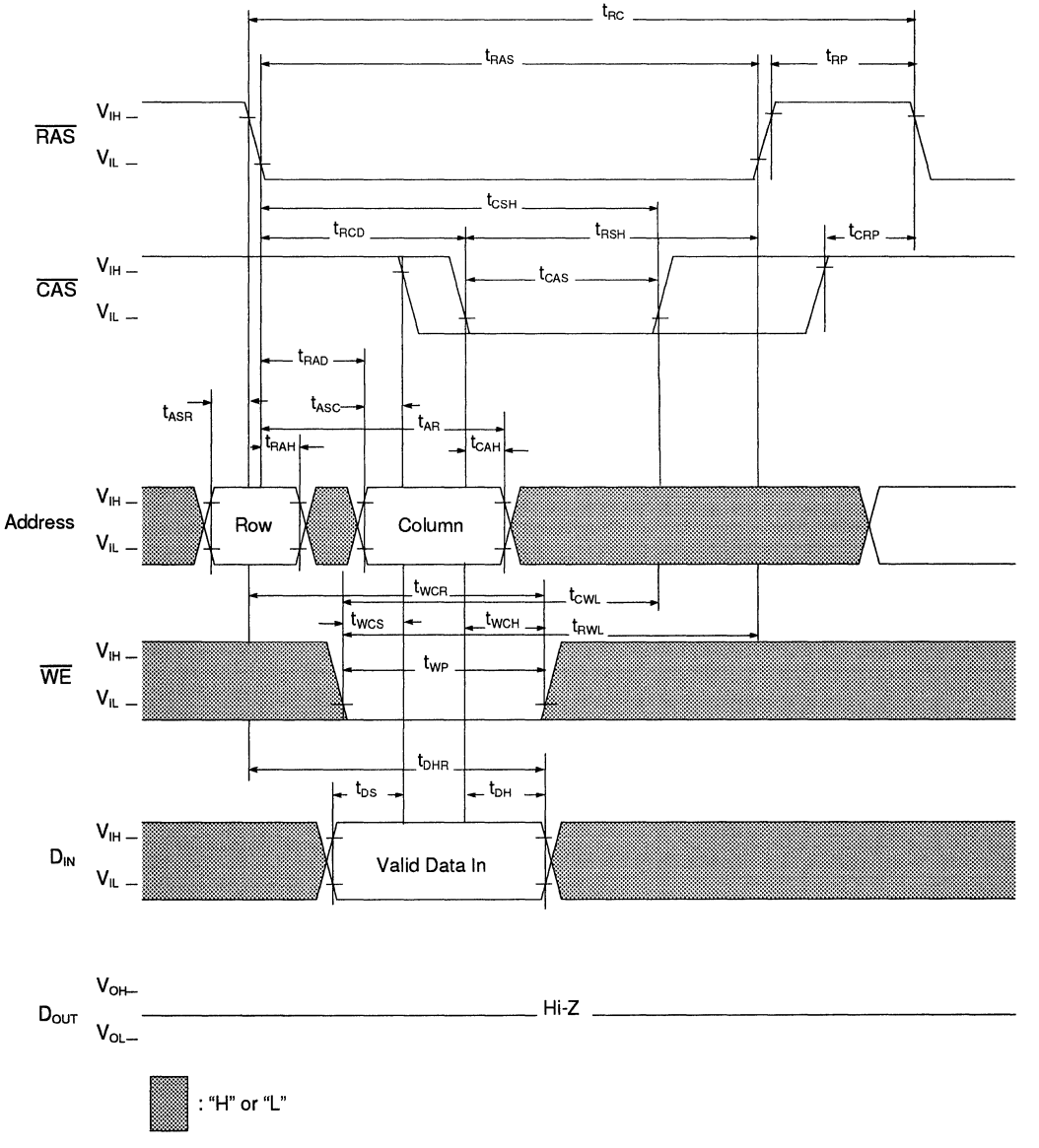
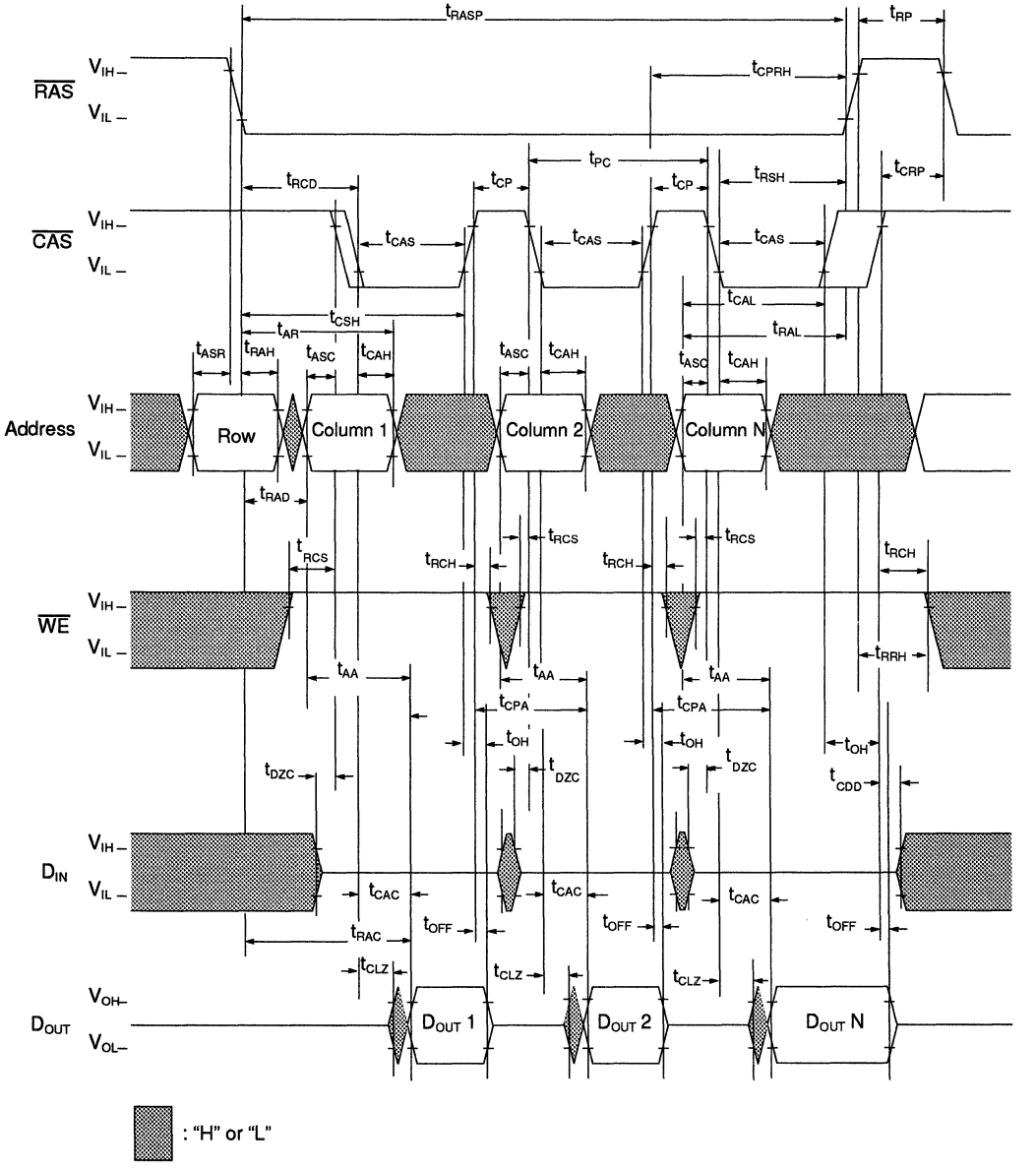
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

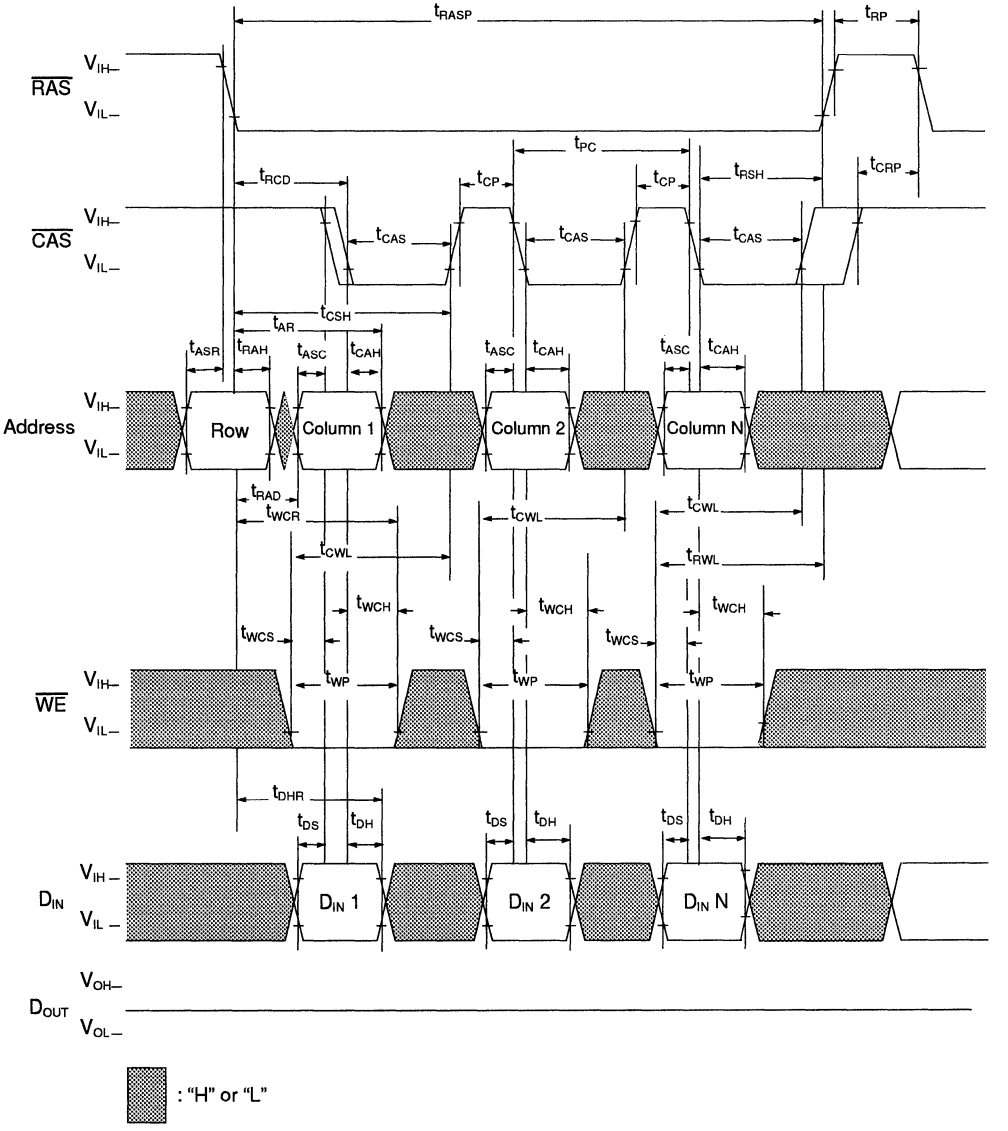
Write Cycle (Early Write)



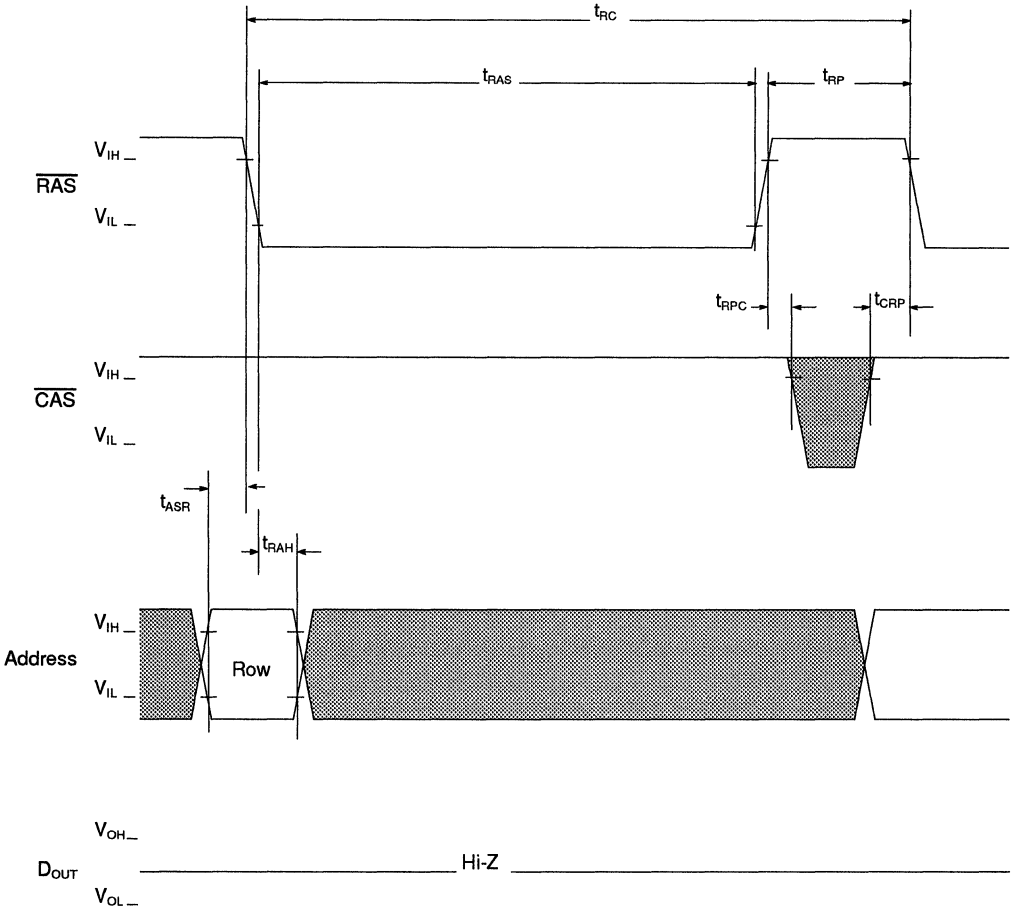
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

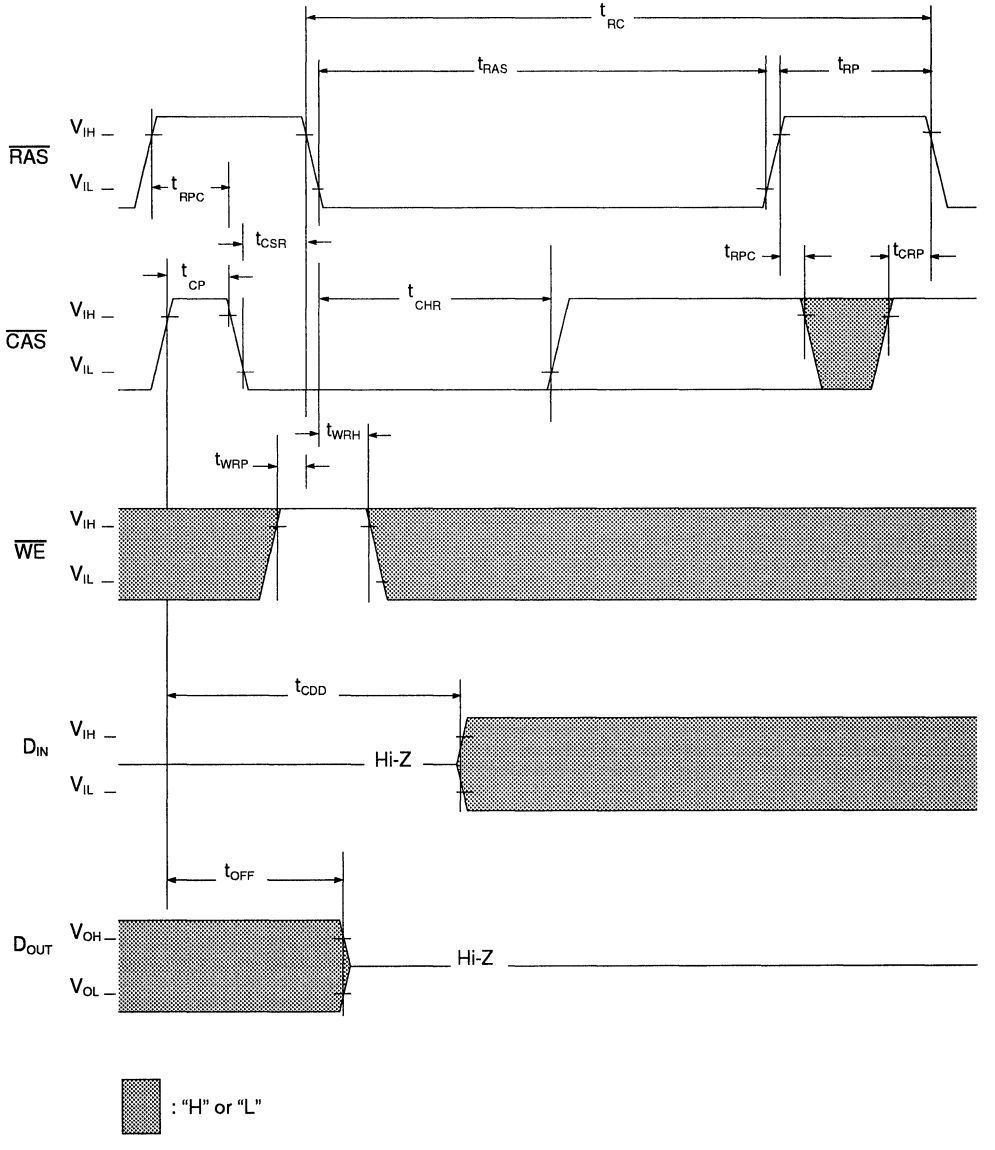


$\overline{RAS}$ Only Refresh Cycle



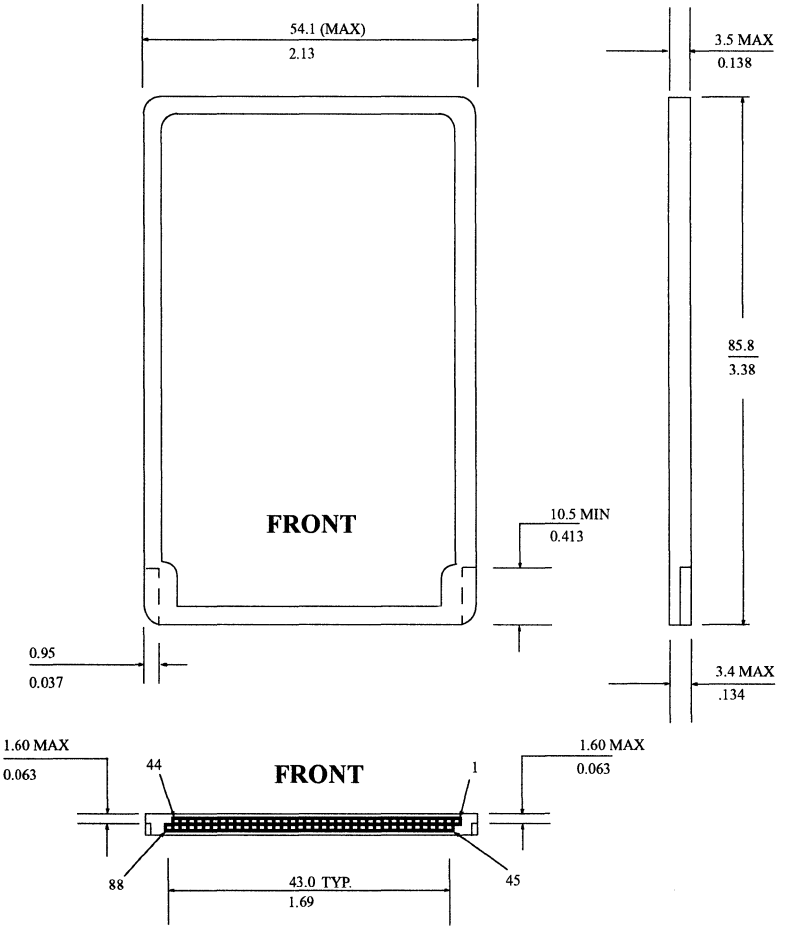
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

2M x 36 5.0V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

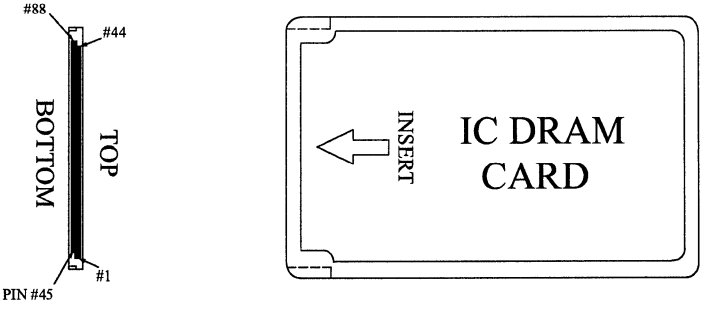
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	29ns
t_{AA}	Access Time From Address	46ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	50ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 5.0V, ± 0.25V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x18 or x36 selectability
- 10/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 1024 refresh cycles distributed across 128ms
- Polarized Connector

Description

The IBM11J2360BL is a 8MB industry standard 88-pin IC DRAM card. It is organized as a 2M x 36 high speed memory array. It is built using 16 - 1Mx4 devices, 8 - 1Mx1 devices and is compatible to the JEDEC/PCMCIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x36 configuration the memory may be utilized as two banks, each having four unique bytes. The x18 configuration may be utilized as four banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other banks in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. The related 2M x 32 version of this ICDRAM card is IBM11J2320BLA

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, PQ17, PQ26, PQ35	Parity Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

Pinout

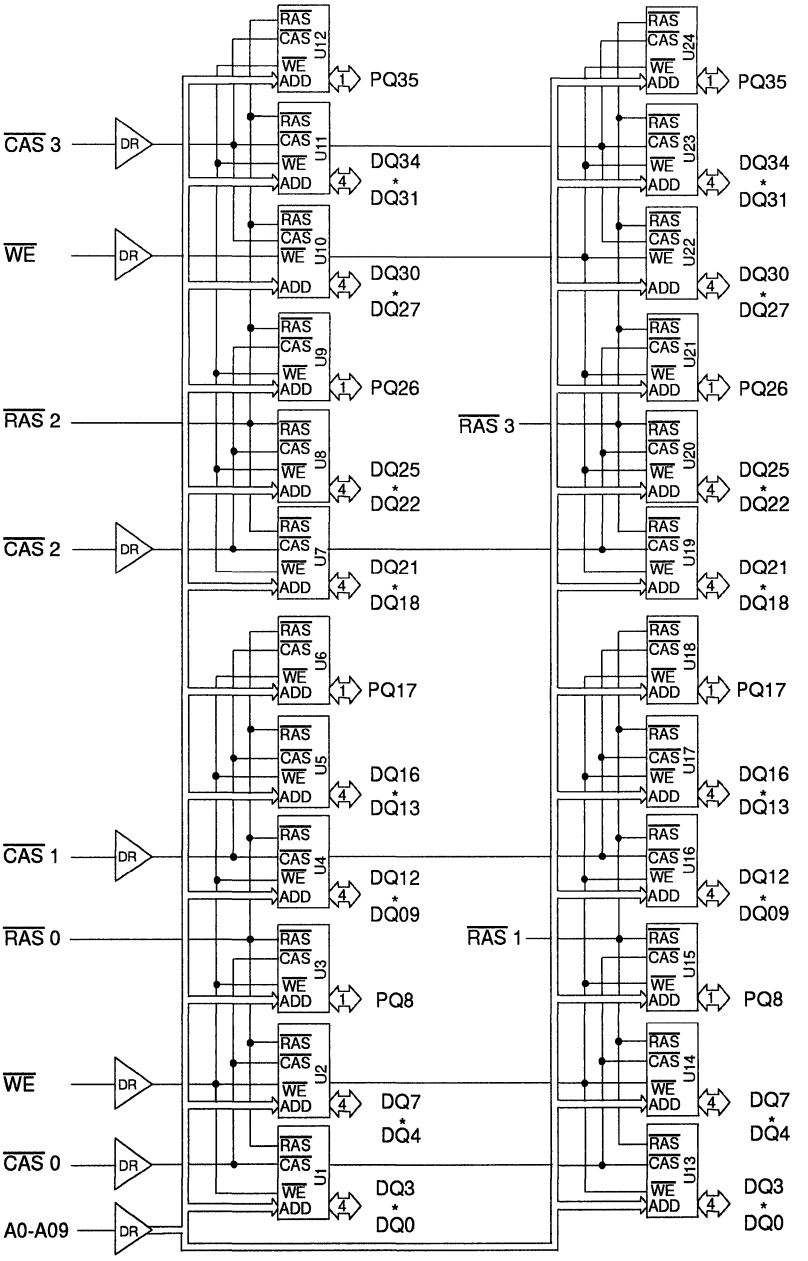
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	NC	47	DQ19	69	$\overline{RAS3}$
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	V_{CC}	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	V_{CC}	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	PQ26	76	PD8
11	NC	33	PQ17	55	NC	77	NC
12	PQ8	34	DQ9	56	V_{SS}	78	NC
13	A0	35	NC	57	A1	79	PQ35
14	A2	36	DQ10	58	A3	80	DQ27
15	V_{CC}	37	V_{CC}	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	NC	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	NC	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	NC	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	$\overline{RAS1}$	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

1. DQ numbering is compatible with non parity (x32) version)

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J2360BLA-70	2M x 36	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	NC
PD3	V_{SS}
PD4	V_{SS}
PD5 (Number of Banks/Organization)	V_{SS}
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +6.0	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-1.0 to +6.0	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-1.0 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	11.8	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.4	—	V_{CC} + 0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	57	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O1}$	Output Capacitance (DQ0~DQ34)	32	pF	
$C_{I/O2}$	Output Capacitance (PQ8, PQ17, PQ26, PQ35)	42	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	1120	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	48	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	1120	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	1040	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	4.8	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	1120	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			4.8	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 10ns ($\overline{CAS}$, $\overline{WE}$) or 11ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	11	—	ns	
t_{RAH}	Row Address Hold Time	10	—	ns	
t_{ASC}	Column Address Setup Time	3	—	ns	
t_{CAH}	Column Address Hold Time	17	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	42	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	24	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	29	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 21ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 23ns (6ns before max t_{CAC} of 29ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	15	—	ns	
t_{WP}	Write Command Pulse Width	16	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	25	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	29	ns	1, 2
t_{AA}	Access Time from Address	—	46	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	46	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	29	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	49	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	49	ns	1, 2

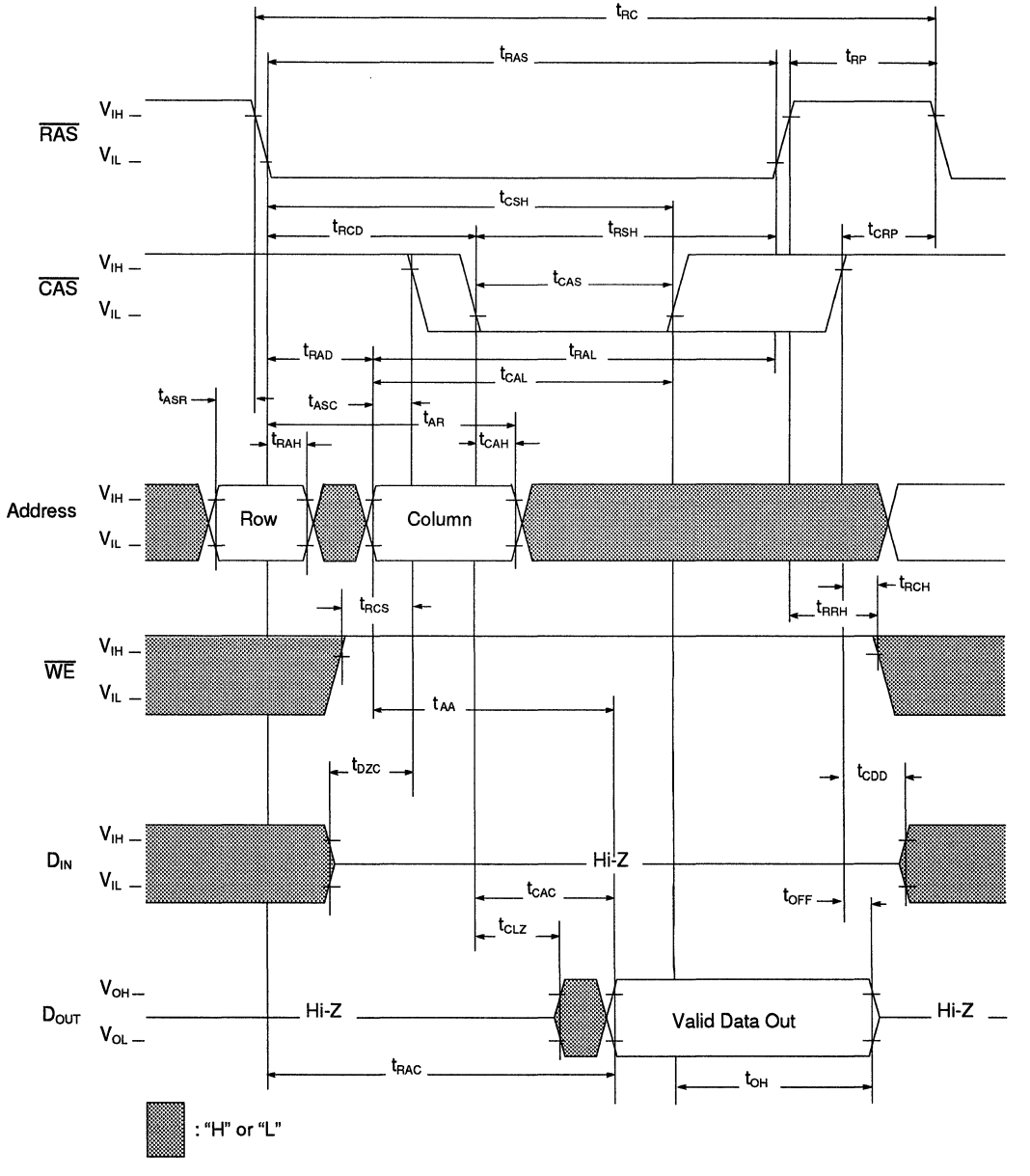
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

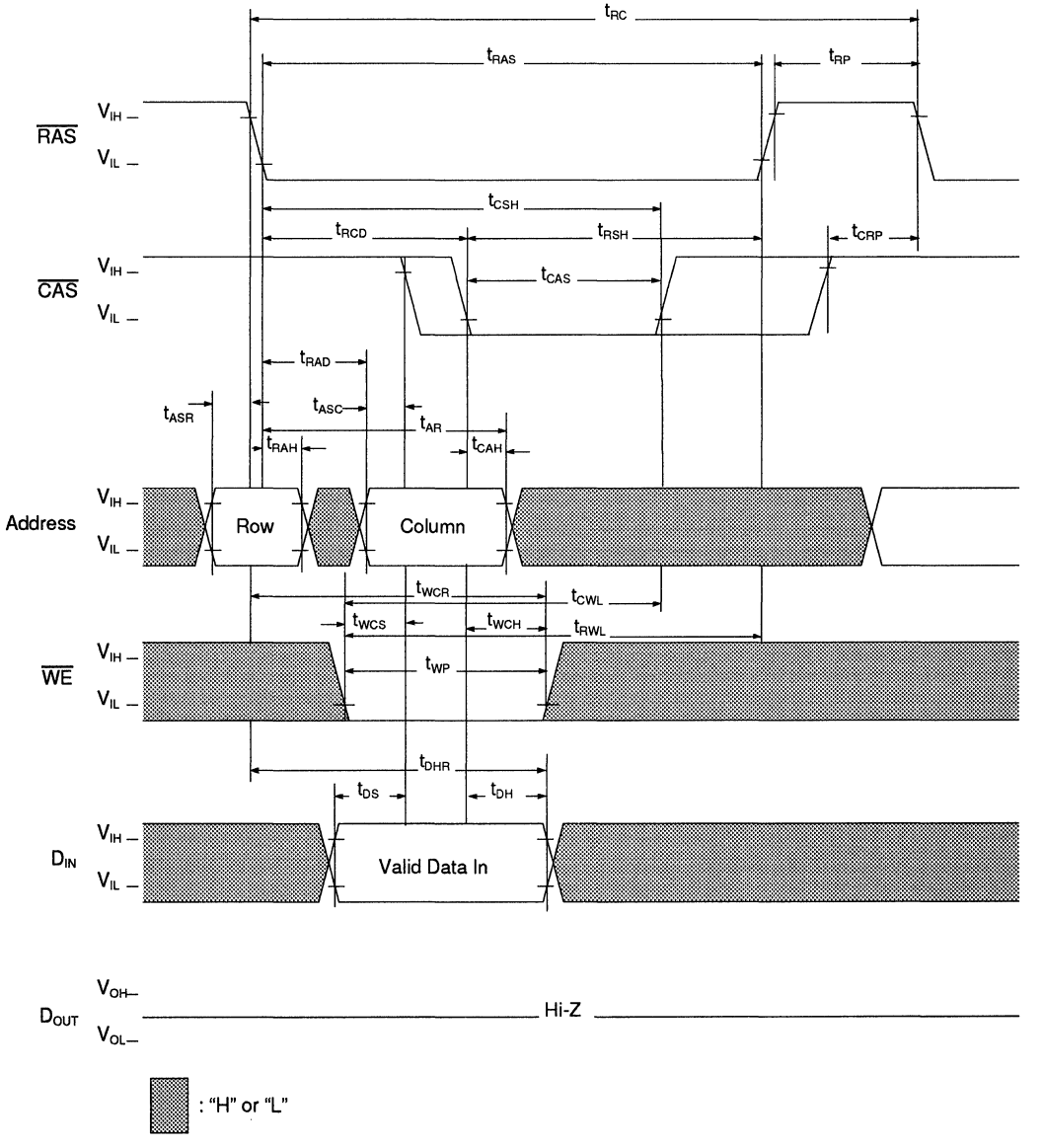
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	13	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	8	—	ns	
t_{REF}	Refresh Period	—	128	ms	1

1. 1024 refreshes are required every 128ms.

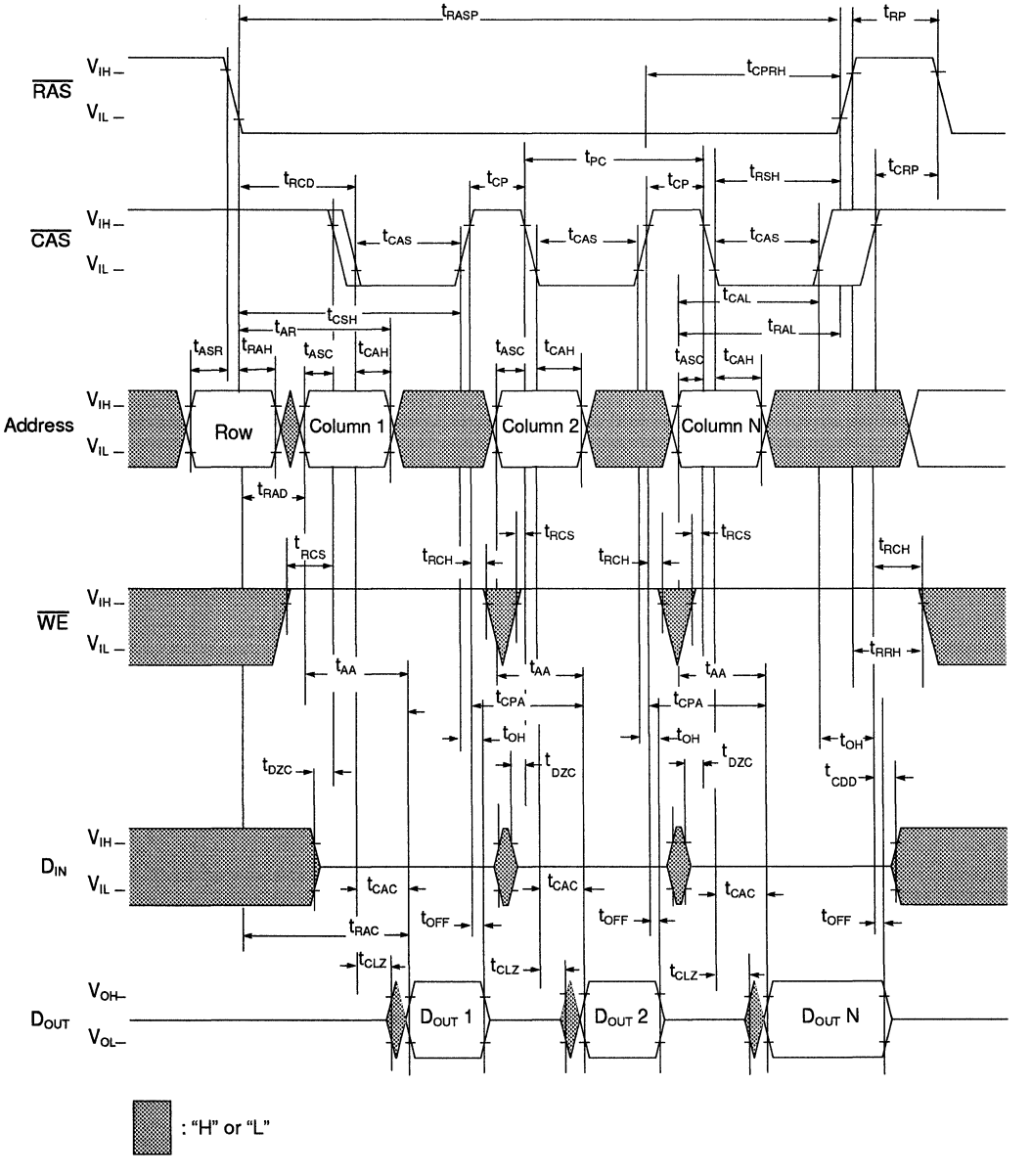
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

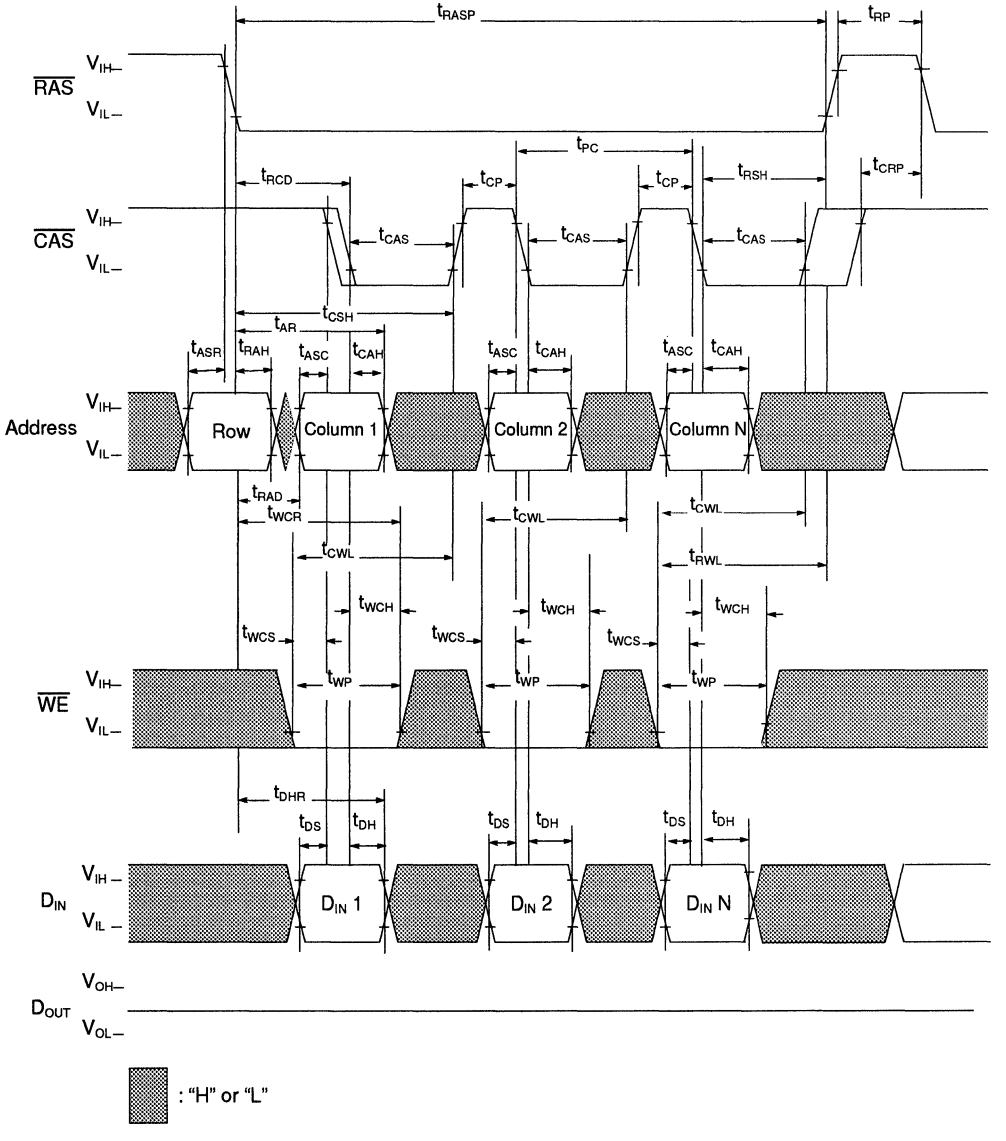
Write Cycle (Early Write)



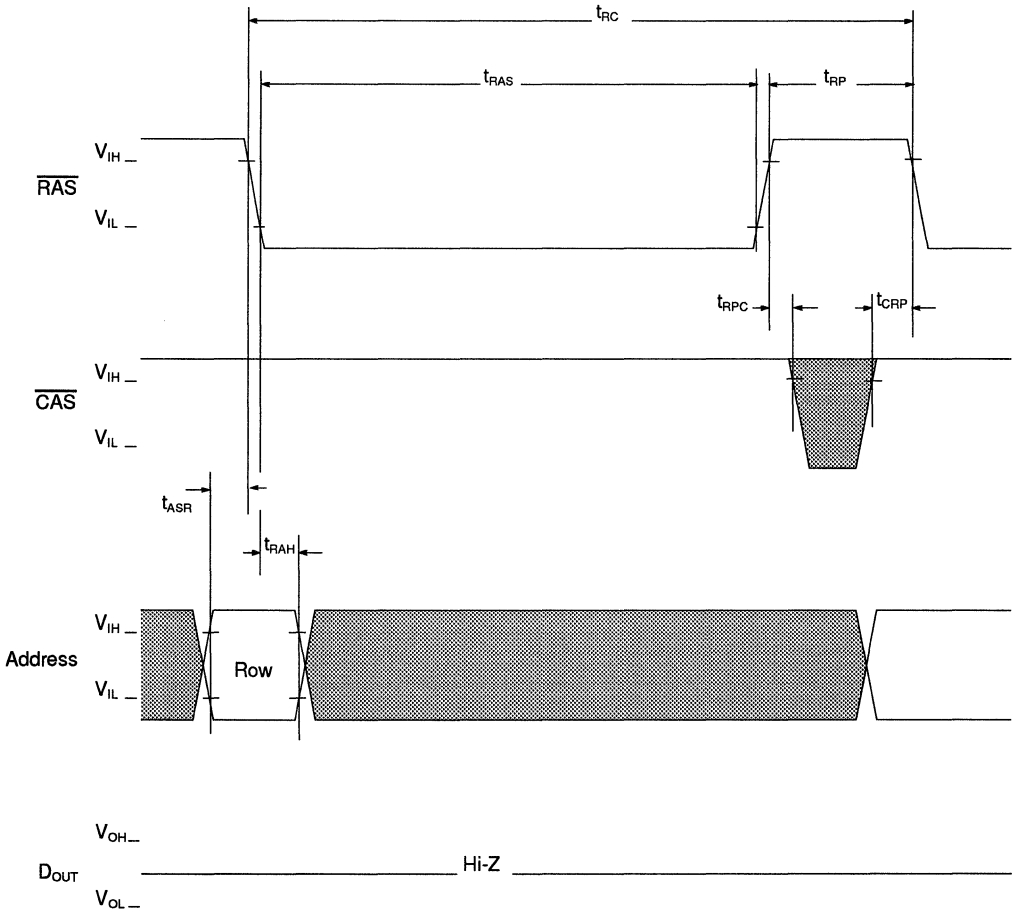
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

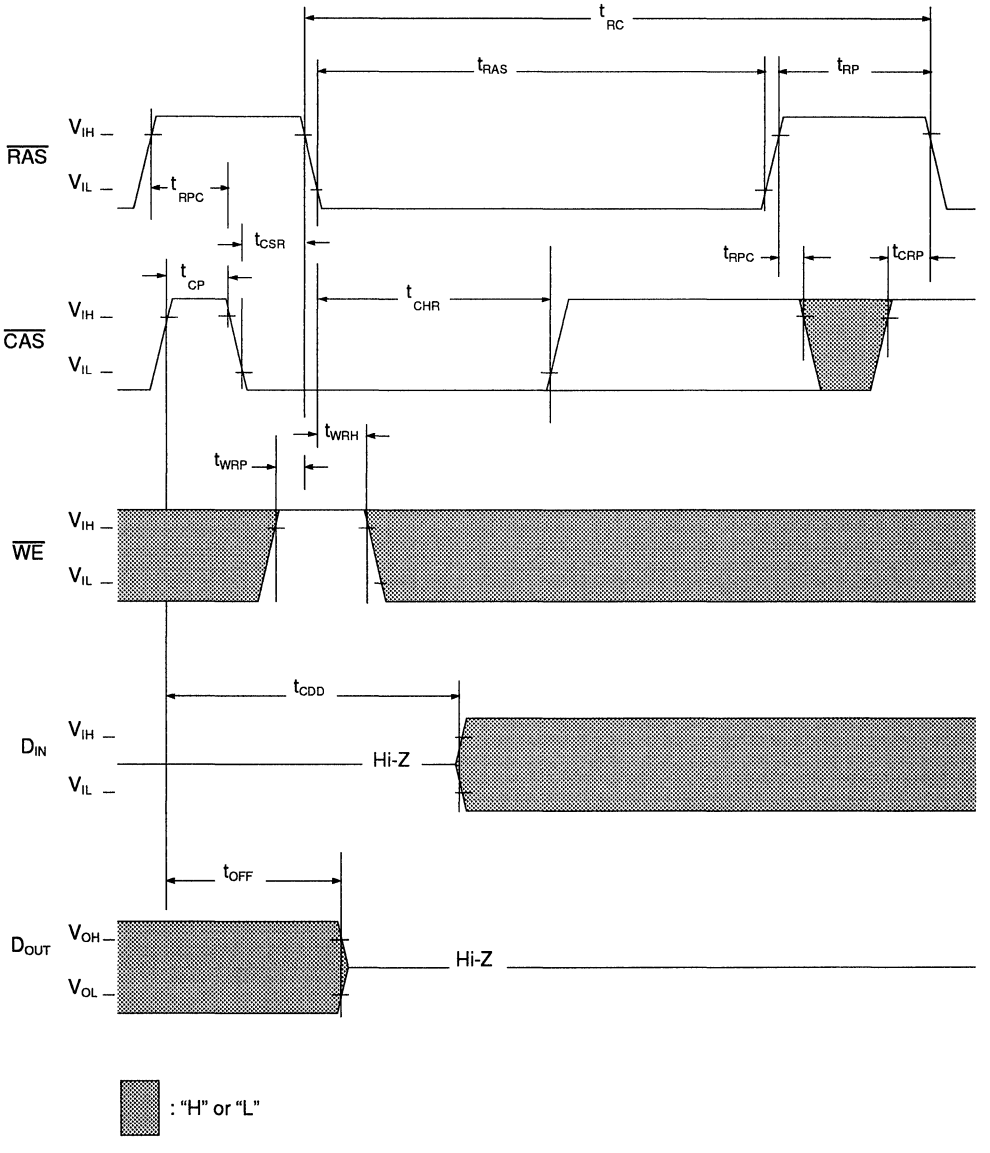


$\overline{RAS}$ Only Refresh Cycle



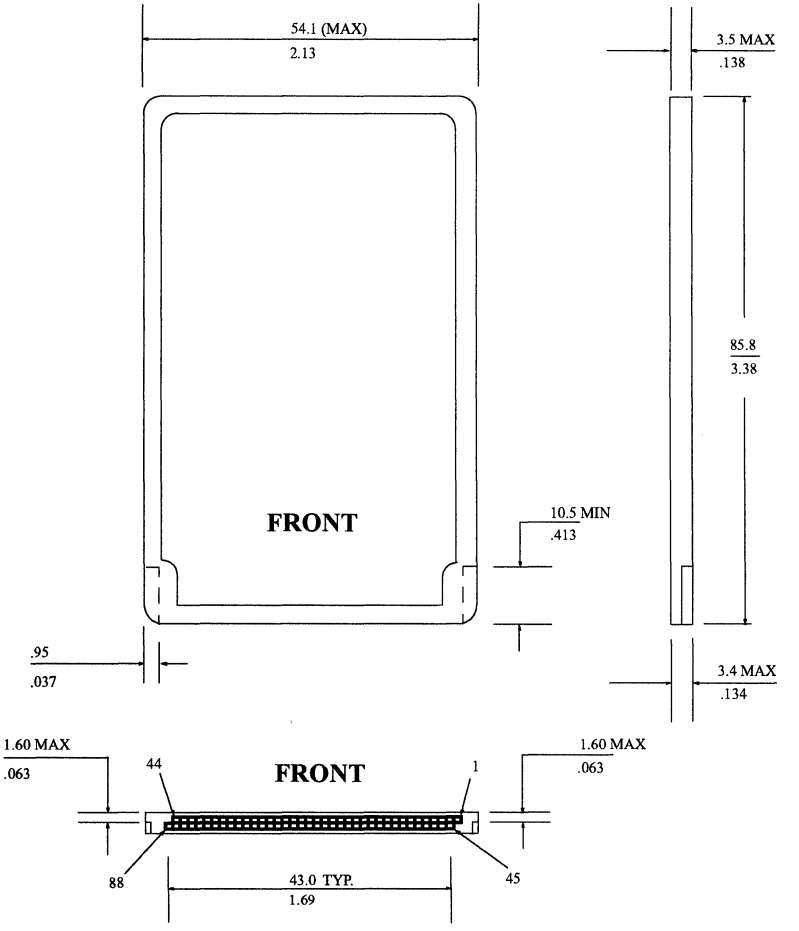
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

4M x 36 5.0V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

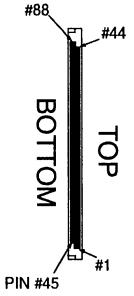
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns
t_{AA}	Access Time From Address	42ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

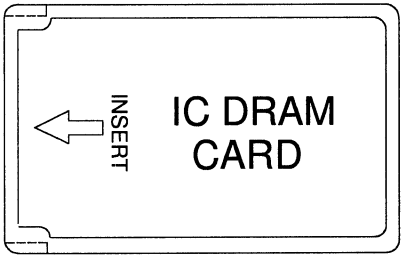
- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 5.0V, ± 0.25V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x18 or x36 selectability
- 11/11 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 2048 refresh cycles distributed across 256ms
- Polarized Connector

Description

The IBM11J4360BL is a 16MB industry standard 88-pin IC DRAM card. It is organized as a 4M x 36 high speed memory array. It is built using 8- 4Mx4 devices, 4- 4Mx1 devices and is compatible to the JEDEC/PCMCIA/JEIDA 88-pin standard. Each bit is uniquely addressed via 22 address bits. . Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x36 configuration the memory is a single bank, having four unique bytes. The x18 configuration may be utilized as two banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other banks in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. The related 4M x 32 version of this ICDRAM card is IBM11J4320BLA.

Card Outline





Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, PQ17, PQ26, PQ35	Parity Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

Pinout

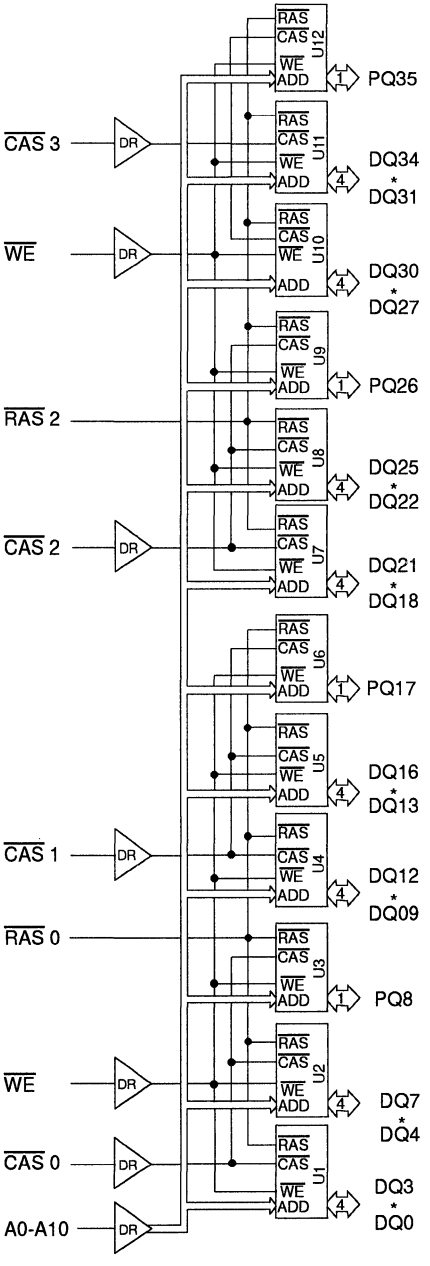
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	NC	47	DQ19	69	NC
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	V_{CC}	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	V_{CC}	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	PQ26	76	PD8
11	NC	33	PQ17	55	NC	77	NC
12	PQ8	34	DQ9	56	V_{SS}	78	NC
13	A0	35	NC	57	A1	79	PQ35
14	A2	36	DQ10	58	A3	80	DQ27
15	V_{CC}	37	V_{CC}	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	NC	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	NC	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	A10	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	NC	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

1. DQ numbering is compatible with non parity (x32) version)

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J4360BLA-70	4M x 36	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	V_{SS}
PD3	NC
PD4	V_{SS}
PD5 (Number of Banks/Organization)	NC
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +7.0	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to V_{CC} + 0.5, 7.0	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	10.8	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.4	—	V_{CC} + 0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	57	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O1}$	Output Capacitance (DQ0~DQ34)	25	pF	
$C_{I/O2}$	Output Capacitance (PQ8, PQ17, PQ26, PQ35)	30	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	1280	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	24	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	1280	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	1080	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	2.4	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	1280	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			3.6	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 10s ($\overline{CAS}$, $\overline{WE}$) or 11ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	7	—	ns	
t_{RAH}	Row Address Hold Time	8	—	ns	
t_{ASC}	Column Address Setup Time	2	—	ns	
t_{CAH}	Column Address Hold Time	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	28	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 21ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 23ns (6ns before max t_{CAC} of 29ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	16	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	20	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	42	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	42	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	25	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	50	ns	1, 2

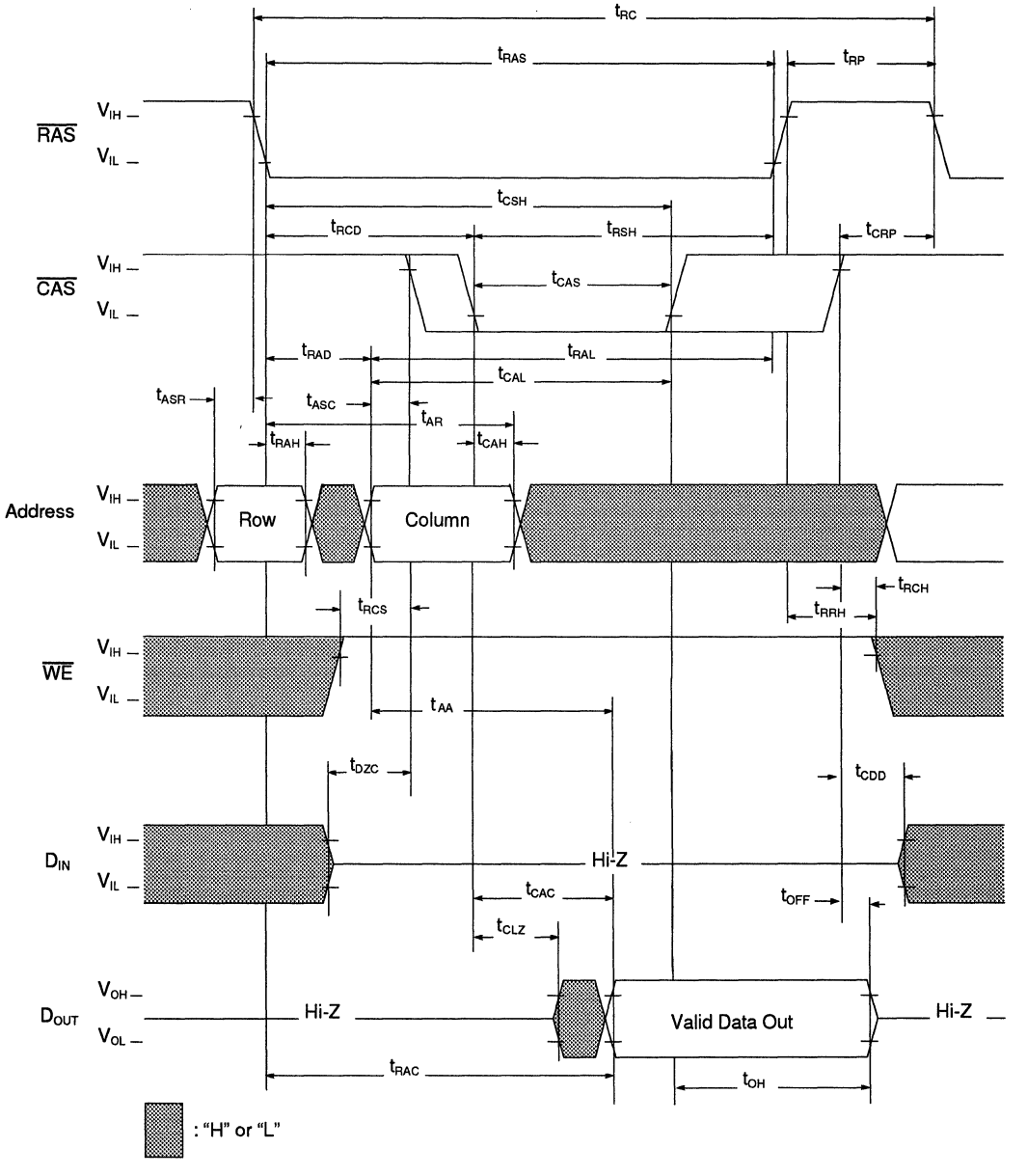
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

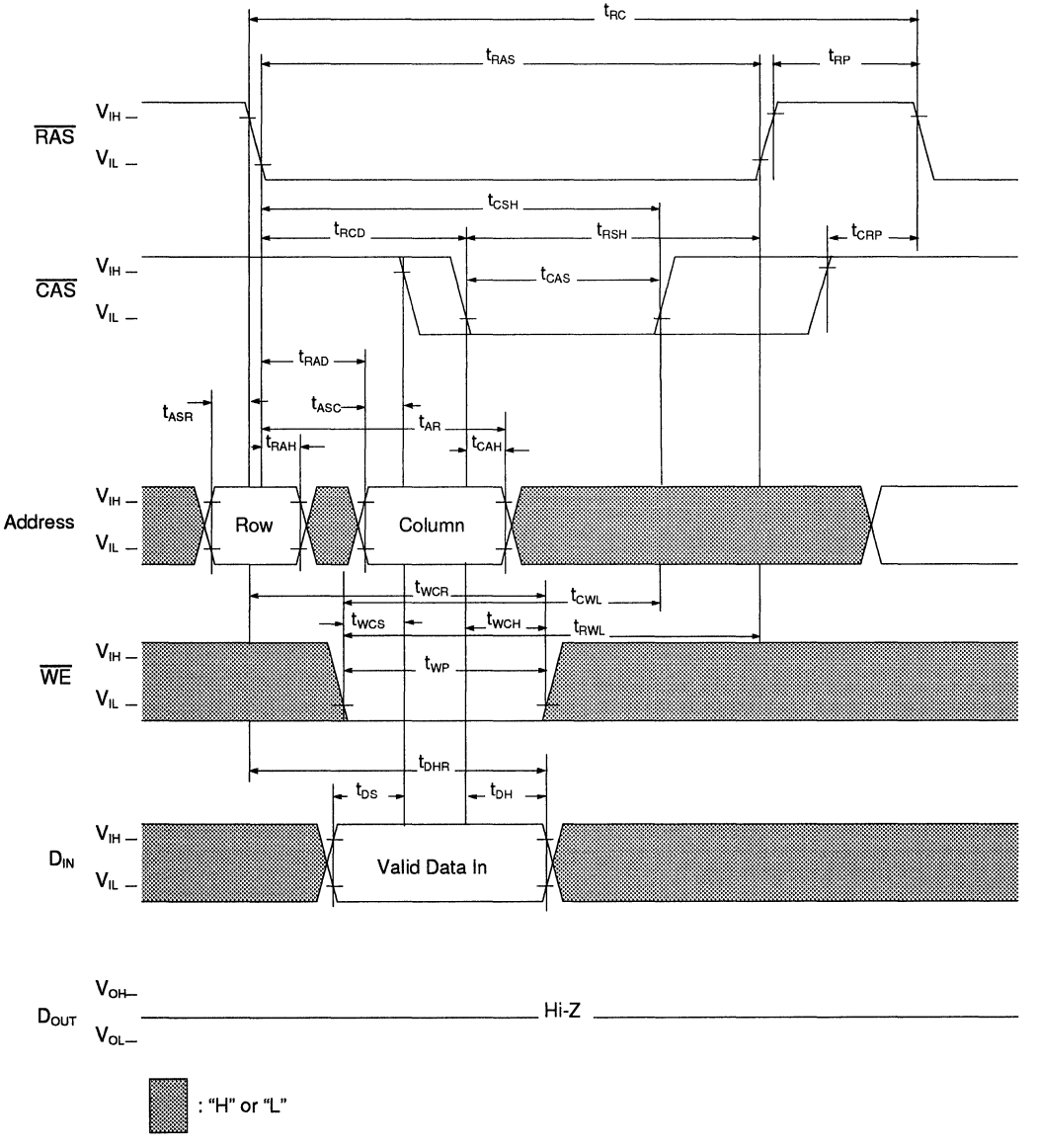
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	16	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	8	—	ns	
t_{REF}	Refresh Period	—	256	ns	1

1. 2048 refreshes are required every 256ms.

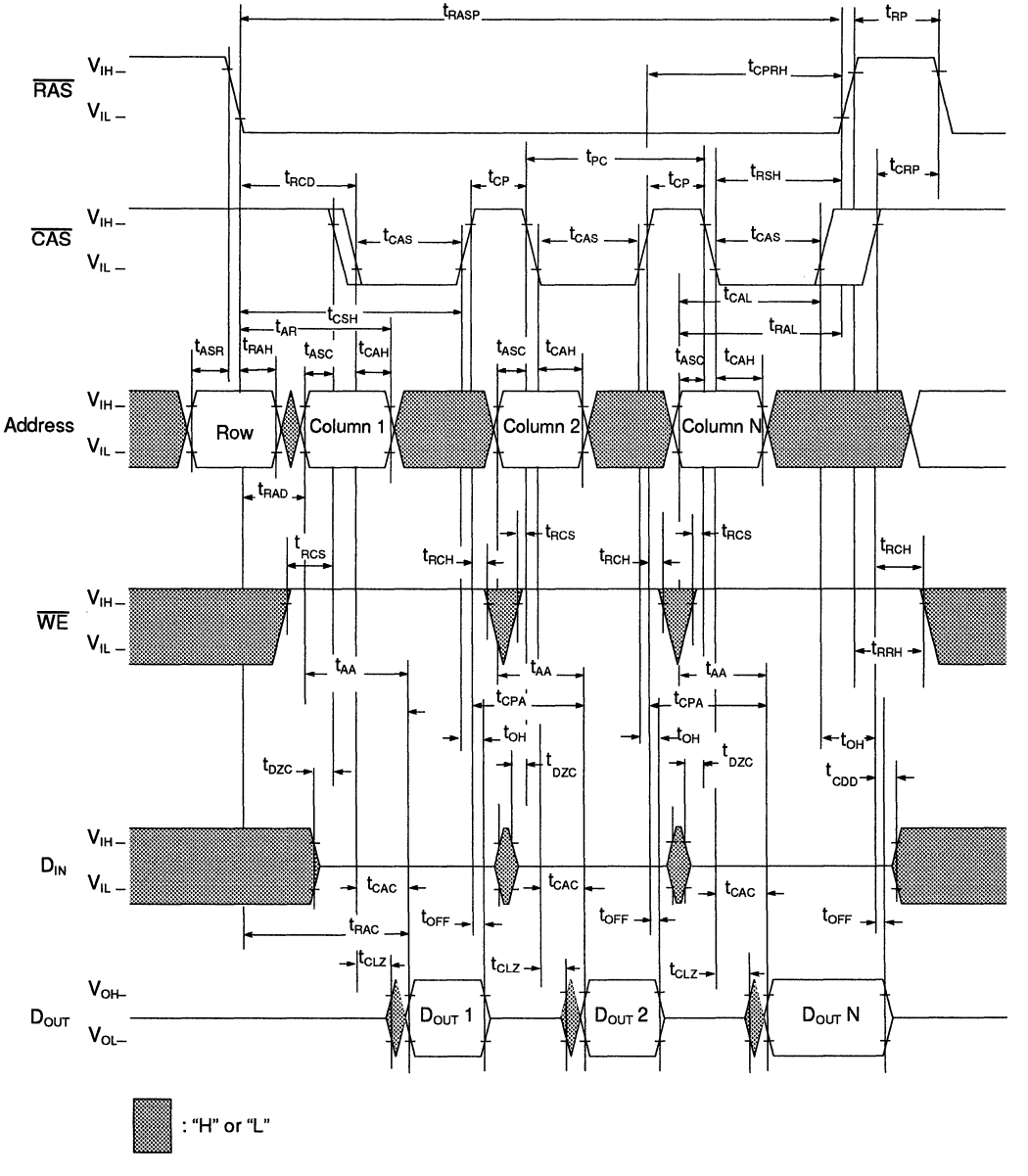
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

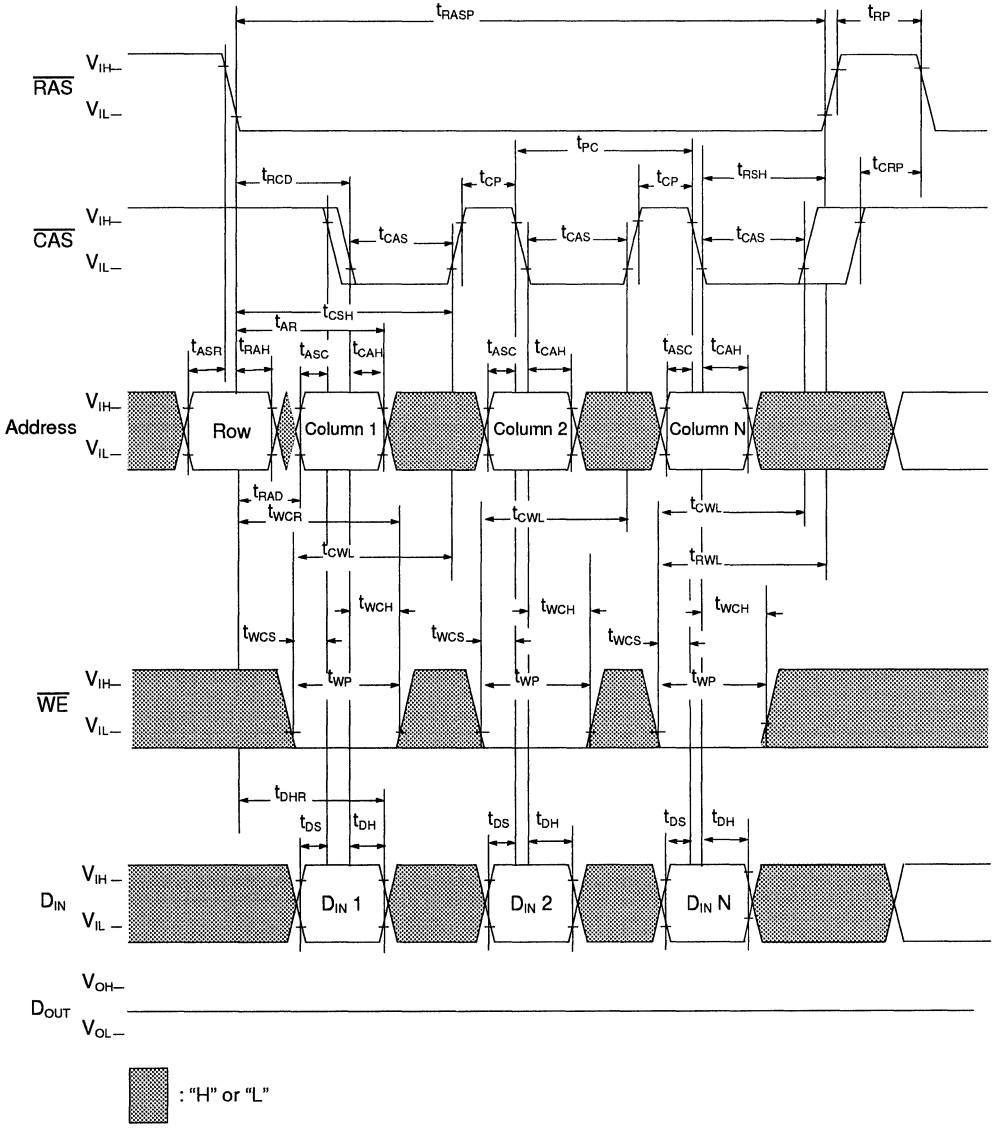
Write Cycle (Early Write)



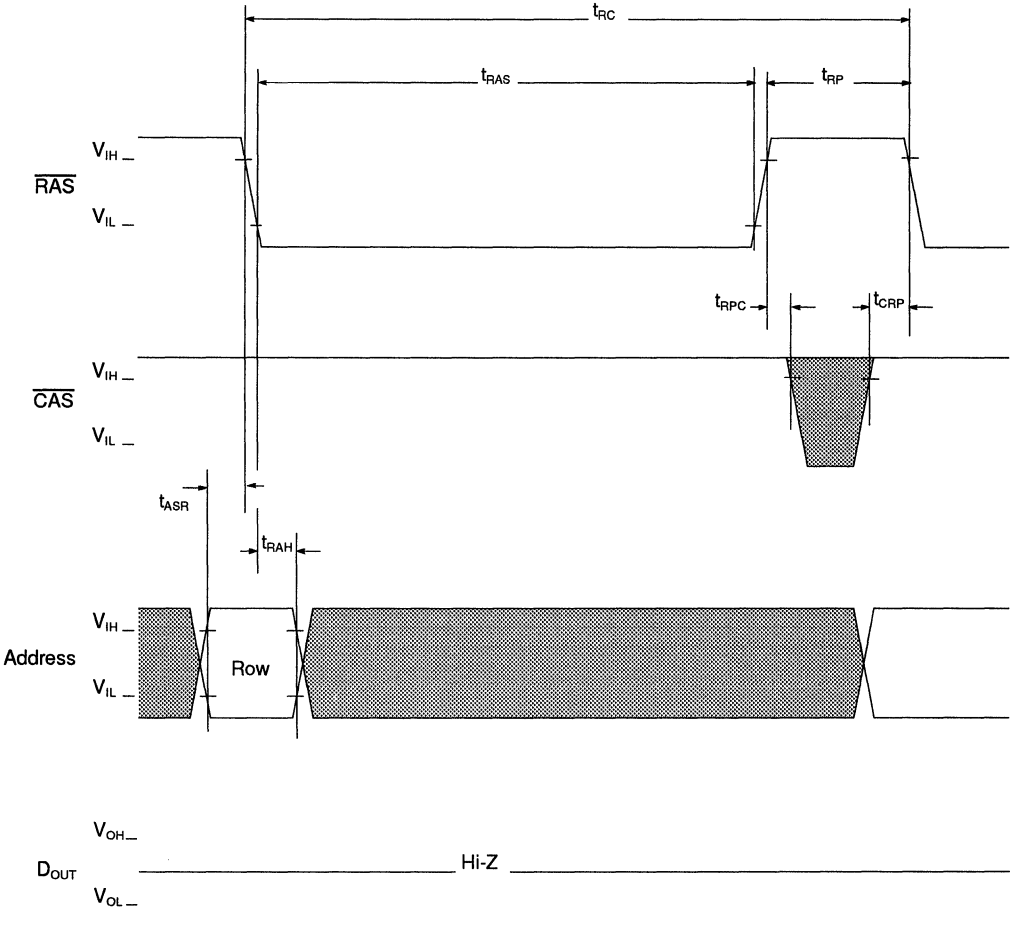
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



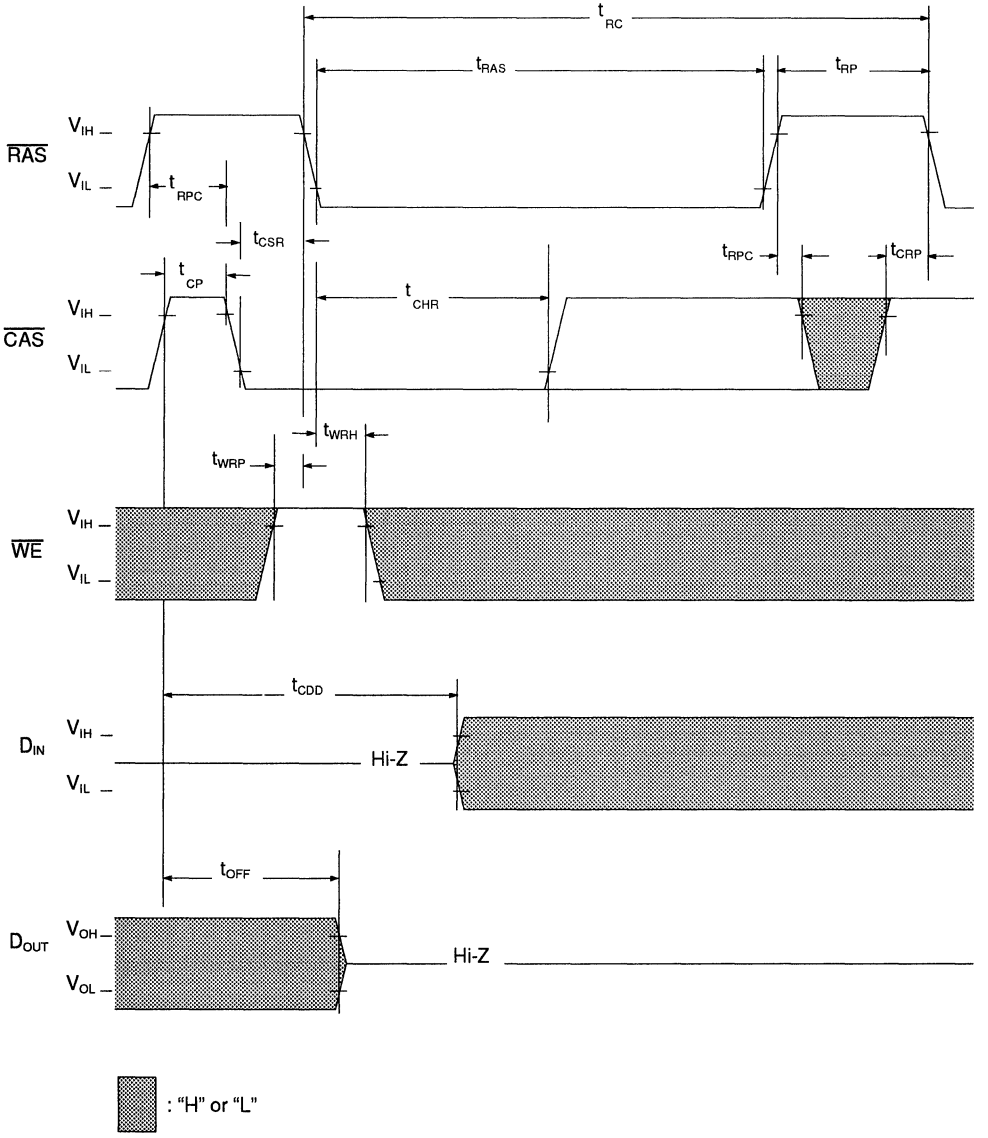
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

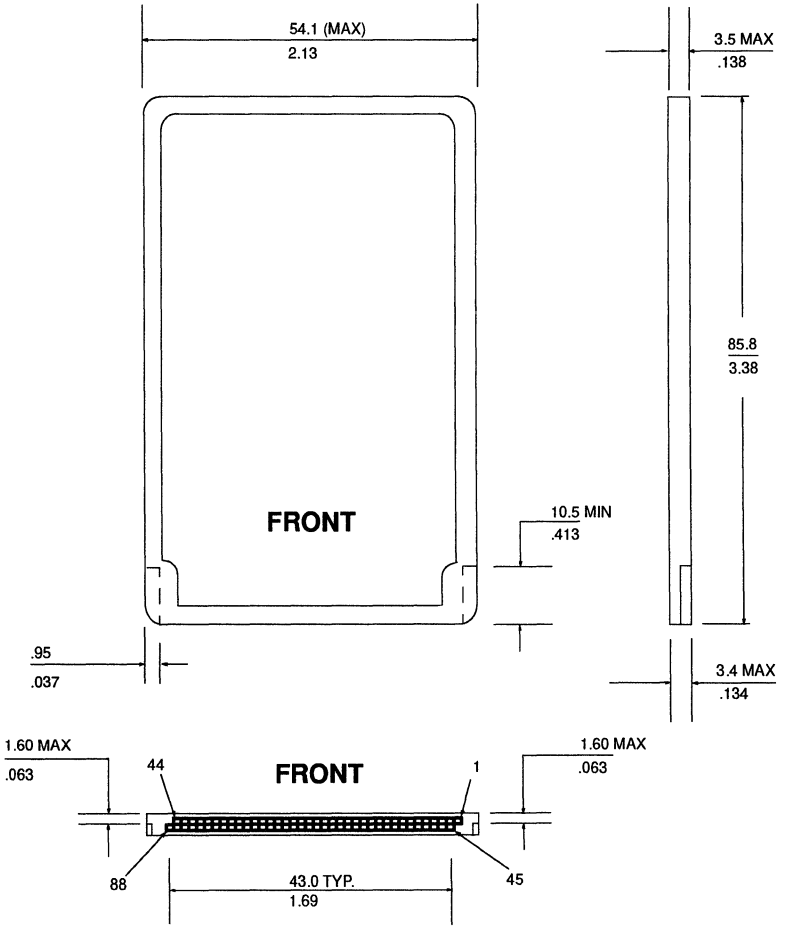
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

4M x 36 5.0V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

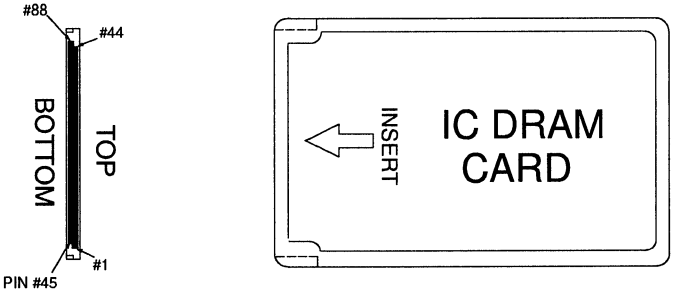
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns
t_{AA}	Access Time From Address	42ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 5.0V, ± 0.25V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x18 or x36 selectability
- 12/11 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 4096 refresh cycles distributed across 256ms
- Polarized Connector

Description

The IBM11J4360DL is a 16MB industry standard 88-pin IC DRAM card. It is organized as a 4M x 36 high speed memory array. It is built using 8- 4Mx4 devices, 4- 4Mx1 devices and is compatible to the JEDEC/PCMCIA/JEIDA 88-pin standard. Each bit is uniquely addressed via 22 address bits. The x4 Drams require 12 ROW/10 COLUMN addresses and the x1 DRAMS require 11ROW/11 COLUMN addresses. The highest order ROW addresses must be sent as the highest order COLUMN address to satisfy both DRAM requirements. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x36 configuration the memoryis a single bank, each having four unique bytes. The x18 configuration may be utilized as twobanks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other banks in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. The related 4M x 32 version of this ICDRAM card is IBM11J4320DLA

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A11	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, PQ17, PQ26, PQ35	Parity Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

Pinout

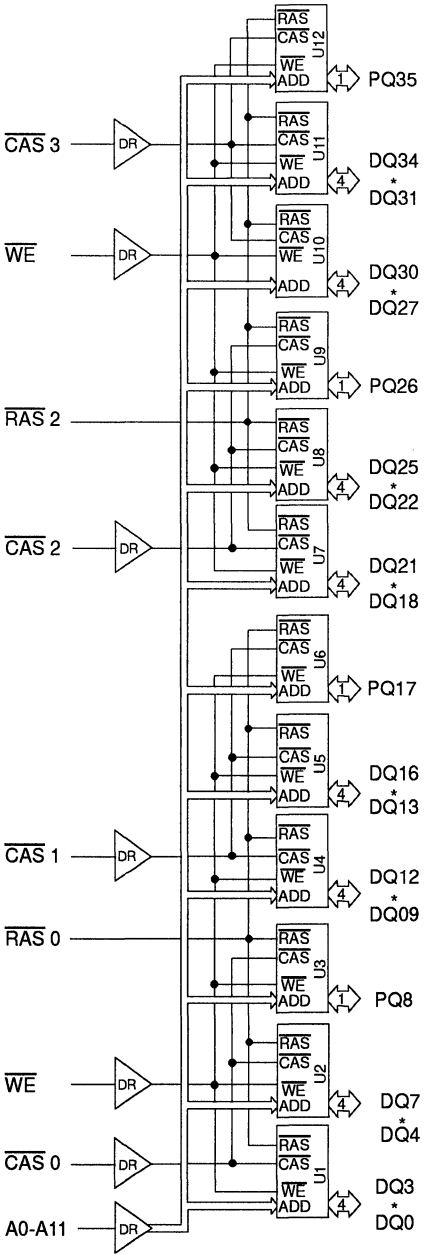
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	NC	47	DQ19	69	NC
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	V_{CC}	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	V_{CC}	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	PQ26	76	PD8
11	NC	33	PQ17	55	NC	77	NC
12	PQ8	34	DQ9	56	V_{SS}	78	NC
13	A0	35	NC	57	A1	79	PQ35
14	A2	36	DQ10	58	A3	80	DQ27
15	V_{CC}	37	V_{CC}	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	NC	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	A11	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	A10	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	NC	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

1. DQ numbering is compatible with non parity (x32) version)

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J4360DLA-70	4M x 36	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	V_{SS}
PD3	NC
PD4	V_{SS}
PD5 (Number of Banks/Organization)	NC
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +7.0	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to V_{CC} + 0.5, 7.0	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	10.8	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.4	—	V_{CC} + 0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	57	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O1}$	Output Capacitance (DQ0~DQ34)	25	pF	
$C_{I/O2}$	Output Capacitance (PQ8, PQ17, PQ26, PQ35)	30	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	1000	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	24	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	1000	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	800	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	2.4	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	1000	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			3.6	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 10s ($\overline{CAS}$, $\overline{WE}$) or 11ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	7	—	ns	
t_{RAH}	Row Address Hold Time	8	—	ns	
t_{ASC}	Column Address Setup Time	2	—	ns	
t_{CAH}	Column Address Hold Time	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	28	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 21ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 23ns (6ns before max t_{CAC} of 29ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	16	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	20	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	42	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	42	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	25	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	50	ns	1, 2

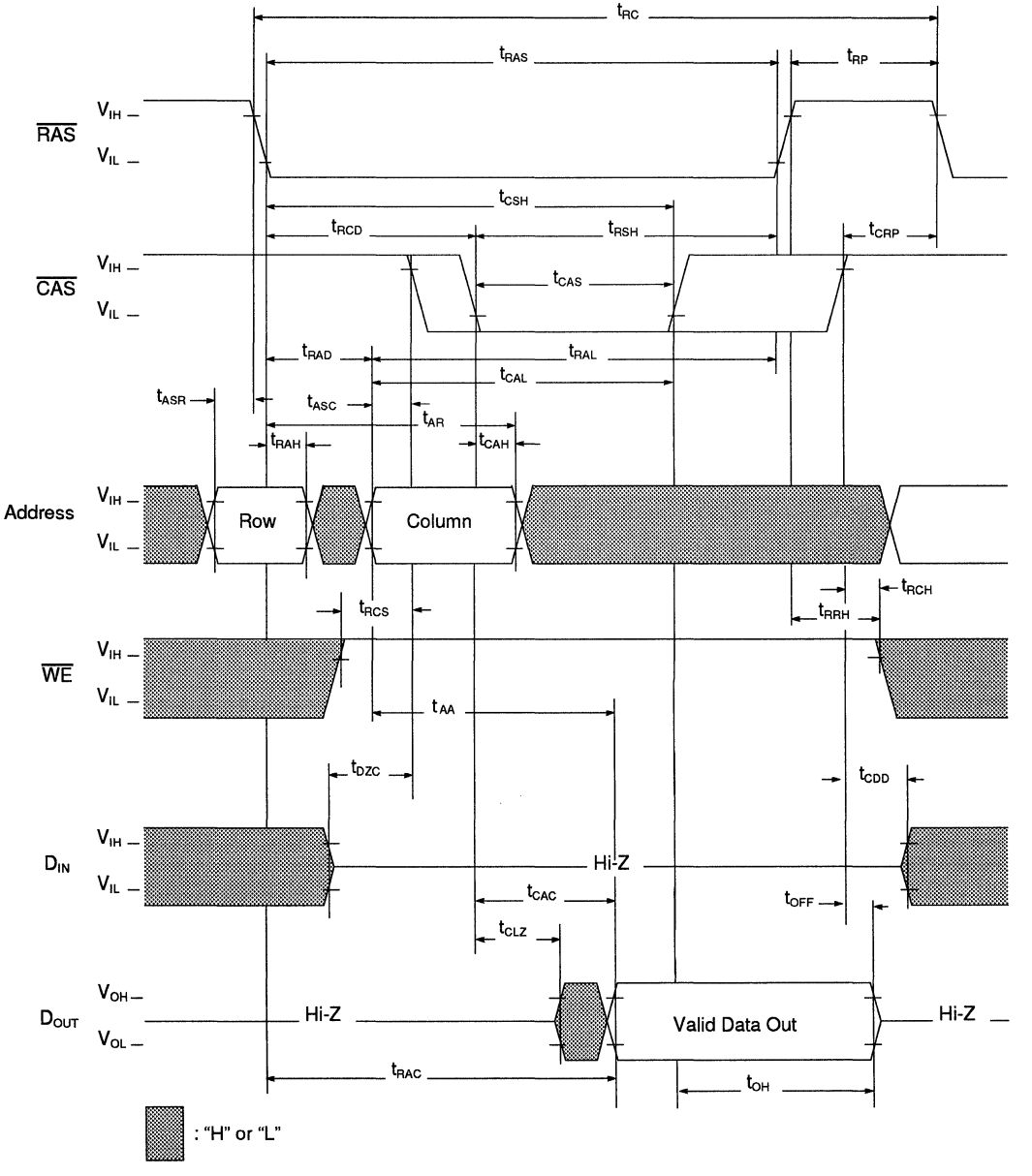
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

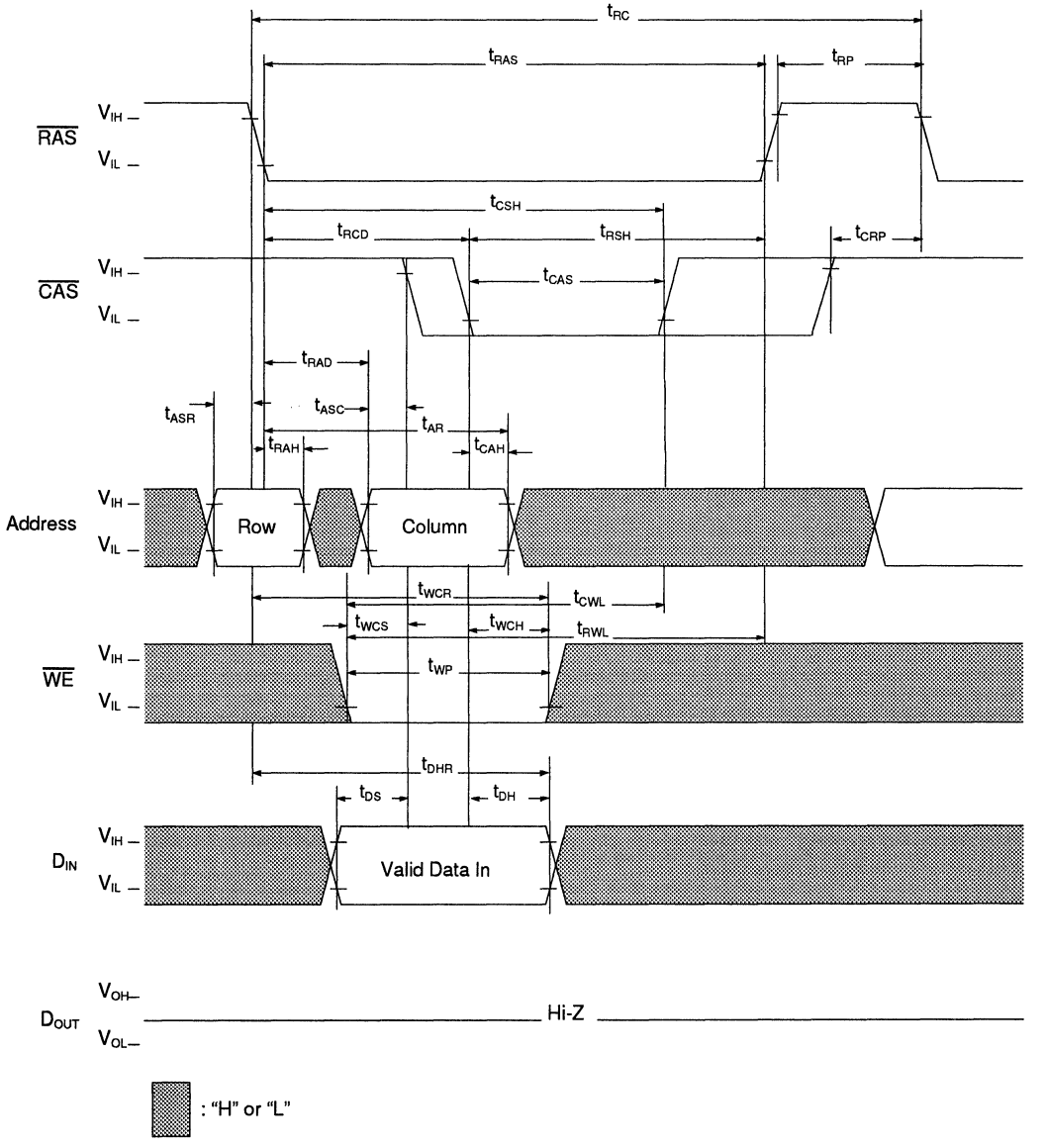
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	16	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	8	—	ns	
t_{REF}	Refresh Period	—	256	ns	1

1. 4096 refreshes are required every 256ms.

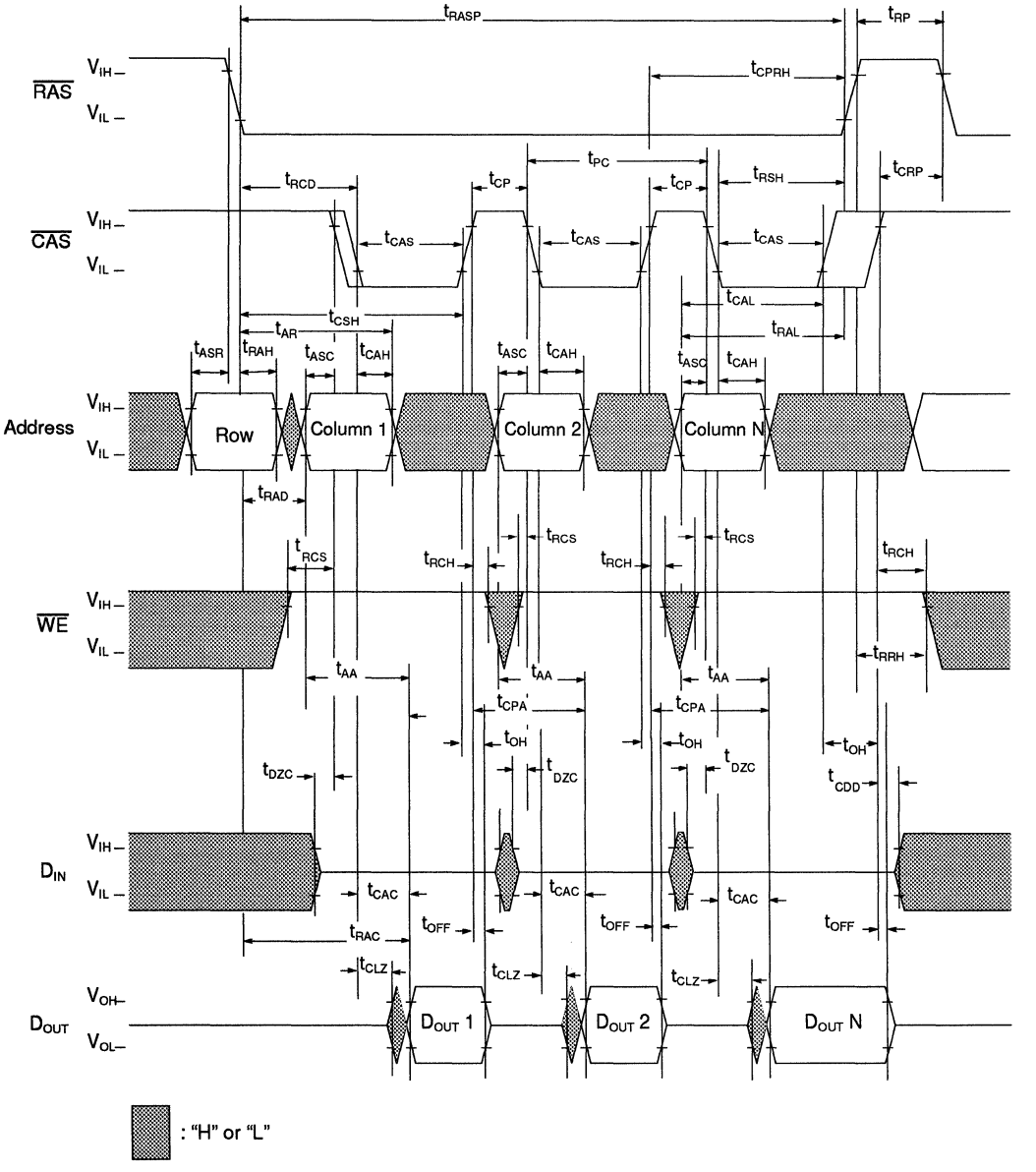
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

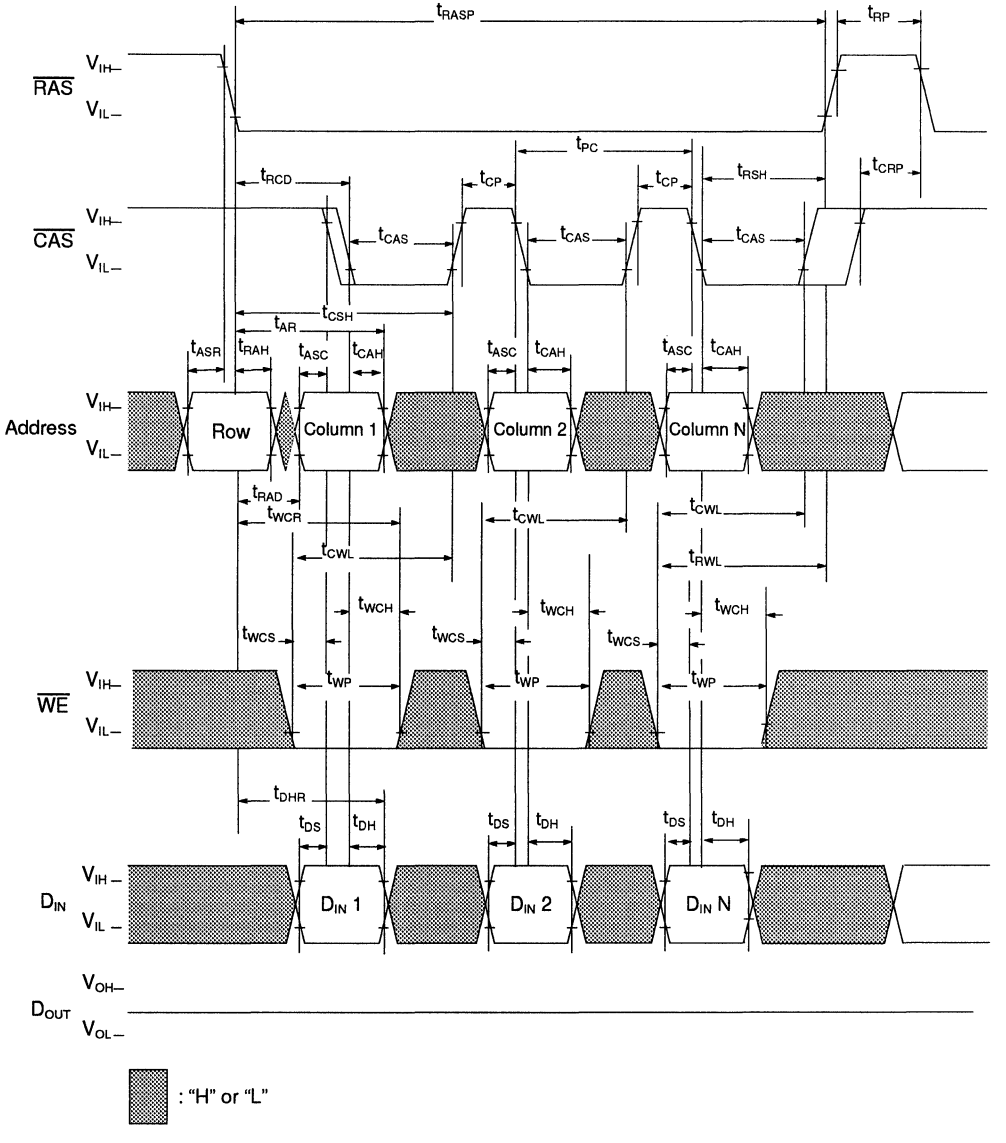
Write Cycle (Early Write)



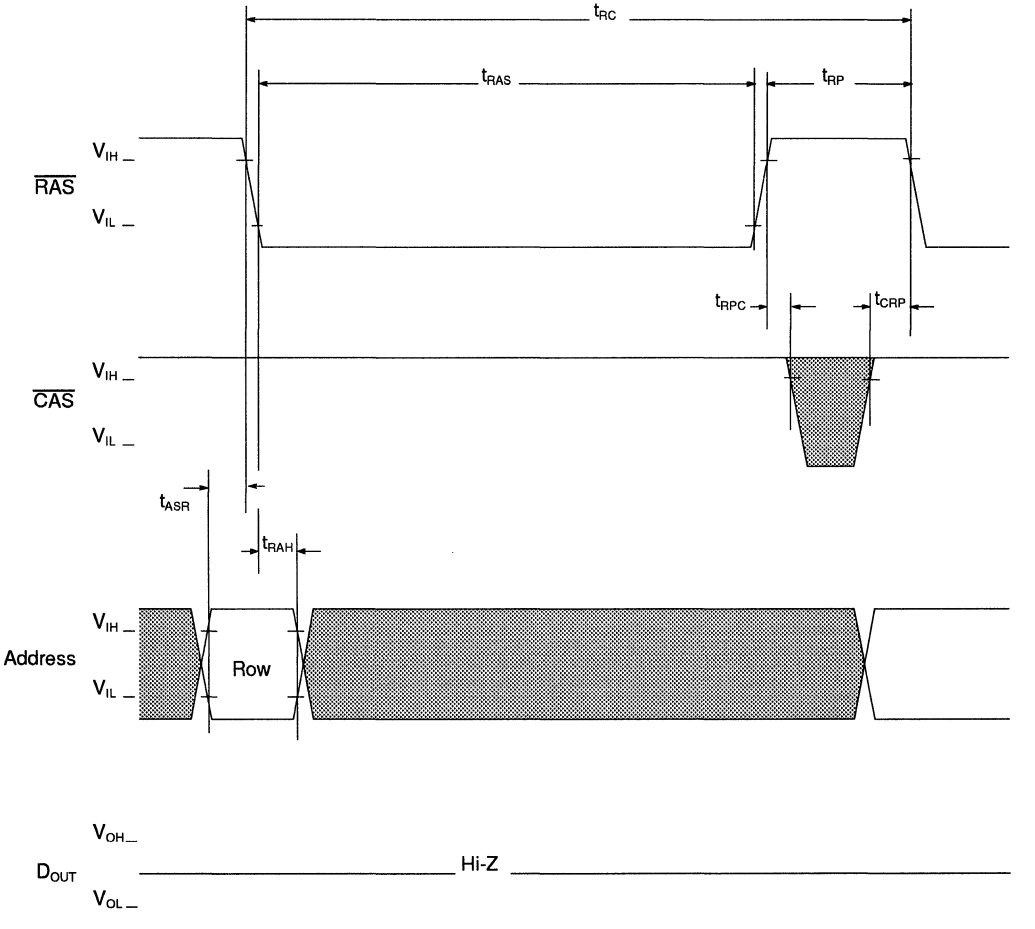
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

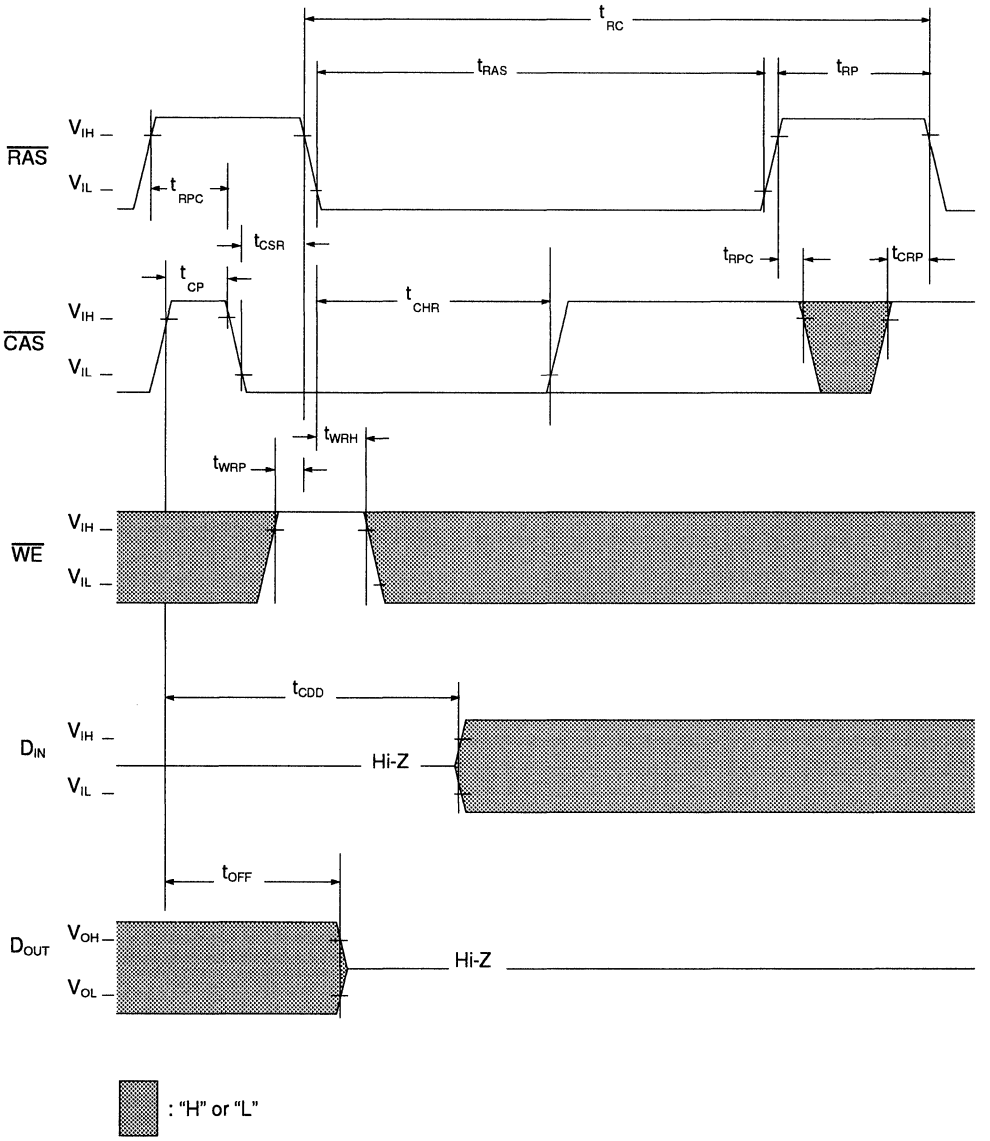


$\overline{RAS}$ Only Refresh Cycle



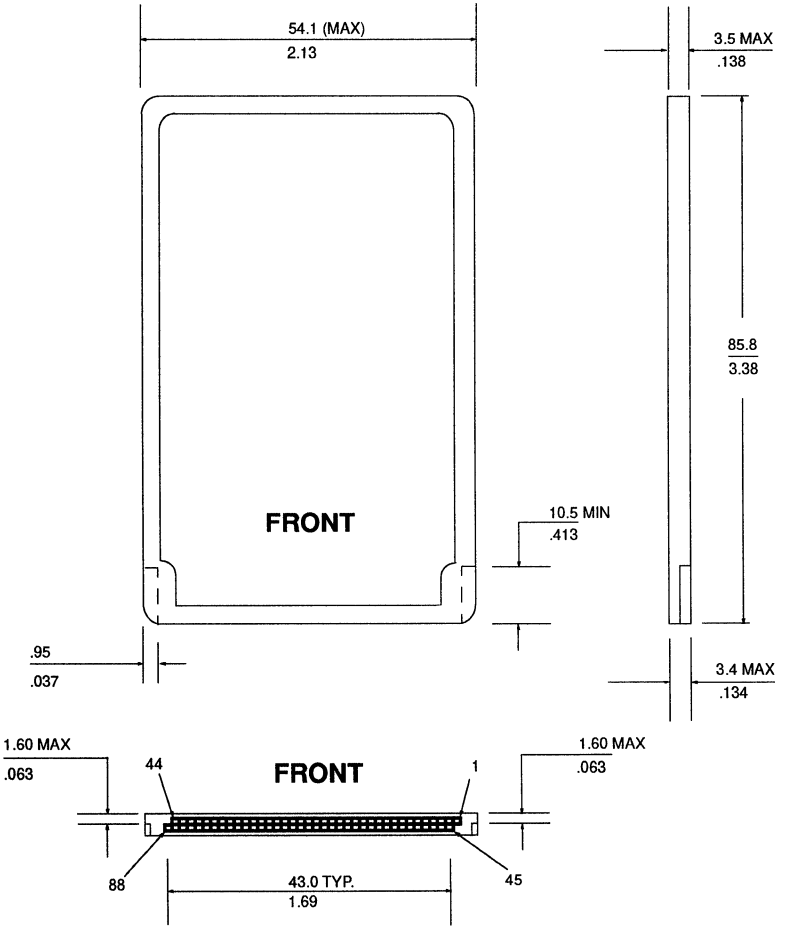
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Preliminary

8M x 36 5.0V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

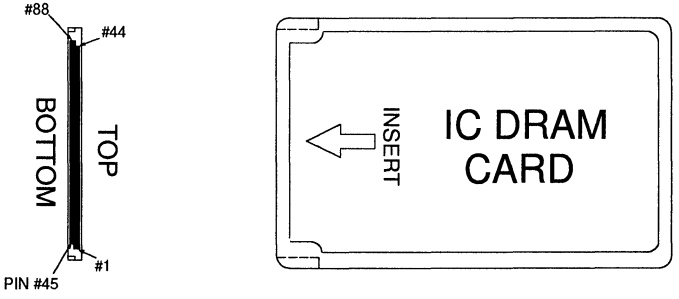
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns
t_{AA}	Access Time From Address	42ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 5.0V, ± 0.25V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x18 or x36 selectability
- 11/11 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 2048 refresh cycles distributed across 256ms
- Polarized Connector

Description

The IBM11J8360DL is a 32MB industry standard 88-pin IC DRAM card. It is organized as a 8M x 36 high speed memory array. It is built using 16 - 4Mx4 devices, 8 - 4Mx1 devices and is compatible to the JEDEC/PCMCIA/JEIDA 88-pin standard. Each bit is uniquely addressed via 22 address bits. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x36 configuration the memory may be utilized as two banks, each having four unique bytes. The x18 configuration may be utilized as four banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other banks in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications.

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, PQ17, PQ26, PQ35	Parity Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

Pinout

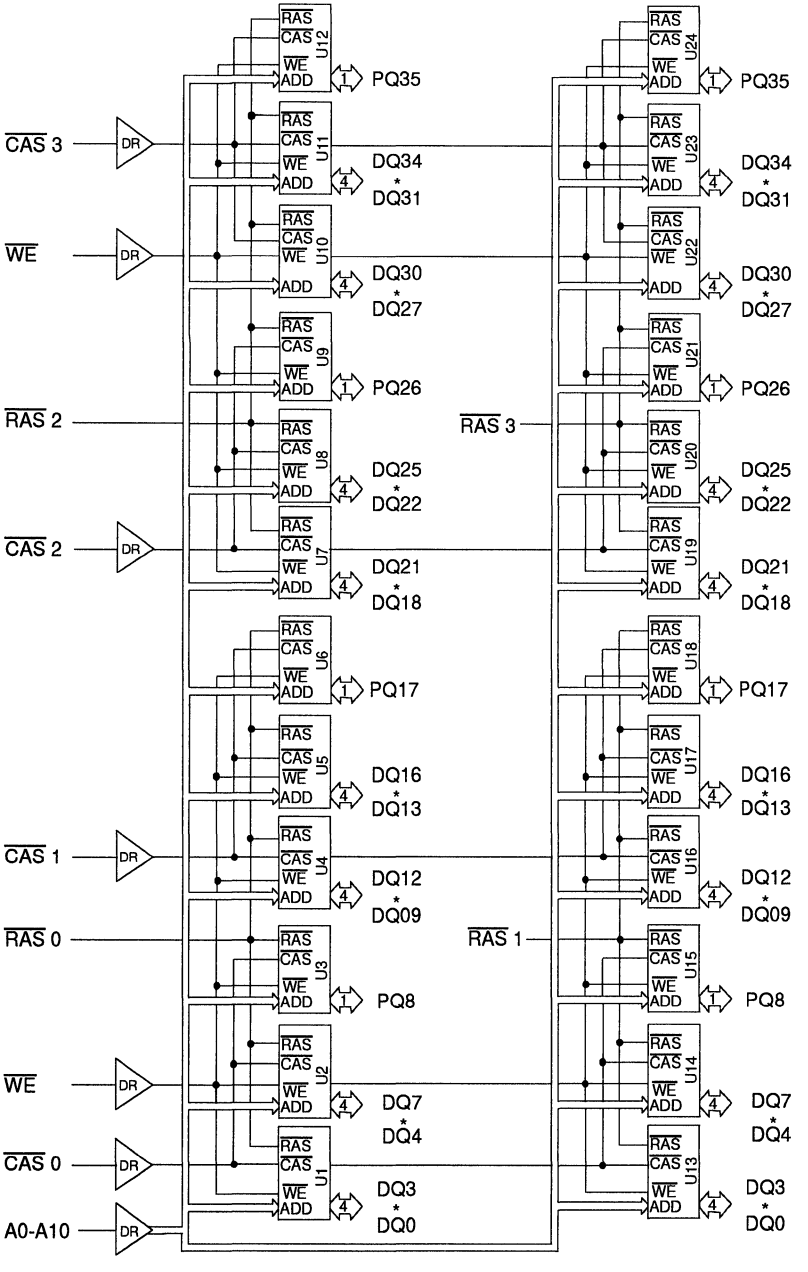
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	NC	47	DQ19	69	$\overline{RAS3}$
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	V_{CC}	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	V_{CC}	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	PQ26	76	PD8
11	NC	33	PQ17	55	NC	77	NC
12	PQ8	34	DQ9	56	V_{SS}	78	NC
13	A0	35	NC	57	A1	79	PQ35
14	A2	36	DQ10	58	A3	80	DQ27
15	V_{CC}	37	V_{CC}	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	NC	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	NC	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	A10	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	$\overline{RAS1}$	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

1. DQ numbering is compatible with non parity (x32) version)

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J8360BLA-70	8M x 36	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	V_{SS}
PD3	NC
PD4	V_{SS}
PD5 (Number of Banks/Organization)	V_{SS}
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +7.0	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to V_{CC} + 0.5, 7.0	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	10.8	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.4	—	V_{CC} + 0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	57	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O1}$	Output Capacitance (DQ0~DQ34)	32	pF	
$C_{I/O2}$	Output Capacitance (PQ8, PQ17, PQ26, PQ35)	42	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	1200	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	48	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	1200	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	1080	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	4.8	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	1200	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			7.2	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 10s ($\overline{CAS}$, $\overline{WE}$) or 11ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	7	—	ns	
t_{RAH}	Row Address Hold Time	8	—	ns	
t_{ASC}	Column Address Setup Time	2	—	ns	
t_{CAH}	Column Address Hold Time	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	28	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 21ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 23ns (6ns before max t_{CAC} of 29ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	16	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	20	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	42	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	42	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	25	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	50	ns	1, 2

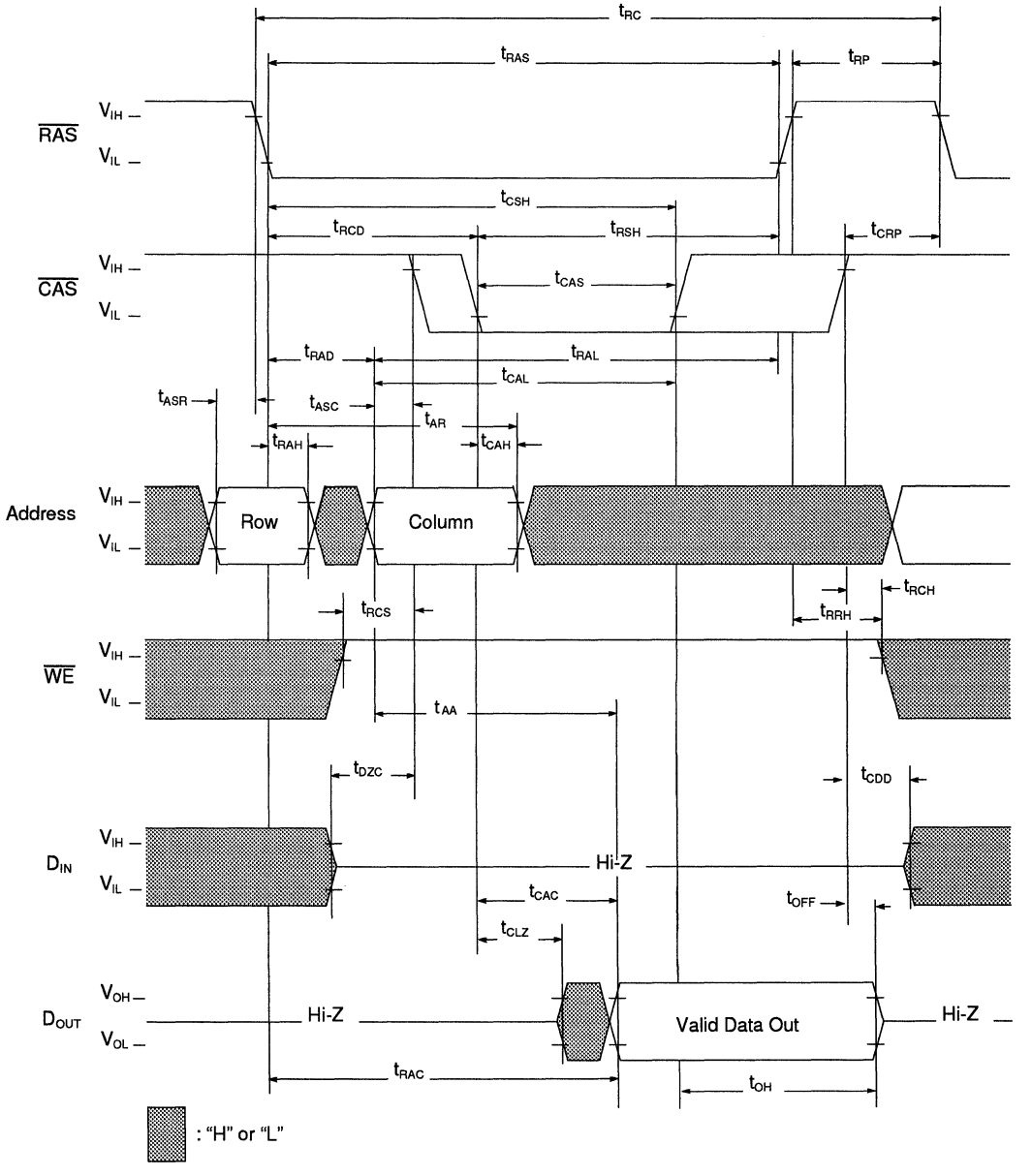
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

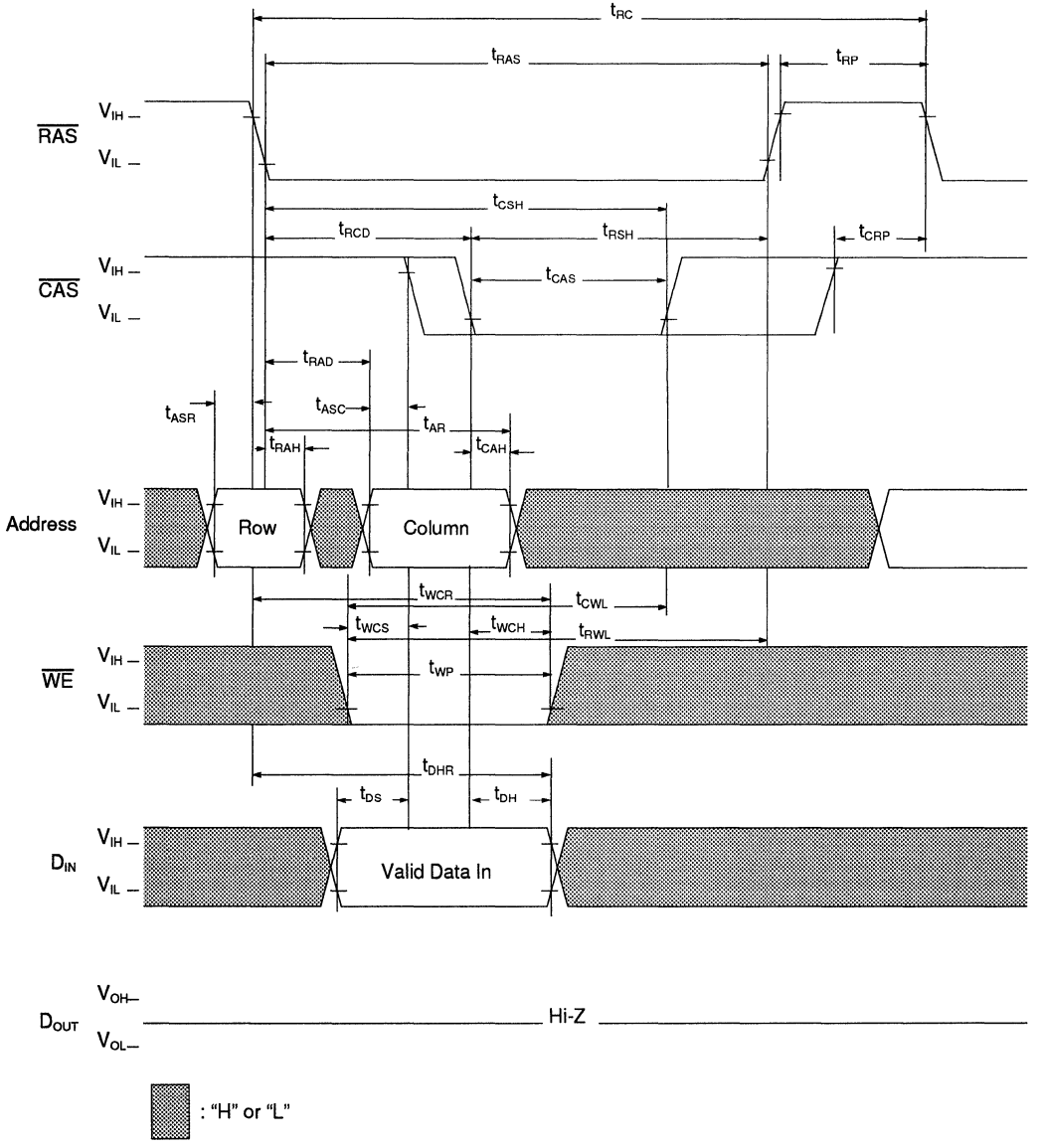
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	16	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	8	—	ns	
t_{REF}	Refresh Period	—	256	ns	1

1. 2048 refreshes are required every 256ms.

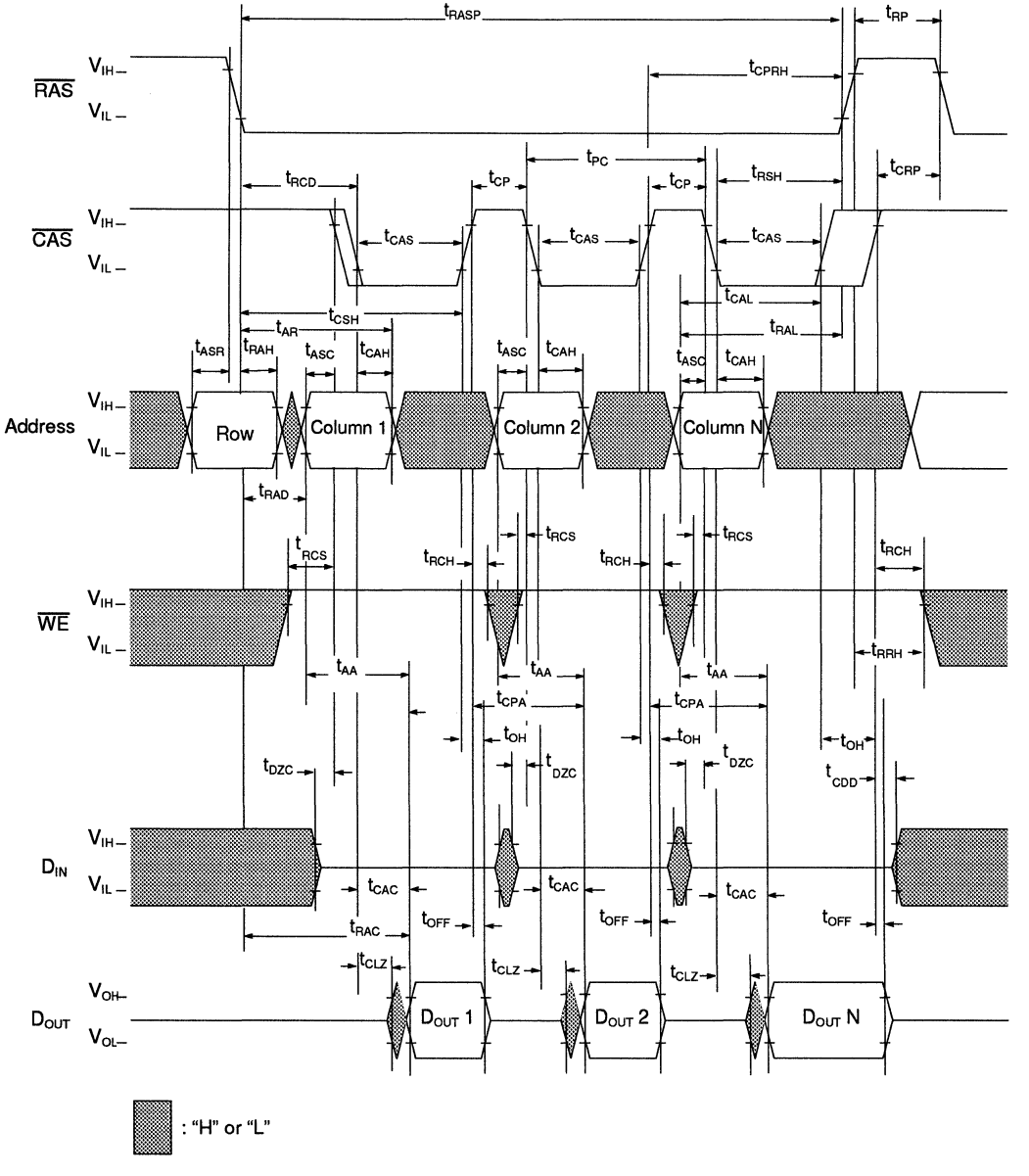
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

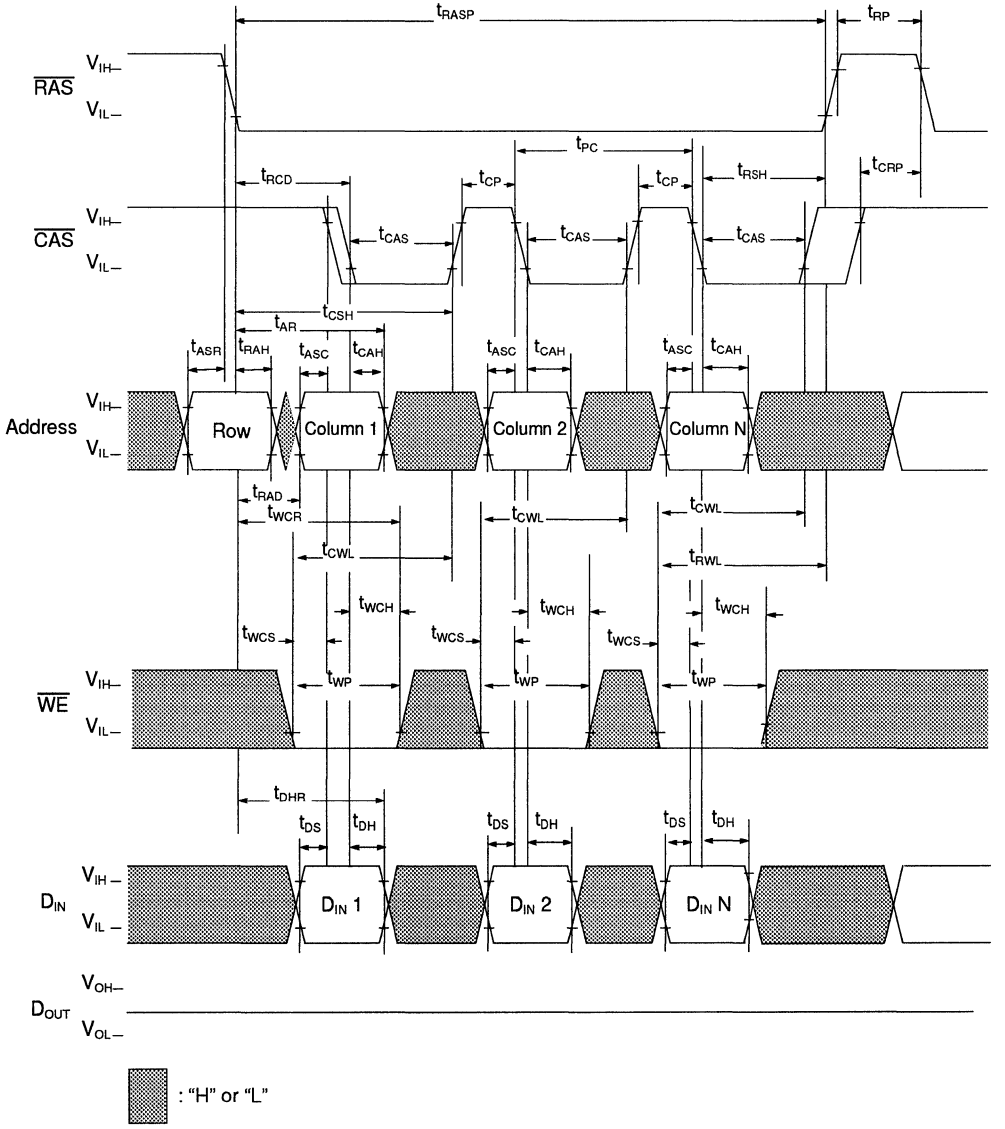
Write Cycle (Early Write)



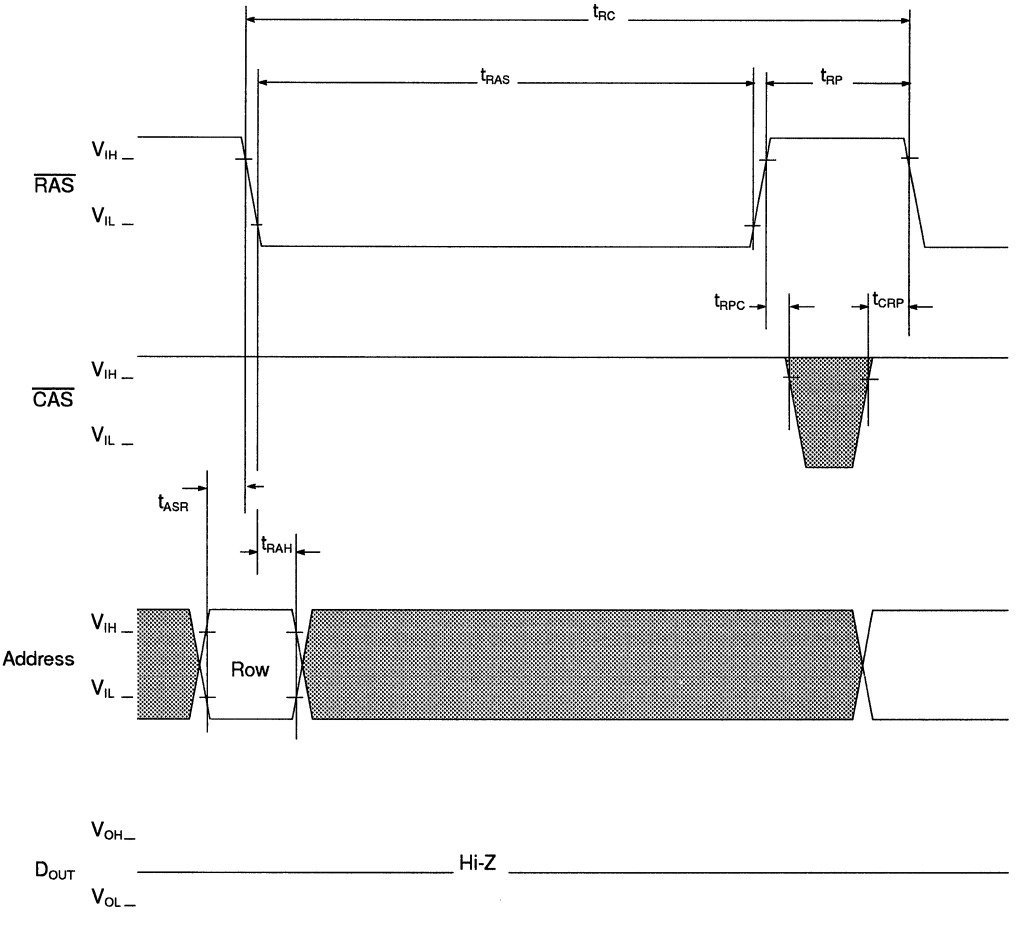
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

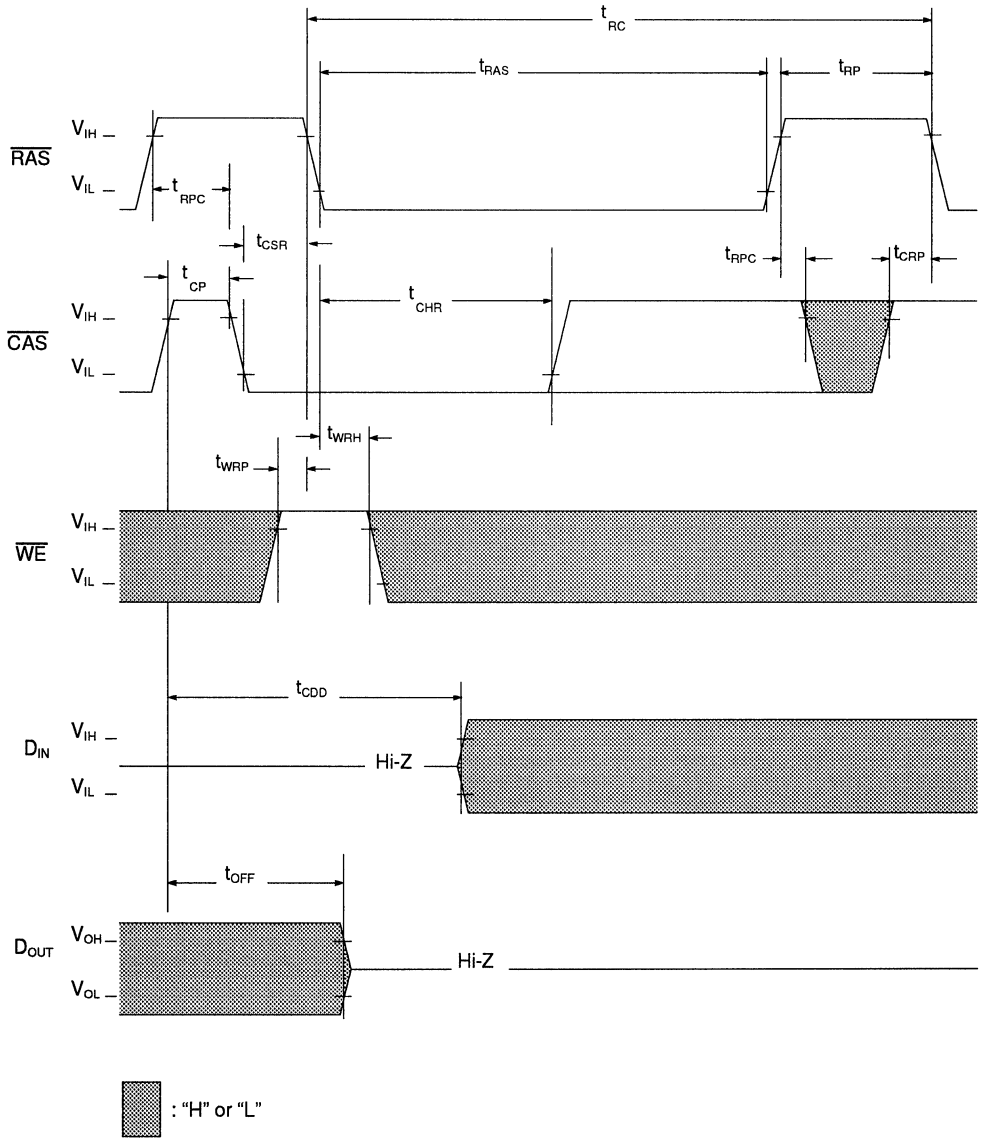


$\overline{RAS}$ Only Refresh Cycle



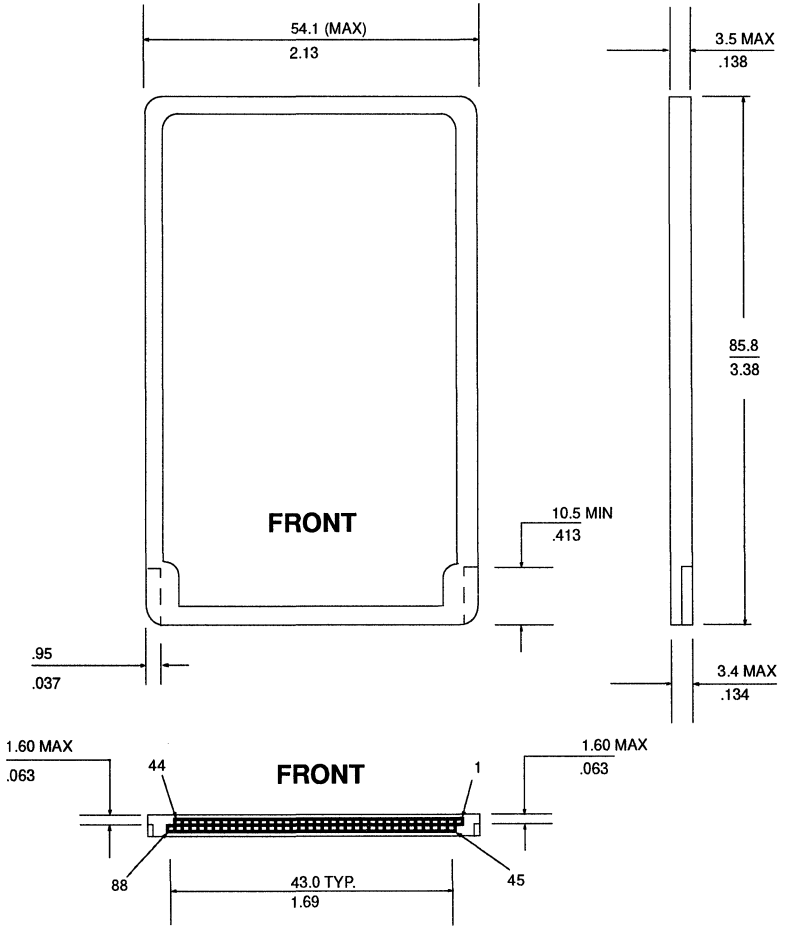
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

8M x 36 5.0V IC DRAM Card

Features

- Industry Standard 88Pin IC DRAM Card
- Performance:

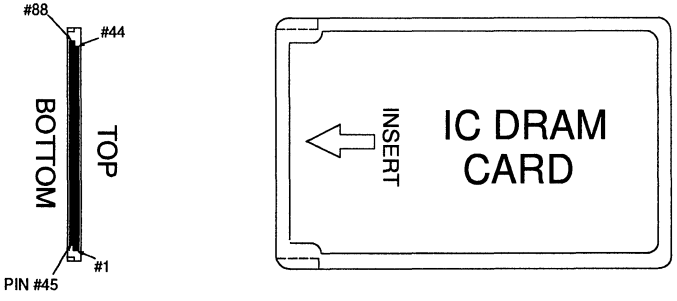
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns
t_{AA}	Access Time From Address	42ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Industry Standard DRAM functions & timings
- High Performance CMOS process
- Single 5.0V, ± 0.25V Power Supply
- All inputs buffered except $\overline{RAS}$ and DATA inputs
- Multiple $\overline{RAS}$ inputs for x18 or x36 selectability
- 12/11 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, $\overline{CAS}$ before $\overline{RAS}$ and BBU (Battery Backup)
- 4096 refresh cycles distributed across 256ms
- Polarized Connector

Description

The IBM11J8360DL is a 32MB industry standard 88-pin IC DRAM card. It is organized as a 8M x 36 high speed memory array. It is built using 16 - 4Mx4 devices, 8 - 4Mx1 devices and is compatible to the JEDEC/PCMCIA/JEIDA 88-pin standard. Each bit is uniquely addressed via 22 address bits. The x4 Drams require 12 ROW/10 COLUMN addresses and the x1 DRAMS require 11ROW/11 COLUMN addresses. The highest order ROW addresses must be sent as the highest order COLUMN address to satisfy both DRAM requirements. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and $\overline{RAS}$ signals are not buffered, which preserves the access specification of 70ns. Multiple $\overline{RAS}$ inputs are used to conserve power by allowing individual bank selection. In the x36 configuration the memory may be utilized as two banks, each having four unique bytes. The x18 configuration may be utilized as four banks each having two unique bytes. Only one bank is activated by each $\overline{RAS}$, leaving the other banks in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. The related 8M x 32 version of this ICDRAM card is IBM11J8320DLA

Card Outline



Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A11	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, PQ17, PQ26, PQ35	Parity Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects

Pinout

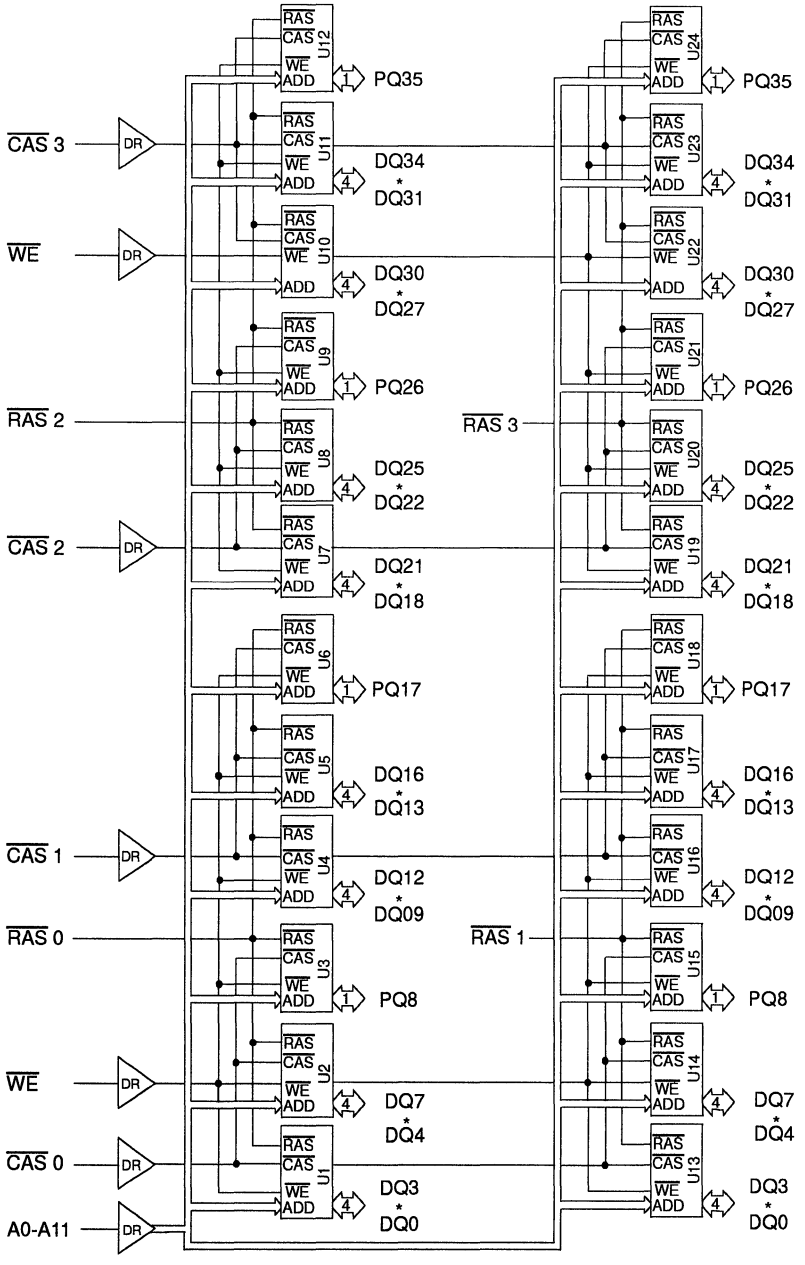
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	23	$\overline{CAS0}$	45	V_{SS}	67	V_{SS}
2	DQ0	24	$\overline{CAS1}$	46	DQ18	68	$\overline{CAS3}$
3	DQ1	25	NC	47	DQ19	69	$\overline{RAS3}$
4	DQ2	26	$\overline{RAS2}$	48	DQ20	70	$\overline{WE}$
5	DQ3	27	V_{CC}	49	DQ21	71	PD1
6	DQ4	28	PD2	50	DQ22	72	PD3
7	DQ5	29	PD4	51	DQ23	73	V_{SS}
8	DQ6	30	PD6	52	DQ24	74	PD5
9	V_{CC}	31	NC	53	DQ25	75	PD7
10	DQ7	32	NC	54	PQ26	76	PD8
11	NC	33	PQ17	55	NC	77	NC
12	PQ8	34	DQ9	56	V_{SS}	78	NC
13	A0	35	NC	57	A1	79	PQ35
14	A2	36	DQ10	58	A3	80	DQ27
15	V_{CC}	37	V_{CC}	59	A5	81	DQ28
16	A4	38	DQ11	60	A7	82	DQ29
17	NC	39	DQ12	61	A9	83	DQ30
18	A6	40	DQ13	62	A11	84	DQ31
19	A8	41	DQ14	63	V_{SS}	85	DQ32
20	A10	42	DQ15	64	NC	86	DQ33
21	NC	43	DQ16	65	$\overline{RAS1}$	87	DQ34
22	$\overline{RAS0}$	44	V_{SS}	66	$\overline{CAS2}$	88	V_{SS}

1. DQ numbering is compatible with non parity (x32) version)

Ordering Information

Part Number	Organization	Speed	Notes
IBM11J8360DLA-70	8M x 36	70ns	For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version.

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1 (PD1 - PD4: Addressing/Dram Type)	V_{SS}
PD2	V_{SS}
PD3	NC
PD4	V_{SS}
PD5 (Number of Banks/Organization)	V_{SS}
PD6 (Speed)	V_{SS}
PD7	NC
PD8 (Refresh Type)	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +7.0	V	1
V_{IN}	Input Voltage ($\overline{RAS}$ & DATA)	-0.5 to V_{CC} + 0.5, 7.0	V	1
	Input Voltage (Redriven Signals)	-0.5 to V_{CC} + 0.5	V	1
V_{OUT}	Output Voltage	-0.5 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +55	°C	1
T_{STG}	Storage Temperature	-40 to +85	°C	1
P_D	Power Dissipation	10.8	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 55°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage ($\overline{RAS}$ & DATA)	2.4	—	V_{CC} + 0.5	V	1
	Input High Voltage (Redriven Signals)	2.0	—	V_{CC}	V	1
V_{IL}	Input Low Voltage ($\overline{RAS}$ & DATA)	-0.5	—	0.8	V	1
	Input Low Voltage (Redriven Signals)	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0~A9)	15	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	57	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	20	pF	
$C_{I/O1}$	Output Capacitance (DQ0~DQ34)	32	pF	
$C_{I/O2}$	Output Capacitance (PQ8, PQ17, PQ26, PQ35)	42	pF	

DC Electrical Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	1000	mA	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	48	mA	1, 3
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	1000	mA	
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	800	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	4.8	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	1000	mA	
I_{CC7}	Battery Backup Refresh Current Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤ V_{IL}, $\overline{WE}$ ≥ V_{IH}, t_{RAS} ≤ 1µSec, t_{RC} = 125µSec)			7.2	mA	1, 2
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$,ADD	-10	+10		
		$\overline{WE}$	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for the X32 configuration using One Bank

AC Characteristics (T_A = 0 to +55°C, V_{CC} = 5.0 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delays: 2ns minimum, 10s ($\overline{CAS}$, $\overline{WE}$) or 11ns (Address) maximum delay, no pulse shrinkage. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 70ns
4. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	21	—	ns	2
t_{ASR}	Row Address Setup Time	7	—	ns	
t_{RAH}	Row Address Hold Time	8	—	ns	
t_{ASC}	Column Address Setup Time	2	—	ns	
t_{CAH}	Column Address Hold Time	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	45	ns	2
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	28	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	—	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	ns	

1. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 21ns plus a minimum t_{OH} of 2ns would result in turning data out of the card at 23ns (6ns before max t_{CAC} of 29ns).
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. This timing parameter is not applicable to this product, but may apply to a related product in this family.

Write Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	
t_{WCH}	Write Command Hold Time	16	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	ns	1
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	20	—	ns	

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	42	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	42	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OH}	Output Data Hold Time	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	25	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	2	29	ns	5

1. Access time is determined by the later of t_{RAC}, t_{CAC}, t_{AA} or t_{CPA}.
2. Measured with two TTL loads and 100pF.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	50	ns	1, 2

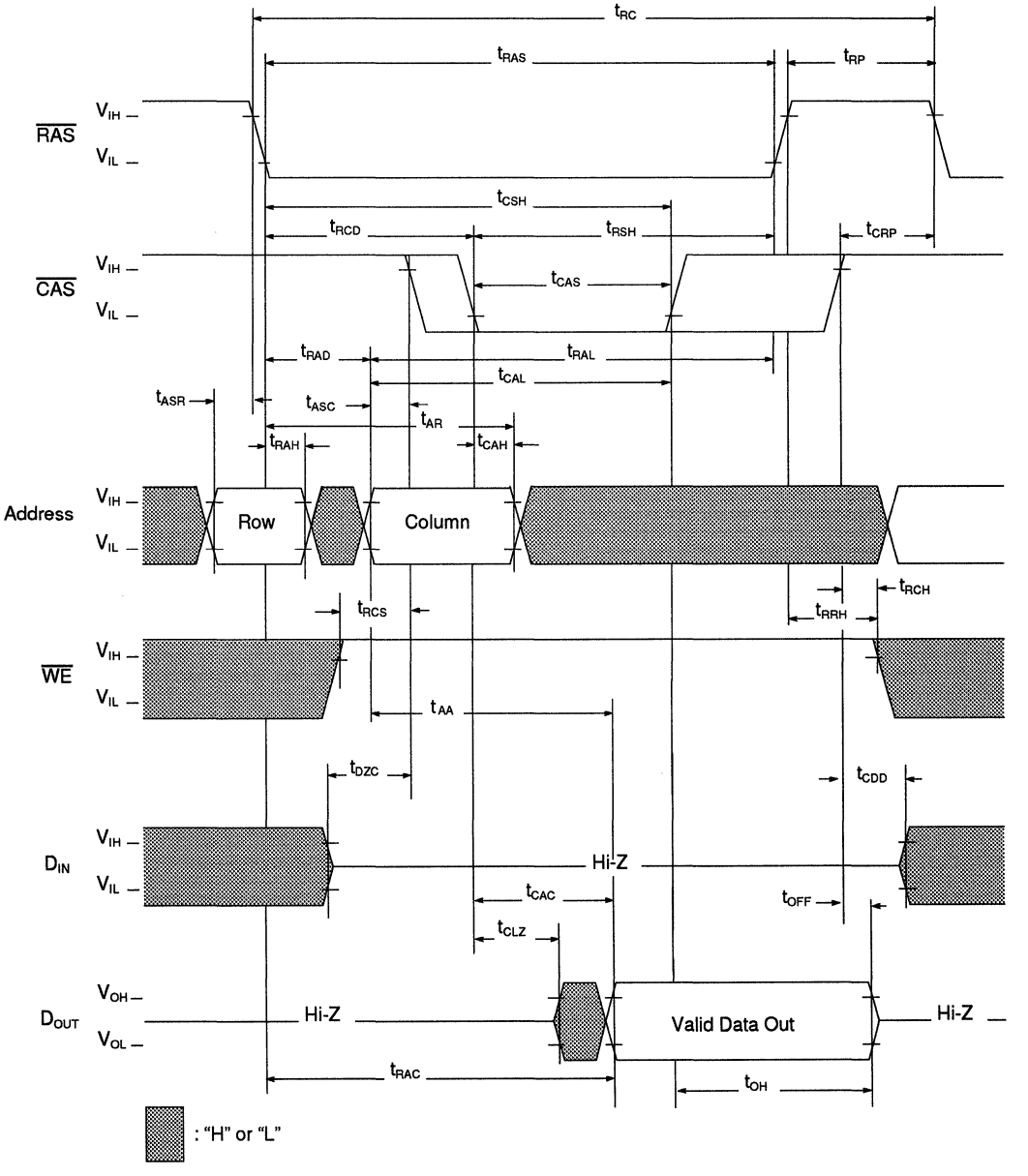
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pf.

Refresh Cycle

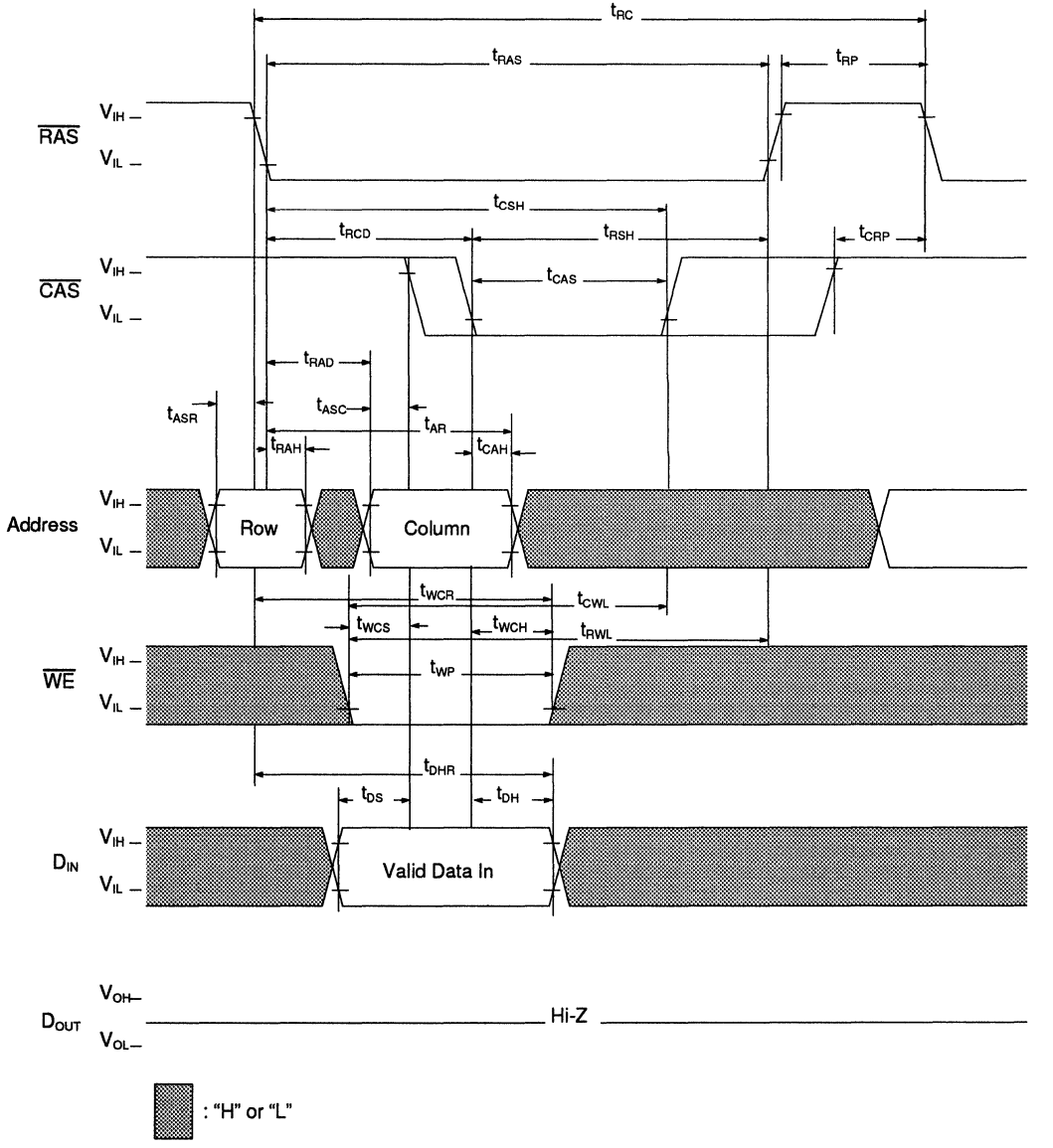
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	18	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	16	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	8	—	ns	
t_{REF}	Refresh Period	—	256	ns	1

1. 4096 refreshes are required every 256ms.

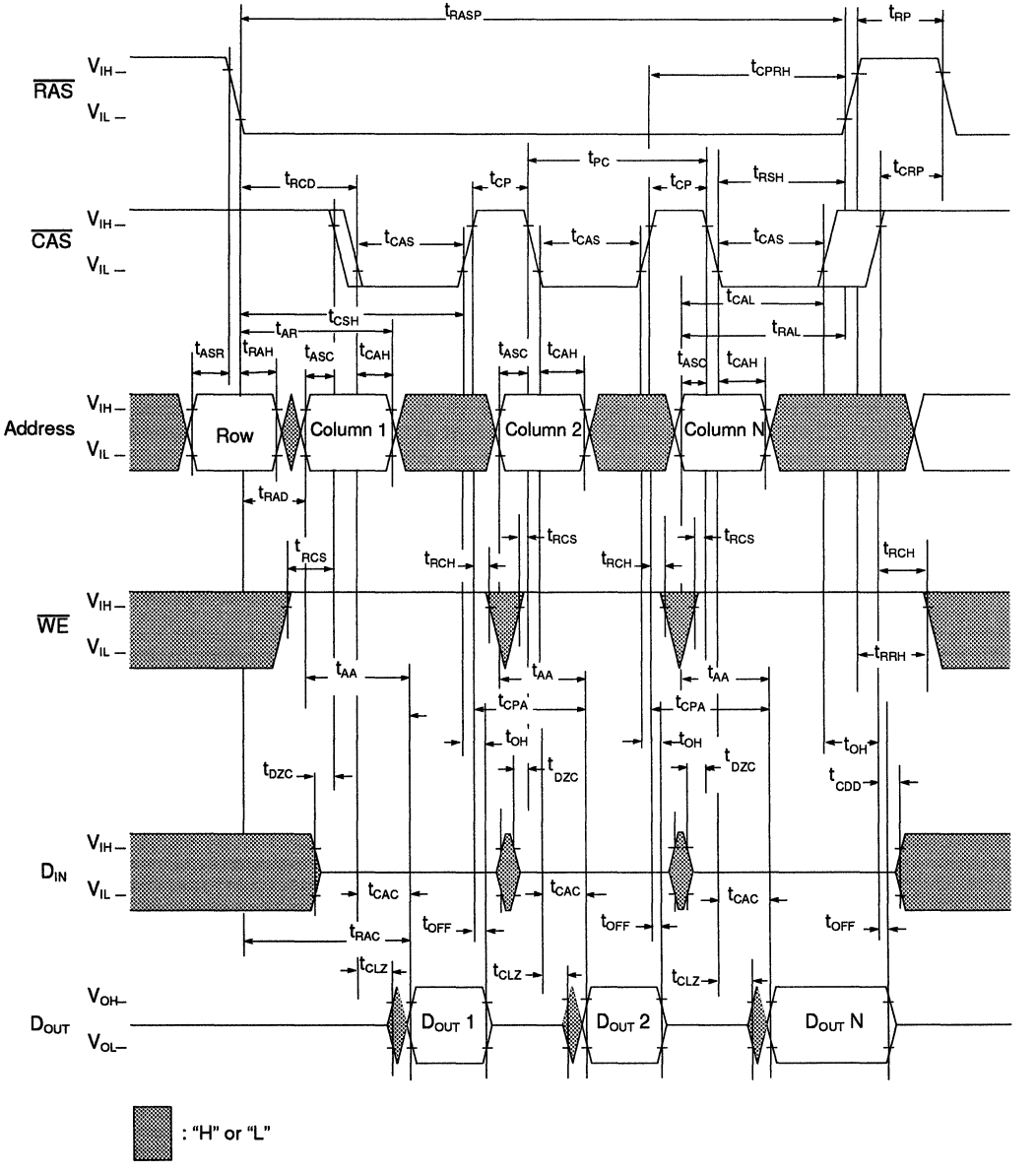
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Hi-Z
Valid Data Out
Hi-Z
tRAC
tOH
: "H" or "L"

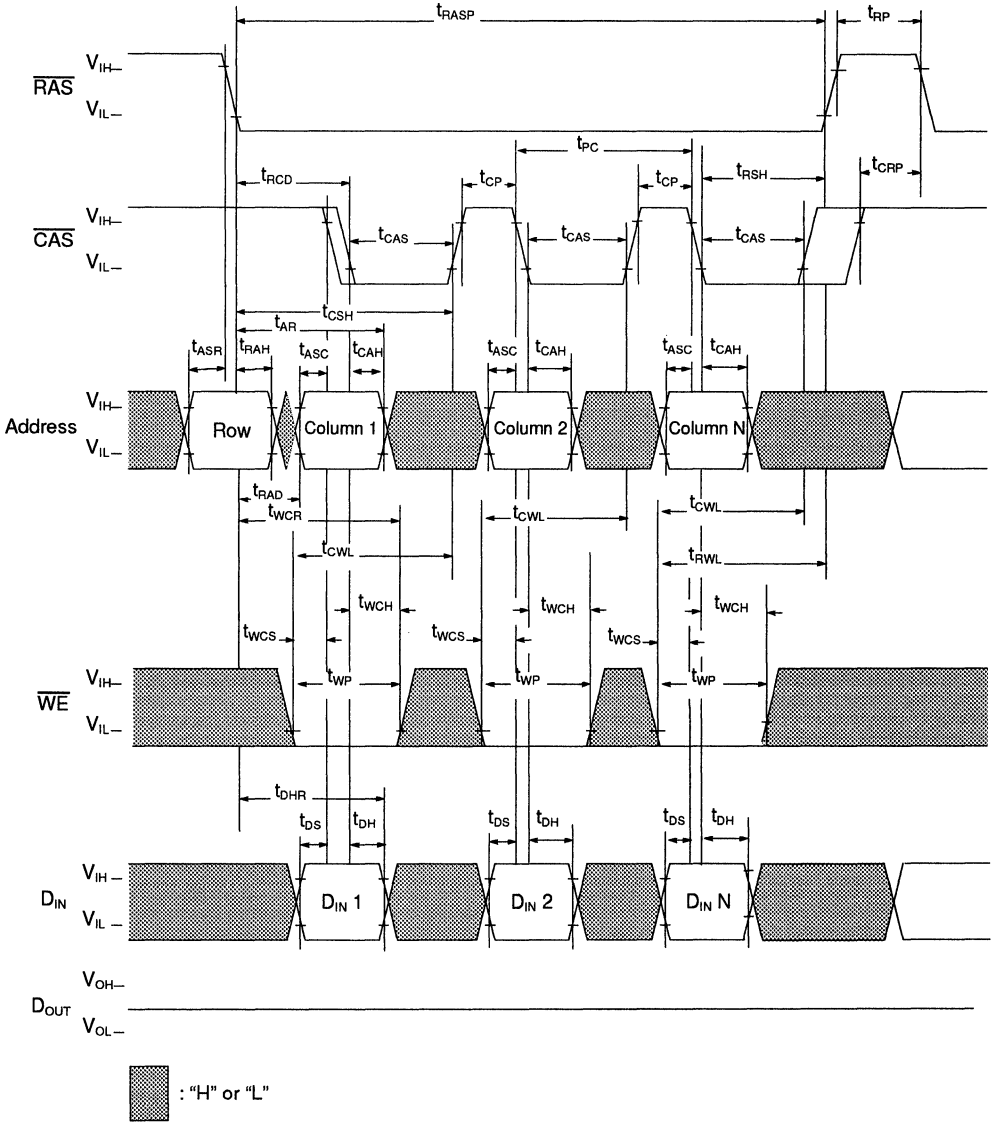
Write Cycle (Early Write)



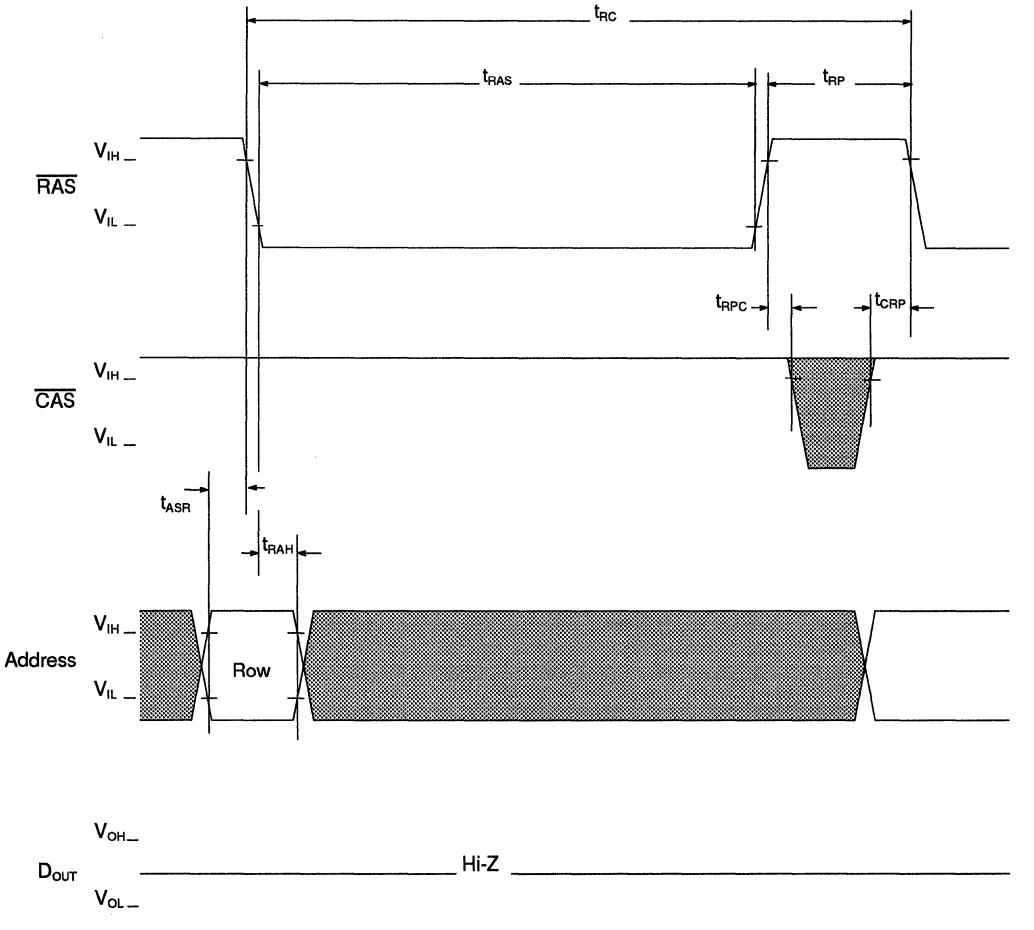
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



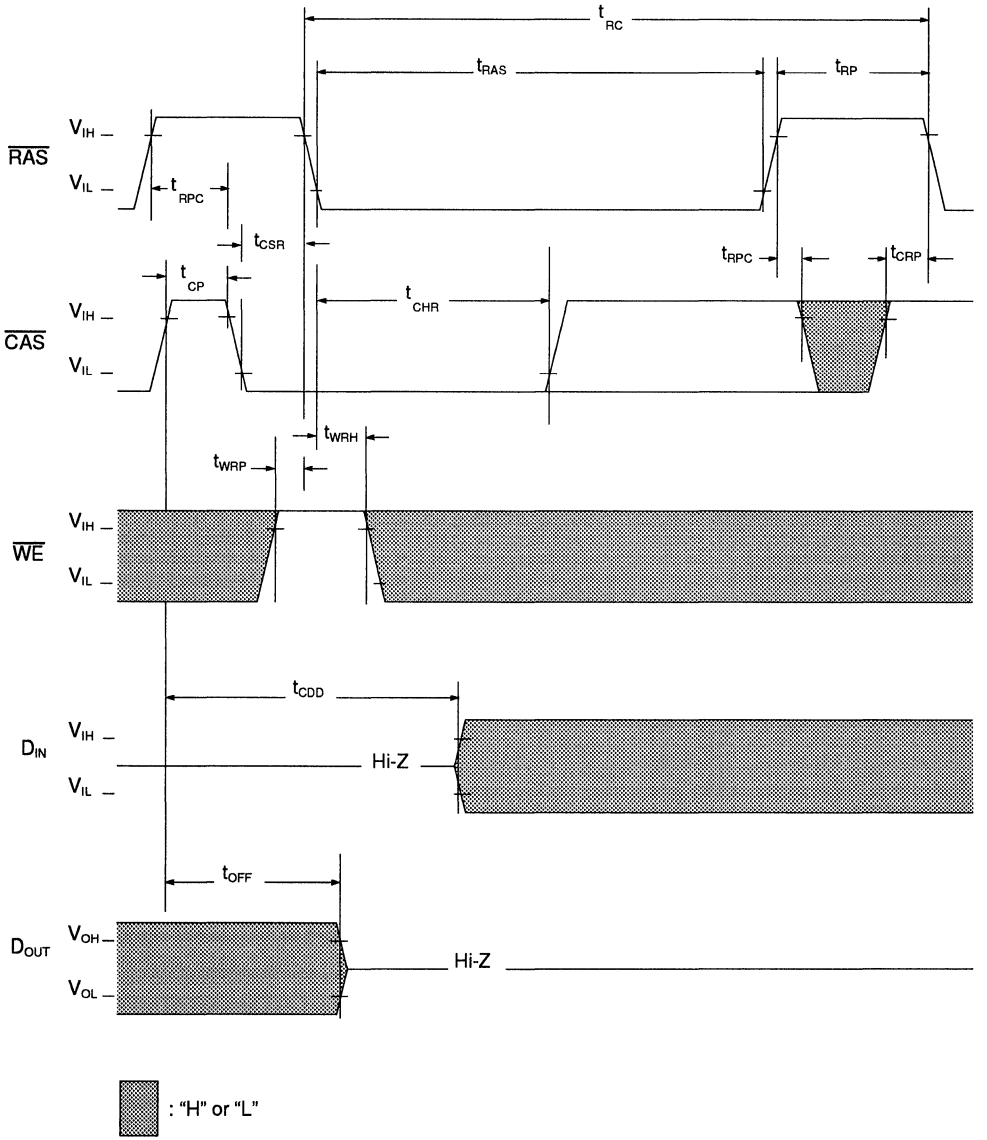
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

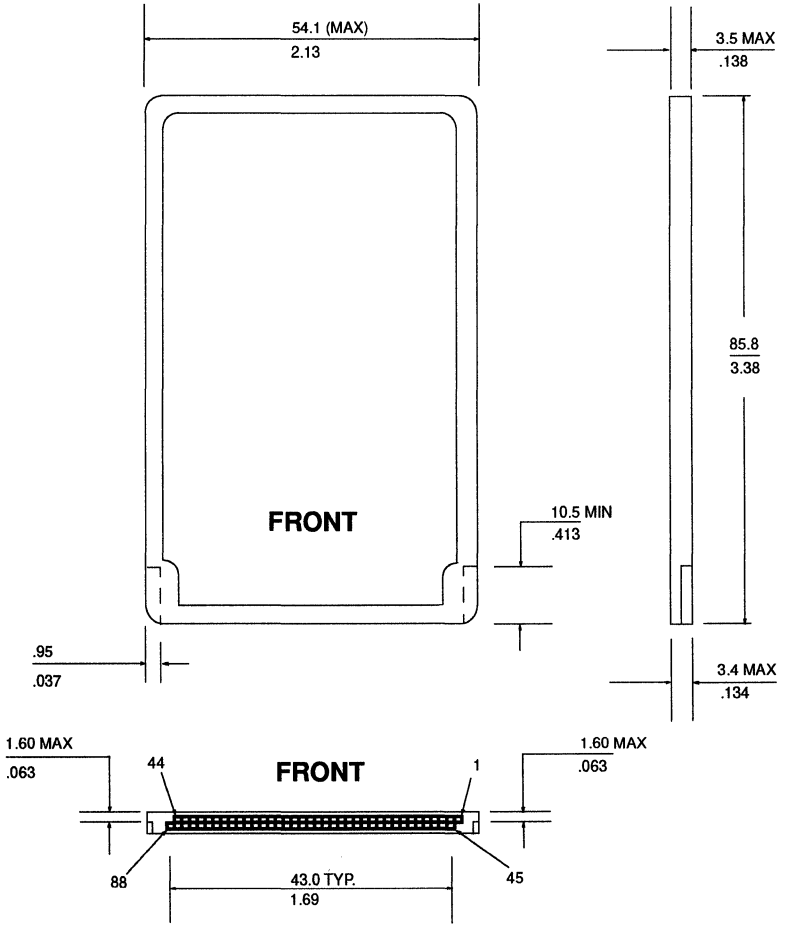
Note: $\overline{WE}$, D_{IN} are "H" or "L"

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Application Notes

Introduction

DRAMs may be supplied on modules known as SIMMs, DIMMs, SO DIMMs or IC DRAM cards. These assemblies are designed in a well-defined industry standard format. There are significant advantages to the system designer of using these modules rather than unique assemblies of DRAMs.

1. Most personal computers, workstations and other computer-based systems require low-cost customer upgradeable memory, ease of repair and, or variable-base memory sizes (for different models). Because DRAM modules are designed to a JEDEC standard, they and their associated connectors are widely available from a variety of vendors. The end-user can easily acquire memory upgrades from the original system manufacturer or from a large number of specialized suppliers. These "user friendly" upgrades are easily installed, changed or removed without extensive training.
2. The use of industry standard DRAM Modules enables the system supplier to design systems that will be compatible with higher density DRAM technology as it becomes available.
3. No viable method of socketing the rapidly-emerging TSOP DRAM packaging exists. An external carrier such as a DRAM module is necessary.
4. DRAM modules are configured to support multiple memory subsystem architectures such as Non-parity, Parity, and ECC.
5. DRAM module connectors can consume less system board or adapter card real estate than directly attaching individual chips, thus providing potential density increases.

Module Descriptions

The IBM Microelectronics Division offers a broad range of industry-standard DRAM modules:

72 pin Single-Inline-Memory Modules (SIMMs)

72-pin SIMMs are popular 5V-only, industry standard assemblies with functionally equivalent contacts on both sides of the card. Capacity ranges from 1 to 32MB. They have 32, 36 or 40 data bits in 4-byte wide data busses and are constructed with 1 to 16Mb SOJ or TSOP-packaged DRAMs. They are 4.25 inches wide and vary in height (generally 1 inch). Presence Detect pins provide speed and density information.

168 pin Dual-Inline-Memory Modules (DIMMs)

168-pin DIMMs are designed to a new industry standard using functionally unique contacts on both sides of the card. Both 3.3 V and 5.0V versions are currently available. Constructed with 4 to 64Mb DRAMs, their capacity is 8 to 128MB with future DIMMs planned to 512MB when assembled with 256Mb DRAM technology. They are 5.25 inches wide and vary in height ranging from 1 to 1.5 inches. Data busses have 64, 72 or 80 data bits. Eight buffered Presence Detect pins provide speed and density information while two additional Identity pins provide bus size and self-refresh information.

72 pin Small-Outline-Dual-Inline-Memory Modules (SO DIMMs)

Useful in mobile or portable computer applications, 72 pin SO (small outline) DIMMs are 2.35 inches wide with a variable height ranging from 1 to 1.5 inches. They are constructed with 4 to 16Mb DRAMs (TSOP packages only) and are also extendable to 256Mb DRAMs. Data bus widths are 32 or 36 data bits with capacities of 2MB to 16MB currently available.

IC DRAM Cards

Also intended for portable applications, IC DRAM cards are fully enclosed rugged assemblies having dimensions equivalent to the popular PCMCIA cards. Similar in architecture to 72 pin SIMMs, these 88 pin cards are 3.37 by 2.13 by 0.130 inches in size and available in 5 or 3V configurations. Constructed with 4 to 16Mb TSOP-packaged DRAMs, 32 and 36 bit capacities of 2 to 32MB are offered. Future cards can be based with up to 256Mb technology.Eight Presence Detect pins provide speed/density information.

DRAM Module Pin Assignment Impact

Within each DRAM module type, pinouts vary due to different densities, memory architecture and DRAM chip technology. The application note specific to the module type provides the pin assignment detail needed for the memory system designer to maximize the benefits of using the module. Also included are recommendations on how to use the Presence Detect pins in system design to enable the system to sense the installed DRAM module type (additional details are found in the individual data sheets).

Prior to designing or specifying any memory subsystem, the designer should become familiar with the timing characteristics of the DRAM modules to be used. Although some DRAM modules appear to be compatible from an architectural and pinout perspective, they may not have identical timing characteristics. Often differences in DRAM modules can be accommodated by careful design of memory controller but a thorough timing analysis involving all of the anticipated DRAM modules is essential to ensure a robust, reliable, trouble-free system.

Glossary

The following is a mini-glossary of computer memory terms that have a particular significance when used in connection with DRAM modules:

Parity

Parity is generally applied on a byte-wide basis, e.g., a 4-byte SIMM will have four, 8-bit bytes plus one parity bit per each byte. (Refer to Byte-write) By necessity, parity, as opposed to a non-parity DRAM modules, have additional DRAM chips and additional cost. Parity is useful to assist in diagnosis of the sources of system problems. This guards against inaccurate data processing and unexplained system hangs.

Byte-write

CPUs can perform memory operations involving less than the full data bus width. For example, a so-called 4-byte processor will fetch or store, one, two, three or all four bytes. This requires the DRAM module architecture to support operations such that some bytes may be masked during store operations so that only particular bytes will be accessed, hence the term "Byte-write". Industry Standard DRAM modules designed for Byte-write applications, have individual CAS- addressable data bytes.

Presence Detect and ID Pins

Pins defined to permit the interfacing system to derive information such as speed, density, ECC, parity or functional information about each DRAM module plugged into a socket. The information provided by these pins is in accordance with established, JEDEC standards and can be exploited to allow the system to automatically configure the memory system.

ECC-Optimized

Some systems employed in particular mission-critical applications require memory fault tolerance via ECC (error correction code) techniques. ECC results in memory operations being carried out across all data bits and check bits simultaneously. Since there is no need for byte-write capability, the module's addressing architecture is unique to ECC operations, hence the term, ECC-optimized.

Check Bits

Extra data bits provided by a DRAM Module to support ECC function. In the case of 4 data bytes, this can be 7 or 8 bits producing 39 or 40 data bits. For 8 data bytes, 8 additional bits results in a total of 72 bits. (Refer to ECC-optimized)

ECC-on-Simm (EOS)

These SIMMs are designed to be plug compatible with parity based SIMMs but include on-board ECC logic that corrects single-DRAM errors in each byte of SIMM data. System memory data I/O operations via the SIMM are performed on a parity basis, with the on-board ECC features being transparent. These SIMMs provide a convenient way of upgrading a system to fault-tolerant capability without system alterations.

Low Power

A growing percentage of systems require low-power memory for portable and "green" or environmentally conscious computers. Low Power implies that DRAM chips with extended memory retention, or self-refresh capability that result in very low power supply currents, are used on the module.

Voltage Keying

Some DRAM modules are equipped with special notches, or keys, to ensure that they can only be plugged into systems with the appropriate power supply. 3.3V DRAMs will not work and are subject to damage if plugged into 5V systems.

72 Pin SIMM Design Considerations

The table on page 1358 is a listing of the pinout of all 4 types of 72 pin SIMMs with those pins that have different usage identified. The following explains the differences in more detail:

Data (DQ) Pins.

Most pinout differences occur in the DQ assignments, although the impact of these differences is not as large as might appear at first glance. Parity and non-parity SIMMs differ only in that the non-parity modules lack the parity bits, that are assigned as follows:

$\overline{CAS}$	DQ BITS (x32, x36)	PARITY BIT (x36 ONLY)
0	0 - 7	8
1	9 - 16	17
2	18 - 25	26
3	27 - 34	35

This implies that a system can easily be designed to accommodate either parity or non-parity SIMMs.

Eight-byte ECC systems are implemented with a total of 64 data bits and 8 check bits, or a total of 72 data bits. Two 36-bit ECC-optimized SIMMs are used in parallel in these applications. Four-byte ECC systems involve 32 data bits and 7, or 8 check bits, which is supported by x40 ECC-optimized SIMMs.

The DQ pins on ECC SIMMs are assigned differently since these SIMM's do not have $\overline{CAS}$- controllable individual bytes. (Note that a x40 ECC SIMM has an additional 4 DQ pins more than a x36 parity or ECC SIMM.) A specific memory subsystem can be designed to support either parity or ECC. This enables a single system to be utilized in multiple ways. Although there appears to be a significant difference in the ECC and parity data pins, this is due to identification numbering schemes. This is easily accommodated by making the proper design provisions in the interfacing memory controller.

Control Architecture

The following lists the key differences in basic addressing data word and byte selection organization:

- ECC-optimized SIMMs do not have addressable words and use $\overline{RAS}0$ for the first bank and $\overline{RAS}1$ for the second bank. These SIMMs also do not have addressable bytes and use $\overline{CAS}0$ for the first bank and $\overline{CAS}1$ for the second bank.
- Parity and non-parity organized SIMMs have individual addressable bytes via the 4 $\overline{CAS}$ signals. They also have 2-byte addressable words via $\overline{RAS}$ signals. This permits the use of these SIMMs in 2-byte processor based systems. $\overline{RAS}0$ and $\overline{RAS}2$ select the words in the first bank while $\overline{RAS}1$ and $\overline{RAS}3$ select the second-bank words, if the SIMM is so equipped.
- Note that the ECC SIMMs do not need $\overline{RAS}2$, $\overline{RAS}3$, $\overline{CAS}2$ or $\overline{CAS}3$.

DRAM Addressing Effects

Modules based on DRAM chips organized 1 Mb deep (e.g., a 4 Mb chip organized 1 Mbx4) utilize 10 row and 10 column address bits, identified as A0 through A9. Modules using DRAM chips organized 4Mb deep need 22 address bits. Some of these chips are organized as 12 row and 10 column bits, labeled A0 through A11 and some are organized as 11 row and 11 column bits, A0 through A10[1]. Note that A10 and A11 occur at different pins on ECC and parity and non-parity based SIMMs.

Memory refresh problems will occur if all of the required row columns are not refreshed. The memory system designer is advised to ensure the memory refresh generation portion of the memory controller logic correctly accommodates the requirements of all of the SIMMs to be supported. Refresh period and row address requirements are not the same for all 72 pin SIMMs. DRAM chip cell retention has been designed so that modules based on 1Mb

1. Sometimes referred to as symmetrical, or square addressing.

72 Pin SIMM Pin Assignments

Pin #.	Non-Parity	Parity	ECC Optimized		Pin #	Non-Parity	Parity	ECC Optimized	
	X 32	X 36	X 36	X 40		X 32	X 36	X 36	X 40
1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	*37	-	PQ17	DQ19	DQ19
2	DQ0	DQ0	DQ0	DQ0	*38	-	PQ35	DQ20	DQ20
3	DQ18	DQ18	DQ1	DQ1	39	V_{SS}	V_{SS}	V_{SS}	V_{SS}
4	DQ1	DQ1	DQ2	DQ2	40	$\overline{CAS0}$	$\overline{CAS0}$	$\overline{CAS0}$	$\overline{CAS0}$
5	DQ19	DQ19	DQ3	DQ3	*41	$\overline{CAS2}$	$\overline{CAS2}$	A10	A10
6	DQ2	DQ2	DQ4	DQ4	*42	$\overline{CAS3}$	$\overline{CAS3}$	A11	A11
7	DQ20	DQ20	DQ5	DQ5	43	$\overline{CAS1}$	$\overline{CAS1}$	$\overline{CAS1}$	$\overline{CAS1}$
8	DQ3	DQ3	DQ6	DQ6	44	$\overline{RAS0}$	$\overline{RAS0}$	$\overline{RAS0}$	$\overline{RAS0}$
9	DQ21	DQ21	DQ7	DQ7	45	$\overline{RAS1}$	$\overline{RAS1}$	$\overline{RAS1}$	$\overline{RAS1}$
10	V_{CC}	V_{CC}	V_{CC}	V_{CC}	*46	-	-	DQ21	DQ21
*11	-	-	PD5	PD5	47	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$
12	A0	A0	A0	A0	*48	-	-	$\overline{ECC}$	$\overline{ECC}$
13	A1	A1	A1	A1	49	DQ9	DQ9	DQ22	DQ22
14	A2	A2	A2	A2	50	DQ27	DQ27	DQ23	DQ23
15	A3	A3	A3	A3	51	DQ10	DQ10	DQ24	DQ24
16	A4	A4	A4	A4	52	DQ28	DQ28	DQ25	DQ25
17	A5	A5	A5	A5	53	DQ11	DQ11	DQ26	DQ26
18	A6	A6	A6	A6	54	DQ29	DQ29	DQ27	DQ27
*19	-	A10	$\overline{OE}$	$\overline{OE}$	55	DQ12	DQ12	DQ28	DQ28
20	DQ4	DQ4	DQ8	DQ8	56	DQ30	DQ30	DQ29	DQ29
21	DQ22	DQ22	DQ9	DQ9	57	DQ13	DQ13	DQ30	DQ30
22	DQ5	DQ5	DQ10	DQ10	58	DQ31	DQ31	DQ31	DQ31
23	DQ23	DQ23	DQ11	DQ11	59	V_{CC}	V_{CC}	V_{CC}	V_{CC}
24	DQ6	DQ6	DQ12	DQ12	60	DQ32	DQ32	DQ32	DQ32
25	DQ24	DQ24	DQ13	DQ13	61	DQ14	DQ14	DQ33	DQ33
26	DQ7	DQ7	DQ14	DQ14	62	DQ33	DQ33	DQ34	DQ34
27	DQ25	DQ25	DQ15	DQ15	63	DQ15	DQ15	DQ35	DQ35
28	A7	A7	A7	A7	*64	DQ34	DQ34	-	DQ36
*29	-	A11	DQ16	DQ16	*65	DQ16	DQ16	-	DQ37
30	V_{CC}	V_{CC}	V_{CC}	V_{CC}	*66	-	-	-	DQ38
*31	A8	A8	A8	A8	67	PD1	PD1	PD1	PD1
32	A9	A9	A9	A9	68	PD2	PD2	PD2	PD2
*33	$\overline{RAS3}$	$\overline{RAS3}$	-	-	69	PD3	PD3	PD3	PD3
*34	$\overline{RAS2}$	$\overline{RAS2}$	-	-	70	PD4	PD4	PD4	PD4
*35	-	PQ26	DQ17	DQ17	*71	-	-	-	DQ39
*36	-	PQ8	DQ18	DQ18	72	V_{SS}	V_{SS}	V_{SS}	V_{SS}

*Indicates differences (DQs are scrambled)

and 4Mb-deep DRAMS are compatible in the same system. This is possible because the longer cell retention in 4Mb chips compensates for the additional number of row cycles.

Presence Detect Considerations

Presence Detects can provide the following benefits:

- Determine if any SIMM is present.
- Determine module density and generate proper addressing and refresh requirements as appropriate.
- Determine DRAM module speed
- Determine if non-ECC or ECC to provide proper addressing and DQ interpretation.
- Protect against incorrect speed SIMM plugged in.
- Ensure all installed SIMMs are the same type.

The table on page 1360 shows the listing for the 72 pin SIMM family. Presence detect ouputs must be tied to V_{CC} through a pullup resistor to generate a high-logic level when the SIMM PD pin is open or low-voltage when the PD pin is grounded. This produces the required logical signals decodable by the interfacing logic. The Presence Detect circuitry does not permit "dotting" of signals. If a particular system supports multiple SIMM sockets, then MUX methods can be employed to minimize the memory support chip pins used for Presence Detect inputs from multiple SIMM sockets.

If Presence Detect signals are employed, then the system user is freed, to some extent, of having to follow complex SIMM installation instructions and limitations spelled out in the operations manual. In addition, a systems power-up test procedure can be employed to perform memory tests to determine the memory present and/or the number of memory banks on an installed SIMM and adjust control and addressing signals as necessary.

72 Pin SIMM Presence Detect Truth Table

Pin #		48	67	68	69	70	11
Organization	t_{RAC}	$\overline{ECC}$	PD1	PD2	PD3	PD4	#PD5
256K x32, x 36, x40	100 ns	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	NC
	80 ns	V_{SS}	V_{SS}	NC	NC	V_{SS}	NC
	70 ns	V_{SS}	V_{SS}	NC	V_{SS}	NC	NC
	60 ns	V_{SS}	V_{SS}	NC	NC	NC	NC
512K x32, x 36, x40	100 ns	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	NC
	80 ns	V_{SS}	NC	V_{SS}	NC	V_{SS}	NC
	70 ns	V_{SS}	NC	V_{SS}	V_{SS}	NC	NC
	60 ns	V_{SS}	NC	V_{SS}	NC	NC	NC
1M x32, x 36, x40	100 ns	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC
	80 ns	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	NC
	70 ns	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC
	60 ns	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
2M x32, x 36, x40	100 ns	V_{SS}	NC	NC	V_{SS}	V_{SS}	NC
	80 ns	V_{SS}	NC	NC	NC	V_{SS}	NC
	70 ns	V_{SS}	NC	NC	V_{SS}	NC	NC
	60 ns	V_{SS}	NC	NC	NC	NC	NC
4M x32, x 36, x40	80 ns	V_{SS}	V_{SS}	NC	NC	V_{SS}	V_{SS}
	70 ns	V_{SS}	V_{SS}	NC	V_{SS}	NC	V_{SS}
	60 ns	V_{SS}	V_{SS}	NC	NC	NC	V_{SS}
	50 ns	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}
8M x32, x 36, x40	80 ns	V_{SS}	NC	V_{SS}	NC	V_{SS}	V_{SS}
	70 ns	V_{SS}	NC	V_{SS}	V_{SS}	NC	V_{SS}
	60 ns	V_{SS}	NC	V_{SS}	NC	NC	V_{SS}
	50 ns	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}

NC=Open circuit (No connections)

$\overline{ECC}$ Pin: V_{SS} for ECC Module, NC for NON ECC Module

PD5 applies only to ECC-Optimized SIMMs. For this PD only, the SIMM PD will be grounded through a 2.6K Ω resistor.

Basic Architecture

A listing of the 168 Pin DIMM Pin Assignments begins on page 1362.

Intended primarily for use in 8-byte systems, although use in 4-byte systems is supported via on-board interleave, the basic structure of 168 pin DIMMs is organized by assignment of the data, $\overline{RAS}$, $\overline{CAS}$, and to a lesser degree, $\overline{WE}$ and $\overline{OE}$ pins. Bank width is defined as being one DRAM chip deep by the following data bus width:

DIMM type	Data bus width
Non-Parity	64
Parity	72
ECC-Optimized (8 byte)	72
ECC-Optimized (4 byte)	80

If a DIMM has two banks, the corresponding data I/Os from each bank are dotted. Banks are divided into words, 0 and 2, selectable by $\overline{RAS}$0 and $\overline{RAS}$2 on the first bank, and if so equipped, $\overline{RAS}$1 and $\overline{RAS}$3 on the second bank. Data pins are assigned to words as in the following table (note the DRAM chip organization affects DQ assignments on 8-byte ECC modules):

DIMM TYPE	Word0 Data	Word2 Data
Non-Parity	DQ0-7, 9-16, 18-25, 27-34	DQ36-43, 45-52, 54-61, 63-70
Parity	Above DQs plus PQ8, 17, 26, 35	Above DQs plus PQ44, 53, 62, 71
ECC,8-byte (x4, x9, x18 chips) (x8 chips)	DQ0-35 DQ0-39	DQ36-71 DQ40-71
ECC, 4-byte	DQ0-39	DQ40-79

On parity and non-parity DIMMs, the words are divided into bytes, selectable by $\overline{CAS}$0-3 in Word0 and $\overline{CAS}$4-7 on Word2. The same $\overline{CAS}$ signals are assigned to the second bank's bytes if present on the DIMM. ECC DIMMs do not have addressable bytes and utilize $\overline{CAS}$ as follows (note the difference depending on DRAM chip type on 8-byte modules).

Bank	$\overline{CAS}$	Data Bit Assignments (DRAM CHIPS)		
		8-Byte (x4, x9, x18)	8-Byte (x8)	4-Byte (x4, x8)
1	0	DQ0-35	DQ0-39	DQ0-39
1	4	DQ36-71	DQ40-71	DQ40-79
2	1	DQ0-35	DQ0-39	DQ0-39
2	5	DQ36-71	DQ40-71	DQ40-79

Memory systems can be configured to support any and all types of 168 pin DIMM types. There is more consistency between 168 pin DIMM pinouts than on 72 pin SIMMs, greatly facilitating design of a flexible memory subsystem.

Buffered Inputs

All 168 pin DIMM signals except $\overline{RAS}$ and data signals are buffered via on-board, high performance logic modules. $\overline{RAS}$ and data signals are not buffered which preserves the basic t_{RAC} access specification of the DRAM chips. Capacitive loading of the other signals is reduced which reduces the need for "glue" logic in the memory sub-system. The DIMMs specified timings include all buffer, net and skew delays. Buffer propagation delay is a maximum of 5 ns.

DRAM Addressing Effects

The 168 pin DIMM has been architected to provide for a multitude of potential DRAM chip depth granularities as follows

DRAM Chip Depth (Mb)	Row Addresses	Column Addresses	Cell Retention (ms)
1	A0-A9	A0-A9	16
2	A0-A10	A0-A10	32
4	A0-A10 or A0-A11	A0-A10 or A0-A9	32 or 64
8	A0-A11	A0-A10	64
16	A0-A12	A0-A10	128

Memory refresh problems will occur if all of the required rows columns are not refreshed. The memory system designer is advised to ensure the memory refresh generation portion of the memory

168 PIN DIMM PIN ASSIGNMENTS (Part 1 of 3)

Front Side (left side 1-42, right side 43-84)					Back Side (left side 85-126, right side 127-168)				
Pin #	x64 Non-Parity	x72 Parity	x72 ECC	x80 ECC	Pin #	x64 Non-Parity	x72 Parity	x72 ECC	x80 ECC
1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	85	V_{SS}	V_{SS}	V_{SS}	V_{SS}
2	DQ0	DQ0	DQ0	DQ0	86	DQ36	DQ36	DQ36	DQ40
3	DQ1	DQ1	DQ1	DQ1	87	DQ37	DQ37	DQ37	DQ41
4	DQ2	DQ2	DQ2	DQ2	88	DQ38	DQ38	DQ38	DQ42
5	DQ3	DQ3	DQ3	DQ3	89	DQ39	DQ39	DQ39	DQ43
6	V_{CC}	V_{CC}	V_{CC}	V_{CC}	90	V_{CC}	V_{CC}	V_{CC}	V_{CC}
7	DQ4	DQ4	DQ4	DQ4	91	DQ40	DQ40	DQ40	DQ44
8	DQ5	DQ5	DQ5	DQ5	92	DQ41	DQ41	DQ41	DQ45
9	DQ6	DQ6	DQ6	DQ6	93	DQ42	DQ42	DQ42	DQ46
10	DQ7	DQ7	DQ7	DQ7	94	DQ43	DQ43	DQ43	DQ47
*11	NC	PQ8	DQ8	DQ8	*95	NC	PQ44	DQ44	DQ48
12	V_{SS}	V_{SS}	V_{SS}	V_{SS}	96	V_{SS}	V_{SS}	V_{SS}	V_{SS}
13	DQ9	DQ9	DQ9	DQ9	97	DQ45	DQ45	DQ45	DQ49
14	DQ10	DQ10	DQ10	DQ10	98	DQ46	DQ46	DQ46	DQ50
15	DQ11	DQ11	DQ11	DQ11	99	DQ47	DQ47	DQ47	DQ51
16	DQ12	DQ12	DQ12	DQ12	100	DQ48	DQ48	DQ48	DQ52
17	DQ13	DQ13	DQ13	DQ13	101	DQ49	DQ49	DQ49	DQ53
18	V_{CC}	V_{CC}	V_{CC}	V_{CC}	102	V_{CC}	V_{CC}	V_{CC}	V_{CC}
19	DQ14	DQ14	DQ14	DQ14	103	DQ50	DQ50	DQ50	DQ54
20	DQ15	DQ15	DQ15	DQ15	104	DQ51	DQ51	DQ51	DQ55
21	DQ16	DQ16	DQ16	DQ16	105	DQ52	DQ52	DQ52	DQ56
*22	NC	PQ17	DQ17	DQ17	*106	NC	PQ53	DQ53	DQ57
23	V_{SS}	V_{SS}	V_{SS}	V_{SS}	107	V_{SS}	V_{SS}	V_{SS}	V_{SS}
*24	NC	NC	NC	DQ18	*108	NC	NC	NC	DQ58
*25	NC	NC	NC	DQ19	*109	NC	NC	NC	DQ59
26	V_{CC}	V_{CC}	V_{CC}	V_{CC}	110	V_{CC}	V_{CC}	V_{CC}	V_{CC}
27	$\overline{WE0}$	$\overline{WE0}$	$\overline{WE0}$	$\overline{WE0}$	111	NC	NC	NC	NC
28	$\overline{CAS0}$	$\overline{CAS0}$	$\overline{CAS0}$	$\overline{CAS0}$	112	$\overline{CAS1}$	$\overline{CAS1}$	$\overline{CAS1}$	$\overline{CAS1}$
*29	$\overline{CAS2}$	$\overline{CAS2}$	NC	NC	*113	$\overline{CAS3}$	$\overline{CAS3}$	NC	NC
30	$\overline{RAS0}$	$\overline{RAS0}$	$\overline{RAS0}$	$\overline{RAS0}$	114	$\overline{RAS1}$	$\overline{RAS1}$	$\overline{RAS1}$	$\overline{RAS1}$
31	$\overline{OE0}$	$\overline{OE0}$	$\overline{OE0}$	$\overline{OE0}$	115	NC	NC	NC	NC
32	V_{SS}	V_{SS}	V_{SS}	V_{SS}	116	V_{SS}	V_{SS}	V_{SS}	V_{SS}
33	A0	A0	A0	A0	117	A1	A1	A1	A1
34	A2	A2	A2	A2	118	A3	A3	A3	A3
35	A4	A4	A4	A4	119	A5	A5	A5	A5
36	A6	A6	A6	A6	120	A7	A7	A7	A7

* Indicates Differences (DQ's are scrambled)

168 PIN DIMM PIN ASSIGNMENTS (Part 2 of 3)

Front Side (left side 1-42, right side 43-84)					Back Side (left side 85-126, right side 127-168)				
Pin #	x64 Non-Parity	x72 Parity	x72 ECC	x80 ECC	Pin #	x64 Non-Parity	x72 Parity	x72 ECC	x80 ECC
37	A8	A8	A8	A8	121	A9	A9	A9	A9
38	A10	A10	A10	A10	122	A11	A11	A11	A11
39	A12	A12	A12	A12	123	A13	A13	A13	A13
40	V_{CC}	V_{CC}	V_{CC}	V_{CC}	124	V_{CC}	V_{CC}	V_{CC}	V_{CC}
41	NC	NC	NC	NC	125	NC	NC	NC	NC
42	NC	NC	NC	NC	126	B0	B0	B0	B0
43	V_{SS}	V_{SS}	V_{SS}	V_{SS}	127	V_{SS}	V_{SS}	V_{SS}	V_{SS}
44	$\overline{OE2}$	$\overline{OE2}$	$\overline{OE2}$	$\overline{OE2}$	128	NC	NC	NC	NC
45	$\overline{RAS2}$	$\overline{RAS2}$	$\overline{RAS2}$	$\overline{RAS2}$	129	$\overline{RAS3}$	$\overline{RAS3}$	$\overline{RAS3}$	$\overline{RAS3}$
46	$\overline{CAS4}$	$\overline{CAS4}$	$\overline{CAS4}$	$\overline{CAS4}$	130	$\overline{CAS5}$	$\overline{CAS5}$	$\overline{CAS5}$	$\overline{CAS5}$
*47	$\overline{CAS6}$	$\overline{CAS6}$	NC	NC	*131	$\overline{CAS7}$	$\overline{CAS7}$	NC	NC
48	$\overline{WE2}$	$\overline{WE2}$	$\overline{WE2}$	$\overline{WE2}$	132	$\overline{PDE}$	$\overline{PDE}$	$\overline{PDE}$	$\overline{PDE}$
49	V_{CC}	V_{CC}	V_{CC}	V_{CC}	133	V_{CC}	V_{CC}	V_{CC}	V_{CC}
*50	NC	NC	NC	DQ20	*134	NC	NC	NC	DQ60
*51	NC	NC	NC	DQ21	*135	NC	NC	NC	DQ61
52	DQ18	DQ18	DQ18	DQ22	136	DQ54	DQ54	DQ54	DQ62
53	DQ19	DQ19	DQ19	DQ23	137	DQ55	DQ55	DQ55	DQ63
54	V_{SS}	V_{SS}	V_{SS}	V_{SS}	138	V_{SS}	V_{SS}	V_{SS}	V_{SS}
55	DQ20	DQ20	DQ20	DQ24	139	DQ56	DQ56	DQ56	DQ64
56	DQ21	DQ21	DQ21	DQ25	140	DQ57	DQ57	DQ57	DQ65
57	DQ22	DQ22	DQ22	DQ26	141	DQ58	DQ58	DQ58	DQ66
58	DQ23	DQ23	DQ23	DQ27	142	DQ59	DQ59	DQ59	DQ67
59	V_{CC}	V_{CC}	V_{CC}	V_{CC}	143	V_{CC}	V_{CC}	V_{CC}	V_{CC}
60	DQ24	DQ24	DQ24	DQ28	144	DQ60	DQ60	DQ60	DQ68
61	NC	NC	NC	NC	145	NC	NC	NC	NC
62	NC	NC	NC	NC	146	NC	NC	NC	NC
63	NC	NC	NC	NC	147	NC	NC	NC	NC
64	NC	NC	NC	NC	148	NC	NC	NC	NC
65	DQ25	DQ25	DQ25	DQ29	149	DQ61	DQ61	DQ61	DQ69
66	NC	PQ26	DQ26	DQ30	150	NC	PQ62	DQ62	DQ70
67	DQ27	DQ27	DQ27	DQ31	151	DQ63	DQ63	DQ63	DQ71
68	V_{SS}	V_{SS}	V_{SS}	V_{SS}	152	V_{SS}	V_{SS}	V_{SS}	V_{SS}
69	DQ28	DQ28	DQ28	DQ32	153	DQ64	DQ64	DQ64	DQ72
70	DQ29	DQ29	DQ29	DQ33	154	DQ65	DQ65	DQ65	DQ73
71	DQ30	DQ30	DQ30	DQ34	155	DQ66	DQ66	DQ66	DQ74
72	DQ31	DQ31	DQ31	DQ35	156	DQ67	DQ67	DQ67	DQ75
73	V_{CC}	V_{CC}	V_{CC}	V_{CC}	157	V_{CC}	V_{CC}	V_{CC}	V_{CC}

* Indicates Differences (DQ's are scrambled)

168 PIN DIMM PIN ASSIGNMENTS (Part 3 of 3)

Front Side (left side 1-42, right side 43-84)					Back Side (left side 85-126, right side 127-168)				
Pin #	x64 Non-Parity	x72 Parity	x72 ECC	x80 ECC	Pin #	x64 Non-Parity	x72 Parity	x72 ECC	x80 ECC
74	DQ32	DQ32	DQ32	DQ36	158	DQ68	DQ68	DQ68	DQ76
75	DQ33	DQ33	DQ33	DQ37	159	DQ69	DQ69	DQ69	DQ77
76	DQ34	DQ34	DQ34	DQ38	160	DQ70	DQ70	DQ70	DQ78
77	NC	PQ35	DQ35	DQ39	*161	NC	PQ71	DQ71	DQ79
78	V_{SS}	V_{SS}	V_{SS}	V_{SS}	162	V_{SS}	V_{SS}	V_{SS}	V_{SS}
79	PD1	PD1	PD1	PD1	163	PD2	PD2	PD2	PD2
80	PD3	PD3	PD3	PD3	164	PD4	PD4	PD4	PD4
81	PD5	PD5	PD5	PD5	165	PD6	PD6	PD6	PD6
82	PD7	PD7	PD7	PD7	166	PD8	PD8	PD8	PD8
83	ID0	ID0	ID0	ID0	167	ID1	ID1	ID1	ID1
84	V_{CC}	V_{CC}	V_{CC}	V_{CC}	168	V_{CC}	V_{CC}	V_{CC}	V_{CC}

* Indicates Differences (DQ's are scrambled)

controller logic correctly accommodates the requirements of all the DIMMs to be supported. Also, different page depths due to different column address requirements must be accounted for.

Voltage Keying

The diagram below shows the keying methodology employed on 8-byte DIMMs.

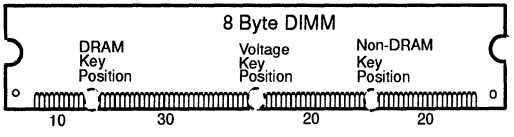
One key defines DRAM type and one key defines voltage. This key provides a positive interlock so that DIMMs can only be plugged into a system with the proper supply voltage, reducing potential damage to the module DRAM chips. Unless the designer chooses the appropriate connector the system will not work.

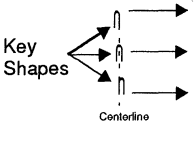
Presence Detect Considerations

Presence Detects can provide the following benefits:

- Determine if any DIMM is present.
- Determine module density and generate proper addressing and refresh requirements as appropriate.
- Determine DRAM module speed
- Determine if non-ECC or ECC to provide proper addressing and DQ interpretation.
- Protect against incorrect speed DIMM plugged in.
- Ensure all installed DIMMs are the same type.

168 Pin DIMM Keying Methodology





Left Key	Center Key	* Right Key
SDRAM	5V	No Key
St'd DRAM	3.3V	No Key
RFU	x.xV	No Key

* For DRAM/SDRAM assemblies, this area is populated with pads.

The table on page 1367 presents the complete listing of 168 pin DIMM presence detects and configurations. PD values are optimized for use in systems which allow "bussed" PDs to reduce system board wiring. On-board buffers can gate the PD data onto a common "PD Bus" in the system if desired. The PD bits can be gated onto the PD bus via use of the $\overline{\text{PDE}}$, or PD enable, signal when at low-level. The system can read one DIMM socket data at a time via enabling the appropriate $\overline{\text{PDE}}$ bit or, if all $\overline{\text{PDE}}$ bits are tied to ground, then it may read separate PD lines from each DIMM.

ID bits are designed such that they may also be bussed, although they are not buffered on-board the DIMM. The modes are defined so these pins may be "dotted", if desired, to provide information on the entire DIMM bank. This is very useful, for example, to test if all installed DIMMs are ECC or not. Note also that if a system wants to run in Self- refresh mode, all installed DIMMs must support this feature, if not, ID1 will be grounded.

If Presence Detect signals are employed, then the system user is freed, to some extent, of having to follow complex DIMM installation instructions and limitations spelled out in the operations manual. In addition, a systems power-up test procedure can be employed to perform memory tests to determine the memory present and/or the number of memory banks on an installed DIMM and adjust control and addressing signals as necessary.

168 Pin DIMM Presence Detect

PD Bits				DIMM Density MB	# Banks	DIMM Configuration	DRAM Configuration	DRAM Address	
4	3	2	1					Row	Column
164	80	163	79						
NC	NC	NC	NC			No Module Inserted			
V_{SS}	V_{SS}	V_{SS}	V_{SS}	2	1	256K x64/72, 256K x72	256K x 16/18	9	9
V_{SS}	V_{SS}	V_{SS}	NC	4	2	512K x64/72, 512K x72	256K x 16/18	9	9
V_{SS}	V_{SS}	NC	V_{SS}	4	1	512K x 64/72, 512K x 72/80	512K x 8/9	10	9
V_{SS}	V_{SS}	NC	NC	8	2	1Mx64/72, 1Mx72/80	512K x 8/9	10	9
V_{SS}	NC	V_{SS}	V_{SS}	8	1	1Mx64/72, 1Mx72/80	1M x 4/16/18	10	10*
V_{SS}	NC	V_{SS}	NC	16	2	2Mx64/72, 2Mx72/80	1M x 4/16/18	10	10*
V_{SS}	NC	NC	V_{SS}	8	1	1Mx64/72, 1Mx72	1M x 16/18	12	8
NC	V_{SS}	V_{SS}	V_{SS}	16	2	2Mx64/72, 2Mx72	1M x 16/18	12	8
NC	V_{SS}	V_{SS}	NC	16	1	2Mx64/72, 2Mx72/80	2M x 8/9	11	10
NC	V_{SS}	NC	V_{SS}	32	2	4Mx64/72, 4Mx72/80	2M x 8/9	11	10
NC	V_{SS}	NC	NC	32	1	4Mx72, N/A	4M x 4/1/18	12	11
NC	V_{SS}	NC	NC	32	1	4Mx64, 4Mx72/80	4M x 4/16	12	10
NC	NC	V_{SS}	V_{SS}	64	2	8Mx64/72, 8Mx72	4M x 16/18	12	10
NC	NC	V_{SS}	NC	64	1	8Mx64/72, 8Mx72/80	8M x 8/9	12	11
NC	NC	NC	V_{SS}	128	2	16Mx64/72, 16Mx72/80	8M x 8/9	12	11
NC	NC	NC	NC	128	1	16Mx64/72, 16Mx72/80	16M x 4	13	11
V_{SS}	V_{SS}	V_{SS}	V_{SS}	128	1	16Mx64/72, 16Mx72	16M x 16/18	TBD	TBD
V_{SS}	V_{SS}	V_{SS}	NC	256	2	32Mx64/72, 32Mx72	16M x 16/18	TBD	TBD
V_{SS}	V_{SS}	NC	V_{SS}	256	1	32Mx64/72, 32Mx72/80	32M x 8/9	TBD	TBD
V_{SS}	V_{SS}	NC	NC	512	2	64Mx64/72, 64Mx72/80	32M x 8/9	TBD	TBD
V_{SS}	NC	V_{SS}	V_{SS}	512	1	64Mx64/72, 64Mx72/80	64M x 4	TBD	TBD
V_{SS}	NC	NC	NC	EXPANSION CODE					

* 1M x 16/18 DRAMS with 10/10 Addressing may dissipate excessive power in some applications. Care must be taken to ensure device thermal limits are not exceeded. The 12/8 decode is provided as a low power option.

EDO Detection

PD Bit		Fast Page	Fast Page with EDO
PD 5	81	V_{SS}	NC

DIMM Speed (T_{RAC})

PD Bit		40 ns	50 ns	60 ns	70 ns	80 ns
PD 6	165	NC	V_{SS}	NC	V_{SS}	NC
PD 7	82	V_{SS}	V_{SS}	NC	NC	V_{SS}

ECC/Parity Detection

PD Bit		ECC	Parity
PD 8	166	V_{SS}	NC

ID BITS (May be "Dot-ORed" at system level)

		x 64 Parity/x72 ECC	x 72 Parity/x 80 ECC
ID0 (DIMM Type)	83	V_{SS}	NC

		Normal Refresh	Self Refresh
ID1 (Refresh Mode)	167	V_{SS}	NC

Basic Architecture

A listing of the 88 Pin IC DRAM Card Pin Assignments is on page 1370 .

The small size of these cards, which conforms to the JEDEC/PCMCIA/JEIDA 88-pin standard, together with low-power features makes them useful in portable, add-on memory applications. They can be used in 4-byte systems with support for 2-byte systems provided via 2-byte interleave. As in other DRAM modules, banks are defined as being one DRAM chip deep. Two types of banks are currently available (potential for ECC exists):

IC DRAM Type	Data Bus Width
Non-parity	32
Parity	36

In 2-banked IC DRAMs, the data I/O for each bank are dotted. Banks are divided into words, 0 and 2, selectable by $\overline{RAS0}$ and $\overline{RAS2}$ on the first bank, and if so equipped, $\overline{RAS1}$ and $\overline{RAS3}$ on the second bank. Data pins are assigned to words as:

IC DRAM Type	Word0 Data	Word2 Data
Non-parity	DQ0 - 16	DQ18 - 34
Parity	DQ0 - 8 plus PQ8 DQ9 - 16 plus PQ17	DQ18 - 25 plus PQ26 DQ27 - 43 plus PQ35

On parity and non-parity cards, words are divided into two bytes, selectable by $\overline{CAS0}$ and $\overline{CAS1}$ in Word0 and $\overline{CAS2}$ and $\overline{CAS3}$ in Word2. The same $\overline{CAS}$ signals are assigned to the second bank's bytes if present on the card.

Memory systems can be configured to support both types of cards. Note: the only pin difference in the two card types, is on the parity IC DRAM's where extra data pins are used for parity purposes.

DRAM Addressing Effects

IC DRAM cards are designed to provide for a multitude of potential DRAM chip depth granularities as shown in the following table:

DRAM Chip Depth (Mb)	Row Addresses	Column Addresses	Cell Retention (ms)
0.25 (256K)	A0 - A8	A0 - A8	64
.5 (512K)	A0 - A9	A0 - A8	128
1	A0 - A9 or A0 - A11	A0 - A9 or A0 - A7	128
2	A0 - A10	A0 - A9	128
4	A0 - A11 or A0 - A11	A0 - A9 or A0 - A10	256

Memory refresh is of particular importance on IC DRAM cards due to their use in portable applications. The memory system designer is advised to ensure the memory refresh generation portion of the memory controller logic correctly accommodates the requirements of all the cards desired to be supported. Also, different page depths due to different column address requirements must be accounted for.

88 Pin IC DRAM Card Pin Assignments

Pin #	Top Side x 32	Top Side x 36	Pin #	Bottom Side x 32	Bottom Side x 36
1	V_{SS}	V_{SS}	45	V_{SS}	V_{SS}
2	DQ0	DQ0	46	DQ18	DQ18
3	DQ1	DQ1	47	DQ19	DQ19
4	DQ2	DQ2	48	DQ20	DQ20
5	DQ3	DQ3	49	DQ21	DQ21
6	DQ4	DQ4	50	DQ22	DQ22
7	DQ5	DQ5	51	DQ23	DQ23
8	DQ6	DQ6	52	DQ24	DQ24
9	V_{CC} (5.0V)	V_{CC} (5.0V)	53	DQ25	DQ25
10	DQ7	DQ7	*54	-	PQ26
11	V_{CC} (3.3V)	V_{CC} (3.3V)	55	**NC	**NC
*12	-	PQ8	56	Vss	Vss
13	A0	A0	57	A1	A1
14	A2	A2	58	A3	A3
15	V_{CC} (5.0V)	V_{CC} (5.0V)	59	A5	A5
16	A4	A4	60	A7	A7
17	V_{CC} (3.3V)	V_{CC} (3.3V)	61	A9	A9
18	A6	A6	62	A11	A11
19	A8	A8	63	V_{SS}	V_{SS}
20	A10	A10	64	A13	A13
21	A12	A12	65	RAS1	RAS1
22	RAS0	RAS0	66	CAS2	CAS2
23	CAS0	CAS0	67	V_{SS}	V_{SS}
24	CAS1	CAS1	68	CAS3	CAS3
25	V_{CC} (3.3V)	V_{CC} (3.3V)	69	RAS3	RAS3
26	RAS2	RAS2	70	WE	WE
27	V_{CC} (5.0V)	V_{CC} (5.0V)	71	PD1	PD1
28	PD2	PD2	72	PD3	PD3
29	PD4	PD4	73	V_{SS}	V_{SS}
30	PD6	PD6	74	PD5	PD5
31	**RFE	**RFE	75	PD7	PD7
32	**RFE	**RFE	76	PD8	PD8
*33	-	PQ17	77	**RFE	**RFE
34	DQ9	DQ9	78	PD9	PD9
35	V_{CC} (3.3V)	V_{CC} (3.3V)	*79	-	PQ35
36	DQ10	DQ10	80	DQ27	DQ27
37	V_{CC} (5.0V)	V_{CC} (5.0V)	81	DQ28	DQ28
38	DQ11	DQ11	82	DQ29	DQ29
39	DQ12	DQ12	83	DQ30	DQ30
40	DQ13	DQ13	84	DQ31	DQ31
41	DQ14	DQ14	85	DQ32	DQ32
42	DQ15	DQ15	86	DQ33	DQ33
43	DQ16	DQ16	87	DQ34	DQ34
44	V_{SS}	V_{SS}	88	V_{SS}	V_{SS}

*Indicates Differences

**Reserved For Potential ECC Use

Buffered Inputs

All 88 pin IC DRAM signals except $\overline{RAS}$ and data signals are buffered via on-board, high performance logic modules. $\overline{RAS}$ and data signals are not buffered which preserves the basic t_{RAC} access specification of the DRAM chips. Capacitive loading of the other signals is reduced which reduces the need for "glue" logic in the memory sub-system. The IC DRAM's specified timings include all buffer, net and skew delays. Buffer propagation delay is a maximum of 5 ns.

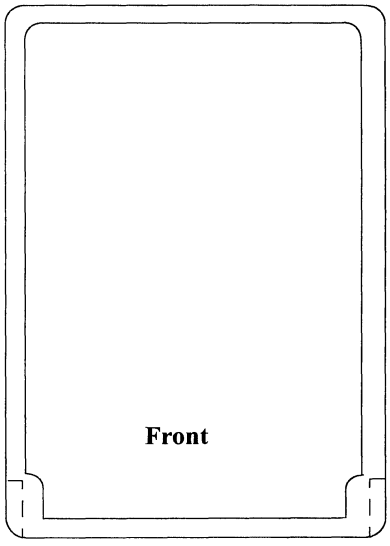
Voltage Keying

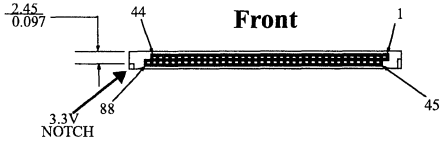
IC DRAM cards do not have voltage keying but the connector is designed to guard against incorrect insertion. Because power supply voltage is assigned different pins for 5V and 3V cards, protection against incorrect voltages is provided. See diagram.

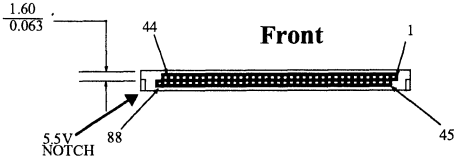
Presence Detect Considerations

The table on page 1372 presents the complete listing of IC DRAM card presence detects and configurations. Note: that due to different DRAM chip technology being used on otherwise similar cards, refresh characteristics can vary. However, decoding of the PDs can be used to indicate the differences.

Voltage Keying







88 Pin IC DRAM Card Presence Detect

PD Bits					Card Density MB	Dram Organization
5	4	3	2	1		
74	29	72	28	71		
NC	NC	NC	NC	NC	No Card	
NC V_{SS}	V_{SS} V_{SS}	V_{SS} V_{SS}	V_{SS} V_{SS}	V_{SS} V_{SS}	1 2	256K x 1, 4, 16, 18 256K x 1, 4, 16, 18
NC V_{SS}	V_{SS} V_{SS}	V_{SS} V_{SS}	V_{SS} V_{SS}	NC NC	2 4	512K x 8, 9 512K x 8, 9
NC V_{SS} NC V_{SS}	V_{SS} V_{SS} NC NC	V_{SS} V_{SS} V_{SS} V_{SS}	NC NC NC NC	V_{SS} V_{SS} V_{SS} V_{SS}	4 8 4 8	1M x 1, 4, 16, 18 1M x 1, 4, 16, 18 1M x 16, 18 1M x 16, 18
NC V_{SS}	V_{SS} V_{SS}	V_{SS} V_{SS}	NC NC	NC NC	8 16	2M x 8, 9 2M x 8, 9
NC V_{SS}	V_{SS} V_{SS}	NC NC	V_{SS} V_{SS}	V_{SS} V_{SS}	16 32	4M x 1, 4, 16, 18 4M x 1, 4, 16, 18
NC V_{SS}	V_{SS} V_{SS}	NC NC	V_{SS} V_{SS}	NC NC	32 64	8M x 8, 9 8M x 8, 9
NC V_{SS}	V_{SS} V_{SS}	NC NC	NC NC	Vss V_{SS}	64 128	16M x 1, 4, 16, 18 16M x 1, 4, 16, 18

PD Speed

	PD7	PD6
SPEED (RAC)	75	30
100 ns	V_{SS}	V_{SS}
80 ns	V_{SS}	NC
70 ns	NC	V_{SS}
60 ns	NC	NC
50 ns	V_{SS}	V_{SS}

PD Refresh

	PD8
Refresh Type	76
Standard	NC
Self Refresh	V_{SS}

PD Page Type

	PD9
Page Type	78
Fast Page	NC
EDO	V_{SS}

Basic Architecture

A listing of the 72 Pin SO DIMM Pin Assignments is on page 1374.

Intended primarily for the emerging low-power market, or any system in which space is at a premium, this new family of DIMMs can be used in 4-byte systems with support for 2-byte systems provided via 2-byte interleave. As in other DRAM modules, banks are defined as being one DRAM chip deep. Two types of banks are available:

SO DIMM	Data Bus Width
Non-parity	32
Parity	36

If a SO DIMM has two banks, then the corresponding data I/Os from each bank are dotted. Banks are divided into words, 0 and 2, selectable by $\overline{RAS0}$ and $\overline{RAS2}$ on the first bank, and if so equipped, $\overline{RAS1}$ and $\overline{RAS3}$ on the second bank.

Data pins are assigned to words as:

DIMM Type	Word0 Data	Word2 Data
Non-parity	DQ0 - 16	DQ18 - 34
Parity	DQ0 - 8 plus PQ8 DQ9 - 16 Plus PQ17	DQ18 - 25 plus PQ26 DQ27 - 43 Plus PQ35

On parity and non-parity SO DIMMs, the words are divided into two bytes, selectable by CAS0 and 1 in Word0 and CAS2 and 3 in Word2. The same CAS signals are assigned to the second bank's bytes if present on the SO DIMM.

Memory systems can be configured to support both types of SO DIMMs. Note the only pin difference in the two types of SO DIMMs is the 4 extra data pins on the parity SO DIMMs used for parity purposes.

DRAM addressing effects

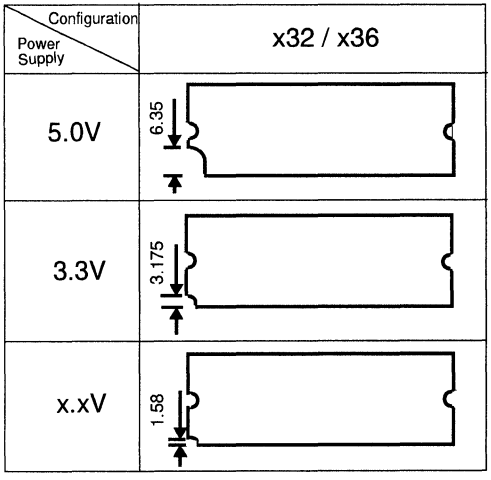
SO DIMMs are designed to provide for a multitude of potential DRAM chip depth granularities as shown in the following table:

DRAM Chip Depth (MB)	Row Addresses	Column Addresses	Cell Retention (ms)
1	A0 - A9	A0 - A9	64
	A0 - A11	A0 - A7	64
2	A0 - A10	A0 - A9	256
4	A0 - A11	A0 - A9	256

Memory refresh is of particular importance on SO DIMMs due to use in portable applications. The memory system designer should ensure the memory refresh generation portion of the memory controller logic correctly accommodates the requirements of all of the SO DIMMs to be supported. Also, different page depths due to different column address requirements must be accounted for.

Mechanical Keying

These SO DIMMs have a different sized notch at the DIMM's left edge of to differentiate between power supplies as is shown below. The purpose of this mechanical keying is to ensure that low-power DIMMs can't be plugged into systems with incorrect power supplies. The designer must select the appropriate connector for the expected SO DIMM.



72 Pin SO DIMM Pin Assignments

Pin #	Front Side X 32	Front Side X 36	Pin #	Back Side X 32	Back Side X 36
1	V_{ss}	V_{ss}	2	DQ0	DQ0
3	DQ1	DQ1	4	DQ2	DQ2
5	DQ3	DQ3	6	DQ4	DQ4
7	DQ5	DQ5	8	DQ6	DQ6
9	DQ7	DQ7	10	V_{cc}	V_{cc}
11	PD1	PD1	12	A0	A0
13	A1	A1	14	A2	A2
15	A3	A3	16	A4	A4
17	A5	A5	18	A6	A6
19	A10	A10	*20	NC	PQ8
21	DQ9	DQ9	22	DQ10	DQ10
23	DQ11	DQ11	24	DQ12	DQ12
25	DQ13	DQ13	26	DQ14	DQ14
27	DQ15	DQ15	28	A7	A7
29	A11	A11	30	V_{cc}	V_{cc}
31	A8	A8	32	A9	A9
33	$\overline{RAS3}$	$\overline{RAS3}$	34	$\overline{RAS2}$	$\overline{RAS2}$
35	DQ16	DQ16	*36	NC	PQ17
37	DQ18	DQ18	38	DQ19	DQ19
39	V_{ss}	V_{ss}	40	$\overline{CAS0}$	$\overline{CAS0}$
41	$\overline{CAS2}$	$\overline{CAS2}$	42	$\overline{CAS3}$	$\overline{CAS3}$
43	$\overline{CAS1}$	$\overline{CAS1}$	44	$\overline{RAS0}$	$\overline{RAS0}$
45	$\overline{RAS1}$	$\overline{RAS1}$	46	A12	A12
47	$\overline{WE}$	$\overline{WE}$	48	A13	A13
49	DQ20	DQ20	50	DQ21	DQ21
51	DQ22	DQ22	52	DQ23	DQ23
53	DQ24	DQ24	54	DQ25	DQ25
*55	NC	PQ26	56	DQ27	DQ27
57	DQ28	DQ28	58	DQ29	DQ29
59	DQ31	DQ31	60	DQ30	DQ30
61	V_{cc}	V_{cc}	62	DQ32	DQ32
63	DQ33	DQ33	64	DQ34	DQ34
*65	NC	PQ35	66	PD2	PD2
67	PD3	PD3	68	PD4	PD4
69	PD5	PD5	70	PD6	PD6
71	PD7	PD7	72	V_{ss}	V_{ss}

*Indicates Differences

Presence Detect Considerations

Presence Detects can provide the following benefits:

- Determine if any SO DIMM is present.
- Determine module density and generate proper addressing and refresh requirements as appropriate.
- Determine DRAM module speed
- Determine if non-ECC or ECC to provide proper addressing and DQ interpretation.
- Protect against incorrect speed SO DIMM plugged in.
- Ensure all installed SO DIMMs are the same type.

The table on page 1376 presents the complete listing of 72 pin SO DIMM presence detects and configurations. SO DIMMs PD characteristics are very similar to those of 72 pin SIMMs except that SO DIMMs have 7 versus 5 PD pins as do 72 pin SIMMs. Also, these 7 PDs contain different coded information.

Presence detect outputs must be tied to V_{CC} through a pullup resistor to generate a high-logic level when the SO DIMM PD pin is open or low-voltage when the PD pin is grounded. This produces the required logical signals decodable by the interfacing logic. The Presence Detect circuitry does not permit "dotting" of signals. If a particular system supports multiple SO DIMM sockets, then MUX methods can be employed to minimize the memory support chip pins used for Presence Detect inputs from multiple SO DIMM sockets.

If Presence Detect signals are employed, then the system user is freed, to some extent, of having to follow complex SO DIMM installation instructions and limitations spelled out in the operations manual. In addition, a systems power-up test procedure can be employed to perform memory tests to determine the memory present and/or the number of memory banks on an installed SO DIMM and adjust control and addressing signals as necessary.

72 PIN SO DIMM Presence Detect

Organization	Chip Organization	Addressing		PD			
		Row	Column	4	3	2	1
				68	67	66	11
No Module				NC	NC	NC	NC
512k x 32	512k x 8	10	9	NC	V_{SS}	V_{SS}	V_{SS}
512k x 36	512k x 9	10	9	NC	V_{SS}	V_{SS}	V_{SS}
1M x 32	512k x 8	10	9	V_{SS}	V_{SS}	V_{SS}	V_{SS}
1M x 32	1M x 4, 16, 18	10	10	NC	V_{SS}	V_{SS}	NC
1M x 36	512k x 9	10	9	V_{SS}	V_{SS}	V_{SS}	V_{SS}
2M x 32	2M x 8	11	10	NC	V_{SS}	NC	V_{SS}
2M x 36	2M x 9	11	10	NC	V_{SS}	NC	V_{SS}
4M x 32	2M x 8	11	10	V_{SS}	V_{SS}	NC	V_{SS}
4M x 32	4M x 4	12,11	10,11	NC	V_{SS}	NC	NC
4M x 36	2M x 9	11	10	V_{SS}	V_{SS}	NC	V_{SS}
8M x 32	8M x 8	12	11	NC	NC	V_{SS}	V_{SS}
8M x 36	8M x 9	12	11	NC	NC	V_{SS}	V_{SS}
16M x 32	8M x 8	12	11	V_{SS}	NC	V_{SS}	V_{SS}
16M x 32	16M x 4	13	11	NC	NC	V_{SS}	NC
16M x 36	8M x 9	12	11	V_{SS}	NC	V_{SS}	V_{SS}
32M x 32	32M x 8	TBD	TBD	NC	NC	NC	V_{SS}
32M x 36	32M x 9	TBD	TBD	NC	NC	NC	V_{SS}
64M x 32	32M x 8	TBD	TBD	V_{SS}	NC	NC	V_{SS}
64M x 32	64M x 4	TBD	TBD	NC	V_{SS}	V_{SS}	V_{SS}
64M x 36	32M x 9	TBD	TBD	V_{SS}	NC	NC	V_{SS}
1M x 32, 36	1M x 16, 18	12	8	NC	NC	V_{SS}	NC
2M x 32, 36	1M x 16, 18	12	8	V_{SS}	NC	V_{SS}	NC
2M x 32, 36	1M x 16, 18	10	10	V_{SS}	V_{SS}	V_{SS}	NC

PD Speed

Speed- t_{RAC}	PD5	PD6
	69	70
50 ns	V_{SS}	V_{SS}
60 ns	NC	NC
70 ns	V_{SS}	NC
80 ns	NC	V_{SS}

PD Refresh

Refresh Type	PD7
	71
Standard	NC
Self-refresh	V_{SS}

ECC-on-SIMM Memory Modules

The ECC-on-SIMM family of memory modules are DRAM SIMMs organized as 1M x 36, 2M x 36, 4M x 36, and 8M x 36. In addition to the JEDEC standard pinout, a special option is available which brings out an error indicator signal for each byte of data on the SIMM. The four error lines are brought to the SIMM tabs on pins 29, 46, 66 and 71 for errors on byte 0, 1, 2, and 3, respectively.

Part Number Applicability

The error indicator option is currently available only on gold-tab, 70ns ECC-on-SIMM modules. The cross reference table for standard modules and error indicator modules is shown below.

Organization	Standard Part Number	Error Indicator Part Number
1M x 36	IBM11E1480B-70	IBM11E1490B-70
2M x 36	IBM11E2480B-70	IBM11E2490B-70
4M x 36	IBM11E4480B-70	IBM11E4490B-70
8M x 36	IBM11E8480B-70	IBM11E8490B-70

Error Indicator Line Timings

The error indicator signals are minus-active. They are driven by 4mA tristate drivers; they can not be dotted. The error lines are valid for the same duration as data on a read. That is, 20ns (Tcac) after CAS is valid during a read cycle, the error lines will be valid. They will remain valid until CAS returns high. The drivers will come out of tristate about 5ns after CAS falls and return to tristate about 5ns after CAS rises, although these timings are not guaranteed. The lines will activate whenever a single-bit error is being corrected or a double bit error is detected. In case of the latter, bad parity will be sent to the system to indicate an uncorrectable error. An active error line could indicate an error in either of the two data-bit DRAMs or the check-bit DRAM associated with that byte.

Error line functioning during write operations

The ECC-on-SIMM module will detect bad parity on write operations. That is, if the system sends any byte of data with parity different than that of the first byte of data written after power-on, the SIMM will flag that data as being invalid and return a parity error when data is subsequently read. During write operations, the error line comes out of tristate with the same timings as in a read operation, ie approximately 5ns after CAS transitions, however it is valid from a point 15ns after valid CAS and remains valid until CAS rises. An error during a write operation indicates that a parity error is being detected and that a subsequent read of that data will also reflect that parity error. The use of the error line during write operations has not been characterized.

Introduction

Although small, there is some likelihood that DRAM-based memory in a computer can fail. These fails are of two basic categories:

1. Hard fails, in which the nature of the fail repeats, and is basically permanent. Fixing these fails permanently may require replacement of some part of the memory hardware. Hard error rates are known as HERs.
2. Soft fails, Non-permanent fails that may never reoccur, or occur at infrequent intervals. [Soft fails are effectively "fixed" by powering the system off and back on.] Soft error rates are known as SERs.

SERs are higher than HERs. These errors stem from two sources: alpha particles and cosmic rays. Alpha particle SERs have been virtually eliminated in modern DRAM technology. No DRAM is entirely insensitive to cosmic rays, but IBM DRAMs have very low cosmic ray sensitivity because the IBM 'inside-store' trench cell stores more charge. In addition, the 'inside-store' trench stores the charge in a dielectric capacitor, minimizing the charge collection area.

All system designers should have a basic goal of providing as reliable system as possible. Over time, methods have been developed (and discussed and debated endlessly!) to minimize the impact of system memory fails via improving system fault-tolerance. This note presents a comparison from an advantage/disadvantage aspect, of the four basic levels of fault tolerance:

- Non-parity
- Parity
- ECC, or error-correction coding
- EOS, or ECC-on-SIMM

Non-parity

Basically, non-parity systems have no fault-tolerance at all. The reason they are even used is because they have the lowest inherent cost. No additional memory is necessary as is the case with parity or ECC techniques. Since a parity-type data byte has 9 bits versus 8 for non-parity, memory cost is 12.5% higher. Also the non-parity memory controller is simplified since it does not need the logic gates to calculate parity or ECC check bits. Portable systems which place a premium on minimizing power might benefit from the reduction in memory power due to less DRAM chips. Finally, the memory system data bus is narrower which reduces the amount of data buffers. In modern memories, HERs and SERs are now smaller than previously, as a result the likelihood of memory errors occurring in a given system for its entire operating life has dropped to an extremely small level. Estimates place the value of memory fails in a modern office desk top computer at less than one in ten years. This error rate maybe tolerable because:

- The error may result in a system hang, or doing something so anomalous as to be obvious to the user, in which case he turns off the system and reboots. This is the case with a soft error, for example.
- In the case of hard errors rendering a system inoperative, running the system diagnostics may lead to the problem source.
- Low-end systems such as games, due to their extreme market cost sensitivity probably can't justify the extra cost of parity memory.

At any rate, employing no fault-tolerance in a system is simply gambling that memory errors are unlikely, and if they do occur, result in an inherent cost less than the additional hardware necessary for error detection. However, the disadvantage is that the errors can lead to a serious problem such as calculating the wrong value to go into a bank check, or in the case of a system being used as a server, a memory error forcing a system hang and bringing down all LAN-resident client systems with subsequent loss of productivity. Finally, with a non-parity memory system, problem traceability is difficult which is not the case with parity or ECC. These techniques at least isolate to a memory source as the culprit, thus reducing both the time and cost of problem resolutions.

Parity

Parity, as mentioned previously, results in increasing initial system cost due primarily to the additional memory bits involved. Parity cannot correct system errors, but, since parity can detect errors it can make the user aware of memory errors when they occur.

This has three basic benefits:

1. Guards against the consequences of faulty calculations based on incorrect data.
2. Pinpoints source of errors which assists in problem resolution, thus improving system serviceability.
3. Potential users may perceive system as higher-quality than non-parity systems, resulting in marketplace benefits.

Finally, DRAM module-based systems can easily be designed to function both in a parity or non-parity environment which enables the system manufacturer to offer their system purchasers the choice of parity if they feel the additional cost is justified for their particular application.

ECC

Since studies have indicated that approximately 98% of memory errors are of a single-bit variety, the most commonly used type of ECC is one in which the attendant memory controller detects and corrects single-bit errors and detects, but can't correct double-bit errors, in an accessed data word. This type of ECC is know as SEC-DED and requires an additional 7 check bits over 32 bits in a four-byte system and 8 check bits in an eight-byte system. ECC in a four-byte system obviously costs more than non-parity or parity but in an eight-byte system ECC and parity costs are equal.

ECC entails the memory controller calculating the check bits on a memory-write operation, and performing a compare between the read and calculated check-bits on a read operation, and then, if necessary, correcting bad bit(s). The additional ECC logic in the memory controller is not very significant in this age of inexpensive, high performance, VLSI logic but ECC actually affects memory performance on writes, since the operation must be timed to wait for the calculation of check bits, and reads if the system waits for corrected data. On a partial-word write, the entire word must first be read, then the affected byte(s) rewritten and new check bits calculated. This turns partial-word write operations into slower read-modify-writes.

Most memory errors are of a single-bit nature, correctable by ECC. Incorporating this fault tolerant technique provides high system reliability and attendant availability. An ECC-based system is a good choice for servers, work-stations or mission-critical applications in which the cost of a potential memory error outweighs the additional memory and system cost to correct it and ensure it does not detract from system reliability.

By designing a system that allows the user to make the choice of ECC or parity, or non-parity for that matter, ultimate flexibility is provided. Several of IBM's personal computer systems provide user selectability of memory fault-tolerance techniques.

EOS

These DRAM module types provide an upgrade path to ECC via replacing the previously installed modules with EOS-type SIMMS, thus entailing no processor or planar changes. The EOS SIMMs carry out ECC not on word, but on single-byte boundaries. Through the use of high-speed DRAMs and fast on-board logic, performance degradation is effectively masked. The cost of ECC implementation using EOS is higher than a combination of ECC DRAM modules and a ECC compatible memory controller. This is due primarily to the extra memory necessary to perform ECC on a per-byte basis (ECC on a byte requires 4 check bits, thus on a 32-bit word a total of 16 check-bits are necessary) and the repetition of the ECC logic on each installed SIMM. However, EOS simms are an excellent method to obtain the reliability-enhancing advantages of ECC without performance impacts. They also provide the system OEM with a method to provide the system purchaser a choice between ECC and parity-based memory.

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