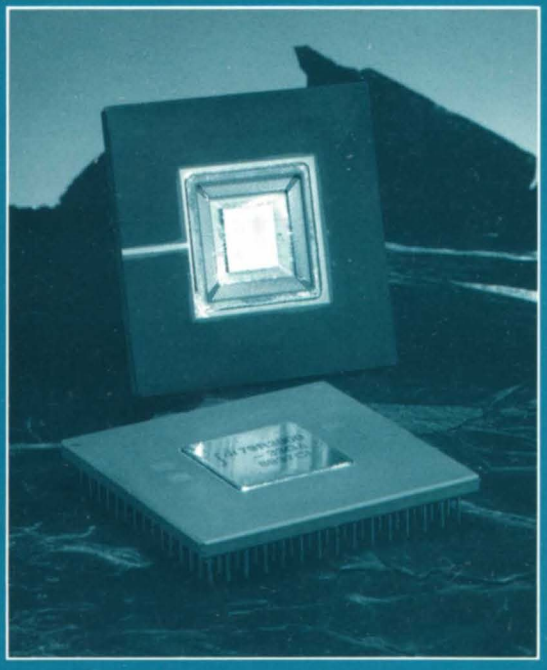
1991
IDT RISC
R3000A, R3001, R3051™ Family
Product Information



Integrated Device Technology, Inc.

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IDT RISC
R3000A, R3001, R3051™ Family
Product Information

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LIFE SUPPORT POLICY

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1. **Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
2. **A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.**

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RISC CPU PROCESSOR

IDT79R3000

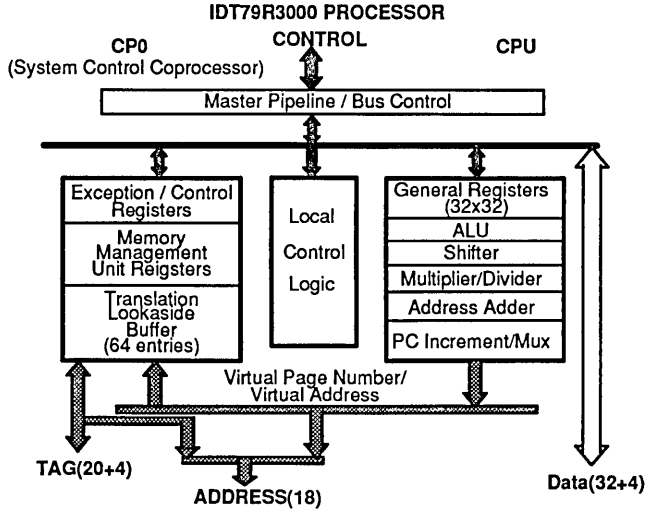
FEATURES:

- Enhanced instruction set compatible version of the IDT79R2000 RISC CPU.
- Full 32-bit Operation—Thirty-two 32-bit registers and all instructions and addresses are 32-bit.
- Efficient Pipelining—The CPU's 5-stage pipeline design assists in obtaining an execution rate approaching one instruction per cycle. Pipeline stalls and exceptions are handled precisely and efficiently.
- On-Chip Cache Control—The IDT79R3000 provides a high bandwidth memory interface that handles separate external Instruction and Data Caches ranging in size from 4 to 256 Kbytes each. Both the caches are accessed during a single CPU cycle. All cache control is on-chip.
- On-Chip Memory Management Unit—A fully-associative, 64 entry Translation Lookaside Buffer (TLB) provides fast address translation for virtual-to-physical memory mapping of the 4 Gigabyte virtual address space.
- Coprocessor Interface—The IDT79R3000 generates all addresses and handles memory interface control for up to three additional tightly coupled external processors.
- Optimizing Compilers are available for C, Fortran, Pascal, COBOL, Ada, and PL/1.
- UNIX™ System V.3 and BSD 4.3 operating systems supported.
- High-speed CEMOS™ technology.
- Instruction set compatible with the IDT79R2000 RISC CPU.
- 16.7MHz, 20MHz, 25MHz and 33MHz clock rates yield up to 28 MIPS sustained throughput.
- Supports independent multiword block refill of both the instruction and data caches with variable block sizes.
- Supports concurrent refill and execution of instructions.
- Partial word stores executed as read-modify-write operations.
- 6 external interrupt inputs (up to 64 different sources), 2 software interrupts, with single cycle latency to exception handler routine.
- Flexible multiprocessing support on chip with no impact on uniprocessor designs.
- Military product compliant to MIL-STD-883, Class B.

DESCRIPTION:

The IDT 79R3000 RISC Microprocessor consists of two tightly-coupled processors integrated on a single chip. The first processor is a full 32-bit CPU based on RISC (Reduced Instruction Set Computer) principles to achieve a new standard of microprocessor performance. The second processor is a system control coprocessor, called CP0, containing a fully-associative 64 entry TLB (Translation Lookaside Buffer), MMU (Memory Management Unit) and control registers, supporting a 4 Gigabyte virtual memory subsystem, and a Harvard Architecture Cache Controller achieving a bandwidth of over 260 Mbytes/second using industry standard static RAMs.

This data sheet provides an overview of the features and architecture of the 79R3000 CPU, Revision 2.0. A more detailed description of the operation of the device is incorporated in the "R3000 Family Hardware User Manual", and a more detailed architectural overview is provided in the "mips RISC Architecture" book, both available from IDT. Documentation providing details of the software and development environments supporting this processor are also available from IDT.



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IDT79R3000 CPU Registers

The IDT 79R3000 CPU provides 32 general purpose 32-bit registers, a 32-bit Program Counter, and two 32-bit registers that hold the results of integer multiply and divide operations. Only two of the 32 general registers have a special purpose: register r0 is hard-wired to the value "0", which is a useful constant, and register r31 is used as the link register in jump-and-link instructions (return address for subroutine calls).

The CPU registers are shown in Figure 2. Note that there is no Program Status Word (PSW) register shown in this figure: the functions traditionally provided by a PSW register are instead provided in the *Status* and *Cause* registers incorporated within the System Control Coprocessor (CP0).

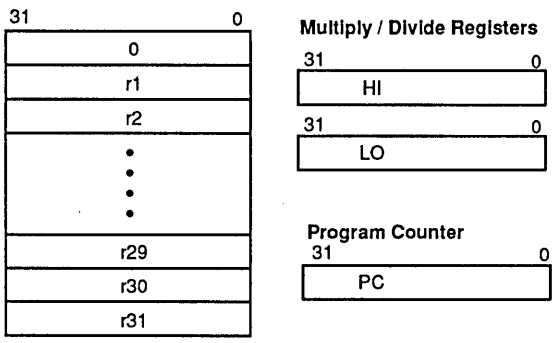


Figure 2. IDT79R3000 CPU Registers

Instruction Set Overview

All IDT 79R3000 instructions are 32 bits long, and there are only three instruction formats. This approach simplifies instruction decoding thus minimizing instruction execution time. The 79R3000 processor initiates a new instruction on every run cycle, and is able to complete an instruction on almost every clock cycle. The only exceptions are the Load instructions and Branch instructions, which each have a single cycle of latency associated with their execution. Note, however, that in the majority of cases the compilers are able to fill these latency cycles with useful instructions which do not require the result of the previous instruction. This effectively eliminates these latency effects.

The actual instruction set of the CPU was determined after extensive simulations to determine which instructions should be implemented in hardware, and which operations are best synthesized in software from other basic instructions. This methodology resulted in the R3000 having the highest performance of any available microprocessor.

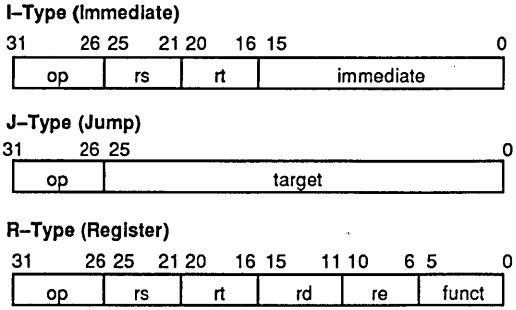


Figure 3. IDT79R3000 Instruction Formats

The IDT79R3000 instruction set can be divided into the following groups:

- **Load/Store** instructions move data between memory and general registers. They are all I-type instructions, since the only addressing mode supported is base register plus 16-bit, signed immediate offset.

  The Load instruction has a single cycle of latency, which means that the data being loaded is not available to the instruction immediately after the load instruction. The compiler will fill this delay slot with either an instruction which is not dependent on the loaded data, or with a NOP instruction. There is no latency associated with the store instruction.

  Loads and Stores can be performed on byte, half-word, word, or unaligned word data (32 bit data not aligned on a modulo-4 address). The CPU cache is constructed as a write-through cache.

- **Computational** instructions perform arithmetic, logical and shift operations on values in registers. They occur in both R-type (both operands and the result are registers) and I-type (one operand is a 16-bit immediate) formats.

  Note that computational instructions are three operand instructions; that is, the result of the operation can be stored into a different register than either of the two operands. This means that operands need not be overwritten by arithmetic operations. This results in a more efficient use of the large register set.

- **Jump and Branch** instructions change the control flow of a program. Jumps are always to a paged absolute address formed by combining a 26-bit target with four bits of the Program counter (J-type format, for subroutine calls), or 32-bit register byte addresses (R-type, for returns and dispatches). Branches have 16-bit offsets relative to the program counter (I-type). Jump and Link instructions save a return address in Register 31. The 79R3000 instruction set features a number of branch conditions. Included is the ability to compare a register to zero and branch, and also the ability to branch based on a comparison between two registers. Thus, net performance is increased since software does not have to perform arithmetic instructions prior to the branch to set up the branch conditions.

- **Coprocessor** instructions perform operations in the coprocessors. Coprocessor Loads and Stores are I-type. Coprocessor computational instructions have coprocessor-dependent formats (see coprocessor manuals).

- **Coprocessor 0** instructions perform operations on the System Control Coprocessor (CP0) registers to manipulate the memory management and exception handling facilities of the processor.

- **Special** instructions perform a variety of tasks, including movement of data between special and general registers, system calls, and breakpoint. They are always R-type.

Table 1 lists the instruction set of the IDT79R3000 processor.

OP	DESCRIPTION
	Load/Store Instructions
LB	Load Byte
LBU	Load Byte Unsigned
LH	Load Halfword
LHU	Load Halfword Unsigned
LW	Load Word
LWL	Load Word Left
LWR	Load Word Right
SB	Store Byte
SH	Store Halfword
SW	Store Word
SWL	Store Word Left
SWR	Store Word Right
	Arithmetic Instructions (ALU Immediate)
ADDI	Add Immediate
ADDIU	Add Immediate Unsigned
SLTI	Set on Less Than Immediate
SLTIU	Set on Less Than Immediate Unsigned
ANDI	AND Immediate
ORI	OR Immediate
XORI	Exclusive OR Immediate
LUI	Load Upper Immediate
	Arithmetic Instructions (3–operand, register–type)
ADD	Add
ADDU	Add Unsigned
SUB	Subtract
SUBU	Subtract Unsigned
SLT	Set on Less Than
SLTU	Set on Less Than Unsigned
AND	AND
OR	OR
XOR	Exclusive OR
NOR	NOR
	Shift Instructions
SLL	Shift Left Logical
SRL	Shift Right Logical
SRA	Shift Right Arithmetic
SLLV	Shift Left Logical Variable
SRLV	Shift Right Logical Variable
SRAV	Shift Right Arithmetic Variable

OP	DESCRIPTION
	Multiply/Divide Instructions
MULT	Multiply
MULTU	Multiply Unsigned
DIV	Divide
DIVU	Divide Unsigned
MFHI	Move From HI
MTHI	Move To HI
MFLO	Move From LO
MTLO	Move To LO
	Jump and Branch Instructions
J	Jump
JAL	Jump and Link
JR	Jump to Register
JALR	Jump and Link Register
BEQ	Branch on Equal
BNE	Branch on Not Equal
BLEZ	Branch on Less than or Equal to Zero
BGTZ	Branch on Greater Than Zero
BLTZ	Branch on Less Than Zero
BGEZ	Branch on Greater than or Equal to Zero
BLTZAL	Branch on Less Than Zero and Link
BGEZAL	Branch on Greater than or Equal to Zero and Link
	Special Instructions
SYSCALL	System Call
BREAK	Break
	Coprocessor Instructions
LWCz	Load Word from Coprocessor
SWCz	Store Word to Coprocessor
MTCz	Move To Coprocessor
MFCz	Move From Coprocessor
CTCz	Move Control to Coprocessor
CFCz	Move Control From Coprocessor
COPz	Coprocessor Operation
BCzT	Branch on Coprocessor z True
BCzF	Branch on Coprocessor z False
	System Control Coprocessor (CP0) Instructions
MTC0	Move To CP0
MFC0	Move From CP0
TLBR	Read indexed TLB entry
TLBWI	Write Indexed TLB entry
TLBWR	Write Random TLB entry
TLBP	Probe TLB for matching entry
RFE	Restore From Exception

Table 1. IDT79R3000 Instruction Summary

IDT79R3000 System Control Coprocessor (CP0)

The IDT79R3000 can operate with up to four tightly-coupled coprocessors (designated CP0 through CP3). The System Control Coprocessor (or CP0), is incorporated on the IDT79R3000 chip and supports the virtual memory system and exception handling functions of the IDT79R3000. The virtual memory system is implemented using a Translation Lookaside Buffer and a group of programmable registers as shown in Figure 4.

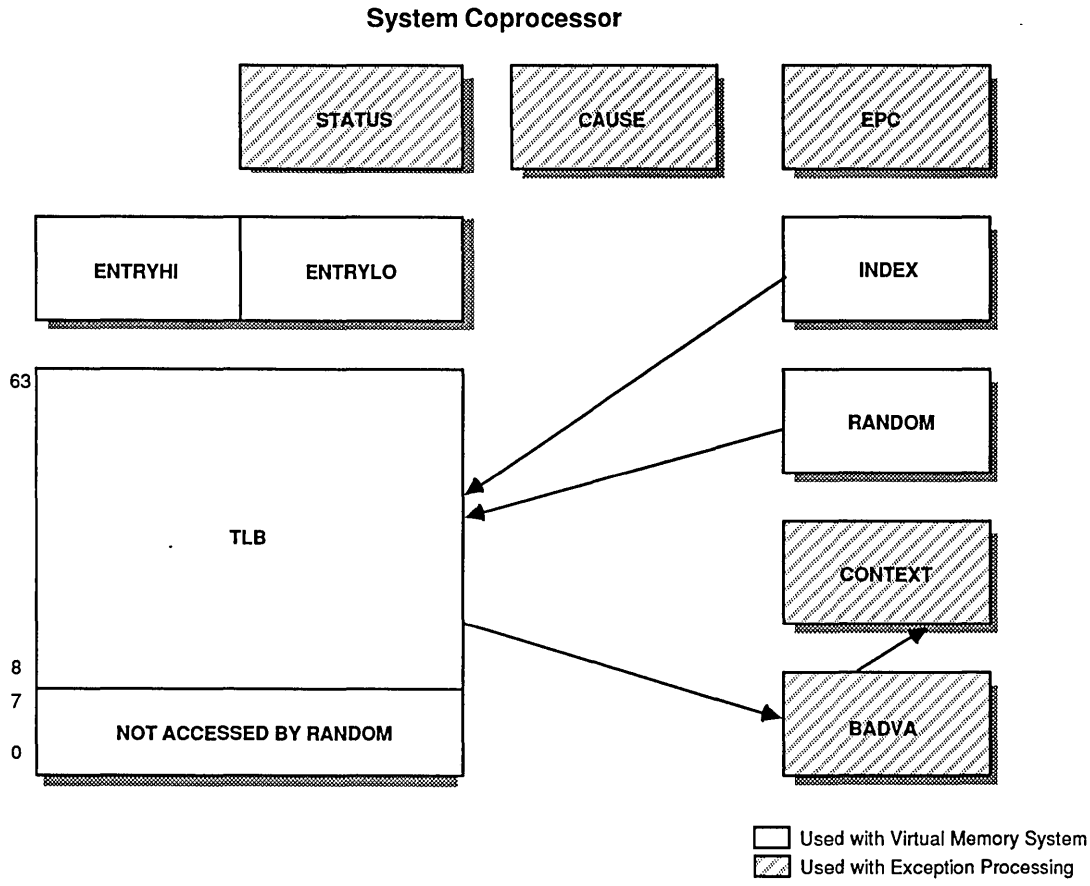


Figure 4. The System Coprocessor Registers

System Control Coprocessor (CP0) Registers

The CP0 registers shown in Figure 4 are used to control the memory management and exception handling capabilities of the IDT79R3000. Table 2 provides a brief description of each register.

REGISTER	DESCRIPTION
EntryHi	High half of a TLB entry
EntryLo	Low half of a TLB entry
Index	Programmable pointer into TLB array
Random	Pseudo–random pointer into TLB array
Status	Mode, interrupt enables, and diagnostic status info
Cause	Indicates nature of last exception
EPC	Exception Program Counter
Context	Pointer into kernel's virtual Page Table Entry array
BadVA	Most recent bad virtual address
PRId	Processor revision identification (Read only)

Table 2. System Control Coprocessor (CP0) Registers

Memory Management System

The IDT79R3000 has an addressing range of 4 Gbytes. However, since most IDT79R3000 systems implement a physical memory smaller than 4 Gbytes, the IDT79R3000 provides for the logical expansion of memory space by translating addresses composed in a large virtual address space into available physical memory address. The 4 GByte address space is divided into 2 GBytes which can be accessed by both the users and the kernel, and 2 GBytes for the kernel only.

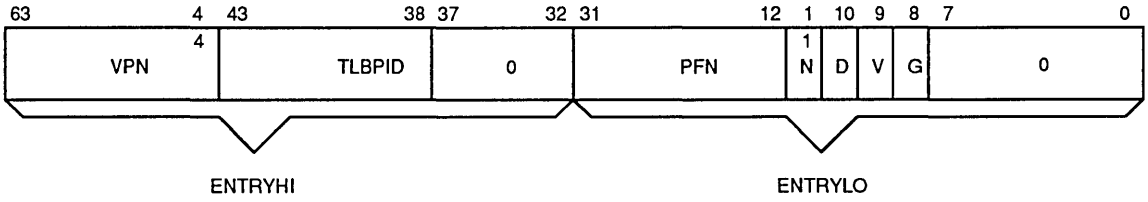
The TLB (Translation Lookaside Buffer)

Virtual memory mapping is assisted by the Translation Lookaside Buffer (TLB). The on-chip TLB provides very fast virtual memory access and is well-matched to the requirements of multi-tasking operating systems. The fully-associative TLB contains 64 entries, each of which maps a 4-Kbyte page, with controls for read/write access, cacheability, and process identification. The TLB allows each user to access up to 2 Gbytes of virtual address space.

Figure 5 illustrates the format of each TLB entry. The Translation operation involves matching the current Process ID (PID) and upper 20 bits of the address against PID and VPN (Virtual Page Number) fields in the TLB. When both match (or the TLB entry is Global), the VPN is replaced with the PFN (Physical Frame Number) to form the physical address.

TLB misses are handled in software, with the entry to be replaced determined by a simple RANDOM function. The routine to process a TLB miss in the UNIX environment requires only 10–12 cycles, which compares favorably with many CPUs which perform the operation in hardware.

TLB ENTRY FORMAT



VPN – Virtual Page number
TLBPID – Process ID
PFN – Physical frame number
N – Non-cacheable flag
D – Dirty flag (Write protect)
V – Valid entry flag
G – Global flag (ignore PID)
O – Reserved

Figure 5. TLB Entry Format

IDT79R3000 Operating Modes

The IDT79R3000 has two operating modes: *User* mode and *Kernel* mode. The IDT79R3000 normally operates in the User mode until an exception is detected forcing it into the Kernel mode. It remains in the Kernel mode until a Restore From Exception *(RFE)* instruction is executed. The manner in which memory addresses are translated or *mapped* depends on the operating mode of the IDT79R3000. Figure 6 shows the MMU translation performed for each of the operating modes.

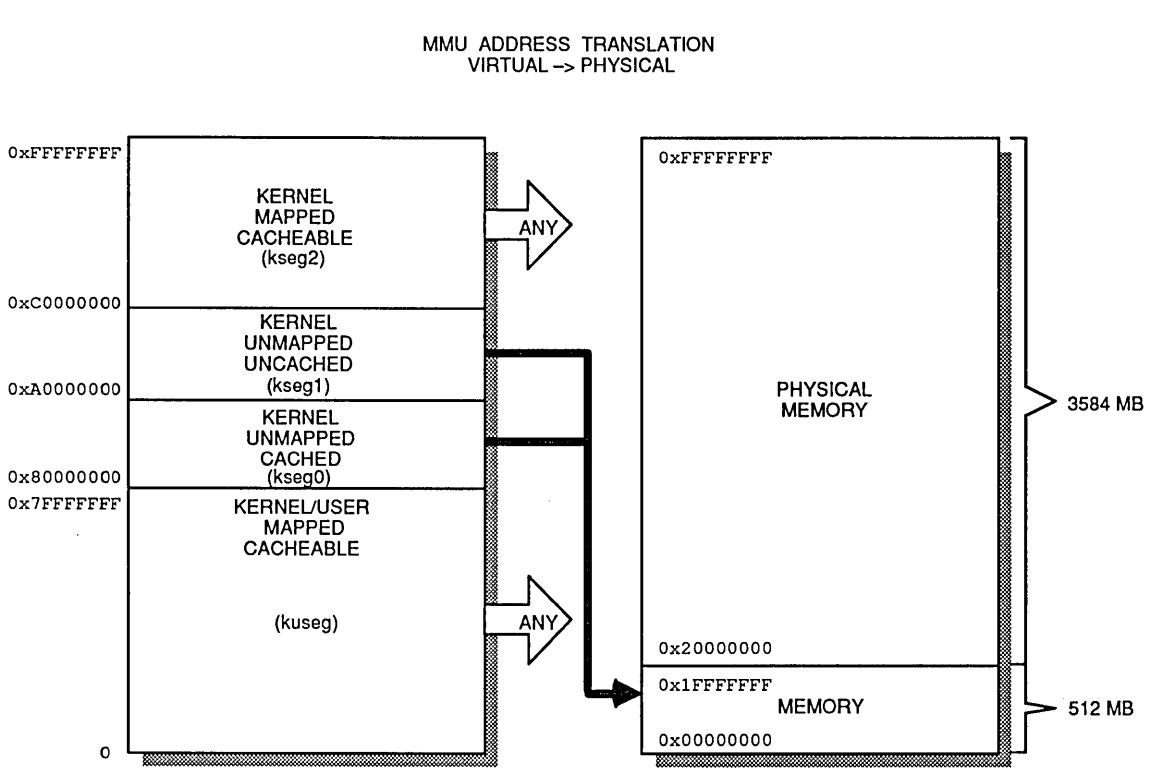


Figure 6. IDT79R3000 Virtual Address Mapping

User Mode—in this mode, a single, uniform virtual address space (kuseg) of 2 Gbyte is available. Each virtual address is extended with a 6-bit process identifier field to form unique virtual addresses. All references to this segment are mapped through the TLB. Use of the cache for up to 64 processes is determined by bit settings for each page within the TLB entries.

Kernel Mode—four separate segments are defined in this mode:

- *kuseg*—when in the kernel mode, references to this segment are treated just like user mode references, thus streamlining kernel access to user data.
- *kseg0*—references to this 512 Mbyte segment use cache memory but are not mapped through the TLB. Instead, they always map to the first 0.5 GBytes of physical address space.
- *kseg1*—references to this 512 Mbyte segment are not mapped through the TLB and do not use the cache. Instead, they are hard-mapped into the same 0.5 GByte segment of physical address space as *kseg0*.
- *kseg2*—references to this 1 Gbyte segment are always mapped through the TLB and use of the cache is determined by bit settings within the TLB entries.

IDT79R3000 Pipeline Architecture

The execution of a single IDT79R3000 instruction consists of five primary steps:

1) **IF** —Fetch the instruction (I-Cache).
2) **RD** —Read any required operands from CPU registers while decoding the instruction.
3) **ALU** —Perform the required operation on instruction operands.
4) **MEM**—Access memory (D-Cache).
5) **WB** —Write back results to register file.

Each of these steps requires approximately one CPU cycle as shown in Figure 7 (parts of some operations overlap into another cycle while other operations require only 1/2 cycle).

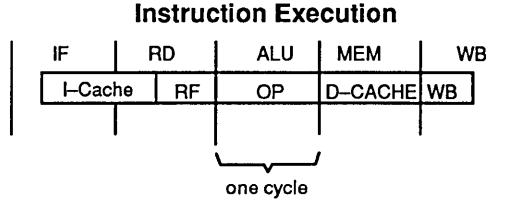


Figure 7. IDT79R3000 Instruction Pipeline

The IDT79R3000 uses a 5-stage pipeline to achieve an instruction execution rate approaching one instruction per CPU cycle. Thus, execution of five instructions at a time are overlapped as shown in Figure 8.

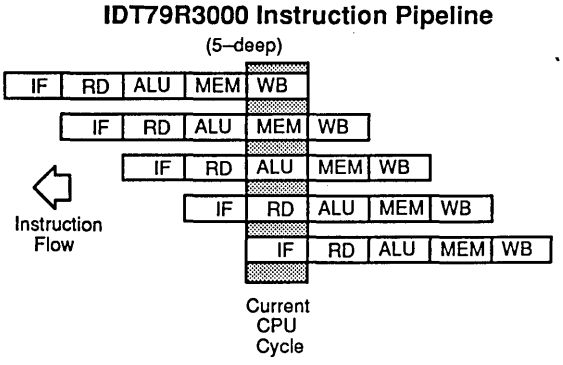


Figure 8. IDT79R3000 Execution Sequence

This pipeline operates efficiently because different CPU resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

Memory System Hierarchy

The high performance capabilities of the IDT79R3000 processor demand system configurations incorporating techniques frequently employed in large, mainframe computers but seldom encountered in systems based on more traditional microprocessors.

A primary goal of systems employing RISC techniques is to minimize the average number of cycles each instruction requires for execution. In order to achieve this goal, RISC processors incorporate a number of RISC techniques including a compact and uniform instruction set, a deep instruction pipeline (as described above), and utilization of optimizing compilers. Many of the advantages obtained from these techniques can, however, be negated by an inefficient memory system.

Figure 9 illustrates memory in a simple microprocessor system. In this system, the CPU outputs addresses to memory and reads instructions and data from memory or writes data to memory. The address space is completely undifferentiated: instructions, data, and I/O devices are all treated the same. In such a system, a primary limiting performance factor is memory bandwidth.

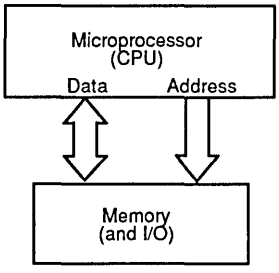


Figure 9. A Simple Microprocessor Memory System

Figure 10 illustrates a memory system that supports the significantly greater memory bandwidth required to take full advantage of the IDT79R3000's performance capabilities. The key features of this system are:

- **External Cache Memory**—Local, high-speed memory (called *cache* memory) is used to hold instructions and data that is repetitively accessed by the CPU (for example, within a program loop) and thus reduces the number of references that must be made to the slower-speed main memory. Some microprocessors provide a limited amount of cache memory on the CPU chip itself. The external caches supported by the IDT79R3000 can be much larger; while a small cache can improve performance of some programs, significant improvements for a wide range of programs require large caches.
- **Separate Caches for data and Instructions**—Even with high-speed caches, memory speed can still be a limiting factor because of the fast cycle time of a high-performance microprocessor. The IDT79R3000 supports separate caches for instructions and data and alternates accesses of the two caches during each CPU cycle. Thus, the processor can obtain data and instructions at the cycle rate of the CPU using caches constructed with commercially available IDT static RAM devices.

  In order to maximize bandwidth in the cache while minimizing the requirement for SRAM access speed, the R3000 divides a single-processor clock cycle into two phases. During one phase, the address for the data cache access is presented while data previously addressed in the instruction cache is read; during the next phase, the data operation is completed while the instruction cache is being addressed. Thus, both caches are read in a single processor cycle using only one set of address and data pins.
- **Write Buffer**—In order to ensure data consistency, all data that is written to the data cache must also be written out to main memory. The cache write model used by the IDT79R3000 is that of a write-through cache; that is, all data written by the CPU is immediately written into the main memory. To relieve the CPU of this responsibility (and the inherent performance burden) the IDT79R3000 supports an interface to a write buffer. The IDT79R3020 Write Buffer captures data (and associated addresses) output by the CPU and ensures that the data is passed on to main memory.

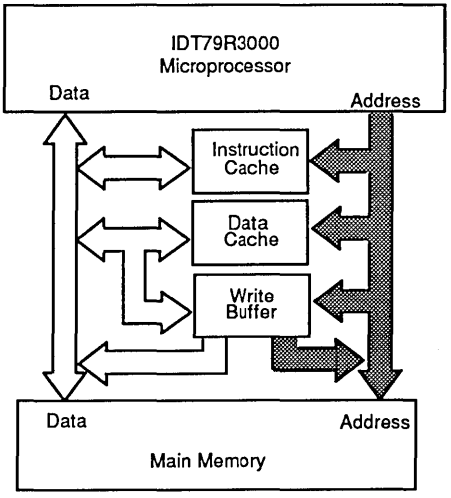


Figure 10. An IDT79R3000 System with a High-Performance Memory System

IDT79R3000 Processor Subsystem Interfaces

Figure 11 illustrates the three subsystem interfaces provided by the IDT79R3000 processor:

- **Cache control** interface (on-chip) for separate data and instruction caches permits implementation of off-chip caches using standard IDT SRAM devices. The 79R3000 directly controls the cache memory with a minimum of external components. Both the instruction and data cache can vary from 0 to 256K Bytes (64 K entries). The 79R3000 also includes the TAG control logic which determines whether or not the entry read from the cache is the desired data.

  The 79R3000 cache controller implements a direct mapped cache for high net performance (bandwidth). It has the ability to refill multiple words when a cache miss occurs, thus reducing the effective miss rate to less than 2% for large caches. When a cache miss occurs, the 79R3000 can support refilling the cache in 1, 4, 8, 16, or 32 word blocks to minimize the effective penalty of having to access main memory. The 79R3000 also incorporates the ability to perform instruction streaming; while the cache is refilling, the processor can resume execution once the missed word is obtained from main memory. In this way, the processor can continue to execute concurrently with the cache block refill.
- **Memory controller** interface for system (main) memory. This interface also includes the logic and signals to allow operation with a write buffer to further improve memory bandwidth. In addition to the standard full word access, the memory controller supports the ability to write bytes and half-words by using partial word operations. The memory controller also supports the ability to retry memory accesses if, for example, the data returned from memory is invalid and a bus error needs to be signalled.
- **Coprocessor Interface**—The IDT79R3000 features a tightly coupled co-processor interface in which all co-processors maintain synchronization with the main processor; reside on the same data bus as the main processor; and participate in bus transactions in an identical manner to the main processor. The IDT79R3000 generates all required cache and memory control signals, including cache and memory addresses for attached coprocessors. As a result, only the data bus and a few control signals need to be connected to a coprocessor.

  The interface supports three types of coprocessor instructions: loads/stores, coprocessor operations, and processor-coprocessor transfers. Note that coprocessor loads and stores occur directly between the coprocessor and memory, without requiring the data to go through the CPU.

  Synchronization between the CPU and external coprocessors is achieved using a Phased-Lock Loop interface to the coprocessor. The coprocessor physical interface also includes coprocessor condition signals (CpCond(n)), which are used in coprocessor branch instructions, and a coprocessor busy signal (CpBusy) which is used to stall the CPU if the coprocessor needs to hold off subsequent operations.

  Finally, a precise exception interface is defined between the CPU and coprocessors using the external interrupt inputs of the CPU. This allows a coprocessor exception, even if it was the result of a multi-cycle operation, to be traced to the precise coprocessor operation which caused it. This is an important feature for languages which can define specific error handlers for each task.

  The interface supports up to four separate coprocessors. Coprocessor 0 is defined to be the system control coprocessor, and resides on the same chip as the CPU unit. Coprocessor 1 is the Floating Point Accelerator, IDT 79R3010. Coprocessors 2 and 3 are available to support an interface to application specific functions.

MULTIPROCESSING SUPPORT

The IDT79R3000 supports multiprocessing applications in a simple but effective way. Multiprocessing applications require cache coherency across the multiple processors. The IDT79R3000 offers two signals to support cache coherency: the first, MPStall, stalls the processor within two cycles of being received and keeps it from accessing the cache. This allows an external agent to snoop into the processor data cache. The second signal, MPInvalidate, causes the processor to write data on the data cache bus which indicates the externally addressed cache entry is invalid. Thus, a subsequent access to that location would result in a cache miss, and the data would be obtained from main memory.

The two MP signals would be generated by a external logic which utilizes a secondary cache to perform bus snooping functions. The 79R3000 does not impose an architecture for this secondary cache, but rather is flexible enough to support a variety of application specific architectures and still maintain cache coherency. Further, there is no impact on designs which do not require this feature.

ADVANCED FEATURES

The IDT79R3000 offers a number of additional features such as the ability to swap the instruction and data caches, facilitating diagnostics and cache flushing. Another feature isolates the caches, which forces cache hits to occur regardless of the contents of the tag fields.

Further features of the IDT79R3000 are configured during the last four cycles prior to the negation of the RESET input. These functions include the ability to select cache sizes and cache refill block sizes; the ability to utilize the multiprocessor interface; whether or not instruction streaming is enabled; whether byte ordering follows "Big-Endian" or "Little-Endian" protocols, etc. Table 3 shows the configuration options selected at Reset. These are further discussed in the "Hardware User's Manual".

BACKWARD COMPATIBILITY WITH 79R2000

The IDT79R3000 can be used in sockets designed for the 79R2000A. The pin-out of the 79R3000 has been selected to ensure this compatibility, with new functions mapped onto previously unused pins. The instruction set is compatible with that of the 79R2000 at the binary level. As a result, code written for the older processor can be executed. New features, such as block refill, instruction streaming, etc. can be selectively disabled.

In most 79R2000A applications, the 79R3000 can be placed in the socket with no modification to initialization settings. The initialization of the 79R3000 includes whether or not the device should operate as a 79R2000A. Systems using 79R2000A would normally have this input configured so that the device would default to this mode. Further application assistance on this topic is available from IDT.

A SPECIAL NOTE ON PACKAGING

Both the flat pack and the PGA packages for the 79R3000 incorporate separate power and ground planes to eliminate noise associated with high frequency operation. This, coupled with the numerous power and ground pins provided on the device, helps to ensure very reliable operation.

INPUT	W CYCLE	X CYCLE	Y CYCLE	Z CYCLE
$\overline{Int0}$	$\overline{DBlkSize0}$	$\overline{DBlkSize1}$	Extend Cache	$\overline{BigEndian}$
$\overline{Int1}$	$\overline{IBlkSize0}$	$\overline{IBlkSize1}$	Reserved(1)	$\overline{TriState}$
$\overline{Int2}$	Reserved(1)	IStream	Reserved(1)	$\overline{NoCache}$
$\overline{Int3}$	Reserved(1)	StorePartial	MultiProcessor	BusDriveOn
$\overline{Int4}$	$\overline{PhaseDelayOn}$(2)	$\overline{PhaseDelayOn}$(2)	$\overline{PhaseDelayOn}$(2)	$\overline{PhaseDelayOn}$(2)
$\overline{Int5}$	$\overline{R3000\ Mode}$(2)	$\overline{R3000\ Mode}$(2)	$\overline{R3000\ Mode}$(2)	$\overline{R3000\ Mode}$(2)

NOTES:
1. Reserved entries must be driven high.
2. These values must be driven stable throughout the entire RESET period.

Table 3: IDT79R3000 Mode Selectable Features

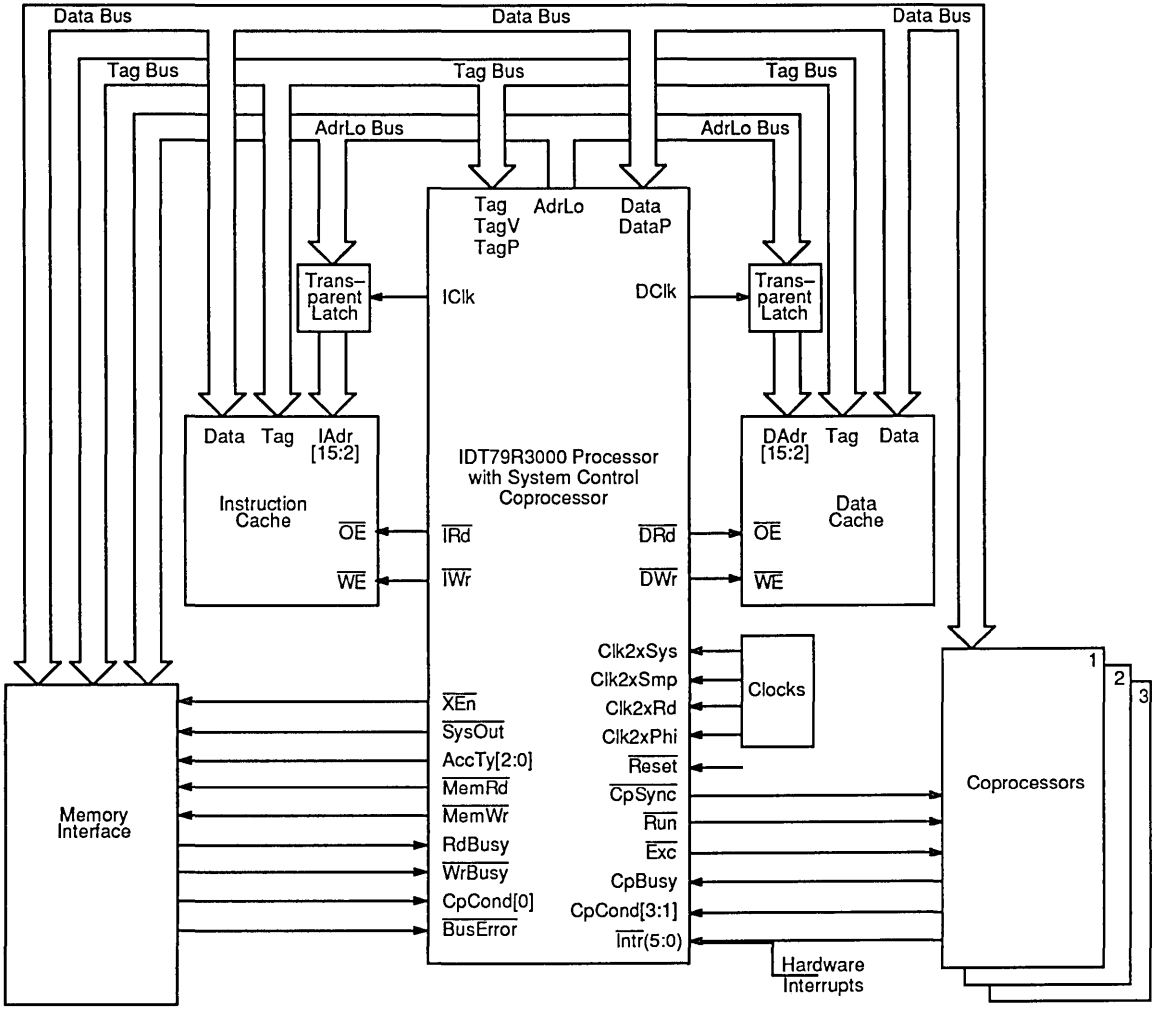
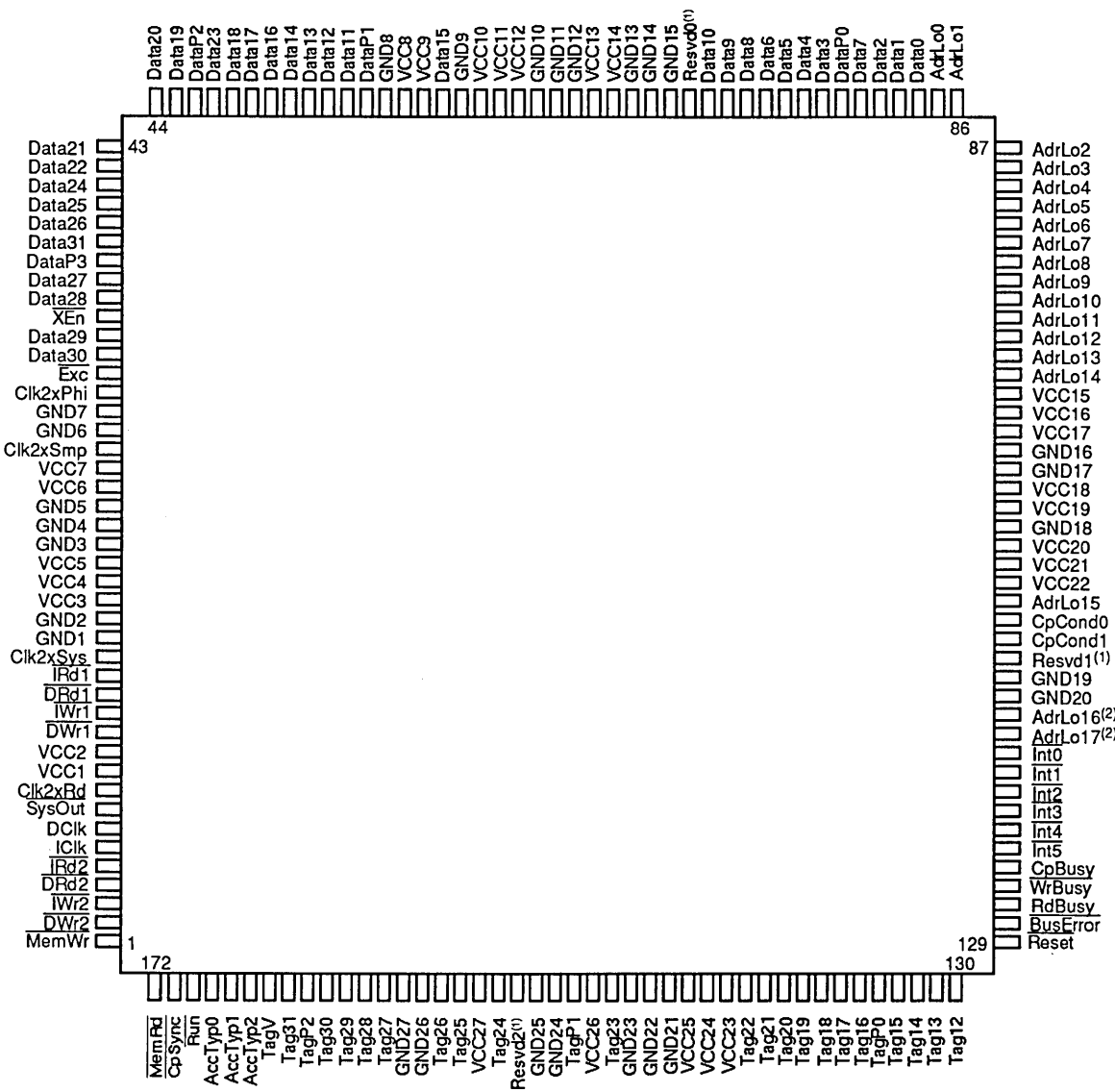


Figure 11. IDT79R3000 Subsystem Interfaces Example; 64 KB Caches

PIN CONFIGURATION



172-PIN CERAMIC FLATPACK
(Cavity Side View)

NOTES:

1. Reserved pins must not be connected.
2. AdrLo 16 & 17 are multi-function pins which are controlled by mode select programming on interrupt pins at reset time.
   AdrLo 16: MP Invalidate, CpCond (2).
   AdrLo 17: MP Stall, CpCond (3).

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VCC14	AdrLo 6	AdrLo 10	AdrLo 11	VCC12	AdrLo 14	AdrLo 15	CpCond 0	AdrLo[1] 16	AdrLo[1] 17	$\overline{\text{Intr2}}$	$\overline{\text{Intr5}}$	$\overline{\text{Wr}}$ $\overline{\text{Busy}}$	$\overline{\text{Reset}}$	VCC10
B	AdrLo 3	$\overline{\text{DRd2}}$	AdrLo 7	AdrLo 9	AdrLo 12	$\overline{\text{IRd2}}$	AdrLo 13	CpCond 1	$\overline{\text{Intr1}}$	$\overline{\text{Intr3}}$	Cp Busy	$\overline{\text{Bus}}$ $\overline{\text{Error}}$	$\overline{\text{DR2}}$	Tag12	Tag15
C	AdrLo 0	AdrLo 4	VCC13	AdrLo 5	AdrLo 8	GND13	GND12	VCC11	$\overline{\text{Intr0}}$	$\overline{\text{Intr4}}$	Rd Busy	GND11	Tag13	TagP0	Tag18
D	Data 1	AdrLo 2	GND0										Tag14	Tag17	Tag19
E	DataP 0	Data 0	AdrLo 1										Tag16	Tag20	VCC9
F	VCC0	Data 7	Data 2										GND10	Tag21	Tag23
G	Data 4	Data 3	GND1										GND9	Tag22	TagP1
H	Data 6	Data 5	Data 8										VCC8	Tag25	Tag24
J	Data 10	DataP 1	Data 9										Tag28	Tag29	Tag26
K	Data 15	Data 11	GND2										GND8	Tag P2	Tag27
L	VCC1	Data 12	Data 17										Acc Typ2	Tag31	Tag30
M	Data 13	Data 16	DataP 2										GND7	Acc Typ1	VCC7
N	Data 14	Data 18	Data 19	GND3	Data 24	Data P3	VCC3	VCC4	GND5	GND6	$\overline{\text{DRd1}}$	$\overline{\text{Mem}}$ $\overline{\text{Wr}}$	$\overline{\text{Mem}}$ $\overline{\text{Rd}}$	$\overline{\text{Run}}$	TagV
P	Data 23	Data 20	$\overline{\text{IWr2}}$	Data 22	Data 26	Data 27	$\overline{\text{XEn}}$	Data 30	Clk2x Sys	Clk2x Rd	DClk	$\overline{\text{IRd1}}$	$\overline{\text{IWr1}}$	$\overline{\text{Cp}}$ $\overline{\text{Sync}}$	Acc Typ0
Q	VCC2	Data 21	Data 25	Data 31	Data 28	GND4	Data 29	$\overline{\text{Excep}}$ $\overline{\text{tion}}$	Clk2x Phi	Clk2x Smp	$\overline{\text{SysOut}}$	VCC5	IClk	$\overline{\text{DWr1}}$	VCC6

144-Pin PGA (Top View)

NOTE:

1. AdrLo 16 & 17 are multi-function pins which are controlled by mode select programming on interrupt pins at reset time.
   AdrLo16: MP Invalidate, CpCond (2).
   AdrLo17: MP Stall, CpCond (3).

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
Data (0–31)	I/O	A 32-bit bus used for all instruction and data transmission among the processor, caches, memory interface, and coprocessors.
DataP (0–3)	I/O	A 4-bit bus containing even parity over the data bus.
Tag (12–31)	I/O	A 20-bit bus used for transferring cache tags and high addresses between the processor, caches, and memory interface.
TagV	I/O	The tag validity indicator.
TagP (0–2)	I/O	A 3-bit bus containing even parity over the concatenation of TagV and Tag.
AdrLo (0–17)	O	An 18-bit bus containing byte addresses used for transferring low addresses from the processor to the caches and memory interface. (AdrLo 16: CpCond (2), AdrLo 17: CpCond (3) set by reset initialization).
$\overline{\text{IRd1}}$	O	Read enable for the instruction cache.
$\overline{\text{IWr1}}$	O	Write enable for the instruction cache.
$\overline{\text{IRd2}}$	O	An identical copy of $\overline{\text{IRd1}}$ used to split the load.
$\overline{\text{IWr2}}$	O	An identical copy of $\overline{\text{IWr1}}$ used to split the load.
IClk	O	The instruction cache address latch clock. This clock runs continuously.
$\overline{\text{DRd1}}$	O	The read enable for the data cache.
$\overline{\text{DWr1}}$	O	The write enable for the data cache.
$\overline{\text{DRd2}}$	O	An identical copy of $\overline{\text{DRd1}}$ used to split the load.
$\overline{\text{DWr2}}$	O	An identical copy of $\overline{\text{DWr1}}$ used to split the load.
DClk	O	The data cache address latch clock. This clock runs continuously.
$\overline{\text{XEn}}$	O	The read enable for the Read Buffer.
AccTyp (0–2)	O	A 3-bit bus used to indicate the size of data being transferred on the data bus, whether or not a data transfer is occurring, and the purpose of the transfer.
$\overline{\text{MemWr}}$	O	Signals the occurrence of a main memory write
$\overline{\text{MemRd}}$	O	Signals the occurrence of a main memory read.
$\overline{\text{BusError}}$	I	Signals the occurrence of a bus error during a main memory read or write.
$\overline{\text{Run}}$	O	Indicates whether the processor is in the run or stall state.
$\overline{\text{Exception}}$	O	Indicates that the instruction about to commit state should be aborted and other exception related information.
$\overline{\text{SysOut}}$	O	A reflection of the internal processor clock used to generate the system clock.
$\overline{\text{CpSync}}$	O	A clock which is identical to $\overline{\text{SysOut}}$ and used by coprocessors for timing synchronization with the CPU.
RdBusy	I	The main memory read stall termination signal. In most system designs RdBusy is normally asserted and is deasserted only to indicate the successful completion of a memory read. RdBusy is sampled by the processor only during memory read stalls.
$\overline{\text{WrBusy}}$	I	The main memory write stall initiation/termination signal.
CpBusy	I	The coprocessor busy stall initiation/termination signal.
CpCond (0–1)	I	A 2-bit bus used to transfer conditional branch status from the coprocessors to the main processor.
CpCond (2–3)	I	Conditional branch status from coprocessors to the processor. Function is provided on AdrLo 16/17 pins and is selected at reset time.
MPStall	I	Multiprocessing Stall. Signals to the processor that it should stall accesses to the caches in a multiprocessing environment. This is physically the same pin as CpCond3; its use is determined at RESET initialization.
MPInvalidate	I	Multiprocessing Invalidate. Signals to the processor that it should issue invalidate data on the cache data bus. The address to be invalidated is externally provided. This is the same pin as CpCond2; its use is determined at RESET initialization.
$\overline{\text{Int}}$ (0–5)	I	A 6-bit bus used by the memory interface and coprocessors to signal maskable interrupts to the processor. At reset time, mode select values are read in.
Clk2xSys	I	The master double frequency input clock used for generating $\overline{\text{SysOut}}$.
Clk2xSmp	I	A double frequency clock input used to determine the sample point for data coming into the processor and coprocessors.
Clk2xRd	I	A double frequency clock input used to determine the enable time of the cache RAMs.
Clk2xPhi	I	A double frequency clock input used to determine the position of the internal phases, phase1 and phase2.
$\overline{\text{Reset}}$	I	Synchronous initialization input used to force execution starting from the reset memory address. $\overline{\text{Reset}}$ must be deasserted synchronously but asserted asynchronously. The deassertion of $\overline{\text{reset}}$ must be synchronized by the leading edge of SysOut.

ABSOLUTE MAXIMUM RATINGS[1, 3]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
V_{IN}	Input Voltage[2]	–0.5 to +7.0	–0.5 to +7.0	V

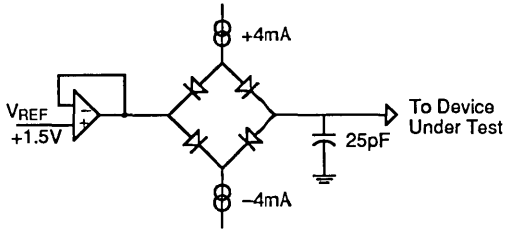
NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –3.0V for pulse width less than 15ns.
   V_{IN} should not exceed V_{CC} +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	–55°C to +125°C	0V	5.0 ± 10%
Commercial	0°C to +70°C	0V	5.0 ± 5%

OUTPUT LOADING FOR AC TESTING



DC ELECTRICAL CHARACTERISTICS— COMMERCIAL TEMPERATURE RANGE T_A = 0°C to +70°C, V_{CC} = +5.0V ± 5%

SYMBOL	PARAMETER	TEST CONDITIONS	16.67MHz MIN.	16.67MHz MAX.	20.0MHz MIN.	20.0MHz MAX.	25.0MHz MIN.	25.0MHz MAX.	33.33MHz MIN.	33.33MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{OHC}	Output HIGH Voltage[7]	V_{CC} = Min., I_{OH} = –4mA	4.0	—	4.0	—	4.0	—	4.0	—	V
V_{OHT}	Output HIGH Voltage [4, 6]	V_{CC} = Min., I_{OH} = –8mA	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OLT}	Output LOW Voltage [4, 6]	V_{CC} = Min., I_{OL} = 8mA	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IH}	Input HIGH Voltage [5]		2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage [1]		—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage [2, 5]		3.0	—	3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage [1, 2]		—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance [6]		—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance [6]		—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = Max.	—	575	—	650	—	750	—	850	mA
I_{IH}	Input HIGH Leakage [3]	V_{IH} = V_{CC}	—	10	—	10	—	10	—	10	µA
I_{IL}	Input LOW Leakage [3]	V_{IL} = GND	–10	—	–10	—	–10	—	–10	—	µA
I_{OZ}	Output Tri–state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–40	40	–40	40	–40	40	–40	40	µA

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{Reset}$.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag busses only. Note that V_{IH} and V_{IL} also apply to these signals. V_{OHT} and V_{OLT} are provided to give the designer further information about these specific signals.
5. V_{IH} should not be held above V_{CC} + 0.5 volts.
6. Guaranteed by design.
7. V_{OHC} applies to $\overline{RUN}$ and $\overline{Exception}$.

DC ELECTRICAL CHARACTERISTICS— MILITARY TEMPERATURE RANGE (T_A = –55°C to +125°C, V_{CC} = +5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67MHz MIN.	16.67MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	V
V_{OHC}	Output HIGH Voltage[7]	V_{CC} = Min., I_{OH} = –4mA	4.0	—	V
V_{OHT}	Output HIGH Voltage [4, 6]	V_{CC} = Min., I_{OH} = –8mA	2.4	—	V
V_{OLT}	Output LOW Voltage [4, 6]	V_{CC} = Min., I_{OL} = 8mA	—	0.8	V
V_{IH}	Input HIGH Voltage [5]		2.0	—	V
V_{IL}	Input LOW Voltage [1]		—	0.8	V
V_{IHS}	Input HIGH Voltage [2, 5]		3.0	—	V
V_{ILS}	Input LOW Voltage [1, 2]		—	0.4	V
C_{IN}	Input Capacitance [6]		—	10	pF
C_{OUT}	Output Capacitance [6]		—	10	pF
I_{CC}	Operating Current	V_{CC} = Max.	—	750	mA
I_{IH}	Input HIGH Leakage [3]	V_{IH} = V_{CC}	—	10	µA
I_{IL}	Input LOW Leakage [3]	V_{IL} = GND	–10	—	µA
I_{OZ}	Output Tri–state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–40	40	µA

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag busses only. Note that V_{IH} and V_{IL} also apply to these signals. V_{OHT} and V_{OLT} are provided to give the designer further information about these specific signals.
5. V_{IH} should not be held above V_{CC} + 0.5 volts.
6. Guaranteed by design.
7. V_{OHC} applies to $\overline{\text{Run}}$ and $\overline{\text{Exception}}$.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3] — COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67MHz MIN.	16.67MHz MAX.	20.0MHz MIN.	20.0MHz MAX.	25.0MHz MIN.	25.0MHz MAX.	33.33MHz MIN.	33.33MHz MAX.	UNIT
Clock											
T_{CkHigh}	Input Clock High[2]	Transition < 5ns	12.5	—	10	—	8	—	6	—	ns
T_{CkLow}	Input Clock Low[2]	Transition < 5ns	12.5	—	10	—	8	—	6	—	ns
T_{CkP}	Input Clock Period[2]		30	500	25	500	20	500	15	500	ns
	Clk2xSys to Clk2xSmp[6]		0	tcyc/4	0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd[6]		0	tcyc/4	0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi[6]		9	tcyc/4	7	tcyc/4	5	tcyc/4	3.5	tcyc/4	ns
Run Operation											
T_{DEn}	Data Enable[3]		—	–2	—	–2	—	–1.5	—	–1	ns
T_{DDis}	Data Disable[3]		—	–1	—	–1	—	–0.5	—	–0.5	ns
T_{DVal}	Data Valid	Load = 25pF	—	3	—	3	—	2	—	2	ns
T_{WrDly}	Write Delay	Load = 25pF	—	5	—	4	—	3	—	2	ns
T_{DS}	Data Set–up		9	—	8	—	6	—	4.5	—	ns
T_{DH}	Data Hold		–2.5	—	–2.5	—	–2.5	—	–1.5	—	ns
T_{CBS}	CpBusy Set–up		13	—	11	—	9	—	7	—	ns
T_{CBH}	CpBusy Hold		–2.5	—	–2.5	—	–2.5	—	–1.5	—	ns
T_{AcTy}	Access Type (1:0)	Load = 25pF	—	7	—	6	—	5	—	4	ns
T_{AT2}	Access Type (2)	Load = 25pF	—	17	—	14	—	12	—	8.5	ns
T_{MWr}	Memory Write	Load = 25pF	1	27	1	23	1	18	1	9.5	ns
T_{Exc}	Exception	Load = 25pF	—	7	—	7	—	5	—	3.5	ns
Stall Operation											
T_{SAVal}	Address Valid	Load = 25pF	—	30	—	23	—	20	—	15	ns
T_{SAcTy}	Address Type	Load = 25pF	—	27	—	23	—	18	—	10	ns
T_{MRdi}	Memory Read Initiate	Load = 25pF	1	27	1	23	1	18	1	10	ns
T_{MRdt}	Memory Read Terminate	Load = 25pF	—	7	—	7	—	5	—	3.5	ns
T_{Stl}	Run Terminate	Load = 25pF	2	17	2	15	2	11	2	8	ns
T_{Run}	Run Initiate	Load = 25pF	—	7	—	6	—	4	—	3	ns
T_{SMWr}	Memory Write	Load = 25pF	1	27	1	23	1	18	1	9.5	ns
T_{SExc}	Exception Valid	Load = 25pF	—	20	—	18	—	15	—	10	ns
Reset Initialization											
T_{RST}	Reset Pulse Width		6	—	6	—	6	—	6	—	Tcyc
T_{rstPLL}	Reset timing, Phase–lock on[4, 5]		3000	—	3000	—	3000	—	3000	—	Tcyc
T_{rstcp}	Reset timing, Phase–lock off[4, 5]		128	—	128	—	128	—	128	—	Tcyc
Capacitive Load Deration											
CLD	Load Derate[6]		0.5	1	0.5	1	0.5	1	0.5	1	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters apply when the 79R3010 Floating Point Coprocessor is connected to the CPU. With phase lock on, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. With the exception of the $\overline{\text{Run}}$ signal, no two signals on a given device will derate for a given load by a difference greater than 15%.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3] — MILITARY TEMPERATURE RANGE (T_A = −55°C to +125°C, V_{CC} = +5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67MHz MIN.	16.67MHz MAX.	UNIT
Clock					
T_{CkHigh}	Input Clock High[2]	Transition < 5ns	12.5	—	ns
T_{CkLow}	Input Clock Low[2]	Transition < 5ns	12.5	—	ns
T_{CkP}	Input Clock Period[2]		30	500	ns
	Clk2xSys to Clk2xSmp[6]		0	tcyc/4	ns
	Clk2xSmp to Clk2xRd[6]		0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi[6]		9	tcyc/4	ns
Run Operation					
T_{DEn}	Data Enable[3]		—	−2	ns
T_{DDis}	Data Disable[3]		—	−1	ns
T_{DVal}	Data Valid	Load = 25pF	—	3	ns
T_{WrDly}	Write Delay	Load = 25pF	—	5	ns
T_{DS}	Data Set-up		9	—	ns
T_{DH}	Data Hold		−2.5	—	ns
T_{CBS}	CpBusy Set-up		13	—	ns
T_{CBH}	CpBusy Hold		−2.5	—	ns
T_{AcTy}	Access Type (1:0)	Load = 25pF	—	7	ns
T_{AT2}	Access Type (2)	Load = 25pF	—	17	ns
T_{MWr}	Memory Write	Load = 25pF	1	27	ns
T_{Exc}	Exception	Load = 25pF	—	7	ns
Stall Operation					
T_{SAVal}	Address Valid	Load = 25pF	—	30	ns
T_{SAcTy}	Address Type	Load = 25pF	—	27	ns
T_{MRdi}	Memory Read Initiate	Load = 25pF	1	27	ns
T_{MRdt}	Memory Read Terminate	Load = 25pF	—	7	ns
T_{Stl}	Run Terminate	Load = 25pF	2	17	ns
T_{Run}	Run Initiate	Load = 25pF	—	7	ns
T_{SMWr}	Memory Write	Load = 25pF	1	27	ns
T_{SExc}	Exception Valid	Load = 25pF	—	20	ns
Reset Initialization					
T_{RST}	Reset Pulse Width		6	—	Tcyc
T_{rstPLL}	Reset timing, Phase-lock on[4, 5]		3000	—	Tcyc
T_{rstcp}	Reset timing, Phase-lock off[4, 5]		128	—	Tcyc
Capacitive Load Deration					
CLD	Load Derate[6]		0.5	1	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters apply when the 79R3010 Floating Point Coprocessor is connected to the CPU. With phase lock on, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. With the exception of the $\overline{\text{Run}}$ signal, no two signals on a given device will derate for a given load by a difference greater than 15%.

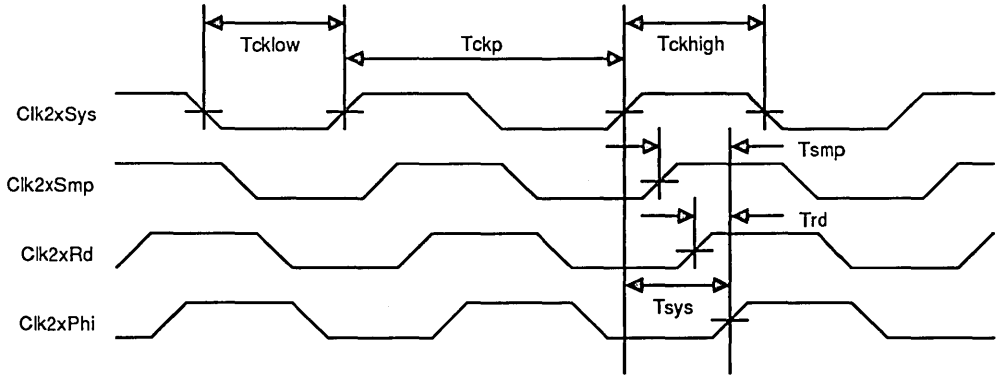
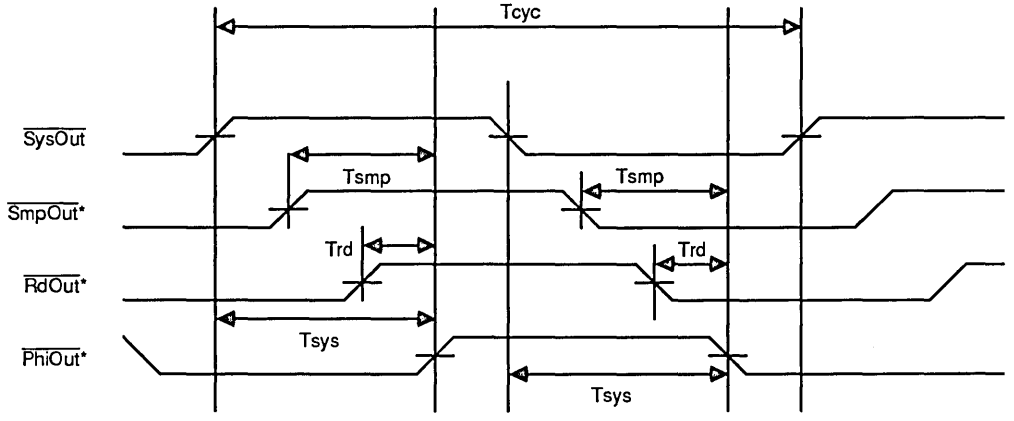


Figure 12. Input Clock Timing



* These signals are not actually output from the processor. They are drawn to provide a reference for other timing diagrams.

Figure 13. Processor Reference Clock Timing

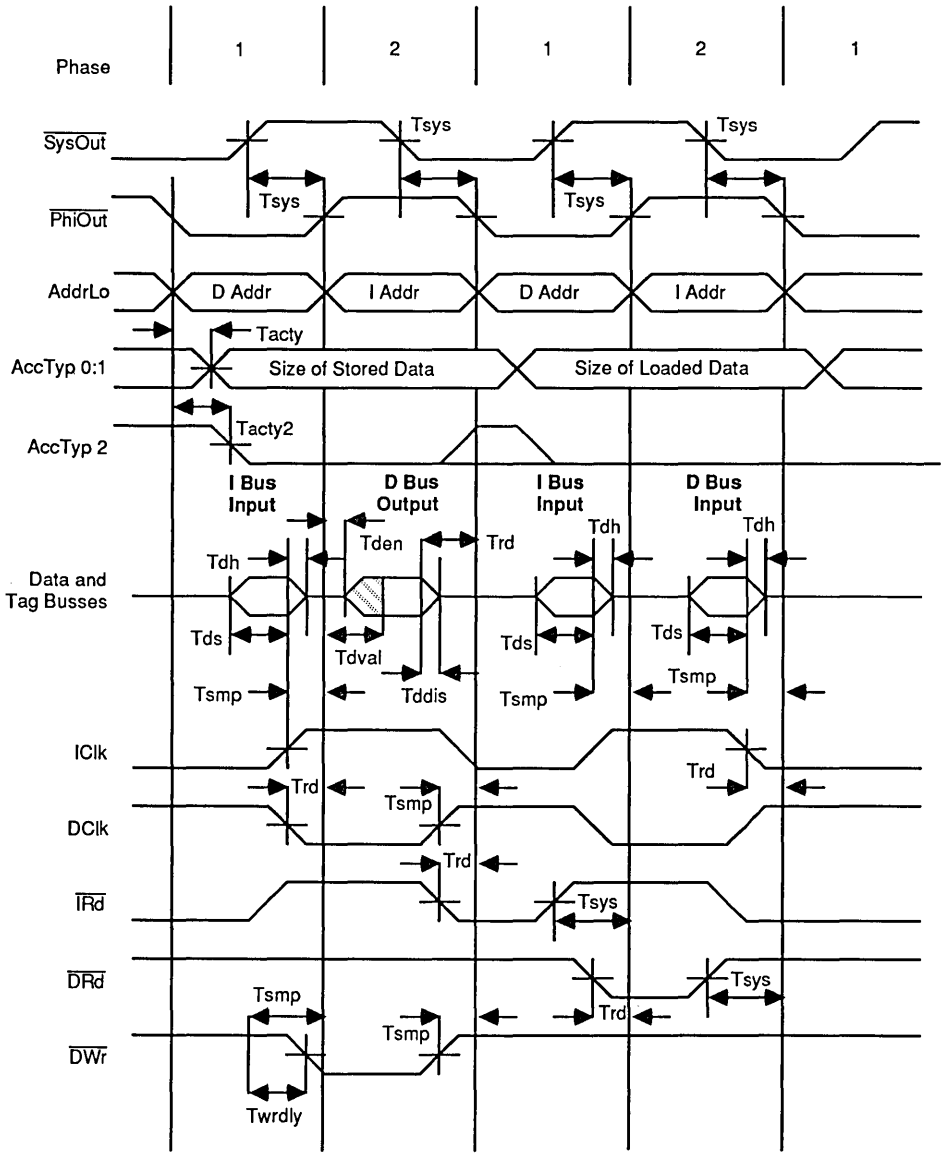


Figure 14. Synchronous Memory (Cache) Timing

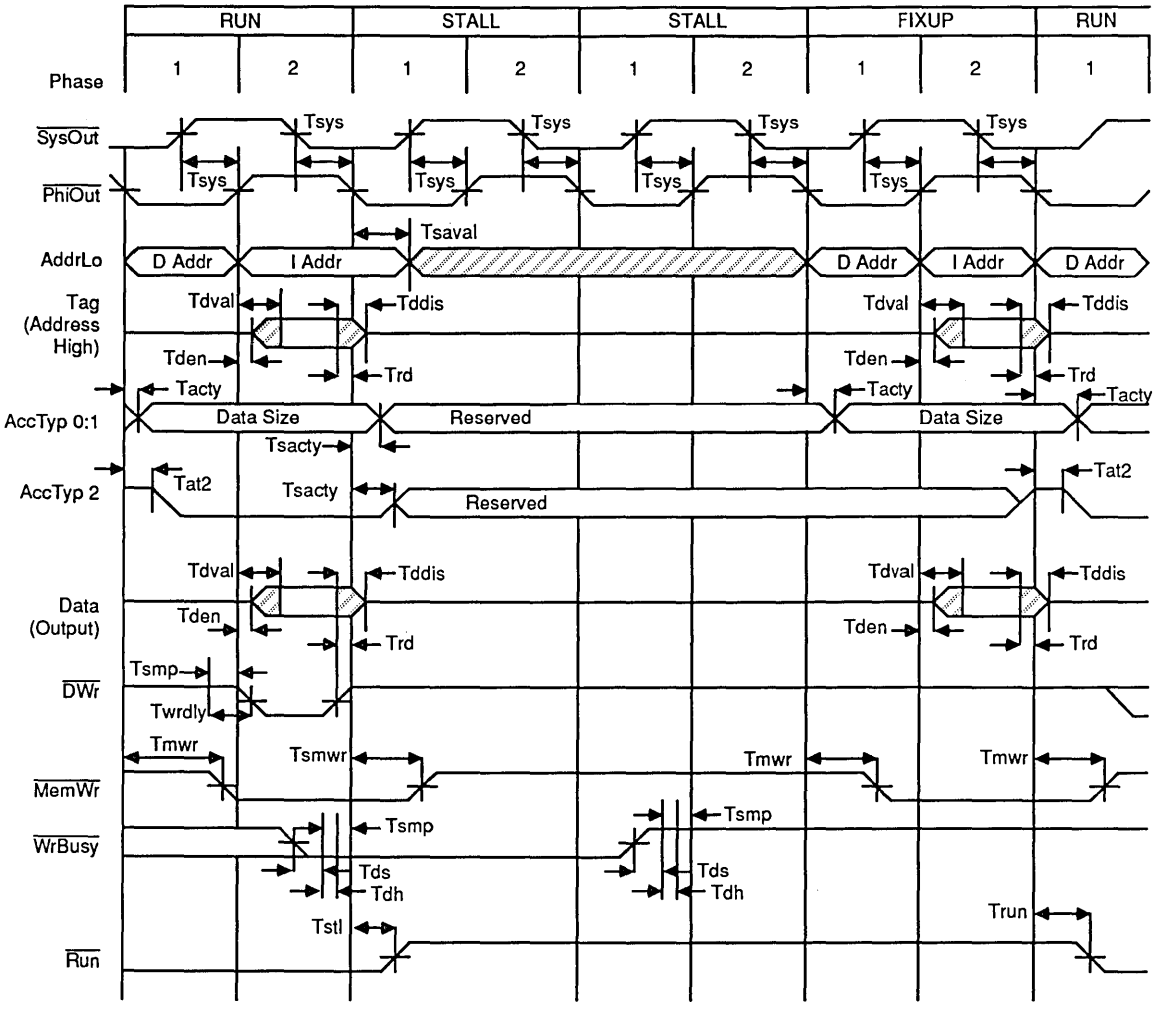


Figure 15. Memory Write Timing

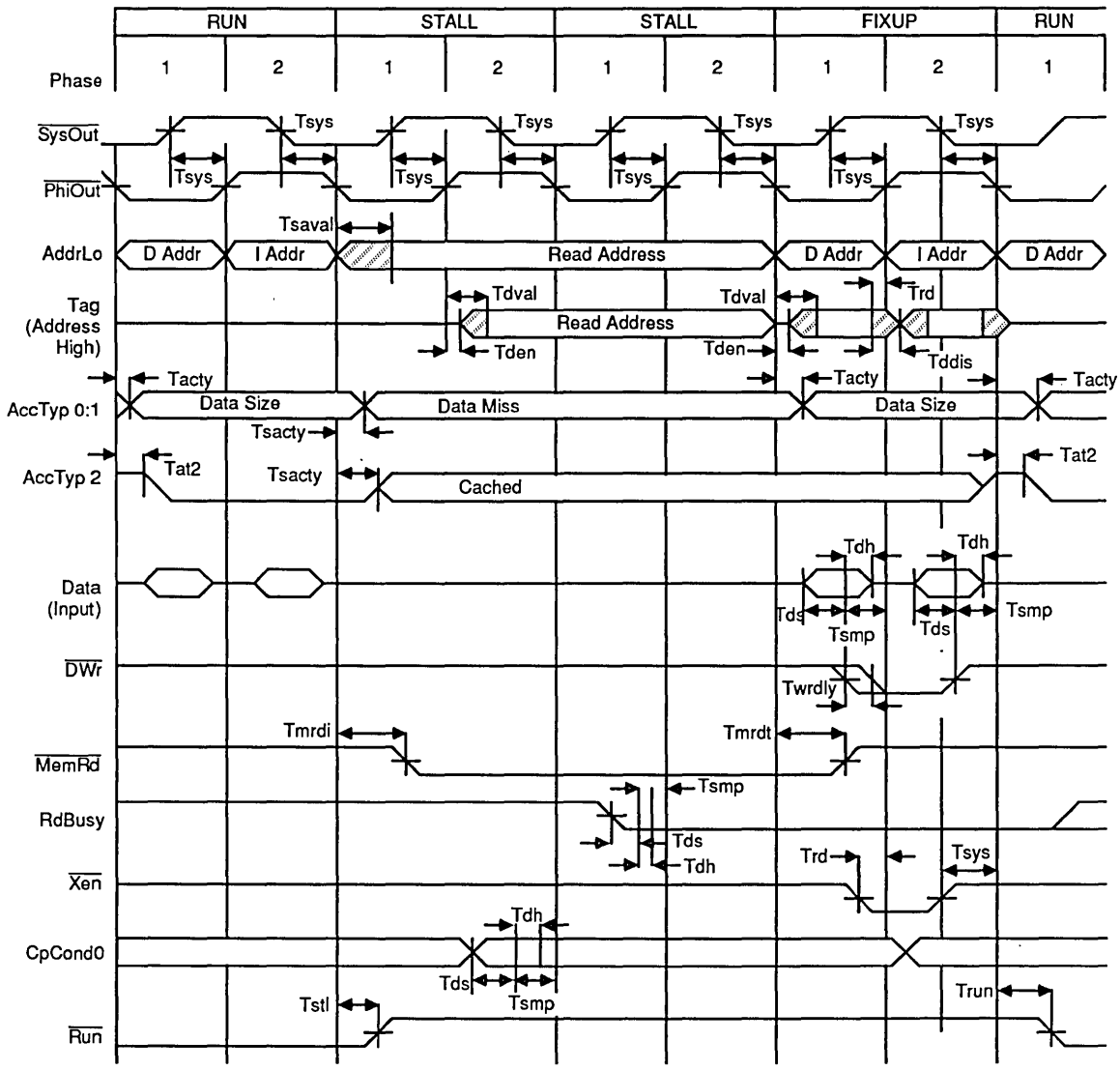


Figure 16. Memory Read Timing

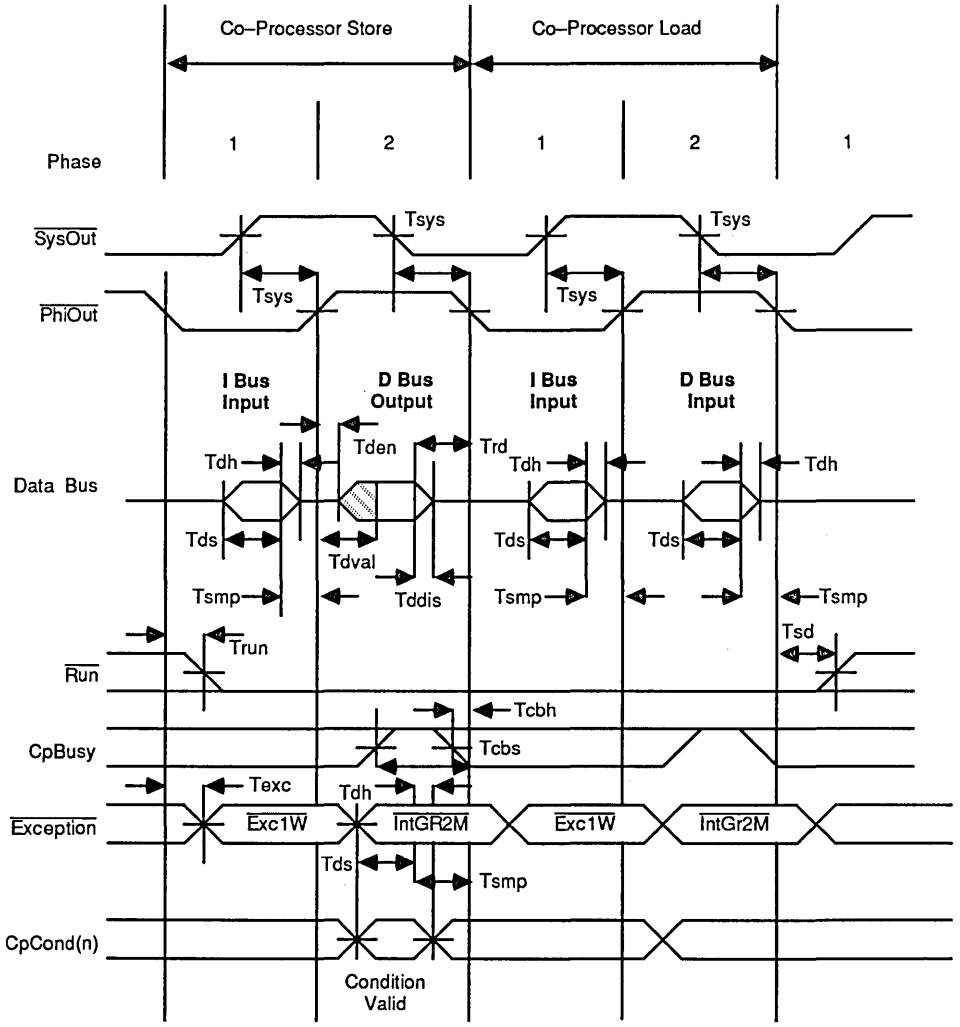


Figure 17. Co–Processor Load/Store Timing

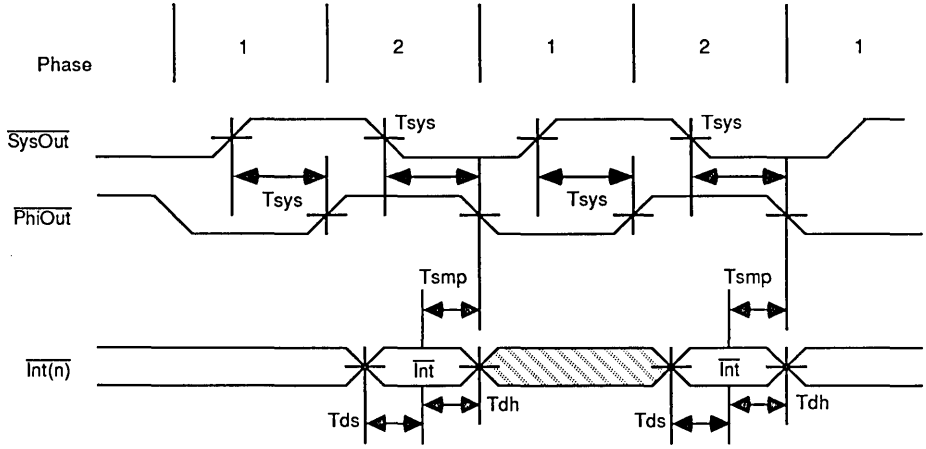
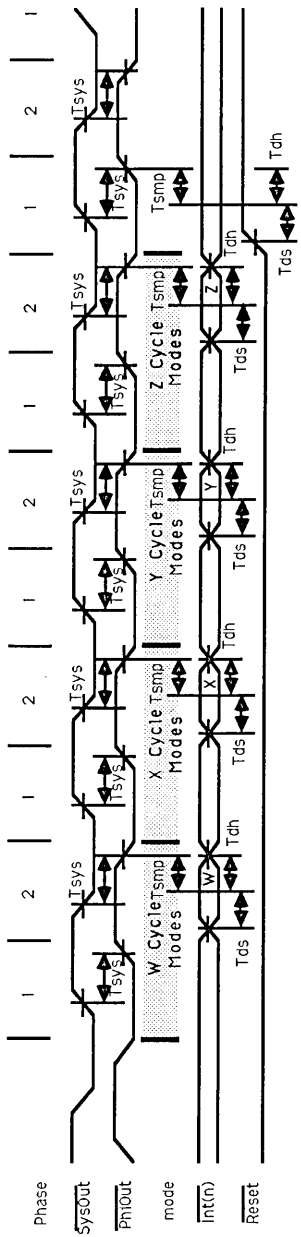


Figure 18. Interrupt Timing

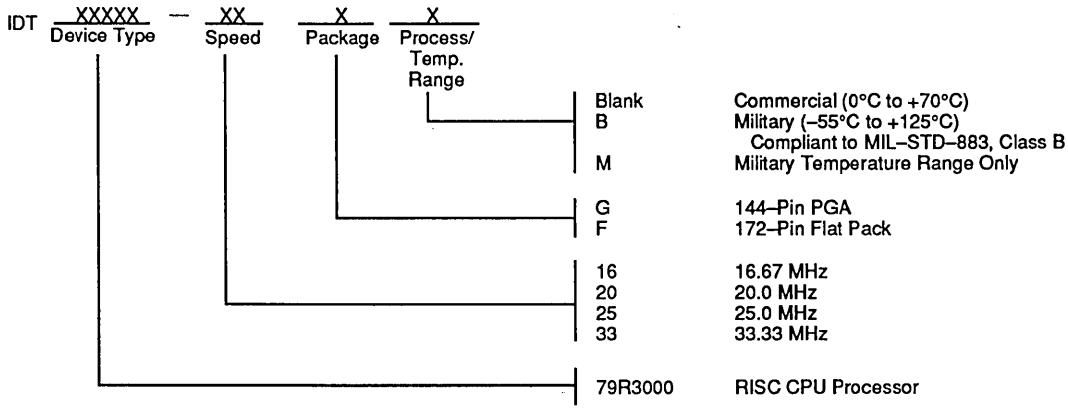


NOTES:

1. Reset must be negated synchronously; however, it can be asserted asynchronously. Designs should not rely on the proper functioning of $\overline{\text{SysOut}}$ prior to the assertion of $\overline{\text{Reset}}$.
2. If $\overline{\text{Phase-Lock On}}$ or $\overline{\text{R3000 Mode}}$ are asserted as mode select options, they should be asserted throughout the Reset period, to insure that the slowest co-processor in the system has sufficient time to lock the CPU clocks.
3. $\overline{\text{Reset}}$ is acturally sampled in both Phase 1 and Phase 2. To insure proper initialization, it is recommended that $\overline{\text{Reset}}$ be negated relative to the end of Phase 1.

Figure 19. Mode Vector Initialization

ORDERING INFORMATION



Integrated Device Technology, Inc.

RISC CPU PROCESSOR

PRELIMINARY
IDT79R3000A
IDT79R3000AE

FEATURES:

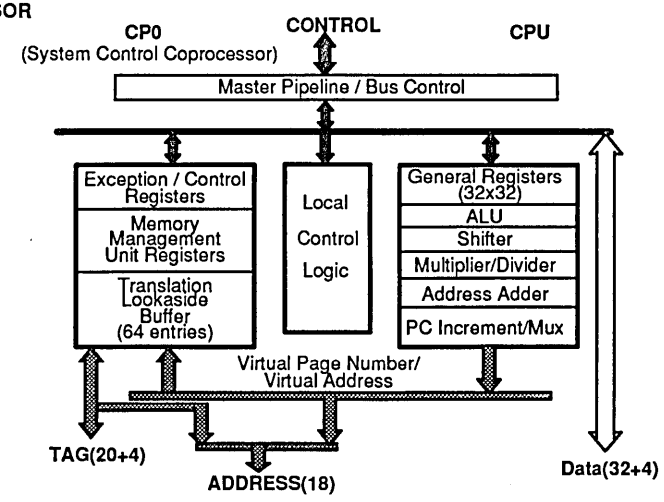
- Enhanced instruction set compatible version of the IDT79R2000, IDT79R3000 RISC CPUs.
- Upwardly pin–compatible with IDT79R3000 RISC CPU.
- IDT79R3000A "E" version relaxes system memory timing requirements.
- Full 32-bit Operation—Thirty-two 32-bit registers and all instructions and addresses are 32-bit.
- Efficient Pipelining—The CPU's 5-stage pipeline design assists in obtaining an execution rate approaching one instruction per cycle. Pipeline stalls and exceptions are handled precisely and efficiently.
- On-Chip Cache Control—The IDT79R3000 provides a high bandwidth memory interface that handles separate external Instruction and Data Caches ranging in size from 4 to 256 Kbytes each. Both the caches are accessed during a single CPU cycle. All cache control is on-chip.
- On-Chip Memory Management Unit—A fully-associative, 64 entry Translation Lookaside Buffer (TLB) provides fast address translation for virtual-to-physical memory mapping of the 4 Gigabyte virtual address space.
- Coprocessor Interface—The IDT79R3000 generates all addresses and handles memory interface control for up to three additional tightly coupled external processors.
- Optimizing Compilers are available for C, Fortran, Pascal, COBOL, Ada, and PL/1.
- UNIX™ System V.3 and BSD 4.3 operating systems supported.
- High-speed CEMOS™ technology.
- Instruction set compatible with the IDT79R2000 RISC CPU.
- 16.7MHz, 20MHz, 25MHz and 33MHz clock rates yield up to 28 MIPS sustained throughput.
- Supports independent multiword block refill of both the instruction and data caches with variable block sizes.
- Supports concurrent refill and execution of instructions.
- Partial word stores executed as read-modify-write operations.
- 6 external interrupt inputs (up to 64 different sources), 2 software interrupts, with single cycle latency to exception handler routine.
- Flexible multiprocessing support on chip with no impact on uniprocessor designs.
- Military product compliant to MIL-STD-883, Class B.

DESCRIPTION:

The IDT 79R3000A RISC Microprocessor consists of two tightly-coupled processors integrated on a single chip. The first processor is a full 32-bit CPU based on RISC (Reduced Instruction Set Computer) principles to achieve a new standard of microprocessor performance. The second processor is a system control coprocessor, called CP0, containing a fully-associative 64 entry TLB (Translation Lookaside Buffer), MMU (Memory Management Unit) and control registers, supporting a 4 Gigabyte virtual memory subsystem, and a Harvard Architecture Cache Controller achieving a bandwidth of over 260 Mbytes/second using industry standard static RAMs.

This data sheet provides an overview of the features and architecture of the 79R3000A CPU, Revision 3.0. A more detailed description of the operation of the device is incorporated in the "R3000A Family Hardware User Manual", and a more detailed architectural overview is provided in the "mips RISC Architecture" book, both available from IDT. Documentation providing details of the software and development environments supporting this processor are also available from IDT.

IDT79R3000A PROCESSOR



CEMOS is a trademark of Integrated Device Technology, Inc.
UNIX is a registered trademark of AT&T.

IDT79R3000A CPU Registers

The IDT79R3000A CPU provides 32 general purpose 32-bit registers, a 32-bit Program Counter, and two 32-bit registers that hold the results of integer multiply and divide operations. Only two of the 32 general registers have a special purpose: register r0 is hardwired to the value "0", which is a useful constant, and register r31 is used as the link register in jump-and-link instructions (return address for subroutine calls).

The CPU registers are shown in Figure 2. Note that there is no Program Status Word (PSW) register shown in this figure: the functions traditionally provided by a PSW register are instead provided in the *Status* and *Cause* registers incorporated within the System Control Coprocessor (CP0).

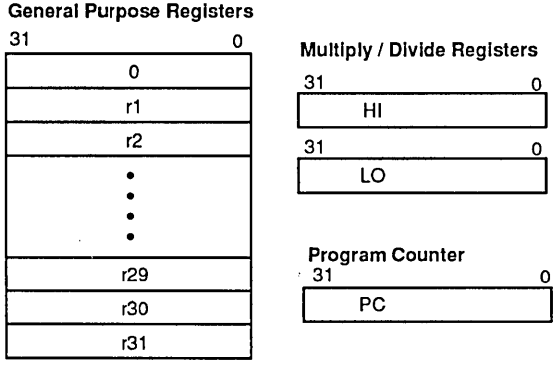


Figure 2. IDT79R3000A CPU Registers

Instruction Set Overview

All IDT79R3000A instructions are 32 bits long, and there are only three instruction formats. This approach simplifies instruction decoding thus minimizing instruction execution time. The 79R3000A processor initiates a new instruction on every run cycle, and is able to complete an instruction on almost every clock cycle. The only exceptions are the Load instructions and Branch instructions, which each have a single cycle of latency associated with their execution. Note, however, that in the majority of cases the compilers are able to fill these latency cycles with useful instructions which do not require the result of the previous instruction. This effectively eliminates these latency effects.

The actual instruction set of the CPU was determined after extensive simulations to determine which instructions should be implemented in hardware, and which operations are best synthesized in software from other basic instructions. This methodology resulted in the R3000A having the highest performance of any available microprocessor.

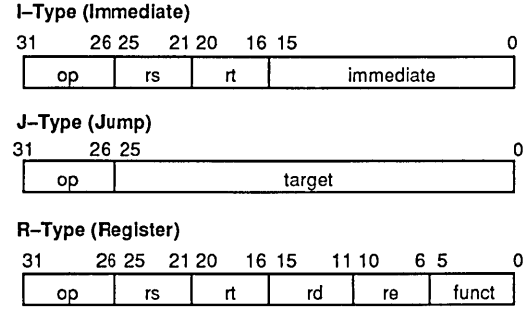


Figure 3. IDT79R3000A Instruction Formats

The IDT79R3000A instruction set can be divided into the following groups:

- **Load/Store** instructions move data between memory and general registers. They are all I-type instructions, since the only addressing mode supported is base register plus 16-bit, signed immediate offset.

  The Load instruction has a single cycle of latency, which means that the data being loaded is not available to the instruction immediately after the load instruction. The compiler will fill this delay slot with either an instruction which is not dependent on the loaded data, or with a NOP instruction. There is no latency associated with the store instruction.

  Loads and Stores can be performed on byte, half-word, word, or unaligned word data (32 bit data not aligned on a modulo-4 address). The CPU cache is constructed as a write-through cache.

- **Computational** instructions perform arithmetic, logical and shift operations on values in registers. They occur in both R-type (both operands and the result are registers) and I-type (one operand is a 16-bit immediate) formats.

  Note that computational instructions are three operand instructions; that is, the result of the operation can be stored into a different register than either of the two operands. This means that operands need not be overwritten by arithmetic operations. This results in a more efficient use of the large register set.

- **Jump and Branch** instructions change the control flow of a program. Jumps are always to a paged absolute address formed by combining a 26-bit target with four bits of the Program counter (J-type format, for subroutine calls), or 32-bit register byte addresses (R-type, for returns and dispatches). Branches have 16-bit offsets relative to the program counter (I-type). Jump and Link instructions save a return address in Register 31. The 79R3000A instruction set features a number of branch conditions. Included is the ability to compare a register to zero and branch, and also the ability to branch based on a comparison between two registers. Thus, net performance is increased since software does not have to perform arithmetic instructions prior to the branch to set up the branch conditions.

- **Coprocessor** instructions perform operations in the coprocessors. Coprocessor Loads and Stores are I-type. Coprocessor computational instructions have coprocessor-dependent formats (see coprocessor manuals).

- **Coprocessor 0** instructions perform operations on the System Control Coprocessor (CP0) registers to manipulate the memory management and exception handling facilities of the processor.

- **Special** instructions perform a variety of tasks, including movement of data between special and general registers, system calls, and breakpoint. They are always R-type.

Table 1 lists the instruction set of the IDT79R3000A processor.

OP	DESCRIPTION
	Load/Store Instructions
LB	Load Byte
LBU	Load Byte Unsigned
LH	Load Halfword
LHU	Load Halfword Unsigned
LW	Load Word
LWL	Load Word Left
LWR	Load Word Right
SB	Store Byte
SH	Store Halfword
SW	Store Word
SWL	Store Word Left
SWR	Store Word Right
	Arithmetic Instructions (ALU Immediate)
ADDI	Add Immediate
ADDIU	Add Immediate Unsigned
SLTI	Set on Less Than Immediate
SLTIU	Set on Less Than Immediate Unsigned
ANDI	AND Immediate
ORI	OR Immediate
XORI	Exclusive OR Immediate
LUI	Load Upper Immediate
	Arithmetic Instructions (3–operand, register–type)
ADD	Add
ADDU	Add Unsigned
SUB	Subtract
SUBU	Subtract Unsigned
SLT	Set on Less Than
SLTU	Set on Less Than Unsigned
AND	AND
OR	OR
XOR	Exclusive OR
NOR	NOR
	Shift Instructions
SLL	Shift Left Logical
SRL	Shift Right Logical
SRA	Shift Right Arithmetic
SLLV	Shift Left Logical Variable
SRLV	Shift Right Logical Variable
SRAV	Shift Right Arithmetic Variable

OP	DESCRIPTION
	Multiply/Divide Instructions
MULT	Multiply
MULTU	Multiply Unsigned
DIV	Divide
DIVU	Divide Unsigned
MFHI	Move From HI
MTHI	Move To HI
MFLO	Move From LO
MTLO	Move To LO
	Jump and Branch Instructions
J	Jump
JAL	Jump and Link
JR	Jump to Register
JALR	Jump and Link Register
BEQ	Branch on Equal
BNE	Branch on Not Equal
BLEZ	Branch on Less than or Equal to Zero
BGTZ	Branch on Greater Than Zero
BLTZ	Branch on Less Than Zero
BGEZ	Branch on Greater than or Equal to Zero
BLTZAL	Branch on Less Than Zero and Link
BGEZAL	Branch on Greater than or Equal to Zero and Link
	Special Instructions
SYSCALL	System Call
BREAK	Break
	Coprocessor Instructions
LWCz	Load Word from Coprocessor
SWCz	Store Word to Coprocessor
MTCz	Move To Coprocessor
MFCz	Move From Coprocessor
CTCz	Move Control to Coprocessor
CFCz	Move Control From Coprocessor
COPz	Coprocessor Operation
BCzT	Branch on Coprocessor z True
BCzF	Branch on Coprocessor z False
	System Control Coprocessor (CP0) Instructions
MTC0	Move To CP0
MFC0	Move From CP0
TLBR	Read indexed TLB entry
TLBWI	Write Indexed TLB entry
TLBWR	Write Random TLB entry
TLBP	Probe TLB for matching entry
RFE	Restore From Exception

Table 1. IDT79R3000A Instruction Summary

IDT79R3000A System Control Coprocessor (CP0)

The IDT79R3000A can operate with up to four tightly-coupled coprocessors (designated CP0 through CP3). The System Control Coprocessor (or CP0), is incorporated on the IDT79R3000 chip and supports the virtual memory system and exception handling functions of the IDT79R3000A. The virtual memory system is implemented using a Translation Lookaside Buffer and a group of programmable registers as shown in Figure 4.

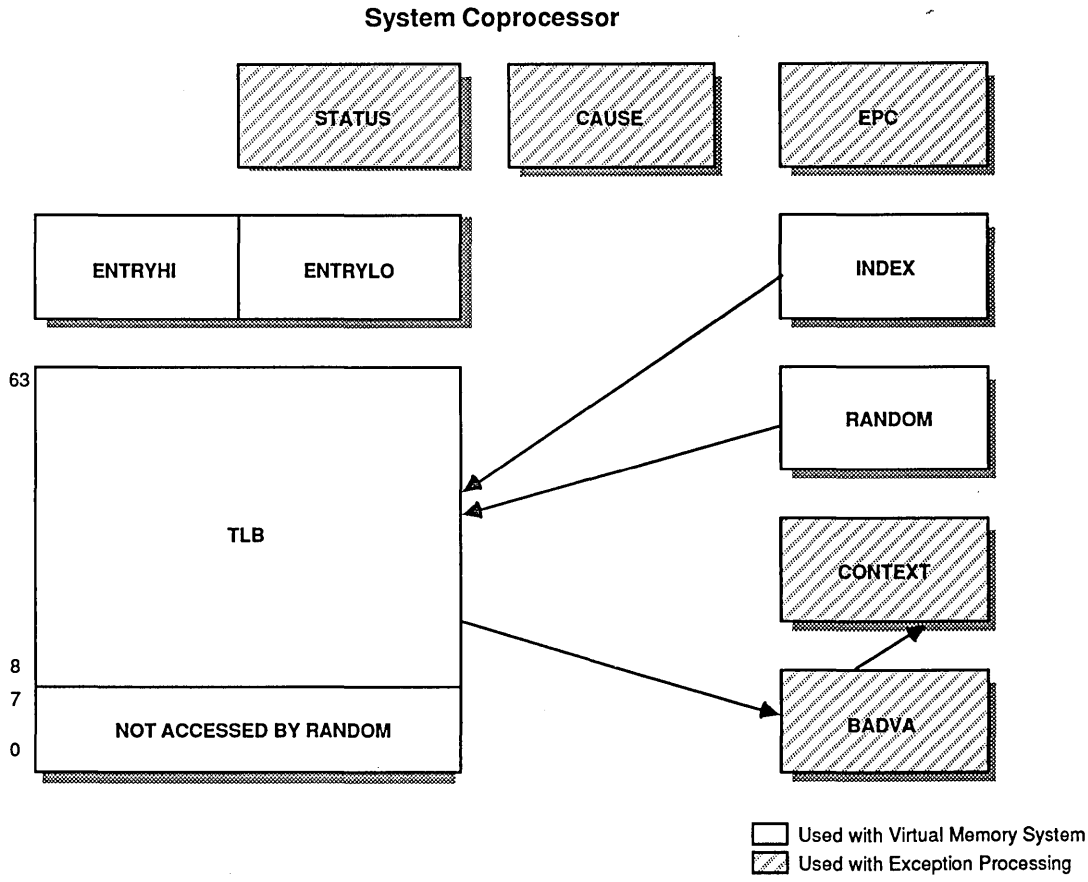


Figure 4. The System Coprocessor Registers

System Control Coprocessor (CP0) Registers

The CP0 registers shown in Figure 4 are used to control the memory management and exception handling capabilities of the IDT79R3000A. Table 2 provides a brief description of each register.

REGISTER	DESCRIPTION
EntryHi	High half of a TLB entry
EntryLo	Low half of a TLB entry
Index	Programmable pointer into TLB array
Random	Pseudo–random pointer into TLB array
Status	Mode, interrupt enables, and diagnostic status info
Cause	Indicates nature of last exception
EPC	Exception Program Counter
Context	Pointer into kernel's virtual Page Table Entry array
BadVA	Most recent bad virtual address
PRId	Processor revision identification (Read only)

Table 2. System Control Coprocessor (CP0) Registers

Memory Management System

The IDT79R3000A has an addressing range of 4 Gbytes. However, since most IDT79R3000A systems implement a physical memory smaller than 4 Gbytes, the IDT79R3000A provides for the logical expansion of memory space by translating addresses composed in a large virtual address space into available physical memory address. The 4 GByte address space is divided into 2 GBytes which can be accessed by both the users and the kernel, and 2 GBytes for the kernel only.

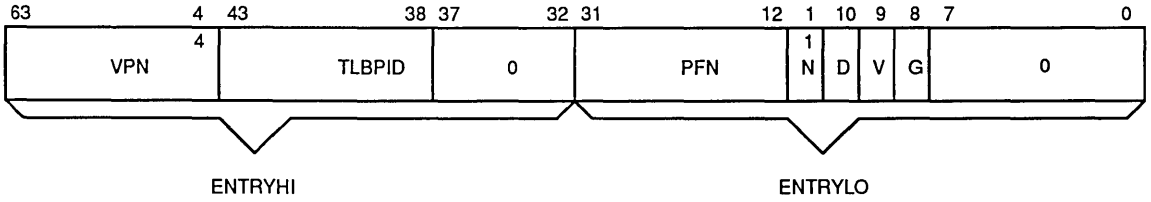
The TLB (Translation Lookaside Buffer)

Virtual memory mapping is assisted by the Translation Lookaside Buffer (TLB). The on-chip TLB provides very fast virtual memory access and is well-matched to the requirements of multitasking operating systems. The fully-associative TLB contains 64 entries, each of which maps a 4-Kbyte page, with controls for read/write access, cacheability, and process identification. The TLB allows each user to access up to 2 Gbytes of virtual address space.

Figure 5 illustrates the format of each TLB entry. The Translation operation involves matching the current Process ID (PID) and upper 20 bits of the address against PID and VPN (Virtual Page Number) fields in the TLB. When both match (or the TLB entry is Global), the VPN is replaced with the PFN (Physical Frame Number) to form the physical address.

TLB misses are handled in software, with the entry to be replaced determined by a simple RANDOM function. The routine to process a TLB miss in the UNIX environment requires only 10–12 cycles, which compares favorably with many CPUs which perform the operation in hardware.

TLB ENTRY FORMAT



VPN – Virtual Page number
TLBPID – Process ID
PFN – Physical frame number
N – Non-cacheable flag
D – Dirty flag (Write protect)
V – Valid entry flag
G – Global flag (ignore PID)
O – Reserved

Figure 5. TLB Entry Format

IDT79R3000 Operating Modes

The IDT79R3000A has two operating modes: *User* mode and *Kernel* mode. The IDT79R3000A normally operates in the User mode until an exception is detected forcing it into the Kernel mode. It remains in the Kernel mode until a Restore From Exception *(RFE)* instruction is executed. The manner in which memory addresses are translated or *mapped* depends on the operating mode of the IDT79R3000A. Figure 6 shows the MMU translation performed for each of the operating modes.

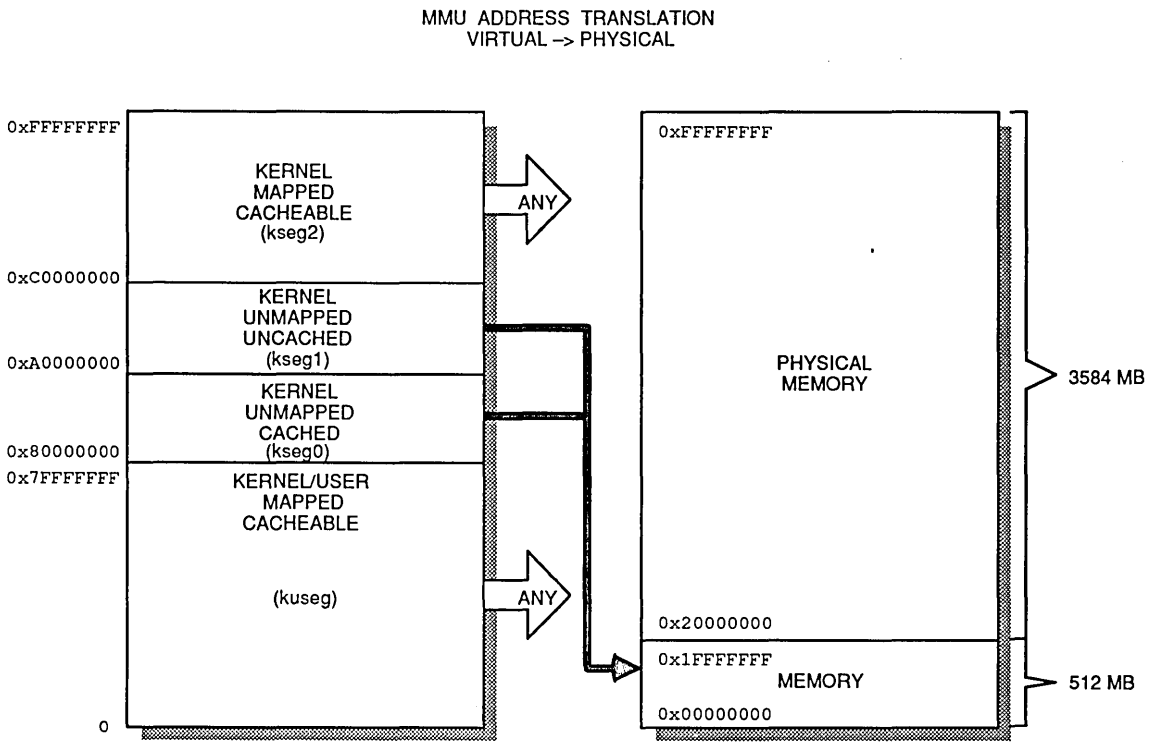


Figure 6. IDT79R3000A Virtual Address Mapping

User Mode—in this mode, a single, uniform virtual address space (kuseg) of 2 Gbyte is available. Each virtual address is extended with a 6-bit process identifier field to form unique virtual addresses. All references to this segment are mapped through the TLB. Use of the cache for up to 64 processes is determined by bit settings for each page within the TLB entries.

Kernel Mode—four separate segments are defined in this mode:

- *kuseg*—when in the kernel mode, references to this segment are treated just like user mode references, thus streamlining kernel access to user data.
- *kseg0*—references to this 512 Mbyte segment use cache memory but are not mapped through the TLB. Instead, they always map to the first 0.5 GBytes of physical address space.
- *kseg1*—references to this 512 Mbyte segment are not mapped through the TLB and do not use the cache. Instead, they are hard-mapped into the same 0.5 GByte segment of physical address space as *kseg0*.
- *kseg2*—references to this 1 Gbyte segment are always mapped through the TLB and use of the cache is determined by bit settings within the TLB entries.

IDT79R3000 Pipeline Architecture

The execution of a single IDT79R3000A instruction consists of five primary steps:

1) **IF** —Fetch the instruction (I-Cache).
2) **RD** —Read any required operands from CPU registers while decoding the instruction.
3) **ALU** —Perform the required operation on instruction operands.
4) **MEM**—Access memory (D-Cache).
5) **WB** —Write back results to register file.

Each of these steps requires approximately one CPU cycle as shown in Figure 7 (parts of some operations overlap into another cycle while other operations require only 1/2 cycle).

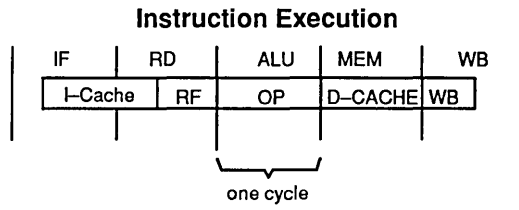


Figure 7. IDT79R3000A Instruction Pipeline

The IDT79R3000A uses a 5-stage pipeline to achieve an instruction execution rate approaching one instruction per CPU cycle. Thus, execution of five instructions at a time are overlapped as shown in Figure 8.

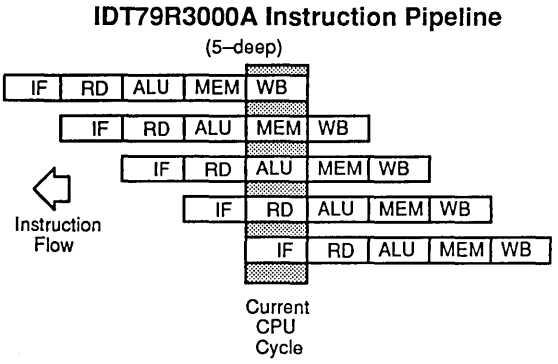


Figure 8. IDT79R3000A Execution Sequence

This pipeline operates efficiently because different CPU resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

Memory System Hierarchy

The high performance capabilities of the IDT79R3000A processor demand system configurations incorporating techniques frequently employed in large, mainframe computers but seldom encountered in systems based on more traditional microprocessors.

A primary goal of systems employing RISC techniques is to minimize the average number of cycles each instruction requires for execution. In order to achieve this goal, RISC processors incorporate a number of RISC techniques including a compact and uniform instruction set, a deep instruction pipeline (as described above), and utilization of optimizing compilers. Many of the advantages obtained from these techniques can, however, be negated by an inefficient memory system.

Figure 9 illustrates memory in a simple microprocessor system. In this system, the CPU outputs addresses to memory and reads instructions and data from memory or writes data to memory. The address space is completely undifferentiated: instructions, data, and I/O devices are all treated the same. In such a system, a primary limiting performance factor is memory bandwidth.

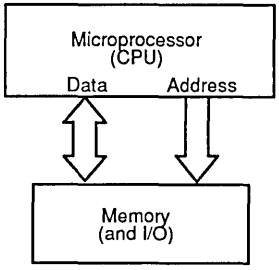


Figure 9. A Simple Microprocessor Memory System

Figure 10 illustrates a memory system that supports the significantly greater memory bandwidth required to take full advantage of the IDT79R3000A's performance capabilities. The key features of this system are:

- **External Cache Memory**—Local, high-speed memory (called *cache* memory) is used to hold instructions and data that is repetitively accessed by the CPU (for example, within a program loop) and thus reduces the number of references that must be made to the slower-speed main memory. Some microprocessors provide a limited amount of cache memory on the CPU chip itself. The external caches supported by the IDT79R3000A can be much larger; while a small cache can improve performance of some programs, significant improvements for a wide range of programs require large caches.
- **Separate Caches for data and Instructions**—Even with high-speed caches, memory speed can still be a limiting factor because of the fast cycle time of a high-performance microprocessor. The IDT79R3000A supports separate caches for instructions and data and alternates accesses of the two caches during each CPU cycle. Thus, the processor can obtain data and instructions at the cycle rate of the CPU using caches constructed with commercially available IDT static RAM devices.

  In order to maximize bandwidth in the cache while minimizing the requirement for SRAM access speed, the R3000A divides a single-processor clock cycle into two phases. During one phase, the address for the data cache access is presented while data previously addressed in the instruction cache is read; during the next phase, the data operation is completed while the instruction cache is being addressed. Thus, both caches are read in a single processor cycle using only one set of address and data pins.
- **Write Buffer**—In order to ensure data consistency, all data that is written to the data cache must also be written out to main memory. The cache write model used by the IDT79R3000A is that of a write-through cache; that is, all data written by the CPU is immediately written into the main memory. To relieve the CPU of this responsibility (and the inherent performance burden) the IDT79R3000A supports an interface to a write buffer. The IDT79R3020 Write Buffer captures data (and associated addresses) output by the CPU and ensures that the data is passed on to main memory.

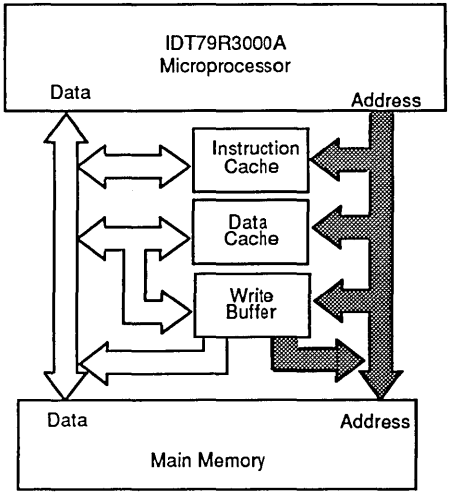


Figure 10. An IDT79R3000A System with a High-Performance Memory System

IDT79R3000A Processor Subsystem Interfaces

Figure 11 illustrates the three subsystem interfaces provided by the IDT79R3000A processor:

- **Cache control** interface (on-chip) for separate data and instruction caches permits implementation of off-chip caches using standard IDT SRAM devices. The 79R3000A directly controls the cache memory with a minimum of external components. Both the instruction and data cache can vary from 0 to 256K Bytes (64 K entries). The 79R3000A also includes the TAG control logic which determines whether or not the entry read from the cache is the desired data.

  The 79R3000A cache controller implements a direct mapped cache for high net performance (bandwidth). It has the ability to refill multiple words when a cache miss occurs, thus reducing the effective miss rate to less than 2% for large caches. When a cache miss occurs, the 79R3000A can support refilling the cache in 1, 4, 8, 16, or 32 word blocks to minimize the effective penalty of having to access main memory. The 79R3000A also incorporates the ability to perform instruction streaming; while the cache is refilling, the processor can resume execution once the missed word is obtained from main memory. In this way, the processor can continue to execute concurrently with the cache block refill.
- **Memory controller** interface for system (main) memory. This interface also includes the logic and signals to allow operation with a write buffer to further improve memory bandwidth. In addition to the standard full word access, the memory controller supports the ability to write bytes and half-words by using partial word operations. The memory controller also supports the ability to retry memory accesses if, for example, the data returned from memory is invalid and a bus error needs to be signalled.
- **Coprocessor Interface**—The IDT79R3000A features a tightly coupled co-processor interface in which all co-processors maintain synchronization with the main processor; reside on the same data bus as the main processor; and participate in bus transactions in an identical manner to the main processor. The IDT79R3000A generates all required cache and memory control signals, including cache and memory addresses for attached coprocessors. As a result, only the data bus and a few control signals need to be connected to a coprocessor.

  The interface supports three types of coprocessor instructions: loads/stores, coprocessor operations, and processor-coprocessor transfers. Note that coprocessor loads and stores occur directly between the coprocessor and memory, without requiring the data to go through the CPU.

  Synchronization between the CPU and external coprocessors is achieved using a Phased-Lock Loop interface to the coprocessor. The coprocessor physical interface also includes coprocessor condition signals (CpCond(n)), which are used in coprocessor branch instructions, and a coprocessor busy signal (CpBusy) which is used to stall the CPU if the coprocessor needs to hold off subsequent operations.

  Finally, a precise exception interface is defined between the CPU and coprocessors using the external interrupt inputs of the CPU. This allows a coprocessor exception, even if it was the result of a multi-cycle operation, to be traced to the precise coprocessor operation which caused it. This is an important feature for languages which can define specific error handlers for each task.

  The interface supports up to four separate coprocessors. Coprocessor 0 is defined to be the system control coprocessor, and resides on the same chip as the CPU unit. Coprocessor 1 is the Floating Point Accelerator, IDT 79R3010A. Coprocessors 2 and 3 are available to support an interface to application specific functions.

MULTIPROCESSING SUPPORT

The IDT79R3000A supports multiprocessing applications in a simple but effective way. Multiprocessing applications require cache coherency across the multiple processors. The IDT79R3000A offers two signals to support cache coherency: the first, MPStall, stalls the processor within two cycles of being received and keeps it from accessing the cache. This allows an external agent to snoop into the processor data cache. The second signal, MPInvalidate, causes the processor to write data on the data cache bus which indicates the externally addressed cache entry is invalid. Thus, a subsequent access to that location would result in a cache miss, and the data would be obtained from main memory.

The two MP signals would be generated by a external logic which utilizes a secondary cache to perform bus snooping functions. The 79R3000A does not impose an architecture for this secondary cache, but rather is flexible enough to support a variety of application specific architectures and still maintain cache coherency. Further, there is no impact on designs which do not require this feature. Further, the 79R3000A has improved on the microprocessor support found in the 79R3000, by allowing the use of cache RAMs with internal address latches in multiprocessor systems.

ADVANCED FEATURES

The IDT79R3000A offers a number of additional features such as the ability to swap the instruction and data caches, facilitating diagnostics and cache flushing. Another feature isolates the caches, which forces cache hits to occur regardless of the contents of the tag fields. The IDT79R3000A allows the processor to execute user tasks of the opposite byte ordering (endianness) of the operating system, and further allows parity checking to be disabled. More details on these features can be found in the IDT 79R3000A Family Hardware User's Manual.

Further features of the IDT79R3000A are configured during the last four cycles prior to the negation of the RESET input. These functions include the ability to select cache sizes and cache refill block sizes; the ability to utilize the multiprocessor interface; whether or not instruction streaming is enabled; whether byte ordering follows "Big-Endian" or "Little-Endian" protocols, etc. Table 3 shows the configuration options selected at Reset. These are further discussed in the "Hardware User's Manual".

BACKWARD COMPATIBILITY WITH 79R2000

The IDT79R3000A can be used in sockets designed for the 79R3000A. The pin-out of the 79R3000A has been selected to ensure this compatibility, with new functions mapped onto previously unused pins. The instruction set is compatible with that of the 79R2000 at the binary level. As a result, code written for the older processor can be executed. New features can be selectively disabled.

In most 79R3000A applications, the 79R3000A can be placed in the socket with no modification to initialization settings. Further application assistance on this topic is available from IDT.

PACKAGE THERMAL SPECIFICATIONS

The IDT79R3000 utilizes special packaging techniques to improve both the thermal and electrical characteristics of the microprocessor.

In order to improve the electrical characteristics of the device, the package is constructed using multiple signal planes, including individual power planes and ground planes to reduce noise associated with high-frequency TTL parts. In addition, the 175-pin PGA package utilizes extra power and ground pins to reduce tve inductance from the internal power planes to the power planes of the PC Board.

In order to improve the electrical characteristics of the microprocessor, the device is housed using cavity down packaging. In addition, these packages incorporate a copper–tungsten thermal slug designed to efficiently transfer heat from the die to the case of the package, and thus effectively lower the thermal resistance of the package. The use of an additional external heat sink affixed to the package thermal slug further decreases the effective thermal resistance of the package.

The case temperature may be measured in any environment to determine whether the device is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the package cavity (the package cavity is the side where the package lid is mounted).

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient (Øca) for the given package. The following equation relates ambient and case temperature:

$$T_A = T_C - P^*Øca$$

where P is the maximum power consumption, calculated by using the maximum I_{CC} from the DC Electrical Characteristics section.

Typical values for Øca at various airflows are shown in table 3 for the various CPU packages.

	Airflow - (ft/min)					
	0	200	400	600	800	1000
Øca (175–PGA, 144–PGA)	21	7	3	2	1	0.5
Øca (172 Quad Flatpack)	23	9	4	3	2.5	1.5

Table 3. Thermal Resistance (Øca) at Various Airflows

INPUT	W CYCLE	X CYCLE	Y CYCLE	Z CYCLE
$\overline{Int0}$	$\overline{DBlkSize0}$	$\overline{DBlkSize1}$	$\overline{Extend\ Cache}$	$\overline{BigEndian}$
$\overline{Int1}$	$\overline{IBlkSize0}$	$\overline{IBlkSize1}$	$\overline{MPAdrDisable}$	$\overline{TriState}$
$\overline{Int2}$	$\overline{DispPar/RevEnd}$	IStream	$\overline{IgnoreParity}$	$\overline{NoCache}$
$\overline{Int3}$	Reserved(1)	StorePartial	MultiProcessor	BusDriveOn
$\overline{Int4}$	$\overline{PhaseDelayOn}$(2)	$\overline{PhaseDelayOn}$(2)	$\overline{PhaseDelayOn}$(2)	$\overline{PhaseDelayOn}$(2)
$\overline{Int5}$	$\overline{R3000\ Mode}$(2)	$\overline{R3000\ Mode}$(2)	$\overline{R3000\ Mode}$(2)	$\overline{R3000\ Mode}$(2)

NOTES:
1. Reserved entries must be driven high.
2. These values must be driven stable throughout the entire RESET period.

Table 3: IDT79R3000A Mode Selectable Features

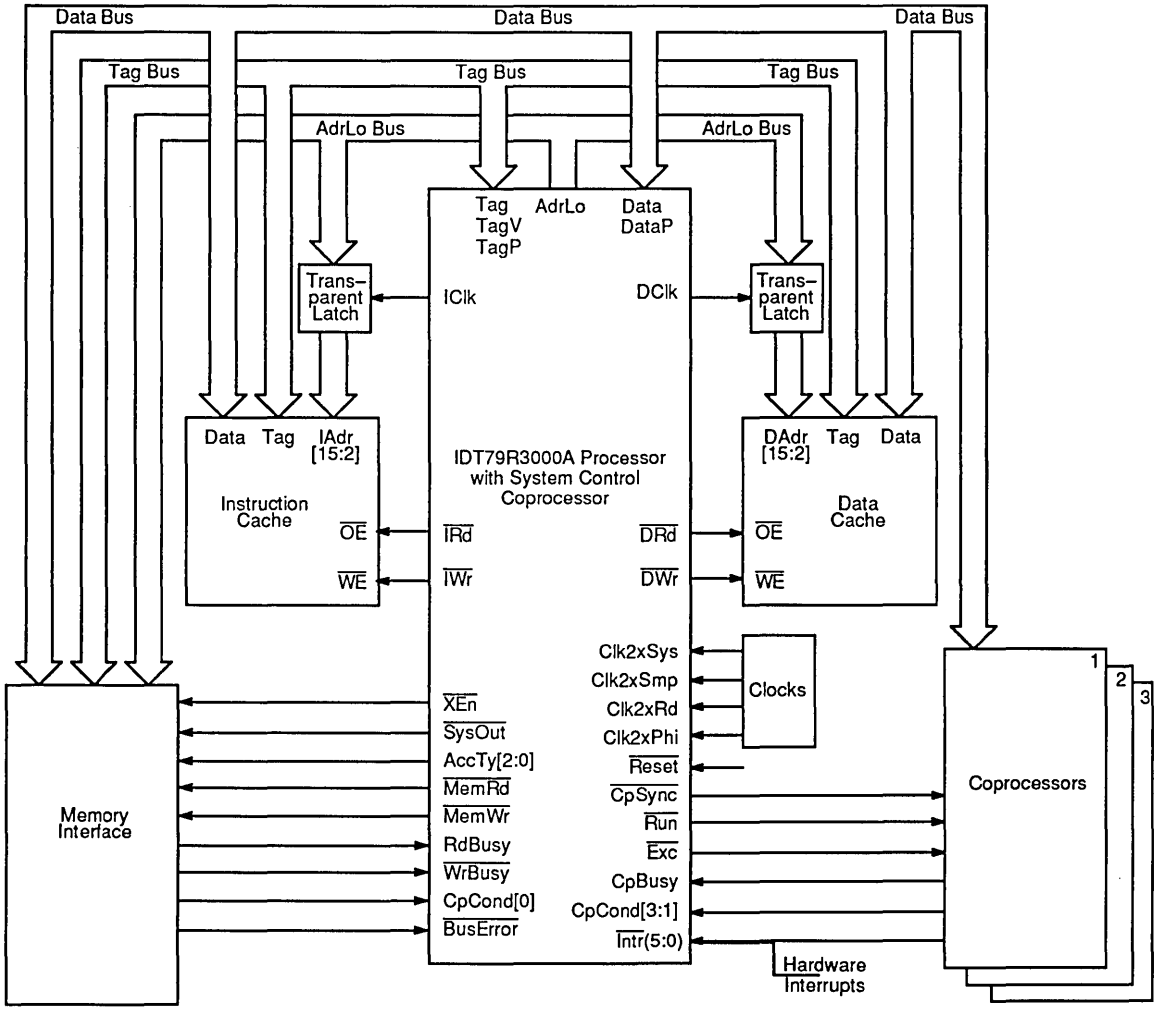
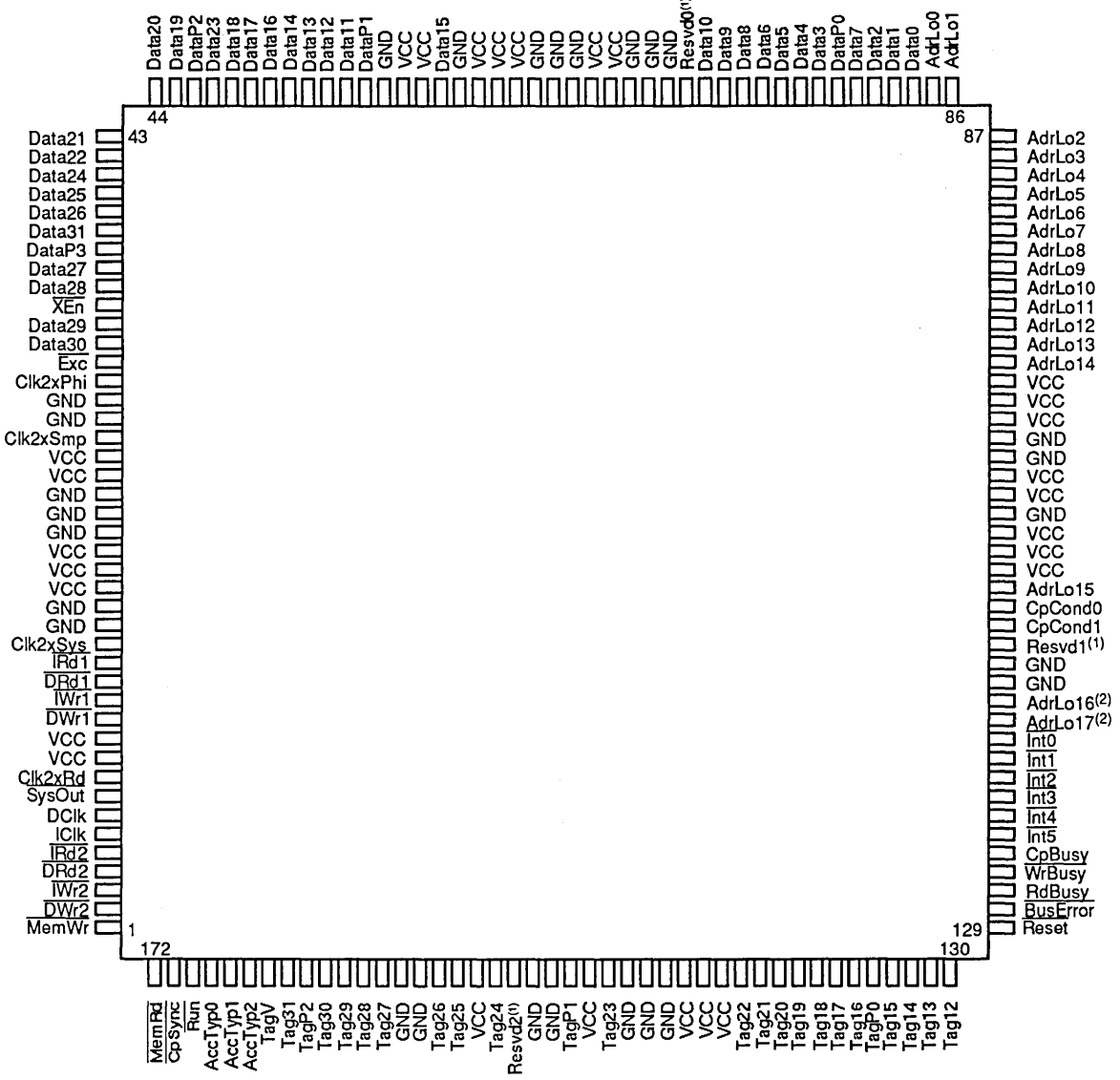


Figure 11. IDT79R3000A Subsystem Interfaces Example; 64 KB Caches

PIN CONFIGURATION



172-PIN CERAMIC FLATPACK
(Top View)

NOTES:

1. Reserved pins must not be connected.
2. AdrLo 16 & 17 are multi-function pins which are controlled by mode select programming on interrupt pins at reset time.
   AdrLo 16: MP Invalidate, CpCond (2).
   AdrLo 17: MP Stall, CpCond (3).

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VCC	AdrLo 6	AdrLo 10	AdrLo 11	VCC	AdrLo 14	AdrLo 15	CpCond 0	AdrLo[1] 16	AdrLo[1] 17	$\overline{\text{Intr2}}$	$\overline{\text{Intr5}}$	$\overline{\text{Wr}}$ $\overline{\text{Busy}}$	$\overline{\text{Reset}}$	VCC
B	AdrLo 3	$\overline{\text{DRd2}}$	AdrLo 7	AdrLo 9	AdrLo 12	$\overline{\text{IRd2}}$	AdrLo 13	CpCond 1	$\overline{\text{Intr1}}$	$\overline{\text{Intr3}}$	Cp Busy	$\overline{\text{Bus}}$ $\overline{\text{Error}}$	$\overline{\text{DR2}}$	Tag12	Tag15
C	AdrLo 0	AdrLo 4	VCC	AdrLo 5	AdrLo 8	GND	GND	VCC	$\overline{\text{Intr0}}$	$\overline{\text{Intr4}}$	Rd Busy	GND	Tag13	TagP0	Tag18
D	Data 1	AdrLo 2	GND										Tag14	Tag17	Tag19
E	DataP 0	Data 0	AdrLo 1										Tag16	Tag20	VCC
F	VCC	Data 7	Data 2										GND	Tag21	Tag23
G	Data 4	Data 3	GND										GND	Tag22	TagP1
H	Data 6	Data 5	Data 8										VCC	Tag25	Tag24
J	Data 10	DataP 1	Data 9										Tag28	Tag29	Tag26
K	Data 15	Data 11	GND										GND	Tag P2	Tag27
L	VCC	Data 12	Data 17										Acc Typ2	Tag31	Tag30
M	Data 13	Data 16	DataP 2										GND	Acc Typ1	VCC
N	Data 14	Data 18	Data 19	GND	Data 24	Data P3	VCC	VCC	GND	GND	$\overline{\text{DRd1}}$	$\overline{\text{Mem}}$ $\overline{\text{Wr}}$	$\overline{\text{Mem}}$ $\overline{\text{Rd}}$	$\overline{\text{Run}}$	TagV
P	Data 23	Data 20	$\overline{\text{IWr2}}$	Data 22	Data 26	Data 27	$\overline{\text{XEn}}$	Data 30	Clk2x Sys	Clk2x Rd	DClk	$\overline{\text{IRd1}}$	$\overline{\text{IWr1}}$	$\overline{\text{Cp}}$ $\overline{\text{Sync}}$	Acc Typ0
Q	VCC	Data 21	Data 25	Data 31	Data 28	GND	Data 29	$\overline{\text{Excep}}$ $\overline{\text{tion}}$	Clk2x Phi	Clk2x Smp	$\overline{\text{SysOut}}$	VCC	IClk	$\overline{\text{DWr1}}$	VCC

144-Pin PGA (Top View)

NOTE:

1. AdrLo 16 & 17 are multi-function pins which are controlled by mode select programming on interrupt pins at reset time.
   AdrLo16: MP Invalidate, CpCond (2).
   AdrLo17: MP Stall, CpCond (3).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A		AdrLo 6	AdrLo 10	AdrLo 11	VCC	AdrLo 14	AdrLo 15	CpCond 0	AdrLo(1) 16	AdrLo(1) 17	$\overline{\text{Intr2}}$	$\overline{\text{Intr5}}$	$\overline{\text{Wr}}$ / $\overline{\text{Busy}}$	$\overline{\text{Reset}}$	VCC
B	AdrLo 3	$\overline{\text{DRd2}}$	AdrLo 7	AdrLo 9	AdrLo 12	$\overline{\text{IRd2}}$	AdrLo 13	CpCond 1	$\overline{\text{Intr1}}$	$\overline{\text{Intr3}}$	Cp Busy	$\overline{\text{Bus}}$ / $\overline{\text{Error}}$	$\overline{\text{DR2}}$	Tag12	Tag15
C	AdrLo 0	AdrLo 4	VCC	AdrLo 5	AdrLo 8	GND	GND	VCC	$\overline{\text{Intr0}}$	$\overline{\text{Intr4}}$	Rd Busy	GND	Tag13	TagP0	Tag18
D	Data 1	AdrLo 2	GND	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	Tag14	Tag17	Tag19
E	DataP 0	Data 0	AdrLo 1	VCC								VCC	Tag16	Tag20	VCC
F	VCC	Data 7	Data 2	GND								GND	GND	Tag21	Tag23
G	Data 4	Data 3	GND	VCC								VCC	GND	Tag22	TagP1
H	Data 6	Data 5	Data 8	GND								GND	VCC	Tag25	Tag24
J	Data 10	DataP 1	Data 9	VCC								VCC	Tag28	Tag29	Tag26
K	Data 15	Data 11	GND	GND								GND	GND	Tag P2	Tag27
L	VCC	Data 12	Data 17	VCC								VCC	Acc Typ2	Tag31	Tag30
M	Data 13	Data 16	DataP 2	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	GND	Acc Typ1	VCC
N	Data 14	Data 18	Data 19	GND	Data 24	Data P3	VCC	VCC	GND	GND	$\overline{\text{DRd1}}$	$\overline{\text{Mem}}$ / $\overline{\text{Wr}}$	$\overline{\text{Mem}}$ / $\overline{\text{Rd}}$	$\overline{\text{Run}}$	TagV
P	Data 23	Data 20	$\overline{\text{IWr2}}$	Data 22	Data 26	Data 27	$\overline{\text{XEn}}$	Data 30	Clk2x Sys	Clk2x Rd	DClk	$\overline{\text{IRd1}}$	$\overline{\text{IWr1}}$	$\overline{\text{Cp}}$ / $\overline{\text{Sync}}$	Acc Typ0
Q	VCC	Data 21	Data 25	Data 31	Data 28	GND	Data 29	$\overline{\text{Excep}}$ / $\overline{\text{tion}}$	Clk2x Phi	Clk2x Smp	$\overline{\text{SysOut}}$	VCC	IClk	$\overline{\text{DWr1}}$	VCC

175-Pin PGA (Top View)

NOTE:

1. AdrLo 16 & 17 are multi-function pins which are controlled by mode select programming on interrupt pins at reset time.
   AdrLo16: MP Invalidate, CpCond (2).
   AdrLo17: MP Stall, CpCond (3).

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
Data (0–31)	I/O	A 32-bit bus used for all instruction and data transmission among the processor, caches, memory interface, and coprocessors.
DataP (0–3)	I/O	A 4-bit bus containing even parity over the data bus.
Tag (12–31)	I/O	A 20-bit bus used for transferring cache tags and high addresses between the processor, caches, and memory interface.
TagV	I/O	The tag validity indicator.
TagP (0–2)	I/O	A 3-bit bus containing even parity over the concatenation of TagV and Tag.
AdrLo (0–17)	O	An 18-bit bus containing byte addresses used for transferring low addresses from the processor to the caches and memory interface. (AdrLo 16: CpCond (2), AdrLo 17: CpCond (3) set by reset initialization).
$\overline{\text{IRd1}}$	O	Read enable for the instruction cache.
$\overline{\text{IWr1}}$	O	Write enable for the instruction cache.
$\overline{\text{IRd2}}$	O	An identical copy of $\overline{\text{IRd1}}$ used to split the load.
$\overline{\text{IWr2}}$	O	An identical copy of $\overline{\text{IWr1}}$ used to split the load.
IClk	O	The instruction cache address latch clock. This clock runs continuously.
$\overline{\text{DRd1}}$	O	The read enable for the data cache.
$\overline{\text{DWr1}}$	O	The write enable for the data cache.
$\overline{\text{DRd2}}$	O	An identical copy of $\overline{\text{DRd1}}$ used to split the load.
$\overline{\text{DWr2}}$	O	An identical copy of $\overline{\text{DWr1}}$ used to split the load.
DClk	O	The data cache address latch clock. This clock runs continuously.
$\overline{\text{XEn}}$	O	The read enable for the Read Buffer.
AccTyp (0–2)	O	A 3-bit bus used to indicate the size of data being transferred on the data bus, whether or not a data transfer is occurring, and the purpose of the transfer.
$\overline{\text{MemWr}}$	O	Signals the occurrence of a main memory write
$\overline{\text{MemRd}}$	O	Signals the occurrence of a main memory read.
$\overline{\text{BusError}}$	I	Signals the occurrence of a bus error during a main memory read or write.
$\overline{\text{Run}}$	O	Indicates whether the processor is in the run or stall state.
$\overline{\text{Exception}}$	O	Indicates that the instruction about to commit state should be aborted and other exception related information.
$\overline{\text{SysOut}}$	O	A reflection of the internal processor clock used to generate the system clock.
$\overline{\text{CpSync}}$	O	A clock which is identical to $\overline{\text{SysOut}}$ and used by coprocessors for timing synchronization with the CPU.
RdBusy	I	The main memory read stall termination signal. In most system designs RdBusy is normally asserted and is deasserted only to indicate the successful completion of a memory read. RdBusy is sampled by the processor only during memory read stalls.
$\overline{\text{WrBusy}}$	I	The main memory write stall initiation/termination signal.
CpBusy	I	The coprocessor busy stall initiation/termination signal.
CpCond (0–1)	I	A 2-bit bus used to transfer conditional branch status from the coprocessors to the main processor.
CpCond (2–3)	I	Conditional branch status from coprocessors to the processor. Function is provided on AdrLo 16/17 pins and is selected at reset time.
MPStall	I	Multiprocessing Stall. Signals to the processor that it should stall accesses to the caches in a multiprocessing environment. This is physically the same pin as CpCond3; its use is determined at RESET initialization.
MPInvalidate	I	Multiprocessing Invalidate. Signals to the processor that it should issue invalidate data on the cache data bus. The address to be invalidated is externally provided. This is the same pin as CpCond2; its use is determined at RESET initialization.
$\overline{\text{Int}}$ (0–5)	I	A 6-bit bus used by the memory interface and coprocessors to signal maskable interrupts to the processor. At reset time, mode select values are read in.
Clk2xSys	I	The master double frequency input clock used for generating $\overline{\text{SysOut}}$.
Clk2xSmp	I	A double frequency clock input used to determine the sample point for data coming into the processor and coprocessors.
Clk2xRd	I	A double frequency clock input used to determine the enable time of the cache RAMs.
Clk2xPhi	I	A double frequency clock input used to determine the position of the internal phases, phase1 and phase2.
$\overline{\text{Reset}}$	I	Synchronous initialization input used to force execution starting from the reset memory address. $\overline{\text{Reset}}$ must be deasserted synchronously but asserted asynchronously. The deassertion of $\overline{\text{reset}}$ must be synchronized by the leading edge of SysOut.

ABSOLUTE MAXIMUM RATINGS[1, 3]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A,T_C	Operating Temperature	0 to +70 (Ambient)	–55 to +125 (Case)	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature[2]	–55 to +125	–65 to +150	°C
V_{IN}	Input Voltage	–0.5 to +7.0	–0.5 to +7.0	V

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –3.0V for pulse width less than 15ns.
   V_{IN} should not exceed V_{CC} +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

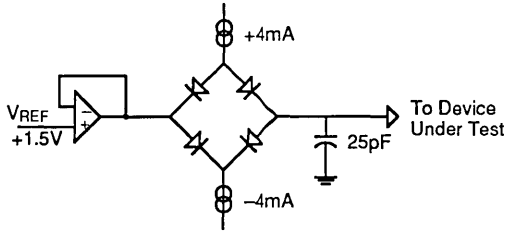
AC TEST CONDITIONS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{IH}	Input HIGH Voltage	3.0	—	V
V_{IL}	Input LOW Voltage	—	0.4	V
V_{IHS}	Input HIGH Voltage	3.5	—	V
V_{ILS}	Input LOW Voltage	—	0.4	V

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	TEMPERATURE	GND	V_{CC}
Military	–55°C to +125°C (Case)	0V	5.0 ± 10%
Commercial	0°C to +70°C (Ambient)	0V	5.0 ± 5%

OUTPUT LOADING FOR AC TESTING



DC ELECTRICAL CHARACTERISTICS— COMMERCIAL TEMPERATURE RANGE T_A = 0°C to +70°C, V_{CC} = +5.0V ± 5%

SYMBOL	PARAMETER	TEST CONDITIONS	16.67MHz		20.0MHz		25.0MHz		33.33MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{OHC}	Output HIGH Voltage(7)	V_{CC} = Min., I_{OH} = –4mA	4.0	—	4.0	—	4.0	—	4.0	—	V
V_{OHT}	Output HIGH Voltage (4, 6)	V_{CC} = Min., I_{OH} = –8mA	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OLT}	Output LOW Voltage (4, 6)	V_{CC} = Min., I_{OL} = 8mA	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IH}	Input HIGH Voltage (5)		2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage (1)		—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage (2, 5)		3.0	—	3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage (1, 2)		—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance (6)		—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance (6)		—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 70°C	—	450	—	550	—	650	—	750	mA
I_{IH}	Input HIGH Leakage (3)	V_{IH} = V_{CC}	—	10	—	10	—	10	—	10	µA
I_{IL}	Input LOW Leakage (3)	V_{IL} = GND	–10	—	–10	—	–10	—	–10	—	µA
I_{OZ}	Output Tri–state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–40	40	–40	40	–40	40	–40	40	µA

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag busses only. Note that V_{IH} and V_{IL} also apply to these signals. V_{OHT} and V_{OLT} are provided to give the designer further information about these specific signals.
5. V_{IH} should not be held above Vcc + 0.5 volts.
6. Guaranteed by design.
7. V_{OHC} applies to $\overline{\text{RUN}}$ and $\overline{\text{Exception}}$.

DC ELECTRICAL CHARACTERISTICS— MILITARY TEMPERATURE RANGE (T_C = –55°C to +125°C, V_{CC} = +5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67MHz		20.0MHz		25.0MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	V
V_{OHC}	Output HIGH Voltage(7)	V_{CC} = Min., I_{OH} = –4mA	4.0	—	4.0	—	4.0	—	V
V_{OHT}	Output HIGH Voltage (4, 6)	V_{CC} = Min., I_{OH} = –8mA	2.4	—	2.4	—	2.4	—	V
V_{OLT}	Output LOW Voltage (4, 6)	V_{CC} = Min., I_{OL} = 8mA	—	0.8	—	0.8	—	0.8	V
V_{IH}	Input HIGH Voltage (5)		2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage (1)		—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage (2, 5)		3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage (1, 2)		—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance (6)		—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance (6)		—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 70°C	—	550	—	675	—	775	mA
I_{IH}	Input HIGH Leakage (3)	V_{IH} = V_{CC}	—	10	—	10	—	10	µA
I_{IL}	Input LOW Leakage (3)	V_{IL} = GND	–10	—	–10	—	–10	—	µA
I_{OZ}	Output Tri–state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–40	40	–40	40	–40	40	µA

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag busses only. Note that V_{IH} and V_{IL} also apply to these signals. V_{OHT} and V_{OLT} are provided to give the designer further information about these specific signals.
5. V_{IH} should not be held above Vcc + 0.5 volts.
6. Guaranteed by design.
7. V_{OHC} applies to $\overline{\text{RUN}}$ and $\overline{\text{Exception}}$.

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3000A[1, 2, 3] — COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67MHz MIN.	16.67MHz MAX.	20.0MHz MIN.	20.0MHz MAX.	25.0MHz MIN.	25.0MHz MAX.	33.33MHz MIN.	33.33MHz MAX.	UNIT
Clock											
T_{CkHigh}	Input Clock High[2]	Note 7	12.5	—	10	—	8	—	6	—	ns
T_{CkLow}	Input Clock Low[2]	Note 7	12.5	—	10	—	8	—	6	—	ns
T_{CkP}	Input Clock Period[2]		30	500	25	500	20	500	15	500	ns
	Clk2xSys to Clk2xSmp[6]		0	tcyc/4	0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd[6]		0	tcyc/4	0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi[6]		9	tcyc/4	7	tcyc/4	5	tcyc/4	4.5	tcyc/4	ns
Run Operation											
T_{DEn}	Data Enable[3]		—	–2	—	–2	—	–1.5	—	–1.5	ns
T_{DDis}	Data Disable[3]		—	–1	—	–1	—	–0.5	—	–0.5	ns
T_{DVal}	Data Valid	Load = 25pF	—	3	—	3	—	3	—	2.5	ns
T_{WrDly}	Write Delay	Load = 25pF	—	5	—	4	—	3	—	3	ns
T_{DS}	Data Set–up		9	—	8	—	7	—	5	—	ns
T_{DH}	Data Hold[3]		–2.5	—	–2.5	—	–2.5	—	–2.5	—	ns
T_{CBS}	CpBusy Set–up		13	—	11	—	9	—	7	—	ns
T_{CBH}	CpBusy Hold		–2.5	—	–2.5	—	–2.5	—	–2.5	—	ns
T_{AcTy}	Access Type (1:0)	Load = 25pF	—	7	—	6	—	5	—	3.5	ns
T_{AT2}	Access Type (2)	Load = 25pF	—	17	—	14	—	12	—	8.5	ns
T_{MWr}	Memory Write	Load = 25pF	—	27	—	23	—	18	—	13.5	ns
T_{Exc}	Exception	Load = 25pF	—	7	—	7	—	5	—	3.5	ns
T_{Aval}	Address Valid	Load = 25pF	—	2	—	2	—	2	—	1	ns
T_{IntS}	$\overline{Int(n)}$ Set–up		9	—	8	—	7	—	5	—	ns
T_{IntH}	$\overline{Int(n)}$ Hold		–2.5	—	–2.5	—	–2.5	—	–2.5	—	ns
Stall Operation											
T_{SAVal}	Address Valid	Load = 25pF	—	30	—	23	—	20	—	15	ns
T_{SAcTy}	Address Type	Load = 25pF	—	27	—	23	—	18	—	13.5	ns
T_{MRdi}	Memory Read Initiate	Load = 25pF	1	27	1	23	1	18	1	13.5	ns
T_{MRdt}	Memory Read Terminate	Load = 25pF	—	27	—	23	—	18	—	13.5	ns
T_{Stl}	Run Terminate	Load = 25pF	3	17	3	15	3	10	2	7.5	ns
T_{Run}	Run Initiate	Load = 25pF	—	7	—	6	—	4	—	2	ns
T_{SMWr}	Memory Write	Load = 25pF	3	27	3	23	3	18	2	13.5	ns
T_{SExc}	Exception Valid	Load = 25pF	—	15	—	13	—	10	—	7.5	ns
Reset Initialization											
T_{RST}	Reset Pulse Width		6	—	6	—	6	—	6	—	Tcyc
T_{rstPLL}	Reset timing, Phase–lock on[4, 5]		3000	—	3000	—	3000	—	3000	—	Tcyc
T_{rstcp}	Reset timing, Phase–lock off[4, 5]		128	—	128	—	128	—	128	—	Tcyc
Capacitive Load Deration											
CLD	Load Derate[6]		0.5	2	0.5	1	0.5	1	0.5	1	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters apply when the 79R3010 Floating Point Coprocessor is connected to the CPU. With phase lock on, $\overline{Reset}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. With the exception of the $\overline{Run}$ signal, no two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 2.5ns for 33.33 MHz; clock transition time < 5ns for other speeds.

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3000AE[1, 2, 3] — COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67MHz MIN.	16.67MHz MAX.	20.0MHz MIN.	20.0MHz MAX.	25.0MHz MIN.	25.0MHz MAX.	33.33MHz MIN.	33.33MHz MAX.	UNIT
Clock											
T_{CkHigh}	Input Clock High[2]	Note 7	12.5	—	10	—	8	—	6	—	ns
T_{CkLow}	Input Clock Low[2]	Note 7	12.5	—	10	—	8	—	6	—	ns
T_{CkP}	Input Clock Period[2]		30	500	25	500	20	500	15	500	ns
	Clk2xSys to Clk2xSmp[6]		0	tcyc/4	0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd[6]		0	tcyc/4	0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi[6]		9	tcyc/4	7	tcyc/4	5	tcyc/4	3.5	tcyc/4	ns
Run Operation											
T_{DEn}	Data Enable[3]		—	-2	—	-2	—	-1.5	—	-1.5	ns
T_{DDis}	Data Disable[3]		—	-1	—	-1	—	-0.5	—	-0.5	ns
T_{DVal}	Data Valid	Load = 25pF	—	3	—	3	—	3	—	2	ns
T_{WrDly}	Write Delay	Load = 25pF	—	5	—	4	—	3	—	2	ns
T_{DS}	Data Set-up		9	—	8	—	6	—	4.5	—	ns
T_{DH}	Data Hold[3]		-2.5	—	-2.5	—	-2.5	—	-2.5	—	ns
T_{CBS}	CpBusy Set-up		13	—	11	—	9	—	7	—	ns
T_{CBH}	CpBusy Hold		-2.5	—	-2.5	—	-2.5	—	-2.5	—	ns
T_{AcTy}	Access Type (1:0)	Load = 25pF	—	7	—	6	—	5	—	3.5	ns
T_{AT2}	Access Type (2)	Load = 25pF	—	17	—	14	—	12	—	8.5	ns
T_{MWr}	Memory Write	Load = 25pF	—	27	—	23	—	18	—	9.5	ns
T_{Exc}	Exception	Load = 25pF	—	7	—	7	—	5	—	3.5	ns
T_{Aval}	Address Valid	Load = 25pF	—	1.5	—	1.5	—	1.5	—	1	ns
T_{IntS}	$\overline{Int(n)}$ Set-up		9	—	8	—	6	—	4.5	—	ns
T_{IntH}	$\overline{Int(n)}$ Hold		-2.5	—	-2.5	—	-2.5	—	-2.5	—	ns
Stall Operation											
T_{SAVal}	Address Valid	Load = 25pF	—	30	—	23	—	20	—	15	ns
T_{SAcTy}	Address Type	Load = 25pF	—	27	—	23	—	18	—	13.5	ns
T_{MRdi}	Memory Read Initiate	Load = 25pF	—	27	—	23	—	18	—	13.5	ns
T_{MRdt}	Memory Read Terminate	Load = 25pF	—	27	—	23	—	18	—	10	ns
T_{Stl}	Run Terminate	Load = 25pF	3	17	3	15	3	10	2	7.5	ns
T_{Run}	Run Initiate	Load = 25pF	—	7	—	6	—	4	—	3	ns
T_{SMWr}	Memory Write	Load = 25pF	3	27	3	23	3	18	2	9.5	ns
T_{SExc}	Exception Valid	Load = 25pF	—	15	—	13	—	10	—	7.5	ns
Reset Initialization											
T_{RST}	Reset Pulse Width		6	—	6	—	6	—	6	—	Tcyc
T_{rstPLL}	Reset timing, Phase-lock on[4, 5]		3000	—	3000	—	3000	—	3000	—	Tcyc
T_{rstcp}	Reset timing, Phase-lock off[4, 5]		128	—	128	—	128	—	128	—	Tcyc
Capacitive Load Deration											
CLD	Load Derate[6]		0.5	2	0.5	1	0.5	1	0.5	1	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters apply when the 79R3010 Floating Point Coprocessor is connected to the CPU. With phase lock on, $\overline{Reset}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. With the exception of the $\overline{Run}$ signal, no two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 2.5ns for 33.33 MHz; clock transition time < 5ns for other speeds.

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3000A[1, 2, 3] — MILITARY TEMPERATURE RANGE (T_C = −55°C to +125°C, V_{CC} = +5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67MHz MIN.	16.67MHz MAX.	20.0MHz MIN.	20.0MHz MAX.	25.0MHz MIN.	25.0MHz MAX.	UNIT
Clock									
T_{CkHigh}	Input Clock High[2]	Note 7	12.5	—	10	—	8	—	ns
T_{CkLow}	Input Clock Low[2]	Note 7	12.5	—	10	—	8	—	ns
T_{CkP}	Input Clock Period[2]		30	500	25	500	20	500	ns
	Clk2xSys to Clk2xSmp[6]		0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd[6]		0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi[6]		9	tcyc/4	7	tcyc/4	5	tcyc/4	ns
Run Operation									
T_{DEn}	Data Enable[3]		—	−2	—	−2	—	−1.5	ns
T_{DDis}	Data Disable[3]		—	−1	—	−1	—	−0.5	ns
T_{DVal}	Data Valid	Load = 25pF	—	3	—	3	—	3	ns
T_{WrDly}	Write Delay	Load = 25pF	—	5	—	4	—	3	ns
T_{DS}	Data Set-up		9	—	8	—	7	—	ns
T_{DH}	Data Hold[3]		−2.5	—	−2.5	—	−2.5	—	ns
T_{CBS}	CpBusy Set-up		13	—	11	—	9	—	ns
T_{CBH}	CpBusy Hold		−2.5	—	−2.5	—	−2.5	—	ns
T_{AcTy}	Access Type (1:0)	Load = 25pF	—	7	—	6	—	5	ns
T_{AT2}	Access Type (2)	Load = 25pF	—	17	—	14	—	12	ns
T_{MWr}	Memory Write	Load = 25pF	—	27	—	23	—	18	ns
T_{Exc}	Exception	Load = 25pF	—	7	—	7	—	5	ns
T_{Aval}	Address Valid	Load = 25pF	—	2	—	2	—	2	ns
T_{IntS}	$\overline{Int(n)}$ Set-up		9	—	8	—	7	—	ns
T_{IntH}	$\overline{Int(n)}$ Hold		−2.5	—	−2.5	—	−2.5	—	ns
Stall Operation									
T_{SAVal}	Address Valid	Load = 25pF	—	30	—	23	—	20	ns
T_{SAcTy}	Address Type	Load = 25pF	—	27	—	23	—	18	ns
T_{MRdi}	Memory Read Initiate	Load = 25pF	1	27	1	23	1	18	ns
T_{MRdt}	Memory Read Terminate	Load = 25pF	—	27	—	23	—	18	ns
T_{Stl}	Run Terminate	Load = 25pF	3	17	3	15	3	10	ns
T_{Run}	Run Initiate	Load = 25pF	—	7	—	6	—	4	ns
T_{SMWr}	Memory Write	Load = 25pF	3	27	3	23	3	18	ns
T_{SExc}	Exception Valid	Load = 25pF	—	15	—	13	—	7.5	ns
Reset Initialization									
T_{RST}	Reset Pulse Width		6	—	6	—	6	—	Tcyc
T_{rstPLL}	Reset timing, Phase-lock on[4, 5]		3000	—	3000	—	3000	—	Tcyc
T_{rstcp}	Reset timing, Phase-lock off[4, 5]		128	—	128	—	128	—	Tcyc
Capacitive Load Deration									
CLD	Load Derate[6]		0.5	2	0.5	1	0.5	1	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters apply when the 79R3010 Floating Point Coprocessor is connected to the CPU. With phase lock on, $\overline{Reset}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. With the exception of the $\overline{Run}$ signal, no two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 2.5ns for 33.33 MHz; clock transition time < 5ns for other speeds.

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3000AE[1, 2, 3] — MILITARY TEMPERATURE RANGE (T_C = −55°C to +125°C, V_{CC} = +5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67MHz MIN.	16.67MHz MAX.	20.0MHz MIN.	20.0MHz MAX.	25.0MHz MIN.	25.0MHz MAX.	UNIT
Clock									
T_{CkHigh}	Input Clock High[2]	Note 7	12.5	—	10	—	8	—	ns
T_{CkLow}	Input Clock Low[2]	Note 7	12.5	—	10	—	8	—	ns
T_{CkP}	Input Clock Period[2]		30	500	25	500	20	500	ns
	Clk2xSys to Clk2xSmp[6]		0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd[6]		0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi[6]		9	tcyc/4	7	tcyc/4	5	tcyc/4	ns
Run Operation									
T_{DEn}	Data Enable[3]		—	−2	—	−2	—	−1.5	ns
T_{DDis}	Data Disable[3]		—	−1	—	−1	—	−0.5	ns
T_{DVal}	Data Valid	Load = 25pF	—	3	—	3	—	3	ns
T_{WrDly}	Write Delay	Load = 25pF	—	5	—	4	—	3	ns
T_{DS}	Data Set–up		9	—	8	—	7	—	ns
T_{DH}	Data Hold[3]		−2.5	—	−2.5	—	−2.5	—	ns
T_{CBS}	CpBusy Set–up		13	—	11	—	9	—	ns
T_{CBH}	CpBusy Hold		−2.5	—	−2.5	—	−2.5	—	ns
T_{AcTy}	Access Type (1:0)	Load = 25pF	—	7	—	6	—	5	ns
T_{AT2}	Access Type (2)	Load = 25pF	—	17	—	14	—	12	ns
T_{MWr}	Memory Write	Load = 25pF	—	27	—	23	—	18	ns
T_{Exc}	Exception	Load = 25pF	—	7	—	7	—	5	ns
T_{AVal}	Address Valid	Load = 25pF	—	2	—	2	—	2	ns
T_{IntS}	$\overline{Int(n)}$ Set–up		9	—	8	—	7	—	ns
T_{IntH}	$\overline{Int(n)}$ Hold		−2.5	—	−2.5	—	−2.5	—	ns
Stall Operation									
T_{SAVal}	Address Valid	Load = 25pF	—	30	—	23	—	20	ns
T_{SAcTy}	Address Type	Load = 25pF	—	27	—	23	—	18	ns
T_{MRdi}	Memory Read Initiate	Load = 25pF	—	27	—	23	—	18	ns
T_{MRdt}	Memory Read Terminate	Load = 25pF	—	27	—	23	—	18	ns
T_{Stl}	Run Terminate	Load = 25pF	3	17	3	15	3	10	ns
T_{Run}	Run Initiate	Load = 25pF	—	7	—	6	—	4	ns
T_{SMWr}	Memory Write	Load = 25pF	3	27	3	23	3	18	ns
T_{SExc}	Exception Valid	Load = 25pF	—	15	—	13	—	10	ns
Reset Initialization									
T_{RST}	Reset Pulse Width		6	—	6	—	6	—	Tcyc
T_{rstPLL}	Reset timing, Phase–lock on[4, 5]		3000	—	3000	—	3000	—	Tcyc
T_{rstcp}	Reset timing, Phase–lock off[4, 5]		128	—	128	—	128	—	Tcyc
Capacitive Load Deration									
CLD	Load Derate[6]		0.5	2	0.5	1	0.5	1	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters apply when the 79R3010 Floating Point Coprocessor is connected to the CPU. With phase lock on, $\overline{Reset}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. With the exception of the $\overline{Run}$ signal, no two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 2.5ns for 33.33 MHz; clock transition time < 5ns for other speeds.

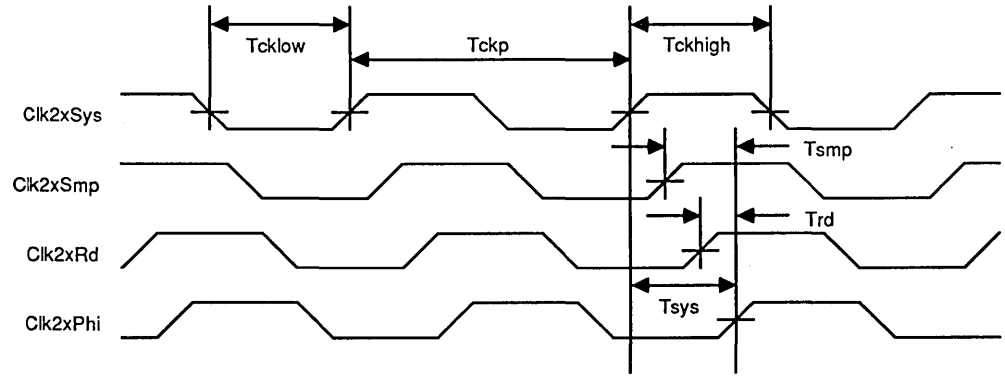
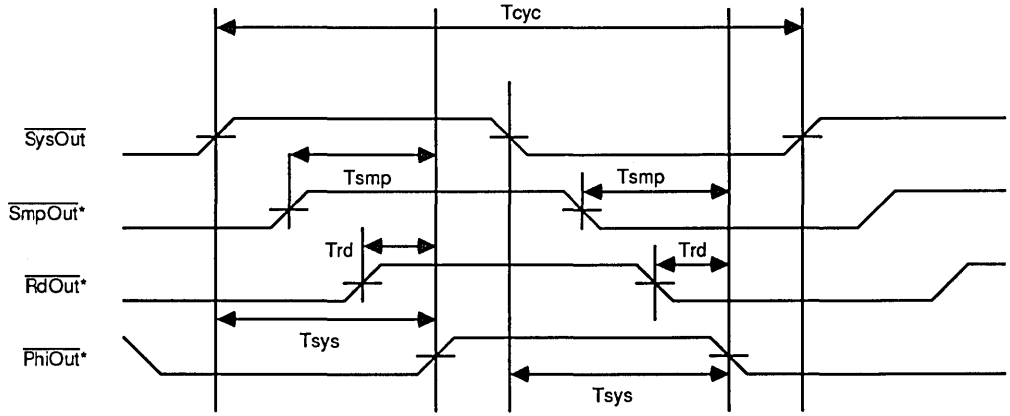


Figure 12. Input Clock Timing



* These signals are not actually output from the processor. They are drawn to provide a reference for other timing diagrams.

Figure 13. Processor Reference Clock Timing

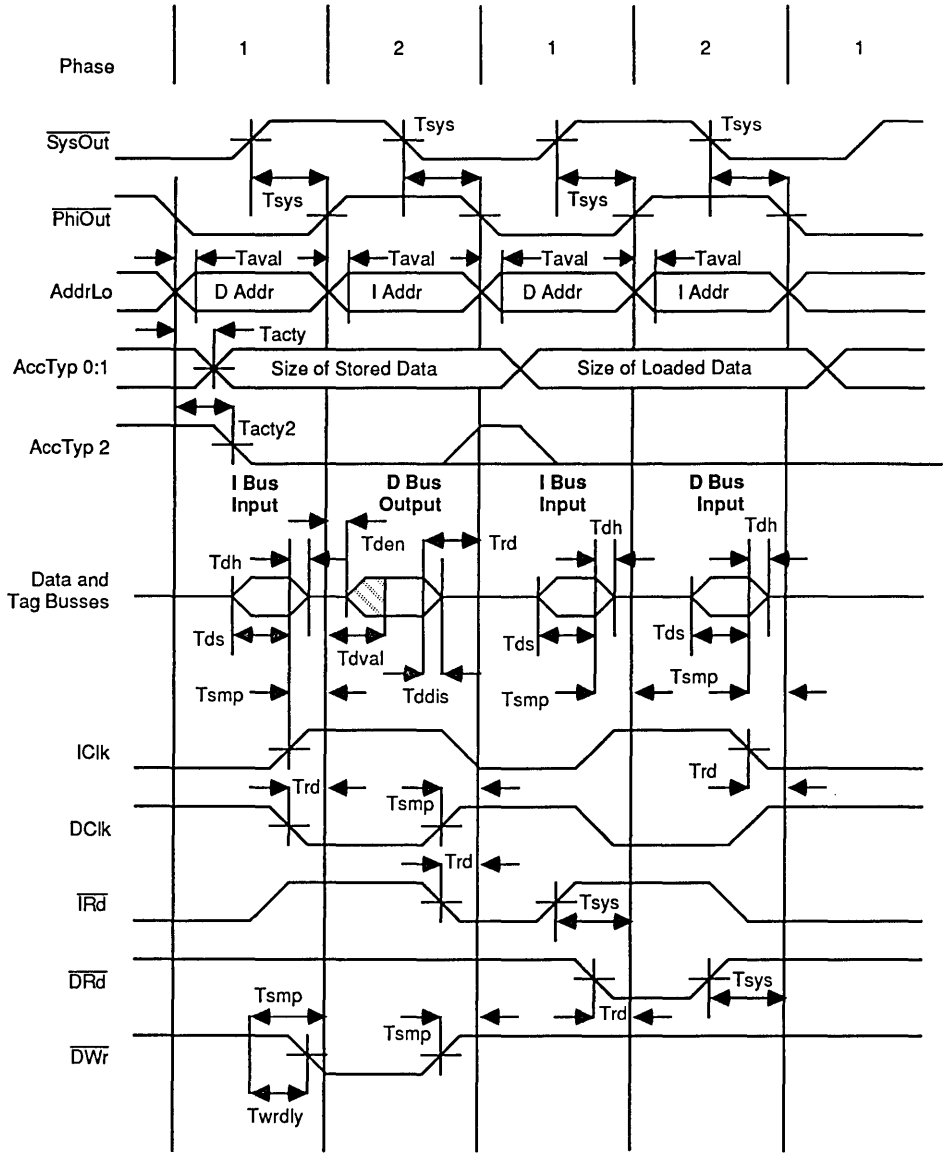


Figure 14. Synchronous Memory (Cache) Timing

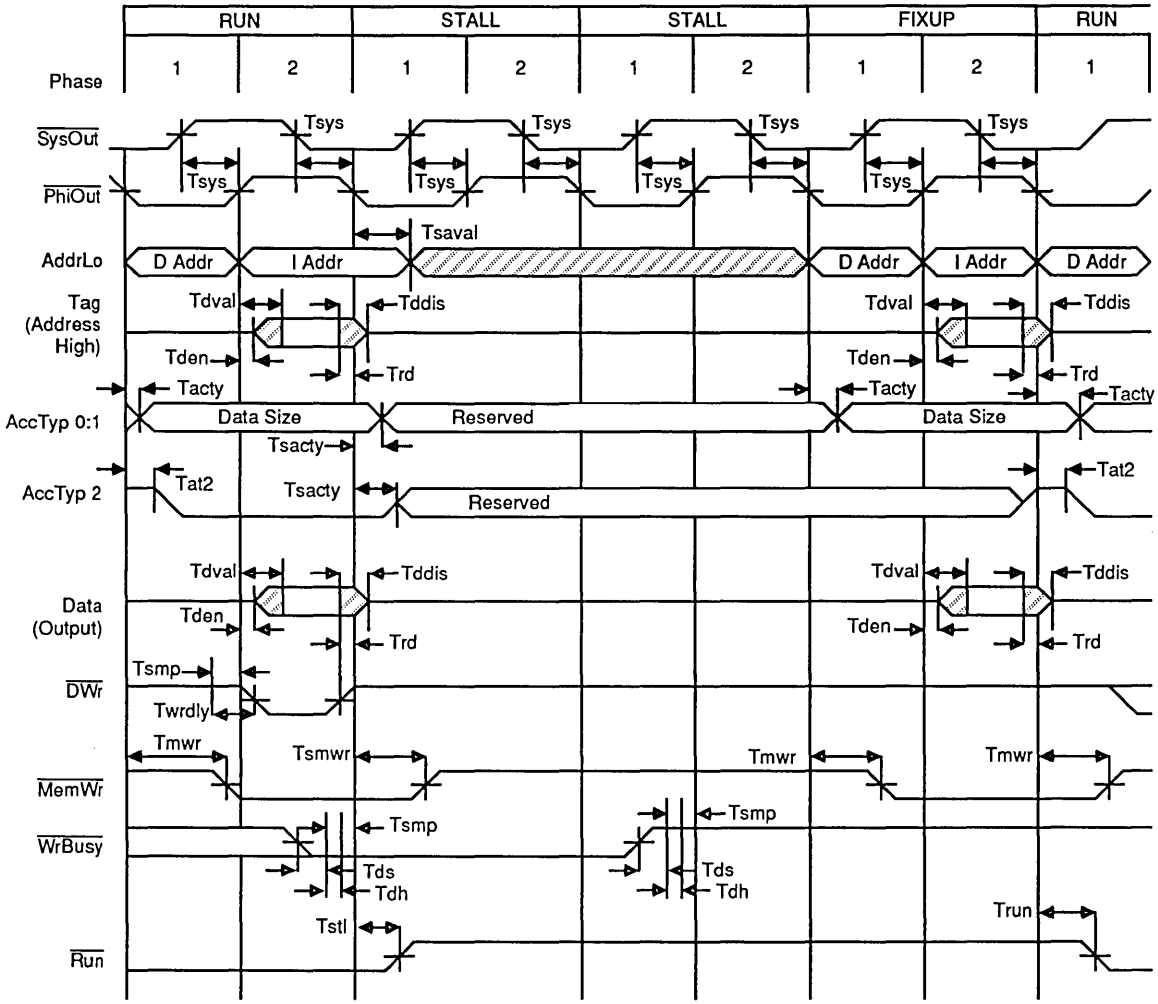


Figure 15. Memory Write Timing

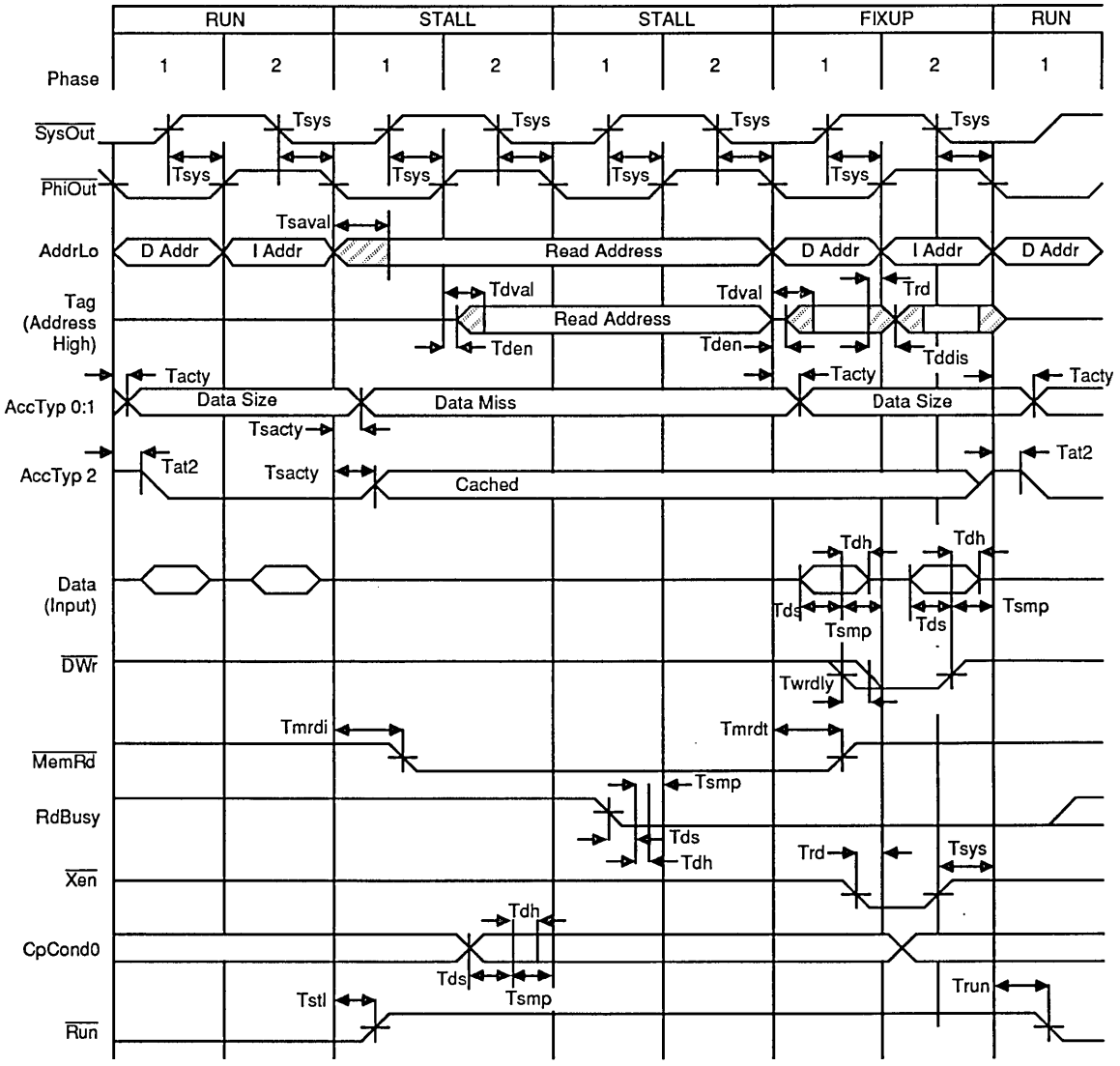


Figure 16. Memory Read Timing

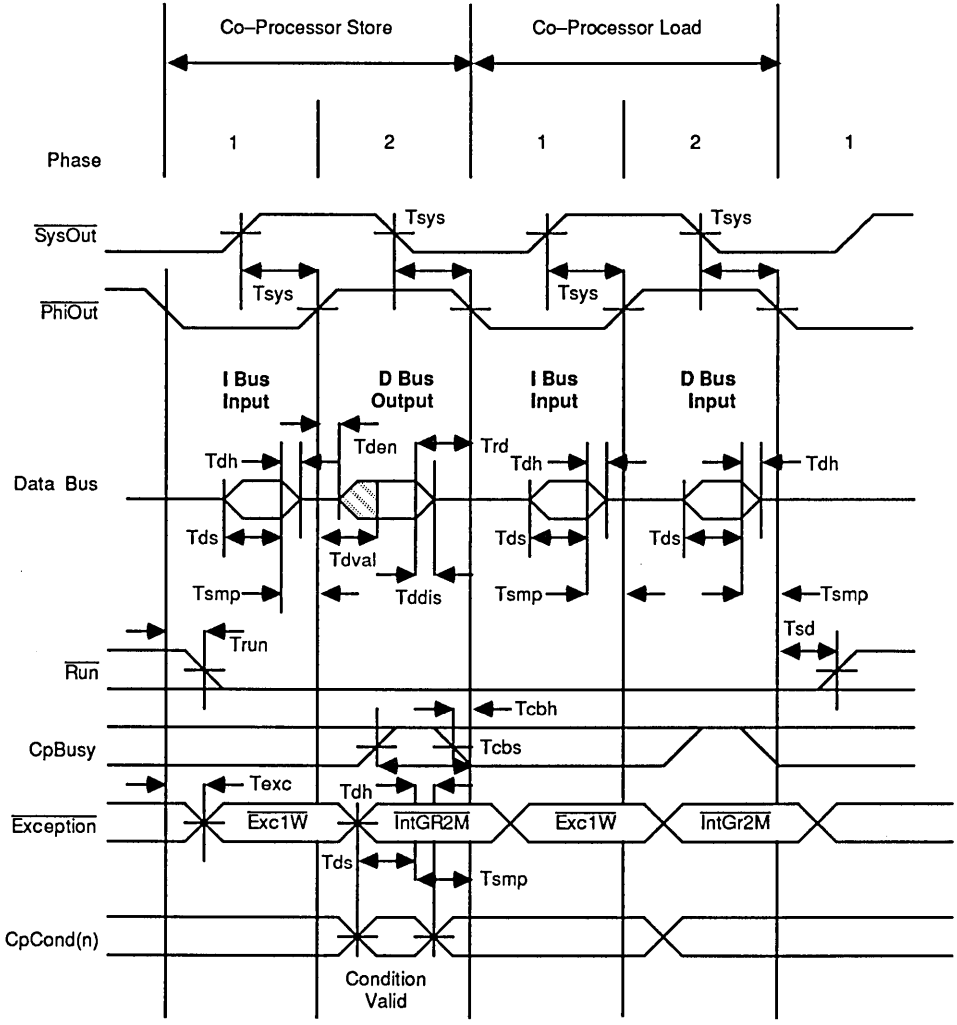


Figure 17. Co–Processor Load/Store Timing

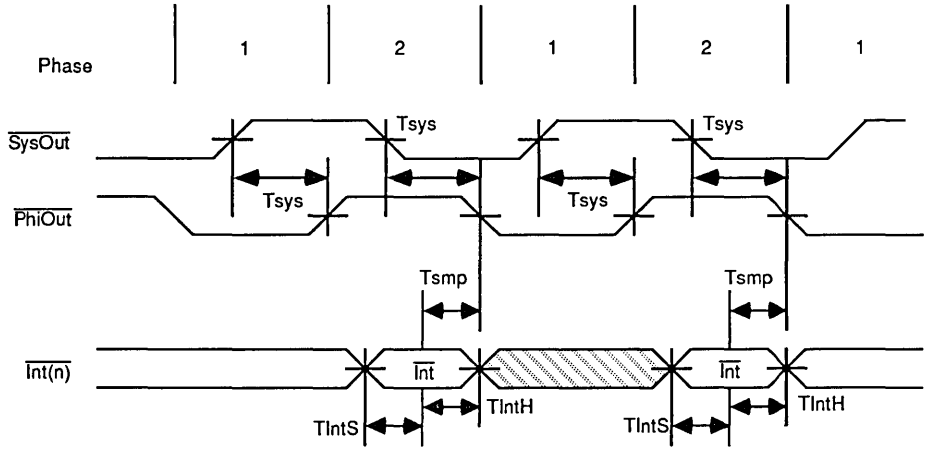
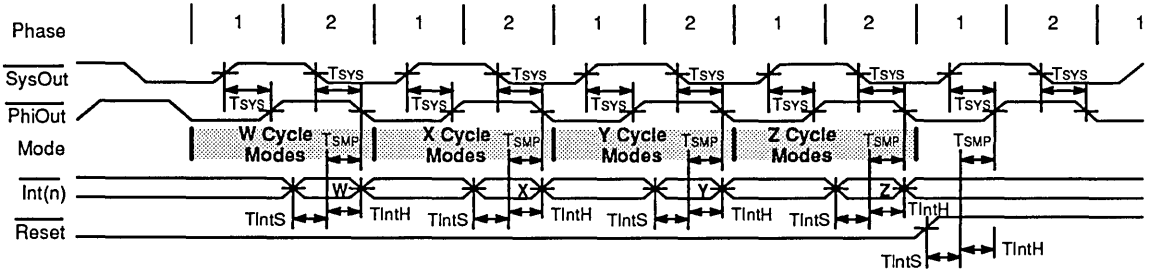


Figure 18. Interrupt Timing

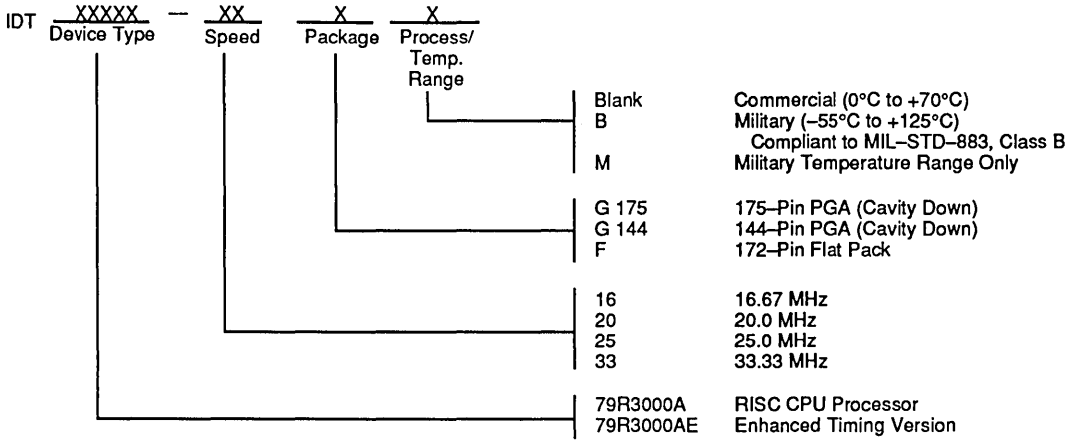


NOTES:

1. Reset must be negated synchronously; however, it can be asserted asynchronously. Designs should not rely on the proper functioning of SysOut prior to the assertion of Reset.
2. If Phase-Lock On or R3000 Mode are asserted as mode select options, they should be asserted throughout the Reset period, to insure that the slowest co-processor in the system has sufficient time to lock the CPU clocks.
3. Reset is actually sampled in both Phase 1 and Phase 2. To insure proper initialization, it is recommended that Reset be negated relative to the end of Phase 1.

Figure 19. Mode Vector Initialization

ORDERING INFORMATION



Integrated Device Technology, Inc.

RISController™

PRELIMINARY
IDT79R3001

FEATURES:

- Enhanced Instruction Set compatible version of IDT79R3000 RISC CPU
- Achieves high–performance with reduced parts count and lower overall system cost
- Flexible on–chip cache controller supports various cache, main memory sizes
- Supports optional data parity with parity error output signal
- Works with IDT79R3010 RISC Floating–Point Coprocessor
- DMA interface support
- Large synchronous memory space for real–time systems
- Full 32–bit operations — 32–bit registers, 32–bit address and data interface
- On–chip memory management unit with 64 fully associative TLB entries maps 4 Gbyte virtual address space
- High–speed interrupt response (6 interrupt input pins) with precise exception capability
- High–speed CEMOS™ technology results in speeds from 12.5 to 25MHz
- Supports caches from 8 Kbytes to 16Mbytes
- Independent block refill sizes for the instruction and data caches
- Concurrent cache refill and execution
- Works on 8–, 16– and 32–bit data
- Supports unaligned 32–bit data
- Optimizing compilers for C, Ada, Pascal, Fortran
- RTOS support for C or Ada environments

DESCRIPTION:

The IDT79R3001 brings the high–performance inherent in the IDT79R3000 RISC Microprocessor to lower cost systems. It does this while maintaining full (both User and Kernel) software compatibility with both the IDT79R2000A and IDT79R3000 RISC Microprocessors.

The IDT79R3001 achieves lower system cost by reducing the number of components required to construct a synchronous memory (or cache) external to the processor and by simplifying the asynchronous memory interface. By removing the requirement for parity and allowing the system designer to select the cache organization which best suits the system, overall parts count is dramatically reduced while maintaining high performance.

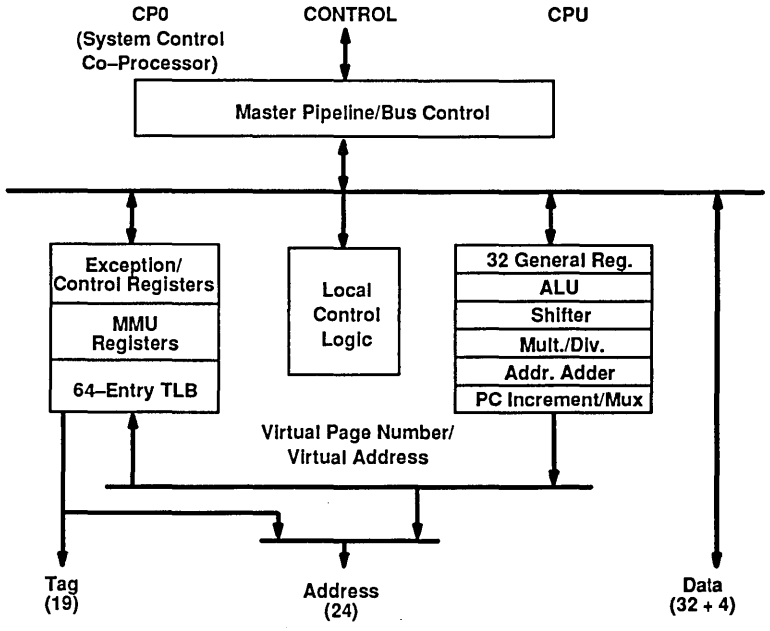


Figure 1. IDT79R3001 Block Diagram

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The IDT79R3001 RISC Microprocessor extends the ability of the IDT79R3000 family to support embedded and cost sensitive applications. Its level of integration and flexibility allows high–performance systems to be constructed at reasonable cost in a straightforward manner, without forcing the system designer to support features not required in his application.

The IDT79R3001 consists of two tightly coupled processors integrated on a single chip. The first processor is a full 32–bit CPU based on RISC principles to achieve a new standard of performance in microprocessor based systems. The second processor is a system control co–processor, called CP0, containing a fully associative 64–entry TLB (Translation Lookaside Buffer), MMU (Memory Management Unit), and control registers, supporting a 4 Gigabyte virtual memory subsystem and a Harvard Architecture Synchronous Memory/Cache controller which achieves ultra–high bandwidth using industry standard SRAM devices.

This data sheet provides an overview of the features and architecture of the IDT79R3001 CPU. A more detailed description of the operation and timing of this device is incorporated in the "IDT79R3001 Hardware User's Guide", and a detailed architectural overview is provided in the "mips RISC Architecture" book, both available from IDT. Further literature describing the hardware, software, and development tools for the IDT79R3001 are also available from IDT.

HARDWARE OVERVIEW

The IDT79R3001 is a high–performance RISC microprocessor incorporating a fast execution engine and sophisticated yet flexible memory interface designed to support the processor bandwidth requirements at minimal system cost.

Execution Engine

The IDT79R3001 contains the same basic execution engine as the ultra–high performance IDT79R3000 and thus achieves over 20 MIPS performance at 25 MHz.

The key to the performance of the processor is the instruction pipeline, illustrated in Figure 2. The execution of a single IDT79R3001 instruction consists of five primary steps, some of which may be broken down further into smaller subsets.

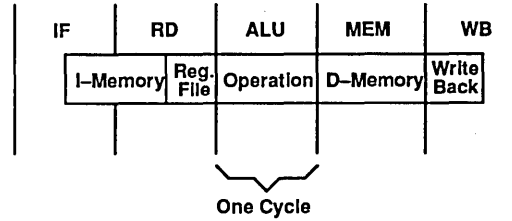


Figure 2. IDT79R3001 Five–Stage Pipeline

The five primary stages of the pipeline, each of which require approximately one CPU cycle, are:

IF	Instruction Fetch, when the processor fetches the instruction from the Instruction Synchronous Memory
RD	Read required operands from on–chip register file while decoding the instruction.
ALU	Perform the required operation on instruction operands.
MEM	Access data memory (load or store)
WB	Write results back to register file.

Thus, the CPU achieves an average execution rate approaching one instruction per CPU cycle, since the execution of five instructions at a time are overlapped within the processor (Figure 3). Optimizing compiler technology fully comprehends the interaction of software with the various pipeline resources, and serves to both eliminate any potential pipeline conflicts which might arise and to maximize instruction throughput.

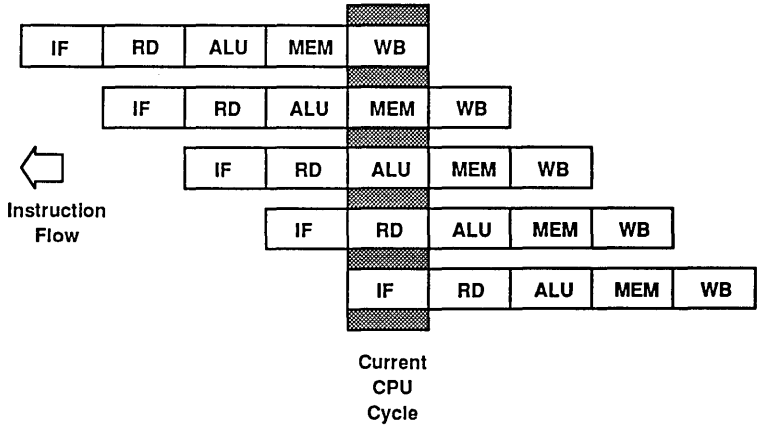


Figure 3. Instruction Execution in IDT79R3001 Pipeline

The IDT79R3001 Memory Interfaces

The key to achieving the inherent performance of the IDT79R3001 is to design a memory subsystem capable of providing a new instruction to the processor on almost every clock cycle.

Like the IDT79R3000, the IDT79R3001 supports a hierarchical view of the memory subsystem. However, the IDT79R3001 allows the system designer to make more trade–offs in the partitioning and architecture of the various levels in order to more completely meet the needs of certain types of applications.

The IDT79R3001 supports two classifications of external memory: synchronous and asynchronous. The Harvard–Architecture (separate instruction and data memories) synchronous memory allows the processor to achieve the highest levels of performance. The processor is able to obtain both an instruction and data word from the synchronous memory on every clock cycle, resulting in high instruction and data throughput.

The asynchronous memory space contains larger, slower memory devices such as EPROM, main memory DRAMs, and peripheral devices. Multiple clock cycles are required for data movement in the asynchronous memory.

Many systems implement a memory hierarchy between these two memory spaces, whereby the synchronous memory space is used as processor caches and the asynchronous memory space is used for main memory. The IDT79R3001 integrates a flexible Direct–Mapped Cache Controller On–Chip, eliminating external cache control logic and minimizing cache management overhead. If the synchronous memory space is used for processor caches, then cache "misses" will cause the processor to automatically process an asynchronous memory transfer to refill the cache.

The key to achieving the system cost and performance goals of an IDT79R3001–based system is to partition the memory system to the needs of the application.

Synchronous Memory System

As with any high–performance processor, the IDT79R3001 requires high–bandwidth to achieve high–performance. Thus, it is important that the majority of its execution occur in the synchronous memory space. In applications which require substantial amounts of main memory, this memory space will be implemented as instruction and data caches.

The synchronous memory is designed to be able to supply both an instruction and data word to the processor on each clock cycle. When the synchronous memory spaces are used as caches, then they are used to hold instruction and data that is repetitively accessed by the CPU (for example, within a program loop). This reduces the number of slower asynchronous memory cycles and thus achieves higher performance.

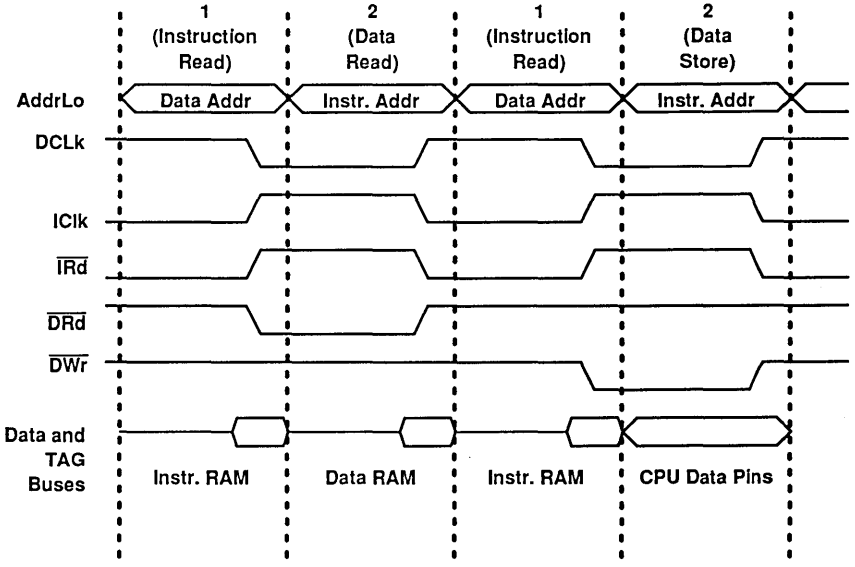


Figure 4. Synchronous Memory Control Timing

Some microprocessors incorporate small amounts of cache on–chip, which has a very small and unpredictable effect on the execution of large programs. The IDT79R3001 supports caches of from 8kB in size up through 16MB, thus bringing substantial performance improvements to very large programs and also allowing real–time system designers to design cache–based systems to support deterministic requirements.

The IDT79R3001 directly controls the synchronous memory interface (whether it is being used as caches or not) with a minimum of external components. The IDT79R3001 includes all control signals and cache TAG control logic (for a direct mapped cache) for the synchronous memory interfaces. Parity over the data portion of each synchronous memory can be optionally selected at RESET time for applications which desire to make this cost trade–off.

The synchronous interface works by dividing the basic CPU cycles into two phases. During one phase, a cache address is presented by the processor and captured by external latches (the latch control signals are directly generated by the CPU). During the next phase, the address for the other memory space is generated and captured while the data movement operation for the first cache is completed. The processor directly generates the SRAM Output Enable and Write Enable signals and the address latch enable signals, requiring no external decoding. This is illustrated in Figure 4.

Further, the IDT79R3001 supports the ability to refill multiple words into the cache from main memory when a cache–miss occurs, further reducing system cost and increasing performance in cache–based systems. The IDT79R3001 can obtain 1, 4, 8, 16, or 32 words from main memory when processing a cache–miss, thus amortizing the cache–miss penalty over a large amount of data.

The IDT79R3001 also performs instruction streaming, which is the simultaneous execution of incoming instructions while the cache is being refilled.

The actual width of the tag bus, and whether or not parity over the data parts of each synchronous memory, is determined according to how the device is initialized. The IDT79R3001 can accommodate a TAG bus width of 0–19 bits, compatible with a variety of cache sizes and cacheable main memory choices. The IDT79R3001 allows the system designer to scale the synchronous memory system exactly according to the system needs, thus eliminating extra memory and logic devices and achieving substantial cost savings with no loss of performance.

Thus, the synchronous memory interface of the IDT79R3001 allows for high–bandwidth memory systems to be implemented with a minimum of control logic. This is desirable, since RISC performance tends to be a function of memory bandwidth. By simplifying the design of the synchronous memory system (illustrated in Figure 5), it is easier for the system designer to achieve high performance with minimum chip count and without requiring ultra–fast or specialty components.

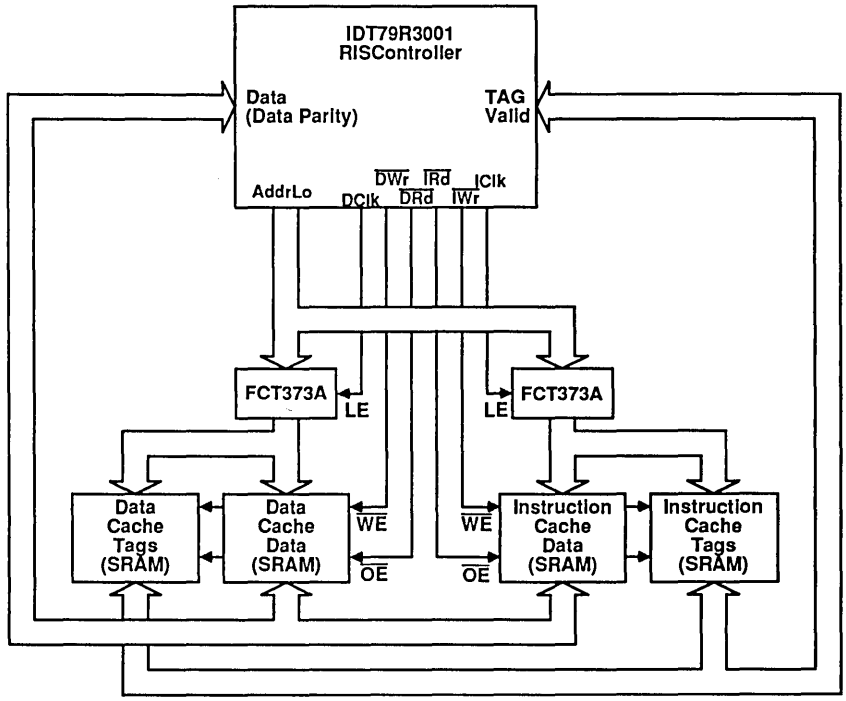


Figure 5. IDT79R3001 Synchronous Interface

The TAG Bus

The TAG bus of the IDT79R3001 has been designed to allow the system designer to implement the exact cache configuration that is right for the system. For larger caches, low–order TAG bits do not need to be supplied for the TAG comparison. Additionally, the number of high–order TAG bits supplied is determined by the system designer, according to the amount of cacheable main memory the system supports. Since most embedded systems would tend to implement caches of 16KB and greater, and cacheable memory spaces of 32MB or smaller, significant cost and area reductions are achieved by configuring a smaller TAG bus.

The system configures the on–chip TAG comparator at RESET Initialization time. If a TAG bit is not to be included in the synchronous memory TAG bit compare, a pull–down resistor of 4kΩ is connected to the appropriate IDT79R3001 TAG pin. If a TAG bit is to be included, no resistor is required (the IDT79R3001 pulls floating inputs to V_{cc} during RESET by a small pull–up, which is disabled when RESET is negated).

If a TAG bit is excluded from the cycle–by–cycle comparison, it is still driven out with the appropriate address value during write cycles or asynchronous memory reads. Thus, the system designer still has the full 4 Gbyte of address space available for address decoding, without requiring the synchronous memory to be able to cache all such addresses.

Figure 6 illustrates a reduced system, which implements 16KB of Instruction and 16KB of data cache, and 512MB of cacheable address space, using just 6 IDT71586 4Kx16 Latched CacheRAM™ components and 4 pull–down resistors.

Note that in systems which do not implement the synchronous memory space as cache, then pull–down resistors would be added to all TAG pins. The Valid Pin still needs to be supplied on each cycle, thus allowing various memory schemes to be implemented (such as static column DRAM). However, the IDT79R3001 can be initialized to not assert the Valid pin as an output during Write cycles, simplifying the design of logic to drive the signal.

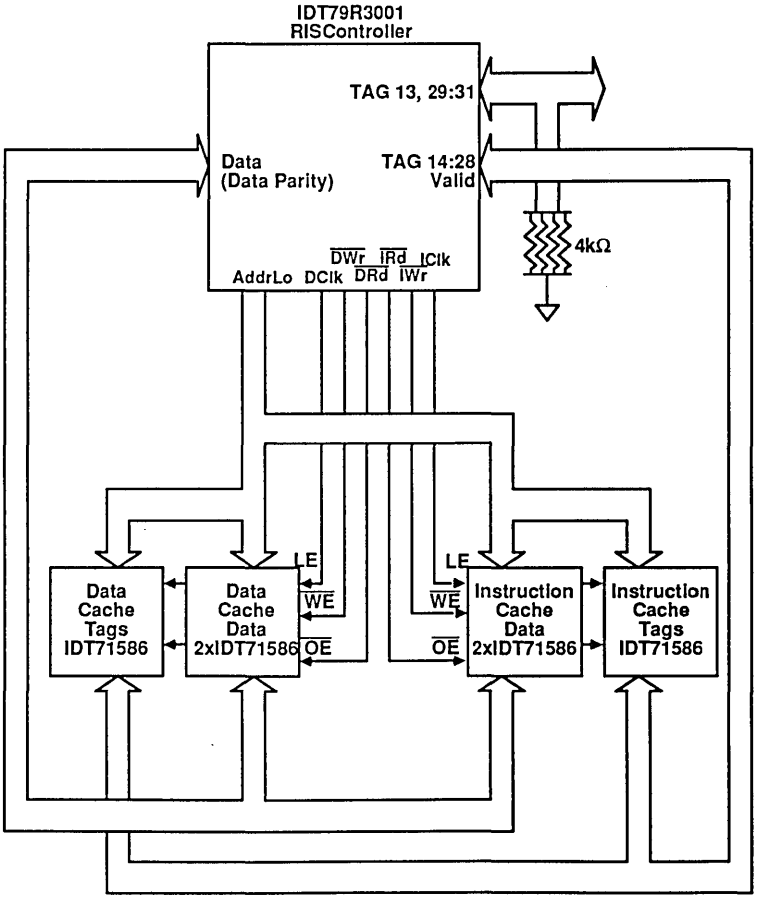


Figure 6. Small Footprint Cache for IDT79R3001

Cache Update

When the on–chip TAG comparator indicates that the item read from the cache was not the desired item, a cache–miss is processed. A main memory (asynchronous) transfer is automatically processed.

The IDT79R3001 desires to update the cache using a burst refill of multiple adjacent words from main memory. The processor is "stalled" until the first word of the block is available. The processor is then released, and the block of words is brought into the cache at the rate of one word per CPU clock cycle.

Note that if the cache–miss was in the instruction cache, the processor is capable of simultaneously executing the incoming instruction stream as the cache is updated, thus effectively making the cache update transparent to the system and increasing performance.

Write Cycles

The IDT79R3001 utilizes a write through cache. That is, data written by the processor is both written to the cache and main memory simultaneously. Thus, main memory always has a current copy of all data.

Typically, latching devices are used between the cache subsystem and the slower main memory. These Write Buffers capture the data simultaneous with the cache update, allowing the processor to continue to the next cycle without actually waiting for the main memory transfer to complete. The IDT79R3001 generates parity over the data field on write cycles, which can be propagated into both the synchronous and asynchronous memory spaces.

When the processor writes less than a 32–bit quantity (a "partial" word), the processor can perform a "read–modify–write" of the cache. That is, the processor will read the 32–bit word containing

the partial address(es) to be updated from the cache. If a "hit" occurs, then the new data will be merged with the old and the new 32–bit value will be written both to the cache and to main memory. If a cache "miss" occurs, then only the partial data is written to main memory and the cache is unchanged. Partial word capability is selected as a RESET option.

THE ASYNCHRONOUS MEMORY INTERFACE

The IDT79R3001 also supports an asynchronous memory interface, which supports the use of slower memory devices such as slow DRAM, EPROM and also supports the use of peripherals and other "non–cacheable" devices.

In general, if a cache–miss (or parity error, if enabled) occurs, the processor will automatically use the asynchronous memory interface to retrieve the desired data, and will update the cache accordingly.

Additionally, software can force the use of the asynchronous memory space through the use of the on–chip MMU. When the processor seeks either instructions or data within a certain address range (kseg1), the processor knows that this data is uncacheable and will perform an asynchronous memory transfer. Additionally, within cacheable memory, TLB entries can be used to mark certain pages as "uncacheable". When an address of an "uncacheable" page is used, the processor will automatically use the asynchronous memory space.

The asynchronous memory space uses the same data bus as the synchronous memory space. This facilitates the automatic updating of cache memory when the asynchronous memory is accessed due to cache–miss activity or memory writes. The asynchronous address bus is composed from the synchronous memory AddrLo bus, and the TAG bus. External logic devices (such as IDT74FCT374A registers) are used to capture AddrLo and TAG values for the asynchronous transfer address. Note that systems which exclude invididual TAG bits from comparison (to reduce cache width) still have all TAGs available as outputs.

The data path between the processor and the asynchronous memory space is managed according to the needs of the application. Write Buffer FIFO devices, such as the IDT79R3020, are used to capture address and data during store cycles. These devices are used to capture the data in one cycle, and allow the processor to continue to execute from the synchronous memory while the slower asynchronous memory actual retires the write.

The read path is also constructed according to the needs of the system. If block refill is used, then the read path is highly dependent on the design of the main memory system. Pipeline devices such as IDT74FCT520A, or simple latches such as IDT74FCT374, may be used.

A simple asynchronous memory interface is shown in Figure 7. In this system, main memory is assumed to be fast enough to support the block refill requirements of the system, thus simplifying the read path. In fact, both the read and write data paths are actually managed through a single set of IDT29FCT52A bidirectional latching transceivers.

During write cycles (which are typically captured by Write Buffers), the processor asserts $\overline{\text{MemWr}}$ to indicate that a write cycle is in progress. The memory system negates WrBusy to indicate that the processor is done with the write cycle.

During read cycles, the processor will assert $\overline{\text{MemRd}}$ to indicate that a main memory read is in progress. The memory system will hold RdBusy active until the desired data is available. The processor will activate the $\overline{\text{XEn}}$ signal to allow data to be passed from the main memory to the processor data bus. If the cache is to be updated with the new data, then the processor will assert the appropriate cache write signal to allow the cache RAMs to capture the incoming data bus.

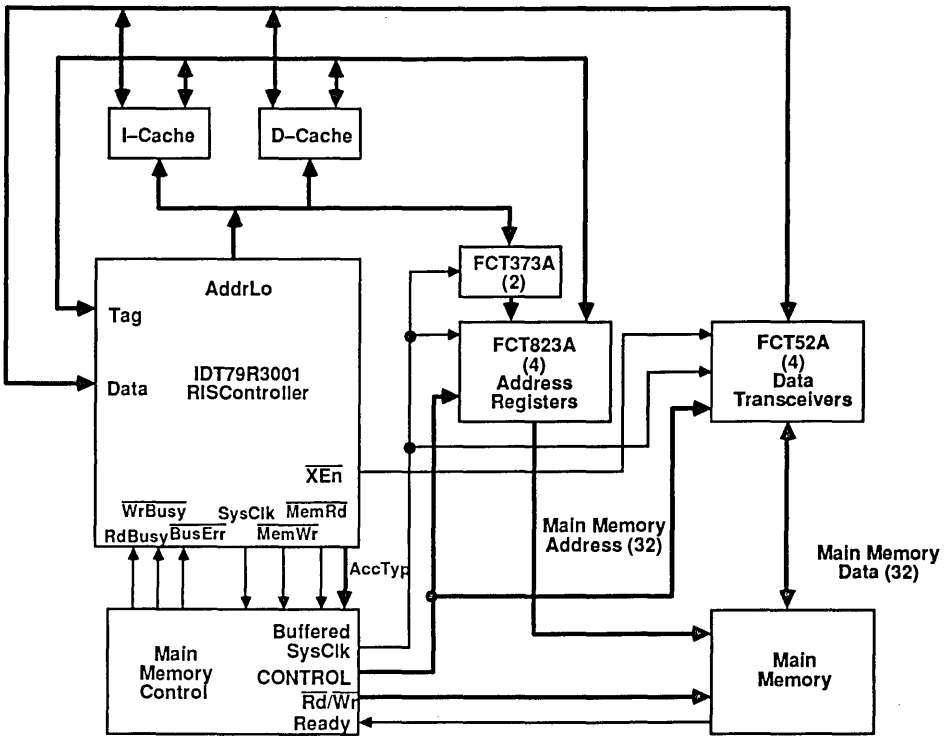


Figure 7. IDT79R3001 Asynchronous Interface

The AccTyp bus is used to indicate the size of the data transfer (8, 16, 24, or 32 bits), and for main memory reads, whether or not the data is "cacheable". This simplifies the main memory address decoding, since the AccTyp indicates whether the main memory needs to perform a burst read of multiple words.

Co-Processor Interface

The IDT79R3001 implements a co-processor interface, which allows the use of the IDT79R3010 high-performance RISC Floating Point Accelerator without requiring the use of external interface components.

The co-processor interface has been designed to make system co-processors appear to the programmer as if they were on-chip extensions of the core execution engine. Thus, the IDT79R3010 FPA works as a true co-processor, rather than as a peripheral which must be programmed.

In the IDT79R3001 co-processor model, the CPU is responsible for controlling all data cycles. The co-processor keeps in synchronization with the CPU (including the pipeline stages), and uses a Phase-Locked Loop to keep synchronized with the processor bus traffic. The co-processor then "snoops" the data bus, watching for co-processor instructions. It also knows when data cycles on the bus are intended for it (either as a target in co-processor load operations, or as a source for co-processor store operations), and performs the data portion of the operation when appropriate. Thus, co-processors effectively load and store directly with memory, without requiring operands to go through the CPU first. This achieves the highest levels of performance (note that the co-processor interface also supports move, whereby data can be moved directly between the CPU and any co-processor).

Figure 8 illustrates the use of the IDT79R3010 in a IDT79R3001 system. The co-processor interface manages synchronization between the parts, and is used to communicate status from the co-processor to the CPU. CpBusy, or co-processor busy, stalls the CPU until the busy co-processor resource (requested by a co-processor instruction) is free, and CpCond, or co-processor condition, is used to report status on co-processor test instructions. CpSync, is used to help the co-processor stay "locked" to the CPU, so that the co-processor knows when data is on the bus to be sampled on load operations or when to place data on the bus for store operations.

Note that the co-processor sits on the same data bus as the CPU, but has no connection to the address bus. The CPU is responsible for performing all memory addressing, including the determination of "cache hit", write-buffer full cycles, and any processing that might be required for cache misses.

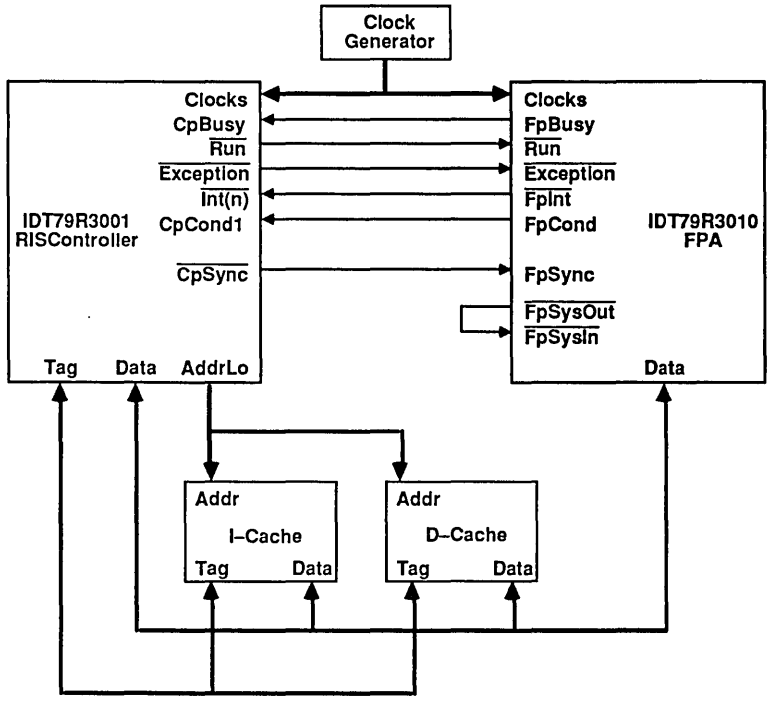


Figure 8. IDT79R3001 Interface to IDT79R3010 Floating Point Co-Processor

Interrupts

The IDT79R3001 features 6 separate interrupt input pins. Interrupts are not vectored, but rather cause the general exception vector address to be the next execution address.

These pins are not encoded internally; external logic can choose to implement these interrupt lines as either 6 or 64 interrupt sources; software would then perform the appropriate decoding to get to the specific interrupt handler.

Interrupts are recognized in the ALU stage of the on-chip pipeline. Instructions less advanced in the pipeline are "flushed" and will be restarted when the return from exception occurs (an on-chip register contains the address of the instruction which was excepted). Instructions further advanced in the pipeline are allowed to continue. Unlike other RISC processors, the IDT79R3001 does not require the programmer to save and restore pipeline status to allow normal execution to be resumed. Depending on the application and exception, at most software would need to save/restore the on-chip data registers, status register, Exception PC and exception "cause" register.

Note that the co-processor model includes "precise exceptions". That is, an exception is signaled to the exact instruction which generated the exceptional condition. No further state commitments are made by the IDT79R3001 and, thus, the exact context at the time of the exception is known to the programmer. This is true even for multi-cycle operations, such as those of the FPA.

DMA Interface

The IDT79R3001 features a simple DMA interface which allows an external master to gain control of the synchronous memory space. Note that it is not necessary to include logic on the CPU to arbitrate for the asynchronous memory space; the read/write buffer interface is where such arbitration logic belongs and it is left to the system designer to implement the type of asynchronous memory structure that best fits the application.

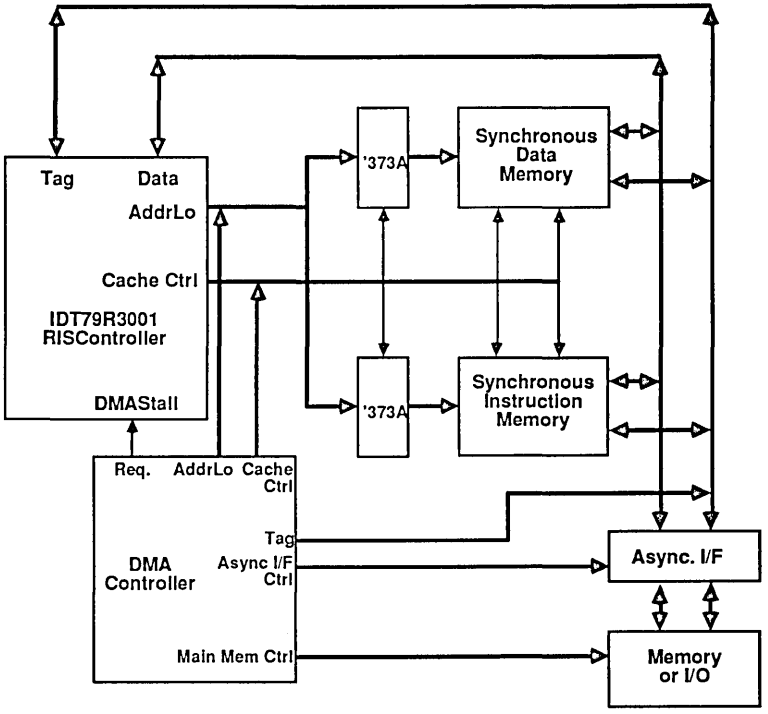


Figure 9. IDT79R3001 DMA Interface

When an external master "owns" the synchronous bus, the CPU will tri–state the following pins and buses:

AddrLo: The Synchronous memory direct address bus.

Data & Tag: The synchronous memory RAM data lines.

Cache Control: $\overline{IRd}$, $\overline{IWr}$, IClk, $\overline{DRd}$, $\overline{DWr}$ and DClk. This allows the external master to use the existing control lines to control the synchronous memory.

$\overline{XEn}$: The read buffer transceiver enable, which will allow the external master to use the read/write buffer path for DMA.

Valid: This enables the DMA interface to be used for multiprocessing applications.

The DMA interface consists of a single input signal, DMAStall, which causes the processor to stall and to tri–state the above named lines. The external master is guaranteed mastership of the bus within a very short number of cycles, depending on the exact external bus activity of the CPU when the DMA was requested. The DMA master negates the DMAStall signal when the DMA operation is completed to allow the CPU to resume processing. Consult the "IDT79R3001 Hardware User's Guide" for more details.

Figure 9 illustrates the system connection of an external DMA master to a IDT79R3001 system.

Advanced Features

The IDT79R3001 contains special features which provide added flexibility across a number of applications, as well as allow for system diagnostic support.

In support of diagnostics, the IDT79R3001 allows for cache "swapping" (interchange of which memory bank is for instruction and which is for data), which is useful in system initialization, cache flushing, and diagnostics. Additionally, the caches can be "isolated" from main memory, which forces cache "hits" to occur regardless of the tag comparison, and which is useful in determining that the synchronous memory space RAMs are functional.

An additional feature is the ability to enable parity checking over the data field of each synchronous memory. If parity is enabled, the processor will check the parity when a synchronous access occurs; if a parity error is detected, it is signaled to the external world on the $\overline{\text{Parity Error}}$ signal and a cache–miss cycle is processed. The $\overline{\text{Parity Error}}$ signal will remain low until the parity error flag in the CP0 status register is cleared by software.

A number of other system selectable features are selected at reset time. The input reset "vectors" are sampled on the interrupt input lines during the last four cycles of the reset period. The input vectors are listed in Table 1. These selections include the ability to select the block refill sizes for each of the instruction and data memories, whether Big Endian or Little Endian order is to be used, whether to use data parity, and whether or not to accommodate a Phase–Locked Loop for a co–processor. The initialization of the CPU and meaning of each input vector is more fully explained in the "IDT79R3001 Hardware User's Guide".

INPUT	W CYCLE	X CYCLE	Y CYCLE	Z CYCLE
$\overline{Int0}$	Reserved	Reserved	Reserved	Reserved
$\overline{Int1}$	Reserved	Reserved	Reserved	Reserved
$\overline{Int2}$	$\overline{DBlkSize0}$	$\overline{DBlkSize1}$	$\overline{Parity\ On}$	Valid Output
$\overline{Int3}$	$\overline{IBlkSize0}$	$\overline{IBlkSize1}$	StorePartial	ControlLow
$\overline{Int4}$	$\overline{PllOn}$	$\overline{PllOn}$	$\overline{PllOn}$	$\overline{PllOn}$
$\overline{Int5}$	Reserved	BigEndian	$\overline{TriState}$	Reserved

*Reserved signals must be "high" during these cycles.

Table 1. IDT79R3001 Mode Selectable Features

PROCESSOR ARCHITECTURE

The IDT79R3001 is a full implementation of the IDT79R2000A/ IDT79R3000 Instruction Set Architecture (the MIPS–I ISA). This architecture is discussed in great detail in "mips RISC Architecture", available from IDT.

IDT79R3001 CPU Registers

The IDT79R3001 CPU provides 32 general purpose (orthogonal) 32–bit registers, a 32–bit Program Counter and two 32–bit registers used to hold the results of the CPU integer multiply and divide operations.

Two of the 32 general registers have special purposes designed to increase processor performance: register r0 is hardwired to the value "0", a useful constant; and register r31 is used as the link register in jump–and–link instructions (the return address for subroutine calls). Otherwise, there is no requirement that a particular register be used as a stack or frame pointer, etc., although there is a register convention as part of the "mips ABI" (Applications Binary Interface standard) which the compiler suite uses.

The CPU registers are illustrated in Figure 10. Note that there is no Program Status Word register shown in this figure. The functions traditionally provided by a PSW register are instead provided in the Status and Cause Registers incorporated within the on–chip System Control Co–Processor (CP0). The instruction set does not use condition codes.

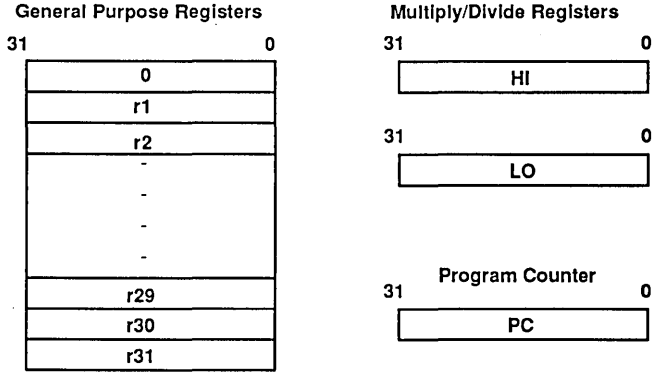


Figure 10. IDT79R3001 Registers

Instruction Set Overview

All IDT79R3001 instructions are 32 bits long and there are only three instruction formats (see Figure 11). This approach simplifies decoding, thus minimizing instruction execution time. The IDT79R3001 processor initiates a new instruction on every RUN cycle, and is able to complete an instruction on almost every clock cycle. The only exceptions are the LOAD instructions and BRANCH instructions, which each have a single cycle of latency associated with their execution (that is, the instruction immediately after the branch is always executed regardless of the branch condition; similarly, the data loaded by a LOAD instruction is not available to the subsequent instruction). However, in the majority of cases the compilers (and even the MIPS assembler) is able to reorder instructions to fill these latency cycles with useful instructions which do not require the results of the previous instruction (in the worst case, a NOP instruction is inserted). This effectively eliminates these latency effects and does not require the applications programmer to be aware of the pipeline structure.

The actual instruction set of the CPU was determined after extensive simulations to determine which instructions should be implemented in hardware and which operations are best synthesized in software from other basic operations. This methodology has resulted in the highest performance processor available.

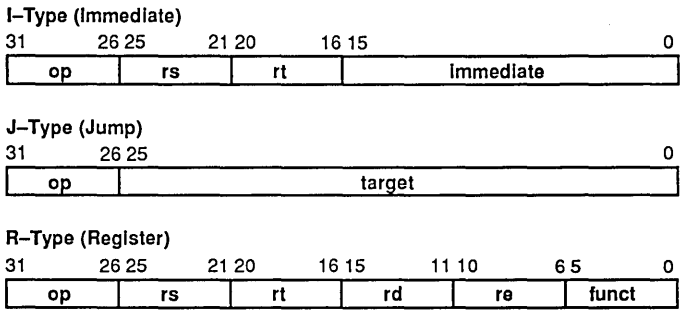


Figure 11. IDT79R3001 Instruction Formats

The IDT79R3001 instruction set can be divided into the following groups:

- **Load/Store Instructions** move data between memory and the general registers. These are all "I–Type" instructions. The only addressing mode supported is base register plus signed, immediate 16–bit offset. This effectively allows three addressing modes: register plus offset, register (using zero offset), and immediate (using r0, the zero register).

  The Load instruction has a single cycle of latency, as described above. That is, the instruction immediately after the load instruction cannot rely on the new data; however, the assembler and compilers automatically handle this, reordering code to insure that no conflicts occur. Note that the store operation has no latency in its effect.

  Loads and stores can be performed on byte, half–word, word, or unaligned word data (32–bit data not aligned on a modulo–4 address).
- Computational instructions perform arithmetic, logical, and shift operations on values in registers. They occur in both "R–Type" (both operands and the result are general registers), and "I–Type" (one operand is a 16–bit immediate value) formats.

  Note that computational instructions are three operand instructions: that is, the result register can be different from both source registers. This means that operands need not be overwritten by arithmetic operations. This results in a more efficient use of the register set, and further increases performance.
- Jump and Branch instructions change the flow of control of a program. Jumps are always to a paged absolute address formed by combining a 26–bit target with four bits of the Program Counter ("J–Type" format for subroutine calls), or 32–bit register byte addresses ("R–Type", for Returns and dispatches). Branches have 16–bit offsets relative to the program counter ("I–Type").

  Jump and Link instructions save a return address in Register 31. The IDT79R3001 instruction set features numerous branch conditions. Included is the ability to branch based on a comparison of two registers, or on the comparison of a register to zero. Thus, net performance is increased since the processor does not have to precede the branch instruction with arithmetic operations.
- Co–processor instructions perform operations in the co–processors (such as the IDT79R3010 FPA). Co–processor Loads and Stores are "I–Type"; computational instructions have co–processor dependent formats.
- Co–processor 0 instructions perform operations on the System Control Co–Processor (CP0) registers to manipulate the memory management and exception handling facilities of the on–chip co–processor.
- Special instructions perform a variety of tasks, including movement of data between general and special registers, system calls, and breakpoint operations. These are always "R–Type".

IDT79R3001 System Control Co–processor (CP0)

The IDT79R3001 can operate with up to four tightly coupled co–processors, designated CP0–CP3. CP0 is included on–chip as co–processor 0, the System Control Co–processor. CP0 is responsible for supporting both the virtual memory system and the exception handling functions of the IDT79R3001.

OP	DESCRIPTION	OP	DESCRIPTION
	Load/Store Instructions		**Multiply/Divide Instructions**
LB	Load Byte	MULT	Multiply
LBU	Load Byte Unsigned	MULTU	Multiply Unsigned
LH	Load Halfword	DIV	Divide
LHU	Load Halfword Unsigned	DIVU	Divide Unsigned
LW	Load Word	MFHI	Move From HI
LWL	Load Word Left	MTHI	Move To HI
LWR	Load Word Right	MFLO	Move From LO
SB	Store Byte	MTLO	Move To LO
SH	Store Halfword		**Jump and Branch Instructions**
SW	Store Word	J	Jump
SWL	Store Word Left	JAL	Jump and Link
SWR	Store Word Right	JR	Jump to Register
	Arithmetic Instructions (ALU Immediate)	JALR	Jump and Link Register
		BEQ	Branch on Equal
ADDI	Add Immediate	BNE	Branch on Not Equal
ADDIU	Add Immediate Unsigned	BLEZ	Branch on Less than or Equal to Zero
SLTI	Set on Less Than Immediate	BGTZ	Branch on Greater Than Zero
SLTIU	Set on Less Than Immediate Unsigned	BLTZ	Branch on Less Than Zero
		BGEZ	Branch on Greater than or Equal to Zero
ANDI	AND Immediate		
ORI	OR Immediate	BLTZAL	Branch on Less Than Zero and Link
XORI	Exclusive OR Immediate	BGEZAL	Branch on Greater than or Equal to Zero and Link
LUI	Load Upper Immediate		
			Special Instructions
	Arithmetic Instructions (3–operand, register–type)	SYSCALL	System Call
		BREAK	Break
ADD	Add		
ADDU	Add Unsigned		**Co–processor Instructions**
SUB	Subtract	LWCz	Load Word from Co–processor
SUBU	Subtract Unsigned	SWCz	Store Word to Co–processor
SLT	Set on Less Than	MTCz	Move To Co–processor
SLTU	Set on Less Than Unsigned	MFCz	Move From Co–processor
		CTCz	Move Control to Co–processor
AND	AND	CFCz	Move Control From Co–processor
OR	OR	COPz	Co–processor Operation
XOR	Exclusive OR	BCzT	Branch on Co–processor z True
NOR	NOR	BCzF	Branch on Co–processor z False
	Shift Instructions		**System Control Co–processor (CP0) Instructions**
SLL	Shift Left Logical		
SRL	Shift Right Logical	MTC0	Move To CP0
SRA	Shift Right Arithmetic	MFC0	Move From CP0
SLLV	Shift Left Logical Variable	TLBR	Read indexed TLB entry
SRLV	Shift Right Logical Variable	TLBWI	Write Indexed TLB entry
SRAV	Shift Right Arithmetic Variable	TLBWR	Write Random TLB entry
		TLBP	Probe TLB for matching entry
		RFE	Restore From Exception

Table 2. IDT79R3001 Instruction Summary

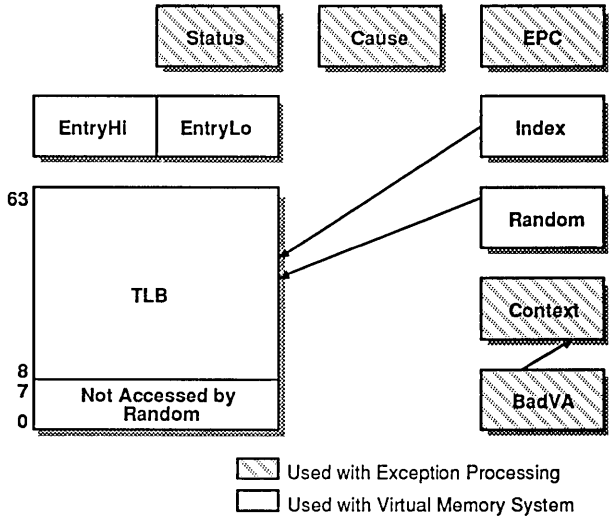


Figure 12. System Control Co–processor (CP0) Registers

CP0 Registers

As a co–processor, CP0 has a number of registers which it uses to perform its control functions. These include 64 fully associative Translation Lookaside Buffers (TLBs), used to manage the virtual memory space; registers to manage the TLB set; and the exception handling registers. Figure 12 illustrates the register set of the System Control Co–processor. Table 3 provides a brief explanation of the function of each of these registers. A more detailed explanation of the use of each of these registers is included in the "mips RISC Architecture" manual.

REGISTER	DESCRIPTION
EntryHi	High half of a TLB entry
EntryLo	Lower half of a TLB entry
Index	Programmable pointer into TLB array
Random	Pseudo–random pointer into TLB array
Status	Mode, interrupt enables and diagnostic status information
Cause	Indicates nature of last exception
EPC	Exception Program Counter—contains address of instruction which detected the exception
Context	Pointer into the kernel's virtual Page Table Entry array
BadVA	Most recent bad virtual address
PrID	Processor revision identification

Table 3. CP0 Registers

Memory Management System

The IDT79R3001 supports a virtual memory system, so that each task in a given application can be unaware of the addressing needs of other tasks. This is also useful in systems with limited physical memory; the IDT79R3001 provides for the logical expansion of memory by translating addresses composed in a large virtual space into available physical memory addresses.

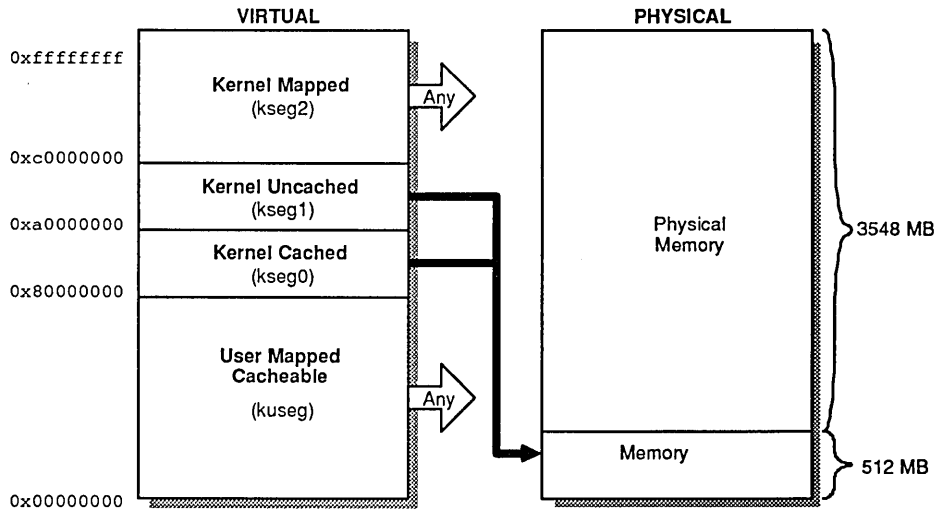
IDT79R3001 Operating Modes

The IDT79R3001 has two operating modes: User Mode and Kernel Mode. The IDT79R3001 normally operates in the User Mode until an exception is detected, forcing it into the Kernel Mode. The processor remains in Kernel Mode until the exceptions are handled and the processor executes an RFE (Return from Exception) instruction, which will restore it to User Mode. Kernel Mode allows software to alter machine state information such as that contained in the CP0 registers; that is, if in User Mode an access is attempted to Co–processor 0 and the Kernel has not enabled the User to access the co–processor, an exception will occur. Similarly, if a User task attempts to use a Kernel virtual address, an exception will occur. Thus, system resources are protected from User tasks.

The manner in which memory addresses are translated (mapped) depends on the operating mode of the IDT79R3001 and on the virtual address desired. Figure 13 illustrates the virtual address mapping performed by the IDT79R3001:

User Mode – in this mode, a single, uniform virtual address space (kuseg) of 2 Gbyte is available to each user task (tasks are further identified by a 6–bit process identifier field in order to form unique virtual addresses). All references to this segment are mapped using the TLB, which utilizes both the virtual address and the Process ID field to perform the virtual–to–physical mapping (note that this allows the cache to be shared by up to 64 User processes at a time without requiring time consuming Cache or TLB flushing).

MMU ADDRESS TRANSLATION

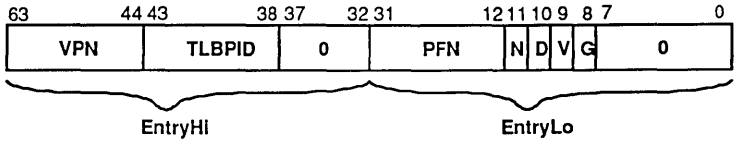


Kernel Mode – Four separate segments are accessible through this mode:

- **kuseg** – When in the Kernel Mode, references to this segment are treated just like User Mode references, thus streamlining Kernel accesses to User memory.
- **kseg0** – References to this 512 Mbyte segment may use the cache memory, but are not translated by the TLB. Instead, these addresses map directly to the first 512 Mbytes of the physical address space. Note that many dedicated embedded applications will utilize this address space and kseg1 only, rather than any of the TLB mapped segments.
- **kseg1** – References to this 512 Mbyte segment are not mapped through the TLB. Additionally, this memory is viewed as uncacheable, which means that references through this segment will always use the asynchronous memory interface. As with kseg0, references through this segment are hard–mapped to the first 512 Mbytes of physical memory. When the processor boots, the reset vector is contained in this segment, so that the processor does not require either the cache or the TLB to be valid at RESET time.
- **kseg2** – References to this 1 Gbyte segment are always mapped through the TLB. As with kuseg, the ability of memory pages to be cached is determined by a bit setting in the TLB entry for that page.

The Translation Lookaside Buffer (TLB)

The translation of virtual addresses in either kuseg or kseg2 (mapped segments) is performed by the on–chip Translation Lookaside Buffer array. This array consists of 64 fully–associative (content addressable) memory elements. Each entry maps a 4Kbyte virtual page to a 4Kbtye physical page. Each TLB entry contains other information about the virtual address it maps (such as which User process it maps) and also about the physical address (such as whether it is cacheable or writeable).



VPN–Virtual Page Number
TLBPID – Process Identifier
PFN – Physical Frame Number
N – Non–cacheable Physical Page
D – Dirty Page / Write Protect
V – Valid TLB Entry
G – Global translation (ignore PID)
0 – Reserved

Figure 14. TLB Entry Format

Figure 14 illustrates the format of each TLB entry. The translation operation is illustrated in Figure 15. The upper portion of the desired virtual address is compared against the VPN field of each TLB entry. Additionally, the current process ID (contained in the TLBHI register) is matched against the PID field of the TLB entry (if the TLB entry is marked as Global, the PID comparison is ignored). If a match occurs, and the TLB entry is marked as Valid, then the translation is completed by replacing the VPN of the virtual address with the corresponding PFN (Physical Frame Number).

Note that the use of the TLB does not incur an execution penalty, since the execution engine pipeline includes stages to cover for the time required to make the TLB search and translation.

TLB misses occur when no successful match occurs. These events are handled in software. The CP0 registers give the software enough information to obtain the appropriate TLB entry at speeds which exceed those achieved by many CPUs which use hardware TLB replacement (10–12 cycles under UNIX).

When a TLB miss occurs, the address of the instruction which was executing is stored in the EPC register, and the BadVA register contains the address which was being translated. The Context register uses the BadVA value to generate a direct pointer to the kernel Page Table Entry for the desired virtual address. The Random register suggests the TLB entry to be replaced by the new entry. Note that the lower eight TLB entries are not pointed to by Random; the kernel software can thus insure that it is constantly mapped, and deterministic response is guaranteed.

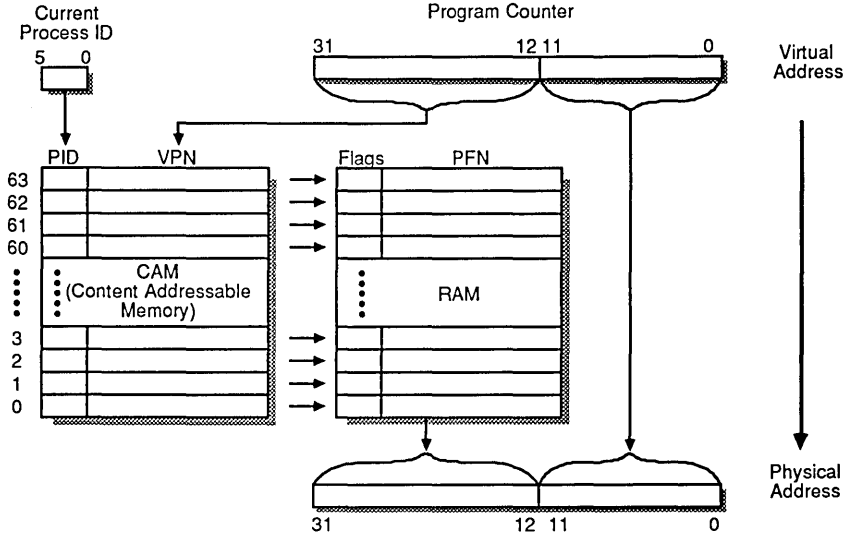


Figure 15. Virtual to Physical TLB Translation

BACKWARD COMPATIBILITY WITH IDT79R2000A AND 79R3000 PROCESSORS

The IDT79R3001 can execute the same binary software (either kernel or user) that is executed by either the IDT79R2000A or IDT79R3000. At the system level, some hardware re–design is necessary to achieve the cost savings inherent in the IDT79R3001 hardware interface.

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
Memory Interface		
Data (0:31)	I/O	A 32–bit bus used for all instruction and data transmission among the processor, synchronous memory space, asynchronous memory space and co–processors.
DataP (0:3)	I/O	A 4–bit bus containing even parity over the data bus. If parity checking is enabled, a parity error will cause the $\overline{\text{PErr}}$ signal to be asserted and a cache–miss to occur. Regardless of whether parity checking is enabled, the processor will always generate parity on writes.
Tag (13:31)	I/O	A 19–bit bus used for transferring cache tags and high–order address bits between the processor, caches and asynchronous memory spaces.
AddrLo (0:23)	O	A 24–bit bus containing low–order byte addresses for both the synchronous (cache) and asynchronous memory spaces.
Synchronous Memory Control		
$\overline{\text{IRd}}$	O	The output enable for the instruction cache. The polarity of this signal is selectable.
$\overline{\text{IWr}}$	O	The write enable for the instruction cache. The polarity of this signal is selectable.
IClk	O	The instruction cache address latch clock. The clock runs continuously.
$\overline{\text{DRd}}$	O	The output enable for the data cache. The polarity of this signal is selectable.
$\overline{\text{DWr}}$	O	The write enable for the data cache. The polarity of this signal is selectable.
DClk	O	The data cache address latch clock. The clock runs continuously.
Valid	I/O	A high on this signal indicates that the Tags just read from the cache are valid. When a cache update occurs, the processor will generate the appropriate Valid bit.
$\overline{\text{PErr}}$	O	If parity checking is enabled, this signal is an active low output of the internal CP0 parity error status bit. It is driven low when a parity error is detected and remains low until software clears the parity error flag in the status register. This pin is physically the same pin as AccTyp2. Its function is selected during device reset.
Asynchronous Memory Interface		
$\overline{\text{XEn}}$	O	The transceiver enable for the read buffer.
AccTyp (0:2)	O	A 3–bit bus used to indicate the size of data being transferred on the asynchronous memory bus, whether or not a data transfer is occurring and the purpose of the transfer. If parity checking is enabled, AccTyp2 becomes the $\overline{\text{PErr}}$ signal.
$\overline{\text{MemWr}}$	O	Signals the occurance of an asynchronous memory write cycle.
$\overline{\text{MemRd}}$	O	Signals the occurance of an asynchronous memory read cycle.
$\overline{\text{BusError}}$	I	Signals the occurance of a bus error during an asynchronous memory transfer cycle.
$\overline{\text{Run}}$	O	Indicates whether the processor is in a RUN or STALL state.
$\overline{\text{Exception}}$	O	Indicates the instruction about to commit processor state should be aborted and other exception related information.
$\overline{\text{SysOut}}$	O	A clock derived from the internal processor clock used to generate the system clock.
RdBusy	I	The asynchronous memory read stall termination signal. In most system designs, RdBusy is normally asserted and is deasserted only to indicate the successful completion of the memory read. RdBusy is sampled by the processor only during memory read stalls.
$\overline{\text{WrBusy}}$	I	The asynchronous memory write stall initiation/termination signal. $\overline{\text{WrBusy}}$ is only sampled during write operation.
Co–Processor Interface		
$\overline{\text{CpSync}}$	O	A clock which is identical to $\overline{\text{SysOut}}$ and used by co–processors for timing synchronization with the CPU.
CpBusy	I	The co–processor busy stall initiation/termination signal.
CpCond (0:3)	I	A 4–bit bus used to transfer conditional branch status from the co–processors to the CPU. CpCond(0) is used to control whether or not a cache burst refill occurs; the other signals are used as input port pins for co–processor branch instructions.
Processor Control Signals		
DMAStall	I	DMA Stall. Signals to the processor that it should stall accesses to the synchronous memories and tri–state the synchronous memory interface.
$\overline{\text{Int}}$ (0:5)	I	A 6–bit bus used to signal maskable interrupts to the CPU. A reset time, mode values are sampled from this bus to initialize the processor. During normal operation, these signals are not latched by the processor and must remain asserted until the processor acknowledges the interrupt (through software) to the interrupt source.
Clk2xSys	I	The master double frequency input clock, used to generate $\overline{\text{SysOut}}$.
Clk2xSmp/Rd	I	A double frequency clock input used to determine the sample point for data coming into the CPU and co–processors and used to determine the enable time of the synchronous memory RAMs.
Clk2xPhi	I	A double frequency clock input used to determine the position of the two internal phases.
$\overline{\text{Reset}}$	I	Initialization input used to force execution starting from the reset memory address. $\overline{\text{Reset}}$ should be asserted asynchronously but must be negated synchronously with the leading edge of $\overline{\text{SysOut}}$.

ABSOLUTE MAXIMUM RATINGS[1, 3]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature[2]	−55 to +125	−65 to +150	°C
V_{IN}	Input Voltage	−0.5 to +7.0	−0.5 to +7.0	V

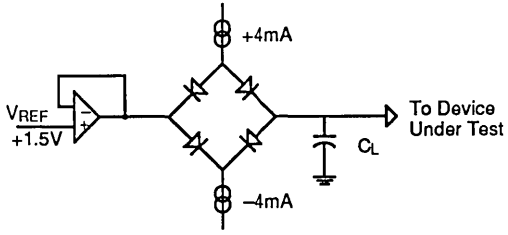
NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = −3.0V for pulse width less than 15ns.
   V_{IN} should not exceed V_{CC} +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0 ± 5%

OUTPUT LOADING FOR AC TESTING



SIGNAL	C_L
$\overline{IRd}$, $\overline{DRd}$, $\overline{IWr}$, $\overline{DWr}$	50pF
All others	25pF

DC ELECTRICAL CHARACTERISTICS— COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67MHz MIN.	16.67MHz MAX.	20.0MHz MIN.	20.0MHz MAX.	25.0MHz MIN.	25.0MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4mA	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OH} = 4mA	—	0.4	—	0.4	—	0.4	V
V_{OHT}	Output HIGH Voltage [4,7]	V_{CC} = Min., I_{OH} = −8mA	2.4	—	2.4	—	2.4	—	V
V_{OHC}	Output HIGH Voltage [8]	V_{CC} = Min., I_{OH} = −4mA	4.0	—	4.0	—	4.0	—	V
V_{OLT}	Output LOW Voltage [4,7]	V_{CC} = Min., I_{OH} = 8mA	—	0.8	—	0.8	—	0.8	V
V_{IH}	Input HIGH Voltage [5]		2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage		—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage [2,5]		3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage [1,2]		—	0.4	—	0.4	—	0.4	V
I_{RESET}	Input HIGH Current[6]		10	100	10	100	10	100	µA
C_{IN}	Input Capacitance[7]		—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance[7]		—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = Max.	—	575	—	650	—	750	mA
I_{IH}	Input HIGH Leakage [3]	V_{IH} = V_{CC}	—	10	—	10	—	10	µA
I_{IL}	Input LOW Leakage [3]	V_{IL} = GND	−10	—	−10	—	−10	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	−40	40	−40	40	−40	40	µA

NOTES:

1. V_{IL} Min. = −3.0V for pulse width less than 15ns. V_{IL} should not fall below −0.5 Volts for longer periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp/Rd, Clk2xPhi, CpBusy, and $\overline{Reset}$.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag buses only. Note that V_{IH} and V_{IL} also apply to these signals. V_{OHT} and V_{OLT} are supplied as additional information to help the system designer understand the relationship between current drive and output voltage on these pins.
5. V_{IH} should not be held above Vcc + 0.5 volts.
6. The IDT79R3001 contains an internal pull-up/current source on the TAG pins to facilitate initialization. This current source is disconnected when $\overline{Reset}$ is inactive.
7. Guaranteed by design.
8. V_{OHC} applies to $\overline{Run}$ and $\overline{Exception}$.

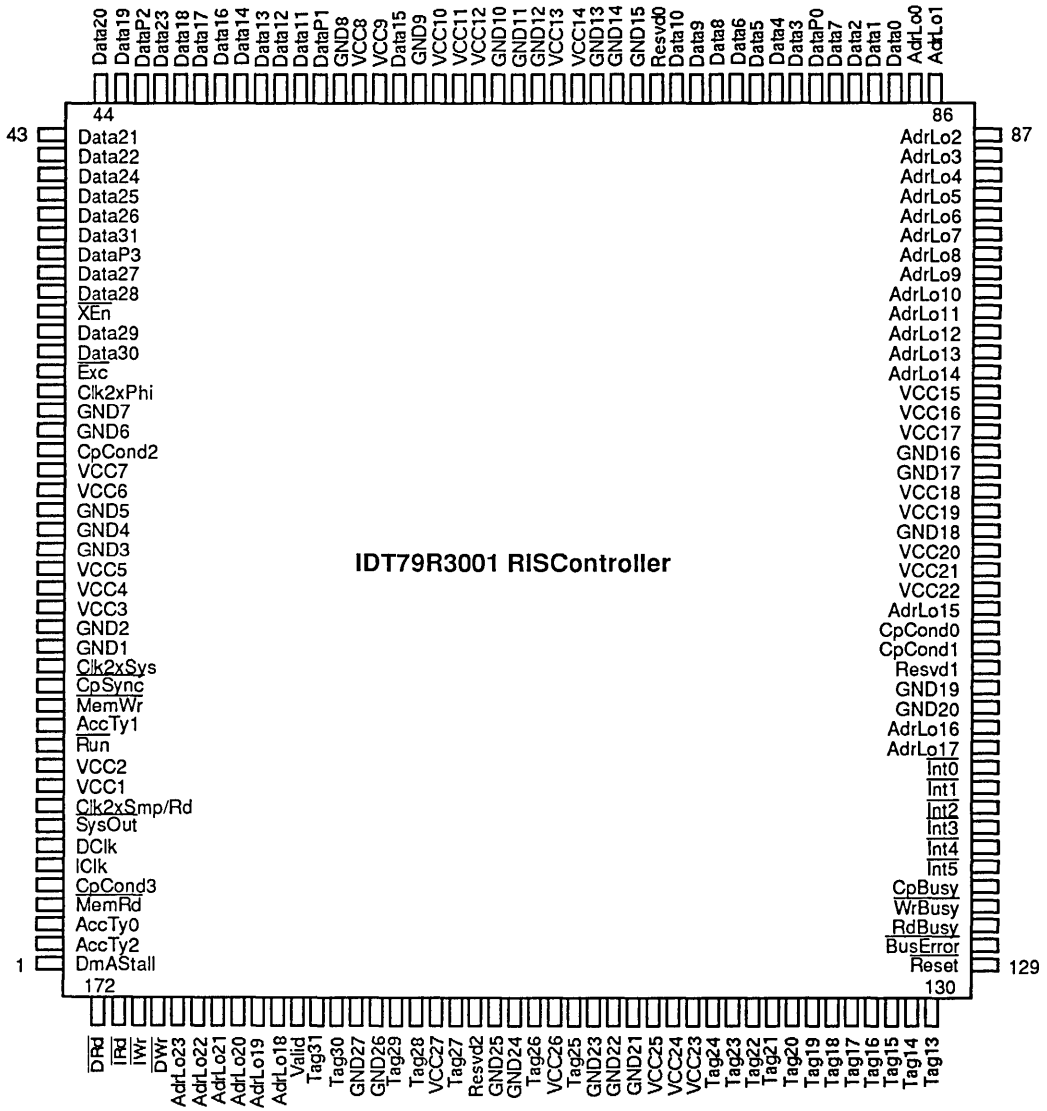
AC ELECTRICAL CHARACTERISTICS—(1,4)
COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67MHz MIN.	16.67MHz MAX.	20.0MHz MIN.	20.0MHz MAX.	25.0MHz MIN.	25.0MHz MAX.	UNIT
Clock									
T_{CkHigh}	Input Clock High(2)	Transition < 5ns	12.5	—	10	—	8	—	ns
T_{CkLow}	Input Clock Low(2)	Transition < 5ns	12.5	—	10	—	8	—	ns
T_{CkP}	Input Clock Period(5)		30	500	25	500	20	500	ns
	Clk2xSys to Clk2xSmp/Rd(5)		0	Tcyc/4	0	Tcyc/4	0	Tcyc/4	ns
	Clk2xSmp/Rd to Clk2xPhi(5)		9	Tcyc/4	7	Tcyc/4	5	Tcyc/4	ns
Run Operation									
T_{DEn}	Data Enable(3)		—	–2	—	–2	—	–1.5	ns
T_{DDis}	Data Disable(3)		—	–1	—	–1	—	–0.5	ns
T_{DVal}	Data Valid	Load = 25pF	—	3	—	3	—	2	ns
T_{WrDly}	Write Delay	Load = 25pF	—	5	—	4	—	3	ns
T_{DS}	Data Set–up		9	—	8	—	6	—	ns
T_{DH}	Data Hold		–2.5	—	–2.5	—	–2.5	—	ns
T_{CBS}	CpBusy Set–up		13	—	11	—	9	—	ns
T_{CBH}	CpBusy Hold		–2.5	—	–2.5	—	–2.5	—	ns
T_{AcTy}	Access Type (1:0)	Load = 25pF	—	7	—	6	—	5	ns
T_{AT2}	Access Type2	Load = 25pF	17	—	14	—	12	—	ns
T_{MWr}	Memory Write	Load = 25pF	1	27	1	23	1	18	ns
T_{Exc}	Exception	Load = 25pF	—	7	—	7	—	5	ns
Stall Operation									
T_{SAVal}	Address Valid	Load = 25pF	—	30	—	23	—	20	ns
T_{SAcTy}	Address Type	Load = 25pF	—	27	—	23	—	18	ns
T_{MRdi}	Memory Read Initiate	Load = 25pF	1	27	1	23	1	18	ns
T_{MRd}	Read Terminate	Load = 25pF	—	7	—	7	—	5	ns
T_{Stl}	Run Terminate	Load = 25pF	2	17	2	15	2	11	ns
T_{Run}	Run Initiate	Load = 25pF	—	7	—	6	—	4	ns
T_{SMWr}	Memory Write	Load = 25pF	1	27	1	23	1	18	ns
T_{SEc}	Exception Valid	Load = 25pF	—	20	—	18	—	15	ns
T_{DMADis}	DMA Drive On	Load = 25pF	3	15	3	15	3	15	ns
T_{DMAEn}	DMA Drive Off	Load = 25pF	—	10	—	10	—	10	ns
Reset Initialization									
T_{RST}	Reset Pulse Width		6	—	6	—	6	—	Tcyc
T_{RSTTAG}	Reset Pulse Width, Pull–downs on Tag		140	—	140	—	140	—	µS
Capacitive Load Deration									
C_{LD}	Load Derate(6)		0.5	1	0.5	1	0.5	1	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all three 2x Clocks: Clk2xSys, Clk2xSmp/Rd and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters are illustrated in detail in the "IDT79R3001 Hardware Interface Guide".
5. Tcyc is one CPU clock cycle (2 cycles of a 2x clock).
6. With the exception of $\overline{Run}$, no two signals of a given device will derate by a difference greater than 15%.

PIN CONFIGURATIONS
172–Pin Ceramic Flatpack (Cavity Side View)



Note:
1. AccTyp2 is redefined to be Parity Error if the parity enable option is selected at device initialization.

PIN CONFIGURATIONS (continued)
144–Pin PGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VCC14	AdrLo 6	AdrLo 10	AdrLo 11	VCC12	AdrLo 14	AdrLo 15	CpCond 0	AdrLo 16	AdrLo 17	$\overline{Int2}$	$\overline{Int5}$	$\overline{Wr}$ $\overline{Busy}$	$\overline{Reset}$	VCC10
B	AdrLo 3	$\overline{Mem}$ $\overline{Wr}$	AdrLo 7	AdrLo 9	AdrLo 12	$\overline{Cp}$ $\overline{Sync}$	AdrLo 13	CpCond 1	$\overline{Int1}$	$\overline{Int3}$	Cp Busy	$\overline{Bus}$ $\overline{Error}$	$\overline{Run}$	Tag13	Tag16
C	AdrLo 0	AdrLo 4	VCC13	AdrLo 5	AdrLo 8	GND13	GND12	VCC11	$\overline{Int0}$	$\overline{Int4}$	Rd Busy	GND11	Tag14	Tag17	Tag20
D	Data 1	AdrLo 2	GND0										Tag15	Tag19	Tag21
E	DataP 0	Data 0	AdrLo 1										Tag18	Tag22	VCC9
F	VCC0	Data 7	Data 2										GND10	Tag23	Tag25
G	Data 4	Data 3	GND1										GND9	Tag24	Tag26
H	Data 6	Data 5	Data 8				IDT79R3001 RISController						VCC8	Tag28	Tag27
J	Data 10	DataP 1	Data 9										Tag31	Valid	Tag29
K	Data 15	Data 11	GND2										GND8	AdrLo 19	Tag30
L	VCC1	Data 12	Data 17										AdrLo 22	AdrLo 20	AdrLo 18
M	Data 13	Data 16	DataP 2										GND7	AdrLo 23	VCC7
N	Data 14	Data 18	Data 19	GND3	Data 24	DataP 3	VCC3	VCC4	GND5	GND6	$\overline{Mem}$ $\overline{Rd}$	DmA Stall	$\overline{DRd}$	$\overline{IWr}$	AdrLo 21
P	Data 23	Data 20	AccTy1	Data 22	Data 26	Data 27	$\overline{XEn}$	Data 30	Clk2x Sys	Clk2x Smp/Rd	$\overline{DClk}$	Cp Cond3	AccTy0	$\overline{IRd}$	$\overline{DWr}$
Q	VCC2	Data 21	Data 25	Data 31	Data 28	GND4	Data 29	$\overline{Excep}$ $\overline{tion}$	Clk2x Phi	Cp Cond2	$\overline{SysOut}$	VCC5	IClk	AccTy2	VCC6

Note:
1. AccTyp2 is redefined to be $\overline{Parity\ Error}$ if the parity enable option is selected at device initialization.

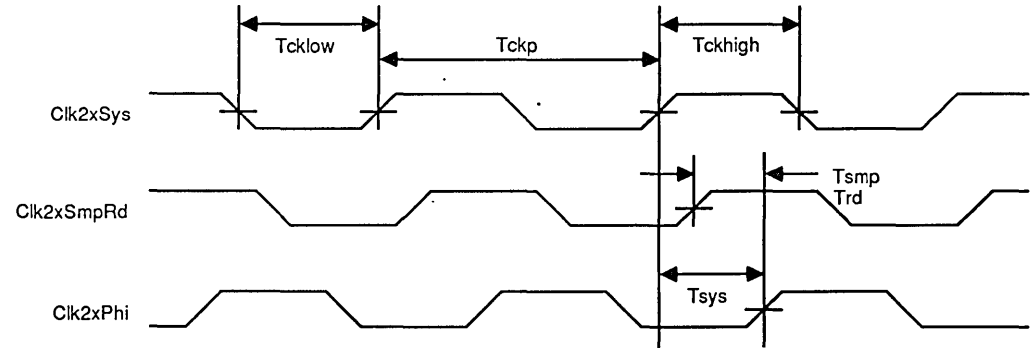
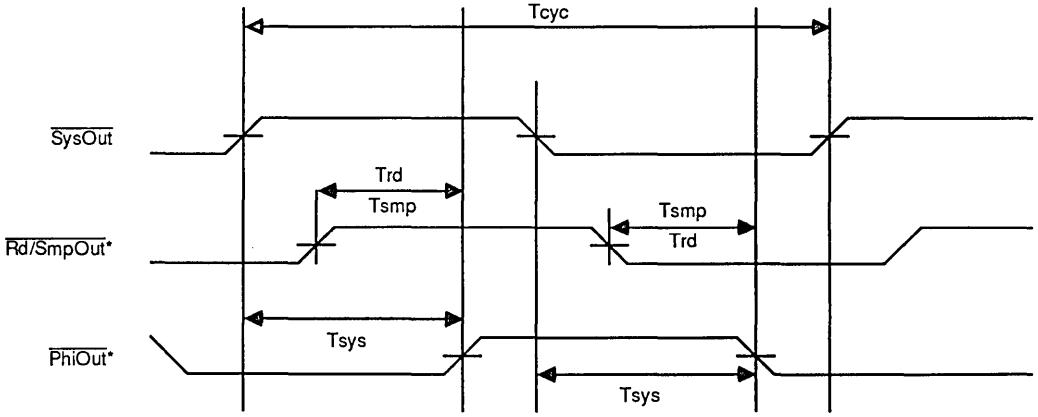


Figure 16. Input Clock Timing



* These signals are not actually output from the processor. They are drawn to provide a reference for other timing diagrams.

Figure 17. Processor Reference Clock Timing

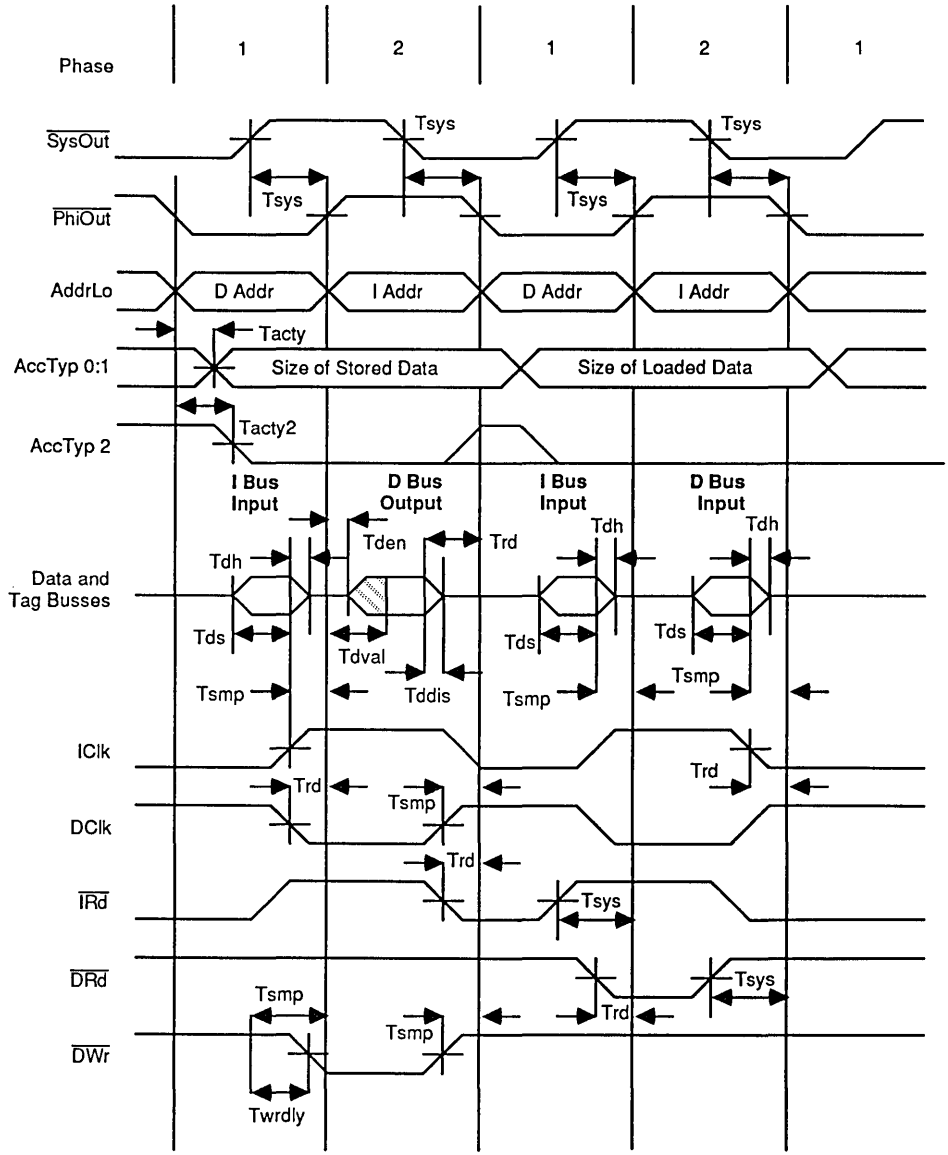


Figure 18. Synchronous Memory (Cache) Timing

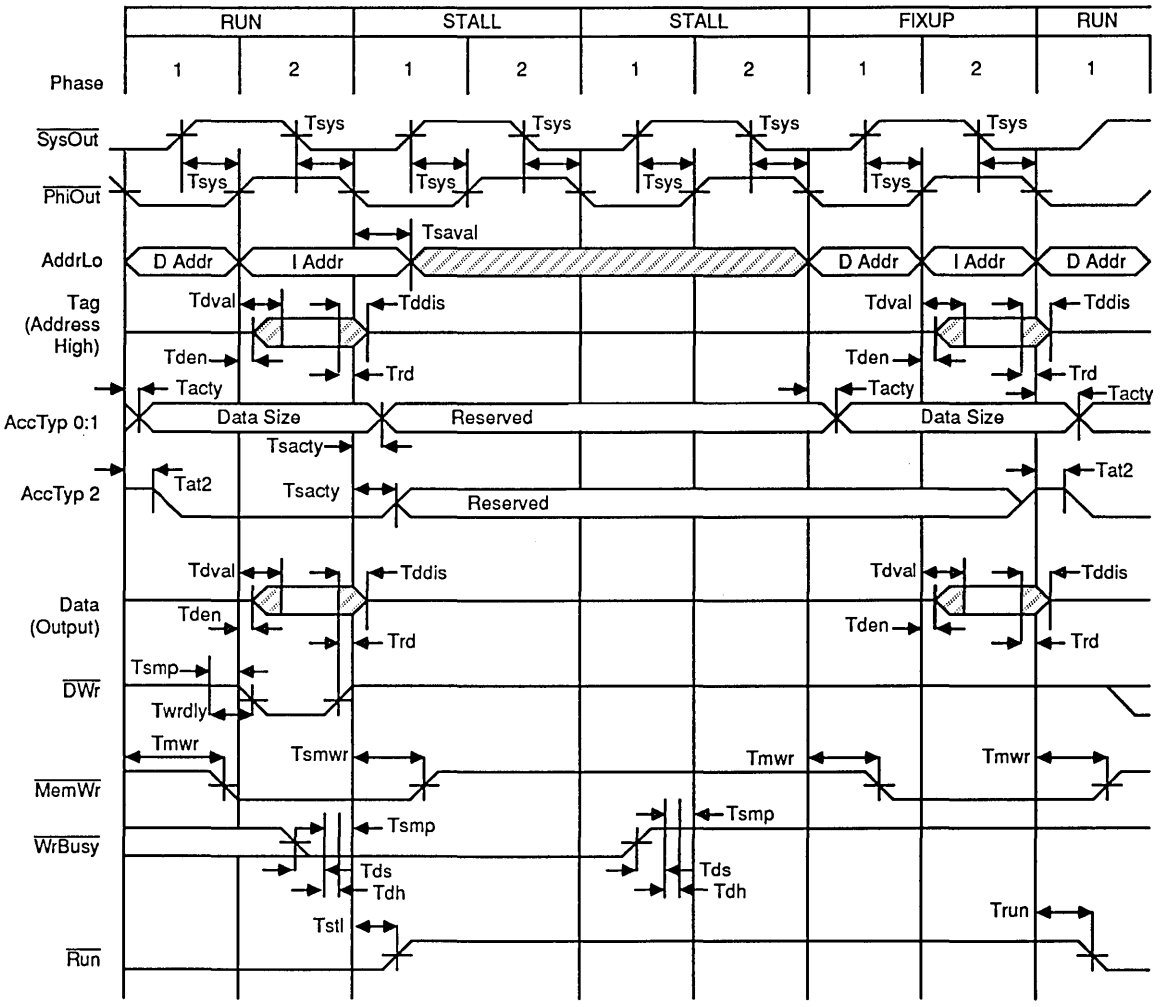


Figure 19. Memory Write Timing

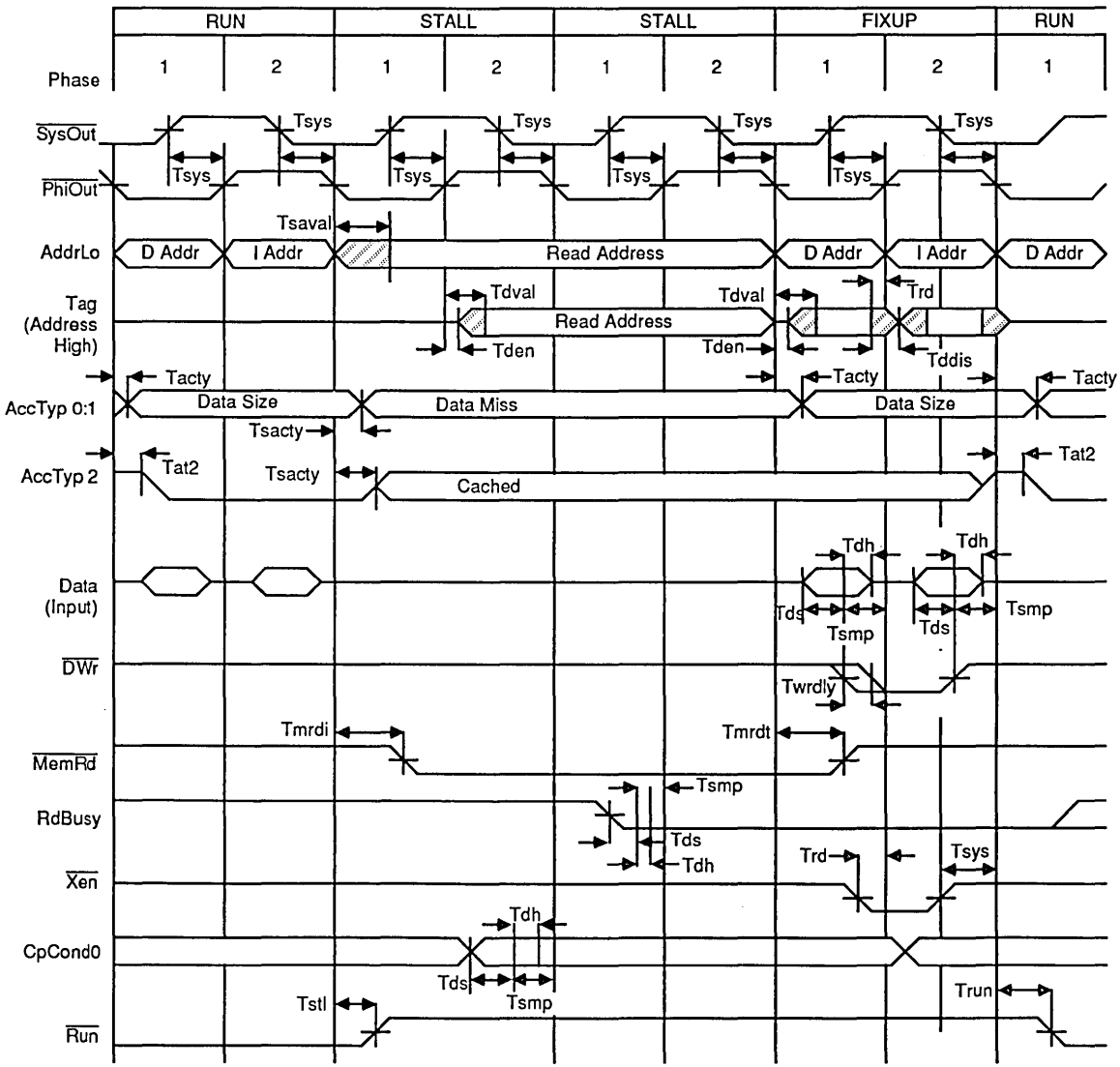


Figure 20. Memory Read Timing

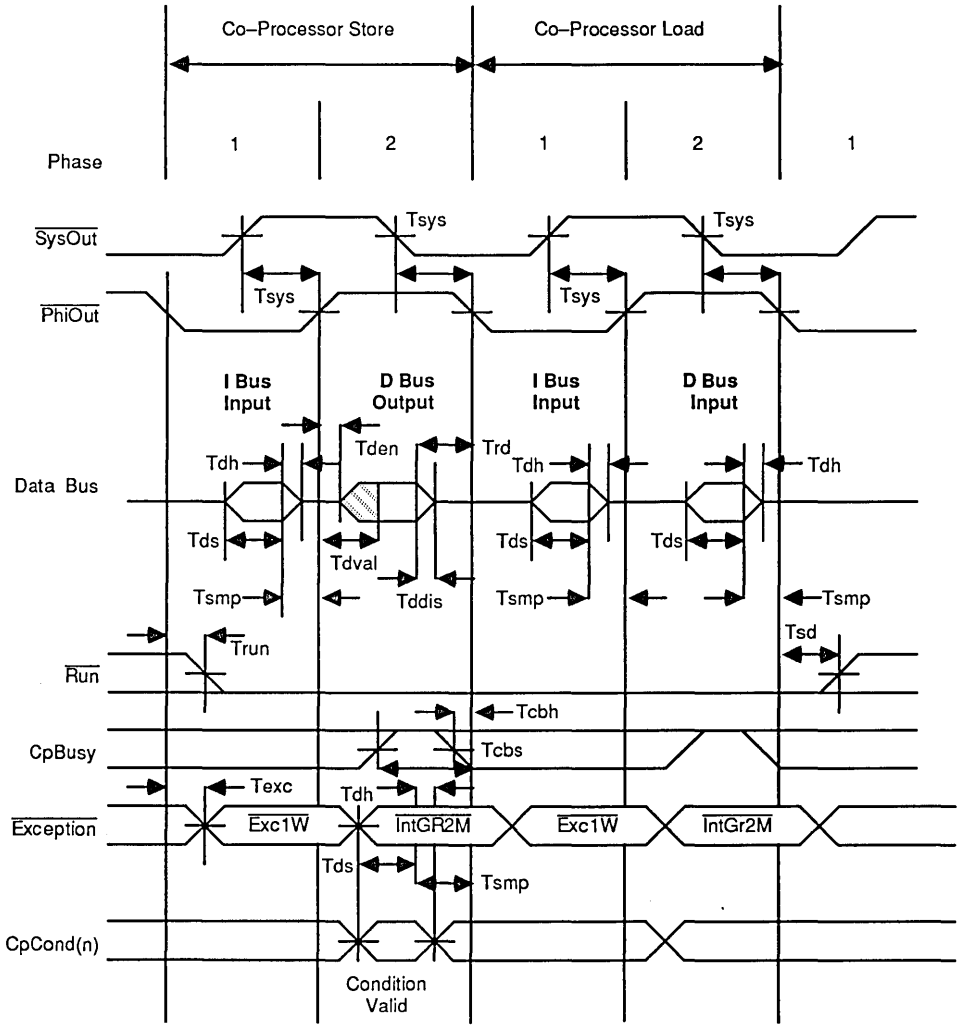


Figure 21. Co–Processor Load/Store Timing

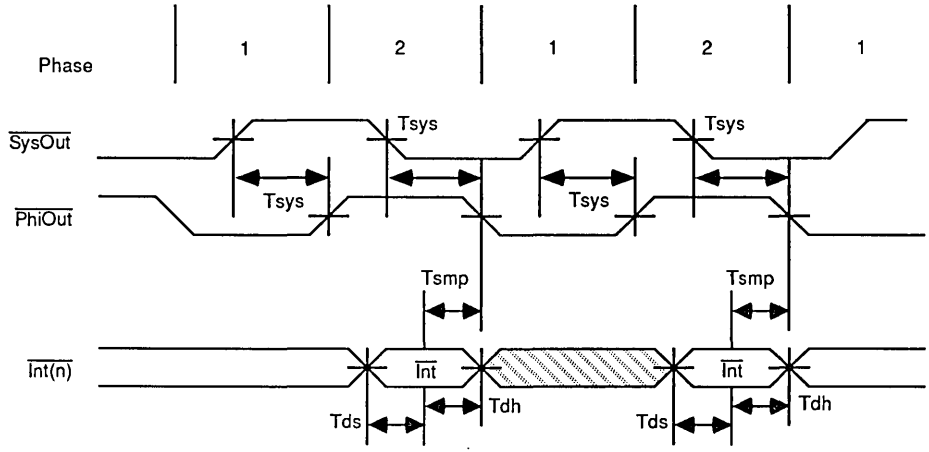
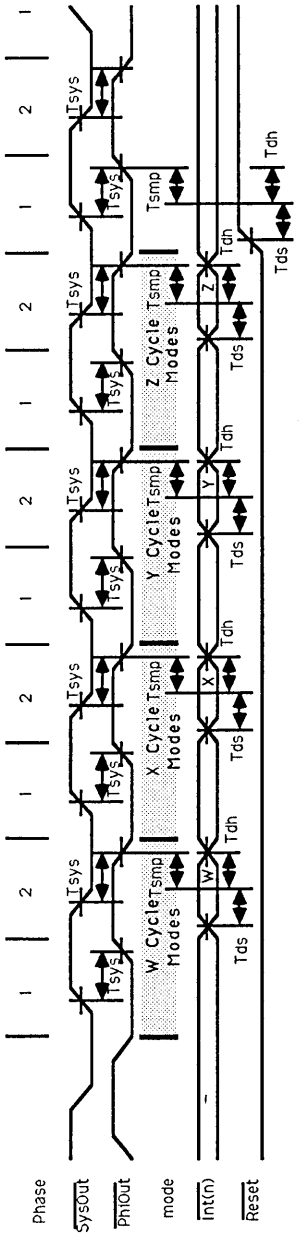


Figure 22. Interrupt Timing



NOTES:

1. Reset must be negated synchronously; however, it can be asserted asynchronously. Designs should not rely on the proper functioning of $\overline{\text{SysOut}}$ prior to the assertion of $\overline{\text{Reset}}$.
2. If $\overline{\text{Phase-Lock On}}$ or $\overline{\text{R3000 Mode}}$ are asserted as mode select options, they should be asserted throughout the Reset period, to insure that the slowest co-processor in the system has sufficient time to lock the CPU clocks.
3. $\overline{\text{Reset}}$ is acturally sampled in both Phase 1 and Phase 2. To insure proper initialization, it is recommended that $\overline{\text{Reset}}$ be negated relative to the end of Phase 1.

Figure 23. Mode Vector Initialization

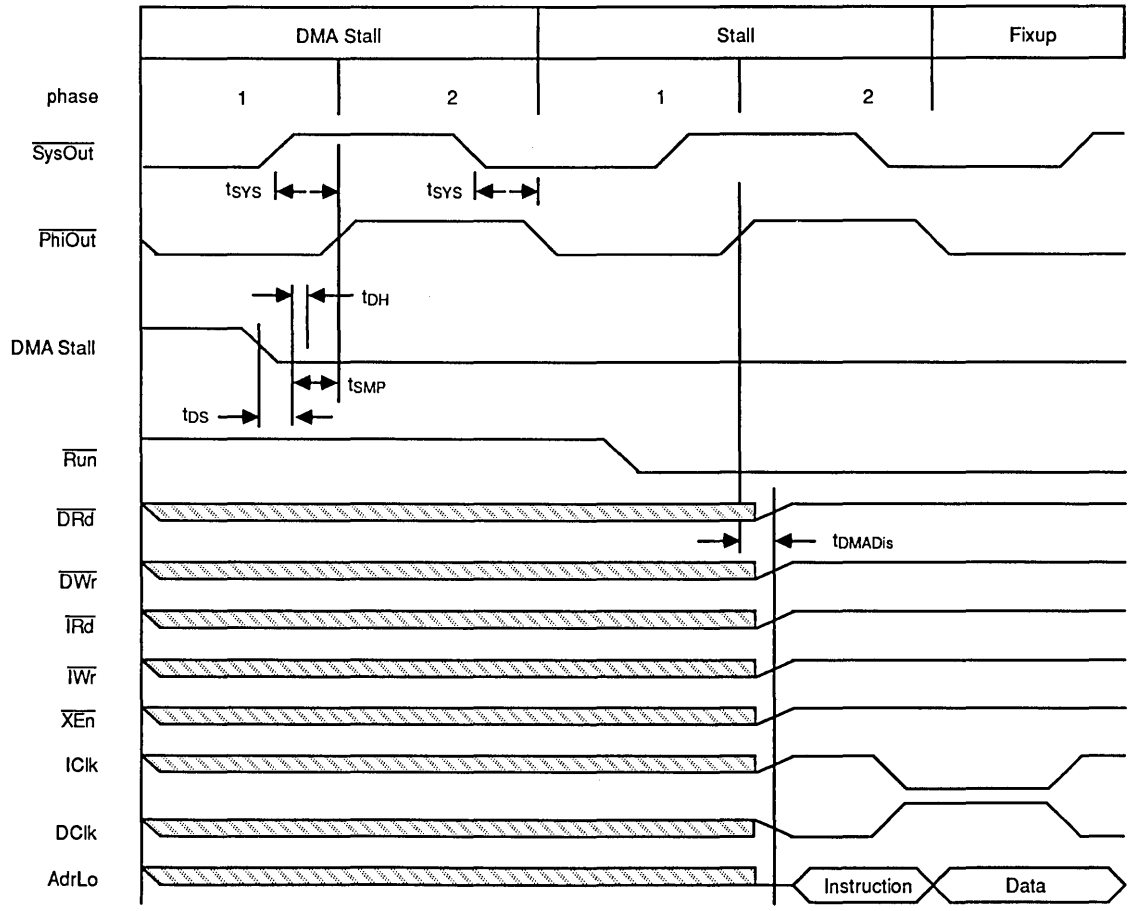


Figure 24. Entering DMA Stall

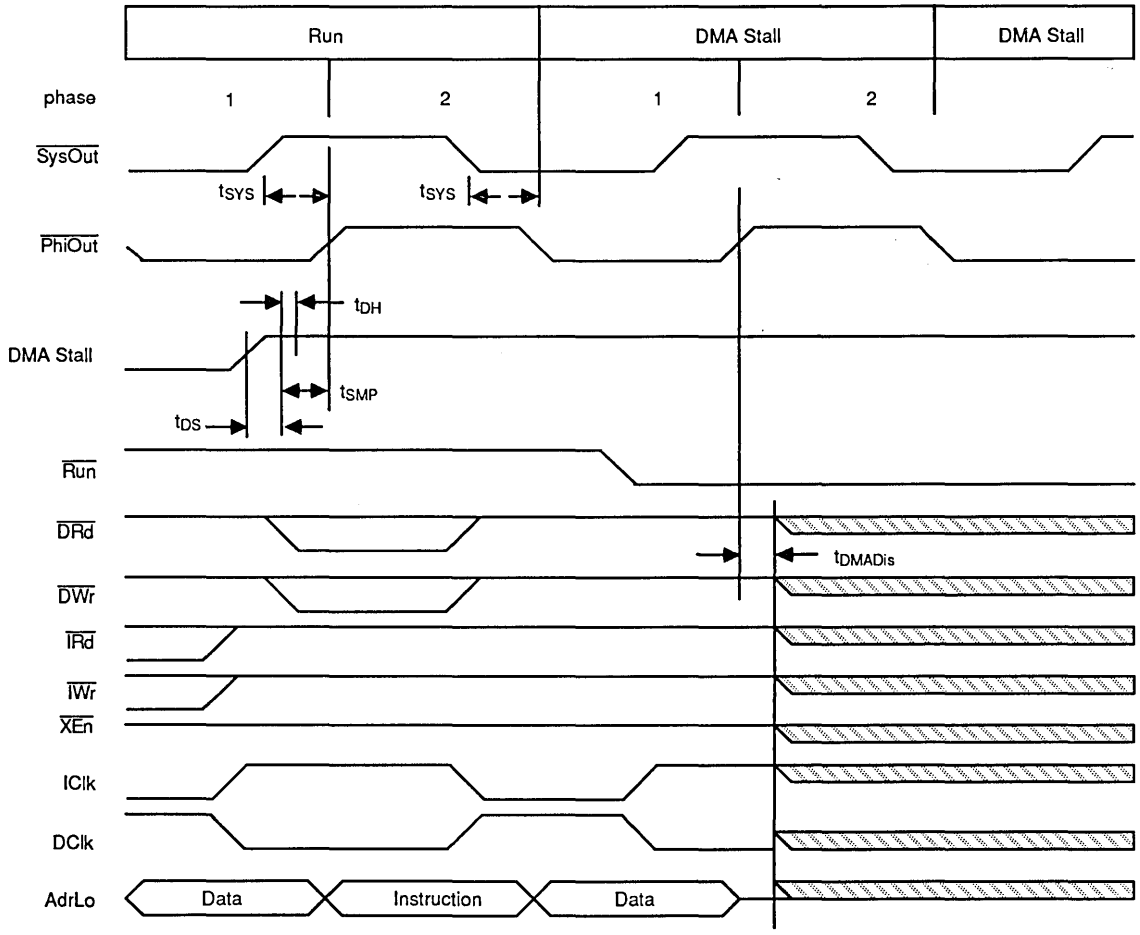
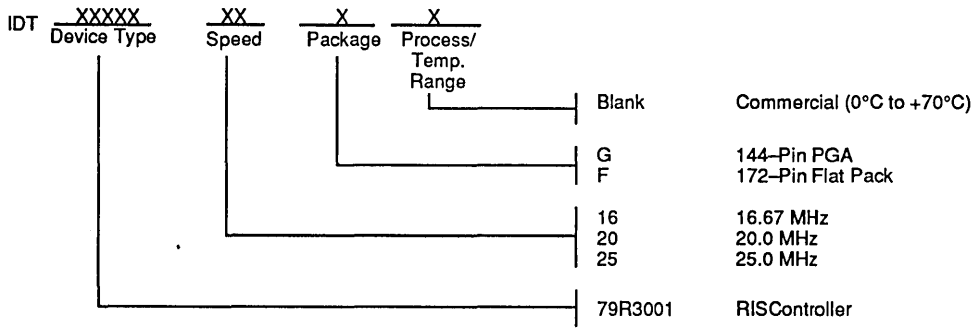


Figure 25. Completing DMA Stall

ORDERING INFORMATION



Integrated Device Technology, Inc.

RISC FLOATING-POINT ACCELERATOR (FPA)

IDT79R3010

FEATURES:

- Hardware Support of Single- and Double-Precision Operations:
  - Floating-Point Add
  - Floating-Point Subtract
  - Floating-Point Multiply
  - Floating-Point Divide
  - Floating-Point Comparisons
  - Floating-Point Conversions
- Sustained performance:
  - 9 MFLOPS single precision LINPACK
  - 6 MFLOPS double precision LINPACK
- Cycle Time:
  - 30ns (33.33MHz)
  - 40ns (25MHz)
  - 60ns (16.67MHz)
  - 80ns (12.5MHz)
- Direct, high-speed interface with IDT79R3000 Processor
- Supports Full Conformance With IEEE 754–1985 Floating-Point Specification
- Full 64-bit operation using sixteen 64-bit data registers
- High-speed CEMOS™ technology
- Pin, function and software compatible with the IDT79R2010A RISC FPA
- Military product compliant to MIL-STD-883, Class B
- 32-bit status/control register providing access to all IEEE-Standard exception handling
- Load/store architecture allows data movement directly between FPA and memory or between CPU and FPA
- Overlapped operation of independent floating point ALUs

DESCRIPTION:

The IDT79R3010 Floating-Point Accelerator (FPA) operates in conjunction with the IDT79R3000 Processor and extends the IDT79R3000's instruction set to perform arithmetic operations on values in floating-point representations. The IDT79R3010 FPA, with associated system software, fully conforms to the requirements of ANSI/IEEE Standard 754–1985, "IEEE Standard for Binary Floating-Point Arithmetic." In addition, the architecture fully supports the standard's recommendations.

This data sheet provides an overview of the features and architecture of the 79R3010 FPA, Revision 2.0. A more detailed description of the operation of the device is incorporated in the "R3000 Family Hardware User's Manual", and a more detailed architectural overview is provided in the "mips RISC Architecture" book, both available from IDT.

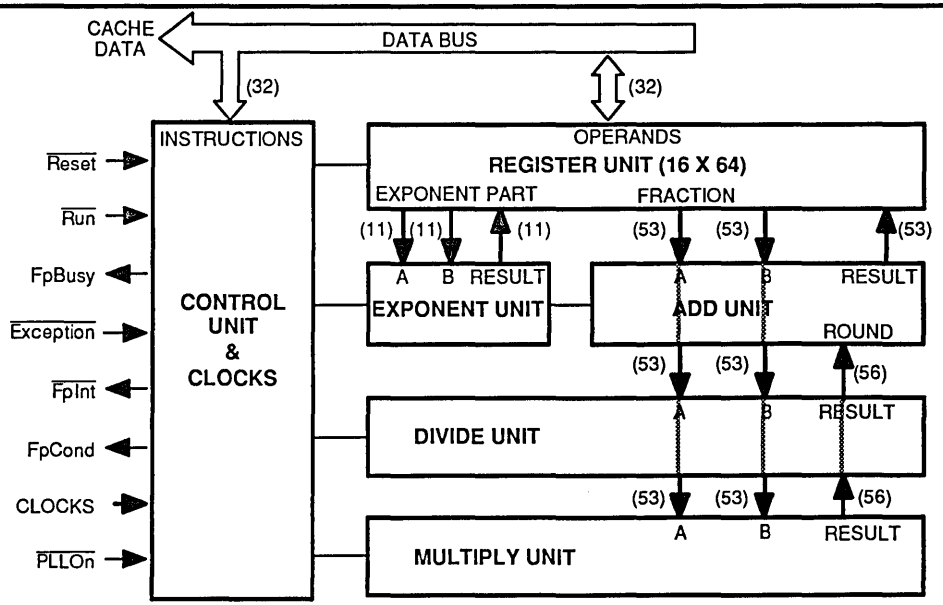


Figure 1. IDT79R3010 Functional Block Diagram

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DSC-9022/2

IDT79R3010 FPA REGISTERS

The IDT79R3010 FPA provides 32 general purpose 32-bit registers, a Control/Status register, and a Revision Identification register. The tightly-coupled coprocessor interface causes the register resources of the FPA to appear to the systems programmers as an extension of the CPU internal registers. The FPA registers are shown in Figure 2.

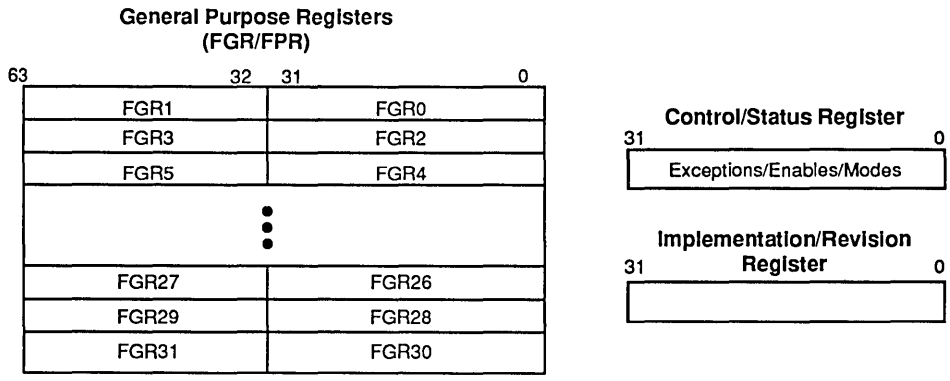


Figure 2. IDT79R3010 FPA Registers

Floating-point coprocessor operations reference three types of registers:

- Floating-Point Control Registers (FCR)
- Floating-Point General Registers (FGR)
- Floating-Point Registers (FPR)

Floating-Point General Registers (FGR)

There are 32 Floating-Point General Registers (FGR) on the FPA. They represent directly-addressable 32-bit registers, and can be accessed by Load, Store, or Move Operations.

Floating-Point Registers (FPR)

The 32 FGRs described in the preceding paragraph are also used to form sixteen 64-bit Floating-Point Registers (FPR). Pairs of general registers (FGRs), for example FGR0 and FGR1 (refer to Figure 2) are physically combined to form a single 64-bit FPR. The FPRs hold a value in either single- or double-precision floating-point format. Double-precision format FPRs are formed from two adjacent FGRs.

Floating-Point Control Registers (FCR)

There are 2 Floating-Point Control Registers (FCR) on the FPA. They can be accessed only by Move operations and include the following:

- Control/Status register, used to control and monitor exceptions, operating modes, and rounding modes;
- Revision register, containing revision information about the FPA.

COPROCESSOR OPERATION

The FPA continually monitors the IDT79R3000 processor instruction stream. If an instruction does not apply to the coprocessor, it is ignored; if an instruction does apply to the coprocessor, the FPA executes that instruction and transfers necessary result and exception data synchronously to the IDT79R3000 main processor.

The FPA performs three types of operations:

- Loads and Stores;
- Moves;
- Two- and three-register floating-point operations.

Load, Store, and Move Operations

Load, Store, and Move operations move data between memory or the IDT79R3000 Processor registers and the IDT79R3010 FPA registers. These operations perform no format conversions and cause no floating-point exceptions. Load, Store, and Move operations reference a single 32-bit word of either the Floating-Point General Registers (FGR) or the Floating-Point Control Registers (FCR).

Floating-Point Operations

The FPA supports the following single- and double-precision format floating-point operations:

- Add
- Subtract
- Multiply
- Divide
- Absolute Value
- Move
- Negate
- Compare

In addition, the FPA supports conversions between single- and double-precision floating-point formats and fixed-point formats.

The FPA incorporates separate Add/Subtract, Multiply, and Divide units, each capable of independent and concurrent operation. Thus, to achieve very high performance, floating point divides can be overlapped with floating point multiplies and floating point additions. These floating point operations occur independently of the actions of the CPU, allowing further overlap of integer and floating point operations. Figure 3 illustrates an example of the types of overlap permissible.

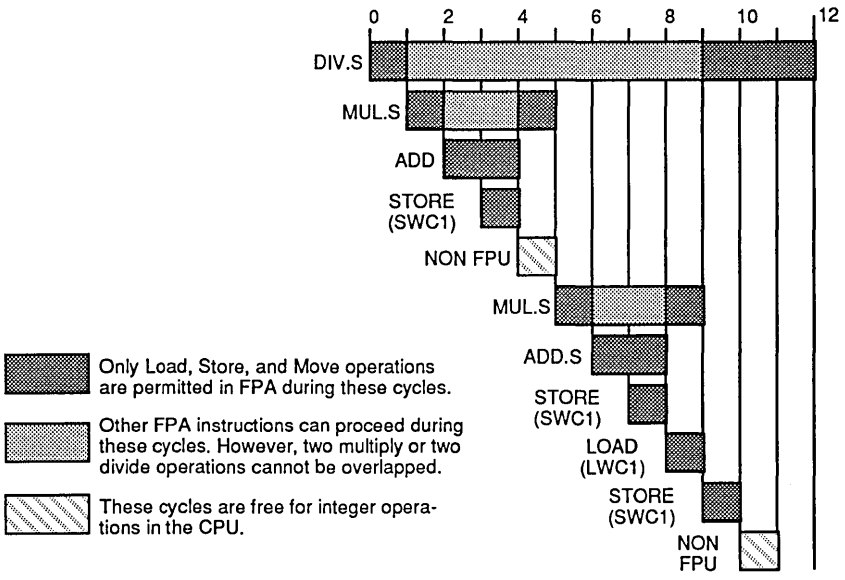


Figure 3. Examples of Overlapping Floating Point Operation

Exceptions

The IDT79R3010 FPA supports all five IEEE standard exceptions:

- Invalid Operation
- Inexact Operation
- Division by Zero
- Overflow
- Underflow

The FPA also supports the optional, Unimplemented Operation exception that allows unimplemented instructions to trap to software emulation routines.

The FPA provides precise exception capability to the CPU; that is, the execution of a floating point operation which generates an exception causes that exception to occur at the CPU instruction which caused the operation. This precise exception capability is a requirement in applications and languages which provide a mechanism for local software exception handlers within software modules.

INSTRUCTION SET OVERVIEW

All IDT79R3010 instructions are 32 bits long and they can be divided into the following groups:

- **Load/Store and Move** instructions move data between memory, the main processor and the FPA general registers.
- **Computational** instructions perform arithmetic operations on floating point values in the FPA registers.
- **Conversion** instructions perform conversion operations between the various data formats.
- **Compare** instructions perform comparisons of the contents of registers and set a condition bit based on the results. The result of the compare operation is output on the FpCond output of the FPA, which is typically used as CpCond1 on the CPU for use in coprocessor branch operations.

Table 1 lists the instruction set of the IDT79R3010 FPA.

OP	Description	OP	Description
	Load/Store/Move Instructions		**Computational Instructions**
LWC1	Load Word to FPA	**ADD.fmt**	Floating–point Add
SWC1	Store Word from FPA	**SUB.fmt**	Floating–point Subtract
MTC1	Move Word to FPA	**MUL.fmt**	Floating–point Multiply
MFC1	Move Word from FPA	**DIV.fmt**	Floating–point Divide
CTC1	Move Control word to FPA	**ABS.fmt**	Floating–point Absolute value
CFC1	Move Control word from FPA	**MOV.fmt**	Floating–point Move
		NEG.fmt	Floating–point Negate
	Conversion Instructions		**Compare Instructions**
CVT.S.fmt	Floating–point Convert to Single FP	**C.cond.fmt**	Floating–point Compare
CVT.D.fmt	Floating–point Convert to Double FP		
CVT.W.fmt	Floating–point Convert to fixed–point		

Table 1. IDT79R3010 Instruction Summary

IDT79R3010 PIPELINE ARCHITECTURE

The IDT79R3010 FPA provides an instruction pipeline that parallels that of the IDT79R3000 processor. The FPA, however, has a 6-stage pipeline instead of the 5-stage pipeline of the IDT79R3000: the additional FPA pipe stage is used to provide efficient coordination of exception responses between the FPA and main processor.

The execution of a single IDT79R3010 instruction consists of six primary steps:

1) **IF**—Instruction Fetch. The main processor calculates the instruction address required to read an instruction from the I-Cache. No action is required of the FPA during this pipe stage since the main processor is responsible for address generation.
2) **RD**—The instruction is present on the data bus during phase 1 of this pipe stage and the FPA decodes the data on the bus to determine if it is an instruction for the FPA.
3) **ALU**—If the instruction is an FPA instruction, instruction execution commences during this pipe stage.
4) **MEM**—If this is a coprocessor load or store instruction, the FPA presents or captures the data during phase 2 of this pipe stage.
5) **WB**—The FPA uses this pipe stage solely to deal with exceptions.
6) **FWB**—The FPA uses this stage to write back ALU results to its register file. This stage is the equivalent of the WB stage in the IDT79R3000 main processor.

Each of these steps requires approximately one FPA cycle as shown in Figure 3 (parts of some operations spill over into another cycle while other operations require only 1/2 cycle).

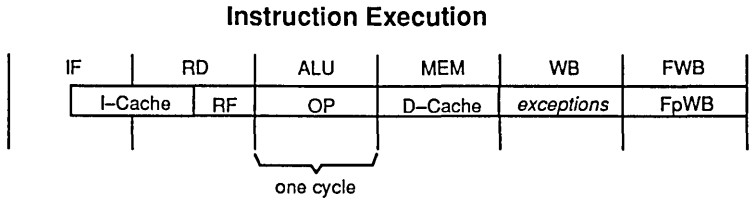


Figure 4. IDT79R3010 Instruction Summary

The IDT79R3010 uses a 6-stage pipeline to achieve an instruction execution rate approaching one instruction per FPA cycle. Thus, execution of six instructions at a time are overlapped as shown in Figure 5.

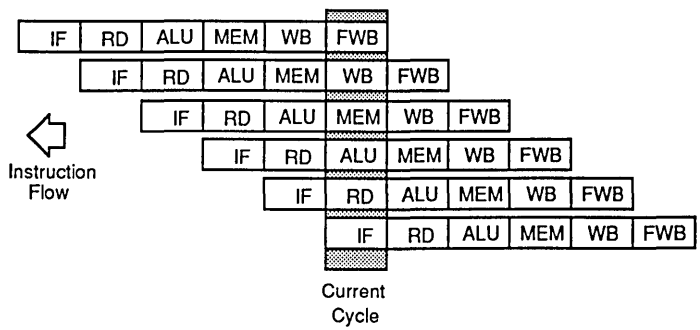
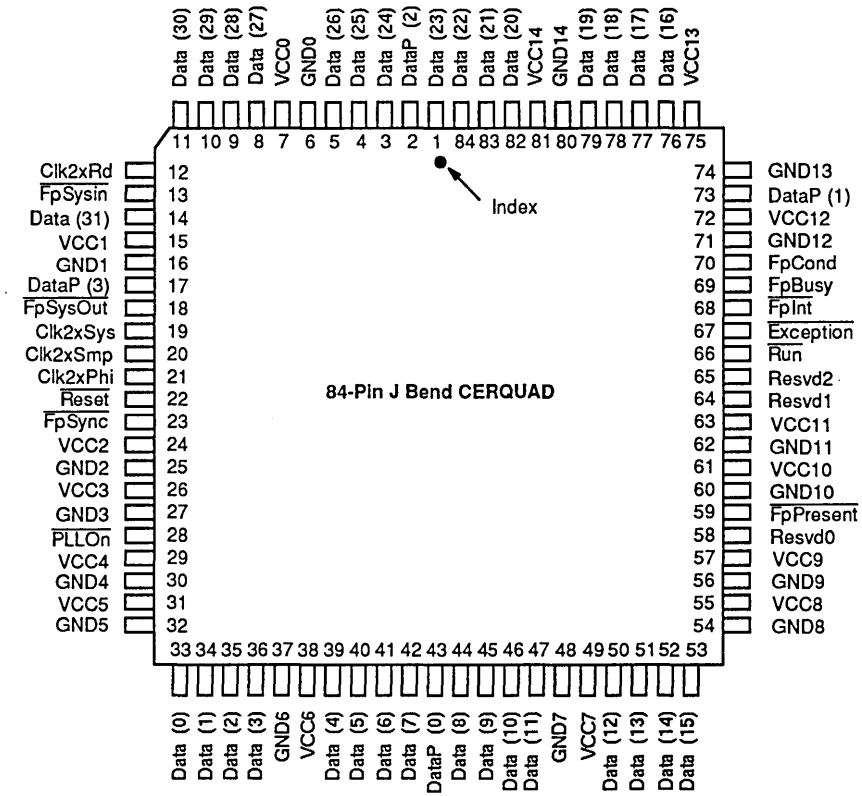


Figure 5. IDT79R3010 Instruction Pipeline

This pipeline operates efficiently because different FPA resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

PIN CONFIGURATION
(Top View)



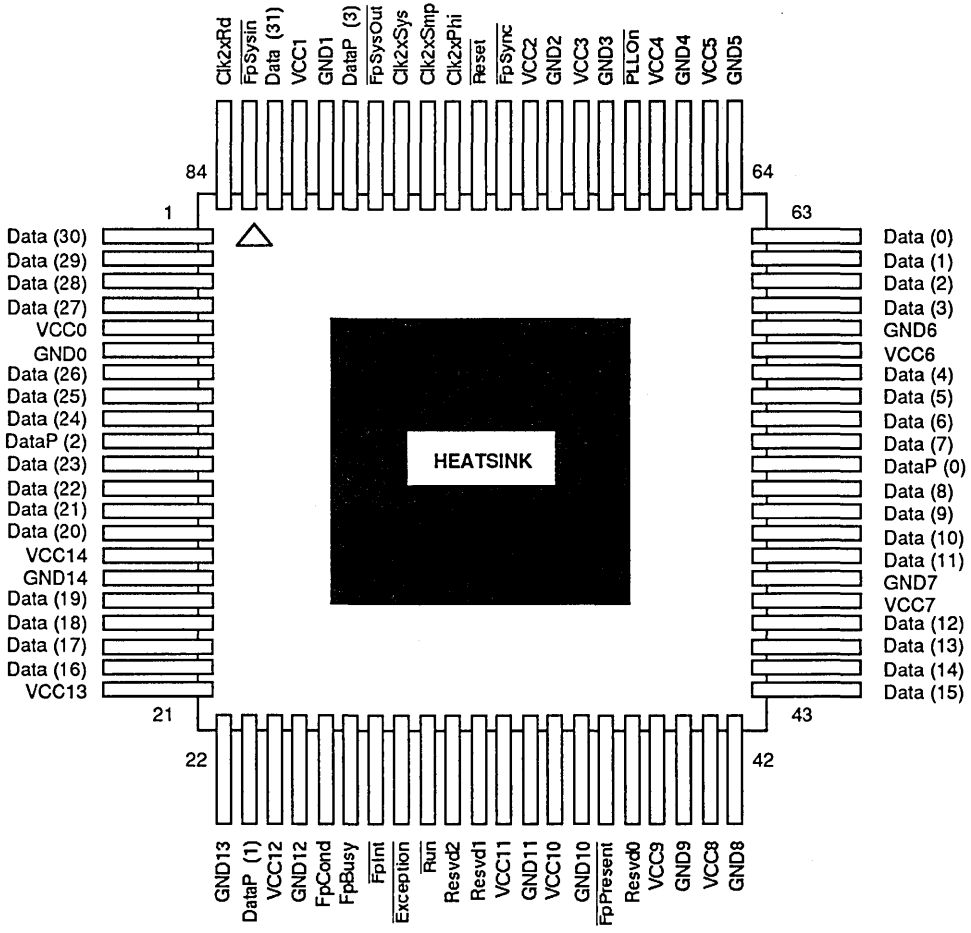
Note:
Reserved pins must not be connected.

PIN CONFIGURATION
(Ceramic, Cavity Down)— BOTTOM VIEW

	1	2	3	4	5	6	7	8	9	10	11	12
M	Vss	Vcc	Data 17	DataP 1	Vss	FP Cond	$\overline{\text{FPInt}}$	Vss	$\overline{\text{Run}}$	Rsrvd 1	Vcc	Vss
L	Data 21	Data 20	Data 18	Data 16	Vcc	FPBusy	Except-tion	Vcc	Rsrvd 2	$\overline{\text{FP}}$ Present	Data 15	Data 14
K	Vss	Vcc	Data 19							Rsrvd 0	Vcc	Vss
J	Data 23	Data 22									Data 13	Data 12
H	Data 24	DataP 2									Data 11	Data 10
G	Data 26	Data 25				84–Pin Ceramic Pin Grid Array					Vcc	Vss
F	Vss	Vcc									Data 8	Data 9
E	Data 27	Data 28									Data 7	DataP 0
D	Data 29	Data 30									Data 5	Data 6
C	Vss	Vcc	Clk2x Rd							Data 2	Vcc	Vss
B	$\overline{\text{Fp}}$ SysIn	Data 31	DataP 3	Vcc	Clk2x Sys	Vcc	Clk2x Phi	Vcc	$\overline{\text{PllOn}}$	Data 1	Data 3	Data 4
A	Vss	Vcc	$\overline{\text{FpSys}}$ Out	Vss	Clk2x Smp	Vss	$\overline{\text{Reset}}$	Vss	$\overline{\text{FP}}$ Sync	Data 0	Vcc	Vss

NOTE:
1. Reserved pins must not be connected.

PIN CONFIGURATION
84–L QUAD FLATPACK (CAVITY DOWN)
TOP VIEW



NOTE:
1. Reserved pins must not be connected.

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
Data (0–31)	I/O	A multiplexed 32-bit bus used for instruction and data transfers on phase 1 and phase 2, respectively.
DataP (0–3)	O	A 4-bit bus containing even parity over the data bus. Parity is generated by the FPA on stores.
$\overline{\text{Run}}$	I	Input to the FPA which indicates whether the processor-coprocessor system is in the run or stall state.
$\overline{\text{Exception}}$	I	Input to the FPA which indicates exception related status information.
FpBusy	O	Signal to the CPU indicating a request for a coprocessor busy stall.
FpCond	O	Signal to the CPU indicating the result of the last comparison operation.
$\overline{\text{FpInt}}$	O	Signal to the CPU indicating that a floating-point exception has occurred for the current FPA instruction.
$\overline{\text{Reset}}$	I	Synchronous initialization input used to distinguish the processor-FPA synchronization period from the execution period. $\overline{\text{Reset}}$ must be synchronized by the leading edge of $\overline{\text{SysOut}}$ from the CPU.
$\overline{\text{PllOn}}$	I	Input which during the reset period determines whether the phase lock mechanism is enabled and during the execution period determines the output timing model.
$\overline{\text{FpPresent}}$	O	Output which is pulled to ground through an impedance of approximately 0.5k ohms. By providing an external pullup on this line, an indication of the presence or absence of the FPA can be obtained.
Clk2xSys	I	A double frequency clock input used for generating $\overline{\text{FpSysOut}}$.
Clk2xSmp	I	A double frequency clock input used to determine the sample point for data coming into the FPA.
Clk2xRd	I	A double frequency clock input used to determine the disable point for the data drivers.
Clk2xPhi	I	A double frequency clock input used to determine the position of the internal phases, phase 1 and phase 2.
$\overline{\text{FpSysOut}}$	O	Synchronization clock from the FPA.
$\overline{\text{FpSysIn}}$	I	Input used to receive the synchronization clock from the FPA.
$\overline{\text{FpSync}}$	I	Input used to receive the synchronization clock from the CPU.

ABSOLUTE MAXIMUM RATINGS[1, 3]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature[2]	–55 to +125	–65 to +150	°C
V_{IN}	Input Voltage	–0.5 to +7.0	–0.5 to +7.0	V

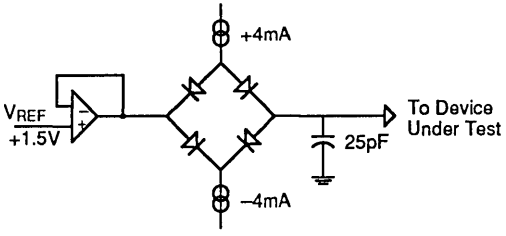
NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –3.0V for pulse width less than 15ns.
   V_{IN} should not exceed V_{CC} +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	–55°C to +125°C	0V	5.0 ± 10%
Commercial	0°C to +70°C	0V	5.0 ± 5%

OUTPUT LOADING FOR AC TESTING



DC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0 V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	33.33MHz MIN.	33.33MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{OLFP}	Output LOW Voltage[5]	V_{CC} = Min, I_{OL} = 1.5mA	—	0.5	—	0.5	—	0.5	—	0.5	V
V_{IH}	Input HIGH Voltage[6]		2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage[1]		—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage[2,6]		3.0	—	3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage[1,2]		—	0.4	—	0.4	—	0.4	—	0.4	V
V_{IHC}	Input HIGH Voltage[4,6]		4.0	—	4.0	—	4.0	—	4.0	—	V
V_{ILC}	Input LOW Voltage[1,4]		—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance[7]		—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance[7]		—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = Max	—	625	—	675	—	750	—	900	mA
I_{IH}	Input HIGH Leakage[3]	V_{IH} = V_{CC}	–10	10	–10	10	–10	10	–10	10	µA
I_{IL}	Input LOW Leakage[3]	V_{IL} = GND	–10	10	–10	10	–10	10	–10	10	µA
I_{OZ}	Output Tri–state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–40	40	–40	40	–40	40	–40	40	µA

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5V for longer periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, $\overline{\text{FpSysIn}}$, $\overline{\text{FpSync}}$ and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{IHC} and V_{ILC} apply to $\overline{\text{Run}}$, $\overline{\text{PllOn}}$ and $\overline{\text{Exception}}$.
5. V_{OLFP} applies to the $\overline{\text{FPPresent}}$ pin only.
6. V_{IH} and V_{IHS} should not be held above Vcc + 0.5 Volts.
7. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS — MILITARY TEMPERATURE RANGE (T_A = −55°C to +125°C, V_{CC} = +5.0 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4mA	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min., I_{OL} = 1.5mA	—	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	V
V_{IHS}	Input HIGH Voltage(2,6)		3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	V
V_{IHC}	Input HIGH Voltage(4,6)		4.0	—	V
V_{ILC}	Input LOW Voltage(1,4)		—	0.4	V
C_{IN}	Input Capacitance(7)		—	10	pF
C_{OUT}	Output Capacitance(7)		—	10	pF
I_{CC}	Operating Current	V_{CC} = Max.	—	720	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	−10	10	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	−10	10	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	−40	40	µA

NOTES:

1. V_{IL} Min. = −3.0V for pulse width less than 15ns. V_{IL} should not fall below −0.5V for longer periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, $\overline{\text{FpSysIn}}$, $\overline{\text{FpSync}}$ and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{IHC} and V_{ILC} apply to $\overline{\text{Run}}$, $\overline{\text{PllOn}}$ and $\overline{\text{Exception}}$.
5. V_{OLFP} applies to the $\overline{\text{FPPresent}}$ pin only.
6. V_{IH}, V_{IHC} and V_{IHS} should not be held above Vcc + 0.5 V.
7. Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS — (1, 3)

COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0 V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	33.33 MHz MIN.	33.33 MHz MAX.	UNIT
Clock											
T_{CkHigh}	Input Clock High(2)	Transition < High	12	—	10	—	8	—	8	—	ns
T_{CkLow}	Input Clock Low(2)	Transition < High	12	—	10	—	8	—	6	—	ns
T_{CkP}	Input Clock Period		30	1000	25	1000	20	1000	15	1000	ns
	Clk2xSys to Clk2xSmp(5)		0	tcyc/4	0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		9	tcyc/4	7	tcyc/4	5	tcyc/4	3.5	tcyc/4	ns
Timing Parameters											
T_{DEn}	Data Enable(3)		—	–2	—	–2	—	–1.5	—	–1	ns
T_{DDIs}	Data Disable(3)		—	–1	—	–1	—	–0.5	—	–0.5	ns
T_{DVal}	Data Valid	Load = 25pF	—	3	—	3	—	2	—	2	ns
T_{RSDS}	Reset Set–up		15	—	15	—	10	—	10	—	ns
T_{DS}	Data Set–up		9	—	8	—	6	—	4.5	—	ns
T_{DH}	Data Hold		–2.5	—	–2.5	—	–2.5	—	–2.5	—	ns
T_{FpCond}	Fp Condition		—	35	—	30	—	25	—	18	ns
T_{FpBusy}	Fp Busy		—	15	—	13	—	10	—	7	ns
T_{FpInt}	Fp Interrupt		—	40	—	35	—	25	—	18	ns
T_{FpMov}	Fp Move To		—	35	—	30	—	25	—	18	ns
T_{ExS}	Exception Set–up		10	—	9	—	7	—	7	—	ns
T_{ExH}	Exception Hold		0	—	0	—	0	—	0	—	ns
T_{RunS}	Run Set–up		10	—	9	—	7	—	7	—	ns
T_{RunH}	Run Hold		–2	—	–2	—	–2	—	–2	—	ns
Reset Initialization											
T_{rstPLL}	Reset Timing, Phase–lock on(4, 5)		3000	—	3000	—	3000	—	3000	—	Tcyc
T_{rst}	Reset Timing, Phase–lock off(5)		128	—	128	—	128	—	128	—	Tcyc
Capacitive Load Deration											
CLD	Load Derate(6)		0.5	1	0.5	1	0.5	1	0.5	1	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. With $\overline{\text{PllOn}}$ asserted, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. No two signals on a given device will derate for a given load by a difference greater than 15%.

AC ELECTRICAL CHARACTERISTICS — (1, 3)

MILITARY TEMPERATURE RANGE (T_A = −55°C to +125°C, V_{CC} = +5.0 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	16.67 MHz MIN.	MAX.	UNIT
Clock					
T_{CkHigh}	Input Clock High(2)	Transition < High	12	—	ns
T_{CkLow}	Input Clock Low(2)	Transition < High	12	—	ns
T_{CkP}	Input Clock Period		30	500	ns
	Clk2xSys to Clk2xSmp(5)		0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		9	tcyc/4	ns
Timing Parameters					
T_{DEn}	Data Enable(3)		—	−2	ns
T_{DDis}	Data Disable(3)		—	−1	ns
T_{DVal}	Data Valid	Load = 25pF	—	3	ns
T_{RSDS}	Reset Set−up		15	—	ns
T_{DS}	Data Set−up		9	—	ns
T_{DH}	Data Hold		2.5	—	ns
T_{FpCond}	Fp Condition		—	35	ns
T_{FpBusy}	Fp Busy		—	15	ns
T_{FpInt}	Fp Interrupt		—	40	ns
T_{FpMov}	Fp Move To		—	35	ns
T_{ExS}	Exception Set−up		10	—	ns
T_{ExH}	Exception Hold		0	—	ns
T_{RunS}	Run Set−up		10	—	ns
T_{RunH}	Run Hold		−2	—	ns
Reset Initialization					
T_{rstPLL}	Reset Timing, Phase−lock on(4, 5)		3000	—	Tcyc
T_{rst}	Reset Timing, Phase−lock off(5)		128	—	Tcyc
Capacitive Load Deration					
CLD	Load Derate(6)		0.5	1	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. With $\overline{\text{PllOn}}$ asserted, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. No two signals on a given device will derate for a given load by a difference greater than 15%.

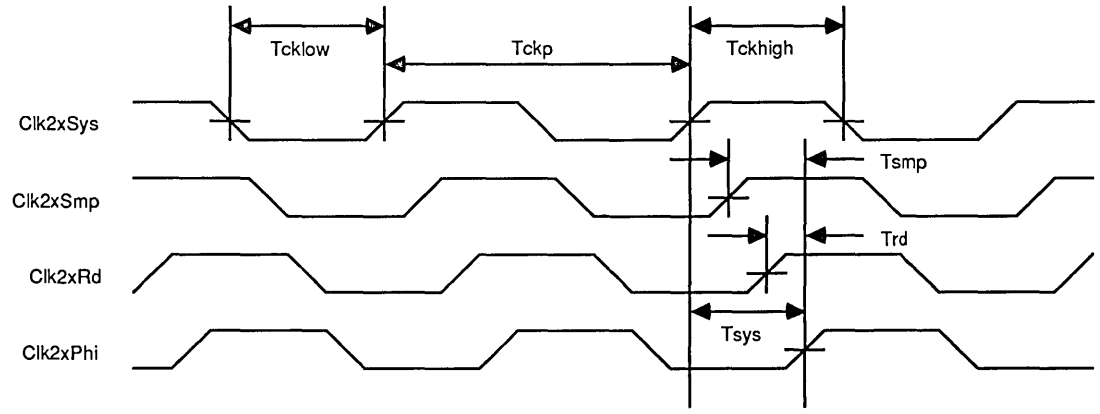
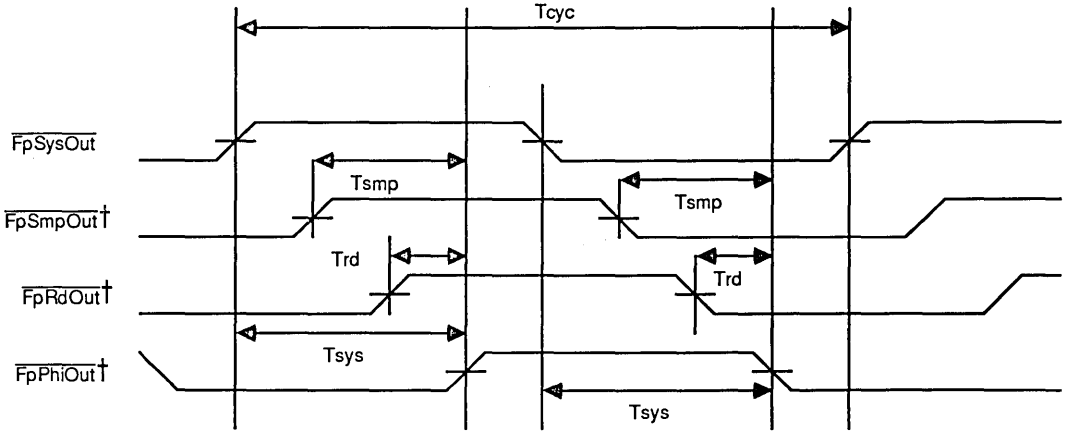


Figure 6. Input "2x" Clock Timing



†These signals are not actually output from the floating point accelerator. They are drawn to provide a reference for other timing diagrams.

Figure 7. Processor Reference Clock

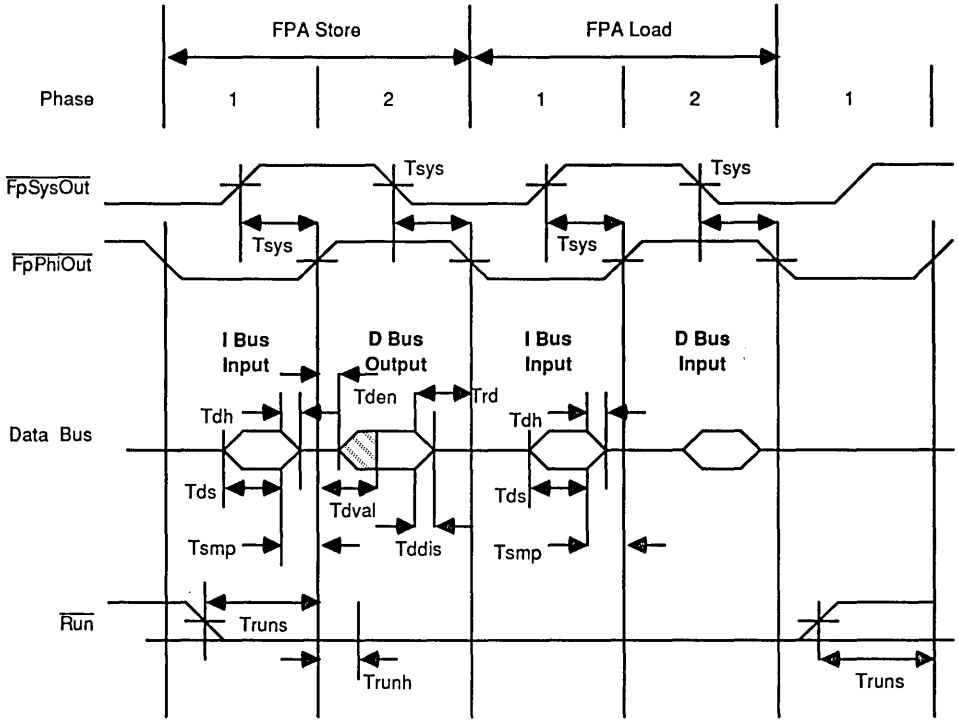


Figure 8. Floating Point Load/Store Timing

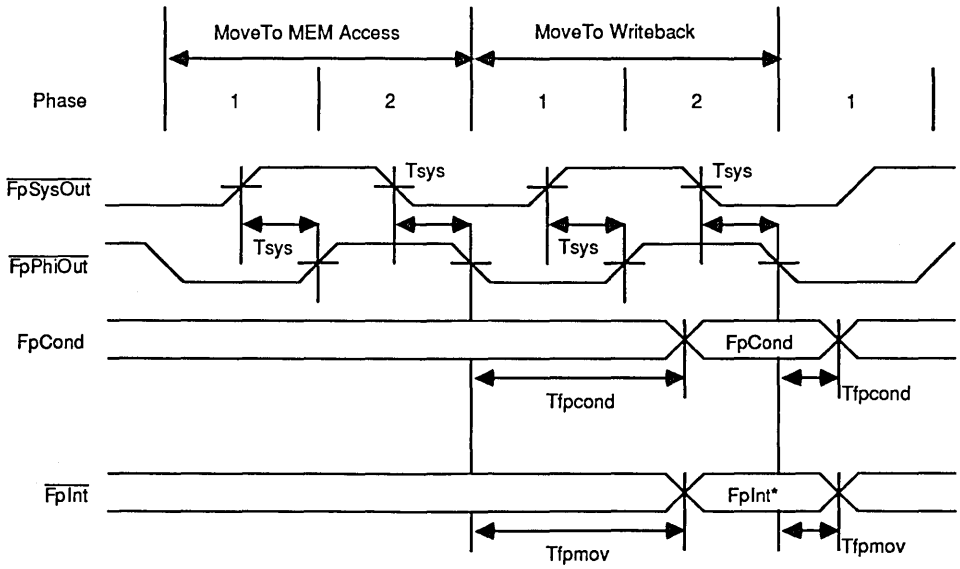


Figure 9. Move to FPC Status Timing

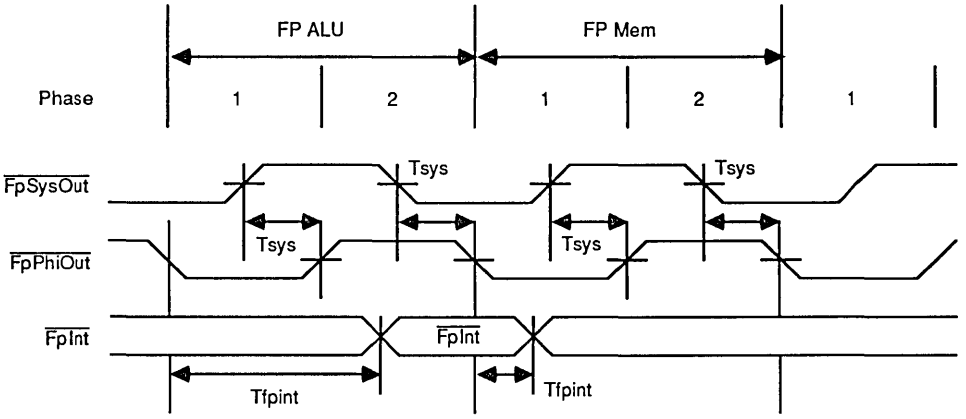


Figure 10. Floating Point Interrupt Timing

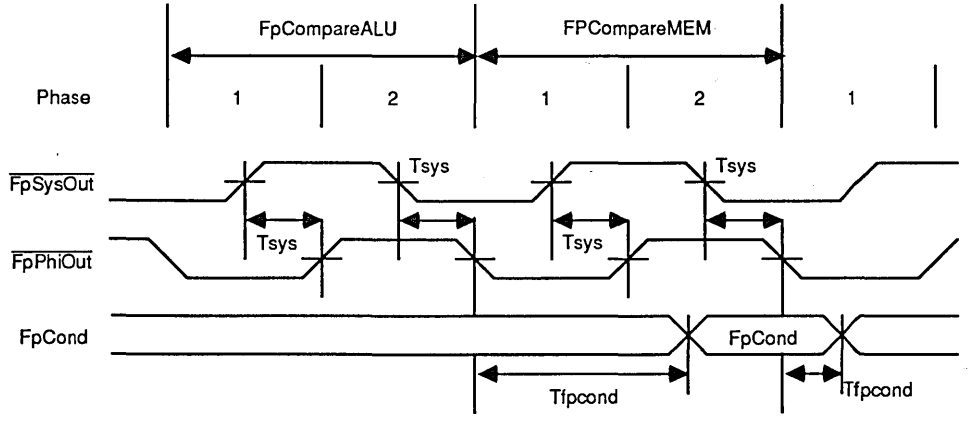


Figure 11. Floating Point Condition Timing

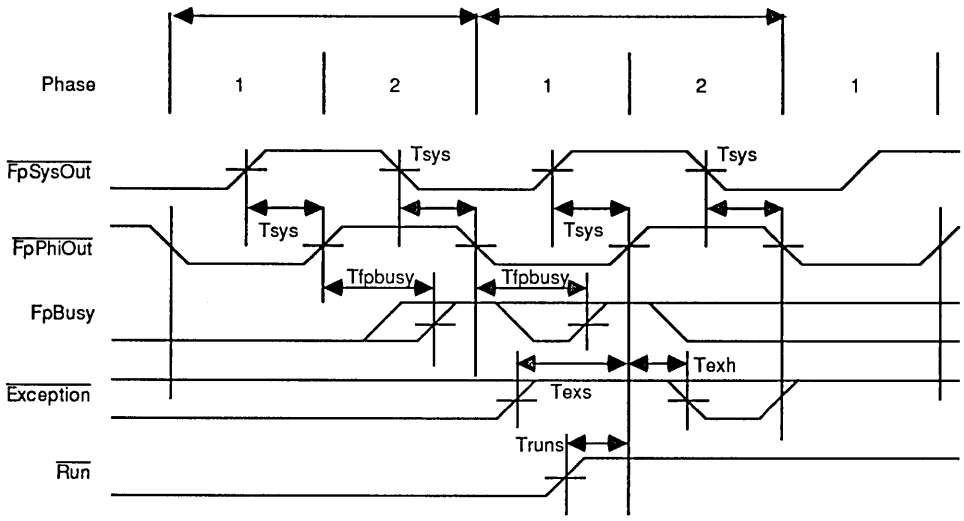


Figure 12. Floating Point Busy, Exception Timing

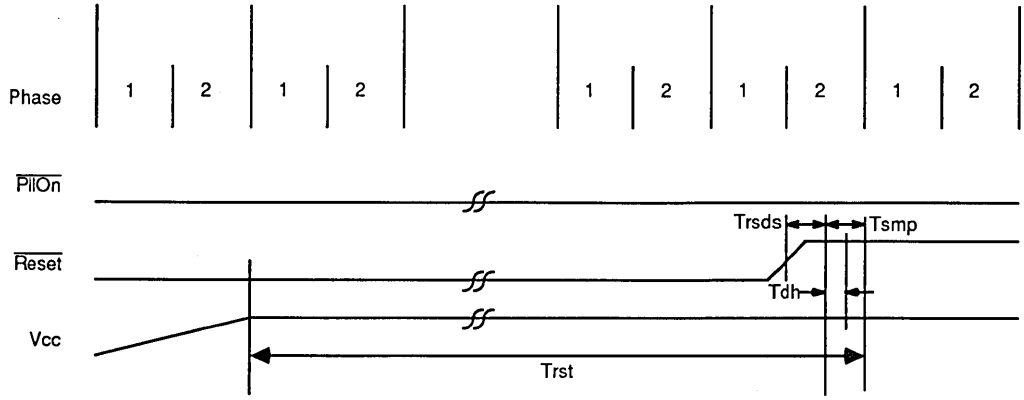
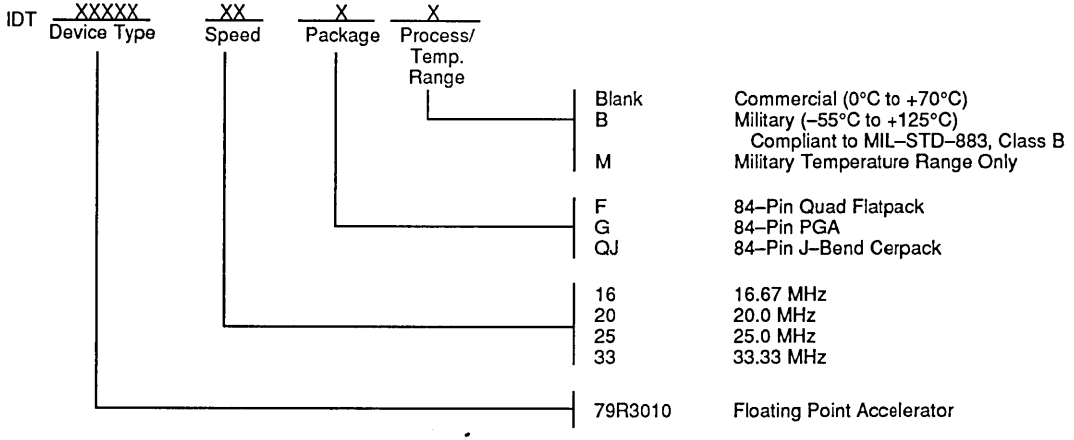


Figure 13. Power-On Reset Timing

ORDERING INFORMATION



Integrated Device Technology, Inc.

RISC FLOATING-POINT ACCELERATOR (FPA)

IDT79R3010A
IDT79R3010AE

FEATURES:

- Hardware Support of Single- and Double-Precision Operations:
  - Floating-Point Add
  - Floating-Point Subtract
  - Floating-Point Multiply
  - Floating-Point Divide
  - Floating-Point Comparisons
  - Floating-Point Conversions
- Sustained performance:
  - 11 MFLOPS single precision LINPACK
  - 7.3 MFLOPS double precision LINPACK
- 16.7MHz through 40MHz operation
- Direct, high-speed interface with IDT79R3000 Processor
- Supports Full Conformance With IEEE 754–1985 Floating-Point Specification
- Full 64-bit operation using sixteen 64-bit data registers
- High-speed CEMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- 32-bit status/control register providing access to all IEEE-Standard exception handling
- Load/store architecture allows data movement directly between FPA and memory or between CPU and FPA
- Overlapped operation of independent floating point ALUs
- Fully pin–compatible with IDT79R3010/IDT79R3010L

DESCRIPTION:

The IDT79R3010A Floating-Point Accelerator (FPA) operates in conjunction with the IDT79R3000A Processor and extends the IDT79R3000A's instruction set to perform arithmetic operations on values in floating-point representations. The IDT79R3010A FPA, with associated system software, fully conforms to the requirements of ANSI/IEEE Standard 754–1985, "IEEE Standard for Binary Floating-Point Arithmetic." In addition, the architecture fully supports the standard's recommendations.

This data sheet provides an overview of the features and architecture of the 79R3010A FPA. A more detailed description of the operation of the device is incorporated in the "R3000A Family Hardware User's Manual", and a more detailed architectural overview is provided in the "mips RISC Architecture" book, both available from IDT.

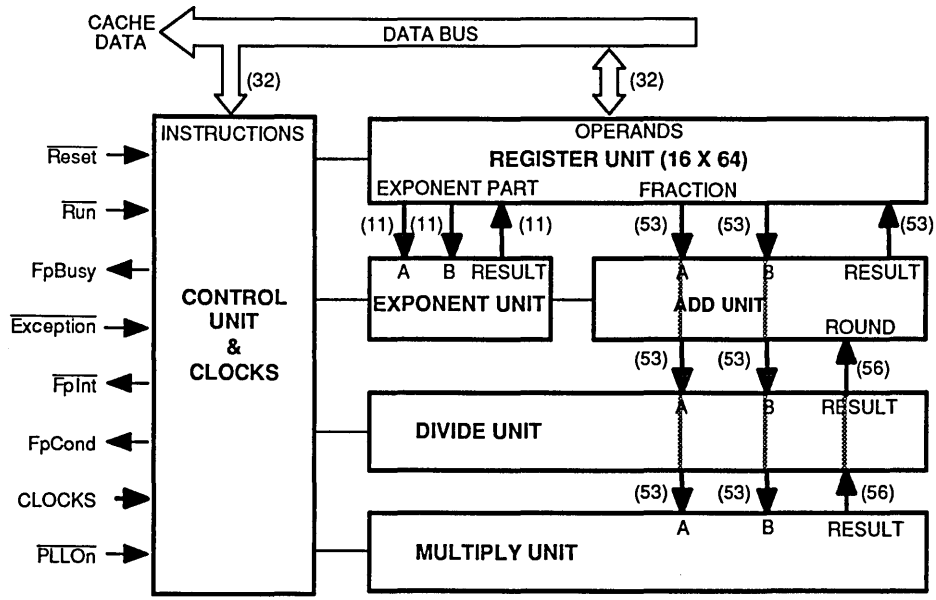


Figure 1. IDT79R3010A Functional Block Diagram

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IDT79R3010A FPA REGISTERS

The IDT79R3010A FPA provides 32 general purpose 32-bit registers, a Control/Status register, and a Revision Identification register. The tightly-coupled coprocessor interface causes the register resources of the FPA to appear to the systems programmers as an extension of the CPU internal registers. The FPA registers are shown in Figure 2.

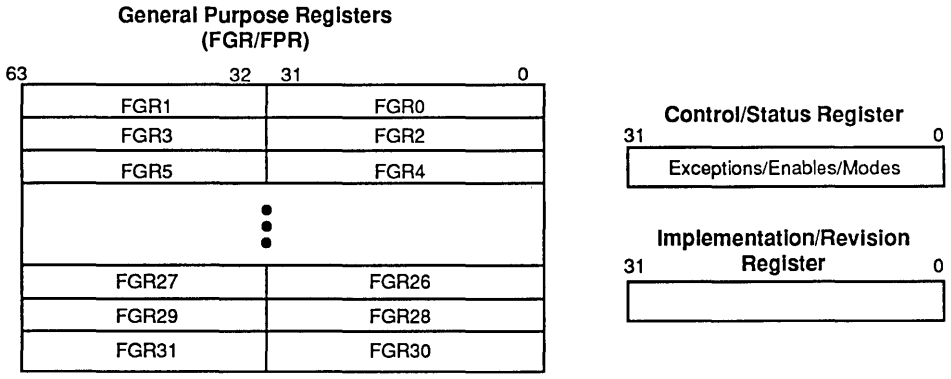


Figure 2. IDT79R3010A FPA Registers

Floating-point coprocessor operations reference three types of registers:

- Floating-Point Control Registers (FCR)
- Floating-Point General Registers (FGR)
- Floating-Point Registers (FPR)

Floating-Point General Registers (FGR)

There are 32 Floating-Point General Registers (FGR) on the FPA. They represent directly-addressable 32-bit registers, and can be accessed by Load, Store, or Move Operations.

Floating-Point Registers (FPR)

The 32 FGRs described in the preceding paragraph are also used to form sixteen 64-bit Floating-Point Registers (FPR). Pairs of general registers (FGRs), for example FGR0 and FGR1 (refer to Figure 2) are physically combined to form a single 64-bit FPR. The FPRs hold a value in either single- or double-precision floating-point format. Double-precision format FPRs are formed from two adjacent FGRs.

Floating-Point Control Registers (FCR)

There are 2 Floating-Point Control Registers (FCR) on the FPA. They can be accessed only by Move operations and include the following:

- Control/Status register, used to control and monitor exceptions, operating modes, and rounding modes;
- Revision register, containing revision information about the FPA.

COPROCESSOR OPERATION

The FPA continually monitors the IDT79R3000A processor instruction stream. If an instruction does not apply to the coprocessor, it is ignored; if an instruction does apply to the coprocessor, the FPA executes that instruction and transfers necessary result and exception data synchronously to the IDT79R3000A main processor.

The FPA performs three types of operations:

- Loads and Stores;
- Moves;
- Two- and three-register floating-point operations.

Load, Store, and Move Operations

Load, Store, and Move operations move data between memory or the IDT79R3000A Processor registers and the IDT79R3010A FPA registers. These operations perform no format conversions and cause no floating-point exceptions. Load, Store, and Move operations reference a single 32-bit word of either the Floating-Point General Registers (FGR) or the Floating-Point Control Registers (FCR).

Floating-Point Operations

The FPA supports the following single- and double-precision format floating-point operations:

- Add
- Subtract
- Multiply
- Divide
- Absolute Value
- Move
- Negate
- Compare

In addition, the FPA supports conversions between single- and double-precision floating-point formats and fixed-point formats.

The FPA incorporates separate Add/Subtract, Multiply, and Divide units, each capable of independent and concurrent operation. Thus, to achieve very high performance, floating point divides can be overlapped with floating point multiplies and floating point additions. These floating point operations occur independently of the actions of the CPU, allowing further overlap of integer and floating point operations. Figure 3 illustrates an example of the types of overlap permissible.

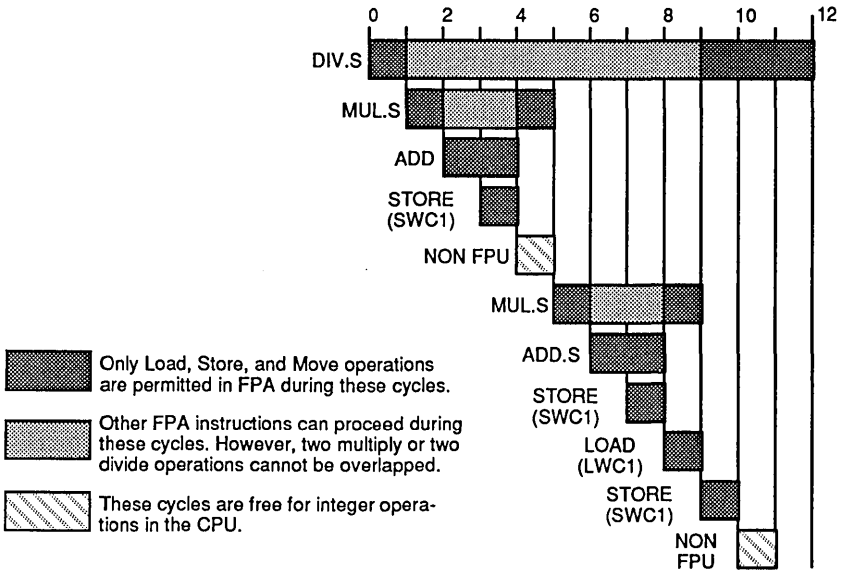


Figure 3. Examples of Overlapping Floating Point Operation

Exceptions

The IDT79R3010A FPA supports all five IEEE standard exceptions:

- Invalid Operation
- Inexact Operation
- Division by Zero
- Overflow
- Underflow

The FPA also supports the optional, Unimplemented Operation exception that allows unimplemented instructions to trap to software emulation routines.

The FPA provides precise exception capability to the CPU; that is, the execution of a floating point operation which generates an exception causes that exception to occur at the CPU instruction which caused the operation. This precise exception capability is a requirement in applications and languages which provide a mechanism for local software exception handlers within software modules.

INSTRUCTION SET OVERVIEW

All IDT79R3010 instructions are 32 bits long and they can be divided into the following groups:

- **Load/Store and Move** instructions move data between memory, the main processor and the FPA general registers.
- **Computational** instructions perform arithmetic operations on floating point values in the FPA registers.
- **Conversion** instructions perform conversion operations between the various data formats.
- **Compare** instructions perform comparisons of the contents of registers and set a condition bit based on the results. The result of the compare operation is output on the FpCond output of the FPA, which is typically used as CpCond1 on the CPU for use in coprocessor branch operations.

Table 1 lists the instruction set of the IDT79R3010A FPA.

OP	Description	OP	Description
	Load/Store/Move Instructions		**Computational Instructions**
LWC1	Load Word to FPA	**ADD.fmt**	Floating–point Add
SWC1	Store Word from FPA	**SUB.fmt**	Floating–point Subtract
MTC1	Move Word to FPA	**MUL.fmt**	Floating–point Multiply
MFC1	Move Word from FPA	**DIV.fmt**	Floating–point Divide
CTC1	Move Control word to FPA	**ABS.fmt**	Floating–point Absolute value
CFC1	Move Control word from FPA	**MOV.fmt**	Floating–point Move
		NEG.fmt	Floating–point Negate
	Conversion Instructions		**Compare Instructions**
CVT.S.fmt	Floating–point Convert to Single FP	**C.cond.fmt**	Floating–point Compare
CVT.D.fmt	Floating–point Convert to Double FP		
CVT.W.fmt	Floating–point Convert to fixed–point		

Table 1. IDT79R3010A Instruction Summary

IDT79R3010 PIPELINE ARCHITECTURE

The IDT79R3010A FPA provides an instruction pipeline that parallels that of the IDT79R3000A processor. The FPA, however, has a 6-stage pipeline instead of the 5-stage pipeline of the IDT79R3000: the additional FPA pipe stage is used to provide efficient coordination of exception responses between the FPA and main processor.

The execution of a single IDT79R3010A instruction consists of six primary steps:

1) **IF**—Instruction Fetch. The main processor calculates the instruction address required to read an instruction from the I-Cache. No action is required of the FPA during this pipe stage since the main processor is responsible for address generation.
2) **RD**—The instruction is present on the data bus during phase 1 of this pipe stage and the FPA decodes the data on the bus to determine if it is an instruction for the FPA.
3) **ALU**—If the instruction is an FPA instruction, instruction execution commences during this pipe stage.
4) **MEM**—If this is a coprocessor load or store instruction, the FPA presents or captures the data during phase 2 of this pipe stage.
5) **WB**—The FPA uses this pipe stage solely to deal with exceptions.
6) **FWB**—The FPA uses this stage to write back ALU results to its register file. This stage is the equivalent of the WB stage in the IDT79R3000A main processor.

Each of these steps requires approximately one FPA cycle as shown in Figure 3 (parts of some operations spill over into another cycle while other operations require only 1/2 cycle).

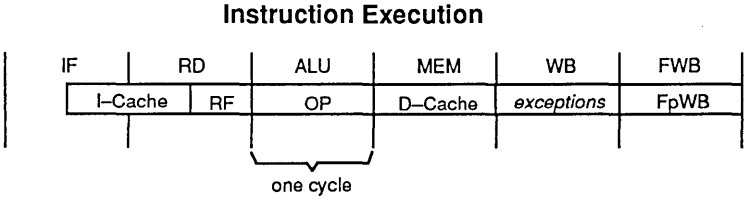


Figure 4. IDT79R3010A Instruction Summary

The IDT79R3010A uses a 6-stage pipeline to achieve an instruction execution rate approaching one instruction per FPA cycle. Thus, execution of six instructions at a time are overlapped as shown in Figure 5.

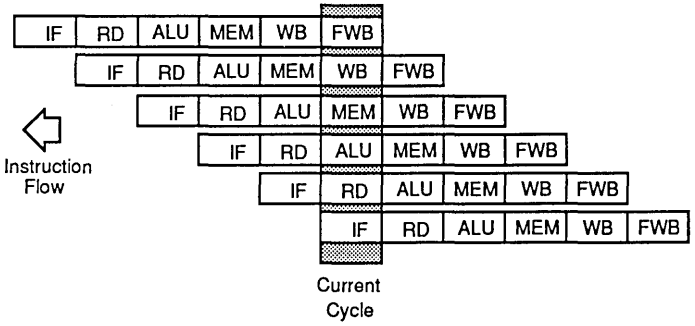


Figure 5. IDT79R3010A Instruction Pipeline

This pipeline operates efficiently because different FPA resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

PACKAGE THERMAL SPECIFICATIONS

The IDT79R3010A utilizes special packaging techniques to improve both the thermal and electrical characteristics of the floating point accelerator.

In order to improve the electrical characteristics of the device, the package is constructed using multiple signal planes, including individual power planes and ground planes to reduce noise associated with high–frequency TTL parts.

In order to improve the thermal characteristics of the floating point accelerator, the device is housed using cavity down packaging for the flatpack and the PGA (the J–bend CerQuad is cavity up). In addition, these packages incorporate a copper–tungsten thermal slug designed to efficiently transfer heat from the die to the case of the package, and thus effectively lower the thermal resistance of the package. The use of an additional external heat sink affixed to the package thermal slug further decreases the effective thermal resistance of the package.

The case temperature may be measured in any environment to determine whether the device is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the package cavity (the package cavity is the side where the package lid is mounted).

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient (θ_{ca}) for the given package. The following equation relates ambient and case temperature:

$$T_A = T_C - P * \theta_{ca}$$

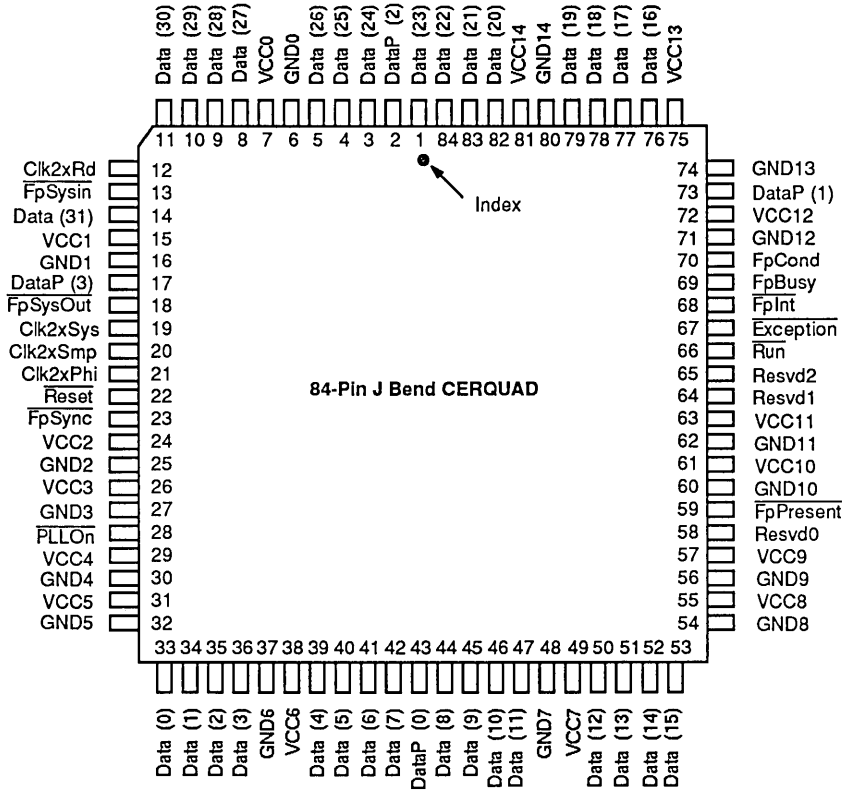
where P is the maximum power consumption, calculated by using the maximum Icc from the DC Electrical Characteristics section.

Typical values for θ_{ca} at various airflows are shown in table 2 for the various CPU packages.

	Airflow - (ft/min)					
	0	200	400	600	800	1000
Øca (84–PGA)	22	8	3	2	1.5	1.0
Øca (84–Flatpack)	22	9	4	3	2	1.5
Øca (84–CerQuad)	25	17	12	8	7	6

Table 2. Thermal Resistance (Øca) at Various Airflows

PIN CONFIGURATION
(Top View)



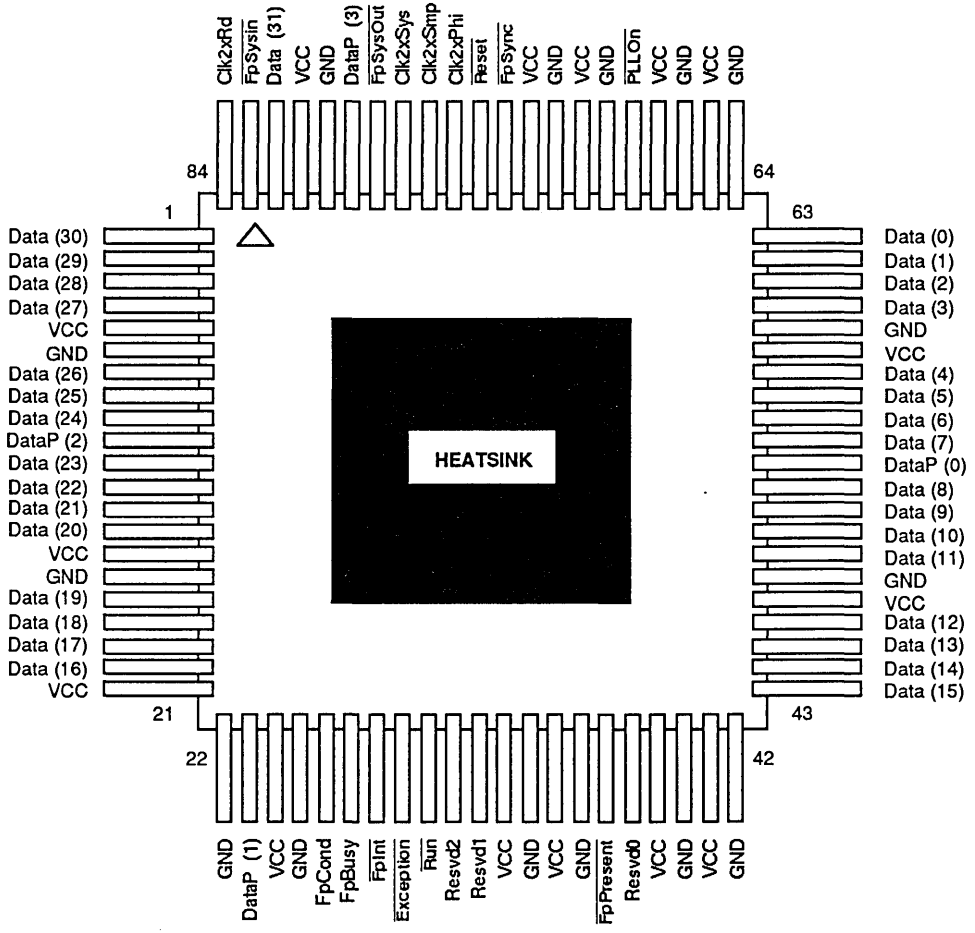
Note:
Reserved pins must not be connected.

PIN CONFIGURATION
(Ceramic, Cavity Down)— BOTTOM VIEW

	1	2	3	4	5	6	7	8	9	10	11	12
M	Vss	Vcc	Data 17	DataP 1	Vss	FP Cond	$\overline{\text{FPInt}}$	Vss	$\overline{\text{Run}}$	Rsrvd 1	Vcc	Vss
L	Data 21	Data 20	Data 18	Data 16	Vcc	FPBusy	Excep-tion	Vcc	Rsrvd 2	$\overline{\text{FP}}$ Present	Data 15	Data 14
K	Vss	Vcc	Data 19							Rsrvd 0	Vcc	Vss
J	Data 23	Data 22									Data 13	Data 12
H	Data 24	DataP 2									Data 11	Data 10
G	Data 26	Data 25				84–Pin Ceramic Pin Grid Array					Vcc	Vss
F	Vss	Vcc									Data 8	Data 9
E	Data 27	Data 28									Data 7	DataP 0
D	Data 29	Data 30									Data 5	Data 6
C	Vss	Vcc	Clk2x Rd							Data 2	Vcc	Vss
B	$\overline{\text{Fp}}$ SysIn	Data 31	DataP 3	Vcc	Clk2x Sys	Vcc	Clk2x Phi	Vcc	$\overline{\text{PllOn}}$	Data 1	Data 3	Data 4
A	Vss	Vcc	$\overline{\text{FpSys}}$ Out	Vss	Clk2x Smp	Vss	$\overline{\text{Reset}}$	Vss	$\overline{\text{FP}}$ Sync	Data 0	Vcc	Vss

NOTE:
1. Reserved pins must not be connected.

PIN CONFIGURATION
84–L QUAD FLATPACK (CAVITY DOWN)
TOP VIEW



NOTE:
1. Reserved pins must not be connected.

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
Data (0–31)	I/O	A multiplexed 32-bit bus used for instruction and data transfers on phase 1 and phase 2, respectively.
DataP (0–3)	O	A 4-bit bus containing even parity over the data bus. Parity is generated by the FPA on stores.
$\overline{\text{Run}}$	I	Input to the FPA which indicates whether the processor-coprocessor system is in the run or stall state.
$\overline{\text{Exception}}$	I	Input to the FPA which indicates exception related status information.
FpBusy	O	Signal to the CPU indicating a request for a coprocessor busy stall.
FpCond	O	Signal to the CPU indicating the result of the last comparison operation.
$\overline{\text{FpInt}}$	O	Signal to the CPU indicating that a floating-point exception has occurred for the current FPA instruction.
$\overline{\text{Reset}}$	I	Synchronous initialization input used to distinguish the processor-FPA synchronization period from the execution period. $\overline{\text{Reset}}$ must be synchronized by the leading edge of $\overline{\text{SysOut}}$ from the CPU.
$\overline{\text{PllOn}}$	I	Input which during the reset period determines whether the phase lock mechanism is enabled and during the execution period determines the output timing model.
$\overline{\text{FpPresent}}$	O	Output which is pulled to ground through an impedance of approximately 0.5k ohms. By providing an external pullup on this line, an indication of the presence or absence of the FPA can be obtained.
Clk2xSys	I	A double frequency clock input used for generating $\overline{\text{FpSysOut}}$.
Clk2xSmp	I	A double frequency clock input used to determine the sample point for data coming into the FPA.
Clk2xRd	I	A double frequency clock input used to determine the disable point for the data drivers.
Clk2xPhi	I	A double frequency clock input used to determine the position of the internal phases, phase 1 and phase 2.
$\overline{\text{FpSysOut}}$	O	Synchronization clock from the FPA.
$\overline{\text{FpSysIn}}$	I	Input used to receive the synchronization clock from the FPA.
$\overline{\text{FpSync}}$	I	Input used to receive the synchronization clock from the CPU.

ABSOLUTE MAXIMUM RATINGS[1, 3]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A, T_C	Operating Temperature	0 to +70[4, 5]	–55 to +125 (Case)	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature[2]	–55 to +125	–65 to +150	°C
V_{IN}	Input Voltage	–0.5 to +7.0	–0.5 to +7.0	V

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –3.0V for pulse width less than 15ns.
   V_{IN} should not exceed V_{CC} +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.
4. 16–33MHz Only, 0 to +70 (Ambient)
5. 37–40MHz Only, 0 to +70 (Case)

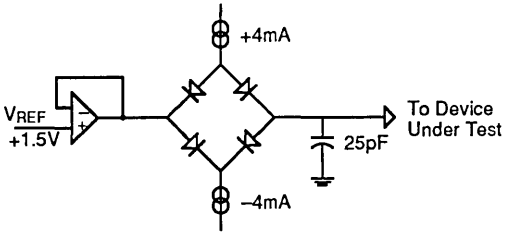
AC TEST CONDITIONS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{IH}	Input HIGH Voltage	3.0	—	V
V_{IL}	Input LOW Voltage	—	0.4	V
V_{IHS}	Input HIGH Voltage	3.5	—	V
V_{ILS}	Input LOW Voltage	—	0.4	V
V_{IHC}	Input HIGH Voltage	4.0	—	V
V_{ILC}	Input LOW Voltage	—	0.4	V

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	TEMPERATURE	GND	V_{CC}
Military	–55°C to +125°C (Case)	0V	5.0 ± 10%
Commercial 16–33MHz	0°C to +70°C (Ambient)	0V	5.0 ± 5%
Commercial 37–40MHz	0°C to +70°C (Case)	0V	5.0 ± 5%

OUTPUT LOADING FOR AC TESTING



DC ELECTRICAL CHARACTERISTICS FOR IDT79R3010A — COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0 V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67 MHz		20.0 MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4mA	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min, I_{OL} = 1.5mA	—	0.5	—	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,6)		3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	—	0.4	V
V_{IHC}	Input HIGH Voltage(4,6)		4.0	—	4.0	—	V
V_{ILC}	Input LOW Voltage(1,4)		—	0.4	—	0.4	V
C_{IN}	Input Capacitance(7)		—	10	—	10	pF
C_{OUT}	Output Capacitance(7)		—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5.0V, T_A = 70°C	—	525	—	600	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	–10	10	–10	10	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–10	10	–10	10	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–40	40	–40	40	µA

DC ELECTRICAL CHARACTERISTICS FOR IDT79R3010AE — COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0 V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	25.0 MHz		33.33MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4mA	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min, I_{OL} = 1.5mA	—	0.5	—	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,6)		3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	—	0.4	V
V_{IHC}	Input HIGH Voltage(4,6)		4.0	—	4.0	—	V
V_{ILC}	Input LOW Voltage(1,4)		—	0.4	—	0.4	V
C_{IN}	Input Capacitance(7)		—	10	—	10	pF
C_{OUT}	Output Capacitance(7)		—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5.0V, T_A = 70°C	—	650	—	700	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	–10	10	–10	10	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–10	10	–10	10	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–40	40	–40	40	µA

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5V for longer periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, $\overline{\text{FpSysIn}}$, $\overline{\text{FpSync}}$ and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{IHC} and V_{ILC} apply to $\overline{\text{Run}}$, $\overline{\text{PllOn}}$ and $\overline{\text{Exception}}$.
5. V_{OLFP} applies to the $\overline{\text{FPPresent}}$ pin only.
6. V_{IH} and V_{IHS} should not be held above V_{CC} + 0.5 Volts.
7. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS FOR IDT79R3010AE — COMMERCIAL TEMPERATURE RANGE (T_C = 0°C to +70°C, V_{CC} = +5.0 V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	37MHz		40MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4mA	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min, I_{OL} = 1.5mA	—	0.5	—	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,6)		3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	—	0.4	V
V_{IHC}	Input HIGH Voltage(4,6)		4.0	—	4.0	—	V
V_{ILC}	Input LOW Voltage(1,4)		—	0.4	—	0.4	V
C_{IN}	Input Capacitance(7)		—	10	—	10	pF
C_{OUT}	Output Capacitance(7)		—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5.0V, T_A = 70°C	—	725	—	750	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	–10	10	–10	10	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–10	10	–10	10	µA
I_{OZ}	Output Tri–state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–40	40	–40	40	µA

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5V for longer periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, $\overline{\text{FpSysIn}}$, $\overline{\text{FpSync}}$ and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{IHC} and V_{ILC} apply to $\overline{\text{Run}}$, $\overline{\text{PllOn}}$ and $\overline{\text{Exception}}$.
5. V_{OLFP} applies to the $\overline{\text{FPPresent}}$ pin only.
6. V_{IH} and V_{IHS} should not be held above V_{CC} + 0.5 Volts.
7. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS FOR IDT79R3010A — MILITARY TEMPERATURE RANGE (T_C = −55°C to +125°C, V_{CC} = +5.0 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67 MHz		20.0 MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −4mA	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min, I_{OL} = 1.5mA	—	0.5	—	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,6)		3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	—	0.4	V
V_{IHC}	Input HIGH Voltage(4,6)		4.0	—	4.0	—	V
V_{ILC}	Input LOW Voltage(1,4)		—	0.4	—	0.4	V
C_{IN}	Input Capacitance(7)		—	10	—	10	pF
C_{OUT}	Output Capacitance(7)		—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5.0V, T_A = 70°C	—	575	—	650	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	−10	10	−10	10	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	−10	10	−10	10	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	−40	40	−40	40	µA

DC ELECTRICAL CHARACTERISTICS FOR IDT79R3010AE — MILITARY TEMPERATURE RANGE (T_C = −55°C to +125°C, V_{CC} = +5.0 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	25.0 MHz		33.33MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −4mA	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min, I_{OL} = 1.5mA	—	0.5	—	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,6)		3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	—	0.4	V
V_{IHC}	Input HIGH Voltage(4,6)		4.0	—	4.0	—	V
V_{ILC}	Input LOW Voltage(1,4)		—	0.4	—	0.4	V
C_{IN}	Input Capacitance(7)		—	10	—	10	pF
C_{OUT}	Output Capacitance(7)		—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5.0V, T_A = 70°C	—	700	—	750	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	−10	10	−10	10	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	−10	10	−10	10	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	−40	40	−40	40	µA

NOTES:

1. V_{IL} Min. = −3.0V for pulse width less than 15ns. V_{IL} should not fall below −0.5V for longer periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, $\overline{\text{FpSysIn}}$, $\overline{\text{FpSync}}$ and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{IHC} and V_{ILC} apply to $\overline{\text{Run}}$, $\overline{\text{PllOn}}$ and $\overline{\text{Exception}}$.
5. V_{OLFP} applies to the $\overline{\text{FPPresent}}$ pin only.
6. V_{IH} and V_{IHS} should not be held above V_{CC} + 0.5 Volts.
7. Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3010A — (1, 3)
COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0 V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	UNIT
Clock							
T_{CkHigh}	Input Clock High(2)	Note 7	12	—	10	—	ns
T_{CkLow}	Input Clock Low(2)	Note 7	12	—	10	—	ns
T_{CkP}	Input Clock Period		30	1000	25	1000	ns
	Clk2xSys to Clk2xSmp(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		9	tcyc/4	7	tcyc/4	ns
Timing Parameters							
T_{DEn}	Data Enable(3)		—	–2	—	–2	ns
T_{DDis}	Data Disable(3)		—	–1	—	–1	ns
T_{DVal}	Data Valid	Load = 25pF	—	3	—	3	ns
T_{RSDS}	Reset Set–up		15	—	15	—	ns
T_{DS}	Data Set–up		9	—	8	—	ns
T_{DH}	Data Hold(3)		–2.5	—	–2.5	—	ns
T_{FpCond}	Fp Condition		—	35	—	30	ns
T_{FpBusy}	Fp Busy		—	15	—	13	ns
T_{FpInt}	Fp Interrupt		—	40	—	35	ns
T_{FpMov}	Fp Move To		—	35	—	30	ns
T_{RExS}	Exception Set–up (Run Cycle)		14	—	12	—	ns
T_{SExS}	Exception Set–up (Stall Cycle)		12	—	10	—	ns
T_{ExH}	Exception Hold		0	—	0	—	ns
T_{RunS}	Run Set–up		17	—	15	—	ns
T_{RunH}	Run Hold		–2	—	–2	—	ns
T_{StallS}	Stall Set–up		10	—	10	—	ns
T_{StallH}	Stall Hold		–2	—	–2	—	ns
Reset Initialization							
T_{rstPLL}	Reset Timing, Phase–lock on(4, 5)		3000	—	3000	—	Tcyc
T_{rst}	Reset Timing, Phase–lock off(5)		128	—	128	—	Tcyc
Capacitive Load Deration							
CLD	Load Derate(6)		0.5	2	0.5	1	ns/25pF

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. With $\overline{\text{PllOn}}$ asserted, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. No two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 5ns.

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3010AE — (1, 3)
COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0 V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION	25.0 MHz MIN.	25.0 MHz MAX.	33.33 MHz MIN.	33.33 MHz MAX.	UNIT
Clock							
T_{CkHigh}	Input Clock High(2)	Note 7	8	—	6	—	ns
T_{CkLow}	Input Clock Low(2)	Note 7	8	—	6	—	ns
T_{CkP}	Input Clock Period		20	1000	15	1000	ns
	Clk2xSys to Clk2xSmp(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		5	tcyc/4	3.5	tcyc/4	ns
Timing Parameters							
T_{DEn}	Data Enable(3)		—	–1.5	—	–1	ns
T_{DDis}	Data Disable(3)		—	–0.5	—	–0.5	ns
T_{DVal}	Data Valid	Load = 25pF	—	2	—	2	ns
T_{RSDS}	Reset Set–up		10	—	10	—	ns
T_{DS}	Data Set–up		6	—	4.5	—	ns
T_{DH}	Data Hold(3)		–2.5	—	–2.5	—	ns
T_{FpCond}	Fp Condition		—	25	—	17	ns
T_{FpBusy}	Fp Busy		—	10	—	7	ns
T_{FpInt}	Fp Interrupt		—	25	—	18	ns
T_{FpMov}	Fp Move To		—	25	—	16	ns
T_{RExS}	Exception Set–up (Run Cycle)		11	—	9	—	ns
T_{SExS}	Exception Set–up (Stall Cycle)		8	—	6.5	—	ns
T_{ExH}	Exception Hold		0	—	0	—	ns
T_{RunS}	Run Set–up		15	—	12.5	—	ns
T_{RunH}	Run Hold		–2	—	–1.5	—	ns
T_{StallS}	Stall Set–up		9	—	7	—	ns
T_{StallH}	Stall Hold		–2	—	–2	—	ns
Reset Initialization							
T_{rstPLL}	Reset Timing, Phase–lock on(4, 5)		3000	—	3000	—	Tcyc
T_{rst}	Reset Timing, Phase–lock off(5)		128	—	128	—	Tcyc
Capacitive Load Deration							
CLD	Load Derate(6)		0.5	1	0.5	1	ns/25pF

NOTES:

7. All timings are referenced to 1.5V.
8. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
9. This parameter is guaranteed by design.
10. With $\overline{\text{PllOn}}$ asserted, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
11. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
12. No two signals on a given device will derate for a given load by a difference greater than 15%.
13. Clock transition time < 2.5ns for 33MHz; clock transition time < 5ns for all other speeds.

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3010AE — (1, 3)
COMMERCIAL TEMPERATURE RANGE (T_C = 0°C to +70°C, V_{CC} = +5.0 V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION	37.0 MHz MIN.	37.0 MHz MAX.	40.0 MHz MIN.	40.0 MHz MAX.	UNIT
Clock							
T_{CkHigh}	Input Clock High(2)	Note 7	5.5	—	5.5	—	ns
T_{CkLow}	Input Clock Low(2)	Note 7	5.5	—	5.5	—	ns
T_{CkP}	Input Clock Period		13.5	1000	12.5	1000	ns
	Clk2xSys to Clk2xSmp(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		3.5	tcyc/4	3	tcyc/4	ns
Timing Parameters							
T_{DEn}	Data Enable(3)		—	–1.5	—	–1	ns
T_{DDIs}	Data Disable(3)		—	–0.5	—	–0.5	ns
T_{DVal}	Data Valid	Load = 25pF	—	2	—	2	ns
T_{RSDS}	Reset Set–up		8	—	8	—	ns
T_{DS}	Data Set–up		4.5	—	4	—	ns
T_{DH}	Data Hold(3)		–2.5	—	–2.5	—	ns
T_{FpCond}	Fp Condition		—	17	—	16	ns
T_{FpBusy}	Fp Busy		—	6.5	—	6	ns
T_{FpInt}	Fp Interrupt		—	18	—	17	ns
T_{FpMov}	Fp Move To		—	16	—	16	ns
T_{RExS}	Exception Set–up (Run Cycle)		9	—	8.5	—	ns
T_{SExS}	Exception Set–up (Stall Cycle)		6	—	5.5	—	ns
T_{ExH}	Exception Hold		0	—	0	—	ns
T_{RunS}	Run Set–up		10	—	9	—	ns
T_{RunH}	Run Hold		–2	—	–1.5	—	ns
T_{StallS}	Stall Set–up		6.5	—	6	—	ns
T_{StallH}	Stall Hold		–2	—	–2	—	ns
Reset Initialization							
T_{rstPLL}	Reset Timing, Phase–lock on(4, 5)		3000	—	·3000	—	Tcyc
T_{rst}	Reset Timing, Phase–lock off(5)		128	—	128	—	Tcyc
Capacitive Load Deration							
CLD	Load Derate(6)		0.5	1	0.5	1	ns/25pF

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. With $\overline{\text{PllOn}}$ asserted, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. No two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 2.5ns for 33MHz. Clock transition <5 for 25 MHz.

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3010A — (1, 3)
MILITARY TEMPERATURE RANGE (T_C = –55°C to +125°C, V_{CC} = +5.0 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	UNIT
Clock							
T_{CkHigh}	Input Clock High(2)	Note 7	12	—	10	—	ns
T_{CkLow}	Input Clock Low(2)	Note 7	12	—	10	—	ns
T_{CkP}	Input Clock Period		30	1000	25	1000	ns
	Clk2xSys to Clk2xSmp(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		9	tcyc/4	7	tcyc/4	ns
Timing Parameters							
T_{DEn}	Data Enable(3)		—	–2	—	–2	ns
T_{DDIs}	Data Disable(3)		—	–1	—	–1	ns
T_{DVal}	Data Valid	Load = 25pF	—	3	—	3	ns
T_{RSDS}	Reset Set–up		15	—	15	—	ns
T_{DS}	Data Set–up		9	—	8	—	ns
T_{DH}	Data Hold(3)		–2.5	—	–2.5	—	ns
T_{FpCond}	Fp Condition		—	35	—	30	ns
T_{FpBusy}	Fp Busy		—	15	—	13	ns
T_{FpInt}	Fp Interrupt		—	40	—	35	ns
T_{FpMov}	Fp Move To		—	35	—	30	ns
T_{RExS}	Exception Set–up (Run Cycle)		14	—	12	—	ns
T_{SExS}	Exception Set–up (Stall Cycle)		12	—	10	—	ns
T_{ExH}	Exception Hold		0	—	0	—	ns
T_{RunS}	Run Set–up		17	—	15	—	ns
T_{RunH}	Run Hold		–2	—	–2	—	ns
T_{StallS}	Stall Set–up		10	—	10	—	ns
T_{StallH}	Stall Hold		–2	—	–2	—	ns
Reset Initialization							
T_{rstPLL}	Reset Timing, Phase–lock on(4, 5)		3000	—	3000	—	Tcyc
T_{rst}	Reset Timing, Phase–lock off(5)		128	—	128	—	Tcyc
Capacitive Load Deration							
CLD	Load Derate(6)		0.5	2	0.5	1	ns/25pF

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. With $\overline{\text{PllOn}}$ asserted, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. No two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 5ns.

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3010AE — (1, 3)
MILITARY TEMPERATURE RANGE (T_C = −55°C to +125°C, V_{CC} = +5.0 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	25.0 MHz MIN.	25.0 MHz MAX.	33.33 MHz MIN.	33.33 MHz MAX.	UNIT
Clock							
T_{CkHigh}	Input Clock High(2)	Note 7	8	—	6	—	ns
T_{CkLow}	Input Clock Low(2)	Note 7	8	—	6	—	ns
T_{CkP}	Input Clock Period		20	1000	15	1000	ns
	Clk2xSys to Clk2xSmp(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		5	tcyc/4	3.5	tcyc/4	ns
Timing Parameters							
T_{DEn}	Data Enable(3)		—	−1.5	—	−1	ns
T_{DDIs}	Data Disable(3)		—	−0.5	—	−0.5	ns
T_{DVal}	Data Valid	Load = 25pF	—	2	—	2	ns
T_{RSDS}	Reset Set−up		10	—	10	—	ns
T_{DS}	Data Set−up		6	—	4.5	—	ns
T_{DH}	Data Hold(3)		−2.5	—	−2.5	—	ns
T_{FpCond}	Fp Condition		—	25	—	17	ns
T_{FpBusy}	Fp Busy		—	10	—	7	ns
T_{FpInt}	Fp Interrupt		—	25	—	18	ns
T_{FpMov}	Fp Move To		—	25	—	16	ns
T_{RExS}	Exception Set−up (Run Cycle)		11	—	9	—	ns
T_{SExS}	Exception Set−up (Stall Cycle)		8	—	6.5	—	ns
T_{ExH}	Exception Hold		0	—	0	—	ns
T_{RunS}	Run Set−up		15	—	12.5	—	ns
T_{RunH}	Run Hold		−2	—	−1.5	—	ns
T_{StallS}	Stall Set−up		9	—	7	—	ns
T_{StallH}	Stall Hold		−2	—	−2	—	ns
Reset Initialization							
T_{rstPLL}	Reset Timing, Phase−lock on(4, 5)		3000	—	3000	—	Tcyc
T_{rst}	Reset Timing, Phase−lock off(5)		128	—	128	—	Tcyc
Capacitive Load Deration							
CLD	Load Derate(6)		0.5	1	0.5	1	ns/25pF

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. With $\overline{\text{PllOn}}$ asserted, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. No two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 2.5ns for 33MHz; clock transition time < 5ns for all other speeds.

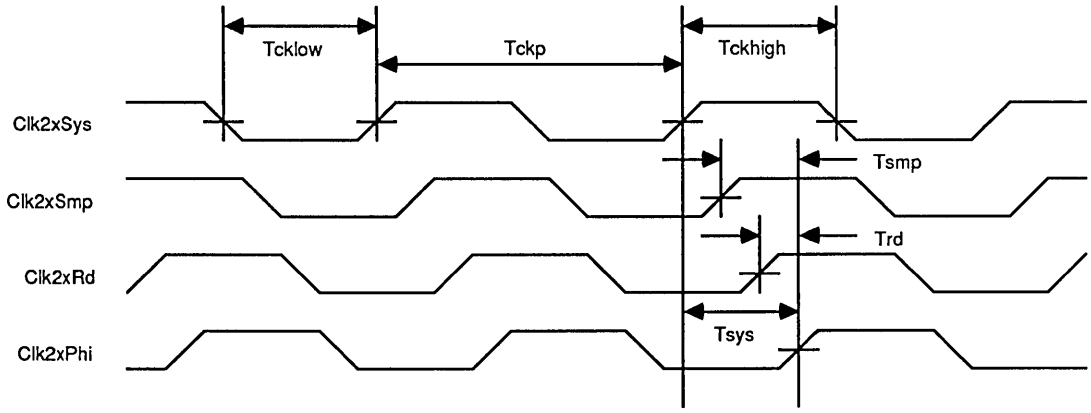
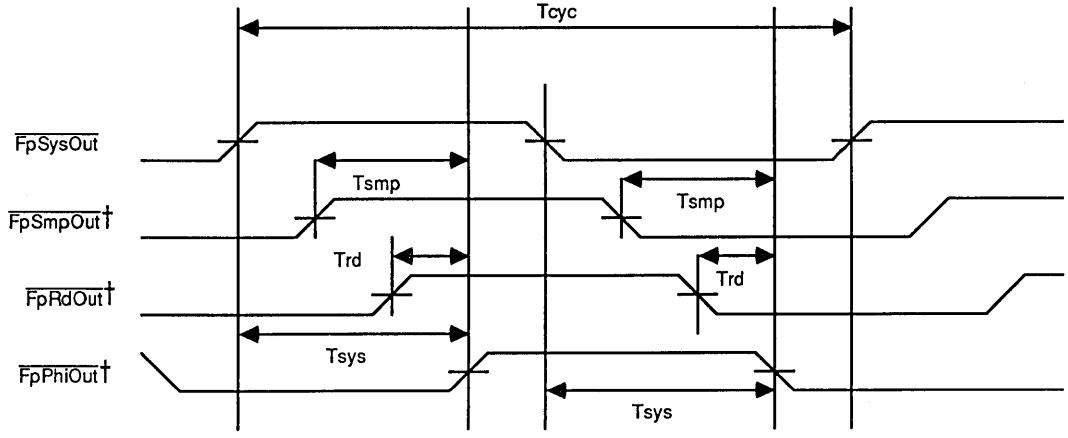


Figure 6. Input "2x" Clock Timing



†These signals are not actually output from the floating point accelerator. They are drawn to provide a reference for other timing diagrams.

Figure 7. Processor Reference Clock

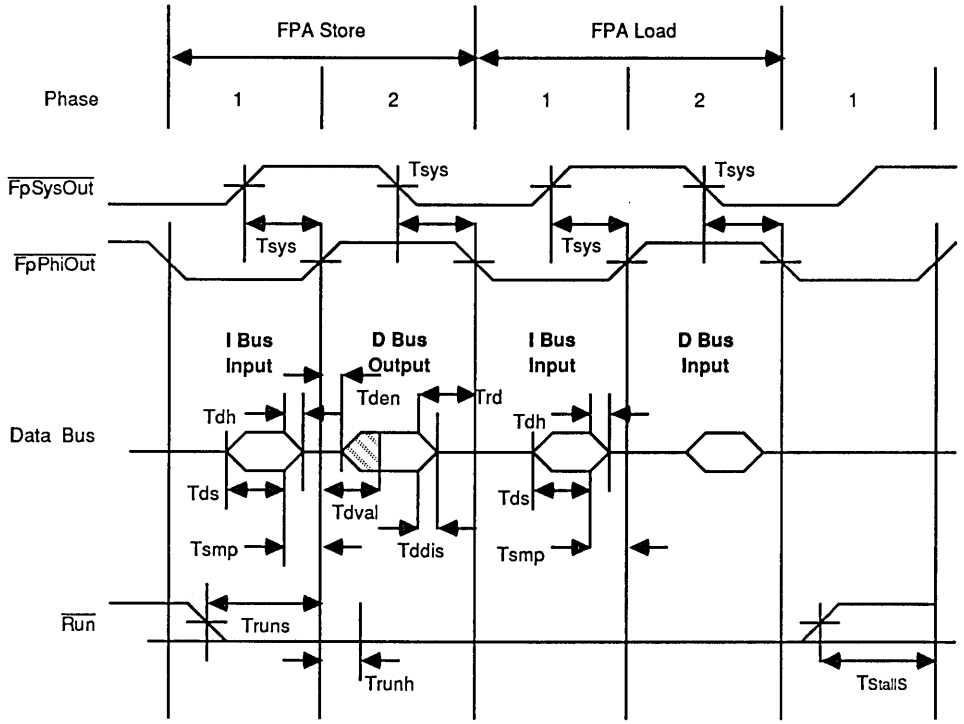


Figure 8. Floating Point Load/Store Timing

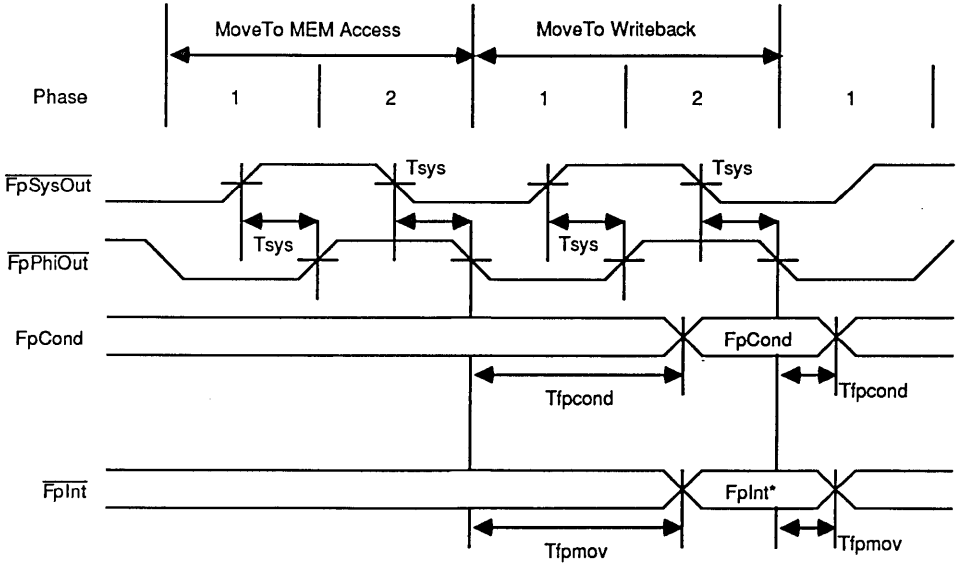


Figure 9. Move to FPC Status Timing

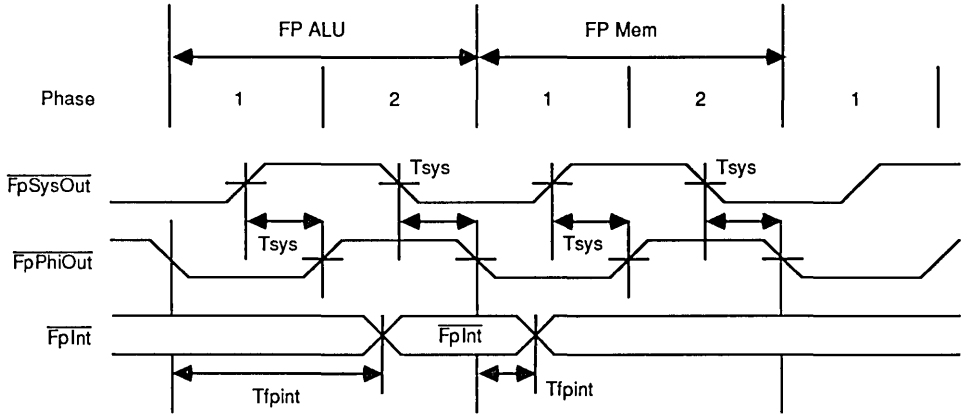


Figure 10. Floating Point Interrupt Timing

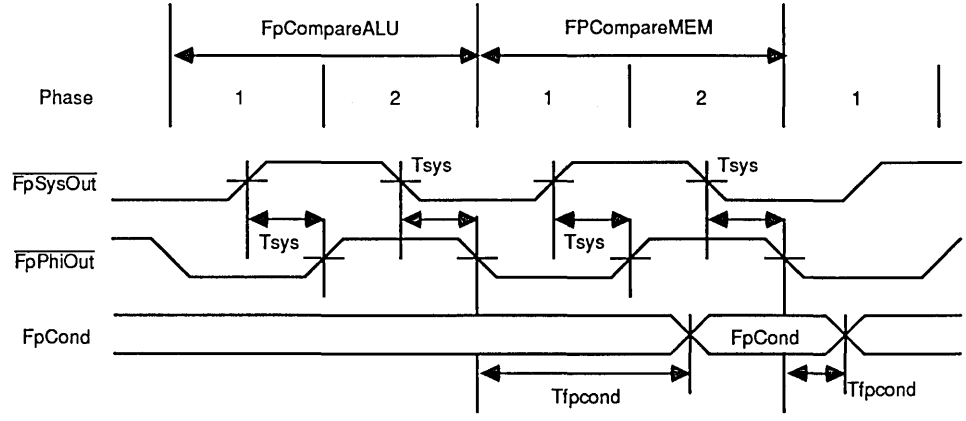


Figure 11. Floating Point Condition Timing

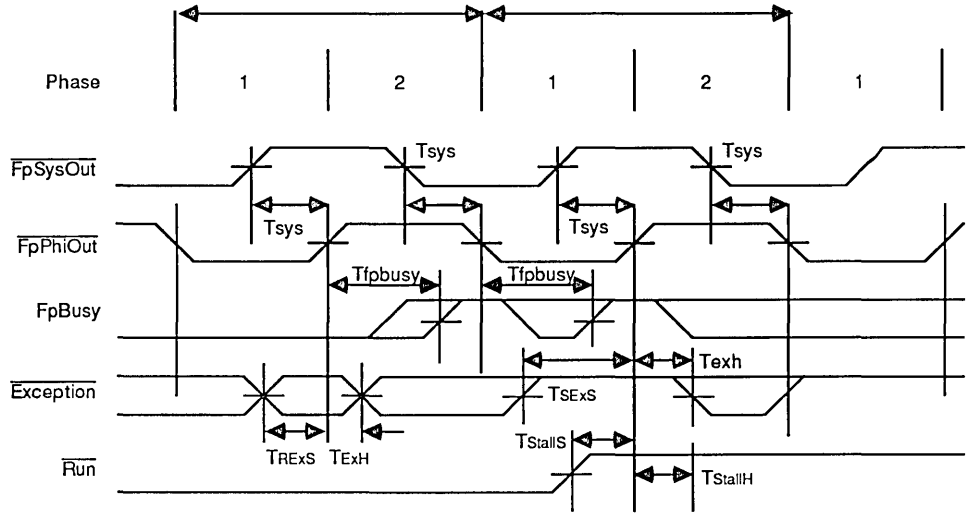


Figure 12. Floating Point Busy, Exception Timing

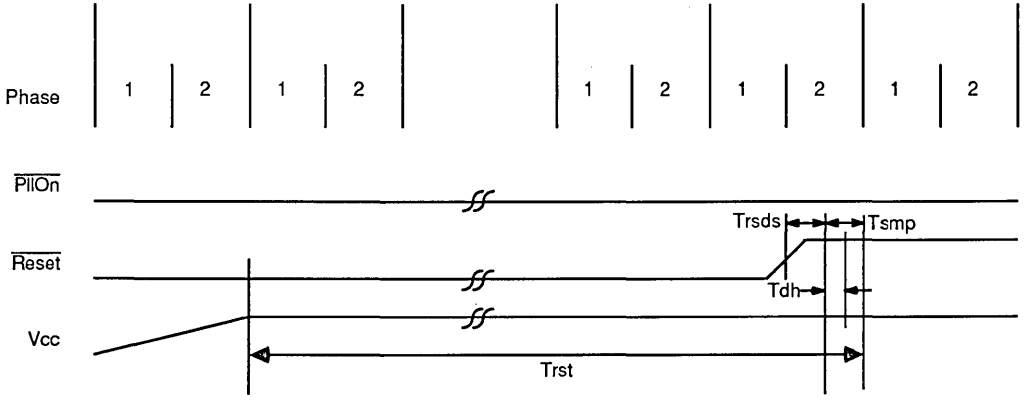
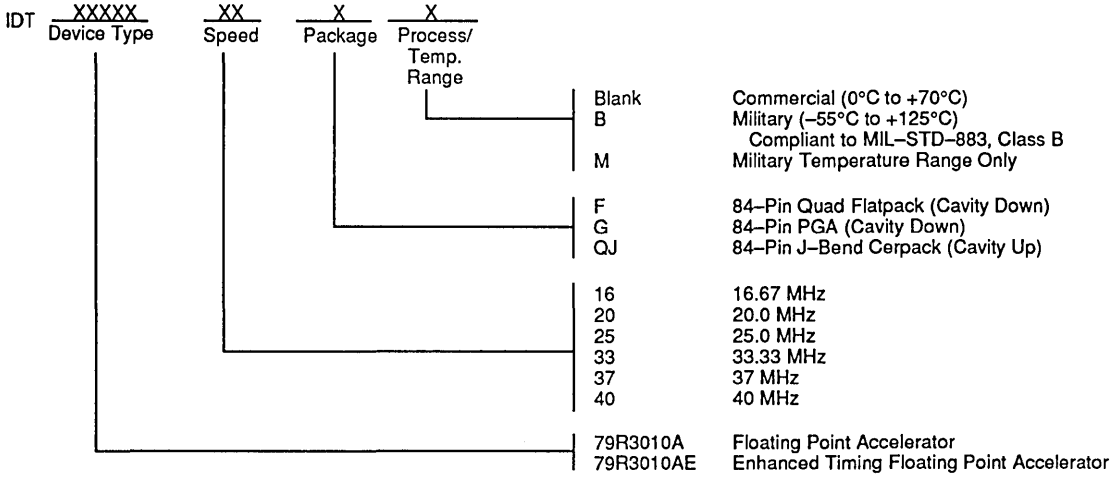


Figure 13. Power-On Reset Timing

ORDERING INFORMATION



Integrated Device Technology, Inc.

RISC CPU WRITE BUFFER

IDT79R3020

FEATURES:

- Temporary storage buffers to enhance the performance of the IDT79R3000 RISC CPU processor
- Allows for write operations by the RISC CPU processor during Run cycles
- Each Write Buffer has four locations to handle an 8-bit address slice and a 9-bit data slice (including a parity bit)
- High-speed CEMOS™ technology
- Pin, functionally and software compatible with the MIPS Computer Systems R2020 Write Buffer
- Speeds from 16.7 to 33.33 MHz
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT79R3020 Write Buffer enhances the performance of IDT79R3000 systems by allowing the processor to perform write operations during Run cycles instead of resorting to time-consuming stall cycles. Each IDT79R3020 device handles an 8-bit slice of address, and a 9-bit slice of data (one parity bit per byte); thus, four IDT79R3020s provide 4-deep buffering of 32 bits of address and 36 bits of data and parity. Figure 1 illustrates the functional position of the Write Buffer in an IDT79R3000 system.

Whenever the processor performs a write operation, the Write Buffer captures the output data and its address (including the access type bits). The Write Buffer can hold up to four data–address sets while it waits to pass the data on to main memory. Transfers from the processor to the write buffers occur synchronously at the cycle rate of the processor and the write buffer signals the processor if it is unable to accept data. The write buffer also provides a set of handshake signals to communicate with a main memory controller and coordinate the transfer of write data to main memory.

The sections that follow describe these IDT79R3020 Write Buffer interfaces:

- the processor-Write Buffer interface
- the Write Buffer-main memory interface
- a miscellaneous, Write Buffer-board control interface.

WRITE BUFFER

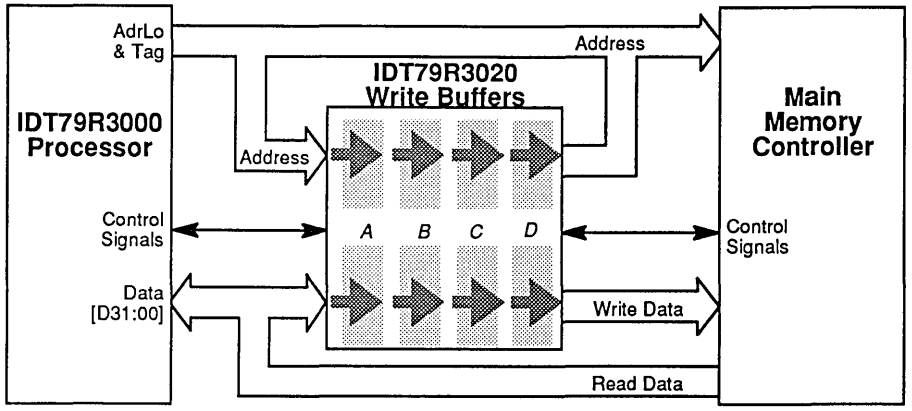


Figure 1. The IDT79R3020 Write Buffer in an IDT79R3000 System

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WRITE BUFFER - IDT79R3000 PROCESSOR INTERFACE

Figure 2 shows the signals comprising the Write Buffer interface to the IDT79R3000 (all descriptions assume that four IDT79R3020 Write Buffers are used to implement a 32-bit, buffered interface). The AdrLo bus and Tag bus bits from the processor are both connected to the Write Buffer to form a 32-bit physical address that is captured by the buffers. Thirty-two bits of data, four bits of parity, and two access type bits are also captured by the Write Buffer. The paragraphs that follow describe the Write Buffer-processor interface signals and the timing of processor-to-Write Buffer data transfers.

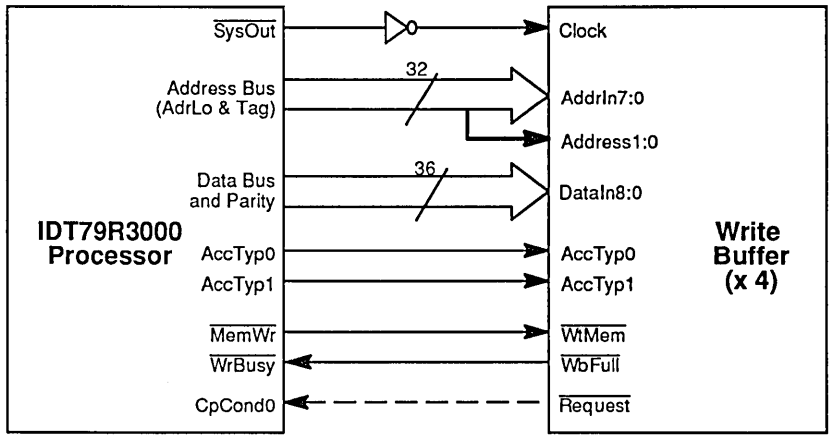


Figure 2. Write Buffer — IDT79R3000 Processor Interface

Write Buffer-Processor Interface Signals

Clock

An inverted version of the IDT79R3000's SysOut signal from the IDT79R3000 processor that synchronizes data transfers. The Write Buffer uses the trailing edge of *Clock* to latch the contents of the AdrLo bus and uses the leading *Clock* edge to latch the contents of the Data and Tag buses.

DataIn8:0

Nine input data lines from the IDT79R3000 processor's Data bus (eight bits of data and one bit of parity).

AddrIn7:0

Eight input address lines from the IDT79R3000 processor. The address lines are taken from the AdrLo and Tag buses.

Address1:0

The two least significant address bits from the IDT79R3000 processor. These two address bits must be connected to all four Write Buffers and are used in conjunction with the access type (*AccTyp1:0*) signals, the *Position1:0* signals, and the *BigEndian* signal to determine which byte(s) in a word are being written into a particular Write Buffer.

AccTypIn1:0

The access type signals from the IDT79R3000 processor specifying the size of a data access: word, tri-byte, half-word, or byte.

WtMem

This input is connected to the MemWr signal from the IDT79R3000 processor that is asserted whenever the processor is performing a store (write) operation.

Request

The primary purpose of this signal is to request access to memory and is described later when the Write Buffer-Main Memory Interface is discussed. The Request signal can also be connected to the CpCond0 input of the IDT79R3000 and can then be tested by software to determine if there is any data in the Write Buffer. Since Request is deasserted if there is no data in the Write Buffer, software can determine if a previous write operation (for example, to an I/O device) has been completed before initiating a read or read status operation from that device.

WbFull

The Write Buffer asserts this signal to the IDT79R3000's WrBusy input whenever it cannot accept any more data; that is, when the current write will fill the buffer or the buffer has all address-data pairs occupied. The IDT79R3000 processor performs a write-busy stall if it needs to store data while the WbFull/WrBusy signal is asserted.

Data & Address Connections

Figure 3 illustrates how four Write Buffers are connected to the address and data outputs of the IDT79R3000 processor.

Address Inputs

Each Write Buffer device has eight address inputs (AdrIn7:0). The four low-order bits (AdrIn3:0) are clocked into the device on the trailing edge of the Clock signal and are taken from the IDT79R3000's AdrLo bus. The four high-order bits (AdrIn7:4) are clocked into the device on the rising edge of the Clock signal and are taken from the IDT79R3000's Tag bus.

Each device also has separate inputs (Address1, Address0) for the two low-order bits from the AdrLo bus. These bits must be input to each device since they comprise the byte pointer. Note in Figure 3 that the two low-order AdrIn inputs (AdrIn1:0) to Write Buffer device 0 are connected to ground since the Address1, Address0 inputs already supply these bits to the device.

Data Inputs

Each Write Buffer device has nine data inputs that are clocked into the device on the leading edge of the Clock signal and are taken from the IDT79R3000's Data bus. In Figure 3, each device captures eight bits of data and one bit of parity. Also note that the data bits assigned to each device correspond to the address bits connected to the device. This arrangement is required since data

selection is dependent on a combination of the AccType signals and the two low order address bits. The arrangement also simplifies system utilization of the "Read Error Address" feature described later.

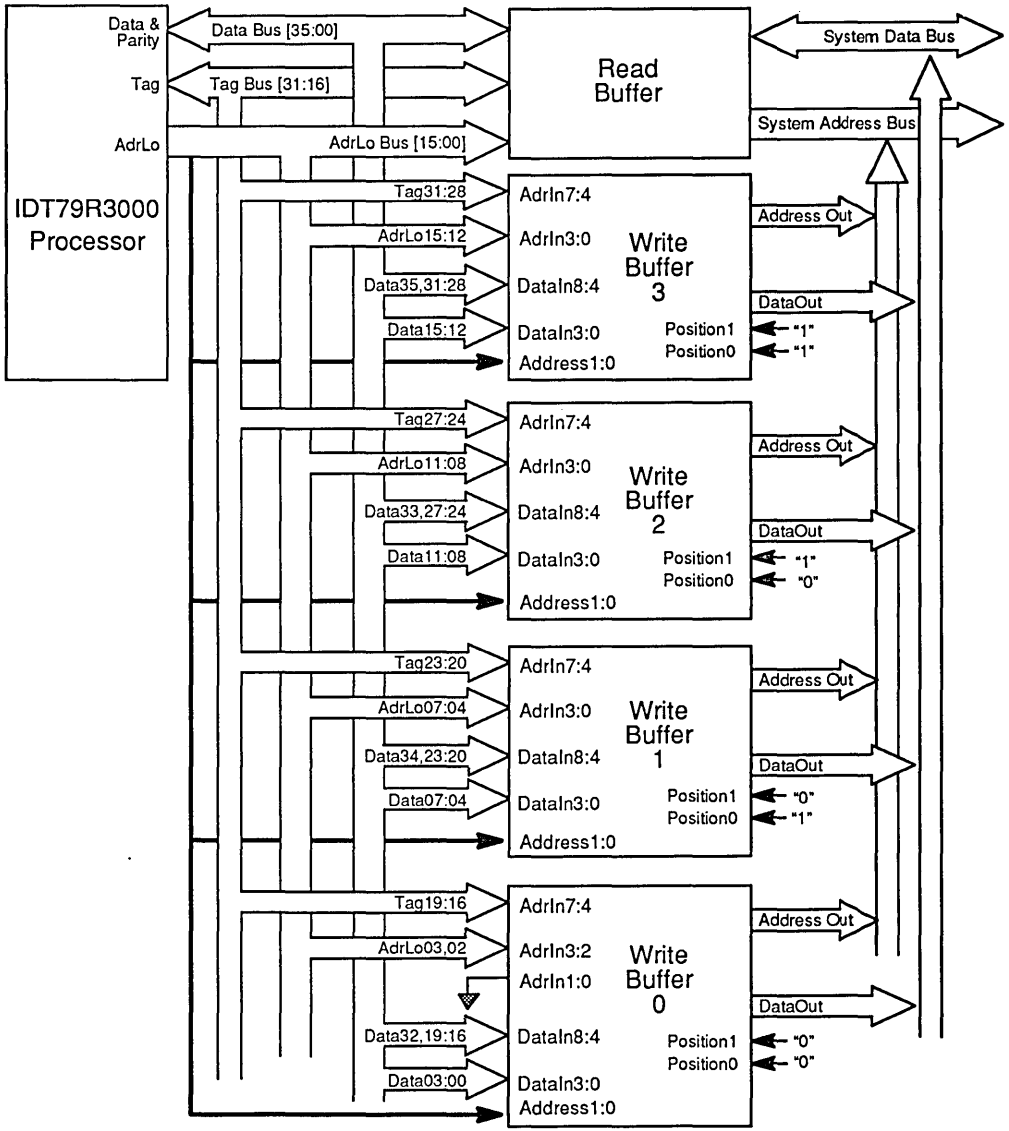


Figure 3. Write Buffer Data and Address Line Connections

The *Position1* and *Position0* signals shown in Figure 3 specify the nibble position within a halfword that each write buffer device comprises.

Write Buffer - Processor Timing

Transfers between the processor and the Write Buffers occur synchronously: the Clock signal from the processor is input to the Write Buffers and used to clock the address and data information into the Write Buffers' latches. Figure 4 illustrates the timing for the processor-Write Buffer interface.

When the $\overline{\text{WrMem}}$ signal is asserted, the low-order address bits, and the Address 1:0 inputs, are latched on the trailing edge of the Clock signal (1). The rising edge of Clock (2) is used to latch the high-order address bits, the access type inputs and the contents of the data bus.

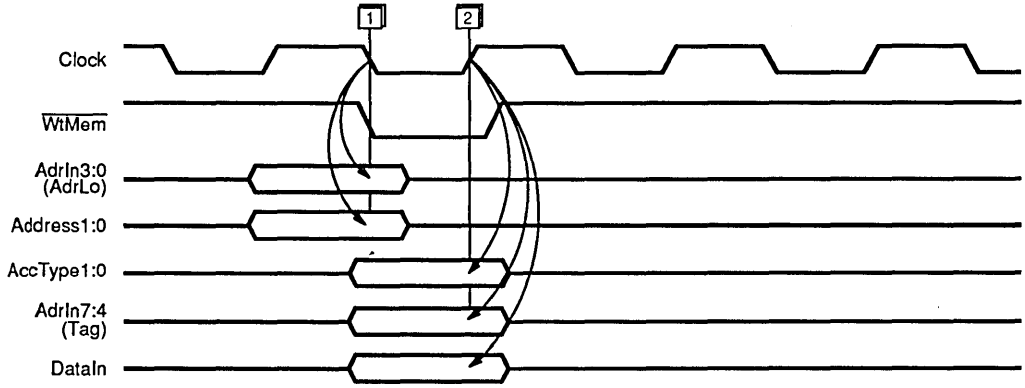


Figure 4. Processor — Write Buffer Interface Timing

WRITE BUFFER - MAIN MEMORY INTERFACE

Figure 5 shows the signals comprising the Write Buffer interface to main memory. This interface is essentially decoupled from the Write Buffer-processor interface: although some synchronization of the memory interface signals and the Clock signal is required, the handshaking signals in this interface have no direct connection to the operation of the Write Buffer-processor interface.

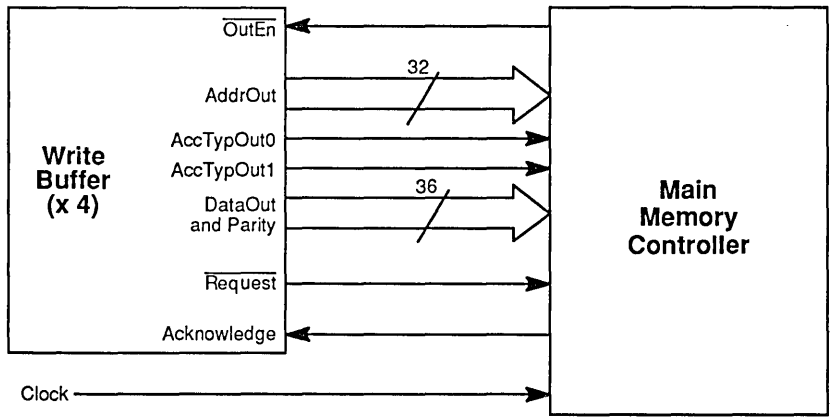


Figure 5. Write Buffer — Main Memory Interface

Write Buffer - Main Memory Interface Signals

Each Write Buffer provides the following signals that comprise the interface to a main memory controller:

AddrOut 7:0

Eight address line output from each Write Buffer.

DataOut 8:0

Nine data lines from each Write Buffer (eight bits of data and one bit of parity).

AccTypOut 1:0

The access type signals from the Write Buffer specifying the size of a data access: word, tri-byte, half-word, or byte.

$\overline{\text{OutEn}}$

The memory controller asserts this write input to enable the tri-state outputs of the IDT79R3020 address and data signals.

$\overline{\text{Request}}$

The Write Buffer asserts this signal to inform the main memory system that it has data to be written to memory.

Acknowledge

The main memory system asserts this signal when it has captured the data presented by the Write Buffer on the DataOut lines.

Write Buffer - Main Memory Interface Timing

Figure 6 illustrates the timing for the transfer of data from the Write Buffer to the main memory system. The sequence illustrated in this figure is as follows:

1) When the Write Buffer has a data-address pair for transfer to the memory system, it asserts the Request signal.
2) When memory system is ready to handle the Write Buffer data, it asserts the OutEn signal to enable the Write Buffers' address and data outputs onto the system buses.
3) When memory system no longer requires the Write Buffer address and data outputs, it asserts the Acknowledge signal. The Write Buffer responds to this signal by discarding the address-data pair that was just output.
4) The memory system can deassert the OutEn signal to return the Write Buffers' address and data outputs to their tri-state condition.
5) Since the Request signal remains asserted, the memory system asserts the OutEn signal again to enable the next address-data pair onto the system buses.
6) When memory system has accepted the second address-data pair, it again asserts the Acknowledge signal. If the Write Buffer is now empty, it responds to this signal by deasserting the Request signal.

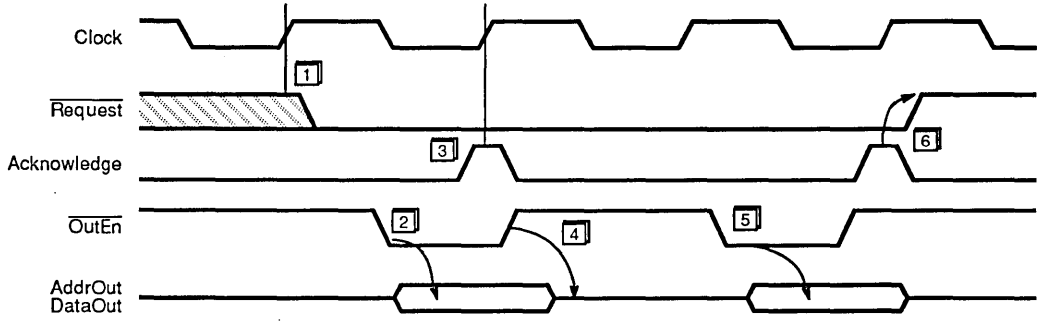


Figure 6. Write Buffer — Main Memory Interface Timing

Note that the buffer's interface to main memory is not completely asynchronous: assertion of the Request signal by the Write Buffer is synchronized with the rising edge of Clock, and the Acknowledge signal input by main memory has a minimum set up and hold time in relation to the Clock signal.

MISCELLANEOUS WRITE BUFFER - BOARD LOGIC INTERFACE

The Write Buffers support several functions that utilize signals that do not fit neatly into the descriptions of either the processor or main memory interfaces. These functions and signals typically involve miscellaneous logic on a CPU board and include the following:

- byte gathering
- configuration connections (Big Endian, Position 1:0)
- address matching logic
- error address latch logic

The sections that follow describe each of these categories.

Byte Gathering

The Write Buffers perform byte (half-word, tri-byte and word) gathering to decrease the number of write transfers to same location; that is, sequential writes to the same WORD address have their data combined into the same address-data pair buffer.

Byte gathering is prohibited in the address-data pair that is currently available to the memory controller. Thus, the first write into an empty Write Buffer will not have subsequent writes gathered into it because it is currently available for output to memory. Writes to the same location (byte) may be overwritten in the Write Buffer if the gathering is not prohibited by the preceding rule.

The Write Buffers present address-data pairs to the main memory controller in the sequence in which they were received from the processor except in the case of gathered data, where bytes or half words can be collected and written to main memory in a single write operation. If the address-data pair buffer is scheduled to be output, then gathering is inhibited and the buffer contents are presented to the main memory controller. Subsequent writes are then placed in another buffer. No reliance should be placed in any aspect of gathering (except that it only involves sequential writes to the same word address) as it is not readily deterministic. Non-sequential writes to the same word address are not gathered.

Note that gathering can require that two main memory controller references be used to empty a single Write Buffer entry. For example, this can occur if Bytes 0 and 3 of a word are sequentially written. Where order in writing is important, such as in I/O controllers, software should avoid sequential accesses to the same word. In cases where write-read access ordering is important but reading of the write location is not desired, such as during I/O, then a write followed by a write to a dummy location followed by a read of the dummy location will insure the first write has occurred before continuing. Alternatively, the Request signal can be tested to determine that the Write Buffer is empty.

Configuration Logic Connections

Because of their byte gathering capability, each buffer device internally maintains a record of each valid byte in an address/data pair. To do this, each device must have a way of determining which data bits within a word it is handling. The following signals determine how the write buffers handle data that is written to the devices:

- **Position 1, Position 0** - these signals (in conjunction with Big Endian) determine how each Write Buffer decodes the Address 1/0 and AccType 1/0 to determine if it should store the data inputs. Refer to Figure 3 for an illustration of how data bits are assigned to Write Buffer devices based on their *position*.
- **Big Endian** - When asserted, byte 0 is the leftmost, most significant byte (big-endian): when deasserted, byte 0 is the rightmost, least-significant byte (little-endian).
- **Address 1, Address 0** - these signals (taken from the AdrLo bus) must be connected to all buffer devices since they determine which byte within a word is being accessed.

- **AccType 1, AccType 0** - these inputs signals specify the data size of a write operation as shown in Table 1.

Table 1 shows how these signals operate to specify how bytes are saved within the Write Buffers.

Access Type 1 0	Address 1 0	Bytes Accessed: 31 Big-Endian 0	Bytes Accessed: 31 Little-Endian 0
1 1 (word)	0 0	0 1 2 3	3 2 1 0
1 0 (triple-byte)	0 0	0 1 2	2 1 0
	0 1	1 2 3	3 2 1
0 1 (halfword)	0 0	0 1	1 0
	1 0	2 3	3 2
0 0 (byte)	0 0	0	0
	0 1	1	1
	1 0	2	2
	1 1	3	3

Table 1. Byte Specifications for Write Operations

The lower two address bits of the device in position zero (as determined by the two POSITION inputs) are inhibited; that is, they are not stored directly as they are output on the AdrLo bus. Instead, on output, the lower two address bits are generated from the indication of the positions of the valid data bytes as determined by above table.

MatchOut/MatchIn Logic and Read Conflicts

Whenever the processor references main memory (either a write or a read reference), the Write Buffers compare the word address from the CPU with the word addresses stored in the buffers. If any word address matches, the buffers assert signals that can be used by the main memory controller to ensure that the Write Buffer is emptied before the read access with the conflicting address has been performed.

Figure 7 illustrates the Write Buffer signals involved in address comparison logic. Each write buffer provides four output signals (MatchOut A, B, C, and D) which correspond to the four buffer ranks (A, B, C, D) in each device as shown in Figure 1. These MatchOut signals can be externally NANDed as shown in Figure 7 to determine if the address being input matches those in any rank of the Write Buffer.

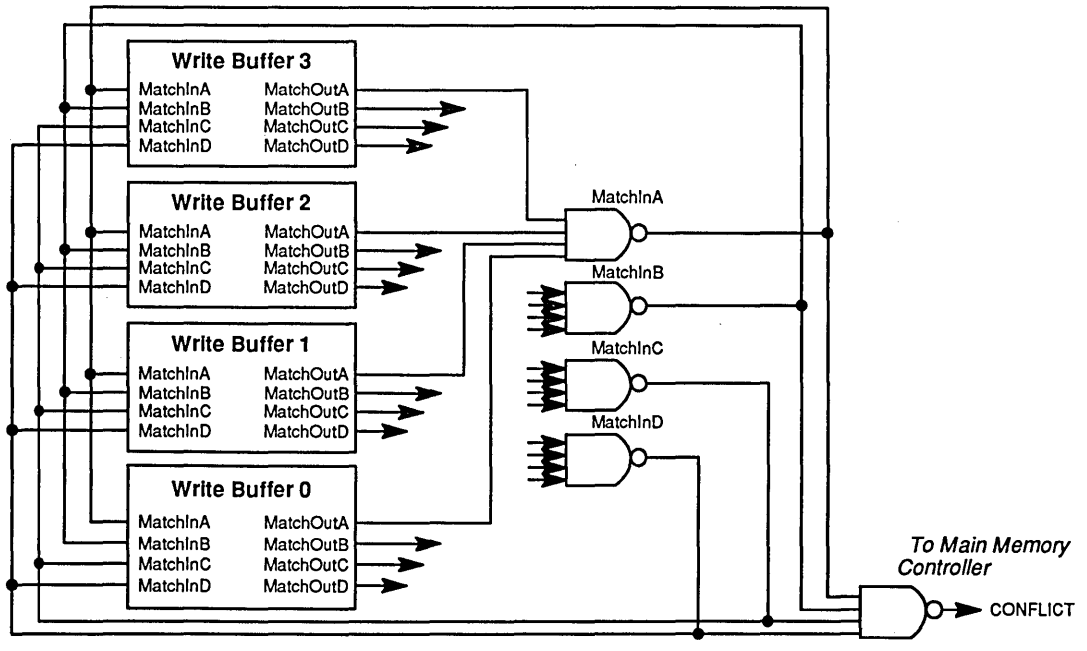


Figure 7. Write Buffer MatchOut/MatchIn Logic

The outputs of the NAND gates are fed into Write Buffers via the MatchIn A, B, C, and D signals and are used within each device as part of the byte gathering logic. The NAND gate outputs can be NANDed together as shown in Figure 7 with the resultant signal used (in conjunction with the processor's $\overline{\text{MEMRD}}$ signal) to alert the main memory controller logic that there is a pending buffered write that conflicts with a just-issued read. The main memory controller can then delay the read access until the Request signal is deasserted indicating that the Write Buffer has been emptied.

Error Address Latch

The write buffer incorporates an internal latch that can be loaded with one of the buffered addresses and subsequently enabled out onto the data lines. This feature can be used by error handling routines to read an address back from the Write Buffer and analyze or recover from certain bus errors. Figure 8 shows the signals involved in operation of this latch.

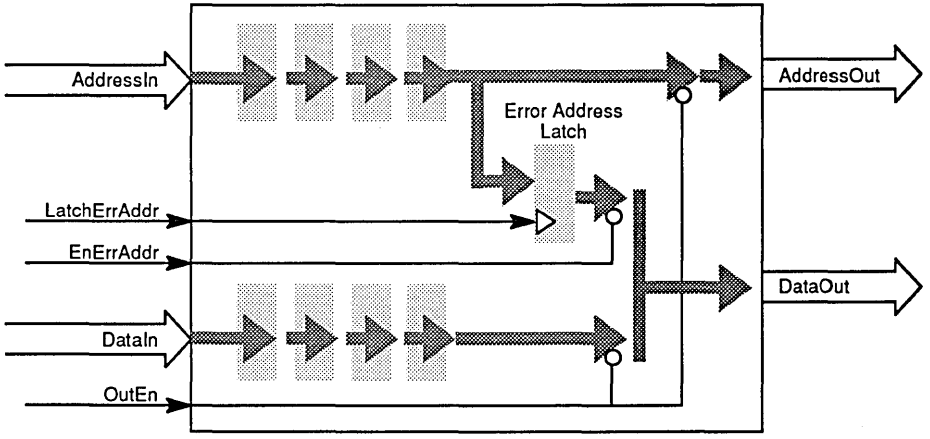


Figure 8. The Write Buffer Error Address Latch

When the LatchErrAddr signal is asserted, the address currently available to the address outputs of the Write Buffer is latched into the internal latch. This address can then be output on the DataOut lines by asserting the EnErrAdr signal so that the processor can read the address in as data. Refer to the AC specifications for timing parameters of the signals associated with the error address latch.

ABSOLUTE MAXIMUM RATINGS[1, 3]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature[2]	–55 to +125	–65 to +150	°C
V_{IN}	Input Voltage	–0.5 to +7.0	–0.5 to +7.0	V

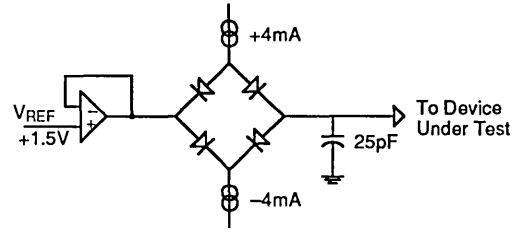
NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	–55°C to +125°C	0V	5.0 ± 10%
Commercial	0°C to +70°C	0V	5.0 ± 5%

OUTPUT LOADING FOR AC TESTING



DC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0 V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	33.33MHz MIN.	33.33MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage[1]		2.4	—	2.4	—	2.4	—	2.4	—	V
V_{IL}	Input LOW Voltage[2]		—	0.8	—	0.8	—	0.8	—	0.8	V
C_{IN}	Input Capacitance		10	—	10	—	10	—	10	—	pF
C_{OUT}	Output Capacitance		10	—	10	—	10	—	10	—	pF
I_{CC}	Operating Current	V_{CC} = Max	—	50	—	60	—	70	—	80	mA
I_{IH}	Input HIGH Leakage	V_{IH} = V_{CC}	—	10	—	10	—	10	—	10	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–10	—	–10	—	–10	—	–10	—	µA
I_{OZ}	Output Tri–state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–40	40	–40	40	–40	40	–40	40	µA

DC ELECTRICAL CHARACTERISTICS — MILITARY TEMPERATURE RANGE (T_A = –55°C to +125°C, V_{CC} = +5.0 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage[1]		2.4	—	2.4	—	2.4	—	V
V_{IL}	Input LOW Voltage[2]		—	0.8	—	0.8	—	0.8	V
C_{IN}	Input Capacitance		10	—	10	—	10	—	pF
C_{OUT}	Output Capacitance		10	—	10	—	10	—	pF
I_{CC}	Operating Current	V_{CC} = Max	—	50	—	60	—	70	mA
I_{IH}	Input HIGH Leakage	V_{IH} = V_{CC}	—	10	—	10	—	10	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–10	—	–10	—	–10	—	µA
I_{OZ}	Output Tri–state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–40	40	–40	40	–40	40	µA

NOTES:

1. V_{IH} should be held above V_{CC} + 0.5 Volts.
2. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 Volts for longer periods.

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE (T_A + 0°C to 70°C, V_{CC} = +5.0V ± 5%)

SYMBOL	PARAMETER	16.67 MHz		20.0 MHz		25.0 MHz		33.33 MHz		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t1	Addrin (3:0) to Clock falling setup	8	—	7	—	6	—	3	—	ns
t2	Addrin (3:0) from Clock falling hold	4	—	4	—	4	—	3	—	ns
t3	Address 1:0 to Clock falling setup	8	—	7	—	6	—	3	—	ns
t4	Address 1:0 from Clock falling hold	4	—	4	—	4	—	3	—	ns
t5	Access Type 1:0 to Clock rising setup	7	—	6	—	5	—	4	—	ns
t6	Access Type 1:0 from Clock rising hold	3	—	3	—	2	—	2	—	ns
t7	Addrin (7:4) to Clock rising setup	7	—	5	—	4	—	4	—	ns
t8	Addrin (7:4) from Clock rising hold	3	—	3	—	2	—	1	—	ns
t9	DataIn (8:0) to Clock rising setup	7	—	5	—	4	—	4	—	ns
t10	DataIn (8:0) from Clock rising hold	3	—	3	—	2	—	1	—	ns
t11	$\overline{\text{WrtMem}}$ to Clock rising setup	10	—	8	—	7	—	6	—	ns
t12	$\overline{\text{WrtMem}}$ from Clock rising hold	6	—	5	—	4	—	3	—	ns
t13	Request from Clock rising	—	32	—	30	—	22	—	16	ns
t14	Acknowledge to Clock rising setup	12	—	11	—	6	—	4	—	ns
t15	Acknowledge from Clock rising hold	7	—	6	—	5	—	3	—	ns
t16	LatchErrAdr to Acknowledge rising	5	—	5	—	5	—	3	—	ns
t17	$\overline{\text{WbFull}}$ active from Clock rising	—	21	—	19	—	17	—	9	ns
t18	$\overline{\text{WbFull}}$ inactive from Clock rising	—	21	—	19	—	11	—	9	ns
t19	OutEn to AddrOut (7:0), DataOut (8:0) valid	2	15	2	15	2	15	2	12	ns
t20	OutEn to AddrOut (7:0), DataOut (8:0) tri-state	2	15	2	15	2	15	2	12	ns
t21	MatchOut (ABCD) from Clock rising	—	24	—	22	—	20	—	15	ns
t22	MatchIn (ABCD) to Clock rising setup	10	—	9	—	8	—	5	—	ns
t23	MatchIn (ABCD) from Clock rising hold	3	—	3	—	3	—	3	—	ns
t24	$\overline{\text{EnErrAdr}}$ to Data (error latch) valid	2	15	2	15	2	15	2	15	ns
t25	$\overline{\text{EnErrAdr}}$ to Data (error latch) tri-state	2	15	2	15	2	15	2	15	ns
t26	Address/Data out from Clock rising	—	30	—	27	—	24	—	16	ns
t27	$\overline{\text{Reset}}$ to Clock rising, set-up	10	—	10	—	10	—	8	—	ns
t28	$\overline{\text{Reset}}$ from Clock rising, hold	3	—	2	—	1	—	1	—	ns
t29	Reset low pulse width	8	—	8	—	8	—	8	—	cycles
t30	$\overline{\text{WbFull}}$ High from Clock rising (after $\overline{\text{Reset}}$)	—	22	—	21	—	20	—	11	ns
t31	$\overline{\text{Request}}$ High from $\overline{\text{Reset}}$ low	—	20	—	19	—	18	—	16	ns
t32	Access TypOut 1:0 low from $\overline{\text{Reset}}$ low	—	28	—	26	—	25	—	23	ns
t33	Match Out (ABCD) Low from $\overline{\text{Reset}}$ low	—	21	—	20	—	20	—	15	ns
t34	Address/Data out tri-state from $\overline{\text{Reset}}$ low (OutEn negated)	—	32	—	30	—	27	—	23	ns
t35	Access TypeOut from Clock rising	—	32	—	30	—	27	—	23	ns
tcyc	Clock Pulse Width	60	2000	50	2000	40	2000	30	2000	ns
tckhigh	Clock High Pulse Width	24	—	20	—	16	—	12	—	ns
tcklow	Clock Low Pulse Width	24	—	20	—	16	—	12	—	ns

AC ELECTRICAL CHARACTERISTICS — MILITARY TEMPERATURE RANGE (T_A + −55°C to 125°C, V_{CC} = +5.0V ± 10%)

SYMBOL	PARAMETER	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	UNIT
t1	Addrin (3:0) to Clock falling setup	8	—	7	—	6	—	ns
t2	Addrin (3:0) from Clock falling hold	4	—	4	—	4	—	ns
t3	Address 1:0 to Clock falling setup	8	—	7	—	6	—	ns
t4	Address 1:0 from Clock falling hold	4	—	4	—	4	—	ns
t5	Access Type 1:0 to Clock rising setup	7	—	6	—	5	—	ns
t6	Access Type 1:0 from Clock rising hold	3	—	3	—	2	—	ns
t7	Addrin (7:4) to Clock rising setup	7	—	5	—	4	—	ns
t8	Addrin (7:4) from Clock rising hold	3	—	3	—	2	—	ns
t9	DataIn (8:0) to Clock rising setup	7	—	5	—	4	—	ns
t10	DataIn (8:0) from Clock rising hold	3	—	3	—	2	—	ns
t11	$\overline{\text{WrtMem}}$ to Clock rising setup	10	—	8	—	7	—	ns
t12	$\overline{\text{WrtMem}}$ from Clock rising hold	6	—	5	—	4	—	ns
t13	Request from Clock rising	—	32	—	30	—	22	ns
t14	Acknowledge to Clock rising setup	12	—	11	—	6	—	ns
t15	Acknowledge from Clock rising hold	7	—	6	—	5	—	ns
t16	LatchErrAdr to Acknowledge rising	5	—	5	—	5	—	ns
t17	$\overline{\text{WbFull}}$ active from Clock rising	—	21	—	19	—	17	ns
t18	$\overline{\text{WbFull}}$ inactive from Clock rising	—	21	—	19	—	11	ns
t19	OutEn to AddrOut (7:0), DataOut (8:0) valid	2	15	2	15	2	15	ns
t20	OutEn to AddrOut (7:0), DataOut (8:0) tri-state	2	15	2	15	2	15	ns
t21	MatchOut (ABCD) from Clock rising	—	24	—	22	—	20	ns
t22	MatchIn (ABCD) to Clock rising setup	10	—	9	—	8	—	ns
t23	MatchIn (ABCD) from Clock rising hold	3	—	3	—	3	—	ns
t24	$\overline{\text{EnErrAdr}}$ to Data (error latch) valid	2	15	2	15	2	15	ns
t25	$\overline{\text{EnErrAdr}}$ to Data (error latch) tri-state	2	15	2	15	2	15	ns
t26	Address/Data out from Clock rising	—	30	—	27	—	24	ns
t27	$\overline{\text{Reset}}$ to Clock rising, set-up	10	—	10	—	10	—	ns
t28	$\overline{\text{Reset}}$ from Clock rising, hold	3	—	2	—	1	—	ns
t29	$\overline{\text{Reset}}$ low pulse width	8	—	8	—	8	—	cycles
t30	$\overline{\text{WbFull}}$ High from Clock rising (after $\overline{\text{Reset}}$)	—	22	—	21	—	20	ns
t31	$\overline{\text{Request}}$ High from $\overline{\text{Reset}}$ low	—	20	—	19	—	18	ns
t32	Access TypOut 1:0 low from $\overline{\text{Reset}}$ low	—	28	—	26	—	25	ns
t33	Match Out (ABCD) Low from $\overline{\text{Reset}}$ low	—	21	—	20	—	20	ns
t34	Address/Data out tri-state from $\overline{\text{Reset}}$ low (OutEn negated)	—	32	—	30	—	27	ns
t35	Access TypeOut from Clock rising	—	32	—	30	—	27	ns
tcyc	Clock Pulse Width	60	2000	50	2000	40	2000	ns
tckhigh	Clock High Pulse Width	24	—	20	—	16	—	ns
tcklow	Clock Low Pulse Width	24	—	20	—	16	—	ns

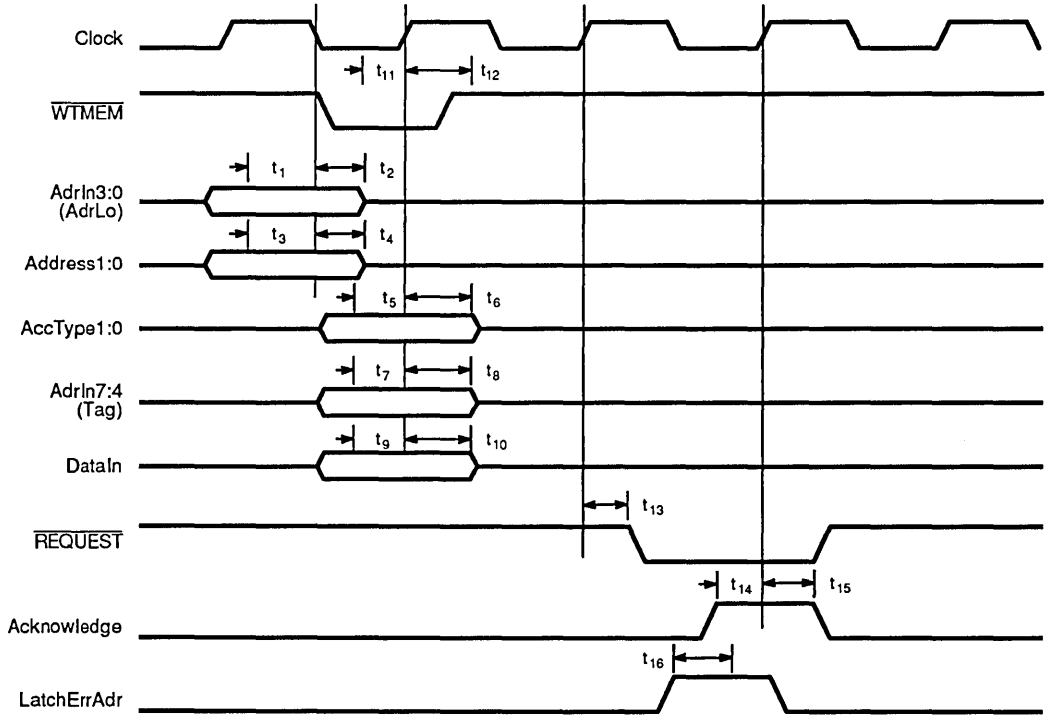


Figure 9. Write Buffer Timing Specifications

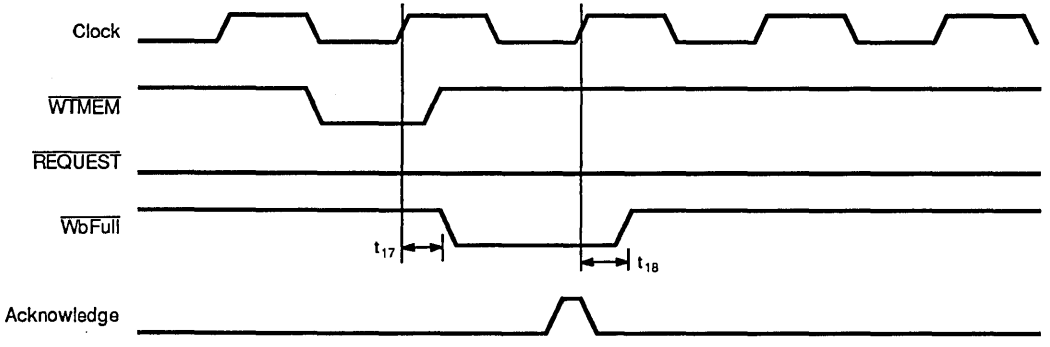


Figure 10. WBFULL Signal Timing Specifications

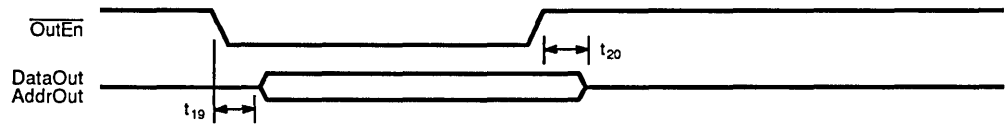


Figure 11. $\overline{\text{OUTEN}}$ Timing Specifications

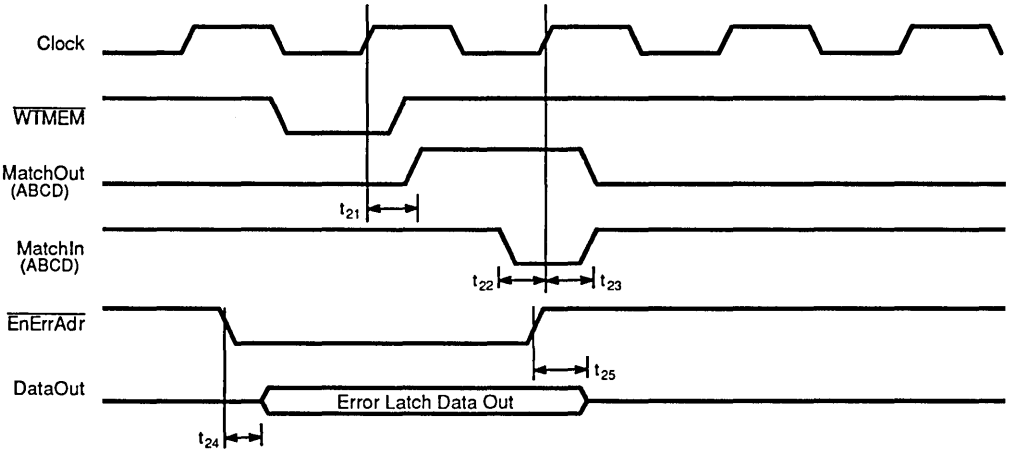


Figure 12. Match and Error Latch Timing Specifications

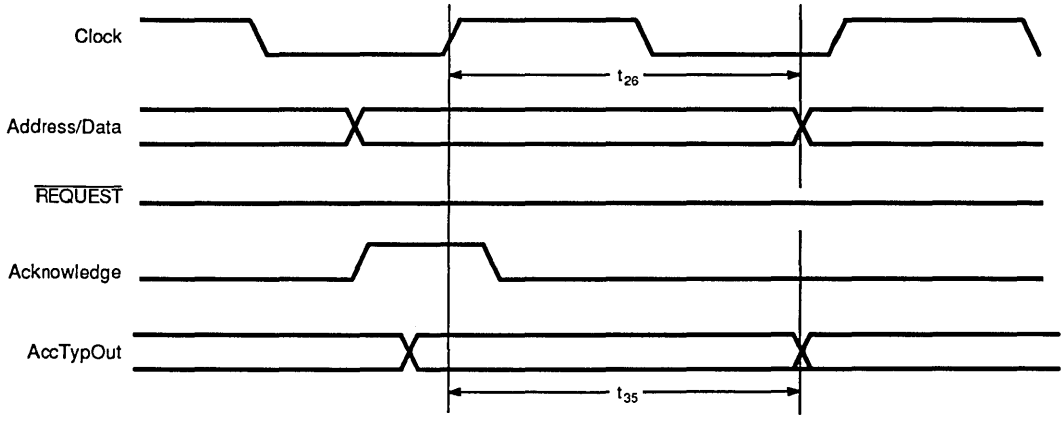


Figure 13. Address/Data Out, Access Type Out

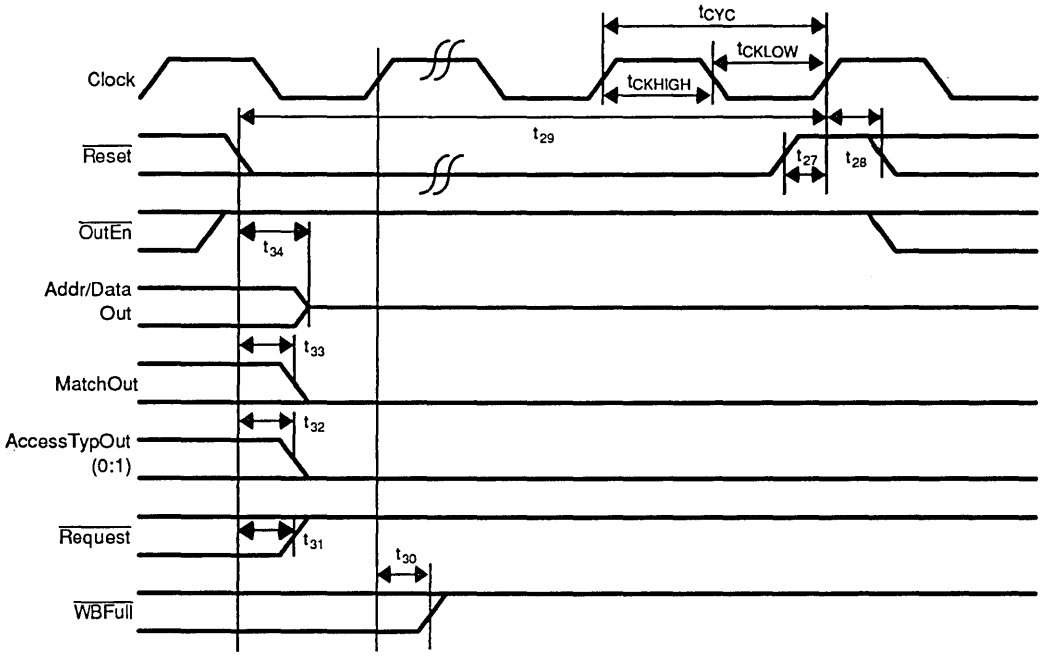
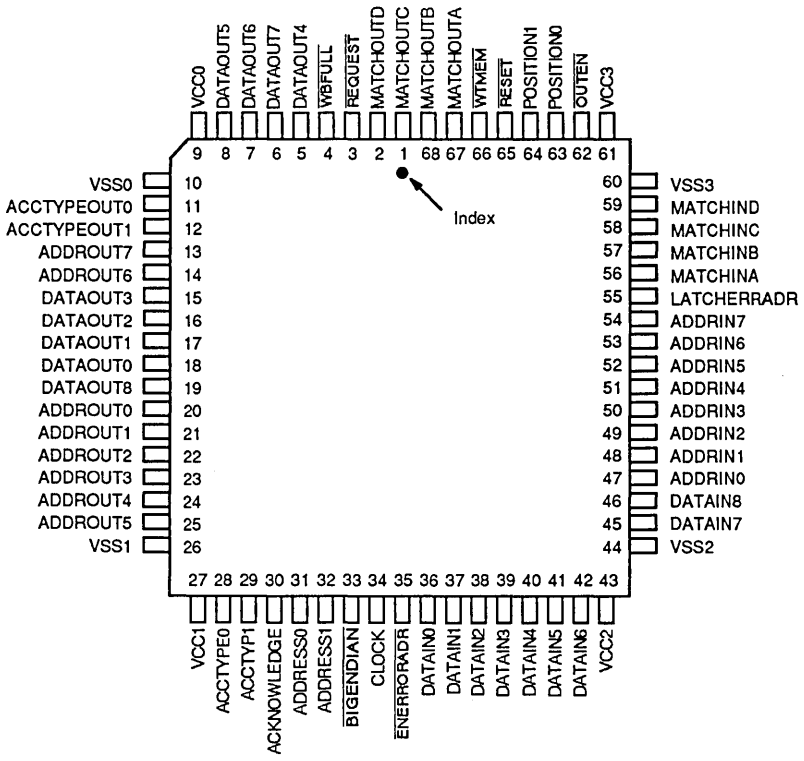


Figure 14. Reset Timing

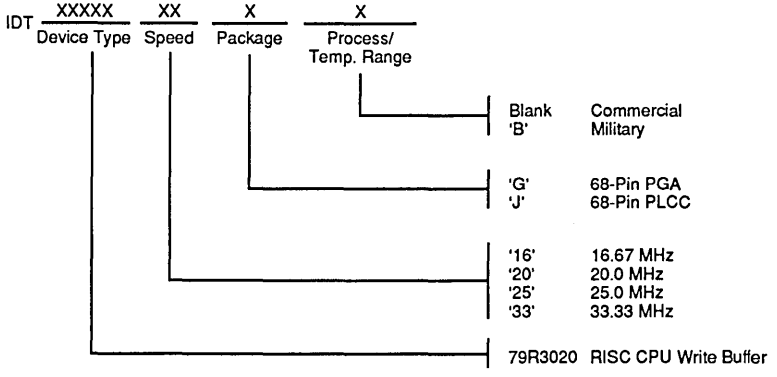
68-PIN CPGA FOR R3020
PIN GRID ARRAY (CERAMIC) – BOTTOM VIEW

	1	2	3	4	5	6	7	8	9	10	11
L		ACC-TYPE0	AC-KNOWL-EDGE	AD-DRESS1	CLOCK	DATA-IN0	DATA-IN2	DATA-IN4	DATA-IN6	VCC2	
K	GND1	VCC1	ACC-TYPE1	AD-DRESS0	BIG-ENDIAN	EN-ERROR-ADR	DATA-IN1	DATA-IN3	DATA-IN5	GND2	DATA-IN7
J	ADDR-OUT5	ADDR-OUT4								DATA-IN8	ADDR-IN0
H	ADDR-OUT3	ADDR-OUT2								ADDR-IN1	ADDR-IN2
G	ADDR-OUT1	ADDR-OUT0								ADDR-IN3	ADDR-IN4
F	DATA-OUT8	DATA-OUT0								ADDR-IN5	ADDR-IN6
E	DATA-OUT1	DATA-OUT2								ADDR-IN7	LATCH-ERR-ADR
D	DATA-OUT3	ADDR-OUT6								MATCH-INA	MATCH-INB
C	ADDR-OUT7	ACC-TYPE OUT1								MATCH-INC	MATCH-IND
B	ACC-TYPE OUT0	GND0	DATA-OUT7	DATA-OUT4	REQUEST	MATCH-OUTC	MATCH-OUTA	RESET	PO-SITION0	VCC3	GND3
A		VCC0	DATA-OUT5	DATA-OUT6	WBFULL	MATCH-OUTD	MATCH-OUTB	WTMEM	PO-SITION1	OUTEN	

PIN CONFIGURATION
PLASTIC LEADED CHIP CARRIER
(TOP VIEW)



ORDERING INFORMATION



Integrated Device Technology, Inc.

IDT79R3051 FAMILY OF INTEGRATED RISControllers™

ADVANCE INFORMATION
IDT 79R3051™, 79R3051E
IDT 79R3052™, 79R3052E

FEATURES:

- Instruction set compatible with IDT79R3000A and IDT79R3001 MIPS RISC CPUs
- High level of integration minimizes system cost, power consumption
  - 79R3000A /79R3001 Execution Engine
  - R3051 features 4kB of Instruction Cache
  - R3052 features 8kB of Instruction Cache
  - All devices feature 2kB of Data Cache
  - "E" Versions (Extended Architecture) feature full function Memory Management Unit, including 64-entry Translation Lookaside Buffer (TLB)
  - 4-deep write buffer eliminates memory write stalls
  - 4-deep read buffer supports burst refill
  - On-chip DMA arbiter
  - Bus Interface Minimizes Processor Stalls
- Single clock input
- Direct interface to R3720/21/22 RISChipset
- 35 MIPS, over 64,000 Dhrystones at 40 MHz
- Low cost 84-pin PLCC packaging
- Flexible bus interface allows simple, low cost designs
- 20, 25, 33, and 40 MHz operation
- Complete software support
  - Optimizing compilers
  - Real-time operating systems
  - Monitors/debuggers
  - Floating Point Software
  - Page Description Languages

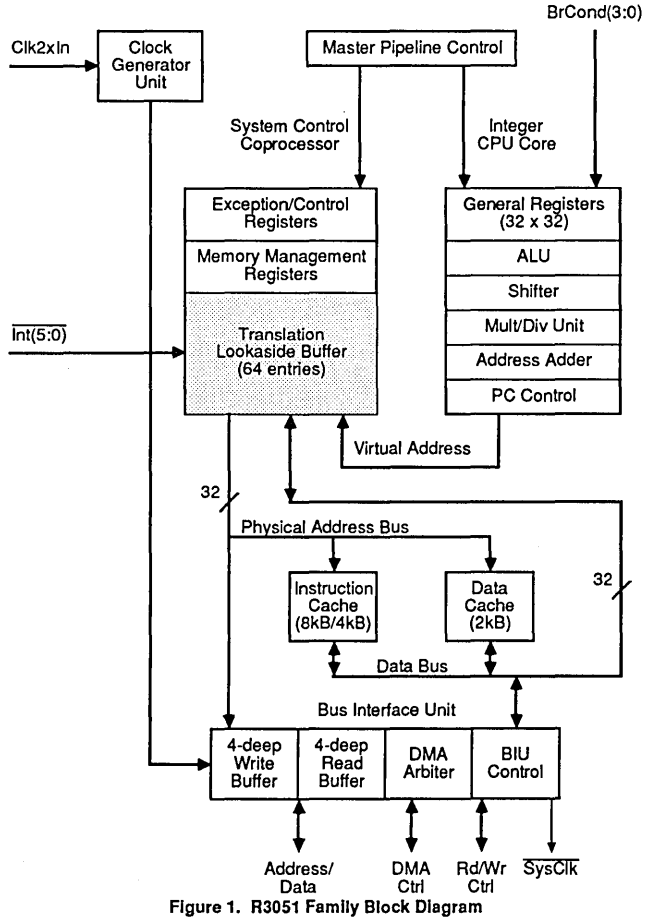


Figure 1. R3051 Family Block Diagram

OCTOBER 1990

INTRODUCTION

The IDT R3051 Family is a series of high-performance 32-bit microprocessors featuring a high level of integration, and targeted to high-performance but cost sensitive embedded processing applications. The R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power sensitive applications.

Functional units were integrated onto the CPU core in order to reduce the total system cost, rather than to increase the inherent performance of the integer engine. Thus, the R3051 family is able to offer 35 MIPS of integer performance at 40 MHz without requiring external SRAM or caches.

Further, the R3051 family brings dramatic power reduction to these embedded applications, allowing the use of low-cost packaging for devices up to 25 MHz. The R3051 family allows customer applications to bring maximum performance at minimum cost.

Figure 1 shows a block level representation of the functional units within the R3051 family. The R3051 family could be viewed as the embodiment of a discrete solution built around the IDT 79R3000A or 79R3001. However, by integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

Currently, there are four members of the R3051 family family. All devices are pin and software compatible: the differences lie in the amount of instruction cache, and in the memory management capabilities of the processor:

- The R3052"E" incorporates 8kB of Instruction Cache, and features a full function memory management unit (MMU) including a 64-entry fully-associative Translation Lookaside Buffer (TLB). This is the same memory management unit incorporated in the IDT 79R3000A and 79R3001.
- The R3052 also incorporates 8kB of Instruction Cache. However, the memory management unit is a much simpler subset of the capabilities of the enhanced versions of the architecture, and in fact does not use a TLB.
- The R3051"E" incorporates 4kB of Instruction Cache. Additionally, this device features the same full function MMU (including TLB file) as the R3052"E", and R3000A.
- The R3051 incorporates 4kB of Instruction Cache, and uses the simpler memory management model of the R3052.

An overview of the functional blocks incorporated in these devices follows.

CPU Core

The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close to single cycle execution rate. The CPU core contains a five stage pipeline, and 32 orthogonal 32-bit registers. The R3051 family implements the MIPS-I ISA. In fact, the execution engine of the R3051 family is the same as the execution engine of the R3000A (and R3001). Thus, the R3051 family is binary compatible with those CPU engines.

The execution engine of the R3051 family uses a five-stage pipeline to achieve close to single cycle execution. A new instruction can be started in every clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). Figure 2 shows the concurrency achieved by the R3051 family pipeline.

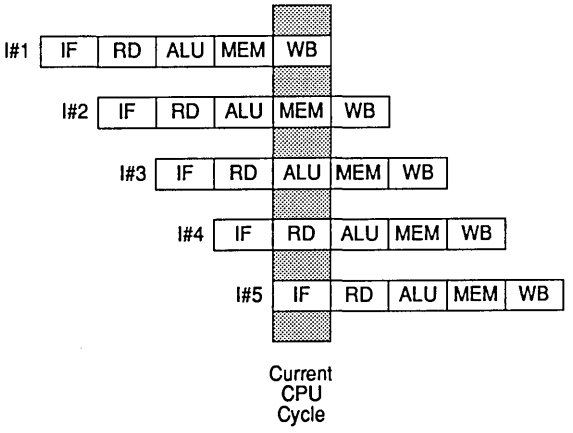


Figure 2. R3051 Family 5-Stage Pipeline

System Control Co-Processor

The R3051 family also integrates on-chip the System Control Co-processor, CP0. CP0 manages both the exception handling capability of the R3051 family, as well as the virtual to physical mapping of the R3051 family.

There are two versions of the R3051 family architecture: the Extended Architecture Versions (the R3051E and R3052E) contain a fully associative 64-entry TLB which maps 4kB virtual pages into the physical address space. The virtual to physical mapping thus includes kernel segments which are hard mapped to physical addresses, and kernel and user segments which are mapped on a page basis by the TLB into anywhere within the 4GB physical address space. In this TLB, 8 page translationss can be "locked" by the kernel to insure deterministic response in real-time applications. These versions thus use the same MMU structure as that found in the IDT 79R3000A and 79R3001. Figure 3 shows the virtual to physical address mapping found in the extended architecture versions of the processor family.

The Extended Architecture devices allow the system designer to implement kernel software to dynamically manage User task utilization of memory resources, and also allow the Kernel to effectively "protect" certain resources from user tasks. These capabilities are important in a number of embedded applications, from process control (where resource protection may be extremely important) to X-Window display systems (where virtual memory management is extremely important).

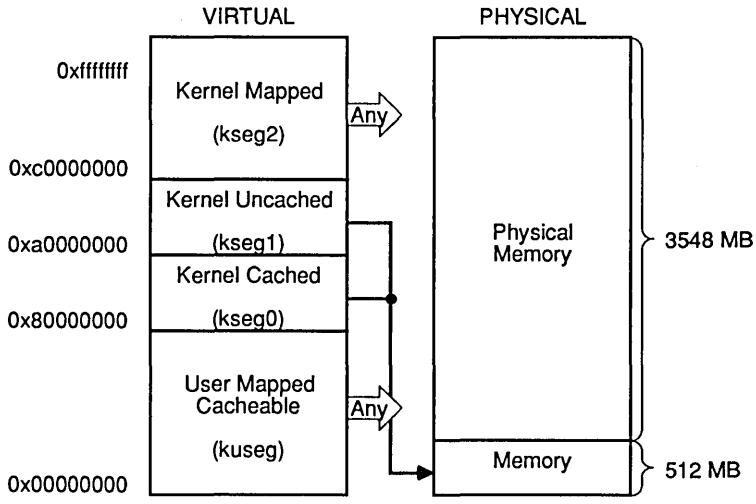


Figure 3. Virtual to Physical Mapping of Extended Architecture Versions

The base versions of the architecture (the R3051 and R3052) remove the TLB and institute a fixed address mapping for the various segments of the virtual address space. The base processors support distinct kernel and user mode operation without requiring page management software, leading to a simpler software model. The memory mapping used by these devices is illustrated in figure 4. Note that the reserved address spaces shown are for compatibility with future family members.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to execute page management software. This distinction can take the form of physical memory protection, accomplished by address decoding, or in other forms. In systems which do not wish to implement memory protection, and wish to have the kernel and user tasks operate out of a single unified memory space, upper address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

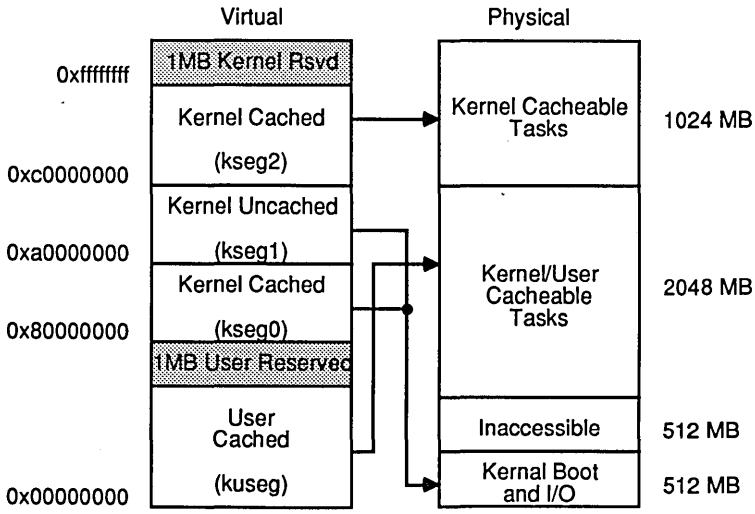


Figure 4. Virtual to Physical Mapping of Base Architecture Versions

Clock Generation Unit

The R3051 family is driven from a single input clock. On-chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line required in R3000A and R3001 based applications.

Instruction Cache

The current family includes two different instruction cache sizes: the R3051 family (the R3051 and R3051E) feature 4kB of instruction cache, and the R3052 and R3052E each incorporate 8kB of Instruction Cache. For all four devices, the instruction cache is organized as a line size of 16 bytes (four words). This relatively large cache achieves a hit rate well in excess of 95% in most applications, and substantially contributes to the performance inherent in the R3051 family. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses (rather than virtual addresses), and thus does not require flushing on context switch.

Data Cache

All four devices incorporate an on-chip data cache of 2kB, organized as a line size of 4 bytes (one word). This relatively large data cache achieves hit rates well in excess of 90% in most applications, and contributes substantially to the performance inherent in the R3051 family. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance.

Bus Interface Unit

The R3051 family uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slow memory devices.

The R3051 family bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE signal to de-multiplex the A/D bus, and simple handshake signals to process processor read and write requests. In addition to the read and write interface, the R3051 family incorporates a DMA arbiter, to allow an external master to control the external bus.

The R3051 family incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and presents it to the bus interface as write transactions at the rate the memory system can accommodate. Figure 5 illustrates a basic write transaction for the R3051/52.

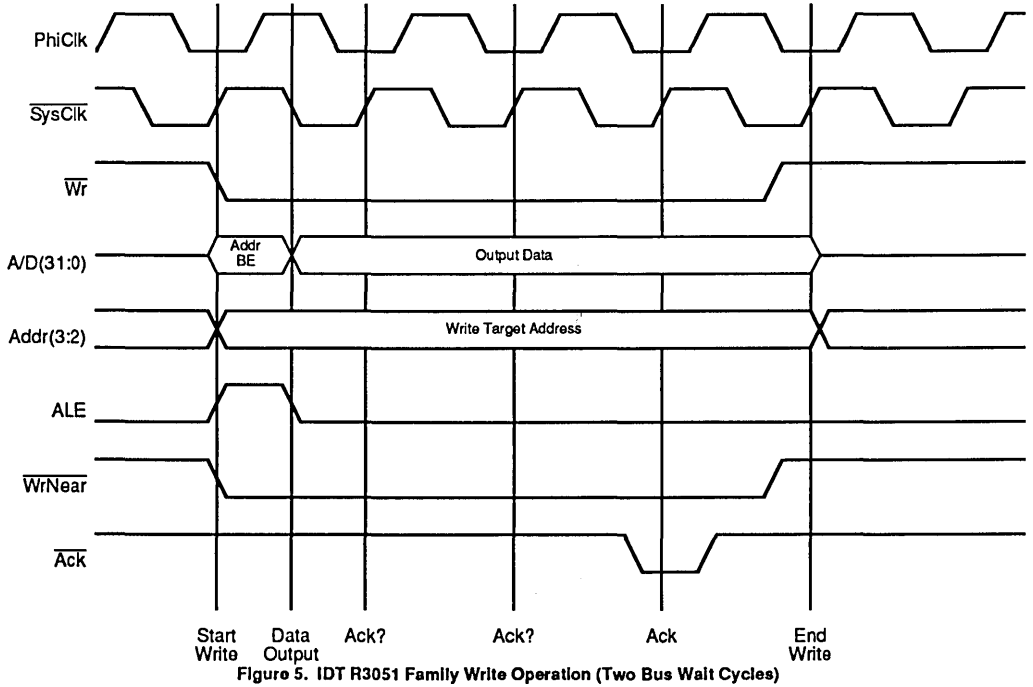


Figure 5. IDT R3051 Family Write Operation (Two Bus Wait Cycles)

The R3051/52 read interface performs both single word reads and quad word reads. Single word reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to utilize page or nibble mode DRAMs (and possibly use interleaving), if desired, in high-performance systems, or use simpler techniques to reduce complexity. Figure 6 illustrates a basic single word read; figure 7 illustrates a burst block transfer. More aggressive designs could significantly reduce the number of processor stall cycles from those shown here.

In order to accommodate slower quad word reads, the R3051 family incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches. Figure 8 shows the action of the processor for a "throttled" quad word read. Depending on the cost vs. performance tradeoffs appropriate to a given application, the system design engineer could include true burst support from the DRAM to provide for high-performance cache miss processing, or utilize the read buffer to process quad word reads from slower memory systems.

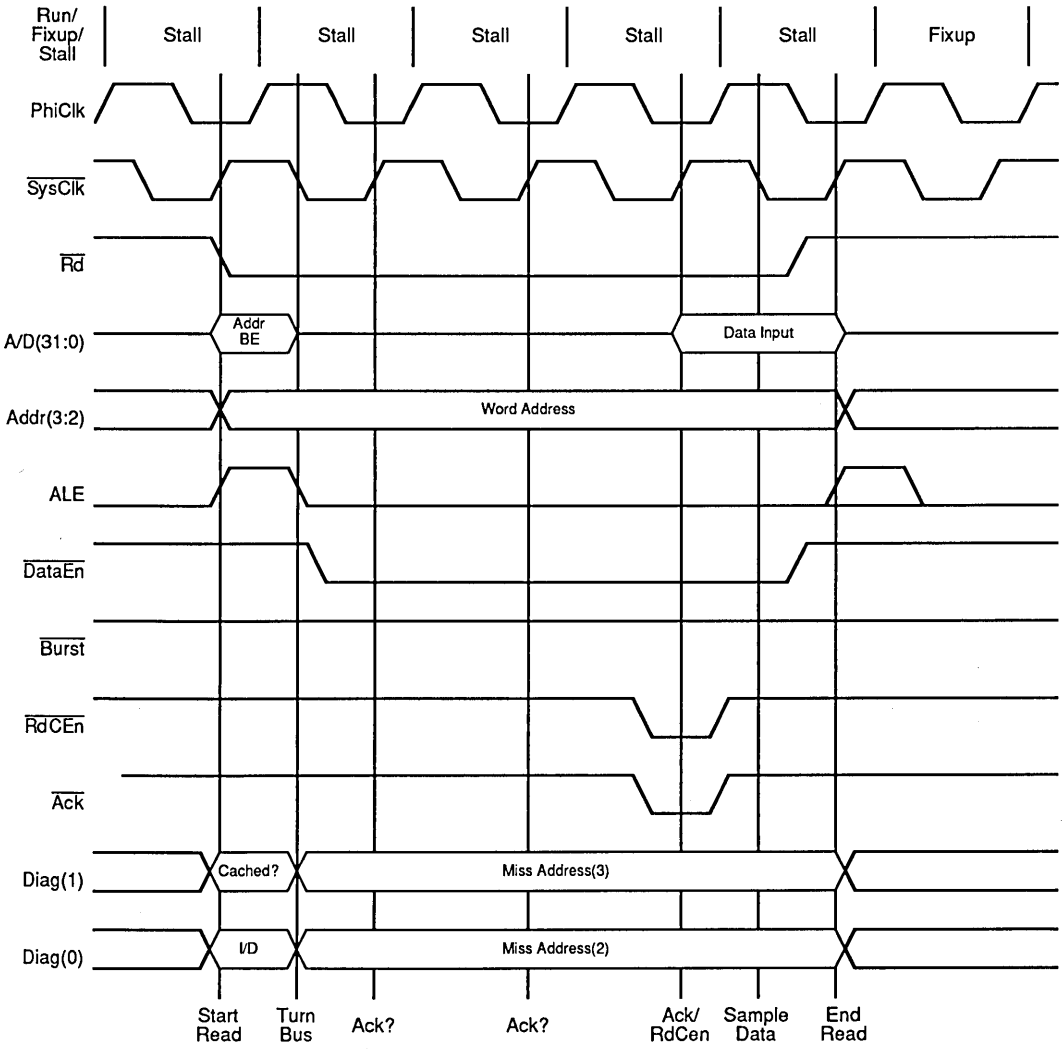


Figure 6. IDT R3051 Family Single Word Read Operation (Two Bus Wait Cycles)

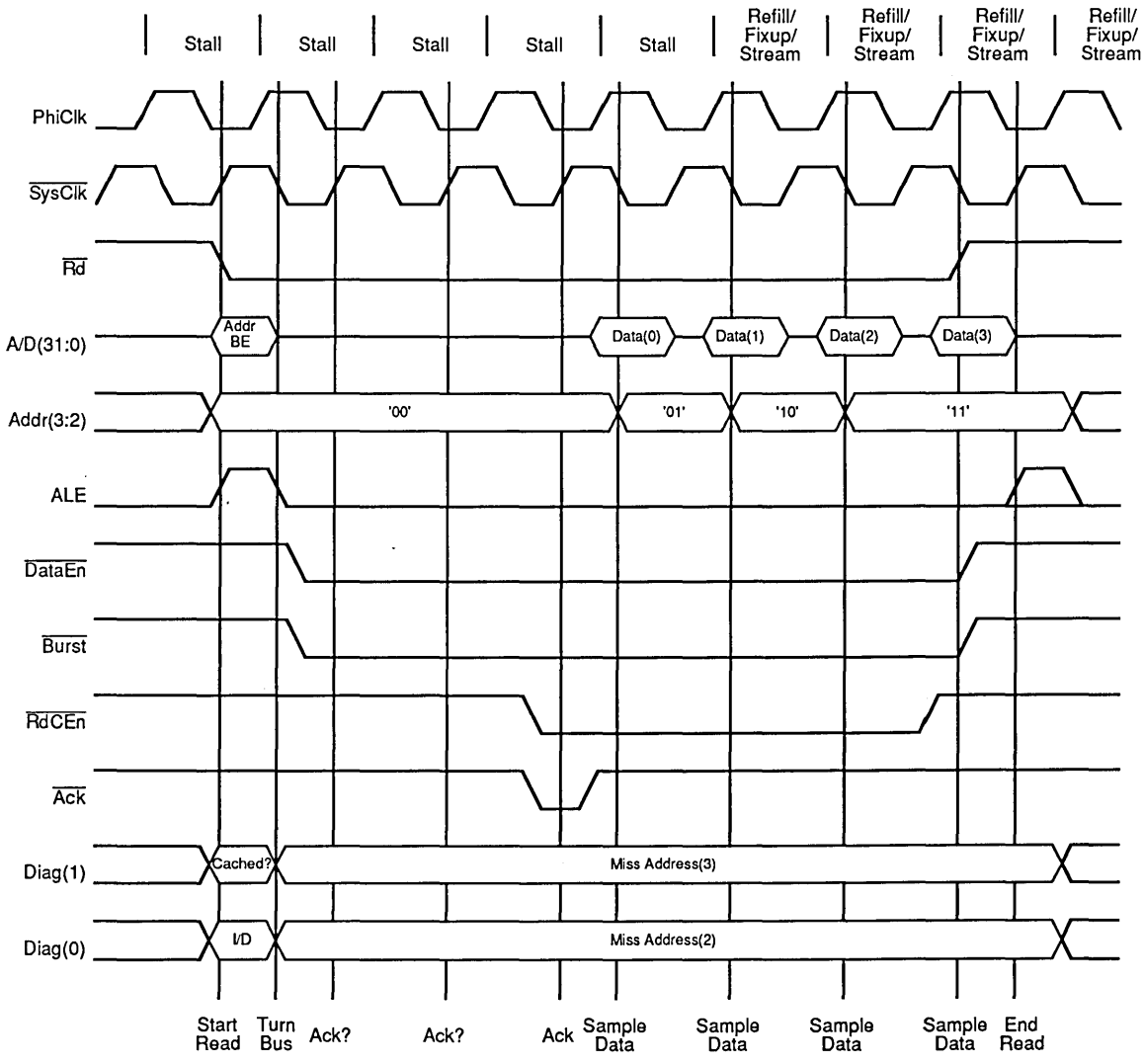


Figure 7. IDT R3051 Family Burst Read Operation (Two Bus Wait Cycles)

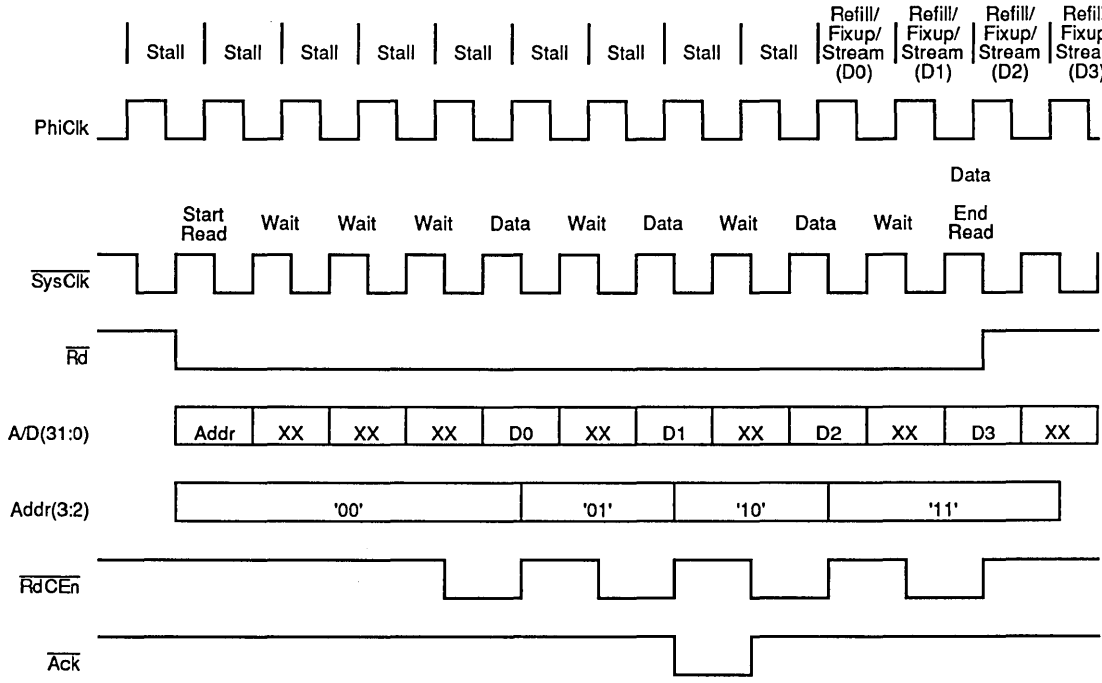


Figure 8. IDT R3051 Family Throttled Quad Read Operation (Three Bus Wait Cycles, One Bus Wait Cycle Between Words)

SYSTEM USAGE

The IDT R3051 family has been specifically designed to easily connect to low-cost memory systems. Typical low-cost memory systems utilize slow EPROMs, DRAMs, and application specific peripherals. These systems may also typically contain large, slow static RAMs, although the IDT R3051 family has been designed to not specifically require the use of external SRAMs.

Figure 9 shows a typical system block diagram. Transparent latches are used to de-multiplex the R3051/52 address and data busses from the A/D bus. The data paths between the memory system elements and the R3051/52 A/D bus is managed by simple octal devices. A small set of simple PALs can be used to control the various data path elements, and to control the handshake between the memory devices and the R3051/52.

Alternately, the memory interface can be constructed using the IDT R3051 family RISChipset, which includes DRAM control, data path control for interleaved memories, and other general memory and system interface control functions. These devices are described in separate data sheets. Figure 10 illustrates a simple system constructed using the R3051 family support chip set.

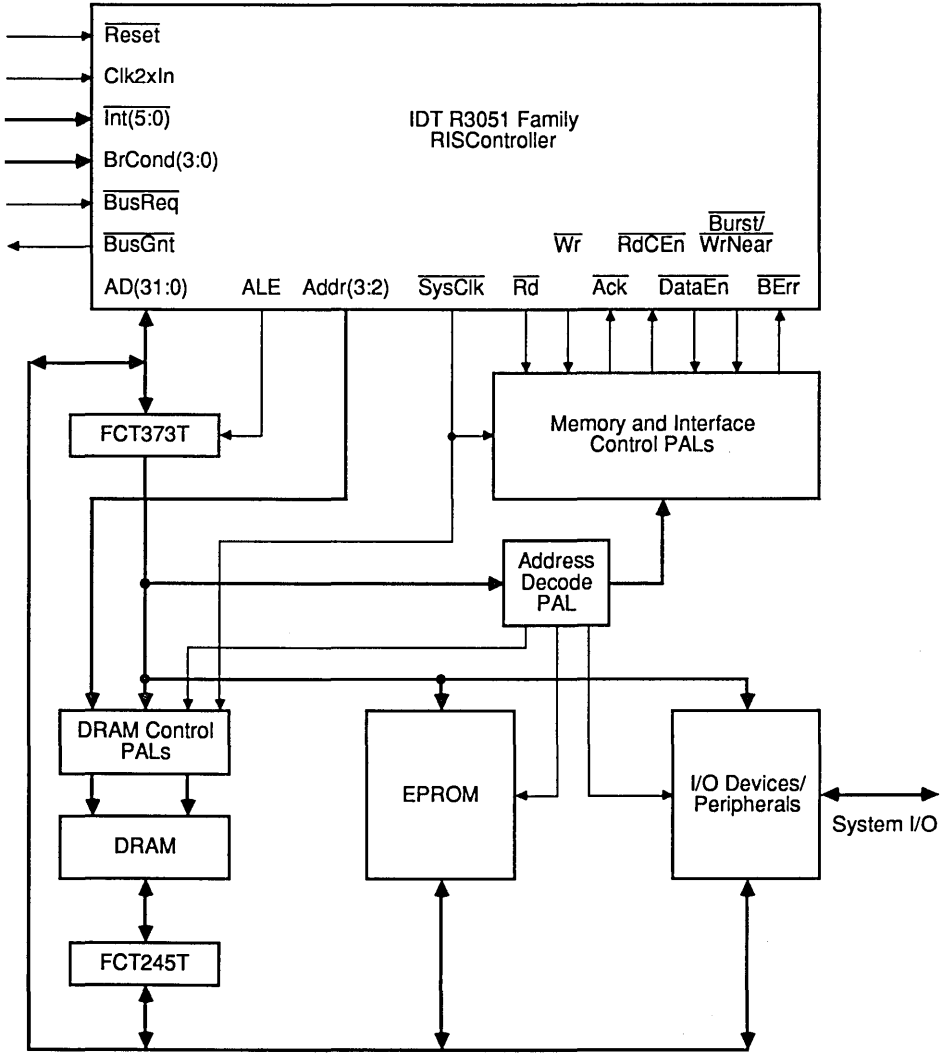


Figure 9. Typical R3051 Family Based System

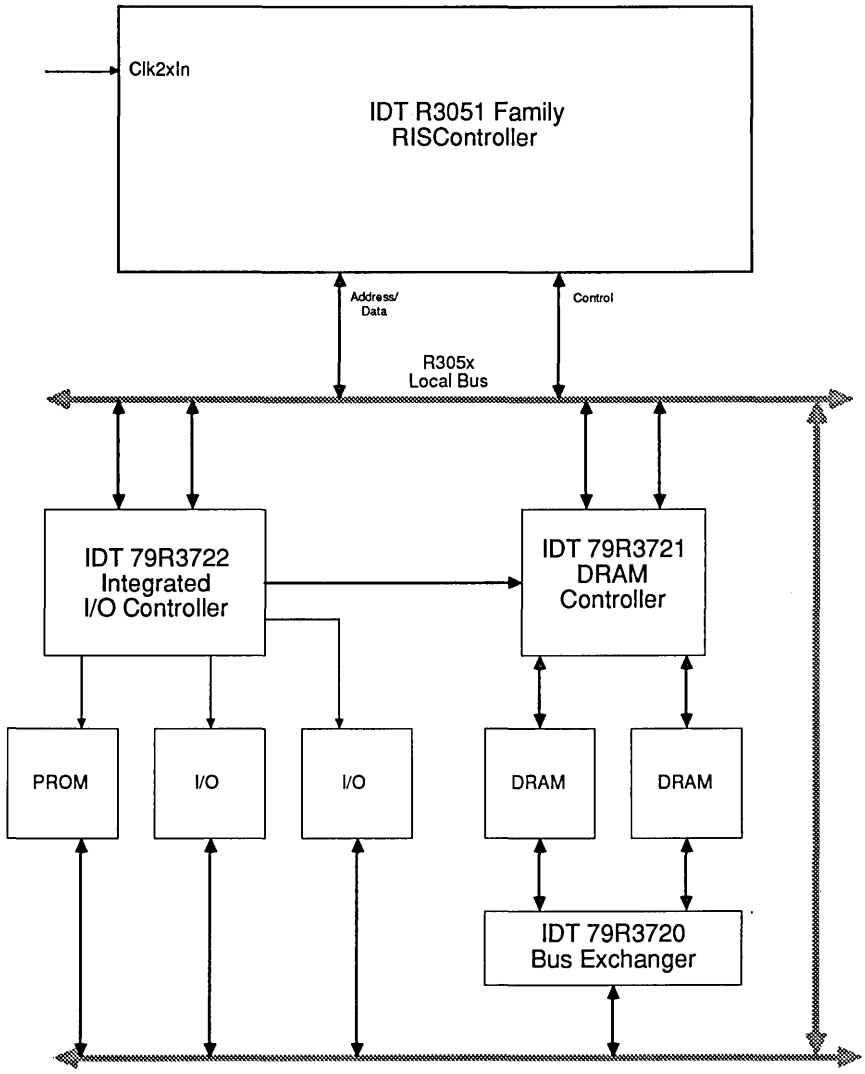


Figure 10. R3051 Family Chip Set Based System

DEVELOPMENT SUPPORT

The IDT R3051 family is supported by a rich set of development tools, ranging from system simulation tools through prom monitor support, logic analysis tools, and sub-system modules.

Figure 11 is an overview of the system development process typically used when developing R3051 family-based applications. The R3051 family is supported by powerful tools through all phases of project development. These tools allow timely, parallel development of hardware and software for R3051/52 based applications, and include tools such as:

- A program, Cache-3051, which allows the performance of an R3051 family based system to be modeled and understood without requiring actual hardware.
- Sable, an instruction set simulator.
- Optimizing compilers from MIPS, the acknowledged leader in optimizing compiler technology.
- IDT Cross development tools, available in a variety of development environments.
- The high-performance IDT floating point library software.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT Prom Monitor.
- The IDT Laser Printer System board, which directly drives a low-cost print engine, and runs Microsoft TrueImage™ Page Description Language on top of PeerlessPage™ Advanced Printer Controller BIOS.
- Adobe PostScript™ Page Description Language, ported to the R3000 instruction set, runs on the IDT R3051 family.
- The IDT Prom Monitor, which implements a full prom monitor (diagnostics, remote debug support, peek/poke, etc.).

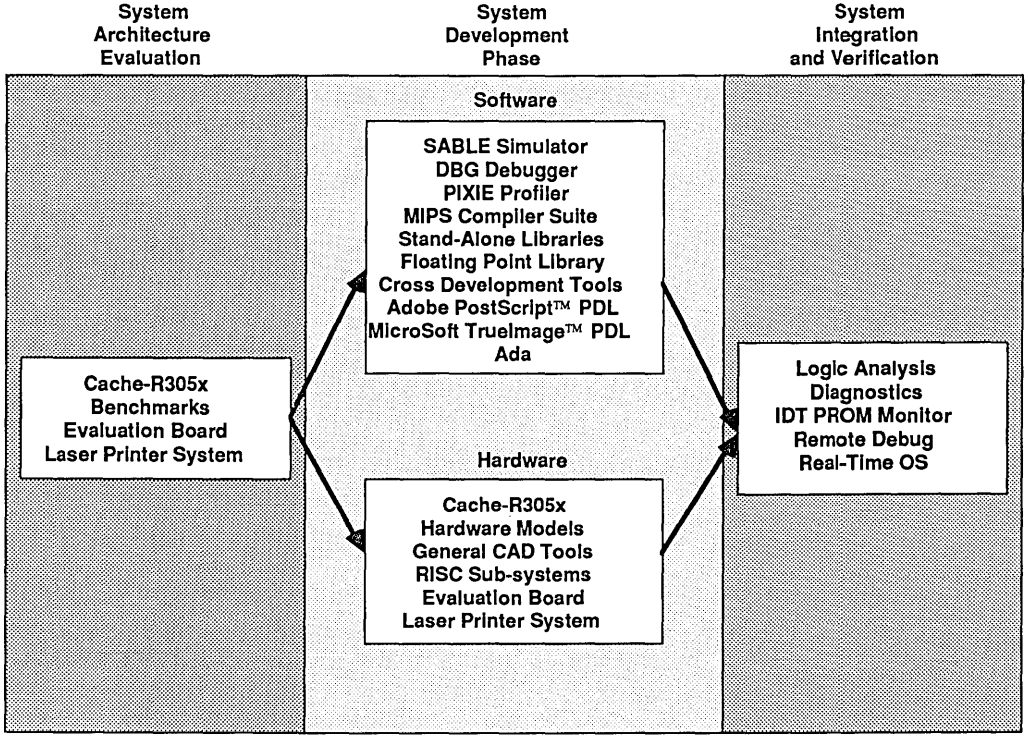


Figure 11. R3051 Family Development Toolchain

PERFORMANCE OVERVIEW

The R3051 family achieves a very high-level of performance. This performance is based on:

- **An efficient execution engine.** The CPU performs ALU operations and store operations at a single cycle rate, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the execution engine achieves over 35 MIPS performance when operating out of cache.
- **Large on-chip caches.** The R3051 family contains caches which are substantially larger than those on the majority of today's embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the R3051 family to achieve actual sustained performance very close to its peak execution rate.
- **Autonomous multiply and divide operations.** The R3051 family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the R3051 family to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than "step" operations.
- **Integrated write buffer.** The R3051 family features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support.** The R3051 family enables the system designer to utilize page mode or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

These techniques combine to allow the processor to achieve 35 MIPS integer performance, and over 64,000 dhrystones at 40 MHz without the use of external caches or zero wait-state memory devices.

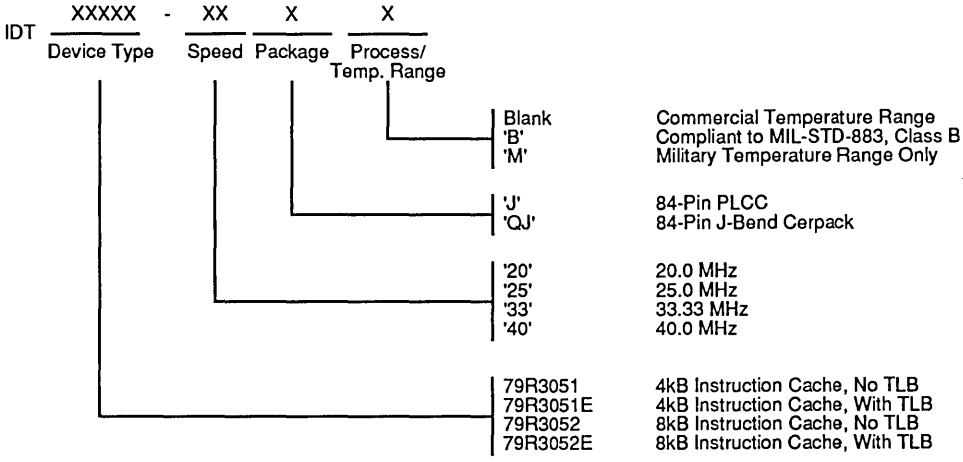
PIN DESCRIPTION:

PIN NAME	I/O	DESCRIPTION
A/D(31:0)	I/O	**Address/Data:** A 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one cycle, and which is used to transmit data between this device and external memory resources on other cycles. Bus transactions on this bus are logically separated into two phases: during the first phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of: **Address(31:4):** The high-order address for the transfer is presented. **$\overline{BE}$(3:0):** These strobes indicate which bytes of the 32-bit bus will be involved in the transfer. During write cycles, the bus contains the data to be stored and is driven from the internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single word transaction or in a burst of four words, and places it into the on-chip read buffer.
Addr(3:2)	O	**Low Address (3:2)** A 2-bit bus which indicates which word is currently expected by the processor. Specifically, this two bit bus presents either the address bits for the single word to be transferred (writes or single word reads) or functions as a two bit counter starting at '00' for burst read operations.
Diag(1)	O	**Diagnostic Pin 1.** This output indicates whether the current bus read transaction is due to an on-chip cache miss, and also presents part of the miss address. The value output on this pin is time multiplexed: **Cached:** During the phase in which the A/D bus presents address information, this pin is an active high output which indicates whether the current read is a result of a cache miss.The value of this pin at this time in other than read cycles is undefined. **Miss Address (3):** During the remainder of the read operation, this output presents address bit (3) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.
Diag(0)	O	**Diagnostic Pin 0.** This output distinguishes cache misses due to instruction references from those due to data references, and presents the remaining bit of the miss address. The value output on this pin is also time multiplexed: **I/$\overline{D}$:** If the "Cached" Pin indicates a cache miss, then a high on this pin at this time indicates an instruction reference, and a low indicates a data reference. If the read is not due to a cache miss but rather an uncached reference, then this pin is undefined during this phase. **Miss Address (2):** During the remainder of the read operation, this output presents address bit (2) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.
ALE	O	**Address Latch Enable:** Used to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by external logic to capture the address for the transfer.
$\overline{DataEn}$	O	**Data Input Enable:** This signal indicates that the A/D bus is no longer being driven by the processor during read cycles, and thus the external memory system may enable the drivers of the memory system onto this bus without having a bus conflict occur. During write cycles, or when no bus transaction is occurring, this signal is negated.

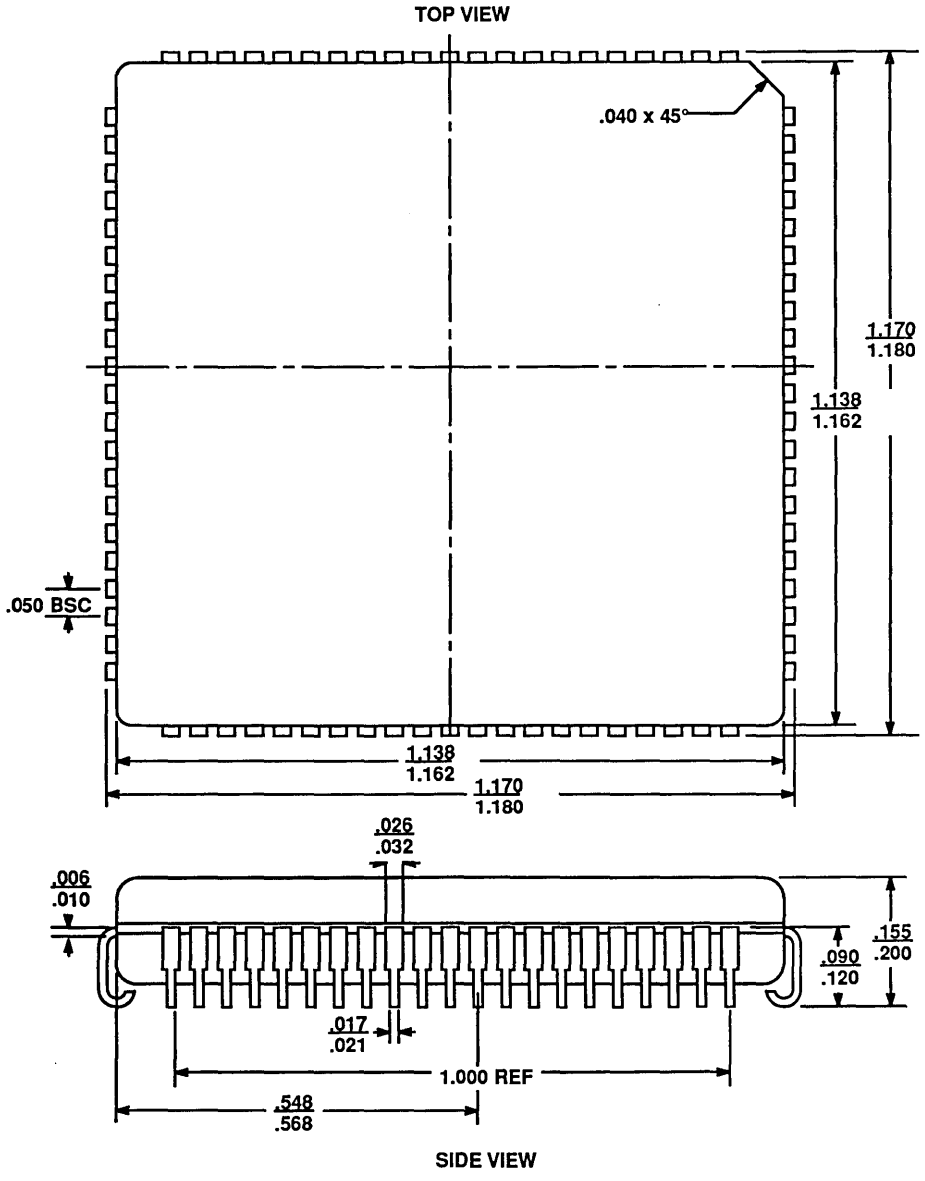
PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
Burst/ WrNear	O	**Burst Transfer/Write Near:** On read transactions, this signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if selected at device reset time. On write transactions, this output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 256 byte page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs.
Rd	O	**Read:** An output which indicates that the current bus transaction is a read.
Wr	O	**Write:** An output which indicates that the current bus transaction is a write.
Ack	I	**Acknowledge:** An input which indicates to the device that the memory system has sufficiently processed the bus transaction, and that the CPU may either advance to the next write buffer entry or process the read data.
RdCEn	I	**Read Buffer Clock Enable:** An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
SysClk	O	**System Reference Clock:** An output from the CPU which reflects the timing of the internal processor sys clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit.
BusReq	I	**DMA Arbiter Bus Request:** An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master.
BusGnt	O	**DMA Arbiter Bus Grant.** An output from the CPU used to acknowledge that a BusReq has been detected, and that the bus is relinquished to the external master.
SBrCond(3:2) BrCond(1:0)	I	**Branch Condition Port:** These external signals are internally connected to the CPU signals CpCond(3:0). These signals can be used by the branch on co-processor condition instructions as input ports. There are two types of Branch Condition inputs: the SBrCond inputs have special internal logic to synchronize the inputs, and thus may be driven by asynchronous agents. The direct Branch Condition inputs must be driven synchronously.
BErr	I	Bus Error: Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.
Int(5:3) SInt(2:0)	I	**Processor Interrupt:** During operation, these signals are logically the same as the Int(5:0) signals of the R3000. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals of the R3000. There are two types of interrupt inputs: the SInt inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The other interrupt inputs are not internally synchronized. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts.
Clk2xIn	I	**Master clock Input:** This is a double frequency input used to control the timing of the CPU. Internally, the clock generator unit derives the four processor "2xclk" signals from this clock.
Reset	I	**Master Processor Reset:** This signal initializes the CPU. Mode selection is performed during the last cycle of reset.
Rsvd(4:0)	I/O	**Reserved:** These five signal pins are reserved for testing and for future revisions of this device. Users must not connect these pins.

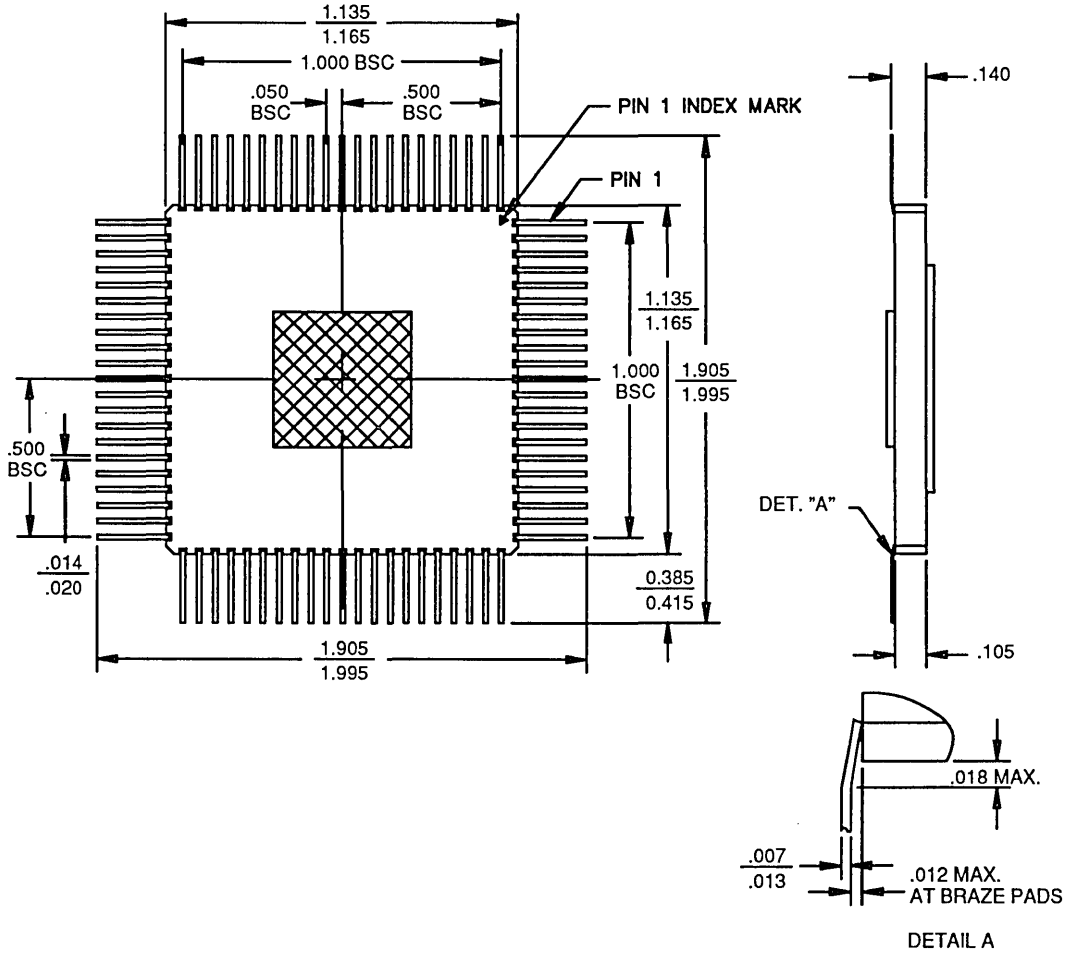
ORDERING INFORMATION



PACKAGE DIMENSIONS
84-LEAD CERQUAD (J BEND)

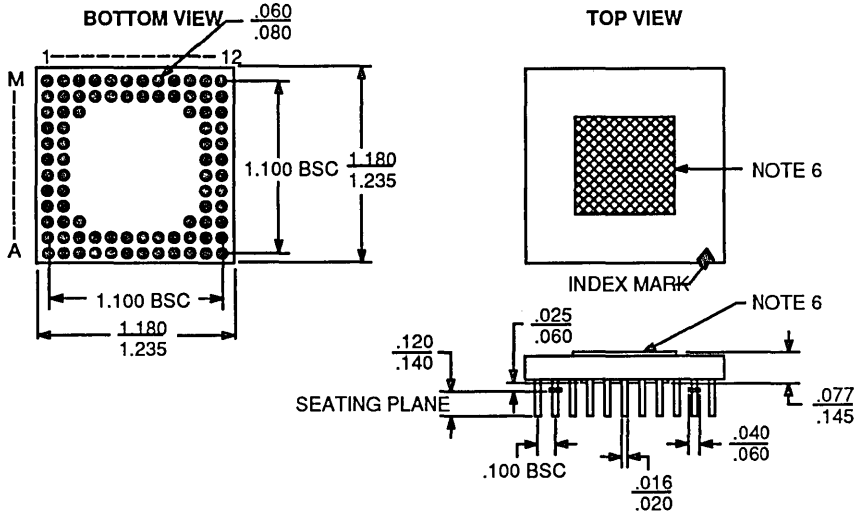


PACKAGE DIMENSIONS
84-LEAD FLATPACK (CAVITY DOWN)

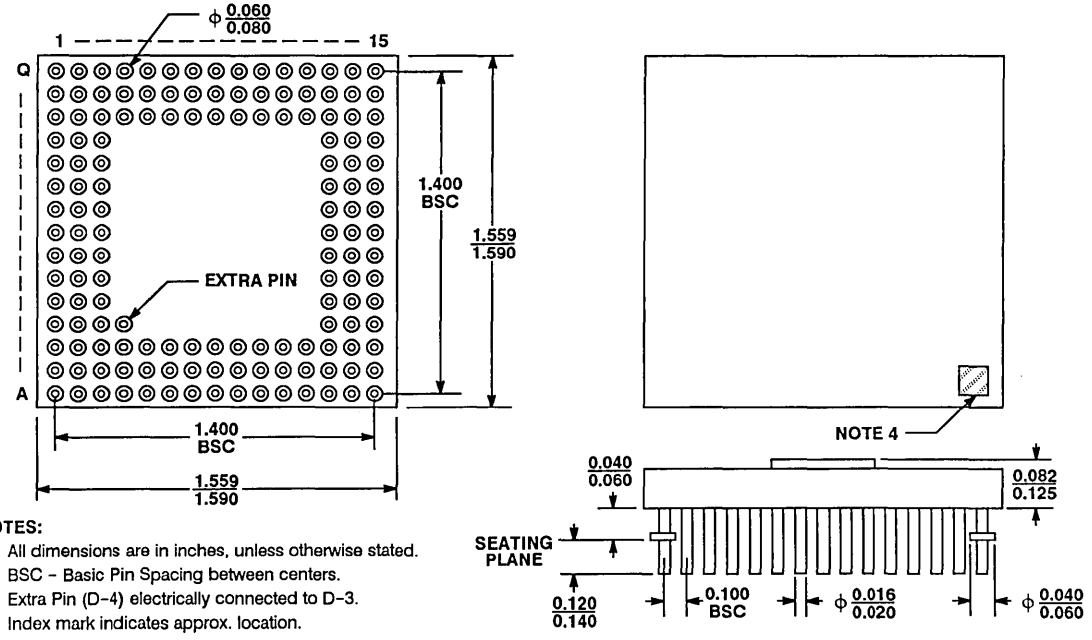


NOTES:
1. All dimensions are in inches, unless otherwise specified.
2. BSC — Basic lead spacing between centers.
3. Cross hatched area indicates intergrall metallic heat sink.

PACKAGE DIMENSIONS
84-PIN PGA (CAVITY DOWN)

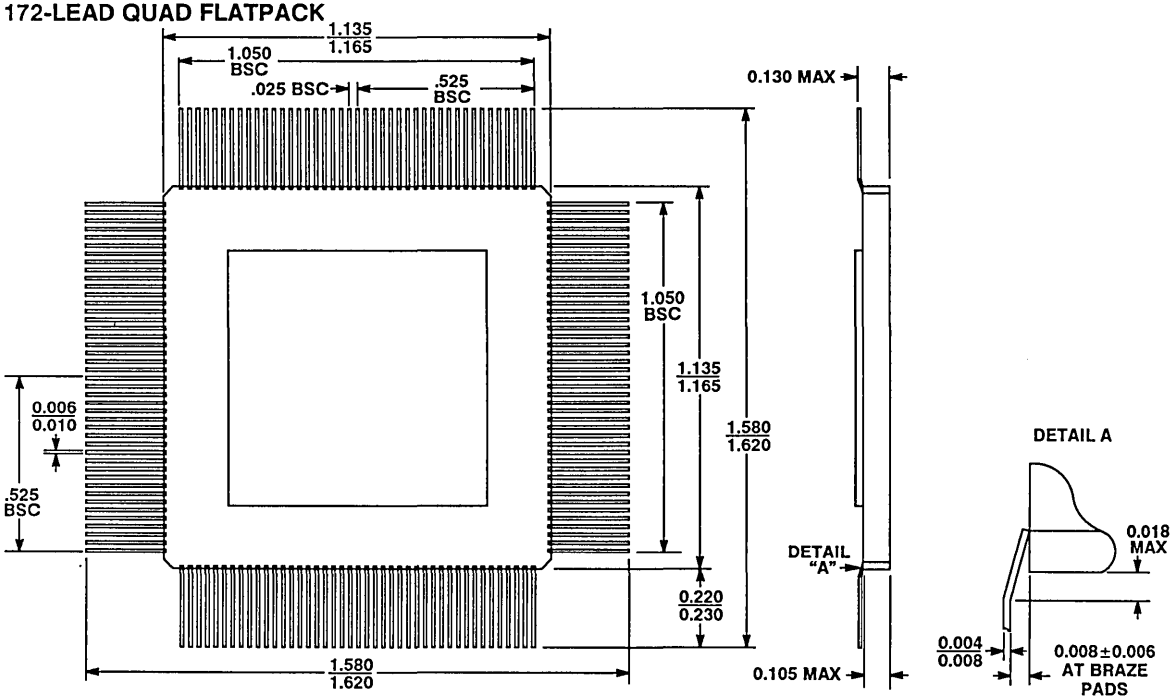


144 Pin PGA



NOTES:
1. All dimensions are in inches, unless otherwise stated.
2. BSC - Basic Pin Spacing between centers.
3. Extra Pin (D-4) electrically connected to D-3.
4. Index mark indicates approx. location.

PACKAGE DIMENSIONS
172-LEAD QUAD FLATPACK



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