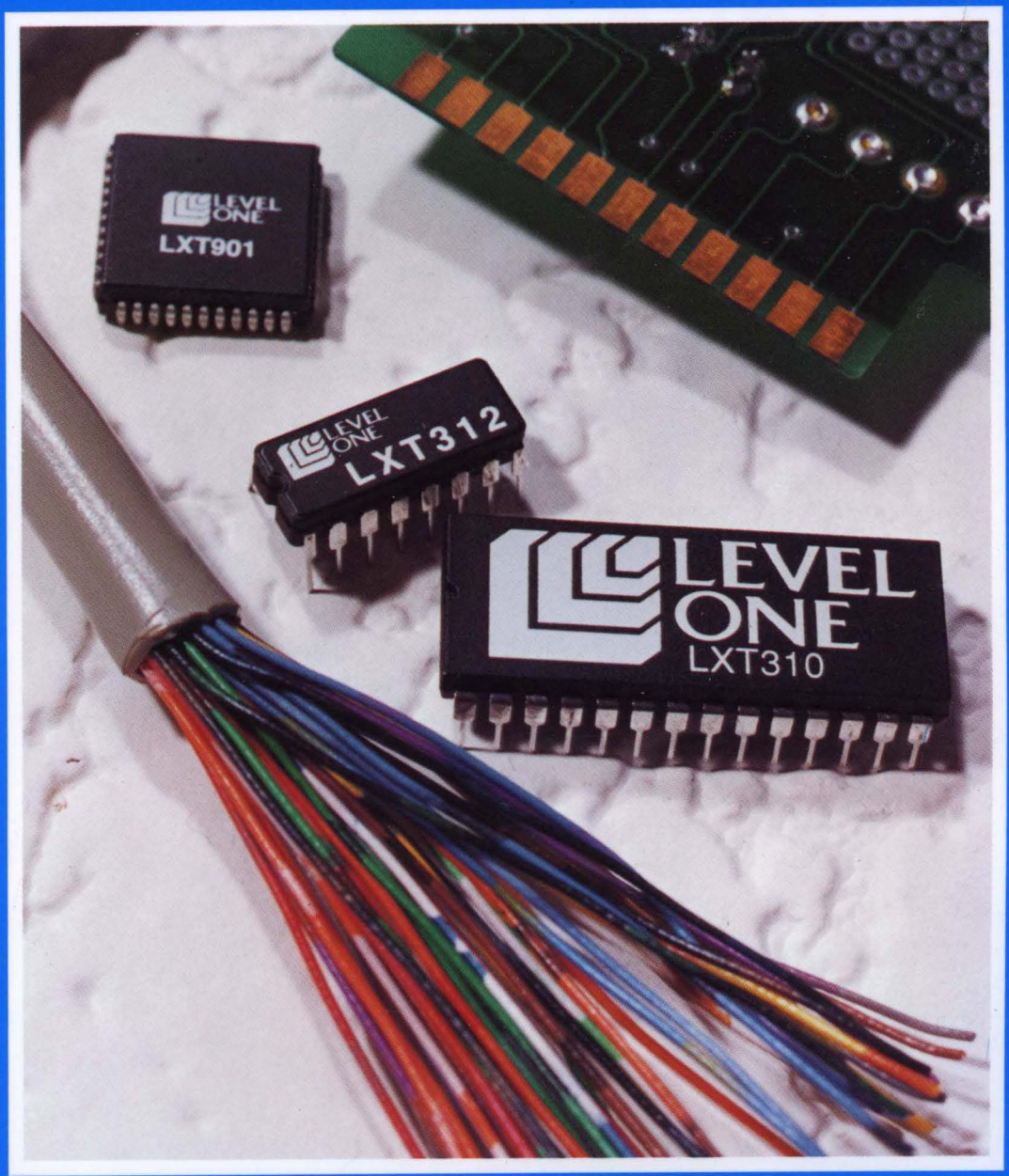
LEVEL ONE

Communications Data Book - 1994

Communications

Data Book

1994



LEVEL ONE

The Level One Credo

Our Mission — **We shall strive to be the leader in supplying Silicon Connectivity solutions and to provide a fair return on investment to our shareholders while being a responsible corporate citizen in our community.**

Our Quality Goal — **We shall strive to achieve Total Customer Satisfaction.**

Our Pledge — **We pledge to both external and internal customers that we shall strive to anticipate, understand, and fulfill their needs. We shall continuously improve each of our work functions to enhance the value of our products and services.**

Robert S. Pepper

Robert S. Pepper, Ph.D.
President and CEO

The industry's leading producer of mixed-signal silicon connectivity solutions for high-speed digital communications networks

1994 Data Book

Product Status Indicators

In this publication the designations Advance, Preliminary and Standard are used as follows:

Advance Information	indicates a product still in the design cycle. Any specifications listed are engineering targets only.
Preliminary Information	indicates a product which has not been released to production. Some specifications may be changed or added after full qualification and production release.
Standard Product	indicates a product which has been qualified and released to production.

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General Information

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LEVEL ONE®

Level One

Providing Silicon Solutions for Communications Connectivity

Mission

Level One Communications, Inc. of Folsom, California, is a rapidly growing dedicated producer of silicon solutions for complex mixed-signal (analog and digital) communications and networking connectivity applications. The company is a recognized leader specializing in the development of very large scale integrated circuit (VLSI) Application Specific Standard Products (ASSPs), such as transceivers, repeaters and related devices used in two key areas of the rapidly-expanding telecommunications and data communications industry:

1) Connectivity solutions for Digital Transmission systems, including fast-growing T1/E1 and
2) Connectivity solutions for Networking systems including Local and Wide Area Networks (LAN/WAN) such as Ethernet 10Base T; datacom, and digital modems.

A majority of the devices in Level One's product line include complex functions incorporated on single silicon chips for applications formerly requiring multiple chip sets or board level solutions.

Market Data

With several patents, the company provides a wide variety of proprietary problem-solving silicon connectivity solutions in today's $2.7 billion mixed-signal IC market which is projected to grow at a compounded rate of 30 percent annually and exceed $5 billion by 1997, according to VLSI Research. The two major market segments currently served by Level One's products are expected to grow from $800 million in 1992 to more than $2.8 billion by 1997.

History

Level One was founded in December 1985. The company's principal investor is Warburg, Pincus Capital Company of New York. As its name implies, Level One's initial focus was on the physical layer ("layer one") of the Open Systems Interconnection (OSI) seven-layer network reference model developed by the International Standards Organization (ISO). In August, 1993 the company completed an initial public offering. A secondary offering was completed in February, 1994. Level One is traded on the NASDAQ exchange under the symbol LEVL. The company currently occupies two buildings in a Folsom, CA business park. In April, 1994, Level One plans to move to a new 60,000² ft. facility.

Forward Migrations

Today Level One is adding value to its portfolio of more than 50 products by integrating solutions encompassing higher layers of the OSI model into its ICs at the data transfer/conditioning layer (layer two), as well as the network switching, routing and controller layer (layer three). Level Ones's products today are aimed directly at the growing digital telecom/datacom connectivity markets. These Level One solutions are essential in an age when new technologies and customer demand are increasing the need for higher transmission speeds and greater system performance.

As demand increases for higher transmission speeds, moving from the upper limit of the analog/voice domain (at 64 kilobits per second) to the gigabit level and even beyond, Level One will continue to implement its product migration strategy by developing mixed analog/digital signal processing devices required at these higher bit rates. The technologies and IC design techniques Level One has perfected for baseband short- and long-haul transmission markets are also applicable in the development of products for use in broadband coaxial cable and fiber optic systems.

The Electronic Superhighway
Level Ones's advanced silicon connectivity solutions are key building blocks of tomorrow's voice/data network and the chief enablers of the national information superhighway linking homes and businesses across the nation and around the globe.

Revenue Growth & Profitability
Level One's revenue growth rate has been exceptional. In 1991, product revenues were 400% greater than 1990, and 1992 revenues were 175% greater than 1991. Product revenue for 1993 shows a 105% growth compared with the previous year. The company has enjoyed consistent profitability since the first quarter of 1992.

Capitalization
Level One today has a total capitalization approaching $50 million, including proceeds from the initial and secondary public offerings. The two offerings, coupled with consistently increasing earnings and growth, have placed the company on a firm financial foundation which Level One can leverage successfully in advancing to the next stage of corporate development.

Differentiation
Level One fills a unique niche in the mixed-signal market. Level One made its reputation first in the ubiquitous copper wire universe (which is still far and away the dominant industry sector for WAN and LAN applications) while also preparing to address the needs of non-copper transmission. This strategy will continue to guide Level One's growth as the Regional Bell Operating Companies (RBOC) and other leading telephone companies work with cable television providers to provide a full service network in the years ahead. The company expects that the need for connectivity and interoperability across baseband and broadband networks will require the mixed-signal silicon connectivity solutions provided by Level One.

Installed Plant
While the top 12 telecommunications companies in America today (telephone and cable TV) have a total combined installed plant of 430,000 miles of coaxial cable and 6.18 million miles of fiber optic cable (as reported in Fortune's April 19, 1993 issue), there is a total of 1.325 billion miles of copper in place in the franchise territories of the eight largest telephone companies alone. As fiber/coax installations increase (as evidenced by cable giant Tele-Communications, Inc.'s {TCI} plans to spend $2 billion on an eight-city fiber hub expansion program and PacTel's announcement of a $16 billion fiber/coax deployment in the San Francisco Bay Area), Level One is positioning itself to serve this expanding market.

New Applications
In order to implement the growing number of advanced interactive, multimedia, and enterprise networking applications*, there is increasing demand for mixed-signal silicon connectivity solutions to leverage the extensive existing investments in the installed copper wire base, while — at the same time — gearing up to provide solutions to serve the growing needs of the future mixed media and coax/fiber worlds. Level One is positioning itself to capture a significant share of each market sector.

(*Applications include, but are not limited to: videoconferencing; Group IV Fax; educational services; telecommuting, image retrieval; modem pooling; teleconferencing; wide area connectivity; secure voice; leased line backup; desktop conferencing; file transfer; PC access; distributed computing; remote LAN; CAD, CAE, and CAM.)

Industry Leadership
Major ingredients of a firm's success can be found in the number of industry leadership positions a company achieves for itself, as well as by

the number of industry "firsts" and exclusive, sole-source products it develops. Level One maintains an extensive, ongoing research and development program to develop state-of-the-art silicon solutions for the mixed-signal, analog/digital transmission and networking markets. The company's R&D program has already yielded significant successes as evidenced by this partial list of Level One's accomplishments:

Transmission Achievements

- A world leader in twisted-pair telecom/datacom transceivers.
- Worlds' first supplier of long-haul T1 transceivers with a one-chip CSU for networking applications.
- A complete line of fully integrated T1/E1 short-haul transceivers
  (Level One is the number one supplier in this market).
- The industry's only fully-integrated quad T1/E1 receivers used in the growing SONET multiplexing and T1/E1 test, monitoring and performance market.
- Exclusive worldwide provider of integrated Clock Rate Adapters for E1 and T1 interfaces.
- The world's first integrated T1 and E1 repeater chips based on four Level One patents. Today Level One offers four repeaters: single T1, dual T1, single E1 and dual E1.
- Organized consortium of leading manufacturers to develop chips compliant with the new industry standard for high-speed digital subscriber loop interface at T1 or E1 speeds, the HDSL Data Pump.

Networking Achievements

- Developed the world's first fully integrated extended range transceivers for Switched 56 service and Dataphone Digital Service (DDS).
- Supports the rapid growth of the LAN market with new 10Base T Ethernet network interface connectivity designs.
- Introduced a single chip Media Attachment Unit (MAU) used to connect to an Ethernet LAN and a hub transceiver for multipoint repeaters. Level One is now one of the world's top three 10Base T MAU suppliers.
- The industry's first Ethernet twisted-pair-to-coaxial-cable adapter IC.
- The first firm (in 1992) to address the data communications industry's electromagnetic interference needs by integrating transmit filter functions onto a chip.
- Developed the first multiport quad hub repeater chip, the LXT914, with integrated transmit filters for 10Base T networks.

Unique Design and Modeling / Simulation Systems

At the heart of Level One's new product development effort is a world class team of communications mixed-signal silicon design specialists. They comprise a "rare breed" among today's engineering school graduates who are very much in demand among developers of telecom/datacom chip-level components and also among original equipment manufacturers for today's networks.

To assist this team in its R&D pursuits, Level One has developed a state-of-the-art, proprietary Computer Aided Design (CAD) system as well as a software modeling and simulation system (LxWAVE™) that enables it to design and test complete VLSI circuits in a fraction of the time it usually takes to bring new semiconductor products to market — and with fewer design revisions than competitors require.

Level One knows of no other company in the world that has a modeling system to rival LxWAVE, a proprietary software simulation tool used to model both the physical-level communications system and the associated metallic transmission networks. LxWAVE has two parts: LxNET™ and LxSYS™. LxNET is transmission simulation software modeling dispersion and attenuation of baseband signals for a given set of twisted pair transmission line characteristics. LxSYS is software designed to simulate the

system of interrelated functional blocks, and models the transceiver's resulting behavior and performance. Together LxNET and LxSYS accurately predict system-level performance of actual transmission networks. These software tools, combined with very powerful automatic test equipment, enable Level One to test its ICs as if they were transmitting in the real world.

Market Positioning

Level One's goal is to become the prime source for the best performing, highest quality IC products in the industry delivered on time with strong field backup support and better customer relations than any other semiconductor provider in the market.

The company is focused on finding silicon connectivity solutions for system needs in the most cost-effective manner. To maintain its leadership position, Level One strives to continue to reduce the cost of its products and to provide its customers with higher added-value silicon connectivity solutions.

Quality and Reliability Assurance

Extremely stringent quality standards are mandated by Level One's CEO, and are every employee's responsibility. Level One's quality and reliability assurance focus starts at the product definition stage and continues through every aspect of product design, manufacture, testing and customer support.

Level One is committed to producing products of exceptionally high quality and reliability. A quality semiconductor device meets or exceeds specifications and is delivered on time. A reliable semiconductor device continues to conform to specifications over the life of the equipment of which it is a part.

Quality and reliability cannot be inspected in, screened in or tested in — they must be **built-in** to each device. Building in quality and reliability starts with the initial specification and proceeds through design and production.

The company has developed an exacting quality assurance process that has proven successful in reducing failure rates to an absolute minimum for the more than five million silicon connectivity ICs produced by the company to date. A rigorous program of foundry and assembly selection, audit and qualification — as well as internal controls — ensures a consistent supply of high quality and reliable devices.

The company establishes a benchmark performance level all foundries and assemblies must meet and maintain in order to both qualify for, and continue to comply with, the company's exacting, state-of-the-art manufacturing and production standards. Level One, and all of its affiliated foundries and assemblies, have an objective of being ISO 9000 compliant by the end of 1994.

Low Failure Rates

The success of Level One's quality and reliability assurance program is demonstrated by the company's extremely low failure/return rate. Level One's return rate is less than .4 percent of annual sales, which is much better than the semiconductor industry goal of under 1 percent of annual sales. The average mean time before failure (MTBF) for Level One's ICs is in excess of 10 million hours.

Multiple Foundry Strategy

Level One's flexible design methodology utilizes multiple independent silicon foundries — in the U.S. as well as offshore — to fabricate its integrated circuits. This enables Level One to optimize its manufacturing base to take advantage of process innovations and production schedules. This strategy also reduces total reliance on a single source and provides a backup mechanism to ensure on time product delivery.

Quality and Reliability

Designing in Quality

Level One has developed a unique approach to transceiver design and testing. This approach enables us to ensure that all of the devices we manufacture meet performance specifications. Using our proprietary simulation tool, LxWAVE™, we generate analog signals that model transmission through various networks and systems. This enables Level One to test designs and finished devices under simulated worst-case conditions to ensure performance to specifications in extremely demanding scenarios.

LxWAVE consists of two simulation tools: LxNET™ and LxSYS™. LxNET starts with a transmission line model using stored transmission line parameters, many of which are actual laboratory measured values. Level One has constructed a wide variety of line models of various gauges and including single and multi-pair bundles. The transmission loop environment can then be modeled by simulating the effect of topology on the transmission network. The topology can include transformers, inductors, capacitors, resistors, active circuitry, bridge taps and other external disturbers. With a given line model, LxNET calculates the response of the loop anywhere along the loop.

LxSYS, the second part of LxWAVE, simulates the behavior of the transceiver in design. To construct the behavior model, LxSYS uses software modules corresponding to circuitry in the Level One design library. Jitter and noise, analog offsets and nonlinearities, and bandwidth limitations may also be added.

In the design stage, Level One engineers use LxWAVE to simulate the response of the transceiver for various inputs and under various operating conditions. With these responses, we develop a template defining the range into which the transceiver's output should fall. These templates are saved for later testing.

Designing In Reliability

During design, the reliability aspect of the device is as important to Level One as performance, die size, and yield. Therefore, Level One has established design/layout rules and guidelines aimed at ensuring reliability. These guidelines are followed carefully for all Level One designs; they are updated as required by failure analysis history or process changes.

Design and layout guidelines used for Level One designs are intended to ensure reliable circuit operation. Included in the guidelines are rules intended to reduce susceptibility to latch-up, enhance circuit ESD robustness, avoid trace and contact electromigration, ensure dielectric integrity, reduce metal stress and provide compatibility with packaging. These guidelines are determined in conjunction with the wafer foundries to guarantee compatibility with their processes. Packaging and assembly related guidelines are developed with the assembly house to enhance package reliability and die protection.

In addition, Level One designs are very conservative. Chip components are never designed to the limits of process capabilities or operated under conditions that could lead to instability. Designs are subjected to in-depth circuit simulation at temperature, voltage and processing extremes before being committed to silicon. In order to guarantee operation at these extremes, circuit designs must be conservative.

Level One devices are designed for fabrication at several different foundries. The processes used by these different foundries are similar, but not identical. Therefore, our designs must be able to encompass the process differences between foundries. This results in devices less sensitive to variations that may occur during processing or during the life of the device.

Foundry and Assembly House Qualification

The process of choosing and qualifying a wafer foundry or an assembly house starts long before any product is built at the facility. Each contractor is studied in detail to assure compatibility with Level One requirements. Factors examined at an assembly house include: package capabilities; attach types; temperature profiles; mold compound and epoxy types; inspections; process control; and quality procedures.

Foundries are evaluated for their ability to produce Level One designs. The foundry's device models or Level One generated models are used to determine the foundry's compatibility. Extensive simulation is performed at process, voltage and temperature extremes to ensure circuit functionality. The process flow and construction topology are evaluated for top coat effectiveness; glassivation and metallization step coverages; effectiveness of planarization; electromigration performance; etc. Reliability data is evaluated for compliance with Level One reliability requirements.

The manufacturing and quality procedures followed by the foundry are evaluated carefully to be sure they can control the process to Level One specifications. Also, complete lot traceability must be retained.

Finally, both the foundry and the assembly house must be committed to constant quality improvement through the use of control charts, quality groups, and corrective/preventive actions on any anomalies reported by customers. Currently, the company has qualified foundries in North America, Europe and Asia. Multiple foundries reduce the risks associated with dependency on a single vendor.

Level One assembly in ceramic and plastic DIP, PLCC, TQFP and PQFP packages is currently being handled by assembly houses in Asia, Europe and the USA.

Contractor Control

Contractor control is important to ensure consistent performance. Control is a continuous process, accomplished through a multifaceted approach. Contractor surveillance is an important part of the Level One standard product flow. Electrical measurements of basic transistor and topology structures are examined for each wafer lot received. Each incoming packaged device lot is subjected to material verification, inspection, and QC monitor report review. In addition, incoming wafer and packaged device lots are visually inspected on a sample basis. Any anomalies or trends are detected and reported early in the process.

Periodically, Level One audits foundry and assembly house process monitor and control procedures, quality monitoring, and incoming material quality assurance.

Product Qualification

Level One products must undergo a strenuous qualification procedure before production shipments begin. Product qualification includes: establishment of functional and parametric test procedures; qualification of the device; qualification of the process to be used; and qualification of the package.

A device built using a new foundry or a new assembly house must undergo the most encompassing qualification procedure. Because subsets of the qualification procedure are specific to foundry processes and packages, products using pre-qualified processes or packages require qualification only of the portions of the procedure not satisfied by prior qualification. Every qualified product is capable of meeting each applicable qualification requirement.

Among the tests and stresses included in the qualification procedure are the following:

- operating life tests
- Temperature Humidity Bias (THB) 85°C/85% RH or 130°C/85% RH
- autoclave
- temperature cycling
- thermal shock
- latch-up immunity
- ESD susceptibility
- package and lead mechanical integrity testing
- hermeticity

Such comprehensive testing stresses the device design, process and package. For example, operating life tests stress the device with bias (in a static or dynamic mode) at elevated temperatures to accelerate possible failure mechanisms that could occur during the life of the device. Failure mechanisms accelerated during life testing include parameter shifts, leakages, electromigration and oxide defects. These failure mechanisms have been thoroughly studied, and found to follow the Arrhenius relationship for reaction rate acceleration with temperature. This enables Level One to simulate life at a nominal operating temperature in a relatively short time.

Autoclave and THB tests are used to evaluate the resistance to moisture of devices packaged in plastic. The ability of the package to protect the die is evaluated in autoclave, in an unbiased, high temperature, pressurized steam environment. Metallization corrosion is the dominant failure mechanism. Bias-dependent moisture effects are enhanced through THB, which is a humid (85% RH), high temperature (85°C or 130°C) environment. Failure mechanisms include metallization corrosion, leakages and voltage shifts. The package, process and circuit design are all stressed with THB.

Package and bond integrity are evaluated using temperature cycling, thermal shock, and package and lead mechanical testing

Destructive physical analysis (DPA) is used to evaluate the details of construction, workmanship, and potential reliability. In this analysis, the package and/or die is dissected and examined in detail, using X-ray, optical microscopy, and scanning electron microscopy. Items such as bond wire dress, ball formation, die attach, lead frame, package or mold compound, passivation integrity, die construction and workmanship are analyzed.

Product Monitoring

After a product is qualified, Level One's product monitoring program continues to verify quality and long-term reliability. Under this program, the Quality and Reliability Department takes periodic samples of the product from finished goods and subjects them to selected product qualification tests. Process related tests are performed on a quarterly basis. Each process/foundry used in production is monitored separately. Package reliability testing is performed bi-annually. Each production package type/assembly is monitored individually.

The results of the reliability testing performed for the product monitoring program are published in Level One Reliability Reports.

An important area of product monitoring is reviewing failure history for indications of process or assembly anomalies. If trends are seen, the anomaly is identified through failure analysis, pinpointing possible process or assembly influences. Level One then implements corrective actions, working with the foundry or assembly house. Design rules and guidelines are modified, if necessary, to prevent future reoccurrence of the failure mechanism.

Production Flow

Production flow is shown in Figure 1. Level One participates in quality and reliability monitoring through each aspect of the production cycle by reviewing electrical and inspection data from the foundry and assembly house. At Level One, we perform all device testing (at the wafer and package level), as well as wafer and package inspections, using in-house expertise.

With each wafer lot, the foundry sends results of electrical measurements of basic transistor and topology structures. These measurements are reviewed by Level One Quality and Engineering and compared to specified values for the process. If the deviation falls outside the specification limits, the material is held until disposition by Quality. Feedback to the foundry is immediate, and a mutually-agreed-upon corrective action plan is executed.

A similar inspection and QC monitoring report is received with each assembled lot from the assembly house. This report is reviewed for each incoming lot.

When required, 100% burn-in is performed on the lot. Burn-in yield is monitored by statistical process control. When a lot is found to have burn-in yield outside the control limits, the lot is held until disposition by Quality. A lot sample burn-in is run on material that is not 100% burned-in. Lots that do not pass specific criteria are held until disposition by Quality.

Before disposition to box stock, the lot traveler is reviewed by Quality to ensure that all test, inspection and production steps have been performed.

A sample of the product must pass a rigorous quality acceptance test before authorization to ship is given. This testing, consisting of electrical and visual inspection, is performed by Quality. Upon successful completion of this test, authorization to ship is given by Quality.

By maintaining close working relationships with the foundries and assembly houses, Level One is involved throughout the production of the product.

Testing

All devices are 100% tested using parametric and functional tests using analog and digital test vectors from the LxWAVE simulator. Test vectors are downloaded to the production tester for incorporation into test programs. The analog and digital signals transmitted through various networks are reconstructed by the tester and used as stimuli to the device under test (DUT). Noise can be added to further evaluate the device's response under less than optimum operating conditions. The response is sampled by the tester and compared to the template constructed for the particular input stimulus.

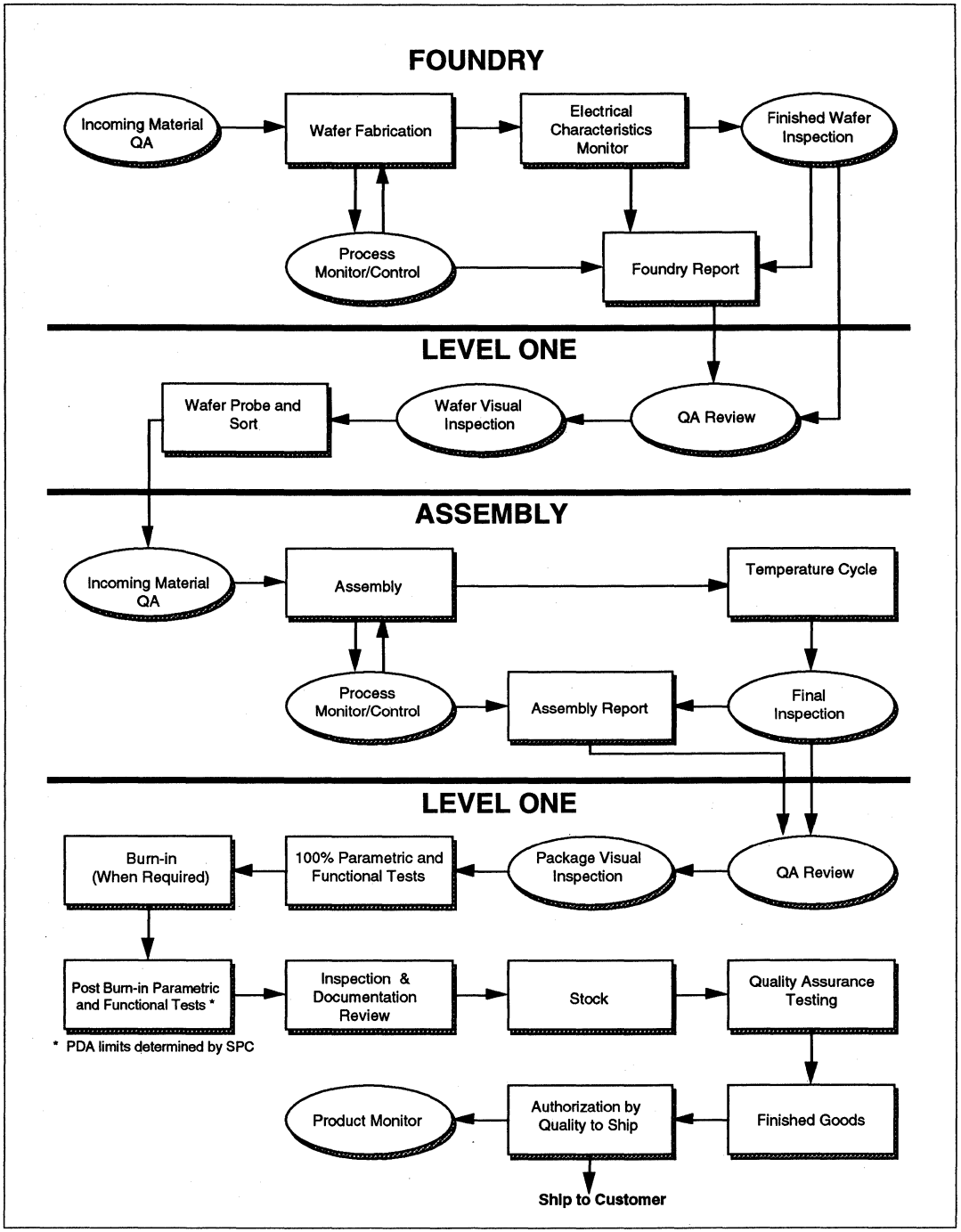
Using the simulated waveforms, the DUT is tested for response to various line lengths and superimposed noise amplitudes. Typically, the DUT is first tested with a "zero-length line" waveform as if the receiver and the driver were tied directly to one another. This is a functional test of the major blocks of the DUT. A worst-case waveform is applied next. This is simulation of a specified line length with noise superimposed on the signal. This ensures conformance to the specifications even under worst-case conditions.

These dynamic functional tests, combined with parametric tests, ensure that the devices are rigorously tested under various operating conditions without the use of cable spools or other hardware.

Product Traceability

To ensure traceability, each lot traveler tracks the product history including: foundry lot; assembly; inspections; tests; burn-in (if required); quality control and quality acceptance testing; and shipping destination. This documentation is retained for future reference. The lot traveler enables Level One to determine which lots were shipped to a particular customer. In addition, each device is branded with the lot number and a special trace code to enable complete traceability.

Figure 1: Level One Production Flow



Electrostatic Discharge

Electrostatic discharge (ESD) can damage sensitive semiconductor devices. Damage occurs unless precautions are taken to eliminate the generation of dangerous static levels, and to design robust circuitry with sufficient protection. Level One uses both approaches to ensure that the devices shipped to our customers are uncompromised, and that they will survive normal handling.

Level One's design guidelines for ESD protection produce devices which tolerate nominal ESD levels without damage. Before use in device designs, we test the susceptibility to ESD damage of standard input and output cells, using special Level One designed test circuits. In addition, the ESD susceptibility of each device type is determined as part of the product qualification before release to production.

Proper ESD handling of devices is policy at Level One. Those who handle devices are fully trained in the proper procedures for handling static-sensitive devices and know that handling devices incorrectly may damage them. Packaged devices are handled only at special workstations designed to eliminate damaging static levels. Packaged devices are shipped in containers designed to eliminate risk of damage caused by ESD.

Constant Improvement Program

To assure shipment of high-quality, highly reliable devices, Level One pursues constant improvement in all aspects of production and testing. For example, small group problem-solving teams have been assembled. The teams consist of personnel from both operations and quality, working together to solve problems and improve our manufacturing flow.

Transmission Products

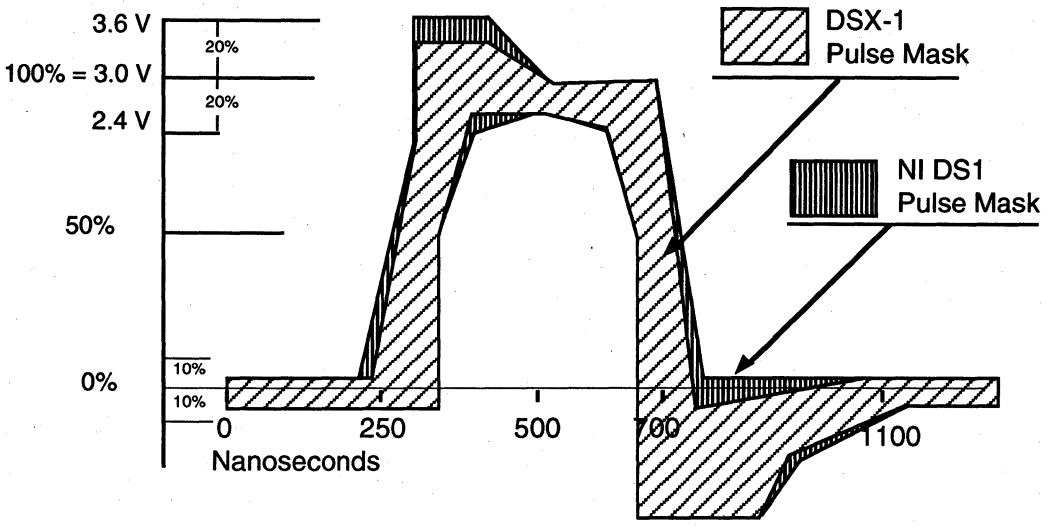
1994 Communications Data Book

LEVEL ONE®

Primary Rate Specifications

Function	DSX-1 (T1.403)	DS-1	E1 (G.703)	S2 (I.431)
Line Rate	1.544 MHz ± 200 B/S	1.544 MHz ± 75 B/S	2.048 MHz ± 50 ppm	2.048 MHz ± 50 ppm
Cable Length to DSX point	ABAM/655 ft	3000/6000 ft	350 m (1000 ft)	1000 m
Pulse Amplitude	2.4 - 3.6 V	2.4 - 3.6 V	2.37 V (±10%) Coax (75 Ω) 3.0 V (±10%) Twisted-Pair (120 Ω)	
Receive Attenuation	<10 dB	0 - 36 dB	0 - 6 dB at 1.024 MHz	0 - 18 dB at 1.024 MHz
Line Build-Out	Pre-Equalized Pulses	0.0, 7.5, 15 dB	No	No
Maximum Successive Zeros	15 (or B8ZS)	15 (or B8ZS)	HDB3 Code	HDB3 Code
Maximum Jitter	Worst Case: 138 UI @ 1 Hz 28 UI @ 100 Hz 10 UI @ 310 Hz	Worst Case: 138 UI @ 1 Hz 28 UI @ 10-300 Hz .4 UI @ 10 kHz	20-2400 Hz: 1.5 UI	N/A
Applicable Level One Transceivers	LXT300/301 LXT304A LXT305/305A Short Haul T1	LXT310 Long Haul T1	LXT300/301 LXT304A LXT305/305A Short Haul E1	LXT318 Long Haul E1

1.544 MHz DSX-1 Pulse Mask

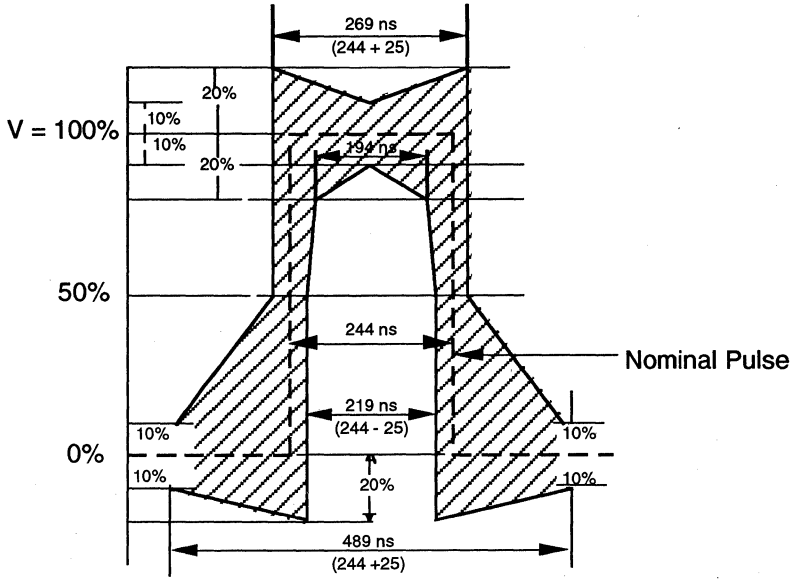


NOTE: The Network Interface DS1 spec is a relaxed version of the DSX-1 Pulse Mask which allows for cable loss between the equipment output and the Network Interface.

1.544 MHz T1 Pulse Mask Corner Point Specifications

DSX-1 Template				NI DS1 Template			
Maximum Curve		Minimum Curve		Maximum Curve		Minimum Curve	
Time (ns)	% V	Time (ns)	% V	Time (ns)	% V	Time (ns)	% V
0	5	0	-5	0	5	0	-5
250	5	350	-5	250	5	350	-5
325	80	350	50	325	80	350	50
325	115	400	95	325	120	400	90
425	115	500	95	425	120	500	95
500	105	600	90	500	105	600	90
675	105	650	50	675	105	650	50
725	-7	650	-45	725	5	650	-45
1100	5	800	-45	1100	5	800	-45
1250	5	925	-20	1250	5	896	-26
		1100	-5			1100	-5
		1250	-5			1250	-5

2.048 MHz E1 Pulse Mask



2.048 MHz E1 Pulse Mask Specifications

Parameter	Coaxial Cable	Shielded Twisted-pair	Units
Test load impedance	75	100	ohms
Nominal peak voltage of a mark	2.37	3	V
Peak voltage of a space	0 ± 0.237	0 ± 0.3	V
Nominal pulse width	244	244	ns
Ratio of amplitudes of positive and negative pulses at center of pulse	95 - 105	95 - 105	%
Ratio of widths of positive and negative pulses at nominal half amplitude	95 - 105	95 - 105	%

Short Haul T1/E1 Transceiver Overview

Function	LXT300	LXT301	LXT304A	LXT305A
Receiver Features	Data / Clock Recovery, Jitter Attenuation	Cata / Clock Recovery	Data / Clock Recovery Jitter Attenuation	Data / Clock Recovery
Transmitter Features	Line Driver	Line Driver	Line Driver	Line Driver Jitter Attenuation
Recommended Load	25 Ω typical	25 Ω typical	75 Ω typical	75 Ω typical
Transmit Return Loss	Fixed	Fixed	Adjustable	Adjustable
Loss of Signal Reset Condition	Detection of 1 mark	Detection of 1 mark	12.5% mark density 4 marks in 32 bits	12.5% mark density 4 marks in 32 bits
Number of E1 Equalizer Codes	1	1	2	2
µP Interface	Yes	No	Yes	Yes

LXT300 / LXT301

T1/E1 Integrated Short Haul Transceivers with Receive Jitter Attenuation

General Description

The LXT300 and LXT301 are fully integrated transceivers for both North American 1.544 MHz (T1), and European 2.048 MHz (E1) applications. Transmit pulse shapes (DSX-1 or E1) are selectable for various line lengths and cable types.

The LXT300 provides receive jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface. The LXT301 is pin compatible, but does not provide jitter attenuation or a serial interface.

Both transceivers offer a variety of diagnostic features including transmit and receive monitoring. Clock inputs may be derived from an on-chip crystal oscillator or digital inputs. They use an advanced double-poly, double-metal CMOS process and each requires only a single 5-volt power supply.

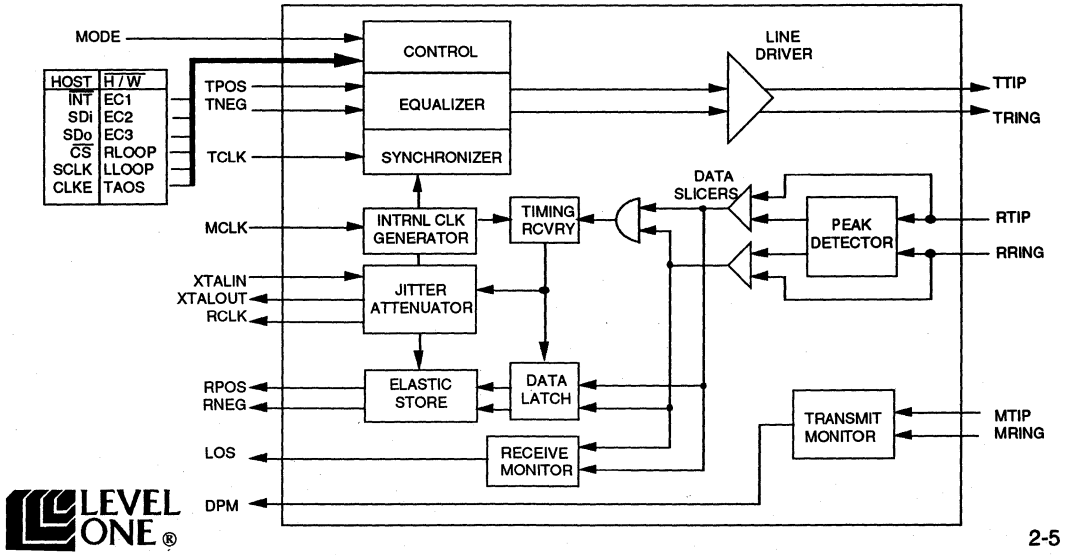
Applications

- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

Features

- Compatible with most popular PCM framers including the LXP2180A and LXP2181A
- Line driver, data recovery and clock recovery functions
- Receive jitter attenuation starting at 3 Hz meets or exceeds AT&T Pub 62411 (LXT300 only)
- LXT300 and LXT301 are pin compatible, and offer pin and functional compatibility with Crystal CS61574 (LXT300) and Crystal CS6158 (LXT301)
- Minimum receive signal of 500 mV
- Selectable slicer levels (E1/DSX-1) improve SNR
- Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- Local and remote loopback functions
- Transmit Driver Performance Monitor (DPM) output
- Receive monitor with Loss of Signal (LOS) output
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Microprocessor controllable (LXT300 only)
- Available in 28 pin DIP or PLCC

Figure 1: LXT300 Block Diagram



Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	–	6.0	V
Input voltage, any pin [1]	V_{IN}	RGND - 0.3	RV+ + 0.3	V
Input current, any pin [2]	I_{IN}	-10	10	mA
Ambient operating temperature	T_A	-40	85	°C
Storage temperature	T_{STG}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation not guaranteed at these extremes.
[1] Excluding RTIP and RRING which must stay within -6V to RV + 0.3V.
[2] Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100mA.

Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
DC supply [3]	RV+, TV+	4.75	5.0	5.25	V	
Ambient operating temperature	T_A	-40	25	85	°C	
Total power dissipation [4]	P_D	-	620	–	mW	100% ones density & maximum line length @ 5.25 V

[3] TV+ must not exceed RV+ by more than 0.3 V.
[4] Power dissipation while driving 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

Digital Characteristics (T_A = -40° to 85°C, V+ = 5.0 V ±5%, GND = 0 V)

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
High level input voltage [5,6] (pins 1-5, 10, 23-28)	V_{IH}	2.0	–	–	V	
Low level input voltage [5,6] (pins 1-5, 10, 23-28)	V_{IL}	–	–	0.8	V	
High level output voltage [5,6] (pins 6-8, 11, 12, 23, 25)	V_{OH}	2.4	–	–	V	I_{OUT}=- 400 µA
Low level output voltage [5,6] (pins 6-8, 11, 12, 23, 25)	V_{OL}	–	–	0.4	V	I_{OUT}=1.6mA
Input leakage current	I_{LL}	-10	–	+10	µA	
Three-state leakage current[5] (pin 25)	I_{3L}	-10	–	+10	µA	

[5] Functionality of pins 23 and 25 depends on mode. See Host / Hardware Mode descriptions.
[6] Output drivers will output CMOS logic levels into CMOS loads.

Analog Specifications (T_A = -40° to 85°C, V+ = 5.0 V ±5%, GND = 0 V)

Parameter		Min	Typ	Max	Units	Test Conditions
AMI Output Pulse Amplitudes	DSX-1	2.4	3.0	3.6	V	measured at the DSX
	E1	2.7	3.0	3.3	V	measured at line side
Recommended Output Load at TTIP and TRING		–	25	–	Ω	
Jitter added by the transmitter [7]	10Hz - 8kHz	–	–	0.01	UI	
	8kHz - 40 kHz	–	–	0.025	UI	
	10Hz - 40 kHz	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Sensitivity below DSX	(0dB = 2.4V)	13.6	–	–	dB	
		500	–	–	mV	
Loss of Signal threshold		–	0.3	–	V	
Data decision threshold	DSX-1	63	70	77	%peak	
	E1	43	50	57	% peak	
Allowable consecutive zeros before LOS		160	175	190	–	
Input jitter tolerance	10kHz - 100kHz	0.4	–	–	UI	
Jitter attenuation curve corner frequency [8]		–	3	–	Hz	

[7] Input signal to TCLK is jitter-free.
[8] Circuit attenuates jitter at 20 dB/decade above the corner frequency.

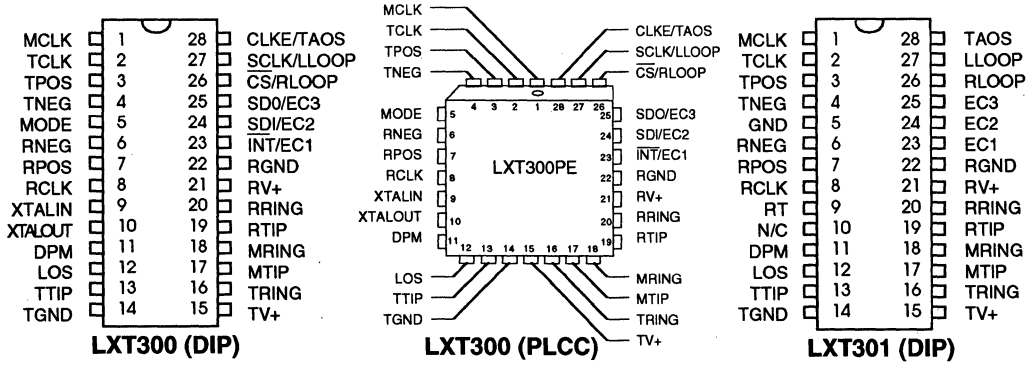


Table 1: Pin Descriptions

Pin #	Sym	I/O	Name	Description
1	MCLK	I	Master Clock	A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. *LXT300 Only: If MCLK not applied, this pin should be grounded.*
2	TCLK	I	Transmit Clock	Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is not supplied, the transmitter remains powered down.
3	TPOS	I	Transmit Positive Data	Input for positive pulse to be transmitted on the twisted-pair line.
4	TNEG	I	Transmit Negative Data	Input for negative pulse to be transmitted on the twisted-pair line.
5	MODE	I	Mode Select *(LXT300)*	Setting MODE to logic 1 puts the LXT300 in the Host mode. In the Host mode, the serial interface is used to control the LXT300 and determine its status. Setting MODE to logic 0 puts the LXT300 in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status.
	GND	-	- *(LXT301)*	Tie to Ground.
6	RNEG	O	Receive Negative Data	Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). Both outputs are stable and valid on the rising edge of RCLK. *LXT300 only: In the Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware mode both outputs are stable and valid on the rising edge of RCLK.*
7	RPOS	O	Receive Positive Data	
8	RCLK	O	Recovered Clock	This is the clock recovered from the signal received at RTIP and RRING.
9	RT	-	Resistor Termination *(LXT301)*	Connect to RV+ through a 1 kΩ resistor.

Table 1: Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
9	XTALIN	I	Crystal Input *(LXT300)*	An external crystal operating at four times the bit rate (6.176 MHz for DSX-1, 8.192 MHz for E1 applications with an 18.7pF load) is required to enable the jitter attenuation function of the LXT300. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and floating the XTALOUT pin.
10	XTALOUT	O	Crystal Output *(LXT300)*	
10	N/C	-	-- *(LXT301)*	No connection
11	DPM	O	Driver Performance Monitor	DPM goes to a logic 1 when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains at logic 1 until a signal is detected.
12	LOS	O	Loss Of Signal	LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when a mark is detected.
13	TTIP	O	Transmit Tip	Differential Driver Outputs. These outputs are designed to drive a 25 Ω load. The transmitter will drive 100 Ω shielded twisted-pair cable through a 2:1 step-up transformer without additional components. To drive 75Ω coaxial cable, two 2.2 Ω resistors are required in series with the transformer.
16	TRING	O	Transmit Ring	
14	TGND	-	Transmit Ground	Ground return for the transmit drivers power supply TV+.
15	TV+	I	Transmit Power Supply	+5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3V.
17	MTIP	I	Monitor Tip	These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another LXT300 or 301 on the board. *LXT300 only: To prevent false interrupts in the host mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-level voltage. The monitor clock can range from 100kHz to the TCLK frequency.*
18	MRING	I	Monitor Ring	
19	RTIP	I	Receive Tip	The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
20	RRING	I	Receive Ring	
21	RV+	I	Receive Power Supply	+5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	-	Receive Ground	Ground return for power supply RV+.

Table 1: Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
23	$\overline{INT}$	O	Interrupt *(Host Mode)*	This *LXT300 Host* mode output goes low to flag the host processor when LOS or DPM go active. $\overline{INT}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{INT}$ is reset by clearing the respective register bit (LOS and/or DPM.)
	EC1	I	Equalizer Control 1 *(H/W Mode)*	The signal applied at this pin in the *LXT300 Hardware mode and LXT301* is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
24	SDI	I	Serial Data In *(Host Mode)*	The serial data input stream is applied to this pin when the *LXT300* operates in the *Host mode*. SDI is sampled on the rising edge of SCLK.
	EC2	I	Equalizer Control 2 *(H/W Mode)*	The signal applied at this pin in the *LXT300 Hardware mode and LXT301* is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
25	SDO	O	Serial Data Out *(Host Mode)*	The serial data from the on-chip register is output on this pin in the *LXT300 Host mode*. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is high.
	EC3	I	Equalizer Control 3 *(H/W Mode)*	The signal applied at this pin in the *LXT300 Hardware mode and LXT301* is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
26	$\overline{CS}$	I	Chip Select *(Host Mode)*	This input is used to access the serial interface in the *LXT300 Host mode*. For each read or write operation, $\overline{CS}$ must transition from high to low, and remain low.
	RLOOP	I	Remote Loopback *(H/W Mode)*	This input controls loopback functions in the *LXT300 Hardware mode and LXT301*. Setting RLOOP to a logic 1 enables the Remote Loopback mode. Setting both RLOOP and LLOOP causes a Reset .
27	SCLK	I	Serial Clock *(Host Mode)*	This clock is used in the *LXT300 Host mode* to write data to or read data from the serial interface registers.
	LLOOP	I	Local Loopback *(H/W Mode)*	This input controls loopback functions in the *LXT300 Hardware mode and LXT301*. Setting LLOOP to a logic 1 enables the Local Loopback Mode.
28	CLKE	I	Clock Edge *(Host Mode)*	Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	I	Transmit All Ones *(H/W Mode)*	When set to a logic 1, TAOS causes the *LXT300 (Hardware mode) and LXT301* to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

Functional Description

The LXT300 and 301 are fully integrated PCM transceivers for both 1.544 MHz (DSX-1) and 2.048 MHz (E1) applications. Both transceivers allow full-duplex transmission of digital data over existing twisted-pair installations. Figure 1 is a simplified block diagram of the LXT300. The LXT301 is shown in Figure 2. The LXT301 is similar to the LXT300, but does not incorporate the Jitter Attenuator and associated Elastic Store, or the serial interface port.

The LXT300 and 301 transceivers each interface with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

Transmitter

The transmitter circuits in the LXT300 and 301 are identical. The following discussion applies to both models. Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 2. Refer to Table 3 and Figure 3 for master and transmit clock timing characteristics. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Equalizer Control signals are hard-wired to the LXT301.
LXT300 Only: Equalizer Control signals may be hardwired in the Hardware mode, or input as part of the serial data stream (SDI) in the Host mode.

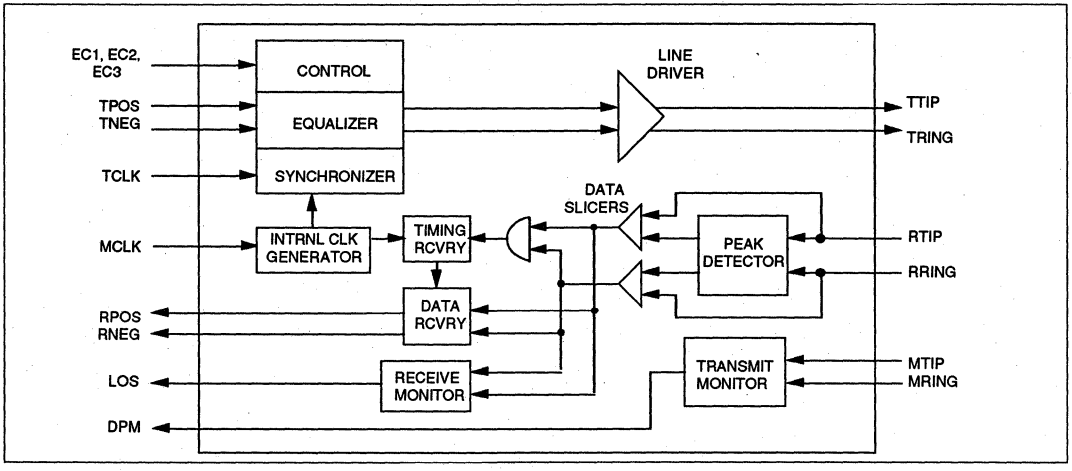
Pulses can be shaped for either 1.544 or 2.048 MHz applications. 1.544 MHz pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The LXT300 and 301 also match FCC and ECSA specifications for CSU applications. 2.048 MHz pulses can drive coaxial or shielded twisted-pair lines using appropriate resistors in line with the output transformer.

Table 2: Equalizer Control Inputs

EC3	EC2	EC1	Line Length[1]	Cable Loss[2]	Application	Frequency
0	1	1	0 - 133 ft ABAM	0.6 dB	DSX-1	1.544 MHz
1	0	0	133 - 266 ft ABAM	1.2 dB		
1	0	1	266 - 399 ft ABAM	1.8 dB		
1	1	0	399 - 533 ft ABAM	2.4 dB		
1	1	1	533 - 655 ft ABAM	3.0 dB		
0	0	0	CCITT Recommendation G.703		E1	2.048 MHz
0	1	0	FCC Part 68, Option A		CSU (DS-1)	1.544 MHz

[1] Line length from transceiver to DSX-1 cross-connect point.
[2] Maximum cable loss at 772 kHz.

Figure 2: LXT301 Block Diagram



Driver Performance Monitor

The transceiver incorporates a Driver Performance Monitor (DPM) in parallel with the TTIP and TRING at the output transformer. The DPM output level goes high upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

Line Code

The LXT300 and 301 transmit data as a 50% AMI line code as shown in Figure 4. Power consumption is reduced by activating the AMI line driver only to transmit a mark. The output driver is disabled during transmission of a space.

Table 3: LXT300 and 301 Master Clock and Transmit Timing Characteristics (See Figure 3)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Master clock frequency	DSX-1	MCLK	-	1.544	-	MHz	
	E1	MCLK	-	2.048	-	MHz	
Master clock tolerance		MCLKt	-	±100	-	ppm	
Master clock duty cycle		MCLKd	40	-	60	%	
Crystal frequency	DSX-1	fc	-	6.176	-	MHz	
LXT300 only	E1	fc	-	8.192	-	MHz	
Transmit clock frequency	DSX-1	TCLK	-	1.544	-	MHz	
	E1	TCLK	-	2.048	-	MHz	
Transmit clock tolerance		TCLKt	-	-	±50	ppm	
Transmit clock duty cycle		TCLKd	10	-	90	%	
TPOS/TNEG to TCLK setup time		t_{SUT}	25	-	-	ns	
TCLK to TPOS/TNEG Hold time		t_{HT}	25	-	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 3: LXT300 and 301 Transmit Clock Timing Diagram

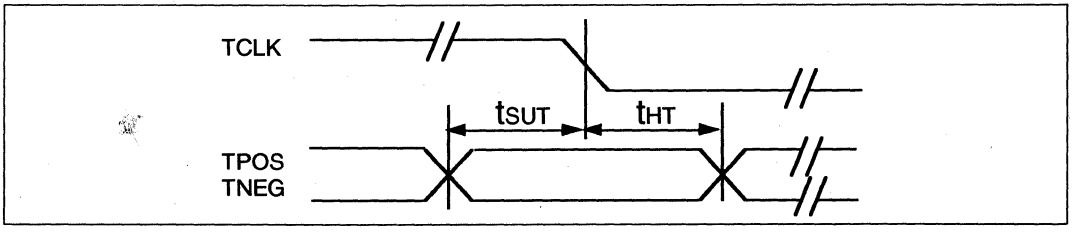
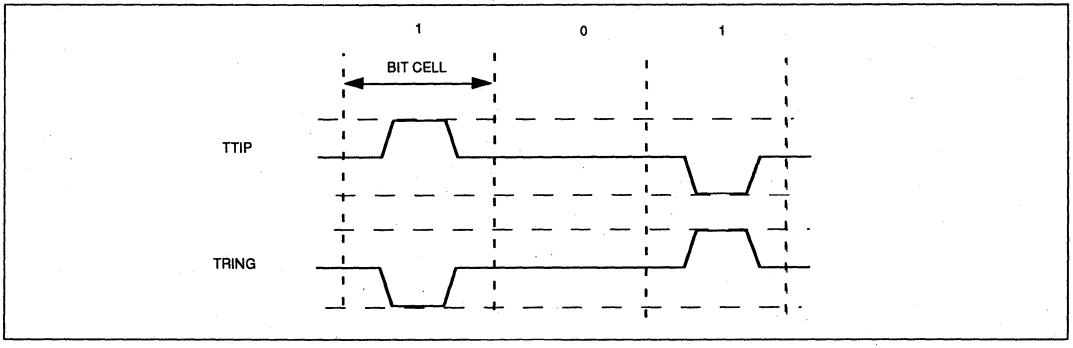


Figure 4: 50% AMI Coding Diagram



Receiver

The LXT300 and LXT301 receivers are identical except for the jitter attenuator and elastic store. The following discussion applies to both transceivers except where noted.

The signal is received from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Table 4 and Figure 5 for LXT300 receiver timing. LXT301 receiver timing is shown in Table 5 and Figure 6.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (determined by Equalizer Control inputs EC1 - EC3 ≠ 000) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (EC inputs = 000) the threshold is set to 50 %.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB). Regardless of received signal level, the peak detectors are held above a minimum level of .3 V to provide immunity from impulsive noise.

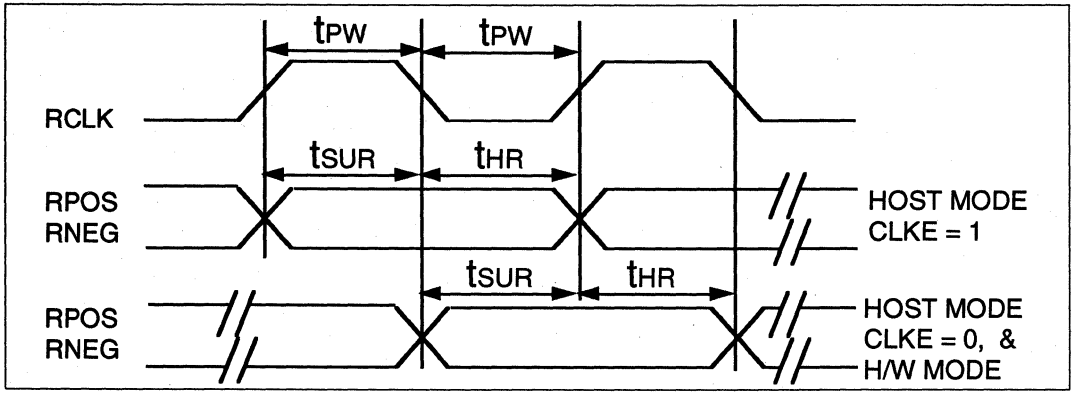
After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The receive monitor generates a Loss of Signal (LOS) output upon receipt of 175 consecutive zeros

Table 4: LXT300 Receive Characteristics (See Figure 5)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Receive slicer threshold	DSX-1	RST	65	70	75	%	
	E1	RST	45	50	55	%	
Receive clock duty cycle		RCLKd	40	-	60	%	
Receive clock pulse width	DSX-1	t_{PW}	-	324	-	ns	
	E1	t_{PW}	-	244	-	ns	
RPOS / RNEG to RCLK	DSX-1	t_{SUR}	-	274	-	ns	
rising setup time	E1	t_{SUR}	-	194	-	ns	
RCLK rising to RPOS /	DSX-1	t_{HR}	-	274	-	ns	
RNEG hold time	E1	t_{HR}	-	194	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 5: LXT300 Receive Clock Timing Diagram



(spaces). The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and the RCLK output is replaced with the MCLK.

(In the LXT300 only, if MCLK is not supplied the RCLK output will be replaced with the centered crystal clock.)

The LOS pin will reset as soon as a one (mark) is received.

In the LXT300 only, recovered clock signals are supplied to the jitter attenuator and the data latch. The recovered data is passed to the elastic store where it is buffered and synchronized with the dejittered recovered clock (RCLK).

Jitter Attenuation (LXT300 Only)

Jitter attenuation of the LXT300 clock and data outputs is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 6 for crystal

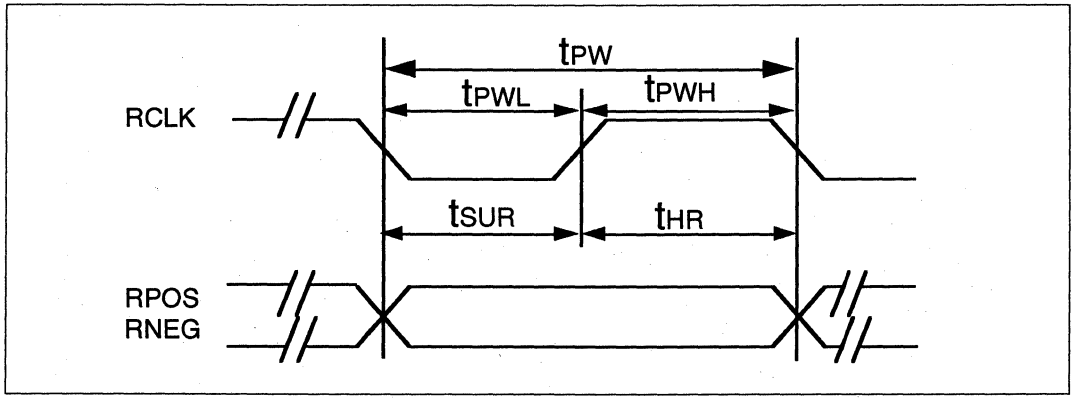
2

Table 5: LXT301 Receive Timing Characteristics (See Figure 6)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Receive clock duty cycle [2]	DSX-1	RCLKd	40	50	60	%	
	E1	RCLKd	40	50	60	%	
Receive clock pulse width [2]	DSX-1	t_{PW}	594	648	702	ns	
	E1	t_{PW}	447	488	529	ns	
Receive clock pulse width high	DSX-1	t_{PWH}	-	324	-	ns	
	E1	t_{PWH}	-	244	-	ns	
Receive clock pulse width low	DSX-1	t_{PWL}	270	324	378	ns	
	E1	t_{PWL}	203	244	285	ns	
RPOS / RNEG to RCLK rising setup time	DSX-1	t_{SUR}	50	270	-	ns	
	E1	t_{SUR}	50	203	-	ns	
RCLK rising to RPOS / RNEG hold time	DSX-1	t_{HR}	50	270	-	ns	
	E1	t_{HR}	50	203	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
[2] RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz, 0.2 UI clock displacement for 2.048 MHz.)

Figure 6: LXT301 Receive Clock Timing Diagram



specifications. The ES is a 32 x 2-bit register. Recovered data is clocked into the ES with the recovered clock signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the receive path.

Operating Modes

The LXT300 and 301 transceivers can be controlled through hard-wired pins (Hardware mode). Both transceivers can also be commanded to operate in one of several diagnostic modes.

LXT300 Only: The LXT300 can be controlled by a microprocessor through a serial interface (Host mode). The mode of operation is set by the MODE pin logic level.

Host Mode Operation (LXT300 Only)

To allow a host microprocessor to access and control the LXT300 through the serial interface, MODE is set to 1. The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte. Figure 7 shows the serial interface data structure and timing.

The Host mode provides a latched Interrupt output ($\overline{INT}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as follows:

CLKE	Output	Clock	Valid Edge
LOW	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
HIGH	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

The LXT300 serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The LXT300 contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select ($\overline{CS}$) input to transition from high to low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 7 lists serial data output bit combinations for each status. Serial data I/O timing characteristics are shown in Table 8, and Figures 8 and 9.

Hardware Mode Operation (LXT300 and 301)

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{INT}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS and RNEG outputs are valid on the rising edge of RCLK. The LXT301 operates in Hardware mode at all times.

LXT300 Only: To operate in Hardware mode, MODE must be set to 0. Equalizer Control signals (EC1 through EC3)

Table 6: LXT300 Crystal Specifications (External)

Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency Stability	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical

are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host mode.

Reset Operation (LXT300 and 301)

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. MCLK provides the receiver reference for the LXT301. The crystal oscillator provides the receiver reference in the LXT300. If the LXT300 crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and then begins calibration.

Table 7: LXT300 Serial Data Output Bits (See Figure 7)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	Local Loopback active
0	1	1	TAOS and Local Loopback active
1	0	0	Remote Loopback active
1	0	1	DPM has changed state since last Clear DPM occurred
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred

Figure 7: LXT300 Serial Interface Data Structure

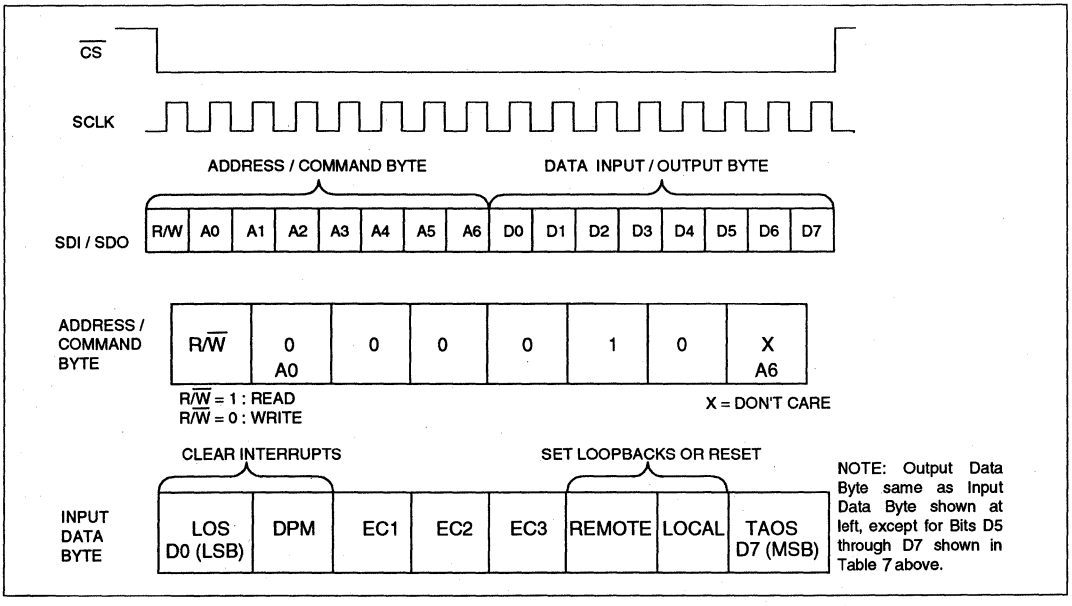


Table 8: LXT300 Serial I/O Timing Characteristics (See Figures 8 and 9)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	-	-	100	ns	Load 1.6 mA, 50pF
SDI to SCLK setup time	t_{DC}	50	-	-	ns	
SCLK to SDI hold time	t_{CDH}	50	-	-	ns	
SCLK low time	t_{CL}	240	-	-	ns	
SCLK high time	t_{CH}	240	-	-	ns	
SCLK rise and fall time	t_R , t_F	-	-	50	ns	
CS to SCLK setup time	t_{CC}	50	-	-	ns	
SCLK to CS hold time	t_{CCH}	50	-	-	ns	
CS inactive time	t_{CWH}	250	-	-	ns	
SCLK to SDO valid	t_{CDV}	-	-	200	ns	
SCLK falling edge or CS rising edge to SDO high Z	t_{CDZ}	-	100	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 8: LXT300 Serial Data Input Timing Diagram

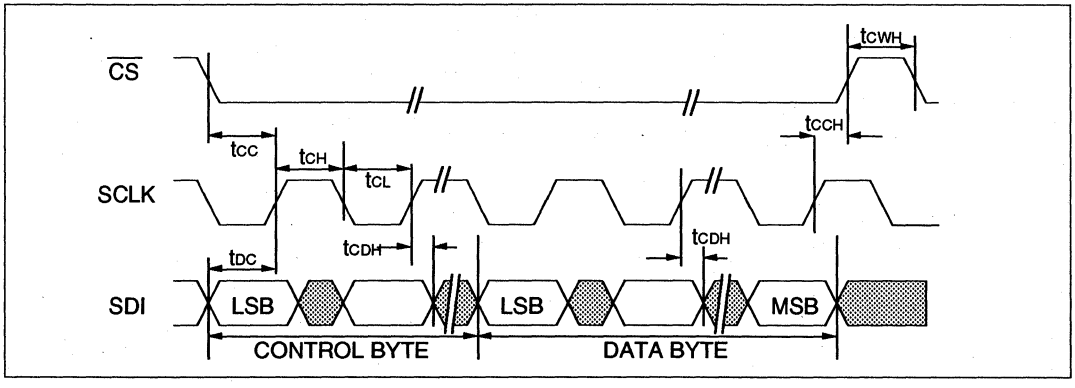
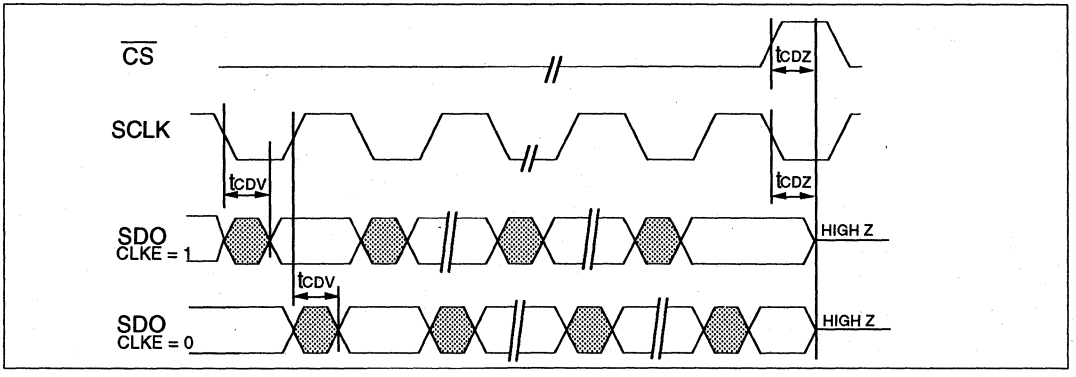


Figure 9: LXT300 Serial Data Output Timing Diagram



Diagnostic Mode Operation

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of 1's at the TCLK frequency when the TAOS mode is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK.) The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs (or a stream of 1's if the TAOS command is active) will be transmitted normally.

LXT300 Only: When used in this mode with a crystal, the transceiver can be used as a stand-alone jitter attenuator.

Power Requirements

The LXT300 and 301 are low-power CMOS devices. Each operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3V of each other, and decoupled to their respective grounds separately, as shown in Figure 10. Isolation between the transmit and receive circuits is provided internally.

Applications

LXT300 1.544 MHz T1 Interface Applications

Figure 10 is a typical 1.544 MHz T1 application. The LXT300 is shown in the Host mode with the LXP2180A T1/ESF Framer providing the digital interface with the host controller. Both devices are controlled through the serial interface. An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68µF and 0.1 µF on the receive side.)

LXT300 2.048 MHz E1 Interface Applications

Figure 11 is a typical 2.048 MHz E1 application. The LXT300 is shown in Hardware mode with the LXP2181A E1/CRC4 Framer. Resistors are installed in line with the transmit transformer for loading a 75 Ω coaxial cable. The in-line resistors are not required for transmission on 100 Ω shielded twisted-pair lines. As in the T1 application Figure 10, this configuration is illustrated with a crystal in place to enable the LXT300 Jitter Attenuation Loop, and a single power supply bus. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function.

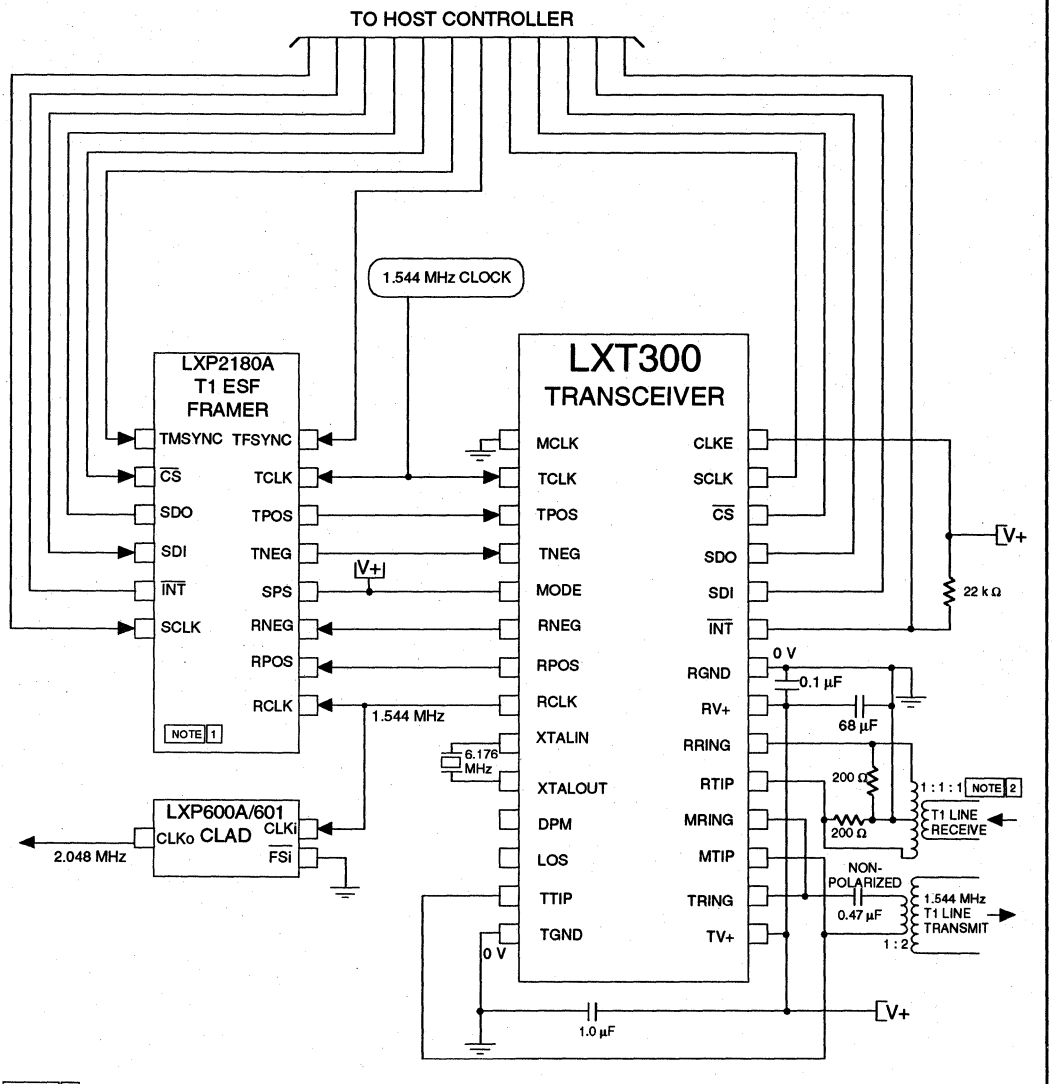
LXT301 1.544 MHz T1 Interface

Figure 12 is a typical 1.544 MHz T1 application of the LXT301. The LXT301 is shown with the LXP2180A T1/ESF Framer. An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68µF and 0.1 µF on the receive side.)

LXT301 2.048 MHz E1 Interface

Figure 13 is a typical 2.048 MHz E1 application of the LXT301. The LXT301 is shown with the LXP2181A E1/CRC4 Framer. Resistors are installed in line with the transmit transformer for loading a 75 Ω coaxial cable. The in-line resistors are not required for transmission on 100 Ω shielded twisted-pair lines. As in the T1 application Figure 12, this configuration is illustrated with a single power supply bus. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function.

Figure 10: Typical LXT300 1.544 MHz T1 Application (Host Mode)



NOTE 1 IN ADDITION TO THE LXP2180A, THE LXT300 IS COMPATIBLE WITH A WIDE VARIETY OF DIGITAL FRAMING AND SIGNALING DEVICES, INCLUDING THE LXP2181A, DS2180A, MT8976, AND R8070.

NOTE 2 WHEN LXT300 IS CONNECTED TO THE CROSS-CONNECT FRAME THROUGH A LOW LEVEL MONITOR JACK, RECEIVE TRANSFORMER SHOULD BE 1 : 2 : 2 TO BOOST THE INPUT SIGNAL.

Figure 11: Typical LXT300 2.048 MHz E1 Application (Hardware Mode)

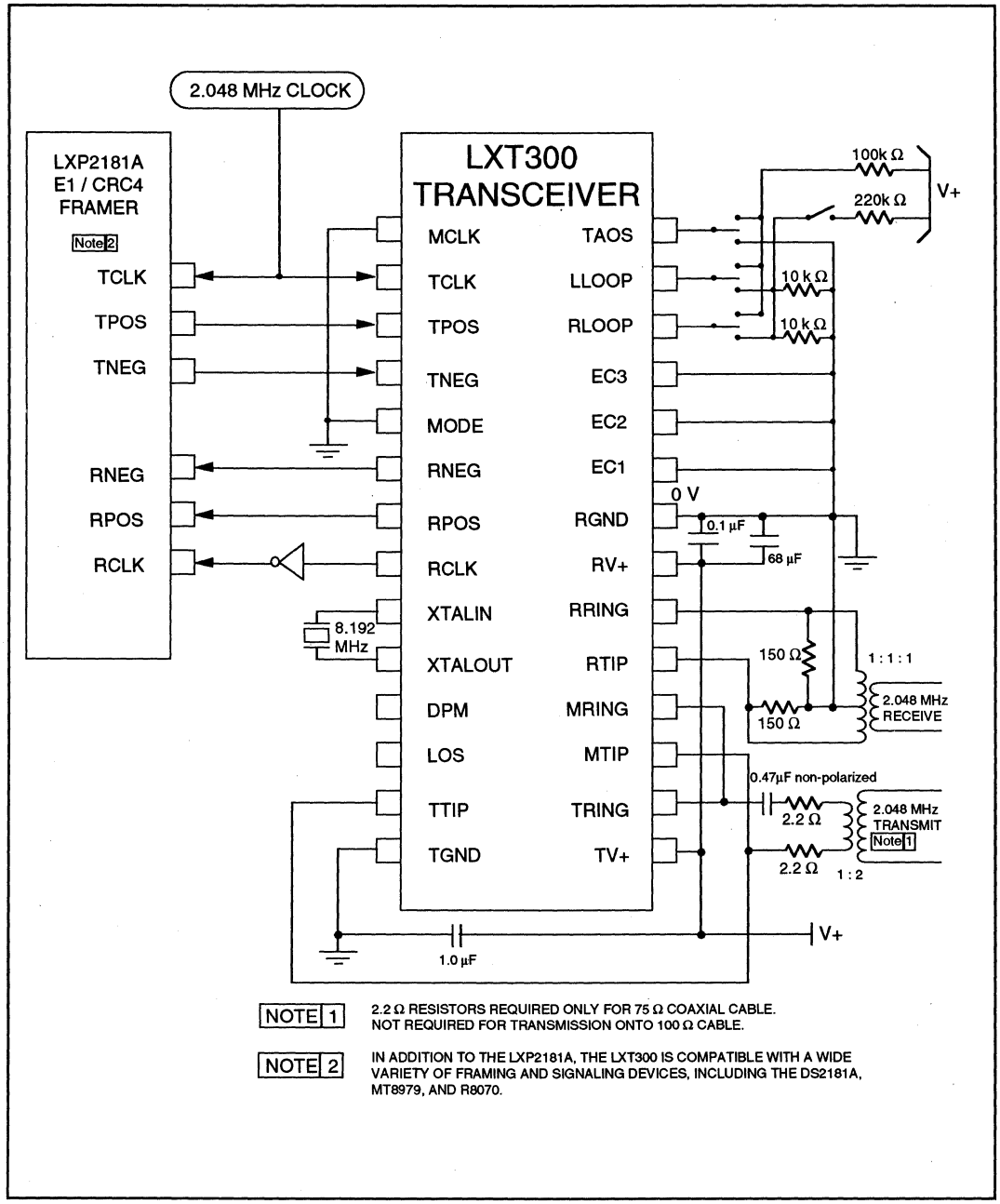


Figure 12: Typical LXT301 1.544 MHz T1 Application

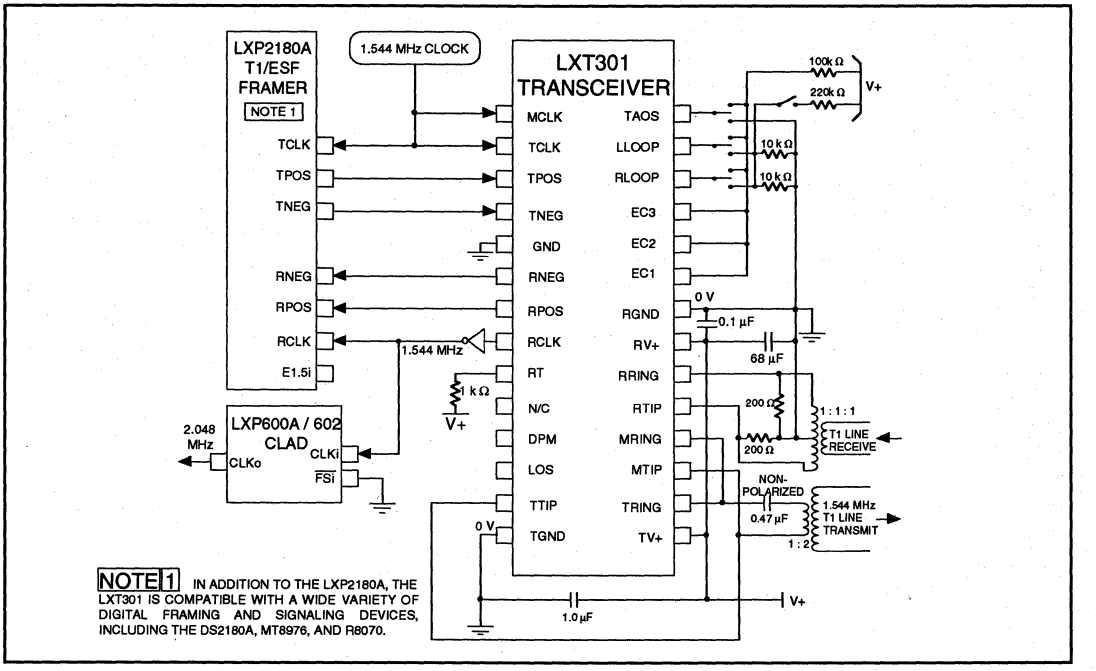
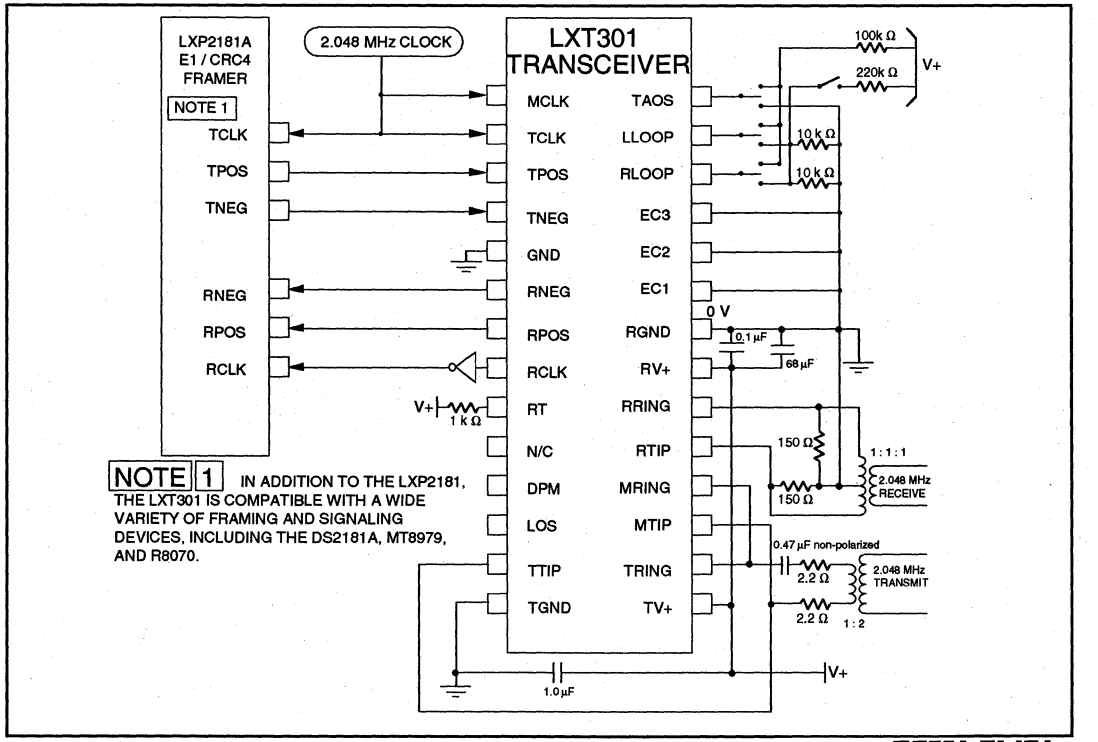


Figure 13: Typical LXT301 2.048 MHz E1 Application



Preliminary Information
February, 1994

LXT300Z/ LXT301Z

T1/E1 Integrated Short Haul Transceivers with Receive Jitter Attenuation

General Description

The LXT300Z and LXT301Z are fully integrated transceivers for both North American 1.544 MHz (T1), and European 2.048 MHz (E1) applications. They are pin and functionally compatible with standard LXT300/301 devices, with some circuit enhancements.

The LXT300Z provides receive jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface. The LXT301Z is pin compatible, but does not provide jitter attenuation or a serial interface. Transmit drivers provide low output impedance, constant during transmission of both marks and spaces, resulting in an improved performance over various cable networking configurations. Both transceivers offer a variety of diagnostic features including transmit and receive monitoring. Clock inputs may be derived from an on-chip crystal oscillator or digital inputs. They use an advanced double-poly, double-metal CMOS process and each requires only a single 5-volt power supply.

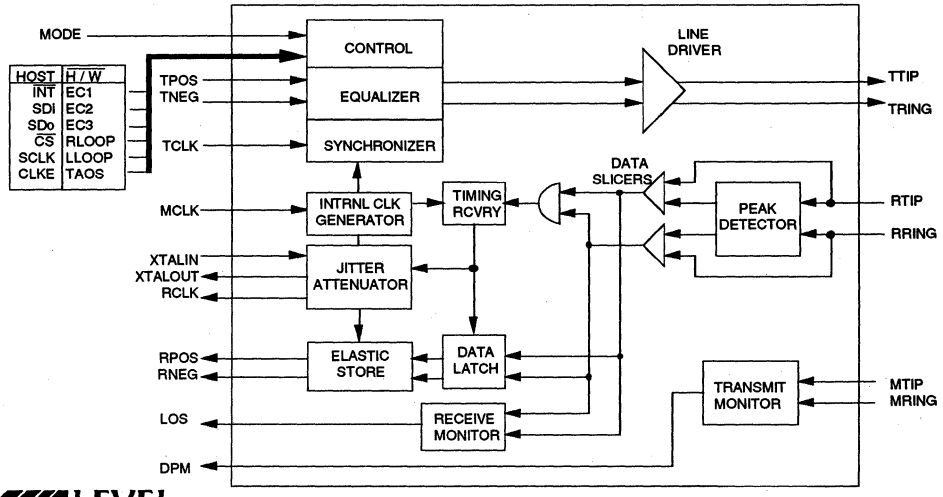
Applications

- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

Features

- Compatible with most popular PCM framers including the LXP2180A and LXP2181A
- Line driver, data recovery and clock recovery functions
- Receive jitter attenuation starting at 3 Hz meets or exceeds AT&T Pub 62411 (LXT300Z only)
- Constant low impedance drivers during marks and spaces (3 Ω typical)
- Transmit amplitude variation with supply is less than 1% (typical)
- Minimum receive signal of 500 mV
- Selectable slicer levels (E1/DSX-1) improve SNR
- Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- Local and remote loopback functions
- Transmit Driver Performance Monitor (DPM) output
- Receive monitor with Loss of Signal (LOS) output (12.5% one's density reset)
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Microprocessor controllable (LXT300Z only)
- Available in 28 pin DIP or PLCC

Figure 1: LXT300Z Block Diagram



LXT304A

Low-Power T1/E1 Integrated Short Haul Transceiver with Receive Jitter Attenuation

General Description

The LXT304A is a fully integrated low-power transceiver for both North American 1.544 MHz (T1), and European 2.048 MHz (E1) applications. It features a constant low output impedance transmitter allowing for high transmitter return loss in T1/E1 applications. Transmit pulse shapes (DSX-1 or E1) are selectable for various line lengths and cable types.

The LXT304A provides receive jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface.

It offers a variety of diagnostic features including transmit and receive monitoring. The device incorporates an on-chip crystal oscillator, and also accepts digital clock inputs. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

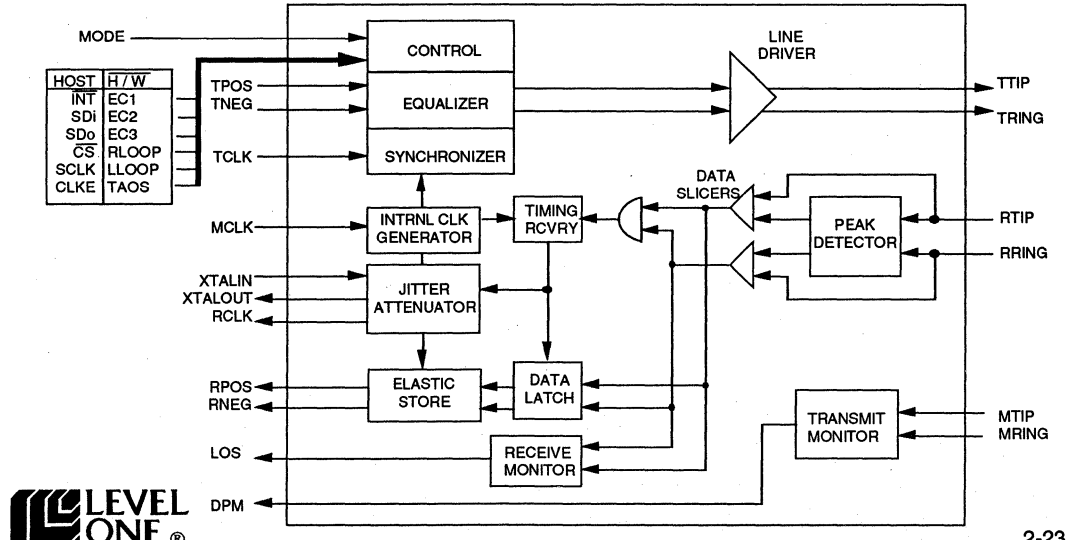
Applications

- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

Features

- Low power consumption (400 mW maximum) 40% less than the LXT300
- Constant low output impedance transmitter regardless of data pattern
- High transmit and receive return loss
- Meets or exceeds all industry specifications including CCITT G.703, ANSI T1.403 and AT&T Pub 62411
- Compatible with most popular PCM framers including the LXP2180A (T1) and LXP2181A (E1)
- Line driver, data recovery and clock recovery functions
- Minimum receive signal of 500 mV
- Selectable slicer levels (E1/DSX-1) improve SNR
- Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- Local and remote loopback functions
- Transmit / Receive performance monitors with DPM and LOS outputs
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Receive jitter attenuation starting at 3 Hz
- Microprocessor controllable
- Available in 28 pin DIP or PLCC

Figure 1: LXT304A Block Diagram



Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	–	6.0	V
Input voltage, any pin [1]	V_{IN}	RGND - 0.3	RV+ + 0.3	V
Input current, any pin [2]	I_{IN}	-10	10	mA
Ambient operating temperature	T_A	-40	85	°C
Storage temperature	T_{STG}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation not guaranteed at these extremes.
[1] Excluding RTIP and RRING which must stay within -6V to RV + 0.3V.
[2] Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100mA.

Electrical Characteristics (T_A = -40° to 85°C, V+ = 5.0 V ±5%, GND = 0 V)

Parameter	Sym	Min	Max	Units	Test Conditions
Total power dissipation [3]	P_D	–	400	mW	100% ones density & max line length @ 5.25 V
High level input voltage [4,5] (pins 1-5, 10, 23-28)	V_{IH}	2.0	–	V	
Low level input voltage [4,5] (pins 1-5, 10, 23-28)	V_{IL}	–	0.8	V	
High level output voltage [4,5] (pins 6-8, 11, 12, 23, 25)	V_{OH}	2.4	–	V	I_{OUT}=- 400 µA
Low level output voltage [4,5] (pins 6-8, 11, 12, 23, 25)	V_{OL}	–	0.4	V	I_{OUT}=1.6mA
Input leakage current [6]	I_{LL}	0	±10	µA	
Three-state leakage current [4] (pin 25)	I_{3L}	0	±10	µA	

[3] Power dissipation while driving 75 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
[4] Functionality of pins 23 and 25 depends on mode. See Host / Hardware Mode descriptions.
[5] Output drivers will output CMOS logic levels into CMOS loads.
[6] Except MTIP and MRING I_{LL} = ± 50 µA.

Analog Specifications (T_A = -40° to 85°C, V+ = 5.0 V ±5%, GND = 0 V)

Parameter		Min	Typ	Max	Units	Test Conditions
AMI Output Pulse Amplitudes	DSX-1	2.4	3.0	3.6	V	measured at the DSX
	CEPT	2.7	3.0	3.3	V	measured at line side
Recommended output load at TTIP and TRING		–	75	–	Ω	
Jitter added by the transmitter [7]	10Hz - 8kHz	–	–	0.01	UI	
	8kHz - 40 kHz	–	–	0.025	UI	
	10Hz - 40 kHz	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Sensitivity below DSX	(0dB = 2.4V)	13.6	–	–	dB	
		500	–	–	mV	
Loss of Signal threshold		–	0.3	–	V	
Data decision threshold	DSX-1	63	70	77	%peak	
	CEPT	43	50	57	% peak	
Allowable consecutive zeros before LOS		160	175	190	–	
Input jitter tolerance	10kHz - 100kHz	0.4	–	–	UI	
Jitter attenuation curve corner frequency [8]		–	3	–	Hz	

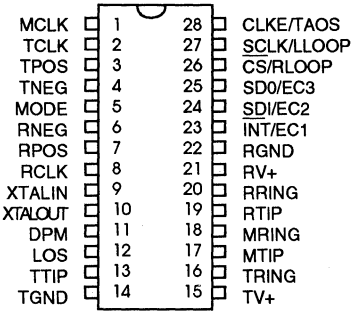
Minimum Return Loss [9,10]	Transmit Min	Transmit Typ	Receive Min	Receive Typ		
51 kHz - 102 kHz	20	28	20	30	dB	
102 kHz - 2.048 MHz	20	28	20	30	dB	
2.048 MHz - 3.072 MHz	20	24	20	25	dB	

[7] Input signal to TCLK is jitter-free.
[8] Circuit attenuates jitter at 20 dB/decade above the corner frequency.
[9] In accordance with CCITT G.703/RC6367A return loss specifications when wired per Figure 10 (DSX-1) or Figure 11 (CEPT).
[10] Guaranteed by design.

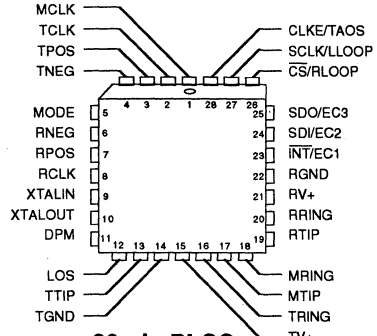
Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
DC supply [1]	RV+, TV+	4.75	5.0	5.25	V
Ambient operating temperature	T_A	-40	25	85	°C

[1] TV+ must not exceed RV+ by more than 0.3 V.



28-pin DIP



28-pin PLCC

Table 1: Pin Descriptions

Pin #	Sym	I/O	Name	Description
1	MCLK	I	Master Clock	A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
2	TCLK	I	Transmit Clock	Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is not supplied, the transmitter remains powered down.
3	TPOS	I	Transmit Positive Data	Input for positive pulse to be transmitted on the twisted-pair line.
4	TNEG	I	Transmit Negative Data	Input for negative pulse to be transmitted on the twisted-pair line.
5	MODE	I	Mode Select	Setting MODE to logic 1 puts the LXT304A in the Host mode. In the Host mode, the serial interface is used to control the LXT304A and determine its status. Setting MODE to logic 0 puts the LXT304A in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status.
6	RNEG	O	Receive Negative Data	Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). Both outputs are stable and valid on the rising edge of RCLK. In the Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware mode both outputs are stable and valid on the rising edge of RCLK.
7	RPOS	O	Receive Positive Data	
8	RCLK	O	Recovered Clock	This is the clock recovered from the signal received at RTIP and RRING.

Table 1: Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
9	XTALIN	I	Crystal Input	An external crystal operating at four times the bit rate (6.176 MHz for DSX-1, 8.192 MHz for E1 applications with an 18.7pF load) is required to enable the jitter attenuation function of the LXT304A. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
10	XTALOUT	O	Crystal Output	
11	DPM	O	Driver Performance Monitor	DPM goes to a logic 1 when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains at logic 1 until a signal is detected.
12	LOS	O	Loss Of Signal	LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when the received signal reaches 12.5% ones density, based on 4 ones in any 32 bit periods with no more than 15 consecutive zeros.
13	TTIP	O	Transmit Tip	Differential Driver Outputs. These low impedance outputs achieve maximum power savings through a 1:1.15 transformer (T1), or a 1:1 (75 Ω) or 1:1.26 (120- Ω) transformer (E1) without additional components. To provide higher return loss, resistors may be used in series with a transformer as specified in Tables 8, 9 and 10.
16	TRING	O	Transmit Ring	
14	TGND	-	Transmit Ground	Ground return for the transmit drivers power supply TV+.
15	TV+	I	Transmit Power Supply	+5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3V.
17	MTIP	I	Monitor Tip	These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another LXT304A on the board. To prevent false interrupts in the host mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-level voltage. The monitor clock can range from 100kHz to the TCLK frequency.
18	MRING	I	Monitor Ring	
19	RTIP	I	Receive Tip	The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
20	RRING	I	Receive Ring	
21	RV+	I	Receive Power Supply	+5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	-	Receive Ground	Ground return for power supply RV+.

Table 1: Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
23	$\overline{INT}$	O	Interrupt *(Host Mode)*	This LXT304A Host mode output goes low to flag the host processor when LOS or DPM go active. $\overline{INT}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{INT}$ is reset by clearing the respective register bit (LOS and/or DPM.)
	EC1	I	Equalizer Control 1 *(H/W Mode)*	The signal applied at this pin in the LXT304A Hardware mode is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
24	SDI	I	Serial Data In *(Host Mode)*	The serial data input stream is applied to this pin when the LXT304A operates in the Host mode. SDI is sampled on the rising edge of SCLK.
	EC2	I	Equalizer Control 2 *(H/W Mode)*	The signal applied at this pin in the LXT304A Hardware mode is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
25	SDO	O	Serial Data Out *(Host Mode)*	The serial data from the on-chip register is output on this pin in the LXT304A Host mode. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is high.
	EC3	I	Equalizer Control 3 *(H/W Mode)*	The signal applied at this pin in the LXT304A Hardware mode is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
26	$\overline{CS}$	I	Chip Select *(Host Mode)*	This input is used to access the serial interface in the LXT304A Host mode. For each read or write operation, $\overline{CS}$ must transition from high to low, and remain low.
	RLOOP	I	Remote Loopback *(H/W Mode)*	This input controls loopback functions in the LXT304A Hardware mode. Setting RLOOP to a logic 1 enables the Remote Loopback mode. Setting both RLOOP and LLOOP causes a Reset .
27	SCLK	I	Serial Clock *(Host Mode)*	This clock is used in the LXT304A Host mode to write data to or read data from the serial interface registers.
	LLOOP	I	Local Loopback *(H/W Mode)*	This input controls loopback functions in the LXT304A Hardware mode. Setting LLOOP to a logic 1 enables the Local Loopback Mode.
28	CLKE	I	Clock Edge *(Host Mode)*	Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	I	Transmit All Ones *(H/W Mode)*	When set to a logic 1, TAOS causes the LXT304A (Hardware mode) to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

Functional Description

The LXT304A is a fully integrated PCM transceiver for both 1.544 MHz (DSX-1) and 2.048 MHz (E1) applications. It allows full-duplex transmission of digital data over existing twisted-pair installations.

Figure 1 is a simplified block diagram of the LXT304A. The LXT304A transceiver interfaces with two twisted-pair lines, one twisted-pair for transmit, one twisted-pair for receive.

Receiver

The LXT304A receives the signal input from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Table 2 and Figure 2 for LXT304A receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (determined by Equalizer Control inputs EC1 - EC3 ≠ 000) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (EC inputs = 000 or 001) the threshold is 50 %.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB of attenuation). Regardless of received signal level, the peak detectors are held above a minimum level of .3 V to provide immunity from impulsive noise.

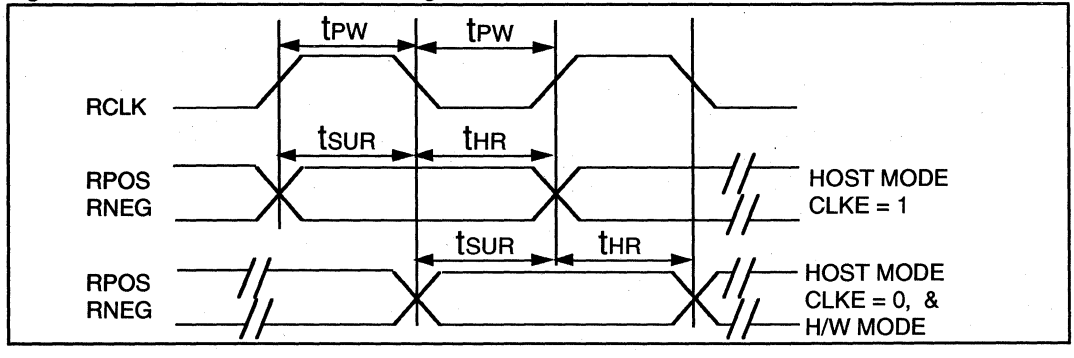
After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The data and clock recovery circuits are highly tolerant with an input jitter tolerance significantly better than required by Pub 62411, as shown in Figure 3.

Table 2: LXT304A Receive Characteristics (See Figure 2)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Receive slicer threshold	DSX-1	RST	65	70	75	%	
	CEPT	RST	45	50	55	%	
Receive clock duty cycle		RCLKd	40	-	60	%	
Receive clock pulse width	DSX-1	t_{PW}	-	324	-	ns	
	CEPT	t_{PW}	-	244	-	ns	
RPOS / RNEG to RCLK	DSX-1	t_{SUR}	-	274	-	ns	
rising setup time	CEPT	t_{SUR}	-	194	-	ns	
RCLK rising to RPOS /	DSX-1	t_{HR}	-	274	-	ns	
RNEG hold time	CEPT	t_{HR}	-	194	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 2: LXT304A Receive Clock Timing



The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and a smooth transition replaces the RCLK output with the MCLK. (If MCLK is not supplied the RCLK output will be replaced with the centered crystal clock.) The LOS pin is reset when the received signal reaches 12.5% ones density (4 marks in 32 bits) with no more than 15 consecutive zeros.

Recovered clock signals are supplied to the jitter attenuator and the data latch. The recovered data is passed to the elastic store where it is buffered and synchronized with the dejittered recovered clock (RCLK).

Jitter Attenuation

Jitter attenuation of the LXT304A clock and data outputs is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 3 for crystal specifications. The ES is a 32 x 2-bit register. Recovered data is clocked into the ES with the recovered clock signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the receive path.

Figure 3: Typical Receiver Input Jitter Tolerance (Loop Mode)

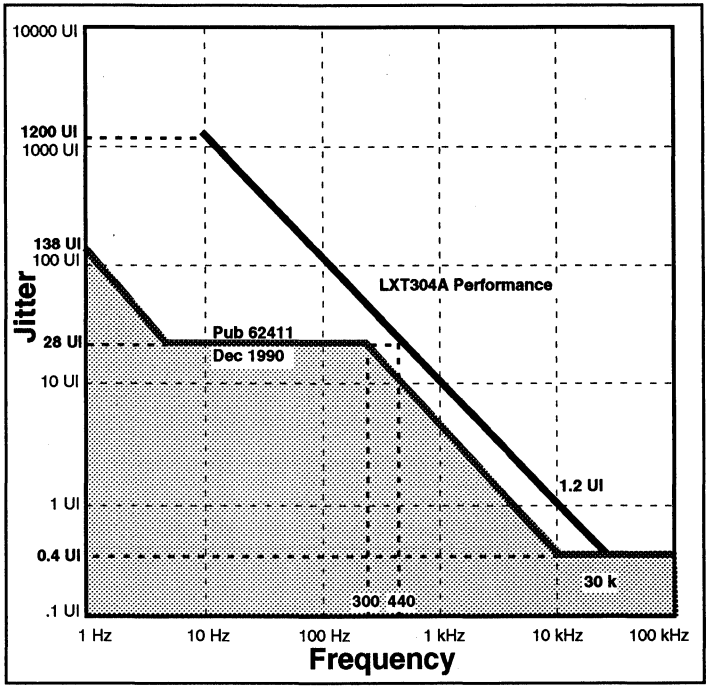


Table 3: LXT304A Crystal Specifications (External)

Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency Stability	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical

Transmitter

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). If TCLK is not supplied the transmitter remains powered down, except during remote loopback. Refer to Table 4 and Figure 4 for master and transmit clock timing characteristics.

The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 5. Equalizer Control signals may be hardwired in the Hardware mode, or input as part of the serial data stream (SDI) in the Host mode. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The line driver provides a constant low output impedance of 3 Ω (typical). This well controlled output impedance provides excellent return loss (> 20 dB) when used with external 9.4 Ω precision resistors (± 1% accuracy) in series with a transmit transformer with a turns ratio of 1:2.3 (± 2% accuracy). Series resistors also provide increased surge protection and reduce short circuit current flow.

Pulses can be shaped for either 1.544 or 2.048 MHz applications. 1.544 MHz pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The LXT304A also matches FCC and ECSA specifications for CSU applications. A 1:1.15 transmit transformer is used for 1.544 MHz systems. For higher return loss in DSX-1 applications, use 9.4 Ω resistors in series with a 1:2.3 transmit transformer.

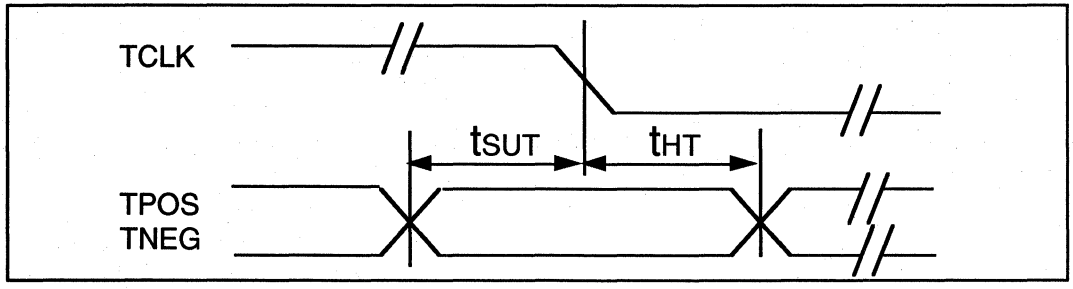
2.048 MHz pulses can drive coaxial or shielded twisted-pair lines. For E1 systems, a 1:2 transmit transformer and series resistors are recommended. This design meets or exceeds all CCITT and European PTT specifications for transmit and receive return loss. A 1:1 or 1:1.26 transformer may be used without series resistors.

Table 4: LXT304A Master Clock and Transmit Timing Characteristics (See Figure 4)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	DSX-1	MCLK	-	1.544	-	MHz
	E1	MCLK	-	2.048	-	MHz
Master clock tolerance		MCLKt	-	±100	-	ppm
Master clock duty cycle		MCLKd	40	-	60	%
Crystal frequency	DSX-1	fc	-	6.176	-	MHz
	E1	fc	-	8.192	-	MHz
Transmit clock frequency	DSX-1	TCLK	-	1.544	-	MHz
	E1	TCLK	-	2.048	-	MHz
Transmit clock tolerance		TCLKt	-	-	±50	ppm
Transmit clock duty cycle		TCLKd	10	-	90	%
TPOS/TNEG to TCLK setup time		t_{SUT}	25	-	-	ns
TCLK to TPOS/TNEG Hold time		t_{HT}	25	-	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 4: LXT304A Transmit Clock Timing



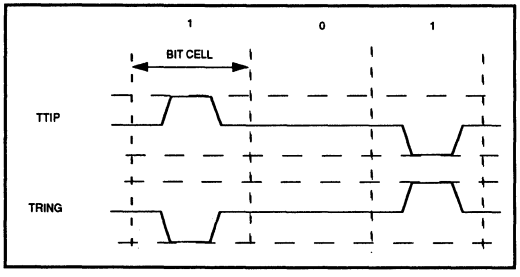
Driver Performance Monitor

The transceiver incorporates a Driver Performance Monitor (DPM) in parallel with TTIP and TRING at the output transformer. The DPM output goes high upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

Line Code

The LXT304A transmits data as a 50% AMI line code as shown in Figure 5. The output driver maintains a constant low output impedance regardless of whether it is driving marks or spaces.

Figure 5: 50% AMI Coding



Operating Modes

The LXT304A transceiver can be controlled through hard-wired pins (Hardware mode) or by a microprocessor through a serial interface (Host mode). The mode of operation is set by the MODE pin logic level. The LXT304A can also be commanded to operate in one of several diagnostic modes.

Host Mode Operation

To allow a host microprocessor to access and control the LXT304A through the serial interface, MODE is set to 1.

The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte. Figure 6 shows the serial interface data structure and timing.

The Host mode provides a latched Interrupt output (INT) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as follows:

CLKE	Output	Clock	Valid Edge
LOW	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
HIGH	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

The LXT304A serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The LXT304A contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select (CS) input to transition from high to low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 6 lists serial data output bit combinations for each status. Serial data I/O timing characteristics are shown in Table 7, and Figures 7 and 7.

Table 5: Equalizer Control Inputs

EC3	EC2	EC1	Line Length[1]	Cable Loss[2]	Application	Frequency
0	1	1	0 - 133 ft ABAM	0.6 dB	DSX-1	1.544 MHz
1	0	0	133 - 266 ft ABAM	1.2 dB		
1	0	1	266 - 399 ft ABAM	1.8 dB		
1	1	0	399 - 533 ft ABAM	2.4 dB		
1	1	1	533 - 655 ft ABAM	3.0 dB		
0	0	0	CCITT Recommendation G.703		E1 - Coax (75 Ω)	2.048 MHz
0	0	1			E1 - Twisted-pair (120 Ω)	
0	1	0	FCC Part 68, Option A		CSU (DS-1)	1.544 MHz

[1] Line length from transceiver to DSX-1 cross-connect point.
[2] Maximum cable loss at 772 kHz.

Hardware Mode Operation

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the INT and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS and RNEG outputs are valid on the rising edge of RCLK. To operate in Hardware mode, MODE must be set to 0. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host mode.

Reset Operation

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. The crystal oscillator provides the receiver reference. If the LXT304A crystal oscillator is grounded, MCLK is used as the receiver reference clock.

Table 6: LXT304A Serial Data Output Bits (See Figure 6)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	Local Loopback active
0	1	1	TAOS and Local Loopback active
1	0	0	Remote Loopback active
1	0	1	DPM has changed state since last Clear DPM occurred
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred

Figure 6: LXT304A Serial Interface Data Structure

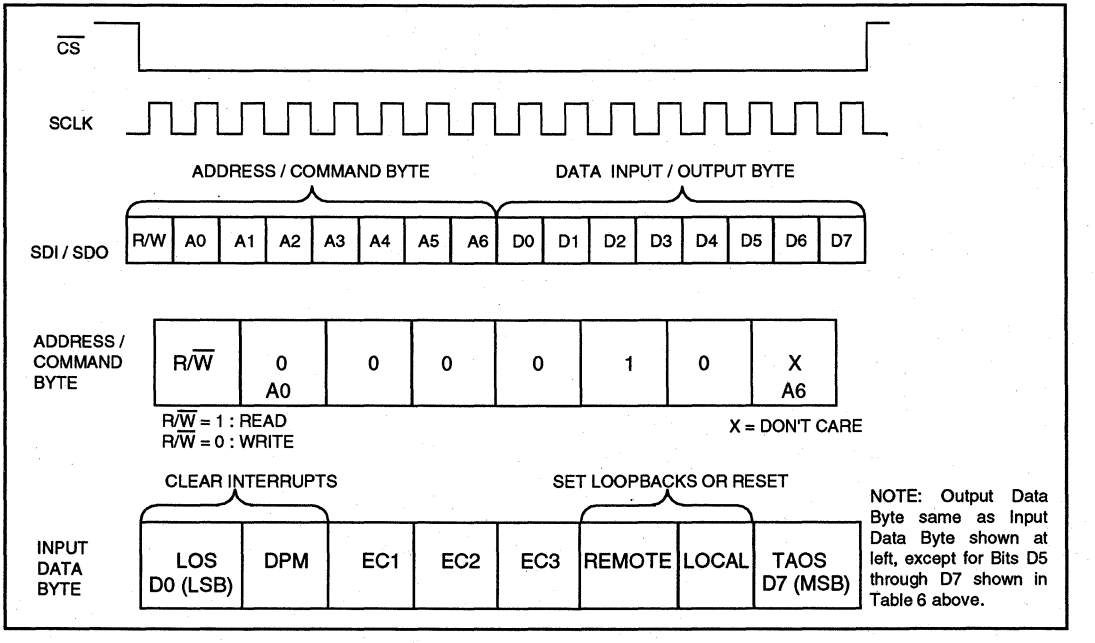


Table 7: LXT304A Serial I/O Timing Characteristics (See Figures 7 and 8)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	-	-	100	ns	Load 1.6 mA, 50pF
SDI to SCLK setup time	t_{DC}	50	-	-	ns	
SCLK to SDI hold time	t_{CDH}	50	-	-	ns	
SCLK low time	t_{CL}	240	-	-	ns	
SCLK high time	t_{CH}	240	-	-	ns	
SCLK rise and fall time	t_R , t_F	-	-	50	ns	
$\overline{CS}$ to SCLK setup time	t_{CC}	50	-	-	ns	
SCLK to $\overline{CS}$ hold time	t_{CCH}	50	-	-	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	-	-	ns	
SCLK to SDO valid	t_{CDV}	-	-	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	-	100	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 7: LXT304A Serial Data Input Timing Diagram

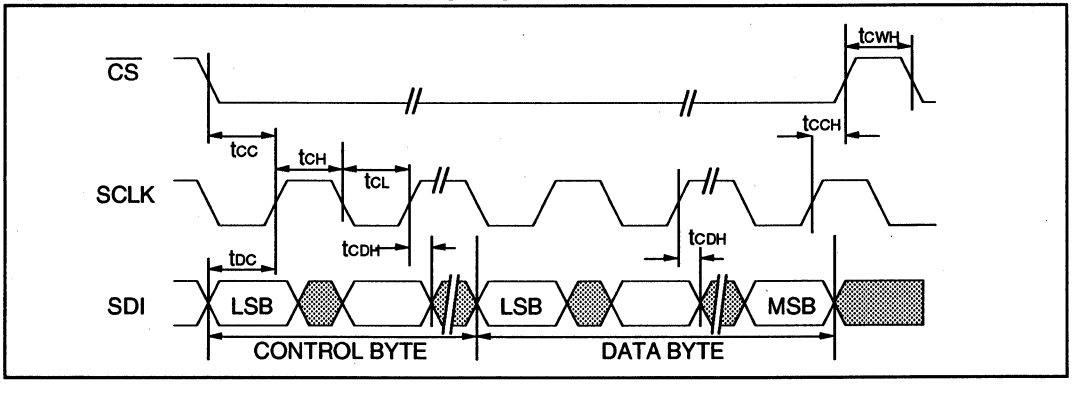
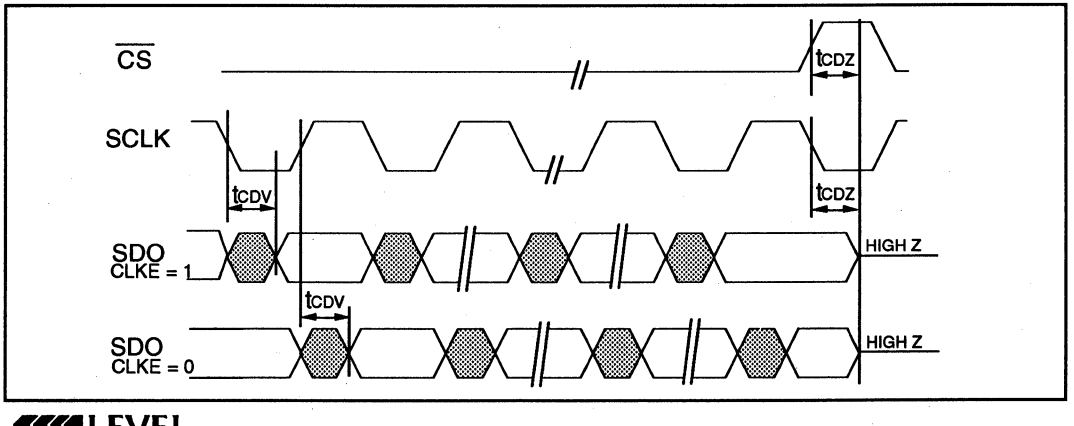


Figure 8: LXT304A Serial Data Output Timing Diagram



The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and then calibration begins.

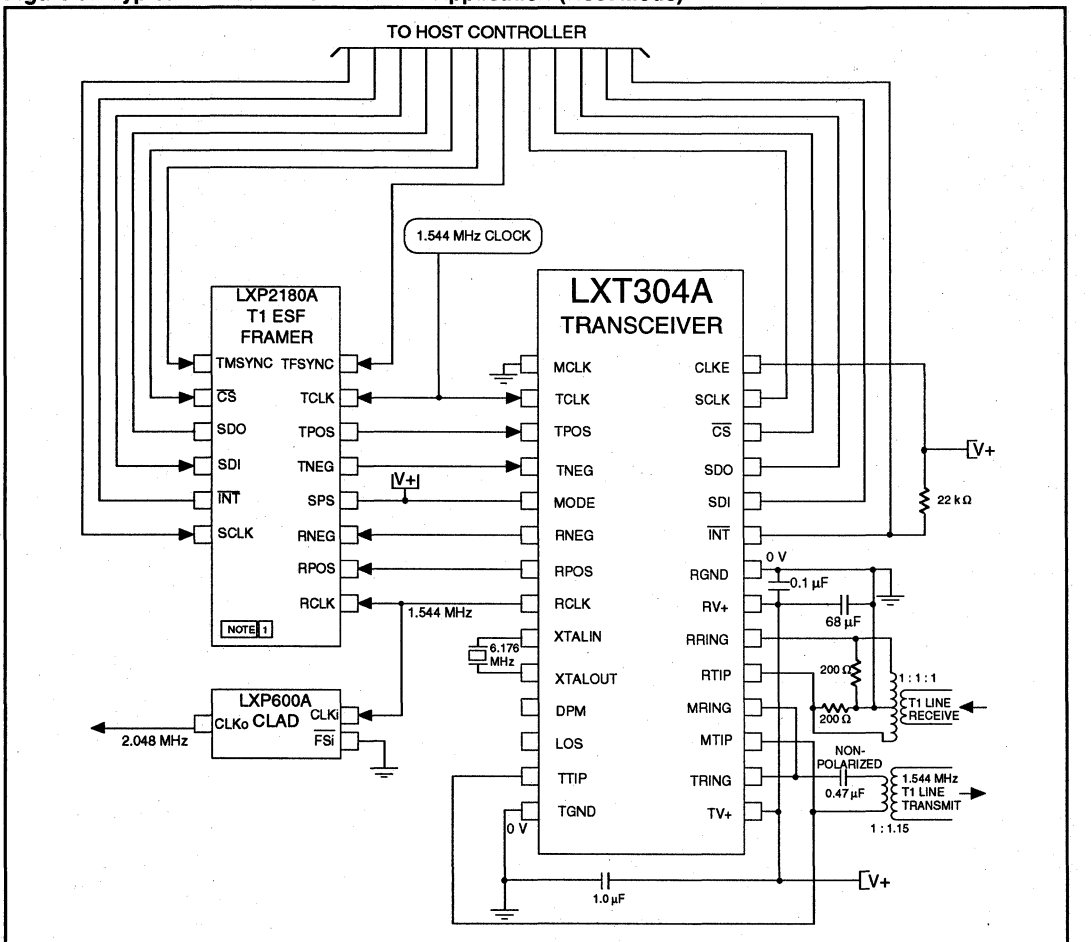
Diagnostic Mode Operation

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of 1's at the TCLK frequency when TAOS is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK.) The transmitter circuits are unaffected. The TPOS and TNEG inputs (or a stream of 1's if the TAOS command is active) will be transmitted normally. When used in this mode with a crystal, the transceiver can be used as a stand-alone jitter attenuator.

Figure 9: Typical LXT304A 1.544 MHz T1 Application (Host Mode)



NOTE 1 IN ADDITION TO THE LXP2180A, THE LXT304A IS COMPATIBLE WITH A WIDE VARIETY OF DIGITAL FRAMING AND SIGNALING DEVICES, INCLUDING THE LXP2181A, DS2180A, MT8976, AND R8070.

Power Requirements

The LXT304A is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3V of each other, and decoupled to their respective grounds separately, as shown in Figure 9. Isolation between transmit and receive circuits is provided internally. During normal operation, TAOS or LLOOP, the transmitter powers down if TCLK is not supplied.

Applications

1.544 MHz T1 Interface Applications

Figure 9 is a typical 1.544 MHz T1 application using a 1:1.15 transmit transformer without in-line resistors to provide maximum power savings. The LXT304A is shown in the Host mode with the LXP2180A T1/ESF Framer providing the digital interface with the host controller. Both devices are controlled through the serial interface. An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68µF and 0.1 µF on the receive side.)

1.544 MHz DSX-1 Applications

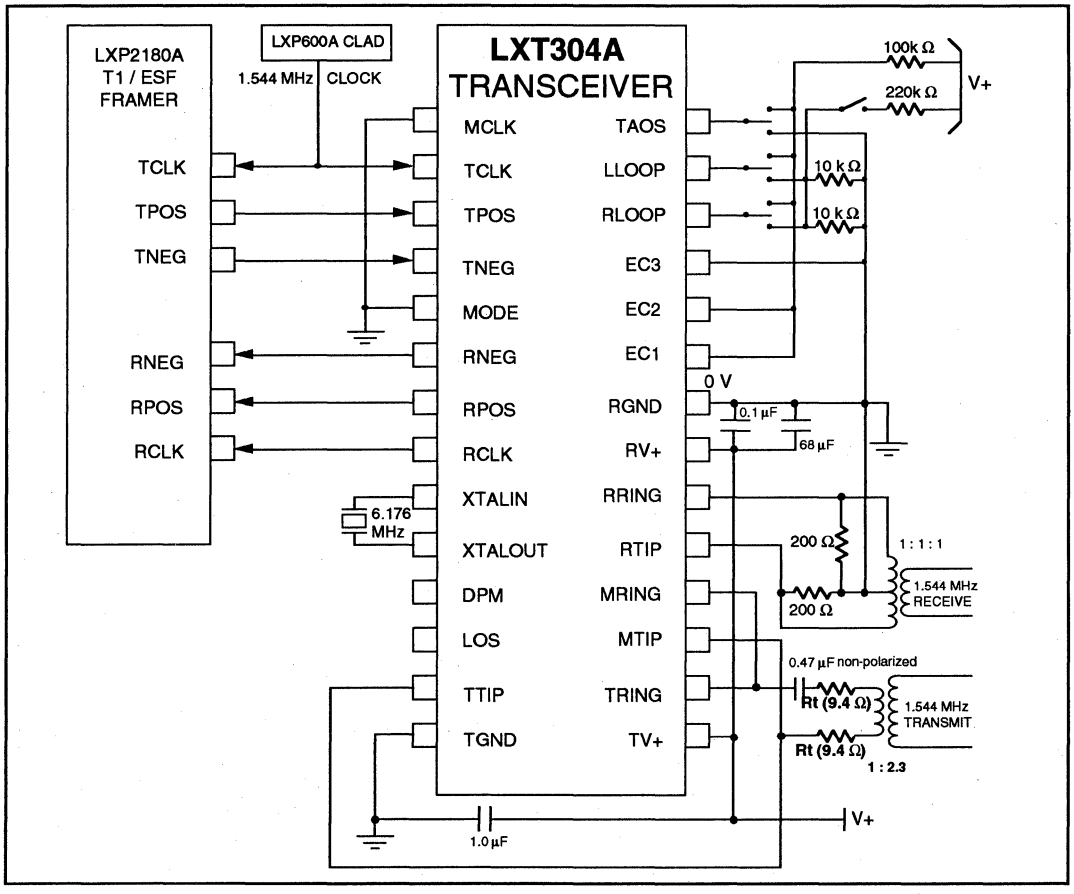
Figure 10 is a 1.544 MHz DSX-1 application using EC code 011. For DSX-1 applications, series resistors can be used to provide higher return loss. Table 8 lists transformer ratios, Rt values and typical return losses for 1.544 MHz EC codes.

Table 8: T1/DSX-1 Output Combinations (100 Ω)

EC	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
011 - 111	1 : 1.15	Rt = 0 Ω	0.5 dB
011 - 111	1 : 2	Rt = 9.4 Ω	20 dB
011 - 111	1 : 2.3	Rt = 9.4 Ω	28 dB

[1] Transformer turns ratio accuracy is ± 2 %.
[2] Rt values are ± 1 %.
[3] Typical return loss, 102 kHz - 2.048 MHz band.

Figure 10: Typical LXT304A DSX-1 Application (Hardware Mode)



2.048 MHz E1 Interface Applications

Figure 11 is a 2.048 MHz E1 TWP application using EC code 001 and 15 Ω Rt resistors in line with the transmit transformer to provide high return loss and surge protection. When high return loss is not a critical factor, a 1:1 or 1:1.26 transformer without in-line resistors provides maximum power savings. Tables 9 and 10 list typical return loss figures for various transformer ratios, Rt values and associated 2.048 MHz EC codes for 75 Ω coax and 120 Ω TWP, respectively. The LXT304A is shown in Hardware mode with the LXP2181A E1/CRC4 Framer. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function. As in the DSX-1 application Figure 10, this configuration is illustrated with a crystal in place to enable the LXT304A Jitter Attenuation Loop, and a single power supply bus.

Table 9: E1 Output Combinations (75 Ω)

EC	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
0 0 1	1 : 1	Rt = 10 Ω	5 dB
0 0 1	1 : 2	Rt = 14.3 Ω	12 dB
0 0 0	1 : 1	Rt = 0 Ω	0.5 dB
0 0 0	1 : 2	Rt = 9.4 Ω	24 dB

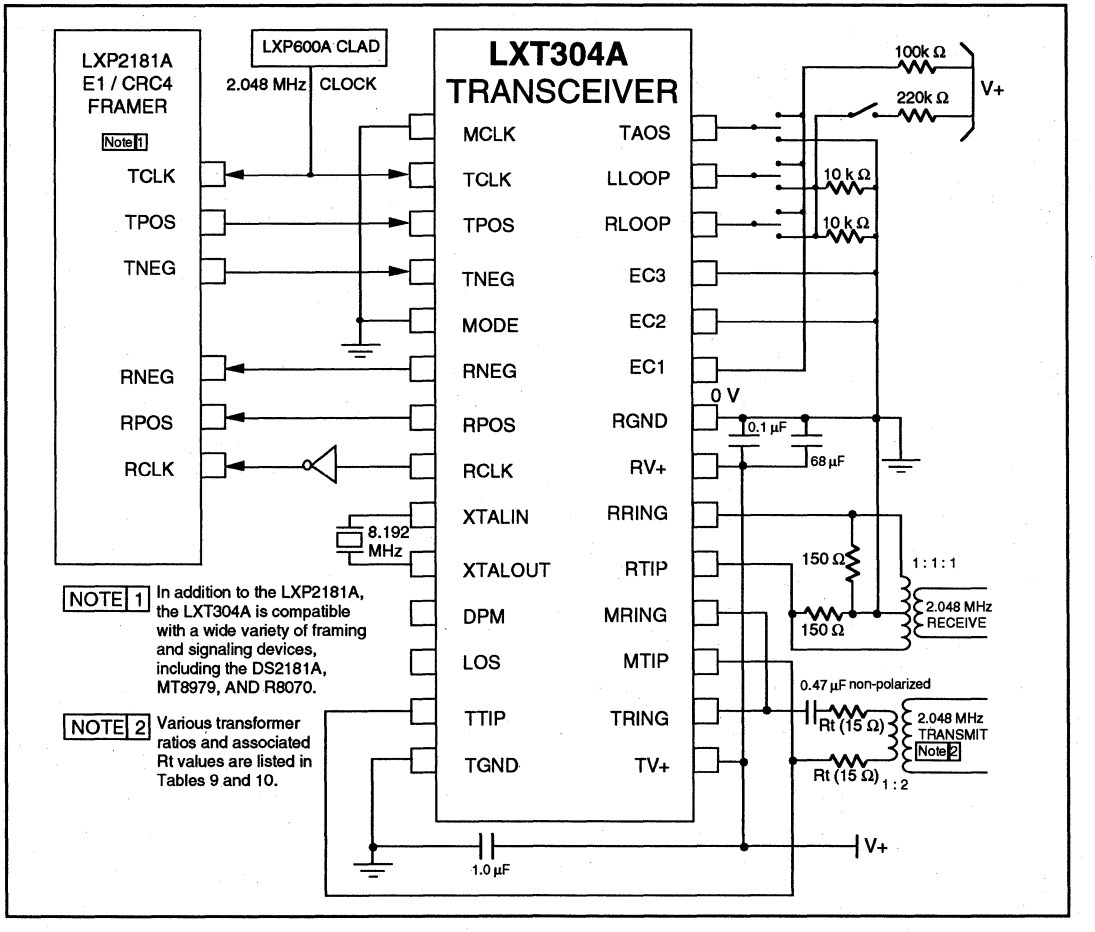
[1] Transformer turns ratio accuracy is ± 2 %.
[2] Rt values are ± 1 %.
[3] Typical return loss, 102 kHz - 2.048 MHz band.

Table 10: E1 Output Combinations (120 Ω)

EC	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
0 0 1	1 : 1	Rt = 0 Ω	0.5 dB
0 0 1	1 : 2	Rt = 15 Ω	30 dB
0 0 0	1 : 1.26	Rt = 0 Ω	0.5 dB
0 0 0	1 : 2	Rt = 8.7 Ω	12 dB

[3] Transformer turns ratio accuracy is ± 2 %.
[2] Rt values are ± 1 %.
[3] Typical return loss, 102 kHz - 2.048 MHz band.

Figure 11: LXT304A 2.048 MHz E1 Application (Hardware Mode)



D4 Channel Bank Applications

Existing D4 Channel Bank architectures frequently employ: (1) a plug-in card for T1 pulse generation (6.0 V peak); and (2) a separate card for pulse shaping and Line Build-Out (LBO). The LXT304A integrates the functions of both cards on a single chip producing a DSX-1 compatible, 3.0 V peak output pulse with a standard transformer. In new designs, the LXT304A can replace two cards with one. However, the LXT304A is also compatible with existing dual-card architectures. With an appropriate output transformer, the LXT304A can produce full 6.0 V peak amplitude pulses suitable for D4 Channel Bank applications with separate pulse shaping/LBO cards.

To achieve the 6.0 V peak output, the FCC Part 68-010 Equalizer Code setting is used. (EC = 010). With the standard 1:1.15 transformer, this code produces a 3.0 V peak pulse. However, doubling the transformer turns ratio to 1:2.30 produces the desired 6.0 V peak pulse.

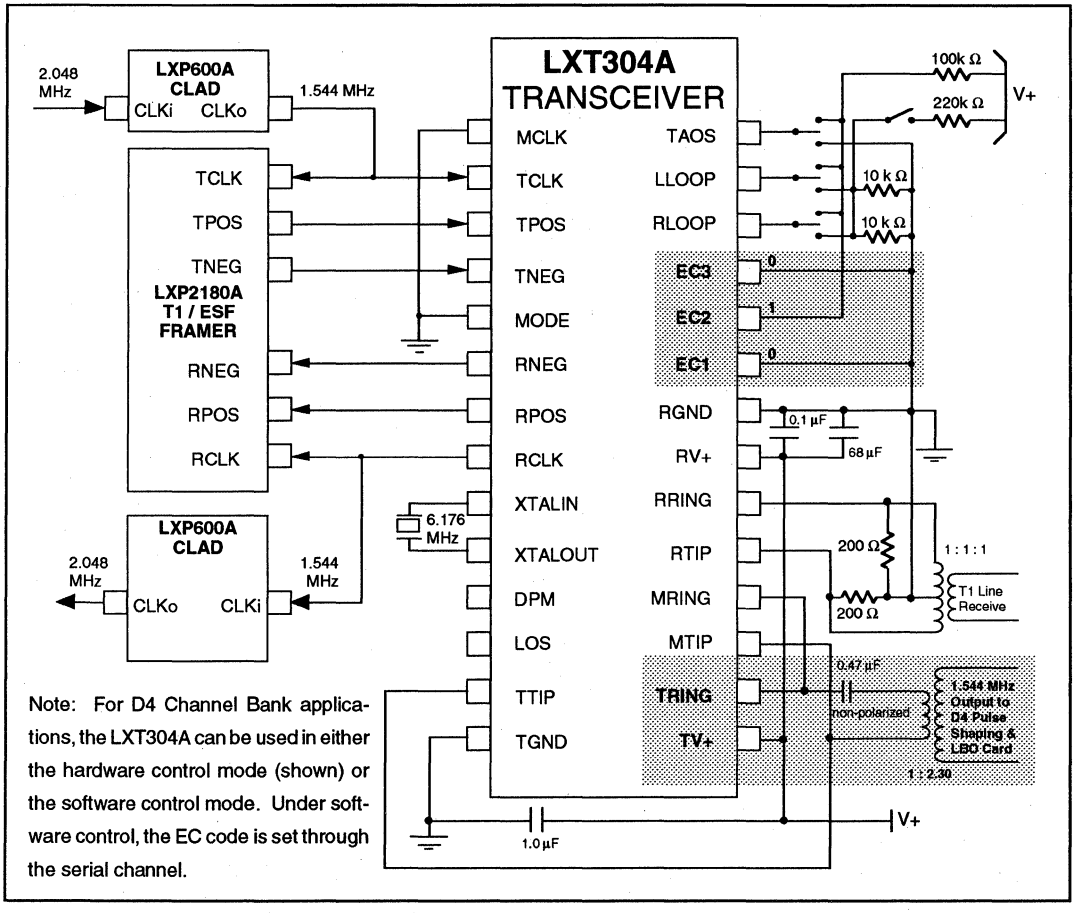
Figure 12 shows a D4 Channel Bank application circuit using the correct Equalizer Code setting and transformer. Transformer specifications are listed in Table 11. Vendors supplying suitable transformers include Pulse Engineering, Bel Fuse, Midcom and Schott. Application circuit functionality was confirmed using a Pulse Engineering PE65558 transformer.

Table 11: Transformer Specifications

Parameter	Value
Turns Ratio	1:2.3 (±5 %)
Primary Inductance	1.2 mH min
Leakage Inductance	0.5 µH max
Interwinding Capacitance	25 pF max
Series Resistance	1.0 Ω PRI

Note: Typical pulse undershoot = 30% (±10) %.

Figure 12: LXT304A 1.544 MHz D4 Channel Bank Applications (Hardware Mode)



Note: For D4 Channel Bank applications, the LXT304A can be used in either the hardware control mode (shown) or the software control mode. Under software control, the EC code is set through the serial channel.

NOTES:

LXT305

T1/E1 Integrated Short Haul Transceiver with Transmit Jitter Attenuation

General Description

The LXT305 is a fully integrated transceiver for both North American 1.544 MHz (T1), and European 2.048 MHz (E1) applications. Transmit pulse shapes (T1 or E1) are selectable for various line lengths and cable types.

The LXT305 provides transmit jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface. It is especially well suited for applications involving T1 and higher rates such as M13 mux, SONET, etc. A variety of diagnostic features including transmit and receive monitoring are incorporated. Clock inputs may be derived from an on-chip crystal oscillator or digital inputs.

The LXT305, an advanced double-poly, double-metal CMOS device, requires only a single 5-volt power supply.

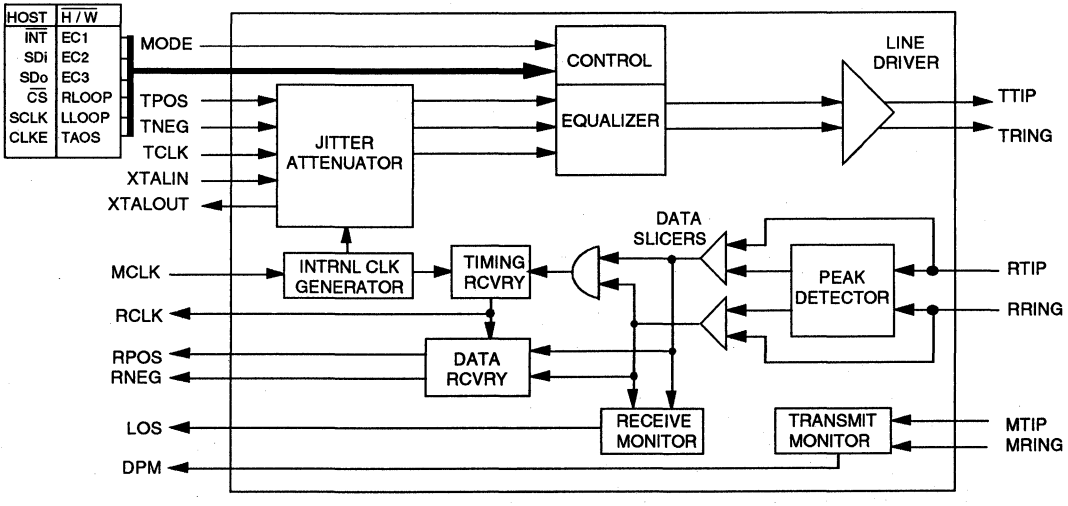
Applications

- SONET Equipment
- M13 Multiplexers
- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

Features

- Compatible with most popular PCM framers including the LXP2180A and LXP2181A
- Line driver, data recovery and clock recovery functions
- Minimum receive signal of 500 mV
- Selectable slicer levels (T1/E1) improve SNR
- Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- Local and remote loopback functions
- Transmit Driver Performance Monitor (DPM) output
- Receive monitor with Loss of Signal (LOS) output
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Pin and functional compatibility with Crystal CS61535
- Replaces CS61534
- Transmit jitter attenuation starting at 3 Hz
- Microprocessor controllable
- Available in 28 pin DIP and PLCC

Figure 1: LXT305 Block Diagram



Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	–	6.0	V
Input voltage, any pin [1]	V_{IN}	RGND - 0.3	RV+ + 0.3	V
Input current, any pin [2]	I_{IN}	-10	10	mA
Ambient operating temperature	T_A	-40	85	°C
Storage temperature	T_{STG}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation not guaranteed at these extremes.
[1] Excluding RTIP and RRING which must stay within -6V to RV + 0.3V.
[2] Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100mA.

Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
DC supply [3]	RV+, TV+	4.75	5.0	5.25	V	
Ambient operating temperature	T_A	-40	25	85	°C	
Total power dissipation [4]	P_D	-	620	–	mW	100% ones density & maximum line length @ 5.25 V

[3] TV+ must not exceed RV+ by more than 0.3 V.
[4] Power dissipation while driving 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

Digital Characteristics (T_A = -40° to 85°C, V+ = 5.0 V ±5%, GND = 0 V)

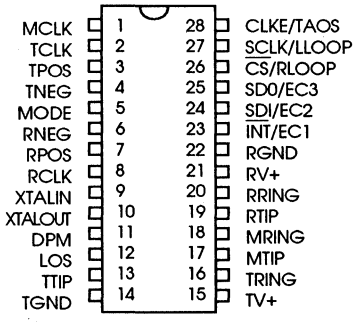
Parameter	Sym	Min	Typ	Max	Units	Test Conditions
High level input voltage [5,6] (pins 1-5, 10, 23-28)	V_{IH}	2.0	–	–	V	
Low level input voltage [5,6] (pins 1-5, 10, 23-28)	V_{IL}	–	–	0.8	V	
High level output voltage [5,6] (pins 6-8, 11, 12, 23, 25)	V_{OH}	2.4	–	–	V	I_{OUT}=- 400 µA
Low level output voltage [5,6] (pins 6-8, 11, 12, 23, 25)	V_{OL}	–	–	0.4	V	I_{OUT}=1.6mA
Input leakage current	I_{LL}	-10	–	+10	µA	
Three-state leakage current [5] (pin 25)	I_{3L}	-10	–	+10	µA	

[5] Functionality of pins 23 and 25 depends on mode. See Host / Hardware Mode descriptions.
[6] Output drivers will output CMOS logic levels into CMOS loads.

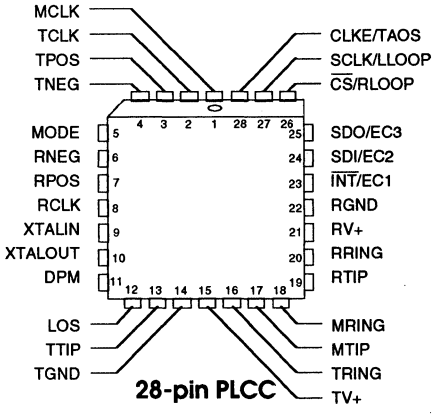
Analog Specifications (T_A = -40° to 85°C, V+ = 5.0 V ±5%, GND = 0 V)

Parameter		Min	Typ	Max	Units	Test Conditions
AMI Output Pulse Amplitudes	T1	2.4	3.0	3.6	V	measured at the DSX
	E1	2.7	3.0	3.3	V	measured at line side
Recommended Output Load at TTIP and TRING		–	25	–	Ω	
Jitter added by the transmitter [7]	10Hz - 8kHz	–	–	0.01	UI	
	8kHz - 40 kHz	–	–	0.025	UI	
	10Hz - 40 kHz	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Sensitivity below DSX	(0dB = 2.4V)	13.6	–	–	dB	
		500	–	–	mV	
Loss of Signal threshold		–	0.3	–	V	
Data decision threshold	T1	63	70	77	%peak	
	E1	43	50	57	% peak	
Allowable consecutive zeros before LOS		160	175	190	–	
Input jitter tolerance	10kHz - 100kHz	0.4	–	–	UI	
Jitter attenuation curve corner frequency [8]		–	3	–	Hz	

[7] Input signal to TCLK is jitter-free.
[8] Circuit attenuates jitter at 20 dB/decade above the corner frequency.



28-pin DIP



28-pin PLCC

2

Pin Descriptions

Pin #	Sym	I/O	Name	Description
1	MCLK	I	Master Clock	A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
2	TCLK	I	Transmit Clock	Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK. Except during remote loopback, the transmitter remains powered down if TCLK is not supplied.
3	TPOS	I	Transmit Positive Data	Input for positive pulse to be transmitted on the twisted-pair line.
4	TNEG	I	Transmit Negative Data	Input for negative pulse to be transmitted on the twisted-pair line.
5	MODE	I	Mode Select	Setting MODE to logic 1 puts the LXT305 in the Host mode. In the Host mode, the serial interface is used to control the LXT305 and determine its status. Setting MODE to logic 0 puts the LXT305 in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status.
6	RNEG	O	Receive Negative Data	Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). In the Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware mode both outputs are stable and valid on the rising edge of RCLK.
7	RPOS	O	Receive Positive Data	
8	RCLK	O	Recovered Clock	This is the clock recovered from the signal received at RTIP and RRING.

Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
9	XTALIN	I	Crystal Input	An external crystal operating at four times the bit rate (6.176 MHz for T1, 8.192 MHz for E1 applications) with an 18.7pF load is required to enable the jitter attenuation function of the LXT305. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
10	XTALOUT	O	Crystal Output	
11	DPM	O	Driver Performance Monitor	DPM goes to a logic 1 when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains at logic 1 until a signal is detected.
12	LOS	O	Loss Of Signal	LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when a mark is received.
13	TTIP	O	Transmit Tip	Differential Driver Outputs. These outputs are designed to drive a 25 Ω load. The transmitter will drive 100 Ω shielded twisted-pair cable through a 2:1 step-up transformer without additional components. To drive 75Ω coaxial cable, two 2.2 Ω resistors are required in series with the transformer.
16	TRING	O	Transmit Ring	
14	TGND	-	Transmit Ground	Ground return for the transmit drivers power supply TV+.
15	TV+	I	Transmit Power Supply	+5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3V.
17	MTIP	I	Monitor Tip	These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another LXT305 on the board. *Host mode only:* To prevent false interrupts in the host mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-level voltage. The monitor clock can range from 100kHz to the TCLK frequency.
18	MRING	I	Monitor Ring	
19	RTIP	I	Receive Tip	The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
20	RRING	I	Receive Ring	
21	RV+	I	Receive Power Supply	+5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	-	Receive Ground	Ground return for power supply RV+.

Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
23	$\overline{INT}$	O	Interrupt *(Host Mode)*	This LXT305 Host mode output goes low to flag the host processor when LOS or DPM go active. $\overline{INT}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{INT}$ is reset by clearing the respective register bit (LOS and/or DPM.)
	EC1	I	Equalizer Control 1 *(H/W Mode)*	The signal applied at this pin in the LXT305 Hardware mode is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
24	SDI	I	Serial Data In *(Host Mode)*	The serial data input stream is applied to this pin when the LXT305 operates in the Host mode. SDI is sampled on the rising edge of SCLK.
	EC2	I	Equalizer Control 2 *(H/W Mode)*	The signal applied at this pin in the LXT305 Hardware mode is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
25	SDO	O	Serial Data Out *(Host Mode)*	The serial data from the on-chip register is output on this pin in the LXT305 Host mode. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is high.
	EC3	I	Equalizer Control 3 *(H/W Mode)*	The signal applied at this pin in the LXT305 Hardware mode is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
26	$\overline{CS}$	I	Chip Select *(Host Mode)*	This input is used to access the serial interface in the LXT305 Host mode. For each read or write operation, $\overline{CS}$ must transition from high to low, and remain low.
	RLOOP	I	Remote Loopback *(H/W Mode)*	This input controls loopback functions in the LXT305 Hardware mode. Setting RLOOP to a logic 1 enables the Remote Loopback mode. Setting both RLOOP and LLOOP causes a Reset .
27	SCLK	I	Serial Clock *(Host Mode)*	This clock is used in the LXT305 Host mode to write data to or read data from the serial interface registers.
	LLOOP	I	Local Loopback *(H/W Mode)*	This input controls loopback functions in the LXT305 Hardware mode. Setting LLOOP to a logic 1 enables the Local Loopback Mode.
28	CLKE	I	Clock Edge *(Host Mode)*	Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	I	Transmit All Ones *(H/W Mode)*	When set to a logic 1, TAOS causes the LXT305 (Hardware mode) to transmit a continuous stream of marks at the MCLK frequency.

Functional Description

The LXT305 is a fully integrated PCM transceiver for both 1.544 MHz (T1) and 2.048 MHz (E1) applications which allows full-duplex transmission of digital data over existing twisted-pair installations.

Figure 1 is a simplified block diagram of the LXT305. The LXT305 transceiver interfaces with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

Transmitter

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). If TCLK is not supplied, the transmitter remains powered down (except during remote loopback). The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 1. Refer to Table 2 and Figure 2 for master and transmit clock timing characteristics. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Equalizer Control signals may be hardwired in the Hardware mode, or input as part of the serial data stream (SDI) in the Host mode.

Pulses can be shaped for either 1.544 or 2.048 MHz applications. 1.544 MHz pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The LXT305 also matches FCC and ECSA specifications for CSU applications. 2.048 MHz pulses can drive either coaxial or shielded twisted-pair lines using appropriate resistors in line with the output transformer.

Jitter Attenuation

Jitter attenuation of the LXT305 transmit outputs is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 3 for crystal specifications. The ES is a 32 x 2-bit register. Transmit data is clocked into the ES with the transmit clock (TCLK) signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the transmit path.

Driver Performance Monitor

The transceiver incorporates a Driver Performance Monitor (DPM) connected in parallel with TTIP and TRING at the output transformer. The DPM output level goes high upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

Line Code

The LXT305 transmits data as a 50% AMI line code as shown in Figure 3. Power consumption is reduced by activating the AMI line driver only to transmit a mark. The output driver is disabled during transmission of a space.

Table 1: Equalizer Control Inputs

EC3	EC2	EC1	Line Length[1]	Cable Loss[2]	Application	Frequency
0	1	1	0 - 133 ft ABAM	0.6 dB	DSX-1	1.544 MHz
1	0	0	133 - 266 ft ABAM	1.2 dB		
1	0	1	266 - 399 ft ABAM	1.8 dB		
1	1	0	399 - 533 ft ABAM	2.4 dB		
1	1	1	533 - 655 ft ABAM	3.0 dB		
0	0	0	CCITT Recommendation G.703		E1	2.048 MHz
0	1	0	FCC Part 68, Option A		CSU (DS-1)	1.544 MHz

[1] Line length from transceiver to DSX-1 cross-connect point.
[2] Maximum cable loss at 772 kHz.

Table 2: LXT305 Master Clock and Transmit Timing Characteristics (See Figure 2)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	T1	MCLK	-	1.544	-	MHz
	E1	MCLK	-	2.048	-	MHz
Master clock tolerance		MCLKt	-	±100	-	ppm
Master clock duty cycle		MCLKd	40	-	60	%
Crystal frequency	T1	fc	-	6.176	-	MHz
	E1	fc	-	8.192	-	MHz
Transmit clock frequency	T1	TCLK	-	1.544	-	MHz
	E1	TCLK	-	2.048	-	MHz
Transmit clock tolerance		TCLKt	-	-	±50	ppm
Transmit clock duty cycle		TCLKd	10	-	90	%
TPOS/TNEG to TCLK setup time		t_{SUT}	25	-	-	ns
TCLK to TPOS/TNEG Hold time		t_{HT}	25	-	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 2: LXT305 Transmit Clock Timing Diagram

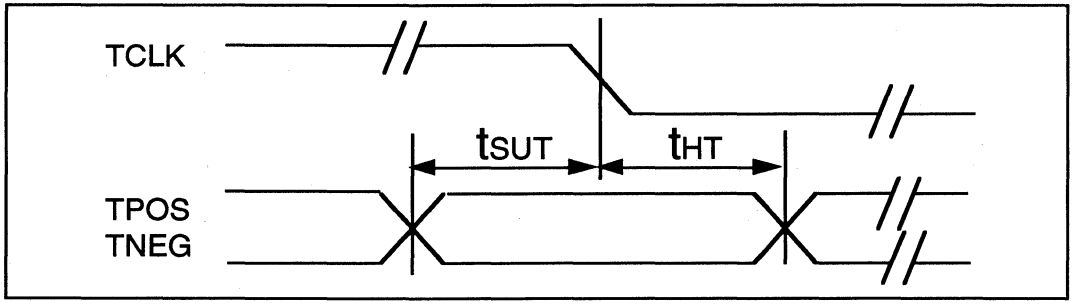
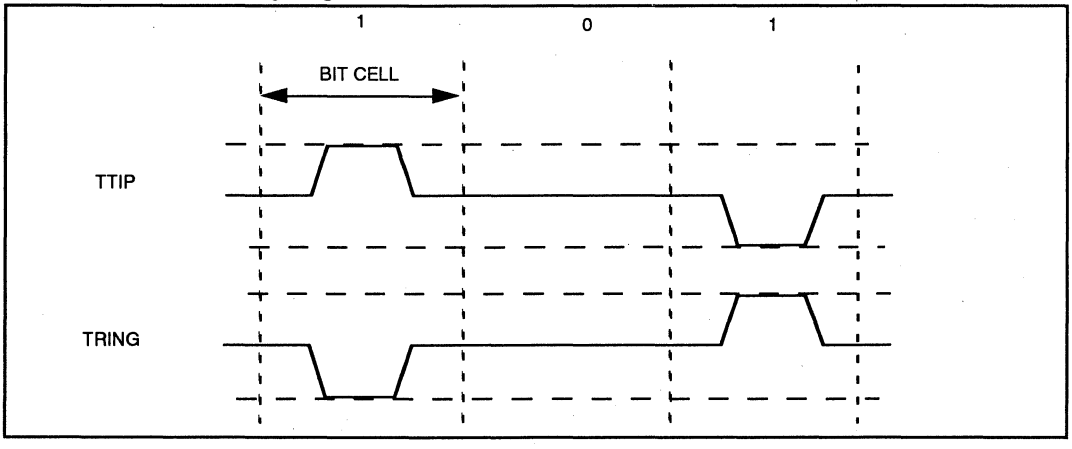


Figure 3: 50% AMI Coding Diagram



Receiver

The signal is received from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Table 4 and Figure 4 for LXT305 receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For T1 applications (determined by Equalizer Control inputs EC1 - EC3 ≠ 000) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (EC inputs = 000) the threshold is set to 50 %.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum cable length is 1500 feet of ABAM cable (approximately 6 dB). Regardless of received signal level, the peak detectors are held above a minimum level of .3 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The receive monitor generates a Loss of Signal (LOS) output upon receipt of 175 consecutive zeros (spaces). The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and the RCLK output is replaced with the MCLK. The LOS output is reset when a mark is received.

Operating Modes

The LXT305 transceiver can be controlled by a microprocessor through the serial interface (Host mode), or through hard-wired pins (Hardware mode). The mode of operation is set by the MODE pin logic level. The transceivers can also be commanded to operate in one of several diagnostic modes.

Table 3: LXT305 Crystal Specifications (External)

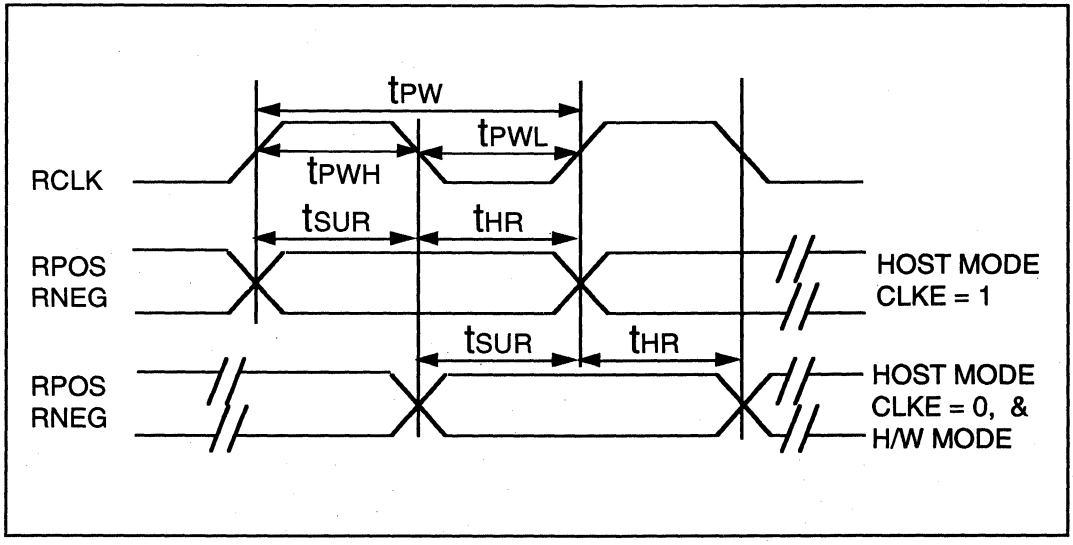
Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency Stability	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical

Table 4: LXT305 Receive Characteristics (See Figure 4)

Parameter		Sym	Min	Typ[1]	Max	Units
Receive slicer threshold	T1	RST	65	70	75	%
	E1	RST	45	50	55	%
Receive clock duty cycle [2]	T1	RCLKd	40	50	60	%
	E1	RCLKd	40	50	60	%
Receive clock pulse width [2]	T1	t_{PW}	594	648	702	ns
	E1	t_{PW}	447	488	529	ns
Receive clock pulse width high	T1	t_{PWH}	-	324	-	ns
	E1	t_{PWH}	-	244	-	ns
Receive clock pulse width low	T1	t_{PWL}	270	324	378	ns
	E1	t_{PWL}	203	244	285	ns
RPOS / RNEG to RCLK rising setup time	T1	t_{SUR}	50	270	-	ns
	E1	t_{SUR}	50	203	-	ns
RCLK rising to RPOS / RNEG hold time	T1	t_{HR}	50	270	-	ns
	E1	t_{HR}	50	203	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
[2] RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz, 0.2 UI clock displacement for 2.048 MHz.)

Figure 4: LXT305 Receive Clock Timing Diagram



Host Mode Operation

To allow a host microprocessor to access and control the LXT305 through the serial interface, MODE is set to 1. The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte.

The Host mode provides a latched Interrupt output ($\overline{INT}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as follows:

CLKE	Output	Clock	Valid Edge
LOW	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
HIGH	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

The LXT305 serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The LXT305 contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select ($\overline{CS}$) input to transition from high to low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 5 lists serial data output bit combinations for each status. Serial data structure is shown in Figure 5 and I/O timing characteristics are shown in Table 6, and Figures 6 and 7.

Hardware Mode Operation

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{INT}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS and RNEG outputs are valid on the rising edge of RCLK.

To operate in Hardware mode, MODE must be set to 0. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host mode.

Reset Operation

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. MCLK provides the receiver reference. The crystal oscillator provides the transmitter reference. If the LXT305 crystal oscillator is grounded, MCLK is used as the transmitter reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and then begins calibration.

Table 5: LXT305 Serial Data Output Bits (See Figure 5)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	Local Loopback active
0	1	1	TAOS and Local Loopback active
1	0	0	Remote Loopback active
1	0	1	DPM has changed state since last Clear DPM occurred
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred

Figure 5: LXT305 Serial Interface Data Structure

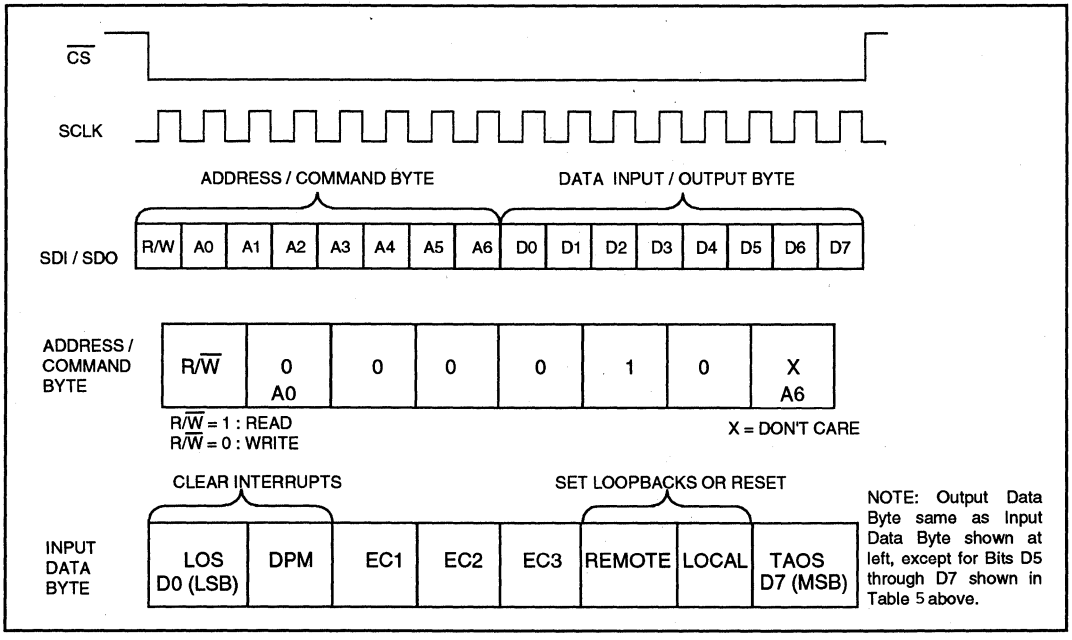


Table 6: LXT305 Serial I/O Timing Characteristics (See Figures 6 and 7)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	-	-	100	ns	Load 1.6 mA, 50pF
SDI to SCLK setup time	t_{DC}	50	-	-	ns	
SCLK to SDI hold time	t_{CDH}	50	-	-	ns	
SCLK low time	t_{CL}	240	-	-	ns	
SCLK high time	t_{CH}	240	-	-	ns	
SCLK rise and fall time	t_R , t_F	-	-	50	ns	
CS to SCLK setup time	t_{CC}	50	-	-	ns	
SCLK to CS hold time	t_{CCH}	50	-	-	ns	
CS inactive time	t_{CWH}	250	-	-	ns	
SCLK to SDO valid	t_{CDV}	-	-	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	-	100	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 6: LXT305 Serial Data Input Timing Diagram

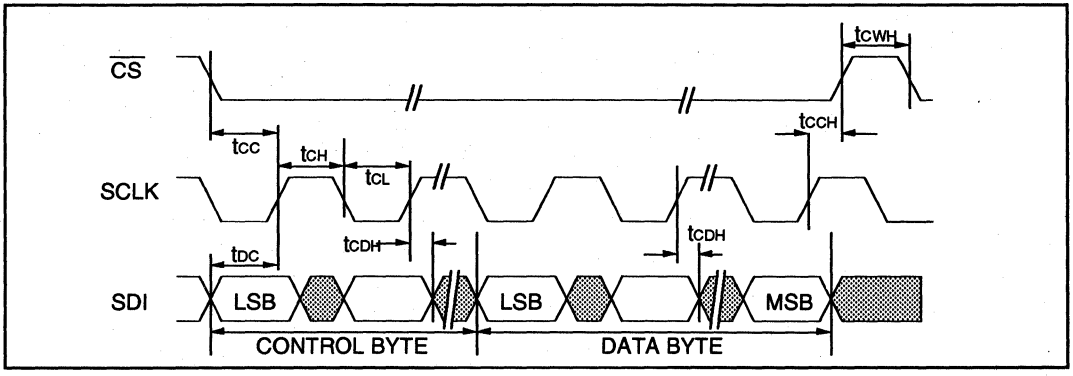
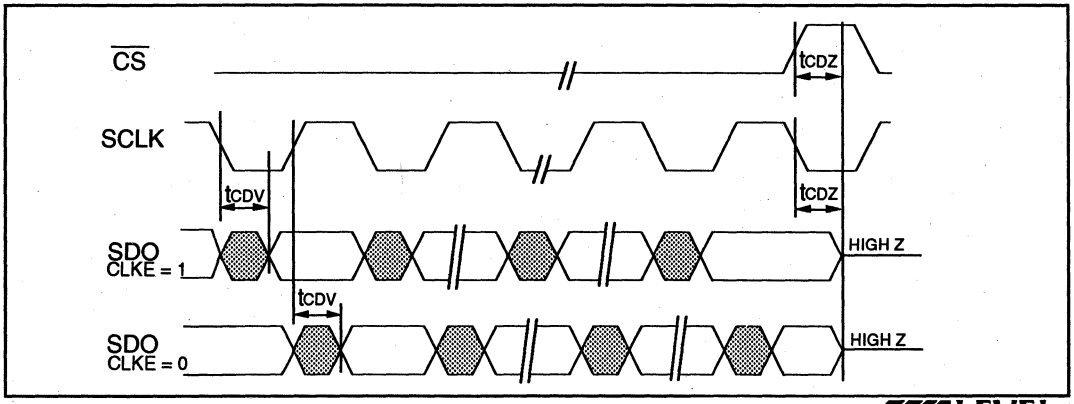


Figure 7: LXT305 Serial Data Output Timing Diagram



Diagnostic Mode Operation

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of 1's at the TCLK frequency when TAOS is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback. During TAOS, the transmitter is locked to MCLK.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK.) The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs will be transmitted normally. (A stream of 1's will be transmitted if the TAOS command is active.)

Power Requirements

The LXT305 is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3V of each other, and decoupled to their respective grounds separately, as shown in Figure 8. Isolation between the transmit and receive circuits is provided internally. Except during remote loopback, the transmitter powers down if TCLK is not supplied.

Applications

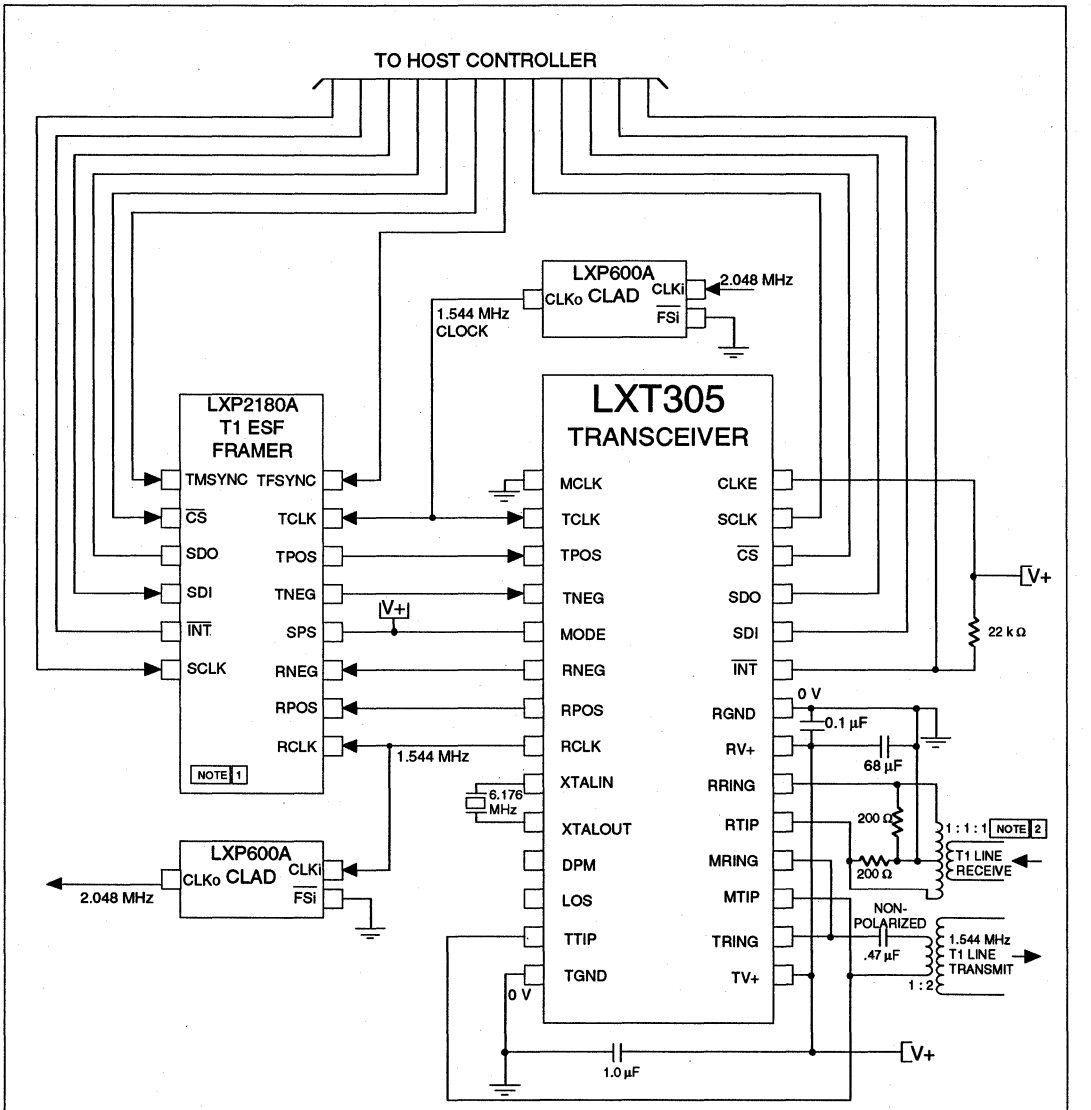
1.544 MHz DSX-1 Interface Applications

Figure 8 is a typical 1.544 MHz DSX-1 application. The LXT305 is shown in the Host mode with the LXP2180A T1/ESF Framer providing the digital interface with the host controller. Both devices are controlled through the serial interface. An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68µF and 0.1 µF on the receive side.)

2.048 MHz E1 Interface Applications

Figure 9 is a typical 2.048 MHz E1 application. The LXT305 is shown in Hardware mode with the LXP2181A E1/CRC4 Framer. Resistors are installed in line with the transmit transformer for loading a 75 Ω coaxial cable. The in-line resistors are not required for transmission on 100 Ω shielded twisted-pair lines. As in the DSX-1 application Figure 8, this configuration is illustrated with a crystal in place to enable the LXT305 Jitter Attenuation Loop, and a single power supply bus. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function.

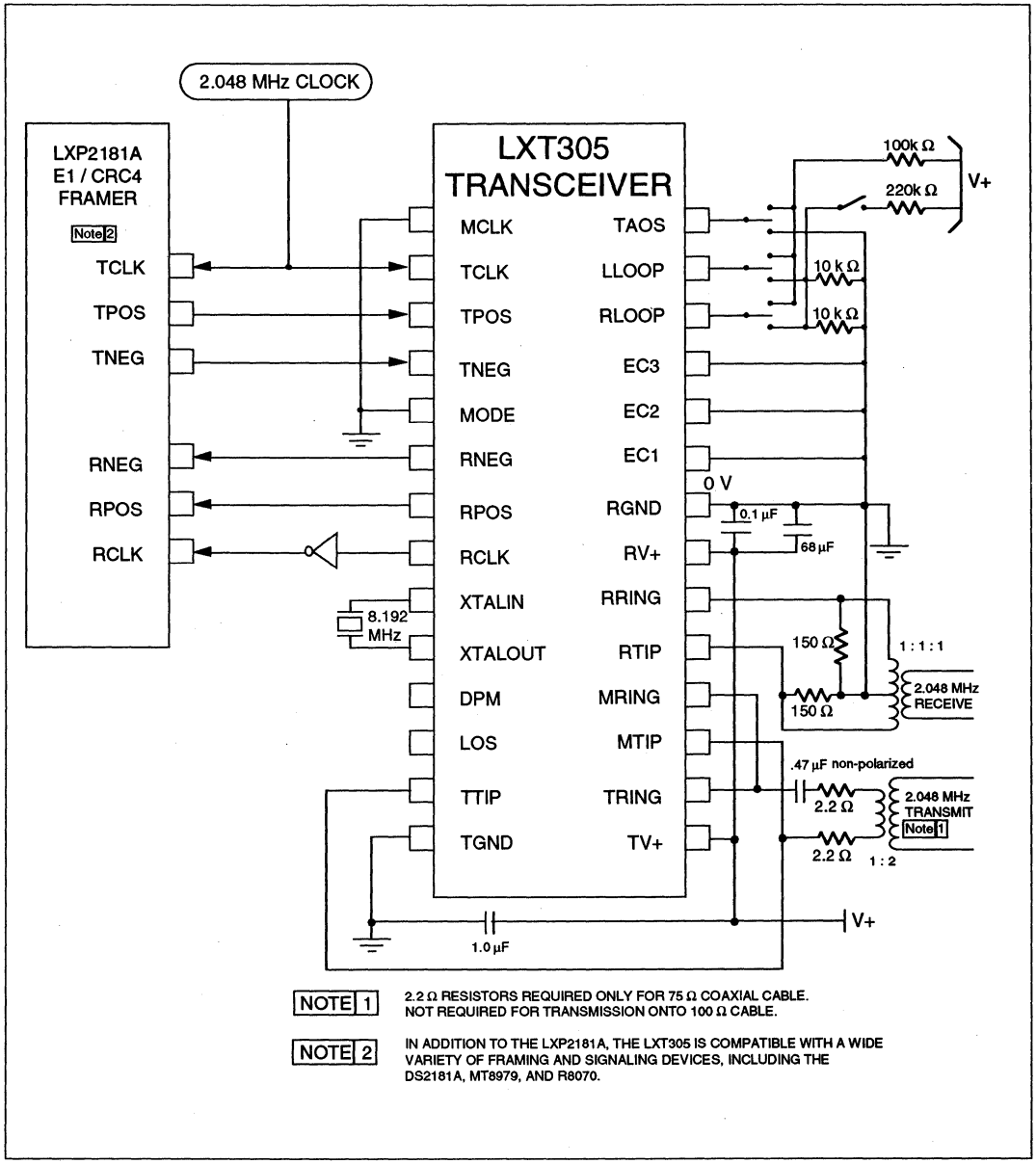
Figure 8: Typical LXT305 1.544 MHz T1 Application (Host Mode)



NOTE 1 IN ADDITION TO THE LXP2180A, THE LXT305 IS COMPATIBLE WITH A WIDE VARIETY OF DIGITAL FRAMING AND SIGNALING DEVICES, INCLUDING THE LXP2181A, DS2180A, MT8976, AND R8070.

NOTE 2 WHEN LXT305 IS CONNECTED TO THE CROSS-CONNECT FRAME THROUGH A LOW LEVEL MONITOR JACK, RECEIVE TRANSFORMER SHOULD BE 1 : 2 : 2 TO BOOST THE INPUT SIGNAL.

Figure 9: Typical LXT305 2.048 MHz E1 Application (Hardware Mode)



NOTES:

LXT305A

Low Power T1/E1 Integrated Short Haul Transceiver with Transmit Jitter Attenuation

General Description

The LXT305A is a fully integrated transceiver for both North American 1.544 MHz (T1), and European 2.048 MHz (E1) applications. Transmit pulse shapes (T1 or E1) are selectable for various line lengths and cable types.

The LXT305A provides transmit jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface. It is especially well suited for applications in which the T1/E1 signals are demultiplexed from a higher rate service such as DS3 or SONET. This demultiplexing results in a "gapped" clock which the 305A smooths out.

The LXT305A, an advanced double-poly, double-metal CMOS device, requires only a single 5-volt power supply.

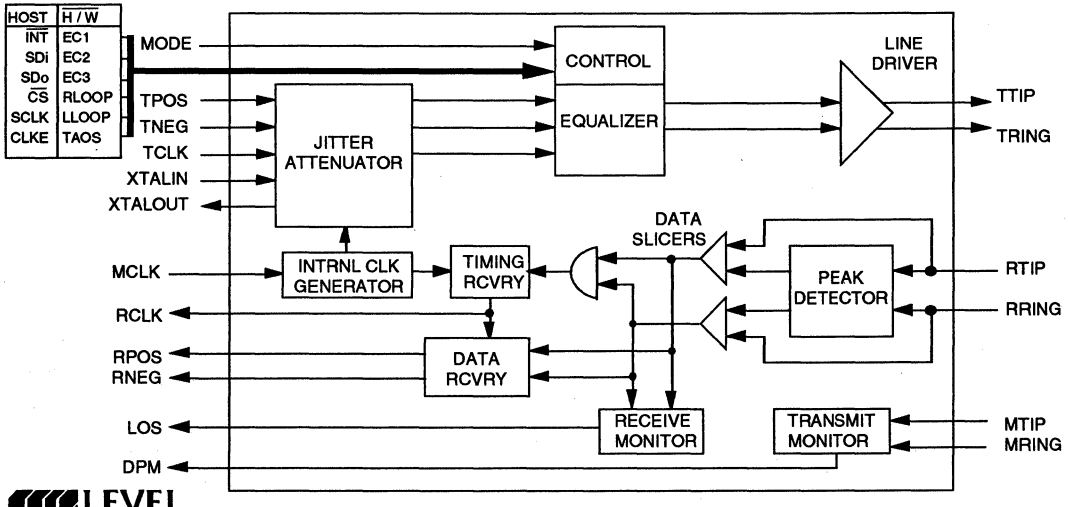
Applications

- SONET Equipment
- M13 Multiplexers
- Digital microwave Radio
- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

Features

- Low power consumption (400 mW maximum) 40% less than the LXT305
- Constant low output impedance transmitter, regardless of data pattern
- Compatible with most popular PCM framers including the LXP2180A and LXP2181A
- Line driver, data recovery and clock recovery functions
- Minimum receive signal of 500 mV
- Selectable slicer levels (T1/E1) improve SNR
- Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- Local and remote loopback functions
- Transmit Driver Performance Monitor (DPM) output
- Receive monitor with Loss of Signal (LOS) output
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Transmit jitter attenuation starting at 3 Hz
- Microprocessor controllable
- Available in 28-pin DIP and PLCC

Figure 1: LXT305A Block Diagram



Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	–	6.0	V
Input voltage, any pin [1]	V_{IN}	RGND - 0.3	RV+ + 0.3	V
Input current, any pin [2]	I_{IN}	-10	10	mA
Ambient operating temperature	T_A	-40	85	°C
Storage temperature	T_{STG}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation not guaranteed at these extremes.
[1] Excluding RTIP and RRING which must stay within -6V to RV + 0.3V.
[2] Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100mA.

Electrical Characteristics (T_A = -40° to 85°C, V+ = 5.0 V ±5%, GND = 0 V)

Parameter	Sym	Min	Max	Units	Test Conditions
Total power dissipation [3]	P_D	–	400	mW	100% ones density & max line length @ 5.25 V
High level input voltage [4,5] (pins 1-5, 10, 23-28)	V_{IH}	2.0	–	V	
Low level input voltage [4,5] (pins 1-5, 10, 23-28)	V_{IL}	–	0.8	V	
High level output voltage [4,5] (pins 6-8, 11, 12, 23, 25)	V_{OH}	2.4	–	V	I_{OUT}=- 400 µA
Low level output voltage [4,5] (pins 6-8, 11, 12, 23, 25)	V_{OL}	–	0.4	V	I_{OUT}=1.6mA
Input leakage current [6]	I_{LL}	0	±10	µA	
Three-state leakage current [4] (pin 25)	I_{3L}	0	±10	µA	

[3] Power dissipation while driving 75 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
[4] Functionality of pins 23 and 25 depends on mode. See Host / Hardware Mode descriptions.
[5] Output drivers will output CMOS logic levels into CMOS loads.
[6] Except MTIP and MRING I_{LL} = ± 50 µA.

Analog Specifications (T_A = -40° to 85°C, V+ = 5.0 V ±5%, GND = 0 V)

Parameter		Min	Typ	Max	Units	Test Conditions
AMI Output Pulse Amplitudes	DSX-1	2.4	3.0	3.6	V	measured at the DSX
	CEPT	2.7	3.0	3.3	V	measured at line side
Recommended output load at TTIP and TRING		–	75	–	Ω	
Jitter added by the transmitter [7]	10Hz - 8kHz	–	–	0.01	UI	
	8kHz - 40 kHz	–	–	0.025	UI	
	10Hz - 40 kHz	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Sensitivity below DSX	(0dB = 2.4V)	13.6	–	–	dB	
		500	–	–	mV	
Loss of Signal threshold		–	0.3	–	V	
Data decision threshold	DSX-1	63	70	77	%peak	
	CEPT	43	50	57	% peak	
Allowable consecutive zeros before LOS		160	175	190	–	
Input jitter tolerance	10kHz - 100kHz	0.4	–	–	UI	
Jitter attenuation curve corner frequency [8]		–	3	–	Hz	

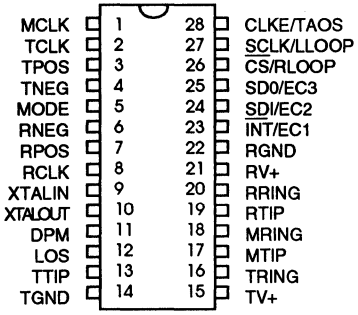
Minimum Return Loss [9,10]	Transmit Min	Transmit Typ	Receive Min	Receive Typ		
51 kHz - 102 kHz	20	28	20	30	dB	
102 kHz - 2.048 MHz	20	28	20	30	dB	
2.048 MHz - 3.072 MHz	20	24	20	25	dB	

[7] Input signal to TCLK is jitter-free.
[8] Circuit attenuates jitter at 20 dB/decade above the corner frequency.
[9] In accordance with CCITT G.703/RC6367A return loss specifications (CEPT), when wired as shown in Figure 9.
[10] Guaranteed by design.

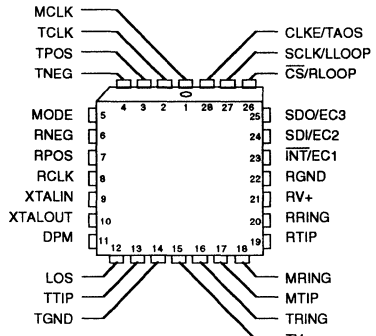
Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
DC supply [1]	RV+, TV+	4.75	5.0	5.25	V
Ambient operating temperature	T_A	-40	25	85	°C

[1] TV+ must not exceed RV+ by more than 0.3 V.



28-pin DIP



28-pin PLCC

Pin Descriptions

Pin #	Sym	I/O	Name	Description
1	MCLK	I	Master Clock	A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
2	TCLK	I	Transmit Clock	Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK.
3	TPOS	I	Transmit Positive Data	Input for positive pulse to be transmitted on the twisted-pair line.
4	TNEG	I	Transmit Negative Data	Input for negative pulse to be transmitted on the twisted-pair line.
5	MODE	I	Mode Select	Setting MODE to logic 1 puts the LXT305A in the Host mode. In the Host mode, the serial interface is used to control the LXT305A and determine its status. Setting MODE to logic 0 puts the LXT305A in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status.
6	RNEG	O	Receive Negative Data	Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). Both outputs are stable and valid on the rising edge of RCLK. In the Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware mode both outputs are stable and valid on the rising edge of RCLK.
7	RPOS	O	Receive Positive Data	
8	RCLK	O	Recovered Clock	This is the clock recovered from the signal received at RTIP and RRING.

Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
9	XTALIN	I	Crystal Input	An external crystal operating at four times the bit rate (6.176 MHz for T1, 8.192 MHz for E1 applications) with an 18.7pF load is required to enable the jitter attenuation function of the LXT305A. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
10	XTALOUT	O	Crystal Output	
11	DPM	O	Driver Performance Monitor	DPM goes to a logic 1 when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains at logic 1 until a signal is detected.
12	LOS	O	Loss Of Signal	LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when the receive signal input reaches 12.5% marks density (4 marks in 32 bit periods) with no more than 15 consecutive zeros.
13	TTIP	O	Transmit Tip	Differential Driver Outputs. These low impedance outputs achieve maximum power savings through a 1:1.15 transformer (T1) or a 1:1 (75 Ω) or 1:1.26 (120 Ω) transformer (E1) without additional components. To provide higher return loss, resistors may be used in series with a transformer as specified in Tables 7, 8 and 9.
16	TRING	O	Transmit Ring	
14	TGND	-	Transmit Ground	Ground return for the transmit drivers power supply TV+.
15	TV+	I	Transmit Power Supply	+5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3V.
17	MTIP	I	Monitor Tip	These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another LXT305A on the board. *Host mode only:* To prevent false interrupts in the host mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-level voltage. The monitor clock can range from 100 kHz to the TCLK frequency.
18	MRING	I	Monitor Ring	
19	RTIP	I	Receive Tip	The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
20	RRING	I	Receive Ring	
21	RV+	I	Receive Power Supply	+5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	-	Receive Ground	Ground return for power supply RV+.

Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
23	$\overline{INT}$	O	Interrupt *(Host Mode)*	This LXT305A Host mode output goes low to flag the host processor when LOS or DPM go active. $\overline{INT}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{INT}$ is reset by clearing the respective register bit (LOS and/or DPM.)
	EC1	I	Equalizer Control 1 *(H/W Mode)*	The signal applied at this pin in the LXT305A Hardware mode is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
24	SDI	I	Serial Data In *(Host Mode)*	The serial data input stream is applied to this pin when the LXT305A operates in the Host mode. SDI is sampled on the rising edge of SCLK.
	EC2	I	Equalizer Control 2 *(H/W Mode)*	The signal applied at this pin in the LXT305A Hardware mode is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
25	SDO	O	Serial Data Out *(Host Mode)*	The serial data from the on-chip register is output on this pin in the LXT305A Host mode. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is high.
	EC3	I	Equalizer Control 3 *(H/W Mode)*	The signal applied at this pin in the LXT305A Hardware mode is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
26	$\overline{CS}$	I	Chip Select *(Host Mode)*	This input is used to access the serial interface in the LXT305A Host mode. For each read or write operation, $\overline{CS}$ must transition from high to low, and remain low.
	RLOOP	I	Remote Loopback *(H/W Mode)*	This input controls loopback functions in the LXT305A Hardware mode. Setting RLOOP to a logic 1 enables the Remote Loopback mode. Setting both RLOOP and LLOOP causes a Reset .
27	SCLK	I	Serial Clock *(Host Mode)*	This clock is used in the LXT305A Host mode to write data to or read data from the serial interface registers.
	LLOOP	I	Local Loopback *(H/W Mode)*	This input controls loopback functions in the LXT305A Hardware mode. Setting LLOOP to a logic 1 enables the Local Loopback Mode.
28	CLKE	I	Clock Edge *(Host Mode)*	Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	I	Transmit All Ones *(H/W Mode)*	When set to a logic 1, TAOS causes the LXT305A (Hardware mode) to transmit a continuous stream of marks at the MCLK frequency.

Functional Description

The LXT305A is a fully integrated PCM transceiver for both 1.544 MHz (T1) and 2.048 MHz (E1) applications which allows full-duplex transmission of digital data over existing twisted-pair installations.

Figure 1 is a simplified block diagram of the LXT305. The LXT305A transceiver interfaces with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

Transmitter

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 1. Refer to Table 2 and Figure 2 for master and transmit clock timing characteristics. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Equalizer Control signals may be hardwired in the Hardware mode, or input as part of the serial data stream (SDI) in the Host mode.

Pulses can be shaped for either 1.544 or 2.048 MHz applications. 1.544 MHz pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The LXT305A also matches FCC and ECSA specifications for CSU applications. 2.048 MHz pulses can drive either coaxial or shielded twisted-pair lines.

Jitter Attenuation

Jitter attenuation of the LXT305A transmit outputs is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 3 for crystal specifications. The ES is a 32 x 2-bit register. Transmit data is clocked into the ES with the transmit clock (TCLK) signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the transmit path.

Driver Performance Monitor

The transceiver incorporates a Driver Performance Monitor (DPM) connected in parallel with TTIP and TRING at the output transformer. The DPM output level goes high upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

Line Code

The LXT305A transmits data as a 50% AMI line code as shown in Figure 3. The output driver maintains a constant low output impedance of 3 Ω (typical) regardless of whether it is driving marks or spaces. This well controlled output impedance provides excellent return loss (> 20 dB) when used with external 9.4 Ω precision resistors (± 1% accuracy) in series with a transmit transformer with a turns ratio of 1:2.3 (± 2% accuracy) . Series resistors also provide increased surge protection and reduced short circuit current flow.

Table 1: Equalizer Control Inputs

EC3	EC2	EC1	Line Length[1]	Cable Loss[2]	Application	Frequency
0	1	1	0 - 133 ft ABAM	0.6 dB	DSX-1	1.544 MHz
1	0	0	133 - 266 ft ABAM	1.2 dB		
1	0	1	266 - 399 ft ABAM	1.8 dB		
1	1	0	399 - 533 ft ABAM	2.4 dB		
1	1	1	533 - 655 ft ABAM	3.0 dB		
0	0	0	CCITT Recommendation G.703		E1 - Coax	2.048 MHz
0	0	1			E1 - Twisted-Pair	
0	1	0	FCC Part 68, Option A		CSU (DS-1)	1.544 MHz

[1] Line length from transceiver to DSX-1 cross-connect point.
[2] Maximum cable loss at 772 kHz.

Table 2: LXT305A Master Clock and Transmit Timing Characteristics (See Figure 2)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	T1	MCLK	-	1.544	-	MHz
	E1	MCLK	-	2.048	-	MHz
Master clock tolerance		MCLKt	-	±100	-	ppm
Master clock duty cycle		MCLKd	40	-	60	%
Crystal frequency	T1	fc	-	6.176	-	MHz
	E1	fc	-	8.192	-	MHz
Transmit clock frequency	T1	TCLK	-	1.544	-	MHz
	E1	TCLK	-	2.048	-	MHz
Transmit clock tolerance		TCLKt	-	-	±50	ppm
Transmit clock duty cycle		TCLKd	10	-	90	%
TPOS/TNEG to TCLK setup time		t_{SUT}	25	-	-	ns
TCLK to TPOS/TNEG Hold time		t_{HT}	25	-	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 2: LXT305A Transmit Clock Timing Diagram

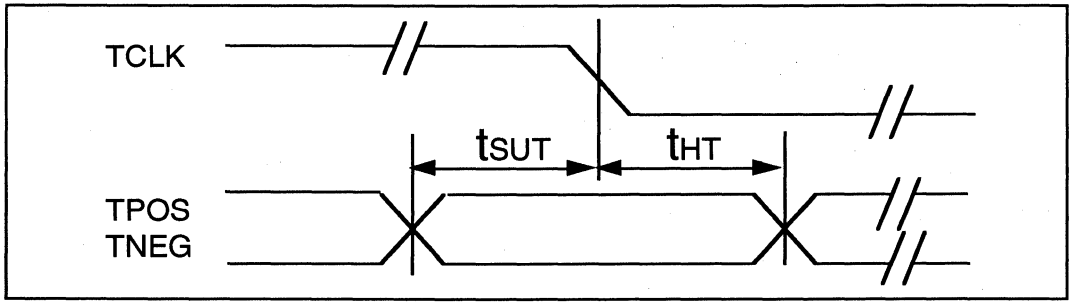
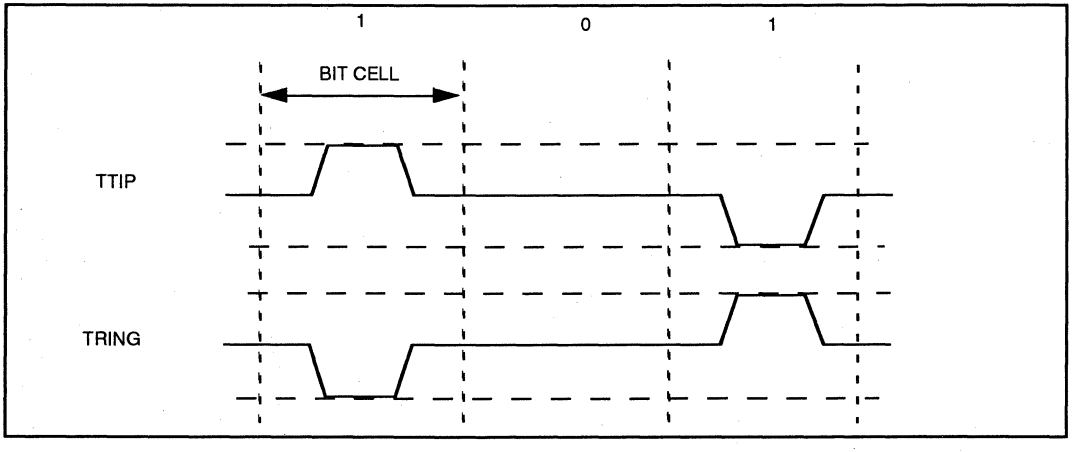


Figure 3: 50% AMI Coding Diagram



Receiver

The signal is received from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Table 4 and Figure 4 for LXT305A receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For T1 applications (determined by Equalizer Control inputs EC1 - EC3 ≠ 000 or 001) the

Table 3: LXT305A Crystal Specifications (External)

Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency Stability	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)
Pullability	CL = 11.7 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 11.7 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical

Table 4: LXT305A Receive Characteristics (See Figure 4)

Parameter		Sym	Min	Typ[1]	Max	Units
Receive slicer threshold	T1	RST	65	70	75	%
	E1	RST	45	50	55	%
Receive clock duty cycle [2]	T1	RCLKd	40	50	60	%
	E1	RCLKd	40	50	60	%
Receive clock pulse width [2]	T1	t_{PW}	594	648	702	ns
	E1	t_{PW}	447	488	529	ns
Receive clock pulse width high	T1	t_{PWH}	-	324	-	ns
	E1	t_{PWH}	-	244	-	ns
Receive clock pulse width low	T1	t_{PWL}	270	324	378	ns
	E1	t_{PWL}	203	244	285	ns
RPOS / RNEG to RCLK rising setup time	T1	t_{SUR}	50	270	-	ns
	E1	t_{SUR}	50	203	-	ns
RCLK rising to RPOS / RNEG hold time	T1	t_{HR}	50	270	-	ns
	E1	t_{HR}	50	203	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

[2] RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz, 0.2 UI clock displacement for 2.048 MHz.)

threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (EC inputs = 000 or 001) the threshold is set to 50 %.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum cable length is 1500 feet of ABAM cable (approximately 6 dB). Regardless of received signal level, the peak detectors are held above a minimum level of .3 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The data and clock recovery circuits are highly tolerant, with an input jitter tolerance significantly better than required by Pub 62411, as shown in Figure 5. The receive monitor generates a Loss of Signal (LOS) output upon receipt of 175 consecutive zeros (spaces). The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and the RCLK output is replaced with the MCLK. Received marks are output regardless of the LOS status, but the LOS pin will not reset until the ones density reaches 12.5%. This level is based on receipt of at least 4 ones in any 32 bit periods with no more than 15 consecutive zeros.

Figure 4: LXT305A Receive Clock Timing Diagram

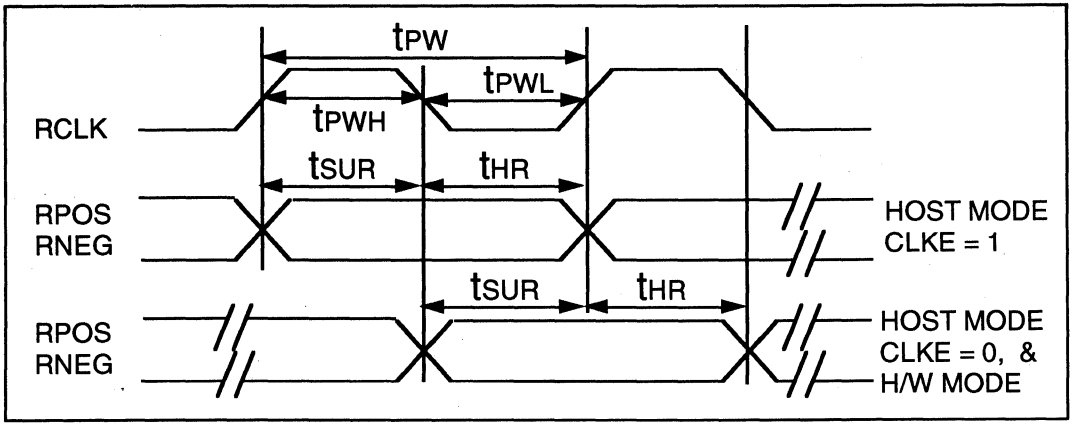
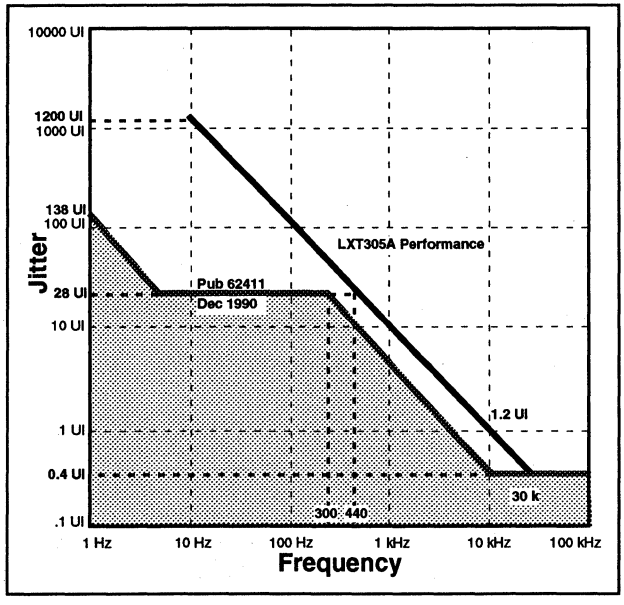


Figure 5: LXT305A Receive Jitter Tolerance



Operating Modes

The LXT305A transceiver can be controlled by a microprocessor through a serial interface (Host mode), or by hard-wired pins (Hardware mode). The mode of operation is set by the MODE pin logic level. The transceivers can also be commanded to operate in one of several diagnostic modes.

Host Mode Operation

To allow a host microprocessor to access and control the LXT305A through the serial interface, MODE is set to 1. The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte.

The Host mode provides a latched Interrupt output ($\overline{INT}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as follows:

CLKE	Output	Clock	Valid Edge
LOW	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
HIGH	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

The LXT305A serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The LXT305A contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select ($\overline{CS}$) input to transition from high to low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 5 lists serial data output bit combinations for each status. Serial data structure is shown in Figure 6 and I/O timing characteristics are shown in Table 6, and Figures 7 and 8.

Hardware Mode Operation

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{INT}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS and RNEG outputs are valid on the rising edge of RCLK.

To operate in Hardware mode, MODE must be set to 0. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host mode.

Reset Operation

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. MCLK provides the receiver reference. The crystal oscillator provides the transmitter reference. If the LXT305A crystal oscillator is grounded, MCLK is used as the transmitter reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0, then calibration begins.

Table 5: LXT305A Serial Data Output Bits (See Figure 6)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	Local Loopback active
0	1	1	TAOS and Local Loopback active
1	0	0	Remote Loopback active
1	0	1	DPM has changed state since last Clear DPM occurred
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred

Figure 6: LXT305A Serial Interface Data Structure

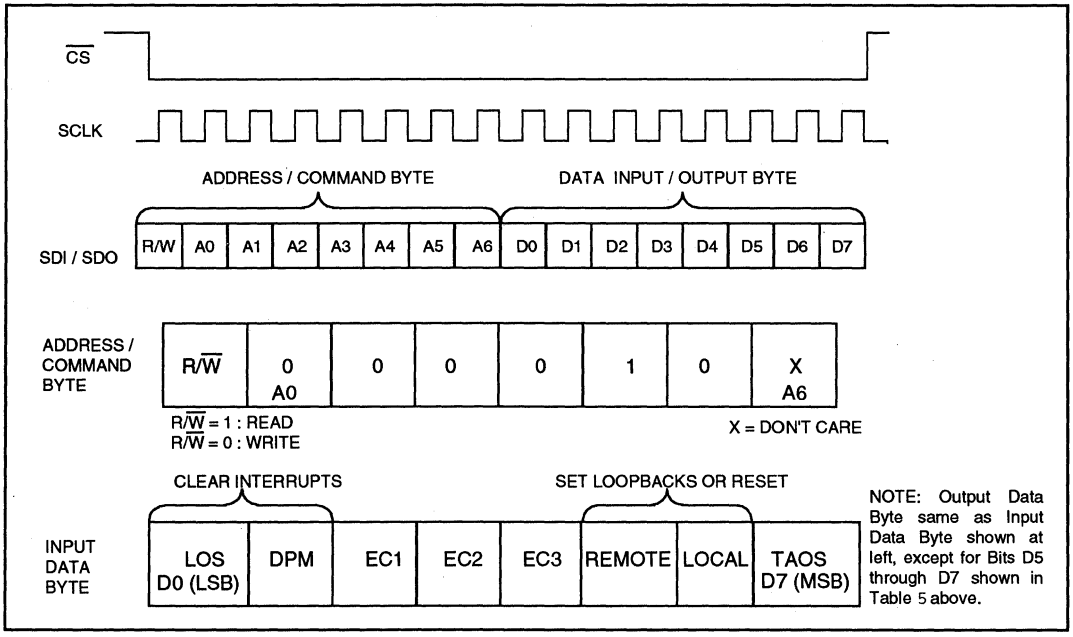


Table 6: LXT305A Serial I/O Timing Characteristics (See Figures 7 and 8)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	-	-	100	ns	Load 1.6 mA, 50pF
SDI to SCLK setup time	t_{DC}	50	-	-	ns	
SCLK to SDI hold time	t_{CDH}	50	-	-	ns	
SCLK low time	t_{CL}	240	-	-	ns	
SCLK high time	t_{CH}	240	-	-	ns	
SCLK rise and fall time	t_R, t_F	-	-	50	ns	
CS to SCLK setup time	t_{CC}	50	-	-	ns	
SCLK to CS hold time	t_{CCH}	50	-	-	ns	
CS inactive time	t_{CWH}	250	-	-	ns	
SCLK to SDO valid	t_{CDV}	-	-	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	-	100	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 7: LXT305A Serial Data Input Timing Diagram

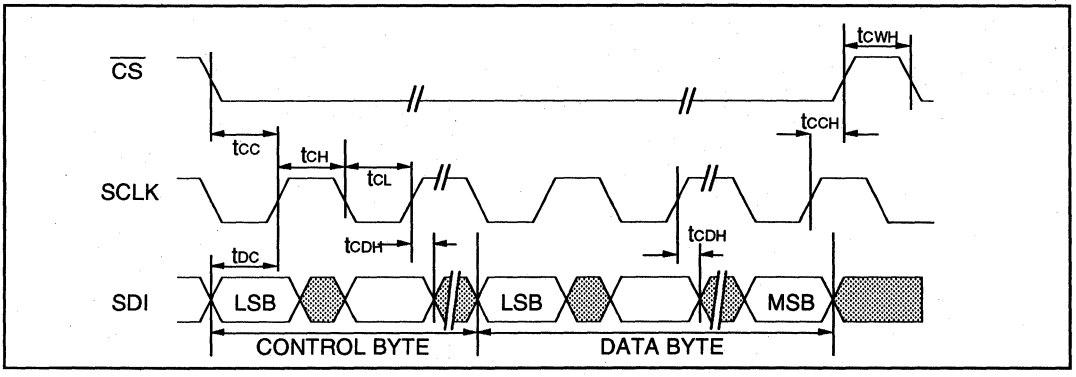
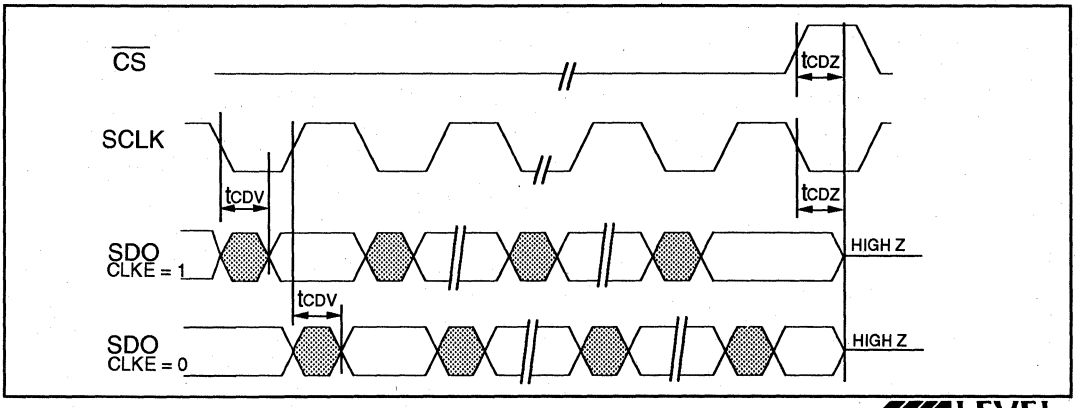


Figure 8: LXT305A Serial Data Output Timing Diagram



Diagnostic Mode Operation

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of 1's when the TAOS mode is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback. During TAOS, the transmitter is locked to MCLK. If MCLK is not supplied, the transmitter powers down.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK.) The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs will be transmitted normally. (A stream of 1's will be transmitted if the TAOS command is active.) During local loopback if TCLK is not supplied, the transmitter powers down. If LOS and LLOOP are both active, LLOOP takes precedence, forcing RCLK = TCLK.

Power Requirements

The LXT305A is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ±.3V of each other, and decoupled to their respective grounds separately, as shown in Figure 9. Isolation between the transmit and receive circuits is provided internally.

The transmitter powers down to conserve power when the required clock input is not supplied. The LXT305A enters the power down mode during normal operation and local loopback if TCLK is not supplied, and during TAOS if MCLK is not supplied.

Applications

1.544 MHz T1 Interface Applications

Figure 9 is a typical 1.544 MHz T1 interface application using a 1:1.15 transmit transformer without in-line resistors for maximum power savings. The LXT305A is shown in the Host mode with the LXP2180A T1/ESF Framer providing the digital interface with the host controller. Both devices are controlled through the serial interface. An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68µF and 0.1 µF on the receive side.)

For DSX-1 applications, series resistors can be used in line with the transmit transformer to provide higher return loss. Table 7 lists transformer ratios, Rt values and typical return loss values for 1.544 MHz EC codes.

2.048 MHz E1 Interface Applications

Figure 10 is a typical 2.048 MHz E1 application. The LXT305A is shown in Hardware mode with the LXP2181A E1/CRC4 Framer. As in the DSX-1 application Figure 9, this configuration is illustrated with a crystal in place to enable the LXT305A Jitter Attenuation Loop, and a single power supply bus. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function. EC3 and EC2 are hardwired to ground, but the EC1 pin is switchable high or low selecting codes 000 and 001. With the 1 : 1 transformer ratio and code 000 selected on the EC inputs, the LXT305A outputs the CCITT specified 2.37 V pulse onto 75 Ω coaxial cable. Simply changing the EC code to 001 allows the LXT305A to match the 3.0 V pulse specification for 120 Ω shielded twisted-pair cable. No transformer change is required. For situations where at 1:1.26 transformer is desired, EC code 000 selects the correct output for 120 Ω twisted-pair cable.

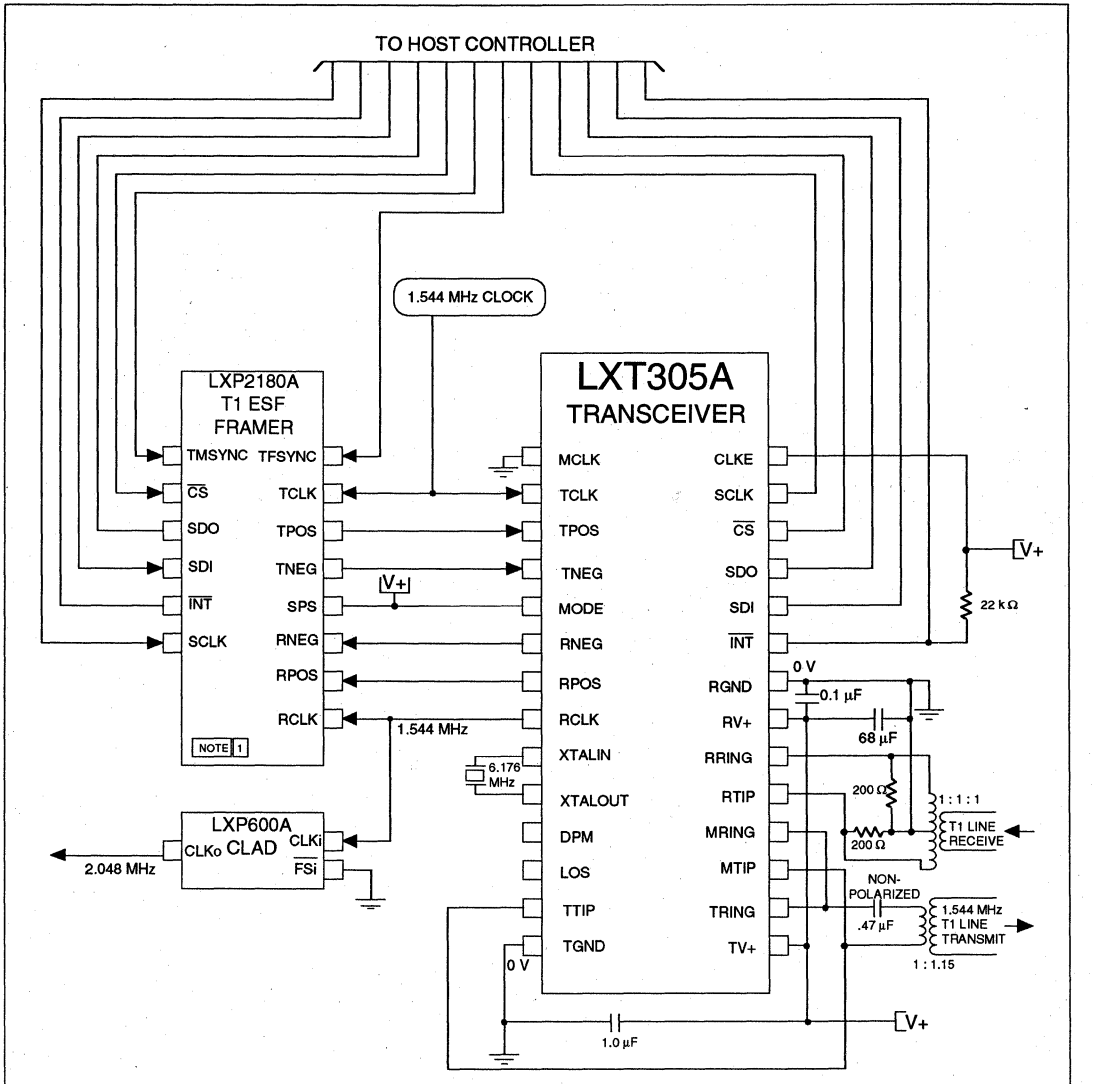
To achieve higher return loss, increased surge protection and lower output short circuit current, series resistors can be used in line with the transmit transformer. Tables 8 and 9 list transformer ratios, series resistor (Rt) and typical return loss values with associated 2.048 MHz EC codes for 75 Ω coax and 120 Ω TWP, respectively.

Table 7: T1/DSX-1 Output Combinations (100 Ω)

EC	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
011 - 111	1 : 1.15	Rt = 0 Ω	0.5 dB
011 - 111	1 : 2	Rt = 9.4 Ω	20 dB
011 - 111	1 : 2.3	Rt = 9.4 Ω	28 dB

[1] Transformer turns ratio accuracy is ± 2 %.
[2] Rt values are ± 1 %.
[3] Typical return loss, 102 kHz - 2.048 MHz band.

Figure 9: Typical LXT305A 1.544 MHz T1 Application (Host Mode)



NOTE 1 IN ADDITION TO THE LXP2180A, THE LXT305A IS COMPATIBLE WITH A WIDE VARIETY OF DIGITAL FRAMING AND SIGNALING DEVICES, INCLUDING THE LXP2181, DS2180A, MT8976, AND R8070.

Table 8: E1/CEPT Output Combinations (75 Ω)

EC	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
0 0 1	1 : 1	Rt = 10 Ω	5 dB
0 0 1	1 : 2	Rt = 14.3 Ω	12 dB
0 0 0	1 : 1	Rt = 0 Ω	0.5 dB
0 0 0	1 : 2	Rt = 9.4 Ω	24 dB

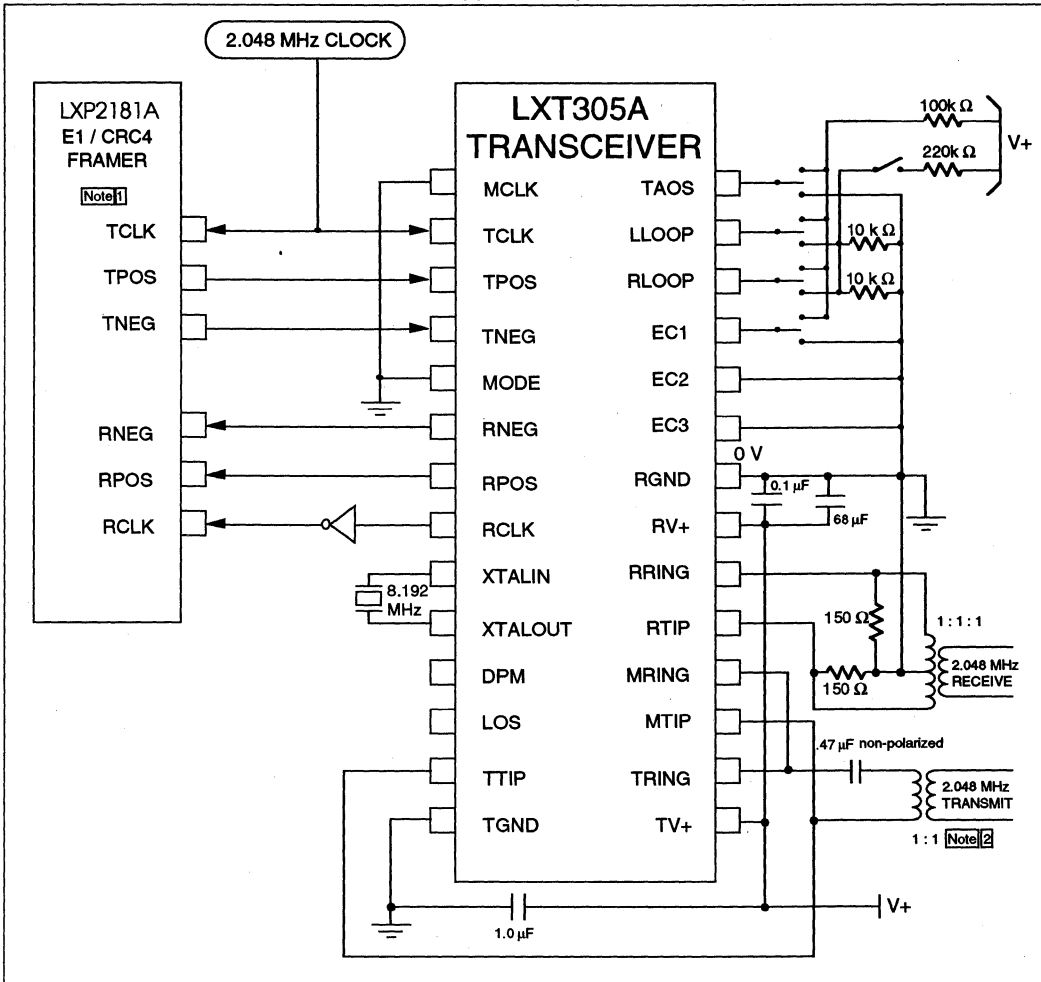
[1] Transformer turns ratio accuracy is ± 2 %.
[2] Rt values are ± 1 %.
[3] Typical return loss, 102 kHz - 2.048 MHz band.

Table 9: E1/CEPT Output Combinations (120 Ω)

EC	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
0 0 1	1 : 1	Rt = 0 Ω	0.5 dB
0 0 1	1 : 2	Rt = 15 Ω	30 dB
0 0 0	1 : 1.26	Rt = 0 Ω	0.5 dB
0 0 0	1 : 2	Rt = 8.7 Ω	12 dB

[3] Transformer turns ratio accuracy is ± 2 %.
[2] Rt values are ± 1 %.
[3] Typical return loss, 102 kHz - 2.048 MHz band.

Figure 10: Typical LXT305A 2.048 MHz E1 Application (Hardware Mode)



NOTE 1 IN ADDITION TO THE LXP2181, THE LXT305A IS COMPATIBLE WITH A WIDE VARIETY OF FRAMING AND SIGNALING DEVICES, INCLUDING THE LXP2180A, DS2181, MT8979, AND R8070.

NOTE 2 FOR 75 Ω COAXIAL CABLE, USE A 1 : 1 TRANSFORMER RATIO AND EC CODE 000.
FOR 120 Ω TWISTED-PAIR CABLE USE EITHER A 1 : 1 TRANSFORMER WITH EC CODE 001, OR A 1 : 1.26 TRANSFORMER WITH CODE 000 .

LXT310

T1 CSU / ISDN PRI Transceiver

General Description

The LXT310 is the first fully integrated transceiver for T1 CSU and ISDN Primary Rate Interface (ISDN PRI) applications at 1.544 MHz. This transceiver operates over 6,000 feet of 22 AWG twisted-pair cable without any external components. To compensate for shorter lines, 7.5 dB, 15 dB, and 22.5 dB frequency-dependent transmit Line Build-Outs (LBOs) are provided.

The device offers selectable B8ZS encoding/decoding, and unipolar or bipolar data I/O. The LXT310 also provides jitter attenuation in either the transmit or receive direction starting at 6 Hz, and incorporates a serial interface (SIO) for microprocessor control.

The LXT310 offers a variety of diagnostic features including loopbacks and loss of signal monitoring. It uses an advanced double-poly, double-metal CMOS process and require only a single 5-volt power supply.

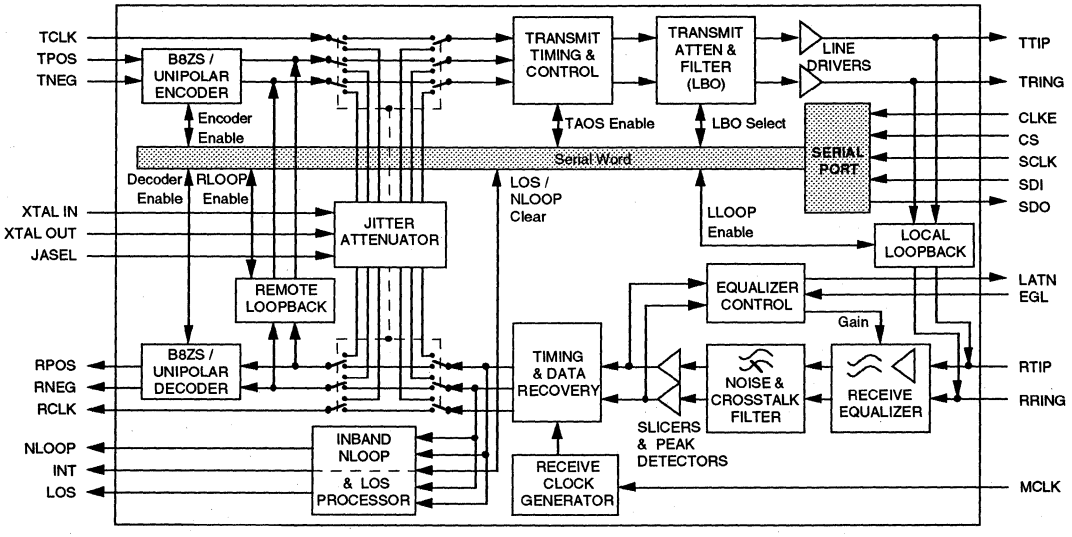
Applications

- ISDN Primary Rate Interface (PRI) (ANSI T1.408)
- CSU interface to T1 Service (Pub 62411)
- DS1 Metallic Interface (ANSI T1.403)
- T1 LAN bridge
- CPU to CPU Channel Extenders
- Digital Loop Carrier - Subscriber Carrier Systems
- T1 Mux
- Channel Banks

Features

- Fully integrated transceiver comprising: on-chip equalizer; timing recovery/control; data processor; receiver; and transmitter with Line Build-Out and digital control
- Meets or exceeds ANSI and CCITT specifications including T1.403, T1.408, and AT&T Pub 62411
- Selectable Receiver Sensitivity. Fully restores the received signal after transmission through a cable with attenuation of either 0 to 26 dB, or 0 to 36 dB @772 kHz
- Selectable Unipolar or Bipolar data I/O
- Selectable B8ZS encoding/decoding
- Line attenuation indication output
- 138 UI jitter tolerance at 1 Hz
- Output short circuit current limit protection
- On-line idle mode for redundant systems
- 7.5 dB, 15 dB, and 22.5 dB transmit LBOs
- Local, remote and inband network loopback functions
- Receive monitor with Loss of Signal (LOS) output
- Jitter attenuation starting at 6 Hz, switchable to transmit or receive path
- Microprocessor controllable

Figure 1: LXT310 Block Diagram



Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	–	6.0	V
Input voltage, any pin	V_{IN}	RGND - 0.3	RV+ + 0.3	V
Input current, any pin [1]	I_{IN}	-10	10	mA
Ambient operating temperature	T_A	-40	85	°C
Storage temperature	T_{STG}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation not guaranteed at these extremes.
[1] Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100mA.

Operating Conditions/Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
DC supply [2]	RV+, TV+	4.75	5.0	5.25	V	
Ambient operating temperature	T_A	–	25	–	°C	
Power dissipation [3]	P_D	–	375	450	mW	100% ones density & maximum line length @ 5.25 V

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
[2] TV+ must not exceed RV+ by more than 0.3 V.
[3] Power dissipation while driving 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

Digital Characteristics (T_A = -40° to 85°C, V+ = 5.0 V ±5%, GND = 0 V)

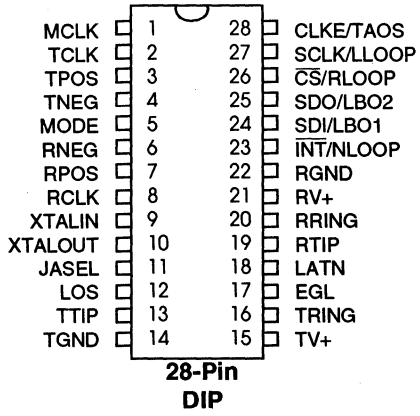
Parameter	Sym	Min	Typ	Max	Units	Test Conditions
High level input voltage [1,2] (pins 1-5, 10, 23-28)	V_{IH}	2.0	–	–	V	
Low level input voltage [1,2] (pins 1-5, 10, 23-28)	V_{IL}	–	–	0.8	V	
High level output voltage [1,2] (pins 6-8, 12, 23, 25)	V_{OH}	2.4	–	–	V	I_{OUT}=- 400 µA
Low level output voltage [1,2] (pins 6-8, 12, 23, 25)	V_{OL}	–	–	0.4	V	I_{OUT}=1.6mA
Input leakage current	I_{LL}	0	–	± 10	µA	
Three-state leakage current[1] (pin 25)	I_{3L}	0	–	± 10	µA	

[1] Functionality of pins 23 and 25 depends on mode. See Host / Hardware Mode descriptions.
[2] Output drivers will output CMOS logic levels into CMOS loads.

Analog Characteristics (T_A = -40° to 85°C, V+ = 5.0 V ±5%, GND = 0 V)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
Recommended output load at TTIP and TRING		50	–	200	Ω	
AMI Output Pulse Amplitudes		2.4	3.0	3.6	V	
Jitter added by the transmitter [2]	10Hz - 8kHz [3]	–	–	0.01	UI	measured at the output with LBO1 = 0, and LBO2 = 0
	8kHz - 40 kHz [3]	–	–	0.02	UI	
	10Hz - 40 kHz [3]	–	–	0.02	UI	
	Broad Band	–	–	0.04	UI	
Receive signal attenuation range @ 772 kHz	Mode 1 (EGL = 1)	0	26	–	dB	
	Mode 2 (EGL = 0)	0	36	–	dB	
Allowable consecutive zeros before LOS		160	175	190	–	
Input jitter tolerance	10kHz - 100kHz	0.4	–	–	UI	0 dB line
	1 Hz	138	–	–	UI	
Jitter attenuation curve corner frequency [4]		–	6	–	Hz	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
[2] Input signal to TCLK is jitter-free.
[3] Guaranteed by characterization; not subject to production testing.
[4] Circuit attenuates jitter at 20 dB/decade above the corner frequency.



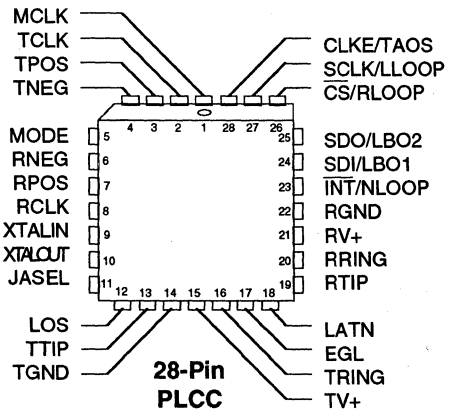


Table 1: Pin Descriptions

Pin #	Sym	I/O	Name	Description
1	MCLK	I	Master Clock	A 1.544 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
2	TCLK	I	Transmit Clock	Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK.
3	TPOS/ TDATA	I	Transmit Data Input	Input data to be transmitted on the twisted-pair line. Normally, pin 3 is TPOS and pin 4 is TNEG, the positive and negative sides of a bipolar input pair. However, if pin 4 is held high for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), the LXT310 switches to a unipolar mode. The LXT310 returns to bipolar I/O when pin 4 goes low.
4	TNEG/ UBS	I	Data Input/ Polarity Select	
5	MODE	I	Mode Select	Setting MODE to logic 1 selects the Host mode. In Host mode, the serial interface is enabled for control and status reporting. Setting MODE to logic 0 selects the Hardware (H/W) mode. In Hardware mode the serial interface is disabled; hard-wired pins control configuration and report status. Tying MODE to RCLK enables Hardware mode and the B8ZS encoder/decoder.
6	RNEG	O	Receive Data Negative	In Bipolar data I/O mode pins 6 and 7 are bipolar data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING, and a signal on RPOS corresponds to a positive pulse on RTIP/RRING. RNEG/ RPOS outputs are Non-Return-to-Zero (NRZ). In Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In Hardware mode both outputs are stable and valid on the RCLK rising edge.
7	RPOS	O	Receive Data Positive	
6	BPV	O	Bipolar Violation	In Unipolar data I/O mode, pin 6 goes high to indicate receipt of a Bipolar Violation of the AMI code.
7	RDATA	O	Receive Data	In Unipolar mode, data received from the twisted-pair line is output at pin 7.
8	RCLK	O	Receive Clock	This is the clock recovered from the signal received at RTIP and RRING.

Table 1: Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
9	XTALIN	I	Crystal Input	An external crystal (18.7 pF load capacitance, pullable) operating at 6.176 MHz (four times the bit rate) is required to enable the jitter attenuation function of the LXT310. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and leaving the XTALOUT pin unconnected.
10	XTALOUT	O	Crystal Output	
11	JASEL	I	Jitter Attenuation Select	Selects jitter attenuation location. When JASEL = 1, the jitter attenuator is active in the receive path. When JASEL = 0, the jitter attenuator is active in the transmit path.
12	LOS	O	Loss Of Signal	LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when the received signal reaches a mark density of 12.5% (determined by receipt of four marks within 32 bit periods.) Received marks are output on RPOS and RNEG even when LOS is at a logic 1.
13	TTIP	O	Transmit Tip	Differential Driver Outputs. These outputs are designed to drive a 50 - 200 Ω load. Line matching resistors and transformer can be selected to give the desired pulse height.
16	TRING	O	Transmit Ring	
14	TGND	-	Tx Ground	Ground return for the transmit drivers power supply TV+.
15	TV+	I	Transmit Power Supply	+5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ± 0.3V.
17	EGL	I	Equalizer Gain Limit	Input sets equalizer gain. When EGL = 0, up to 36 dB of equalizer gain may be added. When EGL = 1, equalizer gain is limited to no more than 26 dB.
18	LATN	O	Line Attenuation Indication (See Figure 6)	Encoded output. Pulse width, relative to RCLK, indicates receive equalizer gain setting (line insertion loss at 772 kHz) in 7.5 dB steps. When LATN = 1 RCLK pulse, the equalizer is set at 7.5 dB gain, 2 pulses = 15 dB, 3 pulses = 22.5 dB and 4 pulses = 0 dB. Output is valid on the rising edge of RCLK.
19	RTIP	I	Receive Tip	The AMI signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
20	RRING	I	Receive Ring	
21	RV+	I	Receive Power Supply	+5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	-	Rx Ground	Ground return for power supply RV+.
23	NLOOP	O	Network Loopback *(H/W Mode)*	When high, indicates Inband Network Loopback has been activated by reception of 00001 pattern for five seconds. NLOOP is reset by reception of 001 for five seconds, or by activation of RLOOP or LLOOP.
	INT	O	Interrupt *(Host Mode)*	This LXT310 Host mode output goes low to flag the host processor when LOS or NLOOP changes state. $\overline{INT}$ is an open drain output and should be tied to power supply RV+ through a resistor. $\overline{INT}$ is reset by clearing the LOS or NLOOP register bit.

Table 1: Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
24	SDI	I	Serial Data In *(Host Mode)*	The serial data input stream is applied to this pin when the LXT310 operates in the Host mode. SDI is sampled on the rising edge of SCLK.
	LBO1	I	Line Build-Out Select 1 *(H/W Mode)*	In Hardware mode this input is used in conjunction with LBO2 to select the transmit line build-outs: 00 = 0 dB, 01 = 7.5 dB, 10 = 15 dB, and 11 = 22.5 dB.
25	SDO	O	Serial Data Out *(Host Mode)*	The serial data from the on-chip register is output on this pin in the LXT310 Host mode. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is high.
	LBO2	I	Line Build-Out Select 2 *(H/W Mode)*	The signal applied at this pin in the LXT310 Hardware mode is used in conjunction with LBO1 to select the transmit line build-outs. 00 = 0 dB, 01 = 7.5 dB, 10 = 15 dB, and 11 = 22.5 dB.
26	$\overline{CS}$	I	Chip Select *(Host Mode)*	This input is used to access the serial interface in the Host mode. For each read or write operation, $\overline{CS}$ must transition from high to low, and remain low.
	RLOOP	I	Remote Loopback *(H/W Mode)*	This input controls loopback in the Hardware mode. Setting RLOOP to a logic 1 enables Remote Loopback. During Remote Loopback, in-line encoders and decoders are bypassed. Setting both RLOOP and LLOOP while holding TAOS low causes a Reset. Setting both RLOOP and LLOOP with TAOS high (or tying RCLK to RLOOP) enables Network Loopback detection.
27	SCLK	I	Serial Clock *(Host Mode)*	This clock is used in the Host mode to write data to or read data from the serial interface registers.
	LLOOP	I	Local Loopback *(H/W Mode)*	This input controls loopback functions in the Hardware mode. Setting LLOOP to a logic 1 enables the Local Loopback Mode. Setting both LLOOP and RLOOP while holding TAOS low causes a Reset.
28	CLKE	I	Clock Edge *(Host Mode)*	Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	I	Transmit All Ones *(H/W Mode)*	When set to a logic 1 in the Hardware mode, TAOS causes the LXT310 to transmit a stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback. Setting TAOS, LLOOP and RLOOP simultaneously enables Network Loopback detection.

Functional Description

The LXT310 is a fully integrated PCM transceiver for 1.544 MHz (T1) applications. It allows full-duplex transmission of digital data over existing twisted-pair installations.

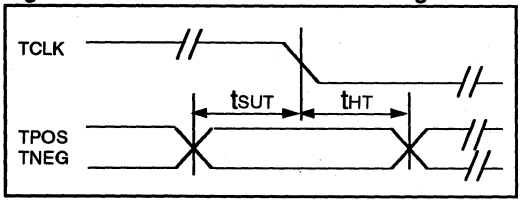
The LXT310 interfaces with two twisted-pair lines (one pair for transmit, one pair for receive) through standard pulse transformers and appropriate resistors.

Figure 1 is a block diagram of the LXT310. The transceiver may be controlled by a microprocessor through the serial port (Host Mode), or by individual pin settings (Hardware Mode). The jitter attenuator may be positioned in either the transmit or receive path.

Transmitter

Input data (bipolar or unipolar) for transmission onto the line is clocked serially into the device. Bipolar data is input at pin 3 (TPOS) and pin 4 (TNEG). Unipolar data is input at pin 3 (TDATA) only. (Unipolar mode is enabled by holding pin 4 high for 16 RCLK cycles). Input data may be passed through the Jitter Attenuator and/or B8ZS encoder, if selected. In Host mode, B8ZS is selected by setting bit D3 of the input data byte. In Hardware mode, B8ZS is selected by connecting the MODE pin to RCLK. Input synchronization is supplied by the transmit clock (TCLK). Timing requirements for TCLK and the Master Clock (MCLK) are defined in Table 2 and Figure 2.

Figure 2: LXT310 Transmit Clock Timing



Idle Mode

The LXT310 incorporates a transmit idle mode. This allows multiple transceivers to be connected to a single line for redundant applications. TTIP and TRING remain in a high impedance state when TCLK is not present (TCLK grounded). The high impedance state can be temporarily disabled by enabling either TAOS, Remote Loopback or Network Loopback.

The transmitted pulse shape is determined by Line Build Out (LBO) inputs LBO1 and LBO2 as follows:

Line Build-Out (dB)	0	7.5	15	22.5
LBO1	0	1	0	1
LBO2	0	0	1	1

LBO settings are input through the serial port in the Host mode. In the Hardware mode, LBO inputs are applied through individual pins. Shaped pulses meeting the various T1 CSU and ISDN PRI requirements are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Refer to Table 3 and Figure 3 for T1 pulse mask specifications.

Table 2: LXT310 Master Clock and Transmit Timing Characteristics (See Figure 2)

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
Master clock frequency	MCLK	-	1.544	-	MHz	
Master clock tolerance	MCLKt	-	±100	-	ppm	
Master clock duty cycle	MCLKd	40	-	60	%	
Crystal frequency	fc	-	6.176	-	MHz	LXT310 only
Transmit clock frequency	TCLK	-	1.544	-	MHz	
Transmit clock tolerance	TCLKt	-	-	±100	ppm	
Transmit clock duty cycle	TCLKd	10	-	90	%	
TPOS/TNEG to TCLK setup time	t_{SUT}	50	-	-	ns	
TCLK to TPOS/TNEG Hold time	t_{HT}	50	-	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Short Circuit Limit

The LXT310 transmitter is equipped with a short-circuit limiter. This feature limits to approximately 120 mA RMS the current the transmitter will source into a low-impedance load. The limiter trips when the RMS current exceeds the limit for 100 µs (~ 150 marks). It automatically resets when the load current drops below the limit.

The LXT310 meets or exceeds FCC and AT&T specifications for CSU and NI applications, as well as ANSI T1E1, and CCITT requirements for ISDN PRI.

Line Code

The LXT310 transmits data as a 50% AMI line code as shown in Figure 4. Power consumption is reduced by activating the AMI line driver only to transmit a mark. The output driver is disabled during transmission of a space. Biasing of the transmit DC level is on-chip.

Receiver

The twisted-pair input is received via a 1:1 transformer. Recovered data is output at RPOS/RNEG (RDATA in unipolar mode), and the recovered clock is output at RCLK. Refer to Table 4 and Figure 5 for receiver timing.

2

Figure 3: 1.544 MHz T1 Pulse Mask

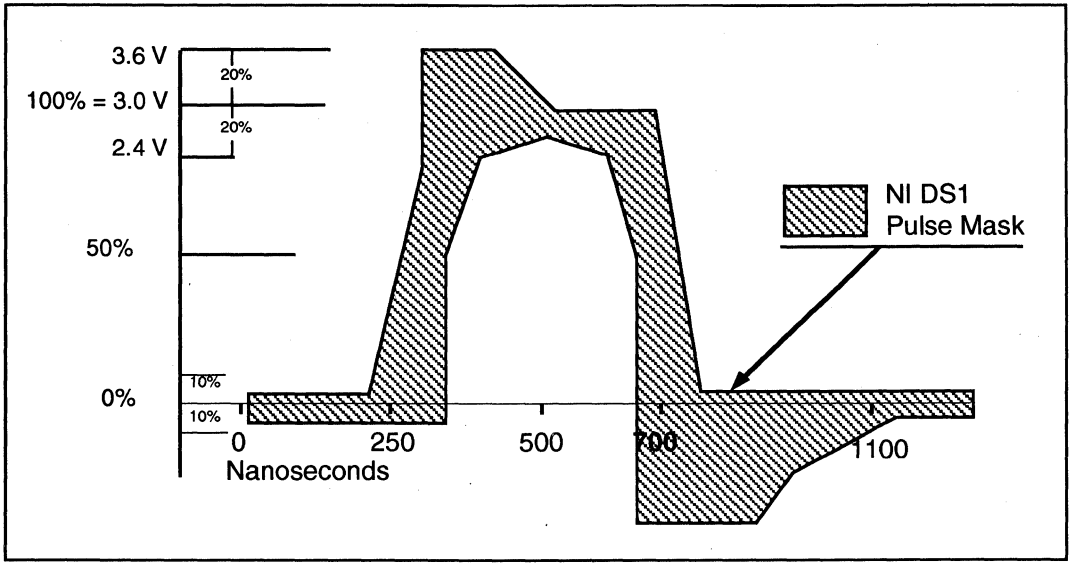
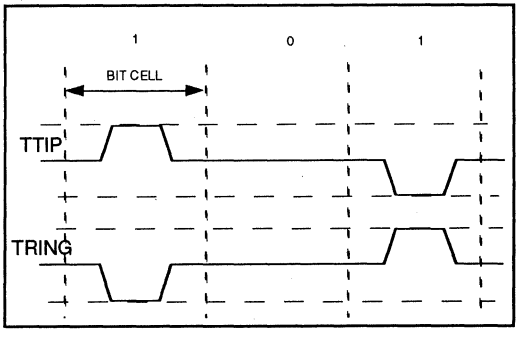


Table 3: Pulse Mask Corner Point Specifications

Maximum Curve		Minimum Curve	
Time (ns)	% V	Time (ns)	% V
0	5	0	-5
250	5	350	-5
325	80	350	50
325	120	400	90
425	120	500	95
500	105	600	90
675	105	650	50
725	5	650	-45
1100	5	800	-45
1250	5	896	-26
		1100	-5
		1250	-5

Figure 4: 50% AMI Coding Diagram



The signal received at RPOS and RNEG is processed through the receive equalizer. The Equalizer Gain Limit (EGL) input determines the maximum gain that may be applied at the equalizer. When set to 0, up to 36 dB of gain may be applied.

When EGL = 1, gain is limited to no more than 26 dB providing for increased noise margin in shorter loop operation. Insertion loss of the line in 7.5 dB steps, as indicated by the receive equalizer setting, is encoded in the LATN output as shown in Figure 6.

Table 4: LXT310 Receive Timing Characteristics (See Figure 5)

Parameter	Sym	Min	Typ[1]	Max	Units
Receive clock duty cycle [2]	RCLKd	40	50	60	%
Receive clock pulse width [2]	t_{PW}	600	648	700	ns
Receive clock pulse width high	t_{PWH}	-	324	-	ns
Receive clock pulse width low	t_{PWL}	303	324	345	ns
RPOS / RNEG to RCLK rising setup time	t_{SUR}	-	274	-	ns
RCLK rising to RPOS /RNEG hold time	t_{HR}	-	274	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
[2] RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz.)

Figure 5: LXT310 Receive Clock Timing

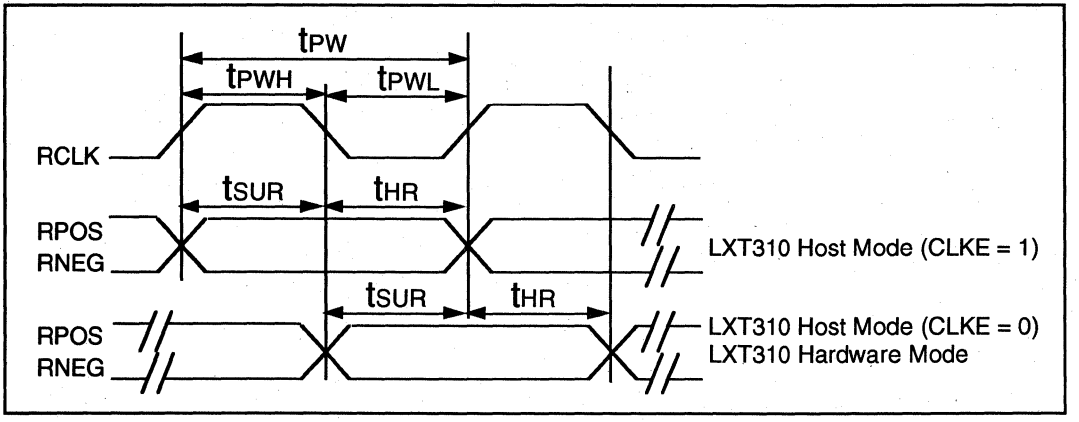
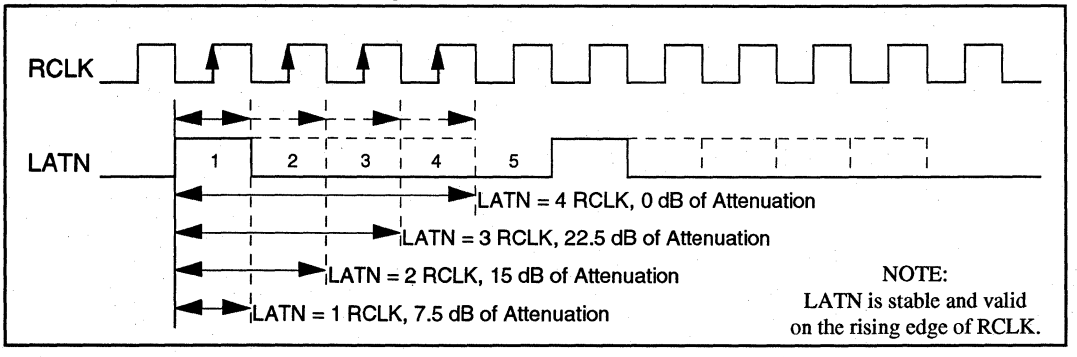


Figure 6: LATN Pulse Width Encoding



The equalized signal is filtered and applied to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. The threshold is set to 50% of the peak value. The receiver is capable of accurately recovering signals with up to 36 dB of cable attenuation (from 2.4 V).

After processing through the data slicers, the received signal is routed to the data and timing recovery section, then to the B8ZS decoder (if selected) and to the LOS processor. The LOS Processor loads a digital counter at the RCLK frequency. The count is incremented each time a zero (space) is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and a smooth transition replaces the RCLK output with the MCLK. (*During LOS if MCLK is not supplied and JASEL = 1, the RCLK output is replaced with the centered crystal clock.*)

Received marks will be output regardless of the LOS status, but the LOS pin will not reset until the ones density reaches 12.5 %. This level is based on receipt of at least 4 ones in any 32 bit periods.

Jitter Attenuation

Jitter attenuation is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 5 for crystal specifications. The ES is a 32 x 2-bit register. When JASEL = 1, the JAL is positioned in the receive path. When JASEL = 0, the JAL is positioned in the transmit path.

Data (TPOS/TNEG / TDATA or RPOS/RNEG / RDATA) is clocked into the ES with the associated clock signal (TCLK or RCLK), and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the associated path.

Operating Modes

The LXT310 can be controlled by a microprocessor through a serial interface (Host mode), or through individual pins, (Hardware mode). The mode of operation is set by the MODE pin logic level.

Host Mode Operation

The LXT310 operates in the Host mode when MODE is set to 1. The 16-bit serial word consists of an 8-bit Command/ Address byte and an 8-bit Data byte. Table 6 lists the output data bit combinations. Figure 7 shows the serial interface data structure and timing. The Host mode provides a latched Interrupt output (INT) which is triggered by a change in the LOS or NLOOP bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor writes a one to the respective bit in the serial input data byte.

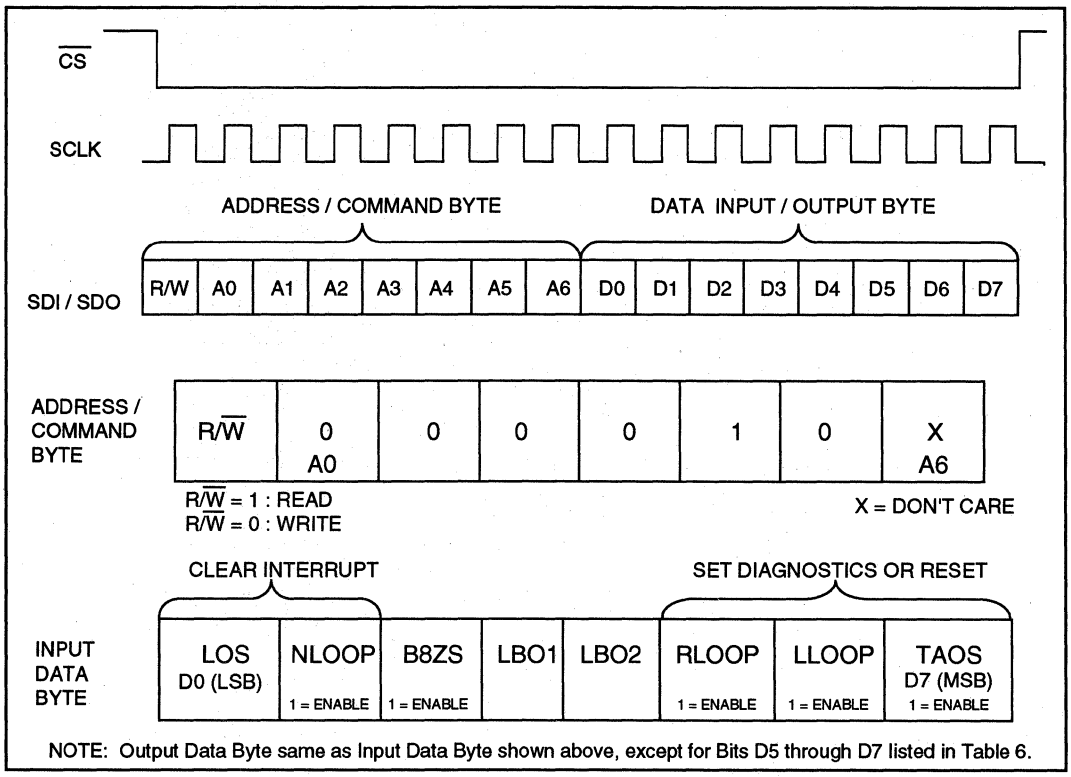
Table 5: LXT310 Crystal Specifications (External)

Parameter	Specification
Frequency	6.176 MHz
Frequency Stability	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)
Pullability	CL = 11.7 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm
Effective series resistance	40 Ω Maximum
Crystal cut	AT
Resonance	Parallel
Maximum drive level	2.0 mW
Mode of operation	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical

Table 6: LXT310 Serial Data Output Bit Coding (See Figure 7)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	LLOOP active
0	1	1	TAOS and LLOOP active
1	0	0	RLOOP active
1	0	1	NLOOP has changed state since last Clear NLOOP occurred.
1	1	0	LOS has changed state since last Clear LOS occurred.
1	1	1	LOS and NLOOP have both changed state since last Clear NLOOP and Clear LOS.

Figure 7: LXT310 Serial Interface Data Structure



NOTE: Output Data Byte same as Input Data Byte shown above, except for Bits D5 through D7 listed in Table 6.

Host mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as listed in Table 7.

Table 7: CLKE Settings

Output	Clock	CLKE = 0	CLKE = 1
RPOS/RNEG	RCLK	Rising Edge	Falling Edge
SDO	SCLK	Falling Edge	Rising Edge

The LXT310 serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The LXT310 contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select (CS) input to transition from high to low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Serial data I/O timing characteristics are shown in Table 8, and Figures 8 and 9.

Hardware Mode Operation

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the INT and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS/RNEG or RDATA outputs are valid on the rising edge of RCLK. The LXT310 operates in Hardware mode only when MODE is set to 0 or connected to RCLK.

Initialization and Reset Operation

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. The crystal oscillator provides the receiver reference. If the crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing ones to RLOOP and LLOOP, and a zero to TAOS. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns while holding TAOS low. In either mode, reset clears and sets all registers to 0.

Diagnostic Mode Operation

In Transmit All Ones (TAOS) mode, the TPOS and TNEG inputs to the transceiver are ignored and the transceiver transmits a continuous stream of 1's at the TCLK frequency. (If TCLK is not provided, TAOS is locked to the MCLK.) This can be used as the Blue Alarm Indicator (AIS). In Host mode, TAOS is commanded by writing a one to bit D7 of the input data byte. In Hardware mode, TAOS is commanded by setting pin 28 high. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

Local Loopback (LLOOP) is designed to exercise the maximum number of functional blocks. During LLOOP operation, the RTIP/RRING inputs from the line are disconnected. Instead, the transmit outputs are routed back into the receive inputs. This tests the encoders/decoders, jitter attenuator, transmitter, receiver and timing recovery sections. In Host mode, Local Loopback is commanded by writing a one to bit D6 of the input data byte. In Hardware mode, Local Loopback is commanded by setting pin 27 high. If TAOS and LLOOP are both set, the All Ones pattern is transmitted onto the line while the TPOS/TNEG input data is looped back to the RPOS/RNEG outputs.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TCLK and TPOS/TNEG or TDATA) are ignored, and the in-line encoders and decoders are bypassed. The RPOS/RNEG or RDATA outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line. In Host mode, Remote Loopback is commanded by writing a one to bit D5 of the input data byte. In Hardware mode, Remote Loopback is commanded by setting pin 26 high.

Network Loopback can be commanded from the network when the Network Loopback detect function is enabled. In Host mode, Network Loopback (NLOOP) detection is enabled by simultaneously writing ones to RLOOP, LLOOP and TAOS, then writing zeros in the next cycle. In Hardware mode, Network Loopback detection is enabled by holding RLOOP, LLOOP and TAOS high simultaneously for 200 ns then bringing them to logic 0, or by tying RCLK to RLOOP. NLOOP detection may be disabled by resetting the chip.

When NLOOP detection is enabled, the receiver monitors the input data stream for the NLOOP data patterns (00001 = enable, 001 = disable). When an NLOOP enable data pattern is repeated for a minimum of five seconds (with 10^{-3} BER), the device begins remote loopback operation. The LXT310 responds to both framed and unframed NLOOP patterns. Once remote network loopback detection is enabled at the chip and activated by the correct data pattern, it is identical to remote loopback initiated at the chip. NLOOP is reset by receiving the disable pattern for 5 seconds, or by activation of RLOOP. NLOOP is temporarily interrupted by LLOOP, but the NLOOP state is not reset.

Table 9: LXT310 Serial I/O Timing Characteristics (See Figures 9 and 10)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	-	-	100	ns	Load 1.6 mA, 50pF
SDI to SCLK setup time	t_{DC}	50	-	-	ns	
SCLK to SDI hold time	t_{CDH}	50	-	-	ns	
SCLK low time	t_{CL}	240	-	-	ns	
SCLK high time	t_{CH}	240	-	-	ns	
SCLK rise and fall time	t_R, t_F	-	-	50	ns	
CS to SCLK setup time	t_{CC}	50	-	-	ns	
SCLK to CS hold time	t_{CCH}	50	-	-	ns	
CS inactive time	t_{CWH}	250	-	-	ns	
SCLK to SDO valid	t_{CDV}	-	-	200	ns	
SCLK falling edge or CS rising edge to SDO high Z	t_{CDZ}	-	100	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 8: LXT310 Serial Data Input Timing Diagram

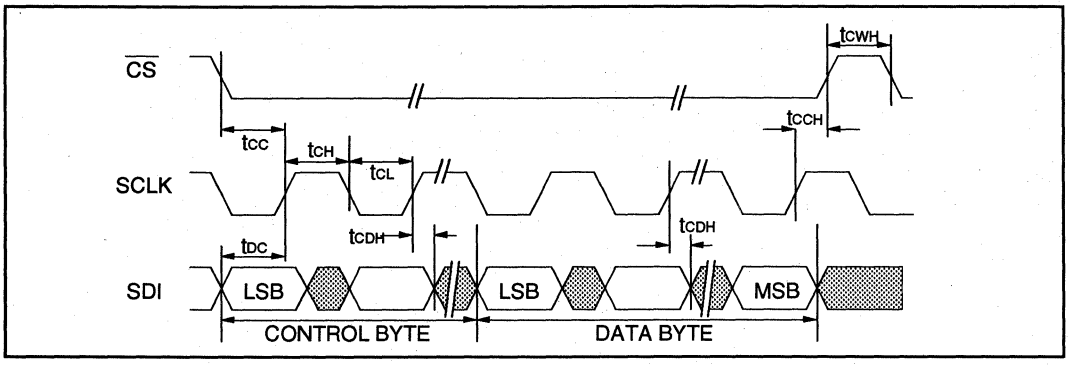
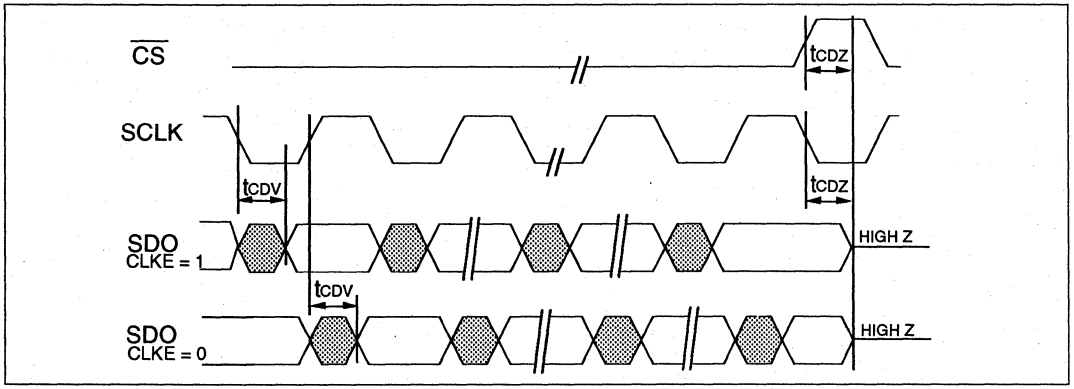


Figure 9: LXT310 Serial Data Output Timing Diagram



Application Considerations

LATN Decoding Circuits and External Components

To conserve pins, the line attenuation output is encoded as a simple serial bit stream. Table 9 provides the decoded output for each equalizer setting. Figure 10 is a typical decoding circuit for the LATN output. It uses a 2-bit synchronous counter (half of a 4-bit counter) with synchronous reset, and a pair of flip-flops. Table 10 lists approved crystals and transformers.

Power Requirements

The LXT310 is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3V of each other, and decoupled to their respective grounds separately, as shown in Figure 11. Isolation between the transmit and receive circuits is provided internally.

2

Table 9: LATN Output Coding

L1	L2	Line Attenuation
0	0	0.0 dB
0	1	-7.5 dB
1	0	-15.0 dB
1	1	-22.5 dB

Figure 10: Typical LATN Decoding Circuit

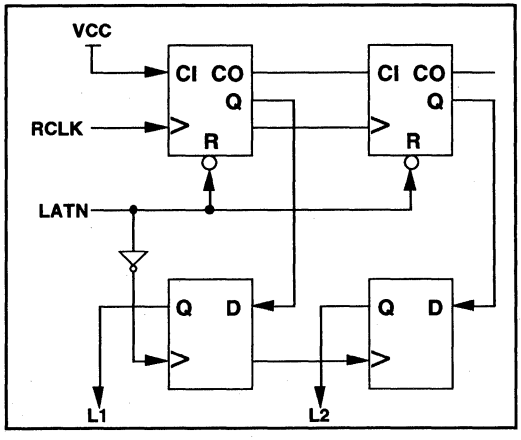


Table 10: Approved Crystals and Transformers

Component	Manufacturer	Part Numbers
Crystal (6.176 MHz)	M-Tron	MP-1 3808-010 / 4144-002
	Monitor Products	MSC1311-01B
	CTS Knights	6176-180
	Valpey Fisher	VF49A16FN1
	U .S. Crystal	U18-18-6176SP
Tx Transformer (1 : 2)	Bell Fuse	0553-5006-IC
	FEE Fil-Mag	66Z1308
	Midcom	671-5832
	Pulse Engineering	65351, 65771
	Schott Corp	67127370 and 67130850
	HALO	TD61-1205G and TD67-1205G (combo Tx/Rx)
Rx Transformer (1 : 1)	FEE Fil-Mag	FE 8006-155
	Midcom	671-5792
	Pulse Engineering	64936 and 65778
	Schott Corp	67130840 and 67109510
	HALO	TD61-1205G and TD67-1205G (combo Tx/Rx)

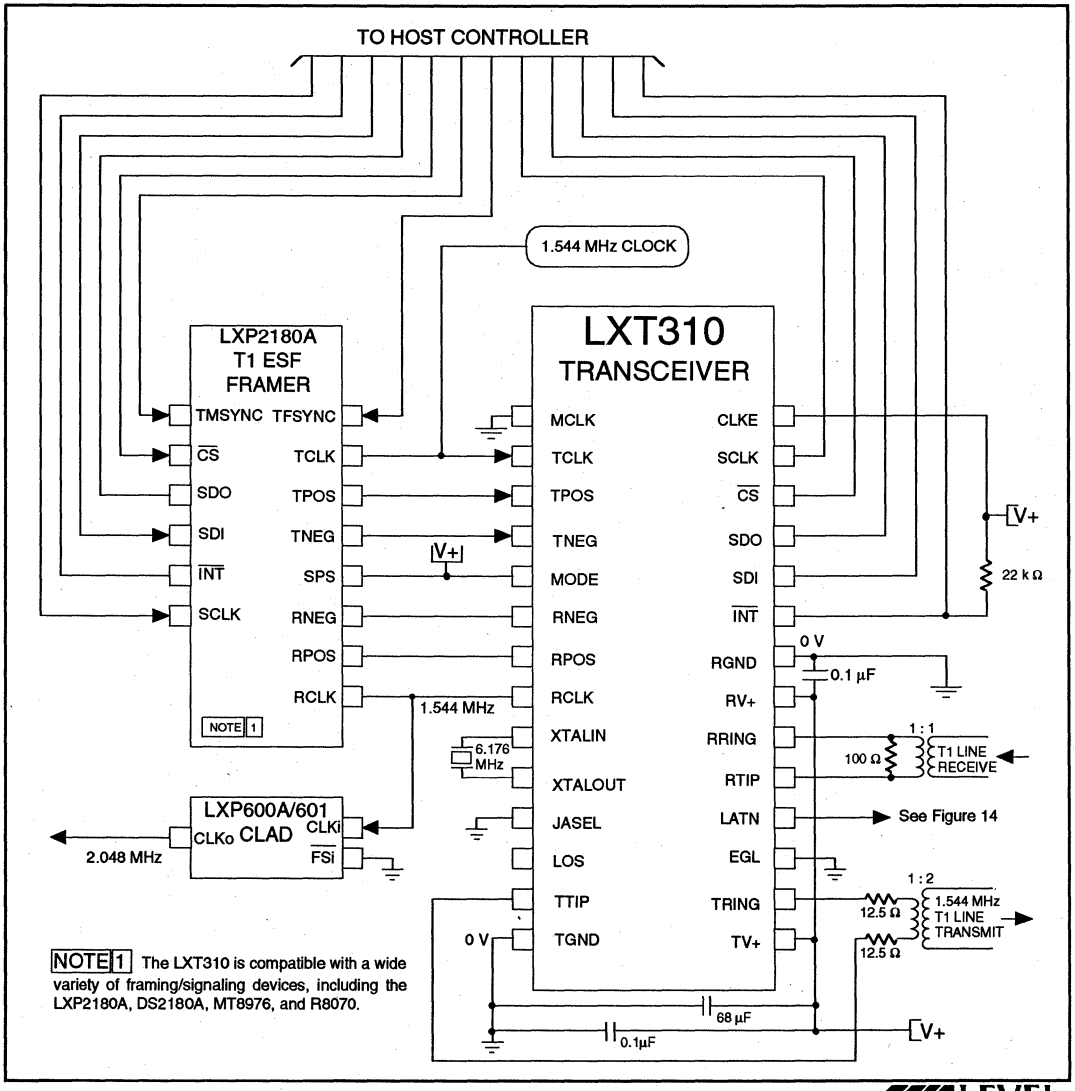
Host Mode Applications

Figure 11 shows a typical T1 CSU application with the LXT310 operating in the Host mode (MODE pin tied high). The LXP2180A T1/ESF Framer provides the digital interface with the host controller. Both devices are controlled through the serial interface. In the Host mode, the LOS alarm is reported via the serial port so the LOS pin is allowed to float.

An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The 6.176 MHz crystal across XTALIN and XTALOUT enables the JAL which is switched to the transmit side by the ground on JASEL. (Refer to Table 10 for approved crystals and transformers.) The power supply inputs are tied to a common bus with appropriate decoupling capacitors (68µF and 0.1 µF) installed on each side.

The twisted-pair interfaces are relatively simple. A 100 Ω resistor across the input of a 1:1 transformer is used on the receive side, and a pair of 12.5 Ω resistors are installed in line with the 1:2 output transformer.

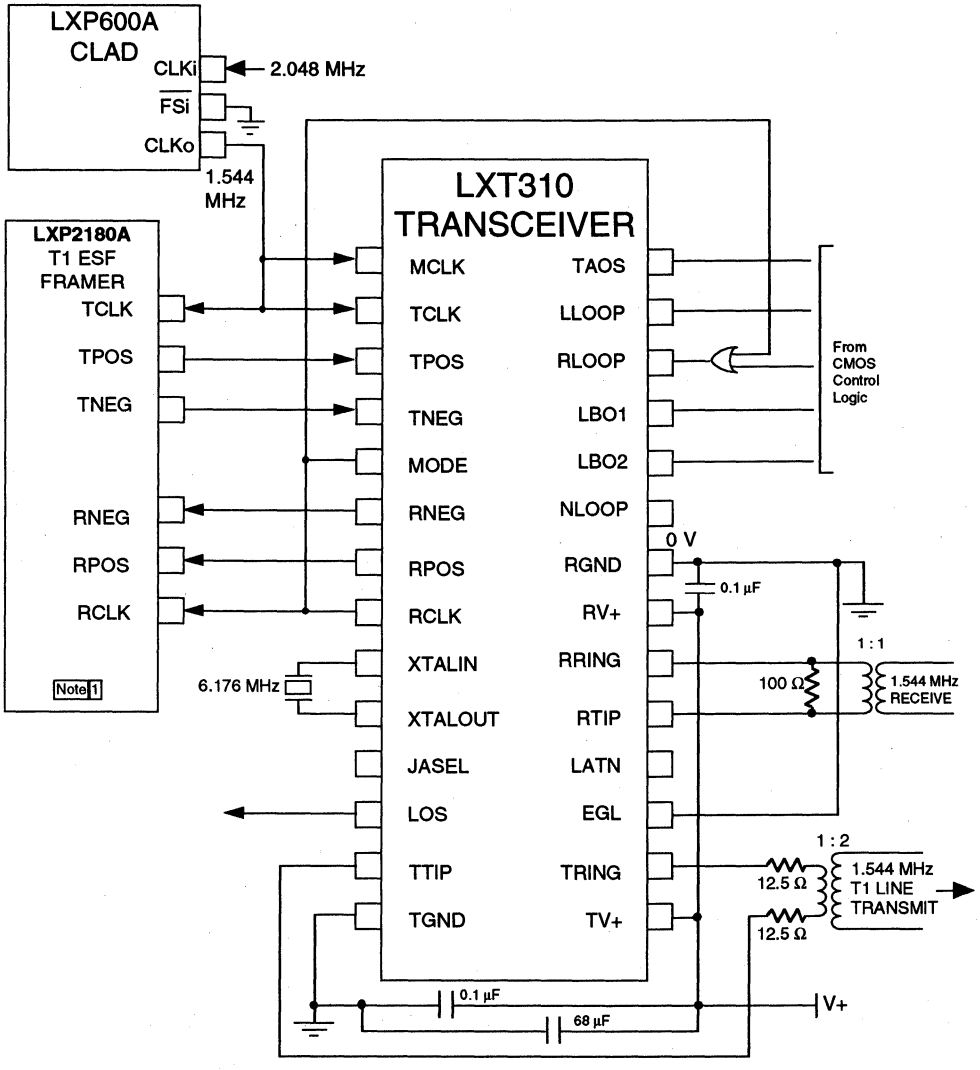
Figure 11: Typical LXT310 Host Mode T1/CSU Application



LXT310 Hardware Mode Applications

Figure 12 is a typical 1.544 MHz ISDN PRI application with the LXT310, LXP2180A framer and an LXP600A clock adapter. The LXT310 is operating in the Hardware mode with B8ZS encoding enabled (MODE pin 5 tied to RCLK). As in the T1 CSU application, Figure 11, this configuration is illustrated with a single power supply bus. CMOS control logic is used to set both LBO pins high, selecting the 22.5 dB LBO, and the EGL pin is tied low, allowing for full receiver gain. The TAOS, LLOOP and RLOOP diagnostic modes are individually controllable. The RCLK input to the OR gate at RLOOP allows for clocking of the RLOOP pin, which enables network loopback detection. The receive and transmit line interfaces are identical to the Host mode application shown in Figure 11.

Figure 12: Typical LXT310 Hardware Mode Application



NOTE 1 In addition to the LXP2180A, the LXT310 is compatible with a wide variey of framing/signaling devices, including the DS2180A, MT8976 and R8070.

NOTES:

LXT318
E1 NTU / ISDN PRI Transceiver

General Description

The LXT318 is the first fully integrated transceiver for E1 Network Termination Unit (NTU) and ISDN Primary Rate Interface (ISDN PRI) applications at 2.048 MHz. The transceiver operates from 0.0 km to 2.6 km of 0.6 mm (22 AWG) twisted-pair cable without any external components.

The LXT318 offers selectable HDB3 encoding/decoding, and unipolar or bipolar data I/O. The LXT318 also provides jitter attenuation in either the transmit or receive direction starting at 6 Hz, and incorporates a serial interface (SIO) for microprocessor control.

The LXT318 offers a variety of diagnostic features including loopbacks and loss of signal monitoring. It is built using an advanced double-poly, double-metal CMOS process and require only a single 5-volt power supply.

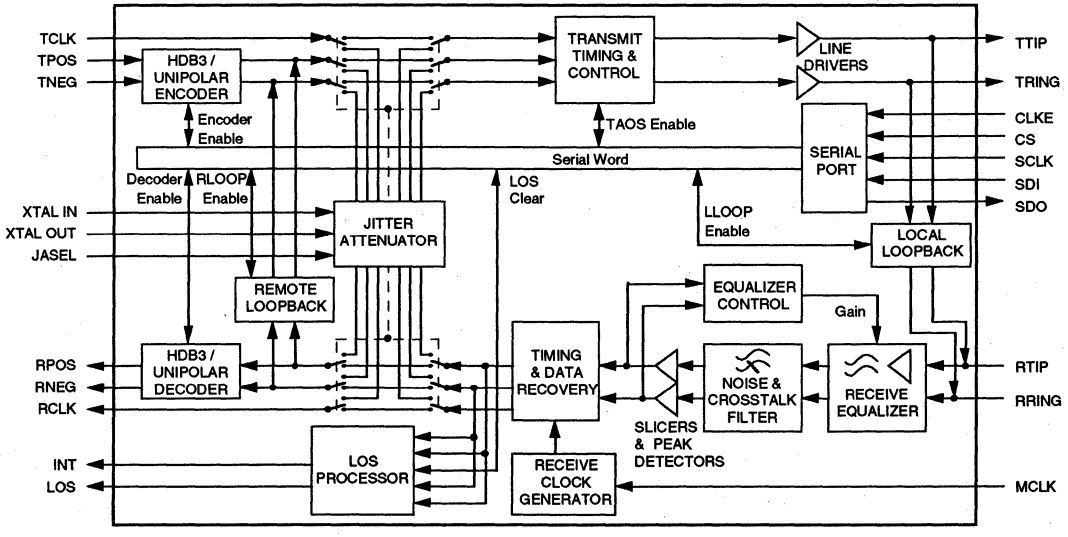
Applications

- PCM 30 / ISDN PRI Interface (CCITT G.703, I.431)
- NTU (interface to E1 Service)
- E1 Mux or LAN bridge
- CPU to CPU Channel Extenders
- Digital Loop Carrier - Subscriber Carrier Systems
- Channel Banks

Features

- Fully integrated transceiver comprising: on-chip equalizer; timing recovery/control; data processor; receiver; transmitter and digital control
- Pin compatible with the LXT310 T1 CSU/ISDN PRI (1.544 MHz) Transceiver
- Meets or exceeds CCITT specifications including G.703, G.736, I.431 and G.823 for E1 short haul (6 dB) or long haul (43 dB) applications
- Fully restores the received signal after transmission through a cable with attenuation of 43 dB @1024 kHz
- Selectable Unipolar or Bipolar data I/O
- Selectable HDB3 encoding/decoding
- Output short circuit current limit protection
- On-line idle mode for testing or for redundant systems
- Local and remote loopback functions
- Receive monitor with Loss of Signal (LOS) output
- Jitter attenuation starting at 6 Hz, switchable to transmit or receive path
- Microprocessor controllable
- Available in 28-pin DIP and PLCC (extended temp)

Figure 1: LXT318 Block Diagram



Absolute Maximum Ratings				
Parameter	**Sym**	**Min**	**Max**	**Units**
DC supply (referenced to GND)	RV+, TV+	–	6.0	V
Input voltage, any pin	V_{IN}	RGND - 0.3	RV+ + 0.3	V
Input current, any pin [1]	I_{IN}	-10	10	mA
Ambient operating temperature	T_A	-40	85	°C
Storage temperature	T_{STG}	-65	150	°C

WARNING: Operations at or beyond these limits may permanently damage the device. Normal operation not guaranteed at these extremes.
[1] Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+ and TGND can withstand continuous current of 100mA.

Operating Conditions/Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
DC supply [2]	RV+, TV+	4.75	5.0	5.25	V	
Ambient operating temperature	T_A	-40	–	+85	°C	
Power dissipation [3]	P_D	–	300	400	mW	100% ones density & maximum line length @ 5.25 V

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
[2] TV+ must not differ from RV+ by more than 0.3 V.
[3] Power dissipation while driving 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

Digital Characteristics (T_A = -40° to 85°C, V+ = 5.0 V ±5%, GND = 0 V)

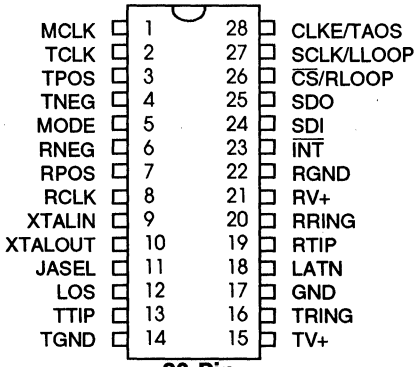
Parameter	Sym	Min	Typ	Max	Units	Test Conditions
High level input voltage [1,2] (pins 1-5, 10, 23-28)	V_{IH}	2.0	–	–	V	
Low level input voltage [1,2] (pins 1-5, 10, 23-28)	V_{IL}	–	–	0.8	V	
High level output voltage [1,2] (pins 6-8, 12, 23, 25)	V_{OH}	2.4	–	–	V	I_{OUT}=- 400 µA
Low level output voltage [1,2] (pins 6-8, 12, 23, 25)	V_{OL}	–	–	0.4	V	I_{OUT}=1.6mA
Input leakage current	I_{LL}	0	–	± 10	µA	
Three-state leakage current [1] (pin 25)	I_{3L}	0	–	± 10	µA	

[1] Functionality of pins 23 and 25 depends on mode. See Host / Hardware Mode descriptions.
[2] Output drivers will output CMOS logic levels into CMOS loads.

Analog Characteristics (T_A = -40° to 85°C, V+ = 5.0 V ±5%, GND = 0 V)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
Recommended output load at TTIP and TRING		50	120	200	Ω	
AMI Output Pulse Amplitudes		2.7	3.0	3.3	V	measured at the
Jitter added by the transmitter [2]	20Hz - 100kHz [3]	–	–	0.05	UI	output
Input jitter tolerance	20 kHz - 100 kHz	0.2	0.3	–	UI	0 - 43 dB line
	10 Hz	100	500	–	UI	
Jitter attenuation curve corner frequency [4]		–	6	–	Hz	
Receive signal attenuation range @ 1024 kHz		0	43	–	dB	
Allowable consecutive zeros before LOS		160	175	190	–	
Minimum Return Loss [9,10]		Transmit Min Typ		Receive Min Typ		
	51 kHz - 102 kHz	TBD TBD		12 TBD	dB	
	102 kHz - 2.048 MHz	TBD TBD		18 TBD	dB	
	2.048 MHz - 3.072 MHz	TBD TBD		14 TBD	dB	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
[2] Input signal to TCLK is jitter-free.
[3] Guaranteed by characterization; not subject to production testing.
[4] Circuit attenuates jitter at 20 dB/decade above the corner frequency.



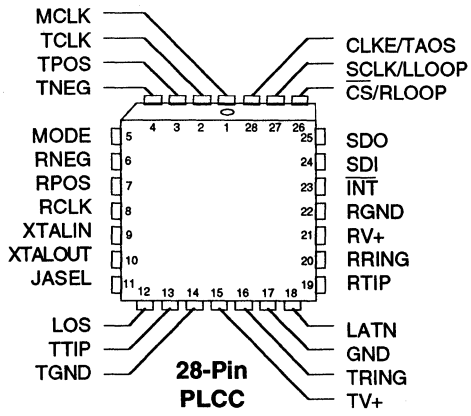


Table 1: Pin Descriptions

Pin #	Sym	I/O	Name	Description
1	MCLK	I	Master Clock	A 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
2	TCLK	I	Transmit Clock	Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK.
3	TPOS/ TDATA	I	Transmit Data Input	Input for data to be transmitted on the twisted-pair line. Normally, pin 3 is TPOS and pin 4 is TNEG, the positive and negative sides of a bipolar input pair. However, when pin 4 is held high for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), the LXT318 switches to a unipolar mode. Unipolar mode pin functions are listed in Table 2.
4	TNEG/ UBS	I	Data Input/ Polarity Select	
5	MODE	I	Mode Select	Setting MODE to logic 1 puts the LXT318 in the Host mode. In the Host mode, the serial interface is used to control the LXT318 and determine its status. Setting MODE to logic 0 puts the LXT318 in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status. Tying MODE to RCLK activates the Hardware mode and enables the HDB3 encoder/ decoder.
6	RNEG/ BPV	O	Receive Negative Data	Bipolar data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). In Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In Hardware mode both outputs are stable and valid on the rising edge of RCLK. In Unipolar mode, pin 6 output is a Bipolar Violation indication and pin 7 is the unipolar data output. See Table 2 for Unipolar mode functions.
7	RPOS/ RDATA	O	Receive Positive Data	
8	RCLK	O	Receive Clock	This is the clock recovered from the signal received at RTIP and RRING.

Table 1: Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
9	XTALIN	I	Crystal Input	An external crystal (18.7 pF load capacitance, pullable) operating at four times the bit rate (8.192 MHz) is required to enable the jitter attenuation function of the LXT318. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
10	XTALOUT	O	Crystal Output	
11	JASEL	I	Jitter Attenuation Select	Selects jitter attenuation location. When JASEL = 1, the jitter attenuator is active in the receive path. When JASEL = 0, the jitter attenuator is active in the transmit path.
12	LOS	O	Loss Of Signal	LOS goes to logic 1 after 175 consecutive spaces and returns to logic 0 when the received signal reaches 12.5% mark density (minimum of four marks within 32 bit periods, with no more than 15 consecutive zeros.) Received marks are output on RPOS and RNEG even when LOS is at a logic 1.
13	TTIP	O	Transmit Tip	Differential Driver Outputs. These outputs are designed to drive a 50 - 200 Ω load. Line matching resistors and transformer can be selected to give the desired pulse height.
16	TRING	O	Transmit Ring	
14	TGND	-	Tx Ground	Ground return for the transmit drivers power supply TV+.
15	TV+	I	Transmit Power Supply	+5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ± 0.3V.
17	GND	–	Ground	This pin must be tied to ground.
18	LATN	O	Line Attenuation Indication	Encoded output. Pulse width, relative to RCLK, indicates receive equalizer gain setting (line insertion loss at 1024 kHz) in 9.5 dB steps. When LATN = 1 RCLK pulse, the equalizer is set at 9.5 dB gain; 2 pulses = 19 dB; 3 pulses = 28.5 dB and 4 pulses = 0 dB. Output is valid on the rising edge of RCLK.
19	RTIP	I	Receive Tip	The AMI signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
20	RRING	I	Receive Ring	
21	RV+	I	Receive Power Supply	+5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	–	Rx Ground	Ground return for power supply RV+.
23	$\overline{INT}$	O	Interrupt *(Host Mode)*	In Host mode, this pin goes low to flag the host processor when LOS changes state. $\overline{INT}$ is an open drain output and should be tied to power supply RV+ through a resistor. Reset $\overline{INT}$ by clearing the LOS register bit.
	GND	–	Ground *(H/W Mode)*	In Hardware mode, this pin is inactive and should be tied to ground.
24	SDI	I	Serial Data In *(Host Mode)*	The serial data input stream is applied to this pin when the LXT318 operates in the Host mode. SDI is sampled on the rising edge of SCLK.
	GND	–	Ground *(H/W Mode)*	This pin is inactive in the Hardware mode and should be tied to ground.

Table 1: Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
25	SDO	O	Serial Data Out *(Host Mode)*	In the Host mode, serial data from the on-chip register is output on this pin. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. SDO goes to a high-impedance state when the serial port is being written to.
	GND	–	Ground *(H/W Mode)*	This pin is inactive in the Hardware mode and should be tied to ground.
26	$\overline{CS}$	I	Chip Select *(Host Mode)*	In the Host mode, this input is used to access the serial interface. For each read or write operation, $\overline{CS}$ must transition from high to low, and remain low.
	RLOOP	I	Remote Loopback *(H/W Mode)*	In the Hardware mode, this input controls remote loopback. Setting RLOOP to a logic 1 enables Remote Loopback. During Remote Loopback, in-line encoders and decoders are bypassed. Setting both RLOOP and LLOOP while holding TAOS low causes a Reset.
27	SCLK	I	Serial Clock *(Host Mode)*	In the Host mode, this clock is used to write data to or read data from the serial interface registers.
	LLOOP	I	Local Loopback *(H/W Mode)*	In the Hardware mode, this input controls local loopback. Setting LLOOP to a logic 1 enables the Local Loopback Mode. Setting both LLOOP and RLOOP while holding TAOS low causes a Reset.
28	CLKE	I	Clock Edge *(Host Mode)*	In the Host mode, this pin controls transitions of the data outputs. Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	I	Transmit All Ones *(H/W Mode)*	In the Hardware mode, this pin controls the TAOS function. When set to a logic 1, TAOS causes the LXT318 to transmit a stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

Table 2: Unipolar Data I/O Pin Descriptions

Pin #	Sym	I/O	Name	Description
3	TDATA	I	Transmit Data	Unipolar input for data to be transmitted on the twisted-pair line.
4	UBS	I	Uni-Bi Polarity Select	When pin 4 is held high for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), the LXT318 switches to unipolar data I/O. The device immediately returns to bipolar I/O when pin 4 goes low.
6	BPV	O	Bipolar Violation	Pin 6 goes high when a bipolar violation is received.
7	RDATA	O	Receive Data	Unipolar data output. RDATA is a Non-Return-to-Zero (NRZ) output. In Host mode, CLKE determines the clock edge at which RDATA is stable and valid. In Hardware mode RDATA is stable and valid on the rising edge of RCLK.

Note: Table 2 lists only those pins which are affected by the switch to unipolar data I/O.

Functional Description

The LXT318 is a fully integrated PCM transceiver for 2.048 MHz (E1) applications. It allows full-duplex transmission of digital data over existing twisted-pair installations.

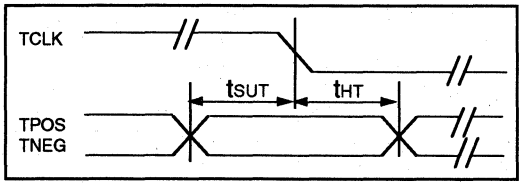
The LXT318 transceiver interfaces with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

Figure 1 is a block diagram of the LXT318. This transceiver may be controlled by a microprocessor through the serial port (Host Mode), or by individual pin settings (Hardware Mode). The jitter attenuator may be positioned in either the transmit or receive path, as determined by pin 11 (JASEL).

Transmitter

Input data (bipolar or unipolar) for transmission onto the line is clocked serially into the LXT318. Bipolar data is input at pin 3 (TPOS) and pin 4 (TNEG). Unipolar data is input at pin 3 (TDATA) only. (Unipolar mode is enabled by holding pin 4 high for 16 RCLK cycles). Input data may be passed through the Jitter Attenuator and/or HDB3 encoder, if selected. In Host mode, HDB3 is selected by setting bit D3 of the input data byte. In Hardware mode, HDB3 is selected by connecting the MODE pin to RCLK. Input synchronization is supplied by the transmit clock (TCLK). Timing requirements for TCLK and the Master Clock (MCLK) are defined in Figure 2 and Table 3.

Figure 2: LXT318 Transmit Clock Timing



Line Code

The LXT318 transmits data as a 50% AMI line code as shown in Figure 3. Biasing of the transmit DC level is on-chip. Shaped pulses meeting the various CCITT requirements are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Refer to Figure 4 for E1 pulse mask specifications.

Idle Mode

The LXT318 incorporates a transmit idle mode. This allows multiple transceivers to be connected to a single line for redundant applications or for testing purposes. TTIP and TRING remain in a high impedance state when TCLK is not present (TCLK grounded). The high impedance state can be temporarily disabled by enabling Remote Loopback.

Figure 3: 50% AMI Coding Diagram

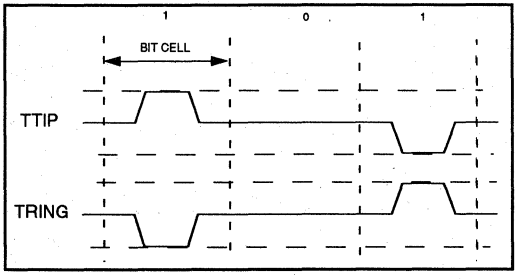


Table 3: LXT318 Master Clock and Transmit Timing Characteristics (See Figure 2)

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
Master clock frequency	MCLK	-	2.048	-	MHz	
Master clock tolerance	MCLKt	-	±100	-	ppm	
Master clock duty cycle	MCLKd	40	-	60	%	
Crystal frequency	fc	-	8.192	-	MHz	
Transmit clock frequency	TCLK	-	2.048	-	MHz	
Transmit clock tolerance	TCLKt	-	-	±100	ppm	
Transmit clock duty cycle	TCLKd	10	-	90	%	
TPOS/TNEG to TCLK setup time	t_{SUT}	50	-	-	ns	
TCLK to TPOS/TNEG Hold time	t_{HT}	50	-	-	ns	

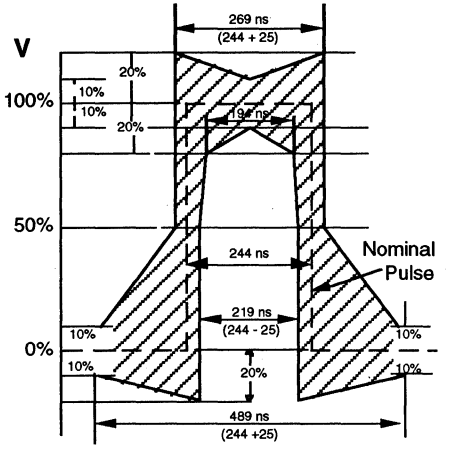
[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Short Circuit Limit

The LXT318 transmitter is equipped with a short-circuit limiter. This feature limits to approximately 120 mA RMS the current the transmitter will source into a low-impedance load. The limiter trips when the RMS current exceeds the limit for 100 µs (~ 150 marks). It automatically resets when the load current drops below the limit.

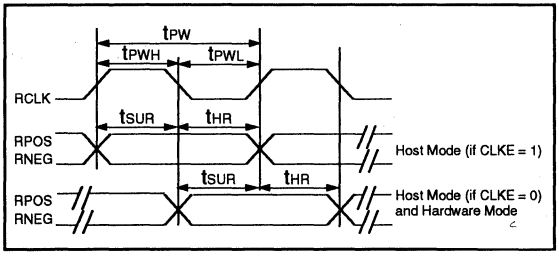
The LXT318 meets or exceeds CCITT specifications for NTU applications, as well as requirements for ISDN PRI.

Figure 4: 2.048 MHz E1 Pulse Mask



Parameter	TPW	Units
Test load impedance	120	Ω
Nominal peak mark voltage	3.0	V
Nominal peak space voltage	0 ± 0.30	V
Nominal pulse width	244	ns
Ratio of positive and negative pulse amplitudes at center of pulse	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	%

Figure 5: LXT318 Receive Clock Timing



Receiver

The receiver input from the twisted-pair is received via a 1:1 transformer. Recovered data is output at RPOS/RNEG (RDATA in unipolar mode), and the recovered clock is output at RCLK. Refer to Figure 5 and Table 4 for receiver timing.

The signal received at RTIP and RRING is processed through the receive equalizer which may apply up to 43 dB of gain. Insertion loss of the line, as indicated by the

Table 4: LXT318 Receive Timing Characteristics (See Figure 5)

Parameter	Sym	Min	Typ[1]	Max	Units
Receive clock duty cycle [2]	RCLKd	40	50	60	%
Receive clock pulse width [2]	t_{PW}	–	488	–	ns
Receive clock pulse width high	t_{PWH}	-	244	-	ns
Receive clock pulse width low	t_{PWL}	220	244	268	ns
RPOS / RNEG to RCLK rising setup time	t_{SUR}	-	194	-	ns
RCLK rising to RPOS /RNEG hold time	t_{HR}	-	194	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

[2] RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 2.048 MHz.)

receive equalizer setting, is encoded in the LATN output as shown in Figure 6.

The equalized signal is filtered and applied to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. The threshold is set to 50% of the peak value. The receiver is capable of accurately recovering signals with up to 43 dB of cable attenuation (from 2.7 V).

After processing through the data slicers, the received signal is routed to the data and timing recovery section, then to the HDB3 decoder (if selected) and to the LOS processor. The data and timing recovery sections provide an input jitter tolerance significantly better than required by CCITT G.823, as shown in Figure 7.

The LOS Processor loads a digital counter at the RCLK frequency. The count is incremented each time a zero (space) is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS

Figure 6: LXT318 Line Attenuation (LATN) Pulse Width Encoding

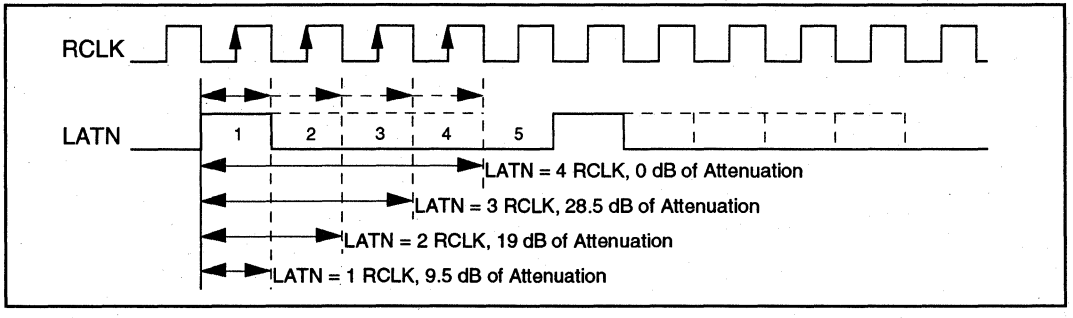
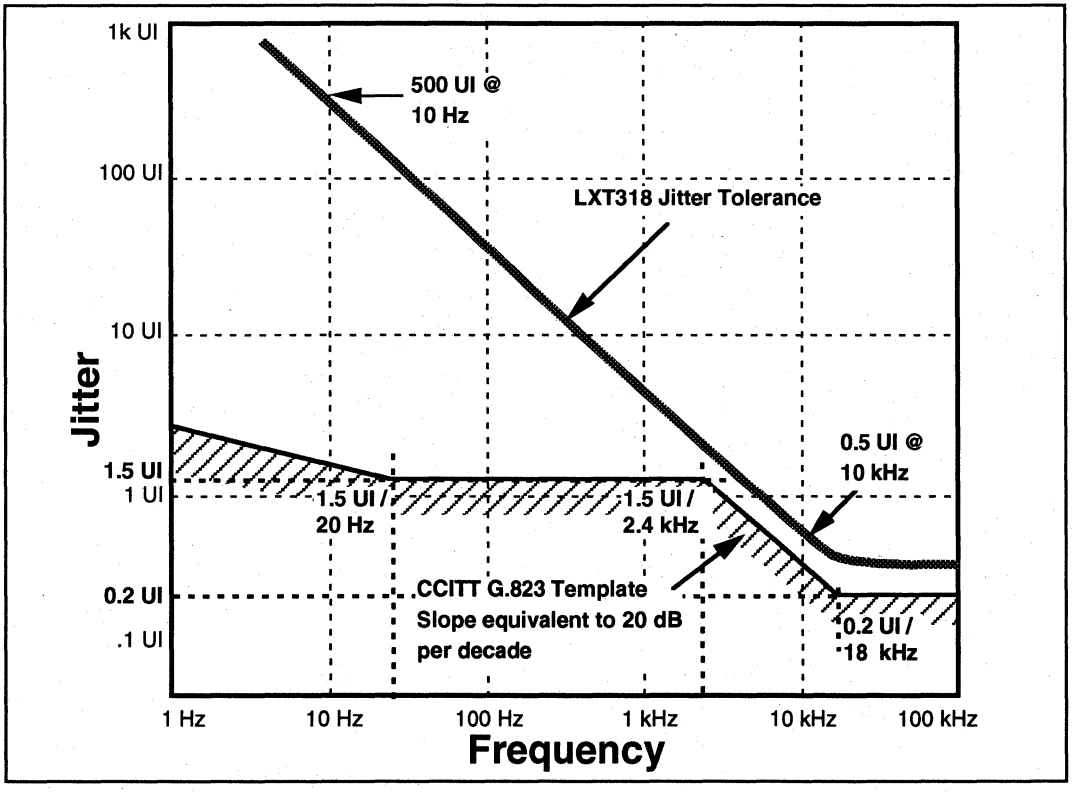


Figure 7: LXT318 Jitter Tolerance @ 43 dB (Typical)



pin goes high, and a smooth transition replaces the RCLK output with the MCLK. *(During LOS , if MCLK is not supplied and JASEL = 1, the RCLK output is replaced with the centered quartz crystal frequency.)*

Received marks will be output regardless of the LOS status, but the LOS pin will not reset until the ones density reaches 12.5 %. This level is based on receipt of at least 4 ones in any 32 bit periods, with no more than 15 consecutive zeros.

Jitter Attenuation

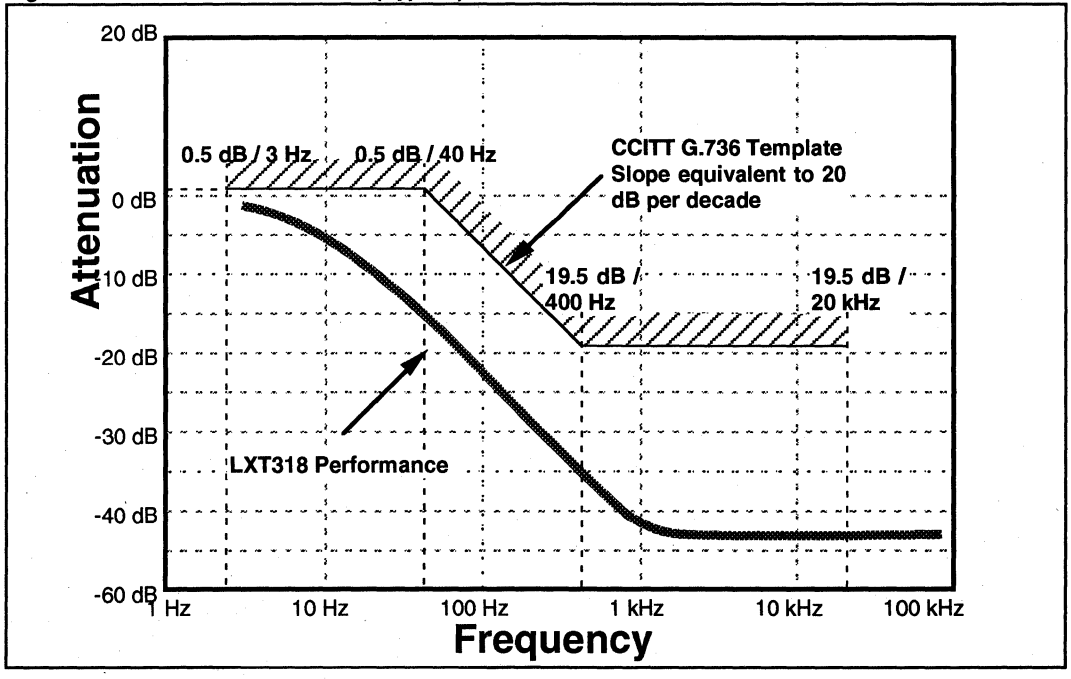
Jitter attenuation is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). Figure 8 shows the LXT318 jitter attenuation performance compared with the jitter template specified by CCITT G.736. An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 5 for crystal specifications. The ES is a 32 x 2-bit register. When JASEL = 1, the JAL is positioned in the receive path. When JASEL = 0, the JAL is positioned in the transmit path.

Data (TPOS/TNEG / TDATA or RPOS/RNEG / RDATA) is clocked into the ES with the associated clock signal (TCLK or RCLK), and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the associated path.

Table 5: LXT318 Crystal Specifications (External)

Parameter	Specification
Frequency	8.192 MHz
Frequency Stability	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm
Effective series resistance	40 Ω max
Crystal cut	AT
Resonance	Parallel
Drive level	2.0 mW max
Mode of operation	Fundamental
Crystal holder	HC49 (R3W), C_0 = 7 pF max C_M = 17 fF typical

Figure 8: LXT318 Jitter Attenuation (Typical)



Control Modes

The LXT318 transceiver can be controlled by a microprocessor through a serial interface (Host mode), or through individual hard-wired pins (Hardware mode). The mode of operation is determined by the input to pin 5 (MODE). With MODE set high (1), the LXT318 operates in the Host mode. With MODE set low (0), the LXT318 operates in the Hardware mode. With MODE tied to RCLK, the LXT318 operates in the Hardware mode with the HDB3 encoder/decoder enabled. The LXT318 can also be commanded to operate in one of several diagnostic modes.

Host Mode Control

The LXT318 operates in the Host mode when pin 5 (MODE) is set high. In Host mode the LXT318 is controlled through the serial I/O port (SIO) by a microprocessor. The LXT318 provides a pair of data registers, one for command inputs and one for status outputs, and an interrupt ($\overline{INT}$) output.

An SIO transaction is initiated by a low-going pulse on the two Chip Select pin, $\overline{CS}$. The 318 responds by writing the incoming serial word from the SDI pin into its command register. If the command word contains a read request, the 318 subsequently outputs the contents of its status register onto the SDO pin. The Clock Edge (CLKE) signal determines when the SDO and receive data outputs are valid, relative to the Serial Clock (SCLK) or RCLK as listed in Table 6.

Table 6: CLKE Settings

CLKE	Output	Clock	Valid Edge
LOW	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
HIGH	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

The 16-bit serial word consists of an 8-bit Command/Address byte and an 8-bit Data byte as shown in Figures 9 and 10. SIO timing characteristics are shown in Table 8, and Figures 11 and 12.

Serial Input Word

Figure 9 shows the Serial Input data structure. The LXT318 is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. Bit 1 of the serial Address/Command byte provides Read/Write (R/W) control when the chip is accessed. The R/W bit is set to logic 1 to read the data output byte from the chip, and set to logic 0 to write the input data byte to the chip.

The second 8 bits of a write operation, the Data Input byte, clear Loss of Signal (LOS) interrupts, reset the chip, and control HDB3 encoding/decoding, and diagnostic modes. The first bit (D0) clears and/or masks LOS interrupts, the third bit (D2) enables or disables HDB3 coding/decoding, and the last 3 bits (D5 - D7) control operating modes (normal and diagnostic) and chip reset. Refer to Table 7 for details on bits D5 - D7.

Table 7: SIO Input Bit Settings (See Figure 9)

Mode	RLOOP Bit D5	LLOOP Bit D6	TAOS Bit D7
RLOOP	1	0	N/A
LLOOP	0	1	N/A
TAOS	0	N/A	1
RESET	1	1	0

Serial Output Word

Figure 10 shows the Serial Output data structure. When the Serial Input word had bit A0 = 1, the LXT318 drives the output data byte onto the SDO pin. The output data byte reports Loss of Signal (LOS) conditions, HDB3 code setting, and operating modes (normal or diagnostic as shown in Table 8). The first bit (D0) reports LOS status. The third bit (D2) reports the HDB3 setting. The last 3 bits (D5 - D7) report operating modes and interrupt status.

Table 8: LXT318 Serial Data Output Bit Coding (See Figure 10)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	LLOOP active
0	1	1	TAOS and LLOOP active
1	0	0	RLOOP active
1	0	1	Reserved
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	Reserved

The Host mode provides a latched Interrupt output pin, $\overline{INT}$. An interrupt is triggered by a change in the LOS bit (D0 of the output data byte). If the $\overline{INT}$ line is high (no interrupt is pending), bits D5 - D7 report the operating modes listed in Table 8. If the $\overline{INT}$ line is low, the interrupt status overrides all other reports and bits D5 - D7 reflect the interrupt status as listed in Table 8.

Figure 9: LXT318 SIO Input Data Structure

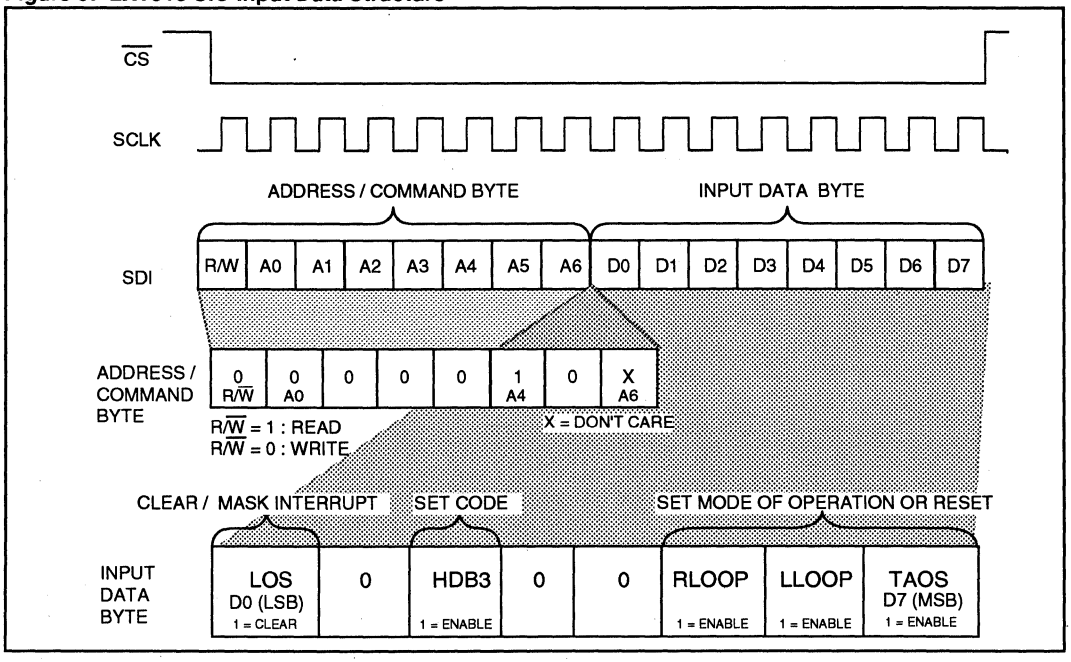


Figure 10: LXT318 SIO Output Data Structure

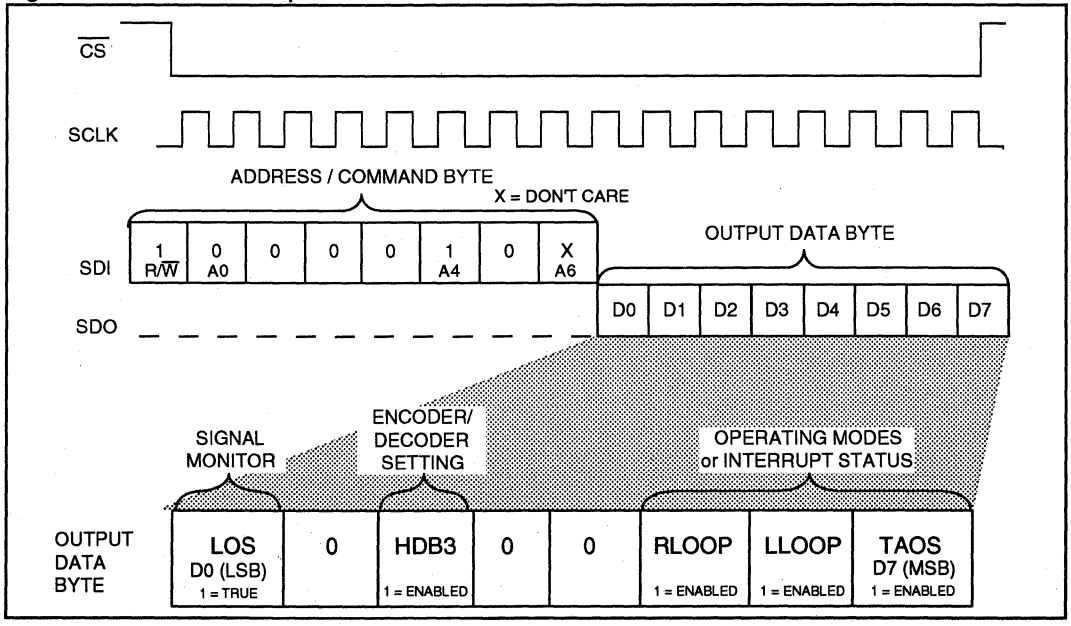


Table 9: LXT318 Serial I/O Timing Characteristics (See Figures 11 and 12)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	-	-	100	ns	Load 1.6 mA, 50pF
SDI to SCLK setup time	t_{DC}	50	-	-	ns	
SCLK to SDI hold time	t_{CDH}	50	-	-	ns	
SCLK low time	t_{CL}	240	-	-	ns	
SCLK high time	t_{CH}	240	-	-	ns	
SCLK rise and fall time	t_R , t_F	-	-	50	ns	
$\overline{CS}$ to SCLK setup time	t_{CC}	50	-	-	ns	
SCLK to $\overline{CS}$ hold time	t_{CCH}	50	-	-	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	-	-	ns	
SCLK to SDO valid	t_{CDV}	-	-	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	-	100	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 11: LXT318 Serial Data Input Timing Diagram

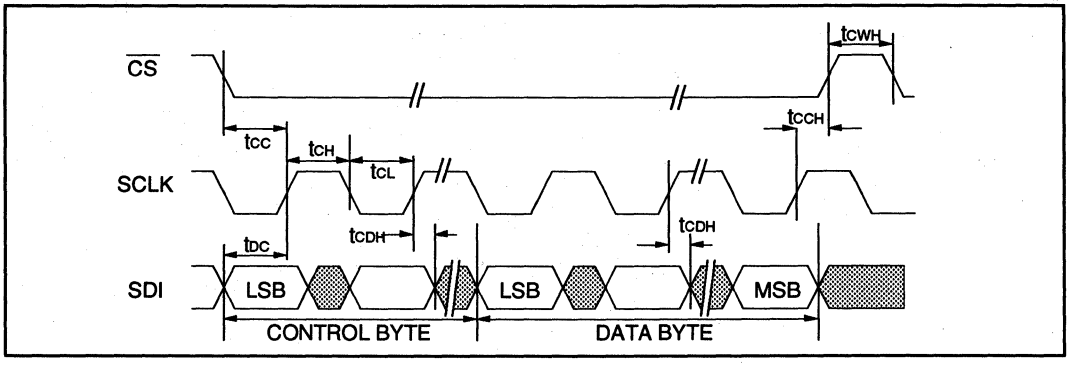
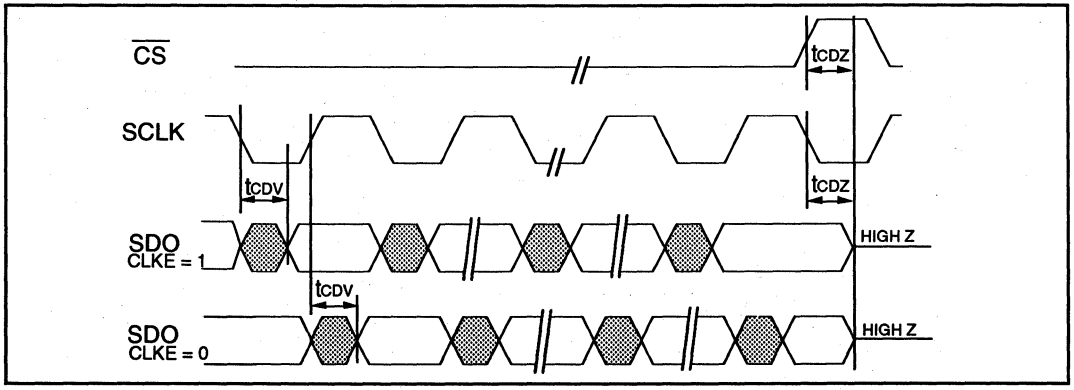


Figure 12: LXT318 Serial Data Output Timing Diagram

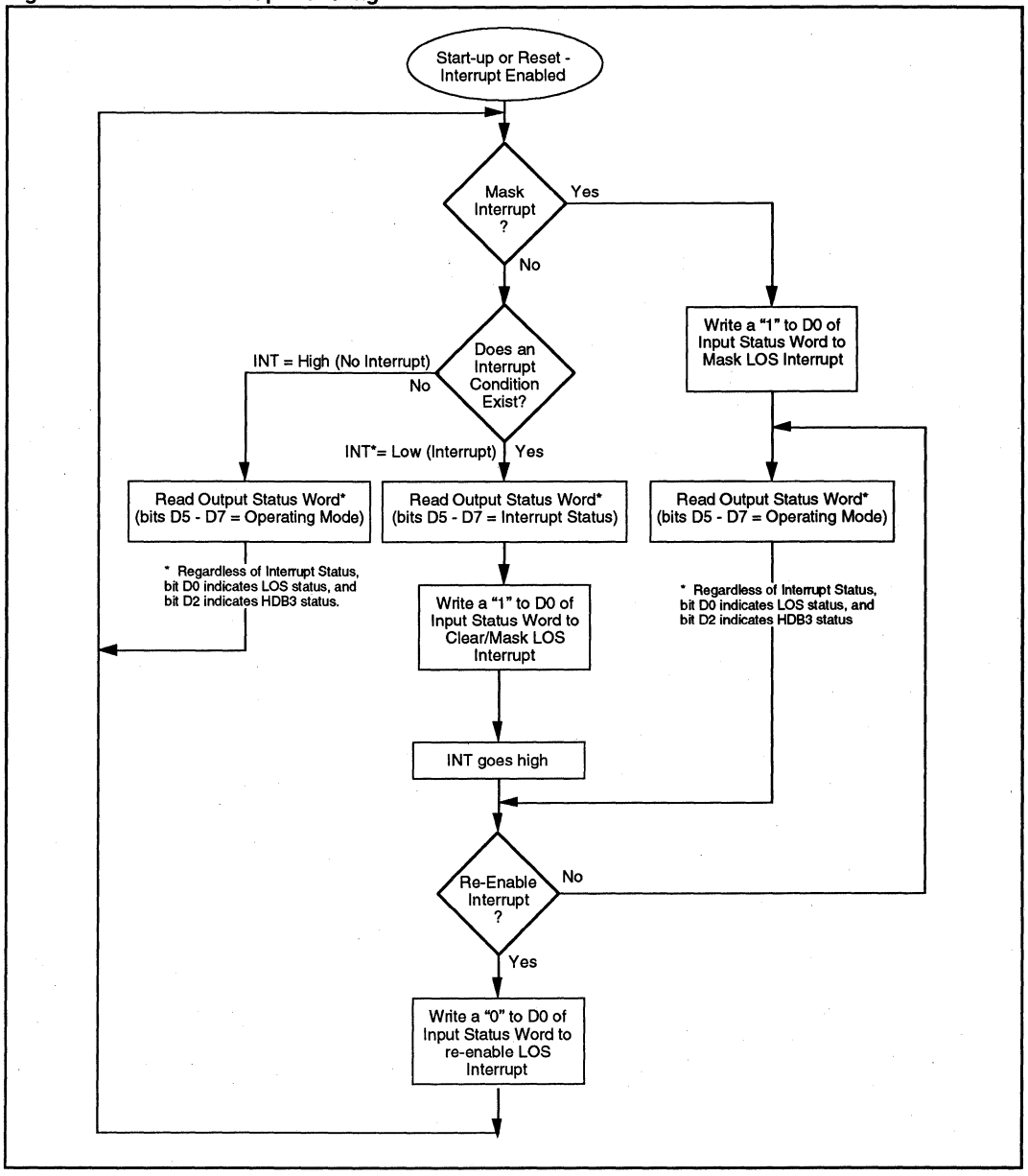


Interrupt Handling

As shown in Figure 13, the interrupt generator can be masked by writing a one to the respective bit of the input data byte (D0). When an interrupt has occurred, the $\overline{INT}$ output pin is pulled low. The output stage of the $\overline{INT}$ pin consists only of a pull-down device. Hence, an external pull-up resistor is required. The interrupt is cleared as follows:

1. If the interrupt bit (LOS, D0 of the output data byte) is high, writing a one to the respective input bit (D0, of the input data byte) will clear the interrupt. Leaving a one in this bit position will effectively mask the interrupt. To re-enable the interrupt capability, reset D0 to zero.
2. If the LOS bit is not high, the interrupt will be cleared by resetting the chip. To reset the chip, set data input bits D5 and D6 = 1, and D7 = 0.

Figure 13: LXT318 Interrupt Handling



Hardware Mode Operation

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{INT}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS/RNEG or RDATA outputs are valid on the rising edge of RCLK. The LXT318 operates in Hardware mode only when MODE is set to 0 or connected to RCLK.

Initialization and Reset Operation

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. The crystal oscillator provides the receiver reference. If the crystal oscillator is grounded, MCLK is used as the receiver reference clock. All PLLs are continuously calibrated.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing ones to RLOOP and LLOOP, and a zero to TAOS. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns while holding TAOS low. In either mode, reset sets all registers to 0.

Diagnostic Mode Operation

Transmit All Ones. See Figure 14. In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored and the transceiver transmits a continuous stream of 1's at the TCLK frequency. (In the LXT318 with JASEL = 0 and TCLK not provided, TAOS is locked to the MCLK.) This can be used as the Blue Alarm Indicator (AIS). In Host mode, TAOS is commanded by writing a one to bit D7 of the input data byte. In Hardware mode, TAOS is commanded by setting pin 28 high. TAOS can be commanded simultaneously with Local Loopback as shown in Figure 15, but is inhibited during Remote Loopback.

Local Loopback. See Figure 16. Local Loopback (LLOOP) is designed to exercise the maximum number of functional blocks. During LLOOP operation, the RTIP/RRING inputs from the line are disconnected. Instead, the transmit outputs are routed back into the receive inputs. This tests the encoders/decoders, jitter attenuator, transmitter, receiver and timing recovery sections. In Host mode, Local Loopback is commanded by writing a one to bit D6 of the input data byte. In Hardware mode, Local Loopback is commanded by setting pin 27 high. If TAOS and LLOOP are both set, the All Ones pattern is transmitted onto the line while the TPOS/TNEG input data is looped back to the RPOS/RNEG outputs through the jitter attenuator.

Remote Loopback. See Figure 17. In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TCLK and TPOS/TNEG or TDATA) are ignored, and the in-line encoders and decoders are bypassed. The RPOS/RNEG or RDATA outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line. In Host mode, Remote Loopback is commanded by writing a one to bit D5 of the input data byte. In Hardware mode, Remote Loopback is commanded by setting pin 26 high.

Application Considerations

LATN Decoding Circuits and External Components

The line attenuation (LATN) output is encoded as a simple serial bit stream for use in line monitoring applications. Table 10 provides the decoded output for each equalizer setting. Figure 18 is a typical decoding circuit for the LATN output. It uses a 2-bit synchronous counter (half of a 4-bit counter) with synchronous reset, and a pair of flip-flops. Table 11 lists approved crystals and transformers.

Figure 14: TAOS Data Path

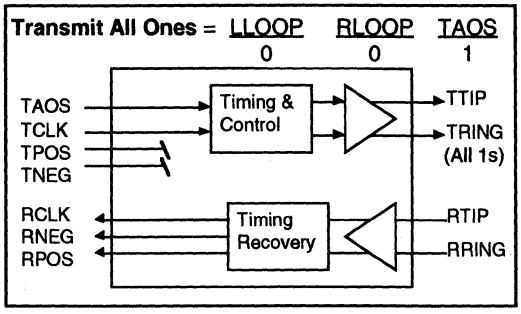


Figure 15: TAOS with LLOOP Data Path

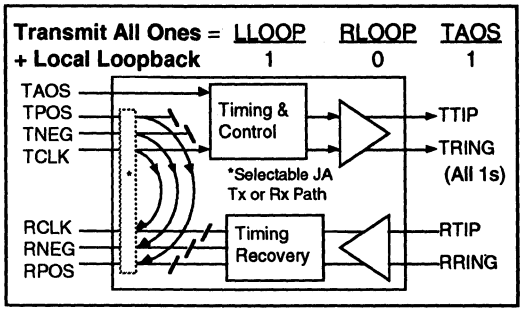


Figure 16: Local Loopback Data Path

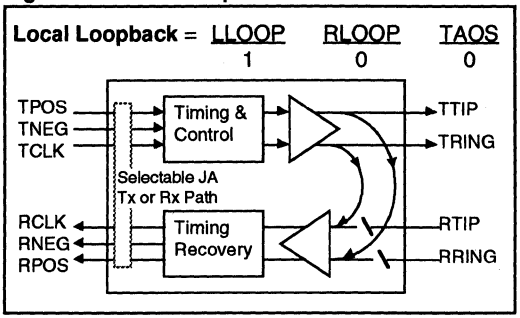


Figure 17: Remote Loopback Data Path

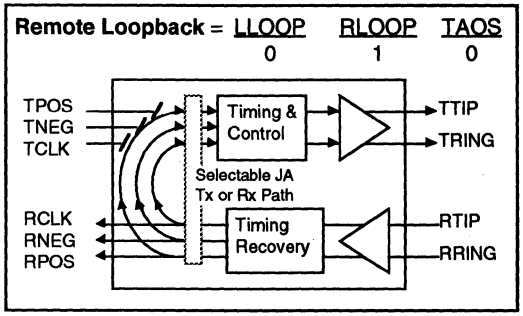
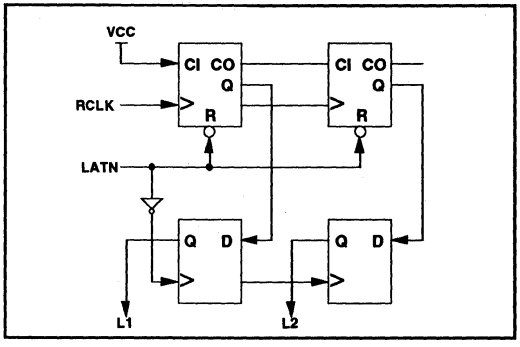


Table 10: LATN Output Coding

L1	L2	Line Attenuation
0	0	0.0 dB
0	1	-9.5 dB
1	0	-19.0 dB
1	1	-28.5 dB

Figure 18: Typical LATN Decoding Circuit



Power Requirements

The LXT318 is a low-power CMOS devices. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ±.3V of each other, and decoupled to their respective grounds separately, as shown in Figure 19. Isolation between the transmit and receive circuits is provided internally.

LXT318 Host Mode Applications

Figure 19 shows a typical E1 NTU application with the LXT318 operating in the Host mode (MODE pin tied high). The LXP2181A E1/CRC Framer provides the digital interface with the host controller. Both devices are controlled through the serial interface. In the Host mode, the LOS alarm is reported via the serial port so the LOS pin is not used (although it still reports valid LOS status.)

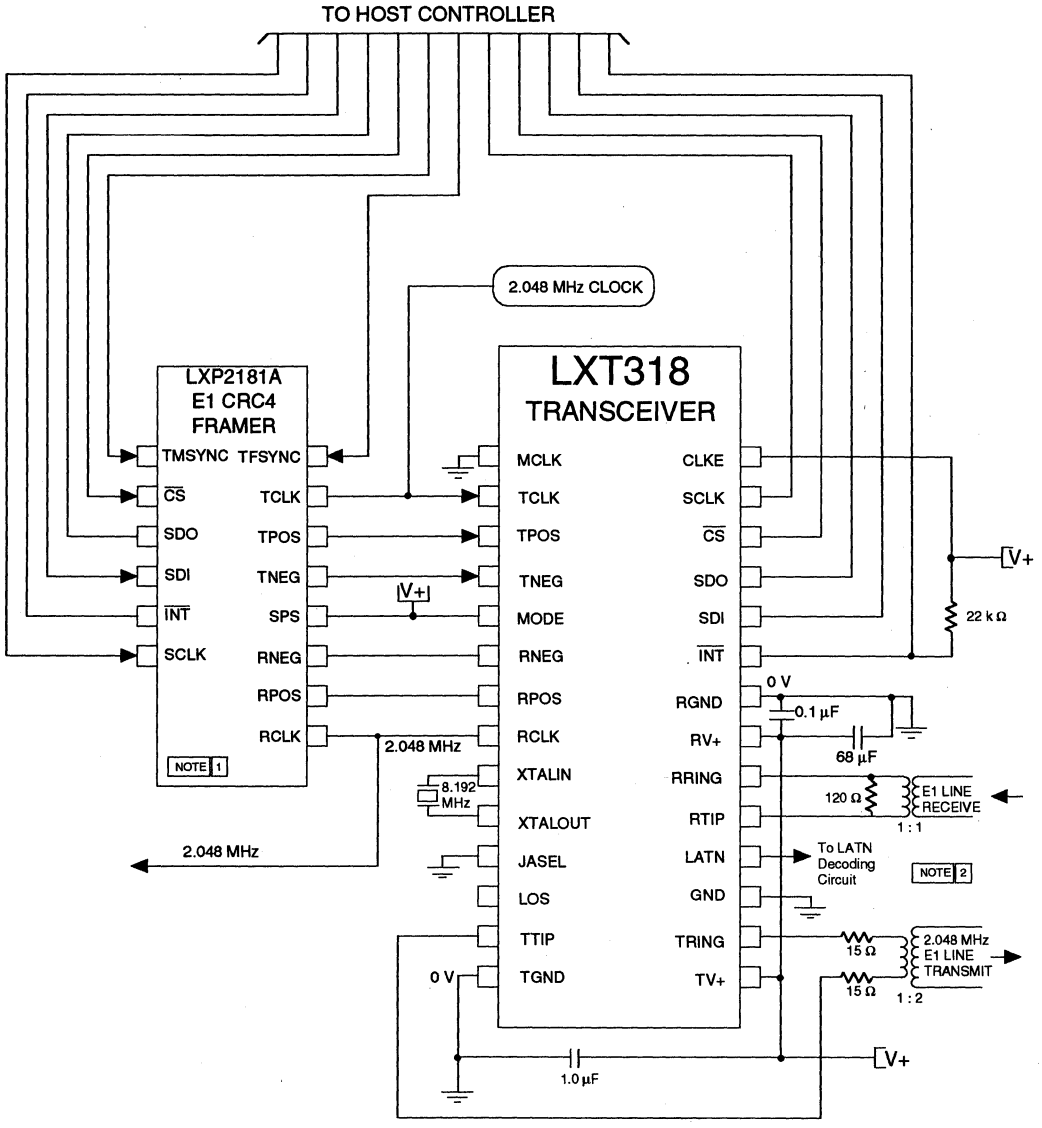
The 8.192 MHz crystal across XTALIN and XTALOUT enables the JAL which is switched to the transmit side by the ground on JASEL. The power supply inputs are tied to a common bus with appropriate decoupling capacitors (68µF and 0.1 µF) installed on each side.

The line interfaces are relatively simple. A 120 Ω resistor (for TWP applications) across the input of a 1:1 transformer is used on the receive side, and a pair of 15 Ω resistors are installed in series with the 1:2 transmit transformer.

Table 11: Approved Crystals and Transformers

Component	Manufacturer	Part Numbers
Crystal (8.192 MHz)	CTS Knights	8192-100
	M-Tron	3808-020
	Monitor Products	MSC1311-01B-8.192
	U .S. Crystal	U18-18-8192SP
	Valpey Fisher	VF49A16FN1-8.192
Tx Transformer (1:2)	Bell Fuse	0553-5006-IC
	FEE Fil-Mag	66Z1308
	Midcom	671-5832
	Pulse Engineering	65351, 65771
	Schott Corp	67127370 and 67130850
	HALO	TD61-1205G and TD67-1205G (combo Tx/Rx)
Rx Transformer (1:1)	FEE Fil-Mag	FE 8006-155
	Midcom	671-5792
	Pulse Engineering	64936 and 65778
	Schott Corp	67130840 and 67109510
	HALO	TD61-1205G and TD67-1205G (combo Tx/Rx)

Figure 19: Typical LXT318 Host Mode E1 / NTU Application



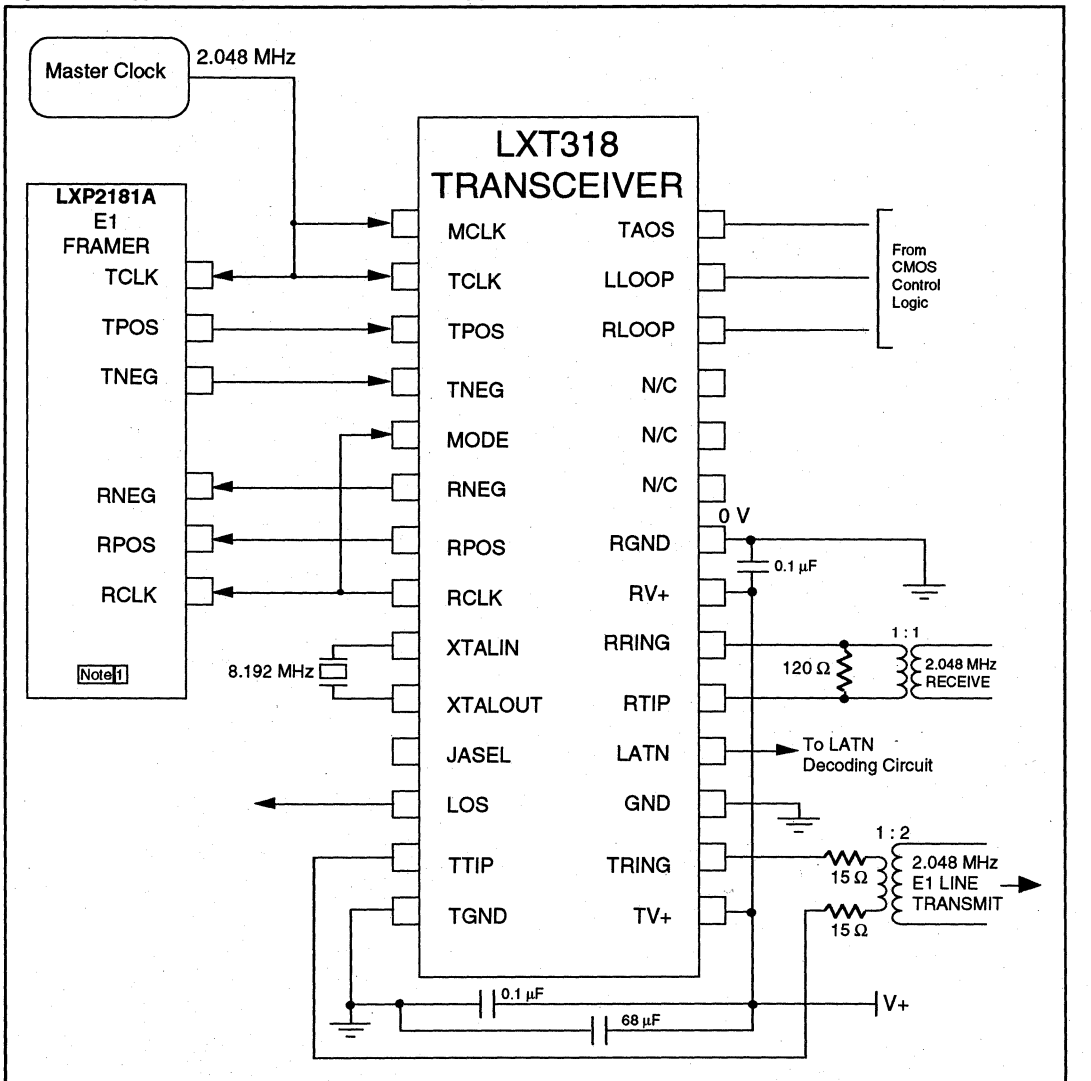
NOTE 1 IN ADDITION TO THE LXP2181A, THE LXT318 IS COMPATIBLE WITH A WIDE VARIETY OF DIGITAL FRAMING AND SIGNALING DEVICES, INCLUDING THE DS2181A, MT8979, AND R8070.

NOTE 2 THE LXT318 IS COMPATIBLE WITH A VARIETY OF TRANSFORMER RATIOS AND RESISTOR VALUES.

LXT318 Hardware Mode Applications

Figure 20 shows a typical 2.048 MHz application with the LXT318 operating in the Hardware mode. As in Figure 19, this configuration is illustrated with a single power supply bus. CMOS control logic is used to set the TAOS, LLOOP and RLOOP diagnostic modes individually. The RCLK output is tapped to clock the MODE pin, enabling HDB3 encoding. The receive and transmit line interfaces are identical to the Host mode application shown in Figure 19.

Figure 20: Typical LXT318 Hardware Mode Application



NOTE 1 In addition to the LXP2181A, the LXT318 is compatible with a wide variey of framing/signaling devices, including the DS2181A, MT8979 and R8070.

LXT332

Dual T1 / E1 Line Interface Unit

General Description

The LXT332 is a fully integrated dual Line Interface Unit (LIU) for both North American 1.544 MHz (T1), and European 2.048 MHz (E1/CEPT) applications. It features B8ZS/HDB3 encoders and decoders, and a constant low output impedance transmitter for high return loss. Transmit pulse shape is selectable for various line lengths and cable types.

The LXT332 incorporates an advanced crystal-less digital jitter attenuator starting at 6 Hz, switchable to either the transmit or receive side. This eliminates the need for an external quartz crystal. It offers both a serial interface (SIO) for microprocessor control and a hardware control mode for stand-alone operation.

The LXT332 offers a variety of advanced diagnostic and performance monitoring features. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

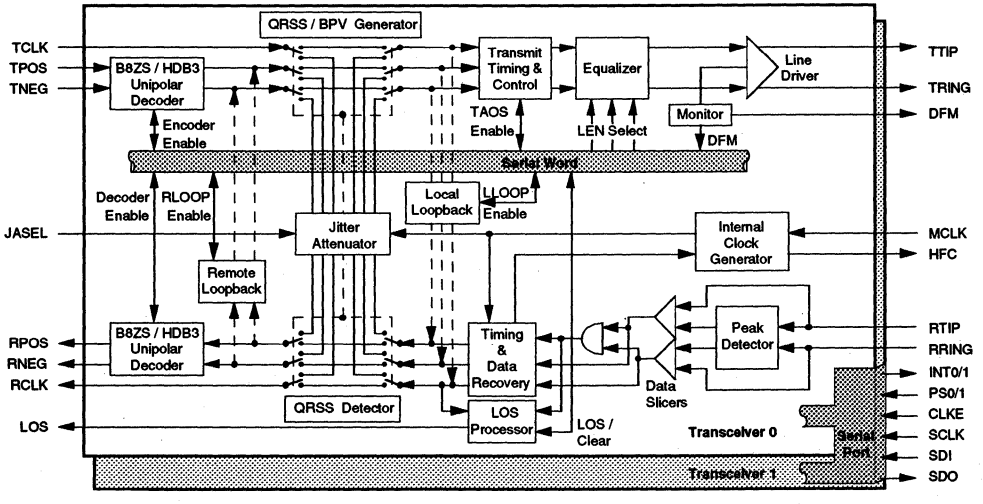
Applications

- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- SONET/SDH Multiplexers
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

Features

- Digital (crystal-less) jitter attenuation, selectable for receive or transmit path
- High transmit and receive return loss
- Constant low output impedance transmitter with programmable equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- Meets or exceeds industry specifications including CCITT G.703, ANSI T1.403 and AT&T Pub 62411
- Compatible with most industry standard framers
- Complete line driver, data recovery and clock recovery functions
- Minimum receive signal of 500 mV, with selectable slicer levels (CEPT/DSX-1) to improve SNR
- Local, remote, and dual loopback functions
- Built-In Self Test with QRSS Pattern Generator
- Transmit / Receive performance monitors with Driver Fail Monitor (DFM) and Loss of Signal (LOS) outputs
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Available in 44-pin PLCC

Figure 1: LXT332 Block Diagram



- **Two complete LIUs in a single PLCC**
- **Simplifies board design, saves real estate**
- **Proven architecture (LXT3xx series)**
- **New Features**

In addition to the **inherent advantages** of a dual LIU, the LXT332 also provides several **advanced features** which are not available in other LXT30x-series devices. All of the added features are **easily implemented**. Many require only a clock pulse to change from one mode to another. Some features are available in Host Mode only.

Standard LXT332 Features

- **Tristate Outputs**
  All LXT332 output pins can be forced to a high-Z tristate mode. The tristate mode is enabled or disabled by the TRSTE pin.

- **Bipolar or Unipolar Data I/O**
  The LXT332 / Framer interface can be either bipolar (default) or unipolar (selectable). The unipolar mode is selected by applying a clock to the TRSTE pin. The MCLK, TCLK, RCLK or any other available clock that is close to the line frequency can be used.

- **B8ZS or HDB3 Zero Suppression**
  The LXT332 incorporates zero suppression encoders and decoders for use in the unipolar data I/O mode. The encoders/decoders can be activated or deactivated by changing the logic level on the re-mapped TNEG pin.

- **Selectable Jitter Attenuation**
  Jitter attenuation can be placed in either the transmit or receive path, or deactivated. The Jitter Attenuation Select (JASEL) pin determines the jitter attenuation mode.

- **Dual Loopback**
  This option enables simultaneous loopbacks to both the framer and the line. The TCLK, TPOS and TNEG framer inputs are routed through the jitter attenuator and looped back out the RCLK RPOS and RNEG outputs. The RTIP/RRING line inputs are looped back through the timing recovery block and line driver onto the TTIP/TRING outputs.

Additional Host-Mode Features

- **High Frequency Clocks**
  The LXT332 provides a pair of high frequency clock outputs, one from each LIU. These 8x clocks (12.352 MHz for T1, 16.384 MHz for E1) are tied to the de-jittered clock from the JA of the respective LIU.

- **Bipolar Violation Insertion**
  The same pins which provide the High Frequency Clocks can also be used to insert bipolar violations into the outgoing data stream. Violations can be inserted into each LIU channel independently.

- **Built-In Self Test (QRSS)**
  The LXT332 can generate and transmit a QRSS pattern for Built-In Self Test (BIST) applications. Logic errors and bipolar violations can be inserted into the QRSS output. The LXT332 also detects QRSS pattern synchronization and reports bit errors in the received QRSS pattern data stream.

- **AIS Detection**
  The LXT332 detects the AIS alarm signal on the receive side independent of the loopback modes. When AIS is detected (less than 3 zeros in 2048 bits), the LXT332 provides an indicator output.

LXT312 / LXT315

Low Power T1 PCM Repeaters

General Description

The LXT312 and LXT315 are integrated repeater circuits for T1 carrier systems. The LXT312 is a dual repeater and the LXT315 is a single repeater. The LXT312 and LXT315 are designed to operate as regenerative repeaters for 1.544 Mbit/s data rate PCM lines. Each includes all circuits required for a regenerative repeater system including the equalization network, automatic line build-out (ALBO), and a state of the art analog/digital clock extraction network tuned by an external crystal.

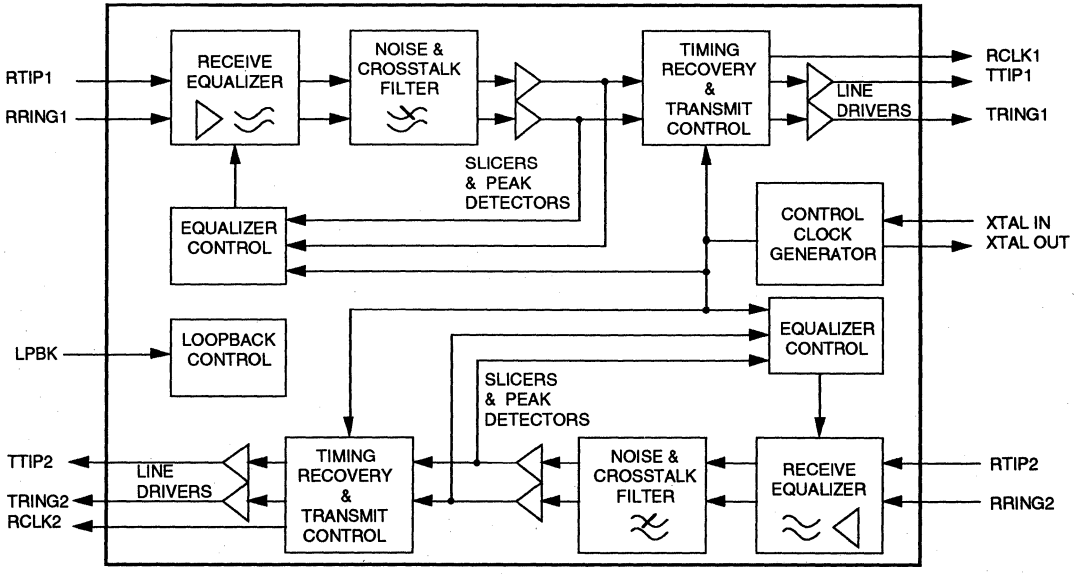
The key feature of the LXT312 family is that it requires only a crystal and a minimum of other components to complete a repeater design. Compared with traditional tuned coil-type repeaters, they offer significant savings in component and labor costs, along with reduced voltage drop/power consumption, and improved reliability. To ensure performance for all loop lengths, the LXT312 and LXT315 are 100% AC/DC tested using inputs generated by Level One's proprietary transmission line and network simulator.

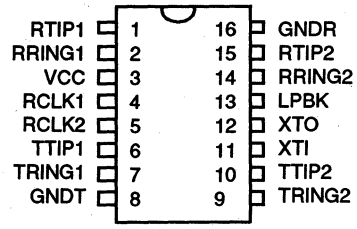
The LXT312 and LXT315 are advanced CMOS devices which require only a single +5V power supply.

Features

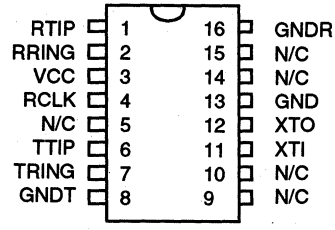
- Integrated repeater circuit on a single CMOS chip
- On-chip equalization network
- On-chip ALBO
- Low power consumption
- No tuning coil
- On-chip Loopback
- Recovered Clock Output
- 0 to 36 dB dynamic range
- -11 dB interference margin
- Compatible with CB113/TA24 specifications
- Single 5 V only CMOS technology
- Available in 16-pin ceramic DIP

Figure 1: LXT312 Block Diagram





LXT312



LXT315

Pin Descriptions

Pin #	Sym	I/O	Name	Description
1	RTIP1	I	Repeater Tip and	Tip and ring receive inputs for Channel 1.
2	RRING1	I	Ring Inputs	
4	RCLK1	O	Recovered Clock	Clock output recovered from Channel 1 receive input.
6	TTIP1	O	Repeater Tip and	Open drain output drivers for Channel 1.
7	TRING1	O	Ring Outputs	
11	XTI	I	Crystal Oscillator	Either a 6.176 MHz crystal must be connected across these two
12	XTO	O	Input and Output	pins, or a clock must be applied at XTI and XTO left floating.
3	VCC	I	Power Supply	Power supply input for all circuits. +5 V (±0.25 V)
8	GNDT	–	Transmit Ground	Ground return for transmit circuits.
16	GNDR	–	Receive Ground	Ground return for receive circuits.
9 [1]	TRING2	O	Repeater Side 2 Tip	On the LXT312 dual repeater, these are open drain output
10 [1]	TTIP2	O	and Ring Outputs	drivers for Channel 2.
14 [1]	RRING2	I	Repeater Side 2	On the LXT312 dual repeater these are tip and ring receive
15 [1]	RTIP2	I	Ring and Tip Inputs	inputs for Channel 2.
5 [1]	RCLK2	O	Recovered Clock	On the LXT312 dual repeater, this is the recovered clock output for Channel 2.
13 [2]	LPBK	I	Loopback Control	On the LXT312, this pin controls Loopback Selection. High = Loopback side 1 data to side 2. Low = No Loopback.

Notes:
1. On the LXT315 single repeater, these pins are not connected (N/C).
2. On the LXT315 single repeater, this pin must be connected to GND.

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

• Supply Voltage	V_{CC}	-0.3 V to 6 V
• Driver Voltage	V_{OH}	18 V
• Receiver Current	I_{CC}	100 mA
• Operating temperature	T_{OP}	-40 °C (min) to +85 °C (max)
• Storage temperature	T_{ST}	-65 °C (min) to +150 °C (max)

Recommended Operating Conditions (Voltages are with respect to ground unless otherwise specified.)

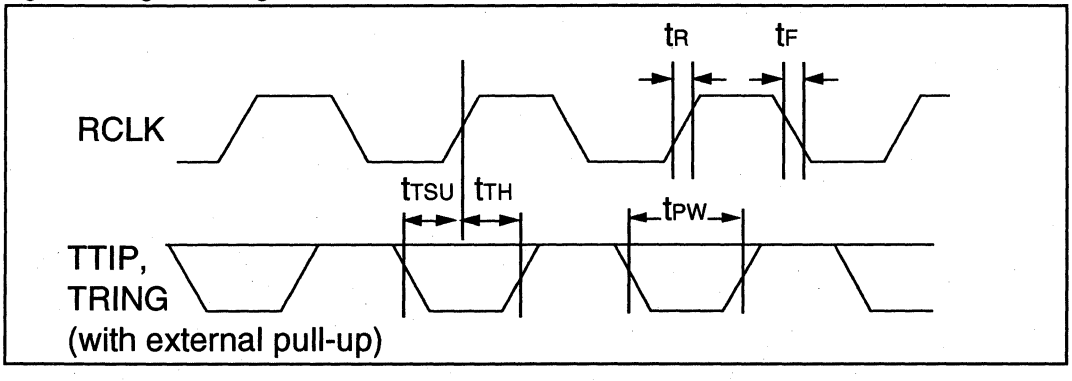
Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Operating temperature	T_{OP}	-40	–	85	°C

Electrical Characteristics (Ta = -40 to 85 °C, V_{CC} = 5V ±5%)

Parameter		Symbol	Min	Typ[1]	Max	Units
Interference Margin		SNR	-11	–	–	dB
Receiver Dynamic Range		–	-36	–	0	dB
Digital Outputs - Low	(I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
	(I_{OL} = 10 µA)	V_{OL}	–	0.2	–	V
Digital Outputs - High	(I_{OH} = 0.4 mA)	V_{OH}	2.4	–	–	V
	(I_{OH} < 10 µA)	V_{OH}	–	4.5	–	V
Digital Inputs - High		V_{IH}	2.0	–	–	V
Digital Inputs - Low		V_{IL}	–	–	0.8	V
Supply Current	All zeros	I_{CC}	–	15	22	mA
(from VCC supply)[2]	All ones	I_{CC}	–	–	23	mA
Driver Leakage Current (V_{DVR} = 18 V)		I_{LL}	–	–	100	µA
Driver Pulse Amplitude (Driver output I_O = 20 mA)		A_P	0.65	–	0.95	V
Driver Pulse Width		t_{PW}	299	324	349	ns
Driver Pulse Imbalance		–	–	–	15	ns
Rise and Fall Time (any digital output[2])		t_R / t_F	–	–	18	ns
Setup Time - TTIP/TRING to RCLK		t_{TSU}	90	–	–	ns
Hold Time - TTIP/TRING from RCLK		t_{TH}	90	–	–	ns

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Measured with $C_{LOAD} \leq 10$ pF, $R_{LOAD} > 100$ kΩ.

Figure 2: Digital Timing Characteristics



General Description

PCM signals are attenuated and dispersed in time as they travel down a transmission line. Repeaters are required to amplify, reshape, regenerate and retime the PCM signal, then retransmit it.

The LXT312 and LXT315 each contain all the circuits required to build a complete PCM repeater. The operational range of the repeaters is 0 to 36 dB of cable loss at 772 kHz (equal to 6300 feet of 22 gauge pulp-insulated cable between repeaters).

Functional Description

Receive Function

The signal is received through a 1 : 1 transformer at RTIP and RRING and equalized for up to 36 dB of cable loss. The receive equalizer uses a proprietary on-chip adaptive filter technique which is equivalent to a 3-port ALBO equalizer design. The monolithic structure of the filter and the absence of external components provide excellent ISI and dispersion elimination, and accurate data transfer over temperature.

Receiver noise immunity is optimized by a proprietary crosstalk elimination filter which eliminates the unneeded high frequency components of the received signal.

Timing Recovery Function

The equalized signal is full wave rectified and used to generate information for the timing recovery circuit. This circuit uses a mixed analog/digital technique to provide a low-jitter PLL similar to a tuned tank with excellent jitter tracking ability. But unlike a tuned tank, the free running frequency of the PLL clock is accurately controlled by the external reference crystal. No adjustment is required. Refer to Table 1 for crystal specifications.

Recovered clock signals are available on the RCLK pins for applications that require synchronization to the bit stream.

Transmit Function

Recovered data is resynchronized to the recovered clock signal by the timing recovery and transmit control section. The data is then retransmitted to the network via two open drain, high voltage transistors.

Loopback Function (LXT312 Only)

The LXT312 includes a loopback function for network diagnostics. With the LPBK pin low, the repeater operates in the normal mode. When the LPBK pin is pulled high, the data is looped back from side 1 to side 2.

Test Setups

Both the LXT312 and LXT315 are fully tested (100% AC and DC parameters) using inputs generated by Level One's proprietary transmission line and network simulator. Device testing includes receiver jitter tolerance, jitter transfer and interference margin, and receiver immunity to gaussian and 60 Hz noise. Specifications and bench test setups are shown in Figures 3 through 10.

Receiver Jitter Tolerance Testing

Receiver jitter tolerance meets the template shown in Figure 3, when operated at line losses from 0 to 36 dB. Figure 4 shows the setup used for jitter tolerance testing.

Table 1: LXT312/315 Crystal Specifications

Parameter	Specification
Frequency	6.176 MHz
Frequency [1]	± 50 ppm
Effective series resistance	40 Ω Maximum
Crystal cut	AT
Resonance	Parallel
Maximum drive level	2.0 mW
Mode of operation	Fundamental

[1] @ 25° C, C Load = 10 pF; and from -40° C to + 85° C (Ref 25° C reading)

Figure 3: Receiver Jitter Tolerance Template

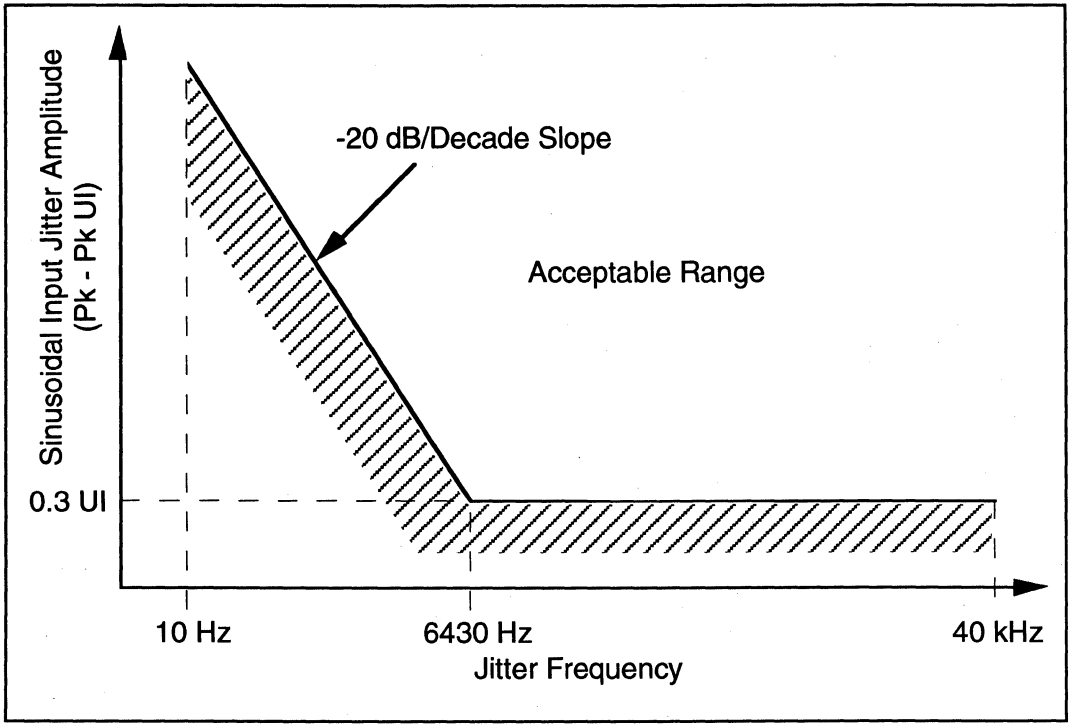
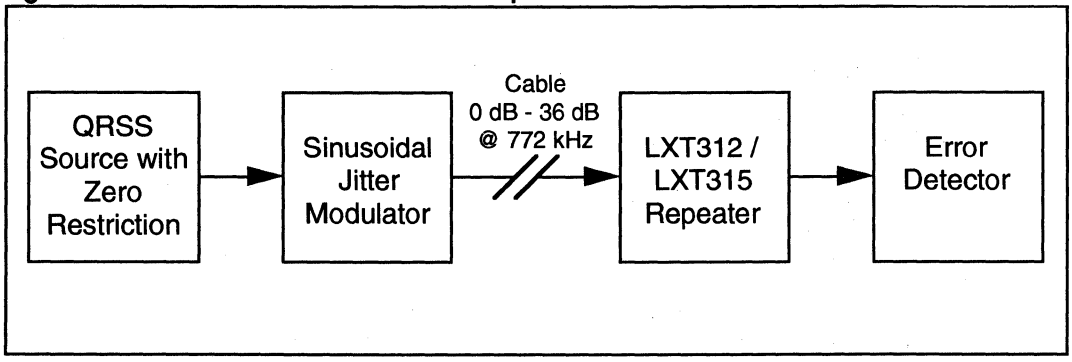


Figure 4: Receiver Jitter Tolerance Test Setup



Receiver Jitter Transfer Testing

Receive jitter transfer meets the template shown in Figure 5, when operated with line losses from 0 to 36 dB and input jitter amplitude of 0.15 UI peak-to-peak. Jitter gain at a given frequency is defined as the difference between intrinsic jitter and additive jitter at the measurement frequency, divided by the amplitude of the input jitter. Figure 6 shows the setup used for jitter transfer testing.

Interference Margin Testing

The LXT312 and LXT315 receiver noise interference margin is specified at a minimum of -11 dB for line losses from 0 dB to 36 dB. The test setup used to measure noise margin is shown in Figure 7.

Figure 5: Receiver Jitter Transfer Template

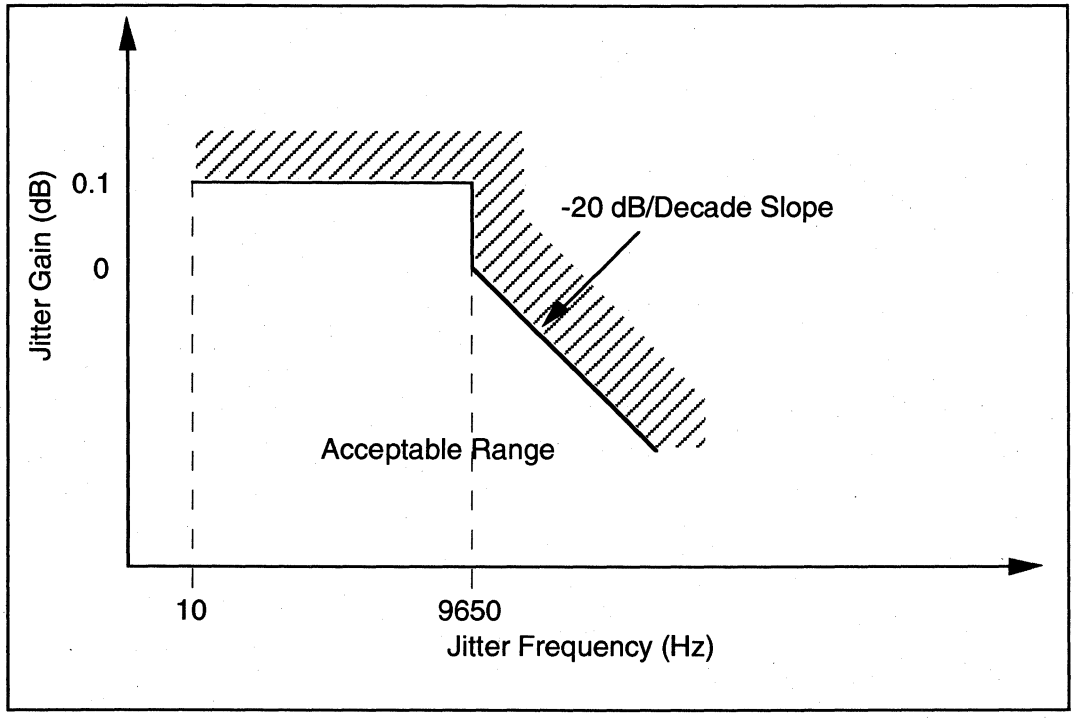
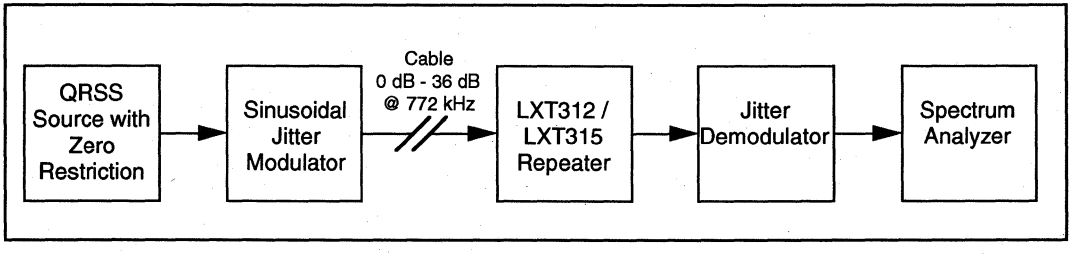


Figure 6: Receiver Jitter Transfer Test Setup



Gaussian Noise Immunity Testing

Receiver immunity to gaussian noise is specified at a maximum BER of 10^{-7} for a quasi-random T1 signal at 1.544 MHz (± 130 ppm). The receiver must be immune to noise power expressed as Np = - (L + 4.7) dBm, where L corresponds to the line loss and is valid for 0 - 36 dB.

Figure 8 shows the setup used to test gaussian noise immunity. The noise source is gaussian to at least 6 sigma and filtered to simulate expected noise in a binder group (per AT&T TA #24/CB113).

60 Hz Pulse Modulation Immunity Testing

Receiver immunity to 60 Hz pulse amplitude modulation is specified using the gaussian noise source described in the previous paragraph on gaussian noise immunity. Pulse amplitude modulation is specified between 10% and 30% of the nominal amplitude (see AT&T TA #24/CB113 for details on the modulation envelope). Figure 9 shows the setup used for testing receiver immunity to 60 Hz pulse amplitude modulation. The following figures reflect noise power for 10^{-7} BER at each modulation level, where L corresponds to the line loss and is valid for 0 - 35 dB:

Modulation Level	Noise Power
10%	Np = - (L + 5.7) dBm
20%	Np = - (L + 6.7) dBm
30%	Np = - (L + 8.7) dBm

2

Figure 7: Receiver Noise Interference Margin Test Setup

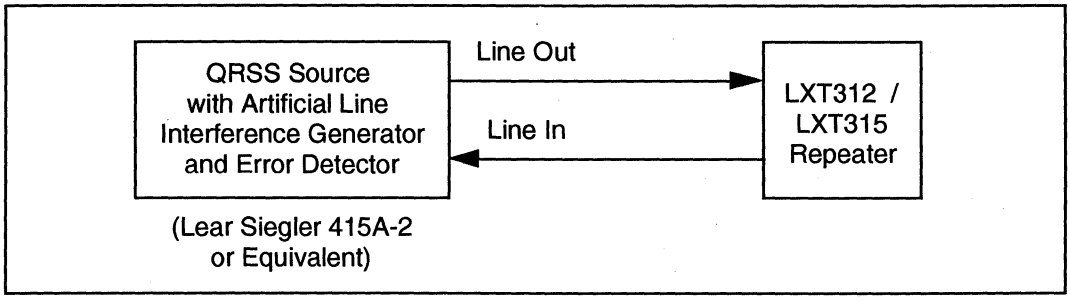
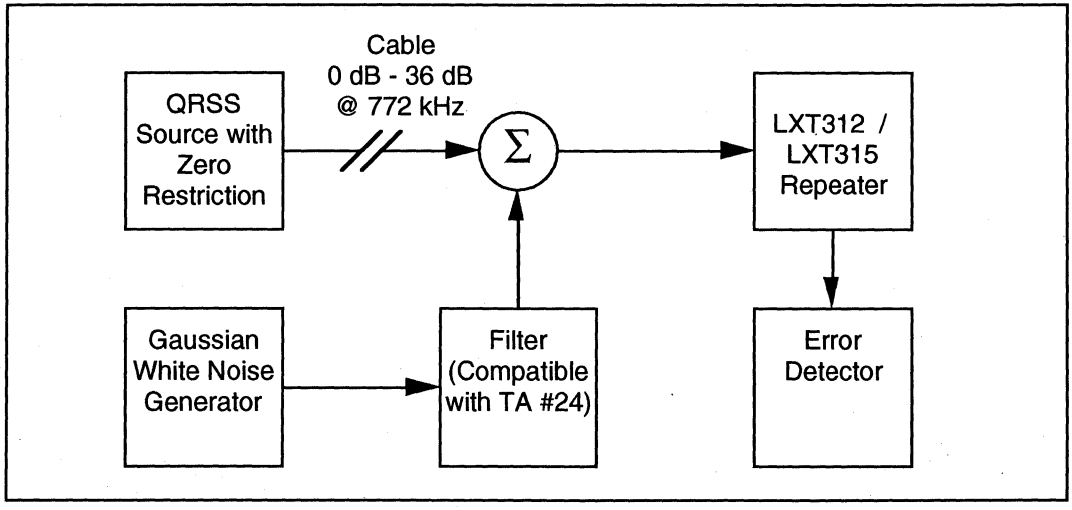


Figure 8: Receiver Gaussian Noise Immunity Test Setup



Receiver Timing Recovery Testing

Receiver timing recovery phase shift modulation for repetitive 8-bit patterns is specified at less than 0.07 UI. This is tested using any two out of 35 possible 8-bit patterns and measuring the change in output pulse timing from one pattern to the other (see AT&T TA #24 / CB113 for details on the patterns). Switching rate from one pattern to the other is specified at between 300 Hz and 500 Hz. The setup used to test receiver timing recovery phase shift modulation is shown in Figure 10.

Figure 9: Receiver 60 Hz Pulse Amplitude Modulation Immunity Test Setup

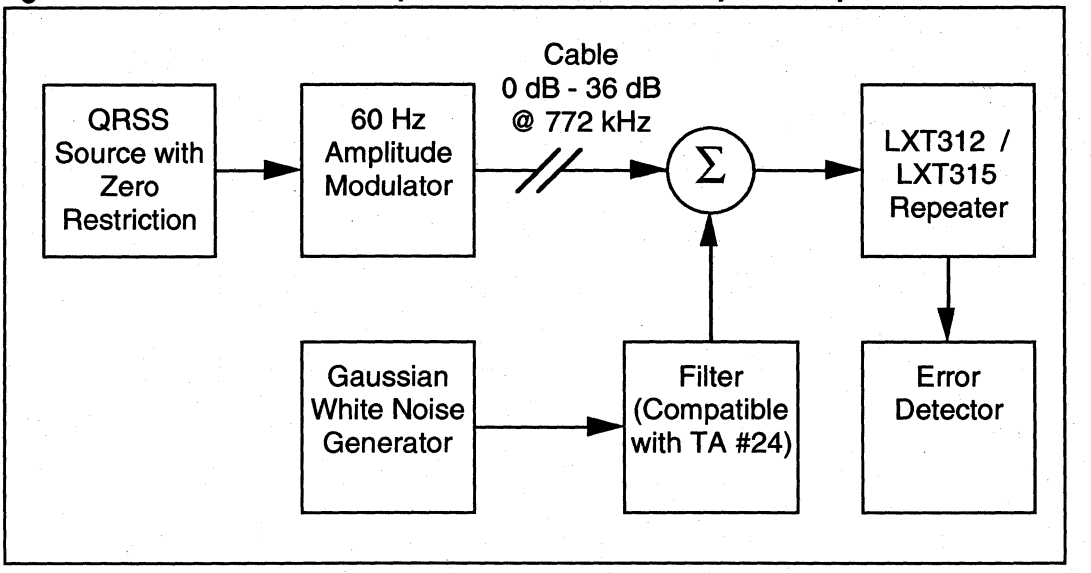
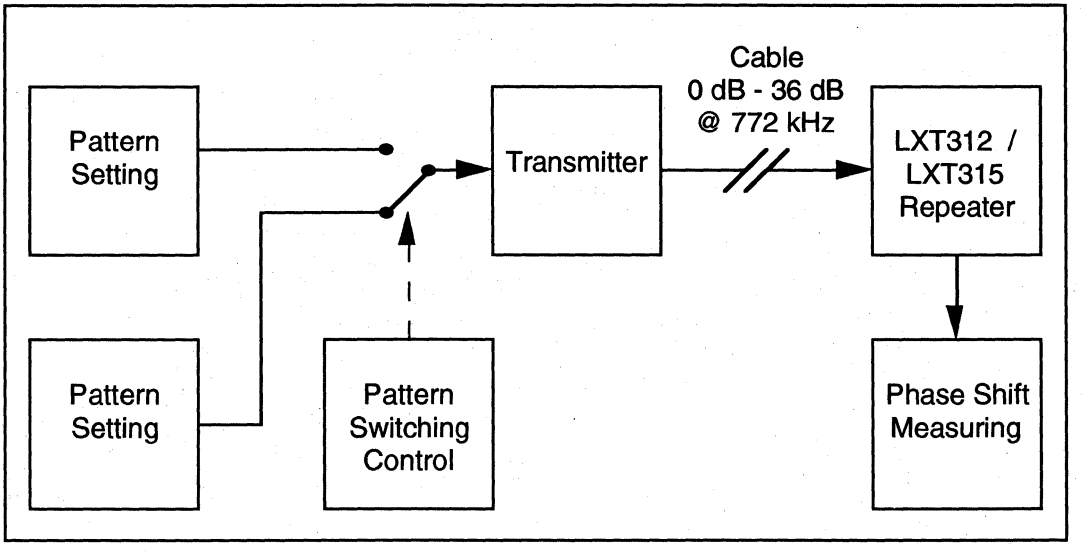


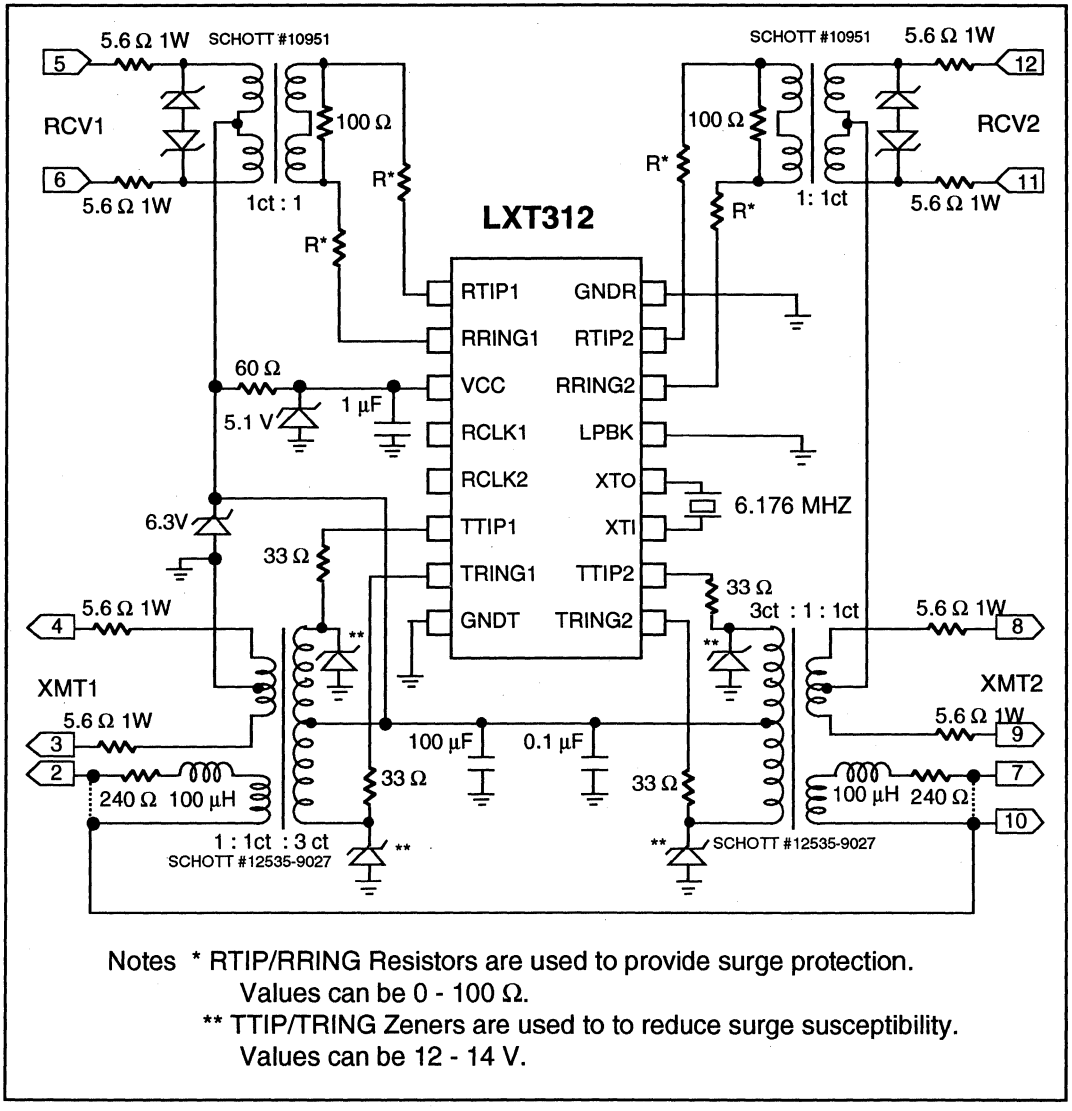
Figure 10: Receiver Timing Recovery Phase Shift Modulation Test Setup



Applications

Figure 11 is a typical T1 dual repeater application circuit showing standard repeater card edge connections. A jumper selectable shorting option for the fault location circuitry is also shown (dashed lines, connector pins 2 and 7).

Figure 11: Typical T1 Dual Repeater Application Diagram



Notes * RTIP/RRING Resistors are used to provide surge protection.
Values can be 0 - 100 Ω.
** TTIP/TRING Zeners are used to to reduce surge susceptibility.
Values can be 12 - 14 V.

NOTES:

LXT313 / LXT316

Low Power E1 PCM Repeaters

General Description

The LXT313 and LXT316 are integrated repeater circuits for E1 carrier systems. The LXT313 is a dual repeater and the LXT316 is a single repeater. The LXT313 and LXT316 are designed to operate as regenerative repeaters for 2.048 Mbit/s data rate PCM lines. Each includes all circuits required for a regenerative repeater system including the equalization network, automatic line build-out (ALBO), and a state of the art analog/digital clock extraction network tuned by an external crystal.

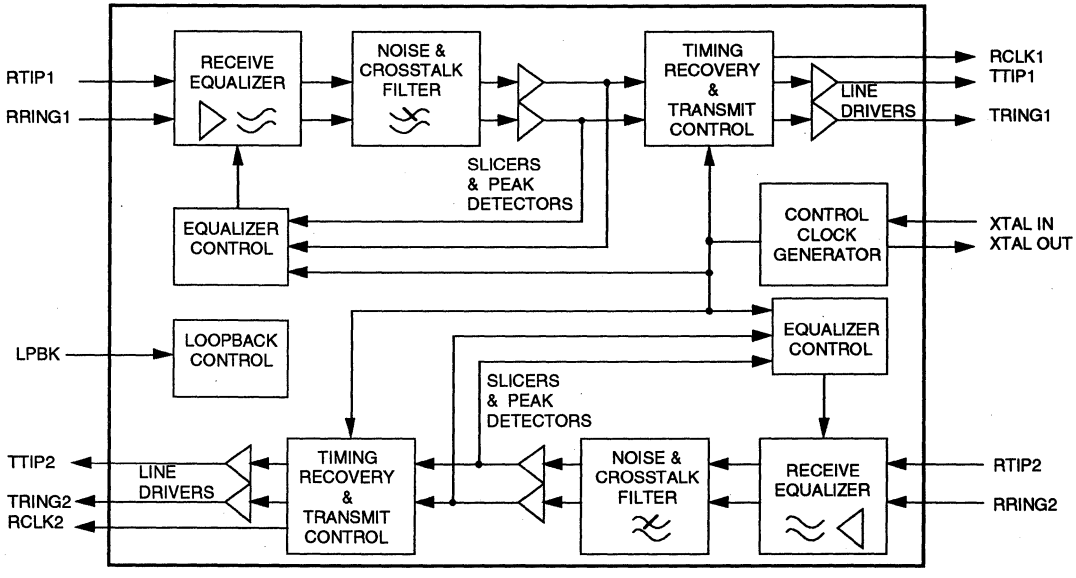
The key feature of the LXT313 family is that it requires only a crystal and a minimum of other components to complete a repeater design. Compared with traditional tuned coil-type repeaters, they offer significant savings in component and labor costs, along with reduced voltage drop/power consumption, and improved reliability. To ensure performance for all loop lengths, the LXT313 and LXT316 are 100% AC/DC tested using inputs generated by Level One's proprietary transmission line and network simulator.

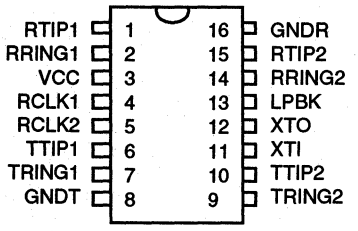
The LXT313 and LXT316 are advanced CMOS devices which require only a single +5V power supply.

Features

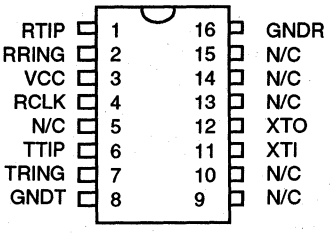
- Integrated repeater circuit on a single CMOS chip
- On-chip equalization network
- On-chip ALBO
- Low power consumption
- No tuning coil
- On-chip Loopback
- Recovered Clock Output
- 0 to 43 dB dynamic range
- -14 dB interference margin
- Single 5 V only CMOS technology
- Available in 16-pin ceramic DIP

Figure 1: LXT313 Block Diagram





LXT313



LXT316

Pin Descriptions

Pin #	Sym	I/O	Name	Description
1	RTIP1	I	Repeater Tip and	Tip and ring receive inputs for Channel 1.
2	RRING1	I	Ring Inputs	
4	RCLK1	O	Recovered Clock	Clock output recovered from Channel 1 receive input.
6	TTIP1	O	Repeater Tip and	Open drain output drivers for Channel 1.
7	TRING1	O	Ring Outputs	
11	XTI	I	Crystal Oscillator	Either a 8.192 MHz crystal must be connected across these two
12	XTO	O	Input and Output	pins, or a clock must be input at XTI and XTO left floating.
3	VCC	I	Power Supply	Power supply input for all circuits. +5 V (±0.25 V)
8	GNDT	–	Transmit Ground	Ground return for transmit circuits.
16	GNDR	–	Receive Ground	Ground return for receive circuits.
9 [1]	TRING2	O	Repeater Channel 2	On the LXT313 dual repeater, these are open drain output
10 [1]	TTIP2	O	Tip and Ring Outputs	drivers for Channel 2.
14 [1]	RRING2	I	Repeater Channel 2	On the LXT313 dual repeater these are tip and ring receive
15 [1]	RTIP2	I	Ring and Tip Inputs	inputs for Channel 2.
5 [1]	RCLK2	O	Recovered Clock	On the LXT313 dual repeater, this is the recovered clock output for Channel 2.
13 [2]	LPBK	I	Loopback Control	On the LXT313, this pin controls Loopback Selection. High = Loopback side 1 data to side 2. Low = No Loopback.

Notes:
1. On the LXT316 single repeater, these pins are not connected (N/C).
2. On the LXT316 single repeater, this pin must be connected to GND.

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

• Supply Voltage	V_{CC}	-0.3 V to 6 V
• Driver Voltage	V_{OH}	18 V
• Receiver Current	I_{CC}	100 mA
• Operating temperature	T_{OP}	-40 °C (min) to +85 °C (max)
• Storage temperature	T_{ST}	-65 °C (min) to +150 °C (max)

Recommended Operating Conditions (Voltages are with respect to ground unless otherwise specified.)

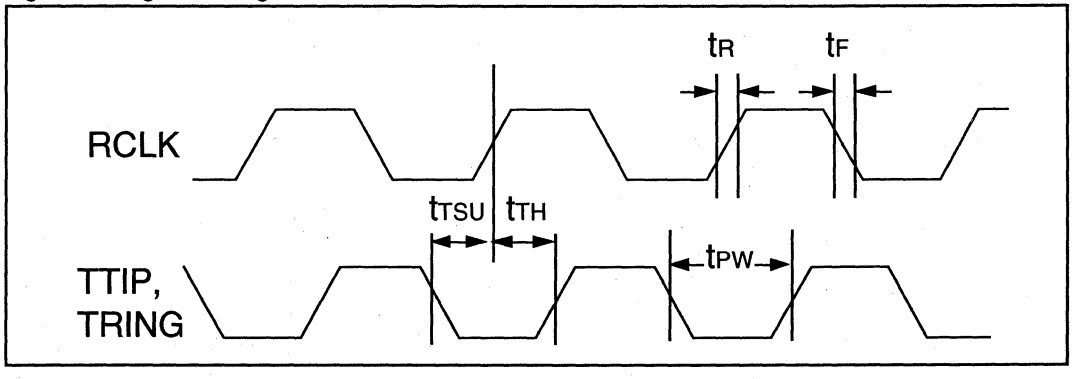
Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Operating temperature	T_{OP}	-40	–	85	°C

Electrical Characteristics (Ta = -40 to 85 °C, V_{CC} = 5V ±5%)

Parameter		Symbol	Min	Typ[1]	Max	Units
Interference Margin		SNR	-14	–	–	dB
Receiver Dynamic Range		–	-43	–	0	dB
Digital Outputs - Low	(I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
	(I_{OL} = 10 µA)	V_{OL}	–	0.2	–	V
Digital Outputs - High	(I_{OH} = 0.4 mA)	V_{OH}	2.4	–	–	V
	(I_{OH} < 10 µA)	V_{OH}	–	4.5	–	V
Digital Inputs - High		V_{IH}	2.0	–	–	V
Digital Inputs - Low		V_{IL}	–	–	0.8	V
Supply Current	All zeros	I_{CC}	–	15	23	mA
(from VCC supply)[2]	All ones	I_{CC}	–	–	25	mA
Driver Leakage Current (V_{DVR} = 18 V)		I_{LL}	–	–	100	µA
Driver Pulse Amplitude (Driver output I_O = 20 mA)		A_P	0.65	–	0.95	V
Driver Pulse Width		t_{PW}	219	244	269	ns
Driver Pulse Imbalance		–	–	–	15	ns
Rise and Fall Time (any digital output[2])		t_R / t_F	–	–	25	ns
Setup Time - TTIP/TRING to RCLK		t_{TSU}	90	–	–	ns
Hold Time - TTIP/TRING from RCLK		t_{TH}	90	–	–	ns

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Measured with $C_{LOAD} \leq 10$ pF, $R_{LOAD} > 100$ kΩ.

Figure 2: Digital Timing Characteristics



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The LXT313 and LXT316 each contain all the circuits required to build a complete PCM repeater. The operational range of the repeaters is 0 to 43 dB of cable loss at 1.024 MHz (equal to 2 km of 22 gauge pulp-insulated cable between repeaters).

Functional Description

Receive Function

The signal is received through a 1 : 1 transformer at RTIP and RRING and equalized for up to 43 dB of cable loss. The receive equalizer uses a proprietary on-chip adaptive filter technique which is equivalent to a 3-port ALBO equalizer design. The monolithic structure of the filter and the absence of external components provide excellent ISI and dispersion elimination, and accurate data transfer over temperature.

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The equalized signal is full wave rectified and used to generate information for the timing recovery circuit. This circuit uses a mixed analog/digital technique to provide a low-jitter PLL similar to a tuned tank with excellent jitter tracking ability. But unlike a tuned tank, the free running frequency of the PLL clock is accurately controlled by the external reference crystal. No adjustment is required. Refer to Table 1 for crystal specifications.

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The LXT313 includes a loopback function for network diagnostics. With the LPBK pin low, the repeater operates in the normal mode. When the LPBK pin is pulled high, the data is looped back from side 1 to side 2.

Test Setups

Both the LXT313 and LXT316 are fully tested (100% AC and DC parameters) using inputs generated by Level One's proprietary transmission line and network simulator. Device testing includes receiver jitter tolerance, jitter transfer and interference margin for line losses from 0 dB to 43 dB @ 1.024 MHz. Specifications and bench test setups are shown in Figures 3 through 7.

Receiver Jitter Tolerance Testing

Receiver jitter tolerance meets the template shown in Figure 3, when operated at line losses from 0 to 43 dB. Figure 4 shows the setup used for jitter tolerance testing.

Table 1: LXT313/316 Crystal Specifications

Parameter	Specification
Frequency	8.192 MHz
Frequency [1]	± 50 ppm
Effective series resistance	30 Ω Maximum
Crystal cut	AT
Resonance	Parallel
Maximum drive level	2.0 mW
Mode of operation	Fundamental

[1] @ 25° C, C Load = 10 pF; and from -40° C to + 85° C (Ref 25° C reading)

Figure 3: Receiver Jitter Tolerance Template

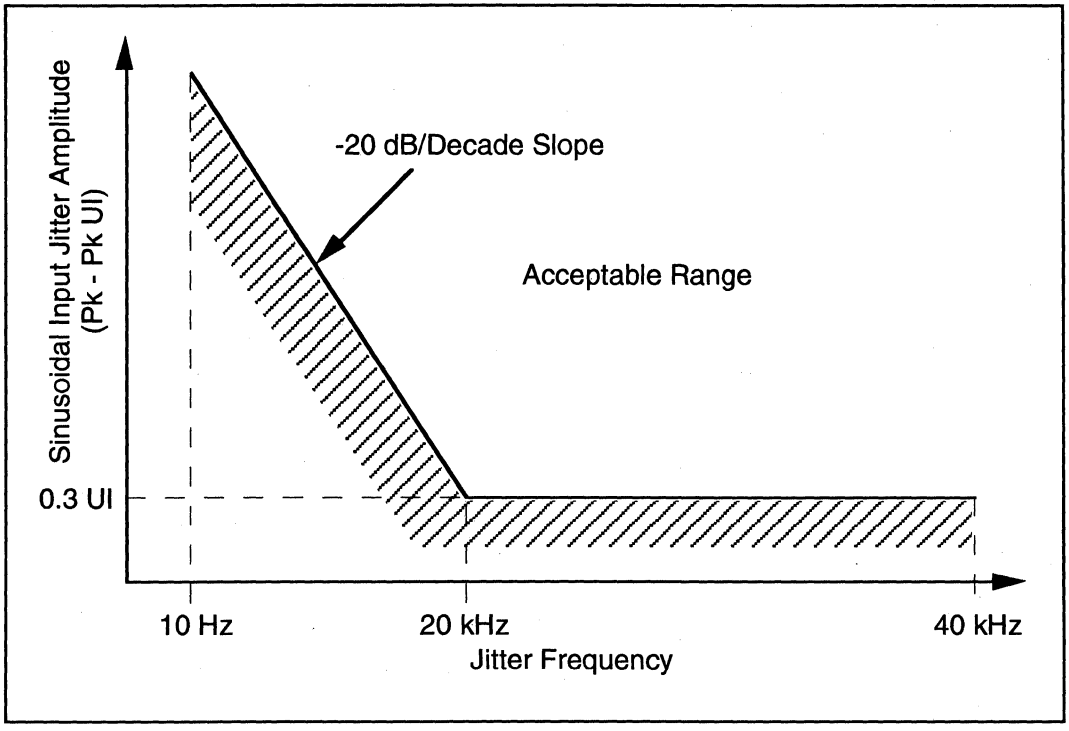
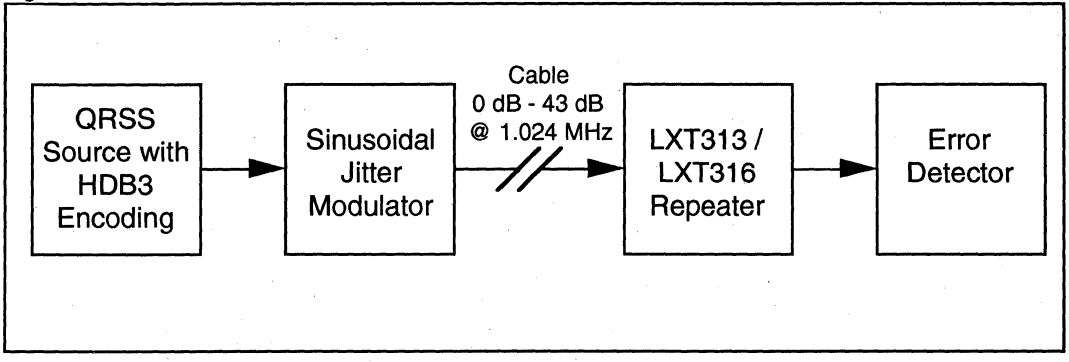


Figure 4: Receiver Jitter Tolerance Test Setup



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Receive jitter transfer meets the template shown in Figure 5, when operated with line losses from 0 to 43 dB and input jitter amplitude of 0.15 UI peak-to-peak. Jitter gain at a given frequency is defined as the difference between intrinsic jitter and additive jitter at the measurement frequency, divided by the amplitude of the input jitter. Figure 6 shows the setup used for jitter transfer testing.

Interference Margin Testing

The LXT313 and LXT316 receiver noise interference margin is specified at a minimum of -14 dB for line losses from 0 dB to 43 dB. The test setup used to measure noise margin is shown in Figure 7.

Figure 5: Receiver Jitter Transfer Template

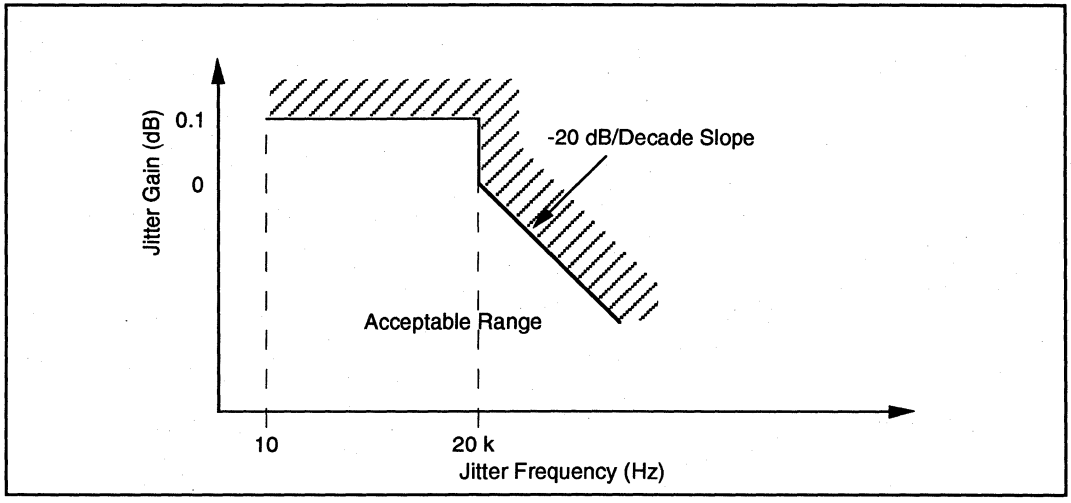


Figure 6: Receiver Jitter Transfer Test Setup

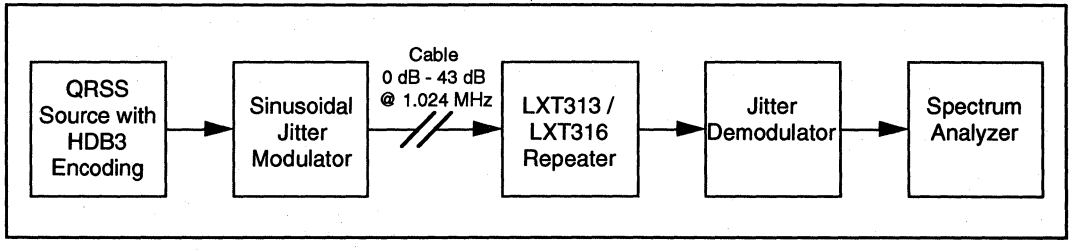
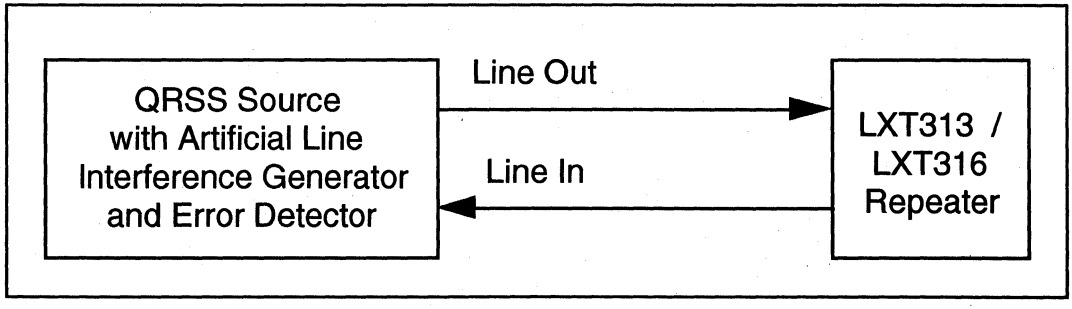


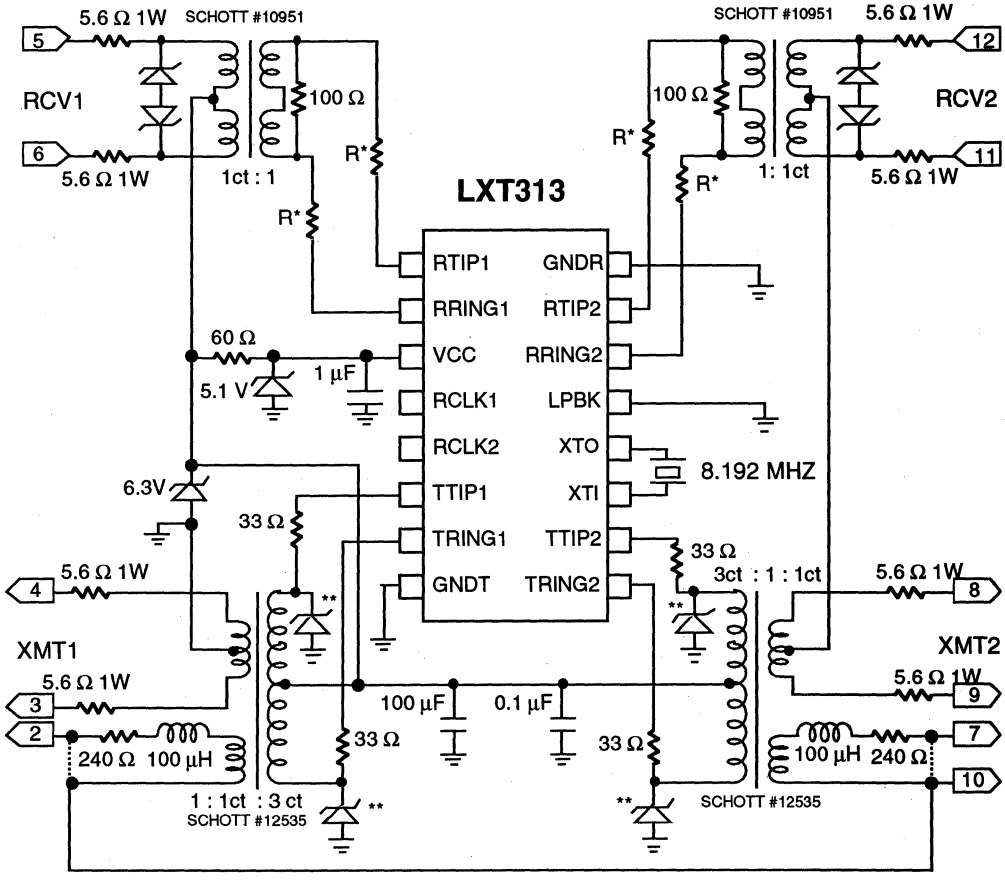
Figure 7: Receiver Noise Interference Margin Test Setup



Applications

Figure 8 is a typical E1 dual repeater application circuit showing standard repeater card edge connections. A jumper selectable shorting option for the fault location circuitry is also shown (dashed lines, connector pins 2 and 7).

Figure 8: Typical E1 Dual Repeater Application Diagram



Notes * RTIP/RRING Resistors are used to provide surge protection.
Values can be 0 - 100 Ω.
** TTIP/TRING Zeners are used to to reduce surge susceptibility.
Values can be 12 - 14 V.

NOTES:

LXT324

T1/E1 Integrated Quad Receiver

General Description

The LXT324 is a fully integrated quad PCM receiver for both North American 1.544 MHz (T1), and European 2.048 MHz (E1) applications. It incorporates four independent receivers in a single 28-pin DIP or PLCC. The operating frequency is pin selectable.

The LXT324 receiver performs data and timing recovery, and uses peak detection and a variable threshold to reduce impulsive noise. LXT324 receiver sensitivity down to 500 mV allows for up to 13.6 dB of attenuation.

The LXT324 is an advanced double-poly, double-metal CMOS device and requires only a single 5-volt power supply.

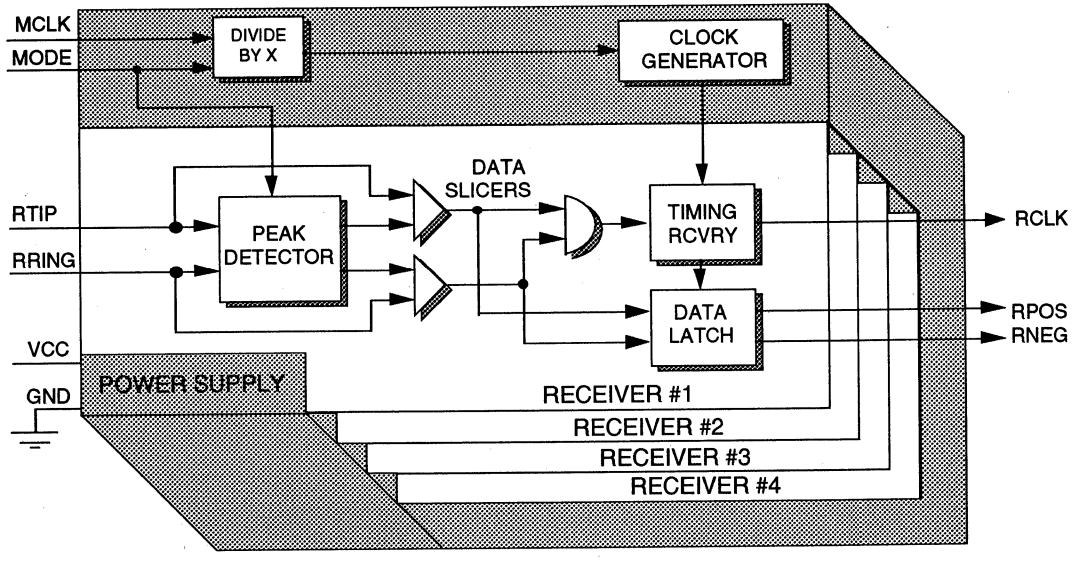
Applications

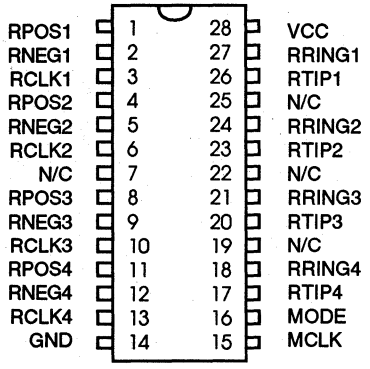
- High-density T1/E1 line cards
- DSX-1/E1 test equipment
- DSX-1/E1 line monitoring
- DSX-1/ E1 receive line interface

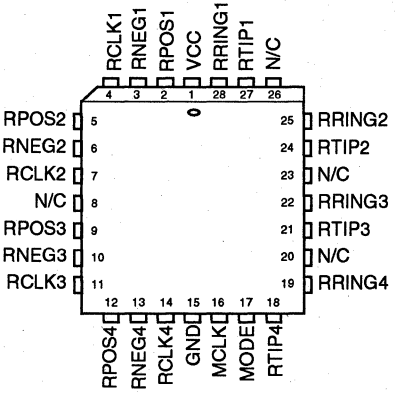
Features

- 4 independent DSX-1/E1 receivers
- Circuit functions include data and clock recovery
- Single Master Clock input
- Meets or exceeds AT&T PUB 62411 requirements for input jitter tolerance
- Unipolar RPOS and RNEG outputs
- Minimum receive signal of 500 mV
- Selectable slicer levels (DSX-1/CEPT) to provide improved SNR
- Single 5 V only CMOS technology
- Available in 28-pin DIP and PLCC

Figure 1: Block Diagram







Pin Descriptions

Pin # DIP	Pin # PLCC	Sym	I/O	Name	Description
1	2	RPOS1	O	Receiver 1 Positive Data	Receiver 1 data outputs. A signal on RNEG1 corresponds to receipt of a negative pulse on RTIP1 and RRING1. A signal on RPOS1 corresponds to receipt of a positive pulse on RTIP1 and RRING1. RNEG1 and RPOS1 outputs are Non-Return-to-Zero (NRZ). Both outputs are stable and valid on the rising edge of RCLK1.
2	3	RNEG1	O	Receiver 1 Negative Data	
3	4	RCLK1	O	Recovered Clock 1	This is the clock recovered from the signal received at RTIP1 and RRING1.
4	5	RPOS2	O	Receiver 2 Positive and Negative Data and Recovered Clock	These are the data and clock outputs recovered from the signal received at RTIP2 and RRING2.
5	6	RNEG2	O		
6	7	RCLK2	O		
7	8	N/C	-	N/C	No connection.
8	9	RPOS3	O	Receiver 3 Positive and Negative Data and Recovered Clock	These are the data and clock outputs recovered from the signal received at RTIP3 and RRING3.
9	10	RNEG3	O		
10	11	RCLK3	O		
11	12	RPOS4	O	Receiver 4 Positive and Negative Data and Recovered Clock	These are the data and clock outputs recovered from the signal received at RTIP4 and RRING4.
12	13	RNEG4	O		
13	14	RCLK4	O		
14	15	GND	--	Ground	Ground.
15	16	MCLK	I	Master Clock	A 1.544 MHz or 2.048 MHz clock input used to generate internal clocks. Upon loss of signal, the RCLKs are derived from MCLK.

Pin Descriptions continued

Pin # DIP	Pin # PLCC	Sym	I/O	Name	Description
16	17	MODE	I	Mode Select	Setting MODE to logic 1 sets the data slicer thresholds to 50% of the incoming signal (CEPT mode). Setting MODE to logic 0 sets the data slicer thresholds to 70% of the incoming signal (DSX-1 mode). The Mode Select operates independently from the MCLK rate. This allows the 50% slicer ratio to be used with a 1.544 MHz MCLK, for improved sensitivity.
17	18	RTIP4	I	Receiver 4 Tip	The AMI signal received from the fourth twisted-pair line is applied at these pins. A center-tapped, center-grounded transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS4/RNEG4, and RCLK4 pins.
18	19	RRING4	I	Receiver 4 Ring	
19	20	N/C	-	N/C	No connection. Must be grounded to reduce crosstalk.
20	21	RTIP3	I	Receiver 3 Tip and Ring	The AMI signal received from the third twisted-pair line is applied to the LXT324 at these pins.
21	22	RRING3	I		
22	23	N/C	-	N/C	No connection. Must be grounded to reduce crosstalk.
23	24	RTIP2	I	Receiver 2 Tip and Ring	The AMI signal received from the second twisted-pair line is applied to the LXT324 at these pins.
24	25	RRING2	I		
25	26	N/C	-	N/C	No connection. Must be grounded to reduce crosstalk.
26	27	RTIP1	I	Receiver 1 Tip and Ring	The AMI signal received from the first twisted-pair line is applied to the LXT324 at these pins.
27	28	RRING1	I		
28	1	VCC	I	Power Supply	+5 VDC power supply.

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

• Supply voltage	V_{CC}	-0.3V to 6V
• Voltage on any I/O pin[1]	$V_{I/O}$	GND -0.3V to V_{CC} +0.3V
• Current on any I/O pin[2]	$I_{I/O}$	±10 mA
• Package power dissipation	P_D	1 W
• Storage temperature	T_{ST}	-65 °C (min) to 150 °C (max)

[1] Excluding RTIP and RRING which must stay within -6V to RV + 0.3V.
[2] Transient currents of up to 100 mA will not cause SCR latch-up.

Recommended Operating Conditions (Voltages are with respect to ground unless otherwise stated)

Parameter	Sym	Min	Typ	Max	Units
Supply voltage	V_{CC}	4.75	5	5.25	V
Operating Temperature	T_{OP}	-40	-	85	°C

DC Electrical Characteristics (Clocked operation over recommended temperature and power supply ranges.)

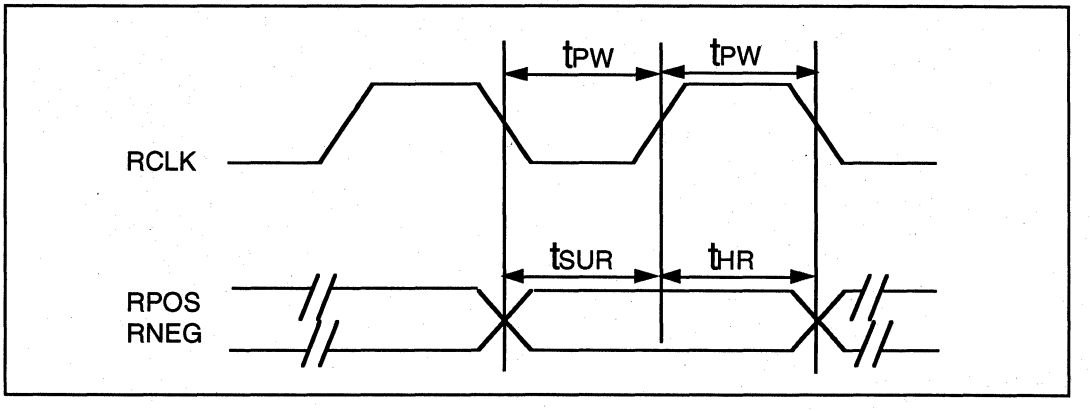
Parameter	Sym	Min	Typ	Max	Units	Test Conditions
Supply current	I_{CC}	-	-	40	mA	
Input high voltage	V_{IH}	2.0	-	-	V	Digital inputs
Input low voltage	V_{IL}	-	-	0.8	V	Digital inputs
Output high voltage	V_{OH}	2.4	-	-	V	I_O=.4mA
Output low voltage	V_{OL}	-	-	0.4	V	I_O=1.6mA
Input leakage current	I_{LL}	-	-	± 10	µA	Digital inputs
Output current	I_O	-	-	1.6	mA	V_O = 0.4 V
Output Rise/Fall time	T_{RF}	-	-	25	ns	15 pF load

Master and Receive Clock Timing Characteristics (See Figure 2)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Master clock frequency	DSX-1	MCLK	-	1.544	-	MHz	
	CEPT	MCLK	-	2.048	-	MHz	
Master clock tolerance		MCLKt	-	±100	-	ppm	
Master clock duty cycle		MCLKd	40	50	60	%	
Receive clock duty cycle		RCLKd	40	50	60	%	
Receive clock pulse width	DSX-1	t_{PW}	270	324	378	ns	
	CEPT	t_{PW}	203	244	285	ns	
RPOS / RNEG to RCLK rising setup time	DSX-1	t_{SUR}	50	270	-	ns	
	CEPT	t_{SUR}	50	203	-	ns	
RCLK rising to RPOS / RNEG hold time	DSX-1	t_{HR}	50	270	-	ns	
	CEPT	t_{HR}	50	203	-	ns	
Rise/fall time - any digital output		t_{RF}	-	-	25	ns	15 pF load

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 2: Clock Timing Diagram



Functional Description

The LXT324 is a fully integrated PCM receiver for both 1.544 MHz (DSX-1) and 2.048 MHz (CEPT) applications. The mode of operation is set by the MCLK frequency and the MODE pin logic level. The LXT324 is a low-power CMOS device which operates from a single +5 V power supply.

Figure 1 is a simplified block diagram of the LXT324. Receiver characteristics are listed in Table 1. The signal is received from the twisted-pair line on each side of a center-grounded transformer. (Positive pulses are received at RTIP and negative pulses are received at RRING.) This differential signal is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (MODE Select = 0) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For CEPT applications (MODE Select = 1) the threshold is set to 50 %. The slicer threshold is maintained through a capacitive storage arrangement and a combination of Refresh and Bleed-off circuitry. This design balance prevents the refresh circuitry from driving the threshold too high, while ensuring that it is maintained over long strings of successive zeros.

The LXT324 is capable of accurately recovering signals with up to 13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of 500 mV. Maximum cable length is 1500 feet of ABAM cable (approximately 6 dB). Regardless of received signal level, the peak detectors are held above a minimum level of 0.15 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections. Recovered clock signals are supplied to the data latch. The recovered data is synchronized with the recovered clock (RCLK), then output at RNEG and RPOS. RPOS and RNEG outputs are valid on the rising edge of RCLK.

Line Interface

The LXT324 interfaces with four twisted-pair lines (one twisted-pair for each receiver) through standard pulse transformers and appropriate resistors. Recommended transformer characteristics are listed in Table 2.

2

Table 1: Receiver Characteristics

Parameter		Sym	Min	Typ[1]	Max	Units
Slicer ratio	DSX-1	SRd	63	70	77	%
	CEPT	SRc	43	50	57	%
Dynamic range		DR	0.50	–	3.6	Vpeak
Undershoot		US	–	–	62	%
Sensitivity below DSX		–	13.6	–	–	dB
(0dB = 2.4V)		–	500	–	–	mV

Table 2: Recommended Transformer Characteristics

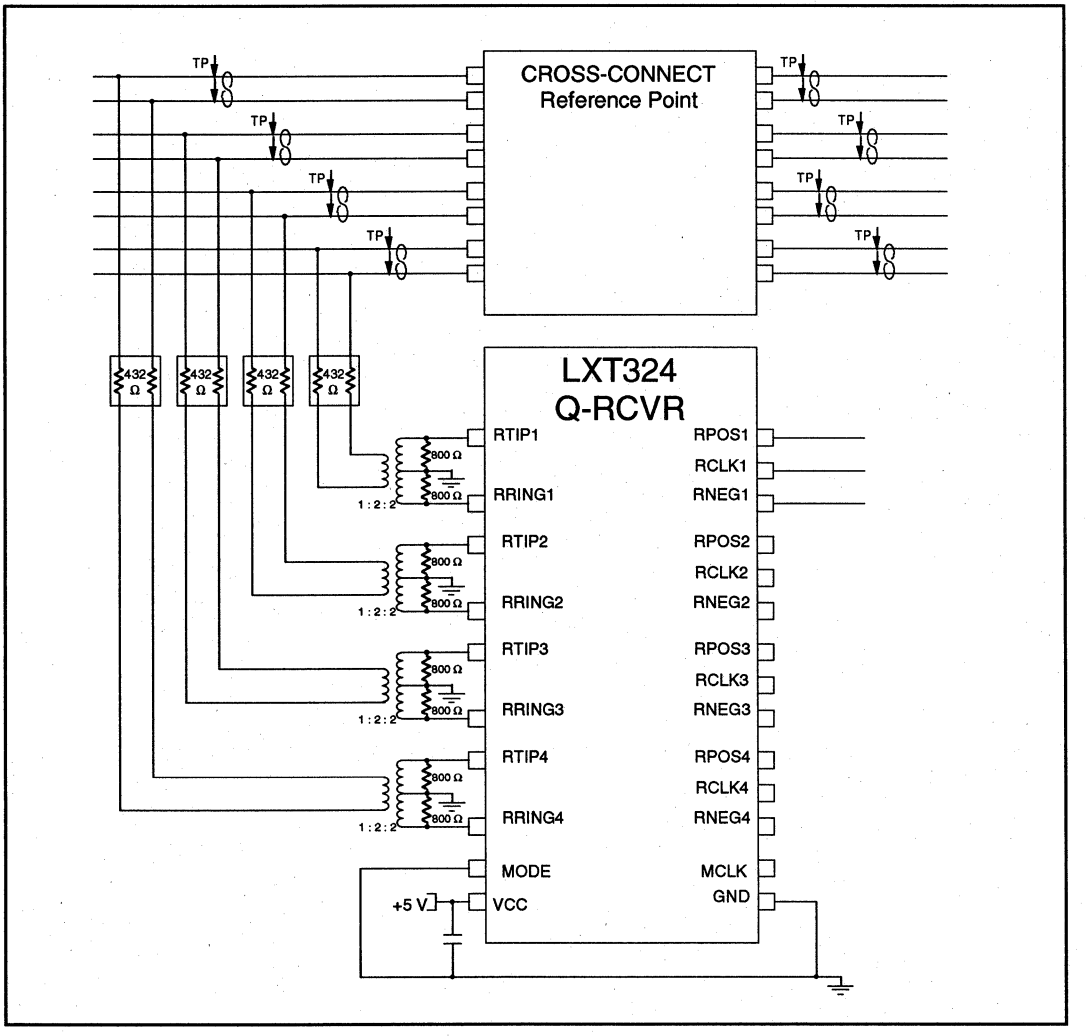
Parameter		1 : 1 : 1	1 : 2 : 2	Units
DC resistance	Primary	1.0 maximum	1.0 maximum	Ω
	Secondary	1.0 maximum	2.0 maximum	Ω
Primary inductance		1.2 typical	0.5 minimum	mH
Leakage inductance		0.5 maximum	1.0 maximum	µH
Interwinding capacitance		25 maximum	40 maximum	pF

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Applications

The LXT324 is compatible with both DSX-1 and CEPT systems. Low +5 V only power consumption simplifies design considerations where multiple receivers are required. The LXT324 is well suited for use in both test equipment and monitor applications. The primary difference in circuit design for these two applications is the input transformer. The typical DSX-1 pulse seen in test equipment applications requires a 1:1:1 transformer at the receiver input. The attenuated pulse seen in monitor applications may require a 1:2:2 transformer to boost the input signal. Figure 3 is a typical 1.544 MHz DSX-1 application. The LXT324 is shown tapped into the Cross Connect frame with 800 Ω resistors across each leg of the center tapped, center grounded 1:2:2 step-up transformer.

Figure 3: Test / Monitor Equipment Application Diagram



LXT325

T1/E1 Integrated Quad Receiver with LOS

General Description

The LXT325 is a fully integrated quad PCM receiver for both North American 1.544 MHz (T1), and European 2.048 MHz (E1) applications. It incorporates four independent receivers in a single 28-pin DIP or PLCC. Each receiver incorporates a Loss Of Signal (LOS) detection circuit and output driver. The operating frequency is pin selectable.

The LXT325 receiver performs data and timing recovery, and uses peak detection and a variable threshold to reduce impulsive noise. LXT325 receiver sensitivity down to 500 mV allows for up to 13.6 dB of attenuation.

The LXT325 is an advanced double-poly, double-metal CMOS device and requires only a single 5-volt power supply.

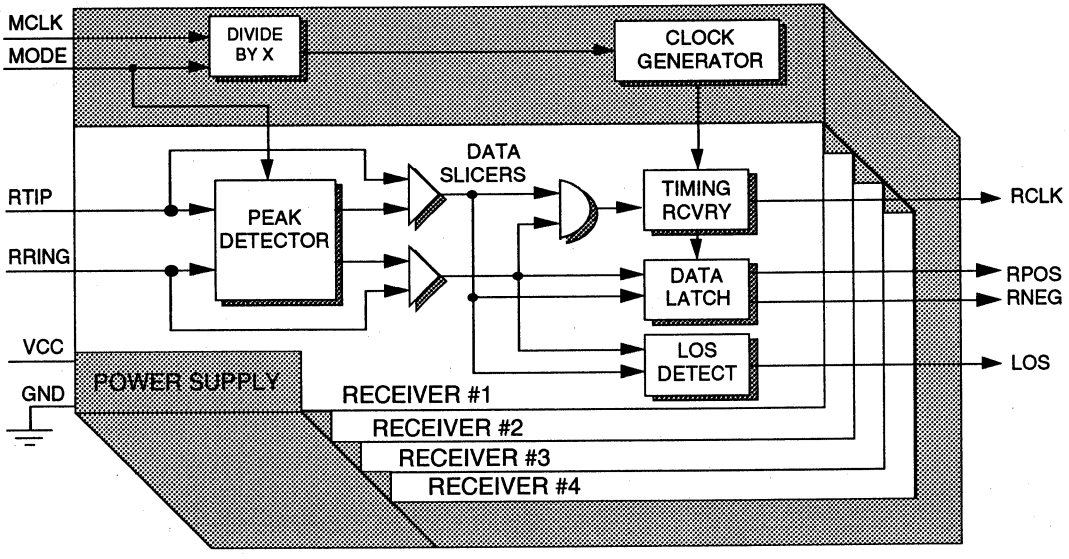
Applications

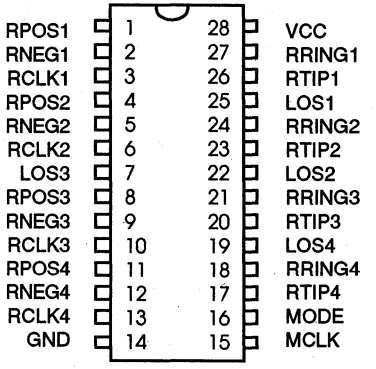
- High-density T1/E1 line cards
- DSX-1/CEPT test equipment
- DSX-1/CEPT line monitoring
- DSX-1/CEPT receive line interface

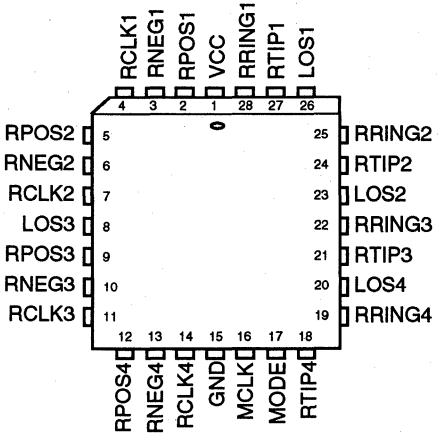
Features

- 4 independent DSX-1/CEPT receivers
- Loss Of Signal (LOS) output for each receiver
- Circuit functions include data and clock recovery
- Single Master Clock input
- Meets or exceeds AT&T PUB 62411 requirements
- Unipolar RPOS and RNEG outputs
- Minimum receive signal of 500 mV
- Selectable slicer levels (DSX-1/CEPT) to provide improved SNR
- Single 5 V only CMOS technology
- Available in 28-pin plastic DIP and PLCC

Figure 1: Block Diagram







Pin Descriptions

Pin # DIP	Pin # PLCC	Sym	I/O	Name	Description
1	2	RPOS1	O	Receiver 1 Positive Data	Receiver 1 data outputs. A signal on RNEG1 corresponds to receipt of a negative pulse on RTIP1 and RRING1. A signal on RPOS1 corresponds to receipt of a positive pulse on RTIP1 and RRING1. RNEG1 and RPOS1 outputs are Non-Return-to-Zero (NRZ). Both outputs are stable and valid on the rising edge of RCLK1.
2	3	RNEG1	O	Receiver 1 Negative Data	
3	4	RCLK1	O	Recovered Clock 1	This is the clock recovered from the signal received at RTIP1 and RRING1.
4	5	RPOS2	O	Receiver 2 Positive and Negative Data and Recovered Clock	These are the data and clock outputs recovered from the signal received at RTIP2 and RRING2.
5	6	RNEG2	O		
6	7	RCLK2	O		
7	8	LOS3	O	Loss of Signal 3	LOS pins go high when the associated receiver detects 175 consecutive spaces. The LOS output returns low when a mark is received.
8	9	RPOS3	O	Receiver 3 Positive and Negative Data and Recovered Clock	These are the data and clock outputs recovered from the signal received at RTIP3 and RRING3.
9	10	RNEG3	O		
10	11	RCLK3	O		
11	12	RPOS4	O	Receiver 4 Positive and Negative Data and Recovered Clock	These are the data and clock outputs recovered from the signal received at RTIP4 and RRING4.
12	13	RNEG4	O		
13	14	RCLK4	O		
14	15	GND	--	Ground	Ground.
15	16	MCLK	I	Master Clock	A 1.544 MHz or 2.048 MHz clock input used to generate internal clocks. Upon loss of signal, the RCLKs are derived from MCLK.

Pin Descriptions continued

Pin # DIP	Pin # PLCC	Sym	I/O	Name	Description
16	17	MODE	I	Mode Select	Setting MODE to logic 1 sets the data slicer thresholds to 50% of the incoming signal (CEPT mode). Setting MODE to logic 0 sets the data slicer thresholds to 70% of the incoming signal (DSX-1 mode). The Mode Select operates independently from the MCLK rate. This allows the 50% slicer ratio to be used with a 1.544 MHz MCLK, for improved sensitivity.
17	18	RTIP4	I	Receiver 4 Tip	The AMI signal received from the fourth twisted-pair line is applied at these pins. A center-tapped, center-grounded transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS4/RNEG4, and RCLK4 pins.
18	19	RRING4	I	Receiver 4 Ring	
19	20	LOS4	O	Loss of Signal	LOS output for receiver 4.
20	21	RTIP3	I	Receiver 3 Tip and Ring	The AMI signal received from the third twisted-pair line is applied to the LXT325 at these pins.
21	22	RRING3	I		
22	23	LOS2	-	Loss of Signal	LOS output for receiver 2.
23	24	RTIP2	I	Receiver 2 Tip and Ring	The AMI signal received from the second twisted-pair line is applied to the LXT325 at these pins.
24	25	RRING2	I		
25	26	LOS1	O	Loss of Signal	LOS output for receiver 1.
26	27	RTIP1	I	Receiver 1 Tip and Ring	The AMI signal received from the first twisted-pair line is applied to the LXT325 at these pins.
27	28	RRING1	I		
28	1	VCC	I	Power Supply	+5 VDC power supply.

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

• Supply voltage	V_{CC}	-0.3V to 6V
• Voltage on any I/O pin[1]	$V_{I/O}$	GND -0.3V to V_{CC} +0.3V
• Current on any I/O pin[2]	$I_{I/O}$	±10 mA
• Package power dissipation	P_D	1 W
• Storage temperature	T_{ST}	-65 °C (min) to 150 °C (max)

[1] Excluding RTIP and RRING which must stay within -6V to RV + 0.3V.
[2] Transient currents of up to 100 mA will not cause SCR latch-up.

Recommended Operating Conditions (Voltages are with respect to ground unless otherwise stated)

Parameter	Sym	Min	Typ	Max	Units
Supply voltage	V_{CC}	4.75	5	5.25	V
Operating Temperature	T_{OP}	-40	-	85	°C

DC Electrical Characteristics (Clocked operation over recommended temperature and power supply ranges.)

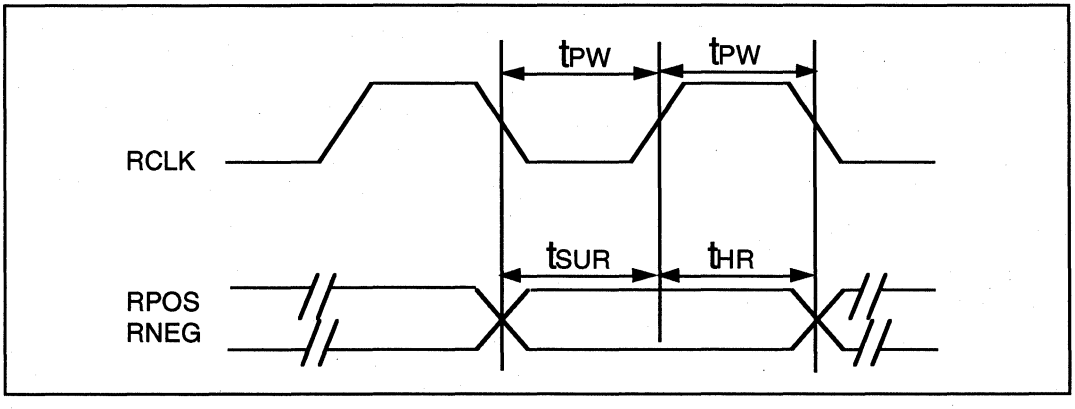
Parameter	Sym	Min	Typ	Max	Units	Test Conditions
Supply current	I_{CC}	-	-	40	mA	
Input high voltage	V_{IH}	2.0	-	-	V	Digital inputs
Input low voltage	V_{IL}	-	-	0.8	V	Digital inputs
Output high voltage	V_{OH}	2.4	-	-	V	I_O=.4mA
Output low voltage	V_{OL}	-	-	0.4	V	I_O=1.6mA
Input leakage current	I_{LL}	-	-	± 10	µA	Digital inputs
Output current	I_O	-	-	1.6	mA	V_O = 0.4 V
Output Rise/Fall time	T_{RF}	-	-	25	ns	15 pF load

Master and Receive Clock Timing Characteristics (See Figure 2)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Master clock frequency	DSX-1	MCLK	-	1.544	-	MHz	
	CEPT	MCLK	-	2.048	-	MHz	
Master clock tolerance		MCLKt	-	±100	-	ppm	
Master clock duty cycle		MCLKd	40	50	60	%	
Receive clock duty cycle		RCLKd	40	50	60	%	
Receive clock pulse width	DSX-1	t_{PW}	270	325	378	ns	
	CEPT	t_{PW}	203	244	285	ns	
RPOS / RNEG to RCLK	DSX-1	t_{SUR}	50	270	-	ns	
rising setup time	CEPT	t_{SUR}	50	203	-	ns	
RCLK rising to RPOS /	DSX-1	t_{HR}	50	270	-	ns	
RNEG hold time	CEPT	t_{HR}	50	203	-	ns	
Rise/fall time - any digital output		t_{RF}	-	-	25	ns	15 pF load

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 2: Clock Timing Diagram



Functional Description

The LXT325 is a fully integrated PCM receiver for both 1.544 MHz (DSX-1) and 2.048 MHz (CEPT) applications. The mode of operation is set by the MCLK frequency and the MODE pin logic level. The LXT325 is a low-power CMOS device which operates from a single +5 V power supply.

Figure 1 is a simplified block diagram of the LXT325. Receiver characteristics are listed in Table 1. The signal is received from the twisted-pair line on each side of a center-grounded transformer. (Positive pulses are received at RTIP and negative pulses are received at RRING.) This differential signal is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (MODE Select = 0) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For CEPT applications (MODE Select = 1) the threshold is set to 50 %. The slicer threshold is maintained through a capacitive storage arrangement and a combination of Refresh and Bleed-off circuitry. This design balance prevents the refresh circuitry from driving the threshold too high, while ensuring that it is maintained over long strings of successive zeros.

The LXT325 is capable of accurately recovering signals with up to 13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of 500 mV. Maximum cable length is 1500 feet of ABAM cable (approximately 6 dB). Regardless of received signal level, the peak detectors are held above a minimum level of 0.15 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections. Recovered clock signals are supplied to the data latch. The recovered data is synchronized with the recovered clock (RCLK), then output at RNEG and RPOS. RPOS and RNEG outputs are valid on the rising edge of RCLK.

Line Interface

The LXT325 interfaces with four twisted-pair lines (one twisted-pair for each receiver) through standard pulse transformers and appropriate resistors. Recommended transformer characteristics are listed in Table 2.

Table 1: Receiver Characteristics

Parameter		Sym	Min	Typ[1]	Max	Units
Slicer ratio	DSX-1	SRd	63	70	77	%
	CEPT	SRc	43	50	57	%
Dynamic range		DR	0.50	–	3.6	Vpeak
Undershoot		US	–	–	62	%
Sensitivity below DSX		–	13.6	–	–	dB
(0dB = 2.4V)		–	500	–	–	mV

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

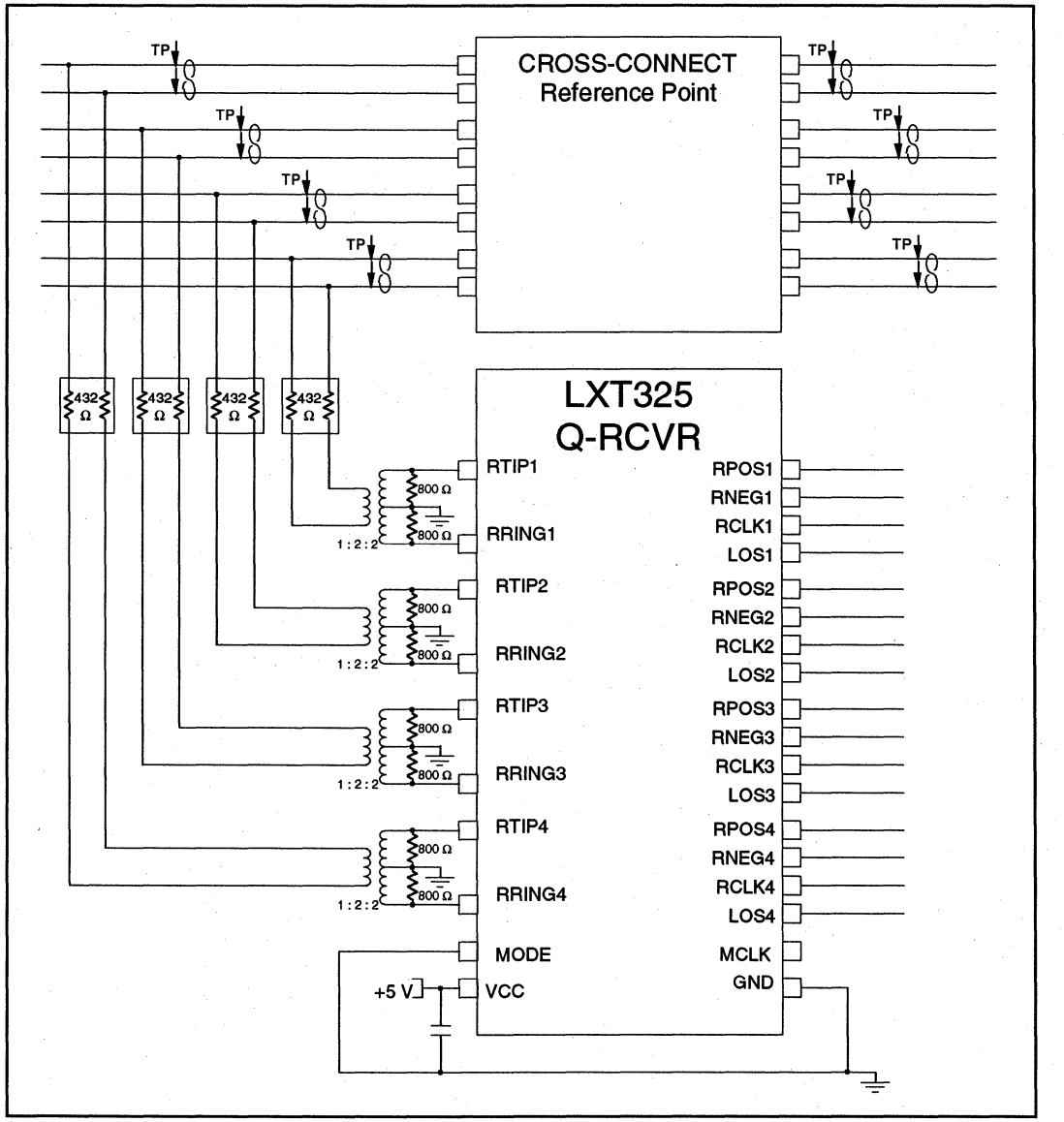
Table 2: Recommended Transformer Characteristics

Parameter		1 : 1 : 1	1 : 2 : 2	Units
DC resistance	Primary	1.0 maximum	1.0 maximum	Ω
	Secondary	1.0 maximum	2.0 maximum	Ω
Primary inductance		1.2 typical	0.5 minimum	mH
Leakage inductance		0.5 maximum	1.0 maximum	µH
Interwinding capacitance		25 maximum	40 maximum	pF

Applications

The LXT325 is compatible with both DSX-1 and CEPT systems. Low +5 V only power consumption simplifies design considerations where multiple receivers are required. The LXT325 is well suited for use in both test equipment and monitor applications. The primary difference in circuit design for these two applications is the input transformer. The typical DSX-1 pulse seen in test equipment applications requires a 1:1:1 transformer at the receiver input. The attenuated pulse seen in monitor applications may require a 1:2:2 transformer to boost the input signal. Figure 3 is a typical 1.544 MHz DSX-1 application. The LXT325 is shown tapped into the Cross Connect frame with 800 Ω resistors across each leg of the center tapped, center grounded 1:2:2 step-up transformer.

Figure 3: Test / Monitor Equipment Application Diagram



LXP600A, LXP602 and LXP604

Low-Jitter Clock Adapters (CLAD)

General Description

The LXP600A, LXP602 and LXP604 Clock Adapters (CLADs) incorporate Level One's patented frequency conversion circuitry. The LXP600A and LXP602 convert a 1.544 MHz input clock to a 2.048 MHz output clock, or vice versa. The LXP604 converts between 1.544 MHz and 4.096 MHz. Each CLAD produces two different high frequency output (HFO) clocks for applications which require a higher-than-baud rate backplane or system clock.

Level One's patented locking method enables the CLAD to perform frequency conversion with no external components, while generating very little jitter on the output clock. The conversion is digitally controlled so the output clock (CLKO) is as accurate as the input clock (CLKI), and the two clocks are frequency locked together. When an input frame sync pulse ($\overline{FSI}$) is provided, the CLAD also phase locks CLKI and CLKO together, and locks the output frame sync pulse ($\overline{FSO}$) to $\overline{FSI}$.

Features

- Generates a 1.544 MHz clock and its frame sync from a 2.048 MHz or 4.096 MHz clock and its frame sync, or vice versa
- Low output jitter meets AT&T Publication 62411 for 1.544 MHz, and CCITT Recommendation G.823 for 2.048 MHz
- Digital control of frequency conversion process
- No external components
- Available in 8-pin plastic DIP
- Pin-selectable operation mode
- Advanced CMOS device requires only a single +5V power supply

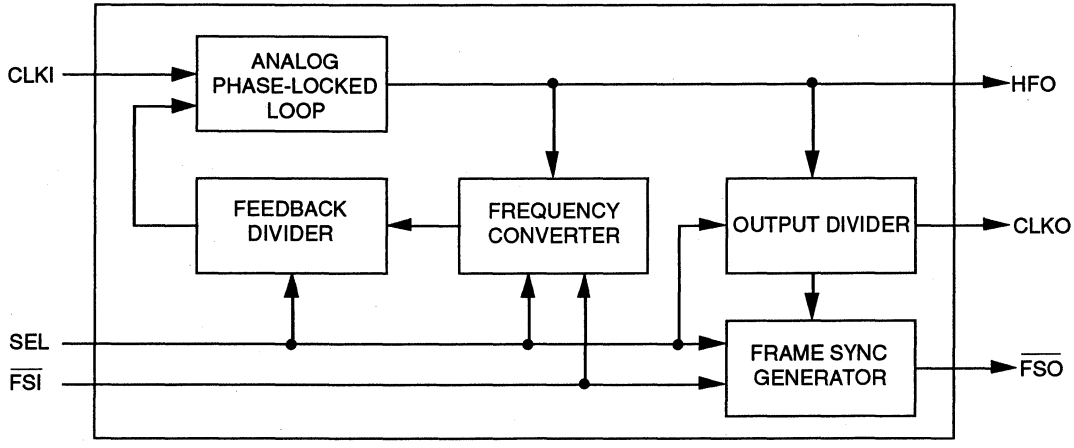
Frequency Conversions

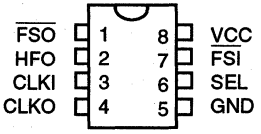
CLAD	CLKI	CLKO	HFO
LXP600A	1.544 2.048	2.048 1.544	6.144 6.176
LXP602	1.544 2.048	2.048 1.544	8.192 6.176
LXP604	1.544 4.096	4.096 1.544	8.192 6.176

Applications

- Internal timing system for Channel Banks, Digital Loop Carriers, Multiplexers, Internal Timing Generators, PBX, etc.
- Conversion between 2.048 MHz or 4.096 MHz backplane rates and 1.544 MHz T1 clock rate.
- Conversion between North American and European standards (T1 / E1 Converter).

Figure 1: LXP600A/602/604 Block Diagram





8-pin DIP

Table 1: Pin Descriptions

Pin #	Sym	I/O	Name	Description
1	$\overline{FSO}$	O	Frame Sync Output	Frame synchronization output at 8 kHz. $\overline{FSO}$ is synched to CLKO and to $\overline{FSI}$ (if $\overline{FSI}$ is provided.)
2	HFO	O	High Frequency Output	HFO is used to derive CLKO. HFO can also clock external devices. HFO is always a multiple of CLKO (CLKO x 2, x3, or x4). Actual frequencies are determined by device, CLKI and CLKO frequencies and Mode Select (SEL) input, as listed in Table 6.
3	CLKI	I	Clock Input	Input clock (1.544, 2.048 or 4.096 MHz) to be converted.
4	CLKO	O	Clock Output	Output clock (1.544, 2.048 or 4.096 MHz) derived from CLKI.
5	GND	-	Ground	Ground.
6	SEL	I	Mode Select	Controls frequency conversion as listed in Table 6. When SEL = 1, higher frequency CLKI (2.048 for LXP600A and LXP602, or 4.096 MHz for LXP604) is converted to 1.544 MHz CLKO. When SEL = 0, 1.544 MHz CLKI is converted to higher frequency CLKO (2.048 for LXP600A and LXP602, or 4.096 MHz for LXP604).
7	$\overline{FSI}$	I	Frame Sync Input	8 kHz frame synchronization pulse. Tie high or low if not used.
8	VCC	-	Power Supply	+5 V power supply input.

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

• Supply Voltage	V_{cc}	-0.3 V to 7 V
• Voltage on any I/O pin	V_{io}	Minimum = GND - 0.3 V Maximum = V_{cc} + 0.3 V
• Current on any I/O pin[1]	I_{io}	±10 mA
• Package power dissipation	P_d	340 mW
• Storage temperature	T_{ST}	-65 °C to +150 °C

[1]Transient currents of up to 100 mA will not cause SCR latch-up.

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Table 2: Operating Conditions (Voltages are with respect to ground unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Supply voltage	V_{CC}	4.75	5.0	5.25	V	
Supply current	I_{CC}	-	-	8	mA	No TTL loading
	I_{CC}	-	-	14	mA	Full TTL loading
Operating temperature	T_{OP}	-40	-	85	°C	

Table 3: Digital Characteristics

Parameter	Symbol	Min	Max	Units
Input low voltage	V_{IL}	-	0.8	V
Input high voltage	V_{IH}	2.0	-	V
Output low voltage (I_{OL} = + 1.6 mA)	V_{OL}	-	0.4	V
Output low voltage (I_{OL} < + 10 µA)	V_{OL}	-	0.2	V
Output high voltage (I_{OH} = - 0.4 mA)	V_{OH}	2.4	-	V
Output high voltage (I_{OH} < - 10 µA)	V_{OH}	4.5	-	V
Input leakage current	I_{LL}	-10	10	µA

Table 4: Timing Values (see Figure 2)

Parameter	Symbol	Min	Max	Units
Capture range on CLKI	-	±10000	-	ppm
Lock range on CLKI	-	±10000	-	ppm
Input clock duty cycle	-	35	65	%
Rise/fall time on CLKI, $\overline{FSI}$	Trf	-	40	ns
Rise/fall time on CLKO, $\overline{FSO}$, HFO with a 25 pF load	Trf	-	40	ns

Figure 2: Rise and Fall Times

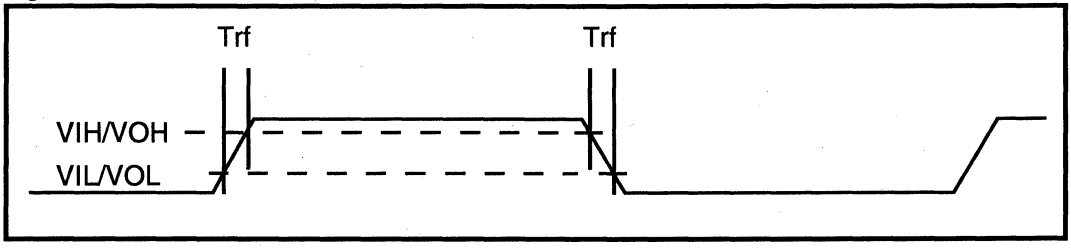


Table 5: Timing Values (see Figures 3 through 7)

Parameter	Symbol	Min	Typ[1]	Max	Units
$\overline{FSI}$ setup time from CLKI rising	Tsui	46	-	-	ns
$\overline{FSI}$/CKLI hold time	Thi	30	-	-	ns
$\overline{FSI}$ pulse width (low)	Twi	76	-	TCLKI[2]	ns
CLKO delay from CLKI	TdC	-15	0	+15	ns
CLKO duty cycle	Cdc	49	-	51	%
$\overline{FSO}$ delay from HFO	TdF	-5	-	30	ns
$\overline{FSO}$ pulse width (low)	Two	-	-	TCLKO[3]	ns
CLKO delay from HFO	TdH	-15	-	+15	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
[2] TCLKI is the period of CLKI.
[3] TCLKO is the period of CLKO.

Figure 3: LXP600A and LXP602 High to Low Frequency Conversion Frame Sync Alignment

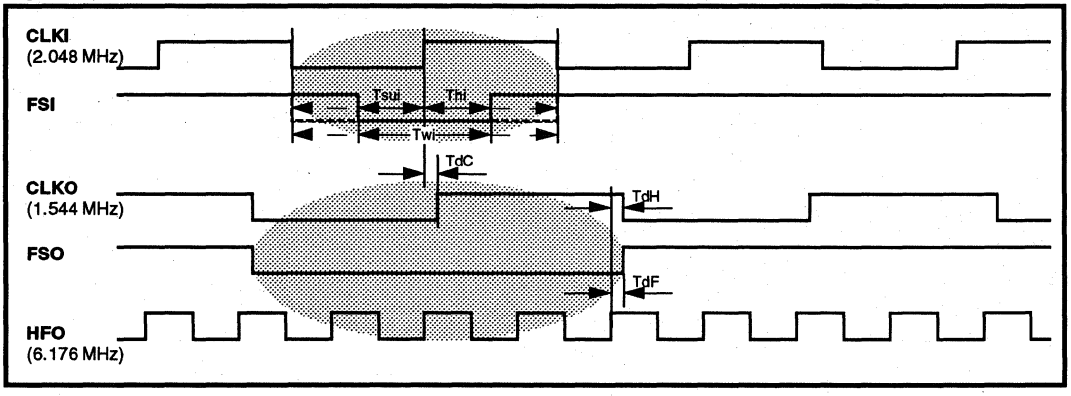


Figure 4: LXP604 High to Low Frequency Conversion Frame Sync Alignment

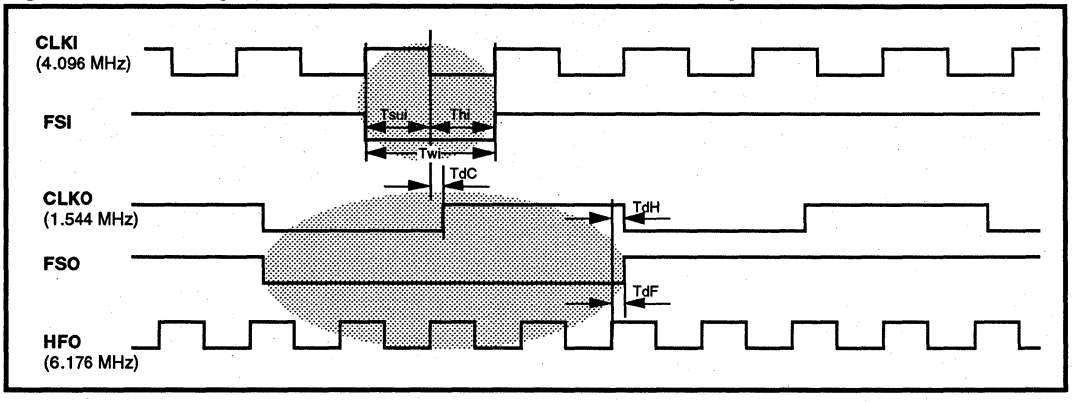


Figure 5: LXP600A Low to High Frequency Conversion Frame Sync Alignment

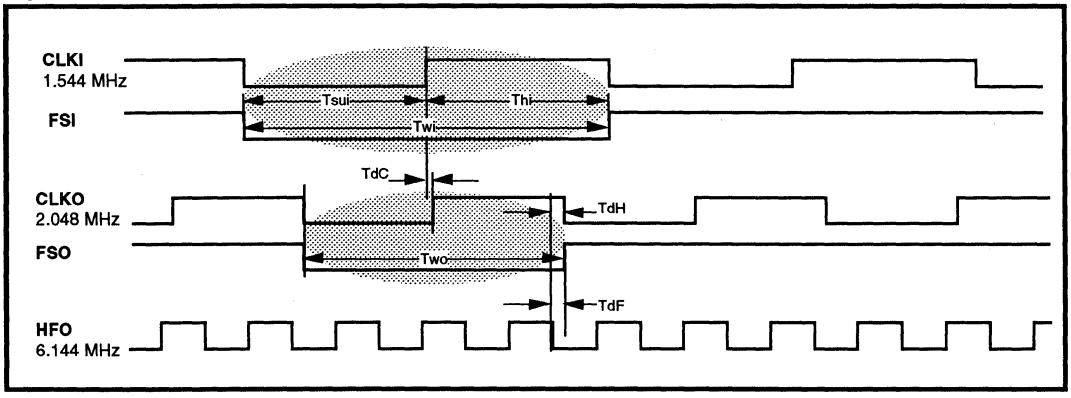


Figure 6: LXP602 Low to High Frequency Conversion Frame Sync Alignment

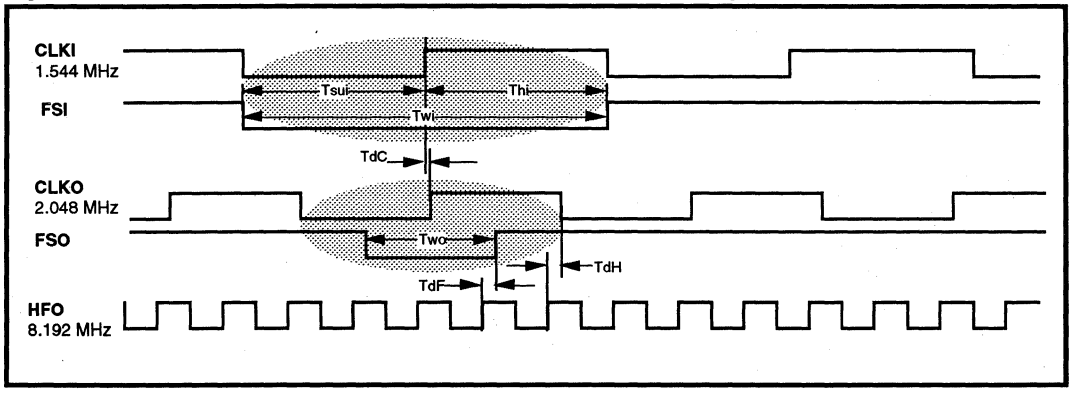
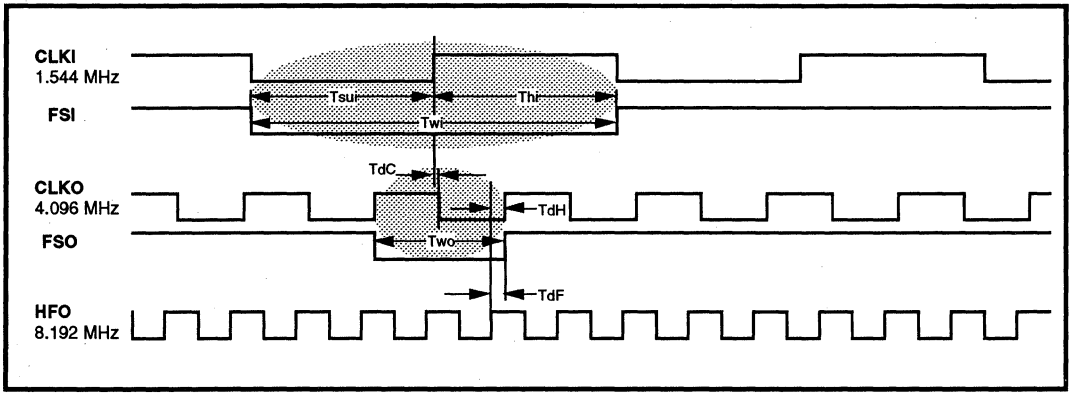


Figure 7: LXP604 Low to High Frequency Conversion Frame Sync Alignment



Functional Description

The CLADs convert an input clock (CLKI) at a particular frequency to an output clock (CLKO) at a different frequency. They also produces a frame sync output (FSO) and a high frequency output (HFO) clock. The HFO is a multiple (2x, 3x, or 4x) of CLKO. The HFO and CLKI/CLKO conversion frequencies are different for each device, and controlled by the Mode Select input as listed in Table 6.

The LXP600A and LXP602 convert between 1.544 MHz and 2.048 MHz. When converting from 2.048 MHz to 1.544 MHz, both CLADs produce a 6.176 MHz HFO. However, when converting from 1.544 MHz to 2.048 MHz, the LXP600A produces a 6.144 MHz HFO and the LXP602 produces an 8.192 MHz HFO.

The LXP604 converts between 1.544 MHz and 4.096 MHz. When converting from 4.096 to 1.544 MHz the LXP604 HFO is 6.176. When converting from 1.544 MHz to 4.096 MHz, the LXP604 produces an 8.192 MHz HFO.

The Mode Select (SEL) input controls whether the device converts to a higher or lower frequency as described below:

- 2.048 or 4.096 to 1.544 MHz: To produce a 1.544 MHz output clock from a 2.048 MHz or 4.096 MHz input clock, SEL must be set high. In this mode HFO = 6.176 MHz for all CLADs.

- 1.544 to 2.048 MHz or 4.096 MHz: To produce a 2.048 MHz or 4.096 MHz output clock from a 1.544 MHz input clock, SEL must be set low. In this mode the LXP600A HFO = 6.144 MHz, and the LXP602 and LXP604 HFO = 8.192 MHz.

In both frequency modes, CLKO is frequency locked to CLKI. When $\overline{FSI}$ is applied, CLKO and CLKI are also phase locked with $\overline{FSO}$ and $\overline{FSI}$ synchronized as shown in Figures 3 through 7.

When $\overline{FSI}$ is first asserted, the CLKI and CLKO rising edges will be aligned within a maximum of 500 ms.

If $\overline{FSI}$ is not provided, pin 7 should be tied high or low. CLKO and $\overline{FSO}$ are still generated with the CLKO frequency locked to CLKI.

Output Jitter

Refer to Table 7. The CLAD output jitter meets the following specifications:

- 2.048 MHz or 4.096 MHz to 1.544 MHz: In this mode of operation, the CLADs meet the output jitter requirements of AT&T Publication 62411. When there is no jitter on input clock CLKI, the maximum jitter on CLKO is 0.020 UI pp with no bandlimiting, 0.010 UI pp over the range of 10 Hz to 40 kHz, and 0.012 UI pp in the 8 - 40 kHz band.

- 1.544 MHz to 2.048 MHz or 4.096 MHz: In this mode of operation, the CLADs meet the output jitter requirements of CCITT Recommendation G.823. When there is no jitter on input clock CLKI, the maximum jitter on CLKO is 0.035 UI pp over the range of 20 Hz to 100 kHz, and 0.025 UI pp in the 18 - 100 kHz band.

Table 6: CLAD Frequency Conversions

CLAD	CLKI	CLKO	HFO	SEL
LXP600A	1.544	2.048	6.144	0
	2.048	1.544	6.176	1
LXP602	1.544	2.048	8.192	0
	2.048	1.544	6.176	1
LXP604	1.544	4.096	8.192	0
	4.096	1.544	6.176	1

Table 7: Output Jitter Specifications

Parameter	Sym	Frequency	Spec[1]	Typ[2]	Max	Units	Test Conditions
Output Jitter on CLKO	Tj1	No Bandlimiting	0.050	0.010	0.020	UI pp	CLKI = 2.048 or 4.096 MHz
CLKO = 1.544 MHz		10 Hz to 40 kHz	0.025	0.005	0.010	UI pp	JI = 0
(All CLADs)		8 kHz to 40 kHz	0.025	0.006	0.012	UI pp	$\overline{FSI}$ applied
Output Jitter on CLKO	Tj2	20 Hz to 100 kHz	1.500	0.025	0.035	UI pp	CLKI = 1.544 MHz,
CLKO = 2.048 MHz							JI = 0
(LXP600A and 602 Only)		18 kHz to 100 kHz	0.200	0.015	0.025	UI pp	$\overline{FSI}$ applied

[1] Specifications from AT&T Publication 62411 and CCITT Recommendations G.823 (for 1.544 MHz and 2.048 MHz, respectively).

[2] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Jitter Transfer

The CLADs are sensitive to jitter on the input clock in certain frequency bands. The jitter transfer curve is determined by the frequency and amplitude of the input jitter. Figures 8 and 9 show nominal jitter transfer measured in nanoseconds. These figures graph output jitter (less intrinsic jitter) divided by input jitter (0.25 UI). Jitter transfer from a 2.048 MHz CLKI to a 1.544 MHz CLKO is shown in Figure 8. In this mode, jitter in the critical 8 kHz band is slightly attenuated while jitter in the 18 - 70 kHz band is transferred with a small net gain. Jitter transfer from a 1.544 MHz CLKI to a 2.048 MHz CLKO is shown in Figure 9. In both modes, with an input jitter level of 0.25 UI, jitter transfer is held below a net gain of 1.110.

(Jitter transfer varies with input jitter. Performance in a specific application should be verified in the actual circuit.)

Figure 8: Nominal Jitter Transfer - 2.048 MHz CLKI to 1.544 MHz CLKO (Input Jitter = 0.25 UI)

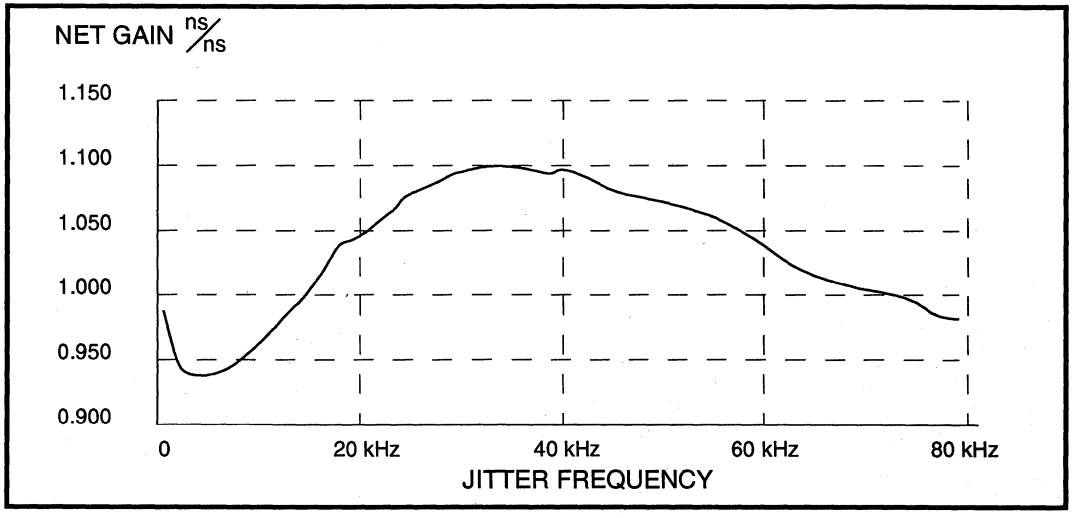
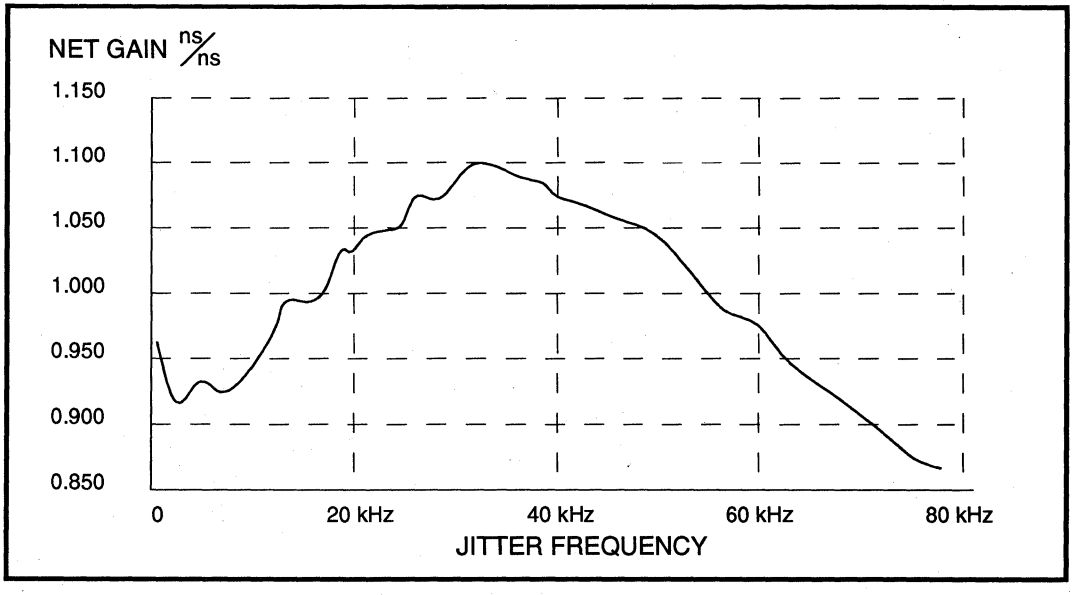


Figure 9: Nominal Jitter Transfer - 1.544 MHz CLKI to 2.048 MHz CLKO (Input Jitter = 0.25 UI)



Design Considerations

Power-up

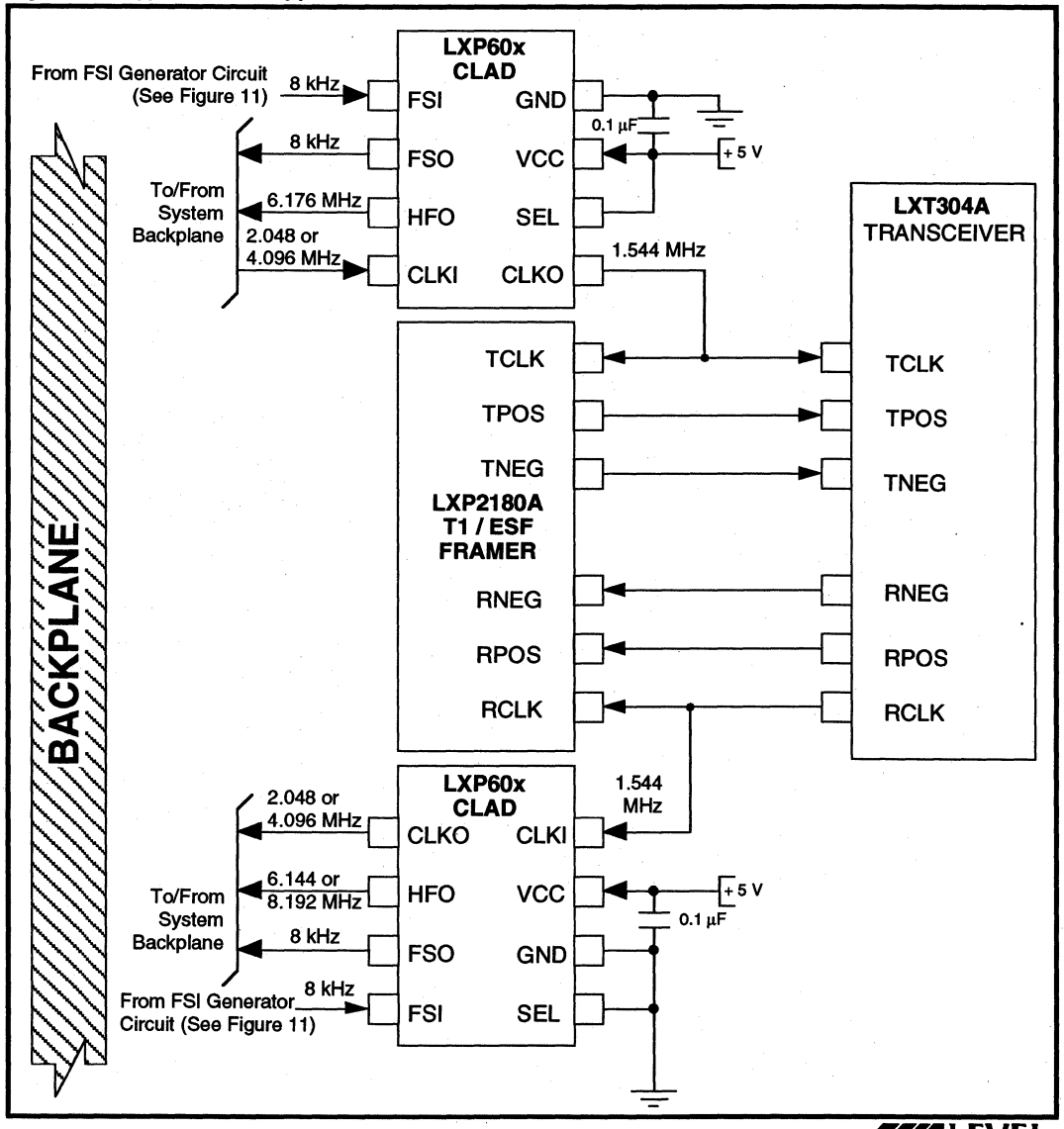
Standard CMOS device precautions apply to the CLAD. Inputs must be applied either simultaneously with or after the power supply VCC. CLAD input signals include CLKI, FSI and SEL.

The CLAD internal circuitry takes a maximum of 200 ms to stabilize. There is an additional delay of 500 ms maximum for CLKO to be phase-locked to the incoming clock CLKI during frame synchronization FSI.

Power Supply Decoupling and Filtering

The CLAD are designed to meet AT&T Publication 62411 specifications for jitter in the range from 10 Hz to 100 kHz. Proper power supply decoupling is critical for meeting these specifications. As shown in Figure 10, a typical application with a pair of CLADs for backplane frequency conversion, a standard 0.1µF bypass capacitor is recommended.

Figure 10: Typical CLAD Application Circuit



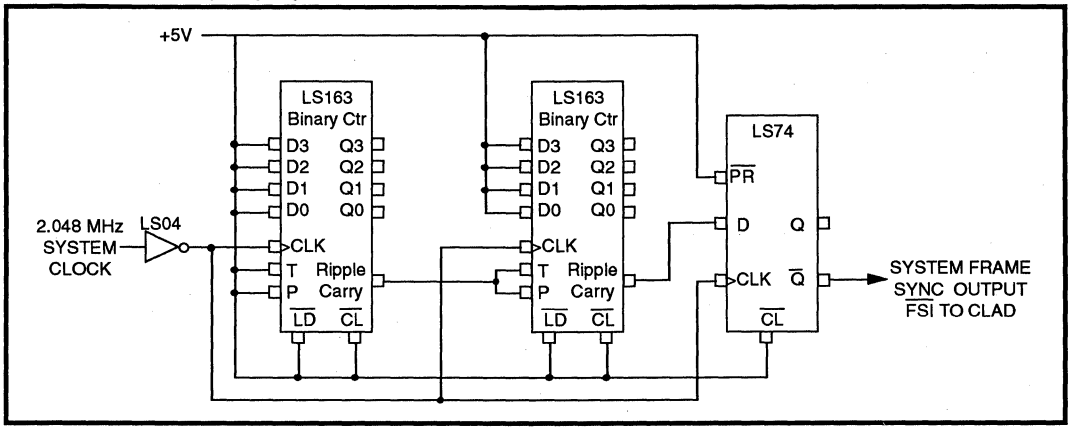
The CLADs are monolithic silicon devices which incorporates both analog and digital circuits. CLAD application circuit design may require closer attention to power supply filtering and bypassing than required for strictly digital devices.

Switching power supplies which operate below 100 kHz may produce noise spikes which can affect the analog sections of the CLAD. These spikes should be filtered with an RC network at the CLAD VCC pin.

Frame Sync Generation

A frame sync pulse is required to synchronize the input and output clocks. If a frame sync pulse is not provided on the backplane, one can be generated from the existing 2.048 MHz backplane clock. A typical FSI generation circuit is shown in Figure 11.

Figure 11: Frame Sync (FSI) Generation Circuit



NOTES:

LXP610

Low-Jitter Multi-Rate Clock Adapter (CLAD)

General Description

The LXP610 Multi-Rate Clock Adapter (CLAD) offers pin-selectable frequency conversion between T1 and E1 rates as well as 8 additional rates from 1.544 MHz to 8.192 MHz. The output clock is frequency locked to the input clock. When an input frame sync pulse is provided, the CLAD phase locks the input and output clocks together, and locks the 8 kHz output frame sync pulse to the input frame sync pulse. The frame sync polarity is also pin selectable.

Five different high frequency output clocks are available for applications which require a higher-than-baud rate backplane or system clock. The high frequency output (HFO) clock varies with the input clock frequency.

Level One's patented locking method enables the CLAD to perform frequency conversion with no external components, while generating very little jitter on the output clock. The conversion is digitally controlled so the output clock is as accurate as the input clock.

The CLAD is an advanced CMOS device. It requires only a single +5 V power supply.

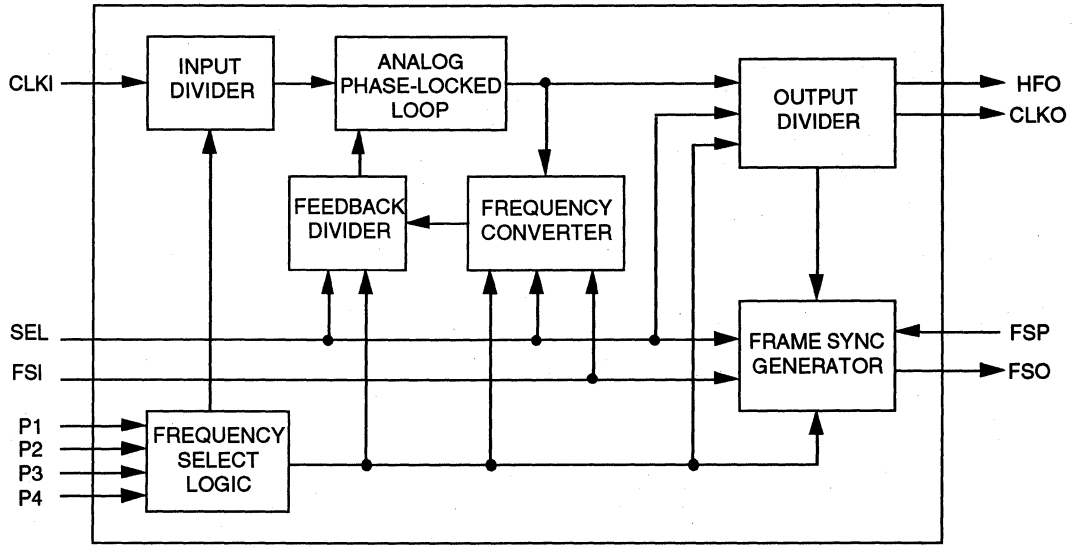
Features

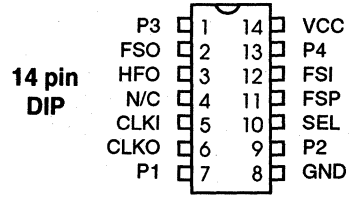
- Translates between 10 different frequencies. Generates basic and high frequency output clocks and frame sync from an input clock and its frame sync.
- High Frequency Output clock for higher-than-baud rate backplane systems
- Low output jitter meets AT&T Publication 62411 for 1.544 MHz, and CCITT Recommendation G.823 for 2.048 MHz
- Digital control of frequency conversion process
- No external components
- Pin-selectable operation mode
- Low-power 5V only CMOS in 14-pin plastic DIP or 28-pin PLCC

Applications

- Internal timing system for Channel Banks, Digital Loop Carriers, Multiplexers, Internal Timing Generators, etc.
- Conversion between T1/E1 clock rates and higher frequency backplane rates (T1/E1 converter)
- Special backplane interfaces (e.g. NTI 2.56 MHz)

Figure 1: CLAD Block Diagram





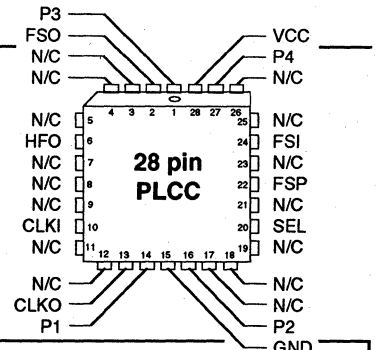


Table 1: Pin Descriptions

Pin # DIP	Pin # PLCC	Sym	I/O	Name	Description
1	1	P3	I	Program Pin 3	Program pins control frequency conversion and FSO pulse width in conjunction with the SEL pin as listed in Table 2.
7	14	P1	I	Program Pin 1	
9	16	P2	I	Program Pin 2	
13	27	P4	I	Program Pin 4	
2	2	FSO	O	Frame Sync Output	Frame synchronization output at 8 kHz. FSO is synched to CLKO and to FSI (if FSI is provided.) Active low unless FSP = 1.
3	6	HFO	O	High Frequency Output	A high frequency output which can be used to clock external devices. HFO outputs are determined in accordance with Table 2.
5	10	CLKI	I	Clock Input	Primary rate clock to be converted.
6	13	CLKO	O	Clock Output	Primary rate clock derived from CLKI.
8	15	GND	-	Ground	Ground.
10	20	SEL	I	Mode Select	Controls frequency conversion and FSO pulse width in conjunction with Program pins 1-4, as listed in Table 2.
11	22	FSP	I	Frame Sync Polarity	When high, causes FSI and FSO to be active high pulses.
12	24	FSI	I	Frame Sync Input	Frame synchronization pulse (8 kHz or any subrate multiple). Active low when FSP = 0. Active high when FSP = 1.
14	28	VCC	I	Power Supply Input	+5 V power supply input.

NOTE: The following pins are not connected (N/C): DIP pin 4 and PLCC pins 3, 4, 5, 7, 8, 9, 11, 12, 17, 18, 19, 21, 23, 25 and 26.

Table 2: Program Pin Functions

Mode Select				SEL = 0				SEL = 1			
P4	P3	P2	P1	CLKI	CLKO	HFO	FSO	CLKI	CLKO	HFO	FSO
0	0	0	0	1.544	2.048	6.144	Long (L)	2.048	3.088	6.176	L
0	0	0	1	3.088	2.048	8.192	Short (S)	2.048	3.088	6.176	L
0	0	1	0	1.544	2.048	6.144	L	2.048	1.544	6.176	L
0	0	1	1	1.544	2.048	8.192	S	2.048	1.544	6.176	L
0	1	0	0	1.544	2.560	7.680	L	2.560	1.544	7.720	L
0	1	0	1	6.176	4.096	8.192	L	8.192	3.088	6.176	L
0	1	1	0	1.544	2.560	7.680	L	2.560	1.544	7.720	L
0	1	1	1	6.176	2.048	8.192	S	8.192	1.544	6.176	L
1	0	0	0	3.088	2.048	6.144	L	2.048	3.088	6.176	L
1	0	0	1	3.088	4.096	8.192	L	4.096	3.088	6.176	L
1	0	1	0	3.088	2.048	6.144	L	2.048	3.088	6.176	L
1	0	1	1	1.544	4.096	8.192	L	4.096	1.544	6.176	L
1	1	0	0	6.176	2.560	7.680	L	2.560	1.544	7.720	L
1	1	0	1	6.176	4.096	8.192	L	8.192	3.088	6.176	L
1	1	1	0	6.176	2.560	7.680	L	2.560	1.544	7.720	L
1	1	1	1	6.176	4.096	8.192	L	8.192	1.544	6.176	L

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

• Supply Voltage	V_{CC}	-0.3 V to 7 V
• Voltage on any I/O pin	$V_{I/O}$	Minimum = GND - 0.3 V Maximum = V_{CC} + 0.3 V
• Current on any I/O pin[1]	$I_{I/O}$	±10 mA
• Package power dissipation	P_D	340 mW
• Storage temperature	T_{ST}	-65 °C to +150 °C

Table 3: Operating Conditions/Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Supply voltage	V_{CC}	4.75	5.0	5.25	V	
Supply current	I_{CC}	-	-	8	mA	No TTL loading
	I_{CC}	-	-	14	mA	Full TTL loading
Operating temperature	T_{OP}	-40	-	85	°C	

[1] Transient currents of up to 100 mA will not cause SCR latch-up.

Table 4: Digital Characteristics

Parameter	Symbol	Min	Max	Units
Input low voltage	V_{IL}	-	0.8	V
Input high voltage	V_{IH}	2.0	-	V
Output low voltage (I_{OL} = + 1.6 mA)	V_{OL}	-	0.4	V
Output low voltage (I_{OL} < + 10 µA)	V_{OL}	-	0.2	V
Output high voltage (I_{OH} = - 0.4 mA)	V_{OH}	2.4	-	V
Output high voltage (I_{OH} < - 10 µA)	V_{OH}	4.5	-	V
Input leakage current	I_{LL}	-10	10	µA

Table 5: Timing Values (see Figure 2)

Parameter	Symbol	Min	Max	Units
Capture range on CLKI	-	±10000	-	ppm
Lock range on CLKI	-	±10000	-	ppm
Input clock duty cycle	-	35	65	%
Rise/fall time on CLKI, FSI	Trf	-	40	ns
Rise/fall time on CLKO, FSO, HFO with a 25 pF load	Trf	-	40	ns

Figure 2: Rise and Fall Times

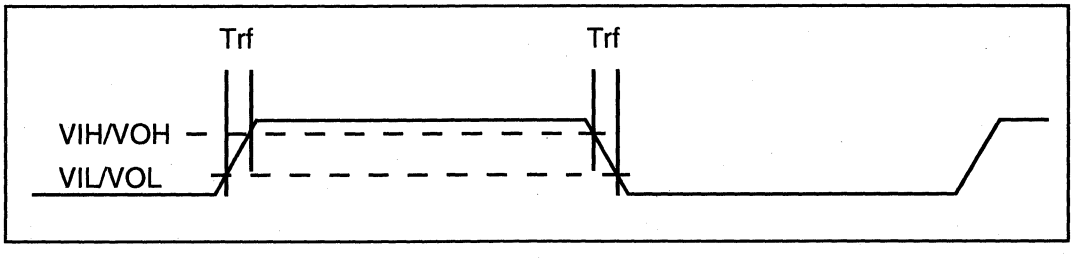


Table 6: Timing Values (see Figures 3 through 7)

Parameter	Symbol	Min	Typ	Max	Units
FSI setup time from CLKI rising	Tsui	46	-	-	ns
FSI/CKLI hold time	Thi	30	-	-	ns
FSI pulse width	Twi	76	-	TCLKI[1]	ns
CLKO delay from CLKI	TdC	-15	0	+15	ns
CLKO duty cycle	Cdc	49	-	51	%
FSO delay from HFO	TdF	-5	-	30	ns
FSO pulse width	Two	-	-	TCLKO[2]	ns
CLKO delay from HFO	TdH	-15	-	15	ns

[1] TCLKI is the period of CLKI.
[2] TCLKO is the period of CLKO.

Figure 3: Timing Relationships - FSI / CLKI to CLKO / FSO and HFO

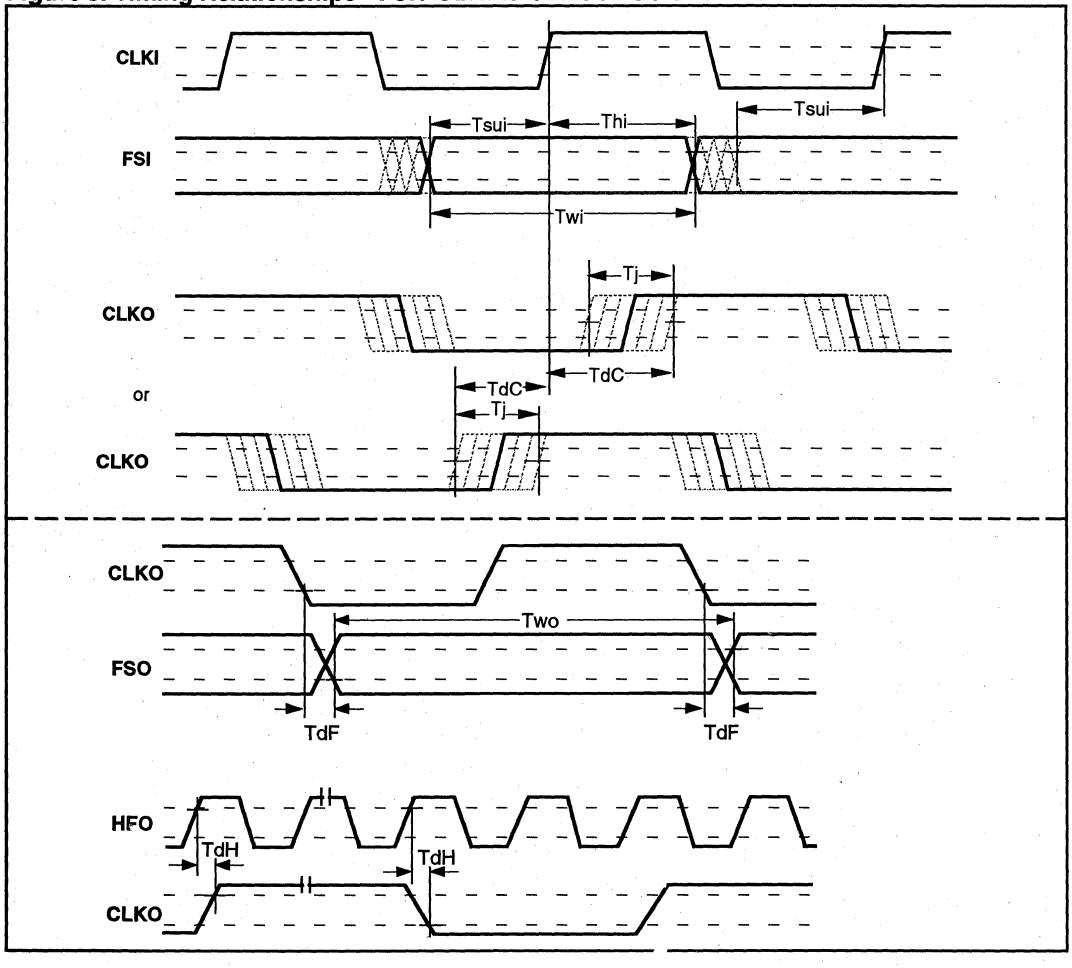


Figure 4: Output Frame Sync Alignment when HFO = 2 x CLKO

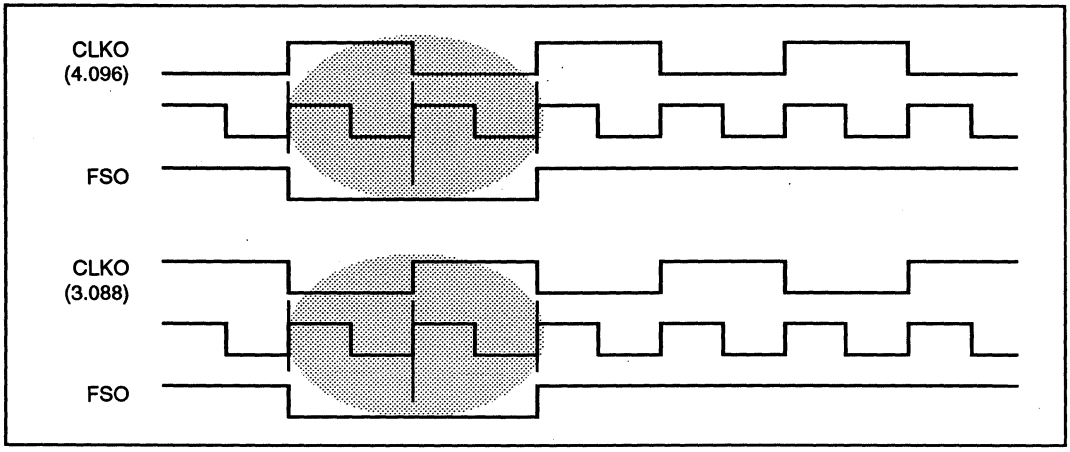


Figure 5: Output Frame Sync Alignment when HFO = 3 x CLKO

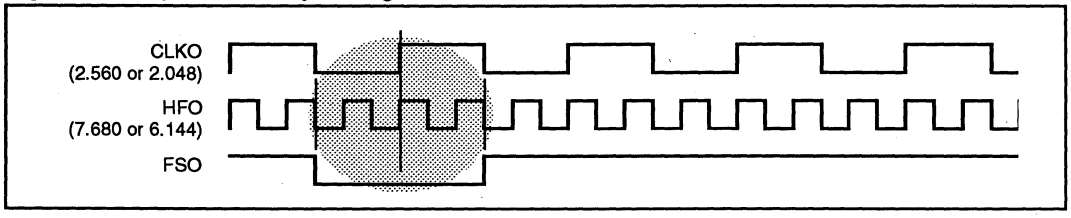


Figure 6: Output Frame Sync Alignment when HFO = 4 x CLKO

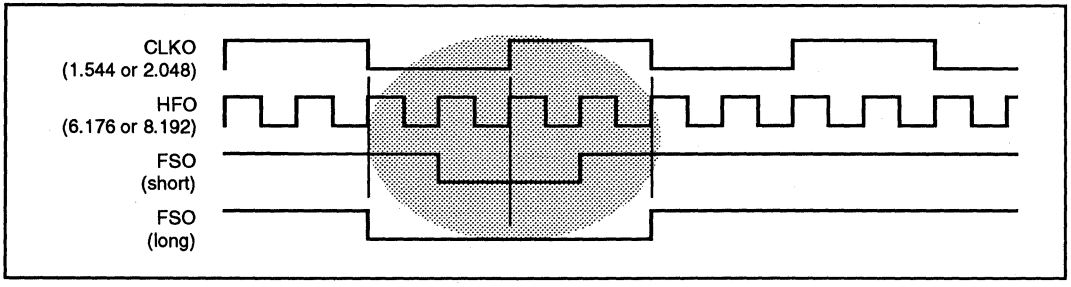
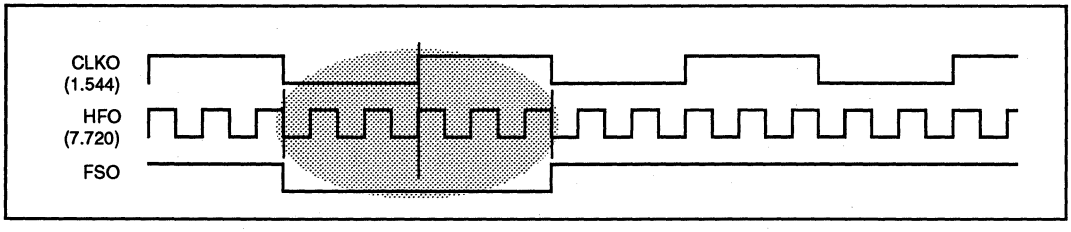


Figure 7: Output Frame Sync Alignment when HFO = 5 x CLKO



Functional Description

The CLAD converts an input clock (CLKI) at a particular frequency to an output clock (CLKO) at a different frequency. It also produces a frame sync output (FSO) and a high frequency output clock (HFO). The HFO frequency is a multiple (2x, 3x, 4x, or 5x) of CLKO. The specific frequencies are determined by the Mode Select (SEL) and Program (P1 - P4) inputs. Table 7 lists the CLKO and HFO frequencies available with a given input CLKI. (Table 2, page 2, lists the same data, keyed to Program Pin settings.) Figures 4 through 7 show output frame sync alignments.

CLKO is always frequency-locked to CLKI. When a frame sync input (FSI) is supplied, CLKI and CLKO are also phase-locked. The CLAD accepts FSI pulses at 8 kHz, or at any sub-rate multiple (ie., 1, 2 or 4 kHz). The frame sync output (FSO) pulse is synchronized to the FSI pulse.

When an 8 kHz FSI is first asserted, the CLKI and CLKO rising edges will be aligned within a maximum of 500 ms. For other FSI rates, the alignment period is correspondingly lengthened. For example, at 4 kHz, the FSI/FSO alignment is completed within a maximum of one second.

If an input frame sync pulse is not provided, the FSI pin should be tied high or low. CLKO and FSO are still generated with the CLKO frequency locked to CLKI.

Table 7: Input to Output Frequency Conversion Options

CLKI	CLKO	HFO	FSO	P4	P3	P2	P1	SEL
1.544	2.048	6.144	Long (L)	0	0	X	0	0
1.544	2.048	8.192	Short (S)	0	0	1	1	0
1.544	2.560	7.680	L	0	1	X	0	0
1.544	4.096	8.192	L	1	0	1	1	0
2.048	1.544	6.176	L	0	0	1	X	1
2.048	3.088	6.176	L	0	0	0	X	1
2.048	3.088	6.176	L	1	0	X	0	1
2.560	1.544	7.720	L	X	1	X	0	1
3.088	2.048	6.144	L	1	0	X	0	0
3.088	2.048	8.192	S	0	0	0	1	0
3.088	4.096	8.192	L	1	0	0	1	0
4.096	1.544	6.176	L	1	0	1	1	1
4.096	3.088	6.176	L	1	0	0	1	1
6.176	2.048	8.192	S	0	1	1	1	0
6.176	2.560	7.680	L	1	1	X	0	0
6.176	4.096	8.192	L	0	1	0	1	0
6.176	4.096	8.192	L	1	1	X	1	0
8.192	1.544	6.176	L	X	1	1	1	1
8.192	3.088	6.176	L	X	1	0	1	1

Output Jitter

Refer to Table 8. The CLAD output jitter meets the following specifications:

- 2.048 MHz or 4.096 MHz to 1.544 MHz: In this mode of operation, the CLAD meets the output jitter requirements of AT&T Publication 62411. When there is no jitter on input clock CLKI, the maximum jitter on CLKO is 0.020 UI pp with no bandlimiting, 0.010 UI in the 10 Hz - 40 kHz band, and 0.012 UI in the 8 - 40 kHz band.

- 1.544 MHz to 2.048 MHz or 4.096 MHz: In this mode of operation when there is no jitter on input clock CLKI, the maximum jitter on CLKO is 0.035 UI pp over the range of 20 Hz to 100 kHz, and 0.025 UP pp in the 18-100 kHz band.

Jitter Transfer

The CLAD is sensitive to jitter on the input clock in certain frequency bands. The jitter transfer curve is determined by the frequency and amplitude of the input jitter. Figures 8 and 9 show nominal jitter transfer measured in nanoseconds. These figures graph output jitter (less intrinsic jitter) divided by input jitter (0.25 UI). Jitter transfer from a 2.048 MHz CLKI to a 1.544 MHz CLKO is shown in Figure 8. In this mode, jitter in the critical 8 kHz band is attenuated while jitter in the 18 - 70 kHz band is transferred with a small net gain. Jitter transfer from a 1.544 MHz CLKI to a 2.048 MHz CLKO is shown in Figure 9. In both modes, with an input jitter level of 0.25 UI, jitter transfer is held below a net gain of 1.110. (Jitter transfer varies with the input jitter level. Performance in a particular application should be verified in the actual circuit.)

Table 8: Output Jitter Specifications

Parameter	Sym	Frequency	Spec[1]	Typ[2]	Max	Units	Test Conditions
Output Jitter on CLKO CLKO = 1.544 MHz	Tj1	No Bandlimiting	0.050	0.010	0.020	UI pp	CLKI = 2.048 or 4.096 MHz JI = 0 $\overline{FSI}$ applied
		10 Hz to 40 kHz	0.025	0.005	0.010	UI pp	
		8 kHz to 40 kHz	0.025	0.006	0.012	UI pp	
Output Jitter on CLKO CLKO = 2.048 MHz	Tj2	20 Hz to 100 kHz	1.500	0.025	0.035	UI pp	CLKI = 1.544 MHz, JI = 0 $\overline{FSI}$ applied
		18 kHz to 100 kHz	0.200	0.015	0.025	UI pp	

[1] Specifications from AT&T Publication 62411 and CCITT Recommendations G.823 (for 1.544 MHz and 2.048 MHz, respectively).

[2] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 8: Nominal Jitter Transfer - 2.048 MHz CLKI to 1.544 MHz CLKO (Input Jitter = 0.25 UI)

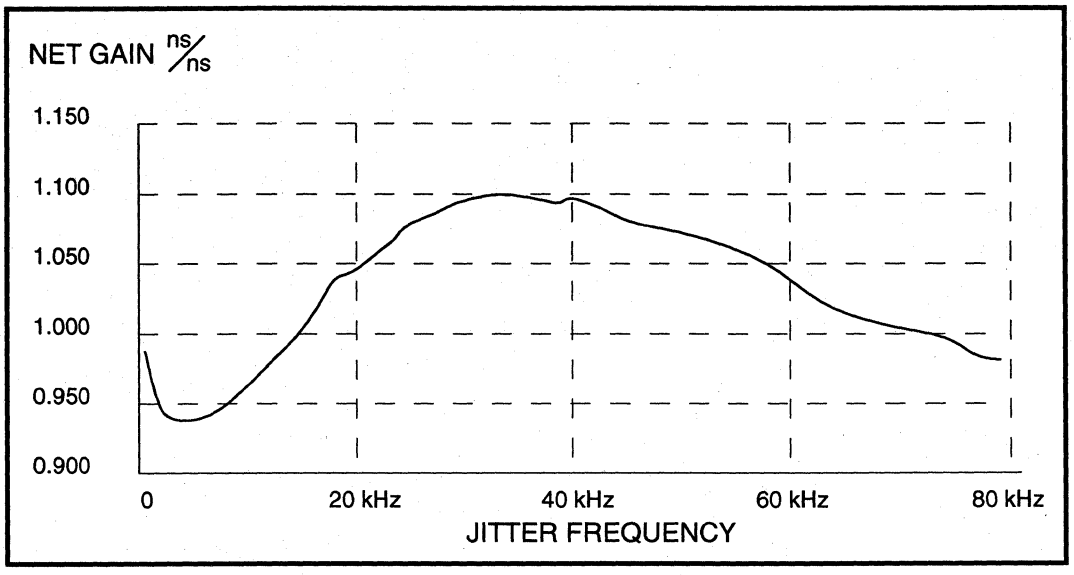
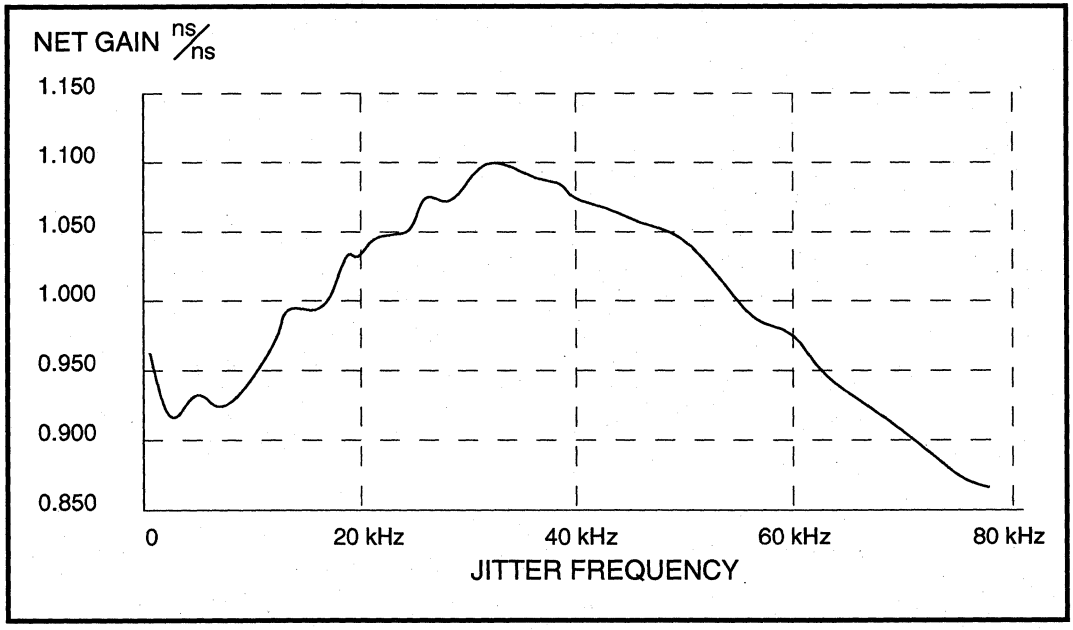


Figure 9: Nominal Jitter Transfer - 1.544 MHz CLKI to 2.048 MHz CLKO (Input Jitter = 0.25 UI)



Application and Design Considerations

Frame Sync Generation

A frame sync pulse is required to synchronize the input and output clocks. If a frame sync pulse is not provided on the backplane, one can be generated from the existing 2.048 MHz backplane clock. A typical FSI generation circuit is shown in Figure 10.

Power Supply Decoupling and Filtering

The LXP610 CLAD is designed to meet AT&T Publication 62411 specifications for jitter in the range from 10 Hz to 100 kHz. Proper power supply decoupling is critical for meeting these specifications. As shown in Figure 11, a standard 0.1µF bypass capacitor is recommended.

The CLAD is a monolithic silicon device which incorporates both analog and digital circuits. CLAD application circuit design may require closer attention to power supply filtering and bypassing than required for strictly digital devices.

Switching power supplies which operate below 100 kHz may produce noise spikes which can affect the analog sections of the CLAD. These spikes should be filtered with an RC network at the CLAD VCC pin.

Typical Application

Figure 11 shows a typical application circuit using a pair of LXP610 CLADs to convert between the 2.56 MHz backplane frequency and the 1.544 MHz T1 rate. The CLAD at the top of the figure provides the 1.544 MHz TCLK for the T1 framer and transceiver. For conversion from 2.56 MHz to 1.544 MHz, P1, P2, and P4 are tied low; and P1 and SEL are tied high. In this configuration, the LXP610 HFO is 7.720 MHz.

The CLAD at the bottom of Figure 11 produces the 2.56 MHz backplane clock. For conversion from 1.544 MHz to 2.56 MHz, P1, P2, P3 and P4 are tied high; and SEL is tied low. The HFO produced in this configuration is 7.680 MHz.

2

Figure 10 Frame Sync (FSI) Generation Circuit

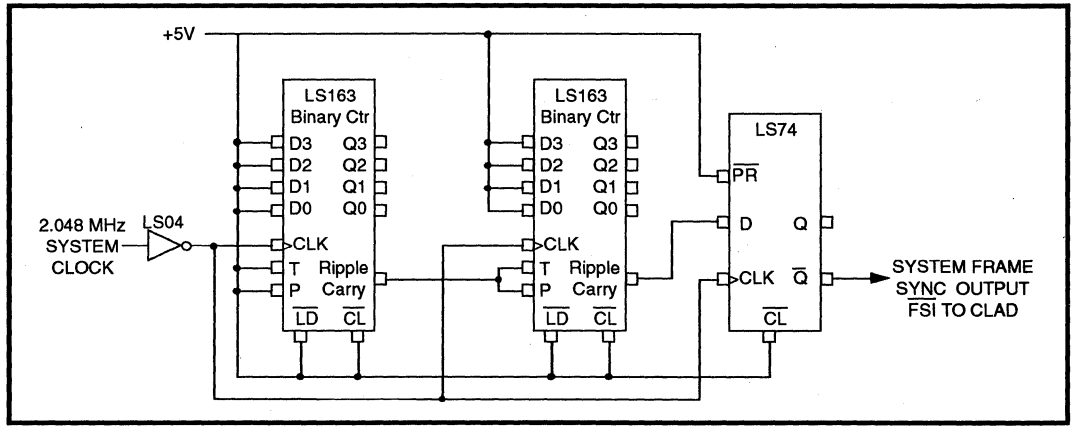
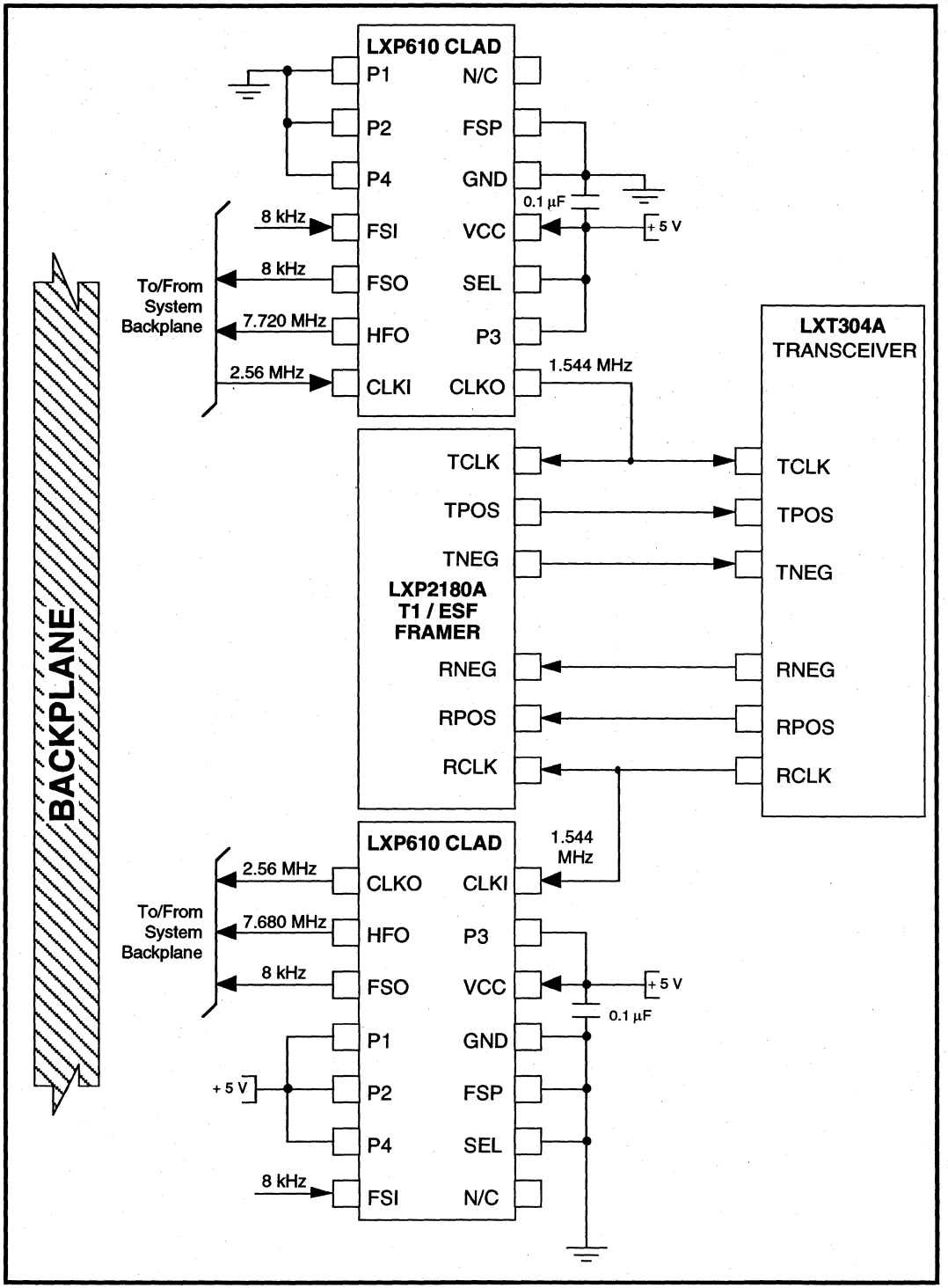


Figure 11: Typical Application Circuit



LXP2175

T1/E1 Elastic Store

General Description

The LXP2175 is one of a family of Level One Primary Rate Interface solutions. It is compatible with LXT30x series transceivers, and LXP2180A/2181A framer/formatters. The LXP2175 is a low-power CMOS elastic-store memory optimized for use in primary rate telecommunications transmission equipment.

Compatible with North American T1 (1.544 MHz) and European E1 (2.048 MHz) primary rate networks, the device serves as a synchronous element between asynchronous data streams. The LXP2175 has several flexible operating modes which eliminate support logic and hardware otherwise required to interconnect parallel or serial TDM backplanes. The LXP2175 is a drop-in replacement for the DS2175.

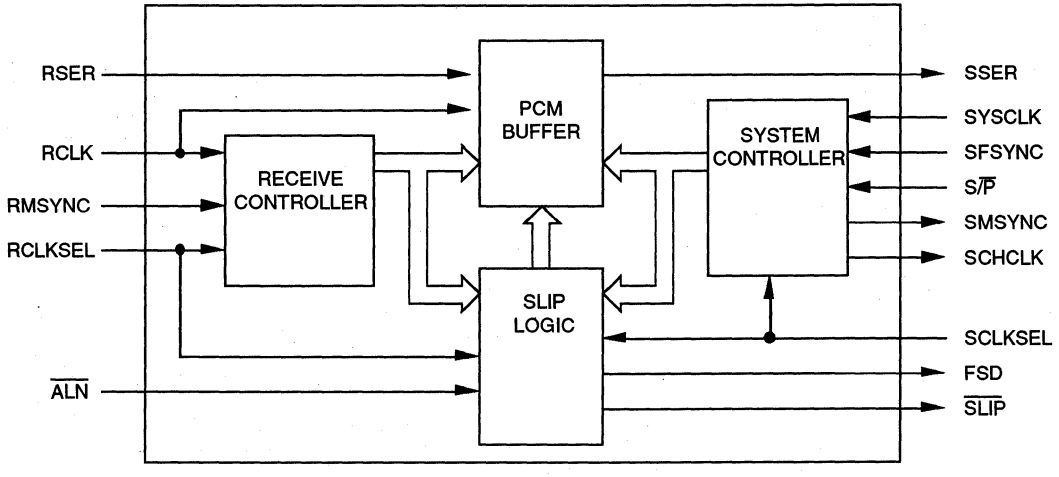
Applications

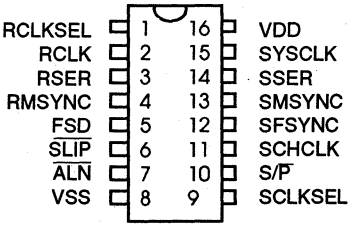
- Digital Trunks
- Drop and Insert Equipment
- Digital Cross-connects (DACS)
- Private Network Equipment
- PABX-to-computer interfaces such as DMI and CPI.

Features

- Drop-in replacement for the DS2175
- Rate buffer for T1/E1 transmissions
- Synchronizes loop-timed and system-timed T1/E1 data streams
- Ideal for 1.544 to 2.048 MHz rate conversion
- Supports parallel and serial backplanes
- Easily monitored two-frame buffer depth
- Comprehensive on-chip slip control logic
- Slips occur only on frame boundaries
- Outputs report slip occurrences and direction
- Align feature allows buffer to be recentered at any time
- Available in 16-pin DIP and SOP
- Compatible with Level One LXP2180A and LXP2181A framer/formatters

Figure 1: Block Diagram





Pin Descriptions

Pin	Sym	I/O	Name	Description
1	RCLKSEL	I	Receive Clock Select	Tie to VSS for 1.544 MHz applications, to VDD for 2.048 MHz.
2	RCLK	I	Receive Clock	Primary 1.544 MHz or 2.048 MHz data clock.
3	RSER	I	Receive Serial Data	Sampled on falling edge of RCLK.
4	RMSYNC	I	Receive Multi-frame Sync	Rising edge establishes receive side frame and multiframe boundaries.
5	FSD	O	Frame Slip Direction	State indicates direction of last slip; latched on slip occurrence.
6	$\overline{\text{SLIP}}$	O	Frame Slip	Active low, open collector output. Held low for 65 SYSCLK cycles when a slip occurs.
7	$\overline{\text{ALN}}$	I	Align	Recenters buffer on next system side frame boundary when forced low.
8	VSS	–	Signal Ground	0.0 volt ground return.
9	SCLKSEL	I	System Clock Select	Tie to VSS for 1.544 MHz applications, to VDD for 2.048 MHz.
10	S/$\overline{\text{P}}$	I	Serial Parallel Select	Tie to VSS for parallel backplane applications, to VDD for serial.
11	SCHCLK	O	System Channel Clock	Transitions high on channel boundaries; useful for serial to parallel conversion of channel data.
12	SFSYNC	I	System Frame Sync	Rising edge establishes system side frame boundaries.
13	SMSYNC	O	System Multi-frame Sync	Slip-compensated multiframe output. Used with RMSYNC to monitor depth of store in real time.
14	SSER	O	System Serial Data	Updated on rising edge of SYSCLK.
15	SYSCLK	I	System Clock	1.544 or 2.048 MHz data clock.
16	VDD	I	Positive Supply	+5 Volt power supply input.

PCM Buffer

The LXP2175 utilizes a two-frame buffer to synchronize incoming PCM data to the system backplane clock. Buffer depth is mode dependent: 2.048 MHz to 2.048 MHz applications use 64 bytes of buffer memory; all other modes are supported by 48 bytes. The buffer samples data at RSER on the falling edge of RCLK. Output data appears at SSER and is updated on the rising edge of SYSCLK. The buffer depth is constantly monitored by on-board contention logic. A "slip" occurs when the buffer is completely emptied or filled. Slips automatically recenter the buffer to a one-frame depth and always occur on frame boundaries.

Data Format

Data is presented to, and output from, the elastic store in a "framed" format. A rising edge at RMSYNC establishes receive side frame boundaries (see Figures 2 and 3). A rising edge at SFSYNC establishes system side multiframe boundaries (see Figures 4 and 5). North American (T1) frames contain 24 data channels of 8 bits each and an F-bit (193 bits total). European (E1) frames contain 32 data channels (256 bits). The frame rate of both systems is 8 KHz. RMSYNC and SFSYNC do not require a pulse at every frame boundary. If desired, they may be pulsed once to establish frame alignment. Internal counters will then maintain the frame alignment and may be reinforced by the next rising edge at RMSYNC and/or SFSYNC.

Slip Correction Capability

The two-frame buffer depth is adequate for T1 and E1 applications where short-term jitter synchronization, rather than correction of significant frequency differences, is required. The LXP2175 provides a balance between total delay (less than 250 ms at its full depth) and slip correction capability.

Buffer Recentering

Many applications require that the buffer be recentered during system power-up and/or initialization. Forcing ALN low recenters the buffer on the next rising edge of SFSYNC. A slip will occur during this recentering if the buffer depth is adjusted. If the depth is presently optimum, no adjustment (slip) occurs.

Slip Reporting

SLIP is held low for 65 SYSCLK cycles when a slip occurs. SLIP is an active-low, open-collector output. FSD indicates slip direction. When low (buffer empty), a frame of data was repeated at SSER during the previous slip. When high (buffer full), a frame of data was deleted. FSD is updated at every slip occurrence.

Buffer Depth Monitoring

SMSYNC is a system side output pulse which indicates system side multiframe boundaries. The distance between rising edges at RMSYNC and SMSYNC indicates the current buffer depth. Slip direction and/or an impending slip condition may be determined by monitoring RMSYNC and SMSYNC real time. SMSYNC is held high for 65 SYSCLK cycles.

Clock Select

Receive and system side clock frequencies are independently selectable by inputs RCLKSEL and SCLKSEL. 1.544 MHz is selected when RCLKSEL (SCLKSEL)=0; and 2.048 MHz is selected when RCLKSEL (SCLKSEL)= 1. In 1.544 MHz (receive) to 1.544 MHz (system) applications, the F-bit is passed through the receive buffer and presented at SSER immediately after a rising edge on SFSYNC. The F-bit is forced to 1 in 2.048 MHz to 1.544 MHz applications. No F-bit position exists in 2.048 MHz system side applications.

Parallel Compatibility

The LXP2175 is compatible with parallel and serial backplanes. In serial applications ($S/\overline{P} = 1$), channel 1 data appears at SSER after a rising edge at SFSYNC. In parallel applications ($S/\overline{P} = 0$), the device utilizes a look-ahead circuit. Data is output 8 clocks earlier as shown in Figures 4 and 5, allowing a user to parallel convert data externally, using an HC595 shift register.

Figure 2: Receive Side Timing (RCLK = 1.544 MHz)

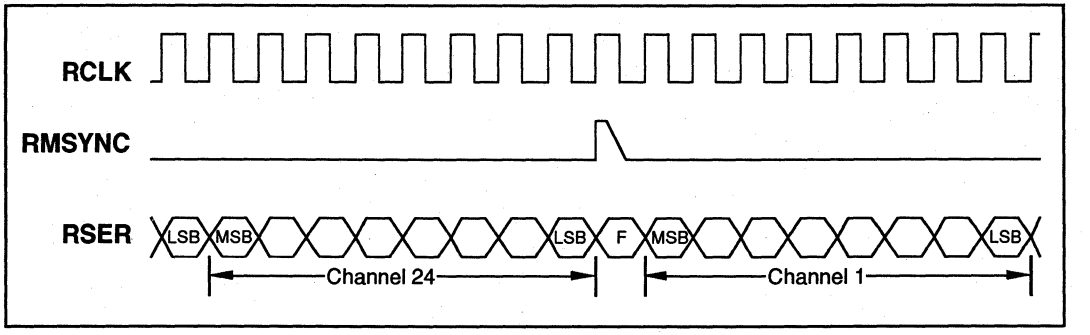
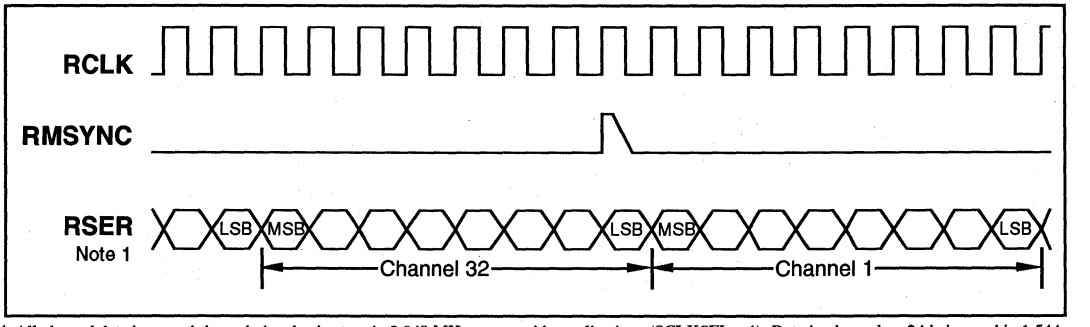
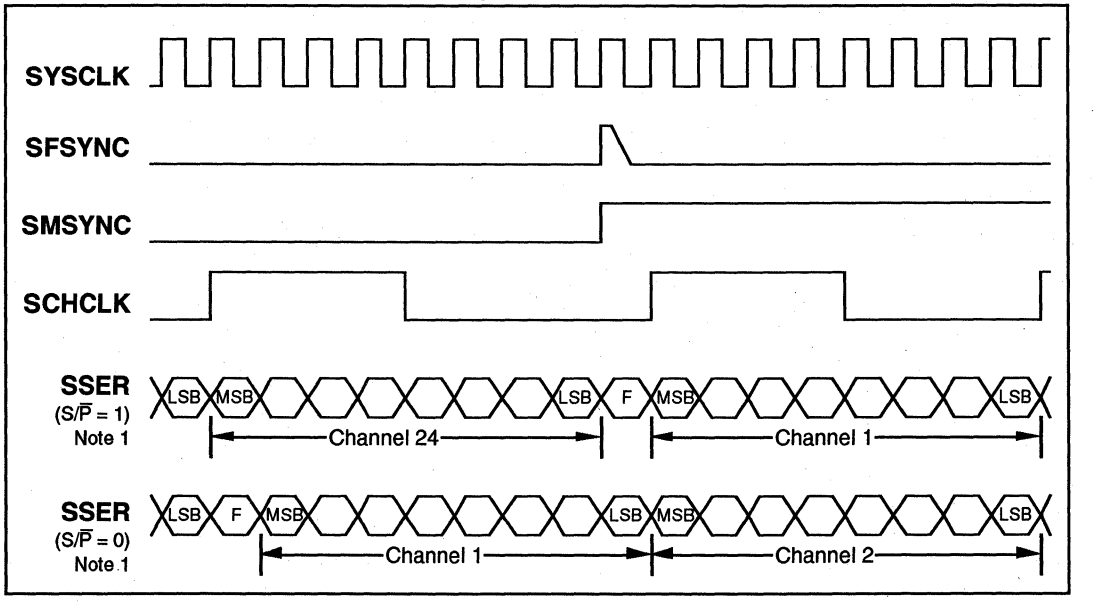


Figure 3: Receive Side Timing (RCLK = 2.048 MHz)



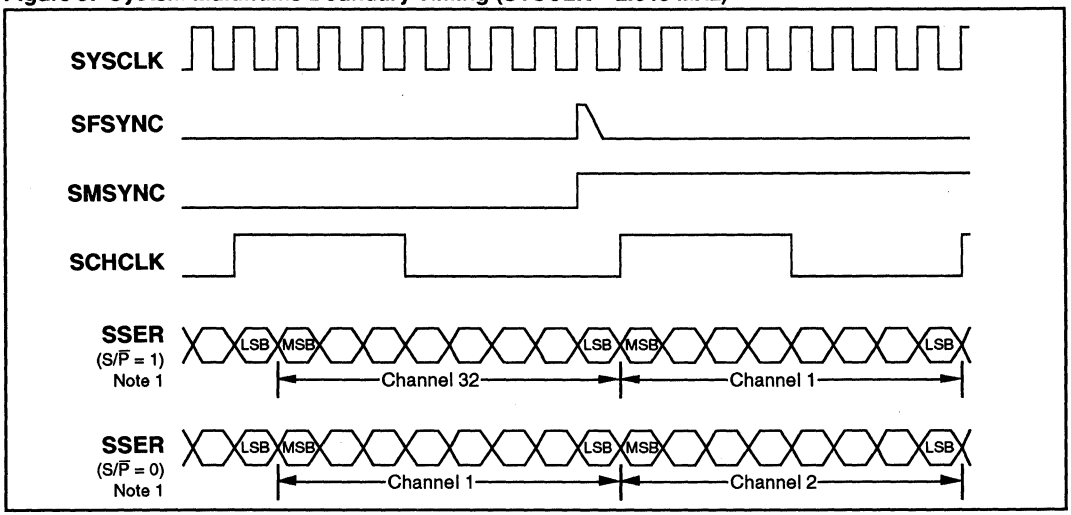
[1] All channel data is passed through the elastic store in 2.048 MHz system side applications (SCLKSEL = 1); Data in channels > 24 is ignored in 1.544 MHz system side applications (SCLKSEL = 0).

Figure 4: System Multiframe Boundary Timing (SYSCLK = 1.544 MHz)



[1] In 1.544 MHz receive side applications (RCLKSEL = 0), the F-bit position contains F-bit data extracted from the data stream at RSER. The F-bit position is forced to "1" in 2.048 MHz receive side applications (RCLKSEL = 1).

Figure 5: System Multiframe Boundary Timing (SYSCLK = 2.048 MHz)



[1] All channel data is passed through the elastic store in 2.048 MHz system side applications (SCLKSEL = 1); Data in channels > 24 is ignored in 1.544 MHz system side applications (SCLKSEL = 0).

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- Voltage on any pin relative to ground -1.0V to + 7V
- Operating temperature (2175SC and NC) 0 °C (min) to 70 °C (max)
  (2175SE and NE) -40 °C (min) to 85 °C (max)
- Storage temperature -55 °C (min) to 125 °C (max)
- Soldering temperature 260 °C for 10 seconds

Recommended Operating Conditions (Voltages are with respect to ground (VSS) unless otherwise stated)

Parameter	Sym	Min	Typ[1]	Max	Units
Logic 1	V_{IH}	2.0	–	V_{DD} + .3	V
Logic 0	V_{IL}	-0.3	–	+0.8	V
Supply voltage	V_{DD}	4.5	5	5.5	V

DC Electrical Characteristics - Clocked operation over recommended temperature and power supply ranges

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input capacitance	C_{IN}	–	–	5	pF	
Output capacitance	C_{OUT}	–	–	7	pF	
Supply current	I_{DD}	–	6	-	mA	See Notes 2 and 3
Input leakage	I_{IL}	-1.0	–	+1.0	µA	
Output high current	I_{OH}	-1.0	–	–	mA	V_{OH} = 2.4 V, See Note 4
Output low current	I_{OL}	+4.0	–	–	mA	V_{OL} = 0.4 V, See Note 5

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] SYSCLK = RCLK = 1.544 MHz
[3] Outputs Open
[4] All outputs except $\overline{SLIP}$, which is open collector.
[5] All outputs.

A.C. Electrical Characteristics

Parameter	Sym	Min	Max	Units
RCLK Period	t_{RCLK}	200	-	ns
RCLK, SYSCLK Rise and Fall	t_R, t_F	-	20	ns
RCLK Pulse Width	t_{RWH}, t_{RWL}	100	-	ns
SYSCLK Pulse Width	t_{SWH}, t_{SWL}	100	-	ns
SYSCLK Period	t_{SCLK}	200	-	ns
RMSYNC Setup to RCLK Rising	t_{SC}	$-t_{RWH}/2$	$+t_{RWL}/2$	ns
SFSYNC Setup to SYSCLK Rising	t_{SC}	$-t_{SWH}/2$	$+t_{SWL}/2$	ns
RMSYNC, SFSYNC, $\overline{ALN}$ Pulse Width	t_{PW}	100		ns
RSER Setup to RCLK Falling	t_{SD}	50		ns
RSER Hold from RCLK Falling	t_{HD}	50		ns
Propagation Delay SYSCLK to SSER, or RCLK to RSER	t_{PVD}	-	75	ns
Propagation Delay SYSCLK to SMSYNC High	t_{PSS}	-	75	ns
Propagation Delay SYSCLK or RCLK to $\overline{SLIP}$ Low, FSD low/high	t_{PS}	-	100	ns
$\overline{ALN}$ Setup to SFSYNC Rising	t_{SR}	500	-	ns

Figure 6: Receive A.C. Timing Diagram

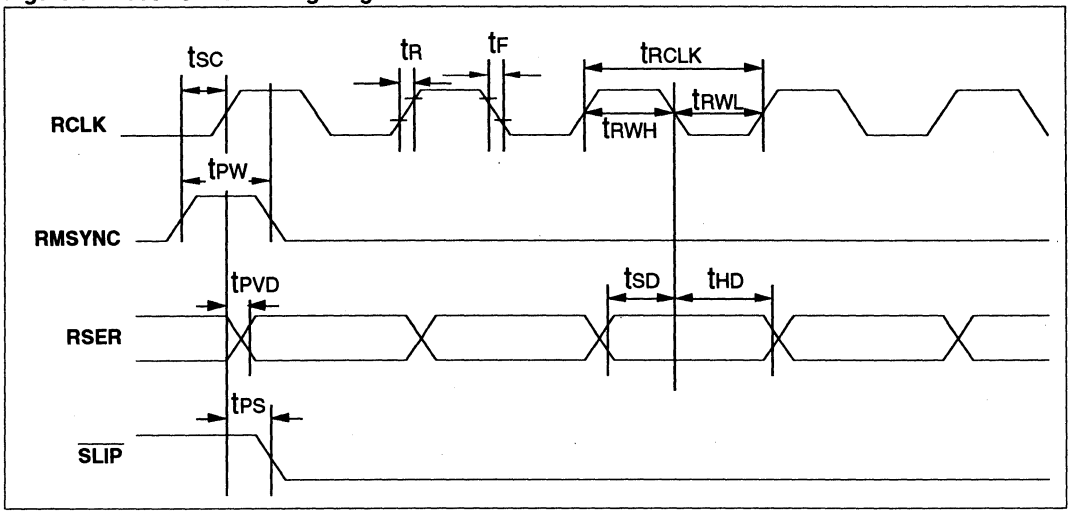
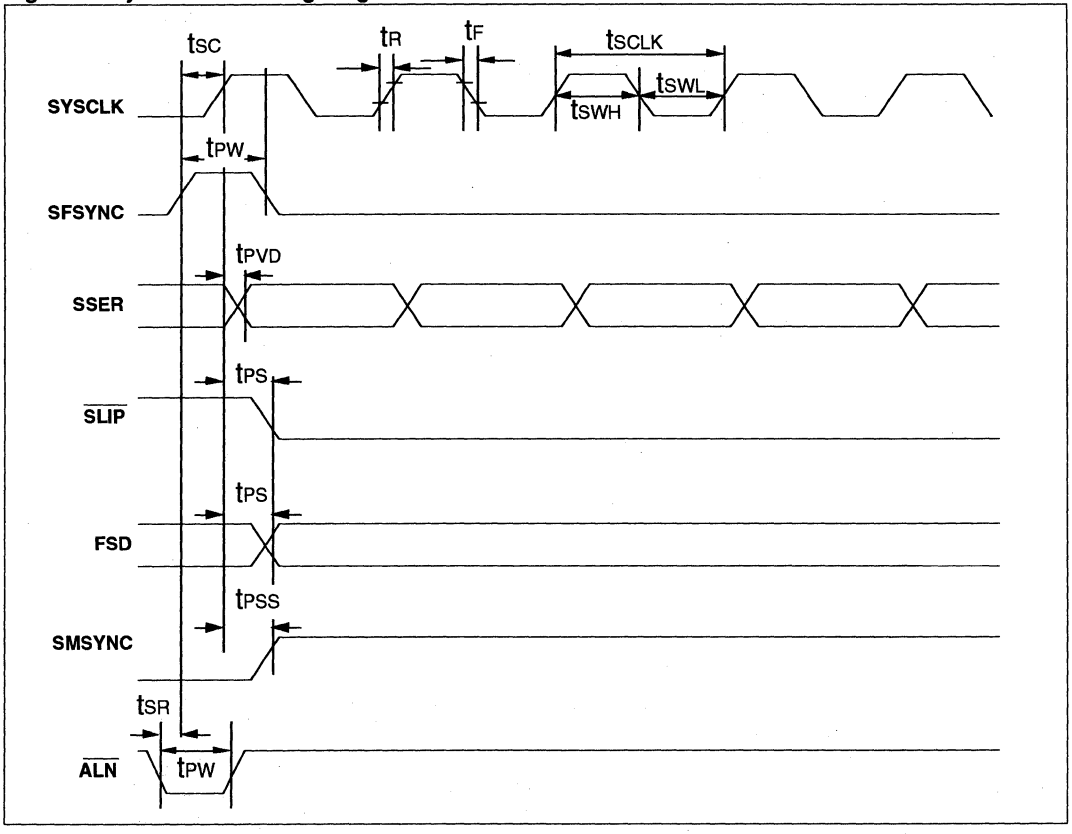


Figure 7: System A.C. Timing Diagram



Notes:

LXP2176

T1 Receive Buffer

General Description

The LXP2176 is one of a family of Level One T1 interface solutions and is compatible with the LXT300/301 Transceiver, the LXP2180A Framer/Formatter, and the LXP600/601 Clock Rate Adapter. The LXP2176 is a low-power CMOS device specifically designed for synchronizing receive side loop-timed T-carrier data streams with system side timing. The device has several flexible operating modes which simplify interfacing incoming data to parallel and serial TDM backplanes. The device extracts, buffers and integrates ABCD signaling; signaling updates are prohibited during alarm or slip conditions. The buffer replaces extensive hardware in existing applications with one integrated chip. The LXP2176 is a fully pin-compatible drop-in replacement for the DS2176.

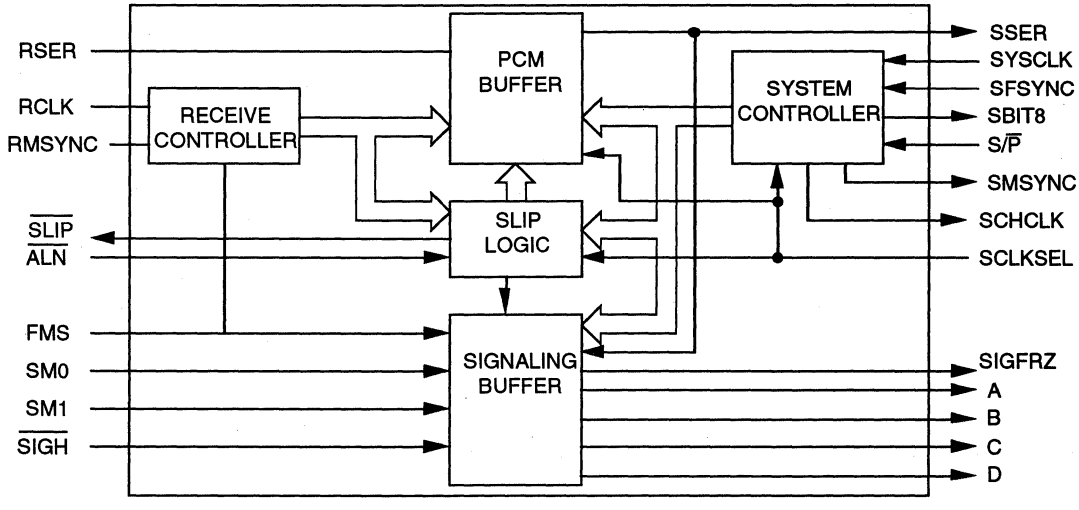
Applications

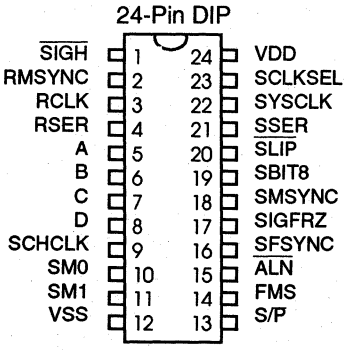
- Digital Trunks
- Drop and Insert Equipment
- Transcoders
- Digital Cross-connects (DACS)
- Private Network Equipment
- PABX-to-computer interfaces such as DMI and CPI.

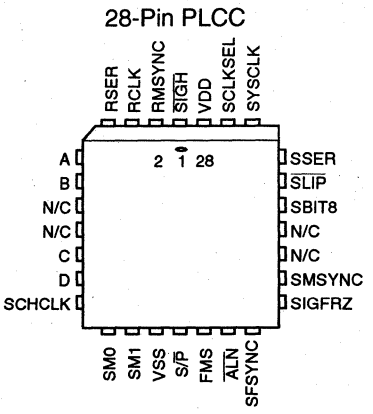
Features

- Drop-in replacement for the DS2176
- Synchronizes loop-timed and system timed Tl data streams
- Two-frame buffer depth; slips occur on frame boundaries
- Output indicates when slip occurs
- Buffer may be recentered externally
- Ideal for 1.544 to 2.048 MHz rate conversion
- Interfaces to parallel or serial backplanes
- Extracts and buffers robbed-bit signaling
- Inhibits signaling updates during alarm or slip conditions
- Integration feature "debounces" signaling
- Slip-compensated output indicates when signaling updates occur
- Compatible with LXP2180A T1 framer/formatter
- Choice of 24-pin DIP or 28-pin PLCC (surface mount)

Figure 1: Block Diagram







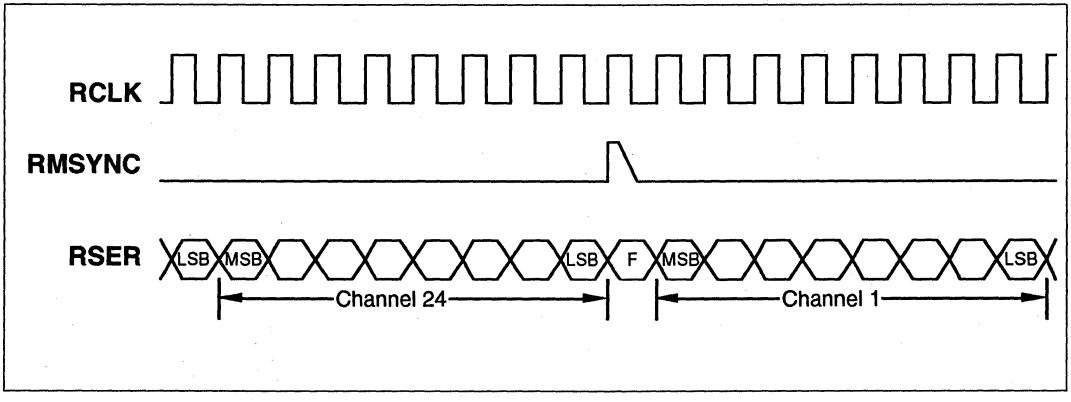
Pin Descriptions

Pin		Sym	I/O	Name	Description
DIP	PLCC				
1	1	SIGH	I	Signaling Inhibit	When low, ABCD signaling updates are disabled for a period determined by SM0 and SM1, or until returned high.
2	2	RMSYNC	I	Receive Multi-frame Sync	Must be pulsed high at multiframe boundaries to establish frame and multiframe alignment.
3	3	RCLK	I	Receive Clock	Primary 1.544 MHz clock.
4	4	RSER	I	Receive Serial Data	Sampled on falling edge of RCLK.
5 6 7 8	5 6 9 10	A B C D	O	RBS Outputs	Robbed-Bit Signaling Outputs
9	11	SCHCLK	I	System Channel Clock	Transitions high on channel boundaries; useful for serial-to-parallel conversion of channel data.
10 11	12 13	SM0 SM1	O	Signaling Modes 0 and 1	Select signaling supervision technique.
12	14	VSS	–	Signal Ground	Signal Ground. 0.0 volts.
13	15	S/P	I	Serial Parallel Select	Tie to VSS for parallel backplane applications, to VDD for serial.
14	16	FMS	I	Frame Mode Select	Tie to VSS to select 193S (D4) framing, to VDD for 193E (extended).
15	17	ALN	I	Align	Recenters buffer on next system side frame boundary when forced low.
16	18	SFSYNC	I	System Frame Sync	Rising edge establishes start of frame.

Pin Descriptions continued

Pin		Sym	I/O	Name	Description
DIP	PLCC				
17	19	SIGFRZ	O	Signaling Freeze	When high, indicates signaling updates have been disabled internally via a slip or externally by forcing $\overline{\text{SIGH}}$ low.
18	20	SMSYNC	O	System Multi-frame Sync	Slip-compensated multiframe output; indicates when signaling updates are made.
19	23	SBIT8	I	System Bit 8	High during the LSB time of each channel. Used to reinsert extracted signaling into outgoing data stream.
20	24	$\overline{\text{SLIP}}$	O	Frame Slip	Active low, open collector output. Held low for 64 SCLK cycles when a slip occurs.
21	25	SSER	O	System Serial Output	Updated on rising edge of SYSCLK.
22	26	SYSCLK	I	System Clock	1.544 or 2.048 MHz data clock.
23	27	SCLKSEL	I	System Clock Select	Tie to VSS for 1.544 MHz applications, to VDD for 2.048 MHz.
24	28	VDD	I	Positive Supply	+5 Volt power supply input.

Figure 2: Receive Side Timing



OVERVIEW

The LXP2176 performs two primary functions:

1) Synchronization of received T1 PCM data (looped timed) to host backplane frequencies
2) Supervision of robbed-bit signalling data embedded in the data stream.

The buffer, while optimized for use with the LXP2180A T1 Framer/formatter, is also compatible with other framers and transceivers. The LXP2180A data sheet should serve as a valuable reference when designing with the LXP2176.

DATA SYNCHRONIZATION

PCM Buffer

The LXP2176 utilizes a two-frame buffer (386 bits) to synchronize incoming PCM data to the system backplane clock. The buffer samples data at RSER on the falling edge of RCLK. Output data appears at SSER and is updated on the rising edge of SYSCLK. A rising edge at RMSYNC establishes receive side frame and multiframe alignment as shown in Figure 2. A rising edge at SFSYNC establishes system side frame alignment. The buffer depth is constantly monitored by on-board contention logic, a "slip" occurs when the buffer is completely emptied or filled. Slips automatically recenter the buffer to a one-frame depth and always occur on frame boundaries.

Slip Correction Capability

The two-frame buffer depth is adequate for most T-carrier applications where short-term jitter synchronization, rather than correction of significant frequency differences, is required. The LXP2176 provides a balance between total delay and slip correction capability.

Buffer Recentering

$\overline{\text{SLIP}}$ is held low for 65 SYSCLK cycles when a slip occurs. $\overline{\text{SLIP}}$ is an active-low, open-collector output.

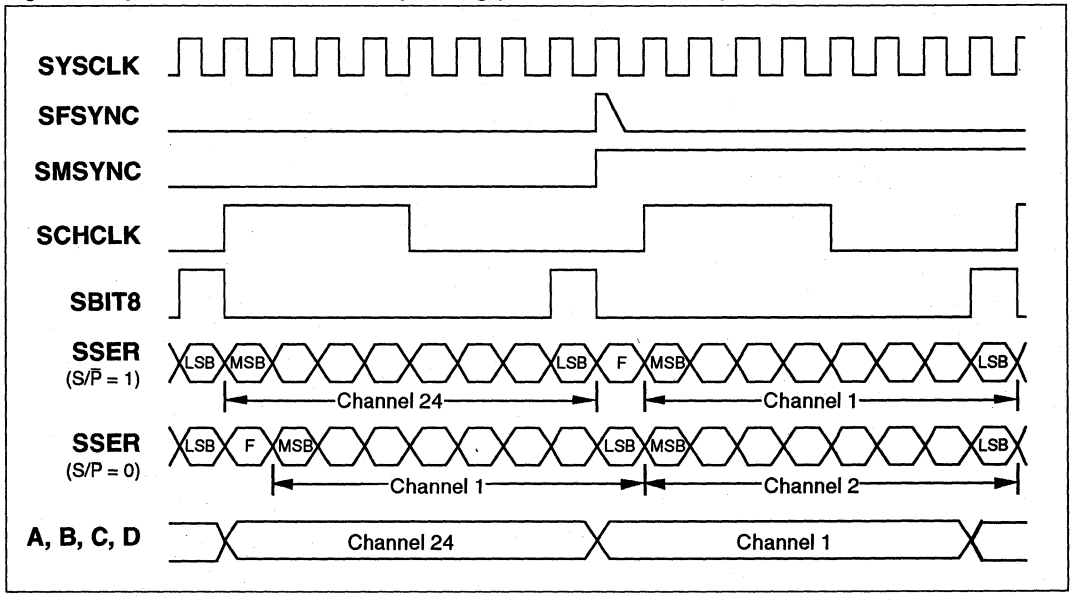
Buffer Depth Monitoring

SMSYNC is a system side output pulse which indicates system side multiframe boundaries. The distance between rising edges at RMSYNC and SMSYNC indicates the current buffer depth. Slip direction and/or an impending slip condition may be determined by monitoring RMSYNC and SMSYNC in real time. SMSYNC is held high for 65 SYSCLK cycles.

Clock Select

The LXP2176 is compatible with two common backplane frequencies: 1.544 MHz, selected when SCLKSEL=0; and 2.048 MHz, selected when SCLKSEL= 1. In 1.544 MHz

Figure 3: System Multiframe Boundary Timing (SYSCLK = 1.544 MHz)



applications the F-bit is passed through the receive buffer and presented at SSER immediately after a rising edge on SFSYNC. The F-bit is dropped in 2.048 MHz applications and the MSB of channel 1 appears at SSER one bit period after a rising edge at SFSYNC. SSER is forced to 1 in all channels greater than 24. See Figures 3 and 4.

In 2.048 MHz applications (SCLKSEL=1), the PCM buffer control logic establishes slip criteria different from that used in 1.544 MHz applications to compensate for the faster system-side read frequency.

Figure 4: System Multiframe Boundary Timing (SYSCLK = 2.048 MHz)

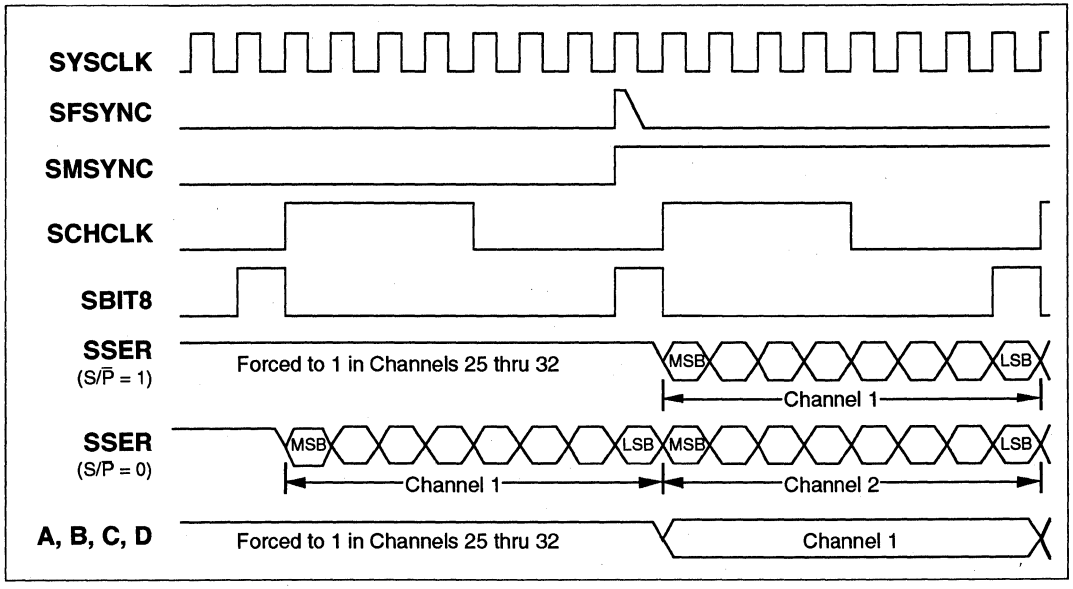


Figure 5: 193S System Multiframe Timing

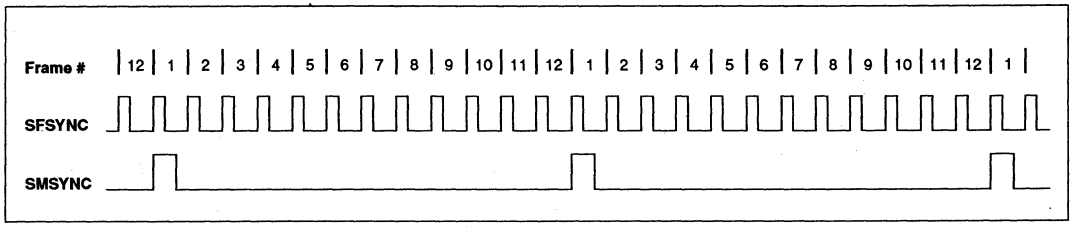
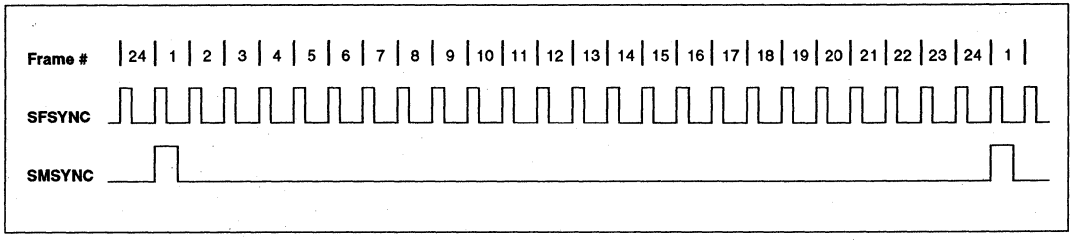


Figure 6: 193E System Multiframe Timing



Parallel Compatibility

The LXP2176 is compatible with parallel and serial backplanes. Channel 1 data appears at SSER after a rising edge at SFSYNC as shown in Figures 3 and 4 (serial applications, S/$\overline{P}$ = 1). The device utilizes a look-ahead circuit in parallel applications (S/$\overline{P}$ = 0). Data is output 8 clocks earlier, allowing a user to parallel convert data externally.

SIGNALING SUPERVISION

Extraction

In digital channel banks, robbed bit signaling data is inserted into the LSB of each channel during signaling frames. In 193S framing (FMS = 0) applications, A signaling data is inserted into frame 6 and B signaling data is inserted into frame 12. 193E framing (FMS = 1) includes two additional signaling bits: C signaling data is inserted into frame 18 and D signaling data is inserted into frame 24. This embedded signaling data is synchronized to system side timing (via the PCM buffer) before being extracted and presented at outputs A, B, C, and D. Outputs A, B, C and D are valid for each individual channel time and are repeated per channel for all frames of the multiframe. In 193S applications, outputs C and D contain the previous multiframe's A and B data. Signaling updates occur once per multiframe, at the rising edge of SMSYNC unless prohibited by a freeze.

Freeze

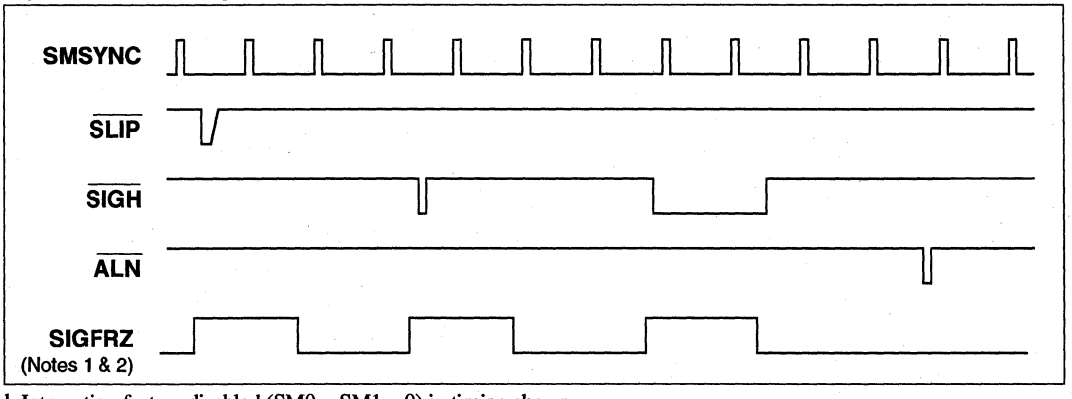
The signaling buffer allows the LXP2176 to "freeze" (prevent update of) signaling information during alarm or slip conditions. A slip condition or forcing $\overline{SIGH}$ low freezes signaling; duration of the freeze is dependent on SM0 and SM1. Updates will be unconditionally prohibited when $\overline{SIGH}$ is held low. During freezing conditions "old" data is recirculated in the output registers and appears at A,B,C and D. SIGFRZ is held high during the freeze condition, and returns low on the next signaling update. Input to output delay of signaling data is equal to one multiframe (the depth

Table 2: Signaling Supervision Modes

SM0	SM1	FMS	Selected Mode
0	0	0	193S framing, no integration, 1 multiframe freeze.
0	0	1	193E framing, no integration, 1 multiframe freeze.
0	1	0	193S framing, 2 multiframes integration and freeze.
0	1	1	193E framing, 2 multiframes integration and freeze.
1	0	0[1]	193S framing, 5 multiframes integration, 2 multiframes freeze.
1	0	1[1]	193E framing, 3 multiframes integration, 2 multiframes freeze.
1	1	0	Test mode.
1	1	1	Test mode.

[1] During slip or alarm conditions, integration is limited to 2 multiframes to minimize signaling delay.

Figure 7: Slip and Signaling Supervision Logic Timing



[1] Integration feature disabled (SM0 = SM1 = 0) in timing shown.

[2] Depending on present buffer depth, forcing $\overline{ALN}$ low may or may not cause a slip condition.

of the signaling buffer) + the current depth of the PCM buffer (1 frame + approximately 1 frame).

Integration

Signaling integration is another feature of the LXP2176. When selected, it minimizes the impact of random noise hits on the span and resultant robbed-bit signaling corruption. Integration requires that per-channel signaling data be in the same state for two or more multiframes before appearing at A, B, C, and D. SM0 and SM1 are used to select the degree of integration or to bypass the feature totally. Integration is limited to two multiframes during slip or alarm conditions to minimize update delay.

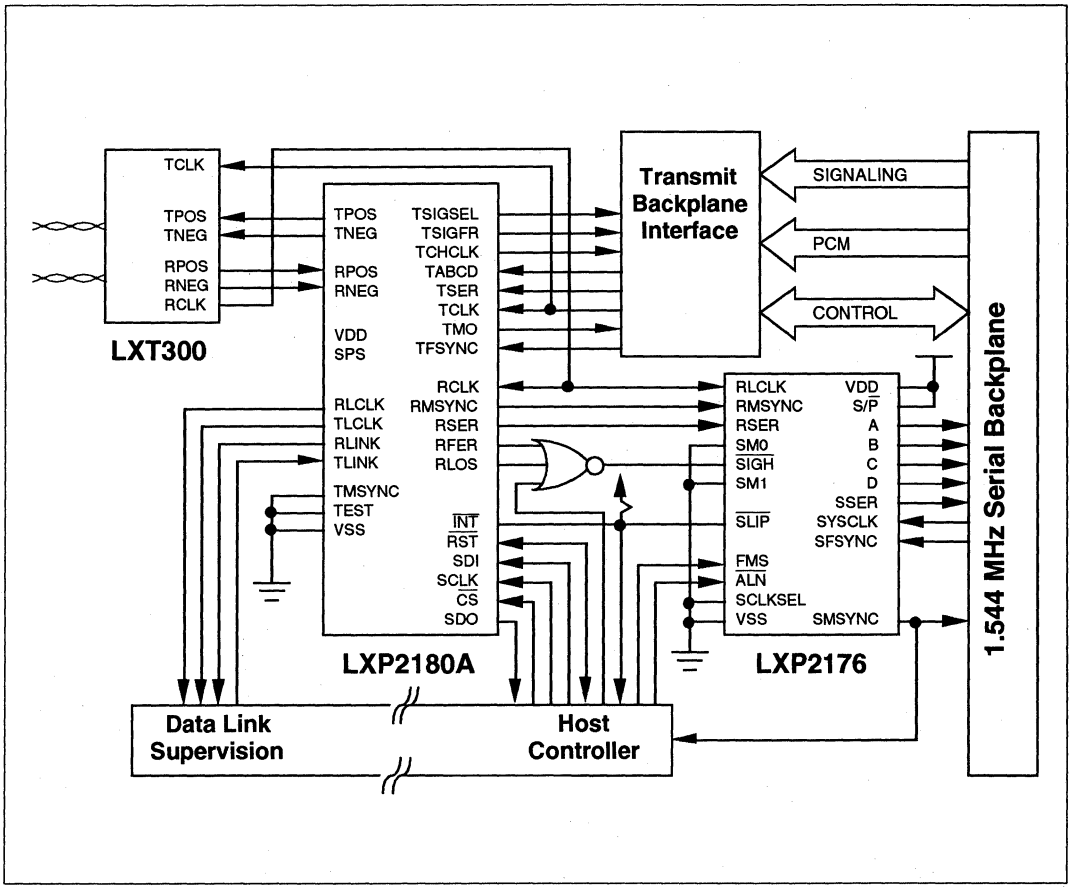
Clear Channel Considerations

The LXP2176 does not merge the "processed" signaling information with outgoing PCM data at SSER. This assures integrity of data in clear channel applications. SBIT8 indicates the LSB position of each channel. When combined with off-chip support logic, it allows the user to selectively insert robbed-bit signaling data into the outgoing data stream.

LXP2176/LXP2180A System Application

Figure 8 shows how the LXP2180A T1 Framer/Formatter and the LXP2176 Receive Buffer interconnect in a typical application.

Figure 8: Serial 1.544 MHz Backplane Interface Application



Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- Voltage on any pin relative to ground -1.0V to + 7V
- Operating temperature -40 °C (min) to 85 °C (max)
- Storage temperature -55 °C (min) to 125 °C (max)
- Soldering temperature 260 °C for 10 seconds

Recommended Operating Conditions (Voltages are with respect to ground (GND) unless otherwise stated)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Logic 1	V_{IH}	2.0	–	V_{DD} + .3	V	
Logic 0	V_{IL}	-0.3	–	+0.8	V	
Supply voltage	V_{DD}	4.5	5	5.5	V	
Capacitance						
Input capacitance	C_{IN}	–	–	5	pF	
Output capacitance	C_{OUT}	–	–	7	pF	
DC Electrical Characteristics - Clocked operation over recommended temperature and power supply ranges						
Supply current	I_{DD}	–	6	10	mA	See Notes 2 and 3
Input leakage	I_{IL}	-1.0	–	+1.0	µA	
Output high current	I_{OH}	-1.0	–	–	mA	V_{OH} = 2.4 V, See Note 4
Output low current	I_{OL}	+4.0	–	–	mA	V_{OL} = 0.4 V, See Note 5
Output leakage	I_{LO}	-1.0	–	+1.0	µA	See Note 6

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] TCLK = RCLK = 1.544 MHz
[3] Outputs Open
[4] All outputs except $\overline{SLIP}$, which is open collector.
[5] All outputs.
[6] Applies to $\overline{SLIP}$ when tristated.

A.C. Electrical Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units
RCLK Period	t_{RCLK}	250	648		ns
RCLK, SYSCLK Rise and Fall	t_R, t_F			20	ns
RCLK Pulse Width	t_{RWH}, t_{RWL}	125	324		ns
SYSCLK Pulse Width	t_{SWH}, t_{SWL}	100	244		ns
SYSCLK Period	t_{SCLK}	200	488		ns
RMSYNC Setup to RCLK Rising	t_{SC}	$-t_{RWH}/2$		$+t_{RWL}/2$	ns
SFSYNC Setup to SYSCLK Rising	t_{SC}	$-t_{SWH}/2$		$+t_{SWL}/2$	ns
RMSYNC, SFSYNC, $\overline{\text{SIGH}}$, $\overline{\text{ALN}}$ Pulse Width	t_{PW}	100			ns
RSER Setup to RCLK Falling	t_{SD}	50			ns
RSER Hold from RCLK Falling	t_{HD}	50			ns
Propagation Delay SYSCLK to SSER, A, B, C, D	t_{PVD}			100	ns
Propagation Delay SYSCLK to SMSYNC High	t_{PSS}			75	ns
Propagation Delay SYSCLK or RCLK to $\overline{\text{SLIP}}$ Low	t_{PS}			100	ns
Propagation Delay SYSCLK to SIGFRZ Low/High	t_{PSF}			75	ns
$\overline{\text{ALN}}$, $\overline{\text{SIGH}}$ Setup to SFSYNC Rising	t_{SR}	500			ns

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2 TCLK = RCLK = 1.544 MHz
3 Outputs Open
4 All outputs except SLIP, which is open collector.
5 All outputs.
6 Applies to SLIP when tristated.

Figure 9: Receive A.C. Timing Diagram

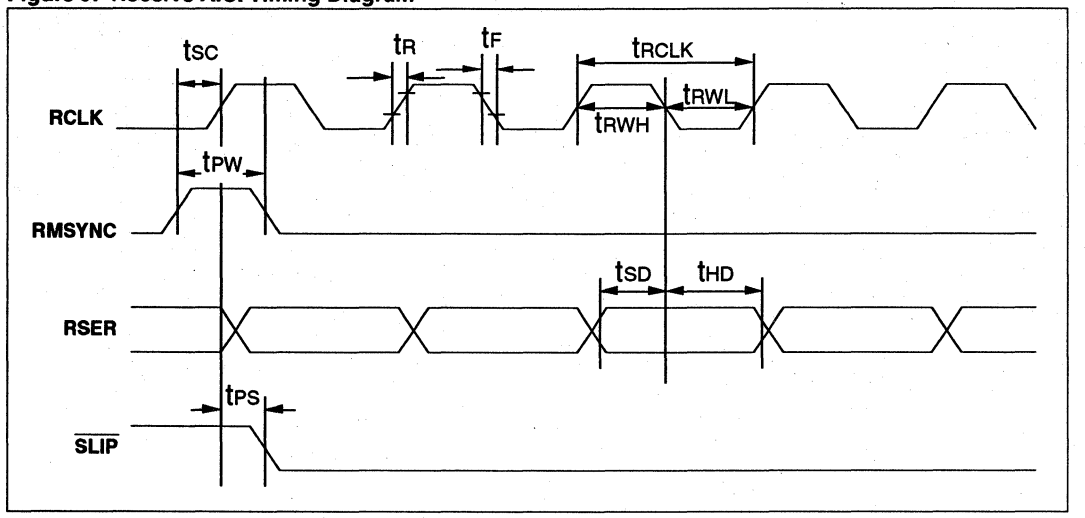
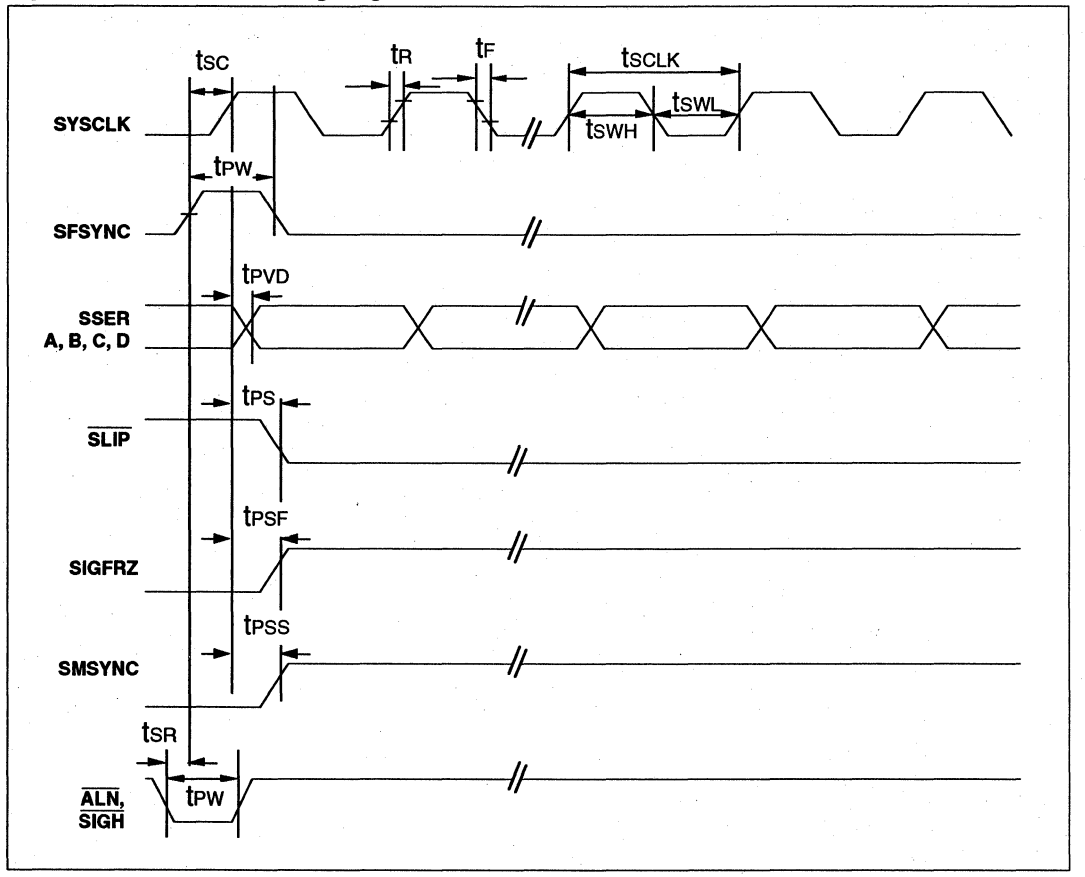


Figure 10: System A.C. Timing Diagram



LXP2180A

T1 ESF Framer/Formatter

General Description

The LXP2180A is one of a family of Level One T1 interface solutions. It is compatible with the LXT300 series transceivers and LXP600 series clock adapters. The device interfaces to the DS1 1.544 Mbps digital trunk. A pin compatible drop-in replacement for the Dallas DS2180A, the LXP2180A provides all formatting necessary for transmission on the T1 link. It supports both 193S and 193E superframe standards and provides clear channel capability through appropriate zero suppression and signaling modes.

The transmit framer/formatter circuits generate appropriate framing bits, insert robbed bit signaling, supervise zero suppression, generate alarms and provide output clocks for data conditioning and decoding. The receive and synchronizer circuits establish frame and multiframe boundaries, extract signaling data and report alarms and signaling formats. Control functions allow both stand-alone Hardware mode operation and Host mode operation for use with a microprocessor/microcontroller.

The LXP2180A is a monolithic CMOS device which requires only a single +5V power supply.

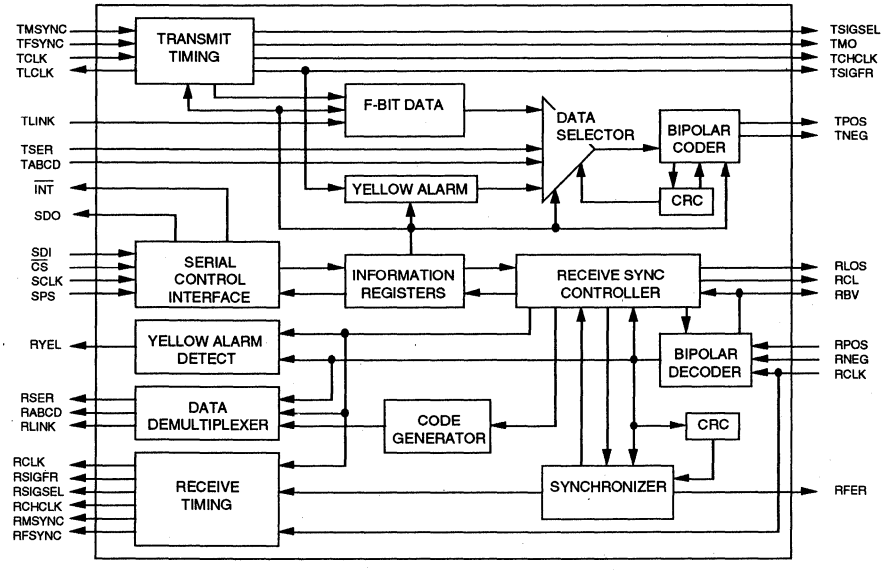
Applications

- DS1/ESF digital trunk interfaces
- Computer to PBX interfaces (DMI and CPI)
- High speed computer to computer data links
- Digital cross-connect interface

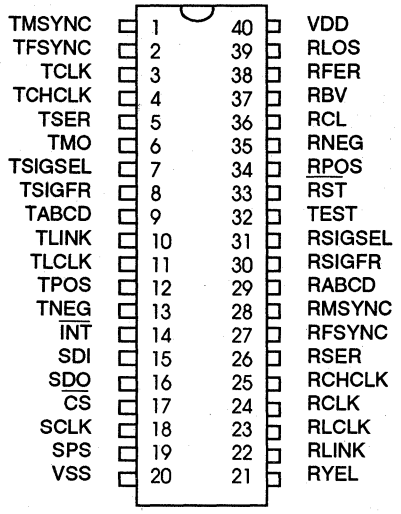
Features

- Drop-in replacement for the DS2180A
- Single chip DS1 rate framer/formatter
- Supports common framing standards
  - 12 frames/superframe "193S"
  - 24 frames/superframe "193E"
- Three zero suppression modes
  - B7 stuffing
  - B8ZS
  - Transparent
- Simple serial interface for configuration, control and status monitoring in Host mode
- Hardware mode for stand-alone applications requires no host processor
- Compatible with LXT300 series transceivers
- Selectable 0, 2, 4, 16 state robbed bit signaling modes
- Allows mix of "clear" and "non-clear" DS0 channels on same DS1 link
- Alarm generation and detection
- Receive error detection and counting for transmission performance monitoring
- +5V supply, low-power CMOS technology
- Available in 40-pin plastic DIP and 44-pin PLCC

Figure 1: Block Diagram



40-Pin DIP



44-Pin PLCC

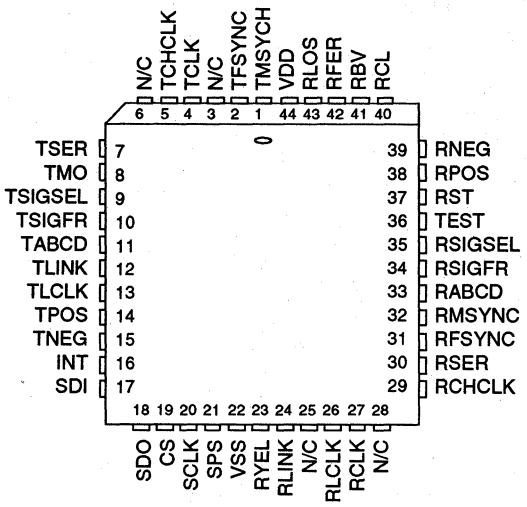


Table 1: Transmit Pin Descriptions

Pin# DIP	Pin# PLCC	Sym	I/O	Name	Description
1	1	TMSYNC	I	Transmit Multi-frame Sync	Transmit Multiframe Sync may be pulsed high at multiframe boundaries to reinforce multiframe alignment, or tied low, which allows internal multiframe counter to free run.
2	2	TFSYNC	I	Transmit Frame Sync Channel B2	Transmit Frame Sync. Rising edge identifies frame boundary. May be pulsed every frame to reinforce internal frame counter, or tied low to allow TMSYNC to establish frame/multiframe alignment.
3	4	TCLK	I	Transmit Clock	1.544 MHz primary clock.
4	5	TCHCLK	O	Transmit Channel Clock	192 kHz clock which identifies time slot (channel) boundaries. Useful for parallel to serial conversion of channel data.
5	7	TSER	I	Transmit Serial Data	NRZ data input, sampled on falling edge of TCLK.
6	8	TMO	O	Transmit Multi-frame Out	Output of internal multiframe counter, indicates multiframe boundaries. 50% duty cycle.
7	9	TSIGSEL	O	Transmit Signal-ing Select	In 193E framing mode, this output is a 0.667 kHz clock which identifies signaling frames A and C. In 193S framing, it's a 1.33 kHz clock.
8	10	TSIGFR	O	Transmit Signal-ing Frame	High during signaling frames, low otherwise.
9	11	TABCD	I	Transmit ABCD Signaling	When enabled via TCR.4, sampled during channel LSB time in signaling frames on falling edge of TCLK.

Table 1: Transmit Pin Descriptions continued

Pin# DIP	Pin# PLCC	Sym	I/O	Name	Description
10	12	TLINK	I	Transmit Data Link	Sampled during F-bit time (falling edge of TCLK) of odd frames for insertion into the outgoing data stream (193E-FDL insertion). Sampled during the F-bit time of even frames for insertion into the outgoing data (193S-External S-Bit insertion).
11	13	TLCLK	O	Transmit Link Clock	Transmit Link Clock is a 4 kHz demand clock for TLINK input.
12	14	TPOS	O	Transmit Positive and Negative Data	Transmit Bipolar Data Outputs. Updated on rising edge of TCLK.
13	15	TNEG	O		

Table 2: Port Pin Description

Pin# DIP	Pin# PLCC	Sym	I/O	Name	Description
14	16	$\overline{\text{INT}}$[1]	O	Receive Alarm Interrupt	In Host mode, an active low, open drain output which flags the host controller during alarm conditions.
15	17	SDI[1]	I	Serial Data Input	Serial port input data for on-board registers. Sampled on rising edge of SCLK (Host mode).
16	18	SDO[1]	O	Serial Data Output	Serial output of control and status information from on-board registers. Updated on falling edge of SCLK, tri-stated during serial port write or when $\overline{\text{CS}}$ is high (Host mode).
17	19	$\overline{\text{CS}}$[1]	I	Chip Select	Must be low to write or read the serial port registers (Host mode).
18	20	SCLK[1]	I	Serial Data Clock	Used to read or write the serial port registers (Host mode).
19	21	SPS	I	Serial Port Select	Tie to VDD to select serial port (Host mode). Tie to VSS to select the Hardware mode.

1. Multifunction pins; see Hardware mode description.

Table 3: Power and Test Pin Descriptions

Pin# DIP	Pin# PLCC	Sym	I/O	Name	Description
20	22	VSS	–	Signal Ground	0.0 V signal ground.
32	36	TEST	I	Test Mode	Tie to VSS for normal operation.
40	44	VDD	–	Positive Supply	+5V power supply input.

Table 4: Receive Pin Descriptions

Pin# DIP	Pin# PLCC	Sym	I/O	Name	Description
21	23	RYEL	O	Receive Yellow Alarm	Transitions high when yellow alarm detected, goes low when alarm clears.
22	24	RLINK	O	Receive Link Data	Updated with extracted FDL data one RCLK before start of odd frames (193E) and held until next update. Updated with extracted S-bit data one RCLK before start of even frames (193S) and held until next update.
23	26	RLCLK	O	Receive Link Clock	4 kHz demand clock for RLINK.
24	27	RCLK	I	Receive Clock	1.544 MHz primary clock.
25	29	RCHCLK	O	Receive Channel Clock	192 kHz clock, identifies time slot (channel) boundaries.
26	30	RSER	O	Receive Serial Data	Received NRZ serial data, updated on rising edge of RCLK.
27	31	RFSYNC	O	Receive Frame Sync	Extracted 8 kHz clock, one RCLK wide, indicates F-bit position in each frame.
28	32	RMSYNC	O	Receive Multi-frame Sync	Extracted multiframe sync; edge indicates start of multiframe. 50% duty cycle.
29	33	RABCD	O	Receive ABCD Signaling	Extracted signaling data output, valid for each channel time in signaling frames. In non-signaling frames, RABCD outputs the LSB of each channel word.
30	34	RSIGFR	O	Receive Signaling Frame	High during signaling frames, low during re-sync and non-signaling frames.
31	35	RSIGSEL	O	Receive Signaling Select	In 193E framing a .667 kHz clock which identifies signaling frames A and C. A 1.33 kHz clock in 193S framing.
33	37	$\overline{\text{RST}}$	I	Reset	High-low transition clears all internal registers and resets receive side counters. High-low-high transition initiates a receive resync.
34	38	RPOS	I	Receive Positive and Negative Inputs	Receive Bipolar Data Inputs are sampled on the falling edge of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.
35	39	RNEG	I		
36	40	RCL	O	Receive Carrier Loss	Receive Carrier Loss goes high if 32 consecutive "0's" appear at RPOS and RNEG. Goes low after next "1."
37	41	RBV	O	Receive Bipolar Violation	Receive Bipolar Violation goes high during accused bit tie at RSER if bipolar violation detected, low otherwise.
38	42	RFER	O	Receive Frame Error	Receive Frame Error. High during F-bit time when FT or FS errors occur (193S) or when FPS or CRC errors occur (193E). Low during resync.
39	43	RLOS	O	Receive Loss of Sync	RLOS indicates sync status. Goes high when internal resync is in progress, low otherwise.

Table 5: Register Summary

Register	Address	Side[1]	Description / Function
RSR	0000	R[2]	Receive Status Register. Reports all receive alarm conditions.
RIMR	0001	R	Receive Interrupt Mask Register. Allows masking of individual alarm generated interrupts.
BVCR	0010	R	Bipolar Violation Count Register. An 8-bit presetable counter which records individual bipolar violations.
ECR	0011	R	Error Count Register. Two independent 4-bit counters which record OOF occurrences, and individual frame bit or CRC errors.
CCR[3]	0100	T/R	Common Control Register. Selects device operating characteristics common to receive and transmit sides.
RCR[3]	0101	R	Receive Control Register. Programs device operating characteristics unique to the receive side.
TCR[3]	0110	T	Transmit Control Register. Selects additional transmit side modes.
TIR1 TIR2 TIR3	0111 1000 1001	T T T	Transmit Idle Registers. Designate which outgoing channels are to be substituted with idle code.
TTR1 TTR2 TTR3	1010 1011 1100	T T T	Transmit Transparent Registers. Designate which outgoing channels are to be treated transparently. (No robbed bit signaling or bit 7 zero insertion.)
RMR1 RMR2 RMR3	1101 1110 1111	R R R	Receive Mark Registers. Designate which incoming channels are to be replaced with idle or digital milliwatt codes (under control of RCR).

Notes

[1] Transmit or Receive side register.

[2] RSR is a read-only register. All other registers are read/write.

[3] Reserved bit locations in control registers should be programmed to 0 to maintain compatibility with future transceiver products.

Operating Modes

In the Host mode, pins 14 through 18 comprise a microprocessor/microcontroller compatible serial port which can be used for device configuration, control and status monitoring.

In the Hardware mode no offboard processor is required. Pins 14 through 18 are re-configured into "Hardwired" select pins. Features such as selective "clear" DS0 channels, insertion of idle code and alteration of sync algorithm are unavailable in the Hardware mode.

Host Mode

Serial Port Interface

Pins 14 through 18 of the LXP2180A serve as a microprocessor/microcontroller compatible serial port. Sixteen onboard registers allow the user to update operational characteristics and monitor device status via a host controller, minimizing hardware interfaces. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads and/or writes by the host.

Address/Command Byte

Reading or writing the control, configuration or status registers requires writing one address/command byte (ACB) prior to transferring register data. As shown in Figure 2, the first bit written (LSB) of the address/command word specifies register read or write. The following 4-bit nibble identifies the register address. The next two bits are reserved and must be set to zero for proper operation. The last bit of the address/command word enables burst mode when set; the burst mode causes all registers to be consecutively written or read. Data is written to and read from the transceiver LSB first.

Chip Select and Clock Control

All data transfers are initiated by driving the $\overline{CS}$ input low. Input data is latched on the rising edge of SCLK and must be valid during the previous low period of SCLK to prevent momentary corruption of register data during writes. Data is output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated if the $\overline{CS}$ input transitions high. Port control logic is disabled and SDO tristated when $\overline{CS}$ is high.

Data I/O

Data I/O timing is shown in Figure 3. Following the eight SCLK cycles that input an address/command byte to write, a data byte is strobed into the addressed register on the rising edges of the next eight SCLK cycles. Following an address/command word to read, contents of the selected register are output on the falling edges of the next eight SCLK cycles. The SDO pin is tri-stated during device write, and may be tied to SDI in applications where the host processor has a bidirectional I/O pin.

Burst Mode

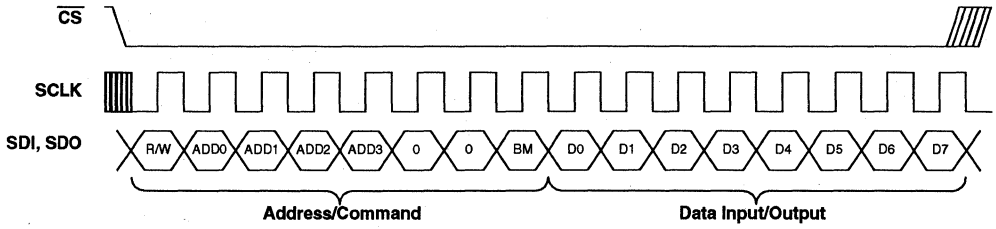
The burst mode allows all on-board registers to be consecutively read or written by the host processor. A burst read is used to poll all registers; RSR contents will be unaffected. This feature minimizes device initialization time on power-up or system reset. Burst mode is initiated when ACB.7 is set and the address nibble is 0000. Burst is terminated by low-high transition on $\overline{CS}$.

Figure 2: Address/Command Byte (ACB)

(MSB)							(LSB)
BM	–	–	ADD3	ADD2	ADD1	ADD0	R/W

Symbol	Position	Name And Description
BM	ACB.7	Burst Mode. If set (and ACB.1 through ACB.4 = 0) burst read or write is enabled.
–	ACB.6	Reserved. Must be set to 0 for proper operation.
–	ACB.5	Reserved. Must be set to 0 for proper operation.
ADD3	ACB.4	MSB of register address.
ADD0	ACB.1	LSB of register address.
R/$\overline{W}$	ACB.0	Read/Write Select. 0 = write addressed register. 1 = read addressed register.

Figure 3: Serial Port Read/Write



1. SDI sampled on rising edge of SCLK.
2. SDO updated on falling edge of SCLK.

Common Control Register

The Common Control Register (CCR) is shown in Figure 4.

Loopback

Enabling loopback will typically induce an Out Of Frame (OOF) condition. If appropriate bits are set in the receive control register (RCR), the receiver will resync to the looped transmit frame alignment. During the looped condition, the transmit outputs (TPOS, TNEG) will transmit all "1's" unframed. All operating modes (B8ZS, alarm, signaling, etc.) except for blue alarm transmission are available in loopback.

Bit Seven Stuffing

Existing systems meet ones density requirements by forcing bit 7 of all zero channels to 1. Bit 7 stuffing is globally enabled by asserting bit CCR.1, and may be disabled on an individual channel basis by setting appropriate bits in TTR1 - TTR3.

B8ZS

The LXP2180A supports existing and emerging zero suppression formats. Selection of B8ZS coding maintains system ones density requirements without disturbing data integrity as required in emerging clear channel applications. B8ZS coding replaces eight consecutive outgoing zeros with a B8ZS code word. Any received B8ZS code word is replaced with all zeros.

Figure 4: Common Control Register

(MSB)							(LSB)
–	FRSR2	EYELMD	FM	SYELMD	B8ZS	B7	LPBK

Symbol	Position	Name And Description
–	CCR.7	Reserved. Must be set to 0 for proper operation.
FRSR2	CCR.6	Function of Rec Status Register 2. 0 = Detected B8ZS code words reported at RSR.2. 1 = Change of Frame Alignment (COFA) reported at RSR.2 when last resync resulted in change of frame or multiframe alignment.
EYELMD	CCR.5	193E Yellow Mode Select. 0 = Yellow alarm is a repeating pattern set of 00 hex and FF hex. 1 = Yellow alarm is a "0" in the bit 2 position of all channels.
FM	CCR.4	Frame Mode Select. 0 = D4 (193S, 12 frames/superframe). 1 = Extended (193E, 24 frames/superframe)
SYELMD	CCR.3	193S Yellow Mode Select. Determines yellow alarm type to be transmitted and detected while in 193S framing. If set, yellow alarms are a "1" in the S-bit position of frame 12. If cleared, yellow alarm is a "0" in bit 2 of all channels. Does not affect 193E yellow alarm operation.
B8ZS	CCR.2	Bipolar Eight Zero Suppression. 0 = No B8ZS. 1 = B8ZS enabled.
B7	CCR.1	Bit Seven Zero Suppression. If CCR.1 = 1, channels with an all zero content will be transmitted with bit 7 forced to "1." If CCR.1 = 0, no bit 7 stuffing occurs.
LPBK	CCR.0	Loopback. When set, the device internally loops output transmit data into the incoming receive data buffers and TCLK is internally substituted for RCLK.

Transmit Control Register

The Transmit Control Register (TCR) is shown in Figure 5.

Transmit Blue Alarm

The blue alarm, also known as the Alarm Indication Signal (AIS), is an unframed, all 1's sequence enabled by asserting TCR.1. Blue alarm overrides all other transmit data patterns and is disabled by clearing TCR.1. Use of the TIR registers allows an unframed, all 1's alarm transmission if required by the network.

Transmit Yellow Alarm

In 193E framing, a yellow alarm is a repeating pattern set of FF (Hex) and 00 (Hex) on the 4 kHz facility data link (FDL). In 193S framing, the yellow alarm format is dependent on the state of bit CCR.3. In all modes, yellow alarm is enabled by asserting TCR.0 and disabled by clearing TCR.0.

Transmit Signaling

When enabled via TCR.4, channel signaling is inserted in frames 6 and 12 (193S); or 6, 12, 18 and 24 (193E) in the 8th bit position of every channel word. Signaling data is sampled at TABCD on the falling edge of TCLK during bit 8 of each input word during signaling frames. Logical combination of clocks TMO, TSIGFR and TSIGSEL allow external multiplexing of separate links for A, B or A, B, C, D signaling sources.

Transmit Transparency Registers

The Transmit Transparency Registers, TTR1 - TTR3, are shown in Figure 6. Individual DS0 channels in the T1 frame

Figure 5: Transmit Control Register

(MSB)							(LSB)
ODF	TFPT	TCP	RBSE	TIS	193SI	TBL	TYEL

Symbol	Position	Name And Description
ODF	TCR.7	Output Data Format. 0 = Bipolar data at TPOS and TNEG. 1 = NRZ data at TPOS; TNEG = 0.
TFPT	TCR.6	Transmit Framing Pass Through. 0 = FT/FPS sourced internally. 1 = FT/FPS sampled at TSER during F-bit time.
TCP	TCR.5	Transmit CRC Pass Through. 0 = Transmit CRC code internally generated. 1 = TSER sampled at CRC F-bit time for external CRC insertion.
RBSE	TCR.4	Robbed Bit Signaling Enable. 1 = signaling inserted in all channels during signaling frames. 0 = No signaling inserted. (The TTR registers allow the user to disable signaling insertion on selected DS0 channels.)
TIS	TCR.3	Transmit Idle Code Select. Determines idle code format to be inserted into channels marked by the TIR registers. 0 = insert 7F (Hex) into marked channels. 1 = insert FF (Hex) into marked channels.
193SI	TCR.2	193S S-bit Insertion. Determines source of transmitted S-bit. 0 = internal S-bit generator. 1 = external (sampled at TLINK input).
TBL	TCR.1	Transmit Blue Alarm. 0 = disabled. 1 = enabled.
TYEL	TCR.0	Transmit Yellow Alarm. 0 = disabled. 1 = enabled.

may be programmed clear (no inserted robbed bit signaling and no bit 7 zero suppression) by setting the appropriate bits in the TTR registers. Channel transparency is required in mixed voice/data and data-only environments such as ISDN, where data integrity must be maintained.

Transmit Idle Code Insertion

The Transmit Idle Registers, TIR1 - TIR3, are shown in Figure 7. Individual outgoing channel in the frame can be programmed with idle code by asserting the appropriate bits in the transmit idle registers. One of two idle code formats, 7F (Hex) and FF (Hex) may be selected by the user via TCR.3. If enabled, robbed bit signaling data is inserted into the idle channel, unless the appropriate TTR bit is set for that channel. This feature eliminates external hardware currently required to intercept and stuff unoccupied channels in the DS1 bit stream. Transmit insertion hierarchy is shown in Figure 8.

Transmit Multiframe Timing

Transmit multiframe timing for 193S framing and 193E framing is shown in Figures 9 and 10, respectively. Transmit multiframe boundary timing is shown in Figure 11.

Figure 6: Transmit Transparency Registers

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TTR1
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TTR2
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TTR3

Symbol	Position	Name And Description
CH24	TTR3.7	Transmit Transparency Registers. Each of these bit positions represents a DS0 channel in the outgoing frame. When set, the corresponding channel is transparent.
CH1	TTR1.0	

Figure 7: Transmit Idle Registers

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3

Symbol	Position	Name And Description
CH24	TIR3.7	Transmit Idle Registers. Each of these bit positions represents a DS0 channel in the outgoing frame. When set, the corresponding channel will output an idle code format determined by TCR.3.
CH1	TIR1.0	

Figure 8: Transmit Insertion Hierarchy

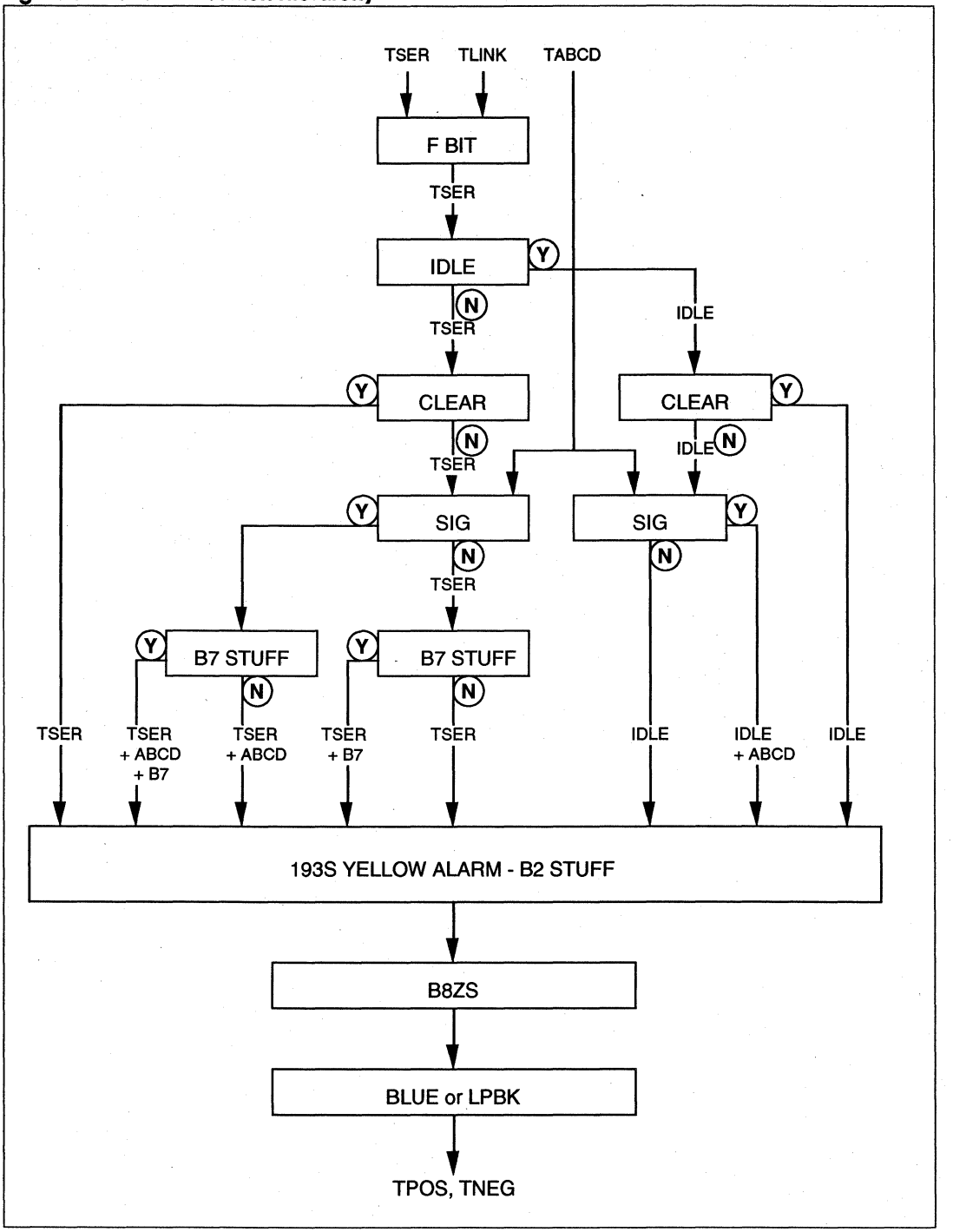
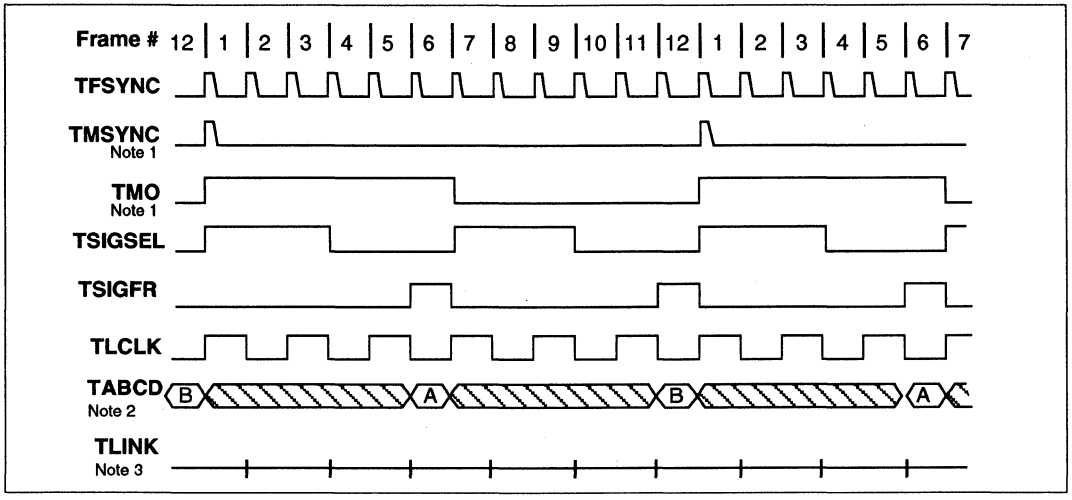
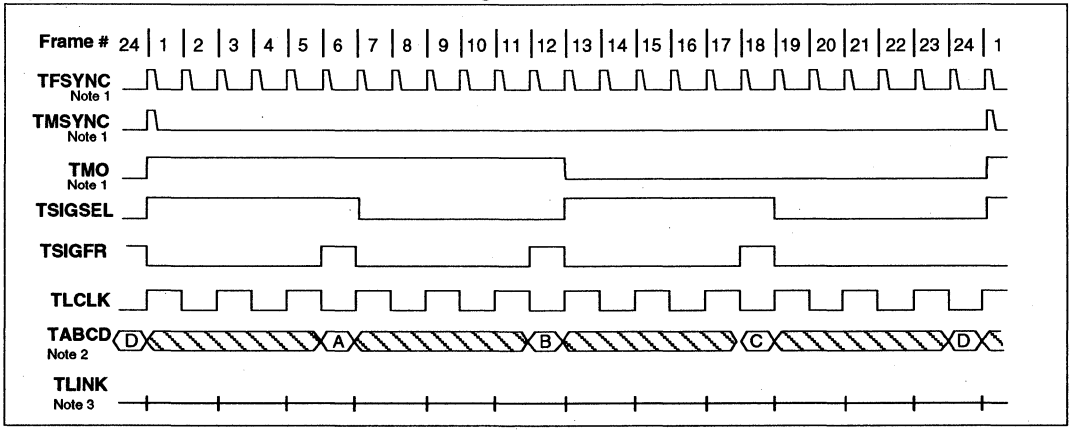


Figure 9: 193S Transmit Multiframe Timing



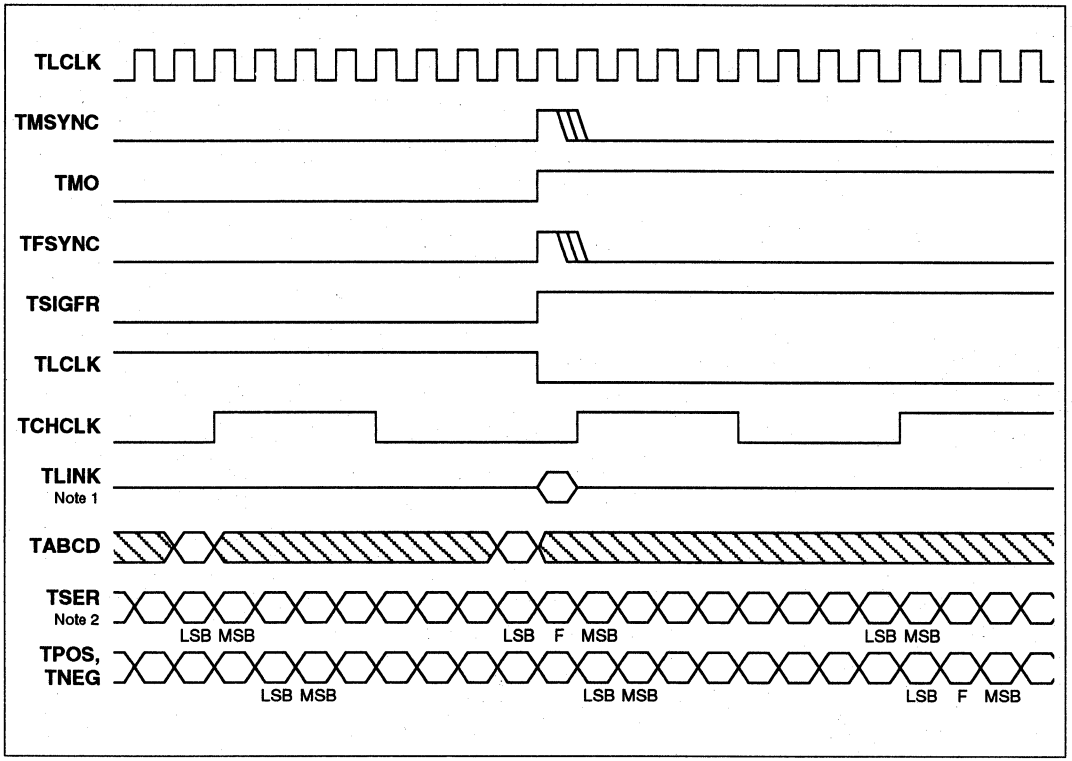
1. Transmit frame and multiframe timing may be established in one of four ways:
   a. With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries, allowing internal counters to determine frame timing.
   b. TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.
   c. TMSYNC and TFSYNC may be continuously pulsed to establish and reinforce frame and superframe timing.
   d. If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.
2. Channels in which robbed bit signaling is enabled will sample TABCD during the LSB bit time in frames indicated.
3. When external S-bit insertion is enabled, TLINK will be sampled during the F-bit time of even frames and inserted into the outgoing data stream.

Figure 10: 193E Transmit Multiframe Timing



1. Transmit frame and multiframe timing may be established in one of four ways:
   a. With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries, allowing internal counters to determine frame timing.
   b. TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.
   c. TMSYNC and TFSYNC may be continuously pulsed to establish and reinforce frame and superframe timing.
   d. If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.
2. Channels in which robbed bit signaling is enabled will sample TABCD during the LSB bit time in frames indicated.
3. TLINK is sampled during the F-bit time of odd frames and inserted into the outgoing data stream (FDL data).

Figure 11: Transmit Multiframe Boundary Timing



1. TLINK timing shown is for 193E framing. In 193E framing, TLINK is sampled as indicated for insertion into F-bit position of odd frames. When S-bit insertion is enabled in 193S framing, TLINK is sampled during even frames.
2. If TCR.5 = 1, TSER is sampled during the F-bit time of CRC frames for insertion into the outgoing data stream (193E framing only).

Receive Control Register

The Receive Control Register (RCR) is shown in Figure 12.

Receive Code Insertion

Incoming receive channels can be replaced with idle (Hex 7F) or digital milliwatt (u-Law format) codes. The Receive Mark Registers (RMR 1 - RMR3) indicate which channels are inserted. RMR registers are shown in Figure 13. When set, bit RCR.5 serves as a global enable for marked channels, and bit RCR.4 selects inserted code format: 0 = idle code, 1 = digital milliwatt.

Receive Synchronizer

Bits RCR.0 through RCR.3 allow the user to control operational characteristics of the synchronizer. Sync algorithm, candidate qualify testing, auto resync, and command resync modes may be altered at any time in response to changing span conditions.

Figure 12: Receive Control Register

(MSB)							(LSB)
ARC	OOF	RCI	RCS	SYNCC	SYNCT	SYNCE	RESYNC

Symbol	Position	Name And Description
ARC	RCR.7	Auto Resync Criteria. 0 = Resync on OOF or RCL event. 1 = resync on OOF only.
OOF	RCR.6	Out-Of-Frame Condition Detection. 0 = two of four framing bits in error. 1 = two of five framing bits in error.
RCI	RCR.5	Receive Code Insert. When set, the receive code selected by RCR.4 is inserted into channels marked by RMR registers. If clear, no code is inserted.
RCS	RCR.4	Receive Code Select. 0 = idle code. 1 = digital Milliwatt.
SYNCC	RCR.3	Sync Criteria. Determines the type of algorithm used by the receive synchronizer and differs for each frame mode. **193S Framing** (CCR.4 = 0). 0 = synchronize to frame boundaries using F_T pattern, then search for multiframe using F_S. 1 = cross couple F_T and F_S patterns in sync algorithm. **193E Framing** (CCR.4 = 1). 0 = normal sync (uses FPS only). 1 = validate new alignment with CRC before declaring sync.
SYNCT	RCR.2	Sync Time. If set, 24 consecutive F-bits of the framing pattern must be qualified before sync is declared. If clear, 10 bits are qualified.
SYNCE	RCR.1	Sync Enable. If clear, the transceiver will automatically begin a resync if two of the previous four or five framing bits were in error, or if carrier loss is detected. If set, no auto resync occurs.
RESYNC	RCR.0	Resync. When toggled low to high, the transceiver will initiate resync immediately. The bit must be cleared, then set again for subsequent resyncs.

Receive Signaling

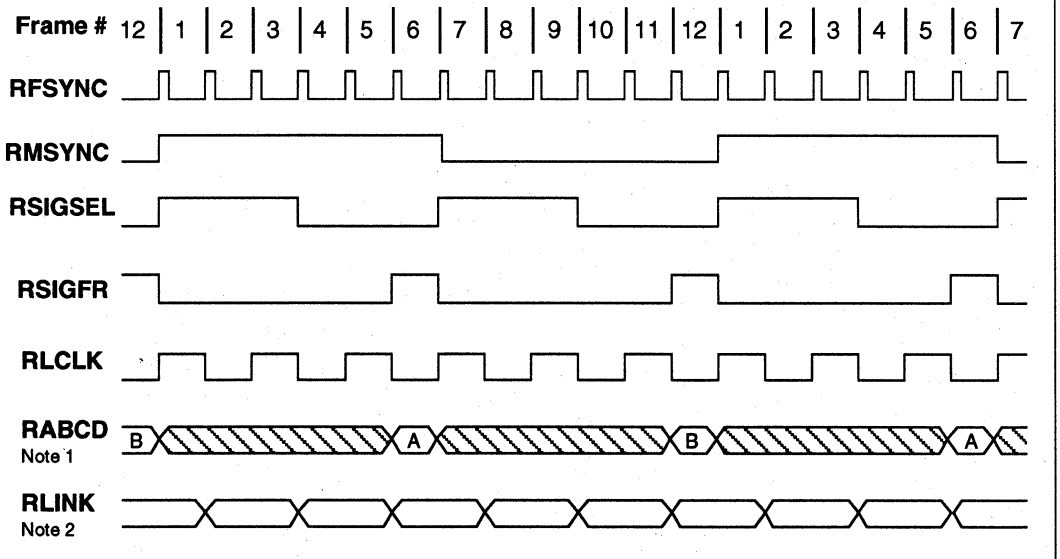
Robbed bit signaling data is presented at RABCD during each channel time in signaling frames for all 24 incoming channels. Logical combination of clocks RMSYNC, RSIGFR and RSIGSEL allow the user to identify and extract AB or ABCD signaling data. Receive multiframe timing for 193S and 193E framing modes are shown in Figures 14 and 15, respectively. Receive multiframe boundary timing is shown in Figure 16.

Figure 13: Receive Mark Registers

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RMR1
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RMR2
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RMR3

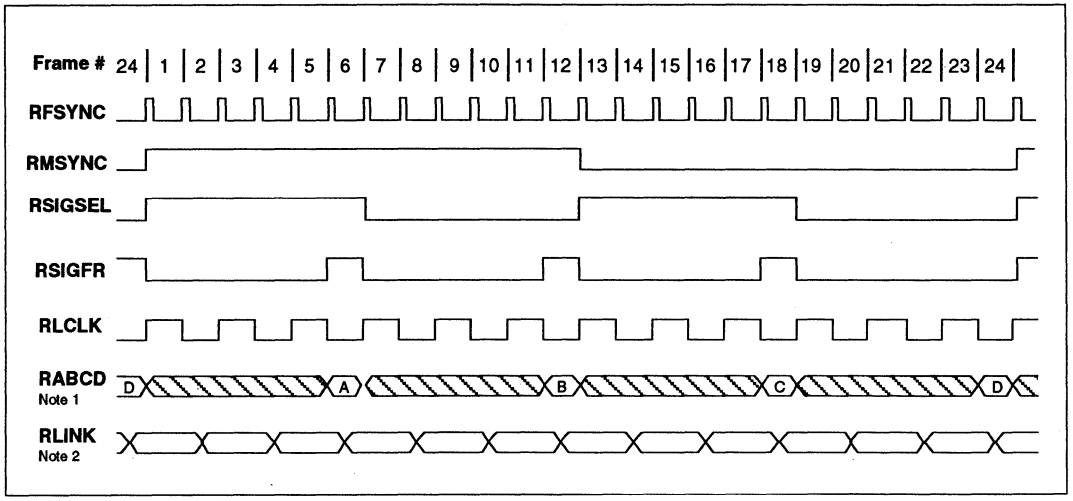
Symbol	Position	Name And Description
CH24	RMR3.7	Receive Mark Registers. Each of these bit positions represents a DS0 channel in the incoming T1 frame. When set, the corresponding channel will output codes determined by RCR.4 and RCR.5.
CH1	RMR1.0	

Figure 14: 193S Receive Multiframe Timing



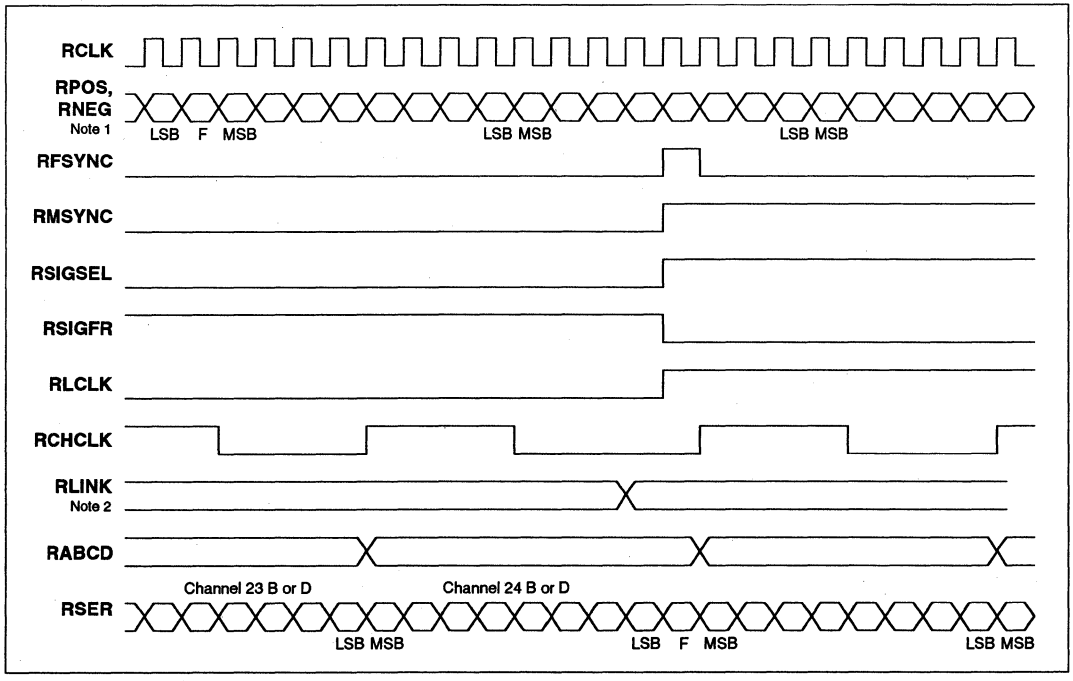
1. Signaling data is updated during signaling frames on channel boundaries. RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (S-bit) is updated one bit time prior to S-bit frames and held for two frames.

Figure 15: 193E Receive Multiframe Timing



1. Signaling data is updated during signaling frames on channel boundaries. RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (FDL-bit) is updated one bit time prior to odd frames and held for two frames.

Figure 16: Receive Multiframe Boundary Timing



1. Total delay from RPOS and RNEG to RSER output is 13 RCLK periods.
2. RLINK timing shown is for 193E timing. In 193S timing, RLINK is updated on even frame boundaries and is held across multiframe edges.

Receive Alarm Reporting

Incoming serial data is monitored by the transceiver for alarm occurrence. Alarm conditions are reported in two ways: (1) via transition on the alarm output pins; and (2) registered interrupt, in which the host controller reads the Receive Status Register (RSR) in response to an alarm driven interrupt. The RSR register is shown in Figure 17. Interrupts may be direct, in which the transceiver demands service for a real time alarm, or count-overflow triggered, in which an on-board alarm event counter exceeds a user-programmed threshold. The user may mask individual alarm conditions by clearing the appropriate bits in the receive interrupt mask register (RIMR). The RIMR register is shown in Figure 18.

Alarm Servicing

The host controller must service the transceiver in order to clear an interrupt condition. Clearing appropriate bits in the RIMR will unconditionally clear an interrupt. Direct interrupts (those driven from real-time alarms) will be cleared when the RSR is directly read, unless the alarm condition still exists. Count-overflow interrupts (BVCS, FCS) are not cleared by a direct read of the RSR. They will be cleared only when the user presets the appropriate count register to a value other than all "1's." A burst read of the RSR will not clear an interrupt condition.

Alarm Counters

The three on-board alarm event counters (BPV, OOF, and ESF) allow the transceiver to monitor and record error events without processor intervention on each event occurrence. All of these counters are presetable by the user, establishing an event count interrupt threshold. As each counter saturates, the next error event occurrence will set a bit in the RSR and generate an interrupt unless masked. The user may read these registers at any time; in many systems, the host will periodically poll these registers to establish link error rate performance.

Figure 17: Receive Status Register (RSR)

(MSB)							(LSB)
BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

Symbol	Position	Name And Description
BVCS	RSR.7	Bipolar Violation Count Saturation. Set when the 8-bit counter at BVCR saturates.
ECS	RSR.6	Error Count Saturation. Set when either of the 4-bit counters at ECR saturates.
RYEL	RSR.5	Receive Yellow Alarm. Set when yellow alarm detected. (Detected yellow alarm format determined by CCR.4 and CCR.3.)
RCL	RSR.4	Receive Carrier Loss. Set when 32 consecutive "0's" appear at RPOS and RNEG.
FERR	RSR.3	Frame Bit Error. Set when F_T (193S) or FPS (193E) bit error occurs.
B8ZSD	RSR.2	Bipolar Eight Zero Substitution Detect. Set when B8ZS code word detected.
RBL	RSR.1	Receive Blue Alarm. Set when two consecutive frames have less than three zeros (total) in the data stream (F-bit positions not tested).
RLOS	RSR.0	Receive Loss of Sync. Set when resync is in progress; if RCR.1 = 0, RLOS transitions high on an OOF event or carrier loss, indicating auto resync.

BVCR - Bipolar Violation Count Register

The BVCR register is shown in Figure 19. This 8-bit binary up counter saturates at 255 and will generate an interrupt for each occurrence of a bipolar violation once saturated (RIMR.7 = 1). Presetting this register allows the user to establish specific count interrupt thresholds. The counter will count "up" to saturation from the preset value, and may be read at any time. Counter increments occur at all times and are not disabled by resync.

Figure 18: Receive Interrupt Mask Register (RIMR)

(MSB)							(LSB)
BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

Symbol	Position	Name And Description
BVCS	RIMR.7	Bipolar Violation Count Saturation Mask. 1 = interrupt enabled. 0 = interrupt masked.
ECS	RIMR.6	Error Count Saturation Mask. 1 = interrupt enabled. 0 = interrupt masked.
RYEL	RIMR.5	Receive Yellow Alarm Mask. 1 = interrupt enabled. 0 = interrupt masked.
RCL	RIMR.4	Receive Carrier Loss Mask. 1 = interrupt enabled. 0 = interrupt masked.
FERR	RIMR.3	Frame Bit Error Mask. 1 = interrupt enabled. 0 = interrupt masked.
B8ZSD	RIMR.2	Bipolar Eight Zero Substitution Detect Mask. 1 = interrupt enabled. 0 = interrupt masked.
RBL	RIMR.1	Receive Blue Alarm Mask. 1 = interrupt enabled. 0 = interrupt masked.
RLOS	RIMR.0	Receive Loss of Sync Mask. 1 = interrupt enabled. 0 = interrupt masked.

Figure 19: Bipolar Violation Count Register (BVCR)

(MSB)							(LSB)
BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0

Symbol	Position	Name And Description
BVD7	BVCR.7	MSB of bipolar violation count.
BVD0	BVCR.0	LSB of bipolar violation count.

Error Count Register - Out Of Frame and Errored Superframe Events

These separate 4-bit binary up counters saturate at a count of 15 and will generate an interrupt for each occurrence of an OOF event or an ESF event after saturation (RIMR.6 = 1). Presetting these counters allows the user to establish specific count interrupt thresholds. The counters will count up to saturation from the preset value, and may be read at any time. These counters share the same register address, and must be written to or read from simultaneously.

Out Of Frame (OOF) is declared when at least two of four (or five) consecutive framing bits are in error. F_T bits are tested for OOF occurrence in 193S; the FPS bits are tested in 193E. OOF events are recorded by the 4-bit OOF counter in the error count register. The OOF counter records out of frame events in both 193S and 193E. In the 193E framing mode, the OOF event is logically "OR'ed" with an on-chip generated CRC checksum. This event, known as errored superframe, is recorded by the 4-bit ESF error counter in the error count register. In the 193S framing mode, the 4-bit ESF counter records individual F_T and F_S errors when RCR.3 = 1, or F_T errors only when RCR.3 = 0. ECR counter increments are disabled when resync is in progress (RLOS high).

Alarm Outputs

The transceiver also provides direct alarm outputs for applications when additional decoding and demuxing are required to supplement the on-board alarm logic. Alarm output timing is shown in Figure 21.

RLOS Output

The receive loss of sync output indicates the status of the receiver synchronizer circuitry: when high, an off-line resynchronization is in progress and a high-low transition indicates resync is complete. The RLOS bit (RSR.0) is a latched version of the RLOS output. If the auto-resync mode is selected (RCR.1 = 0) RLOS is a real time indication of a carrier loss or OOF event occurrence.

RYEL Output

The yellow alarm output transitions high when a yellow alarm is detected. A high-low transition indicates the alarm condition has been cleared. The RYEL bit (RSR.5) is a latched version of the RYEL output. In 193E framing, the yellow alarm pattern detected is 16 pattern sets of 00 (Hex) and FF (Hex) received at RLINK. In 193S framing, the yellow alarm format is dependent on CCR.3: if CCR.3 = 0, the RYEL output transitions high if bit 2 of the 256 or more consecutive channels is 0; If CCR.3 = 1, yellow alarm is declared when the S-bit received in frame 12 is 1.

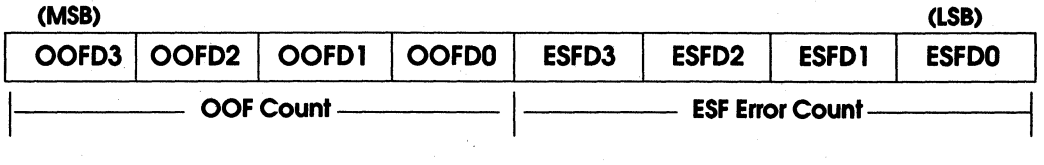
RBV output

The bipolar violation output transitions high when the accused bit emerges at RSER. RBV will go low at the next bit time if no additional violations are detected.

RFER Output

The receive frame error output transitions high at the F-bit time and is held high for two bit periods when a frame error

Figure 20: Error Count Register (ECR)



Symbol	Position	Name And Description
OOFD3	ECR.7	MSB of OOF event count.
OOFD0	ECR.4	LSB of OOF event count.
ESFD3	ECR.3	MSB of ESF error count.
ESFD0	ECR.0	LSB of ESF error count.

occurs. In 193S framing, F_T and F_S patterns are tested. The FPS pattern is tested in 193E framing. Additionally, in 193E framing, RFER reports a CRC error by a low-high-low transition (one bit period wide) one half RCLK period before a low-high transition on RMSYNC.

Reset

A high-low transition on $\overline{RST}$ clears all registers and forces immediate receive resync when $\overline{RST}$ returns high. This reset has no effect on transmit frame, multiframe, or channel counters. $\overline{RST}$ must be held low on system power-up to insure proper initialization of transceiver counters and registers. Following reset, the host processor should restore all control modes by writing appropriate registers with control data.

Hardware Mode

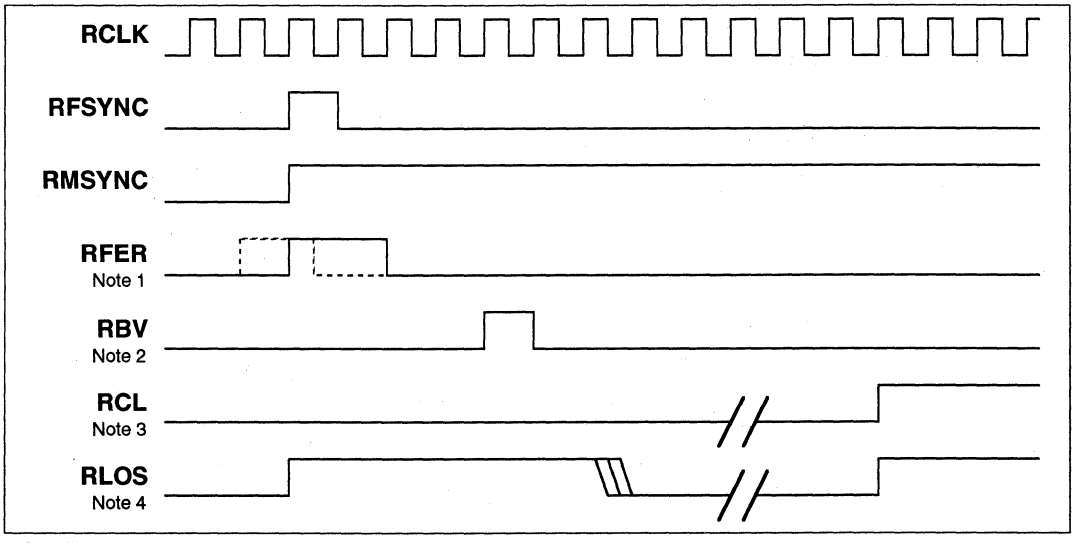
For preliminary system prototyping or applications which do not require the features offered by the serial port, the transceiver can be reconfigured by the SPS pin. Tying SPS to VSS disables the serial port, clears all internal registers except CCR and TCR and redefines pins 14 through 18 as mode control inputs. Hardware mode control inputs are listed in Table 6. The Hardware mode allows device retrofit into existing applications where mode control and alarm conditioning circuits are often designed with discrete logic.

Hardware Common Control

In the Hardware mode bits TCR.2, CCR.4, TCR.0, CCR.1 and CCR.2 map to pins 14 through 18. The loopback feature (bit CCR.0) is enabled by tying pins 17 (zero suppression) and 18 (B8ZS) to 1. (The last states of pins 17 and 18 are latched as when both pins are taken high, preserving the current zero suppression mode). Robbed bit signaling (bit TCR.4) is enabled for all channels. The user may tie TSER to TABCD externally to disable signaling if so desired. Bit CCR.3 is forced to 0, which selects bit 2 yellow alarm in 193S framing. Contents of the RCR, as well as the remaining bit locations in the CCR and TCR, are cleared in the Hardware mode. The $\overline{RST}$ input may be used to force immediate receiver resync, and has no effect on transmit.

2

Figure 21: Alarm Output Timing



NOTES:

1. RFER transitions high during F-bit time if received framing pattern bit is in error. (Frame 12 F-bits in 193S are ignored if CCR.3 = 1.) Also, in 193E, RFER transitions ½ bit time before the rising edge of RMSYNC to indicate a CRC error for the previous multiframe.
2. RBV indicates received bipolar violations and transitions high when accused bit emerges from RSER. If B8ZS is enabled, RBV will not report the zero replacement code.
3. RCL transitions high (during 32nd bit time) when 32 consecutive bits received are "0". RCL transitions low when the next "1" is received.
4. RLOS transitions high during the F-bit time that caused an OOF event (any 2 of 4 consecutive FT or FPS bits are in error) if auto-resync mode is selected (RCR.1 = 0). Resync will also occur when loss of carrier is detected (RCL = 1). When RCR.1 = 1, RLOS remains low until resync occurs, regardless of OOF or carrier loss flags. In this situation, resync is initiated only when RCR.0 transitions low-to-high or the $\overline{RST}$ pin transitions high-low-high.

T1 OVERVIEW

Framing Standards

The LXP2180A is compatible with the existing Bell System D4 framing standard described in AT&T PUB 43801 and the new extended superframe format (ESF) as described in AT&T C.B. #142. In this document, D4 framing is referred to as 193S, and ESF (also known as Fe) is referred to as 193E. Programmable features of the LXP2180A allow support of other framing standards which are derivatives of 193E and 193S. The salient differences between the 193S and 193E formats are the number of frames per superframe and use of the F-bit position (refer to Tables 7 and 8). In 193S, 12 frames make up a superframe; in 193E, 24. A frame consists of 24 channels (time-slots) of 8-bit data preceded by an F-bit. Channel data is transmitted and received MSB first.

F-Bits

The use of the F-bit position in 193S is split between the terminal framing pattern (known as F_T-Bits) which provides frame alignment information, and the signaling framing pattern (known as F_S-bits) which provides multiframe alignment information. In 193E framing, the F-bit position is shared by the framing pattern sequence (FPS), which provides frame and multiframe alignment information, a 4 kHz data link (Facility data link) known as FDL, and CRC (cyclic redundancy check) bits. The FDL bits are used for control and maintenance (inserted by the user at TLINK). The CRC bits are an indicator of link quality and may be monitored by the user to establish error performance.

Signaling

During frames 6 and 12 in 193S, A and B signaling information is inserted into the LSB of all channels transmitted. In 193E, A and B data is inserted into frames 6 and 12; C and D data is inserted into frames 18 and 24. This allows a maximum of four signaling states to be transmitted per superframe in 193S; 16 states per superframe in 193E.

Alarms

The LXP2180A supports all alarm pattern generation and detection required in typical Bell System applications. These alarm modes are explained in AT&T PUB 43801, AT&T C. B. #142 and elsewhere in this document.

Line Coding

T1 line data is transmitted in a bipolar alternate mark inversion (AMI) line format; ones are transmitted as alternating negative and positive pulses and zeros are simply the absence of pulses. This technique minimizes DC voltage on the T1 span and allows clock to be extracted from data. The network currently has a one's density constraint to keep clock extraction circuitry functioning, which is usually met by forcing bit 7 of any channel consisting of all 0's to 1. The use of Bipolar Eight Zero Substitution (B8ZS) satisfies all the ones density requirements, while allowing data traffic to be transmitted without corruption. This feature is known as clear channel and is explained more completely in AT&T C.B. #144. When the B8ZS feature is enabled, any outgoing stream of eight consecutive zeros is replaced with a B8ZS code word. If the last "one" transmitted was positive, the

Table 6: Hardware Mode Pin Descriptions

Pin #	Register Bit Location	Name and Description
14	TCR-D2	193S - S-bit Insertion[1]. 1 = external; 0 = internal
15	CCR-D4	Framing Mode Select. 1 = 193E; 0 = 193S
16	TCR-D0	Transmit Yellow Alarm[2,3]. 1 = enabled; 0 = disabled
17	CCR-D1	Zero Suppression[3]. 1 = bit 7 stuffing; 0 = transparent
18	CCR-D2	B8ZS[3]. 1 = enabled; 0 = disabled

NOTES:
1. S-bit yellow alarm (193S) is not internally supported; however, the user may elect to insert external S-bits for alarm purposes.
2. Bit 2 (193S) and data link (193E) yellow alarms are supported.
3. Tying pins 17 and 18 high enables loopback in the Hardware mode.

inserted code is 000 + - 0 - +; if negative, the code word inserted is 000 - + 0 + -. Bipolar violations occur in the fourth and seventh bit positions, which are ignored by the DS2180A error monitoring logic when B8ZS is enabled. Any received B8ZS code word is replaced with all 0's if B8ZS is enabled. Also, the receive status register will report any occurrence of B8ZS code words to the host controller. This allows the user to monitor the link for upgrade to clear channel capability, and respond to it. The B8ZS monitoring feature works at all times and is independent of the state of CCR.2.

TRANSMITTER OVERVIEW

The transmit side of the LXP2180A is made up of six major functional blocks: timing and clock generation, data selector, bipolar coder, yellow alarm, F-bit data and CRC. The timing and clock generation circuit develops all on-board and output clocks to the system from inputs TCLK, TFSYNC and TMSYNC. The yellow alarm circuitry generates mode dependent yellow alarms. The CRC block generates checksum results utilized in 193E framing. F-bit data provides mode dependent framing patterns and allows insertion of link or S-bit data externally. All of these blocks feed into the data selector, where (under control of the CCR, TCR, TIRs and TTRs) the contents of the outgoing data stream are established by bit selection and insertion. The bipolar coder formats the output of the data selector to make it compatible with bipolar transmission techniques and inserts zero suppression codes. The bipolar coder also supports the on-board loopback feature. Input-to-output delay of the transmitter is 10 TCLK cycles.

Table 7: 193E Framing Format

Frame #	F-Bit Use			Bit use In Each Channel		Signaling-Bit Use		
	FPS[1]	FDL[2]	CRC[3]	Data	Signaling[4, 5]	2-State	4-State	16-State
1	–	M	–	Bits 1 - 8				
2	–	–	C1	Bits 1 - 8				
3	–	M	–	Bits 1 - 8				
4	0	–	–	Bits 1 - 8				
5	–	M	–	Bits 1 - 8				
6	–	–	C2	Bits 1 - 7	Bit 8	A	A	A
7	–	M	–	Bits 1 - 8				
8	0	–	–	Bits 1 - 8				
9	–	M	–	Bits 1 - 8				
10	–	–	C3	Bits 1 - 8				
11	–	M	–	Bits 1 - 8				
12	1	–	–	Bits 1 - 7	Bit 8	A	B	B
13	–	M	–	Bits 1-8				
14	–	–	C4	Bits 1 - 8				
15	–	M	–	Bits 1 - 8				
16	0	–	–	Bits 1 - 8				
17	–	M	–	Bits 1 - 8				
18	–	–	C5	Bits 1 - 7	Bit 8	A	A	C
19	–	M	–	Bits 1-8				
20	1	–	–	Bits 1 - 8				
21	–	M	–	Bits 1 - 8				
22	–	–	C6	Bits 1 - 8				
23	–	M	–	Bits 1 - 8				
24	1	–	–	Bits 1 - 7	Bit 8	A	B	D

NOTES:
1. FPS - Framing Pattern Sequence.
2. FDL - 4 kHz Facility Data Link; M = message bits.
3. CRC - Cyclic Redundancy Check Bits. The CRC code will be internally generated by the device when TCR.5 = 0. When TCR.5 = 1, externally supplied CRC data will be sampled at TSER during the F-bit time of frames 2, 6, 10, 14, 18 and 22.
4. The user may program any individual channels clear, in which case Bit 8 will be used for data, not signaling.
5. Depending on application, the user can support 2-state, 4-state or 16-state signaling by the appropriate decodes of TMO, TSIGFR, TSIGSEL (transmit side) and RMSYNC, RSIGFR and RSIGSEL (receive side).

RECEIVER OVERVIEW

Synchronizer

The heart of the receiver is the synchronizer/sync monitor. This circuit serves two purposes: 1) monitoring the incoming data stream for loss of frame or multiframe alignment; and 2) searching for a new frame alignment pattern when sync loss is detected. When sync loss is detected, the synchronizer begins an off-line search for the new alignment; all output timing signals remain at the old alignment with the exception of RSIGFR, which is forced low during resync. When one and only one candidate is qualified, the output timing will move to the new alignment at the beginning of the next multiframe. One frame later, RLOS will transition low, indicating valid sync and the resumption of the normal sync monitoring mode. Several bits in the RCR allow tailoring of the resync algorithm by the user. These bits are described in the following paragraphs.

Sync Time (RCR.2)

Bit RCR.2 determines the number of consecutive framing pattern bits to be qualified before SYNC is declared. If RCR.2 = 1, the algorithm will validate 24 bits, if RCR.2 =0, 10 bits are validated. 24-bit testing results in superior false framing protection, while 10-bit testing minimizes reframe time (although in either case, the synchronizer will only establish resync when one and only one candidate is found).

Resync (RCR.0)

A zero-to-one transition of RCR.0 causes the synchronizer to search for the framing pattern sequence immediately, regardless of the internal sync status. In order to initiate another resync command, this bit must be cleared and then set again.

Sync Enable (RCR.1)

When RCR.1 is cleared, the receiver will initiate automatic resync if any of the following events occur:
1) an OOF event (Out-Of-Frame), or 2) carrier loss (32 consecutive 0's appear at RPOS and RNEG). An OOF event occurs any time that 2 of 4 F_T or FPS bits are in error. When RCR.1 is set, the automatic resync circuitry is disabled; in this case, resync can only be initiated by setting RCR.0 to 1, or externally via a low-high transition on $\overline{RST}$. Note that using $\overline{RST}$ to initiate resync resets the receive output timing while $\overline{RST}$ is low; use of RCR.1 does not affect output timing until the new alignment is located.

Sync Criteria (RCR.3)

193E Bit RCR.3 determines which sync algorithm is utilized when resync is in progress (RLOS = 1). In 193E framing, when RCR.3 = 0, the synchronizer will lock only to the FPS pattern and will move to the new frame and multiframe alignment after the framing candidate is

Table 8: 193S Framing Format

Frame #	F-Bit Use		Bit use In Each Channel		Signaling-Bit Use
	FT[1]	FS[2]	Data	Signaling[4]	
1	1	–	Bits 1 - 8		
2	–	0	Bits 1 - 8		
3	0	–	Bits 1 - 8		
4	–	0	Bits 1 - 8		
5	1	–	Bits 1 - 8		
6	–	1	Bits 1 - 7	Bit 8	A
7	0	–	Bits 1 - 8		
8	–	1	Bits 1 - 8		
9	1	–	Bits 1 - 8		
10	–	1	Bits 1 - 8		
11	0	–	Bits 1 - 8		
12	–	0[3]	Bits 1 - 7	Bit 8	B

NOTES:
1. FT (terminal framing) bits provide frame alignment information.
2. FS (signaling frame) bits provide multiframe alignment information.
3. The S-bit in frame 12 may be used for yellow alarm transmission and detection in some applications.
4. The user may program any individual channels clear, in which case Bit 8 will be used for data, not signaling.

qualified. RLOS will go low one frame after the move to the new alignment. When RCR.3 = 1, the new alignment is further tested by a CRC code match. RLOS will transition low after a CRC match occurs. If no CRC match occurs in three attempts (three multiframes), the algorithm will reset and a new search for the framing pattern begins. It takes 9 ms for the synchronizer to check the first CRC code after the new alignment has been loaded. Each additional CRC test takes 3 ms. Regardless of the state of RCR.3, if more than one candidate exists after about 24 ms, the synchronizer will begin eliminating emulators by testing their CRC codes online in order to find the true framing candidate.

193S In 193S framing, when RCR.3 = 1, the synchronizer will cross check the FT pattern with the FS pattern to help eliminate false framing candidates such as digital milliwatts. The FS patterns are compared to the repeating pattern . . . 00111000111000 . . . (001llX0 if CCR.3—YELMD—is equal to a 1). In this mode, FT and FS patterns must be correctly identified by the synchronizer before sync is declared. Clearing RCR.3 causes the synchronizer to search for FT patterns (101010 . . .) without cross-coupling the FS pattern. Frame sync will be established using the FT information, while multiframe sync will be established only if valid FS information is present. If no valid FS pattern is identified, the synchronizer will move to the FT alignment, RLOS will go low, and a false multiframe position may be indicated by RMSYNC. RFER will indicate when the received S-bit pattern does not match the assumed internal multiframe alignment. This mode can be used in applications where non-standard S-bit patterns exist. In such applications, multiframe alignment information can be decoded externally by using the S-bits present at RLINK.

APPLICATIONS

Backplane Interface

A typical backplane interface circuit is shown in Figure 22. The LXP2180A is shown in Host mode with an LXP2176 providing the interface to the backplane, and an LXT300 providing the line interface.

Processor-Based Signaling

Many robbed-bit signaling applications utilize a microprocessor to insert transmit signaling data into the outgoing data stream. The circuit shown in Figure 23 decouples the processor timing from that of the LXP2180A by use of a small FIFO memory. The processor writes to the FIFO (6 bytes are written: 3 for A data, 3 for B data) only when signaling updates are required. The FIFO automatically retransmits old data when no updates occur. The system is interrupt-driven from the transmit multiframe sync input; the processor must update the FIFO prior to Frame 6 (625 µs after interrupt) to prevent data corruption. The application circuit shown supports 193S framing; additional hardware is required for 193E applications.

Table 9: Average Reframe Time[1]

Frame Mode	RCR.2 = 0			RCR.2 = 1			Units
	Min	Avg	Max	Min	Avg	Max	
193S	3.0	3.75	4.5	6.5	7.25	8.0	ms
193E	6.0	7.5	9.0	13.0	14.5	16.0	ms

NOTES:
1. Average Reframe Time is defined here as the average time it takes from the start of resync (rising edge of RLOS) to the actual loading of the new alignment (on a multiframe edge) into the output receive timing.

Figure 22: Backplane Interface Application using LXP2180A with LXP2176

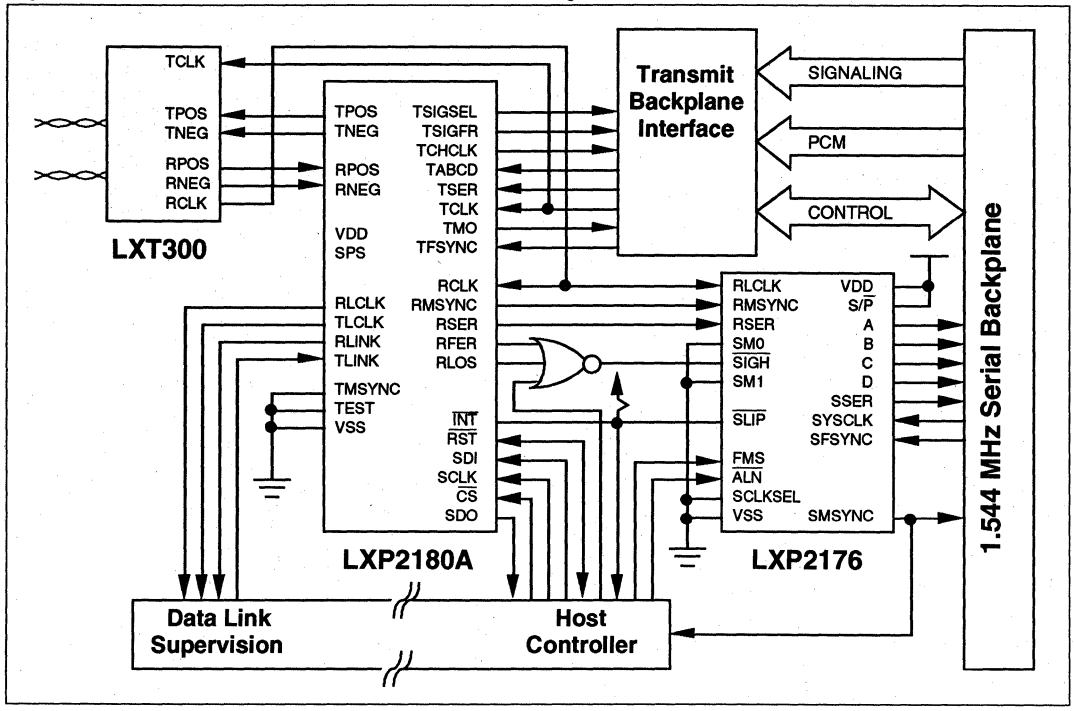
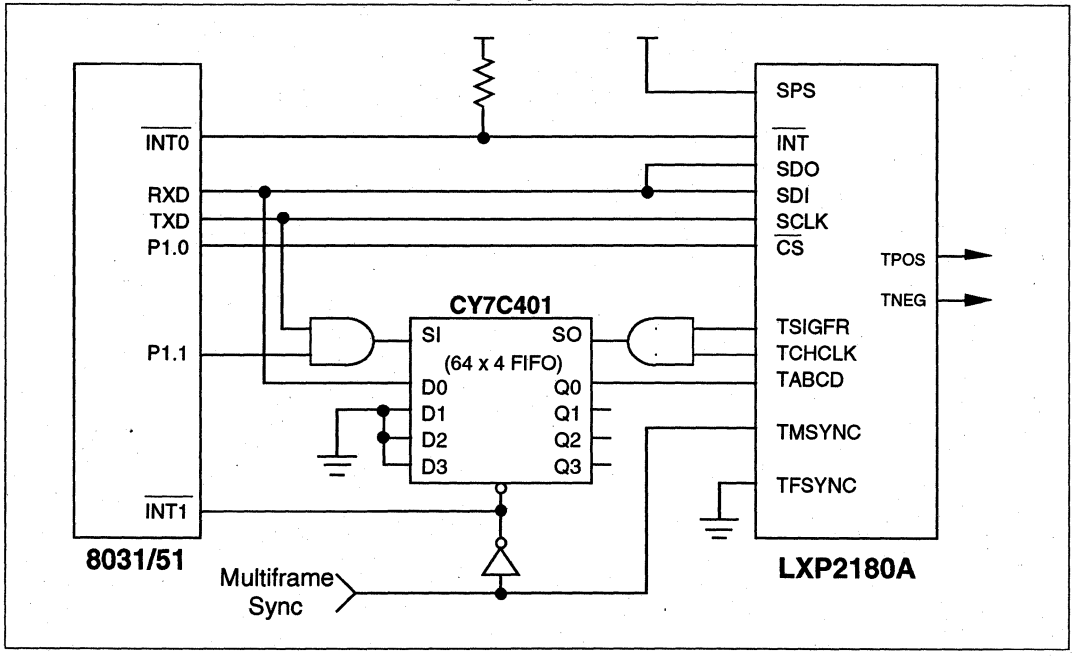


Figure 23: Processor-Based Transmit Signaling Insertion Application



LEVEL ONE®

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- Voltage on any pin relative to ground -1.0V to + 7V
- Operating temperature -40 °C (min) to +85 °C (max)
- Storage temperature -55 °C (min) to +125 °C (max)
- Soldering temperature 260 °C for 10 seconds

Recommended Operating Conditions (Voltages are with respect to ground (GND) unless otherwise stated)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Logic 1	V_{IH}	2.0	–	V_{DD} + .3	V	
Logic 0	V_{IL}	-0.3	–	+0.8	V	
Supply voltage	V_{DD}	4.5	5	5.5	V	
Capacitance						
Input capacitance	C_{IN}	–	–	5	pF	
Output capacitance	C_{OUT}	–	–	7	pF	
DC Electrical Characteristics - Clocked operation over recommended temperature and power supply ranges						
Supply current	I_{DD}	–	3	10	mA	See Notes 2 and 3
Input leakage	I_{IL}	–	–	1	µA	
Output leakage	I_{OL}	–	–	1	µA	See Note 4
Output high current	I_{OH}	-1	–	–	mA	V_{OH} = 2.4 V, See Note 5
Output low current	I_{OL}	+4	–	-	mA	V_{OL} = 0.4 V, See Note 6

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] TCLK = RCLK = 1.544 MHz
[3] Outputs open.
[4] Applies to SDO when tristated.
[5] All outputs except INT, which is open collector.
[6] All outputs.

A.C. Electrical Characteristics - Serial Port

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions[2]
SDI to SCLK Setup	t_{DC}	50	–	–	ns	C load = 100 pF
SCLK to SDI Hold	t_{CDH}	50	–	–	ns	C load = 100 pF
SDI to SCLK Falling Edge	t_{CD}	50	–	–	ns	C load = 100 pF
SCLK Low Time	t_{CL}	250	–	–	ns	C load = 100 pF
SCLK High Time	t_{CH}	250	–	–	ns	C load = 100 pF
SCLK Rise and Fall Time	t_F, t_F	–	–	500	ns	C load = 100 pF
$\overline{CS}$ to SCLK Setup	t_{CC}	50	–	–	ns	C load = 100 pF
SCLK to $\overline{CS}$ Hold	t_{CCH}	50	–	–	ns	C load = 100 pF
$\overline{CS}$ Inactive Time	t_{CWH}	250	–	–	ns	C load = 100 pF
SCLK to SDO Valid	t_{CDV}	–	–	200	ns	C load = 100 pF
$\overline{CS}$ to SDO High Z	t_{CDZ}	–	–	75	ns	C load = 100 pF
SCLK Setup to $\overline{CS}$ Falling	t_{SSC}	50	–	–	ns	C load = 100 pF

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Measured at V_{IH} = 2.0V, V_{IL} = .8V, and 10 ns maximum rise and fall time.

Figure 24: Serial Port Write A.C. Timing

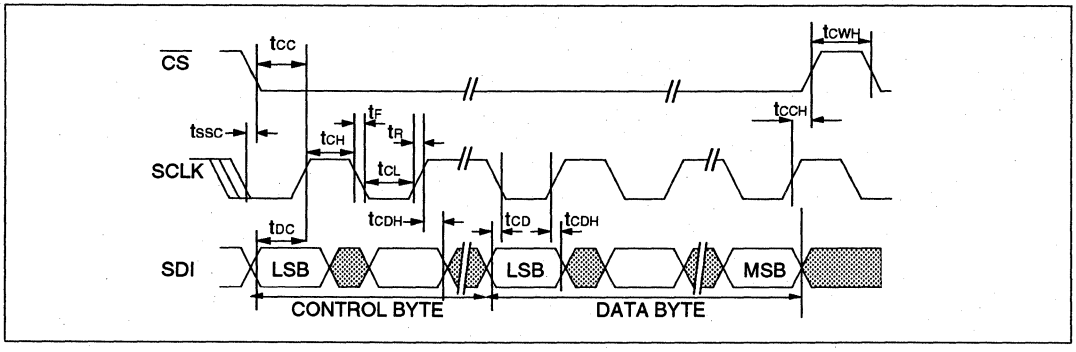
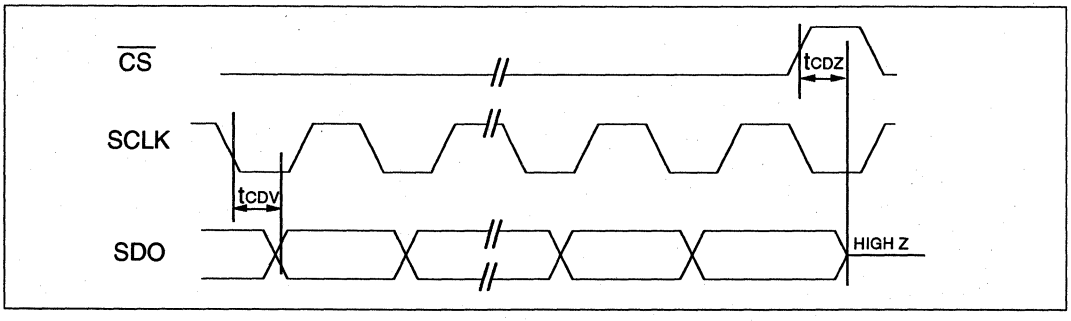


Figure 25: Serial Port Read A.C. Timing

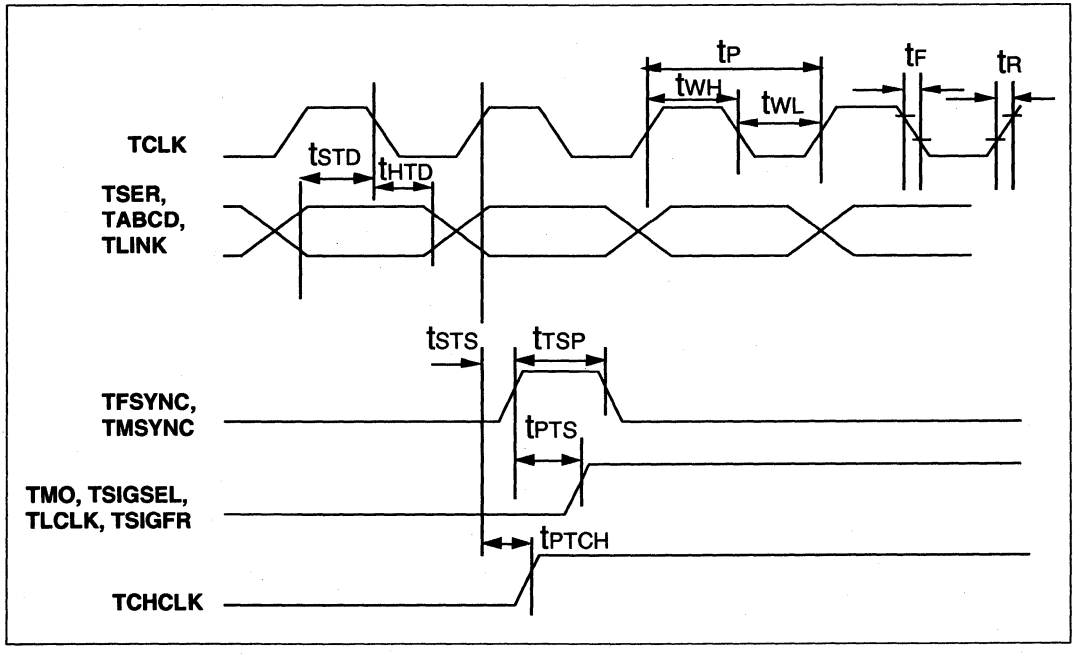


A.C. Electrical Characteristics - Transmit

Parameter	Sym	Min	Max	Units	Test Conditions[1]
TCLK Period	t_P	250	–	ns	C load = 100 pF
TCLK Pulse Width	t_{WL}, t_{WH}	125	–	ns	C load = 100 pF
TCLK, RCLK Rise & Fall Times	t_R, t_F	–	–	ns	C load = 100 pF
TSER, TABCD, TLINK Setup to TCLK Falling	t_{STD}	50	–	ns	C load = 100 pF
TSER, TABCD, TLINK Hold from TCLK Falling	t_{HTD}	50	–	ns	C load = 100 pF
TFSYNC, TMSYNC Setup to TCLK Rising	t_{STS}	-125	125	ns	C load = 100 pF
Propagation Delay TFSYNC to TMO, TSIGSEL, TSIGFR, TLCLK	t_{PTS}	–	75	ns	C load = 100 pF
Propagation Delay TCLK to TCHCLK	t_{PTCH}	–	75	ns	C load = 100 pF
TFSYNC, TMSYNC Pulse Width	t_{TSP}	100	–	ns	C load = 100 pF

[1] Measured at V_{IH} = 2.0V, V_{IL} = .8V, and 10 ns maximum rise and fall time.

Figure 26: Transmit A.C. Timing Diagram

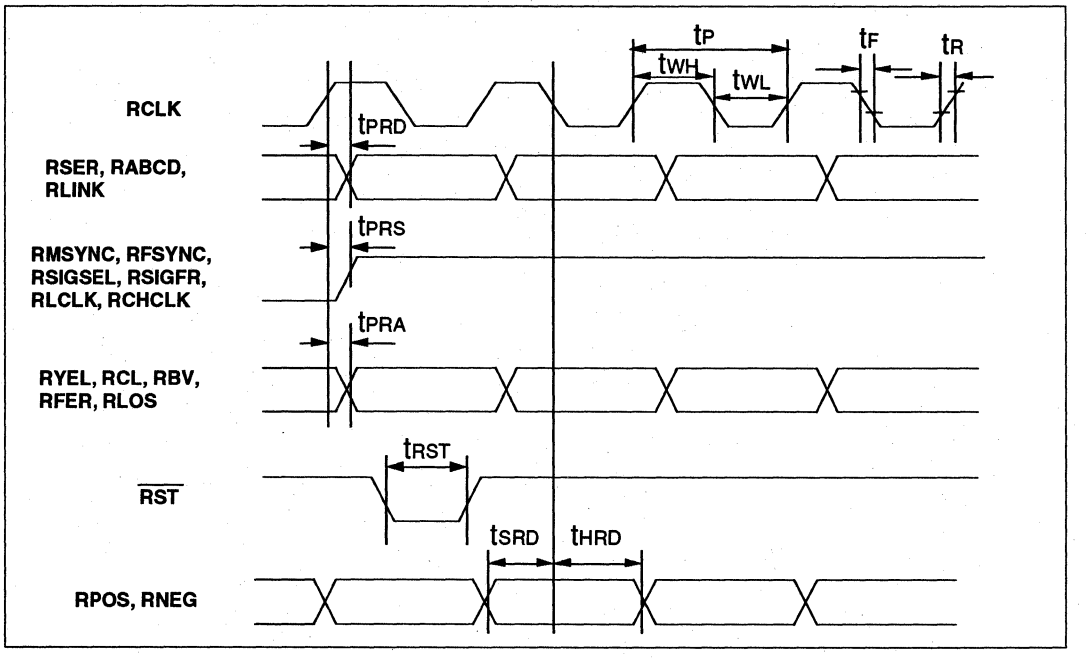


A.C. Electrical Characteristics - Receive

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions[2]
Propagation Delay RCLK to RMSYNC, RFSYNC, RSIGSEL, RSIGFR, RLCLK, RCHCLK	t_{PRS}	–	–	75	ns	C Load = 100 pF
Propagation Delay RCLK to RSER, RABCD, RLINK	t_{PRD}	–	–	75	ns	C Load = 100 pF
Transition Time, All Outputs	t_{TTR}	–	–	20	ns	C Load = 100 pF
RCLK Period	t_P	250	648	–	ns	C Load = 100 pF
RCLK Pulse Width	t_{WL}, t_{WH}	125	324	–	ns	C Load = 100 pF
RCLK Rise & Fall Times	t_R, t_F	–	20	–	ns	C Load = 100 pF
RPOS, RNEG Setup to RCLK Falling	t_{SRD}	50	–	–	ns	C Load = 100 pF
RPOS, RNEG Hold to RCLK Falling	t_{HRD}	50	–	–	ns	C Load = 100 pF
Propagation Delay RCLK to RYEL, RCL, RFER, RLOS, RBV	t_{PRA}	–	–	–	ns	C Load = 100 pF
Minimum $\overline{RST}$ Pulse Width on System Power Up or Restart	t_{RST}	1	–	–	µs	C Load = 100 pF

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Measured at V_{IH} = 2.0V, V_{IL} = .8V, and 10 ns maximum rise and fall time.

Figure 27: Receive A.C. Timing Diagram



LXP2181A

E1 CRC Framer/Formatter

General Description

The LXP2181A is one of a family of Level One E1/CEPT (2.048 MHz) interface solutions. An enhanced version of the earlier LXP2181, it is a pin compatible drop-in replacement for the Dallas DS2181A. A selectable 2181 Emulation mode provides full backward compatibility with the LXP2181 and DS2181. It is designed for E1 networks and supports all logical requirements of CCITT Red Book Recommendations G.704, G.706 and G.732.

The transmit side generates framing patterns and CRC4 codes, formats outgoing channel and signaling data and produces network alarm codes. The receive side decodes the incoming data and establishes frame, CAS multiframe, and CRC4 multiframe alignments. Once synchronized, the device extracts channel, signaling and alarm data.

The device offers both Host and Hardware control modes. In Host mode, a serial port allows access to 14 on-chip control and status registers. In this mode, a host processor controls such features such as error logging, per-channel code manipulation and alteration of the receive synchronizer algorithm. The Hardware mode is intended for preliminary system prototyping and/or retrofitting into existing systems. This mode requires no host processor and disables special features available in the processor mode.

The LXP2181A is a monolithic CMOS device which requires only a single +5V power supply.

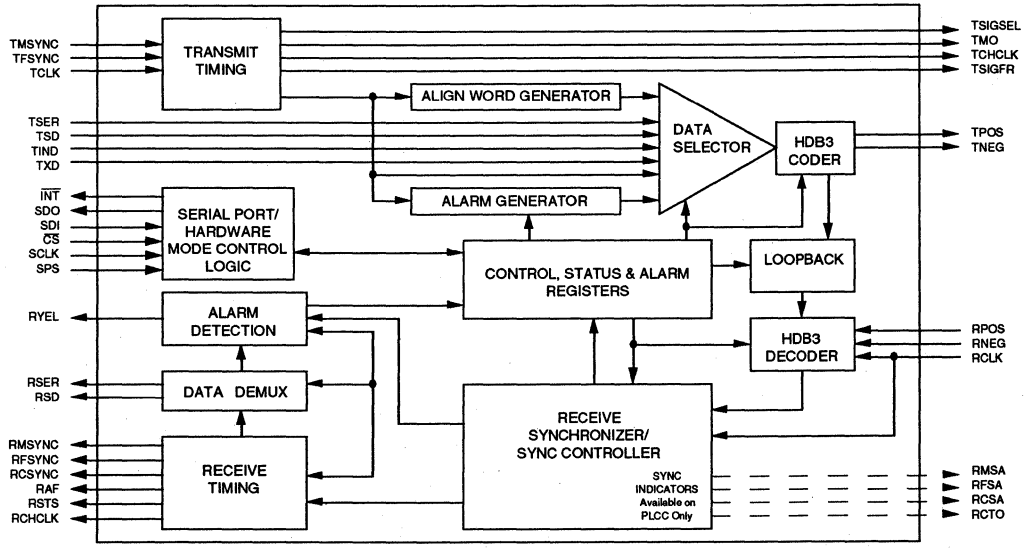
Features

- Drop-in replacement for the DS2181A.
- 2181 Emulation mode provides full backward compatibility with the LXP2181 and DS2181
- Single chip primary rate framer/formatter meets CCITT standards G.704, G.706 and G.732
- Supports new CRC4 based framing standards and CAS and CCS signaling standards
- Host mode uses simple serial interface for device configuration and control
- Hardware mode for stand-alone applications requires no host processor
- Comprehensive on-chip alarm generation, alarm detection and error logging logic
- Shares footprint with LXP2180A T1 Framer/Formatter
- Fully compatible with LXT30X series transceivers and LXP60X series clock adapters
- Available in 40-pin DIP or 44-pin PLCC

Applications

- Computer-to-PBX interfaces (DMI and CPI)
- High speed computer to computer data links
- Digital cross-connect interface

Figure 1: Block Diagram



Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- Voltage on any pin relative to ground -1.0V to + 7V
- Operating temperature -40 °C (min) to 85 °C (max)
- Storage temperature -55 °C (min) to 125 °C (max)
- Soldering temperature 260 °C for 10 seconds

Recommended Operating Conditions (Voltages are with respect to ground (VSS) unless otherwise stated)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Logic 1	V_{IH}	2.0	–	V_{DD} + .3	V	
Logic 0	V_{IL}	-0.3	–	+0.8	V	
Supply voltage	V_{DD}	4.5	5	5.5	V	
Capacitance						
Input capacitance	C_{IN}	–	–	5	pF	
Output capacitance	C_{OUT}	–	–	7	pF	
DC Electrical Characteristics - Clocked operation over recommended temperature and power supply ranges						
Supply current	I_{DD}	–	6	10	mA	See Notes 2 and 3
Input leakage	I_{IL}	-1.0	–	+1.0	µA	See Note 4
Output leakage	I_{OL}	-1.0	–	+1.0	µA	See Note 5
Output high current	I_{OH}	-1.0	–	–	mA	V_{OH} = 2.4 V, See Note 6
Output low current	I_{OL}	+4.0	–	-	mA	V_{OL} = 0.4 V, See Note 7

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] TCLK = RCLK = 2.048 MHz.
[3] Outputs Open.
[4] $0V < V_{IN} < V_{DD}$
[5] All outputs except INT, which is open collector.
[6] All outputs.
[7] Applies to SDO when tristated.

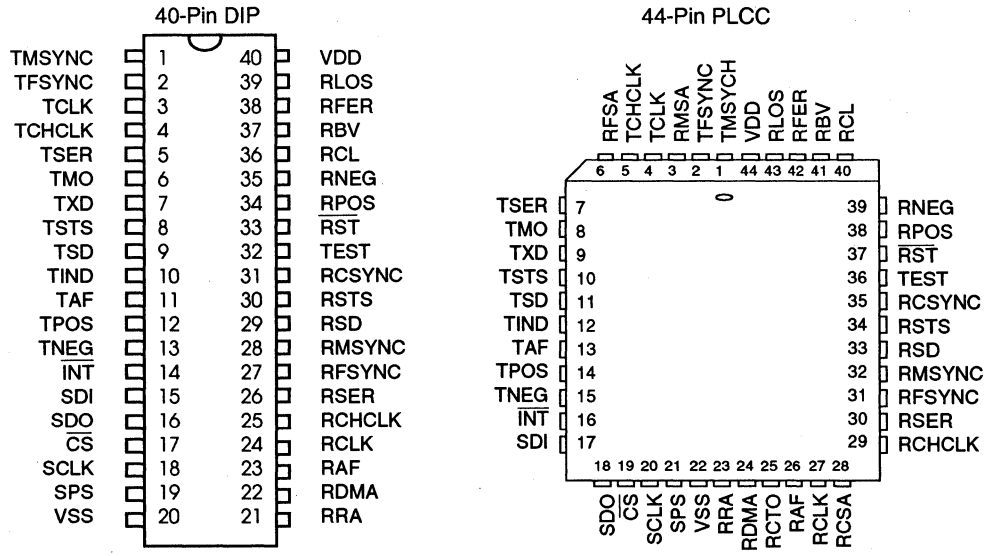


Table 1: Transmit Pin Descriptions

Pin#		Sym	I/O	Name	Description
DIP	PLCC				
1	1	TMSYNC	I	Transmit Multi-frame Sync	Transmit Multiframe Sync. Low-high transition establishes start of CAS and/or CRC4 multiframe. May be tied low, which allows internal multiframe counter to run free.
2	2	TFSYNC	I	Transmit Frame Sync Channel B2	Transmit Frame Sync. Low-high transition every frame period establishes frame boundaries. May be tied low allowing TMSYNC to establish frame boundaries.
3	4	TCLK	I	Transmit Clock	2.048 MHz primary clock.
4	5	TCHCLK	O	Transmit Channel Clock	256 kHz clock which identifies time slot (channel) boundaries. Useful for parallel to serial conversion of channel data.
5	7	TSER	I	Transmit Serial Data	NRZ data input, sampled on falling edges of TCLK.
6	8	TMO	O	Transmit Multi-frame Out	Output of internal multiframe counter, high during frame 0. Low otherwise.
7	9	TXD	I	Transmit Extra Data	Sampled on falling edge of TCLK during bit times 5, 7, and 8 of time slot 16 in frame 0 when CAS signaling is enabled.
8	10	TSTS	O	Transmit Signal-ing Time slot	High during time slot 16 of every frame. Low otherwise.
9	11	TSD	I	Transmit Signal-ing Data	CAS signaling data input. Sampled on falling edges of TCLK for insertion into outgoing time slot 16 when enabled.

Table 1: Transmit Pin Descriptions continued

Pin# DIP	Pin# PLCC	Sym	I/O	Name	Description
10	12	TIND	I	Transmit International and National Data	Sampled on falling edge of TCLK during bit 1 time of time slot 0 every frame (international) and/or during bit times 4 through 8 of time slot 0 during non-align frames (national) when enabled.
11	13	TAF	O	Transmit Alignment Frame	High during frames containing the frame alignment signal, low otherwise.
12	14	TPOS	O	Transmit Positive and Negative Data	Transmit Bipolar Data Outputs. Updated on rising edge of TCLK.
13	15	TNEG	O		

Table 2: Port Pin Description

Pin# DIP	Pin# PLCC	Sym	I/O	Name	Description
14	16	$\overline{\text{INT}}$[1]	O	Receive Alarm Interrupt	An active low, open drain output which flags the host controller during alarm conditions.
15	17	SDI[1]	I	Serial Data Input	Data for on-chip control registers. Sampled on rising edge of SCLK.
16	18	SDO[1]	O	Serial Data Output	Serial output of control and status information from on-chip registers. Updated on falling edge of SCLK, tristated during serial port write or when $\overline{\text{CS}}$ is high.
17	19	$\overline{\text{CS}}$[1]	I	Chip Select	Must be low to write or read the serial port registers.
18	20	SCLK[1]	I	Serial Data Clock	Used to read or write the serial port registers.
19	21	SPS	I	Serial Port Select	Tie to VDD to select serial port (Host mode). Tie to VSS to select the Hardware mode.

1. Multifunction pins; see Hardware mode description (Table 9, page 21).

Table 3: Power and Test Pin Descriptions

Pin# DIP	Pin# PLCC	Sym	I/O	Name	Description
20	22	VSS	–	Signal Ground	0.0 V signal ground.
32	36	TEST	I	Test Mode	Tie to VDD for normal operation. Tie to VSS for 2181 emulation.
40	44	VDD	–	Positive Supply	+5V power supply input.

Table 4: Receive Pin Descriptions

Pin# DIP	Pin# PLCC	Sym	I/O	Name	Description
21	23	RRA	O	Receive Remote Alarm	Transitions high when yellow alarm detected, goes low when alarm clears.
22	24	RDMA	O	Receive Distant Multiframe Alarm	Transitions high when yellow alarm detected, goes low when alarm clears.
23	26	RAF	O	Receive Alignment Frame	High during frames containing the alignment signal. Low otherwise.
24	27	RCLK	I	Receive Clock	2.048 MHz primary clock.
25	29	RCHCLK	O	Receive Channel Clock	256 KHz clock, identifies time slot (channel) boundaries; useful for serial-to-parallel conversion of channel data.
26	30	RSER	O	Receive Serial Data	Received NRZ serial data, updated on rising edge of RCLK.
27	31	RFSYNC	O	Receive Frame Sync	Trailing edge indicates start of frame.
28	32	RMSYNC	O	Receive Multi-frame Sync	Low-high transition indicates start of CAS multiframe; held high during frame 0.
29	33	RSD	O	Receive Signaling Data	Extracted time slot 16 data, updated on rising edge of RCLK.
30	34	RSTS	O	Receive Signaling Time slot	High during time slot 16 of every frame. Low otherwise.
31	35	RCSYNC	O	Receive CRC4 Sync	Low-high transition indicates start of CRC4 multiframe. Held high during CRC4 frames 0 through 7 and held low during frames 8 through 15.
33	37	$\overline{\text{RST}}$	I	Reset	Must be asserted during device power-up and when changing to/ from the Hardware mode.
34	38	RPOS	I	Receive Positive and Negative Inputs	Receive Bipolar Data Inputs are sampled on the falling edge of RCLK.
35	39	RNEG	I		
36	40	RCL	O	Receive Carrier Loss	Low-high transition indicates loss of carrier.
37	41	RBV	O	Receive Bipolar Violation	Receive Bipolar Violation pulses high during detected bipolar violations.
38	42	RFER	O	Receive Frame Error	Receive Frame Error pulses high when frame alignment, CAS multiframe alignment or CRC4 words are received in error.
39	43	RLOS	O	Receive Loss of Sync	RLOS indicates synchronizer status: high when frame, CAS and/or CRC4 multiframe search underway; low otherwise.

Table 5: LXP2181AP (PLCC Package) Receive Sync Indicator Pin Descriptions[1]

PLCC Pin#	Sym	I/O	Name	Description
3	RMSA	O	Receive Multi-Frame Search Active	Indicates Receive Multiframe Search Active. Transitions high when the synchronizer searching for the CAS multiframe alignment word is activated.
6	RFSA	O	Receive Frame Search Active	Indicates Receive Frame Search Active. Transitions high when the synchronizer searching for the FAS is active.
25	RCTO	O	Receive CRC4 Counter Time-Out	Indicates Receive CRC4 Time-Out. Transitions high when the RCTO counter reaches its maximum count of 32. Returns low when: (1) LXP2181A reaches CRC4 multiframe synchronization; (2) CRC4 is disabled via CRC.2; or (3) LXP2181A is issued a hardware reset via the RST pin.
28	RCSA	O	Receive CRC4 Search Active	Indicates Receive CRC4 Search Active. Transitions high when the synchronizer searching for the CRC4 multiframe alignment word is active.

[1] These pin descriptions apply only to the LXP2181AP (PLCC package), and only when the device is operating in the normal mode. These pins are tri-stated during the 2181 Emulation mode.

Table 6: Register Summary

Register	Address	Side[1]	Description / Function
RIMR	0000	R	Receive Interrupt Mask Register. Allows masking of alarm generated interrupts.
RSR	0001	R[2]	Receive Status Register. Reports all receive alarm conditions.
BVCR	0010	R	Bipolar Violation Count Register. 8-bit presetable counter which records individual bipolar violations.
CECR	0011	R	CRC4 Error Count Register. 8-bit presetable counter which records individual CRC4 errors.
FECR	0100	R	Frame Error Count Register. 8-bit presetable counter which logs individual errors in the received frame alignment signal.
RCR[3]	0101	R	Receive Control Register. Establishes receive side operating characteristics.
CCR[3]	0110	T/R	Common Control Register. Establishes additional operating characteristics common to both transmit and receive sides.
TCR[3]	0111	T	Transmit Control Register. Selects additional transmit side modes.
TIR1 TIR2 TIR3 TIR4	1000 1001 1010 1011	T T T T	Transmit Idle Registers. Designate which outgoing time slots are to be substituted with idle code.
TINR	1100	T	Transmit International and National Register. When enabled via the TCR, contents are inserted into the outgoing national and/or international bit positions.
TXR	1101	T	Transmit Extra Register. When enabled via the TCR, contents are inserted into the outgoing extra bit positions.

[1] Transmit or Receive side register.
[2] RSR is a read-only register. All other registers are read/write.
[3] Reserved bit locations in control registers should be programmed to 0, to maintain compatibility with future products.

Operating Modes

The LXP2181A operates in either the Host mode or the Hardware mode. In the Host mode pins 14 through 18 comprise a microprocessor/microcontroller compatible serial port which can be used for device configuration, control and status monitoring.

In the Hardware mode no offboard processor is required. Pins 14 through 18 are reconfigured into "Hardwired" select pins.

Host Mode - Serial Port Interface

Pins 14 through 18 of the LXP2181A serve as a microprocessor/microcontroller compatible serial port. Fourteen onboard registers (refer to Table 6) allow the user to update operational characteristics and monitor device status via a host controller, minimizing hardware interfaces. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads and/or writes by the host. The timing set is identical to that of "8051 type" microcontrollers operating in serial port mode 0. For proper operation of the port and the transmit and receive registers, the user should provide TCLK and RCLK as well as SCLK.

Address/Command Byte

An address/command byte (ACB) must precede any read or write of the port registers. As shown in Figure 2, the first bit (LSB) of the address/command word specifies register read or write. The following 4-bit nibble identifies the register address. The next two bits are reserved and must be set to zero for proper operation. The last bit of the address/command word enables burst mode when set; the burst mode causes all registers to be consecutively written or read. Data is written to and read from the port LSB first.

Chip Select and Clock Control

All data transfers are initiated by driving the $\overline{CS}$ input low. Input data is latched on the rising edge of SCLK and must be valid during the previous low period of SCLK to prevent momentary corruption of register data during writes. Data is output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated and SDO is tristated when the $\overline{CS}$ input transitions high.

Clocks

To access the serial port registers both TCLK and RCLK are required along with SCLK. Transmit and receive registers are internally accessed by TCLK and RCLK, respectively. The CCR is considered a receive register for this purpose.

Data I/O

Data I/O timing is shown in Figure 3. Following the 8 SCLK cycles that input a Write address/command byte, data at SDI is strobed into the addressed register on the rising edges of the next 8 SCLK cycles. Following a Read address/command word, contents of the selected register are output at SDO on the falling edges of the next 8 SCLK cycles. The SDO pin is tristated during device write, and may be tied to SDI in applications where the host processor has a bidirectional I/O pin.

Burst Mode

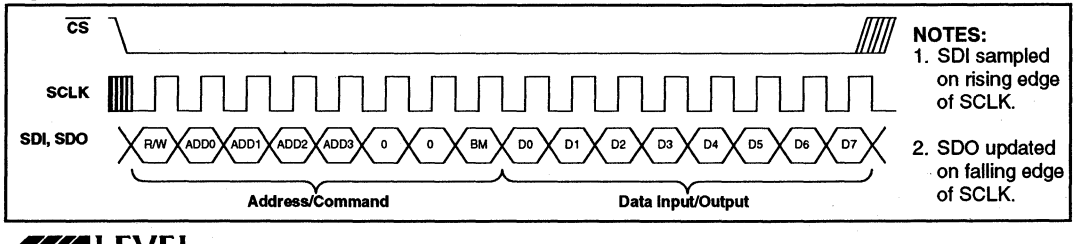
The burst mode allows all on-chip registers to be consecutively read or written by the host processor. This feature minimizes device initialization time on power-up or system reset. Burst mode is initiated when ACB.7 is set and the address nibble is 0000. All registers must be read or written during the burst mode. If $\overline{CS}$ transitions high before the burst is complete, data validity is not guaranteed.

Figure 2: Address/Command Byte (ACB)

(MSB)							(LSB)
BM	–	–	ADD3	ADD2	ADD1	ADD0	R/W

Symbol	Position	Name And Description
BM	ACB.7	Burst Mode. If set (and ACB.1 through ACB.4 = 0) burst read or write is enabled.
–	ACB.6	Reserved. Must be set to 0 for proper operation.
–	ACB.5	Reserved. Must be set to 0 for proper operation.
ADD3	ACB.4	MSB of register address.
ADD0	ACB.1	LSB of register address.
R/W	ACB.0	Read/Write Select. 0 = write addressed register. 1 = read addressed register.

Figure 3: Serial Port Read/Write



E1 Frame Structure

The E1 frame is made up of 32 8-bit channels (time slots) numbered from 0 to 31. The frame alignment signal in bit positions 2 thru 8 of time slot 0 of every other frame is independent of the various multiframe modes described below. Outputs TAF and RAF indicate frames which contain the alignment signal. Time slot 0 of frames not containing the frame alignment signal is used for alarm and national data.

Multiframe Signaling Modes

E1 networks support Channel Associated Signaling (CAS) or Common Channel Signaling (CCS). These signaling modes are independently selectable for transmit and receive sides. Bit 5 of the Transmit Control Register (TCR), shown in Figure 4, controls transmit signaling mode. The Receive Control Register (RCR) controls receive side signaling mode.

CAS Mode

CAS (selected when TCR.5 = 0 and/or when RCR.5 = 0) is a bit oriented signaling technique which utilizes a 16 frame multiframe. The multiframe alignment signal (0-hex), extra and alarm bits occupy time slot 16 of frame 0. Time slot 16 of the remaining 15 frames is reserved for channel signaling data. Four signaling bits (A, B, C and D) are transmitted once per multiframe as shown in Figure 8. CAS output format is shown in Figure 9. Input TMSYNC establishes the transmitted CAS multiframe position. Signaling data may be sourced from input TSD (TCR.6 = 1) or multiplexed into TSER (TCR.6 = 0).

Figure 4: Transmit Control Register

(MSB)							(LSB)
TUA1	TSS	TSM	INBS	NBS	XBS	TSA1	ODM

Symbol	Position	Name And Description
TUA1	TCR.7	Transmit Unframed All 1s. 0 = Normal Operation. 1 = Replace outgoing data at TPOS and TNEG with unframed all 1's code.
TSS	TCR.6	Transmit Signaling Select[1]. 0 = Signaling data embedded in the serial bit stream is sampled at TSER during time slot 16. 1 = Signaling data is channel associated and sampled at TSD as shown in Table 6.
TSM	TCR.5	Transmit Signaling Mode[1]. 0 = Channel Associated Signaling (CAS) 1 = Common Channel Signaling (CCS)
INBS	TCR.4	International Bit Select. 0 = Sample international bit at TIND. 1 = Outgoing international bit = TINR.7.
NBS	TCR.3	National Bit Select. 0 = Sample national bits at TIND. 1 = Source outgoing national bits from TINR.4 through TINR.0.
XBS	TCR.2	Extra Bit Select. 0 = Sample extra bits at TXD. 1 = Source extra bits from TXR.0, TXR.1 and TXR.3.
TSA1	TCR.1	Transmit Signaling All 1's. 0 = Normal Operation. 1 = Force contents of time slot 16 in all frames to all 1's.
ODM	TCR.0	Output Data Mode. 0 = TPOS and TNEG outputs are 100% duty cycle. 1 = TPOS and TNEG outputs are 50% duty cycle.

[1] When the Common Channel Signaling (CCS) mode is enabled (TCR.5 = 1), the TSD input is disabled internally; all time slot 16 data is sampled at TSER.

CCS Mode

CCS (selected when TCR.5 = 1 and/or when RCR.1 = 1) utilizes all bit positions of time slot 16 in every frame for "message oriented" signaling data transmission. In CCS mode one can use either time slot 16 or any one of the other 30 data channels for message oriented signaling. The CCS mode has no multiframe structure and the insertion of CAS multiframe alignment, distant multiframe alarm and/or extra bits into time slot 16 is disabled. TSER is the source of time slot 16 data.

CRC4 Coding

The need for enhanced error monitoring capability and additional protection against emulators of the frame alignment word has let to the development of a cyclic redundancy check (CRC) procedure. Receive and transmit side CRC modes are enabled by bits 2 and 3, respectively, of the Common Control Register (CCR) shown in Figure 5. When enabled, CRC4 coding replaces the international bit positions in frames 0 thru 12 and 14 with a CRC4 multiframe alignment pattern and associated checksum words. The CRC4 multiframe must begin with a frame containing the frame alignment signal (CCR.6 = 0). A rising edge at TMSYNC establishes the CRC4 multiframe alignment (TMSYNC will also establish outgoing CAS multiframe alignment if enabled via TCR.5).

Incoming CRC4 multiframe alignment is indicated by RCSYNC. Detected CRC4 checksum errors are reported at output RFER and logged in the CECR.

Receive Synchronizer

The fixed characteristics of the receive synchronizer may be modified by use of programmable characteristics resident in the CCR and in the Receive Control Register (RCR) shown in Figure 6. Sync criteria must be met before synchroniza-

Figure 5: Common Control Register[1]

(MSB)							(LSB)
–	TAFP	THDE	RHDE	TCE	RCE	EMM	LLB

Symbol	Position	Name And Description
–	CCR.7	Reserved. Must be set to 0 for proper operation.
TAFP	CCR.6	Transmit Align Frame Position[2]. When clear, the CAS multiframe begins with a frame containing the frame alignment signal. When set, the CAS multiframe begins with a frame not containing the frame alignment signal.
THDE	CCR.5	Transmit HDB3 Enable. 0 = Outgoing data at TPOS and TNEG is AMI coded. 1 = Outgoing data at TPOS and TNEG is HDB3 coded.
RHDE	CRC.4	Receive HDB3 Enable. 0 = Incoming data at RPOS and RNEG is AMI coded. 1 = Incoming data at RPOS and RNEG is HDB3 coded.
TCE	CCR.3	Transmit CRC4 Enable. When set, outgoing international bit positions in frames 0 through 12 and 14 are replaced by CRC4 multiframe alignment and checksum words.
RCE	CCR.2	Receive CRC4 Enable. 0 = Disable CRC4 multiframe synchronizer. 1 = Enable CRC4 synchronizer, search for CRC4 multiframe alignment once frame alignment complete.
EMM	CCR.1	2181 Emulation Mode. 0 = 2181 Emulation Mode. 1 = Normal Operation.
LLB	CCR.0	Local Loopback. 0 = Normal Operation. 1 = Internally loop TPOS, TNEG and TCLK to RPOS, RNEG and RCLK.

[1] CCR is considered a receive register and operates from RCLK and SCLK.

[2] This bit must be cleared when CRC4 multiframe mode is enabled (CCR.3 = 1); its state does not affect CCS framing (RCR.5 = 1).

tion is declared. Resync criteria establish error occurrences which will cause an auto-resync event when enabled (RCR.1 = 0).

As shown in Figure 7, the receive synchronizer searches for the frame alignment signal (FAS) first. Once identified, the output timing set associated with the framing pattern (all outputs except RCSYNC) is updated to that new alignment. If enabled, the synchronizer then begins CAS and/or CRC4 multiframe search, outputs RMSYNC and/or RCSYNC are then updated. Output RLOS is held high during the entire resync process, then transitions low after the last output timing update indicating resync is complete. Figure 7 also shows the four synchronizer activity indicators available only on the LXP2181AP (PLCC package). Refer to Table 5.

Fixed Frame Sync Criteria

Valid frame sync is assumed when the correct frame alignment signal is present in frame N and frame N+2 and not present in frame N+1 (Bit 2 of Time slot 0 of Frame N+1 is also checked for "1"). CAS and/or CRC4 multiframe alignment search is initiated when the frame search is complete if enabled via RCR.5 and/or CCR.2.

Fixed CAS Multiframe Sync Criteria

CAS multiframe sync is declared when the multiframe alignment pattern is properly detected and time slot 16 of the previous frame contains code other than zeros. *When operating in the 2181 emulation mode, frame search is restarted if no valid pattern can be found in 12 to 14 ms.*

Fixed CRC4 Multiframe Sync Criteria

CRC4 multiframe sync is declared if at least two valid CRC4 multiframe alignment signals are found within 8 ms after frame alignment is completed. If not found within 8 ms, frame search is restarted. The search for multiframe alignment signal is performed in time slot 0 of frames not containing the frame alignment signal. *When operating in the 2181 emulation mode, CRC4 multiframe search timeout is extended from 8 ms to between 12 and 14 ms.*

Figure 6: Receive Control Register

(MSB)							(LSB)
–	–	RSM	CMSC	CMRC	FRC	SYNCE	RESYNC

Symbol	Position	Name And Description
–	RCR.7	Reserved, must be set to 0 for proper operation.
–	RCR.6	Reserved, must be set to 0 for proper operation.
RSM	RCR.5	Received Signaling Mode. 0 = Channel Associated Signaling (CAS) 1 = Common Channel Signaling (CCS).
CMSC	RCR.4	CAS Multiframe Sync Criteria. 0 = Declare sync when fixed sync criteria are met. 1 = Declare sync when fixed criteria are met and two additional consecutive valid multiframe alignment signals are detected.
CMRC	RCR.3	CAS Multiframe Resync Criteria. 0 = Utilize only fixed sync criteria. 1 = Resync if fixed criteria met and/or if two consecutive time slot 16 words have values of zero in the first four MSB positions (0000xxxx).
FRC	RCR.2	Frame Resync Criteria. 0 = Utilize only fixed resync criteria. 1 = Resync if fixed criteria met and/or if bit 2 in time slot 0 of non-align frames is received in error on three consecutive occasions.
SYNCE	RCR.1	Sync Enable. If clear, the transceiver will automatically begin a resync if error criteria are met. If set, no auto resync occurs.
RESYNC	RCR.0	Resync. When toggled low to high, the receive synchronizer will initiate resync immediately. The bit must be cleared, then set again for subsequent resyncs.

Fixed Frame Resync Criteria

When enabled via RCR.1, the device will automatically initiate frame search whenever the frame alignment word is received in error three consecutive times.

Fixed CAS Multiframe Resync Criteria

When enabled via RCR.1, the device will automatically initiate frame search whenever two consecutive CAS multiframe alignment words are received in error.

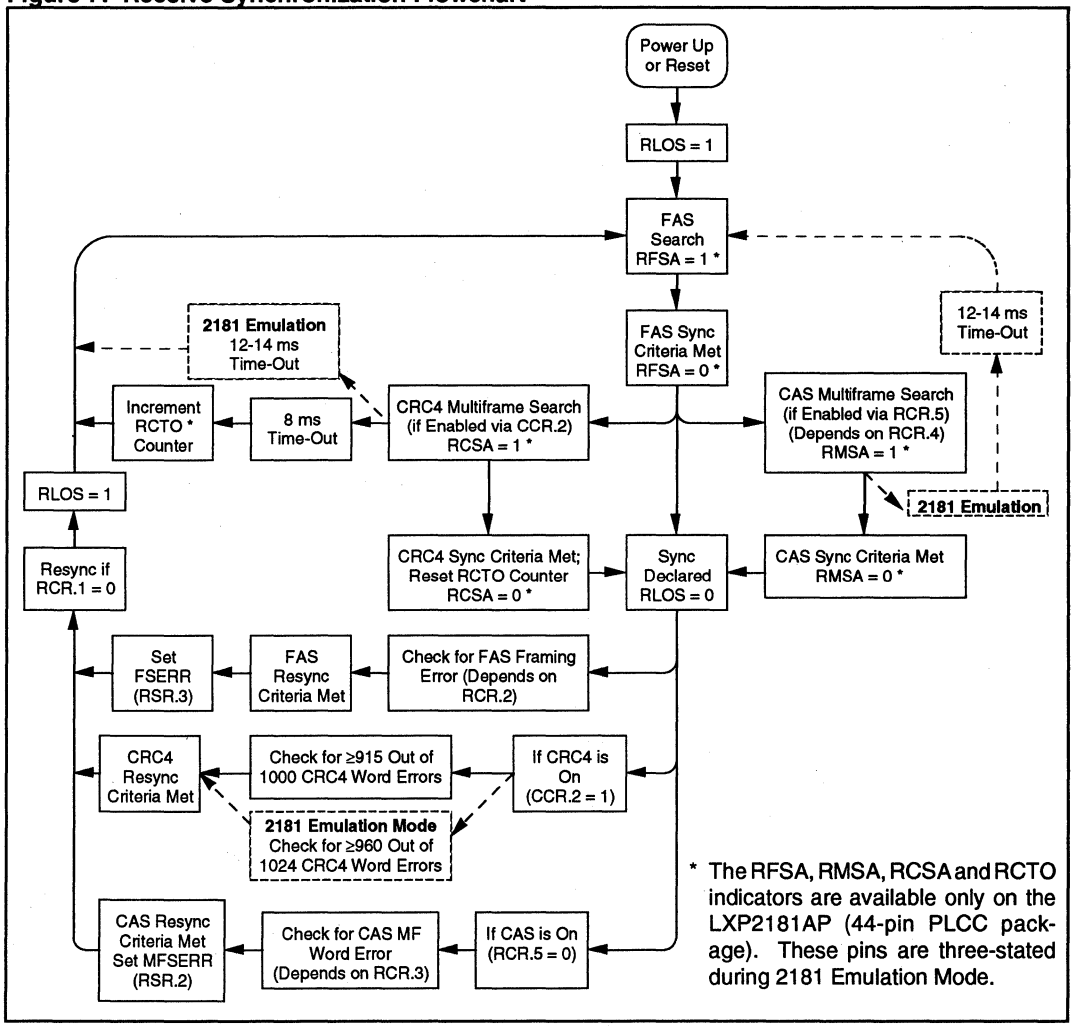
Fixed CRC4 Multiframe Resync Criteria

When enabled via RCR.1, the device will automatically initiate frame search whenever 85 or fewer individual CRC4 bits of the last 1000 CRC4 words are received without error. Even when the incoming CRC4 code words are random data, the probability that 85 bits are good out of 1000 words is almost 100%. The threshold for the CRC4 Multiframe Resync Criteria is chosen such that under most circumstances it will not be triggered. (*In the 2181 Emulation mode, the resync criteria is relaxed to 64 out of 1024 words.*)

When the LXP2181A is used with a processor, the user may choose his own threshold by using the on-chip CRC4 Error Count Register (CECR). There can be only one possible CRC4 word error per ms, so the counter can be used to monitor errors for a maximum period of 255 ms before possible saturation. This period can be extended, for example, by reading the CECR every 200 ms, clearing it, and accumulating the error count in a host microcontroller. Five such reads would establish a one second monitoring period. For example, a threshold of 700 CRC4 word errors in a one second monitoring period can be set this way. The resync

2

Figure 7: Receive Synchronization Flowchart



process can be manually initiated using bit position 0 in the Receive Control Register (RCR.0).

For hardware mode applications of the LXP2181A, the RFER pin may be used with RCSYNC pin to demultiplex the CRC4 word errors. Errors are then counted externally. The resync process can be manually initiated using the Reset pin.

CAS Signaling Source

CAS applications sample signaling data at TSER when TCR.6 = 0; an on-chip data multiplexer accepts CAS data input at TSD when TCR.6 = 1. Refer to Table 7 and Figure 8 for TSD input timing. The data multiplexer must be disabled (TCR.6 = 0) when the CCS mode is enabled (TCR.5 = 1). The CAS output format is shown in Figure 9.

Transmit International and National Data

Bit 1 of time slot 0 in all frames is known as the international bit. When TCR.4 = 1, the transmitted international bit is sourced from TINR.7 (see Figure 10). When TCR.4 = 0, the transmitted international bit is sampled at TIND during the first bit period of each frame. The international bit positions in all outgoing frames except 13 and 15 are replaced by CRC4 codewords and the CRC4 multiframe alignment signal when CCR.3 = 1.

Bits 4 thru 8 of time slot 0 in non-align frames are reserved for national use. When TCR.3 = 1, the transmitted national bits are sourced from register locations TINR.4 thru TINR.0. If TCR.3 = 0, the national bits are sampled at TIND during bit times 4 thru 8 of time slot 0 in non-align frames.

Reserved bit positions in the TINR must be set to 0 when written; those bits may be 0 or 1 when read.

Transmit Extra Data

In the CAS mode, time slot 16 of frame 0 contains the multiframe alignment pattern, extra bits and the distant multiframe alarm. When CAS is enabled (TCR.5 = 0), the

Table 7: TSD Input Timing (TCR.6 = 1; TCR.5 = 0)

Frame #	Time Slot Signaling Data Sampled at TSD
0	17
1	1, 18
2	2, 19
3	3, 20
4	4, 21
5	5, 22
6	6, 23
7	7, 24
8	8, 25
9	9, 26
10	10, 27
11	11, 28
12	12, 29
13	13, 30
14	14, 31
15	15

[1] A, B, C and D signaling data is sampled on the falling edges of TCLK during bit times 5, 6, 7 and 8 of time slots indicated.

Figure 8: TSD Input Timing

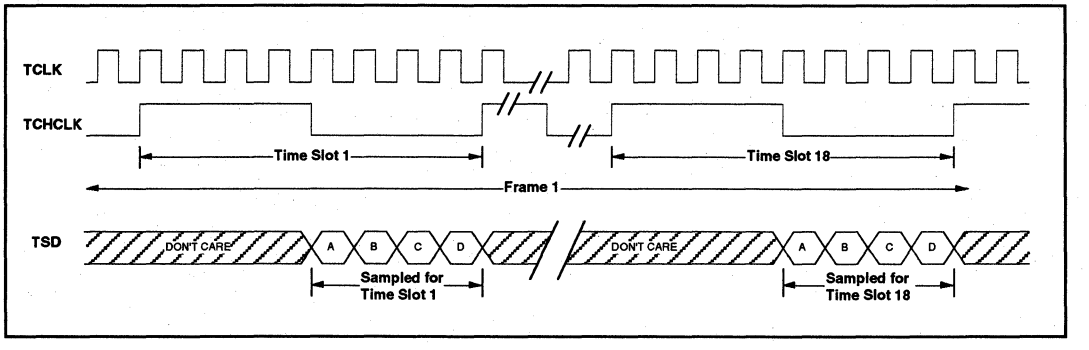


Figure 9: CAS Output Format in Time Slot 16

Frame 0[1]	Frame 1		Frame 15	
0000 XYXX	ABCD for time slot 1	ABCD for time slot 17	ABCD for time slot 15	ABCD for time slot 31

[1] Time slot 16 of Frame 0 is reserved for the multiframe alignment word (0000), distant multiframe alarm (Y) and extra bits (X-XX).

Figure 10: Transmit International and National Register

(MSB)							(LSB)
INB	–	TRA	NB4	NB5	NB6	NB7	NB8

Symbol	Position	Name And Description
INB	TINR.7	International Bit. Inserted into the outgoing data stream when TCR.4 = 1.
–	TINR.6	Reserved, must be set to 0 for proper operation.
TRA	TINR.5	Transmit Remote Alarm. 0 = Normal Operation; bit 3 of time slot 0 in non-alignment frames clear. 1 = Alarm Condition; bit 3 of time slot 0 in non-alignment frames set.
NB4 NB5 NB6 NB7 NB8	TINR.4 TINR.3 TINR.2 TINR.1 TINR.0	Transmit National Bits. Inserted into the outgoing data stream at TPOS and TNEG when TCR.3 = 1.

Figure 11: Transmit Extra Register

(MSB)							(LSB)
–	–	–	–	XB1	TDMA	XB2	XB3

Symbol	Position	Name And Description
–	TXR.7	Reserved, must be set to 0 for proper operation.
–	TXR.6	Reserved, must be set to 0 for proper operation.
–	TXR.5	Reserved, must be set to 0 for proper operation.
–	TXR.4	Reserved, must be set to 0 for proper operation.
XB1	TXR.3	Extra Bit 1.
TDMA	TXR.2	Transmit Distant Multiframe Alarm 0 = Normal Operation; bit 6 of time slot 16 in frame 0 clear. 1 = Alarm condition; bit 6 of time slot 16 in frame 0 set.
XB2	TXR.1	Extra Bit 2.
XB3	TXR.0	Extra Bit 3.

Figure 12: Transmit Idle Registers

(MSB)							(LSB)	
TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0[1]	TIR1
TS15	TS14	TS13	TS12	TS11	TS10	TS9	TS8	TIR2
TS23	TS22	TS21	TS20	TS19	TS18	TS17	TS16[1]	TIR3
TS31	TS30	TS29	TS28	TS27	TS26	TS25	TS24	TIR4

Symbol	Position	Name And Description
TS31 TS0	TIR4.7 TIR1.0	Transmit Idle Registers. Each of these bit positions represents a time slot in the outgoing stream at TPOS and TNEG. When set, the contents of that time slot are forced to idle code (11010101).

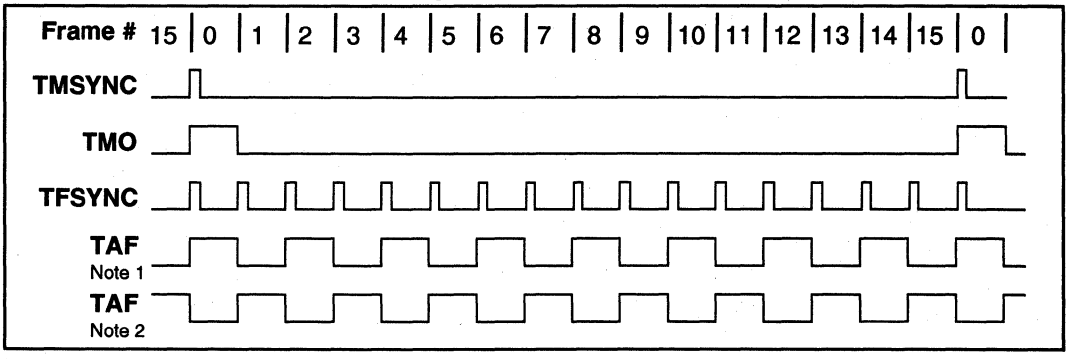
extra bits (see Figure 11) are sourced from TXR.0, TXR.1 and TXR.3 (TCR.2 = 1) or the extra bits are sampled externally at TXD during the extra bit time (TCR.2 = 0). The extra bits, alignment pattern and alarm signal are not utilized in the CCS mode (TCR.5 = 1), input TSER "overwrites" all time slot 16 bit positions.

Reserved bit positions in the TXR must be set to 0 when written, those bits may be 0 or 1 when read.

Transmit Timing

A low-high transition at TMSYNC once per multiframe (every 2 ms) or at a multiple of the multiframe rate establishes outgoing CAS and/or CRC4 multiframe alignment. Output TMO indicates that alignment. A low-high transition at TFSYNC at the frame rate (125 µs) or at a multiple of the frame rate establishes the outgoing frame position. Output TAF indicates that alignment.

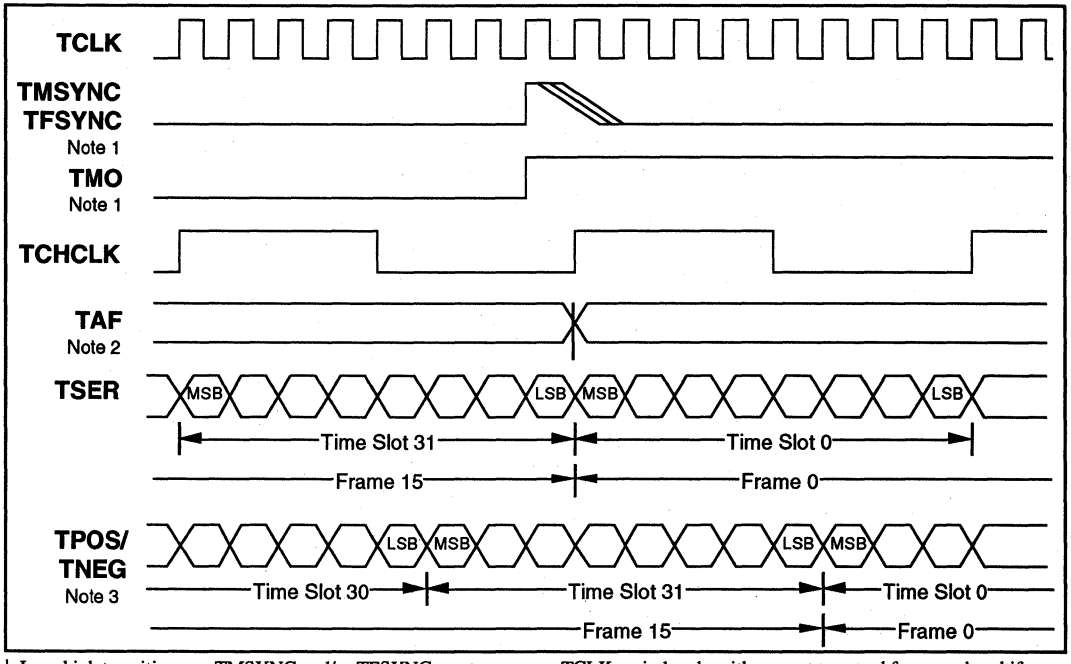
Figure 13: Transmit Multiframe Timing



[1] Alignment frames are "even" frames of the CAS and/or CRC4 multiframes (CCR.6 = 0).

[2] Alignment frames are "odd" frames of the CAS multiframe (CCR.6 = 1).

Figure 14: Transmit Multiframe Boundary Timing



[1] Low-high transitions on TMSYNC and/or TFSYNC must occur one TCLK period early with respect to actual frame and multiframe boundaries. TMO follows the rising edge of TMSYNC or TFSYNC.

[2] TAF transitions on true frame boundaries.

[3] Delay from TSER to TPOS, TNEG is five TCLK periods.

TMSYNC and/or TFSYNC may be tied low by the user, in which case the arbitrary frame and multiframe alignment established by the device will be indicated at TMO and TAF.

Output TAF also indicates frames containing the frame alignment signal. Those frames may be "even or odd" numbering frames of the outgoing CAS multiframe (CCR.6).

Receive Signaling

Receive signaling data is available at two outputs; RSER and RSD (see Figure 16). RSER outputs the signaling data in time slot 16. The signaling data is also extracted from time slot 16 and presented at RSD during the time slots shown in Table 8.

Table 8: Receive Signaling

Frame #	RSD[1] Valid During Time Slot #
0	15[2]
1	17[2]
2	1, 18
3	2, 19
4	3, 20
5	4, 21
6	5, 22
7	6, 23
8	7, 24
9	8, 25
10	9, 26
11	10, 27
12	11, 28
13	12, 29
14	13, 30
15	4, 31

Notes: Applicable only to CAS systems.

[1] RSD is valid for the least significant nibble in each indicated time slot. Time slot A data appears in bit 5, B in bit 6, C in bit 7, and D in bit 8.

[2] RSD does not output valid data during time slots 0 and 16.

Figure 15: Transmit Signaling Time Slot Timing

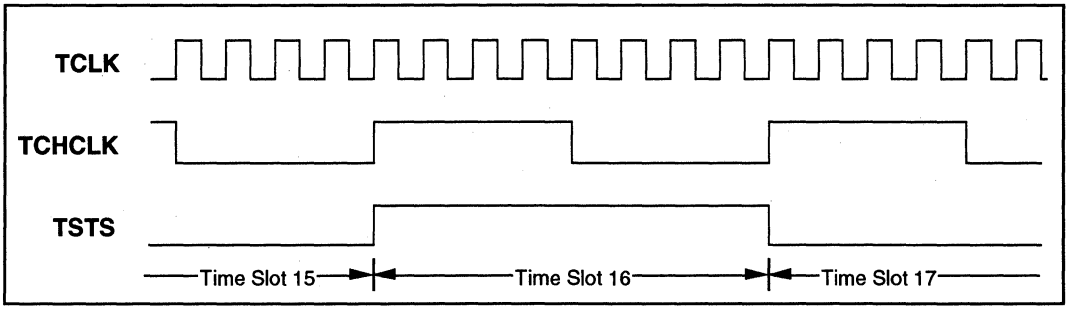
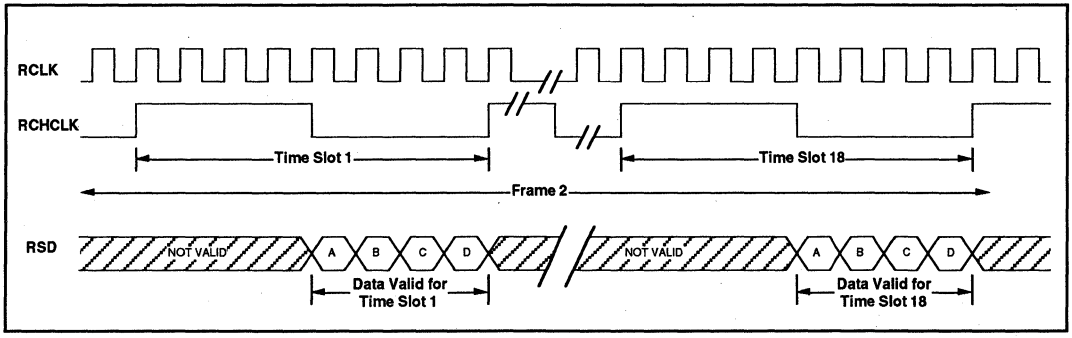


Figure 16: RSD Timing



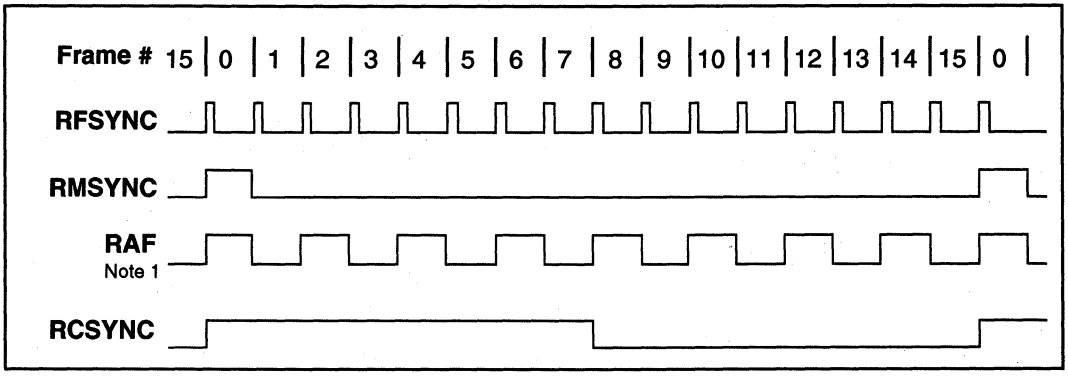
Receive Timing

The receive side output timing set is identical to that found on the transmit side. The user may tie receive outputs directly to the transmit inputs for "drop and insert" applications. The received data at RPOS and RNEG appears at RSER after six RCLK delays, without any change except for the HDB3 to NRZ conversion when HDB3 is enabled.

Alarm Reporting and Interrupt Servicing

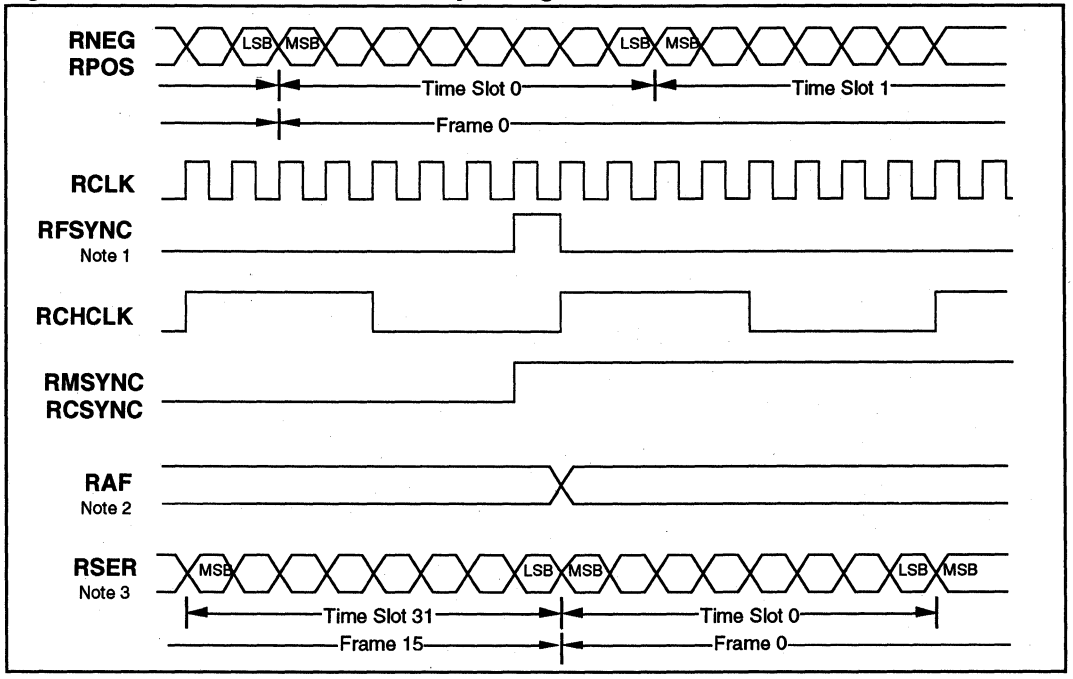
Alarm and error conditions are reported at outputs and the RSR. Use of the RSR and error count registers simplifies system error monitoring. The RSR may be read in one of two ways; a burst read does not disturb the RSR contents, a direct read will clear all bits set in the RSR unless the alarm condition which set them is still active.

Figure 17: Receive Multiframe Timing



[1] The CAS multiframe may start with an align or non-align frame. The CRC4 multiframe always starts with an align frame.

Figure 18: Receive Multiframe Boundary Timing



[1] Low-high transitions on RMSYNC and RFSYNC occur one RCLK period early with respect to actual frame and multiframe boundaries.

[2] RAF transitions on true frame boundaries.

[3] Delay from RPOS, RNEG to RSER is six RCLK periods.

Interrupts are enabled via the RIMR and are generated whenever an alarm or error condition sets an RSR bit. The host controller must service the transceiver in order to clear an interrupt condition. Clearing the appropriate RIMR bit will unconditionally clear an interrupt.

Error Logging

The BVCR, CECR and FECR contain 8-bit binary up counters which increment on individual bipolar violations, CRC4 code word errors (when CCR.2 = 1), and word errors in the frame alignment signal. Each counter saturates at 255. Once saturated, each following error occurrence will generate an interrupt (RIMR.0 = 1) until the register is reprogrammed to a value other than FF (hex). Presetting the registers allows the user to establish specific error count thresholds; the counter will count "up" to saturation from the preset value. The BVCR increments at all times (regardless of sync status). CECR and FECR increments are disabled whenever resync is in progress (RLOS high).

Alarm Outputs

Alarm conditions are also reported in real time at alarm outputs. These outputs may be used with off-chip logic to complement the on-chip error reporting capability of the LXP2181A. In the Hardware mode, they are the only alarm reporting means available.

RLOS

The RLOS output indicates the status of the receive synchronizer. When high, frame, CAS multiframe and/or CRC4

Figure 19: Receive Status Register (RSR)

(MSB)							(LSB)
RRA	RDMA	RSA1	RUA1	FSERR	MFSERR	RLOS	ECS

Symbol	Position	Name And Description
RRA	RSR.7	Receive Remote Alarm. Set when bit 3 of time slot 0 in non-align frames set for three consecutive non-align frames.
RDMA	RSR.6	Receive Distant Multiframe Alarm[1]. Set when bit 6 of time slot 16 in frame 0 set for three consecutive multiframes.
RSA1	RSR.5	Receive Signaling All "1"s. Set when contents of time slot 16 have been all "1"s for two consecutive frames.
RUA1	RSR.4	Receive Unframed All "1"s. Set when <3 bit positions of the last align and non-align frames received have been 0.
FSERR	RSR.3	Frame Resync Criteria Met. Set when the Frame Error Criteria is met, also the Frame Resync is initiated if RCR.1 = 0.
MFSERR	RSR.2	CAS Multiframe Resync Criteria Met. Set when the CAS multiframe error criteria is met, also the Frame Resync is initiated if RCR.1 = 0.
RLOS	RSR.1	Receive Loss of Sync. Set when resync is in progress.
ECS	RSR.0	Error Count Saturation. Set when any of the on-chip counters at FECR, CECR or BVCR saturates.

[1] When in the CCS mode, the RDMA flag bit and the RDMA pin have no significance. It will be set when bit 6 of time slot 16 in frame 0 is set for three consecutive multiframes in either CAS or CCS mode.

multiframe synchronization is in progress. A high-low transition indicates resync is complete. The RLOS bit (RSR.1) is a "latched" version of the RLOS output.

RRA

The remote alarm output transitions high when a remote alarm is detected. A high-low transition indicates the alarm condition has been cleared. The alarm condition is defined as bit 3 of time slot 0 set for three consecutive non-align frames. The alarm state is cleared when bit 3 has been clear for three consecutive non-align frames. The RRA bit (RSR.7) is a "latched" version of the RRA output.

RBV

RBV outputs one RCLK pulse when the accused bit emerges at RSER. RBV will return low when RCLK goes low, and RBV pin bipolar violations are logged in the BVCR. The RBV pin provides a pulse which can be counted externally for every violation.

RDMA

RDMA transitions high when bit 6 of time slot 16 in frame 0 is set for three consecutive occasions and returns low when the bit is clear for three consecutive occasions. The RDMA bit (RSR.6) is a "latched" version of the RDMA output.

RCL

Transitions high after 32 consecutive "0s" appear at RPOS and RNEG, goes low at next "1" occurrence.

RFER

The RFER output transitions high when received frame alignment, CAS multiframe alignment and/or CRC4 code words are in error. The FECR and CECR log error events

Figure 20: Receive Interrupt Mask Register (RIMR)

(MSB)							(LSB)
RRA	RDMA	RSA1	RUA1	FSERR	MFSERR	RLOS	ECS

Symbol	Position	Name And Description
RRA	RIMR.7	Receive Remote Alarm. 1 = Interrupt Enabled. 0 = Interrupt Masked.
RDMA	RIMR.6	Receive Distant Multiframe Alarm. 1 = Interrupt Enabled. 0 = Interrupt Masked.
RSA1	RIMR.5	Receive Signaling All "1"s. 1 = Interrupt Enabled. 0 = Interrupt Masked.
RUA1	RIMR.4	Receive Unframed All "1"s. 1 = Interrupt Enabled. 0 = Interrupt Masked.
FSERR	RIMR.3	Frame Resync Criteria Met 1 = Interrupt Enabled. 0 = Interrupt Masked.
MFSERR	RIMR.2	CAS Multiframe Resync Criteria Met. 1 = Interrupt Enabled. 0 = Interrupt Masked.
RLOS	RIMR.1	Receive Loss of Sync. 1 = Interrupt Enabled. 0 = Interrupt Masked.
ECS	RIMR.0	Error Count Saturation. 1 = Interrupt Enabled. 0 = Interrupt Masked.

reported at this output. FECR logs only the Frame Alignment errors. CECR logs CRC4 code word errors.

To complement the on-chip error logging capabilities of the LXP2181A, the system designer may use off-chip logic gated by receive side outputs RCHCLK, RAF, RSTS and RCSYNC to demux error states present at RFER.

Reset

A high-low transition on $\overline{RST}$ clears all internal registers except the three error counters; a resync is initiated until $\overline{RST}$ returns high. $\overline{RST}$ must be held low on system power-up and when switching to/from the Hardware mode. Following reset, the host processor should update all on-chip registers to establish desired operating modes.

Figure 21: Bipolar Violation Count Register (BVCR)

(MSB)							(LSB)
BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0

Symbol	Position	Name And Description
BVD7	BVCR.7	MSB of bipolar violation count.
BVD0	BVCR.0	LSB of bipolar violation count.

Figure 22: CRC4 Error Count Register (CECR)

(MSB)							(LSB)
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CEC0

Symbol	Position	Name And Description
CRC7	CECR.7	MSB OF CRC4 error count.
CRC0	CECR.0	LSB of CRC4 error count.

Figure 23: Frame Error Count Register (FECR)

(MSB)							(LSB)
FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0

Symbol	Position	Name And Description
FE7	FECR.7	MSB of frame error count.
FE0	FECR.0	LSB of frame error count.

Figure 24: RFER Output Timing for All Error Conditions

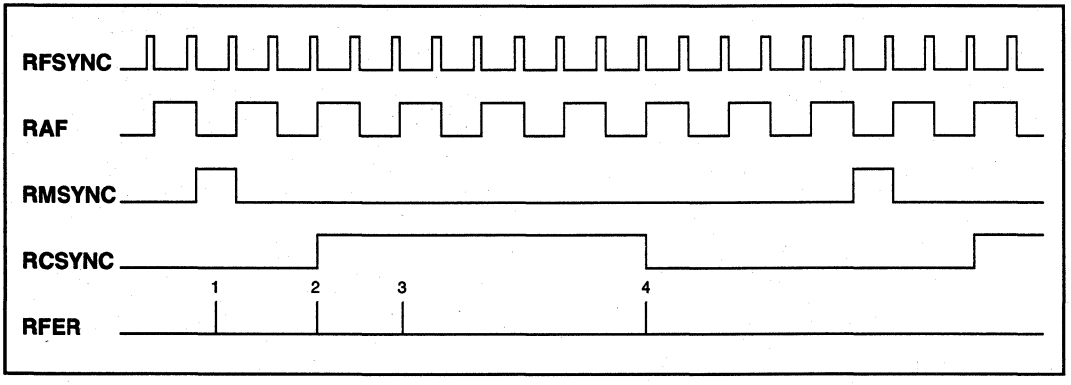


Figure 25: CAS Multiframe Alignment Error

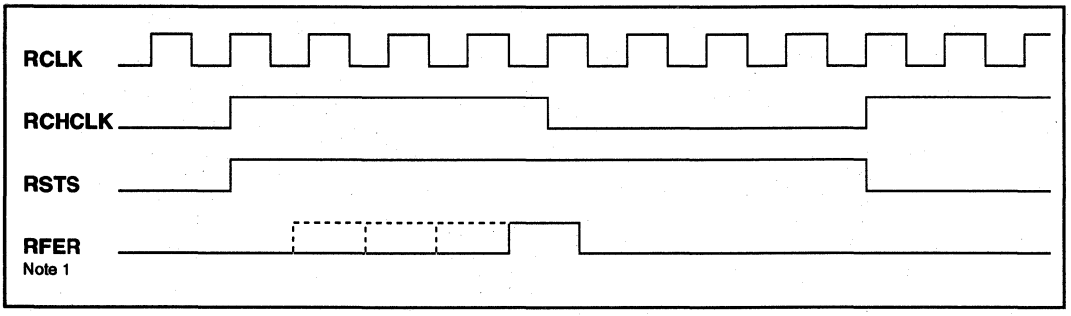
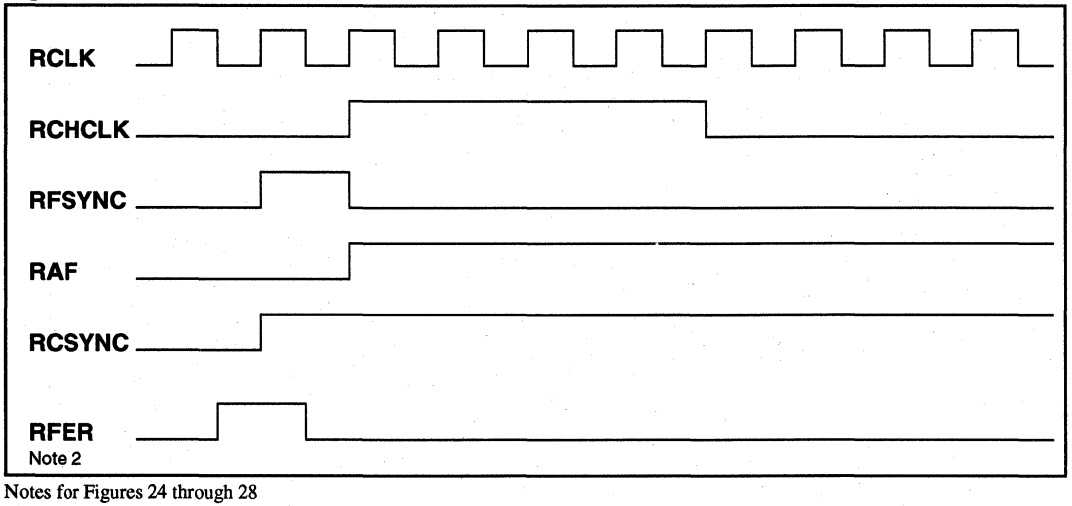


Figure 26: CRC4 Sub-Multiframe 2 Errored



Notes for Figures 24 through 28

[1] CAS multiframe alignment word received in error, RFER will transition high at first error occurrence and remain high as shown.

[2] Previous CRC4 sub-multiframe 2 errored.

[3] Frame alignment word errored.

[4] Previous CRC4 sub-multiframe errored.

Figure 27: Frame Alignment Word Errored

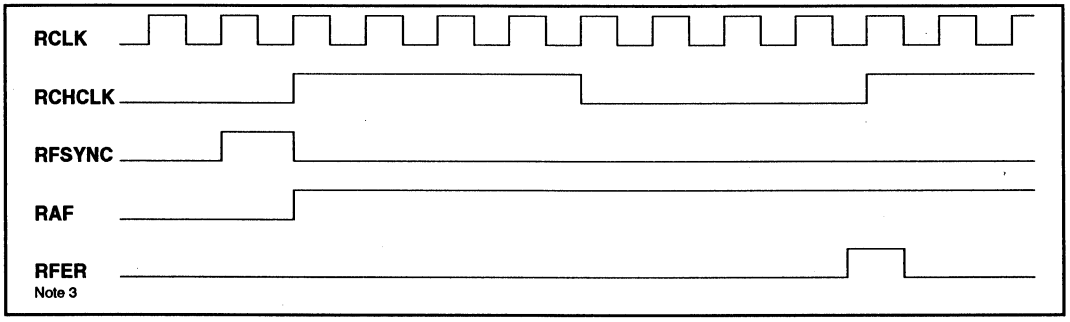
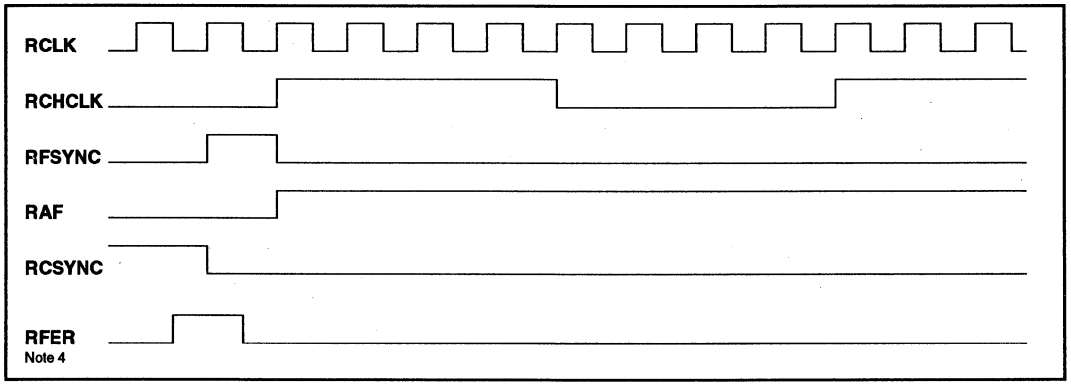


Figure 28: CRC4 Sub-Multiframe 1 Errored



Notes for Figures 27 and 28

[3] Frame alignment word errored.

[4] Previous CRC4 sub-multiframe errored.

Hardware Mode

An on-chip hardware control mode simplifies preliminary system prototyping and serves applications which do not require the features of the serial port. Tying SPS low disables the serial port, clears all internal register locations except those in Table 9 and redefines pins 14 thru 18 as mode control inputs. The mode control inputs establish the device operational characteristics listed in Table 9. The Hardware mode simplifies device retrofit into existing applications where control interfaces are designed with discrete logic.

Table 9: Hardware Mode Control

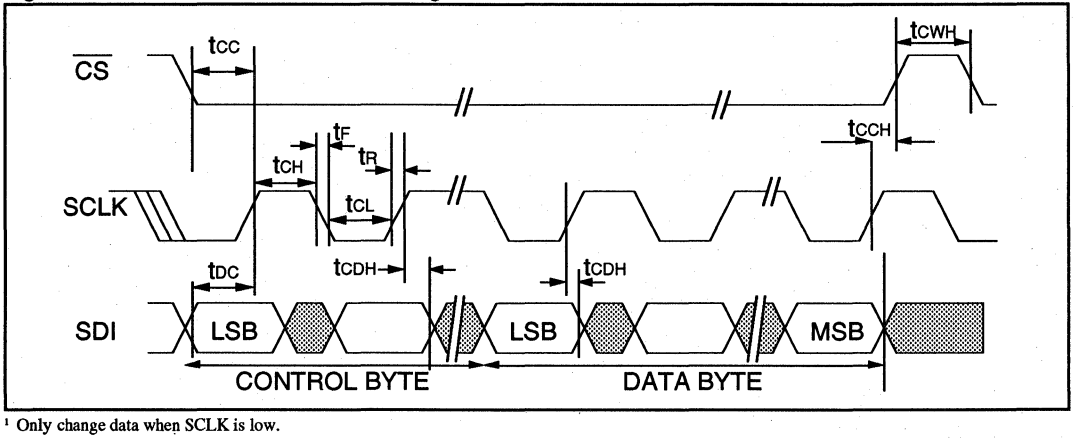
Pin #	Register Location	Name And Description
14	TINR.5	TRA - Transmit Remote Alarm 0 = Normal Operation. 1 = Enable Alarm.
15	TXR.2	TDMA - Transmit Distant Multiframe Alarm. 0 = Normal Operation. 1 = Enable Alarm.
16	CCR.5 / CCR.4	Data Format. 0 = Input/output data AMI coded. 1 = Input/output data HDB3 coded.
17	CCR.3 / CCR.2	Transmit and Receive CRC4 Multiframe. 0 = Disabled. 1 = Enabled.
18	TCR.5 / RCR.5	Transmit and Receive CAS Multiframe. 0 = Enabled. 1 = Disabled.

A.C. Electrical Characteristics - Serial Port

Parameter	Sym	Min	Max	Units	Test Conditions[1]
SDI to SCLK Setup	t_{DC}	50	–	ns	C load = 100 pF
SCLK to SDI Hold	t_{CDH}	50	–	ns	C load = 100 pF
SCLK Low Time	t_{CL}	244	–	ns	C load = 100 pF
SCLK High TIme	t_{CH}	244	–	ns	C load = 100 pF
SCLK Rise and Fall Time	t_F, t_F	–	100	ns	C load = 100 pF
$\overline{CS}$ to SCLK Setup	t_{CC}	50	–	ns	C load = 100 pF
SCLK to $\overline{CS}$ Hold	t_{CCH}	50	–	ns	C load = 100 pF
$\overline{CS}$ Inactive Time	t_{CWH}	250	–	ns	C load = 100 pF
SCLK to SDO Valid	t_{CDV}	–	200	ns	C load = 100 pF
$\overline{CS}$ to SDO High Z	t_{CDZ}	–	75	ns	C load = 100 pF

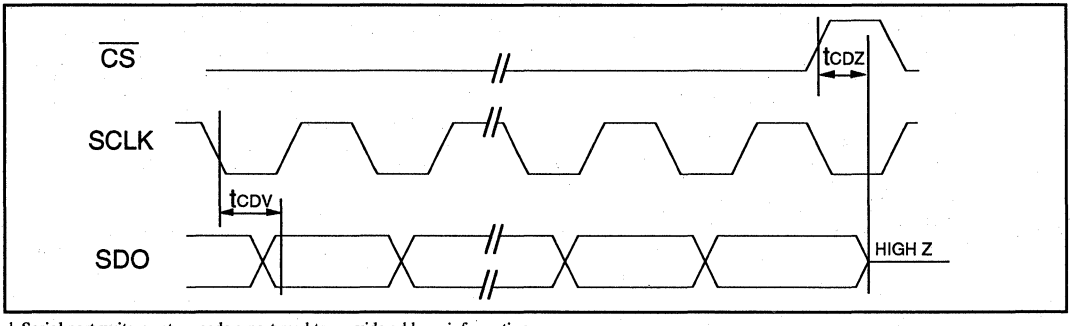
[1] Measured at V_{IH} = 2.0V, V_{IL} = .8V, and 10 ns maximum rise and fall time.
T_A = -40°C to +85°C (E version); 0°C to +70°C (C version). V_{DD} = 5V (± 5V).

Figure 29: Serial Port Write A.C. Timing



[1] Only change data when SCLK is low.
[2] Shaded regions indicate "don't care" states of input data.

Figure 30: Serial Port Read A.C. Timing



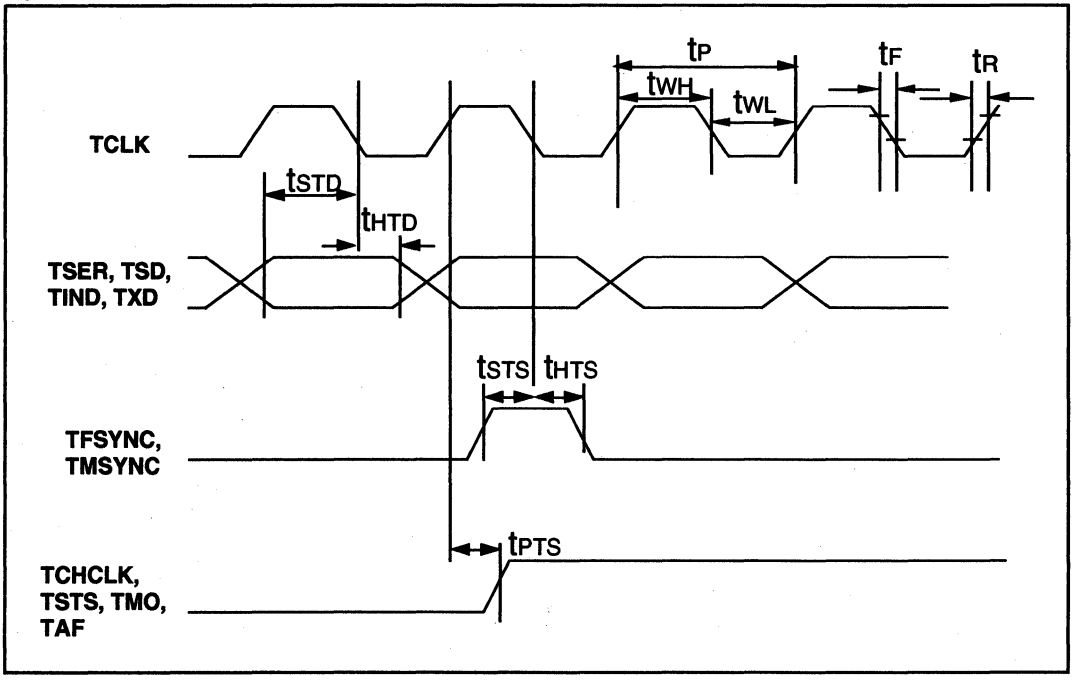
[1] Serial port write must precede a port read to provide address information.

A.C. Electrical Characteristics - Transmit[1]

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
TCLK Period	t_P	–	488	–	ns	C load = 100 pF
TCLK Pulse Width	t_{WL}, t_{WH}	–	244	–	ns	C load = 100 pF
TCLK, RCLK Rise & Fall Times	t_R, t_F	–	20	–	ns	C load = 100 pF
TSER, TSD, TIND, TXD Setup to TCLK Falling	t_{STD}	50	–	–	ns	C load = 100 pF
TSER, TSD, TIND, TXD Hold to TCLK Falling	t_{HTD}	50	–	–	ns	C load = 100 pF
TFSYNC, TMSYNC Setup to TCLK Falling	t_{STS}	75	–	125	ns	C load = 100 pF
TFSYNC , TMSYNC Hold to TCLK Falling	t_{HTS}	50	–	75	ns	C load = 100 pF
Propagation Delay TCLK to TCHCLK,	t_{PTS}	–	–	75	ns	C load = 100 pF
TSTS, TMO, TAF		100	–	–	ns	C load = 100 pF

[1] Measured at V_{IH} = 2.0V, V_{IL} = .8V, and 10 ns maximum rise and fall time.
T_A = -40°C to +85°C (E version); 0°C to +70°C (C version). V_{DD} = 5V (± 5V).
[2] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 31: Transmit A.C. Timing Diagram

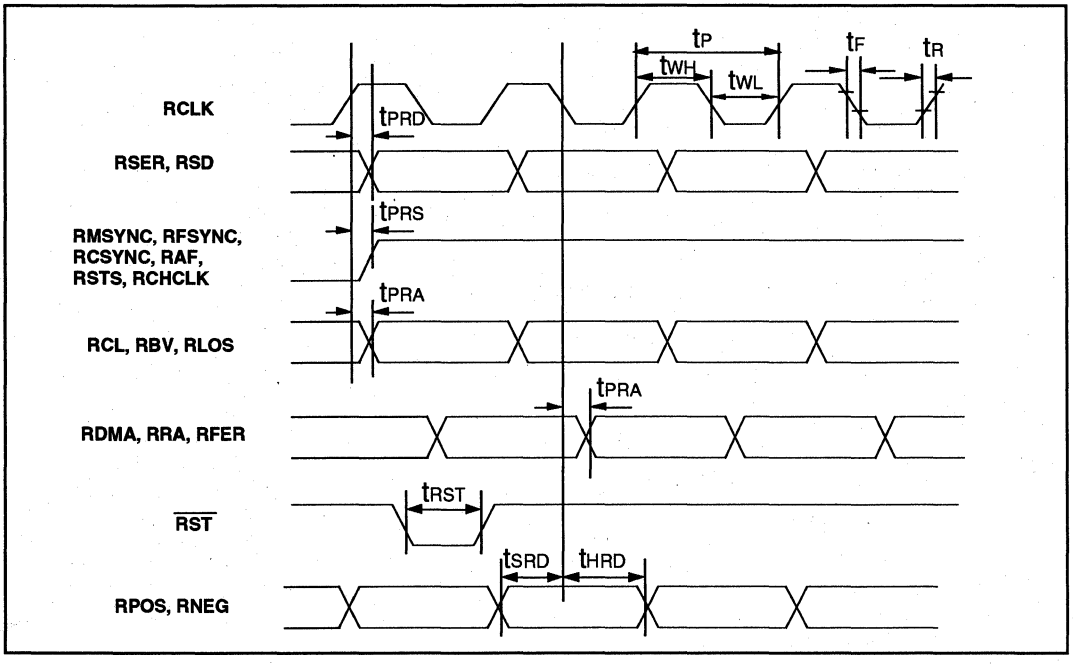


A.C. Electrical Characteristics - Receive[1]

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
Propagation Delay RCLK to RMSYNC, RFSYNC, RSTS, RCHCLK, RAF	t_{PRS}	–	–	75	ns	CL = 100 pF
Propagation Delay RCLK to RSER, RSD	t_{PRD}	–	–	75	ns	CL = 100 pF
Transition Time, All Outputs	t_{TTR}	–	–	20	ns	C load = 100 pF
RCLK Period	t_P	–	488	–	ns	C load = 100 pF
RCLK Pulse Width	t_{WL}, t_{WH}	–	244	–	ns	C load = 100 pF
RCLK Rise & Fall Times	t_R, t_F	–	20	–	ns	C load = 100 pF
RPOS, RNEG Setup to RCLK Falling	t_{SRD}	50	–	–	ns	C load = 100 pF
RPOS, RNEG Hold to RCLK Falling	t_{HRD}	50	–	–	ns	C load = 100 pF
Propagation Delay RCLK to RLOS, RRA, RBV, RFER, RDMA, RCL	t_{PRA}	–	–	75	ns	C load = 100 pF
Minimum $\overline{RST}$ Pulse Width on System Power Up or Restart	t_{RST}	1	–	–	µs	C load = 100 pF

[1] Measured at V_{IH} = 2.0V, V_{IL} = .8V, and 10 ns maximum rise and fall time.
[2] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 32: Receive A.C. Timing Diagram



Local Area Networking Products

1994 Communications Data Book

LEVEL ONE®

LXT901

Universal Ethernet Interface Adapter (Internal MAU)

with Integrated 10Base T MAU, EnDec, AUI and Filters

General Description

The LXT901 Universal Ethernet Interface Adapter is designed for IEEE 802.3 physical layer applications. It provides all the active circuitry to interface most standard 802.3 controllers to either the 10Base-T media or Attachment Unit Interface (AUI). In addition to standard 10 Mbps Ethernet, the LXT901 also supports full-duplex operation at 20 Mbps.

LXT901 functions include Manchester encoding/decoding, receiver squelch and transmit pulse shaping, jabber, link testing and reversed polarity detection/correction. The LXT901 can be used to drive either the AUI drop cable or the 10Base-T twisted-pair cable with only a simple isolation transformer. No external filters are required. Selectable termination impedance allows the LXT901 to be used with either shielded or unshielded twisted-pair cable.

The LXT901 is fabricated with an advanced CMOS process and requires only a single 5-volt power supply.

Applications

- Laptop/Palmtop portables (PCMCIA compatibles)
- Computer/workstation 10Base-T LAN adapter boards

Key Features

Functional Features

- Integrated Filters - No External Filters Required
- Integrated Manchester Encoder/Decoder
- 10Base-T compliant Transceiver
- AUI Transceiver
- Supports Standard and Full-Duplex Ethernet

Convenience Features

- Automatic/Manual AUI/RJ45 Selection
- Automatic Polarity Correction
- Programmable Impedance Driver
- Power Down Mode and four loopback modes
- Available in 64-pin TQFP and 44-pin PLCC packages

Diagnostic Features

- Four LED Drivers
- AUI/RJ45 Loopback
- Remote Signaling of Link Down and Jabber conditions

3

Figure 1: LXT901 Block Diagram

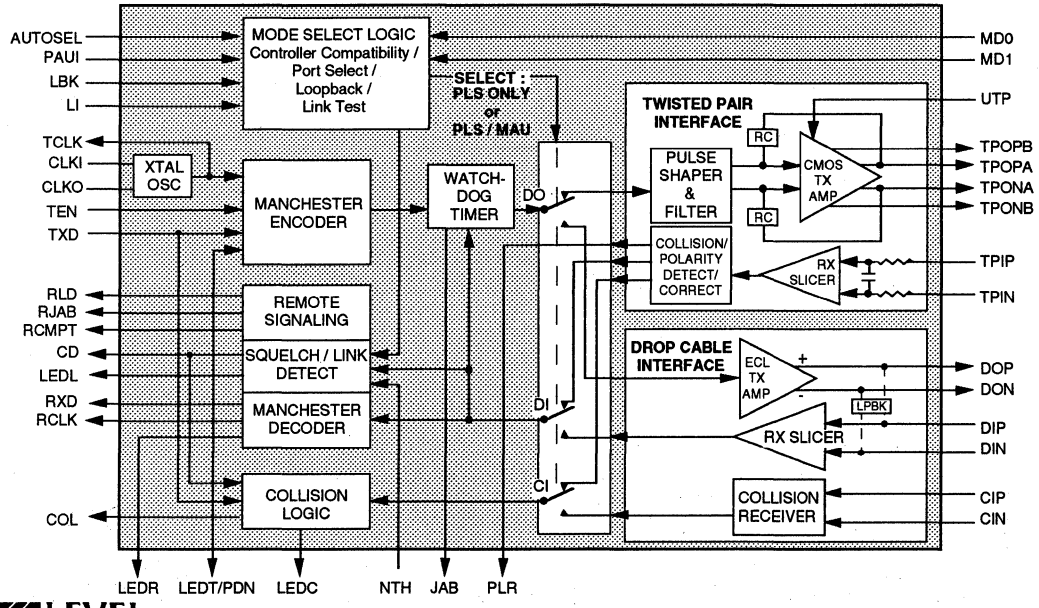


Table 1: Controller Compatibility Mode Options

Controller Mode:	Setting: MD1	MD0
Mode 1 - For Advanced Micro Devices AM7990 or compatible controllers	0	0
Mode 2 - For Intel 82586, 82596 or compatible controllers	0	1
Mode 3 - For Fujitsu MB86950, MB86960 or compatible controllers (Seeq 8005)	1	0
Mode 4 - For National Semiconductor 8390 or compatible controllers (TI TMS380C26)	1	1

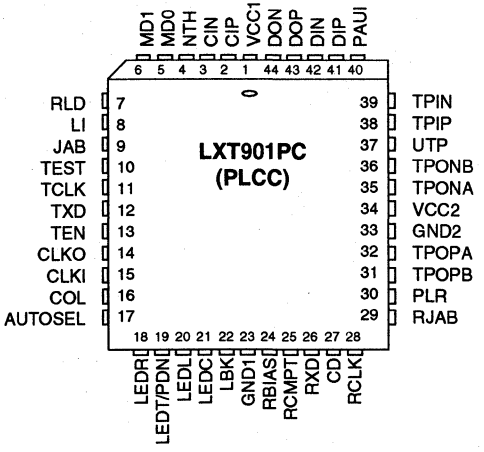


Table 2: Pin Descriptions

PLCC	TQFP	Sym	I/O	Name	Description
1 34 –	10 56 9	VCC 1 VCC 2 VCCA	I I I	Power Inputs 1, 2 and A (TQFP only)	+ 5 volt power supply inputs.
2 3	11 12	CIP CIN	I I	AUI Collision Pair	Differential input pair connected to the AUI transceiver CI circuit. The input is collision signaling or SQE.
4	13	NTH	I	Normal Threshold	When NTH = 1, the normal TP squelch threshold is in effect. When NTH = 0, the normal TP squelch threshold is reduced by 4.5 dB.
5 6	14 15	MD0 MD1	I I	Mode Select 0 Mode Select 1	Mode select pins determine controller compatibility mode in accordance with Table 1, above.
7	18	RLD	O	Remote Link Down	Output goes high to signal to the controller that the remote port is in link down condition.
8	19	LI	I	Link Test Enable	Controls Link Integrity Test; enabled when LI = 1, disabled when LI = 0.
9	21	JAB	O	Jabber Indicator	Output goes high to indicate Jabber state.
10	22	TEST	I	Test	Open.
11	23	TCLK	O	Transmit Clock	A 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller.
12	24	TXD	I	Transmit Data	Input signal containing NRZ data to be transmitted on the network. TXD is connected directly to the transmit data output of the controller.
13	25	TEN	I	Transmit Enable	Enables data transmission and starts the watchdog timer. Synchronous to TCLK (see Figures 4, 10, 16 and 22 for details).
14 15	26 27	CLKO CLKI	O I	Crystal Oscillator	A 20 MHz crystal (Mtron MP-1/MP-2) must be connected across these pins, or a 20 MHz clock applied at CLKI with CLKO left open.
16	28	COL	O	Collision Detect	Output which drives the collision detect input of the controller.
17	29	AUTO SEL	I	Automatic Port Select	When AUTOSEL = 1, automatic port selection is enabled (the 901 defaults to the AUI port only if TP link integrity = Fail). When AUTOSEL = 0, manual port selection is enabled (the PAUI pins determines the active port).

Table 2: Pin Descriptions continued

PLCC	TQFP	Sym	I/O	Name	Description
18	34	LEDR	O	Receive LED	Open drain driver for the receive indicator LED. Output is pulled low during receive.
19	35	LEDT/ PDN	O I	Transmit LED/ Power Down	Open drain driver for the transmit indicator. Output is pulled low during transmit. If externally tied low, the LXT901 goes to power down state.
20	36	LEDL	O	Link LED	Open drain driver for link integrity indicator. Output is pulled low during link test pass. If externally tied low, internal circuitry is forced to "Link Pass" state and 901 will continue to transmit link test pulses.
21	37	LEDC	O	Collision LED	Open drain driver for the collision indicator pulls low during collision. If externally tied low, the LXT901 disables the internal TP loopback and collision detect circuits for full-duplex operation or external TP loopback.
22	38	LBK	I	Loopback	Enables internal loopback mode. See Figure 7 (Mode 1), Figure 13 (Mode 2), Figure 19 (Mode 3) and Figure 25 (Mode 4) for details.
23 33 –	39 55 40	GND1 GND2 GNDA	– – –	Ground Returns 1, 2 and A (TQFP only)	Grounds.
24	42	RBIAS	I	Bias Control	A 12.4 kΩ 1% resistor to ground at this pin controls operating circuit bias.
25	44	RCMPT	O	Remote Compatibility	Output goes high to signal the controller that the remote port is compatible with the LXT901 remote signaling features.
26	45	RXD	O	Receive Data	Output signal connected directly to the receive data input of the controller.
27	46	CD	O	Carrier Detect	An output to notify the controller of activity on the network.
28	47	RCLK	O	Receive Clock	A recovered 10 MHz clock which is synchronous to the received data and connected to the controller receive clock input.
29	51	RJAB	O	Remote Jabber	Output goes high to indicate that the remote port is in Jabber condition.
30	52	PLR	O	Polarity Reverse	Output goes high to indicate reversed polarity at the TP input.
31 36 32 35	53 58 54 57	TPOPB TPONB TPOPA TPONA	O O O O	Twisted-Pair Transmit Pairs A & B	Two differential driver pair outputs (A and B) to the twisted-pair cable. The outputs are pre-equalized; no external filters are required. Two pairs are used to provide compatibility with both 100 Ω load cable and 150 Ω load cable.
37	59	UTP	I	UTP / STP Select	When UTP = 0, 150 Ω termination for shielded TP is selected. When UTP = 1, 100 Ω termination for unshielded TP is selected.
38 39	61 62	TPIP TPIN	I I	Twisted-Pair Receive Pair	A differential input pair from the twisted-pair cable. Receive filter is integrated on-chip. No external filters are required.
40	3	PAUI	I	Port/AUI Select	In Manual Port Select mode (AUTOSEL = 0), PAUI selects the active port. When PAUI = 1, the AUI port is selected. When PAUI = 0, the TP port is selected. In Auto Port Select mode, PAUI must be tied to ground.
41 42	4 5	DIP DIN	I I	AUI Receive Pair	Differential input pair from the AUI transceiver DI circuit. The input is Manchester encoded.
43 44	7 8	DOP DON	O O	AUI Transmit Pair	A differential output driver pair for the AUI transceiver cable. The output is Manchester encoded.

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Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- Supply Voltage V_{CC} - 0.3 V (min) to + 6 V (max)
- Operating temperature T_{OP} 0 °C (min) to +70 °C (max)
- Storage temperature T_{ST} -65 °C (min) to +150 °C (max)

Table 3: Operating Conditions (Voltage with respect to ground unless otherwise specified.)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Recommended supply voltage		V_{CC}	4.75	5.0	5.25	V	
Recommended operating temperature		T_{OP}	0	-	70	°C	
Supply current		I_{CC}	–	65	85	mA	Idle mode
	Normal mode	I_{CC}	–	90	110	mA	Transmitting on TP
		I_{CC}	–	70	90	mA	Transmitting on AUI
	Power Down mode	I_{CC}	–	0.75	2	mA	

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 4: I/O Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input low voltage [2]		V_{IL}	–	–	0.8	V	
Input high voltage [2]		V_{IH}	2.0	–	–	V	
Output low voltage		V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
Output low voltage		V_{OL}	–	–	10	% V_{CC}	I_{OL} < 10 µA
Output low voltage (Open drain LED Driver)		V_{OL}	–	–	0.7	V	I_{OL} = 10 mA
Output high voltage		V_{OH}	2.4	–	–	V	I_{OH} = 40 µA
Output high voltage		V_{OH}	90	–	–	% V_{CC}	I_{OH} < 10 µA
Output rise time	CMOS	_	–	3	12	ns	C_{LOAD} = 20 pF
TCLK & RCLK	TTL	–	–	2	8	ns	
Output fall time	CMOS	–	–	3	12	ns	C_{LOAD} = 20 pF
TCLK & RCLK	TTL	–	–	2	8	ns	
CLKI rise time (externally driven)		–	–	–	10	ns	
CLKI duty cycle (externally driven)		–	–	50/50	40/60	%	

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Limited functional test patterns are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V.

Table 5: AUI Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input low current	I_{IL}	–	–	-700	µA	
Input high current	I_{IH}	–	–	500	µA	
Differential output voltage	V_{OD}	± 550	–	± 1200	mV	
Differential squelch threshold	V_{DS}	150	220	350	mV	5 MHz square wave input

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Functional Description

The LXT901 Universal Ethernet Interface Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. It functions as a PLS-Only device (for use with 10Base-2 or 10Base-5 coaxial cable networks) or as an Integrated PLS/MAU (for use with 10Base-T twisted-pair networks). In addition to standard 10Mbps operation, the LXT901 also supports full-duplex 20 Mbps operation.

The LXT901 interfaces a back end controller to either an AUI drop cable or a twisted-pair (TP) cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The AUI interface comprises three circuits: Data Output (DO), Data Input (DI) and Collision (CI). The twisted-pair interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to the three basic interfaces, the LXT901 contains an internal crystal oscillator and four LED drivers for visual status reporting.

Functions are defined from the back end controller side of the interface. The LXT901 Transmit function refers to data transmitted by the back end to the AUI cable (PLS-Only mode) or to the twisted-pair network (Integrated PLS/MAU mode). The LXT901 Receive function refers to data received by the back end from the AUI cable (PLS-Only) or from the twisted-pair network (Integrated PLS/MAU mode). In the integrated PLS/MAU mode, the LXT901 performs all required MAU functions defined by the IEEE 802.3 10Base–T specification such as collision detection, link integrity testing, signal quality error messaging, jabber control and loopback. In the PLS-Only mode, the LXT901 receives incoming signals from the AUI DI circuit with ± 18 ns of jitter and drives the AUI DO circuit.

3

Table 6: TP Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	Z_{OUT}	–	5	–	Ω	
Peak differential output voltage	V_{OD}	3.3	3.5	3.7	V	Load = 100 Ω at TPOP and TPON
Transmit timing jitter addition [2]	–	–	± 6.4	± 10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections [2,3]	–	–	± 3.5	± 5.5	ns	After line model specified by IEEE 802.3 for 10Base-T internal MAU
Receive input impedance	Z_{IN}	–	20	–	kΩ	Between TPIP/TPIN, CIP/CIN & DIP/DIN
Differential squelch threshold (Normal threshold : NTH = 1)	V_{DS}	300	420	585	mV	5 MHz square wave input
Differential squelch threshold (Reduced threshold : NTH = 0)	V_{DSL}	180	250	345	mV	5 MHz square wave input

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Parameter is guaranteed by design; not subject to production testing.
[3] IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 7: Switching Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ	Max	Units
Jabber Timing:					
Maximum transmit time	–	20	–	150	ms
Unjab time	–	250	–	750	ms
Link Integrity Timing:					
Time link loss	–	65	–	66	ms
Time between Link Integrity Pulses	–	8	–	24	ms
Interval for valid receive Link Integrity Pulses	–	4.1	–	65	ms

Controller Compatibility Modes

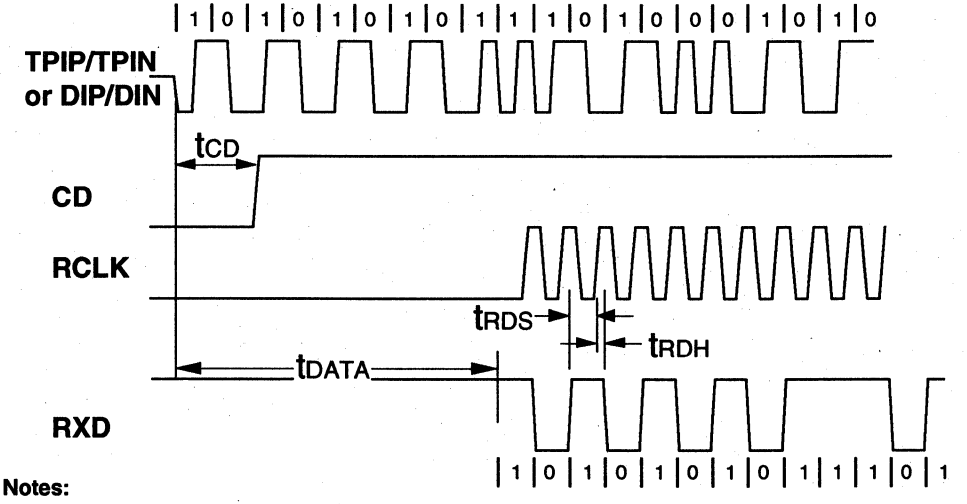
The LXT901 is compatible with most industry standard controllers including devices produced by Advanced Micro Devices (AMD), Intel, Fujitsu, National Semiconductor, Seeq and Texas Instruments. Four different control signal timing and polarity schemes (Modes 1 through 4) are required to achieve this compatibility. Mode select pins (MD0 and MD1) determine Controller compatibility modes as listed in Table 1.

A complete set of timing diagrams is provided for each mode as follows:
Mode 1 : Figures 2 - 7,
Mode 2 : Figures 8 - 13,
Mode 3 : Figures 14 - 19,
Mode 4 : Figures 20 - 25.

Related timing specifications are provided in Table 8 (RCLK/Start-of-Frame), Table 9 (RCLK/End-of-Frame), Table 10 (Transmit Timing) and Table 11 (Collision Detection, COL/CI Output and Loopback Timing).

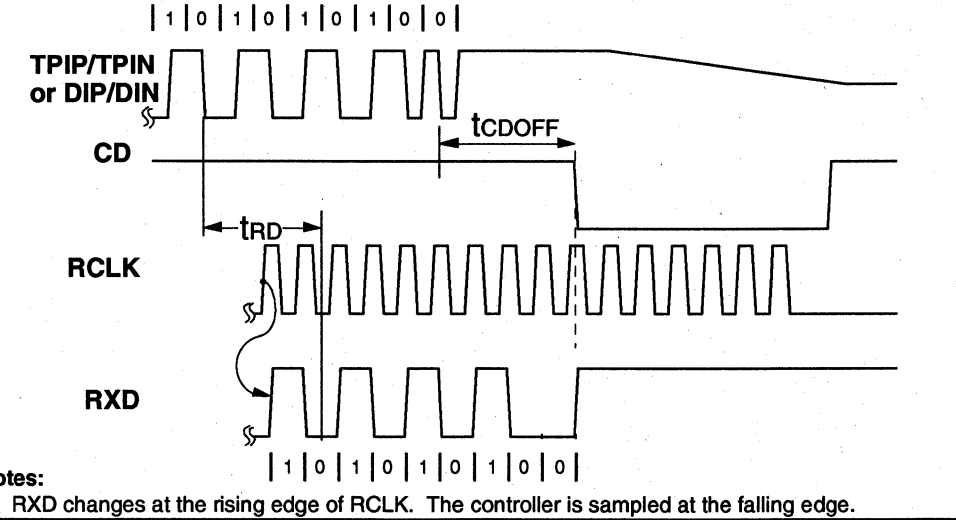
Figures 2 through 7 - Timing Diagrams for Mode 1 (MD1 = 0, MD0 = 0)

Figure 2: Mode 1 RCLK/SoF Timing



Notes:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 3: Mode 1 RCLK/EoF Timing



Notes:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 4: Mode 1 Transmit Timing

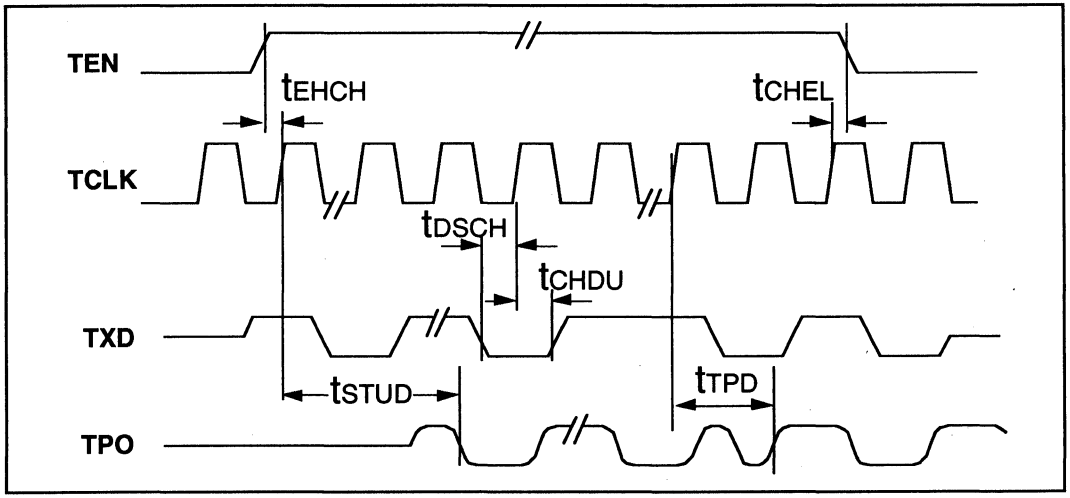


Figure 5: Mode 1 Collision Detect Timing

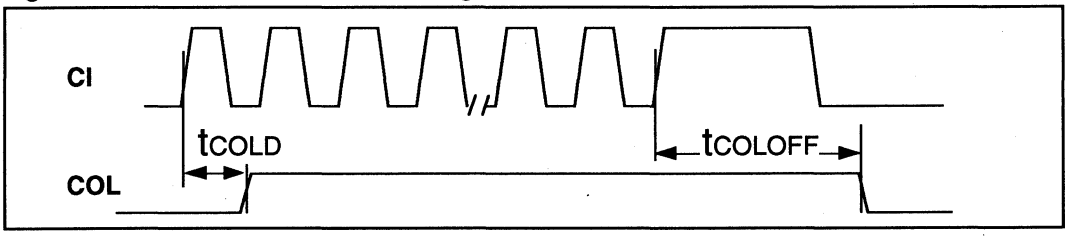


Figure 6: Mode 1 COL/CI Output Timing

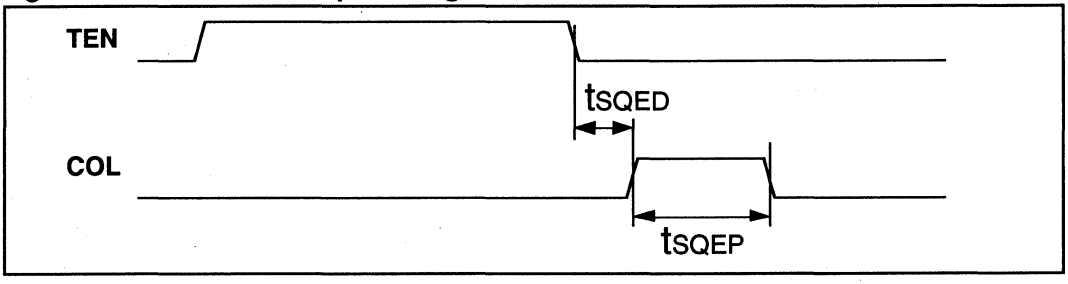
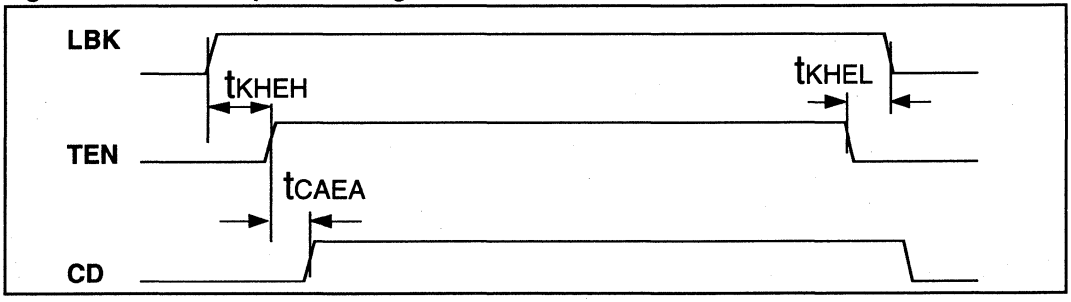
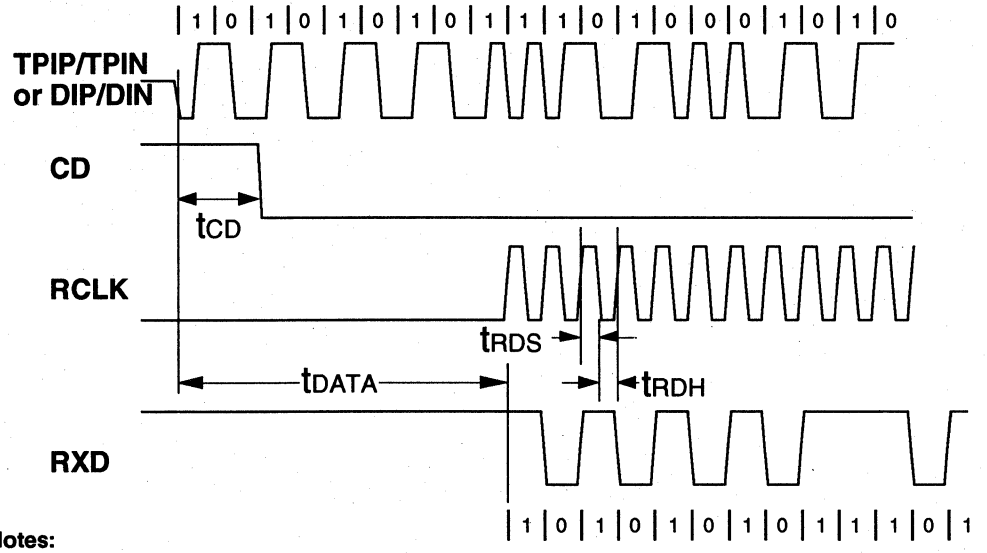


Figure 7: Mode 1 Loopback Timing



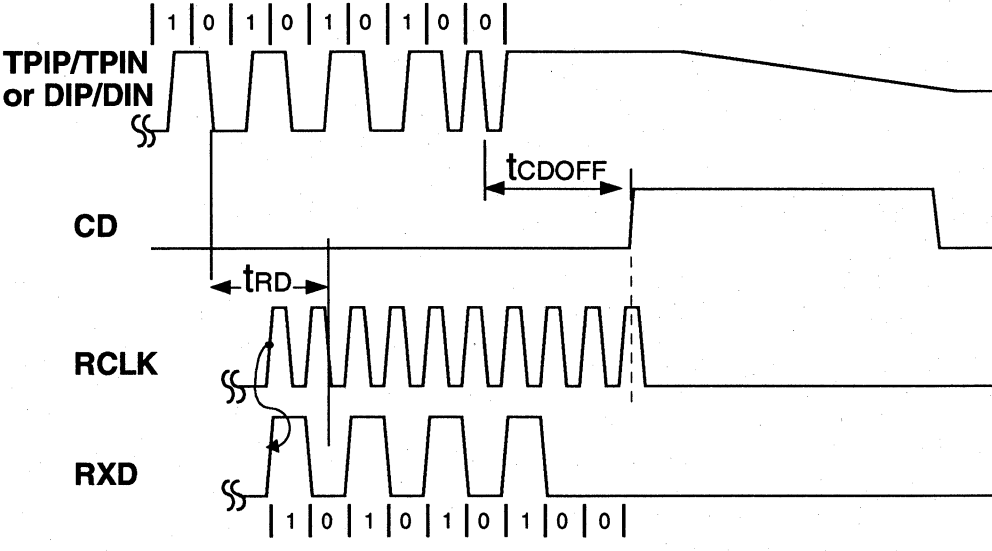
Figures 8 through 13 - Timing Diagrams for Mode 2 (MD1 = 0, MD0 = 1)

Figure 8: Mode 2 RCLK/Start-of-Frame Timing



Notes:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 9: Mode 2 RCLK/End-of-Frame Timing



Notes:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 10: Mode 2 Transmit Timing

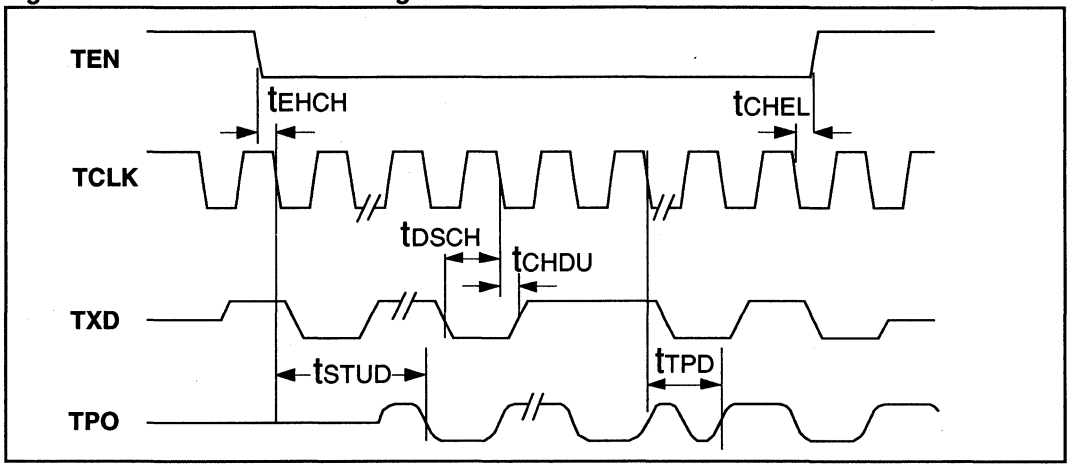


Figure 11: Mode 2 Collision Detect Timing

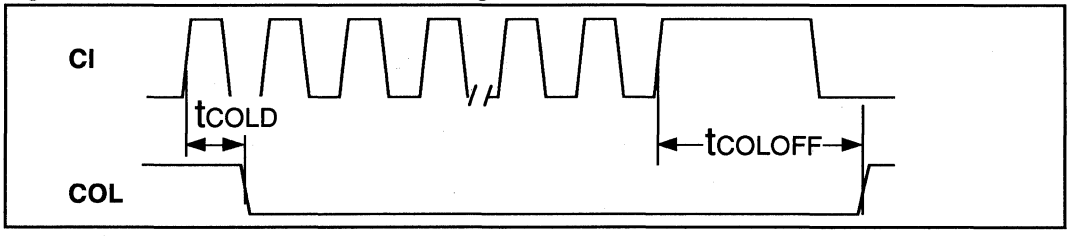
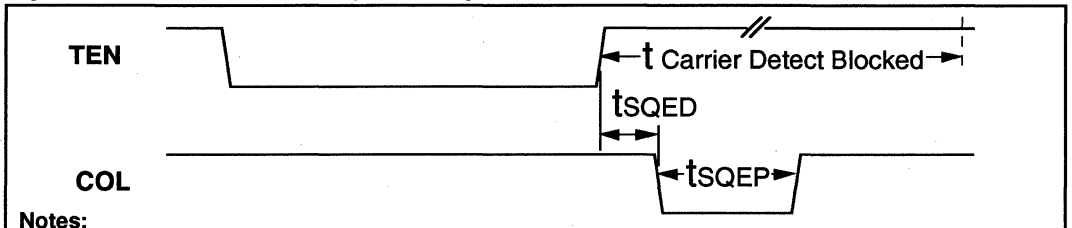
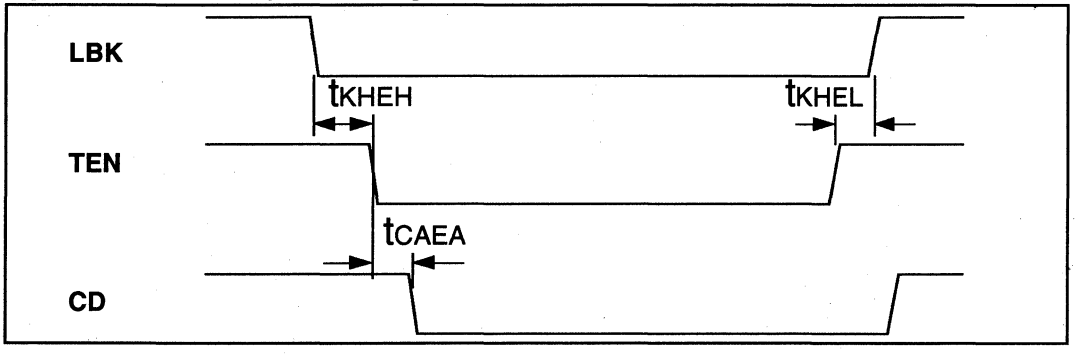


Figure 12: Mode 2 COL/CI Output Timing



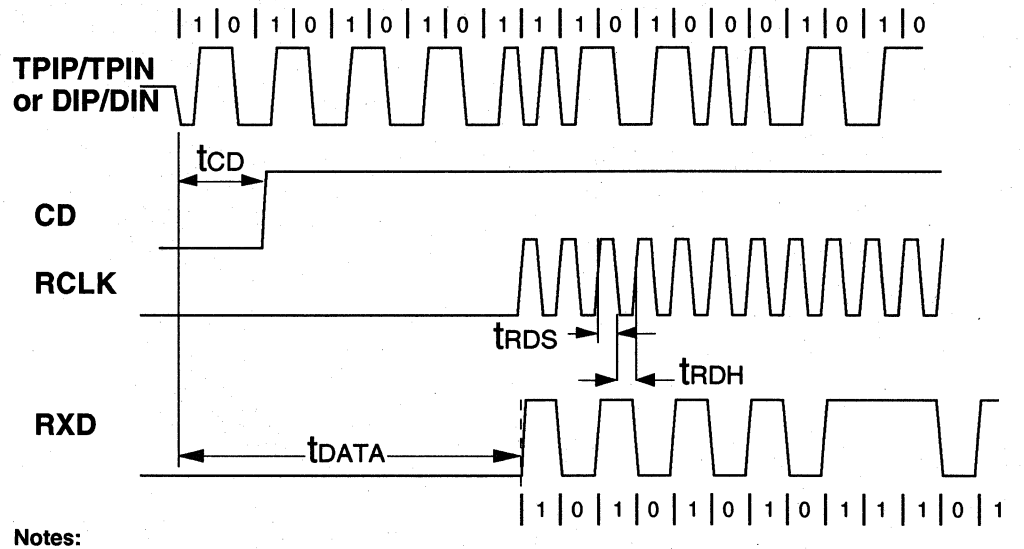
Notes:
1. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

Figure 13: Mode 2 Loopback Timing



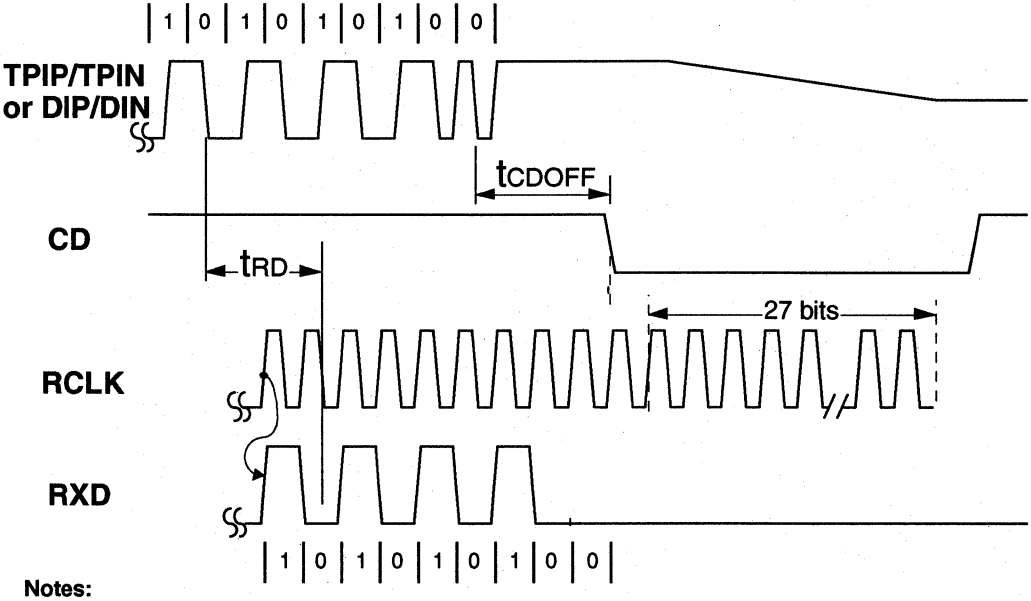
Figures 14 through 19 - Timing Diagrams for Mode 3 (MD1 = 1, MD0 = 0)

Figure 14: Mode 3 RCLK/Start-of-Frame Timing



Notes:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 15: Mode 3 RCLK/End-of-Frame Timing



Notes:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 16: Mode 3 Transmit Timing

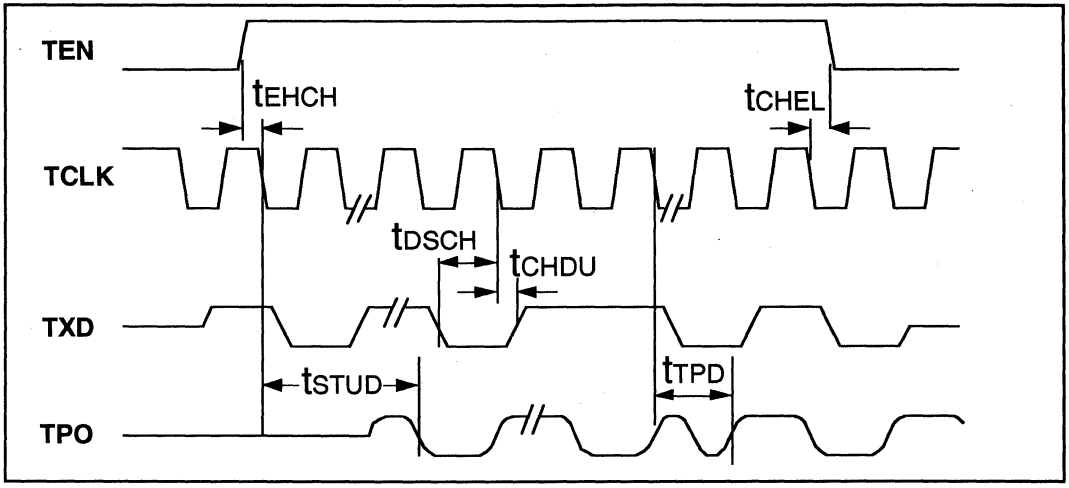


Figure 17: Mode 3 Collision Detect Timing

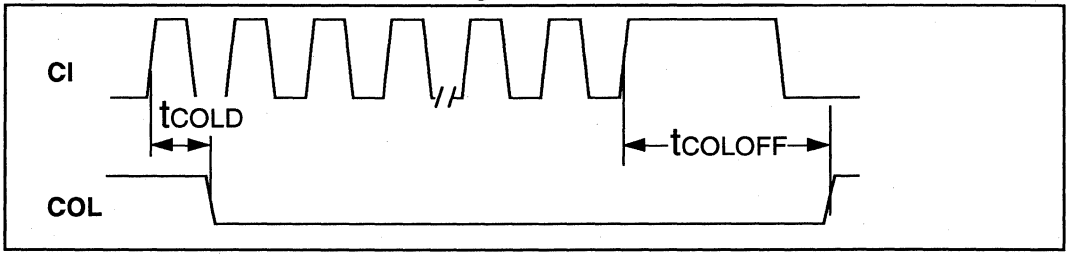


Figure 18: Mode 3 COL/CI Output Timing

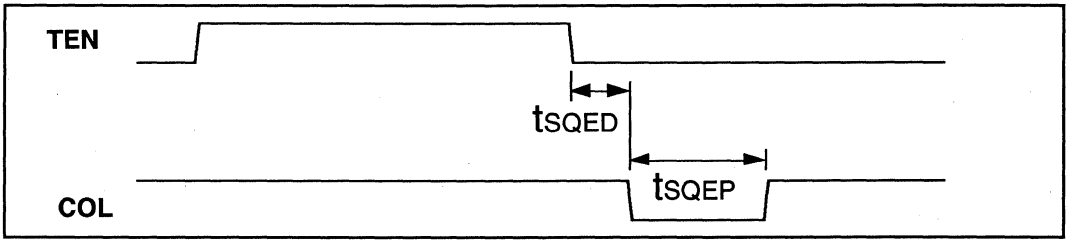
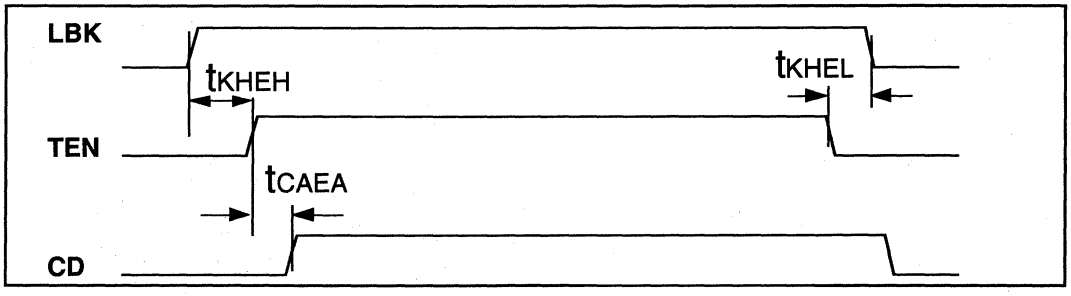
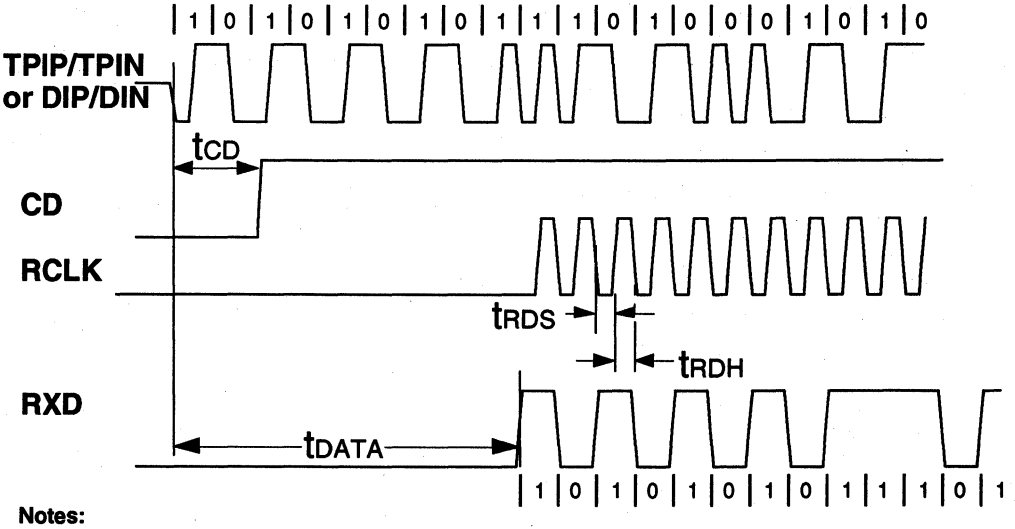


Figure 19: Mode 3 Loopback Timing



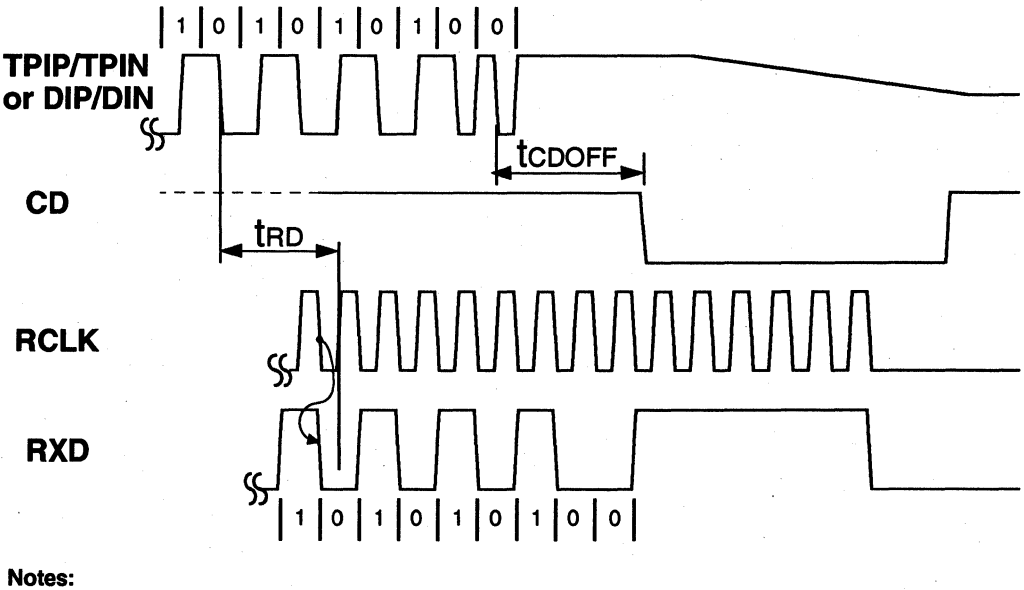
Figures 20 through 25 - Timing Diagrams for Mode 4 (MD1 = 1, MD0 = 1)

Figure 20: Mode 4 RCLK/SoF Timing



Notes:
1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 21: Mode 4 RCLK/EoF Timing



Notes:
1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 22: Mode 4 Transmit Timing

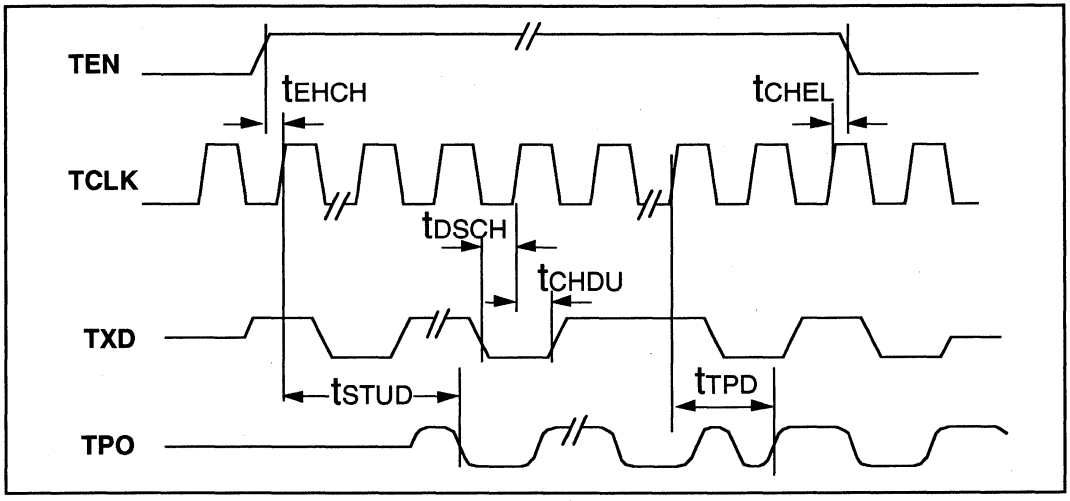


Figure 23: Mode 4 Collision Detect Timing

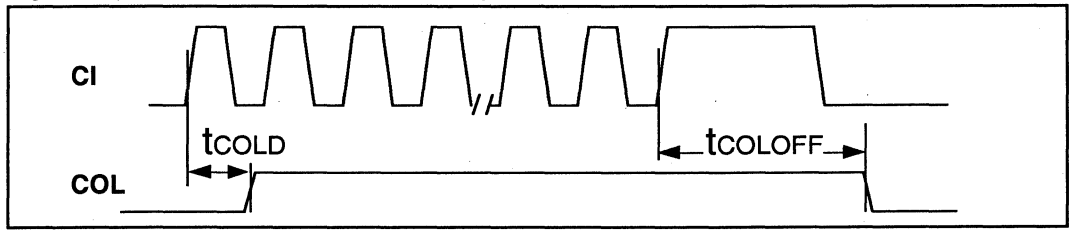


Figure 24: Mode 4 COL/CI Output Timing

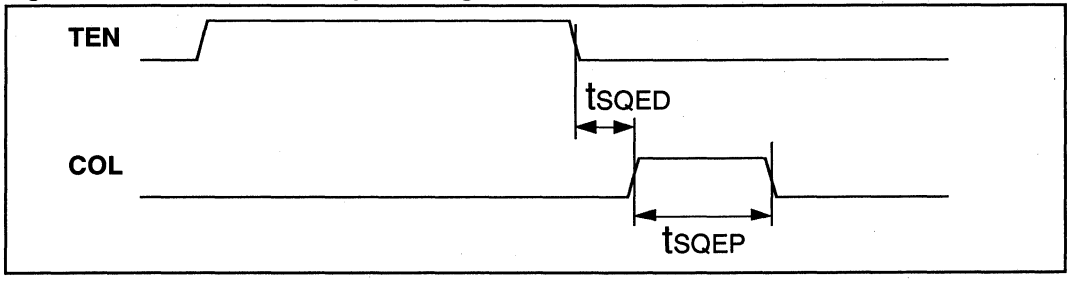


Figure 25: Mode 4 Loopback Timing

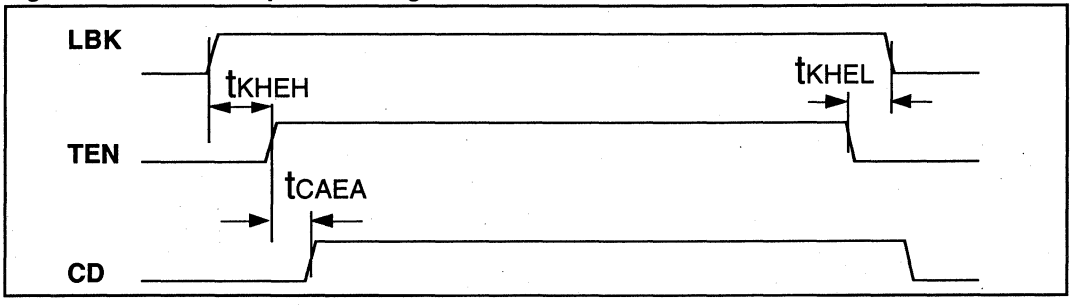


Table 8: RCLK/Start-of-Frame Timing

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Decoder acquisition time	AUI	t_{DATA}	–	900	1100	ns
	TP	t_{DATA}	–	1300	1500	ns
CD turn-on delay	AUI	t_{CD}	–	50	200	ns
	TP	t_{CD}	–	400	550	ns
Receive data setup	Mode 1	t_{RDS}	43	70	–	ns
from RCLK	Modes 2, 3 and 4	t_{RDS}	30	45	–	ns
Receive data hold	Mode 1	t_{RDS}	10	20	–	ns
from RCLK	Modes 2, 3 and 4	t_{RDS}	30	45	–	ns

Table 9: RCLK/End-of-Frame Timing

Parameter	Type	Symbol	Mode 1	Mode 2	Mode 3	Mode 4	Units
RCLK hold after CD off	Minimum	t_{RCH}	5	1	27	5	bt
Rcv data throughput delay	Maximum	t_{RD}	400	375	375	375	ns
CD turn off delay [2]	Maximum	t_{CDOFF}	500	475	475	475	ns
Receive block out after TEN off	Typical [1]	t_{IFG}	5	50	–	–	bt

Table 10: Transmit Timing

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
TEN setup from TCLK	t_{EHCH}	22	–	–	ns
TXD setup from TCLK	t_{DSCH}	22	–	–	ns
TEN hold after TCLK	t_{CHEL}	5	–	–	ns
TXD hold after TCLK	t_{CHDU}	5	–	–	ns
Transmit start-up delay - AUI	t_{STUD}	–	200	450	ns
Transmit start-up delay - TP	t_{STUD}	–	350	450	ns
Transmit through-put delay - AUI	t_{TPD}	–	–	300	ns
Transmit through-put delay - TP	t_{TPD}	–	338	350	ns

Table 11: Collision Detection, COL/CI Output and Loopback Timing

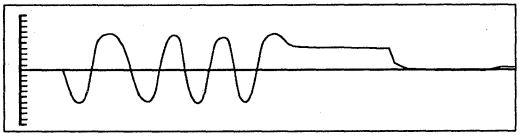
Parameter	Symbol	Minimum	Typical [1]	Maximum	Units
COL turn on delay	t_{COLD}	–	–	500	ns
COL turn off delay	t_{COLOFF}	–	–	500	ns
COL (SQE) Delay after TEN off	t_{SQED}	0.65	–	1.6	µs
COL (SQE) Pulse Duration	t_{SQEP}	500	–	1500	ns
LBK setup from TEN	t_{KHEH}	10	25	–	ns
LBK hold after TEN	t_{KHEL}	10	0	–	ns

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] CD Turnoff delay measured from middle of last bit, so timing specification is unaffected by the value of the last bit.

Transmit Function

The LXT901 receives NRZ data from the controller at the TXD input as shown in Figure 1, and passes it through a Manchester encoder. The encoded data is then transferred to either the AUI cable (the DO circuit) or the twisted-pair network (the TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP, shown in Figure 26. The TPO output is pre-distorted and prefiltered to meet the 10 Base-T jitter template. **An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. No external filters are required.** During idle periods, the LXT901 transmits link integrity test pulses on the TPO circuit (if LI is enabled and integrated PLS/ MAU mode is selected). The UTP pin controls LXT901 termination impedance.

Figure 26: LXT901 TPO Output Waveform



When UTP = 0, the LXT901 is set for shielded TP (150 Ω). When UTP = 1, the LXT901 is set for unshielded TP (100 Ω).

Jabber Control Function

Figure 27 is a state diagram of the LXT901 Jabber control function. The LXT901 on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions, and activates the JAB pin. Once the LXT901 is in the jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it will exit the jabber state.

SQE Function

In the integrated PLS/MAU mode, the LXT901 supports the signal quality error (SQE) function as shown in Figure 28. After every successful transmission on the 10Base-T network, the 901 transmits the SQE signal for 10BT±5BT over the internal CI circuit which is indicated on the COL pin of the device. When using the 10Base 2 port of the 901, the SQE function is determined by the external MAU attached.

Figure 27: Jabber Control Function

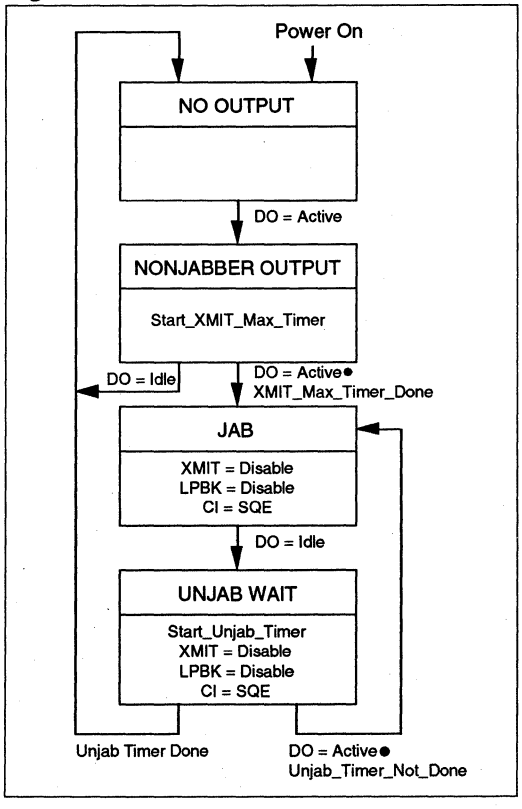
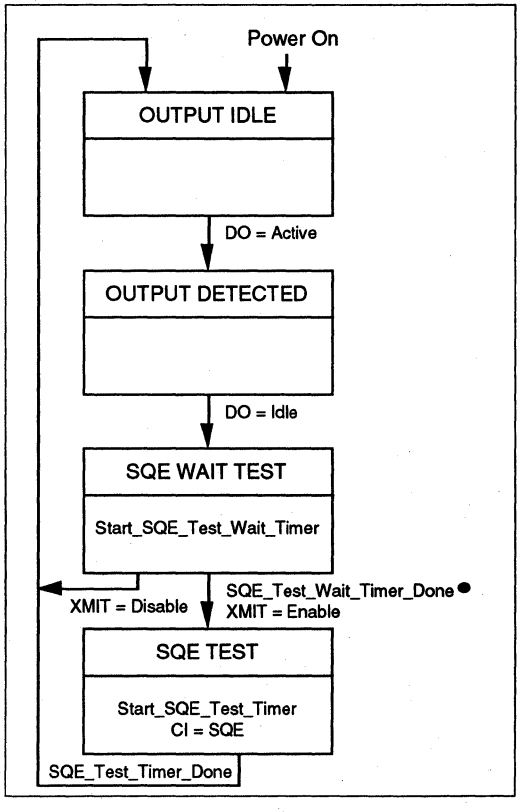


Figure 28: SQE Function



Receive Function

The LXT901 receive function acquires timing and data from the twisted-pair network (the TPI circuit) or from the AUI (the DI circuit). Valid received signals are passed through the on-chip filters and Manchester decoder then output as decoded NRZ data and receive timing on the RXD and RCLK pins, respectively.

An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. **No external filters are required.** The receive function is activated only by valid data streams above the squelch level and with proper timing. If the differential signal at the TPI or the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT901 receive function enters the idle state. If the polarity of the TPI circuit is reversed, LXT901 detects the polarity reverse and reports it via the PLR output. The LXT901 automatically corrects reversed polarity.

Polarity Reverse Function

The LXT901 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever polarity is reversed, these two counters are reset to zero. If the LXT901 enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity Testing is disabled, polarity detection is based only on received data.). Polarity correction is always enabled.

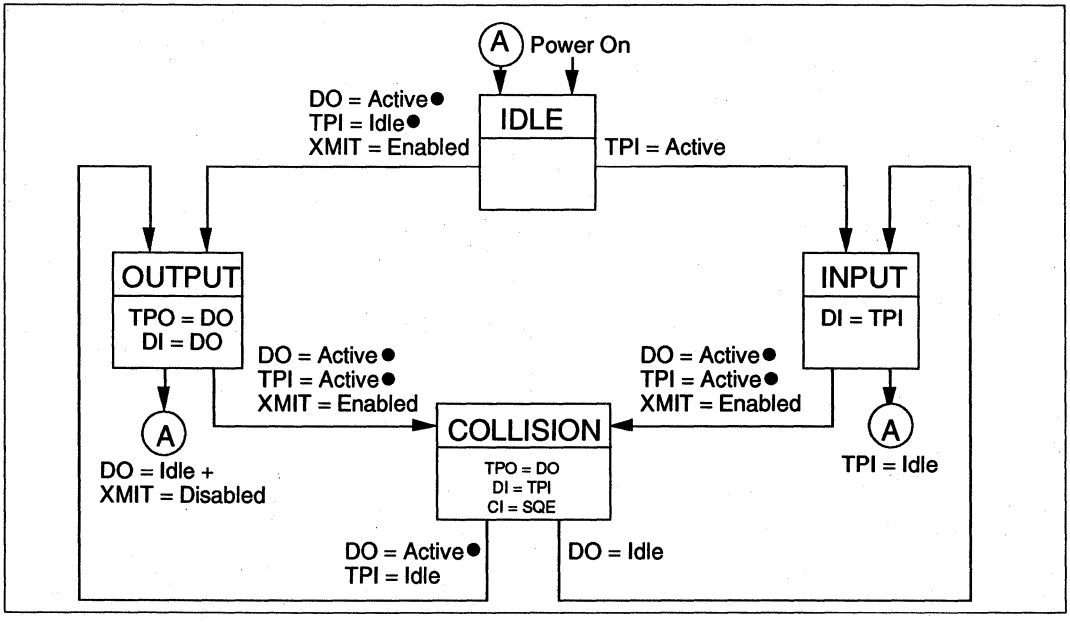
Collision Detection Function

The collision detection function operates on the twisted pair side of the interface. For standard (half-duplex) 10Base-T operation, a collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT901 reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 29 is a state diagram of the LXT901 collision detection function. Refer to Table 11 for collision detection and COL/CI output timing (NOTE: For full-duplex operation, the collision detection circuitry must be disabled.)

Loopback Function

The LXT901 provides the normal loopback function specified by the 10 Base-T standard for the twisted-pair port. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the LXT901 from the TXD pin through the Manchester encoder/decoder to the RXD pin and returned to the back-end. This "normal" loopback function is disabled when a data collision occurs, clearing the RXD

Figure 29: Collision Detection Function



circuit for the TPI data. Normal loopback is also disabled during link fail and jabber states.

The LXT901 also provides three additional loopback functions. An external loopback mode, useful for system-level testing, is controlled by pin 21 (LEDC). When LEDC is tied low, the LXT901 disables the collision detection and internal loopback circuits, to allow external loopback.

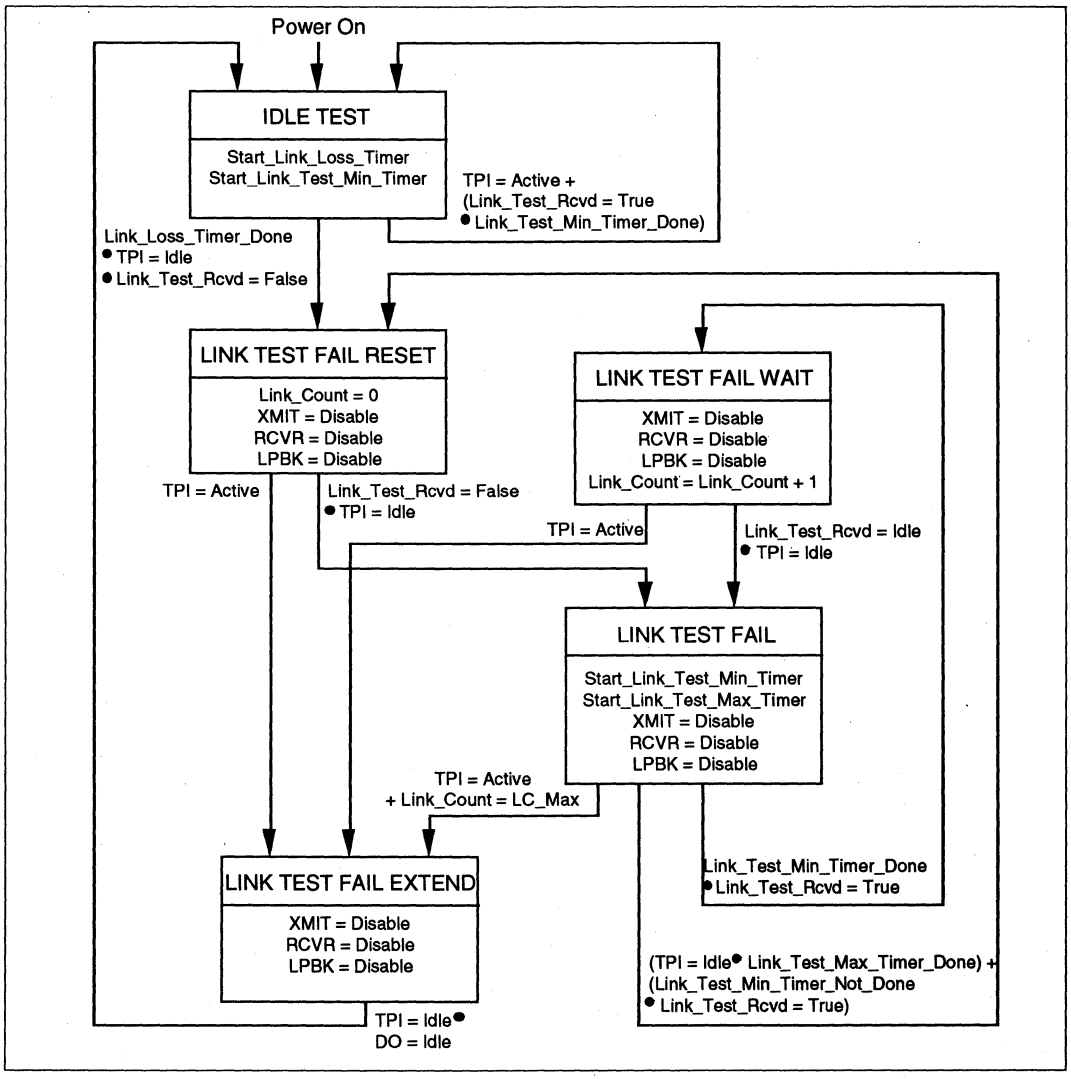
"Forced" TP loopback is controlled by pin 22 (LBK). When the TP port is selected and LBK = 1, TP loopback is "forced", overriding collisions on the TP circuit. When LBK = 0, normal loopback is in effect.

AUI loopback is also controlled by the LBK pin. When the AUI port is selected and LBK = 1, data transmitted by the back-end is internally looped back from the TXD pin through the Manchester encoder/decoder to the RXD pin. When LBK = 0, no AUI loopback occurs.

Link Integrity Test

Figure 30 is a state diagram of the LXT901 Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled when pin 8 (LI) is tied high. When enabled, the receiver recognizes link integrity pulses which

Figure 30: Link Integrity Test Function



are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The LXT901 ignores any link integrity pulse with interval less than 2 - 7 ms. The LXT901 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

Remote Signaling

The LXT901 transmits standard link pulses which meet the 10BaseT specification. However, the 901 encodes additional status information into the link pulse by varying the link pulse timing. This is referred to as remote signaling. Using alternate pulse intervals, the LXT901 can signal three local conditions: link down, jabber, and remote signaling compatibility. Figure 31 shows the interval variations used to signal local status to the other end of the line. The LXT901 also recognizes these alternate pulse intervals when received from a remote unit. Remote status conditions are reported to the controller over the RLD, RJAB and RCMPT output pins.

Applications

Figures 32 through 38 show typical LXT901 applications.

Auto Port Select with External Loopback Control (Figure 32)

Figure 32 is a typical LXT901 application. The diagram is arranged to group similar pins together; it does not represent the actual LXT901 pinout. The controller interface pins (transmit data, clock and enable; receive data and clock; and the collision detect, carrier detect and loopback control pins) are shown at the top left.

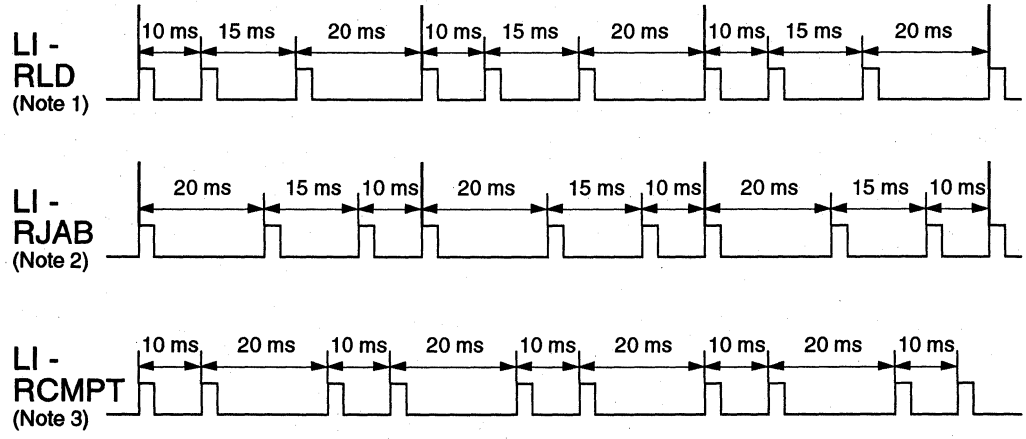
Programmable option pins are grouped center left. The PAUI pin is tied to ground and all other option pins are tied high. This set-up selects the following options:

- Automatic Port Selection (PAUI = 0 and AUTOSEL = 1)
- Normal Receive Threshold (NTH = 1)
- Mode 4 (compatible with National NS8390 controllers) (MD0 = 1, MD1 = 1)
- 100 Ω termination for unshielded TP cable (UTP = 1)
- Link Testing Enabled (LI = 1)

Status outputs are grouped at lower left. Local status outputs drive LED indicators and remote status indicators are available as required.

Power and ground pins are shown at the bottom of the diagram. A single power supply is used for both VCC1 and VCC2 with a decoupling capacitor installed between the power and ground busses.

Figure 31: Remote Signaling Link Integrity Pulse Timing

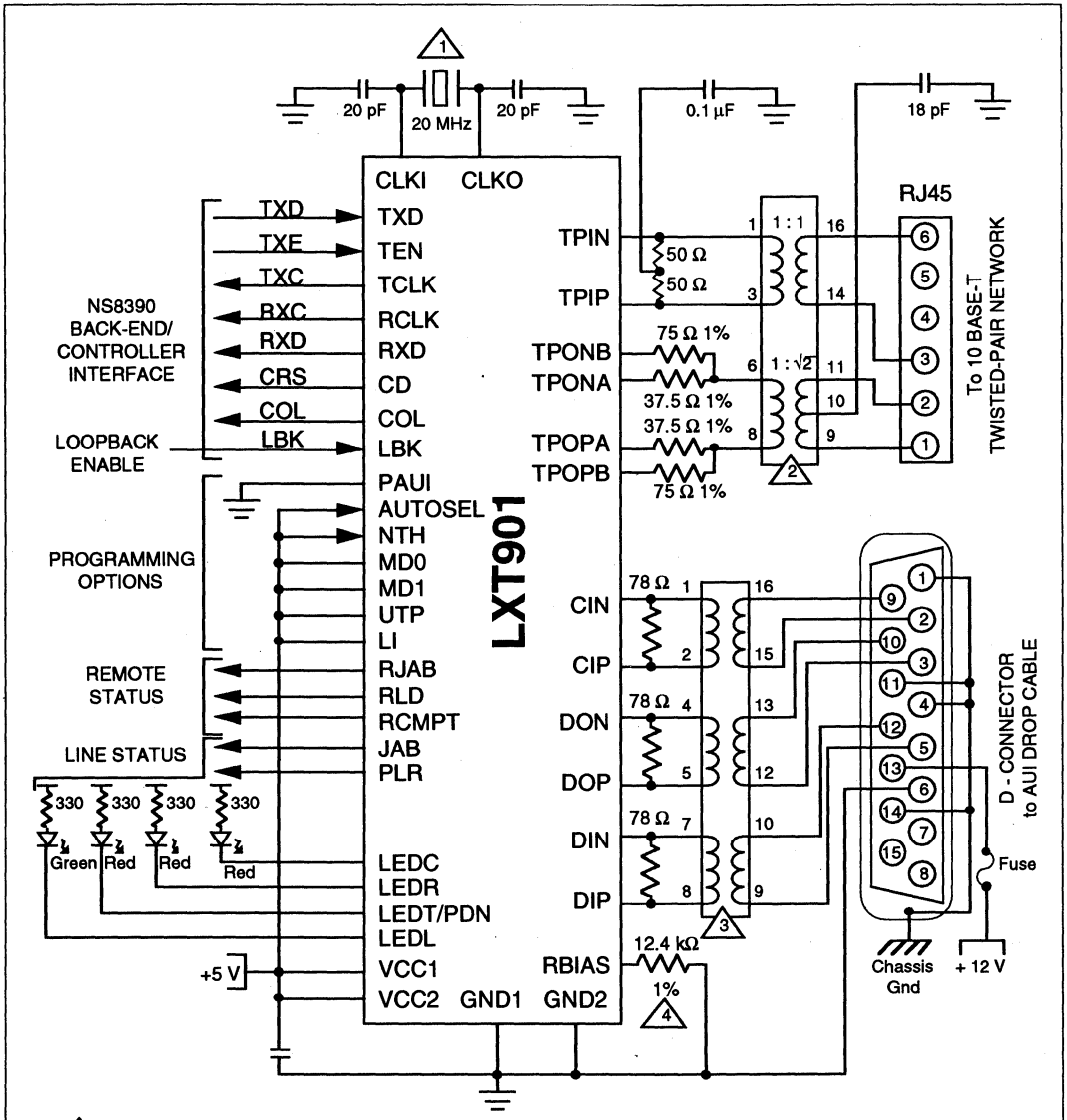


Notes:

1. For Remote Link Down (RLD) signaling, the interval between LI pulses increments from 10 ms to 15 ms to 20 ms, and then the cycle starts over.
2. For Remote Jabber (RJAB) signaling, the interval between LI pulses decrements from 20 ms to 15 ms to 10 ms, and then the cycle starts over.
3. For Remote Compatibility (RCMPT) signaling, the interval between LI pulses continually switches between 10 ms and 20 ms.

The TP and AUI interfaces are shown at upper and lower right, respectively. Impedance matching resistors are installed in each I/O pair but no external filters are required. Suitable transformers are listed in notes 2 and 3.

Figure 32: LAN Adapter Board Application - Auto Port Select with External LPBK Control

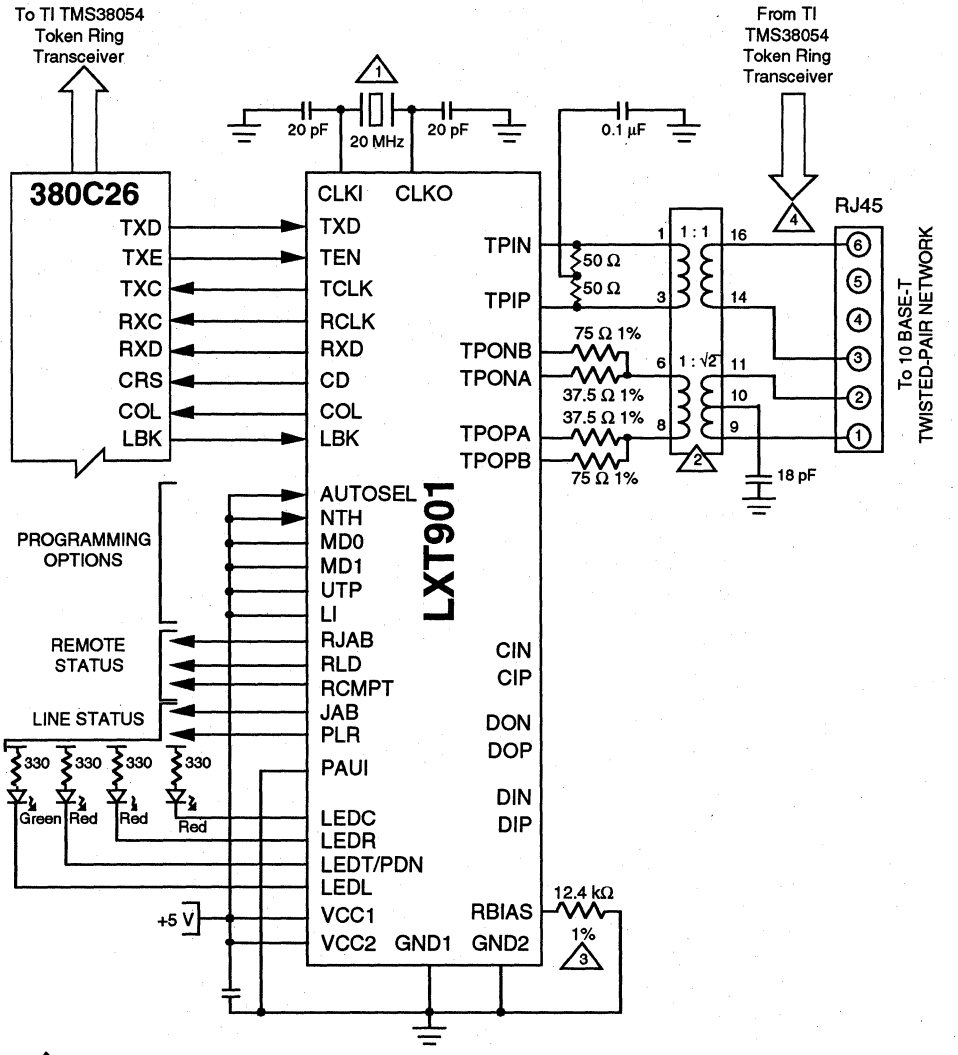


1. Suitable crystals include the MTRON MP-1 and MP-2.
2. Suitable TP transformers include the Fil-Mag 23Z128, and SM23Z128; Valor PT4069 and ST7011; Pulse Engineering PE65994 and PE65745; Belfuse S553-0716 and A553-0716; and Halo Electronics TD42-2006Q and TG42-2006WH1.
3. Suitable AUI transformers include the Fil-Mag 23Z90 and SM23Z90; Valor LT6030 and ST7030; Pulse Engineering PE64502; and Halo Electronics TD01-0756K and TG01-0756W.
4. Bias resistor RBIAS should be located close to the pin and isolated from other signals.

Dual Network Support - 10Base T and Token Ring (Figure 33)

Figure 33 shows the LXT901 with a Texas Instruments 380C26 CommProcessor. The 380C26 is compatible with Mode 4 (MD0 and MD1 both high). When used with the 380C26, both the LXT901 and a TMS38054 Token Ring transceiver can be tied to a single RJ45 allowing dual network support from a single connector. The LXT901 AUI port is not used.

Figure 33: LXT901/380C26 Interface for Dual Network Support of 10Base T and Token Ring

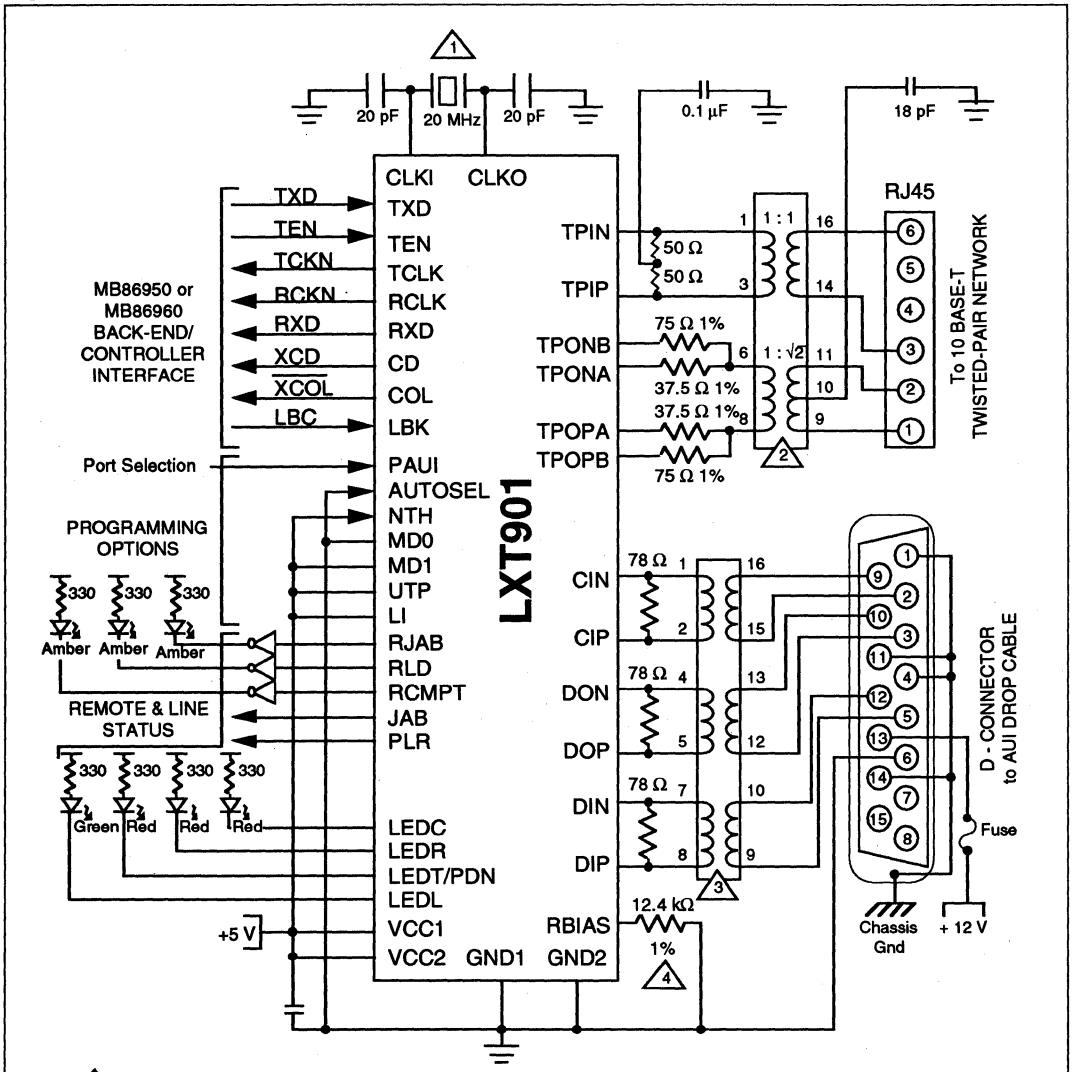


1. Suitable crystals include the MTRON MP-1 and MP-2.
2. Suitable TP transformers include the Fil-Mag 23Z128, and SM23Z128; Valor PT4069 and ST7011; Pulse Engineering PE65994 and PE65745; Belfuse S553-0716 and A553-0716; and HALO Electronics TD42-2006Q and TG42-2006WH1.
3. Bias resistor RBIAS should be located close to the pin and isolated from other signals.
4. Additional magnetics and switching logic (not shown) is required to implement the dual network solution.

Manual Port Select with Link Test Function (Figures 34 and 35)

With MD0 low and MD1 tied high, the LXT901 logic and framing are set to Mode 3 (compatible with Fujitsu MB86950 and MB86960, and Seeq 8005 controllers). Figure 34 shows the setup for Fujitsu controllers. Figure 35 shows the four inverters required to interface with the Seeq 8005 controller. As in Figure 32, both these Mode 3 applications show the LI pin tied high, enabling Link

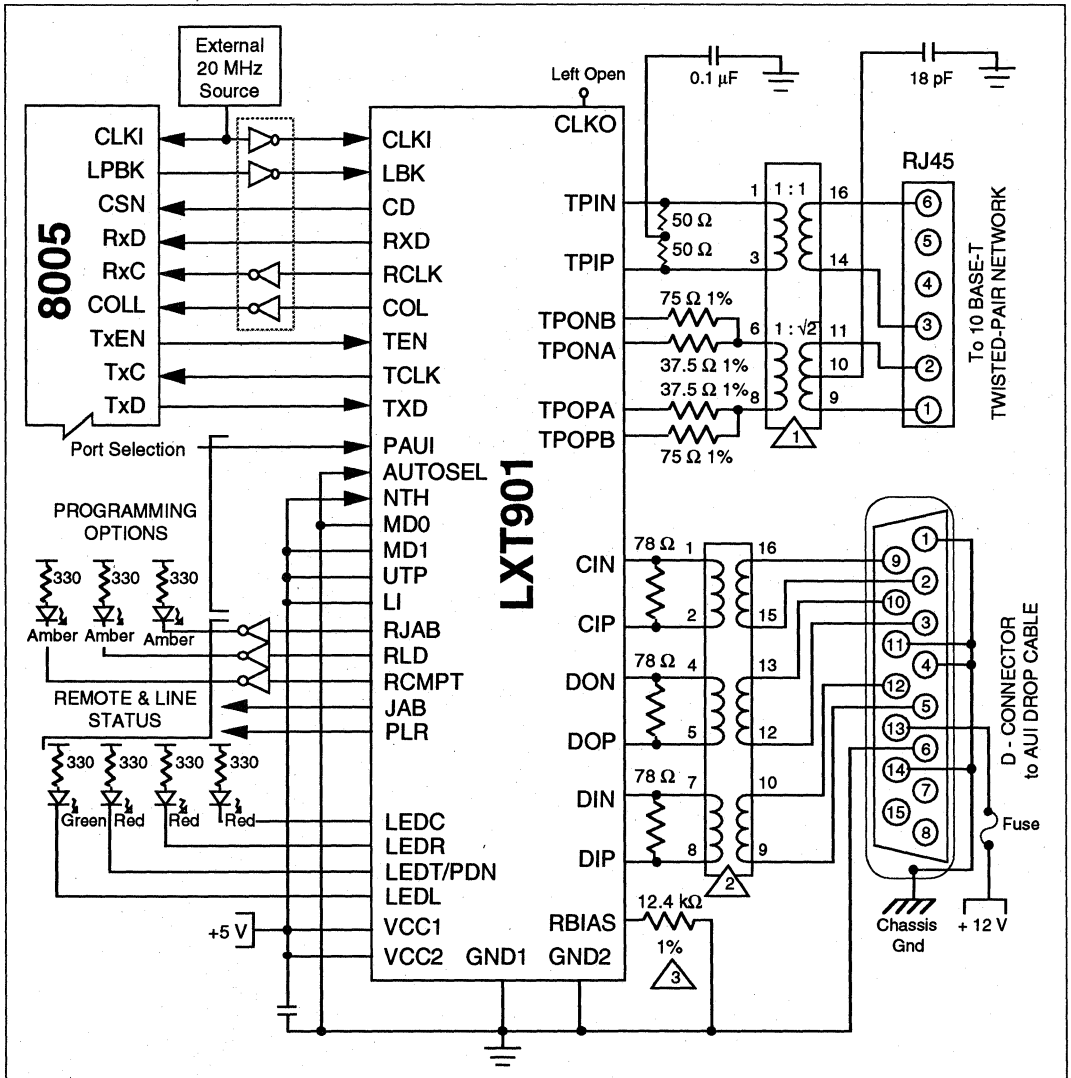
Figure 34: LAN Adapter Board Application - Manual Port Select with Link Test Function



1. Suitable crystals include the MTRON MP-1 and MP-2.
2. Suitable TP transformers include the Fil-Mag 23Z128, and SM23Z128; Valor PT4069 and ST7011; Pulse Engineering PE65994 and PE65745; Belfuse S553-0716 and A553-0716; and Halo Electronics TD42-2006Q and TG42-2006WH1.
3. Suitable AUI transformers include the Fil-Mag 23Z90 and SM23Z90; Valor LT6030 and ST7030; Pulse Engineering PE64502; and Halo Electronics TD01-0756K and TG01-0756W.
4. Bias resistor RBIAS should be located close to the pin and isolated from other signals.

Testing; and the UTP and NTH pins are both tied high, selecting the standard receiver threshold and 100 Ω termination for unshielded TP cable. However, in these applications AUTOSEL is tied low, allowing external port selection through the PAUI pin. The remote status outputs are inverted to drive LED indicators.

Figure 35: Manual Port Select with Seeq 8005 Controller



1 Suitable TP transformers include the Fil-Mag 23Z128, and SM23Z128; Valor PT4069 and ST7011; Pulse Engineering PE65994 and PE65745; Belfuse S553-0716 and A553-0716; and HALO Electronics TD42-2006Q and TG42-2006WH1.

2 Suitable AUI transformers include the Fil-Mag 23Z90 and SM23Z90; Valor LT6030 and ST7030; Pulse Engineering PE64502; and HALO Electronics TD01-756K, and TG01-0756W.

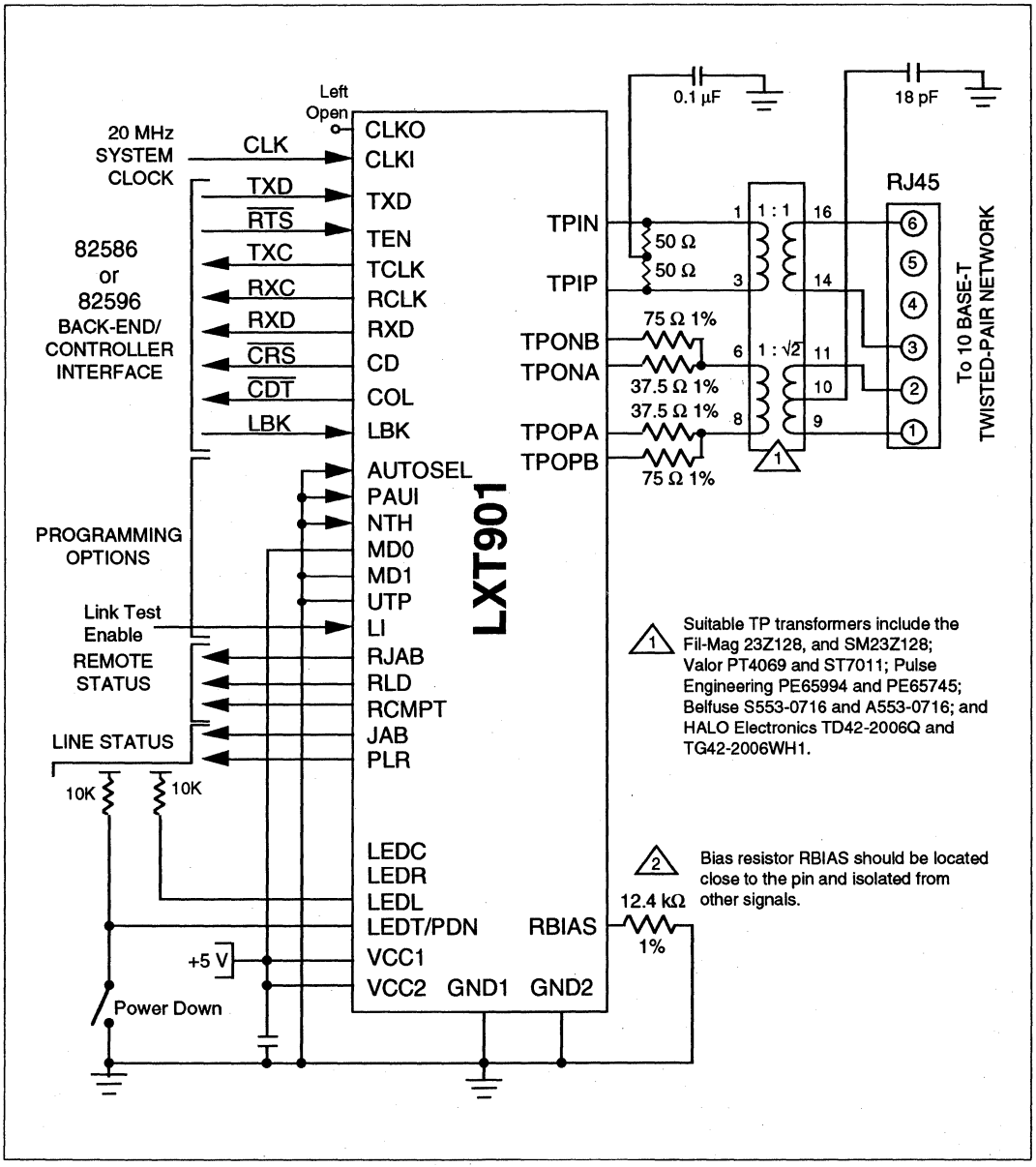
3 Bias resistor RBIAS should be located close to the pin and isolated from other signals.

150 Ω Shielded Twisted-Pair Only (Figure 36)

Figure 36 shows the LXT901 in a typical twisted-pair only application. The DTE is connected to a 10Base-T network through the twisted-pair RJ45 connector. (The AUI port is not used.) With MD0 tied high and MD1 grounded, the LXT901 logic and framing are set to Mode 2 (compatible with Intel 82586 and 82596 controllers).

A 20 MHz system clock input at CLKI is used in place of the crystal oscillator. (CLKO is left open.) The LI pin externally controls the link test function. The UTP and NTH pins are both tied low, selecting the reduced receiver threshold and 150 Ω termination for shielded TP cable. The switch at LEDT/PDN manually controls the power down mode.

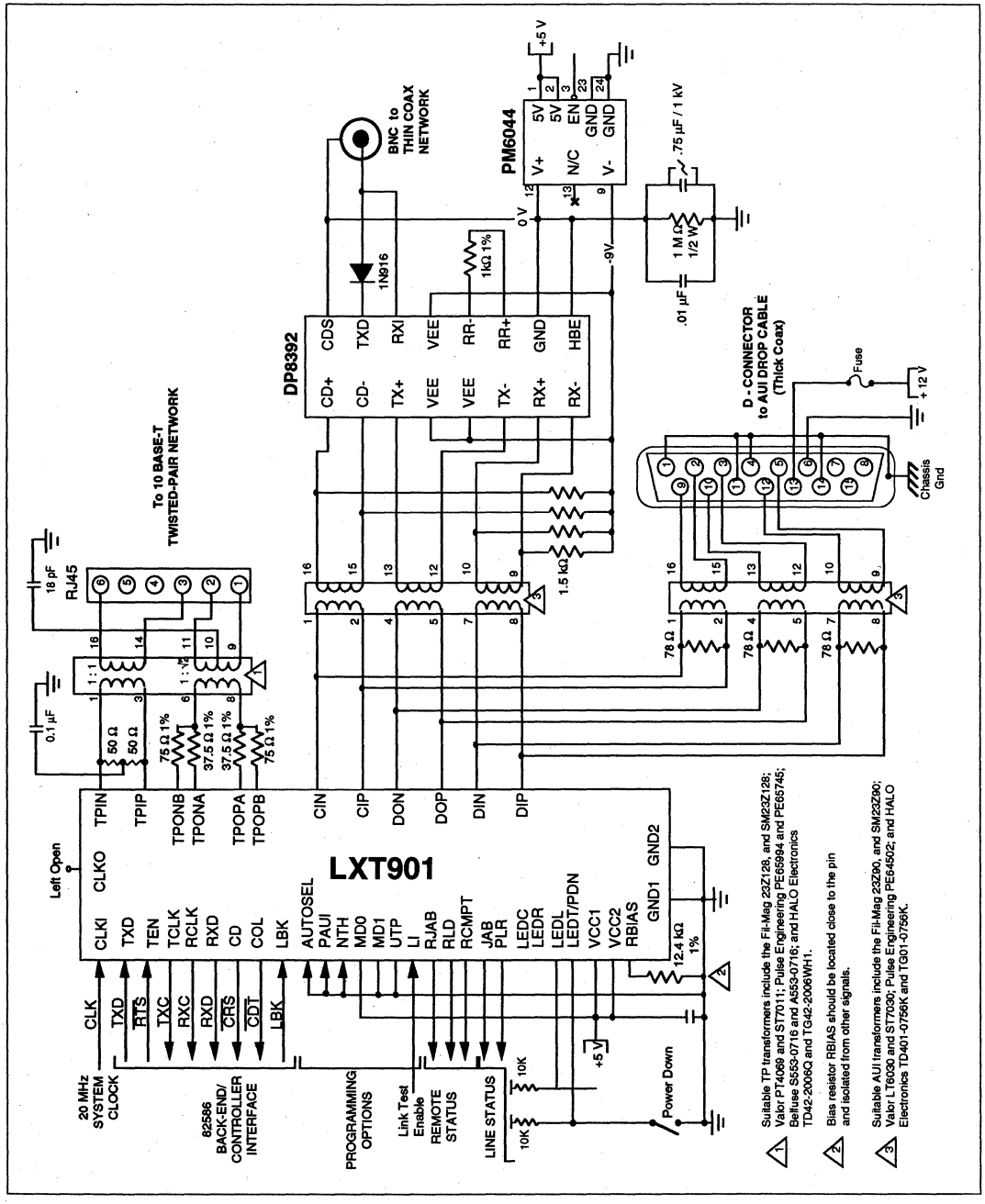
Figure 36: 150 Ω Shielded Twisted-Pair Only Application



Three Media Application (Figure 37)

Like Figure 36, Figure 37 shows the LXT901 in Mode 2 (compatible with Intel 82586/686 controllers) with the same options and twisted-pair interface. However, Figure 37 adds a pair of connections to the AUI port which was not used in Figure 36. Two transformers are used to couple the AUI port to either a D-connector or a BNC connector. (A DP8392 coax transceiver with PM6044 power supply are required to drive the thin coax network through the BNC.)

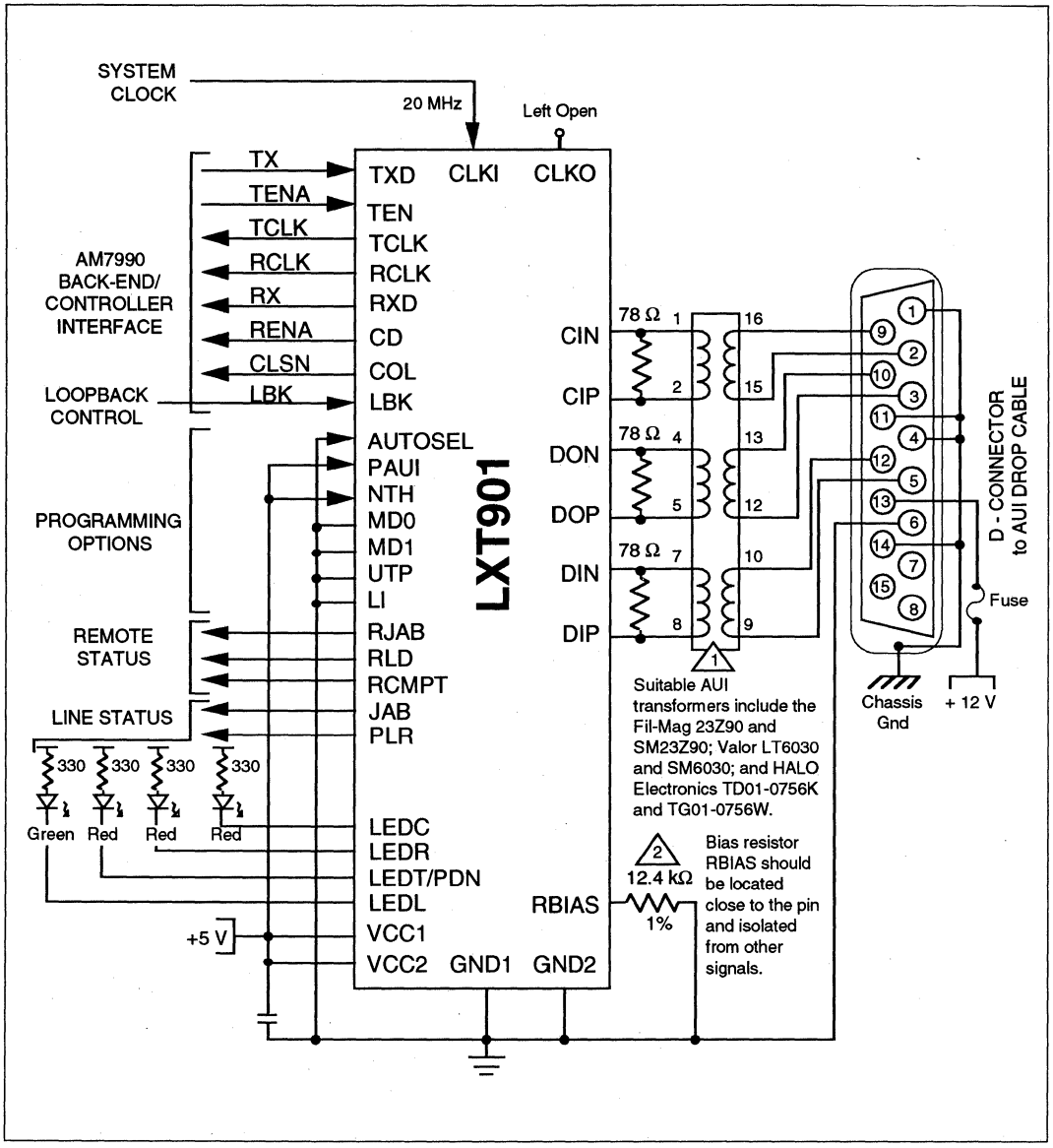
Figure 37: Three Media Application



AUI Encoder/Decoder Only (Figure 38)

In this application the DTE is connected to a coaxial network through the AUI. AUTOSEL is tied low and PAUI is tied high, manually selecting the AUI port. The twisted-pair port is not used. With MD1 and MD0 both low, the LXT901 logic and framing are set to Mode 1 (compatible with AMD AM7990 controllers). The LI pin is tied low, disabling the link test function. The LBK input controls loopback. A 20 MHz system clock is supplied at CLKI with CLKO left open.

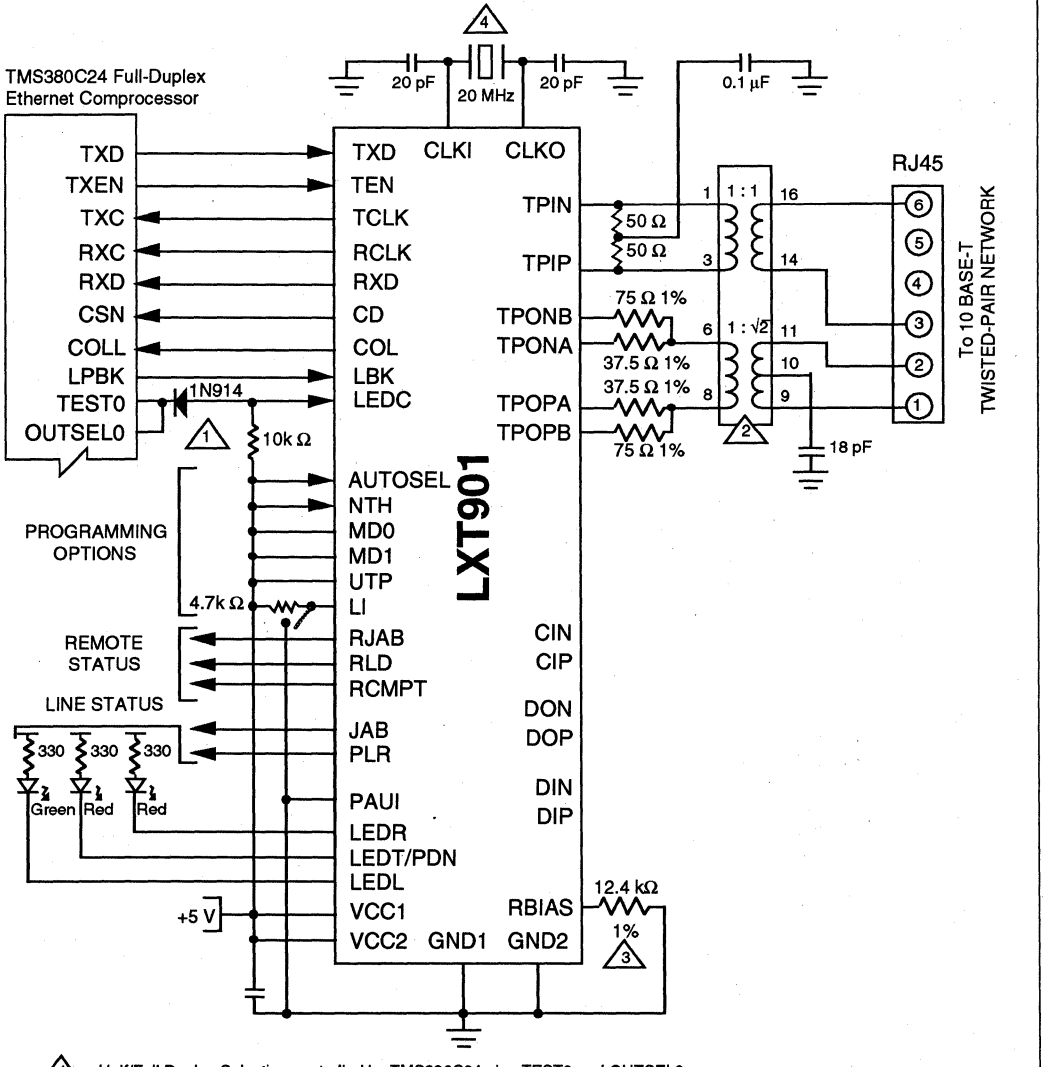
Figure 38: AUI Encoder/Decoder Only Application



Full Duplex Support (Figure 39)

Figure 39 shows the LXT901 with a Texas Instruments 380C24 CommProcessor. The 380C24 is compatible with Mode 4 (MD0 and MD1 both high). When used with the 380C24 or other full duplex-capable controller, the LXT901 supports full-duplex Ethernet, effectively doubling the available bandwidth of the network. In this application the LXT901 AUI port is not used.

Figure 39: Full-Duplex Application - Auto Port Select with External LPBK Control



1. Half/Full Duplex Selection controlled by TMS380C24 pins TEST0 and OUTSEL0.
2. Suitable TP transformers include the Fil-Mag 23Z128, and SM23Z128; Valor PT4069 and ST7011; Pulse Engineering PE65994 and PE65745; Belfuse S553-0716 and A553-0716; and HALO Electronics TD42-2006Q and TG42-2006WH1.
3. Bias resistor RBIAS should be located close to the pin and isolated from other signals.
4. Suitable crystals include the MTRON MP-1 and MP-2.

LXT902

Ethernet Twisted-Pair Media Attachment Unit

General Description

The LXT902 twisted-pair Media Attachment Unit (TP-MAU) is designed to allow Ethernet connections to use the existing twisted-pair wiring plant through an Ethernet Attachment Unit Interface (AUI). The LXT902 provides the electrical interface between the AUI and the twisted-pair wire.

LXT902 functions include level-shifted data pass-through from one transmission media to another, collision detection, Signal Quality Error (SQE) testing and automatic correction of polarity reversal on the twisted pair input. It also includes LED drivers for transmit, receive, jabber, collision, reversed polarity detect and link functions.

The LXT902 is an advanced CMOS device and requires only a single 5-volt power supply.

Applications

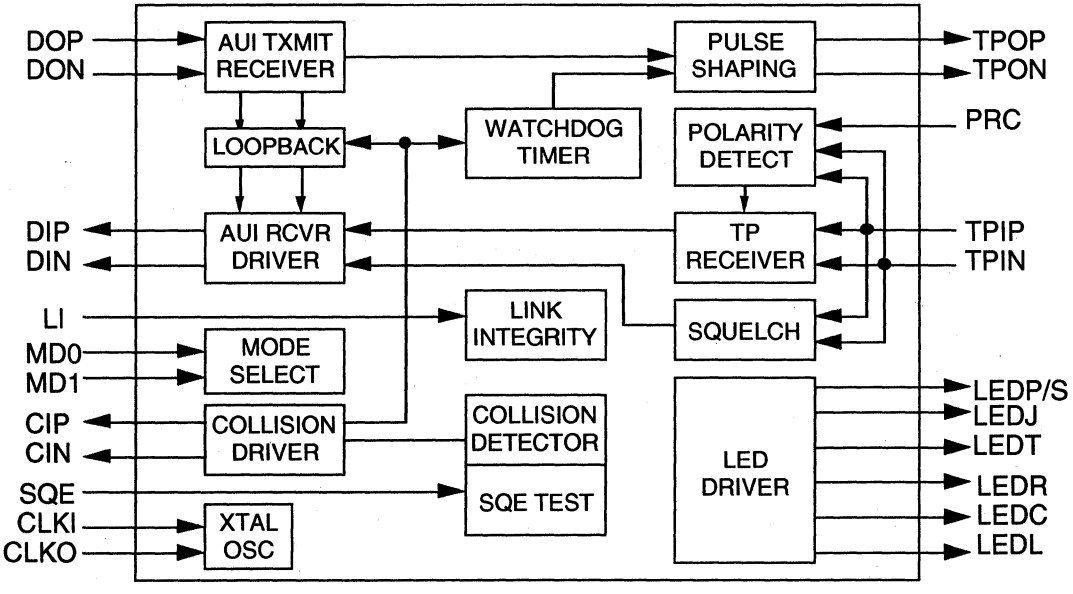
- Computer/workstation interface boards
- LAN repeater
- External 10Base-T converter

Features

- Meets or exceeds IEEE 802.3 standards for AUI and 10Base-T interface
- Direct interface to AUI and RJ45 connectors
- Automatic AUI/RJ45 selection
- Internal predistortion generation
- Internal common mode voltage generation
- Jabber function
- Selectable link test, SQE test disable
- Twisted-pair receive polarity reverse detection and selectable polarity correction
- LED driver for transmit, receive, jabber, collision, link and reversed polarity indicators or for flashing status indicator
- Single 5 V supply, CMOS technology
- Available in 28-pin DIP or PLCC

3

Figure 1: Block Diagram



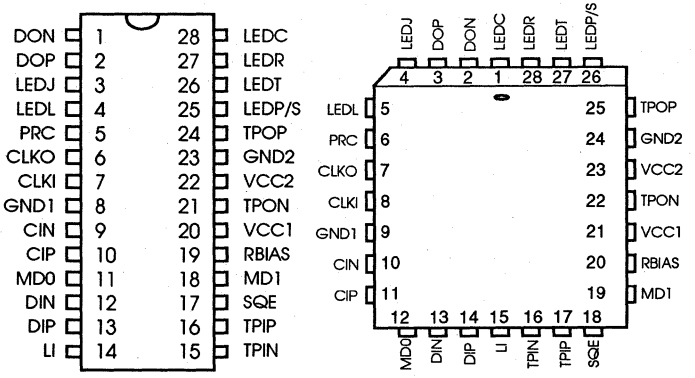


Table 1: Mode Select Options

MD1	MD0	Mode
0	0	10Base-T compliant MAU
0	1	Reduced squelch level
1	0	Half current AUI driver
1	1	DO, DI & CI ports disabled
1	Clock	Test Mode, Jabber on
0	Clock	Test mode, Jabber Disabled

Table 2: Pin Descriptions

Pin # DIP	Pin # PLCC	Sym	I/O	Name	Description
1 2	2 3	DON DOP	I I	Data Out Negative Data Out Positive	Differential input pair connected to the AUI transceiver DO circuit.
3	4	LEDJ	I/O	Jabber LED Driver	Open drain driver for the Jabber indicator LED. Output goes active[1] when watchdog timer begins jab, and stays active until end of the unjab wait period (491 - 525 ms) . When tied to ground, causes LEDP/S to act as a multi-function blinking status indicator.
4	5	LEDL	O	Link LED Driver	Open drain driver for the Link indicator LED. Output is active except during Link Fail or when Link Integrity Test is disabled.
5	6	PRC	I/O	Polarity Reverse Correction	The LXT902 automatically corrects reversed polarity at TPI when PRC is tied high. In Test mode, this pin is a 10 MHz output.
6 7	7 8	CLKO CLKI	– –	Crystal Oscillator	The LXT902 requires either a 20 MHz crystal (or ceramic resonator) connected across these pins, or a 20 MHz clock applied at CLKI.
8	9	GND1	–	Ground 1	Ground.
9 10	10 11	CIN CIP	O O	Collision Negative Collision Positive	Differential driver output pair tied to the collision presence pair of the Ethernet transceiver AUI cable. The collision presence signal is a 10 MHz square wave. This output is activated when a collision is detected on the network, during self-test by the SQE sequence, or after the watchdog timer has expired to indicate the transmit wire pair has been disabled.
11	12	MD0	I	Mode Select 0	Selects operating modes in conjunction with MD1. See Table 1 above for mode select options.
12 13	13 14	DIN DIP	O O	Data In Negative Data In Positive	Differential driver pair connected to the AUI transceiver DI circuit.
14	15	LI	I	Link Integrity Test Enable	Link integrity testing is enabled when this pin is tied high. With link test enabled, the LXT902 sends the link integrity signal in the absence of transmit traffic. It also recognizes received link test pulses, indicating the receive wire pair is present in the absence of transmit traffic.
15 16	16 17	TPIN TPIP	I I	Twisted Pair Receive Inputs	Differential receive inputs from the twisted pair input filter.

[1] LED drivers pull low when active.

Table 2: Pin Descriptions continued

Pin # DIP	Pin # PLCC	Sym	I/O	Name	Description
17	18	SQE	I/O	Signal Quality Error Test Enable	SQE is enabled when this pin is tied high. When enabled, the LXT902 sends the signal quality error test sequence to the CI of the AUI cable after every successful transmission to the media. In Test mode, SQE becomes a 20 MHz output.
18	19	MD1	I	Mode Select 1	Selects operating modes in conjunction with MD0. (See Table 1.) MD1 clock input between 2.0 and 2.5 MHz enables Test mode.
19	20	RBIAS	–	Resistor Bias Control	Bias control pin for the operating circuit. Bias set from external resistor to ground. External resistor value = 12.4 kΩ (± 1%).
20	21	VCC1	I	Power Supply 1	+5 V power supply.
21 24	22 25	TPON TPOP	O O	Twisted Pair Transmit Outputs	Transmit drivers to the twisted-pair output filter. The output is Manchester encoded and pre-distorted to meet the 10Base-T template.
22	23	VCC2	I	Power Supply 2	+5 V power supply.
23	24	GND 2	–	Ground 2	Ground.
25	26	LEDP/S	O	Polarity/Status LED Driver	Open drain LED driver. In normal mode, LEDP/S is active when reversed polarity is detected. If LEDJ is tied to ground, the output LEDP/S indicates multiple status conditions as shown in Figure 2. On solid = Normal, 1 Blink = Link Down, 2 Blinks = Jabber, 5 Blinks = Polarity Reversed.
26	27	LEDT	O	Transmit LED Driver	Open drain driver for the Transmit indicator LED. Output is active during transmit.
27	28	LEDR	O	Receive LED Driver	Open drain driver for the Receive indicator LED. Output is active during receive.
28	1	LEDC	O	Collision LED Driver	Open drain driver for the Collision indicator LED. Output is active when a collision occurs.

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- Supply Voltage V_{CC} -0.3 V to 6 V
- Operating temperature T_{OP} 0 °C (min) to +70 °C (max)
- Storage temperature T_{ST} -65 °C (min) to +150 °C (max)

Recommended Operating Conditions (Voltages are with respect to ground unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage[1]	V_{CC}	4.75	5.0	5.25	V
Operating temperature	T_{OP}	0	-	70	°C

[1] Maximum voltage differential between VCC1 and VCC2 must not exceed 0.3V.

Switching Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Min	Typ[1]	Max	Units
Jabber Timing				
Maximum transmit time[2]	98.5	–	131	ms
Unjab time[2]	491	–	525	ms
Time from Jabber to CS0 on CIP/CIN [3]	0	–	900	ns
Link Integrity Timing				
Time link loss[2]	65	–	66	ms
Time between Link Integrity Pulses[2]	9	–	11	ms
Interval for valid receive Link Integrity Pulses[2]	4.1	–	65	ms
Collision Timing				
Simultaneous TPI/TPO to CSO state on CIN/CIP	0	–	900	ns
DO loopback to TPI on DI [3]	300	–	900	ns
CS0 state delay after TPI/DO idle	–	–	900	ns
CS0 high pulse width	40	–	60	ns
CS0 low pulse width	40	–	60	ns
CS0 frequency	–	10	–	MHz
SQE Timing				
SQE signal duration	500	–	1500	ns
Delay after last positive transition of DO	0.6	–	1.6	µs
LED Timing				
LEDC, LEDT, LEDR on time[2]	100	–	–	ms
LEDP/S on time[2] (See Figure 2)	–	164	–	ms
LEDP/S period [2] (See Figure 2)	–	328	–	ms
General				
Receive start-up delay	0	–	500	ns
Transmit start-up delay	0	–	200	ns
Loopback start-up delay	0	–	500	ns

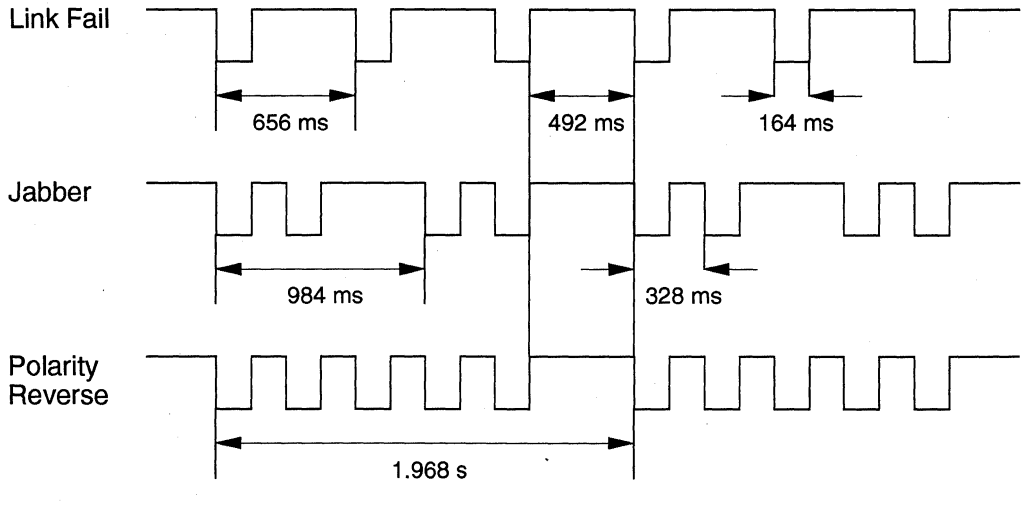
[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Switching times reduced by a factor of 1024 during Test mode.
[3] Parameter is guaranteed by design; not subject to production testing.

I/O Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input low voltage[2]	V_{IL}	–	–	0.8	V	
Input high voltage[2]	V_{IH}	2.0	–	–	V	
Output low voltage (Open drain LED Driver)	V_{OL}	–	–	0.7	V	Drive current = 10 mA
Supply current ($V_{CC}1 = V_{CC}2 = 5.25$ V)	I_{CC}	–	60	70	mA	Line Idle
		–	125	140	mA	Line Active, transmitting all ones
Input leakage current[3]	I_{LL}	–	±1	±10	µA	Input between VCC and GND
Three state leakage current (high Z)	I_{TS}	–	±1	±10	µA	Output between VCC and GND

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] MD0, MD1, SQE, PRC and LI pins. MD0 clock (test mode) must be CMOS level input.
[3] Not including TPIN, TPIP, DOP or DON.

Figure 2: LEDP/S Status Indication Timing



NOTE: LEDP/S status indications are shown in order of priority, i.e., Link Fail indication supersedes Jabber indication which supersedes Polarity Reverse (when PRC = 1). Reversed polarity conditions supersede Link Fail conditions when PRC = 0 (Polarity Correction Disabled). At the LEDL indicator, reversed polarity conditions are reported as Link Fail when PRC = 0. This allows the user to distinguish between actual link failure and apparent link failure due to polarity reversal.

AUI Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input low current	I_{IL}	–	–	-700	µA	
Input high current	I_{IH}	–	–	500	µA	
Differential output voltage	V_{OD}	± 550	–	± 1200	mV	
Differential squelch threshold	V_{DS}	–	220	–	mV	
Receive input impedance	R_Z	–	20	–	kΩ	Between DOP and DON

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Transmit Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	Z_{OUT}	–	5	–	Ω	
Peak differential output voltage	V_{OD}	± 4.5	–	± 5.2	V	Load = 200 Ω at TPOP and TPON
Transmit timing jitter addition [2]	–	–	–	± 8	ns	After Tx filter, 0 line length
Transmit timing jitter addition [2]	–	–	–	± 3.5	ns	After Tx filter and line model specified by IEEE 802.3 for 10Base-T

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Parameter is guaranteed by design; not subject to production testing.

Receive Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Receive input impedance	Z_{IN}	–	20	–	kΩ	Between TPIP/TPIN
Differential squelch threshold	V_{DS}	–	420	–	mV	
Reduced squelch threshold	V_{DSR}	–	300	–	mV	
Receive timing jitter [2]	–	–	–	1.5	ns	

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Parameter is guaranteed by design; not subject to production testing.

Functional Description

The LXT902 Media Attachment Unit (MAU) interfaces the Attachment Unit Interface (AUI) to the unshielded twisted pair cables, transferring data in both directions between the two. The AUI side of the interface comprises three circuits: Data Output (DO), Data Input (DI) and Control Interface (CI). The twisted pair network side of the interface comprises two circuits: Twisted Pair Input (TPI) and Twisted Pair Output (TPO). In addition to the five basic circuits, the LXT902 contains an internal crystal oscillator, separate power and ground pins for analog and digital circuits, various logic controls and six LED drivers for status indications.

Functions are defined from the AUI side of the interface. The LXT902 Transmit function refers to data transmitted by the Data Terminal Equipment (DTE) through the AUI and MAU to the twisted pair network. The LXT902 Receive function refers to data received by the DTE through the MAU and AUI from the twisted pair network. In addition to basic transmit and receive functions, the LXT902 performs all required MAU functions defined by the IEEE 802.3 10Base-T specification such as collision detection, link integrity testing, Signal Quality Error (SQE), jabber control and loopback.

Transmit Function

The LXT902 transfers manchester encoded data from the AUI port of the DTE (the DO circuit) to the twisted pair network (the TPO circuit). The output signal on TPON and TPOP is pre-distorted to meet the 10 Base-T jitter template, and filtered to meet FCC requirements. The output waveform (after the transmit filter) is shown in Figure 3. If the differential inputs at the DO circuit fall below 75% of the threshold level for 8 bit times (typical), the LXT902 transmit function will enter the idle state. During idle periods, the LXT902 transmits link integrity test pulses on the TPO circuit.

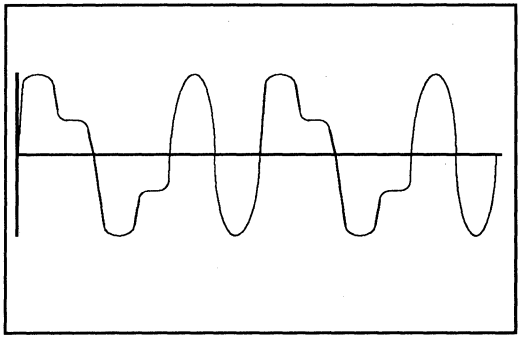
Receive Function

The LXT902 receive function transfers serial data from the twisted pair network (the TPI circuit) to the DTE (over the DI circuit of the AUI). An internal squelch function discriminates noise from link test pulses and valid data streams. Only valid data streams activate the receive function. If the differential inputs at the TPI circuit fall below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT902 receive function will enter the idle state. The TPI threshold can be reduced by approximately 3 dB to allow for longer loops in low-noise environments. The reduced threshold is selected when MD1 = 0 and MD0 = 1.

Polarity Reverse Function

The LXT902 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse with the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever polarity is reversed, these two counters are reset to zero. If the LXT902 enters the link fail

Figure 3: LXT902 TPO Output Waveform



state and no data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity is disabled, polarity detection is based only on received data pulses.)

Collision Detection Function

The collision detection function operates on the twisted pair side of the interface. A collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT902 reports collisions to the AUI by sending a 10 MHz signal over the CI circuit. The collision report signal is output no more than 9 bit times (BT) after the chip detects a collision. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the DTE over the DI circuit, disabling the loopback. Figure 4 is a state diagram of the LXT902 collision detection function (refer to IEEE 802.3 10Base-T specification).

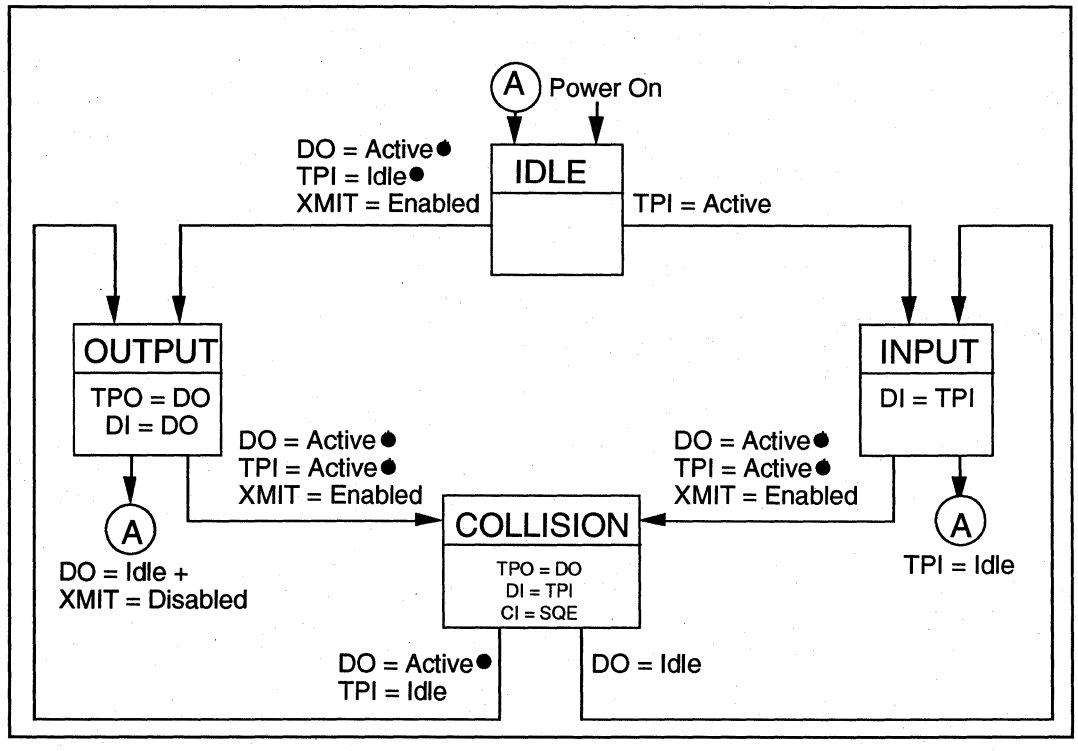
Loopback Function

The LXT902 loopback function operates in conjunction with the transmit function. Data transmitted by the DTE is internally looped back within the LXT902 from the DO pins to the DI pins and returned to the DTE. The loopback function is disabled when a data collision occurs, clearing the DI circuit for the TPI data. Loopback is also disabled during link fail and jabber states.

SQE Test Function

Figure 5 is a state diagram of the SQE Test function. The SQE test function is enabled when the SQE pin is tied high. When enabled, the SQE test sequence is transmitted to the controller after every successful transmission on the 10Base-T network. When a successful transmission is completed, the LXT902 transmits the SQE signal to the AUI over the CI circuit for 10 BT ± 5 BT. The SQE function can be disabled for hub applications by tying the SQE pin to ground.

Figure 4: Collision Detection Function



Jabber Control Function

Figure 6 is a state diagram of the LXT902 Jabber control function. The LXT902 on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the Watchdog timer disables the transmit and loopback functions, and sends the SQE signal to the DTE over the CI circuit. Once the LXT902 is in the jabber state, the DO circuit must remain idle for a period of 491 to 525 ms before it will exit the jabber state.

Link Integrity Test Function

Figure 7 is a state diagram of the LXT902 Link Integrity Test Function. The Link Integrity Test is used to determine the status of the receive side twisted pair cable. The link integrity test is enabled when the LI pin is tied high. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit and loopback functions. The LXT902 ignores any link integrity pulse with interval less than 2 - 7 ms. The LXT902 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

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Figure 5: SQE Test Function

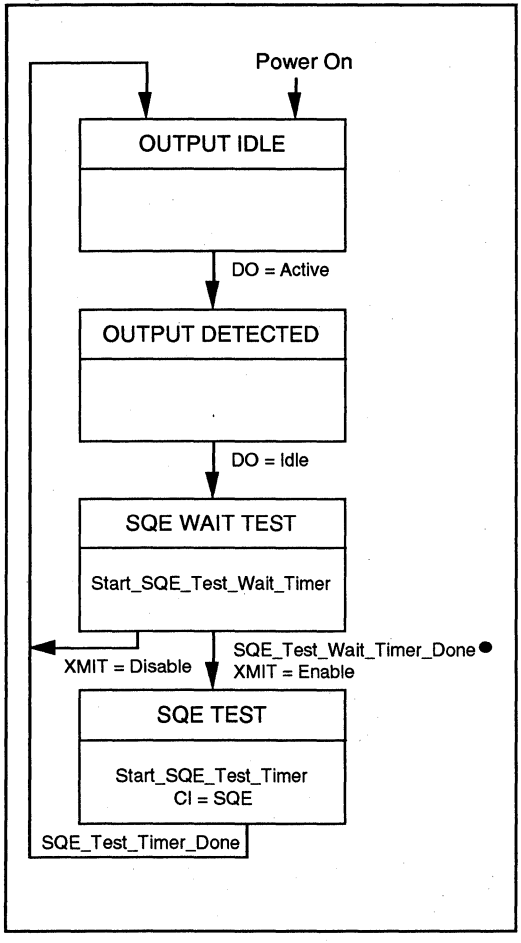
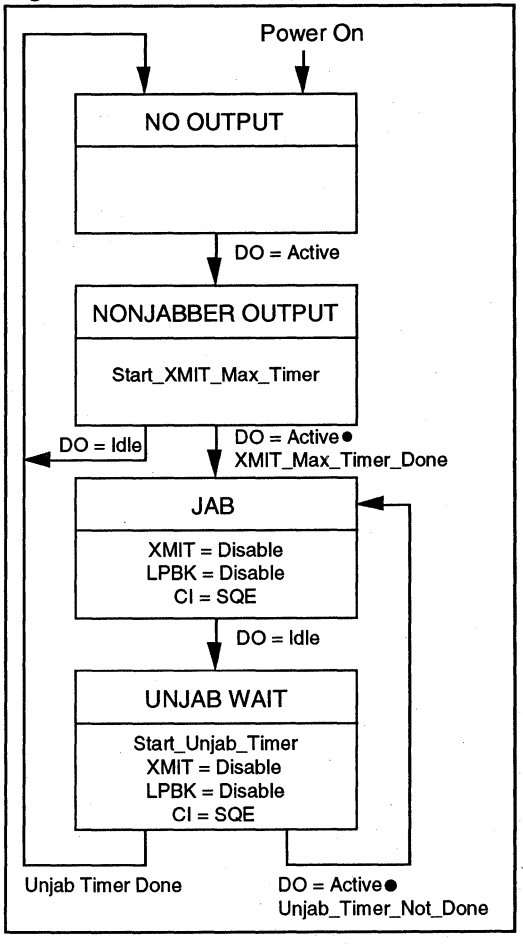


Figure 6: Jabber Control Function



Test Mode

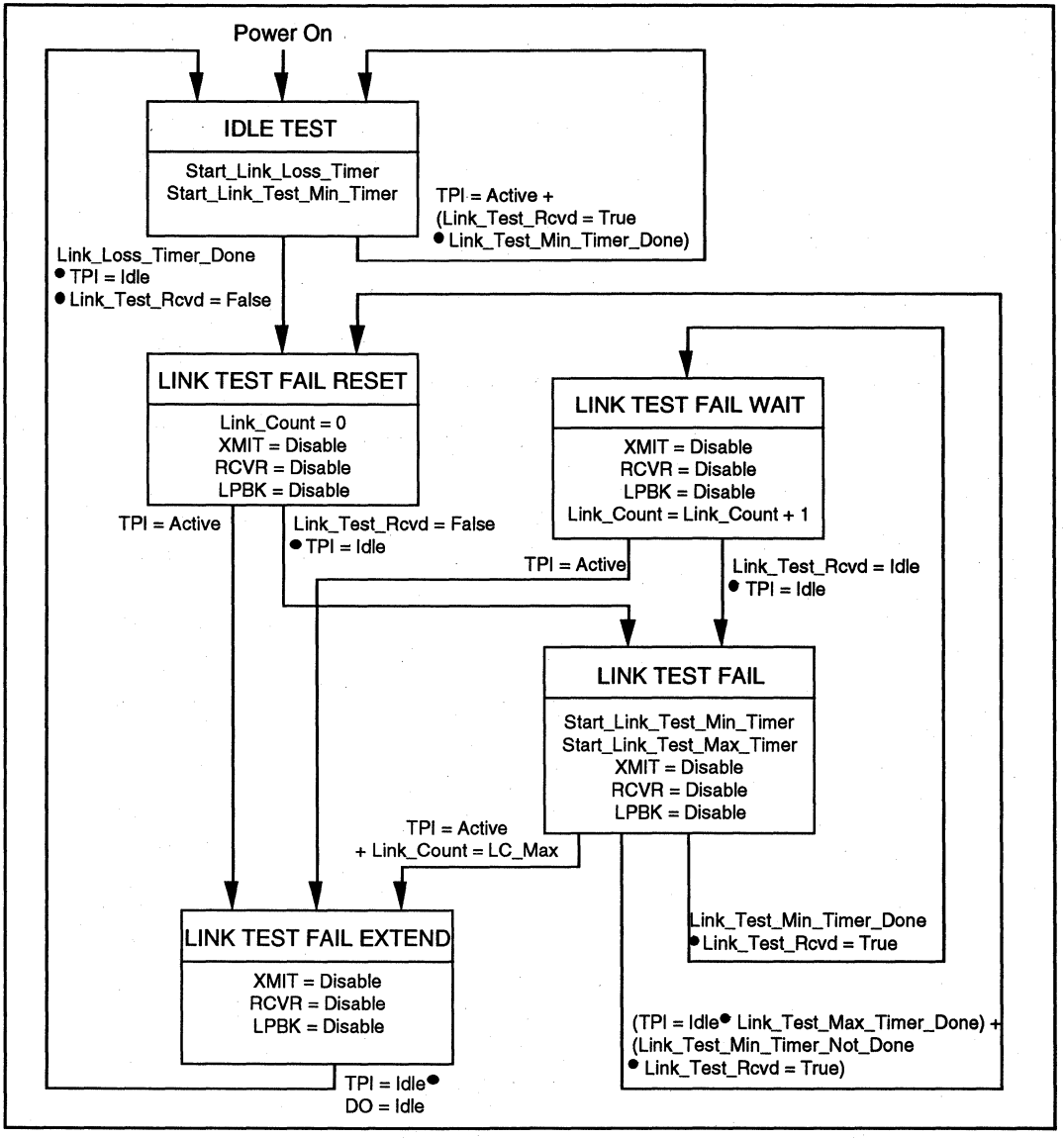
The LXT902 Test mode is selected when a 2 - 2.5 MHz clock is input on the MD0 mode select pin. Test mode sets the internal counter chains to run at 1024 times their normal speed. The maximum transmit time, unjab time, Link Integrity timing and LED timing are reduced by a factor of 1024. During test operation, 10 MHz and 20 MHz signals are output on the PRC and SQE pins, respectively. When Test mode is selected, the SQE function cannot be disabled. In Test mode the PRC function can be disabled by the LI pin. Jabber can be disabled by setting MD1 = 0.

Applications

External MAU

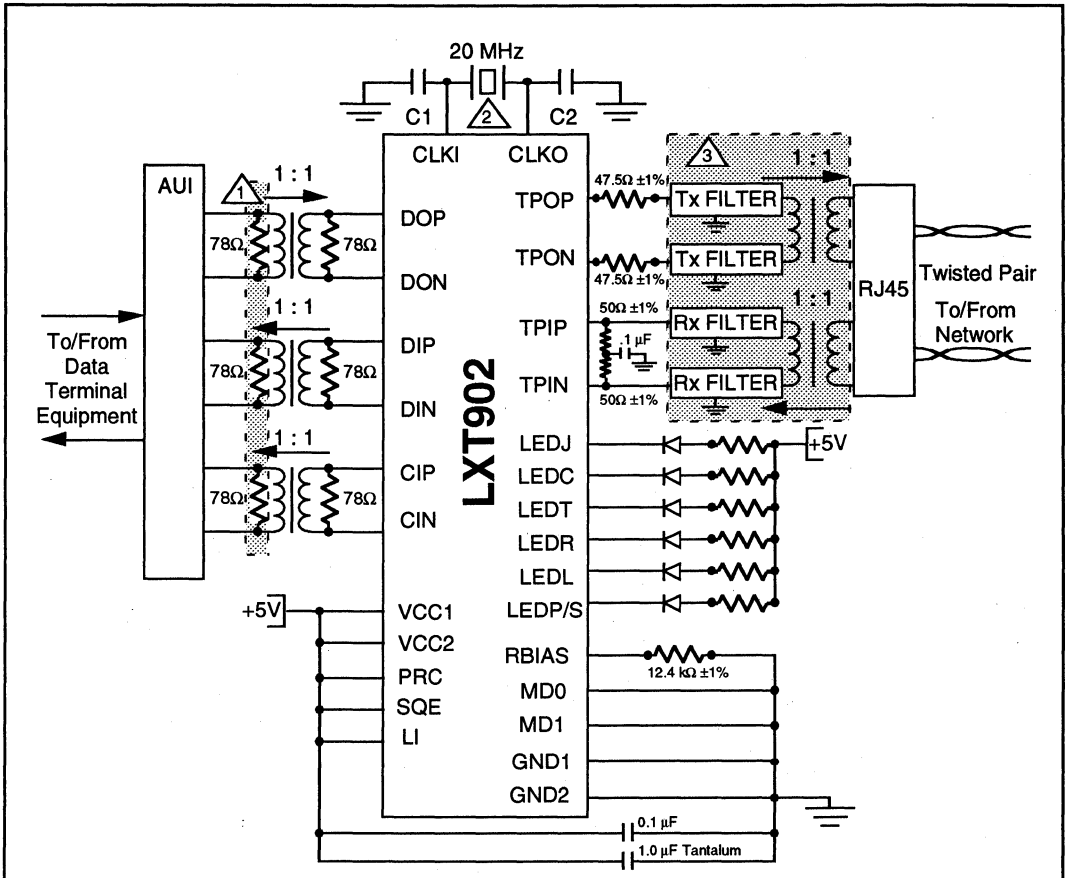
Figure 8 shows the LXT902 in a typical external MAU application, interfacing between an AUI and the RJ45 connectors of the twisted pair network. A 20 MHz crystal (or

Figure 7: Link Integrity Test Function



ceramic resonator) connected across CLKI and CLKO provides the required clock signal. Transmit and receive filters are required in the TPO and TPI circuits. Details of the transmit and receive filters are shown in Figures 9 and 10, respectively. (Differential filters are also recommended.)

Figure 8: LXT902 External MAU Application Diagram



1. Typically, resistors on the AUI side of the transformer are already present in the terminal. If termination resistors are present in the terminal, the shaded resistors are not required.
2. A 20 MHz (±1%) crystal or ceramic resonator may be used at CLKI/CLKO.
3. Suitable integrated filter/transformers include Pulse Engineering PE65421, FilMag 78Z1120B; Valor PT3877; and HALO Electronics FD02-101G and FD12-101G.

Figure 9: Transmit Filter Diagram

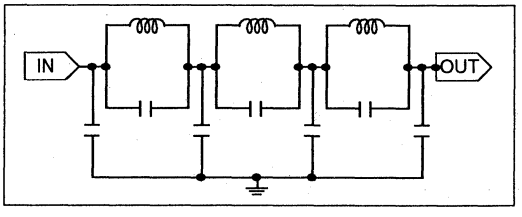
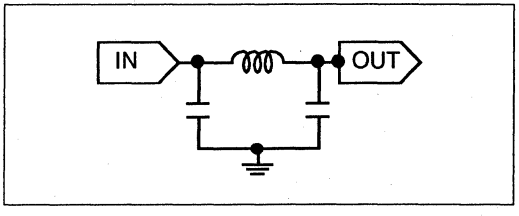


Figure 10: Receive Filter Diagram



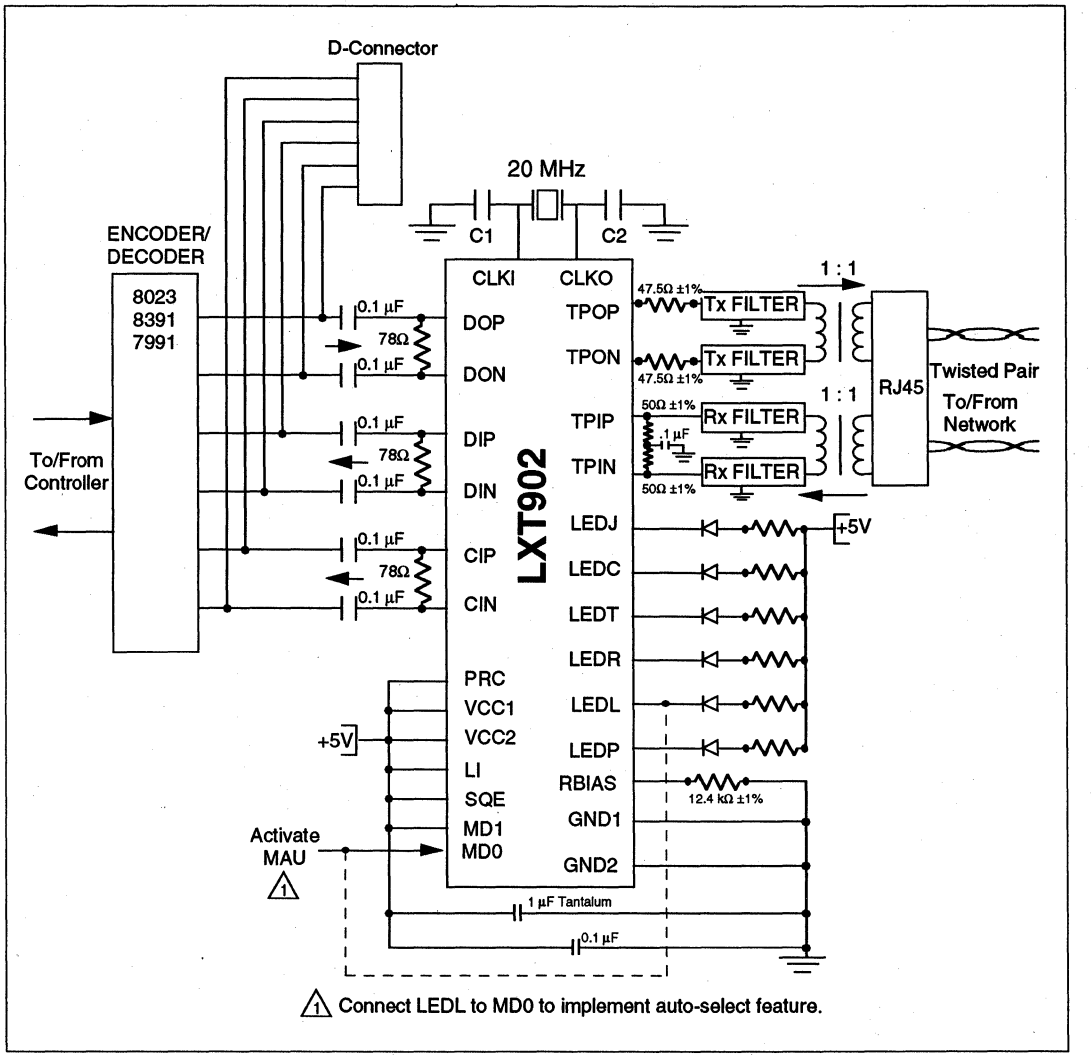
Internal MAU

Figure 11 shows an internal MAU application which takes advantage of the LXT902's unique AUI/10Base-T switching feature to select either the D-connector (AUI) or the RJ45 connector (10Base-T). No termination resistors are used on the LXT902 side of the AUI interface to prevent impedance mismatch with the drop cable. The half current drive mode is used to maintain the same voltage levels in the absence of termination resistors. This application uses capacitive coupling instead of transformer coupling. MD1 is tied high so MD0 functions as the mode control switch.

When MD0 is low, the half current drive mode is selected. When MD0 is high, the LXT902 is effectively removed from the circuit. The 902 AUI ports (DO, DI and CI) are disabled isolating the LXT902 from the AUI. The LXT902 DI and CI ports go to a high impedance state and the DO port is ignored.

To implement an auto-select function, LEDL can be tied to MD0. This activates the 902/AUI interface when the TP link is active (data or link integrity pulses) and disables it when the link is inactive.

Figure 11: LXT902 Internal MAU Application Diagram



LXT903

10Base-T Hub Transceiver

General Description

The LXT903 hub transceiver is designed for use in multi-port repeaters. It interfaces the hub (a multi-port transceiver) to the unshielded twisted-pair media. The LXT903 performs transmit, receive and receive squelch functions. Additional implementations include 10Base-T link integrity testing, automatic correction of receive polarity reversal, and a watchdog timer to jab continuous transmission.

The LXT903 software control mode provides a microprocessor interface with extensive command and status options. The hardware mode provides stand-alone operation.

The LXT903 is an advanced CMOS device and requires only a single 5-volt power supply.

Applications

- Multi-port Repeaters

Features

- Meets or exceeds IEEE 802.3 standards for 10Base-T interface
- Provides predistorted signal to the transmit filter
- Internal programmable squelch circuits
- Detection and correction of reversed polarity
- Microprocessor interface and control
- Differential or single-ended transmit input
- LED driver for jabber, link and reversed polarity
- Single 5 V supply, low-power CMOS technology
- Available in 24-pin DIP and 28-pin PLCC packages

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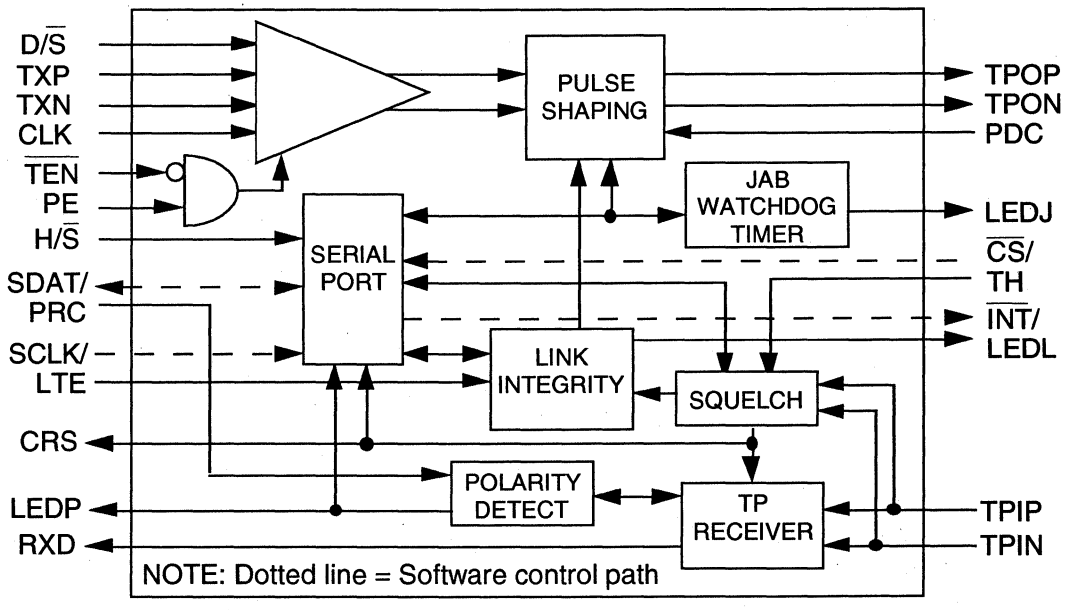
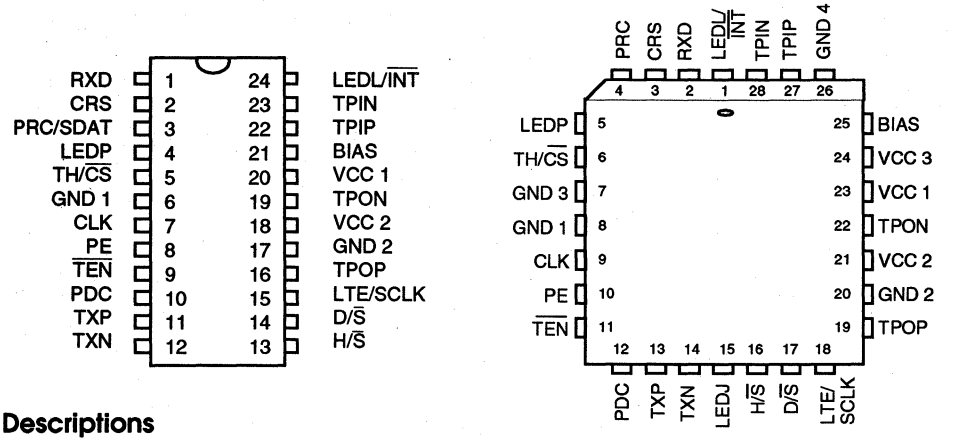
Figure 1: Block Diagram





Pin Descriptions

Pin # DIP	Pin # PLCC	Sym	I/O	Name	Description
1	2	RXD	O	Receive Data	Data received from the twisted-pair is output to the hub controller DI circuit on this pin as a CMOS level Manchester encoded data stream. High impedance when in software shut down mode.
2	3	CRS	O	Carrier Sense	Goes high to indicate valid receive data. High impedance when in software shut down mode.
3	4	PRC	I	Polarity Reverse Correction *(Hardware Control)*	In the hardware control mode, tying this pin high enables the LXT903 to automatically correct for reversed polarity at the TPI circuit.
		SDAT	I/O	Serial Data *(Software Control)*	In software control mode, this pin is the serial data I/O port.
4	5	LEDP	O	Polarity Reverse	Open drain output. Active low indicates polarity reversed.
5	6	TH	I	Threshold Control *(Hardware Control)*	In hardware mode, forcing this pin low reduces the TP receive squelch by 4.5 dB.
		$\overline{CS}$	I	Chip Select *(Software Control)*	Active low input accesses the serial port in the software mode. $\overline{CS}$ must transition high to low, and remain low for each port operation.
6	8	GND1	–	Ground # 1	Ground.
7	9	CLK	I	Clock	20 MHz CMOS level clock input.
8	10	PE	I	Port Enable	Active CMOS high enables the transmitter. In differential input mode, PE must be high when $\overline{TEN}$ is low to enable transmitter.
9	11	$\overline{TEN}$	I	Transmit Enable	Active CMOS low enables the transmitter when PE is high. Required for differential input mode only.
10	12	PDC	I	Pre-Distortion Control	A CMOS level, synchronous input signal at logic 1 will predistort the output voltage (differential input mode only).
11 12	13 14	TXP TXN	I I	Data Out Positive Data Out Negative	Differential input pair connected to the hub controller DO circuit. When D/$\overline{S}$ pin is tied low, TXP becomes single-ended CMOS level input, synchronous to the 20 MHz CLK.

Pin Descriptions continued

Pin # DIP	Pin # PLCC	Sym	I/O	Name	Description
N/A	15	LEDJ	O	Jabber LED Driver	Open drain driver for the Jabber indicator LED. Goes active when watchdog timer begins jab and stays active until end of the unjab wait period (491 - 525 ms).
13	16	H/$\overline{S}$	I	Hardware/Software Control Select	When set to a logic 0, selects software control mode. When set to a logic 1, selects hardware control mode.
14	17	D/$\overline{S}$	I	Differential/Single-Ended Select	When set to a logic 0, selects single-ended TXP input. When set to a logic 1, selects differential TXP/TXN input.
15	18	LTE	I	Link Test Enable *(Hardware Control)*	In hardware control mode, an active high on this pin enables the link test function.
		SCLK	I	Serial Clock *(Software Control)*	The serial clock required for software control operation is input on this pin. SCLK must be ≤ 2 MHz.
16	19	TPOP	O	Twisted Pair Transmit Outputs	Transmit drivers to the twisted-pair output filter. The output is pre-distorted to meet the 10Base-T template.
19	22	TPON	O		
17	20	GND 2	–	Ground 2	Ground.
N/A	7	GND 3	–	Ground 3	Ground.
N/A	26	GND 4	–	Ground 4	Ground.
18	21	VCC 2	–	Power Supply # 2	+ 5 V power supply input.
20	23	VCC 1	–	Power Supply # 1	+ 5 V power supply input.
N/A	24	VCC 3	–	Power Supply # 3	+ 5 V power supply input.
21	25	BIAS	O	Resistor Bias Control	Bias control for the operating circuit. Bias is set from an external 12.4 kΩ resistor to ground.
22	27	TPIP	I	Twisted-Pair Receive Inputs	Differential receive inputs from the twisted-pair input filter.
23	28	TPIN	I		
24	1	LEDL[1]	O	Link Driver *(Hardware Control)*	LED driver indicates link activity.
		$\overline{INT}$	O	Interrupt *(Software Control)*	The microprocessor interrupt required for software control is output on this pin. The interrupt is an open drain, active low which indicates Jab, Link Failure or Non-correctable Polarity.

[1] LED drivers pull low when active.

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

• Supply Voltage	V_{CC}	-0.3 V to 6 V
• Operating temperature	T_{OP}	0 °C (min) to +70 °C (max)
• Storage temperature	T_{ST}	-65 °C (min) to +150 °C (max)

Recommended Operating Conditions (Voltages are with respect to ground unless otherwise specified.)

Parameter	Symbol	Min	Typ[1]	Max	Units
Supply voltage[2]	V_{CC}	4.75	5.0	5.25	V
Operating temperature	T_{OP}	0	-	70	°C

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Maximum voltage differential between VCC1 and VCC2 (and VCC3 for PLCC parts) must not exceed 0.3V.

I/O Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input low voltage	V_{IL}	–	–	0.8	V	
Input high voltage	V_{IH}	2.0	–	–	V	
Output low voltage (Open drain LED Driver[2])	V_{OL}	–	–	0.7	V	I_{OUT} = 10 mA
Supply current	I_{CC}	-	40	-	mA	Line Idle
		-	75	-	mA	Line Active
Input leakage current[3]	I_{LL}	-	±1	±10	µA	Input between VCC and GND
High Z state leakage current	I_{TS}	-	±1	±10	µA	Output between VCC and GND

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] LED Drivers can sink up to 10 mA of drive current.
[3] Not including TPIN, TPIP, TXN, TXP, PDC, PE, CLK or $\overline{TEN}$.

CMOS I/O Characteristics[1] (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[2]	Max	Units
Input low voltage	V_{CIL}	–	2.0	–	V
Input high voltage	V_{CIH}	–	3.0	–	V
Output low voltage	V_{COL}	–	0	–	V
Output high voltage	V_{COH}	–	5.0	–	V
Input leakage current	I_{CIL}	–	± 1.0	–	µA

[1] Pins TXP, TXN, $\overline{TEN}$, PE, PDC, CLK and RXD.
[2] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Transmit Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	Z_{OUT}	–	5	–	Ω	
Peak differential output voltage	V_{OD}	± 4.5	–	± 5.2	V	Load = 200 Ω at TXP/TXN
Differential voltage imbalance	V_{OB}	–	–	± 40	mV	Load = 200 Ω at TXP/TXN
Transmit timing jitter addition	–	–	–	± 8	ns	After Tx filter, 0 line length
Transmit timing jitter addition	–	–	–	± 3.5	ns	After Tx filter and line model specified by IEEE 802.3 for 10Base-T

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

3

Receive Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Receive input impedance	Z_{IN}	–	20	–	kΩ	Between TPIP/TPIN
Differential squelch threshold	V_{DS}	–	420	–	mV	
Reduced squelch threshold	V_{DSR}	–	250	–	mV	
Receive timing jitter	–	–	–	1.5	ns	

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Switching Characteristics[1] (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Min	Typ	Max	Units
Jabber Timing				
Maximum transmit time	88.5	–	144	ms
Unjab time	442	–	578	ms
Link Integrity Timing				
Time link loss	65	–	66	ms
Time between Link Integrity Pulses	9	–	11	ms
Valid interval for received Link Integrity Pulses	4.1	–	65	ms

Switching Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ	Max	Units
Serial interface Timing					
SCLK low time	t_{S1}	100	–	–	ns
SCLK high time	t_{S2}	100	–	–	ns
$\overline{CS}$ to SCLK setup time	t_{S3}	50	–	–	ns
SCLK to $\overline{CS}$ hold time	t_{S4}	0	–	–	ns
$\overline{CS}$ inactive time	t_{S5}	50	–	–	ns
SDAT to SCLK setup time	t_{S6}	50	–	–	ns
SCLK to SDAT hold time	t_{S7}	0	–	–	ns
SCLK to SDAT valid	t_{S8}	–	–	100	ns
SCLK falling edge or $\overline{CS}$ rising edge to SDAT high Z	t_{S9}	–	–	100	ns
SCLK rise/fall time	–	–	–	20	ns
Transmit Timing (Single Ended Mode)					
TXP setup time to CLK high	t_{ST1}	20	–	–	ns
TXP hold time from CLK high	t_{ST2}	0	–	–	ns
Transmit Timing (Differential Mode)					
TXP rising edge to PDC rising edge	t_{DT1}	–	50	–	ns
TXP low to PDC low	t_{DT2}	–	0	–	ns
TXP high to TXN low	t_{DT3}	0	–	± 5	ns
TXP low to TXN high	t_{DT4}	0	–	± 5	ns
Receive Timing					
Valid receive data to CRS high	t_{R1}	–	–	500	ns
Receive steady state propagation delay	t_{R2}	–	–	100	ns
Receive turn-off to CRS low	t_{R3}	250	–	400	ns
Receiver jitter	t_{R4}	–	–	± 1.5	ns
CRS high to RXD low	t_{R5}	0	–	100	ns
General					
Receive start-up delay	–	0	–	500	ns
Transmit start-up delay	–	0	–	200	ns
TXP/TXN rise/fall time	t_{TRF}	–	5	–	ns

Figure 2: LXT903 Serial Interface Timing

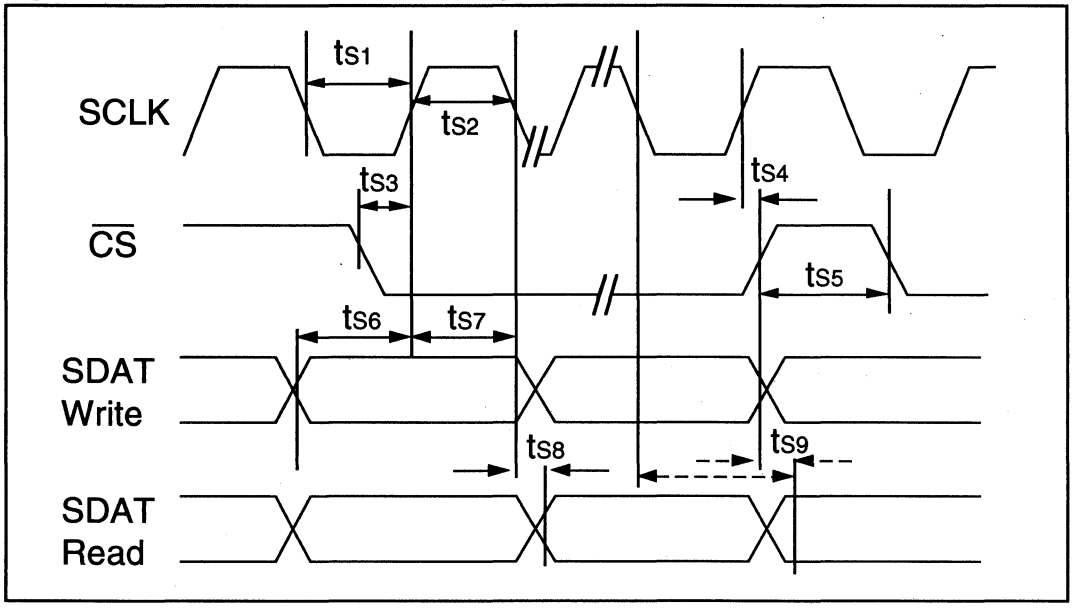


Figure 3: LXT903 Transmit Timing - Single Ended Input Mode

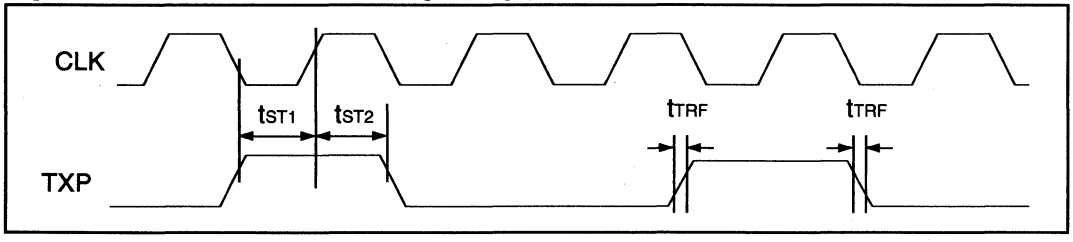


Figure 4: LXT903 Transmit Timing - Differential Input Mode

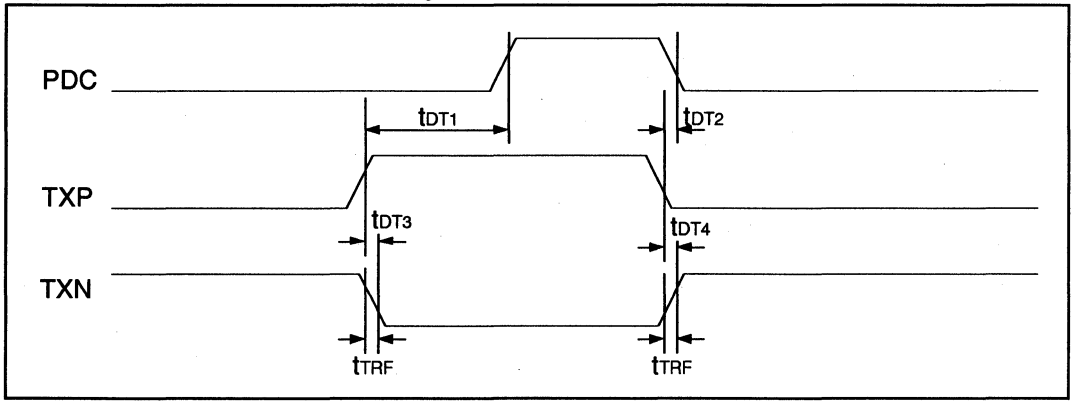
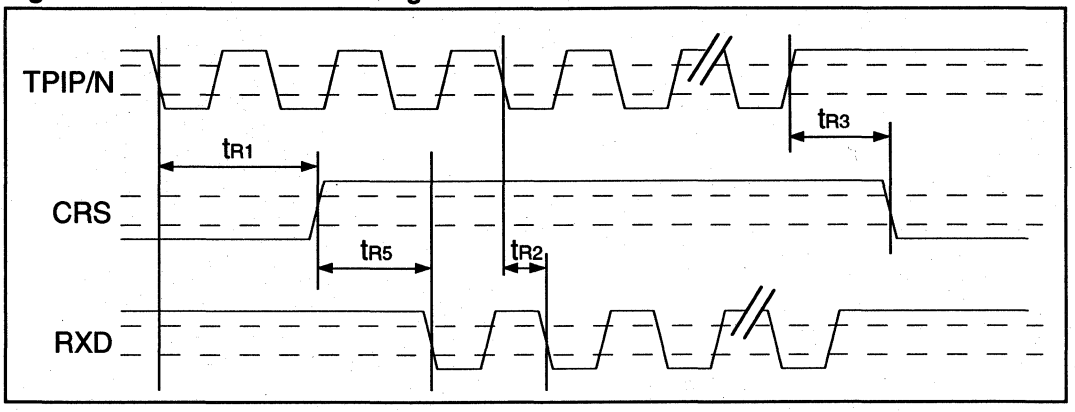


Figure 5: LXT903 Receive Timing



Functional Description

The LXT903 hub transceiver interfaces a hub controller to unshielded twisted-pair cables, transferring data in both directions. The hub side of the interface comprises three circuits: Transmit (the DO output from the hub controller), Receive (the DI input to the hub controller), and Status/ Command. The twisted-pair network side of the interface comprises two circuits: Twisted Pair Input (TPI) and Twisted Pair Output (TPO). In addition to these basic circuits, the LXT903 contains logic controls and LED drivers for status indications.

Functions are defined from the hub side of the interface. The LXT903 Transmit function refers to data transmitted by the hub over the DO circuit to the twisted-pair network. The LXT903 Receive function refers to data received by the hub over the DI circuit from the twisted-pair network. In addition to basic transmit and receive functions, the LXT903 performs some of the MAU functions defined by the IEEE 802.3 10Base-T specification such as link integrity testing and jabber control. The LXT903 also offers extensive software control and status reporting capabilities available through the serial interface.

Transmit Function

The LXT903 transfers manchester encoded, CMOS level data from the hub controller to the twisted-pair network (the TPO circuit). The output signal on TPON and TPOP is predistorted to meet the 10 Base-T jitter template. The output waveform (after the transmit filter) is shown in Figure 6. During idle periods, the LXT903 transmits link integrity test pulses on the TPO circuit. Transmitter inputs can be differential or single-ended, as selected by the D/$\overline{S}$ pin. The differential input is TXP/TXN. Single-ended input is supplied by TXP.

Single Ended Input Mode

The single ended transmit interface consists of TXP, Port Enable (PE) and the 20 MHz clock input (CLK). In the single-ended mode, TXP is sampled before transmission at the 20 MHz clock rate and must meet the specified setup and hold times relative to the CLK input. Predistortion control is generated internally. PE must be high for transmission to occur. Transmission begins at the first low-going data on TXP. End of Frame is detected when TXP is held high for more than 150 ns (plus setup and hold times).

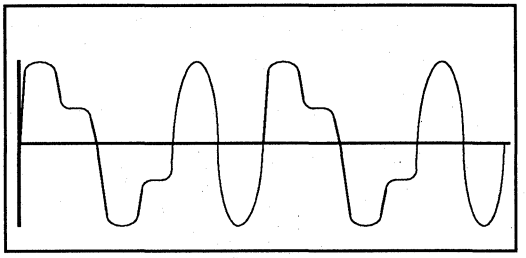
Differential Input Mode

In the differential input mode, the transmit interface consists of TXP and TXN, PE, PDC, and the Transmit Enable input ($\overline{TEN}$). Transmission starts when PE is high and $\overline{TEN}$ is low, and ends when either PE or $\overline{TEN}$ goes inactive. Predistortion control is provided by the PDC input.

Receive Function

The LXT903 receive function accepts serial data from the twisted-pair network (the TPI circuit), converts it to a CMOS level signal, and passes it to the hub controller. An internal squelch function discriminates noise from link test pulses and valid data streams. Only valid data streams activate the receive function. If the differential signal at the TPI circuit

Figure 6: LXT903 TPO Output Waveform

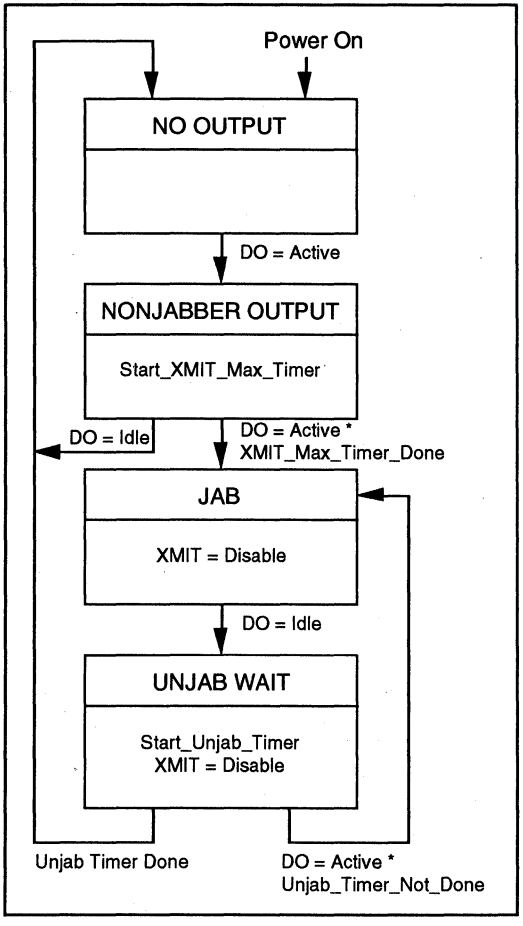


input falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT903 receive function will enter the idle state. A reduced threshold is available which lowers the squelch level by 4.5 dB. Reducing the squelch level extends the network range when used with a low-noise media such as shielded twisted-pair. In the software control mode, the reduced threshold is selected through the serial interface. In the hardware mode, the reduced threshold is selected by tying the TH pin low.

Polarity Reverse Function

The LXT903 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is declared when eight opposite link pulses are received without receipt of a link pulse with the expected polarity. Reversed polarity is also declared if four frames are received with a reversed start-of-idle. Whenever reversed polarity is declared, these two counters are reset to zero. If the LXT903 enters the link fail state and no receive data or link pulses are received within 96 to 128 ms, the polarity is reset to the default (non-flipped) condition. (If Link Integrity is disabled, polarity detection is based only on received data.)

Figure 7: Jabber Control Function



Jabber Control Function

Figure 7 is a state diagram of the LXT903 Jabber control function. In the software mode, jabber control may be disabled through the serial port. In the hardware mode, jabber control is enabled at all times. The LXT903 on-chip watchdog timer prevents the device from locking into a continuous transmit mode. When a transmission exceeds the time limit, the Watchdog timer disables the transmit function. Once the LXT903 is in the jabber state, the transmit circuit must remain idle for a period of 491 to 525 ms before it will exit the jabber state.

Link Integrity Test

Figure 8 is a state diagram of the LXT903 Link Integrity Test Function. The Link Integrity Test is used to determine the status of the receive side twisted-pair cable. Link testing is enabled when the LTE pin is tied high. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulse is detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit function. The LXT903 ignores any link integrity pulse with interval less than 2 - 7 ms. The LXT903 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses. Link activity is indicated by a low on the LEDL pin.

Hardware Control Mode

In hardware control mode the serial port is not used, and the transceiver is accessed and controlled through individual pins. Hardware control mode is selected when the H/$\overline{S}$ pin is set to a logic 1.

Software Control Mode

To allow a microprocessor to access and control the LXT903 through the serial interface, the H/$\overline{S}$ pin is set to logic 0. The serial interface consists of three signals: the Chip Select input ($\overline{CS}$), the bidirectional Serial Data port (SDAT), and a Serial Clock (SCLK). The LXT903 incorporates a standard microcontroller interface which operates with any standard 8051 using $\overline{TXD}$/RXD (port 3) for SCLK and SDAT, and any port for $\overline{CS}$. The SCLK frequency should be 5 MHz or less. In software control mode, the LEDL pin is reconfigured as an interrupt out ($\overline{INT}$). $\overline{INT}$ is an open drain, active low which is set by any of three conditions: Jab, Link Fail, or Non-Correctable Polarity. The $\overline{INT}$ signal stays active until CS goes active (low). The $\overline{INT}$ bit remains set until the first port read cycle. Once set and then cleared, $\overline{INT}$ will not set again until all failure interrupts return to a pass state. The $\overline{INT}$ signal can be masked by bit C4 of the Command word. The serial data (SDAT) is contained in a

16-bit word consisting of an 8-bit Address/Command byte and an 8-bit Command/Status byte. Figure 9 shows the serial interface data structure and timing.

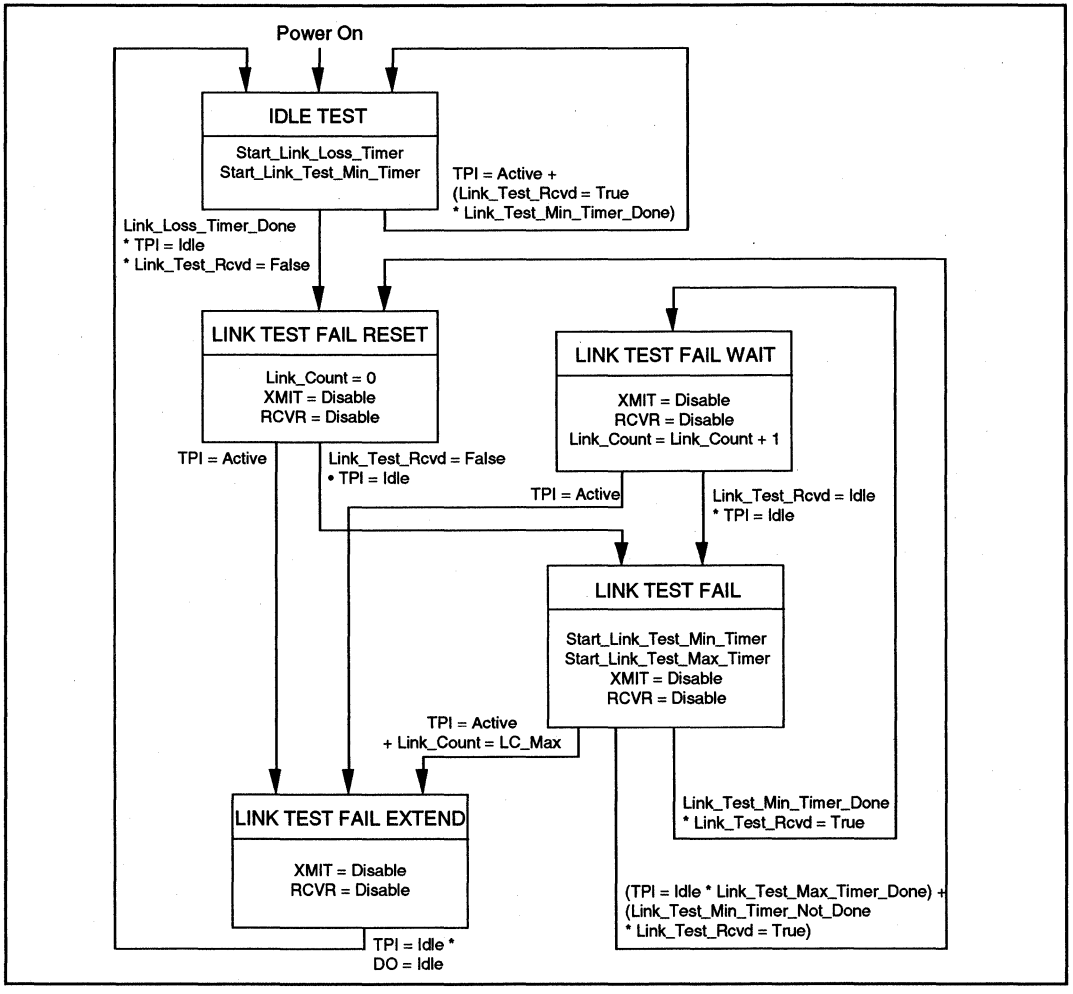
The Address/Command bits are assigned as follows:

AC0 Test Mode. Must be 0 (1 reserved for Factory)
AC1 Address Bit 0. Must be 0 (reserved)
AC2 Address Bit 1. Must be 0 (reserved)
AC3 Address Bit 2. Must be 1 (reserved)
AC4 Read/Write. 1 = Read, 0 = Write
AC5 Must be 0 (reserved)
AC6 Must be 0 (reserved)
AC7 Must be 0 (reserved)

The Command (Write) bits are assigned as follows:

C0 Shut Down (TXP/TXN and TEN are ignored, RXD and CRS go to high impedance. Standard transmit functions are disabled, but Link Pulse reception/transmission continue.)
C1 Link Test Enable/Disable
C2 Jabber Enable/Disable
C3 Polarity Correction Enable
C4 Mask Interrupt (Prevents the open drain $\overline{INT}$ pin from going active.)
C5 Reduced Threshold (Receive threshold reduced by 4.5 dB.)
C6 Must be 0 (reserved)
C7 Must be 0 (reserved)

Figure 8: Link Integrity Test Function

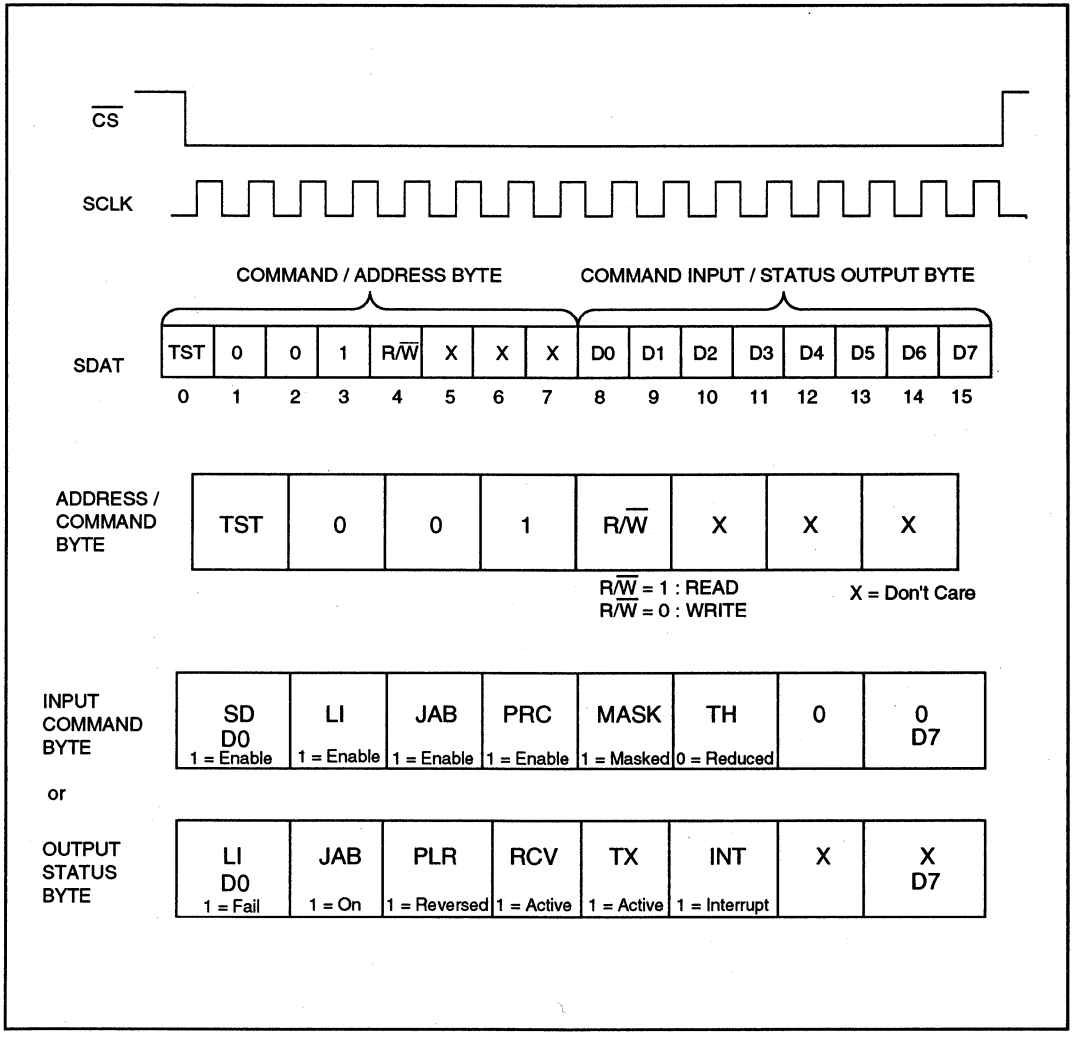


The Status (Read) bits are assigned as follows:

S0 Link Test Fail/Pass
S1 Jabber On/Off
S2 Polarity Reversed/Normal
S3 Receiver Active (Cleared on Read)
S4 Transmitter Active (Cleared on Read)
S5 Interrupt (Cleared on Read)
S6 Don't Care
S7 Don't Care

The LXT903 serial port is accessed by causing the Chip Select ($\overline{CS}$) input to transition from high to low. Bit 4 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation.

Figure 9: LXT903 Serial Interface Data Structure



Applications

Figure 10 shows the LXT903 in a typical hardware control application. The LXT903 hub transceivers interface the Hub Controller to the RJ45 connectors of the twisted pair network. The D/$\overline{S}$ pin is grounded, effecting the single ended mode, so TXN, PDC and $\overline{TEN}$ are not connected. An external source provides the required 20 MHz clock signal. Transmit and receive filters are required in the TPO and TPI circuits. Details of the transmit and receive filters are shown in Figures 11 and 12, respectively. (Differential filters are also recommended.) Integrated filters such as the Valor PT3877, Fil-Mag 78Z1120B or Pulse Engineering PE65421 may be used. Figure 13 shows a typical software control application, operating in the differential input mode (D/$\overline{S}$ is tied high) with TXN, $\overline{TEN}$, and PDC connected.

Figure 10: Typical LXT903 Hardware Control Application

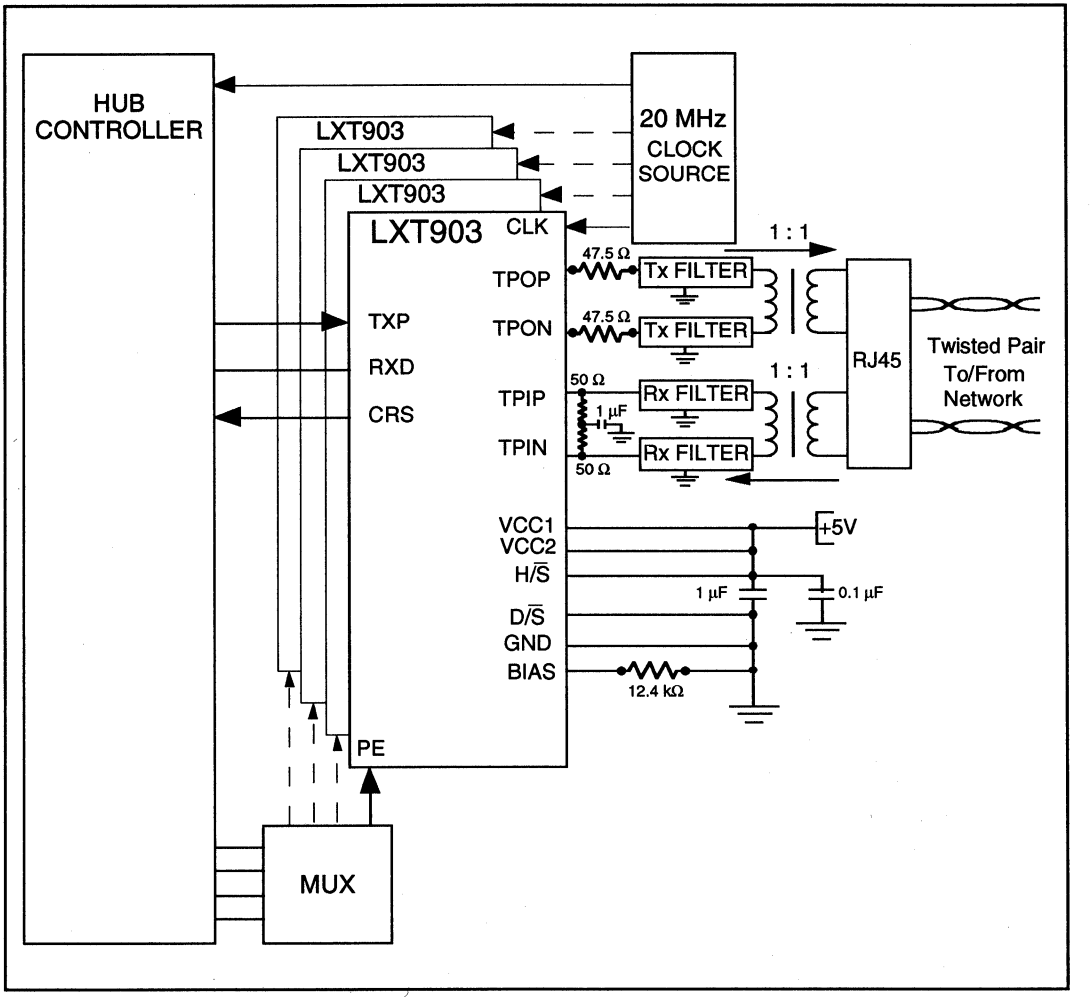


Figure 11: Transmit Filter Diagram

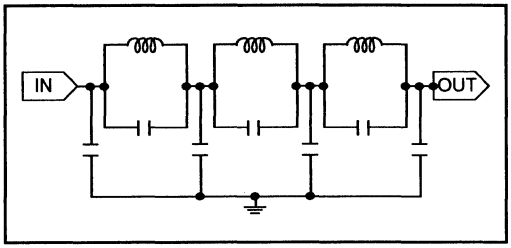


Figure 12: Receive Filter Diagram

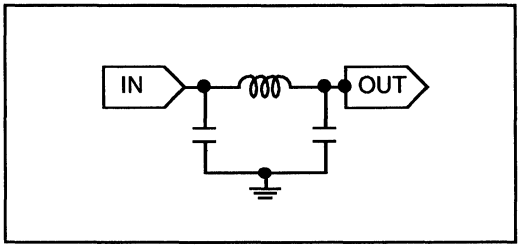
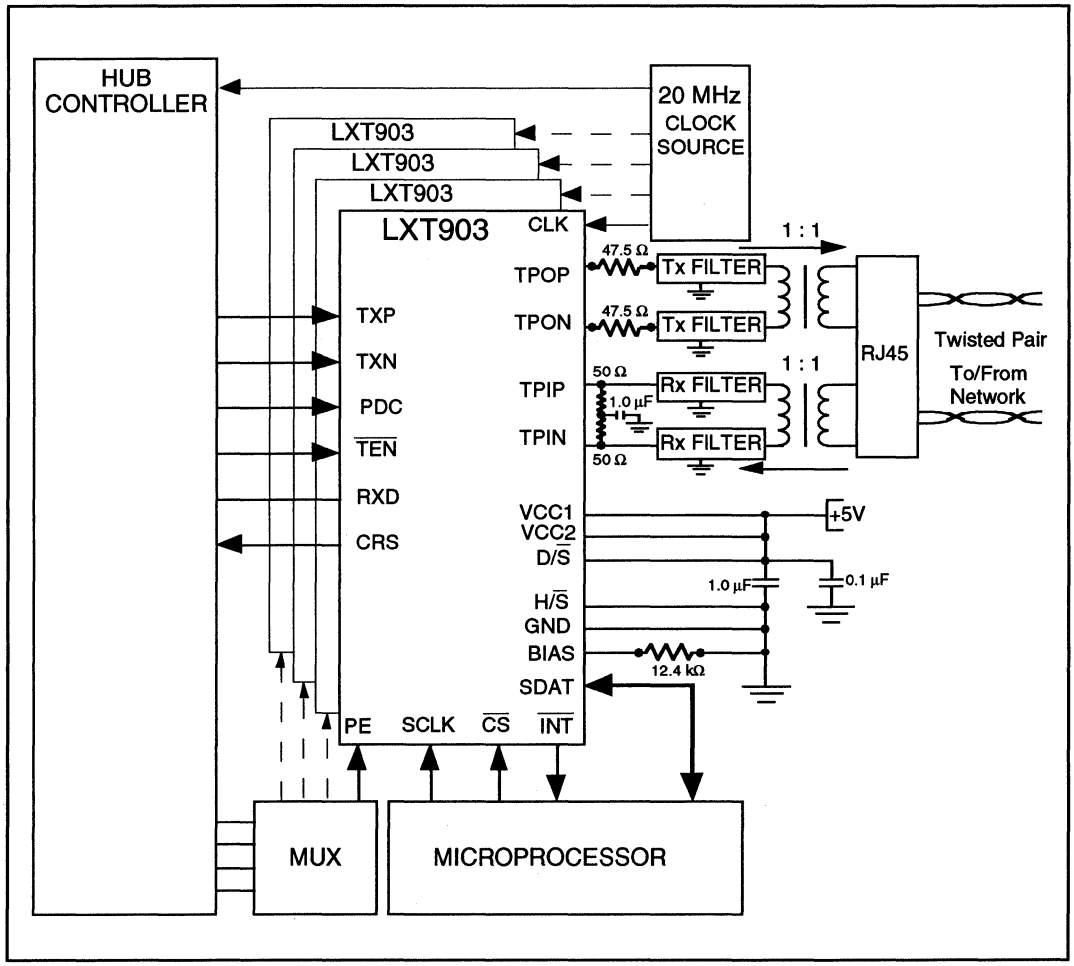


Figure 13: Typical LXT903 Software Control Application



NOTES:

LXT906

Ethernet Twisted-Pair / Coax Adapter

General Description

The LXT906 Twisted-Pair / Coax Adapter is designed to allow a cost effective Ethernet implementation in a mixed media environment. Combined with a coax transceiver such as the DP8392, the LXT906 offers a complete adapter solution.

LXT906 functions include level-shifted data pass-through from one transmission media to another, collision detection and propagation, and automatic correction of polarity reversal on the twisted pair input. It also includes LED drivers for jabber, coax receive and collision, twisted pair receive and collision, reversed polarity detect and link indication functions.

The LXT906 is an advanced CMOS device and requires only a single 5 volt power supply.

Applications

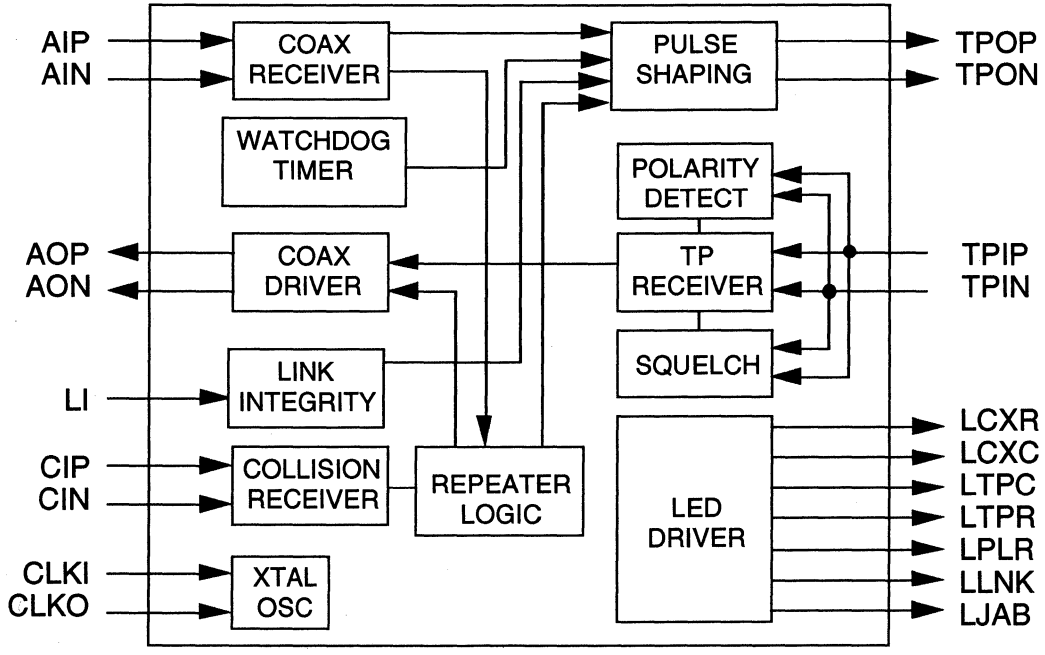
- 10Base-T to Coax (10Base5 and 10Base2) adapter

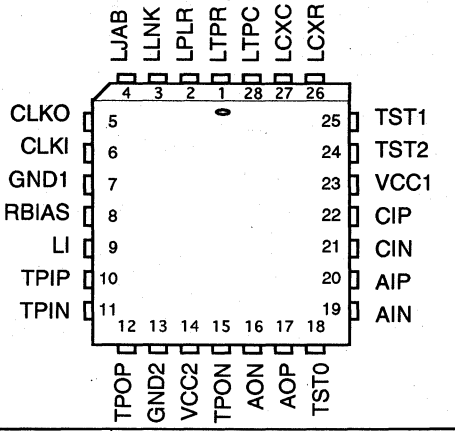
Features

- Direct interface to Coax transceiver and to RJ45 connectors.
- Collision detection and propagation
- Internal predistortion generation
- Internal common mode voltage generation
- Selectable link test
- Twisted-pair receive polarity reverse detection and correction
- LED drivers for TP and coax receive; TP and coax collision; jabber, link active and reversed polarity indicators
- Single 5 V supply, CMOS technology
- Available in 28-pin PLCC

3

Figure 1: Block Diagram





Pin Descriptions

Pin	Sym	I/O	Name	Description
1	LTPR	O	TP Receive LED Driver	Open drain driver for the TP Receive indicator LED. Output pulls low whenever TP receiver is active.
2	LPLR	O	TP Reverse Polarity LED Driver	Open drain driver for the TP Reversed Polarity indicator LED. Output pulls low whenever reversed polarity is detected.
3	LLNK	O	TP Link LED Driver	Open drain driver for the TP Link indicator LED. Output goes high whenever link is active.
4	LJAB	O	Jabber LED Driver	Open drain driver for the Jabber indicator LED. Output pulls low whenever LXT906 is in a jabber condition.
5 6	CLKO CLKI	I/O	Crystal Oscillator	The LXT906 requires either a 20 MHz crystal (or ceramic resonator) connected across these pins, or a 20 MHz clock applied at CLKI.
7	GND1	–	Ground 1	Ground.
8	RBIAS	I	Resistor Bias Control	Bias control pin for the operating circuit. Bias set from external resistor to ground. External resistor value = 12.4 kΩ (± 1%).
9	LI	I	Link Integrity	Enables Link Integrity Testing when tied high.
10 11	TPIP TPIN	I I	Twisted-Pair Receive Inputs	Differential receive inputs from the twisted pair input filter.
12 15	TPOP TPON	O O	Twisted-Pair Transmit Outputs	Transmit drivers to the twisted-pair output filter. The output is Manchester encoded and pre-distorted to meet the 10Base-T template.
13	GND2	–	Ground 2	Ground.
14	VCC2	I	Power Supply 2	+5 V power supply input.
16 17	AON AOP	O O	AUI Out Negative AUI Out Positive	Differential driver output pair connected to the Coax AUI.
18	TST0	–	Test Pin 0	Test pin for factory use. This pin must be left unconnected.

Pin Descriptions continued

Pin	Sym	I/O	Name	Description
19 20	AIN AIP	I I	AUI In Negative AUI In Positive	Data input pair from the Coax AUI.
21 22	CIN CIP	I I	Collision Negative Collision Positive	Differential input pair tied to the collision presence pair of the Ethernet Coax transceiver.
23	VCC1	I	Power Supply 1	+5 V power supply.
24 25	TST2 TST1	– –	Test Pin 2 Test Pin 1	Test pins reserved for factory use. These pins must be left unconnected.
26	LCXR	O	Coax (AUI) Receive LED Driver	Open drain driver for the Coax Receive indicator LED. Output pulls low whenever coax receiver is active.
27	LCXC	O	Coax Collision LED Driver	Open drain driver for the Coax Collision indicator LED. Output pulls low whenever a collision is detected on the coax circuit.
28	LTPC	O	TP Collision LED Driver	Open drain driver for the TP Collision indicator LED. Output pulls low whenever a collision is detected on the TP line.

3

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- Supply Voltage V_{CC} -0.3 V to 6 V
- Operating temperature T_{OP} 0 °C (min) to +70 °C (max)
- Storage temperature T_{ST} -65 °C (min) to +150 °C (max)

Recommended Operating Conditions (Voltages are with respect to ground unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Operating temperature	T_{OP}	0	-	70	°C

Switching Characteristics (Ta = 0 to 70 °C, V_{CC} = 5 V ± 5 %)

Parameter	Min	Typ[1]	Max	Units
Jam Timing				
Transmit time	96	–	–	bit
Link Integrity Timing				
Time link loss[2]	65	–	66	ms
Time between Link Integrity Pulses[2]	9	–	11	ms
Interval for valid receive Link Integrity Pulses[2]	3.9	–	65	ms
Collision Timing				
End of collision to end of jam	–	–	1200	ns
Jabber Timing				
Maximum transmit time	–	–	5.1	ms
Unjab time	–	6.4	–	us
LED Timing				
LED on time	100	–	–	ms
General				
Transmit recovery time	–	–	12	bit
Carrier recovery time	–	–	3	bit
TP receive to AUI transmit	0	–	500	ns
AUI receive to TP transmit	0	–	200	ns

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Switching times reduced by a factor of 1024 during Test mode.

AUI Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5 V ± 5 %)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input low current	I_{IL}	–	–	-700	µA	
Input high current	I_{IH}	–	–	500	µA	
Differential output voltage	V_{OD}	± 550	–	± 1200	mV	
Differential squelch threshold	V_{DS}	–	220	–	mV	
Receive input impedance	R_Z	–	20	–	kΩ	Between AOP and AON

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

I/O Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5 V ± 5 %)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input low voltage	V_{IL}	–	–	0.8	V	
Input high voltage	V_{IH}	2.0	–	–	V	
Output low voltage (Open drain LED Driver)	V_{OL}	–	–	0.7	V	Load current = 10 mA
Supply current ($V_{CC}1 = V_{CC}2 = 5.25$ V)	I_{CC}	–	60	80	mA	Line Idle
		–	125	150	mA	Line Active, transmitting all ones
Input leakage current[2]	I_{LL}	–	± 1	50	µA	Input between VCC and GND

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Not including TPIN, TPIP, AIP, AIN, CIP or CIN.

3

TP Transmit Characteristics (Ta = 0 to 70 °C, V_{CC} = 5 V ± 5 %)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	Z_{OUT}	–	5	–	Ω	
Peak differential output voltage	V_{OD}	± 4.5	–	± 5.2	V	Load = 200 Ω at TPOP and TPON
Transmit timing jitter addition [2]	–	–	–	± 8	ns	After Tx filter, 0 line length

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Parameter is guaranteed by design; not subject to production testing.

TP Receive Characteristics (Ta = 0 to 70 °C, V_{CC} = 5 V ± 5 %)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Receive input impedance	Z_{IN}	–	20	–	kΩ	Between TPIP/TPIN
Differential squelch threshold	V_{DS}	–	420	–	mV	
Receive timing jitter [2]	–	–	–	1.5	ns	

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Parameter is guaranteed by design; not subject to production testing.

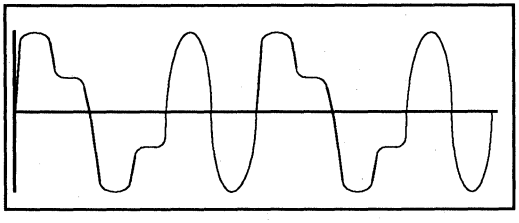
Functional Description

The LXT906 interfaces the coaxial transceiver (AUI) to the unshielded twisted pair cables, transferring data in both directions. The AUI side of the interface comprises three circuits: Data Output (AO), Data Input (AI) and Collision Interface (CI). The twisted pair network side of the interface comprises two circuits: Twisted Pair Input (TPI) and Twisted Pair Output (TPO). In addition to the five basic circuits, the LXT906 contains an internal crystal oscillator, various logic controls and seven LED drivers for status indications.

Coax to TP Function

The LXT906 receives data from the coax transceiver on the AI circuit and transmits it to the twisted pair network on the TPO circuit. The output signal on TPON and TPOP is pre-distorted to meet the 10Base-T jitter template. The output waveform (after the transmit filter) is shown in Figure 2. If the differential inputs at the AI circuit fall below 75% of the threshold level for 8 bit times (typical), the LXT906 TP transmit function will enter the idle state. During idle periods, the LXT906 transmits link integrity test pulses on the TPO circuit.

Figure 2: LXT906 TPO Output Waveform



TP to Coax Function

The LXT906 receives data from the twisted pair network on the TPI circuit and transmits it to the coax transceiver on the AO circuit. An internal squelch function discriminates noise from link test pulses and valid data streams. Only valid data streams activate the TP receive function. If the differential inputs at the TPI circuit fall below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT906 TP receive function will enter the idle state. The Coax-to-TP data path is disabled when the TP-to-Coax path is active. The Coax-to-TP path is enabled 9 bit times after end of TP-to-Coax transmission.

Polarity Reverse Function

The LXT906 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is detected when eight link pulses of the opposite (unexpected) polarity are received without receipt of a link pulse with the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever polarity is reversed, these two counters are reset to zero. If the LXT906 enters the link fail state and no data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity is disabled, polarity detection is based only on received data pulses.) The LXT906 automatically corrects for reversed polarity.

Jabber Function

The LXT906 interrupts its output if it has transmitted continuously for longer that 5 ms on TPOP/TPON or AOP/AON. During jab the repeater state machine is disabled. Transmission is re-enabled when no activity has been detected on TPIP/TPIN or AIP/AIN for 6.4 µs.

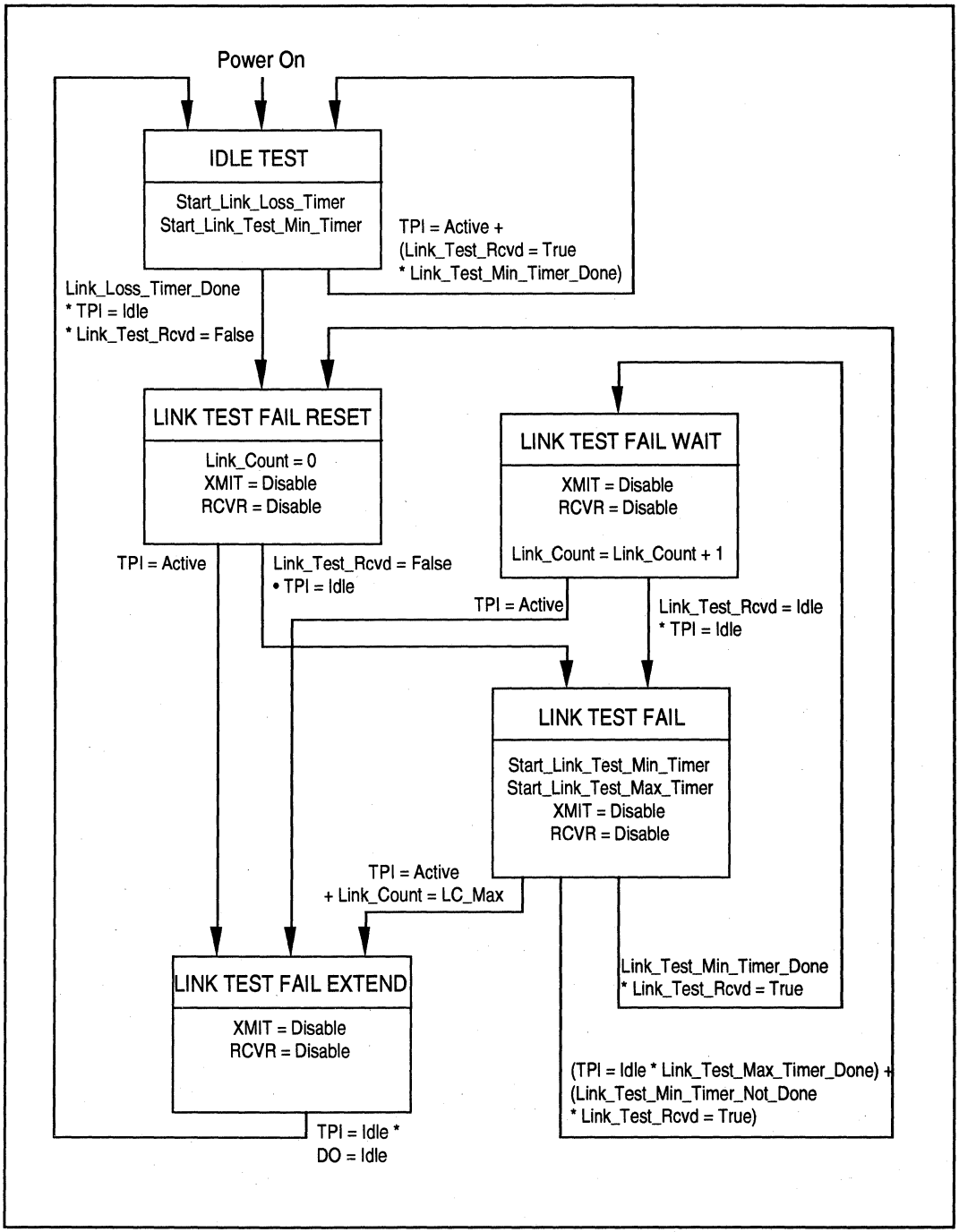
Link Integrity Test Function

Figure 3 is a state diagram of the LXT906 Link Integrity Test Function. The Link Integrity Test is used to determine the status of the twisted pair cable. Link integrity testing is enabled when the LI pin is tied high. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit function and the repeater state machine. The LXT906 ignores any link integrity pulse with interval less than 2 - 7 ms. The LXT906 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

Collision Propagation Function

A TP collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. A Coax collision is detected when a valid collision signal is present at CIP/CIN. If a collision is detected the appropriate collision LED (TP or coax) is activated and a Jam frame is transmitted as described in Figure 4. The Jam length is always a minimum of 96 bits: 64 bits of alternating 1's and 0's, followed by an all 1's pattern.

Figure 3: Link Integrity Test Function



LXT906 State Diagram

The state diagram, Figure 4, describes the operation of the LXT906. It is similar to a repeater state diagram, however the 906 does not provide retiming, preamble regeneration or fragment extension. The LXT906 avoids fragment generation by using a minimum Jam size of 96 bits. Since the TP side does not have a receive collision detection it is not considered in this implementation.

Description of State diagram variables :

cXcoll : Coax collision active
TPcoll : TP collision active
cXact : Coax data active
TPact : TP data active
Tw1 : 9 bit time
Tw2 : 3 bit time
Jam : Minimum 96 bit time

Figure 4: LXT906 State Diagram

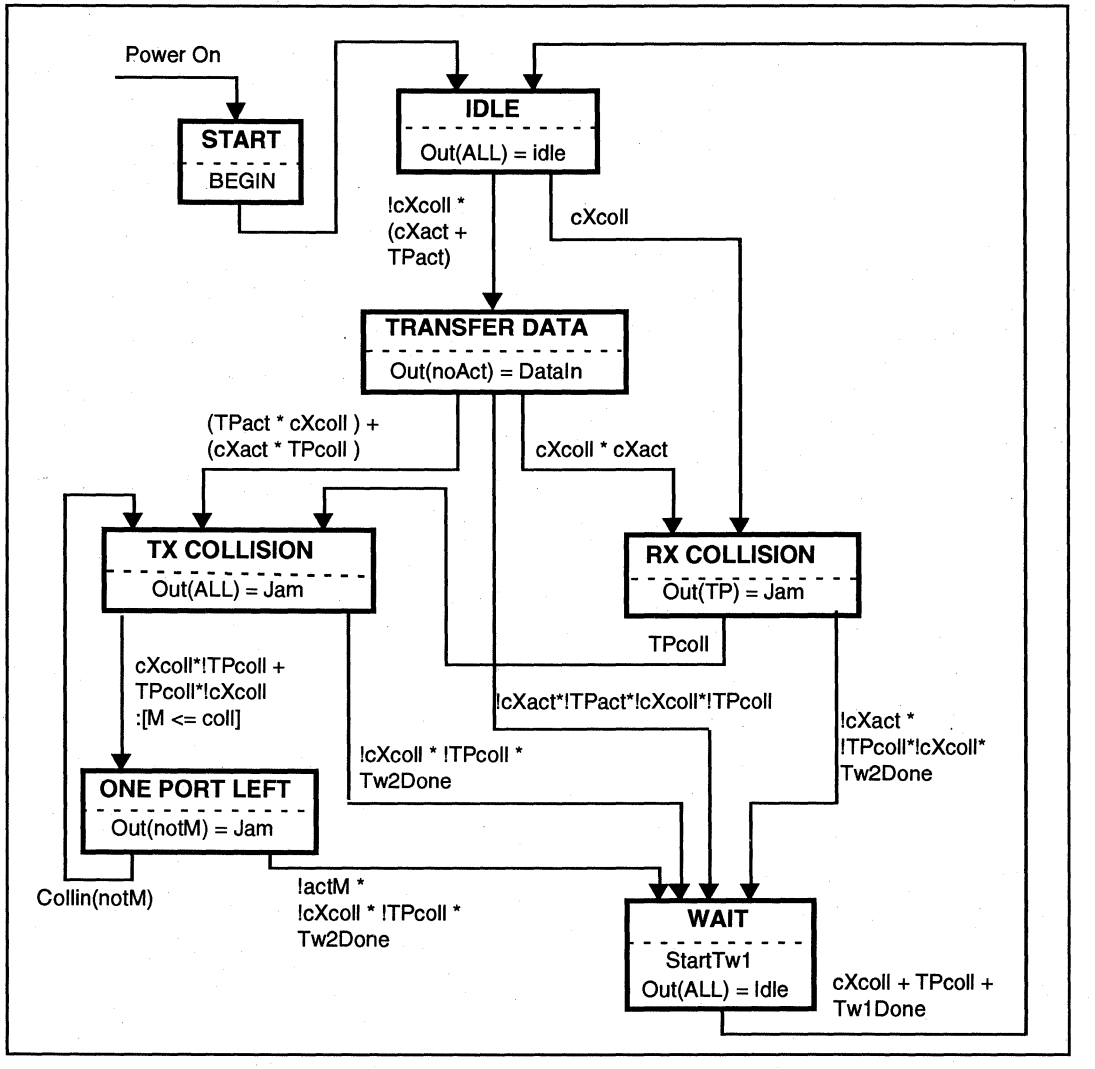
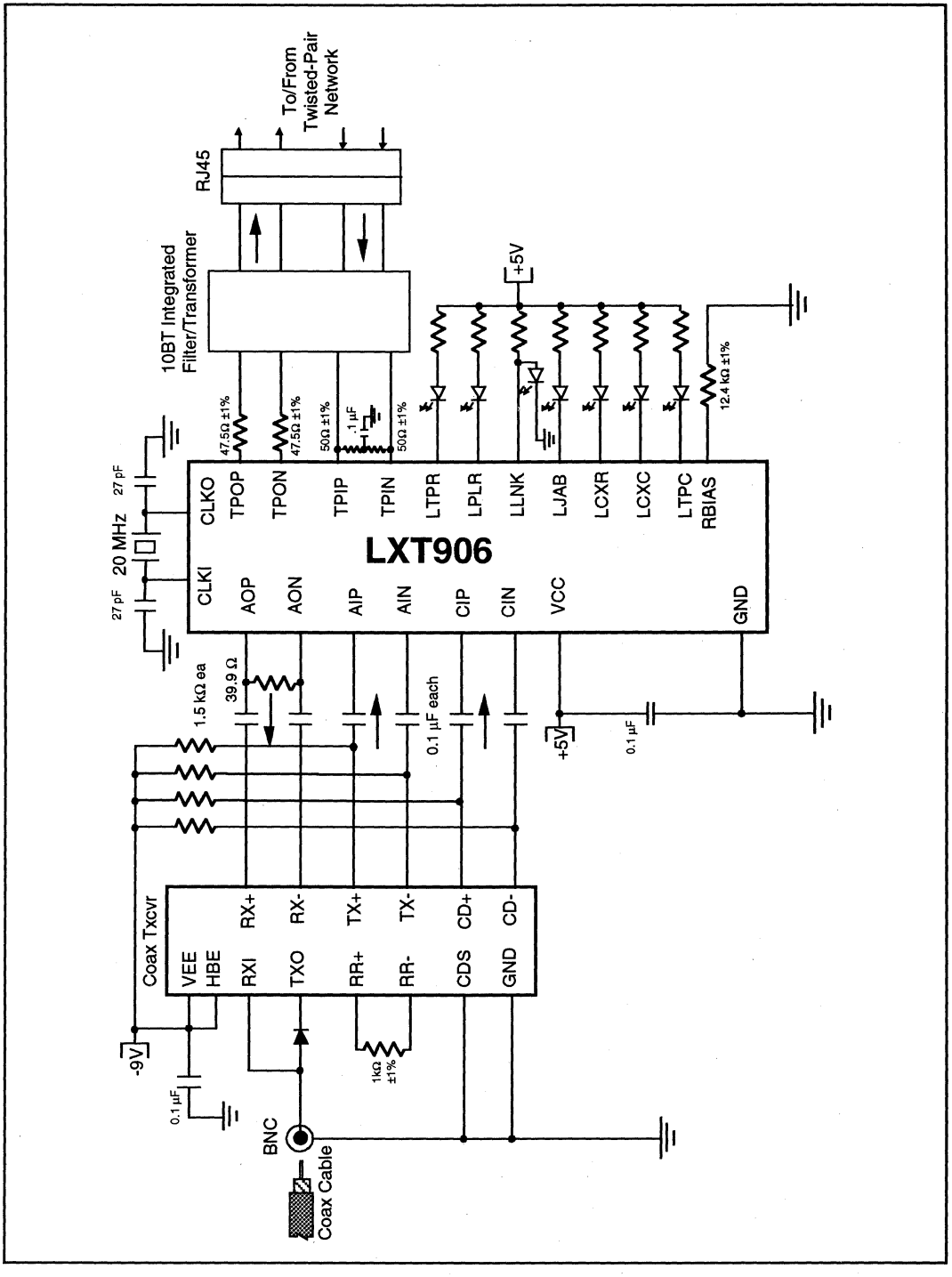


Figure 5: Typical TP to Coax Adapter Application Circuit



NOTES:

Advance Information
December 1993

LXT907

Ethernet Interface for Hub, Switch and Adapter Applications (Internal MAU) with Integrated 10Base T MAU, EnDec, AUI and Filters

General Description

The LXT907 Hub/Switch/Repeater Ethernet Interface is designed for IEEE 802.3 physical layer applications. It provides, in a single CMOS device, all the active circuitry for interfacing most standard 802.3 controllers to either the 10Base-T media or Attachment Unit Interface (AUI).

LXT907 functions include Manchester encoding/decoding, receiver squelch and transmit pulse shaping, jabber, link testing and reversed polarity detection/correction. The LXT907 can be used to drive either the AUI drop cable or the 10Base-T twisted-pair cable with only a simple isolation transformer. No external filters are required. The LXT907 can be used with both standard (10 Mbps) and full-duplex (20 Mbps) Ethernet controllers.

The LXT907 is fabricated with an advanced CMOS process and requires only a single 5-volt power supply.

Applications

- Hub/Switches for dedicated LAN connections
- Computer/workstation 10Base-T LAN adapter boards

Key Features

Functional Features

- Integrated Filters - No External Filters Required
- Integrated Manchester Encoder/Decoder
- 10Base-T compliant Transceiver
- AUI Transceiver
- Full Duplex Capable (20 Mbps)

Convenience Features

- Automatic/Manual AUI/RJ45 Selection
- Automatic Polarity Correction
- SQE Disable/Enable function
- Power Down Mode
- Four loopback modes for better testing

Diagnostic Features

- Four LED Drivers
- AUI/RJ45 Loopback
- Remote Signaling of Link Down and Jabber conditions

3

Figure 1: LXT907 Block Diagram

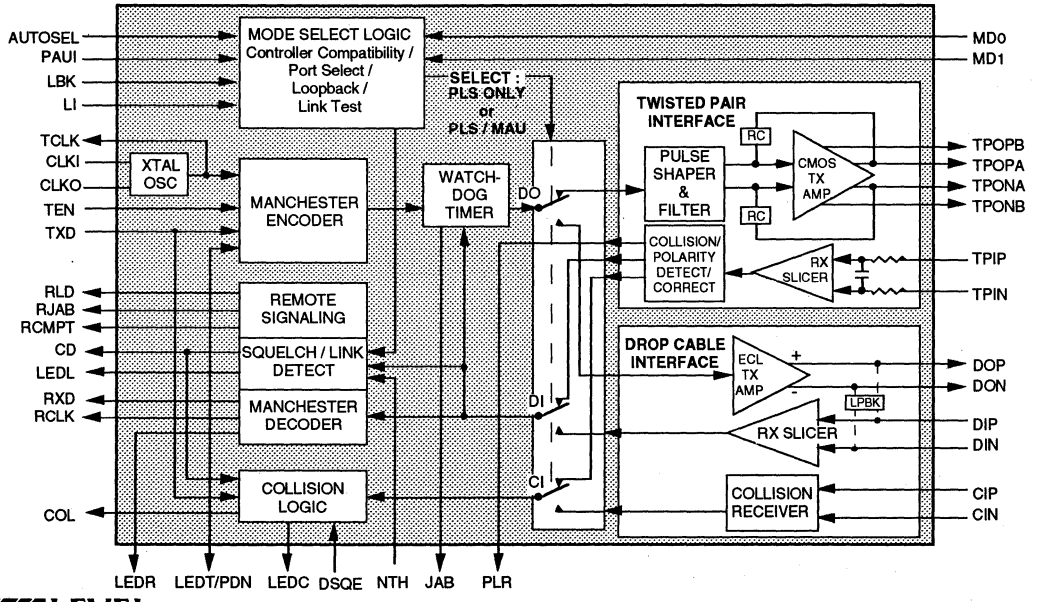


Table 1: Controller Compatibility Mode Options

Controller Mode:	Setting: MD1	MD0
Mode 1 - For Advanced Micro Devices AM7990 or compatible controllers	0	0
Mode 2 - For Intel 82586, 82596 or compatible controllers	0	1
Mode 3 - For Fujitsu MB86950, MB86960 or compatible continuous clock type controllers (Seeq 8005)	1	0
Mode 4 - For National Semiconductor 8390 or compatible controllers (TI TMS380C26)	1	1

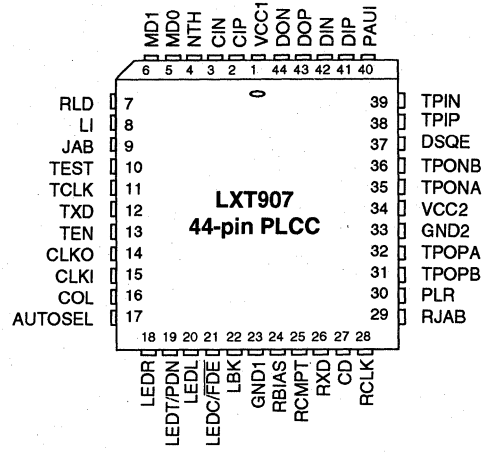


Table 2: Pin Descriptions

Pin #	Sym	I/O	Name	Description
1 34	VCC 1 VCC 2	I I	Power Inputs 1 and 2	+ 5 volt power supply inputs.
2 3	CIP CIN	I I	AUI Collision Pair	Differential input pair connected to the AUI transceiver CI circuit. The input is collision signaling or SQE.
4	NTH	I	Normal Threshold	When NTH = 1, the normal TP squelch threshold is enabled. When NTH = 0, the normal TP squelch threshold is reduced by 4.5 dB.
5 6	MD0 MD1	I I	Mode Select 0 Mode Select 1	Mode select pins determine controller compatibility mode in accordance with Table 1, above.
7	RLD	O	Remote Link Down	Output goes high to signal to the controller that the remote port is in link down condition.
8	LI	I	Link Test Enable	Controls Link Integrity Test; enabled when LI = 1, disabled when LI = 0.
9	JAB	O	Jabber Indicator	Output goes high to indicate Jabber state.
10	TEST	I	Test	Open.
11	TCLK	O	Transmit Clock	A 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller.
12	TXD	I	Transmit Data	Input signal containing NRZ data to be transmitted on the network. TXD is connected directly to the transmit data output of the controller.
13	TEN	I	Transmit Enable	Enables data transmission and starts the watchdog timer. Synchronous to TCLK (see Figures 4, 10, 16 and 22 for details).
14 15	CLKO CLKI	O I	Crystal Oscillator	A 20 MHz crystal (Mtron MP-1/MP-2) must be connected across these pins, or a 20 MHz clock applied at CLKI with CLKO left open.
16	COL	O	Collision Detect	Output which drives the collision detect input of the controller.

Table 2: Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
17	AUTO SEL	I	Automatic Port Select	When AUTOSEL = 1, automatic port selection is enabled (the LXT907 defaults to the AUI port only if TP link integrity = Fail). When AUTOSEL = 0, manual port selection is enabled (the PAUI pin determines the active port).
18	LEDR	O	Receive LED	Open drain driver for the receive indicator LED. Output is pulled low during receive, except when data is being looped back to DIN/DIP from a remote transceiver (external MAU). LED "On" (i.e., low output) time is extended by approximately 100 ms.
19	LEDT/ PDN	O I	Transmit LED/ Power Down	Open drain driver for the transmit indicator LED. Output is pulled low during transmit. LED "On" (i.e., low output) time is extended by approximately 100 ms. If externally tied low, the LXT907 goes to power down state.
20	LEDL	O	Link LED	Open drain driver for link integrity indicator LED. Output is pulled low during link test pass. If externally tied low, internal circuitry is forced to "Link Pass" state and LXT907 will continue to transmit link test pulses.
21	LEDC/ $\overline{\text{FDE}}$	O	Collision LED/ Full Duplex Enable	Open drain driver for the collision indicator LED pulls low during collision. LED "On" (i.e., low output) time is extended by approximately 100 ms. If externally tied low, the LXT907 enables full duplex operation by disabling the internal TP loopback and collision detection circuits in anticipation of external TP loopback or full duplex operation.
22	LBK	I	Loopback	Enables internal loopback mode. See Figure 7 (Mode 1), Figure 13 (Mode 2), Figure 19 (Mode 3) and Figure 25 (Mode 4) for details.
23 33	GND1 GND2	– –	Ground Returns 1 and 2	Grounds.
24	RBIAS	I	Bias Control	A 12.4 kΩ 1% resistor to ground at this pin controls operating circuit bias.
25	RCMPT	O	Remote Compatibility	Output goes high to signal the controller that the remote port is compatible with the LXT907 remote signaling features.
26	RXD	O	Receive Data	Output signal connected directly to the receive data input of the controller.
27	CD	O	Carrier Detect	An output to notify the controller of activity on the network.
28	RCLK	O	Receive Clock	A recovered 10 MHz clock which is synchronous to the received data and connected to the controller receive clock input.
29	RJAB	O	Remote Jabber	Output goes high to indicate that the remote port is in Jabber condition.
30	PLR	O	Polarity Reverse	Output goes high to indicate reversed polarity at the TP input.
31 36 32 35	TPOPB TPONB TPOPA TPONA	O O O O	Twisted-Pair Transmit Pairs A & B	Two differential driver pair outputs (A and B) to the twisted-pair cable. The outputs are pre-equalized; no external filters are required. Two pairs must be shorted together with 24.9 Ω 1% resistors to match impedance of 100Ω UTP.

Table 2: Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
37	DSQE	I	Disable SQE	When DSQE = 1, the SQE function is disabled. When DSQE = 0, the SQE function is enabled. SQE must be disabled for normal operation in Hub/Switch/Repeater applications.
38 39	TPIP TPIN	I I	Twisted-Pair Receive Pair	A differential input pair from the twisted-pair cable. Receive filter is integrated on-chip. No external filters are required.
40	PAUI	I	Port/AUI Select	In Manual Port Select mode (AUTOSEL = 0), PAUI selects the active port. When PAUI = 1, the AUI port is selected. When PAUI = 0, the TP port is selected. In Auto Port Select mode, PAUI must be tied to ground.
41 42	DIP DIN	I I	AUI Receive Pair	Differential input pair from the AUI transceiver DI circuit. The input is Manchester encoded.
43 44	DOP DON	O O	AUI Transmit Pair	A differential output driver pair for the AUI transceiver cable. The output is Manchester encoded.

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- Supply Voltage V_{CC} - 0.3 V (min) to + 6 V (max)
- Operating temperature T_{OP} 0 °C (min) to +70 °C (max)
- Storage temperature T_{ST} -65 °C (min) to +150 °C (max)

Table 3: Operating Conditions (Voltage with respect to ground unless otherwise specified.)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Recommended supply voltage		V_{CC}	4.75	5.0	5.25	V	
Recommended operating temperature		T_{OP}	0	-	70	°C	
Supply current		I_{CC}	–	65	85	mA	Idle mode
	Normal mode	I_{CC}	–	90	110	mA	Transmitting on TP
		I_{CC}	–	70	90	mA	Transmitting on AUI
	Power Down mode	I_{CC}	–	0.75	2	mA	

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 4: I/O Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input low voltage [2]		V_{IL}	–	–	0.8	V	
Input high voltage [2]		V_{IH}	2.0	–	–	V	
Output low voltage		V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
Output low voltage		V_{OL}	–	–	10	% V_{CC}	I_{OL} < 10 µA
Output low voltage (Open drain LED Driver)		V_{OL}	–	–	0.7	V	I_{OL} = 10 mA
Output high voltage		V_{OH}	2.4	–	–	V	I_{OH} = 40 µA
Output high voltage		V_{OH}	90	–	–	% V_{CC}	I_{OH} < 10 µA
Output rise time	CMOS	_	–	3	12	ns	C_{LOAD} = 20 pF
TCLK & RCLK	TTL	–	–	2	8	ns	
Output fall time	CMOS	–	–	3	12	ns	C_{LOAD} = 20 pF
TCLK & RCLK	TTL	–	–	2	8	ns	
CLKI rise time (externally driven) [2]		–	–	–	10	ns	
CLKI duty cycle (externally driven) [2]		–	–	50/50	40/60	%	

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Limited functional test patterns are performed under these input conditions. The majority of functional tests are performed at levels of 0V and 3V. This applies to all inputs except TPIP, TPIN, DIP, DIN, CIP and CIN.

Table 5: AUI Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input low current	I_{IL}	–	–	-700	µA	
Input high current	I_{IH}	–	–	500	µA	
Differential output voltage	V_{OD}	± 550	–	± 1200	mV	
Differential squelch threshold	V_{DS}	150	220	350	mV	5 MHz square wave input

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 6: TP Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	Z_{OUT}	–	5	–	Ω	
Peak differential output voltage	V_{OD}	3.3	3.5	3.7	V	Load = 100 Ω at TPOP and TPON
Transmit timing jitter addition [2]	–	–	± 6.4	± 10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections [2,3]	–	–	± 3.5	± 5.5	ns	After line model specified by IEEE 802.3 for 10Base-T internal MAU
Receive input impedance	Z_{IN}	–	20	–	kΩ	Between TPIP/TPIN, CIP/CIN & DIP/DIN
Differential squelch threshold						
- Normal (NTH = 1)	V_{DS}	300	420	585	mV	5 MHz square wave input
- Reduced (NTH = 0)	V_{DSL}	180	250	345	mV	5 MHz square wave input

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Parameter is guaranteed by design; not subject to production testing.
[3] IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Functional Description

The LXT907 Universal Ethernet Interface Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. It functions as a PLS-Only device (for use with 10Base-2 or 10Base-5 coaxial cable networks) or as an Integrated PLS/MAU (for use with 10Base-T twisted-pair networks).

The LXT907 interfaces a back end controller to either an AUI drop cable or a twisted-pair (TP) cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The AUI interface comprises three circuits: Data Output (DO), Data Input (DI) and Collision (CI). The twisted-pair interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to the three basic interfaces, the LXT907 contains an internal crystal oscillator and four LED drivers for visual status reporting.

Functions are defined from the back end controller side of the interface. The LXT907 Transmit function refers to data transmitted by the back end to the AUI cable (PLS-Only mode) or to the twisted-pair network (Integrated PLS/MAU mode). The LXT907 Receive function refers to data received by the back end from the AUI cable (PLS-Only) or from the twisted-pair network (Integrated PLS/MAU mode). In the integrated PLS/MAU mode, the LXT907 performs all required MAU functions defined by the IEEE 802.3 10Base–T specification such as collision detection, link integrity testing, signal quality error messaging, jabber control and loopback. In the PLS-Only mode, the LXT907 receives incoming signals from the AUI DI circuit with ± 18 ns of jitter and drives the AUI DO circuit.

Controller Compatibility Modes

The LXT907 is compatible with most industry standard controllers including devices produced by Advanced Micro Devices (AMD), Intel, Fujitsu, National Semiconductor, Seeq and Texas Instruments. Four different control signal timing and polarity schemes (Modes 1 through 4) are required to achieve this compatibility. Mode select pins (MD0 and MD1) determine Controller compatibility modes as listed in Table 1.

A complete set of timing diagrams is provided for each mode as follows:
Mode 1 : Figures 2 - 7,
Mode 2 : Figures 8 - 13,
Mode 3 : Figures 14 - 19,
Mode 4 : Figures 20 - 25.
Related timing specifications are provided in Table 8 (RCLK/Start-of-Frame), Table 9 (RCLK/End-of-Frame), Table 10 (Transmit Timing) and Table 11 (Collision Detection, COL/CI Output and Loopback Timing).

Table 7: Switching Characteristics (Ta = 0 to 70 °C, V_{cc} = 5V ±5%)

Parameter	Symbol	Min	Typ	Max	Units
Jabber Timing:					
Maximum transmit time	–	20	–	150	ms
Unjab time	–	250	–	750	ms
Link Integrity Timing:					
Time link loss	–	65	–	66	ms
Time between Link Integrity Pulses	–	8	–	24	ms
Interval for valid receive Link Integrity Pulses	–	4.1	–	65	ms

Table 8: RCLK/Start-of-Frame Timing

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Decoder acquisition time	AUI	t_{DATA}	–	900	1100	ns
	TP	t_{DATA}	–	1300	1500	ns
CD turn-on delay	AUI	t_{CD}	–	50	200	ns
	TP	t_{CD}	–	400	550	ns
Receive data setup	Mode 1	t_{RDS}	43	70	–	ns
from RCLK	Modes 2, 3 and 4	t_{RDS}	30	45	–	ns
Receive data hold	Mode 1	t_{RDH}	10	20	–	ns
from RCLK	Modes 2, 3 and 4	t_{RDH}	30	45	–	ns
RCLK shut off delay from CD assert (Mode 3)		t_{SWS}	–	± 100	–	ns

Table 9: RCLK/End-of-Frame Timing

Parameter	Type	Symbol	Mode 1	Mode 2	Mode 3	Mode 4	Units
RCLK hold after CD off	Min	t_{RCH}	5	1	–	5	bt
Rcv data throughput delay	Max	t_{RD}	400	375	375	375	ns
CD turn off delay [2]	Max	t_{CDOFF}	500	475	475	475	ns
Receive block out after TEN off	Typ [1]	t_{IFG}	5	50	–	–	bt
RCLK switching delay after CD off	Typ [1]	t_{SWE}	–	–	120 (±80)	–	ns

Table 10: Transmit Timing

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
TEN setup from TCLK	t_{EHCH}	22	–	–	ns
TXD setup from TCLK	t_{DSCH}	22	–	–	ns
TEN hold after TCLK	t_{CHEL}	5	–	–	ns
TXD hold after TCLK	t_{CHDU}	5	–	–	ns
Transmit start-up delay - AUI	t_{STUD}	–	200	450	ns
Transmit start-up delay - TP	t_{STUD}	–	350	450	ns
Transmit through-put delay - AUI	t_{TPD}	–	–	300	ns
Transmit through-put delay - TP	t_{TPD}	–	338	350	ns

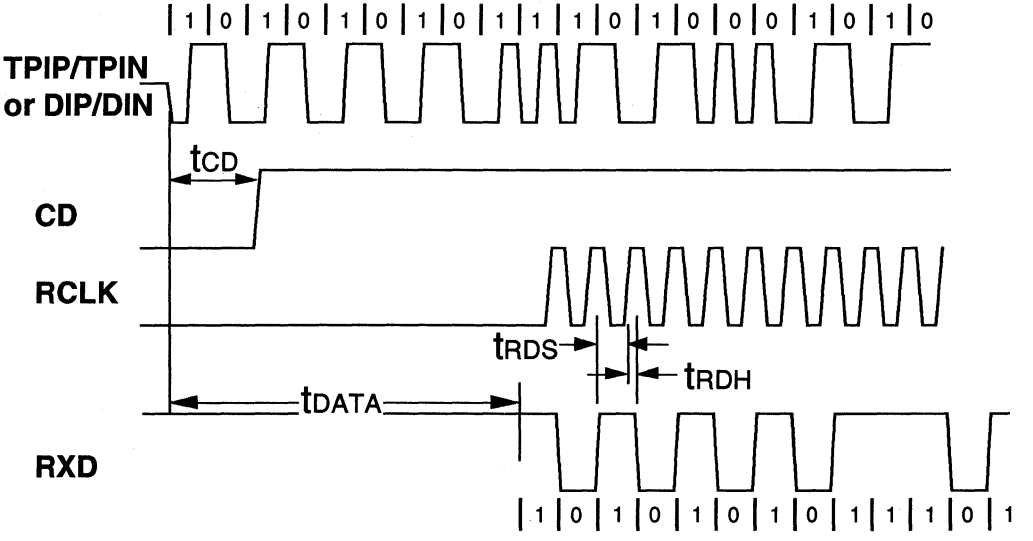
Table 11: Collision Detection, COL/CI Output and Loopback Timing

Parameter	Symbol	Minimum	Typical [1]	Maximum	Units
COL turn on delay	t_{COLD}	–	–	500	ns
COL turn off delay	t_{COLOFF}	–	–	500	ns
COL (SQE) Delay after TEN off [3]	t_{SQED}	0.65	–	1.6	µs
COL (SQE) Pulse Duration [3]	t_{SQEP}	500	–	1500	ns
LBK setup from TEN	t_{KHEH}	10	25	–	ns
LBK hold after TEN	t_{KHEL}	10	0	–	ns

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] CD Turnoff delay measured from middle of last bit, so timing specification is unaffected by the value of the last bit.
[3] When SQE is enabled (DSQE = 0).

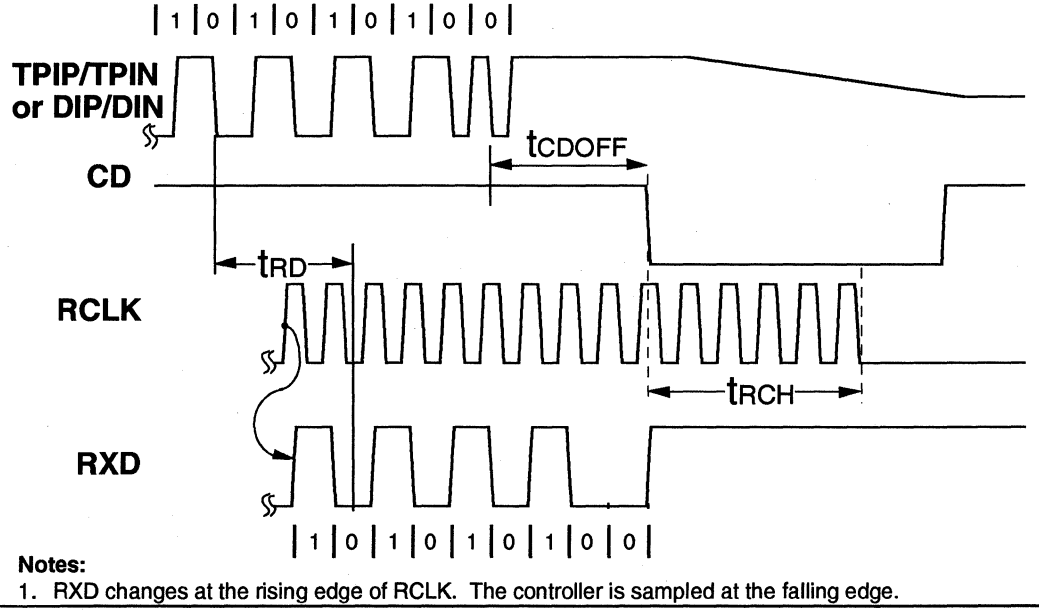
Figures 2 through 7 - Timing Diagrams for Mode 1 (MD1 = 0, MD0 = 0)

Figure 2: Mode 1 RCLK/Start-of-Frame Timing



Notes:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 3: Mode 1 RCLK/End-of-Frame Timing



Notes:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 4: Mode 1 Transmit Timing

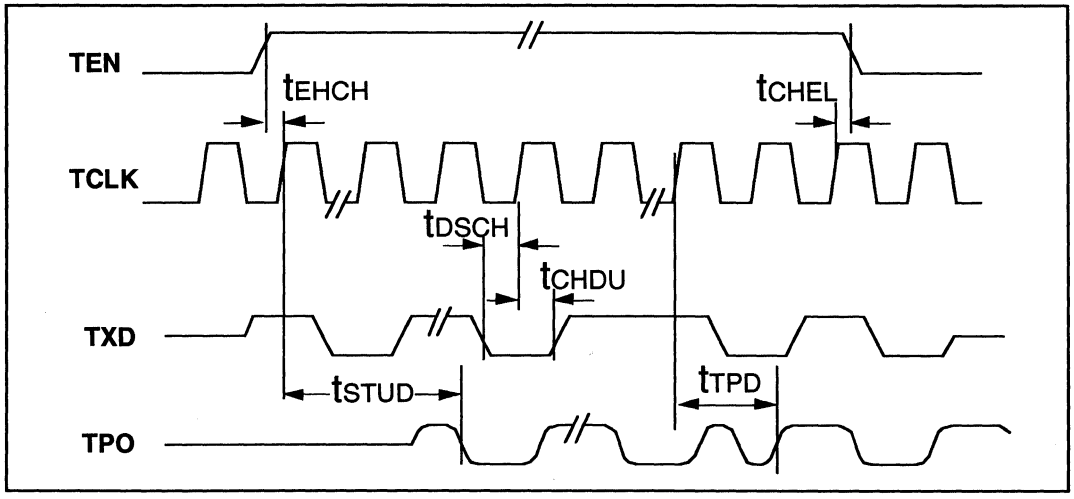


Figure 5: Mode 1 Collision Detect Timing

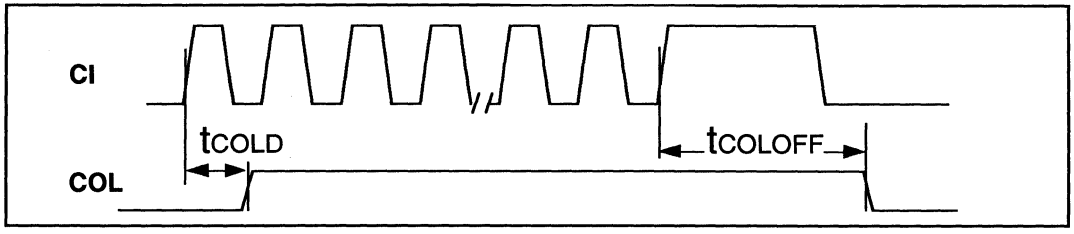
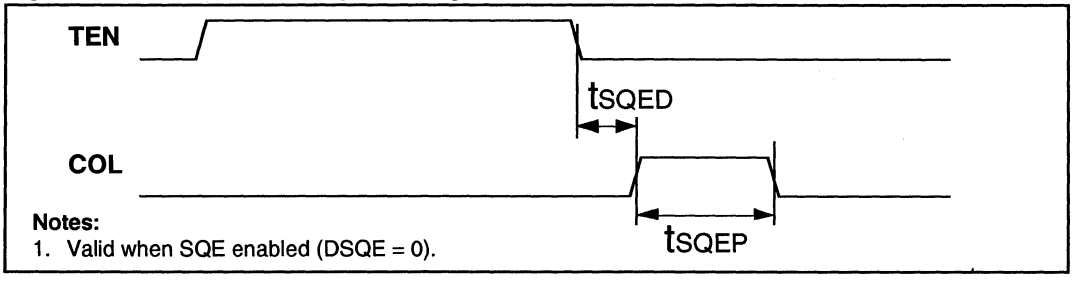
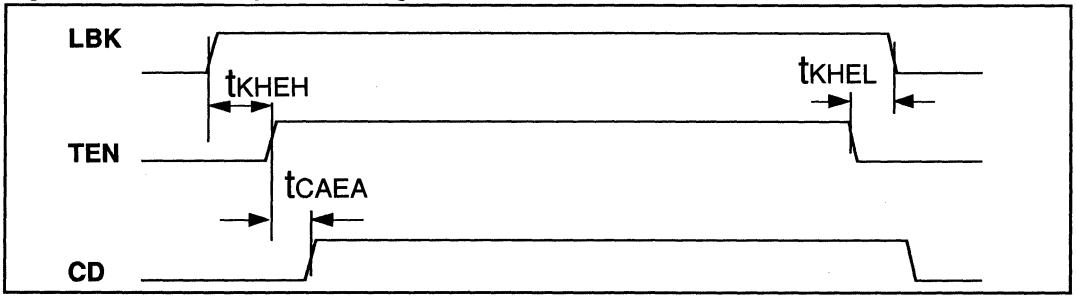


Figure 6: Mode 1 COL/CI Output Timing



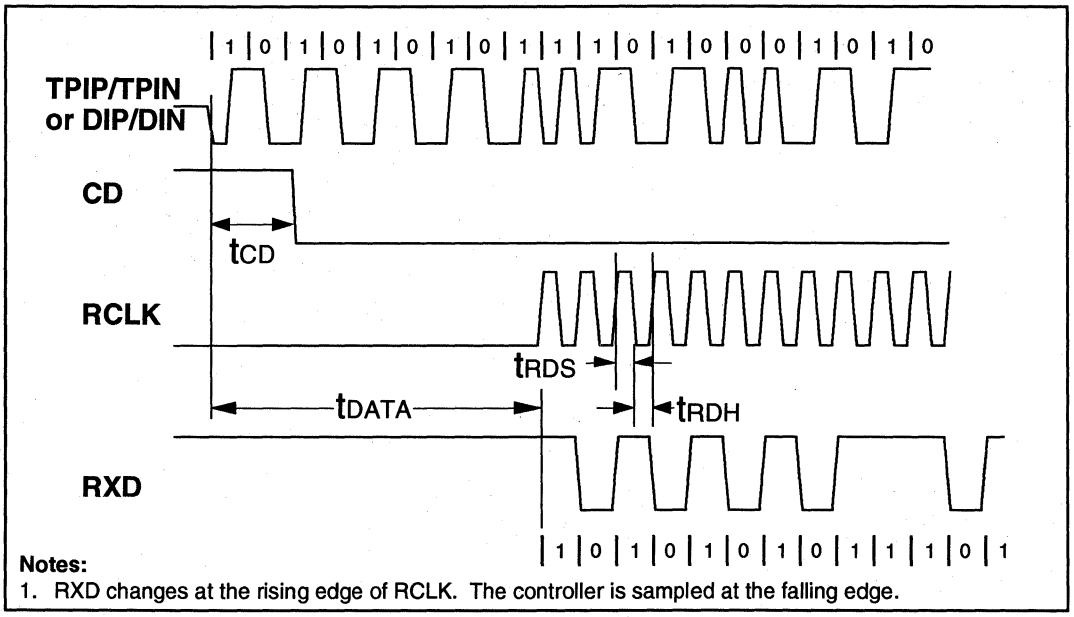
Notes:
1. Valid when SQE enabled (DSQE = 0).

Figure 7: Mode 1 Loopback Timing



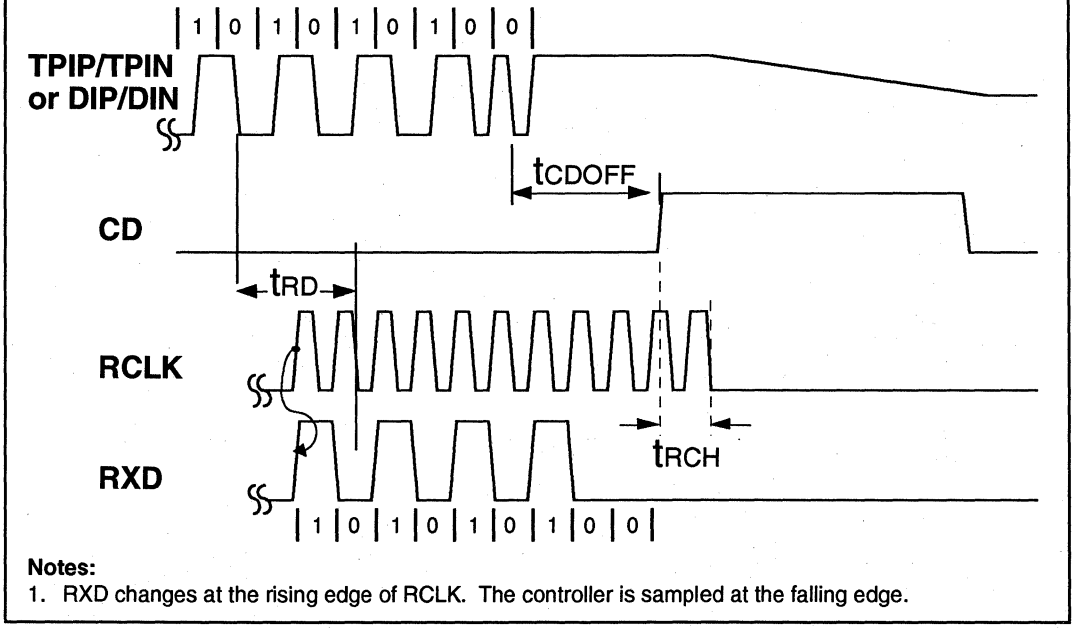
Figures 8 through 13 - Timing Diagrams for Mode 2 (MD1 = 0, MD0 = 1)

Figure 8: Mode 2 RCLK/Start-of-Frame Timing



Notes:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 9: Mode 2 RCLK/End-of-Frame Timing



Notes:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 10: Mode 2 Transmit Timing

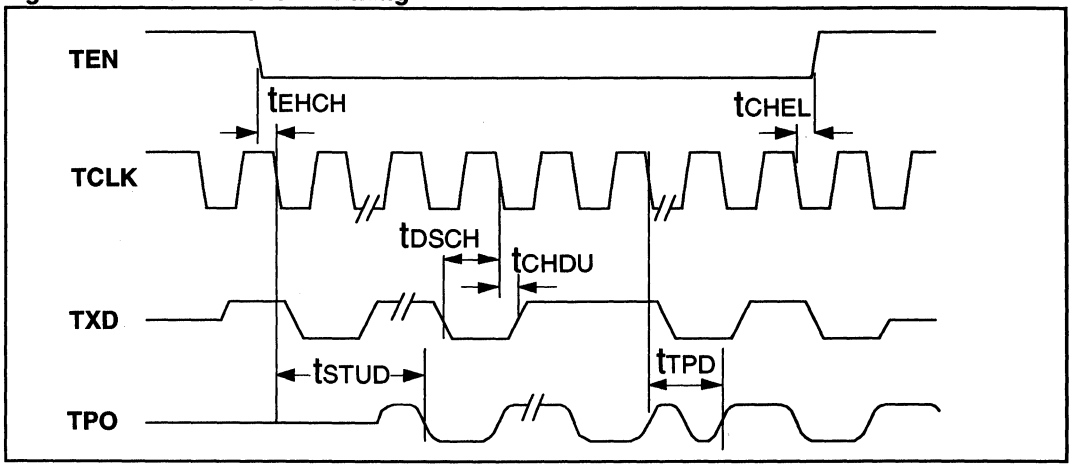


Figure 11: Mode 2 Collision Detect Timing

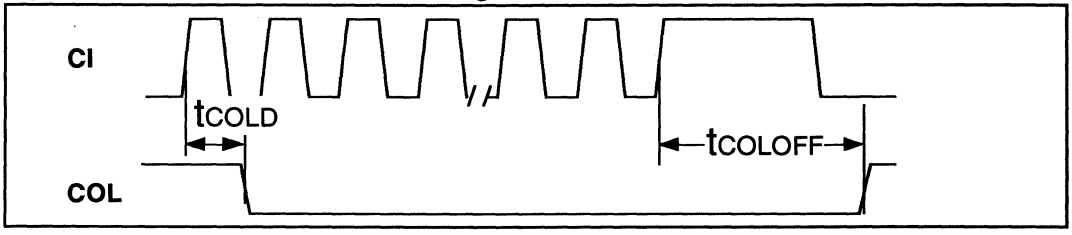
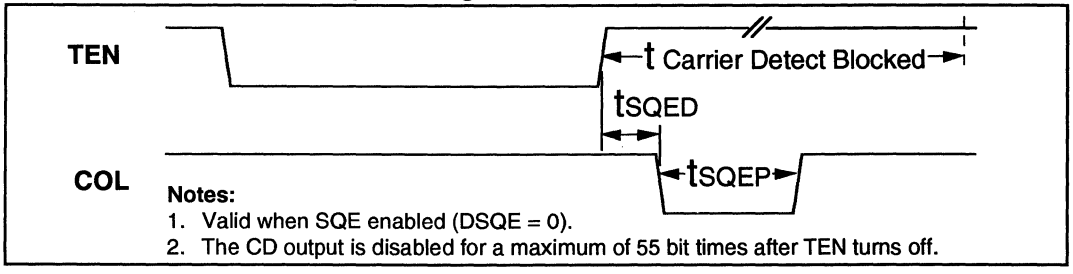
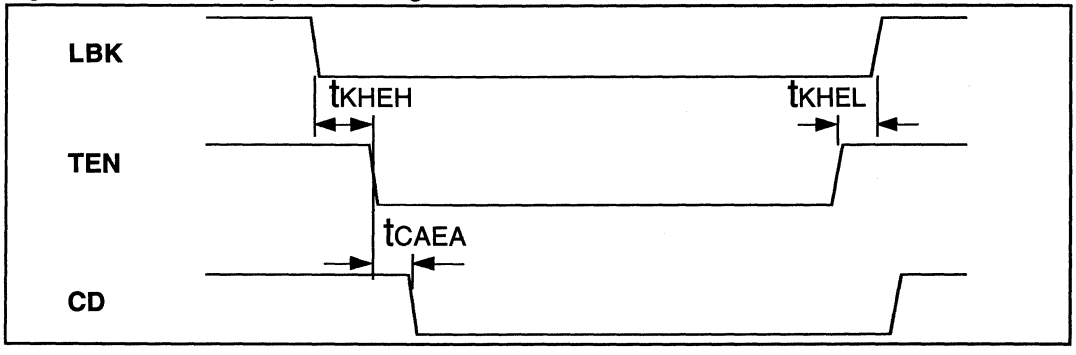


Figure 12: Mode 2 COL/CI Output Timing



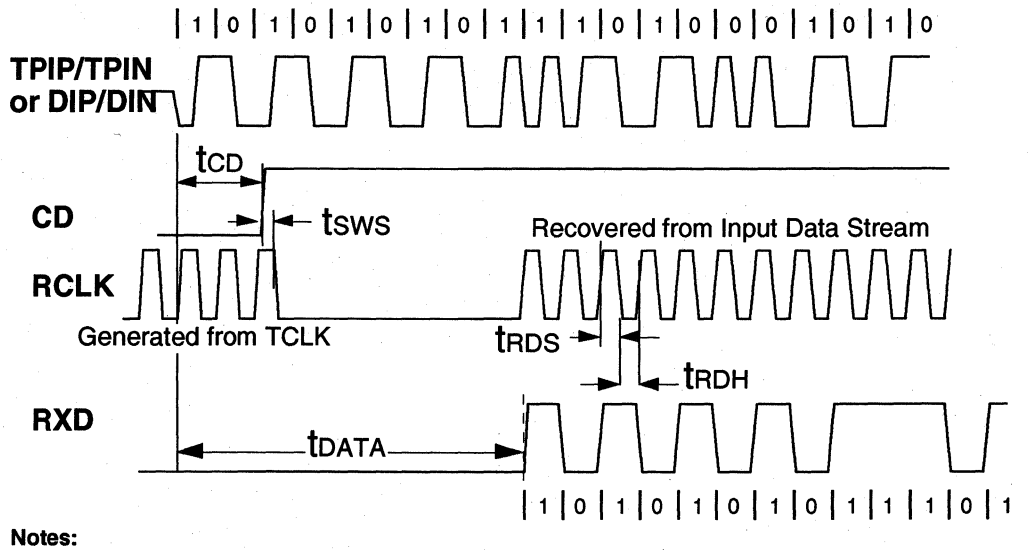
Notes:
1. Valid when SQE enabled (DSQE = 0).
2. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

Figure 13: Mode 2 Loopback Timing



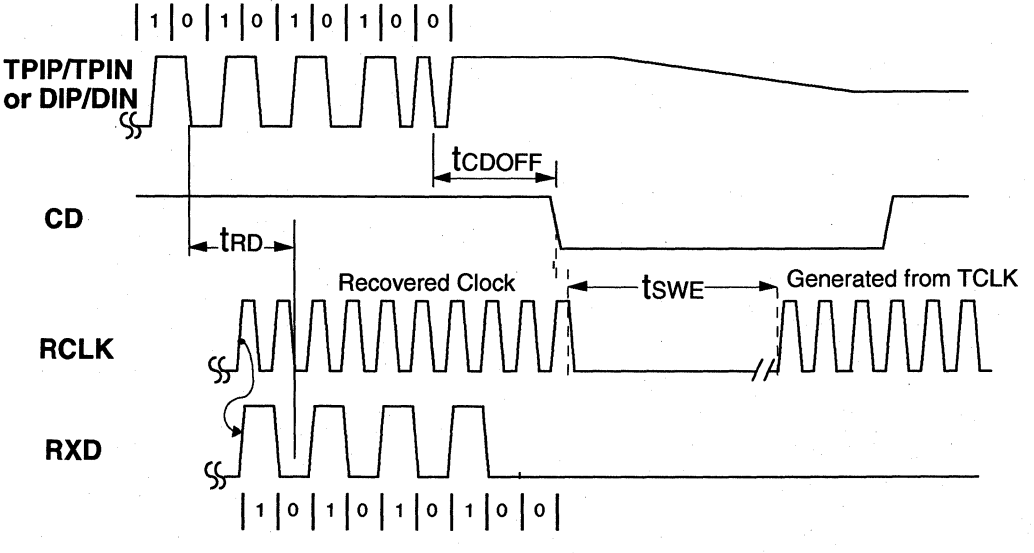
Figures 14 through 19 - Timing Diagrams for Mode 3 (MD1 = 1, MD0 = 0)

Figure 14: Mode 3 RCLK/Start-of-Frame Timing



Notes:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 15: Mode 3 RCLK/End-of-Frame Timing



Notes:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 16: Mode 3 Transmit Timing

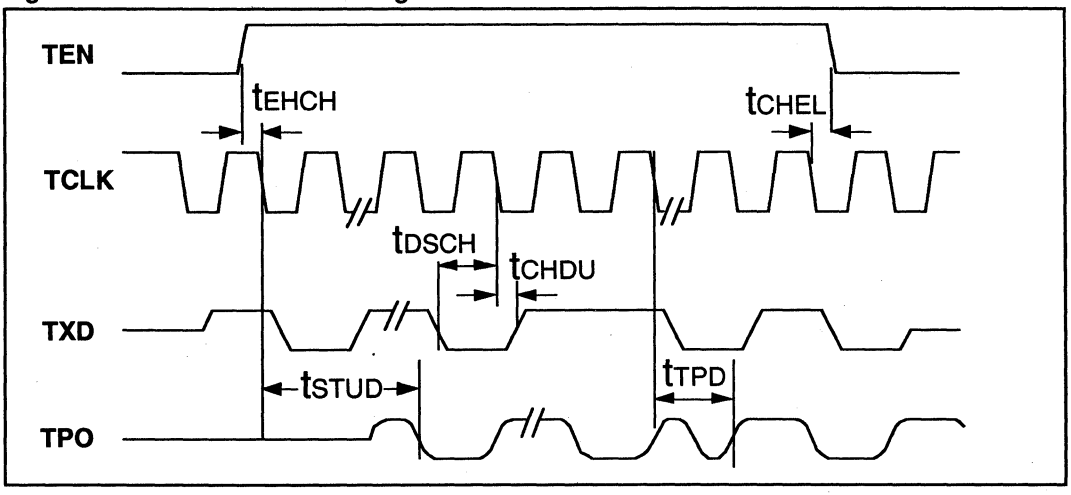


Figure 17: Mode 3 Collision Detect Timing

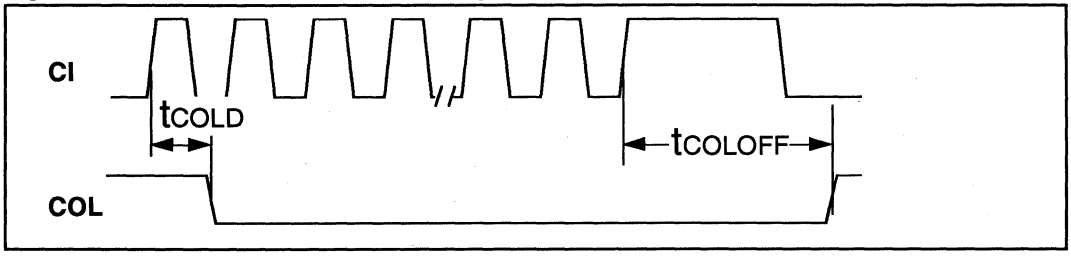
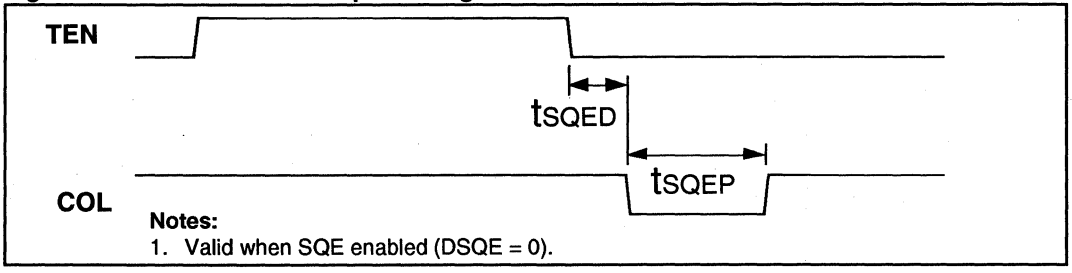
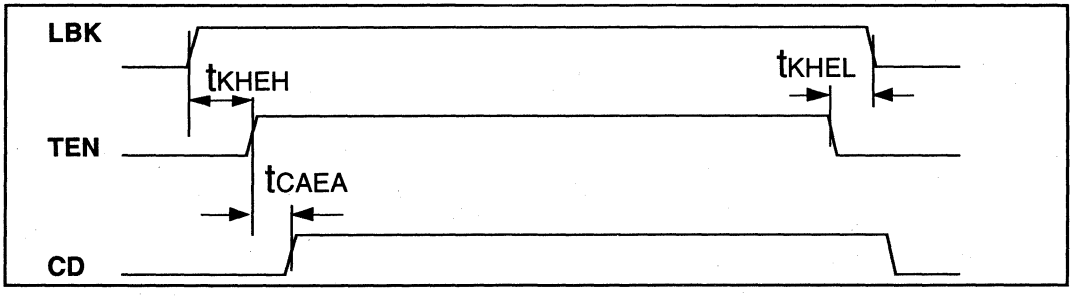


Figure 18: Mode 3 COL/CI Output Timing



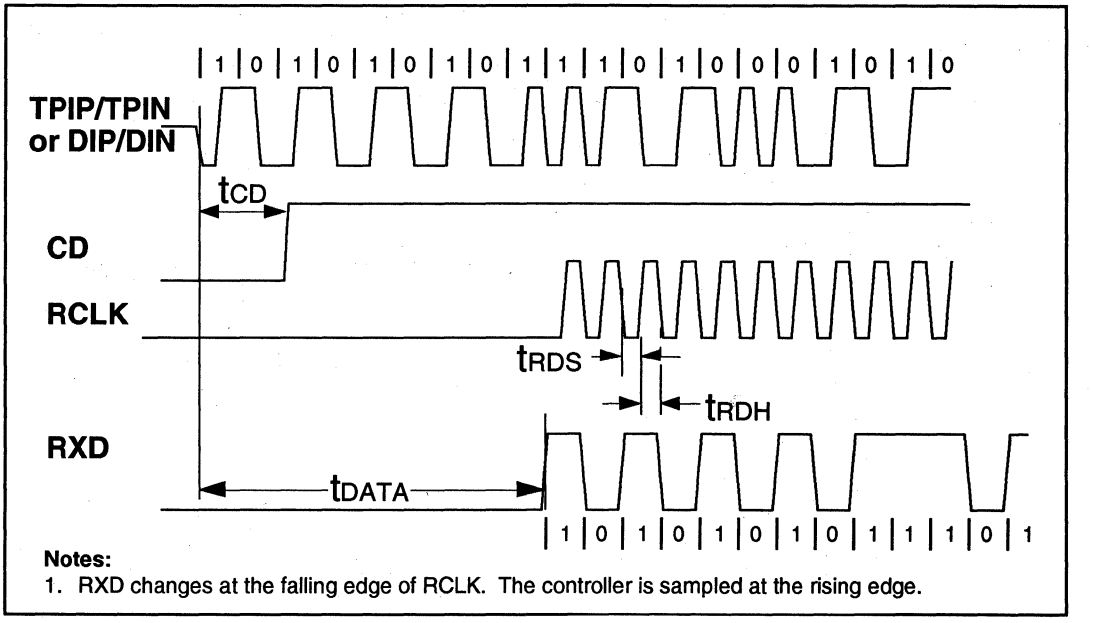
Notes:
1. Valid when SQE enabled (DSQE = 0).

Figure 19: Mode 3 Loopback Timing



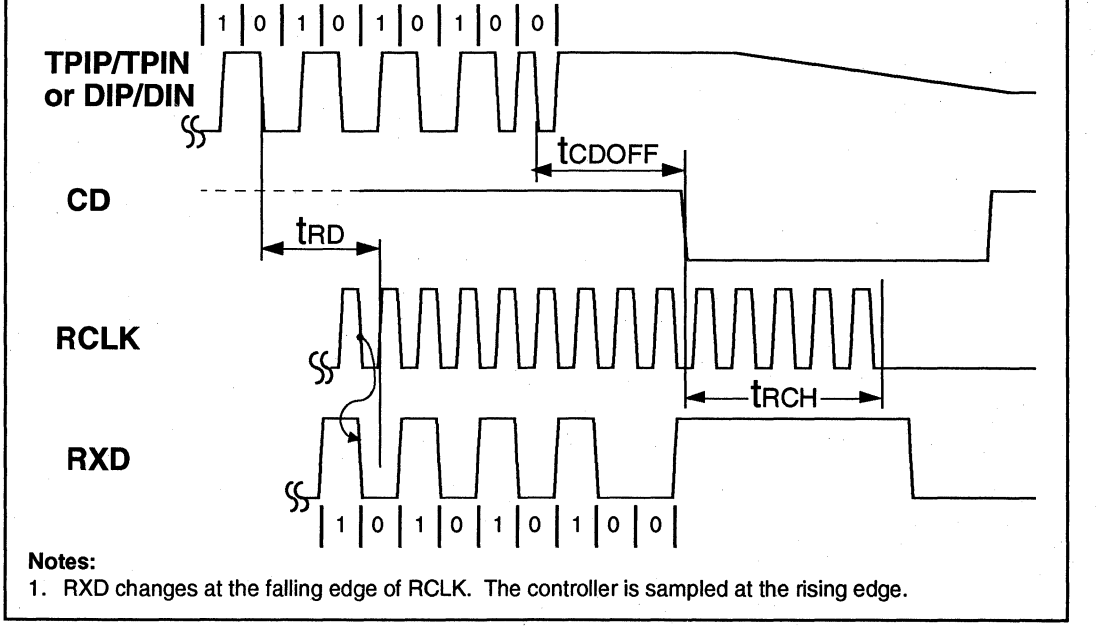
Figures 20 through 25 - Timing Diagrams for Mode 4 (MD1 = 1, MD0 = 1)

Figure 20: Mode 4 RCLK/Start-of-Frame Timing



Notes:
1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 21: Mode 4 RCLK/End-of-Frame Timing



Notes:
1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 22: Mode 4 Transmit Timing

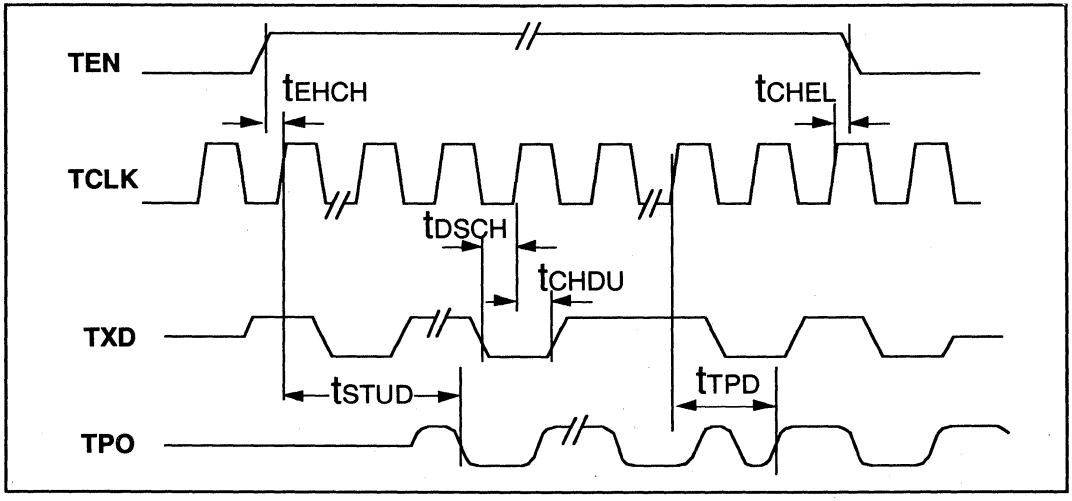


Figure 23: Mode 4 Collision Detect Timing

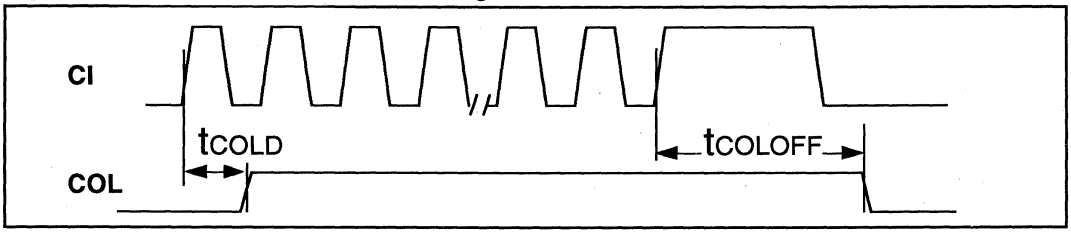
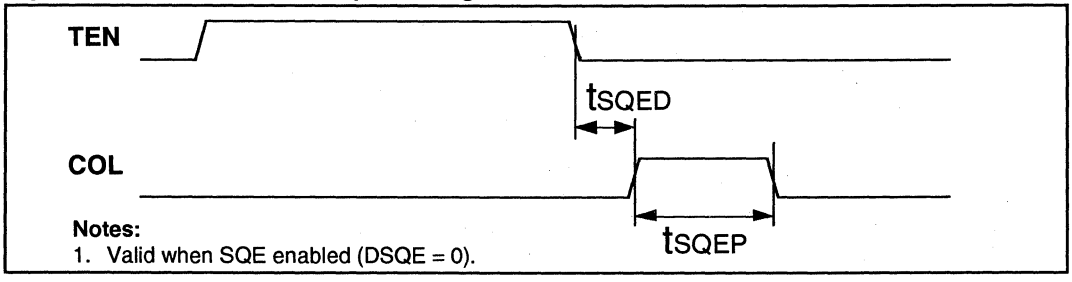
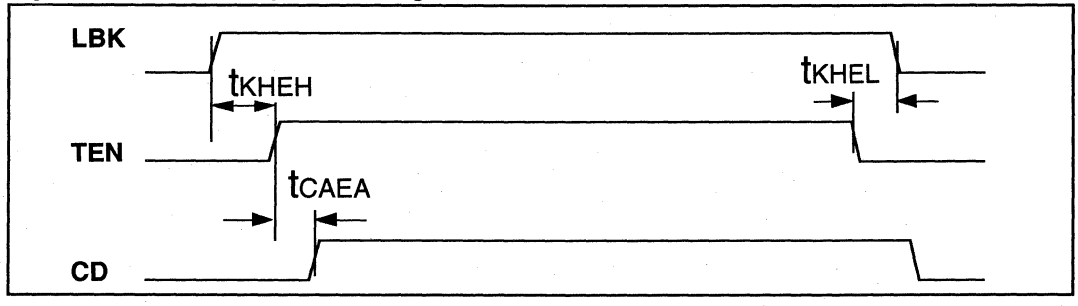


Figure 24: Mode 4 COL/CI Output Timing



Notes:
1. Valid when SQE enabled (DSQE = 0).

Figure 25: Mode 4 Loopback Timing



Transmit Function

The LXT907 receives NRZ data from the controller at the TXD input as shown in Figure 1, and passes it through a Manchester encoder. The encoded data is then transferred to either the AUI cable (the DO circuit) or the twisted-pair network (the TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP, shown in Figure 26. The TPO output is pre-distorted and prefiltered to meet the 10 Base-T jitter template. **An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. No external filters are required.** During idle periods, the LXT907 transmits link integrity test pulses on the TPO circuit (if LI is enabled and integrated PLS/MAU mode is selected). External resistors control the termination impedance.

Figure 26: LXT907 TPO Output Waveform

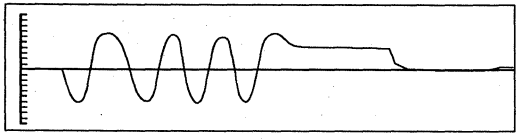
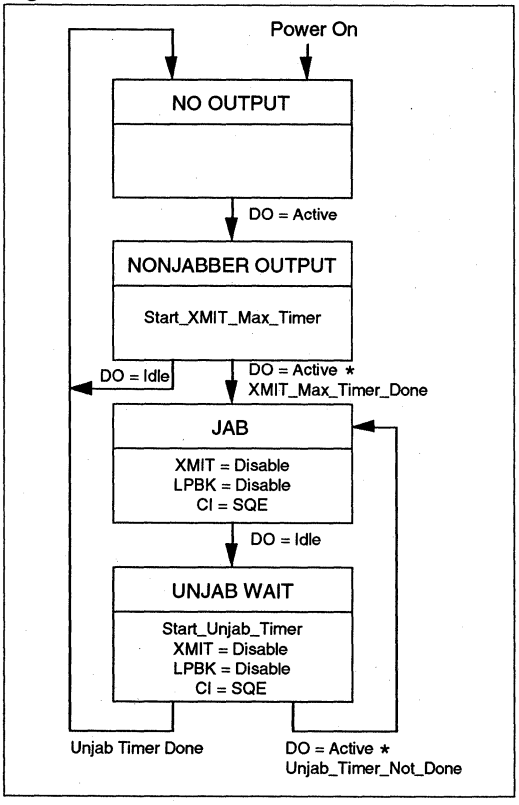


Figure 27: Jabber Control Function



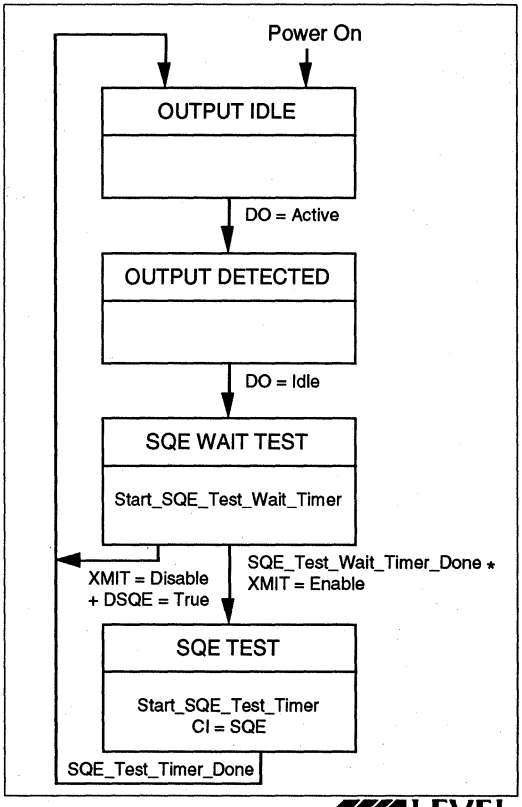
Jabber Control Function

Figure 27 is a state diagram of the LXT907 Jabber control function. The LXT907 on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions, and activates the JAB pin. Once the LXT907 is in the jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it will exit the jabber state.

SQE Function

The LXT907 supports the signal quality error (SQE) function as shown in Figure 28, although the SQE function can be disabled. After every successful transmission on the 10Base-T network when SQE is enabled, the LXT907 transmits the SQE signal for 10BT ± 5BT over the internal CI circuit which is indicated on the COL pin of the device. When using the 10Base 2 port of the LXT907, the SQE function is determined by the external MAU attached. SQE must be disabled for normal operation in hub and switch applications. The SQE function is disabled when DSQE = 1 and enabled when DSQE = 0.

Figure 28: SQE Function



Receive Function

The LXT907 receive function acquires timing and data from the twisted-pair network (the TPI circuit) or from the AUI (the DI circuit). Valid received signals are passed through the on-chip filters and Manchester decoder then output as decoded NRZ data and receive timing on the RXD and RCLK pins, respectively.

An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. **No external filters are required.** The receive function is activated only by valid data streams above the squelch level and with proper timing. If the differential signal at the TPI or the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT907 receive function enters the idle state. If the polarity of the TPI circuit is reversed, LXT907 detects the polarity reverse and reports it via the PLR output. The LXT907 automatically corrects reversed polarity.

Polarity Reverse Function

The LXT907 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is detected when eight consecutive opposite receive link pulses are detected without receipt of one link pulse or frame of the expected polarity. Reversed polarity is also detected if four consecutive frames are received with a reversed start-of-idle.

If the LXT907 enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity Testing is disabled, polarity detection is based only on received data.). Polarity correction is always enabled.

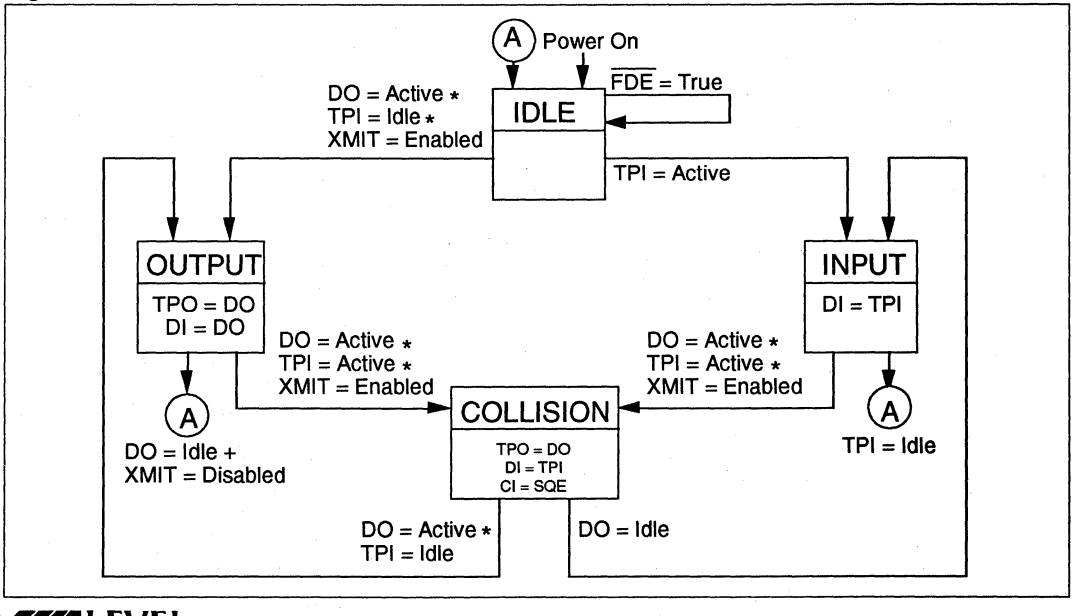
Collision Detection Function

The collision detection function operates on the twisted pair side of the interface. For standard (half-duplex) 10Base T networks, a collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT907 reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 29 is a state diagram of the LXT907 collision detection function. Refer to Table 11 for collision detection and COL/CI output timing. (NOTE: For full-duplex operation, the collision detection circuitry must be disabled.)

Loopback Function

The LXT907 provides the normal loopback function specified by the 10 Base-T standard for the twisted-pair port. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the LXT907 from the TXD pin through the Manchester encoder/decoder to the RXD pin and returned to the back-end. This "normal" loopback function is

Figure 29: Collision Detection Function



disabled when a data collision occurs, clearing the RXD circuit for the TPI data. Normal loopback is also disabled during link fail and jabber states.

The LXT907 also provides three additional loopback functions. An external loopback mode, useful for system-level testing, is controlled by pin 21 (LEDC). When LEDC is tied low, the LXT907 disables the collision detection and internal loopback circuits, to allow external loopback.

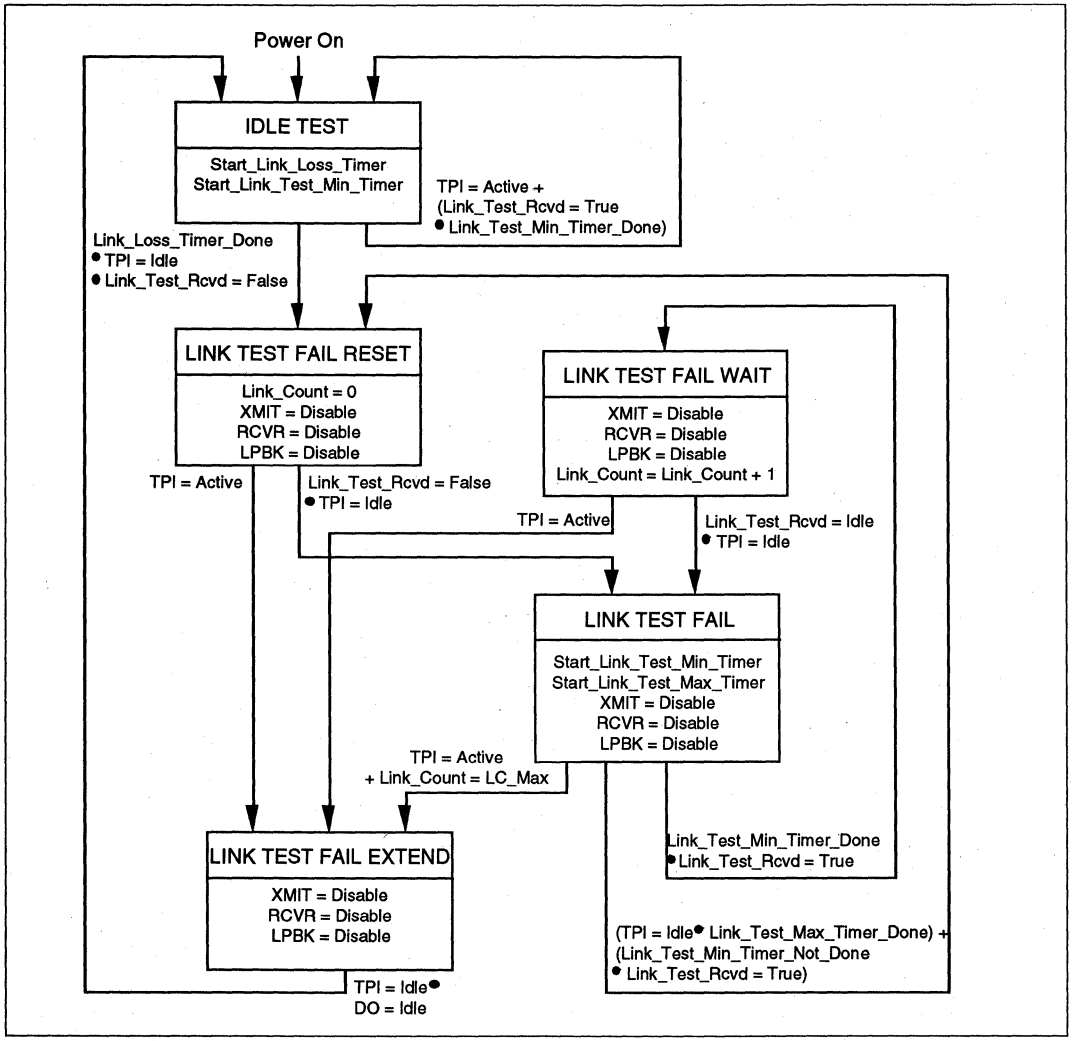
"Forced" TP loopback is controlled by pin 22 (LBK). When the TP port is selected and LBK = 1, TP loopback is "forced", overriding collisions on the TP circuit. When LBK = 0, normal loopback is in effect.

AUI loopback is also controlled by the LBK pin. When the AUI port is selected and LBK = 1, data transmitted by the back-end is internally looped back from the TXD pin through the Manchester encoder/decoder to the RXD pin. When LBK = 0, no AUI loopback occurs.

Link Integrity Test

Figure 30 is a state diagram of the LXT907 Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled when pin 8 (LI) is tied high. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial

Figure 30: Link Integrity Test Function



data stream or link integrity pulses are detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The LXT907 ignores any link integrity pulse with interval less than 2 - 7 ms. The LXT907 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

Remote Signaling

The LXT907 transmits standard link pulses which meet the 10BaseT specification. However, the LXT907 encodes additional status information into the link pulse by varying the link pulse timing. This is referred to as remote signaling. Using alternate pulse intervals, the LXT907 can signal three local conditions: link down, jabber, and remote signaling compatibility. Figure 31 shows the interval variations used to signal local status to the other end of the line. The LXT907 also recognizes these alternate pulse intervals when received from a remote unit. Remote status conditions are reported to the controller over the RLD, RJAB and RCMPT output pins.

Applications

Figures 32 through 38 show typical LXT907 applications.

Auto Port Select with External Loopback Control (Figure 32)

Figure 32 is a typical LXT907 application. The diagram is arranged to group similar pins together; it does not represent the actual LXT907 pinout. The controller interface pins (transmit data, clock and enable; receive data and clock; and the collision detect, carrier detect and loopback control pins) are shown at the top left.

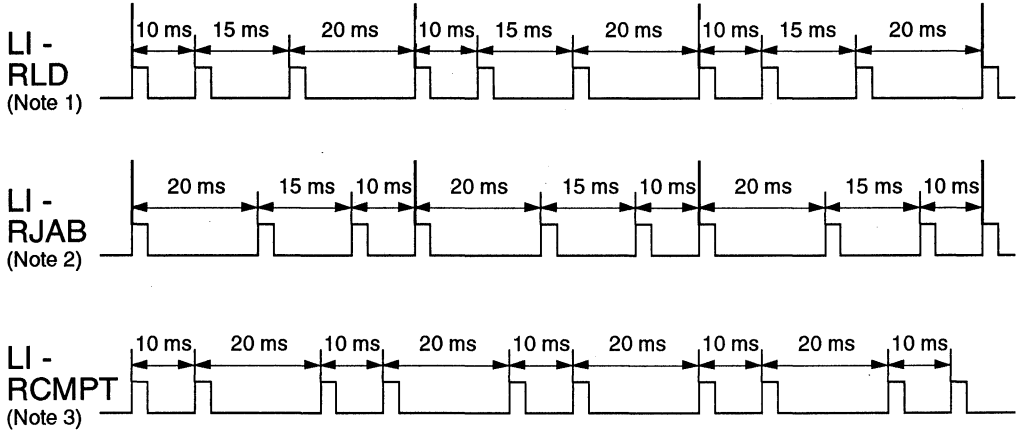
Programmable option pins are grouped center left. The PAUI pin is tied to ground and all other option pins are tied high. This setup selects the following options:

- Automatic Port Selection (PAUI = 0 and AUTOSEL = 1)
- Normal Receive Threshold (NTH = 1)
- Mode 4 (compatible with National NS8390 controllers) (MD0 = 1, MD1 = 1)
- SQE Disabled (DSQE = 1)
- Link Testing Enabled (LI = 1)

Status outputs are grouped at lower left. Local status outputs drive LED indicators and remote status indicators are available as required.

Power and ground pins are shown at the bottom of the diagram. A single power supply is used for both VCC1 and VCC2 with a decoupling capacitor installed between the power and ground buses.

Figure 31: Remote Signaling Link Integrity Pulse Timing

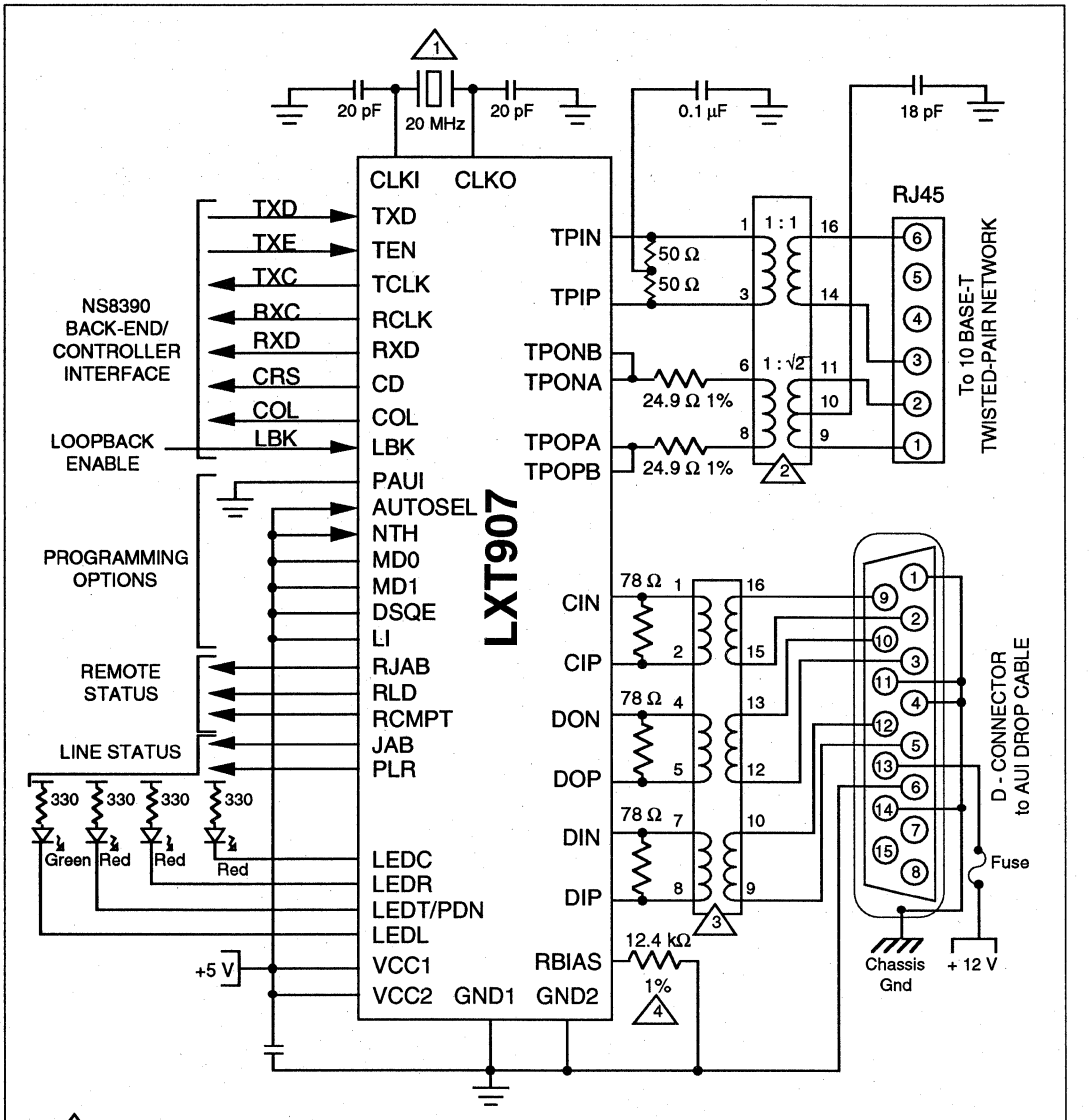


Notes:

1. For Remote Link Down (RLD) signaling, the interval between LI pulses increments from 10 ms to 15 ms to 20 ms, and then the cycle starts over.
2. For Remote Jabber (RJAB) signaling, the interval between LI pulses decrements from 20 ms to 15 ms to 10 ms, and then the cycle starts over.
3. For Remote Compatibility (RCMPT) signaling, the interval between LI pulses continually switches between 10 ms and 20 ms.

The TP and AUI interfaces are shown at upper and lower right, respectively. Impedance matching resistors for 100Ω UTP are installed in each I/O pair but no external filters are required. Suitable transformers are listed in notes 2 and 3.

Figure 32: LAN Adapter Board Application - Auto Port Select with External LPBK Control

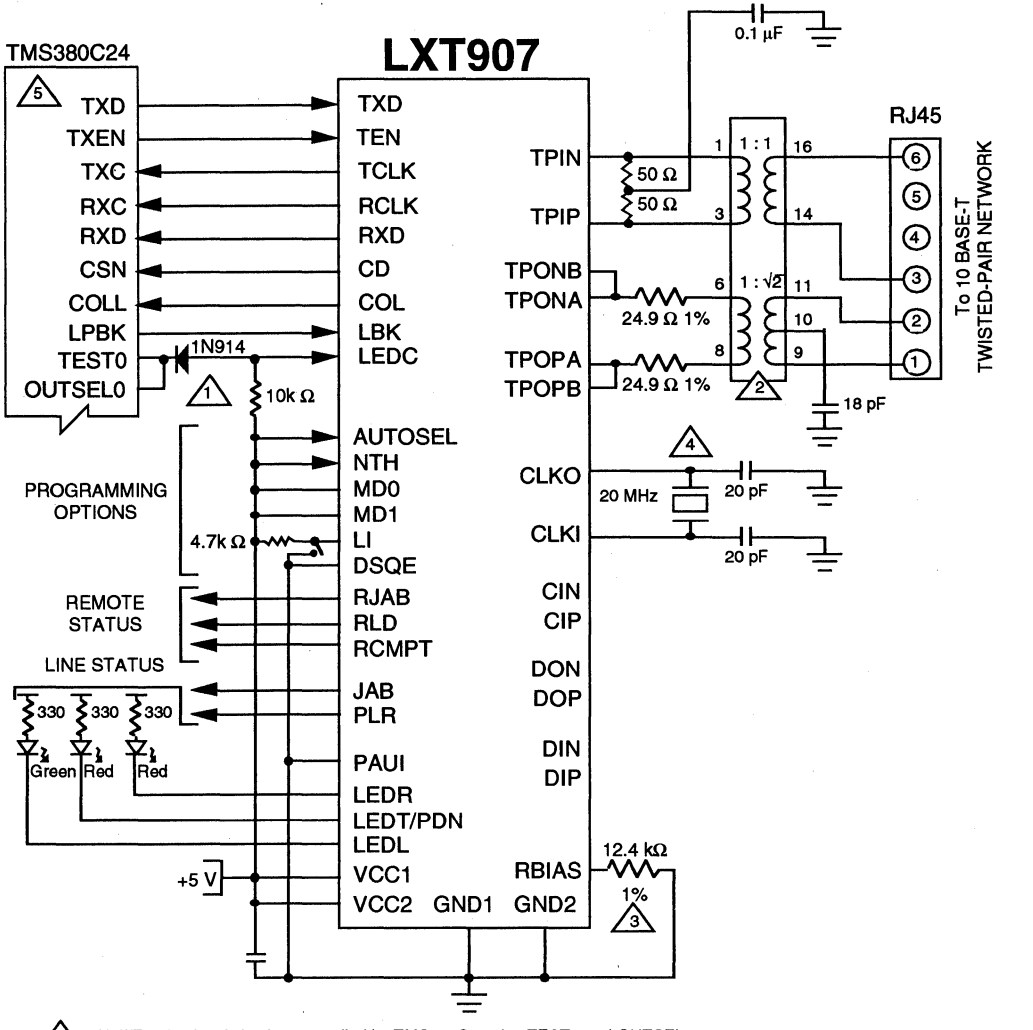


1. Suitable crystals include the MTRON MP-1 and MP-2.
2. Suitable TP transformers include the Fil-Mag 23Z128, and SM23Z128; Valor PT4069 and ST7011; Pulse Engineering PE65994 and PE65745; Belfuse S553-0716 and A553-0716; and Halo Engineering TD42-2006Q and TG42-2006W1.
3. Suitable AUI transformers include the Fil-Mag 23Z90 and SM23Z90; Valor LT6032 and ST7032; Halo TG01-0756K and TG01-1006K; and Pulse Engineering PE64502 and PE65723.
4. Bias resistor RBIAS should be located close to the pin and isolated from other signals.

Full Duplex Support (Figure 33)

Figure 33 shows the LXT907 with a Texas Instruments 380C24 CommProcessor. The 380C24 is compatible with Mode 4 (MD0 and MD1 both high). When used with the 380C24 or other full duplex-capable controller, the LXT907 supports full-duplex Ethernet, effectively doubling the available bandwidth of the network. In this application the SQE function is enabled (DSQE tied to ground), and the LXT907 AUI port is not used.

Figure 33: Full-Duplex Application - Auto Port Select with External LPBK Control

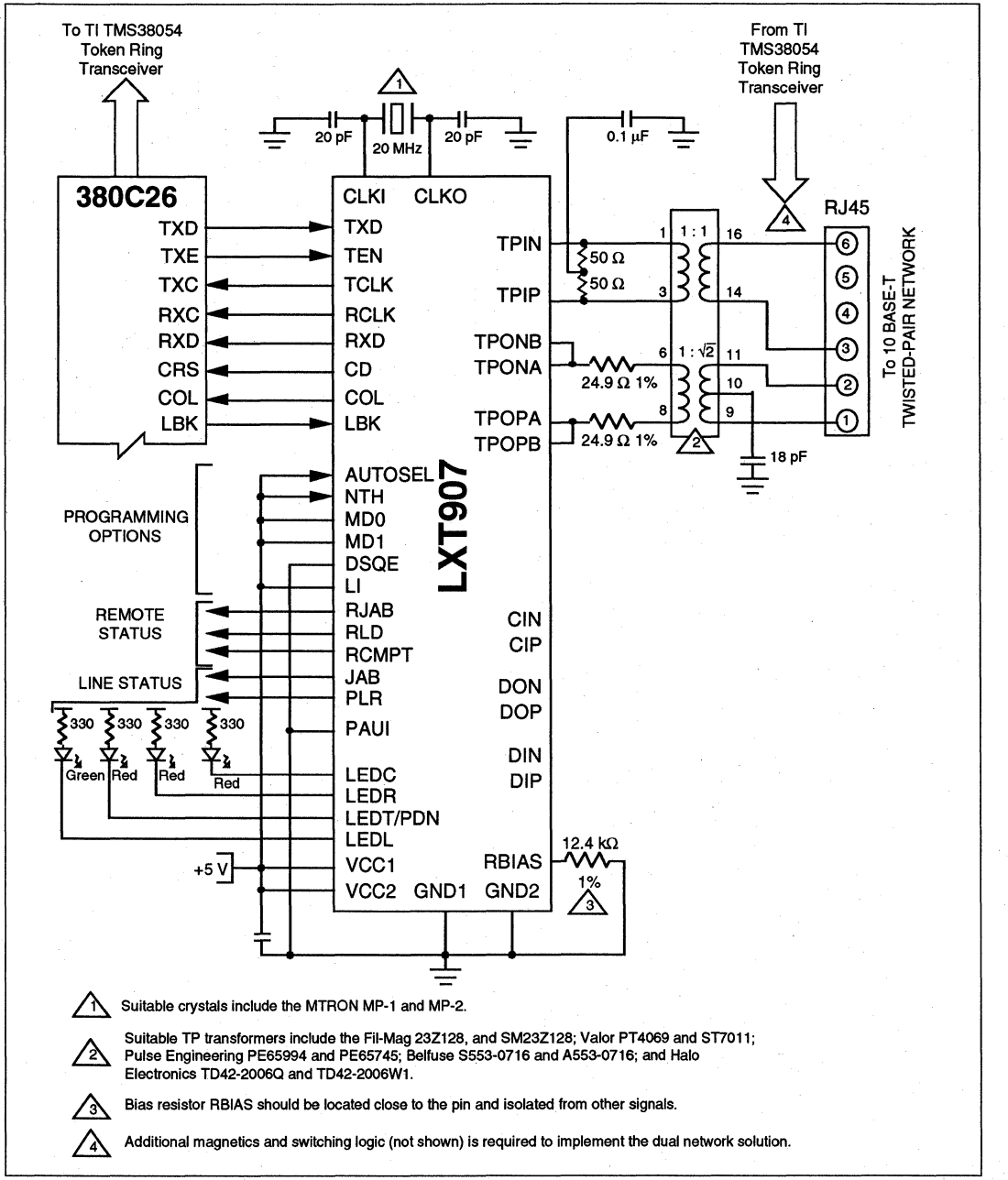


1. Half/Full Duplex Selection controlled by TMS380C24 pins TEST0 and OUTSEL0.
2. Suitable TP transformers include the Fil-Mag 23Z128, and SM23Z128; Valor PT4069 and ST7011; Pulse Engineering PE65994 and PE65745; Belfuse S553-0716 and A553-0716; and Halo Electronics TD42-2006Q and TD42-2006W1.
3. Bias resistor RBIAS should be located close to the pin and isolated from other signals.
4. Suitable crystals include the MTRON MP-1 and MP-2.
5. The TMS380C26 may be substituted for dual network support of 10Base T and Token Ring.

Dual Network Support - 10Base T and Token Ring (Figure 34)

Figure 34 shows the LXT907 with a Texas Instruments 380C26 CommProcessor. The 380C26 is compatible with Mode 4 (MD0 and MD1 both high). When used with the 380C26, both the LXT907 and a TM380054 Token Ring transceiver can be tied to a single RJ45 connector. The SQE function is enabled (DSQE tied to ground), and the LXT907 AUI port is not used.

Figure 34: LXT907/380C26 Interface for Dual Network Support of 10Base T and Token Ring

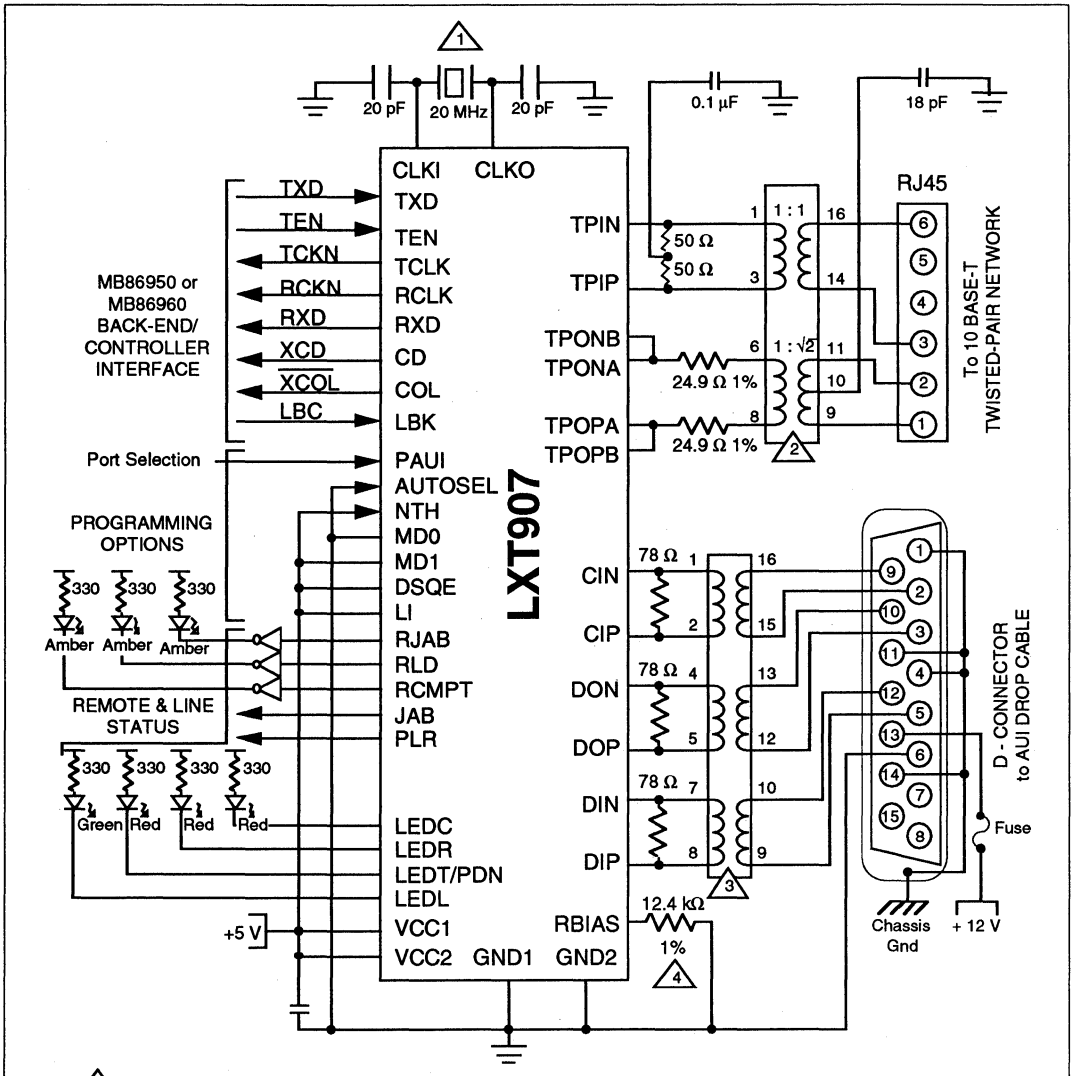


1. Suitable crystals include the MTRON MP-1 and MP-2.
2. Suitable TP transformers include the Fil-Mag 23Z128, and SM23Z128; Valor PT4069 and ST7011; Pulse Engineering PE65994 and PE65745; Belfuse S553-0716 and A553-0716; and Halo Electronics TD42-2006Q and TD42-2006W1.
3. Bias resistor RBIAS should be located close to the pin and isolated from other signals.
4. Additional magnetics and switching logic (not shown) is required to implement the dual network solution.

Manual Port Select with Link Test Function (Figures 35 and 36)

With MD0 low and MD1 tied high, the LXT907 logic and framing are set to Mode 3 (compatible with Fujitsu MB86950 and MB86960, and Seeq 8005 controllers). Figure 35 shows the setup for Fujitsu controllers. Figure 36 shows the four inverters required to interface with the Seeq 8005 controller. Both these Mode 3 applications show the LI pin tied high, enabling Link Testing; and the NTH and

Figure 35: LAN Adapter Board Application - Manual Port Select with Link Test Function



1 Suitable crystals include the MTRON MP-1 and MP-2.

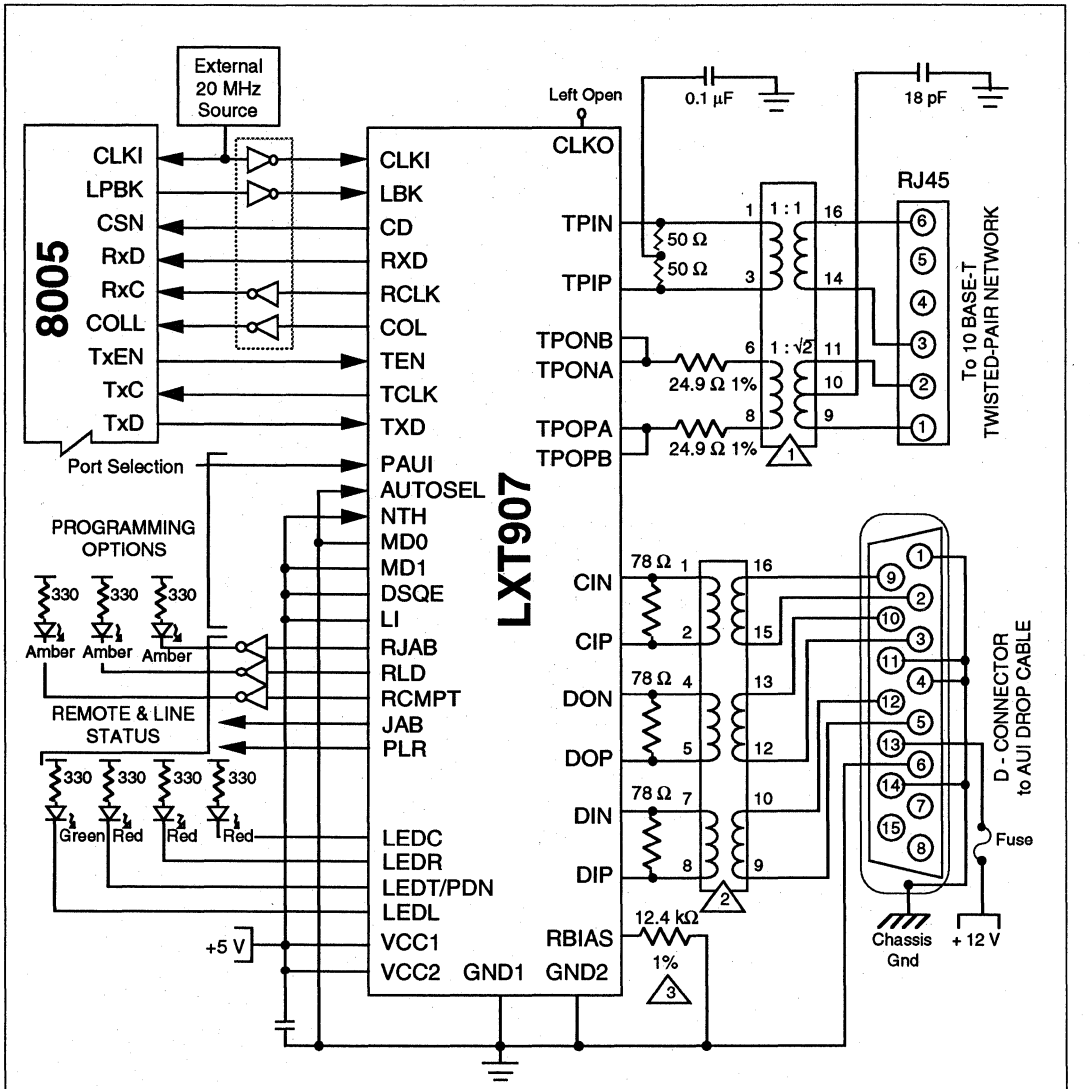
2 Suitable TP transformers include the Fil-Mag 23Z128, and SM23Z128; Valor PT4069 and ST7011; Pulse Engineering PE65994 and PE65745; Belfuse S553-0716 and A553-0716; and Halo Engineering TD42-2006Q and TG42-2006W1.

3 Suitable AUI transformers include the Fil-Mag 23Z90 and SM23Z90; Valor LT6032 and ST7032; Halo TG01-0756K and TG01-1006K; and Pulse Engineering PE64502 and PE65723.

4 Bias resistor RBIAS should be located close to the pin and isolated from other signals.

DSQE pins are both tied high, selecting the standard receiver threshold and disabling the SQE function. However, in these applications AUTOSEL is tied low, allowing external port selection through the PAUI pin. The remote status outputs are inverted to drive LED indicators.

Figure 36: Manual Port Select with Seeq 8005 Controller

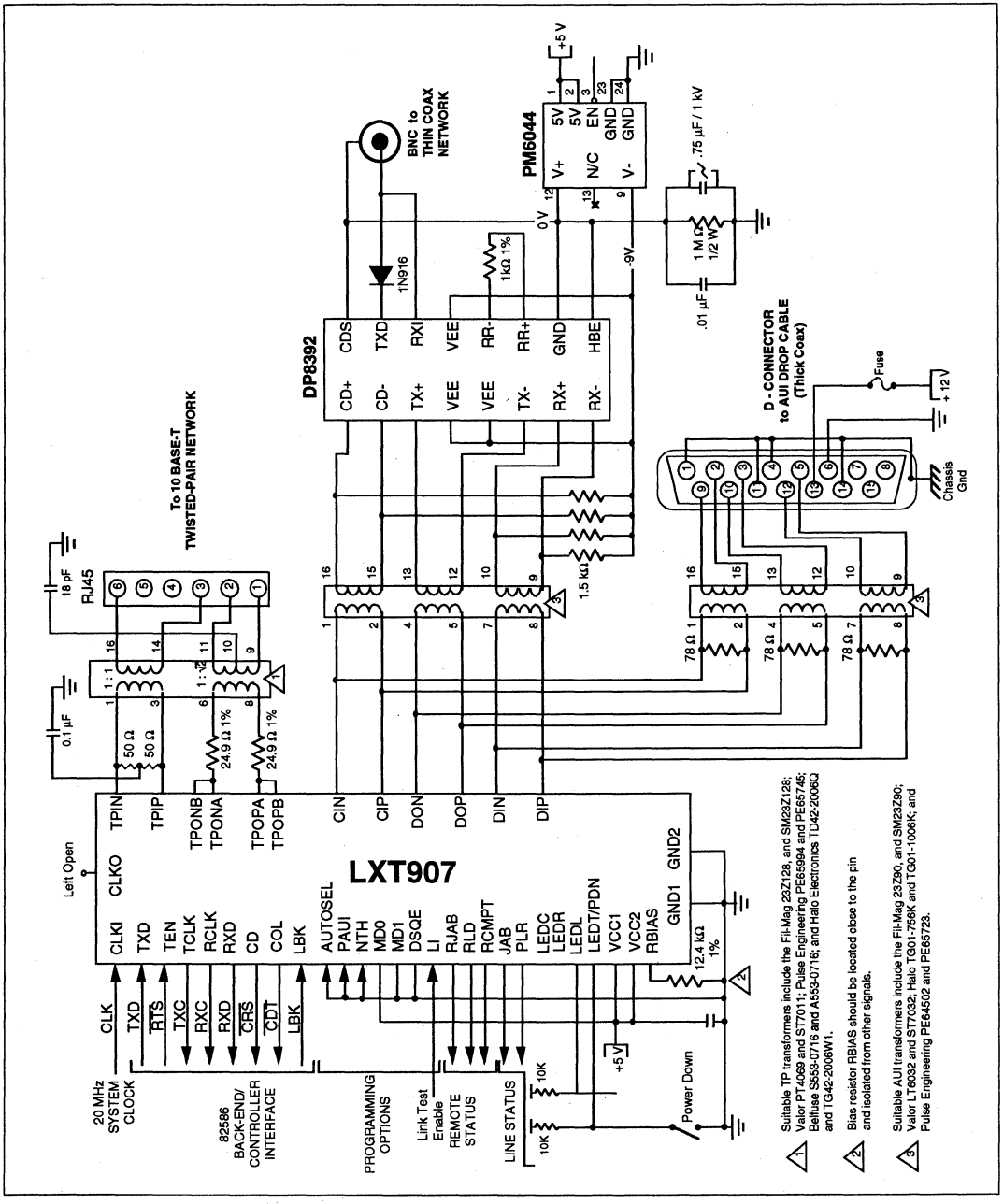


1. Suitable TP transformers include the Fil-Mag 23Z128, and SM23Z128; Valor PT4069 and ST7011; Pulse Engineering PE65994 and PE65745; Belfuse S553-0716 and A553-0716; and HALO TD42-2006Q and TG42-2006W1.
2. Suitable AUI transformers include the Fil-Mag 23Z90 and SM23Z90; Valor LT6032 and ST7032; Halo TG01-0756K and TG01-1006K; and Pulse Engineering PE64502 and PE65723.
3. Bias resistor RBIAS should be located close to the pin and isolated from other signals.

Three Media Application (Figure 37)

Figure 37 shows the LXT907 in Mode 2 (compatible with Intel 82586/686 controllers) with additional media options for the AUI port. Two transformers are used to couple the AUI port to either a D-connector or a BNC connector. (A DP8392 coax transceiver with PM6044 power supply are required to drive the thin coax network through the BNC.)

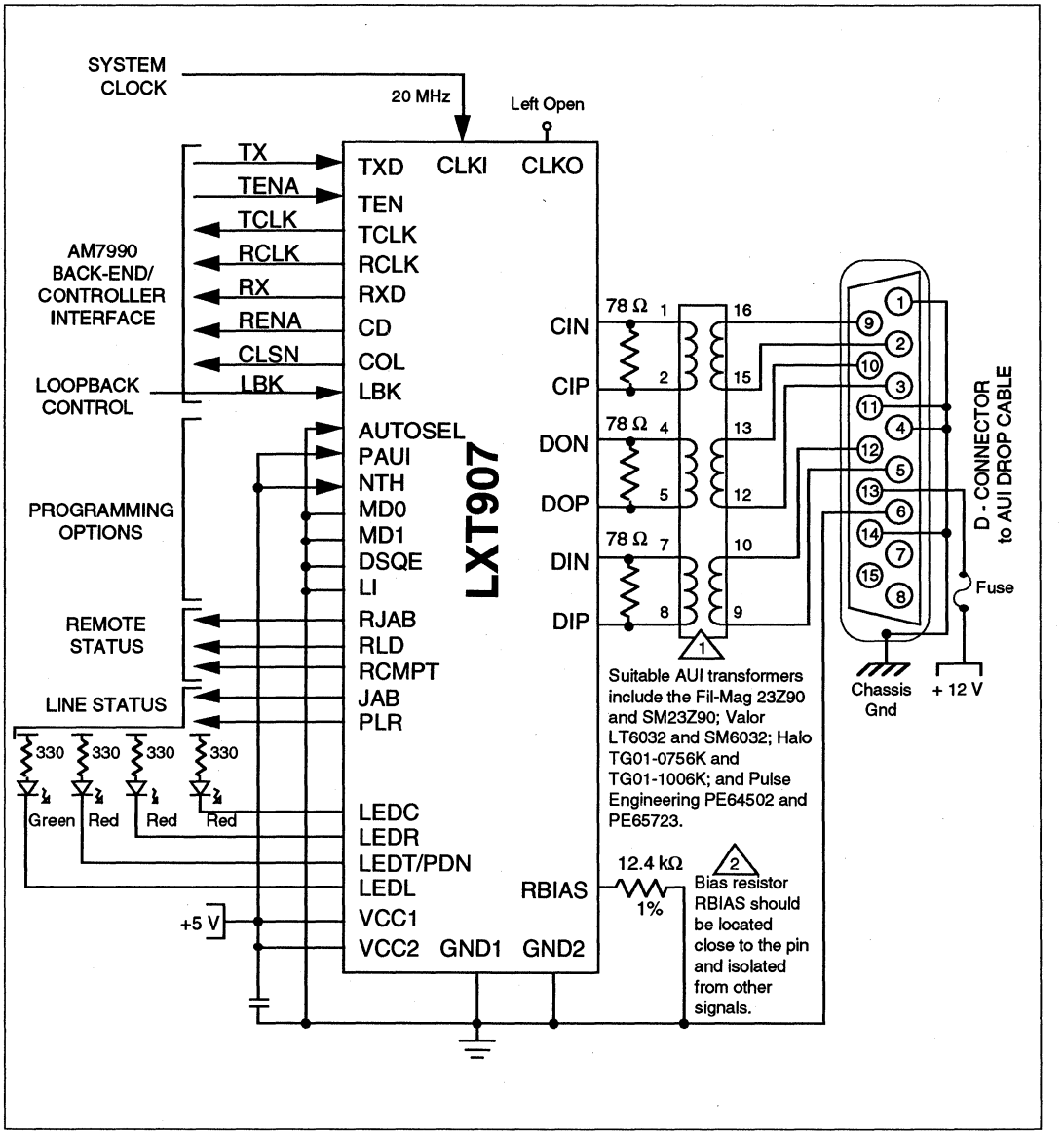
Figure 37: Three Media Application



AUI Encoder/Decoder Only (Figure 38)

In this application the DTE is connected to a coaxial network through the AUI. AUTOSEL is tied low and PAUI is tied high, manually selecting the AUI port. The twisted-pair port is not used. With MD1 and MD0 both low, the LXT907 logic and framing are set to Mode 1 (compatible with AMD AM7990 controllers). The LI pin is tied low, disabling the link test function. The DSQE pin is also low, enabling the SQE function. The LBK input controls loopback. A 20 MHz system clock is supplied at CLKI with CLKO left open.

Figure 38: AUI Encoder/Decoder Only Application



Preliminary Information
February, 1994

LXT914
Flexible Quad Hub Repeater

General Description

The LXT914 is an integrated multi-port repeater designed for mixed-media networks. It provides all the active circuitry required for the repeater function in a single CMOS device. It includes one Attachment Unit Interface (AUI) port and four 10Base-T transceivers. The AUI port allows connection of an external transceiver (10Base-2, 10Base-5, 10Base-T or FOIRL) or a drop cable. The 10Base-T transceivers are entirely self-contained and **require no external filters**.

An inter-repeater backplane interface allows 128 or more 10Base-T ports to be cascaded together. In addition, a serial port provides information for network management.

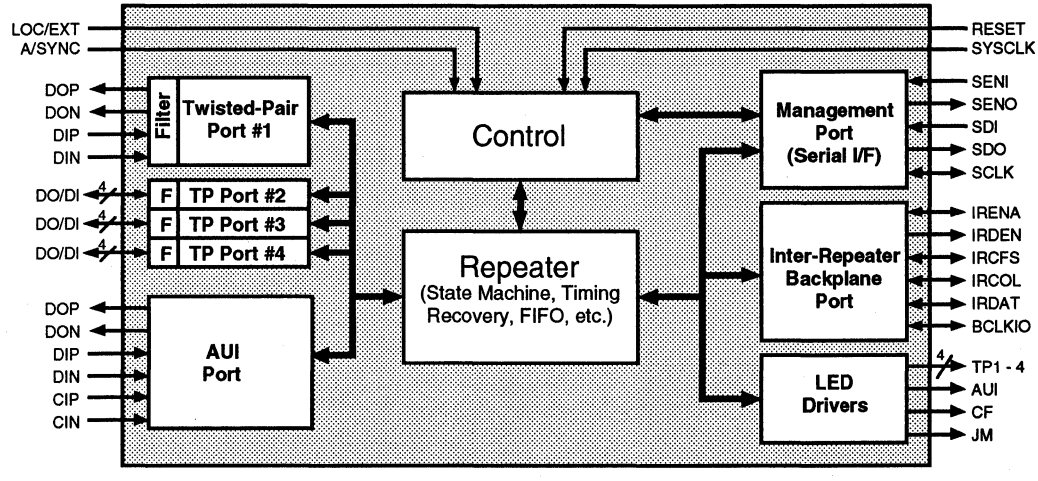
The LXT914 is fabricated with an advanced CMOS process and requires only a single 5-volt power supply.

Key Features

- Four integrated 10Base-T transceivers and one AUI transceiver on a single chip
- Automatic polarity detection and correction
- On-chip transmit and receive filters
- Automatic partitioning of faulty stations
- Programmable squelch level allows extended range in low-noise environments
- Synchronous or asynchronous inter-repeater backplane supports "hot swapping"
- Inter-repeater backplane allows cascaded repeaters, linking 128 or more 10Base-T ports
- Serial port for selecting programmable options
- Seven integrated LED drivers
- Packaged in 68-pin PLCC

3

Figure 1. Block Diagram



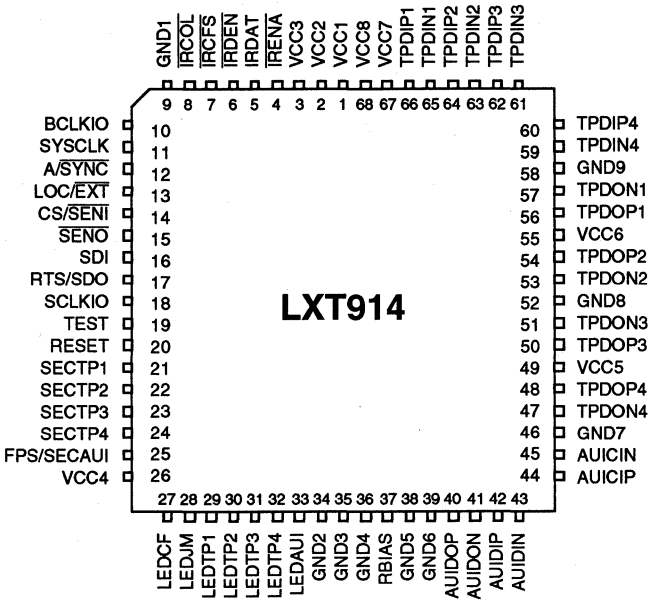


Table 1: Common Power, Ground and Clock Pin Descriptions

Pin #	Symbol	I/O	Name	Description
1 2 3 26 49 55 67 68	VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8	I I I I I I I I	Power Supply Inputs 1 through 8	These pins each require a +5 VDC power supply input. The various inputs may be supplied from a single power source, but special de-coupling requirements may apply. Each VCC input must be within ± 0.3 V of every other VCC input.
9 34 35 36 38 39 46 52 58	GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9	– – – – – – – – –	Ground 1 Ground 2 Ground 3 Ground 4 Ground 5 Ground 6 Ground 7 Ground 8 Ground 9	These pins provide ground return paths for the various power supply inputs.
37	RBIAS	–	Bias	This pin provides bias current for the internal circuitry. The 100 µA bias current is provided through an external 12.4 kΩ resistor to ground.
10	BCLKIO	I/O	Backplane Clock	This 10 MHz clock is used to synchronize multiple repeaters on a common backplane. In the synchronous mode, BCLKIO must be supplied to all repeaters from a common external source. In the asynchronous mode, BCLKIO is supplied only when a repeater is outputing data to the bus. Each repeater outputs its internally recovered clock when it takes control of the bus. Other repeaters on the backplane then sync to BCLKIO for the duration of the transmission.
11	SYSCLK	I	System Clock	The required 20 MHz system clock is input at this pin.

Table 2: Inter-Repeater Backplane Pin Descriptions

Pin #	Symbol	I/O	Name	Description
4	$\overline{\text{IRENA}}$	I/O	Inter-Repeater Backplane Enable	This pin allows individual LXT914 repeaters to take control of the Inter-Repeater Backplane (IRB) data bus (IRDAT). The $\overline{\text{IRENA}}$ bus must be locally pulled up by a 330 Ω resistor.
5	IRDAT	I/O	IRB Data	This pin is used to pass data between multiple repeaters on the IRB. The IRDAT bus must be locally pulled up by a 330 Ω resistor.
6	$\overline{\text{IRDEN}}$	O	IRB Driver Enable	The $\overline{\text{IRDEN}}$ pin is used to enable external bus drivers which may be required in synchronous systems with large backplanes. This is an active low signal which is maintained for the duration of the data transmission. In a multiple repeater configuration, all $\overline{\text{IRDEN}}$ pins may be tied together (wire "OR" ed) to drive the direction input of bi-directional external bus transceivers. This wired OR bus must be locally pulled up by a 330 Ω resistor.
7	$\overline{\text{IRCFS}}$	I/O	IRB Collision Flag Sense	These two pins are used for collision signaling between multiple LXT914 devices on the Inter-Repeater Backplane (IRB). Both the $\overline{\text{IRCFS}}$ bus and the $\overline{\text{IRCOL}}$ bus must be pulled-up globally with 330 Ω resistors. ($\overline{\text{IRCFS}}$ requires a precision resistor (± 1 %).)
8	$\overline{\text{IRCOL}}$	I/O	IRB Collision	

1 The $\overline{\text{IRENA}}$, IRDAT and $\overline{\text{IRDEN}}$ buses are pulled up locally (ie., one pull-up resistor per board. If there are three 914s per board, all three 914s share a single pull-up resistor on **each** board.)

2 The $\overline{\text{IRCFS}}$ and $\overline{\text{IRCOL}}$ buses are pulled up globally (ie., one pull-up resistor for **all** boards. If there are eight boards in the system, all eight boards share a single pull-up resistor. The global pull-up may be located on one of the boards, or on the backplane.)

Table 3: Mode Select Pin Descriptions

Pin #	Symbol	I/O	Name	Description
12	A/$\overline{\text{SYNC}}$	I	Backplane Synch Mode Select	This pin selects the backplane synch mode. When this pin is left floating an internal pull-up defaults to the Asynchronous mode (A/$\overline{\text{SYNC}}$ high). In the asynchronous mode 12 or more LXT914s can be connected on the backplane, and an external 10 MHz backplane clock source is not required. When the synchronous mode is selected (A/$\overline{\text{SYNC}}$ tied low), 32 or more LXT914s can be connected to the backplane and an external 10 MHz backplane clock source is required.
13	LOC/$\overline{\text{EXT}}$	I	Management Mode Select	This pin selects the management mode. When this pin is left floating, an internal pull-up defaults to the Local management mode (LOC/$\overline{\text{EXT}}$ high). In the Local mode, setup parameters are downloaded from an EEPROM during initialization. Once initialized with the setup parameters, the repeater functions independently. When the External management mode is selected (LOC/$\overline{\text{EXT}}$ tied low), an external management device (EMD) provides setup parameters during initialization. The EMD maintains serial communication with the repeater during operation and can change the setup parameters at any time.

Table 4: Serial Port Pin Descriptions - External Management Mode

Pin #	Symbol	I/O	Name	Description
14	$\overline{\text{SENI}}$	I	Serial Enable Input	This active low input is used to access the LXT914 serial interface. To write to the serial input (SDI), the External Management Device (EMD) must drive this pin from high to low. The input must be asserted low concurrent with the appearance of data on SDI and remain low for the duration of the serial input transaction.
15	$\overline{\text{SENO}}$	O	Serial Enable Output	This active low output is used to access the serial interface of the EMD. When the LXT914 sends a data stream to the EMD through the serial port (SDO), this output transitions from high to low and remains low for the duration of the serial transmission.
16	SDI	I	Serial Data Input	This pin is the input for the serial interface with the EMD. Setup and operating parameters are supplied to the LXT914 in a serial data stream from the EMD through this port.
17	SDO	O	Serial Data Output	After every packet transmission or interrupt event, the LXT914 reports status information to the EMD in a serial data stream through this port.
18	SCLK	I	Serial Clock	This 10 MHz clock synchronizes the serial interface between the LXT914 and the EMD. Both devices must be supplied from the same clock source. In synchronous mode, SCLK and BCLK may be tied together.

Table 5: Serial Port Pin Descriptions - Local Management Mode

Pin #	Symbol	I/O	Name	Description
14	CS	O	Chip Select	The LXT914 is designed for use with an EEPROM or similar device which may be used to store setup parameters and serially download them to the LXT914 during initialization. In a single-device application or in the first device of a daisy chain application, this pin is an active high Chip Select output used to enable the EEPROM.
	$\overline{\text{SENI}}$	I	Serial Enable Input	In subsequent devices of a daisy-chain configuration, a high-to-low transition on this pin enables the serial input port (SDI). The input must be asserted concurrent with the appearance of data on SDI and remain low for the duration of the serial input transaction.
15	$\overline{\text{SENO}}$	O	Serial Enable Output	During initialization, the LXT914 accepts 48 bits of setup data through the SDI port. After the 48th bit, the LXT914 asserts this pin low. When multiple LXT914 devices are connected in a daisy-chain, this output is tied to the $\overline{\text{SENI}}$ input of the next device in the chain. Thus each device in the chain is serially enabled by the previous device until all the devices have read in their 48 bits of setup data.
16	SDI	I	Setup Data Input	This pin is the serial input port for the setup parameters (48 bits). This pin should be tied low if no EEPROM is present.
17	RTS	O	Request To Send	In a single device application or in the first device of a daisy chain application, this pin outputs a 9-bit, active high sequence. This pin must be tied to the EEPROM DI input to trigger the EEPROM to download its stored data. In subsequent devices this pin is not used.
18	SCLKIO	I/O	Serial Clock	A 1 MHz clock provided by the first LXT914 in the chain to all subsequent repeaters and the EEPROM. In the Local mode all repeaters have their SCLKIO pins tied together.

Table 6: Miscellaneous Control Pin Descriptions

Pin #	Symbol	I/O	Name	Description
19	TEST	I	Test Mode Select	This pin must be tied low for normal operation. A high on this pin enables the Factory Test mode.
20	RESET	I	RESET	This pin resets the LXT914 circuitry when pulled high for ≥ 1 µs.
21 22 23 24	SECTP1 SECTP2 SECTP3 SECTP4	I I I I	Security Mode Select (TP Ports 1 - 4)	These pins enable the security mode for the respective twisted-pair ports (TP1 through TP4). When pulled high, the LXT914 JAMs the affected port. The SEC pins must be tied low if external security control is not required.
25	SECAUI (External)	I	Security Mode Select (AUI Port)	In the External mode this pin enables the security mode for the AUI port. When pulled high, the LXT914 JAMs the AUI port. The security feature is available only in External management mode.
	FPS (Local)		First Position Select	In the Local mode this pin identifies the first device in a daisy chain configuration. When tied high (First position), the LXT914 controls the local EEPROM by providing clock and handshaking. When tied low (Not First), the LXT914 will accept CLK and data in its turn from previous LXT914s in the data chain.

Table 7: LED Driver Pin Descriptions

Pin #	Symbol	I/O	Name	Description
27	LEDCF	O	Collision & FIFO Error LED Driver	This tri-state LED driver pin reports collisions and FIFO errors. It pulses low to report collisions, and pulses high to report FIFO errors. When this pin is connected to the anode of one LED and to the cathode of a second LED, the LXT914 will simultaneously monitor and report both conditions independently.
28	LEDJM	O	Jabber/MJLP & Manchester Code Violation LED Driver	This tri-state LED driver pin reports jabber and code violations. It pulses low to report MAU Jabber Lockup Protection (MJLP), and pulses high to report manchester code violations. When this pin is connected to the anode of one LED and to the cathode of a second LED, the LXT914 will simultaneously monitor and report both conditions independently.
29 30 31 32	LEDTP1 LEDTP2 LEDTP3 LEDTP4	O O O O	TP Port LED Drivers	These tri-state LED drivers use an alternating pulsed output to report TP port status. Each pin should be tied to a pair of LEDs (to the anode of one LED and the cathode of a second LED). When connected this way, each pin reports five separate conditions (receive, transmit, link integrity, reverse polarity and auto partition).
33	LEDAUI	O	AUI Port LED Driver	This tri-state LED driver uses an alternating pulsed output to report AUI port status. This pin should be tied to a pair of LEDs (to the anode of one LED and the cathode of a second LED). When connected this way, this pin reports five separate conditions (receive, transmit, receive jabber, receive collision and auto partition).

Table 8: Repeater Port Pin Descriptions

Pin #	Symbol	I/O	Name	Description
40 41	AUIDOP AUIDON	O O	AUI Data Out Pos & Neg	These pins are the positive and negative data outputs for the AUI Port.
42 43	AUIDIP AUIDIN	I	AUI Data In Pos & Neg	These pins are the positive and negative data inputs for the AUI Port.
44 45	AUICIP AUICIN	I I	AUI Collision Pos & Neg	These pins are the positive and negative Collision inputs for the AUI Port.
47 48 50 51 53 54 56 57	TPDON4 TPDOP4 TPDOP3 TPDON3 TPDON2 TPDOP2 TPDOP1 TPDON1	O O O O O O O O	Line Driver Outputs for Twisted-Pair Ports	These pins are the positive and negative outputs from the line drivers for the respective twisted-pair ports.
59 60 61 62 63 64 65 66	TPDIN4 TPDIP4 TPDIN3 TPDIP3 TPDIN2 TPDIP2 TPDIN1 TPDIP1	I I I I I I I I	Twisted-Pair Data Inputs Positive & Negative	These pins are the positive and negative data inputs to the respective twisted-pair ports.

Table 9: Operating Conditions (Voltage with respect to ground unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Units
Recommended supply voltage	V_{CC}	4.75	5.0	5.25	V
Recommended operating temperature	T_{OP}	0	-	70	°C
Supply current	I_{CC}	–	–	250	mA

Absolute Maximum Ratings*

- **Supply Voltage** V_{CC} **-0.3 V to 6 V**
- **Operating temperature** T_{OP} **0 °C (min) to +70 °C (max)**
- **Storage temperature** T_{ST} **-65 °C (min) to +150 °C (max)**

* **Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.**

Table 10: I/O Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input low voltage [2]	V_{IL}	–	–	0.8	V	
Input high voltage [2]	V_{IH}	2.0	–	–	V	
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
Output low voltage	V_{OL}	–	–	10	% V_{CC}	I_{OL} < 10 µA
Output high voltage	V_{OH}	2.4	–	–	V	I_{OH} = 40 µA
Output high voltage	V_{OH}	90	–	–	% V_{CC}	I_{OH} < 10 µA
Input low current	I_{IL}	–	–	2	mA	V_{OL} = .4 V
Output rise / fall time	–	–	3	8	ns	C_{LOAD} = 20 pF

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Limited functional test patterns are performed at these input levels. The majority of functional tests are performed at levels of 0.4 V and 2.4V.

3

Table 11: AUI Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input low current [2]	I_{IL}	–	–	-700	µA	
Input high current [2]	I_{IH}	–	–	500	µA	
Differential output voltage	V_{OD}	± 550	–	± 1200	mV	
Receive input impedance [2]	Z_{IN}	–	20	–	kΩ	Between CIP/CIN & DIP/DIN
Differential squelch threshold	V_{DS}	–	220	–	mV	

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Parameter is guaranteed by design; not subject to production testing.

Table 12: TP Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance [2]	Z_{OUT}	–	5	–	Ω	
Peak differential output voltage	V_{OD}	3.3	3.5	3.7	V	Load = 100 Ω at TPOP and TPON
Transmit timing jitter addition [2]	–	–	± 6.4	± 10	ns	0 line length
Transmit timing jitter added by the MAU and PLS sections [2,3]	–	–	± 3.5	± 5.5	ns	After line model specified by IEEE 802.3 for 10Base-T
Receive input impedance [2]	Z_{IN}	–	20	–	kΩ	Between TPIP/TPIN
Differential squelch threshold (Normal threshold : NTH = 1)	V_{DS}	300	420	565	mV	5 MHz square wave input
Differential squelch threshold (Reduced threshold : NTH = 0)	V_{DSL}	180	250	345	mV	5 MHz square wave input

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Parameter is guaranteed by design; not subject to production testing.
[3] IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 13: IRB Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
Output high voltage	V_{OH}	–	–	TBD	mV
Output low voltage	V_{OL}	–	–	% Vcc	mV
Output rise or fall time	T_{RF}	TBD	–	TBD	µS

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 14: Switching Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Minimum	Typical[1]	Maximum	Units
Jabber Timing				
Maximum transmit time	5.0	–	5.5	ms
Unjab time	–	9.6	–	µs
Link Integrity Timing				
Time link loss	–	60	–	ms
Time between Link Integrity Pulses	10	–	20	ms
Interval for valid receive Link Integrity Pulses	4.1	–	30	ms

Table 15: Serial Port Timing (External Mode)

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
SCLKIO high to $\overline{\text{SENI}}$ low (active)	t_{S1}	0	–	50	ns
SCLKIO high to SDIN data valid	t_{S2}	0	–	50	ns
SCLKIO high to $\overline{\text{SENO}}$ low (active)	t_{S3}	5	–	15	ns
SCLKIO low to SDOUT data valid	t_{S4}	5	–	15	ns

Table 16: Inter-Repeater Bus Timing

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
Start of Frame to $\overline{\text{IRDEN}}$ low (active)	t_{IRB1}	10	–	150	ns
Start of Frame to $\overline{\text{IRENA}}$ low (active)	t_{IRB2}	125	–	225	ns
BCLKIO to IRDAT valid	t_{IRB3}	5	–	30	ns
$\overline{\text{IRENA}}$ low (active) to TP outputs active	t_{IRB4}	525	–	600	ns
$\overline{\text{IRENA}}$ low (active) to AUI output active	t_{IRB5}	475	–	525	ns
End of Frame clock to $\overline{\text{IRENA}}$ high (inactive)	t_{IRB6}	5	–	30	ns
$\overline{\text{IRENA}}$ high (inactive) to $\overline{\text{IRDEN}}$ high (inactive)	t_{IRB7}	95	–	105	ns
$\overline{\text{IRENA}}$ high (inactive) to TP outputs inactive	t_{IRB8}	575	–	600	ns
$\overline{\text{IRENA}}$ high (inactive) to AUI output inactive	t_{IRB9}	425	–	450	ns

Figure 2: Serial Port Timing

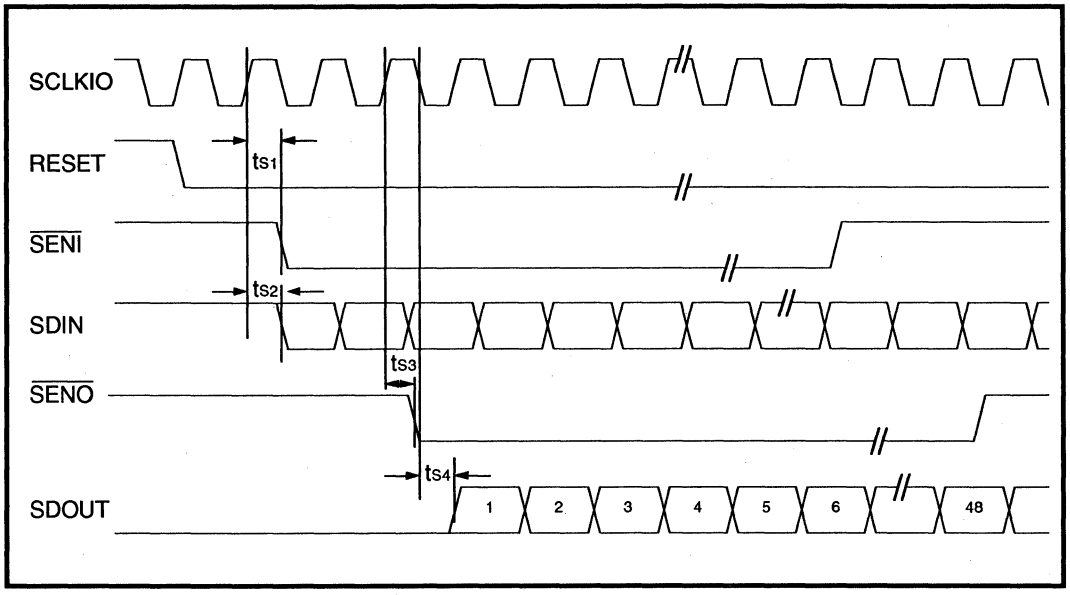
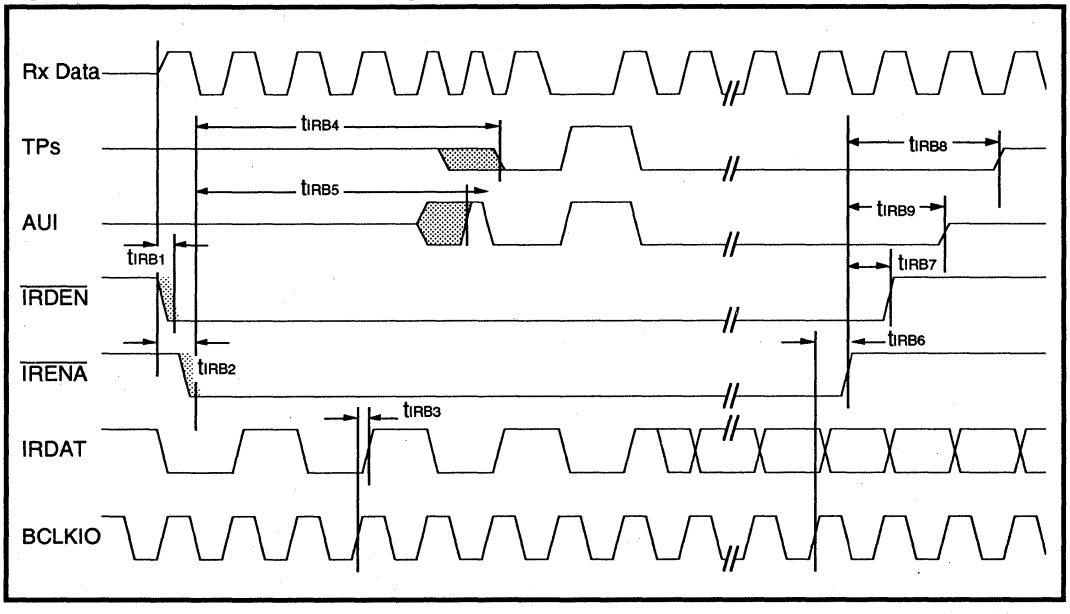


Figure 3: Inter-Repeater Bus Timing



General Description

The LXT914 is an integrated hub repeater for 10Base-T networks. The hub repeater is the central point for information transfer across the network. The LXT914 offers multiple operating modes to suit a broad range of applications ranging from simple 4-port stand-alone hubs, to intelligent 128-port enterprise systems with microprocessor/gate array management.

The LXT914 includes four 10Base-T ports which are essentially self-contained transceivers. The LXT914 also includes an Attachment Unit Interface (AUI) port, a serial port and an Inter-Repeater Backplane (IRB) port. The AUI port allows the 10Base-T network to interface with other networks (10Base-2, 10Base-5 or FOIRL). The serial port allows an external device such as an EEPROM to download setup parameters to the repeater. In more complex designs the serial port can also be used to monitor repeater status. The IRB port enables multiple LXT914s to function as a single repeater.

10Base-T Ports

The four 10Base-T transceiver ports are completely self-contained. Since the transmitters and receivers include the required filtering, only simple, inexpensive transformers are required to complete the 10Base-T interface. Each individual Twisted-Pair (TP) port is implemented in accordance with the IEEE 802.3 10Base-T standard.

AUI Port

The AUI port is fully compliant with IEEE requirements. It allows connection of a drop cable or an external transceiver (10Base-2, 10Base-5, 10Base-T, or FOIRL). The AUI port supports both capacitive coupling and transformer coupling. The AUI transmitter is a current driver which requires a 78Ω termination load.

Serial Port

The serial port provides the management interface to the LXT914. Refer to Table 15 and Figure 2 for serial port timing. The serial port can be either uni-directional or bi-directional, depending on the management mode selected. In the Local management mode the serial port is uni-directional (input only), and is used only to download setup parameters during initialization. The Local mode is intended for use with a simple EEPROM, but the serial port may be tied low if an EEPROM is not required.

In the External management mode, the serial port is bi-directional (input for setup parameters, output for status reports). The External mode is intended for use with an External Management Device (EMD) and a Media Access Controller (MAC). The EMD (typically a gate array) communicates with a microprocessor (eg. Intel 8051) and can control up to three LXT914 repeaters. This simplifies design of a relatively standard 12-port repeater on a single printed circuit board.

Inter-Repeater Backplane

The Inter-Repeater Backplane (IRB) allows several LXT914s to function as a single repeater. Refer to Table 16 and Figure 3 for IRB timing. The IRB also allows several multi-repeater boards to be integrated in a standard rack and to function as a single unit. The IRB supports "hot swapping" for easy maintenance and troubleshooting. Each individual repeater distributes recovered and retimed data to other repeaters on the IRB for broadcast on all ports simultaneously. This simultaneous re-broadcast allows the multi-repeater system to act as a single large repeater unit. The maximum number of repeaters on the IRB is limited by bus loading factors such as parasitic capacitance.

The IRB can be operated synchronously or asynchronously. In the synchronous mode, a common external source provides the 10 MHz backplane clock (BCLKIO) and the 20 MHz system clock (SYSCLK) to all repeaters. (BCLKIO must be synchronous to SYSCLK and may be derived from SYSCLK using a divide-by-two circuit.) In the synchronous mode 32 or more LXT914 repeaters may be connected on the IRB, providing 128 10Base-T ports and 32 AUI ports.

In the asynchronous mode an external BCLKIO source is not required. The repeaters run independently until one takes control of the IRB. The transmitting repeater then outputs its own 10 MHz clock onto the BCLKIO line. All other repeaters sync to that clock for the duration of the transmission. In the asynchronous mode 12 or more LXT914 devices may be connected to the IRB, providing 48 10Base-T ports and 12 AUI ports.

NOTE

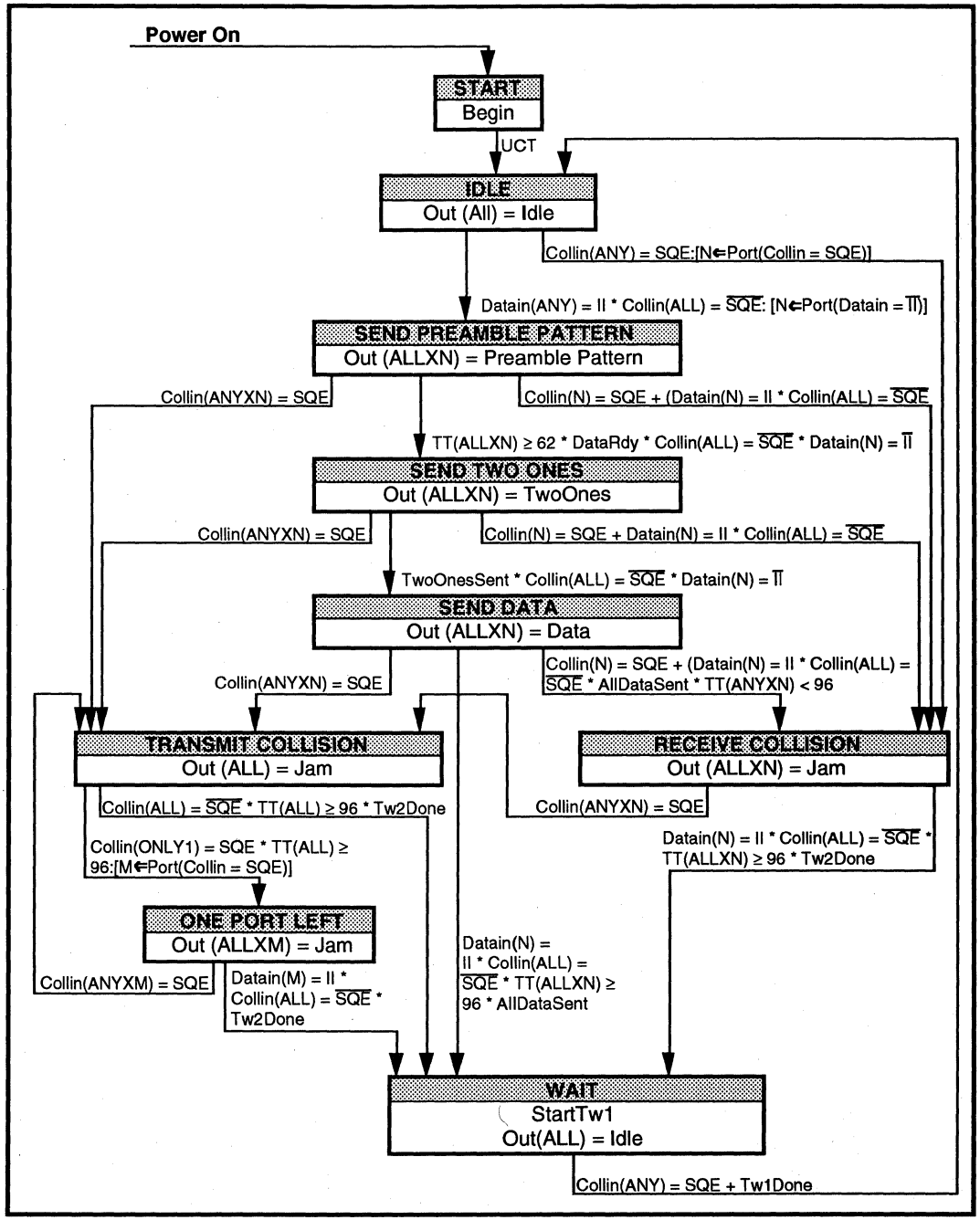
The maximum number of repeaters which may be linked on the backplane is limited by board design factors. These numbers listed above are engineering estimates only and may be increased if stronger drivers and careful board layout is used to reduce capacitive loading.

Repeater Circuitry

The basic repeater circuitry is shared among all the ports within the LXT914. It consists of a global repeater state machine, several timers and counters and the timing recovery circuit. The timing recovery circuit includes a FIFO for retiming and recovery of the clock which is used to clock the receive data out onto the IRB.

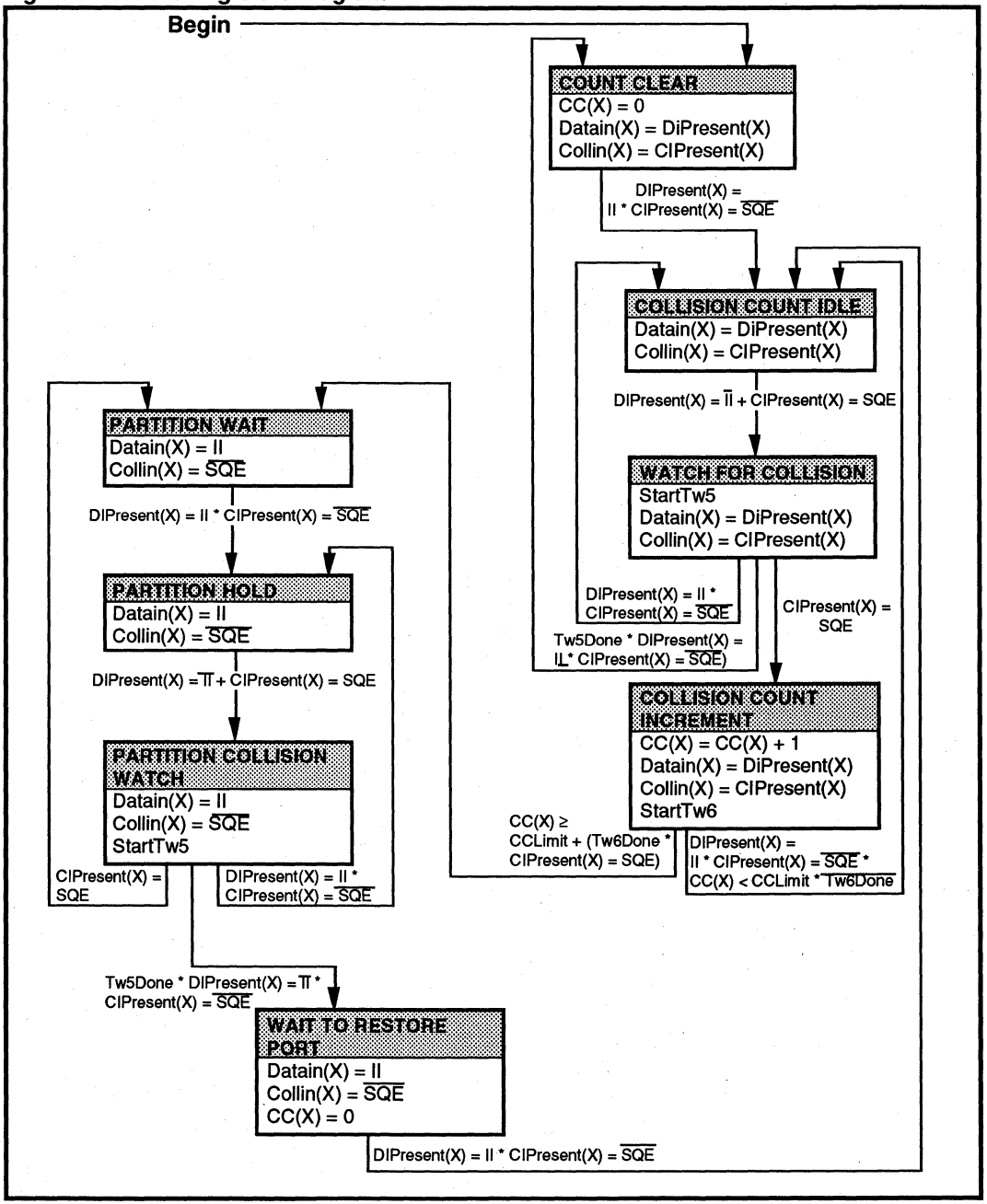
The shared functional blocks of the LXT914 are controlled by the global state machine shown in Figure 4. This diagram and all associated notations used are in strict accordance with section 9.6 of the IEEE 802.3 standard.

Figure 4: Global State Machine



The LXT914 also implements the Partition State Diagram as defined by the IEEE 802.3 standard and shown in Figure 5. The value of CCLimit as implemented in the LXT914 is 64. The CCLimit value sets the number of consecutive collisions that must occur before the port is subjected to automatic partitioning. Auto-partition/reconnection is also supported by the LXT914 with Tw5 conforming to the standard requirement of 450 to 560 bit times.

Figure 5: Partitioning State Diagram



Functional Description

The main functions of the LXT914 hub repeater are data recovery and re-transmission, and collision propagation. Data packets received at the AUI or 10Base-T ports are detected and recovered by the port receivers before being passed to the repeater core circuitry for retiming and re-transmission. Data packets received through the IRB port are essentially passed directly to the core for re-transmission. After recovery of a valid data packet, the repeater broadcasts it to all enabled stations, except the originator station.

Initialization

The following description applies to the initial power-on reset and to any subsequent hardware reset. When a reset occurs, the device senses the levels at the various control pins to determine the correct operating mode.

Local Management Mode Initialization

An internal pull-up causes the LXT914 to default to the Local management mode unless pin 13 (LOC/$\overline{\text{EXT}}$) is tied low. In the Local mode the serial port is a uni-directional interface used only to download setup parameters from an external device.

In a Locally managed multiple-repeater ("daisy chain") configuration, the first repeater in the chain performs special functions. First Position Select (FPS) pin 25 is used to establish position (FPS high = First, FPS low = Not First). After establishing the Hardware mode, each LXT914 monitors FPS pin 25 to determine its position.

If FPS = 1 (First Position), the repeater performs the following functions:

1. Outputs a 1 MHz Serial Clock (SCLK) on pin 18. SCLK is derived from the 20 MHz SYSCLK input in the ASYNC mode, and from BCLKIO in SYNC mode, and is supplied to the SCLK inputs of all other repeaters on the bus and to the EEPROM.
2. Asserts Chip Select (CS) high on pin 14 to enable the EEPROM.
3. Outputs a serial 9-bit request-to-send (RTS) strobe on pin 17. (The programmable device responds to the RTS strobe with a serial data stream containing the setup parameters for all repeaters in the chain.)
4. Clocks the first 48 serial data input (SDI) bits from the EEPROM on pin 16 into its setup register. Refer to Tables 17 and 18 for Setup Register bit assignments.
5. Asserts Serial Enable Output ($\overline{\text{SENO}}$) low on pin 15 to enable the next repeater in line.

The second repeater has FPS tied low and Serial Enable Input ($\overline{\text{SENI}}$) connected to the Serial Enable Output ($\overline{\text{SENO}}$) of the first repeater. When enabled by a low on $\overline{\text{SENI}}$, each repeater downloads its portion of the stream, then stops accepting data and asserts $\overline{\text{SENO}}$ low. The $\overline{\text{SENO}}$ pin is linked to the $\overline{\text{SENI}}$ input of the next repeater. This enables the next repeater to clock in its 48-bit word and so on.

If FPS = 0 (Not First Position), the repeater performs the following functions:

1. $\overline{\text{SYNC}}$s to the 1 MHz Serial Clock (SCLK) on pin 18. SCLK is supplied by the First Position repeater.
2. Responds to $\overline{\text{SENI}}$ low on pin 14 by enabling the SDI port.
3. Clocks 48 bits from the EEPROM into its setup register through the SDI port on pin 16.
4. Asserts $\overline{\text{SENO}}$ low on pin 15 to enable the next repeater in line.

External Management Mode Initialization

The LXT914 operates in the External management mode when pin 13 (LOC/$\overline{\text{EXT}}$) is tied low. In the External mode, the serial port is a bi-directional interface between the LXT914 and an external management device (EMD). The serial port is used to download initial setup parameters to the repeater and to monitor status reports from the repeater. The LXT914 setup parameters can be changed at any time by the EMD. The initialization process for each repeater in a managed mode configuration is the same, regardless of its position; each repeater is connected directly to the EMD. Each LXT914 initializes as follows:

1. Syncs to the 10 MHz Serial Clock (SCLK) on pin 18. SCLK must be supplied from an external source.
2. Responds to $\overline{\text{SENI}}$ low on pin 14 by enabling the SDI port.
3. Clocks 48 bits from the EMD into its setup register through the SDI port on pin 16.
4. Once initialized, the LXT914 reports its status in a 48-bit serial stream after every packet transmission or interrupt event. Refer to Tables 19 and 20 for packet status register bit assignments.

Table 17: Setup Register Bit Assignments

	D7	D6	D5	D4	D3	D2	D1	D0
SR(0)	DISLI3	DISLI2	DISLI1	DISAP4	DISAP3	DISAP2	DISAP1	DISAPA
SR(1)	DISTX2	DISTX1	DISTXA	DPRC4	DPRC3	DPRC2	DPRC1	DISLI4
SR(2)	ERSQ1	DISRX4	DISRX3	DISRX2	DISRX1	DISRXA	DISTX4	DISTX3
SR(3)	DFIFOE	DPFRM	DSQE	DMCV	ERXJAB	ERSQ4	ERSQ3	ERSQ2
SR(4)	RES	RES	RES	RES	RES	RES	RES	DMJLP
SR(5)	RES	RES	RES	RES	RES	RES	RES	RES

Table 18: Setup Register Bit Definitions

BIT	DEFINITION
DISAP(X)	Disable Auto-Partitioning on Port X
DISLI(X)	Disable Link Integrity on Port X (Twisted-pair ports only)
DPRC(X)	Disable Polarity Reverse detection and Correction on Port X (Twisted-pair ports only)
DISTX(X)	Disable Transmit on Port X
DISRX(X)	Disable Receive on Port X
ERSQ(X)	Enable Reduced Squelch on Port X (Twisted-pair ports only)
ERXJAB	Enable Receive JAB (Long Packet) (Global)
DMCV	Disable entering Tx Collision state on reception of Manchester Code Violation
DSQE	Disable Signal Quality Error to provide heartbeat (AUI port only)
DPFRM	Disable End-of-Frame checking for polarity correction (Global)
DFIFOE	Disable entering Tx Collision state on FIFO over/underflow condition (Global)
DMJLP	Disable MJLP counter (Global)
RES	Reserved. Must be set to 0.

Table 19: Packet Status Register Bit Assignments

	D7	D6	D5	D4	D3	D2	D1	D0
PSR(0)	COL2	COL1	COLA	RX4	RX3	RX2	RX1	RXA
PSR(1)	PR2	PR1	LLS4	LLS3	LLS2	LLS1	COL4	COL3
PSR(2)	SPA	AP4	AP3	AP2	AP1	APA	PR4	PR3
PSR(3)	LP3	LP2	LP1	LPA	SP4	SP3	SP2	SP1
PSR(4)	RXJABA	MJLP	LCOL4	LCOL3	LCOL2	LCOL1	LCOLA	LP4
PSR(5)	RES	RXCOL	MANCV	FIFOER	RXJAB4	RXJAB3	RXJAB2	RXJAB1

Table 20: Packet Status Register Bit Definitions

BIT	DEFINITION
RX(X)	Received Packet on Twisted-Pair Port 1-4 or on AUI Port
COL(X)	Transmit Collision of Twisted-Pair Port 1-4 or on AUI Port
LLS(X)	Link Loss State on Twisted-Pair Port 1-4 or on AUI Port
PR(X)	Polarity reversed on Twisted-Pair Port 1-4 or on AUI Port
AP(X)	Auto-Partition circuit isolated Twisted-Pair Port 1-4 or the AUI Port
SP(X)	Short Packet (less than 74 bits) on Twisted-Pair Port 1-4 or on AUI Port
LP(X)	Long Packet (more than 1.3ms) on Twisted-Pair Port 1-4 or on AUI Port
LCOL(X)	Late Collision on Twisted-Pair Port 1-4 or on AUI Port
MJLP	MAU Jabber Lockup Protection
RXJAB(X)	Receive Jabber Lockup Protection
FIFOER	FIFO overflow/underflow
MANCV	Manchester Code Violation
RXCOL	Receive Collision on the AUI Port
RES	Reserved (Not Used)
(X) means port X, which can be any of the four Twisted-Pair Ports or the AUI-Port	

10Base-T Port Operation

10Base-T Reception

Each LXT914 10Base-T port receiver acquires data packets from its twisted-pair input (DIP/DIN). An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. **No external filters are required.** The receive function is activated only by valid data streams (above the squelch level and with proper timing). If the differential signal at the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the port receiver enters the idle state.

Programmable Internal Squelch Level

The 10Base-T port receivers have two squelch levels; a normal level and a reduced squelch level (-4.5 dB). When used with low noise media such as shielded Twisted-Pair cabling, the reduced squelch level allows the loop-length of the network to be extended.

Polarity Detection and Correction

The LXT914 10Base-T ports detect and correct for reversed polarity by monitoring link pulses and end-of-frame sequences. A reversed polarity condition is declared when the port receives sixteen or more incorrect link pulses consecutively, or four frames with reversed start-of-idle sequence. In these cases the receiver reverses the polarity of the signal and thereby corrects for this failure condition. If the port enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity Testing is disabled, polarity detection is based only on received data.)

10Base-T Transmission

Each LXT914 10Base-T port receives NRZ data from the repeater core, and passes it through a Manchester encoder. The encoded data is then transmitted to the twisted-pair network (the DO circuit). The advanced integrated pulse shaping and filtering network produces the pre-distorted and pre-filtered output signal to meet the 10 Base-T jitter template. **An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. No external filters are required.** During idle periods, the LXT914 10Base-T ports transmit link integrity test pulses in accordance with the 802.3 10Base-T standard.

All data packets transmitted by the LXT914 contain a minimum of 56 preamble bits before the start of frame delimiter (SFD). In the Asynchronous mode, preamble regeneration takes place on the transmit side. In the Synchronous mode the preamble is regenerated on the receive side and distributed via the IRB. If the total packet is less than 96 bits including the preamble, the LXT914 extends the packet length to 96 bits by appending a Jam signal (1010...) at the end.

10Base-T Link Integrity Testing

The LXT914 fully supports the 10Base-T Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled unless disabled via the serial channel. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of data traffic. If no data packets or link integrity pulses are detected within 100 (±50) ms, the port enters a link fail state and disables its transmit function. The port will remain in the link fail state until it detects three or more data packets or link integrity pulses.

AUI Port Operation

AUI Reception

The LXT914 AUI port receiver acquires data packets from the network (DIP/DIN). The receive function is activated only by valid data streams above the squelch level. If the differential signal at the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the AUI receiver enters the idle state.

AUI Transmission

The LXT914 AUI port receives NRZ data from the repeater core, and passes it through a Manchester encoder. The encoded data is then transferred to the network (DOP/DON).

Collision Handling

A collision occurs when two or more repeater ports receive simultaneously, or when the AUI CIP/CIN signal is active. The LXT914 fully complies with the IEEE 802.3 collision specifications, both in individual and multi-repeater applications. In multiple-repeater configurations, collision signaling on the IRB allows all repeaters to share collision parameters, acting as a single large repeater.

$\overline{\text{IRCOL}}$ is a digital open-drain pin. $\overline{\text{IRCFS}}$ is an analog/digital port. The $\overline{\text{IRCOL}}$ and $\overline{\text{IRCFS}}$ lines are pulled up globally (ie., each signal requires one pull-up resistor for all boards). If there are eight 3-repeater boards in the system, all eight boards share a single pull-up resistor for $\overline{\text{IRCOL}}$ and a single pull-up resistor for $\overline{\text{IRCFS}}$. The global pull-up may be located on one of the boards, or on the backplane. The $\overline{\text{IRCFS}}$ line requires a precision (± 1 %) resistor.

The $\overline{\text{IRENA}}$, IRDAT and $\overline{\text{IRDEN}}$ lines are each pulled up locally (one pull-up resistor per board) if external bus drivers are used. If no bus drivers are used then only one global pull-up per signal is used..

Security Mode

The LXT914 security mode is fully transparent to the user. In the External management mode, the security feature is available for all four TP ports and the AUI port. In the Local mode, security is available for the TP ports only. (The SECAUI input is reassigned as FPS).

The security inputs are normally held low to disable the security feature. Any input can independently be pulled high to scramble the respective port for any given length of time. For applications which do not require security control, the SEC pins must be tied low.

The security mode pins are real time response inputs. This allows the board designer to screen the destination address with an application specific device and (on match of the destination address) to assert the security input to jam the respective port for the given frame. This real time detection and jam assertion method provides the flexibility to implement customer specific solutions. The destination address decoding and security signal assertion functions can be integrated into the external management device.

LED Display

The LED display interface consists of seven integrated LED drivers, one for each of the five network ports and two for common functions. Each pin provides a three-state pulsed output (+5V, high Z, and 0V) which allows multiple conditions to be monitored and reported independently. Figure 6 shows the LED Driver output conditions and Table 21 lists the repeater states associated with each condition. For example, using red and green LEDs for the twisted pair ports as shown in Figure 6, each TP port LED driver provides the following indications:

- Steady green when link integrity pulses are received
- Blinking green when data is transmitted
- Steady red when reverse polarity is detected
- Blinking red when data is received
- Alternating red and green when the port is auto-partitioned out.

Applications

Figure 7 (Sheets 1 through 4) shows a simple 12-port hub repeater application with 3 LXT914s. This application also provides two additional AUI ports - one D-connector and one coaxial port. The application shown uses the asynchronous backplane mode so no external backplane clock source is required.

Figure 7, Sheet 1, shows the XL93C46 EEPROM which downloads the setup parameters for all the LXT914s at initialization. (This EEPROM could be replaced with a simple resistor which would select the default conditions of all options.) A single 20 MHz crystal provides the SYSCLK for all three 914 chips. The LXT914 on Sheet 1 provides the AUI D-connector as well as four twisted-pair ports. Table 22 lists transformers tested for use with the LXT914.

Figure 7, Sheet 2, shows a second 914 with four TP ports and a coaxial port. A MD-001 coax transceiver is used to implement the port. Sheet 3 shows the third LXT914 with its four TP ports and indicator LEDs. The AUI port of the third 914 is not used. Sheet 4 of the schematic shows the LEDs for the remaining LXT914s, along with the LED operation table.

Table 21: Integrated LED Driver Indications

Condition	LEDTP 1-4	LEDAUI	LEDCF	LEDJM
1	Rx Link Pulse	Rx Jabber	FIFO Error	Manchester Code Violation
2	Tx Packet	Tx Packet	N/A	N/A
3	Reversed Polarity	Rx Collision	Collision	MAU Jabber Lockup Protection (MJLP)
4	Rx Packet	Rx Packet	N/A	N/A
5	Partitioned Out	Partitioned Out	N/A	N/A

Figure 6: Integrated LED Driver Indications

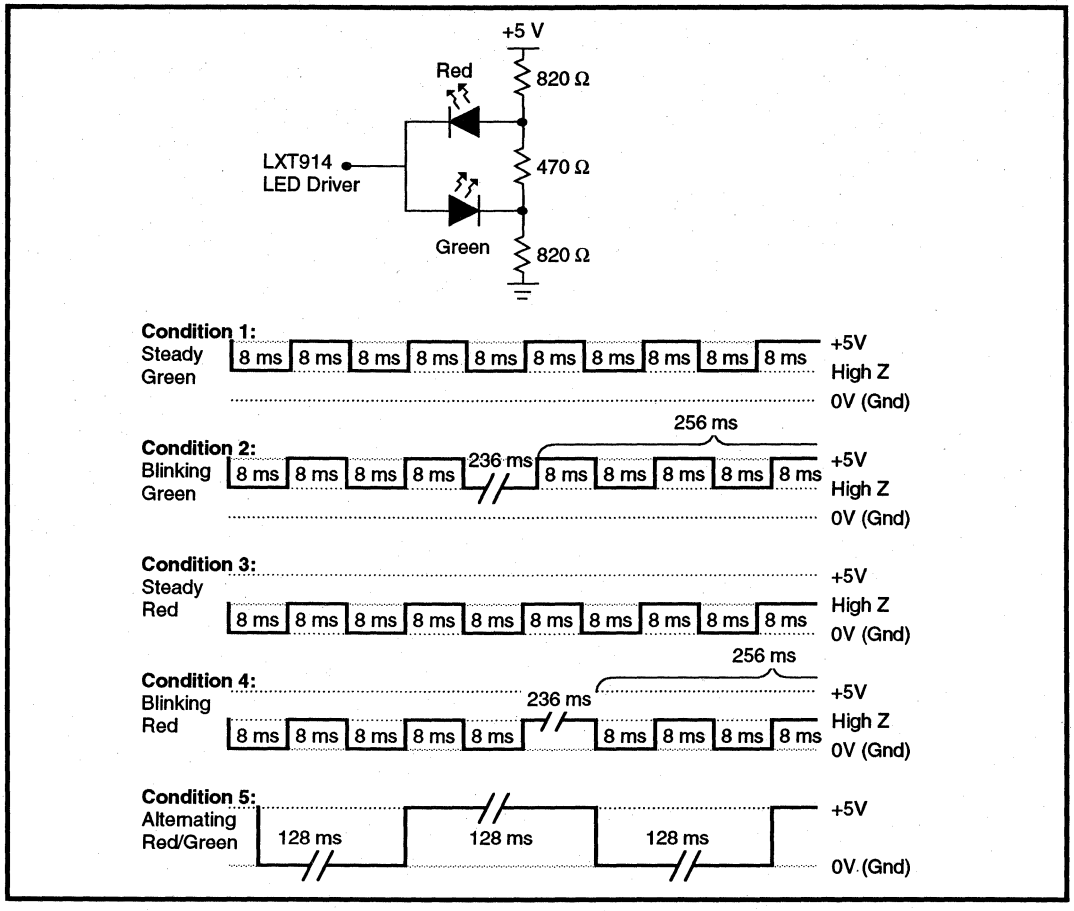
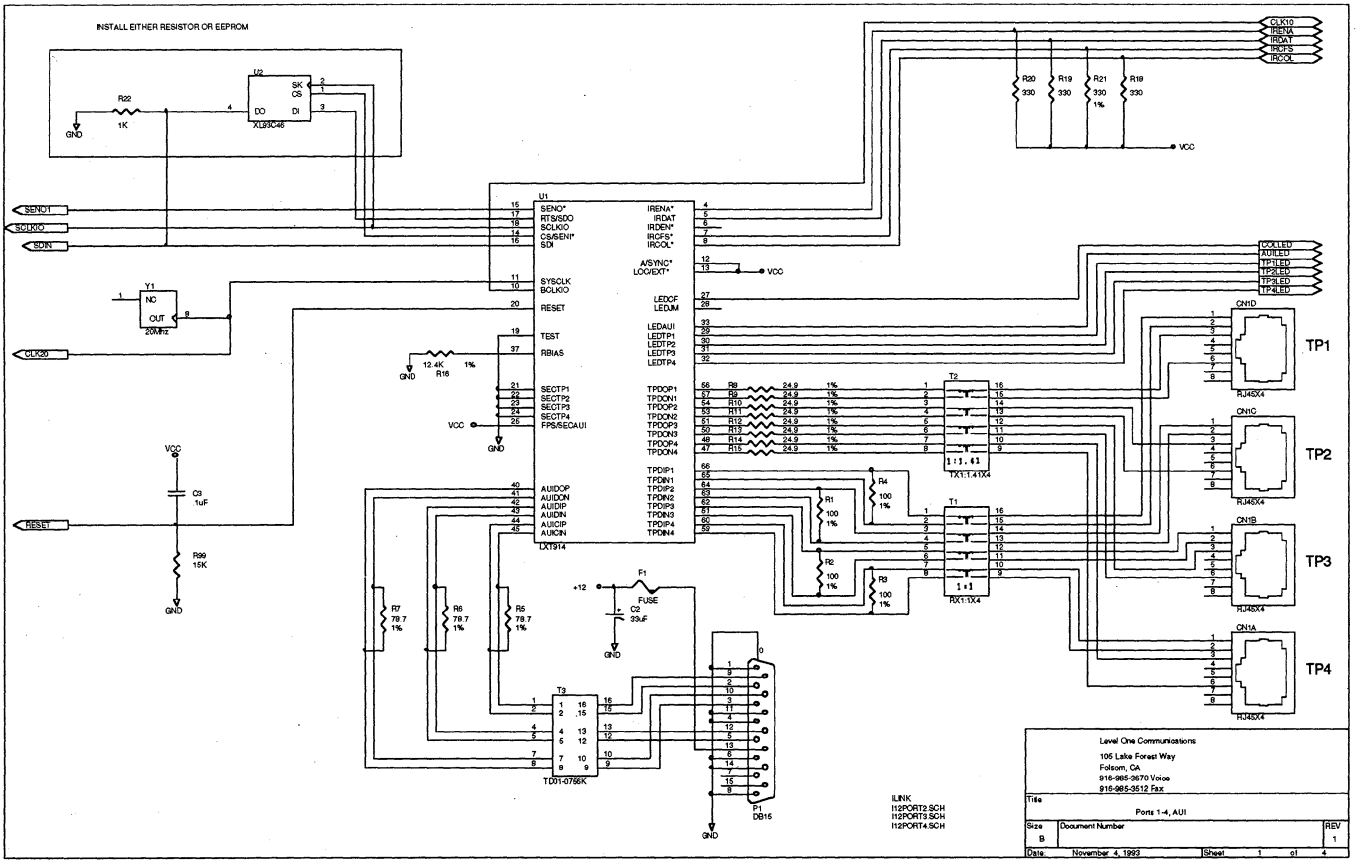


Table 22: Transformer Listing

Port	Manufacturer	Part Number	
Twisted-Pair		**Transmit**	**Receive**
	Bel Fuse	A553-5999-01	A553-5999-00
	FEE Fil-Mag	23Z339	23Z338
	HALO Electronics	TD54-1006L1	TD01-1006L1
	Nanopulse	5977	5976
	PCA	6038	6037
	Pulse Engineering	PE68008	PE68007
	Valor	PT34116	PT34117
AUI	FEE Fil-Mag	23Z90, SM23Z90	
	HALO Electronics	TD01-0756K, TG01-0756W	
	Pulse Engineering	PE64502	
	Valor	LT6030, SM6030	

Figure 7: 12-Port Application Schematic (Sheet 1 of 4)



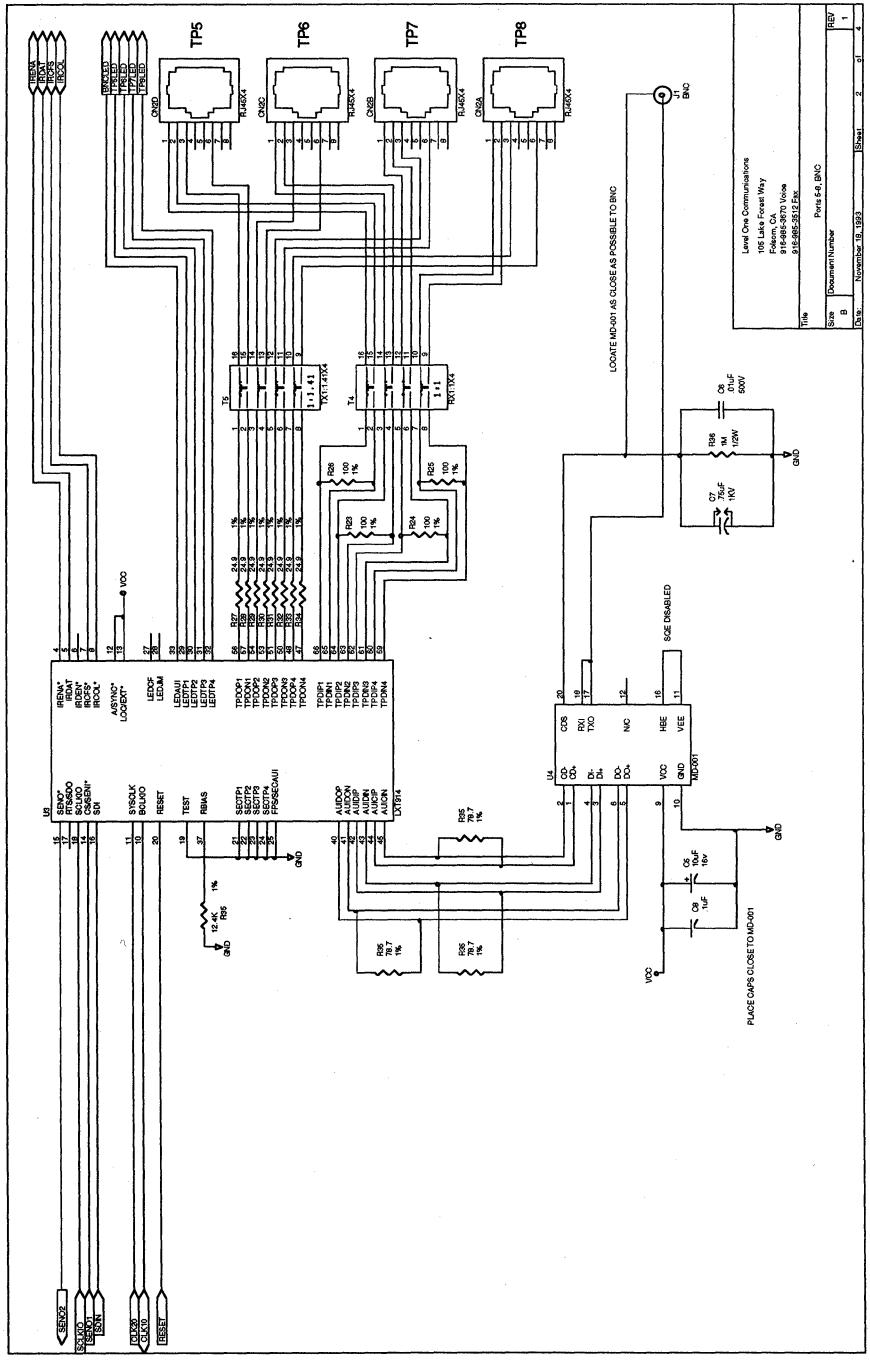


Figure 7: 12-Port Application Schematic (Sheet 2 of 4)

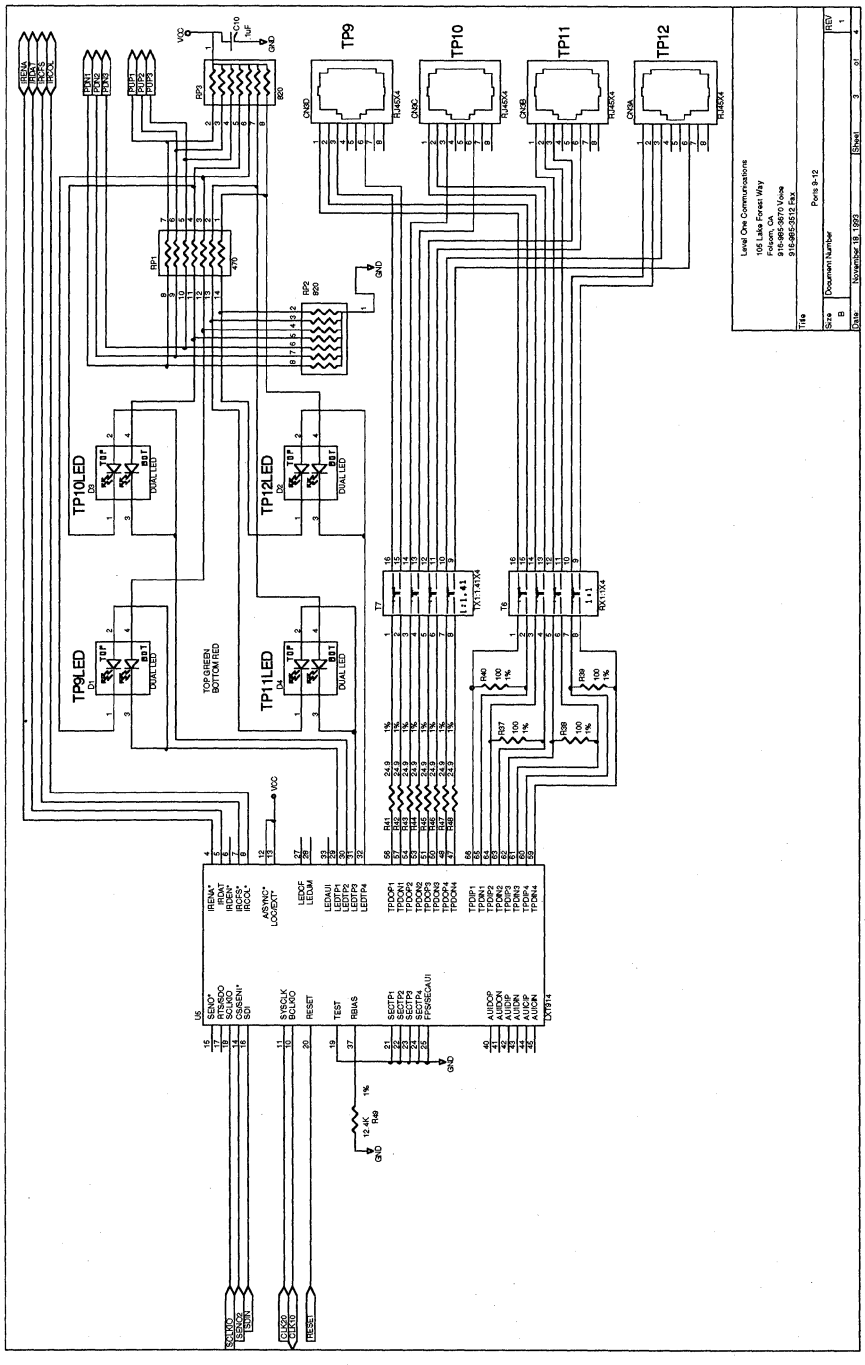
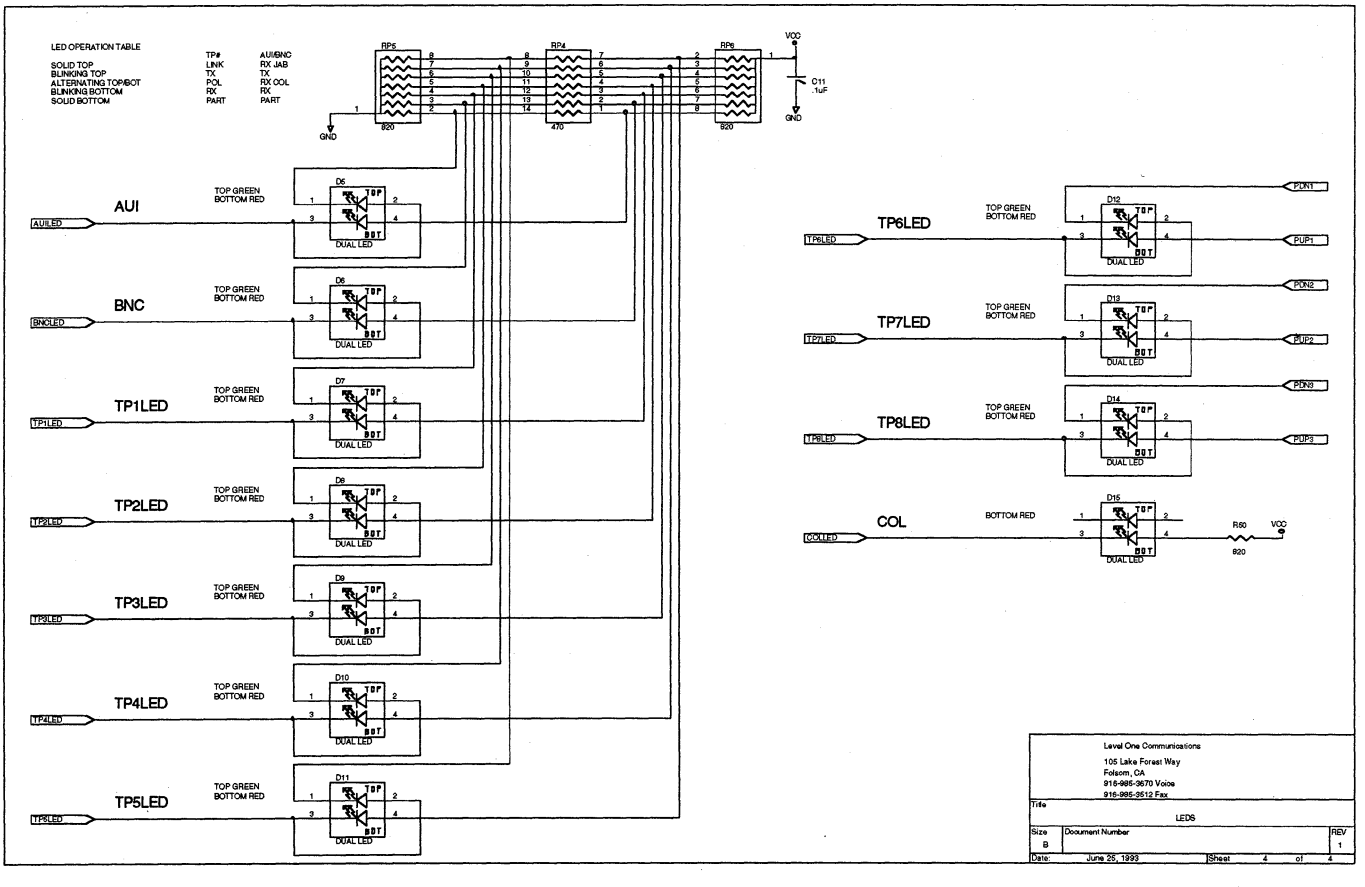


Figure 7: 12-Port Application Schematic (Sheet 3 of 4)

Figure 7: 12-Port Application Schematic (Sheet 4 of 4)



Wide Area Networking Products

1994 Communications Data Book

LEVEL ONE®

Standard Product
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LXT400

All Rate, Extended Range Switched 56 / DDS Transceiver

General Description

The LXT400 is an integrated line interface circuit for Switched 56 (SW 56) and Digital Data Service (DDS), compatible with any combination of 19 to 26 AWG cable. The LXT400 operates at any of 14 preset data rates from 2.4 kbps to 72.0 kbps, providing appropriate transmit pulse shaping, receive signal detection and timing recovery at the metallic interface between the carrier and the customer installation. The LXT400 diagnostic features including loopback, line status and equalizer monitor outputs, while conforming to AT&T, ANSI and Bellcore specifications.

The LXT400 transmit section includes switched capacitor filters, continuous reconstruction filters, and a 50% AMI encoder. The AMI pulse is synchronized with the transmit clock.

The LXT400 receive section performs line equalization, data extraction and timing recovery. The LXT400 has a BER of less than 10^{-7} with up to 49 dB of cable attenuation at the Nyquist frequency for 56 and 72 kbps, and 40 dB at the lower rates. The LXT400 is an advanced CMOS device which requires only a single +5V power supply.

Features

- Integrated transmitter, receiver and timing recovery on a single CMOS chip
- Transparent to framing and coding
- Receive equalizer filters allow data recovery from signals with up to 40 dB of attenuation at the Nyquist frequency, at line rates below 56 kbps, and up to 49 dB at the 56 and 72 kbps line rates
- Single 4.096 MHz crystal or master clock input
- Digital back-end loopback
- Equalizer output monitor pin
- Line status (loop length, RLOS, etc.) available for customer maintenance purposes
- Low power consumption (200 mW typical)
- Available in 28-pin DIP
- Single 5 V only CMOS technology

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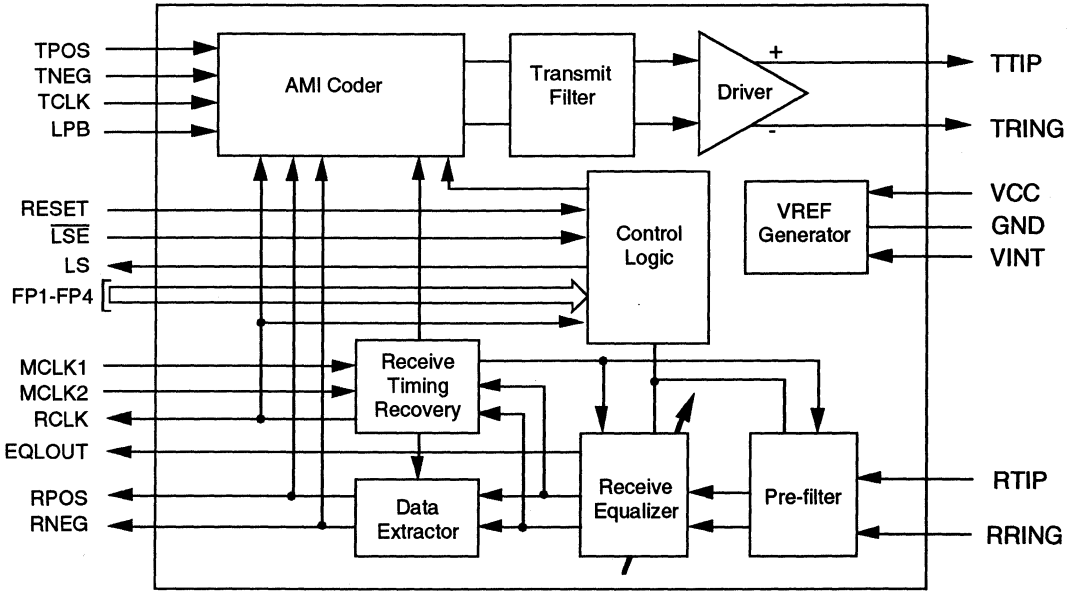
Figure 1: LXT400 Block Diagram



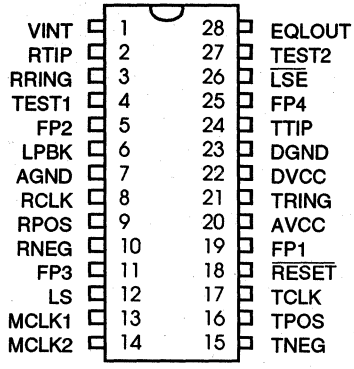


Table 1: Data Rate Programming

FP4	FP3	FP2	FP1	Data Rate [1]
0	0	0	0	2.4 kbps
0	0	0	1	3.2 kbps
0	0	1	0	4.8 kbps
0	0	1	1	6.4 kbps
0	1	0	0	9.6 kbps
0	1	0	1	12.8 kbps
0	1	1	0	19.2 kbps
0	1	1	1	25.6 kbps
1	0	0	0	56.0 kbps
1	0	0	1	72.0 kbps
1	0	1	0	3.5 kbps
1	0	1	1	7.0 kbps
1	1	0	0	14.0 kbps
1	1	0	1	28.0 kbps

Table 2: Pin Descriptions

Pin	Sym	I/O	Name	Description
1	VINT	I	Intermediate Voltage Reference	Reference voltage used for internal analog circuits. This pin must be connected through a 1 kΩ resistor (Rv) to the center node between the two termination resistors, Rr, as shown in Figure 12.
2 3	RTIP RRING	I	Receive Tip Receive Ring	Receive data input pair. RTIP and RRING are a fully differential input for the receive line interface.
4	TEST1	I	Test 1	Factory Test Pin. Leave unconnected.
5 19 11 25	FP2 FP1 FP3 FP4	I I I I	Frequency Programming Inputs 1 thru 4	The LXT400 data rate is set by the logic levels present at the FP1 through FP4 inputs as shown in Table 1, above. For operation at 64 kbps and other alternate data rates, refer to Application Note AN-30.
6	LPBK	I	Loopback	When set to logic 1, activates digital back-end loopback.
7	AGND	-	IC Ground	IC ground for all circuits except the transmit driver.
8	RCLK	O	Recovered Clock	Clock recovered from signal input at RTIP and RRING.
9 10	RPOS RNEG	O O	Receive Data Positive and Negative	Receive data outputs. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. A signal on RNEG corresponds to a negative pulse on RTIP and RRING. Both outputs are stable and valid on the falling edge of RCLK, and are never high simultaneously.
12	LS	O	Line Status Output	An 8-bit serial word indicating loop length, line loss, loss of signal (LOS), etc. LS is valid on the rising edge of RCLK and goes to a high impedance state when LSE is high. If LSE is tied low, the LS output represents LOS only.
13 14	MCLK1 MCLK2	I I	Master Clock 1 Master Clock 2	The required 4.096 MHz input may be provided by a crystal connected across these pins, or by a digital clock connected to MCLK1. If a clock is provided on MCLK1, MCLK2 must be left unconnected.

Note 1. For information on 64 kbps operation and other alternate data rates, refer to Application Note AN-30.

Table 2: Pin Descriptions continued

Pin	Sym	I/O	Name	Description
15 16	TNEG TPOS	I I	Transmit Data Negative and Positive	Inputs are sampled at the halfway point between rising edges of TCLK. AMI pulses are encoded as follows: TPOS TNEG Transmit Signal 0 0 Space 0 1 Negative Pulse 1 0 Positive Pulse 1 1 Space
17	TCLK	I	Transmit Clock	Transmit clock. TPOS and TNEG transitions must be coincident with the rising edges of TCLK.
18	$\overline{\text{RESET}}$	I	Reset	**Hardware reset pin. Must be pulsed low on power-up to initialize all internal circuits. Must also be pulsed low after changing the baud rate and after forcing or releasing any loopback condition.**
20	AVCC	I	IC Power	IC power supply for all circuits except the transmit driver. +5 V (±5%).
21 24	TRING TTIP	O O	Transmit Ring Transmit Tip	Differential driver outputs. Designed to drive the 135 Ω twisted-pair cable through transmit line interface shown in application diagram, Figure 7.
22	DVCC	I	Driver Power	Transmit driver power supply. +5 V (±5%).
23	DGND	-	Driver Ground	Transmit driver ground.
26	$\overline{\text{LSE}}$	I	Line Status Enable	Active low enable for the LS serial port. This pin must transition from high to low to read LS serial data. $\overline{\text{LSE}}$ is sampled on the rising edge of RCLK.
27	TEST2	I	Test 2	Analog test pin. Must be tied to ground.
28	EQLOUT	O	Equalizer Output Monitor	Monitors Equalizer. Must be left open when not used.

Table 3: Absolute Maximum Ratings

Parameter		Min	Max	Units
DC supply -	AVCC referenced to AGND	- 0.3	+ 6.0	V
	DVCC referenced to DGND	- 0.3	+ 6.0	V
	DVCC referenced to AVCC	- 0.3	+ 0.3	V
	DGND referenced to AGND	- 0.3	+ 0.3	V
Input voltage, any pin [1,2]		AGND - 0.3	AVCC + 0.3	V
Input or output diode current, any pin [2]		-	± 20	mA
Continuous output current, any pin [2]		-	± 25	mA
Continuous current, VCC or GND pins		-	± 50	mA
Storage temperature		- 40	+ 150	°C

[1] TTIP and TRING are referenced to DVCC and DGND.
[2] Except supply pins.

Table 4: Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
DC supply	AVCC/DVCC	4.75	5.0	5.25	V
Ambient operating temperature	T_A	-40	-	+85	°C

Table 5: AC Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Notes
Receive Timing (Figure 2)						
RCLK period	t_{PR}	–	1/fb	–	ns	
RCLK pulse width high	t_{RWH}	1/(2 fb) -150	1/(2 fb)	1/(2 fb) + 150	ns	
RPOS/RNEG delay from RCLK rising edge	t_{DP}	–	–	200	ns	2
Transition time on any digital output	t_{TO}	–	10	20	ns	2
Transmit Timing (Figure 3)						
TCLK period	t_{PT}	–	1/fb	–	µs	
TCLK pulse width high	t_{TWH}	400	–	–	ns	
TPOS/TNEG setup to TCLK rising edge	t_{TSU}	-400	–	400	ns	
TPOS/TNEG hold time from the next rising edge of TCLK	t_{TH}	-400	–	400	ns	
Transition time on any digital input	t_{TI}	–	–	40	ns	
LS Serial Port Timing (Figure 4)						
LS delay from RCLK falling edge	t_{LSP}	–	–	200	ns	2
$\overline{LSE}$ setup to RCLK rising edge	t_{LSU}	200	–	–	ns	
$\overline{LSE}$ hold time from RCLK falling edge	t_{LSH}	0	–	–	ns	
$\overline{LSE}$ low to low Z state	t_{LZ}	–	–	100	ns	
$\overline{LSE}$ high to high Z state	t_{HZ}	–	–	100	ns	
MCLK and Reset Timing (Figure 5)						
MCLK1 input frequency	f_{MCLK}	–	4.096	–	MHz	
MCLK1 frequency tolerance - at OCU	f_{TOCU}	–	–	± 50	ppm	
- at DSU @ 2400 bps	f_{TDSU}	–	–	± 80	ppm	
- at DSU @ all other rates	f_{TDSU}	–	–	± 100	ppm	
MCLK pulse width high	t_{MWH}	98	122	146	ns	
RESET pulse width low	t_{RWL}	1000	–	–	ns	
General						
Input capacitance	C_{IN}	–	7	–	pF	
TCLK jitter at DSU with respect to RCLK	t_{JIT}	–	–	2	% t_{PR} at DSU	
RCLK isochronous distortion at DSU	r_{JIT}	–	–	5	% t_{PT} at OCU	
Transmit output jitter with respect to TCLK	o_{JIT}	–	–	3	% t_{PT} at DSU	
Transmit pulse amplitude at TTIP/TRING						
- at 9.6 and 12.8 kbps	A_T	1.44	1.55	1.75	V	3
- at all other rates	A_T	2.56	2.74	2.92	V	3

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Measured with 15 pF load.
[3] The instantaneous peak amplitude of an isolated pulse (i.e.: a mark between two spaces) into a 270 Ω resistive load.

Table 6: DC Electrical Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Supply current (transmitting spaces)	I_{CC}	–	40	60	mA	270 Ω resistor across TTIP and TRING
Supply current (transmitting all marks)	I_{CC}	–	47.5	60	mA	270 Ω resistor across TTIP and TRING
Input low voltage	V_{IL}	–	–	0.8	V	Digital inputs
Input high voltage	V_{IH}	2.0	–	–	V	Digital inputs
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
Output low voltage	V_{OL}	–	0.2	–	V	I_{OL} < 10 µA
Output high voltage	V_{OH}	2.4	–	–	V	I_{OH} = 0.4 mA
Output high voltage	V_{OH}	–	4.5	–	V	I_{OH} < 10 µA
Input leakage current	I_{IL}	-40	–	40	µA	$0 < V_{IN} < V_{CC}$

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

4

Figure 2: Receive Digital Timing

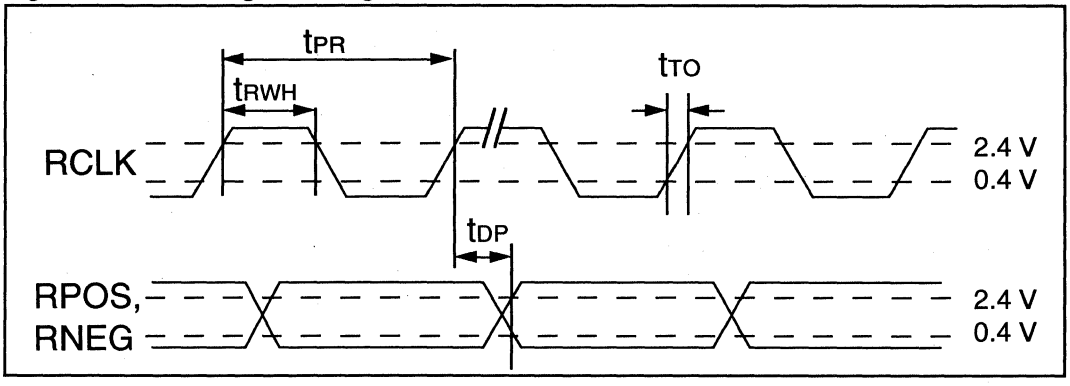
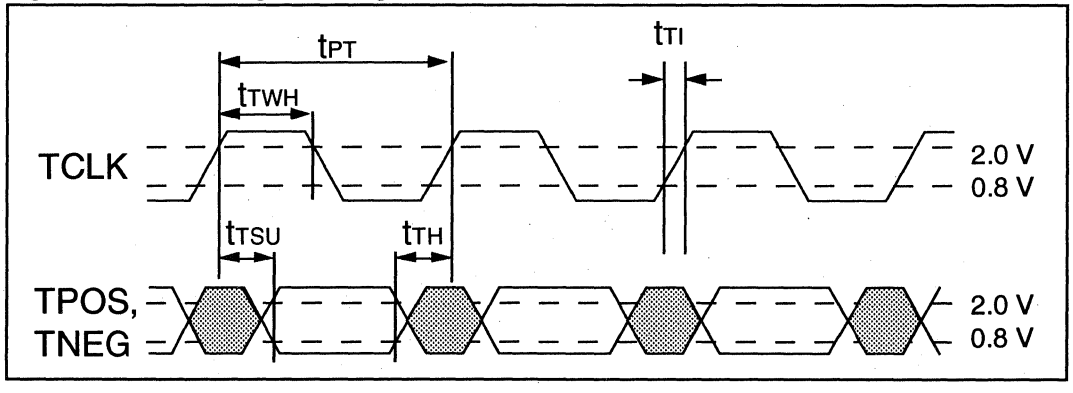


Figure 3: Transmit Digital Timing



General Description

The LXT400 comprises three basic sections: transmit, receive and control logic.

The transmit section includes a 50% AMI encoder, a programmable switched-capacitor low-pass filter, a low-pass notch filter, a transmit timing resynchronizer and a continuous reconstruction filter. An on-chip CMOS driver is also incorporated to drive a 135 Ω line through a transformer.

The receive section includes pre-filters and line equalizers, and the timing recovery and data extraction blocks. An internal digital phase-locked loop (DPLL) is used in conjunction with the MCLK input to synchronize the recovered clock and data.

The control logic block initializes the transceiver, selects receive filters and reports status information on the serial port. Control logic inputs FP1 through FP4 determine the data rate in accordance with Table 1. The control logic executes the initialization procedure upon automatic re-synchronization or external $\overline{\text{RESET}}$. Filter selection optimizes the receive signal-to-noise ratio (SNR) by matching the filter in the equalizer section to the strength of the received signal (a function of loop length/line loss). The control logic block also reports receiver status, estimated line length (as indicated by filter selection) and a receive loss of signal (RLOS) alarm on the serial port.

Functional Description

Initialization

Upon power-up, or after changing the baud rate or loopback condition of the line interface, a $\overline{\text{RESET}}$ pulse is required to initialize the LXT400. On receipt of the $\overline{\text{RESET}}$ pulse, the LXT400 executes an iterative cycle of level detection and offset cancellation to select the appropriate equalizer settings for the received signal. Receiver initialization can be monitored on the serial channel. When received data has a 50% ones density, full operation is achieved within one

Figure 4: LS Serial Port Timing

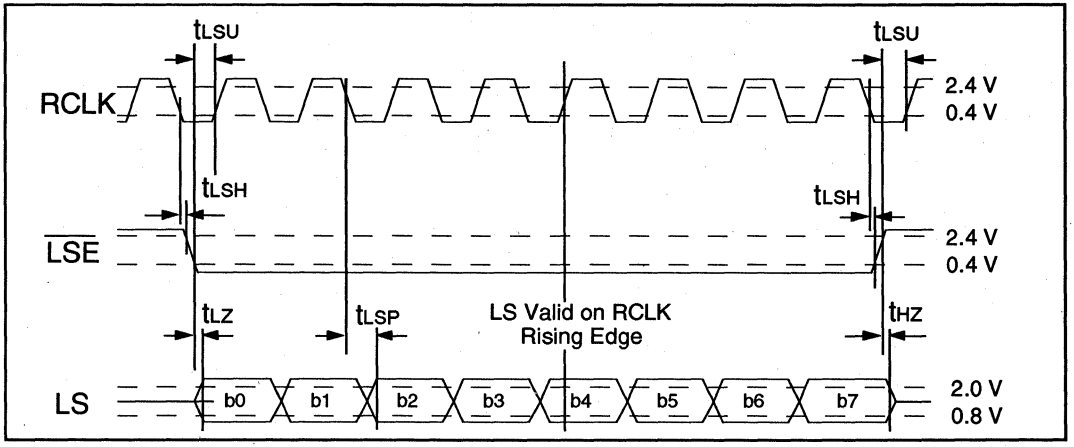
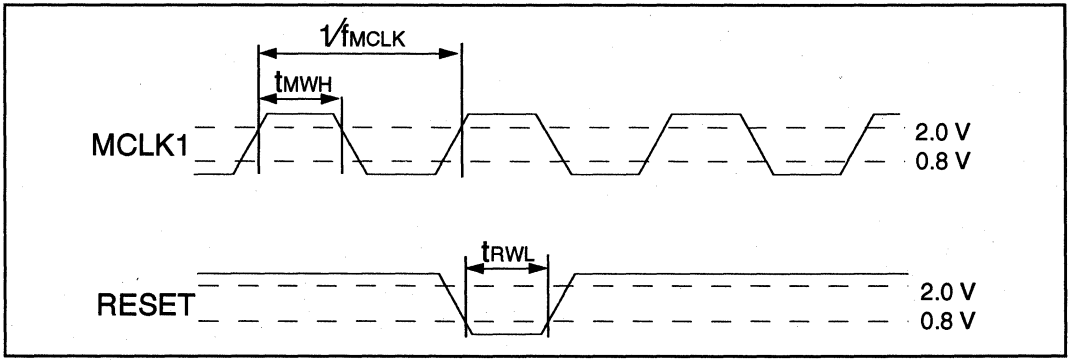


Figure 5: MCLK and RESET Timing



second after $\overline{\text{RESET}}$. Under the minimum ones density condition specified in Table 7, full operation is achieved within eight seconds after $\overline{\text{RESET}}$. Correct initialization assumes the presence of an AMI-coded signal at the RTIP and RRING inputs. The LXT400 will not correctly initialize unless a stable signal which meets the network interface specifications of AT&T Pub 62310 is present at the RTIP and RRING inputs during the entire initialization process. The RPOS/RNEG outputs are not valid until full operation is achieved. During offset cancellation, the RPOS/RNEG outputs do not adhere to the AMI rule. However, once initialized (assuming that a proper baud rate is selected), RPOS and RNEG never simultaneously output a logic 1.

A hardware reset is required after any of the following changes in transceiver configuration:

1. A change in Baud Rate
2. A change in the local analog loopback configuration
3. A local change in the line upon which the transceiver is communicating (for example, configurations for changing lines in a "1 for n" redundancy scheme).

Automatic re-initialization may be triggered by changes in received signal strength as follows:

- If received signal strength increases by more than about 6 dB after full operation is achieved, automatic re-initialization occurs.
- If received signal strength decreases by more than about 4 dB, re-initialization occurs. If the decrease in received signal strength exceeds 6 dB, the LXT400 reports an LOS condition and performs an automatic re-initialization.

The time required to achieve full operation after reinitialization, is the same as required for power-on initialization (i.e., 1 second max with 50% ones density, 8 seconds under minimum ones density conditions). Reinitialization is not triggered by impulse noise events.

Transmission

TPOS and TNEG must have transitions coincident with the rising edges of TCLK. The transmit section generates a 50% AMI pulse according to the pulse encoding rules, which is synchronized with the TCLK input. In DSU applications, RCLK is typically routed back into the TCLK input. The instantaneous baud period varies with the receive DPLL phase adjustments, however, the pulse duty cycle is maintained at 50% of the nominal baud period by internal re-synchronization to TCLK. The AMI pulse is then processed through a set of frequency dependent filters.

Initial filtering at all rates is accomplished by a programmable, switched-capacitor, low-pass filter. This filter is a single-pole type with the pole set at 1.3 times the bit rate (as determined by inputs FP1 - FP4).

For data rates of 2.4, 3.2, 4.8, 6.4, 9.6 and 12.8 kbps, the filtered pulses go through an additional low-pass notch filter. The notch filter is required to protect other DDS services with specific band requirements, and provides the attenuation listed in Table 8. The additional rejection requirement is weighted within each band by "C-Message" weighting over double speech sidebands around a carrier in the middle of each band (28 kHz and 78 kHz). The C-Message weighting function is graphed in Figure 6.

Table 7: Ones Density Requirements

Data Rate (kbps)	Minimum Average Ones Density
2.4, 4.8, 9.6, 19.2	1 / 12
3.2, 6.4, 12.8, 25.6	1 / 16
56.0	1 / 14
72.0	1 / 18
3.5, 7.0, 14.0, 28.0	≈ 1 / 16

Figure 6: C-Message Weighting

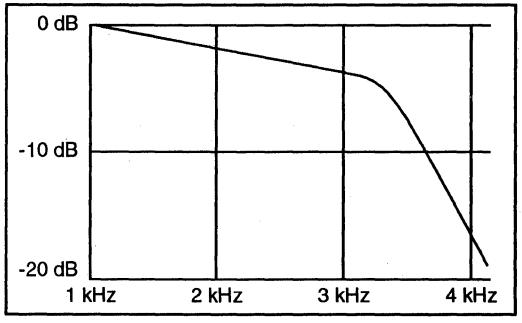


Table 8: Notch Filter Attenuation

OCU/Loop Data Rate (kbps)	Customer (Primary Channel) Data Rate (kbps)	Rejection Band 24 - 32 kHz	Rejection Band 72 - 80 kHz
2.4 or 3.2	2.4	5 dB	1 dB
4.8 or 6.4	4.8	13 dB	9 dB
9.6 or 12.8	9.6	17 dB	8 dB

Depending on the data rate, the frequency template extends to different limits as shown in Table 9. (An alternate notch filter is used for data rates of 3.5 and 7.0 kbps.) The single pole, low-pass filter would maintain the frequency within ± 5%. The notch filter attenuation is added to this.

A continuous filter, common to all data rates, is the final stage. The continuous filter removes high frequency components which remain after processing by the low-pass filter stages. The pulse is then applied to the line driver for transmission onto the twisted-pair line.

Table 9: Frequency Limits per Data Rate

Data Rate (kbps)	Upper Frequency Limit (kHz)
2.4 (3.2)	100
4.8 (6.4)	150
9.6 (12.8)	150
19.2 (25.6)	300
56.0 (72.0)	1750
3.5	100
7.0	150
14.0	150
28.0	1200

Reception

RTIP and RRING inputs are differentially detected, then processed through the pre-filters and equalizer section. The continuous pre-filter removes high frequency noise and prevents aliasing problems for the switched capacitor (SC) line equalizers which follow. Pulse reshaping is achieved by the receive equalizer, which consists of an SC step equalizer and an adaptive decision feedback equalizer (DFE). The DFE eliminates residual inter-symbol interference (ISI) due to echoing by multiple bridged tap connections and the quantized frequency responses of the SC step filters. The DFE is continuously adapted to compensate for ISI due to time varying line characteristics such as temperature, humidity and age. Nine different filter selections based on signal strength are available.

Changes in Received Signal Strength

During initialization, the LXT400 selects filters appropriate to the strength of the received signal. After initialization, the LXT400 continually monitors the receive signal strength to ensure the optimum signal/filter match. Data reception is not affected by impulsive noise events or by slow changes in signal amplitude, such as may be caused by temperature and humidity changes on the line. (The maximum constant rate of change which the LXT400 can track is 6 dB per minute.) However, instantaneous "step" changes (see Figure 7) may temporarily interfere with data reception. Step changes may be due to sudden changes in loop loss, far end transmitter output, etc.

After normal operation has been established, an instantaneous single-step change may cause one of three conditions, as shown in Figure 8.

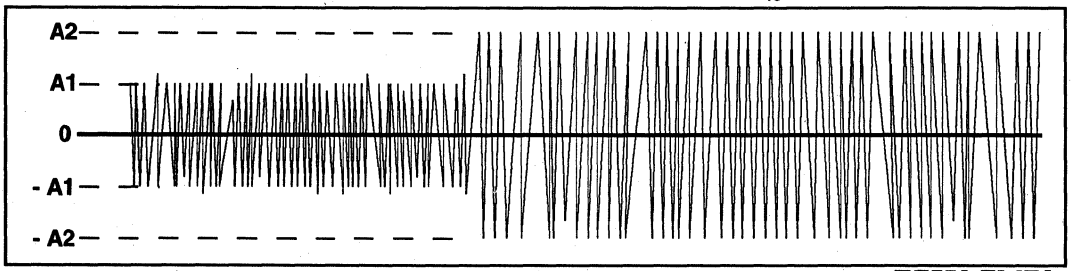
Under Condition 1, the LXT400 automatically adapts to minor step changes in signal strength (assuming that the new input is a valid DDS signal).

Under Condition 3, the LXT400 responds to significant step changes by re-initializing.

Condition 2, while unlikely to occur in an actual DDS implementation, may be observed in the laboratory due to artificial line simulators. Condition 2, which results from a 6 - 20 dB step increase in received signal strength, may result in a signal/filter mismatch. This condition is characterized by excessive bipolar violations (BPVs) which can be observed on RPOS and RNEG. External signal quality detection circuitry can be used to detect excessive BPVs that are not recognized as standard DDS BPV code words. Upon detection of unrecognized BPVs, the user may force a reset on the LXT400 to resume error-free operation.

Under normal operating conditions, step changes in received signal strength are all under local control. Thus, the user can reset the LXT400 once the new receive signal has stabilized at the chip inputs. Remote changes typically involve disconnecting one line and re-connecting another line of

Figure 7: Step Changes in Received Signal Strength = 20 $\log_{10}$ (A_2/A_1) dB



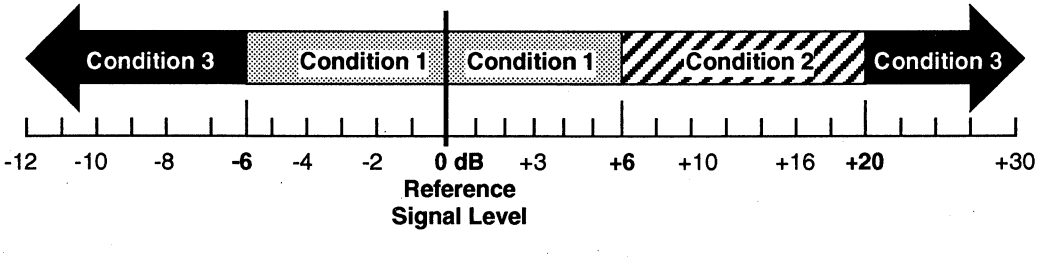
different length. These changes trigger the RLOS report and automatic re-initialization. Any remote changes in line length or transceiver configuration are beyond the local user's control. Remote changes in baud rate are not detected.

Receive Loss of Signal

RLOS goes high when more than 32 consecutive zeros are received, caused either by a true loss of signal, or a signal strength drop greater than 6 dB. The LXT400 automatically re-initializes when RLOS goes high. Figure 9 shows the RTIP/RRING input and RLOS output timing relationships for a true loss of signal. When signal energy returns to the chip input, the LXT400 executes one full activation cycle in the presence of this signal. The result is that RLOS will remain high for a period of time (0.13 s < tH < 16 s) after signal energy reappears.

Figure 10 shows the RTIP/RRING input timing and RLOS output timing relationship for a signal strength decrease greater than 6 dB. In this case, RLOS will go high for a time 0.26 s < tP < 16 s.

Figure 8: Conditions Based on Changes in Received Signal Strength



Condition 3: > 20 dB Increase or > 6 dB Decrease.
Automatic re-initialization. No action required. If the condition is due to a signal strength decrease, the LXT400 also reports RLOS.

Condition 1 : 0 - 6 dB Increase or Decrease.
Automatic compensation (may re-initialize). May pass erroneous data temporarily before resuming error-free performance. No action required.

Condition 2 : 6 - 20 dB Increase.
Re-initialization not guaranteed. The device may continue to pass erroneous data until reset. RESET pulse required to ensure accurate data reception.

Figure 9: RLOS Timing for a True Loss of Signal

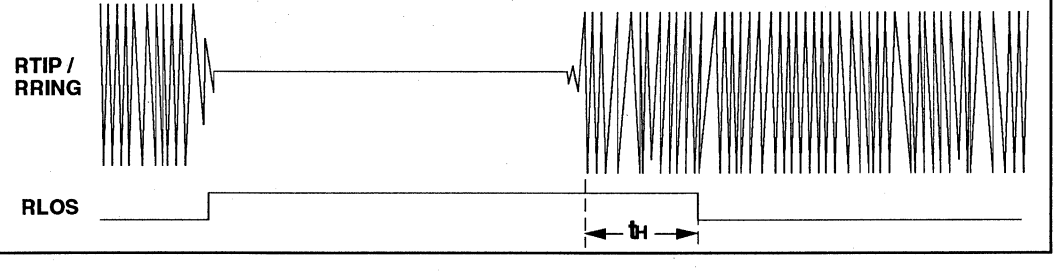
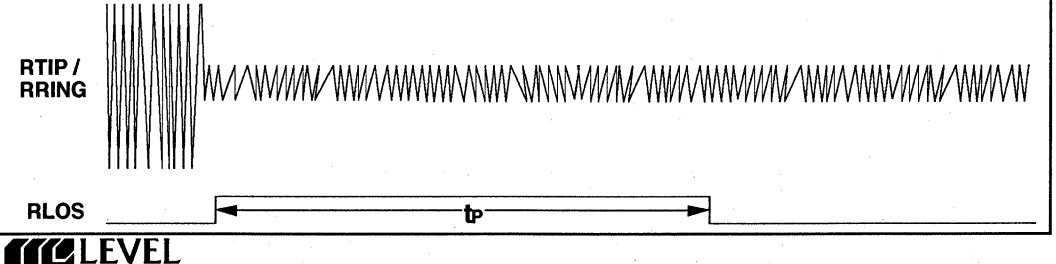


Figure 10: RLOS Timing for a Drop in Signal Strength > 6 dB



Timing Recovery

The timing recovery circuit uses a rate synchronizer to generate a high frequency internal clock from the MCLK input. A DPLL is used to synchronize this internal clock to the received data pulses. The output clock from the DPLL is divided down to generate RCLK and all other required clocks (except TCLK which is an external input).

Data Extraction

The data extraction block provides RPOS and RNEG outputs. A positive differential pulse received between RTIP and RRING results in a logic 1 on RPOS. A negative differential pulse between RTIP and RRING results in a logic 1 on RNEG. RPOS and RNEG are output at the received data rate and are valid on the falling edge of RCLK.

Receiver operation is not affected by the data patterns, provided the ones density requirements of Table 7 are met with no more than 26 consecutive zeros. RLOS is declared after 32 consecutive zeros. However, the RCLK output remains synchronized to the RTIP/RRING input for more than 40 consecutive zeros. Bipolar violations are received properly. The bipolar violation coding rule that successive violations be of alternating polarity must be followed. However, if this rule is temporarily broken (due to channel noise, etc.), long term LXT400 data reception will not be adversely affected.

Loopback Operation

When the LPBK pin is set to a logic 1, the recovered data and clock are sent back through the transmit section and onto the line interface, as well as being output on the RPOS/RNEG and RCLK pins. TPOS/TNEG and TCLK inputs are ignored in the loopback mode.

Serial Port Operation

The line status (LS) output is an 8-bit serial word enabled by pulling LSE low for 8 bit-periods as shown in Figure 4. Bit assignments are listed in Table 10. Approximate line loss and loop length (based on received signal strength/filter selection, assuming far-end pulse transmission compliant with AT&T Pub 62310 or T1E1/90-051) are reported via bits b0 through b3 as listed in Table 11. Bits b4 through b6 indicate the receiver activation state. Bit b7 is the RLOS alarm.

Figure 11 shows the serial output for a typical LXT400 initialization sequence. Bits b0 - b3 report filter selection and bits b4 - b6 report receiver status. Bit b6 toggles to indicate that the receiver is alternating between offset cancellation (b6 - b4 = 100) and receive level detection (b6 - b4 = 000). The receiver starts with the highest-gain filter (b3 - b0 = 0111), cancels systematic voltage offset at the filter output, and then detects the receive signal level at the filter output. If the signal exceeds the threshold for that filter, the LXT400 steps down to the filter with the next-highest gain (b3 - b0 = 1000). This process is repeated until the receive signal level does not exceed the filter threshold.

Once the appropriate filter is selected, the receiver phase-locked loop (PLL) and slicer levels converge to match the receive signal for optimum SNR. During receiver convergence (b6 - b4 = 001), the PLL adapts to sample the peak of the receive pulses and the slicer level adapts to the midway point between zero and the pulse peak voltage. Once convergence is complete, the LXT400 begins full operation (b6 - b4 = 010).

Table 10: LS Word Bit Assignments

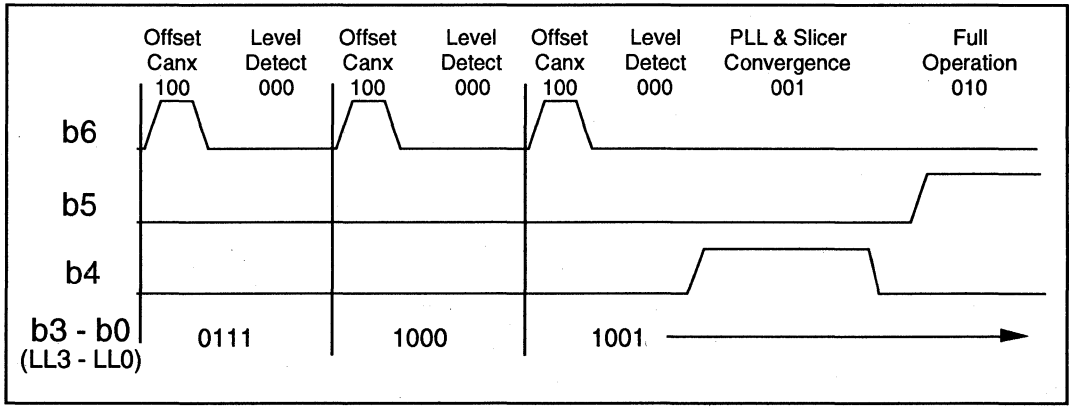
Bit #	Name	Description
b0	LL0	Loop Length Indication, bit 0
b1	LL1	Loop Length Indication, bit 1
b2	LL2	Loop Length Indication, bit 2
b3	LL3	Loop Length Indication, bit 3
b4	S1	Receiver Converging when high
b5	S2	Full Operation when high
b6	S0	Level Detection when high
b7	RLOS	Receive Loss of Signal when high

Table 11: LS Loop Length Bits

Rate	Insertion Loss in dB / Line Range in km (24 AWG PIC, no bridged taps) for LL3 - LL0								
kbps	0111	1000	1001	1010	1011	1100	1101	1110	1111
2.4	N/A	> 38 / > 21.0	38 / 21.0	33 / 17.3	27 / 13.4	22 / 9.6	18 / 6.2	13 / 3.5	7 / 1.8
3.2	N/A	> 38 / > 18.6	38 / 18.6	33 / 15.6	28 / 12.6	22.5 / 9.6	17.5 / 6.5	12.5 / 3.7	7 / 1.8
4.8	N/A	> 38.5 / > 15.8	38.5 / 15.8	33 / 13.2	27 / 10.6	22 / 8.0	16 / 5.3	12 / 2.8	7 / 1.3
6.4	N/A	> 38.5 / > 14.1	38.5 / 14.1	33 / 11.9	27.5 / 9.8	22 / 7.5	17 / 5.3	12.5 / 3.2	7 / 1.5
9.6	N/A	> 37 / > 11.4	37 / 11.4	32 / 9.6	27 / 7.9	22 / 6.2	16 / 4.3	11 / 2.6	5 / 1.1
12.8	N/A	> 39 / > 10.8	39 / 10.8	33 / 9.1	27.5 / 7.4	22 / 5.8	16 / 4.1	11 / 2.9	5 / 1.0
19.2	N/A	> 39 / > 9.2	39 / 9.2	33 / 7.8	27.5 / 6.4	22 / 5.0	16 / 3.5	11 / 2.1	4 / 0.8
25.6	N/A	> 38 / > 8.3	38 / 8.3	33 / 7.0	27.5 / 5.8	22 / 4.5	16 / 3.2	10.5 / 1.9	4 / 0.7
56.0	> 47.5 / > 8.0	47.5 / 8.0	41.5 / 6.9	35 / 5.8	29 / 4.8	22.5 / 3.8	17 / 2.7	10.5 / 1.6	4 / 0.5
72.0	> 48 / > 7.5	48 / 7.5	42 / 6.5	35.5 / 5.5	29 / 4.5	23 / 3.5	17 / 2.5	10.5 / 1.5	3 / 0.5
3.5	N/A	> 39 / > 18.4	39 / 18.4	34 / 15.4	28 / 12.5	23 / 9.6	17.5 / 6.6	12.5 / 3.8	7 / 1.8
7.0	N/A	> 39 / > 13.8	39 / 13.8	34 / 11.7	28 / 9.6	22.5 / 7.5	17.5 / 5.4	12.5 / 3.4	7 / 1.6
14.0	N/A	> 39 / > 10.5	39 / 10.5	34 / 8.9	28 / 7.3	22.5 / 5.7	16.5 / 4.1	11.5 / 2.6	5 / 1.0
28.0	N/A	> 39 / > 8.0	39 / 8.0	33 / 6.8	27.5 / 5.6	22 / 4.3	16 / 3.1	10 / 1.8	4 / 0.7

NOTE: The insertion loss/line range values are defined as being less than or equal to the listed numbers, but greater than the numbers to the immediate right, or zero for LL3 - LL0 = 1111.

Figure 11: Typical Serial Port Output for Receive Activation @ 72 kbps



Design Considerations

Figure 12 shows a typical LXT400 application circuit. A DSU crystal (4.096 MHz) is connected across MCLK1 and MCLK2, with two grounded loading capacitors. The line interface consists of a pair of 1:1 transformers, center-tapped on the line side, with appropriate load resistors. The Rs/ Cs shunt network provides high frequency compensation for the transmit driver. The input signal is developed across the Rr/Rin network. Rv limits current into the low-impedance VINT driver during over-voltage conditions on the line. Table 12 lists external component recommendations.

Crosstalk

It is important to prevent crosstalk between the transmitter and receiver circuits. Steps were taken to reduce this interference inside the LXT400, but precautions must be taken with the line interface circuitry outside the chip as well. Crosstalk is especially high when the idle pattern (alternate positive and negative pulses) is being transmitted because the transmit power is concentrated around the Nyquist frequency (half the baud rate).

PCB Layout

The external line interface circuit must be laid out to minimize coupling of other digital and analog signals into RTIP and RRING (see Figure 13.) These inputs, pins 2 and 3, are high impedance nodes which can pick up interference from adjacent PCB traces. The line interface circuit must be designed for loops with up to 50 dB of loss at the Nyquist frequency, even if the product will never be used on such long lines. When no receive signal is present, the LXT400 will switch to the highest gain filter, which at 56 and 72 kbit/s produces an internal gain of about 50 dB. Unless precautions are taken, substantial interference coupling into RTIP and RRING could exceed the internal slicer levels and prevent the RLOS report. Layout considerations for LXT400 application circuits include:

1. Minimum PCB trace lengths between the LXT400 and the 4.096 MHz crystal and loading capacitors.
2. Minimum PCB trace lengths between resistors Rin and the RTIP and RRING pins. Shield these connections with ground traces.
3. Minimum PCB trace lengths between the receive transformer and the receive termination network.

Figure 12: Typical LXT400 Application Circuit for 72 kbps Operation

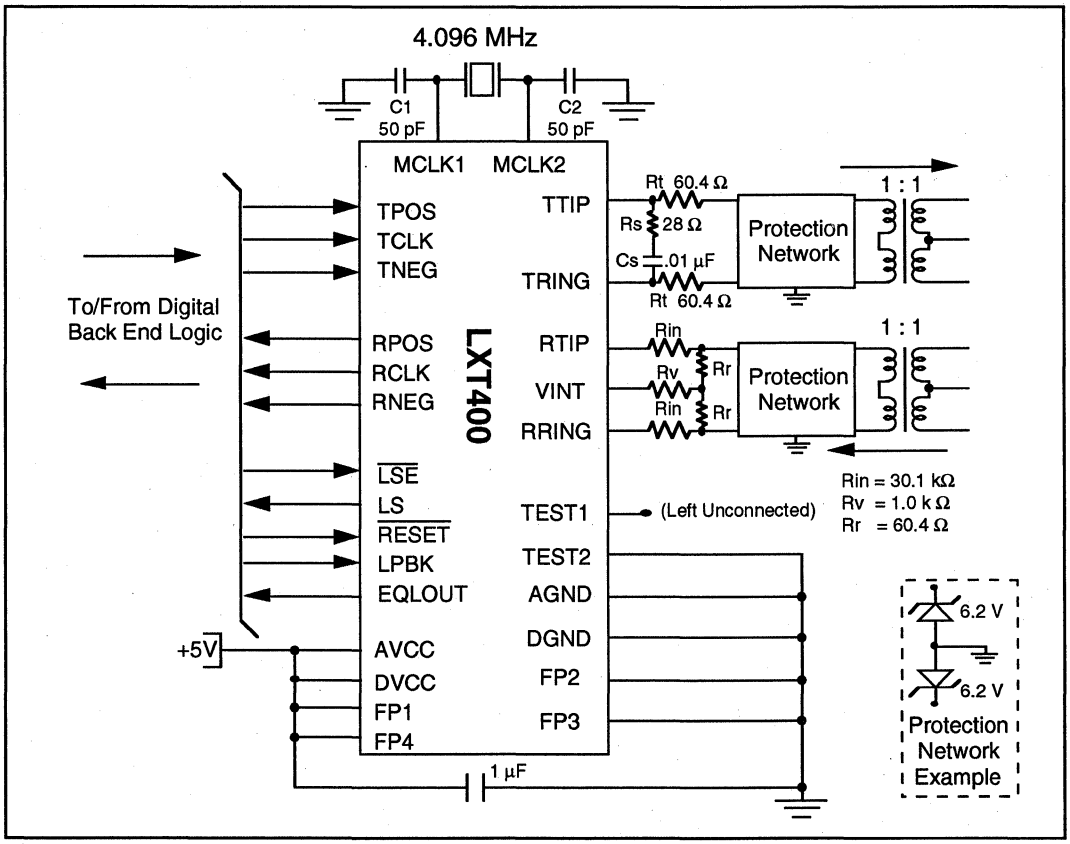
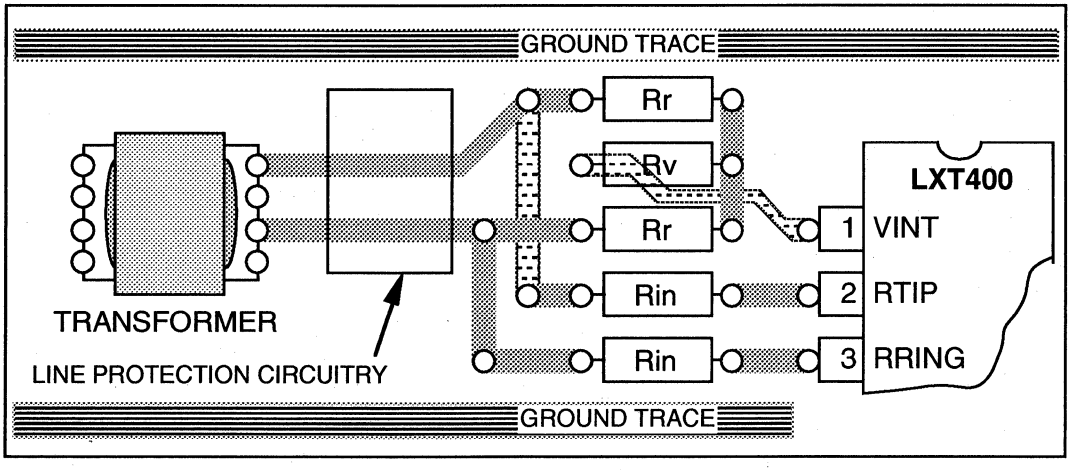


Table 12: External Component Recommendations

Component	Parameter	Recommended Value
Line Transformer Suggested Manufacturers: Midcom - Phone 800/643-2661 Schott - Phone 615/889-8800	Turns ratio	1:1, ± 1%
	Structure	Center tapped (for line side)
	Primary Inductance	200 mH minimum
	Leakage Inductance	22 to 43 µH maximum
	Interwinding Capacitance	350 pF maximum
	DC Resistance (Primary, Rwp)	7 Ω ± 1 Ω
	DC Resistance (Secondary, Rws)	7 Ω ± 1 Ω
Rin	Resistance, Tolerance, Rating	30.1 kΩ, ± 1%, 1/4 W
Rt, Rr	Resistance, Tolerance, Rating	$(135\,\Omega - Rwp - Rws)/2$, ± 1%, 1/4 W
Rv	Resistance, Tolerance, Rating	1 kΩ, ± 5%, 1/4 W
DSU Crystal Suggested Manufacturers: Fox - Phone 813/693-0099 Monitor - Phone 815/432-5296	Nominal frequency	4.096 MHz
	Holder style	HC-49/U
	Operating Mode	Fundamental, parallel resonant
	Load Capacitance	28 pF nominal
	Tolerance	± 25 ppm @ 25 °C
	Range	± 40 ppm, 0 to 70 °C
	Aging	3 ppm per year maximum
	Maximum ESR	50 Ω
	Drive Level	2 mW maximum
DSU Crystal Loading Capacitors	Capacitance, Tolerance, Rating	50 pF, ±5%, 10 V
	Construction	NPO ceramic or equivalent
Transmit Shunt Network		
Rs	Resistance, Tolerance, Rating	28 Ω, ± 5%, 1/4 W
Cs	Capacitance, Tolerance, Rating	0.01 µF, ± 20%, 10 V

Figure 13: Suggested LXT400 PCB Layout



Notes:

Application Notes

1994 Communications Data Book

LEVEL ONE®

LXT300 and LXT310 Interchangeability

Adapting Short-Haul T1 Boards to Long-Haul Applications

General

While the LXT300 is designed for short-haul (up to 200 m) T1/E1 applications and the LXT310 is designed for long-haul (up to 2 km) T1 applications, these transceivers are quite similar in function. There are only minor differences in line interfaces and pin configurations. Therefore, T1 equipment designed for short-haul applications (using the LXT300) can easily be adapted to provide long-haul capability (using the LXT310) as an option. This application note describes the steps necessary to adapt a single design so that it can be used for both long-haul and short-haul applications.

Functional Differences

- In the Hardware mode, three Equalizer inputs on the 300 are replaced by two LBO inputs and an NLOOP output on the LXT310. These pins are identical in the Software mode, but the bit register is defined differently.

- The LXT300 uses two inputs and an output for the Driver Performance Monitor (DPM) function. On the LXT310, these pins are replaced by inputs for Jitter Attenuation Select (JASEL) and Equalizer Gain Limitation (EGL), and an output for Line Attenuation (LATN).

- The LXT300 uses a 1:2 transformer for both the Tx and Rx line interfaces. The LXT310 uses a 1:2 transformer with two 12.5Ω series resistors for the Tx line interface; it uses a 1:1 transformer for the Rx line interface.

Circuit Modifications

To adapt an LXT300 board to accommodate the LXT310, modify the circuit as follows:

1. Cut the DPM output trace from LXT300 pin 11, and tie the LXT310 JASEL input to VCC.

2. Cut the MTIP and MRING inputs to LXT300 pins 17 and 18. Reconfigure the LXT310 input at pin 17 to allow EGL switching, or simply tie pin 17 to ground. Connect the LXT310 output from pin 18 to a LATN decoding circuit.

3. Cut the EC1 input to LXT300 pin 23, and connect the LXT310 output from this pin to NLOOP monitoring circuity.

Line Interface Modifications

On the transmit side, both the LXT300 and LXT310 use a 1:2 transformer. The LXT300 transformer connects directly to the chip as shown in Figure 1a. The LXT310 requires two 12.5 Ω serial resistors in line with the transformer, as shown in Figure 1b.

On the receive side, the LXT300 uses a 1:2 transformer with 400 Ω termination, as shown in Figure 2a. The LXT310 uses a 1:1 transformer with 100 Ω termination, as shown in Figure 2b.

(A 1:2 CT transformer can be used for both devices. For LXT310 boards, connect only one of the secondary windings, an effective 1:1 ratio.)

Figure 1: Transmit Line Interface

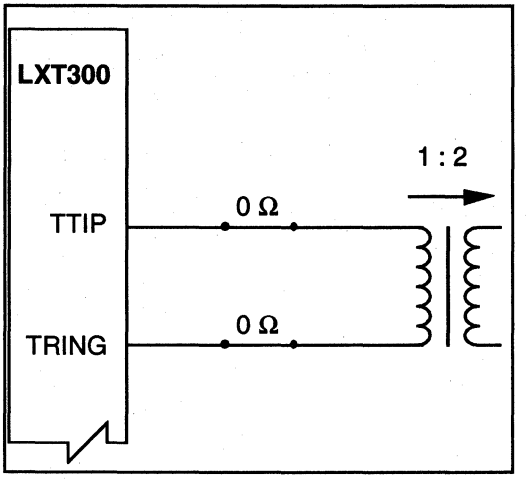


Figure 1a: LXT300 Transmit Line Interface

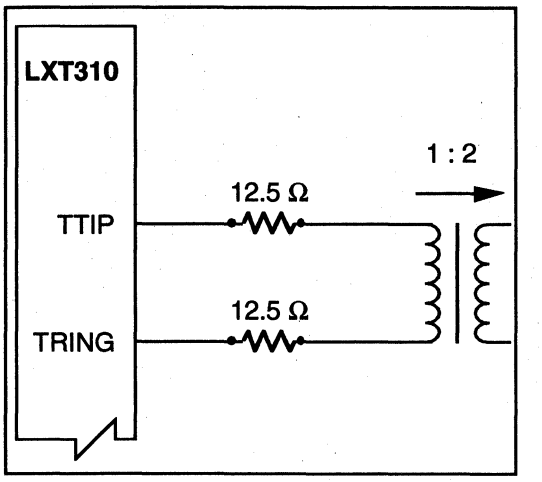


Figure 1b: LXT310 Transmit Line Interface

Figure 2: Receive Line Interface

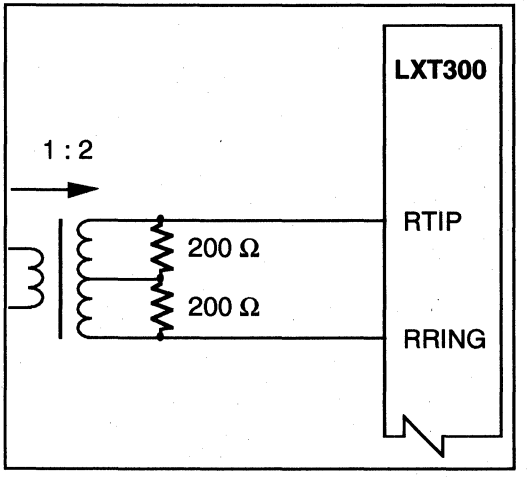


Figure 2a: LXT300 Receive Line Interface

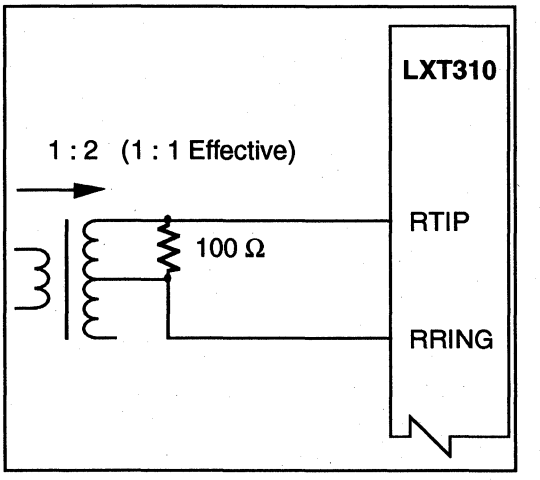


Figure 2b: LXT310 Receive Line Interface

LXT30x and LXT318 Interchangeability

Adapting Short-Haul E1 Designs for Long-Haul Applications

General Description

While the LXT300, 304A and 305A are designed for short-haul T1/E1 applications (up to 14 dB) and the LXT318 is designed for long-haul E1 applications (up to 43 dB), these transceivers are quite similar in function. There are only minor differences in line interfaces and pin configurations. Therefore, E1 equipment designed for short-haul applications (using LXT30x series transceivers) can easily be adapted to provide long-haul capability (using the LXT318). This application note describes the steps necessary to adapt a short-haul design so that it can be used for both long-haul and short-haul applications. (The LXT318 can support both E1 long-haul and E1 short-haul applications.)

Functional Differences

- The LXT30x uses three Equalizer inputs in the Hardware mode. These pins are not used by the 318 and should be tied to ground. These pins are identical in the Software mode, but the bit register is defined differently.

- The LXT30x uses two inputs and an output for the Driver Performance Monitor (DPM) function. On the LXT318, these pins are replaced by an input for Jitter Attenuation Select (JASEL) and an output for Line Attenuation (LATN).

- The LXT30x uses a 1:2 transformer for both the Tx and Rx line interfaces. The LXT318 uses a 1:2 transformer with two 15 Ω series resistors for the Tx line interface, and a 1:1 transformer for the Rx line interface.

Circuit Modifications

To adapt an LXT30x board to accommodate the LXT318, modify the circuit as follows:

1. Cut the DPM output trace from LXT30x pin 11 and tie the LXT318 pin 11 (JASEL) to VCC (to select receive jitter attenuation), or to GND (to select transmit jitter attenuation).

2. Cut the MTIP and MRING inputs to LXT30x pins 17 and 18. Connect the LXT318 input at pin 17 to ground. Connect the LXT318 output from pin 18 to a LATN decoding circuit.

3. For Hardware mode, cut the EC inputs to LXT30x (pins 23, 24 and 25), and connect these LXT318 pins to ground.

Line Interface Modifications

On the transmit side, both the LXT30x and LXT318 use a 1:2 transformer. The LXT30x transformer connects directly to the chip as shown in Figure 1a. The LXT318 requires two 15 Ω series resistors in line with the transformer, as shown in Figure 1b.

On the receive side, the LXT30x uses a 1:2 transformer with 480 Ω termination, as shown in Figure 2a. The LXT318 uses a 1:1 transformer with 120 Ω termination for TWP applications, as shown in Figure 2b.

(A 1:2 CT transformer can be used for both devices. For LXT318 boards, connect only one of the secondary windings, an effective 1:1 ratio.)

Figure 1: Transmit Line Interface

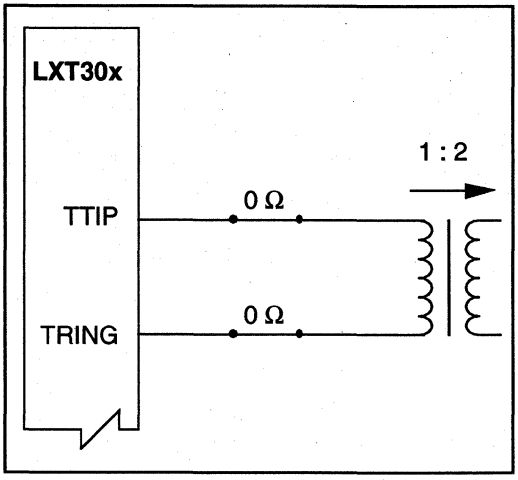


Figure 1a: LXT30x Transmit Line Interface

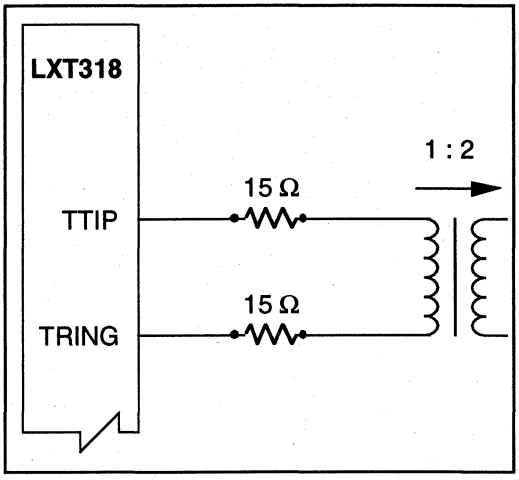


Figure 1b: LXT318 Transmit Line Interface

Figure 2: Receive Line Interface

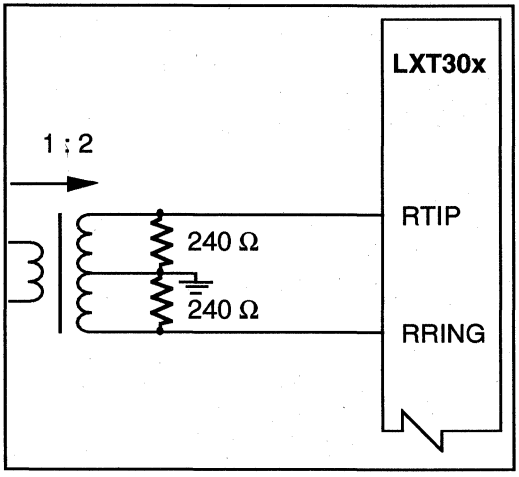


Figure 2a: LXT30x Receive Line Interface

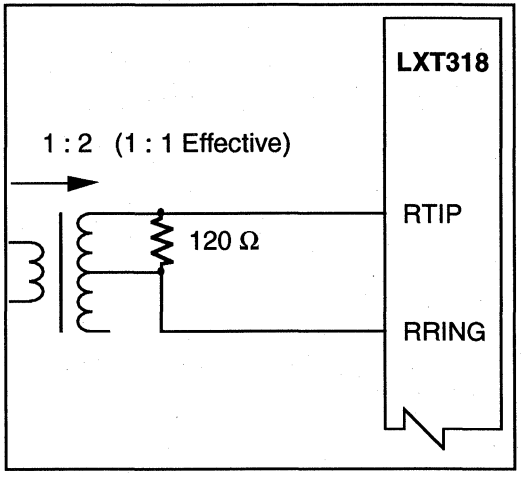


Figure 2b: LXT318 Receive Line Interface

LXT318 Long-Haul E1 Transceiver Solution

Migration from Dual-Chip (LXT304A / LXT316) to Single-Chip (LXT318) Implementation

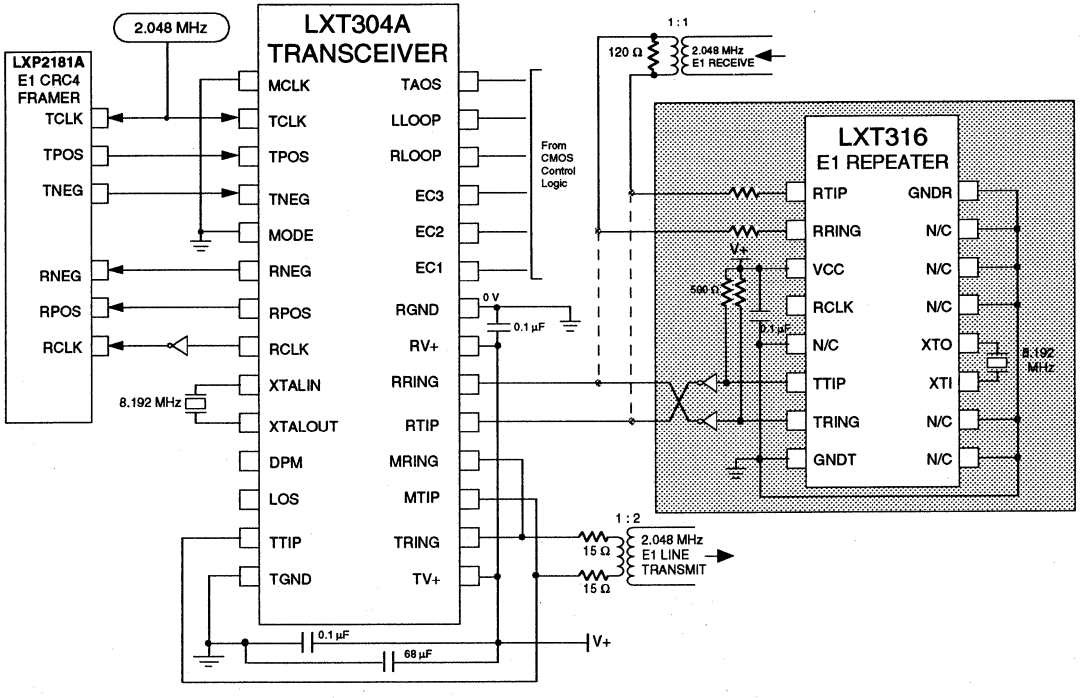
Introduction

This application note provides manufacturers of Long-Haul E1 (2.048 Mbps) transmission equipment with a smooth transition from Level One's LXT304A/316 dual-chip long-haul E1 solution to an advanced single-chip implementation, the LXT318.

There are only minor differences in the line interfaces for single and dual chip solutions. Therefore, E1 equipment designed around the dual-chip solution (using the LXT304A and LXT316) can easily be adapted to take advantage of the fully integrated LXT318.

This application note describes the steps necessary to modify a dual-chip design for use with the LXT318. Both solutions use the same transformers. The modification involves removing the repeater and associated circuitry (shown in the shadowed area of the diagram below).

Long Haul E1 2-Chip Solution



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Functional Differences

- In Hardware mode, the LXT304A uses three Equalizer Control inputs (EC1, EC2 and EC3), and two transmit driver monitor inputs (MTIP and MRING). These functions are not provided on the LXT318. On the LXT318, pins 17, 23, 24 and 25 must be tied to ground. LXT318 pin 18 is now the coded line attenuation (LATN) output.

- On the LXT318, pin 11 is used as an input for Jitter Attenuation Select (JASEL). It should be tied to VCC or ground, as desired.

Circuit Modifications

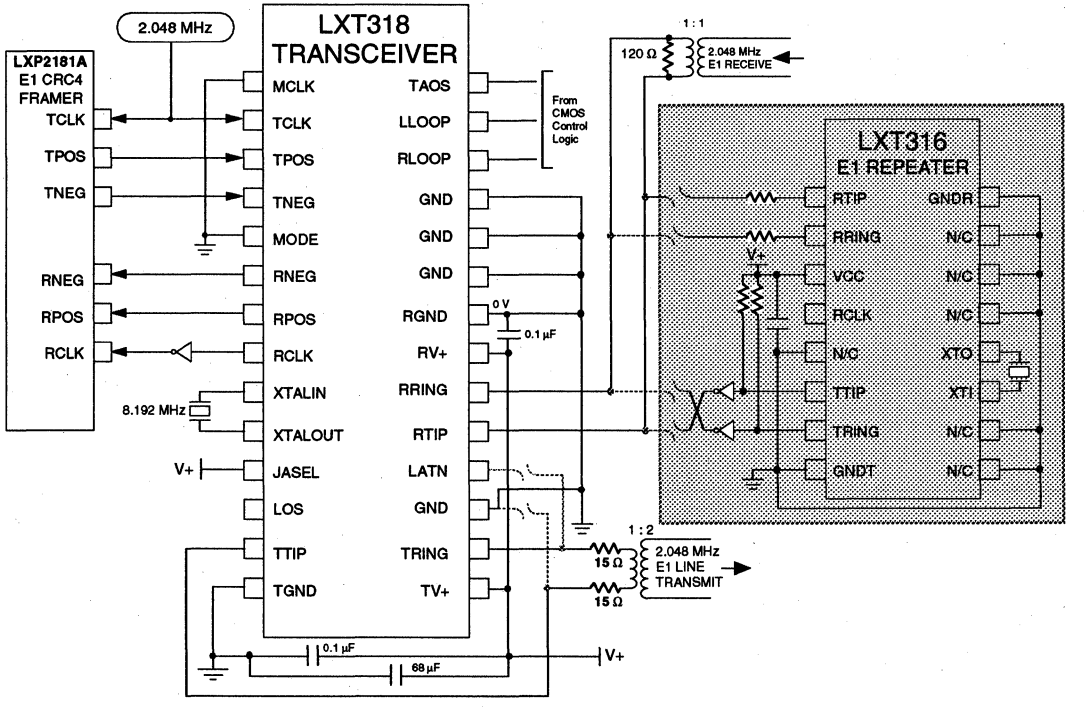
1. To modify a 2-chip long-haul PCB for use with the LXT318, cut the EC1, 2 and 3 inputs to LXT304A (pins 23, 24 and 25). Tie these three pins to ground.

2. Cut the MTIP and MRING inputs to LXT304A pins 17 and 18. Tie pin 17 to ground. Tie pin 18 to an LATN decoding circuit or let it float.

3. Cut the DPM output trace from LXT304A pin 11, and tie the LXT318 JASEL input to VCC (for receive jitter attenuation) or to ground (for transmit jitter attenuation).

4. Remove all the circuitry shown in the shadowed area below, and connect the receive transformer to pins 19 and 20 of the LXT318.

Long Haul E1 1-Chip Solution (LXT318)



LXT30x Transceiver / Framer Interface

Application Guidelines for use with Mitel MT8976 and MT8979 Framers

General Description

This application note provides guidelines for interfacing the Level One LXT300 series (LXT300, 301, 305, 304A and 305A) transceivers with Mitel framers in both T1 and E1 applications. Only minimal circuitry is required to implement the interface. For T1 (1.544 MHz) applications, the transmit data pins may be connected directly between the two chips as shown in Figure 1. A single 4-gate NAND package provides the signal inversion required on the receive side.

Receive side signal inversion is also required for E1/CEPT (2.048 MHz) applications. A similar setup using NAND gates in an E1 application is shown in Figure 2 (back page). Additional circuitry is also required to synchronize the transmit data stream in E1 applications. This synchronization is easily implemented with a pair of D-flip-flops, clocked by the common 2.048 MHz transmit clock.

Figure 1: LXT30x Interface to MT8976 T1 ESF Framer

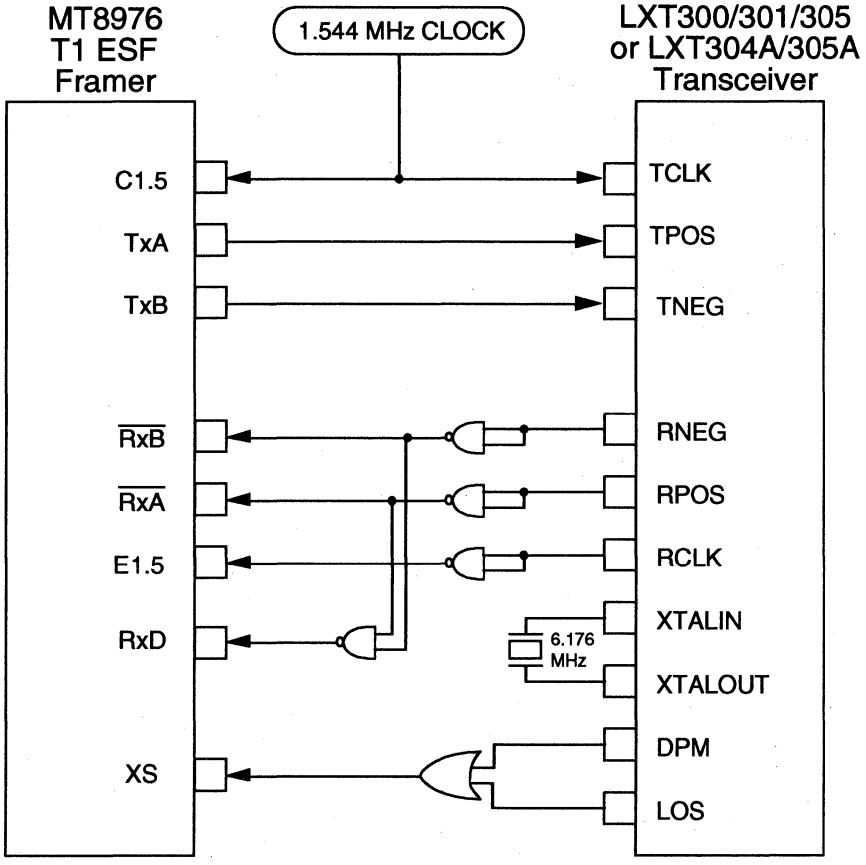


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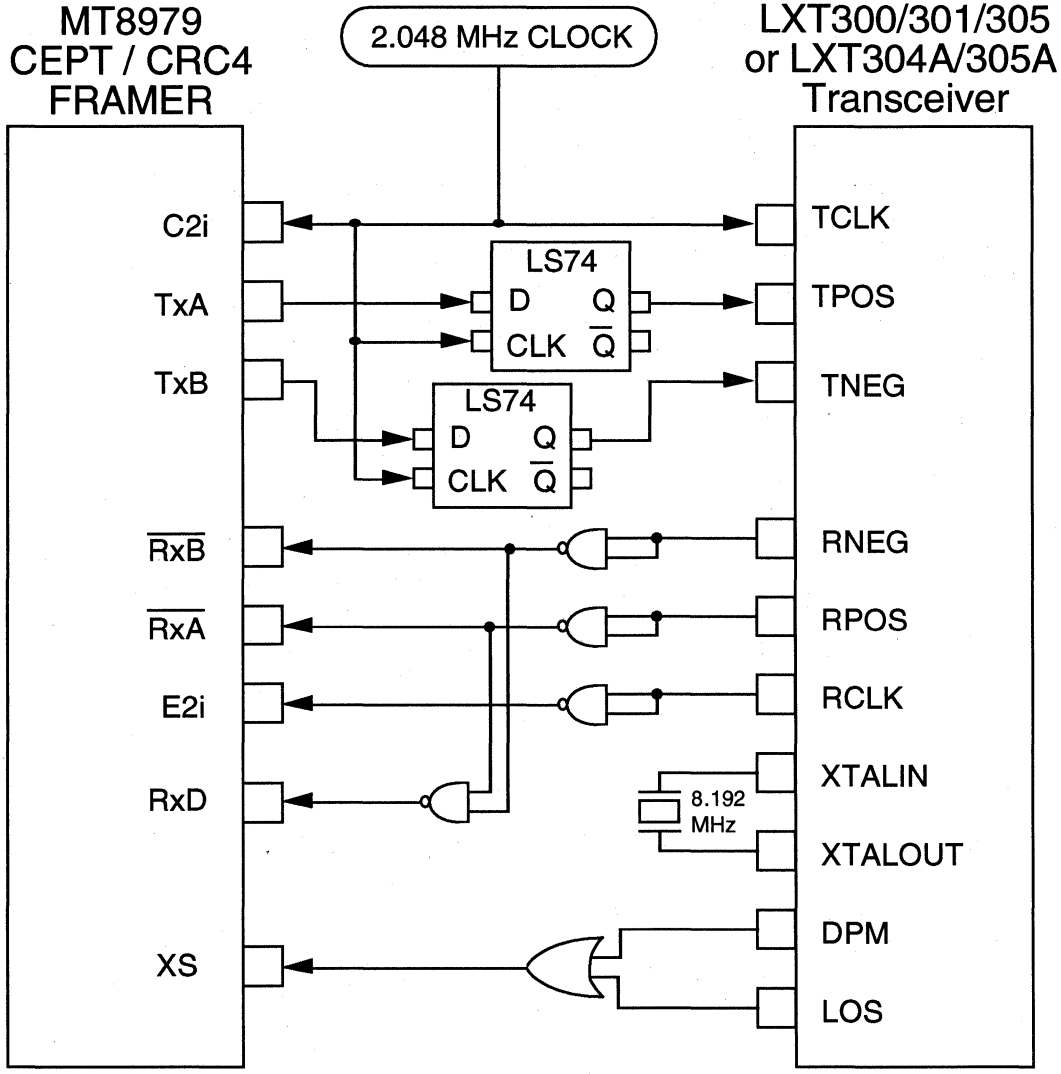
Figure 2: LXT300 Interface to MT8979 E1 CRC Framer



T1 Jitter Performance Measurement

AT&T Pub 62411 Certification

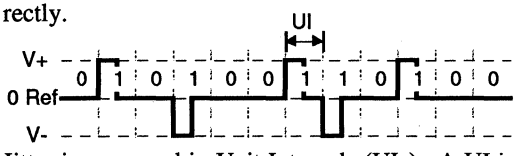
General Description

This application note provides a brief definition of jitter and then summarizes jitter performance requirements and measurement techniques specified for T1 (1.544 MHz) Customer Premises Equipment (CPE).

Requirements for T1 systems are specified by AT&T Publication 62411, December 1990 - Accunet T1.5 Service Description and Interface Specification. (Similar requirements for E1 systems are specified by CCITT G.823 - The Control of Jitter and Wander within Digital Networks.)

Understanding Jitter

T1 signals are composed of square-wave pulses as shown below. A "1" is represented by a positive or negative pulse (the pulses alternate in polarity). A "0" is represented by the absence of a pulse. To enhance timing and data recovery, the duration of a "1" pulse is constrained to ½ of the bit rate period. Deviations in time between when the pulse transitions occur and when the decoding circuits expect them to occur are referred to as jitter. Very low frequency deviations (< 10 Hz) are referred to as wander. These deviations are equivalent to unintentional phase modulation. Any pulse that is phase-shifted by more than 50% will be sampled incorrectly.



Jitter is measured in Unit Intervals (UIs). A UI is equal to the bit rate period. A UI is, therefore, the reciprocal of the frequency. For T1 service, a UI equals 648 ns, while the "1" pulse duration is 324 ns. Jitter amplitude is measured in UI pp (peak-to-peak). Jitter specifications have both an amplitude component and a frequency component; that is, for a given jitter parameter, performance will be specified at a particular amplitude (in UI pp) within a particular frequency band.

Types of Jitter

There are three parameters of jitter performance which are specified and measured:

1. Input Jitter Tolerance (Jitter Accommodation)
2. Output Jitter Generation (Intrinsic Jitter)
3. Jitter Transfer (Jitter Attenuation)

Input Jitter Tolerance. Input jitter tolerance is defined as a system's ability to recover input data correctly in the presence of jitter. This value indicates how much input jitter a system or device can handle before bit errors occur. Individual devices should have as high a tolerance value as possible because the system's jitter tolerance is limited to the tolerance of its most restrictive element. Input jitter tolerance is also referred to as jitter accommodation.

Output Jitter Generation. Output jitter is defined as the amount of jitter generated in the system output when zero jitter is present in the input. Essentially, it is a measure of how "noisy" the system is. Individual system elements should have as low a value as possible because output jitter is additive. Each device in a system adds its own intrinsically generated jitter to the system total, hence the term "jitter budget". Output jitter is also referred to as intrinsic jitter or additive jitter.

Jitter Transfer. Jitter transfer, frequently referred to as jitter attenuation (JA), is defined as the percentage of input jitter which is present in the system output, expressed in dBs. While a certain amount of jitter attenuation is desirable, excessive jitter attenuation can cause problems with frame slippage and synchronization. Therefore, jitter attenuation specifications define an acceptable range of values for a given jitter frequency. (Jitter attenuation circuits typically use an elastic store as a buffer between input and output. Buffer size is directly related to throughput delay. Oversize buffers intended to maximize jitter attenuation may cause equipment to fail requirements for maximum throughput delay.)

AT&T Pub 62411 Compliance Testing

Jitter performance is strongly related to the transmitted bit pattern. AT&T Publication 62411 defines a standard quasi-random test signal (QRTS) used for jitter testing at 1.544 Mbps. The QRTS bit pattern is designed to simulate typical transmission patterns. Jitter performance testing should be conducted in a noise-free environment to eliminate, as far as possible, the effect of other factors on the performance of the device under test.

Input Jitter Tolerance Testing.

The input jitter tolerance of a DTE is characterized by determining the level of jitter required to induce bit errors in a 60-second interval. At frequencies up to 10 kHz, one bit error is allowed. At higher frequencies, up to 5 errored bits are allowed in a 60-second period. (Synchronizers, which provide a system master clock, are held to a tighter spec. They are characterized by determining the level of jitter required to induce a loss of synchronization.) Jitter tolerance is tested at a number of spot frequencies to ensure full characterization across the spectrum. Figure 1A shows the jitter tolerance template for DTE. Figure 1B shows the jitter tolerance template for synchronizers.

Jitter Tolerance Test Procedures

1. Connect the test equipment as shown in Figure 2.

2. Configure the device under test for remote loopback.

3. With its modulation input turned off, configure the RF signal generator for an appropriate output level to drive the external clock input of the BER, through an AC-coupled driver as shown in Figure 2. Test this jitter-free external clocking of the BER with the unit under test.

4. Enable the External FM Modulation mode of operation on the HP8656B.

5. Set the Frequency Synthesizer to the first jitter frequency to be tested. Set the amplitude of this sine wave frequency such that the high/low input LEDs on the HP8656B are off (approximately 2.1 V pp.

6a. DTE Testing. While observing the transmission tester for bit error indications, adjust the modulation index on the signal generator to the level required to produce the minimum error level. (For example, if the synthesizer is set for a jitter frequency of 10 Hz, adjust the modulation index as required to produce no more than one bit error in any 60-second period.)

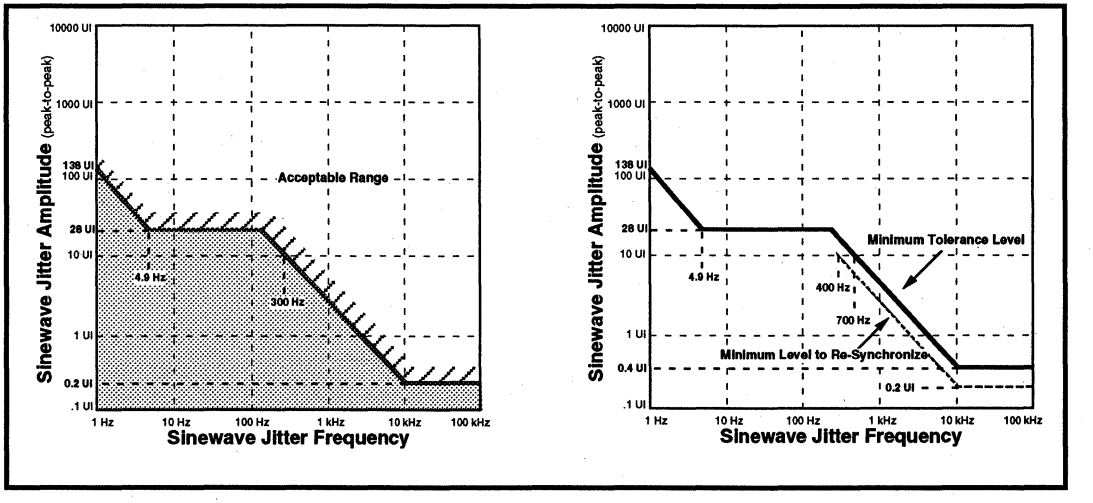
6b. Synchronizer Testing. While observing the transmission tester for clock slips (loss of sync), adjust the modulation index on the signal generator to the level required to produce the loss of sync. Then, reduce the modulation index to the level required to achieve resynchronization. Record **both** values.

7. Determine the jitter tolerance using the formula:

$$UIpp = \Delta f / \pi\ fm$$

where fm = Jitter Frequency
(synthesizer modulation frequency), and
where Δf = FM Modulation Index
(as set on the signal generator).

Figure 1: Input Jitter Tolerance Specified by AT&T Publication 62411



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for example,

$$38\ \text{kHz}/\pi \cdot 10\ \text{Hz} = 1209\ \text{UIpp @ 10 Hz}$$

8. Repeat steps 5 through 7 for additional frequencies to be tested and plot the results as shown in Figure 3.

Figure 2: Input Jitter Tolerance Test Setup

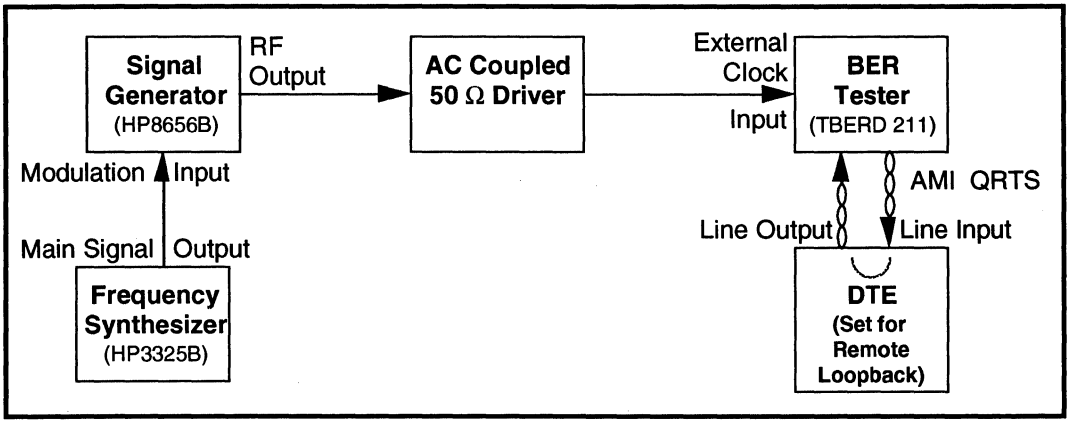
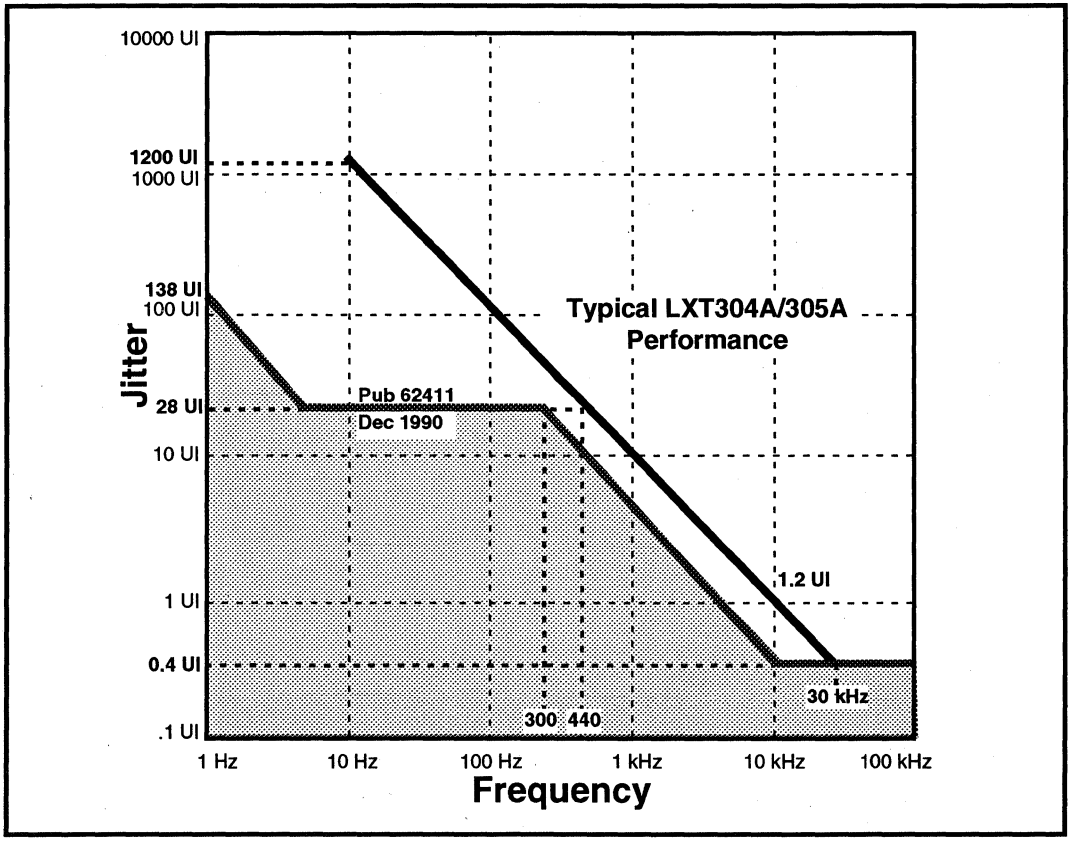


Figure 3: Charting Input Jitter Tolerance Test Results



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Output Jitter Generation Testing.

The intrinsic jitter generated by a DTE is characterized by configuring the device for remote loopback and then monitoring the line output when no jitter is present in the line input. AT&T Publication 62411 lists maximum output jitter values for three separate frequency bands, as well as a fourth value for the unlimited broadband output. Output jitter may be measured with a variety of instruments including peak detectors, true RMS voltmeters and spectrum analyzers. Figure 4 shows a typical test setup. Figure 5 lists the maximum generated jitter allowed in each frequency band, as well as sample test measurements.

Output Jitter Generation Test Procedures

1. Connect a frequency synthesizer, signal generator and telecom tester to produce a jitter-free QRTS output. Figure 2 may be used as a reference.
2. Select the filters in the HP3785B as shown in Figure 4 and monitor the first frequency band.
3. Measure and record the output jitter peak values.
4. Repeat steps 2 and 3 for each remaining band.

Figure 4: Output Jitter Generation Test Setup

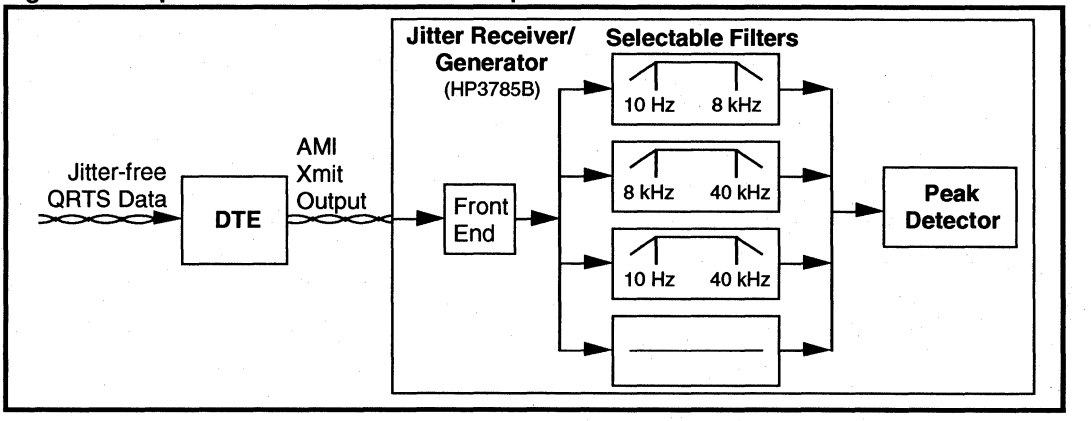


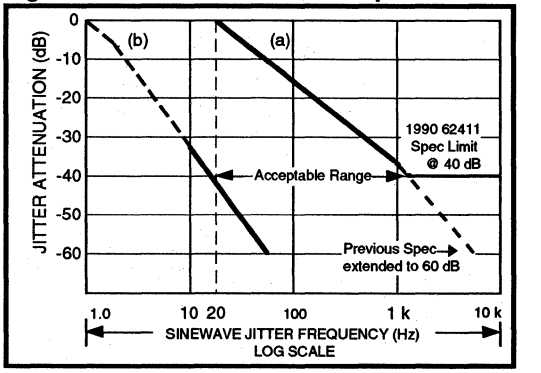
Figure 5: Output Jitter Generation Specification

Frequency Band	62411 Specified Maximum		Typical 304A Performance
10 Hz - 8 kHz	0.02 UI	(0.8 mV rms)	0.002 UI
10 Hz - 40 kHz	0.025 UI	(1.25 mV rms)	0.016 UI
8 kHz - 40 kHz	0.025 UI	(1 mV rms)	0.014 UI
No Bandlimiting	0.05 UI	(2 mV rms)	0.025 UI

Jitter Attenuation Testing.

Jitter attenuation is defined as the percentage of input jitter which is present in the system output, expressed in dBs. While a certain amount of jitter attenuation is desirable, excessive jitter attenuation can cause problems with frame slippage and synchronization. Therefore, jitter attenuation specifications define an acceptable range of values for a given jitter frequency as shown in Figure 6. (Jitter attenuation circuits typically use an elastic store as a buffer between input and output. Buffer size is directly related to throughput delay. Oversize buffers may cause equipment to fail requirements for maximum throughput delay.) Jitter attenuation is also referred to as jitter transfer.

Figure 6: Jitter Attenuation Template



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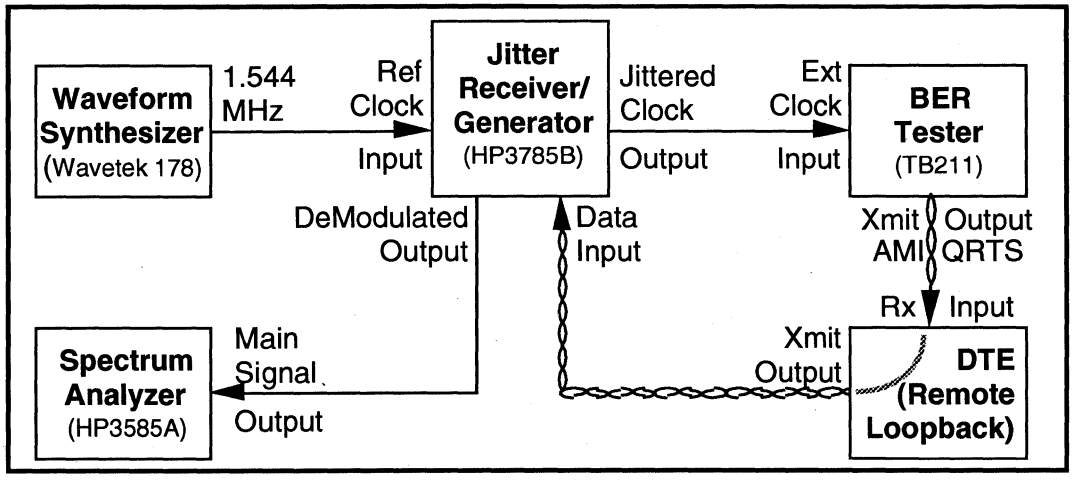
Jitter Attenuation Test Procedures

1. Connect the test equipment as shown in Figure 7.
2. Set the frequency synthesizer to produce a square wave reference clock at 1.544 MHz.
3. Set the jitter generator as follows:
   a. Frequency: lowest frequency to be tested
   b. Amplitude : 75% of the level shown in Figure 1 (use appropriate DTE or Synchronizer template.)
4. Set the spectrum analyzer as follows:
   a. Center Frequency: same as 3a.
   b. Frequency Span: 200 Hz - 500 Hz.
5. Set the reference level (UIINP) on the spectrum analyzer by temporarily connecting the BERT transmit output directly into the data input of the jitter receiver/ generator.
6. Re-connect the test equipment as shown in Figure 7 and set the synthesizer to the first jitter frequency to be tested.
7. Observe the spectrum analyzer (Figure 8) and record the difference between the reference level, UIINP, and the DTE line output level, UIOUT.
8. Repeat steps 3 through 7 for each frequency to be tested and plot the results as shown in Figure 9.

Figure 7: Jitter Attenuation Test Setup



NOTE: The test setup shown in Figure 7 is used to measure jitter amplitudes less than 10 UI (the limit of the HP3785B). Alternate test setups should be used for other jitter amplitudes or amplitude/frequency combinations.

Figure 8: Spectrum Analyzer Display

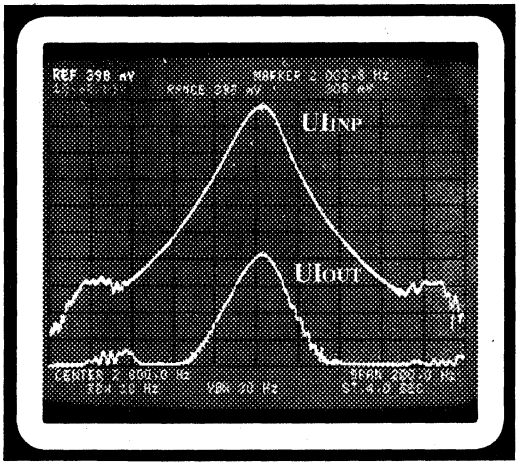
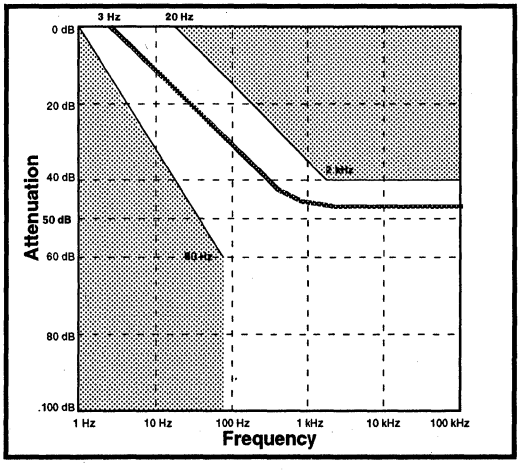


Figure 9: Typical LXT304A JA Performance



NOTES:

LXT310 and LXT304A

Combination DS-1 / DSX-1 CSU Applications

Description

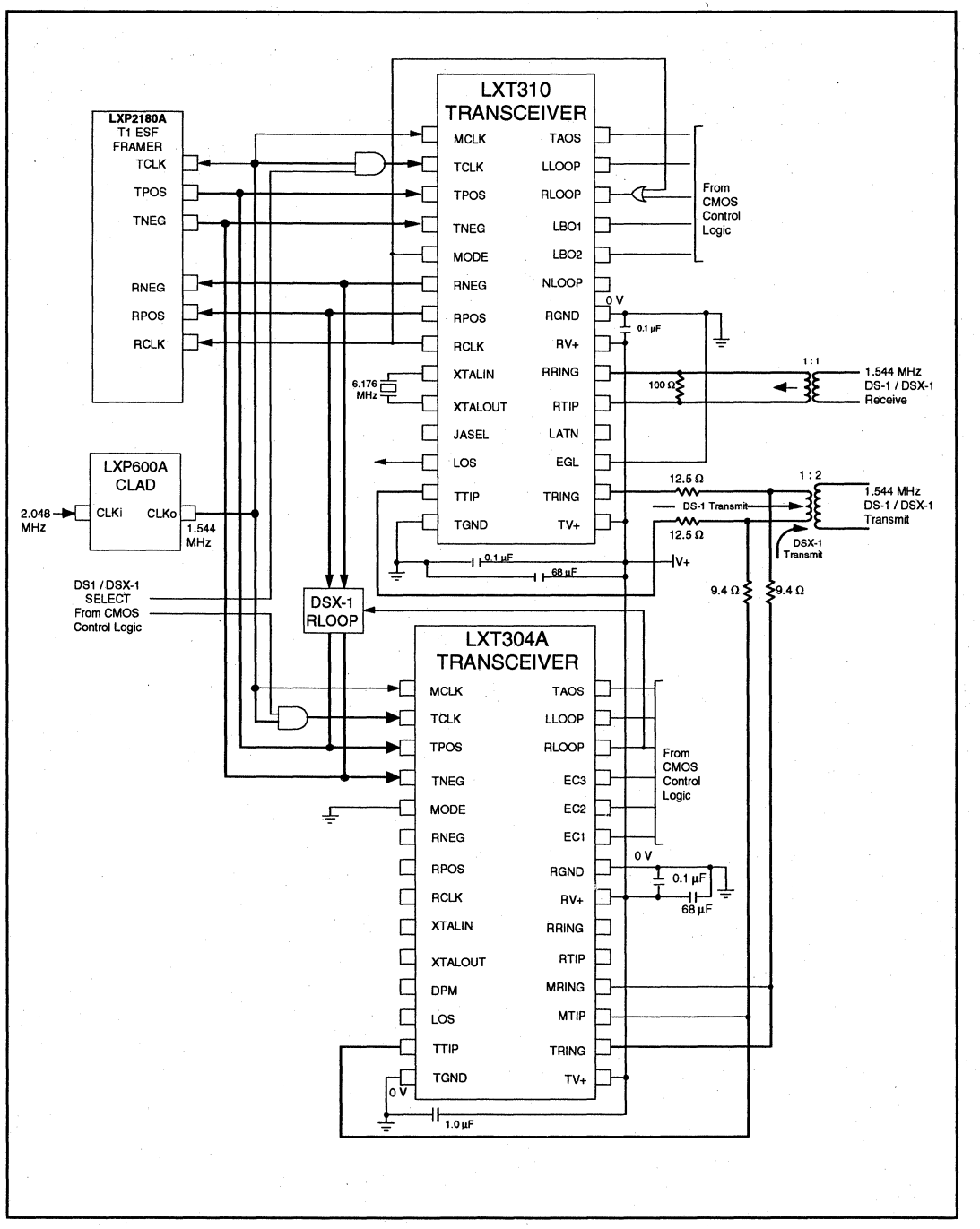
This application note describes a T1 line interface for combination DS-1/DSX-1 CSU applications implemented with an LXT310 long-haul transceiver and an LXT304A short-haul transceiver. Figure 1, on the next page, is a simplified schematic of the application circuit.

Transmit functions are shared between the LXT310 (DS-1) and the LXT304A (DSX-1). Both transmitters are connected to a single 2:1 transmit transformer through matching resistors. A pair of AND gates on the TCLK input pins are used to select the active transmitter. (The transmitters remain in the power-down state with high impedance on the TPOS/TNEG inputs until TCLK is supplied.)

Receive functions for both DS-1 and DSX-1 applications are handled by the LXT310. The receive circuits of the LXT304A are not used.

Some additional circuitry is required to route receive data from the LXT310 to the LXT304A for Remote Loopback in the DSX-1 mode. Refer to the LXT310 and LXT304A data sheets for detailed specifications.

Figure 1: Combination DS-1 / DSX-1 CSU Application Circuit



LXT310 Line Protection Circuitry

Application Guidelines

General Information

This application note provides guidelines for line protection circuitry required in network channel termination equipment (NCTE), a typical LXT310 application. NCTE is installed at the customer premises end of T1 lines. Called "DS-1" loops, these lines are typically outside the office environment. They are subject to overvoltage/ overcurrent stresses from lightning strikes, power crosses, and other noise sources. Protection circuitry is required to protect the line and the termination equipment (CSU, Mux, PBX, etc.) from overload stresses.

NCTE protection requirements are specified in FCC Part 68 (lightning hazards), UL 1459 (AC hazards), Bellcore TR-TSY-000007 and AT&T Pub 62411. These documents differentiate between longitudinal stress (differential between tip/ring and ground) and metallic stress (differential between tip and ring). Longitudinal stresses are more common and include impulsive noise events such as lightning induced surges. Metallic stresses are less likely and are usually caused by power crosses during maintenance activity.

Protective Circuitry

Figure 1 shows a typical LXT310 line interface. Protective circuit elements are described below.

- Resistors R_T, R_R and R_Z in the transmit and receive lines are selected to match the line impedance. They also provide some current limiting action.
- Line transformers T_T and T_R should be breakdown rated at > 1 kV.
- The 6.3 V zener diode bridges clamp metallic stress, passing only the current required to hold tip/ring differential at 6.3 V maximum.
- Current is limited by load resistors R_L, the optional fuses F_L and the diode bridges.
- The gas discharge tubes provide fast reaction protection from lightning strikes, conducting sudden surges to ground.

Suggested component values are listed in Table 1 (back page).

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Figure 1: LXT310 Protection Circuitry

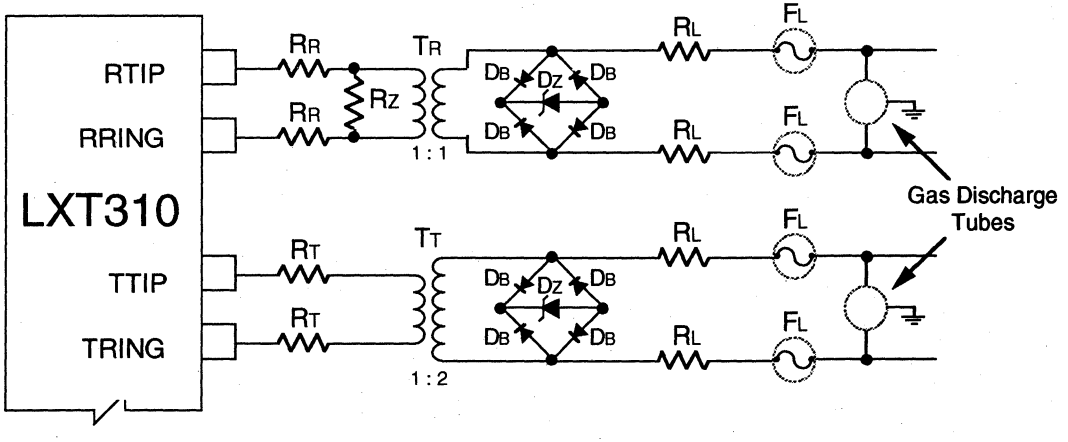


Table 1: Recommended Component Values

Symbol	Value
TT	ET ≥ 1 kV
TR	ET ≥ 1 kV
RL	5.6 Ω, 5 %, 2 W
RT	12.5 Ω, 5 %, ¼ W
RR	100 Ω, 5 %, ¼ W
RZ	100 Ω, 5 %, ¼ W
NB	type 1N4004
NZ	6.3 V, 5 W, type 1N5341A
FL*	In-line fuses, 1 - 1.5 A
GDT*	Gas Discharge Tubes

* Optional devices. May be required for UL approval.

LXT400 Alternate Data Rate Applications

Guidelines for 64 kbps Clear Channel and other Alternate Data Rates

General Information

The LXT400 offers 14 selectable data rates using a single 4.096 MHz master clock. The selectable data rates include the 10 standard DDS rates and four PacBell ADN rates listed in Table 1 below. This application note provides guidelines for using the LXT400 in circuits which operate at additional alternate data rates. **Figure 1, back page, shows a typical 64 kbps clear channel application circuit using a 4.68114 MHz crystal.**

Alternate rate operation is implemented by selecting the closest standard data rate with the Frequency Program pins (FP1 - FP4), and then pulling the chip to the desired data rate with an off-frequency master clock (MCLK). MCLK may be supplied by a crystal across MCLK1 and MCLK2 (as shown in Figure 1), or by a digital clock at MCLK1 with MCLK2 left open.

Table 1: Selectable Data Rates

Data Rates		FP1	FP2	FP3	FP4
DDS	2.4 kbps	0	0	0	0
	3.2 kbps	1	0	0	0
	4.8 kbps	0	1	0	0
	6.4 kbps	1	1	0	0
	9.6 kbps	0	0	1	0
	12.8 kbps	1	0	1	0
	19.2 kbps	0	1	1	0
	25.6 kbps	1	1	1	0
	56.0 kbps	0	0	0	1
	72.0 kbps	1	0	0	1
ADN	3.5 kbps	0	1	0	1
	7.0 kbps	1	1	0	1
	14.0 kbps	0	0	1	1
	28.0 kbps	1	0	1	1

Clock Frequency Selection

Use the following equation to determine the required MCLK frequency $\mathbf{f_o}$:

$$f_o = 4.096\ \text{MHz} \bullet {}^{f_D}/_{f_S}$$

where fD = the desired data rate, and
fS = the selected data rate
(selected by pins FP1 - FP4).

Because the LXT400 oscillator operates best at frequencies above 4 MHz, the next lower data rate should be selected, and used with a higher frequency MCLK. For example, if the desired data rate is 64 kbps, two standard rates (56 kbps and 72 kbps) are equidistant from the desired frequency. Optimum performance is achieved by selecting the 56 kbps data rate and driving MCLK at a frequency higher than the standard 4.096 MHz, to pull the LXT400 up to 64 kbps. With these values plugged into the equation;

$$f_o = 4.096\ \text{MHz} \bullet {}^{64\ k}/_{56\ k}$$

$$f_o = 4.68114\ \text{MHz}$$

When MCLK is supplied by a crystal oscillator[1], the FP pins can be hardwired to the desired frequency. However, in applications which require operation at multiple frequencies (standard and/or alternate), relays or control logic can be used to switch the FP inputs and crystals or digital clocks. (Relays should be selected to minimize the effects of contact resistance and capacitance.) Table 2, back page, lists MCLK frequencies and FP settings for various alternate data rates.

[1] Crystal f_o must be accurate to within ± 40 ppm over the temperature range -40 to +85°C. This ensures an MCLK frequency accurate to within ±100 ppm at the DSU. MCLK frequency at the OCU must be accurate to within ±50 ppm. See LXT400 data sheet for full details.

Table 2: MCLK Frequency Selection for Alternate Data Rates

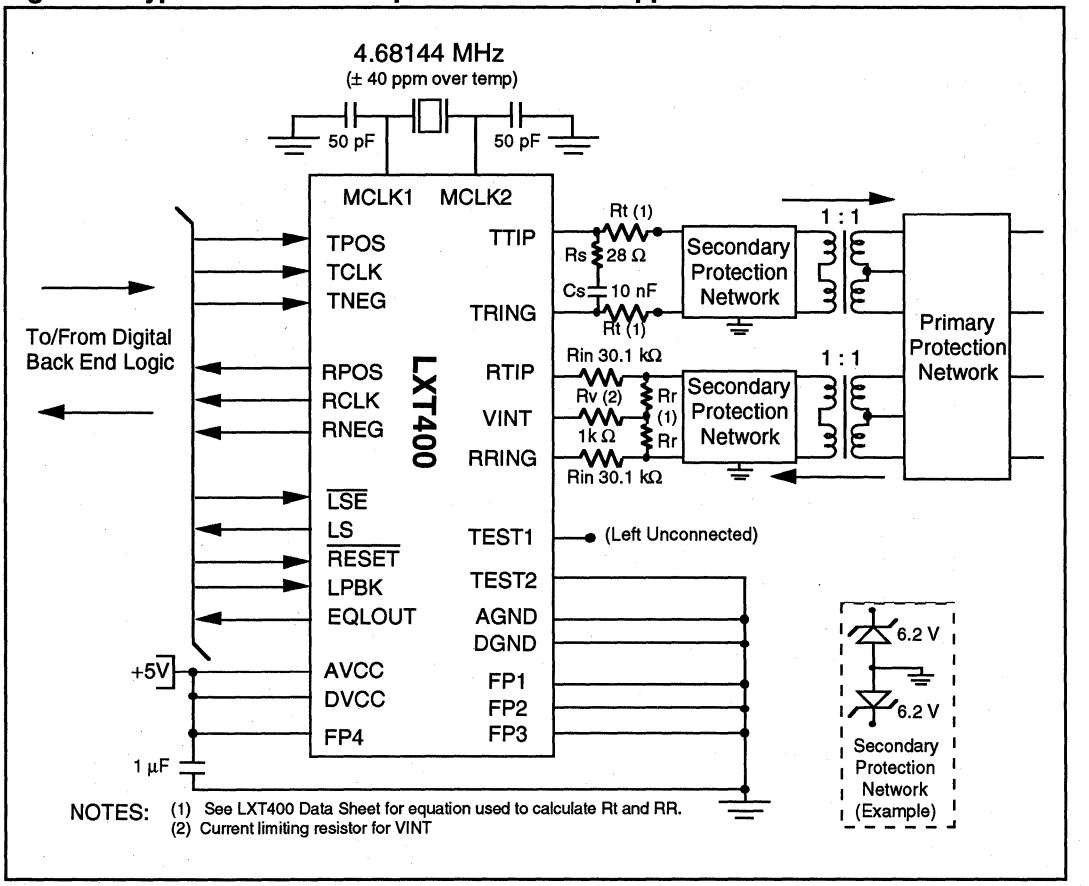
Desired Data Rate	Selected Data Rate	FP1	FP2	FP3	FP4	MCLK[1] Frequency
38.4 kbps	25.6 kbps	1	1	1	0	6.144 MHz
51.2 kbps	56.0 kbps	0	0	0	1	3.74491 MHz[2]
64.0 kbps	56.0 kbps	0	0	0	1	4.68114 MHz

NOTES:

1 Crystal f_O must be accurate to within ± 40 ppm over the temperature range -40 to +85°C. This ensures an MCLK frequency accurate to within ±100 ppm at the DSU. MCLK frequency at the OCU must be accurate to within ±50 ppm. See LXT400 data sheet for full details.

2 In this case the difference between the desired data rate and the selected data rate is small enough that the MCLK frequency may drop below 4 MHz without degrading device operation.

Figure 1: Typical LXT400 64 kbps Clear Channel Application



LXT902 and LXT906 - Impedance Matching for Shielded and Unshielded Twisted-Pair Lines

General

The LXT902 Media Attachment Unit (MAU) and LXT906 Twisted-Pair - Coax (TP-CX) Adapter both require impedance matching with the network media. This application brief provides a short explanation of the impedance matching networks required for shielded and unshielded twisted-pair lines. This information applies to both the LXT902 and the LXT906

Transmit Line Matching

On the transmit side, the LXT902 and LXT906 use resistors in line with the output as shown in Figure 1. To provide an optimum match, the total impedance of the resistors and the filter should equal the line impedance ($RL_1 + RL_2 + ZF = ZL$).

Receive Line Matching

On the receive side the LXT902 and LXT906 use a pair of resistors across the input with the center node tied to ground through a capacitor as shown in Figure 2. To provide an optimum impedance match, use the same formula as used for the transmit side: $RL_1 + RL_2 + ZF = ZL$.

Typical Examples

For example, when the network media is 100 Ω UTP and the filter impedance is 5Ω, each resistor value should be 47.5Ω. When the network media is 150 Ω STP and the filter impedance is 0Ω, each resistor value should be 75Ω. This simple formula works for both devices and for both the transmit and receive line interfaces.

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Figure 1. Transmit Line Interface

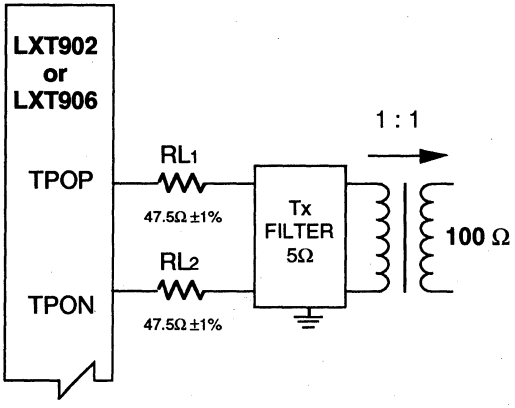
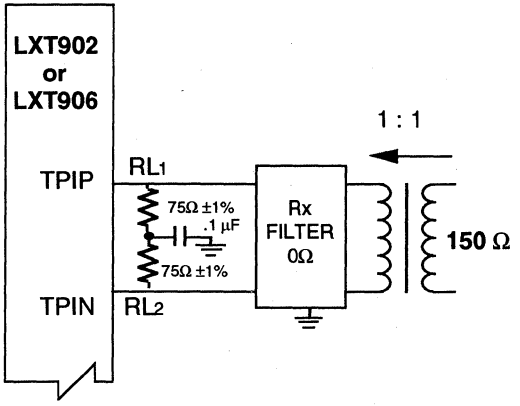


Figure 2. Receive Line Interface



NOTES:

Low Cost FOIRL/Ethernet Media Conversion LXT902 Applications

by Haim Shafir
Senior Design Engineer

General Description

This application note describes a transceiver designed for Fiber Optic Inter-Repeater Link (FOIRL) applications as shown in Figure 1. A FOIRL, defined in the IEEE 802.3 standard, connects two Ethernet repeater units with a fiber optic link. The length of the fiber link between LAN segments is limited to 1 km.

This application note describes a very cost-effective FOIRL transceiver using the Level One LXT902 10Base T Transceiver and standard off-the-shelf components for the Fiber Optic receive/transmit functions.

Features

- Fiber Optic Signal Reception & Transmission
- AUI Reception and Transmission
- Low Light Level Signal Detection
- Fiber Optic Idle Signal Generation
- Diagnostic LEDs

Functional Description

Fiber Optic Receiver

The Fiber Optic receiver uses a Hewlett Packard HFBR-2404 (low-cost miniature FO receiver) and a Motorola MC10H116 (ECL receiver) to convert light pulses from the fiber into electrical signals at Attachment Unit Interface (AUI) levels. These signals are then sent to the LXT902 TP inputs. (The LXT902 will not trigger on a signal ≤1 MHz.)

For low-light level detection, the receive signal is converted to the TTL level. The TTL signal is routed through a high-pass filter into an idle detection circuit clocked at 200 kHz. If no signal transitions are detected, a low light level signal is asserted and the LXT902 is forced into the high impedance state. It remains in the high impedance state until the link is reactivated.

Fiber Optic Transmitter

The Fiber Optic transmitter uses a Hewlett Packard HFBR-1404 (low-cost miniature FO transmitter) and a Signetics 74F3037 (30 ohm driver) for the fiber interface. The 20 MHz clock is divided down to 1 MHz to provide the idle signal. Two D flip-flops detect activity in the LXT902 TP output. When the LXT902 TP signal is idle, a MUX switches the transmit signal to provide a 1 MHz idle signal to the fiber.

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Figure 1: Application Diagram

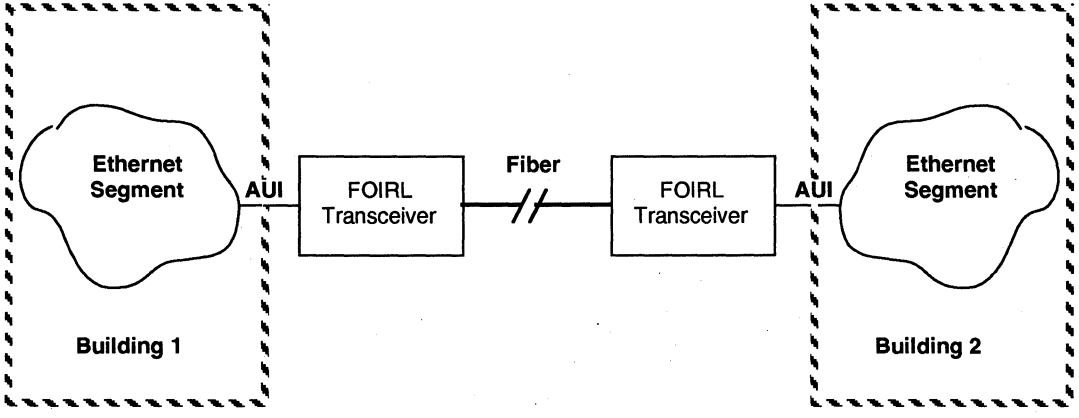


Figure 2: Application Schematic

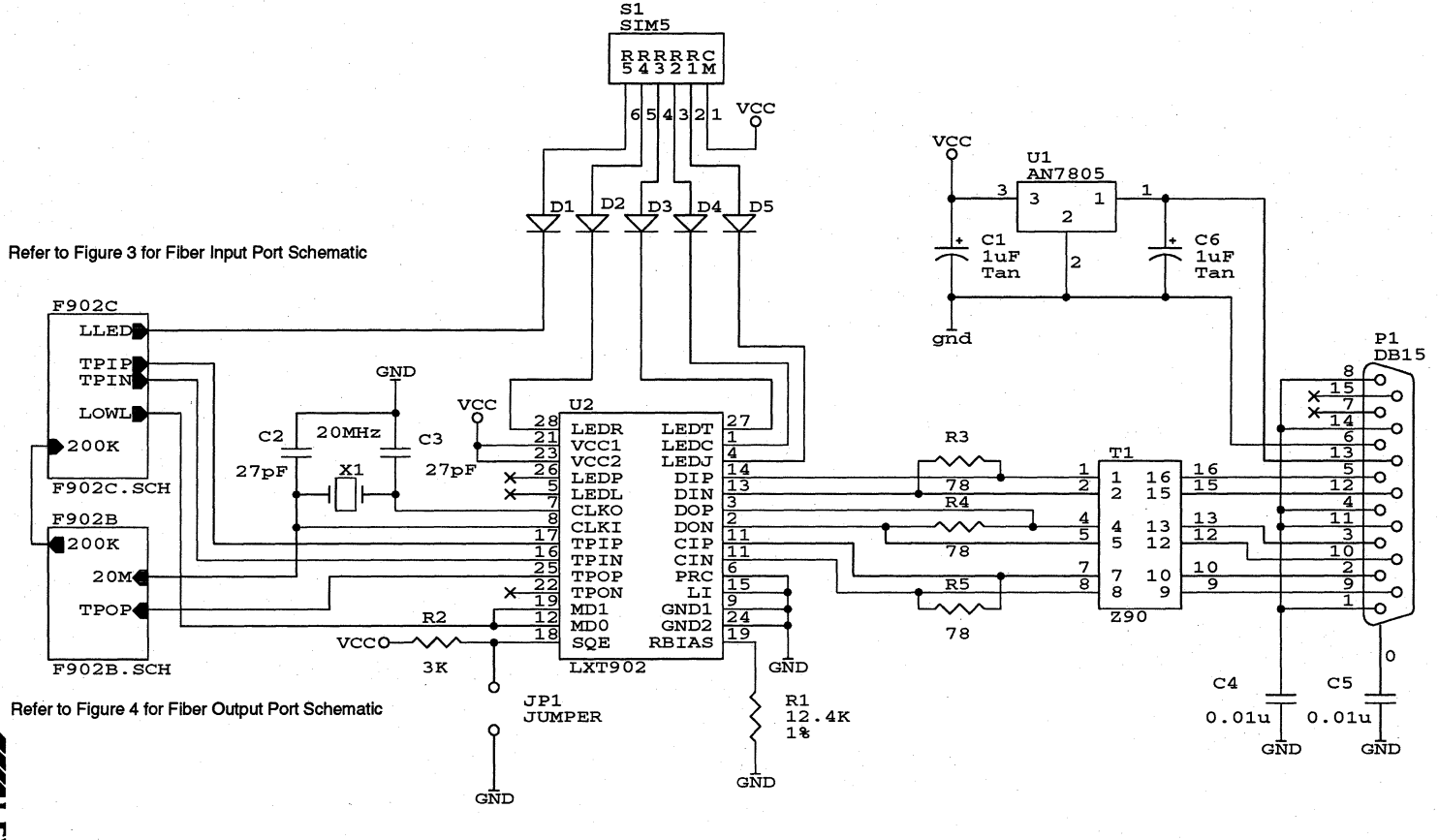


Figure 3: Fiber Input Port Schematic

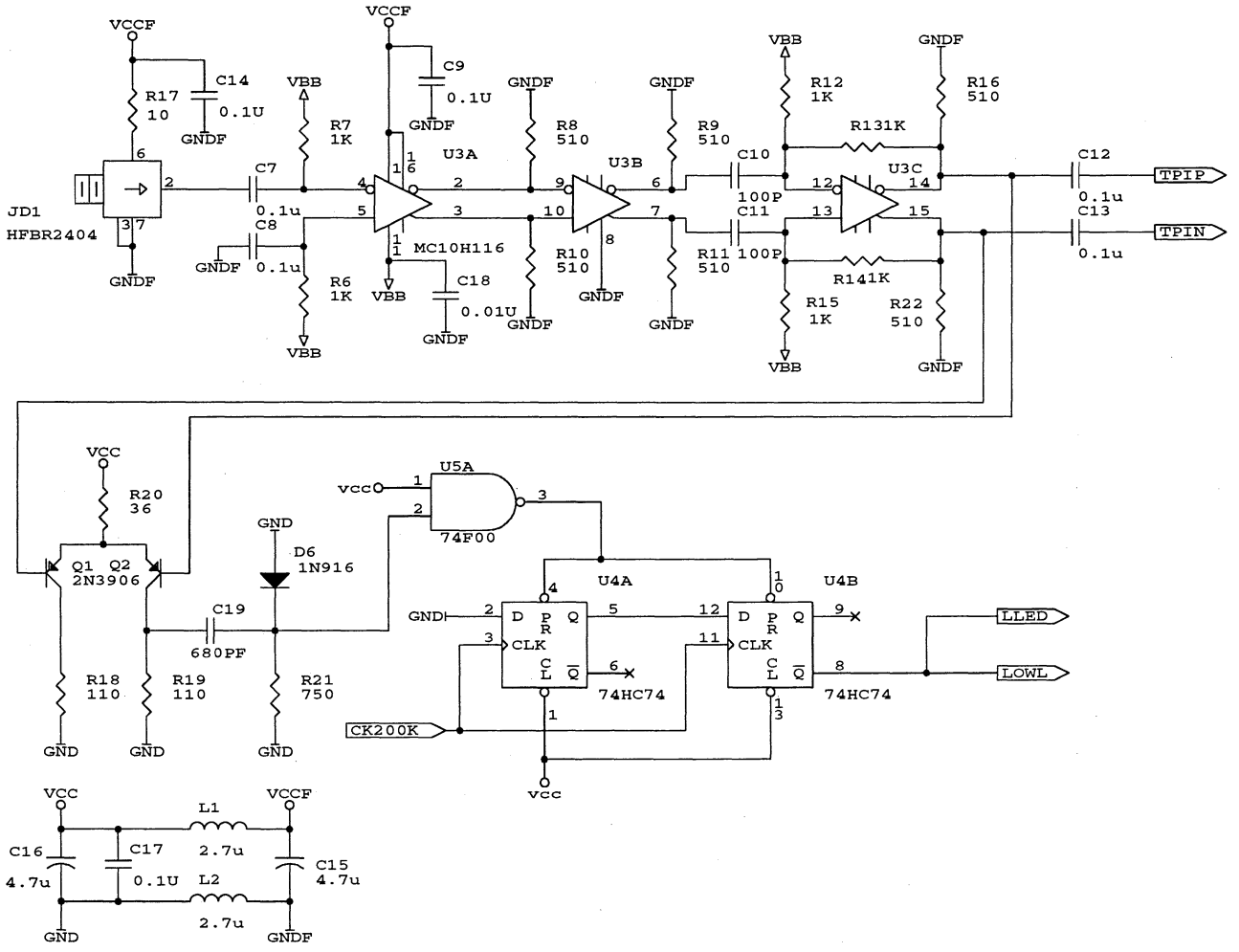
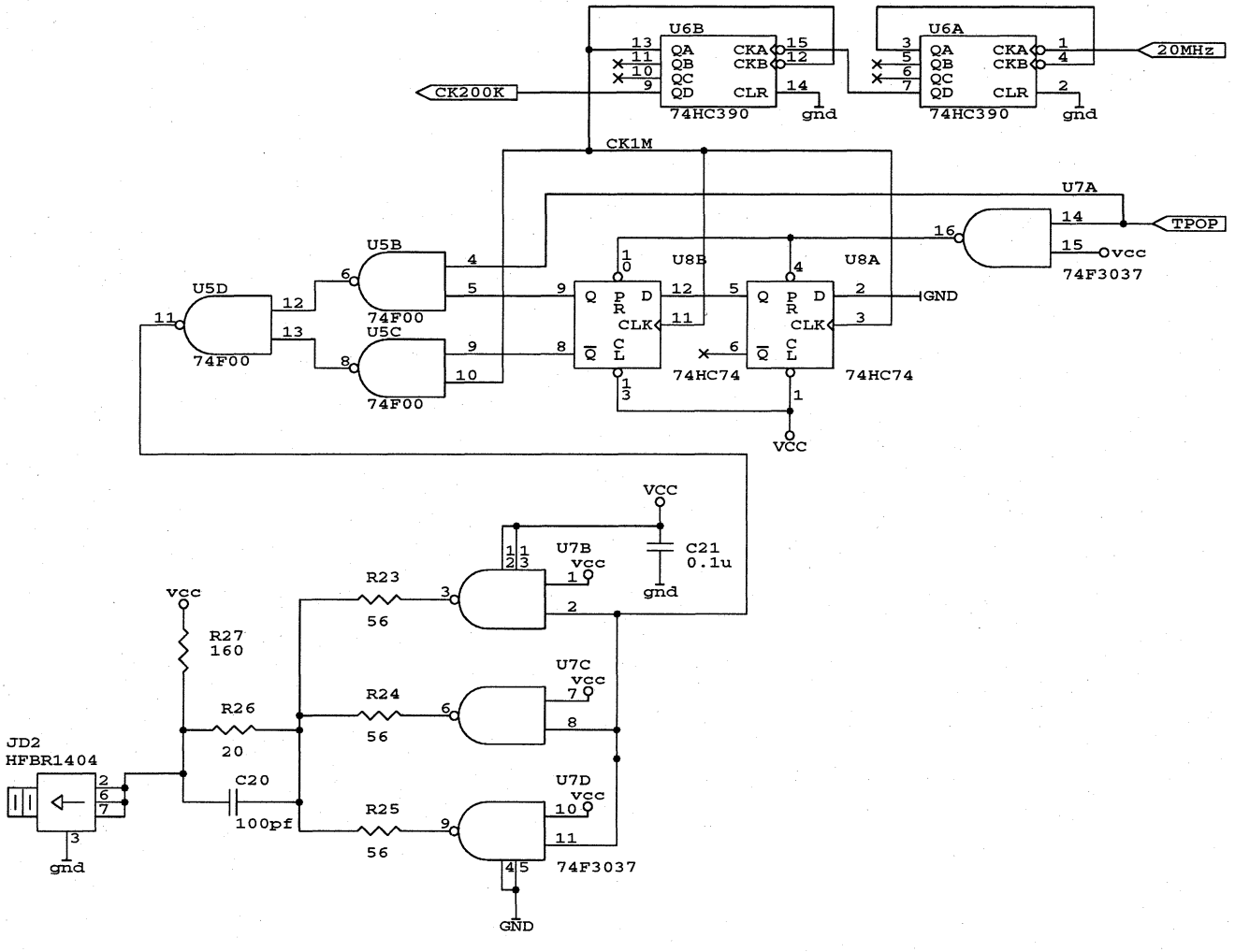


Figure 4: Fiber Output Port Schematic



Implementation

The FOIRL/Ethernet Adapter Board was built as an extension of the Level One LDB902 Demo Board. It was tested with 100 feet of 62.5/125 micron fiber, using SMA connectors. The board was tested on a five-station LAN network, using two different hubs and two different FOIRL transceivers. If space is an issue, a PAL can be used to implement the logic functions.

References

Additional information is available in the following documents:

- Level One LXT902 data sheet
- Level One LDB902 data sheet
- Level One Application Note AN-22
- National Semiconductor DP8392 data sheet
- Signetics 74F3037 data sheet
- Hewlett Packard HFBR-1404 data sheet
- Hewlett Packard HFBR-2404 data sheet
- Hewlett Packard Optoelectronics Designer's Catalog
- Hewlett Packard Application Bulletin 78
- Hewlett Packard Tech Brief 73
- ANSI/IEEE Std 802.3b,c,d, and e - 1989 Edition

Table 1: Application Parts List

Symbol	Description	Symbol	Description
Resistive Components		**Integrated Components**	
R1	12.4 kΩ 1%	U1	AN7805
R2	3 kΩ	U2	LXT902
R3,R4,R5	78 Ω	U3	MC10H116
R6,R7,R12,R13,R14,R15	1 kΩ	U4,U8	74HC74
R8,R9,R10,R11,R16,R22	510 Ω	U5	74F00
R17	10 Ω	U6	74HC390
R18,R19	110 Ω	U7	74F3037
R20	36 Ω		
R21	750 Ω	**Inductive Components**	
R23,R24,R25	56 Ω	L1,L2	2.7 µH
R26	20 Ω		
R27	160 Ω	**Miscellaneous Components**	
		D1	Green LED
Capacitive Components		D2,D3,D5	Red LED
C1,C6	1 µF Tantalum	D4	Amber LED
C2,C3	27 pF	D6	1N916
C4,C5,C18	0.01 µF	JD1	HFBR2404
C7,C8,C9,C12,C13,C14, C17,C21	0.1 µF	JD2	HFBR1404
		JP1	Jumper
C10,C11	100 pF	P1	DB15
C15,C16	4.7 µF	Q1,Q2	2N3906
C19	680 pF	S1	SIM5
C20	100 pF	T1	Z90
		X1	20 MHz

Low Cost FOIRL/Ethernet Media Conversion: LXT906 Applications

General Description

The Fiber Optic Inter-Repeater Link (FOIRL) described in the IEEE 802.3 standard can be used to interconnect two LAN Ethernet (10Base2 or 10Base5) segments. FOIRL provides a standard for connecting two Ethernet repeater units. It is suitable for interconnection of 10Base2 (thin coax) or 10Base5 (thick coax) LAN segments located in different buildings. The length of the fiber link between LAN segments is limited to 1 km.

This application note describes a very cost-effective FOIRL-to-Ethernet adapter board which can be used as shown in Figure 1. Built around the new Level One LXT906 LAN Adapter used as a repeater, this adapter uses the National Semiconductor DP8392 as a coaxial Ethernet transceiver, and other components for the Fiber Optic receive/transmit functions.

Features

- Fiber Optic Signal Reception & Transmission
- Coaxial Ethernet Reception and Transmission
- Low Light Level Signal Detection
- Fiber Optic Idle Signal Generation
- Collision Detection and Propagation
- Diagnostic LEDs

Functional Description

Fiber Optic Receiver

The Fiber Optic receiver uses a Hewlett Packard HFBR-2404 (low-cost miniature FO receiver) and a Motorola MC10H116 (ECL receiver) to convert the on-off fiber signals back into electrical signals at Attachment Unit Interface (AUI) levels. These signals are then sent to the LXT906 Twisted-Pair (TP) inputs. (The LXT906 will not trigger on a signal ≤1 MHz.)

For low-light level detection, the receive signal is converted to TTL levels. The TTL signal goes through a high-pass filter to drive an open drain buffer that discharges an RC circuit. If no on-off signal transitions are detected, low light indicator D2 is turned off and the LXT906 is forced into the reset state (code 000 at pins TST0, TST1 and TST2). It remains in the reset state until the link is reactivated.

Fiber Optic Transmitter

The Fiber Optic transmitter uses a Hewlett Packard HFBR-1404 (low-cost miniature FO transmitter) and a Signetics 74F3037 (30 ohm driver) for the fiber interface. The 20 MHz clock is divided down to 1 MHz to provide the idle signal. An RC circuit and an open drain buffer detect activity in the LXT906 TP output. When the LXT906 TP signal is idle, a MUX switches the transmit signal to provide a 1 MHz idle signal to the fiber.

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Figure 1: Application Diagram

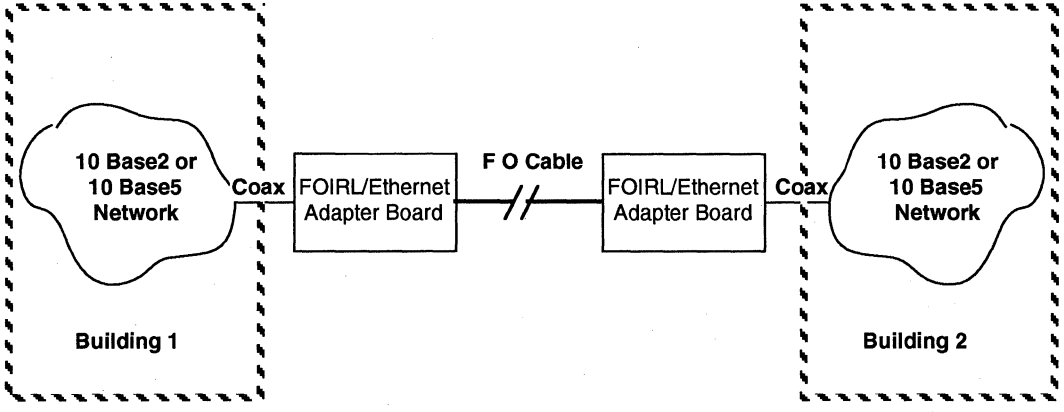

Figure 2: Application Schematic

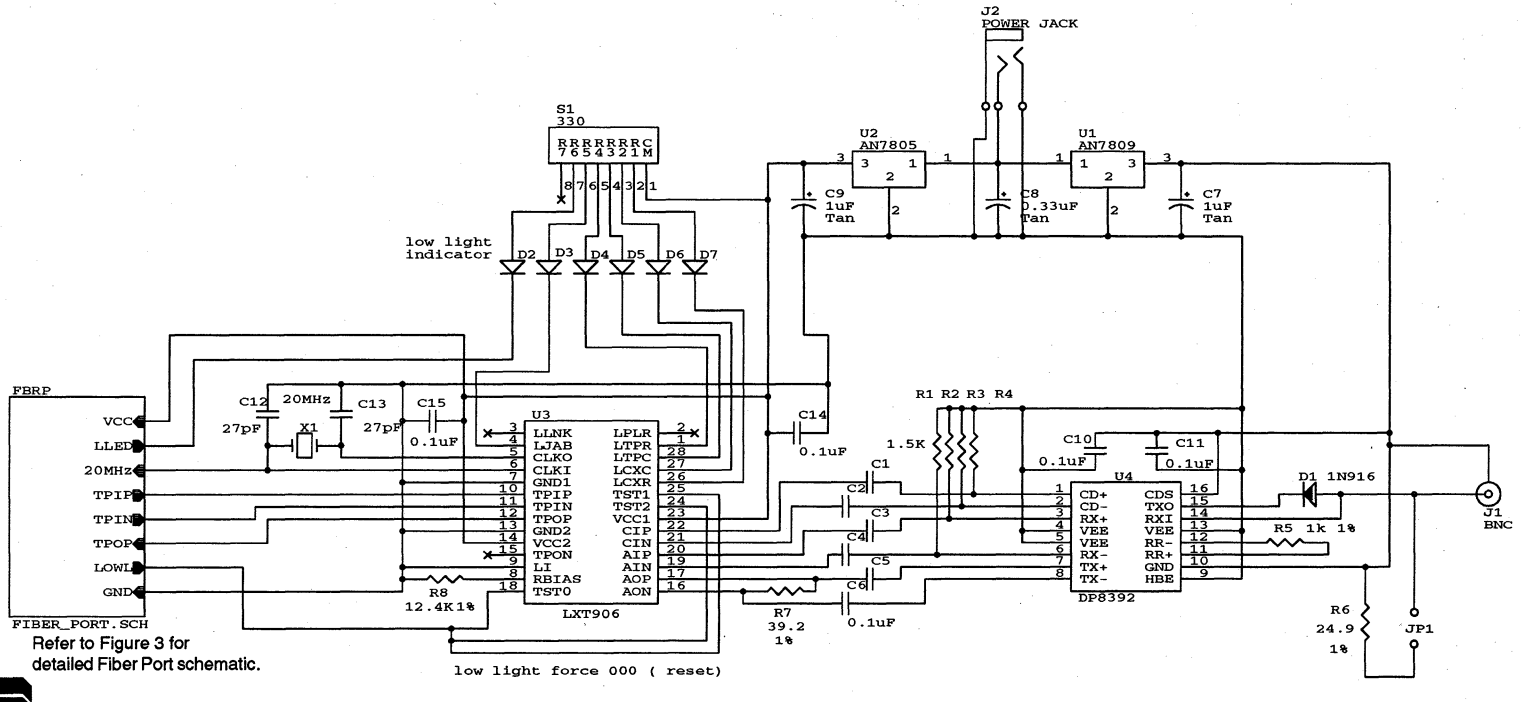

Figure 3: Fiber Port Schematic

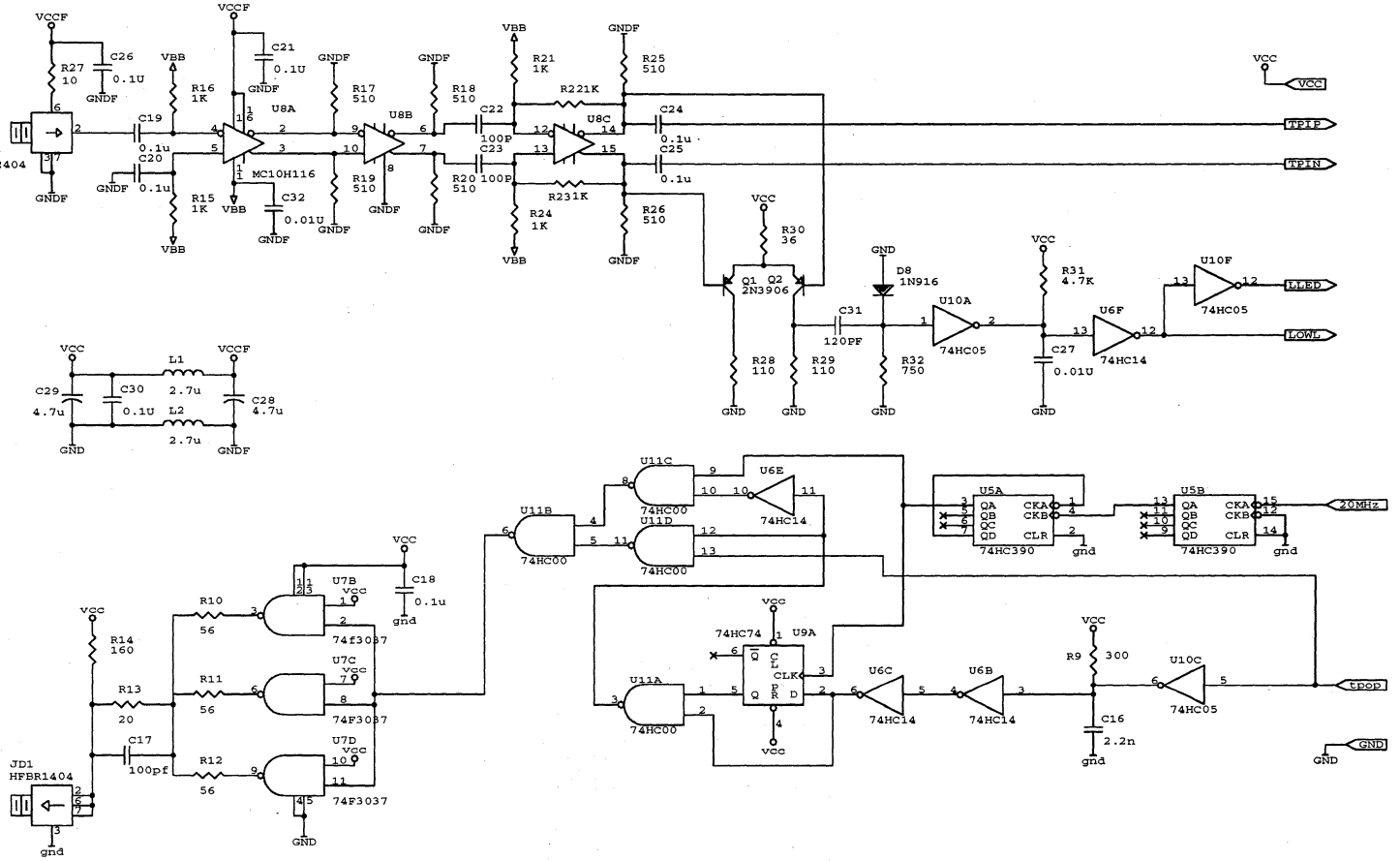

Table 1: Application Parts List

Symbol	Description	Symbol	Description
Integrated Components		**Resistive Components**	
U1	AN7809	R1,R2,R3,R4	1.5 kΩ
U2	AN7805	R5	1 kΩ, 1%
U3	LXT906	R6	24.9 Ω, 1%
U4	DP8392	R7	39.2 Ω, 1%
U5	74HC390	R8	12.4 kΩ, 1%
U6	74HC14	R9	300 Ω
U7	74F3037/ Signetics	R10,R11,R12	56 Ω
U8	MC10H116	R13	20 Ω
U9	74HC74	R14	160 Ω
U10	74HC05	R15,R16,R21,R22,R23,R24	1 kΩ
U11	74HC00	R17,R18,R19,R20,R25,R26	510 Ω
		R27	10 Ω
Capacitive & Inductive Components		R28,R29	110 Ω
C1,C2,C3,C4,C5,C6, C10, C11,C14,C15	0.1 µF	R30	36 Ω
		R31	4.7 kΩ
C7,C9	1 µF TAN	R32	750 Ω
C8	0.33 µF TAN		
C12,C13	27 pF	**Miscellaneous Components**	
C16	2.2 nF	D1,D8	1N916
C17	100 pF	D2	Green LED
C18,C19,C20,C21,C24, C25,C26,C30	0.1 µF	D3,D4,D7	Red LED
		D5,D6	Amber LED
C22,C23	100 pF	JD1	HFBR1404 / HP
C27,C32	0.01 µF	JD2	HFBR2404 /HP
C28,C29	4.7 µF	JP1	Jumper
C31	120 pF	J1	BNC Connector
		J2	Power Jack
Inductive Components		Q1, Q2	2N3906
L1,L2	2.7 µH	S1	330 Ω
		X1	Crystal, 20MHz

Implementation

The FOIRL/Ethernet Adapter Board was built as an extension of the Level One LDB906 Demo Board. It was tested with 100 feet of 62.5/125 micron fiber, using SMA connectors. The board was tested on a five-station LAN network, using two different hubs and two different FOIRL transceivers. If space is an issue, a PAL can be used to implement the logic functions.

References

Additional information is available in the following documents:

- Level One LXT906 data sheet
- Level One LDB906 data sheet
- Level One LXT902 Application Note AN-24
- National Semiconductor DP8392 data sheet
- Signetics 74F3037 data sheet
- Hewlett Packard HFBR-1404 data sheet
- Hewlett Packard HFBR-2404 data sheet
- Hewlett Packard Optoelectronics Designer's Catalog
- Hewlett Packard Application Bulletin 78
- Hewlett Packard Tech Brief 73
- ANSI/IEEE Std 802.3b,c,d, and e - 1989 Edition

Transformer Specifications
for Level One Transceiver Applications

Txcvr	Frequency (kHz)	Turns Ratio (±2%)	Inductance (μH - Min)	Leakage Inductance (μH - Max)	Interwinding Capacitance (pF - Max)	Resistance (Ω - Typ)	Dielectric Breakdown (V - Min)
LXT300 LXT301 Rx & Tx	1544 / 2048	1 : 2 CT	600 Pri	0.75 Pri	50	1.0 Pri 1.0 Sec	500
LXT304A LXT305A Rx	1544 / 2048	1 : 2 CT	600 Pri	0.75 Pri	50	1.0 Pri	500
LXT304A LXT305A Tx	1544 / 2048	1 : 1.15, 1 : 2 CT 1 : 1 1 : 1.126	600 Pri	0.75 Pri	50	1.0 Pri 1.0 Sec	500
LXT310 LXT318 Rx	1544 / 2048	1 : 1 CT	600 Pri	0.75 Pri	50	1.0 Pri 1.0 Sec	1000
LXT310 LXT318 Tx	1544 / 2048	1 : 2 CT	600 Pri	0.75 Pri	50	1.0 Pri 1.0 Sec	1000
LXT324 LXT325 Rx Only	1544 / 2048	1 : 2 : 2	600 Pri	0.75 Pri	50	1.0 Pri 1.0 Sec	500
LXT312/15 LXT313/16 Rx	1544 / 2048	1 : 1 CT	1000 Pri	1.0 Pri	25	1.0 Pri 1.0 Sec	1000
LXT312/15 LXT313/16 Tx	1544 / 2048	1:1 CT:3 CT	1000 Pri	1.0 Pri	25	1.0 Pri 1.0 Sec	1000
LXT400 Rx & Tx	2.4 to 72	1 : 1	700 Pri	22 - 43 Pri	350	15.0 Pri 15.0 Sec (± 1 Ω)	1000

Transformer Specifications

Transceiver	Application	Part Number	Manufacturer
LXT300/301 **LXT304A/5A** **LXT305**	**Tx**	PE-64931, PE-64951 67112060, 67115100 0553-5006-IC 671-5832 6500-07-011 FE 8006-55, 8006-85	Pulse Engineering Schott Corp. Bell Fuse Midcom Nova Magnetics Fil-Mag
LXT310/318	**Tx** **(1:2)**	0553-5006-IC 66Z1308 671-5832 65351, 65771 67127370 and 67130850 TD61-1205G and TD67-1205G (combo Tx/Rx)	Bell Fuse Fil-Mag Midcom Pulse Engineering Schott Corp. HALO
LXT310/318	**Rx** **(1:1)**	FE 8006-155 671-5792 64936 and 65778 67130840 and 67109510 TD61-1205G and TD67-1205G (combo Tx/Rx)	Fil-Mag Midcom Pulse Engineering Schott Corp. HALO
LXT312/315	**Tx**	12535 FE 8006-175	Schott Corp. Fil-Mag
LXT312/315	**Rx**	10951 FE 8006-155	Schott Corp. Fil-Mag
LXT901	**TP**	23Z128, 23Z128SM PT4069, SM4069 PE65994, PE65745 S553-0716, A553-0716 TD42-2006Q, TG42-2006WH1	Fil-Mag Valor Pulse Engineering Bell Fuse HALO Electronics
LXT901 **LXT902** **LXT914**	**AUI**	23Z90, 23Z90SM LT6030, SM6030 PE64502 TD01-0756K, TG01-0756W	Fil-Mag Valor Pulse Engineering HALO Electronics
LXT902 **LXT903** **LXT906**	**TP**	78Z1122B-01, 78Z1122D-01 PT3877 PE65421 FD02-101G, FD12-101G	Fil-Mag Valor Pulse Engineering HALO Electronics
LXT914	**TP** **Tx**	A553-5999-01 23Z339, 23Z339SM TD54-1006L1 5977 6038 PE68008 PT34116	Bel Fuse Fil-Mag HALO Electronics Nanopulse PCA Pulse Engineering Valor
LXT914	**TP** **Rx**	A553-5999-00 23Z338, 23Z338SM TD01-1006L1 5976 6037 PE68007 PT34117	Bel Fuse Fil-Mag HALO Electronics Nanopulse PCA Pulse Engineering Valor

Quartz Crystals for T1/E1 Transceivers

General Information

The Level One LXT300, LXT305, LXT304A, LXT305A, LXT310, and LXT318 transceivers require quartz crystals as companion devices. For the convenience of our customers, Level One buys crystals in volume from a qualified vendor, stocks them and resells them at reasonable prices in conjunction with Level One transceivers.

The LXC6176 is used in T1 applications and the LXC8192 is used in E1 applications. Specifications for the LXC6176 and LXC8192 crystals are listed below.

Level One has evaluated and qualified several crystal vendors for the benefit and convenience of our customers. We believe customers prefer to have multiple approved sources. Quartz crystals qualified for use with Level One transceivers are listed on the next page. We suggest that customers establish relations with one or more of these approved crystal suppliers and buy direct.

Crystal Specifications

Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency Stability	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)
Pullability	CL = 11.7 - 19.0 pF, +ΔF = 175 - 250 ppm CL = 19 - 34 pF, -ΔF = 175 - 250 ppm	CL = 11.7 - 19.0 pF, +ΔF = 95 - 140 ppm CL = 19 - 34 pF, -ΔF = 95 - 140 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 22 fF typical	HC49 (R3W), C_O = 7 pF maximum C_M = 13 fF typical

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Qualified Quartz Crystals

Manufacturer	Part Number	Frequency
M-Tron	3808-010 / 4144-002	6.176 MHz
M-Tron	3808-020 / 4144-001	8.192 MHz
Monitor Products	MSC-1311-01B-6.176	6.176 MHz
Monitor Products	MSC-1311-01B-8.192	8.192 MHz
CTS Knights	6176-180	6.176 MHz
CTS Knights	8192-100	8.192 MHz
Valpey Fisher	VF49A16FN1-6.176	6.176 MHz
Valpey Fisher	VF49A16FN1-8.192	8.192 MHz
US Crystal	U18-18-6176SP	6.176 MHz
US Crystal	U18-18-8192SP	8.192 MHz

Evaluation / Demonstration Boards

1994 Communications Data Book

LEVEL ONE®

February 1994

LDB901 Evaluation/Demonstration Board for the *LXT901 Universal Ethernet Interface Adapter (Internal MAU)*

General Description

The LDB901 is a full-featured 10Base-T PLS/MAU evaluation and demonstration board. It includes the LXT901 Universal Ethernet Interface Adapter and all required support components. An RJ45 connector provides the twisted-pair interface. The coax line interface is provided through a 15-pin D connector. The board provides a complete set of LED status indicators.

Movable jumpers allow operator control of selectable functions. Test points provide access to I/O signals.

This document provides board layout and schematic diagrams (Figures 1 and 2), a complete parts list, demo board specifications and a variety of oscilloscope photographs.

Figure 1: LDB901 Demo Board Layout

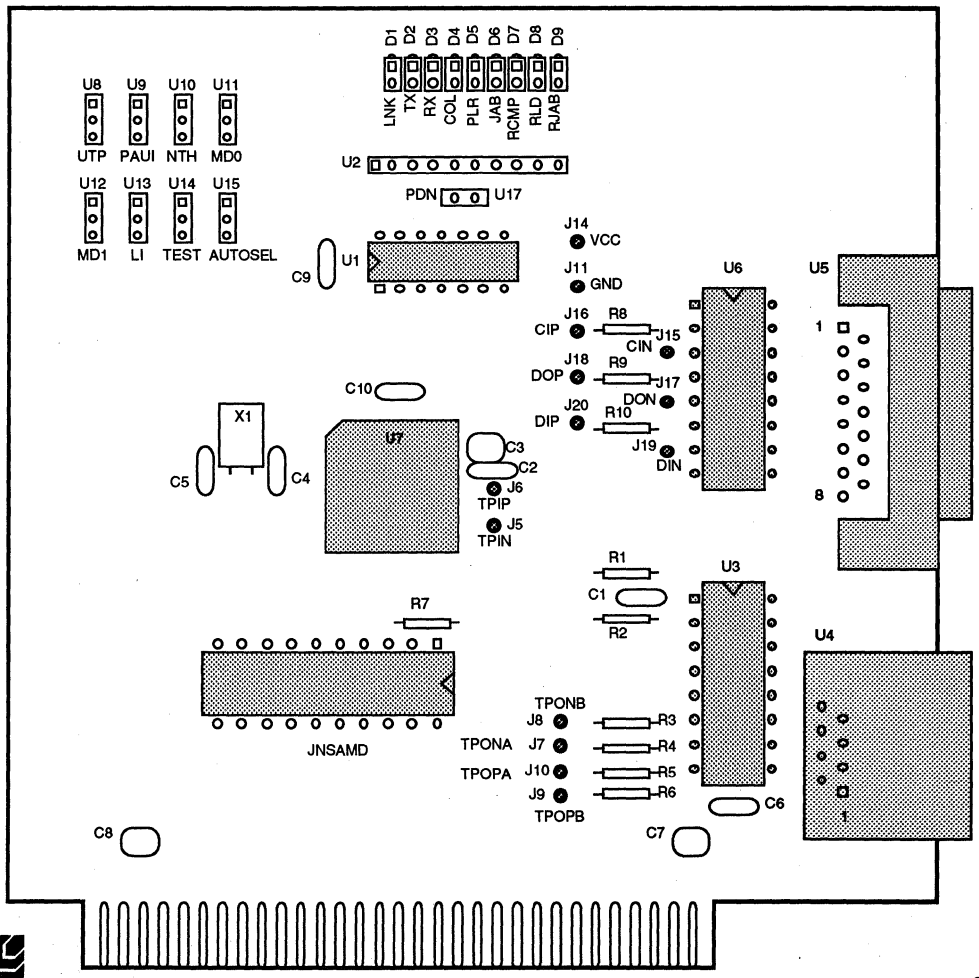


Table 1: Controller Compatibility Mode Options

To Select This Mode:	Set These Levels: MD1	MD0
Mode 1 (Compatible with Advanced Micro Devices AM7990 controllers)	0	0
Mode 2 (Compatible with Intel 82586 controllers)	0	1
Mode 3 (Compatible with Fujitsu MB86950 and MB86960 controllers)	1	0
Mode 4 (Compatible with National Semiconductor 8390 controllers)	1	1

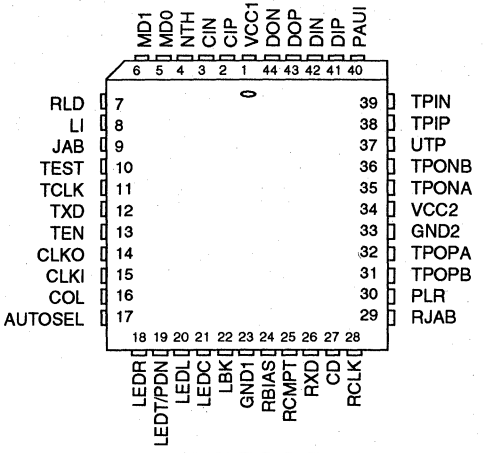


Table 2: LDB901 Parts List

Symbol	Description
Integrated Components	
U1	74HC05
U3	Bel A553-0716 Transformer [1]
U6	Bel A553-0756 Transformer [2]
Capacitive Components	
C1, C2, C9, C10	0.1 µF
C3, C7, C8	10 µF
C4, C5, C6 [3]	18 pF
Resistive Components	
R1, R2	50 Ω, 1%
R3, R6	75 Ω, 1%
R4 - R5	37.5 Ω, 1%
R7	12.4 kΩ, 1%
R8, R9, R10	78 Ω 1%Ω
U2	9-Resistor, 330 Ω Network
Connectors, Cables and Miscellaneous Components	
J5 - J11 and J14 - J20	Test Points
U8 - U15 and U17	Movable Jumpers
D1	LED, Green
D2 - D6	LED, Red
D7 - D9	LED, Amber
U4	RJ45 Connector
U5	D-Connector
JNSAMD	Custom 24-pin Ribbon Cable (VCC & GND Crossed)
X1 [3]	Crystal, 20 MHz

1: In addition to the Bell Fuse transformer installed, suitable TP transformers are also produced by Fil-Mag (23Z128 and SM23Z128), Valor (PT4069 and SM4069) and Pulse Engineering (PE65994 and PE65745).

2: In addition to the Bell Fuse transformer installed, suitable AUI transformers are also produced by Fil-Mag (23Z90 and SM23Z90), Valor (LT6030 and SM6030) and Pulse Engineering (PE64502).

3: Crystal X1 and loading capacitors C4 and C5 are not installed. The 20MHz clock is supplied through the ribbon cable to LXT901 (U7) CLKI. If an external clock is not available, these components may be installed in the positions marked.

Figure 2: Schematic Diagram of the LDB901 Evaluation / Demonstration Board

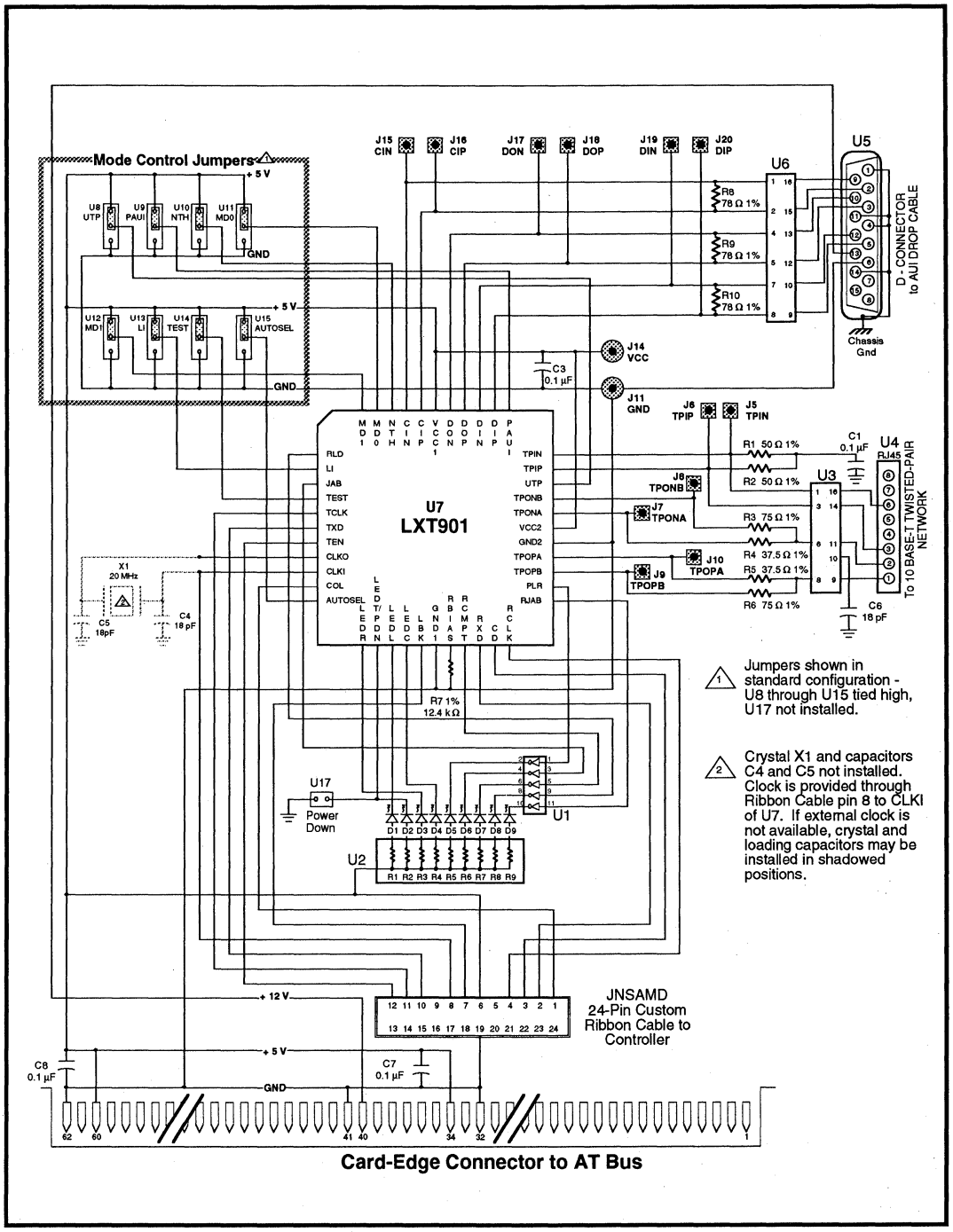


Table 3: LED Status Indicator Assignments

LED	Symbol / Name	Indication
D1 - Green	LNK / Link Integrity	Link is active
D2 - Red	TX / Transmit	Transmitter is active
D3 - Red	RX / Receive	Receiver is active
D4 - Red	COL / Collision	Collision detected
D5 - Red	PLR / Polarity	Polarity is reversed
D6 - Red	JAB / Jabber	Device is in Jabber mode
D7 - Amber	RCMPT / Remote Device Compatibility	Remote signaling compatibility
D8 - Amber	RLD / Remote Link Down	Remote link fail
D9 - Amber	RJAB / Remote Jabber	Remote device in Jabber mode

Table 4: Mode Control Jumper Assignments

Jumper	Symbol / Name	Setting
U8	UTP TP Termination Select	Set high (UTP = 1) to select 100 Ω termination for unshielded TP. Set low (UTP = 0) to select 150 Ω termination for shielded TP.
U9	PAUI Port/AUI Select	In Manual Port Select mode (AUTOSEL = 0), PAUI selects the active port. Set high (PAUI = 1) to select the AUI port. Set low (PAUI = 0) to select the TP port. In Auto Port Select mode (AUTOSEL = 1), PAUI is ignored.
U10	NTH Normal Threshold	Set high (NTH = 1) to select the normal TP squelch threshold. Set low (NTH = 0) to reduce the normal TP squelch threshold by 4.5 dB.
U11 U12	MD0 / Mode Select 0 MD1 / Mode Select 1	Select controller compatibility modes in accordance with Table 1.
U13	LI Link Integrity	Set high (LI = 1) to enable Link Integrity Test function. Set low (LI = 0) to disable Link Integrity Test function.
U14	TEST / Test	Leave this pin floating or connect it to VCC.
U15	AUTOSEL Automatic Port Select	Set high (AUTOSEL = 1) to enable automatic port selection. (When auto selection is enabled, the 901 defaults to the TP port unless the Link Integrity Test fails.) Set low to enable manual port selection with PAUI jumper.
U17	PDN Power Down	When left open, normal operation is enabled. When this jumper is inserted (PDN = 0) the LXT901 powers down.

Table 5: RJ45 Twisted-Pair Connector U4 Pin Assignments

Pin	Symbol	Name / Description
1	TPOP	TP Data Out Positive
2	TPON	TP Data Out Negative
3	TPIP	TP Data In Positive
4	NC	No connection
5	NC	No connection
6	TPIN	TP Data In Negative
7	NC	No connection
8	NC	No connection

Table 6: D-Type AUI Connector U5 Pin Assignments

Pin	Symbol	Name / Description
1	GND	Ground
2	CIP	AUI Collision Input Positive
3	DOP	AUI Data Out Positive
4	GND	Ground
5	DIP	AUI Data In Positive
6	GND	Power Supply ground return, tied to J11
7	NC	No connection
8	NC	No connection
9	CIN	Collision In Negative
10	DON	AUI Data Out Negative
11	GND	Ground
12	DIN	AUI Data In Negative
13	+ 12 V	Tied to AT Bus edge connector pin 40
14	GND	Ground
15	NC	No connection

Table 7: Ribbon-Type Connector J-NS/AMD Pin Assignments

Pin	Symbol	Name / Description
1	COL	Collision output to controller
2	RXD	Receive Data output to controller
3	CD	Carrier Detect output to controller
4	RCLK	Recovered 10 MHz clock
5, 9 & 13 - 18	NC	No connection
6	VCC	+ 5 V, tied to J14
7	LBK	Loopback input from controller
8	CLKI	Tied to 20MHz crystal oscillator
10	TXD	Transmit Data input from controller
11	TCLK	Transmit Clock input from controller
12	TEN	Transmit Enable input from controller
19	GND	Ground
20 - 24	NC	No connection

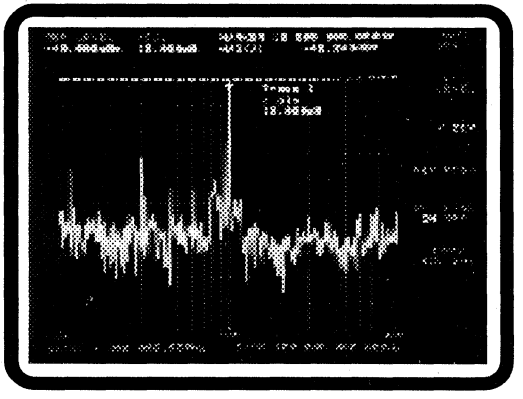
Oscilloscope Photographs

As shown in Figures 3 through 8, the LXT901 fully meets all requirements of the 10Base-T specification. Figures 9 through 11 illustrate compatibility with various controllers. Figures 12 through 21 compare jitter measurements of the LXT901 and LXT902 before and after the twisted-pair line model.

Transmit Harmonics

Figure 3 is a spectrum analysis display of the LXT901 operating in the Transmit All Ones (TAOS) mode. All harmonics are at least 35 dB below the fundamental frequency.

Figure 3: Spectrum Analysis in TAOS Mode



Random Data

Figures 4A and 4B show waveforms produced by 512 bits of random data after transmission through simulated 10Base-T line models. The figures also show the 10Base-T waveform template and jitter specifications superimposed over the measured waveform.

TP Idle Pulse

Figures 5A and 5B show the TP Idle pulse with the Start of TP_Idle template. Figure 5A was measured at the TP outputs of the RJ45 connector. Figure 5B shows the pulse measured after the 10Base-T line model.

Link Test Pulse

Figures 6A and 6B show the Link Test pulse with the Link Test template. Figure 6A was obtained at the TP outputs of the RJ45 connector, and Figure 6B shows the pulse measured after the 10Base-T line model.

AUI Pulse Waveform

Figure 7 shows the DI signal waveform, measured at the AUI interface.

End Of Frame

Figure 8 shows the End Of Frame (EOF) pulse measured at the DI input to the LXT901.

Figure 4A: Random Data after the 100 Ω Line Model (Waveform template and Jitter spec.)

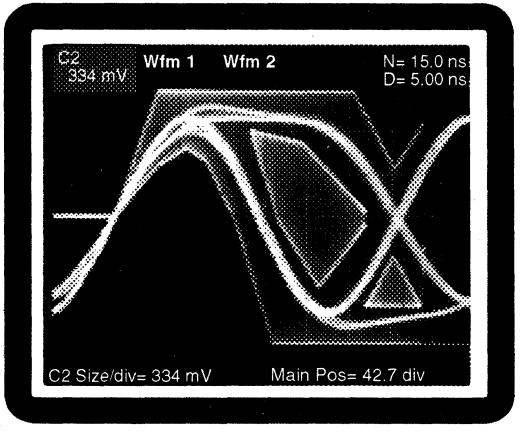


Figure 4B: Random Data after the 150 Ω Line Model (Waveform template and Jitter spec.)

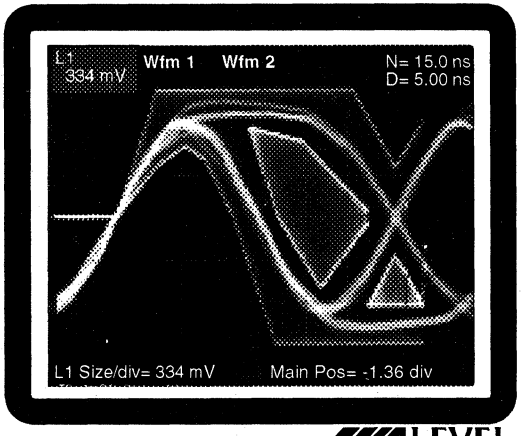


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Figure 5A: TP Idle Pulse before Line Model with Test Load

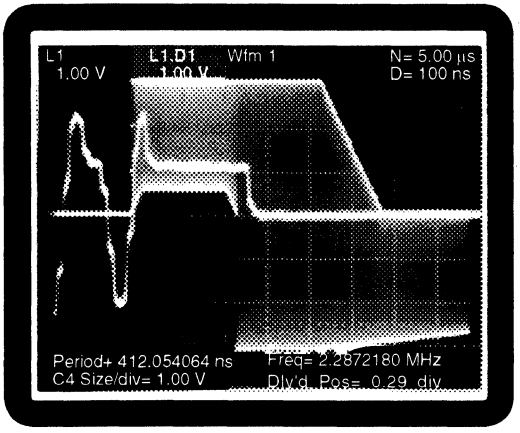


Figure 5B: TP Idle Pulse after Line Model with Test Load

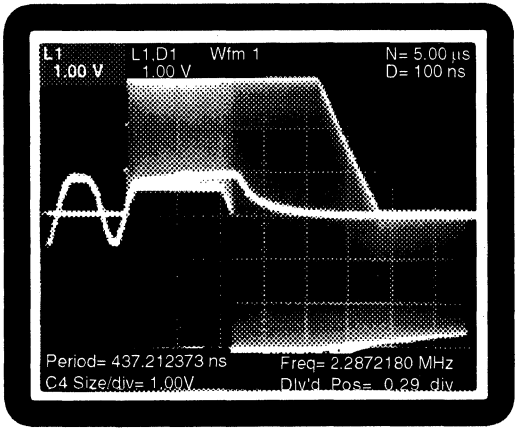


Figure 6A: Link Test Pulse before Line Model

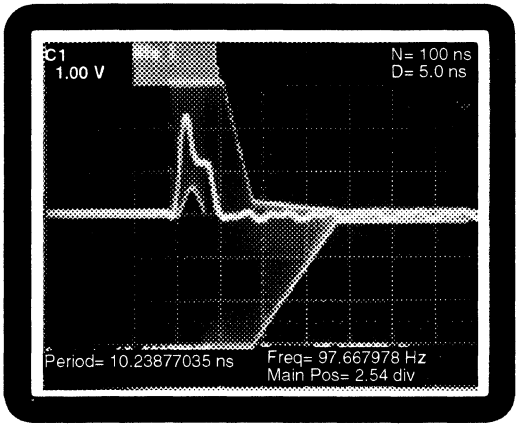


Figure 6B: Link Test Pulse after Line Model

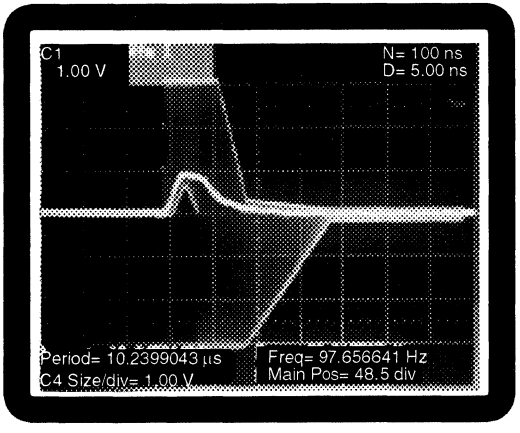


Figure 7: DI (AUI) Rise time < 5 ns with Test Load (Transformer Coupling)

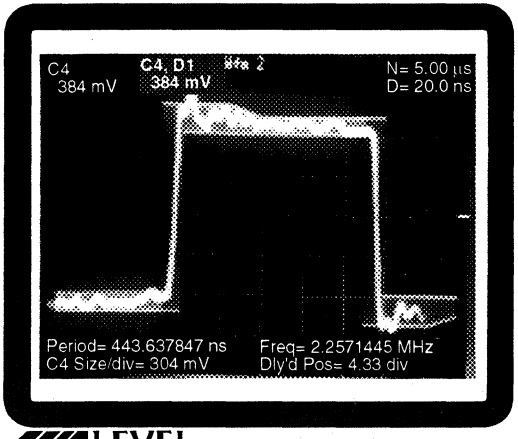
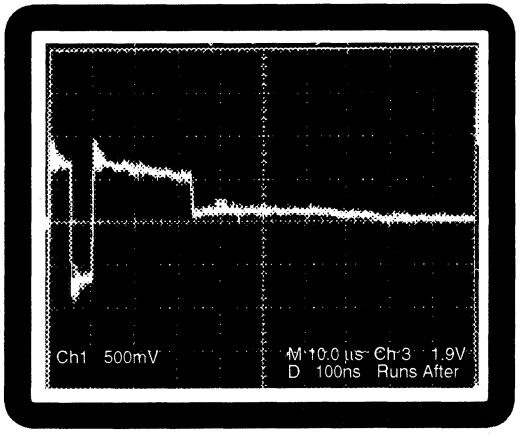


Figure 8: End Of Frame Pulse



6

LXT901 / Controller Compatibility

Figures 9, 10 and 11 are oscilloscope photographs showing start-of-frame (SOF) and end-of-frame (EOF) signals for Modes 2, 3 and 4, respectively. (Mode 1 is similar to Mode 4.)
Each figure shows:

TPI (Twisted-Pair Input),
RXD (Received Data Output),
RCLK (Recovered Clock) and
CD (Carrier Detect).

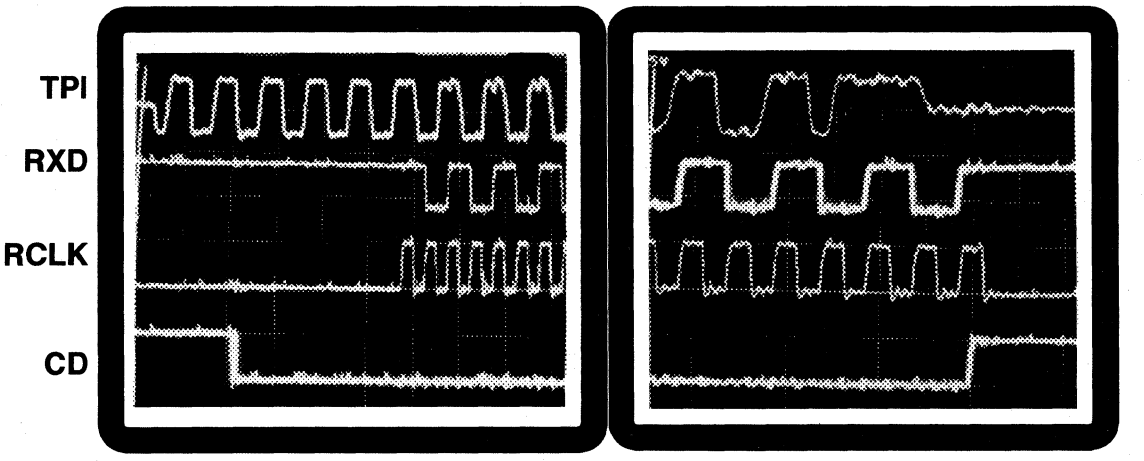
For each pair of oscilloscope photos, figure A shows SOF alignment and figure B shows EOF alignment.

Figures 9A and 9B show Mode 2 frame alignment signals. Mode 2 is compatible with Intel 82586 controllers.

Figures 10A and 10B show Mode 3 frame alignment signals. Mode 3 is compatible with Fujitsu MB86950 and 86960 controllers.

Figure 9A: Mode 2 Start of Frame

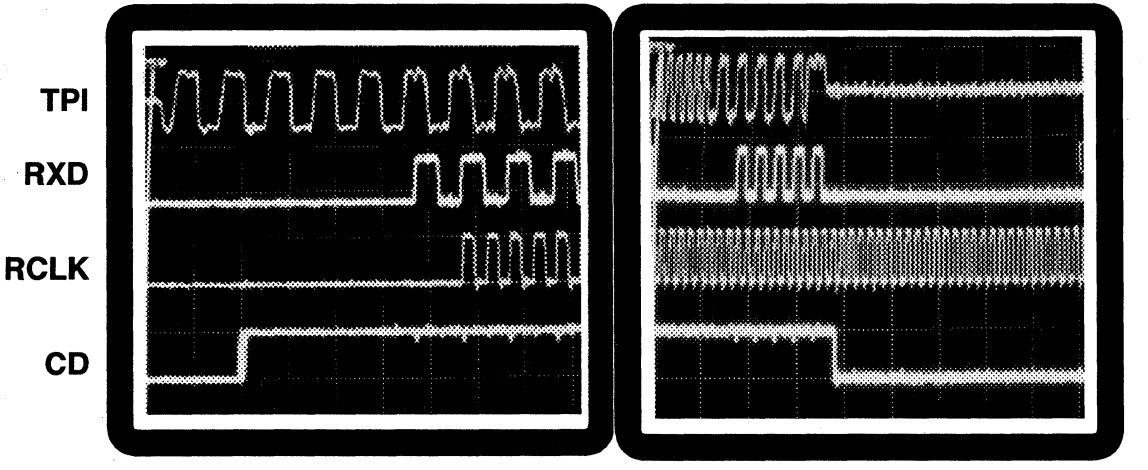
Figure 9B: Mode 2 End of Frame



(Mode 2 : Compatible with Intel Corporation 82586 controllers.)

Figure 10A: Mode 3 Start of Frame

Figure 10B: Mode 3 End of Frame

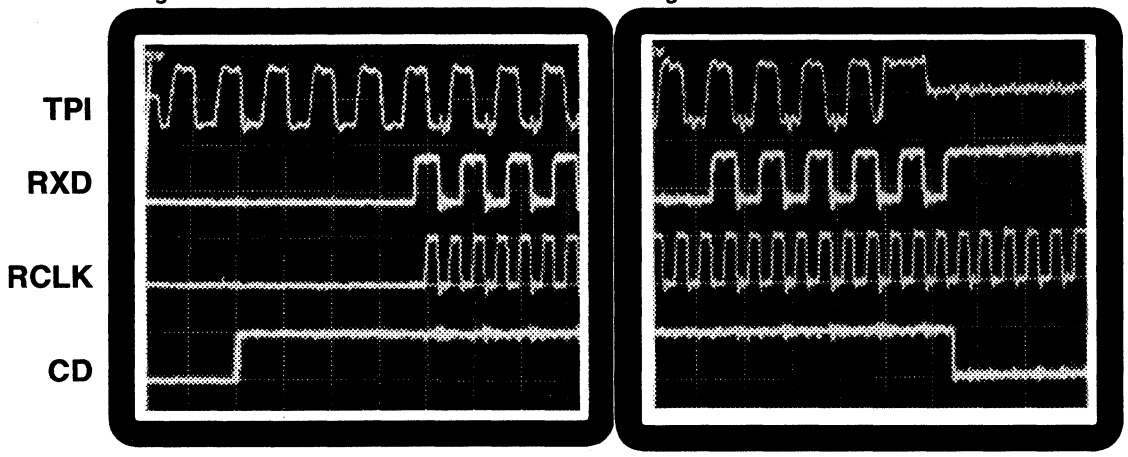


(Mode 3 : Compatible with Fujitsu MB86950 and 86960 controllers.)

Figures 11A and 11B show Mode 4 frame alignment signals. Mode 4 is compatible with National Semiconductor NS8390 controllers. (Controller compatibility Mode 1, compatible with Advanced Micro Devices AM7990 controllers, is similar.)

Figure 11A: Mode 4 Start of Frame

Figure 11B: Mode 4 End of Frame



(Mode 4 : Compatible with National Semiconductor NS8390 controllers.
Mode 1, compatible with Advanced Micro Devices AM7990 controllers, is similar.)

LXT901 / LXT902 Jitter Comparisons

Figures 12 through 21 are jitter performance comparisons of the LXT901 internal MAU and the LXT902 external MAU. Each pair of oscilloscope photographs shows the LXT901 on the left and the LXT902 on the right. The first six photos (Figures 12 through 17) show 0 line length measurements. The remaining four photos (Figures 18 through 21) show measurements taken after the 10Base-T line model. Tables 8 and 9 list the applicable 802.3 specifications for the LXT901 and LXT902, respectively, and the actual oscilloscope measurements.

0 Line Length Measurements

Preamble

Figures 12 and 13 show preamble output jitter. The 10Base-T specification is ± 8 ns. The LXT901 output jitter (Figure 12) is ± 1.4 ns. The LXT902 output jitter (Figure 13) is ± 3 ns.

Table 8: LXT901 Jitter Specs and Measurements

Section	802.3 Spec Internal MAU	LXT901 Measurement
Preamble	± 8.0 ns	± 1.4 ns
Random Data		
0 line length	± 10.0 ns	± 6.4 ns
after line model	± 5.5 ns	± 3.4 ns

Table 9: LXT902 Jitter Specs and Measurements

Section	802.3 Spec External MAU	LXT902 Measurement
Preamble	± 8.0 ns	± 3.0 ns
Random Data		
0 line length	± 8.0 ns	± 6.6 ns
after line model	± 3.5 ns	± 3.5 ns

Random Data

Figures 14 through 17 show random data output jitter. The 10Base-T specification for Internal MAUs (LXT901) is ± 10 ns. With a Rising Edge Trigger (Figure 14), the LXT901 output jitter is ± 6.4 ns. With a Falling Edge Trigger (Figure 16), the LXT901 output jitter is ± 6.0 ns. The 10Base-T specification for External MAUs (LXT902) is ± 8 ns. With a Rising Edge Trigger (Figure 15), the LXT902 output jitter is ± 6.6 ns. With a Falling Edge Trigger (Figure 17), the LXT902 output jitter is ± 6 ns.

Line Model Measurements

Figures 18 through 21 show random data output jitter after the line model. The 10Base-T specification for an internal MAU (LXT901) is ± 5.5 ns. With a Rising Edge Trigger (Figure 18), the LXT901 output jitter is ± 3.2 ns. With a Falling Edge Trigger (Figure 20), the LXT901 output jitter is ± 3.4 ns. The 10Base-T specification for an external MAU (LXT902) is ± 3.5 ns. With a Rising Edge Trigger (Figure 19), the LXT902 output jitter is ± 3.5 ns. With a Falling Edge Trigger (Figure 21), the LXT902 output jitter is ± 3.2 ns.

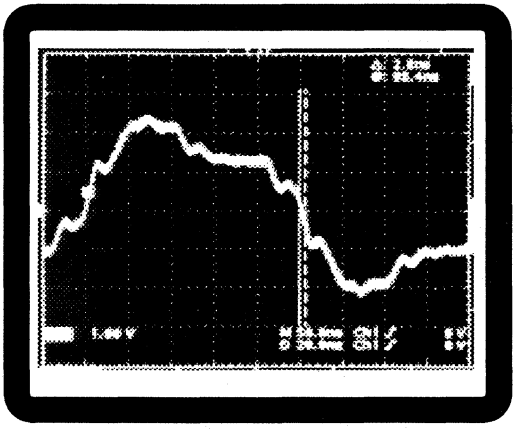


Figure 12: LXT901 Preamble Output Jitter (0 Line Length)

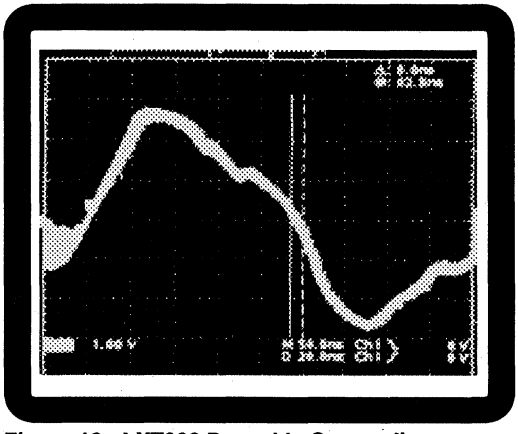


Figure 13: LXT902 Preamble Output Jitter (0 Line Length)

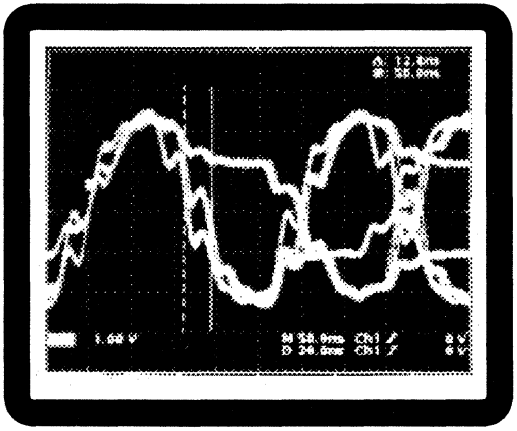


Figure 14: LXT901 Random Data Output Jitter (0 Line Length - Rising Edge Trigger)

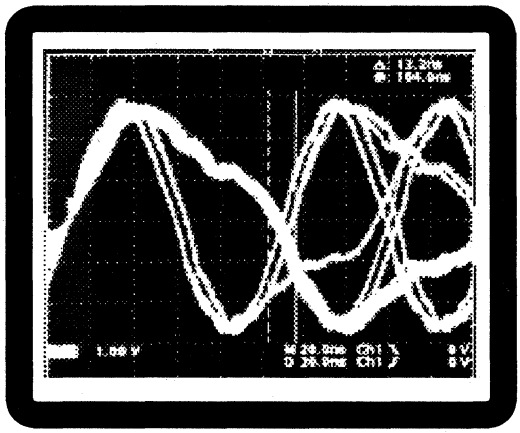


Figure 15: LXT902 Random Data Output Jitter (0 Line Length - Rising Edge Trigger)

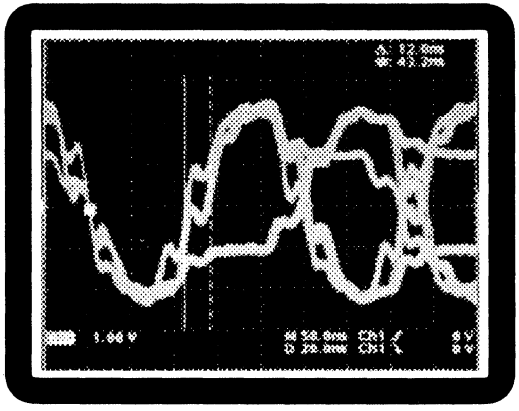


Figure 16: LXT901 Random Data Output Jitter (0 Line Length - Falling Edge Trigger)

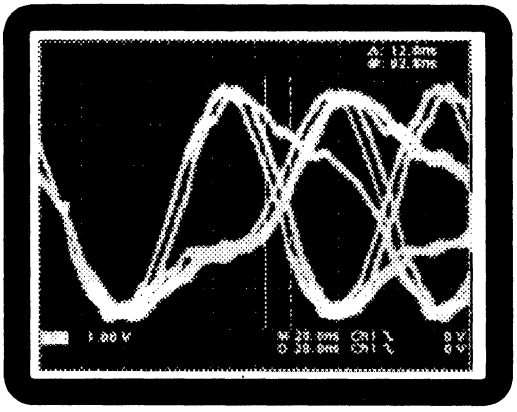


Figure 17: LXT902 Random Data Output Jitter (0 Line Length - Falling Edge Trigger)

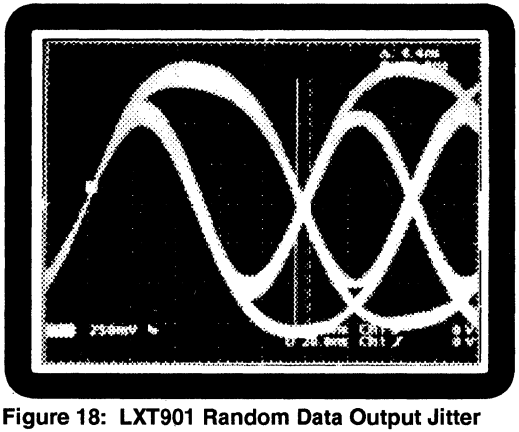


Figure 18: LXT901 Random Data Output Jitter (After Line Model - Rising Edge Trigger)

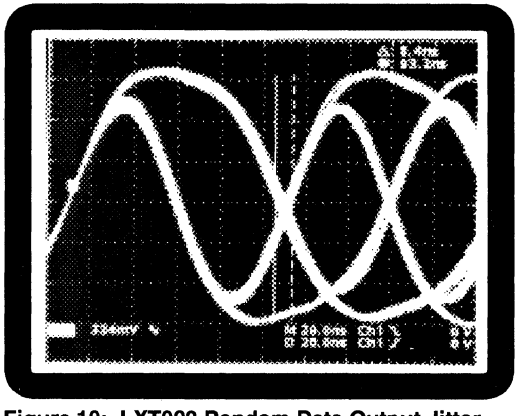


Figure 19: LXT902 Random Data Output Jitter (After Line Model - Rising Edge Trigger)

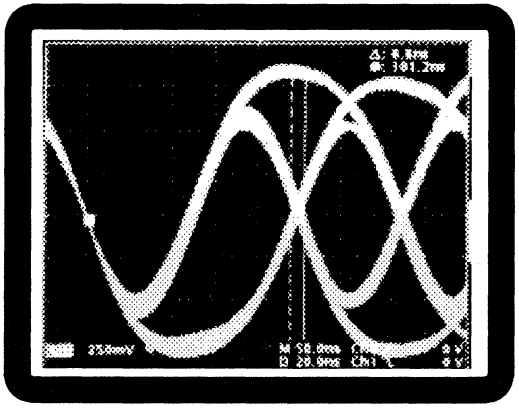


Figure 20: LXT901 Random Data Output Jitter (After Line Model - Falling Edge Trigger)

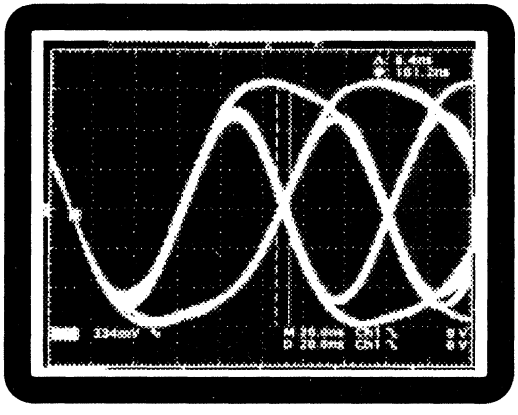


Figure 21: LXT902 Random Data Output Jitter (After Line Model - Falling Edge Trigger)

NOTES:

LDB902 Evaluation/Demonstration Board for the LXT902 10Base-T Media Attachment Unit

General Description

The LDB902 is a full feature 10Base-T MAU evaluation/demonstration board. It includes the LXT902 Ethernet Twisted Pair Media Attachment Unit and all required support components.

The board provides LED status lights for Link, Jabber, Receive, Transmit, Collision and Polarity Reverse. Control switches are provided for Mode 0, Mode 1, SQE test enable, link test enable and polarity correction enable. A 15-pin D connector provides the AUI side interface and an RJ45 jack connects the MAU to the twisted-pair line.

Features

- Meets or exceeds IEEE 802.3 standards for 10Base-T interface
- Socketed LXT902 (PLCC)
- All required components for complete evaluation
- Control of all LXT902 modes
- LED status indicators
- Transmit and receive filters.

Figure 1: LDB902 Block Diagram

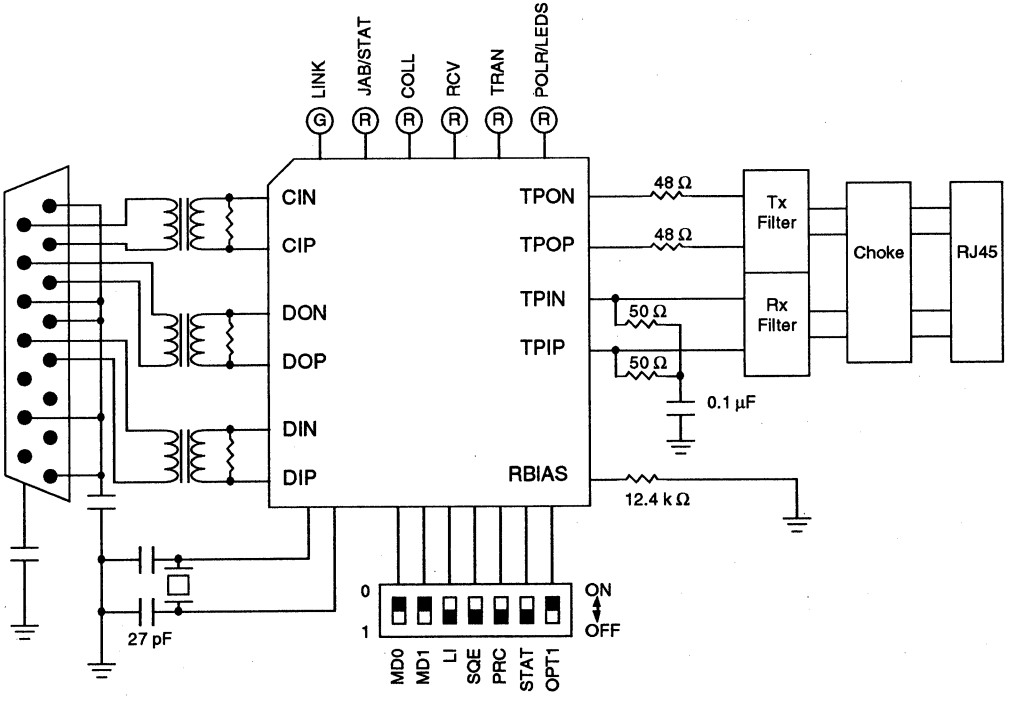


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Table 1: LDB902 Parts List (See Figure 8 for complete schematic)

Symbol	Description
Integrated Components	
U1	LXT902 (in 28-pin socket)
U2	7805CT , 5V voltage regulator
Inductive Components	
T1	Fil-Mag 23Z90 (in 16-pin socket)
T3	Fil-Mag 23Z81, 14-pin DIP, dual choke
T4	Fil-Mag 78Z1120B, or Valor PT3877 filter
Resistive Components	
R1 - R2	78.7 Ω, 1%
R3 - R4	39.2 Ω, 1%
R5	12.4 kΩ, 1%
R6 - R7	47.5 Ω, 1%
R10 - R11	49.9 Ω, 1%
RP1	7-Resistor, 330 Ω network
RP2	5-Resistor, 22 kΩ network
Capacitive Components	
C1-C2	27 pF
C3	1 µF, tantalum
C4	0.1 µF
C5	0.33 µF, tantalum
C6	1 µF
C7	1 µF
C8	0.1 µF
C9	1.0 nF, 5 kV
C10	1.0 nF, 5 kV
Miscellaneous Components	
L1	Miniature green LED
L2-L6	Miniature red LED
X1	20 MHz (± 1%) crystal[1]
J1	8-position, 8-circuit modular RJ45 jack
J2	15-pin male D-connector
S1	7 position switch

Note 1. Ceramic resonator can be used in place of crystal in customer applications.

Functional Description

The LDB902 Evaluation/Demonstration Board interfaces the Attachment Unit Interface (AUI) to the unshielded twisted-pair cables, transferring data in both directions.

AUI Interface

The AUI side of the interface comprises three circuits: Data Output (DO), Data Input (DI) and Control Interface (CI). A 15-pin male D-connector (J2) provides the interface to the AUI cable. As shown in Figure 1, termination resistors are provided for CIP/CIN, DIP/DIN and DOP/DON. A transformer isolates the LXT902 from the AUI connector. The connector shields are shorted together. The shields and the connector shell are connected to ground through a high-voltage capacitor. Pin assignments for the D-connector are listed in Table 2.

Twisted-Pair Interface

The twisted pair network side of the interface comprises two circuits: Twisted Pair Input (TPI) and Twisted Pair Output (TPO). An RJ45 jack (J1) provides the interface to the twisted-pair line. As shown in Figure 1, the LXT902 is connected to the RJ45 jack through transmit and receive filters and the data line filter (a choke). Pin assignments for the RJ45 jack are listed in Table 3.

Control and Status Circuits

In addition to the AUI and twisted-pair interfaces, the LDB902 provides a complete set of mode control switches (switch assembly S1) and LED status indicators (L1 - L6). Each of the five mode control switches is connected to a pull-up resistor and can be shorted to ground. Switch assignments and settings are listed in Table 4.

Status indications are provided by the six on-board LEDs. Although 10 mA LEDs are provided on the demo board, the LXT902 is also directly compatible with high efficiency 2 mA LEDs which can be used for reduced power consumption. LED assignments and functions are listed in Table 5.

Power Supply

The LDB902 requires a 12 - 15 volt input on pin 13 of the D-connector. On-board +5 V voltage regulation is provided by voltage regulator U2. U2 may require a heat sink, depending on application.

Table 2: D-Connector J2 Pin Assignments

Pin	Symbol	LDB902 Connection	Description
3	DO-A	Transformer-DOP	Data Out positive
10	DO-B	Transformer-DON	Data Out negative
11	DO-S	Cap	Data Out shield
5	DI-A	Transformer-DIP	Data In positive
12	DI-B	Transformer-DIN	Data In negative
4	DI-S	Cap	Data In shield
7	NC	No Connection	No connection
15	NC	No Connection	No connection
8	CO-S	Cap	
2	CI-A	Transformer-CIP	Collision In positive
9	CI-B	Transformer-CIN	Collision In negative
1	CI-S	Cap	Collision In shield
6	Vc	GND	Voltage common
13	VP	VCC	Voltage plus
14	VS	Cap	Voltage shield
Shell	PG	Cap	Protective ground

Table 3: RJ45 Connector J1 Pin Assignments

Pin	Symbol	Name	Description
1	TD+	TPOP-filter	Data Out positive
2	TD-	TPON-filter	Data Out negative
3	RD+	TPIP-filter	Data In positive
4	NC	No Connection	No connection
5	NC	No Connection	No connection
6	RD-	TPIN-filter	Data In negative
7	NC	No Connection	No connection
8	NC	No Connection	No connection

Table 4: Mode Control Switch S1 Assignments

Switch	Symbol	Name	Setting
1	MD0	Mode select 0	MD1 / MD0 / Mode ON / ON / 10BT compliant MAU ON / OFF / Reduce squelch (3 dB) OFF / ON / Half current AUI driver OFF / OFF / DO, DI & CI ports disabled
2	MD1	Mode select 1	
3	LI	Link test enable	ON = Disable, OFF = Enable
4	SQE	Signal quality test enable (heart beat)	ON = Disable, OFF = Enable
5	PRC	Polarity correction enable	ON = Disable, OFF = Enable
6	STAT	Serial Status Light enable	ON = LEDP indicates serial status OFF = LEDP indicates polarity reverse
7	OPT1	Customer Option 1	Not Connected

Table 5: LED Status Indicator Assignments

LED	Color	Name	Indication
1	Green	Link Integrity	Link is active
2	Red	Jabber	Jabber is active
3	Red	Collision	Collision is active
4	Red	Receive	Receive is active
5	Red	Transmit	Transmit is active
6	Red	Polarity	Polarity is reversed[1]

Note 1: When S1 Switch STAT is set to ON, the Polarity LED becomes a blinking status indicator. Refer to the LXT902 Data Sheet for additional information on the status indications.

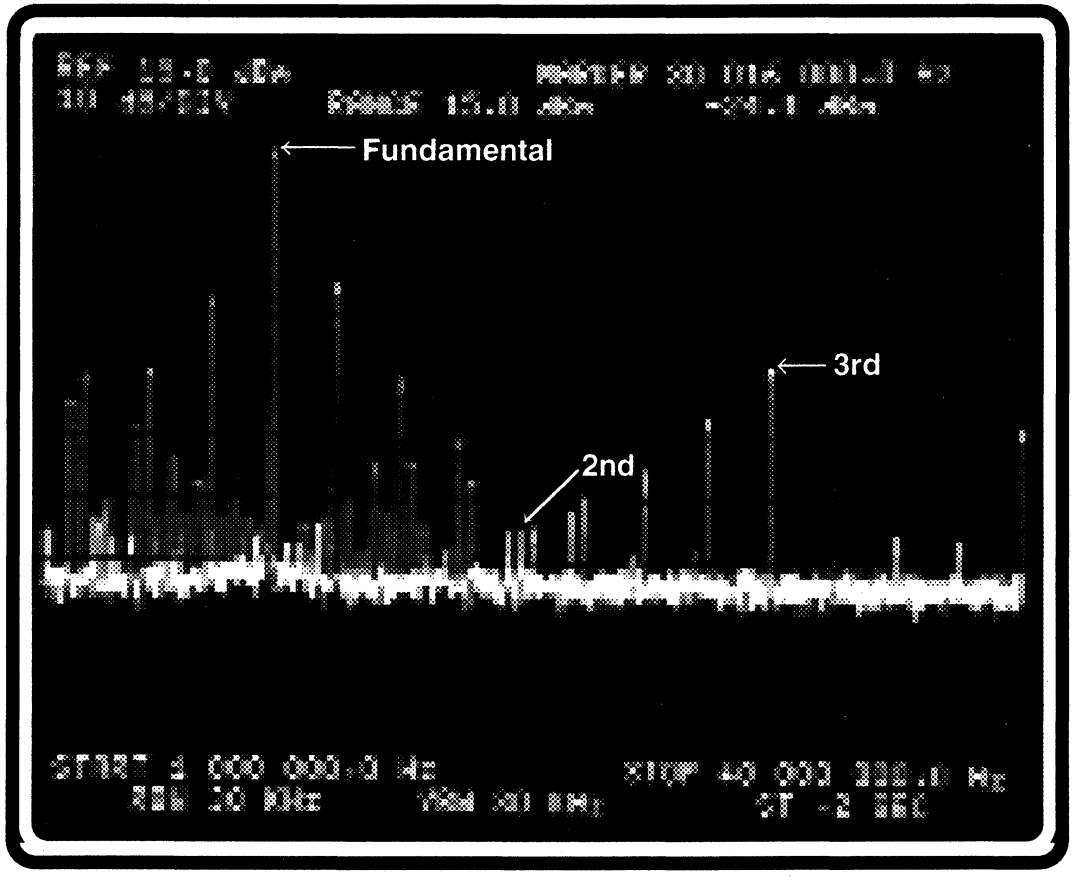
Test Measurements

The LDB902 Evaluation/Demonstration Board provides access to all signals and waveforms required to fully evaluate the LXT902. A variety of measurements are included here for comparison purposes. As shown in the scope photographs (Figures 2 through 7), the LXT902 fully meets all requirements of the 10Base-T specification.

Transmit Harmonics

Figure 2 is a spectrum analysis display of the LXT902 operating in the Transmit All Ones (TAOS) mode. The second and third harmonics, noted on the photo, are at least 35 dB below the fundamental frequency.

Figure 2: Transmit All One's - All harmonics are at least -35 dB from fundamental



6

Random Data

Figures 3A and 3B show 512 bits random data waveforms, before and after the line model. Figure 3A shows the waveform at the TP output of the RJ45 connector. Figure 3B shows the waveform after transmission through a simulated 10Base-T line model. Figure 3B also shows the 10Base-T waveform template and jitter specifications superimposed over the measured waveform.

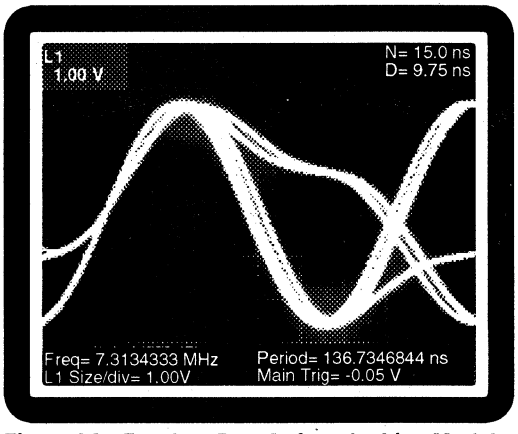


Figure 3A: Random Data before the Line Model

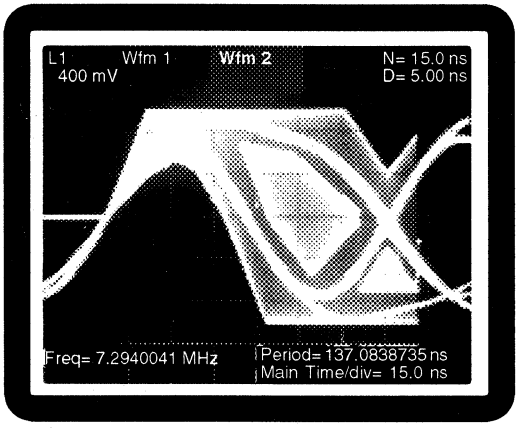


Figure 3B: Random Data after the Line Model (Waveform template and Jitter spec.)

TP Idle Pulse

Figures 4A and 4B show the TP Idle pulse. Figure 4A was measured at the TP outputs of the RJ45 connector. Figure 4B shows the pulse measured after the 10Base-T line model.

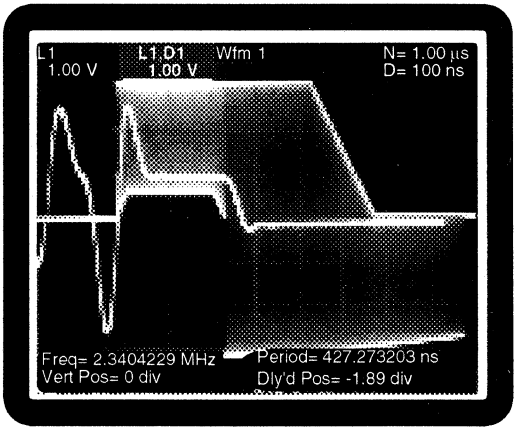


Figure 4A: TP Idle Pulse before Line Model with Test Load

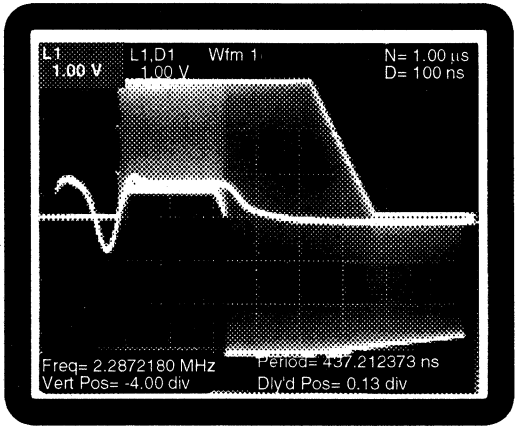


Figure 4B: TP Idle Pulse after Line Model with Test Load

Link Test Pulse

Figures 5A and 5B show the Link Test pulse. The top trace is the magnified waveform and the bottom trace is the original waveform. Figure 5A was obtained at the TP outputs of the RJ45 connector, and Figure 5B shows the pulse measured after the 10Base-T line model.

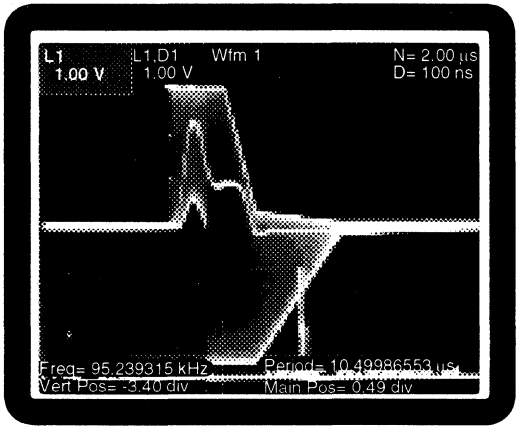


Figure 5A: Link Test Pulse before Line Model

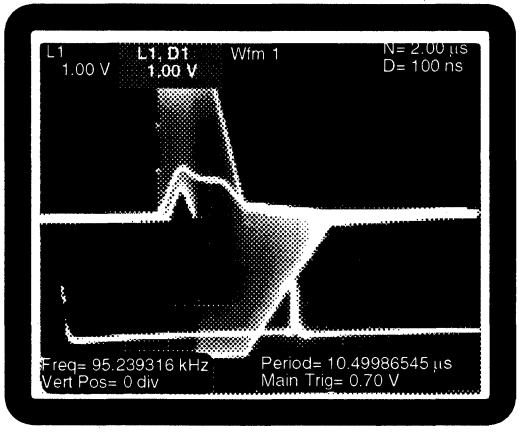


Figure 5B: Link Test Pulse after Line Model

Rise Time

Figures 6A and 6B show the DI signal waveform, measured at the AUI interface. The top trace is the DI waveform magnified for rise time measurement and the bottom trace is the DI signal without magnification. Figures 6A and 6B were obtained using transformer and capacitor coupling, respectively.

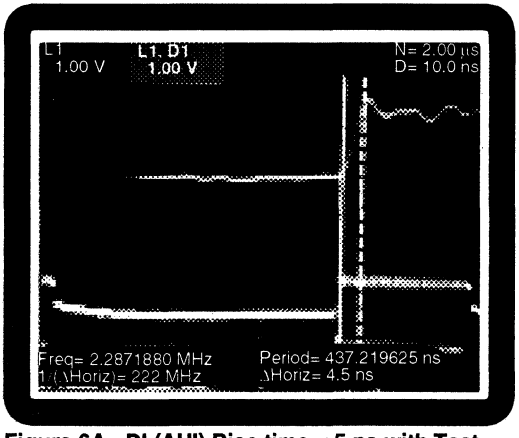


Figure 6A: DI (AUI) Rise time < 5 ns with Test Load (Transformer Coupling)

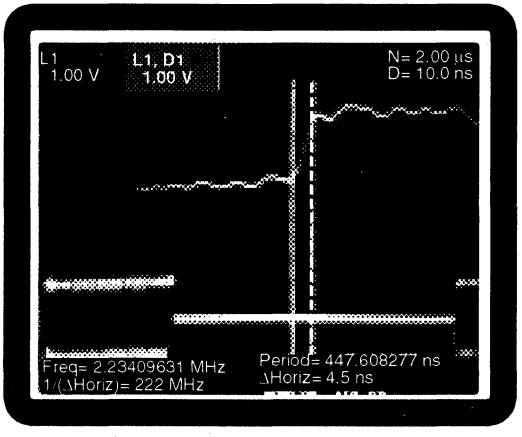


Figure 6B: DI (AUI) Rise time < 5 ns with Test Load (Capacitor Coupling)

End Of Frame

Figures 7A and 7B show the End Of Frame (EOF) pulse measured at the DI input to the LXT902. The top trace is the magnification of the end of frame and the bottom trace is the original waveform. Figure 7A was obtained using transformer coupling. Figure 7B was obtained with a capacitor coupling.

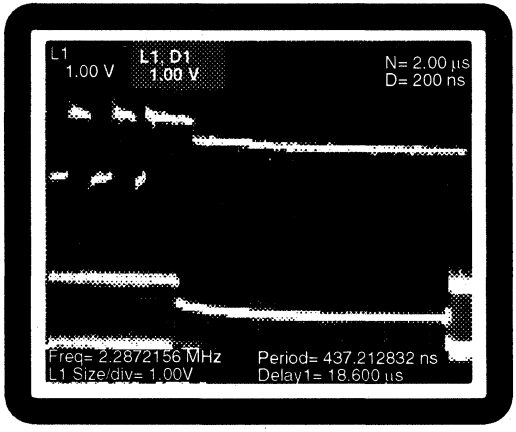


Figure 7A: DI (AUI) End of Frame with Test Load (Transformer Coupling)

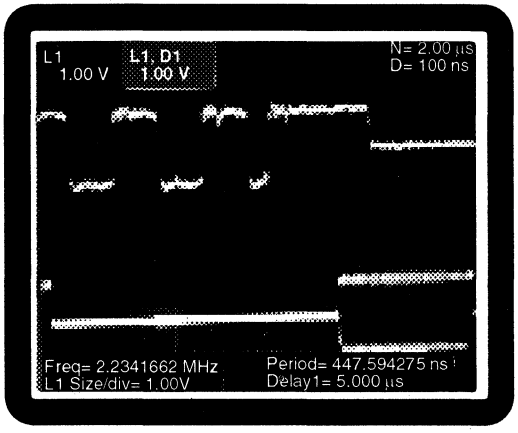
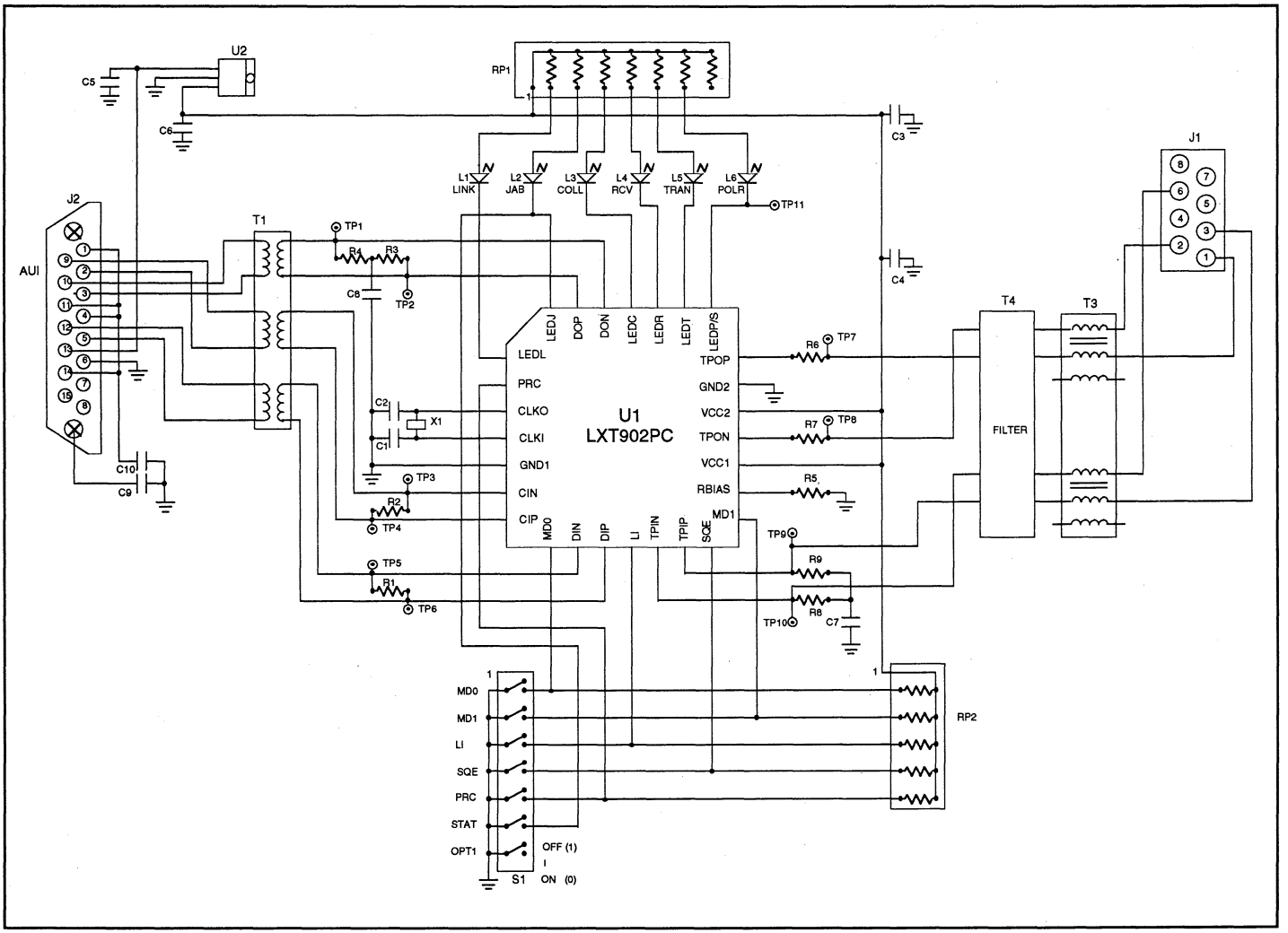


Figure 7B: DI (AUI) End of Frame with Test Load (Capacitor Coupling)

Demonstration Board Schematic

Figure 8 is a schematic diagram of the LDB902 Evaluation/ Demonstration Board.

Figure 8: LDB902 Schematic Diagram



NOTES:

LDB906 Demonstration Board for the LXT906 10Base-T to Coax Adapter

General Description

The LDB906 is an Ethernet twisted-pair to coax adapter board. It includes the LXT906 adapter chip, a DP8392 coax transceiver, and all required support components. An external power supply is packaged with the board.

The LDB906 provides LED status lights for link, jabber, reversed polarity, twisted-pair receive and collision, and coax receive and collision. Control jumpers are provided for link test disable and for 25 Ω termination on the coax side.

The LDB906 functions as a 2-port repeater connecting a 10Base T network segment to a 10Base2 or 10Base5 segment. It provides collision propagation and level translation.

Coax Interface

The board has a male BNC connector for the coax interface. The coax can be terminated with a 25 ohm resistor programmable with a jumper. This is useful when the LDB906 is used to connect an Ethernet adapter directly to a 10BaseT network segment. When the LDB906 is used to interface to a coax segment which is already terminated, this jumper should not be used.

An NSC DP8392 coax transceiver is mounted on the demo board, however, the LXT906 functions equally well with various other coax transceivers. Refer to the appropriate coax transceiver data sheet for correct implementation.

10BaseT Interface

An RJ45 jack and an integrated filter/transformer are provided for the twisted-pair interface. Suitable filters are supplied by FilMag, Valor, Pulse Engineering and Bell Fuse. The 10Base T Link test function is supported on the board, but disabled when Link jumper JP2 is inserted.

Power

12 VDC power is provided via a power jack connected to a wall transformer supplied with the board. Two voltage regulators, U1 (9V) and U2 (5V), supply chip-level power for the board.

Features

- Direct interface to Coax and Twisted-Pair network segments
- RJ45 connector for 10Base T interface
- Male BNC for Coax interface
- Collision detection and propagation
- Jumper-selectable link test
- Jumper-selectable 25 Ω termination for coax side
- 12 V wall transformer power supply
- On-board 5 V and 9 V voltage regulators
- Seven LEDs for the following indications:

Name		Color	When light is on :
JAB	(D2)	Red	Jabber is on
LINK	(D3)	Green	10BaseT link is up
PLR	(D4)	Red	10BaseT polarity reversed
TPRX	(D5)	Red	10BaseT receive active
TPCX	(D6)	Amber	10BaseT collision active
CXCX	(D7)	Amber	Coax collision active
CXRX	(D8)	Red	Coax receive active

LDB906 Parts List

Integrated Components

U1	AN7809, 9V voltage regulator
U2	AN7805, 5V voltage regulator
U3	DP8392, Coax transceiver
U4	PT3877, filter/transformer
U5	LXT906, TP - Coax Converter

Resistive Components

R1 - R4	1.5 k Ω
R5, R6	49.9 Ω, 1%
R7	1 k Ω, 1%
R8	24.9 Ω, 1%
R9	39.2 Ω, 1%
R10	12.4 k Ω, 1%
R11, R12	47.5 Ω, 1%
S1	7-resistor, 330 Ω network

Capacitive Components

C1-C6, C10, C11, C13, C16, C17	0.1 µF

Capacitive Components - continued

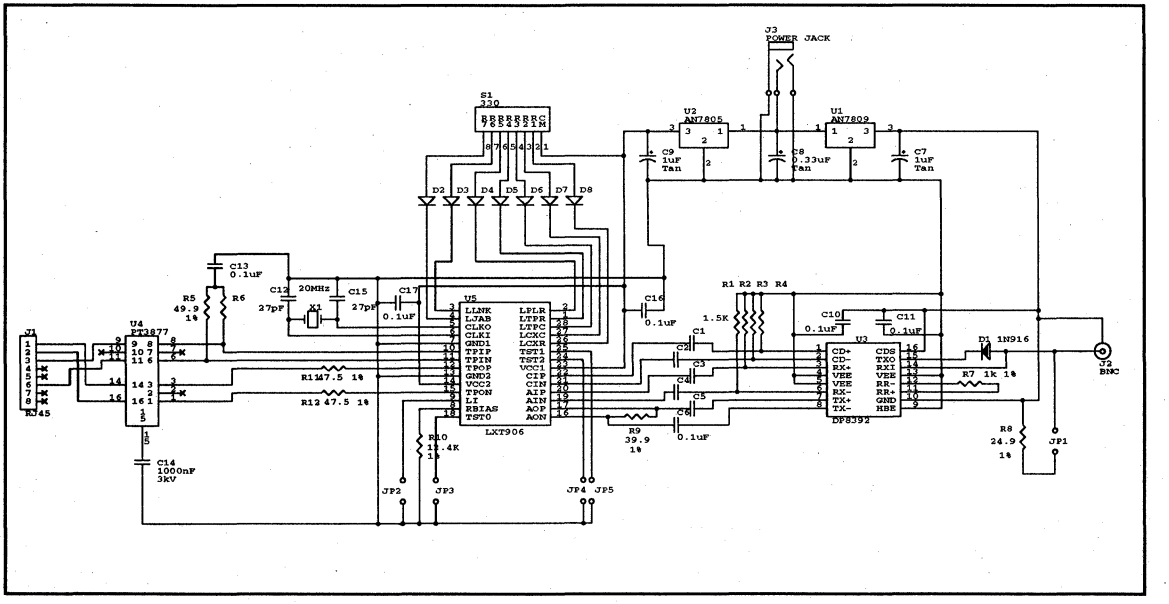
C7, C9	1 µF, tantalum
C8	0.33 µF, tantalum
C12, C15	27 pF
C14	1000 nF, 3 kV

Miscellaneous Components

D1	IN916
D2, D4, D5, D8	Miniature red LED
D3	Miniature green LED
D6, D7	Miniature amber LED
X1	20 MHz (± 1%) crystal[1]
J1	RJ45 jack
J2	male BNC connector
J3	power jack
JP1 - JP5	jumper
PS1	12 V power supply (wall transformer, not shown)

Note 1. Ceramic resonator can be used in place of crystal.

LDB906 Schematic Diagram



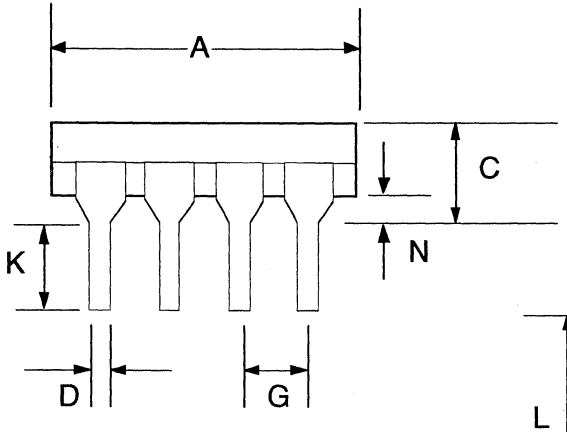
LEVEL ONE®

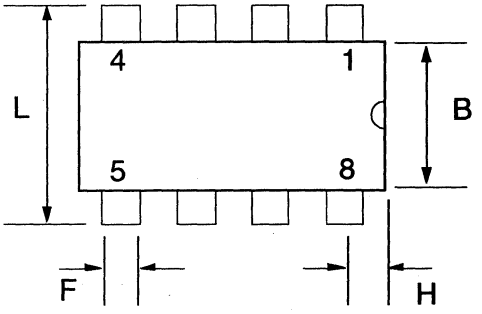
Package Specifications & Ordering Information

1994 Communications Data Book

LEVEL ONE®

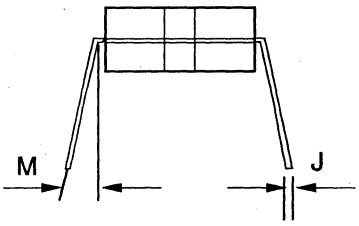
8 pin DIP



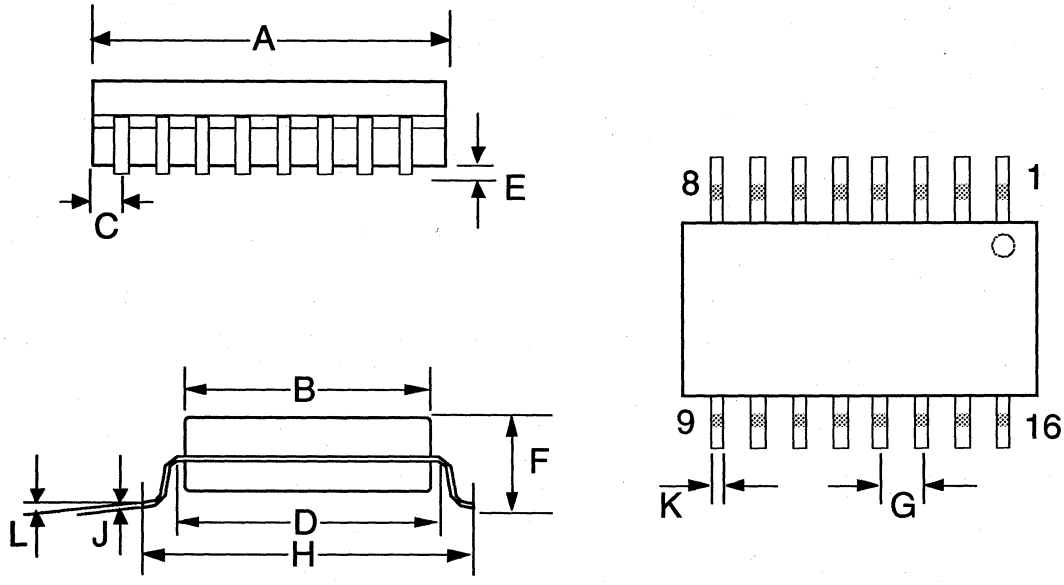


Dual In-Line Ceramic Case

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	.490	—	12.45
B	—	.300	—	7.62
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.200	3.18	5.08
L	.290	.325	7.37	8.26
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52



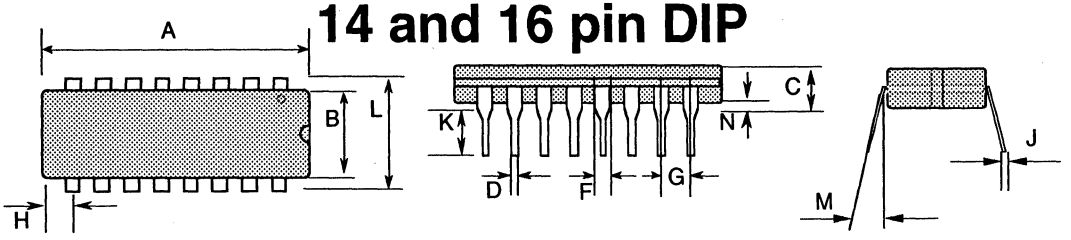
16 pin SOP



16-pin Plastic SOP

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	.396	.414	10.10	10.50
B	.291	.299	7.39	7.59
C	.023	.032	0.58	0.82
D	.325	.330	8.25	8.38
E	.004	.012	0.10	0.31
F	.093	.104	2.26	2.64
G	.050 BSC		1.27 BSC	
H	.394	.419	10.00	10.60
J	.009	.013	0.23	0.33
K	.014	.019	0.36	0.48
L	6° Typical			

14 and 16 pin DIP



14-pin Ceramic DIP

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	.790	—	20.10
B	—	.300	—	7.62
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.200	3.18	5.08
L	.290	.325	7.37	8.26
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52

14-pin Plastic DIP

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	.790	—	20.10
B	—	.300	—	7.62
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.150	3.18	5.08
L	.290	.325	7.37	8.26
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52

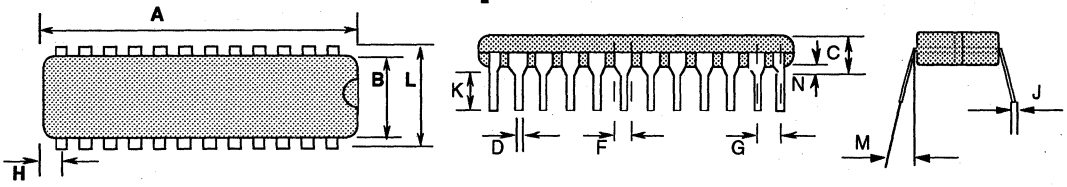
16-pin Ceramic DIP

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	.890	—	22.60
B	—	.300	—	7.62
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.200	3.18	5.08
L	.290	.325	7.37	8.26
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52

16-pin Plastic DIP

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	.890	—	22.60
B	—	.300	—	7.62
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.150	3.18	5.08
L	.290	.325	7.37	8.26
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52

24 pin DIP



Dual In-Line Ceramic Case - 600 mil

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	1.290	—	32.77
B	.500	.600	12.70	15.20
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.200	3.18	5.08
L	.590	.625	14.99	15.90
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52

Dual In-Line Plastic Case - 600 mil

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	1.290	—	32.77
B	.500	.600	12.70	15.20
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.150	3.18	3.81
L	.590	.625	14.99	15.90
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52

Dual In-Line Ceramic Case - 300 mil

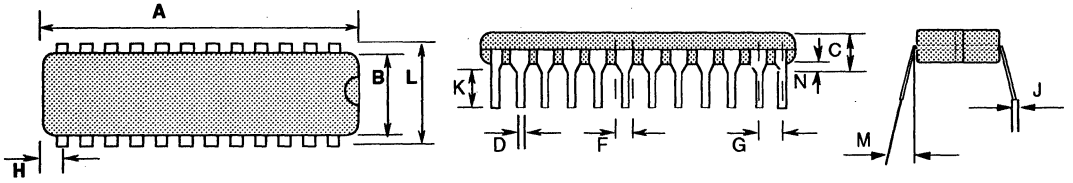
Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	1.290	—	32.77
B	—	.300	—	7.62
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.200	3.18	5.08
L	.290	.325	7.37	8.26
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52

Dual In-Line Plastic Case - 300 mil

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	1.290	—	32.77
B	—	.300	—	7.62
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.150	3.18	3.81
L	.290	.325	7.37	8.26
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52

LEVEL ONE®

28 and 40 pin DIP



28 pin Ceramic DIP

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	1.490	—	37.85
B	.500	.600	12.70	15.20
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.200	3.18	5.08
L	.590	.625	14.99	15.90
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52

28 pin Plastic DIP

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	1.490	—	37.85
B	.500	.600	12.70	15.20
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.150	3.18	3.81
L	.590	.625	14.99	15.90
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52

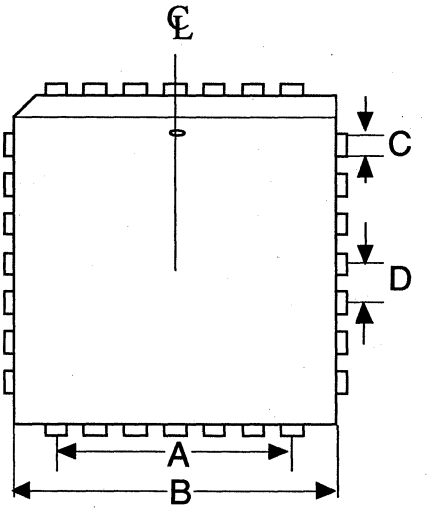
40 pin Ceramic DIP

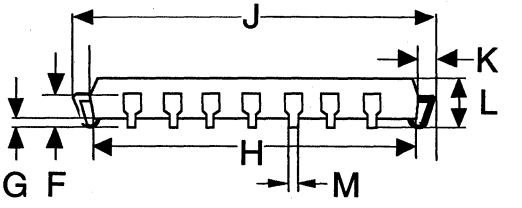
Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	2.090	—	53.09
B	.500	.600	12.70	15.20
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.200	3.18	5.08
L	.590	.625	14.99	15.90
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52

40 pin Plastic DIP

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	2.090	—	53.09
B	.500	.600	12.70	15.20
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.150	3.18	3.81
L	.590	.625	14.99	15.90
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52

28 and 44 pin PLCC





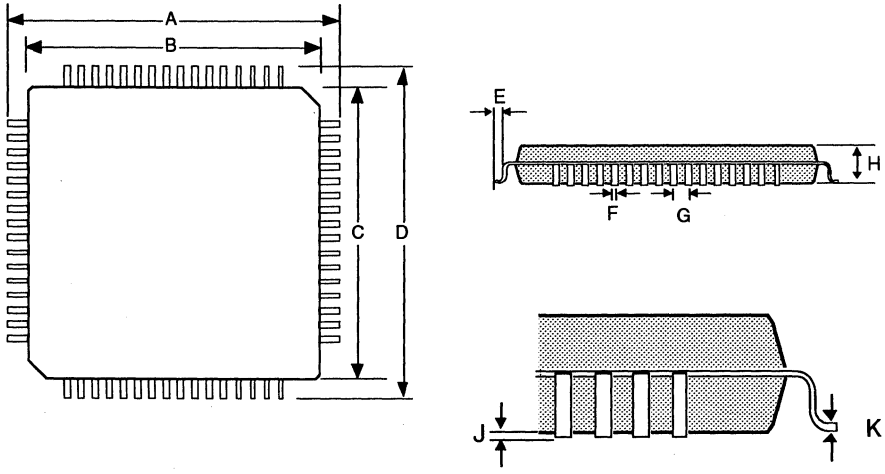
28-pin Plastic Leaded Chip Carrier

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	.290	.310	7.37	7.87
B	.450	.456	11.43	11.58
C	.026	.032	0.66	0.81
D	.050 BSC		1.27 BSC	
F	.090	.120	2.27	3.05
G	.020	—	0.51	—
H	.390	.430	9.91	10.92
J	.485	.495	12.32	12.57
K	.018	.022	0.46	0.56
L	.165	.180	4.20	4.57
M	.013	.021	0.33	0.53

44-pin Plastic Leaded Chip Carrier

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	.490	.510	12.45	12.95
B	.650	.656	16.51	16.66
C	.026	.032	0.66	0.81
D	.050 BSC		1.27 BSC	
F	.090	.120	2.27	3.05
G	.020	—	0.51	—
H	.590	.630	14.99	16.00
J	.685	.695	17.40	17.65
K	.018	.022	0.46	0.56
L	.165	.180	4.20	4.57
M	.013	.021	0.33	0.53

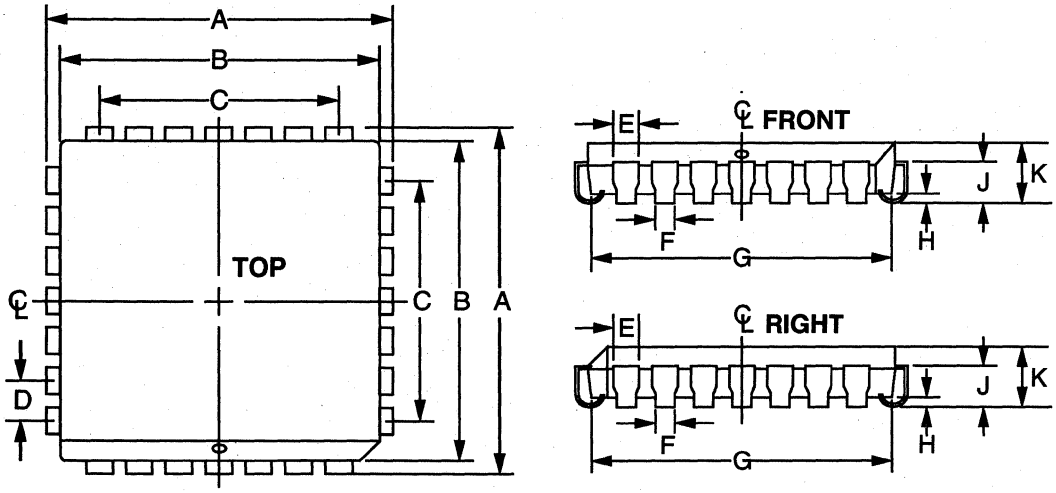
64 pin TQFP



64-pin Thin Quad Flat Pack

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	.461	.484	11.7	12.3
B	.390	.398	9.9	10.1
C	.390	.398	9.9	10.1
D	.461	.484	11.7	12.3
E	.012	.028	0.30	0.70
F	.006	.010	0.14	0.26
G	.016	.024	0.40	0.60
H	.051	.061	1.29	1.55
J	.002	.006	0.04	0.16
K	.004	.007	0.11	0.18

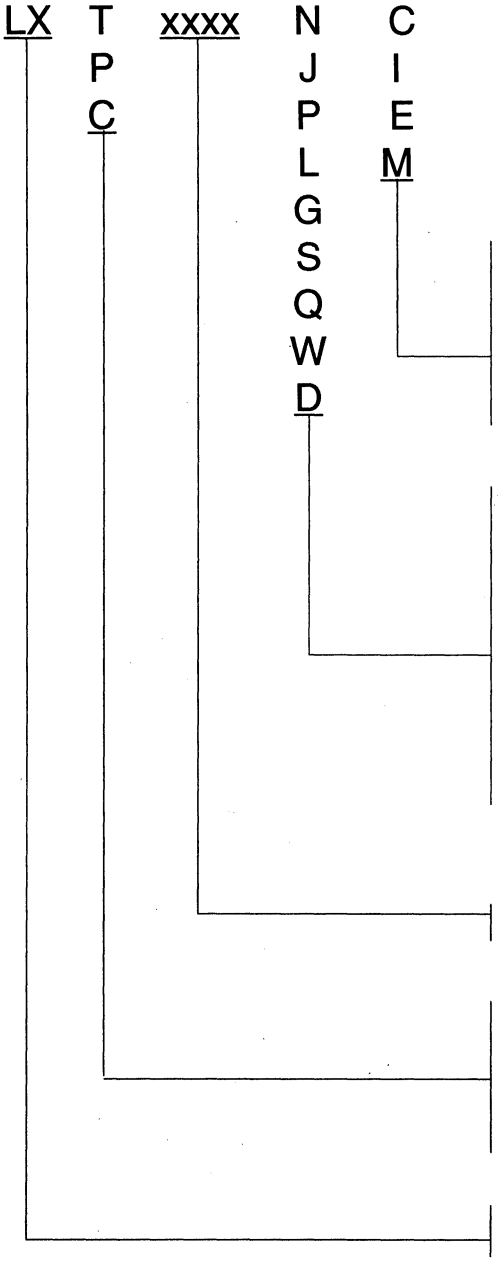
68 pin PLCC



68 pin Plastic Leaded Chip Carrier

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	.985	.995	25.02	25.27
B	.950	.958	24.13	24.33
C	.800 Nominal		20.32 Nominal	
D	.050 Basic		1.27 Basic	
E	.026	.032	.66	.81
F	.013	.021	.33	.53
G	.890	.930	22.61	23.62
H	.020	–	.51	–
J	.090	.130	2.29	3.30
K	.165	.200	4.20	5.08

Ordering Information



Temperature Range:

C = commercial range (0° to 70° C)
I = industrial range (-25°to +85° C)
E = extended range (-40°to +85° C)
M = military specifications (-55° to +125° C)

Package Type:

N = Plastic Dual In-line Package (DIP)
J = Ceramic DIP
P = Plastic Leaded Chip Carrier (PLCC)
T = Thin Quad Flat Pack (TQFP)
Q = Quad Flat Pack (QFP)
S = Plastic Small Outline Package (SOP)

Product ID: 3-5 alpha-numeric digits

Product type:

T = transceivers
P = peripherals
C = crystals

Level One Communications ID

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NOTES:

Sales Representatives and Distributors

1994 Communications Data Book

LEVEL ONE®

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Fax (205) 837-7049

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Fax: (214) 644-8161

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Fax: (408) 733-9970
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- Sales Representative
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1 Bis, Rue Marcel Paul
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91300 Massy, France
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92322 Chatillon Cedex, France
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- Sales Representatives
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30159 Hannover, Germany
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- Distributor
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