Cortina Systems® LXT901A and LXT907A PHY Transceivers

Datasheet: Long Form

The Cortina Systems® LXT901A and LXT907A PHY Transceivers (LXT901A/907A PHY) are new generation Universal Ethernet Transceivers with improved noise immunity and output filtering. The feature set of the LXT901A/907A PHY has been streamlined, removing Remote Signaling capabilities. The LXT901A/907A PHY provide all the active circuitry to interface most standard 802.3 controllers to either the 10BASE-T media or Attachment Unit Interface (AUI).

The LXT901A PHY and LXT907A PHY are identical except for the function of one pin. The LXT901A PHY, with selectable termination impedance allows the use of either shielded or unshielded twisted-pair cable. The LXT907A PHY offers a Signal Quality Error disable (DSQE) function.

LXT901A/907A PHY functions include Manchester encoding/decoding, receiver squelch and transmit pulse shaping, jabber, link testing and reversed polarity detection/correction.

Applications

- 10BASE-T hub and switching products
- Computer/workstation 10BASE-T LAN adapter boards

Features

Functional Features

- Integrated Filters - Simplify FCC Compliance
- Integrated Manchester Encoder/Decoder
- 10BASE-T Transceiver
- AUI Transceiver
- Full-Duplex Capable (20 Mbps)

Diagnostic Features

- Four LED Drivers
- AUI/RJ-45 Loopback

Convenience Features

- Automatic/Manual AUI/RJ-45 Selection
- Automatic Polarity Correction
- SQE Disable function (LXT907A PHY)
- Programmable Impedance Driver (LXT901A PHY)
- Single 3.3V operation
- Power Down Mode and four loopback modes
- Available in 64-pin LQFP and 44-pin PLCC packages
- Commercial (0 to +70°C)

Contents

Figures

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Revision History

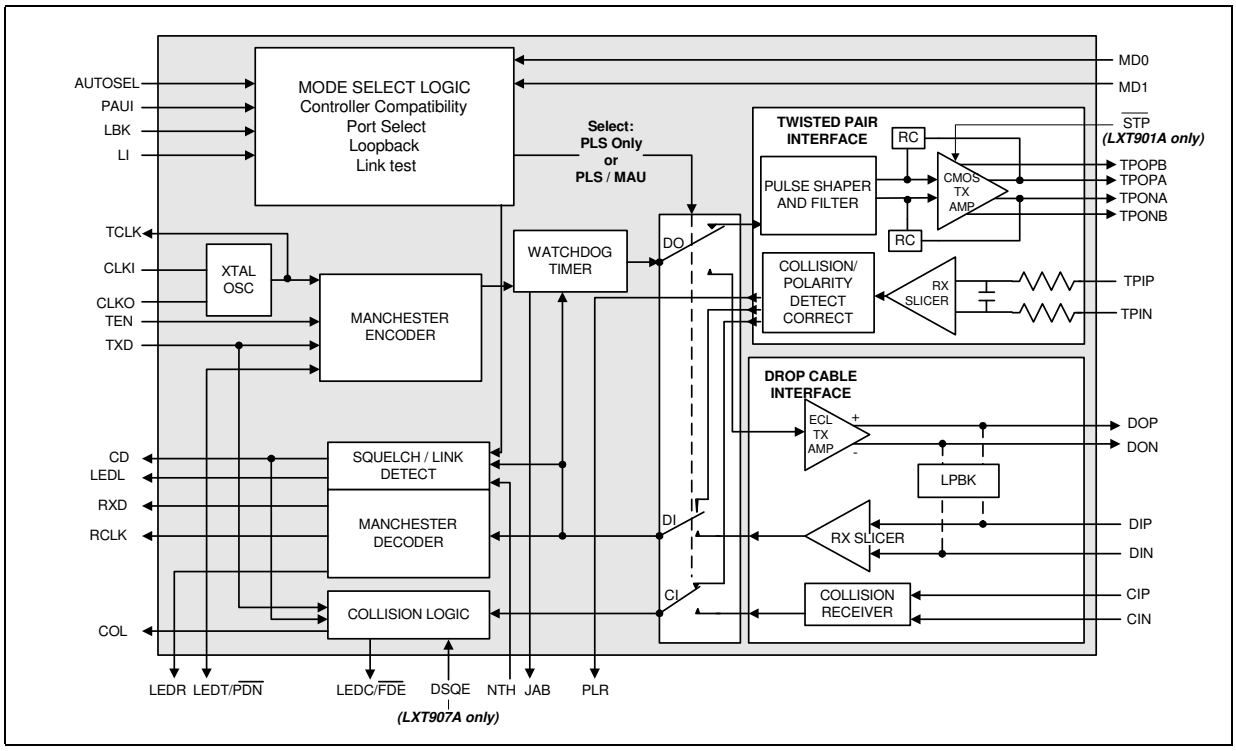
Revision 4.0 Revision Date: 03 December 2007
First release of this document from Cortina Systems, Inc.

Revision 003 Revision Date: 27 November 2005
• Updated Figure 2 “Intel® LXT901A and LXT907A Transceiver Pin Assignments” on page 8. • Added Section 5.1, “Top-Label Marking” on page 44. • Modified Table14 “Product Information” on page 47. • Modified Figure 51 “Ordering Information Matrix – Sample” on page 48.

Revision 002 Revision Date: 01 June 2001
• New items under “Applications”. • Figure 9: Added 0.1 µF label to capacitor at bottom of graphic. • Figure 10: Added 0.1 µF label to capacitor at bottom of graphic. • Figure 11Added 0.1 µF label to capacitor at bottom of graphic. • Figure 12: Added 0.1 µF label to capacitor at bottom of graphic. • Figure 13: Added 0.1 µF label to capacitor at bottom of graphic. • Added 2nd para under Test Specification regarding Quality and Reliability information. • Removed “Ambient operating temperature” from Absolute Maximum Values table. • Added Appendix: Product Ordering Information.

Revision 001 Revision Date: 01 January 2001
Initial release.

Figure 1 LXT901A/907A PHY Block Diagram



1.0 Pin Assignments and Signal Descriptions

Figure 2 LXT901A/907A PHY Pin Assignments

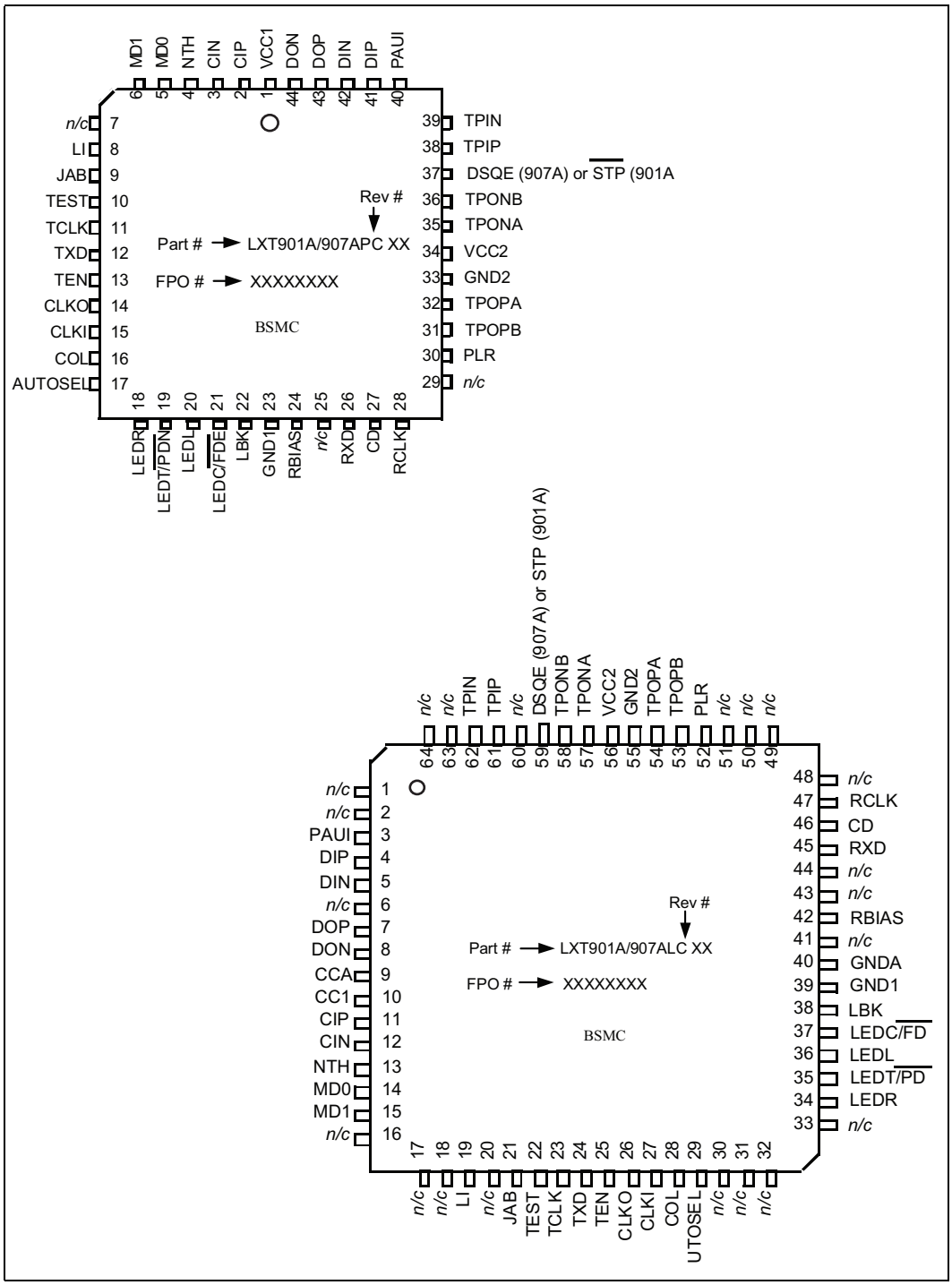


Table 1 LXT901A/907A PHY Signal Descriptions (Sheet 1 of 3)

Pin #		Symbol	I/O[1]	Description
PLCC	LQFP			
1 34	10 56	VCC1 VCC2	– –	**Power Supply 1 and 2.** Power supply inputs of +3.3 volts.
–	9	VCCA	–	**Analog Supply.** (+3.3 V)
2 3	11 12	CIP CIN	I I	**AUI Collision Pair.** Differential input to the AUI transceiver CI circuit. The input is collision signaling or SQE.
4	13	NTH	I	**Normal Threshold.** Selects normal or reduced threshold. When NTH is High, the normal TP squelch threshold is in effect. When NTH is Low, the normal TP squelch threshold is reduced by 4.5 dB.
5 6	14 15	MD0 MD1	I I	**Mode Select 0 (MD0) and Mode Select 1 (MD1).** Mode select pins determine the controller compatibility mode in accordance with Table 2.
8	19	LI	I	**Link Test Enable.** Controls Link Integrity Test; enabled when LI = High, disabled when LI = Low
9	21	JAB	O	**Jabber Indicator.** Output goes High to indicate Jabber state.
10	22	TEST	I	**Test.** For Cortina internal use only. It is recommended to tie this pin High externally.
11	23	TCLK	O	**Transmit Clock.** A 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller.
12	24	TXD	I	**Transmit Data.** Input signal containing NRZ data to be transmitted on the network. Connect TXD directly to the transmit data output of the controller.
13	25	TEN	I	**Transmit Enable.** Enables data transmission and starts the watchdog timer. Synchronous to TCLK (see Test Specifications for details).
14 15	26 27	CLKO CLKI	O I	**Crystal Oscillator.** A 20 MHz crystal must be connected across these pins, or a 20 MHz clock applied at CLKI with CLKO left open.
16	28	COL	O	**Collision Detect.** Output which drives the collision detect input of the controller.
17	29	AUTOSEL	I	**Automatic Port Select.** When High, automatic port selection is enabled (the LXT901A/907A PHY defaults to the AUI port only if TP link integrity = Fail). When Low, manual port selection is enabled (the PAUI pin determines the active port).
18	34	LEDR	OD	**Receive LED.** Open drain driver for the receive indicator LED. Output is pulled Low during receive.
19	35	LEDT/ $\overline{\text{PDN}}$	OD	**Transmit LED (LEDT)/Power Down ($\overline{\text{PDN}}$).** Open drain driver for the transmit indicator. Output is pulled Low during transmit. **Do not allow this pin to float. If unused, tie High.** If externally pulled Low, the LXT901A/907A PHY goes to power down state.
20	36	LEDL	OD	**Link LED.** Open drain driver for link integrity indicator. Output is pulled Low during link test pass. If externally tied Low, internal circuitry is forced to “Link Pass” state and the LXT901A/907A PHY will transmit link test pulses continuously.

1. I/O Column Coding: I = Input, O = Output, OD = Open Drain

Table 1 LXT901A/907A PHY Signal Descriptions (Sheet 2 of 3)

Pin #		Symbol	I/O[1]	Description
PLCC	LQFP			
21	37	LEDC/ $\overline{\text{FDE}}$	OD	**Collision LED (LEDC)/Full-Duplex Enable ($\overline{\text{FDE}}$).** Open drain driver for the collision indicator pulls Low during collision. LED "On" (i.e., Low output) time is extended by approximately 100 ms. If externally tied Low, enables full-duplex operation by disabling the internal TP loopback and collision detection circuits in anticipation of external TP loopback or full-duplex operation. If this pin is not used, tie high or directly to Vcc.
22	38	LBK	I	**Loopback.** Enables internal loopback mode. Refer to Functional Description for details.
23 33	39 55	GND1 GND2	– –	**Ground Returns 1 and 2.** Grounds
–	40	GNDA	–	**Analog Ground.**
24	42	RBIAS	I	**Bias Control.** A 12.4 kΩ 1% resistor to ground at this pin controls operating circuit bias.
26	45	RXD	O	**Receive Data.** Output signal. Connect directly to the receive data input of the controller.
27	46	CD	O	**Carrier Detect.** An output to notify the controller of activity on the network.
28	47	RCLK	O	**Receive Clock.** A recovered 10 MHz clock which is synchronous to the received data. Connect to the controller receive clock input.
30	52	PLR	O	**Polarity Reverse.** Output goes High to indicate reversed polarity at the TP input.
31 36 32 35	53 58 54 57	TPOPB TPONB TPOPA TPONA	O O O O	**Twisted-Pair Transmit Pairs A & B.** Two differential driver pair outputs (A and B) to the twisted-pair cable. The outputs are pre-equalized. Each pair must be shorted together and tied to the transformer through a 24.9 Ω 1% series resistor to match impedance of 100 Ω. Refer to Figure 16 in the Applications Section for information on 150Ω configurations.
37	59	$\overline{\text{STP}}$	I	**$\overline{\text{STP}}$ Select (**LXT901A PHY **only).** When $\overline{\text{STP}}$ is Low, 150 Ω termination for shielded TP is selected. When $\overline{\text{STP}}$ is High, 100 Ω termination for unshielded TP is selected. LXT907A PHY is designed for 100Ω UTP termination (not selectable).
		DSQE	I	**Disable SQE (**LXT907A PHY **only).** When DSQE is High, the SQE function is disabled. When DSQE is Low, the SQE function is enabled. SQE must be disabled for normal operation in Hub/Switch applications. LXT901A PHY operates with SQE enabled (not selectable).
38 39	61 62	TPIP TPIN	I I	**Twisted-Pair Receive Pair.** A differential input pair from the TP cable. Receive filter is integrated on-chip. No external filters are required.
40	3	PAUI	I	**Port/AUI Select.** In Manual Port Select mode (AUTOSEL Low), PAUI selects the active port. When PAUI is High, the AUI port is selected. When PAUI is Low, the TP port is selected. In Auto Port Select mode, PAUI must be tied to ground.

1. I/O Column Coding: I = Input, O = Output, OD = Open Drain

Table 1 LXT901A/907A PHY Signal Descriptions (Sheet 3 of 3)

Pin #		Symbol	I/O[1]	Description
PLCC	LQFP			
41 42	4 5	DIP DIN	I I	**AUI Receive Pair.** Differential input pair from the AUI transceiver DI circuit. The input is Manchester encoded.
43 44	7 8	DOP DON	O O	**AUI Transmit Pair.** A differential output driver pair for the AUI transceiver cable. The output is Manchester encoded.
7, 25, 29	1, 2, 6, 16, 17, 18, 20, 30, 31, 32, 33, 41, 43, 44, 48, 49, 50, 51, 60, 63, 64	N/C	–	**No Connect** (Internally tied to ground).

1. I/O Column Coding: I = Input, O = Output, OD = Open Drain

2.0 Functional Description

The LXT901A/907A PHY performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. They function as a PLS-Only device (for use with 10BASE-2 or 10BASE-5 coaxial cable networks) or as an Integrated PLS/MAU (for use with 10BASE-T twisted-pair networks). In addition to standard 10 Mbps operation, they also support full-duplex 20 Mbps operation.

The LXT901A/907A PHY interfaces a back-end controller to either an AUI drop cable or a twisted-pair (TP) cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The AUI interface comprises three circuits: Data Output (DO), Data Input (DI) and Collision (CI). The twisted-pair interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to the three basic interfaces, the LXT901A/907A PHY contains an internal crystal oscillator and four LED drivers for visual status reporting.

Functions are defined from the back-end controller side of the interface. The Transmit function refers to data transmitted by the back-end to the AUI cable (PLS-Only mode) or to the twisted-pair network (Integrated PLS/MAU mode). The Receive function refers to data received by the back-end from the AUI cable (PLS-Only) or from the twisted-pair network (Integrated PLS/MAU mode). In the integrated PLS/MAU mode, the LXT901A/907A PHY performs all required MAU functions defined by the IEEE 802.3 10BASE–T specification such as collision detection, link integrity testing, signal quality error messaging, jabber control and loopback. In the PLS-Only mode, the LXT901A/907A PHY receives incoming signals from the AUI DI circuit with ± 18 ns of jitter and drives the AUI DO circuit.

2.1 Controller Compatibility Modes

The LXT901A/907A PHY are compatible with most industry standard controllers including devices produced by Motorola*, AMD*, Intel*, Fujitsu*, National Semiconductor*, Seeq* and Texas Instruments*. Four different control signal timing and polarity schemes (Modes 1 through 4) are required to achieve this compatibility. Mode select pins (MD0 and MD1) determine Controller compatibility modes as listed in Table 2. Refer to Test Specifications for a complete set of timing diagrams for each mode.

Table 2 Controller Compatibility Modes

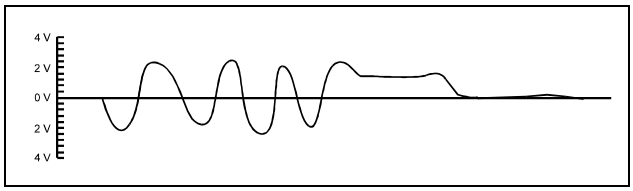
Controller Mode	Setting	
	MD1	MD0
Mode 1 For Motorola* 68EN360, MPC860, Advanced Micro Devices* AM7990 or compatible controllers	Low	Low
Mode 2 For Intel* 82596 or compatible controllers[1]	Low	High
Mode 3 For Fujitsu* MB86950, MB86960 or compatible controllers (Seeq* 8005)[2]	High	Low
Mode 4 For National Semiconductor* 8390 or compatible controllers (TI TMS380C26)	High	High

1. Refer to Intel* Application Note 51 when designing with Intel* Controllers.
2. SEEQ controllers require inverters on CLK1, LBK, RCLK and COL.

2.2 Transmit Function

The LXT901A/907A PHY receives NRZ data from the controller at the TXD input, as shown in the block diagram on the first page of this Data Sheet, and passes it through a Manchester encoder. The encoded data is then transferred to either the AUI cable (the DO circuit) or the twisted-pair network (the TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP as shown in Figure 3. The TPO output is pre-distorted and prefiltered to meet the 10BASE-T jitter template. An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance. During idle periods, the LXT901A/907A PHY transmits link integrity test pulses on the TPO circuit (if LI is enabled and integrated PLS/ MAU mode is selected). External resistors control the termination impedance for the LXT907A PHY. External resistors and the STP Pin control termination impedance on the LXT901A PHY.

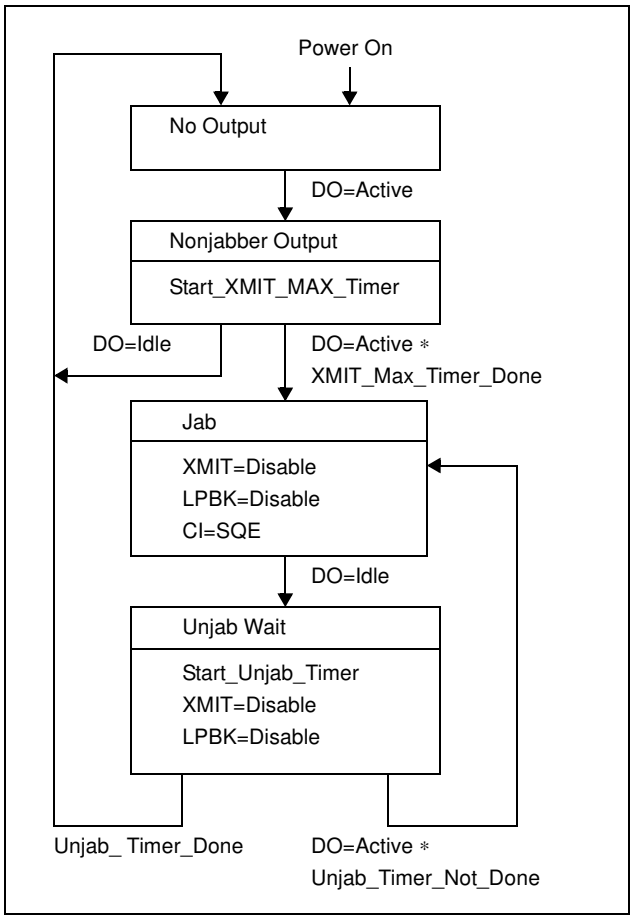
Figure 3 TPO Output Waveform



2.2.1 Jabber Control Function

Figure 4 is a state diagram of the LXT901A/907A PHY Jabber control function. The on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions, and activates the JAB pin. Once the LXT901A/907A PHY is in the jabber state, the TXD circuit must remain idle for a period of 250 to 750 ms before it will exit the jabber state.

Figure 4 Jabber Control Function



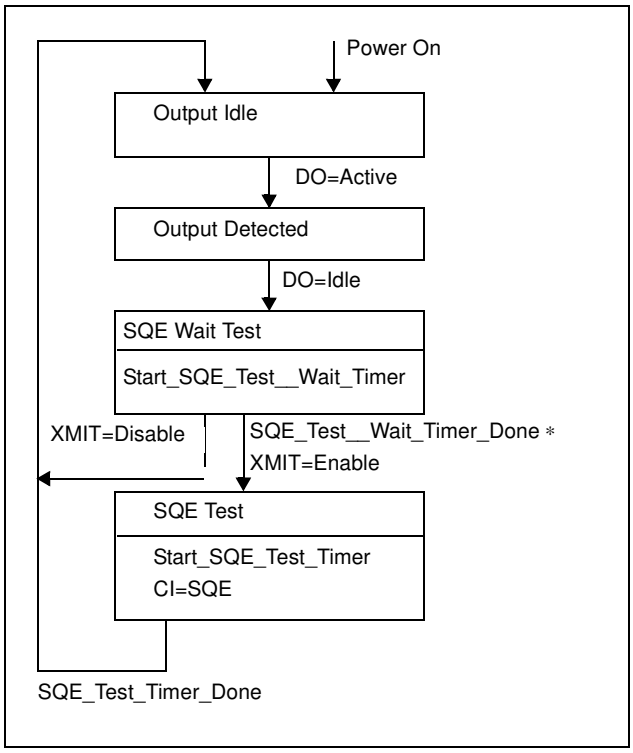
2.2.2 SQE Function

In the integrated PLS/MAU mode, the LXT901A/907A PHY supports the signal quality error (SQE) function as shown in Figure 5, although the SQE function can be disabled on the LXT907A PHY. After every successful transmission on the 10BASE-T network, when SQE is enabled, the LXT901A/907A PHY transmits the SQE signal for 10BT ± 5BT over the internal CI circuit which is indicated on the COL pin of the device. When using the AUI of the LXT901A/907A PHY, the SQE function is determined by the external MAU attached.

2.2.2.1 SQE Disable Function (LXT907A PHY only)

SQE must be disabled for normal operation in hub and switch applications. The LXT907A PHY is configured with an SQE Disable function. The SQE function is disabled when DSQE is set High, and enabled when DSQE is Low.

Figure 5 SQE Function



2.3 Receive Function

The LXT901A/907A PHY receive function acquires timing and data from the twisted-pair network (the TPI circuit) or from the AUI (the DI circuit). Valid received signals are passed through the on-chip filters and Manchester decoder, then output as decoded NRZ data and receive timing on the RXD and RCLK pins, respectively.

An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level and with proper timing. If the differential signal at the TPI or the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT901A/907A PHY receive function enters the idle state. If the polarity of the TPI circuit is reversed, LXT901A/907A PHY detects the polarity reverse and reports it via the PLR output. The LXT901A/907A PHY automatically corrects reversed polarity.

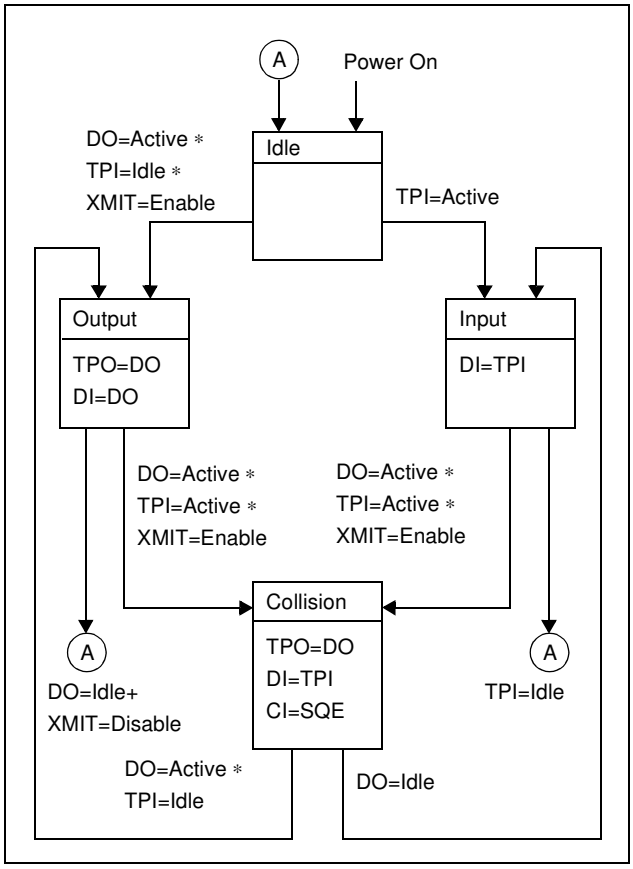
2.3.1 Polarity Reverse Function

The LXT901A/907A PHY polarity reverse function uses both link pulses and end-of-frame data to determine the polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever a correct polarity frame or a correct link pulse is received, these two counters are reset to zero. If the LXT901A/907A PHY enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. If Link Integrity Testing is disabled, polarity detection is based only on received data. Polarity correction is always enabled.

2.3.2 Collision Detection Function

The collision detection function operates on the twisted- pair side of the interface. For standard (half-duplex) 10BASE-T operation, a collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT901A/907A PHY reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 6 is a state diagram of the LXT901A/907A PHY collision detection function. Refer to Test Specifications for collision detection and COL/CI output timing. (NOTE: For full-duplex operation on the TP or AUI port, the collision detection circuitry must be disabled by setting $\overline{\text{FDE}}$ Low.)

Figure 6 Collision Detection Function



2.4 Loopback Functions

2.4.1 Standard TP Loopback

The LXT901A/907A PHY provides the standard loopback function defined by the 10BASE-T specification for the twisted-pair port. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the LXT901A/907A PHY from the TXD pin through the Manchester encoder/decoder to the RXD pin and returned to the back-end. This standard loopback function is disabled when a data collision occurs, clearing the RXD circuit for the TPI data. Standard loopback is also disabled during link fail and jabber states. The LXT901A/907A PHY also provides three additional loopback functions.

2.4.2 Forced TP Loopback

“Forced” TP loopback is controlled by the LBK pin. When the TP port is selected and LBK is High, TP loopback is “forced”, overriding collisions on the TP circuit. When LBK is Low, normal loopback is in effect.

2.4.3 AUI Loopback

AUI loopback is also controlled by the LBK pin. When the AUI port is selected and LBK is High, data transmitted by the back-end is internally looped back from the TXD pin through the Manchester encoder/decoder to the RXD pin. When LBK is Low, no AUI loopback occurs.

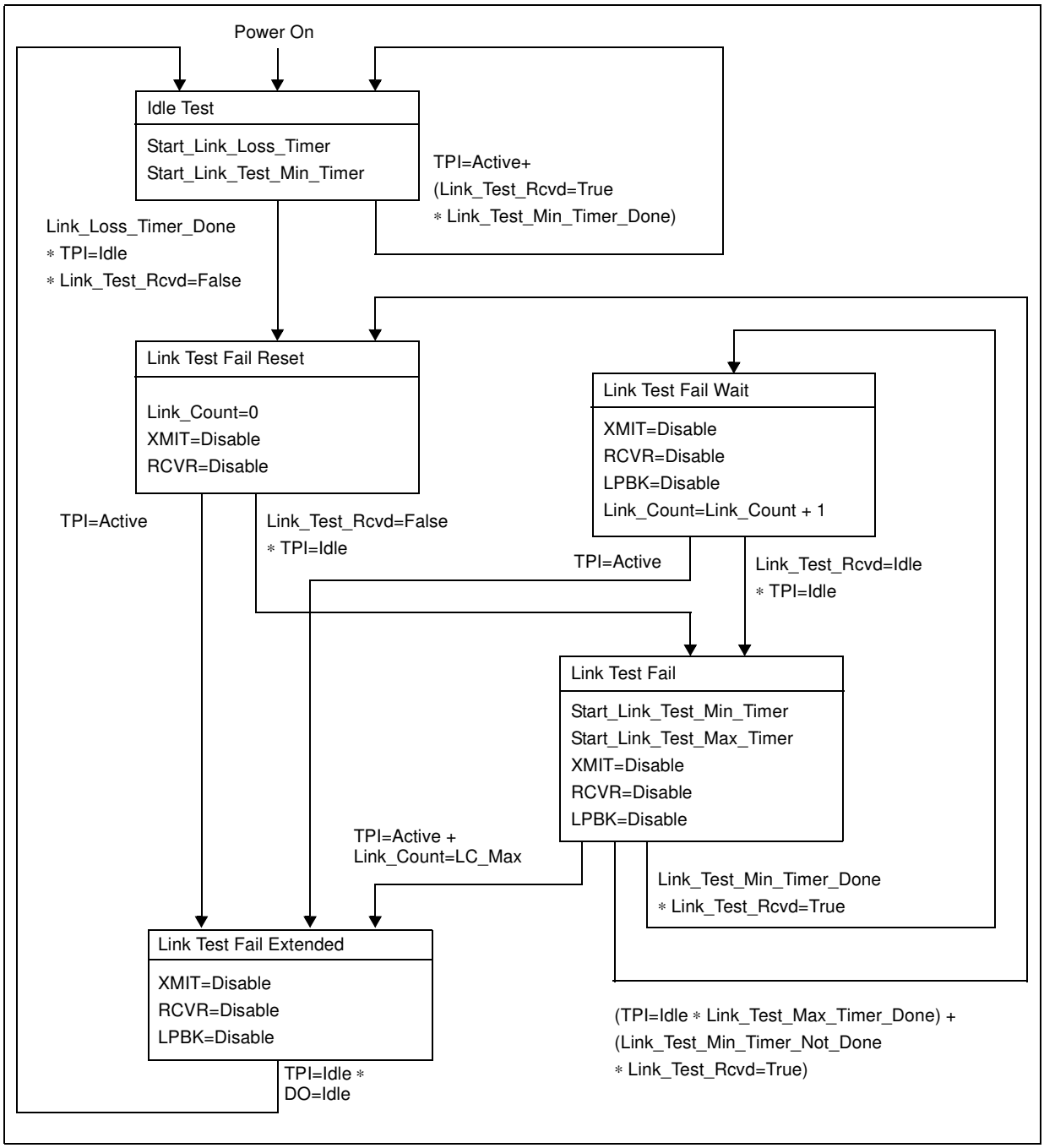
2.4.4 External Loopback

An external loopback mode, useful for system-level testing, is controlled by the LEDC/$\overline{\text{FDE}}$ pin. When LEDC/$\overline{\text{FDE}}$ is tied Low, the LXT901A/907A PHY disables the collision detection and internal loopback circuits, to allow external loopback. External loopback mode can be set on either TP or AUI ports.

2.5 Link Integrity Test Function

Figure 7 is a state diagram of the LXT901A/907A PHY Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled when the LI pin is tied High. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The LXT901A/907A PHY ignores any link integrity pulse with interval less than 2 - 7 ms. The LXT901A/907A PHY will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

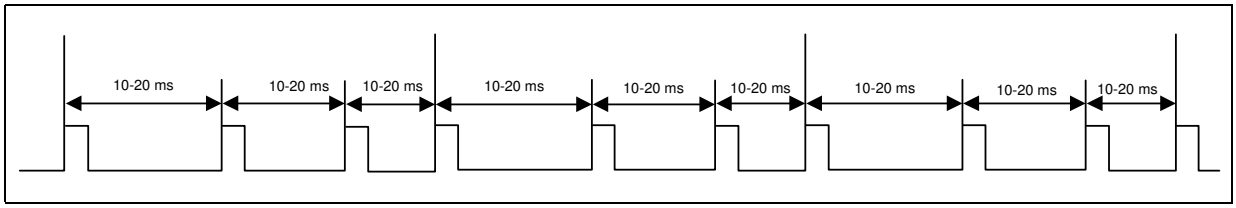
Figure 7 Link Integrity Test Function



2.6 Link Pulse Transmission

When not transmitting data, the LXT901A/907A PHY transmits 802.3-compliant standard link pulses. Figure 8 shows the link integrity pulse timing.

Figure 8 Transmitted Link Integrity Pulse Timing



3.0 Application Information

3.1 Twisted-Pair Impedance Matching

Resistors must be installed on each input and output pair to match impedance of the network media being used. The LXT907A PHY is configured with 100 Ω termination for Unshielded Twisted-Pair (UTP). In this case, the positive and negative sides of both output pairs are shorted together (TPOPA/TPOPB and TPONA/TPONB) and tied to the transformer through a 24.9 Ω 1% series resistor.

The LXT901A PHY is designed with an $\overline{\text{STP}}$ Select pin that allows the device to match both 100 Ω and 150 Ω media. A dual resistor combination can be configured to accommodate either line termination as shown in Figure 16. When 100 Ω termination is selected, both A and B pairs are driven in parallel. When 150 Ω termination is selected, the B pair is tri-stated and only the A pair is driven.

3.2 Crystal Information

Designers should test and validate crystals before committing to a specific component. Based on limited evaluation, Table 3 lists some suitable crystals.

Table 3 Suitable Crystals

Manufacturer	Part Number
MTRON*	MP-1
	MP-2

3.3 Magnetics Information

The LXT901A PHY and LXT907A PHY require a 1:1 ratio for the receive transformer and a 1:$\sqrt{2}$ ratio for the transmit transformer on the twisted-pair interface. The AUI Interface requires a 1:1 ratio for the data-in, data-out, and collision-pair transformers. Designers must test and validate all components for suitability in their applications.

3.4 Typical Applications

Figure 9 through Figure 16 show typical LXT901A/907A PHY applications.

3.4.1 Auto Port Select with External Loopback Control

Figure 9 is a typical LXT901A/907A PHY application. The diagram is arranged to group similar pins together; it does not represent the actual LXT901A/907A PHY pinout. The controller interface pins (transmit data, clock and enable; receive data and clock; and the collision detect, carrier detect and loopback control pins) are shown at the top left.

Programmable option pins are grouped center left. The PAUI pin is tied Low and all other option pins are tied High. This setup selects the following options:

- Automatic Port Selection
  (PAUI Low and AUTOSEL High)
- Normal Receive Threshold (NTH High)
- Mode 4, compatible with National NS8390 controllers (MD0 High, MD1 High)

- SQE Disabled (DSQE High for LXT907A PHY only)
- UTP is selected ($\overline{\text{STP}}$ High for LXT901A PHY only)
- Link Testing Enabled (LI High)

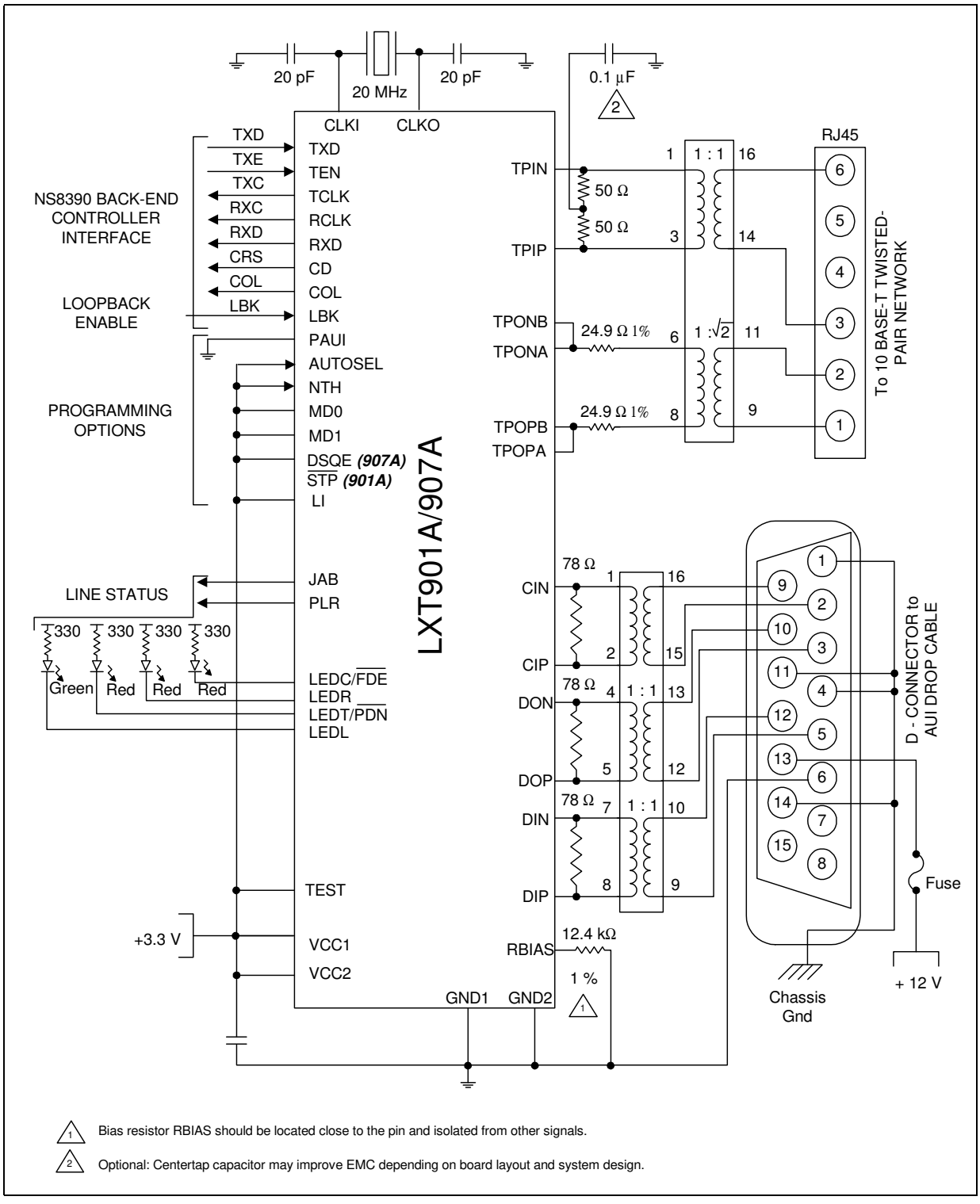
Status outputs are grouped at lower left. Local status outputs drive LED indicators.

Power and ground pins are shown at the bottom of the diagram. A single power supply is used for both VCC1 and VCC2 with a decoupling capacitor installed between the power and ground busses.

An additional power and ground pin (VCCA and GNDA) is supported in designs using the 64-pin LQFP package. A single power supply is used for all three power and ground pins (VCC1, VCC2, VCCA) and (GND1, GND2, GNDA). Install a decoupling capacitor between each power and ground buss.

The TP and AUI interfaces are shown at upper and lower right, respectively. Impedance matching resistors for 100Ω UTP are installed in each I/O pair and no external filters are required.

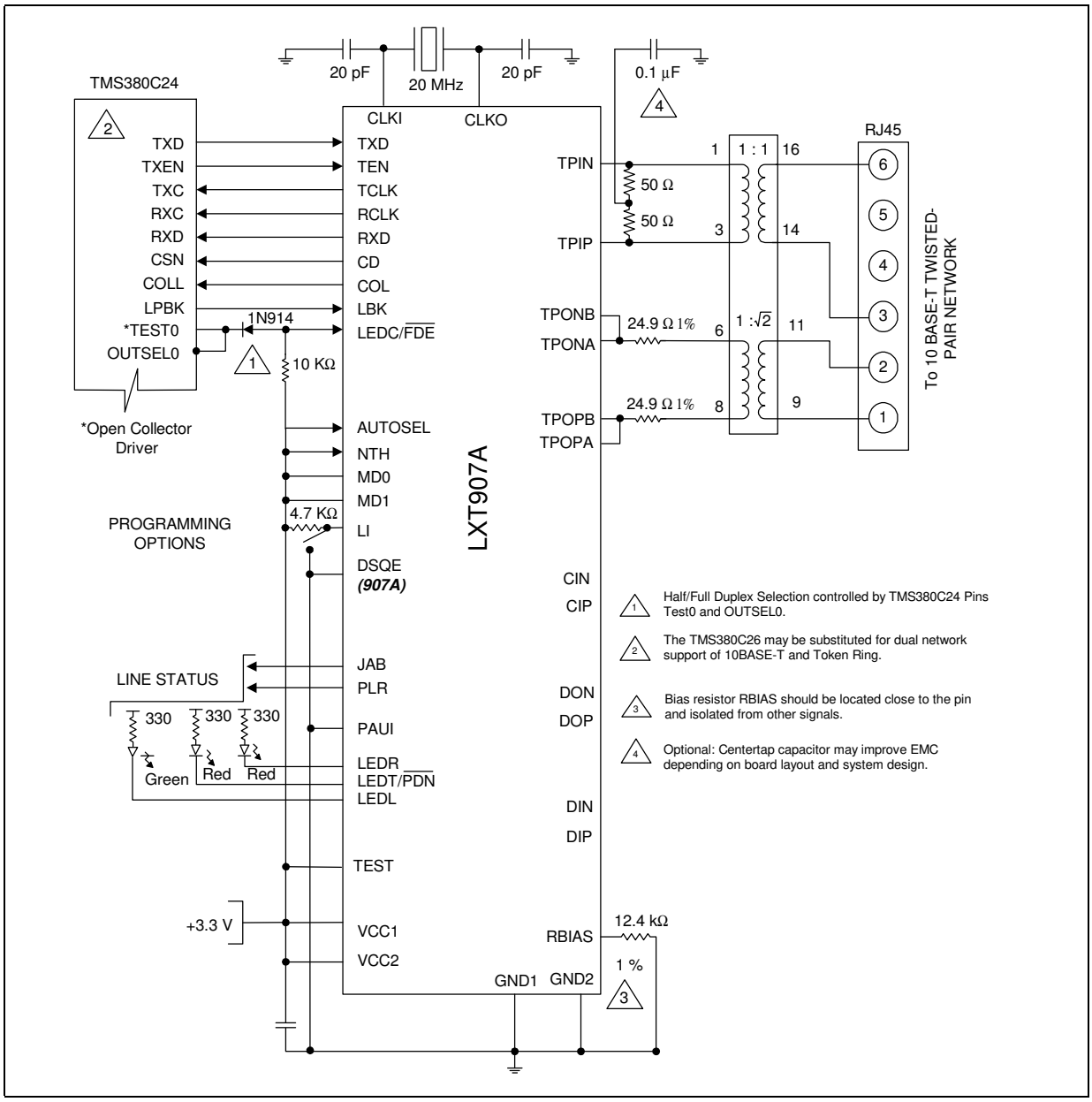
Figure 9 LAN Adapter Board - Auto Port Select with External LPBK Control



3.4.2 Full-Duplex Support

Figure 10 shows the LXT907A PHY with a Texas Instruments* 380C24 CommProcessor. The 380C24 is compatible with Mode 4 (MD0 and MD1 both High). When used with the 380C24, or other full-duplex capable controller, the LXT907A PHY supports full-duplex Ethernet, effectively doubling the available bandwidth of the network. In this application the SQE function is enabled (DSQE tied Low), and the AUI port is not used.

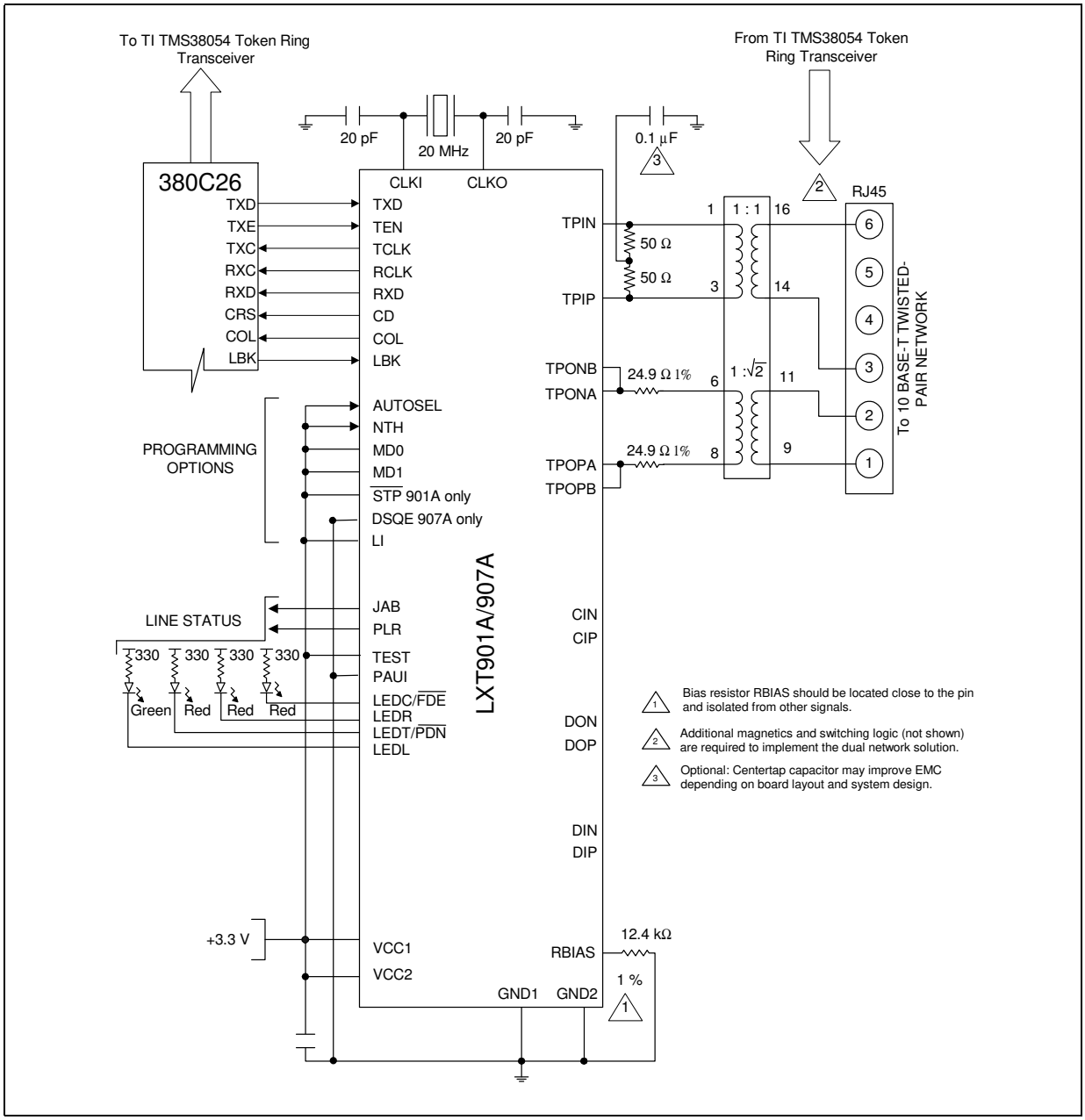
Figure 10 Full-Duplex Operation



3.4.3 Dual Network Support - 10Base-T and Token Ring

Figure 11 shows the LXT901A/907A PHY with a Texas Instruments* 380C26 CommProcessor. The 380C26 is compatible with Mode 4 (MD0 and MD1 both High). When used with the 380C26, both the LXT901A/907A PHY and a TMS38054 Token Ring transceiver can be tied to a single RJ-45 allowing dual network support from a single connector. The LXT901A/907A PHY AUI port is not used. The DSQE pin on the LXT907A PHY is tied Low and the STP pin on the LXT901A PHY is tied High.

Figure 11 380C26 Interface for Dual Network Support of 10BASE-T and Token Ring



3.4.4 Manual Port Select with Link Test Function

With MD0 tied Low and MD1 tied High, the LXT901A/907A PHY logic and framing are set to Mode 3 (compatible with Fujitsu* MB86950 and MB86960, and Seeq* 8005 controllers). Figure 12 shows the setup for Fujitsu* controllers. Figure 13 shows the four inverters required to interface with the Seeq* 8005 controller. As in Figure 9 on page 18 both these Mode 3 applications show the LI pin tied High, enabling Link Testing; and the STP (LXT901A PHY only) and NTH pins are both tied High, selecting the standard receiver threshold and 100Ω termination for unshielded TP cable. However, in these applications AUTOSEL is tied Low, allowing external port selection through the PAUI pin.

Figure 12 LAN Adapter Board - Manual Port Select with Link Test Function

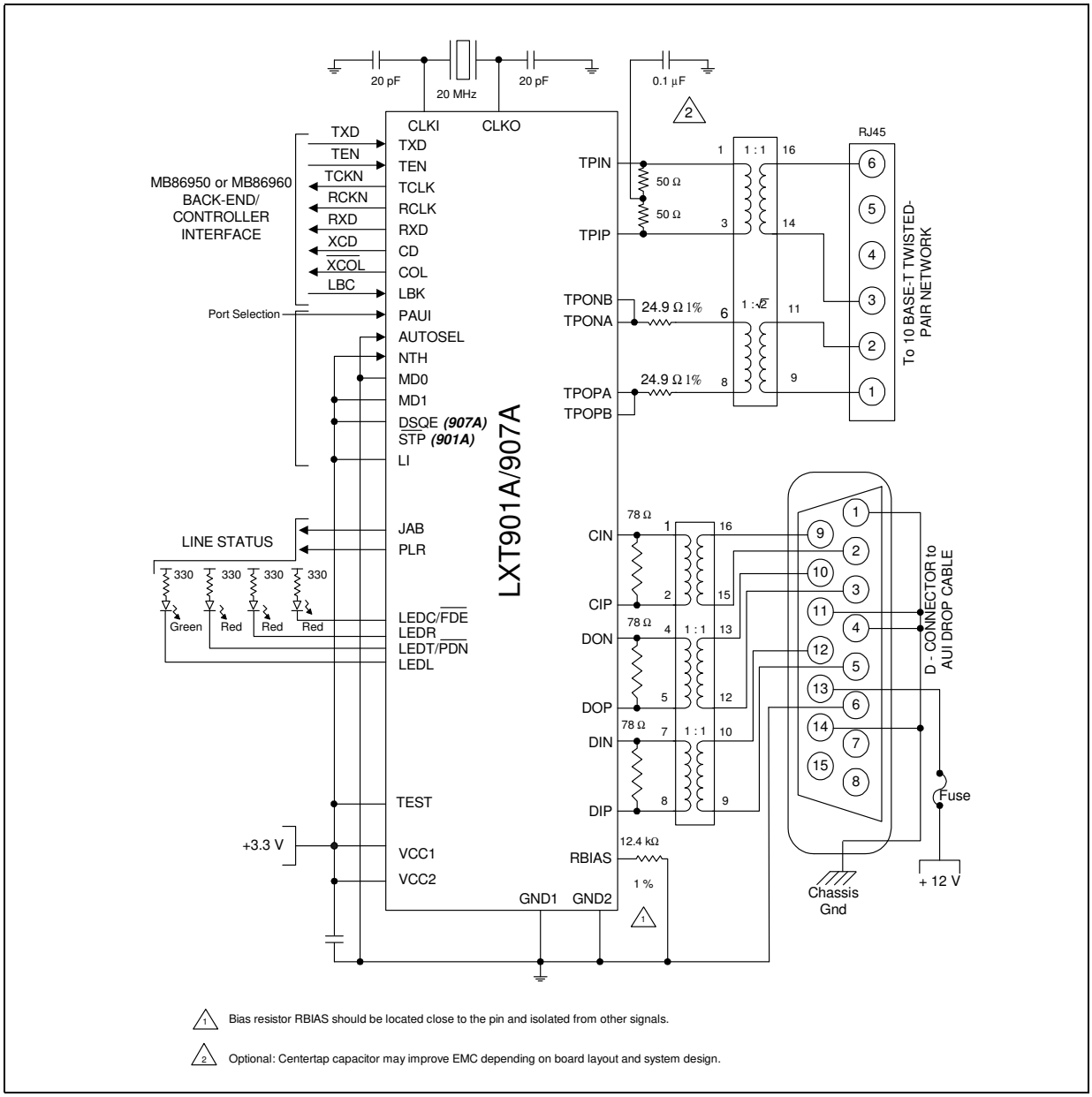
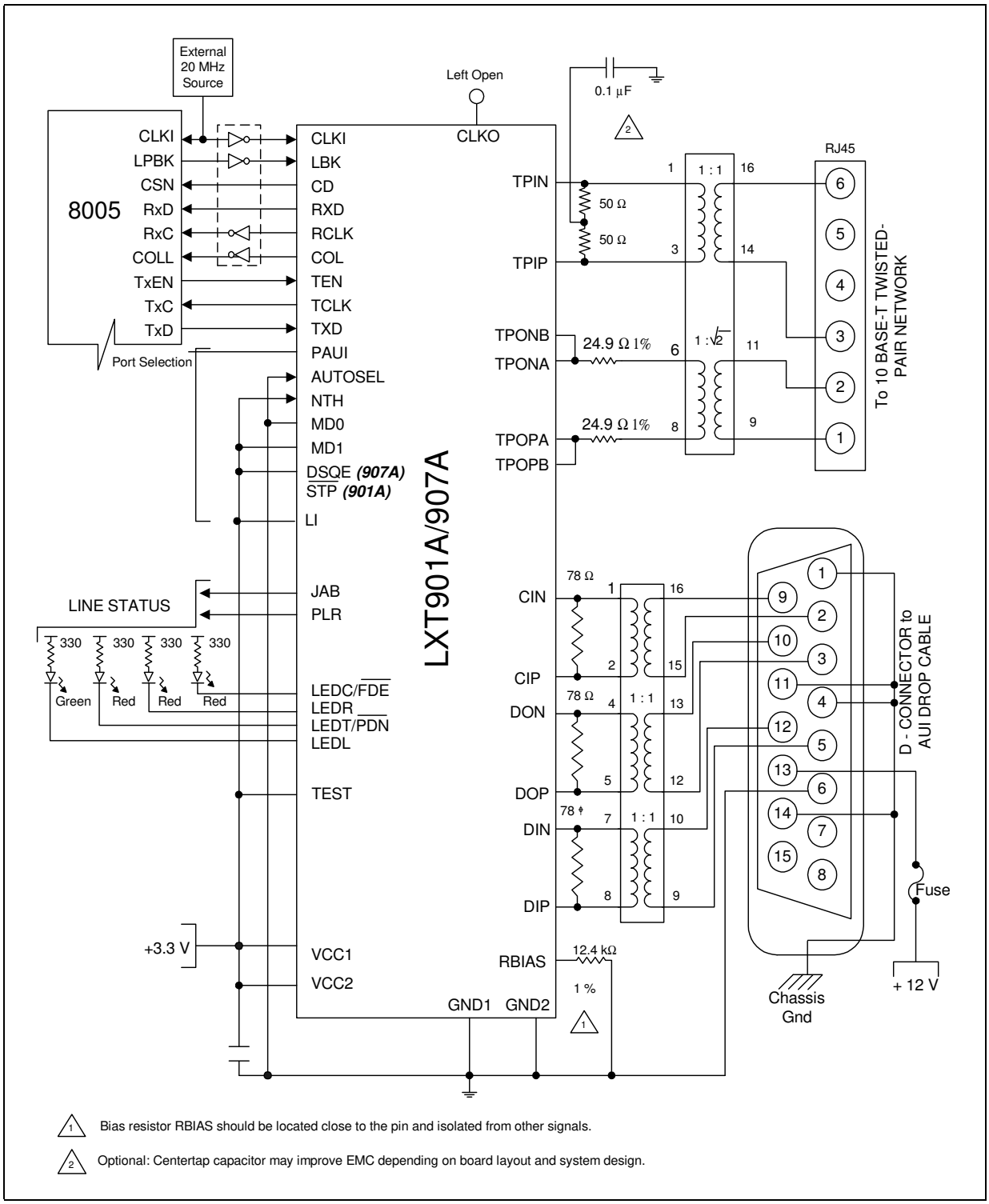


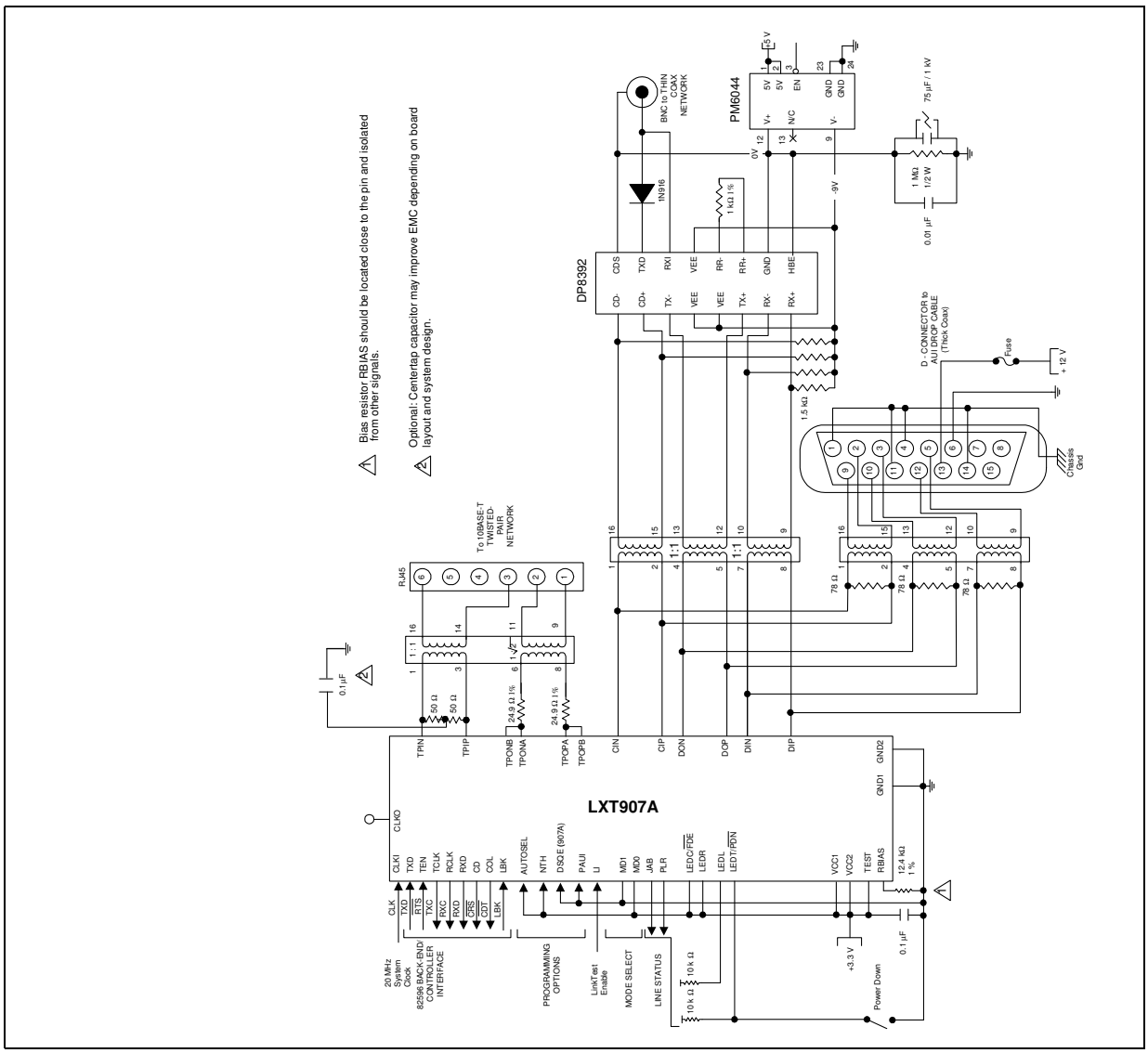
Figure 13 Manual Port Select with Seeq* 8005 Controller



3.4.5 Three Media Application

Figure 14 shows the LXT907A PHY in Mode 2 (compatible with Intel* 82596 controllers) with additional media options for the AUI port. Two transformers are used to couple the AUI port to either a D-connector or a BNC connector. A DP8392 coax transceiver with PM6044 power supply are required to drive the thin coax network through the BNC.

Figure 14 Three Media Application

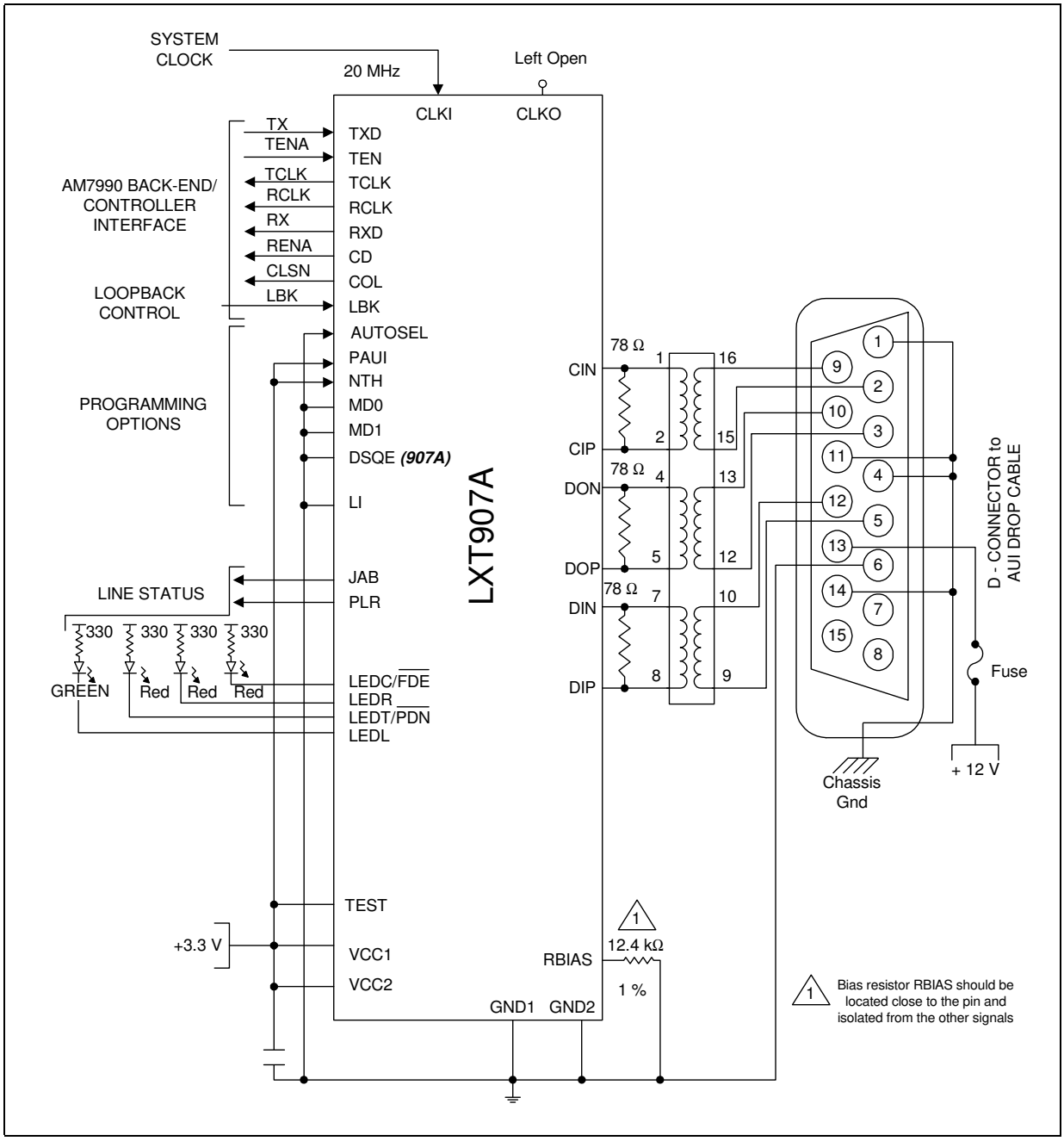


3.4.6 AUI Encoder/Decoder Only

In this application (see Figure 15) the DTE is connected to a coaxial network through the AUI. AUTOSEL is tied Low and PAUI is tied High to manually select the AUI port. The twisted-pair port is not used. With MD1 and MD0 both Low, the logic and framing are set to Mode 1 (compatible with AMD* AM7990 controllers). The LI pin is tied Low, disabling

the link test function. The DSQE pin is also Low, enabling the SQE function on the LXT907A PHY. The LBK input controls loopback. A 20 MHz system clock is supplied at CLK1 with CLK0 left open.

Figure 15 AUI Encoder/Decoder Only Application

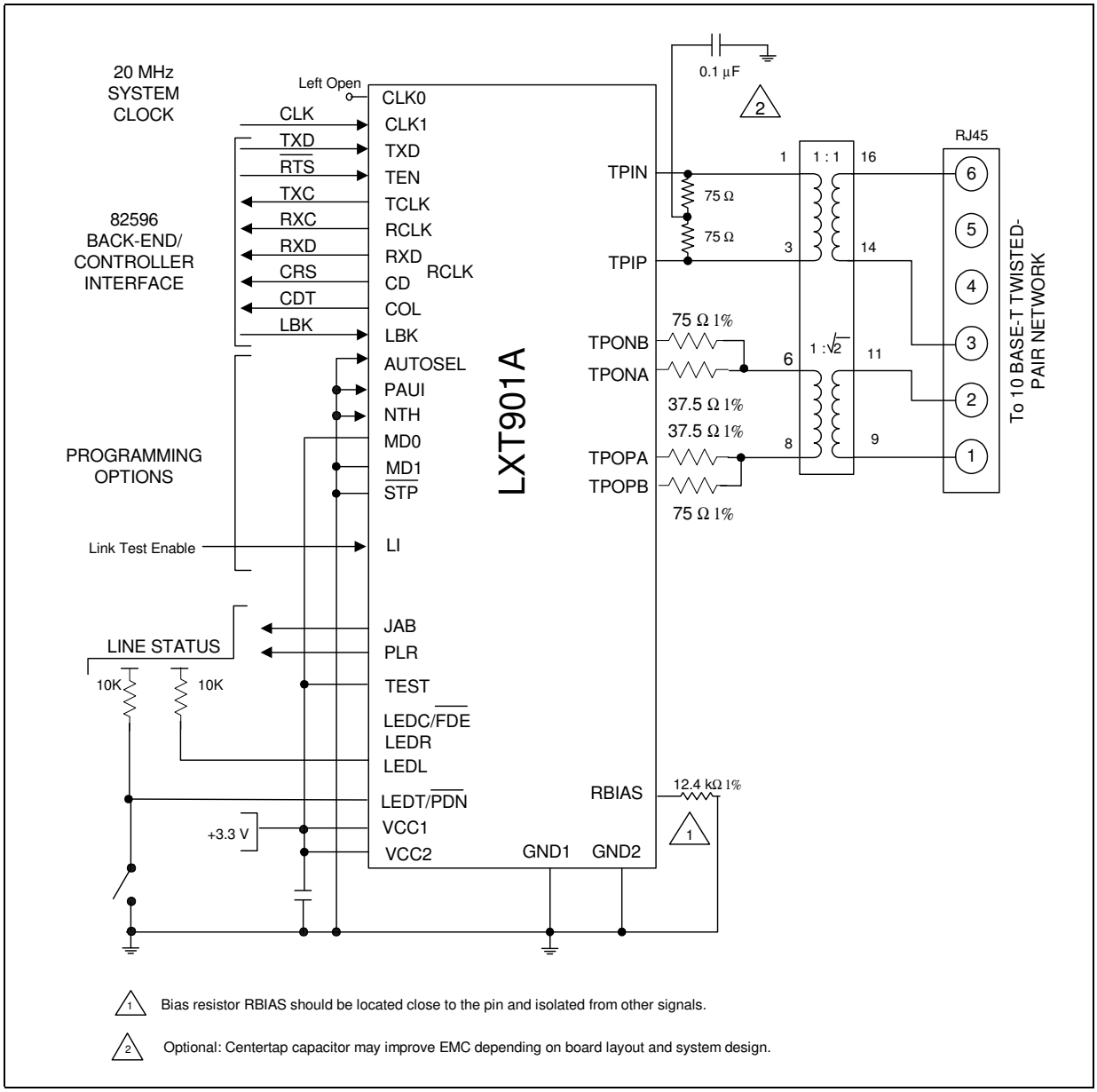


3.4.7 150 Ohm Shielded Twisted-pair only (LXT901A PHY only)

Figure 16 shows the LXT901A PHY in a typical twisted-pair only application. The DTE is connected to a 10BASE-T network through the twisted-pair RJ-45 connector. Note that the AUI port is not used. With MD0 tied High and MD1 Low, the LXT901A PHY logic and framing are set to Mode 2 (compatible with Intel* 82596 controllers).

A 20 MHz system clock input at CLK1 is used in place of the crystal oscillator. (CLK0 is left open). The L1 pin externally controls the link test function. The STP and NTH pins are both tied Low, selecting the reduced receiver threshold and 150 Ω termination for shielded TP cable. The switch at LEDT/PDN manually controls the power down mode.

Figure 16 150 Ohm Shielded Twisted-Pair Only Application (LXT901A PHY)



4.0 Test Specifications

Note: Table 4 through Table 13 and Figure 17 through Figure 42 represent the performance specifications of the LXT901A/907A PHY. These specifications are guaranteed by test except where noted "by design." Minimum and maximum values listed in Table 6 through Table 13 apply over the recommended operating conditions specified in Table 5.

Table 4 Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage	VCC	-0.3	6	V
Ambient operating temperature (Commercial)	TA	0	+70	ºC
Storage temperature	TSTG	-65	+150	ºC

Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Recommended supply voltage[1]	VCC	3.13	3.3	3.47	V
Recommended operating temperature (Commercial)	TOP	0	–	+70	ºC

1. Voltages with respect to ground unless otherwise specified. Power supply should be filtered to suppress high frequency transients, consistent with good PCB design.

Table 6 I/O Electrical Characteristics (Sheet 1 of 2)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage[2]		VIL	–	–	0.8	V	
Input High voltage[2]		VIH	2.0	–	–	V	
Output Low voltage		VOL	–	–	0.4	V	IOL = 1.6 mA
		VOL	–	–	10	%VCC	IOL < 10 µA
Output Low voltage (Open drain LED driver)		VOLL	–	–	0.7	%VCC	IOLL = 10 mA
Output High voltage		VOH	2.4	–	–	V	IOH = 40 µA
		VOH	90	–	–	%VCC	IOH < 10 µA
Output rise time TCLK & RCLK	CMOS	–	–	7	12	ns	CLOAD = 20 pF
	TTL	–	–	7	8	ns	
Output fall time TCLK & RCLK	CMOS	–	–	7	12	ns	CLOAD= 20 pF
	TTL	–	–	7	8	ns	
CLKI rise time (externally driven)		–	–	–	10	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0 V and 3 V.

Table 6 I/O Electrical Characteristics (Sheet 2 of 2)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
CLKI duty cycle (externally driven)		–	–		40/60	%	
Supply current	Normal Mode	ICC	–	65	85	mA	Idle Mode
		ICC	–	95	120	mA	Transmitting on TP
		ICC	–	95	120	mA	Transmitting on AUI
	Power Down Mode	ICC	–	0.03	2	mA	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0 V and 3 V.

Table 7 AUI Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low current	IIL	–	–	-700	µA	
Input High current	IIH	–	–	500	µA	
Differential output voltage	VOD	±550	–	±1200	mV	
Differential squelch threshold	VDS	150	250	350	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 8 TP Electrical Characteristics

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance		ZOUT	–	5	–	Ω	
Transmit timing jitter addition[2]		–	–	±3.3	±10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections[2, 3]		–	–	±3.3	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU
Receive input impedance		ZIN	–	20	–	kΩ	Between TPIP/TPIN, CIP/CIN & DIP/DIN
Differential squelch Threshold	Normal threshold; NTH = 1	VDS	300	400	585	mV	5 MHz square wave input
	Reduced threshold; NTH = 0	VDS	180	250	345	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 9 Switching Characteristics

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Jabber Timing	Maximum transmit time	–	20	–	150	ms
	Unjab time	–	250	–	750	ms
Link Integrity Timing	Time link loss receive	–	50	–	150	ms
	Link min receive	–	2	–	7	ms
	Link max receive	–	50	–	150	ms
	Link transmit period	–	8	10	24	ms

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 10 RCLK/Start-of-Frame Timing

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Decoder acquisition time	AUI	tDATA	–	900	1100	ns
	TP	tDATA	–	1200	1500	ns
CD turn-on delay	AUI	tCD	–	25	200	ns
	TP	tCD	–	425	550	ns
Receive data setup from RCLK	Mode 1	tRDS	60	70	–	ns
	Modes 2, 3 and 4	tRDS	30	45	–	ns
Receive data hold from RCLK	Mode 1	tRDH	10	20	–	ns
	Modes 2, 3 and 4	tRDH	30	45	–	ns
RCLK shut off delay from CD assert (LXT907A PHY only; Mode 3)		tsws	–	±100	–	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 11 RCLK/End-of-Frame Timing

Parameter	Type	Sym	Mode 1	Mode 2	Mode 3	Mode 4	Units
RCLK after CD off	Min	tRC	5	1	27	5	BT
Rcv data throughput delay	Max	tRD	400	375	375	375	ns
CD turn off delay[2]	Max	tCDOFF	500	475	475	475	ns
Receive block out after TEN off	Typ[1]	tIFG	5	50	–	–	BT
RCLK switching delay after CD off (LXT907A PHY only; Mode 3)	Typ[1]	tSWE	–	–	120(±80)	–	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. CD turn-off delay measured from middle of last bit: timing specification is unaffected by the value of the last bit.

Table 12 Transmit Timing

Parameter	Symbol	Minimum	Typical [1]	Maximum	Units
TEN setup from TCLK	tEHCH	22	–	–	ns
TXD setup from TCLK	tDSCH	22	–	–	ns
TEN hold after TCLK	tCHEL	5	–	–	ns
TXD hold after TCLK	tCHDU	5	–	–	ns
Transmit start-up delay - AUI	tSTUD	–	220	450	ns
Transmit start-up delay - TP	tSTUD	–	430	450	ns
Transmit through-put delay - AUI	tTPD	–	–	300	ns
Transmit through-put delay - TP	tTPD	–	300	350	ns
1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.					

Table 13 Collision, COL/CI Output and Loopback Timing

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
COL turn-on delay	tCOLD	–	40	500	ns
COL turn-off delay	tCOLOFF	–	420	500	ns
COL (SQE) Delay after TEN off	tSQED	0.65	1.2	1.6	µs
COL (SQE) Pulse Duration	tSQEP	500	1000	1500	ns
LBK setup from TEN	tKHEH	10	25	–	ns
LBK hold after TEN	tKHEL	10	0	–	ns
1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.					

4.1 Timing Diagrams for Mode 1 (MD1 = Low, MD0 = Low) Figure 17 through Figure 22

Figure 17 Mode 1 RCLK/Start-of-Frame Timing

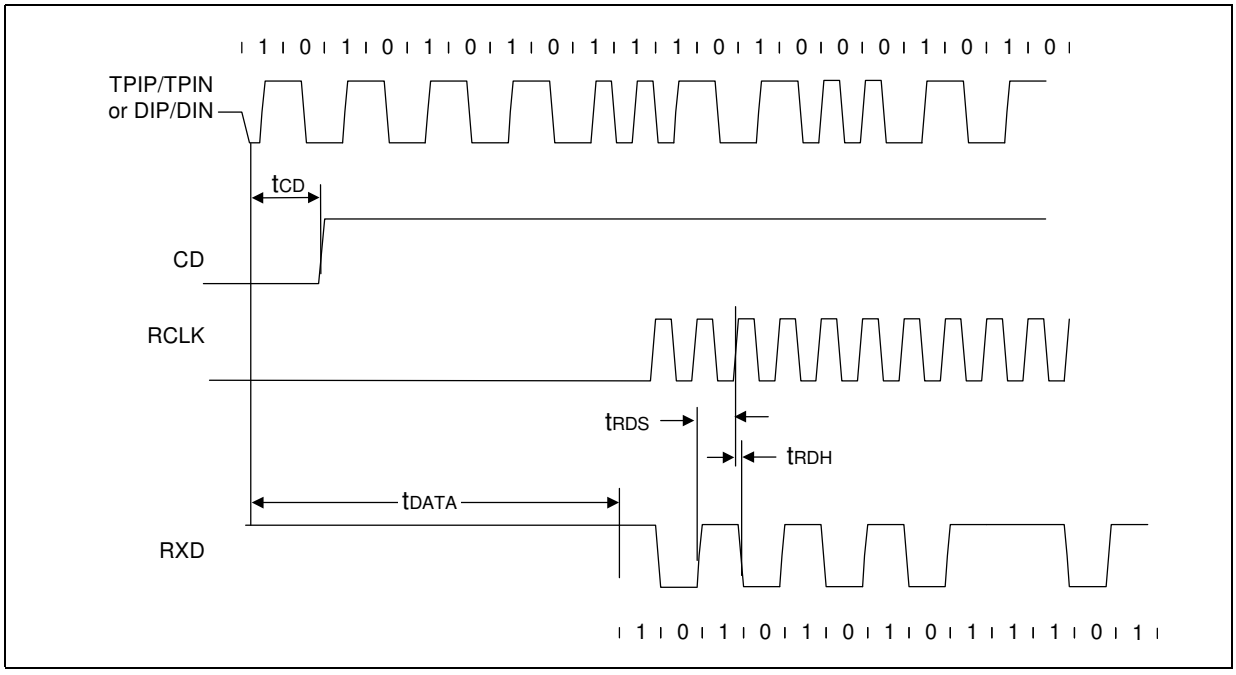


Figure 18 Mode 1 RCLK/End-of-Frame Timing

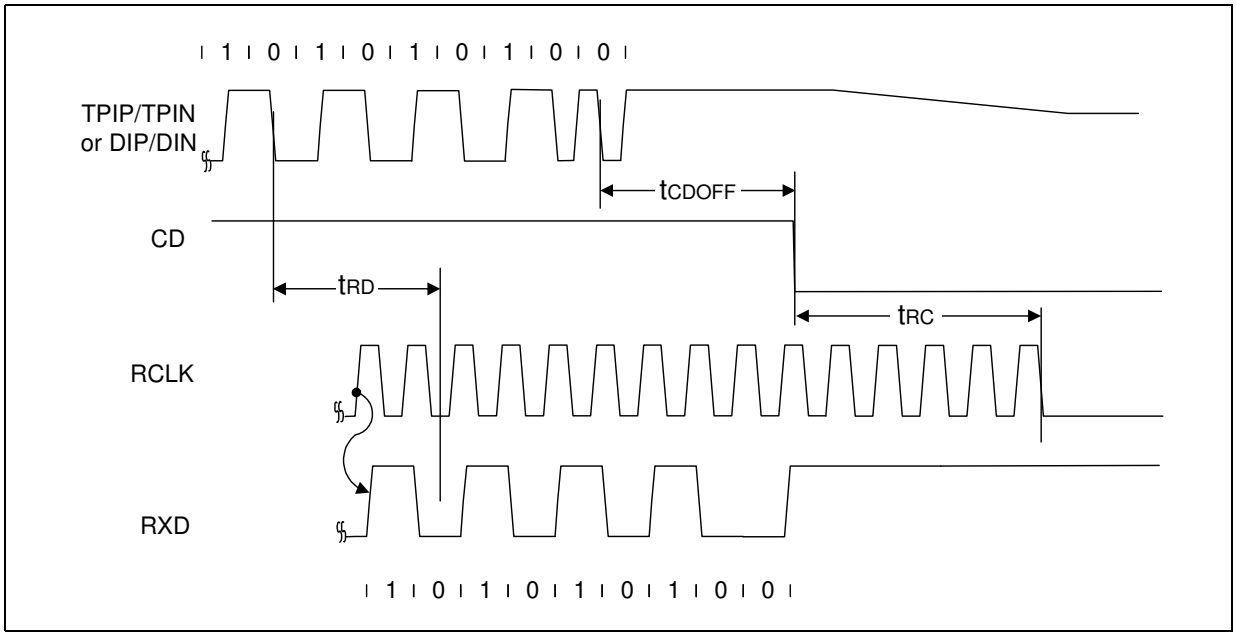


Figure 19 Mode 1 Transmit Timing

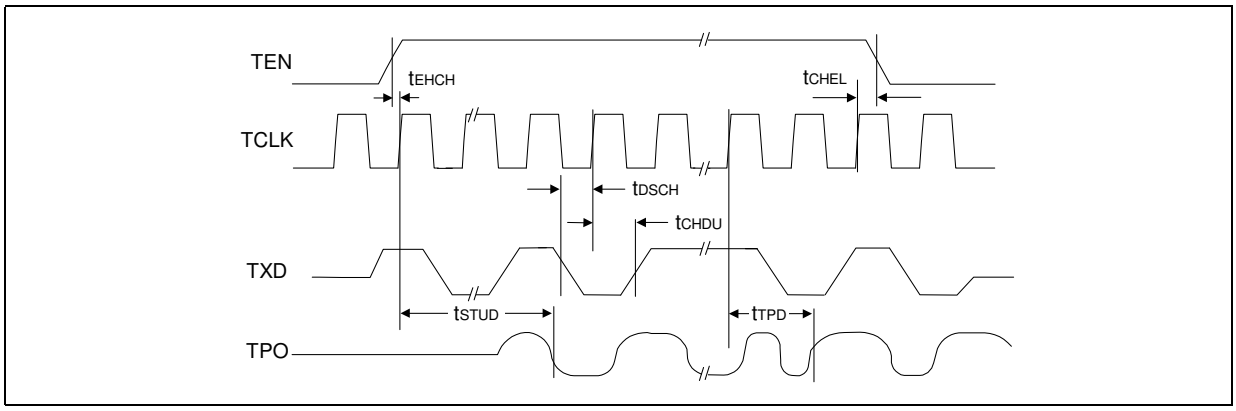


Figure 20 Mode 1 Collision Detect Timing

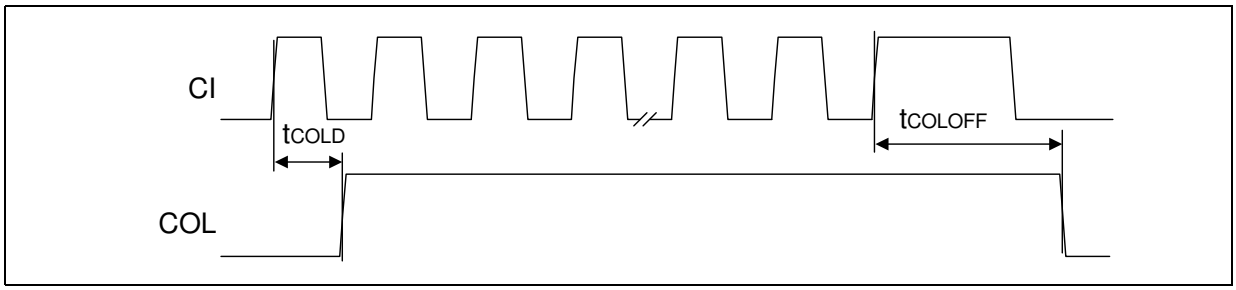


Figure 21 Mode 1 COL/CI Output Timing

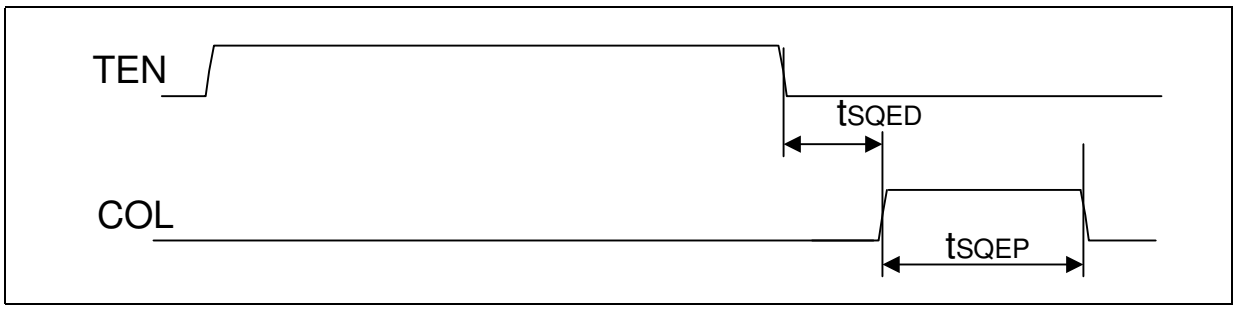


Figure 22 Mode 1 Loopback Timing

4.2 Timing Diagrams for Mode 2 (MD1=Low, MD0=High) Figure 23 through Figure 28

Figure 23 Mode 2 RCLK/Start-of-Frame Timing

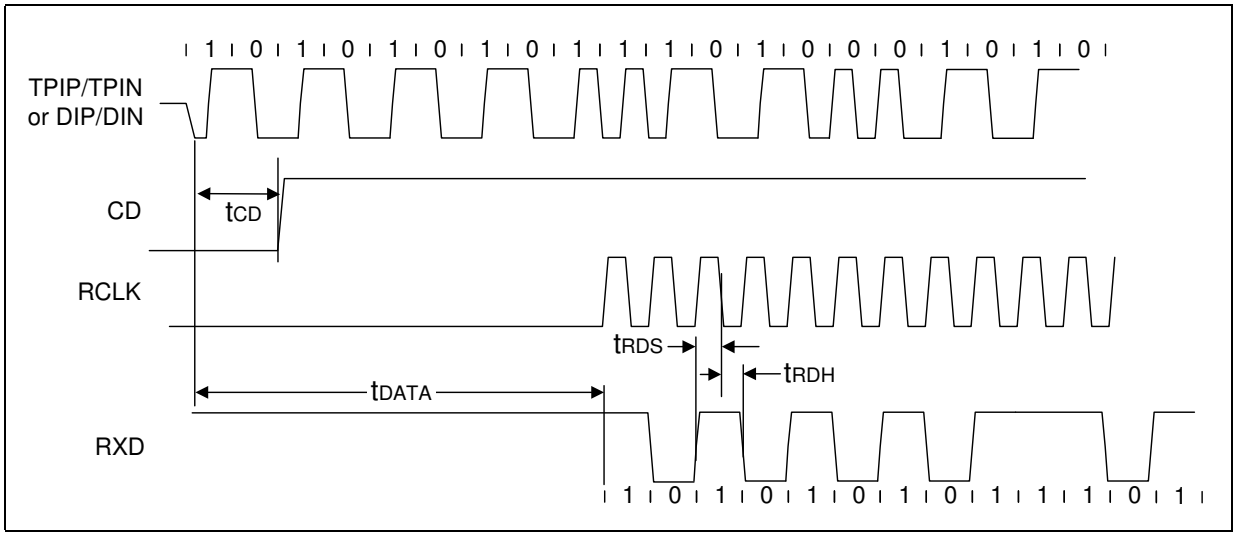


Figure 24 Mode 2 RCLK/End-of-Frame Timing

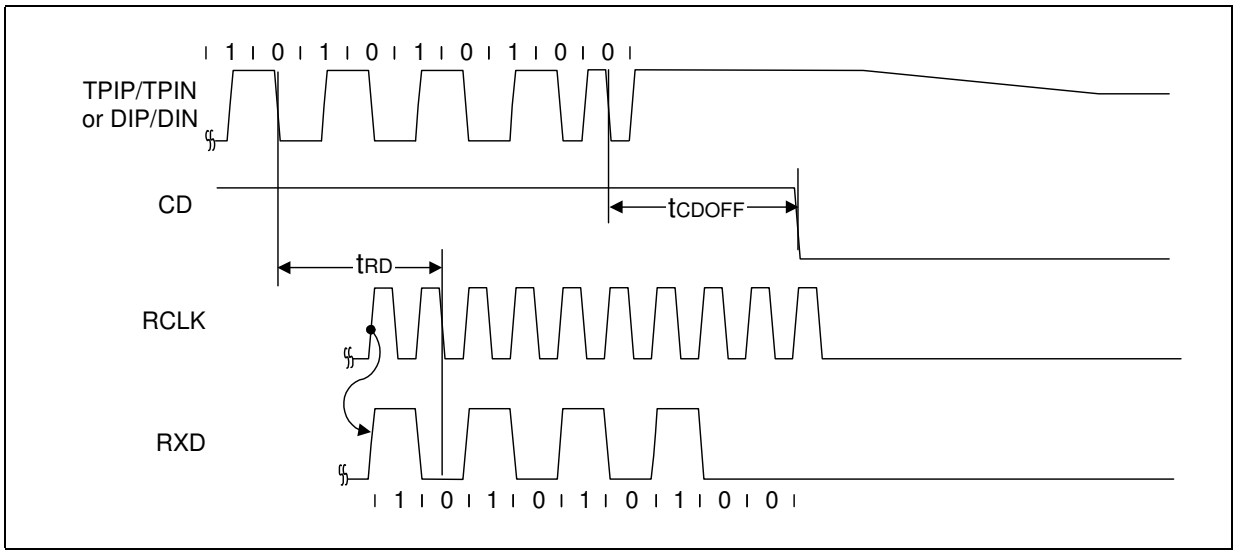


Figure 25 Mode 2 Transmit Timing

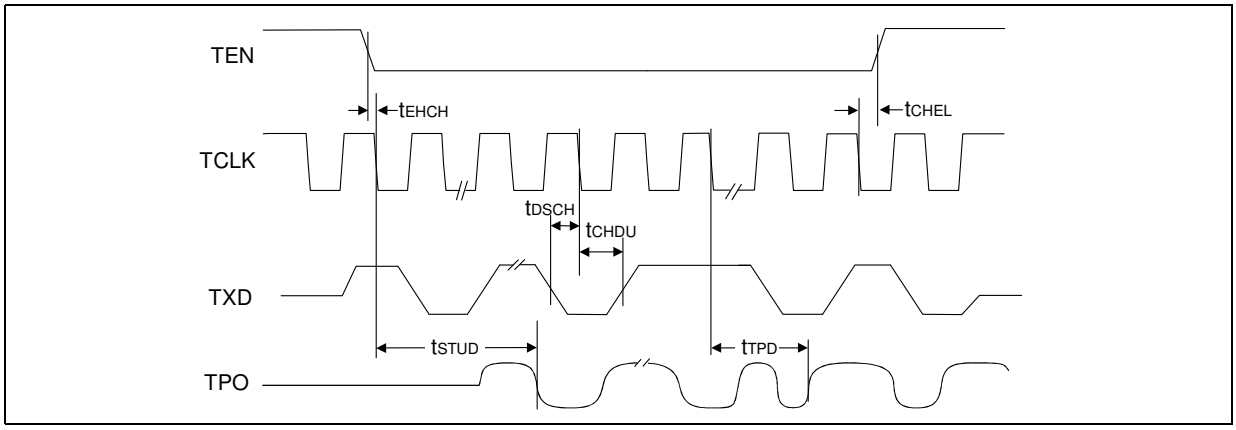


Figure 26 Mode 2 Collision Detect Timing

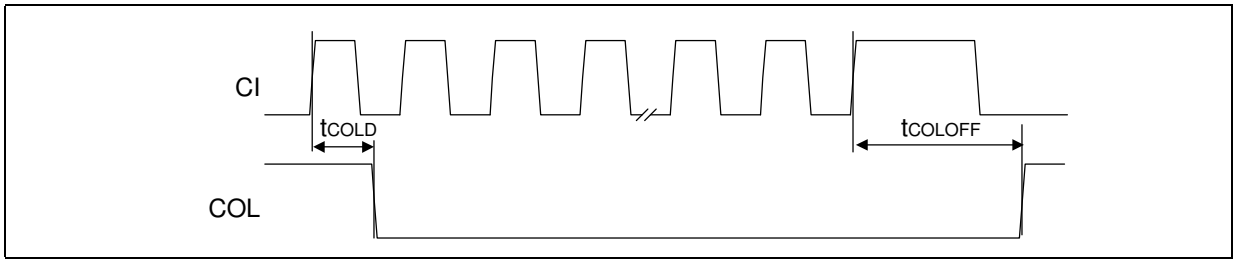


Figure 27 Mode 2 COL/CI Output Timing

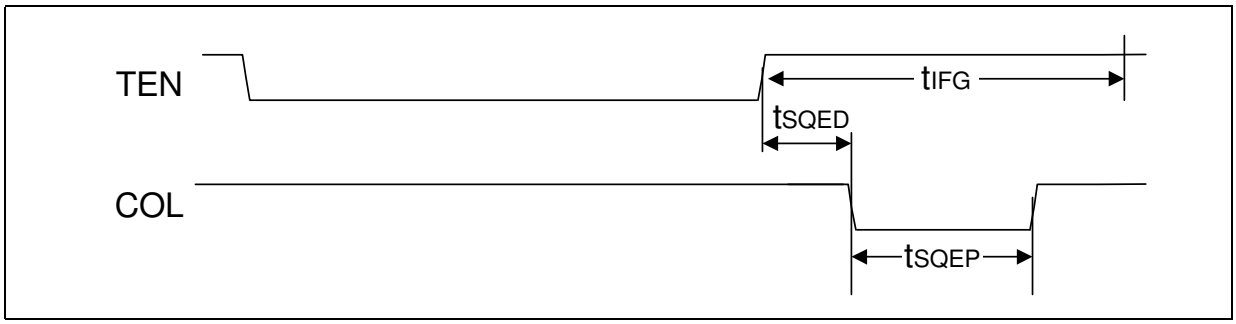
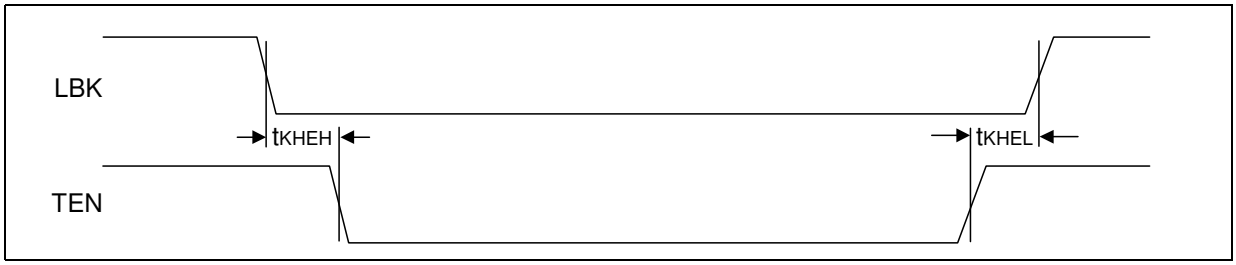


Figure 28 Mode 2 Loopback Timing



4.3 Timing Diagrams for Mode 3 (MD1 = High, MD0 = Low) Figure 29 through Figure 36

Figure 29 Mode 3 RCLK/Start-of-Frame Timing (LXT901A PHY)

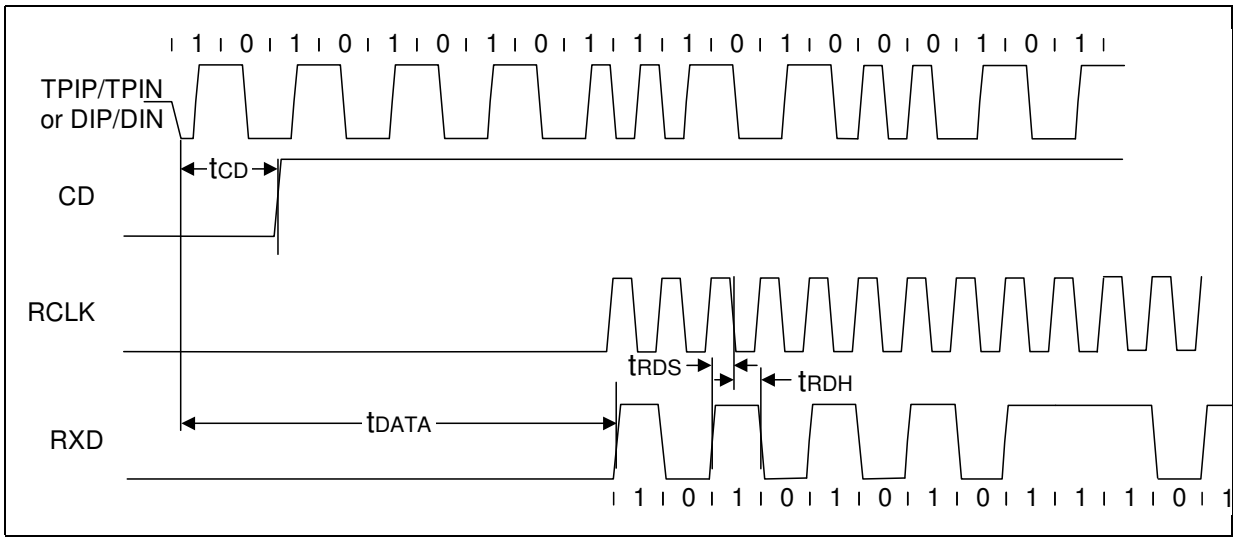


Figure 30 Mode 3 RCLK/End-of-Frame Timing (LXT901A PHY)

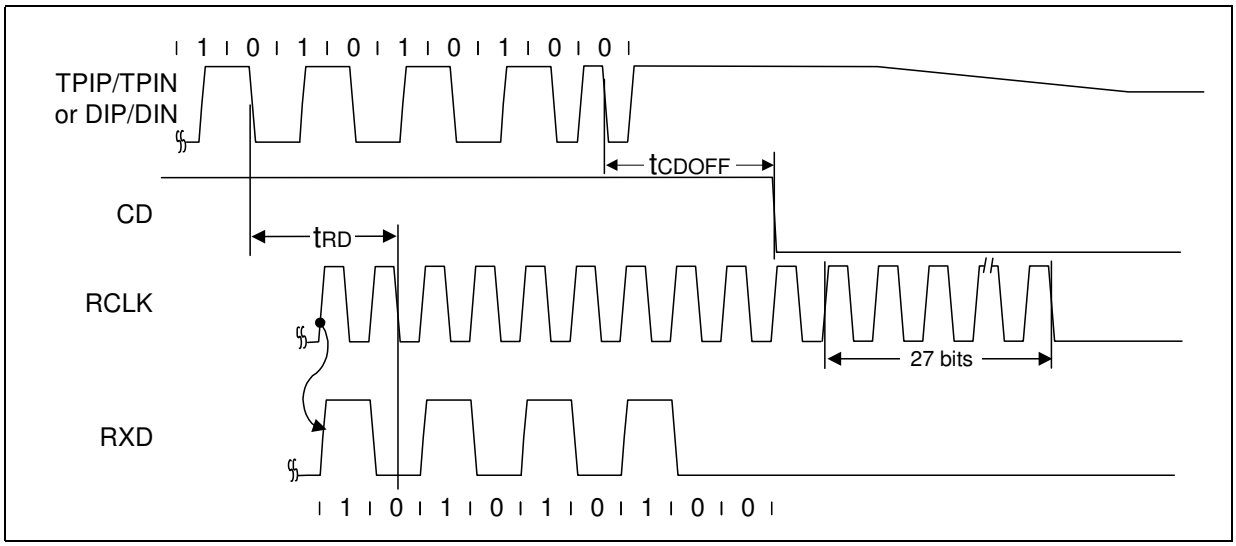


Figure 31 Mode 3 RCLK/Start-of-Frame Timing (LXT907A PHY)

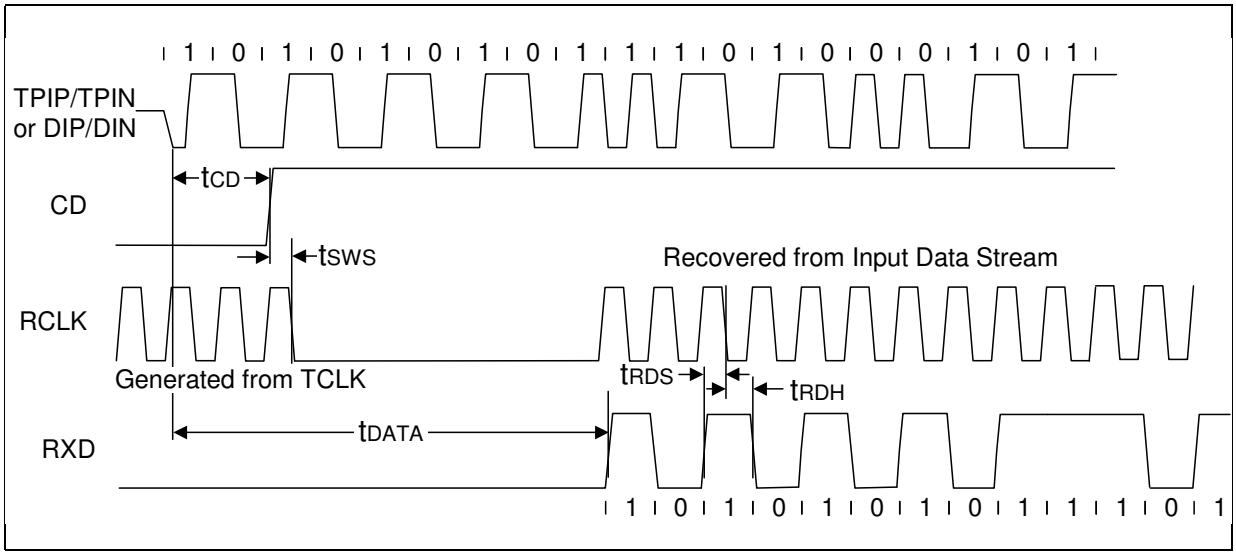


Figure 32 Mode 3 RCLK/End-of-Frame Timing (LXT907A PHY)

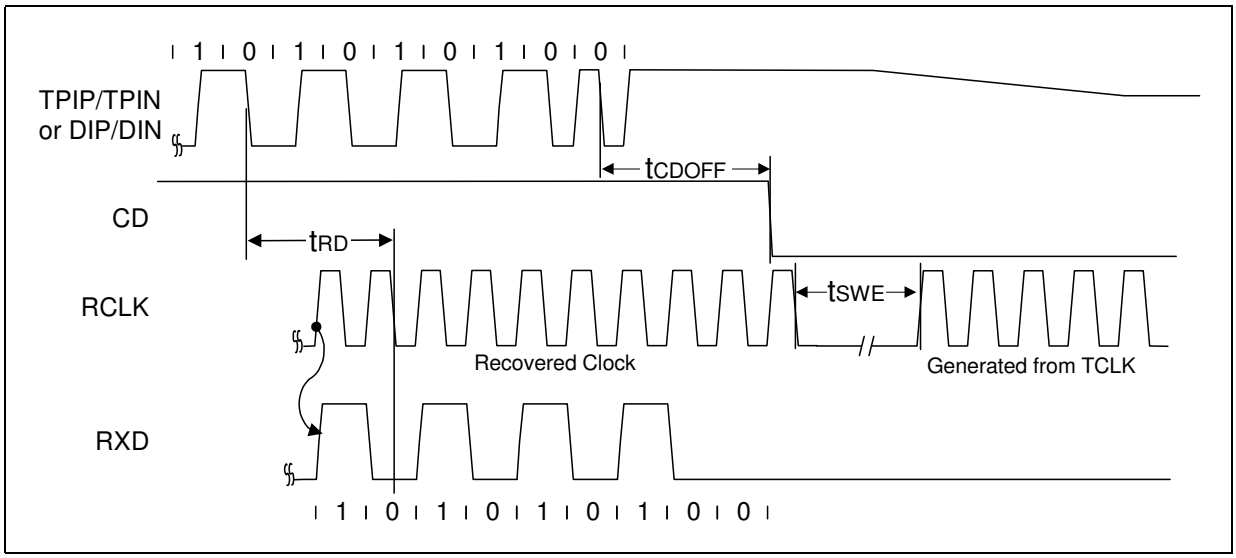


Figure 33 Mode 3 Transmit Timing

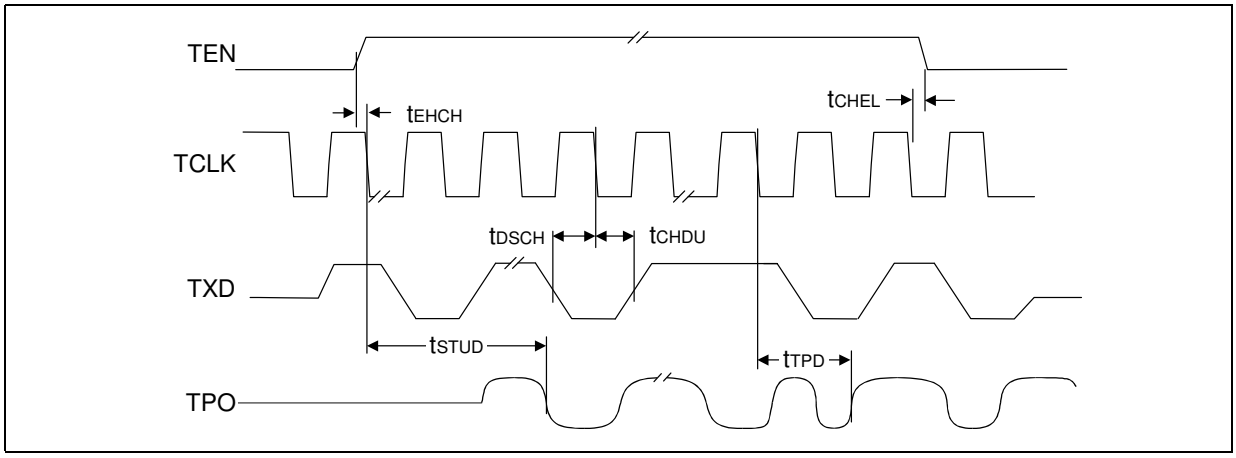


Figure 34 Mode 3 Collision Detect Timing

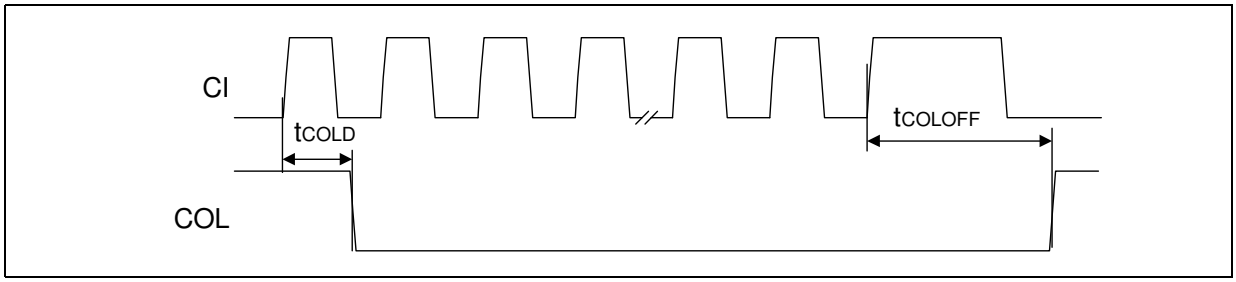


Figure 35 Mode 3 COL/CI Output Timing

Figure 36 Mode 3 Loopback Timing

4.4 Timing Diagrams for Mode 4 (MD1 = High, MD0 = High) Figure 37 through Figure 42

Figure 37 Mode 4 RCLK/Start-of-Frame Timing

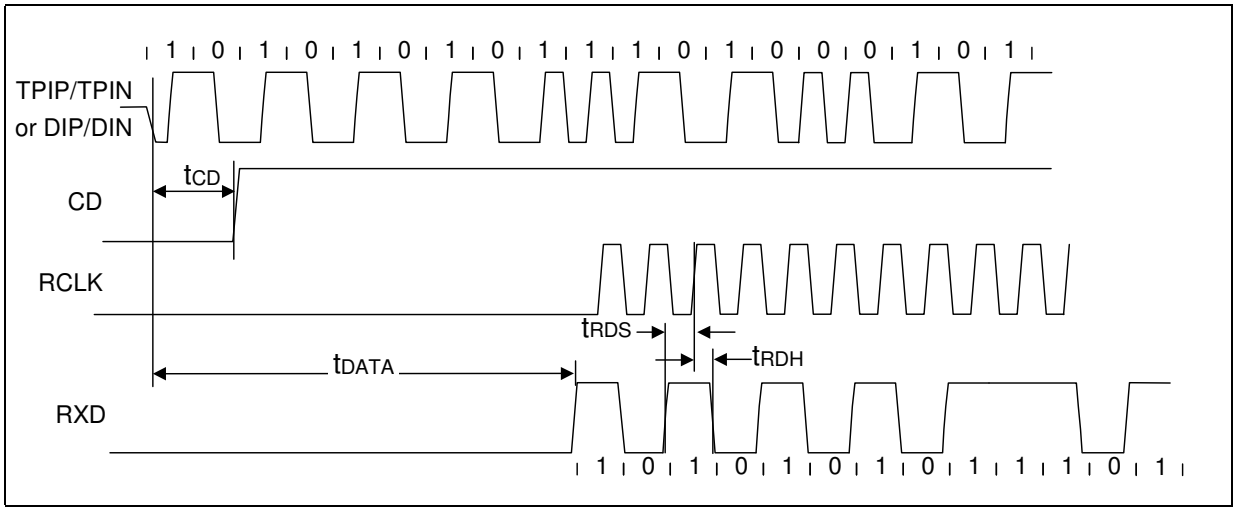


Figure 38 Mode 4 RCLK/End-of-Frame Timing

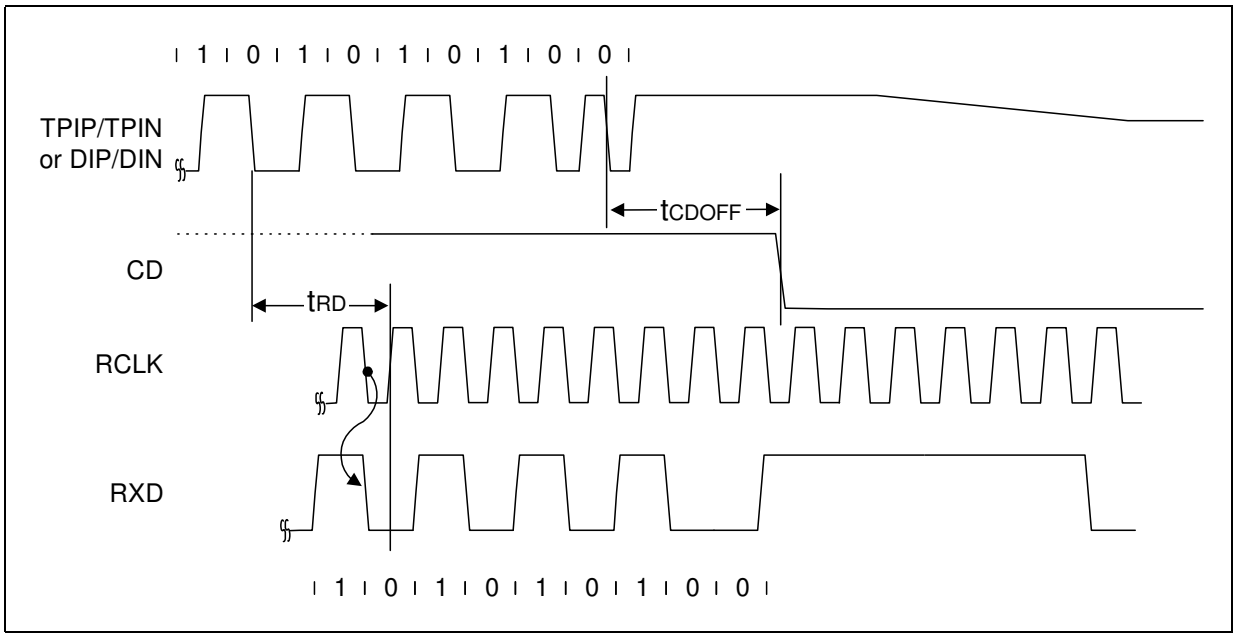


Figure 39 Mode 4 Transmit Timing

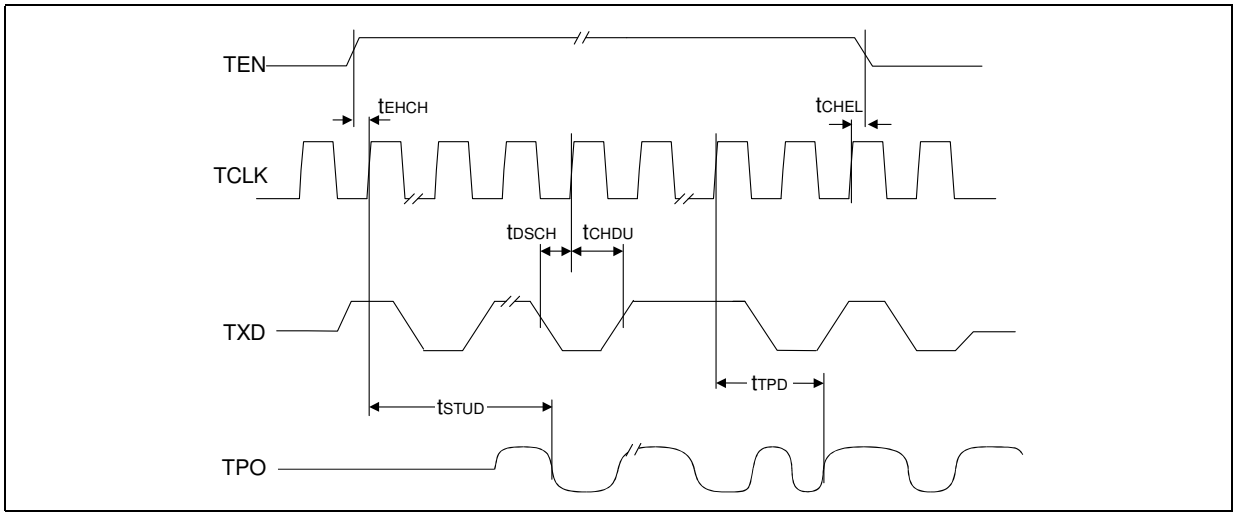


Figure 40 Mode 4 Collision Detect Timing

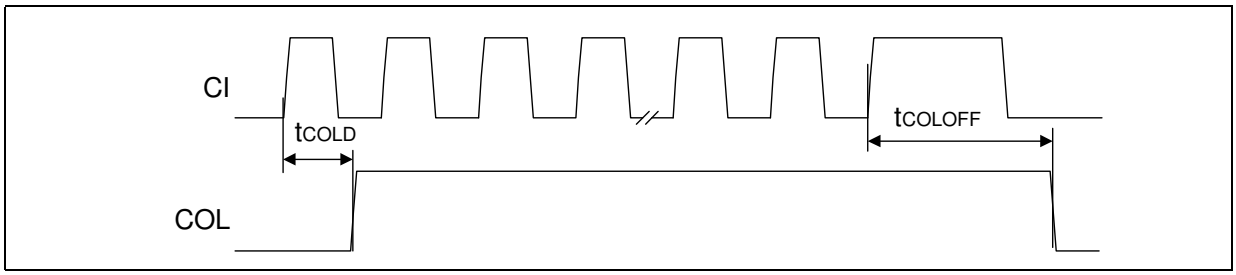


Figure 41 Mode 4 COL/CI Output Timing

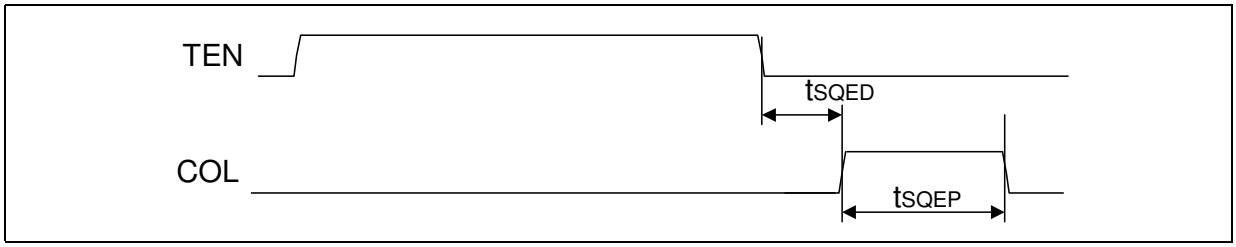


Figure 42 Mode 4 Loopback Timing

5.0 Mechanical Specifications

Figure 43 44-Pin PLCC

44-Pin Plastic Leaded Chip Carrier

- Part Number LXT901APC and LXT907APC (Commercial Temperature Range)

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	0.050	–	1.270	–
C	0.026	0.032	0.660	0.813
D	0.685	0.695	17.399	17.653
D1	0.650	0.656	16.510	16.662
F	0.013	0.021	0.330	0.533

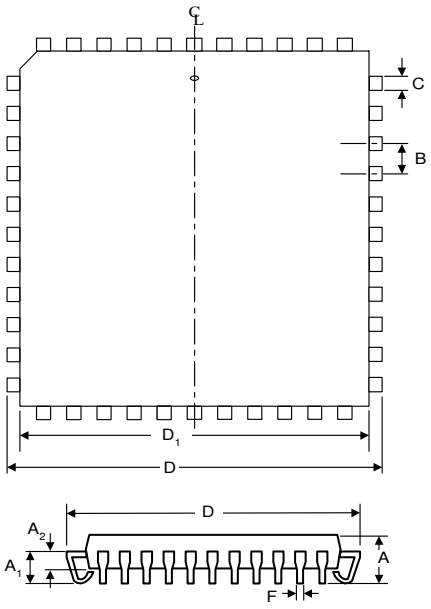
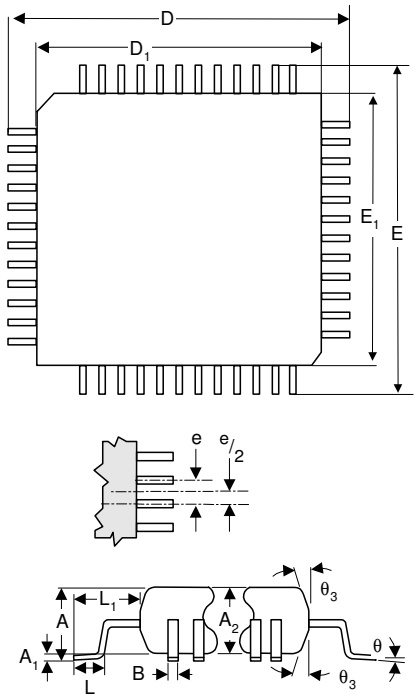


Figure 44 64-Pin LQFP

64-Pin Low-Profile Quad Flat Package

- Part Number LXT901ALC and LXT907ALC (Commercial Temperature Range)

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.063	–	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	.011	0.17	0.27
D	0.472 BSC		12.00 BSC	
D1	0.394 BSC		10.00 BSC	
E	0.472 BSC		12.00 BSC	
E1	0.394 BSC		10.00 BSC	
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
L1	0.039 REF		1.00 REF	
θ3	11°	13°	11°	13°
θ	0°	7°	0°	7°



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