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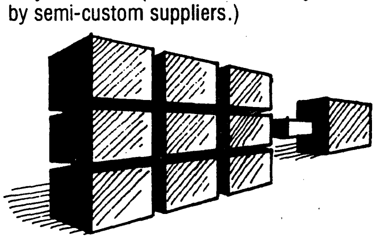

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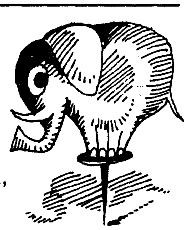

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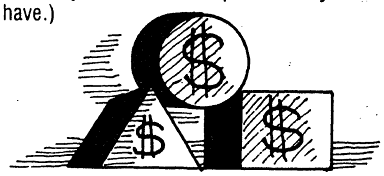

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our universal design rules let us use numerous fabricators, which ensures delivery of your chips on time. The more product you can ship on time, the more money you make. (With semi-custom, multi-sourcing is normally not available.)

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our engineers concentrate on designing the chip and the test program that goes with it, while *your* engineers concentrate on developing new products. (With semi-custom, your engineers are all tied up designing the chip and test program.)

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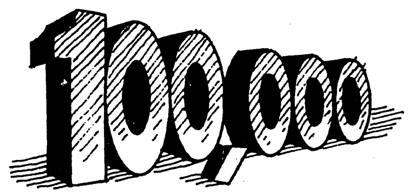

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- ☐ Phased locked loop touch sensitive light dimmer/switches
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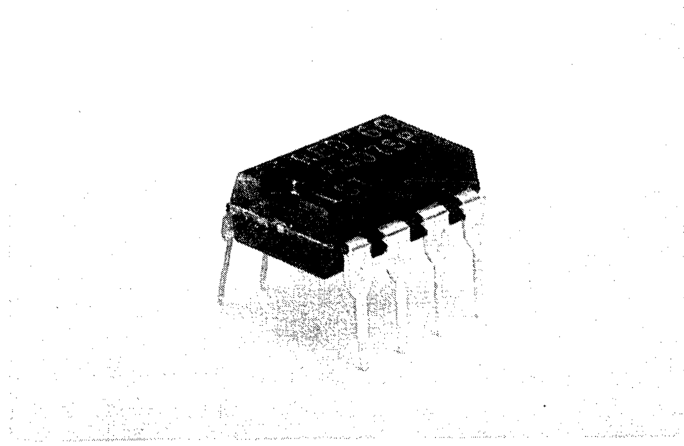
RED SERIES | COMPLEMENTARY MOS (CMOS) DIVIDER CIRCUITS

REVISED NOVEMBER 1985

RED SERIES

RED 5/6	Divide by 5 or 6
RED 50/60	Divide by 50 or 60
RED 100/120	Divide by 100 or 120
RED 300/360	Divide by 300 or 360
RED 500/600	Divide by 500 or 600
RED 3000/3600	Divide by 3000 or 3600



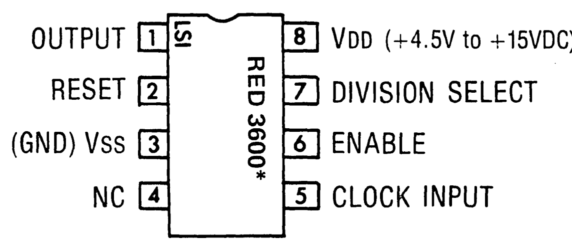
FEATURES:

- Clock input pulse shaper accepts 50 Hz/60 Hz sine wave directly
- Fully static counter operation
- +4.5V to +15V operation (V_{DD} - V_{SS})
- Low power dissipation
- High noise immunity
- Reset
- Input Enable
- 50 Hz/60 Hz division select input
- Ouput low power TTL compatible at +4.5V operation.
- All inputs protected.
- Square Wave Output (except for ÷ 5)

APPLICATION:

Time base generator from either 50 Hz or 60 Hz line frequency to produce:

10 pulses per second	(RED 5/6)
1 pulse per second	(RED 50/60)
1 pulse per 2 seconds	(RED 100/120)
1 pulse per .1 minute	(RED 300/360)
1 pulse per 10 seconds	(RED 500/600)
1 pulse per minute	(RED 3000/3600)



TOP VIEW

STANDARD
8 PIN PLASTIC DIP

DESCRIPTION OF OPERATION:

The counter advances by one on each negative transition of the input clock pulse as long as the Enable signal is "High" and the Reset signal is "Low". When the Enable signal is "Low" the input clock pulses will be inhibited and the counter will be held at the state it was in prior to bringing the Enable "Low". A "High" Reset signal clears the counter to zero count.

Depending on the device used, a "Low" on the Division Select input will cause a Divide by 6, 60, 120, 360, 600 or 3600. A "High" on the Division Select will cause a Divide by 5, 50, 100, 300, 500 or 3000.

*Marking as follows:

PART	MARKING
RED 5/6	RED 6
RED 50/60	RED 60
RED 100/120	RED 120
RED 300/360	RED 360
RED 500/600	RED 600
RED 3000/3600	RED 3600

MAXIMUM RATINGS:

	Symbol	Value	Unit
DC Supply Voltage:	V_{DD}	+18 to -0.5	VDC
Input Voltage:	V_{IN}	V_{DD} to V_{SS}	VDC
Oper. Temp. Range:	T_A	-40 to +85	°C
Storage Temp. Range.	Tstg	-65 to +150	°C

ELECTRICAL CHARACTERISTICS: (TA = 25° unless otherwise specified)

TEST CONDITIONS: Vss = 0V
Output Capacitance Load = 15 pF
Input Rise and Fall times = 20 ns, except clock Rise and Fall times

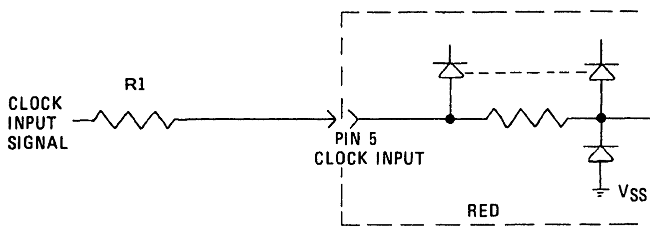
		VDD	Min	Max	Units
	Quiescent Device Current:	5V		10	uA
		10V		20	uA
	Output Voltage, Low Level:	5V		0.01	Volts
		10V		0.01	Volts
	High Level:	5V	4.99		Volts
		10V	9.99		Volts
	Clock Input Voltage, Low Level	5V		1	Volts
		10V		2	Volts
	High Level	5V	4		Volts
		10V	8		Volts
	Input Noise Immunity (except clock):	5V	1.5		Volts
	(Low and High)	10V	3.0		Volts
	Output Drive Current:				
Full Temp. Range	N Channel Sink Current:	4.5V	0.18		mA
	(Vout = Vss + .4V)	10V	0.45		mA
	P Channel Source Current:	4.5V	0.3		mA
	(Vout = VDD - 1V)	10V	0.75		mA

Input Capacitance:	(Any Input)		5	pF
Clock Rise and Fall Time:	5V	No Maximum Limit		
	10V	No Maximum Limit		
Clock Frequency:	5V	DC	600	KHz
	10V	DC	1200	KHz
Input Clock Pulse Width:	5V	800		ns
	10V	400		ns
Output Rise and Fall Time:	5V		225	ns
	10V		150	ns
Propagation Delay to Output:	5V		1500	ns
	10V		750	ns
Enable Set-up Time:	5V		300	ns
	10V		150	ns
Reset Pulse Width:	5V	800		ns
	10V	400		ns
Reset Removal Time:	5V		1200	ns
	10V		600	ns
Reset Propagation Delay to Output:	5V		1400	ns
	10V		700	ns

ENABLE SIGNAL TIMING CONSIDERATION

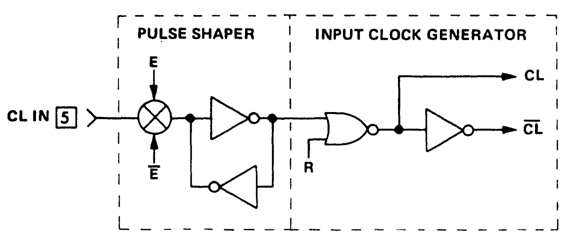
If the Enable signal switches Low during a positive clock phase and then switches High during a negative clock phase, a false count will be registered.

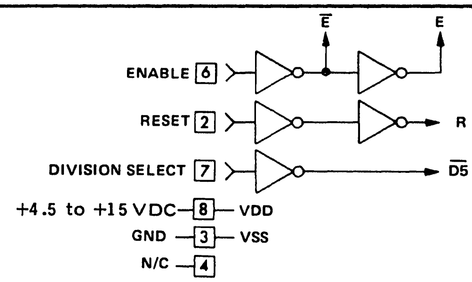
To prevent this from happening, the Enable signal should not switch Low during a positive clock phase unless the switch to High also occurs during a positive clock phase. The Enable signal should normally be switched during a negative clock phase.

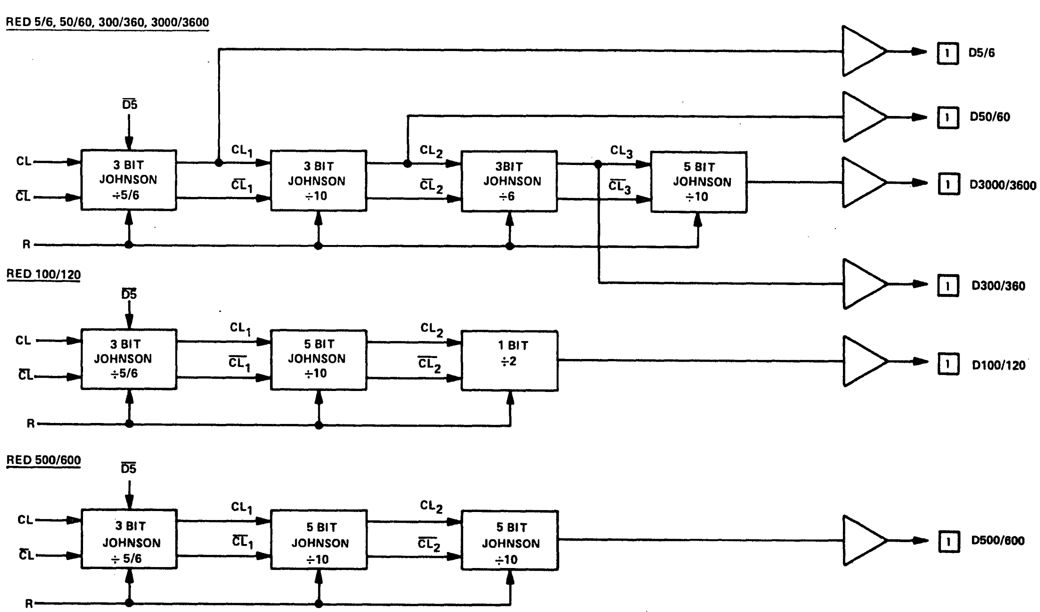


TYPICAL CLOCK INPUT

If input signals are less than V_{SS} or greater than V_{DD}, a series input resistor, R1, should be used to limit the maximum input current to 2 milliamperes.







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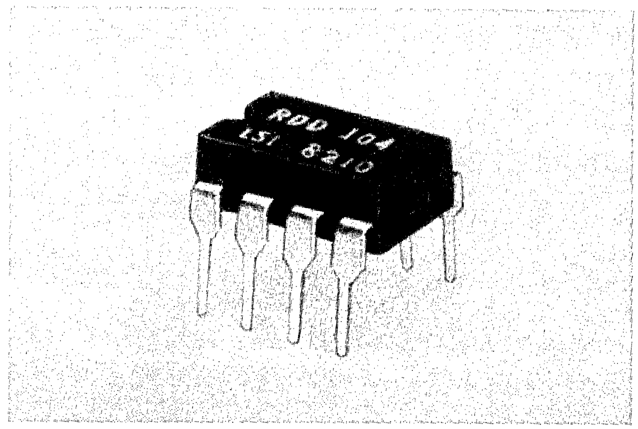
RDD104

SELECTABLE 4 DECADE CMOS DIVIDER

REVISED OCTOBER 1985



FEATURES:

- Selectable Divide by 10, 100, 1000 or 10,000
- Clock Input Shaping Network Accepts Fast or Slow Edge Inputs
- Active Oscillator Network for External Crystal
- Square Wave Output
- Output TTL Compatible at +4.5 Volt Operation
- High Noise Immunity
- Reset
- All Inputs Protected
- +4.5 to +15 Volt Operation
- Low Power Dissipation

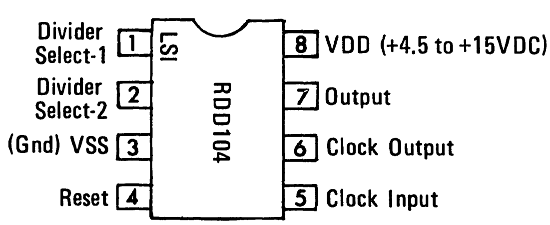
DESCRIPTION OF OPERATION:

The RDD104 is a monolithic CMOS (Complementary MOS) four decade divider circuit that advances on each negative transition of the input clock pulse. When the reset input is high the circuit is cleared to zero. The clock input is applied to a three stage amplifier network whose output is brought out so that an external crystal network can be used to form an oscillator circuit. If the clock output is not used, the amplifier acts as an input buffer. Two select inputs are provided which enables the circuit to divide by 10, 100, 1000, or 10,000.

The divider range is selected according to the following truth table:

DIVIDER SELECT INPUTS		OUTPUT DIVISION
SELECT 2 (Pin 2)	SELECT 1 (Pin 1)	
0	0	10,000
0	1	1,000
1	0	100
1	1	10

Pin Connections RDD104:



TOP VIEW
Standard 8 Pin Plastic Mini-DIP
Figure 1

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_A	−40 to +85	°C
DC Supply Voltage	V_{DD}	+18 to −0.5	VDC
Input Voltage	V_{IN}	V_{DD} to V_{SS}	VDC

D.C. ELECTRICAL CHARACTERISTICS:

(V_{SS} = 0 Volts, C Load = 50pF) Input rise and fall times = 20ns except for clock

	V_{DD}	TEMPERATURE (°C)			UNITS
		−40	+25	+85	
Quiescent Device Current	4.5V	10	10	300	μA Max
	10V	20	20	600	μA Max
Output Voltage, Low Level	4.5V	.01	.01	.05	V Min
	10V	.01	.01	.05	V Min
High Level	4.5V	4.49	4.49	4.45	V Max
	10V	9.99	9.99	9.95	V Max
Input Noise Immunity	4.5V	1.3	1.3	1.3	V Min
(Low and High)	10V	3.0	3.0	3.0	V Min
Output Drive Current	4.5V	2.3	1.9	1.6	mA Min
N Channel Sink Current	10V	5.0	4.0	3.5	mA Min
(V_{OUT}=V_{SS}+.4V)					
P Channel Source Current	4.5V	1.1	.95	.8	mA Min
(V_{OUT} = V_{DD} − 1V)	10V	2.5	2.1	1.8	mA Min
Input Capacitance (any input)			5.0		pF Max

DYNAMIC ELECTRICAL CHARACTERISTICS:

(C Load = 50pF, Input Rise and Fall Times = 20ns Except for Clock)

	V_{DD}	MIN	TYP	MAX	Units
Clock Input Frequency	4.5V	DC		1.5	MHz
	10V	DC		4.0	MHz
	15V	DC		6.0	MHz
Clock Input Rise and Fall Times	4.5 to 15V			No Limit	
Clock Output Rise and Fall Time CL=15pF	4.5V			140	ns
	10V			70	ns
Clock Output Propagation Delay CL=15pF	4.5V			300	ns
	10V			150	ns
Output Rise & Fall Times	4.5V			400	ns
	10V			200	ns
Propagation Delay to Output	4.5V			1500	ns
	10V			750	ns
Reset Pulse Width	4.5V	800			ns
	10V	400			ns
Reset Removal Time	4.5V			500	ns
	10V			250	ns
Reset Propagation Delay to Output	4.5V			1400	ns
	10V			700	ns
Select Input Setup Time	4.5V			800	ns
	10V			400	ns

Minimum Part Oscillator Circuit

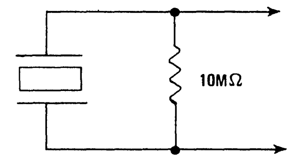


Figure 2

Typical Oscillator Circuit 1 MHz and Below with Trim

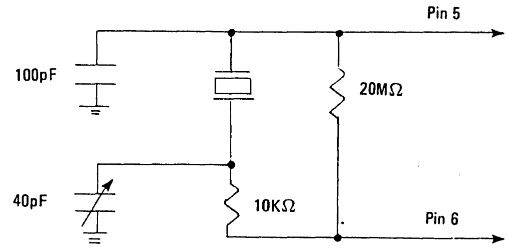


Figure 3

Typical Oscillator Circuit Above 1 MHz with Trim

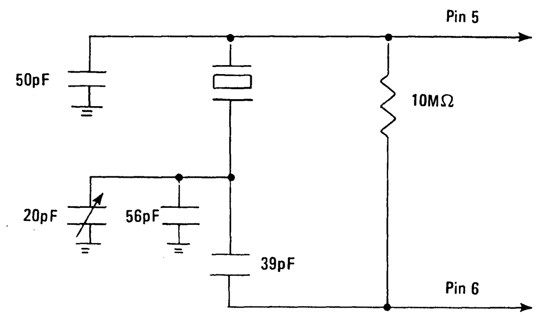


Figure 4

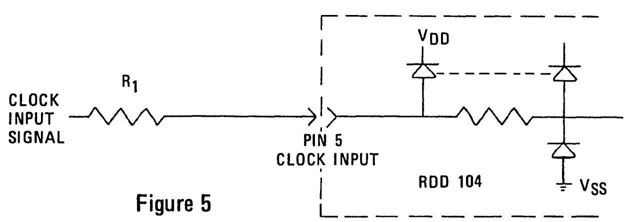


Figure 5

TYPICAL INPUT

If input signals are less than V_{SS} or greater than V_{DD}, a series input resistor, R1, should be used to limit the maximum input current to 2 milliamperes.

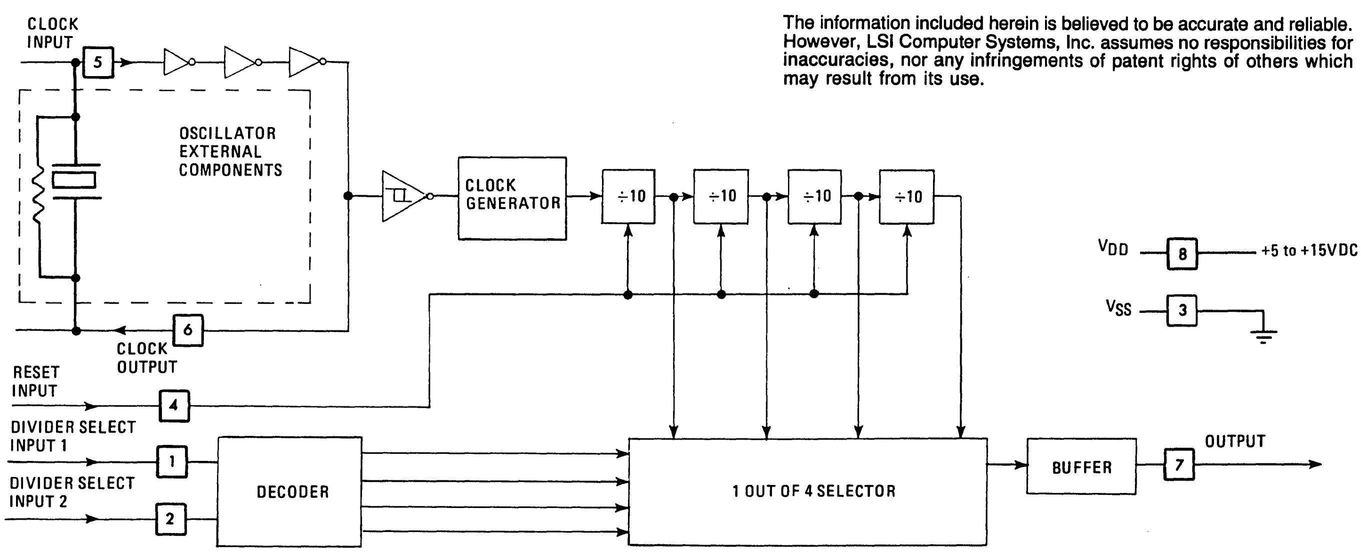


Figure 6 RDD104 BLOCK DIAGRAM

LS3404 SERIES

HIGH QUALITY MELODY CIRCUITS

FEATURES:
- Excellent Pitch Resolution
- Chime-like exponential envelope decay of each note
- Large ROM, 255 note capacity
- Wide variety of available fonts
- Mask programmable melody fonts
- Single or multiple melody capacity
- Auto-turn-off at end of play
- 4.5V to 15 Volt operation
- Low standby current
- Direct drive of PIEZO transducers
- External drive of 8Ω dynamic speakers.

CONNECTION DIAGRAM
Standard 8 Pin Plastic Mini-DIP

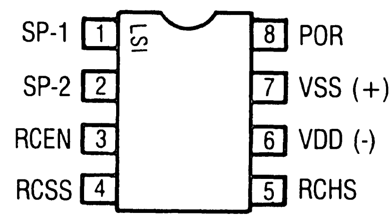


Figure 1

GENERAL DESCRIPTION:

The LS3404 Series are monolithic, Ion implanted MOS circuits designed for the generation of music. The circuit is mask programmable and can hold 255 notes in prom.

The note pitch has an 0.8% resolution for notes up to 2KHZ and 1.3% resolution for notes up to 3KHZ. The note duration ranges from 125 milliseconds for a 1/16th note to 2.0 seconds for a full note. This is equivalent to 120 beats per minute.

The duration counter allows for 8 note durations out of a possible 16 durations to be programmed in each font.

The pitch counter allows for 15 different pitches out of a possible 511 pitches to be programmed in each font.

The pitch counter output is conditioned by an external R/C envelope to provide proper envelope decay and applied to a pair of operational amplifiers which drive a piezoelectric speaker in a push-pull configuration. (See Fig. 2). Only one output is used for driving an external transistor/dynamic speaker combination in a single ended configuration. (See Fig. 3)

The exponential decay envelope imposed on each note accounts for the uniquely realistic quality of sound exhibited by the LS3404 series of circuits.

Upon application of supply VSS, the chip will start to play after a small time delay caused by power on reset. Play will be terminated either by the VSS being removed or completion of the entire play. When being terminated by End of Play (EOP), the circuit will continue to consume power at a reduced rate.

INPUT/ OUTPUT	DESCRIPTION
SP-1, SP-2	Push-pull outputs for driving Piezoelectric capacitive type speaker. Typical speaker has a 27MM diameter with equivalent capacitance of approximately 20,000 PF.
RCEN	R-C envelope input. External resistance-capacitance network for controlling the output envelope.
RCSS	R-C network for internal duration clock oscillator. The duration clock along with an internally programmed counter determines the time duration of each note. The resistance is connected to the negative supply (VDD) and the capacitance is conencted to the positive supply (VSS).
RCHS	R-C network for internal pitch clock oscillator. The pitch clock generates the audio frequency output utilizing an internally programmed counter.
VDD	Negative voltage supply
VSS	Positive voltage supply
POR	Power-on-reset-external capacitor used for initializing circuit at the application of power.

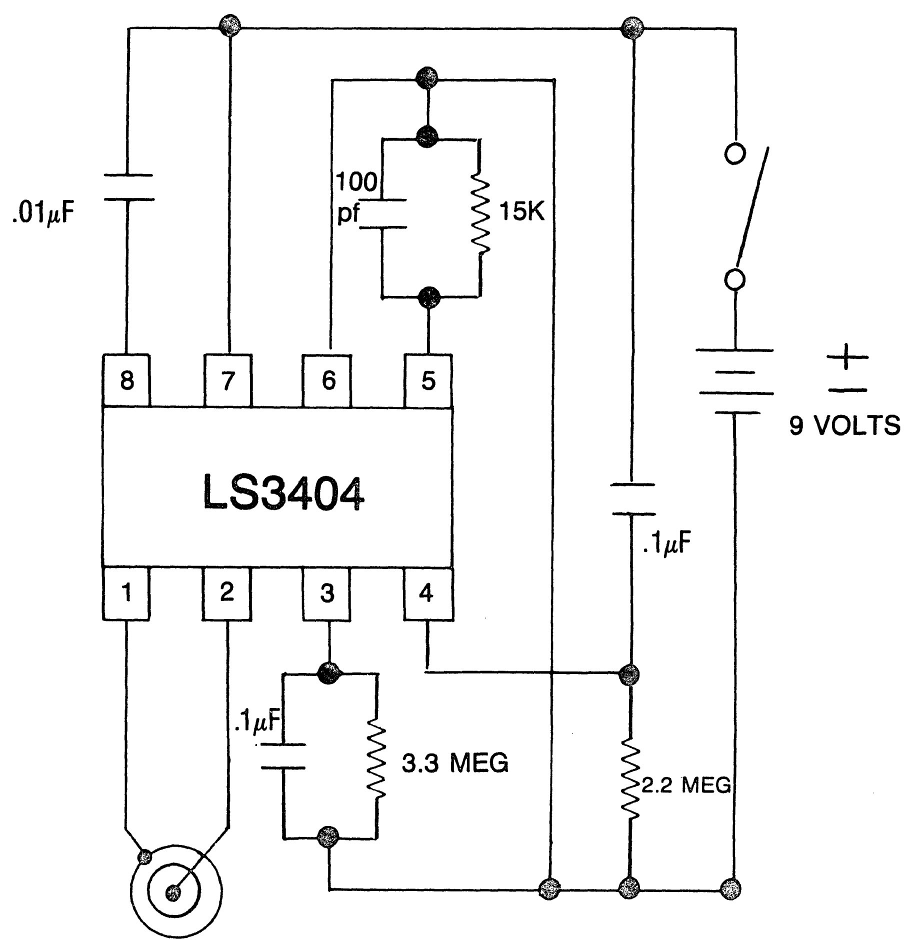


FIGURE 2

Typical Piezoelectric capacitance type speaker connection diagram.

Absolute maximum ratings (all voltages referenced to VDD)

	SYMBOL	VALUE	UNIT
DC supply voltage	VSS	+18	Volts
Voltage (any pin)	VIN	0 to VSS+ .3	Volts
Operating Temperature	TA	0 to +70	°C
Storage Temperature	Tstg	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

PAROMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS	CONDITION	
Supply Voltage	Vss	4.5		15	Volts		
Standby current At end of play	Iss			15 25	Microamperes Microamperes	VSS=6 volts VSS=10 volts	Duration Clock Resistor =2.2Meg Ω
Average operating current including Piezoelectric speaker			4 5		Milliamperes Milliamperes	VSS=6 VDC VSS=9 VDC	
Pitch clock frequency		425	500	575	KHZ	R=15KΩ C=100 pF	
Duration clock frequency			8		HZ	R=2.2 Meg Ω C=.1μF	
Duration clock frequency range		2		30	HZ		
Envelope Resistance			3.3		MEG Ω		
Envelope Capacitance			.1		μF		
Minimum POR Capacitance		.01			μF		
Speaker output peak to peak voltage		4.5 8.0			Volts Volts	Vss=6volts Vss=10volts	pitch frequency =1KHZ
Tracking of output to the envelope		-2.0 -2.5		+.4 +.4	Volts Volts	Vss=6 volts Vss=10 volts	
Composite output Peak to peak voltage		9 16			Volts Volts	Vss=6 volts Vss=10 Volts	

FONT NO.	SONG
3404-02	Christmas Medley
3404-03	"Somewhere My Love"
3404-04	"As Time Goes By"
3404-05	"Let Me Call You Sweetheart"
3404-08	"I'm In The Mood For Love"
3404-09	"Wedding March"
3404-10	"Happy Birthday I"
3404-11	"Zip-A-Dee-Doo-Dah"
3404-12	"Brahm's Lullabye"
3404-14	"Santa Claus Is Coming To Town"
3404-15	Christmas Angel Medley
3404-16	"We Wish You A Merry Christmas"
3404-17	"Walking In A Winter Wonderland"
3404-18	"Jingle Bells"
3404-19	"Joy To The World"
3404-20	"Love Makes The World Go Round"

FONT NO.	SONG
3404-21	"My Favorite Things"
3404-22	"What The World Needs Now"
3404-23	"I'd Do Anything"
3404-24	"Hail To The Chief"
3404-25	"Thanks For The Memories"
3404-26	"Gonna Fly Now" (Rocky)
3404-27	"Lazy Crazy Hazy Days of Summer"
3404-28	"For He's A Jolly Good Fellow"
3404-29	"Pomp & Circumstance"
3404-30	"More"
3404-31	"Ain't She Sweet"
3404-32	"You Are The Sunshine Of My Life"
3404-33	Nursery Rhyme Medley
3404-34	"Happy Birthday II"
3404-35	Brahms/Mozart Lullabye Medley

TABLE I
Listing of the 31 Presently Available Melodies

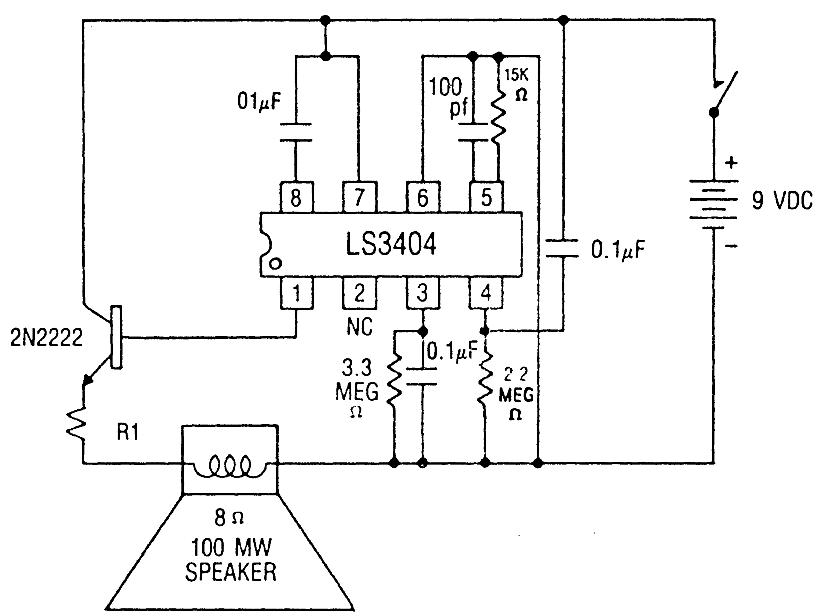


FIGURE 3

Typical 8 Ohm speaker connection. In this configuration only SP-1 is used to drive the external 8 ohm speaker in a single ended mode. Resistor R_1 is used as a volume control and can be omitted for maximum volume.

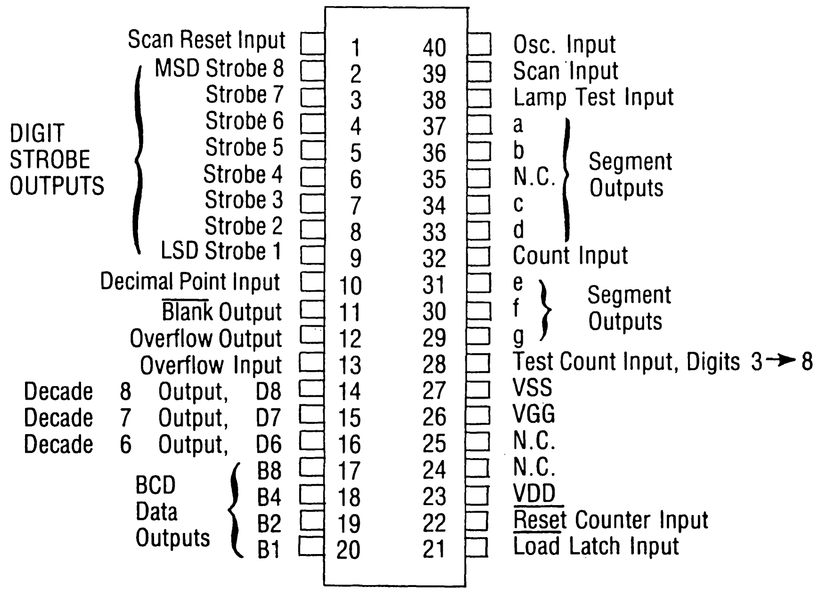
LSI/CSI

LS7030

EIGHT DECADE MULTIPLEXED MOS UP COUNTER

MARCH 1988

CONNECTION DIAGRAM:



TOP VIEW

FEATURES:

- DC to 5MHz Count Frequency
- Multiplexed BCD and 7 Segment Outputs
- DC to 500 KHz Scan Frequency
- Single Power Supply Operation, +4.75VDC to +15VDC
- Compatible with CMOS Logic
- High Input Noise Immunity
- Counter Output Latches
- Leading Zero Blanking
- Low Power Dissipation
- All Inputs Protected

DESCRIPTION:

The LS7030 is a monolithic, ion implanted, 8 decade up counter. The circuit includes latches, multiplexer, leading zero blanking, BCD and 7 segment data outputs.

OPERATING DESCRIPTION:

8 DECADE UP COUNTER

The eight decade ripple through counter increments on the negative edge of the input count pulse. Maximum ripple time is 12 μs (99999999 to 00000000). Maximum count frequency is 5MHz.

RESET

All decades are reset to zero when $\overline{\text{Reset}}$ input is brought low for minimum of 4 μs. The Overflow flip flop is reset at the same time. Reset must be high for a minimum of 1 μs before next valid count can be recorded.

LATCHES

Contents of counter are transferred to latches when $\overline{\text{Load}}$ signal is brought low for a minimum of 4 μs and kept low until a minimum of 12 μs has elapsed from previous negative edge of count pulse (ripple time). Storage of valid data occurs when Load signal is high for a minimum of 1 μs before next negative edge of count pulse or reset. Data is transferred from Overflow flip-flop to Overflow latch at the same time.

NOTE

Package Date Codes starting with "88" have a revised chip with higher count frequency specifications. These improved specifications occur under DYNAMIC ELECTRICAL CHARACTERISTICS as follows:

PARAMETER	SYMBOL	MIN	MAX	UNITS
Count and Test Count Frequency				
(VSS = + 5V ± 5%)	Fc, Ftc	DC	7.5	MHz
(VSS = + 10V)	Fc, Ftc	DC	6	MHz
(VSS = + 15V)	Fc, Ftc	DC	5	MHZ
Count Pulse Width				
(VSS = + 5V ± 5%	Tcpw	66		ns
(VSS = + 10V)	Tcpw	83		ns
(VSS = + 15V)	Tcpw	100		ns

A selected LS7030-1 offers even higher frequency operation where Fc, Ftc operate at 10 MHz (VSS = +5V ±5%), 7.5 MHz (VSS = + 10V), and 6MHz (VSS = +15V) with corresponding changes in Count Pulse Width Specifications.

The only other specification change for the revised chip occurs under SCAN OSCILLATOR as follows:

CAPACITANCE	TYPICAL OSCILLATOR FREQUENCY		
	4.75V	10V	15V
50pf	40.0 KHz	24.2 KHz	22.2 KHz
100pf	22.2 KHz	14.8 KHz	13.8 KHz
470pf	5.0 KHz	3.6 KHz	3.5 KHz
750pf	3.3 KHz	2.4 KHz	2.2 KHz
2000pf	1.3 KHz	.91 KHz	.85 KHz

SCAN OSCILLATOR AND COUNTER

The scan counter is driven by an internal oscillator whose frequency is determined by a capacitor connected between Oscillator input and Scan input. An external scan clock applied to Scan input can also drive the scan counter. Scan counter advances on negative edge of scan clock.
The counter scans from MSD to LSD. When Scan Reset input is brought high the scan counter is forced to MSD state. Internal synchronization guarantees proper scanning no matter when Scan Reset is brought low relative to scan clock. Maximum scan frequency is 500 KHz.

DIGIT STROBES

Timing of Digit Strobes is arranged such that both edges of strobe are guardbanded by a minimum 400 ns within valid BCD data when scan frequency is 100 KHz or less. The guardband is a minimum of 200 ns at 250 KHz scan frequency. At 500 KHz only negative edge of Strobe is guaranteed to be within valid BCD data by a minimum 200 ns.

DECIMAL POINT

A high at the Decimal Point input resets the Blanking Flip Flop causing the display to unblank. Decimal Point should be brought high at start of digit time which has active Decimal Point.

OVERFLOW

The Overflow flip flop sets on the first negative transition of the Overflow Input and remains set until $\overline{\text{Reset}}$ is brought low. Data is transferred from Overflow flip flop to Overflow Latch when $\overline{\text{Load}}$ is brought low. A high at the Overflow Latch causes display to unblank. Overflow Output is output of Overflow Latch. MSB outputs of Decades 6, 7, 8 are available for use as Overflow Input.

BLANKING

Leading zero blanking is employed. At start of each MSD to LSD scan, display is blanked until a nonzero digit or active decimal point is encountered. Display unblanks during LSD time and for a whole scan when Overflow output is high. When Scan Reset is applied, display blanks to prevent display damage.

Blanking information is available at $\overline{\text{Blank}}$ output and is incorporated into 7 segment information.

BCD AND 7 SEGMENT DATA

Data is available in BCD and 7 segment format. BCD data can readily be demultiplexed using Digit Strobes as latch enable signals.

POWER SUPPLIES

+4.75 volts to +15 volts single power supply operation is obtained when VGG and VDD are tied together. Inputs and outputs are CMOS compatible and Minimum Input Noise Immunity of 25% of power supply is guaranteed except for Test Count Input. (Inputs are TTL compatible at +4.75 volt to +5.25 operation.)

With VGG at −12V, VDD at 0V and VSS at +5V all inputs are TTL and CMOS compatible. All outputs are CMOS compatible and BCD and $\overline{\text{BLANK}}$ outputs also provide standard TTL compatibility. In addition, Overflow Output is low power TTL compatible.
In either mode outputs swing between VDD and VSS.

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
Storage Temperature	Tstg	−65 to +150	°C
Operating Temperature	Ta	−25 to +70	°C
Voltage (any pin to VSS)	Vmax	−30 to +0.5	V

DC ELECTRICAL CHARACTERISTICS:

(VDD = VGG = 0V, VSS = +4.75 to +15V, −25°C ≤ Ta ≤ +70°C unless otherwise specified.)

	PARAMETER	SYMBOL	MIN	MAX	UNITS
	Operating Supply Current (@ Fc = 5MHz)	Idds		15	mA
	Input Noise Immunity Low and High	Vni	25% (VSS-VDD)		V
	Test Count Input	Vil	VSS-20	VSS-3.95	V
		Vih	VSS-1.0	VSS	V
D6, D7, D8 OF, BCD, $\overline{\text{Blank}}$ (See Note 1)	Output Voltage "0"	Vol		+0.2	V
	Output Voltage "1"	Voh	VSS-1.0		V
Segment and Strobe Outputs (See Note 2)	Output Voltage "0" (sinking 10 uA)	Vol		+0.5	V
	Output Current "1"				
	VSS=+4.75 (Voh=VSS−0.5V)		0.05		mA
	(Voh=VSS−1V)		0.25		mA
	(Voh=VSS−4V)		0.90		mA
	VSS=+10V (Voh=VSS−2V)		2.0		mA
	(Voh=VSS−3V)		3.0		mA
	VSS=+15V (Voh=VSS−2V)		3.0		mA
	(Voh=VSS−3V)		4.5		mA

Note 1: Current Sink = Same as segment and strobe outputs.
Current Source = N/A at Voh = VSS−.5V for VSS =+4.75V
35μA at Voh = VSS−1V for VSS = +4.75V
40% of segment and strobe outputs at all other specified operating points.

Note 2: Limit segment current to 4.5mA maximum.
Limit strobe current to 6mA maximum.

Note: The following inputs have internal pull down resistors to VDD with maximum sink current of 5 μA at VSS input.

Scan Reset	Test Count
Decimal Point	Count
Overflow	Lamp Test

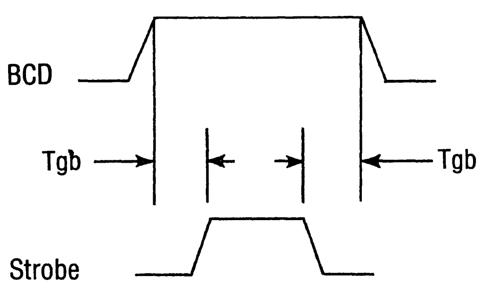
DYNAMIC ELECTRICAL CHARACTERISTICS:

(VDD = VGG = 0V, VSS = +4.75 to+15V, −25°C ≤ Ta ≤ +70°C unless otherwise specified.)

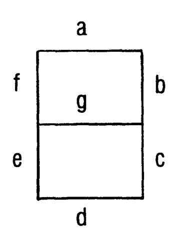
PARAMETER	SYMBOL	MIN	MAX	UNITS
Count and Test Count Frequency	Fc, Ftc	DC	5	MHz
Scan Frequency	Fsc	DC	500	KHz
Count Pulse Width	Tcpw	100		ns
Count Ripple Time	Tcr		12	μs
$\overline{\text{Load}}$ Pulse Width	Tlpw	4		μs
$\overline{\text{Load}}$ Removal Time	Tlr		1	μs
$\overline{\text{Reset}}$ Pulse Width	Trpw	4		μs
$\overline{\text{Reset}}$ Removal Time	Trr		1	μs
Rise and Fall Time				
Count Pulse	**Trfc**		4	μs
Reset Pulse	**Trfr**		4	μs
Test Count Pulse	**Trftc**		80	μs
*Strobe Guard Band Time (Fsc ≤100 kHz)	Tgb	400		ns
*Strobe Guard Band Time (100 kHz ≤Fsc ≤250 kHz)	Tgb	200		ns
*Strobe Guard Band Time (250 kHz ≤Fsc ≤ 500 kHz) negative edge only	Tgb	200		ns

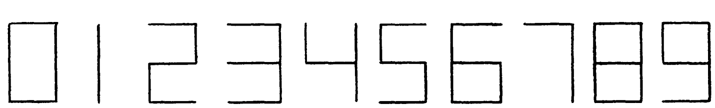
*Defines the minimum time from strobe edges to switching BCD data.

Guardbanded Strobe



Seven Segment Font





SCAN OSCILLATOR:

CAPACITANCE	TYPICAL OSCILLATOR FREQUENC		
	4.75V	10V	15V
50pf	72.8KHz	69.6KHz	76.0KHz
100 pf	48.0KHz	45.6KHz	48.0KHz
470pf	12.0KHz	12.0KHz	14.4KHz
750 pf	9.6KHz	8.8KHz	10.4KHz

TTL COMPATIBLE OUTPUTS:

Power Supplies: VSS = +5V ±5%
VDD = 0V
VGG = −12V ±5%

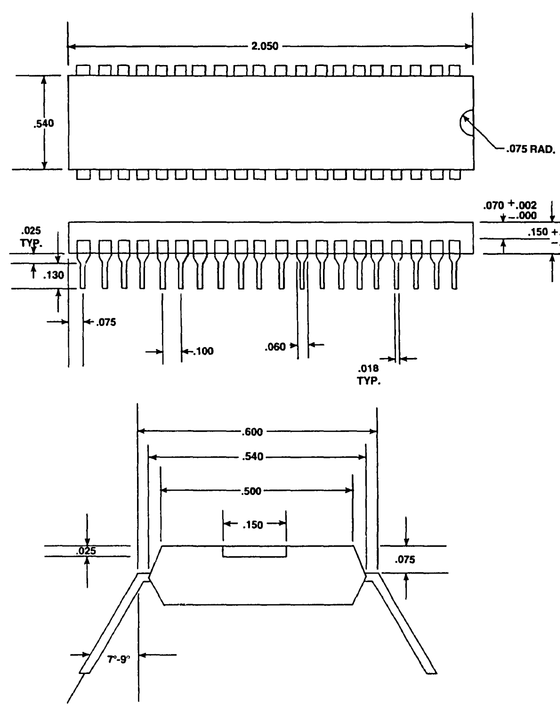
Output Levels:

"1" level ≥ VSS−.5V (sourcing 100 μA)
"0" level ≤ 0.4V (sinking 1.6mA)
} $\overline{\text{BLANK}}$ AND BCD DATA OUTPUTS

"1" level ≥ VSS−.5V (sourcing 40μA)
"0" level ≤ 0.4V (sinking .18mA)
} OVERFLOW OUTPUT

All other outputs as specified for single power supply, VSS = +15V, operation. Inputs as specified for single power supply, VSS = +5V ±5% operation.

PACKAGE DIAGRAM:



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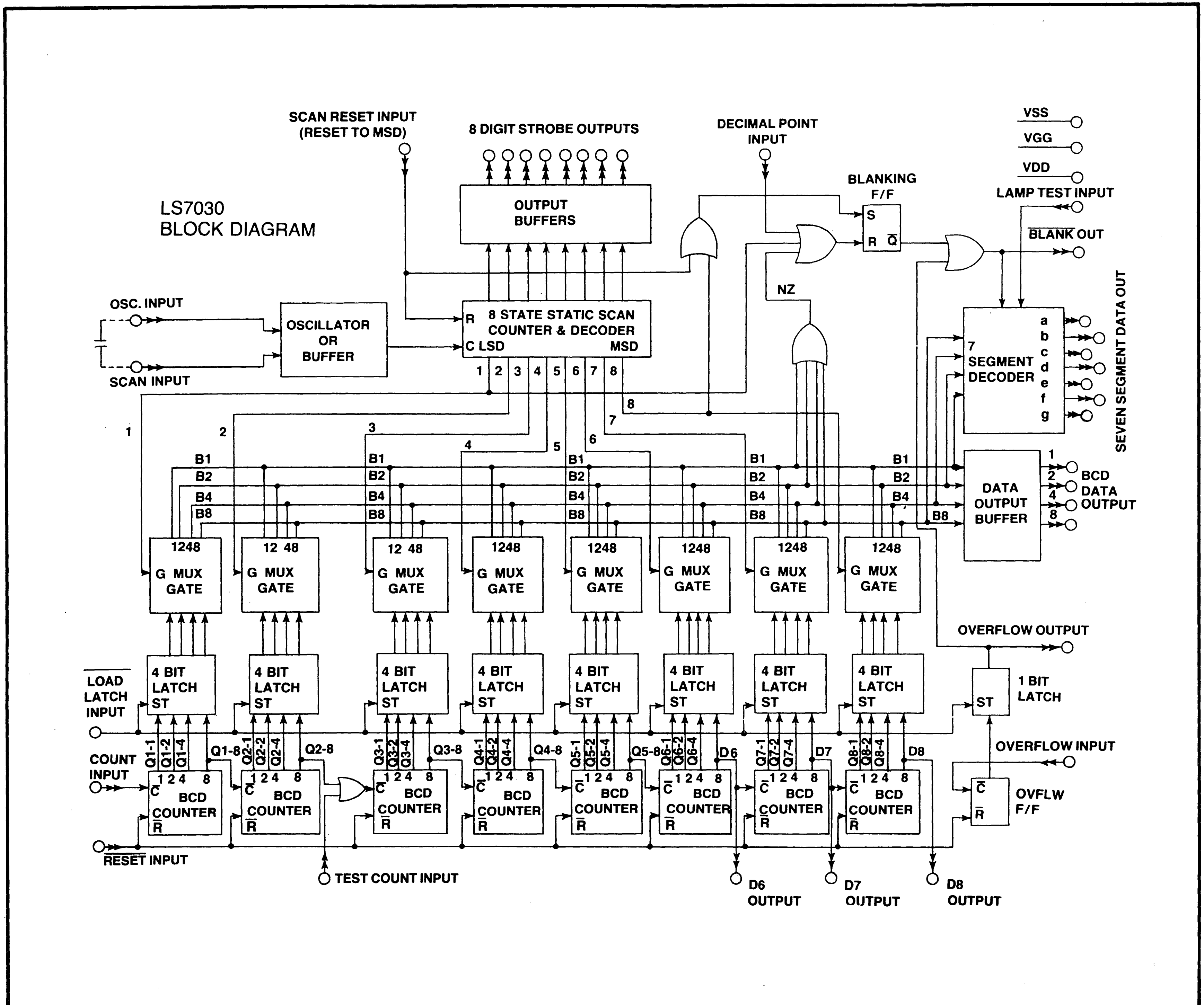


LSI/CSI

LS7031

6 DECADE MOS UP COUNTER WITH 8 DECADE LATCH AND MULTIPLEXER

Revised March 1988

FEATURES:

- DC to 7.5MHz Count Frequency
- Multiplexed BCD Outputs
- DC to 500KHz Scan Frequency
- Ability to Latch External BCD Data in the Two LSD Positions
- Leading Zero Blanking with Decimal Point and Overflow Controls
- Single Power Supply Operation, +4.75VDC to +15VDC
- Compatible with CMOS Logic
- High Input Noise Immunity
- Low Power Dissipation
- All Inputs Protected

DESCRIPTION:

The LS7031 is a monolithic, ion implanted MOS 6 decade up counter. The circuit includes latches, multiplexer, leading zero blanking and BCD data outputs.

DESCRIPTION OF OPERATION:

CLOCK GENERATOR:

The clock for the six decade counter (digit positions 3-8) is formed from the internal 'OR' combination of B4/D2 and B8/D2 if LS7031 is used with external prescaling counters. When operated in this fashion the maximum allowable propagation delay between B4/D2 (H−L) and B8/D2 (L−H), measured at VSS-1.0V, is 10ns. If used as a straight six decade counter, clock pulses may be applied to inputs B4/D2 or B8/D2 with the unused input held low. In either mode of operation total pulse width must be minimum 62 ns. See Block Diagram.

6 DECADE UP COUNTER

The six decade ripple through counter increments on the negative edge of the internal clock. Maximum ripple time is 12μs (999999 to 000000). Maximum count frequency is 7.5MHz.

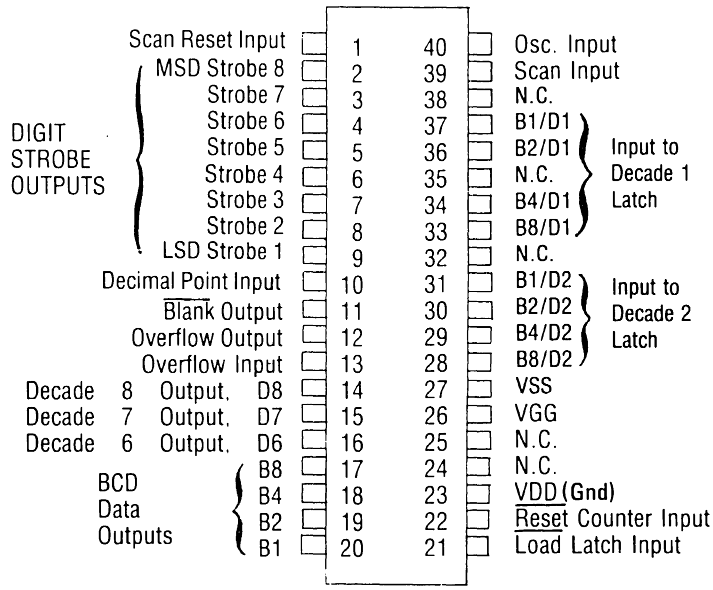
RESET

All 6 counter decades are reset to zero when $\overline{\text{Reset}}$ is brought low for minimum of 4μs. The Overflow flip flop is reset at the same time. $\overline{\text{Reset}}$ must be high for a minimum of 1μs before next valid count can be recorded.

LATCHES

8 decades of latch are provided, two for storage of the two external least significant decade counters and the remaining 6 for internal counter outputs. All latches are loaded when $\overline{\text{Load}}$ signal is brought

CONNECTION DIAGRAM:



TOP VIEW

NOTE

The LS7031-1 is a selected higher count frequency version of the LS7031. The specification differences occur under DYNAMIC ELECTRICAL CHARACTERISTICS as follows:

PARAMETER	SYMBOL	MIN	MAX	UNITS
Count Frequency				
(VSS = + 5V ± 5%)	Fc	DC	10	MHz
(VSS = + 10V)	Fc	DC	7.5	MHz
(VSS = + 15V)	Fc	DC	6	MHZ
Count Pulse Width ((Pulse applied to B4/D2 or B8/D2; 'OR' combination of B4/D2 and B8/D2)				
(VSS = + 5V ± 5%	Tcpw	50		ns
(VSS = + 10V)	Tcpw	62		ns
(VSS = + 15V)	Tcpw	83		ns

Other specifications are unchanged.

low for a minimum of 4 μs and kept low until a minimum of 12 μs has elapsed from previous negative edge of count pulse (ripple time). Storage of valid data occurs when $\overline{\text{Load}}$ signal is high for a minimum of 1 μs before next negative edge of count pulse or reset. Data is transferred from Overflow flip flop to Overflow latch at the same time.

SCAN OSCILLATOR AND COUNTER

The scan counter is driven by an internal oscillator whose frequency is determined by a capacitor connected between Oscillator input and Scan input. An external scan clock applied to Scan input can also drive the scan counter. Scan counter advances on negative edge of scan clock.

The counter scans from MSD to LSD. When Scan Reset input is brought high the scan counter is forced to MSD state. Internal synchronization guarantees proper scanning no matter when Scan Reset is brought low relative to scan clock. Maximum scan frequency is 500 kHz.

DIGIT STROBES

Timing of Digit Strobes is arranged such that both edges of strobe are guardbanded by a minimum 400 ns within valid BCD data when scan frequency is 100 kHz or less. The guardband is a minimum of 200 ns at 250 kHz scan frequency. At 500 kHz only negative edge of Strobe is guaranteed to be within valid BCD data by a minimum 200 ns.

DECIMAL POINT:

A high at the Decimal Point input resets the Blanking Flip Flop causing the display to unblank. Decimal Point should be brought high at start of digit time which has active Decimal Point.

OVERFLOW

The Overflow flip flop sets on the first negative transition of the Overflow Input and remains set until $\overline{\text{Reset}}$ is brought low. Data is transferred from Overflow flip flop to Overflow Latch when $\overline{\text{Load}}$ is brought low. A high at the Overflow latch causes display to unblank. Overflow Output is output of Overflow Latch. MSB outputs of Decades 6, 7, 8 are available for use as Overflow Input.

BLANKING

Leading zero blanking is employed. At start of each MSD to LSD scan, display is blanked until a non zero digit or active decimal point is encountered. Display unblanks during LSD time and whenever Overflow output is high. When Scan Reset is applied, display blanks to prevent display damage.

Blanking information is available at $\overline{\text{Blank}}$ output.

BCD DATA

Data is available in multiplexed BCD format. BCD data can readily be demultiplexed using Digit Strobes as latch enable signals.

POWER SUPPLIES

+4.75 volt to +15 volt single power supply operation is obtained when VGG and VDD are tied together. Inputs and outputs are CMOS compatible. Minimum Input Noise Immunity of 25% of Power Supply is guaranteed for all inputs except Decade 1 and Decade 2 inputs (all inputs are TTL compatible at +4.75 volt to +5.25 volt operation.)

With VGG at −12V, VDD at 0V and VSS at +5V all inputs are TTL and CMOS compatible. All outputs are CMOS compatible, and BCD and $\overline{\text{Blank}}$ outputs also provide standard TTL compatibility. In addition, Overflow Output is low power TTL compatible.

In either mode outputs swing between VDD and VSS.

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
Storage Temperature	Tstg	−65 to +150	°C
Operating Temperature	Ta	−25 to +70	°C
Voltage (any pin to VSS)	Vmax	−30 to +0.5	V

DC ELECTRICAL CHARACTERISTICS:

(VDD = VGG = 0V, VSS = +4.75 to +15V, −25°C ≤ Ta ≤ +70°C unless otherwise specified.)

	PARAMETER	SYMBOL	MIN	MAX	UNITS
	Operating Supply Current (@ Fc = 7.5 MHz)	Idds		15	mA
	Input Noise Immunity Low and High	Vni	25% (VSS-VDD)		V
EXTERNAL DECADE INPUTS	Input Voltage "0"	Vil	VSS-20	VSS-3.95	V
	Input Voltage "1"	Vih	VSS-1.0	VSS	V
D6, D7, D8, OF, BCD, $\overline{\text{BLANK}}$ (See Note 1)	Output Voltage "0"	Vol		+0.2	V
	Output Voltage "1"	Voh	VSS-1.0		V
STROBE OUTPUTS (See Note 2)	Output Voltage "0" (sinking 10 uA)	Vol		+0.5	V
	Output Current "1"				
	VSS = +4.75V (Voh = VSS–0.5V)		0.05		mA
	(Voh = VSS–1V)		0.25		mA
	(Voh = VSS–4V)		0.90		mA
	VSS = +10V (Voh = VSS–2V)		2.0		mA
	(Voh = VSS–3V)		3.0		mA
	VSS = +15V (Voh = VSS–2V)		3.0		mA
	(Voh = VSS–3V)		4.5		mA

Note 1: Current Sink = Same as strobe outputs.
Current Source = N/A at Voh = VSS–.5 for VSS = +4.75V
35μA at Voh = VSS–1V for VSS = +4.75V
40% of strobe outputs at all other specified operating points.

Note 2: Limit strobe current to 6mA maximum.

Note: The following inputs have internal pull down resistors to VDD with maximum sink current of 5 μA, when the input is at VSS.

Scan Reset	B1/D1	B1/D2
Decimal Point	B2/D1	B2/D2
Overflow	B4/D1	B4/D2
	B8/D1	B8/D2

TTL COMPATIBLE OUTPUTS:

Power Supplies:

VGG=–12V±5%. VDD=0V, VSS=+5V ±5%

Output Levels:

Output "One" ≥ VSS–.5V (sourcing 100 μA)
Output "Zero" ≤ 0.4V (sinking 1.6mA) } $\overline{\text{BLANK}}$ AND BCD DATA OUTPUT

Output "One" ≥ VSS–.5V (sourcing 40 μA)
Output "Zero" ≤ 0.4V (sinking, .18mA) } OVERFLOW OUTPUT

All other outputs as specified for single power supply, VSS = +15V, operation. Inputs as specified for single power supply, VSS = +5V ±5% operation.

DYNAMIC ELECTRICAL CHARACTERISTICS:

(VDD = VGG = 0V, VSS = +4.75 to +15V, −25°C ≤ Ta ≤ +70°C unless otherwise specified.)

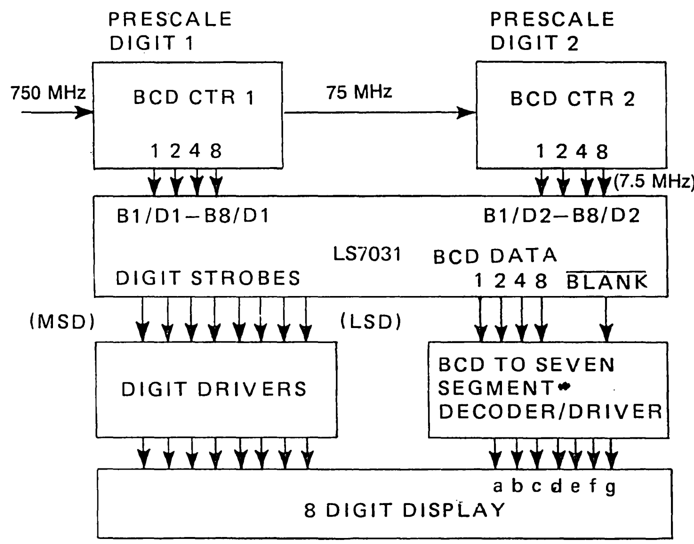
PARAMETER	SYMBOL	MIN	MAX	UNITS
Count Frequency				
(VSS = + 5V ± 5%)	Fc	DC	7.5	MHz
(VSS = + 10V)	Fc	DC	6	MHz
(VSS = + 15V)	Fc	DC	5	MHZ
Scan Frequency	Fsc	DC	500	KHz
Count Pulse Width ((Pulse applied to B4/D2 or B8/D2; 'OR' combination of B4/D2 and B8/D2)				
(VSS = + 5V ± 5%	Tcpw	62		ns
(VSS = + 10V)	Tcpw	83		ns
(VSS = + 15V)	Tcpw	100		ns
** Propagation Delay (B4/D2(H-L)toB8/D2 (L-H)at VSS-1.0V)	Tpr	Overlap	10	ns
Count Ripple Time	Tcr		12	µs
Load Pulse Width	Tlpw	4		µs
Load Removal Time	Tlr		1	µs
Reset Pulse Width	Trpw	4		µs
Reset Removal Time	Trr		1	µs
* Strobe Guard Band Time (Fsc ≤ 100 kHz)	Tgb	400		ns
* Strobe Guard Band Time (100 kHz ≤ Fsc ≤ 250 kHz)	Tgb	200		ns
* Strobe Guard Band Time (250 kHz ≤ Fsc ≤ 500 kHz) negative edge only	Tgb	200		ns

* Defines the minimum time from strobe edges to switching BCD data.

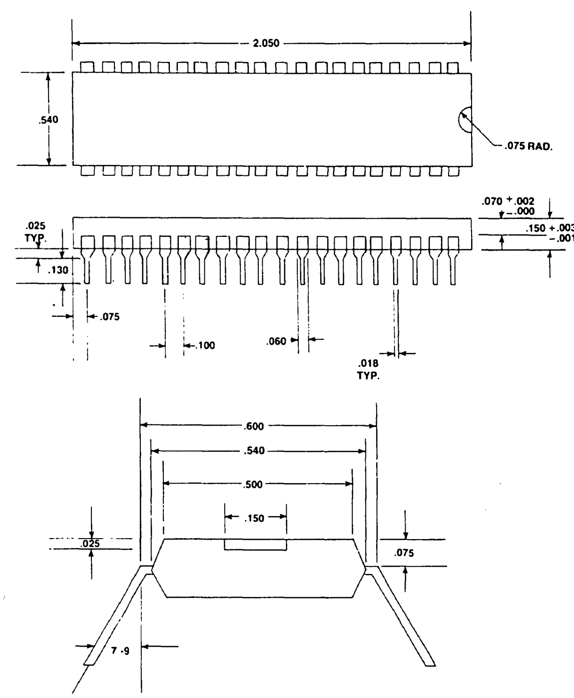
SCAN OSCILLATOR:

CAPACITANCE	TYPICAL OSCILLATOR FREQUENCY 4.75V	10V	15V
50pf	40.0KHz	24.2KHz	22.2KHz
100pf	22.2KHz	14.8KHz	13.8KHz
470pf	5.0KHz	3.6KHz	3.5KHz
750pf	3.3KHz	2.4KHz	2.2KHz
2000pf	1.3KHz	.91KHz	.85KHz

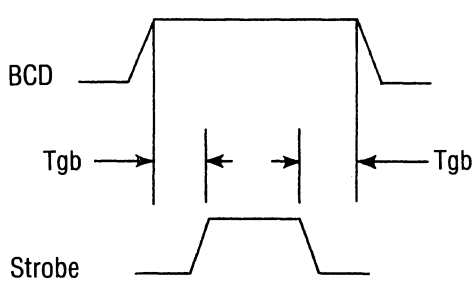
TYPICAL APPLICATION



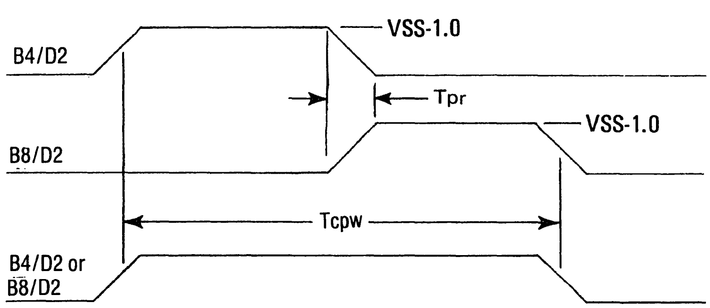
PACKAGE DIAGRAM:



Guardbanded Strobe



*Propagation Delay and Pulse Width



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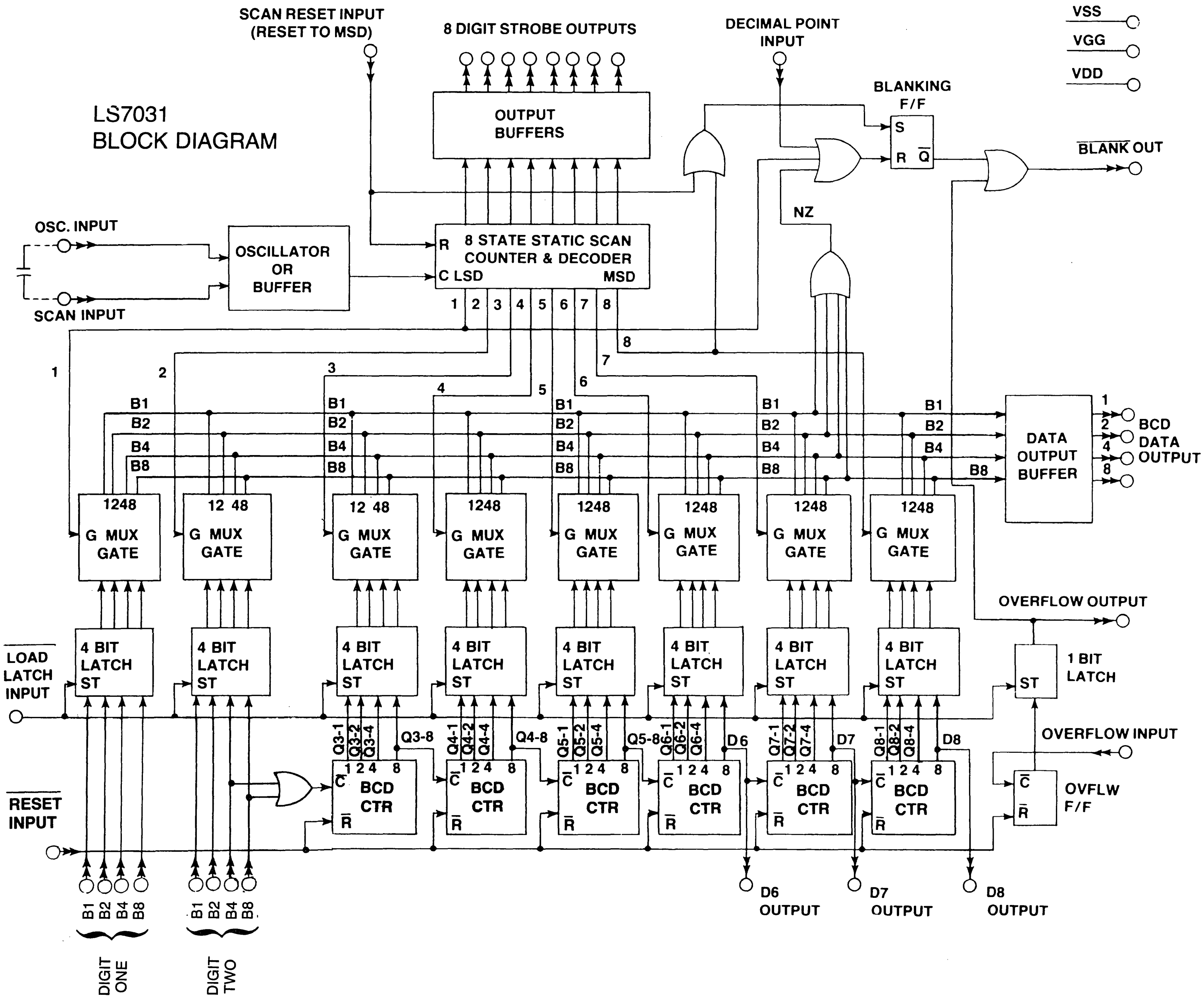
LS7031
BLOCK DIAGRAM



LSI/CSI

LS 7040

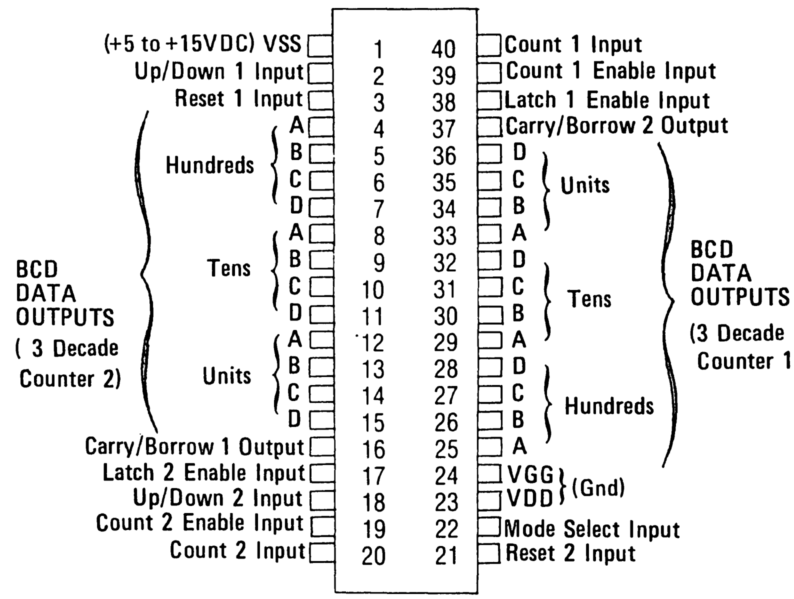
MARCH 1987

DUAL 3 DECADE UP/DOWN COUNTER

FEATURES:

- DC to 350 KHz Count Frequency at +5V Operation
- Fully Synchronous Operation
- Cascadable
- Inputs CMOS, TTL, and DTL Compatible at +5V Operation
- Separate Low Current Drain Power Supply for Counter Stages Permits Battery Stand-by Operation
- Reset
- Count Enable
- Parallel BCD Output Data
- Power-on-Reset
- Count Input Applied to a Regenerative Circuit which Permits Infinite Rise and Fall Times
- Selectable as 6 Decade or Dual 3 Decade Up or Down Counter
- CMOS Type Noise Immunity on all Inputs
- Output Latches
- Single Power Supply Operation, +5VDC to +15VDC

CONNECTION DIAGRAM: TOP VIEW
STANDARD 40 PIN PLASTIC DIP



TOP VIEW

DESCRIPTION:

The LS7040 is a monolithic ion implanted PMOS synchronous Dual 3 Decade or 6 Decade Up/Down Counter including latches and parallel BCD data outputs.

DESCRIPTION OF OPERATION:

UP/DOWN Circuit can be operated as a 6 decade Up or Down counter, a dual 3 decade Up or Down counter, or in a mode where one 3 decade counter counts up and the other counts down. A high input causes counter to operate in the Up mode. A low input (or N/C) causes the counter to operate in the Down mode.

COUNT Counter will operate at speeds up to 350kHz and advances on the negative edge of the input count pulse. When using as a synchronous 6 decade counter, Count 1 and Count 2 must be tied together and must have fast rise and fall times, i.e. 50 μsec max. When using as an asynchronous counter, the input count pulse is applied to the Count 1 Input and the Carry/Borrow 1 output is applied to the Count 2 Input. In this mode, the input count pulse can have an infinite rise and fall time. Refer to Figures 2 through 4 for synchronous and asynchronous counter operation.

RESET A high input will hold all counter stages at zero. When using as a 6 decade counter, Reset 1 and Reset 2 must be tied together.

COUNT ENABLE A high input will permit counting. A low input will inhibit counting and the counter will remain at its last count. When using as a 6 decade counter, Count 1 Enable and Count 2 Enable must be tied together. See Figures 2 through 4.

LATCH ENABLE A high input will cause information present in the counter to be transmitted through the latch. A low input prevents updating of the latches as the counter advances. When using as a 6 decade counter, Latch 1 Enable and Latch 2 Enable must be tied together.

MODE SELECT When input is low (or N/C), the counter becomes a dual 3 decade counter. In this mode of operation the counter can be hooked up as an asynchronous 6 decade counter. A high input causes the counter to operate as a synchronous 6 decade counter.

BCD DATA All 24 BCD data bits stored in the latches are brought out in parallel.

CARRY/BORROW As a Dual 3 Decade Up Counter, Carry signals are positive outputs lasting for one clock period that occur when a count of 999 is reached. Each output is capable of driving another 7040 counter directly. When used as a synchronous 6 decade Up Counter, Carry 2 will be the output Carry and will occur when a count of 999999 is reached while Carry 1 is internally routed into decade 4. As a Dual 3 Decade Down Counter, Borrow Outputs occur when a count of 000 is reached. As a synchronous 6 Decade Down Counter, Borrow 2 will occur when a count of 000000 is reached. When cascading synchronous 6 Decade Counters, Carry/Borrow 2 of the first counter is applied to the Count 1 Enable and Count 2 Enable of the second counter . In this case the count inputs of both counters must be tied together. This arrangement enables fully synchronous operation.

When cascading asynchronous counters, Carry/Borrow 2 of the first counter is applied to Count 1 of the second counter. To Enable counting, Count 1 Enable and Count 2 Enable must be high (VSS).

POWER SUPPLIES The circuit will operate over the range of +5V to +15V. VGG is the supply for all the peripheral circuitry. VDD is the supply for the low current drain counter chain. This is done to facilitate battery stand-by for VDD during a power supply outage condition. (See Figures 5 and 6). During this condition the circuit will continue to count and generate output carry signals. The BCD outputs will not be available and the latch will be inoperative.

POWER-ON-RESET A Power-On-Reset circuit enables the counter to initialize at a count of 000000 when power is first applied.

NOTE: The following inputs have internal pull down resistors to VDD with maximum sink current of 20 μA at VSS input.

Up/Down 1
Up/Down 2
Mode Select

TECHNICAL DATA

Input Specification-With VSS=+15V and VDD=VGG=0V inputs will be High Threshold Logic and CMOS compatible. With VSS=+5V inputs will be TTL, DTL, and CMOS compatible. (TTL and DTL inputs require +3.5 volts logic 1 input).

Outputs - Will be CMOS compatible over entire range of power supply voltage limits.

Logic - Positive true.

Package - 40 pin Dual-In-Line.

MAXIMUM RATINGS:

Parameter	Symbol	Value	Units
Storage Temperature	Tstg	-65 to +150	°C
Operating Temperature	Ta	-25 to +70	°C
Voltage (any pin to VSS)	Vmax	-30 to +.5	V

DC ELECTRICAL CHARACTERISTICS

(VDD = VGG = 0V, VSS = +5V to +15V, -25°C ≤ Ta ≤ +70°C Unless otherwise specified).

Parameter	Symbol	Min.	Max.	Units
Quiescent Supply Current (VSS = +5V)	Idd Igg		2.5 4.5	mA mA
Quiescent Supply Current (VSS = +9V)	Idd Igg		3.0 7.0	mA mA
Quiescent Supply Current (VSS = +15V)	Idd Igg		4.0 11.0	mA mA
Input Capacitance All Inputs	Cin		10	pf
Noise Immunity All Inputs	Vnl Vnh	30%(VSS-VDD) 30%(VSS-VDD)		Volts Volts
Output Levels All Outputs	Vol Voh	 VSS-1	+0.5	Volts Volts

AC ELECTRICAL CHARACTERISTICS

(VDD=VGG=0V, VSS= +5V to +15V, −25°C ≤ Ta ≤+70°C unless otherwise specified).

Parameter	Symbol	Min.	Max.	Units
Count Input Frequency (For Data Outputs) VSS = +5V, 3 Decade	Fc	DC	350	kHz
VSS = +5V, Synchronous 6 Decade	Fc	DC	250	kHz
VSS = +15V, 3 Decade	Fc	DC	250	kHz
VSS= +15V,Synchronous 6 Decade	Fc	DC	175	kHz
Count Input Pulse width (negative Pulse) VSS = +5V	Tcpw	1.5		μs
VSS = +15V	Tcpw	2.5		μs
Count Input Rise and Fall Fall Time				
Asynchronous Counting			No Limit	
Synchronous Counting			50	μs

AC ELECTRICAL CHARACTERISTICS (Cont'd)

Parameter	Symbol	Min.	Max.	Units
Reset Pulse Width	Trpw	4.0		μs
Count Enable Set Up Time	Tces*	2.0		μs
Count Enable Hold Time	Tceh*	2.5		μs
Count Input to Latch Enable Set Up Time	Tcls	4.0		μs
Latch Enable Pulse Width	Tlpw	2.0		μs
Up/Down Set Up Time	Tuds*	2.0		μs
Up/Down Hold Time (See Note 1)	Tudhl*	7.0		μs
	Tudht**	2.5		μs
Propagation Delay (CL = 15 pF)				
Data Output	Tdd*		4.5	μs
Carry Output	Tcd*		5.5	μs

* With respect to count input leading negative edge.

** With respect to count input trailing positive edge.

Note 1: Tudht may be used instead of Tudhl at high frequencies where the Count Input negative pulse width is less than 4.5 μsec. If the pulse width is greater than 4.5μsec., Tudhl must be used.

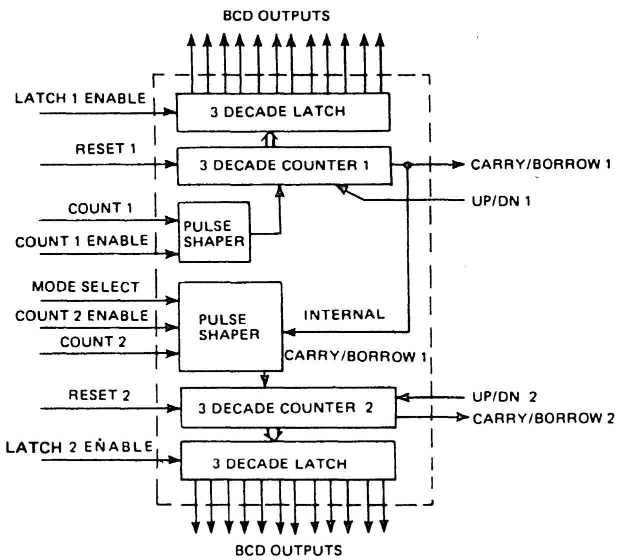


FIGURE 1 – LS7040 BLOCK DIAGRAM

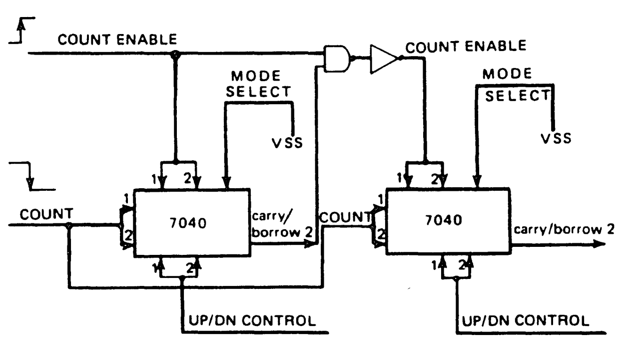


FIGURE 2 – SYNCHRONOUS 12 DECADE COUNTER

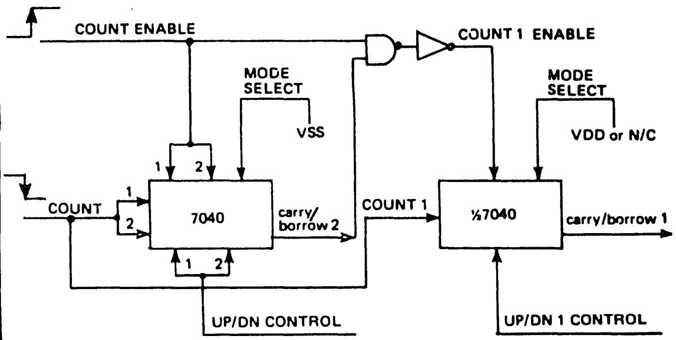


FIGURE 3 – SYNCHRONOUS 9 DECADE COUNTER

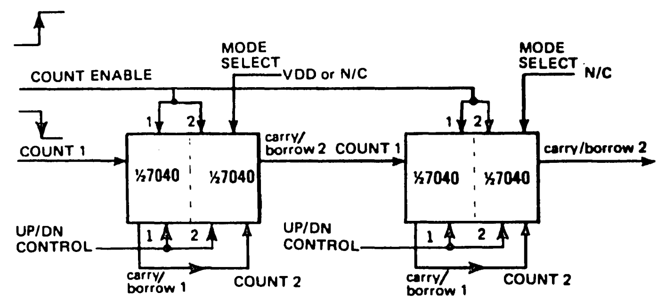
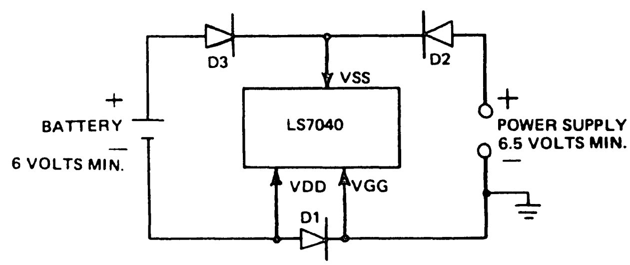


FIGURE 4 – ASYNCHRONOUS 12 DECADE COUNTER

BATTERY STAND-BY SCHEMATICS



Positive Supply System The battery voltage is lower than the supply voltage and is used only in the Power Outage Condition for counting. When the power supply is shut off, the battery supplies current only through VDD. Diode D1 is used to isolate VDD and VGG. Diode D2 is used to prevent VSS from going to ground potential when the power supply shuts off. Diode D3 is used to isolate the battery and the power supply.

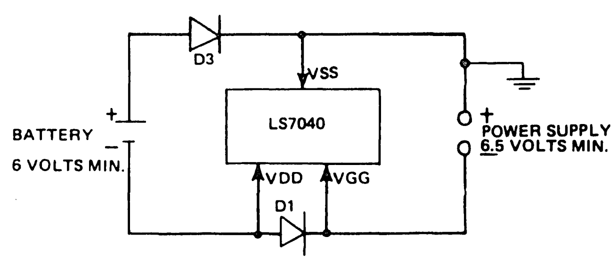


FIGURE 6

Negative Supply System Diode D2 is not needed since VGG going to ground potential will not affect standby operation.

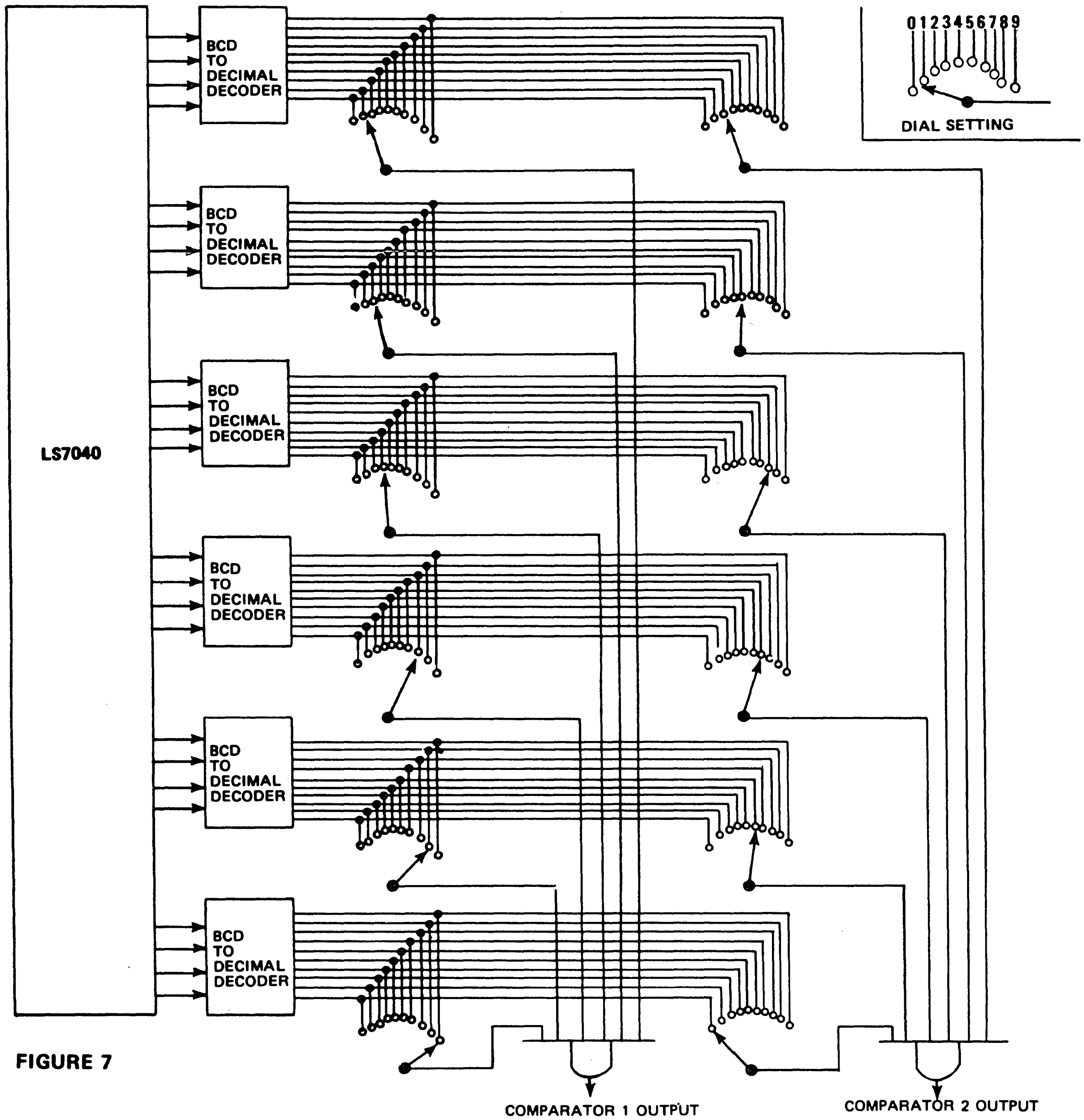


FIGURE 7

APPLICATION NOTE:

The unique feature of the LS7040, and its main advantage over multiplexed counters, is its parallel BCD outputs. These outputs can be applied to as many external preset comparators as desired with a minimum of hardware. Figure 7 illustrates the circuitry for two 6 digit comparators. A BCD to Decimal decoder and a 10 position switch is used for each of the decade outputs. The arms of the 6 switches are combined in an And gate to provide the comparison output. The desired decimal number is selected and the And gate produces a Logic 1 output when the LS7040 reaches that number. For each additional comparator, six 10 position switches and one And gate are added. There is no limit to the number of comparators that can be used with one LS7040 and 6 BCD to decimal decoders. Counter outputs can be displayed by applying the BCD outputs to a 7 segment decoder to drive LED displays.

Because of the cascadability of the LS7040, a 12 digit comparator scheme would use 2 LS7040's and 12 BCD to decade decoders. This scheme can be extended to as many digits as desired.

Figure 7 depicts an output occuring at comparator 1 when the LS7040 reaches a count of 123789. Comparator 2 will produce an output at a count of 247650

An additional advantage of the LS7040 over multiplexed counter outputs occurs when analog circuits and counter circuits are being used together. The demultiplexing signals and associated hardware that are used by a multiplex counter can cause noise to interfere with analog signals. The use of the LS7040 in an analog application will negate the possibility of any noise generation.

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LS7055/LS7056 | 6 DECADE PREDETERMINING UP/DOWN COUNTER

(with 3 presettable storage registers)

REVISED DECEMBER 1985

FEATURES:

- **Single Power Supply Operation +4.75 to +15 Volts**
- **Integral Preset, Presignal and Mainsignal Store**
- **DC to 250KHz Count Frequency**
- Fully Synchronous Operation
  Three Comparators with Output Flags
  Automatic or Manual Preset/Reset Control
- Thumbwheel Interface for Storage Selects
- Prescale on Count Input Selectable
- Count Inhibit
- Up/Down Control
- Scan Rate up to 150KHz
- Scan Oscillator has Override Capability
- Blanking Override for Decimal Point Operation
- Multiplexed 7 Segment and BCD Data Output
- Output Latches
- Reset
- Hysteresis Circuit on Count Input
- CMOS Type Noise Immunity on all other inputs
- Pull Down Resistors on BCD inputs

DESCRIPTION:

The LS7055/LS7056 is a monolithic, ion implanted MOS synchronous 6 decade up/down counter. The circuit includes storages and comparators, zero detect, automatic presetting and resetting, output latches, multiplexed output BCD and seven segment data. Thumbwheel switches can be used to provide BCD data to the storage networks in the circuit.

DESCRIPTION OF OPERATION:

COUNT:

Counter will operate at speeds up to 250 KHz and will advance on the positive edge of the input count pulse.

UP/DOWN:

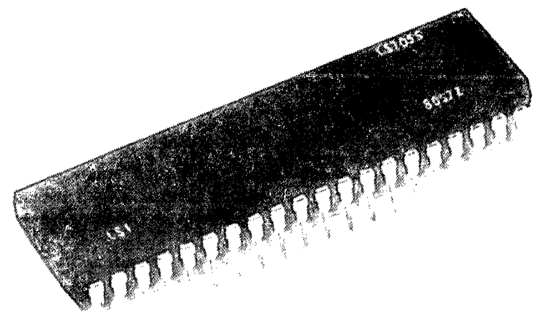
Counter can operate in either the up mode or the down mode. A high input will cause the counter to operate in the up mode while a low input will cause it to operate in the down mode.

COUNT INHIBIT:

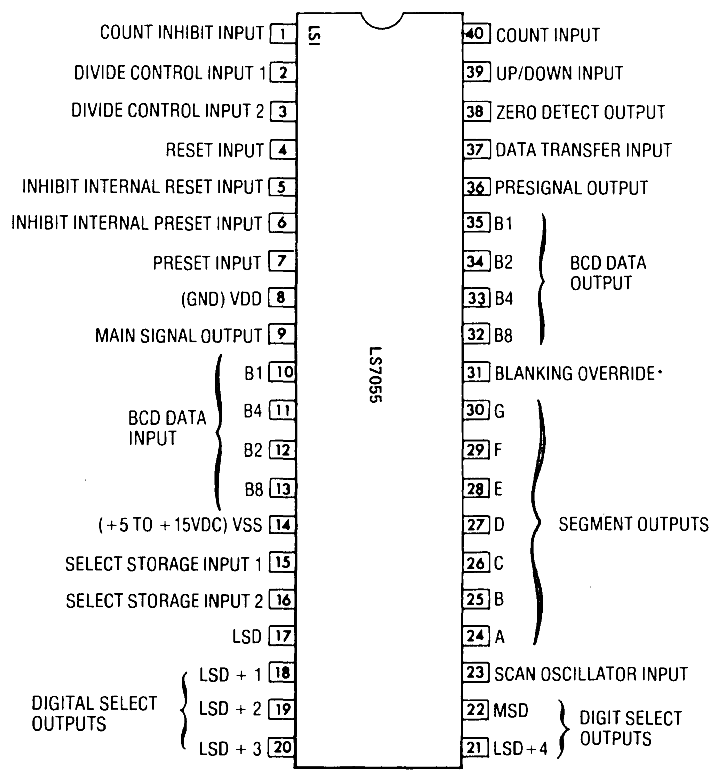
A high input will inhibit counting and the counter will remain at its last count. A low input will enable counting.

DATA TRANSFER INPUT:

A high input will allow the seven segment display and BCD data to follow the count (the internal latches beome transparent). A low input prevents updating of the latches as the count advances and the seven segment display and BCD data outputs remain fixed.



PIN ASSIGNMENT:



•OPTIONAL CHOICE—LAMP TEST (SPECIFY LS7056)

TOP VIEW
Figure 1

RESET:
A high input will hold all counter stages at zero. A low input allows counter operation.

INHIBIT INTERNAL RESET:
A high input will prevent automatically resetting the counter to zero when in the up mode and when the number set in the main signal store is reached.

PRESET:
A high level allows presetting of BCD counter to number set in preset store. A low input allows counter operation.

INHIBIT INTERNAL PRESET:
A high input will prevent automatically presetting the counter to the number set in preset store when in the down mode and when zero is reached.

SELECT STORAGE OF DATA INPUTS:
Two inputs which allow BCD data to be stored in either the preset, presignal, or main signal store. The proper method for loading the stores is depicted in Figure 4.

PIN 15	PIN 16	STORAGE
0	0	No Selection
1	0	Presignal
0	1	Main Signal
1	1	Preset

BCD DATA INPUTS:
Four inputs containing BCD data which are applied to either the preset, presignal, or main signal stores one decade at a time. This data can be provided by a set of thumbwheel switches which are driven by the digit select outputs. Referring to Figure 4, the BCD data inputs have built in pull down resistors (typically 51K ohm).

DIVIDE CONTROL:
Two inputs for allowing selection of either divide by 5, 6, or 1 of the count input.

PIN 2	PIN 3	
0	0	Divide by 5
1	0	Divide by 6
1	1	Divide by 1

MAIN SIGNAL OUTPUT:
An internal comparator will provide a high level output when the number set into the main signal store is reached by the counter. In the automatic mode and with the up/down control in the up position, the counter is reset to zero and the main signal output is typically a 2.5 microsecond wide pulse. In the manual mode (inhibit internal reset is high) the output remains high until the next count input or a reset is applied.

PRESIGNAL OUTPUT:
The presignal comparator provides a high level output when the number set into the presignal storage is reached. The output remains high until the next count input or a reset or preset is applied.

SCAN CLOCK INPUT:
A DC to 150 KHz oscillator input port for driving the internal scan counter is provided. Up to 150 KHz may be used when demultiplexing BCD data using the digit select outputs. The frequency of the oscillator is determined by an external RC network as shown in Figure 4. Table 1 indicates several frequencies and their associated RC networks. The oscillator can be overridden using an external driver. Table 2 indicates the external drive requirements. When displaying, leading zero blanking and unblanking on LSD is provided.

BLANKING OVERRIDE: (LS7055 ONLY)
On circuits with this option, unblanking can be made to occur on any digit by connecting that digit select output to the unblanking input. Since the input has an internal pull down resistor, it can be left floating when not in use.

LAMP TEST: (LS7056 ONLY)
A high input will cause the seven segment outputs to provide all 8's to a display (BCD outputs are not affected).

ZERO DETECT OUTPUT:
A high output occurs whenever the counter is at zero. In the automatic mode, and with the up/down input in the down mode, the counter presets to the number in the preset store and the zero detect output is typically a 1.5 microsecond pulse. In the manual mode (inhibit internal preset is high) the counter remains at zero until a preset or a count input pulse is applied.

DIGIT SELECT OUTPUTS:
Six positive outputs for digit identification. The outputs occur sequentially going from MSD to LSD and can be applied directly to thumbwheel switches. They must be buffered before being applied to the seven segment displays either by a CMOS or transistor buffer as shown in Figure 5. Figure 3 indicates the timing relationship between the digit select outputs and the BCD data outputs.

SEVEN SEGMENT OUTPUTS:
Capable of sourcing current into the base of a common emitter NPN transistor for interfacing to a seven segment display. Small displays needing an average current of .5 milliamperes can be interfaced to the circuit without external transistors. A typical example of a 12 volt circuit is shown in Figure 5.

BCD OUTPUTS:
Four outputs corresponding to the BCD data stored in the latches. The outputs can be demultiplexed using the circuitry shown in Figure 4. As can be seen from the timing diagram of Figure 3, the BCD data output and digit select outputs are completely stable during the positive digit select outputs.

POWER-ON-RESET:
An external RC network applied to the reset input as shown in Figure 4 can be used to reset the counter to "0" upon application of power. The preset input must be held low at this time. The RC time constant should be larger than the power supply rise time. For example, a 100K Ohm resistor and a $.1\mu F$ capacitor could be used if the power supply rise time was 5 milliseconds.

POWER SUPPLIES:
The circuit will operate over the range of +5 to +15 volts. At +5 volts, the inputs are TTL and CMOS compatible (external pull-up resistors must be provided on any input which does not pull up to VSS) when using TTL inputs. At +15 volts, inputs are CMOS compatible. All outputs are CMOS compatible from +5 to +15 volts.

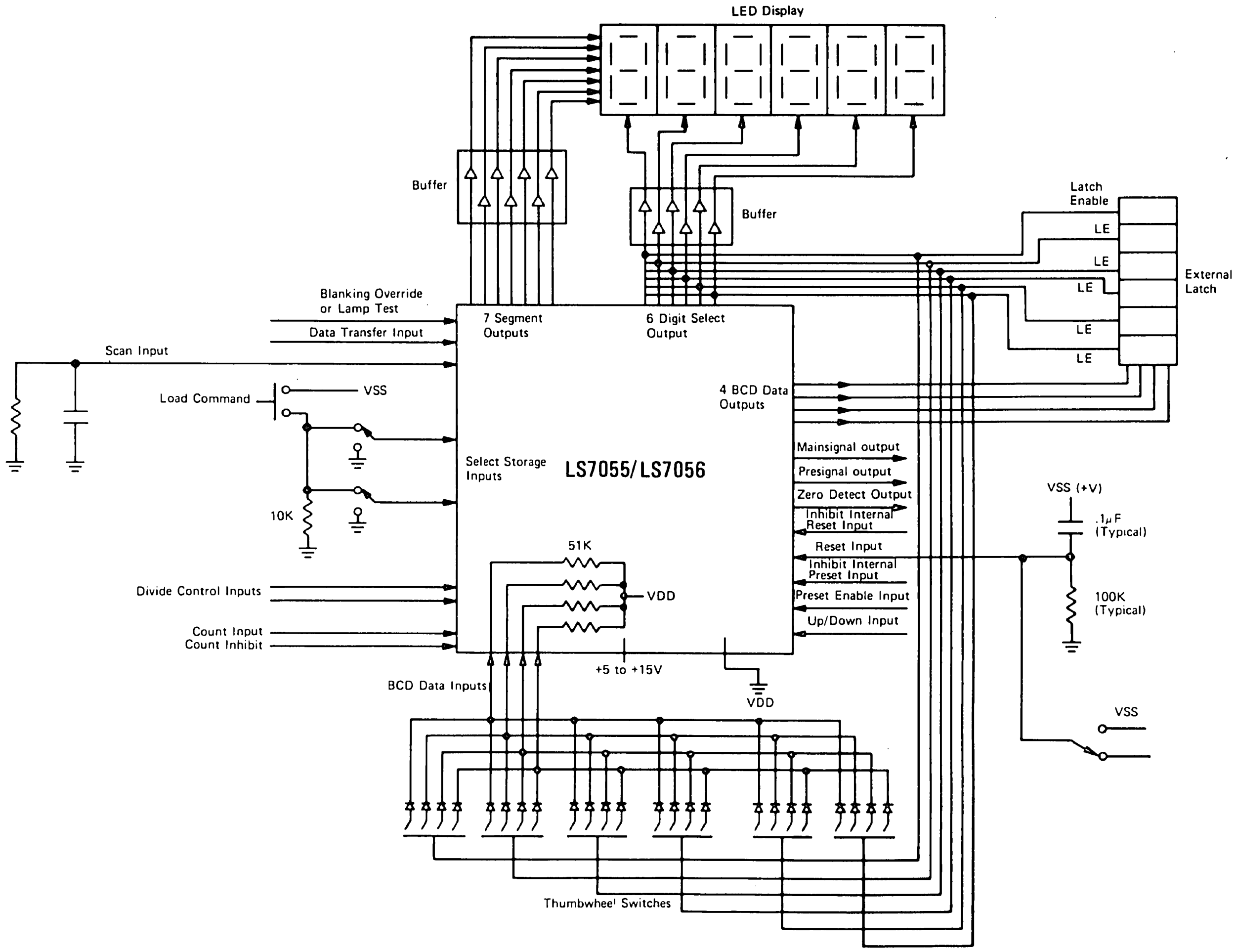


FIGURE 4
SYSTEM INTERCONNECTION DIAGRAM

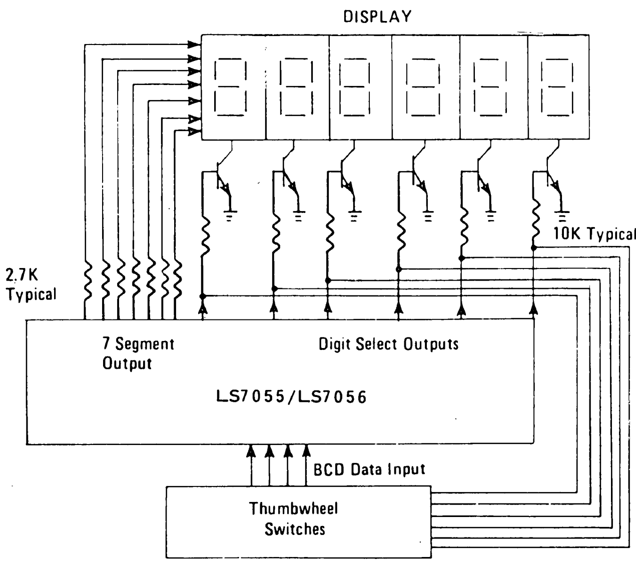


FIGURE 5

Driving a small LED Display (Typically 1/8") at 12 volt power supply. The 2.7K resistors provide approximately 3 milliamperes segment drive.

SCAN TABLE 1

Typical resistor/capacitor values for the scan oscillator

Resistor	Capacitor	Typical Frequency
10KΩ	750pF	150KHz
15KΩ	750pF	100KHz
100KΩ	1000pF	10KHz
1.0 MEGΩ	1000pF	1KHz

TABLE 2

Driver Requirements for Overriding Scan Oscillator Input

Power Supply (volts)	Sink Current	Source Current
5	1.0mA	0
10	4.5mA	0
15	10.0mA	0

MODES OF OPERATION

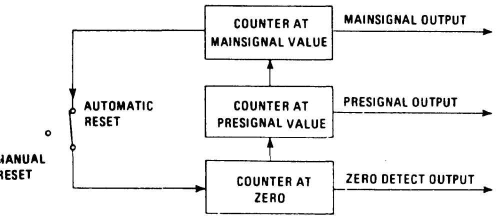


FIGURE 1
AUTOMATIC OR MANUAL OPERATION IN UP MODE

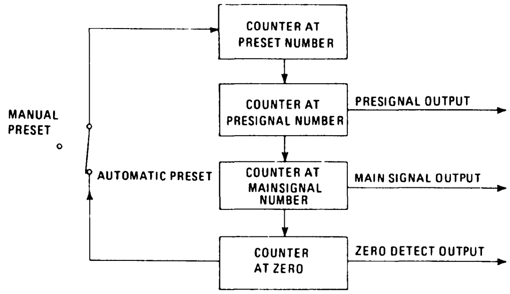


FIGURE 2
AUTOMATIC OR MANUAL OPERATION IN DOWN MODE

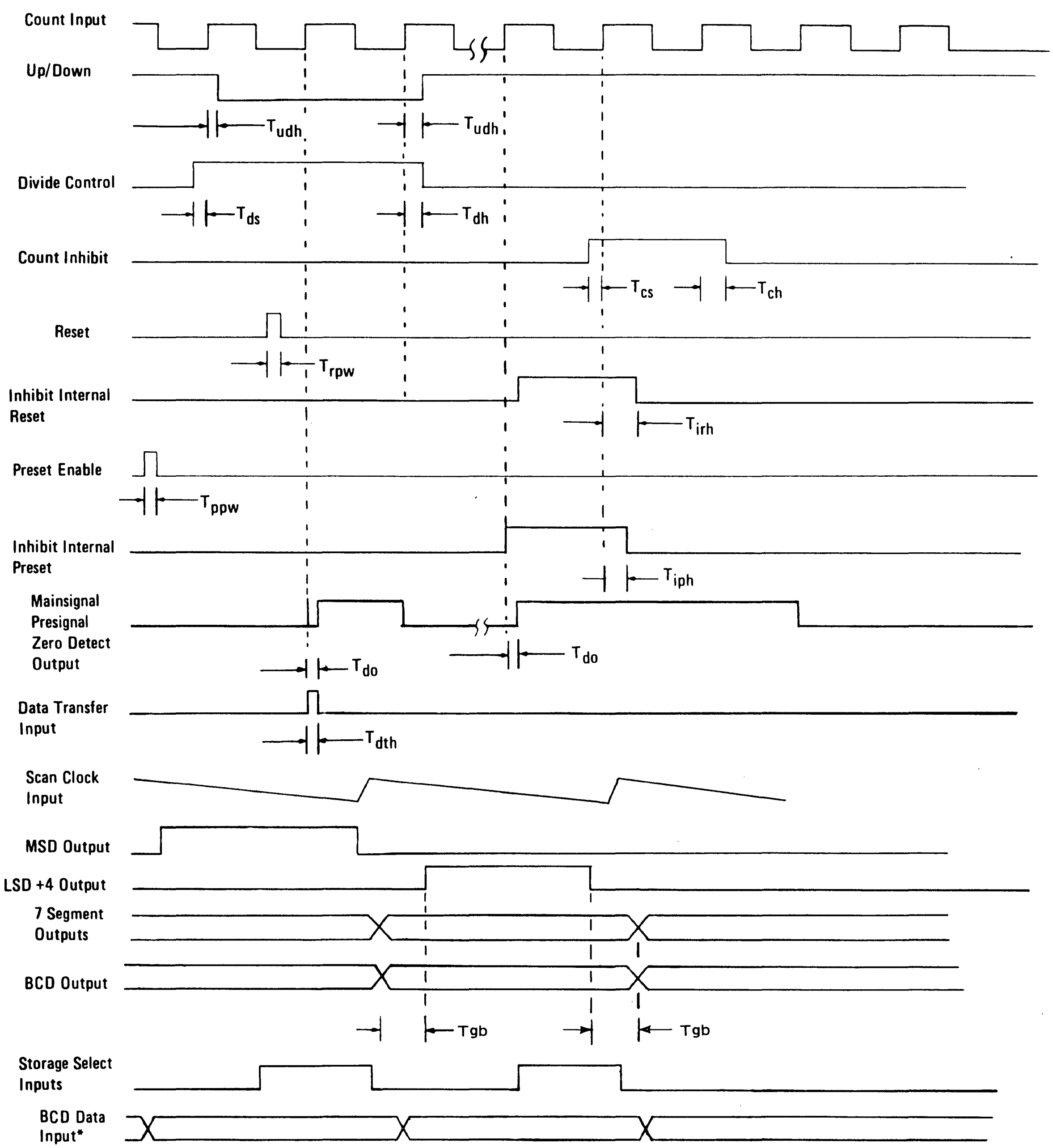


FIGURE 3 TIMING DIAGRAM

*BCD data input assumed to be applied from a set of thumbwheel switches as shown in Figure 5.

MAXIMUM RATINGS:

Parameter	Symbol	Value	Units
Storage Temperature	Tstg	−65 to +150	^oC
Operating Temperature	Ta	−25 to +70	^oC
Voltage (any pin to VSS)	Vmax	−30 to +0.5	V

DC ELECTRICAL CHARACTERISTICS:

(VDD=0V, VSS=+4.75 to +15V, $-25^oC \leq Ta \leq +70^oC$ unless otherwise specified)

Parameter	Symbol	Min.	Max.	Units
Quescent Supply Current				
(All Input Pins Tied to VSS)				
(All Output Pins Left Open)				
VSS=5V	Idd		20	mA
VSS=15V	Idd		25	mA
Input Capacitance All Inputs	Cin		10	PF
Hysterisis On Count Input		30%(VSS-VDD)		Volts
Noise Immunity All Other	VnL	30%(VSS-VDD)		Volts
Inputs	VnH	30%(VSS-VDD)		Volts
Outputs Levels All Outputs	VoL		0.5	Volts
(All Output Pins Left Open)	VoH	VSS-1		Volts
7 Segment Output Current				
Source Current				
VSS=5V, Vout=.7V, 70^oC	Iseg	0.3		mA
VSS=5V, Vout=.7V, 25^oC	Iseg	0.4		mA
VSS=10V, Vout= 7V, 25^oC	Iseg	2.0		mA
VSS=15V, Vout= 13V, 25^oC	Iseg	3.0		mA
Note: Limit Segment Source Current to 4.5 mA max.				
Sink Current(Vout=.4V)				
VSS=5V, 25^oC	Iseg	−21		μA
VSS=10V, 25^oC	Iseg	−17		μA
VSS=15V, 25^oC	Iseg	−15		μA
VSS=15V, 70^oC	Iseg	−10		μA
BCD, Zero Detect, Mainsignal, and Presignal Output Current				
Source Current				
VSS=5V, Vout=4.5V, 70^oC	IoH	.10		mA
VSS=5V, Vout=4.5V, 25^oC	IoH	.13		mA
VSS=10V, Vout=9.0V, 25^oC	IoH	.70		mA
VSS=15V, Vout=13V, 25^oC	IoH	2.5		mA
Note: Limit Digit Select Source Current to 4.5mA max.				
Sink Current(Vout=.4V)				
VSS=5V, 25^oC	IoL	−7.5		μA
VSS=10V, 25^oC	IoL	−6.0		μA
VSS=15V, 25^oC	IoL	−5.5		μA
VSS=15V, 70^oC	IoL	−4.0		μA
Digit Select Output Current				
Source Current				
VSS=5V, Vout=4.5V, 70^oC	IoH	0.28		mA
VSS=5V, Vout=4.5V, 25^oC	IoH	0.35		mA
VSS=10V, Vout=9.0V, 25^oC	IoH	2.0		mA
VSS=15V, Vout= 13.5V, 25^oC	IoH	7.0		mA
Note: Limit digit select current to 10mA.				
Sink Current (Vout=.4V)				
VSS=5V, 25^oC	IoL	−15		μA
VSS=10V, 25^oC	IoL	−12		μA
VSS=15V, 25^oC	IoL	−11		μA
VSS=15V, 70^oC	IoL			μA

DYNAMIC ELECTRICAL CHARACTERISTICS:

(VDD=0V, VSS=+4.75 to +15V, $-25^oC \leq Ta \leq +70^oC$ unless otherwise specified)

Parameter	Symbol	Min.	Max.	Units
Count Input Frequency				
VSS=5V	Fc	DC	250	KHz
VSS=10V	Fc	DC	175	KHz
VSS=15V	Fc	DC	125	KHz
Pulse Width				
VSS=5V	Tcw	2		μsec
VSS=10V	Tcw	2.8		μsec
VSS=15V	Tcw	4		μsec
Rise Time	Tcr		∞	μsec
Fall Time	Tcf		∞	μsec
Scan Input Frequency				
VSS=5V	Fsc	DC	150	KHz
VSS=10V	Fsc	DC	125	KHz
VSS=15V	Fsc	DC	100	KHz
Divide Control				
Set-Up Time	Tds	2.0		μsec
Hold Time	Tdh	8		μsec
Reset Pulse Width**	Trpw	2		μsec
Reset Set-Up Time	Trs	0		μsec
Hold Time	Trh	6		μsec
Inhibit Internal Reset				
Set-Up time	Tirs	0		μsec
Hold Time*	Tirh	3		μsec
Preset Pulse Width**	Tppw	2		μsec
Preset Enable				
Set-Up Time	Tpes	0		μsec
Hold Time	Tpeh	6		μsec
Inhibit Internal Preset				
Set-Up Time	Tips	0		μsec
Hold Time*	Tiph	3		μsec
Data Transfer Pulse Width**	Tdtw	2		μsec
Data Transfer				
Set-Up Time	Tdts	0		
Hold Time	Tdth	6		μsec
Up/Down				
Set-Up Time	Tuds	0		
Hold Time	Tudh	10		μsec
Count Inhibit				
Set-Up Time	Tcs	2		μsec
Hold Time	Tch	10		μsec
Data Outputs (CL=10PF)				
Rise Time	Tdr		1.0	μsec
Fall Time				
VSS=5V	Tdf		2.0	μsec
VSS=10V	Tdf		3.0	μsec
VSS=15V	Tdf		4.0	μsec
Digit Select Outputs Guard Band time within 7 segment and BCD outputs (fig. 3)	Tgb	0.5		μsec
Main Signal, Presignal, Zero Detect Outputs delay with respect to positive edge of Count Input	Tdo		3	μsec

Set-Up and hold times are defined with respect to positive edge of count input except where indicated by asterisks.

*Indicates a hold time which must last for at least one whole count cycle plus five microseconds past the next positive edge of count input.

**Reset, Preset and data transfer pulse width is as specified except if applied when a count input is going positive. In that case the set-up and hold times govern.

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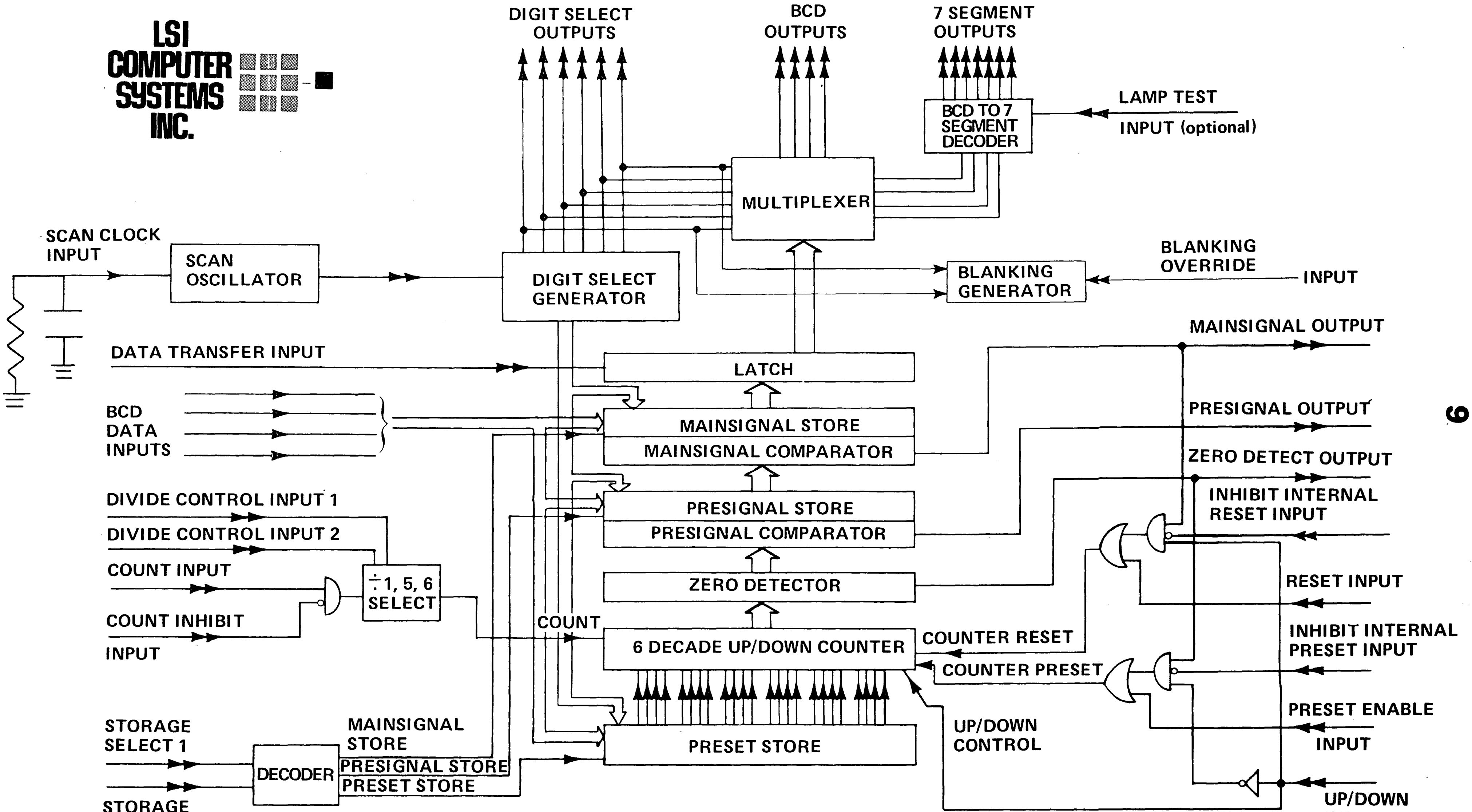

LS7055/LS7056
BLOCK DIAGRAM

6

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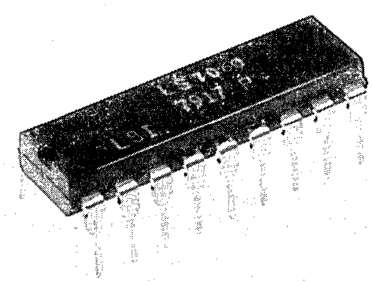
LS7060 | 32 BIT BINARY UP COUNTER

with 32 Bit Latch, Multiplexer and Three-State Drivers

JUNE 1983

FEATURES:

- DC to 10MHz Count Frequency
- 8 Bit Byte Multiplexer
- DC to 1MHz Scan Frequency
- Single Power Supply Operation, +4.75 VDC to +5.25 VDC
- Three-State Data Outputs, Bus and TTL Compatible
- Inputs TTL, NMOS and CMOS Compatible
- Unique Cascade Feature Allows Multiplexing of Successive Bytes of Data in Sequence in Multiple Counter Systems
- Low Power Dissipation
- All Inputs Protected
- 18 Pin DIP



DESCRIPTION:

The LS7060 is a monolithic, ion implanted, N channel MOS Silicon Gate, 32 bit up counter. The circuit includes latches, multiplexer, eight three-state binary data output drivers and output cascading logic.

DESCRIPTION OF OPERATION:

32 BIT BINARY UP COUNTER

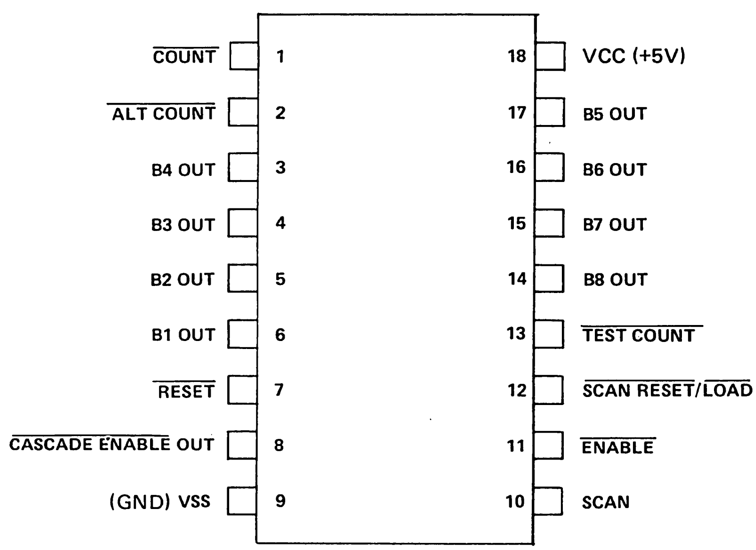
The 32 bit static ripple through counter increments on the negative edge of the input count pulse.
Maximum ripple time is 4μs (transition count of thirty-two "ones" to thirty two "zeros").
Guaranteed count frequency is DC to 10MHz.

$\overline{\text{COUNT}}$, $\overline{\text{ALT COUNT}}$

Input count pulses to the 32 bit counter may be applied through either of these two inputs. The $\overline{\text{Alt Count}}$ input circuitry contains a Schmitt trigger network which allows proper counting with "infinitely" long clock edges. A high applied to either of these two inputs inhibits counting.

$\overline{\text{RESET}}$

All 32 counter bits are reset to zero when $\overline{\text{Reset}}$ is brought low for a minimum of 1μs. $\overline{\text{Reset}}$ must be high for a minimum of 300ns before next valid count can be recorded.



TOP VIEW
STANDARD 18 PIN DIP
Figure 1

TEST COUNT

Count pulses may be applied to the last 16 bits of the binary counter through this input, as long as bit 16 of the counter is a low. The counter advances on the negative transition of these pulses. This input is intended to be used for test purposes. It allows use of the LS7060 as "almost" a full dual 16 bit counter.

LATCHES

32 bits of latch are provided for storage of counter data. All latches are loaded when the Load input is brought low for a minimum of 1μs and kept low until a minimum of 4μs has elapsed from previous negative edge of count pulse (ripple time).

Storage of valid data occurs when Load is brought high for a minimum of 250ns before next negative edge of count pulse or Reset.

SCAN COUNTER AND DECODER

The scan counter is reset to the least significant byte position (state 1) when Scan Reset input is brought low for a minimum of 1μs. The scan counter is enabled for counting as long as the Enable input is held low. The counter advances to the next significant byte position on each negative transition of the Scan pulse. When the scan counter advances to state 5 it disables the Output Drivers and stops in that state until Scan Reset is again brought low.

SCAN

When the scan counter is enabled, each negative transition of this input advances the scan counter to its next state. When Scan is low the Data Outputs are disabled. When Scan is brought high the Data Outputs are enabled and present the latched counter data corresponding to the present state of the scan counter.

Therefore, in microprocessor applications, the Data Output Bus may be utilized for other activities while new data is propagating to the outputs. This positive Scan pulse can be viewed as a "Place the next byte on my bus" instruction from the microprocessor.

Minimum positive and negative pulse widths of 500ns for the Scan signal are required for scan counter operation.

SCAN RESET/LOAD

When this input is brought low for a minimum of 1μs the scan counter is reset to state 1, least significant byte position, and the latches are simultaneously loaded with new count information.

ENABLE

When this input is high, the scan counter and the Data Outputs are disabled. When Enable is low, the scan counter and Data Outputs are enabled for normal operation. Transition of this input should only be made while the Scan input is in a low state in order to prevent false clocking of the scan counter.

CASCADE ENABLE

This output is normally high. It transitions low and stays low when the sc
multiple counter system this output is connected to the Enable input of the
The Scan input and Scan Reset/Load input are carried to all the counters ir
sents its bytes of data to the output bus on each positive transition of the scan
When state 5 of counter 1 is achieved, counter 2 presents its data to the outp
all counters in the cascade have been addressed. See Fig. 4 for an illustration o
This output is TTL, CMOS and NMOS compatible.

THREE-STATE DATA OUTPUT DRIVERS

The eight Data Output Drivers are disabled when either Enable input is high, t
Scan input is low.
The Output Drivers are TTL and Bus compatible.

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE
Storage Temperature	T_{STG}	−55 to +150
Operating Temperature	T_A	0 to +70
Voltage(any pin to VSS)	Vmax	+10 to −0.3

DC ELECTRICAL CHARACTERISTICS

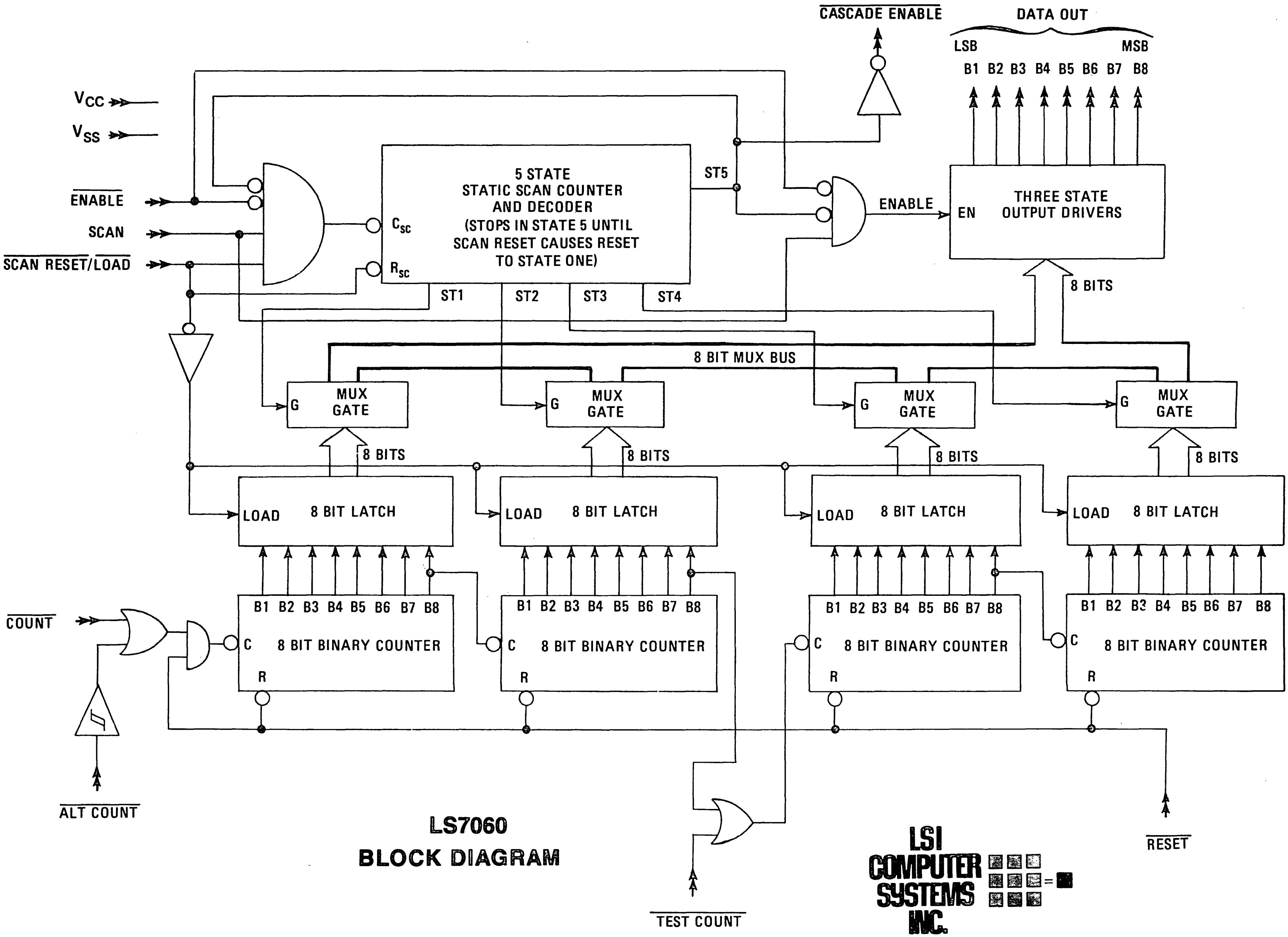
(V_{CC}=+5V±5%, V_{SS}=0V, T_A=0°C to +70°C unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Units
Power Supply Current	I_{DD}		15	mA
Input High Voltage	V_{IH}	+3.5	V_{DD}	V
Input Low Voltage	V_{IL}	0	+0.6	V
Output High Voltage				
Cascade Enable	V_{OH}	V_{CC}−0.2		V
		+2.4		V
B1 – B8		+2.4		V
		+2.0		V
Output Low Voltage				
Cascade Enable	V_{OL}		+0.2	V
			+0.4	V
B1 – B8			+0.4	V
Output Source Current	Isource	3.0		mA
B1 – B8 Outputs		4.8		mA
		7.3		mA
Output Sink Current	Isink	5.7		mA
B1 –B8 Outputs		4.0		mA
		2.2		mA
Output Leakage Current B1 – B8 (Off State)	I_{OL}		1	μA
Input Capacitance	C_{IN}		6	pF
Output Capacitance	C_{OUT}		12	pF
Input Leakage Current	I_{LI}		1	μA
INPUT CURRENT				
*Scan Reset/Load	I_{IH}		−2.5	μA
	I_{IL}		−5	μA
**Count, Alt Count	I_{IH}		5	μA
Test Count	I_{IL}		1	μA

*Input has internal pull-up resistor to V_{CC}

**Inputs have internal pull-down resistor to V_{SS}

5



LS7060
BLOCK DIAGRAM

LSI COMPUTER SYSTEMS INC.

SCAN COUNTER & DECODER OUTPUTS TIMING DIAGRAM

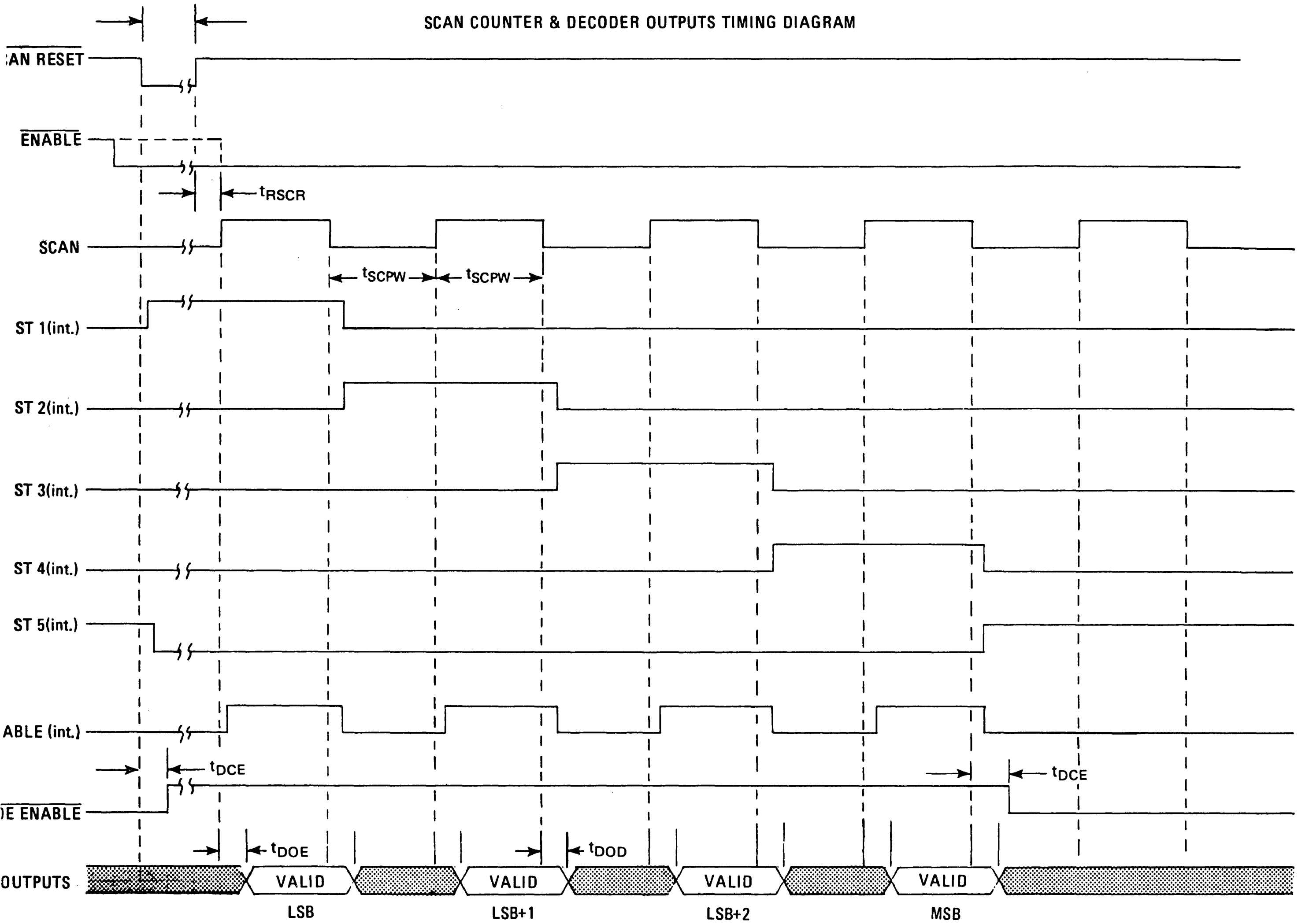


Figure 2

COUNTER TIMING DIAGRAM

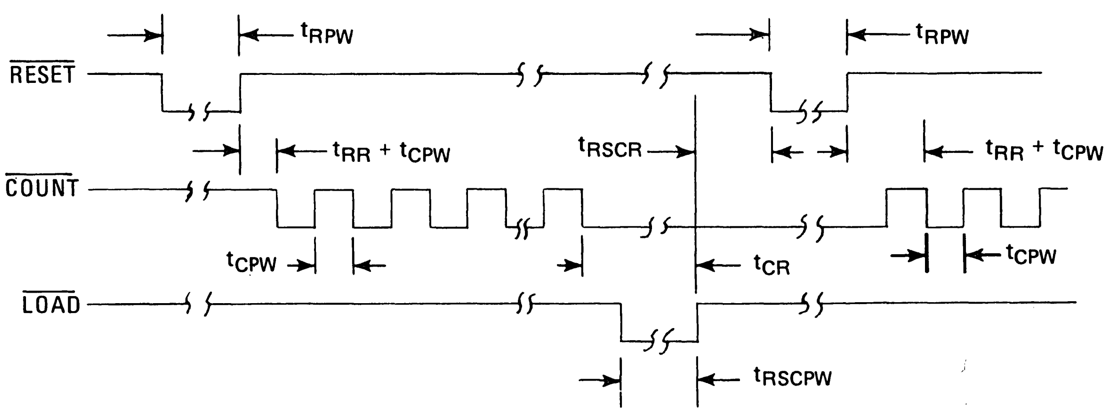


Figure 3

DYNAMIC ELECTRICAL CHARACTERISTICS

(V_{CC}=+5V±5%, V_{SS}=0V, T_A=0°C to +70°C unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Units	Conditions
Count Frequency ($\overline{\text{Count}}$, $\overline{\text{Alt Count}}$, $\overline{\text{Test Count}}$)	fc	DC	10	MHz	
Count Pulse Width (All Count Inputs)	t_{CPW}	40		ns	Measured @ 50% point, Max t_r, t_f =10ns
Count Rise & Fall Time ($\overline{\text{Count}}$, $\overline{\text{Test Count}}$)	t_r, t_f		30	µs	
Count Rise & Fall Time ($\overline{\text{Alt Count}}$)	t_r, t_f		No Max Limit		
Count Ripple Time ($\overline{\text{Count}}$, $\overline{\text{Alt Count}}$)	t_{CR}		4	µs	Transition from 32 ones to 32 zeros from negative edge of count pulse
Count Ripple Time ($\overline{\text{Test Count}}$)	t_{CR}		2	µs	Transition of second 16 bits from all ones to all zeros from negative edge of count pulse
$\overline{\text{Reset}}$ Pulse Width (All Counter Stays Fully Reset)	t_{RPW}	500		ns	Measured @ 50% point Max t_r, t_f =200ns
$\overline{\text{Reset}}$ Removal Time ($\overline{\text{Reset}}$ Removed From All Counter Stages)	t_{RR}		250	ns	Measured from $\overline{\text{Reset}}$ signal @ V_{IH}
Scan Frequency	f_{sc}		1	MHz	
Scan Pulse Width	t_{SCPW}	500		ns	Measured @ 50% point Max t_r, t_f =100ns
$\overline{\text{Scan Reset}}$/$\overline{\text{Load}}$ Pulse Width (All latches loaded and Scan Counter Reset to Least Significant Byte)	t_{RSCPW}	1		µs	Measured @ 50% point Max t_r, t_f =200ns
$\overline{\text{Scan Reset}}$/$\overline{\text{Load}}$ Removal Time (Reset Removed from Scan Counter; Load Command Removed From Latches)	t_{RSCR}		250	ns	Measured from $\overline{\text{Scan Reset}}$/$\overline{\text{Load}}$ @ V_{IH}
Output Disable Delay Time (B1 – B8)	t_{DOD}		200	ns	Transition to Output High Impedance State Measured From Scan @ V_{IL} or $\overline{\text{Enable}}$ @ V_{IH}
Output Enable Delay Time (B1 – B8)	t_{DOE}		200	ns	Transition to Valid On State Measured from Scan @ V_{IH} and $\overline{\text{Enable}}$ @ V_{IL}; Delay to Valid Data Levels for C_{OL}=10pf and one TTL Load or Valid Data Currents for High Capacitance Loads
Output Delay Time $\overline{\text{Cascade Enable}}$	t_{DCE}		300	ns	Negative Transition from Scan @V_{IL} and ST5 of Scan Counter or Positive Transition From $\overline{\text{Scan Reset}}$/$\overline{\text{Load}}$ @ V_{IL} to Valid Data Levels for C_{OL}=10pf and one TTL Load

Refer to page 4 for timing diagrams.

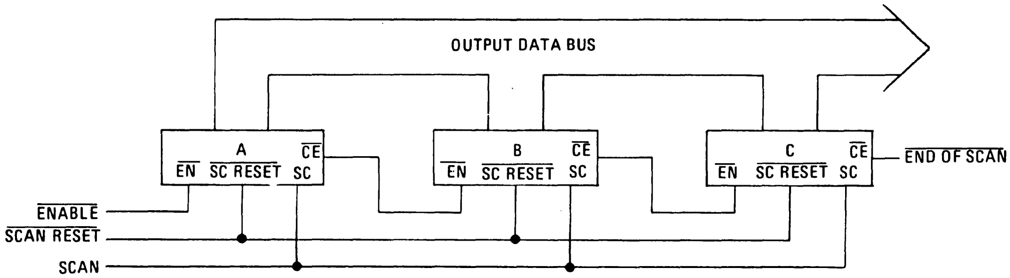
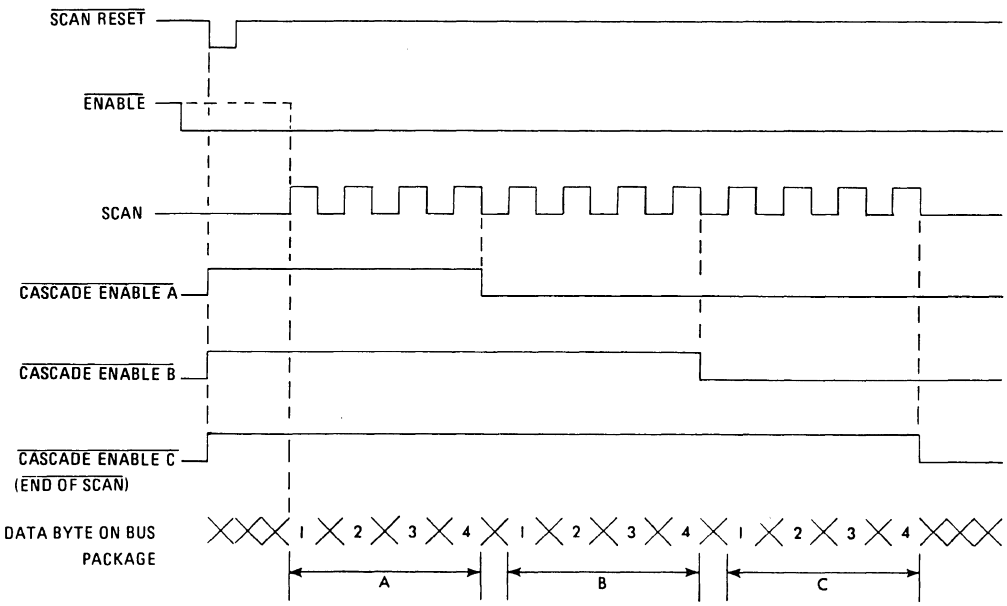


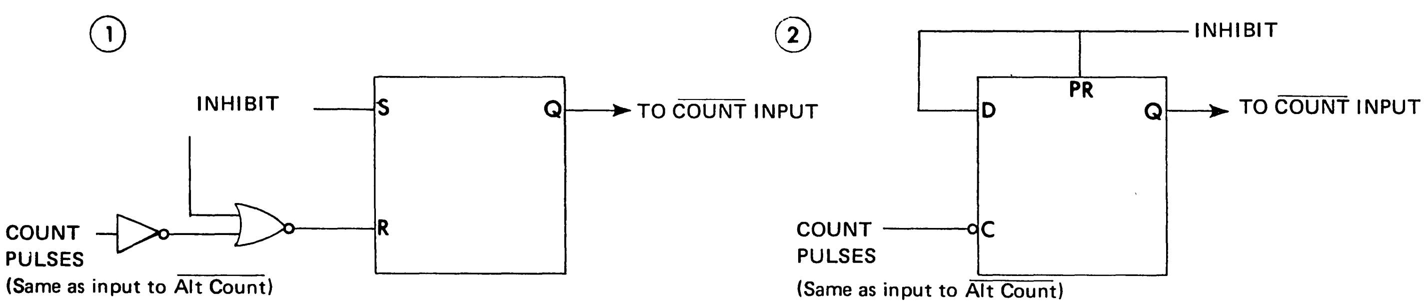
ILLUSTRATION OF A 3 DEVICE CASCADE

Fig. 4



TIMING DIAGRAM

Fig. 5



LS7060 — SYNCHRONIZING INHIBIT WITH C.P.

Fig. 6

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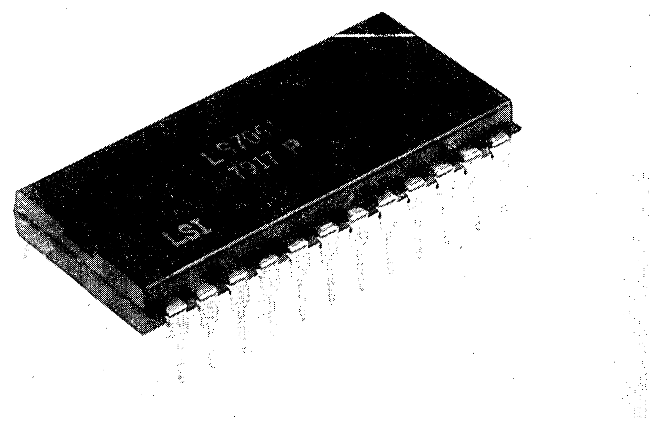
LS7061 — 32 BIT BINARY UP COUNTER

with 40 Bit Latch, Multiplexer and Three-State Drivers

Revised January 1986

FEATURES:

- DC to 10MHz Count Frequency
- 8 Bit Byte Multiplexer
- DC to 1MHz Scan Frequency
- Ability to Latch External 8 Bits of High Speed External Prescaler Thereby Extending Count Frequency to 2.56GHz
- Single Power Supply Operation, +4.75 VDC to +5.25 VDC
- Three-State Data Outputs, Bus and TTL Compatible
- Inputs TTL, NMOS and CMOS Compatible
- Unique Cascade Feature Allows Multiplexing of Successive Bytes of Data in Sequence in Multiple Counter Systems
- Low Power Dissipation
- All Inputs Protected
- 24 Pin DIP



DESCRIPTION:

The LS7061 is a monolithic, ion implanted MOS Silicon Gate, 32 bit up counter. The circuit includes 40 latches, multiplexer, eight three-state binary data output drivers and output cascading logic.

DESCRIPTION OF OPERATION:

32 BIT BINARY UP COUNTER

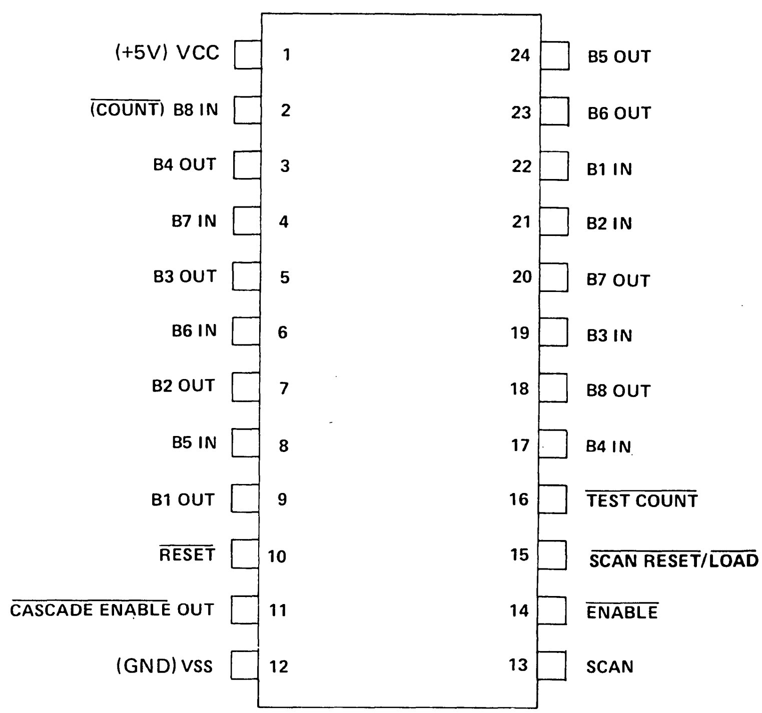
The 32 bit static ripple through counter increments on the negative edge of the input count pulse.
Maximum ripple time is 4μs (transition count of thirty two "ones" to thirty two "zeros").
Guaranteed count frequency is DC to 10MHz.

B8 ($\overline{\text{COUNT}}$)

Input count pulses to the 32 bit counter are applied through this input. This input is the most significant bit of the external data byte.

$\overline{\text{RESET}}$

All 32 counter bits are reset to zero when $\overline{\text{Reset}}$ is brought low for a minimum of 1μs. $\overline{\text{Reset}}$ must be high for a minimum of 300ns before next valid count can be recorded.



LS7061 PIN ASSIGNMENT

$\overline{\text{TEST COUNT}}$

Count pulses may be applied to the last 16 bits of the binary counter through this input, as long as bit 16 of the counter is a low. The counter advances on the negative transition of these pulses. This input is intended to be used for test purposes.

LATCHES

40 bits of latch are provided, eight for storage of the contents of a high speed external prescaling counter and the remaining 32 for the contents of the internal counter. All latches are loaded when the $\overline{\text{Load}}$ input is brought low for a minimum of 1 μs and kept low until a minimum of 4μs has elapsed from previous negative edge of count pulse (ripple time). Storage of valid data occurs when $\overline{\text{Load}}$ is brought high for a minimum of 250ns before next negative edge of count pulse or $\overline{\text{Reset}}$.

SCAN COUNTER AND DECODER

The scan counter is reset to the least significant byte position (State 1) when $\overline{\text{Scan Reset}}$ input is brought low for a minimum of 1 μs. The scan counter is enabled for counting as long as the $\overline{\text{Enable}}$ input is held low. The counter advances to the next significant byte position on each negative transition of the Scan pulse. When the scan counter advances to state 6 it disables the Output Drivers and stops in that state until $\overline{\text{Scan Reset}}$ is again brought low.

SCAN

When the scan counter is enabled, each negative transition of this input advances the scan counter to its next state. When Scan is low the Data Outputs are disabled. When Scan is brought high the Data Outputs are enabled and present the latched counter data corresponding to the present state of the scan counter. Therefore, in microprocessor applications, the Data Output Bus may be utilized for other activities while new data is propagating to the outputs. This positive Scan pulse can be viewed as a "Place the next byte on my bus" instruction from the microprocessor. Minimum positive and negative pulse widths of 500ns for the Scan signal are required for scan counter operation.

$\overline{\text{SCAN RESET}}/\overline{\text{LOAD}}$

When this input is brought low for a minimum of 1μs the scan counter is reset to state 1, least significant byte position, and the latches are simultaneously loaded with new count information.

$\overline{\text{ENABLE}}$

When this input is high, the scan counter and the Data Outputs are disabled. When $\overline{\text{Enable}}$ is low, the scan counter and Data Outputs are enabled for normal operation. Transition of this input should only be made while the Scan input is in a low state in order to prevent false clocking of the scan counter.

CASCADE ENABLE:

This output is normally high. It transitions low and stays low when the scan multiple counter system this output is connected to the $\overline{\text{Enable}}$ input o string. The Scan input and $\overline{\text{Scan Reset}}/\overline{\text{Load}}$ input are carried to all the coun then presents its bytes of data to the Output Bus on each positive transitio discussed. When state 6 of counter 1 is achieved, counter 2 presents its data continues until all counters in the cascade have been addressed. See Fig. 4 fc cade design. This output is TTL, CMOS and NMOS compatible.

THREE-STATE DATA OUTPUT DRIVERS:

The eight Data Output Drivers are disabled when either $\overline{\text{Enable}}$ input is high the Scan input is low.
The Output Drivers are TTL and Bus compatible.

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE
Storage Temperature	T_{STG}	−55 to +150
Operating Temperature	T_A	0 to +70
Voltage(any pin to VSS)	Vmax	+10 to −0.3

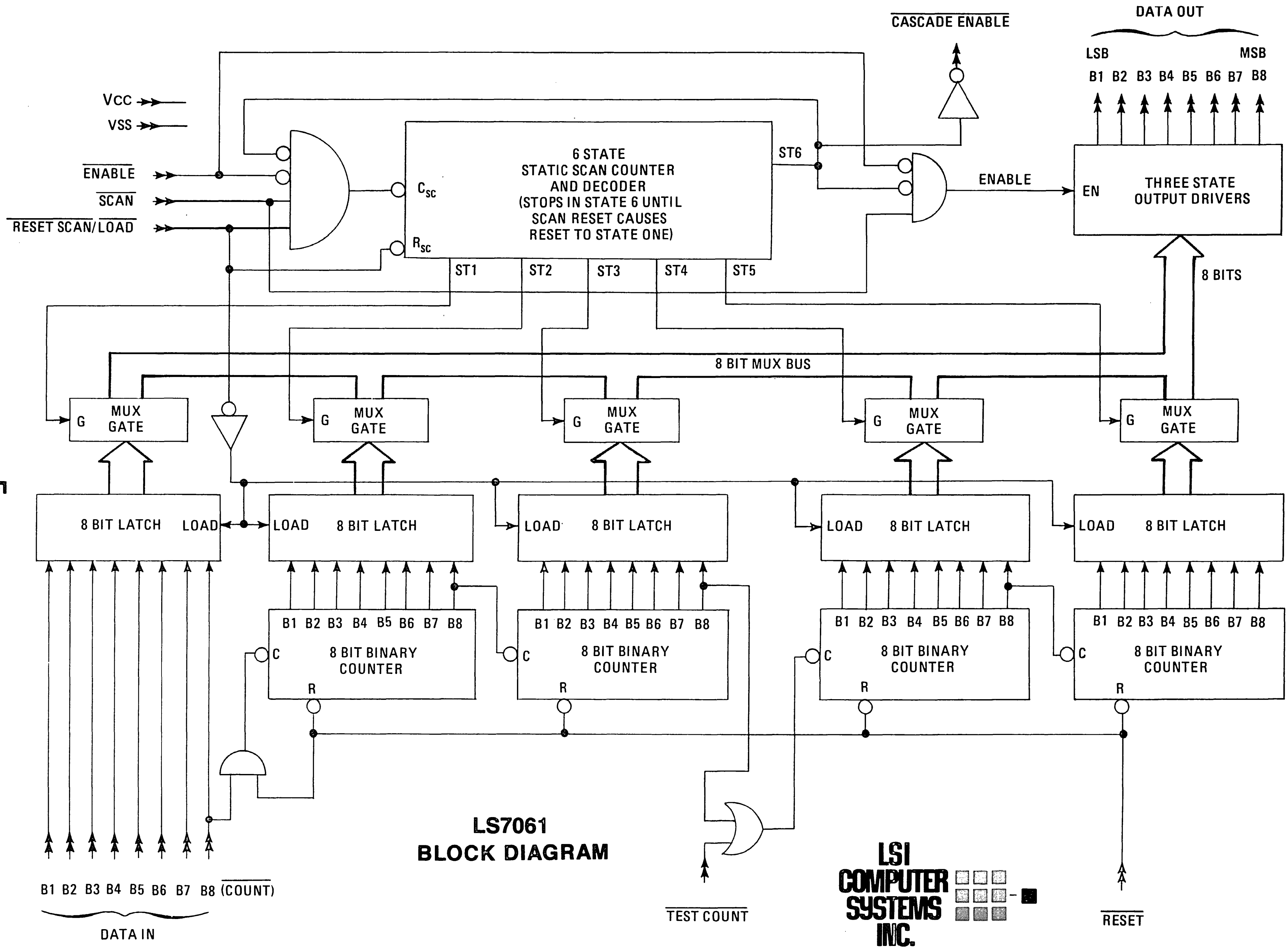
DC ELECTRICAL CHARACTERISTICS

(V_{CC}=+5V±5%, V_{SS} = 0V, T_A=0°C to +70°C unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Uni
Power Supply Current	I_{DD}		15	mA
Input High Voltage	V_{IH}	+3.5	V_{CC}	V
Input Low Voltage	V_{IL}	0	+0.6	V
OUTPUT HIGH VOLTAGE				
Cascade Enable	V_{OH}	V_{CC}−0.2		V
		+2.4		V
B1 – B8		+2.4		V
		+2.0		V
OUTPUT LOW VOLTAGE				
Cascade Enable	V_{OL}		+0.2	V
			+0.4	V
B1 – B8			+0.4	V
Output Source Current	Isource	3.0		mA
B1 – B8 Outputs		4.8		mA
		7.3		mA
Output Sink Current	Isink	5.7		mA
B1 –B8 Outputs		4.0		mA
		2.2		mA
Output Leakage Current B1 – B8 (Off State)	I_{OL}		1	μA
Input Capacitance	C_{IN}		6	pF
Output Capacitance	C_{OUT}		12	pF
Input Leakage Current	I_{LI}		1	μA
INPUT CURRENT				
*$\overline{\text{Scan Reset}}/\overline{\text{Load}}$	I_{IH}		−2.5	μA
	I_{IL}		−5	μA
**B1 - B8 Inputs	I_{IH}		5	μA
$\overline{\text{Test Count}}$	I_{IL}		1	μA

*Input has internal pull-up resistor to V_{CC}

**Inputs have internal pull-down resistor to V_{SS}



LS7061
BLOCK DIAGRAM

LSI COMPUTER SYSTEMS INC.

SCAN COUNTER & DECODER OUTPUTS TIMING DIAGRAM

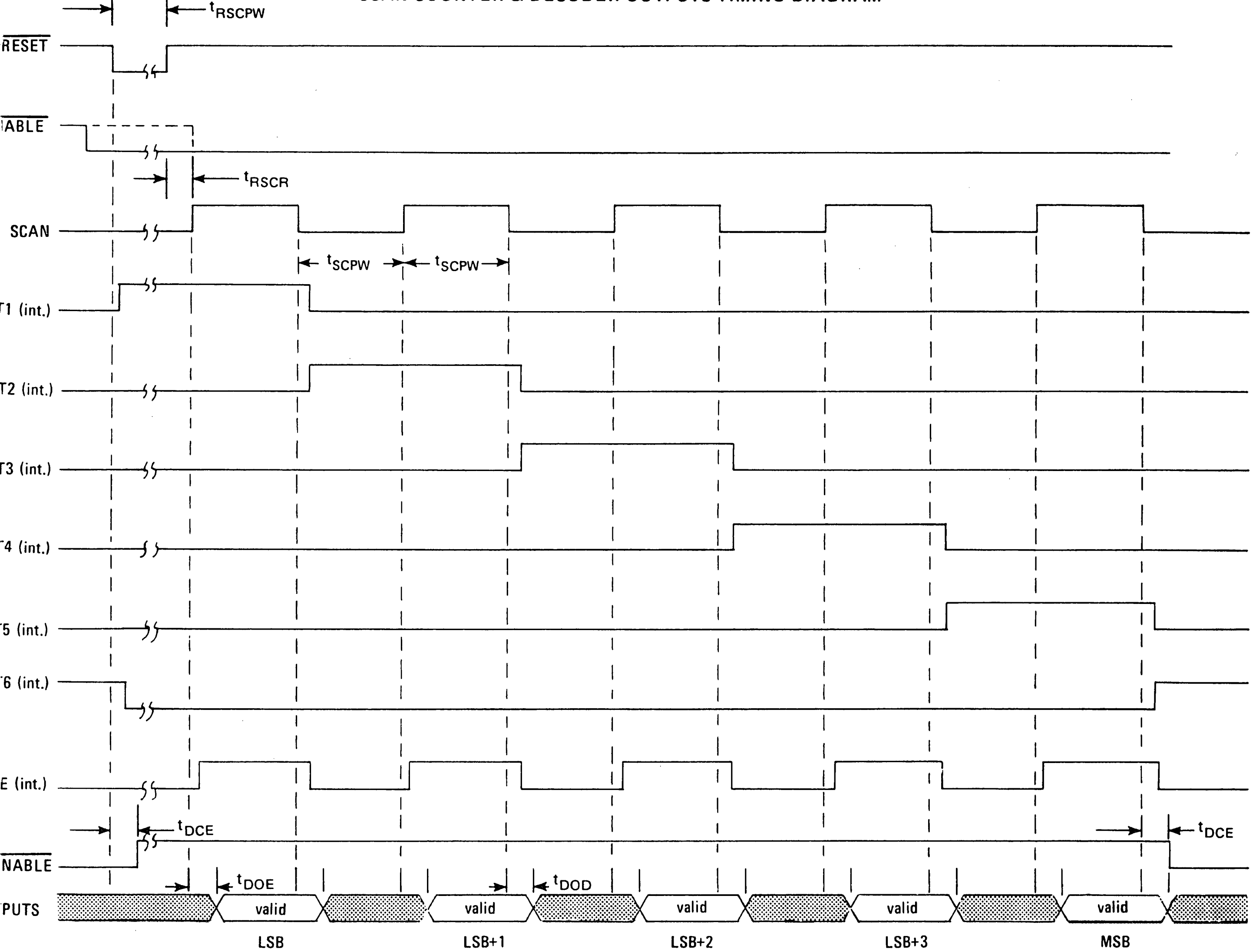


Figure 2

COUNTER TIMING DIAGRAM

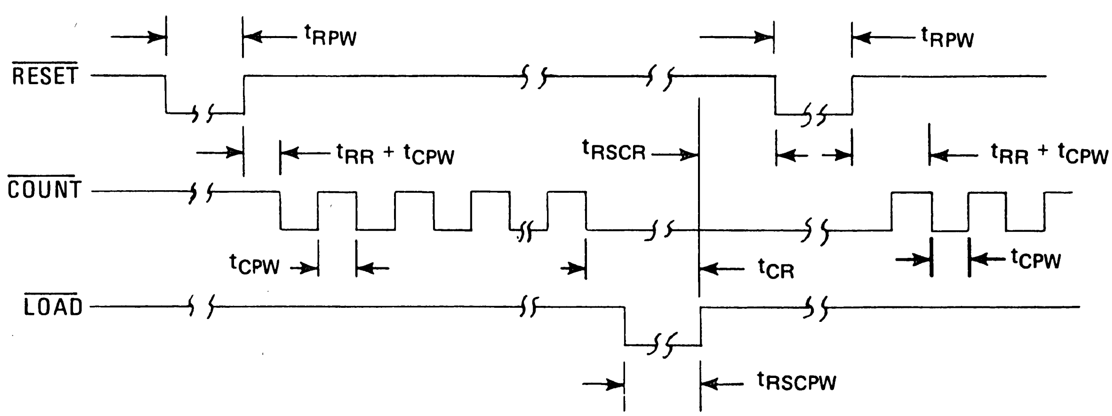


Figure 3

DYNAMIC ELECTRICAL CHARACTERISTICS

(V_{CC}=+5V±5%, V_{SS}=0V, T_A=0°C to +70°C unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Units	Conditions
Count Frequency B8($\overline{\text{Count}}$), $\overline{\text{Test Count}}$)	fc	DC	10	MHz	
Count Pulse Width B8($\overline{\text{Count}}$), $\overline{\text{Test Count}}$	t_{CPW}	40		ns	Measured @ 50% point, Max t_r, t_f =10ns
Count Rise & Fall Time B8($\overline{\text{Count}}$), $\overline{\text{Test Count}}$	t_r, t_f		30	µs	
Count Ripple Time B8($\overline{\text{Count}}$)	t_{CR}		4	µs	Transition from 32 ones to 32 zeros from negative edge of count pulse
Count Ripple Time ($\overline{\text{Test Count}}$)	t_{CR}		2	µs	Transition of second 16 bits from all ones to all zeros from negative edge of count pulse
$\overline{\text{Reset}}$ Pulse Width (All Counter Stages Fully Reset)	t_{RPW}	500		ns	Measured @ 50% point Max t_r, t_f =200ns
$\overline{\text{Reset}}$ Removal Time ($\overline{\text{Reset}}$ Removed From All Counter Stages)	t_{RR}		250	ns	Measured from $\overline{\text{Reset}}$ signal @ V_{IH}
Scan Frequency	f_{sc}		1	MHz	
Scan Pulse Width	t_{SCPW}	500		ns	Measured @ 50% point Max t_r, t_f =100ns
$\overline{\text{Scan Reset/Load}}$ Pulse Width (All latches loaded and Scan Counter Reset to Least Significant Byte)	t_{RSCPW}	1		µs	Measured @ 50% point Max t_r, t_f =200ns
$\overline{\text{Scan Reset/Load}}$ Removal Time (Reset Removed from Scan Counter; Load Command Removed From Latches)	t_{RSCR}		250	ns	Measured from $\overline{\text{Scan Reset/}}$ Load @ V_{IH}
Output Disable Delay Time (B1 – B8)	t_{DOD}		200	ns	Transition to Output High Impedance State Measured From Scan @ V_{IL} or $\overline{\text{Enable}}$ @ V_{IH}
Output Enable Delay Time (B1 – B8)	t_{DOE}		200	ns	Transition to Valid On State Measured from Scan @ V_{IH} and $\overline{\text{Enable}}$ @ V_{IL} ; Delay to Valid Data Levels for C_{OL}=10pf and one TTL Load or Valid Data Currents for High Capacitance Loads
Output Delay Time $\overline{\text{Cascade Enable}}$	t_{DCE}		300	ns	Negative Transition from Scan @V_{IL} and ST6 of Scan Counter or Positive Transition From $\overline{\text{Scan Reset/Load}}$ @ V_{IL} to Valid Data Levels for C_{OL}=10pf and one TTL Load

Refer to page 4 for timing diagrams.

ILLUSTRATION OF A 3 DEVICE CASCADE

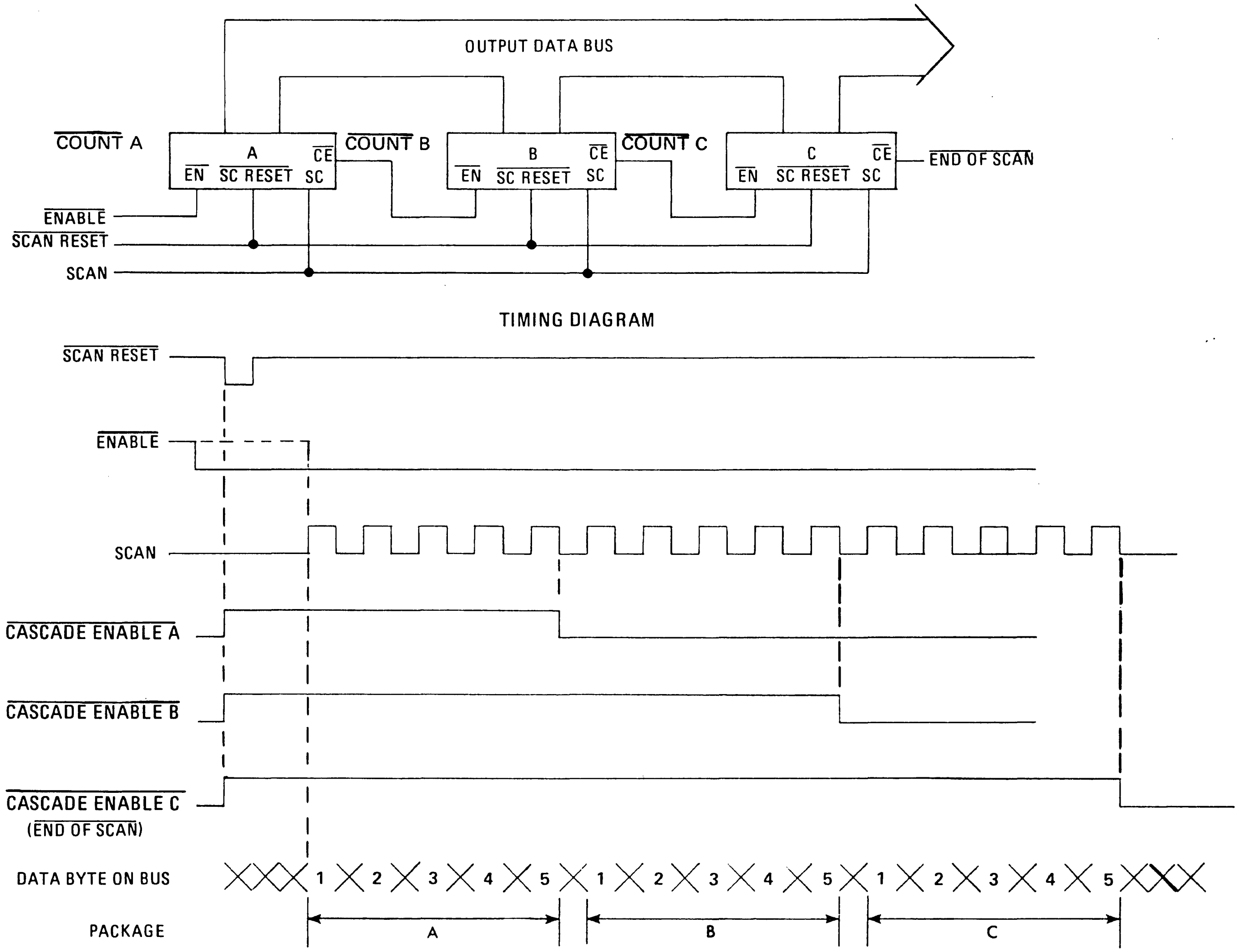
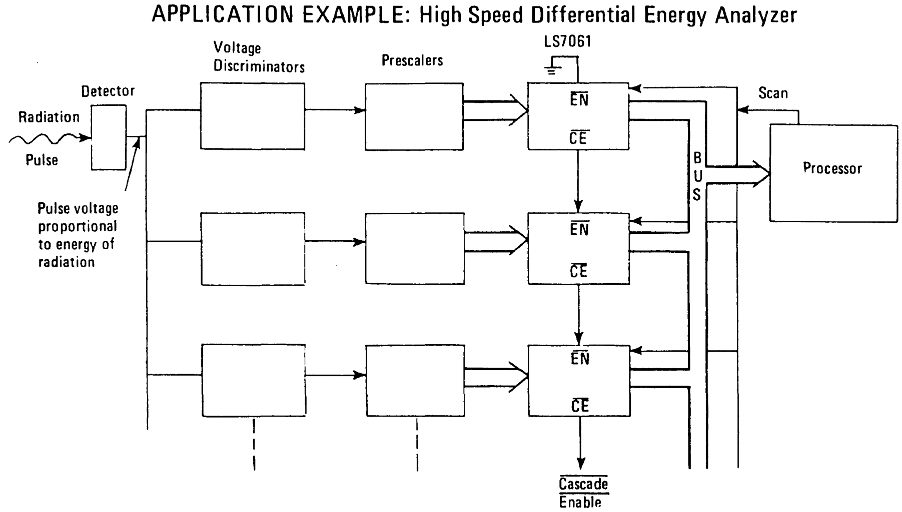


Figure 4

Figure 5

APPLICATION EXAMPLE: High Speed Differential Energy Analyzer



Note: The processor subtracts counts from successive counters to determine the differential energy spectrum.

Figure 6

LSI COMPUTER SYSTEMS INC.

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LSI/CSI

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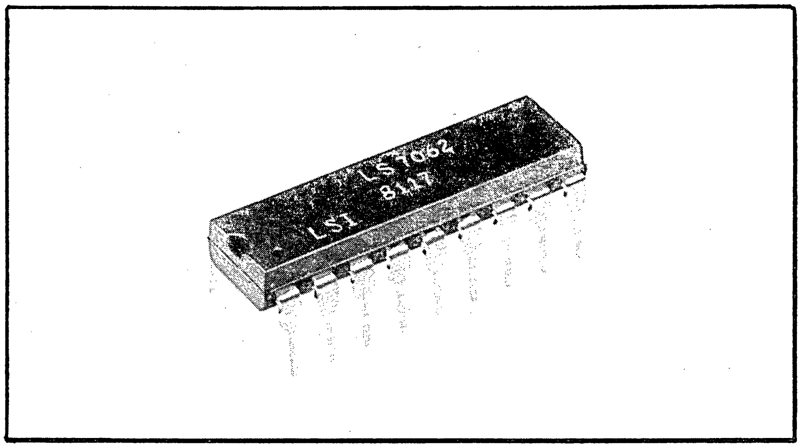
LS7062 | DUAL 16 BIT BINARY UP COUNTER

with 32 Bit Latch, Multiplexer and Three-State Drivers

Revised January 1986

FEATURES:

- DC to 10MHz Count Frequency
- 8 Bit Byte Multiplexer
- DC to 1MHz Scan Frequency
- Single Power Supply Operation, +4.75 VDC to +5.25 VDC
- Three-State Data Outputs, Bus and TTL Compatible
- Inputs TTL, NMOS and CMOS Compatible
- Unique Cascade Feature Allows Multiplexing of Successive Bytes of Data in Sequence in Multiple Counter Systems
- Low Power Dissipation
- All Inputs Protected
- 18 Pin DIP



DESCRIPTION:

The LS7062 is a monolithic, ion implanted MOS dual 16 bit up counter. The circuit includes latches, multiplexer, eight three-stage binary data output drivers and output cascading logic.

DESCRIPTION OF OPERATION:

16 BIT BINARY UP COUNTER

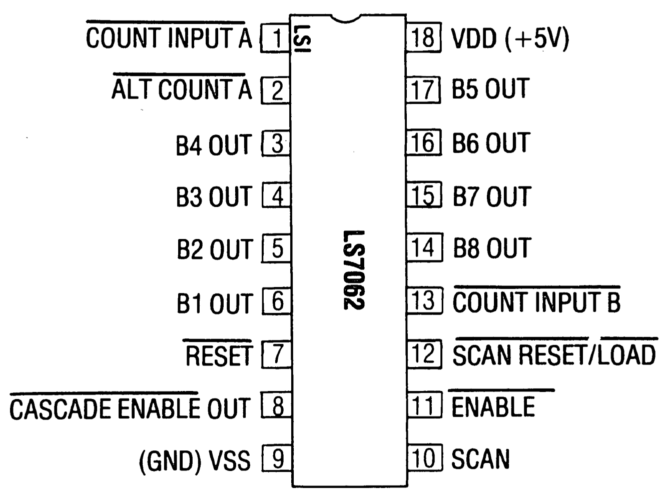
The 16 bit static ripple through counter increments on the negative edge of the input count pulse.
Maximum ripple time is 2μs (transition count of sixteen "ones" to sixteen "zeros").
Guaranteed count frequency is DC to 10 MHz.

$\overline{\text{COUNT INPUT A}}$, $\overline{\text{ALT COUNT A}}$

Input count pulses to the first 16 bit counter may be applied through either of these two inputs. The $\overline{\text{Alt Count A}}$ input circuitry contains a Schmitt trigger network which allows proper counting with "infinitely" long clock edges. A high applied to either of these two inputs inhibits counting.

$\overline{\text{COUNT INPUT B}}$

Count pulses may be applied to the last 16 bits of the binary counter through this input. The counter advances on the negative transition of these pulses.



TOP VIEW
STANDARD 18 PIN DIP
Figure 1

RESET

All 16 counter bits are reset to zero when Reset is brought low for a minimum of 1 us. Reset must be high for a minimum of 300ns before next valid count can be recorded. Count Input B must be held low when reset is brought low to ensure proper reset of Counter B. (See block diagram, figure 7.)

LATCHES

32 bits of latch are provided for storage of counter data. All latches are loaded when the Load input is brought low for a minimum of 1μs and kept low until a minimum of 2μs has elapsed from previous negative edge of count pulse (ripple time).

Storage of valid data occurs when Load is brought high for a minimum of 250ns before next negative edge of count pulse or Reset.

SCAN COUNTER AND DECODER

The scan counter is reset to the least significant byte position (state 1) when Scan Reset input is brought low for a minimum of 1μs. The scan counter is enabled for counting as long as the Enable input is held low. The counter advances to the next significant byte position on each negative transition of the Scan pulse. When the scan counter advances to state 5 it disables the Output Drivers and stops in that state until Scan Reset is again brought low.

SCAN

When the scan counter is enabled, each negative transition of this input advances the scan counter to its next state. When Scan is low the Data Outputs are disabled. When Scan is brought high the Data Outputs are enabled and present the latched counter data corresponding to the present state of the scan counter.
Therefore, in microprocessor applications, the Data Output Bus may be utilized for other activities while new data is propagating to the outputs. This positive Scan pulse can be viewed as a "Place the next byte on my bus" instruction from the microprocessor.
Minimum positive and negative pulse widths of 500ns for the Scan signal are required for scan counter operation.

SCAN RESET/LOAD

When this input is brought low for a minimum of 1μs the scan counter is reset to state 1, least significant byte position, and the latches are simultaneously loaded with new count information.

ENABLE

When this input is high, the scan counter and the Data Outputs are disabled. When Enable is low, the scan counter and Data Outputs are enabled for normal operation. Transition of this input should only be made while the Scan input is in a low state in order to prevent false clocking of the scan counter.

CASCADE ENABLE

The output is normally high. It transitions low and stays low when the scan counter advances to state 5. In a multiple counter system this output is connected to the Enable input of the next counter in the cascading string. The Scan input and Scan Reset/Load input are carried to all the counters in the "Cascade", Counter 1 then presents its bytes of data to

CASCADE ENABLE (cont.)

the output bus on each positive transition of the scan pulse as previously discussed. When state 5 of counter 1 is achieved, counter 2 presents its data to the output bus. This sequence continues until all counters in the cascade have been addressed. See Fig. 4 for an illustration of a 3 device cascade design. This output is TTL, CMOS and NMOS compatible.

THREE-STATE DATA OUTPUT DRIVERS

The eight Data Output Drivers are disabled when either Enable input is hig
Scan input is low.
The Output Drivers are TTL and Bus compatible.

MAXIMUM RATINGS:

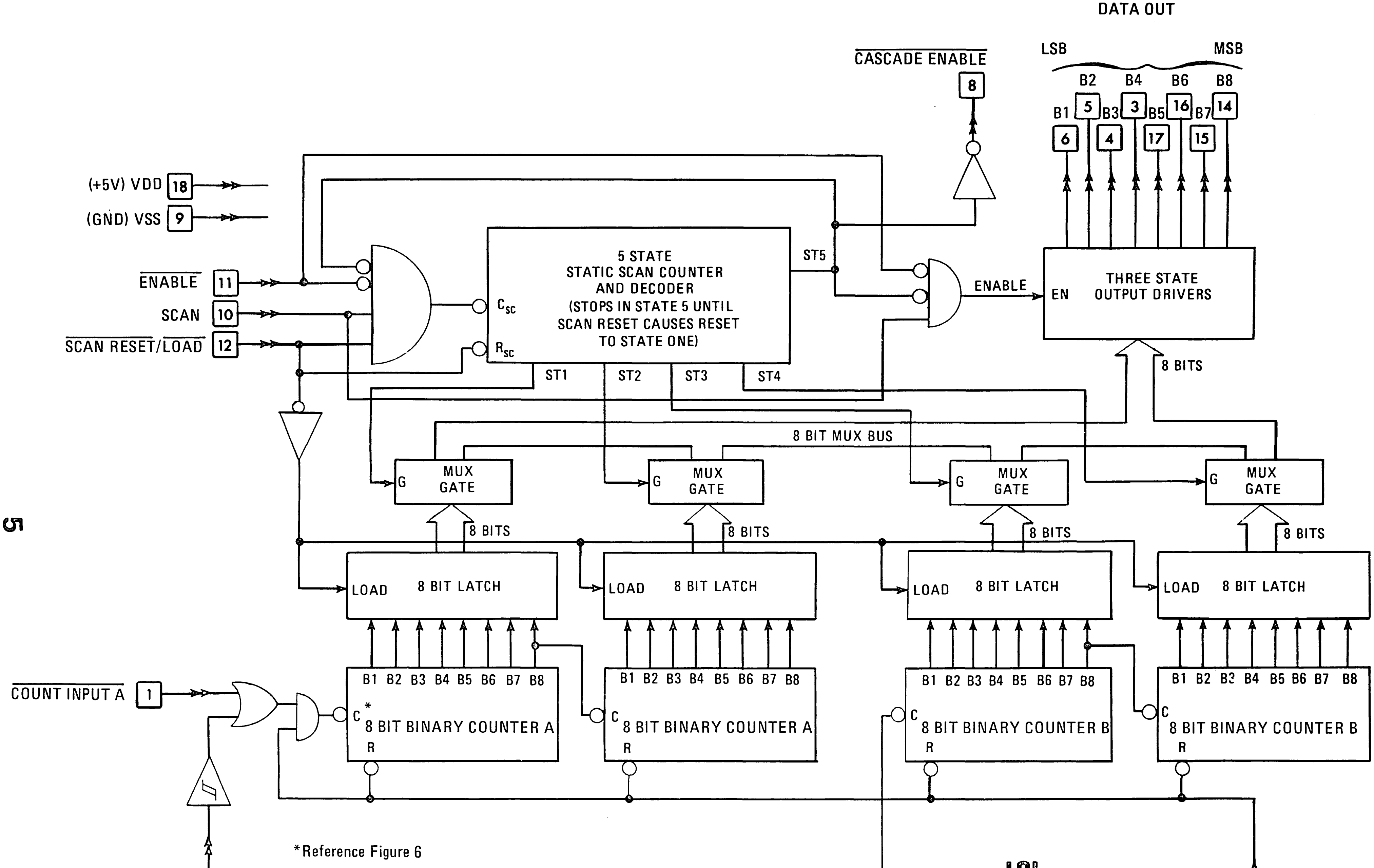
PARAMETER	SYMBOL	VALUE
Storage Temperature	T_{STG}	−55 to +150
Operating Temperature	T_A	0 to +70
Voltage(any pin to VSS)	Vmax	+10 to −0.3

DC ELECTRICAL CHARACTERISTICS

(V_{DD}=+5V±5%, V_{SS}=0V, T_A=0°C to +70°C unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Ur
Power Supply Current	I_{DD}		15	mA
Input High Voltage	V_{IH}	+3.5	V_{DD}	V
Input Low Voltage	V_{IL}	0	+0.6	V
Output High Voltage				
Cascade Enable	V_{OH}	V_{DD}−0.2		V
		+2.4		V
B1 – B8		+2.4		V
		+2.0		V
Output Low Voltage				
Cascade Enable	V_{OL}		+0.2	V
			+0.4	V
B1 – B8			+0.4	V
Output Source Current	Isource	3.0		mA
B1 – B8 Outputs		4.8		mA
		7.3		mA
Output Sink Current	Isink	5.7		mA
B1 – B8 Outputs		4.0		mA
		2.2		mA
Output Leakage Current B1 – B8 (Off State)	I_{OL}		1	μA
Input Capacitance	C_{IN}		6	pF
Output Capacitance	C_{OUT}		12	pF
Input Leakage Current	I_{LI}		1	μA
INPUT CURRENT				
*Scan Reset/Load	I_{IH}		−2.5	μA
	I_{IL}		−5	μA
**Count Input A, Alt Count A	I_{IH}		5	μA
Count Input B	I_{IL}		1	μA

*Input has internal pull-up resistor to V_{DD}
**Inputs have internal pull-down resistor to V_{SS}



LS7062
BLOCK DIAGRAM
FIGURE 7

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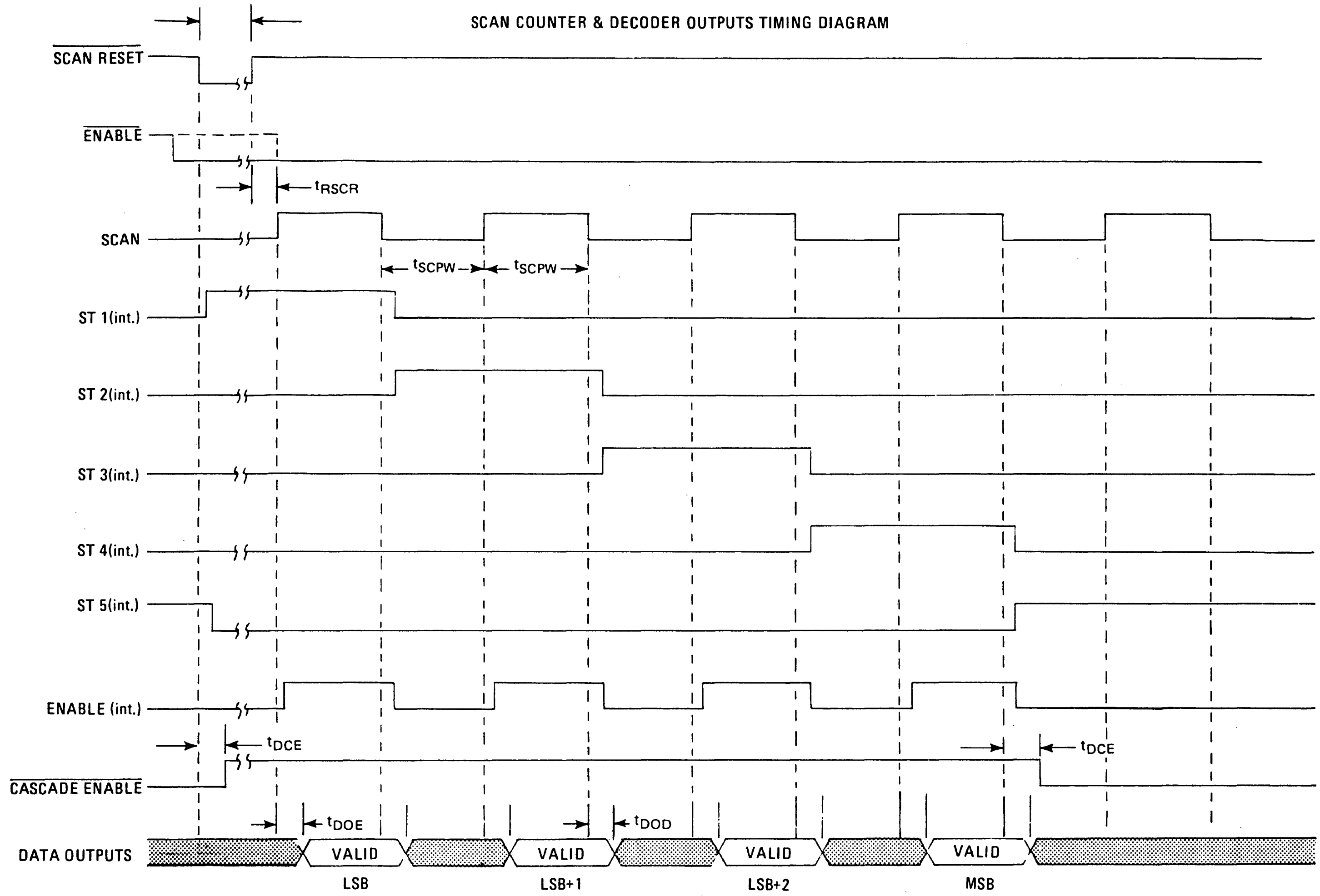


Figure 2

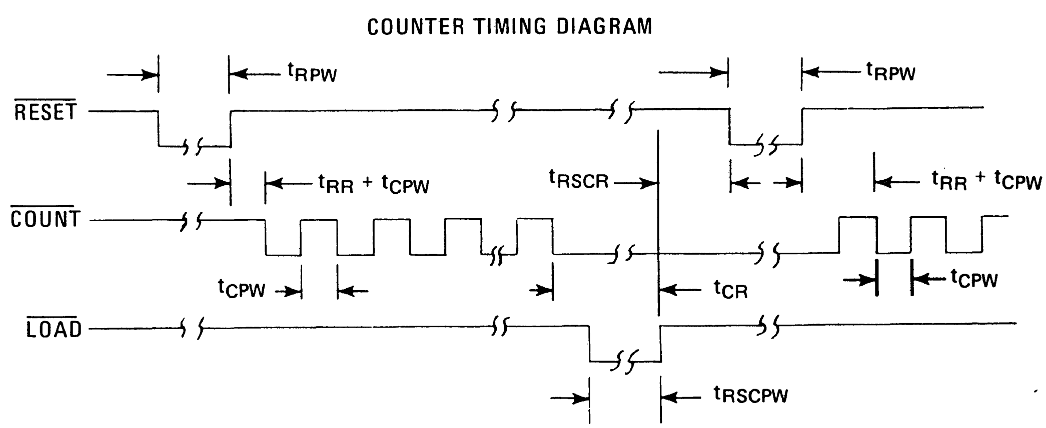


Figure 3

ter is in state 5, or the

ns
ium Operating Frequency,
ax, Outputs No Load

V_{DD}=MIN.
00μA, V_{DD}=MIN.
0μA, V_{DD}=MIN.
0μA, V_{DD}=MIN.
V_{DD}=MIN.
nA, V_{DD}=MIN.
nA, V_{DD}=MIN.
.2V, V_{DD}=MIN.
.8V, V_{DD}=MIN.
.4V, V_{DD}=MIN.
.2V, V_{DD}=MIN.
.8V, V_{DD}=MIN.
.4V, V_{DD}=MIN.
V to +2.4V
MIN.
°C, f=1.0MHz
°C, f=1.0MHz
LE, RESET, SCAN
MAX
MAX, V_{IH}=+3.5
MAX, V_{IL}=0
MAX, V_{IH}=+3.5
MAX, V_{IL}=0

DYNAMIC ELECTRICAL CHARACTERISTICS

(V_{DD}=+5V±5%, V_{SS}=0V, T_A=0°C to +70°C unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Units	Conditions
Count Frequency (Count Input A, Alt Count A, Count Input B)	fc	DC	10	MHz	
Count Pulse Width (All Count Inputs)	t_{CPW}	40		ns	Measured @ 50% point, Max t_r, t_f =10ns
Count Rise & Fall Time (Count Input A, Count Input B)	t_r, t_f		30	μs	
Count Rise & Fall Time (Alt Count A)	t_r, t_f		No Max Limit		
Count Ripple Time (Count Input A, Alt Count A, Count Input B)	t_{CR}		2	μs	Transition from 16 ones to 16 zeros from negative edge of count pulse
Reset Pulse Width (All Counter Stages Fully Reset)	t_{RPW}	500		ns	Measured @ 50% point Max t_r, t_f =200ns
Reset Removal Time (Reset Removed From All Counter Stages)	t_{RR}		250	ns	Measured from Reset signal @ V_{IH}
Scan Frequency	f_{sc}		1	MHz	
Scan Pulse Width	t_{SCPW}	500		ns	Measured @ 50% point Max t_r, t_f =100ns
Scan Reset/Load Pulse Width (All latches loaded and Scan Counter Reset to Least Significant Byte)	t_{RSCPW}	1		μs	Measured @ 50% point Max t_r, t_f =200ns
Scan Reset/Load Removal Time (Reset Removed from Scan Counter; Load Command Removed From Latches)	t_{RSCR}		250	ns	Measured from Scan Reset/Load @ V_{IH}
Output Disable Delay Time (B1 – B8)	t_{DOD}		200	ns	Transistion to Output High Impedance State Measured From Scan @ V_{IL} or Enable @ V_{IH}
Output Enable Delay Time (B1 – B8)	t_{DOE}		200	ns	Transition to Valid On State Measured from Scan @ V_{IH} and Enable @ V_{IL} ; Delay to Valid Data Levels for C_{OL}=10pf and one TTL Load or Valid Data Currents for High Capacitance Loads
Output Delay Time Cascade Enable	t_{DCE}		300	ns	Negative Transition from Scan @V_{IL} and ST5 of Scan Counter or Positive Transition From Scan Reset/Load @ V_{IL} to Valid Data Levels for C_{OL}=10pf and one TTL Load

Refer to page 4 for timing diagrams.

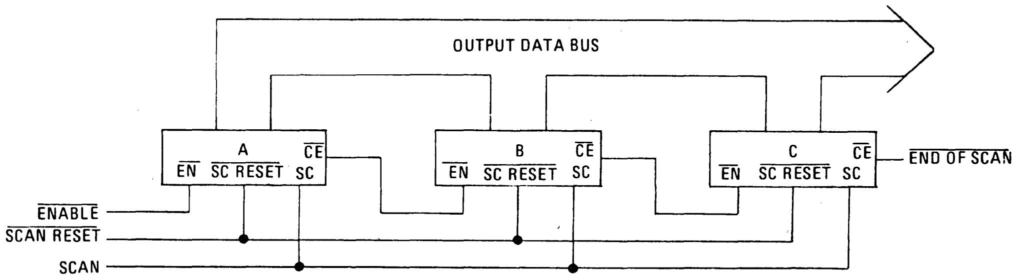
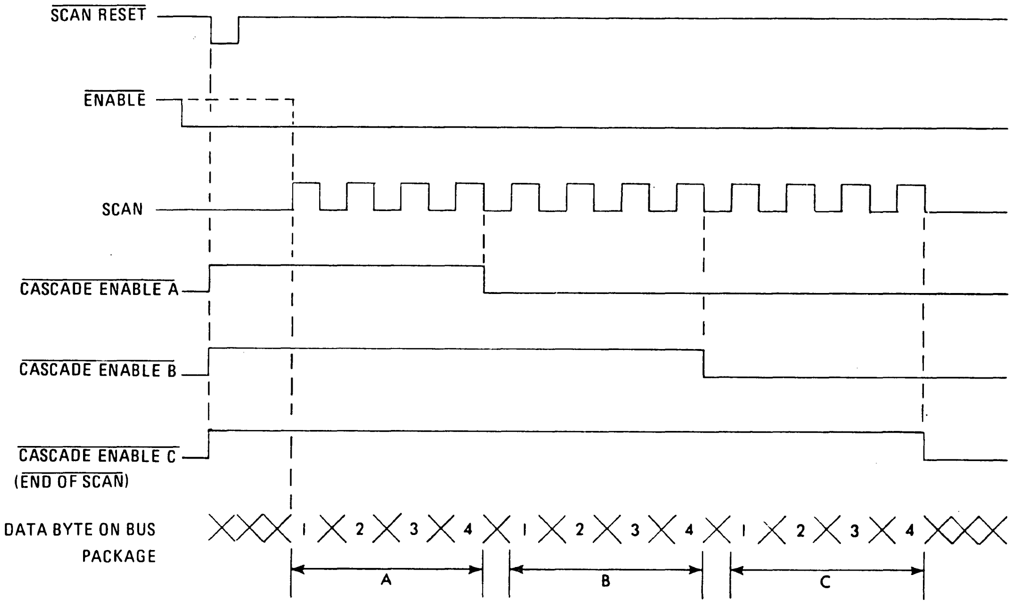


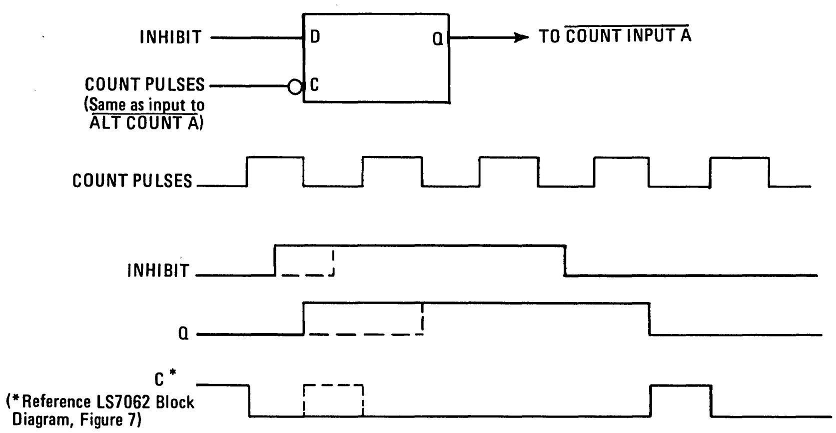
ILLUSTRATION OF A 3 DEVICE CASCADE

FIGURE 4



TIMING DIAGRAM

FIGURE 5



NOTE: Count Input A may only change during positive portion of Count Pulses (Alt Count A) when Count Input A is used as an Inhibit.

SYNCHRONIZING INHIBIT WITH COUNT PULSES FOR COUNTER A

FIGURE 6

LSI/CSI

LS7066

24 BIT MULTIMODE COUNTER

FEATURES:

- Microprocessor Compatible Three State I/O Bus.
- Programmable modes are: Binary, BCD, 24 hour clock up, down, ÷ N, x4 quadrature and single cycle. These modes can co-exist in different combinations.
- DC to 4 MHz
- 24-Bit comparator for pre-set count comparsion.
- Readable status register.
- Input/Output TTL compatible.
- Single +5VDC power supply.
- 20 pin Plastic Dip.

GENERAL DESCRIPTION

The LS7066 is a monolithic, ion implanted MOS 24-bit counter that can be programmed to operate in several different modes. The operating mode is set up by writing control words into internal control registers (see figure 8). There are three 6-bit and one 2-bit control registers for setting up the circuit functional characteristics. In addition to the control registers, there is a 5-bit output status register (OSR) that indicates the current counter status. The LS7066 communicates with external circuits through an 8-bit three state I/O bus. Control and data words are written into the LS7066 through the bus. In addition to the I/O bus, there are a number of discrete inputs and outputs to facilitate instantaneous hardware based control functions and instantaneous status indication.

REGISTER DESCRIPTION

The following hardware registers are addressable through the I/O bus. The addressing modes of these registers are listed in Table 1.

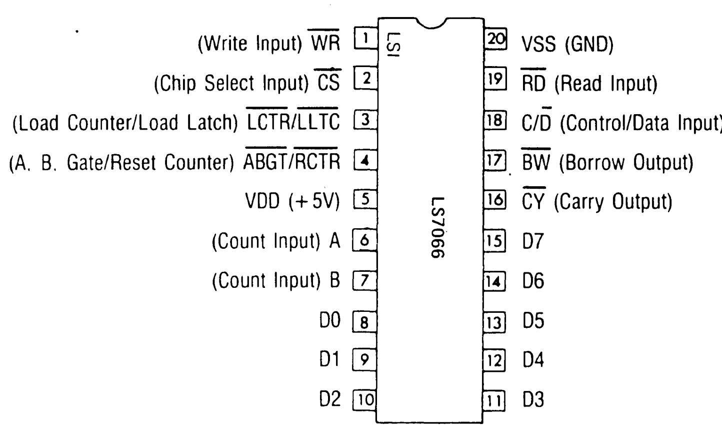
Output Status Register (OSR). The OSR is a 5-bit read only register that holds the counter status information at any given time. When read, the OSR bit 0 through 4 are placed on the I/O bus, D0 through D4 respectively. The OSR bits contain the status information as follows:

Bit 0: Borrow toggle flip-flop (BWT). This flip-flop changes state every time the counter (CNTR) underflows.

Bit 1: Carry toggle flip-flop (CYT). This flip-flop changes state every time the CNTR overflows.

Bit 2: Compare toggle flip-flop (COMPT). This flip-flop changes state every time CNTR equals to preset register (PRO-PR2).

CONNECTION DIAGRAM — TOP VIEW
STANDARD 20 PIN PLASTIC DIP



Bit 3: Sign register. The sign register is set to "1" whenever CNTR underflows indicating that a borrow has taken place. It resets to "0" when CNTR overflows indicating a carry. This register is also reset whenever CNTR is reset.

Bit 4: UP/DN Indicator. In quadrature mode, when set to "1," this bit indicates that the counter is operating in the UP count mode. When reset to "0," it indicates that the counter is in DOWN count mode. When not in quadrature mode this bit is forced to a "1."

Preset Register (PR). The preset register is made of three 8-bit registers, PR0, PR1 and PR2, in concatenation to make one 24-bit register. Data is written into the 3 individual registers with one register being addressed at a time. The 24-bit data can then be transferred into the CNTR all at once.

Output Latch (OL). The output latch is a 24-bit register made of three 8-bit registers OL0, OL1 and OL2. Data from the CNTR can be transferred all at once into the OL. OL0, OL1 and OL2 can then be individually addressed to be read on the I/O bus.

Master Control Register (MCR). The MCR is a 6-bit write only register. A control word written into the MCR sets up the chip characteristics in the following manner:

D0 = 1: Resets the PR/OL address counter.
D1 = 1: Loads the OL with the CNTR value.
D2 = 1: Resets the CNTR borrow toggle flip-flop, the carry toggle flip-flop and the sign register.
D3 = 1: Loads the CNTR with the PR value.
D4 = 1: Resets the compare toggle flip-flop.
D5 = 1: Master reset. The master reset presets the PR to all "1's" and resets the following: the CNTR, all control registers (excepting the MCR), the OL and the OSR. Note that a master reset overrides D1 and D3.

Input Control Register (ICR). The ICR is a 6-bit write only register that controls the operating modes of the 4 discrete inputs called A, B, $\overline{ABGT}/\overline{RCTR}$ and $\overline{LCTR}/\overline{LLTC}$. A counter decrement or increment may also be caused by writing the proper control word into the ICR. The functions of the different bits of the control word are as follows:

D0 = 0: Sets up A as up count input and B as down count input.
D0 = 1: Sets up A as the count input and B as the count up/down direction control input. (See note 1)
D1 = 1: Increments CNTR once. (See note 2)
D2 = 1: Decrements CNTR once.(See note 2)
D3 = 0: Disables inputs A and B.
D3 = 1: Enables inputs A and B.
D4 = 0: $\overline{ABGT}/\overline{RCTR}$ input is set up as the counter external reset input.
D4 = 1: $\overline{ABGT}/\overline{RCTR}$ input is set up as the A and B enable/disable gate.
D5 = 0: $\overline{LCTR}/\overline{LLTC}$ input is set up as the external load command input for the CNTR.
D5 = 1: $\overline{LCTR}/\overline{LLTC}$ input is set up as the external load command input for the OL.

NOTE 1: When B is Setup as UP/DN control input, B may switch only when A is high.

NOTE 2: When incrementing or decrementing the CNTR by writing into the ICR, inputs A and B, if enabled, must be held high.

Output/Counter Control Register (OCCR). The OCCR is a 6-bit write only register. A control word written into the OCCR sets up the counter and the output characteristics in the following manner:

D0 = 0: Sets counter to binary mode.
D0 = 1: Sets counter to BCD mode.
D1 = 1: Sets counter to non-recycle mode. In this mode, the counter counts for only one cycle beginning with a counter "reset" or "load" command and ending with the generation of a carry or a borrow. Following that, the counter is inhibited until a new reset or load command is applied.
D2 = 1: Sets counter to divide by N mode.
D3 = 1: Sets counter to 24 hour clock mode.(See note 3)
D4, D5: These two bits control the $\overline{CY}$ and $\overline{BW}$ output lines as follows:

D5	**D4**	
0	0	Enables active low carry and borrow on $\overline{CY}$ and $\overline{BW}$ respectively.
0	1	Enables the carry and borrow toggle flip-flops on $\overline{CY}$ and $\overline{BW}$ respectively.
1	0	Enables active high carry and borrow on $\overline{CY}$ and $\overline{BW}$ respectively.
1	1	Enables comparator output on $\overline{CY}$ and compare toggle flip-flop on $\overline{BW}$ respectively.

NOTE 3: 24 hour mode overrides binary or BCD mode.

Quadrature Register (QR). The QR is a 2-bit register that enables inputs A and B to count in the X4 quadrature mode. In this mode, "A clocks" leading "B clocks," generate internal up clocks whereas "B clocks" leading "A clocks" generate internal down clocks.

An internal clock is generated for every transition of either A or B clock. The QR Control word assignment is as follows:

D0 = 0: Disables quadrature mode
D0 , D1 = 1 Enables quadrature mode

TABLE 1 - Register Addressing Modes

D7	D6	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	COMMENT
X	X	X	X	X	1	Disable Chip.
0	0	1	1	‾_‾	0	Write to Master Control Register (MCR).
0	1	1	1	‾_‾	0	Write to input control register (ICR).
1	0	1	1	‾_‾	0	Write to output/counter control register (OCCR).
1	1	1	1	‾_‾	0	Write to quadrature register (QR).
X	X	0	1	‾_‾	0	Write to preset register (PR) and increment register address counter. (See note 4)
X	X	0	‾_‾	1	0	Read output latch (OL) and increment register address counter. (See note 4)
X	X	1	‾_‾	1	0	Read output status register (OSR).

X = irrelevant

‾_‾ = Negative Pulse

NOTE 4: Following any control read/write operation a data Read/Write sequence must be preceded by an "Address Counter" reset instruction.

I/O Description: (See register description for I/O Programming.)

DataBus (D0-D7) (Pin 8-Pin 15). The 8-line data bus is a three-state I/O bus for interfacing with the system bus.

$\overline{CS}$ (Chip Select Input) (Pin 2). A logical "0" at this input enables the chip for Read and Write.

$\overline{RD}$ (Read Input) (Pin 19). A logical "0" at this input enables the OSR and the OL to be read on the data bus.

$\overline{WR}$ (Write Input) (Pin 1) A logical "0" at this input enables the data bus to be written into the control and data registers.

C/$\overline{D}$ (Control/Data Input) (Pin 18). A logical "1" at this input enables a control word to be written into one of the four control registers or, the OSR to be read on the I/O bus. A logical "0" on the other hand enables a data word to be written into the PR, or the OL to be read on the I/O bus.

A (Pin 6). Input A is a programmable count input capable of functioning in three different modes, such as, up count input, down count input and quadrature input.

B (Pin 7). Input B is also a programmable count input that can be programmed to function either as down count input, or count direction control gate for input A, or quadrature input. When B is programmed as count direction control gate, B = 0 enables A as the UP Count input and B = 1 enables A as the DN Count input.

$\overline{ABGT}$/$\overline{RCTR}$ (Pin 4) This input may be programmed to function as either inputs A and B enable gate or as external counter reset input. A logical "0" is the active level on this input.

$\overline{LCTR}$/$\overline{LLTC}$ (Pin 3) This input can be programmed to function as the external load command input for either the counter or the OL. When programmed as counter load input, the counter is loaded with the data contained in the PR. When programmed as the OL load input, the OL is loaded with the data contained in the counter. A logical "0" is the active level on this input.

$\overline{CY}$ (Pin 16). 'his output pin can be programmed to serve as one of the following:

A. $\overline{CY}$. True carry out (active "0").
B. CY. Complemented carry out (active "1").
C. CYT. Carry toggle flip-flip out.
D. $\overline{COMP}$. Comparator out (active "0").

$\overline{BW}$ (Pin 17). This output can be programmed to serve as one of the following:

A. $\overline{BW}$. True Borrow out (active "0").
B. BW. Complemented borrow out (active "1").
C. BWT. Borrow toggle flip-flop out.
D. COMPT. Compare toggle flip-flop out.

VDD (Pin 5). Supply voltage positive terminal.

VSS (Pin 20). Supply voltage negative terminal.

Absolute Maximum Ratings:

Parameter	Value	Units
Voltage at any pin with respect to VSS	−0.5 to 12	Volts
Operating Temperature	0 to +70	°C
Storage Temperature	−65 to +150	°C

DC Electrical Characteristics. (All voltages referenced to VSS. Unless otherwise specified, VDD = 5V.)

Parameter	Symbol	Min. Value	Max. Value	Unit	Remarks
Supply Voltage	VDD	4.75	5.5	Volts	–
Supply Current	IDD	20	35	mA	–
Input Low Voltage	V_{IL}	–	0.8	Volts	–
Input High Voltage	V_{IH}	2.0	–	Volts	–
Output Low Voltage	V_{OL}	–	0.4	Volts	@ 4mA Sink
Output High Voltage	V_{OH}	2.5	–	Volts	@ 200ua Source
Input Current	–	–	15	nA	Leakage Current
Output Source Current	I_{SRC}	200	–	uA	@V_{OH} = 2.5 V
Output Sink Current	I_{SNK}	4	–	mA	@ V_{OL} = 0.4 V
Data Bus Off-State Leakage Current	–	–	15	nA	

TRANSIENT CHARACTERISTICS. (See timing Diagrams in Fig. 2 through Fig. 7.)

Parameter	Symbol	Min. Value	Max. Value	Unit
Clock A/B "Low"	Tcl	125	–	ns
Clock A/B "High"	Tch	125	–	ns
Clock A/B Frequency (see note 5)	fc	–	4	MHz
Clock UP/DN Reversal Delay	Tudd	125	–	ns
$\overline{LCTR}$ Positive edge to the next A/B positive OR negative edge delay	T_{LC}	125	–	ns
Clock A/B to $\overline{CY}$/$\overline{BW}$/$\overline{COMP}$ "low" propagation delay	T_{CBL}		160	ns
Clock A/B to $\overline{CY}$/$\overline{BW}$/$\overline{COMP}$ "high" propagation delay	T_{CBH}		350	ns
$\overline{LCTR}$ and $\overline{LLTC}$ pulse width	T_{LCW}	70	–	ns
Clock A/B to CYT, BWT and COMPT "high" propagation delay	T_{TFH}		300	ns
Clock A/B to CYT, BWT and COMP "low" propagation delay	T_{TFL}		300	ns
$\overline{WR}$ pulse width	T_{WW}	400	–	ns
$\overline{RD}$ to data out delay	T_{RD}		400	ns
$\overline{WR}$ to $\overline{WR}$/$\overline{RD}$ Delay (See note 6)	T_{WD}	800	—	ns
Data set-up time for $\overline{WR}$	T_{DS}	0	–	–
Data hold time for $\overline{WR}$	T_{DH}	10	–	ns
$\overline{CS}$, C/$\overline{D}$ set-up time for $\overline{RD}$	T_{CRS}	0	–	ns
$\overline{CS}$, C/$\overline{D}$ hold time for $\overline{RD}$	T_{CRH}	10	–	ns
$\overline{CS}$, C/$\overline{D}$ set-up time for $\overline{WR}$	T_{CWS}	0	–	ns
$\overline{CS}$, hold time for $\overline{WR}$	T_{CWH}	10	–	ns
Quadrature Clock				
Clock A/B "low"	T_{CLQ}	1500	–	ns
Clock A/B "high"	T_{CHQ}	1500	–	ns
A and B phase delay	T_{PH}	750	–	ns
Clock A/B frequency	f_{CQ}	–	333	KHz

NOTE 5: In divide by N mode, the maximum clock frequency is 3MHZ.

NOTE 6: If a write to the LS7066 is followed by a RD/WR with TWD < 800 ns, erroneous data could be written into the LS7066 even if the second RD/WR was not directed to the LS7066. For systems with TWD<800ns, the LS7066 RD/WR inputs must be gated with $\overline{CS}$ input as shown in fig. 9.

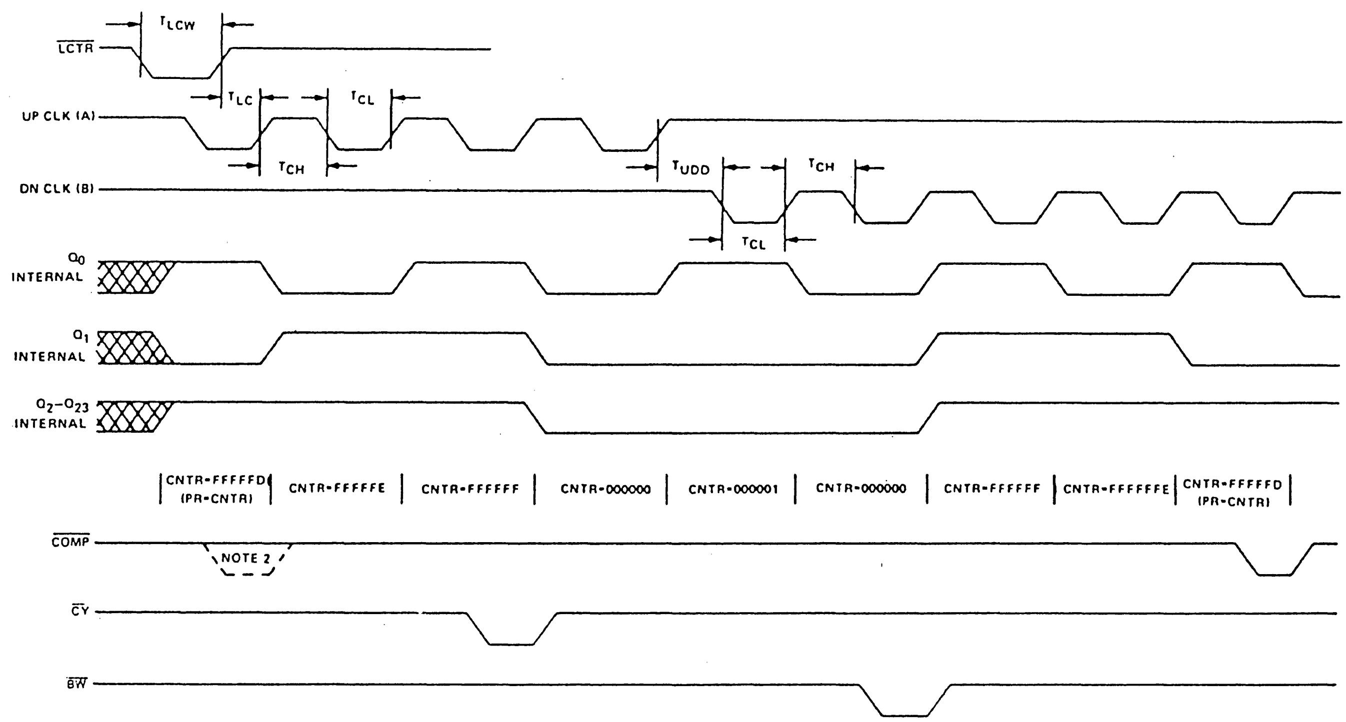


FIGURE 2 - LOAD COUNTER, UP CLOCK, DOWN CLOCK, COMPARE OUT, CARRY, BORROW

Note 1: The counter in this example, is assumed to be operating in the binary mode.

Note 2: No COMP output is generated here, although PR=CNTR. COMP output is disabled with a counter load command and enabled with the rising edge of the next clock, thus eliminating invalid COMP outputs whenever the CNTR is loaded from the PR.

Note 3: When up Clock is active, the DN clock should be held "HIGH" and vice verse.

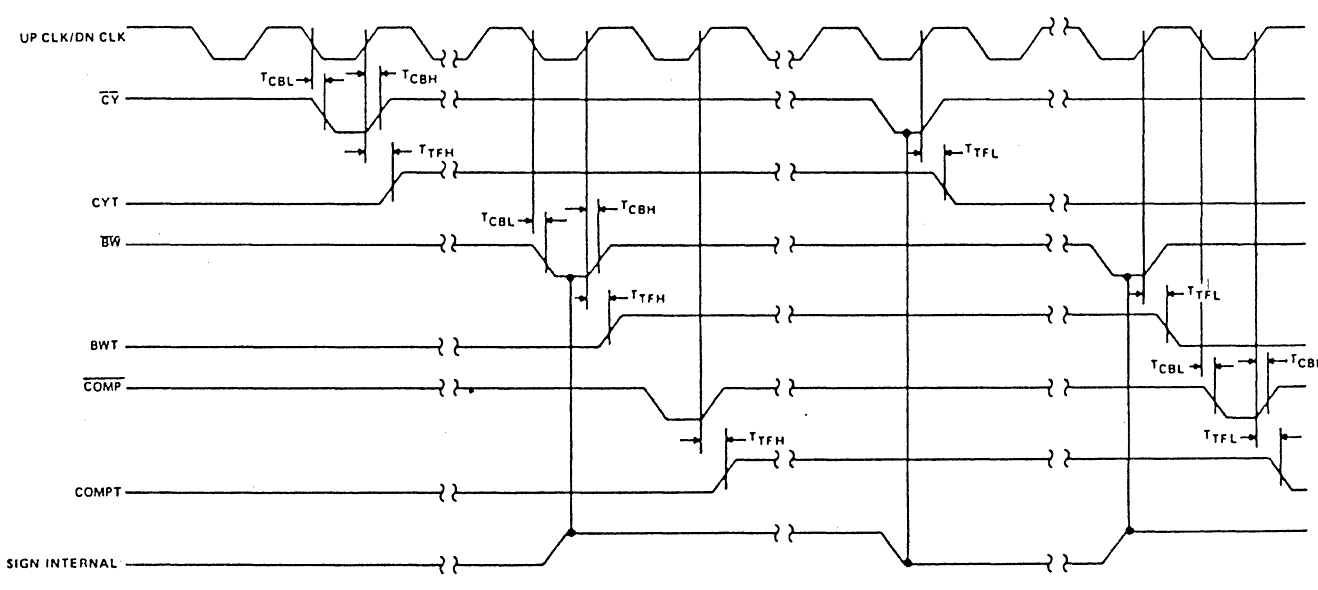


FIGURE 3 — CLOCK TO $\overline{CY}/\overline{BW}$ OUTPUT PROPAGATION DELAYS

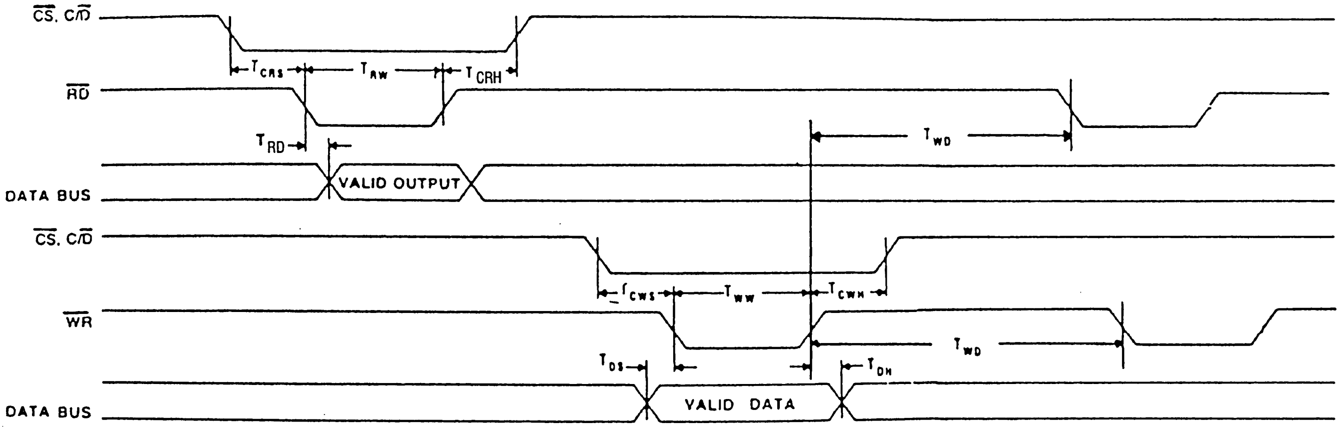
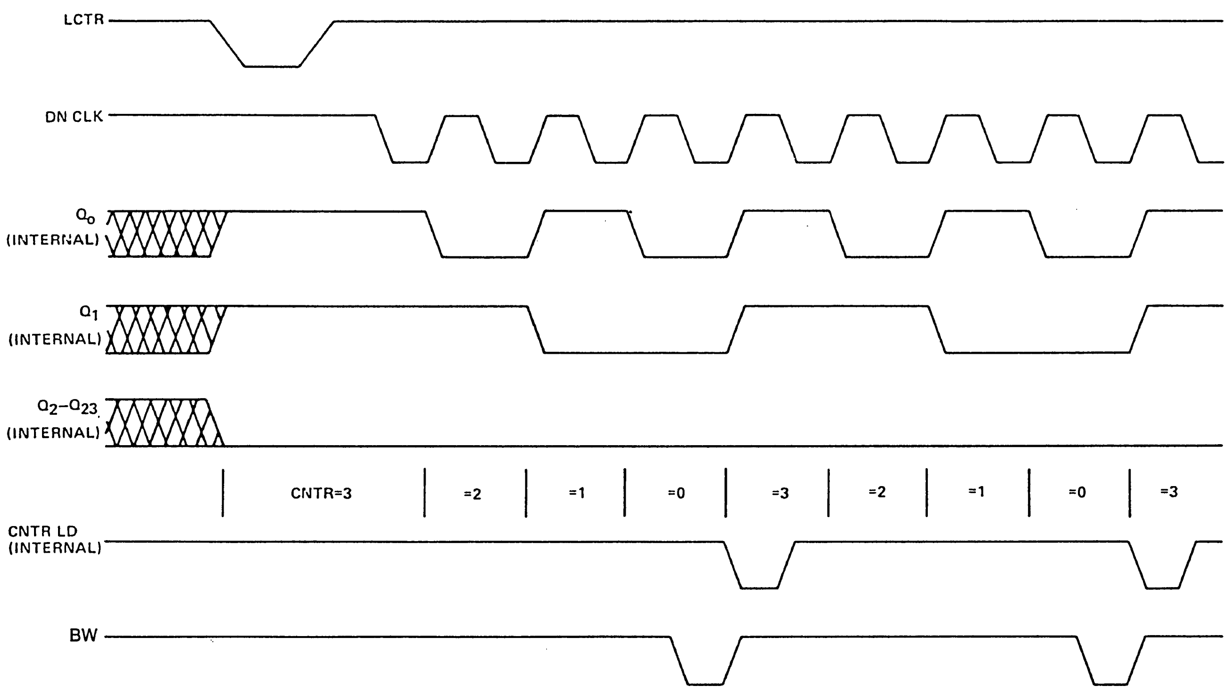


FIGURE 4 — READ/WRITE CYCLES



NOTE: EXAMPLE OF DIVIDE BY 4 IN DOWN COUNT MODE.

FIGURE 5 - DIVIDE BY N MODE

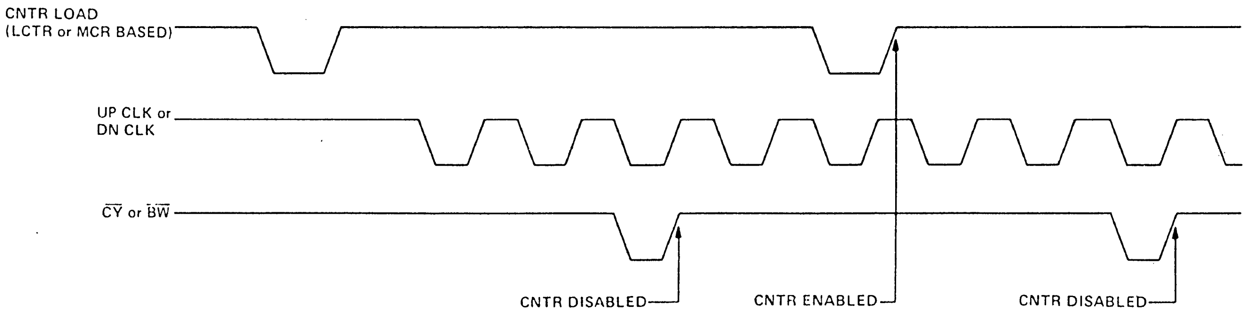


FIGURE 6 - CYCLE ONCE MODE

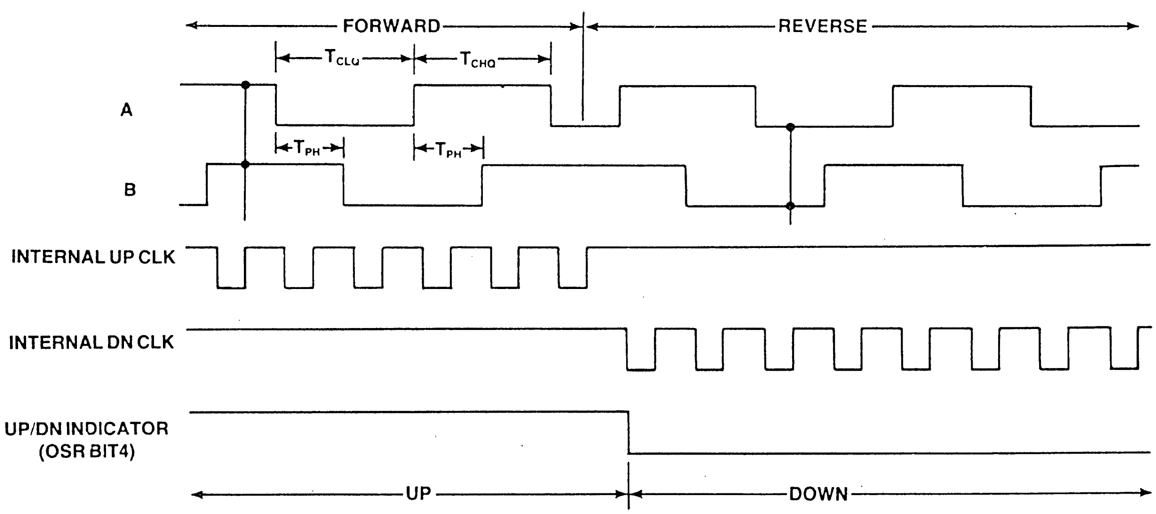


FIGURE 7 – QUADRATURE MODE

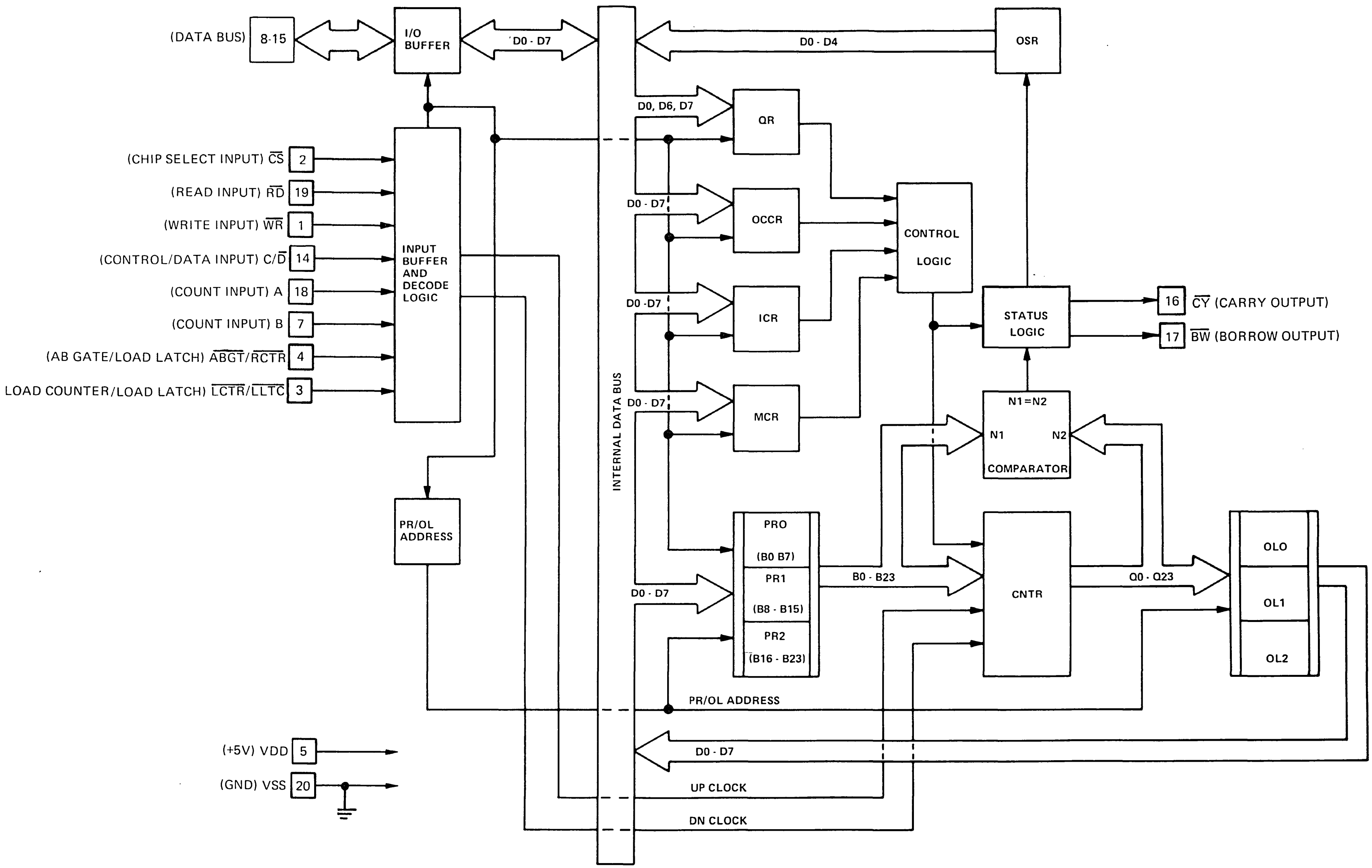
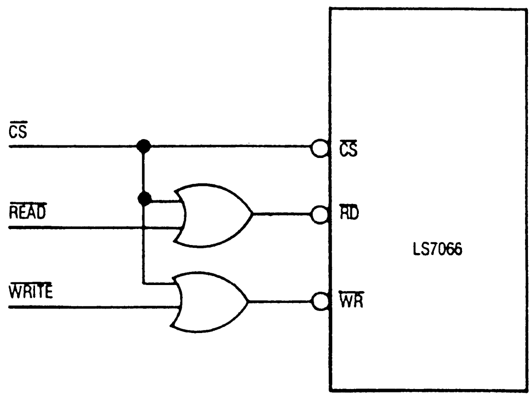


FIGURE 8 — LS7066 BLOCK DIAGRAM



$\overline{CS}$
$\overline{READ}$
$\overline{WRITE}$
$\overline{CS}$
$\overline{RD}$
$\overline{WR}$
LS7066

FIGURE 9

LSI COMPUTER SYSTEMS INC.

Manufacturers of Custom and Standard LSI Circuits
1235 Walt Whitman Road, Melville, NY 11747
TWX: (510) 226-7833 FAX: 516 271 0405
Telephone: (516) 271-0400

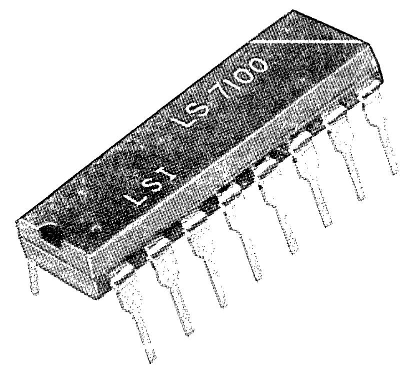
LS7100 | BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

for liquid crystal (dynamic scattering) displays

Revised January 1986

FEATURES:

- Up to −50V Segment Output
- All Inputs are TTL or CMOS Compatible
- Internal Pull-Down Resistors on all Inputs
- Operating Voltage Range From −5V to −60V



DESCRIPTION:

The LS7100 is a monolithic, ion implanted MOS, BCD to 7-segment latched decoder/driver capable of driving displays over a wide voltage range.

This circuit is specifically intended to drive large light scattering liquid crystal displays.

DESCRIPTION OF OPERATION:

COMMON (COM) INPUT

COM is the common source for 7 internal FET Switch segment outputs.

A, B, C, D AND LOAD (LD) INPUTS

The BCD (or binary) data applied to the A,B,C,D inputs are latched into internal flip-flops when the LD input is high. If the input data changes while LD is high, the flip-flops will follow the input data. When LD is low, the inputs are isolated from the flip-flops. The latched data are decoded to 7-segments to control the opening and closing of the segment switch outputs (See display format for 0-15 binary decoding).

Each of these inputs has an internal pull-down (to logic "0") resistor.

SEGMENT OUTPUTS

The segment outputs are open-drain outputs of FET switches, with COM input as the common source. The electrical path from COM to any segment output is effectively an analog switch which can be either closed or opened by decoded data stored in internal latches associated with A,B,C,D inputs. The display segment drive wave-forms are not generated internally. The desired output wave-forms must be applied to the COM input. When a segment analog switch is closed, the drive wave-form at COM is connected to the respective output and when the switch is open, the output is cut off from COM and has very high impedance.

PIN ASSIGNMENT DIAGRAM

LOAD DISPLAY IN, LD	1	16	V_{SS} (+)
C	2	15	g
B	3	14	f
D	4	13	e
A	5	12	d
COMMON, COM	6	11	c
BLANKING IN, BI	7	10	b
(−) V_{DD}	8	9	a

TOP VIEW
STANDARD 16 PIN DIP
FIGURE 1

BLANKING (BI) INPUT

Blanking of the display is provided by the BI. When BI is high, all FET switches are opened thereby turning off display segments. When BI is low, the selected FET switches are closed.

BI has an internal pull-down (to logic "0") resistor.

INPUT INTERFACE

LS7100 inputs can be interfaced with TTL, CMOS, NMOS or PMOS outputs by connecting VSS to the positive terminal (output logic "1", reference supply) of the TTL, CMOS, NMOS or PMOS supply.

ABSOLUTE MAXIMUM RATINGS:

(All voltages referenced to V_{SS}, Pin 16)

	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD}	+0.3 to −60	V
Common In	V_{CI}	+0.3 to −60	V
All other inputs	V_{IN}	+0.3 to −30	V
Operating Temperature	T_A	−40 to +70	^oC
Storage Temperature	Tstg	−65 to +125	^oC

ELECTRICAL CHARACTERISTICS:

$-40^oC \leq T_A \leq 70^oC$ unless otherwise specified

$V_{SS} = 0$ unless otherwise specified

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS, REMARKS
POWER SUPPLY					
V_{DD}	−5	–	−60	V	
I_{DD}	–	600	–	μA	@$V_{DD} = -40V$
COMMON INPUT					
V_{COM} High	–	−.5	0	V	
V_{COM} Low	V_{DD}+3	V_{DD}+10	–	V	
V_{COM} Low $-V_{SS}$	–	–	−50	V	
Leakage Current	–	–	5	nA	@$V_{DD} = -40V$, $V_{DD} + 3V < V_{COM} \leq -0.5V$
ALL OTHER INPUTS					
Input High Voltage V_{IH}, "1"	−1.5	–	0	V	
Input Low Voltage V_{IL}, "0"	V_{DD}	–	−4	V	$V_{DD} \geq -15V$
	−15	–	−4	V	$V_{DD} < -15V$
Input High Current I_{IH}	–	–	40	μA	$T_A = 25^oC$
Input Low Current I_{IL}	–	–	40	μA	$T_A = 25^oC$
SEGMENT OUTPUTS					
OFF Segment Leakage Current	–	5	–	nA	@$V_{DD} = -40V$, $V_{DD} + 3V < V_{SEG} \leq -0.5V$
ON Segment Output Current	–	–	5	mA	Maximum recommended

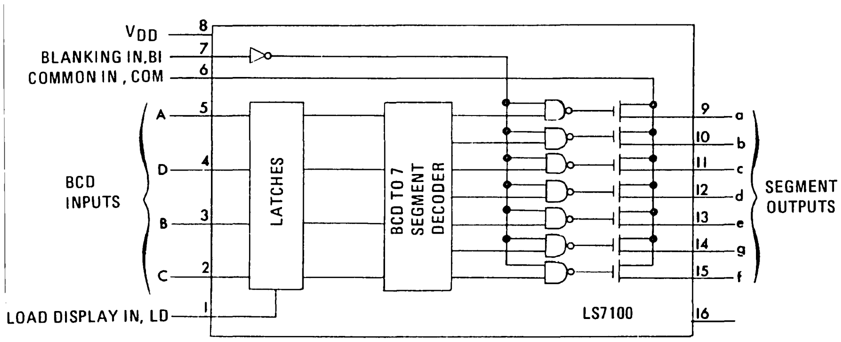
SWITCHING CHARACTERISTICS*

$V_{DD} = -40V$, $T_A = 25^oC$

(Outputs unloaded)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BCD data set up time	t_{DS}	0	–	–	ns
BCD data hold time	t_{HS}	500	–	–	ns
Load pulse width	t_{LW}	1.0	–	–	μs
BCD data pulse width	t_{DW}	1.5	–	–	μs
Blank to seg off delay	t_{PBH}	–	1.0	–	μs
Blank to seg on delay	t_{PBL}	–	1.3	–	μs
Load to seg on delay	t_{PLH}	–	1.5	–	μs
Load to seg off dealy	t_{PLL}	–	1.0	–	μs
Propagation delay from COM input to any segment output	–	–	–	300	ns

*See Figure 3.



LS7100 FUNCTIONAL DIAGRAM
FIGURE 2

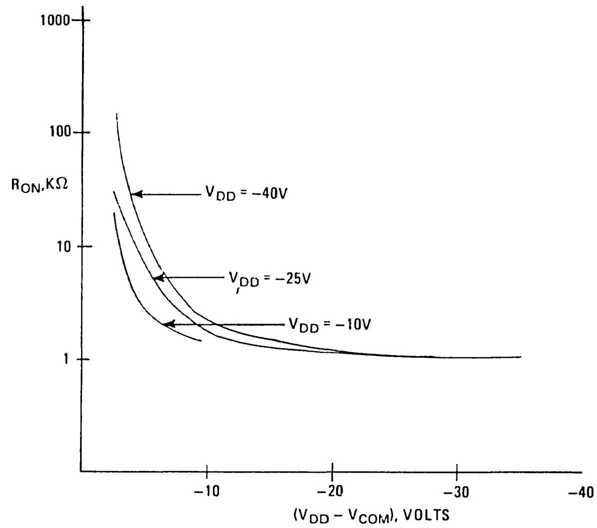
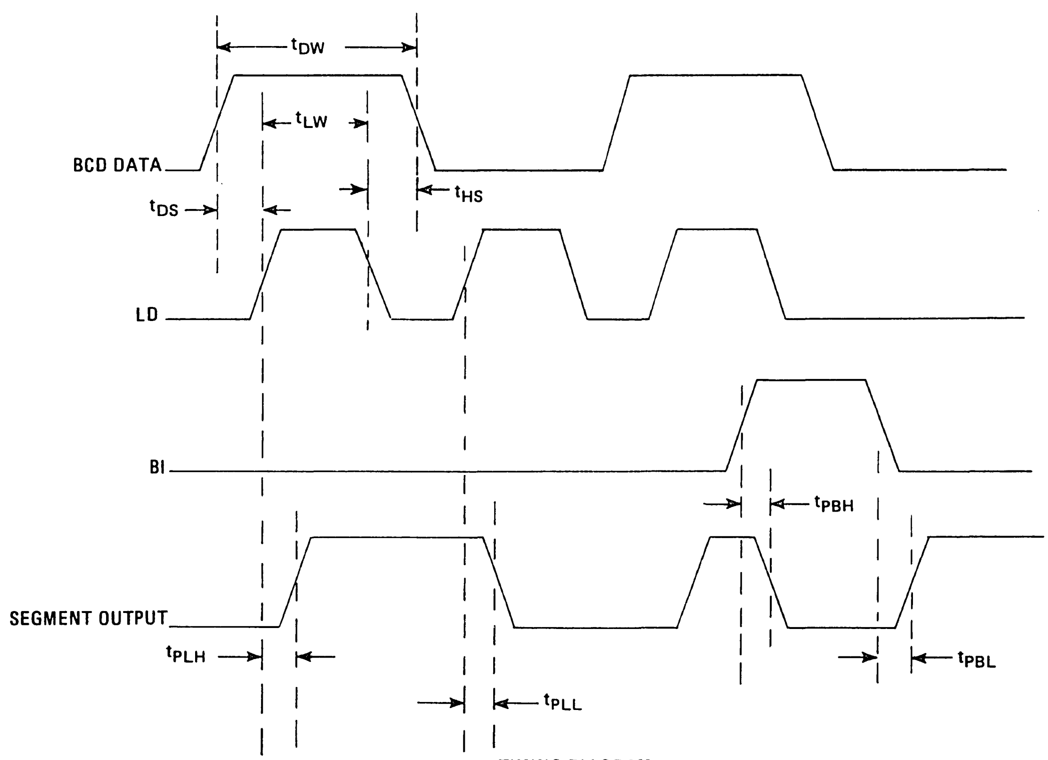


FIGURE 4
CHANNEL ON RESISTANCE, R_{ON}



TIMING DIAGRAM
FIGURE 3

DISPLAY FORMAT

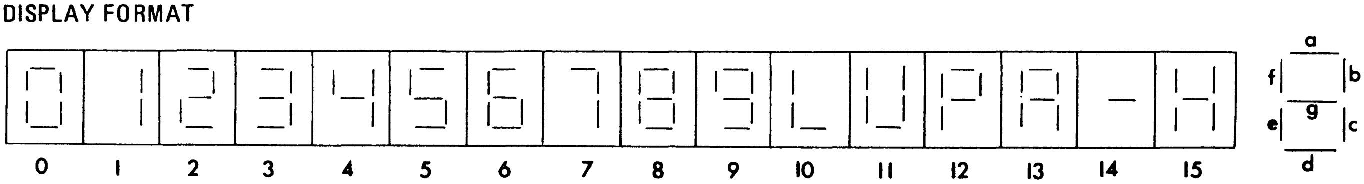
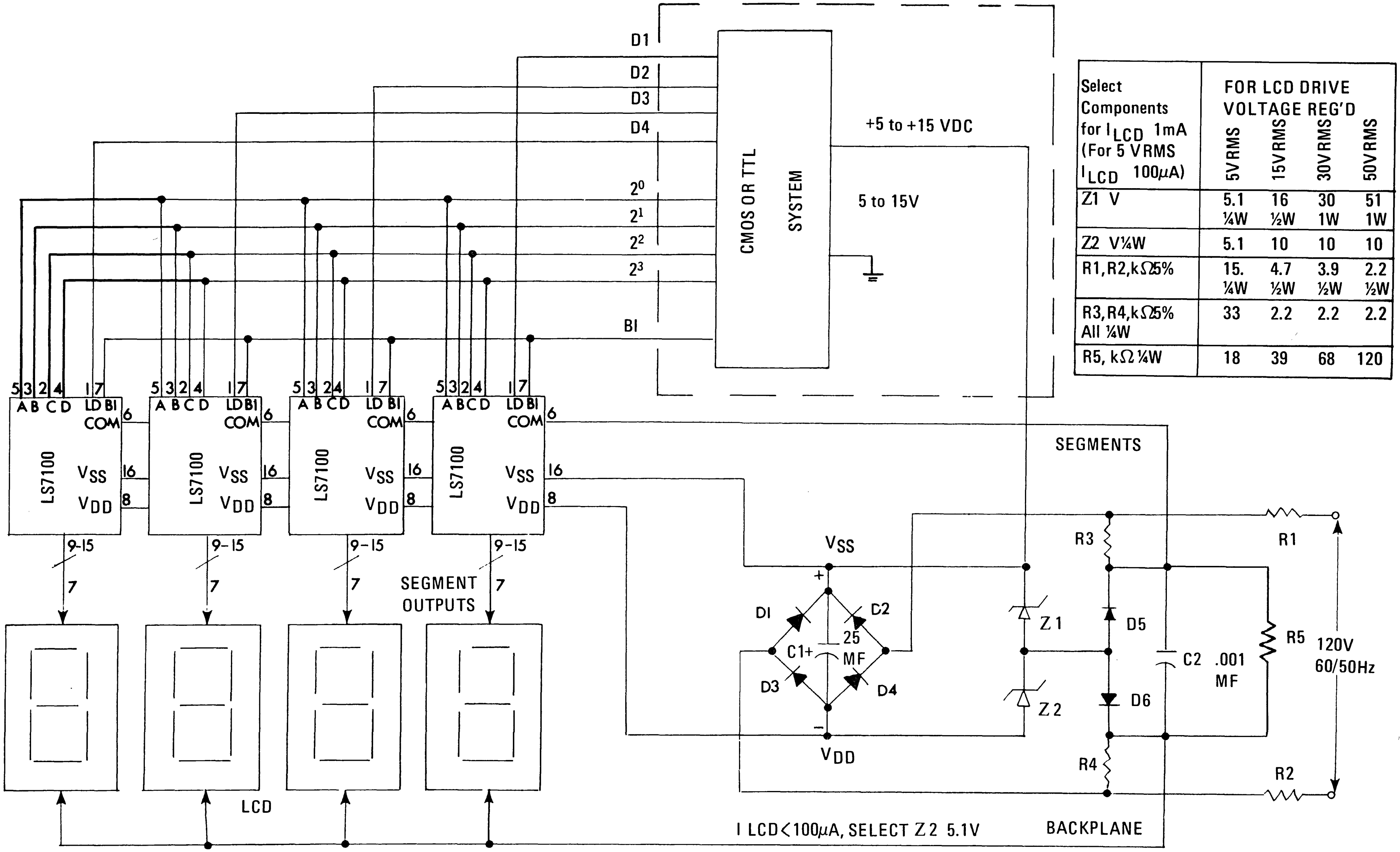


FIGURE 5



Select Components for I_{LCD} 1mA (For 5 VRMS I_{LCD} 100µA)	FOR LCD DRIVE VOLTAGE REG'D 5VRMS	15VRMS	30VRMS	50VRMS
Z1 V	5.1 ¼W	16 ½W	30 1W	51 1W
Z2 V¼W	5.1	10	10	10
R1,R2,kΩ5%	15. ¼W	4.7 ½W	3.9 ½W	2.2 ½W
R3,R4,kΩ5% All ¼W	33	2.2	2.2	2.2
R5, kΩ ¼W	18	39	68	120

APPLICATION NOTE – 4 DIGIT LCD DRIVE USING LS7100
(from 120 V-AC line)

FIGURE 6

4

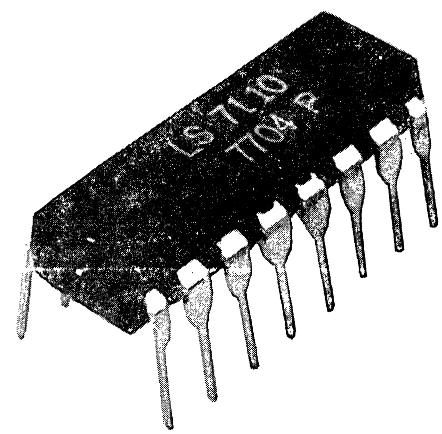
LSI COMPUTER SYSTEMS INC.

Manufacturers of Custom and Standard LSI Circuits
1235 Walt Whitman Road, Melville, NY 11747
TWX: (510) 226-7833 FAX: 516 271 0405
Telephone: (516) 271-0400

LS7110 | Binary Addressable Latched 8 Channel Demultiplexer/Driver

for liquid crystal (dynamic scattering) displays

MARCH 1981



FEATURES:

- Up to −50 Volts Output
- All Inputs are TTL and CMOS Compatible
- Internal Pull-Down Resistors on all Inputs
- Operating Voltage Range From −5V to −60V

DESCRIPTION:

The LS7110 is a monolithic, ion implanted PMOS demultiplexer/driver. It has 8 binary addressable latched output channels capable of driving loads over a wide voltage range. The circuit is intended to drive large light scattering liquid crystal displays.

INPUT/OUTPUT DESCRIPTION: (See Figure 3.)

DESCRIPTION OF OPERATION:

COMMON (COM) INPUT

COM is the common source for 8 FET-switch channel outputs.

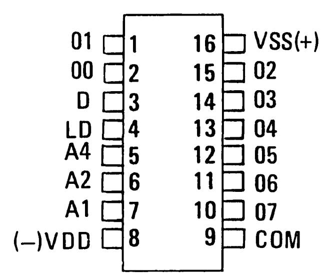
DATA (D) AND LOAD (LD) INPUTS

Data applied to the D input is loaded into one of eight internal flip-flops when the LD input is high. If input data changes while LD is high, the flip-flops will also change accordingly. When LD is low, the flip-flops are isolated from the D input. The output of each flip-flop drives one of the channel output (O) FET switches. A logical "1" at the D input turns the selected switch ON (switch closed) and a "0" turns the switch OFF (switch open circuited). Both of these inputs have internal pull-down (to logic "0") resistors.

CHANNEL OUTPUTS (00 through 07)

The eight channel outputs are open-drain outputs of FET switches with COM input as the common source. The electrical path from the COM to any of the channel outputs is effectively an analog switch which is closed or opened by the associated flip-flop output. The channel output wave forms are not generated internally. The desired output wave form must be applied to the COM input.
The channel outputs are bidirectional in nature, so that any channel output can also be used as an input. In such usage however, the COM input has to be floated or used as an output.

PIN ASSIGNMENT DIAGRAM



TOP VIEW
STANDARD 16 PIN DIP
FIGURE 1

INPUT INTERFACE

LS7110 inputs can be interfaced with TTL, CMOS, NMOS, or PMOS outputs by connecting V_{SS} to the positive terminal of the TTL, CMOS, NMOS or PMOS supply.

ABSOLUTE MAXIMUM RATINGS:

(All voltages referenced to V_{SS}, Pin 16)

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	V_{DD}	+.3 to −60	V
Common In	V_{CI}	+.3 to −60	V
All other inputs	V_{IN}	+.3 to −30	V
Operating Temperature	T_A	−40 to +85	^{0}C
Storage Temperature	T_{stg}	−65 to +125	^{0}C

ELECTRICAL CHARACTERISTICS:

$-40^0C \le T_A \le 85^0C$ unless otherwise specified.

$V_{SS} = 0$ unless otherwise specified.

$V_{DD} = -40$ unless otherwise specified.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS, REMARKS
Supply Voltage	V_{DD}	−5	–	−60	V	
Supply Current	I_{DD}	–	1.0	–	mA	@$V_{DD} = -40$
Common IN HI Vltg	V_{CIH}	–	V_{SS}−.5	V_{SS}	V	
Common IN LO Vltg	V_{CIL}	V_{DD}+3	V_{DD}+10	–	V	
$V_{CIL} - V_{SS}$	–	–	–	−50	V	
Common IN Leakage Current	–	–	–	5	nA	@$V_{DD} = -40V$, $V_{DD} + 3V \le V_{CI} \le V_{SS}$
ALL OTHER INPUTS:						
Input HI Vltg	V_{IH}	V_{SS}−1.5	–	V_{SS}	V	
Input LO Vltg	V_{IL}	V_{DD}	–	V_{SS}−4	V	@$V_{DD} \ge -15V$
		V_{SS}−15	–	V_{SS}−4	V	@$V_{DD} < -15V$
Input HI Current	I_{IH}	–	–	40	μA	@$T_A = 25^0C$
Input LO Current	I_{IL}	–	–	40	μA	@$T_A = 25^0C$
CHANNEL OUTPUT (O):						
Off Channel Leakage Current	I_{OL}	–	–	5	nA	
On Channel Source Current@V_{CI} =0	I_{OS}	100	–	–	μA	@$V_{CIH} - V_{OC}$ = 0.15V
		1	–	–	mA	@$V_{CIH} - V_{OC}$ = 1.5V
		5	–	–	mA	@$V_{CIH} - V_{OC}$ = 6.0V
		10	–	–	mA	@$V_{CIH} - V_{OC}$ =14.0V
On Channel Source Current @$V_{CI} = V_{DD}$+10V	I_{OS}	100	–	–	μA	@$V_{CI} - V_{OC}$ =0.4V
		500	–	–	μA	@$V_{CI} - V_{OC}$ =2.5V
		900	–	–	μA	@$V_{CI} - V_{OC}$ =10V
Common Input to Channel Output Voltage Drop @V_{CI} =0	$V_{CI} - V_{OC}$	1.5	–	–	V	@I_{OC} =1mA
		6.0	–	–	V	@I_{OC} =5mA
Common Input to Channel Output Voltage Drop @$V_{CI} = V_{DD}$+10V	$V_{CI} - V_{OC}$	0.4	–	–	V	@I_{OC} =100μA
		2.5	–	–	V	@I_{OC} =500μA

NOTE: Maximum recommended source current, I_{OS} max = 5mA.

SWITCHING CHARACTERISTICS: (See Fig. 4, see note below)

$V_{SS} = 0$, $V_{DD} = -40V$, $T_A = 25^oC$ unless otherwise specified.

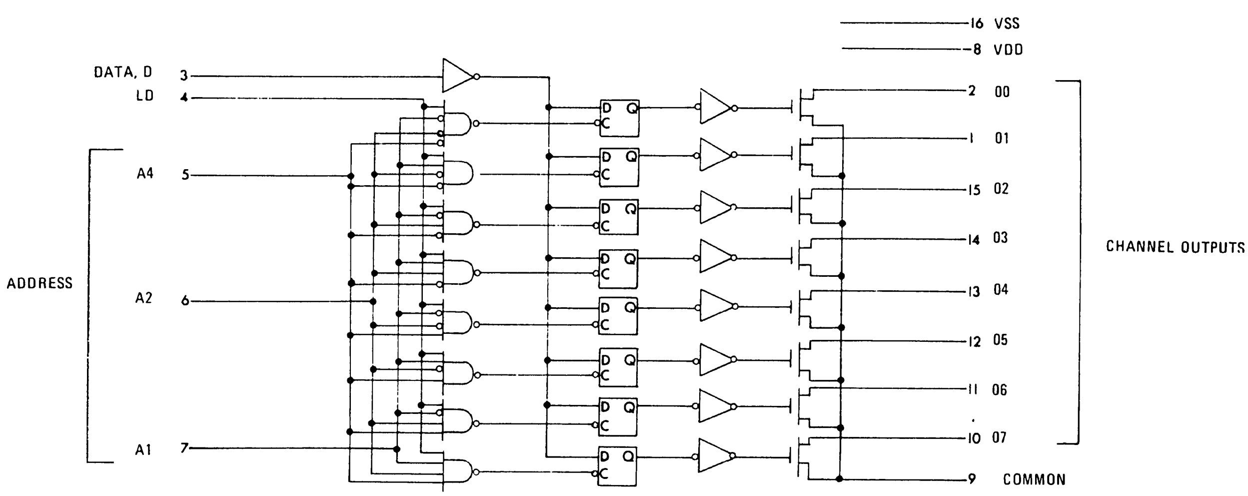
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Address Set-Up Time	t_{AS}	0	–	–	–
Address Hold Time	t_{AH}	600	–	–	nS
Data Set-Up Time	t_{DS}	0	–	–	–
Data Hold Time	t_{DH}	500	–	–	nS
Load Pulse Width	t_{LW}	800	–	–	nS
Address Pulse Width	t_{AW}	1.5	–	–	μs
Data Pulse Width	t_{DW}	1.3	–	–	μs
Turn-On Propagation Delay	t_{PN}	–	1.5	–	μs
Turn-Off Propagation Dealy	t_{PF}	–	1.0	–	μs
Propagation Delay From V_{COM} to Channel Out	t_{IO}	–	–	300	nS

NOTE: Channel outputs unloaded.

TRUTH TABLE FOR OUTPUT SELECTION

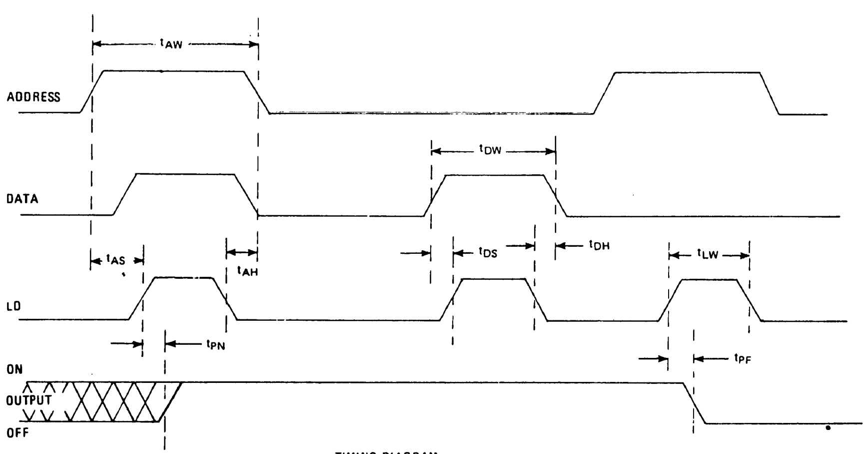
D	A4	A2	A1	LD	07	06	05	04	03	02	01	00
x	x	x	x	0	x	x	x	x	x	x	x	x
0	0	0	0	1	x	x	x	x	x	x	x	Off
1	0	0	0	1	x	x	x	x	x	x	x	On
0	0	0	1	1	x	x	x	x	x	x	Off	x
1	0	0	1	1	x	x	x	x	x	x	On	x
0	0	1	0	1	x	x	x	x	x	Off	x	x
1	0	1	0	1	x	x	x	x	x	On	x	x
0	0	1	1	1	x	x	x	x	Off	x	x	x
1	0	1	1	1	x	x	x	x	On	x	x	x
0	1	0	0	1	x	x	x	Off	x	x	x	x
1	1	0	0	1	x	x	x	On	x	x	x	x
0	1	0	1	1	x	x	Off	x	x	x	x	x
1	1	0	1	1	x	x	On	x	x	x	x	x
0	1	1	0	1	x	Off	x	x	x	x	x	x
1	1	1	0	1	x	On	x	x	x	x	x	x
0	1	1	1	1	Off	x	x	x	x	x	x	x
1	1	1	1	1	On	x	x	x	x	x	x	x

FIGURE 2



FUNCTIONAL DIAGRAM

FIGURE 3



TIMING DIAGRAM

FIGURE 4

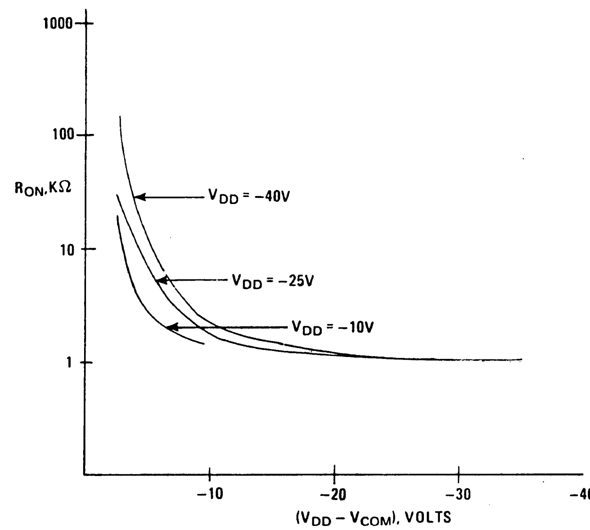
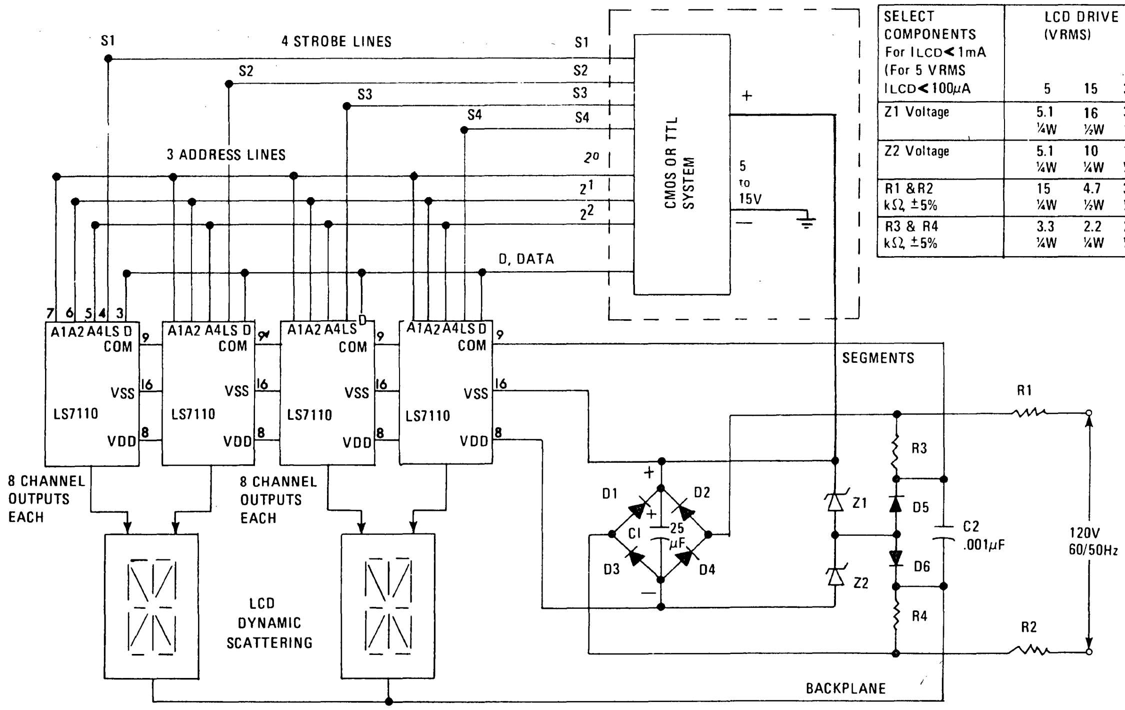


FIGURE 5

CHANNEL ON RESISTANCE, R_{ON}

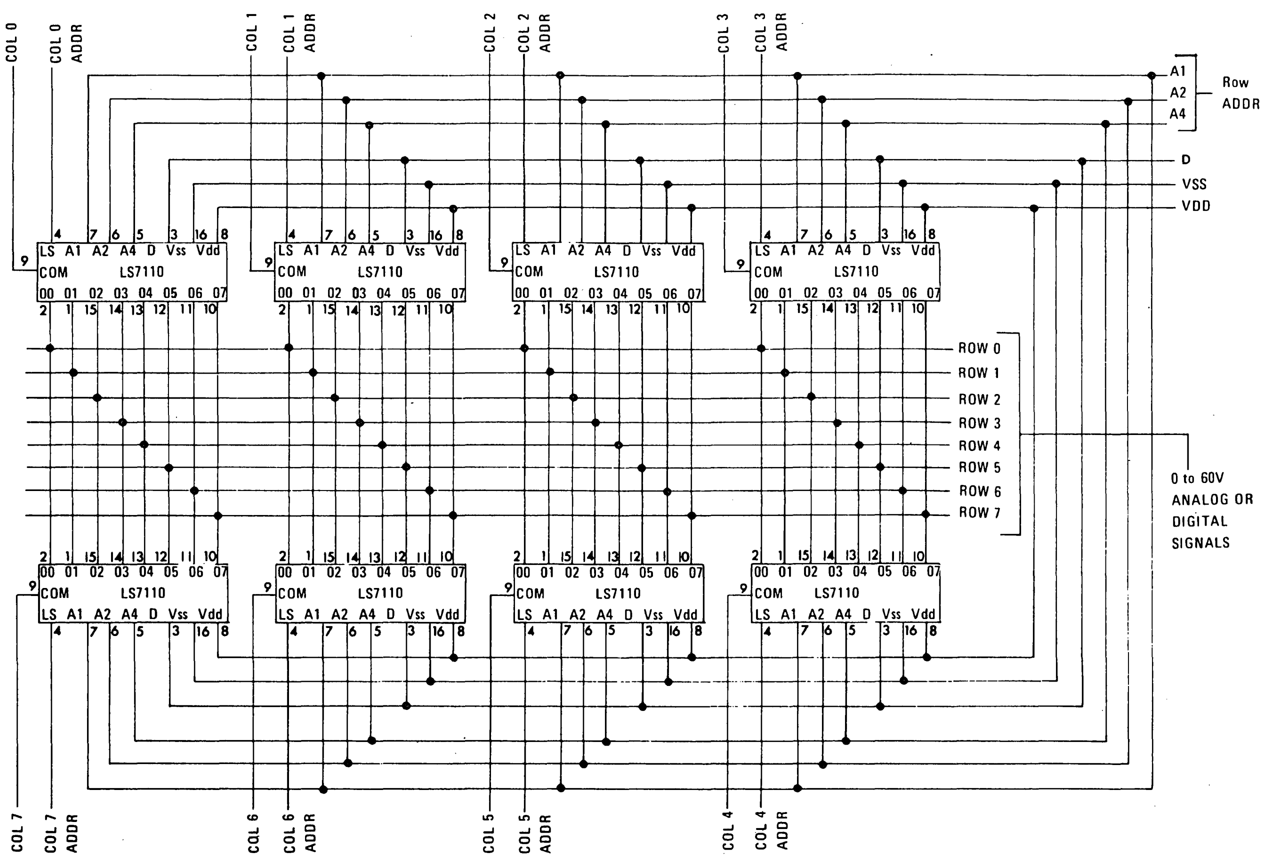


SELECT COMPONENTS For ILCD< 1mA (For 5 VRMS ILCD< 100µA	LCD DRIVE (VRMS) 5	15	30	50
Z1 Voltage	5.1 ¼W	16 ½W	30 1W	51 1W
Z2 Voltage	5.1 ¼W	10 ¼W	10 ¼W	10 ¼W
R1 & R2 kΩ, ±5%	15 ¼W	4.7 ½W	3.9 ½W	2.2 ½W
R3 & R4 kΩ, ±5%	3.3 ¼W	2.2 ¼W	2.2 ¼W	2.2 ¼W

ILCD 100µA, SELECT Z2 = 5.1V
ILCD 1mA, SELECT Z2 = 10V
ILCD 3mA, SELECT Z2 = 15V

APPLICATION NOTE:
2 Character Alpha-Numeric LCD Drive Using LS7110
(From 120 Vac Line)

FIGURE 6



APPLICATION NOTE: 8 x 8 SWITCHBOARD MATRIX USING LS7110

FIGURE 7

LSI/CSI

Manufacturers of Custom and Standard LSI Circuits
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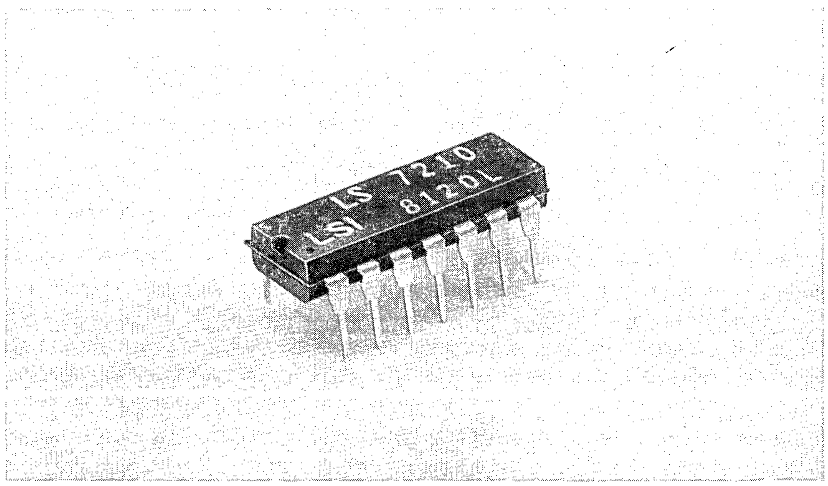
LS7210 PROGRAMMABLE DIGITAL DELAY TIMER

REVISED OCTOBER 1987

FEATURES:

- Programmable Delay from Miliseconds to Hours
- Can be Cascaded for Sequential Events or Extended Delay
- Single Power Supply Operation +4.75V to +15V
- On Chip Oscillator
- Alternate Clock Input
- On Chip Power On Reset
- Internal Pull-ups on Inputs
- Frequency Range to 160 KHz
- CMOS Type Noise Immunity on All Inputs
- All Inputs are CMOS, PMOS & TTL Compatible



DESCRIPTION:

The LS7210 is a monolithic, ion implanted MOS programmable digital timer that can generate a delay in the range of 6ms to infinity. The delay is programmed by 5 binary weighted input bits in combination with the oscillator provided. The chip can be operated into 4 different modes: delayed operate, delayed release, dual delay and one-shot. These modes are selected by the control inputs A & B.

INPUT/OUTPUT DESCRIPTION:

OSCILLATOR INPUT

The frequency of the internal oscillator is set by an RC network connected to the OSC input, as shown in Figure 2. The R and C values for different frequencies is given in Table 3.

EXTERNAL CLOCK INPUT

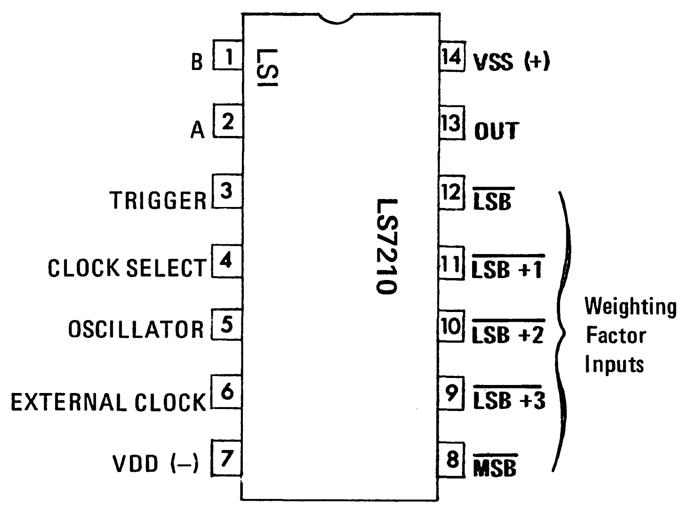
If the internal oscillator is not used, the chip can be driven by an external clock applied to this input.

CLOCK SELECT INPUT

The internal oscillator or the external clock is selected by the proper logical level applied to this input. A logic "1" selects the external clock and logic "0" selects the internal oscillator. The clock select input has an internal pull up resistor.

TRIGGER INPUT

A positive or a negative transition at the trigger input initiates a delay in turning on or off the output. A negative transition always turns on the output with or without delay depending on the selected mode. A positive transition at the trigger input always turns off the output (with the exception of one-shot mode) with or without delay depending on the the selected mode. The delay is a function of the oscillator frequency (or the external clock frequency) and the weighting factor programmed at the weighting factor inputs. The trigger input is clocked into the input latch with the negative edge of the external clock. All timings begin after the latch has been set up. The trigger input has an internal pull-up resistor.



TOP VIEW
STANDARD 14 PIN DIP
Figure 1

WEIGHTING FACTOR INPUT, LSB - MSB

A delay from the trigger input to the output is programmed by applying 1's complement binary weighted numbers at these 5 inputs. The exact equation for the delay is:

$$\text{Delay} = \frac{(1 + 1,023N)}{f}$$ See Fig. 5 Note 3

Where f = The oscillator frequency and N = Weighting factor. All the weighting factor inputs have internal pull-up resistors.

TABLE 1
WEIGHTING BITS ASSIGNMENT

Input	Value
$\overline{LSB}$	1
$\overline{LSB+1}$	2
$\overline{LSB+2}$	4
$\overline{LSB+3}$	8
$\overline{MSB}$	16

Example: For a weighting factor of 25, inputs $\overline{MSB}$, $\overline{LSB+3}$, and $\overline{LSB}$ should be programmed to logic "0".

MODE SELECT INPUTS A & B

The chip can be programmed to operate in 4 different modes by applying the logic levels to inputs A & B as indicated in Table 2. The mode select inputs are clocked into the input latches with the negative edge of the external clock. These inputs should not be changed while a delay timing is in progress. The mode select inputs have internal pull-ups.

MODE DEFINITION: (See Figure 3)

DUAL DELAY MODE

This is the Default Mode when the inputs A & B are left unprogrammed. The function of the Dual Delay mode is to provide a time delay on both the turn-on and turn-off of the output. Once turned on, the output will remain on as long as the trigger input is logic "0". Once turned off, the output will remain off as long as the trigger input is a logic "1".

DELAYED OPERATE MODE

This mode causes a retriggerable delay in turning the output on in response to a negative edge at the trigger input. The output is turned off withour delay in response to a positive transition at the trigger input.

DELAYED RELEASE MODE

This mode causes a retriggerable delay in turning off the output whenever there is a positive transition at the trigger input. The output is turned on without delay in response to a negative transition at the trigger input.

ONE-SHOT MODE

In this mode, the chip functions like a retriggerable monostable multi-vibrator. The output is turned on whenever there is a negative transition at the trigger input. At the end of the programmed delay, the output is turned off automatically. If there is a negative transition at the trigger input before the delay is over, the delay is restarted. A positive transition at the trigger input has no effect on the output in this mode.

OUTPUT

The output is an open drain FET. To obtain proper switching of the output between logic "0" and "1" levels, an external pull down resistor to V_{DD} must be used. If the output is used only as a current source, no such pull down is needed. The output is logically inverted with respect to the trigger input.

TABLE 2
MODE SELECTION

CONTROL A	CONTROL B	MODE
1	1	Dual Delay
1	0	Delayed Release
0	1	Delayed Operate
0	0	One Shot

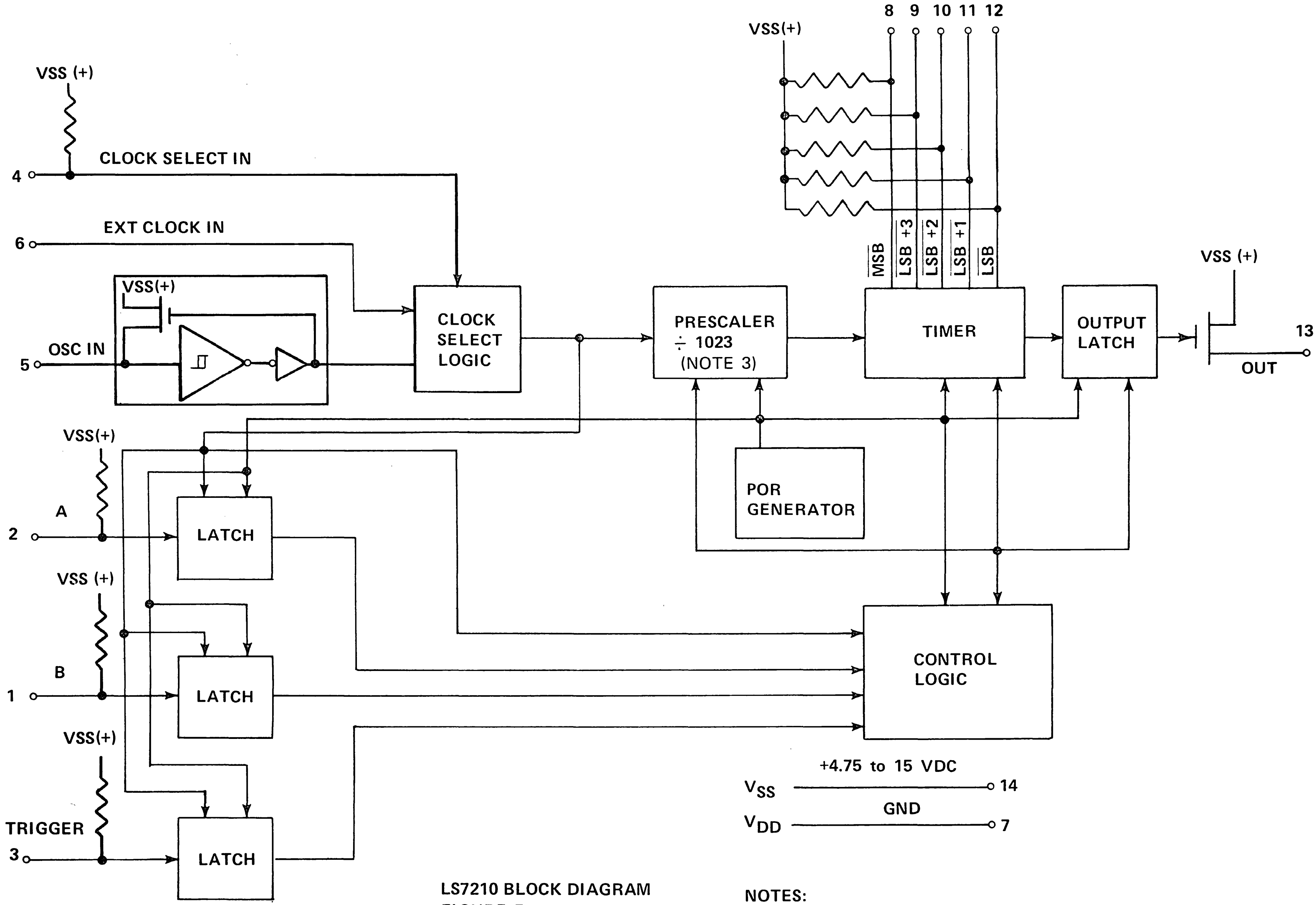
TABLE 3
OSCILLATOR FREQUENCY COMPONENT SELECTION CHART*

R, (KΩ)	C(pF)	@V_{SS}=+5V	@V_{SS}=+10V	@V_{SS}=+15V
47	100	128 KHz	139 KHz	185 KHz
	200	79 KHz	83 KHz	85 KHz
	500	37 KHz	37 KHz	36 KHz
	1000	22 KHz	21 KHz	20 KHz
	50000	610 Hz	500 Hz	475 Hz
470	100	15 KHz	16 KHz	16.5 KHz
	200	9 KHz	9.5 KHz	9.5 KHz
	500	4 KHz	4 KHz	4 KHz
	1000	2.4 KHz	2 KHz	2 KHz
	50000	63 Hz	51 Hz	47 Hz
2000	100	4.2 KHz	4.7 KHz	5 KHz
	200	2.5 KHz	2.7 KHz	2.8 KHz
	500	1.1 KHz	1.1 KHz	1.1 KHz
	1000	670 Hz	617 Hz	610 Hz
	50000	17 Hz	14 Hz	14 Hz
10000	10μF	.02 Hz	.015 Hz	.013 Hz

*NOTE: Frequency values are typical
Accuracy ±10% from Chip to Chip

ABSOLUTE MAXIMUM RATINGS: (All voltages referenced to V_{DD})

	SYMBOL	VALUE	UNITS
DC Supply Voltage	V_{SS}	+18	V
Voltage (Any Pin)	V_{IN}	0 to V_{SS}+.3	V
Operating Temperature	T_A	−25 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C



LS7210 BLOCK DIAGRAM
FIGURE 5

NOTES:

(1) Oscillator FET device can source: 0.6mA @ VSS = +5V
1.6mA @ VSS = +10V
2.7mA @ VSS = +15V

(2) All resistors shown represent a nominal 3 μa constant current source.

(3) ÷1023 is standard. Any number from 1 to 1022 can be mask programmed.

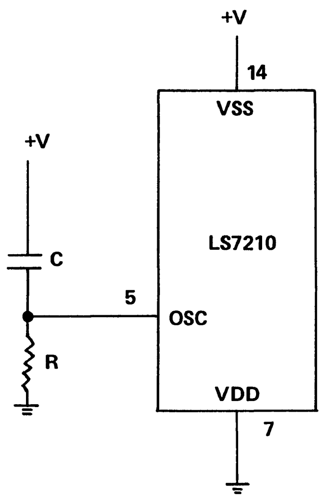


FIGURE 2 – LS7210 OSCILLATOR CONNECTION

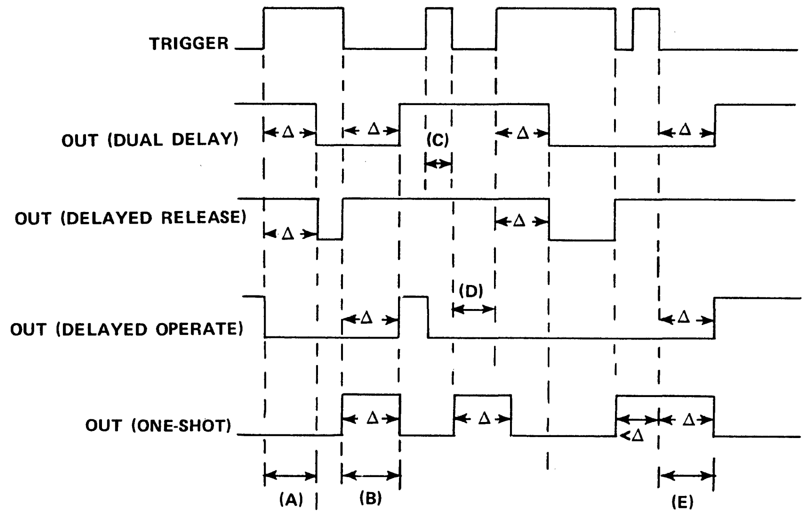


FIGURE 3 – MODE DEFINITION TIMING DIAGRAM

A – Turn-off delay in "Dual Delay" and "Delayed Release" mode.

B – Turn-on delay in "Dual Delay" and "Delayed Operate" mode; one-shot period in "one-shot" mode.

C – Output remains on in "Delayed Release" and "Dual Delay" modes due to negative "trigger" transition before the turn-off delay is over.

D – Output remains off in "Delayed Operate" mode due to positive trigger transition before the turn-on delay is over.

E – One-Shot period extended by re-triggering.

NOTE: Δ is the programmed delay.

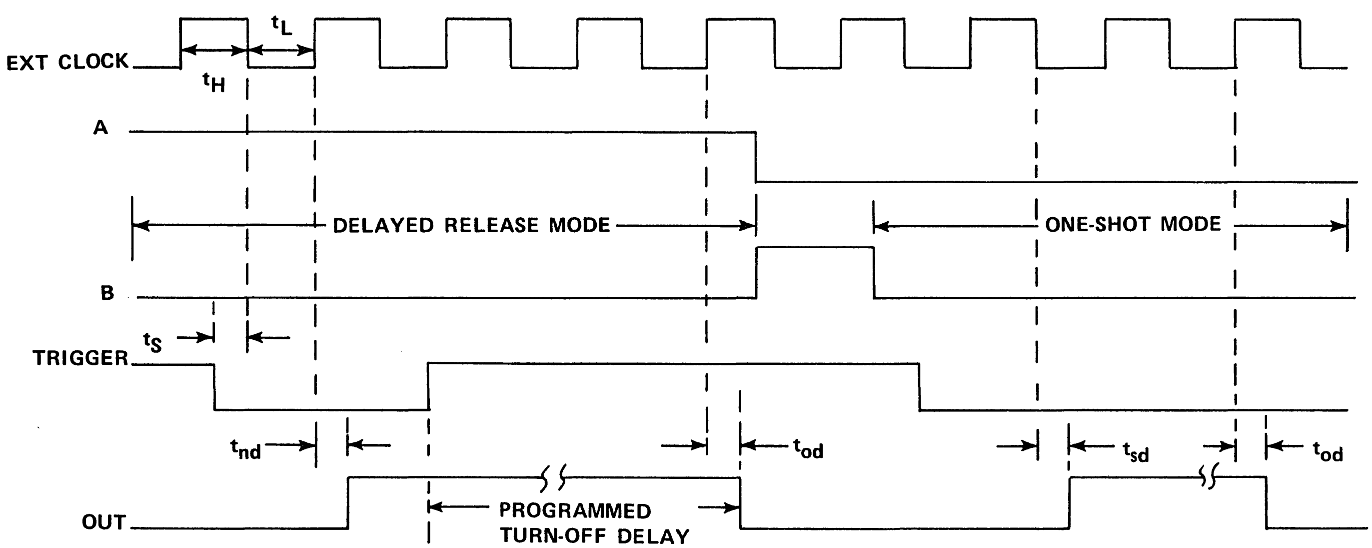


FIGURE 4 – LS7210 TIMING DIAGRAM

Note 1. – A,B and trigger inputs are clocked into the input latches with the negative edge of the ext. clock.

Note 2. – In all modes except One-Shot, the output changes with the positive transition of the ext. clock. In One-Shot mode the output is turned on with the negative transition and turned off with the positive transition of the ext. clock.

DC ELECTRICAL CHARACTERISTICS:
$-25^{o}C \leq T_A \leq +70^{o}C$ unless otherwise specified
All voltages referenced to V_{DD}

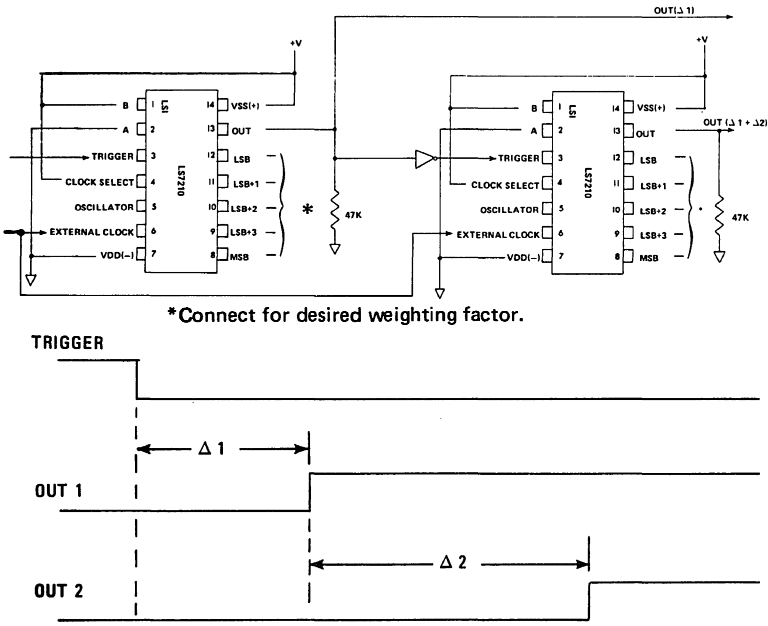
PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITIONS
Supply Voltage	V_{SS}	+4.75	+15.0	V	
Supply Current	I_{SS}	—	3.0	mA	V_{SS} = +15V, output off
Trigger Input					
Logical "1"	V_{TH}	+4	+ 5	V	@V_{SS} = + 5V
		+9	+10	V	@V_{SS} = +10V
		+14	+15	V	@V_{SS} = +15 V
Logical "0"	V_{TL}	0	+ 1	V	@V_{SS} = + 5V
		0	+ 2	V	@V_{SS} = +10V
		0	+ 3	V	@V_{SS} = +15V
All Other Inputs					
Logical "1"	V_{IH}	+4	+ 5	V	@V_{SS} = + 5V
		+8	+10	V	@V_{SS} = +10V
		+12	+15	V	@V_{SS} = +15V
Logical "0"	V_{IL}	0	+1.0	V	@V_{SS} = + 5V
		0	+2.0	V	@V_{SS} = +10V
		0	+3.0	V	@V_{SS} = +15V
Output					
Source Current	I_o	+550	–	μA	@V_0 = + 4.5V, V_{SS} =+ 5V
		+1.0	–	mA	@V_0 = + 4.0V, V_{SS} =+ 5V
		+2.8	–	mA	@V_0 =+ 9.0V, V_{SS} =+10V
		+4.9	–	mA	@V_0 = + 8.0V, V_{SS} =+10V
		+4.2	–	mA	@V_0 = +14.0V, V_{SS} =+15V
		+8.1	–	mA	@V_0 = +13.0V, V_{SS} =+15V

SWITCHING CHARACTERISTICS:
(See Figure 4)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Oscillator Frequency	f_{osc}	.01 Hz	–	100KHz	–
External Clock Frequency	f_{ext}	DC	–	160KHz	–
External Clock Positive Pulse Width	t_H	3	–	–	μs
External Clock Negative Pulse Width	t_L	3	–	–	μs
A, B and Trigger Input Set-Up Time	t_S	–	200	300	ns
EXT Clock to Output Delay (turn-on delay in delayed release mode and turn-off delay in delayed operate mode)	t_{nd}	–	700	1000	ns
EXT Clock to Output Delay at the End of Time Out	t_{od}	–	1	1.6	μs
EXT Clock to Output Delay (turn-on Delay in One Shot Mode)	t_{sd}	–	400	600	ns

APPLICATION EXAMPLES

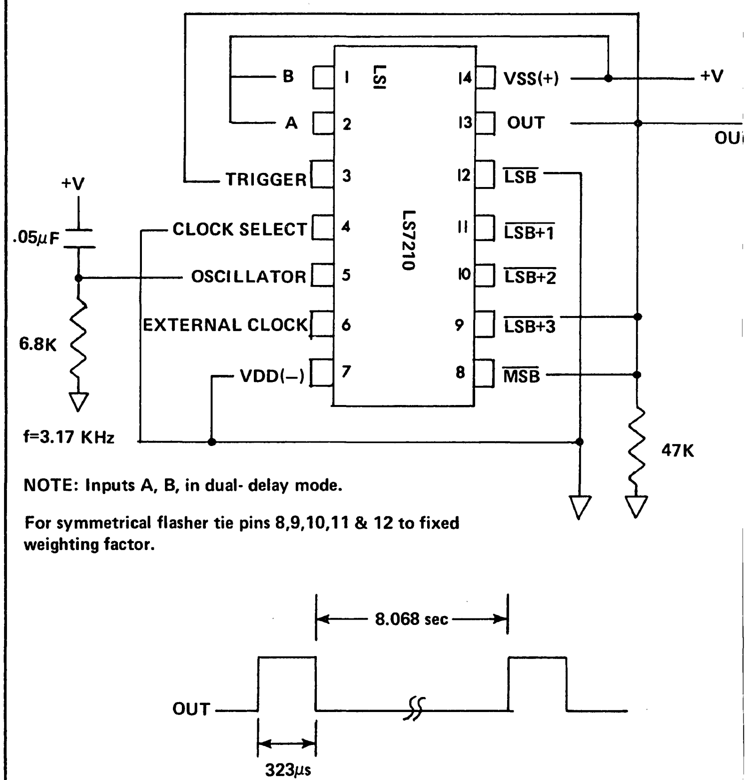
SEQUENTIAL TURN ON



***NOTE:**
Output of LS7210 is open drain FET. Some load to ground is required to cause output to go negative.

FIGURE 6

UNSYMMETRICAL FLASHER



NOTE: Inputs A, B, in dual- delay mode.

For symmetrical flasher tie pins 8,9,10,11 & 12 to fixed weighting factor.

FIGURE 7

LS7210 IN DELAYED OPERATE MODE TO ACHIEVE ONE TO 31 MINUTE DELAY

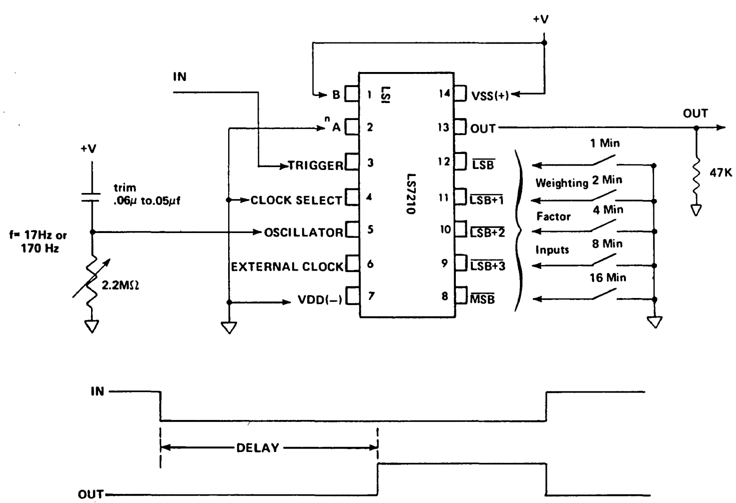
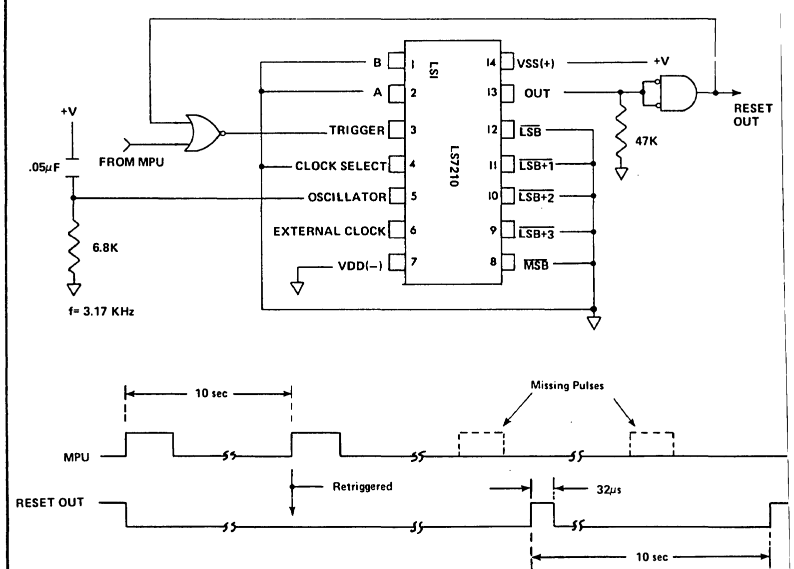


FIGURE 8

AUTO RESET WATCHDOG CIRCUIT



NOTE: Inputs A, B are in One Shot mode.
In this application an output is generated whenever the perodic sampling signal from the MPU is interrupted.

FIGURE 9

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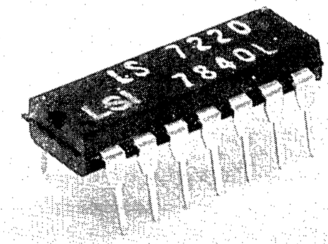
LS7220 | DIGITAL LOCK CIRCUIT

REVISED NOVEMBER 1985

FEATURES:

- Stand Alone Lock Logic
- 5040, 4 Digit Combinations
- Out of Sequence Detection
- Direct LED and Lock Relay Drive
- Chip Enable (For Automotive Applications)
- Externally Controlled Convenience Delay
- Save Memory (For Valet Parking, etc.)
- Internal Pull Down Resistors on All Inputs
- High Noise Immunity
- Low Current Consumption (40μA max@12VDC)
- Single Power Supply Operation (+5V to +18V)
- Momentary or Static Lock Control Output
- All Inputs Protected



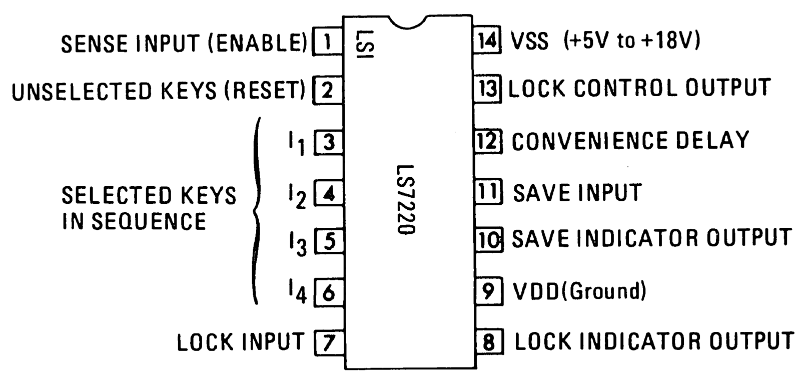
DESCRIPTION:

The LS7220 is a monolithic, ion implanted MOS 4 key keyless lock. The circuit includes sequential logic for interpretation of correct key closure; out of sequence detection circuitry, and save memory.

DESCRIPTION OF OPERATION:

SENSE:
A logical "1" at this input charges the external CONVENIENCE DELAY capacitor, and enables the SELECTED KEYS inputs to be recognized in proper sequence and enables the lock control, lock indicator and save indicator outputs. A low at this input keeps all outputs in the OFF condition (logical "0") and resets the device if the "SAVE MEMORY" was reset by a logical "1" at the LOCK input.

SELECTED KEYS:
A sequence of logical "1"'s at the inputs I_1, I_2, I_3, and I_4 (in correct sequence) set the "SEQUENTIAL MEMORY", causes the LOCK CONTROL output to go high and the LOCK INDICATOR to open.



TOP VIEW
STANDARD 14 PIN DIP
Figure 1

SAVE:
A logical "1" at this input sets the "SAVE MEMORY" and protects the internal "SEQUENTIAL MEMORY" from resetting in the event of a change at the SENSE input. The SAVE status is indicated by a logical "1" at the SAVE INDICATOR output. (See LOCK).

UNSELECTED KEYS:
A logical "1" at this input resets the "SEQUENTIAL DETECTOR" for the SELECTED KEYS inputs. This input may be wired to all the keys that are not part of the input sequence.

LOCK:
A logical "1" at this input removes any previous SAVE status. (See SENSE). This is indicated by an open at the SAVE INDICATOR output.

CONVENIENCE DELAY:
An external capacitor at this input delays changes on any of the outputs when SENSE changes from high to low. The delay is a function of the external capacitance and the supply voltage. See Figure 2.

LOCK CONTROL:
This output is on (logical "1") when SENSE is high and the "SEQUENTIAL MEMORY" is set. (See SELECTED KEYS). This output goes open when SENSE goes low (after convenience delay). It goes to a logical "1" again when SENSE goes high and the "SEQUENTIAL MEMORY" was saved by a logical "1" at the SAVE input.

LOCK INDICATOR:
This output is the complement of the LOCK CONTROL output.

SAVE INDICATOR:
This output is on (logical "1") when SENSE is at logical "1" and the "SAVE MEMORY" is set by a logical "1" at the SAVE input.

POWER-ON-RESET:
A Power-On-Reset circuit resets the device to a "lock" condition upon application of power.

POWER SUPPLIES:
The circuit will operate over the range of +5 to +18 volts.

MAXIMUM RATINGS: (Voltages Referenced to V_{DD})

Rating	Symbol	Value	Units
DC Supply Voltage	V_{ss}	+5 to +18	Vdc
Operating Temperature Range	TA	−25 to +70	°C
Storage Temperature Range	TSTG	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS:
(V_{DD} = 0V, V_{ss} = +5 to +18V, $-25°C \leq TA \leq +70°C$ unless otherwise specified).

OUTPUT SPECIFICATIONS:

	VSS	SOURCE CURRENT MIN	TYP	MAX	UNITS
Lock Control	5Vdc	2.40	3.75	6.30	mA
Output Pin 13	9Vdc	7.20	9.75	14.70	
On (Logic "1")	12Vdc	10.80	14.25	21.00	
$V_{out} = V_{ss}-2$	15Vdc	14.40	18.75	27.30	
	18Vdc	18.00	23.25	30.00*	
Convenience	5Vdc	0.20	0.29	0.50	mA
Delay Pin 12	9Vdc	0.55	0.75	1.13	
On (Logic "1")	12Vdc	0.83	1.10	1.60	
$V_{out} = V_{ss}-2$	15Vdc	1.10	1.44	2.10	
	18Vdc	1.40	1.80	2.30	
Lock Indicator	5Vdc	.40	.60	1.00	mA**
Output Pin 8	9Vdc	3.00	4.30	6.90	
On (Logic "1")	12Vdc	6.10	8.50	13.00	
V_{out} Clamp to	15Vdc	10.40	14.00	21.00	
1.7V	18Vdc	15.80	20.00	30.00*	
Save Indicator	5Vdc	.80	1.20	2.00	mA**
Output Pin 10	9Vdc	6.00	8.60	13.80	
On (Logic "1")	12Vdc	12.20	17.00	30.00*	
V_{out} Clamp to	15Vdc	20.80	28.00	30.00*	
1.7V	18Vdc			30.00*	

* Indicates maximum allowable current drain of 30 milliamperes.
Note: Limit output current to 30mA max.

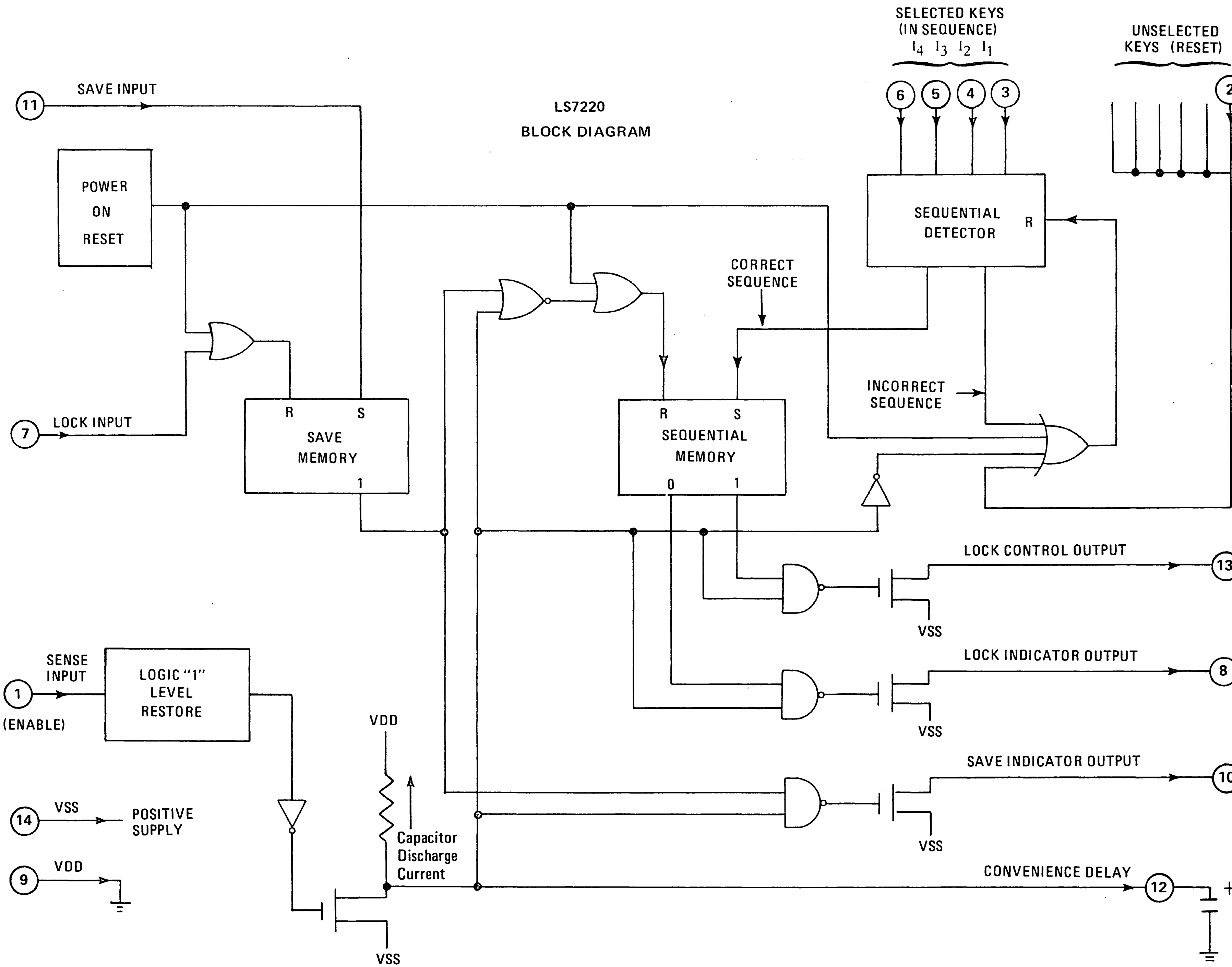
INPUT VOLTAGE SPECIFICATIONS:

	Parameter	Symbol	VSS Vdc	MIN	MAX	UNIT
SENSE INPUT	Input Logic "0"	ViL	5.0	0	Vss−3.0	Vdc
			9	0	Vss−6.0	
			12	0	Vss−8.0	
			15	0	Vss−9.0	
			18	0	Vss−9.5	
	Input Logic "1"	ViH	5.0	Vss−1.5	Vss	Vdc
			9	Vss−3.5	Vss	
			12	Vss−5.5	Vss	
			15	Vss−6.0	Vss	
			18	Vss−6.5	Vss	
All Other Inputs	Input Logic "0"	ViL	Vss	0	Vss−3	Vdc
	Input Logic "1"	ViH	Vss	Vss−1	Vss	

** Current drive balanced for equal brightness on red and green indicators.

NOTE: Typical input load current is 6μA with input @ V_{DD}, V_{SS} @+12V.

5



LS7220
BLOCK DIAGRAM
SELECTED KEYS
(IN SEQUENCE)
I_4 I_3 I_2 I_1
UNSELECTED
KEYS (RESET)
6
5
4
3
2
11
SAVE INPUT
POWER
ON
RESET
SEQUENTIAL
DETECTOR
R
CORRECT
SEQUENCE
INCORRECT
SEQUENCE
7
LOCK INPUT
R
S
SAVE
MEMORY
1
R
S
SEQUENTIAL
MEMORY
0
1
LOCK CONTROL OUTPUT
13
VSS
LOCK INDICATOR OUTPUT
8
SENSE
INPUT
1
(ENABLE)
LOGIC "1"
LEVEL
RESTORE
VDD
VSS
SAVE INDICATOR OUTPUT
10
14
VSS
POSITIVE
SUPPLY
Capacitor
Discharge
Current
VSS
9
VDD
CONVENIENCE DELAY
12
+
VSS

Figure 7

LS7220 FLOW CHART

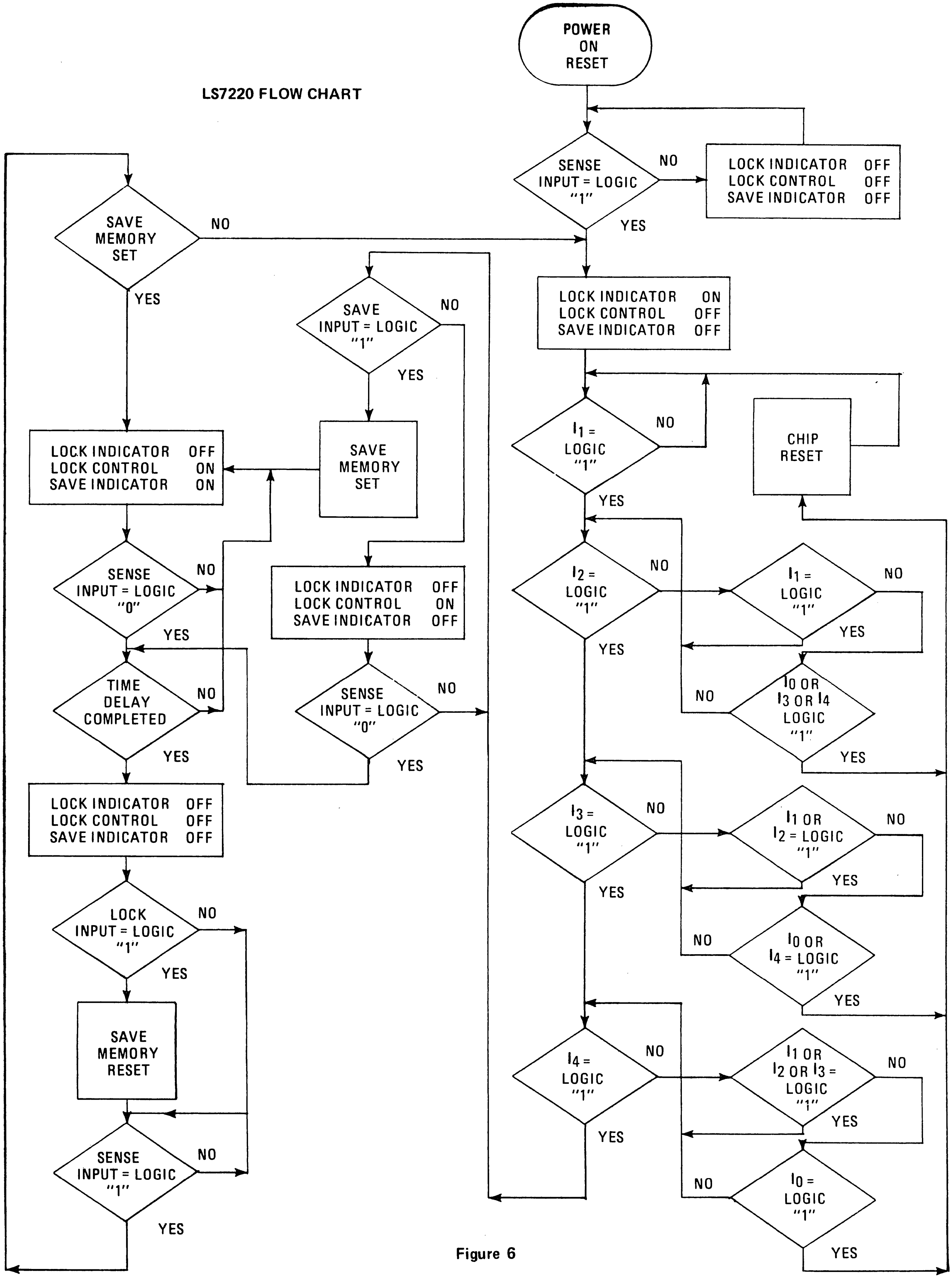


Figure 6

INPUT CAPACITANCE: 10Pf

Parameter	Symbol	MAX	Units
Convenience Delay:			
Set-Up Time } See Note	TS	4	μsec
Hold Time } Below	TH	8	μsec
Input Lock Control:			
Output Delay	TLC	8	μsec
Input Pulse Width	TIW	25	μsec

NOTE: TS and TH were measured without any external capacitance at convenience delay (Pin 12) input.

QUIESCENT SUPPLY CURRENT:

(All inputs and outputs open)

Symbol	Vss	MAX	UNITS
I_{DD}	5Vdc	20	μA
	9Vdc	30	
	12Vdc	40	
	15Vdc	50	
	18Vdc	70	

Typical Hold Time Vs. VSS
(with 1μF convenience delay capacitor)

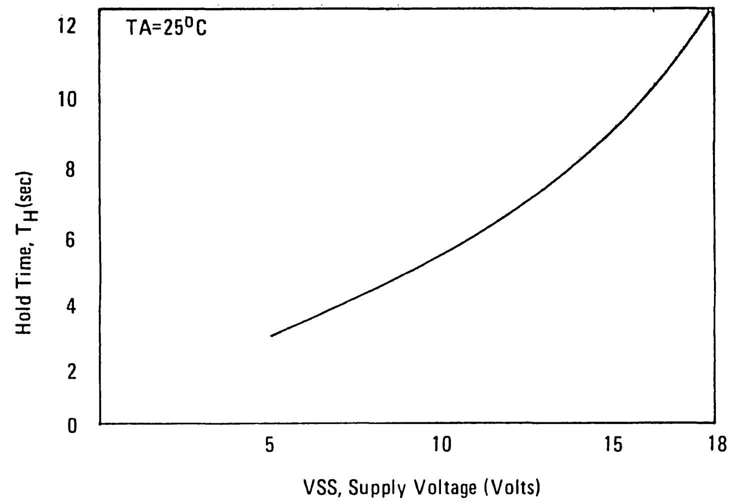
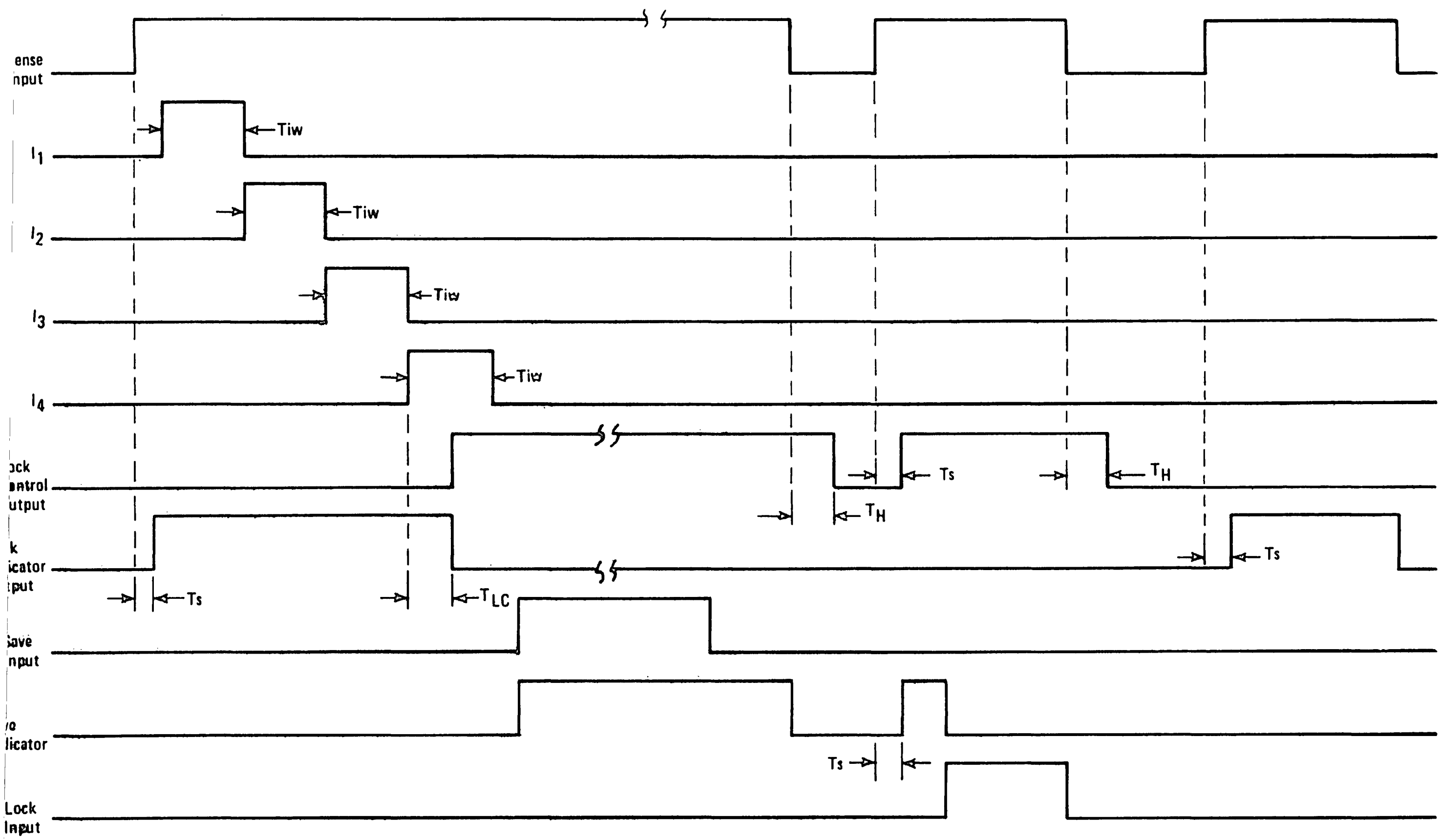
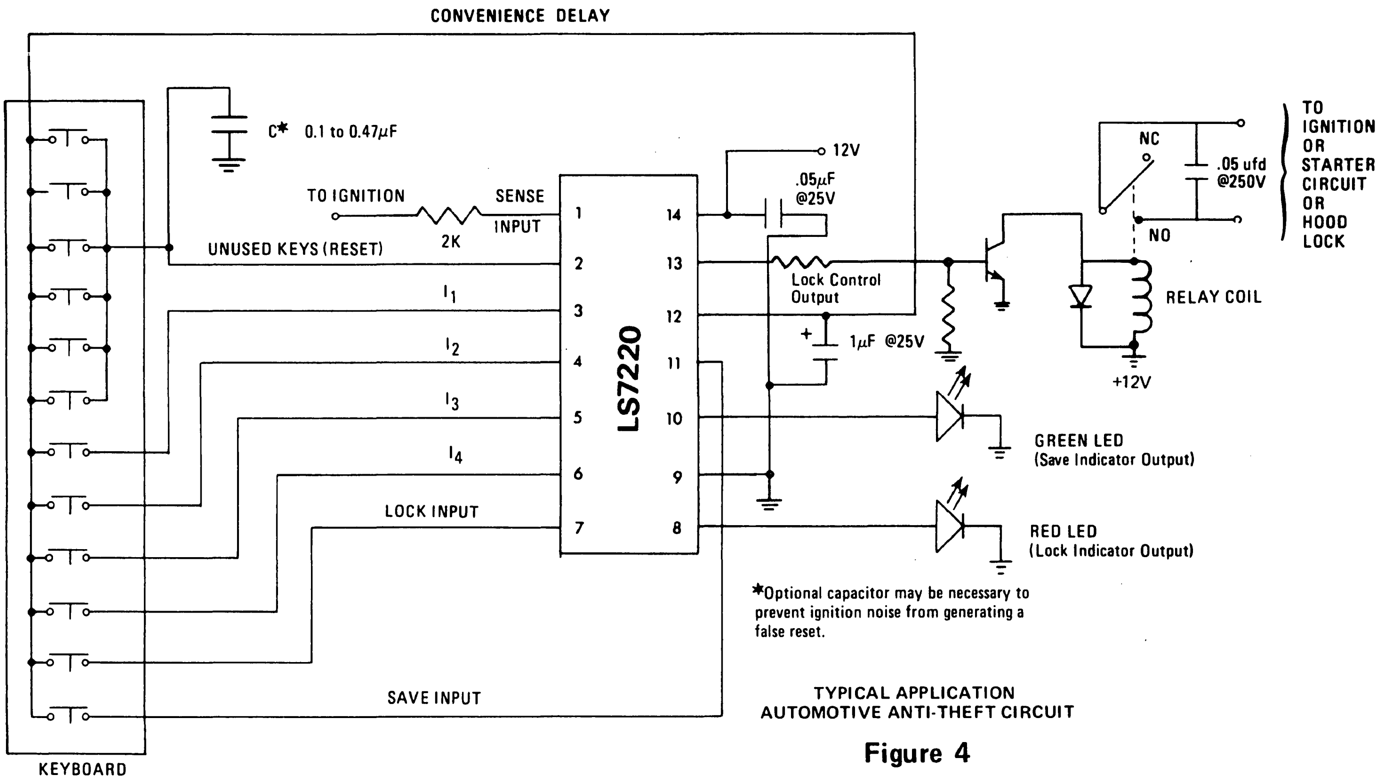


Figure 2



TIMING DIAGRAM

Figure 3



TYPICAL APPLICATION
AUTOMOTIVE ANTI-THEFT CIRCUIT

Figure 4

A typical automotive anti-theft circuit is shown in the schematic diagram. When the ignition switch is turned on the SENSE input (pin 1) goes high and the circuit is ready to accept the unlocking input sequence at I_1, I_2, I_3 and I_4 (pin 3,4,5 and 6 respectively). If the keys associated with these inputs are depressed exactly in sequence of I_1, I_2, I_3 and I_4, the lock control output (pin 13) will become ON and the lock relay will be energized. This state will be indicated by the OFF condition of the lock indicator output (pin 8) which will render the red LED OFF (an indication of unlock condition). If the keys are depressed in any sequence other than as described above, the internal sequential detector will be reset and the entire sequence must be repeated.

In order to save the ON condition of the lock control output when the ignition switch is turned OFF (i.e., when the SENSE input becomes low) the key associated with the SAVE input (pin 11) will have to be depressed. The "SAVE" status will be indicated by a high at the save indicator output (pin 10), which in turn will turn the green LED ON. If the ignition switch is turned OFF while the green LED is on, all the output status will be preserved in the internal memory, so that when the ignition switch is turned on again there will be no need to go through the input sequence again. This feature could be used for valet parking and garage service.

Status saving may be cancelled by depressing the lock key followed by turning the ignition switch OFF for a time greater than the convenience delay. This will also turn OFF the lock control output.

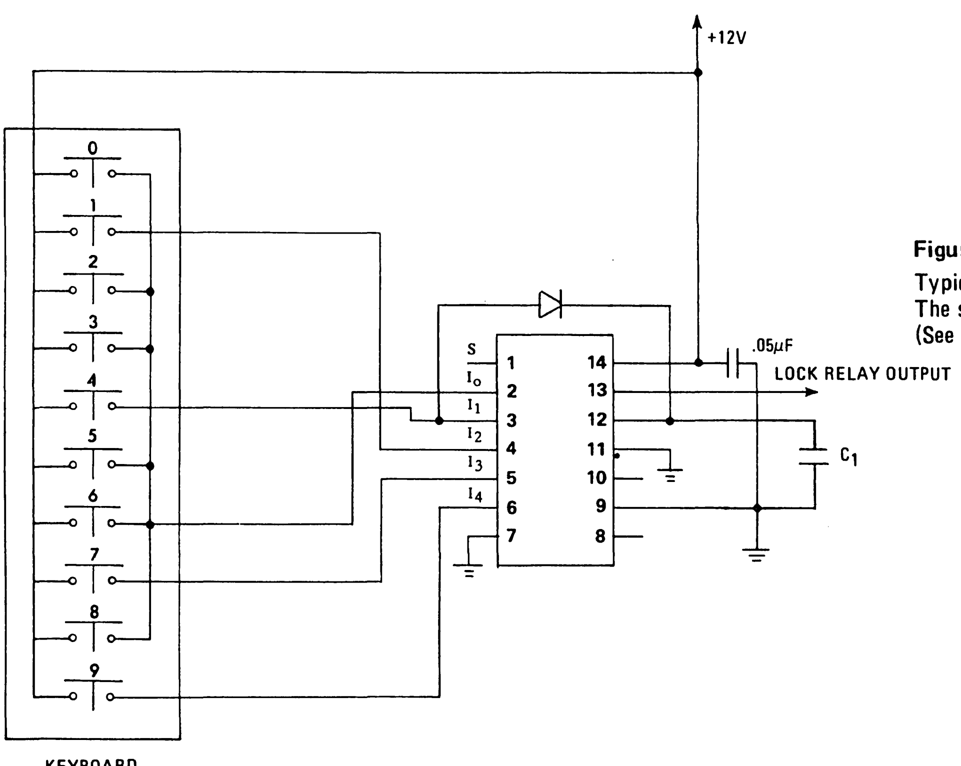


Figure 5

Typical 4 key code having MOMENTARY output. The size of C_1 determines the length of entry time (See Figure 2). The specific code shown is 4179.

LSI/CSI

LS7222

KEYBOARD PROGRAMMABLE DIGITAL LOCK CIRCUIT

FEATURES:

- Stand alone lock logic
- 38416, 4-digit combinations
- 3 different user programmable codes
- Momentary and static lock control outputs
- Internal keyboard debounce circuit
- Tamper detection output
- Circuit status outputs
- Low current consumption 30μa max @ 12 VDC)
- Single power supply operation (+4 to +18 VDC)
- All inputs protected
- High noise immunity

CONNECTION DIAGRAM — TOP VIEW
STANDARD 20 PIN PLASTIC DIP

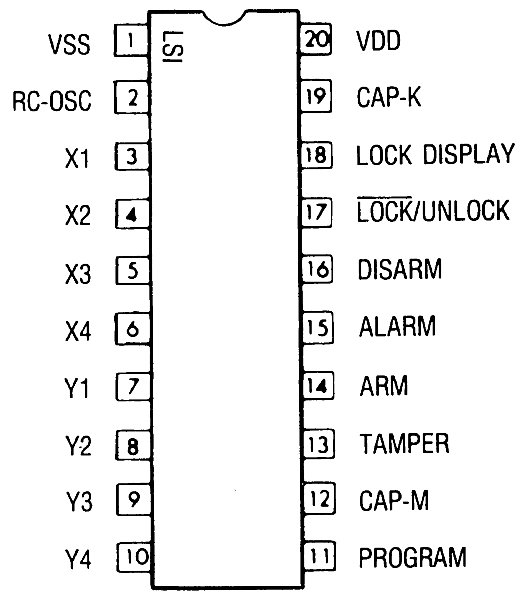


FIGURE 1

GENERAL DESCRIPTION:

The LS7222 is a programmable electronic lock implemented in a monolithic CMOS integrated circuit, packaged in a 20 pin DIP. The circuit contains all the necessary memory, decoder and control logic to make a programmable "keyless" lock system to control electro-mechanical type locks. Input is provided by a matrix keypad whose maximum allowable size is 4 x 4.

The LS7222 can be programmed to recognize 3 different codes: one to lock (arm), one to unlock (disarm), and one to unlock and trigger an alarm (duress). Progamming is done via the keypad inputs. Any entry from the keypad (when not in the program mode) which does not match one of the 3 programmed codes will cause the TAMPER output to become active.

The monolithic, low power CMOS design of the LS7222 enables it to be designed into typical battery backed-up and automotive type security systems.

DETAILED DESCRIPTION:

CODES — There are 3 different function codes which the LS7222 can store in memory. Each code consists of a 4 digit number which must be entered in exact sequence and before the keypad entry enable time expires. The 3 codes and their functions are explained below.

1. The Arm code, when entered from the keypad, causes the $\overline{\text{LOCK}}$/UNLOCK output to latch low and the ARM output to momentarily go high. Whenever power is first applied to the LS7222, the circuit defaults to the Arm code corresponding to the keys X1 Y1, X1 Y2, X2 Y2, X2 Y1. The code can then be altered to any other 4 digit code by entering the Program mode and keying in the new code.
2. The Disarm code, when entered from the keypad, causes the $\overline{\text{LOCK}}$/UNLOCK output to latch high and the DISARM output to momentarily go high. The first 3 digits of the Disarm code must be identical to the first 3 digits of the Arm code; the 4th digit may or may not be identical for the two codes. When the two codes are the same in all 4 digits, i.e. the same code is chosen for arming and disarming, the entry of the code will cause the $\overline{\text{LOCK}}$/UNLOCK output to toggle. This means that if the output was high (unlocked) it will go low (locked) and vice-versa. Whenever power is first applied to the LS7222, the circuit defaults to the DISARM code corresponding to the keys X1 Y1, X1 Y2, X2 Y2, X1 Y1. The code can then be altered by entering the Program mode.
3. The Duress code, when entered from the keypad, causes the $\overline{\text{LOCK}}$/UNLOCK output to latch high and the DISARM output to momentarily go high; at the same time the ALARM output will latch high to enable an external alarm. The first 3 digits of the Duress code must be identical to the first 3 digits of the Arm and Disarm codes; the 4th digit must be different to activate the ALARM output. Whenever power is first applied to the LS7222, the circuit defaults to the Duress code corresponding to the keys X1 Y1, X1 Y2, X2 Y2, X1 Y2. The code can then be altered the same way as the other two codes.

PROGRAM MODE — The current Arm/Disarm/Duress codes may be altered to any other value by initializing the Program mode. The steps involved for altering the codes are as follows:

1. Enter the current Disarm code causing the DISARM output to go high.
2. Before the keypad entry enable time expires, enter the key corresponding to matrix position X4 Y1 two times. This will cause the PROGRAM MODE output to latch high, indicating that the circuit is now in the Program mode. The keypad entry enable timer is disabled during the Program mode.
3. Enter a 6 digit number from the keypad. The PROGRAM MODE output will latch low, indicating that the new codes have successfully been programmed. Of the 6 digits, the first 4 constitute the Arm code; the first 3 and the 5th constitute the Disarm code, and the first 3 and the 6th constitute the Duress code. If an error is introduced or it is desired to change the codes before the 6th digit is typed, enter the key X4 Y3. This will reset the internal memory pointer of the LS7222 and a new 6 digit number can be entered.

KEYPAD INTERFACE — The four X inputs and four Y outputs are designated for keypad interface (see FIG. 2). Since the X inputs have internal pull-ups, the maximum matrix size of 4 by 4 does not have to be utilized. And because the Y outputs have open drains, more than one LS7222 may share the same keypad.

During normal operation the LS7222 will scan the matrix looking for a switch closure. Once a closure has been detected, the internal keyboard debounce logic determines if a "valid" key has been pressed or that if noise is just present. Only one valid input will be generated with any key closure. The use of internal keyboard debouncing and schmitt triggers on the inputs provides the LS7222 with very high noise immunity.

TAMPER — When a valid key has been detected by the LS7222, the entry is compared against the appropriate reference in the internal memory. If the requirements of digit value and code sequential postion are not fulfilled, the TAMPER output will momentarily go high; this indicates that an illegal code entry was attempted. The keypad entry enable timer and memory pointer will both be reset so that entry of the code can be attempted again.

TABLE 1. PIN DESCRIPTIONS

PIN	FUNCTION	DESCRIPTION
1	VSS	Supply voltage negative.
2	RC-OSC	Determines the LS7222's internal clock frequency, which is used for keyboard scanning and debounce. A resistor (to VDD) and a capacitor (to VSS) connected to this input sets the frequency.
3,4,5,6, 7,8,9,10	X1,X2,X3,X4 Y1,Y2,Y3,Y4	The four X inputs and four Y outputs are designed to interface to a keypad matrix whose maximum allowable size is 4 by 4.
11	PROGRAM MODE	This output goes high when the program mode is initiated. It resets to a low state after the 6 digit Arm/Disarm/Duress combination code has been programmed.
12	CAP-M	A capacitor connected between this input and VSS controls the duration of the ARM, DISARM, and TAMPER outputs.
13	TAMPER	Whenever a key is entered that is not a valid code element, this output goes high for a period determined by the capacitor on the CAP-M input.
14	ARM	This output generates an active high output every time the Arm code is entered, irrespective of whether the circuit is currently in the disarmed state or not. The duration of this output is determined by the capacitor on the CAP-M input.
15	ALARM	When the Duress code is entered, this output latches high to enable an external alarm. The ALARM output resets to a low state when the Arm code is entered again.
16	DISARM	This output generates an active high output every time the Disarm code is entered, irrespective of whether the circuit is currently in the armed state or not. The duration of this output is determined by the capacitor on the CAP-M input.
17	$\overline{\text{LOCK}}$/UNLOCK	When the Disarm code or the Duress code is entered, this output latches high. When the Arm code is entered, the output latches low. If the Disarm or Duress code is entered when the output is already high (i.e., already disarmed), the output remains unaffected. Similarly, if the Arm code is entered when the output is already low (i.e. already armed), it remains unchanged. An exception to this rule is when the Arm and Disarm codes are identical in all 4 digits. In that situation, the output will toggle every time the code is entered.
18	LOCK STATUS	Functionally, this output is identical to the $\overline{\text{LOCK}}$/UNLOCK output, with the exception that its polarity is reversed with respect to the $\overline{\text{LOCK}}$/UNLOCK output. This output is intended for driving a display lamp to indicate the lock status.
19	CAP-K	A capacitor connected between this input and VSS sets the time limit for entering a 4 digit code from the keypad. (6 digits when initiating the program mode)
20	VDD	Supply voltage positive.

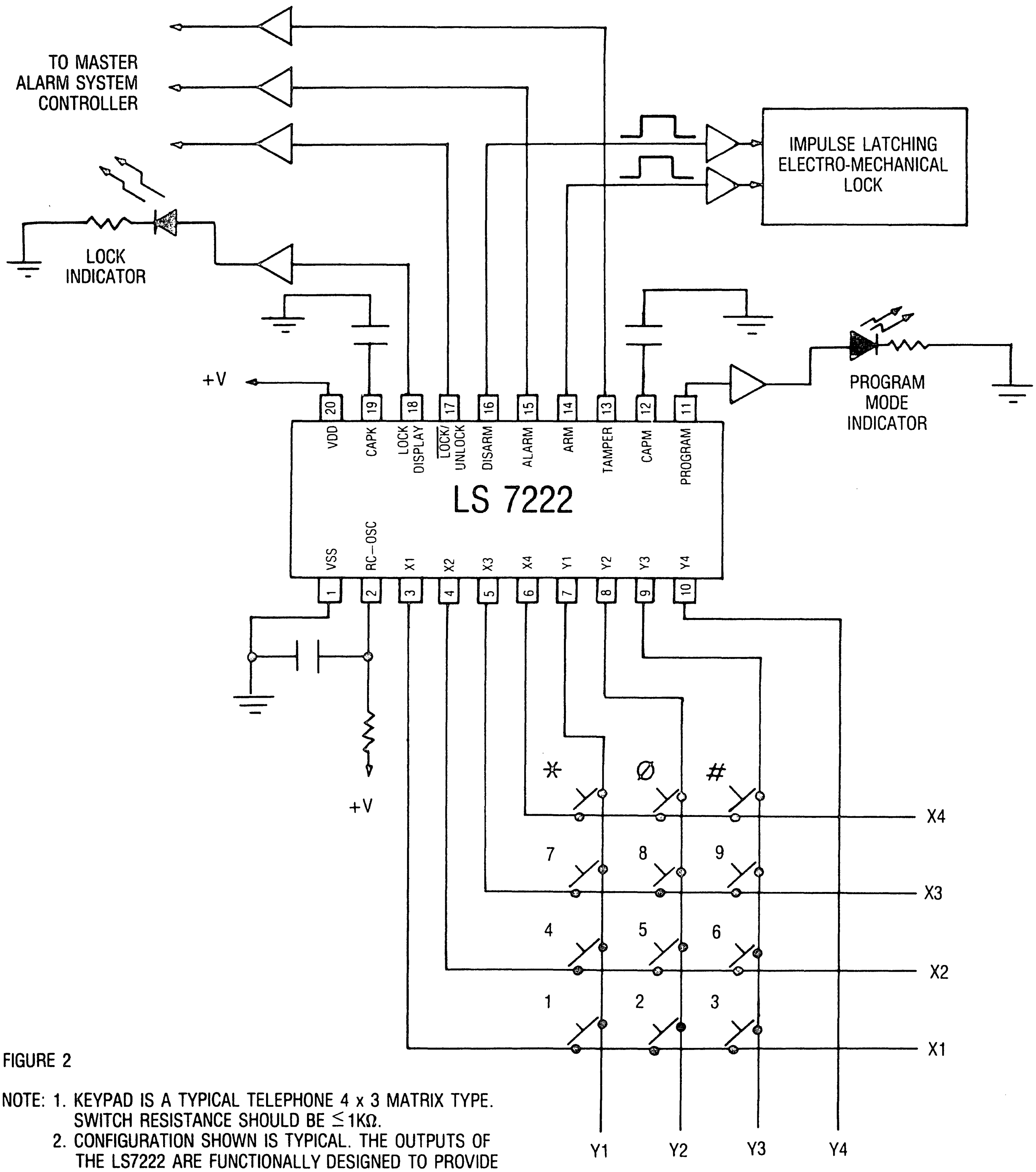


FIGURE 2

NOTE: 1. KEYPAD IS A TYPICAL TELEPHONE 4 x 3 MATRIX TYPE. SWITCH RESISTANCE SHOULD BE $\leq 1K\Omega$.
2. CONFIGURATION SHOWN IS TYPICAL. THE OUTPUTS OF THE LS7222 ARE FUNCTIONALLY DESIGNED TO PROVIDE EITHER STATUS OR DISPLAY INFORMATION

Quiescent supply current: (100pf capacitor to VSS and 1.5M Ω resistor to VDD, connected to the RC-OSC input)

SYMBOL	VDD	MAX	UNIT
I_{DD}	5 VDC	10	μa
	9 VDC	15	
	12 VDC	20	
	15 VDC	25	
	18 VDC	30	

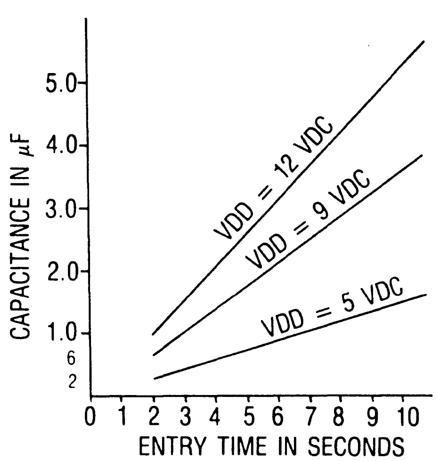
Maximum Ratings: (Voltages references to VSS)

RATING	SYMBOL	VALUE	UNIT
DC supply voltage	VDD	+4 to +18	Vdc
Operating temperature range	TA	-25 to +70	°C
Storage temperature range	TSTG	-65 to +150	°C

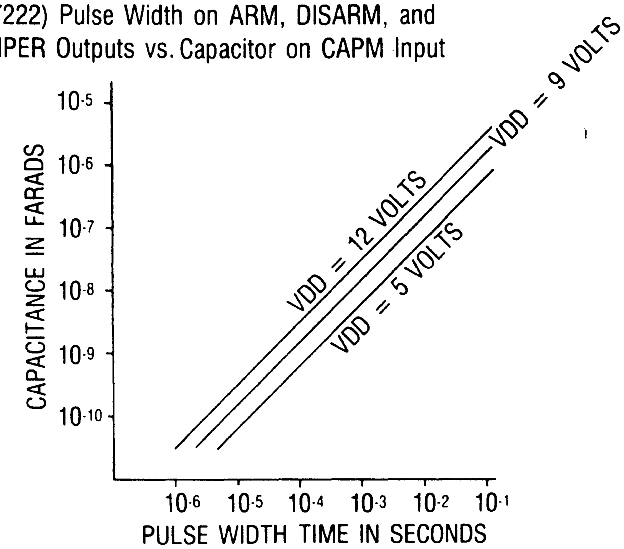
DC Electrical Characteristics:
(VSS = 0V, VDD = +4 to +18V, -25°C ≤ TA ≤ +70°C unless otherwise specified)

PARAMETER	CONDITIONS	VDD	MIN	TYP	MAX	UNITS
Output source current Lock Display, ARM, DISARM Alarm, $\overline{\text{LOCK}}$/UNLOCK Program Mode Outputs	Logic "1" Output $V_{OUT} \geq V_{DD}$ -2V	5VDC 12VDC 18VDC	1.56 5.60 9.07	2.48 8.25 13.2	— — —	ma ma ma
Output Sink Current Lock Display, ARM, DISARM Alarm, $\overline{\text{LOCK}}$/UNLOCK Program Mode Outputs	Logic "0" Output $V_{OUT} \leq V_{SS}$ + .4V	5 VDC 12VDC 18VDC	.404 1.21 1.9	.627 1.78 2.77	— — —	ma ma ma
Output Source Current Tamper Output	Logic "1" Output $V_{OUT} \geq V_{DD}$ -2V	5VDC 12VDC 18VDC	.260 .934 1.51	.413 1.38 2.2	— — —	ma ma ma
Output Sink Current Tamper Output	Logic "0" Output $V_{OUT} \leq V_{SS}$+ .4V	5VDC 12VDC 18VDC	.067 .202 .318	.105 .297 .462	— — —	ma ma ma
Input Level Detection All Inputs	V_{IH} = Logic "1"	5VDC 12VDC 18VDC	3.5 8.0 12.0	— — —	VDD VDD VDD	Vdc Vdc Vdc
	V_{IL} = Logic "0"	5VDC 12VDC 18VDC	VSS VSS VSS	— — —	1.60 4.0 6.0	Vdc Vdc Vdc

Keypad Entry Time vs. Capacitor on CAPK Input



(LS7222) Pulse Width on ARM, DISARM, and TAMPER Outputs vs. Capacitor on CAPM Input



LSI/CSI

LS7223

KEYBOARD PROGRAMMABLE DIGITAL LOCK CIRCUIT

REV. 1/88

FEATURES:

- Stand alone lock logic
- 38416, 4-digit combinations
- 3 different user programmable codes
- Momentary and static lock control outputs
- Internal keyboard debounce circuit
- Tamper detection output
- Circuit status outputs
- Low current consumption 30μa max @ 12 VDC)
- Single power supply operation (+4 to +18 VDC)
- All inputs protected
- High noise immunity

GENERAL DESCRIPTION:

The LS7223 is a programmable electronic lock implemented in a monolithic CMOS integrated circuit, packaged in a 20 pin DIP. The circuit contains all the necessary memory, decoder and control logic to make a programmable "keyless" lock system to control electro-mechanical type locks. Input is provided by a matrix keypad whose maximum allowable size is 4 x 4.

The LS7223 can be programmed to recognize 3 different codes: one to toggle an output, one to toggle an output and generate a pulse, and one to toggle an output and trigger an alarm. Programming is done via the keypad inputs. Any entry from the keypad (when not in the program mode) which does not match one of the 3 programmed codes, will cause the TAMPER output to become active.

The monolithic, low power CMOS design of the LS7223 enables it to be designed into typical battery backed-up and automotive type security systems.

DETAILED DESCRIPTION:

CODES — There are 3 different function codes which the LS7223 can store in memory. Each code consists of a 4 digit number which must be entered in exact sequence and before the keypad entry enable time expires. The 3 codes and their functions are explained below.

1. The Primary code, when entered from the keypad, causes the $\overline{\text{LOCK}}$/UNLOCK 1 output to toggle and the MOMENTARY output to momentarily go high. Whenever power is first applied to the LS7223, the circuit defaults to the Primary code corresponding to the keys X1 Y1, X1 Y2, X2 Y2, X2 Y1. The code can then be altered to any other 4 digit code by entering the Program mode and keying in the new code.

CONNECTION DIAGRAM — TOP VIEW
STANDARD 20 PIN PLASTIC DIP

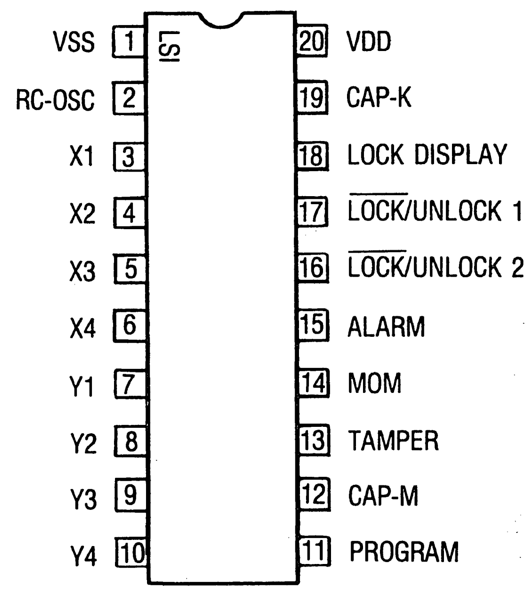


FIGURE 1

2. The Secondary code, when entered from the keypad, causes the $\overline{\text{LOCK}}$/UNLOCK 2 output to toggle. The first 3 digits of the Secondary code must be identical to the first 3 digits of the Primary code; the 4th digit may or not be identical for the two codes. When the two codes are the same in all 4 digits, the entry of the code will cause both the $\overline{\text{LOCK}}$/UNLOCK 1 and the $\overline{\text{LOCK}}$/UNLOCK 2 outputs to toggle. Whenever power is first applied to the LS7223, the circuit defaults to the Secondary code corresponding to the keys X1 Y1, X1 Y2, X2 Y2, X1 Y1. The code can then be altered by entering the Program mode.
3. The Duress code, when entered from the keypad, causes the $\overline{\text{LOCK}}$/UNLOCK 1 output to toggle; at the same time the ALARM output will latch high to enable an external alarm. The first 3 digits of the Duress code must be identical to the first 3 digits of the Primary and Secondary codes; the 4th digit must be different to activate the ALARM output. Whenever power is first applied to the LS 7223, the circuit defaults to the Duress code corresponding to the keys X1 Y1, X1 Y2, X2 Y2, X1 Y2. The code can then be altered the same way as the other two codes.

PROGRAM MODE — The current Primary/Secondary/Duress codes may be altered to any other value by initializing the Program mode. The steps involved for altering the codes are as follows:

1. Enter the current Secondary code causing the $\overline{\text{LOCK}}$/UNLOCK 2 output to toggle.
2. Before the keypad entry enable time expires, enter the key corresponding to matrix position X4 Y1 two times. This will cause the PROGRAM MODE output to latch high, indicating that the circuit is now in the Program mode. The keypad entry enable timer is disabled during the Program mode.
3. Enter a 6 digit number from the keypad. The PROGRAM MODE output will latch low, indicating that the new codes have successfully been programmed. Of the 6 digits, the first 4 constitute the Primary code; the first 3 and the 5th constitute the Secondary code, and the first 3 and the 6th constitute the Duress code. If an error is introduced or it is desired to change the codes before the 6th digit is typed, enter the key X4 Y3. This will reset the internal memory pointer of the LS7223 and a new 6 digit number can be entered.

KEYPAD INTERFACE — The four X inputs and four Y outputs are designated for keypad interface (see FIG. 2). Since the X inputs have internal pull-ups, the maximum matrix size of 4 by 4 does not have to be utilized.

During normal operation the LS7223 will scan the matrix looking for a switch closure. Once a closure has been detected, the internal keyboard debounce logic determines if a "valid" key has been pressed or that if noise is just present. Only one valid input will be generated with any key closure. The use of internal keyboard debouncing and schmitt triggers on the inputs provides the LS7223 with very high noise immunity.

TAMPER — When a valid key has been detected by the LS7223, the entry is compared against the appropriate reference in the internal memory. If the requirements of digit value and code sequential postion are not fulfilled, the TAMPER output will momentarily go high; this indicates that an illegal code entry was attempted. The keypad entry enable timer and the memory pointer will both be reset so that entry of the code can be attempted again.

TABLE 1. PIN DESCRIPTIONS

PIN	FUNCTION	DESCRIPTION
1	VSS	Supply voltage negative.
2	RC-OSC	Determines the LS7223's internal clock frequency, which is used for keyboard scanning and debounce. A resistor (to VDD) and a capacitor (to VSS) connected to this input sets the frequency. With a 1.5MΩ resistor and a 100 pf capacitor, the internal frequency is typically 10 khz and the internal anti-bounce is typically 25 milliseconds.
3,4,5,6, 7,8,9,10	X1,X2,X3,X4 Y1,Y2,Y3,Y4	The four X inputs and four Y outputs are designed to interface to a keypad matrix whose maximum allowable size is 4 by 4.
11	PROGRAM MODE	This output goes high when the program mode is initiated. It resets to a low state after the 6 digit Primary/Secondary/Duress combination code has been programmed.
18	LOCK STATUS	Functionally, this output is identical to the LOCK/UNLOCK 1 output, with the exception that its polarity is reversed with respect to the LOCK/UNLOCK 1 output. This output is intended for driving a display lamp to indicate the lock status.
12	CAP-M	A capacitor connected between this input and VSS controls the duration of the MOMENTARY and TAMPER outputs.
13	TAMPER	Whenever a key is entered that is not a valid code element, this output goes high for a period determined by the capacitor on the CAP-M input.
14	MOMENTARY	This output generates an active high output every time the Primary code is entered. The duration of this output is determined by the capacitor on the CAP-M input.
15	ALARM	When the Duress code is entered, this output latches high to enable an external alarm. The ALARM output resets to a low state when the Primary code is entered again. This output powers-up to a low state.
16	LOCK/UNLOCK 2	Whenever the Secondary code is entered, this output toggles. The output powers-up into a low state.
17	LOCK/UNLOCK 1	Whenever the Primary code or the Duress code is entered, this output toggles. The output powers-up into a low state.
19	CAP-K	A capacitor connected between this input and VSS sets the time limit for entering a 4 digit code from the keypad. (6 digits when initiating the program mode)
20	VDD	Supply voltage positive.

Quiescent supply current: (100pf capacitor to VSS and 1.5M Ω resistor to VDD, connected to the RC-OSC input)

SYMBOL	VDD	MAX	UNIT
I_{DD}	5 VDC	12	μa
↓	9 VDC	18	↓
	12 VDC	25	
	15 VDC	35	
	18 VDC	50	

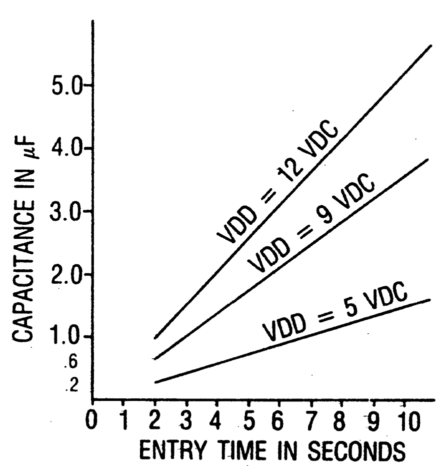
Maximum Ratings: (Voltages references to VSS)

RATING	SYMBOL	VALUE	UNIT
DC supply voltage	VDD	+4 to +18	Vdc
Operating temperature range	TA	-25 to +70	°C
Storage temperature range	TSTG	-65 to +150	°C

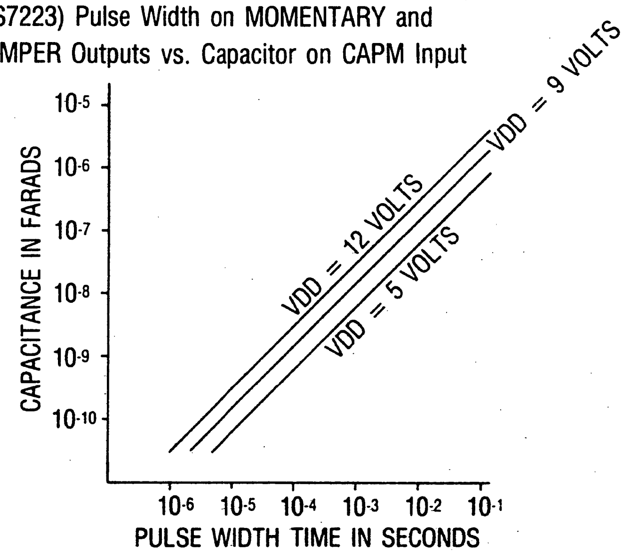
DC Electrical Characteristics:
(VSS = OV, VDD = +4 to +18V, -25°C ≤ TA ≤ +70°C unless otherwise specified)

PARAMETER	CONDITIONS	VDD	MIN	TYP	MAX	UNITS
Output source current Lock Display, Momentary $\overline{\text{LOCK}}$/UNLOCK 2 Alarm, $\overline{\text{LOCK}}$/UNLOCK1 Program Mode Outputs	Logic "1" Output $V_{OUT} \geq V_{DD}$ -2V	5VDC	1.56	2.48	—	ma
		12VDC	5.60	8.25	—	ma
		18VDC	9.07	13.2	—	ma
Output Sink Current Lock Display, Momentary, Alarm, $\overline{\text{LOCK}}$/UNLOCK1, $\overline{\text{LOCK}}$/UNLOCK2 Program Mode Outputs	Logic "0" Output $V_{OUT} \leq V_{SS}$ + .4V	5 VDC	.404	.627	—	ma
		12VDC	1.21	1.78	—	ma
		18VDC	1.9	2.77	—	ma
Output Source Current Tamper Output	Logic "1" Output $V_{OUT} \geq V_{DD}$ -2V	5VDC	.260	.413	—	ma
		12VDC	.934	1.38	—	ma
		18VDC	1.51	2.2	—	ma
Output Sink Current Tamper Output	Logic "0" Output $V_{OUT} \leq V_{SS}$ + .4V	5VDC	.067	.105	—	ma
		12VDC	.202	.297	—	ma
		18VDC	.318	.462	—	ma
Input Level Detection All Inputs	V_{IH}= Logic "1"	5VDC	3.5	—	VDD	Vdc
		12VDC	8.0	—	VDD	Vdc
		18VDC	12.0	—	VDD	Vdc
	V_{IL} = Logic "0"	5VDC	VSS	—	1.60	Vdc
		12VDC	VSS	—	4.0	Vdc
		18VDC	VSS	—	6.0	Vdc

Keypad Entry Time vs. Capacitor on CAPK Input



(LS7223) Pulse Width on MOMENTARY and TAMPER Outputs vs. Capacitor on CAPM Input



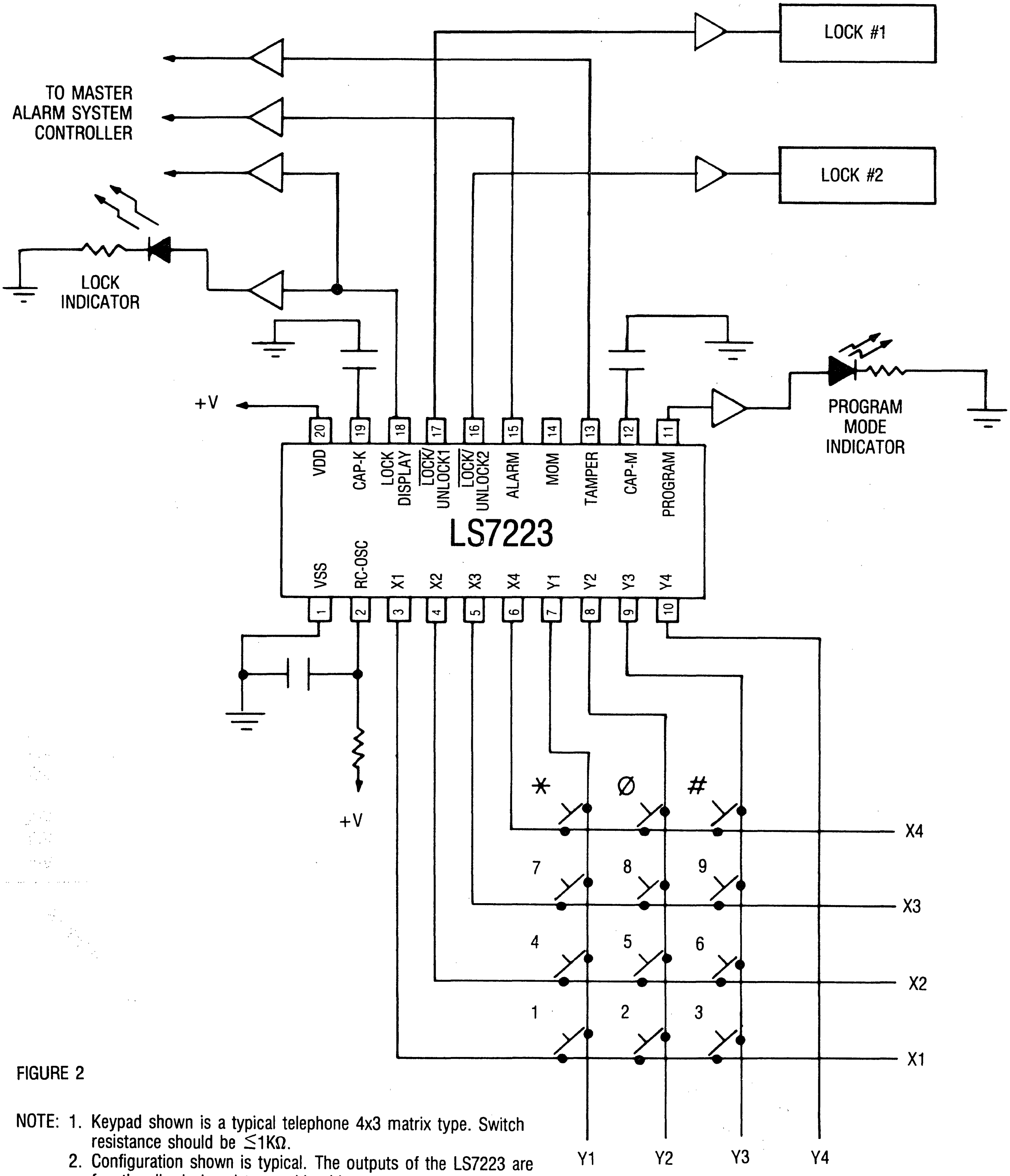


FIGURE 2

NOTE: 1. Keypad shown is a typical telephone 4x3 matrix type. Switch resistance should be ≤1KΩ.
2. Configuration shown is typical. The outputs of the LS7223 are functionally designed to provide either status or display information.

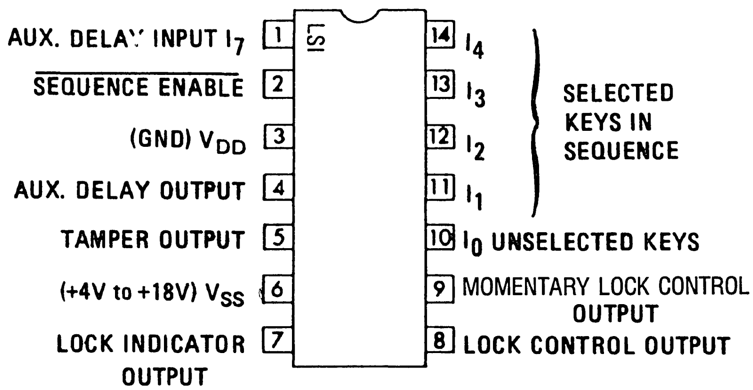
LSI/CSI

LS7225
LS7226*

DIGITAL LOCK CIRCUIT with Tamper Output

FEATURES:

- Stand Alone Lock Logic
- 5040, 4 Digit Combination with a 10 number Key Board
- Out of Sequence Detection
- Tamper Output, Sequence Enable Input
- Direct LED and Lock Relay Drive
- Externally Controlled Combination Delay
- Internal Pull Down Resistors on all Inputs
- High Noise Immunity
- Low Current Consumption (40 μA max @ 12 VDC)
- Single Power Supply Operation (+4V to +18V)
- Momentary or Static Lock Control Output
- Auxilary Delay Circuitry Included



TOP VIEW
STANDARD 14 PIN DIP
Figure 1

DESCRIPTION:

The LS7225 is a monolithic, ion implanted MOS 4 Key Keyless lock. The circuit includes sequential logic for interpretation of correct key closure; a momentary and Static Lock Control output, out of sequence detection circuitry and a tamper output.

DESCRIPTION OF OPERATION:

SELECTED KEYS AND COMBINATION DELAY:
A sequence of logical "1" 's at the inputs I_1, I_2, I_3, and I_4 (in correct sequence) sets the "SEQUENTIAL MEMORY", causing the LOCK CONTROL output to go high, the MOMENTARY LOCK CONTROL OUTPUT to go high, (See MOMENTARY LOCK CONTROL), and the lock indicator to open. An external capacitor at input I_1 (Pin 11) determines the amount of time allowed to enter the SELECTED KEYS inputs in proper sequence. The delay is a function of the external capacitance and the supply voltage (See figure 2)

UNSELECTED KEYS:
A logical "1" at this input resets the SEQUENTIAL DETECTOR" for the SELECTED KEYS inputs and causes the TAMPER output to transmit a pulse. This input should be wired to all the keys that are not part of the input sequence.

LOCK CONTROL:
This toggle output will change state (logical "1" or open) when the "SEQUENTIAL MEMORY" is set. (See SELECTED KEYS).

*See figure 7

LOCK INDICATOR:
This output is the complement of the LOCK CONTROL output (it drives an LED directly.)

MOMENTARY LOCK CONTROL:
This output goes on (Logical "1") when the "SEQUENTIAL MEMORY" is set. It goes open when input I_1 (pin 11) to the input delay level detector changes from logical "1" to logical "0". (See Input Voltage Specification)

TAMPER:
This output gives a 15µs pulse when I_3 or I_4 receives a logic "1" out of sequence or when input pin 10 (unselected key) receives a logical "1". This output is normally open. (See Figure 3) Tamper output is inhibited during the time between "power on" and the first logic "1" input to pin 11.

The tamper output should be used to discharge the capacitor at Pin 11 as shown in figure 8 and figure 4 so that I_1 must be applied again to start a new sequence when a tamper output occurs. Pulse stretcher network is indicated to provide sufficient discharge time.

SEQUENCE ENABLE:
A Logical "1" at this input disables the "SEQUENTIAL DETECTOR" thereby disallowing any sequential input. This input is intended to be used in conjunction with the TAMPER output (See Application Note 2).

POWER-ON-RESET:
A Power-On-Reset circuit resets the device to a "lock" condition upon application of power.

POWER SUPPLIES:
The circuit will operate over the range of +4 to +18 volts.

AUXILIARY DELAY NETWORK (pins 1 & 4)
This retriggerable one shot is provided for any convenient delay generation.

MAXIMUM RATINGS: (Voltages Referenced to V_{DD})

Rating	Symbol	Value	Units
DC Supply Voltage	V_{SS}	+4 to +18	Vdc
Operating Temperature Range	TA	−25 to +70	^oC
Storage Temperature Range	TSTG	−65 to +150	^oC

DC ELECTRICAL CHARACTERISTICS:
(V_{DD}= 0V, V_{SS}= +4 to +18V, $-25^oC \leq TA \leq +70^oC$ unless otherwise specified).

	VSS	MIN	TYP	MAX	UNITS
Lock Control and	5Vdc	1.50	3.00	4.50	mA
Momentary Lock	9Vdc	3.00	5.50	8.00	
Control Output Pin	12Vdc	5.00	7.50	9.50	
8 and 9 On (Logic	15Vdc	8.00	10.00	12.50	
"1") Vout=V_{SS-2}	18Vdc	9.00	11.00	13.50	
Tamper Output	5Vdc	0.05	0.10	0.30	mA
Pin 5 On	9Vdc	0.50	0.80	1.20	
(Logical "1")	12Vdc	0.70	1.00	1.60	
Vout=V_{SS}−2	15Vdc	0.90	1.50	2.00	
	18Vdc	1.50	2.10	2.60	
Aux Delay output	5Vdc	0.40	0.62	0.84	mA
Pin 4 On (Logic	9Vdc	1.24	1.62	2.04	
"1") Vout=V_{SS}−2	12Vdc	1.84	2.37	3.00	
	15Vdc	2.44	3.12	3.84	
	18Vdc	3.04	3.87	4.74	
Lock Indicator	5Vdc	0.30	0.60	1.00	mA
Output Pin 7	9Vdc	2.00	3.00	4.50	
On (Logical "1")	12Vdc	5.00	6.00	7.00	
Vout Clamp to	15Vdc	7.00	8.00	10.00	
1.7V	18Vdc	8.00	10.00	13.00	

INPUT VOLTAGE SPECIFICATIONS:

Parameter	Symbol	V_{SS} Vdc	MIN	MAX	UNITS
INPUT LEVEL DETECTORS Pins 1 and 11					
Input Logic "0"	ViL	5.0	0	V_{SS}−3	Vdc
		9	0	V_{SS}−6	
		12	0	V_{SS}−8	
		15	0	V_{SS}−9	
		18	0	V_{SS}−9.5	
Input Logic "1"	ViH	5.0	V_{SS}−1.0	V_{SS}	Vdc
		9	V_{SS}−2.5	V_{SS}	
		12	V_{SS}−4.5	V_{SS}	
		15	V_{SS}−5.0	V_{SS}	
		18	V_{SS}− 5.5	V_{SS}	
All Other Inputs					
Input Logic "0"	ViL	V_{SS}	0	V_{SS}−3	Vdc
Input Logic "1"	ViH	V_{SS}	V_{SS}−1	V_{SS}	Vdc

NOTE: Typical input load current is 6µA with input @V_{DD}, V_{SS} @+12V.

INPUT CAPACITANCE: 10 PF

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Convenience Delay					
Set-Up Time	T_S	6	8	10	µsec
Hold Time	T_H	14	16	20	µsec
Input Lock Control					
Output Delay	T_{LC}	10	13	15	µsec
Input Pulse Width	T_{iw}	100			µsec
TAmper Output					
Tamper Output					
Pulse Width	T_W			15	µs
Combination Delay					
Rise Time	tr	C+70ns			
Fall Time	tf	C+60ns			

QUIESCENT SUPPLY CURRENT: (All inputs and outputs open)

Symbol	Vss	MAX	UNITS
I_{DD}	5Vdc	20	μA
	9Vdc	30	
	12Vdc	40	
	15Vdc	50	
	18Vdc	70	

Typical Delay Hold Time Vs. Vss
(with 4.7μF Combination Delay)

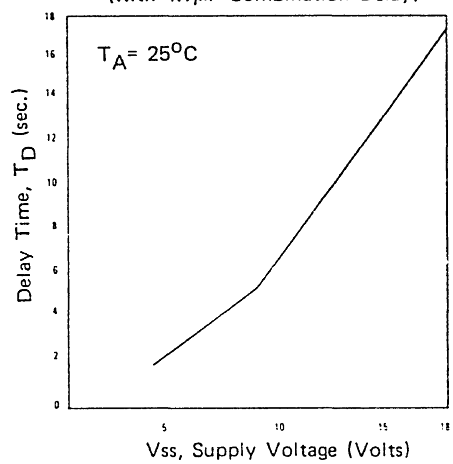
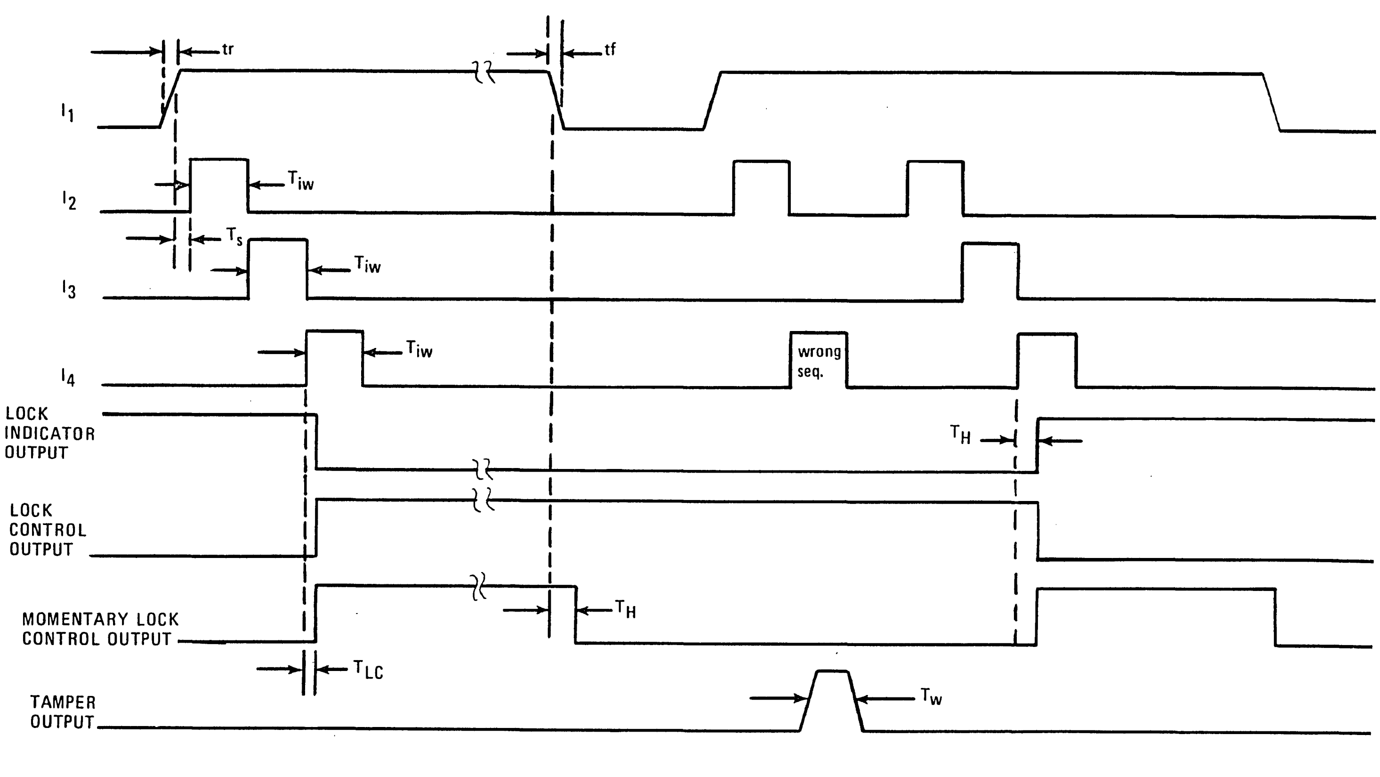


FIGURE 2



Timing Diagram
Figure 3

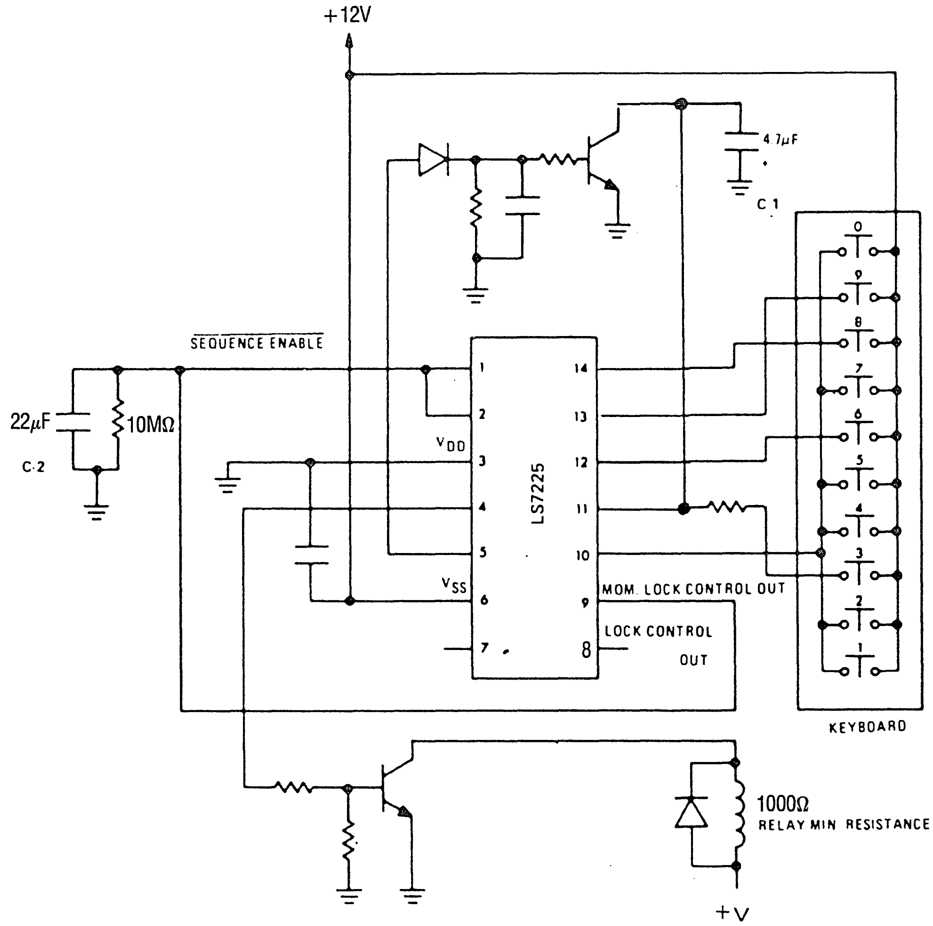


Figure 8

Typical application for independent control of combination (input) time and "UNLOCK" time.

C-1 determines input time.
C-2 determines "UNLOCK" time.

Note: With this configuration one tamper pulse is transmitted at the start of "UNLOCK" time.

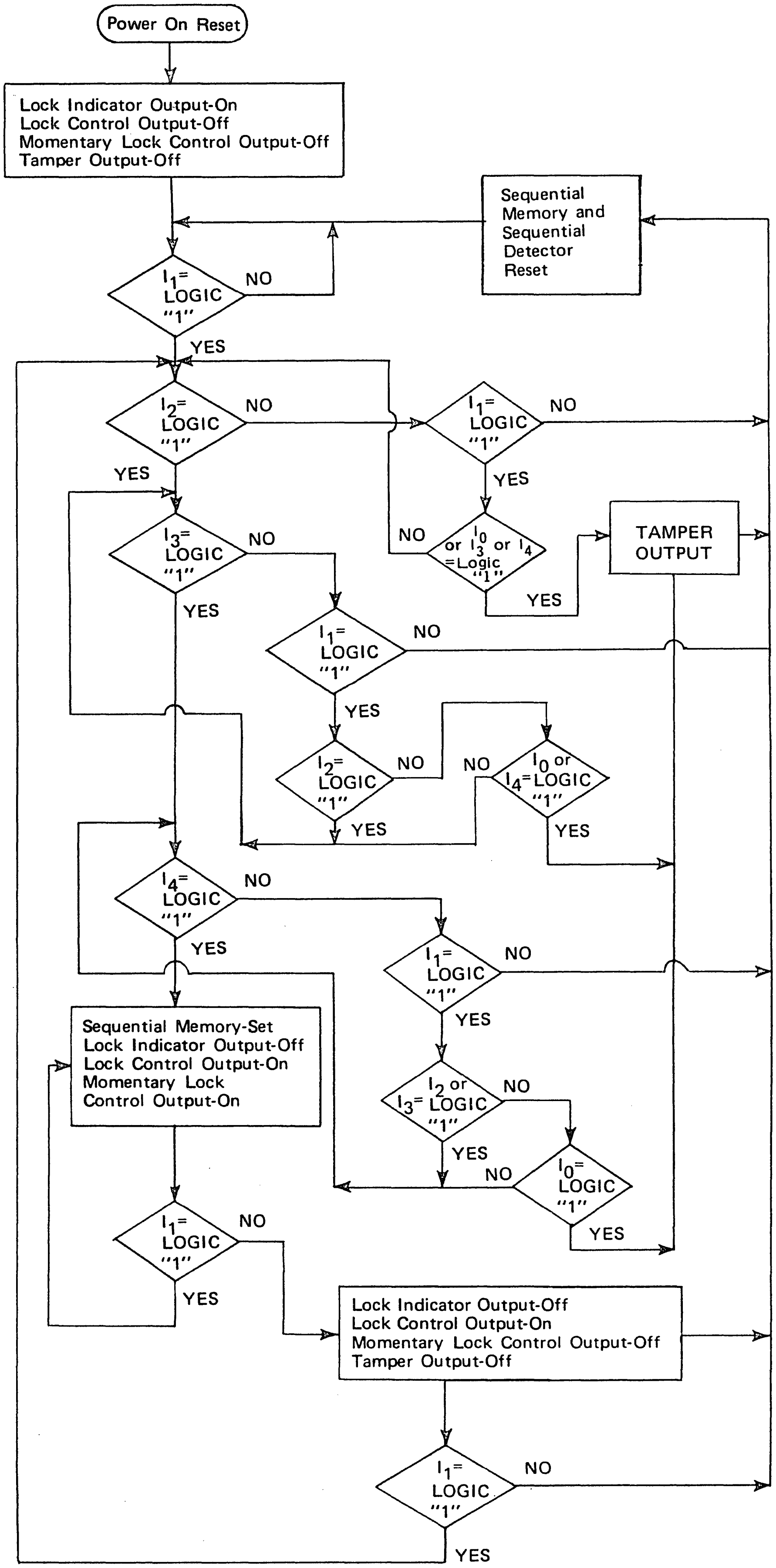

Power On Reset
Lock Indicator Output-On
Lock Control Output-Off
Momentary Lock Control Output-Off
Tamper Output-Off
Sequential Memory and Sequential Detector Reset
I_1= LOGIC "1"
NO
YES
I_2= LOGIC "1"
I_1= LOGIC "1"
I_0 or I_3 or I_4 =Logic "1"
TAMPER OUTPUT
I_3= LOGIC "1"
I_1= LOGIC "1"
I_2= LOGIC "1"
I_0 or I_4=LOGIC "1"
I_4= LOGIC "1"
I_1= LOGIC "1"
I_2 or I_3= LOGIC "1"
I_0= LOGIC "1"
Sequential Memory-Set
Lock Indicator Output-Off
Lock Control Output-On
Momentary Lock Control Output-On
I_1= LOGIC "1"
Lock Indicator Output-Off
Lock Control Output-On
Momentary Lock Control Output-Off
Tamper Output-Off
I_1= LOGIC "1"

Figure 6

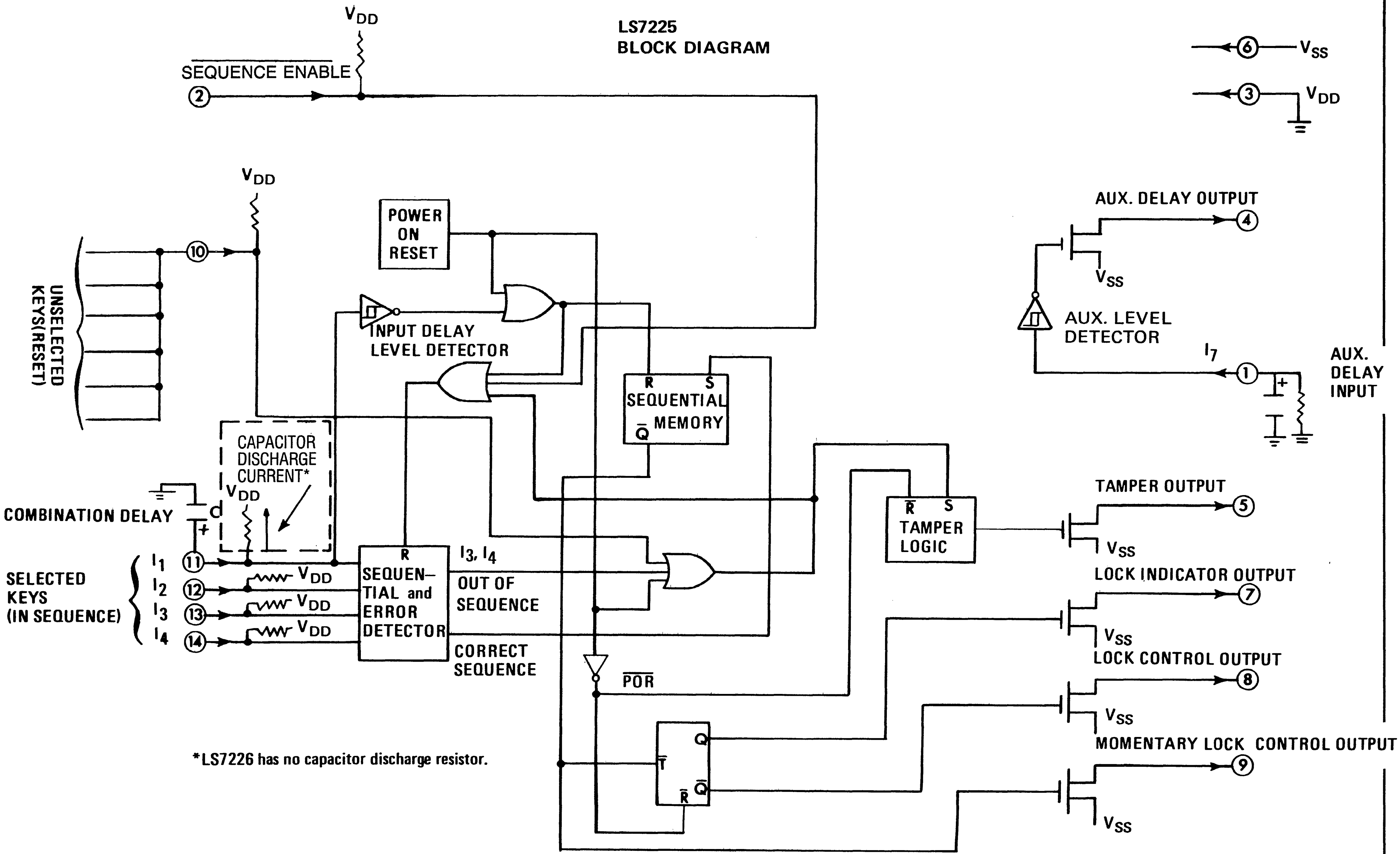
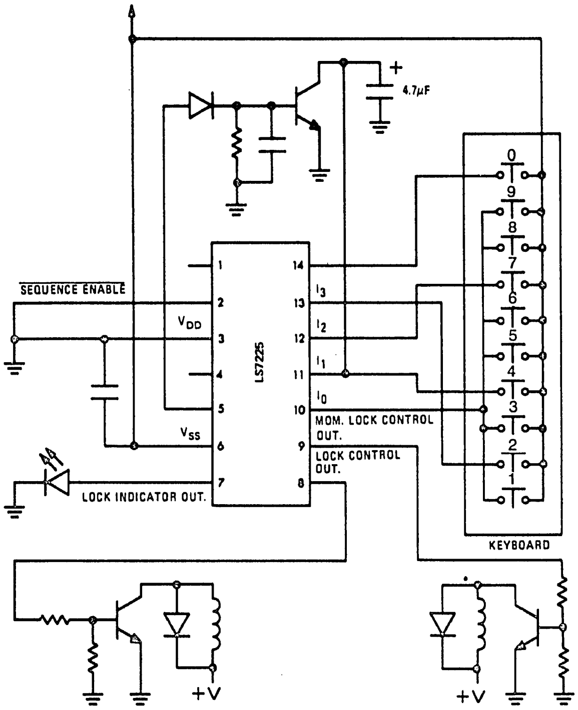

LS7225
BLOCK DIAGRAM
SEQUENCE ENABLE
POWER ON RESET
INPUT DELAY LEVEL DETECTOR
UNSELECTED KEYS(RESET)
CAPACITOR DISCHARGE CURRENT*
COMBINATION DELAY
SELECTED KEYS (IN SEQUENCE)
SEQUENTIAL MEMORY
SEQUENTIAL and ERROR DETECTOR
OUT OF SEQUENCE
CORRECT SEQUENCE
POR
TAMPER LOGIC
AUX. DELAY OUTPUT
AUX. LEVEL DETECTOR
AUX. DELAY INPUT
TAMPER OUTPUT
LOCK INDICATOR OUTPUT
LOCK CONTROL OUTPUT
MOMENTARY LOCK CONTROL OUTPUT
*LS7226 has no capacitor discharge resistor.

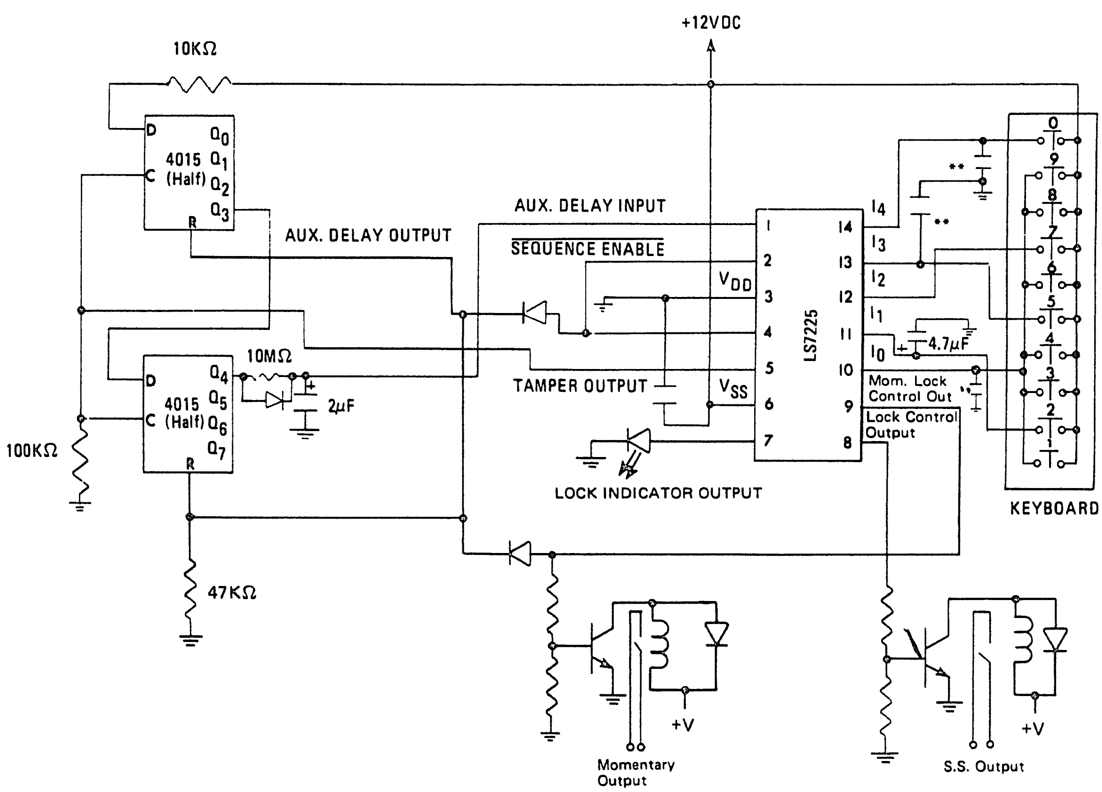
Figure 7



A typical circuit is shown in the schematic diagram. When input I_1 (pin 11) goes high, the circuit is ready to accept the unlocking input sequence at I_2, I_3 and I_4 (pins 12, 13, and 14 respectively). If the Keys associated with these inputs are depressed exactly in sequence of I_1, I_2, I_3 and I_4, the lock control output (pin 8) will become ON, the momentary lock control output (pin 9) will be ON until input I_1 (pin 11) becomes low. The state ON of the lock control will be indicated by the OFF Condition of the lock indicator output (pin 7) which will render the LED OFF (an indication of unlock condition). If the Keys are depressed in any sequence other than as described above, the internal "SEQUENTIAL DETECTOR" will be reset and the entire sequence must be repeated. The lock control output is turned OFF by repeating the input sequence. The Momentary Lock Control output goes high each time the correct sequence is entered. The specific code shown is 4720.

TYPICAL APPLICATION OF LS7225 IN MACHINE OR AREA ACCESS

Figure 4



TYPICAL TAMPER LOCK DISABLE APPLICATION

Figure 5

A System with 12 seconds reset after 5 TAMPER outputs and support circuitry is shown. The specific code is 2750. If the Keys associated with the given code are not depressed exactly in sequence or if any Key associated with the unselected Keys (Reset) is depressed, the pulse from the Tamper output will clock the 4015 Dual 4-bit shift register which transmits a logical "1" from input D to output Q4 after five clock pulses. A logical "1" in Q4 will charge up the 2µF capacitor, turn on the AUX. DELAY OUTPUT for 12 seconds and keep the LS7225 in the RESET Mode vis SEQUENCE ENABLE (pin 2). After the 2µF capacitor discharges, pin 2 of LS7225 becomes a logical "0" and the keyless lock integrated circuit is ready to accept key inputs.

**NOTE: Due to mechanical keyboard bounce it may be necessary to include these (750pf) capacitors.

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7228/LS7229 ADDRESS DECODER/TWO PUSHBUTTON DIGITAL LOCK

REVISED NOVEMBER 1985

FEATURES:
- Stand alone lock logic
- 9 bit code determined by 9 parallel inputs
- Two options of code input available:
  LS7228 – Dual train pulsed input
  LS7229 – Two momentary switches
- Out of sequence disabling circuit
- Current source lock control output
- External controlled delay to set maximum inter-pulse time.
- Single power supply operation (2.5V to 15.0V)
- Low standby current (15uA maximum)
- 16 pin dual-in-line plastic package
- Cascadable

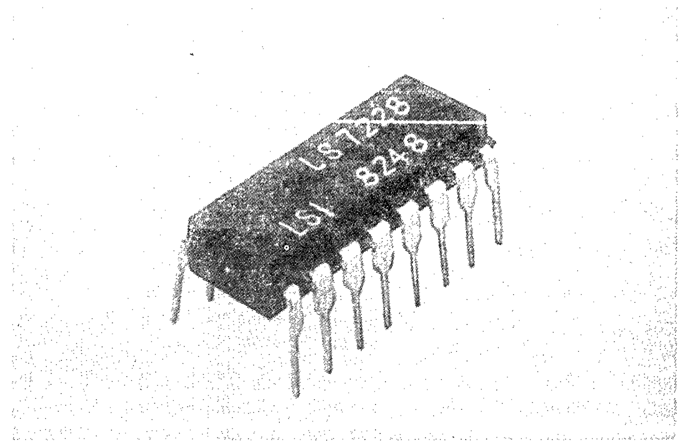
DESCRIPTION:
LS7228/LS7229 are monolithic ion implanted MOS encoder circuits. Each circuit includes logic for interpretation of correct sequential key closure or pulse input and a momentary lock control output. An out of sequence detection will disable any further insertions, and a new sequence may be reapplied after a delay time, determined by an external R/C time constant.

The LS7228 utilizes a dual train input format where the input "one's" data is applied to pin 13 and the input "zero's" is applied to pin 14. The common input (pin 15) is not used. (See figure 4). The LS7229 utilizes two momentary switches and pins 13, 14 and 15 in a manual operating mode.

PROGRAMMING 9 BIT CODE:
Pin 1 (leading bit) and through Pin 9 (end bit) with 512 (leading bit) different combinations. To program a Logic 1 the pin is left floating. To program a Logic 0 the pin is tied to VDD (GND).

LOCK CONTROL OUTPUT:
Code entry is made at the one's port or the zero's port with logical one levels (+ volts) and returned to the logical zero level (GND) in sequential order. The lock control output will change to a logical one after the last correct bit entry returns to logical zero and will remain at a logical one for the period of the external R/C delay. If it is desired to maintain a constant logical one output, a tenth entry either at the one or zero port must be held at a logical one level.

STANDBY AND OPERATING CURRENT:
1. Upon application of supply voltage, the standby section is activated, leaving the remaining portion of the circuit unenergized.



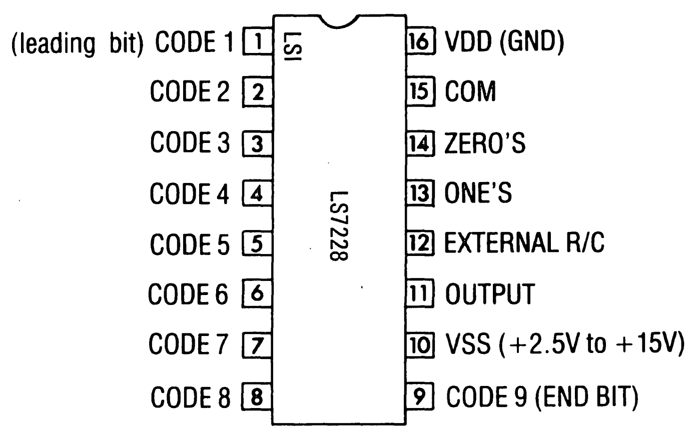


Figure 1
TOP VIEW
Standard 16 pin DIP

STANDBY AND OPERATING CURRENT (cont'd.)
(Standby current is 15 μA max.)
2. The entire circuit is energized by entering the first bit in the code pattern and will be energized only during the selected external R/C delay time, every bit entry will refresh the external delay time. (Operating current is 5mA max.)

CASCADING:
See Figure 4.

DESCRIPTION OF INTERNAL OPERATION: (See fig. 3)
When entering code to either the one's port or the zero's port, an

external capacitor is charged and an internal inhibit is removed to allow further code insertion, providing that the previous insertion was the correct code. In effect, a one is transmitted through the nine BIT shift register if the input sequence agrees with the program applied to pins one through nine.

If an incorrect insertion occurs, the one is prevented from advancing even though further code insertions occur, keeping the external capacitor fully charged. Only the removal of code entrys will allow the external capacitor to discharge and reset the error logic, thereby permitting a new attempt at entering the correct code.

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_a	−25 to +70	°C
Voltage (any pin to V_{SS})	V_{max}	−30 to +0.5	VOLTS

DC ELECTRICAL CHARACTERISTICS

INPUT SPECIFICATIONS

INPUT VOLTAGE

Program Inputs (Pins 1 through 9)

	MIN.	MAX.	UNITS
Logical "1"	V_{SS}-0.5	V_{SS}	VOLTS
Logical "0"	0	V_{SS}−2.5	VOLTS

Serial Inputs (Pins 13, 14, 15)

	SYMBOL	V_{SS} (VDC)	MIN	TYP.	MAX.	UNITS
Input Logic "1" Switching From Logic ("0") to Logic ("1")	V_{IL}	2.5	1.9	1.65	2.5	VDC
		5.0	4.3	4.0	5.0	VDC
		9.0	8.0	7.6	9.0	VDC
		12.0	11.0	10.6	12.0	VDC
		15.0	14.0	13.6	15.0	VDC
Input Logic "0" Switching From Logic ("1") to Logic ("0")	V_{IH}	2.5	0	.7	.3	VDC
		5.0	0	1.5	.5	VDC
		9.0	0	2.0	1.0	VDC
		12.0	0	4.0	1.5	VDC
		15.0	0	4.5	2.0	VDC

External R Applied To Pin 12

SYMBOL	V_{SS}	MIN	TYP.	MAX.	UNITS
R	2.5	33	—	3300	K Ω
	5.0	27	—		K Ω
	9.0	22	—		K Ω
	12.0	15	—		K Ω
	15.0	10	—	3300	K Ω

External R/C Input (Pin 12)

	SYMBOL	V_{SS} (VDC)	TYP.	UNITS
Input Logic "1" Switching From Logic ("0") to Logic ("1")		2.5	1.6	VDC
		5.0	3.8	VDC
		9.0	7.5	VDC
		12.0	10.4	VDC
		15.0	13.4	VDC

	SYMBOL	V_{SS}	TYP.	UNITS
Input Logic "0" Switching From Logic ("1") to Logic ("0")		2.5	.6	VDC
		5.0	1.2	VDC
		9.0	2.2	VDC
		12.0	4.5	VDC
		15.0	6.0	VDC

Input Current To V_{SS} ($V_{IN} = V_{DD}$)

	TYPICAL	MAX.	UNITS
Program Inputs	Standby 1	—	nA
(Pins 1 through 9)	Operating 2	−5	uA

Input Current To V_{DD} (V_{IN} to V_{SS})

Serial Input			
(Pins 13 and 14)	3	5	uA
(Pin 15)	1.5	3	uA

MAX FREQUENCY - vs - OPERATING VOLTAGE FOR DUAL TRAIN OPERATION is Linear with respect to capacitor size applied to pin 12. See Dynamic Electrical Characteristics (See below)

OUTPUT SPECIFICATIONS

LOCK CONTROL OUTPUT PIN 11

SOURCE CURRENT	V_{SS}	MIN.	TYP.	MAX.	UNITS
$V_{OUT} = V_{SS}$ - .5 VDC	2.5VDC	1.4	2.5	3.5	mA
	5.0VDC	3.0	5.6	8.0	mA
	9.0VDC	5.0	9.0	13.0	mA
	12.0VDC	6.0	11.0	16.0	mA
	15.0VDC	7.0	13.0	18.0	mA
$V_{OUT} = V_{SS}$ - 1.0 VDC	2.5VDC	2.2	4.0	5.6	mA
	5.0VDC	6.0	11.0	16.0	mA
	9.0VDC	10.0	18.0	25.0	mA
	12.0VDC	12.0	22.0	31.0	mA
	15.0VDC	14.0	26.0	36.0	mA
$V_{OUT} = V_{SS}$ - 1.5 VDC	2.5VDC	2.7	5.0	7.0	mA
	5.0VDC	8.0	14.0	20.0	mA
	9.0VDC	14.0	26.0	36.0	mA
	12.0VDC	18.0	33.0	46.0	mA
	15.0VDC	20.0	38.0	53.0	mA

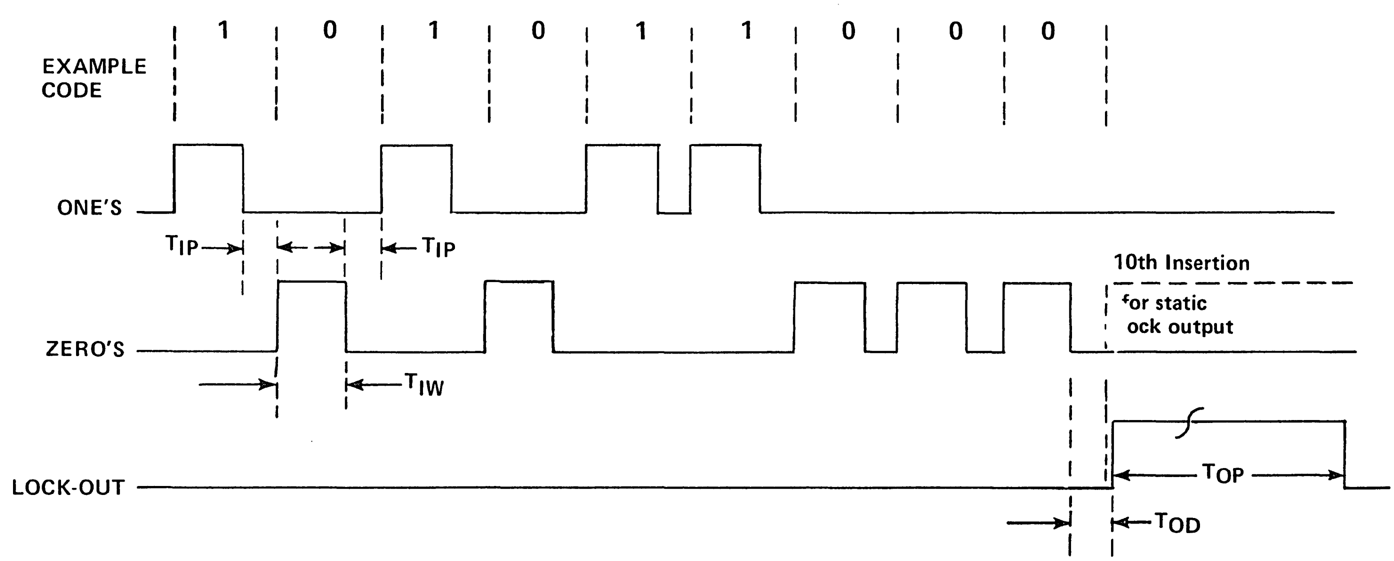
NOTE: Pin 11 (Lock Control Output) is only a current source. Use a resistor to ground (V_{DD}) if driving capacitor load.

DYNAMIC ELECTRICAL CHARACTERISTICS (See Fig. 2)

PARAMETER	SYMBOL	V_{SS}	MIN.	TYP.	MAX.	UNITS
Input Pulse Width (with C on Pin 12 $\leq$.01 uf)	T_{IW}	2.5	50	—	—	usec
		5.0	80	—	—	usec
		9.0	120	—	—	usec
		12.0	160	—	—	usec
		15.0	200	—	—	usec
Output Delay	T_{OD}	—	20	40	70	usec

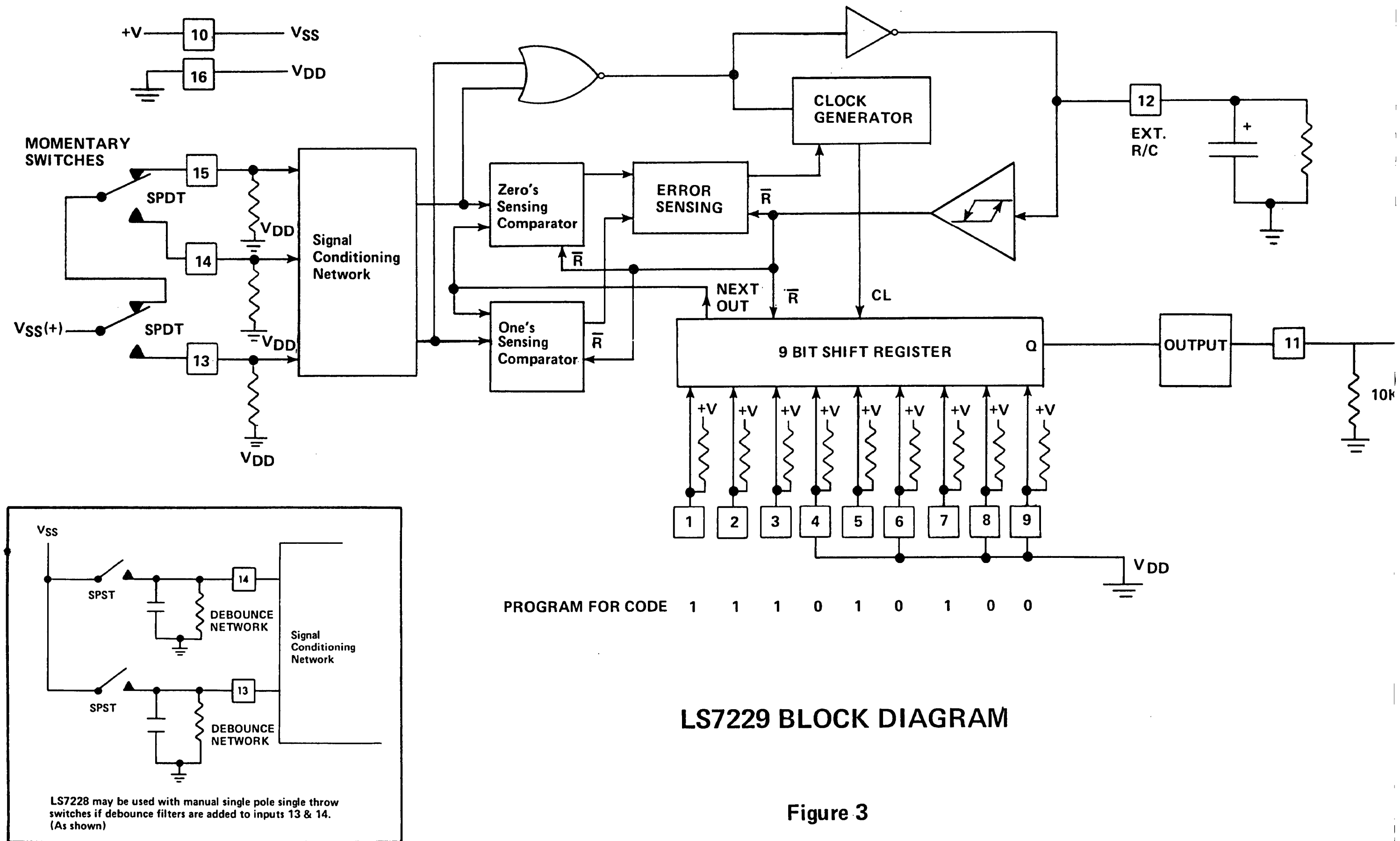
Output Pulse Width T_{OP} typically 1.25 time constants of external RC network applied to Pin 12

PARAMETER	SYMBOL	V_{SS}	MIN.	TYP.	MAX.	UNITS
Input Interpulse time	T_{IP}		30	—	T_{OP}	usec



TIMING DIAGRAM

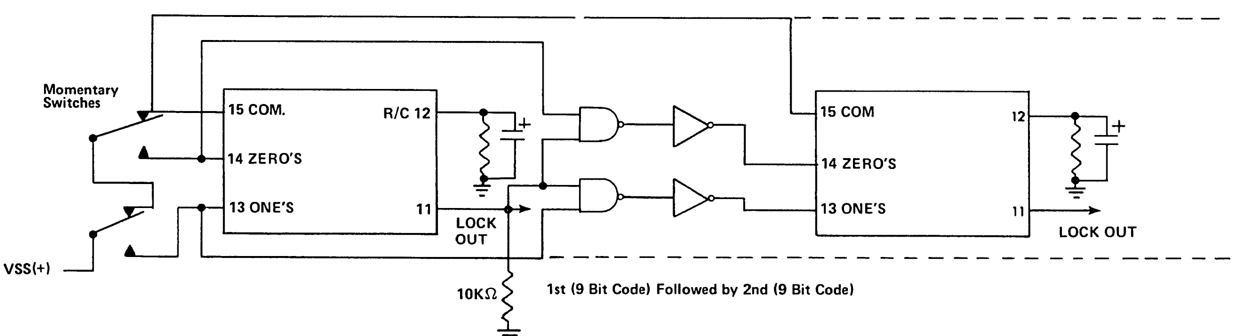
Figure 2



LS7229 BLOCK DIAGRAM

Figure 3

DUAL SWITCH CASCADING SERIES (LS7229)



DUAL TRAIN CASCADING SERIES PARALLEL (LS7228)

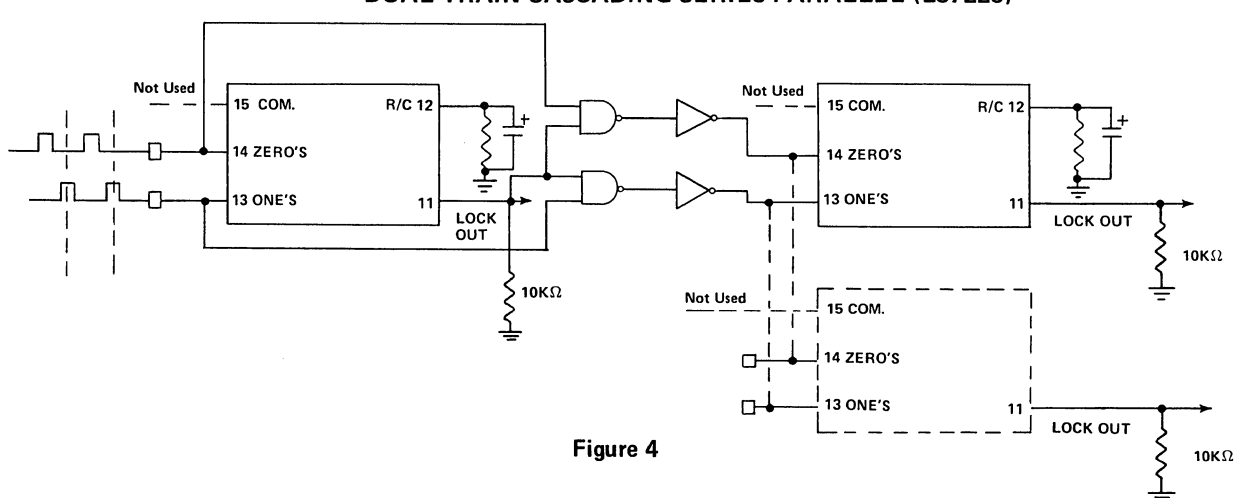


Figure 4

LS 7231-5

TOUCH CONTROL CONTINUOUS DIMMER LIGHT SWITCH AND A.C. MOTOR SPEED CONTROLLER*

FEATURES:

- Phase-locked loop synchronization produces pure AC waveform across output load with no DC offset
- Provides ON/OFF or brightness control of incandescent lamps and ON/OFF or speed control of A.C. motors without the use of mechanical switches.
- Controls brightness by controlling the AC Duty Cycle
- Provides speed control of AC Motors, such as shaded pole and universal series motors
- Controls the "Duty Cycle" from 25% to 88% (on time angles for AC half cycles between 41° and 159° respectively)
- Operates at 50Hz/60Hz line frequency
- Provides control through transformers for low voltage lighting applications
- Input for extensions or remote sensors
- Input for slow dimming
- 12V to 18V DC supply voltage

DESCRIPTION:

LS 7231 through LS 7235 is a series of monolithic, ion implanted MOS circuits that are specifically designed for brightness or ON/OFF control of incandescent lamps or speed of AC motors used on the AC line. The outputs of these chips control the brightness of a lamp or speed of an AC motor by controlling the firing angle of a triac connected in series with the lamp or AC motor. All internal timings are synchronized with the line frequency by means of a built-in phase locked loop circuit. The output occurs once every half cycle of the line frequency. Within the half-cycle, the output can be positioned anywhere between 159° phase angle for maximum brightness/speed and 41° phase angle for minimum brightness/speed in relation to the line frequency. The positioning of the output is controlled by appling a low level at the sensor input or a high level at the slave input.

These functions may be implemented with very few interface components which is described in the application examples. When implemented in this manner, a touching of the sensor plate causes the lamp brightness or AC motor speed to change as follows:

1. If the sensor is touched momentarily (32ms to 332ms), the lamp or AC motor is:

   (a) turned off it it was on.

   (b) turned on if it was off. The brightness/speed resulting is either full brightness/speed or, depending on the circuit type, a previous brightness/speed stored in the memory.

CONNECTION DIAGRAM — TOP VIEW
STANDARD 8 PIN PLASTIC DIP

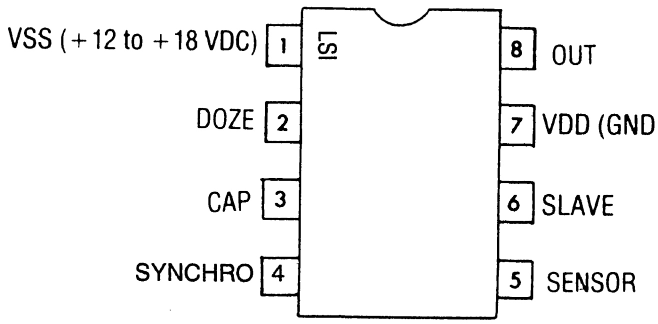


FIGURE 1

* Some motors may require a higher minimum duty cycle (mask option)

2. If the sensor is touched for a prolonged time (more than 332ms) the light intensity changes slowly. As long as the touch is maintained, the change continues; the direction of change reverses whenever the maximum or minimum brightness is reached.

   The circuit also provides an input for slow dimming. By applying a slow clock to this input, the lamp can be dimmed slowly until total turn off occurs. This feature can be useful in children's bedroom lights.

INPUT/OUTPUT DESCRIPTION:

VSS (Pin 1).
Supply voltage positive terminal.

DOZE (Pin 2).
A clock applied to this input causes the brightness to decrease in equal increments with each negative transition of the clock. Eventually, when the lamp becomes off, this input has no further effect. The lamp can be turned on again by activating either the SENSOR input or the SLAVE input. For the transition from maximum brightness to off, a total of 83 clock pulses are needed at the DOZE input.

When either the SENSOR or the SLAVE input is active, the DOZE input is disabled.

CAP (Pin 3).
The CAP input is for external component connection. A capacitor of .047uF ± 20% should be used at this input.

The functional differences of different variations of the light dimmer circuits are explained in Table I and the output phase angle diagrams in Fig. 3.

TABLE I

TYPE	SENSOR (TOUCH) DURATION				DIMMING DIRECTION REVERSAL
	MOMENTARY (32ms to 332ms) (note 3)		PROLONGED (More than 332ms) (note 3)		
	PRE-TOUCH BRIGHTNESS	POST-TOUCH BRIGHTNESS	PRE-TOUCH BRIGHTNESS	POST-TOUCH BRIGHTNESS	
LS7231	Off	Max.	Off	Starts varying at Min.	N/A
	Max.	Off	Max.	Starts varying at Max.	N/A
	Intermediate	Off	Intermediate	Starts varying at Pre-Touch brightness	NO
LS7232	Off	Memory (See note 1)	Off	Starts varying at Memory (Note 2)	YES
	Max.	Off	Max.	Starts varying at Max.	N/A
	Intermediate	Off	Intermediate	Starts varying at Pre-Touch brightness	YES
LS7233	Off	Max.	Off	Starts varying at Min.	N/A
	Max.	Off	Max.	Starts varying at Max.	N/A
	Intermediate	Off	Intermediate	Starts varying at Pre-Touch brightness	YES
LS7234	Off	Memory (See note 1)	Off	Starts varying at Memory (Note 2)	NO
	Max.	Off	Max.	Starts varying at Max.	N/A
	Intermediate	Off	Intermediate	Starts varying at Pre-Touch brightness	NO
LS7235	Off	Max.	N/A	N/A	N/A
	Max.	Off	N/A	N/A	N/A

NOTE 1. "Memory" refers to the brightness stored in the memory. The brightness is stored in the memory when the light is turned off by momentary sensor touch. First time after power-up, momentary touch produces max. brightness.

NOTE 2. First time after power-up, prolonged touch causes intensity to vary starting at min.

NOTE 3. The time figure is based on 60Hz synchro frequency. For 50Hz the figures are 39ms and 399ms.

SYNCHRO (Pin 4).
The a-c line frequency (50Hz/60Hz), when applied to this input, synchronizes all internal timings through a phase locked loop. The signal for this input may be obtained from the line voltage by employing the circuit arrangment shown in the application notes.

SENSOR (Pin 5).
A low level applied to the sensor input controls the turn on or turn off of the output as well as its phase angle with respect to the synchro input. A description of this is provided in the general description and Table I.

SLAVE (Pin 6).
The SLAVE input is functionally similar to the SENSOR input with the exception that the active level is a logical high as compared to the logical low level for the sensor input. It is recommended that the SLAVE input be used instead of the SENSOR input when long extension wires are used between the sensing plates (or switches) and the dimmer chips.

VDD (Pin 7).
Supply voltage negative terminal.

OUT (Pin 8).
The output is a low level pulse occurring once every half cycle of the synchro signal. The phase angle, ϕ of the output in relation to the synchro signal controls the lamp brightness.

In continuous dimming operation (i.e., when the sensor input is continuously held low) the output phase angle, ϕ sweeps up and down between 41° and 159° continuously. The time vs ϕ curve, however, is not a linear one (see Fig. 3). Between two maxima on this curve, there are 4 discontinuous points labeled A_1, B_1, B_2, A_2. The discontinuities are as follows:

1. From maximum to A_1. In this region, ϕ is changed by equal increments ($\Delta\phi$) for every 2 synchro clocks.
2. From A_1 to B_1. In this region, the increments ($\Delta\phi$) take place for every 4 synchro clocks.
3. From B_1 to B_2. In this region ϕ is held at a constant level ($\Delta\phi=0$).
4. From B_2 to A_2. Same as 2.

From A_2 to Maximum. Same as 1.

The slower rate of change in ϕ over $A_1B_1B_2A_2$ region is to accommodate for eye adjustment at lower light intensity.

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
DC supply voltage	VSS	+20	Volt
Any input voltage	V_{IN}	VSS + .5	Volt
Operating temperature	T_A	0 to +80	°C
Storage temperature	Tstg	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS:
(T_A=0 to 80°C, all voltages referenced to VDD)

PARAMETER	SYMBOL	MIN.	TYP	MAX	UNIT	CONDITIONS/ REMARKS
Supply voltage	V_{SS}	+12	—	+18	Volts	
Supply current	I_{SS}		1.0	1.5	mA	
Input Voltages						
Doze LO	V_{IZL}	0	—	V_{SS}-6	Volts	@ Vss=+15V,
Doze HI	V_{IZH}	VSS-2	—	V_{SS}	Volts	output off
Synchro LO	V_{IRL}	0	—	V_{SS}-9.5	Volts	
Synchro HI	V_{IRH}	V_{SS}-5.5	—	V_{SS}	Volts	
Sensor LO	V_{IOL}	0	—	V_{SS}-8	Volts	
Sensor HI	V_{IOH}	V_{SS}-2	—	V_{SS}	Volts	
Slave LO	V_{IVL}	0	—	V_{SS}-8	Volts	
Slave HI	V_{IVH}	V_{SS}-2	—	V_{SS}	Volts	
Input Current:						
Synchro, Sensor & Slave HI	I_{IH}	—	—	110	uA	With Series 1.5MΩ Resistor to 115 VAC Line
Doze HI	—	—	—	5	nA	
Doze LO	—	—	—	5	nA	
Output HI Vltg		—	V_{SS}	—	Volts	
Output LO Vltg		—	V_{SS}-4	—	Volts	
Output Sink Current	—	25	—	—	mA	@ V_{SS}=+15V V_O=V_{SS}-3

FREQUENCY CHARACTERISTICS (See Fig. 2 & 3)

All timings are based on f_S = 60Hz, unless otherwise specified.

PARAMETER	SYMBOL	MIN	TYP.	MAX.	UNIT
Synchro Frequency	f_S	40	—	70	Hz
Sensor Duration (ON/OFF Oper.)	T_{S1}	32	—	332	ms
Sensor Duration (Dimming Oper.)	T_{S2}	332	—	infinite	ms
Doze Frequency	—	—	—	500	Hz
Output Pulse Width	TW	40	—	55	µS
Output Phase-Angle (Note 1)	0	41	—	159	degrees
ϕ Period (Max to Max in continuous dimming)	—	—	3.74	—	sec.
$A_1B_1 = B_2A_2$, duration	—	—	934	—	ms
B_1B_2, Min. intensity dwell	—	—	500	—	ms

Note 1. In the circuit arrangement described in the application notes, the synchro input signal is delayed in phase in relation to the line frequency by about 6°, resulting in a ϕ range between 35° and 152°. With higher R-C value the phase angle range may be shifted down further.

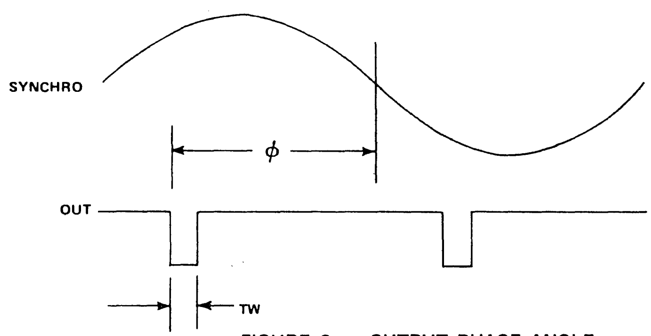
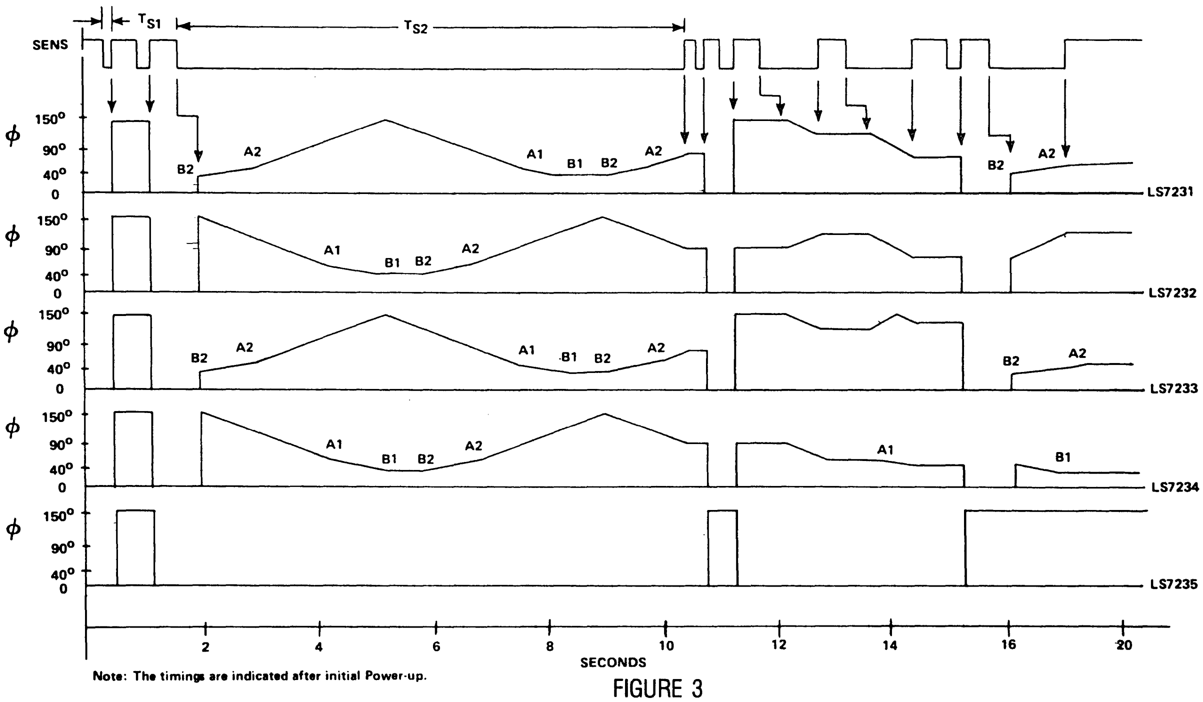


FIGURE 2 — OUTPUT PHASE ANGLE



Note: The timings are indicated after initial Power-up.

FIGURE 3

OUTPUT PHASE-ANGLE, ϕ Vs, SENSOR INPUT

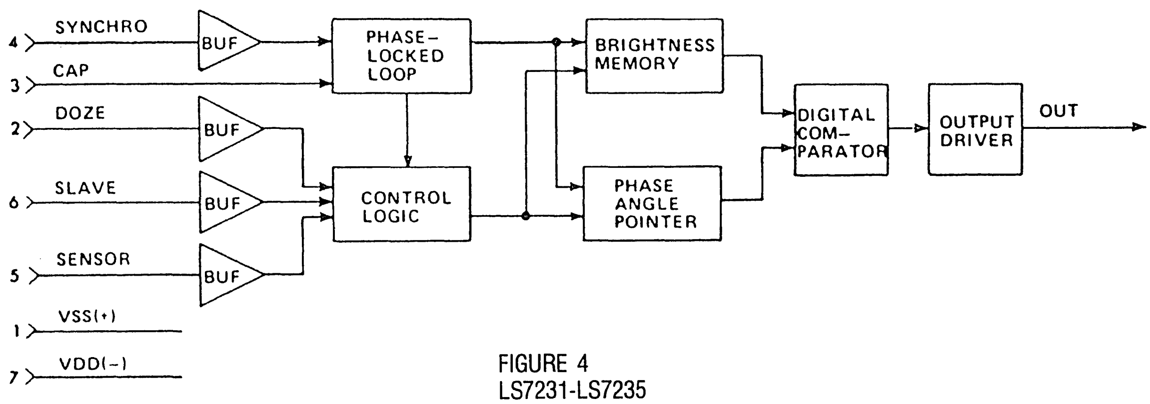


FIGURE 4
LS7231-LS7235
BLOCK DIAGRAM

APPLICATION EXAMPLES:

A typical implementation of the light dimmer circuit is shown in Fig. 5. Here the brightness of the lamp is set by touching the sensor plate. The functions of different components are as follows:

- The 15V DC supply for the chip is provided by Z, D1, R1, C2 and C5.
- R_2 and C_4 generate the filtered signal for the SYNCHRO input for synchronizing the internal PLL with the line frequency.
- R_3 and C_7 act as a filter circuit for the electronic extension. If extensions are not used, the slave input (Pin 6) should be tied to V_{DD} (Pin 7).
- R_4, R_5 and R_6 set up the sensitivity of the sensor input. C_6 provides noise filtering.
- C_3 is the filter capacitor for the internal PLL.
- D_2 limits the positive excursion of Triac gate to about V_{SS} +.5V. This positive excursion of the gate may occur during the triggered state of certain triacs.
- C_1 and L are RF filter circuits.

In the case of momentary power failure, the circuit state remains unchanged for a period of up to 1 sec. For longer power interruptions, the output is shut off.

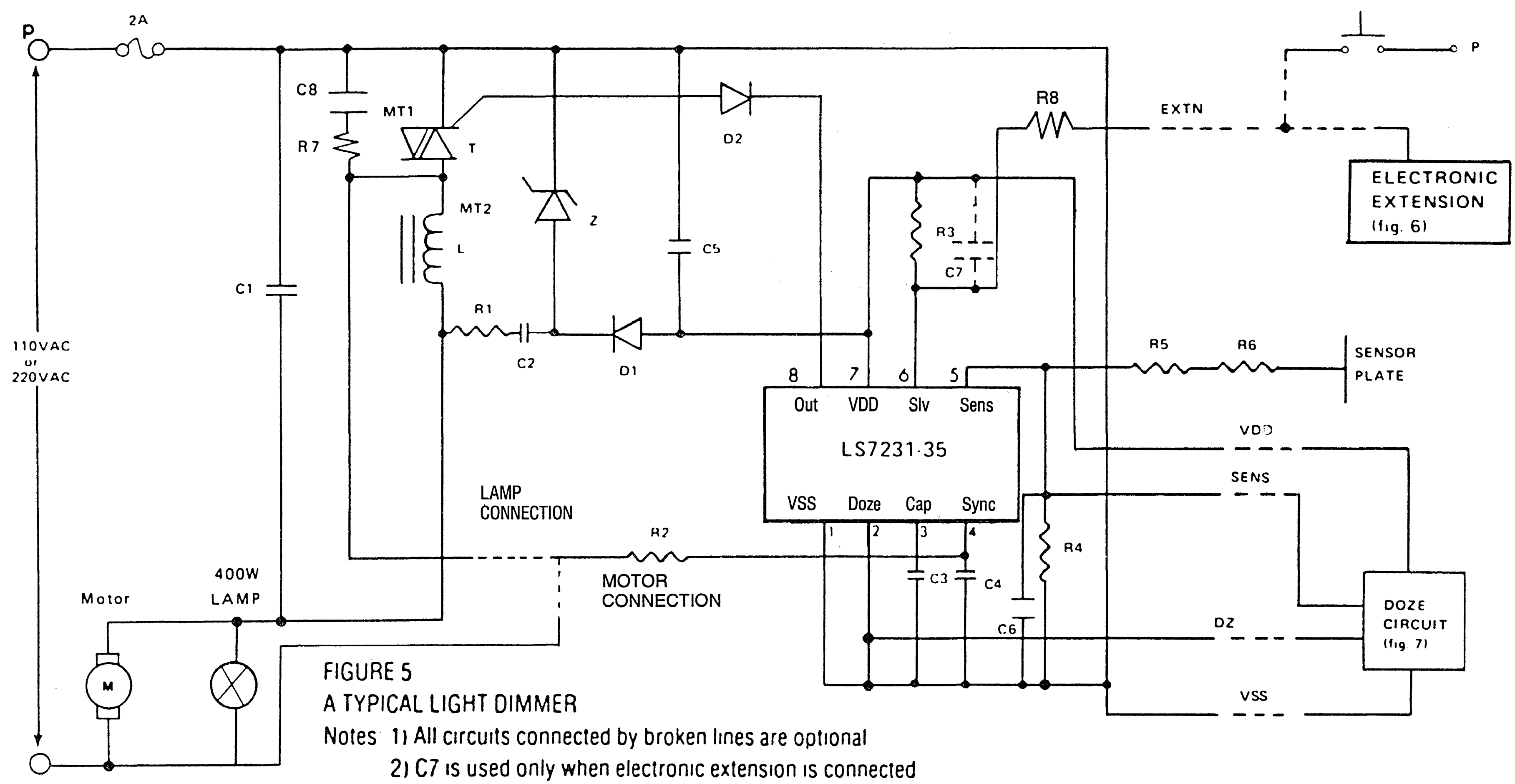


FIGURE 5
A TYPICAL LIGHT DIMMER

Notes: 1) All circuits connected by broken lines are optional
2) C7 is used only when electronic extension is connected
3) Connection between Pin 1 & Pin 2 should be broken when Doze circuit is used

115V

C1 = 0.15μF/250VAC
C2 = 0.22μF/250VAC
C3 = .047μF/16V
C4 = 470pF/600V
C5 = 47μF/25V
C6 = 680pF/50V
C7 = .2μF/25V
R1 = 270Ω/2W
R2 = 1.5M/¼M
R3 = 680KΩ/¼W
** R7 = 1.8KΩ/2W
R8 = 100KΩ/¼W

R4 = 1MΩ to 5MΩ/¼W
(select for sensitivity)
R5, R6 = 2.7MΩ/¼W
D1, D2 = 1N4148
Z = 15V/1W (Zener)
T = TL500D or
Q4004L4 triac (TYPICAL)
L = 100μH
(RFI Filter)
** C8 = .047μF/250V

**R7 and C8 Network may be required for some inductive loads.

220V

C1 = 0.15μF/400VAC
C2 = 0.22μF/400VAC
C3 = .047μF/16V
C4 = 470pF/600V
C5 = 47μF/25V
C6 = 680pF/50V
C7 = .2μF/25V
** C8 = .047μF/400V
R1 = 1KΩ/1W
R2 = 1.5MΩ/ 1/4W
R3 = 680KΩ/¼W
** R7 = 1.8KΩ/2W
R8 = 100KΩ/¼W

R4 = 1MΩ to 5MΩ/¼W
R5, R6 = 4.7MΩ/¼W
D1, D2 = 1N4148
Z = 15V/1W (Zener)
T = Q5004 L4 triac (TYPICAL)
L = 200μH
(RFI Filter)

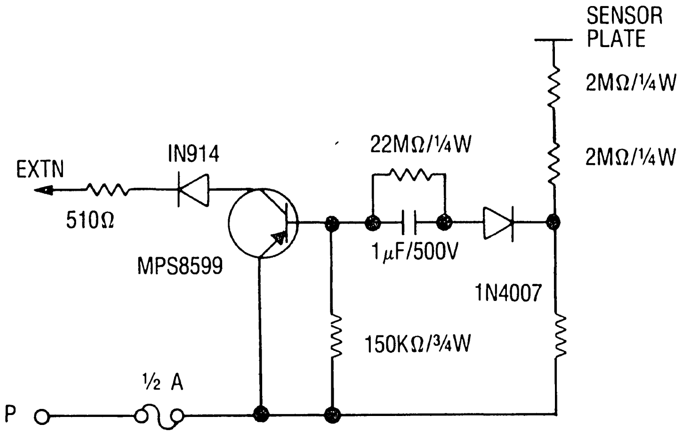


FIGURE 6 — ELECTRONIC EXTENSION

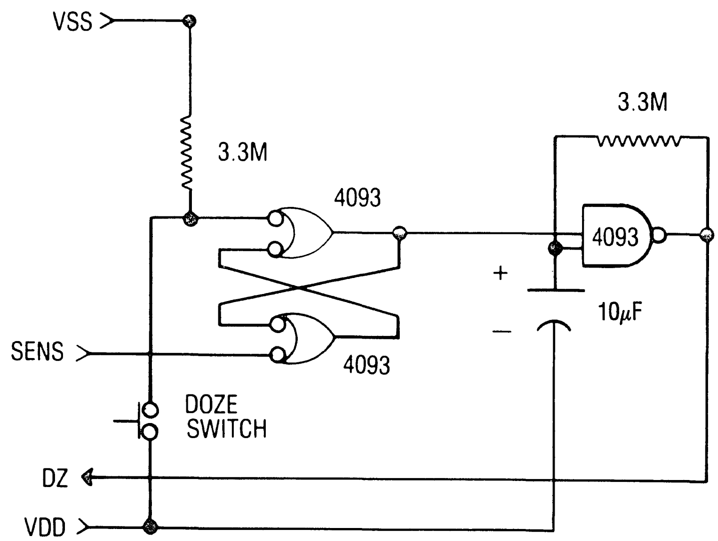


FIGURE 7. DOZE CIRCUIT

EXTENSIONS: (Fig. 6)
All switching and dimming functions can also be implemented by utilizing the slave input. This can be done by either a mechanical switch or the electronic switch in conjunction with a sensing plate as shown in Fig. 6. When the plate is touched, a logical high level is generated at the EXTENSION terminal for both half cycles of the line frequency.

DOZE CIRCUIT: (Fig. 7)
The Doze circuit shown in Fig. 7 generates a slow clock (0.04Hz) at the DZ terminal. If the sensor plate (Fig. 5) is not touched, the SENS terminal of the Doze circuit of Fig. 7 sits at a logical high level. A momentary pressing of the Doze switch sets the SR flip-flop, enabling the oscillator. Every negative transition of the clock (DZ terminal) causes the light intensity to be reduced by equal increments, until eventually the light is shut-off. The oscillator has no further effect on the dimmer circuit. When the light is turned on again by touching the sensor plate, the SR flip-flop is reset and the DZ clock is turned off.

When the Doze circuit is used, the connection between Doze input (Pin 2) and V_{SS} (Pin 1) as shown in Fig. 5, should be removed.

LSI/CSI

LS7237

TOUCH CONTROL STEP DIMMER LIGHT SWITCH AND A.C. MOTOR SPEED CONTROLLER*

FEATURES:

- Phase-locked loop synchronization produces pure AC waveform across output load (no DC offset)
- Provides On/OFF or brightness control of incandescent lamps and ON/OFF control of fluorescent lamps (mode "0" only) without the use of mechanical switches.
- Controls brightness by controlling the AC "duty cycle" hence reducing the power dissipation.
- Provides speed control of AC motors, such as shaded pole and universal series motors
- Controls the "Duty Cycle" from 25% to 88%. (on time angles for AC half cycles between 45° and 159° respectively.)
- Operates on 50Hz/60Hz line frequency.
- Provides control through transformers for low voltage lighting applications.
- Input for extensions or remote sensors.
- 12V to 18V supply voltage.

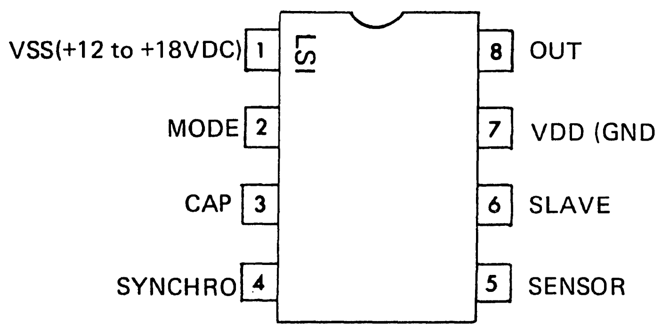
DESCRIPTION:

LS7237 is a monolithic, ion implanted MOS circuit designed for A.C. Power control. The output of the LS7237 triggers a triac (see applications examples) connected in series with either a lamp or an A.C. motor. The lamp brightness or motor speed is determined by controlling the output phase angle (triac triggering angle) in relation to the A.C. line frequency.

The output phase angle can be varied by applying a low level pulse at the SENSOR input or a high level pulse at the SLAVE input. When implemented as shown in the application example, this is accomplished by touching the appropriate sensor plates.

There are five specified levels of power through which the output can be stepped. The power levels (described in terms of lamp brightness, but also applying directly to motor speed) are as follows:

CONNECTION DIAGRAM:



TOP VIEW
Figure 1

* Some motors may require a higher minimum duty cycle (mask option)

LEVEL	BRIGHTNESS (% Rated Wattage)
Off	0
Night Light	9
Mood Light	29
Medium	66
Maximum	99

The circuit may be selected to operate in one of three different modes by tying the MODE input to specific voltage levels (see INPUT/OUTPUT description). The sequences of brightness control in the different modes are as follows:

MODE	BRIGHTNESS SEQUENCE
0	Off - Max - Off
1	Off - Mood - Med - Max - Off
2	Off - Night - Mood - Med - Max - Off

After a power-up, the output comes up in the OFF state. Following that, every time the sensor plate is touched, the output steps to the next level of brightness. The next step following the maximum brightness is the OFF state, initiating a new sequence.

INPUT/OUTPUT DESCRIPTION:

V_{SS} (Pin 1)
Supply voltage positive terminal.

MODE (Pin 2)
The operating mode for the circuit is selected by tying this input as follows:

MODE INPUT	SELECTED MODE
V_{SS}	Mode 0
V_{DD}	Mode 1
Float	Mode 2

CAP (Pin 3)
The CAP input is for external component connection. A capacitor of 0.047 μF $\pm$20% should be used at this input.

SYNCHRO (Pin 4)
The a-c line frequency (50Hz/60Hz), when applied to this input, synchronizes all internal timings with the line frequency through a phase locked loop. The signal for this input may be obtained from the line voltage by employing the circuit arrangement shown in the application examples.

SENSOR (Pin 5)
Low level pulses applied to this input cause the output to step through the successive levels of phase angles (brightness). The output stepping takes place with the trailing edges of the input pulses.

SLAVE (Pin 6)
The SLAVE input is functionally similar to the sensor input with the exception that a positive going pulse is the active signal in this case. It is recommended that the SLAVE input be used instead of the SENSOR input when long extension cables are used between the sensor plate and the dimmer circuit.

V_{DD} (Pin 7)
Supply voltage negative terminal.

OUT (Pin 8)
The output is a low level pulse of fixed duration, occurring every half cycle of the SYNCHRO input signal. The phase angles, ϕ of the output in relation to the synchro signal controls the lamp brightness. The 5 levels of brightness correspond to the phase angle values (ϕ) as follows:

OUTPUT PHASE ANGLE (ϕ)	BRIGHTNESS LEVELS
No output	Off
45°	Night Light
70°	Mood Light
105°	Medium
159°	Maximum

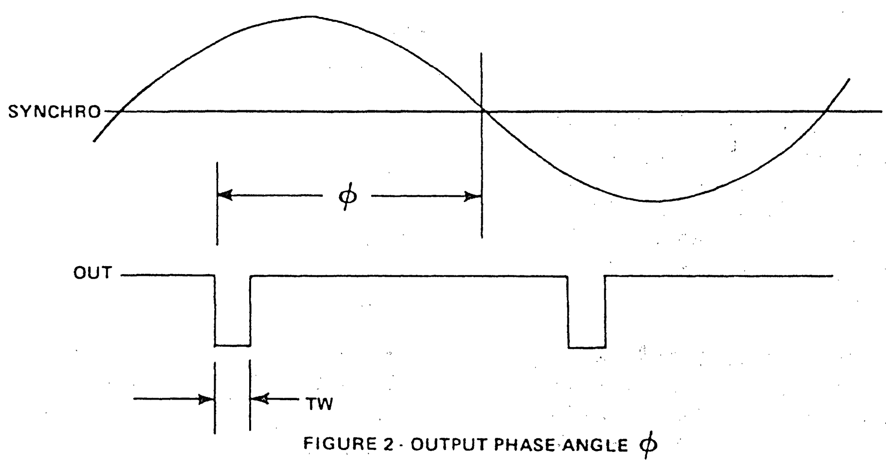


FIGURE 2 · OUTPUT PHASE ANGLE ϕ

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
DC supply voltage	V_{SS}	+20	Volt
Any input voltage	V_{IN}	V_{SS} + .5	Volt
Operating temperature	T_A	0 to +80	°C
Storage temperature	T_{stg}	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 80°C, all voltages referenced to V_{DD})

PARAMETER	SYMBOL	MIN.	TYP	MAX	UNIT	CONDITIONS/ REMARKS
Supply voltage	V_{SS}	+12	—	+18	Volts	
Supply current	I_{SS}		1.0	1.5	mA	@ V_{SS} = +15V, output off
Input voltage						
MODE LO	V_{IZL}	0	—	V_{SS}-9	Volts	
MODE HI	V_{IZH}	V_{SS}-1.5	—	V_{SS}	Volts	
Synchro LO	V_{IRL}	0	—	V_{SS}-9.5	Volts	
Synchro HI	V_{IRH}	V_{SS}-5.5	—	V_{SS}	Volts	
Sensor LO	V_{IOL}	0	—	V_{SS}-8	Volts	
Sensor HI	V_{IOH}	V_{SS}-2	—	V_{SS}	Volts	
Slave LO	V_{IVL}	0	—	V_{SS}-8	Volts	
Slave HI	V_{IVH}	V_{SS}-2	—	V_{SS}	Volts	
Input Current:						
Synchro, Sensor & Slave HI	I_{IH}	—	—	700	uA	V_{input} = V_{SS} = +15V
Synchro, Sensor & Slave LO	I_L	—	—	15	nA	Leakage current
Output HI Vltg		—	V_{SS}	—	Volts	
Output LO Vltg		—	V_{SS}-4	—	Volts	
Output Sink Current	—	25	—	—	mA	@ V_{SS} = +15V V_0 = V_{SS}-3

FREQUENCY CHARACTERISTICS (See Fig. 2 & 3)

All timings are based on f_s = 60Hz, unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Synchro Frequency	f_s	40	—	70	Hz
Sensor Duration	T_{S1}	49	—	Infinite	ms
Output Pulse Width	T_W	40	—	55	μS

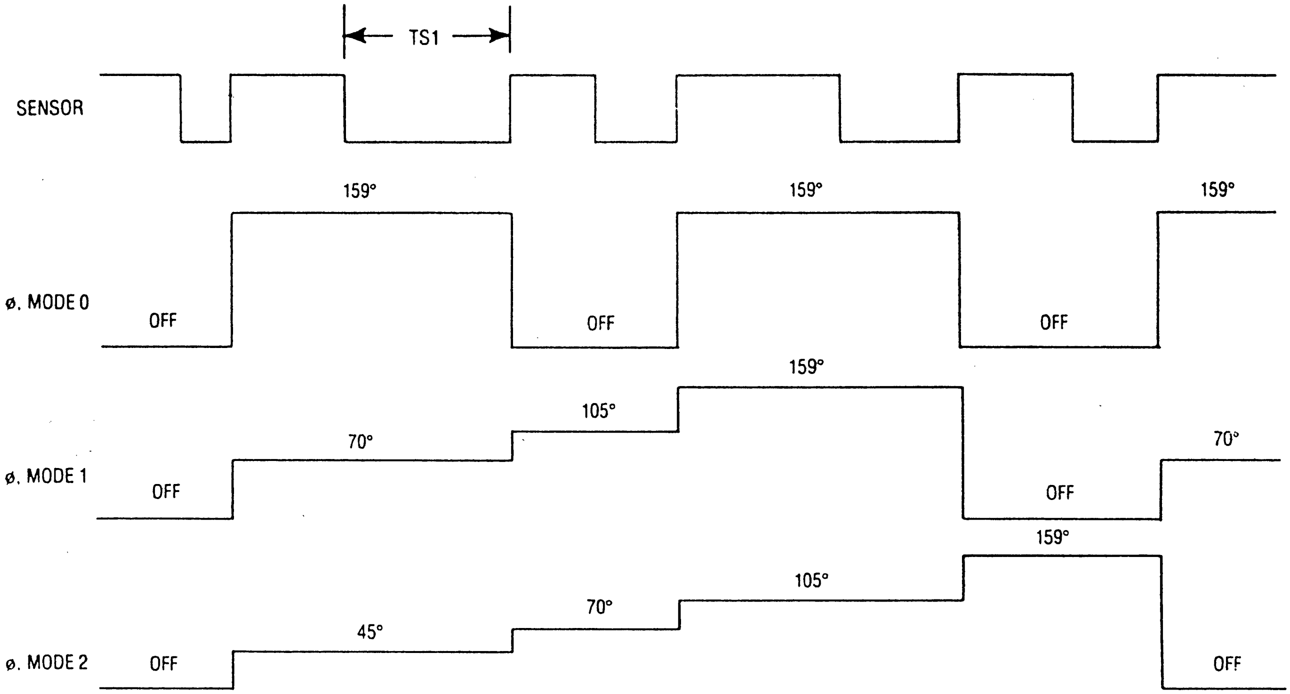


FIGURE 3
SENSOR VS. OUTPUT PHASE ANGLE, ϕ

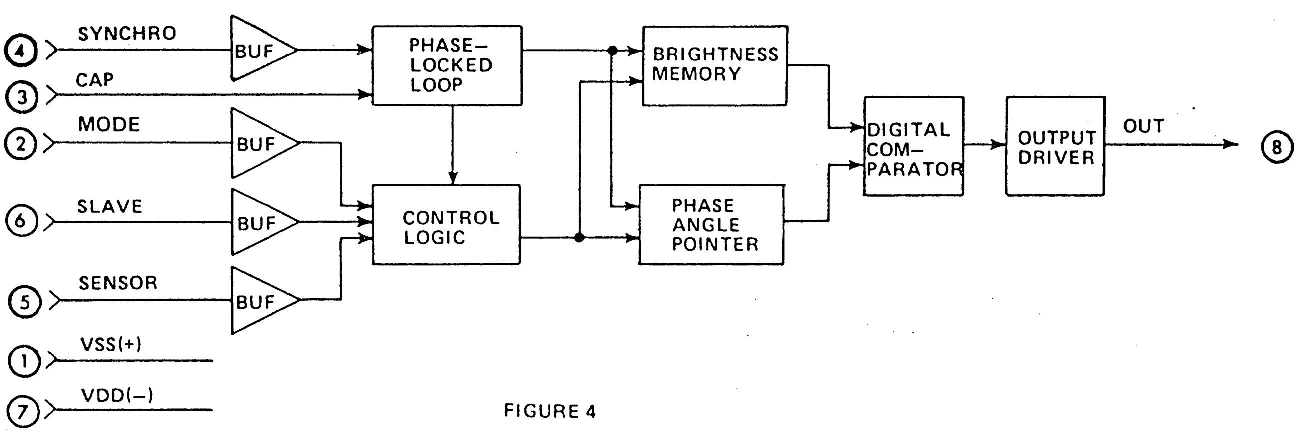


FIGURE 4
BLOCK DIAGRAM

APPLICATION EXAMPLES:

1. A TYPICAL LIGHT DIMMER (FIGURE 5)

A typical implementation of the light dimmer circuit is shown in Fig. 5. Here the brightness of the lamp is set by touching the sensor plate. The functions of different components are as follows:

- The 15V DC supply for the chip is provided by Z, D1, R1, C2 and C5.
- R_2 and C_4 generate the filtered signal for the SYNCHRO input for synchronizing the internal PLL with the line frequency.
- R_3 and C_7 act as a filter for the electronic extension. If extensions are not used, the slave input (Pin 6) should be tied to V_{DD} (Pin 7).
- R_4, R_5, and R_6 set up the sensitivity of the sensor input. C_6 provides noise filtering.
- C_3 is the filter capacitor for the internal PLL.
- D_2 limits the positive excursion of Triac gate to about V_{SS} +.5V. This postive excursion of the gate may occur during the triggered state of certain triacs.
- C_1 and L are RF filter circuits.

In the case of momentary power failure, the circuit state remains unchanged for a period of up to 1 sec. For longer power interruptions, the output is shut off.

115VAC

C1 = 0.15μF/250VAC
C2 = 0.22μF/250VAC
C3 = 0.047μF/25V
C4 = 470pF/600V
C5 = 47μF/25V
C6 = 680pF/50V
C7 = .2μF/25V
R1 = 270 Ω /2W
R2 = 1.5M/¼W
R3 = 680K Ω /¼W

R4 = 1M Ω to 5M Ω (select for sensitivity) /¼W
R5, R6 = 2.7M Ω /¼W
D1, D2 = 1N4148
Z = 15V/1W (Zener)
T = T2500D or Q4004L4 Triac (Typical)
L = 100μH (RFI Filter)

220VAC

C1 = 0.15μF/400VAC
C2 = 0.22μF/400VAC
C3 = 0.047μF/25V
C4 = 470pF/600V
C5 = 47μF/25V
C6 = 680pF/50V
C7 = .2μF/25V
R1 = 1K Ω /1W
R2 = 1.5M Ω
R3 = 680K Ω /¼W

R4 = 1M Ω to 5M Ω /¼W
R5, R6 = 4.7M Ω /¼W
D1, D2 = 1N4148
Z = 15V/1W(Zener)
T = Q5004L4 Triac (Typical)
L = 200μH (RFI Filter)

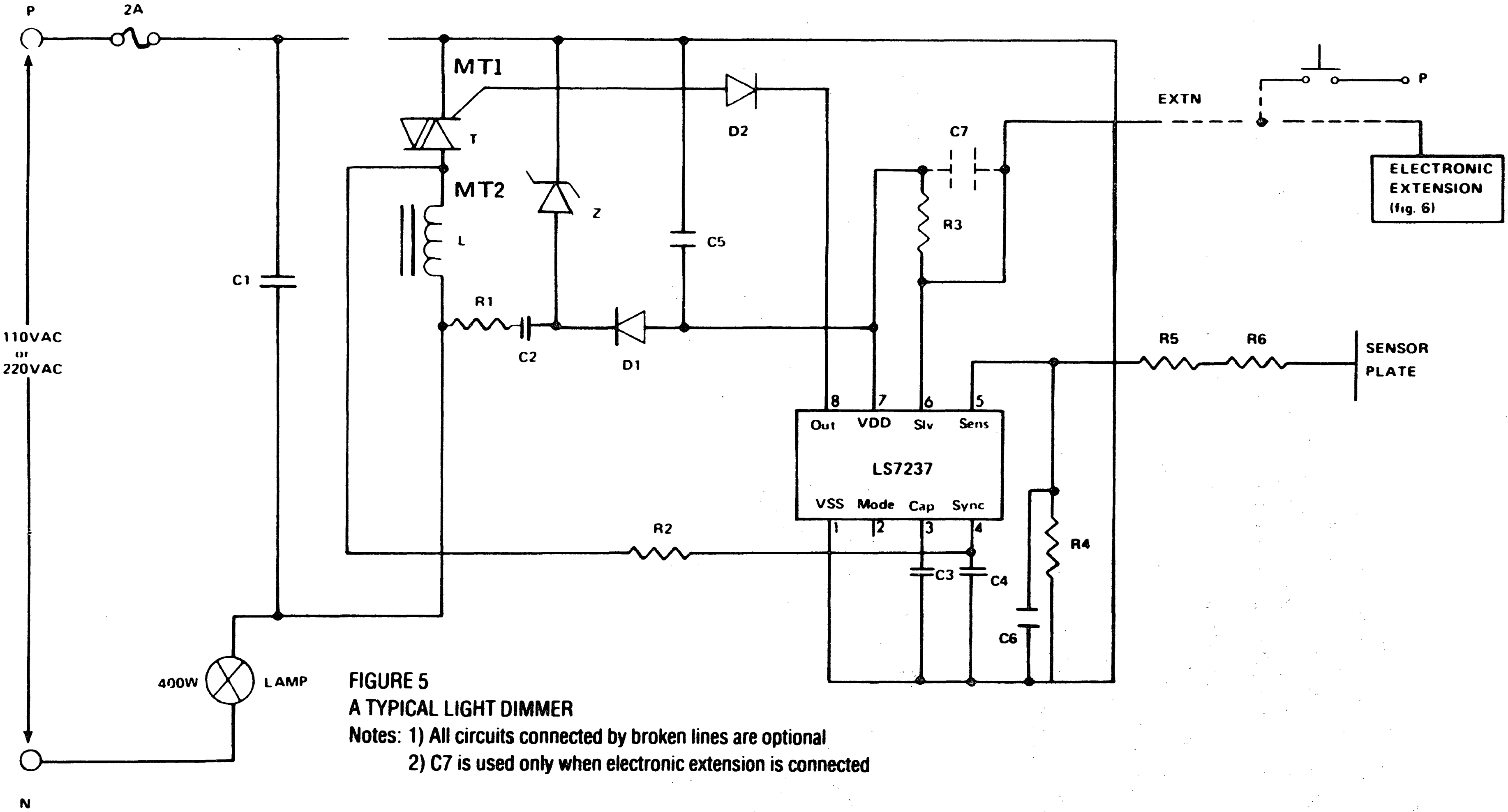


FIGURE 5
A TYPICAL LIGHT DIMMER
Notes: 1) All circuits connected by broken lines are optional
2) C7 is used only when electronic extension is connected

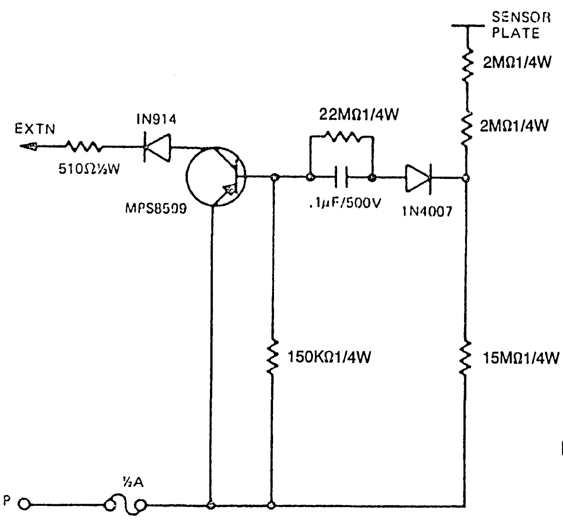
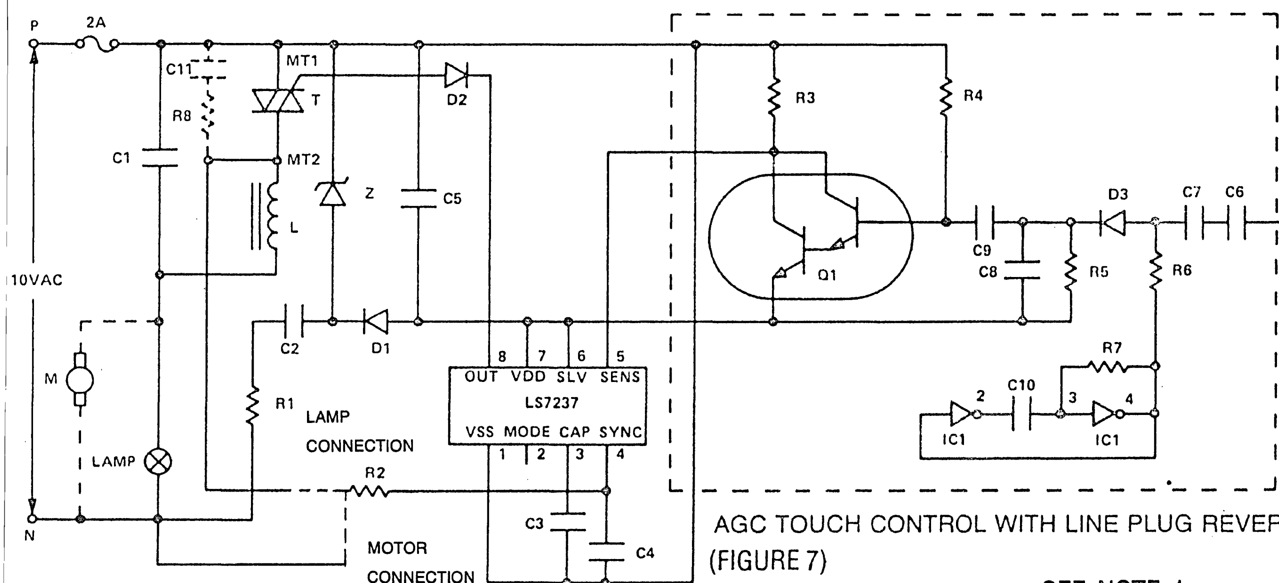


FIG.6 - ELECTRONIC EXTENSION

2. EXTENSIONS (FIGURE 6)

All switching and dimming functions can also be implemented by utilizing the slave input. This can be done by either a mechanical switch or the electronic switch in conjunction with a sensing plate as shown in Fig. 6. When the plate is touched, a logical high level is generated at the EXTENSION terminal for both half cycles of the line frequency.



AGC TOUCH CONTROL WITH LINE PLUG REVERSIBILITY (FIGURE 7)

SEE NOTE 1

C1 = 0.1μF/250V
C2 = 0.5μF/250V
C3 = 0.047μF/16V
C4 = 470pF/600V
C5 = 68μF/25V
C6,C7 = .001μF/1KV
C8 = 0.1μF/50V
C9 = 0.5μF/50V
C10 = 100pF/50V
C11 = 0.047μF/250 V (See Note 2)

R1 = 1KΩ/1W
R2 = 1.5MΩ/1/4W
R3 = 100KΩ/1/4W
R4 = 4.7MΩ/1/4W
R5 = 680KΩ/1/4W
R6 = 10KΩ/1/4W
R7 = 51KΩ/1/4W
R8 = 1.8KΩ//21W (See Note 2)

D1,D2 = 1N4148
D3 = 1N4007
IC1 = CD4069
Z = 15V/1W (ZENER)
Q1 = MPSA13
L = 100μH (RF1 FILTER)
S = SENSOR PLATE
T = Q4004L4 Triac (TYPICAL)

NOTE 1: This circuitry can also be used to achieve reversible plug operation for motor speed control and heating element applications.
NOTE 2: Network R8-C11 is needed for inductive loads (such as motors) only.

3. TOUCH CONTROL WITH AGC (Figure 7) AND LINE PLUG REVERSIBILITY

In applications where a lamp metal body or a motors metal framework is used as the sensor plate, the AGC circuit of Figure 7 may be used to accommodate a wide range of sensor plate sizes. S is the metal body which is also the touch sensor plate.

The CMOS inverter pair (IC 1), along with the RC network R7-C10 forms an oscillator circuit running at a nominal frequency of 100KHz. The oscillation is coupled to the anode of D3 through resistor R6. Since the amplitude of oscillation is of fixed magnitude, the D.C. voltage at the cathode of D3 is at a fixed level. This keeps the darlington pair Q1 on, but close to cutoff level. When S is touched, the amplitude of oscillation at the anode of D3 decreases. This decrease causes the D.C. voltage at the cathode of D3 to drop, which in turn is coupled through C9 to the base of Q1, cutting Q1 off. The collector voltage of Q1 rises to logic 1 level for the LS7237 sense input causing the output to step to the next intensity level. The voltage across C9 adjusts itself automatically as a function of lamp size thereby providing circuit AGC.

SNUBBER NETWORK R8-C11 is only required for inductive loads, such as motors.

LSI/CSI

LS 7331
LS 7332

TOUCH SENSITIVE LIGHT DIMMER AND A.C. MOTOR SPEED CONTROLLER WITH COMPUTER CONTROL AND MONITORING

REVISED JANUARY 1987

FEATURES:

- Provides speed control of A.C. motors and brightness control of incandescent lamps without the use of mechanical switches.
- Controls brightness/motor speed by controlling the a-c "duty cycle" hence reducing the power dissipation
- Controls the "duty cycle" from 23% to 88% (on time angles for a-c half cycles between 41° and 159° respectively.
- Allows computer control of lamp or motor operation.
- Provides outputs to computer indicating when lamp is at full brightness and when it is varying in brightness.
- Has an output that indicates when loss of power has occurred.
- Operates on 50 Hz/60 Hz line frequency.
- Input for extensions or remote sensors.
- Input for slow dimming.
- 12V to 18V DC supply voltage.

DESCRIPTION:

LS 7331 and LS 7332 are monolithic, ion implanted MOS circuits that are specifically designed for the control of brightness of incandescent lamps or speed of AC motors used on the a-c line. The outputs of these chips control the brightness of a lamp or speed of an AC motor by controlling the firing angle of a triac connected in series with the lamp or AC motor. All internal timings are synchronized with the line frequency by means of a built-in phase locked loop circuit. The output occurs once every half cycle of the line frequency. Within the half-cycle, the output can be positioned anywhere between 159° phase angle for maximum brightness/speed and 41° phase angle for minimum brightness/speed in relation to the line frequency. The positioning of the output is controlled by applying a low level at the sensor input or a high level at the slave input. Alternately, the sensor input can be applied via a microprocessor or computer. The DIM and FULL outputs are used to indicate the present state of the lamp or motor to the computer.

These functions may be implemented with very few interface components, which are described in the application examples. When implemented in this manner, a touching of the sensor plate or a control signal from the computer causes the lamp brightness or motor speed to change as follows:

1. If the sensor is touched or a control signal is applied momentarily (32ms to 332ms), the lamp or motor is:

   (a) turned off if it was on,

   (b) turned on if it was off. The brightness/speed to which the light/motor is turned on is either full brightness/speed, or depending on the circuit type, a previous brightness/speed stored in the memory.

CONNECTION DIAGRAM — TOP VIEW
STANDARD 14 PIN PLASTIC DIP

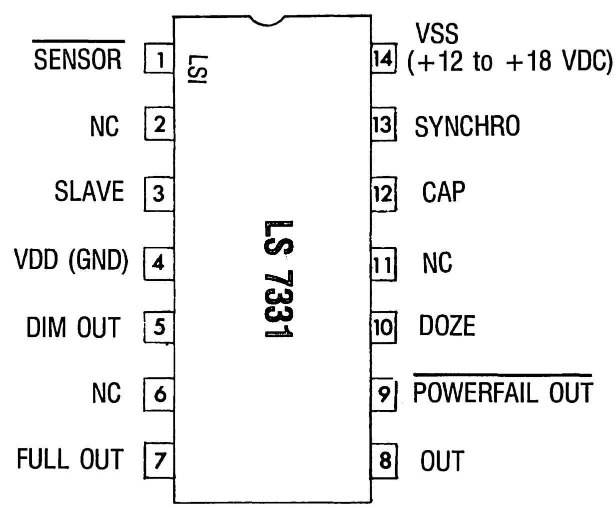


FIGURE 1

2. If the sensor is touched or the control signal is applied for a prolonged time (more than 332ms) the light intensity/speed changes slowly. As long as the touch is maintained, the change continues; the direction of change reverses whenever the maximum or minimum brightness/speed is reached.

   The circuit also provides an input for slow dimming. By applying a slow clock to this input, the lamp can be dimmed slowly until total turn off occurs. This feature can be useful in children's bedroom lights.

INPUT/OUTPUT DESCRIPTION:

VSS (Pin 14).
Supply voltage positive terminal.

$\overline{\text{DOZE}}$ (Pin 10).
A clock applied to this input causes the brightness/speed to decrease in equal increments with each negative transition of the clock. Eventually, when the lamp/motor turns off, this input has no further effect. The lamp/motor can be turned on again by activating either the SENSOR input or the SLAVE input. For the transition from maximum brightness/speed to off, a total of 83 clock pules are needed at the DOZE input.

The functional differences of different variations of the light dimmer circuits are explained in Table I and the output phase angle diagrams in Fig. 3.

TABLE I

TYPE	SENSOR (TOUCH) DURATION				DIMMING DIRECTION REVERSAL
	MOMENTARY (32ms to 332ms) (note 3)		PROLONGED (More than 332ms) (note 3)		
	PRE-TOUCH BRIGHTNESS	POST-TOUCH BRIGHTNESS	PRE-TOUCH BRIGHTNESS	POST-TOUCH BRIGHTNESS	
LS 7331	Off	Max.	Off	Starts varying at Min.	N/A
	Max.	Off	Max.	Starts varying at Max.	N/A
	Intermediate	Off	Intermediate	Starts varying at Pre-Touch brightness	NO
LS 7332	Off	Memory (See note 1)	Off	Starts varying at Memory (Note 2)	YES
	Max.	Off	Max.	Starts varying at Max.	N/A
	Intermediate	Off	Intermediate	Starts varying at Pre-Touch brightness	YES

NOTE 1. "Memory" refers to the brightness stored in the memory. The brightness is stored in the memory when the light is turned off by momentary sensor touch. First time after power-up, momentary touch produces max. brightness.

NOTE 2. First time after power-up, prolonged touch causes intensity to vary starting at min.

NOTE 3. The time figure is based on 60Hz synchro frequency. For 50Hz the figures are 39ms and 399 ms.

When either the $\overline{\text{SENSOR}}$ or the SLAVE input is active, the $\overline{\text{DOZE}}$ input is disabled.

CAP (Pin 12).
The CAP input is for external component connection. A capacitor of $.047\mu F \pm 20\%$ should be used at this input.

SYNCHRO (Pin 13).
The a-c line frequency (50Hz/60Hz), when applied to this input, synchronizes all internal timings through a phase locked loop. The signal for this input may be obtained from the line voltage by employing the circuit arrangement shown in the application notes.

$\overline{\text{SENSOR}}$ (Pin 1).
A low level applied to the SENSOR input controls the turn on or turn off of the output as well as its phase angle with respect to the SYNCHRO input. A description of this is provided in the general description and Table 1.

SLAVE (Pin 3).
The SLAVE input is functionally similar to the SENSOR input with the exception that the active level is a logical high as compared to the logical low level for the SENSOR input. It is recommended that the SLAVE input be used instead of the SENSOR input when long extension wires are used between the sensing plates (or switches) and the dimmer chips.

VDD (Pin 4).
Supply voltage negative terminal.

$\overline{\text{OUT}}$ (Pin 8).
The output is a low level pulse occurring once every half cycle of the SYNCHRO signal. The phase angle, Ø of the output in relation to the SYNCHRO signal controls the lamp brightness/motor speed.

In continuous dimming operation (i.e., when the SENSOR input is continuously held low) the output phase angle, Ø sweeps up and down between 41° and 159° continuously. The time vs Ø curve, however, is not a linear one (see Fig. 3). Between two maxima on this curve, there are 4 discontinuous points labeled A_1, B_1, B_2, A_2. The discontinuities are as follows:

1. From maximum to A_1. In this region, Ø is changed by equal increments (ΔØ) for every 2 SYNCHRO clocks.
2. From A_1 to B_1. In this region, the increments (ΔØ) take place for every 4 SYNCHRO clocks.
3. From B_1 to B_2. In this region Ø is held at a constant level (ΔØ = 0).
4. From B_2 to A_2. Same as 2.

From A_2 to Maximum. Same as 1.

The slower rate of change in Ø over $A_1B_1B_2A_2$ region is to accommodate for eye adjustment at lower light/speed intensity.

DIM OUT (Pin 5).
This CMOS compatible output is high whenever the circuit is in the continuous dimming mode of operation. When the lamp/motor is off or at full brightness/speed, this output is low.

FULL OUT (Pin 7).
This CMOS compatible output is high when the lamp/motor is a full brightness/speed. If the lamp is off or in the continuous dimming mode, this output is low.

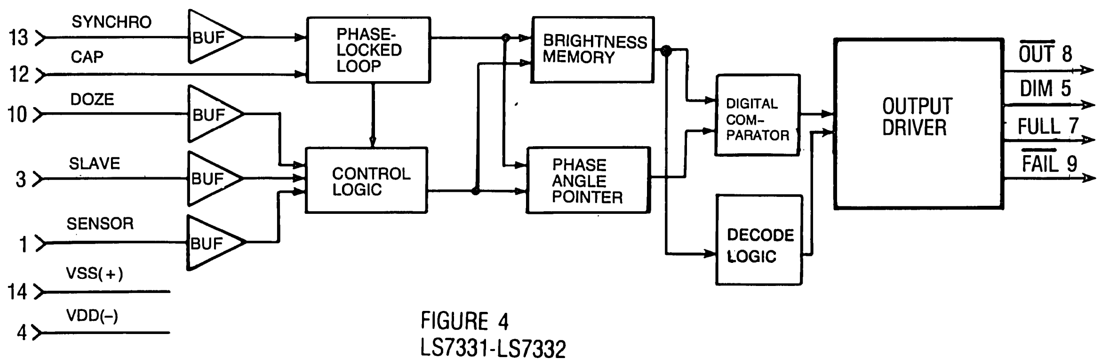


FIGURE 4
LS7331-LS7332
BLOCK DIAGRAM

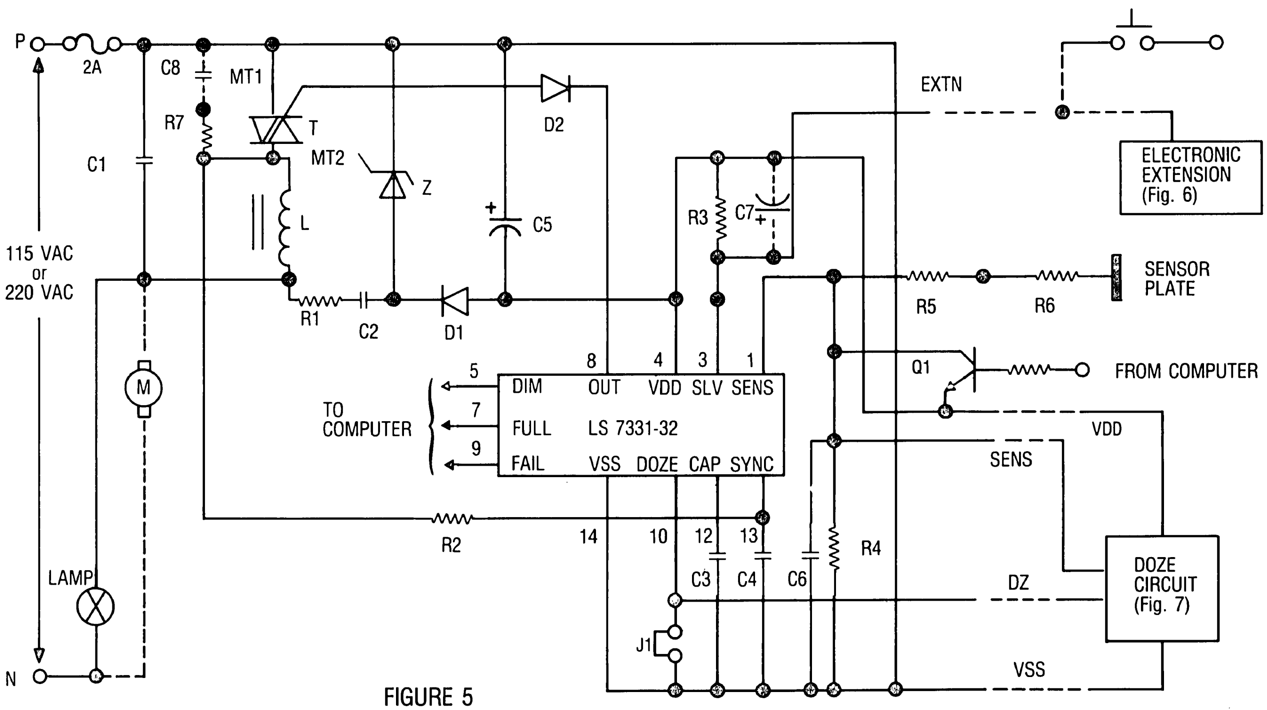


FIGURE 5
A TYPICAL LIGHT DIMMER/MOTOR SPEED CONTROL
Notes: 1) All circuits connected by broken lines are optional
2) C7 is used only when electronic extension is connected
3) Jumper between Pin 10 & VSS should be broken when Doze circuit is used.
4) Network C8-R7 is needed for inductive loads (such as motors) only.

115 VAC

C1 = 0.15μF/250VAC
C2 = 0.22μF/250VAC
C3 = 0.47μF/16V
C4 = 470pF/600V
C5 = 47μF/25V
C6 = 680pF/50V
C7 = 0.2μF/25V
C8 = 0.047μF/250V (see note #4)
R1 = 270Ω/2W
R2 = 1.5MΩ/¼W
R3 = 680KΩ/¼W
R4 = 1MΩ to 5MΩ/¼W (select for sensitivity)
R5, R6 = 2.7MΩ/¼W
R7 = 1.8KΩ/2W (see note -4)
Q1 = 2N2222 or equivalent
D1, D2 = 1N4148
Z = 15V/1W (Zener)
T = T2500 (Triac)
L = 100μH (RFI Filter)

220 VAC

C1 = 0.15μF/250VAC
C2 = 0.22μF/250VAC
C3 = 0.47μF/16V
C4 = 470pF/600V
C5 = 47μF/25V
C6 = 680pF/50V
C7 = 0.2μF/25V
C8 = 0.047μF/250V (see note #4)
R1 = 270Ω/2W
R2 = 1.5MΩ/¼W
R3 = 680KΩ/¼W
R4 = 10KΩ¼W
R4 = 1MΩ to 5MΩ/¼W (select for sensitivity)
R5, R6 = 4.7MΩ/¼W
R7 = 1.8KΩ/2W (see note #4)
Q1 = 2N2222 or equivalent
D1, D2 = 1N4148
Z = 15V/1W (Zener)
T = T2500 (TRIAC)
L = 200μH (RFI Filter)

FREQUENCY CHARACTERISTICS (See Fig. 2 & 3)

All timings are based on $f_S = 60Hz$, unless otherwise specified.

PARAMETER	SYMBOL	MIN	TYP.	MAX.	UNIT
Synchro Frequency	f_S	40	—	70	Hz
Sensor Duration (ON/OFF Oper.)	T_{S1}	32	—	332	ms
Sensor Duration (Dimming Oper.)	T_{S2}	332	—	infinite	ms
Doze Frequency	—	—	—	500	Hz
Output Pulse Width	TW	40	—	55	µS
Output Phase-Angle (Note 1)	0	41	—	159	degrees
ϕ Period (Max to Max in continuous dimming)	—	—	7.28	—	sec.
$A_1B_1 = B_2A_2$. duration	—	—	934	—	ms
B_1B_2. Min. intensity dwell	—	—	500	—	ms

Note 1. In the circuit arrangement described in the application notes, the synchro input signal is delayed in phase in relation to the line frequency by about 6°, resulting in a ϕ range between 35° and 152°. With higher R-C value the phase angle range may be shifted down further.

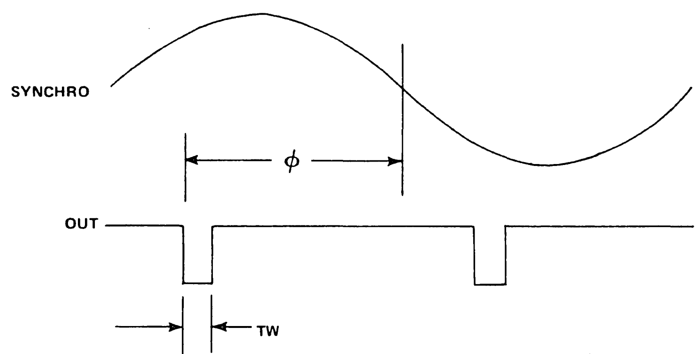


FIGURE 2 OUTPUT PHASE ANGLE ϕ

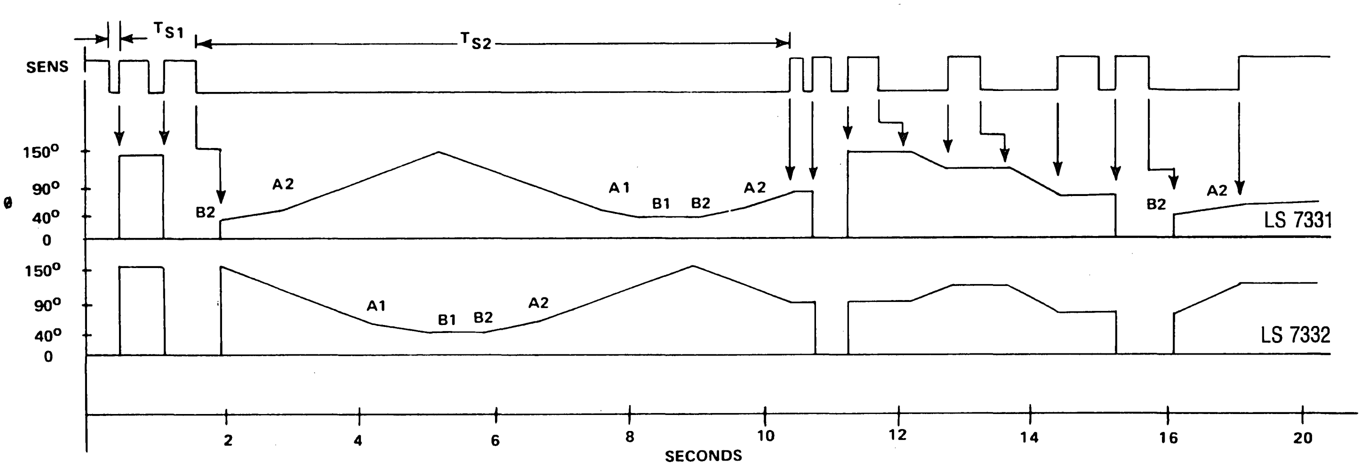


FIGURE 3
OUTPUT PHASE ANGLE, ø Vs, SENSOR OUTPUT

POWER FAIL OUT (Pin 9).

If the SYNCHRO input does not occur for two successvie cycles, then a loss of power is assumed to have occurred and this output becomes low. This output will become positive again one cycle after power is restored. This output is CMOS compatible.

APPLICATION EXAMPLES:

A typical implementation of the light dimmer/motor speed control circuit is shown in Fig. 5. Here the brightness of the lamp/speed of the motor is set by touching the sensor plate or by applying a control signal to 0_1 from the computer. The functions of different components are as follows:

- The 15V DC supply for the chip is provided by Z, D1, R1, C2 and C5.
- R_2 and C_4 generate the filtered signal for the SYNCHRO input for synchronizing the internal PLL with the line frequency.
- R_3 and R_4 are current limiting resistors in the event the extension circuit is incorrectly polarized. If extensions are not used, the slave input (Pin 3) should be tied to V_{DD} (Pin 7).
- R_5 sets up the sensitivity of the sensor input.
- C_3 is the filter capacitor for the internal PLL.
- D_2 limits the positive excursion if Triac gate to about V_{SS} +.5V. This positive excursion of the gate may occur during the triggered state of certain triacs.
- C_1 and L are RF filter circuits.

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
DC supply voltage	VSS	+20	Volt
Any pinput voltage	V_{IN}	VSS + .5	Volt
Operating Temperature	T_A	0 to + 80	°C
Storage Temperature	Tstg	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS:

(T_A =0 to 80°C, all voltages referenced to VDD)

PARAMETER	SYMBOL	MIN.	TYP	MAX	UNIT	CONDITIONS/ REMARKS
Supply voltage	V_{SS}	+12	—	+18	Volts	
Input Voltage						
Doze LO	V_{IZL}	0	—	V_{SS}-6	Volts	@ V_{SS} = +15V,
Doze HI	V_{IZH}	VSS-2	—	V_{SS}	Volts	output off
Synchro LO	V_{IRL}	0	—	V_{SS}-9.5	Volts	
Synchro HI	V_{IRH}	V_{SS}-5.5	—	V_{SS}	Volts	
Sensor LO	V_{IOL}	0	—	V_{SS}-8	Volts	
Sensor HI	V_{IOH}	V_{SS}-2	—	V_{SS}	Volts	
Slave LO	V_{IVL}	0	—	V_{SS}-8	Volts	
Slave HI	V_{IVH}	V_{SS}-2	—	V_{SS}	Volts	
Slave Current:						
Synchro, Sensor & Slave HI	I_{IH}	—	—	700	μA	V_{input}=V_{SS} =+15V
Synchro, Sensor & Slave LO	I_L	—	—	15	nA	Leakage current
Doze HI	—	—	—	5	nA	
Doze LO	—	—	—	5	nA	
Output HI Vltg		—	V_{SS}	—	Volts	
Output LO Vltg		—	V_{SS}-4	—	Volts	
Output Sink Current	—	25	—	—	mA	@V_{SS}=+15V V_0 = V_{SS}-3
Dim, Full	V_{OL}	—	—	0.5	Volts	
& Power Fail	V_{OH}	VSS-1	—	Volts		

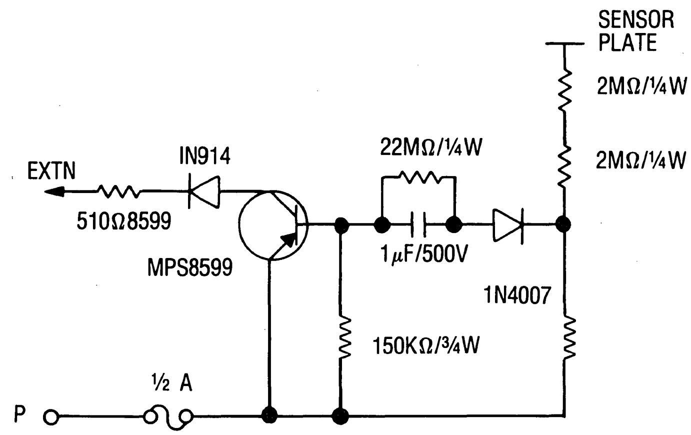


FIGURE 6 — ELECTRONIC EXTENSION

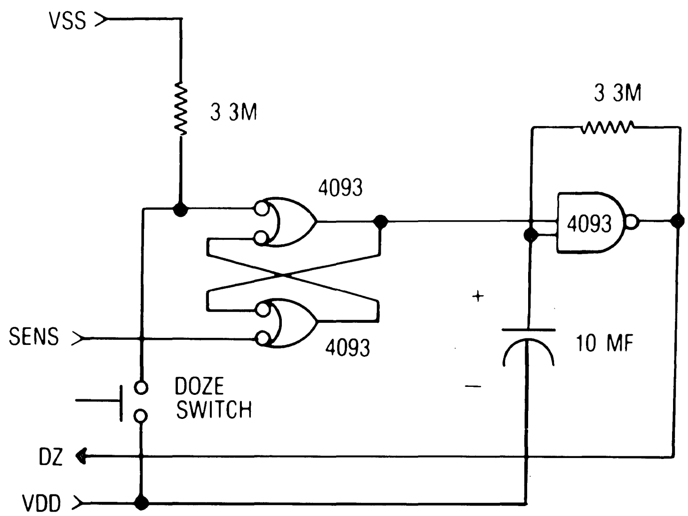


FIGURE 7 DOZE CIRCUIT

In the case of momentary power failure, the circuit state remains unchanged for a period of up to 1 sec. For longer power interruptions, the output is shut off.

EXTENSIONS: (Fig. 6).
All switching and dimming functions can also be implemented by utilizing the slave input. This can be done by either a mechanical switch or the electronic switch in conjunction with a sensing plate as shown in Fig. 6. When the plate is touched, a logical high level is generated at the EXTENSION terminal for both half cycles of the line frequency.

DOZE CIRCUIT: (Fig. 7).
The Doze circuit shown in Fig. 7 generates a slow clock (0.04Hz) at the DZ terminal. If the sensor plate (Fig. 5) is not touched, the SENS terminal of the Doze circuit of Fig. 7 sits at a logical high level. A momentary pressing of the Doze switch sets the SR flip-flop, enabling the oscillator. Every negative transition of the clock (DZ terminal) causes the light intensity to be reduced by equal increments, until eventually the light is shut off. The oscillator has no further effect on the dimmer circuit. When the light/motor is turned on again by touching the sensor plate, the SR flip-flop is reset and the DZ clock is turned off.

When the Doze circuit is used, the connection between Doze input (Pin 10) and V_{SS} (Pin 14) as shown in Fig. 5, should be removed.

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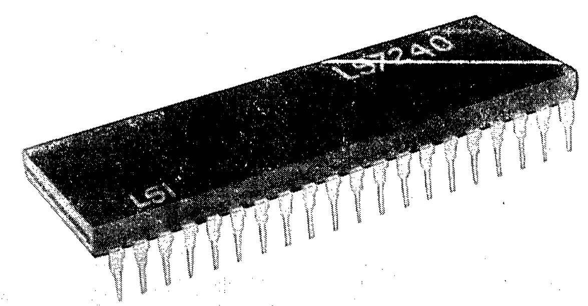
LS7240 | 6 DECADE, 7 LEVEL COMPARATOR WITH MEMORY

Revised January 1986



ΞATURES:

- Direct Interface with CMOS CD4510 Presettable Up/Down Counter
- Direct Interface with LS7040 Dual 3 Decade Counter Multiplexed BCD/HEX Data I/O
- DC to 60KHz Scan Frequency at 5V
- Cascadable
- 7 Levels of 24 Bit Comparators
- Thumbwheel Switch Interface for 7 Level Storage Data
- CMOS Type Noise Immunity
- Single Power Supply Operation +4.75 to +15 Volts
- CMOS Compatibility
- Power-On-Reset
- All Inputs Protected
- High Input Impedance
- Low Power Dissipation

ESCRIPTION:

he LS7240 is a monolithic, ion implanted MOS 7-Level digit (BCD or HEX) memory/comparator. It includes seven decade comparators and memory, a comparator output, 4 bit data I/O Bus, 7 synchronizing strobes for thumbheel and display drive and 24 parallel data input lines. Data ritten in each of the 7 levels of memory is compared with ıe data placed in the 24 bit parallel inputs and the result is ıdicated by the Multiplexed comparator output. The 4 bit O serves as either the inputs for writing into any of the 7 ıemories or outputs for displaying either the 24 bit parallel ata or any one of the memories.

ESCRIPTION OF OPERATION:

CAN OSCILLATOR AND DIGIT SELECT STROBES:

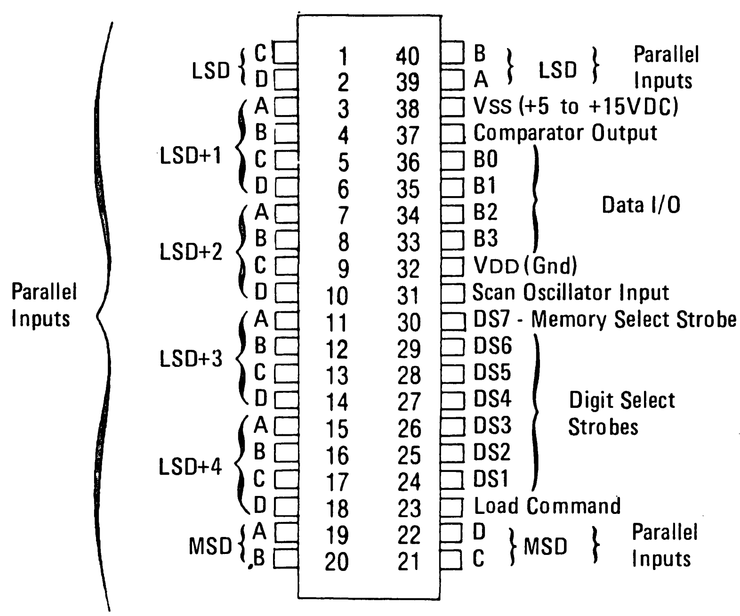
he SELECT STROBE GENERATOR is driven by an ıternal oscillator whose frequency is determined by an ex- ɜrnal RC network (as shown in Fig. 4). Table I indicates ɜveral frequencies and their associated resistor-capacitor etworks.

he SELECT STROBES scan from DS1 to DS7. DS7 selects ıe particular comparator memory to be selected and DS1 ırough DS6 selects the LSD to MSD digit to be loaded. laximum scan frequency is 60KHz at 5V, 40KHz at 10V and 0KHz at 15V. All I/O timings are synchronized by the DS trobes as explained in each I/O section.

ARALLEL INPUT DATA AND COMPARATOR OUTPUT:

CD data applied from the counter to the 24 bit parallel ıputs is compared with the 7-level memory. All 24 bits of ach memory are compared in parallel and 7 internal comıarisons are performed. These comparisons result in a logical 1" if the memory level and input data are equal or a logical 0" if not equal. The internal comparisons are multiplexed vith the strobe outputs, i.e. MEMORY 1 is muxed with DS1,

LS7240 CONNECTION DIAGRAM:



TOP VIEW

FIGURE 1

MEMORY 2 is muxed with DS2, etc. (See Figure 4). A single output comparator line is demuxed externally. The positive edges of the DIGIT STROBES are used to strobe the comparator output line into their respective latches as shown in figures 2 and 5. The positive edge of DS1 is used to demux comparator 1 from the common comparator output, positive edge of DS2 demuxes comparator 2 etc.

The data provided by the counter is BCD data. However, HEX data, binary data or any other format of data may also be used as inputs. All that would be required is that the internal memory is correspondingly loaded.

DATA I/O AND LOAD COMMAND

The 4 bit data I/O acts as inputs when the DS strobes are active (high) and as outputs in between strobes. The in between strobe time is typically 5 μs. In the input mode, the data applied selects the memory to be addressed as well as the 6 digit number to be loaded. Figure 5 indicates how a set of 7 thumbwheel switches is used to load the memory. The LS7240 has internal pull down resistors on its I/O lines. Data applied during DS7 serves as the memory address, while data applied during the succeeding DS1 through DS6 loads LSD through MSD respectively into the selected memory. Data is loaded into the memory at the trailing edges of the DS strobes. In between strobes, when the I/O bus is in the output mode, the selected 6 digit memory is multiplexed out. The MSD is applied to the output during the DS1 and DS2 inter-strobe delay. The LSD+4 output occurs between DS2 and DS3, LSD+3 between DS3 and DS4, LSD+2 between DS4 and DS5, LSD+1 between DS5 and DS6, and LSD between DS6 and DS7.

The load command output can be used as a strobe for storing the output data into external latches for display or control functions.

A number of LOAD/DISPLAY combinations for data I/O is possible as explained in Table II. The data in this truth table refers to the input data applied to the I/O bus during active DS7.

The display is shown in figure 5. The LOAD COMMAND is used to load the BCD DATA into a CD4511 or equivalent. The DIGIT SELECT STROBES are used to enable the LED's as shown. DS2 is used to display the MSD, DS3 displays LSD+4, DS4 displays LSD+3, DS5 displays LSD+2, DS6 displays LSD+1 and DS7 displays LSD.

The LS7240 is equipped with an ANTI-BOUNCE feature. Input data must be stable at the input to the I/O bus for a minimum of 700 scan cycles before it can be loaded into the memory. Typical Anti-Bounce times as a function of scan frequency is indicated in Table III. Similarly, removal of data must be stable for 700 clock cycles before it is recognized as a complete removal.

POWER-ON-RESET:

An internal POWER-ON-RESET is provided to reset all memories to "0" and sets DS7 (Pin 30) to logic "1" upon application of power.

POWER SUPPLIES:

The circuit will operate over the range of +4.75 to +15 volts.

TABLE I

Voltage	Resistor	Capacitor	Typical Frequency
	220KΩ	50pf	60KHz
5V	680KΩ	50pf	30KHz
	1.5MΩ	50pf	15KHz
	470KΩ	50pf	40KHz
10V	1MΩ	50pf	20KHz
	2MΩ	50pf	10KHz
	1MΩ	50pf	20KHz
15V	2MΩ	50pf	10KHz
	4.7MΩ	50pf	5KHz

TABLE II

Truth Table for Load/Display Combination

B3	B2	B1	B0	
0	0	0	1	Display Memory 1
0	0	1	0	Display Memory 2
0	0	1	1	Display Memory 3
0	1	0	0	Display Memory 4
0	1	0	1	Display Memory 5
0	1	1	0	Display Memory 6
0	1	1	1	Display Memory 7
1	0	0	1	Load & Display Memory 1
1	0	1	0	Load & Display Memory 2
1	0	1	1	Load & Dispaly Memory 3
1	1	0	0	Load & Display Memory 4
1	1	0	1	Load & Display Memory 5
1	1	1	0	Load & Display Memory 6
1	1	1	1	Load & Display Memory 7
0	0	0	0	Displays 24 Bit Input Data
1	0	0	0	Resets All Memories and Displays Memory 1.

TABLE III

Scan Frequency (KHz)	Anti-Bounce (milliseconds)
60	12
40	17.5
20	35

TECHNICAL DATA:

INPUTS/OUTPUTS – All inputs and outputs are CMOS compatible over entire range of power supply voltage limits.

LOGIC – Positive True.

PACKAGE – 40 Pin Dual-In-Line plastic.

MAXIMU
Parameter
DC Supply
Operating T
Storage Ten
All inputs
charges. Ca
outside the

DC ELEC
(V_{DD}=0V,

OUTPUT S

SOURCE C

$V_{OH}=V_{SS}-$

$V_{OH}=V_{SS}-$

$V_{OH}=V_{SS}-$

SINK CUR

$V_{OL}=V_{DD}$

SOURCE C

$V_{OH}=V_{SS}-$

$V_{OH}=V_{SS}-1$

$V_{OH}=V_{SS}-$

SINK CURR

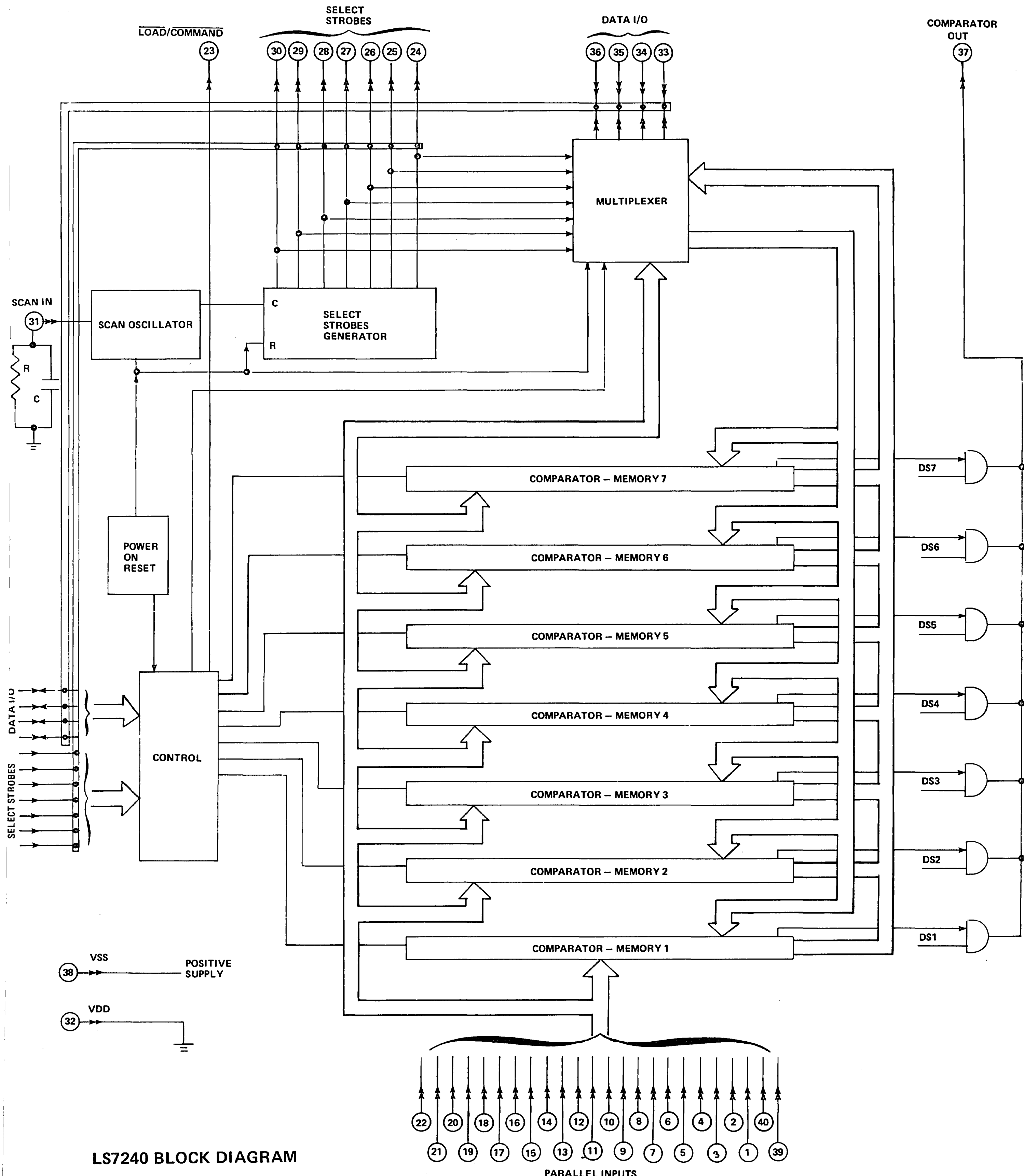
$V_{OL}=V_{DD}+$

BCD I/O
SOURCE CU
$V_{OH}=V_{SS}-$

$V_{OH}=V_{SS}-1$

$V_{OH}=V_{SS}-$

FIGURE A



LS7240 BLOCK DIAGRAM

FIGURE 4

BLOCK DIAGRAM OF PROGRAMMABLE COUNTER CONTROLLER

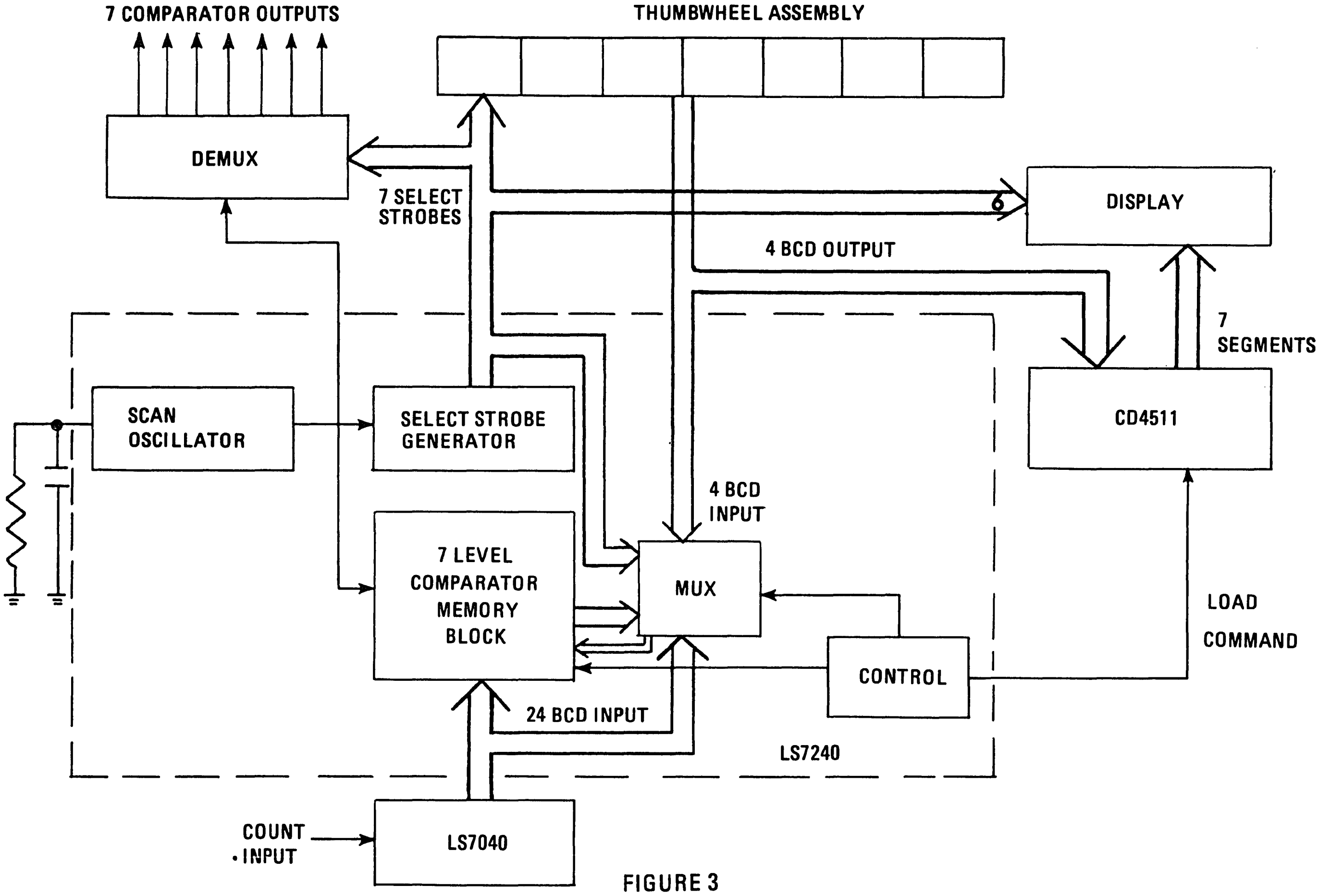
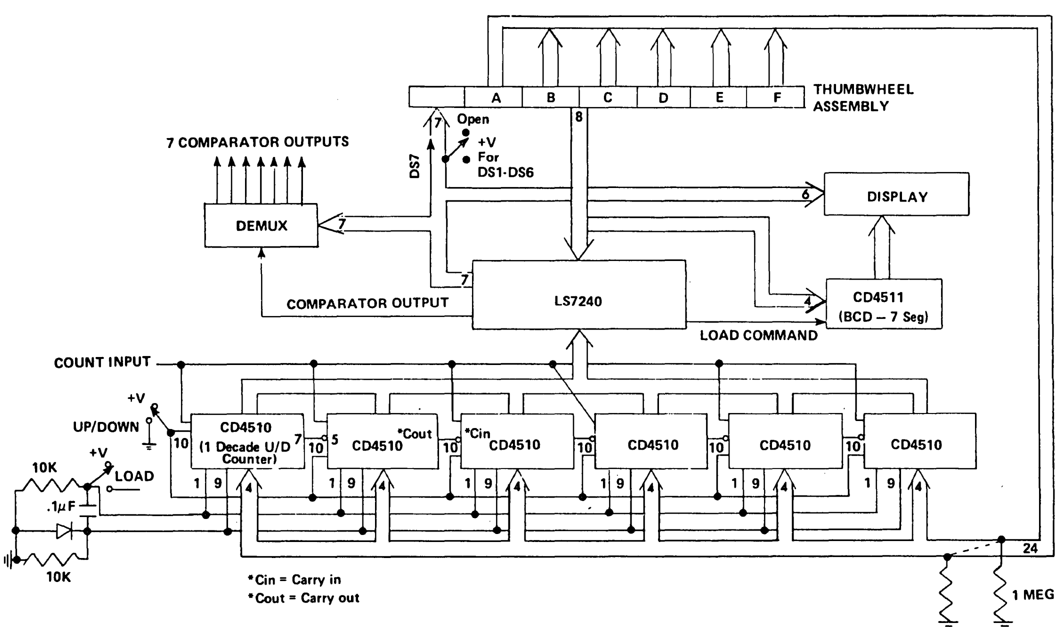


FIGURE 3

SYSTEM INTERCONNECTION USING PRESETTABLE UP/DOWN COUNTERS



The thumbwheel assembly is used to load the LS7240 as well as the synchronous six decade up/down counter. To preset the CD4510's, the inputs to the thumbwheels A.through F are connected to the positive supply and the BCD outputs are applied to their respective CD4510 inputs. External 1 Meg resistors are used at the thumbwheel outputs. The Load Command is used to reset and then preset the counter to the number selected.

FIGURE 5

oltages referenced to V_{DD})

Symbol	Value	Units
V_{SS}	+4.75 to +15	Vdc
T_A	−25 to +70	^oC
T_S, T_G	−65 to +150	^oC

ı circuitry to prevent damage due to high static
ısed to prevent unnecessary application of Voltage

\CTERISTICS:

ıV, $-25^oC \leq T_A \leq +70^oC$ unless otherwise specified).

ıIT SELECT STROBES

V_{SS}	Min.	Typ.	Max.	Units
5Vdc	0.4	1.0	–	mA
10Vdc	1.0	1.6	–	
15Vdc	1.2	2.0	–	
5Vdc	1.4	2.0	–	mA
10Vdc	2.7	4.0	–	
15Vdc	3.5	5.0	–	
5Vdc	2.3	3.0	–	mA
10Vdc	6.0	9.0	–	
15Vdc	7.4	9.6	–	
5Vdc	16.0	27.0	–	μA
10Vdc	13.0	19.0	–	
15Vdc	9.0	15.0	–	

ID AND COMPARATOR OUTPUT

V_{SS}	Min	Typ.	Max.	Units
5Vdc	0.1	0.3	–	mA
10Vdc	0.3	0.6	–	
15Vdc	0.5	1.0	–	
5Vdc	0.2	0.4	–	mA
10Vdc	1.0	1.5	–	
15Vdc	1.5	2.5	–	
5Vdc	0.5	0.9	–	mA
10Vdc	2.2	3.2	–	
15Vdc	3.4	5.0	–	
5Vdc	19.0	30.0	–	μA
10Vdc	16.0	23.0	–	
15Vdc	13.0	17.0		

V_{SS}	Min.	Typ.	Max.	Units
5Vdc	0.1	0.3	–	mA
10Vdc	0.3	0.6	–	
15Vdc	0.5	1.0	–	
5Vdc	0.5	0.9	–	mA
10Vdc	1.0	1.5	–	
15Vdc	1.5	2.5	–	
5Vdc	0.5	0.9	–	mA
10Vdc	2.2	3.2	–	
15Vdc	3.0	5.0	–	

SINK CURRENT, I_{OL}	V_{SS}	Min.	Typ.	Max.	Units
	5Vdc	7.0	10.0	–	μA
$V_{OL}=V_{DD}+.4V$	10Vdc	5.0	7.0	–	
	15Vdc	3.0	5.0	–	

QUIESCENT SUPPLY CURRENT

(All Inputs Pins Tied to V_{SS}) (All Output Pins Left Open)

Symbol	V_{SS}	Max.	Units
I_{DD}	5V	12.0	mA
	10V	15.0	
	15V	18.0	

INPUT VOLTAGE SPECIFICATIONS: (All Inputs Except Scan)

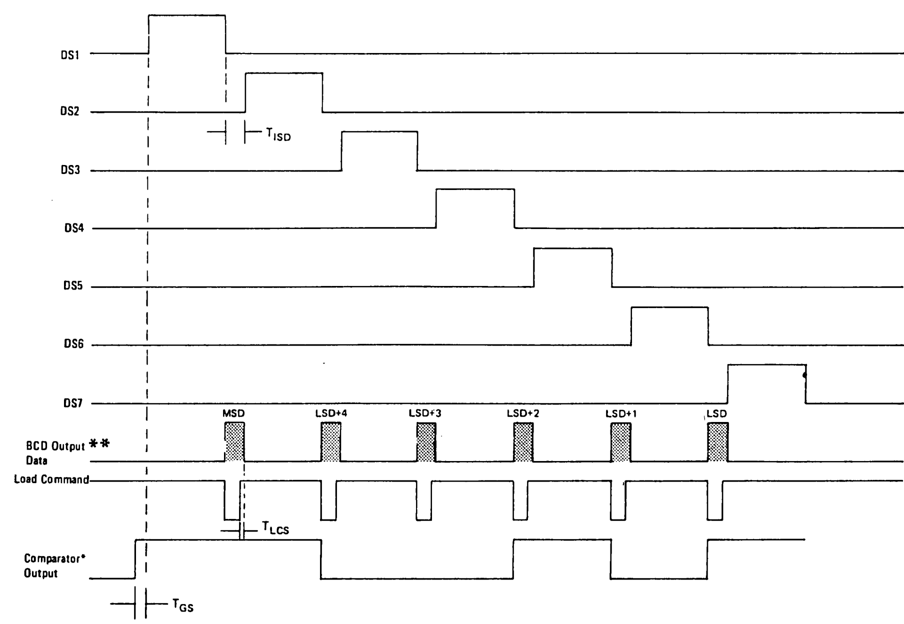
Parameter	Symbol	V_{SS}	Min.	Max.	Units
Input Voltage "0" Level	V_{IL}	5Vdc	0	1.5	Vdc
		10Vdc	0	3.0	
		15Vdc	0	4.5	
Input Voltage "1" Level	V_{IH}	5Vdc	3.5	V_{SS}	Vdc
		10Vdc	7.0	V_{SS}	
		15Vdc	10.5	V_{SS}	

DYNAMIC ELECTRICAL CHARACTERISTICS:

(V_{DD}=0, V_{SS}= +4.75 to +15V, $-25^oC \leq T_A \leq +70^oC$ unless otherwise specified).

Parameter	Symbol	Min.	Max.	Units
Scan Input Frequency				
V_{SS}=5V	f_{SC}	–	60.0	KHz
V_{SS}=10V	f_{SC}	–	40.0	KHz
V_{SS}=15V	f_{SC}	–	20.0	KHz
Inter-strobe delay	t_{ISD} †	1.5	12.0	μs
Load Command Set-Up Time	t_{LCS} †	0.2	2.5	μs
Comparator Output Set-Up Time	t_{CS} †	1.5	10.0	μs

†See Figure 2.



* 4 Comparisons are shown. In normal operation, usually only 1 comparison will occur at a time.

**Shaded areas indicate valid output data.

FIGURE 2

INTERCONNECT DIAGRAM OF TYPICAL COUNTER CONTROLLER

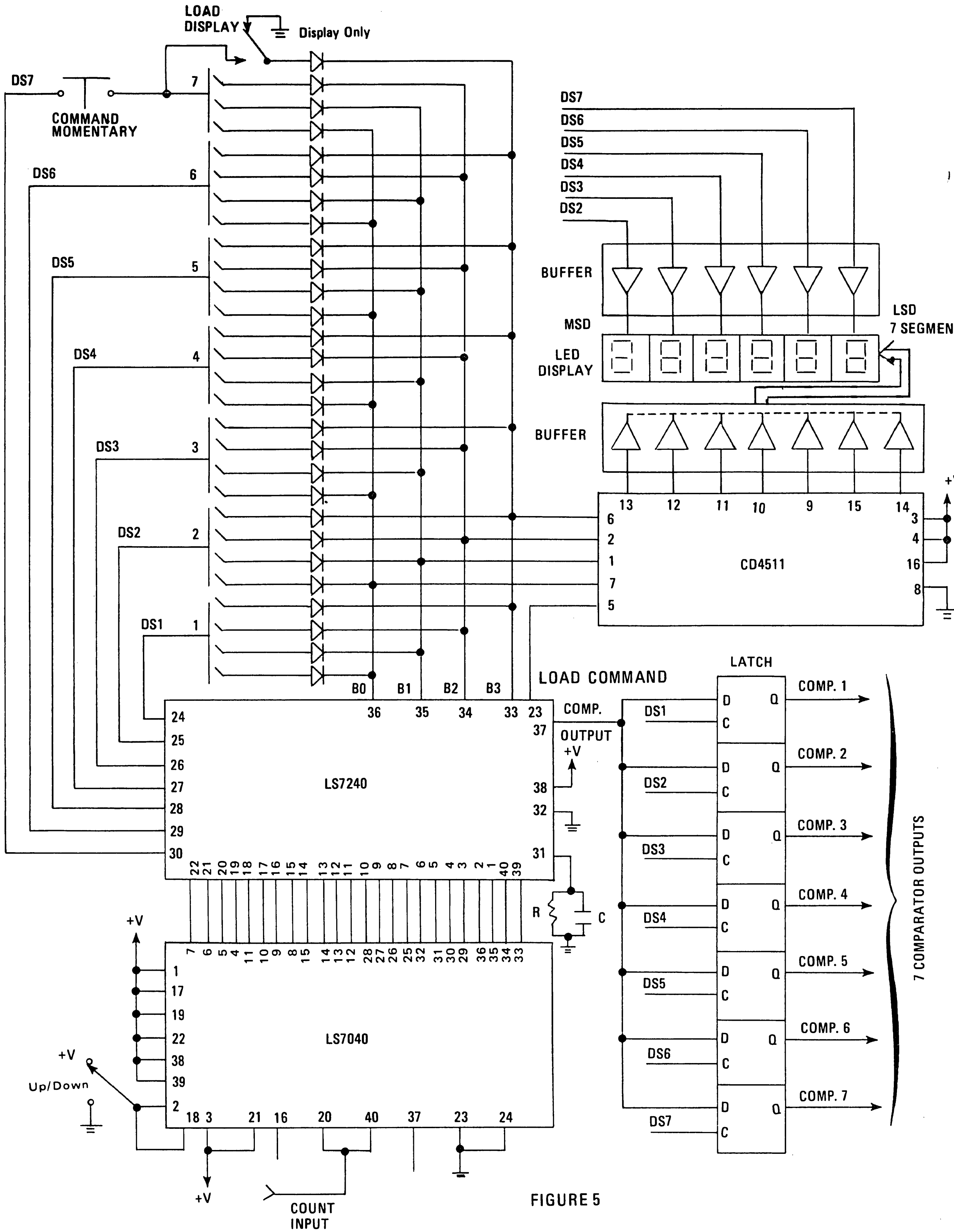


FIGURE 5

The System Interconnection of an LS7240 with an LS7040 and support circuitry is as shown. Thumbwheel 7 selects the memory. Thumbwheel 6 through 1 selects MSD through LSD. If the "Load and Display/Display Only" toggle switch is in the Load and Display position, the data is loaded into the LS7240, and displayed on the LED display when the "COMMAND MOMENTARY" is depressed. The BCD output data of the LS7240 is converted to 7 segment data by the CD4511. As long as the Momentary is held down, the display presents the data just loaded. If the Momentary is released, the display presents the BCD input data from the LS7040. If memory 0 is selected and the toggle switch is in the LOAD AND DISPLAY position, all memories are reset when the momentary is depressed. If the toggle switch is in the "Display Only" position then depressing the momentary will enable the 7 segment display to present what was previously loaded into the memory.

LSI COMPUTER SYSTEMS INC.

Manufacturers of Custom and Standard LSI Circuits
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LS7263 * BRUSHLESS DC MOTOR SPEED CONTROLLER

REVISED NOVEMBER 1985

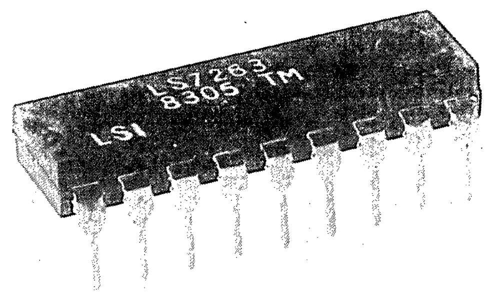
FEATURES:
- Highly accurate speed regulation (±.1% derived from XTL controlled time base.)
- Rapid acceleration to speed with little overshoot
- Positive braking
- 10V to 28V supply range
- Low speed detection output
- Over current logic
- Power on reset
- Six outputs drive power switching bridge directly
- 18 pin dual-in-line package

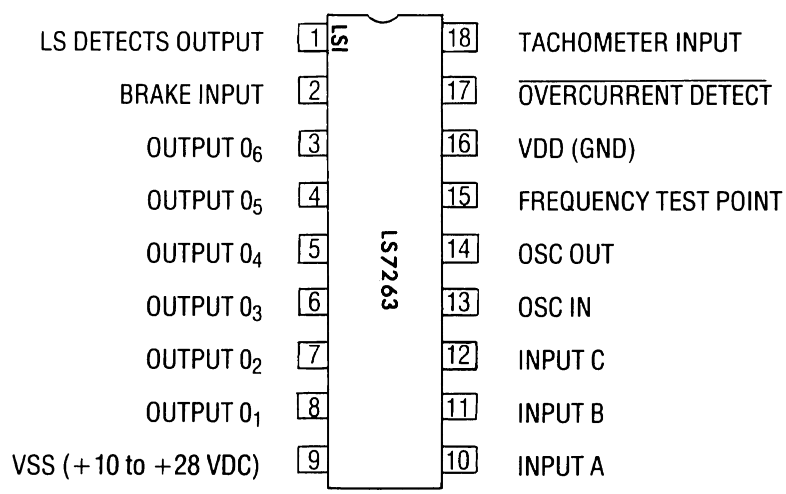
DESCRIPTION:
The LS7263 is a monolithic, ion implanted MOS circuit designed to control the speed of a 3-phase, brushless, D.C. motor. This specific circuit is programmed for use in 3600 RPM applications. The circuit utilizes a 3.58 MHz crystal to provide its accurate speed regulation time base. Overcurrent circuitry is provided to protect the windings, associated drivers and power supply. A positive braking feature is provided to effect rapid deceleration.
Speed corrections are made by measuring the time between tachometer inputs and varying the on time of the drive signal applied to each winding. A sampling window is generated using tachometer input time intervals during which crystal derived clock pulses are accumulated. The contents of the accumulator provide the address of a look up table that has been derived from the physical characteristics of the motor and the load. The look up table output determines the amount of on time for each coil. Positive and negative signals are applied sequentially to each winding driver through the output decoder/driver section.

A static type positive braking system shorts all winding together upon receipt of the brake input. This system creates an electrical load on the motor thus causing rapid deceleration. An overcurrent condition, when sensed at the overcurrent detection input, disables all six winding outputs. Outputs will be reenabled upon removal of the overcurrent condition.

INPUT/OUTPUT DESCRIPTION:
LS DETECT OUTPUT (PIN 1).
This output provides a D.C. level which is high for speeds less than 1100 RPM. It may be used to determine activation of a Winchester drive head.

BRAKE INPUT (PIN 2).
A high level applied to this input turns off outputs 0_1-0_3 and turns on outputs 0_4-0_6, shorting the windings together. The brake input has priority over all other inputs. The brake input is provided with a pull-up resistor.





TOP VIEW
Fig. 1

* See page 4 for available configurations.

INPUT/OUTPUT DESCRIPTION: (continued)

OUTPUTS 0_6, 0_5, 0_4 (PINS 3-5).
These outputs provide the base current (through external limiting resistors) to NPN drivers of the motor coils. They are enabled in the sequence described in Table 1 and for a duration as determined by the internal speed regulation data.

OUTPUTS 0_3, 0_2, 0_1 (PINS 6-8).
The outputs provide the base current to the PNP drivers of the motor coils. They are enabled per Table 1 and the internal speed regulation data.

DESCRIPTION OF OUTPUT SIGNALS: (See Figures 2C, 3C)
An output pair turn on at a change of commutator input state and remain on for a period of time determined by the rotational speed measured within the latest sampling window. The output pulse can be zero if speed is too high. If other than zero, the output width follows the formula O_{PW}=(192 + n × 384 clock periods) × 4 ÷ number of poles, where n varies from zero to 14. If the look up table indicates n is greater than 14, the pair remain on until the next commutation change.

VSS (PIN 9).
Supply voltage positive terminal, (+10 to +28 Vdc.)

A, B, C INPUTS (PINS 10-12).
These inputs have pull up resistors and provide control of the output commutation sequence as per Table 1. A, B, C orginate at the position sensors of the motor (see fig. 2) and must sequence in cyclic order (only one input changes at any time). Figure C illustrates a method for controlling the motor direction of rotation. Figure D indicates how one external invertor may be used to use a 120° circuit type in a 60° sensor separation application (or 60° to 120°).

OSC IN (PIN 13), OSC OUT (PIN 14)
Pin 13 provides one of the two ports necessary for connecting a crystal. It may also be used to drive the circuit from an external clock. Pin 14 is used as the second connection when using a crystal for oscillation. Limited variable speed operation can be obtained by using the oscillator depicted in Figure A whose nominal frequency is 3.58 MHz.

FREQUENCY TEST POINT (PIN 15).
This test output provides the user with a point to measure the oscillator frequency without loading the oscillator. It provides a signal which is one sixth of the oscillator frequency.

VDD (PIN 16).
Supply voltage negative terminal (ground).

$\overline{\text{OVERCURRENT DETECT}}$ (PIN 17).
The Overcurrent Detection Input provides the user a way of protecting the motor windings, drivers and power supply from an overload condition. The user provides a fractional ohm resistor between the positive supply and the common emitters of the PNP drivers. This point is connected to a potentiometer (e.g. 100k ohm), the other end of which is connected to ground and the wiper connected to the overcurrent input. The wiper pickoff is adjusted so that the outputs 0_1-0_6 are off for currents greater than the limit. (Reference Fig. 5) An alternative overcurrent detection circuit is illustrated in Figure B. An overcurrent condition is sensed and latched causing the overcurrent input (pin 17) to become low. When the overcurrent condition terminates, the next positive edge of the chopping frequency will cause pin 17 to become high. This circuit limits the maximum output switching rate to the chopping frequency when an overcurrent condition is prevalent.

An example of setting up the over current follows:

1. Determine the fractional ohm resistance and the maximum current to determine the voltage drop across the resistor and call this V_{OC}.
2. Apply V_{SS}-V_{OC} to the fractional ohmage end of the potentiometer.
3. Hold A, B and C in a known state (e.g. 000). This will enable a pair of outputs in accordance with Table 1.
4. Adjust the potentiometer until outputs 0_1-0_3 are all at V_{SS} and 0_4-0_6 are at ground.
5. Remove the voltage from the potentiometer and connect the potentiometer to the transistor end of the fractional ohm resistor.

TACHOMETER INPUT (PIN 18).
The signal applied to the tachometer input originates at a motor position sensor (one of the commutation inputs may be used). Each negative edge of the tachometer input is synchronized by the one sixth oscillator frequency. The resulting signal 1) transfers new speed regulation data to the "on time" data storage latches, 2) resets the clock pulse accumulator and 3) originates a new sampling window. The tachometer input is provided with a pull-up resistor.

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature			
1. Plastic	T_{ap}	−25 to +70	°C
2. Ceramic	T_{ac}	−55 to +125	°C
Voltage (any pin to V_{SS})	V_{max}	−30 to + 0.5	VOLTS

DC ELECTRICAL CHARACTERISTICS: (+10 to +28 VDC)

SUPPLY CURRENT	SYMBOL	MIN.	MAX.	UNITS
(Excluding Outputs)	I_{DD}	—	22	mA

INPUT SPECIFICATIONS:

Brake, commuting and tachometer (Pins 2, 10, 11, 12, 18)

INPUT VOLTAGE	MIN.	MAX.	UNITS
Logic "1"	V_{SS} - 2.5	V_{SS}	VOLTS
Logic "0"	0	V_{SS} - 5	VOLTS

INPUT CURRENT
Each of the five inputs provides an internal constant current source to V_{SS} of 200 to 400ua (typically 300ua)

OVERCURRENT DETECTION INPUT (PIN 17)

INPUT VOLTAGE	MIN.	MAX.	UNITS
Logic "1"	$(V_{SS}\div 2)+.25$	V_{SS}	VOLTS
Logic "0"	0	$(V_{SS}\div 2)-.25$	VOLTS

Theroretical switching point for the Overcurrent Detection Input is one half of the power supply. Manufacturing tolerances cause the switching point to vary plus or minus .25 volts. After manufacture, the switching point remains fixed with 10mv over time and temperature. The input switching sensitivity is a maximum of 50mV. There is no hysteresis on the overcurrent detection input.

OSCILLATOR INPUT (PIN 13). (When driven from external source.)

	MIN.	MAX.	UNITS
Logic "1"	$V_{SS}-1$	V_{SS}	VOLTS
Logic "0"	0	V_{SS}-6	VOLTS

OUTPUT SPECIFICATIONS

596 KHz TEST (PIN 15)

Designed for 10MΩ, 7pF scope probe.

LS DETECT OUTPUT (PIN 1)

	MIN.	MAX.	UNITS	CONDITIONS
I_{SOURCE}	1.0		mA	Output short circuit to V_{DD}
I_{SINK}	10.0		ua	Output at .5V

0_1-0_6 (PINS 3-8)

0_1-0_3 are current sinks
0_4-0_6 are current sources

Outputs turn on in pairs (see figs. 2C, 3C and 4). For example (see dotted line, fig. 4):
Q8 and Q4 are on, thus enabling a path from the positive supply through the fractional ohm resistor, emitter-base junction of Q101, Q8, Q4, R5 and the base emitter junction of Q105 to ground. The current in the above described pattern is determined by the power supply voltage, the value of R1, the voltage drops across the base-emitter, junction of Q101 and Q105 (1.4 volts for single transistor or 2.8V for Darlington pairs), the impedance of Q8 and Q4 and the value of R5.

TABLE 1A −01,

INPUTS A	B	C	OUTPUTS ENABLED	DRIVER A*	DRIVER B*	DRIVER C*
0	0	0	$0_1, 0_5$	+	−	OFF
1	0	0	$0_3, 0_5$	OFF	−	+
1	1	0	$0_3, 0_4$	−	OFF	+
1	1	1	$0_2, 0_4$	−	+	OFF
0	1	1	$0_2, 0_6$	OFF	+	−
0	0	1	$0_1, 0_6$	+	OFF	−

TABLE 1B −02, −03, −07

INPUTS A	B	C	OUTPUTS ENABLED	DRIVER A*	DRIVER B*	DRIVER C*
0	0	1	$0_2, 0_6$	OFF	+	−
1	0	1	$0_2, 0_4$	−	+	OFF
1	0	0	$0_3, 0_4$	−	OFF	+
1	1	0	$0_3, 0_5$	OFF	−	+
0	1	0	$0_1, 0_5$	+	−	OFF
0	1	1	$0_1, 0_6$	+	OFF	−

Push pull drivers are made up of pairs of Outputs: 0_1 and 0_4 (Driver A), 0_2 and 0_5 (Driver B), 0_3 and 0_6 (Driver C).

*See Fig. 4

DESCRIPTION OF AVAILABLE TYPES

TYPE	POLES	SENSOR SEPARATION	GAIN*
7263-01	4	60°	Medium
7263-02	8	120°	High
7263-03	4	120°	Medium
7263-07	8	120°	Medium

*Gain describes the change of output duty cycle as a function of change of motor speed for the high gain type, the duty cycle is caused to change from 0% to 100% over a 6 RPM motor speed change. For the medium gain type, the duty cycle changes from 0% to 100% when the motor speed changes by 40 RPM.

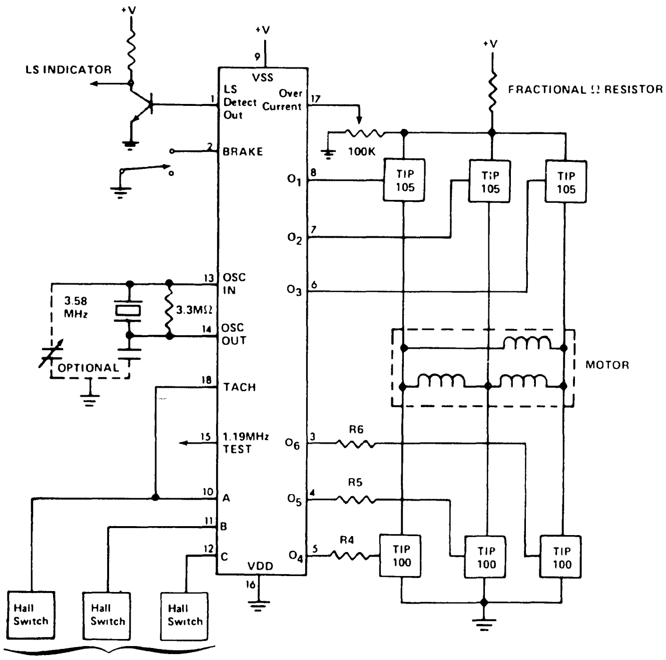
The following chart provides the recommended value for R5. R4 and R6 are the same value.

OUTPUT CURRENT
(DRIVING DARLINGTON PAIRS)

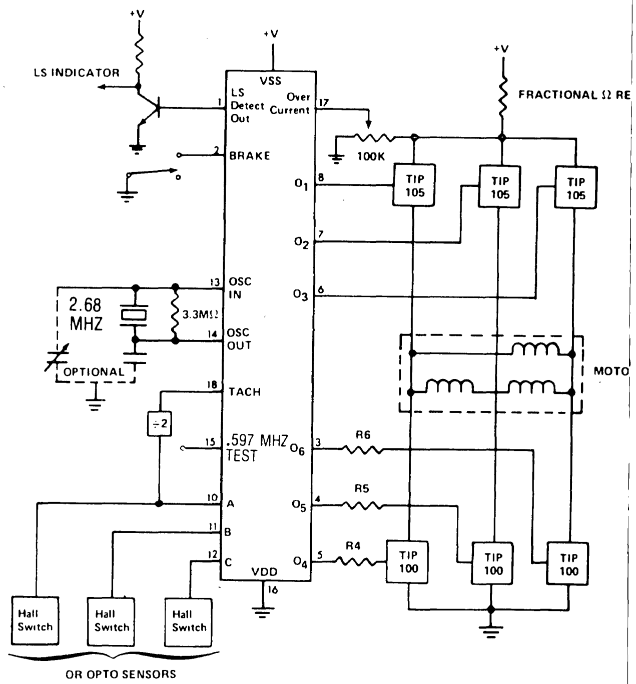
POWER SUPPLY VOLTS	20	15	10	7.5	5	2.5	mA
12	.1	.25	.56	.86	1.5	3.3	
15	.33	.51	.92	1.3	2.1	4.6	
18	*	.76	1.3	1.7	2.8	5.8	
21	*	*	1.6	2.2	3.3	7.0	
24	*	*	1.9	2.6	4.0	8.3	
28	*	*	*	3.2	4.9	9.9	

*causes excessive power dissipation.

RESISTANCE IN KILOHMS

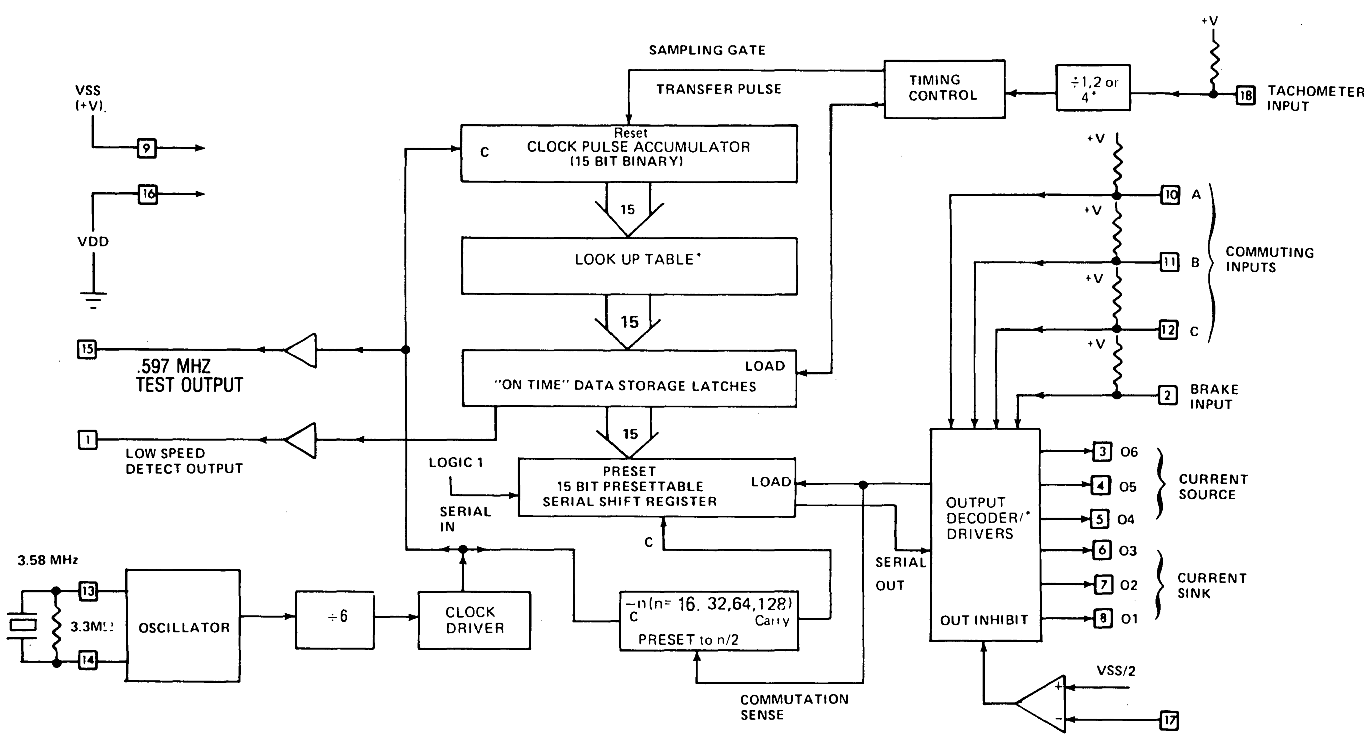


APPLICATION DIAGRAM
THREE PHASE BRUSHLESS DC MOTOR
OPERATING AT 3600 RPM
Figure 5

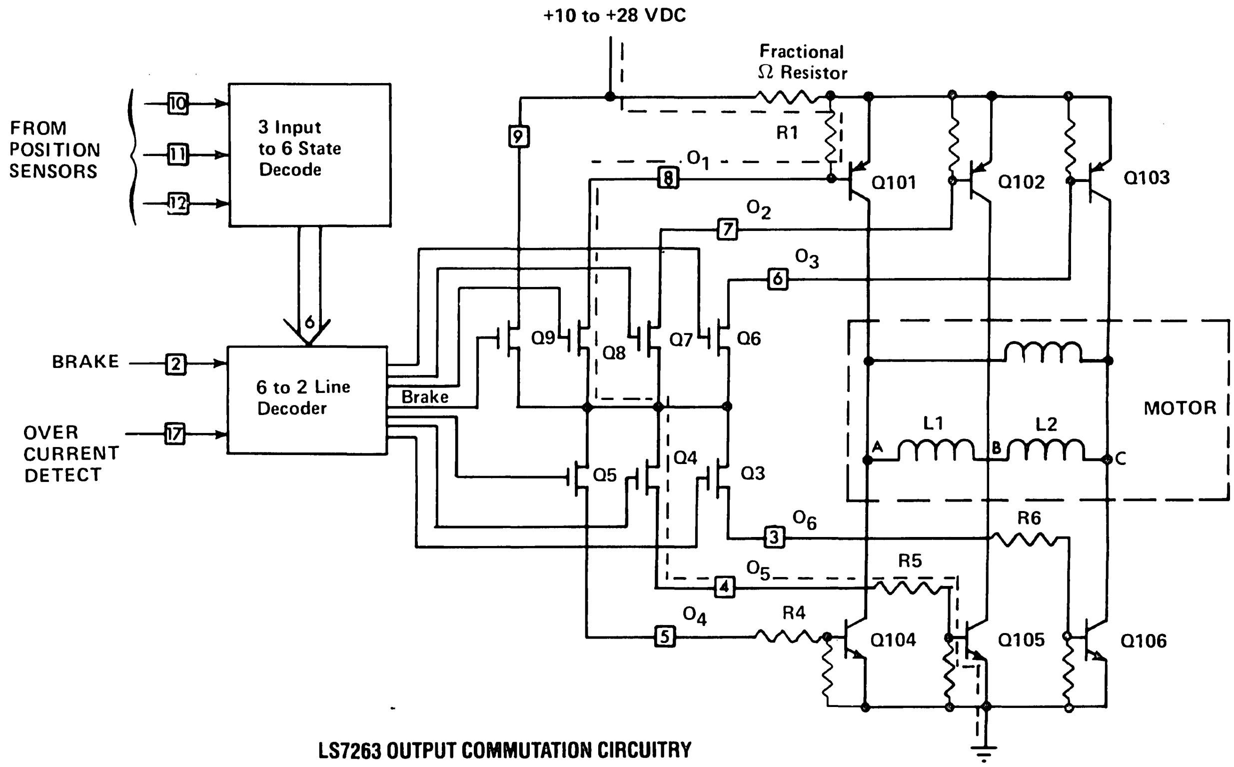


Tach input using ÷2 with output data rate doubled to achie 5400 RPM operation.

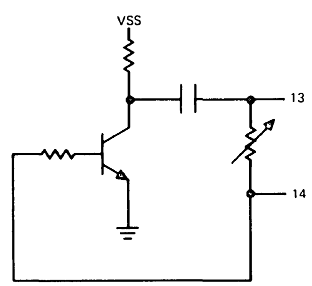
APPLICATION DIAGRAM
THREE PHASE BRUSHLESS DC MOTOR
OPERATING AT 5400 RPM
Figure 6



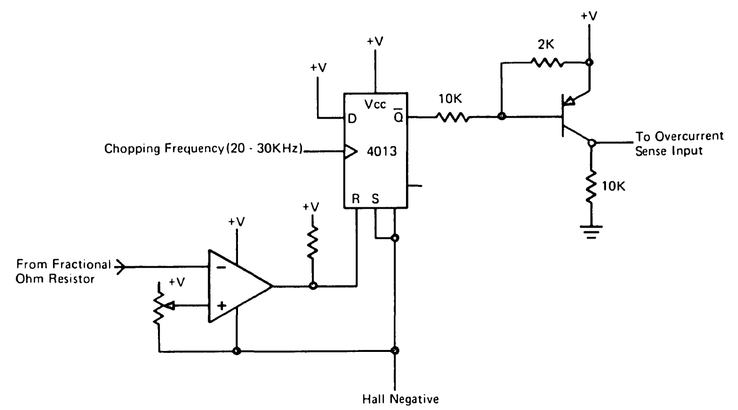
LS7263 MOTOR SPEED CONTROLLER
BLOCK DIAGRAM
Figure 7



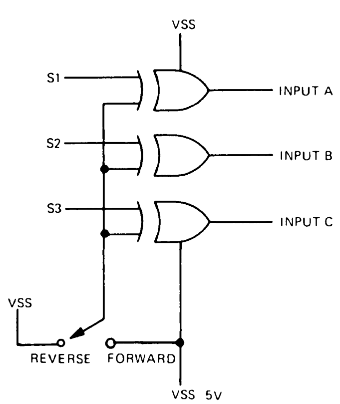
LS7263 OUTPUT COMMUTATION CIRCUITRY
Figure 4



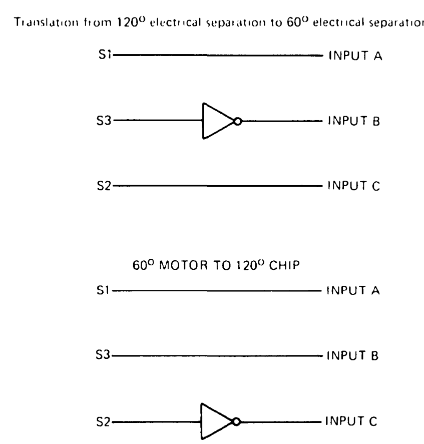
VARIABLE OSCILLATOR · FIGURE A



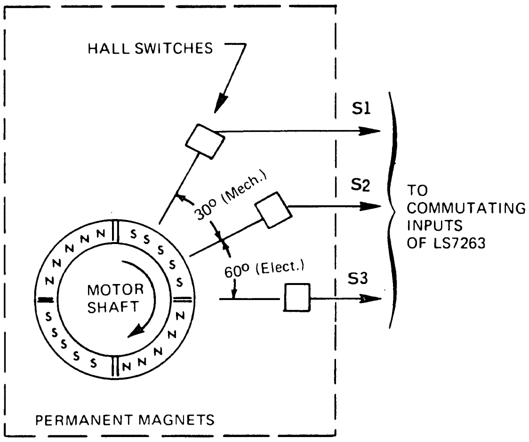
EXTERNAL OVERCURRENT SENSE WITH CHOPPING · FIGURE B



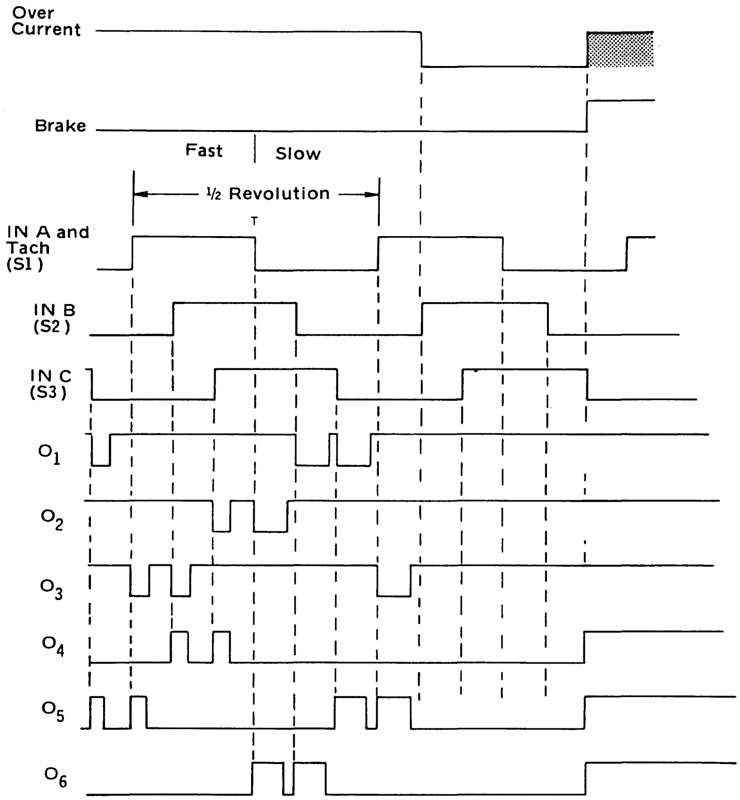
FORWARD REVERSE OPERATION FIGURE C



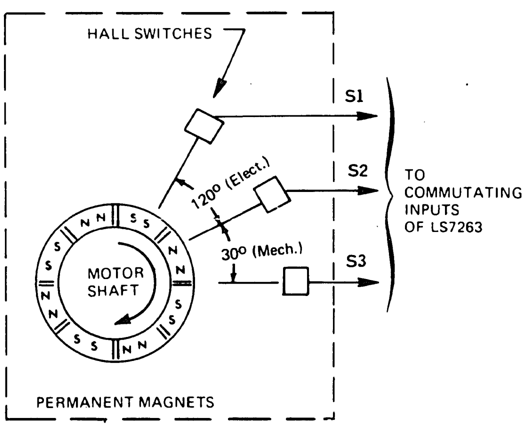
SENSOR SEPARATION CONVERSION FIGURE D



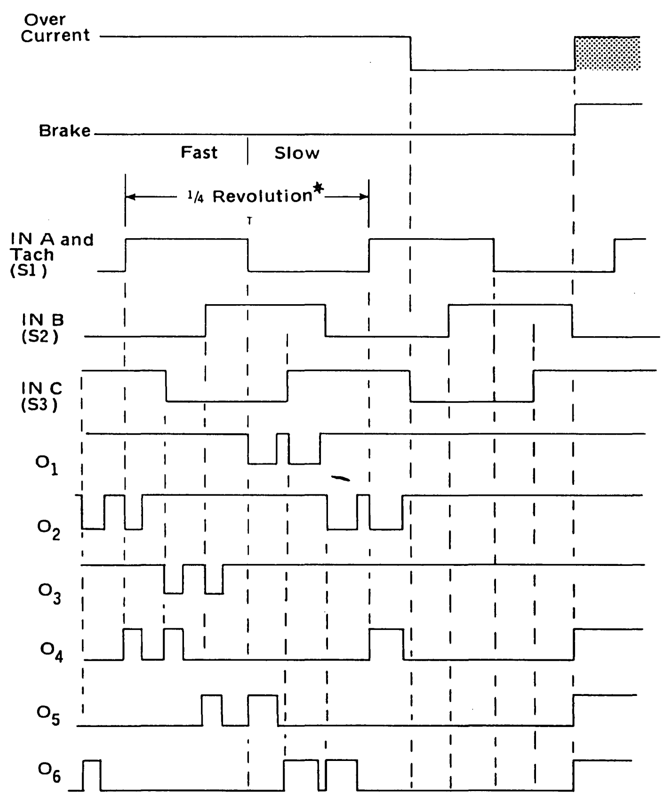
HALL SWITCH POSITIONING DIAGRAM
FOR LS7263-01
FIGURE 1B



TIMING DIAGRAM
FOR LS7263-01
FIGURE 2C

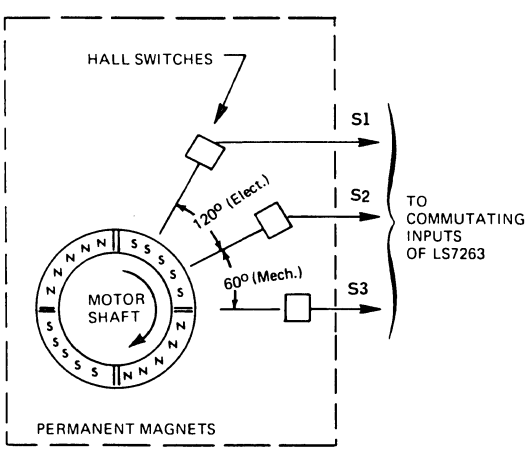


HALL SWITCH POSITIONING DIAGRAM
FOR LS7263-02, 07
FIGURE 2B



TIMING DIAGRAM
FOR LS7263-02, 03, 07
FIGURE 3C

* ½ Revolution for LS 7263-03



HALL SWITCH POSITIONING DIAGRAM
FOR LS 7263-03
FIGURE 3B

LSI COMPUTER SYSTEMS INC.

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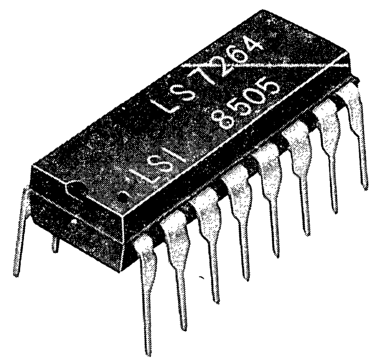
LS7264 | FOUR PHASE BRUSHLESS DC MOTOR SPEED CONTROLLER

REVISED NOVEMBER 1985

FEATURES:
- Highly accurate speed regulation (± .1%) derived from XTL controlled time base.
- Rapid acceleration to speed with little overshoot
- Static braking
- 10V to 28V supply range
- Low speed detection output
- Internal over current logic
- Power on reset
- Four outputs drive power switching transistors directly
- 16 pin dual-in-line package



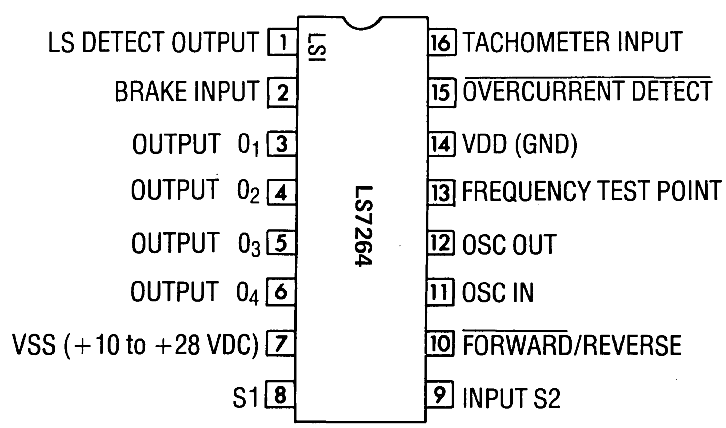
DESCRIPTION:
The LS7264 is a monolithic, ion implanted MOS circuit designed to control the speed of a 4-phase, brushless, D.C. motor. This specific circuit is programmed for use in 3600 RPM applications. The circuit utilizes a 2.4576 MHz crystal to provide its accurate speed regulation time base. Overcurrent circuitry is provided to protect the windings, associated drivers and power supply. A static braking feature is provided to effect rapid deceleration.

Speed corrections are made by measuring the time between tachometer inputs and varying the on time of the drive signal applied to each winding. A sampling window is generated during which crystal derived clock pulses are accumulated. The contents of the accumulator provide the address of a look up table that has been derived from the physical characteristics of the motor and the load. The look up table output determines the amount of on time for each coil. Positive signals are applied sequentially to each winding driver through the output decoder/driver section.

A static type braking system shorts all winding together upon receipt of the brake input. This system creates an electrical load on the motor thus causing rapid deceleration. An overcurrent condition, when sensed at the overcurrent detection input, disables all four winding outputs. Outputs will be reenabled upon removal of the overcurrent condition.

INPUT/OUTPUT DESCRIPTION:
LS DETECT OUTPUT (PIN 1).
This output provides a D.C. level which is high for speeds less than 1000 RPM.

BRAKE INPUT (PIN 2):
A high level applied to this input turns on all outputs, shorting the windings together. The brake input has priority over all other inputs. This feature may only be used when the center tap is connected to the positive supply through an external PNP transistor which is controlled by the brake signal. The brake input is provided with a pull-up resistor.



TOP VIEW
Fig. 1

INPUT/OUTPUT DESCRIPTION: (continued)

OUTPUTS 0_1, 0_2, 0_3, 0_4, (PINS 3-6)

These open drain outputs provide the base current (through external limiting resistors) to the base inputs of NPN drivers of the motor coils. They are enabled in the sequence described in Table 1 and for a duration as determined by the internal speed regulation data.

DESCRIPTION OF OUTPUT SIGNALS: (See Figures 1B)

Each output turns on at a change of commutator input state and remains on for a period of time determined by the rotational speed measured within the latest sampling window. The output pulse can be zero if speed is too high. If other than zero, the output width follows the formula $0_{PW} = (n \times 384 \times 4 \div \text{No. of poles})$ clock periods, where n varies from zero to 15. If the look up table indicates n is greater than 15, the pair remain on until the next commutation change.

VSS (PIN 7).

Supply voltage positive terminal, (+10 to +28 VDC).

S1, S2 INPUTS (PINS 8, 9)

These inputs provide control of the output commutation sequence as per Table 1. S1, S2 originate at the position sensors of the motor (see fig. 2). S1 and S2 are provided with a pull-up resistor.

$\overline{\text{FORWARD}}$/REVERSE INPUT (PIN 10)

This Pin is used to control the motor's direction of rotation (see table I).

OSC IN (PIN 11).

This pin provides one of the two ports necessary for connecting a crystal. It may also be used to drive the circuit from an external clock.

OSC OUT (PIN 12).

This pin is used as the second connection when using a crystal for oscillation.

FREQUENCY TEST POINT (PIN 13).

This test output provides the user with a point to measure the oscillator frequency without loading the oscillator: It provides a signal which is one sixth of the oscillator frequency.

VDD (PIN 14).

Supply voltage negative terminal (ground).

$\overline{\text{OVER CURRENT DETECT}}$ (PIN 15).

The Overcurrent Detection Input provides the user a way of protecting the motor windings, drivers and power supply from an overload condition. The user provides a fractional ohm resistor between the positive supply and the positive side of the motor windings. This point is connected to a potentiometer (e.g. 100k ohm), the other end of which is connected to ground and the wiper connected to the overcurrent input. The wiper pickoff is adjusted so that the outputs 0_1 — 0_4 are off for currents greater than the limit.

An example of setting up the over current follows:

1. Determine the fractional ohm resistance and the maximum current to determine the voltage drops across the resistor and call this V_{OC}.
2. Apply V_{SS}-V_{OC} to the fractional ohmage end of the potentiometer.
3. Hold S1 and S2 in a known state (e.g.00). This will enable 0_1-0_4 outputs in accordance with Table 1.
4. Adjust the potentiometer until outputs 0_1-0_4 are at ground.
5. Remove the voltage from the potentiometer and connect the potentiometer to the winding end of the fractional ohm resistor.

TACHOMETER INPUT (PIN 16).

The signal applied to the tachometer input originates at a motor position sensor (one of the commutation inputs may be used). Each negative edge of the tachometer input is synchronized by the one sixth oscillator frequency. The resulting signal 1) transfers new speed regulation data to the "on time" data storage latches, 2) resets the clock pulse accumulator and 3) originates a new sampling window. The tachometer input is provided with a pull-up resistor.

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature			
1. Plastic	T_{ap}	−25 to +70	°C
2. Ceramic	T_{ac}	−55 to +125	°C
Voltage (any pin to V_{SS})	V_{max}	−30 to +0.5	VOLTS

DC ELECTRICAL CHARACTERISTICS: (+10 to +28 VDC)

SUPPLY CURRENT	SYMBOL	MIN.	MAX.	UNITS
(Excluding Outputs)	1_{DD}	—	22	mA

INPUT SPECIFICATIONS:

Brake, commuting and tachometer (Pins 2, 10, 11, 12, 18)

INPUT VOLTAGE	MIN.	MAX.	UNITS
Logic "1"	V_{SS}-2.5	V_{SS}	VOLTS
Logic "0"	0	V_{SS}-5	VOLTS

INPUT CURRENT

Each of the five inputs provides an internal constant current source to V_{SS} of 200 to 400 ua (typically 300ua)

OVERCURRENT DETECTION INPUT (PIN 15)

INPUT VOLTAGE	MIN.	MAX.	UNITS
Logic "1"	$(V_{SS} \div 2) + .25$	V_{SS}	VOLTS
Logic "0"	0	$(V_{SS} \div 2) - .25$	VOLTS

Theoretical switching point for the Overcurrent Detection Input is one half of the power supply. Manufacturing tolerances cause the switching point to vary plus or minus .25 volts. After manufacture, the switching point remains fixed within 10mv over time and temperature. The input switching sensitivity is a maximum of 50mV. There is no hysteresis on the overcurrent detection input.

OSCILLATOR INPUT (PIN 11). (When driven from external source.)

	MIN.	MAX.	UNITS
Logic "1"	V_{SS}-1	V_{SS}	VOLTS
Logic "0"	0	V_{SS}-6	VOLTS

OUTPUT SPECIFICATIONS

410 KHz TEST (PIN 13)
Designed for 10MΩ, 7pF scope probe.

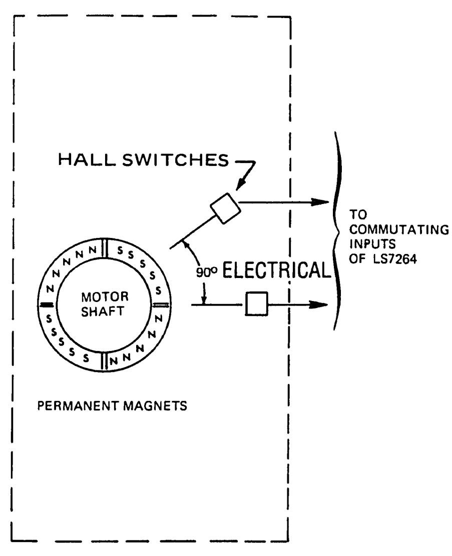
LS DETECT OUTPUT (PIN 1)

	MIN.	MAX.	UNITS	CONDITIONS
I_{SOURCE}	1.0		mA	Output short circuit to V_{DD}
I_{SINK}	10.0		ua	Output at .5V

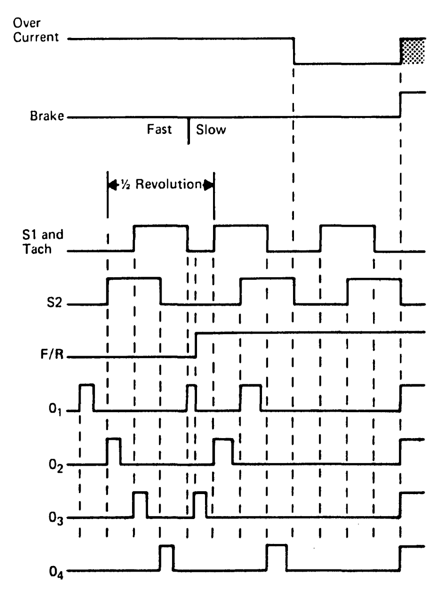
0_1-0_4 (PINS 3-6)
0_1-0_4 are current sources (Base current limiting resistors are required)

TABLE 1

$\overline{F}$/R	S1	S2	OUTPUTS ENABLED
0	0	0	0_1
0	0	1	0_2
0	1	1	0_3
0	1	0	0_4
1	0	0	0_3
1	1	0	0_2
1	1	1	0_1
1	0	1	0_4



HALL SWITCH POSITIONING DIAGRAM FOR LS7264-01 FIGURE 1A



TIMING DIAGRAM FOR LS7264-01 FIGURE 1B

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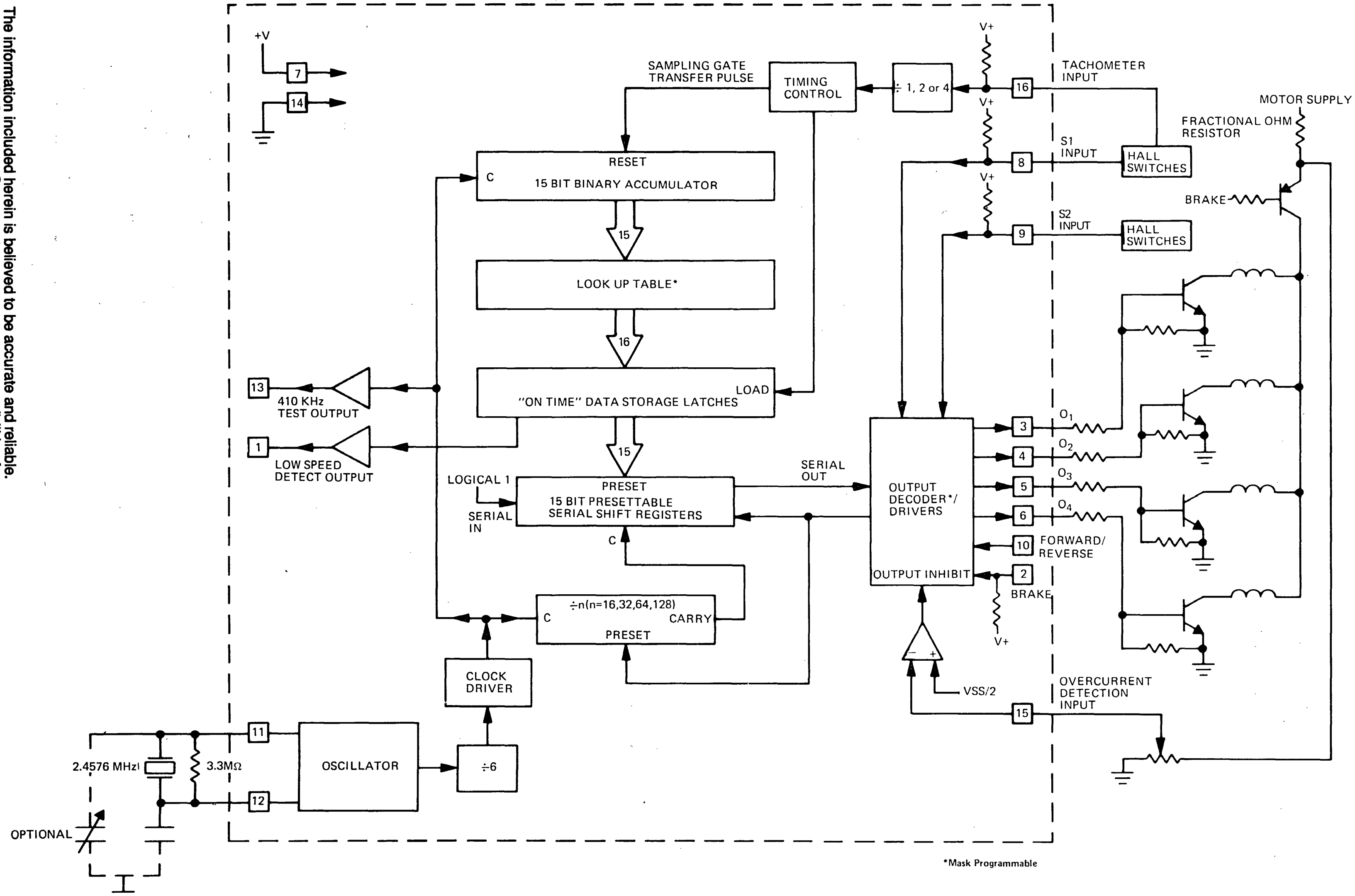

LS7264 MOTOR SPEED CONTROLLER BLOCK DIAGRAM AND INTERCONNECTION FIGURE 2

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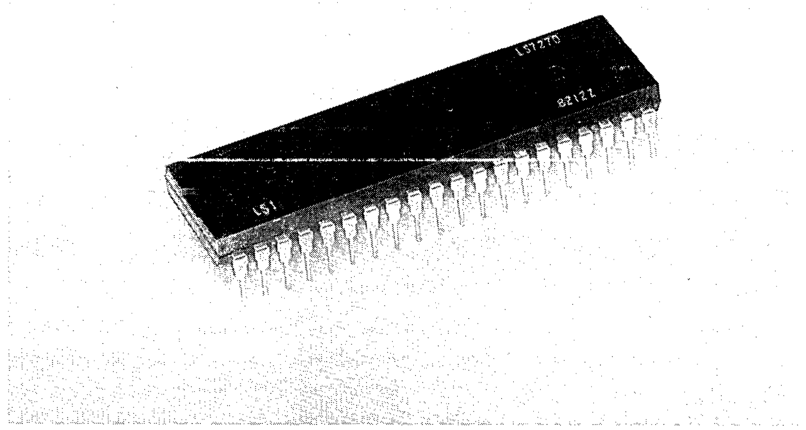
S7270 | PROGRAMMABLE INTEGRATED CONTROLLER/SEQUENCER

NOVEMBER 1984

FEATURES:

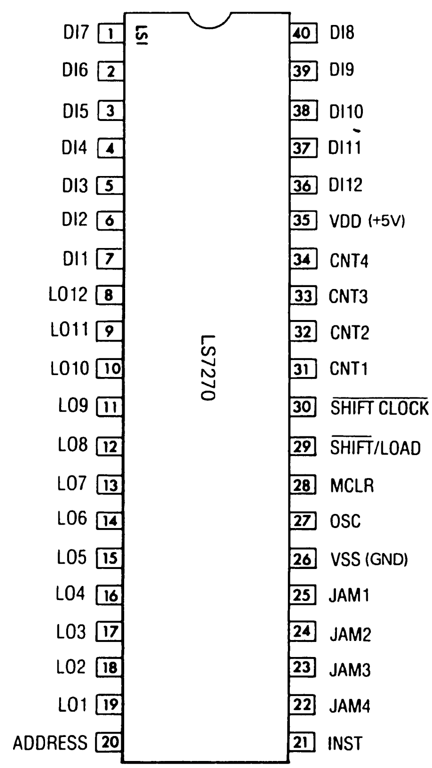
- Hardware oriented simple instruction set
- 4 on-chip 12 bit programmable down-counters
- 4 priority interrupt (JAM) inputs
- 12 discrete inputs
- 12 latched outputs
- 12 discrete memory bit registers
- Anti-bounce circuits on DI, CNT and JAM inputs for direct interface with mechanical switches, keyboards, etc.
- Simple serial interface to external program memory (PROM or ROM)
- External program memory up to 2048 instructions
- On-chip clock generator
- Inputs TTL, NMOS and CMOS compatible
- Outputs TTL, NMOS and CMOS compatible
- Single power supply operation. +4.75 VDC to +12 VDC
- 40 pin plastic DIP



GENERAL DESCRIPTION:

The LS7270 is a monolithic, ion implanted MOS logic controller/sequencer, designed to satisfy a wide variety of timing, sequencing and controlling functions in small to medium sized systems requiring low cost electronic control hardware. A "basic controller/sequencer" type machine can be thought of as a simple "black box" with inputs, outputs and various chip support functions such as power supply, oscillator, etc. As in any sequential logic machine, the present state of the machine is logically combined with the present state of the inputs to produce a new machine state with its corresponding outputs. Hence, as inputs change, the machine reacts generating new outputs depending on its previous state and the new inputs.

In a traditional hardwired logic machine, the sequence of the machine for all possible combinations of inputs is determined by the design of various random logic units all permanently wired so that the results is not very flexible or amenable to change. The solution to this problem as implemented in the LS7270, is to utilize some form of computer or microprocessor type architecture that executes a series of instructions (the program steps) held in a memory (external to the chip) to perform the intended logical combinations of the inputs with the current machine state. In contrast to computers or microprocessors, however, the internal architecture of the LS7270 is geared to individual bit processing, Boolean processing, turn-on and turn-off functions, counting and timing operations as opposed to numeric computations. Broadly speaking, (see Fig. 1



TOP VIEW

and Description of General Architecture) the LS7270 has discrete inputs (DI) that can be addressed and operated upon at the individual bit level, internal flags (T) and storage cells (M) also addressed and operated upon at the bit level, addressable internal counters that can be clocked by external sources and a group of individually addressable output register (LO). Boolean processing is done by selecting and multiplexing various inputs into the Logic Unit (LU) along with the working Accumulator Flag (AF), thus performing sequentially the required Boolean expression and then outputting the result to the appropriate output. This is done under control of a sequence of instructions (a table of logical "O"s and "1"s) fetched from the external program memory.

In operation, the LS7270 serially shifts out a memory address when the chip is in the "shift cycle." An external shift register has to be provided in which the address can be shifted and set up for addressing the memory (see fig. 2). During the shift cycle, clocks are generated at the shift clock output which are in synchronism with the address bit changes at the address output. At the end of the shift cycle, instruction from the memory is loaded into the interface shift register. A new shift cycle begins, and the instruction from the Interface Shift Register is now shifted into the LS7270; simultaneously a new instruction address is shifted out into the interface shift register. The LS7270 continuously alternates between the "shift" and the "load" cycles executing the instruction in between whenever a complete instruction has been fetched. The address is automatically incremented by 1 in every shift cycle so that instructions from higher locations of a memory can be fetched sequentially. This general rule of address sequencing is broken only when an instruction involving an address jump is executed. When an instruction is executed one of the following events may take place (see the instruction set for details):

1. Load 1 of 4 counters with a 12 bit number specified in the instruction field,
2. Decrement one of the counters,
3. Set or reset one of the internal registers,
4. Load the AF with the true or complement value of one of the internal registers or discrete inputs,
5. Combine AF with the true or complement value of any of the internal registers or discrete inputs in Boolean operation,
6. Store the true or complement value of the AF in any of the internal registers or output latches, and finally,
7. Branch out from normal addressing sequence and jump to an address specified in the instruction field.

GENERAL ARCHITECTURE OF LS7270 (See Fig. 1)

Program Counter (PC and PCB). The PC is a 12 bit register that holds the address for the next instruction. The external memory address is serially shifted out from the PC to the memory. The PCB is a back-up register for the PC used internally by the LS7270 chip.

Instruction Register (IR). The IR is a 16 bit register that holds the instruction currently being executed. Instructions from the external memory are serially shifted into the IR.

STACK 0-2. The LS7270 has a 3 level Last In-First Out (LIFO) stack. The next instruction address from the PCB is pushed onto the stack when a Jump to Subroutine (JS) instruction or a JAM 1 interrupt is executed. The address is returned to the PCB when a Return from Subroutine instruction is executed.

JAM Request Registers (JRR 1-4). The JRRs are 4 one-bit registers that are set by the corresponding JAM inputs. The outputs of the JRRs cause a Jump within the program sequence. Each JRR has a dedicated address assigned to it as its jump destination.

Counters (CNTR 1-4). The LS7270 has four 12 bit programmable down-counters. The counters can be clocked by either external count inputs or the internal clock under program control. Outputs from each counter are decoded for zero and testable under program control.

Logic Unit and the Accumulator Flag (LU and AF). The LU performs all the Boolean algebraic operations contained in the LS7270 instruction set and stores the result in the AF.

Temporary Flags (T1-3). The T's are three one-bit registers each of which can be accessed by the TEMP field of the LOGICAL CONTROL group instructions.

Memory Flags (M1-12). The M's are 12 one-bit registers. The output of the LU can be stored in any of these registers by program control. The outputs of the M's in turn can be logically combined with other inputs to the LU.

Latched Output Registers (LO 1-12). The LO's are 12 one-bit registers each of which can be loaded by the LU data. The LO outputs are available on the output pins.

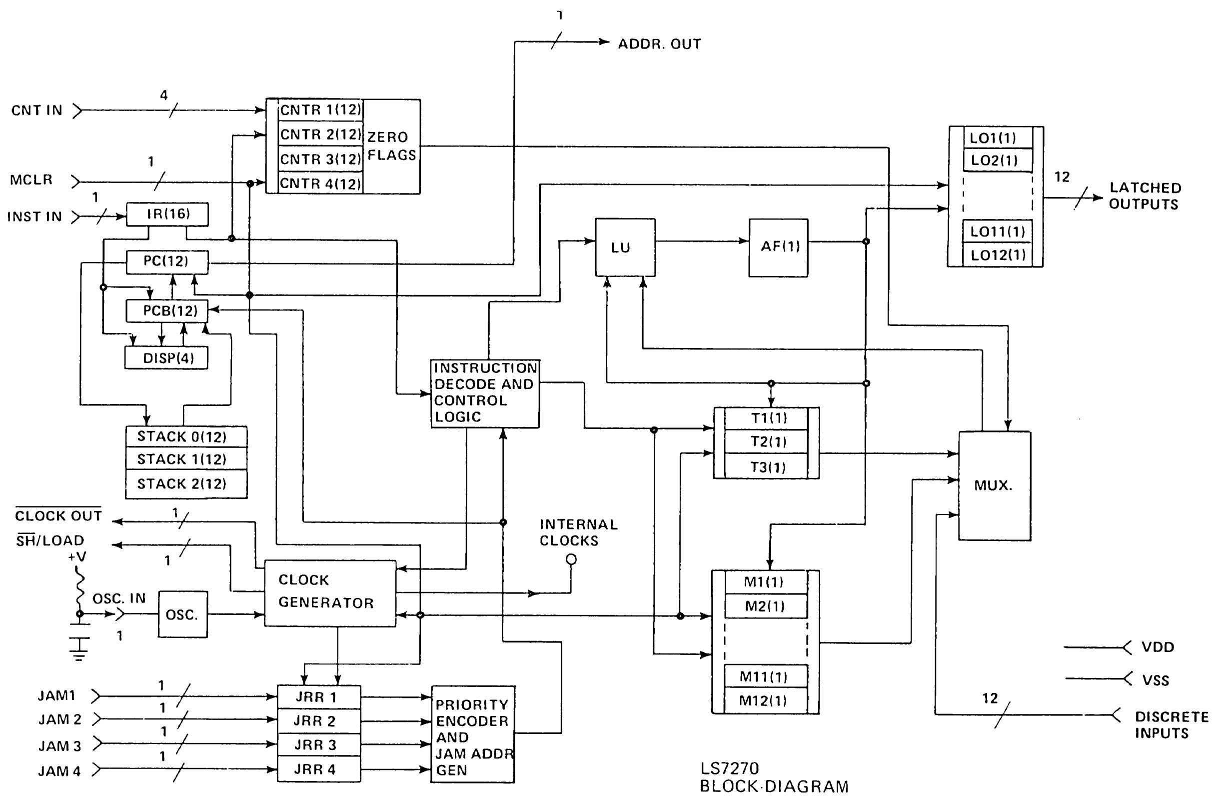
Multiplexer (MUX). The MUX performs all the steering operations of the T's, M's, AF and the Discrete inputs to LU.

DESCRIPTION OF OPERATION: (see figs. 4, 5 and 6)

The LS7270 address consists of 12 bits, and the instruction of 16 bits. In normal operation an instruction cycle consists of 2 shift/load cycles involving 26 shift clocks.

After a reset, the Program Counter (PC) is cleared to address the first memory location (address 0). When the reset is removed, the 12 bit memory address of the first location is serially sent out. During this time, the shift/load output remains low to hold the memory interface shift register in the shift mode. At the end of the shift cycle consisting of 12 shift clocks, the shift/load output goes high placing the interface shift register in the load mode and the first instruction byte (lower byte) from the external memory matrix is loaded into the interface shift register on the thirteenth clock pulse. During every shift/load cycle the PC is incremented by 1 to address the next higher memory location. Then a shift cycle begins again. During this shift cycle while the address for the second byte (higher byte) of the instruction is shifted out to the interface shift register, the lower byte of the instruction, already in the interface shift register, is shifted into the Instruction Register (IR). Note that the internal shift clock for the IR occurs coincident with the first eight shift clocks only since one instruction byte consists of eight bits; there are no shift clocks for the IR corresponding to the remaining five clocks of the total shift/load cycle. At the end of the second shift cycle, the second instruction byte (upper byte) is loaded into the interface register. During the third shift cycle, the upper byte is shifted into the IR and, at the end of the cycle, the instruction is executed. It is important to note that if a smaller external memory is used which does not require all 12 bit addressing capability (4096 bytes or 2048 instructions), the interface register can be implemented with fewer bits and the higher order address bits will simply "fall off' the interface register during the shifting cycle. Thus if only 256 bytes of memory is required, the interface register could be implemented with one octal shift register.

The four programmable down-counters can be driven by either external clocks applied at the counter inputs or decremented under program control. The counters are programmable by instruction control only. During the execution of an instruction for loading or decrementing a counter, the external count input is blocked for a period of 2 shift clocks. The external count input is synchronized with the internal clock so that counter integrity is not lost during the blocking period. The blocking period for any count input lasts between trailing edges of 8th and 10th shift clocks of a high byte fetch cycle containing a load or decrement instruction for the corresponding counter.



LS7270
BLOCK DIAGRAM
FIGURE 1

A counter zero condition can be tested by program control to create decision branching within the program sequence.

The 12 discrete inputs (DI) can be combined with the accumulator flag (AF) to perform Boolean operations and the result steered to 12 single bit memory flags (M) or 12 output latches (LO), or 3 temporary storage flags (T).

I/O DESCRIPTION:

MCLR INPUT:

A high on this input initializes all the registers and holds the clock off. It clears the PC, the JAM request register (JRR), the output latches (LO), the temporary storage flags (T), and the memory flags (M). It presets the down-counters to all 1's. The MCLR input has an internal pull-down (to logic "0") resistor.

OSC INPUT:

An R/C network on this input sets up the frequency of the internal oscillator. The basic oscillator frequency as indicated by the ramp frequency developed on the OSC input is divided down by 4 for generating the internal system clock. The basic oscillator frequency is approximately given by the relation, f = 1/RC.

INST INPUT:

Instructions from external memory are serially shifted into the IR on this input with the LSB being input first. The INST input has an internal pull-down (to logic "0") resistor.

JAM INPUTS:

The JAM inputs are four vectored priority interrupts with JAM 1 having the highest priority and JAM 4 the lowest. A low to high transition of a JAM input forces a specific address into the PC at the end of the currently executing instruction. The four specific addresses allocated for JAM 1 through JAM 4 are 2, 4, 6, and 8, respectively. JAM 1 is different from the other JAMS in that it saves the address of the next instruction on the push down stack so that by including a RETURN instruction at the end of the JAM service routine, the original program sequence can be resumed. JAM request registers are set by a positive transition of the JAM inputs and are reset after the JAM has been serviced. If the JAM input remains high, it will not be serviced a second time. But a high level on a JAM input will inhibit all the lower priority JAM inputs. If a lower priority JAM is activated while a higher priority JAM request is being serviced (with the higher priority JAM input already returned low), the lower priority JAM request will be serviced at the end of the current instruction cycle. All JAM inputs have internal anti-bounce-circuits for direct interface with switches, relays, etc.

COUNTER INPUTS (CNT):

Each of the four counter inputs clocks one of the four 12 bit down counters. The counter advances on the positive transition of the counter input. All counter inputs have internal anti-bounce circuits.

DISCRETE INPUTS (DI):

Each of the 12 discrete inputs can be read by the program as part of Boolean logical expression evaluation. All discrete inputs have internal anti-bounce circuits.

SHIFT CLOCK OUTPUT:

This output is used for clocking the memory interface shift registers. The negative edge of the clock output should be used to clock the shift register.

SHIFT/LOAD OUTPUT:

This output is used for shift/load control of the memory interface shift register. Each shift/load cycle encompasses 13 shift clocks. When the shift/load output is "low," 12 output clocks serially shift out a 12 bit memory address, while the instruction byte from the preceding address is simultaneously shifted into the IR. At the end of the 12 shift clocks, the shift/load output goes "high" for one clock period. During this period, the next instruction byte is loaded into the shift register and a new shift cycle begins.

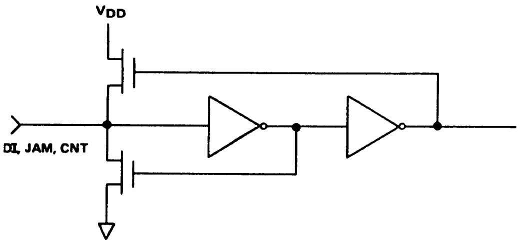


FIGURE 2. Input Anti-Bounce Circuit

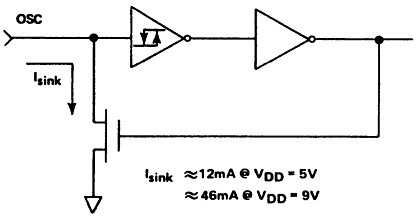


FIGURE 3. Internal Oscillator Circuit

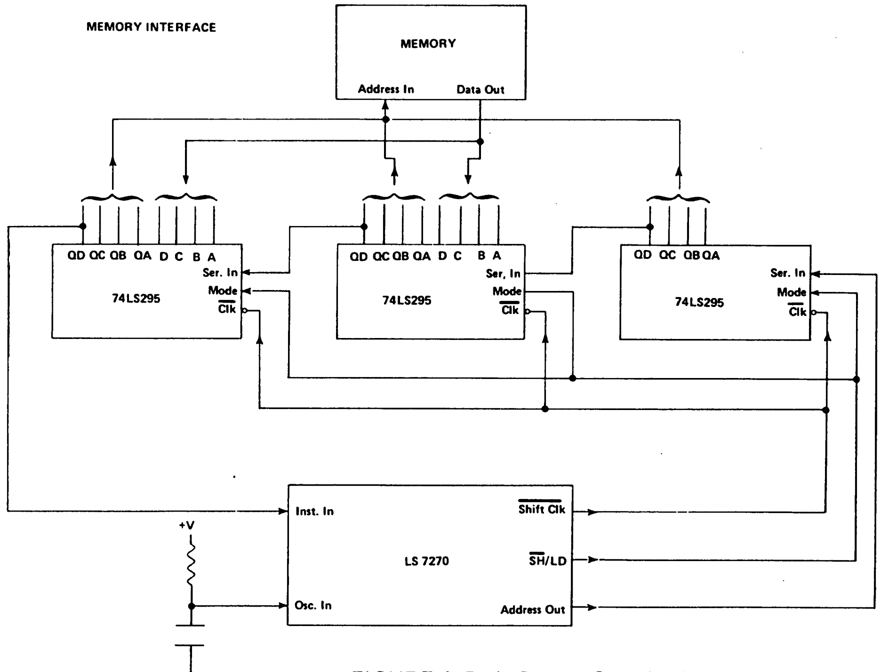
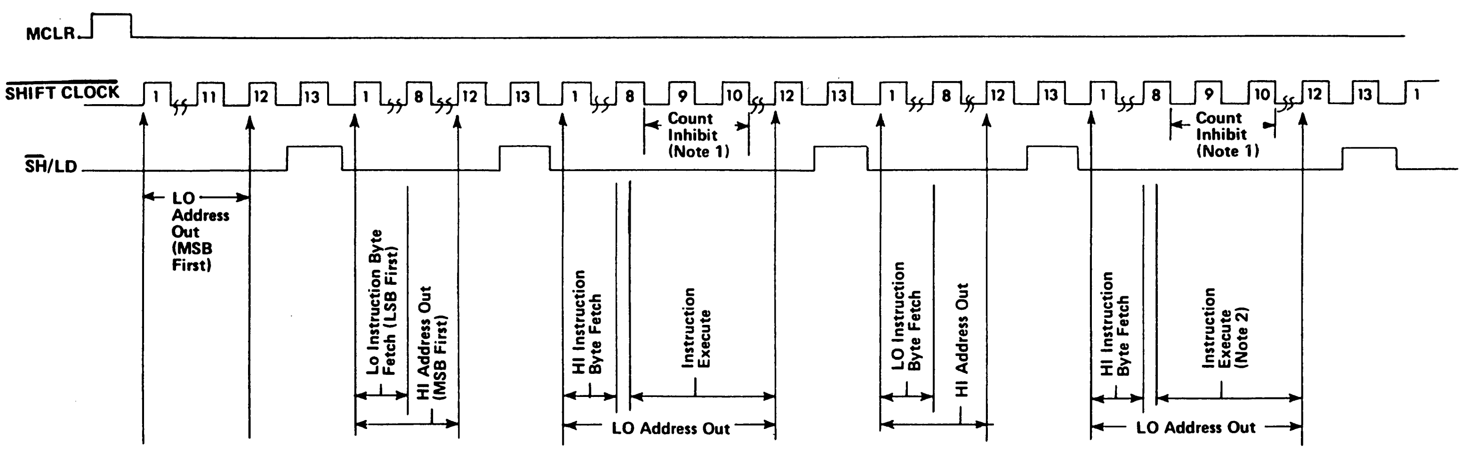


FIGURE 4. Basic System Organization



Note 1 : External Count to a counter is inhibited during the execution of a load or decrement instruction operating on that counter.

Note 2 : Following the execution of a J, JS, RET, SKIP and JAM, three address cycles will be generated instead of regular two, before the next instruction is executed.

FIGURE 5. Instruction Cycles

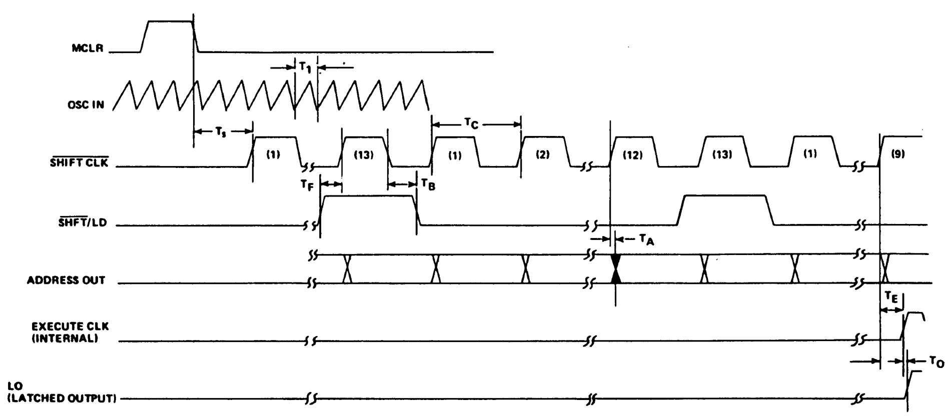


FIGURE 6. Timing Definitions

ADDRESS OUTPUT:
The twelve bit memory addresses are serially shifted out on this output line with the MSB being output first. Address bits change with the rising edge of the shift clock.

LATCHED OUTPUTS (LO):
The twelve latched outputs are driven from 12 flip-flops within the chip. The state of each of these flip-flops is directly under program control so that they can be manipulated according to the required application.

INSTRUCTION SET:
There are two classes of instructions in the LS7270 Controller/Sequencer. The first is the internal control group and the second is the logical operation group. Each is 16 bit in length.

INTERNAL CONTROL GROUP:

0 (1-bit)	OPER (3-bits)	CONSTANT OR ADDRESS (N) (12-bits)

15 0

Operation Code	MNEMONIC	OPERATION
000	NOP	No operation
001	LC1 DC1*	CNTR1 ← N (Load counter 1 with constant N)
010	LC2 DC2*	CNTR2 ← N (Load counter 2 with N)
011	LC3 DC3*	CNTR ← N (Load counter 3 with N)
100	LC4 DC4*	CNTR4 ← N (Load counter 4 with N)
101	J/RT	If N ≠ FFF (HEX), PC ← N (Jump to address N); If N = FFF, PC ← $Stack_0$, $Stack_{0,1}$ ← $Stack_{1,2}$ (Return from subroutine)
110	JS	$Stack_{1,2}$ ← $Stack_{0,1}$, $Stack_0$ ← PC, PC ← N (Jump to subroutine address N and save the return instruction address on the stack)

*If N=0, a load counter instruction is decoded as a decrement counter instruction thereby creating the DC1, DC2, DC3, DC4 instructions.

LOGICAL CONTROL GROUP:

1 (1)	OPER (3)	T/C (1)	ADDRESS,N (5)	TEMP (2)	SKIP/DISP. (4)

15 0

Input Mode

OPER FIELD	MNEMONIC	OPERATION
000	LD/LDC	AF ← (N)/AF ← $(\overline{N})$ Load AF with the true/complement of the value of register addressed by N.
001	AND/ANDC	AF ← AF∧(N)/AF ← AF∧ $(\overline{N})$ AND AF with true/complement value of register addressed by N.
010	OR/ORC	AF ← AF V (N)/AF ← AF V $(\overline{N})$ OR AF with true/complement value of register addressed by N.
011	XOR/XORC	AF ← AF⊕(N)/AF ← AF⊕ $(\overline{N})$ XOR AF with true/complement value of register address by N.

Output Mode

OPER FIELD	MNEMONIC	OPERATION
110	STR/STRC	(N) ← AF/(N) ← $\overline{AF}$ store true/complement value of AF into register addressed by N.
111	SET/CLR	If T/C=0 then (N) ← 1; If T/C=1 then (N) ← 0. Set or clear the register addressed by N.

T/C Field, True/Complement
0 – Select the true value of the addressed register.
1 – Select the complimented value of the addressed register.

ADDRESS, N FIELD – Input Mode Addressing Assignments
00000 to 01011 –Specify DI_1 to DI_{12} , respectively.
01100 to 01111 –Specify CNTR1 equal to zero flag through CNTR4 equal to zero flag,respectively.(see note 1)
10000 to 11011 –Specify M1 through M12 , respectively.
11100 to 11110 –Specify T1 through T3 , respectively.

ADDRESS, N Field – Output Mode Addressing Assignments
00000 to 01011 –Specifies LO1 through LO12 , respectively.
10000 to 11011 –Specifies M1 through M12 , respectively.

TEMP Field – Temporary Storage
00 – Do not store the output of the Logic Unit (LU)
01 – Store LU in T1
10 – Store LU in T2
11 – Store LU in T3

SKIP/DISP Field – Skip/Displacement Field
0000 – Continue to next instruction.
$n_3n_2n_1n_0$ – If the output of the LU is zero, then use $n_3n_2n_1n_0$ as 2's complement displacemnt to be added to the PC for forward and backward branching. $n_3n_2n_1n_0 = -7$ to $+7$.

Note 1: A counter zero flag is set to "1" when the corresponding counter is reset to "0".

MAXIMUM RATINGS:

Parameter	Symbol	Value	Unit
Storage Temperature	T_{STG}	−55 to +150	°C
Operating Temperature	T_A	0 to 70	°C
Voltage (any pin to V_{SS})	V_{max}	+15 to −0.3	V

DC Electrical Characteristics

($V_{SS} = 0$, $T_A = 0°C$ to $+70°C$, unless otherwise specified)

Parameter	V_{DD}	Symbol	Min.	Max.	Units	Conditions
Supply Voltage	–	V_{DD}	+4.75	+12	V	
Supply Current		I_{DD}	–	28	mA	All outputs open ckt.
Input High Vltg	+5V	V_{IH}	+3.0	V_{DD}	V	
	+9V		+37	V_{DD}	V	
	+12V		+4.7	V_{DD}	V	
Input Low Vltg	+5V	V_{IL}	0	+1.0	V	
	+9V		0	+1.5	V	
	+12V		0	+2.4	V	
Output High Vltg		V_{OH}	$V_{DD}-0.2$	–	V	@I_{OH}=20uA
Output Low Vltg	+5V	VOL	–	+0.6	V	@I_{OL}=2.5mA
			–	+0.4	V	@I_{OL}=1.6mA
	+9V		–	+0.6	V	@I_{OL}=6.2mA
			–	+0.4	V	@I_{OL}=4.1mA
	+12V		–	+0.6	V	@I_{OL}=12mA
		–		+0.4	V	@I_{OL}=8mA
Output Source Current	+5V	I_{source}	−770	–	μA	@V_{OH}=+2.0V
			−20	–	μA	@V_{OH}=+4.8V
	+9V		−640	–	μA	@V_{OH}=+6.0V
			−25	–	μA	@V_{OH}=+8.7V
	+12V		−1	–	mA	@V_{OH}=+8V
			−50	–	μA	@V_{OH}=11.5V
Output Sink Current	+5V	I_{sink}	+3.5	–	mA	@V_{OL}=+0.8V
			+2.5	–	mA	@V_{OL}=+0.6V
			+1.6	–	mA	@V_{OL}=+0.4V
	+9V		+8.3	–	mA	@V_{OL}=+0.8V
			+6.2	–	mA	@V_{OL}=+0.6V
			+4.1	–	mA	@V_{OL}=+0.4V
	+12V		+15	–	mA	@V_{OL}=+.8V
			+12	–	mA	@V_{OL}=+.6V
			+8	–	mA	@V_{OL}=+.4V
Input High Current		I_{INH}				
INST IN and MCLR			–	+4.8	μA	@$V_{IH}=V_{DD}-.5V$
All other Inputs			–	−1.0	μA	@$V_{IH}=V_{DD}-.5V$
Input Low Current		I_{INL}				
All Inputs			–	+1.9	μA	@V_{IL}=+0.2V

DYNAMIC ELECTRICAL CHARACTERISTICS

(V_{DD} = +4.75 to +12V, T_A = 0 to +70°C, unless otherwise specified; see Fig. 6)

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Osc. Frequency	f_{osc} (=1/T1)	–	–	2.0	MHz	
Reset Pulse width	T_{WR}	2.5	–	–	μs	
Reset to Shift Clock Delay	T_S	1.0	–	1.25	μs	@f_{osc}=2.0MHZ
Shift Clock Period	T_C(=4T1)	–	2.0	–	μs	@f_{osc}=2.0MHZ
Load Front Porch	T_F(=T1)	–	500		ns	@f_{osc}=2.0MHZ
Load Back Porch	T_B(=T1)	–	500	–	ns	@f_{osc}=2.0MHZ
Shift Clock To address out delay	T_A	30	–	80	ns	
Shift Clock To Execute Delay	$T_E(=T_1)$	–	500	–	ns	
Shift Clock To Output Delay	T_O	–	550	–	ns	
Counter Input frequency	f_{cnt}	–	–	100	KHz	
Counter Input pulse width:						
HI		2.0	–	–	μs	
LO		1.0	–	–	μs	

PROGRAM EXAMPLE

A simple example is given below to illustrate how the codes are constructed.

A momentary push-button switch, S is connected to the DI1 input of the ICS as shown in Fig. 7. It is required that every time S is pushed, the output LO1 will toggle (change state). Note that only the transition from the nondepressed to the depressed state should cause LO1 to toggle; if S is held depressed, it will have no further effect on the output.

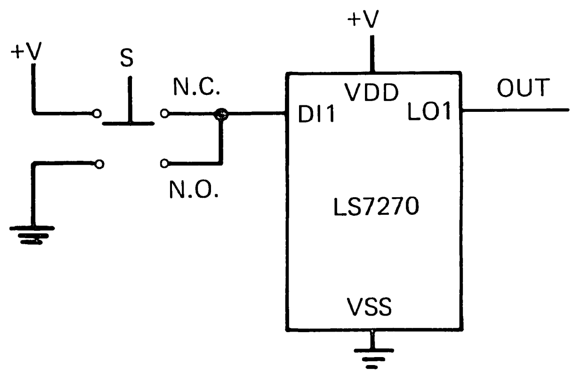


FIGURE 7

Let us assign ICS internal register M1 to store the status of S and M2 to store the status of the output latch LO1 during each sample cycle. A flow chart to describe the program steps is given in Fig 8. The program is in mnemonic code and its binary equivalent is given below.

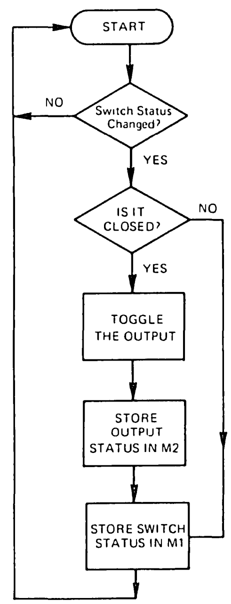


FIGURE 8

Mem. Address (Decimal)	Mnemonic	Binary	Comment
0	STRT: LD DI1, T2	0 0 1 0 0 0 0 0	Read status of S and
1		1 0 0 0 0 0 0 0	save it in T2.
2	XOR M2, −2	0 1 0 0 1 1 1 0	If S changed go to next step,
3		1 0 1 1 0 1 0 0	otherwise back to start.
4	LD T2	0 1 0 0 0 0 0 0	S changed; get ready to
5		1 0 0 0 0 1 1 1	test for open/close.
6	XOR T1, +1	0 0 0 0 0 0 0 1	Closed? If so, skip next step
7		1 0 1 1 0 1 1 1	
8	J UPDT	0 0 0 1 0 0 0 0	Not closed. Go to UPDT
9		0 1 0 1 0 0 0 0	routine to update M2
10	LD M1	0 0 0 0 0 0 0 0	S is closed; so get ready
11		1 0 0 0 0 1 0 0	to toggle.
12	STRC LO1	0 0 0 0 0 0 0 0	Toggled.
13		1 1 1 0 1 0 0 0	
14	STRC M1	0 0 0 0 0 0 0 0	Save current output
15		1 1 1 0 1 1 0 0	status in M1
16	UPDT: LD T2	0 1 0 0 0 0 0 0	Current status of S
17		1 0 0 0 0 1 1 1	
18	STR M2	0 1 0 0 0 0 0 0	Save stauts in M2
19		1 1 1 0 0 1 0 0	
20	J STRT	0 0 0 0 0 0 0 0	Start new sample cycle
21		0 1 0 1 0 0 0 0	

Note here that memory addresses for successive instructions have incremental value of 2. This is because each memory location can only hold a single byte (8 bits), whereas, an instruction consists of 2 bytes. The low byte of the first instruction is stored at address 0 and the high byte at address 1. The low byte of the second instruction at address 2 and the high byte at address 3 and so on.

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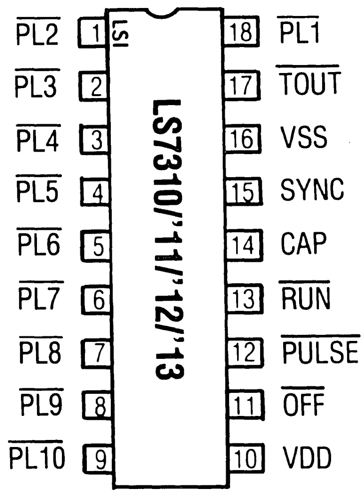
LSI/CSI

LS7310 — LS7313

REV. JANUARY 1988

AC POWER CONTROLLERS

CONNECTION DIAGRAM — TOP VIEW
STANDARD 18 PIN PLASTIC DIP



FEATURES:

- Phase-locked-loop (PLL) synchronization produces pure a-c across the output load (no d-c offset)
- 10 levels of output power ranging from 37% to 97% of rated load wattage
- Controls output power by controlling the a-c Duty Cycle
- Operates on 50Hz/60Hz line frequency for PLL synchronization
- 10V to 14V supply voltage
- 10 I/O's for touch or mechanical switch inputs for power selection and LED driver outputs to indicate selected power
- Speed controller for universal and shaded pole motors

GENERAL DESCRIPTION:

LS7310-LS7313 are specifically designed for appliance power control such as blenders, vacuum cleaners, mixers, etc. I/O's are provided for selecting and indicating 10 power levels, which generally exceed the requirements of most appliances. If, however, the inputs are not fully utilized, only the desired power level inputs/outputs (PL — I/O's) may be hooked up for any specific appliance application.

The LS7310 and LS7311 are designed for external mechanical switch control. The LS7312 and LS7313 are designed for external touch control.

A logic 0 level applied to $\overline{\text{PL}}$ input in excess of T_H (see dynamic characteristics), selects the power level associated with that $\overline{\text{PL}}$ input. $\overline{\text{TOUT}}$ is turned on when the power level selection is followed by the application of either $\overline{\text{RUN}}$ or $\overline{\text{PULSE}}$ input. The $\overline{\text{TOUT}}$ is a negative pulse occuring every half-cycle of the SYNC input with a phase angle that is specific to the selected $\overline{\text{PL}}$ I/O. The $\overline{\text{TOUT}}$ is designed to drive a triac in series with the load to control the a-c duty cycle through the load.

A $\overline{\text{PL}}$ input, when selected as described above, switches its status from being an input to an output. As an output, the $\overline{\text{PL}}$ is designed to drive an LED to indicate the selected power level. The active $\overline{\text{PL}}$ output switches back to the input state, only when a different $\overline{\text{PL}}$ input is selected, the output status now being transferred to the new $\overline{\text{PL}}$ I/O.

I/O DESCRIPTIONS:

$\overline{\text{PL1}}$ — $\overline{\text{PL10}}$ (Inputs/Outputs) 10 inputs/outputs for selecting 10 output phase angles (power levels). When no power level is selected (such as after system power-up), $\overline{\text{PL1}}$ — $\overline{\text{PL10}}$ all act as inputs. When a power level is selected by applying a logical zero at one of these inputs in excess of T_H (see dynamic characteristics), the selected input switches status to become an output in order to drive a display such as an LED. It switches back to the input state only when another $\overline{\text{PL}}$ input is activated. LS7310 and LS7311 have internal pullups of about 100K ohms. LS7312/LS7313 do not have any internal pullups.

RUN (Input) When a logical 0 is applied to the $\overline{\text{RUN}}$ input in excess of T_H, the output ($\overline{\text{TOUT}}$) is turned on at a phase angle selected earlier by one of the $\overline{\text{PL}}$ I/O's. If no power level was selected prior to the application of the RUN input, the circuit remains unaffected. Note that once the $\overline{\text{TOUT}}$ has been enabled, its phase angle can be altered by applying any other $\overline{\text{PL}}$ input without the need to apply the $\overline{\text{RUN}}$ input again. LS7310/LS7311 have 100K Ohm internal pullup on this input. LS7312/LS7313 do not have pullups.

$\overline{\text{OFF}}$ (Input) When a logical zero level is applied to this input in excess of T_H, $\overline{\text{TOUT}}$ is turned off if it was on. If $\overline{\text{TOUT}}$ was already off, the circuit remains unaffected. Note that $\overline{\text{OFF}}$ input does not alter the power level selected by a $\overline{\text{PL}}$ input. Following an $\overline{\text{OFF}}$ operation, $\overline{\text{TOUT}}$ can be turned on at the previous phase angle by applying the $\overline{\text{RUN}}$ input. LS7310/LS7311 have 100K Ohm internal pullups. LS7312/LS7313 do not have pullups.

$\overline{\text{PULSE}}$ (Input) A logical zero level applied to this input turns the $\overline{\text{TOUT}}$ on for as long as the $\overline{\text{PULSE}}$ input is maintained. The $\overline{\text{PULSE}}$ input, however, has no effect if no power level is in selection or if the $\overline{\text{TOUT}}$ has already been turned on by means of the $\overline{\text{RUN}}$ input. LS7310/LS7311 have 100K Ohm pullups. LS7312/LS7313 do not have pullups.

SYNC (Input) Input for PLL reference frequency (50 Hz/60 Hz). All internal clock frequencies are synchronized with the SYNC input.

CAP (Input) Input for external component connection. A capacitor of 0.047μF $\pm$ 20% should be used on this input as shown in the application example (Figure 4).

$\overline{\text{TOUT}}$ (Output) Triac output. This output is designed to drive a triac in series with load and control its firing angle with respect to the a-c.

The LS7310 and LS7312 provide a nominal 33 microsecond output pulse width. Since some motors have large inductive loads producing a large phase delay between voltage and current, a wider output pulse may be required. The LS7311 and LS7313 produce a 1.0 millisecond output pulse width. Otherwise, these parts are identical to the LS7310 and LS7312 respectively.

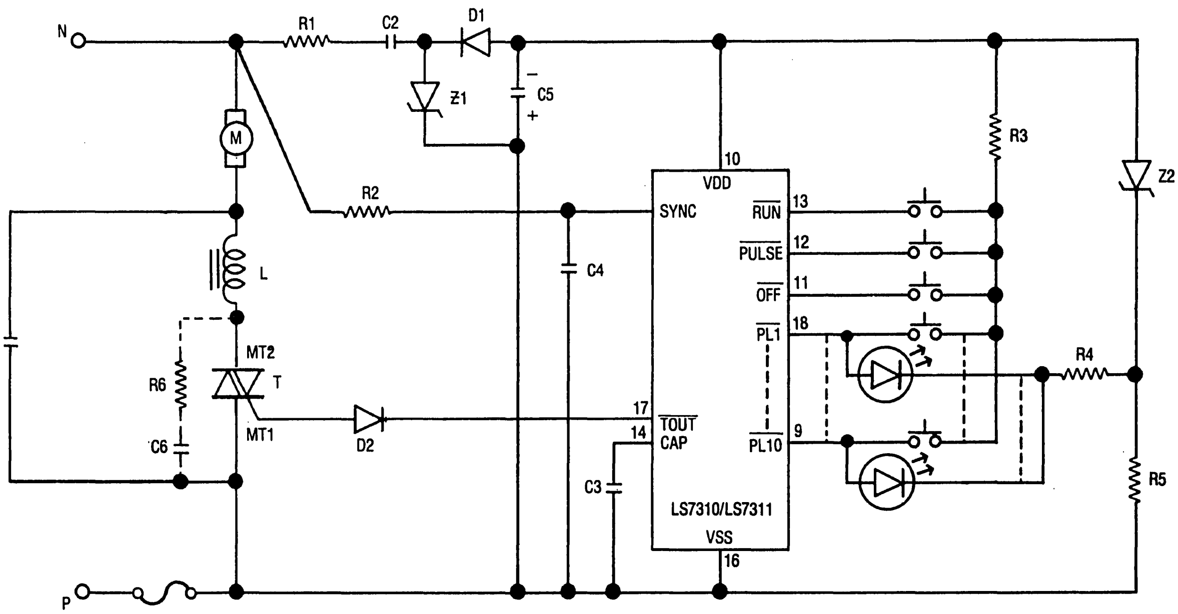
VSS Positive supply terminal.

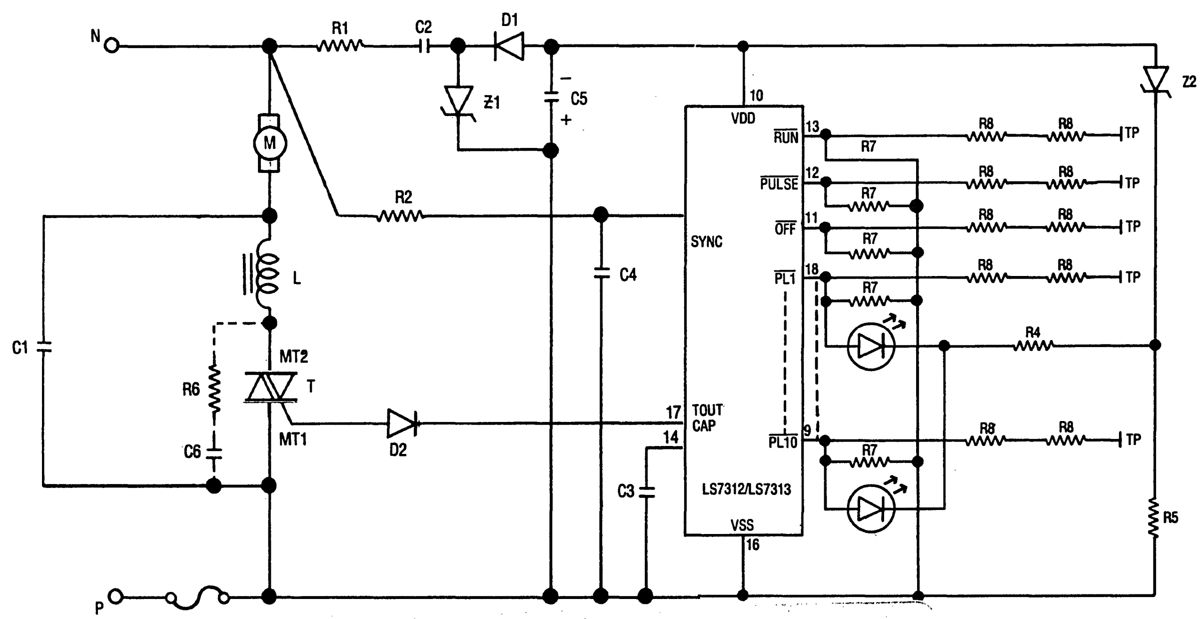
VDD Negative supply terminal.

TABLE 1. OUTPUT CONDUCTION ANGLE*

POWER LEVEL INPUT	$\overline{\text{TOUT}}$, CONDUCTION ANGLE, Ø (DEGREES)	$\frac{\text{OUTPUT POWER}}{\text{RATED POWER}}$ X 100%
PL1	78	37
PL2	86	46
PL3	93	53
PL4	100	60
PL5	107	69
PL6	112	74
PL7	119	79
PL8	127	86
PL9	137	92
PL10	149	97

***Mask Programmable**





*All unused touch inputs must be tied together and brought to VSS through a 100K, ¼W resistor.

115 VAC

C1 = 0.15μF/250 VAC
C2 = 0.68μF/250 VAC
C3 = 0.047μF/25 VDC
C4 = 470pF/25 VAC
C5 = 220μF/25 VDC
**C6 = .047μF/250 VAC
R1 = 270 ohms/2W
R2 = 1.5M ohms/ 1/4W
R3 = 3.3KΩ/ 1/4W
R4 = 390Ω/ 1/4W
R5 = 10KΩ/ 1/4W
**R6 = 1.8KΩ/ 1W
R7 = 1MΩ to 5MΩ/ 1/4W (Select For Sensitivity)
R8 = 2.7MΩ/ 1/4W
Z1 = 13V/1W Zener (±5%)
*Z2 = 6.2 V/ 1/4W Zener (±5%)
D1, D2 = 1N4148
T = L2006L7
L = 100 μH (Rfi Filter)

220 VAC

C1 = 0.15μF/400 VAC
C2 = 0.68μF/400 VAC
C3 = 0.047μF/25 VDC
C4 = 470pF/25 VAC
C5 = 220μF/25 VDC
**C6 = .047μF/400 VAC
R1 = 1KΩ/1W
R2 = 1.5MΩ/ 1/4W
R3 = 3.3KΩ/ 1/4W
R4 = 390Ω/ 1/4W
R5 = 10KΩ/ 1/4W
**R6 = 1.8KΩ/ 2W
R7 = 1MΩ to 5MΩ/ 1/4W
R8 = 4.7 MΩ/ 1/4W
Z1 = 13V/1W Zener (±5%)
*Z2 = 6.2V/ 1/4W Zener (±5%)
D1, D2 = 1N4148
T = L4006L7
L = 100 μH (Rfi Filter)

*Zener type should be that which produces its rated voltage at 500 microamperes or less such as part type MZ4627.
**R6-C6 network may be required for some motor inductive loads. Note: Use LEDs requiring 5 mA or less.

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ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
DC supply voltage	VSS	+20	Volt
Any input voltage	Vin	VSS +.5	Volt
Operating temperature	T_A	0 to +80	°C
Storage temperature	Tstg	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS: (All voltages referenced to VDD)
(T_A = 0 to 80°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Supply voltage	VSS	+10	+12	+14	Volts	—
Supply current	Idd	—	1.2	2	mA	@ VSS = + 12V, All Outputs Off
Input voltages:						
Sync, lo	V_{SYL}	0	—	1/3 VSS	Volts	
Sync, hi	V_{SYH}	2/3 VSS	—	VSS	Volts	
All other inputs, lo	V_{IL}	0	—	1/4 VSS	Volts	
All other inputs, hi	V_{IH}	1/2 VSS	—	VSS	Volts	
Input currents:						
Sync Input	I_{IH}			110	μA	With Series 1.5MΩ Resistor to 115 Vac Line
Input Pull Up Resistance For LS7310, LS7311 $\overline{\text{PL1}}$ — $\overline{\text{PL10}}$	R_{IN}	50	100	200	KΩ	
Output voltages:						
$\overline{\text{TOUT}}$, hi	V_{OTH}	—	0	—	Volts	
$\overline{\text{TOUT}}$, lo	V_{OTL}	—	VSS-4	—	Volts	
Output currents:						
$\overline{\text{TOUT}}$ Sink	I_{OT}	20		—	mA	@ VSS = +12V V_{OTL} = VSS —3 Volts
	I_{OT}	25			mA	@ VSS = +12V V_{OTL} = VSS - 2 Volts
$\overline{\text{PL}}$ Source	I_{OP}	5		—	mA	V_{OPL} = VSS -1 Volts

DYNAMIC CHARACTERISTICS:

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Sync frequency	f_S	40	—	70	Hz	—
$\overline{\text{PL}}$/$\overline{\text{RUN}}$/$\overline{\text{PULSE}}$/$\overline{\text{OFF}}$ hold time	T_H	34	—	infinite	ms	@ 60 Hz Sync
	T_H	40	—	infinite	ms	@ 50 Hz Sync
$\overline{\text{TOUT}}$ pulse width (7310/12)	T_W	—	33	—	μs	@ 60Hz Sync
	T_W	—	39	—	μs	@ 50Hz Sync
$\overline{\text{TOUT}}$ pulse width (7311/13)	T_W	—	1.0	—	ms	@ 50/60Hz Sync

FIGURE 2 — OUTPUT PHASE ANGLE ϕ

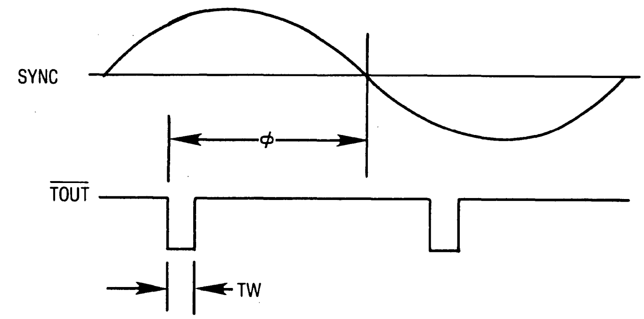
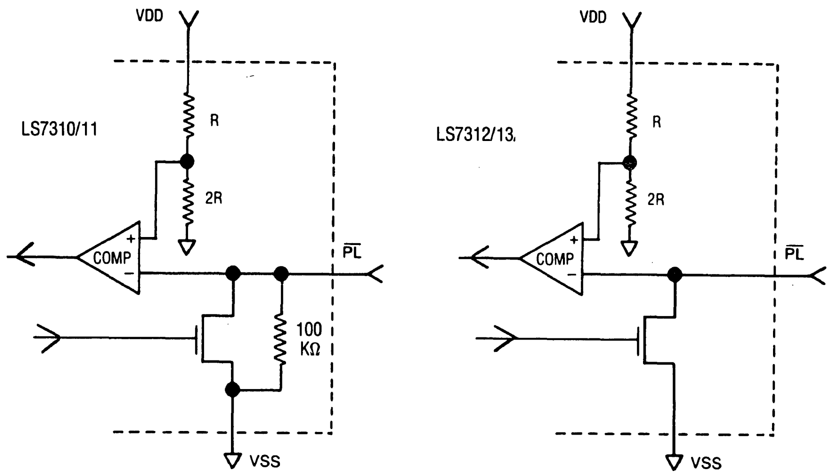


FIGURE 3
$\overline{PL}$ INPUT/OUTPUT CIRCUIT



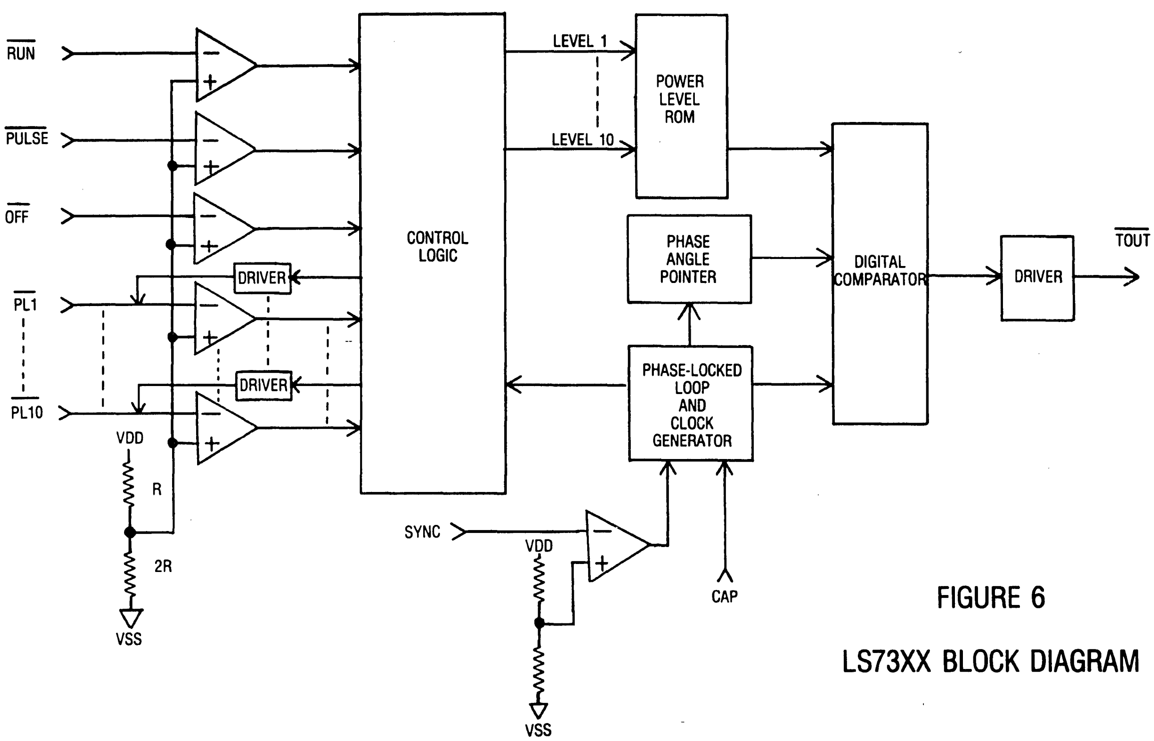


FIGURE 6

LS73XX BLOCK DIAGRAM

LSI/CSI

LS7501
LS7510

TONE ACTIVATED LINE ISOLATION DEVICE

FEATURES:
- Low power CMOS design
- On chip oscillator (32,768HZ external crystal required)
- Tone input can be low level sinusoid (as low as — 30 DBM) or fully digital.
- Mask programmable available frequencies: 11 HZ to 4095 HZ (in 1 HZ steps)
- Sample interval -4.5 seconds (Mask programmable 0.5 to 8.0 seconds).

DESCRIPTION
The LS7501 — LS7510 are frequency discriminator circuits that respond to a standard frequency input if the input is maintained within ± 10HZ during a 4.5 second continuous sample interval. During this interval, the input is being sampled every 0.5 seconds. If it is valid for the sample interval, then the circuit can be used to pulse a relay that disconnects the line to be tested. After 20 seconds of disconnect time, the relay is reset and the line is restored. There are ten standard frequency versions of this circuit. These are indicated in table 1 with their associated input discriminator frequencies.

CONNECTION DIAGRAM: TOP VIEW
STANDARD 16 PIN PLASTIC DIP

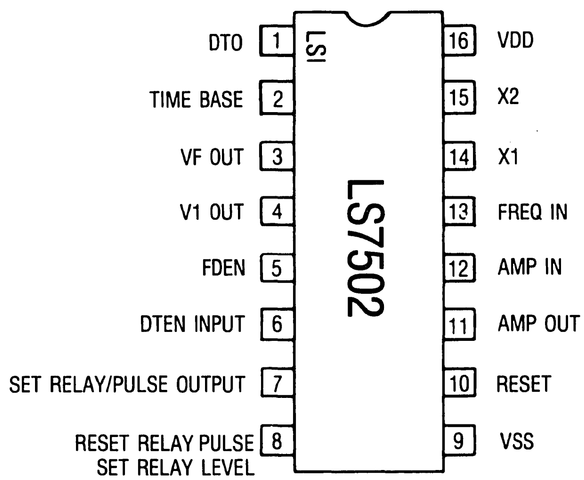


FIGURE 1

TABLE 1

PART NO.	FREQUENCY (HZ)
LS7501	2683
LS7502	2713
LS7503	2743
LS7504	2773
LS7505	2833
LS7506	2863
LS7507	2893
LS7508	2923
LS7509	2953
LS7510	2983

DETAILED DESCRIPTION

A. Input Amplifier:
The amplifier has a minimum gain of 40. The input should be a.c. coupled.

B. Frequency Discriminator:
The frequency input can be a digital source or the output of the amplifier. The input is sampled for a 1/2 second interval and if a proper frequency is present, the VF output goes high.

C. The sample interval timer is enabled when a valid frequency is detected. The purpose of the timer is to insure that the input frequency is continuous for a period of 4.5 seconds ± 125ms. If the applied input frequency is interrupted during the detection period, the timer is reset and a new detection interval is started. At the end of a valid sample period, a 125ms pulse is generated at VI.

D. Disconnect Timer:
Enabled by a positive edge on the DTEN input and clocked at a 2Hz rate, this timer determines the disconnect time. (20 ± .5 seconds). On timeout, a positive pulse is generated on DTO.

E. Clock Generator:
A 32,768 Hz crystal oscillator and a chain of binary dividers provide all the timing signals.

TABLE 2. INPUT, OUTPUT DESCRIPTION		
PIN	FUNCTION	DESCRIPTION
1	DTO	Disconnect timer time out. Active high pulse generated at the end of disconnect time (20 sec); normally connected to Pin 5.
2	TIME BASE	Output clock 32,768 HZ or 8 HZ (Mask Programmable)
3	VF OUT	Valid frequency. Active high when input frequency is 2713 ± 10 HZ (LS7502).
4	VI OUT	125 MS Active high pulse output generated when an input frequency has been valid for the duration of the sample interval (4.5 seconds).
5	FDEN	Frequency detector enable (Positive edge triggered)
6	DTEN INPUT	Disconnect timer enable (Positive edge triggered) normally connected to VI out. It also disables frequency detection.
7	SET RELAY/ PULSE OUTPUT	3.9 ms active high pulse generated when a valid frequency has been present for 4.5 seconds.
8	RESET RELAY PULSE/ SET RELAY LEVEL	3.9 ms active high pulse generated when the disconnect timer times out or a high level that lasts for the duration of the 20 second time out. (Mask programmable). If the reset relay option is active, a pulse is generated on the RESET RELAY Output at power-up.
9	VSS	Ground
10	RESET	External reset. An active high pulse will reset circuit (Internal pull down).
11	AMP OUT	Amplified Tone. Usually connected to the FREQ pin.
12	AMP IN	Tone input for low level (to — 30 DBM) sinusoid.
13	FREQ IN	Digital tone input.
14	X1	Crystal
15	X2	Crystal
16	VDD	Positive Supply

Maximum Ratings: (Voltages referenced to VSS)

RATING	SYMBOL	VALUE	UNIT
DC supply voltage	VDD	+2.5 to +6.0	Vdc
Operating temperature range	TA	-25 to +70	°C
Storage temperature range	TSTG	-65 to +150	°C

DC Electrical Characteristics:
(VSS = 0V, VDD = +2.5 to +6.0V, -25°C TA +70°C unless otherwise specified)

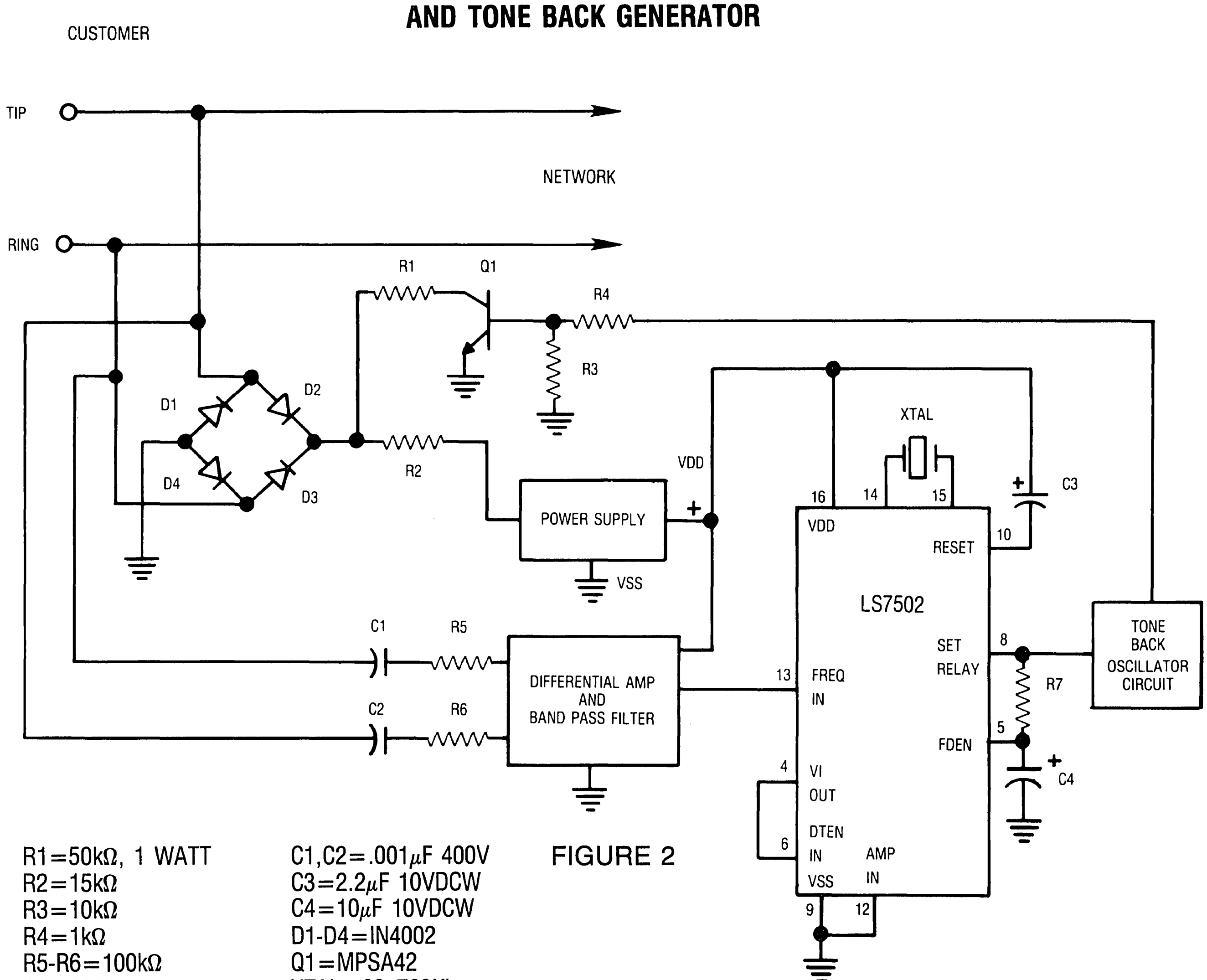
PARAMETER	CONDITIONS	VDD	MIN	MAX	UNITS
Output Source Current	V_0 = 0.7V	2.5V	100	—	μA
	V_0 = 0.7V	5.0V	1.0	—	ma
Output Sink Current	V_0 = 0.25V	2.5V	350	—	μA
	V_0 = 0.25V	5.0V	900		μA
Input Specifications (All Inputs)					
Vi_L (MAX)		2.5V	—	0.75	Volts
		5.0V	—	1.50	Volts
Vi_H (MIN)		2.5V	1.75	—	Volts
		5.0V	3.50	—	Volts
Noise Margins:		2.5 to 5.0V	1.0	—	Volts
Quiescent Device Current:		2.5V	—	20	μA

Note: Reset Input Contains Internal 100KΩ Pulldown.

A.C. Specifications (All Outputs)

PARAMETER	CONDITIONS	VDD	MIN	MAX	UNITS
T_{RISE}, T_{FALL}	CL = 50pf	5.0V	—	1.0	μsec

TELEPHONE LINE INTERROGATOR AND TONE BACK GENERATOR



R1=50kΩ, 1 WATT
R2=15kΩ
R3=10kΩ
R4=1kΩ
R5-R6=100kΩ
R7=200kΩ

C1,C2=.001μF 400V
C3=2.2μF 10VDCW
C4=10μF 10VDCW
D1-D4=IN4002
Q1=MPSA42
XTAL=32•768Khz

FIGURE 2

DESCRIPTION

This application indicates a method for interrogating a telephone line when a 2713Hz (±10Hz) tone is detected for a minimum of 4.5 seconds. (The LS7502 Circuit.)

At the end of the 4.5 second sample period, an oscillator is energized and generates a tone back signal. This signal modulates the line at a voice level of -16DB or 3.5MV peak to peak.

Typical system input activation sensitivity is -30DBM. The unit should also be operational down to 6 volts at the tip/ring network terminals.

As shown in Figure 2, the differential op-amp is connected to the telephone lines through .001μF coupling capacitors. This eliminates the D.C. component and acts as the first filter for 60Hz. The differential amplifier stage is followed by a band pass filter centered around 2713Hz. This filter should be designed for high Q's (Q = 10) and yet utilize current efficient op-amps.

The band pass output is then squared up and connected to the digital tone input (Pin 13). The input signal, is sampled by the digital discrimination section of the LS7502. If 2713Hz (±10Hz) is present for 4.5 seconds, a 125 millisecond pulse at Pin 4 is applied to the DTEN input (Pin 6), causing an internal flip-flop to set an the set relay output (Pin 8) to go high, activating the tone back oscillator.

As the 10μF capacitor (C_4) builds up stored charge, it biases the FDEN input (Pin 5) through R_7 until it is sufficient to reset the internal flip-flop and bring the circuit back to its idle state and turn the tone back oscillator off. By varying the R_7-C_4 network, the time constant for the tone back duration can be varied.

CIRCUIT BLOCK DIAGRAM

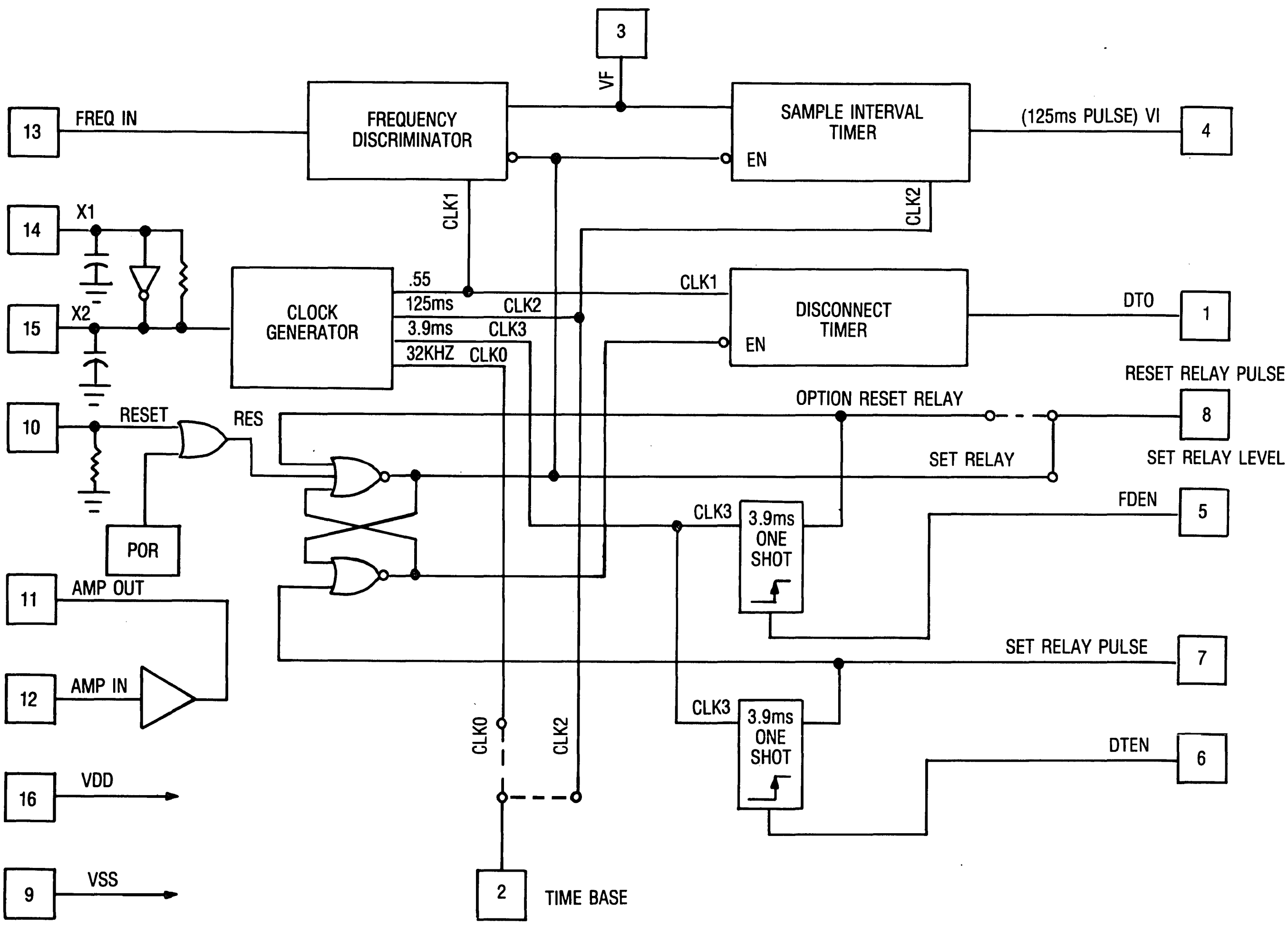


FIGURE 3

NOTE (1) All devices shown on the LS7501 through the LS7510 are configured with the set relay outpout on Pin 8. The reset option can be substituted by optional mask change.

NOTE (2) All devices shown with the exception of the LS7502 are configured with the clock-0, 32KHz output on Pin 2. The LS7502 is configured with the clock-2 time base output of 8Hz. These outputs may be changed with the same optional mask change referred to in Note 1.

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LSI/CSI

APPLICATION NOTE 101

THREE AND FOUR PHASE BRUSHLESS DC MOTOR CONTROLLERS USING PULSE-WIDTH MODULATION

ABSTRACT

This paper describes the five motor circuits which drive brushless DC Motor controllers and are available as standard products from LSI COMPUTER SYSTEMS, INC. The theory of operation of each of the circuits is explained, accompanied by circuit block diagrams. Numerous applications are illustrated and interface circuits for driving high voltage motor windings using bipolar and MOS power transistors are indicated. The first of these five is the LS7261, which is an open or closed loop commutator sequencer. It operates at 7 to 28 volts and has externally selectable input and output codes for 60°, 120°, 240° and 300° electrical sensor spacing. It has a pulse width modulation for analog speed control and forward/reverse inputs. In addition, this circuit contains positive static braking, overcurrent input, and an output enable control. There are 6 outputs for driving 3 phase or 4 phase motors.

Whereas in the LS7261 the overcurrent causes the outputs to switch on and off directly from the overcurrent sense input, the LS7260 and LS7262 circuitry causes the outputs to switch off immediately upon sensing the overcurrent condition. It only switches back on at a rate determined by the pulse width modulation chopping rate.

The LS7263 is a highly accurate speed regulator operating at 10 to 28V and designed to control the speed of a 3-phase brushless DC motor. The specific circuit is programmed for 3600 RPM applications using a 3.58 MHZ crystal. Other speeds can be controlled by changing the crystal frequency or by having the circuit reprogrammed by the company. It is presently available for 4 or 8 pole motors and 60° and 120° sensor separation.

The LS7264 is basically the same as the LS7263 except that it was designed for the 4-phase brushless DC motor.

BRUSHLESS DC MOTOR COMMUTATOR

The advent of brushless DC motors has brought with it the need to integrate its unique circuit control requirements into a flexible, low cost integrated circuit. The ideal circuit should be able to commutate 3 and 4 phase motors. It should have some means of controlling the speed of the motor. It should also have overcurrent protection circuitry, a brake input, a forward/reverse input, and be able to accommodate different electrical sensor spacings.

The heart of the LS7261 and the LS7262 commutator circuit is the decoder which senses the Hall effect inputs and creates the proper turn-on sequence of the output devices which are used to drive the motor. In addition, these circuits are able to commutate properly whether the Hall switches are separated electrically by 60°, 120°, 240°, or 300°. Figure 1 illustrates the commutator circuit block diagram. CS1 and CS2 inputs are used to select the proper decode mode depending on the Hall electrical separations. S_1, S_2, and S_3 designate the Hall inputs. Also indicated are the forward/reverse inputs, the enable input, the brake input, the common input and the output drivers. The speed of the motor can be controlled by the saw tooth oscillator circuitry. The external R-C network was chosen to set the oscillator at approximately 30KHz. The oscillator will ramp within the power supply rails as shown. By adjusting V_{TRIP} to the desired voltage, the comparator output duty cycle can be adjusted to be between 0 and 100%. This output is then applied to the output driver circuitry and causes the outputs to be chopped at the oscillator frequency. Varying the duty cycle will result in output drive signals that can vary from full off to full on or to any level in between.

The LS7260 and LS7262 incorporates a flip flop as part of the overcurrent protection circuitry. An overcurrent condition generates a voltage greater than V_{REF} and resets the flip-flop which disables the output drivers through the And gate. When the overcurrent condition terminates, the next positive

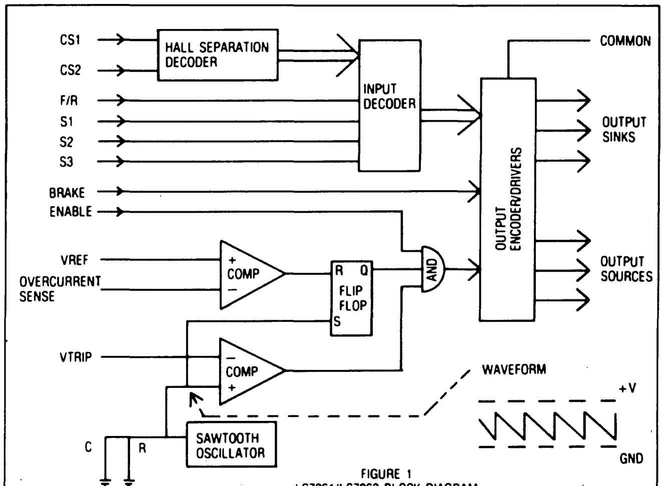


FIGURE 1
LS7261/LS7262 BLOCK DIAGRAM

saw-tooth oscillation edge will enable the drivers again. The ensuing result of this circuit is to limit the maximum switching rate of the output drivers to the chopping frequency. The LS7261 does not have this flip flop. The overcurrent sense comparator drives the And gate directly. In this case, the motor and driver circuit time constants will determine the maximum output driver switching rate.

USing the LS7261/LS7262 for three phase push-pull operation, the output driver circuitry consists of six MOS transistors with a common terminal. The output circuit driving a delta configured motor is shown in Figure 2, while a center tapped single ended driver circuit is illustrated in Figure 3. Pin numbers are included for reference. The sequencer logic causes the external driver transistors to turn on in the correct timing relationship. Referring to Figure 2, it can be seen that in order to drive the motor windings, the external transistors must turn on in pairs. For example, to drive winding L_1, PNP Transistor Q_1 and NPN transistor Q_5 must turn on simultaneously or PNP Q_2 and NPN Q_4 must turn on simultaneously. These transistors are turned on by enabling internal MOS driver transistors. Turning on transistors Q_2 and Q_5 require Q_A and Q_E to turn on. By driving the gates of MOS transistors Q_A and Q_E negative, current is forced to flow through the bases of Q_1 and Q_5. Output 1 (0_1) sinks current and output 5 (0_5) sources current. Similarly, enabling Q_B and Q_D causes current to flow through the bases of Q_2 and Q_4.

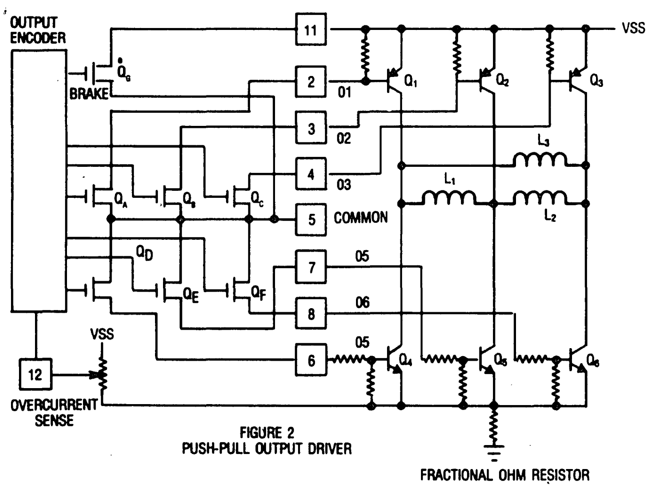


FIGURE 2
PUSH-PULL OUTPUT DRIVER

Using the LS7261/LS7262, the overcurrent circuit indicated in Figure 2 consists of a potentiometer and a fractional ohm resistor. The potentiometer is adjusted until all outputs are disabled for currents greater than the desired limit. During the overcurrent condition, all the MOS driver transistors are cut off which causes the bipolar driver transistors to disable. If a brake signal is applied, then the common terminal is forced to the positive supply voltage, VSS. Since Q_A, Q_B and Q_C are turned on, 0_1, 0_2, and 0_3 are driven to the positive supply voltage cutting off external transistors Q_1, Q_2 and Q_3. In addition, internal transistors Q_D, Q_E and Q_F are turned on which causes Q_4, Q_5 and Q_6 to turn on shorting the motor windings together and stopping the motor. The brake signal always overrides the overcurrent sense input.

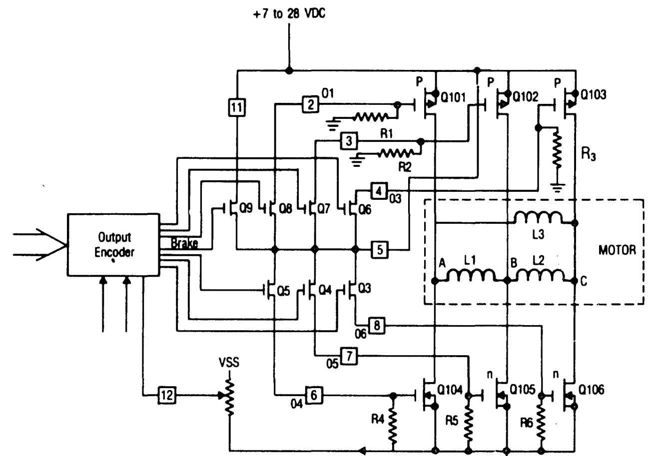


FIGURE 2A
PUSH-PULL OUTPUT DRIVER

Figure 2A indicates a similar circuit using the LS7060 for driving P Channel and N Channel FETS and developing a full 12 volt drive for the N Channel and P Channel FETS when using a 12 volt supply. In this configuration, the appropriate bottom N Channel transistor turns on while the upper P Channel transistor turns off. To turn, winding L_1 on, Q_8 of the LS7260 turns off, allowing the external resistor R_1 to force the gate of Q_{101} to ground. Since the source of Q_{101} is tied to +12 volts, the gate drive on Q_{101} is -12 volts. Internal transistor Q_4 is turned on and since Pin 5 of the LS7260 is tied to +12 volts, the gate drive of Q_{105} becomes +12 volts. Current is forced through L_1 from Q_{101} to Q_{105}. Similar current is reversed through L_1 when P Channel FET Q_{102} turns on and N Channel FET Q_{104} turns on. The overcurrent sense circuitry performs in exactly the same manner as the LS7262 does when driving bipolar transistors. The overcurrent donditions causes internal transistors Q_3, Q_4 and Q_5 to cut off and Q_6, Q_7 and Q_8 to turn on. This causes the external power FETS to turn off. Applying the brake signal causes internal transistors Q_6, Q_7 and Q_8 to turn on cutting off the external P Channel power FETS and causes internal transistors Q_3, Q_4 and Q_5 to turn on which, in turn, turn on the external N Channel power FETS. This causes the Motor windings to short together stopping the motor. As in the LS7262, the brake signal always overrides the overcurrent sense input.

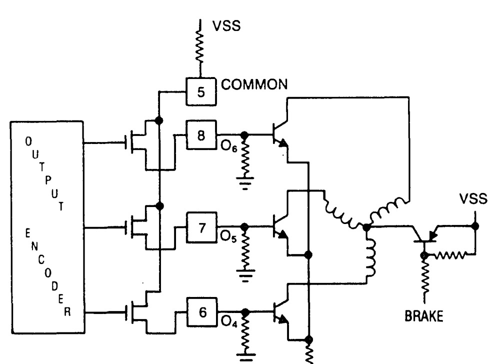
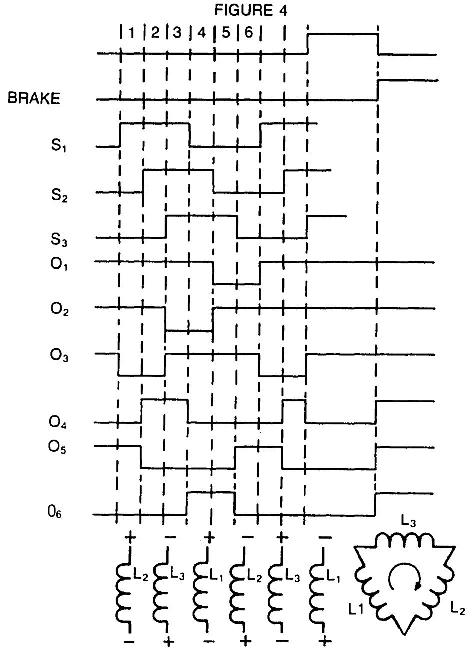


FIGURE 3
SINGLE ENDED OUTPUT DRIVER

Figure 3 illustrates a much simpler set up using single ended drivers. Q_4, Q_5, and Q_6 will turn on sequentially as before. Only one base current limiting resistor is required and this is in series with the common terminal that is connected to the supply voltage. Applying the brake to this circuit causes all the output transistors to turn on and the motor power supply to disconnect which causes the motor windings to short together.

FIGURE 4



COMMUTATION SEQUENCE FOR 60° SENSOR ELECTRICAL SEPARATION

Figure 4 indicates the output commutation sequence for sense inputs which are 60° electrically separated and for the forward/reverse input equal to a logic 1. The motor is assumed to be wound in a delta configuration and clockwise is assumed to indicate a positive voltage. The circuit is assumed to be configured as in Figure 2. When S_1 is high and S_2 and S_3 are low, O_3 becomes negative and O_5 becomes positive turnings on winding L_2 as shown. This is commutation State 1 as shown on Figure 4. The next commutation State 2 occurs when S_1 and S_2 are high and S_3 is low. In this case, O_3 becomes negative and O_5 becomes positive turning on winding L_2 as shown. This is commutation State 1 as shown on Figure 4. The next commutation State 2 occurs when S_1 and S_2 are high and S_3 is low. In this case, O_3 remains negative and O_4 becomes positive causing winding L_3 to turn on as shown. The rest of the sequence is indicated in Figure 4 and will repeat every rotation of 360° electrical degrees. The overcurrent condition causes O_1, O_2 and O_3 to become high and O_4, O_5 and O_6 to become low. As stated previously, this causes all of the output bipolar transistors to cut off. Also is indicated previously, the brake input causes all the outputs to go high shorting the motor windings together.

The LS7261 or LS7262 can also interface with four phase motors by connecting inputs CS_1 and CS_2 low and connecting Hall sense inputs S_2 and S_3 together. Four phase operation is indicated by Table 1.

S_1	S_2, S_3	Forward/Reverse = 1	Forward/Reverse = 0
0	0	O_1	O_4
1	0	O_3	O_6
1	1	O_4	O_1
0	0	O_6	O_3

TABLE 1 — FOUR PHASE COMMUTATION

The four phase motor uses two Hall sensors 90° electrically apart. The Hall inputs create four outputs turning on successively as indicated in Table 1. For single ended drive with center tapped windings, the circuit common is tied to the positive supply through a base limiting resistor and outputs O_1, O_3, O_4 and O_6 drive transistors whose collectors are tied to the four coil windings of a four phase motor and whose center tap is tied to the motor supply.

Circuit driving FETS can be used for the LS7261 or LS7262. A closed loop operation block diagram is depicted in Figure 5. Either one, two or three Hall sense inputs can be used as inputs to the negative edge detector. If two sense inputs are used, they are applied to an exclusive-OR gate whose output drives the negative edge detector. Three sense inputs require two exclusive-OR gates. The use of two or three inputs will increase the loop gain of the feedback loop since the number of pulses appearing at the output of the negative edge detector will double or triple. In Figure 5, one Hall sense input (S_1) is depicted. The output of the negative edge detector is applied to the integrator and consists of pulses whose width is constant but where the separation between pulses is a function of motor speed. The integrator produces a negative D.C. voltage whose value depends on the separation of pulses. If the motor speed increases, pulse separation decreases causing the output of the integrator to become more negative and the output of the operational amplifier to increase. This raises the V_{TRIP} input to the LS7261/LS7262 and lowers the duty cycle of the output driver circuitry. The lower duty cycle will cause the motor speed to decrease. Similarly, a decrease in motor speed causes the pulse separation to widen resulting in a decrease of voltage at the V_{TRIP} input which raises the output driver duty cycle and the resultant motor speed. The desired speed is set by varying the voltage at the positive input terminal of the Op-Amp which adjusts the nominal V_{TRIP} input.

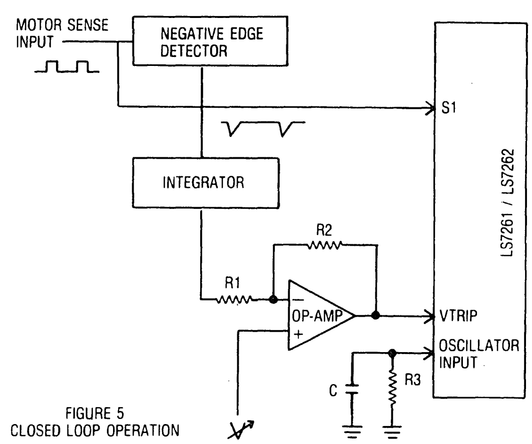


FIGURE 5
CLOSED LOOP OPERATION

The push-pull stage operates by using a P Channel power fet to drive the motor winding to the motor supply and an N Channel power fet to drive the motor winding to ground. With Pin 5 of the LS7261/LS7262 tied to VSS, a positive output at Pin 6 turns on emitter follower Q_6 and the N Channel fet. When the output at Pin 6 returns to zero, resistor R_7 removes the charge on the gate of N Channel transistor Q_5 rapidly cutting the transistor off. A positive output out of Pin 2 turns Q_1, level converter Q_2 and Q_3 off enabling the zener diode to develop the gate drive for the P Channel fet. When the output at Pin 2 returns to zero, Q_1 turns on providing current for Q_2 which turns on Q_3 rapidly shorting out the Zener diode and removing the drive on the gate of the P Channel power fet. This circuit is still not very efficient as it dissipates power in R_4 when Q_4 is off and R_6 when Q_4 is on. A more efficient power fet circuit utilizes identical N Channel power fets in a push-pull configuration. In order to achieve this, an external supply must be developed for driving the gate of the upper N Channel power fet above the motor power supply voltage. A complete working circuit utilizing Siemens BUZ73 power fets operating a 150 volt 3 phase brushless D.C. motor is depicted in Figures 10 and 11. Figure 10 illustrates the power supply used for generating the upper N Channel gate drive. The 555 oscillator provides a square wave which is A-C coupled to a diode network that is referenced to 150 volts by the upper IN4004. The lower IN4004 rectifies the 12 volt peak-to-peak square wave producing approximately 162 volt D.C. at point G. This becomes the gate drive of the upper N-Channel power transistor. Figure 11 illustrates the driver circuit. A high output on Pin 2 turns on Q_1 and Q_2 driving the gate of the upper N Channel fet to 162 volts. The source of this fet will then rise to the motor supply of 150 volts. The 16 volt Zener Diode protects the gate to source junction during the rise time. When the output at Pin 2 returns to zero, Q_1 and Q_2 will turn off causing the gate to source capacitance of the upper N Channel fet to be discharged rapidly through Q_3. A high output on Pin 6 is buffered by two parallel inverters of a CD4050 for charging the gate capacitance of the lower BUZ73 N Channel power fet. A low output on Pin 6 causes the gate capacitance to discharge rapidly. This circuit is extremely efficient since significant current only flows during the switching times.

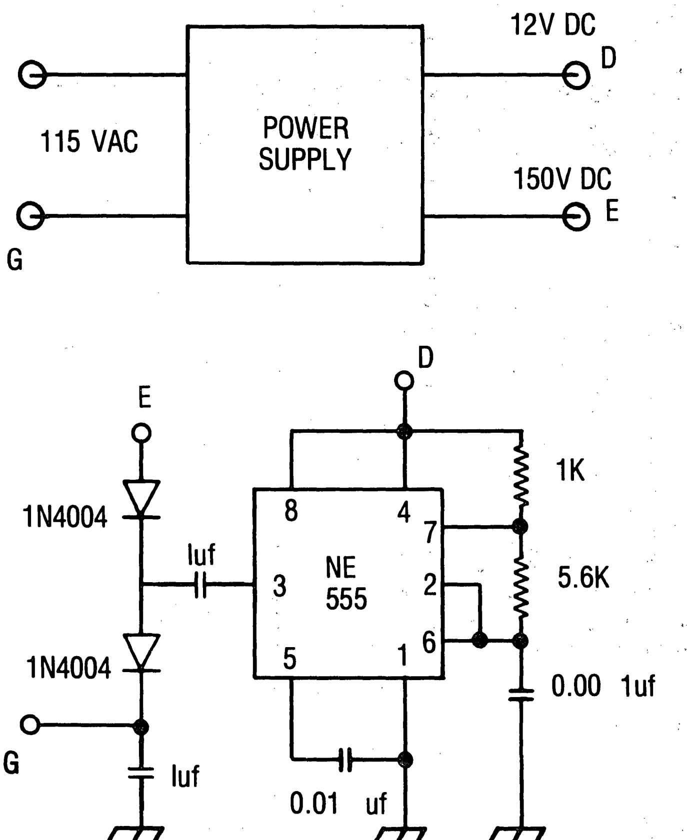


FIGURE 10

VOLTAGE ADDER CIRCUIT FOR ALL N-CHANNEL POWER STAGE MOTOR DRIVER

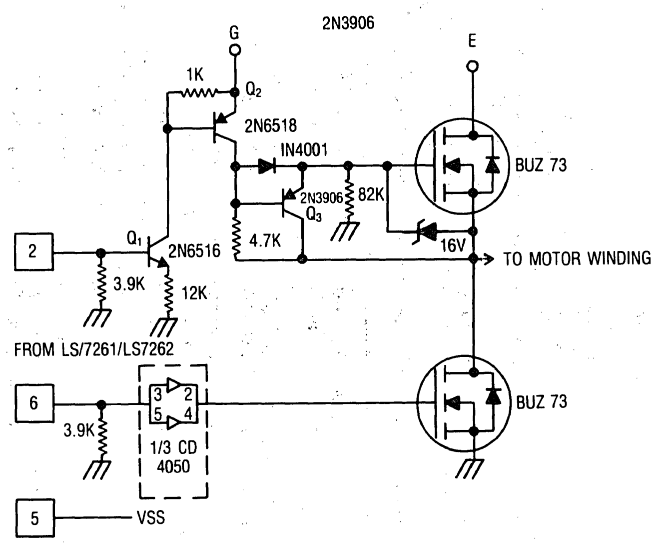


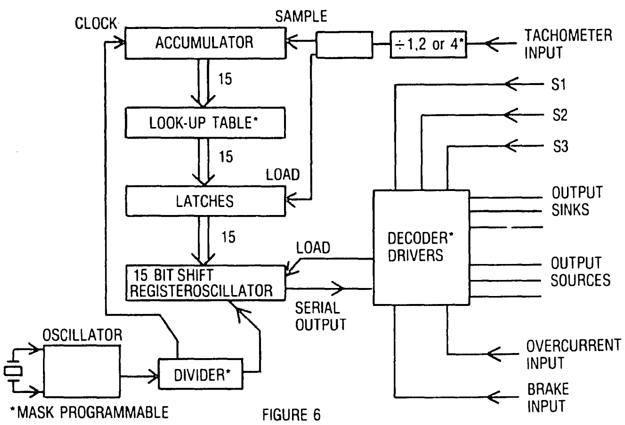
FIGURE 11
HIGH VOLTAGE OUTPUT DRIVER USING TWO-N CHANNEL POWER FETS

EMULATOR

LSI COMPUTER SYSTEMS, INC. has developed an LS7263/LS7264 emulator for optimizing the circuit programmability for any 3 or 4 phase brushless DC motor. If none of the four different types of 3 phase speed controllers or the 1 type of four phase speed controller ready available from LSI COMPUTER SYSTEMS, INC. will exactly match specific motor requirements, then a new circuit can be programmed accordingly. The emulator has 15 thumbwheel switches for adjusting the output power transfer curve and switches for selection of sensor separation, 4 or 8 pole motors, and tachometer division. The emulator provides all the interfacing circuitry found in the integrated circuit and is readily available.

BRUSHLESS DC MOTOR SPEED CONTROLLER

The LS7263 and LS7264 are designed for 3600 RPM ± .1% regulated, fixed speed operation using a 3.58 MHz parallel resonant crystal. The circuits contain programmability for tailoring to specific motor applications. The principle of operation is similar to the closed loop operation previously described. Speed is adjusted by varying the output driver duty cycle. However, the output is not chopped as in the LS7261/LS7262. For each commutation, the corresponding motor winding is turned on and remains on for a percentage of the total time that occurs before the next commutation sequence begins. The On time is determined by a mask programmable ROM Look-Up Table.



*MASK PROGRAMMABLE

FIGURE 6
LS7263/LS7264 BLOCK DIAGRAM

Figure 6 illustrates a simplified block diagram of the circuit. The tachometer input can be any one of the three Hall sense inputs S_1, S_2 or S_3. This input can be divided by 1, 2 or 4 which is mask programmable. This enables speed update information to be gathered either once or twice a revolution for a four pole motor and once, twice, or four times a revolution for an eight pole motor. The output of the tachometer divider circuit is used to transfer new data to the latches and reset the accumulator enabling it to count clock pulses from a zero setting. The accumulator counts for a period equal to the time between tachometer inputs (or a multiple of that time). The number reached in the accumulator is proportional to the time between tachometer inputs which is inversely proportional to the motor speed. As the accumulator advances, its output which addresses the ROM Look Up Table causes the 15 outputs from the Look-Up Table to change from all logic zero's to logic one's, one at a time. The next output of the tachometer divider loads the Look-Up Table outputs into the latches and resets the accumulator to zero. The output driver duty cycle is proportional to the number of stages of the 15 stage latch that are set to a logic one. If the motor had been going at a much slower speed than desired, the latches would be loaded with all logic one's. If the motor had been going at too high a speed, the latches would be loaded with all logic zero's. If the motor is at or near the desired spped, then some of the latches would be loaded with a logic one and others with a logic zero. The exact curve of the percentage of on time versus speed and therefore the loop

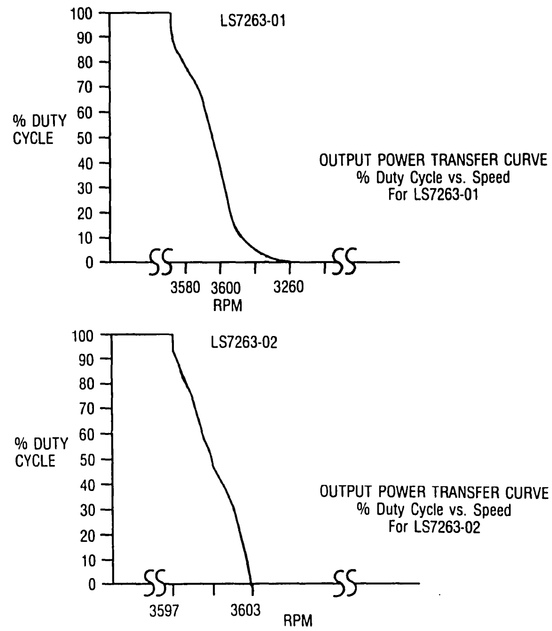


FIGURE 7

gain is detrmined by the ROM in the Look-Up Table and can be tailored to specific motor designs. Figure 7 illustrates the output power transfer curve for 2 versions of the LS7263. The medium gain LS7263-01 circuit has its duty cycle change from 0 to 100% over a 40 RPM motor speed change while the 0 to 100% duty cycle change for the high gain LS7263-02 occurs over a 6 RPM motor speed change.

The outputs of the latches are loaded at the beginning of each new commutation time to the 15 bit shift register. The shift register is clocked by a programmable divider. The divider, whose input is the 3.58 MHz crystal controlled clock, must be programmed to accommodate motors with different numbers of poles since the commutation time will vary, and therefore the speed of the shift register clock must be made to vary. The 15 bits of the shift register are entirely shifted out during each commutation time and applied to the LS7263 decoder driver circuitry. Like the LS7261/LS7262, the LS7263 decoder can be programmed to accommodate sensor separations of 60°, 120°, 240° and 300°. The decoder is set for 90° separation for the LS7264. The decoder driver circuitry provides three output current sinks and three output current sources. These devices have output duty cycles which are determined by the number of latches in the 15 stage latch that are set to a logic one. They will become full On if the motor is going too slow and cut off if the motor is going too fast. A Quiescent condition occurs when the motor is operating at 3600 RPM. The output duty cycle under these conditions is between 30 and 70%. An overcurrent input is also provided which shuts off the output drivers during an overcurrent condition using a circuit similar to that used for the LS7261. Additionally, there is a brake input which will turn off all the sink outputs and a turn on all the source outputs thereby shorting all the motor windings together. There are four versions of the LS7263. Each one has been tailored to a specific motor operating at a fixed 3600 RPM speed. At present, only one version of the LS7264 exists. Table II indicates the programming differences for each circuit available at present.

TYPE	NUMBER OF POLES	SENSOR SEPARATION	GAIN	TACHOMETER DIVISION	DIVIDER SETTING	DUTY CYCLE AT 3600 RPM
7263-01	4	60	Medium	1	384	35%
7263-02	8	120	High	4	192	65%
7263-03	4	120	Medium	2	384	35%
7263-07	8	120	Medium	4	192	65%
7264	4	90	Medium	1	384	65%

TABLE II — DEVICE PROGRAMMING

Even though the LS7263 and LS7264 are designed for fixed speed 3600 RPM operation, other speeds are possible. For example, to operate at 5400 RPM using the LS7263-02, the motor tachometer input is first divided by two and then applied to the integrated circuit. Since the LS7263 now has more time to accumulate clock pulses, the circuit will interpret this to mean that the motor is going too slow and will therefore speed up. By using an external crystal of 2.68 MHz, the motor will operate at exactly 5400 RPM. An alternate method of varying speed is simply to adjust the oscillator input frequency. The oscillator input pin can be forced with an external drive signal instead of hooking it up as a crystal oscillator. By lowering the input drive signal frequency, less clocks will be counted in the accumulator. This will be interpreted by the LS7263 as going too fast and the motor will slow down operation. Operation down to 1500 RPM or less is possible using this technique.

MOTOR DRIVER CIRCUITS

The LS7260/LS7261/62/63/64 are all designed to operate from 7 to 28 volts and have similar output circuitry. Figure 2 indicates a mode of operation in which the motor controller circuit and the motor operate at the same power supply voltage. There are numerous applications in which the DC motor is designed to operate at a voltage higher than the integrated circuit can operate at. In this case, a level converter must be used. For the LS7261/LS7262, level converters are easily constructed if the common input, Pin 5, is tied to the integrated circuit positive supply (VSS). Figures 8, 9 and 11 indicate different level converter circuits using sink output O_1 (Pin 2) and source output O_4 (Pin 6). These outputs are never on simultaneously. Identical circuits are used for O_2 and O_5 and O_3 and O_6. By tying Pin 5 to VSS, all outputs become current sources. Figure 8 illustrates a simple bipolar output stage for level conversin. The Basic bipolar driver circuit uses an NPN and a PNP power transistor in a push-pull arrangement to drive the motor windings. Transistor Q_1 provides the voltage level conversion. A positive output at Pin 2 of the LS7261/LS7262 causes Q_1 to turn on and drive the base of Q_3 through Resistor R_3. A low at Pin 2 cuts off Q_1 and enables transistor Q_3 to turn off rapidly providing R_4 is small. A high appearing at the output of Pin 6 is buffered through emitter follower Q_2 to the base of Q_4. A low at this output causes Q_2 and Q_4 to cut off. For very high voltage applications, the power consumed in R_2 and R_3 can become significant. In these cases, a speed-up capacitor across R_3 and a protective diode across the base to emitter junction of Q_3 is helpful.

One of the disadvantages of the circuit illustrated in Figure 8 is the high power consumed in the resistor network in order to make the level conversion and to have fast switching times. Power fets have an advantage over bipolar power transistors since the drive signals to turn these devices on consist of voltage inputs which do not require large components of current. The equivalent of a push-pull bipolar network utilizes a P Channel and an N Channel power fet. Unfortunately, P Channel power fets are at disadvantage when compared to N Channel power fets. P Channel fets have a much higher on resistance, are harder to get and more expensive than N Channel fets. High on-resistances reduce switching speed and absorb power which lowers efficiency and reliability. However, if a fast P Channel power fet is available, the configuration of Figure 9 can be used.

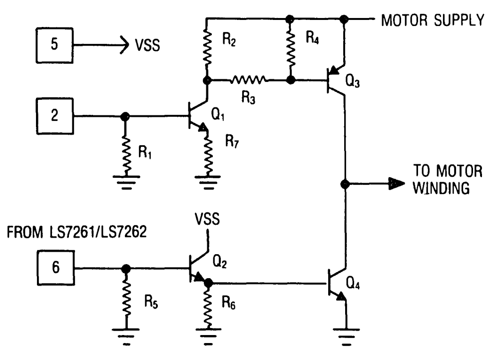


FIGURE 8
BIPOLAR PUSH-PULL MOTOR DRIVER

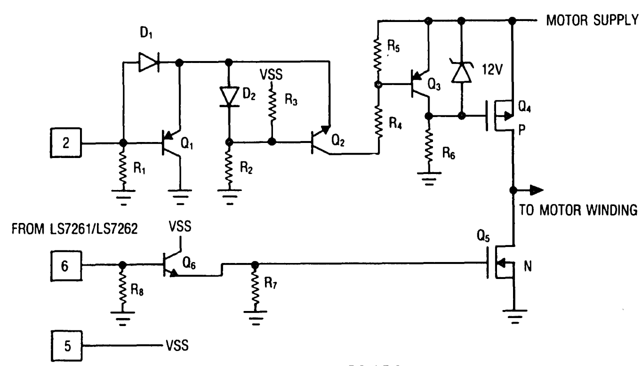


FIGURE 9
HIGH VOLTAGE OUTPUT DRIVER USING A P CHANNEL AND N CHANNEL POWER FET

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PART NUMBER	PACKAGE	DESCRIPTION	1-24	25-99	100	500	1000
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RED 100/120, 300/360 500/600, 3000/3600	8 Lead Plastic DIP	50Hz/60Hz Time Base Frequency Dividers with Reset & Enable	1.95	1.55	1.25	1.05	.90
RDD 104	8 Lead Plastic DIP	Crystal or External Clock Time Base Selectable 4 Decade Frequency Divider	1.90	1.50	1.20	1.00	.85
LS3404, 3406 Series	8 Lead Plastic DIP	Melody Generators with 255 Note Capacity. Mask Programmable ROM produces high quality chime-like sounds with exponential envelope decay of each note.	Special Purchasing Terms Contact Factory for Details.				
LS7030	40 Lead Plastic DIP	7.5MHz 8 Decade Multiplexed Up Counter with 8 Decade Latch (10MHz Version Available)	11.30	9.60	8.15	6.95	5.90
LS7031	40 Lead Plastic DIP	7.5MHz 6 Decade Multiplexed Up Counter with 8 Decade Latch (10MHz Version Available)	11.30	9.60	8.15	6.95	5.90
LS7040	40 Lead Plastic DIP	350KHz Synchronous Dual 3 Decade Up/Down Counter with Parallel BCD Outputs	7.45	6.35	5.40	4.60	3.90
LS7055, LS7056	40 Lead Plastic DIP	250KHz 6 Decade Predetermining Up/Down Counter with Integral Preset, Presignal and Mainsignal Store	8.95	7.60	6.45	5.45	4.65
LS7060	18 Lead Plastic DIP	10MHz 32 Bit Binary Up Counter with Byte Wide Multiplexed Three State Outputs. 32 Bit Latch (15MHz Version Available)	9.70	8.25	7.00	5.95	5.05
LS7061	24 Lead Plastic DIP	10MHz 32 Bit Binary Up Counter with Byte Wide Multiplexed Three State Outputs. 40 Bit Latch (15MHz Version Available)	11.00	9.35	7.95	6.75	5.75
LS7062	18 Lead Plastic DIP	10MHz Dual 16 Bit Binary Up Counter with Byte Wide Multiplexed Three State Outputs. 32 Bit Latch (15MHz Version Avail.)	9.70	8.25	7.00	5.95	5.05
LS7063	24 Lead Plastic DIP	10MHz Dual 16 Bit Binary Up Counter with Byte Wide Multiplexed Three State Outputs. 40 Bit Latch (15MHz Version Avail.)	11.00	9.35	7.95	6.75	5.75
LS7066	40 Lead Plastic DIP	4MHz 24 Bit Multi-Mode Counter Microprocessor Programmable Via 3 State I/O Bus	11.10	8.90	7.10	6.00	5.10
LS7100	16 Lead Plastic DIP	BCD to 7 Segment Latch Decoder/Driver for Liquid Crystal Displays Up to 50V	3.00	2.40	1.95	1.65	1.40
LS7110	16 Lead Plastic DIP	Binary Addressable Latched 8 Channel Demultiplexer/Driver for Liquid Crystal Displays Up to 50V	3.00	2.40	1.95	1.65	1.40
LS7210	14 Lead Plastic DIP	Programmable Digital Delay Timer with Selectable Delay Operate/Release, Dual Delay or One Shot Modes.	2.20	1.75	1.40	1.20	1.00

PART NUMBER	PACKAGE	DESCRIPTION	1-24	25-99	100	500	1000
LS7220, 7225,7226	14 Lead Plastic DIP	Keypad Controlled Digital Locks. Hardware Programmable. 5040 4 Digit Codes	2.30	1.85	1.50	1.25	1.05
LS7222, LS7223	20 Lead Plastic DIP	Keyboard Controlled Digital Locks. Keypad Programmable. 38416 4 Digit Codes.	4.70	3.75	3.00	2.55	2.15
LS7228, LS7229	16 Lead Plastic DIP	Dual Pulse Train or 2 Push Button Controlled Digital Locks. Hardware Programmable. 512 9 Bit Codes	2.30	1.85	1.50	1.25	1.05
LS7231,7232, 7233,7234,7235	8 Lead Plastic DIP	Continuously Variable Lamp Dimmer/AC Power Controller. Touch or Switch Sense.	2.85	2.25	1.80	1.55	1.30
LS7237	8 Lead Plastic DIP	1,3 or 4 Sequential Step Lamp Dimmer/AC Power Controller. Touch or Switch Sense.	1.95	1.55	1.25	1.05	.90
LS7331,LS7332	14 Lead Plastic DIP	Variable Lamp Dimmer/AC Power Controller. Touch/Switch Sense. Dim/Full Bright/Power Fail Output for Microprocessor	3.15	2.50	2.00	1.70	1.45
LS7240	40 Lead Plastic DIP	24 Bit, 7 Level Memory with Multiplexed Comparator. 24 Parallel Inputs.	9.00	8.60	8.15	7.75	7.35
LS7260,7261,7262	20 Lead Plastic DIP	3 or 4 Phase Brushless DC Motor Electronic Commutators. Brake/Reverse/Overcurrent Sense/Speed Control	3.75	3.00	2.40	2.00	1.70
LS7263	18 Lead Plastic DIP	3 Phase Brushless DC Motor Fixed Speed Controller. 0.1% Accuracy. For Disc Drivers & Other Applications.	4.60	3.70	2.95	2.50	2.15
LS7264	16 Lead Plastic DIP	4 Phase Brushless DC Motor Fixed Speed Controller. 0.1% Accuracy. For Disc Drivers & Other Applications.	4.30	3.45	2.75	2.35	2.00
LS7270	40 Lead Plastic DIP	Programmable Integrated Controller/Sequencer	11.30	9.45	8.05	6.85	5.80
LS7310,7311, LS7312,7313	18 Lead Plastic DIP	10 Level AC Power Controller. Power Levels Individually Selectable along with On/Off/Momentary. Touch/Switch Sense	3.75	3.00	2.40	2.05	1.75
LS7501 thru LS7510	16 Lead Plastic DIP	Remote Tone Activated Telephone Line Isolation Controller.	3.70	2.95	2.35	2.00	1.70

NOTES:
1) For extended price quotes, contact factory or your local representative.
2) For price quotes for SOIC,CERDIP, CERAMIC, MIL STD 883 Screening, Waffle Packed Dice, or Probed Wafers, contact factory or your local rep.
3) For samples, contact factory or your local representative.
4) Orders for less than $100.00 must be placed at our distributors.
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