Micro Linear

FB300 Tile Array Family

FB324
BIPOLAR TILE ARRAY

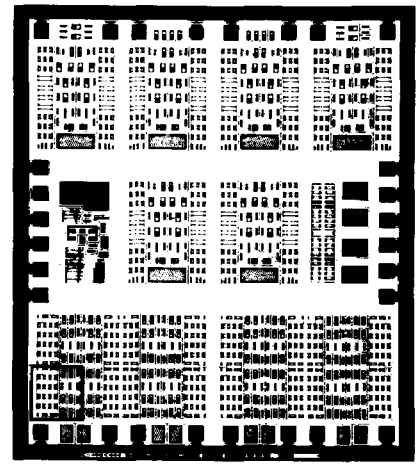
Description

The FB324 has 6 general purpose tiles and 16 high performance tiles. The six general purpose tiles can use any of the predefined macrocells from the FB300 family. The 16 high performance tiles support higher speed and performance macrocells. Macrocells are predefined and tested building blocks such as OP amps, comparators, video amplifiers, AGC amplifiers, timers, sample and hold buffers, and voltage controlled oscillators.

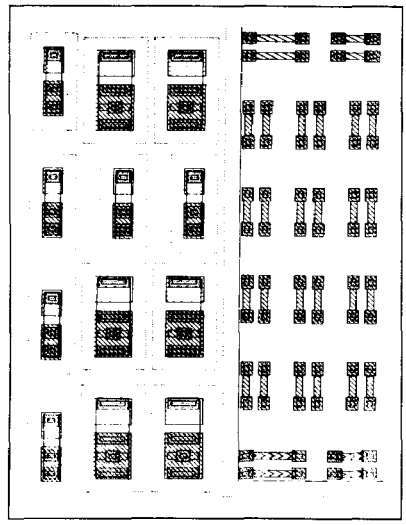
Both the general purpose and high performance tiles allow for both macrocell and component level design. The development of the FB324's 16 high performance tiles are the result of a new high speed, low noise MLCH300 transistor. This transistor achieves this increase in performance because of it's lower base resistance than our general purpose tile equivalent. In addition, a special function tile containing four power NPNs and 36 precision resistors and a reference tile with a dedicated 2.5 or 5 voltage reference exist on the chip.

FB324 Bipolar Tile Array

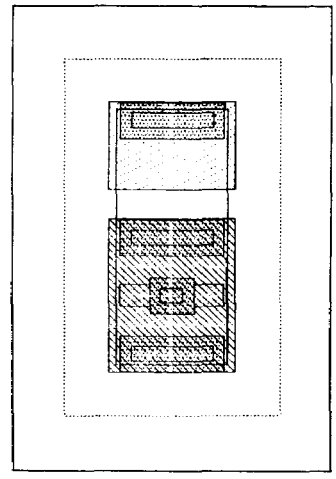
- 16 High Performance Tiles for macrocell or component level design
- Low noise, High speed NPN transistor with low base resistance
- High speed Macrocells for the High Performance Tiles
- 6 General Purpose Tiles, FB300 Family Macrocell compatibility
- Circuit complexity of approximately 14 op amps on a chip
- 1643 analog components for analog design



FB324 Tile Array



High Performance Tile



Low Noise, High Speed NPN Transistor

High Performance Tile Macrocells

MLCH340 Cascode Amplifier
- — programmable gain up to 20
- — can be directly cascaded
- — 3 dB bandwidth of 100 MHz using a gain of 10
- — occupies one high speed tile

MLCH341 D Flip Flop
- — ECL Architecture
- — 100 MHz typical clock frequency
- — occupies two high speed tiles

MLCH342 High Speed Comparator
- — AMD 685 equivalent
- — Total propagation delay of 5 Nsec
- — ECL 10KH compatible outputs
- — Latchable
- — occupies four high speed tiles

MLCH343 Wide band Video Amplifier
- — Signetics 592 based architecture
- — 3 dB bandwidth of 60 MHz at a gain of 100

The High Performance Tile

Each of the 16 High Performance Tiles contain the following components:

High frequency Low noise NPN (MLCH300)	6
Regular NPN (MLC300)	6
850 ohm base link resistor (MLC320)	24
5K ohm implant resistor (MLC321)	4
10K ohm implant resistor (MLC322)	4

FB324 Tile Array Specification

Tiles	
general	6
high speed	16
special function	1
dedicated reference	1
Transistors	
NPN	330
PNP	82
Resistance	
diffused	765k ohms total resistance
qty	804 resistors
implant	2840k ohms total resistance
qty	264 resistors
Capacitance	92 pf
Total components	1643
Bonding pads	28

Electrical Characteristics of the MLCH300 NPN high speed, low noise transistor
(all measurements at 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Collector to Base Breakdown Voltage	BV_{cbo}	I_c = 0.1 mA	25			V
Collector to Emitter Breakdown Voltage	BV_{ceo}	I_c = 0.1 mA	14			V
Emitter to Base Breakdown Voltage	BV_{ebo}	I_e = 0.1 mA	5.7		6.4	V
Temperature Coefficient of BV_{ebo}	$\Delta BV_{ebo}/\Delta T$	I_e = 0.1 mA		2.1		mV/°C
Base to Emitter Voltage	V_{be}	I_e = 1 mA	.71		.76	V
Temperature Coefficient of V_{be}	$\Delta V_{be}/\Delta T$	I_e = 1 mA		-1.65		mV/°C
V_{be} Matching	$\lvert V_{be1}-V_{be2}\rvert$	I_e = 1 mA		0.7	3	mV
Collector to Emitter Saturation Voltage	$V_{ce}(sat)$	I_c = 1 mA, I_b = 0.1 mA		0.12		V
Forward Current Gain	hFe (B)	I_c = 1 mA, V_{ce} = 5V	80		240	
Beta Matching		I_c = 1 mA, V_{ce} = 5V		3		%
Maximum Collector Current	I_c(max)	I_c at Beta = 0.7 Beta (max)	10		12	mA
Gain Bandwidth Product	f_T	I_c = 3, V_{ce} = 5V	630	720		MHz
Base Resistance	rb	I_c = 1mA		250		Ohms

CAD System Support for the FB300 Tile Array Family

Micro Linear does provide both component and macrocell libraries for various CAD systems, including DAISY and Analog Design Tools. This allows the customer to design using our design libraries on general purpose CAD system. The design engineer interconnects Micro Linear's components and macrocells to create a design using the workstation's schematic capture. The analog designer then analyzes the circuit using the system's simulation tools. Our design libraries contain extremely accurate and robust component and macrocell models. This allows for many forms of worst case analysis over process, temperature and voltage. Micro Linear also can provide a prototype kit part set. To facilitate customer education, we offer documentation and a five day course with extensive hands-on training.

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