Micro Linear

ML4816

High Frequency Multi-Mode Resonant Controller

GENERAL DESCRIPTION

The ML4816 controller IC is suitable for a wide range of resonant converter topologies. This controller can be used with Zero Current Switched (ZCS) Quasi Resonant Converters (QRC) requiring constant on-time and modulated off-time, as well as frequency modulated converters such as Series Resonant Converters operating above resonance.

The ML4816's oscillator features independent control of charging and discharging currents (on-time and off-time). Output frequency can be obtained either proportional or inversely proportional to the controlling voltage. In addition, both upper and lower frequency limits (f_{MIN} and f_{MAX}) can be independently set.

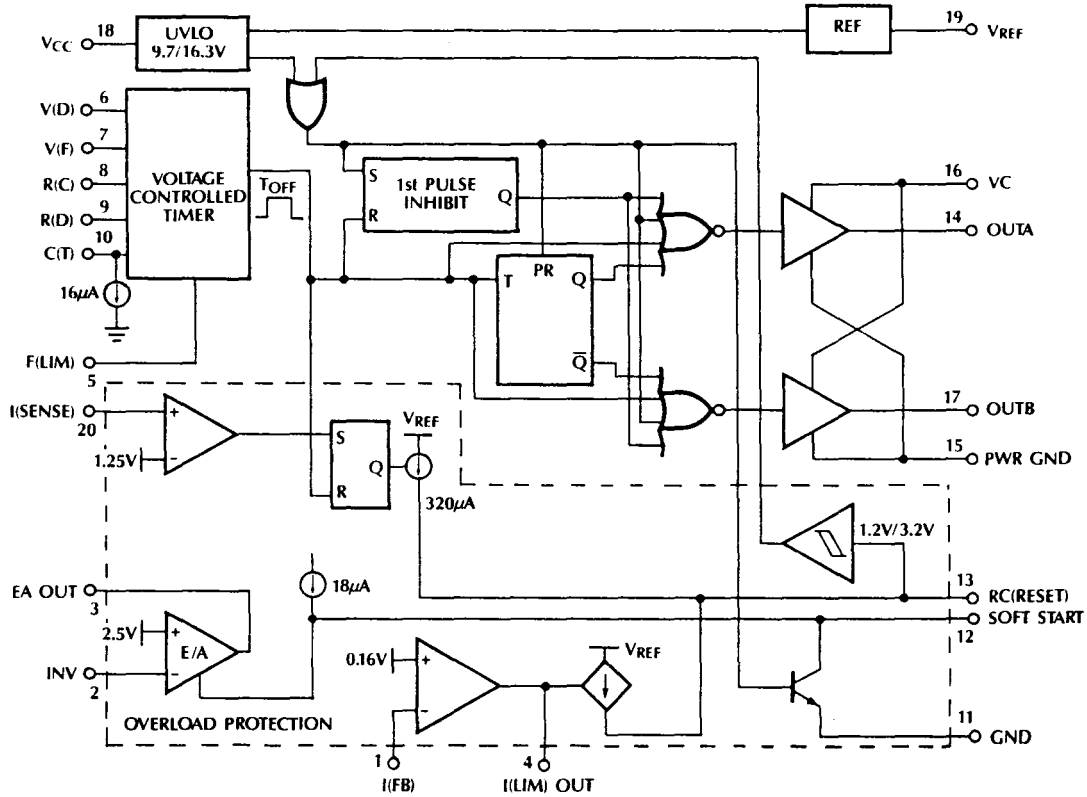
Both pulse-by-pulse and DC current limiting are provided for. Overload protection (shutdown) is triggered after a programmable delay time. Restart after overload shutdown can be delayed by a programmable time. Internal logic disables the gate drive until the oscillator is stable.

The ML4816 includes under-voltage lockout with 6V hysteresis and high current high speed totem pole output drivers for high speed drive of external MOSFETs.

FEATURES

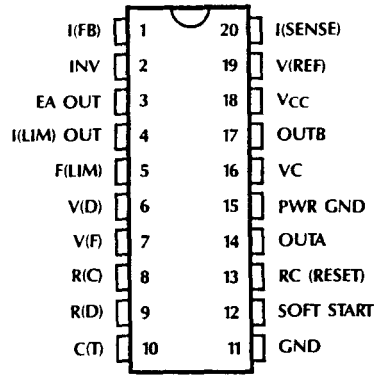
- Supports Zero Current Switched (ZCS) Quasi-Resonant Converters
- Supports Series Resonant (ZVS) converters operating above resonance
- Wide oscillator frequency range
- Programmable f_{MIN} and f_{MAX} limits
- Practical Operation to 2.5MHz (f_{OSC})
- Low Start-up Current and Under-Voltage Lockout Circuits support Off-Line Operation
- Pulse by Pulse or DC Current Limiting
- Integrating Soft Start Reset (Fault Integration) with Programmable Restart Delay
- High current (1.5A peak) totem-pole output drive
- Precision buffered 5V Reference (±1%)

BLOCK DIAGRAM



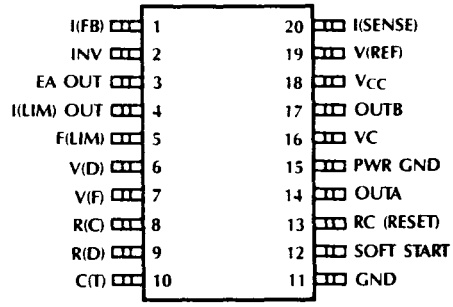
PIN CONFIGURATION

ML4816
20-Pin DIP



TOP VIEW

ML4816
20-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	I(FB)	Input for load current limit.
2	INV	Inverting input to error amp.
3	EA OUT	Output of error amplifier.
4	I(LIM) OUT	Output for load current limit amplifier.
5	F(LIM)	A voltage input sets the maximum on time for the timer.
6	V(D)	Controls the C(T) discharge current and oscillator off time. Connected to error amplifier output for off-time modulation and to V(REF) for constant off time.
7	V(F)	Controls the charging current and oscillator on time. Connected to error amplifier for on time modulation and connected to GND for constant on time.
8	R(C)	External timing resistor to either GND or V(REF) sets the charging current (oscillator on time). This pin can either source or sink current.
9	R(D)	External resistor from this pin to GND sets the oscillator discharge current (off time).
10	C(T)	Timing capacitor for Oscillator.
11	GND	Signal ground.
12	SOFT START	Normally connected to Soft Start capacitor.
13	RC(RESET)	Timing elements for Integrating fault detection and reset delay circuits.
14	OUTA	High Current Totem pole output A.
15	PWR GND	Return for the High Current Totem Pole outputs.
16	VC	Supply for the High Current Totem Pole outputs.
17	OUTB	High Current Totem pole output B.
18	V_{CC}	Positive supply for the IC.
19	V(REF)	Buffered output for the 5.0V voltage reference.
20	I(SENSE)	Primary current sense input for current limit.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 16, 18) 30V
Output Current, Source or Sink (Pin 12)
DC 0.5A
Pulse (0.5μs) 1.5A
Analog Inputs
(Pins 1, 2, 5, 6, 7, 13) ..... –0.3V to 6.3V
Amplifier Output Currents (Pins 3, 4) 5mA
Soft Start Sink Current (Pin 8) 100mA
R(C) Current (Pin 8) ..... –0.5 to +0.5mA
R(D) Current (Pin 9) ..... –4mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP or SOIC ..... 65°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to +70°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, C_T = 470pF, V_{CC} = 15V. V_{CC} is adjusted above the start threshold before settling at 15V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_A = 25°C, I_O = –1mA	4.90	5.00	5.10	V
Line Regulation	12V ≤ V_{CC} ≤ 25V		2	20	mV
Load Regulation	1mA ≤ I_O ≤ 10mA		5	20	mV
Temperature Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (note 1)		0.2	0.4	mV/°C
Total Variation	line, load, temp.	4.85		5.15	V
Output Noise Voltage	10Hz < f < 10KHz		50		μV
Long Term Stability	T_J = 125°C, 1000 Hrs (note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0	–40	–70	–100	mA
Error Amplifier Section					
Non-Inverting Input Voltage		2.37	2.47	2.57	V
Input Bias Current				3	μA
Open-Loop Gain	1 ≤ V_O ≤ 4V	60			dB
Unity Gain Bandwidth	(note 1)	2.5	2.8		MHz
PSRR	12V ≤ V_{CC} ≤ 25V	75			dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7V, $V_{PIN\ 3}$ = 1V	1	2.8		mA
Output Source Current	$V_{PIN\ 2}$ = 2.3V, $V_{PIN\ 3}$ = 4V	–0.5	–2.2		mA
Output High Voltage	$I_{PIN\ 3}$ = –0.5mA	5.0	5.5	6.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA		0.5	1.0	V
Slew Rate			8.5		V/μs
Current-Limit Amplifier Section					
Non-Inverting Input Voltage		0.145	0.16	0.175	V
Input Bias Current				–1	μA
Open-Loop Gain	1 ≤ V_O ≤ 4V	65			dB
Unity Gain Bandwidth	(note 1)	1.0	1.5		MHz
PSRR	12V ≤ V_{CC} ≤ 25V	60			dB
Output Sink Current	$V_{PIN\ 1}$ = 1V, $V_{PIN\ 4}$ = 1V	1	1.6		mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, C_T = 470pF, V_{CC} = 15V. V_{CC} is adjusted above the start threshold before settling at 15V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Amplifier Section (Continued)						
Output Source Current		$V_{PIN\ 1}$ = 0V, $V_{PIN\ 4}$ = 4V	-0.5	-1.1		mA
Output High Voltage		$I_{PIN\ 4}$ = -0.5mA	6.0	7.2	8.0	V
Output Low Voltage		$I_{PIN\ 4}$ = 1mA		0.7	1.0	V
Slew Rate		(note 1)		0.9		V/μs
Current-Sense Section						
Input Bias Current		$V_{PIN\ 20}$ = 0			-2	μA
Current-Sense Threshold			1.20	1.25	1.30	V
Delay to Pin 13		(note 1)		80	150	ns
Soft-Start Section						
Discharging Current		$V_{PIN\ 13}$ = 4V, $V_{PIN\ 12}$ = 1V	20	35		mA
Charging Current		$V_{PIN\ 13}$ = 0, $V_{PIN\ 12}$ = 1V	-14	-18	-22	μA
Overload Protection Section						
Overload Threshold			3.0	3.2	3.5	V
Restart Threshold			1.0	1.2	1.4	V
Pulse-by-pulse Charging Current		$V_{PIN\ 20}$ = 1.35V, $V_{PIN\ 13}$ = 2V		-320		μA
Current-Limit Amp. Controlled Current		$V_{PIN\ 1}$ = 0, $V_{PIN\ 13}$ = 2V $V_{PIN\ 4}$ = 1V $V_{PIN\ 4}$ = 2.5V		 -2.2 -0.9		 mA mA
Voltage-Controlled Timer						
C_T Minimum Discharging Current		$V_{PIN\ 6}$ = 0, $V_{PIN\ 10}$ = 3V	14	16	18	μA
C_T Peak Voltage				3.75		V
C_T Valley Voltage				2.1		V
R(C) Minimum Voltage		$V_{PIN\ 5}$ = $V_{PIN\ 7}$ = 0, 25KΩ from Pin 8 to GND	0.446V_{REF}	0.455V_{REF}	0.464V_{REF}	V
R(C) Voltage		$V_{PIN\ 5} = \frac{8}{11} V_{REF}$, $V_{PIN\ 7}$ = 5V, 25KΩ from Pin 8 to GND	0.713V_{REF}	0.727V_{REF}	0.742V_{REF}	V
R(D) Minimum Voltage		$V_{PIN\ 6}$ = 0, 3KΩ from Pin 9 to GND			0	V
R(D) Maximum Voltage		$V_{PIN\ 6}$ = 5V, 3KΩ from Pin 9 to GND	0.425V_{REF}	0.45V_{REF}	0.475V_{REF}	V
T_{ON}	T_A = 25°C	$V_{PIN\ 5}$ = $V_{PIN\ 7}$ = 0, $V_{PIN\ 6}$ = 3V, 25KΩ from Pin 8 to GND, 3KΩ from Pin 9 to GND	0.66	0.68	0.70	μs
	Total Variation	12V ≤ V_{CC} ≤ 25V (note 1) T_{MIN} ≤ T_A ≤ T_{MAX}	0.63	0.71	0.79	μs
Output Dead Time	T_A = 25°C (note 1)	$V_{PIN\ 5}$ = $V_{PIN\ 7}$ = 0, $V_{PIN\ 6}$ = 5V, 25KΩ from Pin 8 to GND, 3KΩ from Pin 9 to GND	110	120	130	ns
	Total Variation	12V ≤ V_{CC} ≤ 25V (note 1) T_{MIN} ≤ T_A ≤ T_{MAX}	100	120	140	ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, C_T = 470pF, V_{CC} = 15V. V_{CC} is adjusted above the start threshold before settling at 15V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Voltage-Controlled Timer (Continued)						
Frequency	$f_{MAX(1)}$	$V_{PIN\ 5} = V_{PIN\ 7} = 0$, $V_{PIN\ 6}$ = 5V 25KΩ from Pin 8 to GND 3KΩ from Pin 9 to GND	1.1	1.2	1.3	MHz
	$f_{MIN(1)}$	$V_{PIN\ 5} = V_{PIN\ 7} = 0$, $V_{PIN\ 6}$ = 1.4V 25KΩ from Pin 8 to GND 3KΩ from Pin 9 to GND	17	22	26	KHz
	$f_{MAX(2)}$	$V_{PIN\ 5} = \frac{8}{11} V_{REF}$, $V_{PIN\ 7}$ = 2V, $V_{PIN\ 6}$ = 5V 22KΩ from Pin 8 to Pin 19 3KΩ from Pin 9 to GND	1.35	1.45	1.55	MHz
	$f_{MIN(2)}$	$V_{PIN\ 5} = \frac{8}{11} V_{REF}$, $V_{PIN\ 7}$ = 5V, $V_{PIN\ 6}$ = 5V 22KΩ from Pin 8 to Pin 19 3KΩ from Pin 9 to GND	750	800	850	KHz
Under Voltage Lockout Section						
Start Threshold			15.8	16.3	16.8	V
Stop Threshold			9.2	9.7	10.2	V
Supply Current						
Start-Up Current		V_{CC} = 15.5V	1.2	1.5	1.8	mA
Operating Supply Current		$V_{PIN\ 5} = V_{PIN\ 7} = 0$, $V_{PIN\ 6}$ = 5V 25KΩ from Pin 8 to GND 3KΩ from Pin 9 to GND $C_{LA} = C_{LB} = 0$, T_A = 25°C,	26	32	38	mA
		$T_{MIN} \leq T_A \leq T_{MAX}$			53	mA
Output Section						
Output Low Level		I_{SINK} = 20mA		0.1	0.4	V
		I_{SINK} = 200mA		0.7	2.2	V
Output High Level		I_{SOURCE} = 20mA	12.0	13.5		V
		I_{SOURCE} = 200mA	11.5	13.0		V
Rise Time		$C_{LA} = C_{LB}$ = 1nF (note 1)			60	ns
Fall Time		$C_{LA} = C_{LB}$ = 1nF (note 1)			60	ns

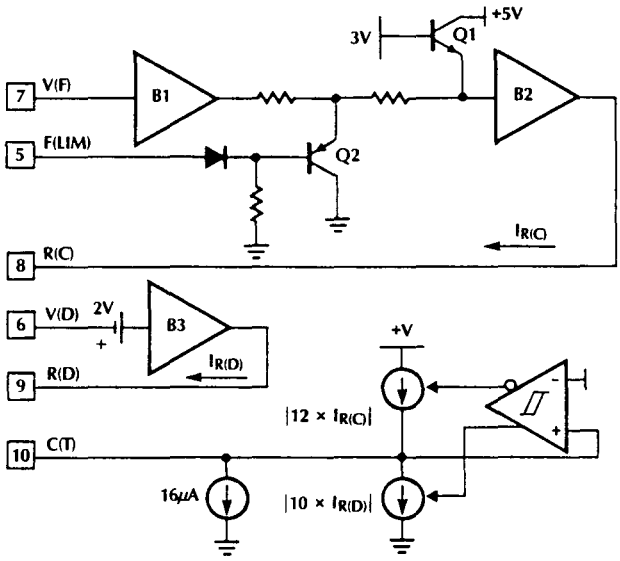
Note 1: This parameter is not 100% tested in production but guaranteed by design.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The oscillator is the core of the ML4816 and is designed to allow the maximum flexibility. This oscillator can be used in two basic modes of operation:

1. On time proportional to V_{IN}, fixed off time with a maximum on time limit (where V_{IN} is the output of the error amplifier).
2. Off time inversely proportional to V_{IN}, fixed on time.



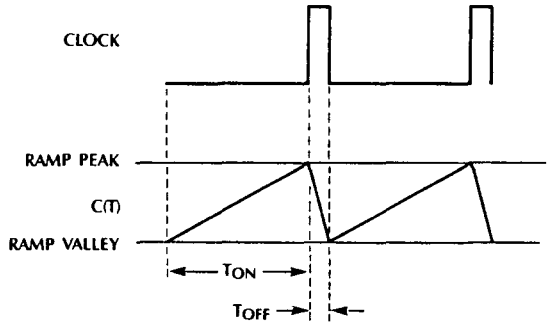


Figure 1. Oscillator Block Diagram

The internal CLOCK signal, shown above, turns the outputs off at its rising edge. Clock remains high and the outputs stay off as long as C(T) is discharging. The discharge time (T_{OFF}) of C(T) is:

$$T_{OFF} = \frac{1.65\ C(T)\ R(D)}{10\ (V(D) - 2V) + 16\mu A\ R(D)} \quad (1)$$

Variable Off-Time, Constant On-Time (Figure 2)

When using a variable off time control, V(D) is tied to the output of the error amplifier. Off time is given by equation (1) while the 16μA current sink prevents the off time from becoming infinite, thereby providing an upper limit to T_{OFF} of:

$$\text{Max } (T_{OFF}) = C(T) \times 1.03 \times 10^5 \quad (2)$$

The on time is given by:

$$T_{ON} = 0.0605\ R(C)\ C(T) \quad (3)$$

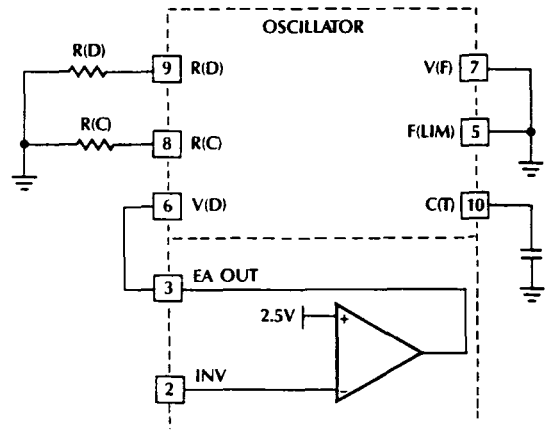


Figure 2. Variable Off Time, Constant On Time Oscillator Connections

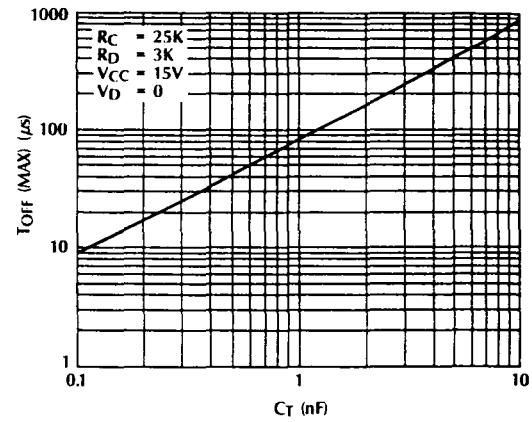


Figure 2a. Max (T_{OFF}) vs. C_T

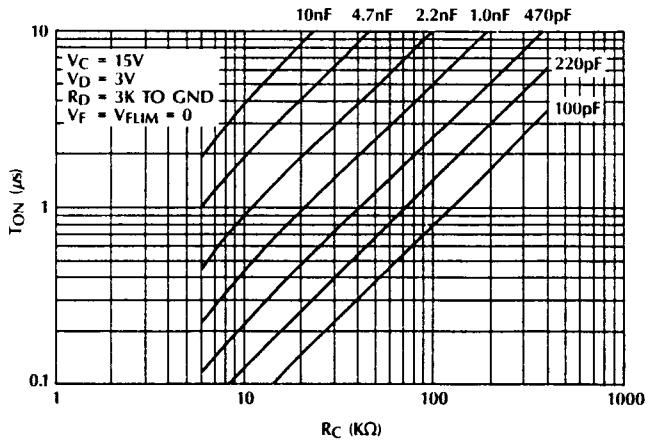


Figure 2b. T_{ON} vs. R(C)

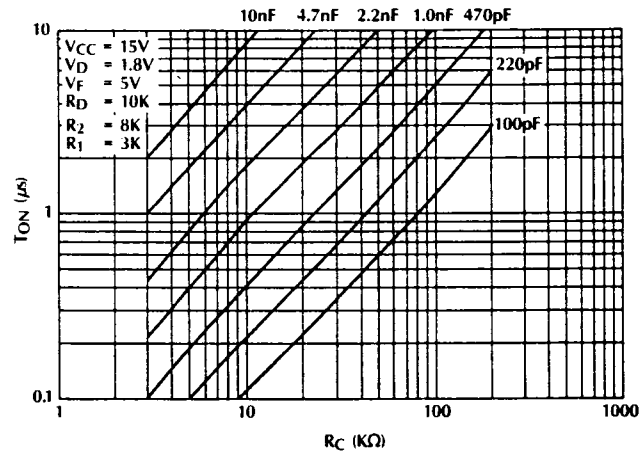


Figure 3a. Minimum T_{ON} for Constant Off-Time Configuration with $V_{FLIM} = \frac{8}{11} \times V_{REF}$

Variable On-Time, Constant Off-Time

The on time (T_{ON}) is controlled by the current flowing from V(REF) through R(C) into B2. The output of B2 is internally limited to be no less than 2.27V and no greater than F(LIM).

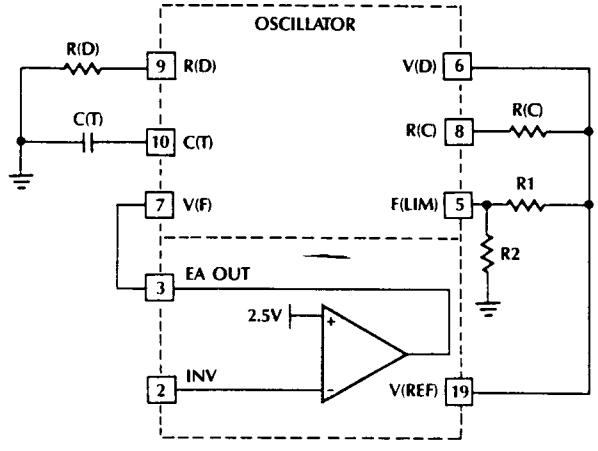


Figure 3. Variable On Time, Constant Off Time Oscillator Connections (T_{ON} Proportional to EA OUT)

The on time for figure 3 is given by:

$$T_{ON} = \frac{0.138\ R(C)\ C(T)}{V(REF) - V(F)} \quad (4)$$

The maximum on time is given by:

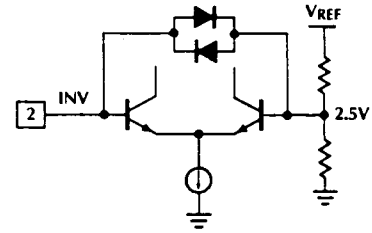
$$T_{ON(MAX)} = \frac{0.138\ R(C)\ C(T)}{V(REF) - F(LIM)} \quad (5)$$

where F(LIM) > 2.27V. The minimum on time is:

$$T_{ON(MIN)} = 0.0506\ R(C)\ C(T) \quad (6)$$

ERROR AMPLIFIER

The ML4816 error amplifier is a 2.5MHz bandwidth, 8.5V/µsec slew rate op-amp with provision for limiting the positive output voltage swing to implement the soft start function.



The Error Amplifier input contains protection diodes as shown above. INV should not be driven lower than 2.5V – V_{BE} or higher than 2.5V + V_{BE}.

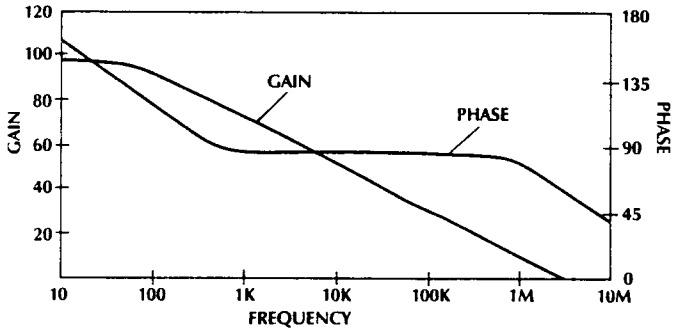


Figure 5. Error Amplifier Open-Loop Gain and Phase vs. Frequency

OUTPUT DRIVER STAGE

The ML4816 has two high current high speed totem pole output drivers each capable of 1.5A peak output, designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors.

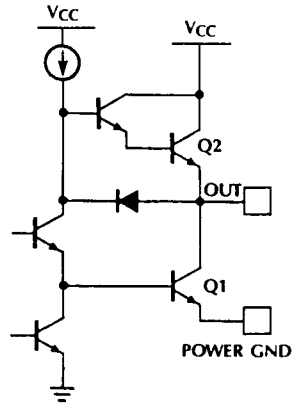


Figure 6. Power Driver Simplified Schematic

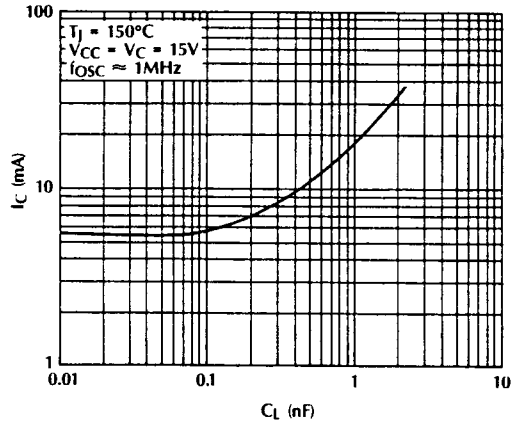


Figure 6a. Output Driver Current Consumption I(C) vs. Output Load Capacitance

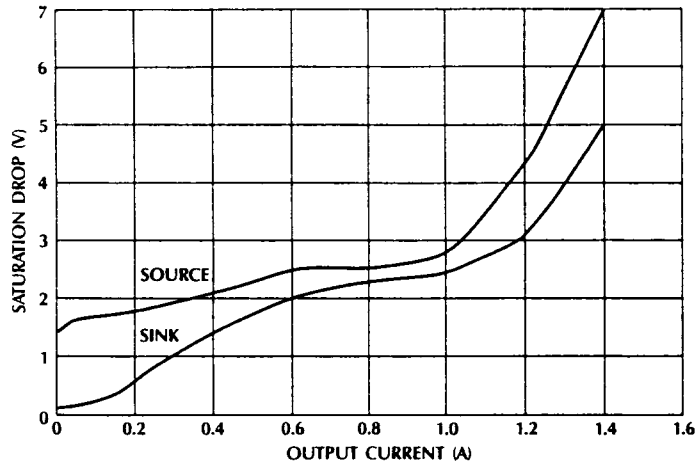


Figure 7. Output Saturation Voltage vs. Output Current

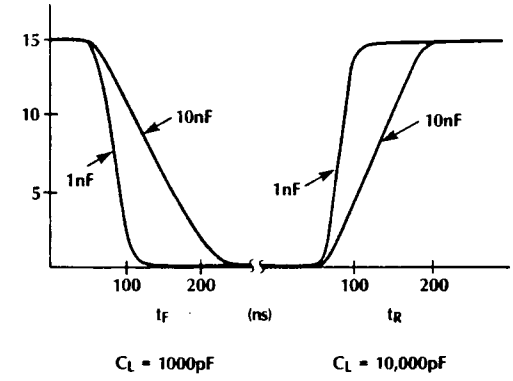


Figure 8. Rise/Fall Time

CURRENT LIMIT, FAULT DETECTION AND SOFT START

The ML4816 has two modes of current limiting: Primary pulse-by-pulse over-current protection and secondary DC average current limiting.

Primary Pulse-by-Pulse Current Limit Circuit

In this mode, the primary current is compared with a 1.25V threshold in comparator X1. When the sensed current exceeds the 1.25V threshold of comparator X1, the R-S latch X2 is set, turning on the 320μA current source to charge C_{RST}. I_{F1} remains on until CLOCK goes high (T_{OFF}). When C_{RST} has charged to 3.2V, a soft start reset occurs. The number of times the outputs reach current limit are "remembered" on C_{RST}. Over time, C_{RST} is discharged by R_{RST} providing a measure of "forgetting" when the over-current condition no longer occurs. If the output fault is removed before C_{RST} reaches 3.2V, C_{RST} discharges slowly through R_{RST} and normal operation resumes.

Over-Current Sensing, Overload Shutdown and Fault Management

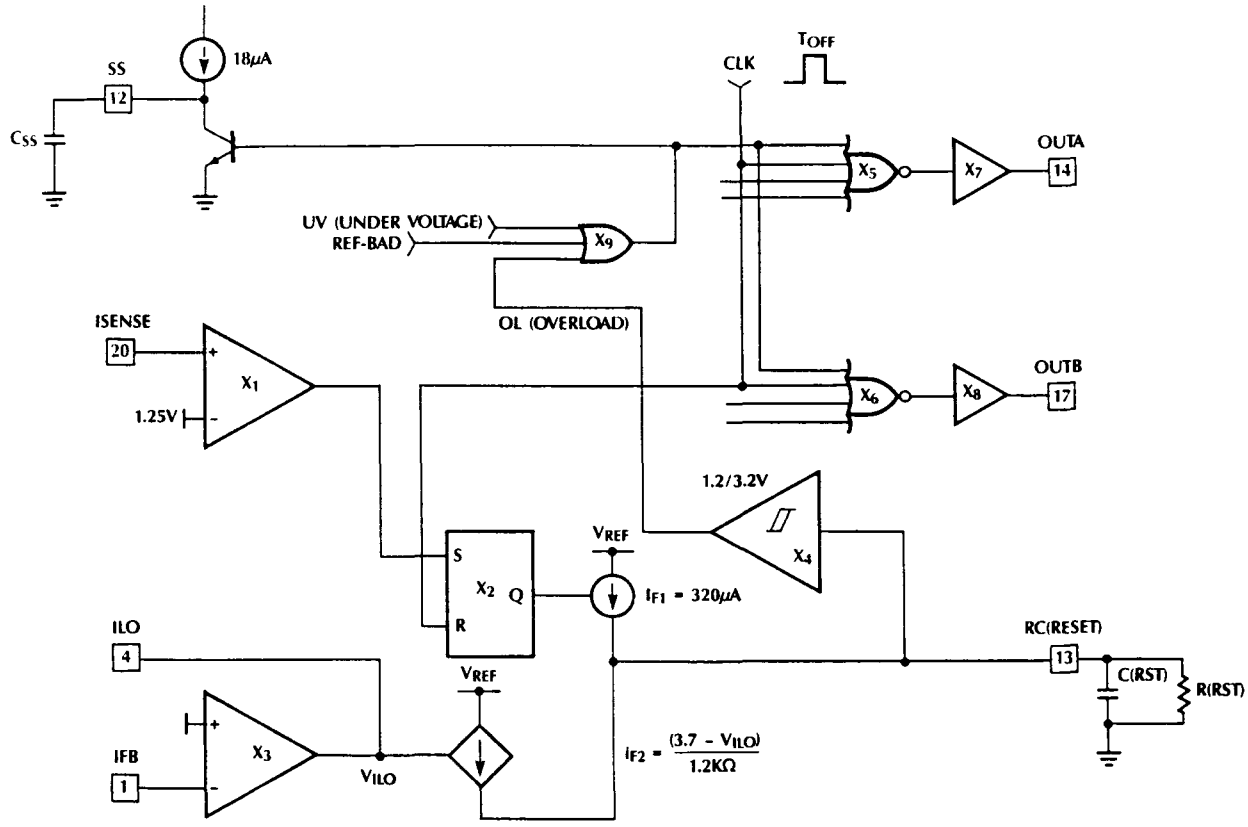


Figure 9. Overload Protection and Fault Management

Secondary dc Current Limit Circuit

In secondary dc current-limiting, the currents in the output rectifiers are sensed, full-wave rectified and smoothed. The smoothed signal is fed into the current-limiting amplifier X_3. If the sensed current is below the 0.16V threshold, the output of X_3 will go above V_{REF} and I_{F2} will be off. As the sensed current exceeds the current-limit threshold, V_{ILO} starts to fall and

$$I_{F2} \left(\approx \frac{V_{REF} - V_{ILO} - 2V_{BE}}{1200\Omega} \right)$$ turns on. I_{F2} charges C_{RST} towards the overload threshold (3.2V) of X_4. C_{RST} charging and temporary recovery through R_{RST} here are similar to the pulse-by-pulse over-current sensing case except that I_{F2} is continuous.

Under persistent output short circuit with either form of over-current protection, C_{RST} is charged until it reaches 3.2V. The gate drives are immediately terminated and the soft-start capacitor C_{SS} is discharged. C_{RST} then discharges through R_{RST} toward the restart threshold (1.2V). Gate drives remain off until C_{RST} is discharged below 1.2V. The time taken for C_{RST} to discharge to the restart threshold is the restart-delay time. This delay reduces the average power delivered to the load during overload, thus protecting both the load and the controller. If overload persists, the controller will continue to hiccup until the cause of overload is removed. The controller undergoes soft-start at each restart.

The overload shutdown and restart sequences for both over-current protection schemes with non-bootstrapped V_{CC} are illustrated in Figures 10 and 11.

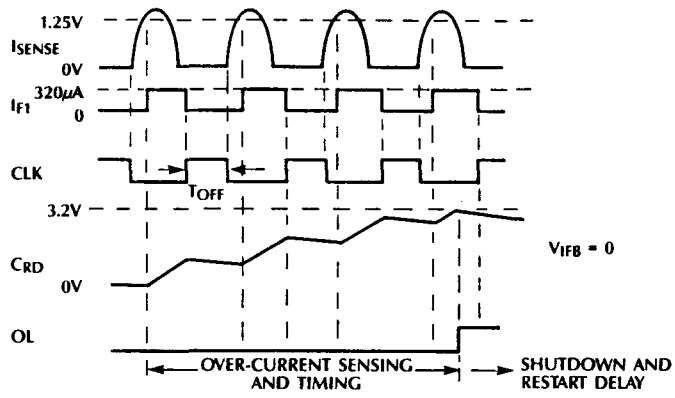


Figure 10. Over-Current Sensing, Overload Shutdown and Restart Sequence (Non-Bootstrapped V_{CC}) (ZCS-QRC Transistor Current Shown)

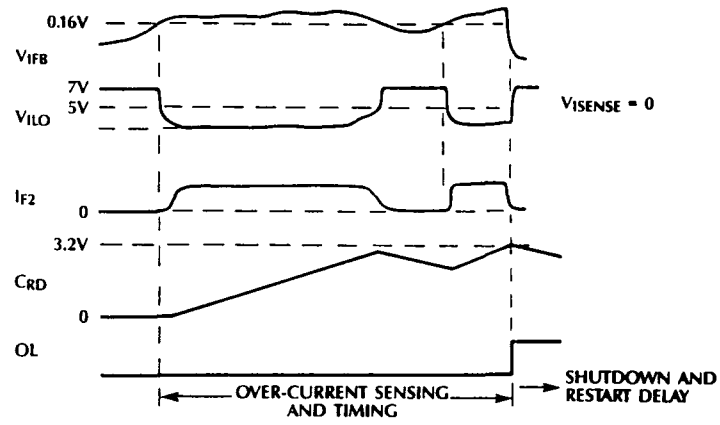


Figure 11. Secondary dc Current Sensing, Overload Shutdown and Restart Sequence (Non-Bootstrapped V_{CC})

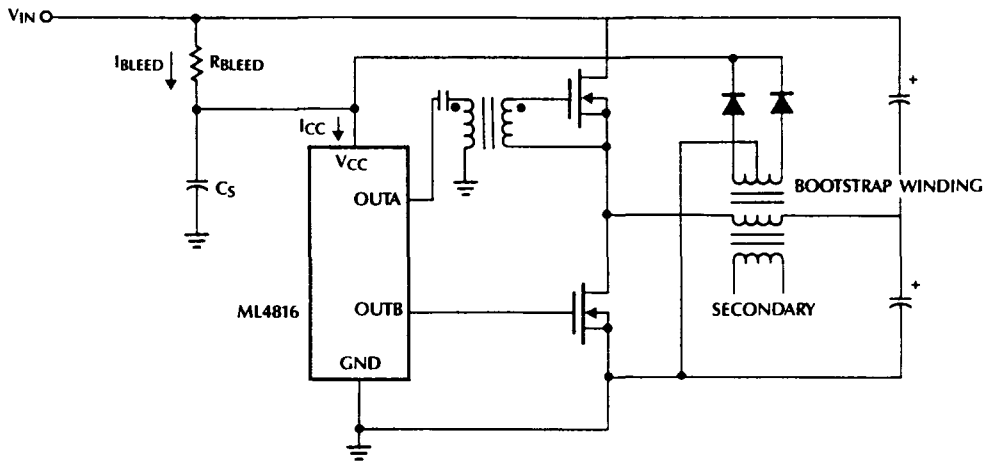


Figure 12. Simplified V_{CC} Bootstrapping Scheme in Half-Bridge Configuration

For a bootstrapped converter, where controller V_{CC} is obtained from an auxiliary winding of the main transformer, (see Figure 12) overload shutdown causes both the converter output and the controller V_{CC} to collapse. Undervoltage lockout (UVLO) is activated and the on-chip bandgap reference is disabled. ML4816 dissipates only 1.5mA during shutdown. Since I_{BLEED} is higher than the start-up current, C_S will be charged towards the UVLO start threshold. When this happens, the entire controller becomes operational except that the gate drives remain off. I_{CC} jumps to its full operational value. Since V_{CC} bootstrapping is not yet available, I_{CC} will discharge C_S below the UVLO stop threshold. The on-chip reference will again be disabled with the controller supply current reduced to 1.5mA. I_{BLEED} will again charge C_S towards the UVLO start threshold. The process repeats until C_{RST} is discharged below the restart threshold. The shutdown and restart sequence is illustrated in Figure 13.

The over-current timing and shutdown sequence can be disabled by grounding pin 13.

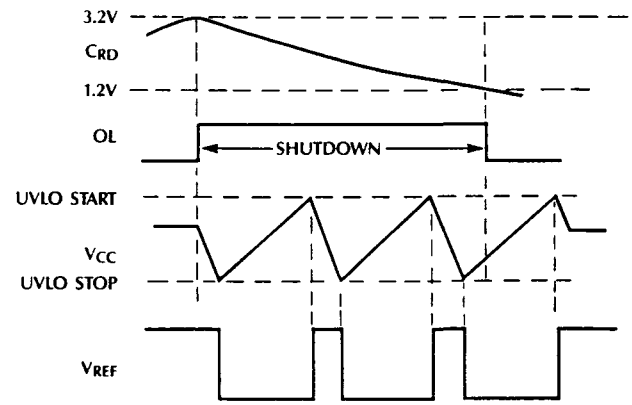


Figure 13. Overload Shutdown, UVLO and Restart Sequence (Bootstrapped Operation)

Auxiliary Output Current-Limiting (RC(RESET) Pin Grounded)

Constant current at power inverter output can be obtained by utilizing the current-limit amplifier with pin 13 shorted to ground. The ILO pin is connected to the EAO pin through two external OR-ing diodes D_1 and D_2 (Figure 14). R_1 is used as a pull-up resistor. The current-limiting loop activates and takes control if the voltage at the inverting input IFB of the current-limit amplifier exceeds the 160mV threshold and ILO is pulled below EAO. The schematic shows that either the main error amplifier or the current-limiting amplifier controls the switching frequency of the converter. The voltage to the IFB pin comes from the output of a current sensor which produces a signal proportional to the output current.

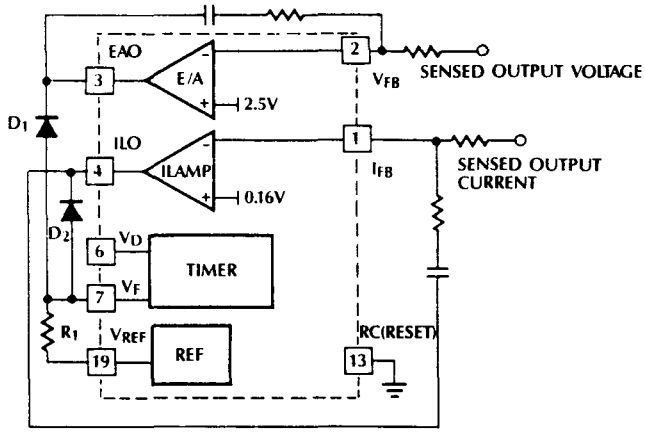


Figure 14. Auxiliary Output Current-Limiting

First-Pulse Inhibit

ML4816 features a unique scheme to prevent input transformer from saturating during initial start-up. Before V_{CC} rises above the undervoltage lockout (UVLO) start threshold, the bandgap reference is disabled. Since the bias circuit of the timer requires a reference output of at least $4V_{BE}$ to operate, the timing capacitor C_T remains fully discharged. As V_{CC} crosses UVLO start threshold at t_0, the reference becomes enabled. The reference output rises at a rate determined by the reference short-circuit current and the external bypass capacitor. C_T remains discharged until V_{REF} exceeds $4V_{BE}$. There is no gate drive until V_{REF} reaches the "reference-good" level (4.4V) (see Figure 16). Once V_{REF} exceeds $4V_{BE}$ (t_1), C_T is charged towards the upper threshold of the oscilllator/timer. Although the gate drives are enabled at t_2, the first-pulse inhibit latch continues to blank the outputs. This latch is reset when C_T voltage crosses the upper oscillator threshold at t_3. OUTA is gated on after the CLK pulse elapses.

Without the first-pulse inhibit circuit, the first OUTA pulse would be on for time T_{ONI} which could be as much as 2 to 3 times longer than the desired T_{ON} time. The first-pulse inhibit latch ensures no abnormally long first gate drive pulse, independent of V_{REF} rise time.

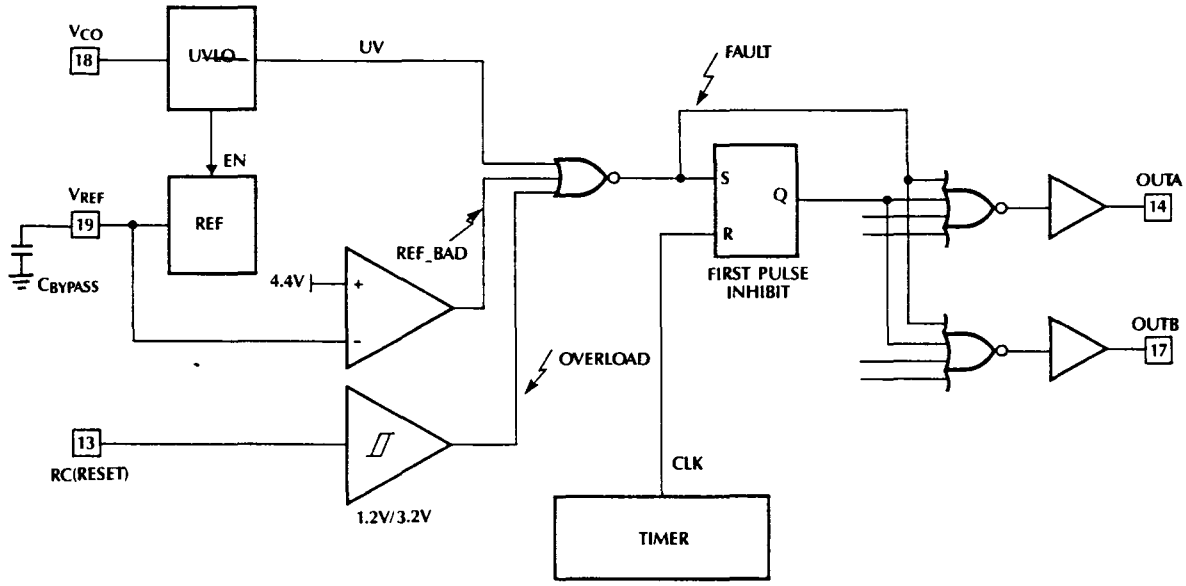


Figure 15. Operation of UVLO and the First-Pulse Inhibit Circuit

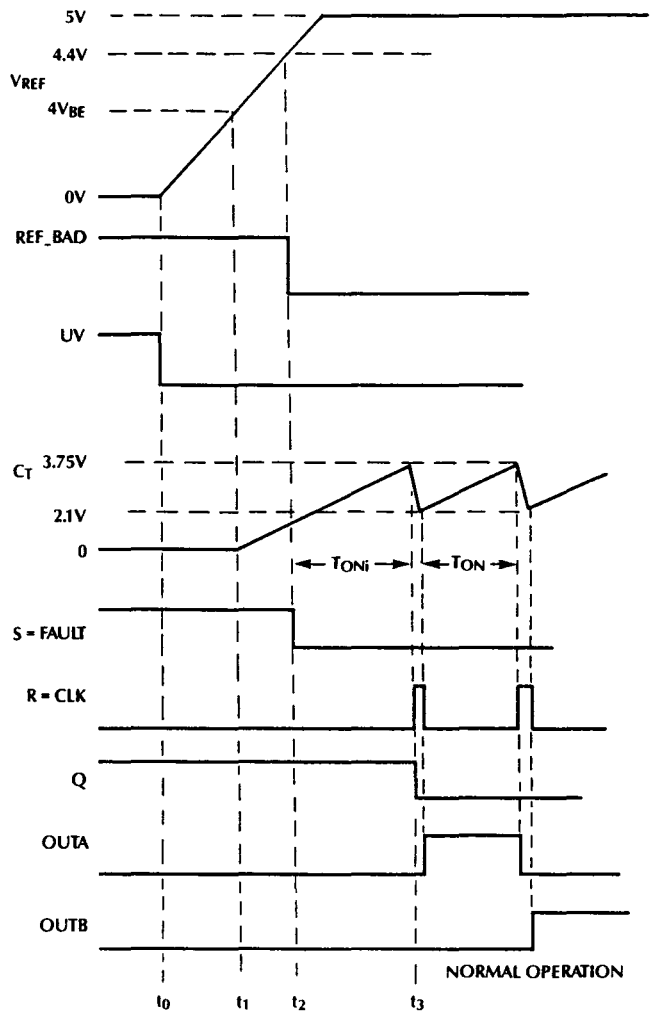
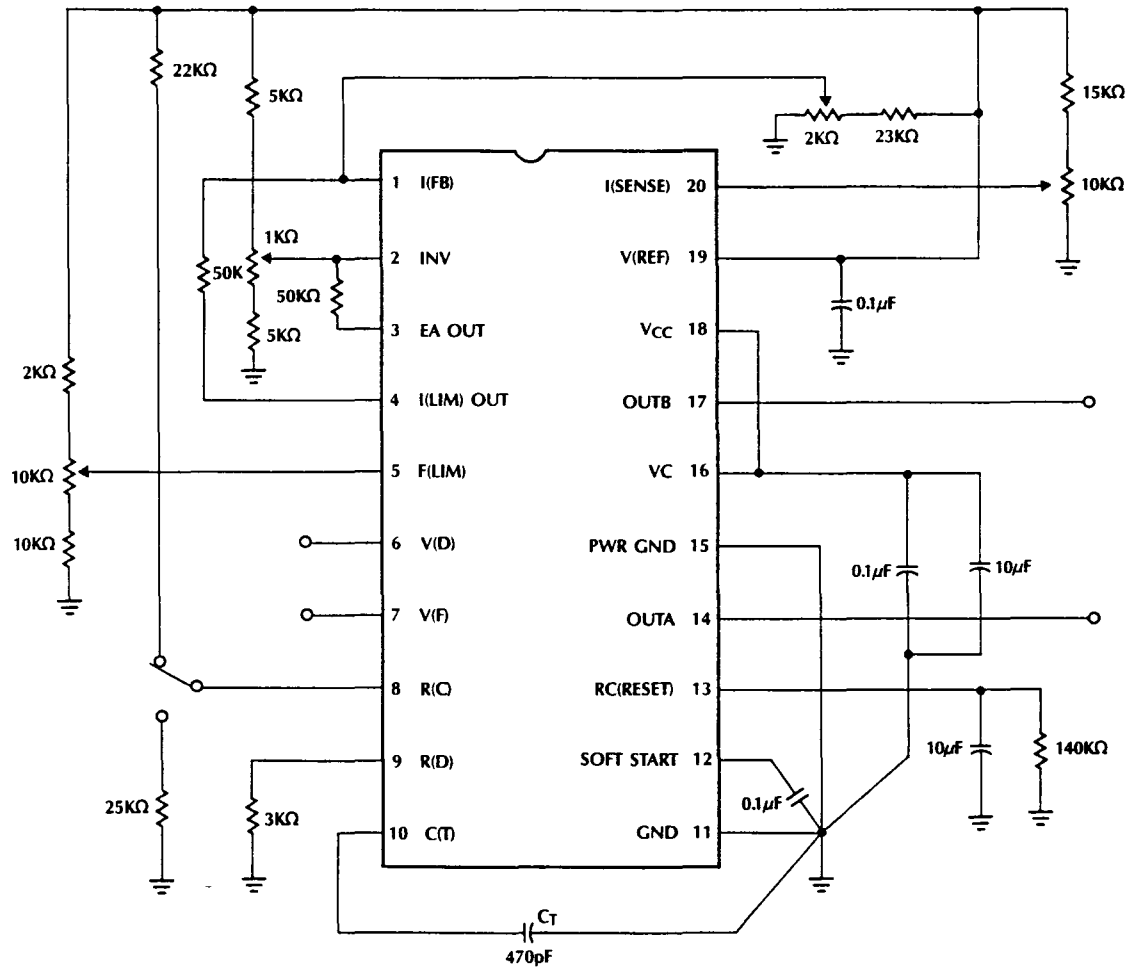


Figure 16. Timing Diagram Illustrating Initial Start-Up and the First-Pulse Inhibit

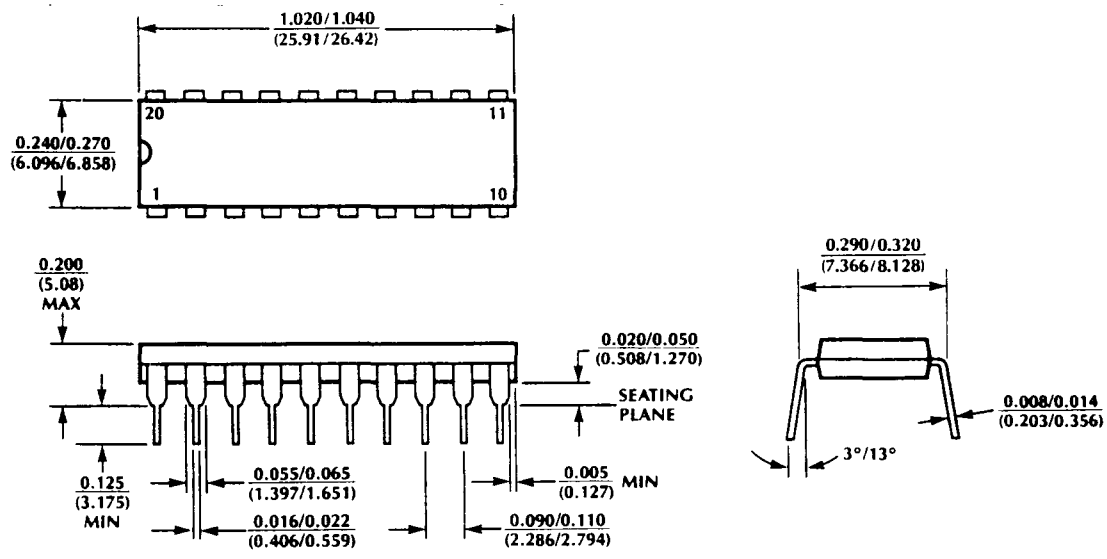
Open Loop Laboratory Test Fixture



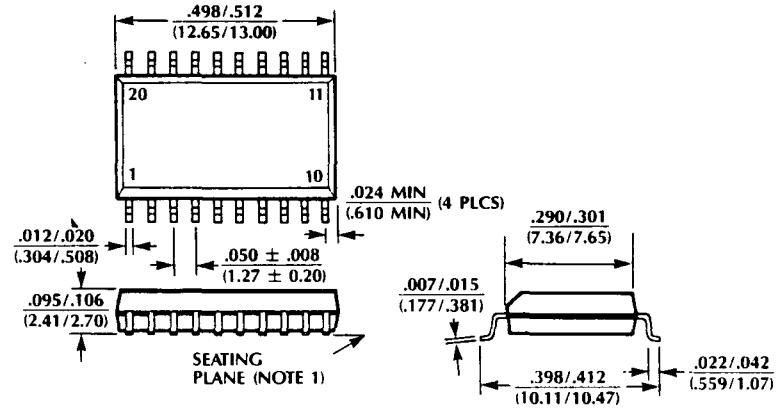
This test fixture is useful for exercising many of the ML4816's functions and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

PHYSICAL DIMENSIONS inches (millimeters)

20-Pin Molded DIP Package (P20)



20-Pin SOIC (S20W)



NOTE 1: SEATING PLANE LEAD COPLANARITY .005 (0.127) (BOTTOM OF LEADS).
NOTE 2: NOMINAL DIMENSIONS ±0.005 (0.127) UNLESS OTHERWISE SPECIFIED.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4816CP	0°C to +70°C	Plastic DIP (P20)
ML4816CS	0°C to +70°C	Plastic SOIC (S20W)

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D835 ML/BL 2.5K 0891-B Printed in U.S.A.