MITSUBISHI SEMICONDUCTORS 1987

BIPOLAR DIGITAL IC

ASTTL

DATA BOOK

MITSUBISHI ELECTRIC

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INVERTER, DRIVERS

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		Propagation time (ns)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)		
Hex Inverter	M74AS04P	5	145	20	2	14P4	2—7
Hex Inverting Driver	M74AS1004AP	3.5	149	48	48	14P4	2—91
Hex Driver	M74AS1034AP	5	193	48	48	14P4	2—95

NAND GATES/DRIVERS

Quadruple 2-input Positive NAND Gate/Driver	M74AS00P	4.5	96	20	2	14P4	2—3
	M74AS1000AP	3.5	105	48	48	14P4	2—89
Triple 3-input Positive NAND Gate	M74AS10P	4.5	72	20	2	14P4	—
Dual 4-input Positive NAND Gate	M74AS20P	5	48	20	2	14P4	2—11
8-input Positive NAND Gate	M74AS30P	5	27	20	2	14P4	—
Hex 2-input NAND Driver	M74AS804BP	4	149	48	48	20P4	2—80
	M74AS1804P	4	149	48	48	20P4	2—97

AND GATES/DRIVERS

Quadruple 2-input Positive AND Gate/Driver	M74AS08P	5.5	132	20	2	14P4	2—9
	M74AS1008AP	5	129	48	48	14P4	2—93
Triple 3-input Positive AND Gate	M74AS11P	6	99	20	2	14P4	—
Dual 4-input Positive AND Gate	M74AS21P	6	66	20	2	14P4	2—13
Hex 2-input AND Driver	M74AS808BP	5	193	48	48	20P4	2—83
	M74AS1808P	5	193	48	48	20P4	2—100

NOR GATES/DRIVERS

Quadruple 2-input Positive NOR Gate	M74AS02P	4.5	111	20	2	14P4	2—5
Triple 3-input Positive NOR Gate	M74AS27P	5.5	94	20	2	14P4	—
Hex 2-input NOR Driver	M74AS805BP	4	176	48	48	20P4	—
	M74AS1805P	4	176	48	48	20P4	—

OR GATE/DRIVERS

Quadruple 2-input Positive OR Gate	M74AS32P	5.8	146	20	2	14P4	2—15
Quadruple 2-input Positive OR Driver	M74AS1032AP	5.5	143	48	48	14P4	—
Hex 2-input OR Driver	M74AS832BP	5.5	215	48	48	20P4	2—86
	M74AS1832P	5.5	215	48	48	20P4	2—103

EXCLUSIVE OR GATE

Quadruple 2-input Exclusive OR Gate	M74AS86P					14P4	—

LINE DRIVERS

Function Description	Output		Type	Specification (Max)				Package outlines	Page
	3-state	Open collector		Propagation time (ns)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)		
Octal Buffer/Line Driver	I	—	M74AS240P	6.5	413	64	15	20P4	2—30
	N	—	M74AS241P	6.2	495	64	15	20P4	2—33
	N	—	M74AS244P	6.2	495	64	15	20P4	2—36
	—	I	M74AS756P	19.5	440	64	—	20P4	2—74
	—	N	M74AS757P	21	523	64	—	20P4	—
	—	N	M74AS760P	18.5	517	64	—	20P4	2—77
Octal Bus Transceiver	N	—	M74AS245P	7.5	787	48	15	20P4	2—39
	I	—	M74AS620P	7	671	64	15	20P4	2—62
	—	N	M74AS621P	24	1040	64	—	20P4	—
	—	I	M74AS622P	25	567	64	—	20P4	—
	N	—	M74AS623P	9	1040	64	15	20P4	2—65
	I	I	M74AS638P	20	671	64	15	20P4	—
	N	N	M74AS639P	22	847	64	15	20P4	—
	I	—	M74AS640P	7	677	64	15	20P4	2—68
	N	—	M74AS645P	9.5	820	64	15	20P4	2—71
Octal Bus Transceiver and Register	N	—	M74AS646P	11	1161	64	15	24P4D	—
	I	—	M74AS648P	11	1073	64	15	24P4D	—
	I	—	M74AS651P	11	1073	64	15	24P4D	—
	N	—	M74AS652P	11	1161	64	15	24P4D	—

I: With inverted output N: With noninverted output

J-K FLIP-FLOPS

Function Description	Type	Specification (Max)				Trigger	Set	Reset	Package outlines	Page
		Operating Frequency (MHz)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)					
Dual J-$\overline{K}$ Flip-Flop	M74AS109P	105	94	20	2	⎍	⎍	⎍	16P4	—
Dual J-K Flip-Flop	M74AS112P			20	2	⎎	⎍	⎍	16P4	—

⎍ : Positive-going edge ⎎ : Negative-going edge ⎍ : Active low-level

D-Type FLIP-FLOPS

Function Description	Output		Type	Specification (Max)				Trigger	Set	Reset	Package outlines	Page
	Active pull-up	3-state		Operating frequency (MHz)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)					
Dual D-Type Flip-Flop	I•N	—	M74AS74P	105	88	20	2	↑	⊓	⊓	14P4	2—17
Hex D-Type Flip-Flop	N	—	M74AS174P	100	248	20	2	↑		⊓	16P4	—
Quadruple D-Type Flip-Flop	I•N	—	M74AS175P	100	187	20	2	↑		⊓	16P4	—
Octal D-Type Flip-Flop	—	N	M74AS374P	125	704	48	15	↑			20P4	2—52
	—	I	M74AS534P	125	704	48	15	↑			20P4	2—59
	—	N	M74AS574P	125	737	48	15	↑			20P4	—
10-Bit Bus Interface Flip-Flop	—	N	M74AS821P		622	48	24	↑			24P4D	—
	—	I	M74AS822P		622	48	24	↑			24P4D	—
9-Bit Bus Interface Flip-Flop	—	N	M74AS823P			48	24	↑		⊓	24P4D	—
	—	I	M74AS824P			48	24	↑		⊓	24P4D	—
8-Bit Bus Interface Flip-Flop	—	N	M74AS825P			48	24	↑		⊓	24P4D	—
Dual 4-Bit D-Type Flip-Flop	—	N	M74AS874P	125	880	48	15	↑		⊓	24P4D	—

I: With inverted output N: With noninverted output I•N: With both inverted and noninverted output
↑ : Positive-going edge ⊓ : Active low-level

LATCHES

Function Description	Output		Type	Specification (Max)				Enable	Set	Reset	Package outlines	Page
	Active pull-up	3-state		Propagation time (ns)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)					
Octal D-Type Transparent Latch	—	N	M74AS373P	11.5	550	48	15	⊔			20P4	2—48
	—	I	M74AS533P	9	605	48	15	⊔			20P4	2—55
	—	N	M74AS573P	11.5	583	48	15	⊔			20P4	—
10-Bit Bus Interface D-Type Latch	—	N	M74AS841P	12	517	48	24	⊔			24P4D	—
	—	I	M74AS842P	12	534	48	24	⊔			24P4D	—
9-Bit Bus Interface D-Type Latch	—	N	M74AS843P	13	506	48	24	⊔	⊓	⊓	24P4D	—
8-Bit Bus Interface D-Type Latch	—	N	M74AS845P	13	468	48	24	⊔	⊓	⊓	24P4D	—
Dual 4-Bit D-Type Latch	—	N	M74AS873P	11.5	710	48	15	⊔		⊓	24P4D	—

I: With inverted output N: With noninverted output ⊔ : Active high-level ⊓ : Active low-level

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SHIFT REGISTERS

Function Description	Type	Specification (Max)				Reset	Package outlines	Page
		Operating frequency (MHz)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)			
8-Bit Universal Shift/Storage Register	M74AS299P			48	15	A	20P4	—
	M74AS323P			48	15	S	20P4	—
4-Bit Bidirectional Universal Shift Register	M74AS194P	80	330	20	2	A	16P4	—

A: Asynchronous S: Synchronous

SYNCHRONOUS COUNTERS

Function Description	Type	Specification (Max)				Trigger	Parallel loading	Reset	Package outlines	Page
		Operating frequency (MHz)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)					
Synchronous Presettable 4-Bit Binary Counter with Direct Reset	M74AS161P	75	292	20	2	↑	S	A	16P4	—
Fully Synchronous Presettable 4-Bit Binary Counter	M74AS163P	75	292	20	2	↑	S	S	16P4	—
Synchronous 4-Bit Up/Down Binary Counter	M74AS169P	75	347	20	2	↑	S	—	16P4	—
Synchronous 8-Bit Up/Down Counter with Direct Reset	M74AS867P	50	1073	20	2	↑	S	A	24P4D	—
Fully Synchronous 8-Bit Up/Down Counter	M74AS869P	45	990	20	2	↑	S	S	24P4D	—

↑ : Positive-going edge A: Asynchronous S: Synchronous

DATA SELECTORS/MULTIPLEXERS

Function Description	Output		Strobe input	Type	Specification (Max)				Package outlines	Page
	Active pull-up	3-state			Propagation time (ns)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)		
8 to 1 Data Selector/Multiplexer	I·N	—	○	M74AS151P	15	165	48	15	16P4	—
	—	I·N	—	M74AS251P			48	15	16P4	—
Dual 4 to 1 Data Selector/Multiplexer	N	—	○	M74AS153P	12.5	182	48	15	16P4	—
	I	—	○	M74AS352P	13	154	48	15	16P4	—
	—	N	—	M74AS253P	13.5	182	48	15	16P4	—
	—	I	—	M74AS353P	12	171	48	15	16P4	—
Quadruple 2 to 1 Data Selector/ Multiplexer	N	—	○	M74AS157P	11	154	20	2	16P4	2—24
	I	—	○	M74AS158P	10.5	124	20	2	16P4	2—27
	—	N	—	M74AS257P	11	175	48	15	16P4	2—42
	—	I	—	M74AS258P	10	139	48	15	16P4	2—45
Quadruple 2-Input Multiplexer with Storage	N	—	—	M74AS298P	11	198	20	2	16P4	—
Hex 2 to 1 Universal Multiplexer	—	I·N	○	M74AS857P	18	963	48	15	24P4D	—

I: With inverted output N: With noninverted output I·N: With both inverted and noninverted output

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DECODER/DEMULTIPLEXER

Function Description	Type	Specification (Max)				Package outlines	Page
		Propagation time (ns)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)		
3 to 8 Decoder/Demultiplexer	M74AS138P	10	110	20	2	16P4	2—21

COMPARATOR

8-Bit Magnitude Comparator	M74AS885P	17.5	1155	20	2	24P4D	—

PARITY GENERATOR

9-Bit Parity Generator/Checker	M74AS280P	12	193	20	2	14P4	—

CARRY GENERATOR

32-Bit Look-Ahead Carry Generator	M74AS882P	14	578	20	2	24P4D	—

ALU

Function Description	Type	Specification (Max)			Package outlines	Page
		Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)		
Arithmetic Logic Unit/Function Generator	M74AS181AP	1100	20	2	24P4D	—
	M74AS881AP	1155	20	2	24P4D	—

REGISTER FILE

Function Description	Type	Specification (Max)					Package outlines	Page
		Access time (ns)	Write time (ns)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)		
Dual 16-By-4 Register File	M74AS870P	15	22	1045	48	15	24P4D	—

SYMBOLOGY

Symbol	Descriptions	
C_L	Load capacitance	Externally connected load capacitance
f_{max}	Maximum clock frequency	Maximum input repetition frequency for normal operation.
F_I	Fan-in	Number of similar inputs
F_O	Fan-out	Number of similar ICs which can be driven by an output
H	Indicates the high logic level	Used in voltage and current suffixes to indicate the high potential level
I	Indicates current or input	Currents flowing into ICs are taken to be positive and those flowing out as negative
I_{CC}	Supply current	The current flowing into the V_{CC} supply terminal of a circuit
I_{CCL}	Low-level supply current	V_{CC} current when the inputs are such that the output is low.
I_{CCH}	High-level supply current	V_{CC} current when the inputs are such that the output is high.
I_{CCZ}	High-impedance supply current	V_{CC} current when the inputs are such that the output is in the high-impedance state.
I_F	Forward current	Forward diode current
I_I	Input current at maximum voltage	The input current flowing when maximum voltage is applied to the IC input pins.
I_{IH}	High-level input current	The current flowing into an input when a specified high voltage is applied.
I_{IL}	Low-level input current	The current flowing out of an input when a specified low voltage is applied.
I_O	Output current	The current flowing out of an output when that output is high-level and 2. 25V is applied.
I_{OH}	High-level output current	The current flowing into or out of an output which is in the high state.
I_{OL}	Low-level output current	The current flowing into an output which is in the low state
I_{OS}	Short-circuit output current	The current flowing out of an output which is in the high state when that output is short circuit to ground.
I_{OZH}	Off-state high-level output current	The current flowing into a disabled 3-state output with a specified high output voltage applied
I_{OZL}	Off-state low-level output current	The current flowing out of a disabled 3-state output with a specified low output voltage applied
I_T	Threshold current	Current which flows when the threshold voltage is applied to the input
I_{T+}	Positive threshold current	Current which flows when the positive threshold voltage is applied to the input
I_{T-}	Negative threshold current	Current which flows when the negative threshold voltage is applied to the input
L	Indicates the low logic level	Used in voltage and current suffixes to indicate the low potential level
O	Indicates output	
P_d	Power dissipation	Product of the supply voltage and the supply current
PRR	Pulse repetition rate	The rate of repetition of an applied pulse train
T_a	Operating free-air temperature	The temperature of the environment surrounding an IC
t_f	Falltime	Time required to fall from the high to the low logic level
t_h	Hold time	The required hold time for specified input after an input has changed
T_{opr}	Operating temperature	The ambient temperature range for normal operation
t_{pd}	Propagation delay time	Amount of time required from a change of input signal until the corresponding change in output, expressed as the average propagation time.
t_{PHL}	Propagation delay time, high-to-low-level output	Amount of time required from a change of input signal until the output changes from high to low.
t_{PHZ}	Output disable time from High level	Amount of time required from a change of input signal until the output changes from high to high-impedance.
t_{PLH}	Propagation delay time, low-to-high-level output	Amount of time required from a change of input signal until the output changes from low to high.
t_{PLZ}	Output disable time from Low level	Amount of time required from a change of input signal until the output changes from low to high-impedance.

SYMBOLOGY

Symbol	Descriptions	
t_w	Pulse width	
t_{WO}	Output pulse width	The width of the pulse appearing in the output of a monostable multivibrator
t_{PZH}	Output enable time to High level	Amount of time required from a change of input signal until the output changes from high-impedance to high.
t_{PZL}	Output enable time to Low level	Amount of time required from a change of input signal until the output changes from high-impedance to low.
t_r	Risetime	Time required to rise from the low to the high logic level
T_{stg}	Storage temperature	The range of surrounding storage temperature for an IC.
t_{su}	Setup time	The required hold time for an input before a particular input may be changed.
V_{CC}	Supply voltage	The voltage applied to the V_{CC} pin.
V_{BE}	Base-emitter voltage	
V_F	Forward voltage	Forward voltage applied to a diode
V_I	Input voltage	Voltage applied to an input
V_{IC}	Input clamp voltage	The forward voltage applied to an input clamping diode.
V_{IH}	High-level input voltage	The range of input voltages that represents a logic high in the system.
V_{IL}	Low-level input voltage	The range of input voltages that represents a logic low in the system.
V_O	Output voltage	Voltage applied to or appearing at an output
V_{OH}	High-level output voltage	Voltage at an output in the high state
V_{OL}	Low-level output voltage	Voltage at an output in the low state
V_P	Pulse amplitude	The voltage difference between the low level and high level of a pulse.
V_T	Threshold voltage	The input voltage at which the output changes
V_{T+}	Positive-going threshold voltage	The threshold voltage at which the output changes when the input is changing from low to high.
V_{T-}	Negative-going threshold voltage	The threshold voltage at which the output changes when the input is changing from high to low.
Z	Indicates the off-state	Indicates that the output is in the high-impedance state.
Z_O	Output impedance	The load impedance which should be connected to such devices as pulse generators.

INTRODUCTION

User demands for higher speeds and lower power dissipation in standard logic ICs has resulted in increased use of high-speed STTL (Schottky TTL) and low power LSTTL (low power Schottky TTL) moving away from TTL (transistor transistor logic).

However, to meet increasing demands for even higher speeds and lower power dissipation, Mitsubishi Electric has begun marketing the next generation of TTL ICs: ALSTTL (advanced low power Schottky TTL) since 1985, and now ASTTL (advanced Schottky TTL), which has higher speeds and lower power dissipation than STTL. When completed, the full lineup will consist of approximately 90 devices.

This section will explain the processing, basic circuit, and electrical characteristics of ASTTL devices.

1. ASTTL Processing

The increased speed and decreased power dissipation of ASTTL is mostly achieved through improved production processes. Propagation time is the amount of time necessary for charging and discharging parasitic capacitance within the IC, and is proportional to the product of resistance and parasitic capacitance. In ASTTL, improved propagation time must be realized by decreaseing the parasitic capacitance, as the resistance of ASTTL is set at 2 to 3 times larger than that of STTL.

The following processes are employed in ASTTL to reduce parasitic capacitance:

- Saturation control with Schottky barrier diodes.
- Oxide film separation.
- Finer patterns.

The processing of ASTTL and ALSTTL are almost the same, but finer patterns have been developed for ASTTL. The minimum size of the ASTTL pattern is 2μm.

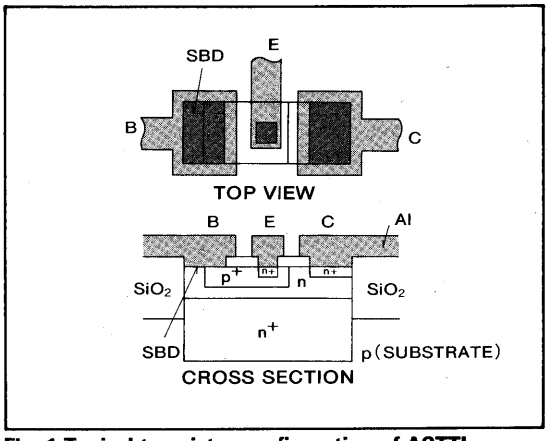


Fig. 1 Typical transistor configuration of ASTTL

2. Basic Circuitry

ASTTL circuitry is similar to ALSTTL, but has been improved in several ways to cope with the problems that occur during high-speed operation.

The basic ASTTL circuit is shown in Fig. 2.

The basic configuration using $T_1 \sim T_8$ and $D_1 \sim D_4$ is the same as that of ALSTTL.

If input A or B is lower than the threshold voltage V_T, the current from R_1 flows into T_1 or T_2, turning T_3, T_4 and T_7 off while turning T_5 and T_6 on and the output is high-level. If both A and B are larger than V_T, the current

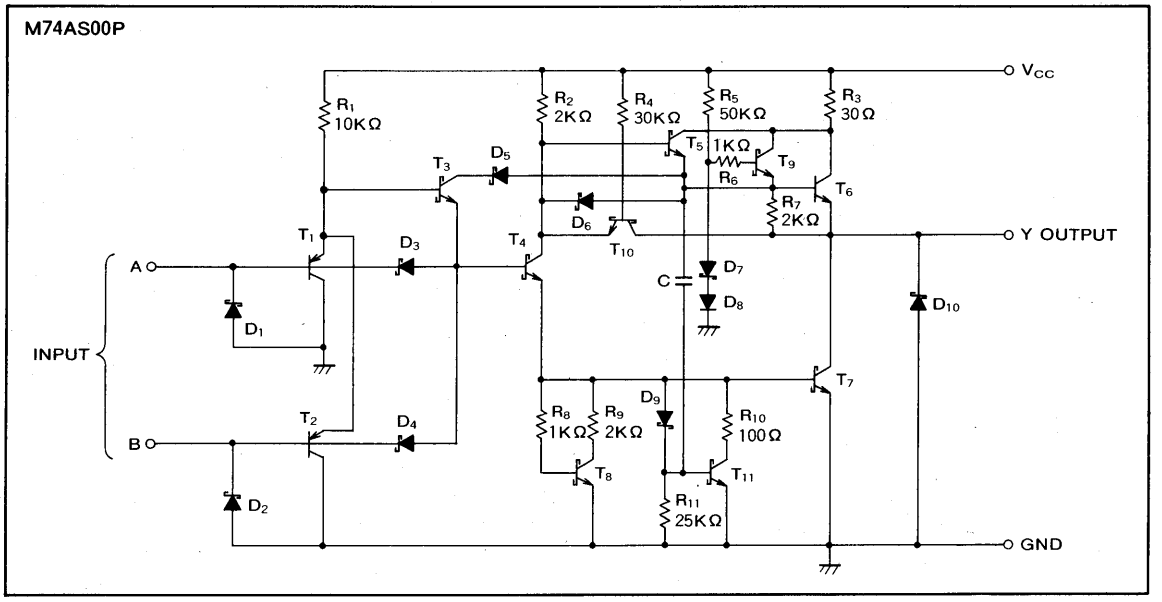


Fig. 2 Basic circuit of the ASTTL M74AS00P series (2 input NAND gate)

from R_1 flows into T_3, T_4 and T_7, turning T_3, T_4 and T_7 on while turning T_5 and T_6 off, and the output is low-level. D_3 and D_4 are Schottky barrier diodes to discharge the base charge of T_4 when the input changes from high-level to low-level, and R_8, R_9, T_8 are circuits to discharge base charge of T_7 when the input changes from high-level to low-level.

D_6, D_9, R_{10}, R_{11}, C and T_{11} are called a "Miller Killer" and form a circuit to decrease the penetrating current. In circuits without Miller Killers, penetrating currents usually flow when the output changes from low-level to high-level. In this case, T_7 turns off slowly while T_6 turns on rather fast, so that momentarily both T_6 and T_7 are on at the same time, allowing a large penetrating current to flow from V_{CC} to GND through R_3, T_6 and T_7. One of the biggest factors that hinders T_7 from turning off is the so-called Miller capacitance between base and collector of T_7. The current flows to the base of T_7 through this capacitance when the output changes from low-level to high-level, keeping T_7 on as the base current of T_7.

Miller Killers are circuits to prevent such Miller effects by turning T_7 off quickly. When T_4 turns off and T_5 turns on, a current from R_3 flows to T_5, C, and T_{11}, turning on T_{11}. T_{11} discharges the base load of T_7, like T_8. But as R_{10} is small, a large current can flow, turning off T_7 quickly and completely. D_9 is used to prevent the base potential of T_{11} from dropping excessively when T_4 is turned on and the current flows through the loop of C, D_6, T_4, and D_9. T_9, R_6, R_5, D_7 and D_8 form a circuit to recover the output voltage after undershoot. If the output voltage decreases to lower than −0.2V, the current from R_5 flows to R_6, T_9 and T_6, turning T_6 on and outputting a large current to quickly recover the output from undershoot.

R_4 and T_{10} increase the collector current of T_4 and turn on T_7 quickly. After T_7 turns on, they increase the base current of T_7 to quickly discharge the load capacitor. D_5 increases the collector current of T_3 and turns on T_4 quickly.

Next, we will observe the relations between some of the electrical characteristics and the circuit. The use of PNP inputs lower the low-level input current to −0.1mA typ., allowing easy drive by LSTTL or ALSTTL.

The threshold voltage V_T is derived from the following formula.

$$V_T = V_{BE}(T_7) + V_{BE}(T_4) + V_{BE}(T_3) - V_{EB}(T_1, T_2) \quad \cdots\cdots (1)$$

where $V_{BE}(T_7)$: Base-emitter voltage of T_7
$V_{BE}(T_4)$: Base-emitter voltage of T_4
$V_{BE}(T_3)$: Base-emitter voltage of T_3
$V_{EB}(T_1, T_2)$: Emitter-base voltage of T_1 or T_2

Formula (1) is exactly the same as that for ALSTTL, but the value of V_{BE} and V_{EB} is larger and the threshold voltage is proportionally higher due to the bigger current of ASTTL compared with ALSTTL. Fig. 3 compares input vs. output voltage characteristics of TTL, LSTTL, ALSTTL and ASTTL, and Fig. 4 shows temperature-dependent input vs. output voltage characteristics.

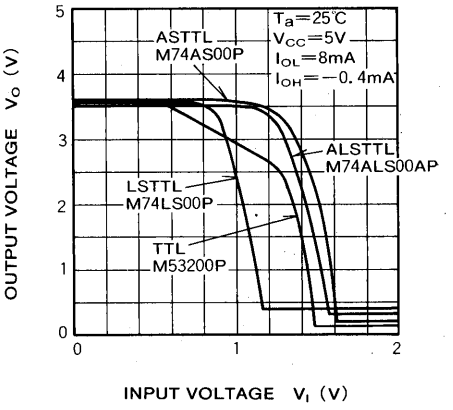


Fig. 3 Input vs. output voltage characteristics (M53200P, M74LS00P, M74ALS00AP, M74AS00P)

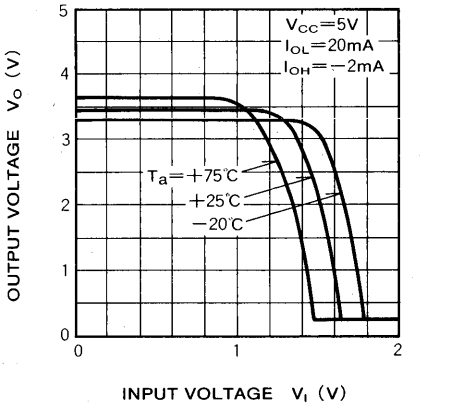


Fig. 4 Temperature-dependent input vs. output voltage characteristics (M74AS00P)

The output is characterized by low impedance, as is apparent from the small value of R_3. As the output impedance is lower than LSTTL, ALSTTL and STTL, capacitive loads can be charged or discharged quickly, while undershoot, overshoot, or power-supply spike currents tend to be large. Although power-supply spike currents due to penetrating currents are reduced considerably by the Miller Killers, and clamp diodes are attached to the input and output to prevent undershoot saturation, enough care should be taken when using these ICs.

3. Electrical characteristics

Table 1 shows the electrical characteristics of Mitsubishi standard bipolar logic in each series.

As is shown in Table 1, the speed of ASTTL is very high and the output current is large. On the other hand,

since the output voltage and input current do not differ much from those of LSTTL, ASTTL can be easily connected to the LSTTL or ALSTTL.

The DC electrical characteristics and switching characteristics of these devices are guaranteed at supply voltages of $V_{CC} = 5V + 10\%$ and operating ambient temperatures of $T_{opr} = -20 \sim +75℃$. We hope them to be easy to use and satisfying for customers with this wide range of guarantee.

Table 1 Electrical characteristics comparison of Mitsubishi Standard bipolar-logic ICs

Parameter \ Series name		ASTTL (M74AS00P)	ALSTTL (M74ALS00AP)	LSTTL (M74LS00P)	TTL (M53200P)
Propagation time (typical) (Note 1)	t_{PLH}	2.3ns	5ns	6ns	12ns
	t_{PHL}	1.7ns	3ns	6ns	8ns
Power dissipation (typical)	P_d	8mW/Gate	1.25mW/Gate	2mW/Gate	10mW/Gate
Threshold voltage (typical)	V_T	1.5V	1.4V	1.1V	1.4V
High-level output current (maximum)	I_{OH}	−2mA	−0.4mA	−0.4mA	−0.4mA
Low-level output current (maximum)	I_{OL}	20mA	8mA	8mA	16mA
High-level output voltage (minimum)	V_{OH}	V_{CC}−2V	V_{CC}−2V	2.7V	2.4V
Low-level output voltage (maximum)	V_{OL}	0.5	0.4V/0.5V	0.4V/0.5V	0.4V
High-level input current (maximum)	I_{IH}	20μA	20μA	20μA	40μA
Low-level input current (maximum)	I_{IL}	−0.5mA	−0.1mA	−0.4mA	−1.6mA
Operating supply voltage	V_{CC}	4.5~5.5V	4.5~5.5V	4.75~5.25V	4.75~5.25V
Conditions for guaranteed propagation performance	T_a	−20~+75℃	−20~+75℃	25℃	25℃
	V_{CC}	4.5~5.5V	4.5~5.5V	5V	5V
	C_L	50pF	50pF	15pF	15pF

Note 1. All typical values are at V_{CC}=5V, T_a=25℃, C_L=15pF.

DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

INTRODUCTION

This section will serve to define and describe those important specifications which must be observed in using ASTTL and to provide information on test methods for these ratings and standard characteristics of the basic gate circuits.

1. ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are the maximum ratings which should not be exceeded for the devices' reliability. When there are several ratings, none should be exceeded, even momentarily. If the device is used beyond these ratings, reliability will be significantly lowered and the IC may be destroyed. The following types of absolute maximum ratings are specified.

(1) Supply voltage (V_{CC})
(2) Input voltage (V_I)
(3) Output voltage (V_O)
(4) Operating temperature range (T_{opr})
(5) Storage temperature range (T_{stg})

Particular care is required with respect to these ratings as exceeding even one of these could cause IC damage.

1-1 Supply voltage (V_{CC})

This rating indicates the maximum value of supply voltage that may be applied to the V_{CC} terminal. This value is also applied to the maximum value of surge voltage under unusual conditions. If voltage beyond this rating is applied, the IC may either be destroyed or its reliability significantly deteriorated.

1-2 Input voltage (V_I)

This rating indicates the maximum value of input voltage that may be applied. Exceeding this value may cause the transistors and diodes in the input circuit to be destroyed and the IC made useless.

1-3 Output voltage (V_O)

This rating indicates the maximum value of voltage that can be applied to the output when the output is high-level. When the device has open collector outputs, this value indicates the breakdown voltage of the output transistor.

1-4 Operating temperature range (T_{opr})

This rating indicates the temperature range in which the device can be operated with all electrical specifications satisfied and full function. The ASTTL is guaranteed over a broad temperature range of −20~+75℃.

1-5 Storage temperature range (T_{stg})

This rating indicates the temperature range in which the IC may be stored without either voltage or current applied. This should not be exceeded in storage nor transport (particularly for transport by air).

2. RECOMMENDED OPERATING CONDITIONS

In recommended operating conditions we specify supply voltage and input/output conditions required for the guaranteed performance of the device.

2-1 Supply voltage (V_{CC})

This rating specifies the permissible supply voltage range. Normally, optimum supply voltage is 5V in TTLs. The permissible supply voltage range of the ASTTL has a maximum value of 5.5V (V_{CCmax}) and a minimum value of 4.5V (V_{CCmin}).

2-2 High-level input voltage (V_{IH})

This rating specifies the voltage value applied to the input terminal when it is in high-level conditions. The minimum value is specified for TTLs, while the maximum value is the absolute maximum rating of the input voltage. The minimum value is sometimes referred to as V_{IH}.

2-3 Low-level input voltage (V_{IL})

This rating specifies the voltage value applied to the input terminal when it is in low-level condition. The maximum value is specified for TTLs. This maximum value is sometimes referred to as V_{IL}.

2-4 High-level output current (I_{OH})

The meaning of high-level output current differs depending on whether the type of output is active pull-up or open collector.

When the output is an active pull-up, then high-level output current is the stipulated maximum value of the current that can be output from the output terminal with the high-level voltage guaranteed when the output is high-level.

This value is related to the number of inputs that can be driven by one output when that output is high-level. For details, see the section entitled "PRECAUTIONS FOR USE."

When the output is an open collector, I_{OH} is the maximum current guaranteed in the "ELECTRICAL CHARACTERISTICS." See 4-3.

2-5 Low-level output current (I_{OL})

Low-level output current is the stipulated maximum value of current that may be applied to the output terminal with low-level output voltage guaranteed when the output is low-level. This value is related to the number of inputs that can be driven by one output when that output is low-level. For details, see the section entitled "PRECAUTIONS FOR USE."

3. FUNCTIONS

The functions of devices are specified by either a function table or timing diagrams. A check of functions is undertaken with the supply voltage at V_{CCmax} and

DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

V_{CCmin}, the input voltage set to V_{IL} and V_{IH}, signals applied to the input terminal according to either the function table or the timing diagram, and the criterion V_{OL} and V_{OH} used for observation of the output.

4. ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed within the specified temperature range and supply voltage range of V_{CCmin} to V_{CCmax}. The test methods are specified to realize the worst case to guarantee the ratings.

4-1 Input clamp voltage (V_{IC})

This specifies the voltage at input terminal when a specified current is applied to the terminal. This voltage is the forward voltage drop of the clamp diode connected between the input and GND. With supply voltage set at V_{CCmin} and all other input terminals open, clamp voltage V_{IC} is measured when specified current I_{IC} is applied to the input terminal.

4-2 High-level output voltage (V_{OH})

This specification is applicable to ICs with active pull-up outputs.

This specifies the minimum value of voltage guaranteed in an output terminal of high-level. With input conditions set so that output becomes high-level, V_{OH} is the voltage when load current I_{OH} flows from the output terminal.

4-3 High-level output current (I_{OH})

This specification is applicable to ICs with open collector outputs.

This is the maximum value of current that flows into the output terminal when output voltage V_{OH} is applied to the output terminal and the output is high-level. Supply voltage is set V_{CCmin} at this time.

4-4 Low-level output voltage (V_{OL})

This specifies the voltage value guaranteed for an output pin in low-level. The supply voltage is set at V_{CCmin} and a load current of I_{OL} is applied.

4-5 Off-state high-level output current (I_{OZH})

This specification is applicable to ICs with 3-state outputs.

This specifies the maximum value of current that flows into the output terminal when the output is in high-impedance state and the minimum value of high-level output voltage is applied to it. At this time, supply voltage is set V_{CCmax} and the input conditions are set so that the output will become low-level when it gets out of the high-impedance state.

4-6 Off-state low-level output current (I_{OZL})

This specification is applicable to ICs with 3-state output.

This specifies the maximum value of current that flows out from the output terminal when the output is in high-impedance state and the maximum value of low-level output voltage is applied to the output terminal. At this time, supply voltage is set V_{CCmax} and the input conditions are set so that the output will become high-state when it gets out of the high-impedance state.

4-7 Input current at maximum voltage (I_I)

This specifies the input current when the maximum input voltage as specified in the absolute maximum ratings is applied to the input and supply voltage set at V_{CCmax}. Input terminals, other than the one being measured, are set to 0V.

4-8 High-level input current (I_{IH})

This specifies the input current when a high-level output voltage is applied to the input terminal. With supply voltage set to V_{CCmax}, the high-level voltage applied to the input is set to the minimum value of LSTTL high-level output voltage (2.7V). Input terminals, other than the one being measured, are set to 0V.

4-9 Low-level input current (I_{IL})

This specifies the input current when a low-level output voltage of LSTTL is applied to the input terminal. With supply voltage set to V_{CCmax}, the low-level voltage applied to the input is set to the maximum value (0.4V) of low-level voltage. Input terminals, other than the one being measured, are set to 4.5V.

4-10 Output current (I_O)

This specification is applicable to ICs with active pull-up outputs.

This specifies the current flowing from the output when 2.25V is applied to the output terminal and the output is high-level. With supply voltage set to V_{CCmax}, either 0V or 4.5V is applied to the inputs so that the output transistor becomes completely off.

This specification is given to test the ability to charge parasitic capacitances in wiring.

4-11 Supply current, outputs high (I_{CCH})

This specifies the current flowing into the supply terminal when the outputs are high-level. With supply voltage set to V_{CCmax}, an input voltage of either 0V or 4.5V is applied setting the output to high-level. All circuits within the IC are set to the above conditions and measured at the same time. Supply current is expressed as the entire IC unit.

4-12 Supply current, outputs low (I_{CCL})

This specifies the current flowing into the supply terminal when the ouputs are low-level. With supply voltage set to V_{CCmax}, an input voltage of either 0V or 4.5V is applied setting the output to low-level. All circuits within

the IC are set to the above condition and measured at the same time.

4-13 Supply current, outputs disabled (I_{CCZ})
This specifies the current flowing into the supply terminal when the outputs are in high-impedance state. With supply voltage set to V_{CCmax}, an input voltage of either 0V or 4.5V is applied setting the output to high-impedance. All circuits within the IC are set to the above condition and measured at the same time.

4-14 Supply current (I_{CC})
I_{CC} is calculated using the following formula where I_{CCH} and I_{CCL} are specified.

$$I_{CC}=\frac{I_{CCH}+I_{CCL}}{2}$$

For ICs without specified I_{CCH} and I_{CCL} values, the value of I_{CC} is specified as the maximum value of current that flows into the supply terminal.

4-15 Positive-going threshold voltage (V_{T+})
This specifies the level of input voltage at the point where the output state changes when the input voltage has increased from a level lower than negative-going threshold level V_{T-}. Depending on the type of device, supply voltage is either 5V or V_{CCmin} at this measurement.

4-16 Negative-going threshold voltage (V_{T-})
This specifies the level of input voltage at the point where the output state changes when the input voltage has decreased from a level higher than the positive-going threshold level V_{T+}. Depending on the type of device, supply voltage is either 5V or V_{CCmin} at this measurement.

4-17 Hysteresis ($V_{T+}-V_{T-}$)
This specifies the difference between positive-going threshold voltage (V_{T+}) and negative-going threshold voltage (V_{T-}). Depending on the type of device, supply voltage is either 5V or V_{CCmin} at this measurement.

5. SWITCHING CHARACTERISTICS
Propagation time, maximum clock frequency and output pulse width are specified in Switching characteristics within $V_{CC}=4.5\sim5.5V$, $Ta=0\sim70℃$ or $Ta=-20\sim+75℃$. The measurements are made with the specified loads connected to the outputs and with the input pulse specified in the low-level voltage V_{IL}, the high-level voltage V_{IH}, the repetitive frequency of PRR, the pulse width of t_W, rise time t_r and fall time t_f.

5-1 Propagation time, low-to-high-level output (t_{PLH})
This specifies the length of time from when the input changes to when the output changes from low-level to high-level. The moment when they changes are specified with the reference voltage level. (See §7-2, 7-3.)

5-2 Propagation time, high-to-low-level output (t_{PHL})
This specifies the length of time from when the input changes to when the output changes from high-level to low-level. The moment when they changes are specified with the reference voltage level. (See §7-2, 7-3.)

5-3 Output enable time to high-level (t_{PZH})
This specification is applicable to ICs with 3-state outputs.

This specifies the length of time from when the input changes to when the output changes from high-impedance state to high-level. The moment when they changes are specified with the reference voltage level. (See §7-2, 7-3.)

5-4 Output enable time to low-level (t_{PZL})
This specification is applicable to ICs with 3-state outputs.

This specifies the length of time from when the input changes to when the output changes from high-impedance state to low-level. The moment when they changes are specified with the reference voltage level. (See §7-2, 7-3.)

5-5 Output disable time from high-level (t_{PHZ})
This specification is applicable to ICs with 3-state outputs.

This specifies the length of time from when the input changes to when the output changes from high-level to high-impedance state. The moment when they changes are specified with the reference voltage levels. (See §7-2, 7-3.)

5-6 Output disable time from low-level (t_{PLZ})
This specification is applicable to ICs with 3-state outputs.

This specifies the length of time from when the input changes to when the output changes from low-level to high-impedance state. The moment when they changes are specified with the reference voltage levels. (See §7-2, 7-3.)

5-7 Maximum clock frequency (f_{MAX})
This specification is applicable to flip-flops or MSIs including flip-flop circuits.

The maximum clock frequency is defined as the highest frequency at which the clock input can be driven through its required sequence while maintaining stable transitions of logic level at the output with other inputs set to cause changes of output logic level in accordance with the specifications. (See §7-2.)

5-8 Output pulse width (t_{WQ})
This specification is applicable to monostable multivib-

rators.

This specifies the width of the pulse appearing at the output at specified reference voltage, when a trigger pulse is applied with specified resistors and capacitors connected to the timing inputs.

6. TIMING REQUIREMENTS

These specifications are applicable to flip-flops and MSIs including flip-flop circuits.

These specify the input timing requirements which must be met to maintain a stable output change in the required sequence when input signals such as clock and reset change.

Timing requirements are specified at an ambient temperature of $T_a = 0 \sim 70℃$ or $T_a = -20 \sim +75℃$, a supply voltage of $V_{CC} = 4.5 \sim 5.5V$, and include pulse width, setup time, hold time, rise time and fall time.

6-1 Pulse width (t_w)

This specification is applicable to flip-flops and MSIs including flip-flop circuits.

This requirement specifies the minimum time between the leading edge and the trailing edge (using specified reference voltage level) of the input pulse waveform. If a pulse of a shorter width is applied, the signal may not only be invalid but also cause a misoperation. (See §7-2, 7-3.)

6-2 Setup time (t_{su})

This specification is applicable to flip-flops and MSIs including flip-flop circuits.

With such ICs, it is necessary to set up the input condition some time before the change of a control input such as the clock input in order to ensure proper recognition of the input signal. This time length is setup time.

Setup time is the length from the set up to the active edge of the control input. The set up and active edge are specified with the reference voltage level.

Negative setup times indicate that the input conditions may be set up after the active edge of the control inputs. (See §7-2, 7-3.)

6-3 Hold time (t_h)

This specification is applicable to flip-flops and MSIs including flip-flop circuits.

With such ICs, it is necessary to maintain the input condition some time after the change of a control input such as the clock input in order to ensure proper recognition of the input signal. This time length is hold time. Hold time is specified in the same manner as setup time.

Negative hold times indicate that the input conditions may be changed before the active edge of the control inputs. (See §7-2, 7-3.)

6-4 Clock risetime (t_r)

This specifies the maximum length of time for the clock input to change from 0.6V to 3.2V. Misoperation may occur when a clock pulse with a risetime greater than this value is applied.

6-5 Clock falltime (t_f)

This specifies the maximum length of time for the clock input to change from 3.2V to 0.6V. Misoperation may occur when a clock pulse with a falltime greater than this value is applied.

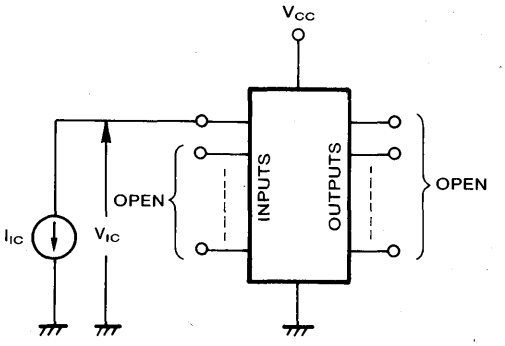
7. TEST CIRCUITS

This section includes typical test circuits for each characteristic. For complicated measurements of such devices as MSIs, refer to the detailed descriptions in the individual data sheets.

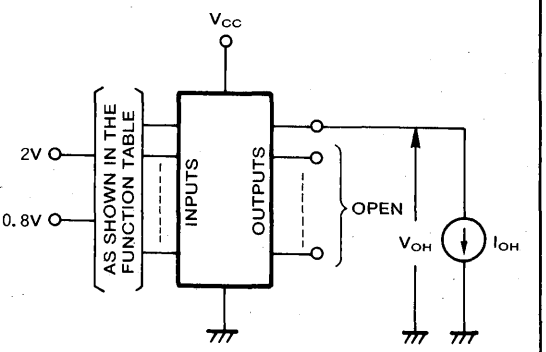
DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

7-1 Circuits for measuring direct current characteristics

V_{IC} MEASUREMENT

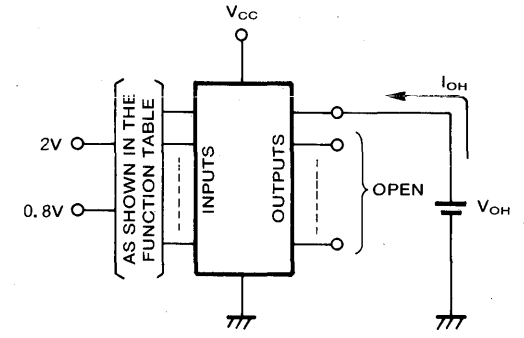


V_{OH} MEASUREMENT



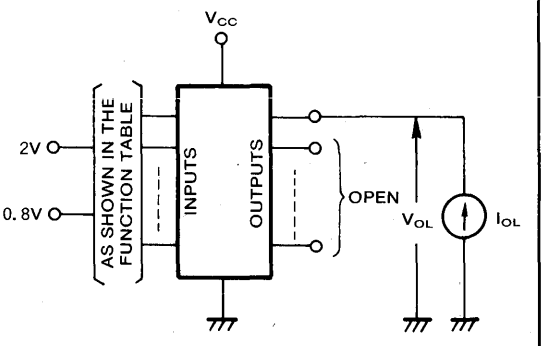
- Input conditions set so that output becomes high-level

I_{OH} MEASUREMENT



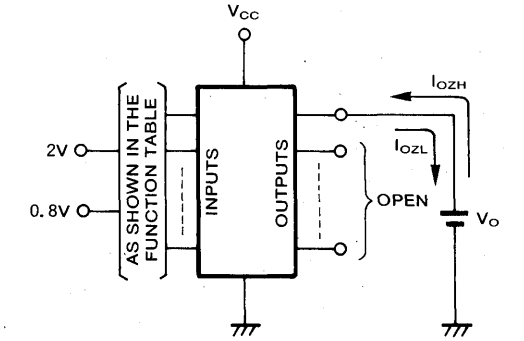
- Input conditions set so that output becomes high-level

V_{OL} MEASUREMENT



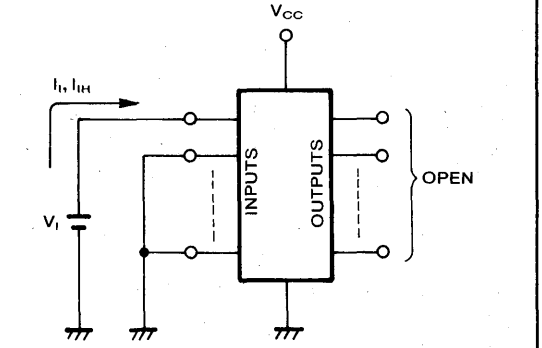
- Input conditions set so that output becomes low-level

I_{OZH}, I_{OZL} MEASUREMENTS



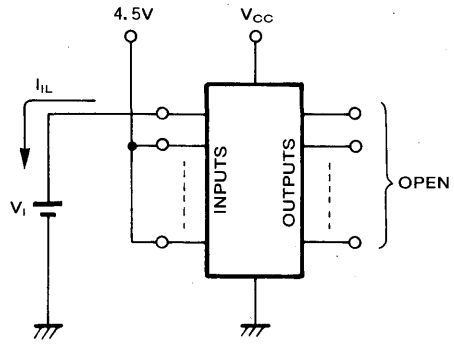
- Input conditions set so that output becomes high-impedance state

I_I, I_{IH} MEASUREMENTS

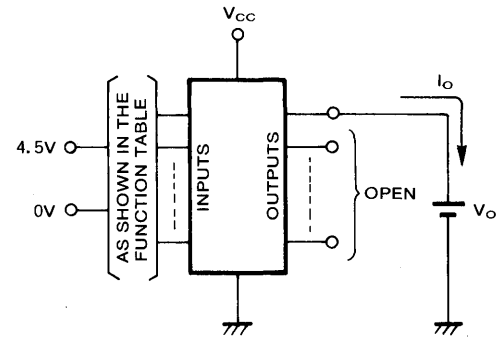


DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

I_{IL} MEASUREMENT

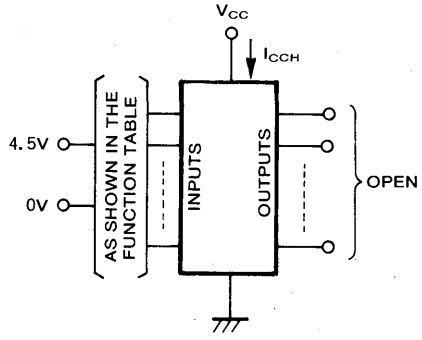


I_O MEASUREMENT



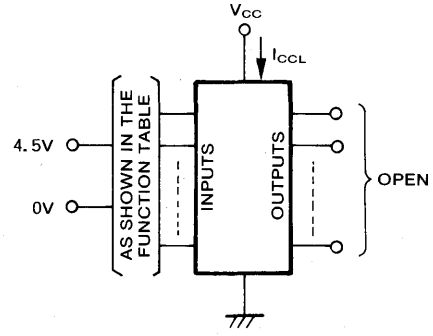
- Input conditions set so that output becomes high-level

I_{CCH} MEASUREMENT



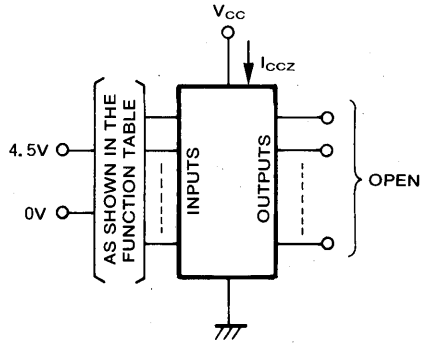
- Input conditions set so that all outputs become high-level

I_{CCL} MEASUREMENT



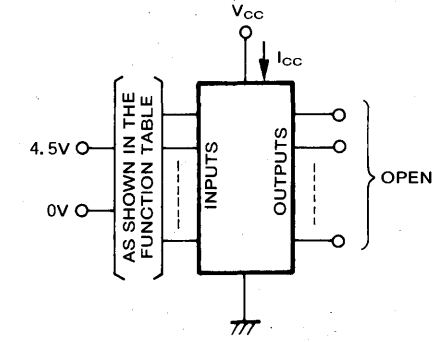
- Input conditions set so that all outputs become low-level

I_{CCZ} MEASUREMENT



- Input conditions set so that all outputs become high-impedance state

I_{CC} MEASUREMENT

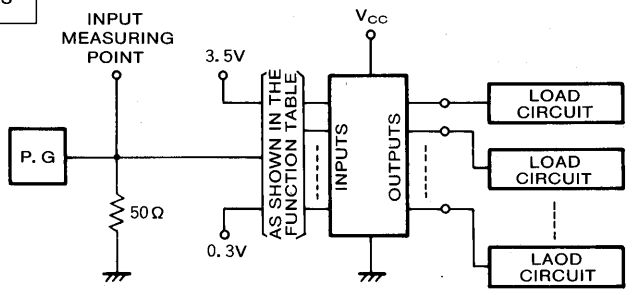


- Input conditions are specified in individual specifications. When no specification is given, I_{CC} is guaranteed in all possible input conditions.

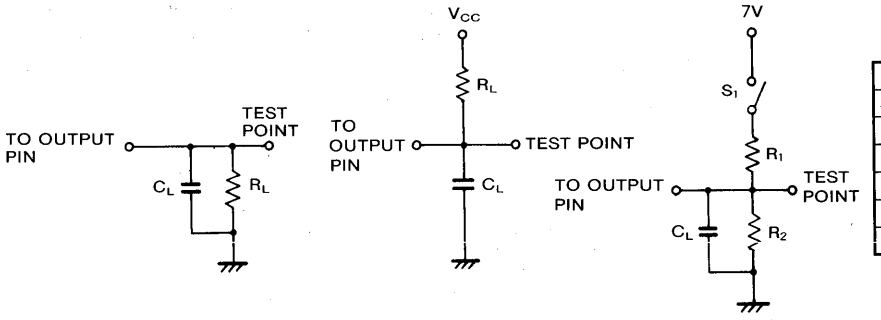
DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

7-2 Circuits for measuring switching characteristics

SWITCHING MEASUREMENTS



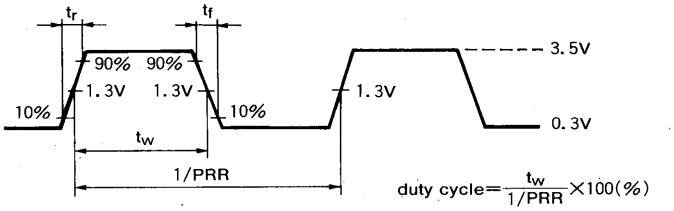
Note 1. The load circuit varies as shown in the following diagrams according to the type of IC output.
C_L includes probe and jig capacitance.



Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

(a) Active pull-up output (b) Open collector output (c) 3-state output

Note 2. The pulse generator (PG) has the following characteristics:



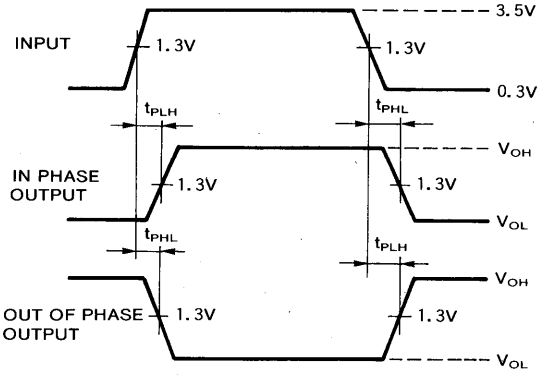
Pulse repetition rate : PRR≦1MHz
Risetime : t_r=2ns
Falltime : t_f=2ns
Duty cycle : duty cycle=50%
Output impedance : Z_O=50Ω

MITSUBISHI ELECTRIC

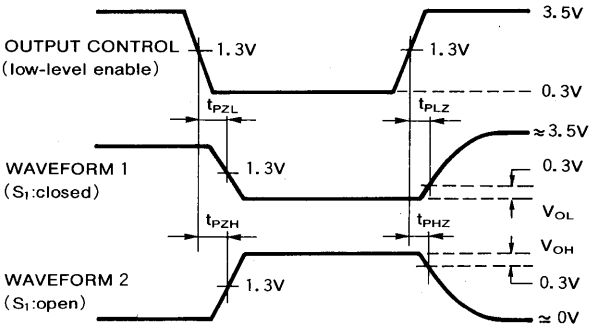
7-3 Timing diagram

Switching time measurement

1. Propagation time



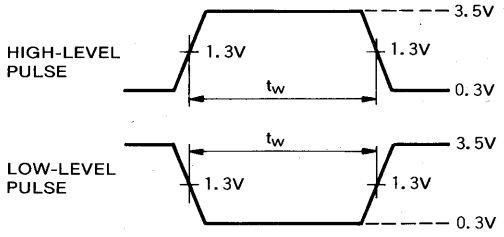
2. Enable and disable time



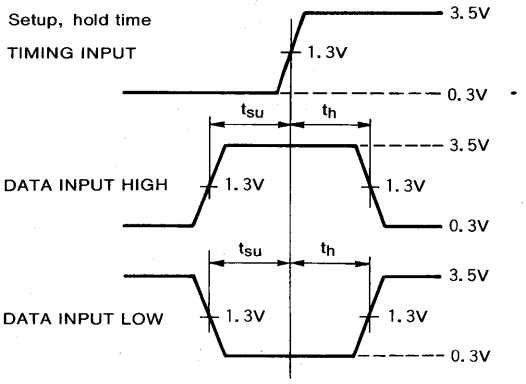
Waveform 1: The input conditions are set so that the output becomes low when enabled.
Waveform 2: The input conditions are set so that the output becomes high when enabled.

Timing Requirements

1. Pulse width

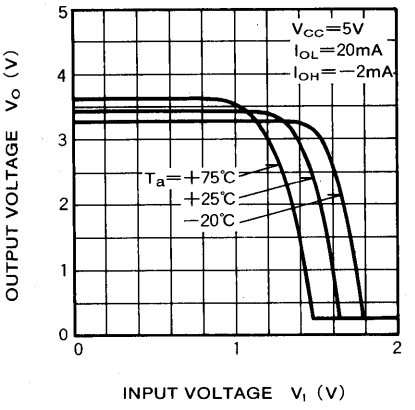


2. Setup, hold time

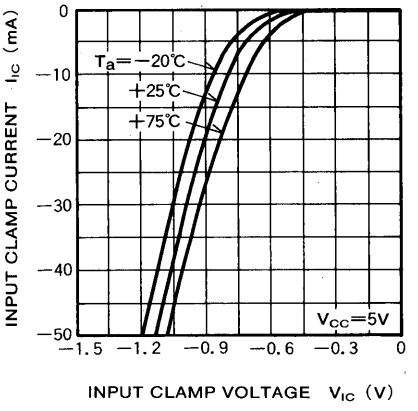


8. TYPICAL CHARACTERISTICS OF BASIC GATE

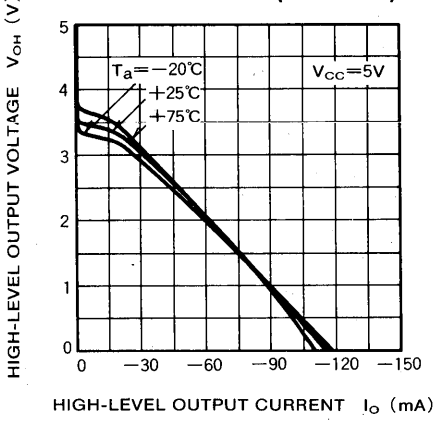
INPUT VS. OUTPUT VOLTAGE CHARACTERISTICS (M74AS00P)



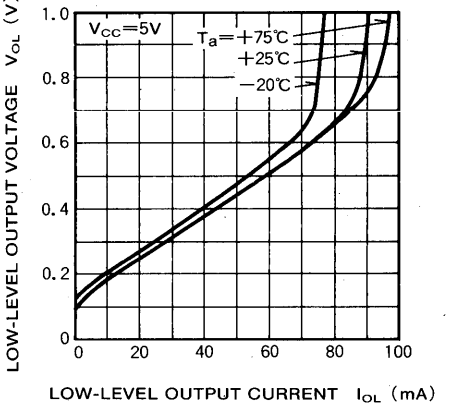
INPUT CLAMP CURRENT VS. INPUT CLAMP VOLTAGE



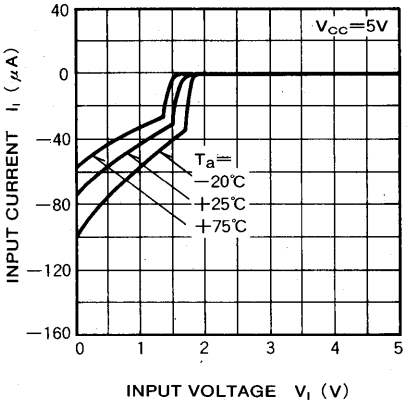
OUTPUT VOLTAGE VS. HIGH-LEVEL OUTPUT CURRENT (M74AS00P)



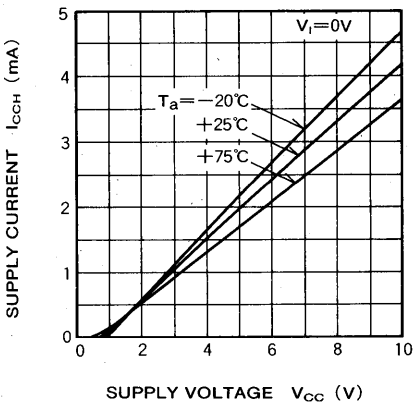
LOW-LEVEL OUTPUT VOLTAGE VS. LOW-LEVEL OUTPUT CURRENT (M74AS00P)



INPUT CURRENT VS. INPUT VOLTAGE (M74AS00P)

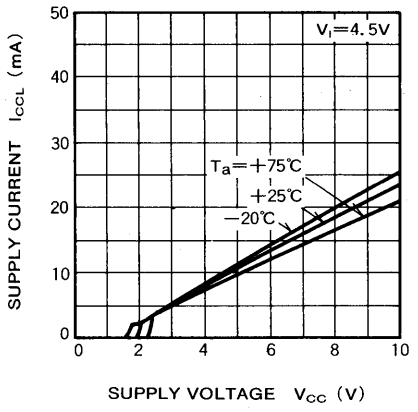


SUPPLY CURRENT VS. SUPPLY VOLTAGE, OUTPUT HIGH (M74AS00P)

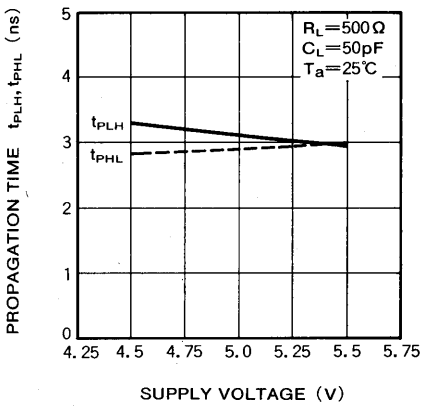


DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

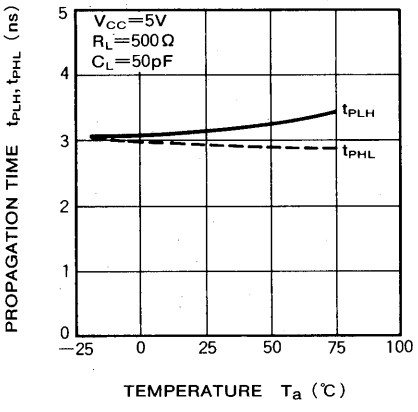
SUPPLY CURRENT VS. SUPPLY VOLTAGE, OUTPUT LOW (M74AS00P)



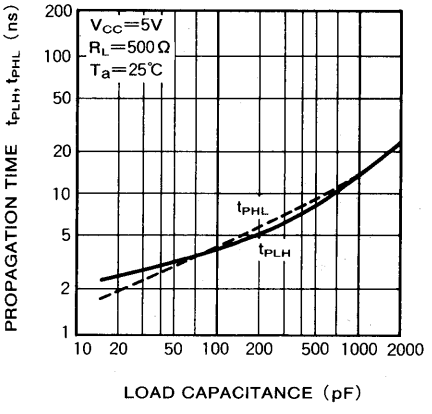
PROPAGATION TIME VS. SUPPLY VOLTAGE (M74AS00P)



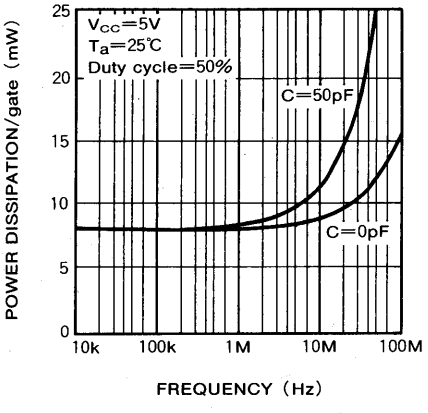
PROPAGATION TIME VS. FREE-AIR TEMPERATURE (M74AS00P)



PROPAGATION TIME VS. LOAD CAPACITANCE (M74AS00P)



POWER DISSIPATION VS. FREQUENCY (M74AS00P)



QUALITY ASSURANCE AND RELIABILITY TESTING

In recent years, advances in integrated circuits have been rapid, with increasing density and speed accompanied by decreasing cost. Because of these advances, it is now practical and economically justifiable to use these devices in systems of greater complexity and in which they were previously considered too expensive. All of these advances add up to increased demand.

We at Mitsubishi foresaw this increased demand and organized our production facilities to meet it. We also realized that simply increasing production to meet the demand was not enough and that positive steps would have to be taken to assure the reliability of our products.

This realization resulted in the development of our Quality Assurance System. The system has resulted in improved products, and Mitsubishi is able to supply its customers' needs with ICs of high reliability and stable quality. This system is the key to future planning for improved design, production and quality assurance.

1. QUALITY ASSURANCE SYSTEM

The Quality Assurance System imposes quality controls on Mitsubishi products from the initial conception of a new product to the final delivery of the product to the customer. A diagram of the total system is shown in Fig. 1. For ease of understanding, the system is divided into three stages.

1-1 Quality Assurance in the Design Stage

The characteristics of the breadboard devices are carefully checked to assure that all specifications are met. Standard integrated circuits and high-quality discrete components are used. During the design stage, extensive use is made of a sophisticated CAD program, which is updated to always include the latest state-of-the-art techniques.

1-2 Production Quality Assurance

Production quality is assured by both management and inspection of the devices.

(1) Environmental control.
(2) Scheduled periodic test and maintenance of design, tools, and test equipment.
(3) Control of ordered materials.
(4) Manufacturing process control.
(5) In-line evaluation: at wafer processing and assembly stages.
(6) Final production inspection: An inspection of the completed device consisting of an external inspection of the device's external measurements, its construction, and an inspection of its electrical characteristics.
(7) Product quality inspection: A final inspection consisting of three groups is undertaken in order to determine whether or not the stock products will meet user's needs.

Group A: Inspection of the device externally, its markings, and its electrical characteristics.

Group B: Inspection of the device environmentally, mechanically, and in terms of life expectancy.

Group C: A reliability test is periodically made from a sampling of lots that pass group A and B tests. This test is conducted every few months to inspect the environmental and mechanical performance and life expectancy of the devices.

1-3 Procedure for Determining the Reliability from Development and Preproduction to Mass Production

Evaluation of reliability described in 1-1 and 1-2 occurs at three levels of production: development, preproduction, and mass production. Once a product passes the development stage inspection, it proceeds to the next level, preproduction, where a limited number of devices are produced and again checked at this level. Upon passing this test, mass production begins and the above-mentioned quality assurance evaluation is undertaken to guarantee quality and reliability.

2. Reliability Control

2-1 Reliability Evaluation

Evaluation of reliability is based internationally on IEC standards for electronics devices and nationally on the RCJ (Reliability Center for Electronics Components of Japan). Mitsubishi Electric has chosen for the standard of its testing MIL-STD-883 and EIAJ-IC-121, outlined below in Table 1.

Table 1 Typical reliability test items and conditions

Group	Item	Test condition
1	High temperature operating life	Maximum operating ambient temperature 1000h
	High temperature storage life	Maximum storage temperature 1000h
	High temperature, high humidity with bias	85℃, 85%RH, V_{CC}=5.5V
2	Soldering heat	260℃, 10s
	Thermal shock	0~100℃ 15 cycles, 10min/Cycle
	Temperature cycling	Minimum to maximum storage temperature. 1hr/cycle
3	Solderability	230℃, 5s, use rosin flux
	Lead integrity	Tension: 340g, 30s Bending stress: 250g, 90°, 3 times
	Vibration	20G, X, Y, Z each direction, 4 times 100~200Hz, 4min/cycle
	Drop test	75cm, 3 times, wooden board, Y_1 direction
	Constant acceleration	20000G, Y_1 direction, 1 min

2-2 Failure Analysis

Devices that have failed during reliability or acceleration tests are analyzed to determine the cause of failure. This information is fed back to the process engineering section and manufacturing section so that improvements can be made to increase reliability. A summary of failure analysis procedures is shown in Table 2.

3. RELIABILITY TESTS

The major failure standards for ASTTL reliability tests are shown in Table 3.

Table 2 Summary of failure analysis procedures

Step	Description
(1) External examination	○Inspection of leads, plating, soldering and welding ○Inspection of materials, sealing, package and marking ○Visual inspection of other items of the specifications ○Use of stereo microscopes, metallurgical microscopes, X-ray photographic equipment, fine leakage and gross leakage testers in the examination
(2) Electrical tests	○Checking for open circuits, short circuits and parametric degradation by electrical parameter measurement ○Observation of characteristics by a synchroscope or a curve tracer and checking of important physical characteristics by electrical characteristics ○Stress tests such as environmental or life test, if required
(3) Internal examination	○Removal of the cover of the device, the optical inspection of the internal structure of the device ○Checking of the silicon chip surface ○Measurement of electrical characteristics by probes, if applicable ○Use of SEM, XMA, and infrared microscanner, if required
(4) Chip analysis	○Use of metallurgical analysis techniques to supplement analysis of the internal examination ○Slicing for cross-sectional inspection ○Analysis of oxide film defects ○Analysis of diffusion defects

Table 3 Failure criteria for reliability test

Parameter		Minor failures		Major failures
		Lower limits	Upper limits	
DC current and voltage characteristics	High-level output voltage (V_{OH})	IVD×0.8	IVD×1.2	UCL or LCL For leakage current UCL×2
	Low-level output voltage (V_{OL})	IVD−0.1V	IVD+0.1V	
	High-level input current (I_{IH})	—	IVD×5	
	Low-level input current (I_{IL})	IVD×0.8	IVD×1.2	
	Output current (I_O)	IVD×0.8	IVD×1.2	
	High-level output current (I_{OH})	—	IVD×5	
Function		—		Short, open, abnormal functions
Appearance		—		Less than 95% soldered
Appearance		—		Lead breakdown

UCL: Upper condition limits LCL: Lower condition limits IVD: Initial values

We welcome and appreciate the cooperation of our customers in developing design specifications, establishing quality levels, controlling incoming inspections, developing assembly and adjusting processes and collecting field data. Mitsubishi is anxious to work with its customers to develop ICs of increased reliability that meet their requirements.

QUALITY ASSURANCE AND RELIABILITY TESTING

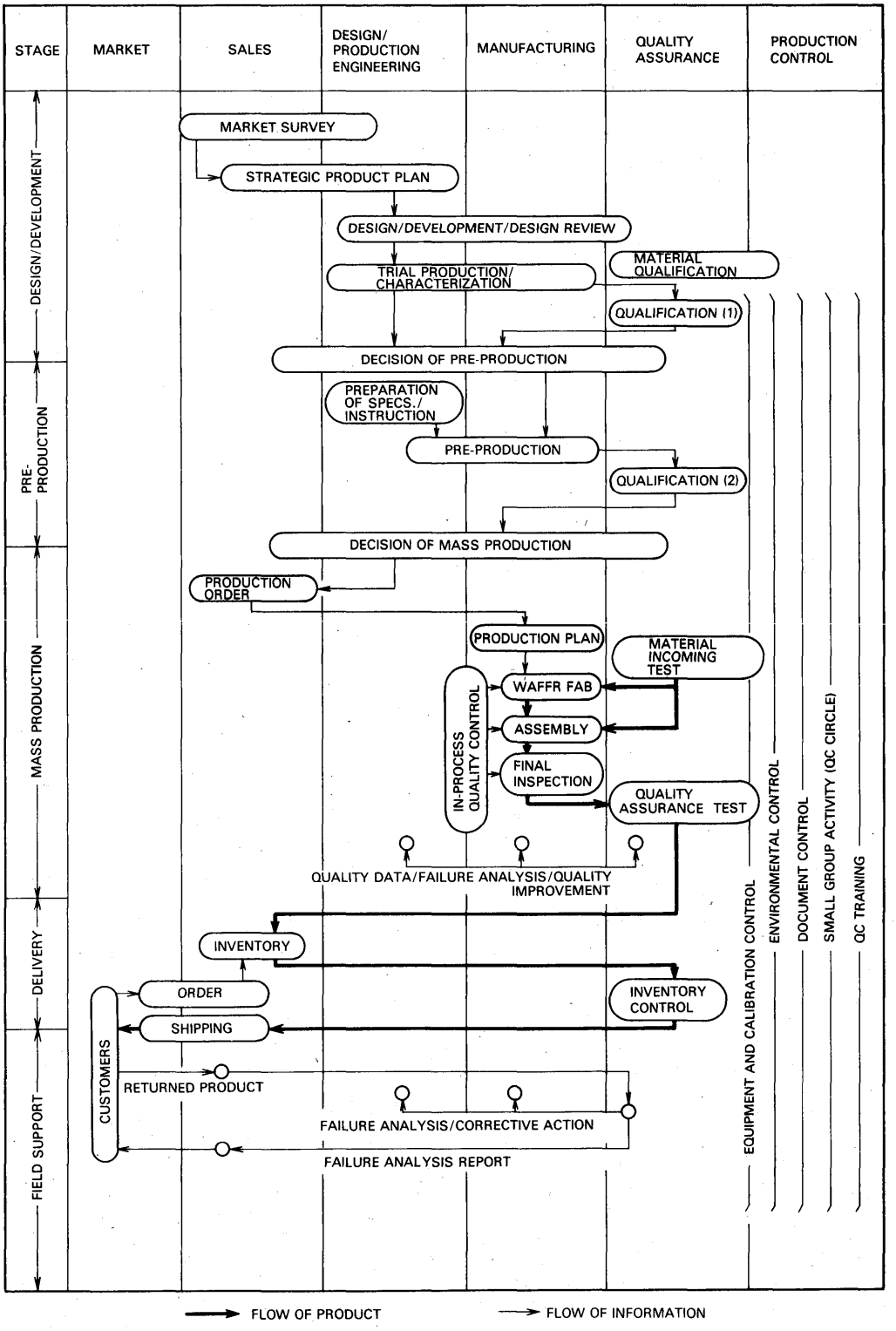


Fig. 1 Flow Chart of Quality Assurance Program

PRECAUTIONS FOR USE

1. INTRODUCTION

The handling of ASTTLs is basically the same as STTLs. However, ASTTLs have faster switching speed and higher input impedance. So, in logic design and system design, more care is required of noise, problems in application and wiring which may lower the reliability. Please read this section carefully.

2. PRECAUTIONS CONCERNING ICs

2-1 Supply voltage (V_{CC})

Absolute maximum ratings of supply voltage reflect the capacity of an IC in unusual conditions such as surge voltage and voltage spikes in transition. When supply voltages greater than these values are applied, excessive current may flow due to a breakdown in the device. This excessive current causes excessive heat, circuit destruction and fusing of internal wiring thus resulting in degradation in IC functions and reliability. It is urged that operation of the devices be conducted within the recommended supply voltage range of $V_{CC}=5V\pm10\%$ as functions and electrical characteristics are guaranteed only in this case.

2-2 Temperature range (T_{opr}, T_{stg})

Temperature range is specified in operating free-air ambient temperature range T_{opr} and storage temperature range T_{stg}. Generally speaking, T_{opr} standard for consumer and industrial use is $0\sim70℃$ while the standard for military use is $-55\sim+125℃$. In order to provide stable use of consumer and industrial equipments even in the winter season, Mitsubishi Electric has set a wide T_{opr} standard of $-20\sim+75℃$ over which functions and electrical characteristics are guaranteed. But of course, the best reliability is achieved when the devices are operated in the vicinity of 25℃. The higher and lower temperature portion of T_{opr} should be considered as a guarantee in unusual conditions caused by troubles in air-conditioners or cooling fans etc.

T_{stg} indicates the temperature range in which a device may be stored without causing characteristics degradation. This specification must be observed in device shipment and sotrage bacause a temperature in excess of these limits may cause drastic decrease in device reliability or damage of the device.

2-3 Input voltage (V_I)

The range of input voltage V_I is specified in the absolute maximum ratings. Destruction of input circuits may occur when a voltage exceeding this range is applied to the inputs. Most of Mitsubishi Electric's ASTTL devices have Schottky-barrier diodes and pnp transistors in their inputs with an upper V_I limit of 7V. The lower limit of V_I is $-0.5V$. When voltages less than this value are applied, parasitic transistors within the IC may operate causing malfunctions of the IC. This malfunction is less likely to occur in ASTTLs than LSTTLs because of their device structures. In normal use, ASTTLs are free from this malfunction.

2-4 Unused terminals

Terminals that are open operate as if a high-level input voltage is applied. However, it is recommended that a constant voltage with low impedance be applied to such open terminals because an IC lead tends to operate as an antenna picking up noise. This is especially true of clock, set and reset inputs of ICs with memory functions such as flip-flops, latches, counters and registers. In such cases, any operation caused by noise will result in false data written in the memory. Please connect unused inputs to V_{CC} line and the inputs that should be always low-level to GND line. Do not connect an unused input with another input of the same gate so that AC noise margin should not lower.

2-5 High-level input signals

High-level input voltage is effective from 2V to the upper limit of the absolute maximum rating for normal TTL ICs. In other words, voltage changes within the high-level range would not cause changes in output. As parasitic capacitance exists between the anode and cathode of Schottky barrier diodes in the input circuit of the ASTTL, when sharp ($\leqq5ns$) changes from a higher voltage to a lower voltage occur in the input, false waveforms may be generated in the output, even if the changes were within the high-level input voltage range. It is therefore important to avoid sharp changes of high-level input signal due to ringing, crosstalk and logical noise, even within the high-level input voltage range. When unused terminals are connected to the voltage supply line, ensure that voltage supply do not exceed $5V\pm10\%$ because false waveforms are also generated in the output when sharp changes occur in the supply voltage.

2-6 Risetime and falltime of input signals

Just as in STTLs, an oscillation in the tens of MHz occurs in the outputs of ASTTLs when a signal with a long risetime or falltime is applied to the input of a gate circuit. In MSIs, when such a signal is applied to the input, abnormal waveforms and misoperation occur. This is especially true for devices such as flip-flops, counters and shift registers that have the risetime and falltime specifications in the timing requirements. Since input waveforms having risetime or falltime greater than the specifications will result in misoperation, it is necessary to ensure that they be held within such limits. Even for devices without these specifications, it is necessary to limit the risetime and falltime of input signals to less than 50ns. Note that this does not hold true for devices such as Schmitt triggers that have hysteresis.

Such long risetime and falltime are often caused by a capacitor connected between an IC output and GND

line or transmission line and GND line. This capacitor may be used for preventing noise or generating either delayed pulses or differencial pulses. Such misoperation can be avoided by the use of a waveform shaper with a Schmitt trigger IC.

2-7 Timing requirements

These conditions give the input signal timing specifications necessary for the proper function of the IC. Devices with such requirements listed must be operated within the limits described to prevent malfunctions.

2-8 Parasitic elements

As shown in Fig. 1, the transistors and diodes that configure ASTTL and ALSTTL ICs have oxide films around them that are used to isolate the individual elements from each other. They also have a p-type domain in the substrate below them. This p-type domain is connected to the GND terminal. Between the GND terminal and the n-type domain that forms the collector of the transistor is formed a parasitic diode that is not shown on the circuit diagram and whose anode is connected to the GND terminal. Parasitic diodes are also connected between the GND terminal and voltage supply terminal (V_{CC}) as well as the output terminals. If the voltage of the output should become less than that of the GND terminal or a reverse supply voltage is applied, current will flow via this parasitic diode causing IC destruction. It is therefore very important to prevent a voltage of less than -0.5V in respect to the GND terminal from being applied to another terminal.

When input voltage V_I drops to less than -0.5V, the largest portion of current flows from the GND terminal via the Schottky barrier diode SBD to the input terminal

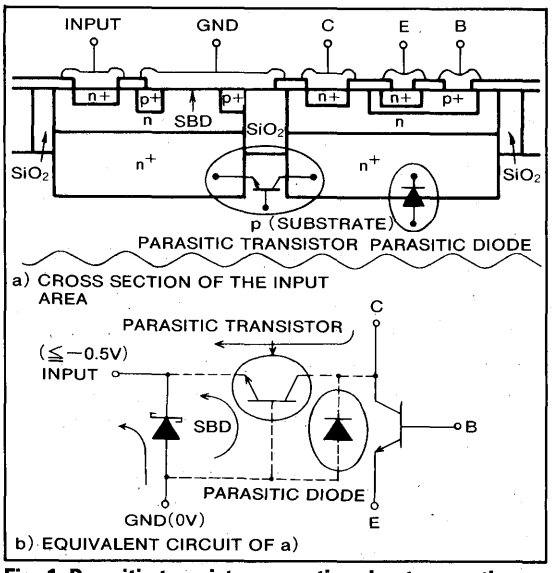


Fig. 1 Parasitic transistor operation due to negative input voltage

as shown in Fig. 1. But, as mentioned in §2-3, the remainder flows from the base of the parasitic transistor to the emitter with current amplification in the collector current. This results in current flowing from the collector of the nearby transistor to the input terminal. The original collector current is drawn into the input terminal causing circuit misoperation. Due to oxide film separation in the ASTTLs, parasitic current amplification is less than that of STTLs making it less likely for misoperation to occur.

2-9 Output loading capacitance

By connecting a capacitor between the GND line of an IC and its output terminal or the line connected with output, delay time can be lengthened and noise can be prevented. This capacitor is charged from the power supply via the active pull-up circuit when the output changes from low-level to high-level. It discharges to GND through the output transistor when the output changes from high-level to low-level. Care must be taken regarding the size of this capacitor because the higher the capacity of the capacitor the greater the energy of charging and discharging through the output circuit causing degradation in it. The capacity of this capacitor depends upon the output characteristics of the IC and the frequency of charging and discharging, but generally a capacitor of less than 1,000pF is used. When a capacitor of 0.1 μF or more is to be used, connect a resistor in series with the capacitor to lengthen the charging and discharging time.

2-10 DC noise margin

There are various DC noise margins, but the one used here is defined as V_{NH} and V_{NL} when the output is either high-level or low-level respectively. They are derived as follows:

$$V_{NH}=V_{OH}-V_{TH} \quad V_{NL}=V_{TL}-V_{OL}$$

Where V_{OH} and V_{OL} are the values derived from transfer curves like Fig. 2 or the values guaranteed in the databook and V_{TH} and V_{TL} are the input voltages that provide V_{OL}max or V_{OH}min. (See Fig. 2) Fig. 3 shows the temperature characteristics of V_{NH} and V_{NL} in actual operating conditions as obtained from transfer characteristics. V_{NH} and V_{NL} of ALSTTL gate are also given for reference.

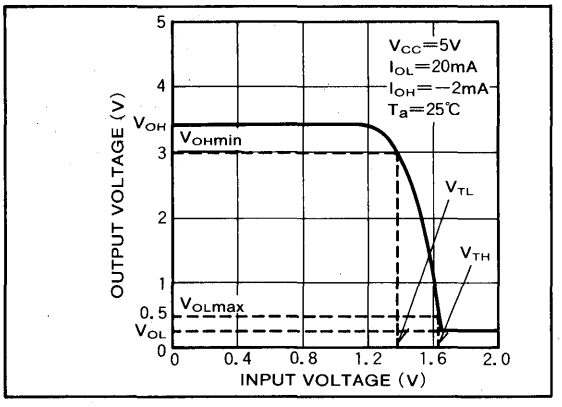


Fig. 2 Transfer characteristics (M74AS00P)

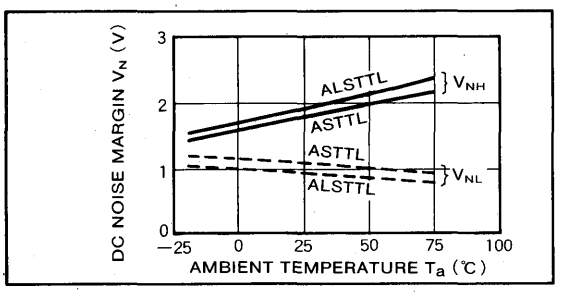


Fig. 3 DC noise margin characteristics (M74AS00P and M74ALS00AP)

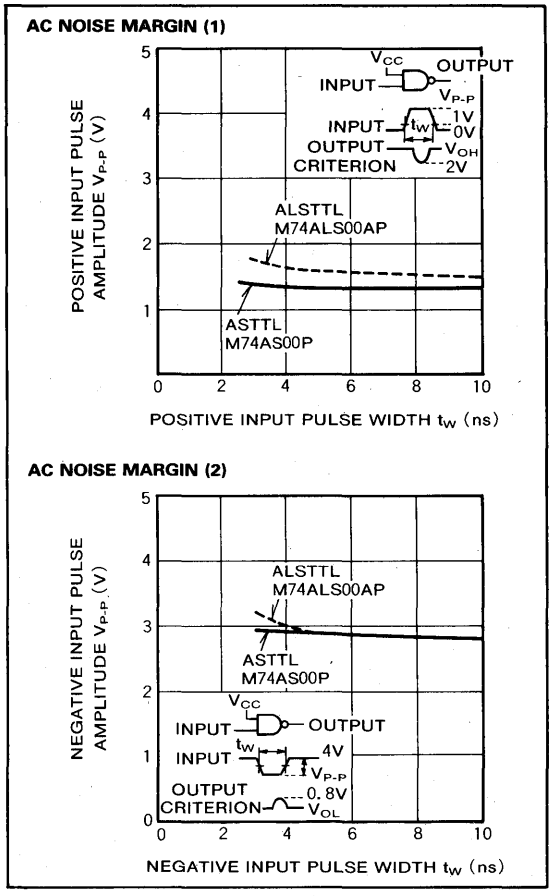


Fig. 4 AC noise margin characteristics

2-11 AC noise margin

Switching of the ASTTL is generally faster than that of the ALSTTL. This results in an AC noise margin lower than that of the ALSTTL.

Fig. 4 shows the AC noise margins of the ALSTTL (M74ALS00AP) and the ASTTL (M74AS00P). Due to its high speed, the ASTTL is easily affected by noise voltage (crosstalk) generated via the floating capacitance between lines. The lines connecting ASTTL ICs should be shorter than the ALSTTL ICs, and the lines between cards should be twisted pairs or coaxial cable.

2-12 Output short-circuit

When an output is high and that output is shorted to GND, excessive current flows and heat is generated in the IC. This is to be avoided if at all possible. However, if for some reason it is necessary to do so, one and only one output per an IC may be shorted for a period not exceeding one second.

2-13 Static electricity, surge

When surge endurance test is done by discharging a precharged 200pF capacitor connected between an input or output terminal and the GND terminal without a series resistor, the leakage characteristics degrade so that 50% of ASTTL and ALSTTL devices experience accumulative failure at 300～400V. Although the static electricity endurance level of the ALSTTL and ASTTL are high, it is still necessary that full care be given to both the handling and system design in order to prevent damages due to static electricity and surge voltages.

2-14 Mechanical and thermal stress

The shaping and cutting of the package or external leads can cause damage to the external leads, degradation of moisture resistant characteristics, and breakage of internal leads. Moreover, be careful that mechanical stress should not be placed on external IC leads from the printed circuit board after the IC has been mounted.

Since the IC is constructed of a number of different materials with different expansion coefficients, the application of sudden temperature changes or extended period of high heat (such as when applying solder) can lead IC to degradation or the breakage of internal leads. To avoid such conditions, it is necessary that the mechanical and thermal stress levels be the lowest.

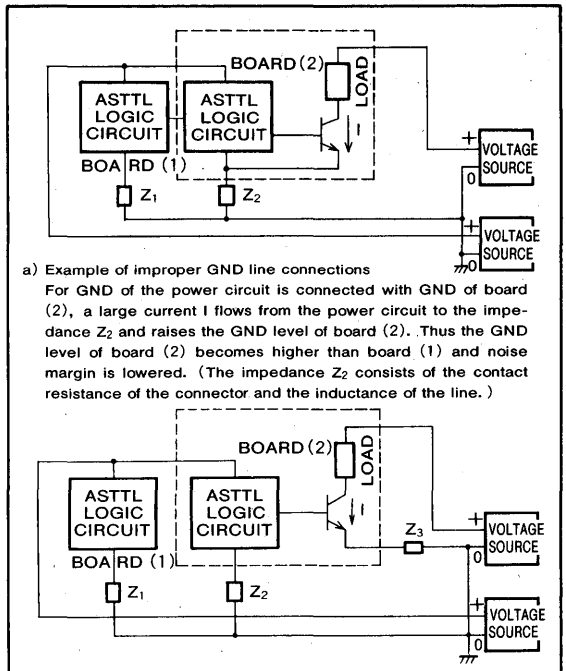
3. PRECAUTIONS CONCERNING SYSTEM DESIGN

3-1 Supply line

As explained in §2-1, the supply voltage should be regulated and decreased in ripples within the recommended operating conditions. (V_{CC} = 5V ± 10%) Moreover, to absorb the current spikes generated during IC switching, a decrease in supply impedance and supply line impedance is necessary. It is recommended that a 0.01~0.22 μF capacitor of good high frequency characteristics (such as porcelain capacitor) be connected between GND and the supply line every 1 to 5 ICs. Also connect a 50~100 μF electrolytic or tantalum capacitor between GND and the supply line every card. In the case of monostable multivibrator or line driver, connect a high frequency capacitor of about 0.1 μF between V_{CC} and GND on every IC. Make both the power supply line and GND line as broad a pattern as possible and make them parallel with each other. V_{CC} plane or mesh is the best.

3-2 Ground (GND) line

Noise may be generated due to common impedance in the GND line. Connecting the GND line to the earth at numerous points can also result in its becoming a noise source when voltage is induced in it by external magnetic fields. For this reason it is important not only that the GND line impedance be dropped, but that careful consideration be given to separating the GND line from other power circuits and electronic devices as shown in Fig. 5, and to the employment of relays and photocouplers for isolating one circuit ground from another. GND pattern should be a plane or a mesh. If it is not possible, make the GND line pattern broader than the power supply line (to minimize the DC resistance and inductance).



a) Example of improper GND line connections
For GND of the power circuit is connected with GND of board (2), a large current I flows from the power circuit to the impedance Z_2 and raises the GND level of board (2). Thus the GND level of board (2) becomes higher than board (1) and noise margin is lowered. (The impedance Z_2 consists of the contact resistance of the connector and the inductance of the line.)

b) Example of proper GND line connections
The GND lines of the power circuit and logic circuit are separated. This prevents a large current from flowing through Z_1 or Z_2, making it unlikely for the generation of a voltage difference between the GND levels of the boards.

Fig. 5 GND line connections

3-3 Fanout and wired-AND connections

(1) IC with active pull-up outputs

The larger portion of ASTTL and ALSTTL devices contain active pull-up (current source) in their output circuits in order to give high-speed switching and higher driving capabilities of capacitive loads. In this type of ICs, it is not possible to make wired-AND connections by connecting the output terminals together. This is because the active pull-up impedance is only 30 Ω when the output is high-level. So, if two outputs are connected together and one of the outputs is high while the other is low, excessive current will flow from the high-level output to the low-level output. Besides the increase of low-level output voltage, this will generate heat and increase current flow in the internal wiring causing misoperation, damages in IC, or a serious decrease in reliability. It is therefore very important that such connections not be made.

Fanout F_O indicates the number of input terminals that can be connected to and driven by an output. Fanout is represented by F_{OL} and F_{OH} for low-level and high-level respectively. The integer part of the smaller of F_{OL} and F_{OH} gives the maximum fanout.

$$F_{OL} \leqq \frac{\overline{I_{OL}}}{|\overline{I_{IL}}|} \qquad F_{OH} \leqq \frac{|\overline{I_{OH}}|}{\overline{I_{IH}}}$$

Where $\overline{I_{OL}}$, $\overline{I_{OH}}$, $\overline{I_{IL}}$ and $\overline{I_{IH}}$ are the maximum values guaranteed of low-level output current I_{OL}, high-level output current I_{OH}, low-level input current I_{IL} and high-level input current I_{IH}, respectively. The above formula is appropriate for load ICs that all have the same I_{IL} and I_{IH} values. When these values are different, use the following formula.

$$\overline{I_{OL}} \geqq \sum_{i=1}^{N} |\overline{I_{ILi}}| \qquad |\overline{I_{OH}}| \geqq \sum_{i=1}^{N} \overline{I_{IHi}}$$

(2) IC with open collector outputs

Wired-AND connections are possible with ICs that have open collector outputs. An open collector output needs a load resistor R_L connected between V_{CC} and itself. The value of R_L may be any value within the range set by $R_{L(min)}$, minimum load resistance, and $R_{L(max)}$, maximum load resistance, which vary according to the number of wired-AND connected outputs M and the number of connected inputs N (fanout). The formula is:

$$R_{L(max)}=\frac{V_{CC}-V_{OH}}{\sum_{i=1}^{M}\overline{I_{OHi}}+\sum_{i=1}^{N}\overline{I_{IHi}}}$$

$$R_{L(min)}=\frac{V_{CC}-V_{OL}}{\overline{I_{OL}}-\sum_{i=1}^{N}|\overline{I_{ILi}}|}$$

Where $\overline{I_{OH}}$, $\overline{I_{IH}}$, $\overline{I_{OL}}$ and $\overline{I_{IL}}$ are the maximum values guaranteed. V_{CC} is the minimum value in which the circuit is expected to function. (usually 4.5V) V_{OH} is the minimum value needed in the circuit. It may be 2.7V or 2.0V or anything.

(3) IC with 3-state output

The 3-state output, in addition to the low-level state and high-level state of the active pull-up output, has a high-impedance state "Z." The use of "Z" permits bus driving operation. As shown in Fig. 6, this method while resembling the previously mentioned wired-AND connection, differs in that only one of the outputs connected to one bus is used in active state with the remainder being placed in the high-impedance state.

The values of M and N are determined by the following formula, where M is the number of outputs connected to the bus and N is the number of inputs connected (fanout).

$$\overline{I_{OL}} \geqq \sum_{i=1}^{M-1}|\overline{I_{OZLi}}|+\sum_{i=1}^{N}|\overline{I_{ILi}}|$$

$$|\overline{I_{OH}}| \geqq \sum_{i=1}^{M-1}|\overline{I_{OZHi}}|+\sum_{i=1}^{N}|\overline{I_{IHi}}|$$

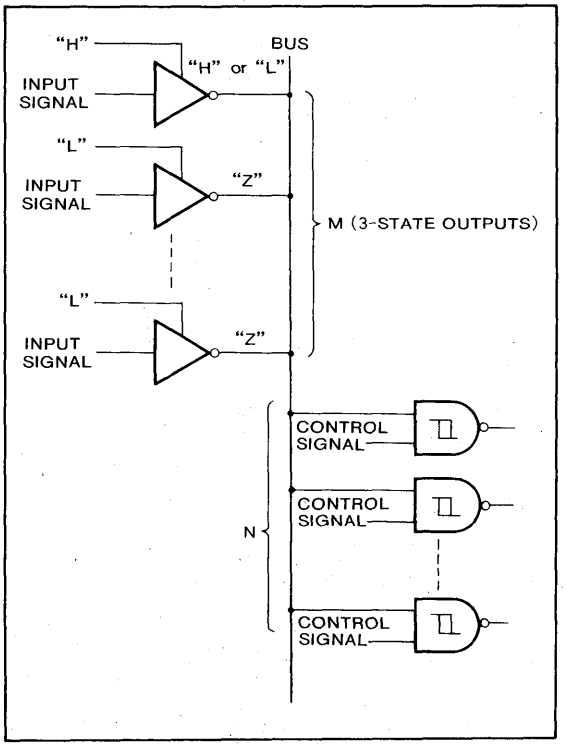


Fig. 6 Bus connection

Since many outputs are connected to the bus in this method, it is necessary that timing be set so that only one of the outputs becomes active while the remainder remain in the high-impedance state. If more than one of the outputs become active at the same time, it is as if active pull-up outputs were connected together creating the condition explained in §3-3-(1). To prevent such conditions, the output enable and disable times have been specified in the switching characteristics of these types of devices. From these specifications, timing should be set so that none of high-impedance outputs becomes active before the active output becomes high-impedance. Take care not to allow active period to overlap because excessive current will flow in the power and GND lines lowering the voltage of the power line and creating noise thus causing misoperation.

3-4 Unused gates

Since there are several independent gate circuits within a gate IC, some gates will remain unused when the IC is used in a logic circuit. As far as operation is concerned, it makes no difference whether or not the terminals of unused gate circuits are left open. However, for example, a comparison of a NAND gate supply current with its terminals left open and with its terminals connected to GND will show that approximately 5 times as much current flows in the former condition as in the latter. Because the input conditions of unused gates can reduce the power supply capacity, it is recommended that unused gate input connections be properly taken care of.

3-5 Length of signal cables between ICs

The length of signal cables between ICs should be kept as short as possible. Otherwise, signal waveform disturbance may be caused by inductive noise or reflection. If the cable is shorter than 10cm, the effect is negligible, but care must be taken if it is longer. Care must be taken for long cables on both inductive noise and reflection as stated in the following sections. A gate for waveform regeneration can be effective when placed in the middle of a long cable.

3-6 Inductive noise

The most troublesome inductive noise is crosstalk. As the noise is transmitted through capacitance and mutual inductance which exist between two parallel cables, following two methods are effective to reduce the noise.

1. Minimize the length of signal cables running parallel, and separate the cables as far as possible.
2. Minimize the effect by lowering the characteristic impedance of signal cables. Use of coaxial cable or twisted-pair cable is preferable but the impedance can be lowered by keeping the signal cable on the PC board as close to GND as possible.

As the output waveform of ASTTL at the rise and fall is

steep, more care is required to prevent crosstalk compared to conventional ICs.

3-7 Twisted-pair cables and coaxial cables

Twisted-pair cables and coaxial cables are suitable for signal transmission among PC boards or for signal cables longer than 30cm. Coaxial cable exceeds twisted-pair cable in immunity from crosstalk but twisted-pair cable is sufficient for ordinary use.

One of the precautions on the usage of these cables is grounding. Ground of the transmission line, driver ICs or receiver ICs, and the capacitance installed between V_{CC} and GND of these ICs should be connected at a point as close to the end of transmission line as possible.

A high-frequency capacitor of 0.1 μF should be used for decoupling between V_{CC} and GND for each driver or receiver IC.

In addition to the above, care should be taken to prevent reflections.

3-8 Reflection

Reflection occurs due to a mismatch between the input or output impedance of an IC and the characteristic impedance of the signal cable. The impedance of printed patterns or jumper lines is 50 to 300 Ω while the input impedance of ASTTL is several tens of kΩ and the output impedance is between several Ω to several tens of Ω. To match the impedance, the following two methods can be used.

1. Connect a resistor (of approximately 100 Ω) in series to the output. Reflection stops when the sum of output impedance and resister is equal to the impedance of the signal cable.
2. Connect a resistor between the input and V_{CC} or GND. Assuming that the resistors between the input and V_{CC}, and between input and GND are parallel, reflection stops when that value is equal to the impedance of the signal cable. (Example: Z_O is 200 Ω, the impedance between the input and V_{CC} 300 Ω, and the impedance between input and GND 600 Ω.)

These methods have the following drawbacks and should be used cautiously: Drive capability decreases in (1), large output current is required in (2), and switching characteristics may change.

Bergeron charts can be used to analyze reflection, as shown in Figs. 8 and 9. This chart shows the high-level

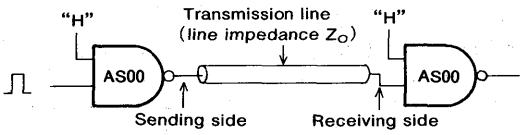


Fig. 7 Driving a transmission line

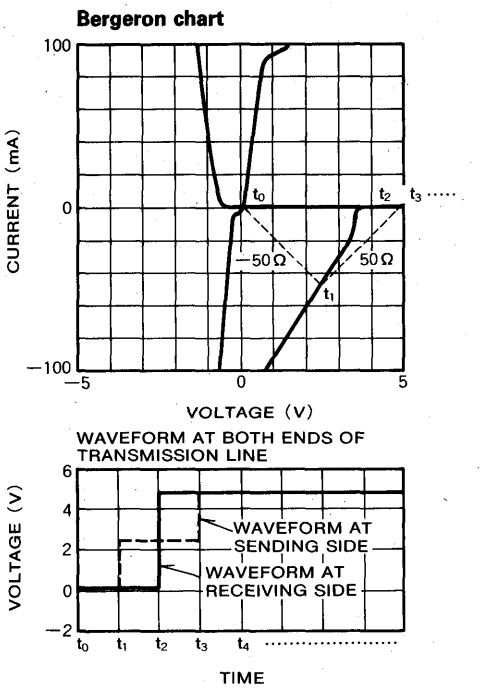


Fig. 8 Anaiysis of reflection (Z_O=50Ω, low-level to high-level)

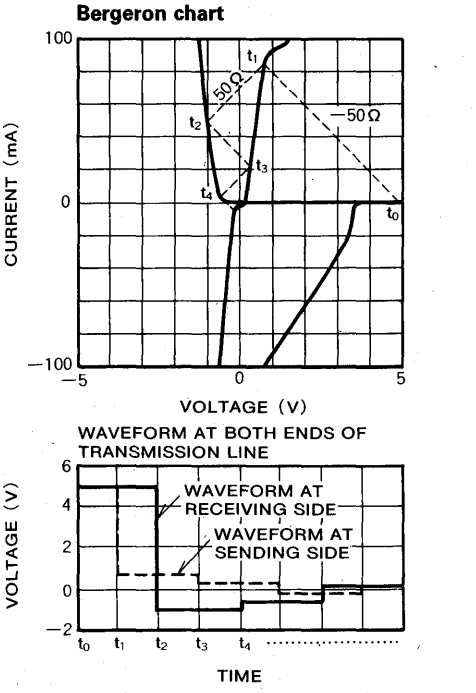


Fig. 9 Analysis of reflection (Z_O=50Ω, high-level to low-level)

MITSUBISHI ELECTRIC

and low-level output characteristics of the IC on the driver (sending) side and the input characteristics of the driven (receiving) side. The currents flowing out of the receiving ICs are expressed positive because they flow into the driving ICs.

Figs. 8 and 9 show the reflection waveform when the M74AS00P is connected as shown in Fig. 7 to both ends of transmission line of $Z_O = 50\Omega$. On the rising edge, an excellent waveform appears at receiving side owing to the $I_{OH} - V_{OH}$ characteristics. The waveform is found to undershoot considerably on the falling edge.

Care should be taken with signal cables connected to many IC loads or those with long branched lines as they tend to cause multiple reflections and distorting the waveform.

3-9 Signal line resonance

In Fig. 10 a), the input of an ASTTL is connected via a wire of several tens of centimeters to a switch, S, which sends ON/OFF condition signals. In such a case, capacitor C may be connected between the input terminal and the GND close to the input terminal, used to prevent the ASTTL from misoperation due to inductive noise.

The equivalent circuit of Fig. 10 a) is shown in Fig. 10 b). When the switch is turned on, a damping oscillation is created between the two terminals C is connected to, as Fig. 11 shows. This damping oscillation may cause misoperation of the ASTTL.

The damping oscillation has a frequency of 1~5MHz when the signal line has a length of 60cm and C = 15,000pF, a frequency that is lower than that experienced in ringing caused by reflection. To prevent this damping oscillation, damping resistor R_D may be added in series to L. The value of R_D is found by using the following formula.

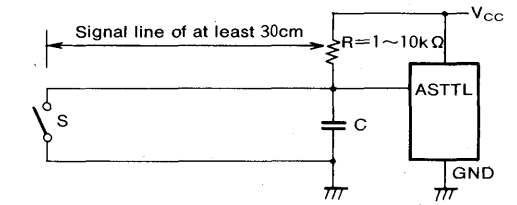
$$f_O = \frac{1}{2\pi\sqrt{LC}}$$

$$R_D \geqq 2\sqrt{\frac{L}{C}}$$

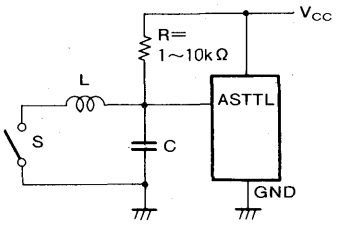
Observation of the damping oscillation in Fig. 11 shows $f_O \fallingdotseq 3$MHz and since C = 15,000pF then $L \fallingdotseq 0.2\,\mu$H and $R_D \geqq 7\Omega$.

Usually, it will be found that a value of 10~47Ω for R_D will prevent such resonant oscillations.

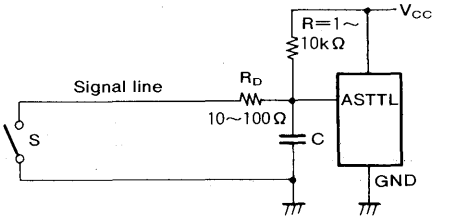
Since an SBD is generally configured between the input and GND of an ASTTL, the magnitude of damping oscillation is small compared to that without an SBD. However, since full prevention cannot be obtained, it is recommended that the circuit shown in Fig. 10 c) be used rather than the one in Fig. 10 a).



a) The signal line and capacitor C form a resonant circuit that can easily cause misoperation.



b) The equivalent circuit of a)



c) R_D is added to prevent resonant oscillation by the signal line and capacitor C.

Fig. 10 Examples of ASTTL application

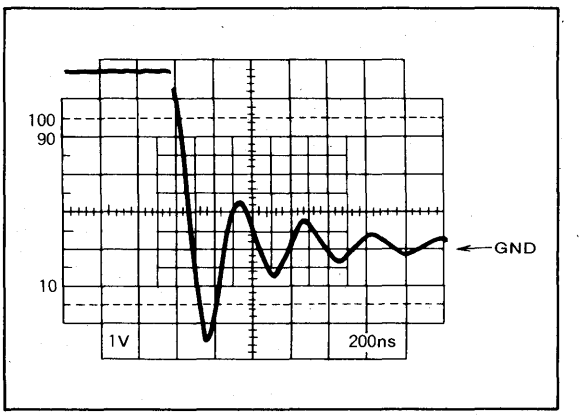
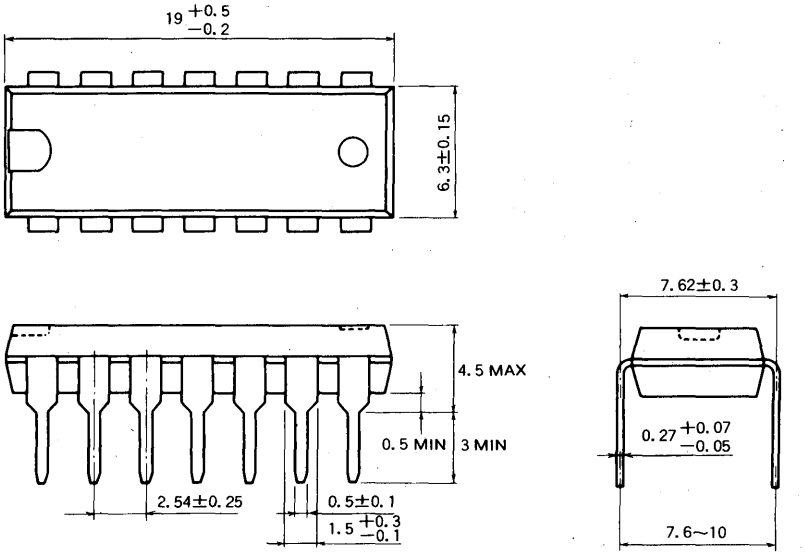


Fig. 11 Example of damping oscillation

PACKAGE OUTLINES

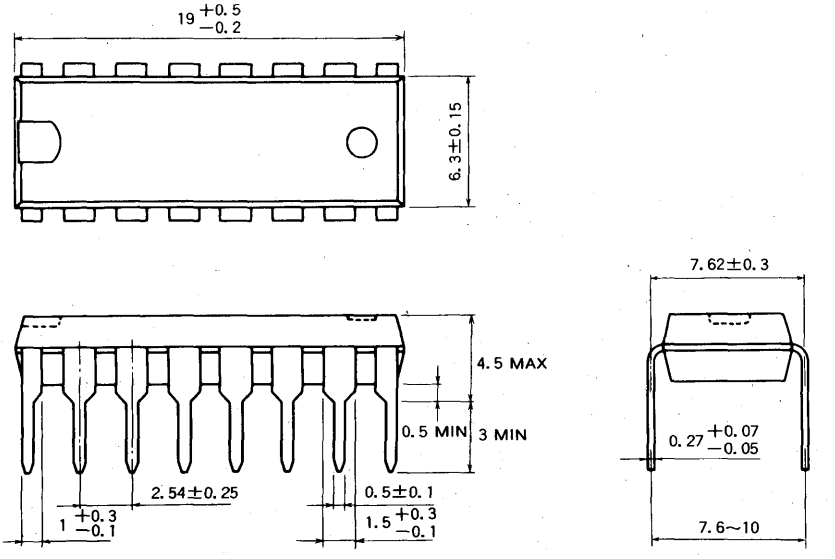
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



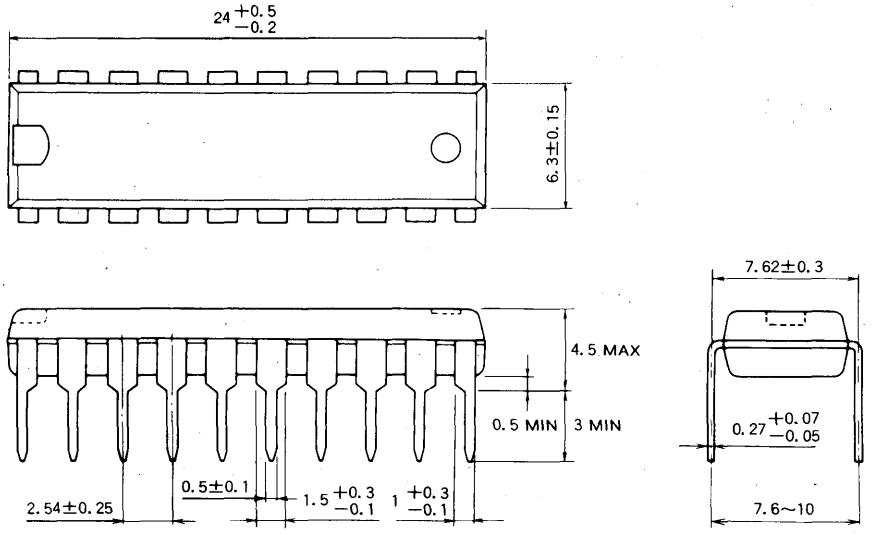
TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm



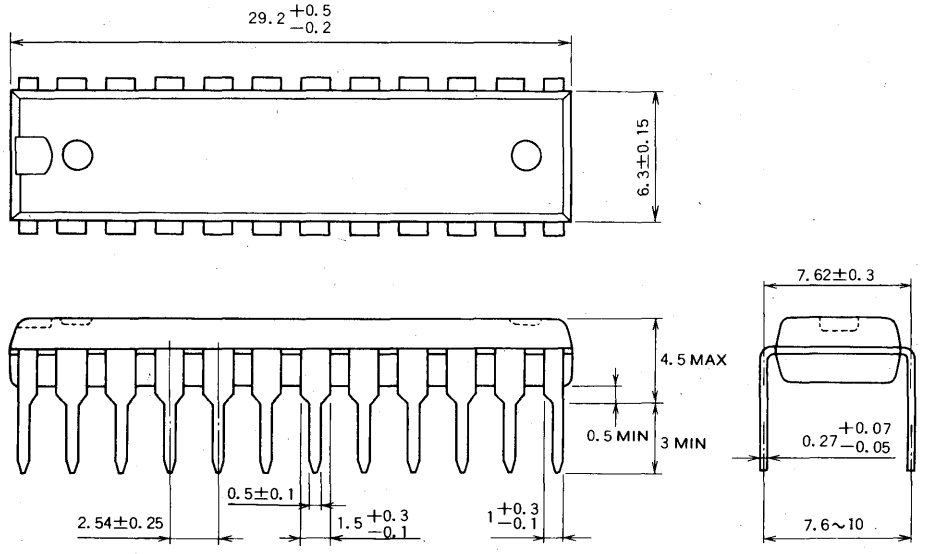
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

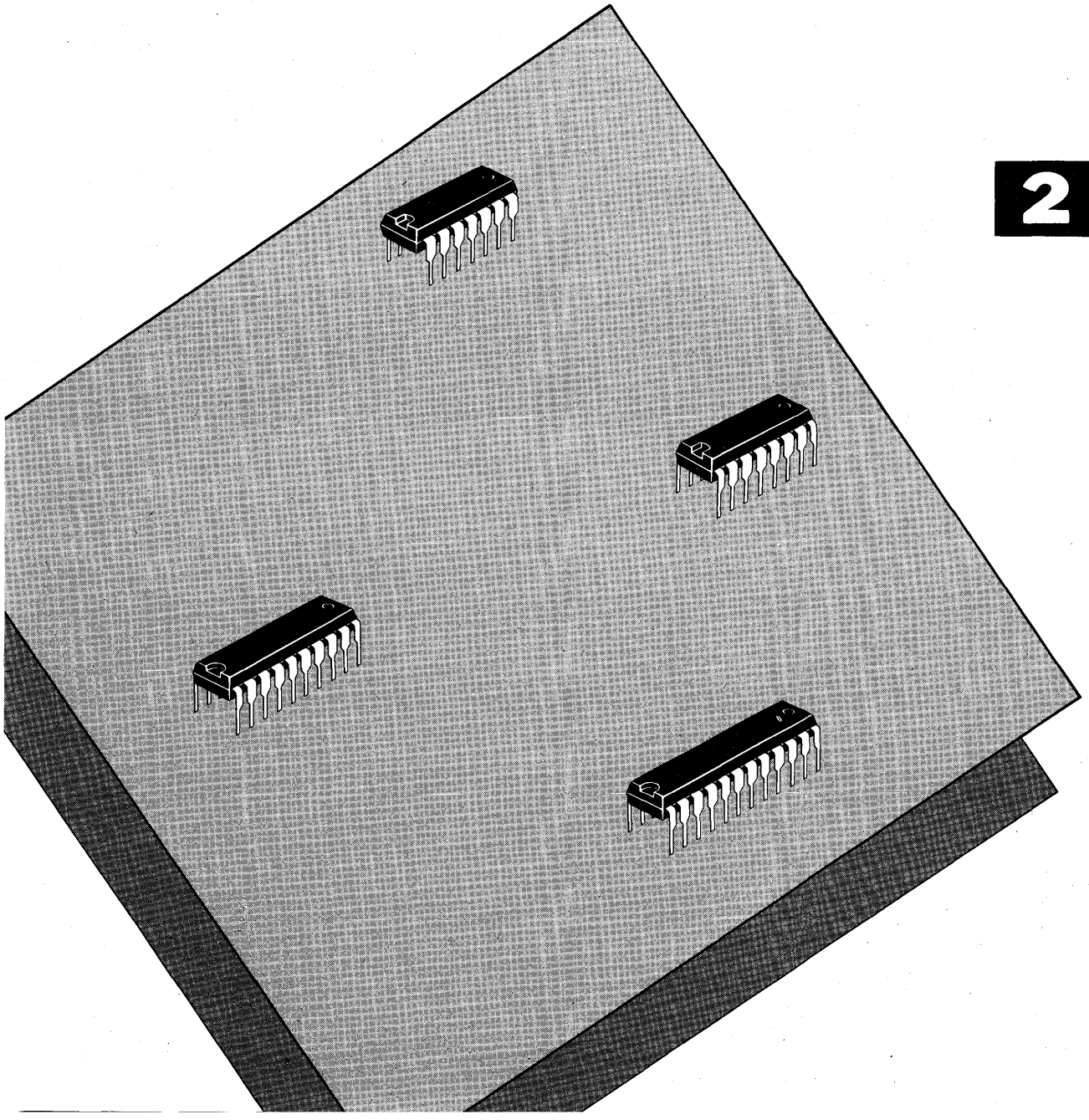
Dimension in mm



DATA SHEETS

INDIVIDUAL DATA

2



NEW PRODUCT

M74AS00P

QUADRUPLE 2-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74AS00P is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High speed (t_{pd}=2ns typical: C_L=15pF)
- Low output impedance
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATION

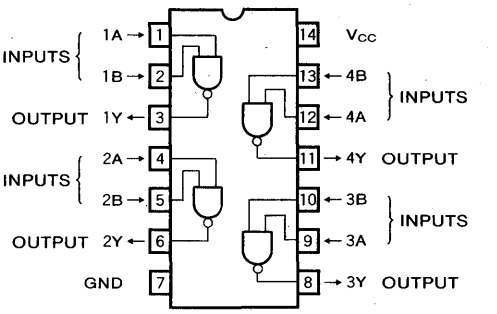
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74AS00P achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit, clamp diodes (both input and output) and undershoot recovery circuit.

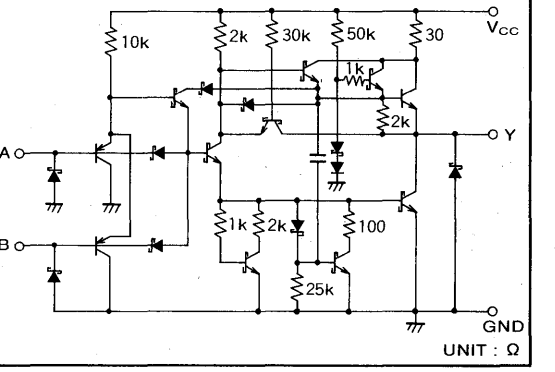
When both A and B inputs are high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−2	mA
I_{OL}	Low-level output current	0		20	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=20mA			0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V			20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=0V		2	3.2	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=4.5V		10.8	17.4	mA

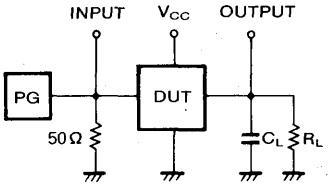
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter			Test conditions/Limits: V_{CC}=4.5∼5.5V (Note 1), C_L=50pF, R_L=500Ω						Unit
				T_a=0∼70℃			T_a=−20∼+75℃			
		Inputs	Output	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A, B	Y	1		4.5	1		5	ns
t_{PHL}				1		4	1		5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

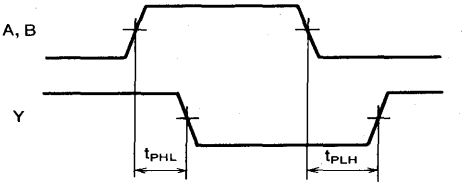
Note 1: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level=1.3V)



MITSUBISHI ELECTRIC

NEW PRODUCT

M74AS02P

QUADRUPLE 2-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74AS02P is a semiconductor integrated circuit consisting of four 2-input positive-logic NOR gates, usable as negative-logic NAND gates.

FEATURES

- High speed
- Low output impedance
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

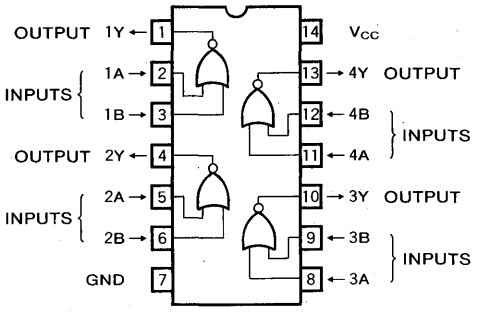
Employing PNP transistors in the inputs and active pull-up in the outputs, the M74AS02P achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit, clamp diodes (both input and output) and undershoot recovery circuit.

When both A and B inputs are low-level, output Y is high-level, and when at least one of the inputs is high, the output is low.

FUNCTION TABLE

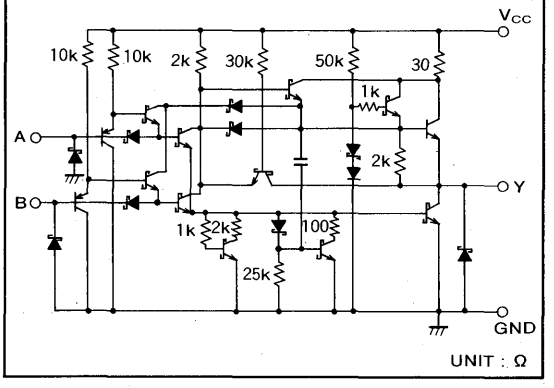
Inputs		Output
A	B	Y
L	L	H
H	L	L
L	H	L
H	H	L

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−2	mA
I_{OL}	Low-level output current	0		20	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=20mA			0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V			20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=0V		3.7	5.9	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=4.5V		12.5	20.1	mA

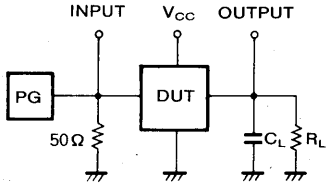
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter			Test conditions/Limits (V_{CC}=4.5∼5.5V (Note 1), C_L=50pF, R_L=500Ω)						Unit
				T_a=0∼70℃			T_a=−20∼+75℃			
		Inputs	Output	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A, B	Y	1		4.5	1		5	ns
t_{PHL}				1		4.5	1		5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

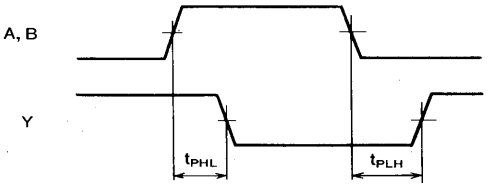
Note 1: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level=1.3V)



NEW PRODUCT

M74AS04P

HEX INVERTER

DESCRIPTION

The M74AS04P is a semiconductor integrated circuit consisting of six inverters.

FEATURES

- High speed
- Low output impedance
- Wide operating temperature range (T_a=−20～+75℃)

APPLICATION

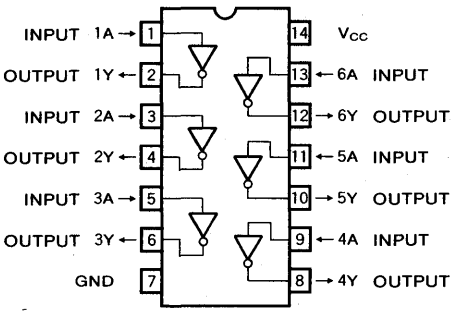
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74AS04P achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit, clamp diodes (both input and output) and undershoot recovery circuit.

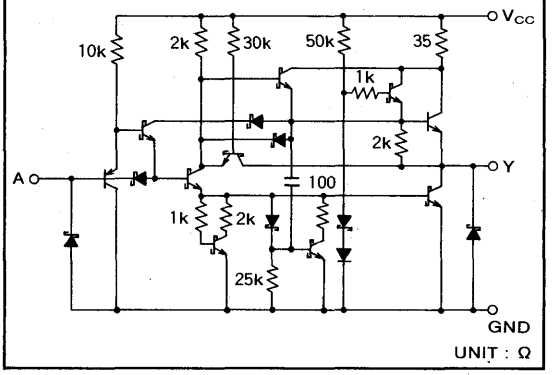
When input A is high-level, output Y is low-level, and when the input is low, the output is high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS (T_a=−20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+7	V
V_I	Input voltage		−0.5～+7	V
V_O	Output voltage	High-level state	−0.5～V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20～+75	℃
T_{stg}	Storage temperature range		−65～+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−2	mA
I_{OL}	Low-level output current	0		20	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=20mA			0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V			20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=0V		3	4.8	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=4.5V		14	26.3	mA

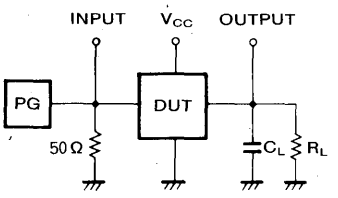
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

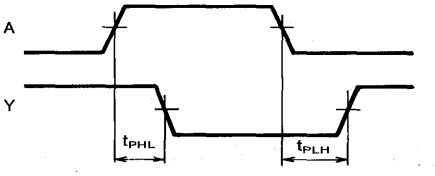
Symbol	Parameter			Test conditions/Limits: V_{CC}=4.5∼5.5V (Note 1), C_L=50pF, R_L=500Ω						Unit
				T_a=0∼70℃			T_a=−20∼+75℃			
		Input	Output	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A	Y	1		5	1		5.5	ns
t_{PHL}				1		4	1		4.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 1: Measurement circuit



TIMING DIAGRAM (Reference level=1.3V)



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

NEW PRODUCT

M74AS08P

QUADRUPLE 2-INPUT POSITIVE AND GATE

DESCRIPTION

The M74AS08P is a semiconductor integrated circuit consisting of four 2-input positive-logic AND gates, usable as negative-logic OR gates.

FEATURES

- High speed
- Low output impedance
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

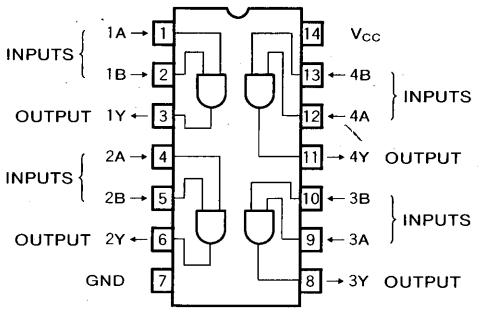
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74AS08P achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit, clamp diodes (both input and output) and undershoot recovery circuit.

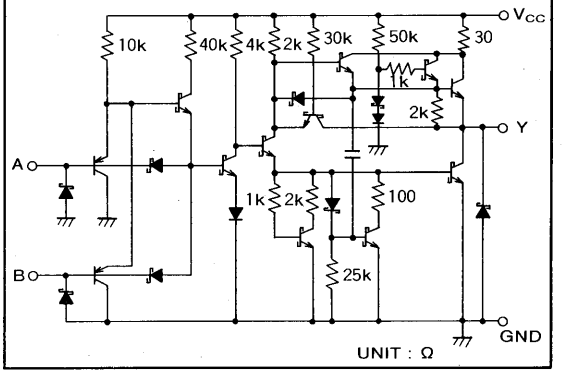
When both A and B inputs are high-level, output Y is high-level, and when at least one of the inputs is low, the output is low.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7	V
V_I	Input voltage		−0.5~+7	V
V_O	Output voltage	High-level state	−0.5~V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20~+75	℃
T_{stg}	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−2	mA
I_{OL}	Low-level output current	0		20	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=20mA			0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V			20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=4.5V		5.8	9.3	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=0V		14.9	24	mA

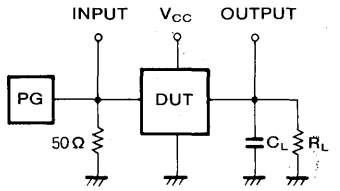
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

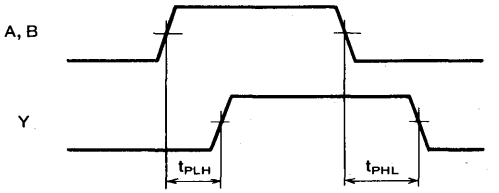
Symbol	Parameter			Test conditions/Limits: V_{CC}=4.5∼5.5V (Note 1), C_L=50pF, R_L=500Ω						Unit
				T_a=0∼70℃			T_a=−20∼+75℃			
		Inputs	Output	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A, B	Y	1		5.5	1		6	ns
t_{PHL}				1		5.5	1		6	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 1: Measurement circuit



TIMING DIAGRAM (Reference level=1.3V)



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

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PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

M74AS20P

DUAL 4-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74AS20P is a semiconductor integrated circuit consisting of two 4-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High speed
- Low output impedance
- Wide operating temperature range (T_a=−20～+75℃)

APPLICATION

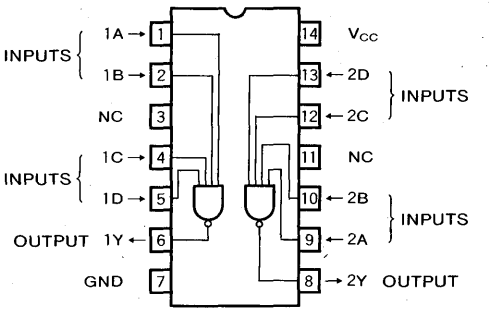
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74AS20P achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit, clamp diodes (both input and output) and undershoot recovery circuit.

When A, B, C, and D inputs are simultaneously high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

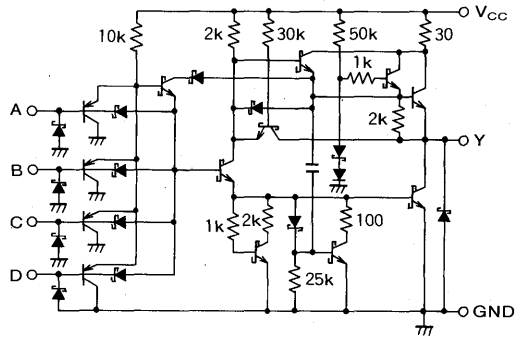
PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



UNIT : Ω

FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

N=B·C·D

ABSOLUTE MAXIMUM RATINGS (T_a=−20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+7	V
V_I	Input voltage		−0.5～+7	V
V_O	Output voltage	High-level state	−0.5～V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20～+75	℃
T_{stg}	Storage temperature range		−65～+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−2	mA
I_{OL}	Low-level output current	0		20	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=20mA			0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V			20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=0V		1	1.6	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=4.5V		5.4	8.7	mA

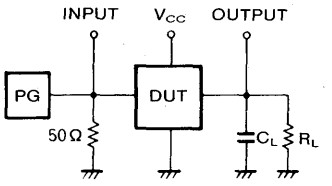
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter			Test conditions/Limits: V_{CC}=4.5∼5.5V (Note 1), C_L=50pF, R_L=500Ω						Unit
				T_a=0∼70℃			T_a=−20∼+75℃			
		Inputs	Output	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A, B	Y	1		5	1		5.5	ns
t_{PHL}		C, D		1		4.5	1		5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

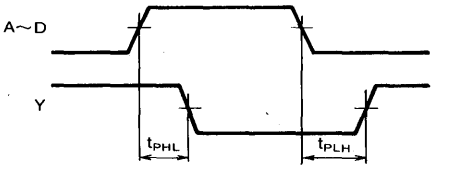
Note 1: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level=1.3V)



MITSUBISHI ELECTRIC

M74AS21P

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

DUAL 4-INPUT POSITIVE AND GATE

DESCRIPTION

The M74AS21P is a semiconductor integrated circuit consisting of two 4-input positive-logic AND gates, usable as negative-logic OR gates.

FEATURES

- High speed
- Low output impedance
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATION

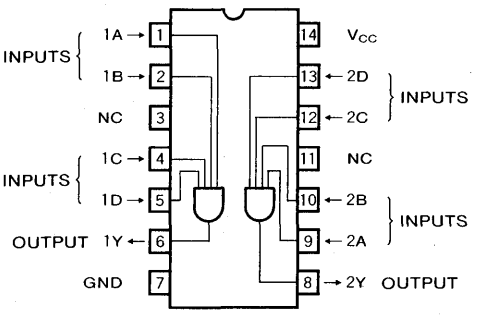
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74AS21P achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit, clamp diodes (both input and output) and undershoot recovery circuit.

When A, B, C, and D inputs are simultaneously high-level, output Y is high-level, and when at least one of the inputs is low, the output is low.

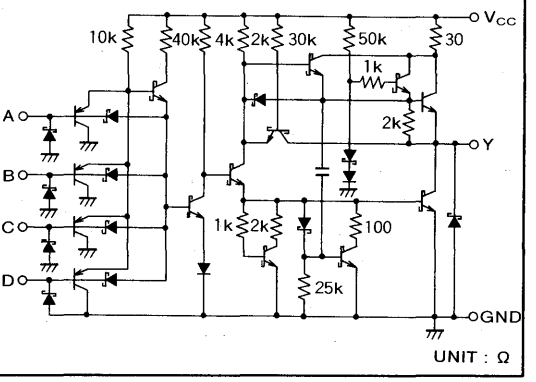
PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	L
H	L	L
L	H	L
H	H	H

N=B·C·D

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−2	mA
I_{OL}	Low-level output current	0		20	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=20mA			0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V			20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=4.5V		2.9	4.6	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=0V		7.4	12	mA

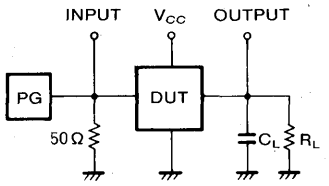
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

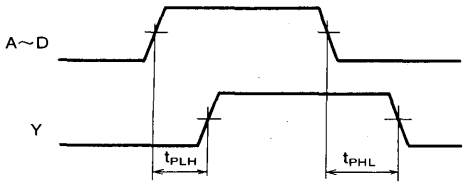
Symbol	Parameter			Test conditions/Limits						Unit
				V_{CC}=4.5∼5.5V (Note 1) C_L=50pF R_L=500Ω						
				T_a=0∼70℃			T_a=−20∼+75℃			
		Inputs	Output	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A, B	Y	1		6	1		6.5	ns
t_{PHL}		C, D		1		6	1		6.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 1: Measurement circuit



TIMING DIAGRAM (Reference level=1.3V)



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

NEW PRODUCT

M74AS32P

QUADRUPLE 2-INPUT POSITIVE OR GATE

DESCRIPTION

The M74AS32P is a semiconductor integrated circuit consisting of four 2-input positive-logic OR gates, usable as negative-logic AND gates.

FEATURES

- High speed
- Low output impedance
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATION

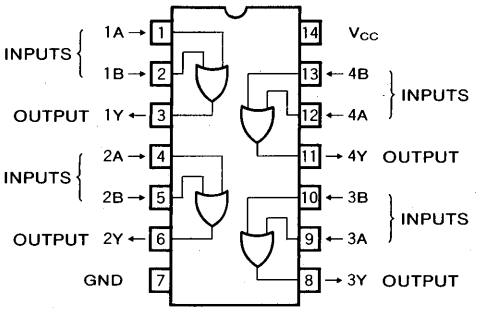
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74AS32P achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit, clamp diodes (both input and output) and undershoot recovery circuit.

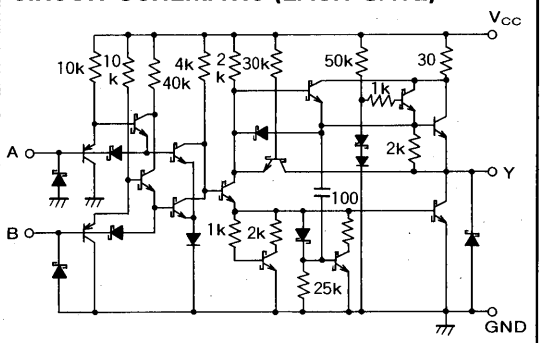
When both A and B inputs are low-level, output Y is low-level, and when at least one of the inputs is high, the output is high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



UNIT : Ω

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−2	mA
I_{OL}	Low-level output current	0		20	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=20mA			0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V			20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=4.5V		7.3	12	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=0V		16.5	26.6	mA

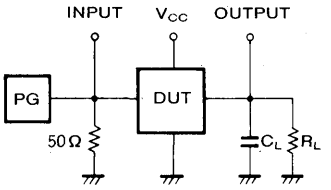
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter			Test conditions/Limits						Unit
				V_{CC}=4.5∼5.5V (Note 1) C_L=50pF R_L=500Ω						
				T_a=0∼70℃			T_a=−20∼+75℃			
		Inputs	Output	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A, B	Y	1		5.8	1		6.5	ns
t_{PHL}				1		5.8	1		6.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

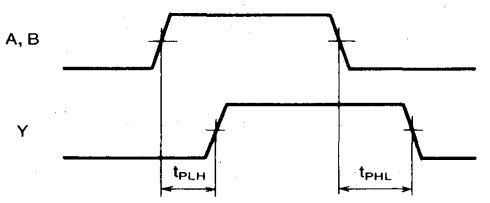
Note 1: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level=1.3V)



MITSUBISHI ELECTRIC

NEW PRODUCT

M74AS74P

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

DESCRIPTION

The M74AS74P is a semiconductor integrated circuit consisting of two D-type positive-edge-triggered flip-flop circuits. Each of the circuits has independent inputs such as data D, clock T, direct set $\overline{S_D}$ and direct reset $\overline{R_D}$.

FEATURES

- Positive-edge-triggering
- Independent inputs and outputs for each flip-flop
- Direct set and reset inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a=−20~+75℃)

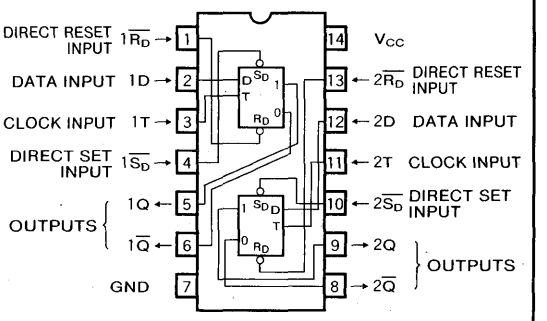
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

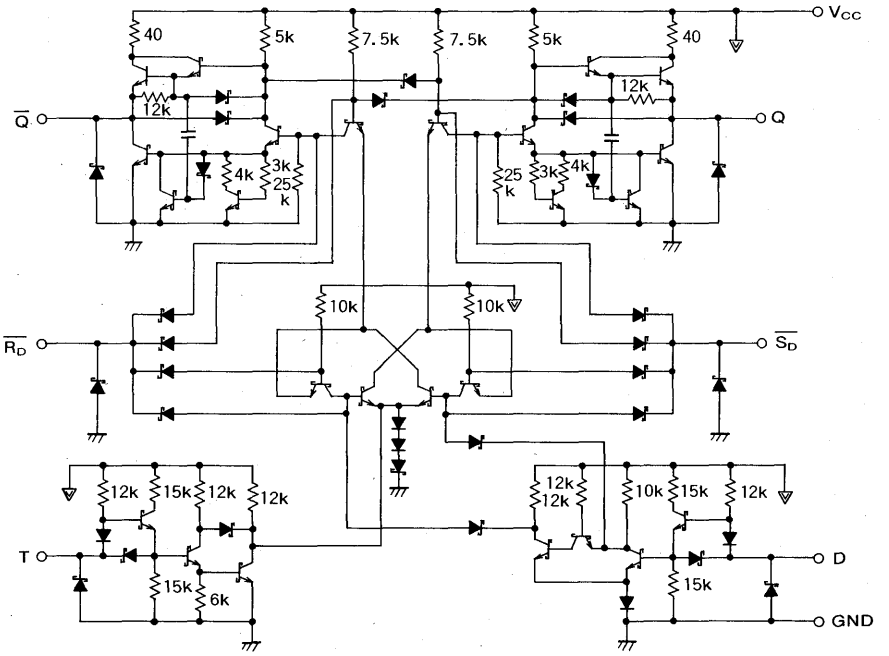
When T changes from low-level to high-level, the D signal just before the change appears at Q and $\overline{Q}$ outputs in accordance with the function table. Use of $\overline{S_D}$ and $\overline{R_D}$ allows direct R-S flip-flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low-level, Q and $\overline{Q}$ are high-level. But if $\overline{S_D}$ and $\overline{R_D}$ become high simultaneously from this condition, the state of Q and $\overline{Q}$ cannot be predicted. When used as a D-type flip-flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained in high-level.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH FLIP-FLOP)



UNIT : Ω

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

FUNCTION TABLE (Note 1)

Inputs				Outputs	
$\overline{S_D}$	$\overline{R_D}$	T	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	L	X	Q^0	$\overline{Q}^0$
H	H	↑	H	H	L
H	H	↑	L	L	H

Note 1 ↑ : Transition from low to high level (positive edge trigger)

Q^0 : Level of Q before the indicated steady-state input conditions were established.

$\overline{Q}^0$: Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

X : Irrelevant

* : If $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high-level from this condition then the state of Q and $\overline{Q}$ cannot be predicted.

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−2	mA
I_{OL}	Low-level output current	0		20	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=20mA			0.5	V
I_I	Input current at maximum voltage		V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current	D, T	V_{CC}=5.5V, V_I=2.7V			20	μA
		$\overline{S_D}$, $\overline{R_D}$				40	
I_{IL}	Low-level input current	D, T	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
		$\overline{S_D}$, $\overline{R_D}$				−1.8	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CC}	Supply current		V_{CC}=5.5V (Note 2)		10.5	16	mA

*: All typical values are at V_{CC}=5V, T_a=25℃.

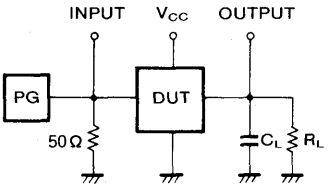
Note 2 : The supply current is measured alternately at D=T=$\overline{S_D}$=0V, $\overline{R_D}$=4.5V (Q=high-level) and D=T=$\overline{R_D}$=0V, $\overline{S_D}$=4.5V ($\overline{Q}$=high-level).

SWITCHING CHARACTERISTICS

Symbol	Parameter			Test conditions/Limits: V_{CC}=4.5∼5.5V, C_L=50pF, R_L=500Ω (Note 3)						Unit
				T_a=0∼70℃			T_a=−20∼+75℃			
		Inputs	Outputs	Min	Typ*	Max	Min	Typ*	Max	
f_{max}	Maximum clock frequency	T	Q, $\overline{Q}$	105			95			MHz
t_{PLH}	Propagation time	$\overline{S_D}$, $\overline{R_D}$	Q, $\overline{Q}$	3		7.5	3		8.5	ns
t_{PHL}				3.5		10.5	3.5		11.5	
t_{PLH}		T	Q, $\overline{Q}$	3.5		8	3.5		9	ns
t_{PHL}				4.5		9	4.5		10	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 3: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

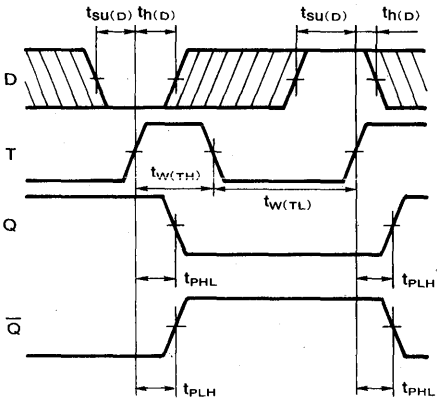
TIMING REQUIREMENTS (V_{CC}=4.5V~5.5V, C_L=50pF, R_L=500Ω)

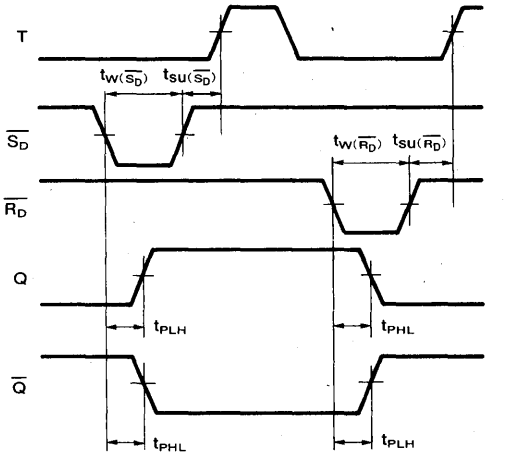
Symbol	Parameter		Limits						Unit
			T_a=0~70℃			T_a=−20~+75℃			
			Min	Typ*	Max	Min	Typ*	Max	
$t_{w(TH)}$	Pulse width	T "H"	4			4			ns
$t_{w(TL)}$		T "L"	5.5			5.5			
$t_{w(\overline{S_D})}$		$\overline{S_D}$ "L"	4			4			
$t_{w(\overline{R_D})}$		$\overline{R_D}$ "L"	4			4			
$t_{su(D)}$	Setup time before T↑	D	4.5			4.5			ns
$t_{su(\overline{S_D})}$		$\overline{S_D}$ "H" (inactive)	2			2			
$t_{su(\overline{R_D})}$		$\overline{R_D}$ "H" (inactive)	2			2			
$t_{h(D)}$	Hold time after T↑	D	0			0			ns

*: All typical values are at V_{CC}=5V, T_a=25℃.

↑: Transition from low to high level (positive edge trigger)

TIMING DIAGRAM (Reference level=1.3V)





Note 4: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

M74AS138P

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

DESCRIPTION

The M74AS138P is a semiconductor integrated circuit of a 3-line-to-8-line decoder/demultiplexer with enable inputs.

FEATURES

- Three types of enable inputs
- 4 to 16 decoder/demultiplexer capability without adding external components
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

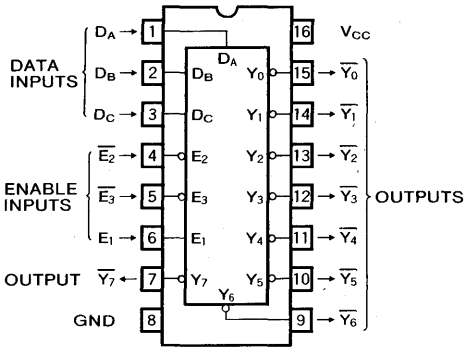
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Using as a decoder, give the address in 3-bit binary code on inputs D_A~D_C, and one output among outputs $\overline{Y_0}$~$\overline{Y_7}$ corresponding to the address become low while the other seven outputs are all high. In this case, set enable input E_1 high and enable inputs $\overline{E_2}$ and $\overline{E_3}$ low. When E_1, $\overline{E_2}$ and $\overline{E_3}$ are in any other condition, the outputs are high irrespective of the status of D_A~D_C.

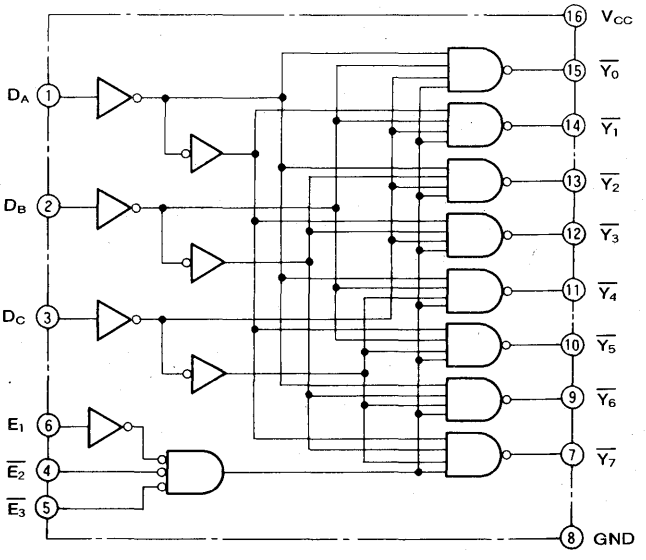
When the device is used as a demultiplexer, it functions as a 1-line-to-8-line demultiplexer by making E_1, $\overline{E_2}$ or $\overline{E_3}$ the data input and D_a~D_c the selection inputs.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs					Outputs							
E_1	$\overline{E_X}$	D_C	D_B	D_A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note 1 : $\overline{E_X}=\overline{E_2}+\overline{E_3}$

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−2	mA
I_{OL}	Low-level output current	0		20	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=20mA			0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V			20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CC}	Supply current	V_{CC}=5.5V		14	20	mA

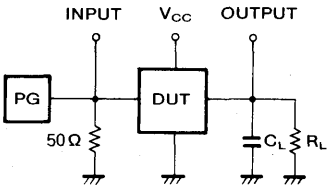
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Inputs	Output	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 2), C_L=50pF, R_L=500Ω; T_a=0~70℃ Min	T_a=0~70℃ Typ*	T_a=0~70℃ Max	T_a=−20~+75℃ Min	T_a=−20~+75℃ Typ*	T_a=−20~+75℃ Max	Unit
t_{PLH}	Propagation time	D_A, D_B	$\overline{Y}$	2		10	2		11	ns
t_{PHL}		D_C		2		9.5	2		10.5	
t_{PLH}		E_1, $\overline{E_2}$	$\overline{Y}$	2		10	2		11	ns
t_{PHL}		$\overline{E_3}$		2		10	2		11	

*: All typical values are at V_{CC}=5V, T_a=25℃.

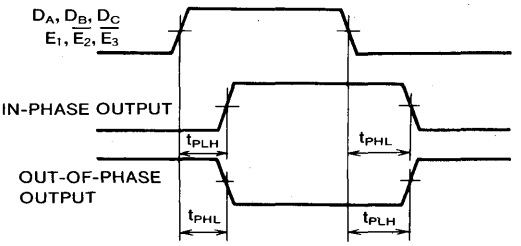
Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

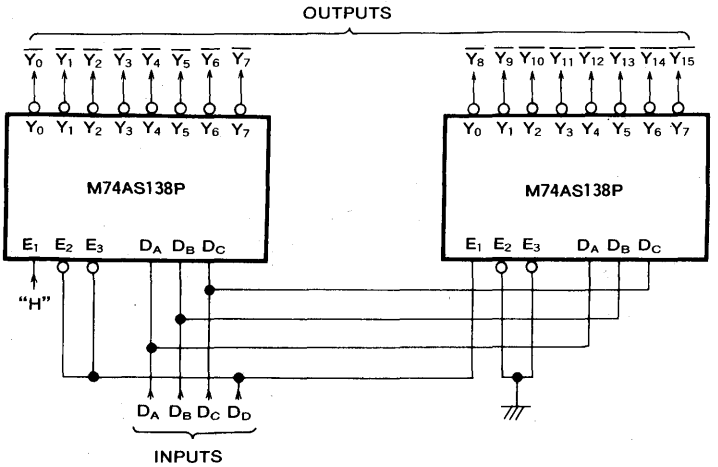
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level=1.3V)



APPLICATION EXAMPLES

4-line to 16-line decoder/demultiplexer



M74AS157P

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

DESCRIPTION

The M74AS157P is a semiconductor integrated circuit consisting of four 2-line to 1-line data selector/multiplexer circuits.

FEATURES

- Strobe input common to all 4 circuits
- Select input common to all 4 circuits
- Low output impedance
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

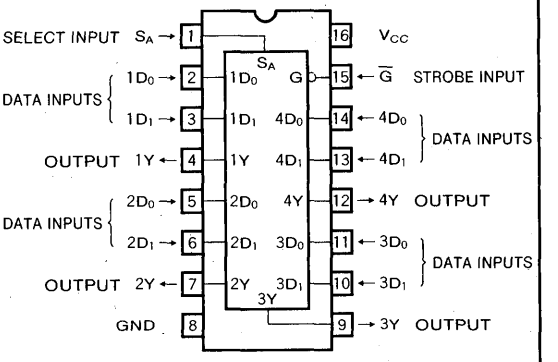
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

This IC has 4 circuits, each of which has a data selection function which selects one line out of 2 lines of signals and a multiplexing function to convert 2-bit parallel data into serial data by time sharing. When 2-line signals are fed to inputs D_0 and D_1 and one of them is specified by the select input S_A, the specified input signal appears at the output Y. By applying 2-bit parallel data to D_0 and D_1 and pulses to S_A, the D_0 and D_1 data appear at Y in that order synchronized with S_A. The S_A and strobe inputs are common to all 4 circuits. When $\overline{G}$ is high, all the outputs, 1Y, 2Y, 3Y and 4Y are low, regardless of other inputs.

M74AS157P has the same functions and pin connections as M74AS257P but the latter is provided with 3-state outputs.

PIN CONFIGURATION (TOP VIEW)



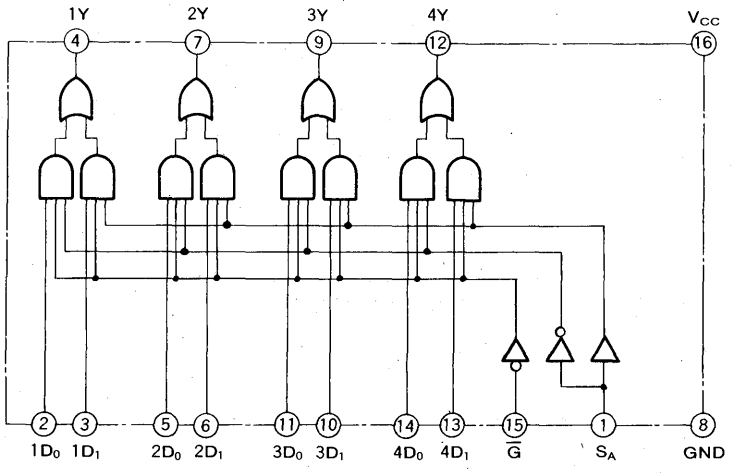
Outline 16P4

FUNCTION TABLE (Note 1)

Inputs				Output
$\overline{G}$	S_A	D_0	D_1	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Note 1. X: Irrelevent

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−2	mA
I_{OL}	Low-level output current	0		20	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=20mA			0.5	V
I_I	Input current at maximum voltage	S_A	V_{CC}=5.5V, V_I=7V			0.2	mA
		D_0, D_1, $\overline{G}$				0.1	
I_{IH}	High-level input current	S_A	V_{CC}=5.5V, V_I=2.7V			40	μA
		D_0, D_1, $\overline{G}$				20	
I_{IL}	Low-level input current	S_A	V_{CC}=5.5V, V_I=0.4V			−1	mA
		D_0, D_1, $\overline{G}$				−0.5	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CC}	Supply current		V_{CC}=5.5V		17.5	28	mA

*: All typical values are at V_{CC}=5V, T_a=25℃.

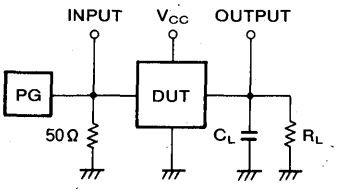
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SWITCHING CHARACTERISTICS

Symbol	Parameter	Inputs	Output	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 2), C_L=50pF, R_L=500Ω; T_a=0~70℃ Min	Typ*	Max	T_a=−20~+75℃ Min	Typ*	Max	Unit
t_{PLH}	Propagation time	D_0, D_1	Y	1		6	1		6.5	ns
t_{PHL}				1		5.5	1		6	
t_{PLH}		S_A	Y	2		11	2		12	ns
t_{PHL}				2		10	2		11	
t_{PLH}		$\overline{G}$	Y	2		10.5	2		11.5	ns
t_{PHL}				2		7.5	2		8	

*: All typical values are at V_{CC}=5V, T_a=25℃.

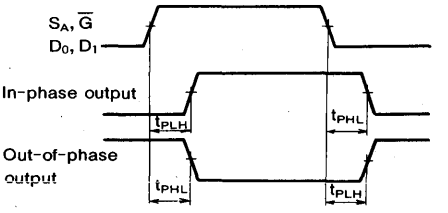
Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level= 1.3V)



M74AS158P

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER(INVERTED)

DESCRIPTION

The M74AS158P is a semiconductor integrated circuit consisting of four 2-line to 1-line data selector/multiplexer circuits.

FEATURES

- Inverted outputs
- Strobe input common to all 4 circuits
- Select input common to all 4 circuits
- Low output impedance
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

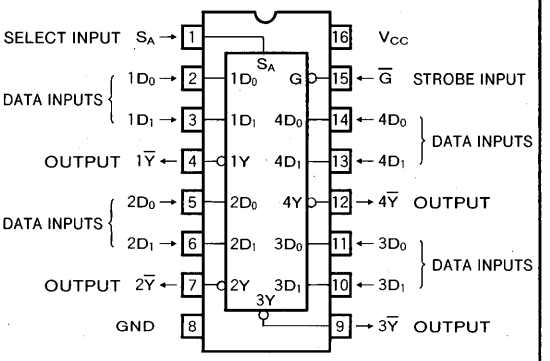
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

This IC has 4 circuits, each of which has a data selection function which selects one line out of 2 lines of signals and a multiplexing function to convert 2-bit parallel data into serial data by time sharing. When 2-line signals are fed to inputs D_0 and D_1 and one of them is specified by the select input S_A, the specified input signal appears inverted at the output $\overline{Y}$. By applying 2-bit parallel data to D_0 and D_1 and pulses to S_A, inverted data of D_0 and D_1 appear at $\overline{Y}$ in that order synchronized with S_A. The S_A and strobe inputs are common to all 4 circuits. When $\overline{G}$ is high, all the outputs, $1\overline{Y}$, $2\overline{Y}$, $3\overline{Y}$ and $4\overline{Y}$ are high, regardless of other inputs.

M74AS158P has the same functions and pin connections as M74AS258P but the latter is provided with 3-state outputs.

PIN CONFIGURATION (TOP VIEW)



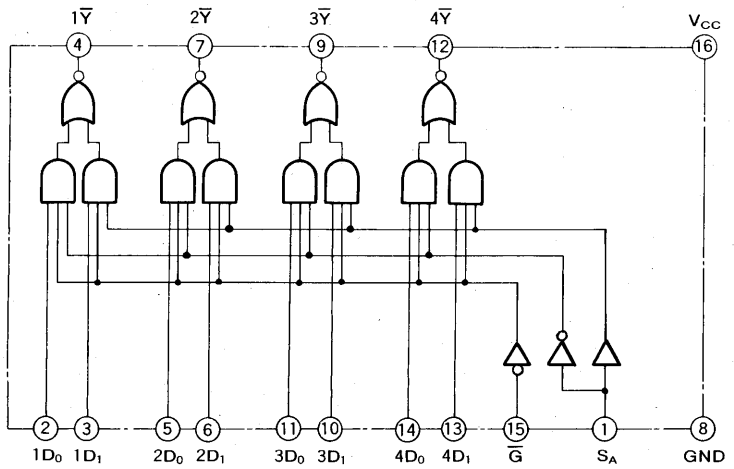
Outline 16P4

FUNCTION TABLE (Note 1)

Inputs				Output
$\overline{G}$	S_A	D_0	D_1	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

Note 1. X: Irrelevant

LOGIC DIAGRAM



QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER(INVERTED)

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−2	mA
I_{OL}	Low-level output current	0		20	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=20mA			0.5	V
I_I	Input current at maximum voltage	S_A	V_{CC}=5.5V, V_I=7V			0.2	mA
		D_0, D_1, $\overline{G}$				0.1	
I_{IH}	High-level input current	S_A	V_{CC}=5.5V, V_I=2.7V			40	μA
		D_0, D_1, $\overline{G}$				20	
I_{IL}	Low-level input current	S_A	V_{CC}=5.5V, V_I=0.4V			−1	mA
		D_0, D_1, $\overline{G}$				−0.5	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CC}	Supply current		V_{CC}=5.5V		15.6	22.5	mA

*: All typical values are at V_{CC}=5V, T_a=25℃.

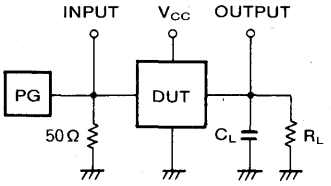
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (INVERTED)

SWITCHING CHARACTERISTICS

Symbol	Parameter	Inputs	Output	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 2), C_L=50pF, R_L=500Ω; T_a=0~70℃ Min	T_a=0~70℃ Typ*	T_a=0~70℃ Max	T_a=−20~+75℃ Min	T_a=−20~+75℃ Typ*	T_a=−20~+75℃ Max	Unit
t_{PLH}	Propagation time	D_0, D_1	$\overline{Y}$	1		5	1		5.5	ns
t_{PHL}				1		4.5	1		5	
t_{PLH}		S_A	$\overline{Y}$	2		9.5	2		10.5	ns
t_{PHL}				2		10.5	2		11.5	
t_{PLH}		$\overline{G}$	$\overline{Y}$	2		6.5	2		7	ns
t_{PHL}				2		10	2		11	

*: All typical values are at V_{CC}=5V, T_a=25℃.

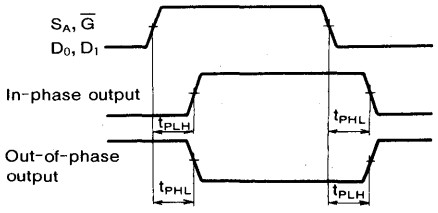
Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74AS240P

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74AS240P is a semiconductor integrated circuit consisting of two blocks of buffers with 3-state inverted outputs and independent output control for each block.

FEATURES

- In-phase output control inputs ($1\overline{OC}$, $2\overline{OC}$)
- High fan-out, 3-state output (I_{OL}=64mA, I_{OH}=−15mA)
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

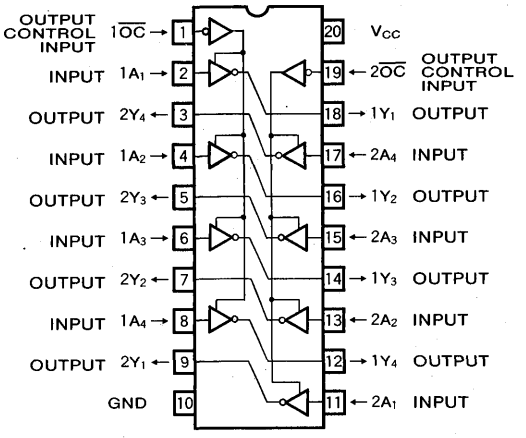
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

When output control input $\overline{OC}$ is low-level, and if input A is low, then output Y is high, if A is high, Y is low. When $\overline{OC}$ is high, Y_1 ~ Y_4 are in high-impedance state irrespective of the status of A.

The outputs of all eight buffers can be simultaneously controlled by connecting $1\overline{OC}$ and $2\overline{OC}$.

PIN CONFIGURATION (TOP VIEW)



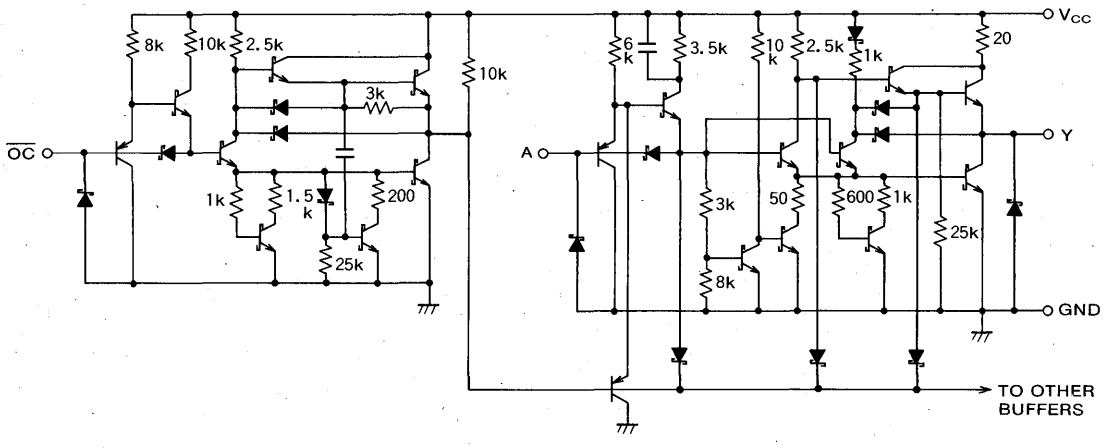
Outline 20P4

FUNCTION TABLE (Note 1)

Inputs		Output
A	$\overline{OC}$	Y
L	L	H
H	L	L
X	H	Z

Note 1: Z : High-impedance state
X : Irrelevant

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state or high-impedance state	−0.5∼+5.5	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−15	mA
I_{OL}	Low-level output current	0		64	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
		V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.4		
			I_{OH}=−15mA	2.4			
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=64mA				0.55	V
I_{OZH}	Off-state high-level output current	V_{CC}=5.5V, V_O=2.7V				50	μA
I_{OZL}	Off-state low-level output current	V_{CC}=5.5V, V_O=0.4V				−50	μA
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V		−50		−150	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V			11	17	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V			51	75	mA
I_{CCZ}	Supply current, all outputs disabled	V_{CC}=5.5V			24	38	mA

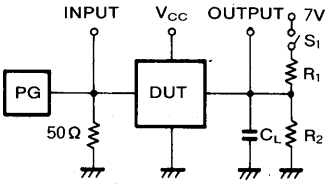
*: *All typical values are at* V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Input	Output	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 2), C_L=50pF, R_1=500Ω, R_2=500Ω; T_a=0~70℃ Min	Typ*	Max	T_a=−20~+75℃ Min	Typ*	Max	Unit
t_{PLH}	Propagation time	A	Y	2		6.5	2		7	ns
t_{PHL}				2		5.7	2		6	
t_{PZH}	Output enable time	$\overline{OC}$	Y	2		6.4	2		7	ns
t_{PZL}				2		9	2		9.5	
t_{PHZ}	Output disable time	$\overline{OC}$	Y	2		5	2		5.5	ns
t_{PLZ}				2		9.5	2		10.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 2: Measurement circuit

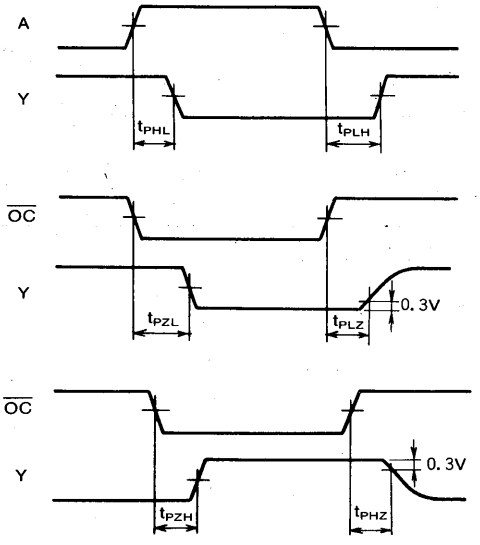


(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

TIMING DIAGRAM (Reference level=1.3V)



M74AS241P

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74AS241P is a semiconductor integrated circuit consisting of two blocks of buffers with 3-state noninverted outputs and independent output control for each block.

FEATURES

- Complementary output control inputs ($1\overline{OC}$, 2OC)
- High fan-out, 3-state output (I_{OL}=64mA, I_{OH}=−15mA)
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

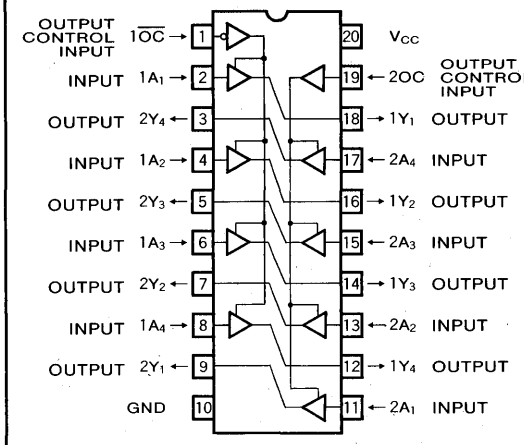
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

When output control input $1\overline{OC}$ is low-level, and if input 1A is low, then output 1Y is low. If 1A is high, 1Y is high. When 2OC is high and input 2A is low, then output 2Y is low, but if 2A is high then 2Y is high. If $1\overline{OC}$ and 2OC are high and low respectively, then all outputs are in high-impedance state.

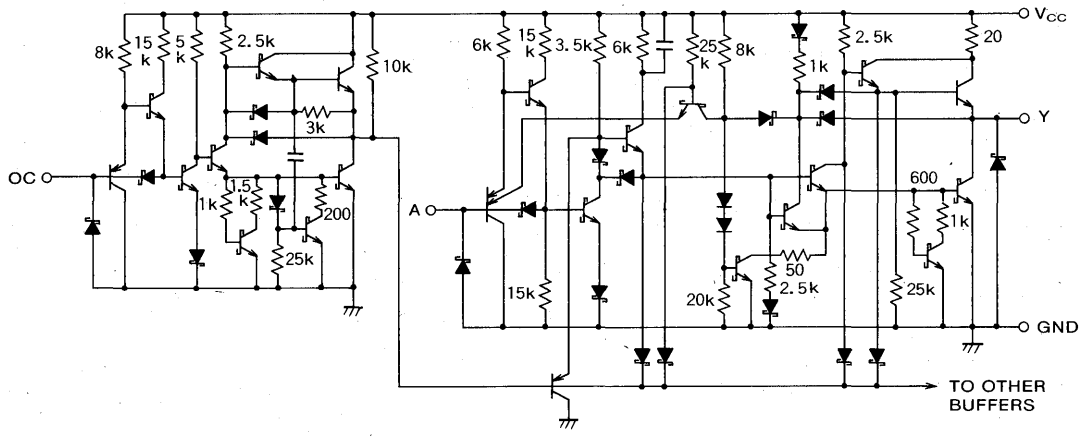
The device can be used as a 4-bit two-way bus driver by connecting $1\overline{OC}$ and 2OC, 1A and 2Y, 2A and 1Y respectively.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

FUNCTION TABLE (Note 1)

Inputs		Output
1A	$1\overline{OC}$	1Y
L	L	L
H	L	H
X	H	Z

Inputs		Output
2A	2OC	2Y
L	H	L
H	H	H
X	L	Z

Note 1: Z : High-impedance state
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state or high-impedance state	−0.5∼+5.5	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−15	mA
I_{OL}	Low-level output current	0		64	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
			V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.4		
				I_{OH}=−15mA	2.4			
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=64mA				0.55	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.5V, V_O=2.7V				50	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.5V, V_O=0.4V				−50	μA
I_I	Input current at maximum voltage		V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current		V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	A	V_{CC}=5.5V, V_I=0.4V				−1	mA
		$\overline{OC}$, OC					−0.5	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V		−50		−150	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.5V			22	35	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.5V			61	90	mA
I_{CCZ}	Supply current, all outputs disabled		V_{CC}=5.5V			35	56	mA

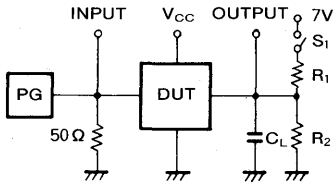
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Input	Output	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 2), C_L=50pF, R_1=500Ω, R_2=500Ω; T_a=0~70℃ Min	Typ*	Max	T_a=−20~+75℃ Min	Typ*	Max	Unit
t_{PLH}	Propagation time	A	Y	2		6.2	2		7	ns
t_{PHL}				2		6.2	2		7	
t_{PZH}	Output enable time	$1\overline{OC}$	Y	2		9	2		10	ns
t_{PZL}				2		7.5	2		8	
t_{PHZ}	Output disable time	$1\overline{OC}$	Y	2		6	2		6.5	ns
t_{PLZ}				2		9	2		10	
t_{PZH}	Output enable time	2OC	Y	3		10.5	3		11	ns
t_{PZL}				3		8.5	3		9.5	
t_{PHZ}	Output disable time	2OC	Y	3		7	3		7.5	ns
t_{PLZ}				3		12	3		13	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 2: Measurement circuit

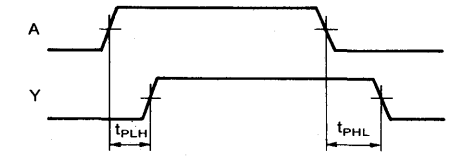


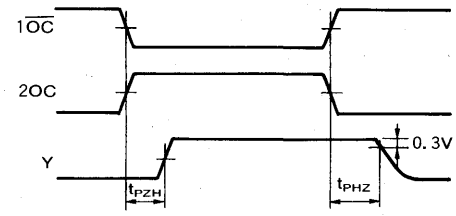
(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

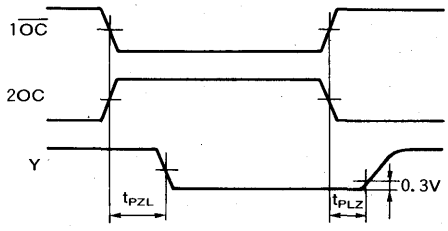
(2) C_L includes probe and jig capacitance.

Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

TIMING DIAGRAM (Reference level=1.3V)







M74AS244P

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74AS244P is a semiconductor integrated circuit consisting of two blocks of buffers with 3-state noninverted outputs and independent output control for each block.

FEATURES

- In-phase output control inputs ($1\overline{OC}$, $2\overline{OC}$)
- High fan-out, 3-state output (I_{OL}=64mA, I_{OH}=−15mA)
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

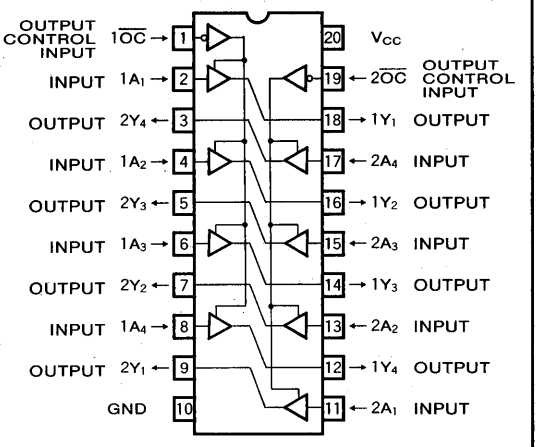
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

When output control input $\overline{OC}$ is low-level, and if input A is low, then output Y is low. If A is high, Y is high. When $\overline{OC}$ is high, Y_1 ~ Y_4 are in high-impedance state irrespective of the status of A.

The outputs of all eight buffers can be controlled simultaneously by connecting $1\overline{OC}$ and $2\overline{OC}$.

PIN CONFIGURATION (TOP VIEW)



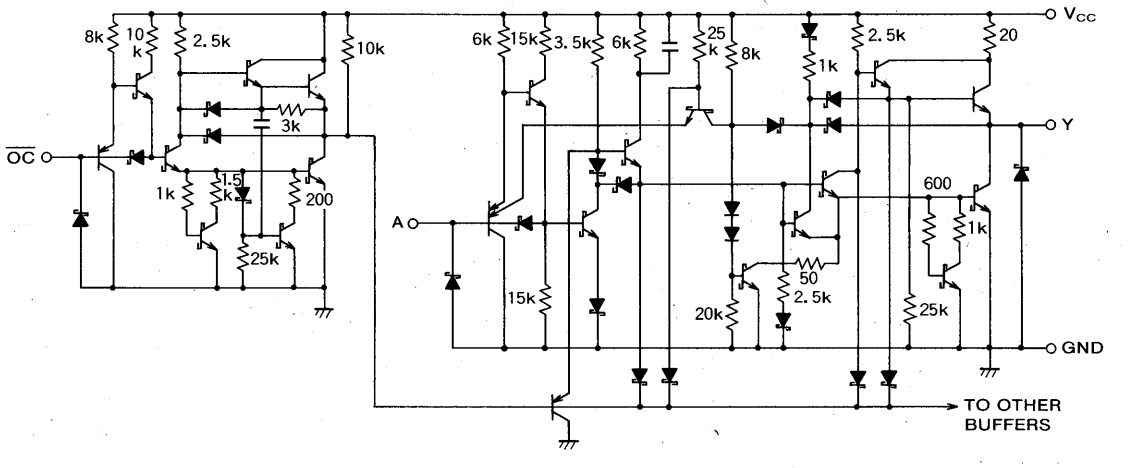
Outline 20P4

FUNCTION TABLE (Note 1)

Inputs		Output
A	$\overline{OC}$	Y
L	L	L
H	L	H
X	H	Z

Note 1: Z : High-impedance state
X : Irrelevant

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

MITSUBISHI ELECTRIC

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state or high-impedance state	−0.5∼+5.5	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−15	mA
I_{OL}	Low-level output current	0		64	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
		V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.4		
			I_{OH}=−15mA	2.4			
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=64mA				0.55	V
I_{OZH}	Off-state high-level output current	V_{CC}=5.5V, V_O=2.7V				50	μA
I_{OZL}	Off-state low-level output current	V_{CC}=5.5V, V_O=0.4V				−50	μA
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current $\overline{OC}$	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
	Low-level input current A					−1	
I_O	Output current	V_{CC}=5.5V, V_O=2.25V		−50		−150	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V			22	34	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V			60	90	mA
I_{CCZ}	Supply current, all outputs disabled	V_{CC}=5.5V			34	54	mA

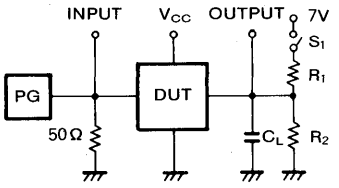
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Input	Output	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 2), C_L=50pF, R_1=500Ω, R_2=500Ω; T_a=0~70℃ Min	Typ*	Max	T_a=−20~+75℃ Min	Typ*	Max	Unit
t_{PLH}	Propagation time	A	Y	2		6.2	2		7	ns
t_{PHL}				2		6.2	2		7	
t_{PZH}	Output enable time	$\overline{OC}$	Y	2		9	2		10	ns
t_{PZL}				2		7.5	2		8	
t_{PHZ}	Output disable time	$\overline{OC}$	Y	2		6	2		6.5	ns
t_{PLZ}				2		9	2		10	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 2: Measurement circuit

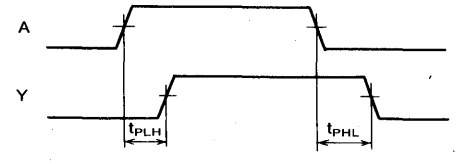


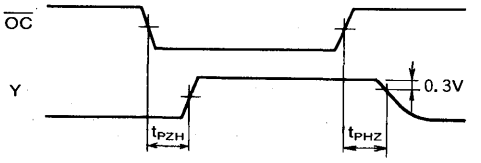
(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

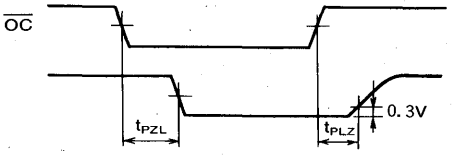
(2) C_L includes probe and jig capacitance.

Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

TIMING DIAGRAM (Reference level=1.3V)







M74AS245P

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74AS245P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state noninverted outputs.

FEATURES

- Two-way transmission or isolation between two 8-bit data
- High fan-out (I_{OL}=48mA, I_{OH}=−15mA)
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

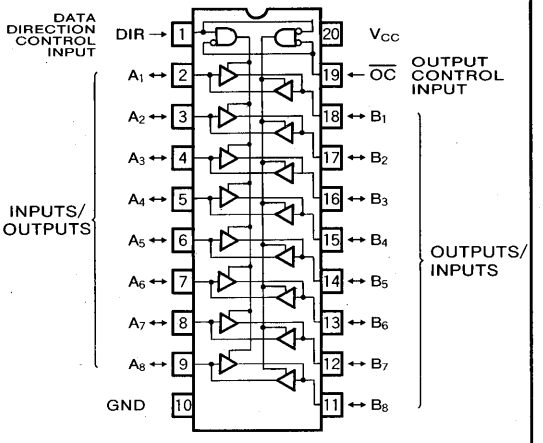
FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with 3-state noninverted outputs.

The input/output direction is controlled by DIR.

When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins. When $\overline{OC}$ is high, both A and B are in the high-impedance state and A and B are isolated.

PIN CONFIGURATION (TOP VIEW)



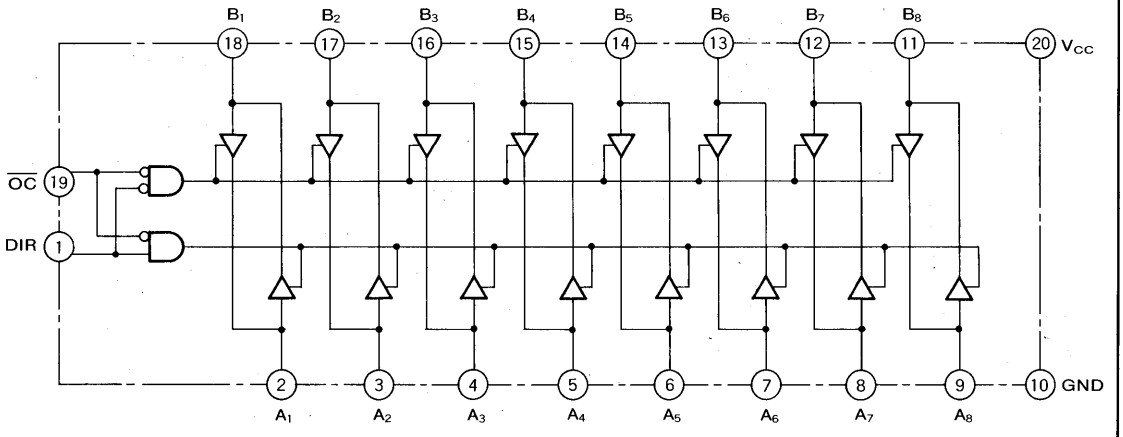
Outline 20P4

FUNCTION TABLE (Note 1)

Inputs		Input/Output	
$\overline{OC}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

Note 1: I : Input pins
O :Output pins (noninverted output)
Z :High-impedance state (A and B are isolated)
X : Irrelevant

LOGIC DIAGRAM



OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5∼+7	V
V_I	Input voltage	A, B		−0.5∼+5.5	V
		DIR, $\overline{OC}$		−0.5∼+7	
V_O	Output voltage		High-level state or high-impedance state	−0.5∼+5.5	V
T_{opr}	Operating free-air ambient temperature range			−20∼+75	℃
T_{stg}	Storage temperature range			−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−15	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
			V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
				I_{OH}=−15mA	2			
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=48mA				0.5	V
I_I	Input current at maximum voltage	DIR, $\overline{OC}$	V_{CC}=5.5V, V_I=7V				0.1	mA
		A, B	V_{CC}=5.5V, V_I=5.5V				0.1	
I_{IH}	High-level input current (Note 2)	DIR, $\overline{OC}$	V_{CC}=5.5V, V_I=2.7V				20	μA
		A, B					70	
I_{IL}	Low-level input current (Note 3)	DIR, $\overline{OC}$	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
		A, B					−0.75	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V		−50		−150	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.5V			62	97	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.5V			95	143	mA
I_{CCZ}	Supply current, all outputs disabled		V_{CC}=5.5V			79	123	mA

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 2: For A and B, I_{IH} includes off-state high-level output current I_{OZH}.

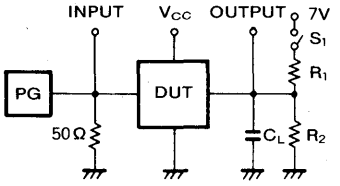
Note 3: For A and B, I_{IL} includes off-state low-level output current I_{OZL}.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Inputs	Outputs	Test conditions/Limits: V_{CC}=4.5~5.5V, C_L=50pF, R_1=500Ω, R_2=500Ω (Note 4)						Unit
				T_a=0~70℃			T_a=−20~+75℃			
				Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A, B	B, A	2		7.5	2		8.5	ns
t_{PHL}				2		7	2		8	
t_{PZH}	Output enable time	$\overline{OC}$	A, B	2		9	2		10	ns
t_{PZL}				2		8.5	2		9.5	
t_{PHZ}	Output disable time	$\overline{OC}$	A, B	2		5.5	2		6	ns
t_{PLZ}				2		9.5	2		10.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 4: Measurement circuit

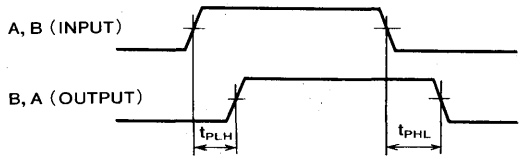


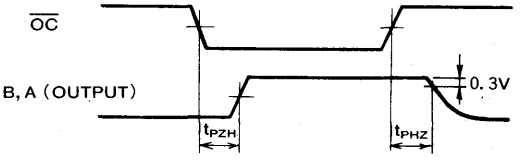
(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

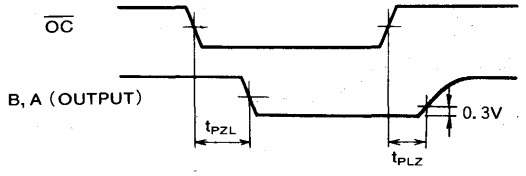
(2) C_L includes probe and jig capacitance.

Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

TIMING DIAGRAM (Reference level=1.3V)







PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M74AS257P

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

DESCRIPTION

The M74AS257P is a semiconductor integrated circuit consisting of four 2-line to 1-line data selector/multiplexer circuits with 3-state outputs.

FEATURES

- Output control input common to all 4 circuits
- Select input common to all 4 circuits
- High fan-out, 3-state output (I_{OL}=48mA, I_{OH}=−15mA)
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

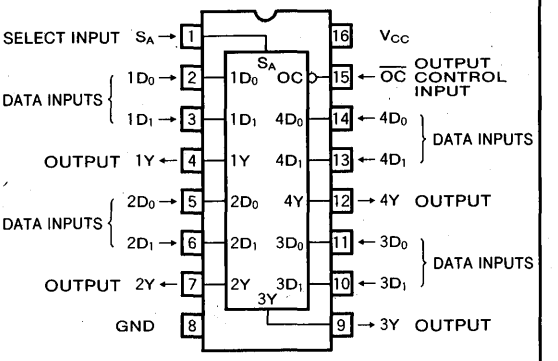
FUNCTIONAL DESCRIPTION

This IC has four data selector circuits which provide 1-line selection of 2 input signals. They can also be used as four multiplexer circuits which convert 2-bit parallel data into serial data by time-sharing. When 2-line signals are applied to the data inputs D_0 and D_1, 1 data input is specified at select input S_A, the specified signal is output at Y.

S_A and output control $\overline{OC}$ are common to all four circuits. When $\overline{OC}$ is set high, 1Y, 2Y, 3Y and 4Y are put in the high-impedance state irrespective of the status of the other inputs.

M74AS257P has the same functions and pin connections as M74AS157P but the latter is provided with active pull-up outputs.

PIN CONFIGURATION (TOP VIEW)



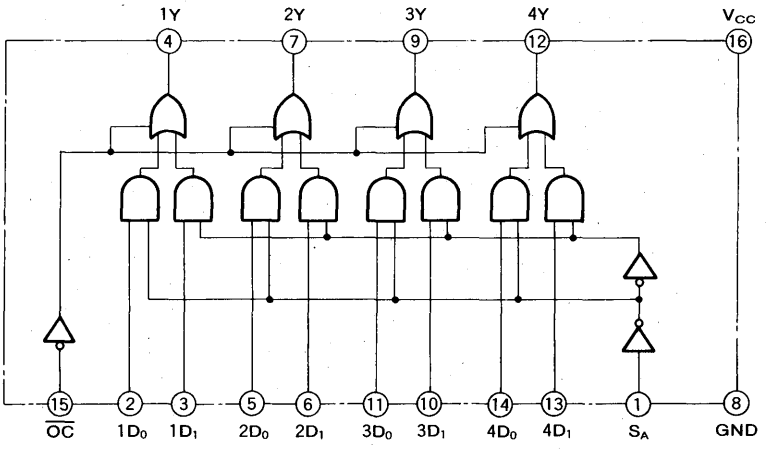
Outline 16P4

FUNCTION TABLE (Note 1)

Inputs				Output
$\overline{OC}$	S_A	D_0	D_1	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Note 1. X: Irrelevant
Z: High-impedance state

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state or high-impedance state	−0.5∼+5.5	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−15	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
			V_{CC}=4.5V, I_{OH}=−15mA	2.4	3.2		
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=48mA			0.5	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.5V, V_O=2.7V			50	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.5V, V_O=0.4V			−50	μA
I_I	Input current at maximum voltage	S_A	V_{CC}=5.5V, V_I=7V			0.2	mA
		D_0, D_1, $\overline{OC}$				0.1	
I_{IH}	High-level input current	S_A	V_{CC}=5.5V, V_I=2.7V			40	μA
		D_0, D_1, $\overline{OC}$				20	
I_{IL}	Low-level input current	S_A	V_{CC}=5.5V, V_I=0.4V			−1	mA
		D_0, D_1, $\overline{OC}$				−0.5	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.5V		12.1	19.7	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.5V		19	30.6	mA
I_{CCZ}	Supply current, all outputs disabled		V_{CC}=5.5V		19.7	31.9	mA

*: All typical values are at V_{CC}=5V, T_a=25℃.

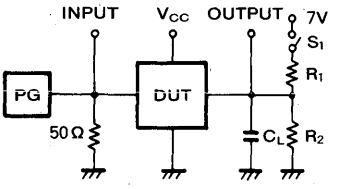
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

SWITCHING CHARACTERISTICS

Symbol	Parameter			Test conditions/Limits: V_{CC}=4.5~5.5V (Note 2), C_L=50pF, R_1=500Ω, R_2=500Ω						Unit
				T_a=0~70℃			T_a=−20~+75℃			
		Inputs	Output	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	D_0, D_1	Y	1		5.5	1		6	ns
t_{PHL}				1		6	1		6.5	
t_{PLH}		S_A	Y	2		11	2		12	ns
t_{PHL}				2		10	2		11	
t_{PZH}	Output enable time	$\overline{OC}$	Y	2		7.5	2		8	ns
t_{PZL}				2		9.5	2		10.5	
t_{PHZ}	Output disable time	$\overline{OC}$	Y	1.5		6.5	1.5		7	ns
t_{PLZ}				2		7	2		7.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 2: Measurement circuit

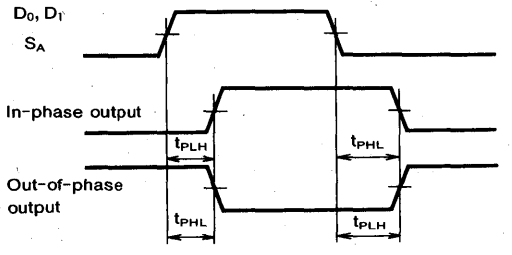


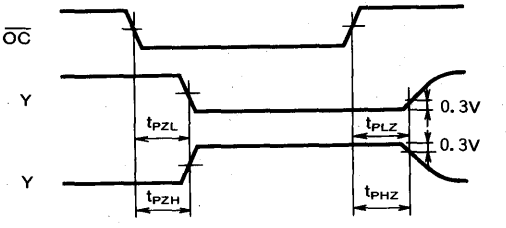
(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

TIMING DIAGRAM (Reference level = 1.3V)





MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change

M74AS258P

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74AS258P is a semiconductor integrated circuit consisting of four 2-line to 1-line data selector/multiplexer circuits with 3-state outputs.

FEATURES

- Inverted outputs
- Output control input common to all 4 circuits
- Select input common to all 4 circuits
- High fan-out, 3-state output (I_{OL}=48mA, I_{OH}=−15mA)
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

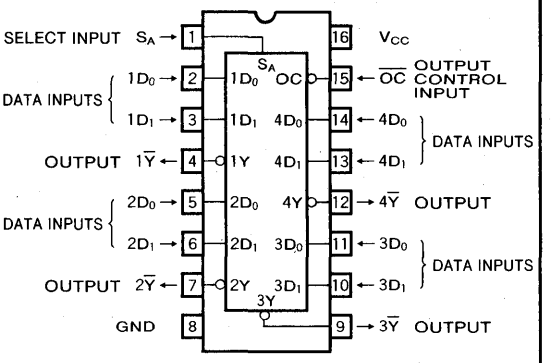
FUNCTIONAL DESCRIPTION

This IC has four data selector circuits which provide 1-line selection of 2 input signals. They can also be used as four multiplexer circuits which convert 2-bit parallel data into serial data by time-sharing. When 2-line signals are applied to the data inputs D_0 and D_1, and 1 data input is specified at select input S_A, the specified signal appears inverted at $\overline{Y}$.

S_A and output control $\overline{OC}$ are common to all four circuits. When $\overline{OC}$ is set high, $1\overline{Y}$, $2\overline{Y}$, $3\overline{Y}$ and $4\overline{Y}$ are put in the high-impedance state irrespective of the status of the other inputs.

M74AS258P has the same functions and pin connections as M74AS158P but the latter is provided with active pull-up outputs.

PIN CONFIGURATION (TOP VIEW)



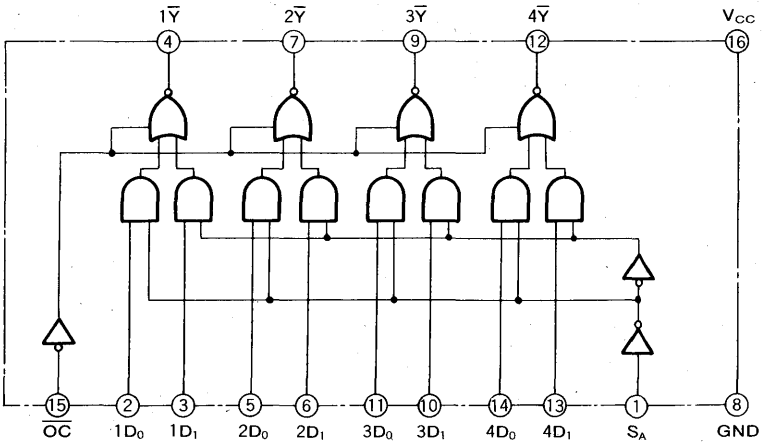
Outline 16P4

FUNCTION TABLE (Note 1)

Inputs				Output
$\overline{OC}$	S_A	D_0	D_1	$\overline{Y}$
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

Note 1. X: Irrelevant
Z: High-impedance state

LOGIC DIAGRAM



QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state or high-impedance state	−0.5∼+5.5	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−15	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
			V_{CC}=4.5V, I_{OH}=−15mA	2.4	3.2		
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=48mA			0.5	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.5V, V_O=2.7V			50	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.5V, V_O=0.4V			−50	μA
I_I	Input current at maximum voltage	S_A	V_{CC}=5.5V, V_I=7V			0.2	mA
		D_0, D_1, $\overline{OC}$				0.1	
I_{IH}	High-level input current	S_A	V_{CC}=5.5V, V_I=2.7V			40	μA
		D_0, D_1, $\overline{OC}$				20	
I_{IL}	Low-level input current	S_A	V_{CC}=5.5V, V_I=0.4V			−1	mA
		D_0, D_1, $\overline{OC}$				−0.5	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.5V		8.4	13.5	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.5V		15.2	24.6	mA
I_{CCZ}	Supply current, all outputs disabled		V_{CC}=5.5V		15.5	25.2	mA

*: All typical values are at V_{CC}=5V, T_a=25℃.

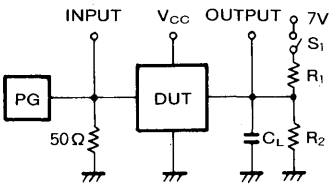
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

SWITCHING CHARACTERISTICS

Symbol	Parameter	Inputs	Output	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 2), C_L=50pF, R_1=500Ω, R_2=500Ω; T_a=0~70℃ Min	T_a=0~70℃ Typ*	T_a=0~70℃ Max	T_a=−20~+75℃ Min	T_a=−20~+75℃ Typ*	T_a=−20~+75℃ Max	Unit
t_{PLH}	Propagation time	D_0, D_1	$\overline{Y}$	1		5	1		5.5	ns
t_{PHL}				1		4	1		4.5	
t_{PLH}		S_A	$\overline{Y}$	2		9.5	2		10.5	ns
t_{PHL}				2		10	2		11	
t_{PZH}	Output enable time	$\overline{OC}$	$\overline{Y}$	2		8	2		8.5	ns
t_{PZL}				2		10	2		11	
t_{PHZ}	Output disable time	$\overline{OC}$	$\overline{Y}$	1.5		6	1.5		6.5	ns
t_{PLZ}				2		6.5	2		7	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 2: Measurement circuit

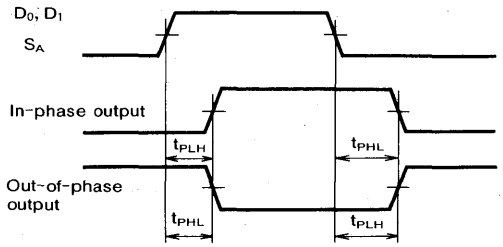


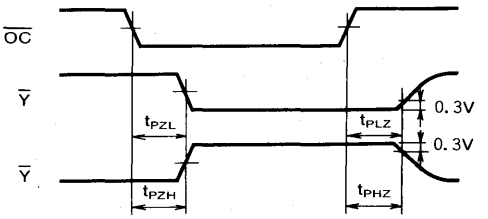
(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

TIMING DIAGRAM (Reference level = 1.3V)





M74AS373P

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74AS373P is a semiconductor integrated circuit consisting of eight D-type latch circuits with 3-state noninverted output and is provided with an output control input and an enable input, both common to all circuits.

FEATURES

- 3-state, high fan-out output (I_{OL}=48mA, I_{OH}=−15mA)
- High package density with eight circuits in one package
- Output control and enable inputs common to all eight circuits
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

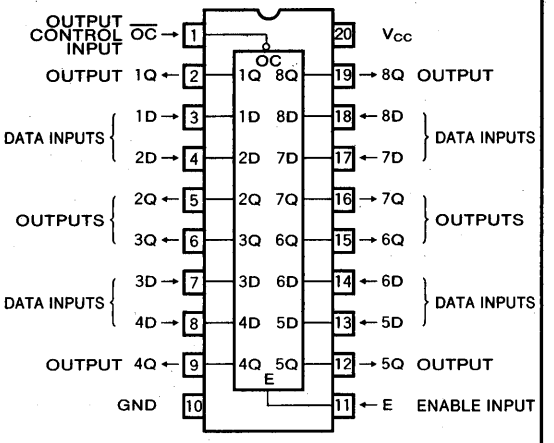
FUNCTIONAL DESCRIPTION

The eight D-type latch circuits have the common output control $\overline{OC}$ and enable input E. While E is high, the information from D appears at the output Q and Q changes with D. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of Q is retained even if D changes.

While $\overline{OC}$ is high, 1Q~8Q are in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While Q is "Z", old data can be retained or new data can be entered.

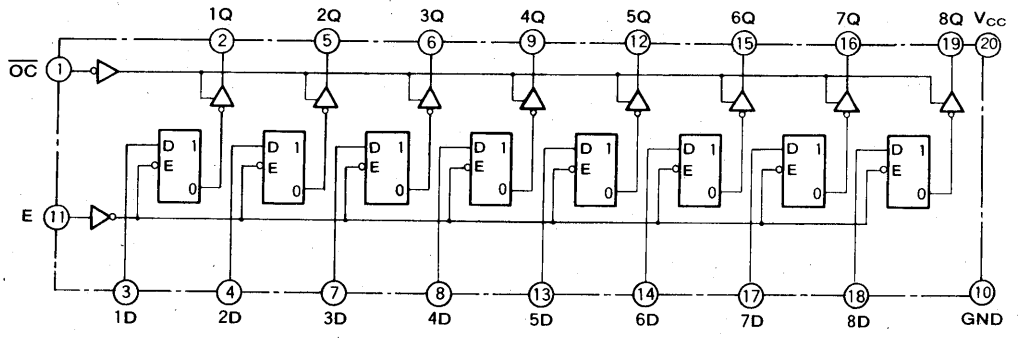
Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bi-directional bus driver.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (NONINVERTED)

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OC}$*	E	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q^0
H	X	X	Z

Note 1. Q^0 : Level of Q before the indicated steady-state input conditions were established
Z : High-impedance state
X : Irrelevant
* : Data can be latched irrespective of $\overline{OC}$.

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state or high-impedance state	−0.5∼+5.5	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−15	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
		V_{CC}=4.5V, I_{OH}=−15mA	2.4	3.3		
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=48mA			0.5	V
I_{OZH}	Off-state high-level output current	V_{CC}=5.5V, V_O=2.7V			50	μA
I_{OZL}	Off-state low-level output current	V_{CC}=5.5V, V_O=0.4V			−50	μA
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V			20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V		55	90	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V		55	85	mA
I_{CCZ}	Supply current, all outputs disabled	V_{CC}=5.5V		65	100	mA

*: All typical values are at V_{CC}=5V, T_a=25℃.

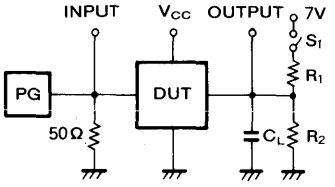
OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (NONINVERTED)

SWITCHING CHARACTERISTICS

Symbol	Parameter	Input	Outputs	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 2), C_L=50pF, R_1=500Ω, R_2=500Ω; T_a=0~70℃ Min	Typ*	Max	T_a=−20~+75℃ Min	Typ*	Max	Unit
t_{PLH}	Propagation time	1D~8D	1Q~8Q	3.5		6	3.5		6.5	ns
t_{PHL}				3.5		6	3.5		6.5	
t_{PLH}		E	1Q~8Q	6.5		11.5	6.5		12.5	ns
t_{PHL}				5		7.5	5		8	
t_{PZH}	Output enable time	$\overline{OC}$	1Q~8Q	2		6.5	2		7	ns
t_{PZL}				4.5		9.5	4.5		10.5	
t_{PHZ}	Output disable time	$\overline{OC}$	1Q~8Q	3		6.5	3		7	ns
t_{PLZ}				3		7	3		7.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

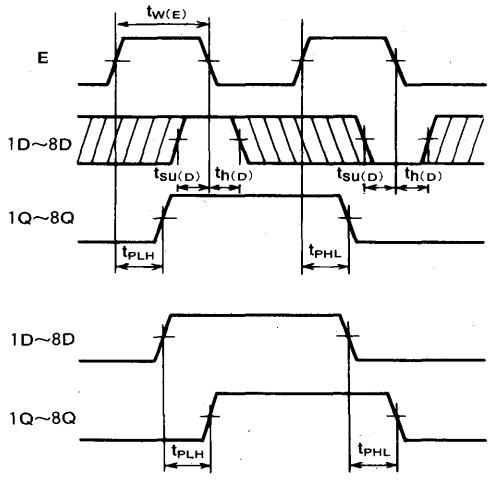
TIMING REQUIREMENTS (V_{CC}=4.5V~5.5V, C_L=50pF, R_2=500Ω)

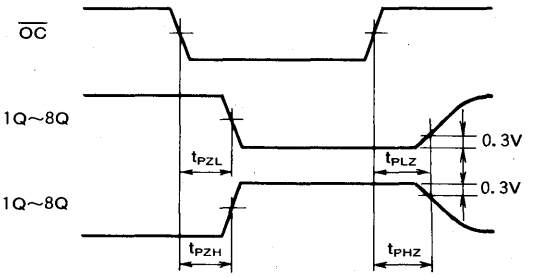
Symbol	Parameter		Limits: T_a=0~70℃ Min	Typ*	Max	T_a=−20~+75℃ Min	Typ*	Max	Unit
$t_{W(E)}$	Pulse width	E "H"	4.5			5			ns
$t_{su(D)}$	Setup time before E↓	1D~8D	2			2			ns
$t_{h(D)}$	Hold time after E↓	1D~8D	3			3			ns

*: All typical values are at V_{CC}=5V, T_a=25℃.
↓: Transition from high to low

OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (NONINVERTED)

TIMING DIAGRAM (Reference level=1.3V)





Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

M74AS374P

OCTAL D-TYPE EDGE-TRIGGERED FLIP FLOP WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74AS374P is a semiconductor integrated circuit consisting of eight D-type positive edge-triggered flip-flop circuits with 3-state noninverted output and is provided with an output control and a clock input, both common to all circuits.

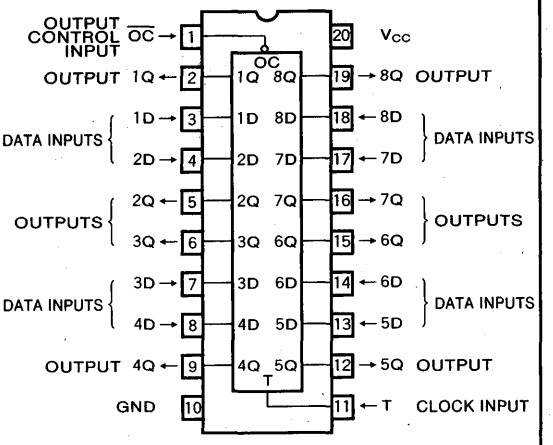
FEATURES

- Positive edge triggering
- 3-state, high fan-out output (I_{OL}=48mA, I_{OH}=−15mA)
- High package density with eight circuits in one package
- Output control and clock inputs common to all eight circuits
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



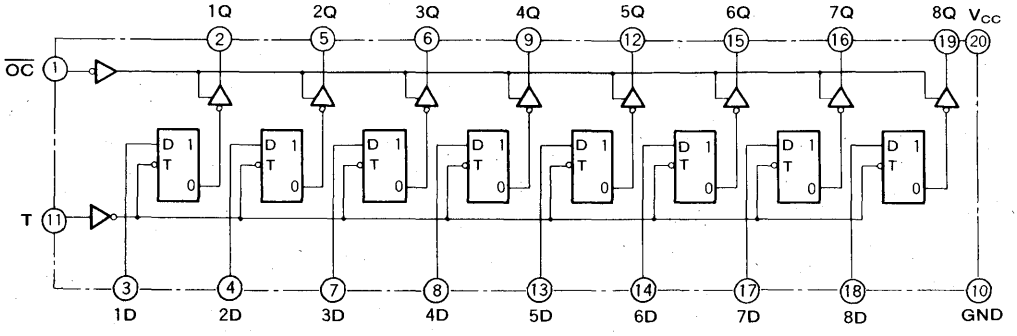
Outline 20P4

FUNCTIONAL DESCRIPTION

The eight D-type edge-triggered flip-flop circuits have the common output control $\overline{OC}$ and clock input T. When T changes from low to high, the status of D immediately before the change appears on the output Q in accordance with the function table.

While $\overline{OC}$ is high, 1Q~8Q are in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While Q is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

LOGIC DIAGRAM



OCTAL D-TYPE EDGE-TRIGGERED FLIP FLOP WITH 3-STATE OUTPUT (NONINVERTED)

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OC}$*	T	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q^0
H	X	X	Z

Note 1. ↑ : Transition from low to high level (positive edge trigger)
Q^0 : Level of Q before the indicated input conditions were established
Z : High-impedance state
X : Irrelevant
* : Data can be stored irrespective of $\overline{OC}$.

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state or high-impedance state	−0.5∼+5.5	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−15	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
			V_{CC}=4.5V, I_{OH}=−15mA	2.4	3.3		
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=48mA			0.5	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.5V, V_O=2.7V			50	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.5V, V_O=0.4V			−50	μA
I_I	Input current at maximum voltage		V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current		V_{CC}=5.5V, V_I=2.7V			20	μA
I_{IL}	Low-level input current	T, $\overline{OC}$	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
		D				−2	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.5V		77	120	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.5V		84	128	mA
I_{CCZ}	Supply current, all outputs disabled		V_{CC}=5.5V		84	128	mA

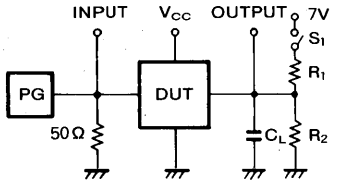
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter			Test conditions/Limits: V_{CC}=4.5~5.5V (Note 2), C_L=50pF, R_1=500Ω, R_2=500Ω						Unit
				T_a=0~70℃			T_a=−20~+75℃			
		Input	Outputs	Min	Typ*	Max	Min	Typ*	Max	
f_{max}	Maximum clock frequency	T	1Q~8Q	125			110			MHz
t_{PLH}	Propagation time	T	1Q~8Q	3		8	3		9	ns
t_{PHL}				4		9	4		10	
t_{PZH}	Output enable time	$\overline{OC}$	1Q~8Q	2		6	2		6.5	ns
t_{PZL}				3		10	3		11	
t_{PHZ}	Output disable time	$\overline{OC}$	1Q~8Q	2		6	2		6.5	ns
t_{PLZ}				2		6	2		6.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

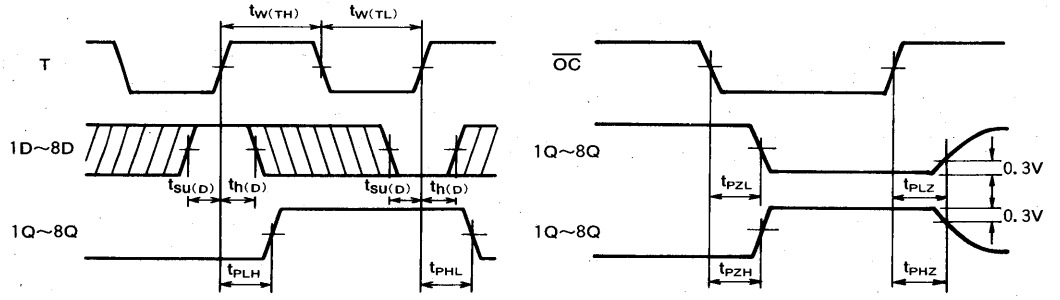
Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

TIMING REQUIREMENTS (V_{CC}=4.5V~5.5V, C_L=50pF, R_2=500Ω)

Symbol	Parameter		Limits: T_a=0~70℃ Min	Typ*	Max	T_a=−20~+75℃ Min	Typ*	Max	Unit
$t_{W(TH)}$	Pulse width	T "H"	4			4.5			ns
$t_{W(TL)}$		T "L"	3			3.5			
$t_{su(D)}$	Setup time before T↑	1D~8D	2			2.5			ns
$t_{h(D)}$	Hold time after T↑	1D~8D	2			2.5			ns

*: All typical values are at V_{CC}=5V, T_a=25℃.
↑: Transition from low to high (positive edge trigger)

TIMING DIAGRAM (Reference level=1.3V)



Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M74AS533P

OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74AS533P is a semiconductor integrated circuit consisting of eight D-type latch circuits with 3-state inverted output and is provided with an output control and an enable input, both common to all circuits.

FEATURES

- 3-state, high fan-out output (I_{OL}=48mA, I_{OH}=−15mA)
- High package density with eight circuits in one package
- Output control and enable inputs common to all eight circuits
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

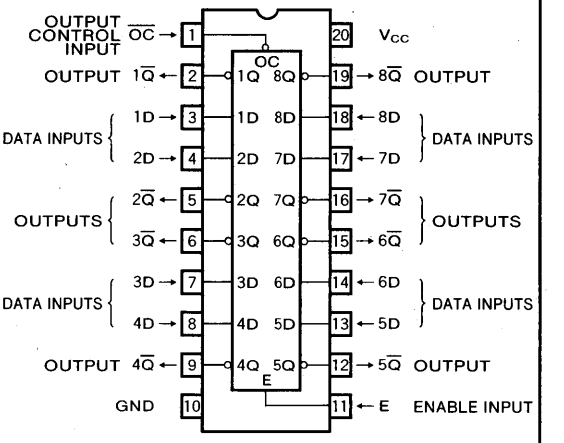
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

The eight D-type latch circuits have the common output control $\overline{OC}$ and enable input E. While E is high, the information from D appears inverted at the output $\overline{Q}$ and $\overline{Q}$ changes with D. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of $\overline{Q}$ is retained even if D changes.

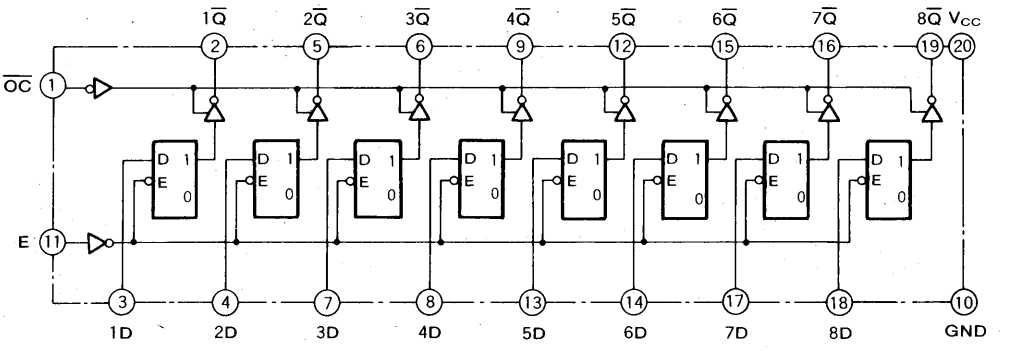
While $\overline{OC}$ is high, $1\overline{Q}$~$8\overline{Q}$ are in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While $\overline{Q}$ is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

LOGIC DIAGRAM



OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (INVERTED)

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OC}$*	E	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}^0$
H	X	X	Z

Note 1. $\overline{Q}^0$: Level of $\overline{Q}$ before the indicated input conditions were established
Z : High-impedance state
X : Irrelevant
* : Data can be stored irrespective of $\overline{OC}$

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state or high-impedance state	−0.5∼+5.5	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−15	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
		V_{CC}=4.5V, I_{OH}=−15mA	2.4	3.3		
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=48mA			0.5	V
I_{OZH}	Off-state high-level output current	V_{CC}=5.5V, V_O=2.7V			50	μA
I_{OZL}	Off-state low-level output current	V_{CC}=5.5V, V_O=0.4V			−50	μA
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V			20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V		62	100	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V		64	100	mA
I_{CCZ}	Supply current, all outputs disabled	V_{CC}=5.5V		71	110	mA

*: All typical values are at V_{CC}=5V, T_a=25℃.

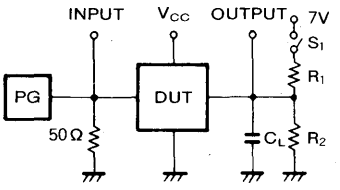
OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUT (INVERTED)

SWITCHING CHARACTERISTICS

Symbol	Parameter			Test conditions/Limits: V_{CC}=4.5~5.5V (Note 2), C_L=50pF, R_1=500Ω, R_2=500Ω						Unit
				T_a=0~70℃			T_a=−20~+75℃			
		Input	Outputs	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	1D~8D	$1\overline{Q}$~$8\overline{Q}$	4		7.5	4		8.5	ns
t_{PHL}				4		7	4		8	
t_{PLH}		E	$1\overline{Q}$~$8\overline{Q}$	5		9	5		10	ns
t_{PHL}				4.5		8	4.5		9	
t_{PZH}	Output enable time	$\overline{OC}$	$1\overline{Q}$~$8\overline{Q}$	2		6.5	2		7	ns
t_{PZL}				4.5		9.5	4.5		10.5	
t_{PHZ}	Output disable time	$\overline{OC}$	$1\overline{Q}$~$8\overline{Q}$	3		6.5	3		7	ns
t_{PLZ}				3		7	3		8	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

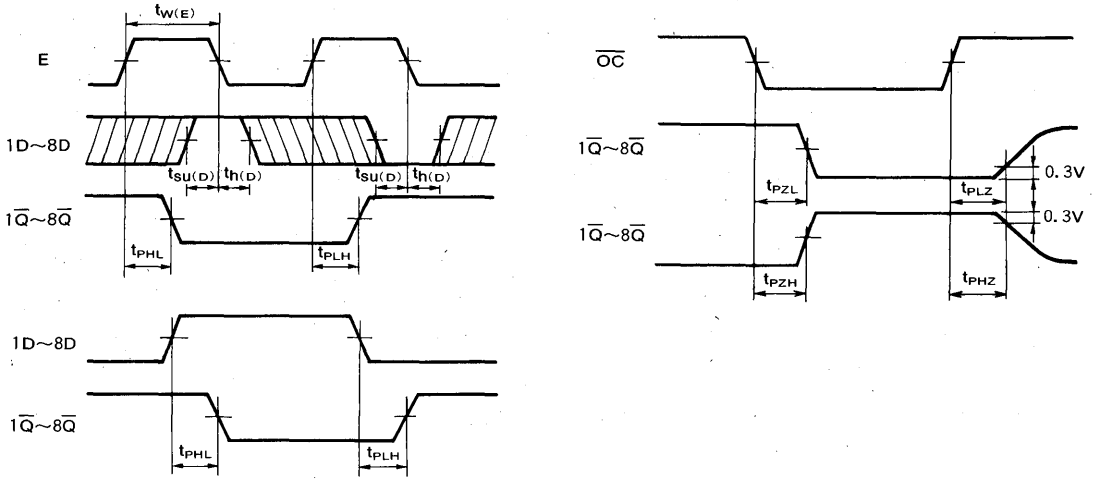
TIMING REQUIREMENTS (V_{CC}=4.5V~5.5V, C_L=50pF, R_2=500Ω)

Symbol	Parameter		Limits: T_a=0~70℃			T_a=−20~+75℃			Unit
			Min	Typ*	Max	Min	Typ*	Max	
$t_{W(E)}$	Pulse width	E "H"	2			2.5			ns
$t_{su(D)}$	Setup time before E↓	1D~8D	2			2			ns
$t_{h(D)}$	Hold time after E↓	1D~8D	3			3			ns

*: All typical values are at V_{CC}=5V, T_a=25℃.

↓: Transition from high to low

TIMING DIAGRAM (Reference level=1.3V)



Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change

M74AS534P

OCTAL D-TYPE EDGE-TRIGGERED FLIP FLOP WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74AS534P is a semiconductor integrated circuit consisting of eight D-type positive edge-triggered flip-flop circuits with 3-state inverted output and is provided with an output control and a clock input, both common to all circuits.

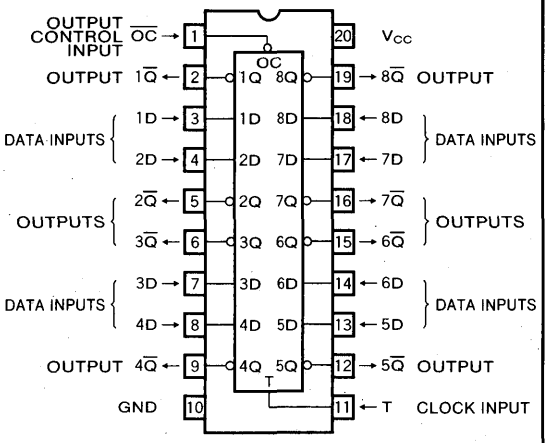
FEATURES

- Positive edge triggering
- 3-state, high fan-out output (I_{OL}=48mA, I_{OH}=−15mA)
- High package density with eight circuits in one package
- Output control and clock inputs common to all eight circuits
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



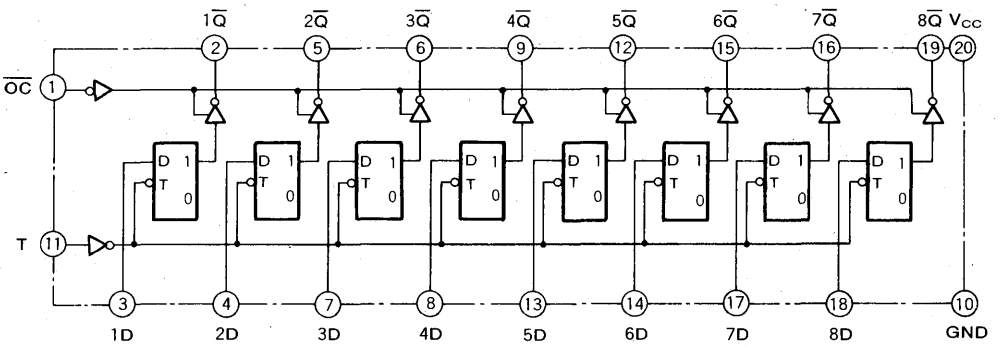
Outline 20P4

FUNCTIONAL DESCRIPTION

This eight D-type edge-triggered flip-flop circuits have the common output control $\overline{OC}$ and clock input T. When T changes from low to high, the status of D immediately before the change appears inverted at the output $\overline{Q}$ in accordance with the function table.

While $\overline{OC}$ is high, $1\overline{Q}$~$8\overline{Q}$ are in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While $\overline{Q}$ is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

LOGIC DIAGRAM



OCTAL D-TYPE EDGE-TRIGGERED FLIP FLOP WITH 3-STATE OUTPUT (INVERTED)

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OC}$*	T	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}^0$
H	X	X	Z

Note 1. ↑ : Transition from low to high level (positive edge trigger)
$\overline{Q}^0$: Level of $\overline{Q}$ before the indicated input conditions were established
Z : High-impedance state
X : Irrelevant
* : Data can be stored irrespective of $\overline{OC}$.

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state or high-impedance state	−0.5∼+5.5	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−15	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
			V_{CC}=4.5V, I_{OH}=−15mA	2.4	3.3		
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=48mA			0.5	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.5V, V_O=2.7V			50	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.5V, V_O=0.4V			−50	μA
I_I	Input current at maximum voltage		V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current		V_{CC}=5.5V, V_I=2.7V			20	μA
I_{IL}	Low-level input current	T, $\overline{OC}$	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
		D				−2	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.5V		77	120	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.5V		84	128	mA
I_{CCZ}	Supply current, all outputs disabled		V_{CC}=5.5V		84	128	mA

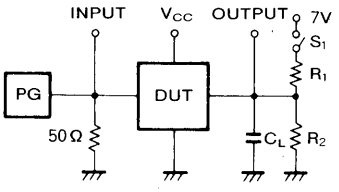
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Input	Outputs	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 2), C_L=50pF, R_1=500Ω, R_2=500Ω; T_a=0~70℃ Min	Typ*	Max	T_a=−20~+75℃ Min	Typ*	Max	Unit
f_{max}	Maximum clock frequency	T	$1\overline{Q}$~$8\overline{Q}$	125			110			MHz
t_{PLH}	Propagation time	T	$1\overline{Q}$~$8\overline{Q}$	3		8	3		9	ns
t_{PHL}				4		9	4		10	
t_{PZH}	Output enable time	$\overline{OC}$	$1\overline{Q}$~$8\overline{Q}$	2		6	2		6.5	ns
t_{PZL}				3		10	3		11	
t_{PHZ}	Output disable time	$\overline{OC}$	$1\overline{Q}$~$8\overline{Q}$	2		6	2		6.5	ns
t_{PLZ}				2		6	2		6.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

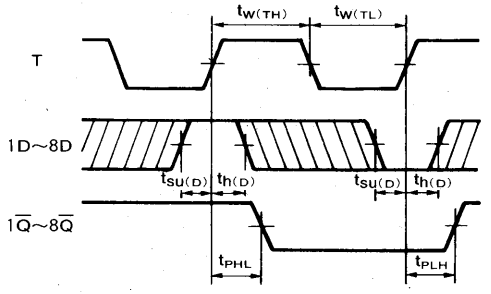
Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

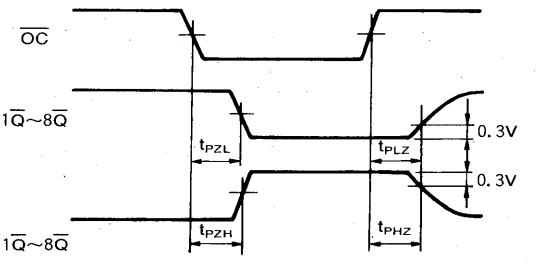
TIMING REQUIREMENTS (V_{CC}=4.5V~5.5V, C_L=50pF, R_2=500Ω)

Symbol	Parameter		Limits: T_a=0~70℃ Min	Typ*	Max	T_a=−20~+75℃ Min	Typ*	Max	Unit
$t_{W(TH)}$	Pulse width	T "H"	4			4.5			ns
$t_{W(TL)}$		T "L"	3			3.5			
$t_{su(D)}$	Setup time before T↑	1D~8D	2			2.5			ns
$t_{h(D)}$	Hold time after T↑	1D~8D	2			2.5			ns

*: All typical values are at V_{CC}=5V, T_a=25℃.
↑: Transition from low to high (positive edge trigger)

TIMING DIAGRAM (Reference level=1.3V)





Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M74AS620P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74AS620P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state inverted outputs.

FEATURES

- Two-way transmission or isolation between two 8-bit data
- High fan-out (I_{OL}=64mA, I_{OH}=−15mA)
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

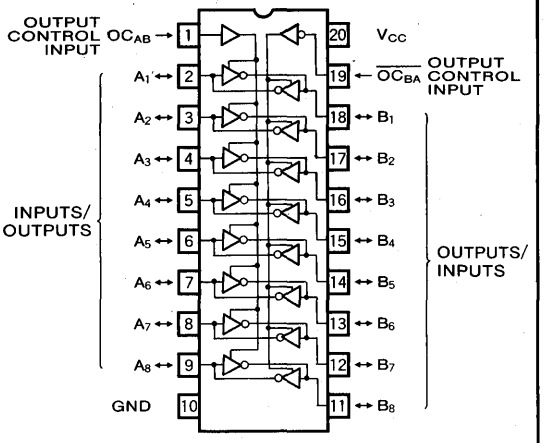
FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with 3-state inverted outputs.

The input/output direction is controlled by OC_{AB} and $\overline{OC_{BA}}$.

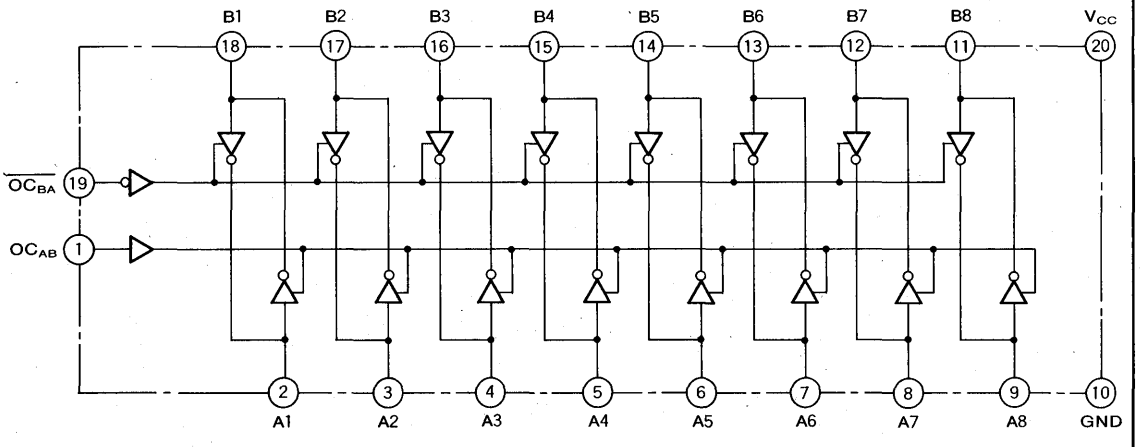
When OC_{AB} and $\overline{OC_{BA}}$ are high, pins A are made the input pins and pins B are made the output pins. When OC_{AB} and $\overline{OC_{BA}}$ are low, B are made the input pins and A are made the output pins. When OC_{AB} is low and $\overline{OC_{BA}}$ is high, both A and B are in the high-impedance state and A and B are isolated. Latch operation is possible when OC_{AB} is high and $\overline{OC_{BA}}$ is low.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

FUNCTION TABLE (Note 1)

Inputs		Input/Output	
$\overline{OC_{BA}}$	OC_{AB}	A	B
L	L	$\overline{O}$	I
H	H	I	$\overline{O}$
H	L	Z	Z
L	H	*	*

Note 1: I : Input pins
$\overline{O}$:Output pins (inverted output)
Z :High-impedance state (A and B are isolated)
* : In this case, data can be latched with the procedure shown below.
(1) Apply the data to be stored to A or B.
(OC_{AB} and $\overline{OC_{BA}}$ must be equally high or equally low.)
(2) Set OC_{AB} high and $\overline{OC_{BA}}$ low respectively.
(3) Remove the data.
(4) The data applied in (1) is stored. If voltage is applied to A or B in this condition, the device may be damaged. Change the status of OC_{AB} or $\overline{OC_{BA}}$ before applying voltage.

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5∼+7	V
V_I	Input voltage	A, B		−0.5∼+5.5	V
		OC_{AB}, $\overline{OC_{BA}}$		−0.5∼+7	
V_O	Output voltage		High-level state or high-impedance state	−0.5∼+5.5	V
T_{opr}	Operating free-air ambient temperature range			−20∼+75	℃
T_{stg}	Storage temperature range			−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−15	mA
I_{OL}	Low-level output current	0		64	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
			V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
				I_{OH}=−15mA	2			
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=64mA				0.55	V
I_I	Input current at maximum voltage	OC_{AB}, $\overline{OC_{BA}}$	V_{CC}=5.5V, V_I=7V				0.1	mA
		A, B	V_{CC}=5.5V, V_I=5.5V				0.1	
I_{IH}	High-level input current (Note 2)	OC_{AB}, $\overline{OC_{BA}}$	V_{CC}=5.5V, V_I=2.7V				20	μA
		A, B					70	
I_{IL}	Low-level input current (Note 3)	OC_{AB}, $\overline{OC_{BA}}$	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
		A, B					−0.75	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V		−50		−150	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.5V			35	57	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.5V			74	122	mA
I_{CCZ}	Supply current, all outputs disabled		V_{CC}=5.5V			48	77	mA

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 2. For A and B, I_{IH} includes off-state high-level output current I_{OZH}.

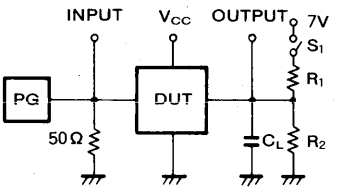
Note 3. For A and B, I_{IL} includes off-state low-level output current I_{OZL}.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Inputs	Outputs	Test conditions/Limits: V_{CC}=4.5~5.5V, C_L=50pF, R_1=500Ω, R_2=500Ω (Note 4)						Unit
				T_a=0~70℃			T_a=−20~+75℃			
				Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A, B	B, A	1		7	1		7.5	ns
t_{PHL}				2		6	2		6.5	
t_{PZH}	Output enable time	$\overline{OC_{BA}}$	A	2		8	2		9	ns
t_{PZL}				2		9	2		10	
t_{PHZ}	Output disable time	$\overline{OC_{BA}}$	A	1		6	1		6.5	ns
t_{PLZ}				2		12	2		13	
t_{PZH}	Output enable time	OC_{AB}	B	2		8	2		9	ns
t_{PZL}				2		9	2		10	
t_{PHZ}	Output disable time	OC_{AB}	B	1		6	1		6.5	ns
t_{PLZ}				2		13	2		14	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 4: Measurement circuit

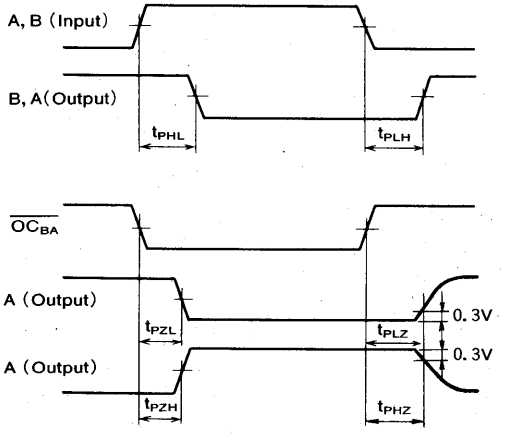


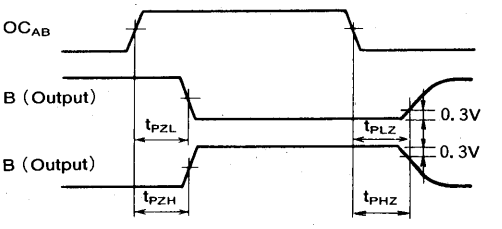
(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

TIMING DIAGRAM (Reference level=1.3V)





PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

M74AS623P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74AS623P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state noninverted outputs.

FEATURES

- Two-way transmission or isolation between two 8-bit data
- High fan-out (I_{OL}=64mA, I_{OH}=−15mA)
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

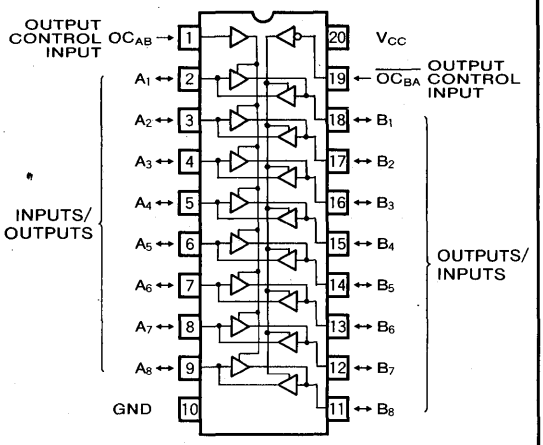
FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with 3-state noninverted outputs.

The input/output direction is controlled by OC_{AB} and $\overline{OC_{BA}}$.

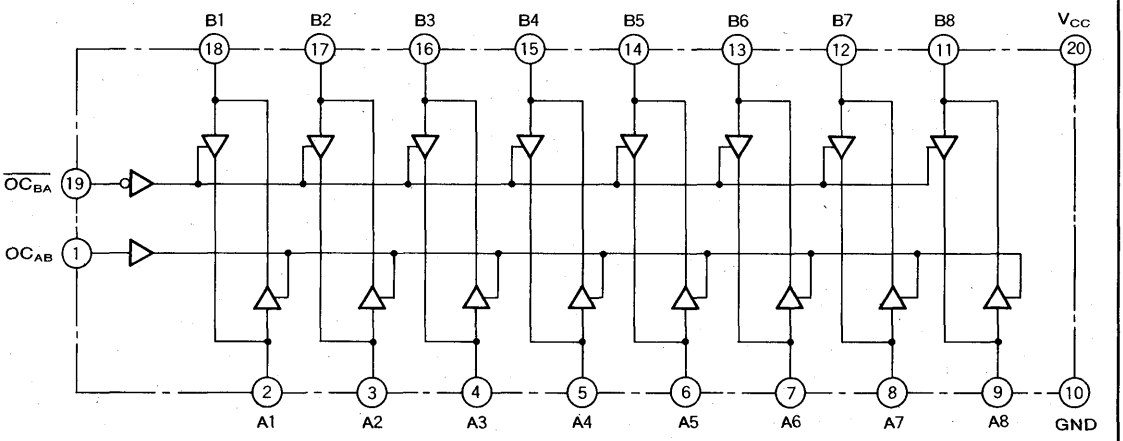
When OC_{AB} and $\overline{OC_{BA}}$ are high, pins A are made the input pins and pins B are made the output pins. When OC_{AB} and $\overline{OC_{BA}}$ are low, B are made the input pins and A are made the output pins. When OC_{AB} is low and $\overline{OC_{BA}}$ is high, both A and B are in the high-impedence state and A and B are isolated. Latch operation is possible when OC_{AB} is high and $\overline{OC_{BA}}$ is low.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

LOGIC DIAGRAM



OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

FUNCTION TABLE (Note 1)

Inputs		Input/Output	
$\overline{OC_{BA}}$	OC_{AB}	A	B
L	L	O	I
H	H	I	O
H	L	Z	Z
L	H	*	*

Note 1: I : Input pins
O : Output pins (non-inverted output)
Z : High-impedance state (A and B are isolated)
* : In this case, data can be latched with the procedure shown below.
(1) Apply the data to be stored to A or B.
(OC_{AB} and $\overline{OC_{BA}}$ must be equally high or equally low.)
(2) Set OC_{AB} high and $\overline{OC_{BA}}$ low respectively.
(3) Remove the data.
(4) The data applied in (1) is stored. If voltage is applied to A or B in this condition, the device may be damaged. Change the status of OC_{AB} or $\overline{OC_{BA}}$ before applying voltage.

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5∼+7	V
V_I	Input voltage	A, B		−0.5∼+5.5	V
		OC_{AB}, $\overline{OC_{BA}}$		−0.5∼+7	
V_O	Output voltage		High-level state or high-impedance state	−0.5∼+5.5	V
T_{opr}	Operating free-air ambient temperature range			−20∼+75	℃
T_{stg}	Storage temperature range			−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−15	mA
I_{OL}	Low-level output current	0		64	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
			V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
				I_{OH}=−15mA	2			
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=64mA				0.55	V
I_I	Input current at maximum voltage	OC_{AB}, $\overline{OC_{BA}}$	V_{CC}=5.5V, V_I=7V				0.1	mA
		A, B	V_{CC}=5.5V, V_I=5.5V				0.1	
I_{IH}	High-level input current (Note 2)	OC_{AB}, $\overline{OC_{BA}}$	V_{CC}=5.5V, V_I=2.7V				20	μA
		A, B					70	
I_{IL}	Low-level input current (Note 3)	OC_{AB}, $\overline{OC_{BA}}$	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
		A, B					−0.75	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V		−50		−150	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.5V			57	93	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.5V			116	189	mA
I_{CCZ}	Supply current, all outputs disabled		V_{CC}=5.5V			71	116	mA

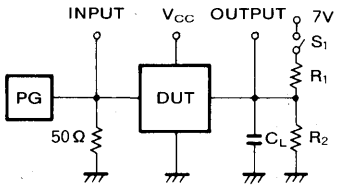
*: All typical values are at V_{CC}=5V, T_a=25℃.
Note 2. For A and B, I_{IH} includes off-state high-level output current I_{OZH}.
Note 3. For A and B, I_{IL} includes off-state low-level output current I_{OZL}.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Input	Output	Test conditions/Limits: V_{CC}=4.5~5.5V, C_L=50pF, R_1=500Ω, R_2=500Ω (Note 4)						Unit
				T_a=0~70℃			T_a=−20~+75℃			
				Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A	B	1		9	1		10	ns
t_{PHL}				1		8	1		9	
t_{PLH}		B	A	1		9	1		10	ns
t_{PHL}				1		8.5	1		9.5	
t_{PZH}	Output enable time	$\overline{OC_{BA}}$	A	2		11	2		12	ns
t_{PZL}				2		10	2		11	
t_{PHZ}	Output disable time	$\overline{OC_{BA}}$	A	1		7.5	1		8	ns
t_{PLZ}				1		11.5	1		12.5	
t_{PZH}	Output enable time	OC_{AB}	B	2		11.5	2		12.5	ns
t_{PZL}				2		11	2		12	
t_{PHZ}	Output disable time	OC_{AB}	B	1		7	1		8	ns
t_{PLZ}				1		9	1		10	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 4: Measurement circuit

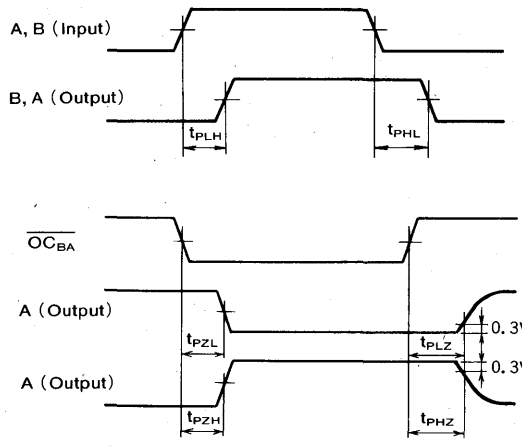


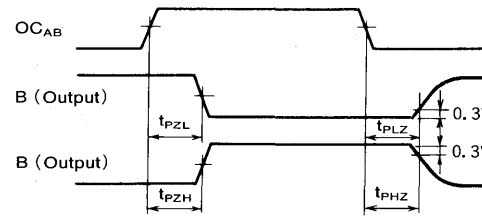
(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

TIMING DIAGRAM (Reference level=1.3V)





PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M74AS640P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74AS640P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state inverted outputs.

FEATURES

- Two-way transmission or isolation between two 8-bit data
- High fan-out (I_{OL}=64mA, I_{OH}=−15mA)
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

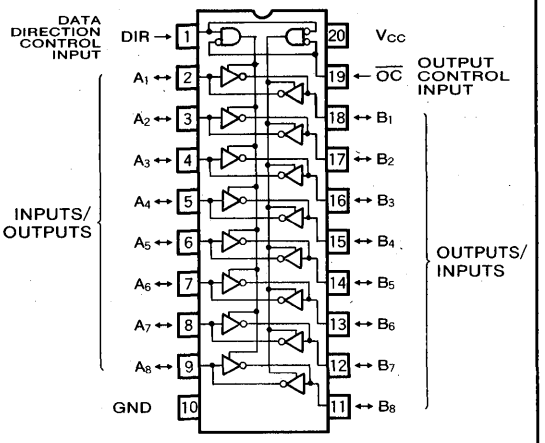
FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with 3-state inverted outputs.

The input/output direction is controlled by DIR.

When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins. When $\overline{OC}$ is high, both A and B are in the high-impedance state and A and B are isolated.

PIN CONFIGURATION (TOP VIEW)



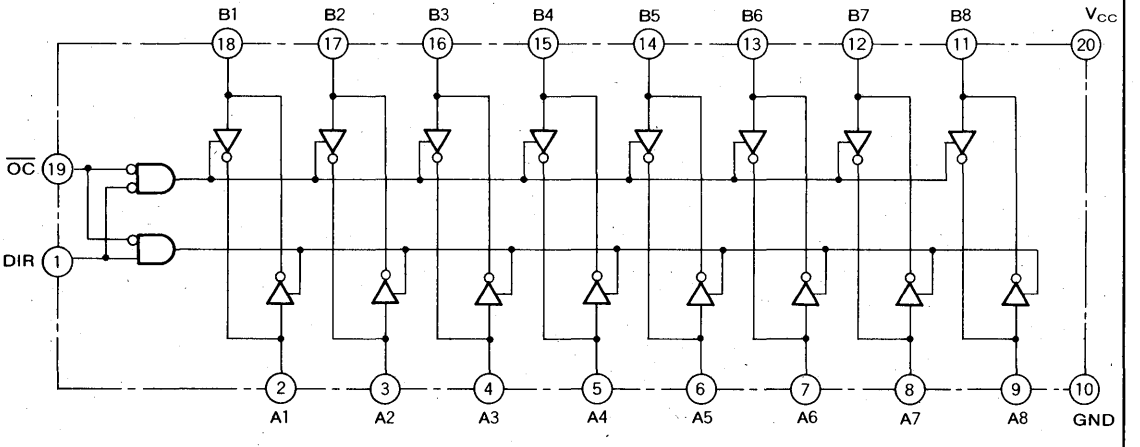
Outline 20P4

FUNCTION TABLE (Note 1)

Inputs		Input/Output	
$\overline{OC}$	DIR	A	B
L	L	$\overline{O}$	I
L	H	I	$\overline{O}$
H	X	Z	Z

Note 1: I : Input pins
$\overline{O}$: Output pins (inverted output)
Z : High-impedance state (A and B are isolated)
X : Irrelevant

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5∼+7	V
V_I	Input voltage	A, B		−0.5∼+5.5	V
		DIR, $\overline{OC}$		−0.5∼+7	
V_O	Output voltage		High-level state or high-impedance state	−0.5∼+5.5	V
T_{opr}	Operating free-air ambient temperature range			−20∼+75	℃
T_{stg}	Storage temperature range			−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−15	mA
I_{OL}	Low-level output current	0		64	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
			V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
				I_{OH}=−15mA	2.4			
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=64mA				0.55	V
I_I	Input current at maximum voltage	DIR, $\overline{OC}$	V_{CC}=5.5V, V_I=7V				0.1	mA
		A, B	V_{CC}=5.5V, V_I=5.5V				0.1	
I_{IH}	High-level input current (Note 2)	DIR, $\overline{OC}$	V_{CC}=5.5V, V_I=2.7V				20	μA
		A, B					70	
I_{IL}	Low-level input current (Note 3)	DIR, $\overline{OC}$	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
		A, B					−0.75	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V		−50		−150	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.5V			37	58	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.5V			78	123	mA
I_{CCZ}	Supply current, all outputs disabled		V_{CC}=5.5V			51	80	mA

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 2. For A and B, I_{IH} includes off-state high-level output current I_{OZH}.

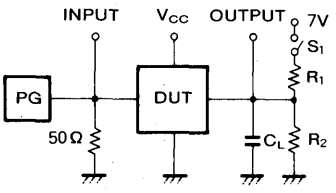
Note 3. For A and B, I_{IL} includes off-state low-level output current I_{OZL}.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Inputs	Outputs	Test conditions/Limits: V_{CC}=4.5~5.5V, C_L=50pF, R_1=500Ω, R_2=500Ω (Note 4)						Unit
				T_a=0~70℃			T_a=−20~+75℃			
				Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A, B	B, A	2		7	2		7.5	ns
t_{PHL}				2		6	2		6.5	
t_{PZH}	Output enable time	$\overline{OC}$	A, B	2		8	2		9	ns
t_{PZL}				2		10	2		11	
t_{PHZ}	Output disable time	$\overline{OC}$	A, B	2		8	2		9	ns
t_{PLZ}				2		13	2		14.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 4: Measurement circuit

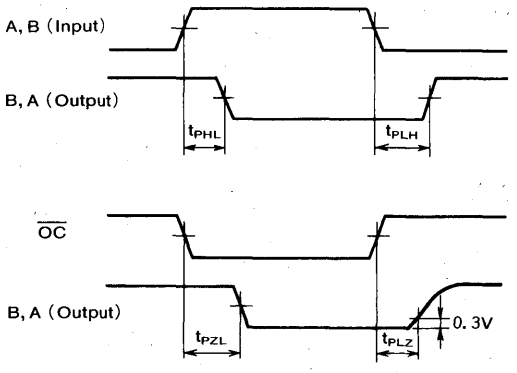


(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

TIMING DIAGRAM (Reference level=1.3V)



M74AS645P

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74AS645P is a semiconductor integrated circuit consisting of eight bus transmitter/receiver circuits with 3-state noninverted outputs.

FEATURES

- Two-way transmission or isolation between two 8-bit data
- High fan-out (I_{OL}=64mA, I_{OH}=−15mA)
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

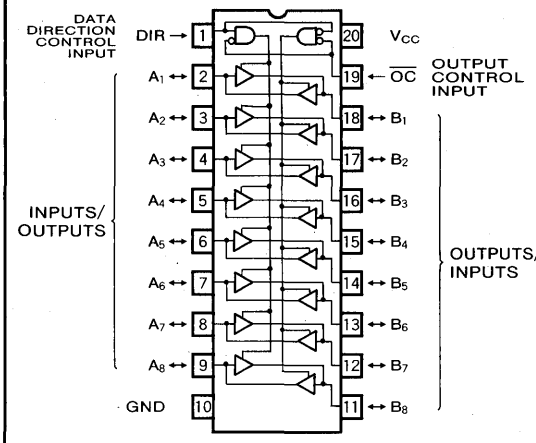
FUNCTIONAL DESCRIPTION

The inputs and outputs are mutually connected to form two-way buffers with 3-state noninverted outputs.

The input/output direction is controlled by DIR.

When DIR is high, pins A are made the input pins and pins B are made the output pins. When DIR is low, B are made the input pins and A are made the output pins. When $\overline{OC}$ is high, both A and B are in the high-impedance state and A and B are isolated.

PIN CONFIGURATION (TOP VIEW)



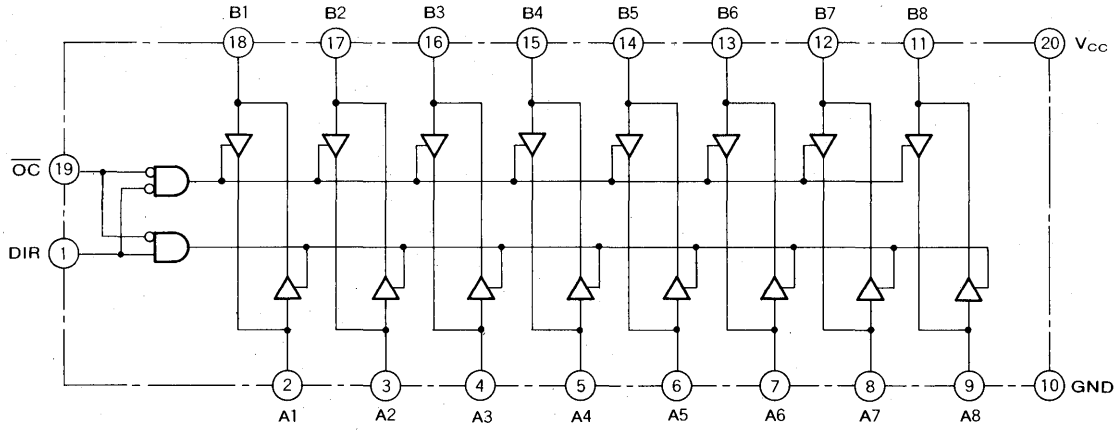
Outline 20P4

FUNCTION TABLE (Note 1)

Inputs		Input/Output	
$\overline{OC}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

Note 1: I : Input pins
O : Output pins (non-inverted output)
Z : High-impedance state (A and B are isolated)
X : Irrelevant

LOGIC DIAGRAM



OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5∼+7	V
V_I	Input voltage	A, B		−0.5∼+5.5	V
		DIR, $\overline{OC}$		−0.5∼+7	
V_O	Output voltage		High-level state or high-impedance state	−0.5∼+5.5	V
T_{opr}	Operating free-air ambient temperature range			−20∼+75	℃
T_{stg}	Storage temperature range			−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−15	mA
I_{OL}	Low-level output current	0		64	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
			V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
				I_{OH}=−15mA	2.4			
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=64mA				0.55	V
I_I	Input current at maximum voltage	DIR, $\overline{OC}$	V_{CC}=5.5V, V_I=7V				0.1	mA
		A, B	V_{CC}=5.5V, V_I=5.5V				0.1	
I_{IH}	High-level input current (Note 2)	DIR, $\overline{OC}$	V_{CC}=5.5V, V_I=2.7V				20	μA
		A, B					70	
I_{IL}	Low-level input current (Note 3)	DIR, $\overline{OC}$	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
		A, B					−0.75	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V		−50		−150	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.5V			62	97	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.5V			95	149	mA
I_{CCZ}	Supply current, all outputs disabled		V_{CC}=5.5V			79	123	mA

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 2. For A and B, I_{IH} includes off-state high-level output current I_{OZH}.

Note 3. For A and B, I_{IL} includes off-state low-level output current I_{OZL}.

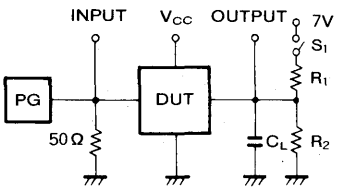
OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

SWITCHING CHARACTERISTICS

Symbol	Parameter	Inputs	Outputs	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 4), C_L=50pF, R_1=500Ω, R_2=500Ω; T_a=0~70℃ Min	Typ*	Max	T_a=−20~+75℃ Min	Typ*	Max	Unit
t_{PLH}	Propagation time	A, B	B, A	2		9.5	2		10.5	ns
t_{PHL}				2		9	2		10	
t_{PZH}	Output enable time	$\overline{OC}$	A, B	2		11	2		12	ns
t_{PZL}				2		10	2		11	
t_{PHZ}	Output disable time	$\overline{OC}$	A, B	2		7	2		8	ns
t_{PLZ}				2		12	2		13	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 4: Measurement circuit

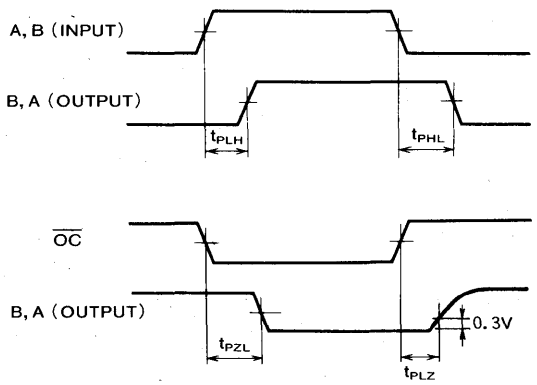


(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

Parameter	S_1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

TIMING DIAGRAM (reference level=1.3V)



M74AS756P

PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change.

OCTAL BUFFER/LINE DRIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

DESCRIPTION

The M74AS756P is a semiconductor integrated circuit consisting of two blocks of buffers with open collector inverted outputs and independent output control for each block.

FEATURES

- Open collector version of M74AS240P
- In-phase output control inputs ($1\overline{OC}$, $2\overline{OC}$)
- High fan-out (I_{OL}=64mA)
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATION

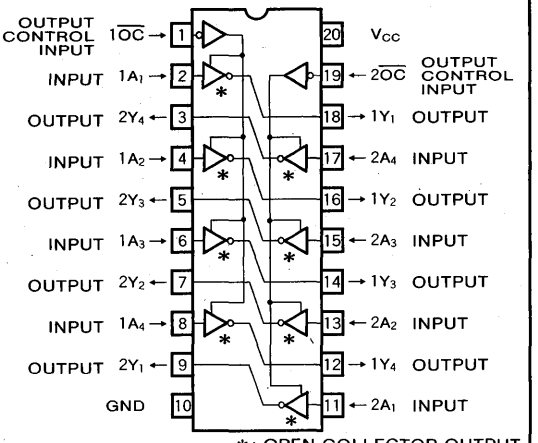
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

When output control input $\overline{OC}$ is low-level, and if input A is low, then output Y is high, if A is high, Y is low. When $\overline{OC}$ is high, Y_1∼Y_4 are high irrespective of the status of A.

The outputs of all eight buffers can be simultaneously controlled by connecting $1\overline{OC}$ and $2\overline{OC}$.

PIN CONFIGURATION (TOP VIEW)



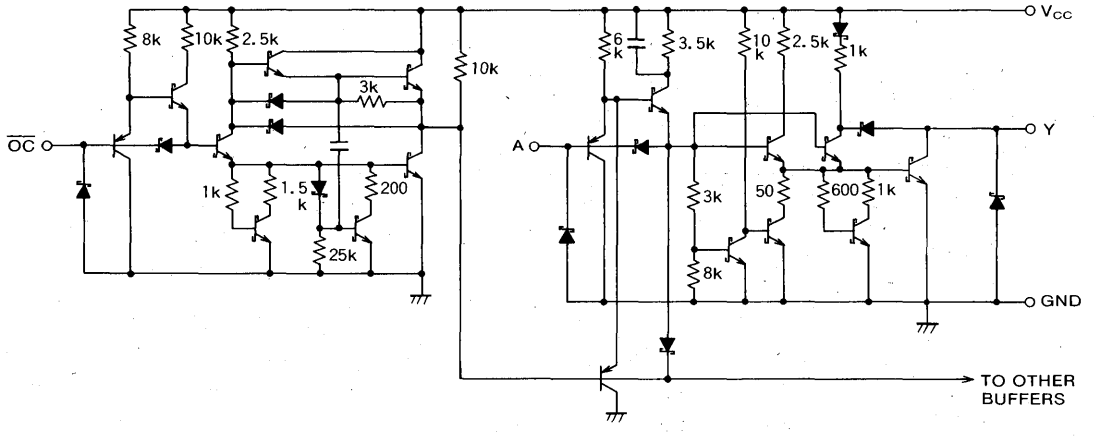
Outline 20P4

FUNCTION TABLE (Note 1)

Inputs		Output
A	$\overline{OC}$	Y
L	L	H
H	L	L
X	H	H

Note 1: X : Irrelevant

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

MITSUBISHI ELECTRIC

OCTAL BUFFER/LINE DRIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼+7	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage			5.5	V
I_{OL}	Low-level output current	0		64	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
I_{OH}	High-level output current	V_{CC}=4.5V, V_{OH}=5.5V			0.1	mA
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=64mA			0.55	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V			20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V		9	15	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V		51	80	mA

*: All typical values are at V_{CC}=5V, T_a=25℃.

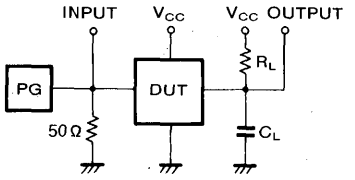
OCTAL BUFFER/LINE DRIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

SWITCHING CHARACTERISTICS

Symbol	Parameter	Input	Output	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 2), C_L=50pF, R_L=500Ω; T_a=0~70℃ Min	Typ*	Max	T_a=−20~+75℃ Min	Typ*	Max	Unit
t_{PLH}	Propagation time	A	Y	3		19	3		21	ns
t_{PHL}				1		6	1		6.5	
t_{PLH}		$\overline{OC}$	Y	3		19.5	3		21.5	ns
t_{PHL}				1		7.5	1		8	

*: All typical values are at V_{CC}=5V, T_a=25℃.

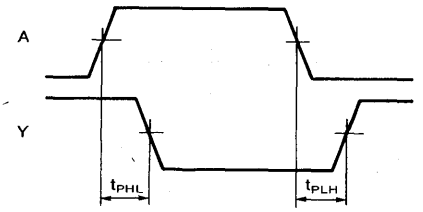
Note 2: Measurement circuit

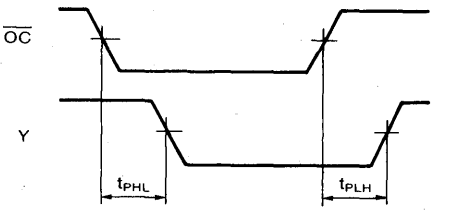


(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level=1.3V)





M74AS760P

OCTAL BUFFER/LINE DRIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

DESCRIPTION

The M74AS760P is a semiconductor integrated circuit consisting of two blocks of buffers with open collector noninverted outputs and independent output control for each block.

FEATURES

- Open collector version of M74AS244P
- In-phase output control inputs ($1\overline{OC}$, $2\overline{OC}$)
- High fan-out (I_{OL}=64mA)
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATION

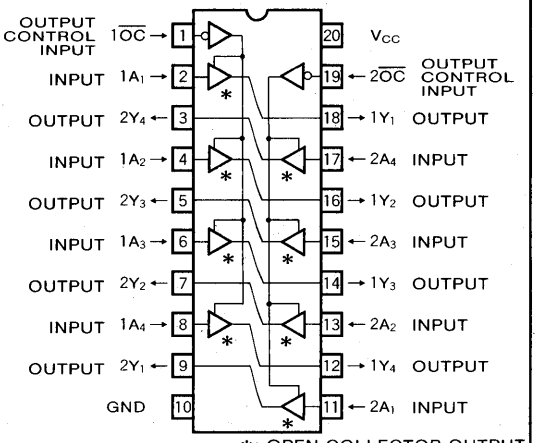
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

When output control input $\overline{OC}$ is low-level, and if input A is low, then output Y is low. If A is high, Y is high. When $\overline{OC}$ is high, Y_1∼Y_4 are high irrespective of the status of A.

The outputs of all eight buffers can be controlled simultaneously by connecting $1\overline{OC}$ and $2\overline{OC}$.

PIN CONFIGURATION (TOP VIEW)



*: OPEN COLLECTOR OUTPUT

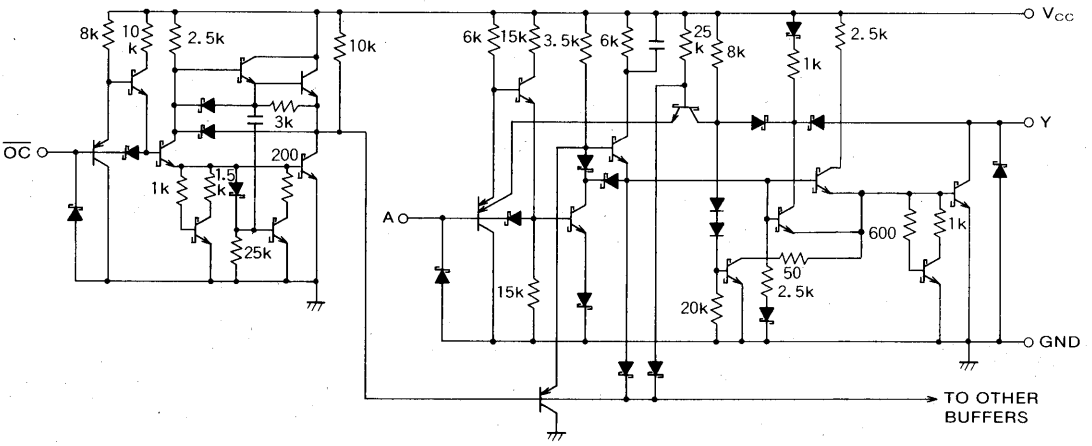
Outline 20P4

FUNCTION TABLE (Note 1)

Inputs		Output
A	$\overline{OC}$	Y
L	L	L
H	L	H
X	H	H

Note 1: X : Irrelevant

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

OCTAL BUFFER/LINE DRIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼+7	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage			5.5	V
I_{OL}	Low-level output current	0		64	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
I_{OH}	High-level output current		V_{CC}=4.5V, V_{OH}=5.5V			0.1	mA
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=64mA			0.55	V
I_I	Input current at maximum voltage		V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current		V_{CC}=5.5V, V_I=2.7V			20	μA
I_{IL}	Low-level input current	$\overline{OC}$	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
		A				−1	
I_{CCH}	Supply current, all outputs high		V_{CC}=5.5V		20	32	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.5V		60	94	mA

*: All typical values are at V_{CC}=5V, T_a=25℃.

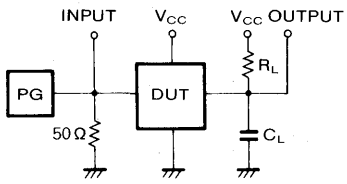
OCTAL BUFFER/LINE DRIVER WITH OPEN COLLECTOR OUTPUT (NONINVERTED)

SWITCHING CHARACTERISTICS

Symbol	Parameter	Input	Output	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 2), C_L=50pF, R_L=500Ω; T_a=0~70℃ Min	T_a=0~70℃ Typ*	T_a=0~70℃ Max	T_a=−20~+75℃ Min	T_a=−20~+75℃ Typ*	T_a=−20~+75℃ Max	Unit
t_{PLH}	Propagation time	A	Y	3		18.5	3		20	ns
t_{PHL}				1		6	1		6.5	
t_{PLH}		$\overline{OC}$	Y	3		18.5	3		20	ns
t_{PHL}				1		7	1		7.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

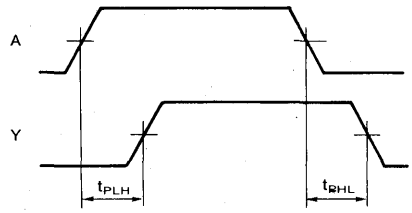
Note 2: Measurement circuit

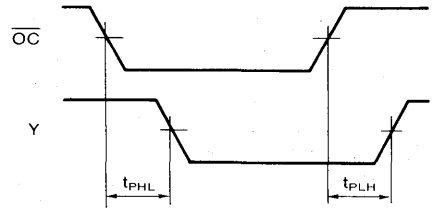


(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level=1.3V)





NEW PRODUCT

M74AS804BP

HEX 2-INPUT NAND DRIVER

DESCRIPTION

The M74AS804BP is a semiconductor integrated circuit consisting of six 2-input positive-logic NAND buffer gates, usable as negative-logic NOR buffer gates.

FEATURES

- High fan-out (I_{OL}=48mA, I_{OH}=−48mA)
- High speed
- Wide operating temperature range (T_a=−20~+75℃)
- High package density with six circuits in one package

APPLICATION

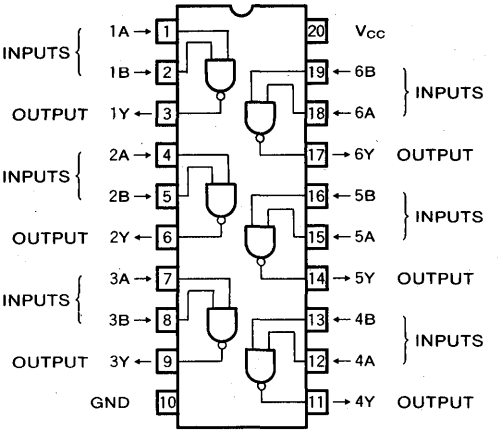
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74AS804BP achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit and clamp diodes (both input and output).

When both A and B inputs are high-level, output Y is low-level, and when at least one of the inputs is low, the output is high. This device has the same function as M74AS1804P with different pin connections.

PIN CONFIGURATION (TOP VIEW)

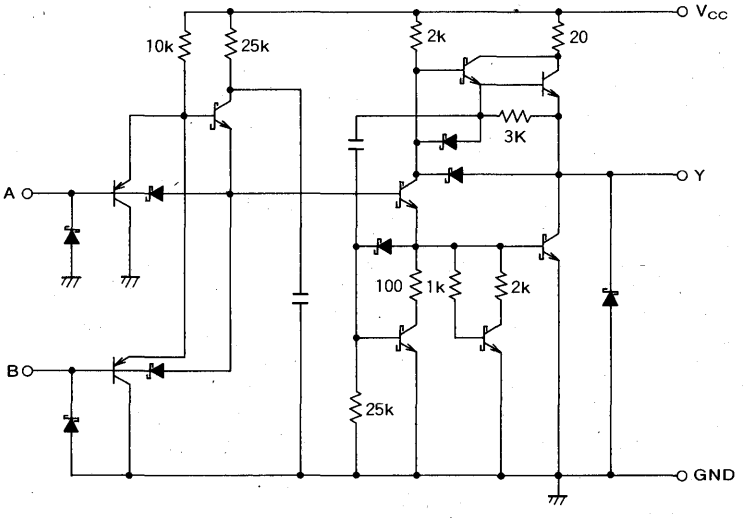


Outline 20P4

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−48	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
		V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
			I_{OH}=−48mA	2			
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=48mA				0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V		−50		−200	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=0V			3.5	5	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=4.5V			16	27	mA

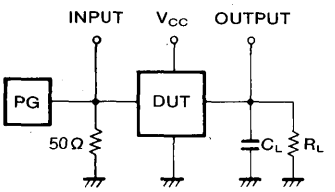
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

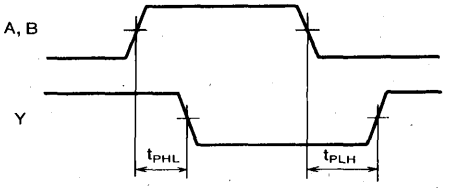
Symbol	Parameter			Test conditions/Limits: V_{CC}=4.5~5.5V (Note 1), C_L=50pF, R_L=500Ω						Unit
				T_a=0~70℃			T_a=−20~+75℃			
		Inputs	Output	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A, B	Y	1		4	1		4.5	ns
t_{PHL}				1		4	1		4.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 1: Measurement circuit



TIMING DIAGRAM (Reference level=1.3V)



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

M74AS808BP

HEX 2-INPUT AND DRIVER

DESCRIPTION

The M74AS808BP is a semiconductor integrated circuit consisting of six 2-input positive-logic AND buffer gates, usable as negative-logic OR buffer gates.

FEATURES

- High fan-out (I_{OL}=48mA, I_{OH}=−48mA)
- High speed
- Wide operating temperature range (T_a=−20~+75℃)
- High package density with six circuits in one package

APPLICATION

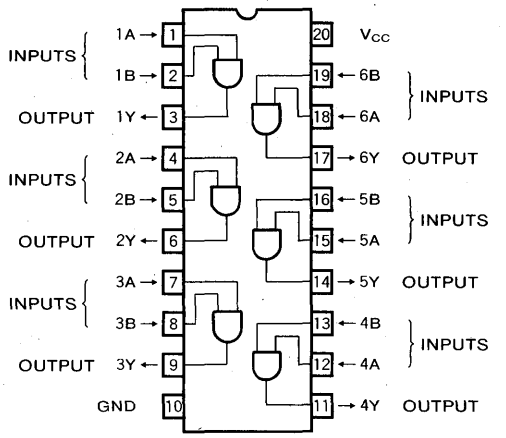
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pullup in the outputs, the M74AS808BP achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit and clamp diodes (both input and output).

When both A and B inputs are high-level, output Y is high-level, and when at least one of the inputs is low, the output is low. This device has the same function as M74AS1808P with different pin connections.

PIN CONFIGURATION (TOP VIEW)

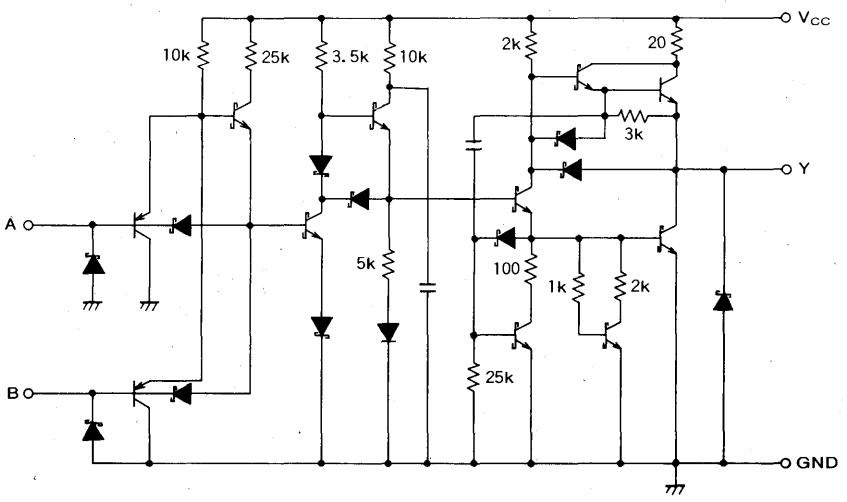


Outline 20P4

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−48	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
		V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
			I_{OH}=−48mA	2			
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=48mA				0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V		−50		−200	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=4.5V			9	13	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=0V			22	33	mA

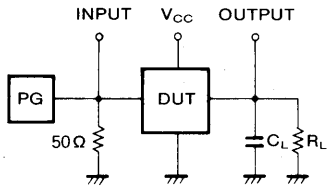
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

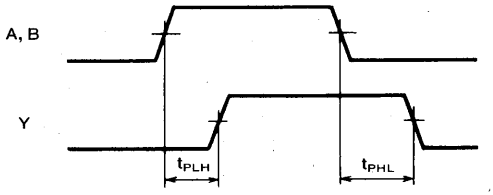
Symbol	Parameter	Inputs	Output	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 1), C_L=50pF, R_L=500Ω; T_a=0~70℃ Min	T_a=0~70℃ Typ*	T_a=0~70℃ Max	T_a=−20~+75℃ Min	T_a=−20~+75℃ Typ*	T_a=−20~+75℃ Max	Unit
t_{PLH}	Propagation time	A, B	Y	1		6	1		6.5	ns
t_{PHL}				1		6	1		6.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 1: Measurement circuit



TIMING DIAGRAM (Reference level=1.3V)



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M74AS832BP

HEX 2-INPUT OR DRIVER

DESCRIPTION

The M74AS832BP is a semiconductor integrated circuit consisting of six 2-input positive-logic OR buffer gates, usable as negative-logic AND buffer gates.

FEATURES

- High fan-out (I_{OL}=48mA, I_{OH}=−48mA)
- High speed
- Wide operating temperature range (T_a=−20~+75℃)
- High package density with six circuits in one package

APPLICATION

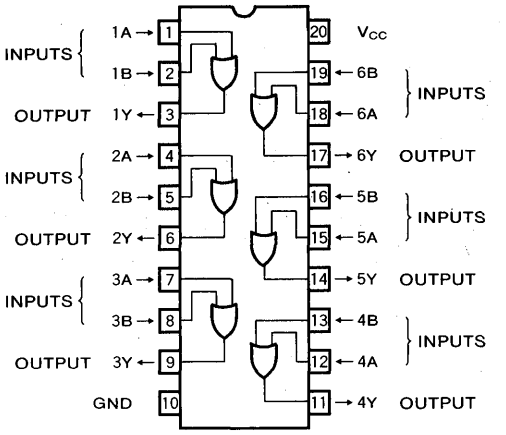
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pullup in the outputs, the M74AS832BP achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit and clamp diodes (both input and output).

When both A and B inputs are low-level, output Y is low-level, and when at least one of the inputs is high, the output is high. This device has the same function as M74AS1832P with different pin connections.

PIN CONFIGURATION (TOP VIEW)

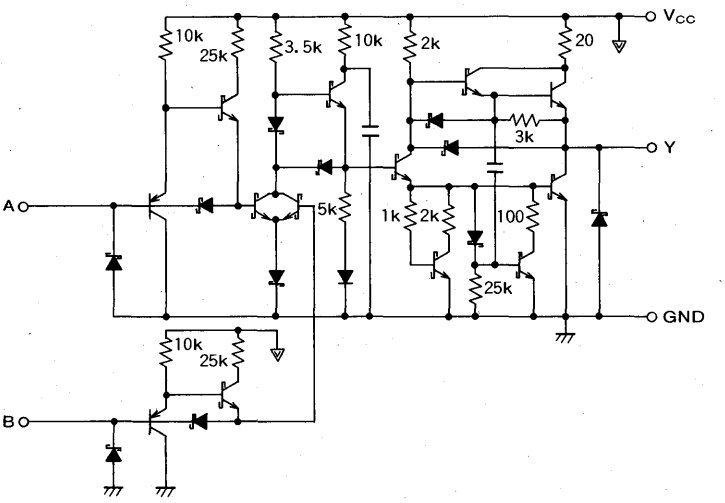


Outline 20P4

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−48	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
		V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
			I_{OH}=−48mA	2			
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=48mA				0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V		−50		−200	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=4.5V			11	17	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=0V			22	36	mA

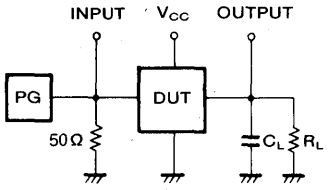
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

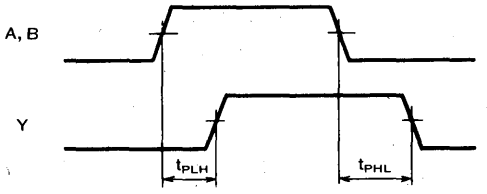
Symbol	Parameter	Inputs	Output	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 1), C_L=50pF, R_L=500Ω; T_a=0~70℃ Min	T_a=0~70℃ Typ*	T_a=0~70℃ Max	T_a=−20~+75℃ Min	T_a=−20~+75℃ Typ*	T_a=−20~+75℃ Max	Unit
t_{PLH}	Propagation time	A, B	Y	1		6.3	1		7	ns
t_{PHL}				1		6.3	1		7	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 1: Measurement circuit



TIMING DIAGRAM (Reference level=1.3V)



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

M74AS1000AP

QUADRUPLE 2-INPUT POSITIVE NAND DRIVER

DESCRIPTION

The M74AS1000AP is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND buffer gates, usable as negative-logic NOR buffer gates.

FEATURES

- High fan-out (I_{OL}=48mA, I_{OH}=−48mA)
- High speed
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATION

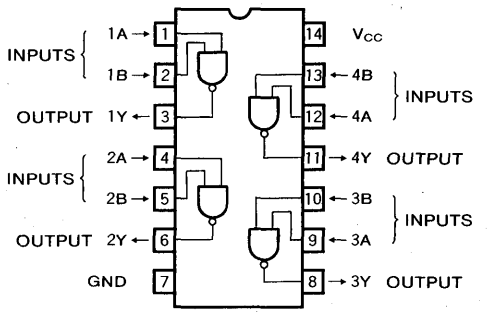
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74AS1000AP achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit and clamp diodes (both input and output).

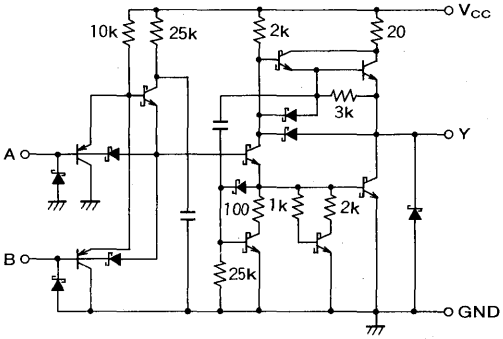
When both A and B inputs are high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−48	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
		V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
			I_{OH}=−48mA	2			
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=48mA				0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V		−50		−200	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=0V			2.3	3.5	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=4.5V			11	19	mA

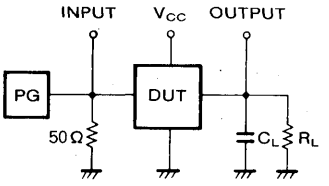
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

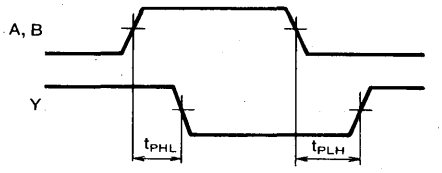
Symbol	Parameter			Test conditions/Limits						Unit
				V_{CC}=4.5∼5.5V (Note 1) C_L=50pF R_L=500Ω						
				T_a=0∼70℃			T_a=−20∼+75℃			
		Inputs	Output	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A, B	Y	1		4	1		4.5	ns
t_{PHL}				1		4	1		4.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 1: Measurement circuit



TIMING DIAGRAM (Reference level=1.3V)



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

PRELIMINARY
Notice This is not a final specification
Some parametric limits are subject to change.

M74AS1004AP

HEX INVERTING DRIVER

DESCRIPTION

The M74AS1004AP is a semiconductor integrated circuit consisting of six buffers with inverted outputs.

FEATURES

- High fan-out (I_{OL}=48mA, I_{OH}=−48mA)
- High speed
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATION

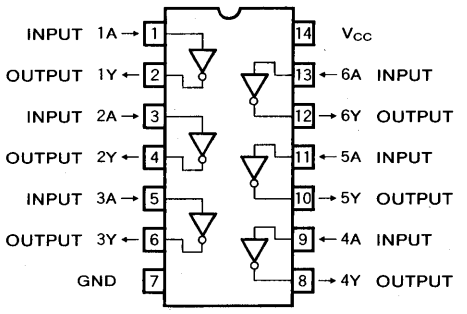
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74AS1004AP achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit and clamp diodes (both input and output).

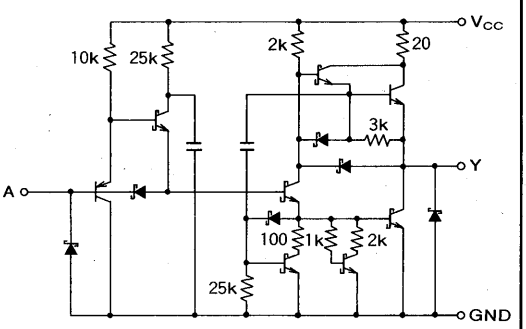
When input A is high-level, output Y is low-level, and when the input is low, the output is high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−48	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
		V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
			I_{OH}=−48mA	2			
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=48mA				0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V		−50		−200	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=0V			3.5	5	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=4.5V			16	27	mA

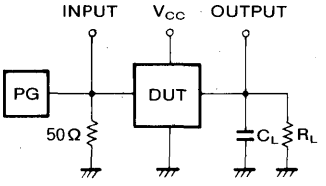
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter			Test conditions/Limits: V_{CC}=4.5∼5.5V, C_L=50pF, R_L=500Ω (Note 1)						Unit
				T_a=0∼70℃			T_a=−20∼+75℃			
		Input	Output	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A	Y	1		4	1		4.5	ns
t_{PHL}				1		4	1		4.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

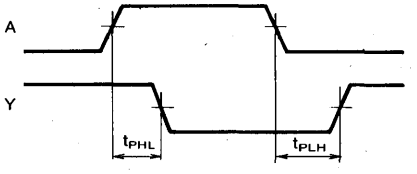
Note 1: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level=1.3V)



MITSUBISHI ELECTRIC

PRELIMINARY
Notice This is not a final specification
Some parametric limits are subject to change

M74AS1008AP

QUADRUPLE 2-INPUT POSITIVE AND DRIVER

DESCRIPTION

The M74AS1008AP is a semiconductor integrated circuit consisting of four 2-input positive-logic AND buffer gates, usable as negative-logic OR buffer gates.

FEATURES

- High fan-out (I_{OL}=48mA, I_{OH}=−48mA)
- High speed
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATION

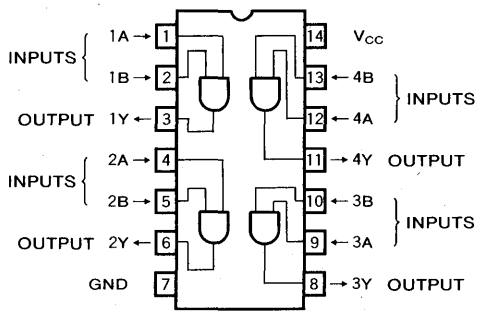
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74AS1008AP achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit and clamp diodes (both input and output).

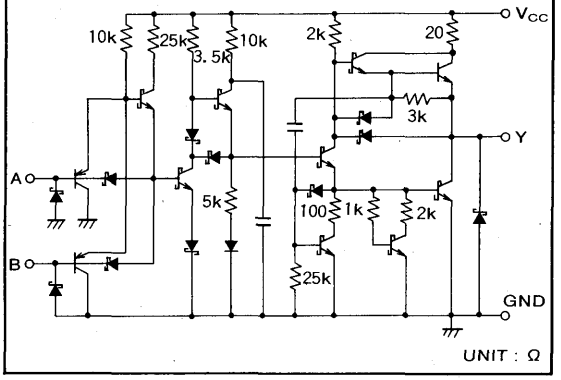
When both A and B inputs are high-level, output Y is high-level, and when at least one of the inputs is low, the output is low.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH BUFFER)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−48	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
		V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
			I_{OH}=−48mA	2			
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=48mA				0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V		−50		−200	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=4.5V			6	9.5	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=0V			14.5	22	mA

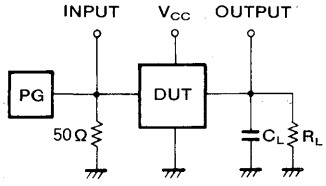
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter			Test conditions/Limits: V_{CC}=4.5∼5.5V (Note 1), C_L=50pF, R_L=500Ω						Unit
				T_a=0∼70℃			T_a=−20∼+75℃			
		Inputs	Output	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A, B	Y	1		6	1		6.5	ns
t_{PHL}				1		6	1		6.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

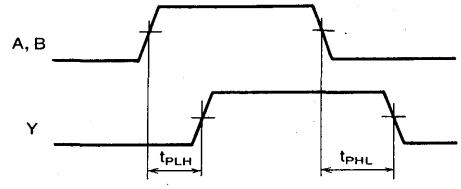
Note 1: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level=1.3V)



MITSUBISHI ELECTRIC

M74AS1034AP

HEX DRIVER

DESCRIPTION

The M74AS1034AP is a semiconductor integrated circuit consisting of six non-inverting drivers.

FEATURES

- High fan-out (I_{OL}=48mA, I_{OH}=−48mA)
- High speed
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATION

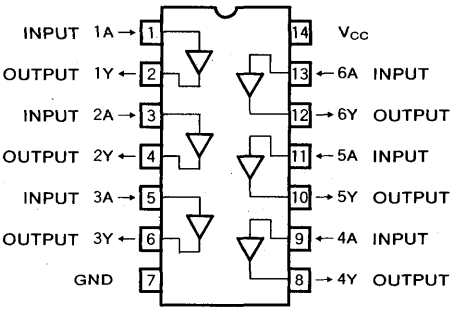
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pull-up in the outputs, the M74AS1034AP achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit and clamp diodes (both input and output).

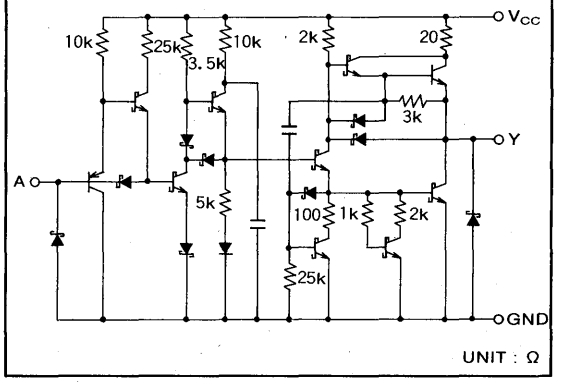
When input A is low-level, output Y is low-level, and when input A is high, output Y is high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

FUNCTION TABLE

Input	Output
A	Y
L	L
H	H

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−48	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
		V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
			I_{OH}=−48mA	2			
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=48mA				0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V		−50	−135	−200	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=4.5V			9	15	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=0V			22	35	mA

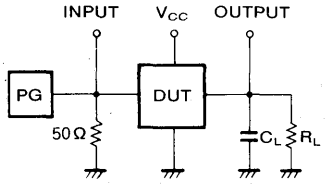
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter			Test conditions/Limits: V_{CC}=4.5∼5.5V (Note 1), C_L=50pF, R_L=500Ω						Unit
				T_a=0∼70℃			T_a=−20∼+75℃			
		Input	Output	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A	Y	1		6	1		6.5	ns
t_{PHL}				1		6	1		6.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

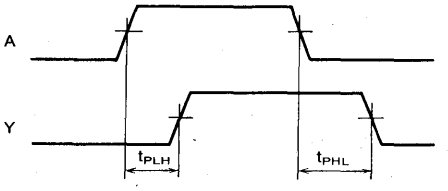
Note 1: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level=1.3V)



MITSUBISHI ELECTRIC

NEW PRODUCT

M74AS1804P

HEX 2-INPUT NAND DRIVER

DESCRIPTION

The M74AS1804P is a semiconductor integrated circuit consisting of six 2-input positive-logic NAND buffer gates, usable as negative-logic NOR buffer gates.

FEATURES

- High fan-out (I_{OL}=48mA, I_{OH}=−48mA)
- High speed
- Wide operating temperature range (T_a=−20~+75℃)
- High package density with six circuits in one package

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

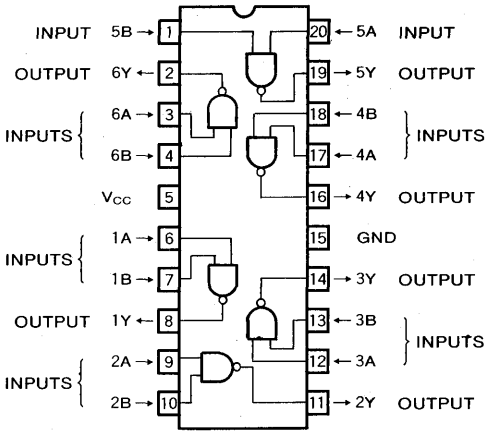
FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pullup in the outputs, the M74AS1804P achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit and clamp diodes (both input and output).

When both A and B inputs are high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

V_{CC} and GND pin connections of M74AS1804P are different from other ASTTL devices to minimize source pin inductances and troubles caused by them.

PIN CONFIGURATION (TOP VIEW)

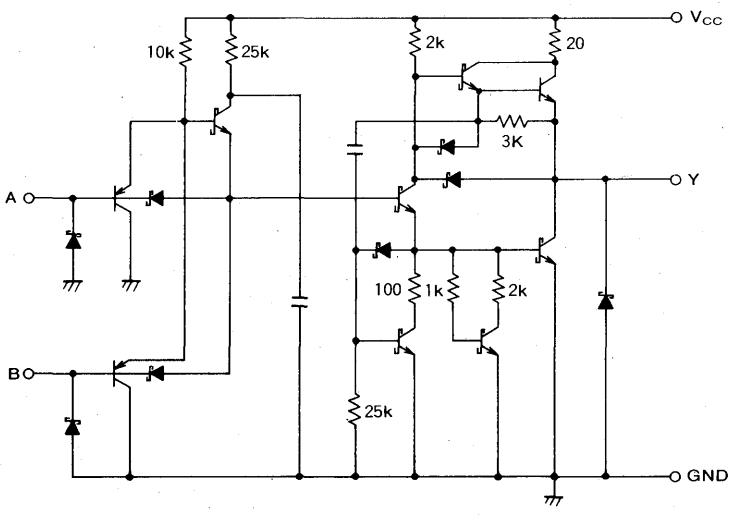


Outline 20P4

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−48	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
		V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
			I_{OH}=−48mA	2			
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=48mA				0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V		−50		−200	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=0V			3.5	5	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=4.5V			16	27	mA

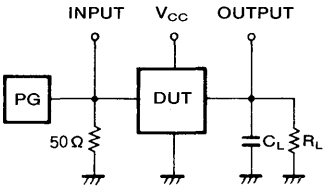
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

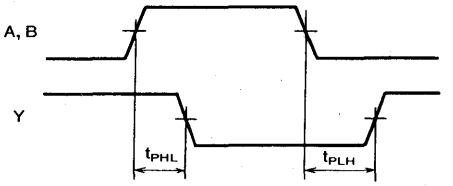
Symbol	Parameter	Inputs	Output	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 1), C_L=50pF, R_L=500Ω; T_a=0~70℃ Min	T_a=0~70℃ Typ*	T_a=0~70℃ Max	T_a=−20~+75℃ Min	T_a=−20~+75℃ Typ*	T_a=−20~+75℃ Max	Unit
t_{PLH}	Propagation time	A, B	Y	1		4	1		4.5	ns
t_{PHL}				1		4	1		4.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 1: Measurement circuit



TIMING DIAGRAM (Reference level=1.3V)



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

M74AS1808P

HEX 2-INPUT AND DRIVER

DESCRIPTION

The M74AS1808P is a semiconductor integrated circuit consisting of six 2-input positive-logic AND buffer gates, usable as negative-logic OR buffer gates.

FEATURES

- High fan-out (I_{OL}=48mA, I_{OH}=−48mA)
- High speed
- Wide operating temperature range (T_a=−20~+75℃)
- High package density with six circuits in one package

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

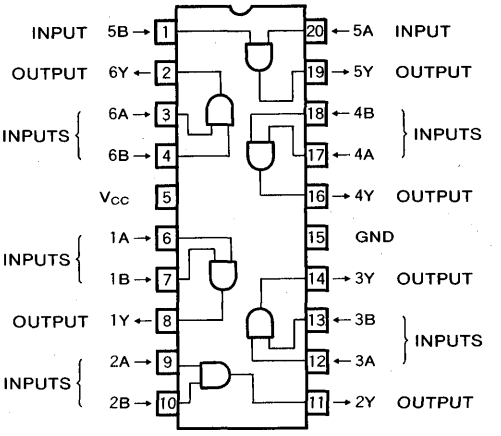
FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pullup in the outputs, the M74AS1808P achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit and clamp diodes (both input and output).

When both A and B inputs are high-level, output Y is high-level, and when at least one of the inputs is low, the output is low.

V_{CC} and GND pin connections of M74AS1808P are different from other ASTTL devices to minimize source pin inductances and troubles caused by them.

PIN CONFIGURATION (TOP VIEW)

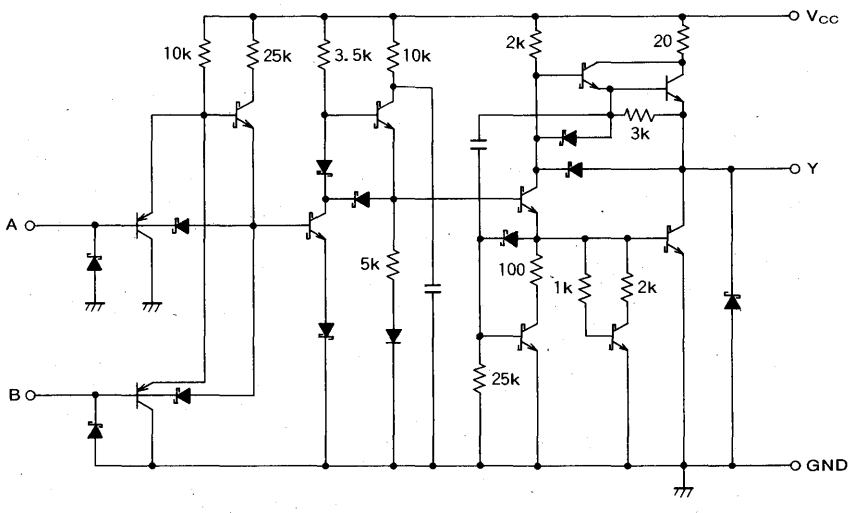


Outline 20P4

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−48	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
		V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
			I_{OH}=−48mA	2			
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=48mA				0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V		−50		−200	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=4.5V			9	13	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=0V			22	33	mA

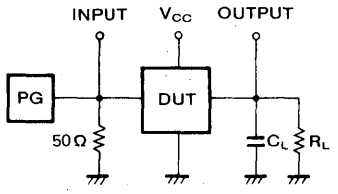
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

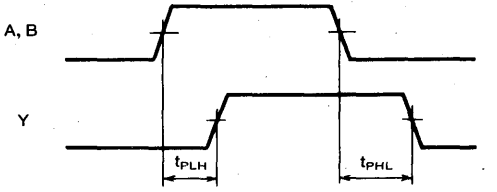
Symbol	Parameter			Test conditions/Limits: V_{CC}=4.5~5.5V (Note 1), C_L=50pF, R_L=500Ω						Unit
				T_a=0~70℃			T_a=−20~+75℃			
		Inputs	Output	Min	Typ*	Max	Min	Typ*	Max	
t_{PLH}	Propagation time	A, B	Y	1		6	1		6.5	ns
t_{PHL}				1		6	1		6.5	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 1: Measurement circuit



TIMING DIAGRAM (Reference level=1.3V)



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{iH}=3.5V, V_{iL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

M74AS1832P

HEX 2-INPUT OR DRIVER

DESCRIPTION

The M74AS1832P is a semiconductor integrated circuit consisting of six 2-input positive-logic OR buffer gates, usable as negative-logic AND buffer gates.

FEATURES

- High fan-out (I_{OL}=48mA, I_{OH}=−48mA)
- High speed
- Wide operating temperature range (T_a=−20~+75℃)
- High package density with six circuits in one package

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

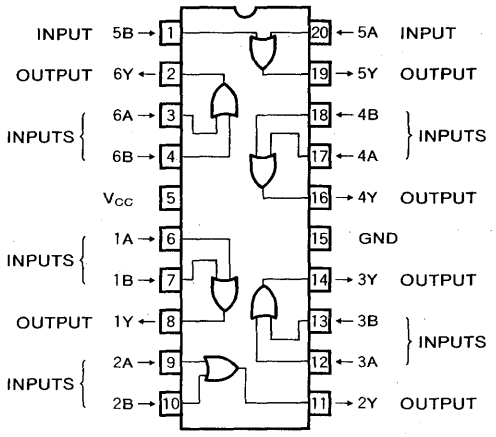
FUNCTIONAL DESCRIPTION

Employing PNP transistors in the inputs and active pullup in the outputs, the M74AS1832P achieves high speed and high fan-out. To reduce problems in high-speed switching, it has Miller-killer circuit and clamp diodes (both input and output).

When both A and B inputs are low-level, output Y is low-level, and when at least one of the inputs is high, the output is high.

V_{CC} and GND pin connections of M74AS1832P are different from other ASTTL devices to minimize source pin inductances and troubles caused by them.

PIN CONFIGURATION (TOP VIEW)

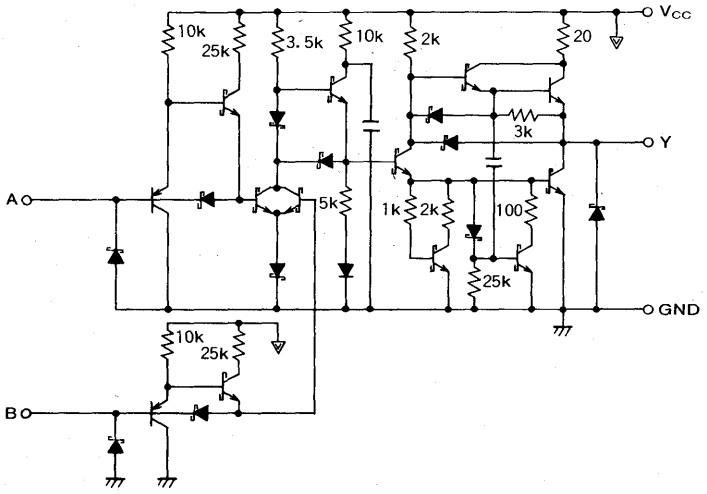


Outline 20P4

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−48	mA
I_{OL}	Low-level output current	0		48	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5V∼5.5V, I_{OH}=−2mA		V_{CC}−2			V
		V_{CC}=4.5V	I_{OH}=−3mA	2.4	3.2		
			I_{OH}=−48mA	2			
V_{OL}	Low-level output voltage	V_{CC}=4.5V, I_{OL}=48mA				0.5	V
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V				−0.5	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V		−50		−200	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.5V, V_I=4.5V			11	17	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.5V, V_I=0V			22	36	mA

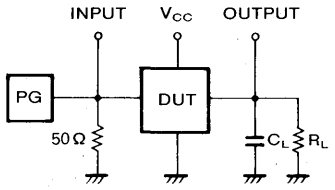
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Inputs	Output	Test conditions/Limits: V_{CC}=4.5~5.5V (Note 1), C_L=50pF, R_L=500Ω; T_a=0~70℃ Min	Typ*	Max	T_a=−20~+75℃ Min	Typ*	Max	Unit
t_{PLH}	Propagation time	A, B	Y	1		6.3	1		7	ns
t_{PHL}				1		6.3	1		7	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 1: Measurement circuit



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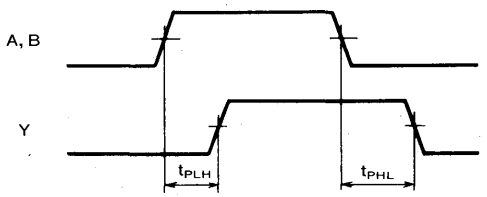
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level=1.3V)



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