MITSUBISHI SEMICONDUCTORS 1987

HIGH SPEED CMOS LOGIC

DATA BOOK

MITSUBISHI ELECTRIC

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1 GUIDANCE

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Note : M74HC266 is equivalent with 74HC7266 which other venders supply.
M74HC266A has an open-drain output and corresponds to the 74LS266.
M74HC266A is equivalent with other vender's 74HC266.

GUIDANCE 1

INDEX BY FUNCTION

INDEX BY FUNCTION (★★ : under development)

Conditions (Rated at V_{CC}=4.5V and T_a=−40∼+85℃, Switching specifications apply at C_L=50pF)

INVERTERS

Type	Description	Electrical characteristics				Outline	Page
		High-level output current (mA)	Low-level output current (mA)	Low-level to high-level output propagation time (ns)	High-level to low-level output propagation time (ns)		
M74HCU04P	Hex Unbuffered Inverter	−4	4	21	21	14P4	2−18
M74HCU04FP						14P2N	
M74HCU04DP						14P2P	
M74HC04P	Hex Inverter	−4	4	24	24	14P4	2−15
M74HC04FP						14P2N	
M74HC04DP						14P2P	
M74HCT04P ★★	Hex Inverter with LSTTL-Compatible Inputs	−4	4	24	24	14P4	2−21
M74HCT04FP ★★						14P2N	
M74HCT04DP ★★						14P2P	
M74HC05P	Hex Inverter with Open-Drain Outputs	—	4	29	21	14P4	2−24
M74HC05FP						14P2N	
M74HC05DP						14P2P	

NAND GATES

M74HC00P	Quadruple 2-Input Positive NAND Gate	−4	4	23	23	14P4	2− 3
M74HC00FP						14P2N	
M74HC00DP						14P2P	
M74HCT00P	Quadruple 2-Input Positive NAND Gate with LSTTL-Compatible Inputs	−4	4	24	24	14P4	2− 6
M74HCT00FP						14P2N	
M74HCT00DP						14P2P	
M74HC03P	Quadruple 2-Input Positive NAND Gate with Open-Drain Outputs	—	4	32	32	14P4	2− 12
M74HC03FP						14P2N	
M74HC03DP						14P2P	
M74HC10P	Triple 3-Input Positive NAND Gate	−4	4	24	24	14P4	2− 33
M74HC10FP						14P2N	
M74HC10DP						14P2P	
M74HC20P	Dual 4-Input Positive NAND Gate	−4	4	23	23	14P4	2− 42
M74HC20FP						14P2N	
M74HC20DP						14P2P	
M74HC30P	8-Input Positive NAND Gate	−4	4	42	42	14P4	2− 49
M74HC30FP						14P2N	
M74HC30DP						14P2P	
M74HC133P	13-Input Positive NAND Gate	−4	4	42	42	16P4	2−131
M74HC133FP						16P2N	
M74HC133DP						16P2P	

AND GATES

M74HC08P	Quadruple 2-Input Positive AND Gate	−4	4	30	30	14P4	2−27
M74HC08FP						14P2N	
M74HC08DP						14P2P	
M74HC09P	Quadruple 2-Input Positive AND Gate with Open-Drain Outputs	—	4	31	25	14P4	2−30
M74HC09FP						14P2N	
M74HC09DP						14P2P	
M74HC11P	Triple 3-Input Positive AND Gate	−4	4	31	31	14P4	2−36
M74HC11FP						14P2N	
M74HC11DP						14P2P	
M74HC21P ★★	Dual 4-Input Positive AND Gate	−4	4	26	26	14P4	2−45
M74HC21FP ★★						14P2N	
M74HC21DP ★★						14P2P	

INDEX BY FUNCTION

NOR GATES

Type	Description	Electrical characteristics				Outline	Page
		High-level output current (mA)	Low-level output current (mA)	Low-level to high-level output propagation time (ns)	High-level to low-level output propagation time (ns)		
M74HC02P	Quadruple 2-Input Positive NOR Gate	−4	4	23	23	14P4	2 — 9
M74HC02FP						14P2N	
M74HC02DP						14P2P	
M74HC27P	Triple 3-Input Positive NOR Gate	−4	4	23	23	14P4	2 — 46
M74HC27FP						14P2N	
M74HC27DP						14P2P	
M74HC4002P	Dual 4-Input Positive NOR Gate	−4	4	30	30	14P4	2 —586
M74HC4002FP						14P2N	
M74HC4002DP						14P2P	
M74HC4078P	8-Input Positive NOR/OR Gate	−4	4	33	33	14P4	2 —643
M74HC4078FP						14P2N	
M74HC4078DP						14P2P	

OR GATES

M74HC32P	Quadruple 2-Input Positive OR Gate	−4	4	25	25	14P4	2 — 52
M74HC32FP						14P2N	
M74HC32DP						14P2P	
M74HC4075P	Triple 3-Input OR Gate	−4	4	29	29	14P4	2 —640
M74HC4075FP						14P2N	
M74HC4075DP						14P2P	
M74HC4078P	8-Input Positive NOR/OR Gate	−4	4	33	33	14P4	2 —643
M74HC4078FP						14P2N	
M74HC4078DP						14P2P	

EXCLUSIVE OR GATES

M74HC86P	Quadruple 2-Input Exclusive OR Gate	−4	4	30	30	14P4	2 —86
M74HC86FP						14P2N	
M74HC86DP						14P2P	

EXCLUSIVE NOR GATES

M74HC266P	Quadruple 2-Input Exclusive NOR Gate	−4	4	30	30	14P4	2 —365
M74HC266FP						14P2N	
M74HC266DP						14P2P	
M74HC266AP	Quadruple 2-Input Exclusive NOR Gate with Open-Drain Outputs	—	4	31	25	14P4	2 —368
M74HC266AFP						14P2N	
M74HC266ADP						14P2P	

AND-OR-INVERTER GATES

M74HC51P	2-Wide, 2-Input/2-Wide, 3-Input AND-OR-INVERT Gates	−4	4	32	32	14P4	2 —59
M74HC51FP						14P2N	
M74HC51DP						14P2P	

INDEX BY FUNCTION

BUFFERS/LINE DRIVERS

Type	Description	Output		Electrical characteristics				Outline	Page
		Two-state	Three-state	High-level output current (mA)	Low-level output current (mA)	Low-level to high-level output propagation time (ns)	High-level to low-level output propagation time (ns)		
M74HC125P	Quadruple 3-State Noninverting Buffer		NI	−6	6	25	25	14P4	2 −120
M74HC125FP								14P2N	
M74HC125DP								14P2P	
M74HC126P	Quadruple 3-State Noninverting Buffer		NI	−6	6	25	25	14P4	2 −124
M74HC126FP								14P2N	
M74HC126DP								14P2P	
M74HC240P	Octal 3-State Inverting Buffer/Line Driver /Line Receiver		I	−6	6	25	25	20P4	2 −273
M74HC240FP								20P2N	
M74HC240DWP								20P2V	
M74HC240-1P	Octal 3-State Inverting Buffer/Line Driver /Line Receiver		I	−24	24	19	19	20P4	2 −277
M74HC240-1FP								20P2N	
M74HC240-1DWP								20P2V	
M74HCT240P	Octal 3-State Inverting Buffer/Line Driver /Line Receiver with LSTTL-Compatible Inputs		I	−6	6	29	29	20P4	2 −281
M74HCT240FP								20P2N	
M74HCT240DWP								20P2V	
M74HCT240-1P ★★	Octal 3-State Inverting Buffer/Line Driver /Line Receiver with LSTTL-Compatible Inputs		I	−24	24	19	19	20P4	2 −285
M74HCT240-1FP ★★								20P2N	
M74HCT240-1DWP ★★								20P2V	
M74HC241P	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver		NI	−6	6	29	29	20P4	2 −289
M74HC241FP								20P2N	
M74HC241DWP								20P2V	
M74HC241-1P	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver		NI	−24	24	23	23	20P4	2 −293
M74HC241-1FP								20P2N	
M74HC241-1DWP								20P2V	
M74HCT241P	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver with LSTTL-Compatible Inputs		NI	−6	6	32	32	20P4	2 −297
M74HCT241FP								20P2N	
M74HCT241DWP								20P2V	
M74HCT241-1P ★★	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver with LSTTL-Compatible Inputs		NI	−24	24	23	23	20P4	2 −301
M74HCT241-1FP ★★								20P2N	
M74HCT241-1DWP ★★								20P2V	
M74HC244P	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver		NI	−6	6	29	29	20P4	2 −313
M74HC244FP								20P2N	
M74HC244DWP								20P2V	
M74HC244-1P	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver		NI	−24	24	23	23	20P4	2 −317
M74HC244-1FP								20P2N	
M74HC244-1DWP								20P2V	
M74HCT244P	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver with LSTTL-Compatible Inputs		NI	−6	6	32	32	20P4	2 −321
M74HCT244FP								20P2N	
M74HCT244DWP								20P2V	
M74HCT244-1P ★★	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver with LSTTL-Compatible Inputs		NI	−24	24	23	23	20P4	2 −325
M74HCT244-1FP ★★								20P2N	
M74HCT244-1DWP ★★								20P2V	
M74HC365P	Hex 3-State Noninverting Buffer with Common Enables		NI	−6	6	30	30	16P4	2 −404
M74HC365FP								16P2N	
M74HC365DP								16P2P	
M74HC366P	Hex 3-State Inverter Buffer with Common Enables		I	−6	6	24	24	16P4	2 −408
M74HC366FP								16P2N	
M74HC366DP								16P2P	
M74HC367P	Hex 3-State Noninverting Buffer with Separate 2-Bit and 4-Bit Sections		NI	−6	6	30	30	16P4	2 −412
M74HC367FP								16P2N	
M74HC367DP								16P2P	
M74HC368P	Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections		I	−6	6	24	24	16P4	2 −416
M74HC368FP								16P2N	
M74HC368DP								16P2P	

BUFFERS/LINE DRIVERS (continued)

Type	Description	Output		Electrical characteristics				Outline	Page
		Two-state	Three-state	High-level output current (mA)	Low-level output current (mA)	Low-level to high-level output propagation time (ns)	High-level to low-level output propagation time (ns)		
M74HC540P	Octal 3-State Inverting Buffer/Line Driver /Line Receiver		I	−6	6	25	25	20P4	2 −490
M74HC540FP								20P2N	
M74HC540DWP								20P2V	
M74HC541P	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver		NI	−6	6	29	29	20P4	2 −494
M74HC541FP								20P2N	
M74HC541DWP								20P2V	
M74HC4049BP	Hex Inverting Buffer/Logic-Level Down Converter	I		−6	6	20	19	16P4	2 −613
M74HC4049BFP								16P2N	
M74HC4049BDP								16P2P	
M74HC4050BP	Hex Noninverting Buffer/Logic-Level Down Converter	NI		−6	6	20	19	16P4	2 −616
M74HC4050BFP								16P2N	
M74HC4050BDP								16P2P	

I : Inverting output NI : Noninverting output

BUS TRANSCEIVERS

M74HC242P	Quadruple 3-State Inverting Bus Transceiver		I	−6	6	25	25	14P4	2 −305
M74HC242FP								14P2N	
M74HC242DP								14P2P	
M74HC243P	Quadruple 3-State Noninverting Bus Transceiver		NI	−6	6	25	25	14P4	2 −309
M74HC243FP								14P2N	
M74HC243DP								14P2P	
M74HC245P	Octal 3-State Noninverting Bus Transceiver		NI	−6	6	28	28	20P4	2 −329
M74HC245FP								20P2N	
M74HC245DWP								20P2V	
M74HC245-1P ★★	Octal 3-State Noninverting Bus Transceiver		NI	−24	24	21	21	20P4	2 −333
M74HC245-1FP ★★								20P2N	
M74HC245-1DWP ★★								20P2V	
M74HCT245-1P ★★	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs		NI	−24	24	21	21	20P4	2 −337
M74HCT245-1FP ★★								20P2N	
M74HCT245-1DWP ★★								20P2V	
M74HC640P	Octal 3-State Inverting Bus Transceiver		I	−6	6	28	28	20P4	2 −529
M74HC640FP								20P2N	
M74HC640DWP								20P2V	
M74HC640-1P ★★	Octal 3-State Inverting Bus Transceiver		I	−24	24	21	21	20P4	2 −533
M74HC640-1FP ★★								20P2N	
M74HC640-1DWP ★★								20P2V	
M74HCT640P-1 ★★	Octal 3-State Inverting Bus Transceiver with LSTTL-Compatible Inputs		I	−24	24	21	21	20P4	2 −537
M74HCT640-1FP ★★								20P2N	
M74HCT640-1DWP ★★								20P2V	
M74HC643P	Octal 3-State Inverting and Noninverting Bus Transceiver		NI, I	−6	6	28	28	20P4	2 −541
M74HC643FP								20P2N	
M74HC643DWP								20P2V	
M74HC643-1P ★★	Octal 3-State Inverting and Noninverting Bus Transceiver		NI, I	−24	24	21	21	20P4	2 −545
M74HC643-1FP ★★								20P2N	
M74HC643-1DWP ★★								20P2V	
M74HCT643-1P ★★	Octal 3-State Inverting and Noninverting Bus Transceiver with LSTTL-Compatible Inputs		NI,I	−24	24	21	21	20P4	2 −549
M74HCT643-1FP ★★								20P2N	
M74HCT643-1DWP ★★								20P2V	
M74HC645P	Octal 3-State Noninverting Bus Transceiver		NI	−6	6	28	28	20P4	2 −553
M74HC645FP								20P2N	
M74HC645DWP								20P2V	

BUFFERS/LINE DRIVERS (continued)

Type	Description	Output		Electrical characteristics				Outline	Page
		Two-state	Three-state	High-level output current (mA)	Low-level output current (mA)	Low-level to high-level output propagation time (ns)	High-level to low-level output propagation time (ns)		
M74HC645-1P ★★	Octal 3-State Noninverting Bus Transceiver		NI	−24	24	21	21	20P4	2 −557
M74HC645-1FP ★★								20P2N	
M74HC645-1DWP★★								20P2V	
M74HCT645-1P ★★	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs		NI	−24	24	21	21	20P4	2 −561
M74HCT645-1FP ★★								20P2N	
M74HCT645-1DWP ★★								20P2V	
M74HC646P ★★	Octal 3-State Noninverting Bus Transceiver and D-Type Flip-Flop		NI	−6	6	43	43	24P4D	2 −565
M74HC646FP ★★								24P2	
M74HC646DWP ★★								24P2V	
M74HC648P ★★	Octal 3-State Inverting Bus Transceiver and D-Type Flip-Flop		I	−6	6	43	43	24P4D	2 −572
M74HC648FP ★★								24P2	
M74HC648DWP ★★								24P2V	

I : Inverting output NI : Noninverting output

SCHMITT TRIGGERS

Type	Description	Electrical characteristics				Outline	Page
		Positive-going threshold voltage (V)	Negative-going threshold voltage (V)	Low-level to high-level output propagation time (ns)	High-level to low-level output propagation time (ns)		
M74HC14P	Hex Schmitt-Trigger Inverter	1.55~3.15	0.9~2.45	31	31	14P4	2 − 39
M74HC14FP						14P2N	
M74HC14DP						14P2P	
M74HC132P	Quadruple 2-Input Schmitt-Trigger Positive NAND Gate	1.55~3.15	0.9~2.45	32	32	14P4	2 −128
M74HC132FP						14P2N	
M74HC132DP						14P2P	

J-K FLIP FLOPS

Type	Description	Electrical characteristics			Trigger	Set	Reset	Outline	Page
		Operating frequency (MHz)	Setup time (ns)	Hold time (ns)					
M74HC73P	Dual J-K Flip-Flop with Reset	21	25	0	↓	—	⊔	14P4	2 − 62
M74HC73FP								14P2N	
M74HC73DP								14P2P	
M74HC76P	Dual J-K Flip-Flop with Set and Reset	21	25	0	↓	⊔	⊔	16P4	2 − 76
M74HC76FP								16P2N	
M74HC76DP								16P2P	
M74HC107P	Dual J-K Flip-Flop with Reset	21	25	0	↓	—	⊔	14P4	2 − 89
M74HC107FP								14P2N	
M74HC107DP								14P2P	
M74HC109P	Dual J-$\overline{K}$ Flip-Flop with Set and Reset	21	25	5	↑	⊔	⊔	16P4	2 − 94
M74HC109FP								16P2N	
M74HC109DP								16P2P	
M74HC112P	Dual J-K Flip-Flop with Set and Reset	21	25	0	↓	⊔	⊔	16P4	2 − 99
M74HC112FP								16P2N	
M74HC112DP								16P2P	
M74HC113P	Dual J-K Flip-Flop with Set	21	25	0	↓	⊔	—	14P4	2 −104
M74HC113FP								14P2N	
M74HC113DP								14P2P	
M74HC114P	Dual J-K Flip-Flop with Set and Common Reset	21	25	0	↓	⊔	⊔	14P4	2 −109
M74HC114FP								14P2N	
M74HC114DP								14P2P	

↑ : Positive-going edge ↓ : Negative-going edge ⊔ : Active low

D-TYPE FLIP FLOPS

Type	Description	Electrical characteristics			Trigger	Set	Reset	Outline	Page
		Operating frequency (MHz)	Setup time (ns)	Hold time (ns)					
M74HC74P	Dual D-Type Flip-Flop with Set and Reset	21	25	0	↑	⊔	⊓	14P4	2 — 67
M74HC74FP								14P2N	
M74HC74DP								14P2P	
M74HC173P	Quadruple 3-State D-Type Flip-Flop with Common Clock and Reset	21	25	0	↑	—	⊓	16P4	2 —225
M74HC173FP								16P2N	
M74HC173DP								16P2P	
M74HC174P	Hex D-Type Flip-Flop with Common Clock and Reset	21	25	5	↑	—	⊔	16P4	2 —230
M74HC174FP								16P2N	
M74HC174DP								16P2P	
M74HC175P	Quadruple D-Type Flip-Flop with Common Clock and Reset	24	25	5	↑	—	⊔	16P4	2 —234
M74HC175FP								16P2N	
M74HC175DP								16P2P	
M74HC273P	Octal D-Type Flip-Flop with Common Clock and Reset	21	25	0	↑	—	⊔	20P4	2 —371
M74HC273FP								20P2N	
M74HC273DWP								20P2V	
M74HC374P	Octal 3-State Noninverting D-Type Flip-Flop	24	18	12	↑	—	—	20P4	2 —433
M74HC374FP								20P2N	
M74HC374DWP								20P2V	
M74HC374-1P ★★	Octal 3-State Noninverting D-Type Flip-Flop	26	13	6	↑	—	—	20P4	2 —438
M74HC374-1FP ★★								20P2N	
M74HC374-1DWP ★★								20P2V	
M74HCT374-1P ★★	Octal 3-State Noninverting D-Type Flip-Flop with LSTTL-Compatible Inputs	26	13	6	↑	—	—	20P4	2 —443
M74HCT374-1FP ★★								20P2N	
M74HCT374-1DWP ★★								20P2V	
M74HC377P ★★	Octal D-Type Flip-Flop with Common Clock and Enable	—	—	—	↑	—	—	20P4	2 —451
M74HC377FP ★★								20P2N	
M74HC377DWP ★★								20P2V	
M74HC534P	Octal 3-State Inverting D-Type Flip-Flop	24	18	12	↑	—	—	20P4	2 —476
M74HC534FP								20P2N	
M74HC534DWP								20P2V	
M74HC534-1P ★★	Octal 3-State Inverting D-Type Flip-Flop	26	13	6	↑	—	—	20P4	2 —481
M74HC534-1FP ★★								20P2N	
M74HC534-1DWP ★★								20P2V	
M74HCT534-1P ★★	Octal 3-State Inverting D-Type Flip-Flop with LSTTL-Compatible Inputs	26	13	6	↑	—	—	20P4	2 —486
M74HCT534-1FP ★★								20P2N	
M74HCT534-1DWP ★★								20P2V	
M74HC564P ★★	Octal 3-State Inverting D-Type Flip-Flop	24	25	0	↑	—	—	20P4	2 —503
M74HC564FP ★★								20P2N	
M74HC564DWP ★★								20P2V	
M74HC574P ★★	Octal 3-State Noninverting D-Type Flip-Flop	24	25	0	↑	—	—	20P4	2 —512
M74HC574FP ★★								20P2N	
M74HC574DWP ★★								20P2V	
M74HC646P ★★	Octal 3-State Noninverting Bus Transceiver and D-Type Flip-Flop	21	25	0	↑	—	—	24P4D	2 —565
M74HC646FP ★★								24P2	
M74HC646DWP ★★								24P2V	
M74HC648P ★★	Octal 3-State Inverting Bus Transceiver and D-Type Flip-Flop	21	25	0	↑	—	—	24P4D	2 —572
M74HC648FP ★★								24P2	
M74HC648DWP ★★								24P2V	

↑ : Positive-going edge ⊔ : Active low

INDEX BY FUNCTION

SYNCHRONOUS BINARY COUNTERS

Type	Description	Electrical characteristics: Count frequency (MHz)	Trigger	Set	Reset	Outline	Page
M74HC161P	Presettable 4-Bit Binary Counter with Asynchronous Reset	21	↑	Ⓢ	⌊⌋Ⓐ	16P4	2—190
M74HC161FP						16P2N	
M74HC161DP						16P2P	
M74HC163P	Presettable 4-Bit Binary Counter with Synchronous Reset	21	↑	Ⓢ	⌊⌋Ⓢ	16P4	2—202
M74HC163FP						16P2N	
M74HC163DP						16P2P	
M74HC191P ★★	Presettable 4-Bit Binary Up/Down Counter	—	↑	Ⓐ	—	16P4	2—241
M74HC191FP ★★						16P2N	
M74HC191DP ★★						16P2P	
M74HC193P ★★	Presettable 4-Bit Binary Up/Down Counter with Reset	14	↑	Ⓐ	⌊⌋Ⓐ	16P4	2—249
M74HC193FP ★★						16P2N	
M74HC193DP ★★						16P2P	
M74HC669P ★★	Presettable 4-Bit Binary Up/Down Counter	—	↑	Ⓢ	—	16P4	2—579
M74HC669FP ★★						16P2N	
M74HC669DP ★★						16P2P	

↑ : Positive-going edge ⎍ : Active high ⌊⌋ : Active low Ⓐ : Asynchronous Ⓢ : Synchronous

SYNCHRONOUS DECADE COUNTERS

M74HC160P	Presettable BCD Counter with Asynchronous Reset	21	↑	Ⓢ	⎍Ⓐ	16P4	2—184
M74HC160FP						16P2N	
M74HC160DP						16P2P	
M74HC162P	Presettable BCD Counter with Synchronous Reset	21	↑	Ⓢ	⎍Ⓢ	16P4	2—196
M74HC162FP						16P2N	
M74HC162DP						16P2P	
M74HC190P ★★	Presettable BCD Up/Down Counter	—	↑	Ⓐ	—	16P4	2—239
M74HC190FP ★★						16P2N	
M74HC190DP ★★						16P2P	
M74HC192P ★★	Presettable BCD Up/Down Counter with Reset	14	↑	Ⓐ	⎍Ⓐ	16P4	2—243
M74HC192FP ★★						16P2N	
M74HC192DP ★★						16P2P	
M74HC4017P ★★	Decade Counter/Divider	16	Note	—	⎍Ⓐ	16P4	2—589
M74HC4017FP ★★						16P2N	
M74HC4017DP ★★						16P2P	

↑ : Positive-going edge ⎍ : Active high ⌊⌋ : Active low Ⓐ : Asynchronous Ⓢ : Synchronous

Note : Positive-going edge when the CLOCK pin is used with CE low, negative-going edge when the CLOCK ENABLE pin is used with CP high.

OCTAL COUNTER/DIVIDERS

M74HC4022P ★★	Octal Counter/Divider	16	Note	—	⎍	16P4	2—599
M74HC4022FP ★★						16P2N	
M74HC4022DP ★★						16P2P	

⎍ : Active high

Note : Positive-going edge when the CLOCK pin is used with CE low, negative-going edge when the CLOCK ENABLE pin is used with CP high.

MONOSTABLE MULTIVIBRATORS

Type	Description	Electrical characteristics: Resistance/capacitance connected to control output pulse width	Retrigger function	Reset function	Outline	Page
M74HC123P ★★	Dual Retriggerable Monostable Multivibrator	1~1MΩ/No limits	●	●	16P4	2—114
M74HC123FP ★★					16P2N	
M74HC123DP ★★					16P2P	
M74HC221P ★★	Dual Monostable Multivibrator	1~1MΩ/No limits		●	16P4	2—265
M74HC221FP ★★					16P2N	
M74HC221DP ★★					16P2P	
M74HC4538P ★★	Dual Precision Monostable Multivibrator (Retriggerable, Resettable)	1~1MΩ/No limits	●	●	16P4	2—662
M74HC4538FP ★★					16P2N	
M74HC4538DP ★★					16P2P	

INDEX BY FUNCTION

LATCHES

Type	Description	Electrical characteristics				Enable	Reset	Outline	Page
		Low-level to high-level output propagation time (ns)	High-level to low-level output propagation time (ns)	Setup time (ns)	Hold time (ns)				
M74HC75P	Dual 2-Bit Transparent Latch	32	32	25	5	⊔	—	16P4	2 — 72
M74HC75FP								16P2N	
M74HC75DP								16P2P	
M74HC259P	8-Bit Addressable Latch/1-of-8 Decoder	54	54	25	0	⊓	⊔	16P4	2 —360
M74HC259FP								16P2N	
M74HC259DP								16P2P	
M74HC279P ★★	Quadruple R-S Latch	—	—	—	—	—	—	16P4	2 —375
M74HC279FP ★★								16P2N	
M74HC279DP ★★								16P2P	
M74HC354P ★★	8-Input Data Selector/Multiplexer with Data and Address Latches and with 3-State Outputs	59	59	13	5	⊔	—	20P4	2 —392
M74HC354FP ★★								20P2N	
M74HC354DWP ★★								20P2V	
M74HC356P ★★	8-Input Data Selector/Multiplexer with Data and Address Latches and with 3-State Outputs	63	63	10	5	↑	—	20P4	2 —398
M74HC356FP ★★								20P2N	
M74HC356DWP ★★								20P2V	
M74HC373P	Octal 3-State Noninverting D-Type Transparent Latch	38	38	18	12	⊔	—	20P4	2 —420
M74HC373FP								20P2N	
M74HC373DWP								20P2V	
M74HC373-1P ★★	Octal 3-State Noninverting D-Type Transparent Latch	25	25	13	6	⊔	—	20P4	2 —425
M74HC373-1FP ★★								20P2N	
M74HC373-1DWP ★★								20P2V	
M74HCT373-1P ★★	Octal 3-State Noninverting D-Type Transparent Latch with LSTTL-Compatible Inputs	25	25	13	6	⊔	—	20P4	2 —429
M74HCT373-1FP ★★								20P2N	
M74HCT373-1DWP ★★								20P2V	
M74HC375P	Dual 2-Bit Transparent Latch	32	32	25	5	⊔	—	16P4	2 —447
M74HC375FP								16P2N	
M74HC375DP								16P2P	
M74HC533P	Octal 3-State Inverting D-Type Transparent Latch	38	38	18	12	⊔	—	20P4	2 —462
M74HC533FP								20P2N	
M74HC533DWP								20P2V	
M74HC533-1P ★★	Octal 3-State Inverting D-Type Transparent	25	25	13	6	⊔	—	20P4	2 —467
M74HC533-1FP ★★								20P2N	
M74HC533-1DWP ★★								20P2V	
M74HCT533-1P ★★	Octal 3-State Inverting D-Type Transparent Latch with LSTTL-Compatible Inputs	25	25	13	6	⊔	—	20P4	2 —472
M74HCT533-1FP ★★								20P2N	
M74HCT533-1DWP ★★								20P2V	
M74HC563P ★★	Octal 3-State Inverting D-Type Transparent Latch	28	28	19	6	⊔	—	20P4	2 —498
M74HC563FP ★★								20P2N	
M74HC563DWP ★★								20P2V	
M74HC573P ★★	Octal 3-State Noninverting D-Type Transparent Latch	28	28	19	6	⊔	—	20P4	2 —507
M74HC573FP ★★								20P2N	
M74HC573DWP ★★								20P2V	

⊔ : Active low ⊓ : Active high ↑ : Positive-going edge

INDEX BY FUNCTION

SHIFT REGISTERS

Type	Description	Electrical characteristics: Clock frequency (MHz)	Trigger	Mode: Right shift	Mode: Left shift	Mode: Parallel load	Reset	Outline	Page
M74HC164P	8-Bit Serial-Input/Parallel-Output Shift Register	21	↑	○	—	—	⊔	14P4	2—208
M74HC164FP								14P2N	
M74HC164DP								14P2P	
M74HC165P ★★	8-Bit Serial-or Parallel-Input/Serial-Output Shift Register	21	↑	○	—	○	—	16P4	2—213
M74HC165FP ★★								16P2N	
M74HC165DP ★★								16P2P	
M74HC166P	8-Bit Serial-or Parallel-Input/Serial-Output Shift Register with Reset	25	↑	○	—	○	⊔	16P4	2—219
M74HC166FP								16P2N	
M74HC166DP								16P2P	
M74HC194P	4-Bit Bidirectional Universal Shift Register	24	↑	○	○	○	⊔	16P4	2—255
M74HC194FP								16P2N	
M74HC194DP								16P2P	
M74HC195P	4-Bit Universal Shift Register	24	↑	○	—	○	⊔	16P4	2—260
M74HC195FP								16P2N	
M74HC195DP								16P2P	
M74HC299P ★★	8-Bit Bidirectional Universal Shift Register with 3-State Parallel Outputs	20	↑	○	○	○	⊔	20P4	2—384
M74HC299FP ★★								20P2N	
M74HC299DWP ★★								20P2V	
M74HC323P ★★	8-Bit Bidirectional Universal Shift Register with 3-State Parallel Outputs	—	↑	○	○	○	⊔	20P4	2—391
M74HC323FP ★★								20P2N	
M74HC323DWP ★★								20P2V	
M74HC595P	8-Bit Serial-Input/Serial-or Parallel-Output Shift Register with Latched 3-State Outputs	21	↑	○	—	—	⊔	16P4	2—517
M74HC595FP								16P2N	
M74HC595DP								16P2P	
M74HC597P ★★	8-Bit Serial-or Parallel-Input Serial-Output Shift Register with Input Latch	21	↑	○	—	○	⊔	16P4	2—523
M74HC597FP ★★								16P2N	
M74HC597DP ★★								16P2P	

↑ : Positive-going edge ⊔ : Active low

BINARY RIPPLE COUNTERS

Type	Description	Electrical characteristics: Count frequency (MHz)	Trigger	Reset	Outline	Page
M74HC393P	Dual 4-Stage Binary Ripple Counter	21	↓	⊓	14P4	2—457
M74HC393FP					14P2N	
M74HC393DP					14P2P	
M74HC4020P ★★	14-Stage Binary Ripple Counter	16	↓	⊓	16P4	2—595
M74HC4020FP ★★					16P2N	
M74HC4020DP ★★					16P2P	
M74HC4024P	7-Stage Binary Ripple Counter	21	↓	⊓	14P4	2—605
M74HC4024FP					14P2N	
M74HC4024DP					14P2P	
M74HC4040P ★★	12-Stage Binary Ripple Counter	16	↓	⊓	16P4	2—609
M74HC4040FP ★★					16P2N	
M74HC4040DP ★★					16P2P	

↓ : Negative-going edge ⊓ : Active high

ASYNCHRONOUS DECADE COUNTER

M74HC390P	Dual 4-Stage Binary Ripple Counter with ÷2 and ÷5 Sections	21	↓	⊓	16P4	2—452
M74HC390FP					16P2N	
M74HC390DP					16P2P	

↓ : Negative-going edge ⊓ : Active high

ANALOG SWITCHES/MULTIPLEXERS

Type	Description	Electrical characteristics			Outline	Page
		"ON" resistance, V_I=2.5V (Ω)	Propagation time(ns)			
			From Data input to output	From Control inhibit to output		
M74HC4051P ★★	8-Channel Analog Multiplexer/Demultiplexer	215	15	93	16P4	2—619
M74HC4051FP ★★					16P2N	
M74HC4051DP ★★					16P2P	
M74HC4052P ★★	Dual 4-Channel Analog Multiplexer/Demultiplexer	215	15	93	16P4	2—625
M74HC4052FP ★★					16P2N	
M74HC4052DP ★★					16P2P	
M74HC4053P ★★	Triple 2-Channel Analog Multiplexer/Demultiplexer	215	15	93	16P4	2—630
M74HC4053FP ★★					16P2N	
M74HC4053DP ★★					16P2P	
M74HC4066P	Quad Analog Switch/Multiplexer/Demultiplexer with Enhanced ON-Resistance Linearity	215	13	29	14P4	2—635
M74HC4066FP					14P2N	
M74HC4066DP					14P2P	

DATA SELECTORS/DIGITAL MULTIPLEXERS

Type	Description	Output type	Electrical characteristics			Outline	Page
			Propagation time(ns)				
			Strobe inhibit to output	Select input to output	Data input to output		
M74HC151P	8-Input Data Selector/Multiplexer	NI, I	35	63	49	16P4	2—161
M74HC151FP						16P2N	
M74HC151DP						16P2P	
M74HC153P	Dual 4-Input Data Selector/Multiplexer	NI	24	44	35	16P4	2—166
M74HC153FP						16P2N	
M74HC153DP						16P2P	
M74HC157P	Quadruple 2-Input Noninverting Data Selector/Multiplexer	NI	29	32	32	16P4	2—176
M74HC157FP						16P2N	
M74HC157DP						16P2P	
M74HC158P	Quadruple 2-Input Inverting Data Selector/Multiplexer	I	29	32	32	16P4	2—180
M74HC158FP						16P2N	
M74HC158DP						16P2P	
M74HC251P	8-Input Data Selector/Multiplexer with 3-State Outputs	3S, NI, I	55	51	49	16P4	2—341
M74HC251FP						16P2N	
M74HC251DP						16P2P	
M74HC253P	Dual 4-Input Data Selector/Multiplexer with 3-State Outputs	3S, NI	38	44	35	16P4	2—346
M74HC253FP						16P2N	
M74HC253DP						16P2P	
M74HC257P	Quadruple 2-Input Data Selector/Multiplexer with 3-State Outputs	3S, NI	38	25	25	16P4	2—351
M74HC257FP						16P2N	
M74HC257DP						16P2P	
M74HC258P ★★	Quadruple 2-Input Data Selector/Multiplexer with 3-State Outputs	3S, I	38	25	25	16P4	2—356
M74HC258FP ★★						16P2N	
M74HC258DP ★★						16P2P	
M74HC298P ★★	Quadruple 2-Input Data Selector/Multiplexer with Output Latch	NI	—	—	—	16P4	2—383
M74HC298FP ★★						16P2N	
M74HC298DP ★★						16P2P	
M74HC354P ★★	8-Input Data Selector/Multiplexer with Data and Address Latches and with 3-State Outputs	3S, NI, I	68	71	59	20P4	2—392
M74HC354FP ★★						20P2N	
M74HC354DWP ★★						20P2V	
M74HC356P ★★	8-Input Data Selector/Multiplexer with Data and Address Latches and with 3-State Outputs	3S, NI, I	41	71	63	20P4	2—398
M74HC356FP ★★						20P2N	
M74HC356DWP ★★						20P2V	

I : Inverting output NI : Noninverting output 3S : Three-state output

INDEX BY FUNCTION

DECODERS

Type	Description	Electrical characteristics: Low-level to high-level output propagation time (ns)	Electrical characteristics: High-level to low-level output propagation time (ns)	Outline	Page
M74HC42P	1-of-10 Decoder	38	38	16P4	2 — 55
M74HC42FP				16P2N	
M74HC42DP				16P2P	
M74HC137P	1-of-8 Decoder/Demultiplexer with Address Latch	43	60	16P4	2 —134
M74HC137FP				16P2N	
M74HC137DP				16P2P	
M74HC138P	1-of-8 Decoder/Demultiplexer	38	50	16P4	2 —139
M74HC138FP				16P2N	
M74HC138DP				16P2P	
M74HCT138P ★★	1-of-8 Decoder/Demultiplexer with LSTTL-Compatible Inputs	38	50	16P4	2 —144
M74HCT138FP ★★				16P2N	
M74HC138DP ★★				16P2P	
M74HC139P	Dual 1-of-4 Decoder/Demultiplexer	55	55	16P4	2 —148
M74HC139FP				16P2N	
M74HC139DP				16P2P	
M74HC154P ★★	1-of-16 Decoder/Demultiplexer	42	42	24P4D	2 —171
M74HC154FP ★★				24P2	
M74HC154DWP ★★				24P2V	
M74HC155P	Dual 1-of-4 Decoder/Demultiplexer	—	—	16P4	2 —175
M74HC155FP				16P2N	
M74HC155DP				16P2P	
M74HC237P	1-of-8 Decoder/Demultiplexer with Address Latch	59	47	16P4	2 —267
M74HC237FP				16P2N	
M74HC237DP				16P2P	
M74HC238P ★★	1-of-8 Decoder/Demultiplexer	—	—	16P4	2 —272
M74HC238FP ★★				16P2N	
M74HC238DP ★★				16P2P	
M74HC259P	8-Bit Addressable Latch/1-of-8 Decoder	54	54	16P4	2 —360
M74HC259FP				16P2N	
M74HC259DP				16P2P	
M74HC4511P ★★	BCD-to-Seven-Segment Latch/Decoder/Display Driver	151	151	16P4	2 —647
M74HC4511FP ★★				16P2N	
M74HC4511DWP ★★				16P2P	
M74HC4514P ★★	1-of-16 Decoder/Demultiplexer with Address Latch ("H" Level Output)	58	44	24P4D	2 —652
M74HC4514FP ★★				24P2	
M74HC4514DWP ★★				24P2V	
M74HC4515P ★★	1-of-16 Decoder/Demultiplexer with Address Latch ("L" Level Output)	58	44	24P4D	2 —657
M74HC4515FP ★★				24P2	
M74HC4515DWP ★★				24P2V	
M74HC4543P ★★	BCD-to-Seven-Segment Latch/Decoder/Display Driver for Liquid-Crystal Displays	96	96	16P4	2 —665
M74HC4543FP ★★				16P2N	
M74HC4543DP ★★				16P2P	

DISPLAYED CHARACTERS

M74HC4511P, M74HC4511FP, M74HC4543P, M74HC4543FP

Decimal value	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Display	0	1	2	3	4	5	6	7	8	9						

INDEX BY FUNCTION

ENCODERS

Type	Description	Electrical characteristics: Low-level to high-level output propagation time (ns)	Electrical characteristics: High-level to low-level output propagation time (ns)	Outline	Page
M74HC147P	10-Line Decimal to 4-Line BCD Priority Encoder	38	38	16P4	2—152
M74HC147FP				16P2N	
M74HC147DP				16P2P	
M74HC148P	8-Line to 3-Line Priority Encoder	38	38	16P4	2—156
M74HC148FP				16P2N	
M74HC148DP				16P2P	

COMPARATORS

M74HC85P	4-Bit Magnitude Comparator	58	58	16P4	2— 81
M74HC85FP				16P2N	
M74HC85DP				16P2P	
M74HC688P	8-Bit Equality Comparator	53	53	20P4	2—582
M74HC688FP				20P2N	
M74HC688DWP				20P2V	

FULL ADDERS

M74HC283P	4-Bit Binary Full Adder with Fast Carry	51	51	16P4	2—379
M74HC283FP				16P2N	
M74HC283DP				16P2P	

PARITY GENERATOR/CHECKERS

M74HC280P	9-Bit Odd/Even Parity Generator/Checker	52	52	14P4	2—376
M74HC280FP				14P2N	
M74HC280DP				14P2P	

REGISTER FILES

M74HC670P ★★	4-By-4 Register File with 3-State Outputs	—	—	16P4	2—581
M74HC670FP ★★				16P2N	
M74HC670DP ★★				16P2P	

SYMBOLOGY

Symbol	Discription	
C_I	Input capacitance	The output capafitance at input terminals
C_L	Load capacitance	Extenally connected output capacitance
C_O	Output disable capacitance	The output capacitance when the output is in the high-impedance state
C_{PD}	Power dissipation capacitance	The internal capacitance of the IC calculated from the power dissipation
C_X	External timing capacitance	The capacitance connected to set the pulse width of monostable multivibrators
f_I	Input frequency	The sine wave frequency applied to the input terminal.
f_{max}	Maximum repetition frequency	The maximum frequency of repetitive inputs at which the device operates normally
GND	Ground	
H	High level	Used as a suffix for current and voltage parameters to indicate the high logic level
I	Current or input	Currents flowing into the IC are positive; currents flowing out of the IC are negative
I_{CC}	Supply current	The current flowing into the IC at the V_{CC} pin
I_{DD}	Supply current	The current flowing into the IC at the V_{DD} pin
I_I	Input current	The current that flows into the IC when an input voltage is applied
I_{IH}	High-level input current	The input current for a high-level input
I_{IL}	Low-level input current	The input current for a low-level input
I_O	Output current	Currents flowing into the IC are positive; currents flowing out of the IC are negative
I_{OFF}	Input off-state leak current	The leakage between the input and output terminals of an analog switch in the off state
I_{OH}	High-level output curent	Output load current in the high-level output state
I_{OL}	Low-level output current	Output load current in the low-level output state
I_{OZH}	Off-state high-level output current	Output current when logic high is applied to an output in the high-impedance state
I_{OZL}	Off-state low-level output current	Output current when logic low is applied to an output in the high-impedance state
L	Low level	Used as a suffix for current and voltage parameters to indicate the low logic level
O	Output	Indicates output
P_d	Power dissipation	The product of the supply voltage and supply current
R_I	Input resistance	External resistance connected at input
R_L	Load resistance	External load resistance
R_{OFF}	Analog switch off resistance	The DC resistance of an analog switch in the off state
R_{ON}	Analog switch on resistance	The DC resistance of an analog switch in the on state
R_X	External timing resistance	The resistance connected to set the pulse width of monostable multivibrators
T_a	Ambient temperature	The air temperature in the vicinity of the IC
t_f	Fall time	The period for an input pulse to change from logic high to low
t_h	Hold time	The period other specified inputs must be held after a single specified input is changed
T_{opr}	Operating (ambient) temperatuer	The ambient temperature range over which the IC will operate correctly
t_{pd}	Propagation delay time	The average period from when the specified input is applied until the specified output changes
t_{PHL}	High-level to low-level output propagation time	The period required for the output to change from logic high to low after the specified input is applied
t_{PHZ}	Output disable time from high-level	The period required for the output to change from logic high to the high-impedance state after the specified input is applied
t_{PLH}	Low-level to high-level output propagation time	The period required for the output to change from logic low to high after the specified input is applied
t_{PLZ}	Output disable time from low-level	The period required for the output to change from logic low to the high-impedance state after the specified input is applied
t_{PZH}	Output enable time to high-level	The period required for the output to change from the high-impedance state to logic high after the specified input is applied
t_{PZL}	Output enable time to low-level	The period required for the output to change from the high-impedance state to logic low after the specified input is applied
t_r	Rise time	The period for an input pulse to change from logic low to high
t_{rec}	Recovery time	The period required from when the input state is released until the next clock pulse can be applied
T_{stg}	Storage temperature	The temperature range over which the IC can be safely stored

SYMBOLOGY

Symbol	Discription	
t_{SU}	Setup time	The period that other specified inputs must be held before the specified input can be applied
t_{THL}	High-level to low-level output transition time	The time required for the output to fall after the specified input is applied
t_{TLH}	Low-level to high-level output transition time	The time required for the output to fall after the specified input is applied
t_W	Pulse width	The period over which a pulse remains within the reference voltage range
t_{WQ}	Output pulse width	The pulse width at the output of a monostable multivibrator
V_{CC}	Supply voltage	The voltage applied at the V_{CC} pin
V_{DD}	Supply voltage	The voltage applied at the V_{DD} pin
V_{EE}	Supply voltage	The voltage applied at the V_{EE} pin
V_H	Hysteresis voltage	The difference between the Positive-going and Negative going threshold voltages of a Schmitt trigger circuit
V_I	Input voltage	The voltage applied to an input
V_{IH}	High-level input voltage	The logic high voltage applied to an input
V_{IL}	Low-level input voltage	The logic low voltages applied to an input
V_O	Output voltage	The voltage applied to or appearing at an output
V_{OH}	High-level output voltage	The voltage at the ouptut in the high-level state.
V_{OL}	Low-level output voltage	The voltage at the output in the low-level state
V_{SS}	Supply voltage	The voltage applied at the V_{SS} pin
V_T	Threshold voltage	When an input crosses this voltage level, the output state changes
V_{T+}	Positive-going threshold voltage	The threshold voltage for the low-to-high state change
V_{T-}	Negative-going threshold voltage	The threshold voltage for the high-to low state change
Z	High-impedance state	Indicates an output in the high-impedance state

INTRODUCTION

The Mitsubishi M74HC series high-speed CMOS devices provide the high-speed operation and high-current drive capacity of bipolar LSTTL while retaining the low power consumption and other advantages of CMOS devices.

The M74HC series devices satisfy JEDEC Standard No. 7, and provide the following advatages over LSTTL devices:

- Low power dissipation: P_d=5μW/package, max. (V_{CC}=5V, T_a=25℃, quiesent state)
- High noise margin: 30% of V_{CC}, min. (V_{CC}=4.5V, 6V)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+80℃
- Low input current: $|I_I| \leq 1\mu A$, max.

These characteristics make the series ideally suited to applications in both industrial and consumer digital equipment.

Ratings

The M74HC series is available in three types: the HC type with waveform-regenerator buffered outputs, the unbuffered HCU type, and the HCT type with TTL-level inputs. JEDEC standards have been adopted for all three types. Table 1 shows the JEDEC absolute maximum ratings, Table 2 the recommended operating conditions, and Tables 3 and 4, the electrical characteristics. Tables 5~8 show the corresponding data for Mitsubishi M74HC series.

The characteristics of the Schmitt triggers, open drain outputs, and analog switches do vary somewhat from the JEDEC standards. For detailed information on these differences, please check the individual data sheets of the device in question.

Table 1 JEDEC 74C/HCU/HCT Series Absolute Maximum Ratings

Symbol	Parameter	Type	Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5~+7.0	V
V_I	Input voltage			−0.5~V_{CC}+0.5	V
V_O	Output voltage			−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current		V_I < 0V	−20	mA
			V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current		V_O < 0V	−20	mA
			V_O > V_{CC}	20	
I_O	Output current	Standard		±25	mA
		Buffered		±35	
I_{CC}	Supply/GND current	Standard	V_{CC}, GND	±50	mA
		Buffered		±70	
Tstg	Storage temperature range			−65~+150	℃

Table 2 JEDEC 74HC/HCT Series Recomended Operating Conditions

Symbol	Parameter		Type	Limits			Unit
				Min	Typ	Max	
V_{CC}	Supply voltage		HC/HCU	2		6	V
			HCT	4.5		5.5	
V_I	Input voltage			0		V_{CC}	V
V_O	Output voltage			0		V_{CC}	V
T_{opr}	Operating temperature range			−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	HC	0		1000	ns
		V_{CC} = 4.5V		0		500	
		V_{CC} = 6.0V		0		400	
			HCT	0		500	

Table 3 JEDEC 74HC/HCU Series Electrical characteristics

Symbol	Parameter	Type	Test conditions		V_{CC}(V)	Limits 25℃ Min	Typ	Max	−40~+85℃ Min	Max	Unit
V_{IH}	High-level input voltage	HC	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
					4.5	3.15			3.15		
					6.0	4.2			4.2		
		HCU			2.0	1.7			1.7		
					4.5	3.6			3.6		
					6.0	4.8			4.8		
V_{IL}	Low-level input voltage	HC	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.3		0.3	V
					4.5			0.9		0.9	
					6.0			1.2		1.2	
		HCU			2.0			0.3		0.3	
					4.5			0.8		0.8	
					6.0			1.1		1.1	
V_{OH}	High-level output voltage	HC Standard	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
				I_{OH} = −20μA	4.5	4.4			4.4		
				I_{OH} = −20μA	6.0	5.9			5.9		
				I_{OH} = −4.0mA	4.5	3.98			3.84		
				I_{OH} = −5.2mA	6.0	5.48			5.34		
		HC Buffered	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		
				I_{OH} = −20μA	4.5	4.4			4.4		
				I_{OH} = −20μA	6.0	5.9			5.9		
				I_{OH} = −6.0mA	4.5	3.98			3.84		
				I_{OH} = −7.8mA	6.0	5.48			5.34		
		HCU	V_I = V_{IL}	I_{OH} = −20μA	2.0	1.8			1.8		
				I_{OH} = −20μA	4.5	4.0			4.0		
				I_{OH} = −20μA	6.0	5.5			5.5		
			V_I = GND	I_{OH} = −4.0mA	4.5	3.86			3.76		
				I_{OH} = −5.2mA	6.0	5.36			5.26		
V_{OL}	Low-level output voltage	HC Standard	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
				I_{OL} = 20μA	4.5			0.1		0.1	
				I_{OL} = 20μA	6.0			0.1		0.1	
				I_{OL} = 4.0mA	4.5			0.26		0.33	
				I_{OL} = 5.2mA	6.0			0.26		0.33	
		HC Buffered	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	
				I_{OL} = 20μA	4.5			0.1		0.1	
				I_{OL} = 20μA	6.0			0.1		0.1	
				I_{OL} = 6.0mA	4.5			0.26		0.33	
				I_{OL} = 7.8mA	6.0			0.26		0.33	
		HCU	V_I = V_{IH}	I_{OL} = 20μA	2.0			0.2		0.2	
				I_{OL} = 20μA	4.5			0.5		0.5	
				I_{OL} = 20μA	6.0			0.5		0.5	
			V_I = V_{CC}	I_{OL} = 4.0mA	4.5			0.32		0.37	
				I_{OL} = 5.2mA	6.0			0.32		0.37	
I_{IH}	High-level input current		V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current		V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current		V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current		V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	Gate	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA
		F/F						4.0		40.0	
		MSI						8.0		80.0	

Table 4 JEDEC 74HCT Serieis Electrical Characteristics

Symbol	Parameter	Type	Test conditions		Limits					Unit
					25℃			−40～+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage		V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	4.5 ≤ 5.5	2.0			2.0		V
V_{IL}	Low-level input voltage		V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	4.5 ≤ 5.5			0.8		0.8	V
V_{OH}	High-level output voltage	Standard	$V_I = V_{IH}$, V_{IL}	I_{OH} = −20μA	4.5	4.4			4.4		V
				I_{OH} = −4.0mA	4.5	3.98			3.84		
		Buffered	$V_I = V_{IH}$, V_{IL}	I_{OH} = −20μA	4.5	4.4			4.4		
				I_{OH} = −6.0mA	4.5	3.98			3.84		
V_{OL}	Low-level output voltage	Standard	$V_I = V_{IH}$, V_{IL}	I_{OL} = 20μA	4.5		0.1		0.1	V
				I_{OL} = 4.0mA	4.5		0.26		0.33	
		Buffered	$V_I = V_{IH}$, V_{IL}	I_{OL} = 20μA	4.5		0.1		0.1	
				I_{OL} = 6.0mA	4.5		0.26		0.33	
I_{IH}	High-level input current		V_I = 5.5V		5.5		0.1		1.0	μA
I_{IL}	Low-level input current		V_I = 0V		5.5		−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current		$V_I = V_{IH}$, V_{IL}, $V_O = V_{CC}$		5.5		0.5		5.0	μA
I_{OZL}	Off-state low-level output current		$V_I = V_{IH}$, V_{IL}, V_O = GND		5.5		−0.5		−5.0	μA
I_{CC}	Quiescent supply current	Gate	$V_I = V_{CC}$, GND, I_O = 0μA		5.5		2.0		20.0	μA
		F/F					4.0		40.0	
		MSI					8.0		80.0	
$\triangle I_{CC}$	Maximum quiescent supply current		V_I = 2.4V (Note 1)		5.5		2.7		2.9	mA

Note 1 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

Table 5 Mitsubishi M74HC/HCU/HCT Series Absolute Maximum Ratings

Symbol	Parameter	Type	Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5～+7.0	V
V_I	Input voltage			−0.5～V_{CC}+0.5	V
V_O	Output voltage			−0.5～V_{CC}+0.5	V
I_{IK}	Input protection diode current		V_I < 0V	−20	mA
			V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current		V_O < 0V	−20	mA
			V_O > V_{CC}	20	
I_O	Output current	Standard		±25	mA
		Buffered		±35	
I_{CC}	Supply/GND current	Standard	V_{CC}, GND	±50	mA
		Buffered		±75	
P_d	Power dissipation			500	mW
Tstg	Storage temperature range			−65～+150	℃

Table 6 Mitsubishi M74HC/HCU/HCT Series Recommended Operating Conditions

Symbol	Parameter		Type	Limits			Unit
				Min	Typ	Max	
V_{CC}	Supply voltage		HC/HCU	2		6	V
			HCT	4.5		5.5	
V_I	Input voltage			0		V_{CC}	V
V_O	Output voltage			0		V_{CC}	V
Topr	Operating temperature range			−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	HC	0		1000	ns
		V_{CC} = 4.5V		0		500	
		V_{CC} = 6.0V		0		400	
			HCT	0		500	
			HCU	No limit			

Table 7 Mitsubishi M74HC/HCU/HCT Series Electrical Characteristics (T_a=−40∼+80℃)

Symbol	Parameter	Type	Test conditions		Limits					Unit
					25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	HC	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
		HCU	V_O = 0.2V, $\|I_O\|$ = 20μA	2.0	1.7			1.7		
			V_O = 0.5V, $\|I_O\|$ = 20μA	4.5	3.6			3.6		
			V_O = 0.5V, $\|I_O\|$ = 20μA	6.0	4.8			4.8		
V_{IL}	Low-level input voltage	HC	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
		HCU	V_O = V_{CC}−0.2V, $\|I_O\|$ = 20μA	2.0			0.3		0.3	
			V_O = V_{CC}−0.5V, $\|I_O\|$ = 20μA	4.5			0.8		0.8	
			V_O = V_{CC}−0.5V, $\|I_O\|$ = 20μA	6.0			1.1		1.1	
V_{OH}	High-level output voltage	HC Standard	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
				I_{OH} = −20μA	4.5	4.4			4.4		
				I_{OH} = −20μA	6.0	5.9			5.9		
				I_{OH} = −4.0mA	4.5	4.18			4.13		
				I_{OH} = −5.2mA	6.0	5.68			5.63		
		HC Buffered	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		
				I_{OH} = −20μA	4.5	4.4			4.4		
				I_{OH} = −20μA	6.0	5.9			5.9		
				I_{OH} = −6.0mA	4.5	4.18			4.13		
				I_{OH} = −7.8mA	6.0	5.68			5.63		
		HCU	V_I = V_{IL}	I_{OH} = −20μA	2.0	1.8			1.8		
				I_{OH} = −20μA	4.5	4.0			4.0		
				I_{OH} = −20μA	6.0	5.5			5.5		
			V_I = GND	I_{OH} = −4.0mA	4.5	3.98			3.84		
				I_{OH} = −5.2mA	6.0	5.48			5.34		
V_{OL}	Low-level output voltage	HC Standard	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
				I_{OL} = 20μA	4.5		0.1		0.1	
				I_{OL} = 20μA	6.0		0.1		0.1	
				I_{OL} = 4.0mA	4.5		0.26		0.33	
				I_{OL} = 5.2mA	6.0		0.26		0.33	
		HC Buffered	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	
				I_{OL} = 20μA	4.5		0.1		0.1	
				I_{OL} = 20μA	6.0		0.1		0.1	
				I_{OL} = 6.0mA	4.5		0.26		0.33	
				I_{OL} = 7.8mA	6.0		0.26		0.33	
		HCU	V_I = V_{IH}	I_{OL} = 20μA	2.0		0.2		0.2	
				I_{OL} = 20μA	4.5		0.5		0.5	
				I_{OL} = 20μA	6.0		0.5		0.5	
			V_I = V_{CC}	I_{OL} = 4.0mA	4.5		0.26		0.33	
				I_{OL} = 5.2mA	6.0		0.36		0.33	
I_{IH}	High-level input current		V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current		V_I = 0V		6.0		−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current		V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0		0.5		5.0	μA
I_{OZL}	Off-state low-level output current		V_I = V_{IH}, V_{IL}, V_O = GND		6.0		−0.5		−5.0	μA
I_{CC}	Quiescent supply current	Gate	V_I = V_{CC}, GND, I_O = 0μA		6.0		1.0		10.0	μA
		F/F					2.0		20.0	
		MSI					4.0		40.0	

Table 8 Mitsubishi M74HCT Series Electrical Characteristics (T_a=−40∼+80℃)

Symbol	Parameter	Type	Test conditions		Limits					Unit
					25℃			−40∼+85℃		
					Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage		V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage		V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	Standard	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
				I_{OH} = −4.0mA, V_{CC} = 4.5V	4.18			4.13		
				I_{OH} = −4.8mA, V_{CC} = 5.5V	5.18			5.13		
		Buffered	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		
				I_{OH} = −6.0mA, V_{CC} = 4.5V	4.18			4.13		
				I_{OH} = −7.2mA, V_{CC} = 5.5V	5.18			5.13		
V_{OL}	Low-level output voltage	Standard	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
				I_{OL} = 4.0mA, V_{CC} = 4.5V			0.26		0.33	
				I_{OL} = 4.8mA, V_{CC} = 5.5V			0.26		0.33	
		Buffered	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	
				I_{OL} = 6.0mA, V_{CC} = 4.5V			0.26		0.33	
				I_{OL} = 7.2mA, V_{CC} = 5.5V			0.26		0.33	
I_{IH}	High-level input current		V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-levelinput current		V_I = GND				−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current		V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current		V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	μA
I_{CC}	Quiescent supply current	Gate	V_I = V_{CC}, GND, I_O = 0μA				1.0		10.0	μA
		F/F					2.0		20.0	
		MSI					4.0		40.0	
$\triangle I_{CC}$	Maximum quiescent supply current		V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one is set at this value and other inputs are fixed at V_{CC} or GND

1. Basic Structure

Fig.1 shows the circuit structures of the M74HC series high-speed CMOS logic and the M4000B series (conventional) CMOS logic. The principal difference between the two is that the M4000B series employs aluminum gates, while the M74HC series employs a silicon-gate process. This fine pattern process has enabled us to increase the MOS transistor drive current capability and reduce the parasitic capacitances. (These two improvements allow the new structure to operate at frequencies as fast as LSTTL speed.)

2. Operational Description

Fig.2 show the one stage inverter circuit that is the basis of the high-speed CMOS logic. Fig.3 shows the behavior of this circuit (supply current I_{CC} and output voltage V_O) when the supply voltage is V_{CC} and the input voltage V_I is raised from GND to V_{CC}.

The characteristic curves of the logic are classified by dividing the graph into three regions according to the input voltage.

Ⅰ : In this region, only p-channel transistor T_2 is on. V_O is at V_{CC} and I_{CC} is negligible.

Ⅱ : In this region, V_O varies as a function of V_I. As V_I increases, n-channel transistor T_1 turns on, causing V_O to fall. The slope of the descent steepens abruptly, and the value of V_I at that point is referred to as the threshold voltage of the circuit. Increases of V_I about this value bring V_O very close to GND level.
The value of V_O in region Ⅱ is determined by the relative on resistances of T_1 and T_2. I_{CC} is constantly flowing, and reaches a maximum where V_I equals the threshold voltage.

Ⅲ : In this region, only T_1 is on. V_O is at GND level, and I_{CC} is negligible.

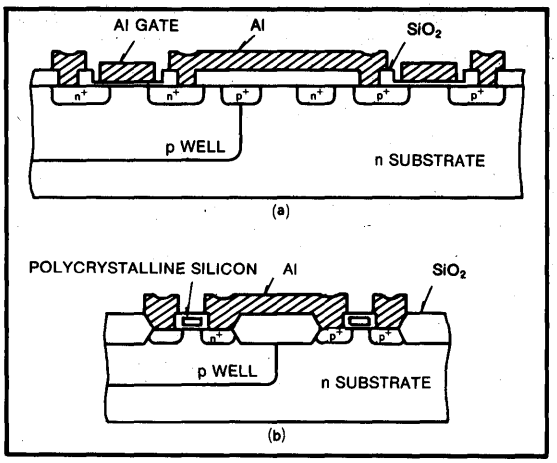


Fig.1 CMOS device structures
(a) Al-GATE CMOS (4000B SERIES)
(b) Si-GATE CMOS (M74HC SERIES)

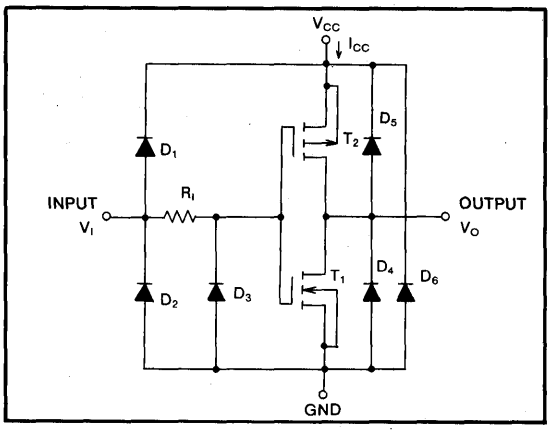


Fig.2 The one stage inverter circuit

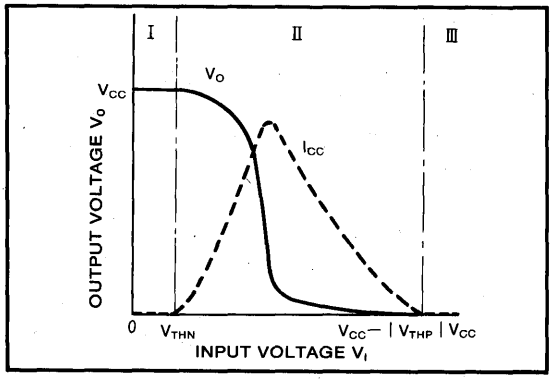


Fig.3 I/O and supply current characteristics of the one stage inverter

3. Transfer Characteristics

In high-speed CMOS logic, the circuit threshold voltage is designed approximately $1/2V_{CC}$, far superior to the TTL and LSTTL logic, where the threshold voltage is independent of the supply voltage.

The M74HC series includes three devices types. The HC type has CMOS-level I/O with buffered outputs. The HCU types has CMOS-level I/O and a single stage of gates. The HCT type has TTL-level inputs and CMOS-level buffered outputs. The accompanying figures show the transfer char-

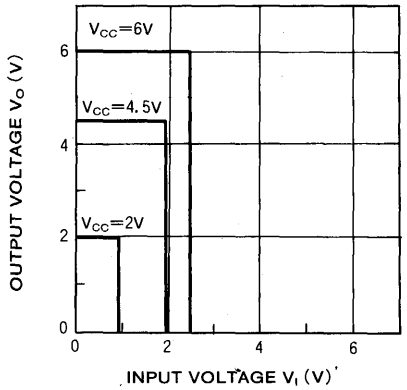


Fig.4-a Qutput voltage vs. input voltage (M74HC00)

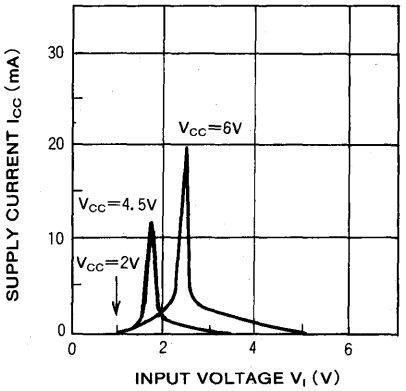


Fig.4-b Supply current vs. input voltage (M74HC00)

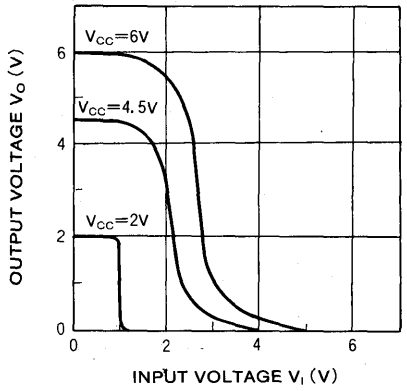


Fig.5-a Output voltage vs. input voltage (M74HCU04)

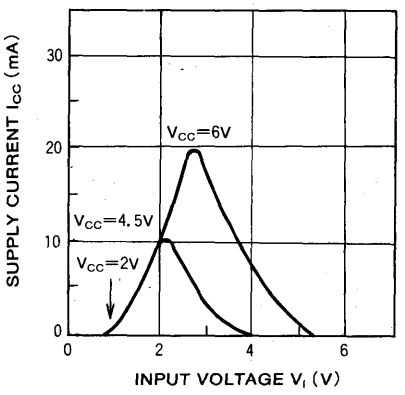


Fig.5-b Supply current vs. input voltage (M74HCU04)

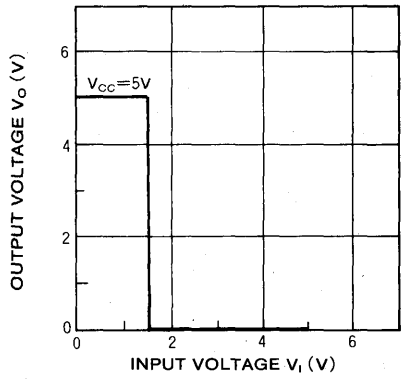


Fig.6-a Output voltage vs. input voltage (M74HCT240)

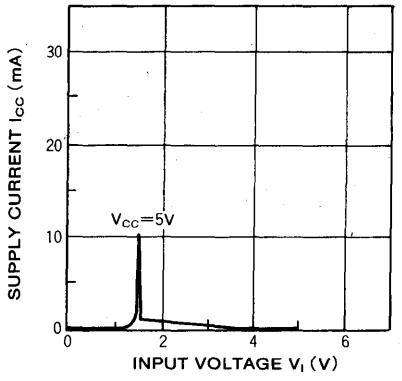


Fig.6-b Supply current vs. input voltage (M74HCT240)

acteristics of representative devices: Fig.4 shows the characteristics of M74HC00, Fig.5 those of M74HCU04, and Fig.6 those of M74HCT240. The left side of the figures (a) shows the output voltage V_O vs. the input voltage V_I. The right side shows the supply current I_{CC} vs the input voltage V_I.

In the HC type, when the input voltage reaches the thresold voltage, the output rieses abruptly and the supply current steeply and then drops steeply. Therefore, even if a slow-changing signal is applied to the input, the output voltnge will be controlled by the steep characteristic curves at the threshold voltage, with the effect of regenerating the input waveforms. These characteristics also prevent the increase in power dissipation that occurs when slow-changing signals are applied to the HCU type.

The output voltage of the HCU type responds more slowly to input voltage variations.

This characteristics make the type suitable for applications in oscillators and other linear circuits. The use of slowly varying input signals, however, will increase the power dissipation.

The HCT type has steep threshold characteristics like the HC type that regenerate the input waveform, but with the HCT type, the input is TTL-level.

4. Switching Characteristics

The propagation time is one of the principal switching characteristics of an IC. In high-speed CMOS, the propagation time is determined by the internal time constant set by the on-state resistances of the p- and n-channel transistors and the capacitance of the wiring and of the next-stage gate. If a capacitive load is connected to the output terminals, the propagation time will be determined by the time constant of the output-stage p- and n-channel transistor on-state resistances and the load capacitance. The supply voltage V_{CC}, the load capacitances C_L, the input rise time t_r, the input fall time t_f, and the ambient temperature T_a all affect the propagation time.

The standard and buffered devices have different output drive-current capacities that cause the two types to exhibit differing relationships between the load capacitance and the propagation delay. Figs. 9 and 10 show the propagation delay vs C_L, Fig. 9 for the standard-type M74HC00, Fig. 10 for buffered-type M74HC240. The propagation delay of the buffered type shows only a small dependence on C_L. In addition, the higher the supply voltage is, the shorter the delay, and the lower the delay dependence on C_L. The delay increase with respect to the load capacitance is linear.

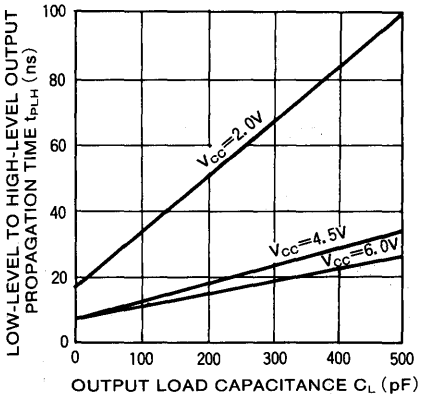


Fig.7-a Low-level to high-level output propagation time (M74HC00)

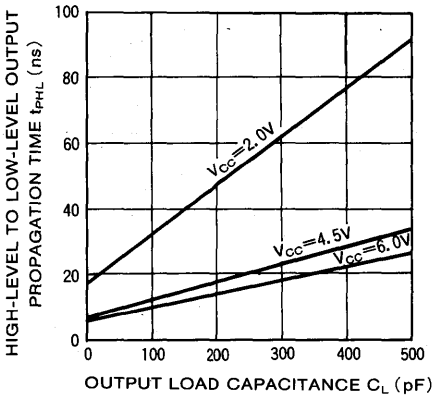


Fig.7-b High-level to low-level output propagation time (M74HC00)

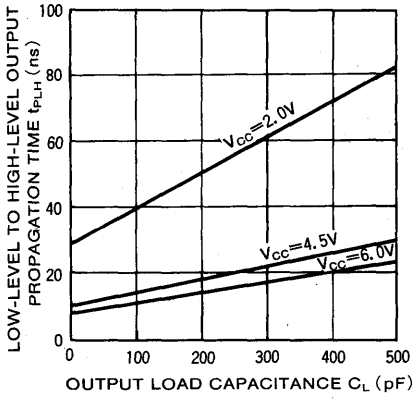


Fig.8-a Low-level to high-level output propagation time (M74HC240)

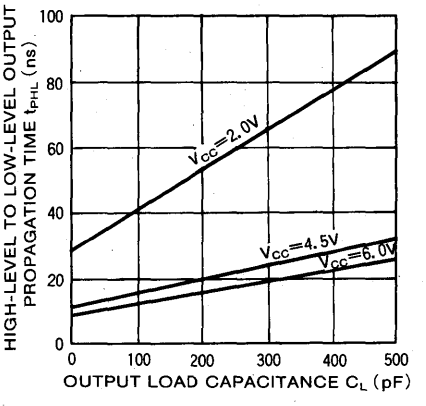


Fig.8-b High-level to low-level output propagation time (M74HC240)

5. Power Dissipation

The high-speed CMOS logic gates consist of n- and p-channel transistors that are serial-connected between V_{CC} and GND. While the gate is held at either V_{CC} or GND, one of the two transistors will be off, which means that while the input is tied to either V_{CC} or GND, the only current drain between V_{CC} and GND (I_{CC}) will be that due to the leakage current of the pn junctions. As a result, the sink current is just 50pA at an ambient temperature T_a=20℃, and still only several nA at T_a=85℃.

As explained in the section 3, high-speed CMOS logic draws greater power during switching, when a current flows between V_{CC} and GND. The higher the supply voltage V_{CC}, and the higher the switching frequency, the larger this current becomes. Capacitive loads at the output due to components or a large fanout will also draw charging currents that further increase the power dissipation. The power dissipation of the HCU type will also rise when driven by input signals with long rise and fall times (t_r, t_f).

Fig.9 shows typical power dissipation vs. operating frequency characteristics per gate of M74HC00 and M74LS00 devices with a capacitive load C_L of 0, 15, and 50pF. The power dissipation of the M74HC00 increases in proportion to the frequency.At a load of 15pF and operating frequency of 10MHz or over, the power dissipation of the M74HC00 exceeds that of the M74LS00, but for must applications, high-speed CMOS logic can substantially reduce power dissipation. When an ideal input waveform is applied, the power dissipation of this logic is given by:

$$P_d=(C_{PD}+C_L)\cdot V_{CC}^2\cdot f+I_{CC}\cdot V_{CC}$$

where C_{PD} is the internal power dissipation capacitance, C_L is the load capacitance, and f is the frequency. So simply connection a capacitive load to the M74HC00 will increase the power dissipation by only the capacitive charging and discharging currents. The same relation holds true in principle for the M74LS00, but even at low frequencies, its power dissipation remains high due to other factors. Another characteristics of high-speed CMOS logic is that the load capacitance is charged at V_{CC} and discharged at GND level, while LSTTL is limited to within the 0.2～4V range. This means that the M74HC00 is more greatly influenced by C_L, so at higher C_L values the bandwidth over which the M74HC00 dissipates less power become narrower. Therefore, good circuit design demands that the capacitative loads be kept as low as possible.

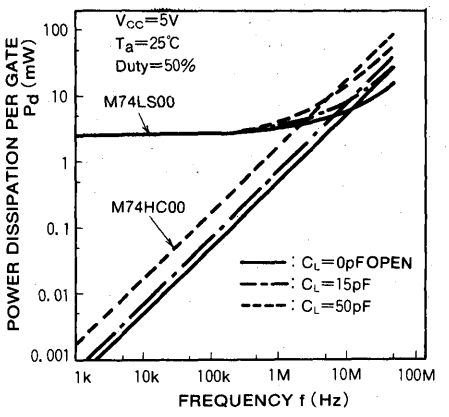


Fig.9 Power dissipation per gate vs. frequency for the M74HC00 and M74LS00

6. Noise Margin

As explained in the section 3, the threshold voltage of high-speed CMOS logic is approximately 1/2 of the supply voltage V_{CC}. In addition, when there is no load, the high-level output voltage V_{OH} is nearly equal to V_{CC}, and the low-level output voltage V_{OL} nearly at GND level. This gives high-speed CMOS logic a much high DC noise margin than LSTTL.

The high-level noise margin V_{HN} and low-level noise margin V_{LN} are given by $V_{HN}=V_{OH}-V_{IL}$, and $V_{LH}=V_{OL}-V_{IL}$. Fig.10 compares V_{HN} and V_{LN} of LSTTL and high-speed CMOS logic at a 5V supply voltage. V_{HN} and V_{LN} are both 1.4 for high-speed CMOS logic, a great improvement over the much lower values of LSTTL. In addition the threshold voltage of LSTTL has a temperature dependence of about −2mV/℃, while high-speed CMOS logic has no such dependence—guaranteeing a constant noise margin over a wide temperature range.

The AC noise margins of LSTTL and high-speed CMOS logic is similar. At a 5V supply voltage, the typical propagation time of both is about 10ns, and both offer similar noise immunity.

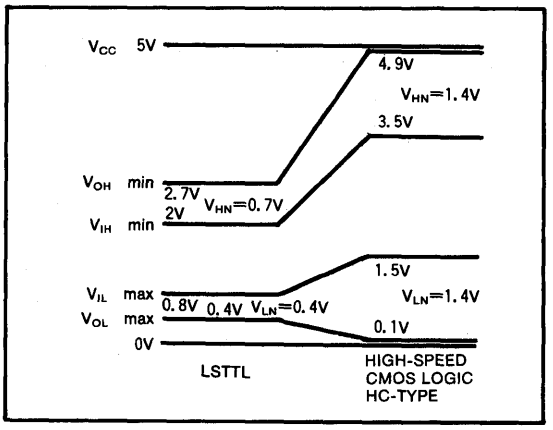


Fig.10 A comparison of LSTTL and high-speed CMOS DC noise margins (V_{CC}=5V)

7. Fanout

Unlike TTL and LSTTL, CMOS logic features an extremely high input impedance, so that when CMOS logic is being driven, high fanout will result in no DC problems. In AC terms, however, the capacitive load increase by the wiring capacitance and about 5pF per driven gate. This increases the propagation time, as shown in Figs. 7 and 8.

8. Input and Output Protection Circuit

The transistors employed in high-speed CMOS logic have a gate-oxide-layer thickness of 0.06μm. This thin oxide layer has an insulation breakdown voltage of only 100V, therefore any larger voltages applied on the gate will destroy the IC. To prevent this from occuring, all devices in the M74HC series feature an input protection circuit consisting of diodes D_1, D_2, and D_3, and resistor R_1 in place of a conventional direct input.

When a steeply sloped positive overvoltage pulse is applied to the input, it charges the parasitic capacitor formed by R_1 in parallel with D_1, D_2, and D_3. The time constant of this circuit delays the voltage rise on the gate, while D_1 passes a current to V_{CC}, this clamps the input voltage at V_{CC}, and prevents high voltages from appearing on the gate oxide layer.

If a steeply sloped negative overvoltage pulse is applied to the input, D_2 and D_3 clamp the gate voltage at their forward-bias voltage level. This means that the circuit can withstand inputs over 500V producted by discharge of a 200pF capacitor, or inputs over 3kV produced by discharge of a 100pF capacitor with a 1.5kΩ resistance. These values are comparable with LSTTL and TTL.

D_4 and D_5 protect the circuit against overvoltages at applied at the outputs. When a surge voltage is applied at V_{CC}, D_6 forms protective circuit. These diodes respond quickly to overvoltages and ensure adequate protection against transients, but extended operation outside the absolute maximum ratings will destroy the protective diodes and the circuit function.

In addition to protection against conditions arising under ordinary use, the M74HC series has been designed to withstand I/O surge currents of up to $\pm$20mA without demage. Although the individual data sheets for the series may not show this I/O protection circuit, each device incorporates this circuit, each device incorporates this circuit.

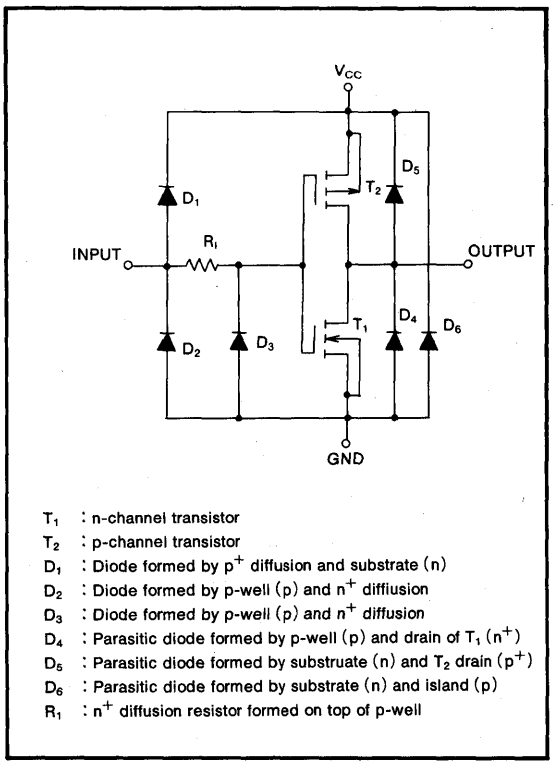


Fig.11 The protection circuit of the M74HC series

DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

This section lists ratings that must be followed to ensure that high-speed CMOS devices operate properly. We define these ratings, describe the test conditions used to measure them, and list standard characteristics.

1. Absolute Maximum Ratings

These are the absolute limits at which the manufacturer guarantees device reliability. None of these ratings may be exceeded, even momentarily, without risking reduced reliability or destruction of the device. Absolute maximum ratings include the following items.

(1) Supply voltage (V_{CC})
(2) Input voltage (V_I)
(3) Switching I/O voltage (V_{IO})
(4) Output voltage (V_O)
(5) Input protection diode current (I_{IK})
(6) Output parasitic diode current (I_{OK})
(7) Output current (I_O)
(8) Supply/GND current (I_{CC})
(9) Power dissipation (P_d)
(10) Storage temperature range (T_{stg})

1-1 Supply Voltage (V_{CC})

Specifies the range of supply voltages that may be safely applied at V_{CC} terminal with respect to ground. This range includes voltage surges that exceed standard operating conditions.

When the applied voltage exceeds this range, parasitic bipolar transistors turn on, and this thyristor operation causes a large current to flow from V_{CC} to GND. This phenomenon, known as "latchup", may either destroy the IC or greatly reduce its reliability.

1-2 Input Voltage (V_I)

Indicates the permissible applied voltage at the input terminals with respect to GND. Exceeding this value may cause latchup.

1-3 Switching I/O Voltage (V_{IO})

Applies to devices containing analog switching circuits such as M74HC4066, and specifies the maximum permissible voltage that may be applied to the switching input or output terminals without causing latchup.

1-4 Output Voltage (V_O)

Usually, fixed voltages are not applied to the output terminals under normal operating conditions, this ratings specifies the maximum surge voltages allowable at the output terminals. When the output state is high, these surges must remain below $V_{CC}+0.5V$, when the output state is low, they cannot drop below $-0.5V$. Surges exceeding the high-state value will cause a current to flow into the IC, which may either destroy the output protection diodes or cause latchup. Surges exceeding the low-state value will cause a current to flow out of the IC with equally damaging effects.

1-5 Input Protection Diode Current (I_{IK})

Usually, fixed currents are not applied to the input terminals under normal operating conditions, specifies the maximum surge current allowable at the input terminals. Surges exceeding this value may destroy the input protection diodes or cause latchup.

1-6 Output Parasitic Diode Current (I_{OK})

Fixed currents are not applied to the output terminals under normal operating conditions.

Specifies the maximum surge currents allowable at the output terminals. The high-state value applies to incoming currents when output is high; the low-state value to outflowing currents when the output is low. Surges exceeding these values may either destroy the output protection diodes or cause latchup.

1-7 Output Current (I_O)

Specifies the maximum allowable currents at the output terminals during normal operation. The high-state value indicates the current outflow, the low-state value, the current influx. Currents exceeding these values may destroy the IC or greatly reduce its reliability.

1-8 Supply/GND current (I_{CC})

Specifies the maximum allowable current flow from V_{CC} to GND during normal operation. Currents exceeding this value may destroy the IC or greatly reduce its reliability.

1-9 Power Dissipation (P_d)

Specifies the maximum allowable power dissipation for the printed-circuit-board-mounted IC at operating temperature (T_{opr}).

1-10 Storage Temperature Range (T_{stg})

Specifies the ambient temperature limits at which the device can be stored when no voltages are applied to either inputs or outputs. Care is especially important when devices are being stored in unheated warehouses or shipped via air freight.

2. Recommended Operating Conditions

These parameters indicate limits of the supply voltage, I/O conditions, and other important factors that must be met for the IC to perform properly under normal use. If these conditions are exceeded, proper operation cannot be guaranteed, even if the device is still operating within the absolute maximum ratings.

2-1 Supply Voltage (V_{CC})

Specifies the supply voltage applied at V_{CC} with respect to ground. The supply voltge of high-speed CMOS devices is 2~6V (4.5~5.5V for type HCT), which is much wider than TTL devices (4.75~5.25V).

2-2 Input Voltage (V_I)

Specifies the optimum input voltage range. This range is the same for all supply voltage range of $V_{CC}=2\sim6V$.

2-3 Output Voltage (V_O)

Specifies desirabel limits for transient voltages at the output pins. This range is the same for all supply voltage range of $V_{CC}=2\sim6V$.

2-4 Operating Temperature Range (T_{opr})

Specifies the ambient tmeperature range within which the

device exhibits the specified electrical characteristics and performs normally.

2-5 Rise and Fall Times (t_r, t_f)

Specifies the optimum rise and fall times of the input waveforms. These limits should be followed at all supply voltages of V_{CC} = 2, 4.5, and 6V, otherwise output oscillation, timing problems, or excessive power dissipation may result. This restriction does not apply to devices incorporating Schmitt trigger inputs.

3. Function

The functional behavior of the device is indicated by either a function table or a timing diagram. These characteristics are checked over the 2~6V supply voltage range. The inputs are set high or low as specified, and the output conditions monitored.

4. Electrical Characteristics (see Section 7-1)

These characteristics are measured at input and output and power supply terminals at temperature T_a under worst-case conditions. All parameters are guaranteed at 2, 4.5, and 6V supply voltages, except for I_{IH}, I_{IL}, I_{OZH}, I_{OZL}, and I_{CC}, which are guaranteed at V_{CC}=6V only.

4-1 High-Level Input Voltage (V_{IH})

Specifies the high-level input voltage required to generate the specified output conditions.

4-2 Low-level Input Voltage (V_{IL})

Specifies the low-level input voltage required to generate the specified output conditions.

4-3 Positive-going Threshold Voltage (V_{T+})

In devices with Schmitt trigger inputs, this parameter indicates the voltage at which the output state inverts as the input voltage is increased from a level below the negative-going threshold voltage (V_{T-}).

4-4 Negative-going Threshold Voltage (V_{T-})

In devices with Schmitt trigger inputs, this parameter indicates the voltage at which the output state inverts as the input voltage is decreased from a level above the positive-going threshold voltage (V_{T+}).

4-5 Hysteresis Voltage (V_H)

In devices with Schmitt trigger inputs, this parameter indicates the difference between the positive-going and negative-going threshold voltages.

4-6 High-level Output Voltage (V_{OH})

Indicates the high-level output voltage obtained at the outputs when high-level input voltage V_{IH} (V_{T+} for Schmitt trigger devices) and low-level input voltage V_{IL} (V_{T-} for Schmitt trigger devices) are applied as specified to the input terminals indicated to the input.

4-7 Low-Level Output Voltage (V_{OL})

Similar to the above. Indicates the low-level output voltage obtained under the specified conditions.

4-8 Maximum Output Leak Current (I_O)

In devices with open drain outputs, this parameter indicates the current outflow with 0V applied at the output voltage or current influx with 6V applied at the output. The supply voltage is 6V.

4-9 On-State Resistance (R_{ON})

Applies to devices containing analog switching circuits. Indicates the DC on-state resistance of the analog switches. Guaranteed for input voltage of 0 to V_{CC}.

4-10 On-State Resistance Variation (ΔR_{ON})

Indicates the difference between the maximum and minimum on-state resistance values (R_{ON}) for analog switches in a single device.

4-11 Off-State Input-to-Output Leak Current (I_{OFF})

Indicates the leakage current that flows from the input to the output of analog switches when 6V is applied. Specified at V_{CC}=6V.

4-12 High-Level Input Current (I_{IH})

Indicates the current that flows into the device when 6V is applied to the input at V_{CC}=6V. I_{IH} for type HCT is determined with input and supply voltages of 5.5V.

4-13 Low-Level Input Current (I_{IL})

Indicates the current that flows out of the device when 0V is applied to the input at V_{CC}=6V. I_{IL} for type HCT is determined with a supply voltage of 5.5V.

4-14 Off-state High-Level Output Current (I_{OZH})

Applies to devices with three-state outputs. Indicates the current that flows into the device when 6V is applied to an output in the high-impedance state at V_{CC} = 6V. I_{OZH} for type HCT is determined with input and supply voltage of 5.5V. When the outputs are not in the high-impedance state, they are kept low by selection of the input conditions.

4-15 Off-State Low-Level Output Current (I_{OZL})

Applies to devices with three-state outputs. Indicates the current that flows out of the device when 0V is applied to an output in the high-impedance state at V_{CC}=6V. I_{OZL} for type HCT is determined with a supply voltage of 5.5V. when the outputs are not in the high-impedance state, they are kept high by selection of the input conditions.

4-16 Quiescent Supply Currnet (I_{CC})

Indicates the current that flows at V_{CC} when the output conditions are stable. The stated values are guaranteed when the input conditions are set according to the function table with high-level inputs at V_{CC} and low-level inputs at ground.

4-17 Maximum Quiesenct Supply Current (ΔI_{CC})

Applies to device with TTL-level inputs (type HCT). Indicates the current that flows at V_{CC} when the output conditions are stable. The current is specified with 2.4V and 0.4V applied at a single input while all other inputs are held at V_{CC} or ground and V_{CC} is at 5V±10%.

4-18 Active-State Supply Currnet (I_{CC})

Applies to one-shot multivibrator circuits. Indicates the current that flows at V_{CC} when the timing circuit constate R_X/C_X is 1/2V_{CC}. The stated values are guaranteed when the

DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

input conditions are set according to the function table with high-level inputs at V_{CC} and low-level inputs at GND.

5. Switching Characteristics (see sections 7-2, 7-3, and 7-4)

The switching characteristics are measured at $T_a = -40 \sim +85°C$, and include the output waveform transition time, propagation time and maximum clock frequency. The measurements are performed with input pulses of specified rise and fall times (t_r, t_f) and specified output load capacitance C_L.

5-1 Low-Level to High-Level Output Transistion Time (t_{TLH})

Indicates the time required for the output waveform to change from 10% to 90% of V_{CC} when inputs are applied to cause the output to change from low to high.

5-2 High-Level to Low-Level Output Transition Time (t_{THL})

Indicates the time required for the output waveform to change from 90% to 10% of V_{CC} when inputs are applied to cause the output to change from high to low.

5-3 Low-Level to High-Level Output Propagation Time (t_{PLH})

Indicates the time required from when the input conditions are changed until the output voltage crosses the specified voltage range moving from low to high.

5-4 High-Level Low-Level Output Propagation Time (t_{PLH})

Indicates the time required from when the input conditions are changed until the output voltage crosses the specified voltage range moving from high to low.

5-5 Output enable time to high-level (t_{PZH})

Applies to devices with three-state outputs. Indicates the time required from when the input conditions are changed until the output state changes from the high-impedance state to logic high.

5-6 Output enable time to low-level (t_{PZL})

Applies to devices with three-state outputs. Indicates the time required from when the input conditions are changed until the output state changes from the high-impedance state to logic low.

5-7 Output disable time from high-level (t_{PHZ})

Applies to devices with three-state ouptuts. Indicates the time required from when the input conditions are changed until the output state changes from logic high to the high-impedance state.

5-8 Output disable time from low-level (t_{PLZ})

Applies to devices with three-state outputs. Indicates the time required from when the input conditions are changed until the output state changes from logic low to the high-impedance state.

5-9 Maximum clock Frequency (f_{max})

Applies to devices containing flip flops. Indicates the maximum frequency at which clock signals can be applied while maintaingin stable output waveforms in the specified sequence. The input conditions are set so that each clock pulse will cause a change in the output state.

5-10 Sine Wave Distortion

Applies to devices containing analog switches. indicates the distortion of sine waves passing through analog switches in the "on" state. The sine wave frequency is 1kHz, and the amplitude $1.25V_{P-P}$. Measurements are performed at $V_{CC}=2.5V$, and $V_{SS}=-2.5V$.

5-11 Maximum Transmission Frequency (f_{max}(I/O))

Applies to devices containing analog switches. Indicates the frequency bandwidth transmitted by analog switches in the "on" state. A $1.25V_{P-P}$ sine wave is applied at the I/O terminals and the frequency is increased until the output is 3dB down from the input level (about 7/10). This frequency is designated at f_{max} (I/O). Measurements are performed at $V_{CC}=2.5V$, and $V_{SS}=-2.5V$.

5-12 Feedthrough

Applies to devices containing analog switches. Indicates the degree of isolation between the I/O terminals of a switch in the off-state. When a sine wave signal is applied at one side of an off-state switch, it is transmitted through the static capacitnace of IC to the other side of the switch at a level that increases proportionally with the frequency of the applied signal. The frequency at which the output voltage is 50dB down from the input voltage (about 1/316), is defined as the feedthrough level.

5-13 Crosstalk (Control-Input-to-Switch)

Applies to devices containing analog switches. Indicates the degree of interference between signals at the control inputs and those at the I/O pins of the analog switches. A pulse is applied to a control input, and the pulse level at an switch terminal is measured with no inputs applied to the switch inputs.

5-14 Crosstalk (Switch-to-Switch)

Applies to devices containing analog swithces. Indicates the degree of interference between signals at the I/O terminals of independent switches. A pulse is applied at an on-state switch input, and the pulse level at the output of a separate off-state switch is measured.

5-15 Maximum Control Frequency (f_{max} (C))

Applies to devices containing analog switches. Indicates the maximum allowable frequency of the signals applied to the control inputs. A standard square-wave signal is applied at a control input, and the frequency is increased until the output level falls to 1/2 of the output level at an input frequency of 1kHz. This frequency is defined as f_{max} (C).

5-16 Input Capacitance (C_I)

Indicates the capacitance between an input terminal and GND. It is normally measured at 0V and f=1MHz.

5-17 Feedthrough Capacitance ($C_{X-Y,\ Y-X}$)

Applies to devices containing analog switches. Indicates the capacitance between I/O terminals of a switch in the off state.

5-18 Off-State Output Capacitance (C_O)

Applies to devices with three-state or open-drain outputs. Indicates the capacitance between outputs in the high-impedance state and ground.

5-19 Power Dissipation Capacitance (C_{pd})

Indicates the internal capacitnace of the device, calculated on the basis of the power dissipation during no-load operation. The no-load power dissipation is calculated as;

$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$$

6. Timing Requirements (see sections 7-2 and 7-3)

These parameters specify the input timing requirements for clock pulses, reset pulses, etc. required by devices containging flip flops to maintain stable output waveforms in the specified sequence.

Timing requirements are measured at $T_a = 25℃$, and include pulse width, setup time, hold time, and recovery time.

6-1 Pulse Width (t_w)

Specifies the minimum interval between the standard voltage levels on the leading and trailing edges of input pulses. Shorter pulses may be ignored or may cause misoperation.

6-2 Setup Time (t_{su})

For input data to be read correctly when a clock pulse or similar read signal is applied, the input conditions must be set in advance by a specified interval termed as the setup time. The setup time is defined as the period from the standard voltage levels of the active edges of the input signals until the standard voltage level of the read signal active edge. Negative setup times indicate that the input conditions can be set after the read signal.

6-3 Hold Time (t_h)

For input data to be read correctly when a clock pulse or similar read signal is applied, the input conditions must be held for specified interval after the read signal is applied. This interval is termed as the hold time. Negative hold times indicate that the input conditions can be changed before the read signal is applied.

6-4 Recovery Time (t_{rec})

The recovery time indicates the interval after a read operation has been performed until a clock pulse can be applied to initiate the next read operation. It is specified as the period between the read operation and the standard voltage level of the clcok pulse active edge.

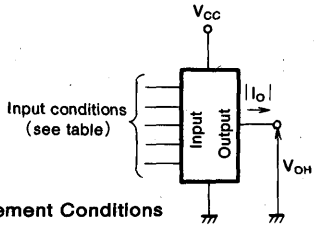
7. Test Circuits

This sections shows typical test circuits used to measure the above paramenters. For detailed test conditions specific to individual devices, refer to the individual data sheets.

DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

7-1 DC Test Circuits

7-1-1 V_{IH}, V_{IL} (1)

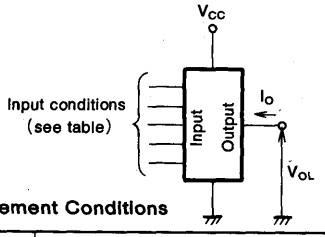


Measurement Conditions

Function	Input conditions
NAND	Input under test at V_{IL}, all others at V_{IH}
AND	All inputs at V_{IH}
NOR	All inputs at V_{IL}
OR	Input under test at V_{IH}, all others at V_{IL}

Note : The input conditions of devices with three-state inputs are set to place the outputs in the active (low-impedance) state.

7-1-2 V_{IH}, V_{IL} (2)

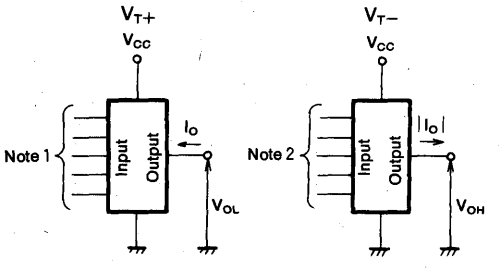


Measurement Conditions

Function	Input conditions
NAND	All inputs at V_{IH}
AND	Input under test at V_{IL}, all others at V_{IH}
NOR	Input under test at V_{IH}, all others at V_{IL}
OR	All inputs at V_{IL}

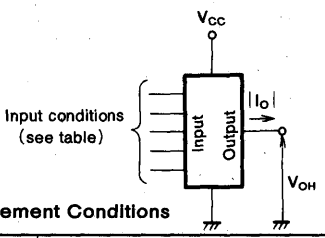
Note : The input conditions of devices with three-state inputs are set to place the outputs in the active (low-impedance) state.

7-1-3 V_{T+}, V_{T-}, V_H ($V_{T+}-V_{T-}$)



Note 1 : When measuring V_{T+}, all inputs are set at V_{T+}.
Note 2 : When measuring V_{T-}, the input under test is set at V_{T-}, and all others at V_{T+}.
Note 3 : Measured at all inputs.

7-1-4 V_{OH}

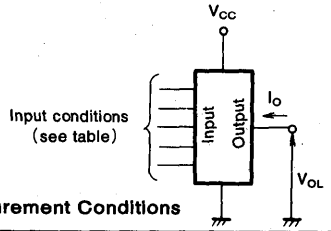


Measurement Conditions

Function	Input conditions
NAND	Input under test at V_{SS}, all others at V_{CC}
AND	All inputs at V_{CC}
NOR	All inputs at GND
OR	Input under test at V_{DD}, all others at GND

Note : The input conditions of devices with three-state inputs are set to place the outputs in the active (low-impedance) state.

7-1-5 V_{OL}

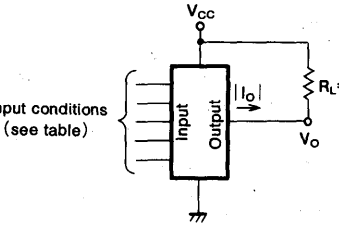


Measurement Conditions

Function	Input conditions
NAND	All inputs at V_{CC}
AND	Input under test at GND, all others at V_{CC}
NOR	Input under test at V_{CC}, all others at GND
OR	All inputs at GND

Note : The input conditions of devices with three-state inputs are set to place the outputs in the active (low-impedance) state.

7-1-6 I_O

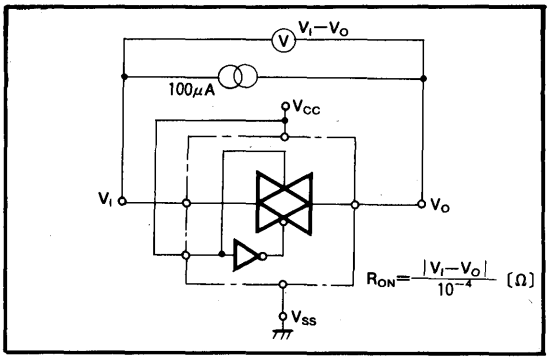


Measurement Conditions

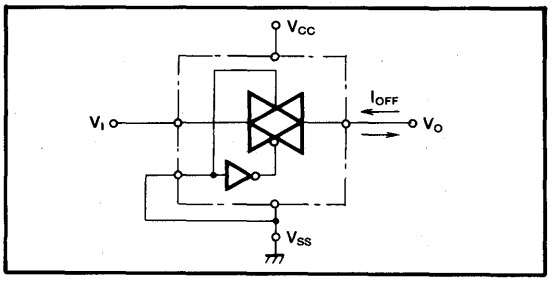
Function	Input conditions
NAND	Input under test at GND, all others at V_{CC}
AND	All inputs at V_{CC}
NOR	All inputs at GND
OR	Input under test at V_{CC}, all others at GND

DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

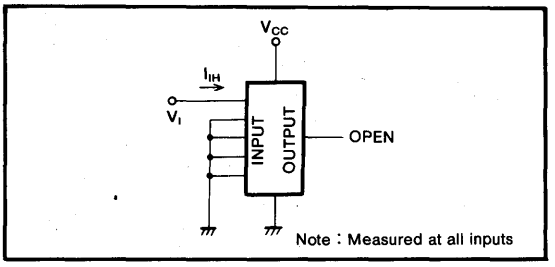
7-1-7 On-State Resistance (R_{ON})



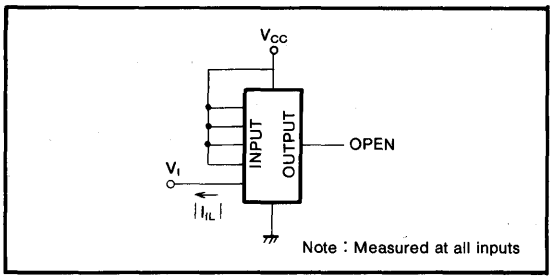
7-1-8 I_{OFF}



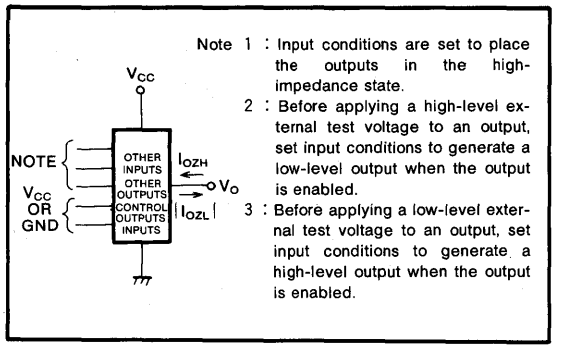
7-1-9 I_{IH}



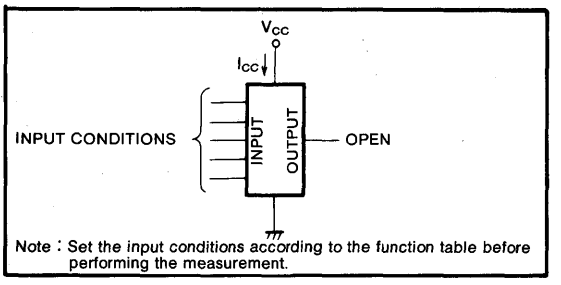
7-1-10 I_{IL}



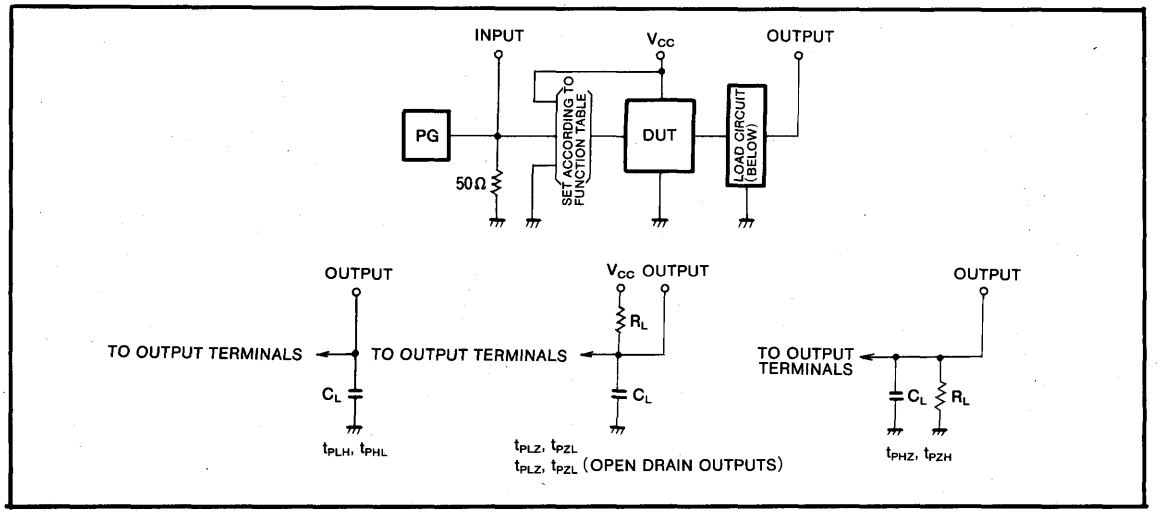
7-1-11 I_{OZH}, I_{OZL}



7-1-12 I_{CC}



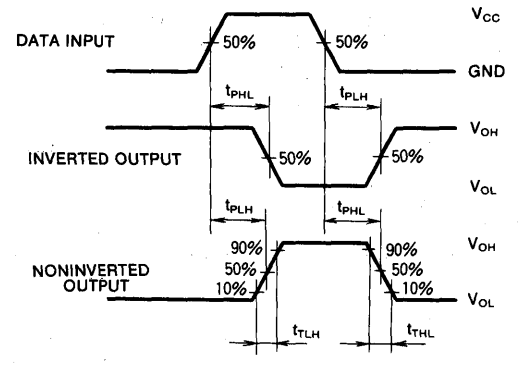
7-2 Switching Characteristics Test Circuits

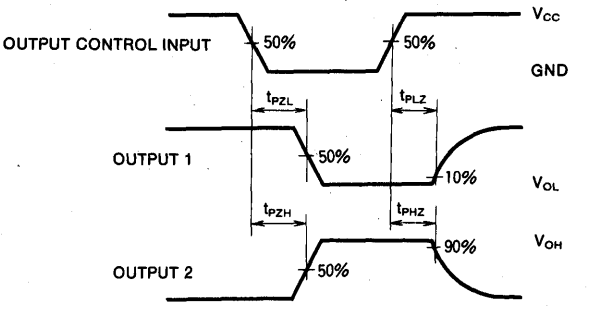


7-3 Timing Charts

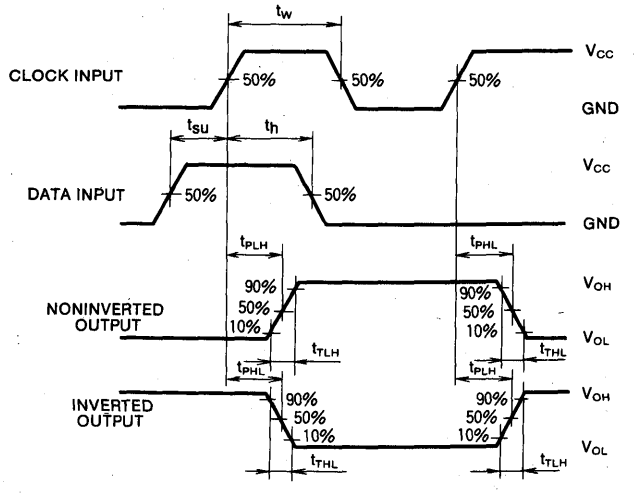
7-3-1 Types HC and HCU

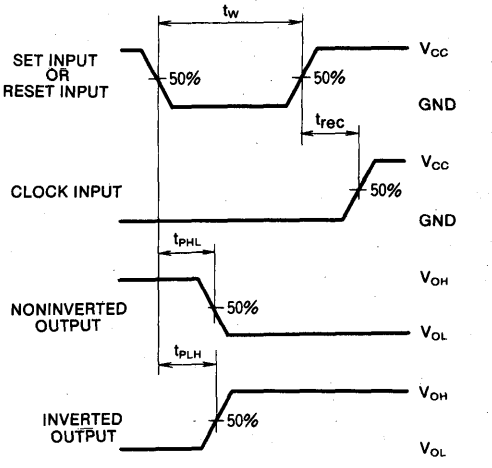
○Typical Gate (including gates with three-state outputs)



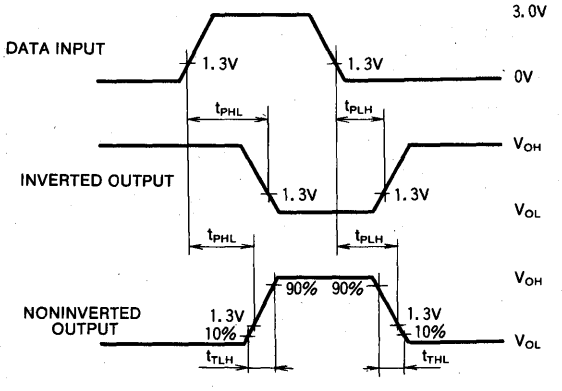


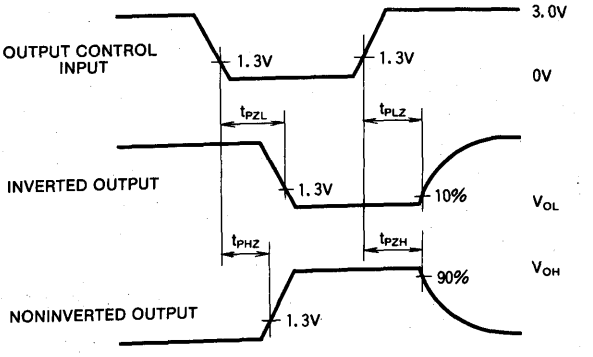
○Typical Flip Flop





7-3-2 Type HCT

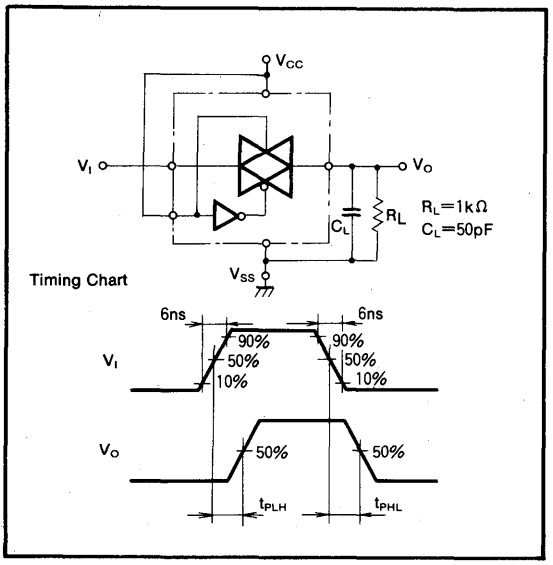




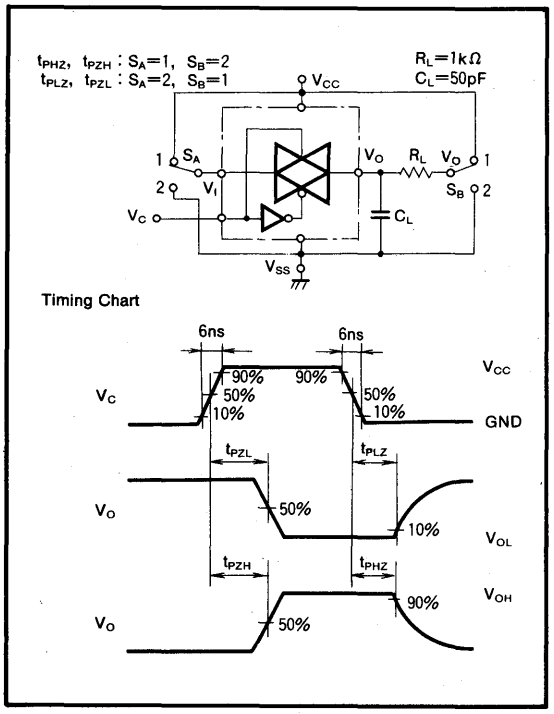
DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

7-4 Switching Characteristic Test Circuits for Analog Switchs

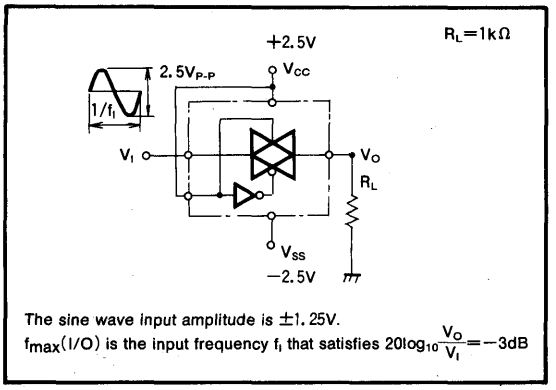
7-4-1 Low-Level to High-Level and High-Level to Low-Level Propagation Time (I/O-to-I/O)



7-4-2 Low-Level to High-Level and High-Level to Low-Level Propagation Time (Control-Input-to-I/O)

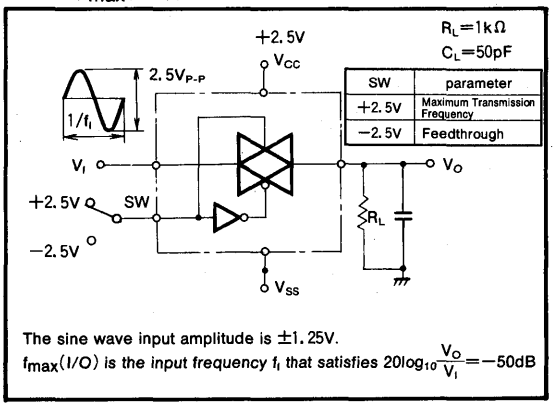


7-4-3 Sine Wave Transmission



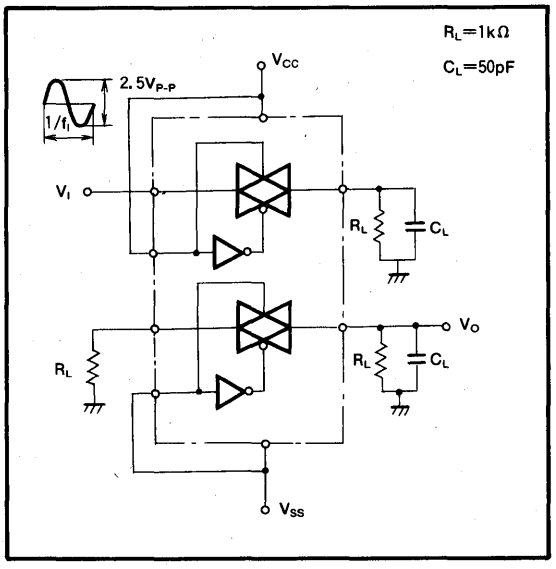
The sine wave input amplitude is ±1.25V.
f_{max}(I/O) is the input frequency f_i that satisfies $20\log_{10}\frac{V_O}{V_I}=-3dB$

7-4-4 Feedthrough, Maximum Transmission Frequency (f_{max}(I/O))



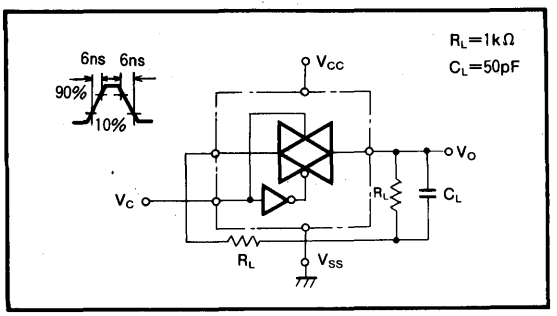
The sine wave input amplitude is ±1.25V.
f_{max}(I/O) is the input frequency f_i that satisfies $20\log_{10}\frac{V_O}{V_I}=-50dB$

7-4-5 Crosstalk (Switch-to-Switch)

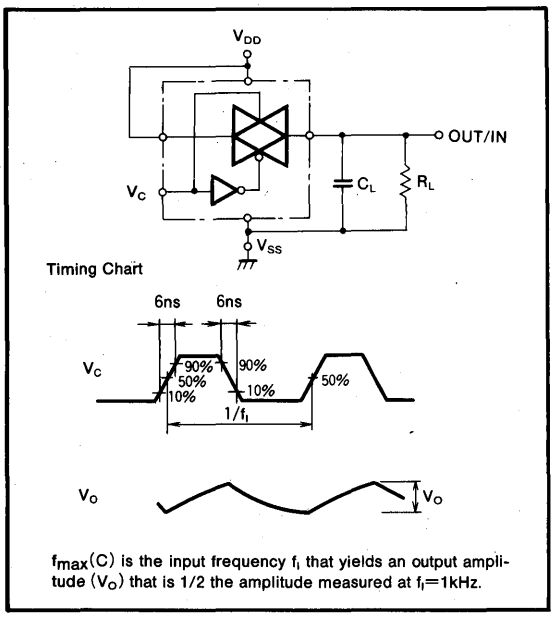


DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

7-4-6 Crosstalk (Control-Input-to-Switch)

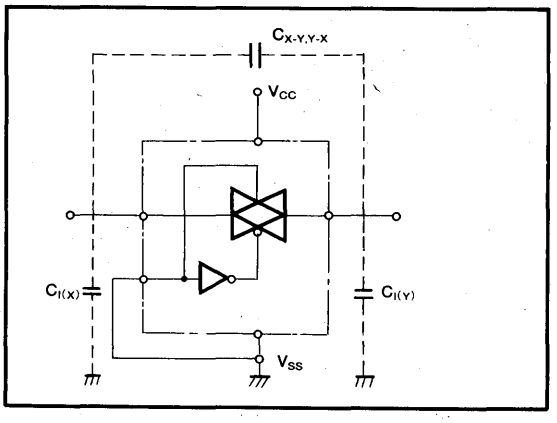


7-4-7 Maximum Control Frequency ($f_{max}(C)$)



$f_{max}(C)$ is the input frequency f_i that yields an output amplitude (V_O) that is 1/2 the amplitude measured at f_i=1kHz.

7-4-8 Input Capacitance C_I, Feedthrough Capacitance ($C_{X-Y, Y-X}$)

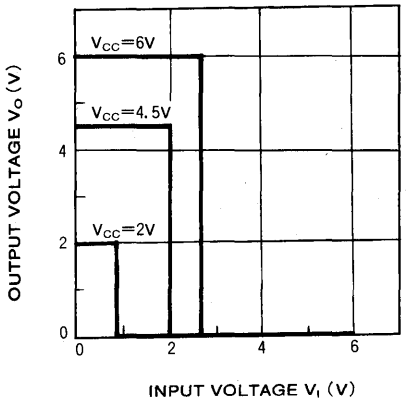


DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

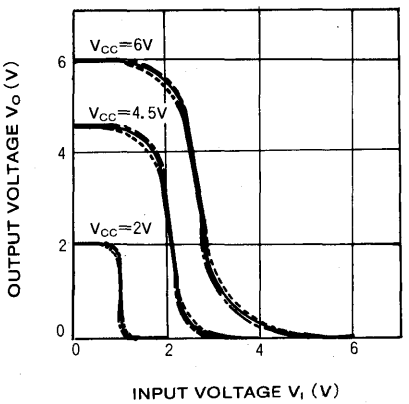
8. Basic Gate Characteristics

T_a=−45℃ —·—·—
T_a=25℃ ————
T_a=85℃ - - - - - -

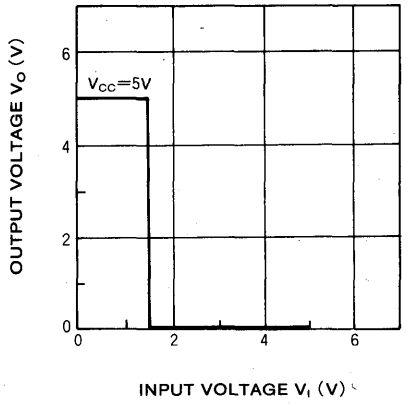
INPUT-TO-OUTPUT TRANSFER CHARACTERISTICS
M74HC00P



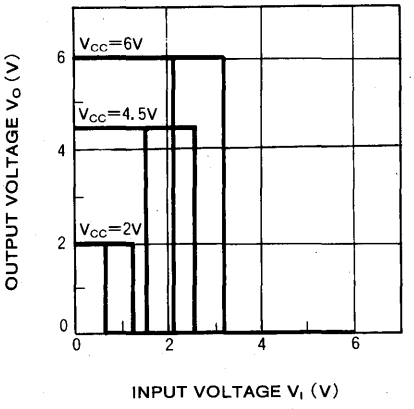
INPUT-TO-OUTPUT TRANSFER CHARACTERISTICS
M74HCU04P



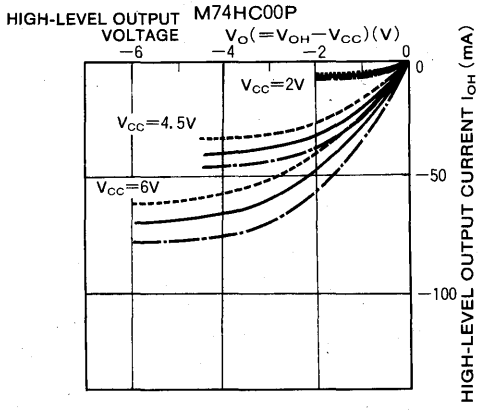
INPUT-TO-OUTPUT TRANSFER CHARACTERISTICS
M74HCT240P



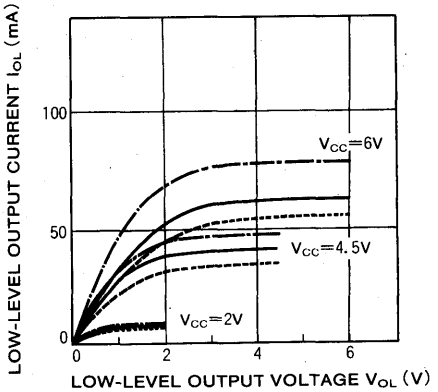
INPUT-TO-OUTPUT TRANSFER CHARACTERISTICS
M74HC132P



HIGH-LEVEL OUTPUT CURRENT VS HIGH-LEVEL OUTPUT VOLTAGE
M74HC00P

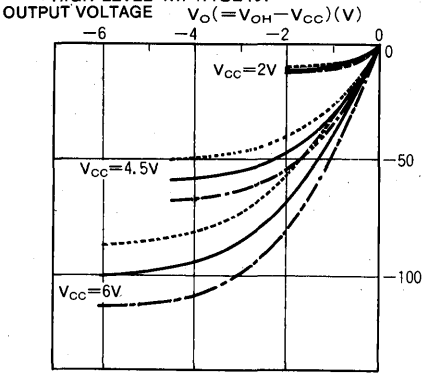


LOW-LEVEL OUTPUT CURRENT VS LOW-LEVEL OUTPUT VOLTAGE
M74HC00P

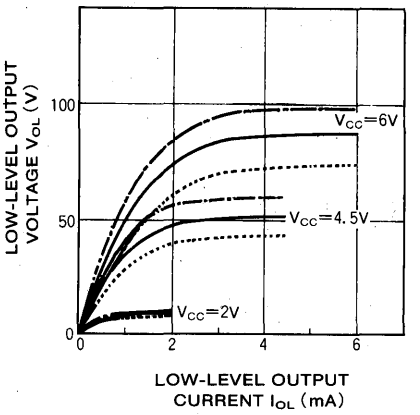


DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT CURRENT VS
HIGH-LEVEL OUTPUT VOLTAGE
M74HC240P

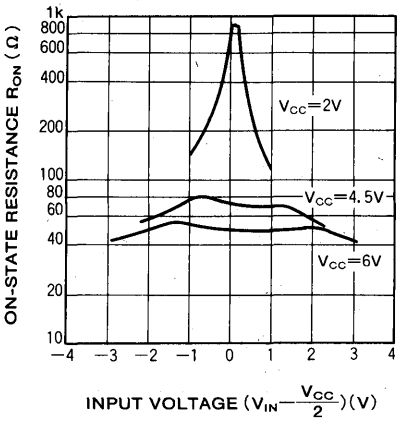


LOW-LEVEL OUTPUT CURRENT VS
LOW-LEVEL OUTPUT VOLTAGE
M74HC240P



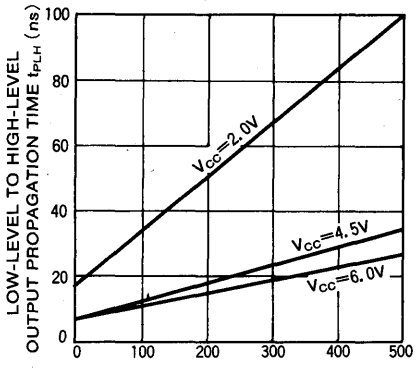
ANALOG SWITCH
ON-STATE RESISTANCE

M74HC4066P

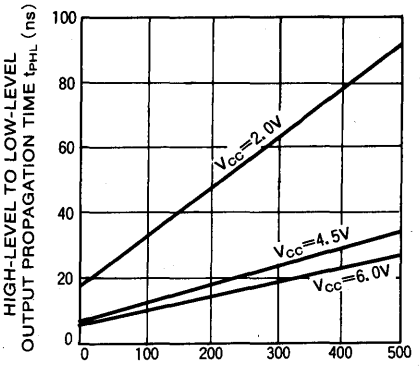


DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

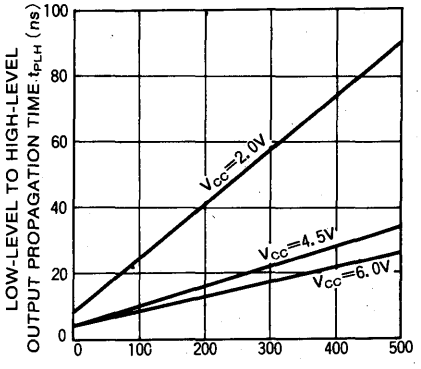
LOW-LEVEL TO HIGH-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE
M74HC00P



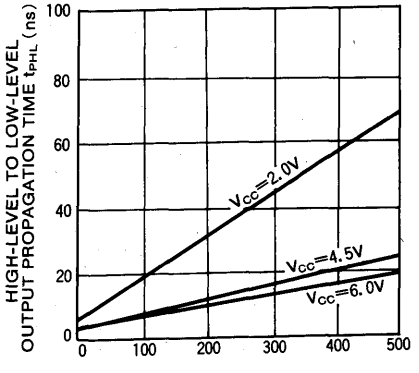
HIGH-LEVEL TO LOW-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE
M74HC00P



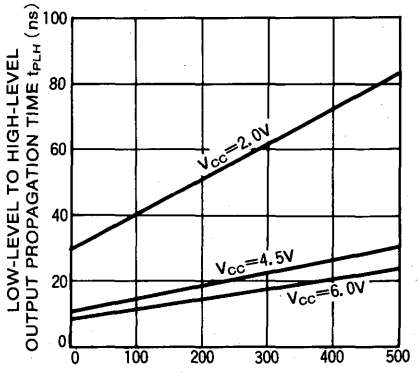
LOW-LEVEL TO HIGH-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE
M74HCU04P



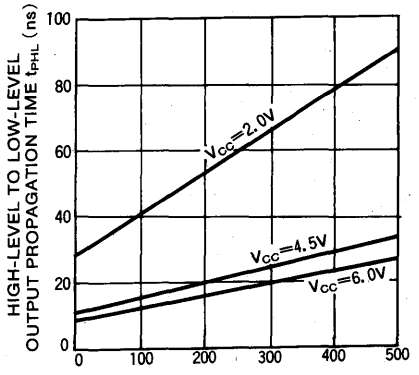
HIGH-LEVEL TO LOW-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE
M74HCU04P



LOW-LEVEL TO HIGH-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE
M74HC240P



HIGH-LEVEL TO LOW-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE
M74HC240P



THE MITSUBISHI QUALITY-ASSURANCE SYSTEM AND DEVICE RELIABILITY DATA

1. Introduction

Technical advances in recent years have allowed manufactures to repidly improve the speed, integration scale, and other facets of IC performance. At the same time, the greater complexity and reliability demands of the electronic-equipment market and the heavy use ICs in automatic insertion and assembly operations mean that manufacturers need reliable devices with consistent performance paramenters. This section introduces the quality-assurance system and reliablility test procedures used at Mitsubishi Electric to guarantee that our customers receive highly uniform and reliable products.

2. The Quality-Assurance System

This system consists of quality-assurance procedures in the design and production processes. Fig. 1 shows the entire system.

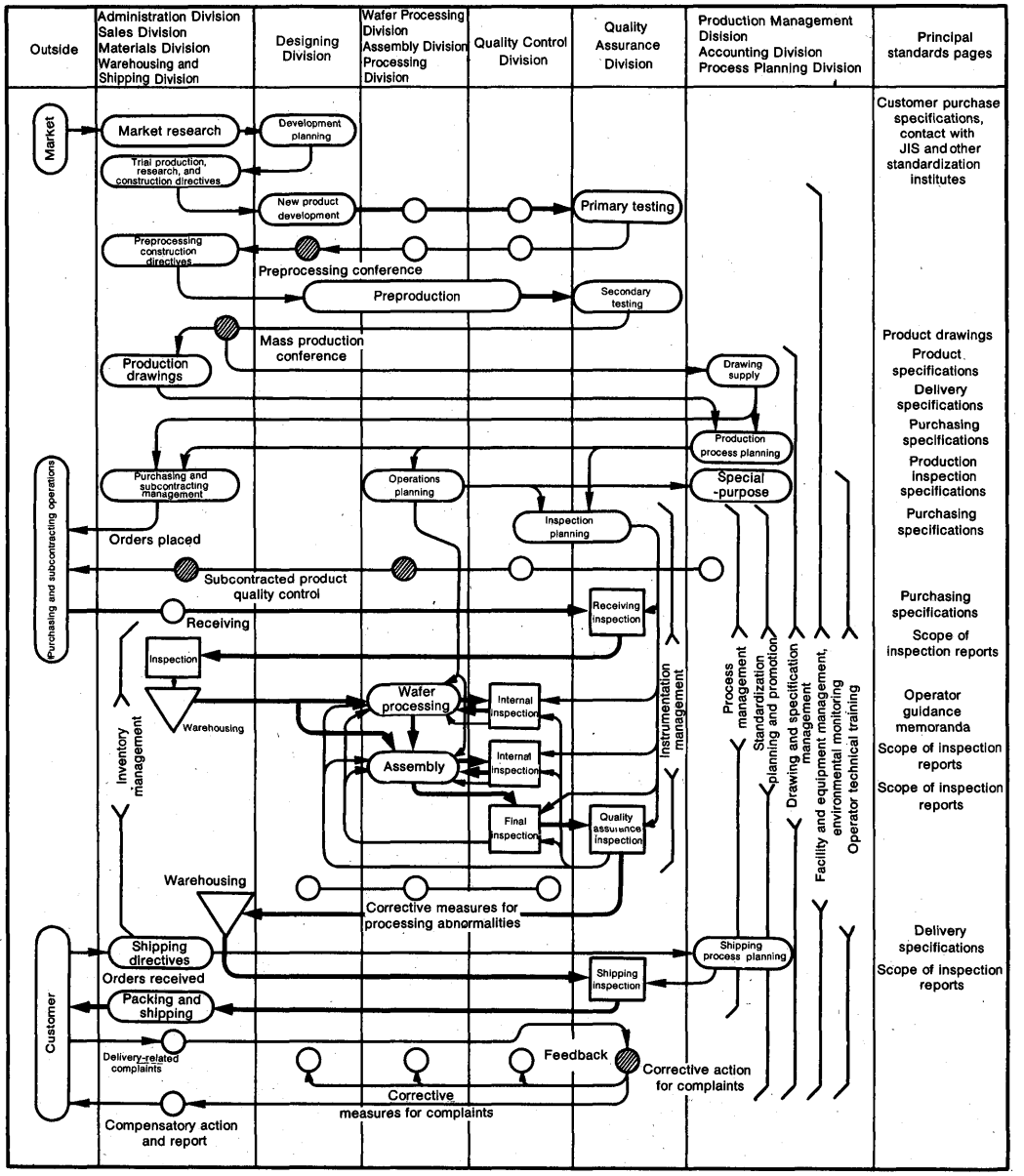


Fig.1 The Quality-Assurance System

Main divisions
Peripheral divisions
Flow of materials,, components and production
Flow of information

MITSUBISHI ELECTRIC

THE MITSUBISHI QUALITY-ASSURANCE SYSTEM AND DEVICE RELIABILITY DATA

2-1 Design Quality Assurance

Quality is maintained through use of two methods:

(1) Breadboard test circuits are configured from ICs and other standard components, and the characteristics and quality are evaluated.

(2) Circuit and device design are perfomed using CAD technology and systematic documented design standards.

2-2 Production Quality Assurance

Quality is maintained by the following management and inspection operations:

(1) Environmental management

(2) Regular and systematic inspection and maintenance of the design, tools, and instrumentation.

(3) Purchased materials quality management

(4) In-process management

(5) Internal inspections performed during wafer processing and assembly

(6) Final pass/fail inspections of finished product appearance, dimensions, construction, and electrical characteristics

(7) Final quality assurance inspection performed from the customer standpoint. This inspection assesses the overall product quality and approves the products for warehousing.

Per Lot Inspection: Visual, labeling, and electrical characteristics.

Regular Inspection: Devices are periodically drawn from passed lots for reliability tests including environmental tests and mechanical durability tests, and aging tests. This inspection is perfomed once in several months.

2-3 Reliability Evaluation from Developement Testing through Mass Production

To verify device reliability as described in sections 2-1 and 2-2, evaluations are performed during trial production, preproduction and mass production stages.

Only when the device passes the primary tests during trial production does it move into preproduction and secondary testing. The preproduction stage involves higher production volumes, and the secondary tests confirm that the quality and reliability verified in the primary testing are maintained. Quality-assurance inspections are also conducted during mass production to ensure continuing quality and reliability.

3. Reliability Tests

3-1 Methods of Determining and Ensuring Reliability

The reliability of high-speed CMOS ICs is evaluated in the following manner:

(1) The basic operation of the circuits is checked at the transistor and cell level using breadboarded circuits. These measurements are used to determine the basic reliability of the wafer process and the design.

(2) A simple block circuit is evaluated.

(3) The products are evaluated as the intergration scale is raised successively to ensure overall reliability. Fig. 2 shows the elements of these processes.

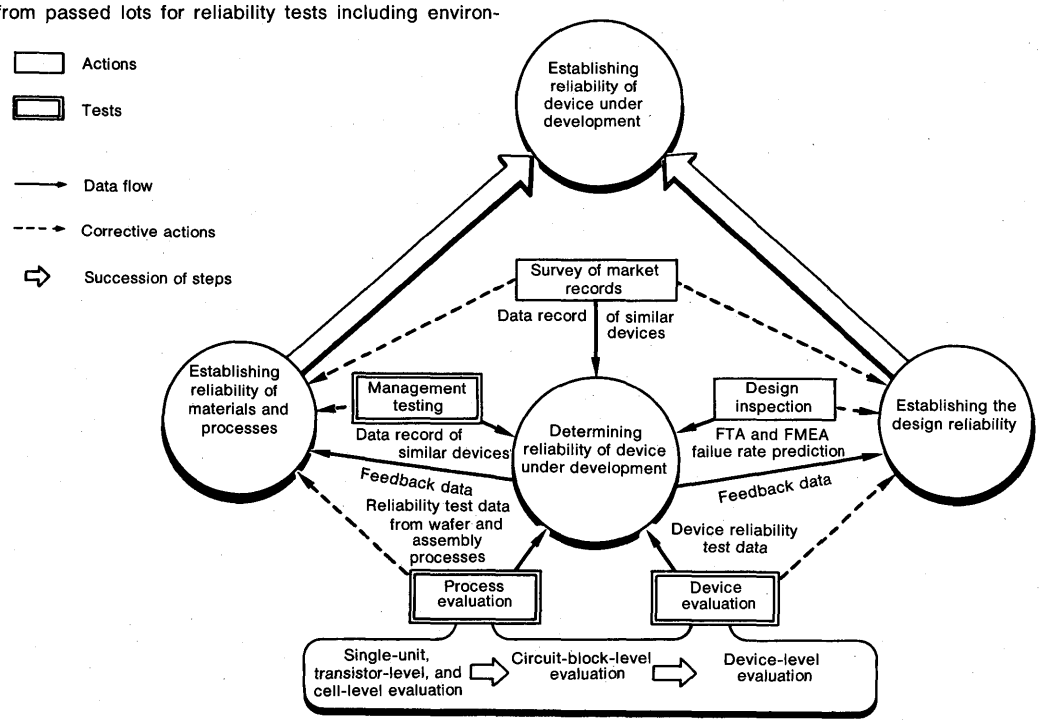


Fig.2 Methods of Determining and Ensuring Reliability

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3-2 Test Items and Conditions

Table 1 Reliability Test Items and Conditions for the M74HC00P Series

Test item		Conditions	Measured parameters
Solderability test		Wetted with rosin-base flux and immersed up to stoppers for 5sec in 230℃ solder bath.	Visual inspection
Thermal stress	Soldering reliability test	260℃, 10sec	Electrical characteristics
	Thermal shock test	−40~125℃, 15cycles, 10min/cycle	
	Temperature cycle test	−65~150℃, 1 hr/cycle	
Lead strength test		250g, 90°, bent three times	Visual inspection
Mechanical stress	Shock test	1500G, 0.5msec, 3times each along X, Y, and Z axes	Electrical characteristics
	Natural drop test	75cm to a wooden board, Y^1 direction, 3times	
	Vibration test	20G, 100~2000Hz, 4times each along X, Y, and Z axes	
	Constant acceration test	20000G, Y direction, 1min	
High-temperature operation life test		T_a=85℃, 125℃, 150℃ V_{CC}=6V, 8.5V	Electrical characteristics
High-temperature storage life test		T_a=150℃	Electrical characteristics
Humidity resistance	High-temperature high-humidity storage test	85℃, 85%RH	Electrical characteristics
	High-temperature high-humidity bias test	85℃, 85%RH V_{CC}=6V	
	Pressure-cooker test (saturated)	121℃, 2atm, 100%	
	Pressure-cooker test (unsaturated)	130℃, 85%RH, V_{CC}=6V	

Table 2 Reliability Test Items and Conditions for the M74HC00FP Series

Test item	Conditions	Measured parameters
Solderbility test	Wetted with rosin-base flux and immersed up to stoppers for 5sec in 230℃ solder bath.	Visual inspection
Soldering thermal stress test (1)	Entire surface immersed in solder (260℃, 10sec, 3times) ⇩ High-temperature, high-humidity bias test (85℃, 85%RH, V_{CC}=6V, 1000hr)	Electrical characteristics
Soldering thermal stress test (2)	Entire surface immersed in solder (260℃, 10sec, 3times) ⇩ Pressure-cooker test (121℃, 2atm, 240hr)	Electrical characteristics
Soldering thermal stress test (3)	High-temperature high-humidity storage (85℃, 85%RH, 24hr) ⇩ Entire surface immersed in solder (260℃, 10sec, 3times) ⇩ High-temperature, high-humidity bias test (85℃, 85%RH, V_{CC}=6V, 1000hr)	Electrical characteristics
Thermal stress test	Entire surface immersed in solder (260℃, 10sec, 3times) ⇩ Thermal shock test (−40~+125℃, 15cycles) ⇩ Temperature cycle test (−65~+150℃, 500cycles)	Electrical characteristics
High-temperature, high-humidity bias test	85℃, 85%RH, V_{CC}=6.0V, 1000hr	Electrical characteristics
Pressure-cooker test (saturated)	121℃, 2atm, 240hr	Electrical characteristics
Pressure-cooker test (unsaturated)	130℃, 85%RH, V_{CC}=6.0V, 1000hr	Electrical characteristics
Lead strength test	250g, 90°, bent three times	Visual inspection
High-temperature operation life test	T_a=125℃, V_{CC}=6.0V, 1000hr	Electrical characteristics
High-temperature storage life test	T_a=150℃, 1000hr	Electrical characteristics

3-3 Deveice Failure Cirteria

(1) Electrical Characteristics

Table 3 Device Failure Criteria

Parameter	Failure points		Unit
	Lower	Upper	
High-level output voltage (V_{OH})	LX0.9	—	V
Low-level output voltage (V_{OL})	—	UX1.1	V
High-level output current (I_{OH})	LX0.8	—	mA
Low-level output current (I_{OL})	LX0.8	—	mA
High-level input voltage (V_{IH})	LX0.8	—	V
Low-level input voltage (V_{IL})	—	UX1.2	V
Input current (I_I)	—	UX2.0	μA
Quiescent supply current (I_{CC})	—	UX2.0	μA
Functional fault	Short, open, misoperation		—

L : Lower limit U : Upper limit

(2) Solderability

Solder adheres to less than 95% of the wetted area.

(3) Terminal Strength

Lead separation or damage is observed.

3-4 Results of Reliability Tests

Table 4 shows the results of reliability tests on M74HC00P series DIP devices, and Table 5 those of M74HC00FP SOP devices.

(1) High-Temperature Operation Tests

Tests were conducted under the following conditions: V_{CC}=6, 8.5V (6V only for SOPs), and T_a=85, 125, 150℃ (125℃ only for SOPs). Table 6 shows the failure ratios based on this data. At T_a=25℃, the statistical failure ratio is 0.0012% /1,000hr (1.2FIT), and at T_a=55℃, it is 0.001%/1,000hr (10FIT).

(2) High-Temperature Storage Test

Devices were stored for 2,000 hours (1,000 for SOPs) without any failures.

(3) Humidity Tests

Test items included 2,000 hours of high-temperature, high-humidity storage, 2,000 hours of high-temperatrue, high-humidity bias (1,000hr for SOPs), and 240 hours each of saturated and unsaturated pressure-cooker tests. No devices failed, indicating that no humidity-related application problems will develop.

(4) Soldering Termal Stress Test

The results show that the heat stress problems generally associated with surface-mounted SOPs have been solved.

(5) Solderability, Thermal Stress, Mechanical Stress, and Terminal Strength Tests

No devices failed during any of these tests. Table 7 shows the results of reliability tests performed on samples drawn from lots at periodic intervales.

(6) Electro-Static Discharge Test

Table 8 shows the results of a electro-static discharge test performed using the capacitor charging method (Mil. Std. 883-C, Method 3015, C=100pF, R=1.5kΩ) Fig.3 shows the test circuit.

M74HC series employ thinner gate oxide layers and use finer patterns than those of M4000B series. This render M74HC series highly vulnerable to static destruction. This potential drawback has been overcome through improved layout and I/O protection circuit design. All pins of all devices can withstand at least ±3kV.

(7) Latchup Resistance Test

Although static electricity would readily cause latchup in previous CMOS devices, the pattern layout and I/O protection of Mitsubishi M74HC series high-speed CMOS devices has eliminated this source of latchup.

In-house checks of latchup resistance were performed using the capacitor-charging and current-injection methods, and in no case did a device fail due to latchup. Instead, the breakdown characteristics were the limiting factor.

Table 9 shows the results determined by the capacitor charging method (Fig.4) based on C=200pF and R=0Ω. The latchup resistance was evaluated at inputs, outputs and V_{CC}.

Fig.10 shows the latchup resistance determined using the current-injection method at the input and output pins. Trigger currnets were typically near ±300mA, indicating extermely high latchup resistance.

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Table 4 Results of Reliability Tests on the M74HC00P Series

Test item		Conditions	Qty	Failures
Solderability test		Wetted with rosin-base flux and immersed up to stoppers for 5sec in 230℃ solder bath.	264	0
Thermal stress	Soldering reliability test	260℃, 10sec	836	0
	Thermal shock test	−40~125℃, 15cycles, 10min/cycle	836	0
	Temperature cycle test	−65~150℃, 1 hr/cycle	836	0
Mechanical stress	Shock test	1500G, 0.5msec, 3times each along X, Y, and Z axes	132	0
	Natural drop test	75cm to a wooden board, Y^1 direction, 3times	132	0
	Vibration test	20G, 100~2000Hz, 4times each along X, Y, and Z axes	132	0
	Constant acceration test	2000G, Y direction, 1min	132	0
Lead strength test		250g, 90°, bent three times	198	0
High-temperature operation life test (1)		85℃, V_{CC}=6V, 2000hr	560	0
High-temperature operation life test (2)		85℃, V_{CC}=8.5V, 2000hr	376	0
High-temperature operation life test (3)		125℃, V_{CC}=6V, 2000hr	298	0
High-temperature operation life test (4)		125℃, V_{CC}=8.5V, 2000hr	146	1(I_{CC} over)
High-temperature operation life test (5)		150℃, V_{CC}=6V, 1000hr	158	0
High-temperature storage life test		150℃, 2000hr	220	0
Humidity resistance	High-temperature high-humidity storage test	85℃, 85%RH, 2000hr	308	0
	High-temperature high-humidity bias test	85℃, 85%RH, V_{CC}=6V 2000hr	452	0
	Pressure-cooker test (saturated)	121℃, 2atm, 240hr	439	0
	Pressure-cooker test (unsaturated)	130℃, 85%RH, V_{CC}=6V, 500hr	302	0

Table 5 Results of Reliability Tests on the M74HC00FP Series

Test item	Conditions	Qty	Failures
Solderbility test	Wetted with rosin-base flux and immersed up to stoppers for 5sec in 230℃ solder bath.	110	0
Soldering thermal stress test (1)	Entire surface immersed in solder (260℃, 10sec, 3times) ⇩ High-temperature, high-humidity bias test (85℃, 85%RH, V_{CC}=6V, 1000hr)	110	0
Soldering thermal stress test (2)	Entire surface immersed in solder (260℃, 10sec, 3times) ⇩ Pressure-cooker test (121℃, 2atm, 240hr)	110	0
Soldering thermal stress test (3)	High-temperature high-humidity storage (85℃, 85%RH, 24hr) ⇩ Entire surface immersed in solder (260℃, 10sec, 3times) ⇩ High-temperature, high-humidity bias test (85℃, 85%RH, V_{CC}=6V, 1000hr)	110	0
Thermal stress test	Entire surface immersed in solder (260℃, 10sec, 3times) ⇩ Thermal shock test (−40~+125℃, 15cycles) ⇩ Temperature cycle test (−65~+150℃, 500cycles)	110	0
High-temperature, high-humidity bias test	85℃, 85%RH, V_{CC}=6.0V, 1000hr	110	0
Pressure-cooker test (saturated)	121℃, 2atm, 240hr	110	0
Pressure-cooker test (unsaturated)	130℃, 85%RH, V_{CC}=6.0V, 1000hr	110	0
Lead strength test	250g, 90°, bent three times	75	0
High-temperature operation life test	T_a=125℃, V_{CC}=6.0V, 1000hr	190	0
High-temperature storage life test	T_a=150℃, 1000hr	110	0

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Table 6 High-Temperature Operation Test Data and Probable Failure Ratio

Test conditions	Test results	Failure ratio (FIT)			Remarks
		25℃	40℃	55℃	
85℃, V_{CC}=6~8.5V, 2000hr	0/936	1.2	3.5	10	Activation energy : 0.6eV
125℃, V_{CC}=6~8.5V, 2000hr	1/444				
125℃, V_{CC}=6V, 1000hr	0/1368				
125℃, V_{CC}=6V, 3000~5000hr	0/328				
150℃, V_{CC}=6V, 1000hr	0/158				

Table 7 Results of Tests on Periodic Sampling (M74HC00P Series)

Test item		Test Conditions	Qty	Failure ratio (FIT)				Remarks
				96H	240H	500H	1000H	
High-temperature operation life test		125℃ V_{CC}=6V	1368	0	0	0	0	
High-temperature storage life test		150℃	792	0	0	0	0	
Humidity resistance	High-temperature high-humidity bias test	85℃, 85%RH V_{CC}=6V	912	0	0	0	0	
	Pressure-cooker test (saturated)	121℃, 2atm, 100%	1824	0	0	0	3*	* 1 : Al corrosion 2 : I_{CC} over
	Pressure-cooker test (unsaturated)	130℃, 85%RH V_{CC}=6V	1053	0	0	0	—	
Temperature cycle test (1)		−65~+150℃, 1hr/cycle, 100 cycles	1824	0				
Temperature cycle test (2)		−65~+150℃, 1hr/cycle, 1,000 cycles	528	0				
Solderability test		Wetted with rosin-base flux and immersed up to stoppers for 5sec in 230℃ solder bath.	1056	0				

Table 8 Results of Electro-Static Discharge Test

Type	Test pin	Polarity	Qty	Breakdown voltage		
				1kV	2kV	3kV
M74HC20P	Input	±	5			➡
	Output	±	5			➡
M74HC32P	Input	±	5			➡
	Output	±	5			➡
M74HC42P	Input	±	5			➡
	Output	±	5			➡
M74HC160P	Input	±	5			➡
	Output	±	5			➡
M74HC164P	Input	±	5			➡
	Output	±	5			➡

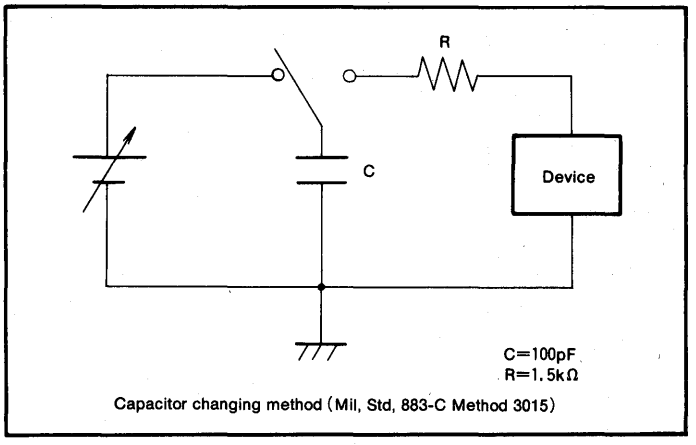

Fig.3 Breakdown voltage test circuit

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Table 9 Results of Latchup Resistance Tests Using the Capacitor Charge Method

Type	Test pin	Polarity	Qty	Test results
M74HC20P	Input	±	5	No latchup
	Output	±	5	〃
	V_{CC}	±	5	〃
M74HC32P	Input	±	5	No latchup
	Output	±	5	〃
	V_{CC}	±	5	〃
M74HC42P	Input	±	5	No latchup
	Output	±	5	〃
	V_{CC}	+	5	〃
M74HC160P	Input	±	5	No latchup
	Output	±	5	〃
	V_{CC}	±	5	〃
M74HC164P	Input	±	5	No latchup
	Output	±	5	〃
	V_{CC}	±	5	〃

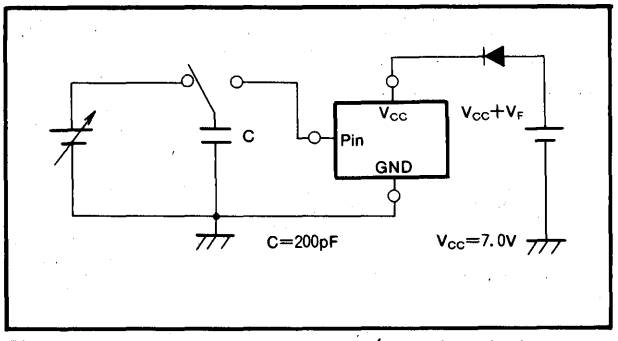


Fig.4 Latchup resistance test circuit (capacitor charing method)

Table 10 Results of Latchup Resistance Tests Using the Current Injection Method

Type	Qty	Input		Output	
		+	−	+	−
M74HC20P	5	>300mA	<−300mA	>300mA	<−300mA
M74HC32P	5	〃	〃	〃	〃
M74HC42P	5	〃	〃	〃	〃
M74HC160P	5	〃	〃	〃	〃
M74HC164P	5	〃	〃	〃	〃

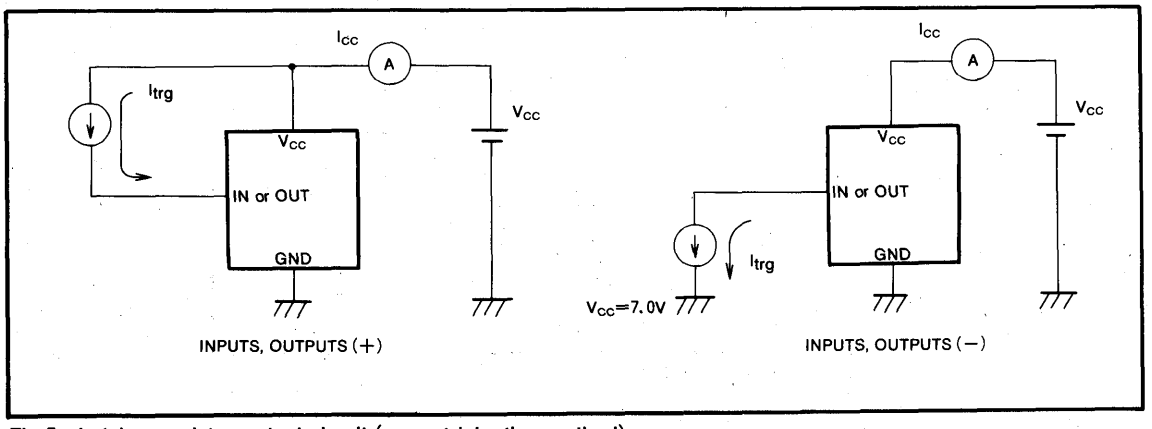


Fig.5 Latchup resistance test circuit (current-injection method)

1. Introduction

The low power dissipation, high noise margin, and wide supply-voltage and operating temperature ranges of high-speed CMOS devices makes them suitable for digital applications in a wide range of industrial and consumer digital equipment. CMOS circuits differ substantially from bipolar logic such as TTL and LSTTL, and therefore require special care.

2. Handling Unused Pins

Unlike bipolar logic, high-speed CMOS logic involves voltage control: input voltages are applied to transistor gates, and these voltage levels determine whether the transistors are on or off. If CMOS input pins are left floating, the output logic level will fluctuate, and erroneous operation may result. Therefore, all unused input pins should be tied to either V_{CC} or GND as described below:

(1) NAND and AND Gates
Tie unused inputs to V_{CC} or other inputs that are in use.

(2) NOR and OR Gates
Tie unused inputs to GND or other inputs that are in use.

(3) Other Types of Circuits
Tie other unused inputs to either V_{CC} or GND. Check the function tables in the individual device data sheets to determine the appropriate level.

If and entire functional block is to be left unused, the input pins should be linked to V_{CC} or GND. Otherwise, I_{CC} may increase unpredicatably.

3. AND Ties

As with TTL and LSTTL, the impedance of both low- and high-level outputs of high-speed CMOS logic is low. This means that if output pins of differing states are linked together in "AND" ties, logic outputs will deviate from standard levels, risking misoperation, higher sink currents, and imparied reliability.

4. Output Load Capacitance

In many high-speed CMOS applications, capacitors are connected between I/O pins and either V_{CC} or GND to increase the propagation delay and to remove signal noises. Capacitors of up to 500pF can be connected directly. Larger capacacitors should be linked through a resistor to keep the charging or discharging currents within 20mA. This design will prevent large currents that could cause latchup during power-supply switching or impair reliability.

5. Shorting of Output to V_{CC} or GND

The p- and n-channel transistors used in CMOS logic do not have output-current limiting. If output pins are accidentally shorted to V_{CC} or GND, excessive currents will flow. For example, when an output pin of buffer IC such as M74HC240 is connected to GND, about 100mA current flows. When the output is tied to V_{CC}, about 80mA current flows. These currents may cause latchup, overheating, damage to the IC's internal wiring, and loss of reliability. Therefore, output pins should never be tied to V_{CC}, GND, or any other fixed voltage level.

6. Power Supply Lines

When high-speed CMOS logic is quiescent, the supply current is extermely small. This would seem to indicate that the power-supply capacitance could also be low; however, when CMOS logic changes state, large transient current spikes flow, just as in TTL and LSTTL devices. To soak up such spikes, the impedances of both the power supply and the supply lines must be low. One method to lower this supply-line impedance is to connect a $0.01 \sim 0.22 \mu F$ plastic-film or ceramic capacitor with good high-frequency characteristics between the V_{CC} and GND lines. $10 \sim 100 \mu F$ electrolytic or tantalum capacitors should also be connected on each printed-circuit board.

The power dissipation current varies widely with the operating frequency, supply voltage, capacitive load, supply voltage, and input signal rise and fall times. The effect of this factors should be considered when designing the power supply.

When CMOS devices are being used with high-current drivers, separate power supplies should be used for the logic and driver circuit, and common loads should be avoided.

7. Preventing Damage by Static Electricity

Static electricity is generated under low-humidity conditions by the friction of clothing, containers and other objects. Most MOS ICs are easily damaged by high-voltage static-electric discharges, but through use of protective circuits Mitshbishi high-speed CMOS devices can tolerate static voltages of over 3kV. This places them on equal footing with TTL and LSTTL devices.

The protection diodes that prevent static damage can to tolerated only limited forward- and reverse-bias currents. Large energy inputs should be avoided, as they will destroy there diodes and thin oxide layers at the transistor input gates. The following measures are recommended to prevent this type of damage.

(1) To prevent static damage during shipping, all ICs are shipped in conductive tubes. After receipt, the ICs should always be stored in conductive tubes or other conductive containers.

(2) Static charges on the body or clothing should be drained off by grounding through $100k\Omega \sim 1M\Omega$ resistors.

(3) All assembly tables, insertion machines, and measuring instruments, and other objects that will come in contact with the ICs should be grounded.

(4) Soldering irons and baths must have power-supply insulation resistances of over 10MΩ to prevent power-supply leakage to the ICs. This equipment should also be grounded.
(5) Printed-circuit boards with ICs installed should be protected from shock, vibration, and friction. To keep potentials from building up, the boards should stored in conductive envelopes, or the terminals should be shorted together.
(6) The humidity of the transport, storage and assembly environments should always be maintained at safe levels.

8. Latchup

The CMOS circuit structure inherently cointains parasitic bipolar transistors. These transistors function as thyristors (SCRs): when they are triggered by an external surge, they turn on, causing a current to flow from V_{CC} to GND. Even after the trigger current ceases, this current continues to flow. The current is very large, and can easily damage or destroy the IC. For this reason, the phenomenon is called "latchup".

8-1 The Latchup Mechanism

Fig.1 shows the structure of a CMOS inverter and its parasitic bipolar transistors, and Fig.2 the thyristor circuit that results in latchup. T_{r1} and T_{r2} have pnpn thyristor structures. If any one of T_{r3}, T_{r4}, T_{r5}, or T_{r6} turn on due to a current surge, a base current will flow to T_{r1} or T_{r2}, initiating latchup.

The following external factors can initiate latchup:
(1) Input voltage (V_I) exceeds supply voltage (V_{CC}). $V_I > V_{CC}$
(2) Input voltage (V_I) falls below GND. $V_I < GND$
(3) Output voltage (V_O) exceeds supply voltage (V_{CC}). $V_O > V_{CC}$
(4) Output voltage (V_O) falls below GND. $V_O < GND$
(5) Supply voltage (V_{CC}) becomes excessive.

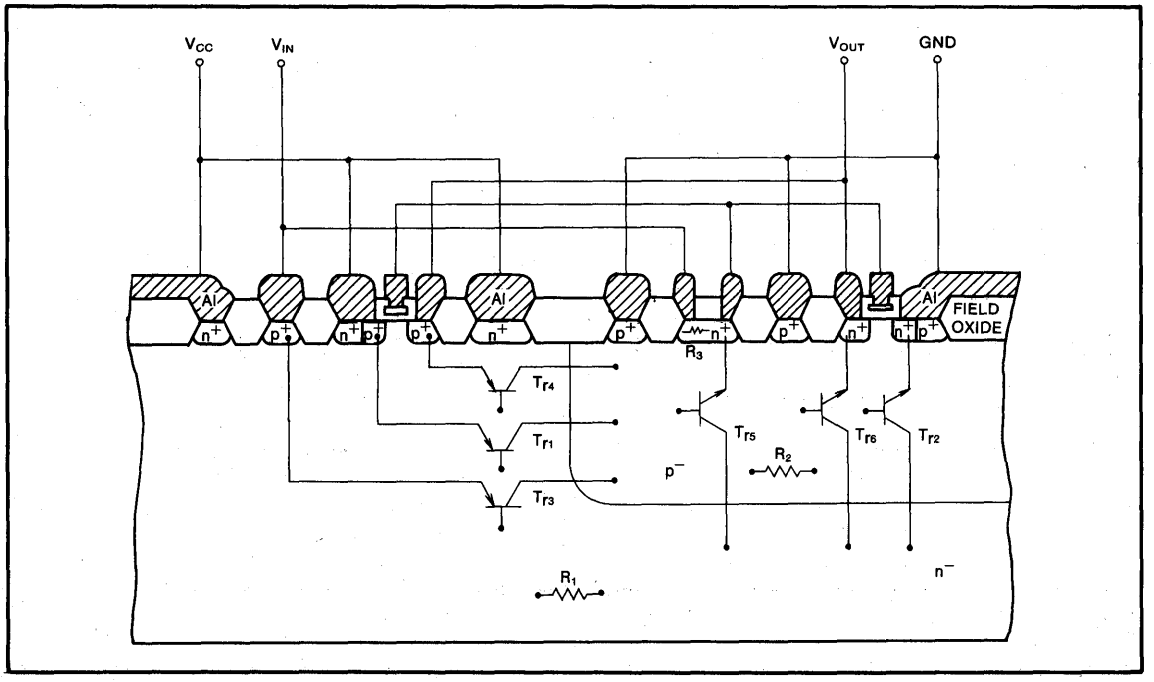


Fig.1 A CMOS inverter and its parasitic transistors

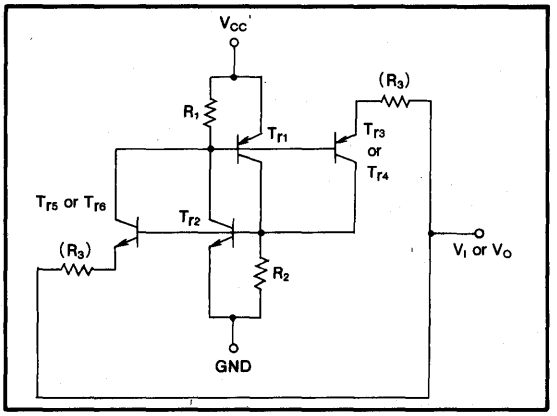


Fig.2 The parasitic transistor circuit that causes latchup

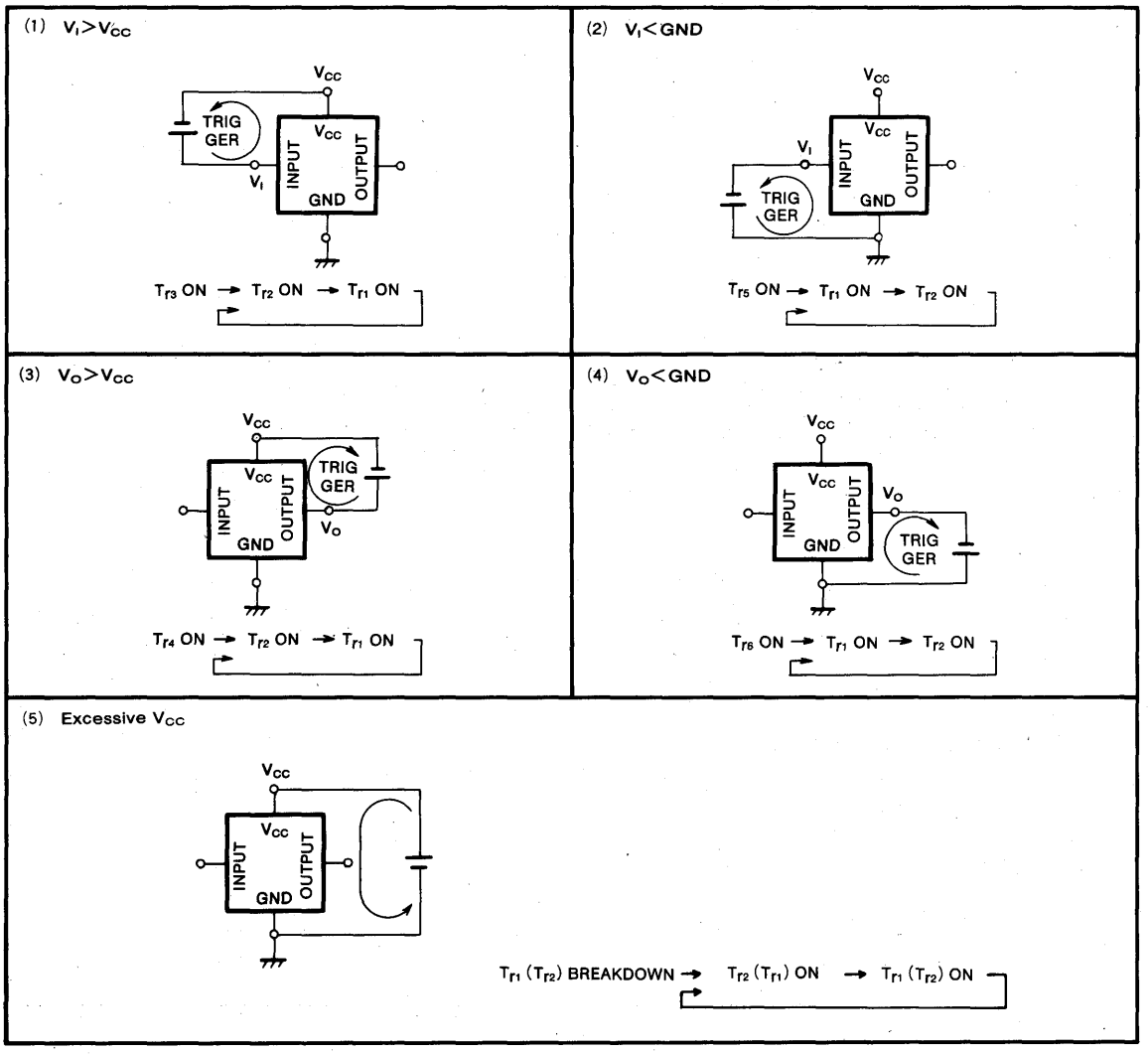


Fig.3 Latchup mechanisms Note : The recirculating arrow indicates latchup.

8-2 Prevention of Latchup

The following steps can be taken to prevent the five conditions listed in section 8-1 from arising.

(1) $V_I > V_{CC}$ and $V_I < GND$

● When using two power supplies

When two supplies are used to power CMOS devices, the differing rise times can readily cause latchup. This problem is avoided by connecting series resistor R to limit the maximum current to 20mA (Fig.4).

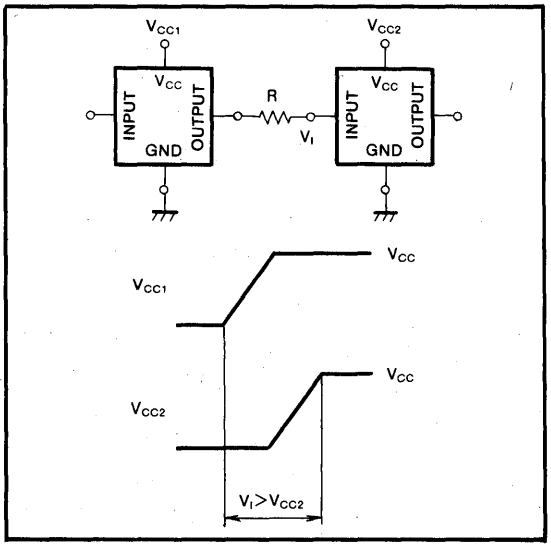


Fig.4 Preventing latchup when dual power supplies are used

● When using a differential circuit

When a differential circuit is used, the input voltage V_I may exceed V_{CC} or drop below GND, causing latchup. This danger is avoided by connecting voltage-clamp diodes and current-limiting resistors (Fig. 5).

9. Mechanical and Thermal Stress

Cutting or deforming the external leads can result in lead breakage or humidity-induced corrosion. Mechanical stress should be avoided when mounting the ICs.

The component materials of ICs have widely varying thermal-expansion coefficents, so rapid temperature changes, extended soldering and other thermal stresses should be avoided as far as possible. Such stresses can damage the semiconductors or break the internal wiring.

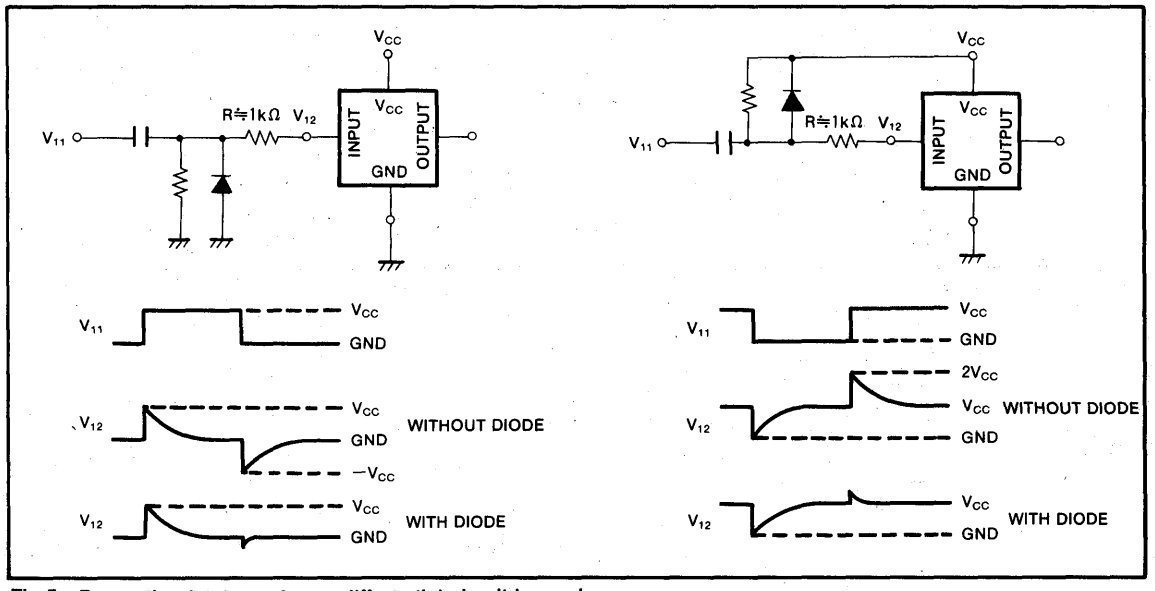
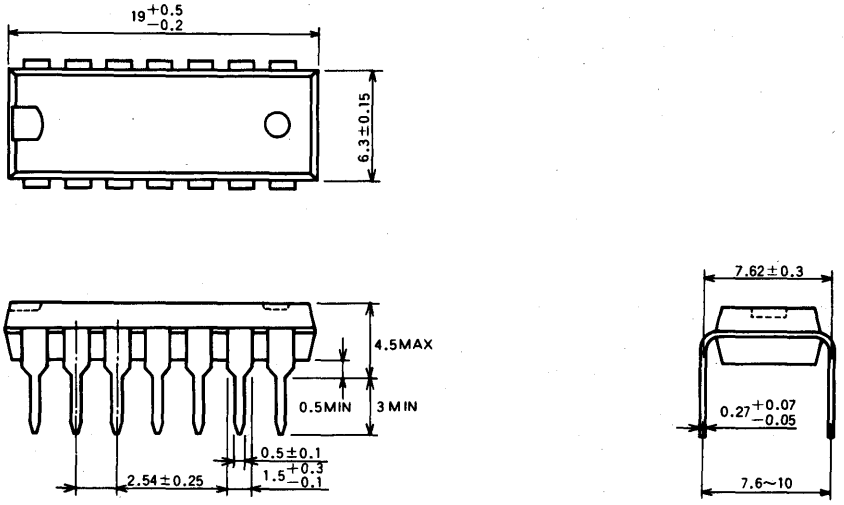


Fig.5 Preventing latchup when a differential circuit is used

PACKAGE OUTLINES

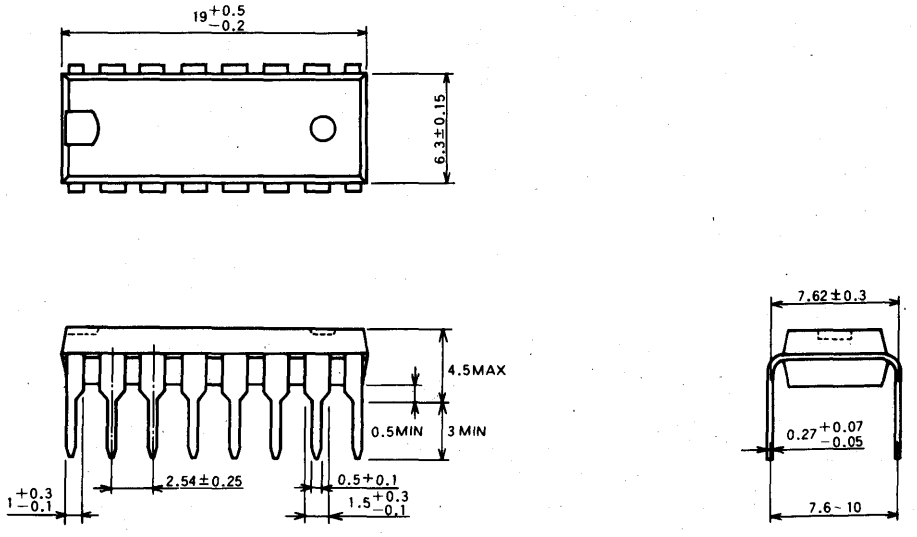
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

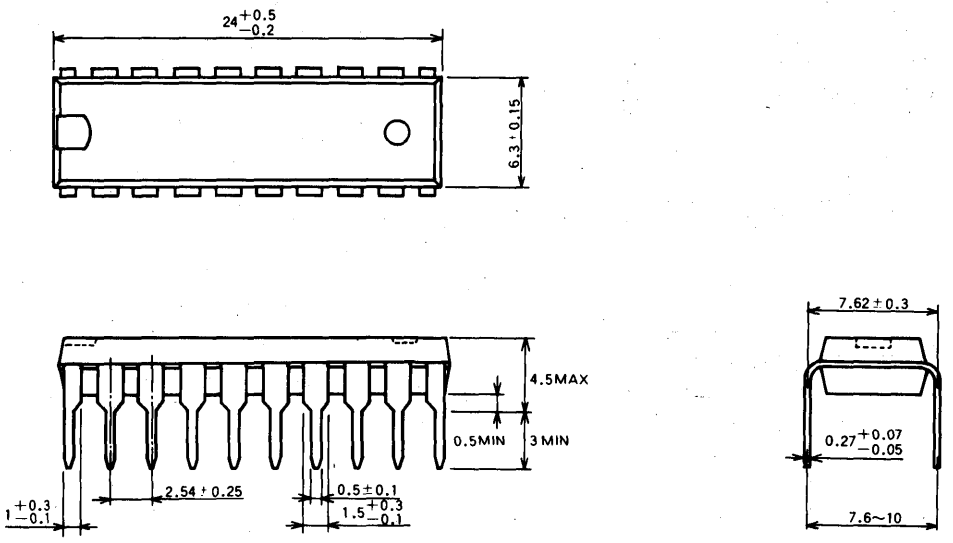
Dimension in mm



PACKAGE OUTLINES

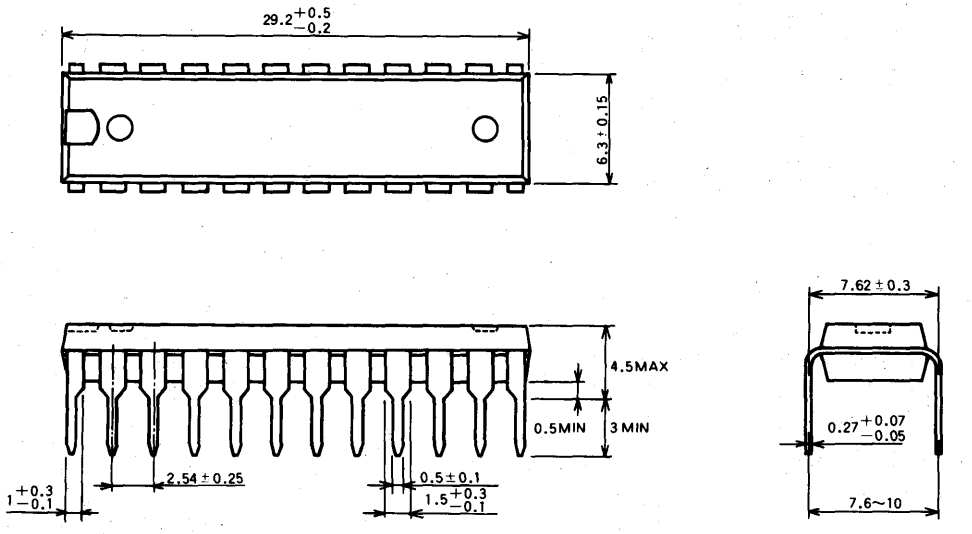
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm

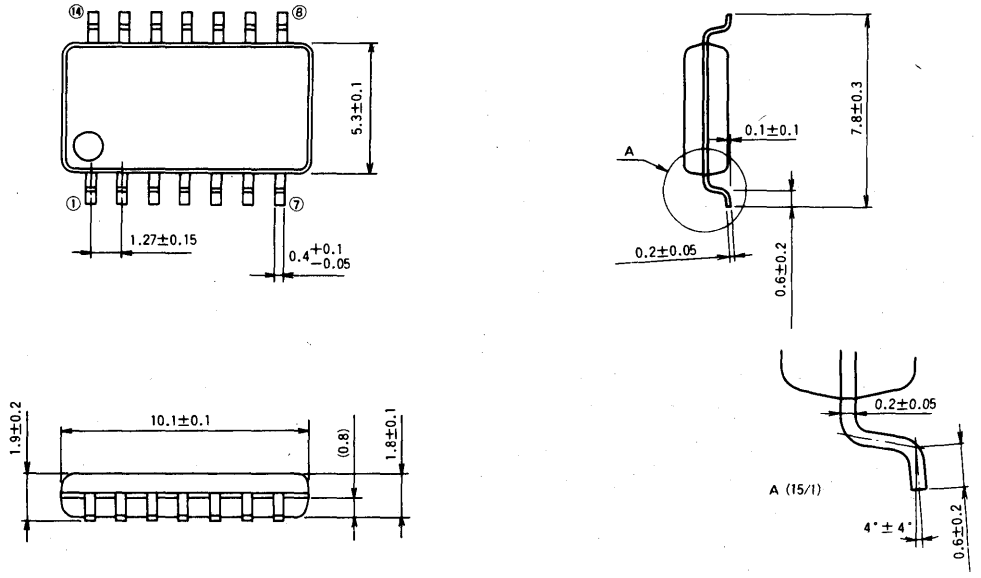


MITSUBISHI ELECTRIC

PACKAGE OUTLINES

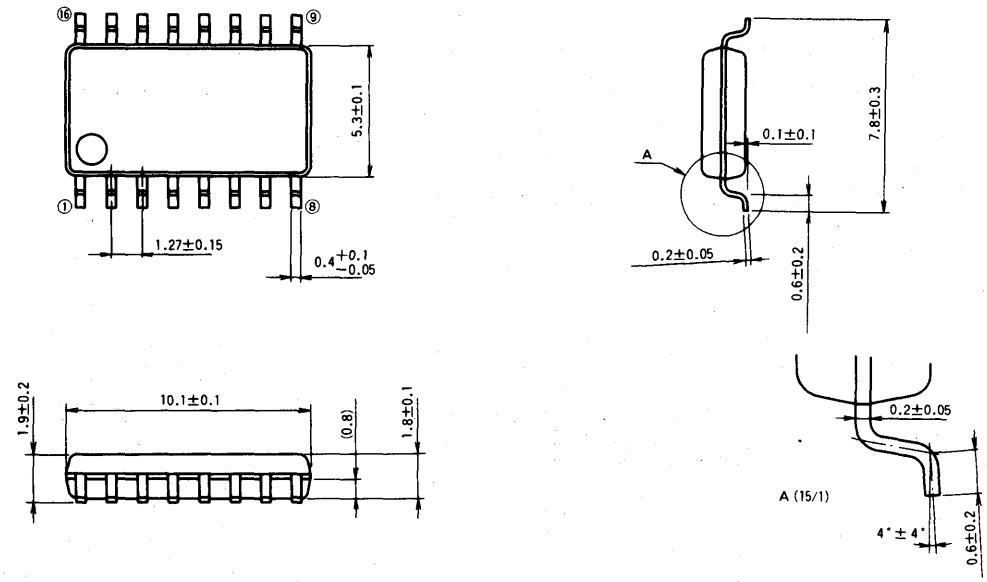
TYPE 14P2N 14PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 16P2N 16PIN MOLDED PLASTIC SOP

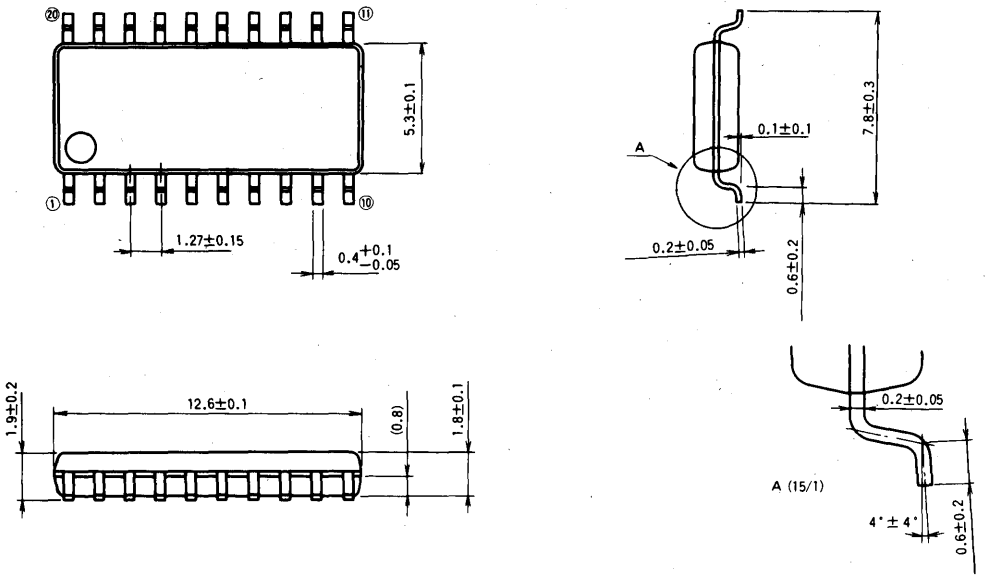
Dimension in mm



PACKAGE OUTLINES

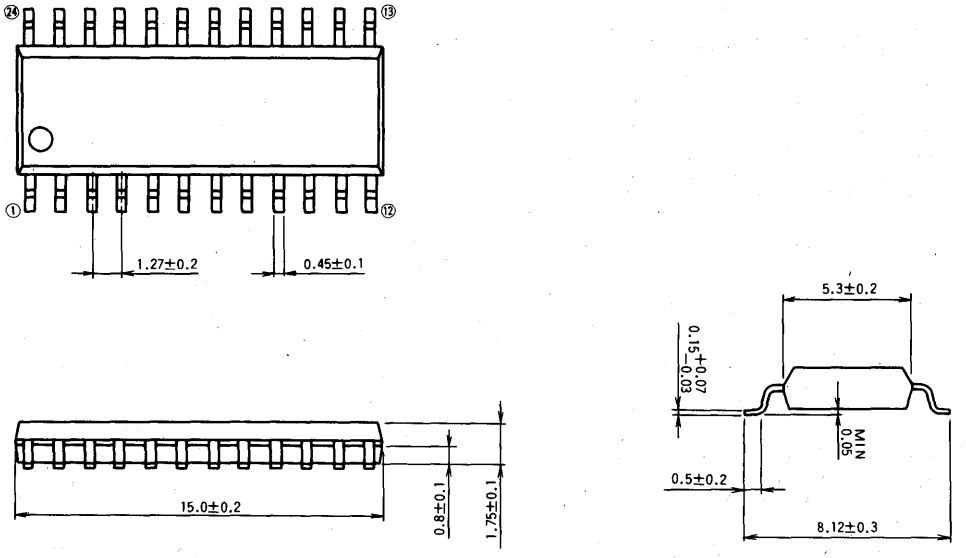
TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 24P2 24PIN MOLDED PLASTIC SOP

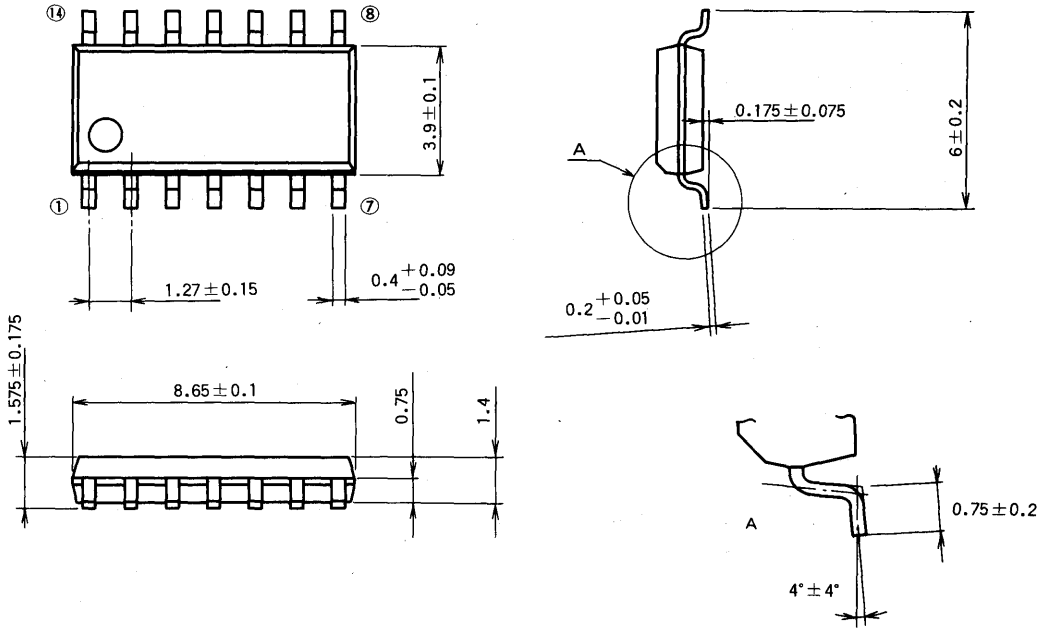
Dimension in mm



PACKAGE OUTLINES

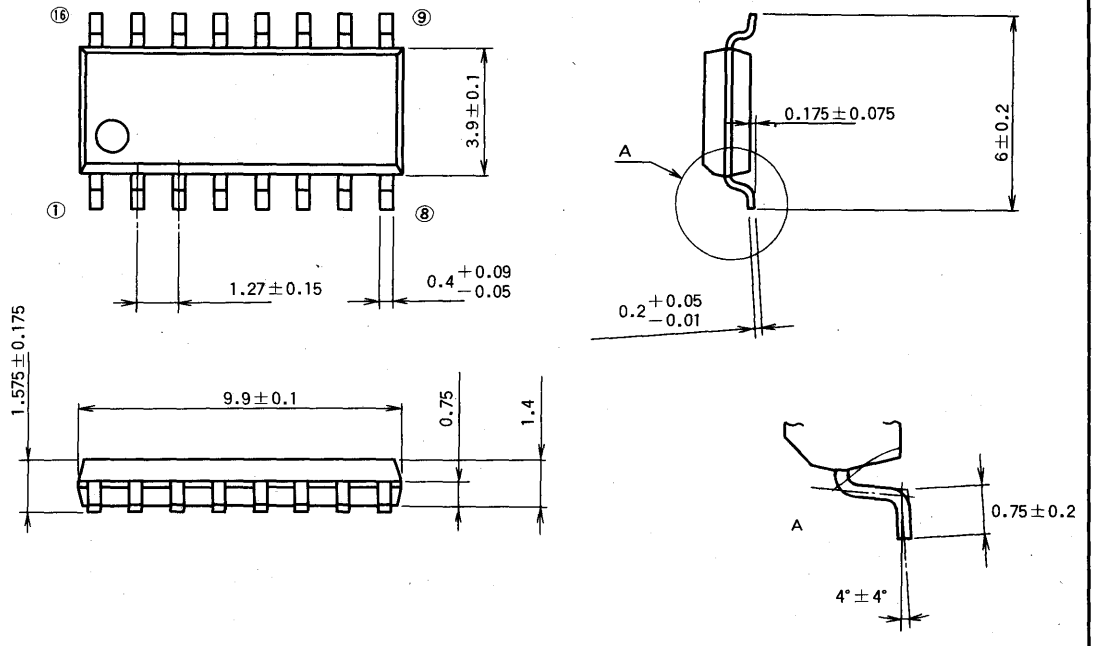
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

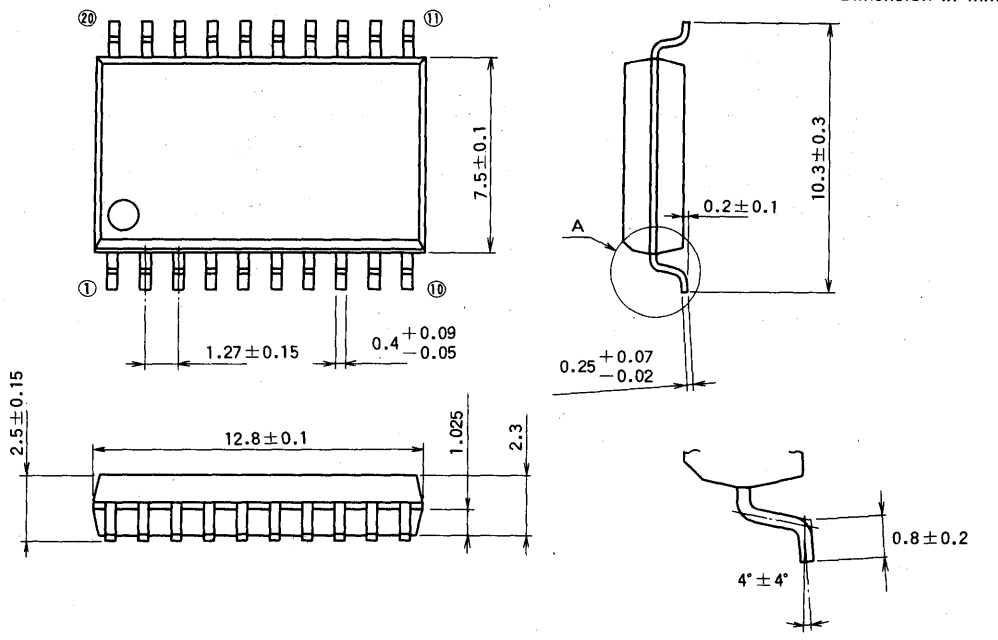
Dimension in mm



PACKAGE OUTLINES

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP(JEDEC 300mil body)

Dimension in mm



DATASHEETS 2

M74HC00P/FP/DP

QUADRUPLE 2-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC00 is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, Vcc=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC00 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS00.

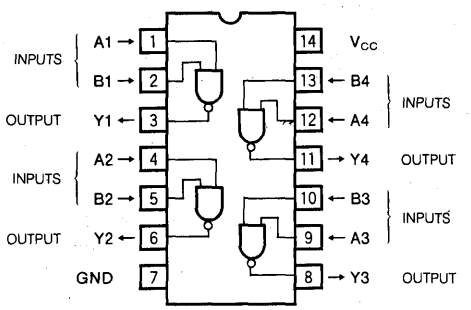
Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When both inputs A and B are high, the output Y will become low, and when at least one of the inputs is low, the output Y will become high.

FUNCTION TABLE

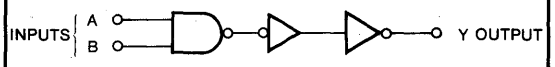
Inputs		Output
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

PIN CONFIGURATION (TOP VIEW)



14P4
Outline 14P2N
14P2P

LOGIC DIAGRAM (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC00FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC00DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

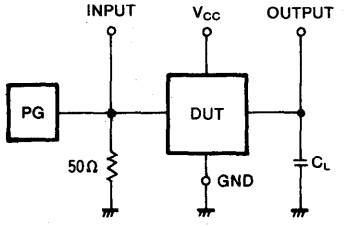
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			90		113	ns
			4.5			18		23	
			6.0			15		19	
t_{PHL}			2.0			90		113	
			4.5			18		23	
			6.0			15		19	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				25				pF

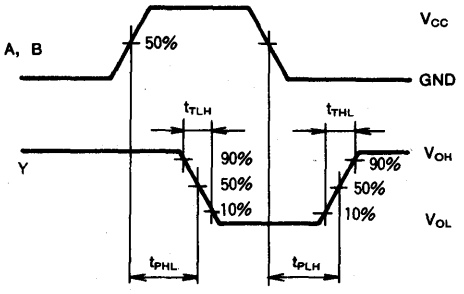
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HCT00P/FP/DP

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT00P is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- TTL level input V_{IL} = 0.8V max V_{IH} = 2.0V min
- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 10 74LSTTL loads
- Wide operating temperature range: T_a=−40∼+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT00 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS00.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

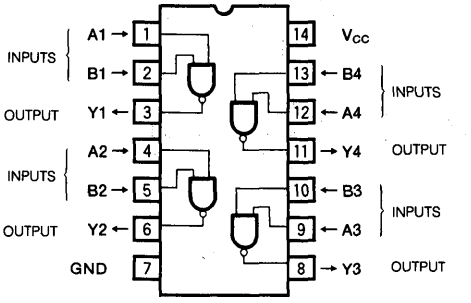
Buffered Y outputs improve input-to-output transfer characteristics and reduce output impedance variations to a minimum with respect to input voltage variations.

When both inputs A and B inputs are high, the output Y will become low, and when at least one of the inputs is low, the output Y will become high.

FUNCTION TABLE

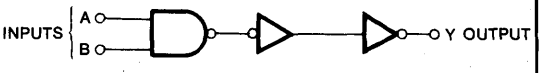
Inputs		Output
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

LOGIC DIAGRAM (EACH GATE)



QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 1 : M74HCT00FP, T_a = −40∼+60℃ and T_a = 60−85℃ are derated at −6mW/℃.
M74HCT00DP, T_a = −40∼+50℃ and T_a = 50−85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −4.0mA, V_{CC} = 4.5V	4.18			4.13		
			I_{OH} = −4.8mA, V_{CC} = 5.5V	5.18			5.13		
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 4.0mA, V_{CC} = 4.5V			0.26		0.33	
			I_{OL} = 4.8mA, V_{CC} = 5.5V			0.26		0.33	
I_{IH}	High-level input current	V_I = 5.5V				0.1		1.0	μA
I_{IL}	High-level input current	V_I = 0V				−0.1		−1.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				1.0		10.0	μA
$\triangle I_{CC}$	Maximum quiescent state supply current	V_I = 2.4V, 0.4V (Note 2)				2.7		2.9	mA

Note 2 : Only one input is set at this value and all others are fixed at V_{CC} or GND.

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

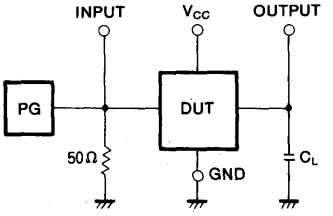
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40∼+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40∼+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			15		19	ns
t_{THL}					15		19	ns
t_{PLH}	Low-level to high-level and high-level to low level output propagation time				18		24	ns
t_{PHL}					18		24	ns
C_I	Input capacitance				10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)							pF

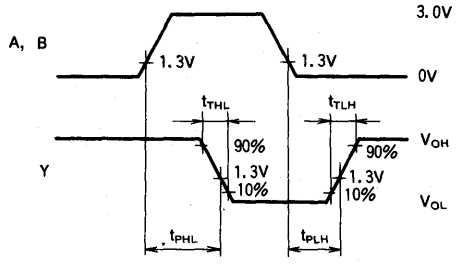
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%∼90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC02P/FP/DP

QUADRUPLE 2-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74HC02 is a semiconductor integrated circuit consisting of four 2-input positive-logic NOR gates, usable as negative-logic NAND gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, Vcc=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

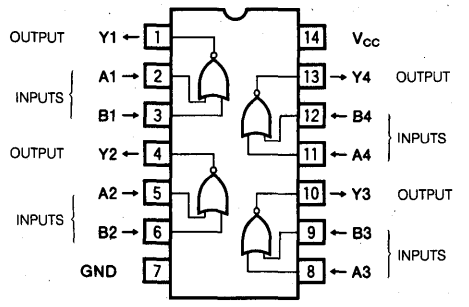
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC02 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS02.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

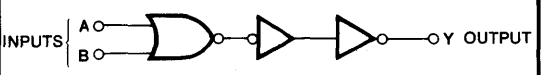
When both inputs A and B are low, the output Y will become high, and when at least one of the inputs is high, the output Y will become low.

PIN CONFIGURATION (TOP VIEW)



14P4
Outline 14P2N
14P2P

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
H	L	L
L	H	L
H	H	L

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC02FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC02DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating themperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, I_{OH} = −20μA	2.0	1.9			1.9		V
		I_{OH} = −20μA	4.5	4.4			4.4		
		I_{OH} = −20μA	6.0	5.9			5.9		
		I_{OH} = −4.0mA	4.5	4.18			4.13		
		I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	2.0			0.1		0.1	V
		I_{OL} = 20μA	4.5			0.1		0.1	
		I_{OL} = 20μA	6.0			0.1		0.1	
		I_{OL} = 4.0mA	4.5			0.26		0.33	
		I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

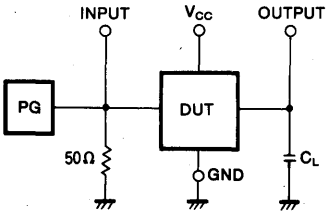
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			90		113	ns
			4.5			18		23	
			6.0			15		19	
t_{PHL}			2.0			90		113	ns
			4.5			18		23	
			6.0			15		19	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				31				pF

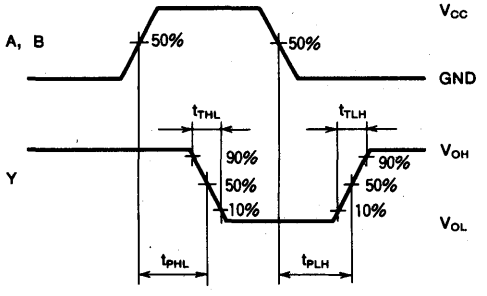
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC03P/FP/DP

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN-DRAIN OUTPUTS

DESCRIPTION

The M74HC03 is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND gates usable as negative-logic NOR gates, with open-drain outputs.

FEATURES

- Open-drain outputs
- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC03 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS03.

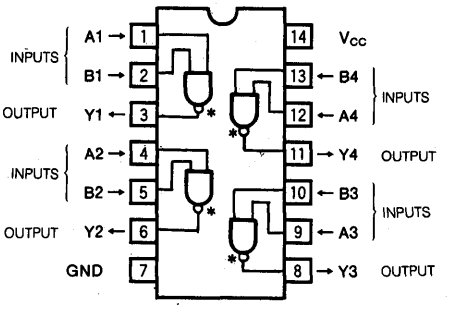
Open-drain outputs allow a versatile selection of high output impedances by connecting external load resistors. This enalbes "AND ties" which are not possible using normal gates. When both inputs A and B are high, the output Y will become low, and when at least one of the inputs is low, Y will become high.

Note that this IC differs from the 74LS03 and a voltage higher than V_{CC} can not be applied to the output.

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

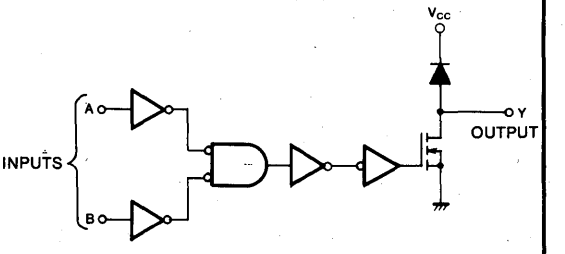
PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

* : Open-drain output

LOGIC DIAGRAM (EACH GATE)



QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN-DRAIN OUTPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 1 : M74HC03FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC03DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OL}	Low-level output voltage	V_I = V_{IH}, I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		V_I = V_{IH}, I_{OL} = 4.0mA	4.5			0.26		0.33	
		V_I = V_{IH}, I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_O	Maximum output leakage current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}	6.0			0.5		5.0	μA
		V_I = V_{IH}, V_{IL}, V_O = GND	6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			1.0		10.0	μA

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN-DRAIN OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

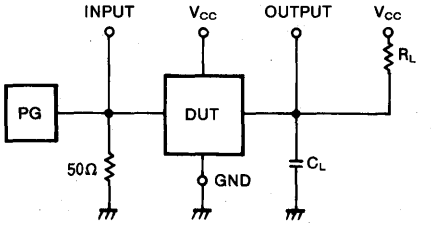
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{THL}	High-level to low-level output transition time	R_L = 1kΩ, C_L = 15pF (Note 3)			10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time	R_L = 1kΩ, C_L = 5pF (Note 3)			20	ns
t_{PHL}		R_L = 1kΩ, C_L = 15pF (Note 3)			20	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{THL}	High-level to low-level output transition time	R_L = 1kΩ, C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
C_I	Input capacitance					10		10	pF
C_O	Output capacitance	A or B = GND				10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				11				pF

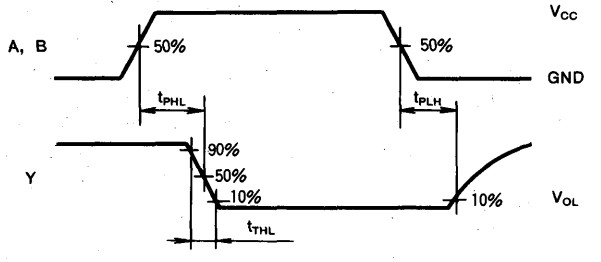
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC04P/FP/DP

HEX INVERTER

DESCRIPTION

The M74HC04 is a semiconductor integrated circuit consisting of six inverters.

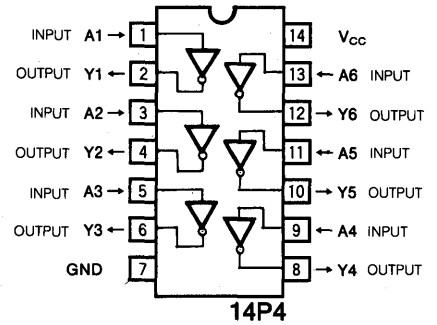
FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC04 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS04.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When input A is high, the output Y will become low, and when input A is low, the output Y will become high.

LOGIC DIAGRAM (EACH INVERTER)

FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC04FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC04DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
					25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

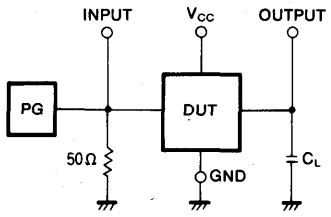
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				17	ns
t_{PHL}					17	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0		75		95	ns
			4.5		15		19	
			6.0		13		16	
t_{THL}			2.0		75		95	ns
			4.5		15		19	
			6.0		13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0		86		108	ns
			4.5		19		24	
			6.0		16		20	
t_{PHL}			2.0		86		108	ns
			4.5		19		24	
			6.0		16		20	
C_I	Input capacitance				10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)			26				pF

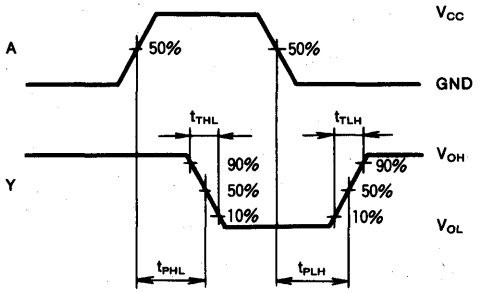
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per inverter)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HCU04P/FP/DP

HEX UNBUFFERED INVERTER

DESCRIPTION

The M74HCU04 is a semiconductor integrated circuit consisting of six unbuffered inverters.

FEATURES

- High-speed: 7ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

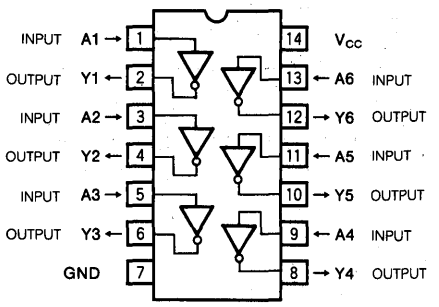
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCU04 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS04.

Unbuffered outputs Y make this device suitable for linear circuit applications such as oscillators and amplifier circuits as well as logic system applications. However, consideration must be given in linear circuit applications dissipated power is much greater than of the 4000B series.

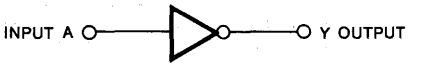
When input A is high, the output Y will become low, and when input A is low, the output Y will become high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

LOGIC DIAGRAM (EACH INVERTER)



FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HCU04FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HCU04DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature range	−40		+85	℃
t_r, t_f	Input risetime, falltime	No limit			ns

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.2V, $\|I_O\|$ = 20μA	2.0	1.7			1.7		V
		V_O = 0.5V, $\|I_O\|$ = 20μA	4.5	3.6			3.6		
		V_O = 0.5V, $\|I_O\|$ = 20μA	6.0	4.8			4.8		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.2V, $\|I_O\|$ = 20μA	2.0			0.3		0.3	V
		V_O = V_{CC}−0.5V, $\|I_O\|$ = 20μA	4.5			0.8		0.8	
		V_O = V_{CC}−0.5V, $\|I_O\|$ = 20μA	6.0			1.1		1.1	
V_{OH}	High-level output voltage	V_I = V_{IL}, I_{OH} = −20μA	2.0	1.8			1.8		V
			4.5	4.0			4.0		
			6.0	5.5			5.5		
		V_I = GND, I_{OH} = −4.0mA	4.5	3.98			3.84		
		V_I = GND, I_{OH} = −5.2mA	6.0	5.48			5.34		
V_{OL}	Low-level output voltage	V_I = V_{IH}, I_{OL} = 20μA	2.0			0.2		0.2	V
			4.5			0.5		0.5	
			6.0			0.5		0.5	
		V_I = V_{CC}, I_{OL} = 4.0mA	4.5			0.26		0.33	
		V_I = V_{CC}, I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

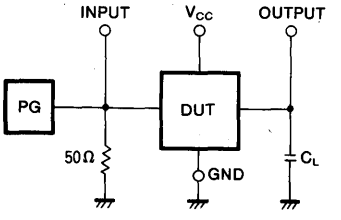
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level andhigh-level to low-level	C_L = 15pF (Note 3)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				13	ns
t_{PHL}	output propagation time				13	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			82		103	ns
			4.5			16		21	
			6.0			14		18	
t_{PHL}			2.0			82		103	ns
			4.5			16		21	
			6.0			14		18	
C_I	Input capacitance					15		15	pF
C_{PD}	Power dissipation capacitance (Note 2)				25				pF

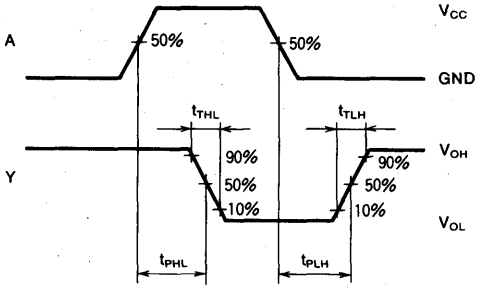
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per inverter)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HCT04P/FP/DP

HEX INVERTER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT04 is a semiconductor integrated circuit consisting of six inverters.

FEATURES

- TTL level input V_{IL}=0.8V, max V_{IH}=2.0V, min
- High-speed: 10ns typ. (C_L=15pF, Vcc=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 10 74LSTTL loads
- Wide operating temperature range: T_a=−40∼+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

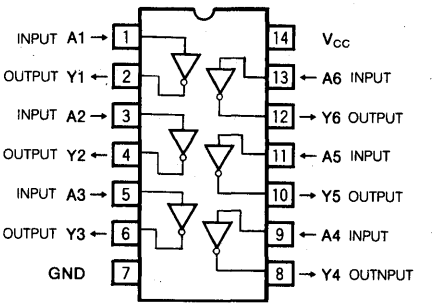
Use of silicon gate technology allows the M74HCT04 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS04.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

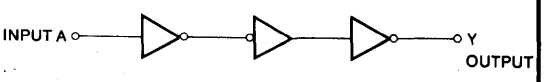
When input A is high, the output Y will become low, and when input A is low, the output Y will become high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

LOGIC DIAGRAM (EACH INVERTER)



FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 1 : M74HCT04FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HCT04DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5		5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature range	−40		+85	℃
t_r, t_f	Input risetime, falltime	0		500	ns

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level ouutput voltage	V_I = V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −4.0mA, V_{CC} = 4.5V	4.18			4.13		
			I_{OH} = −4.8mA, V_{CC} = 5.5V	5.18			5.13		
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 4.0mA, V_{CC} = 4.5V			0.26		0.33	
			I_{OL} = 4.8mA, V_{CC} = 5.5V			0.26		0.33	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				1.0		10.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 2)				2.7		2.9	mA

Note 2 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

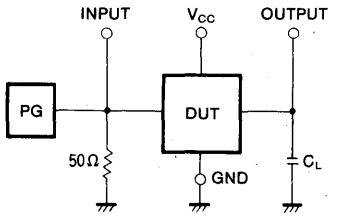
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				15	ns
t_{PHL}	output propagation time				15	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40∼+85℃)

Symbol	Parameter	est conditions	Limits					Unit
			25℃			−40∼+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			15		19	ns
t_{THL}					15		19	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				18		24	ns
t_{PHL}					18		24	ns
C_I	Input capacitance				10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)							pF

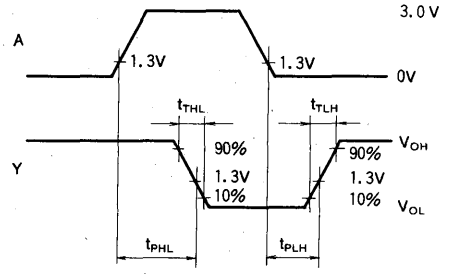
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per inverter)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC05P/FP/DP

HEX INVERTER WITH OPEN-DRAIN OUTPUTS

DESCRIPTION

The M74HC05 is a semiconductor integrated circuit consisting of six inverters with open-drain outputs.

FEATURES

- Open-drain outputs
- High-speed: 8ns typ. (C_LP=15pF, Vcc=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC05 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS05.

Open-drain outputs allow a versatile selection of high output impedances by connecting external load resistors.

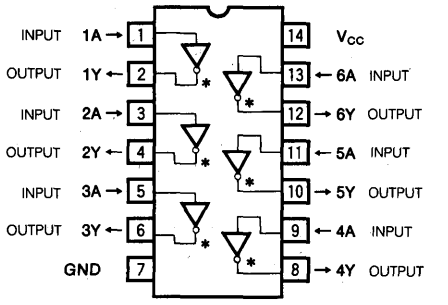
This enables "AND ties" which are not possible using normal gates. When input A is high, the output Y will become low, and when A is low, Y will become high.

Note that this IC differs from the 74LS05 and a voltage higher than Vcc can not be applied to the output.

FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

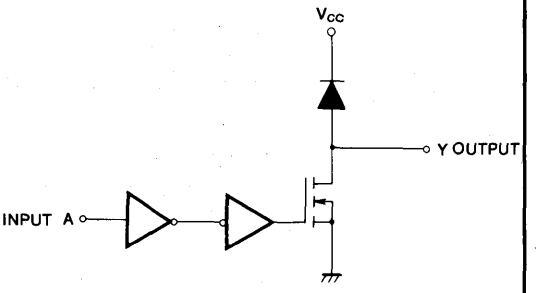
PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

* : Open-drain output

LOGIC DIAGRAM (EACH INVERTER)



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 1 : M74HC05FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC05DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
					25℃			−40∼+85℃	
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level output current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_O	Maximum output leakage current	V_I = V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
		V_I = V_{IL}, V_O = GND		6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

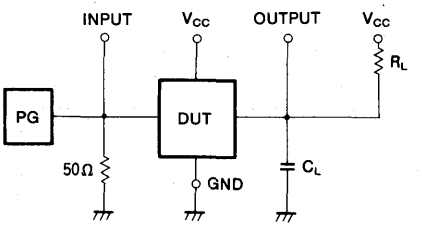
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{THL}	High-level to low-level output transition time	R_L = 1kΩ C_L = 15pF (Note 3)			10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time	R_L = 1kΩ, C_L = 5pF (Note 3)			20	ns
t_{PHL}		R_L = 1kΩ, C_L = 15pF (Note 3)			14	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{THL}	High-level to low-level output transition time	R_L = 1kΩ C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			85		105	ns
			4.5			17		21	
			6.0			14		18	
C_I	Input capacitance					10		10	pF
C_O	Output capacitance	A = GND				10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				8				pF

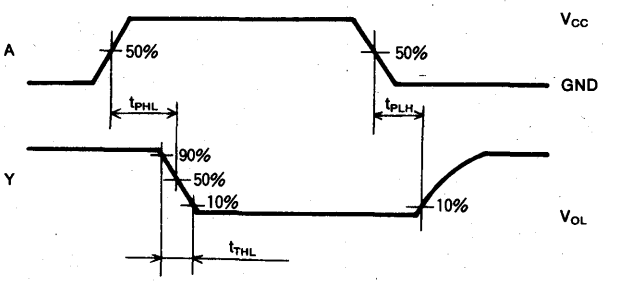
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC08P/FP/DP

QUADRUPLE 2-INPUT POSITIVE AND GATE

DESCRIPTION

The M74HC08 is a semiconductor integrated circuit consisting of four 2-input positive-logic AND gates, usable as negative-logic OR gates.

FEATURES

- High-speed: 9.5ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

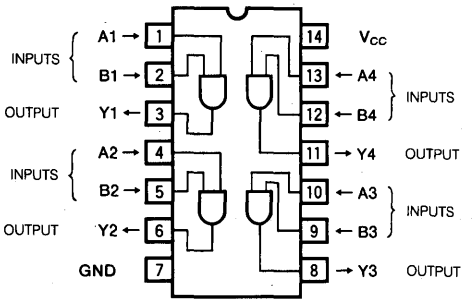
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC08 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS08.

Buffered outputs Y improve input-to-output transfer characteristics and minimizes output impedance variations with respect to input voltage variations.

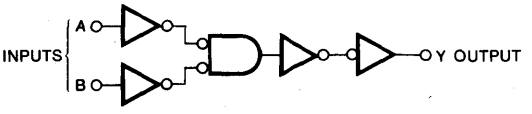
When both inputs A and B are high, the output Y will become high, and when at least one of the inputs is low, Y will become low.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC08FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC08DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

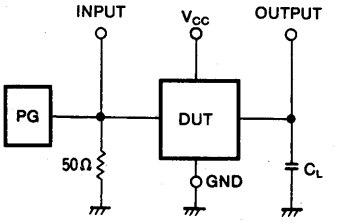
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					20	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			121		151	ns
			4.5			24		30	
			6.0			20		25	
t_{PHL}			2.0			121		151	ns
			4.5			24		30	
			6.0			20		25	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				40				pF

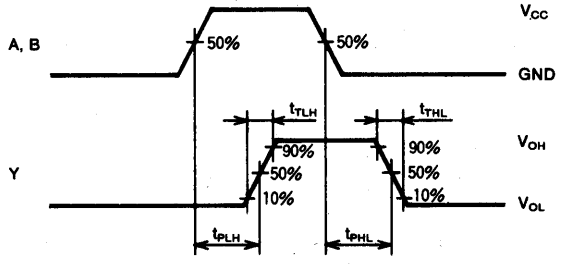
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC09P/FP/DP

QUADRUPLE 2-INPUT POSITIVE AND GATE WITH OPEN-DRAIN OUTPUTS

DESCRIPTION

The M74HC09 is a semiconductor integrated circuit consisting of four 2-input positive-logic AND gates usable as negative-logic OR gates, with open-drain outputs.

FEATURES

- Open-drain outputs
- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

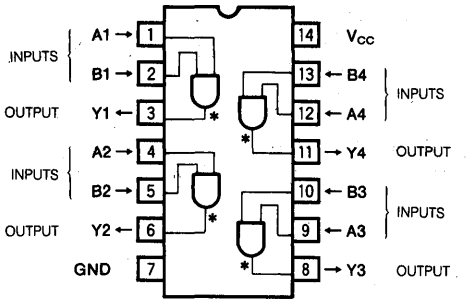
Use of silicon gate technology allows the M74HC09 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS09.

Open-drain outputs allow a versatile selection of high output impedances by connecting external load resistors. This enables "AND ties" which are not possible using normal gates.

When both inputs A and B are high, the output Y will become high, and when either A or B is low, Y will become low.

Note that this IC differs from 74LS09 and a voltage higher than Vcc can not be applied to the outputs.

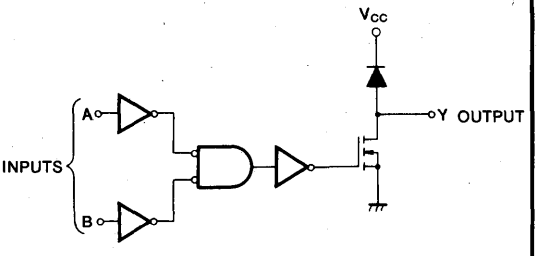
PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

* : Open-drain output

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

QUADRUPLE 2-INPUT POSITIVE AND GATE WITH OPEN-DRAIN OUTPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC09FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC09DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min.	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_O	Maximum output leakage current	V_I = V_{IH}, V_O = V_{CC}		6.0			0.5		5.0	μA
		V_I = V_{IH}, V_O = GND		6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

QUADRUPLE 2-INPUT POSITIVE AND GATE WITH OPEN-DRAIN OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

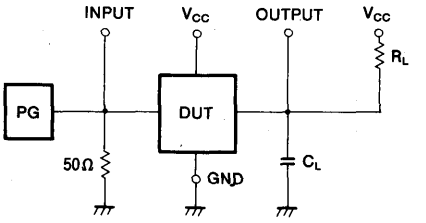
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{THL}	High-level to low-level output transition time	R_L = 1kΩ C_L = 15pF (Note 3)			10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time	R_L = 1kΩ, C_L = 5pF (Note 3)			18	ns
t_{PHL}		R_L = 1kΩ, C_L = 15pF (Note 3)			18	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{THL}	High-level to low-level output transition time	R_L = 1kΩ C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			105		131	ns
			4.5			25		31	
			6.0			23		27	
t_{PHL}			2.0			100		125	ns
			4.5			20		25	
			6.0			17		21	
C_I	Input capacitance					10		10	pF
C_O	Output capacitance	A, B = V_{CC}				10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				10				pF

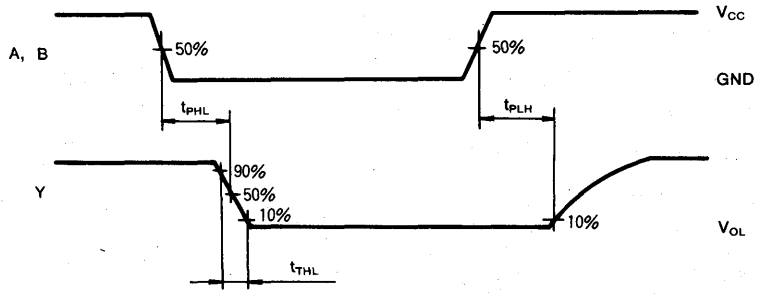
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC10P/FP/DP

TRIPLE 3-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC10 is a semiconductor integrated circuit consisting of three 3-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC10 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS10.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimium output impedance variations with respect to input voltage variations.

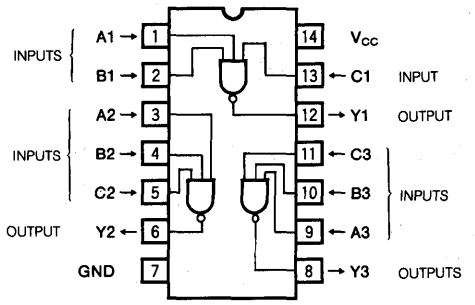
When all inputs A, B and C are high, the output Y will become low, and when at least one of the inputs is low, the output Y will become high.

FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

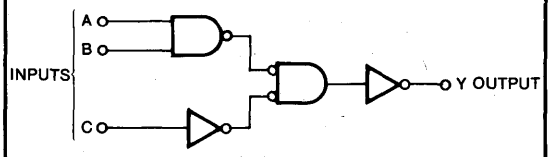
N = B·C

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

LOGIC DIAGRAM (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC10FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC10DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits					Unit
					25℃			−40~+85℃		
					Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent pupply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

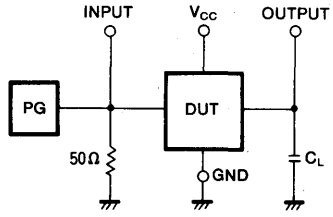
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			95		120	ns
			4.5			19		24	
			6.0			16		20	
t_{PHL}			2.0			95		120	ns
			4.5			19		24	
			6.0			16		20	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				36				pF

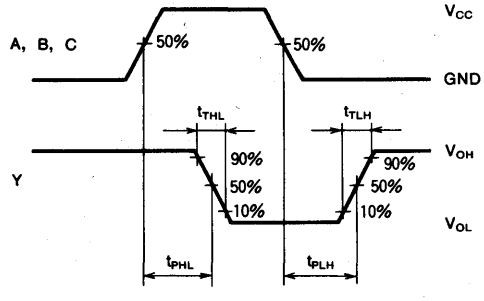
Note 2 : C_{PD} is the internal capacitance of the IC per gate calculated from operation supply current under no-load conditions. (per gate)
The power dissipatiod during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC11P/FP/DP

TRIPLE 3-INPUT POSITIVE AND GATE

DESCRIPTION

The M74HC11 is a semiconductor integrated circuit consisting of three 3-input positive-logic AND gates, usable as negative-logic OR gates.

FEATURES

- High-speed: 12ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC11 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS11.

Buffered outputs Y improve input-to-output transfer characteristics and minimizes output impedance variations with respect to input voltage variations.

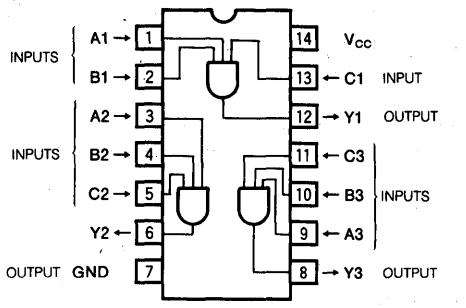
When all inputs A, B and C are high, the output Y will become high, and when at least one of the inputs is low, Y will become low.

FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	L
H	L	L
L	H	L
H	H	H

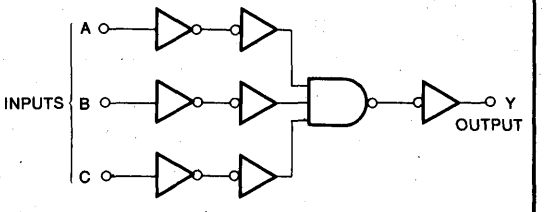
N = B·C

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

LOGIC DIAGRAM (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC11FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC11DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

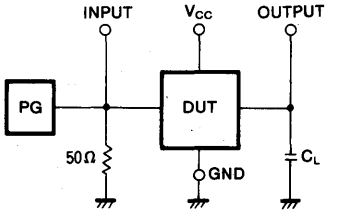
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				20	ns
t_{PHL}					20	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0		75		95	ns
			4.5		15		19	
			6.0		13		16	
t_{THL}			2.0		75		95	ns
			4.5		15		19	
			6.0		13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0		125		156	ns
			4.5		25		31	
			6.0		21		27	
t_{PHL}			2.0		125		156	ns
			4.5		25		31	
			6.0		21		27	
C_I	Input capacitance				10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)			34				pF

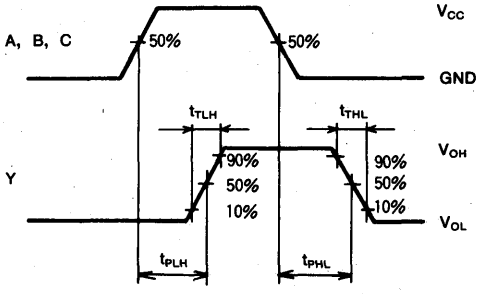
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operating supply current under no-load conditions. (per gate)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC14P/FP/DP

HEX SCHMITT-TRIGGER INVERTER

DESCRIPTION

The M74HC14 is a semiconductor integrated circuit consisting of six Schmitt-trigger inverters.

FEATURES

- High-speed: 12ns typ. (C_L=15pF, Vcc=5V)
- Wide hysteresis voltage width: 0.8V (V_{CC}=5V, typ)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

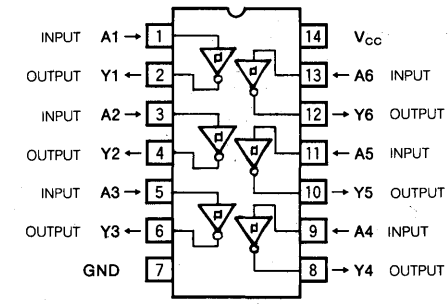
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC14 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS14.

Built-in Schmitt-trigger circuits prevent the occurrence of incorrect oscillations even when input signals having slow rise and fall times are applied. The Schmitt triggers ensure a signal of restored waveshape will appear at the output.

When input A is high, the output Y will become low, and when input A is low, the output Y will become high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

LOGIC DIAGRAM (EACH SCHMITT-TRIGGER)

FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC14FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC14DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature range	−40		+85	℃
t_r, t_f	Input risetime, falltime	No restriction			ns

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
				25℃			−40∼+85℃			
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{T+}	Positive-going threshold voltage	V_O = 0.1V $\|I_O\|$ = 20μA		2.0	0.7		1.5	0.7	1.5	V
				4.5	1.55		3.15	1.55	3.15	
				6.0	2.1		4.2	2.1	4.2	
V_{T-}	Negative-going threshold voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	0.3		1.0	0.3	1.0	V
				4.5	0.9		2.45	0.9	2.45	
				6.0	1.2		3.2	1.2	3.2	
V_H	Hysteresis voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	0.2		1.2	0.2	1.2	V
				4.5	0.4		2.1	0.4	2.1	
				6.0	0.5		2.5	0.5	2.5	
V_{OH}	High-level output voltage	V_I = V_{T-}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{T+}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

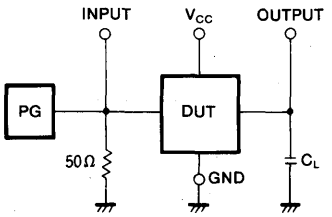
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				22	ns
t_{PHL}					22	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
t_{PHL}			2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				29				pF

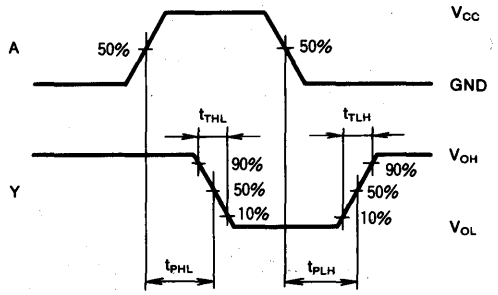
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per inverter)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC20P/FP/DP

DUAL 4-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC20 is a semiconductor integrated circuit consisting of two 4-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC20 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS20.

Buffered output Y improve input-to-output transfer characteristics and reduce to a minimium output impedance variations with respect to input voltage variations.

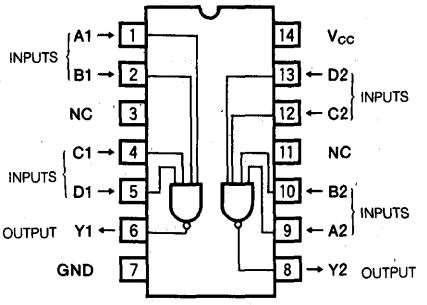
When all inputs A, B, C and D are high, the output Y will become low, and when at least one of the inputs is low, the output Y will become high.

FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

N = B·C·D

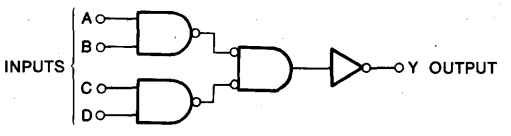
PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

NC : NO CONNECTION

LOGIC DIAGRAM (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC20FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC20DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
					25℃			−40∼+85℃	
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

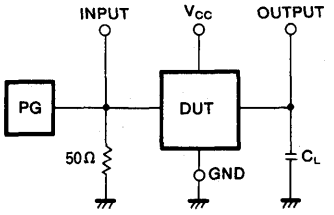
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			90		113	ns
			4.5			18		23	
			6.0			15		19	
t_{PHL}			2.0			90		113	ns
			4.5			18		23	
			6.0			15		19	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				34				pF

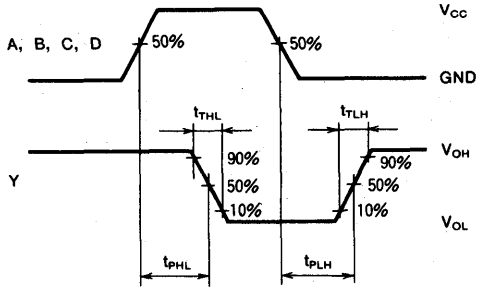
Note 2 : C_{PD} is the internal capacitance of the IC per gate calculated from operation supply current under no-load conditions. (per gate)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC21P/FP/DP

DUAL 4-INPUT POSITIVE AND GATE

DESCRIPTION

The M74HC21 is a semiconductor integrated circuit consisting of two 4-input positive-logic AND gates, usable as negative-logic OR gates.

FEATURES

- High-speed: 12ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise marging: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC21 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS locig 4000B series while giving high-speed performance equivalent to the 74LS21.

Buffered outputs improve input-to-output transfer characteristics and minimizes output impedance variations with respect to input voltage variations.

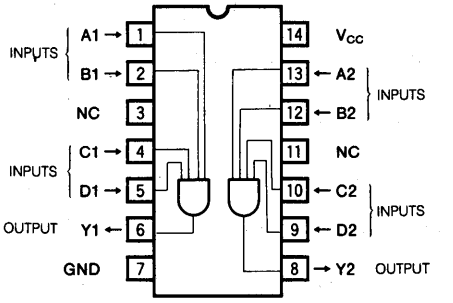
When all inputs A, B, C and D are high, the output Y will become high, and when at least one of the inputs is low, Y will become low.

FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	L
H	L	L
L	H	L
H	H	H

N = B·C·D

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

NC : NO CONNECTION

M74HC27P/FP/DP

TRIPLE 3-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74HC27 is a semiconductor integrated circuit consisting of three 3-input positive-logic NOR gates, usable as negative-logic NAND gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

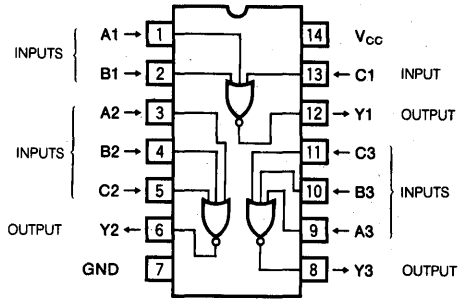
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC27 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS27.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

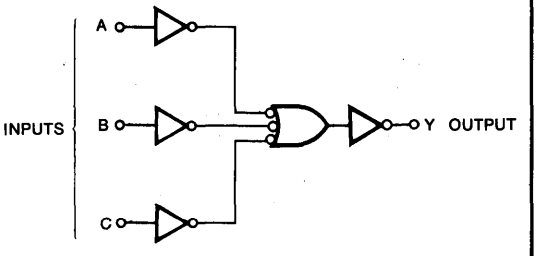
When all inputs A, B and C are low, the output Y will become high, and when at least one of the inputs is high, the output Y will become low.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	L
L	H	L
H	H	L

N = B + C

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC27FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC27DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −4.0mA	4.5	4.18			4.13		
		I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 4.0mA	4.5			0.26		0.33	
		I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

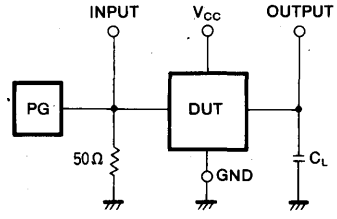
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			90		113	ns
			4.5			18		23	
			6.0			15		19	
t_{PHL}			2.0			90		113	ns
			4.5			18		23	
			6.0			15		19	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				34				pF

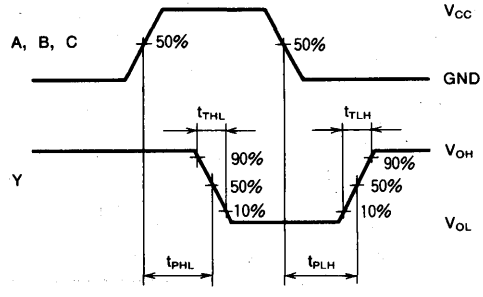
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC30P/FP/DP

8-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC30 is a semiconductor integrated circuit consisting of an 8-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High-speed: 20ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

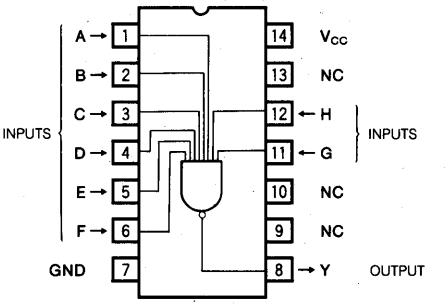
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC30 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS30.

Buffered Y outputs improve input-to-output propagation characteristics and reduce output impedance variations with respect to input voltage variations.

When all inputs A, B, C, D, E, F, G and H are high, the output Y will become low, and when at least one of the inputs is high, the output Y will become high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

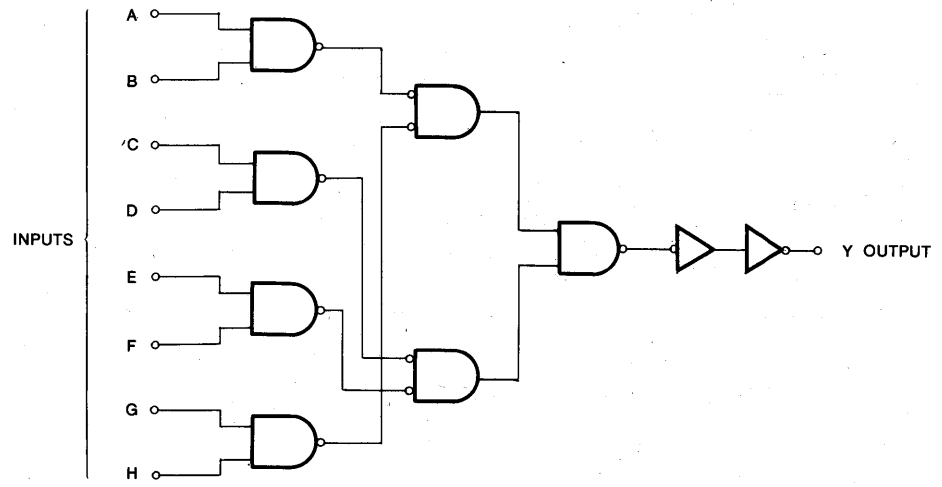
NC : NO CONNECTION

FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

N = B·C·D·E·F·G·H

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 1 : M74HC30FP, T_a = −40∼+60℃ and T_a = 60−85℃ are derated at −6mW/℃
M74HC30DP, T_a = −40∼+50℃ and T_a = 50−85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test condition		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

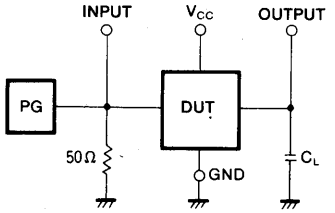
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				30	ns
t_{PHL}					30	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			160		190	ns
			4.5			35		42	
			6.0			30		36	
t_{PHL}			2.0			160		190	ns
			4.5			35		42	
			6.0			30		36	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				33				pF

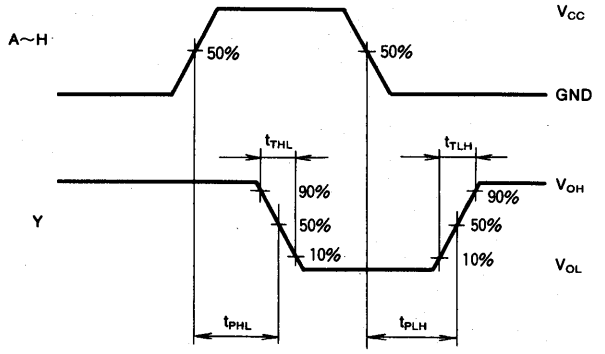
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC32P/FP/DP

QUADRUPLE 2-INPUT POSITIVE OR GATE

DESCRIPTION

The M74HC32 is a semiconductor integrated circuit consisting of four 2-input positive-logic OR gates, usable as negative-logic AND gates.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

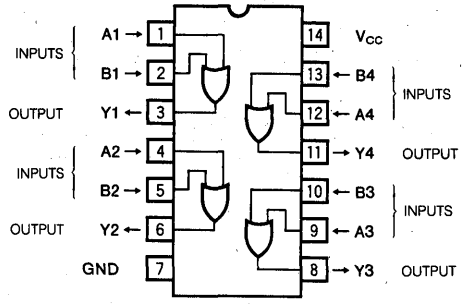
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC32 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS32.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

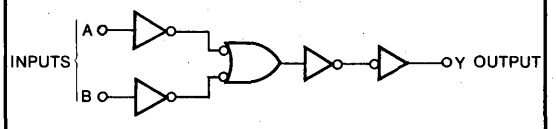
When both inputs A and B are low, output Y will become low, and when at least one of the inputs is high, the output Y will become high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC32FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC32DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}; I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −4.0mA	4.5	4.18			4.13		
		I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IL}; I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 4.0mA	4.5			0.26		0.33	
		I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

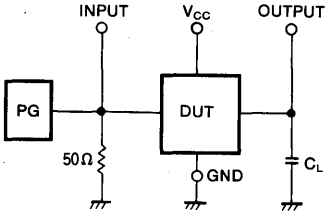
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				18	ns
t_{PHL}					18	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			100		125	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		125	ns
			4.5			20		25	
			6.0			17		21	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				30				pF

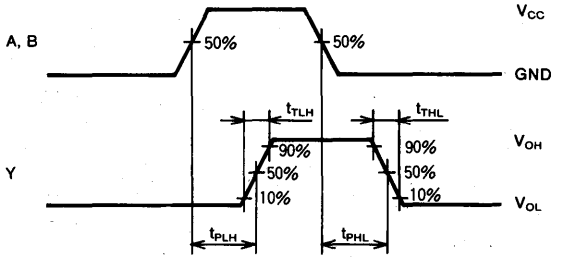
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC42P/FP/DP

1-OF-10 DECODER

DESCRIPTION

The M74HC42 is a semiconductor integrated circuit consisting of a BCD to decimal decoder.

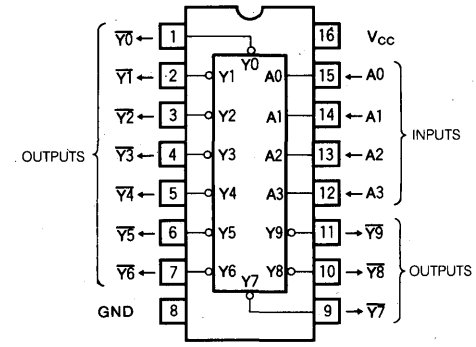
FEATURES

- Active-low output
- High-speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



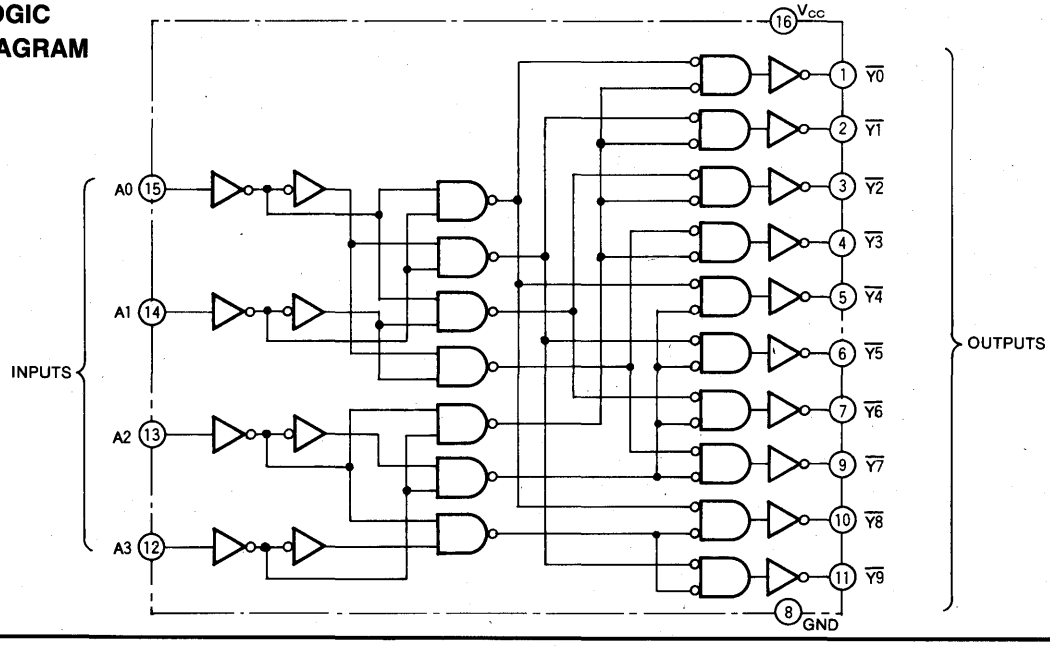
Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC42 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS42.

When a BCD code is applied to inputs A0, A1, A2 and A3, one of outputs $\overline{Y0}$ through $\overline{Y9}$ corresponding to this value will become low and all others will become high. Use A0 for the least significant bit and A3 for the most significant bit. If a value of ten or greater is applied to the inputs (A0 through A3), all outputs will become high.

LOGIC DIAGRAM



FUNCTION TABLE

Decimal number	Inputs				Outputs									
	A3	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	H	L	H	L	H	H	H	H	H	H	H	H	H	H
11	H	L	H	H	H	H	H	H	H	H	H	H	H	H
12	H	H	L	L	H	H	H	H	H	H	H	H	H	H
13	H	H	L	H	H	H	H	H	H	H	H	H	H	H
14	H	H	H	L	H	H	H	H	H	H	H	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 1 : M74HC42FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC42DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0		−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0		4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

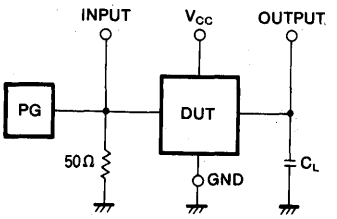
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 3)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time				25	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2～6V, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				86				pF

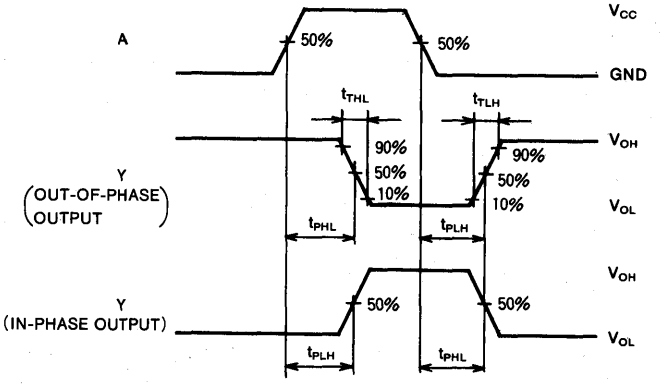
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC51P/FP/DP

2-WIDE,2-INPUT/2-WIDE,3-INPUT AND-OR-INVERT GATES

DESCRIPTION

The M74HC51 is a semiconductor integrated circuit consisting of a 2-wide, 2-input/2-wide, 3-input AND-OR-INVERT gate.

FEATURES

- High speed: 9ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

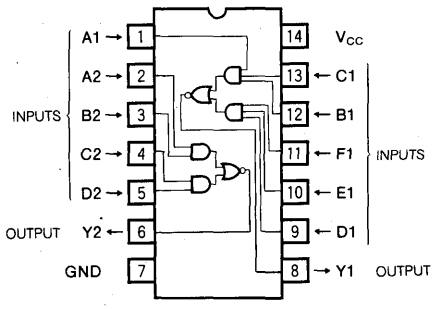
Use of silicon gate technology allows the M74HC51 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS51.

The M74HC51 consists of two NOR gate, one using two 2-inputs AND gates for the input and the other using two 3-input AND gates for the input. The characteristics are described by the following logical equations.

$Y1 = \overline{A1 \cdot B1 \cdot C1 \cdot D1 \cdot E1 \cdot F1}$

$Y2 = \overline{A2 \cdot B2 + C2 \cdot D2}$

PIN CONFIGURATION (TOP VIEW)



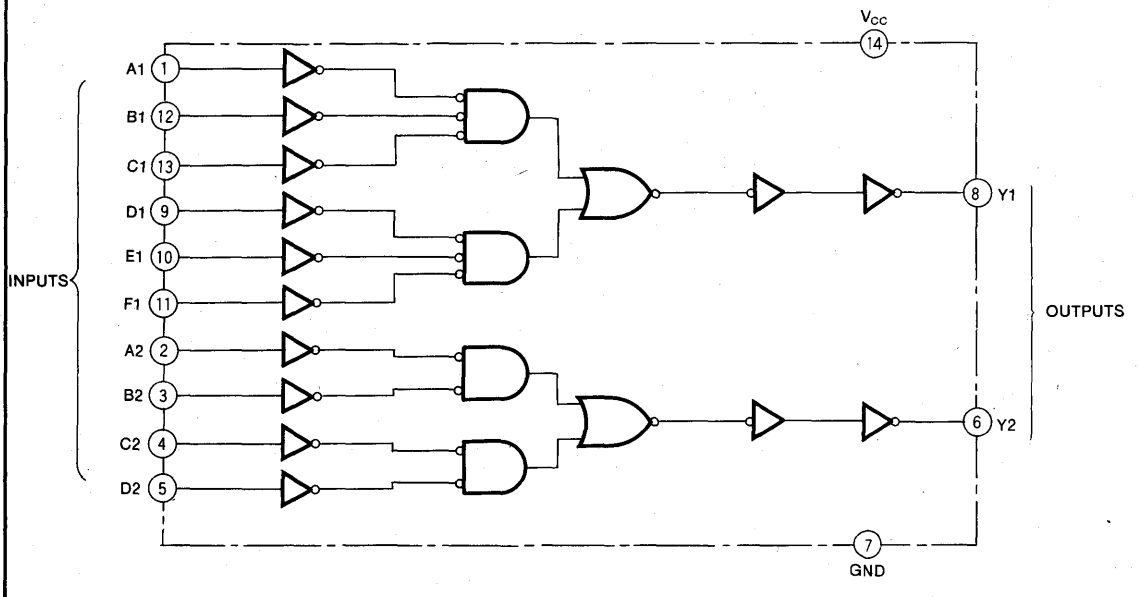
14P4
Outline 14P2N
14P2P

FUNCTION TABLE (Note 1)

Inputs		Output
M	N	Y
L	L	H
H	L	L
L	H	L
H	H	L

Note 1 : M=A1 · B1 · C1
N=D1 · E1 · F1
or
M=A2 · B2
N=C2 · D2

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2. M74HC51FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC51DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits					Unit
					25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

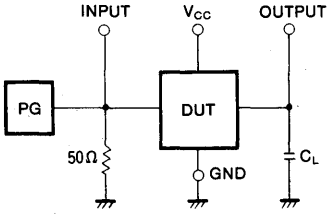
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				20	ns
t_{PHL}					20	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
				25℃		−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				35				pF

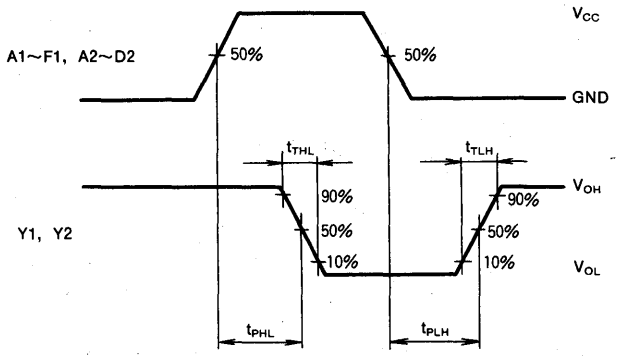
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC73P/FP/DP

DUAL J-K FLIP-FLOP WITH RESET

DESCRIPTION

The M74HC73 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

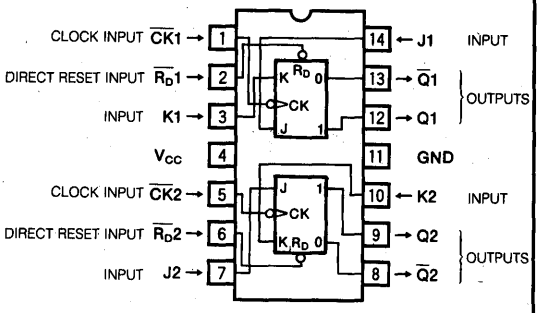
FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

FUNCTIONAL DESCRIPTION

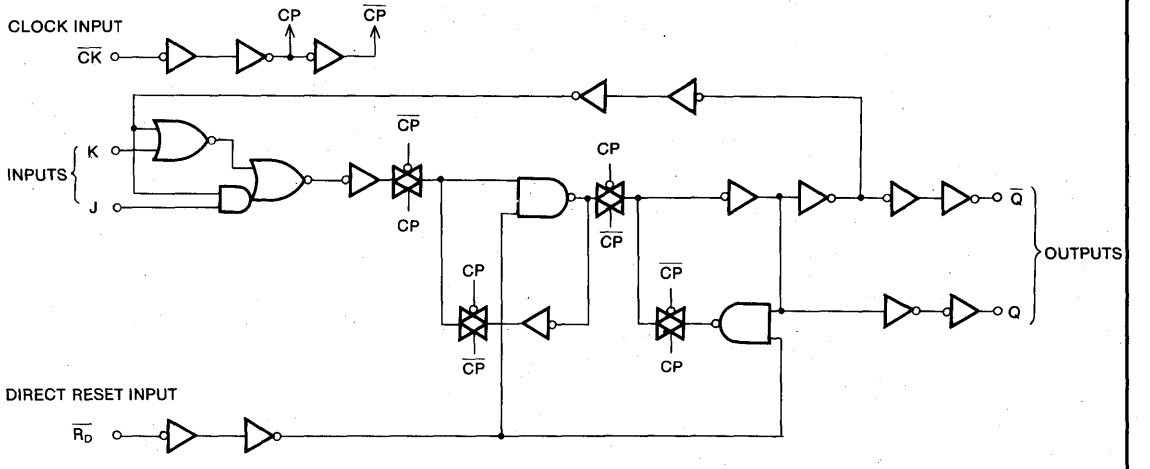
Use of silicon gate technology allows the M74HC73 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS73.

The M74HC73 contains two edge-triggered J-K flip flops, each circuit with independent clock input $\overline{CK}$, direct reset input $\overline{R_D}$, and both inputs J and K.

When $\overline{CK}$ is high, the J and K signals can be read. When $\overline{CK}$ changes from high-level to low-level, the signals just previousy input at J and K appear at outputs Q and $\overline{Q}$ in accordance with the function table given. When $\overline{R_D}$ is low, Q and $\overline{Q}$ will become low and high respectively, irrespective of other inputs. When used as a J-K flip flop, $\overline{R_D}$ should be maintained at high-level.

A unit, the M74HC107, having the same functions and electrical characteristics as the M74HC73 is also available. This offers easy mounting with pins 7 and 14 being GND and V_{CC} respectively.

LOGIC DIAGRAM (EACH FLIP FLOP)



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FUNCTION TABLE (Note 1)

Inputs				Outputs	
$\overline{R_D}$	$\overline{CK}$	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q^0	$\overline{Q}^0$
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	H	H	Toggle	
H	L	X	X	Q^0	$\overline{Q}^0$
H	H	X	X	Q^0	$\overline{Q}^0$
H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high
↓ : Change from high to low
X : Irrelevant
Q^0 : Output state Q before clock input changed
$\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
Toggle : Inversion state before clock input changed

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC73FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC73DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
				25℃			−40∼+85℃			
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ – Q, $\overline{Q}$)				28	ns
t_{PHL}					28	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ – Q, $\overline{Q}$)				34	ns
t_{PHL}					34	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

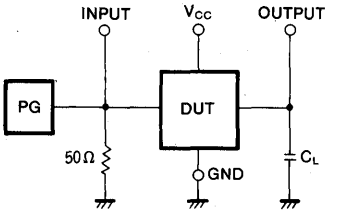
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ – Q, $\overline{Q}$)		2.0			160		195	ns
			4.5			32		39	
			6.0			28		34	
t_{PHL}			2.0			160		195	ns
			4.5			32		39	
			6.0			28		34	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ – Q, $\overline{Q}$)		2.0			195		235	ns
			4.5			39		47	
			6.0			34		40	
t_{PHL}			2.0			195		235	ns
			4.5			39		47	
			6.0			34		40	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				52				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

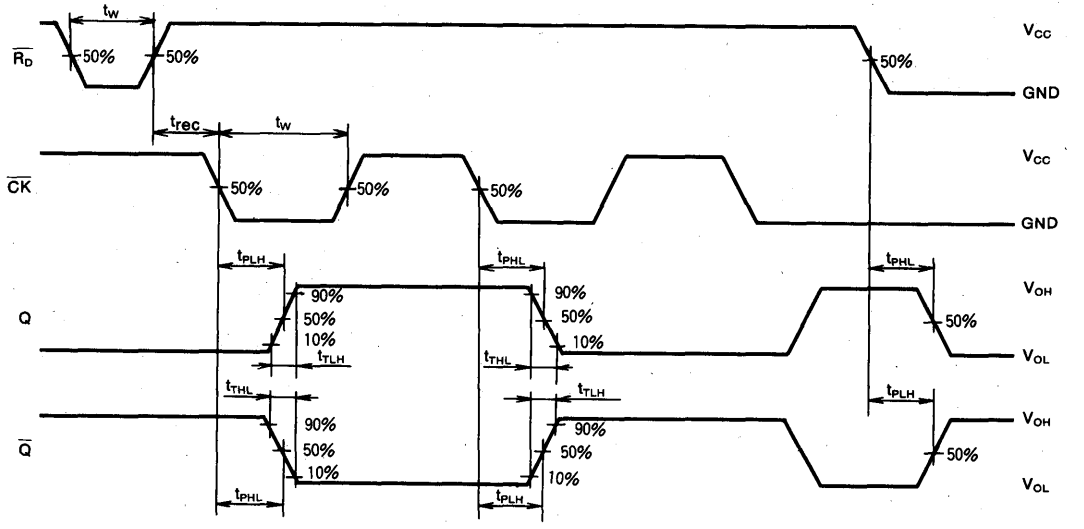
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{R_D}$ recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

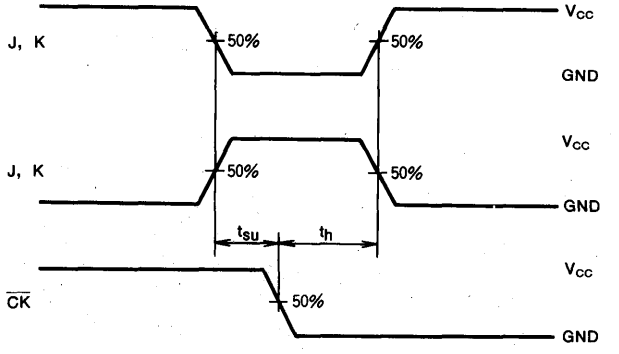
Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC74P/FP/DP

DUAL D-TYPE FLIP-FLOP WITH SET AND RESET

DESCRIPTION

The M74HC74 is a semiconductor integrated circuit consisting of two positive-edge triggered D-type flip flops with independent clock, data, and direct set and reset inputs.

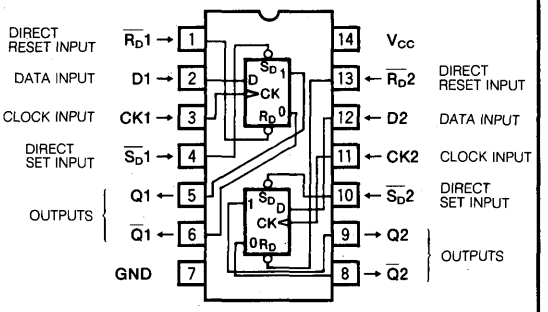
FEATURES

- High-speed: (clock frequency)40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



14P4
Outline 14P2N
14P2P

FUNCTIONAL DESCRIPTION

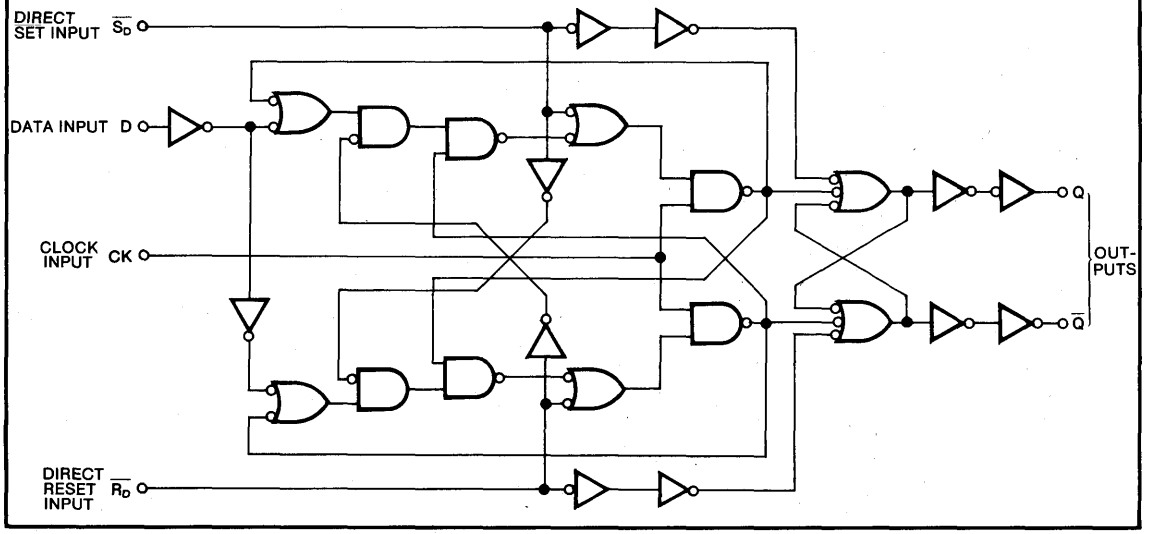
Use of silicon gate technology allows the M74HC74 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS74.

The M74HC74 contains two independent D-type flip flops with independent clock input CK, direct set input $\overline{S_D}$ and direct reset input $\overline{R_D}$.

When used as a D-type flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high-level. When CK changes from low-level to high-level, the signals just previously input present at D appears at outputs Q and $\overline{Q}$ in accordance with the function table given.

Use of $\overline{S_D}$ and $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will both become high. When $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high , the condition of Q and $\overline{Q}$ cannot be predetermined.

LOGIC DIAGRAM (EACH FLIP FLOP)



FUNCTION TABLE (Note 1)

Inputs				Outputs	
$\overline{S_D}$	$\overline{R_D}$	CK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	L	X	Q^0	$\overline{Q}^0$
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	H	X	Q^0	$\overline{Q}^0$
H	H	↓	X	Q^0	$\overline{Q}^0$

Note 1 : X : Irrelevant
↑ : Change from low to high
↓ : Change from high to low
Q^0 : Output state Q before clock input changed
$\overline{Q}^0$: Output state Q before clock input changed
* : When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will become both high. When $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high the condition of Q and $\overline{Q}$ cannot be predetermined.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC74FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC74DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	2.0	1.9			1.9		V
		V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	4.5	4.4			4.4		
		V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	6.0	5.9			5.9		
		V_I = V_{IH}, V_{IL} ; I_{OH} = −4.0mA	4.5	4.18			4.13		
		V_I = V_{IH}, V_{IL} ; I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	2.0			0.1		0.1	V
		V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	4.5			0.1		0.1	
		V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	6.0			0.1		0.1	
		V_I = V_{IH}, V_{IL} ; I_{OL} = 4.0mA	4.5			0.26		0.33	
		V_I = V_{IH}, V_{IL} ; I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

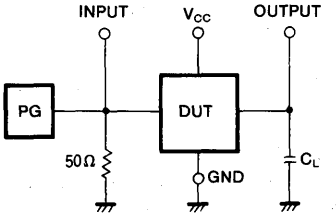
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q, $\overline{Q}$)				30	ns
t_{PHL}					30	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$, $\overline{R_D}$ − Q, $\overline{Q}$)				40	ns
t_{PHL}					40	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q, $\overline{Q}$)		2.0			175		220	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		220	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$, $\overline{R_D}$ − Q, $\overline{Q}$)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				47				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.(per flip-flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit

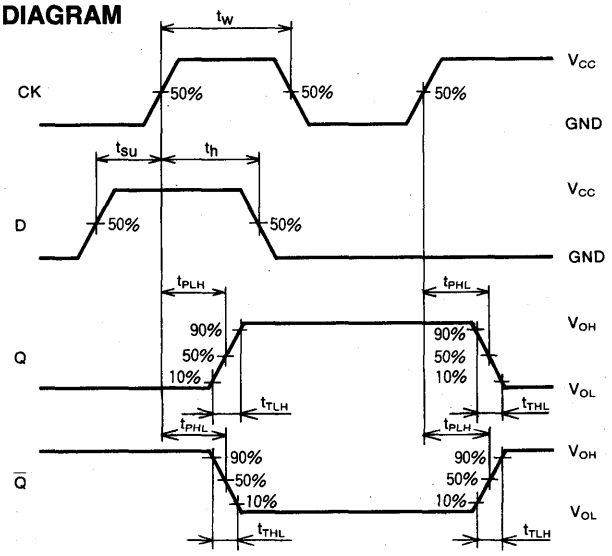


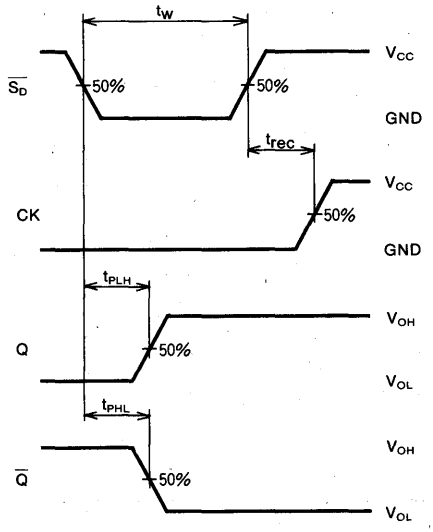
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

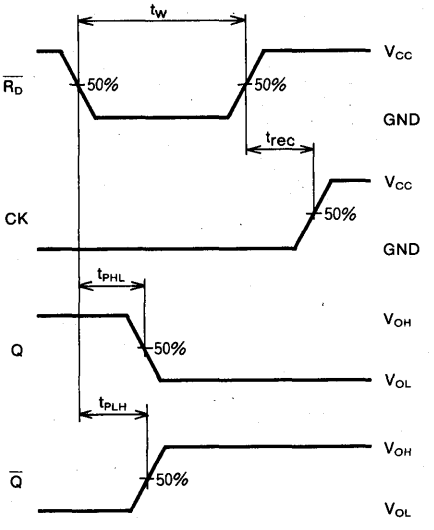
TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{S_D}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	D hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{R_D}$, $\overline{S_D}$ recovery time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

TIMING DIAGRAM







M74HC75P/FP/DP

DUAL 2-BIT TRANSPARENT LATCH

DESCRIPTION

The M74HC75 is a semiconductor integrated circuit consisting of four bistable latches with outputs Q and $\overline{Q}$.

FEATURES

- High-speed: 14ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

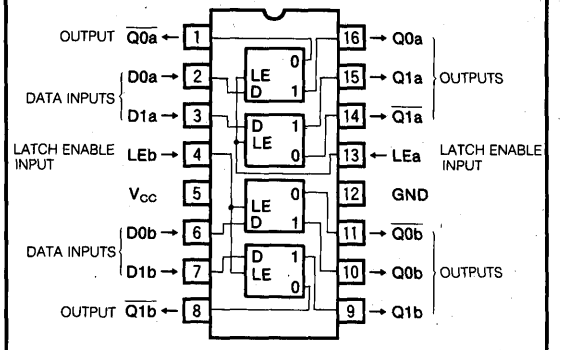
Use of silicon gate technology allows the M74HC75 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS75.

The use of buffered outputs Q and $\overline{Q}$ improves the input to output transfer characteristics and minimizes output impedance variations with respect to input voltage variations.

The M74HC75 has four D-type latches, and is provided with latch enable inputs LE common to two circuits each. When LE is high, the data from the data input D will appear in the outputs Q and $\overline{Q}$. When the D signal changes, the signal that appears in outputs Q and $\overline{Q}$ also will change. When LE changes from high to low, the status of D immediately before the change will be latched. While LE is low, Q and $\overline{Q}$ will not change even if D changes.

A unit, the M74HC375 having the same functions and electrical characteristics as the M74HC75 is also available. This offers easy mounting with pin 8 and 16 being GND and V_{CC} respectively.

PIN CONFIGURATION (TOP VIEW)



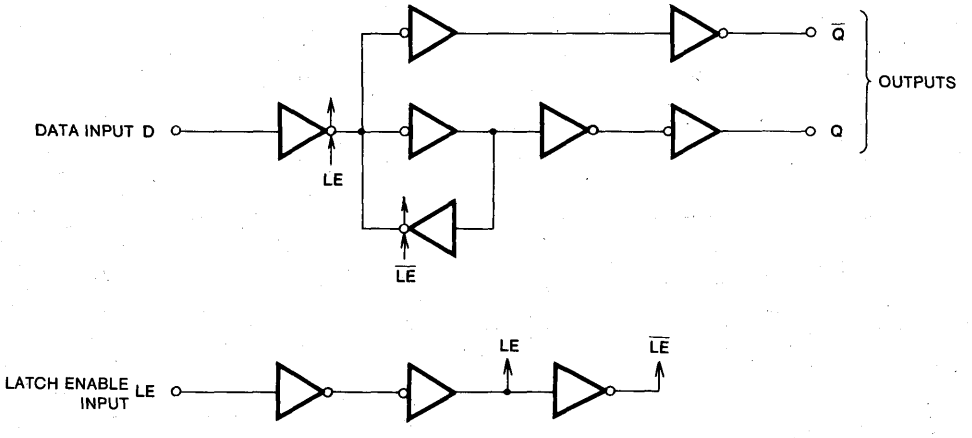
Outline 16P4, 16P2N, 16P2P

FUNCTION TABLE (Note 1)

Inputs		Outputs	
LE	D	Q	$\overline{Q}$
H	H	H	L
H	L	L	H
L	X	Q^0	$\overline{Q}^0$

Note 1 : Q^0, $\overline{Q}^0$: Output state Q, $\overline{Q}$ before input condition is set
X : Irrelevant

LOGIC DIAGRAM (EACH LATCH)



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC75FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC75DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				23	ns
t_{PHL}	output propagation time (D − Q)				23	ns
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (D − $\overline{Q}$)				20	ns
t_{PLH}	Low-level to high-level and high-level to low-level				27	ns
t_{PHL}	output propagation time (LE − Q)				27	ns
t_{PLH}	Low-level to high-level and high-level to low-level				23	ns
t_{PHL}	output propagation time (LE − $\overline{Q}$)				23	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

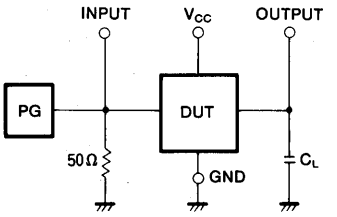
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)		2.0			125		156	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		156	ns
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Q}$)		2.0			110		138	ns
			4.5			22		28	
			6.0			19		24	
t_{PHL}			2.0			110		138	ns
			4.5			22		28	
			6.0			19		24	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − Q)		2.0			145		181	ns
			4.5			29		36	
			6.0			25		31	
t_{PHL}			2.0			145		181	ns
			4.5			29		36	
			6.0			25		31	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − $\overline{Q}$)		2.0			125		156	ns
			4.5			25		31	
			6.0			22		28	
t_{PHL}			2.0			125		156	ns
			4.5			25		31	
			6.0			22		28	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				46				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENT (V_{CC} = 2~6V, T_a = −40~+85℃)

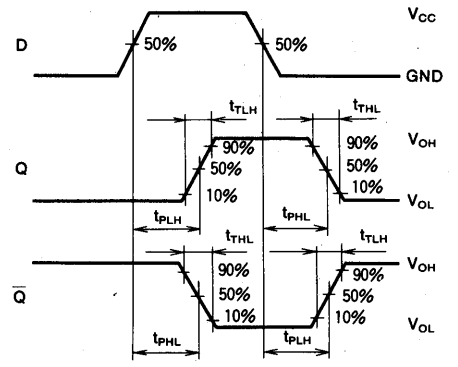
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{LE}$ pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
t_{su}	D setup time with respect to $\overline{LE}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	D hold time with respect to $\overline{LE}$		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

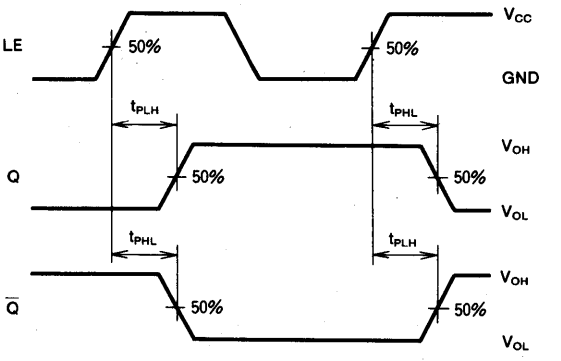
Note 4 : Test Circuit

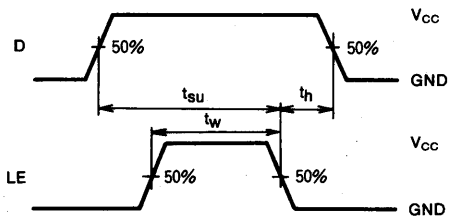


(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







M74HC76P/FP/DP

DUAL J-K FLIP-FLOP WITH SET AND RESET

DESCRIPTION

The M74HC76 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

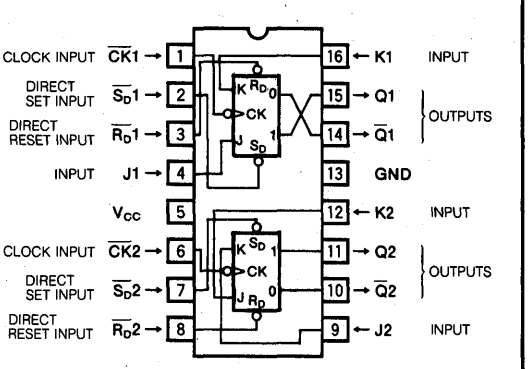
FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

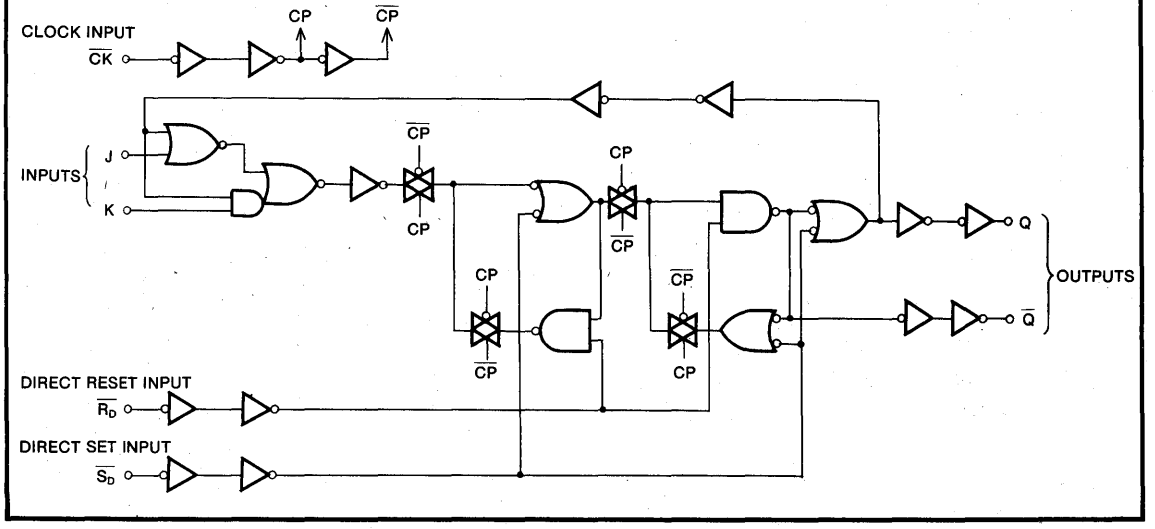
Use of silicon gate technology allows the M74HC76 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS76.

The M74HC76 contains two edge-triggered J-K flip flops, each circuit with independent clock input $\overline{CK}$, direct set input $\overline{S_D}$ and direct reset input $\overline{R_D}$, and both inputs J and K.

When $\overline{CK}$ is high, the J and K signals can be read. When $\overline{CK}$ changes from high-level to low-level, the signals just previously input at J and K appear at outputs Q and $\overline{Q}$ in accordance with the function table given. Use of $\overline{S_D}$ and $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined. When used as a J-K flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high-level.

A unit, the M74HC112, having the same functions and electrical characteristics as the M74HC76 is also avaiable. This offers easy mounting with pin 8 and 16 being GND and V_{CC} respectively.

LOGIC DIAGRAM (EACH FLIP FLOP)



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FUNCTION TABLE (Note 1)

Inputs					Outputs	
$\overline{S_D}$	$\overline{R_D}$	$\overline{CK}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q^0	$\overline{Q}^0$
H	H	↓	L	H	L	H
H	H	↓	H	L	H	L
H	H	↓	H	H	Toggle	
H	H	L	X	X	Q^0	$\overline{Q}^0$
H	H	H	X	X	Q^0	$\overline{Q}^0$
H	H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high
↓ : Change from high to low
X : Irrelevant
Q^0 : Output state Q before clock input changed
$\overline{Q}^0$: Output state Q before clock input changed
Toggle : Inversion state before clock input changed
* : When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ becomes high. When $\overline{S_D}$ and $\overline{R_D}$ become high simultaneously the condition of Q and $\overline{Q}$ cannot be prodetermined.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC76FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC76DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)				26	ns
t_{PHL}					26	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)				33	ns
t_{PHL}					33	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)				33	ns
t_{PHL}					33	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

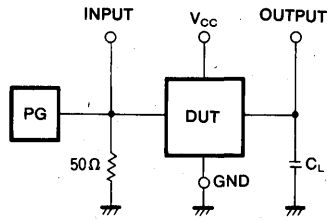
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency		2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			150		180	ns
			4.5			30		36	
			6.0			26		32	
t_{PHL}			2.0			150		180	ns
			4.5			30		36	
			6.0			26		32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)		2.0			190		230	ns
			4.5			38		46	
			6.0			33		40	
t_{PHL}			2.0			190		230	ns
			4.5			38		46	
			6.0			33		40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)		2.0			190		230	ns
			4.5			38		46	
			6.0			33		40	
t_{PHL}			2.0			190		230	ns
			4.5			38		46	
			6.0			33		40	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				56				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

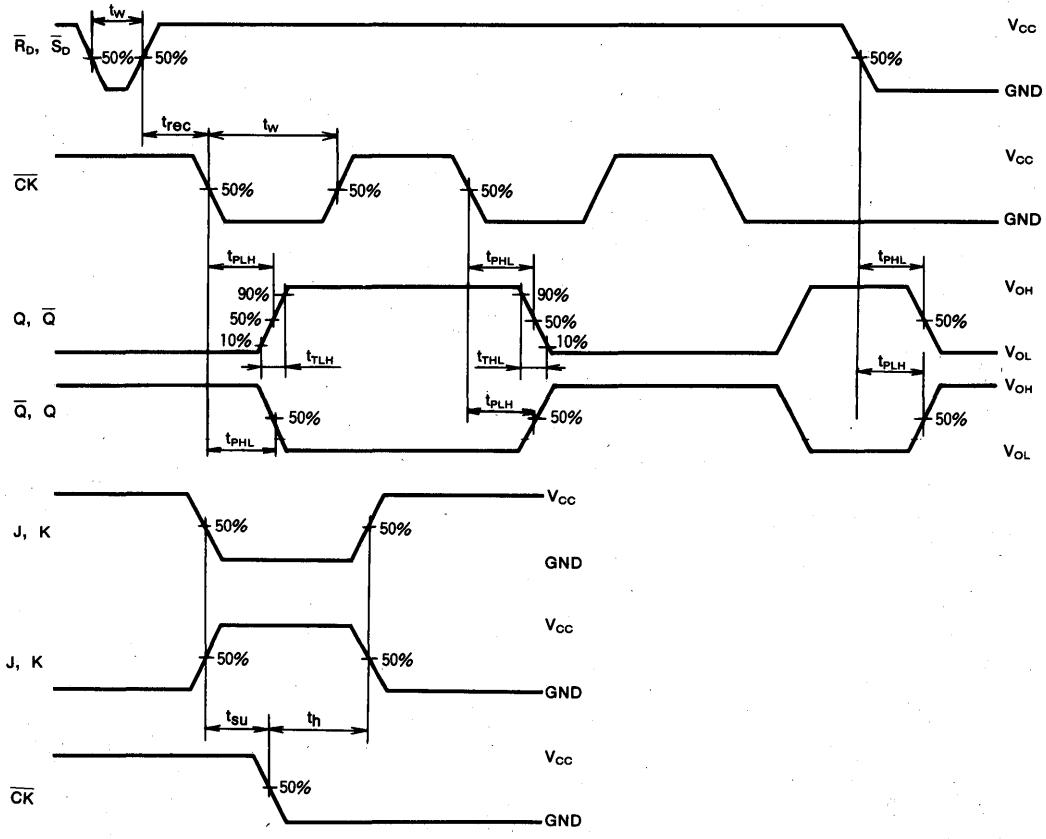
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{S_D}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{R_D}$, $\overline{S_D}$ recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC85P/FP/DP

4-BIT MAGNITUDE COMPARATOR

DESCRIPTION

The M74HC85 is a semiconductor intergrated circuit consisting of a 4-bit digital comparator.

FEATURES

- High-speed: 21ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

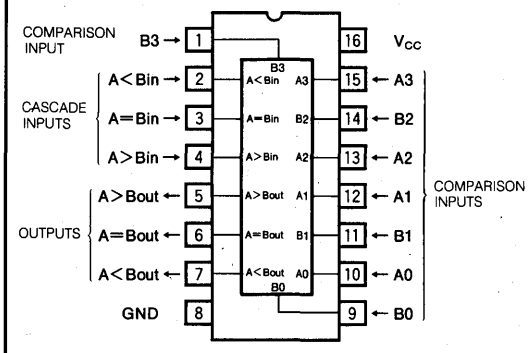
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC85 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS85.

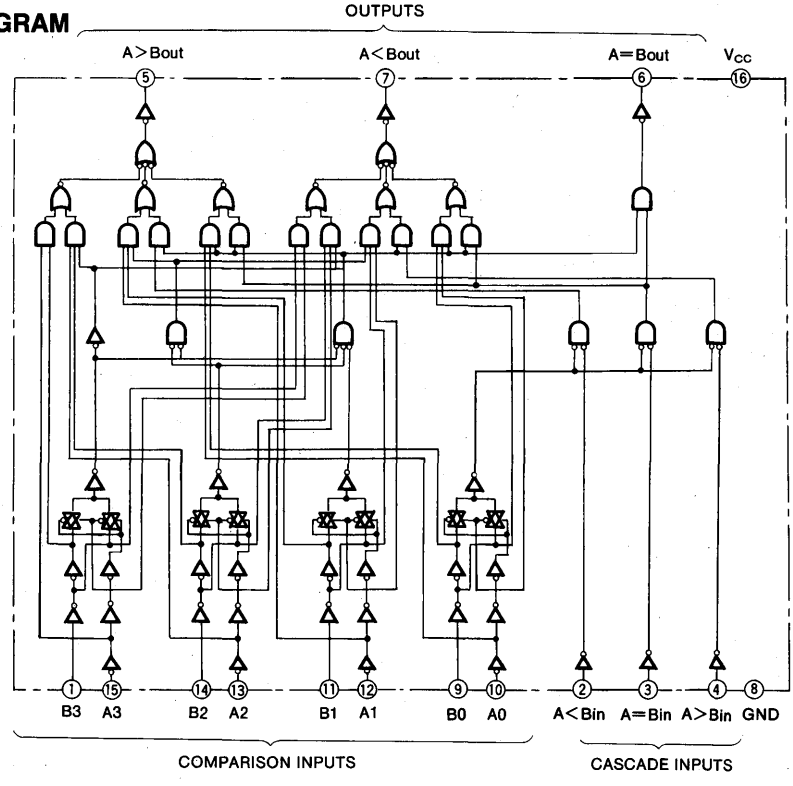
When two 4-bit binary A and B are applied to comparison inputs A0~A3, B0~B3, and cascade input A=Bin is high, the values will be compared and the appropriate output A>Bout, A=Bout or A<Bout will become high. Cascade inputs A>Bin, A=Bin and A<Bin can be connected in cascade to increase the number of bits. (Refer to Application Example)

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs							Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A>Bin	A<Bin	A=Bin	A>Bout	A<Bout	A=Bout
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC85FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC85DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
				25℃			−40∼+85℃			
			V_{CC}(V)	Min	Typ	Max	Min	Max		
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5			V
			4.5	3.15			3.15			
			6.0	4.2			4.2			
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5		V
			4.5			1.35		1.35		
			6.0			1.8		1.8		
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9			V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

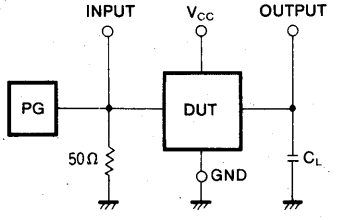
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				40	ns
t_{PHL}	output propagation time (A, B − A > Bout, A < Bout)				40	ns
t_{PLH}	Low-level to high-level and high-level to low-level				35	ns
t_{PHL}	output propagation time (A, B − A = Bout)				35	ns
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (A < Bin, A = Bin − A > Bout)				30	ns
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (A > Bin, A = Bin − A < Bout)				30	ns
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time(A = Bin − A = Bout)				25	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
				25℃		−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − A > Bout, A < Bout)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − A = Bout)		2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PHL}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A < Bin, A = Bin − A > Bout)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A > Bin, A = Bin − A < Bout)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A = Bin − A = Bout)		2.0			145		183	ns
			4.5			29		37	
			6.0			25		31	
t_{PHL}			2.0			145		183	ns
			4.5			29		37	
			6.0			25		31	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				81				pF

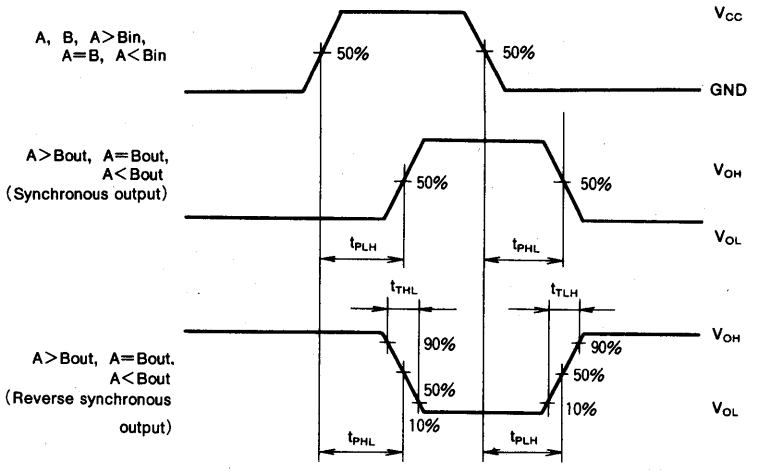
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC86P/FP/DP

QUADRUPLE 2-INPUT EXCLUSIVE OR GATE

DESCRIPTION

The M74HC86 is a semiconductor integrated circuit consisting of four 2-input exclusive OR gates.

FEATURES

- High-speed: 9ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

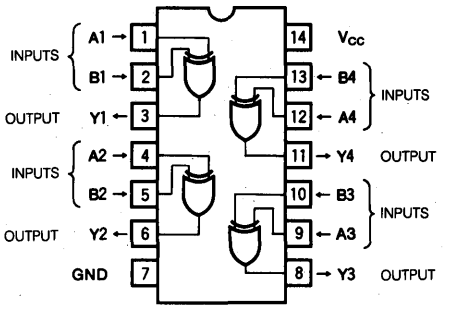
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC86 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS86.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

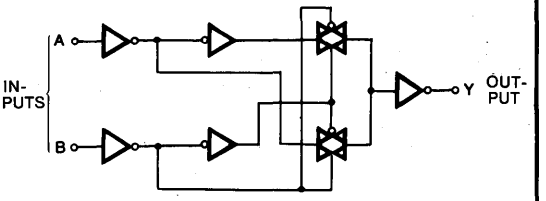
When both inputs A and B are either high or low, the output Y will become low, and when the level of A and B are opposite, Y will become high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	L

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC86FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC86DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

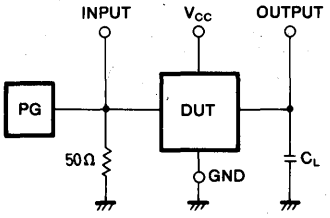
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				20	ns
t_{PHL}					20	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			120		151	ns
			4.5			24		30	
			6.0			20		26	
t_{PHL}			2.0			120		151	ns
			4.5			24		30	
			6.0			20		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				41				pF

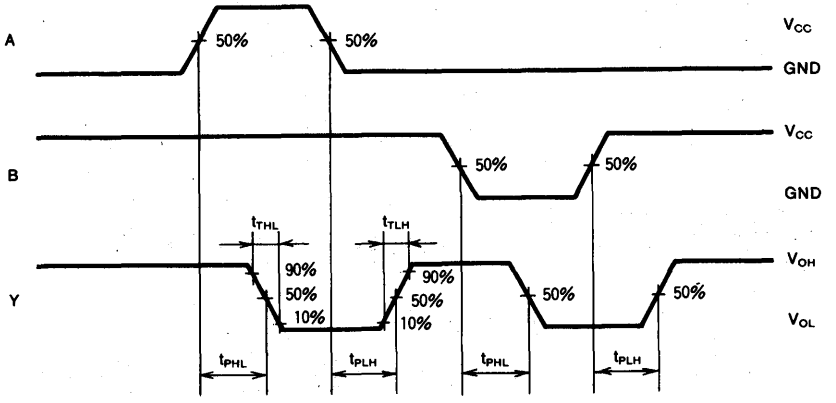
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.(per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC107P/FP/DP

DUAL J-K FLIP-FLOP WITH RESET

DESCRIPTION

The M74HC107 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs

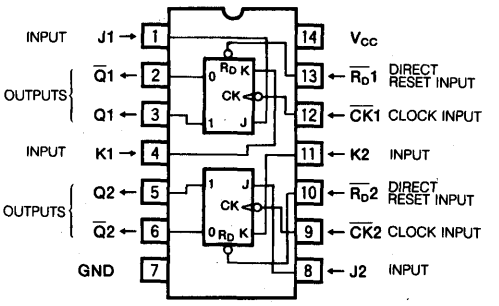
FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC107 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS107.

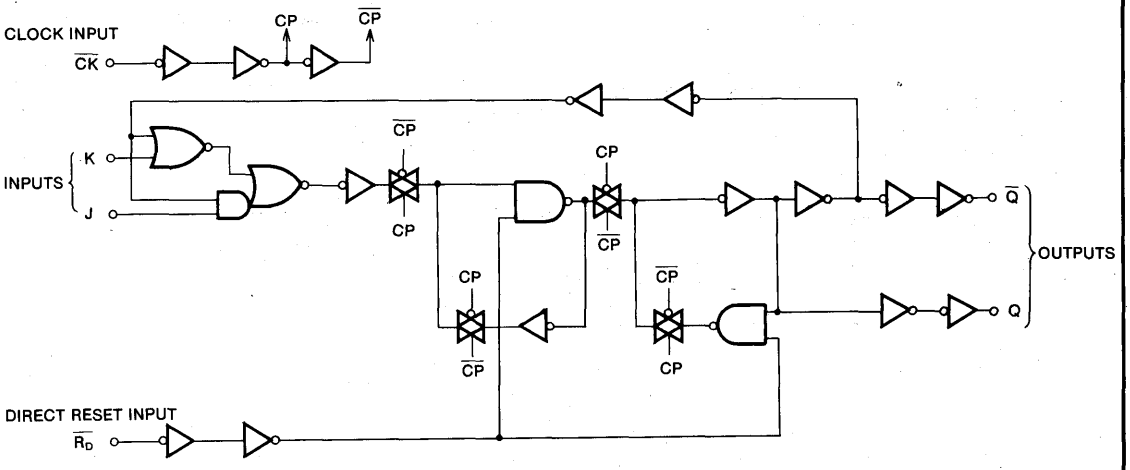
The M74HC107 contains two edge-triggered J-K flip flops, each circuit with independent clock input $\overline{CK}$, direct reset input $\overline{R_D}$, and both inputs J and K.

When $\overline{CK}$ is high, the J and K signals can be read.

When CK changes from high-level to low-level, the signals just previously input at J and K appear at outputs Q and $\overline{Q}$ in accordance with the function table given. When $\overline{R_D}$ is low, Q and $\overline{Q}$ will become low and high respectively, irrespective of other inputs. When used as a J-K flip flop, $\overline{R_D}$ should be maintained at high-level.

M74HC107 is the same functions and electrical characteristics as M74HC73, differing only pin connections.

LOGIC DIAGRAM (EACH FLIP FLOP)



FUNCTION TABLE (Note 1)

Inputs				Outputs	
$\overline{R_D}$	$\overline{CK}$	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q^0	$\overline{Q}^0$
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	H	H	Toggle	
H	L	X	X	Q^0	$\overline{Q}^0$
H	H	X	X	Q^0	$\overline{Q}^0$
H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high
↓ : Change from high to low
X : Irrelevant
Q^0 : Output state Q before clock input changed
$\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
Toggle : Inversion state before clock input changed

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC107FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC107DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				21	ns
t_{PHL}	output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)				21	ns
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)				26	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

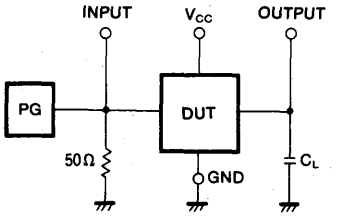
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)		2.0			126		160	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			126		160	ns
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)		2.0			155		194	ns
			4.5			31		39	
			6.0			26		32	
t_{PHL}			2.0			155		194	ns
			4.5			31		39	
			6.0			26		32	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				55				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

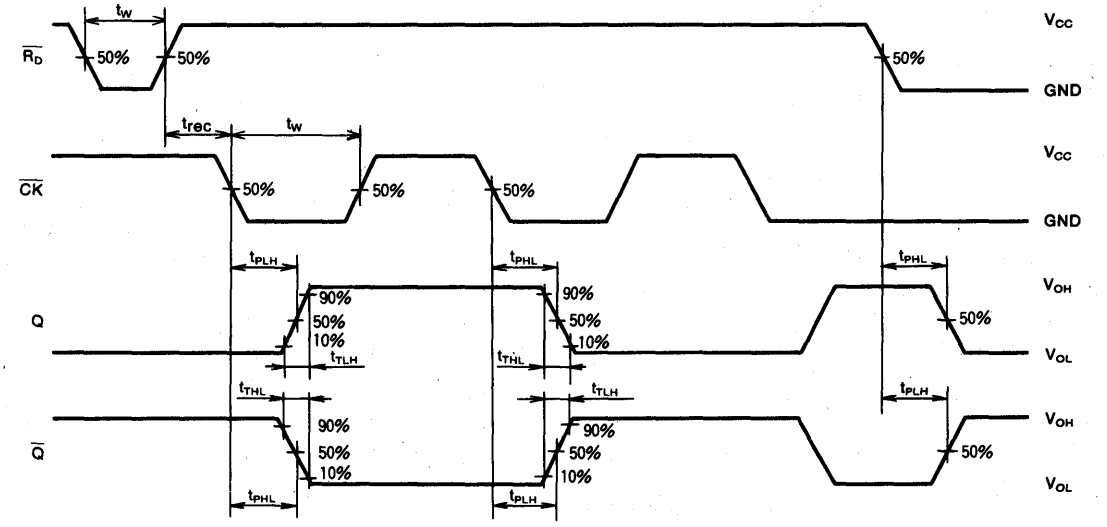
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{R_D}$, recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

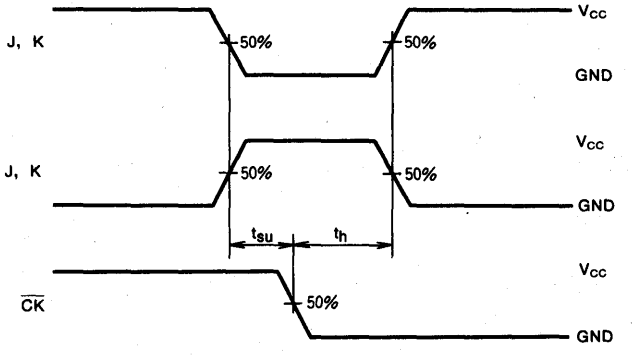
Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC109P/FP/DP

DUAL J-$\overline{K}$ FLIP-FLOP WITH SET AND RESET

DESCRIPTION

The M74HC109 is a semiconductor integrated circuit consisting of two positive-edge triggered J-$\overline{K}$ flip flops with independent control inputs.

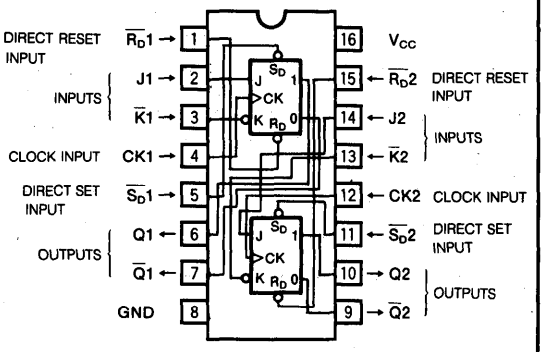
FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N
16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC109 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS109.

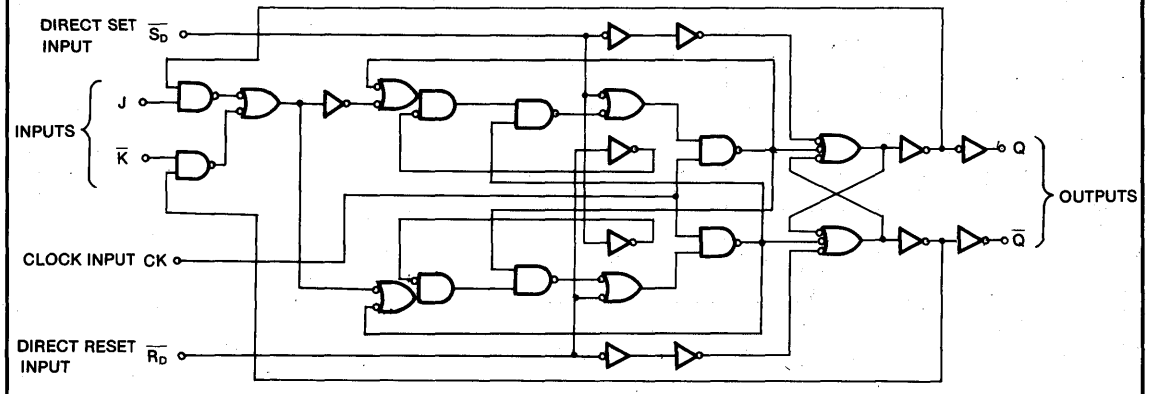
The M74HC109 contains two edge-triddered J-$\overline{K}$ flip flops, each circuit with independent clock input CK, direct set input $\overline{S_D}$, direct reset input $\overline{R_D}$ and both inputs J and $\overline{K}$.

When $\overline{CK}$ is high, the J and K signals can be read.

When CK changes from low-level to high-level, the signals just previously input at J and $\overline{K}$ appear at outputs Q and $\overline{Q}$ in accordance with the function table given. Use of $\overline{S_D}$ and $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined. When used as a J-$\overline{K}$ flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high-level.

Connecting J and $\overline{K}$ will permit the M74HC109 to be used as a D-type flip flop.

LOGIC DIAGRAM (EACH FLIP FLOP)



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FUNCTION TABLE (Note 1)

Inputs					Outputs	
$\overline{S_D}$	$\overline{R_D}$	CK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q^0	$\overline{Q}^0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high
X : Irrelevant
Q^0 : Output state Q before clock input changed
$\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
Toggle : Inversion state before clock input changed
* : When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ become high. when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the outputs of Q and $\overline{Q}$ cannot be predetermined.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Suppl voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC109FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC109DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9			V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (CK − Q, $\overline{Q}$)				30	ns
t_{PLH}	Low-level to high-level and high-level to low-level				40	ns
t_{PHL}	output propagation time ($\overline{S_D}$, $\overline{R_D}$ − Q, $\overline{Q}$)				40	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

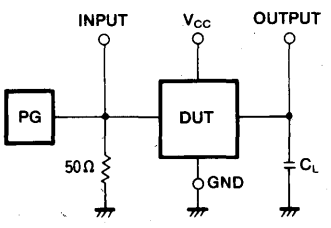
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q, $\overline{Q}$)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$, $\overline{R_D}$ − Q, $\overline{Q}$)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				45				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

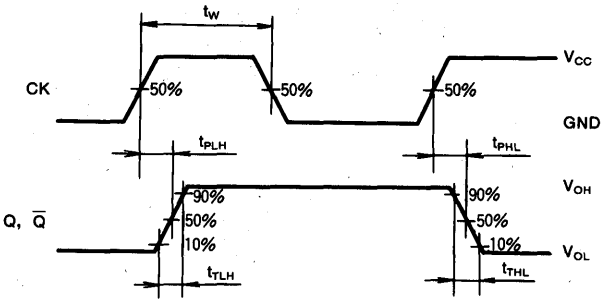
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{S_D}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, $\overline{K}$ setup time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, $\overline{K}$ hold time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		
t_{rec}	$\overline{R_D}$, $\overline{S_D}$ recovery time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

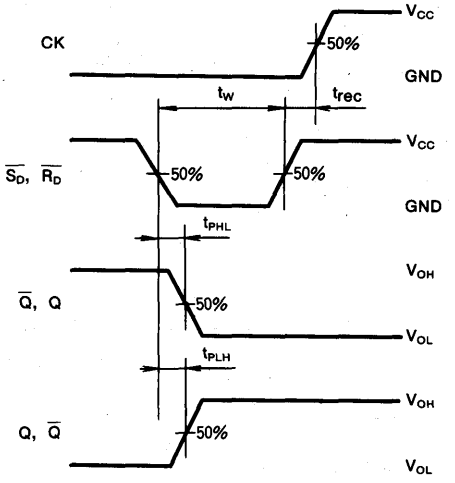
Note 4 : Test Circuit

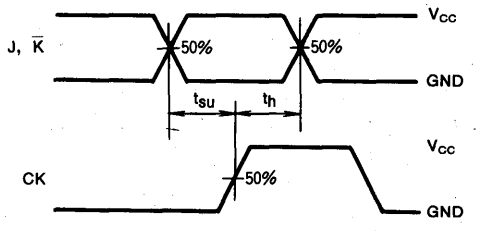


(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







MITSUBISHI ELECTRIC

M74HC112P/FP/DP

DUAL J-K FLIP-FLOP WITH SET AND RESET

DESCRIPTION

The M74HC112 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

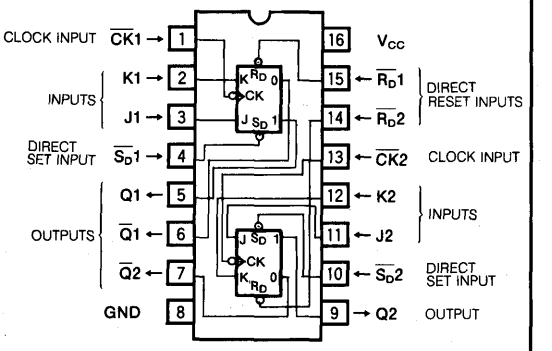
FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC112 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS112.

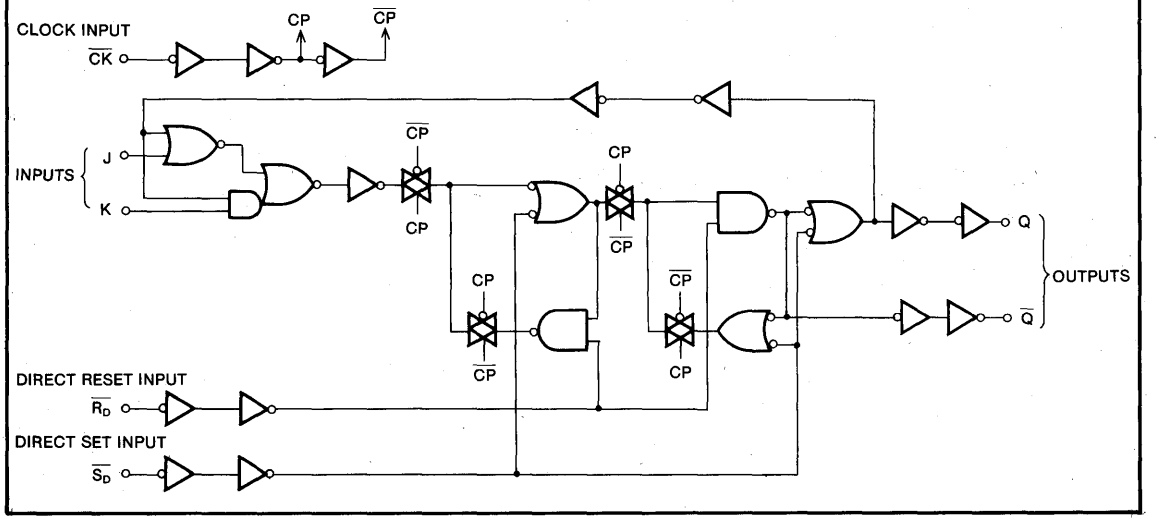
The M74HC112 contains two edge-triggered J-K flip flops, each circuit with independent clock input $\overline{CK}$, direct set input $\overline{S_D}$ and direct reset input $\overline{R_D}$, and both inputs J and K.

When $\overline{CK}$ is high, the J and K signals can be read.

When $\overline{CK}$ changes from high-level to low-level, the signals just previously input at J and K appear at outputs Q and $\overline{Q}$ in accordance with the function table given. Use of $\overline{S_D}$ and $\overline{R_D}$ permits airect R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined. When used as a J-K flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high-level.

M74HC112 is the same functions and electrical characteristics as M74HC76, differing only pin connections.

LOGIC DIAGRAM (EACH FLIP FLOP)



FUNCTION TABLE (Note 1)

Inputs					Outputs	
$\overline{S_D}$	$\overline{R_D}$	$\overline{CK}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q^0	$\overline{Q}^0$
H	H	↓	L	H	L	H
H	H	↓	H	L	H	L
H	H	↓	H	H	Toggle	
H	H	L	X	X	Q^0	$\overline{Q}^0$
H	H	H	X	X	Q^0	$\overline{Q}^0$
H	H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high
↓ : Change from high to low
X : Irrelevant
Q^0 : Output state before clock input changed
$\overline{Q}^0$: Output state before clock input changed
Toggle : Inversion state before clock input changed
* : When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ both becomes high. When $\overline{S_D}$ and $\overline{R_D}$ becomes high, simultaneously, the condition of Q and $\overline{Q}$ cannot be predetermined.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC112FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC112DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0		−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0		2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)				26	ns
t_{PLH}	Low-level to high-level and high-level to low-level				31	ns
t_{PHL}	output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)				31	ns
t_{PLH}	Low-level to high-level and high-level to low-level				31	ns
t_{PHL}	output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)				31	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

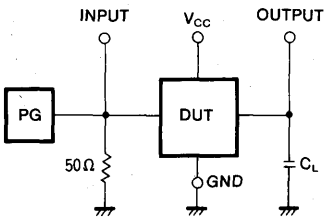
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PHL}			2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)		2.0			180		225	ns
			4.5			36		45	
			6.0			31		38	
t_{PHL}			2.0			180		225	ns
			4.5			36		45	
			6.0			31		38	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)		2.0			180		225	ns
			4.5			36		45	
			6.0			31		38	
t_{PHL}			2.0			180		225	ns
			4.5			36		45	
			6.0			31		38	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				55				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

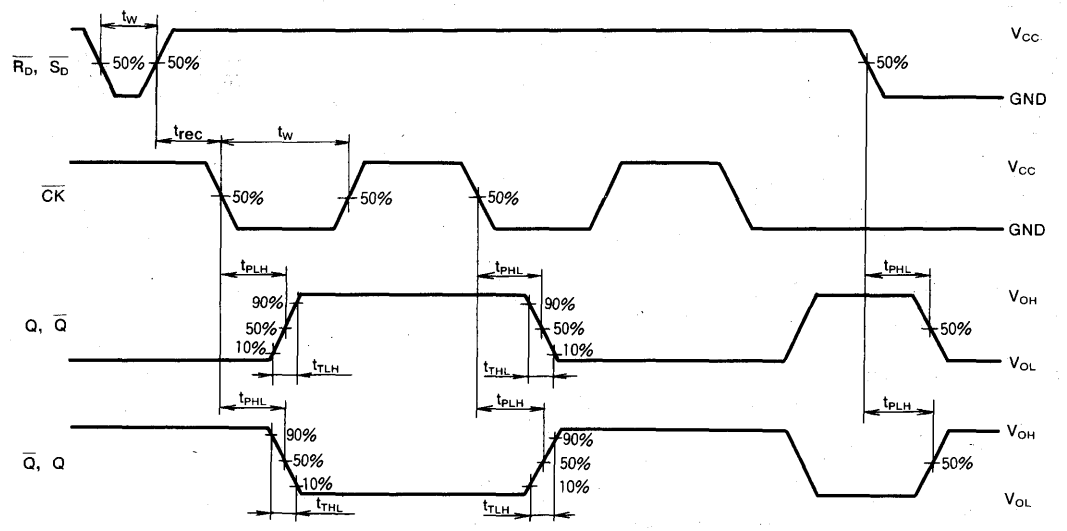
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{S_D}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{R_D}$, $\overline{S_D}$ recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

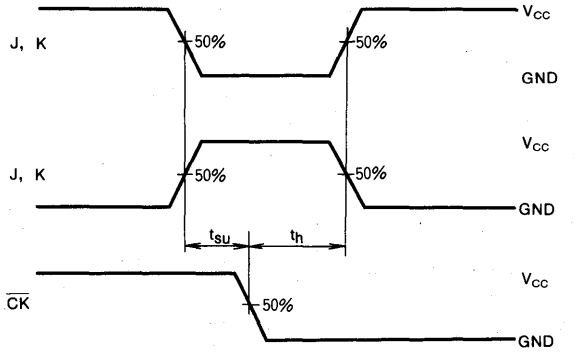
Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC113P/FP/DP

DUAL J-K FLIP-FLOP WITH SET

DESCRIPTION

The M74HC113 is a semiconductor integrated circuit consisting of of two negative-edge triggered J-K flip flops with independent control inputs.

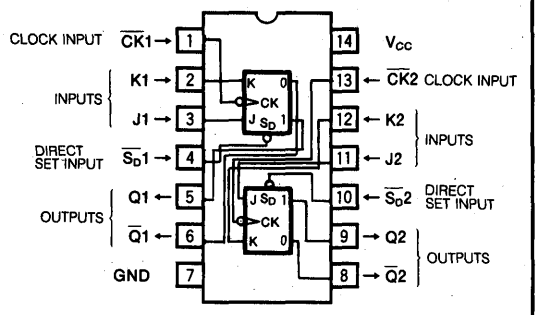
FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

FUNCTIONAL DESCRIPTION

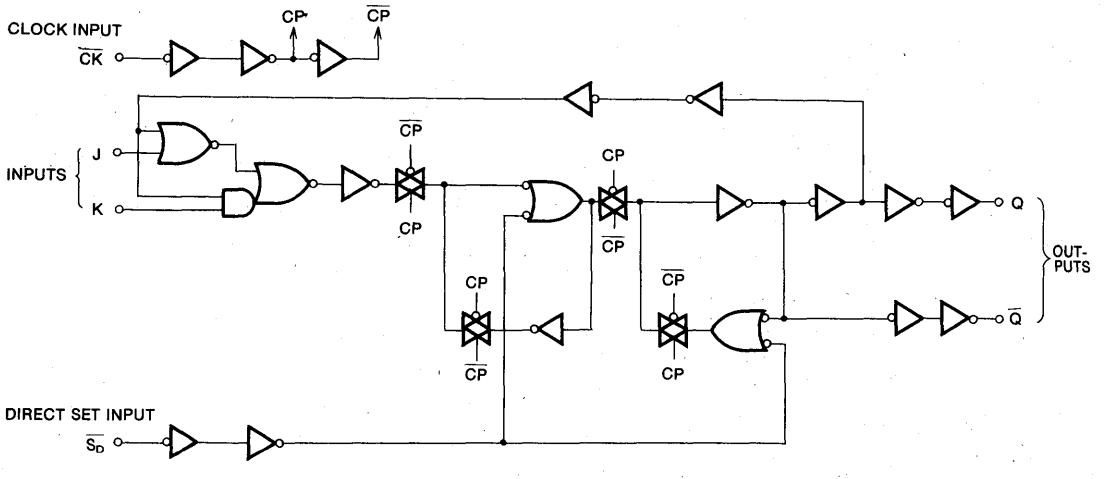
Use of silicon gate technology allows the M74HC113 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS113.

The M74HC113 contains two edge-triggered J-K flip flops, each circuit with independent clock input $\overline{CK}$, direct set input $\overline{S_D}$, and both inputs J and K.

When $\overline{CK}$ is high, the J and K signals can be read.

When $\overline{CK}$ changes from high-level tb low-level, the signals just previously input at J and K appear at outputs Q and $\overline{Q}$ in accordance with the function table given. When $\overline{S_D}$ is low, Q and $\overline{Q}$ will become high and low respectively, irrespective of other inputs. When used as a J-K flip flop, $\overline{S_D}$ should be maintained at high-level.

LOGIC DIAGRAM (EACH FLIP FLOP)



MITSUBISHI ELECTRIC

FUNCTION TABLE (Note 1)

Inputs				Outputs	
$\overline{S_D}$	$\overline{CK}$	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q^0	$\overline{Q}^0$
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	H	H	Toggle	
H	L	X	X	Q^0	$\overline{Q}^0$
H	H	X	X	Q^0	$\overline{Q}^0$
H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high
↓ : Change from high to low
X : Irrelevant
Q^0 : Output state before clock input changed
$\overline{Q}^0$: Output state before clock input changed
Toggle : Inversion state before clock input changed

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC113FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC113DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9			V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0		−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0		2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)				21	ns
t_{PHL}					21	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)				26	ns
t_{PHL}					26	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

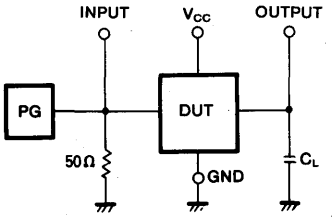
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)		2.0			126		160	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			126		160	ns
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)		2.0			165		210	ns
			4.5			33		41	
			6.0			28		35	
t_{PHL}			2.0			165		210	ns
			4.5			33		41	
			6.0			28		35	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				52				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

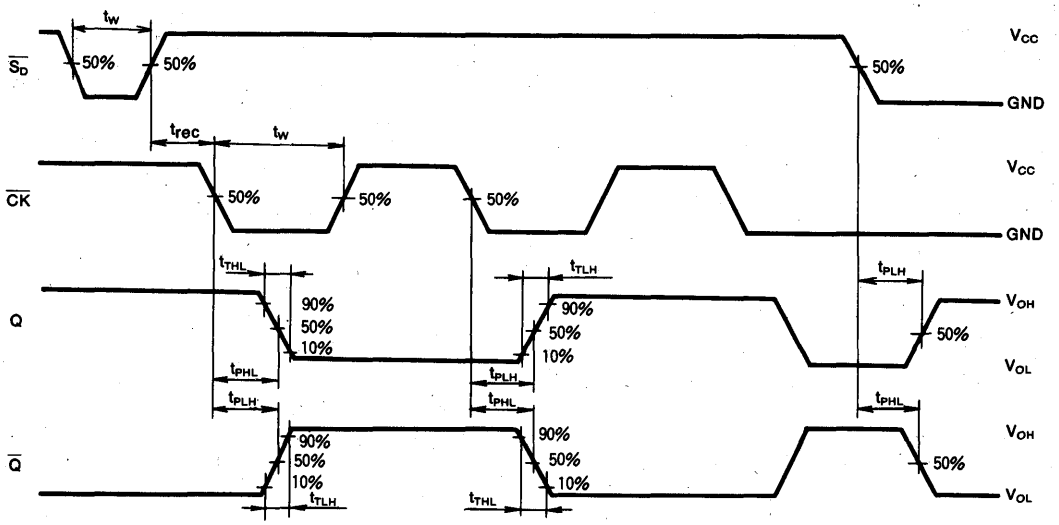
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{S_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{S_D}$ recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

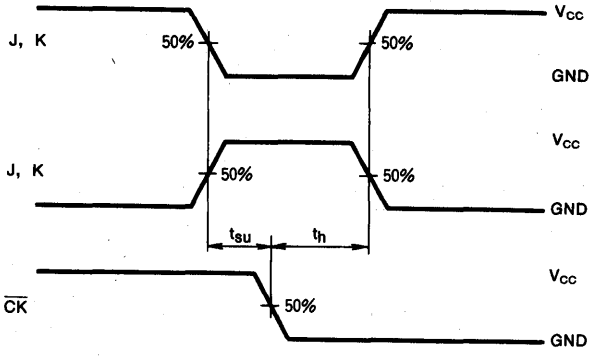
Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





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M74HC114P/FP/DP

DUAL J-K FLIP-FLOP WITH SET AND COMMON RESET

DESCRIPTION

The M74HC114 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

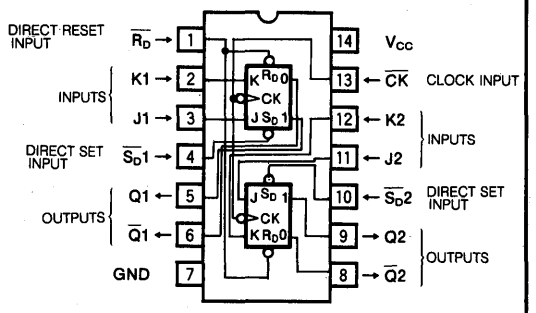
FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



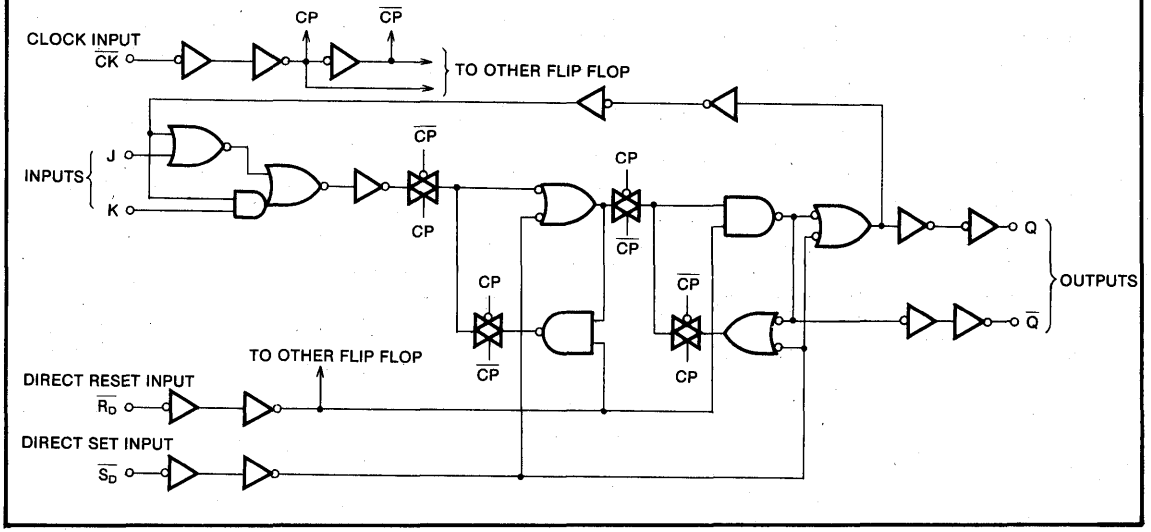
Outline 14P4, 14P2N, 14P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC114 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS114.

The M74HC114 contains two edge-triggered J-K flip flops, each circuit with independent direct set input $\overline{S_D}$, inputs J and K, common clock input $\overline{CK}$, and direct reset input $\overline{R_D}$. When $\overline{CK}$ is high, the J and K signals can be read. When $\overline{CK}$ changes from high-level to low-level, the signals just previously input at J and K appear at outputs Q and $\overline{Q}$ in accordance with the function table given. Use of $\overline{S_D}$ and $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined. When used as a J-K flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high.

LOGIC DIAGRAM (EACH FLIP FLOP)



DUAL J-K FLIP-FLOP WITH SET AND COMMON RESET

FUNCTION TABLE (Note 1)

Inputs					Outputs	
$\overline{S_D}$	$\overline{R_D}$	$\overline{CK}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q^0	$\overline{Q}^0$
H	H	↓	L	H	L	H
H	H	↓	H	L	H	L
H	H	↓	H	H	Toggle	
H	H	L	X	X	Q^0	$\overline{Q}^0$
H	H	H	X	X	Q^0	$\overline{Q}^0$
H	H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high
↓ : Change from high to low
X : Irrelevant
Q^0 : Output state before clock input changed
$\overline{Q}^0$: Output state before clock input changed
Toggle : Inversion state before clock input changed
* : When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will both become high. When $\overline{S_D}$ and $\overline{R_D}$ become high simultaneously, the condition of Q and $\overline{Q}$ cannot be predetermined.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC114FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC114DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0		−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0		2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)				26	ns
t_{PHL}					26	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)				31	ns
t_{PHL}					31	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)				31	ns
t_{PHL}					31	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

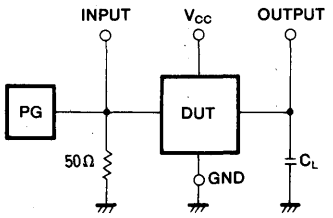
Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PHL}			2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)		2.0			180		225	ns
			4.5			36		45	
			6.0			31		38	
t_{PHL}			2.0			180		225	ns
			4.5			36		45	
			6.0			31		38	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)		2.0			180		225	ns
			4.5			36		45	
			6.0			31		38	
t_{PHL}			2.0			180		225	ns
			4.5			36		45	
			6.0			31		38	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				95				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

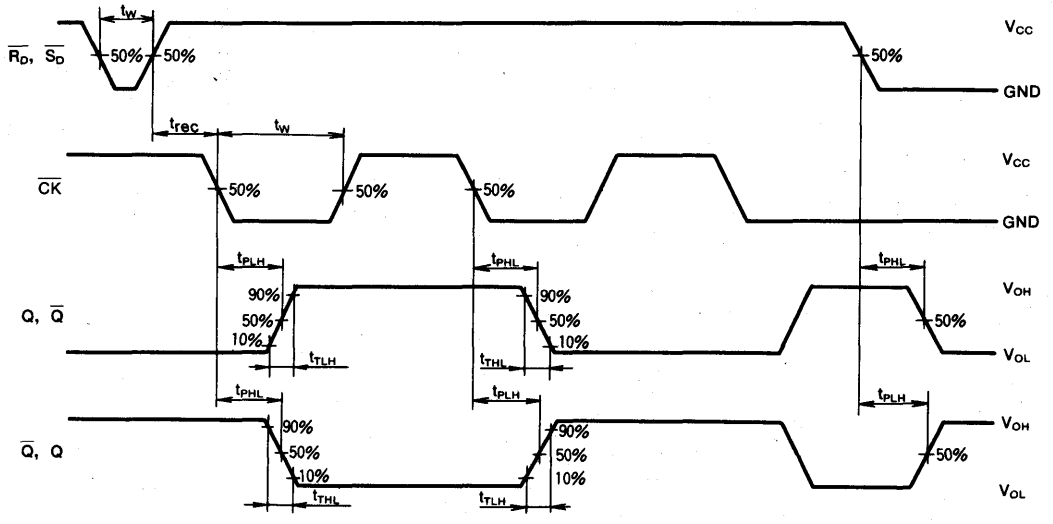
Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{S_D}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{R_D}$, $\overline{S_D}$ recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

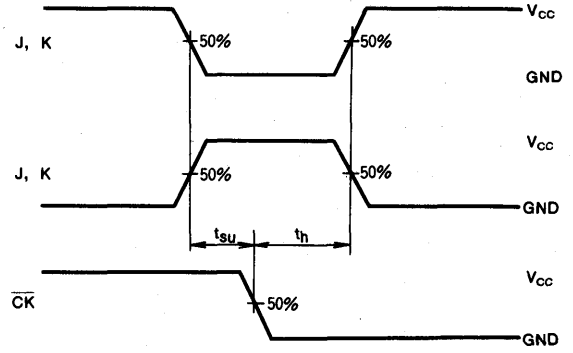
Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC123P/FP/DP

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION

The M74HC123 is a semiconductor integrated circuit consisting of two retriggerable monostable multivibrators with direct reset inputs.

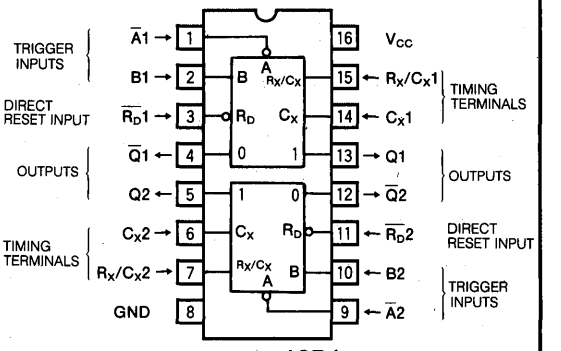
FEATURES

- Retriggerable multivibrator can generate wide output pulses.
- Direct reset input can interrupt output pulses.
- High-speed: 28ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



16P4
Outline 16P2N
16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC123 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS123.

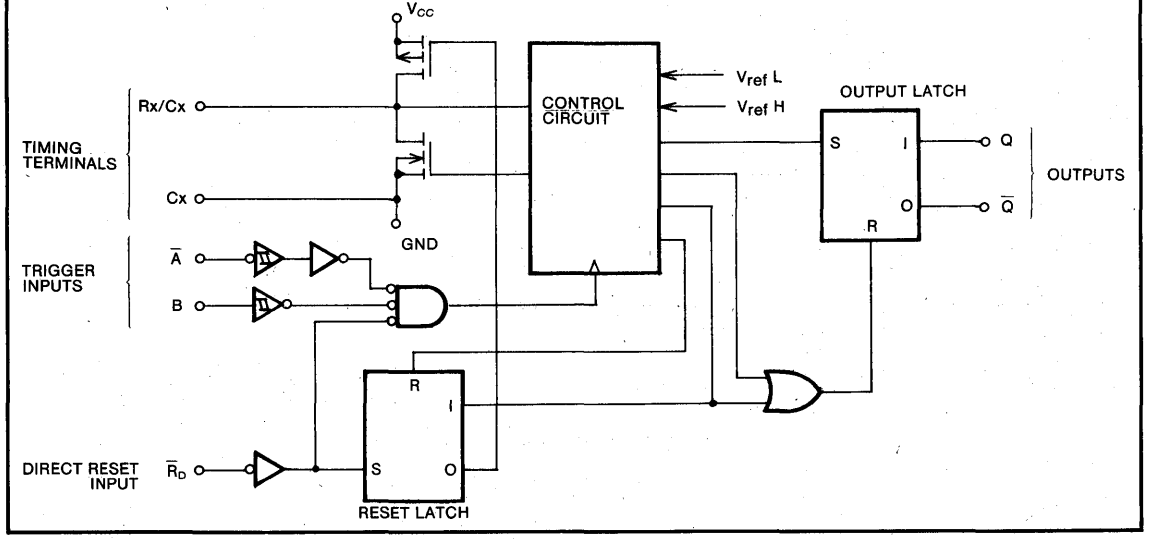
When external resistor R_X and electrostatic capacitor C_X are connected to timing terminals R_X/C_X and C_X as shown in Fig. 1, and trigger pulses are applied at inputs $\overline{A}$ or B, positive pulses will appear at Q and negative pulses at $\overline{Q}$. (Fig. 2-(a))

The pulse width t_{WQ} is set by R_X and C_X. The trigger is applied when $\overline{A}$ changes from high-level to low-level or when B changes from low-level to high-level. The retrigger function is used to obtain longer pulse width and output pulses can be extended by retriggering at $\overline{A}$ or B before the output pulse is completed. (Fig. 2-(b))

When direct reset input $\overline{R_D}$ is set low, Q will be reset low and $\overline{Q}$ will be reset high, irrespective of the output state, allowing output pulses to be narrower by $\overline{R_D}$. (Fig. 2-(c))

When $\overline{R_D}$ changes from low-level to high-level while A is low and B is high, the trigger is applied and Q and $\overline{Q}$ change state.

LOGIC DIAGRAM (EACH MONOSTABLE MULTIVIBRATOR)



MITSUBISHI ELECTRIC

FUNCTION TABLE (Note 1)

Inputs			Outputs	
$\overline{R_D}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
⎍ : Positive one-shot operation
⎎ : Negative one-shot operation
X : Irrelevant

OPERATION

1. How to use the timing terminals

Resistor R_X and capacitor C_X are connected to timing terminals R_X/C_X and C_X, as shown in Fig. 1. If C_X is polar, the positive lead should be connected to the R_X/C_X side, and the negative lead to the C_X side. A diode is connected to prevent latchup.

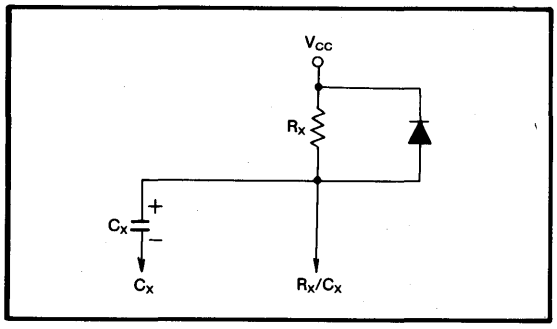


Fig.1 Connection of external resistor R_X and capacitor C_X to timing terminals R_X/C_X and C_X

2. Output Pulse Width t_{WQ}

The output pulse width t_{WQ} is determined as follows:
When $C_X > 100000pF$, $R_X \geqq 10k\Omega$
$t_{WQ} = 0.46C_X \cdot R_X$ (ns)
C_X is given in pF, and R_X in kΩ.

3. Output Pulse Width Control

The output pulse width can be controlled in the following three ways.

3—1 Normal Use

Fig. 2-(a) is the directions as ordinary monostable multivibrator operation and the output pulse width t_{WQ} can be set by using the formula and figure shown in section 2 above.

3—2 Extendtion of the output pulse width with retrigger function

As shown in Fig. 2-(b), the output pulse width can be extended at will by applying additional trigger pulses before the output is completed.

3—3 Shortening of the output pulse width with $\overline{R_D}$ signal

As shown in Fig. 2-(c), the output pulse which has been generated by the trigger signal can be terminated with the $\overline{R_D}$ signal and it is possible to shorten its width as reguired.

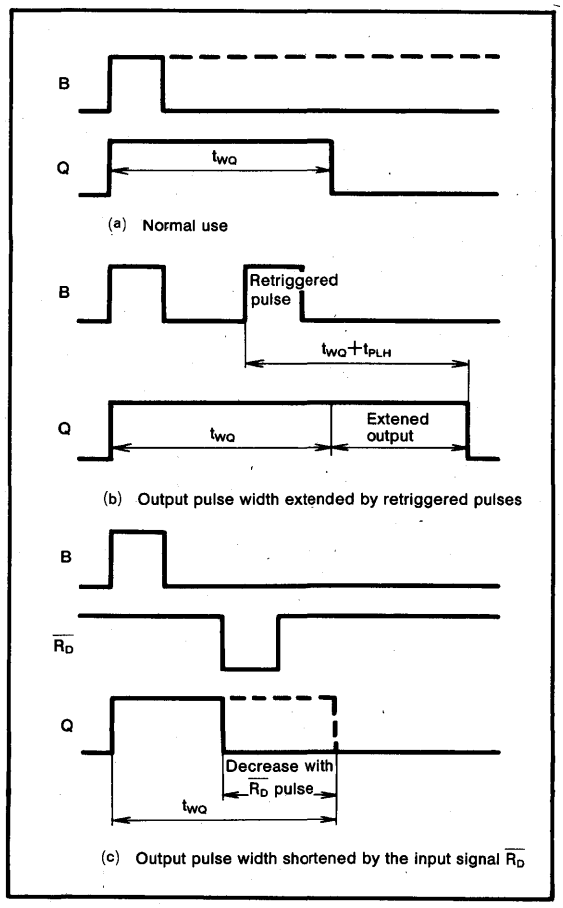


Fig.2 Output pulse width control

4. Precations for Use

4−1 Additional trigger pulses must be applied at least trr later after the previous trigger pulse has been applied. The retrigger pulse during this period is ineffective.

4−2 The lead length of external resistor R_X and capacitor C_X should be as short as possible (less than 3cm) to minimize stray wiring capacitance and to prevent misoperation due to noise. Care should also be taken to isolate this circuit from noise sources as far as possible.

4−3 Insert a capacitor of 0.01 ~ 0.1μF with good high-frequency characteristics between V_{CC} and GND.

4−4 Output pulses may be generated when the power is switched on.

4−5 Capacitor discharge when the power is turned off may cause thermal breakdown or latchup, so a diode should be connected as shown in Fig. 1.

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC123FP, T_a = −40~+70℃ and T_a = 70~85℃ are derated at −6mW/℃.
M74HC123DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime ($\overline{A}$, B)		no restriction			ns
	Input risetime, falltime ($\overline{R_D}$)	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	
R_X	External timing resistance	V_{CC}=2.0V	5		1000	kΩ
		V_{CC}≧3.0V	1		1000	
C_X	External timing capacitance		no restriction			F

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current ($\overline{A}$, B, $\overline{R_D}$)	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current ($\overline{A}$, B, $\overline{R_D}$)	V_I = 0V		6.0			−0.1		−1.0	μA
I_{IH}	High-level input current (R_X/C_X)	V_I = 6V		6.0			0.5		5.0	μA
I_{IL}	Low-level input current (R_X/C_X)	V_I = 0V		6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA
I_{CC}	Active supply current	V_I = V_{CC}, GND, R_X/C_X = 0.5V_{CC}		2.0			120		160	μA
				4.5			300		400	
				6.0			600		800	

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L=15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				43	ns
t_{PHL}	output propagation time ($\overline{A}$, B−Q, $\overline{Q}$)				43	ns
t_{PLH}	Low-level to high-level and high-level to low-level				46	ns
t_{PHL}	output propagation time (Trigger input)($\overline{R_D}$−Q, $\overline{Q}$)				46	ns
t_{PLH}	Low-level to high-level and high-level to low-level				35	ns
t_{PHL}	output propagation time (Reset input)($\overline{R_D}$−Q, $\overline{Q}$)				35	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

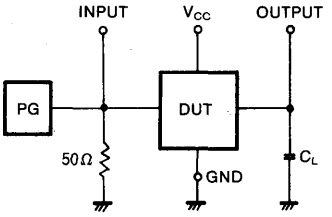
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{A}$, B−Q, $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			240		300	ns
			4.5			48		60	
			6.0			41		51	
t_{PHL}			2.0			240		300	ns
			4.5			48		60	
			6.0			41		51	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (Trigger input) ($\overline{R_D}$−Q, $\overline{Q}$)		2.0			265		330	ns
			4.5			53		66	
			6.0			45		55	
t_{PHL}			2.0			265		330	ns
			4.5			53		66	
			6.0			45		55	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (Reset input) ($\overline{R_D}$−Q, $\overline{Q}$)		2.0			195		245	ns
			4.5			39		49	
			6.0			33		42	
t_{PHL}			2.0			195		245	ns
			4.5			39		49	
			6.0			33		42	
Δt_{WQ}	Pulse width difference between circuits in the same package								%
t_{WQ} (MIN)	Minimum output pulse width	C_X=0pF (Note 4)	2.0			1000		1250	ns
		R_X=5kΩ (V_{CC}=2V)	4.5			200		250	
		R_X=1kΩ (V_{CC}=4.5, 6V)	6.0			180		230	
t_{WQ}	Output pulse width	C_X=100pF	2.0	47		67		67	μs
		R_X=10kΩ	4.5	47		57		57	
		C_L=50pF (Note 4)	6.0	47		57		57	
		C_X=0.1μF	2.0	0.42		0.54	0.42	0.50	ms
		R_X=10kΩ	4.5	0.42		0.50	0.42	0.50	
		C_L=50pF (Note 4)	6.0	0.42		0.50	0.42	0.50	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIERMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

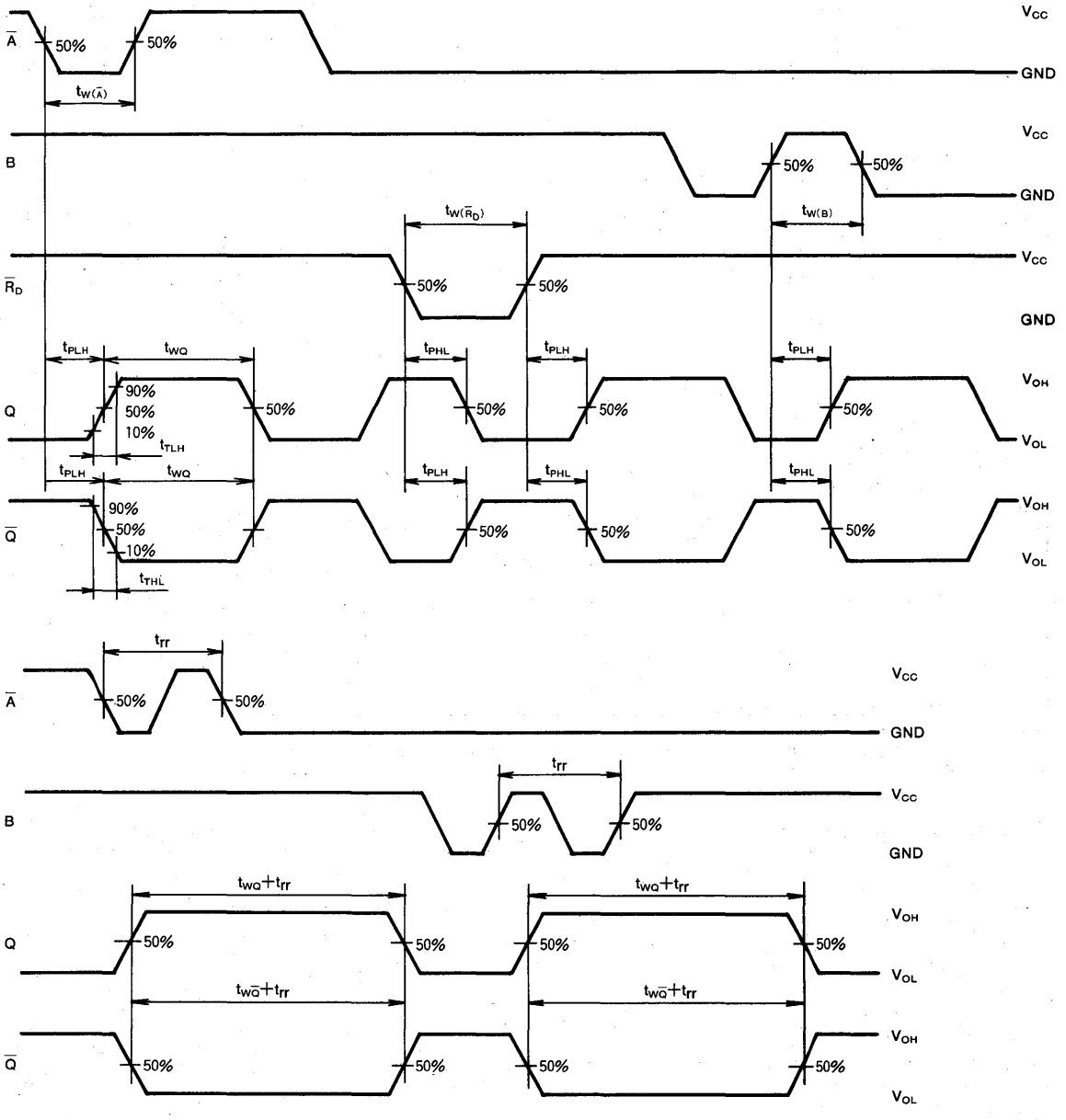
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W ($\overline{A}$, B)	Minimum trigger pulse width		2.0			100		120	ns
			4.5			20		24	
			6.0			17		21	
t_W ($\overline{R_D}$)	Minimum direct reset pulse width		2.0			75		90	ns
			4.5			15		18	
			6.0			13		16	
trr	Minimum retrigger time	C_X=100pF	4.5						ns
		R_X=1kΩ	6.0						
		C_X=0.1μF	4.5						ns
		R_X=1kΩ	6.0						

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC125P/FP/DP

QUADRUPLE 3-STATE NONINVERTING BUFFER

DESCRIPTION

The M74HC125 is a semiconductor integrated circuit consisting of four buffers each with 3-state noninverted outputs and independent output-enable inputs.

FEATURES

- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC125 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS125.

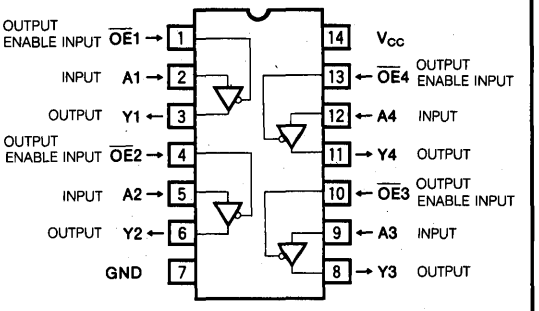
When output-enable input $\overline{OE}$ is low and input A is high then output Y will become high. However, if A is low then Y will become low. When $\overline{OE}$ is high then Y will become high-impedance state, irrespective of A, making the device suitable for a bus line driver.

FUNCTION TABLE (Note 1)

Inputs		Output
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

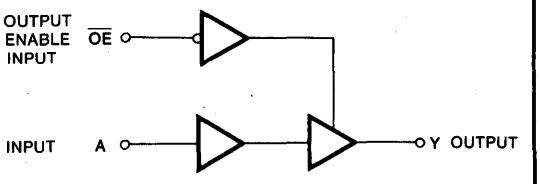
Note 1 : X : Irrelevant
Z : High impedance

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

LOGIC DIAGRAM (EACH BUFFER)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC125FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC125DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}; I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −6.0mA	4.5	4.18			4.13		
		I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IL}; I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 6.0mA	4.5			0.26		0.33	
		I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}	6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND	6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

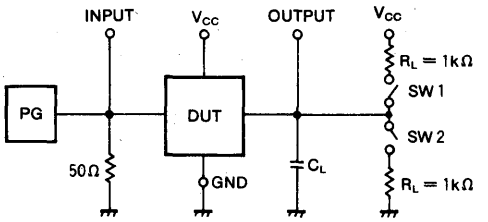
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A—Y)				18	ns
t_{PHL}					18	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$—Y)	C_L = 5pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$—Y)	C_L = 50pF (Note 4)			25	ns
t_{PZH}					25	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)	C_L = 50pF (Note 4)	2.0			100		125	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		125	ns
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 4)	2.0			130		163	ns
			4.5			26		33	
			6.0			22		28	
t_{PHL}			2.0			130		163	ns
			4.5			26		33	
			6.0			22		28	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)	2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
t_{PHZ}			2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)	2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
t_{PZH}			2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
t_{PZL}		C_L = 150pF (Note 4)	2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
t_{PZH}			2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				42				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

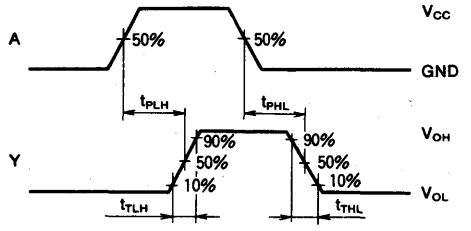
Note 4 : Test Circuit

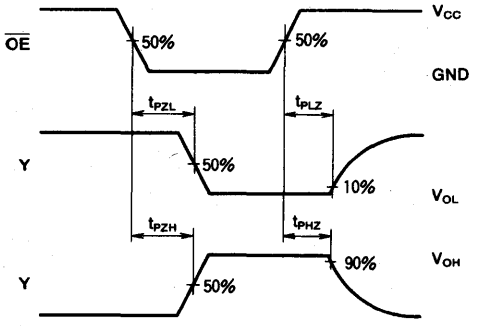


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC126P/FP/DP

QUADRUPLE 3-STATE NONINVERTING BUFFER

DESCRIPTION

The M74HC126 is a semiconductor integrated circuit consisting of four buffers each with 3-state noninverted outputs and independent output-enable inputs.

FEATURES

- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC126 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS126.

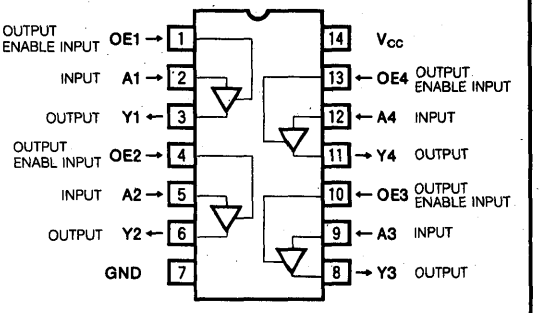
When output-enable input OE is high and input A is high then output Y will become high. However, if A is low then Y will become low. When OE is low then Y will become high-impedance state, irrespective of A, making the device suitable for a bus line driver.

FUNCTION TABLE (Note 1)

Inputs		Output
OE	A	Y
H	L	L
H	H	H
L	X	Z

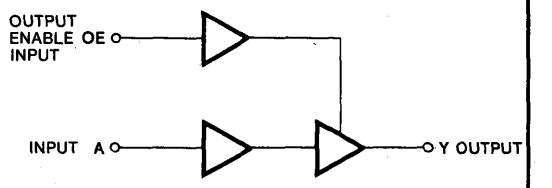
Note 1 : X : Irrelevant
Z : High impedance

PIN CONFIGURATION (TOP VIEW)



Outline 14P4
14P2N
14P2P

LOGIC DIAGRAM (EACH BUFFER)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC126FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC126DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

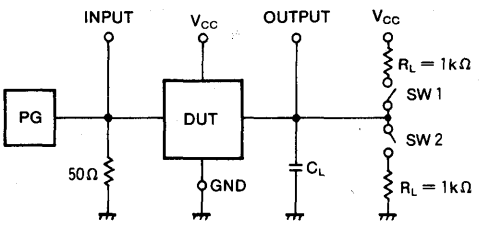
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A—Y)				18	ns
t_{PHL}					18	ns
t_{PLZ}	Output disable time from low-level and high-level (OE—Y)	C_L = 5pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level (OE—Y)	C_L = 50pF (Note 4)			25	ns
t_{PZH}					25	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A—Y)	C_L = 50pF (Note 4)	2.0			100		125	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		125	ns
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 4)	2.0			130		163	ns
			4.5			26		33	
			6.0			22		28	
t_{PHL}			2.0			130		163	ns
			4.5			26		33	
			6.0			22		28	
t_{PLZ}	Output disable time from low-level and high-level (OE—Y)	C_L = 50pF (Note 4)	2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
t_{PHZ}			2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
t_{PZL}	Output enable time to low-level and high-level (OE—Y)	C_L = 50pF (Note 4)	2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
t_{PZH}			2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
t_{PZL}		C_L = 150pF (Note 4)	2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
t_{PZH}			2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	OE = GND				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				43				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

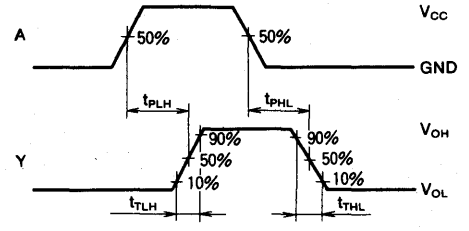
Note 4 : Test Circuit

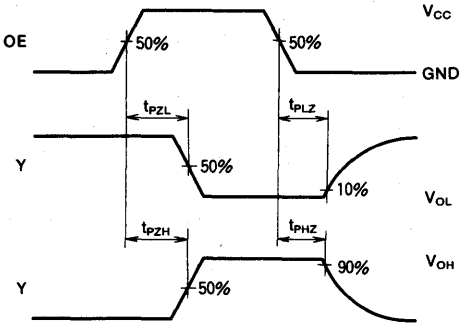


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC132P/FP/DP

QUADRUPLE 2-INPUT SCHMITT-TRIGGER POSITIVE NAND GATE

DESCRIPTION

The M74HC132 is a semiconductor integrated circuit consisting of four 2-input Schmitt-trigger positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High-speed: 13ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range : V_{CC} =2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

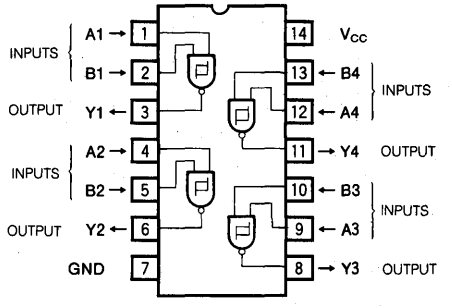
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC132 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS132.

Built-in Schmitt-trigger circuits prevent the occurrence of incorrect oscillations even when input signals having slow rise and fall times are applied. The Schmitt triggers ensure a signal of restored waveshape will appear at the output.

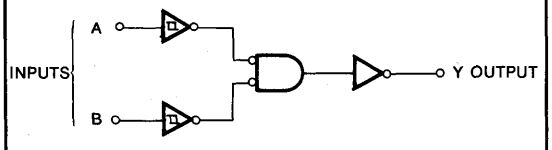
When both A and B inputs are high, the output Y will become low, and when at least one of the inputs is low, the output Y will become high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

LOGIC DIAGRAM (EACH SCHMITT-TRIGGER)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC132FP, T_a = −40~+65℃ and T_a = 65~85℃ are derated at −6mW/℃.
M74HC132DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

QUADRUPLE 2-INPUT SCHMITT-TRIGGER POSITIVE NAND GATE

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature range	−40		+85	℃
t_r, t_f	Input risetime, falltime	No restriction			—

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
					25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{T+}	Positive-going threshold voltage	V_O = 0.1V, V_{CC} − 0.1V $\|I_O\|$ = 20μA		2.0	0.7		1.5	0.7	1.5	V
				4.5	1.55		3.15	1.55	3.15	
				6.0	2.1		4.2	2.1	4.2	
V_{T-}	Negative-going threshold voltage	V_O = V_{CC} − 0.1V $\|I_O\|$ = 20μA		2.0	0.3		1.0	0.3	1.0	V
				4.5	0.9		2.45	0.9	2.45	
				6.0	1.2		3.2	1.2	3.2	
V_H	Hysteresis voltage	V_O = 0.1V, V_{CC} − 0.1V $\|I_O\|$ = 20μA		2.0	0.2		1.2	0.2	1.2	V
				4.5	0.4		2.1	0.4	2.1	
				6.0	0.5		2.5	0.5	2.5	
V_{OH}	High-level output voltage	V_I = V_{T+}, V_{T-}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{T+}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiecent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

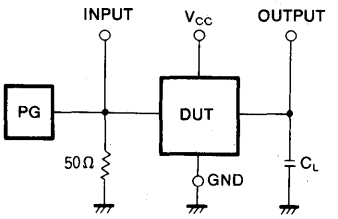
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				22	ns
t_{PHL}					22	

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40∼+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
				25℃		−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				37				pF

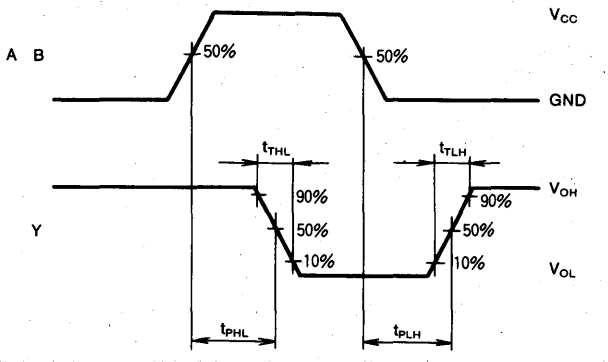
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC} \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%∼90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC133P/FP/DP

13-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC133 is a semiconductor integrated circuit consisting of a 13-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High-speed: 20ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

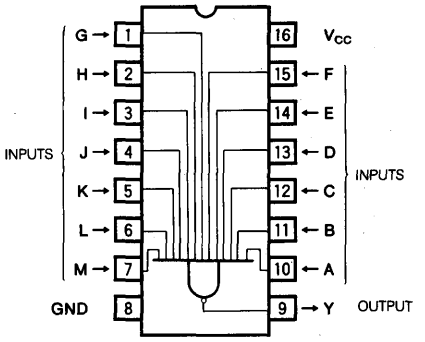
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC133 to maintain the low power dissipation and high noise margin of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS133.

Buffered output Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When inputs A through M are all high, the output Y will become low and when at least one of A through M is low, the output Y will become high.

PIN CONFIGURATION (TOP VIEW)



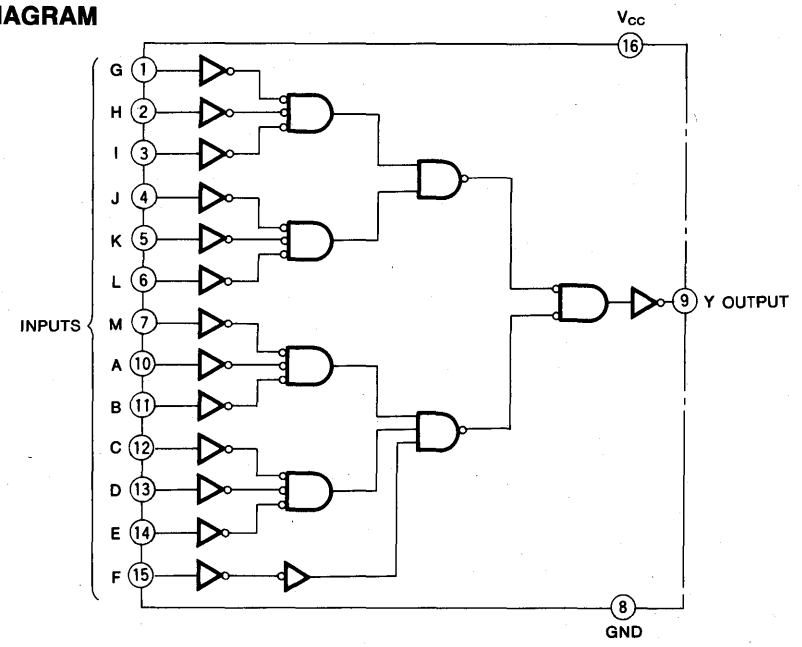
Outline 16P4, 16P2N, 16P2P

FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

N = B·C·D·E·F·G·H·I·J·K·L·M

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 1 : M74HC133FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC133DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

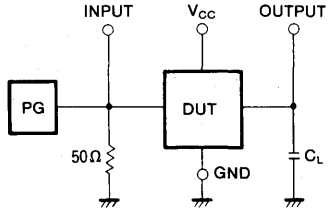
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B, C, D, E, F, G, H, I, J, K, L or M − Y)				30	ns
t_{PHL}					30	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B, C, D, E, F, G, H, I, J, K, L or M − Y)		2.0			160		190	ns
			4.5			35		42	
			6.0			30		36	
t_{PHL}			2.0			160		190	ns
			4.5			35		42	
			6.0			30		36	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				32				pF

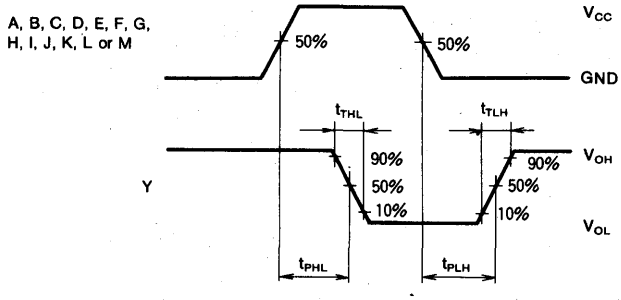
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC137P/FP/DP

1-OF-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

DESCRIPTION

The M74HC137 is a semiconductor integrated circuit consisting of a 3-bit binary to 8-line decoder/demultiplexer with address latch.

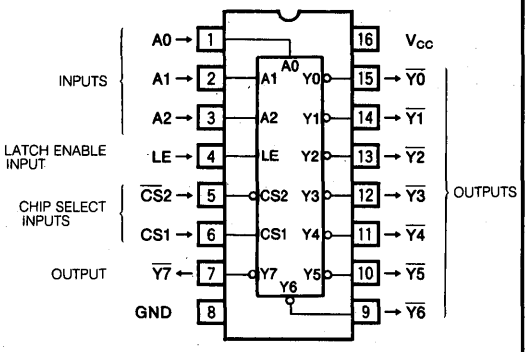
FEATURES

- Built-in address latch
- High-speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N
16P2P

FUNCTIONAL DESCRIPTION

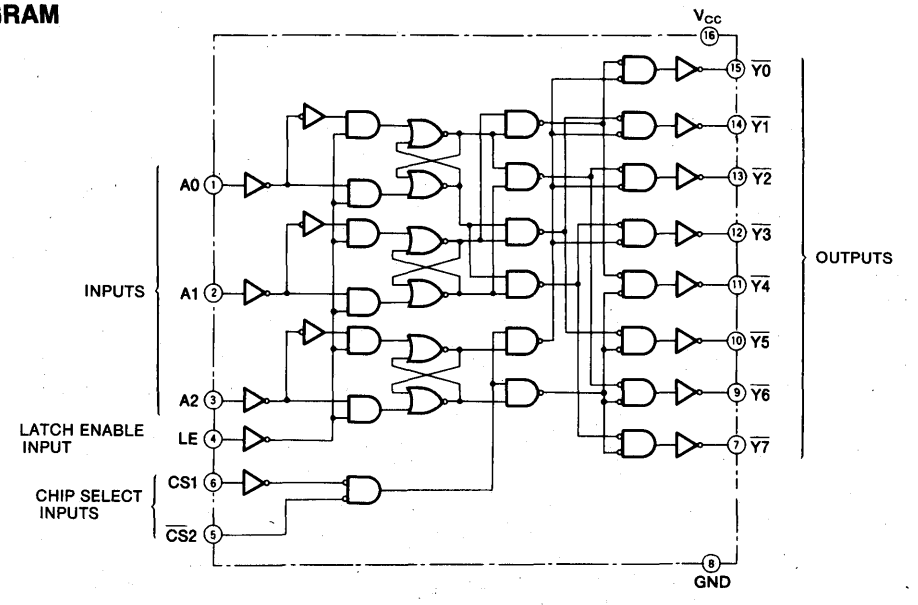
Use of silicon gate technology allows the M74HC137 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS137.

The M74HC137 consists of a 3-bit binary to 8-line decoder/demultiplexer with an address latch to store the signals of inputs A0 through A2. When latch-enable input LE is low, a 3-bit binary code is applied to inputs A0 through A2 goes through the latch and becomes a code input signal. In this case, one of outputs $\overline{Y0}$ through $\overline{Y7}$ corresponding to this value will become low and the other outputs will all become high. In this case, chip select inputs CS1 and $\overline{CS2}$ should be maintained at high and low, respectively. When CS1 and $\overline{CS2}$ are in conditions other than those given above, all outputs will become high.

When LE is high, the A0 through A2 signals exisiting immediately prior to the high-level setting will be stored in the latch. In this case, those stored contens will not change even if A0 through A2 are changed.

When operated as a 1-of-8 demultiplexer, CS1 or $\overline{CS2}$ is used as a data input and A0 through A2 are used as selecting inputs.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

FUNCTION TABLE (Note 1)

Inputs						Outputs							
LE	CS1	$\overline{CS2}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	$\overline{Y0}^0$	$\overline{Y1}^0$	$\overline{Y2}^0$	$\overline{Y3}^0$	$\overline{Y4}^0$	$\overline{Y5}^0$	$\overline{Y6}^0$	$\overline{Y7}^0$

Note 1 : X : Irrelevant
$\overline{Y}^0$: Output state $\overline{Y}$ before LE changed to high level.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC137FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC137DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)				29	ns
t_{PHL}					42	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS2}$ − $\overline{Y}$)				22	ns
t_{PHL}					34	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CS1 − $\overline{Y}$)				25	ns
t_{PHL}					34	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − $\overline{Y}$)				30	ns
t_{PHL}					44	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

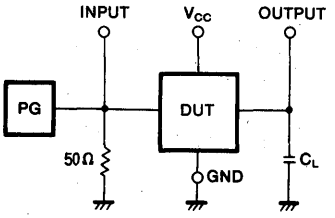
Symbol	Parameter	Test conditions	V_{CC}(V)	Limits 25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)		2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			240		302	ns
			4.5			48		60	
			6.0			41		51	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS2}$ − $\overline{Y}$)		2.0			130		164	ns
			4.5			26		33	
			6.0			22		28	
t_{PHL}			2.0			195		246	ns
			4.5			39		49	
			6.0			33		42	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CS1 − $\overline{Y}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			195		246	ns
			4.5			39		49	
			6.0			33		42	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − $\overline{Y}$)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			250		315	ns
			4.5			50		63	
			6.0			43		54	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				108				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

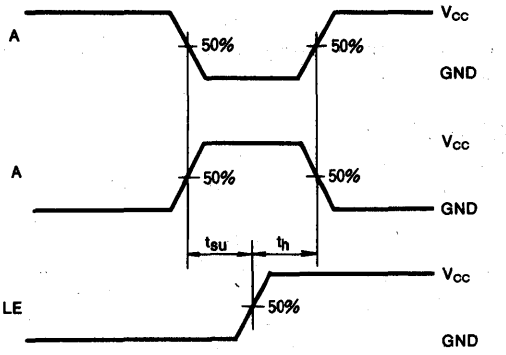
TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	Limits 25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
t_W	LE pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	A setup time with respect to LE		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	A hold time with respect to LE		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		

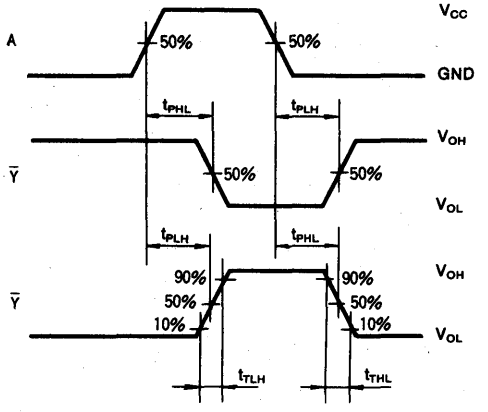
Note 4 : Test Circuit

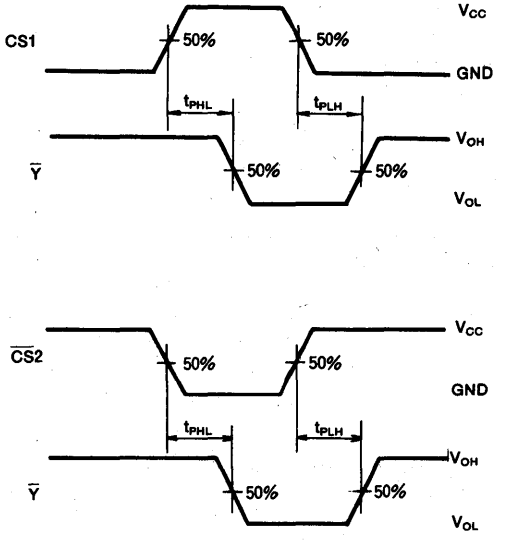


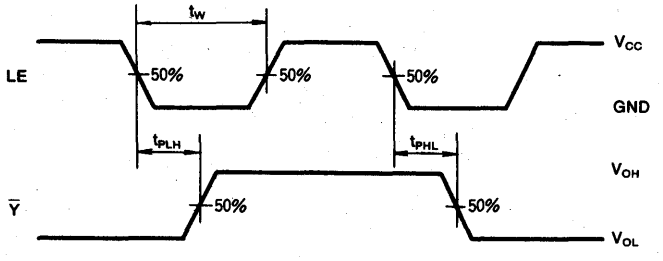
(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



TIMING DIAGRAM







M74HC138P/FP/DP

1-OF-8 DECODER/DEMULTIPLEXER

DESCRIPTION

The M74HC138 is a semiconductor integrated circuit consisting of a 3-bit binary to 8-line decoder/demultiplexer with chip select inputs.

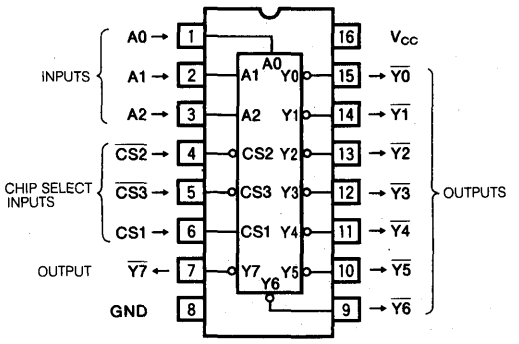
FEATURES

- Three types of chip select inputs
- Expandable to 24 outputs without extenally connected components
- High-speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N
16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC138 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS138.

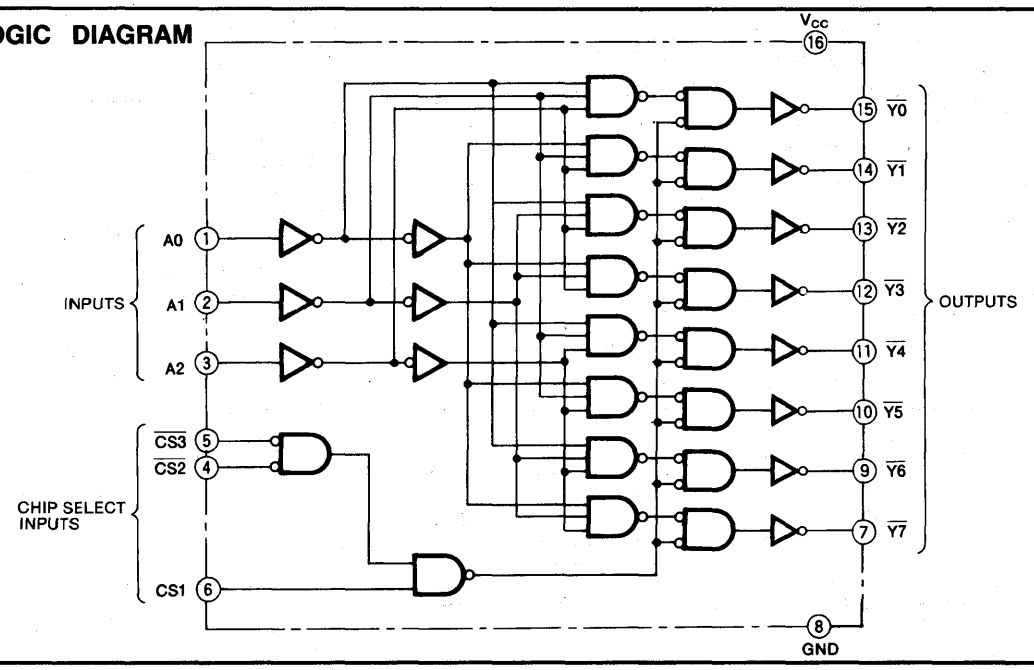
When operated as a decoder, a 3-bit binary code are applied to inputs A0, A1 and A2, one of outputs $\overline{Y0}$ through $\overline{Y7}$ corresponding to this value will become low and the other outputs will all become high.

In this case, chip select input CS1 should be maintained at high while $\overline{CS2}$ and $\overline{CS3}$ should be maintained at low.

When CS1, $\overline{CS2}$ and $\overline{CS3}$ are in conditions other than those given above, all outputs will become high irrespective of A0 through A2.

When operated as a 1-of-8 demultiplexer, CS1, $\overline{CS2}$, or $\overline{CS3}$ is used as data input and A0 through A2 input are used as slecting input.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs					Outputs							
CS1	$\overline{CSX}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note 1 : $\overline{CSX} = \overline{CS2} + \overline{CS3}$
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC138FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC138DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9			V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0		−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0		4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

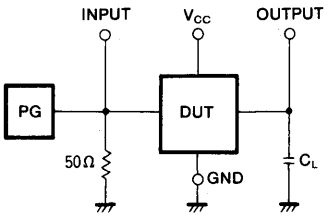
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time (A − $\overline{Y}$)				35	ns
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time (CS1 − $\overline{Y}$)				25	ns
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time ($\overline{CS2}$, $\overline{CS3}$ − $\overline{Y}$)				30	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CS1 − $\overline{Y}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS2}$, $\overline{CS3}$ − $\overline{Y}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				82				pF

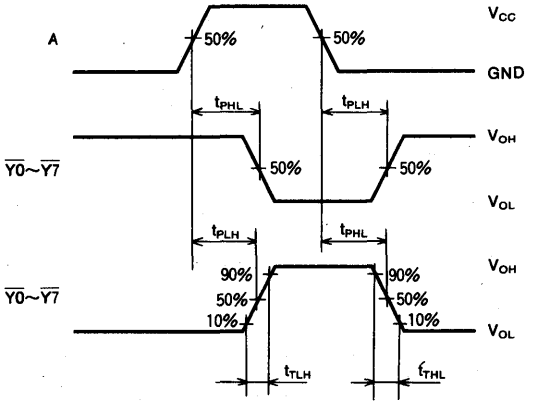
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

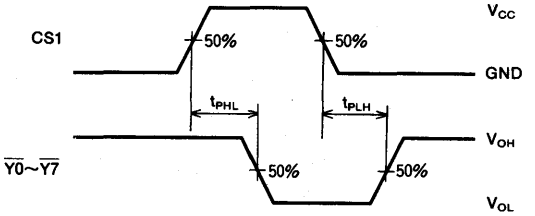
Note 4 : Test Circuit

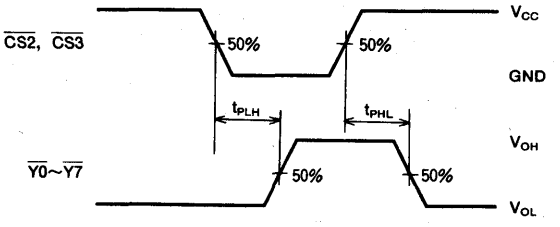


(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HCT138P/FP/DP

1-OF-8 DECODER/DEMULTIPLEXER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT138 is a semiconductor integrated circuit consisting of a 3-bit binary-to 8-line decoder/demultiplexer with chip-select inputs.

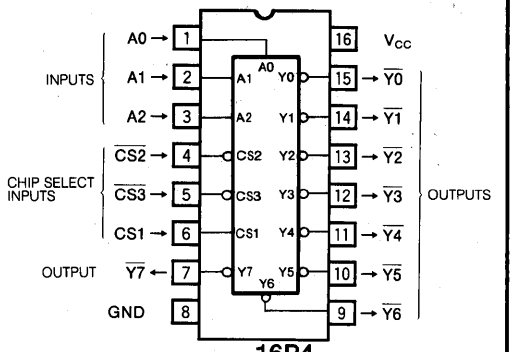
FEATURES

- TTL level input V_{IL} = 0.8V max V_{IH} = 2.0V min
- Three types of chip-select inputs
- High-speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC} + 2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4 16P2N 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT138 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS138.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

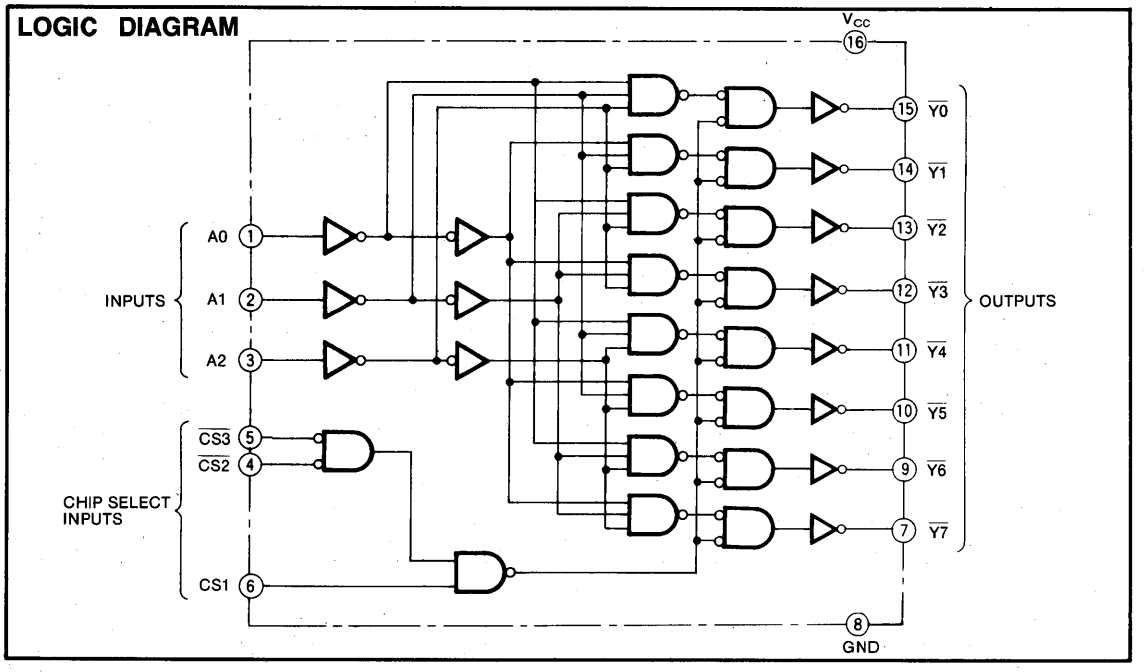
When operated as a decoder, a 3-bit binaly code are applied to inputs A0, A1 and A2, one of outputs $\overline{Y0}$ through $\overline{Y7}$ corresponding to this value will become low and the other outputs will all become high.

In this case, chip select input CS1 should be maintained at high while $\overline{CS2}$ and $\overline{CS3}$ should be maintained at low.

When CS1, $\overline{CS2}$ and $\overline{CS3}$ are in conditions other than those given above, all outputs will become high irrespective of A0 through A2.

When operated as a 1-of-8 demultiplexer, CS1, $\overline{CS2}$ or $\overline{CS3}$ is used as data input and A0 through A2 input are used as slecting input.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

1-OF-8 DECODER/DEMULTIPLEXER WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inputs					Outputs							
CS1	$\overline{CSX}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note 1 : $\overline{CSX} = \overline{CS2} + \overline{CS3}$
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC138FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC138DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_{CC}−0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −4.0mA, V_{CC} = 4.5V	4.18			4.13		
			I_{OH} = −4.8mA, V_{CC} = 5.5V	5.18			5.13		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 4.0mA, V_{CC} = 4.5V			0.26		0.33	
			I_{OL} = 4.8mA, V_{CC} = 5.5V			0.26		0.33	
I_{IH}	High-level input current	V_I = 5.5V				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V				−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				4.0		40.0	μA
$\triangle I_{CC}$	Maximum quiescent state supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all others are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

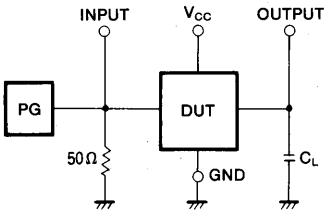
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 5)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time (A − $\overline{Y}$)				35	ns
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time (CS1 − $\overline{Y}$)				25	ns
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time ($\overline{CS2}$, $\overline{CS3}$ − $\overline{Y}$)				30	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level	C_L = 50pF (Note 5)			15		19	ns
t_{THL}	to low-level output transition time				15		19	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A−Y)				30		38	ns
t_{PHL}					40		50	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CS1−Y)				30		38	ns
t_{PHL}					30		38	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS2}$, $\overline{CS3}$−$\overline{Y}$)				30		38	ns
t_{PHL}					35		43	ns
C_I	Input capacitance				10		10	pF
C_{PD}	Power dissipation capacitance (Note 4)							pF

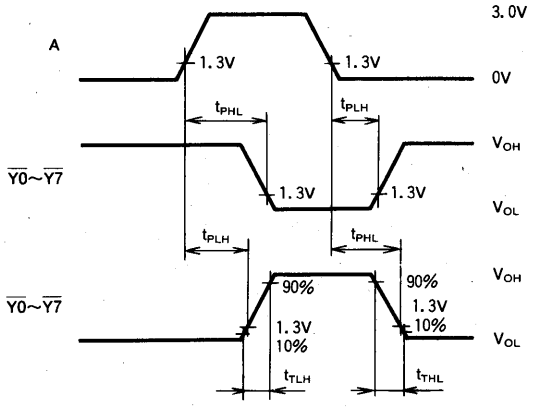
Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

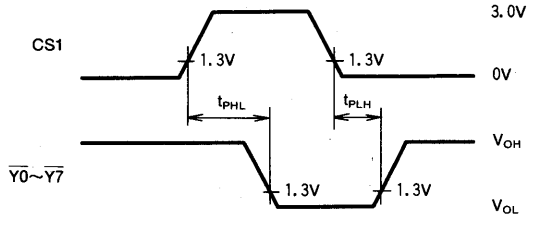
Note 5 : Test Circuit

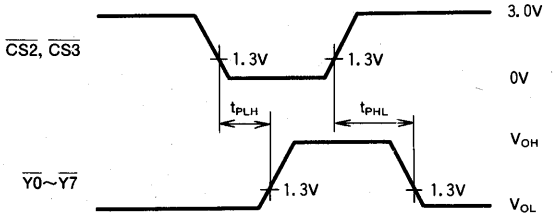


(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







M74HC139P/FP/DP

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

DESCRIPTION

The M74HC139 is a semiconductor integrated circuit consisting of a 2-bit binary to divide-by-4 decoder/demultiplexer with chip select inputs.

FEATURES

- Chip select inputs
- High-speed: 19ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

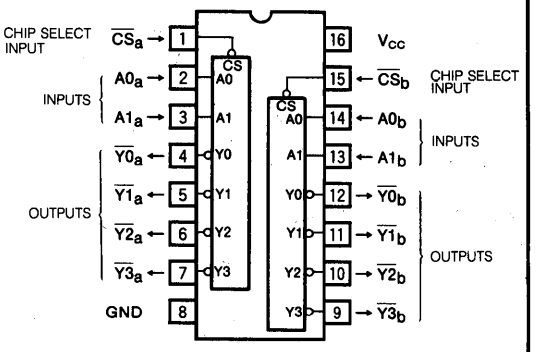
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC139 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS139.

When operated as a decoder, a 2-bit binary code are applied to inputs A0 and A1, one of outputs $\overline{Y0}$ through $\overline{Y3}$ corresponding to this value will become low and the other outputs will all become high. In this case, chip select input $\overline{CS}$ should be maintained at low. When $\overline{CS}$ is high, all outputs will become high irrespective of A0 and A1.

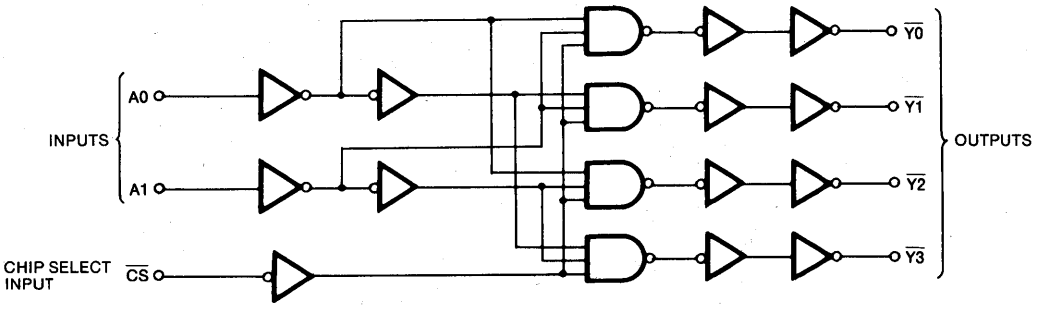
PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

When operated as a 1-of-4 demultiplexer, $\overline{CS}$ is used as a data input and A0 and A1 are used as slecting inputs.

LOGIC DIAGRAM (EACH DECODER/DEMULTIPLEXER)



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FUNCTION TABLE (Note 1)

Inputs			Outputs			
$\overline{CS}$	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC139FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC139DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

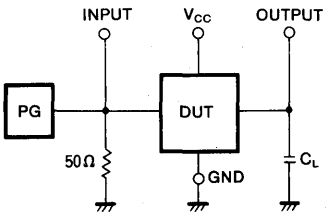
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS}$ − $\overline{Y}$)				30	ns
t_{PHL}					30	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)	Number of delay gate stages 4			30	ns
t_{PHL}					30	ns
t_{PLH}		Number of delay gate stages 5			38	ns
t_{PHL}					38	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS}$ − $\overline{Y}$)		2.0			175		219	ns
			4.5			35		44	
			6.0			30		38	
t_{PHL}			2.0			175		219	ns
			4.5			35		44	
			6.0			30		38	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)	Number of delay gate stages 4	2.0			175		219	ns
			4.5			35		44	
			6.0			30		38	
t_{PHL}			2.0			175		219	ns
			4.5			35		44	
			6.0			30		38	
t_{PLH}		Number of delay gate stages 5	2.0			220		275	ns
			4.5			44		55	
			6.0			38		47	
t_{PHL}			2.0			220		275	ns
			4.5			44		55	
			6.0			38		47	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				62				pF

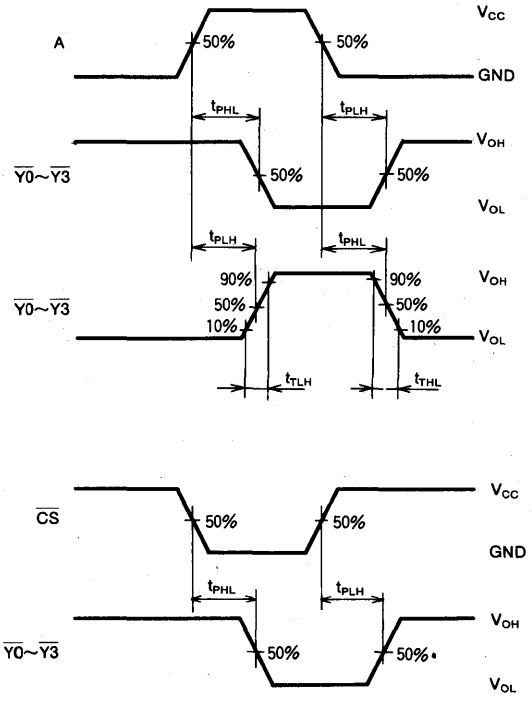
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per decoder)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC147P/FP/DP

10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

DESCRIPTION

The M74HC147 is a semiconductor integrated circuit consisting of a 10-line decimal to 4-line BCD encoder with priority.

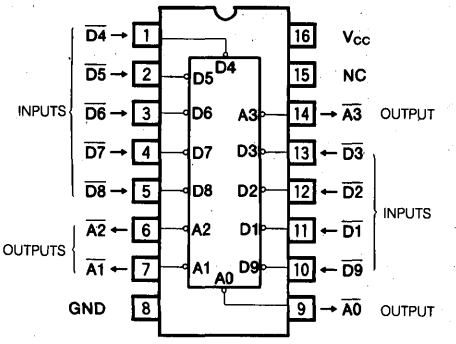
FEATURES

- Priority for data input
- High-speed: 16ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



16P4
Outline 16P2N
16P2P

NC : NO CONNECTION

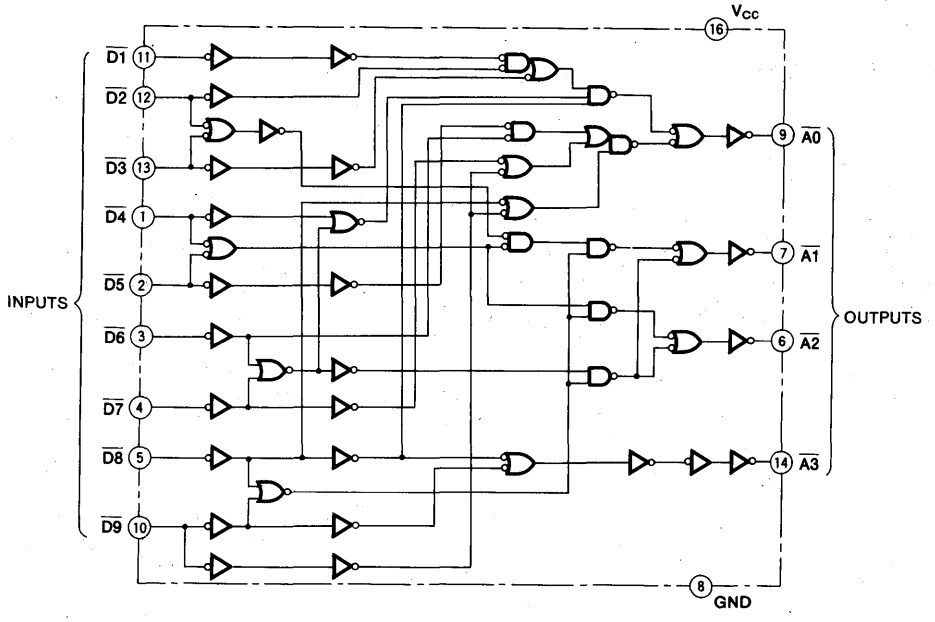
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC147 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS147.

When an input is applied to one of the nine input lines $\overline{D1}$ through $\overline{D9}$, the corresponding inverted BCD code is output at $\overline{A0}$ through $\overline{A3}$. When more than one input is applied simultaneously, the signal at the highest order input pin is given priority.

$\overline{D0}$ does not exist as an input, and when all inputs are high, all outputs will become high, allowing zero to be obtained. The device is ideal for Keyboard encoders or range selectors.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

FUNCTION TABLE (Note 1)

Inputs									Outputs			
$\overline{D1}$	$\overline{D2}$	$\overline{D3}$	$\overline{D4}$	$\overline{D5}$	$\overline{D6}$	$\overline{D7}$	$\overline{D8}$	$\overline{D9}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per, output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC147FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC147DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9			V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

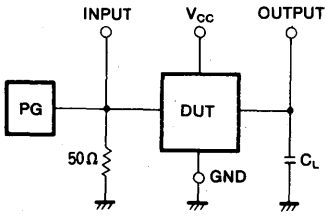
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time ($\overline{D1}$～$\overline{D9}$ − $\overline{A0}$～$\overline{A3}$)				26	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2～6V, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{D}$ − $\overline{A}$)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PHL}			2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

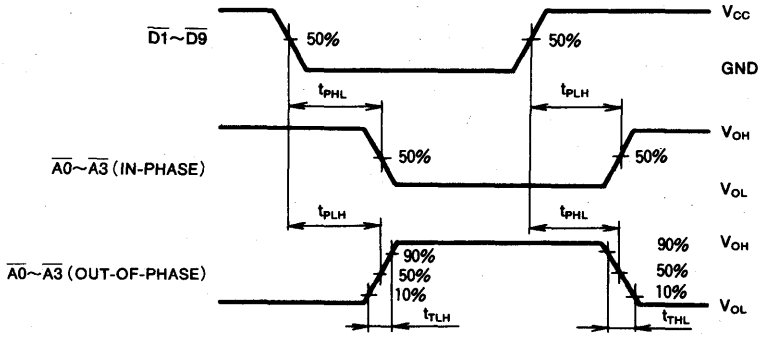
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC148P/FP/DP

8-LINE TO 3-LINE PRIORITY ENCODER

DESCRIPTION

The M74HC148 is a semiconductor integrated circuit consisting of an 8-line binary octal encoder with priority.

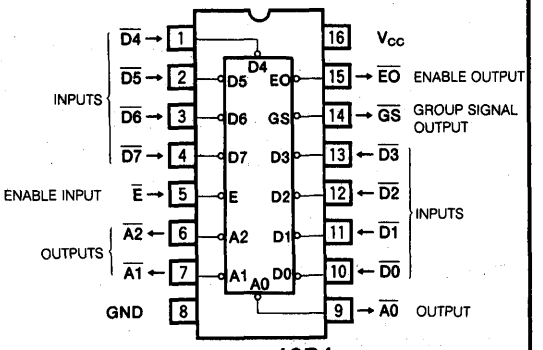
FEATURES

- Priority for date input
- Easily expandable number of input bits
- High-speed: 16ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



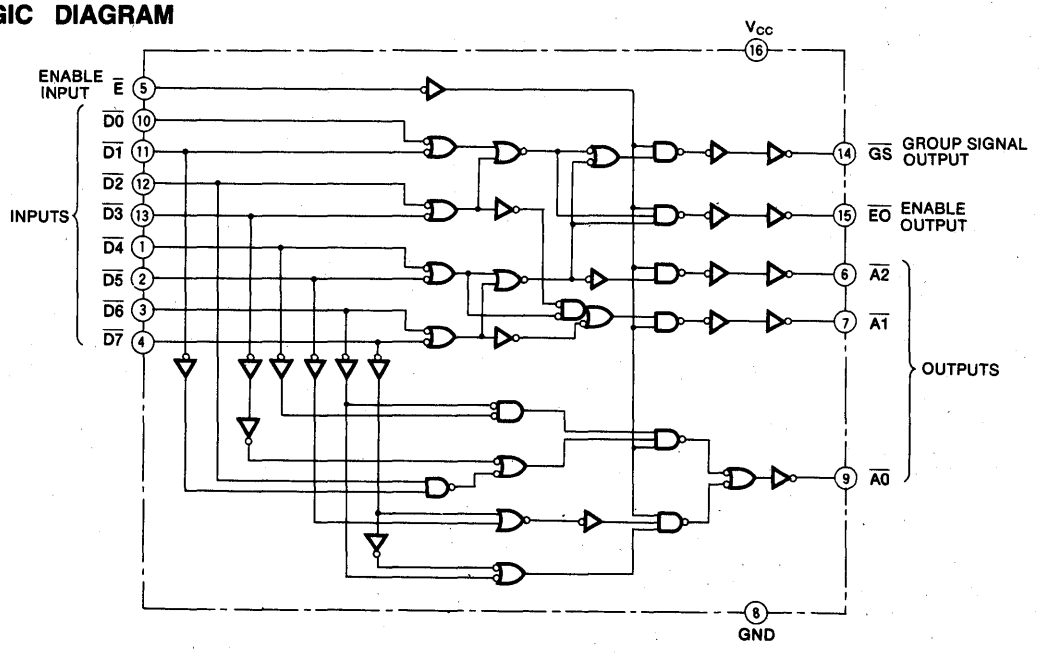
Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC148 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS148.

When an input is applied to one of the eight input lines $\overline{D0}$ through $\overline{D7}$, the corresponding 3-bit binary code is output at $\overline{A0}$ through $\overline{A2}$. When more than one input is applied simultaneously, the highest order pin is given priority. By using enable-input $\overline{E}$, enable-output $\overline{EO}$, and group-signal output $\overline{GS}$, the number of lines can be easily expanded, making the device ideal for keyboard encoders and range selectors.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs									Outputs				
$\overline{E}$	$\overline{D0}$	$\overline{D1}$	$\overline{D2}$	$\overline{D3}$	$\overline{D4}$	$\overline{D5}$	$\overline{D6}$	$\overline{D7}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	$\overline{GS}$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per, output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC148FP, T_a = −40~+70℃ and T_a = 70~85℃ are derated at −6mW/℃.
M74HC148DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

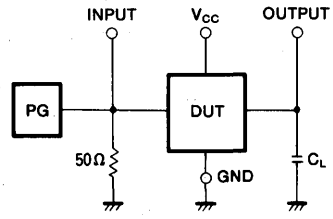
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time ($\overline{D0}$～$\overline{D7}$ − $\overline{A0}$～$\overline{A2}$)				26	ns
t_{PLH}	Low-level to high-level and high-level to low-level				28	ns
t_{PHL}	output propagation time ($\overline{D0}$～$\overline{D7}$ − $\overline{E0}$, $\overline{GS}$)				28	ns
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time ($\overline{E}$ − $\overline{E0}$)				20	ns
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time ($\overline{E}$ − $\overline{GS}$)				20	ns
t_{PLH}	Low-level to high-level and high-level to low-level				21	ns
t_{PHL}	output propagation time ($\overline{E}$ − $\overline{A0}$～$\overline{A2}$)				21	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	Limits 25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{D0}$~$\overline{D7}$ − $\overline{A0}$~$\overline{A2}$)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PHL}			2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{D0}$~$\overline{D7}$ − $\overline{E0}$, $\overline{GS}$)		2.0			165		205	ns
			4.5			33		41	
			6.0			28		35	
t_{PHL}			2.0			165		205	ns
			4.5			33		41	
			6.0			28		35	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{E}$ − $\overline{E0}$)		2.0			120		150	ns
			4.5			24		30	
			6.0			20		26	
t_{PHL}			2.0			120		150	ns
			4.5			24		30	
			6.0			20		26	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{E}$ − $\overline{GS}$)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{E}$ − $\overline{A0}$~$\overline{A2}$)		2.0			125		155	ns
			4.5			25		31	
			6.0			21		26	
t_{PHL}			2.0			125		155	ns
			4.5			25		31	
			6.0			21		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

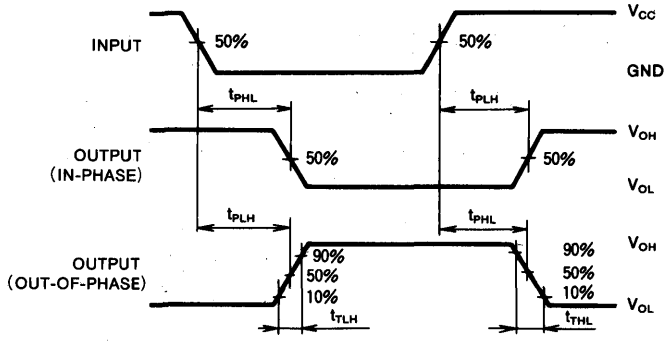
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC151P/FP/DP

8-INPUT DATA SELECTOR/MULTIPLEXER

DESCRIPTION

The M74HC151 is a semiconductor integrated circuit consisting of an 8-line to 1-line date selector/multiplexer.

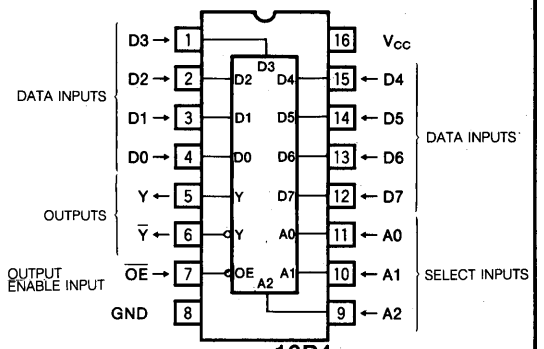
FEATURES

- High-speed: 22ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N
16P2P

FUNCTIONAL DESCRIPTION

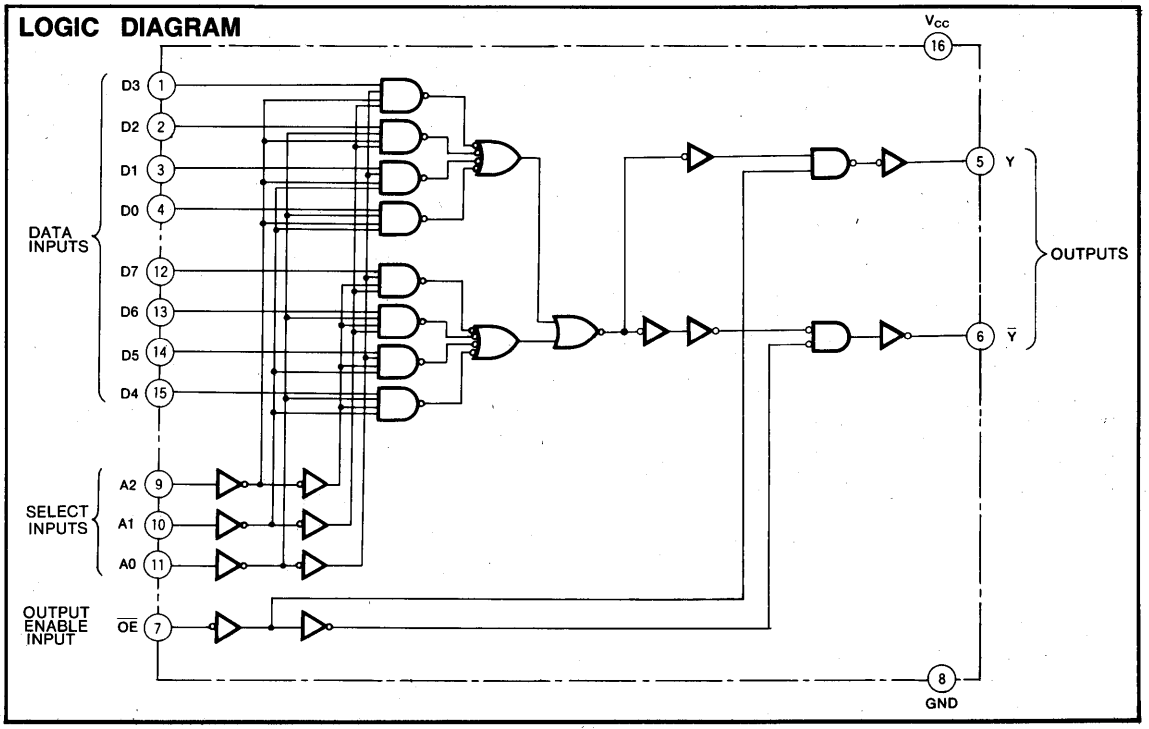
Use of silicon gate technology allows the M74HC151 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS151.

The M74HC151 consists of data selector functions for selecting one of eigh input line signals and multiplexer functions for converting 8-bit parallel data into serial data using time-division.

The 8-line signal is applied to data inputs D0 through D7, and after one of the data inputs has been selected by select inputs A0 through A2, that input signal will be output at Y or an inverted signal will be output at $\overline{Y}$. By applying 8-bit parallel data to D0 through D7, and connecting the output of a synchronous octal counter to A0 through A2, D0 through D7 data will be output at Y synchronous with the clock pulse in the order of D0-D7. When output-enable input $\overline{OE}$ is high, Y will become low and $\overline{Y}$ will become high irrespective of other inputs.

The M74HC151 has the same functions and pin connections as the M74HC251, but the latter has a 3-state output.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs												Outputs	
A2	A1	A0	$\overline{OE}$	D0	D1	D2	D3	D4	D5	D6	D7	Y	$\overline{Y}$
X	X	X	H	X	X	X	X	X	X	X	X	L	H
L	L	L	L	L	X	X	X	X	X	X	X	L	H
L	L	L	L	H	X	X	X	X	X	X	X	H	L
L	L	H	L	X	L	X	X	X	X	X	X	L	H
L	L	H	L	X	H	X	X	X	X	X	X	H	L
L	H	L	L	X	X	L	X	X	X	X	X	L	H
L	H	L	L	X	X	H	X	X	X	X	X	H	L
L	H	H	L	X	X	X	L	X	X	X	X	L	H
L	H	H	L	X	X	X	H	X	X	X	X	H	L
H	L	L	L	X	X	X	X	L	X	X	X	L	H
H	L	L	L	X	X	X	X	H	X	X	X	H	L
H	L	H	L	X	X	X	X	X	L	X	X	L	H
H	L	H	L	X	X	X	X	X	H	X	X	H	L
H	H	L	L	X	X	X	X	X	X	L	X	L	H
H	H	L	L	X	X	X	X	X	X	H	X	H	L
H	H	H	L	X	X	X	X	X	X	X	L	L	H
H	H	H	L	X	X	X	X	X	X	X	H	H	L

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC151FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC151DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

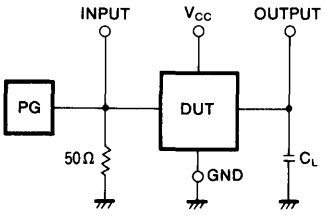
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				29	ns
t_{PHL}	output propagation time (D − Y)				29	ns
t_{PLH}	Low-level to high-level and high-level to low-level				32	ns
t_{PHL}	output propagation time (D − $\overline{Y}$)				32	ns
t_{PLH}	Low-level to high-level and high-level to low-level				43	ns
t_{PHL}	output propagation time (A − Y)				43	ns
t_{PLH}	Low-level to high-level and high-level to low-level				35	ns
t_{PHL}	output propagation time (A − $\overline{Y}$)				35	ns
t_{PLH}	Low-level to high-level and high-level to low-level				23	ns
t_{PHL}	output propagation time ($\overline{OE}$ − Y)				23	ns
t_{PLH}	Low-level to high-level and high-level to low-level				21	ns
t_{PHL}	output propagation time ($\overline{OE}$ − $\overline{Y}$)				21	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Y)		2.0			195		244	ns
			4.5			39		49	
			6.0			33		41	
t_{PHL}			2.0			195		244	ns
			4.5			39		49	
			6.0			33		41	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($D - \overline{Y}$)		2.0			185		231	ns
			4.5			37		46	
			6.0			32		40	
t_{PHL}			2.0			185		231	ns
			4.5			37		46	
			6.0			32		40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)		2.0			250		312	ns
			4.5			50		63	
			6.0			43		54	
t_{PHL}			2.0			250		312	ns
			4.5			50		63	
			6.0			43		54	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($A - \overline{Y}$)		2.0			205		256	ns
			4.5			41		51	
			6.0			35		44	
t_{PHL}			2.0			205		256	ns
			4.5			41		51	
			6.0			35		44	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE} - Y$)		2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
t_{PHL}			2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE} - \overline{Y}$)		2.0			127		159	ns
			4.5			25		32	
			6.0			22		28	
t_{PHL}			2.0			127		159	ns
			4.5			25		32	
			6.0			22		28	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				70				pF

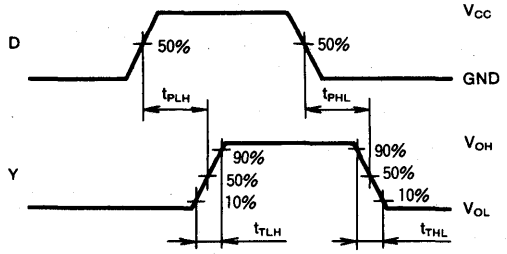
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

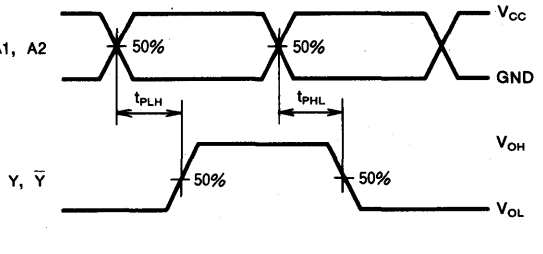
Note 4 : Test Circuit

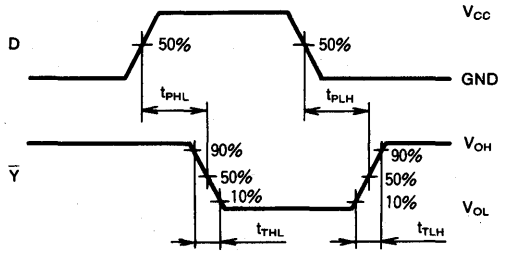


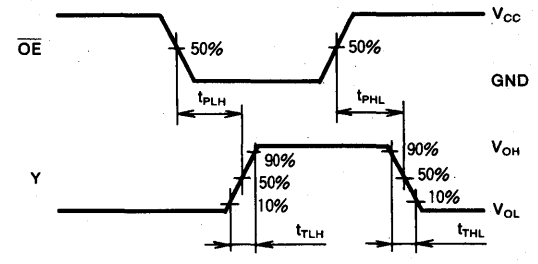
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

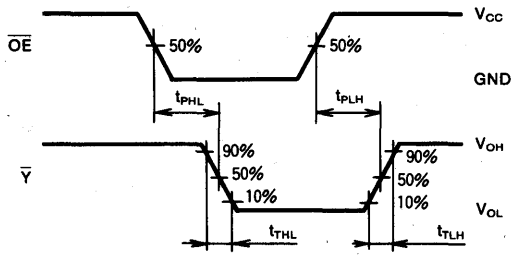
TIMING DIAGRAM











M74HC153P/FP/DP

DUAL 4-INPUT DATA SELECTOR/MULTIPLEXER

DESCRIPTION

The M74HC153 is a semiconductor integrated circuit consisting of two 4-line to 1-line data selectors/multiplexers.

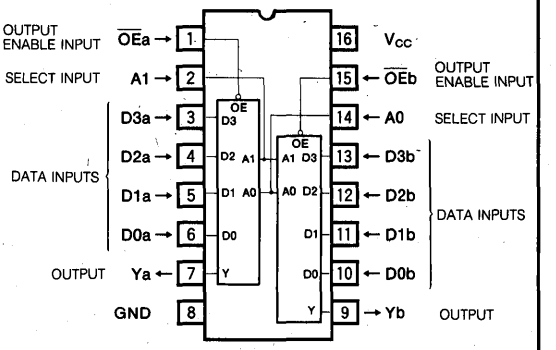
FEATURES

- High-speed: 13ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



16P4
Outline 16P2N
16P2P

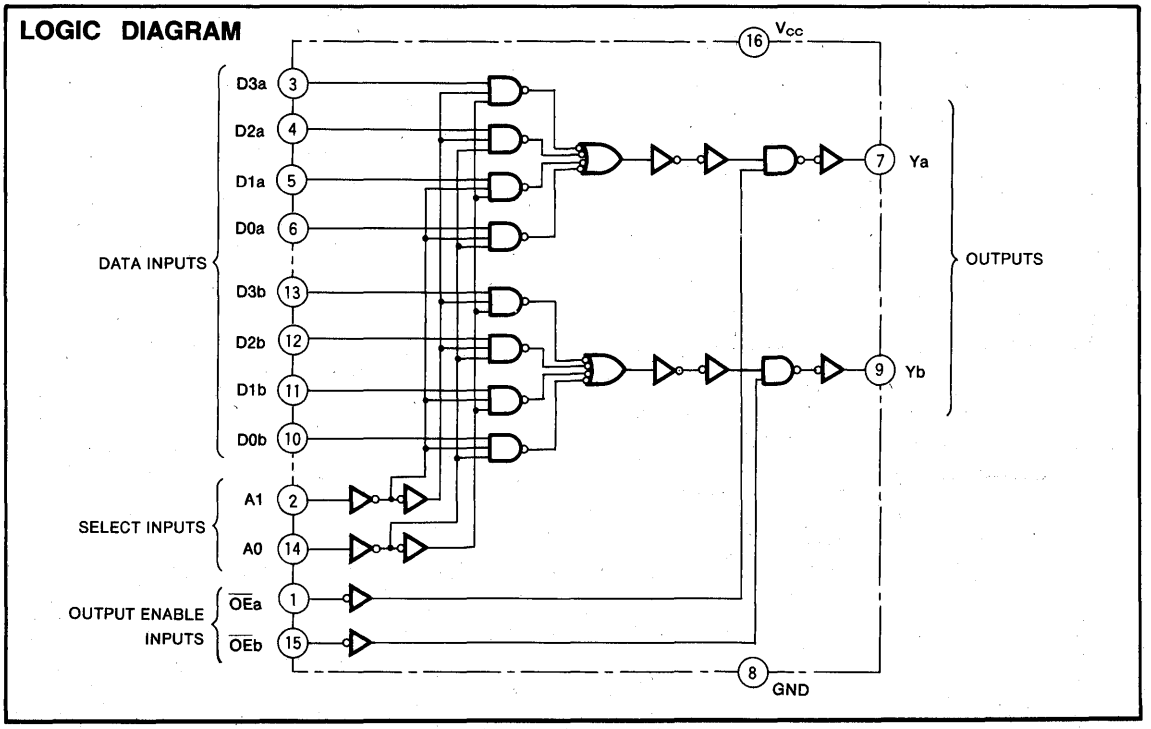
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC153 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS153.

The M74HC153 consists of data selector functions for selecting one of four input line signals and multiplex functions for converting 4-bit parallel data into serial data using time-division.

The 4-line signal is applied to data inputs D0 through D7, and after one of the data inputs has been selected by select inputs A0 and A1, that input signal will be output at Y. By applying 4-bit parallel data to D0 through D3 and connecting the output of a synchronous quadruple counter to A0 and A1, D0 through D3 data will be output at Y synchronous with the clock pulse in the order of D0-D3. Select inputs A are common to the two circuits while the output-enable inputs $\overline{OE}$ are independent. When $\overline{OE}$ is high, Y will become low irrespective of other inputs.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

FUNCTION TABLE (Note 1)

Inputs							Output
A1	A0	D0	D1	D2	D3	$\overline{OE}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC153FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC153DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9			V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

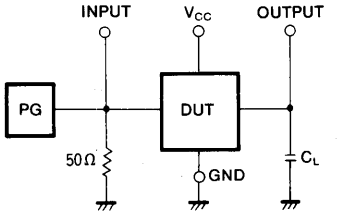
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Y)				23	ns
t_{PHL}					23	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)				30	ns
t_{PHL}					30	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE}$ − Y)				15	ns
t_{PHL}					15	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Y)		2.0			126		158	ns
			4.5			28		35	
			6.0			23		29	
t_{PHL}			2.0			126		158	ns
			4.5			28		35	
			6.0			23		29	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)		2.0			158		198	ns
			4.5			35		44	
			6.0			30		38	
t_{PHL}			2.0			158		198	ns
			4.5			35		44	
			6.0			30		38	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE}$ − Y)		2.0			95		120	ns
			4.5			19		24	
			6.0			16		20	
t_{PHL}			2.0			95		120	ns
			4.5			19		24	
			6.0			16		20	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				48				pF

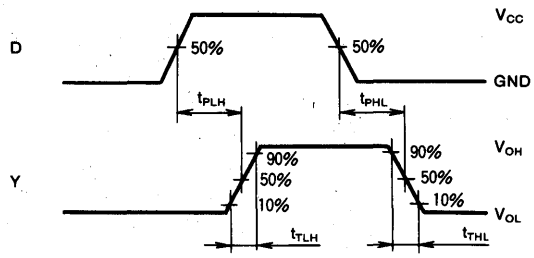
Note 3 : C_{PD} is the internal capacitance of the IC caluculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the follwing iormula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

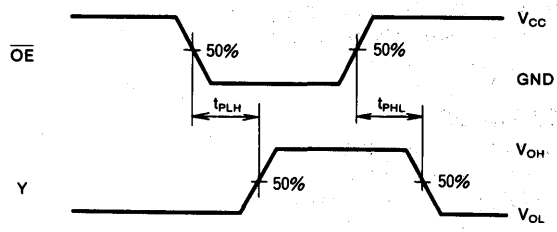
Note 4 : Test Circuit

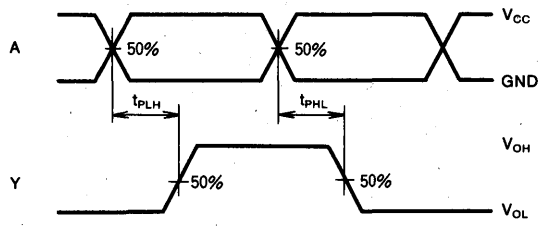


(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC154P/FP/DWP

1-OF-16 DECODER/DEMULTIPLEXER

DESCRIPTION

The M74HC154 is a semiconductor integrated circuit consisting of a 4-bit binary to 16-line decoder/demultiplexer with chip select inputs.

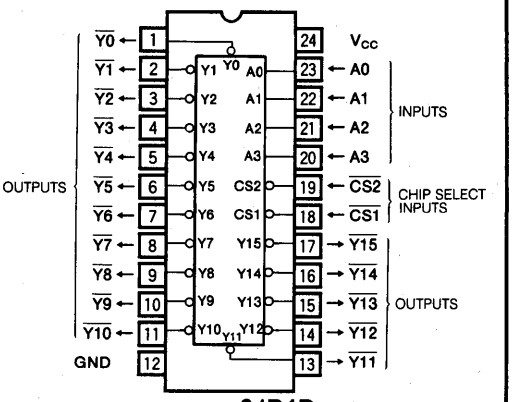
FEATURES

- Two chip select inputs
- High-speed: 21ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D 24P2 24P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC154 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS154.

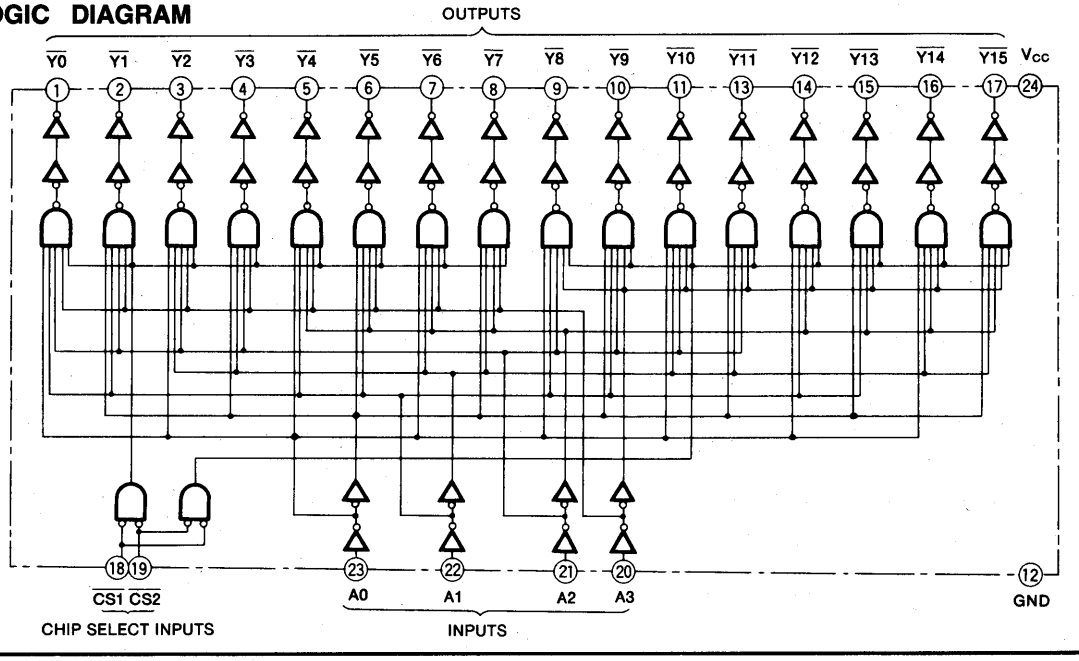
When operated as a 1-of-16 decoder, by applying a 4-bit binary code to inputs A0 through A3, the corresponding output. $\overline{Y0}$ through $\overline{Y15}$ will become low and all the others will become high.

In this case, chip select inputs $\overline{CS1}$ and $\overline{CS2}$ should be maintained low.

When both $\overline{CS1}$ and $\overline{CS2}$ are not low, all outputs will become high irrespective of A0 through A3.

When operated as a 1-of-16 demultiplexer, $\overline{CS1}$ or $\overline{CS2}$ is used as a data input and A0 through A3 are used as selecting inputs.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs						Outputs															
$\overline{CS1}$	$\overline{CS2}$	A3	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$	$\overline{Y10}$	$\overline{Y11}$	$\overline{Y12}$	$\overline{Y13}$	$\overline{Y14}$	$\overline{Y15}$
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC154FP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.
M74HC154DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	low-level input current	V_I = 0V		6.0		−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0		4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

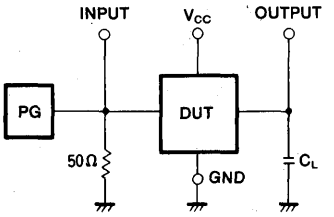
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)				32	ns
t_{PHL}					32	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS1}$, $\overline{CS2}$ − $\overline{Y}$)				32	ns
t_{PHL}					32	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2～6V, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)		2.0			160		190	ns
			4.5			36		42	
			6.0			30		35	
t_{PHL}			2.0			160		190	ns
			4.5			36		42	
			6.0			30		35	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS1}$, $\overline{CS2}$ − $\overline{Y}$)		2.0			160		190	ns
			4.5			36		42	
			6.0			30		35	
t_{PHL}			2.0			160		190	ns
			4.5			36		42	
			6.0			30		35	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

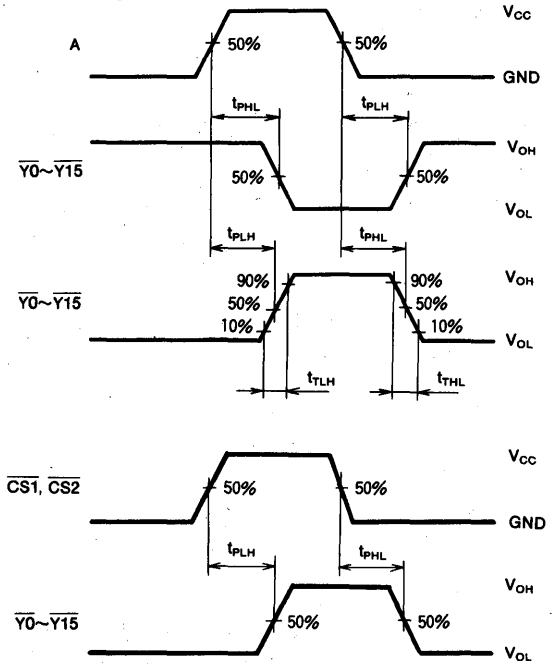
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC155P/FP/DP

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

DESCRIPTION

The M74HC155 is a semiconductor integrated circuit consisting of two 2-bit binary to 4-line decoders/demultiplexers.

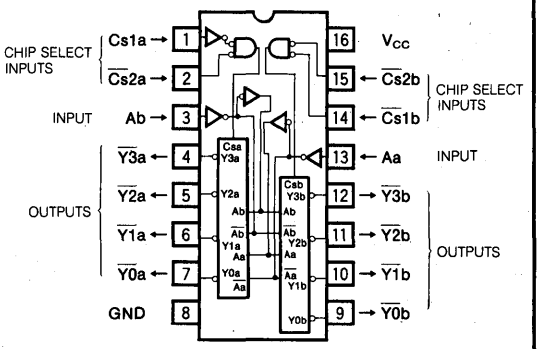
FEATURES

- High-speed: 19ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC155 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS155.

When operated as a 2-bit binary to 4-line decoder, by applying 2-bit binary data to inputs Aa and Ab, the corresponding output $\overline{Y0}$ through $\overline{Y3}$ will become low and all the others will become high.

In this case, chip select inputs $\overline{Cs}$1a and $\overline{Cs}$1b should be maintained at high and low respectively, and chip select inputs $\overline{Cs}$2a and $\overline{Cs}$2b should be maintained low.

When both $\overline{Cs}$2a and $\overline{Cs}$2b are high, all the outputs will become high.

When operated as a 3-bit binary to 8-line decoder, by applying 3rd-bit binary data to connected Cs1a and $\overline{Cs}$2b, the output signals will appear at $\overline{Y0}$b through $\overline{Y3}$b and $\overline{Y0}$a through $\overline{Y3}$a in accordance with the function table given.

When operated as a 1-of-4 demultiplexer, by using Cs1a and $\overline{Cs}$1b as data inputs, and by using Aa and Ab as select inputs, the output signals will appear at $\overline{Y0}$ through $\overline{Y3}$.

When operated as a 1-of-8 demultiplexer, by using connected Cs1a and $\overline{Cs}$1b as 3rd-bit select input, and by using connected $\overline{Cs}$2a and $\overline{Cs}$2b as data input, the output signals will appear at $\overline{Y0}$b through $\overline{Y3}$b and $\overline{Y0}$a through $\overline{Y3}$a.

FUNCTION TABLE (Note 1)

〈2-BIT BINARY TO 4-LINE DECODER/1-LINE TO 4-LINE DEMULTIPLEXER〉

Inputs				Outputs			
Ab	Aa	$\overline{Cs}$2a	Cs1a	$\overline{Y0}$a	$\overline{Y1}$a	$\overline{Y2}$a	$\overline{Y3}$a
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Ab	Aa	$\overline{Cs}$2b	$\overline{Cs}$1b	$\overline{Y0}$b	$\overline{Y1}$b	$\overline{Y2}$b	$\overline{Y3}$b
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

〈3-BIT BINARY TO 8-LINE DECODER/1-LINE TO 8-LINE DEMULTIPLEXER〉

Inputs				Outputs							
Ac	Ab	Aa	$\overline{Cs}$	$\overline{Y0}$b	$\overline{Y1}$b	$\overline{Y2}$b	$\overline{Y3}$b	$\overline{Y0}$a	$\overline{Y1}$a	$\overline{Y2}$a	$\overline{Y3}$a
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Note 1 : X : Irrelevant
Ac : $\overline{Cs}$1a and $\overline{Cs}$1b (when connected)
$\overline{Cs}$: $\overline{Cs}$2a and $\overline{Cs}$2b (when connected)

M74HC157P/FP/DP

QUADRUPLE 2-INPUT NONINVERTING DATA SELECTOR/MULTIPLEXER

DESCRIPTION

The M74HC157 is a semiconductor integrated circuit consisting of four 2-line to 1-line data selectors/multiplexers.

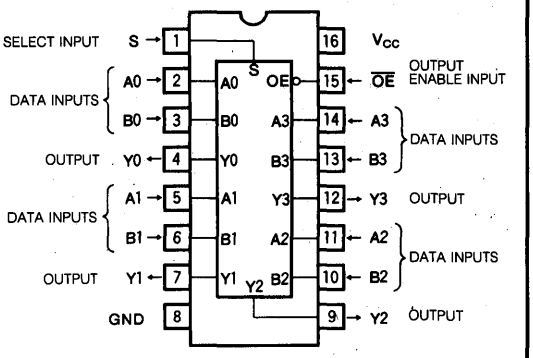
FEATURES

- High-speed: 12ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N
16P2P

FUNCTIONAL DESCRIPTION

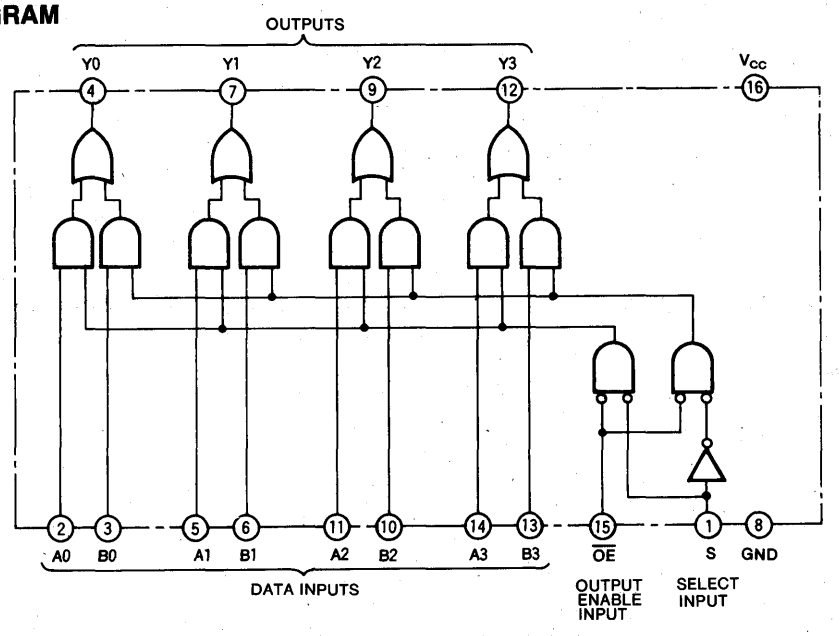
Use of silicon gate technology allows the M74HC157 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS157.

The M74HC157 consists of four circuits each containing data selector functions for selecting one of two input line signals and multiplexer functions for converting 2-bit parallel data into serial data using time-division.

The 2-line signal is applied to data inputs A and B, and after one of the inputs has been selected by select input S, it is output at pin Y. By applying 2-bit parallel data to A and B, and connecting the output of a binary counter to S, A and B date will be output at Y synchronous with the clock pulse in the order A-B. S and output-enable input $\overline{OE}$ are common to all four circuits. When $\overline{OE}$ is high, all outputs, Y will become low irrespective of other inputs.

M74HC157 is the same functions and pin connections as M74HC257, differing in that the output of M74HC257 is 3-state.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

QUADRUPLE 2-INPUT NONINVERTING DATA SELECTOR/MULTIPLEXER

FUNCTION TABLE (Note 1)

Inputs				Output
$\overline{OE}$	S	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC157FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC157DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

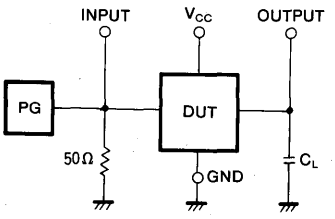
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − Y)				20	ns
t_{PHL}					20	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S − Y)				20	ns
t_{PHL}					20	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE}$ − Y)				18	ns
t_{PHL}					18	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − Y)		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S − Y)		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE}$ − Y)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				51				pF

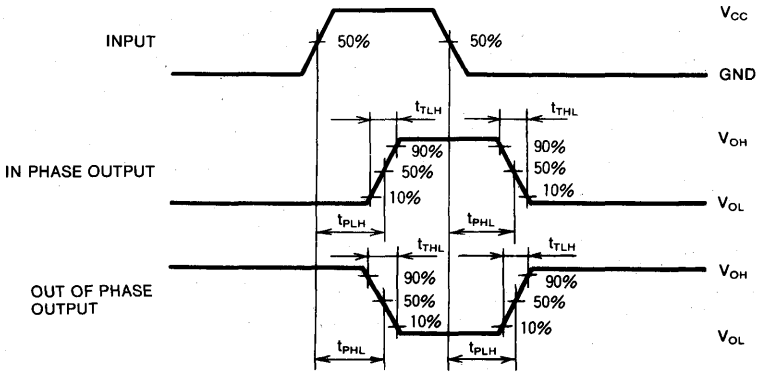
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC158P/FP/DP

QUADRUPLE 2-INPUT INVERTING DATA SELECTOR/MULTIPLEXER

DESCRIPTION

The M74HC158 is a semiconductor integrated circuit consisting of four 2-line to 1-line data selectors/multiplexers.

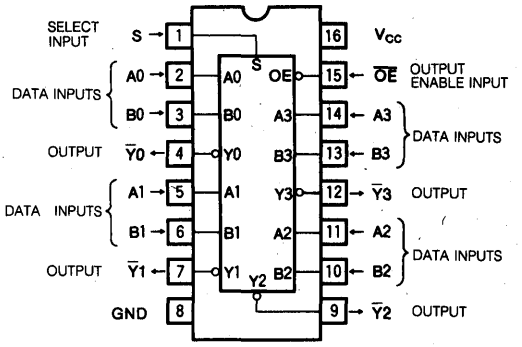
FEATURES

- High-speed: 12ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N
16P2P

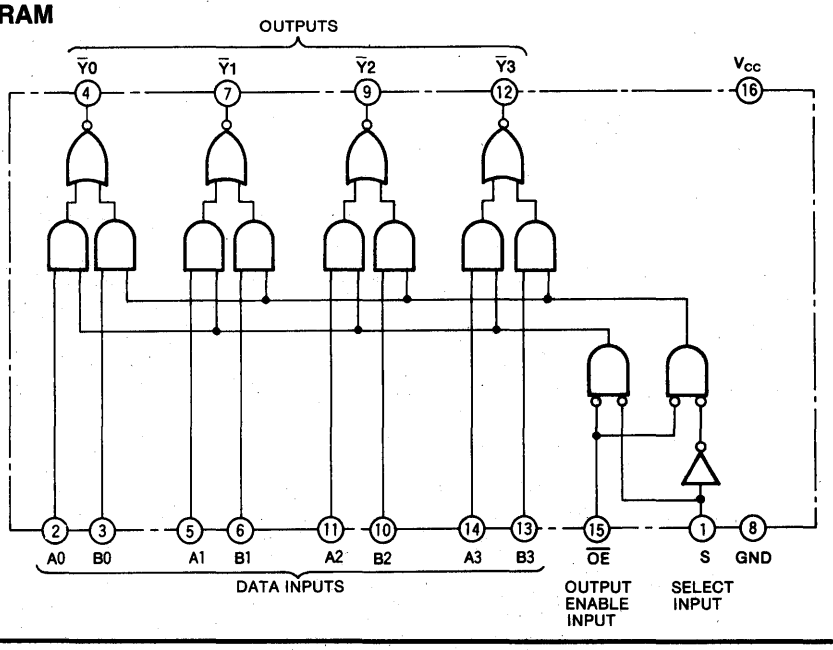
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC158 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS158.

The M74HC158 consists of four circuits each containing date selector functions for selecting one of two input line signals and multiplexer functions for converting 2-bit parallel data into serial data using time-division.

The 2-line signal is applied to data inputs A and B, and after one of the data inputs has been selected by select input S, it is inverted and output at pin $\overline{Y}$. By applying 2-bit parallel data to A and B, and connecting the output of a binary counter to S, the inverted A and B data will be output at $\overline{Y}$ synchronous with the clock pulse in the order A-B. S and output-enable input $\overline{OE}$ are common to all four circuits. When $\overline{OE}$ is high, all outputs, Y will become high irrespective of other inputs.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

QUADRUPLE 2-INPUT INVERTING DATA SELECTOR/MULTIPLEXER

FUNCTION TABLE (Note 1)

Inputs				Output
$\overline{OE}$	S	A	B	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC158FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC158DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

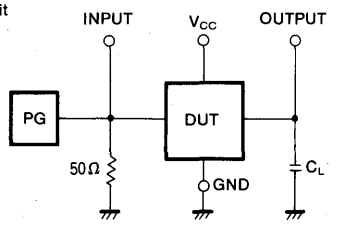
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (A, B − $\overline{Y}$)				20	ns
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (S − $\overline{Y}$)				20	ns
t_{PLH}	Low-level to high-level and high-level to low-level				18	ns
t_{PHL}	output propagation time ($\overline{OE}$ − $\overline{Y}$)				18	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − $\overline{Y}$)		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S − $\overline{Y}$)		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE}$ − $\overline{Y}$)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				82				pF

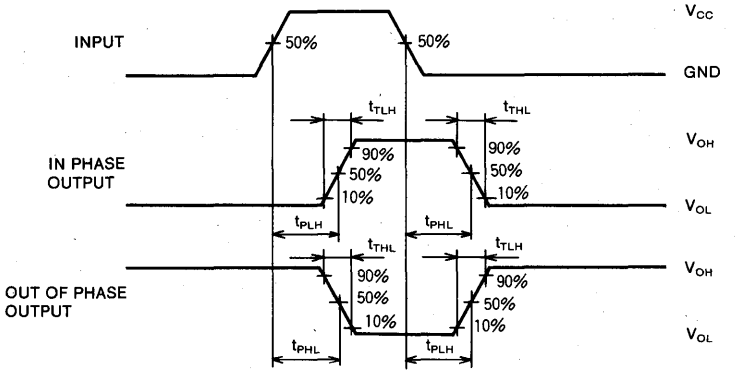
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC160P/FP/DP

PRESETTABLE BCD COUNTER WITH ASYNCHRONOUS RESET

DESCRIPTION

The M74HC160 is a semiconductor integrated circuit consisting of a presettable synchronous BCD counter with an asynchronous reset input.

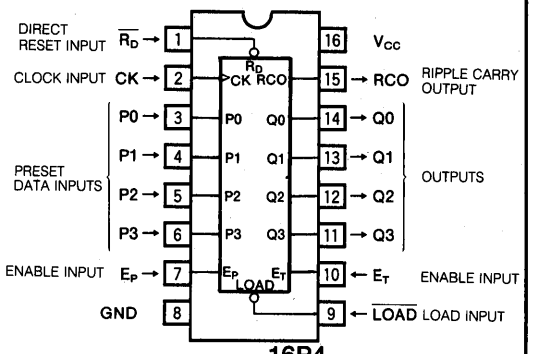
FEATURES

- Asynchronous reset and synchronous preset inputs
- Enable input and ripple carry output allow cascade connection
- Count frequency 45MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4 16P2N 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC160 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS160.

When the count pulse is applied to clock input CK, the number of count pulses will be output at outputs Q0 through Q3 synchronous with the count pulse in BCD code. Counting takes place when CK changes from low-level to high-level.

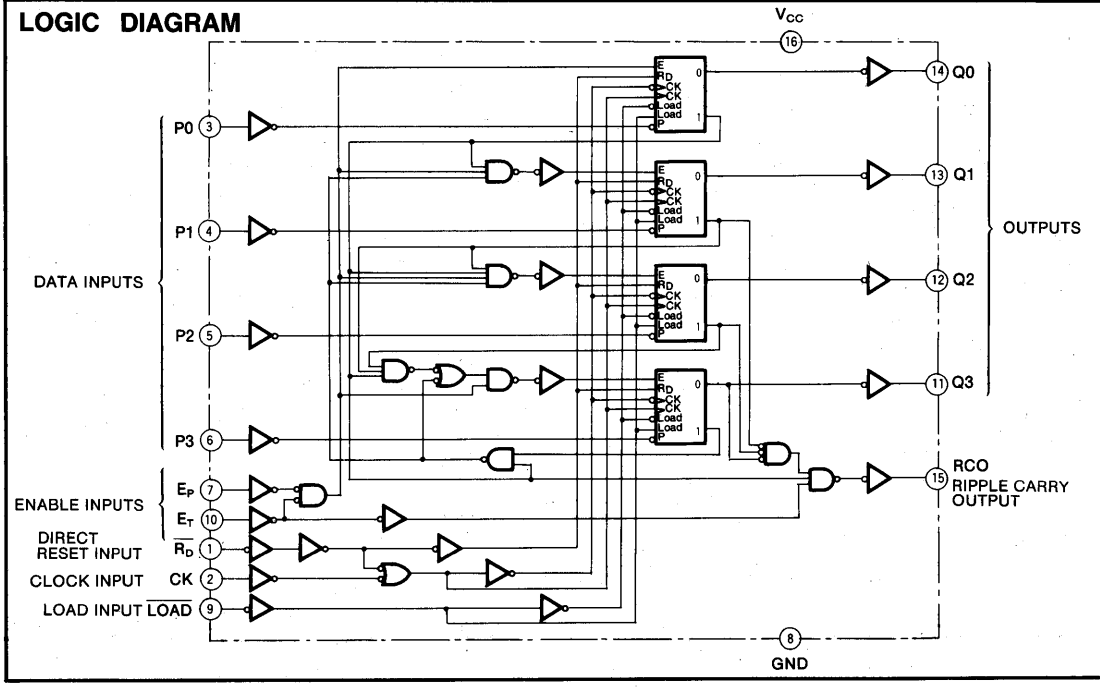
The preset functions synchronously with the count pulse. By supplying data to preset data inputs P0 through P3 and setting load input $\overline{LOAD}$ to low-level, when CK changes from low-level to high-level, the P0 through P3 signals will be output to Q0 through Q3, respectively, irrespective of enable inputs E_P and E_T. This permits persetting of the counter.

When values greater than 10 are preset, the count advances as shown in the State Transition Diagram.

The reset operates asynchronously, and by setting direct reset input $\overline{R_D}$ to low-level, Q0 through Q3 will become low irrespective of other inputs.

The ripple carry output RCO will become high only when Q0 is high, Q1 is low, Q2 is low, Q3 is high and E_T is high. E_P, E_T and RCO are used in cascade connections of the counter synchronous from when the counter is used as a nbit counter. (See the Application Example.)

LOGIC DIAGRAM



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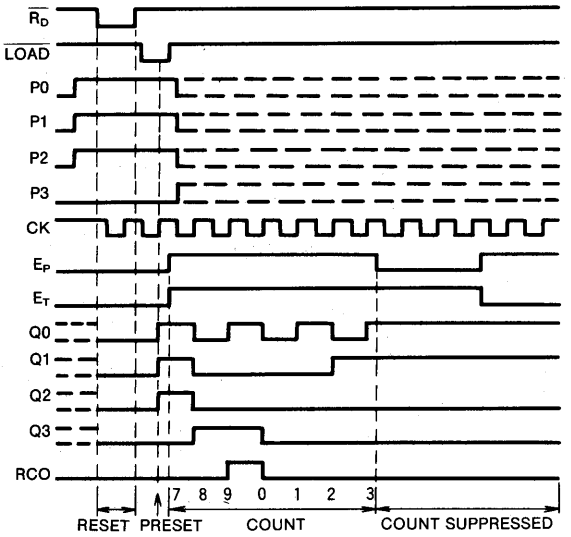
PRESETTABLE BCD COUNTER WITH ASYNCHRONOUS RESET

FUNCTION TABLE (Note 1)

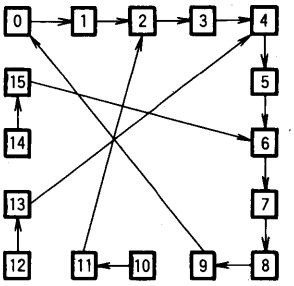
Inputs					Outputs				
$\overline{R_D}$	$\overline{LOAD}$	E_T	E_P	CK	Q0	Q1	Q2	Q3	RCO
L	X	X	X	X	L	L	L	L	L
H	L	L	X	↑	P0	P1	P2	P3	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Count suppressed				L
H	H	H	L	X	Count suppressed				L*

Note 1 : ↑ : Change from low to high (positive-edge trigger)
∗ : RCO is normally low, but will become high when Q0 is high, Q1 is low, Q2 is low, $\overline{Q3}$ is high and E_T is high. Accordingly RCO = Q0 · $\overline{Q1}$ · $\overline{Q2}$ · Q3 · E_T
X : Irrelevant

OPERATION TIMING DIAGRAM



STATE TRANSITION DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC160FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC160DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				28	ns
t_{PHL}	output propagation time (CK − Q)				34	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				36	ns
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time (E_T − RCO)				32	ns
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (CK − RCO)				36	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − RCO)				38	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

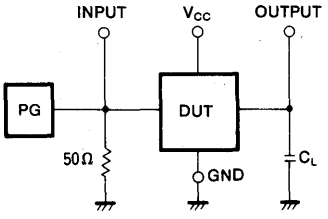
Symbol	Parameter	Test conditions	Limits					Unit
				25℃		−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			205		258	ns
			4.5			41		52	
			6.0			35		44	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (E_T − RCO)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
t_{PHL}			2.0			195		246	ns
			4.5			39		49	
			6.0			33		42	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − RCO)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			215		271	ns
			4.5			43		54	
			6.0			37		46	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − RCO)		2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				57				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIERMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

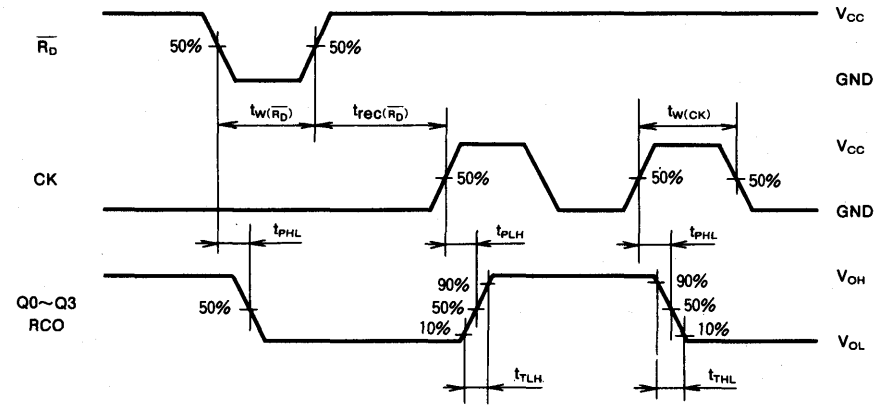
Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{W(CK)}$	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{W(\overline{R_D})}$	Direct reset pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{su(P)}$	P setup time with respect to CK		2.0	150			189		ns
			4.5	30			38		
			6.0	26			32		
$t_{su(\overline{LOAD})}$	$\overline{LOAD}$ setup time with respect to CK		2.0	135			170		ns
			4.5	27			34		
			6.0	23			29		
$t_{su(E)}$	E_T, E_P setup time with respect to CK		2.0	200			250		ns
			4.5	40			50		
			6.0	34			43		
$t_{h(P)}$	P hold time with respect to CK		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
$t_{h(\overline{LOAD})}$	$\overline{LOAD}$ hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{h(E)}$	E_T, E_P hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{rec(\overline{R_D})}$	$\overline{R_D}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		
$t_{rec(\overline{LOAD})}$	$\overline{LOAD}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		

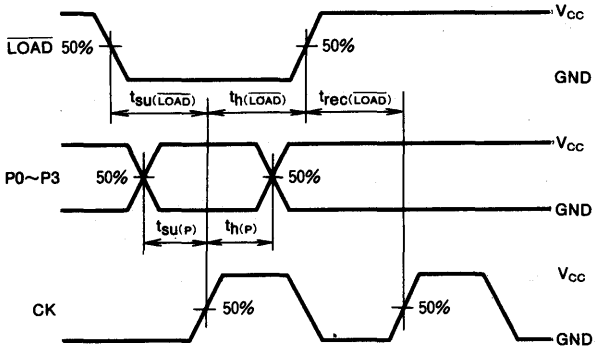
Note 4 : Test Circuit

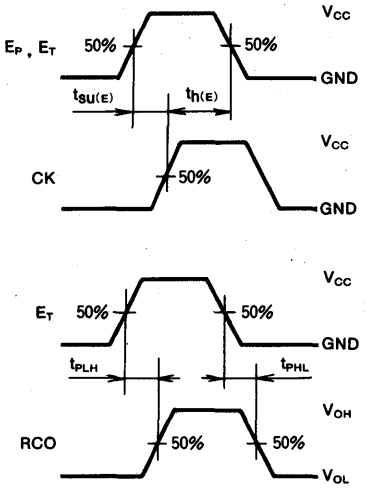


(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

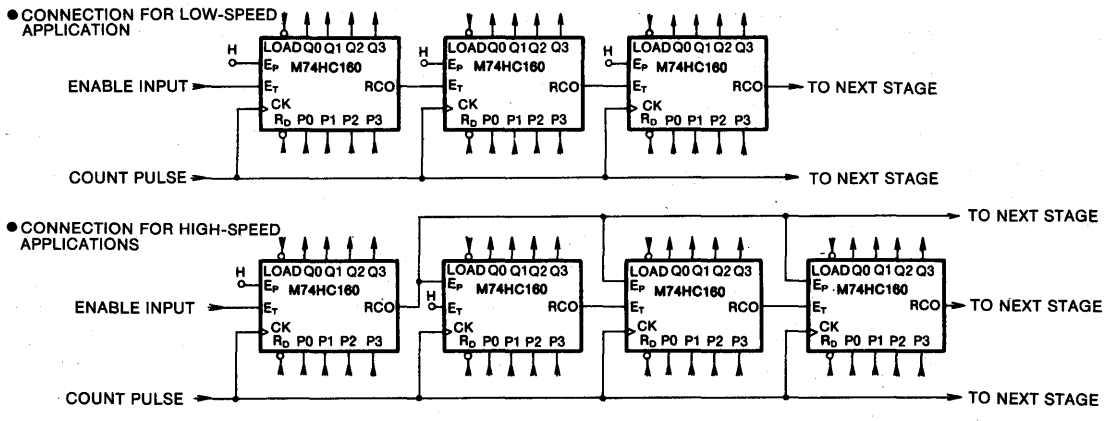
TIMING DIAGRAM







APPLICATION EXAMPLE CONFIGURATION OF A 10^n COUNTER USING CASCADE CONNECTION



M74HC161P/FP/DP

PRESETTABLE 4-BIT BINARY COUNTER WITH ASYNCHRONOUS RESET

DESCRIPTION

The M74HC161 is a semiconductor integrated circuit consisting of a presettable synchronous 4-bit binary (hexadecimal) counter with direct reset input.

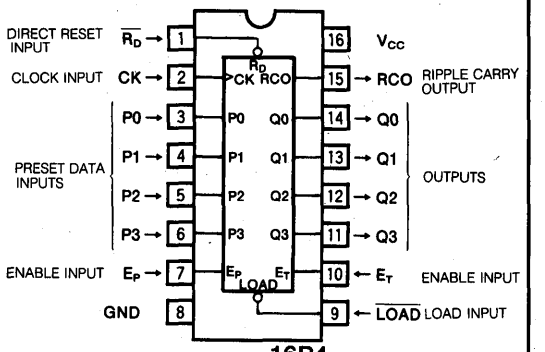
FEATURES

- Direct reset and synchronous preset inputs
- Enable input and ripple carry output for cascade connection
- Count frequency 45MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC161 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS161.

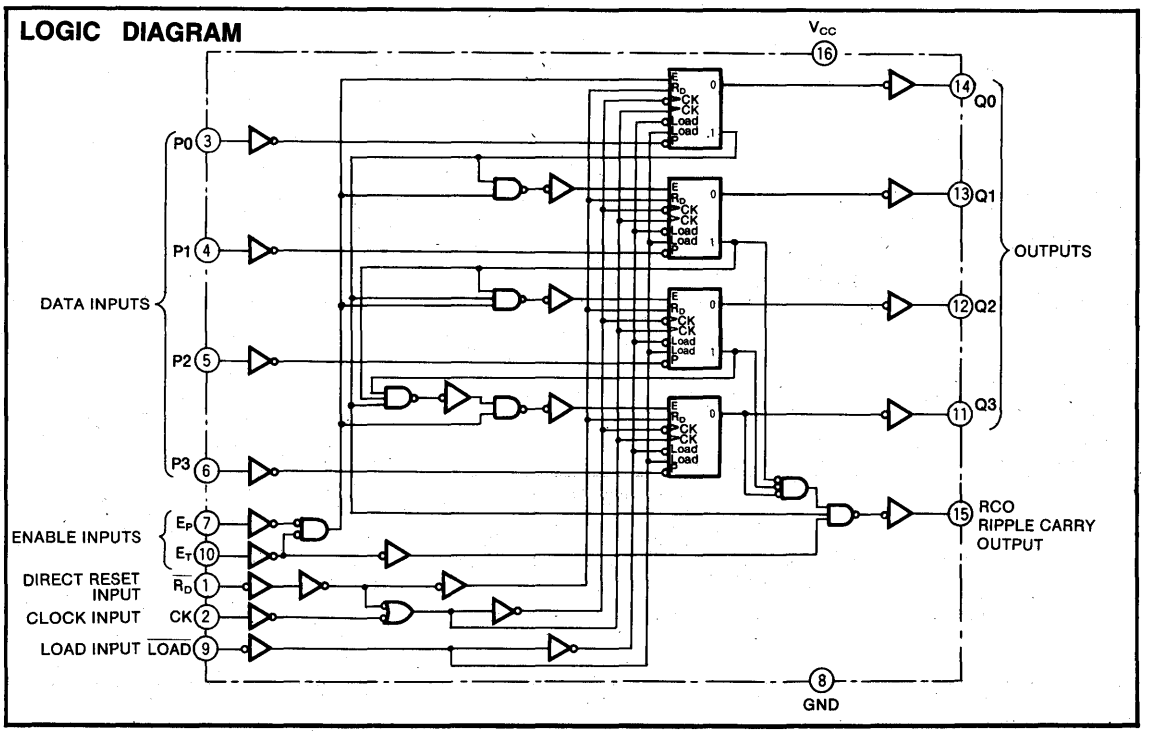
When the count pulse is applied to clock input CK, the number of count pulses will be output at outputs Q0 through Q3 synchronous with the count pulse in 4-bit binary code. Counting takes place when CK changes from low-level to high-level.

The preset functions synchronously with the count pulse. By supplying data to PERSET data inputs P0 through P3 and setting load input $\overline{LOAD}$ to low-level, when CK changes from low-level to high-level, the P0 through P3 signals will be output to Q0 through Q3, respectively, irrespective of enable inputs E_P and E_T. This permits persetting of the counter.

The reset operates asynchronously, and by setting direct reset input $\overline{R_D}$ to low-level. Q0 through Q3 will become low, irrespective of other inputs.

The ripple carry output RCO will become high only when all of Q0, Q1, Q2, Q3 and E_T are high. E_P, E_T and RCO are used in cascade connections of the counter in synchronous from when the counter is used as a n-bit counter. (See the Application Example.)

LOGIC DIAGRAM



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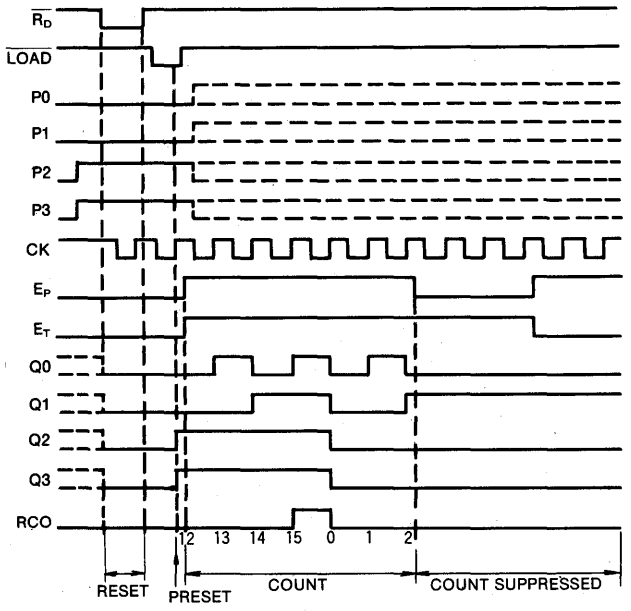
PRESETTABLE 4-BIT BINARY COUNTER WITH ASYNCHRONOUS RESET

FUNCTION TABLE (Note 1)

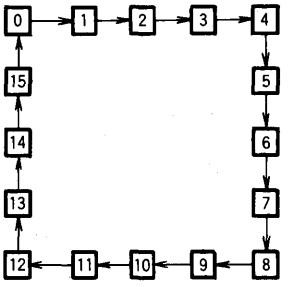
Inputs					Outputs				
$\overline{R_D}$	LOAD	E_T	E_P	CK	Q0	Q1	Q2	Q3	RCO
L	X	X	X	X	L	L	L	L	L
H	L	L	X	↑	P0	P1	P2	P3	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Count suppressed				L
H	H	H	L	X	Count suppressed				L*

Note 1 : ↑ : Change from low to high level (positive-edge trigger)
* : RCO is normally low, but will become high when all of Q0, Q1, Q2, Q3 and E_T are high. Accordingly, RCO = Q0 · Q1 · Q2 · Q3 · E_T
X : Irrelevant

OPERATION TIMING DIAGRAM



STATE TRANSITION DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC161FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC161DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

PRESETTABLE 4-BIT BINARY COUNTER WITH ASYNCHRONOUS RESET

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 2∼6V, T_a = −40∼+85℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				28	ns
t_{PHL}					34	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				36	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (E_T − RCO)				26	ns
t_{PHL}					32	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − RCO)				30	ns
t_{PHL}					36	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − RCO)				38	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			205		258	ns
			4.5			41		52	
			6.0			35		44	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (E_T − RCO)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
t_{PHL}			2.0			195		246	ns
			4.5			39		49	
			6.0			33		42	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − RCO)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			215		271	ns
			4.5			43		54	
			6.0			37		46	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − RCO)		2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				57				pF

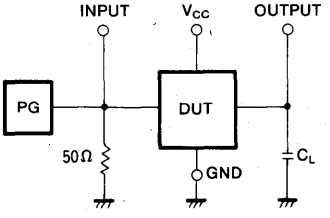
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

PRESETTABLE 4-BIT BINARY COUNTER WITH ASYNCHRONOUS RESET

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{w(CK)}$	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{w(\overline{R_D})}$	Direct reset pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{su(P)}$	P setup time with respect to CK		2.0	150			189		ns
			4.5	30			38		
			6.0	26			32		
$t_{su(\overline{LOAD})}$	$\overline{LOAD}$ setup time with respect to CK		2.0	135			170		ns
			4.5	27			34		
			6.0	23			29		
$t_{su(E)}$	E_T, E_P setup time with respect to CK		2.0	200			250		ns
			4.5	40			50		
			6.0	34			43		
$t_{h(P)}$	P hold time with respect to CK		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
$t_{h(\overline{LOAD})}$	$\overline{LOAD}$ hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{h(E)}$	E_T, E_P hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{rec(\overline{R_D})}$	$\overline{R_D}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		
$t_{rec(\overline{LOAD})}$	$\overline{LOAD}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		

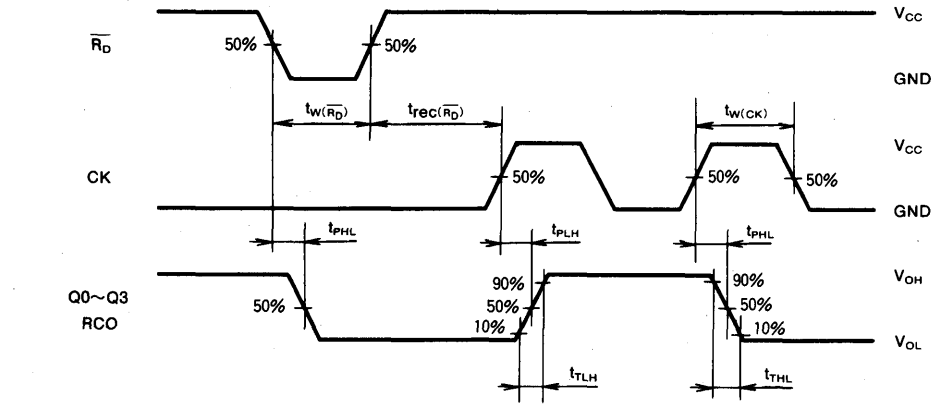
Note 4 : Test Circuit

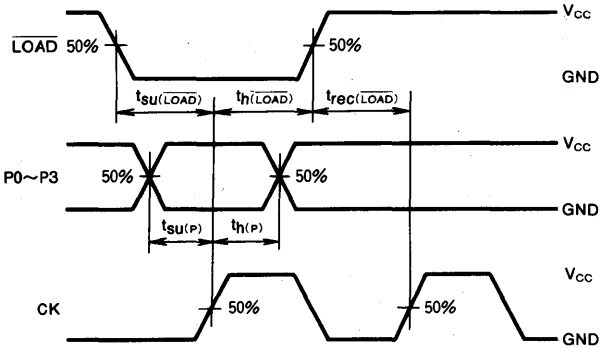


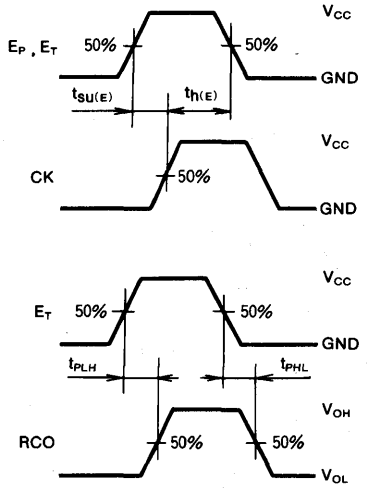
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

PRESETTABLE 4-BIT BINARY COUNTER WITH ASYNCHRONOUS RESET

TIMING DIAGRAM

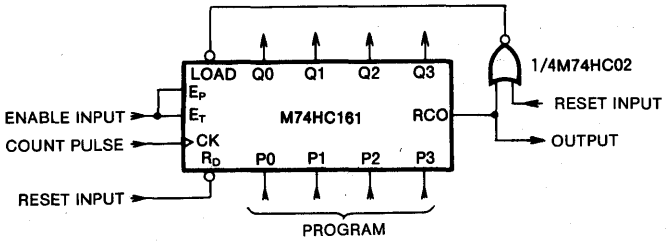






APPLICATION EXAMPLE

CONFIGURATION OF A PROGRAMMABLE DIVIDER



Note 5 : The reset function is invoked by setting the reset input to high and applying a count pulse. The $\overline{R_D}$ pin cannot be used in this application because it sets Q0 through Q3 to low.

P0	P1	P2	P3	Rate of division
L	L	L	L	1/16
H	L	L	L	1/15
L	H	L	L	1/14
H	H	L	L	1/13
L	L	H	L	1/12
H	L	H	L	1/11
L	H	H	L	1/10
H	H	H	L	1/9
L	L	L	H	1/8
H	L	L	H	1/7
L	H	L	H	1/6
H	H	L	H	1/5
L	L	H	H	1/4
H	L	H	H	1/3
L	H	H	H	1/2

M74HC162P/FP/DP

PRESETTABLE BCD COUNTER WITH SYNCHRONOUS RESET

DESCRIPTION

The M74HC162 is a semiconductor integrated circuit consisting of a presettable synchronous BCD counter with a synchronous reset input.

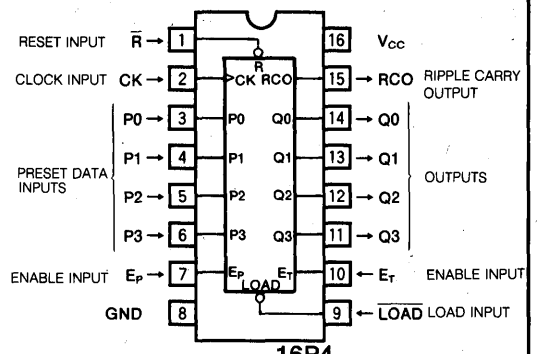
FEATURES

- Synchronous reset and preset inputs
- Enable input and ripple-carry output allow cascade connection
- Count frequency 45MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC162 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS162.

When the count pluse is applied to clock input CK, the number of count pulses will be output at outputs Q0 through Q3 synchronous with the count pulse in BCD code. Counting takes place when CK changes from low-level to high-level.

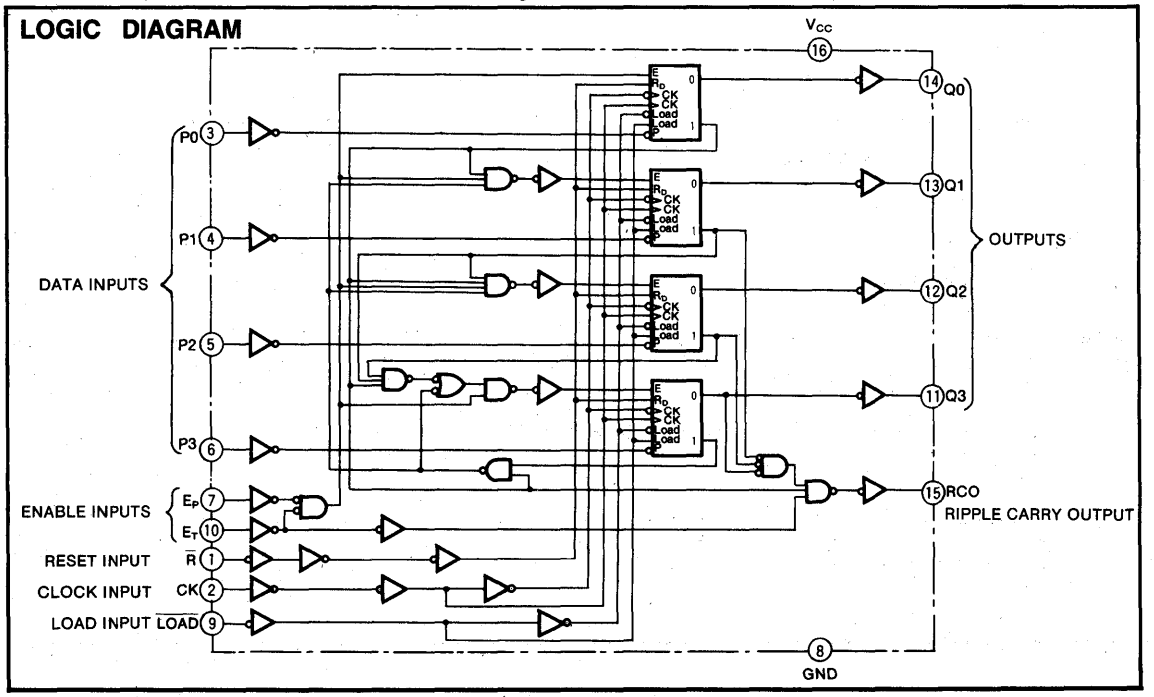
The preset functions synchronously with the count pulse. By supplying data to PERSET data inputs P0 through P3 and setting load input $\overline{LOAD}$ to low-level, when CK changes from low-level to high-level, the P0 through P3 signals will be output to Q0 through Q3, respectively, irrespective of enable inputs E_P and E_T. This permits presetting of the counter.

When values greater than 10 are preset, the count advances as shown in the State Transition Diagram.

The reset operates synchronously with the count pules, and by setting reset input $\overline{R}$ to low-level, Q0 through Q3 will become low when CK changes from low-level to high-level.

The ripple carry output RCO will become high only when Q0 is high, Q1 is low, Q2 is low, Q3 is high and E_T is high. E_P, E_T and RCO are used in cascade connections of the counter in synchronous from when the counter is used as a n-bit counter. (See the Application Example.)

LOGIC DIAGRAM



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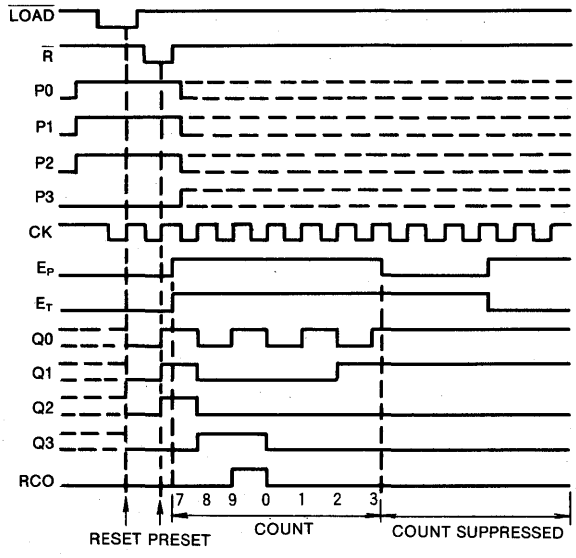
PRESETTABLE BCD COUNTER WITH SYNCHRONOUS RESET

FUNCTION TABLE (Note 1)

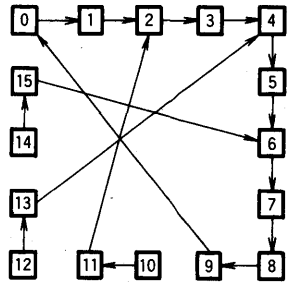
Inputs					Outputs				
$\overline{R}$	LOAD	E_T	E_P	CK	Q0	Q1	Q2	Q3	RCO
L	X	X	X	↑	L	L	L	L	L
H	L	L	X	↑	P0	P1	P2	P3	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Count suppressed				L
H	H	H	L	X	Count suppressed				L*

Note 1 : ↑ : Change from low to high (positive-edge trigger)
* : RCO is normally low, but will become high when Q0 is high, Q1 is low, Q2 is low, Q3 is high and E_T is high. Accordingly RCO = Q0 · $\overline{Q1}$ · $\overline{Q2}$ · Q3 · E_T
X : Irrelevant

OPERATION TIMING DIAGRAM



STATE TRANSITION DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC162FP, T_a = −40~+70℃ and T_a = 70~85℃ are derated at −6mW/℃.
M74HC162DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				28	ns
t_{PHL}	output propagation time (CK − Q)				34	ns
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time (E_T − RCO)				32	ns
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (CK − RCO)				36	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

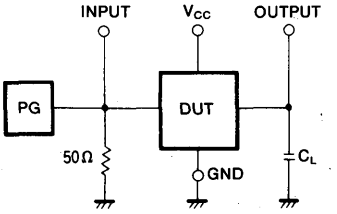
Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			205		258	ns
			4.5			41		52	
			6.0			35		44	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (E_T − RCO)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
t_{PHL}			2.0			195		246	ns
			4.5			39		49	
			6.0			33		42	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − RCO)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			215		271	ns
			4.5			43		54	
			6.0			37		46	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				58				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

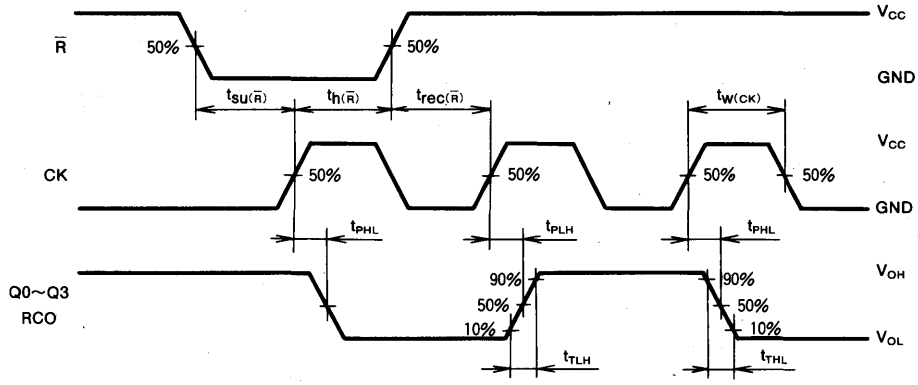
Symbol	Parameter	Test conditions	V_{CC}(V)	Limits 25℃ Min	Typ	Max	Limits −40~+85℃ Min	Max	Unit
$t_{w(CK)}$	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{su(P)}$	P setup time with respect to CK		2.0	150			189		ns
			4.5	30			38		
			6.0	26			32		
$t_{su(\overline{LOAD})}$	$\overline{LOAD}$ setup time with respect to CK		2.0	135			170		ns
			4.5	27			34		
			6.0	23			29		
$t_{su(\overline{R})}$	$\overline{R}$ setup time with respect to CK		2.0	160			202		ns
			4.5	32			40		
			6.0	27			34		
$t_{su(E)}$	E_T, E_P setup time with respect to CK		2.0	200			250		ns
			4.5	40			50		
			6.0	34			43		
$t_{h(P)}$	P hold time with respect to CK		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
$t_{h(\overline{LOAD})}$	$\overline{LOAD}$ hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{h(\overline{R})}$	$\overline{R}$ hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{h(E)}$	E_T, E_P hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{rec(\overline{R})}$	$\overline{R}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		
$t_{rec(\overline{LOAD})}$	$\overline{LOAD}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		

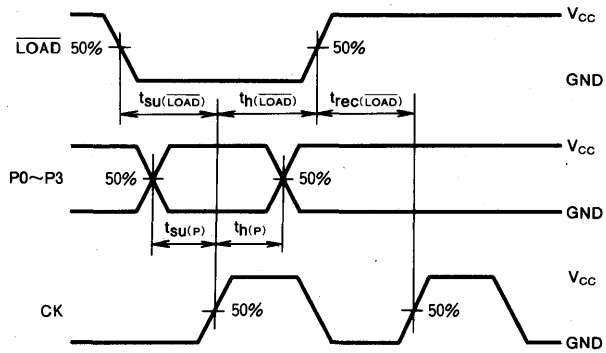
Note 4 : Test Circuit

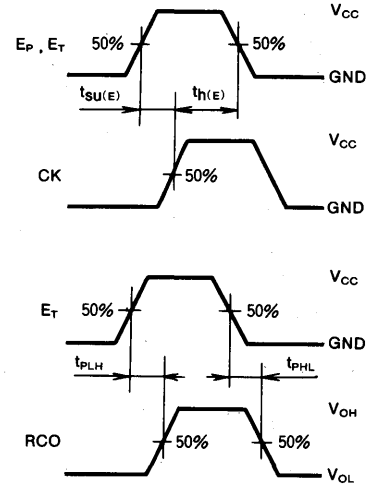


(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM

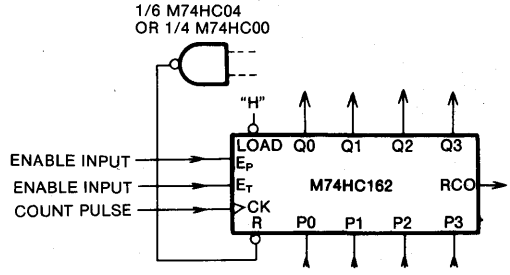






APPLICATION EXAMPLE

CONFIGURATION OF A BASE n COUNTER



BASE n COUNTER	PIN CONNECTED TO GATE INPUT
3	Q1
5	Q2
6	Q0, Q2
7	Q1, Q2
9	Q3

M74HC163P/FP/DP

PRESETTABLE 4-BIT BINARY COUNTER WITH SYNCHRONOUS RESET

DESCRIPTION

The M74HC163 is a semiconductor integrated circuit consisting of a presettable synchronous 4-bit binary (hexadecimal) counter with synchronous reset input.

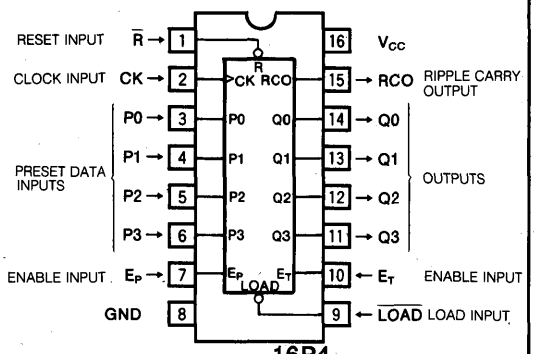
FEATURES

- synchronous reset and preset inputs
- Enable input and ripple-carry output allow cascade connection
- Count frequency: 45MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4 16P2N 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC163 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS163.

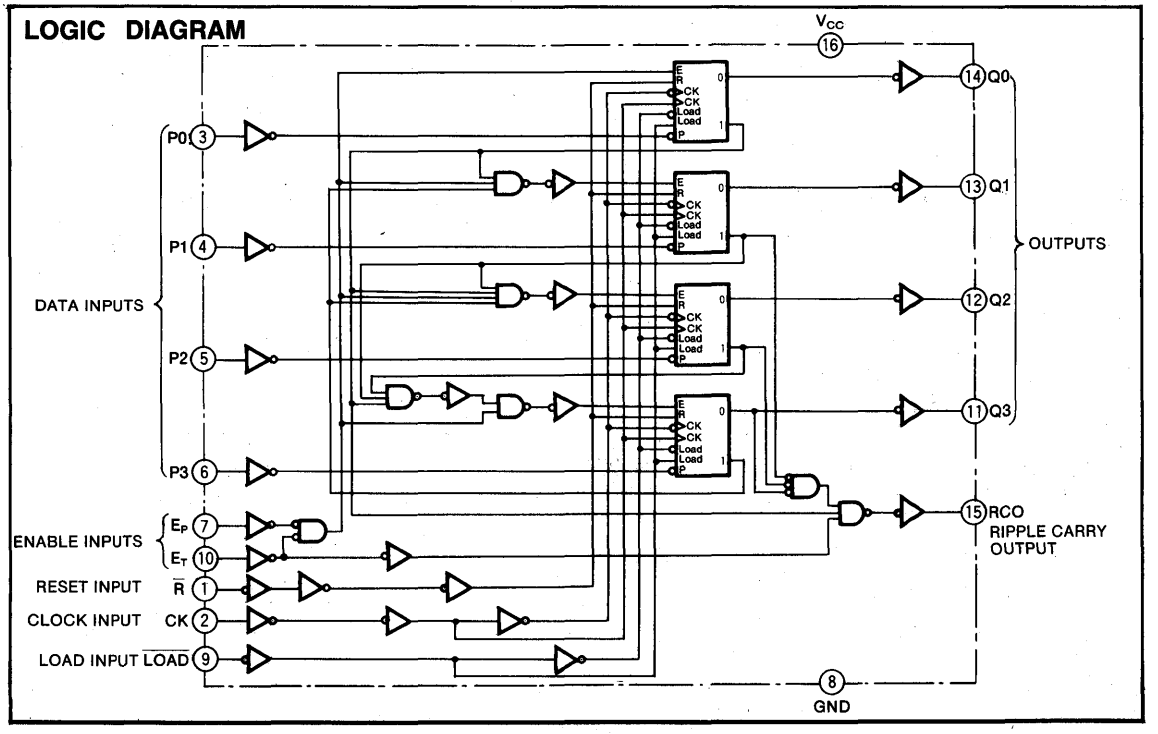
When the count pulse is applied to clock input CK, the number of count pulses will be output at outputs Q0 through Q3 synchronous with the count pulse in 4-bit binary code. Counting takes place when CK changes from low-level to high-level.

The preset functions synchronously with the count pulse. By supplying data to PERSET data inputs P0 through P3 and setting load input $\overline{LOAD}$ to low-level, when CK changes from low-level to high-level, the P0 through P3 signals will be output to Q0 through Q3, respectively, irrespective of enable inputs E_P and E_T. This permits persetting of the counter.

The reset operates synchronously with the count pules, and by setting reset input $\overline{R}$ to low-level, Q0 through Q3 will become low when CK changes from low-level to high-level.

The ripple carry output RCO will become high only when Q0, Q1, Q2, Q3 and E_T are high. E_P, E_T and RCO are used in cascade connections of the counter in synchronous from when the counter is used as a n-bit counter. (See the Application Example.)

LOGIC DIAGRAM



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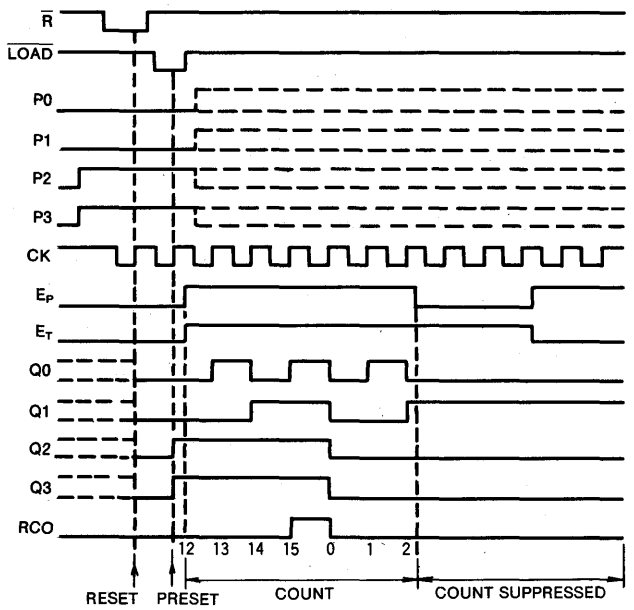
PRESETTABLE 4-BIT BINARY COUNTER WITH SYNCHRONOUS RESET

FUNCTION TABLE (Note 1)

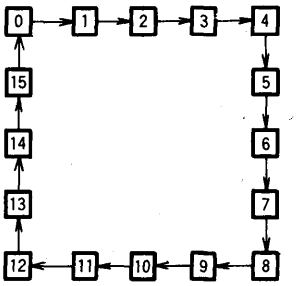
Inputs					Outputs				
$\overline{R}$	LOAD	E_T	E_P	CK	Q0	Q1	Q2	Q3	RCO
L	X	X	X	↑	L	L	L	L	L
H	L	L	X	↑	P0	P1	P2	P3	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Count suppressed				L
H	H	H	L	X	Count suppressed				L*

Note 1 : ↑ : Change from low to high (positive-edge trigger)
* : RCO is normally low, but will become high when all of Q0, Q1, Q2, Q3 and E_T are high. Accordingly, RCO = Q0 · Q1 · Q2 · Q3 · E_T
X : Irrelevant

OPERATION TIMING DIAGRAM



STATE TRANSITION DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC163FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC163DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

PRESETTABLE 4-BIT BINARY COUNTER WITH SYNCHRONOUS RESET

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent pupply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	C_L = 15pF (注4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				28	ns
t_{PHL}	output propagation time (CK − Q)				34	ns
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time (E_T − RCO)				32	ns
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (CK − RCO)				36	ns

PRESETTABLE 4-BIT BINARY COUNTER WITH SYNCHRONOUS RESET

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

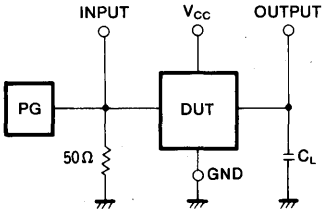
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			205		258	ns
			4.5			41		52	
			6.0			35		44	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (E_T − RCO)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
t_{PHL}			2.0			195		246	ns
			4.5			39		49	
			6.0			33		42	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − RCO)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			215		271	ns
			4.5			43		54	
			6.0			37		46	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				62				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{w(CK)}$	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{su(P)}$	P setup time with respect to CK		2.0	150			189		ns
			4.5	30			38		
			6.0	26			32		
$t_{su(\overline{LOAD})}$	$\overline{LOAD}$ setup time with respect to CK		2.0	135			170		ns
			4.5	27			34		
			6.0	23			29		
$t_{su(\overline{R})}$	$\overline{R}$ setup time with respect to CK		2.0	160			202		ns
			4.5	32			40		
			6.0	27			34		
$t_{su(E)}$	E_T, E_P setup time with respect to CK		2.0	200			250		ns
			4.5	40			50		
			6.0	34			43		
$t_{h(P)}$	P hold time with respect to CK		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
$t_{h(\overline{LOAD})}$	$\overline{LOAD}$ hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{h(\overline{R})}$	$\overline{R}$ hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{h(E)}$	E_T, E_P hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{rec(\overline{R})}$	$\overline{R}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		
$t_{rec(\overline{LOAD})}$	$\overline{LOAD}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		

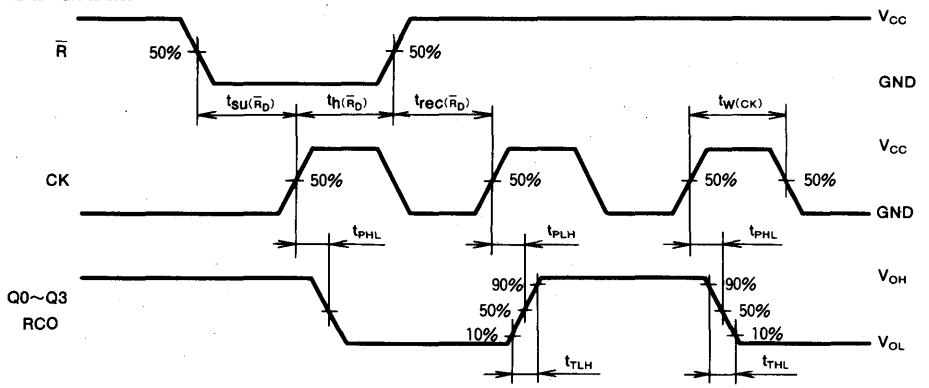
Note 4 : Test Circuit

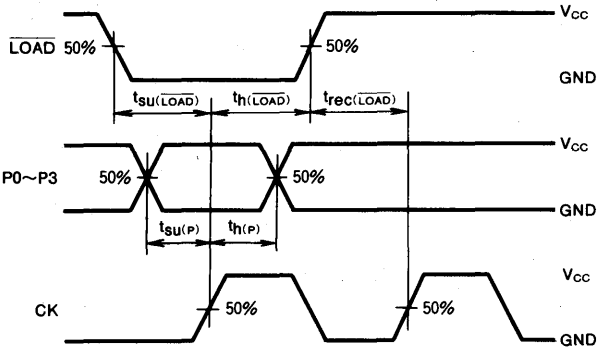


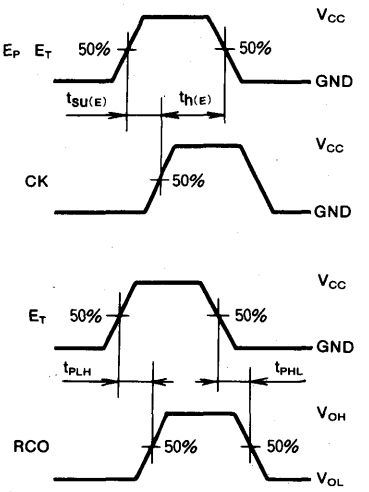
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

PRESETTABLE 4-BIT BINARY COUNTER WITH SYNCHRONOUS RESET

TIMING DIAGRAM

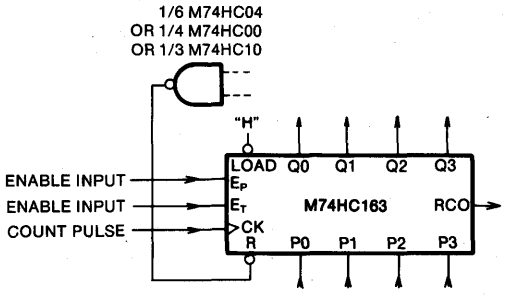






APPLICATION EXAMPLE

CONFIGURATION OF A BASE n COUNTER



BASE	PIN CONNECTED TO GATE INPUT
3	Q1
5	Q2
6	Q0, Q2
7	Q1, Q2
9	Q3
10	Q0, Q3
11	Q1, Q3
12	Q0, Q1, Q3
13	Q2, Q3
14	Q0, Q2, Q3
15	Q1, Q2, Q3

M74HC164P/FP/DP

8-BIT SERIAL-INPUT/PARALLEL-OUTPUT SHIFT REGISTER

DESCRIPTION

The M74HC164 is a semiconductor integrated circuit consisting of an 8-bit serial-input serial/parallel-output shift register with direct reset input.

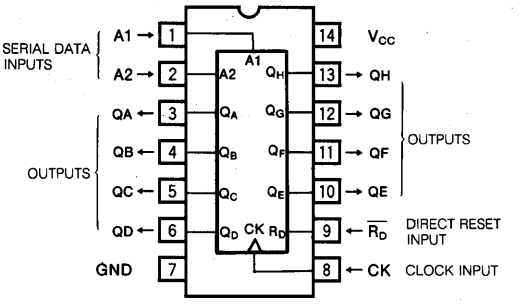
FEATURES

- High-speed: (Clock frequency) 60MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC164 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS164.

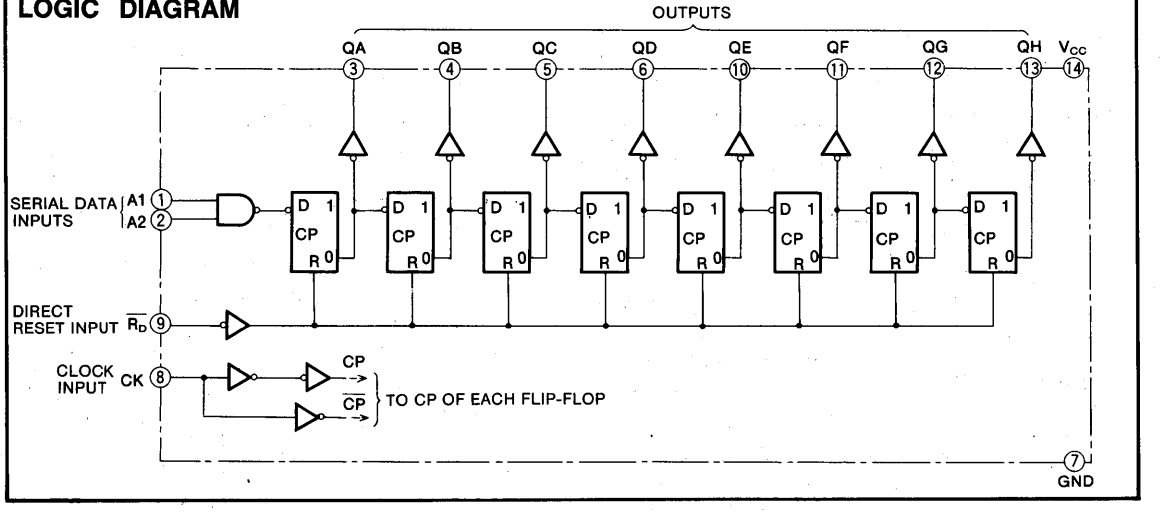
The M74HC164 consists of eight edge-triggered D-type flip-flops. The logical product A1-A2 of the serial data inputs A1 and A2 acts as the shift register input. QA through QH are taken out from the outputs of each flip-flop.

When both A1 and A2 are high, and the clock pulse is applied to clock input CK, the high-level signals will be shifted synchronously with the clock pulse in the order of QA-QH.

When at least one of A1 or A2 is low, the low-level signal will be shifted synchronously with the clock pulse. The shift operation will take place when CK changes from low-level to high-level.

When the direct reset input $\overline{R_D}$ is low, all outputs will be reset to low-level irrespective of other inputs. When used as a shift register, $\overline{R_D}$ should be maintained at high-level.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

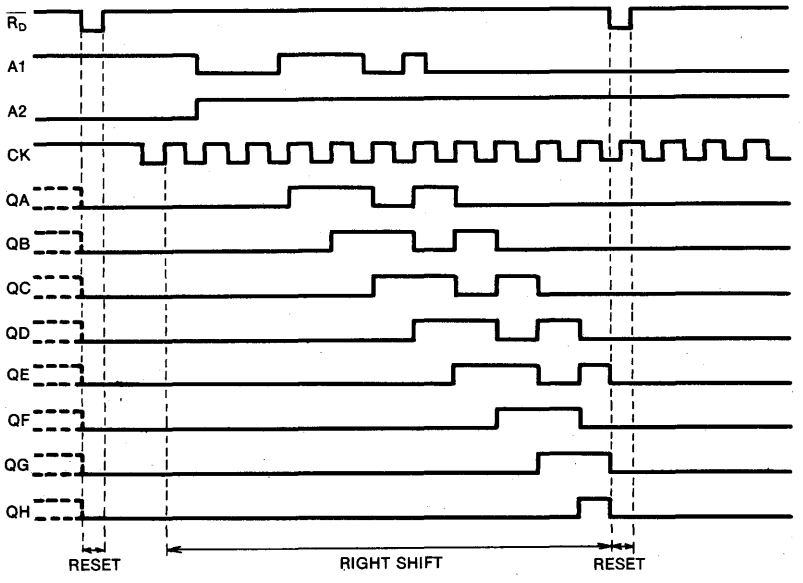
8-BIT SERIAL-INPUT/PARALLEL-OUTPUT SHIFT REGISTER

FUNCTION TABLE (Note 1)

Operating mode	Inputs				Outputs							
	$\overline{R_D}$	CK	A1	A2	QA	QB	QC	QD	QE	QF	QG	QH
Reset	L	X	X	X	L	L	L	L	L	L	L	L
Right shift	H	↑	L	L	L	QA^0	QB^0	QC^0	QD^0	QE^0	QF^0	QG^0
	H	↑	H	L	L	QA^0	QB^0	QC^0	QD^0	QE^0	QF^0	QG^0
	H	↑	L	H	L	QA^0	QB^0	QC^0	QD^0	QE^0	QF^0	QG^0
	H	↑	H	H	H	QA^0	QB^0	QC^0	QD^0	QE^0	QF^0	QG^0
No change	H	↓	X	X	QA^0	QB^0	QC^0	QD^0	QE^0	QF^0	QG^0	QH^0

Note 1 : ↑ : Change from low-level to high-level
↓ : Change from high-level to low-level
Q^0 : Output state before clock input changed
X : Irrelevant

OPERATING TIMING DIAGRAM



8-BIT SERIAL-INPUT/PARALLEL-OUTPUT SHIFT REGISTER

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC164FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC164DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −4.0mA	4.5	4.18			4.13		
		I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 4.0mA	4.5			0.26		0.33	
		I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				30	ns
t_{PHL}					30	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				35	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

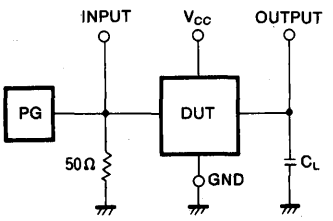
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			175		218	ns
			4.5			35		44	
			6.0			30		38	
t_{PHL}			2.0			175		218	ns
			4.5			35		44	
			6.0			30		38	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			205		256	ns
			4.5			41		51	
			6.0			35		44	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				150				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

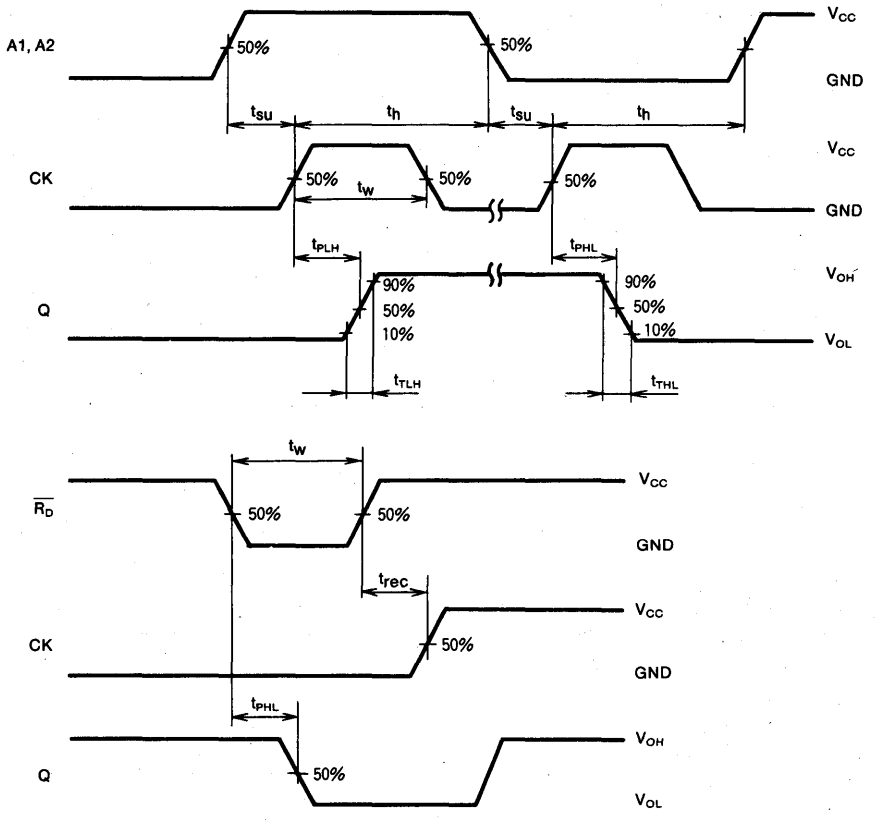
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{R_D}$ clock pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
t_{su}	A setup time with respect to CK		2.0	50			65		ns
			4.5	10			13		
			6.0	9			11		
t_h	A hold time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		
t_{rec}	$\overline{R_D}$ recovery time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC165P/FP/DP

8-BIT SERIAL-OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER

DESCRIPTION

The M74HC165 is a semiconductor integrated circuit consisting of an 8-bit serial- or parallel-input/serial output shift register.

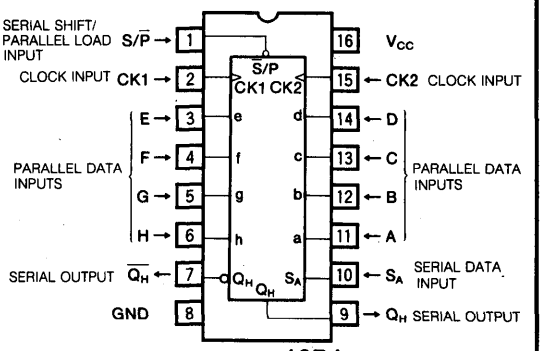
FEATURES

- High-speed: 40MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

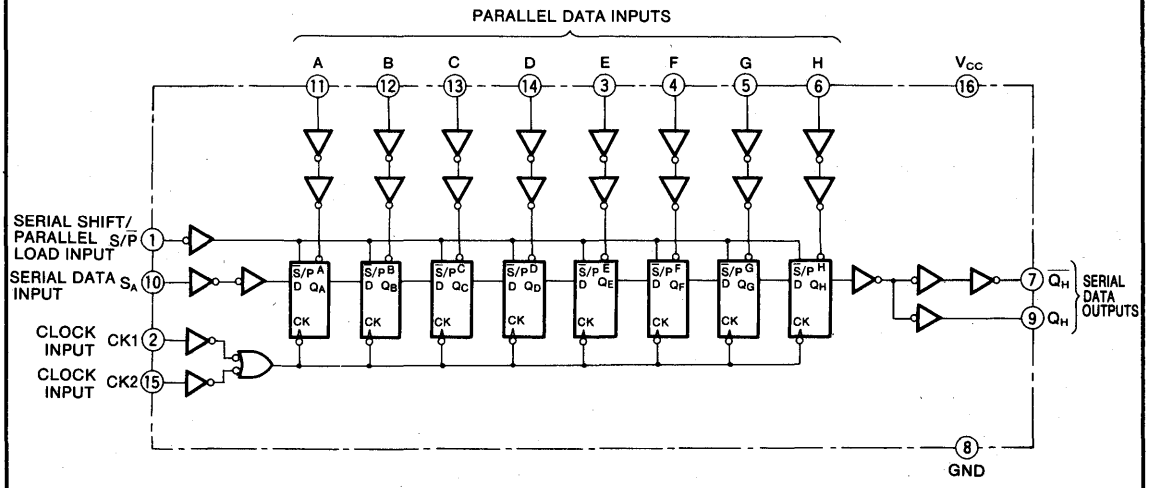
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC165 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS165.

The parallel or serial input mode is selected by serial shift/parallel load input S/$\overline{P}$ signal. When S/$\overline{P}$ is high, serial data input S_A operates and the 8-bit flip flop operates serial shifts with the clock pulse. When S/$\overline{P}$ is low, parallel data inputs A~H operate. As A~H enter direct set, direct reset of each flip flop, irrespective of other inputs be read. Serial data transfer is suspended while parallel loading takes place. The load and shift operation takes place when clock input CK1 or CK2 changes from low to high.

For permit use of combination of two clock or use of one prohibition clock input, clock is 2-input NOR gate. When either input is maintained high, the clock operation stops. When it is maintained low, the data transfer is possible.

LOGIC DIAGRAM



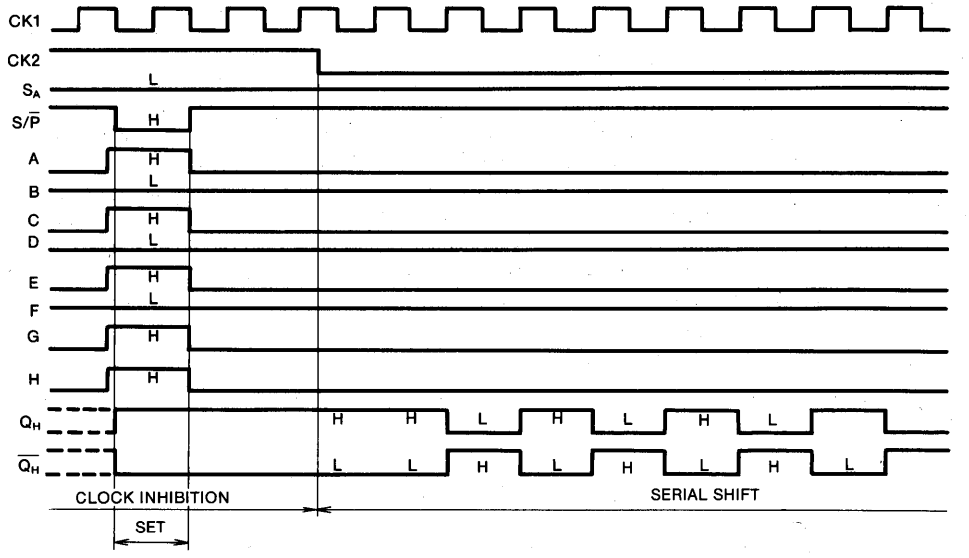
8-BIT SERIAL-OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER

FUNCTION TABLE (Note 1)

Operating mode	Inputs					Outputs								
						Internal							Q_H	$\overline{Q_H}$
	$S/\overline{P}$	CK1	CK2	S_A	A~H	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G		
Load	L	X	X	X	a~h	a	b	c	d	e	f	g	h	$\overline{h}$
Shift	H	↑	L	L	X	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	$\overline{Q_G}^0$
	H	↑	L	H	X	H	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	$\overline{Q_G}^0$
	H	L	↑	L	X	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	$\overline{Q_G}^0$
	H	L	↑	H	X	H	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	$\overline{Q_G}^0$
Clock inhibition	H	H	X	X	X	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	$\overline{Q_H}^0$
	H	X	H	X	X	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	$\overline{Q_H}^0$
No change	H	X	X	X	X	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	$\overline{Q_H}^0$

Note 1 : X : Irrelevant
↑ : Change from low to high
Q^0 : Output state before clock input changed

OPERATING TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC165FP, T_a = −40~+70℃ and T_a = 70~85℃ are derated at −6mW/℃.
M74HC165DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

8-BIT SERIAL-OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q_H or $\overline{Q_H}$)				25	ns
t_{PHL}					25	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S/$\overline{P}$ − Q_H or $\overline{Q_H}$)				30	ns
t_{PHL}					30	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (H − Q_H or $\overline{Q_H}$)				25	ns
t_{PHL}					25	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

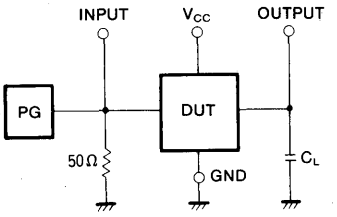
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ.	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (Clock − Q_H, $\overline{Q_H}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($S/\overline{P}$ − Q_H or $\overline{Q_H}$)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (H − Q_H or $\overline{Q_H}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

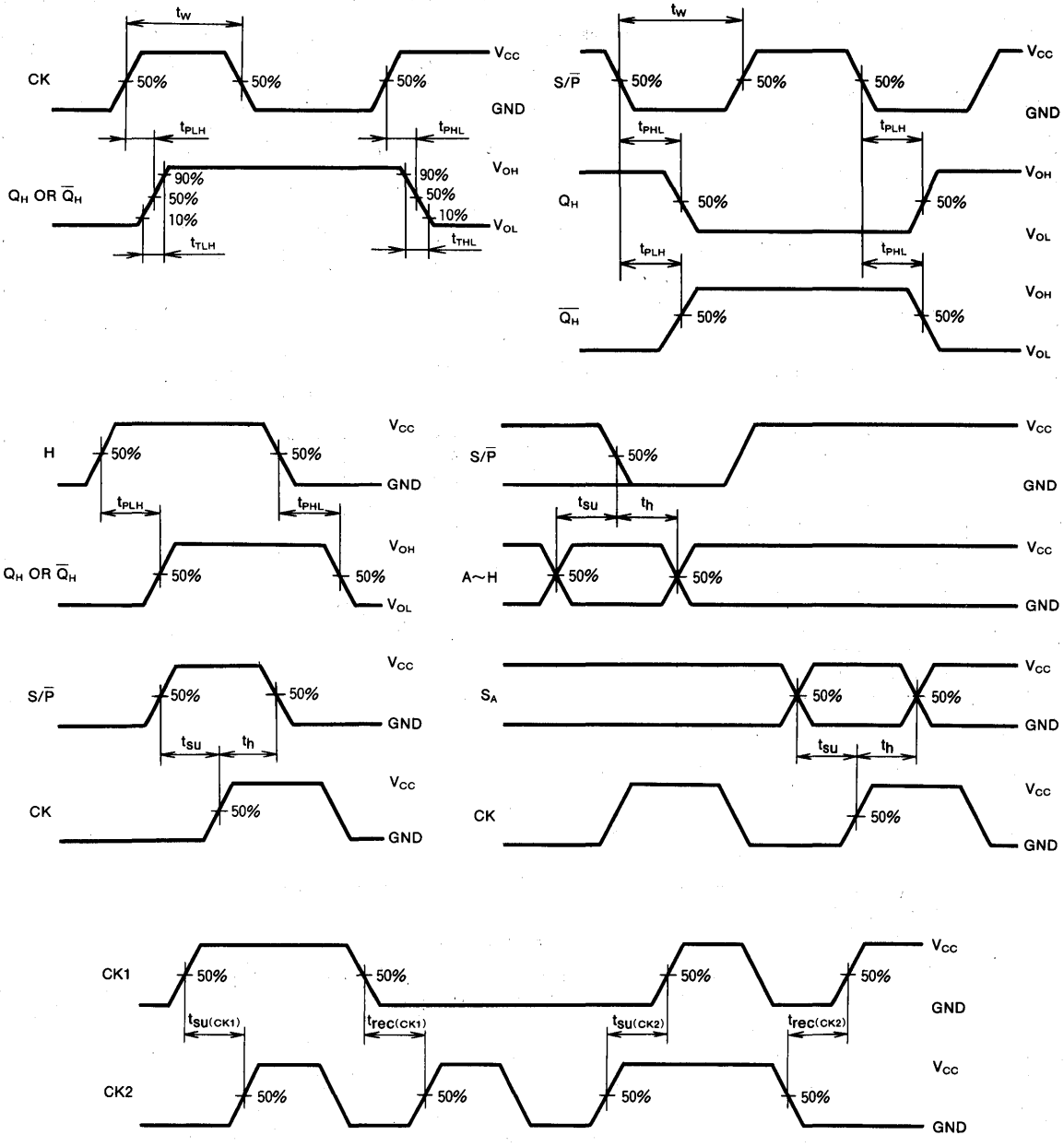
Symbol	Parameter	Test conditions	Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Clock pulse width Load pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	S_A setup time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
	S/$\overline{P}$ setup time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
	A~H setup time with respect to S/$\overline{P}$		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
	CK1 setup time with respect to CK2 CK2 setup time with respect to CK1		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	S_A hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
	S/$\overline{P}$ hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
	A~H hold time with respect to S/$\overline{P}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	CK1 recovery time with respect to CK2 CK2 recovery time with respect to CK1		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC166P/FP/DP

8-BIT SERIAL-OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH RESET

DESCRIPTION

The M74HC166 is a semiconductor integrated circuit consisting of an 8-input serial/parallel-input serial-output shift register.

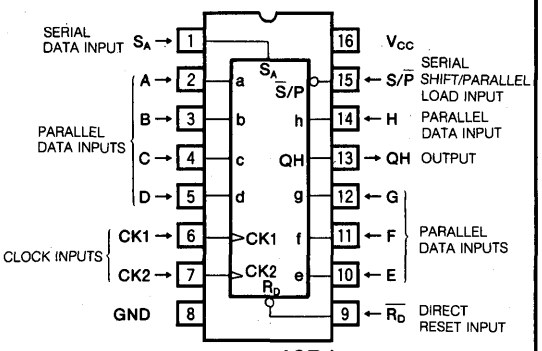
FEATURES

- High-speed: (Clock frequency) 60MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

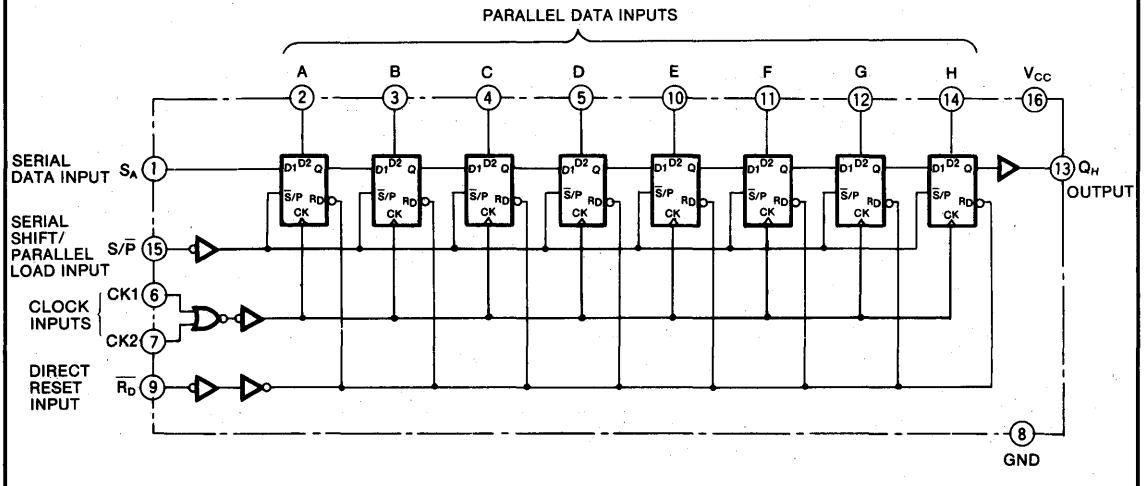
Use of silicon gate technology allows the M74HC166 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS166.

Parallel or serial input modes can be selected by the signal of the serial-shift/parallel-load input S/$\overline{P}$. When S/$\overline{P}$ is high, serial data input S_A is enabled and 8-bit flip-flop is possible to do serial shift by the clock pulse. When S/$\overline{P}$ is low, parallel data inputs A through H are enabled and the input data is loaded syncrnously with the next clock pulse. During the parallel load, transfer of serial data is suppressed. Shift or load is enabled when clock input CK1 or CK2 changes from low-level to high-level.

The clock employs a 2-input NOR, with usable in combination or with either input usable as a clock suppressing input. When one of the inputs is held at high-level, the clock stops; when held at low-level, data transfer is enabled.

When direct reset input $\overline{R_D}$ is low, the shift register is reset irrespective of other inputs.

LOGIC DIAGRAM



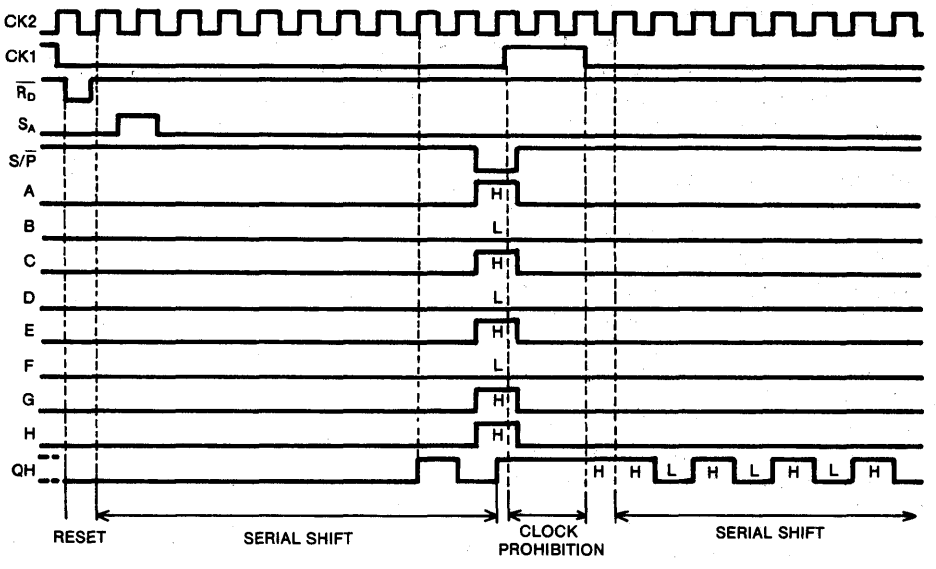
8-BIT SERIAL-OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH RESET

FUNCTION TABLE (Note 1)

Operating mode	Inputs						Outputs		
							Internal		
	$\overline{R_D}$	S/$\overline{P}$	CK1	CK2	S_A	A~H	Q_A	Q_B	Q_H
Load	H	L	X	X	X	a~h	a	b	h
Shift	H	H	↑	L	L	X	L	Q_A^0	Q_G^0
	H	H	↑	L	H	X	H	Q_A^0	Q_G^0
	H	H	L	↑	L	X	L	Q_A^0	Q_G^0
	H	H	L	↑	H	X	H	Q_A^0	Q_G^0
Clock prohibition	H	H	H	X	X	X	Q_A^0	Q_B^0	Q_H^0
	H	H	X	H	X	X	Q_A^0	Q_B^0	Q_H^0
No change	H	H	L	L	X	X	Q_A^0	Q_B^0	Q_H^0
Reset	L	X	X	X	X	X	L	L	L

Note 1 : X : Irrelevent
↑ : Change from low-level to high-level
Q^0 : Output state before clock input changed

OPERATING TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC166FP, T_a = −40~+70℃ and T_a = 70~85℃ are derated at −6mW/℃.
M74HC166DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

8-BIT SERIAL-OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH RESET

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q_H)				25	ns
t_{PHL}					25	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q_H)				25	ns

8-BIT SERIAL-OR
PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH RESET

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	6			5		MHz
			4.5	31			25		
			6.0	36			29		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q_H)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		190	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q_H)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		32	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				76				pF

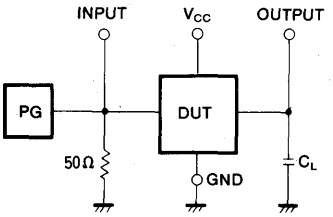
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

8-BIT SERIAL-OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH RESET

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{W(CK)}$	Clock pulse width	2.0	80			100		ns
		4.5	16			20		
		6.0	14			17		
$t_{W(\overline{R_D})}$	Direct reset pulse width	2.0	100			125		ns
		4.5	20			25		
		6.0	17			21		
$t_{SU(A\sim H)}$	A~H setup time with respect to CK	2.0	80			100		ns
		4.5	16			20		
		6.0	14			17		
$t_{SU(S_A)}$	S_A setup time with respect to CK	2.0	80			100		ns
		4.5	16			20		
		6.0	14			17		
$t_{SU(S/\overline{P})}$	$S/\overline{P}$ setup time with respect to CK	2.0	145			180		ns
		4.5	29			36		
		6.0	25			31		
$t_{SU(CK1)}$	CK1 setup time with respect to CK2	2.0	100			125		ns
		4.5	20			25		
		6.0	17			21		
$t_{SU(CK2)}$	CK2 setup time with respect to CK1	2.0	100			125		ns
		4.5	20			25		
		6.0	17			21		
$t_{h(A\sim H)}$	A~H hold time with respect to CK	2.0	5			5		ns
		4.5	5			5		
		6.0	5			5		
$t_{h(S_A)}$	S_A hold time with respect to CK	2.0	5			5		ns
		4.5	5			5		
		6.0	5			5		
$t_{h(S/\overline{P})}$	$S/\overline{P}$ hold time with respect to CK	2.0	0			0		ns
		4.5	0			0		
		6.0	0			0		
$t_{rec(CK1)}$	CK1 recovery time with respect to CK2	2.0	100			125		ns
		4.5	20			25		
		6.0	17			21		
$t_{rec(CK2)}$	CK2 recovery time with respect to CK1	2.0	100			125		ns
		4.5	20			25		
		6.0	17			21		
$t_{rec(\overline{R_D})}$	$\overline{R_D}$ recovery time with respect to CK	2.0	40			50		ns
		4.5	8			10		
		6.0	7			9		

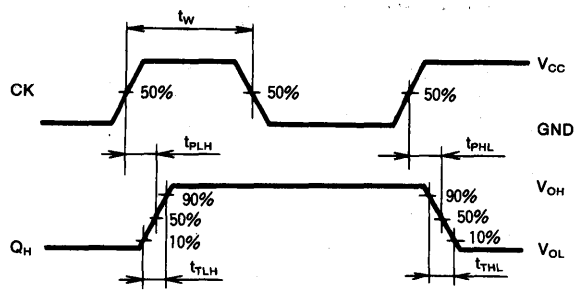
Note 4 : Test Circuit

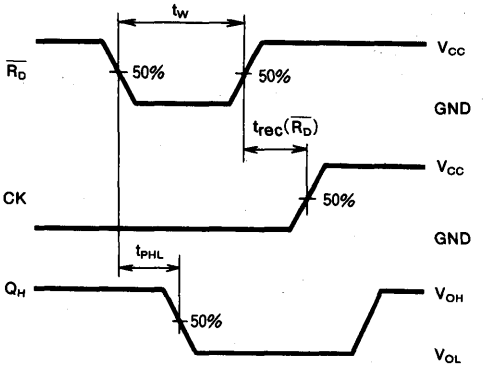


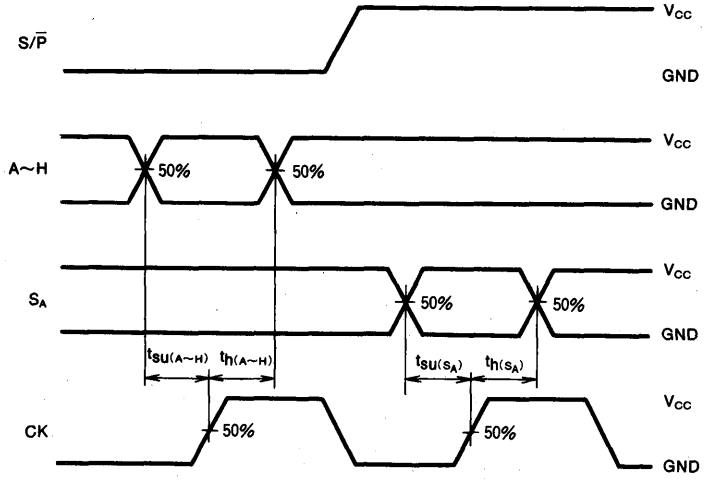
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

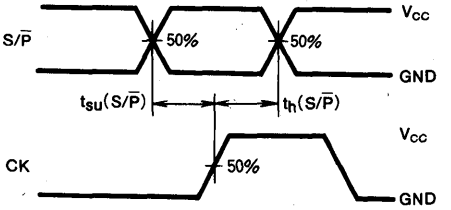
8-BIT SERIAL-OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH RESET

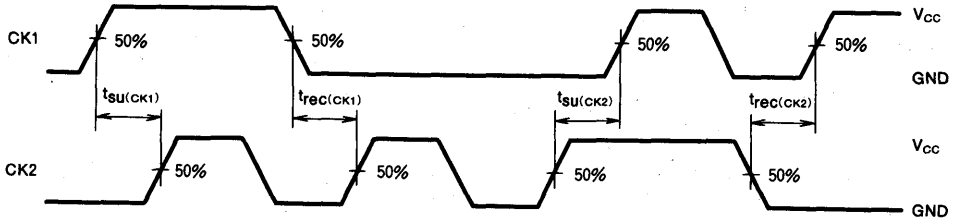
TIMING DIAGRAM











MITSUBISHI ELECTRIC

M74HC173P/FP/DP

QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

The M74HC173 is a semiconductor integrated circuit consisting of a 4-bit register with 3-state output.

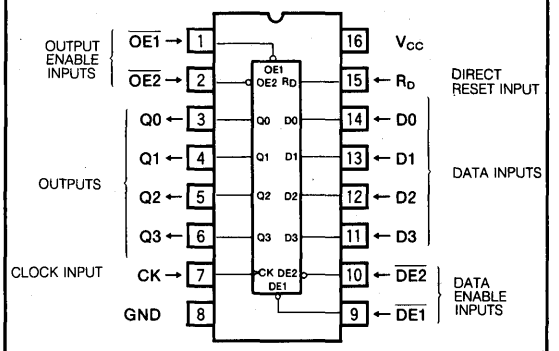
FEATURES

- High-speed: (clock frequency) 60MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

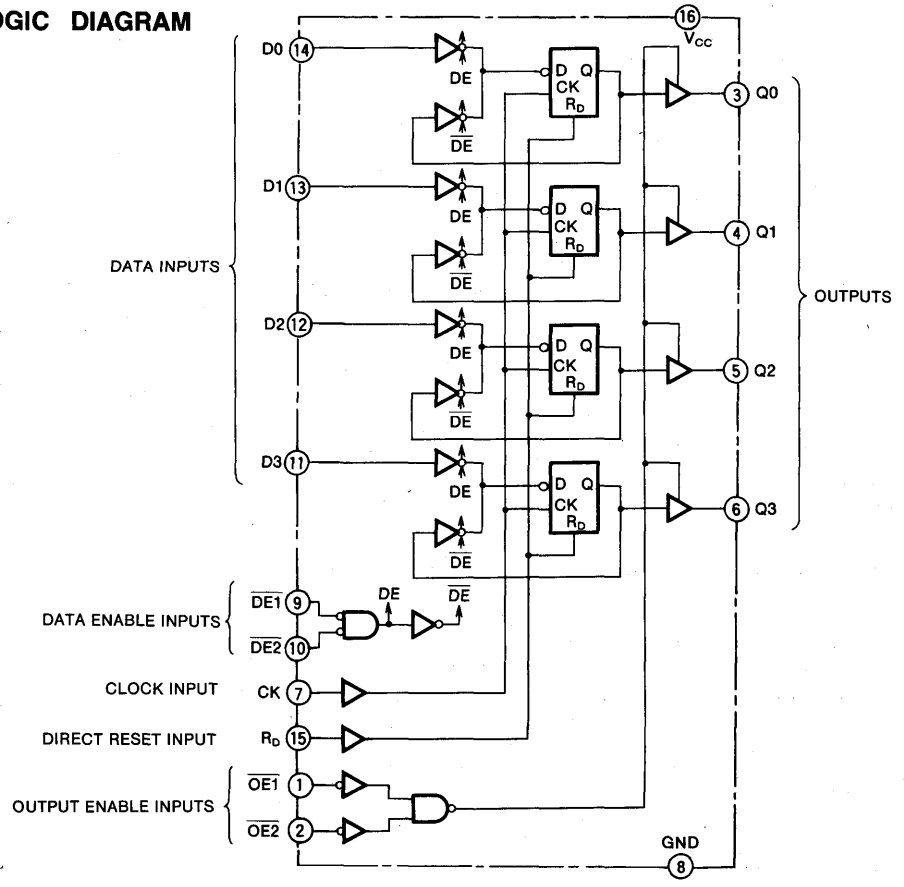
General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

LOGIC DIAGRAM



QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC173 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS173.

The M74HC173 contains four edge-triggered D-type flip-flops with common direct reset input R_D and common clock input CK.

When CK changes from low-level to high-level, the signals just previously input at D appears at outputs Q in accordance with the function table given.

When R_D becomes high while output enable inputs $\overline{OE1}$ and $\overline{OE2}$ are held low, all outputs Q become low-level irrespective of other inputs.

When one of data enable inputs $\overline{DE1}$ or $\overline{DE2}$ is high, while $\overline{OE1}$, $\overline{OE2}$ and R_D are held low, output Q is maintained.

When either $\overline{OE1}$ or $\overline{OE2}$ is high, all outputs Q will become the high-impedance state, and the contents of the flip-flop are not affected even when $\overline{OE1}$ and $\overline{OE2}$ are changed.

When used as a D-type flip-flop, $\overline{OE1}$, $\overline{OE2}$, R_D, $\overline{DE1}$ and $\overline{DE2}$ should all be maintained at low-level.

FUNCTION TABLE (Note 1)

Inputs							Output
$\overline{OE1}$	$\overline{OE2}$	R_D	CK	$\overline{DE1}$	$\overline{DE2}$	D	Q
L	L	H	X	X	X	X	L
L	L	L	L	X	X	X	Q^0
L	L	L	H	X	X	X	Q^0
L	L	L	↑	H	X	X	Q^0
L	L	L	↑	X	H	X	Q^0
L	L	L	↑	L	L	L	L
L	L	L	↑	L	L	H	H
L	L	L	↓	X	X	X	Q^0
L	H	X	X	X	X	X	Z
H	L	X	X	X	X	X	Z
H	H	X	X	X	X	X	Z

Note 1 : Z : High impedance
X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level
Q_0 : Output state Q before clock input changed.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC173FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −7mW/℃
M74HC173DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9			V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 6.0mA	4.5		0.26		0.33	
			I_{OL} = 7.8mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0		−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0		0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0		−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0		4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				31	ns
t_{PHL}	output propagation time (CK − Q)				31	ns
t_{PHL}	High-level to low-level output propagation time (R_D − Q)				27	ns
t_{PLZ}	Low-level, high-level output disable time	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}	($\overline{OE}$ − Q)				25	ns
t_{PZL}	Low-level, high-level output enable time	C_L = 50pF (Note 4)			28	ns
t_{PZH}	($\overline{OE}$ − Q)				28	ns

QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maxmum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)	C_L = 50pF (Note 4)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}		C_L = 150pF (Note 4)	2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PHL}			2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PHL}	High-level to low-level output propagation time (R_D − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PLZ}	Low-level, high-level output disable time ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Low-level, high-level output enable time ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				45				pF

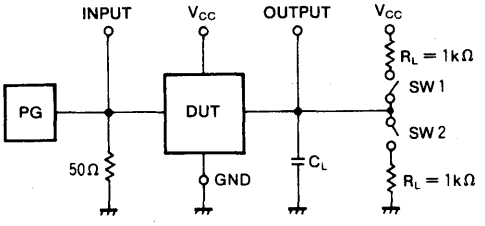
Note 3 : C_{DP} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, R_D Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D, $\overline{DE}$ setup time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	D, $\overline{DE}$ hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	R_D recovery time with respect to CK		2.0	90			113		ns
			4.5	18			23		
			6.0	15			19		

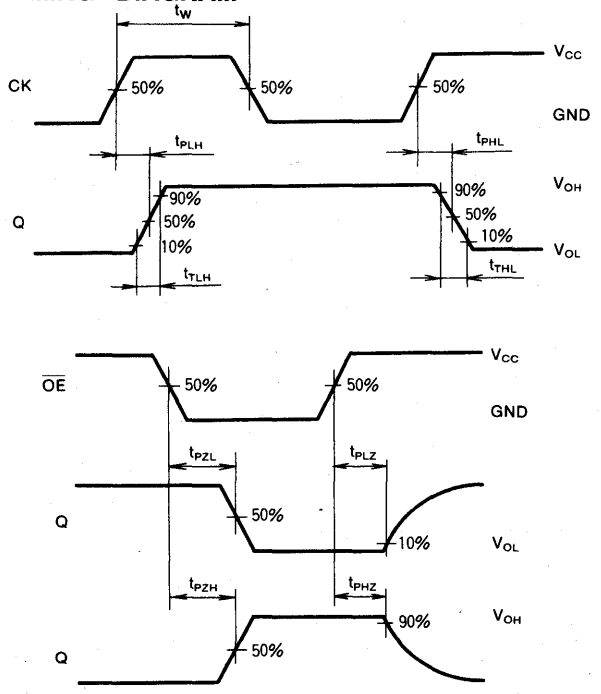
Note 4 : Test Circuit

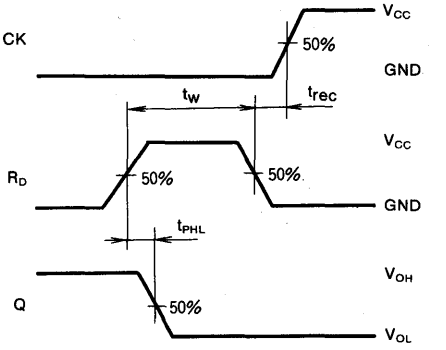


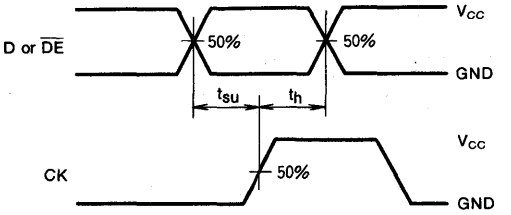
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







M74HC174P/FP/DP

HEX D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

The M74HC174 is a semiconductor integrated circuit consisting of six positive-edge triggered D-type flip flops with common clock and direct reset inputs.

FEATURES

- High-speed: (clock frequency) 60MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

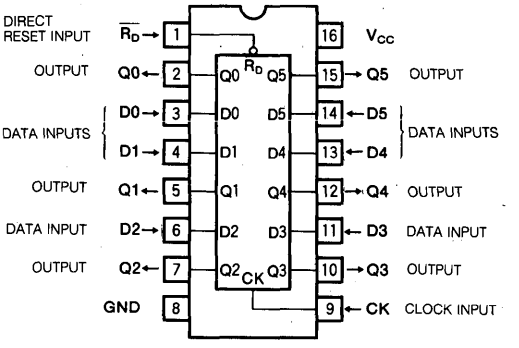
Use of silicon gate technology allows the M74HC174 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS174.

The M74HC174 contains six internal edge-triggered D-type flip-flops with common direct reset input $\overline{R_D}$ and common clock input CK.

When CK changes from low-level to high-level, the signals' just previously input D appears at outputs Q in accordance with the function table given. When $\overline{R_D}$ is low, all outputs Q will become low irrespective of other inputs.

When used as a D-type flip-flop, $\overline{R_D}$ should be maintained at high-level.

PIN CONFIGURATION (TOP VIEW)



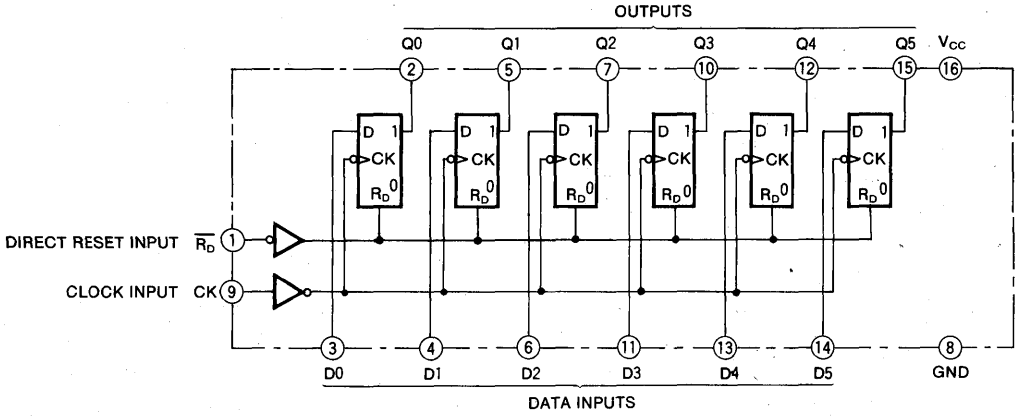
Outline 16P4, 16P2N, 16P2P

FUNCTION TABLE (Note 1)

Inputs			Outputs
$\overline{R_D}$	CK	D	Q
H	↑	H	H
H	↑	L	L
H	↓	X	Q^0
L	X	X	L
H	L	X	Q^0

Note 1 : X : Irrelevant
↑ : Change from low to high
↓ : Change from high to low
Q^0 : Output state Q before clock input changed

LOGIC DIAGRAM



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HEX D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC174FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC174DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				30	ns
t_{PHL}					30	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				30	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

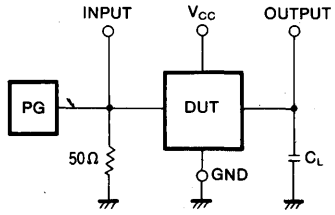
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			165		206	ns
			4.5			33		41	
			6.0			28		35	
t_{PHL}			2.0			165		206	ns
			4.5			33		41	
			6.0			28		35	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			165		206	ns
			4.5			33		41	
			6.0			28		35	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				64				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

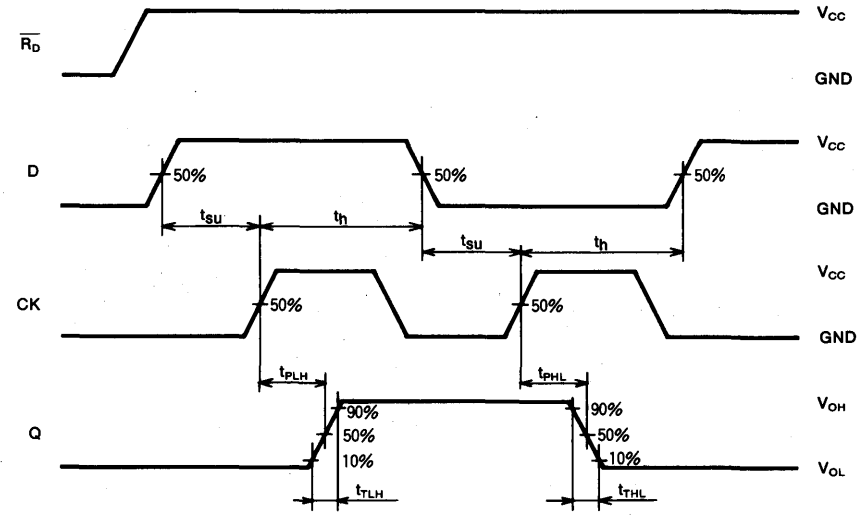
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{w(CK)}$	Clock pulse width		2.0	80			106		ns
			4.5	16			20		
			6.0	14			18		
$t_{w(\overline{R_D})}$	Direct reset pulse width		2.0	80			106		ns
			4.5	16			20		
			6.0	14			18		
t_{su}	D setup time with respect to CK		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	D hold time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		
t_{rec}	$\overline{R_D}$ recovery time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

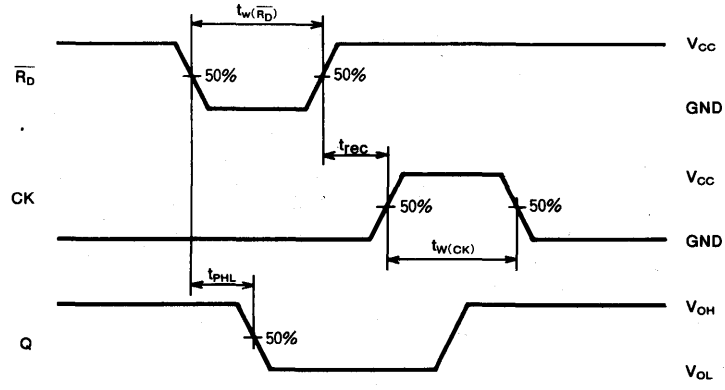
Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC175P/FP/DP

QUADRUPLE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

The M74HC175 is a semiconductor integrated circuit consisting of four positive-edge-triggered D-type flip flops with common clock and direct reset inputs.

FEATURES

- High-speed: (clock frequency) 60MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

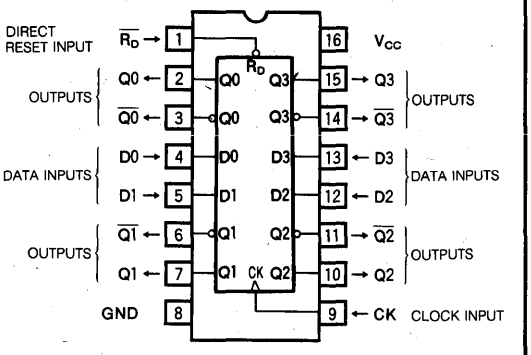
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC175 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS175.

The M74HC175 contains four edge-triggered D-type flip-flops with common direct reset input $\overline{R_D}$ and common clock input CK.

PIN CONFIGURATION (TOP VIEW)



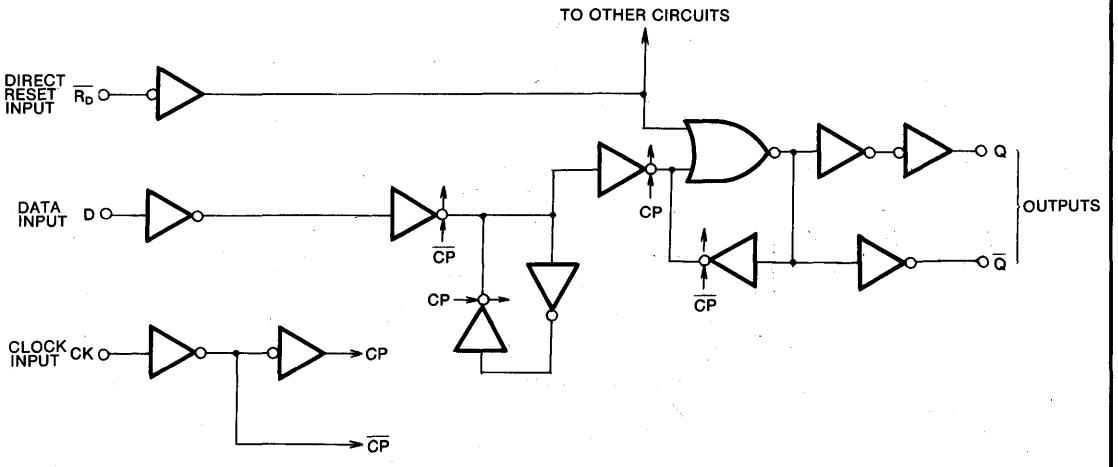
16P4
Outline 16P2N
16P2P

When CK changes from low-level to high-level, the signals just previously input at D appears at outputs Q and $\overline{Q}$ in accordance with the function table given.

When $\overline{R_D}$ is low, output Q and $\overline{Q}$ will become low and high irrespective of other inputs.

When used as a D-type flip flop, $\overline{R_D}$ should be maintained at high-level.

LOGIC DIAGRAM



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QUADRUPLE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

FUNCTION TABLE (Note 1)

Inputs			Outputs	
$\overline{R_D}$	CK	D	Q	$\overline{Q}$
H	↑	H	H	L
H	↑	L	L	H
H	↓	X	Q^0	$\overline{Q^0}$
H	L	X	Q^0	$\overline{Q^0}$
L	X	X	L	H

Note 1 : X : Irrelevant
↑ : Change from low to high
↓ : Change from high to low
Q^0 : Output state Q before clock input changed
$\overline{Q^0}$: Output state Q before clock input changed

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC175FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC175DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

QUADRUPLE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time (CK−Q, $\overline{Q}$)				25	ns
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time ($\overline{R_D}$−Q, $\overline{Q}$)				20	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

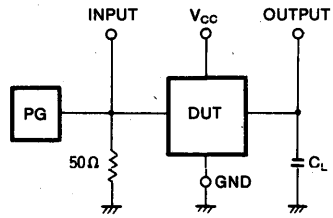
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	6			5		MHz
			4.5	30			24		
			6.0	35			28		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q, $\overline{Q}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$−Q, $\overline{Q}$)		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				52				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

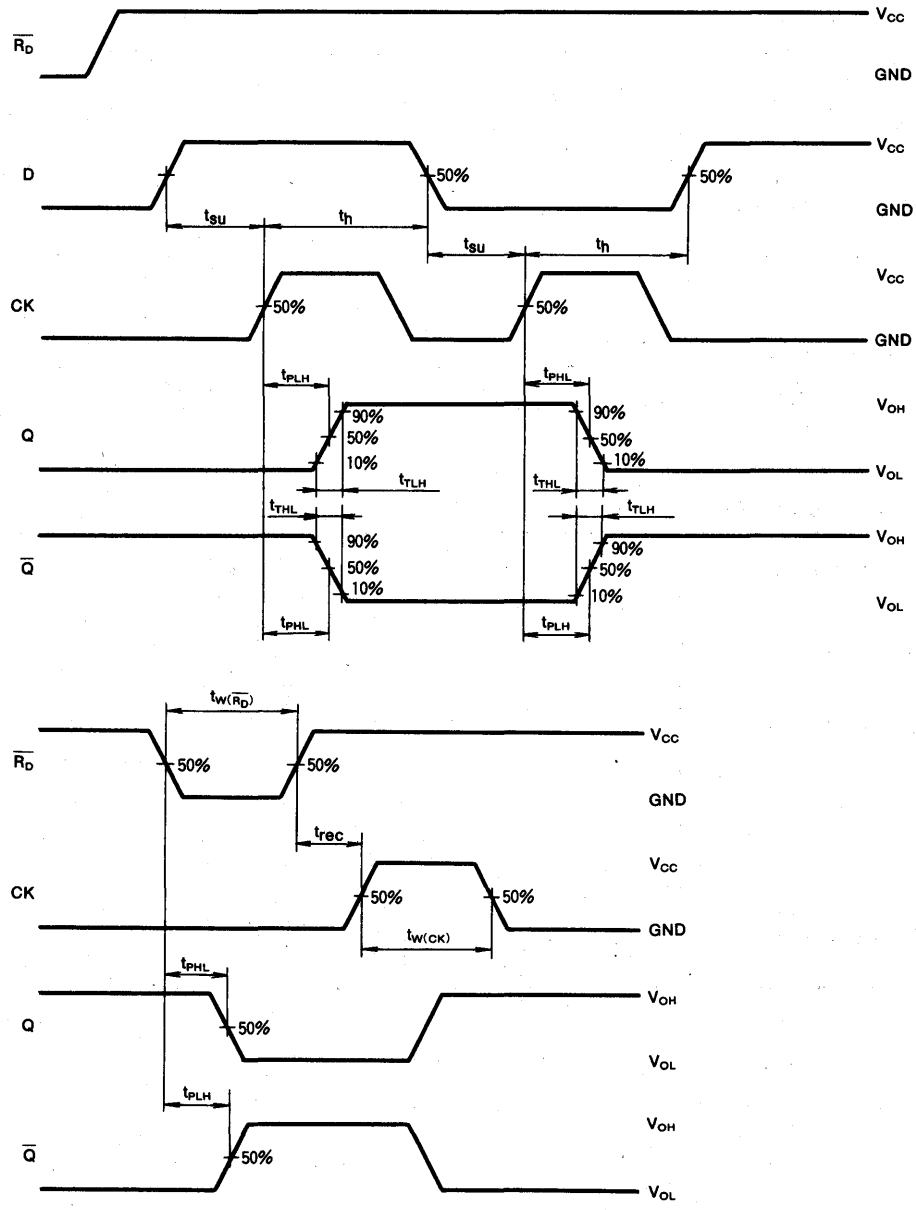
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{W(CK)}$	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{W(\overline{R_D})}$	Direct reset pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	D hold time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		
t_{rec}	$\overline{R_D}$ recovery time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC190P/FP/DP

PRESETTABLE BCD UP/DOWN COUNTER

DESCRIPTION

The M74HC190 is a semiconductor integrated circuit consisting of a presettable synchronous decimal up/down counter with up/down control input.

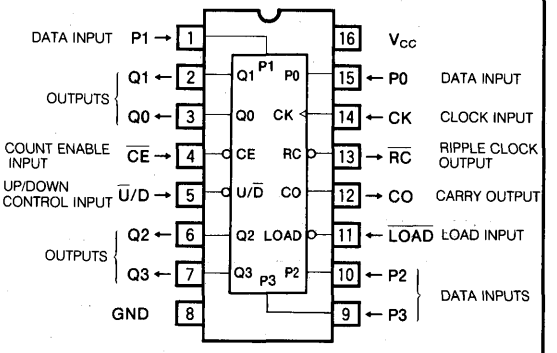
FEATURES

- Up/down switching by up/down control input
- High-speed: (clock frequency) 45MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC190 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS190.

When count enable input $\overline{CE}$ is low and load input $\overline{LOAD}$ is high, and count pulses are applied to clock input CK, the number of count pulses is output at Q0 through Q3 in BCD code in sync with count pulses. The count is incremented when up/down control input $\overline{U}$/D is low, and decremented when $\overline{U}$/D is high. The count is enabled when CK changes from low to high.

The preset function operates irrespective of the count pulse. When data is supplied to data inputs P0 through P3 and load input $\overline{LOAD}$ is low, the signal at P0 through P3 is output at Q0 through Q3 and presets the counter, irrespective of other inputs. When numbers greater than ten are preseted, the counter operates in accordance with the state transition diagram.

The carry output CO becomes high only when 9 appears at Q0 through Q3 during count up and when 0 appears during count down. The ripple clock output $\overline{RC}$ becomes low only when $\overline{CE}$ and CK are both low and when 9 appears at Q0 through Q3 during count up and when 0 appears during count down. $\overline{CE}$, CO and $\overline{RC}$ are used for a cascade connection.

$\overline{CE}$ can be changed from high to low irrespective of CK, but can be changed from low to high only when CK is high. $\overline{U}$/D should be changed only when CK is high.

FUNCTION TABLE (Note 1)

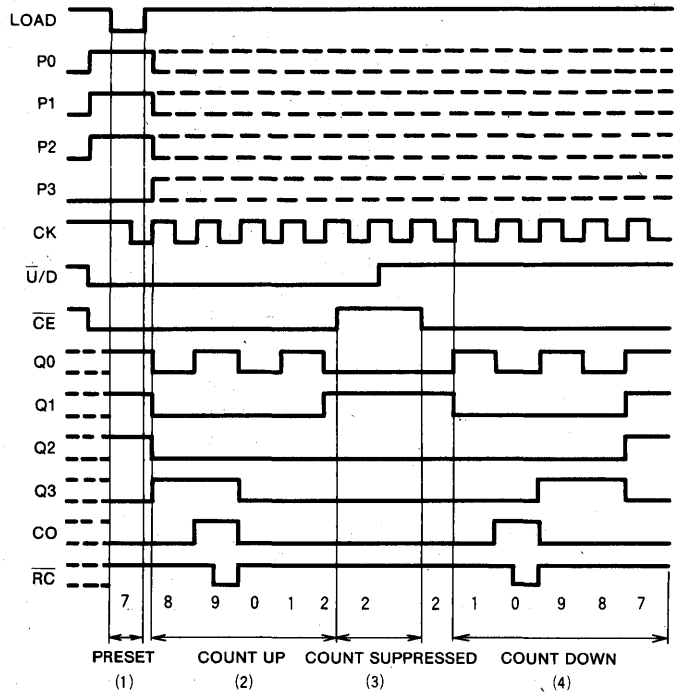
Inputs				Outputs			
$\overline{LOAD}$	$\overline{CE}$	$\overline{U}$/D	CK	Q0	Q1	Q2	Q3
L	X	X	X	P0	P1	P2	P3
H	L	L	↑	Count up			
H	L	H	↑	Count down			
H	H	X	X	Count suppressed			

Note 1 : ↑ : Change from low to high
X : Irrelevant

Inputs			Output
$\overline{CE}$	$CO_{(1)}$	CK	$\overline{RC}$
L	H	L	L
L	H	H	H
H	X	X	H
X	L	X	H

(1) Output CO is generated by the following logic equation.
$CO=\underline{Q0} \cdot \underline{Q3}(\underline{U/D})$ ····· Count up
$CO=\overline{Q0} \cdot \overline{Q1} \cdot \overline{Q2} \cdot \overline{Q3} \cdot (\overline{U}/D)$ ····· Count down

TIMING DIAGRAM



The contents of timing diagram

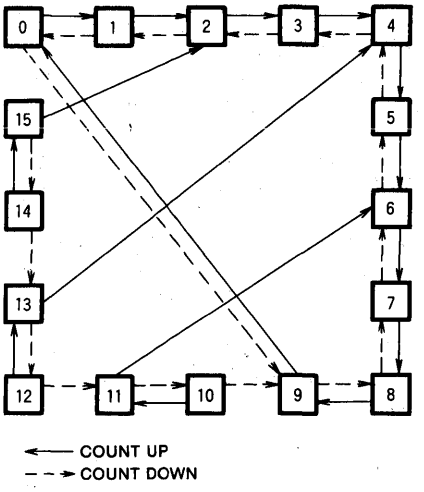
(1) Preset to 7

(2) Count up 8, 9, 0, 1, 2

(3) Count suppressed

(4) Count down 1, 0, 9, 8, 7

STATE TRANSITION DIAGRAM



PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC191P/FP/DP

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

DESCRIPTION

The M74HC191 is a semiconductor integrated circuit consisting of a presettable synchronous 4-bit binary (hexadecimal) counter with up/down control input.

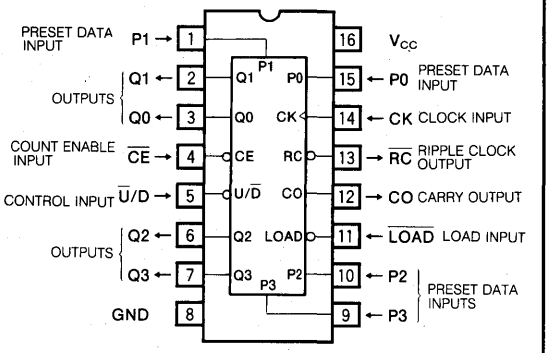
FEATURES

- Up/down switching by up/down control input
- Enable input and ripple clock and carry outputs for cascade connection
- Count frequency 40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC191 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS191.

When count enable input $\overline{CE}$ is low and load input $\overline{LOAD}$ is high, and count pulses are applied to clock input CK, the number of count pulses is output at Q0 throgh Q3 in 4-bit binary code in sync with count pulses. The count is incremented when up/down control input $\overline{U}$/D is low, and decremented when $\overline{U}$/D is high. The count is enabled when CK changes from low to high.

The preset function operates irrespective of the count pulse. When data is supplied to data inputs P0 through P3 and load input $\overline{LOAD}$ is set low, the signal at P0 through P3 is output at Q0 through Q3 irrespective of other inputs, and presets the counter.

The carry output CO will become high only when 15_2 appears at Q0 though Q3 during count up and when 0_2 appears duruing count down. The ripple clock output $\overline{RC}$ will becomes low only when $\overline{CE}$ and CK are both low and when 15_2 appears at Q0 through Q3 during count up and when 0_2 appears during count down. $\overline{CE}$, CO and $\overline{RC}$ are used for a cascade connection.

$\overline{CE}$ can be changed from high to low irrespective of CK, but can be changed from low to high only when CK is high. $\overline{U}$/D should be changed only when CK is high.

FUNCTION TABLE (Note 1)

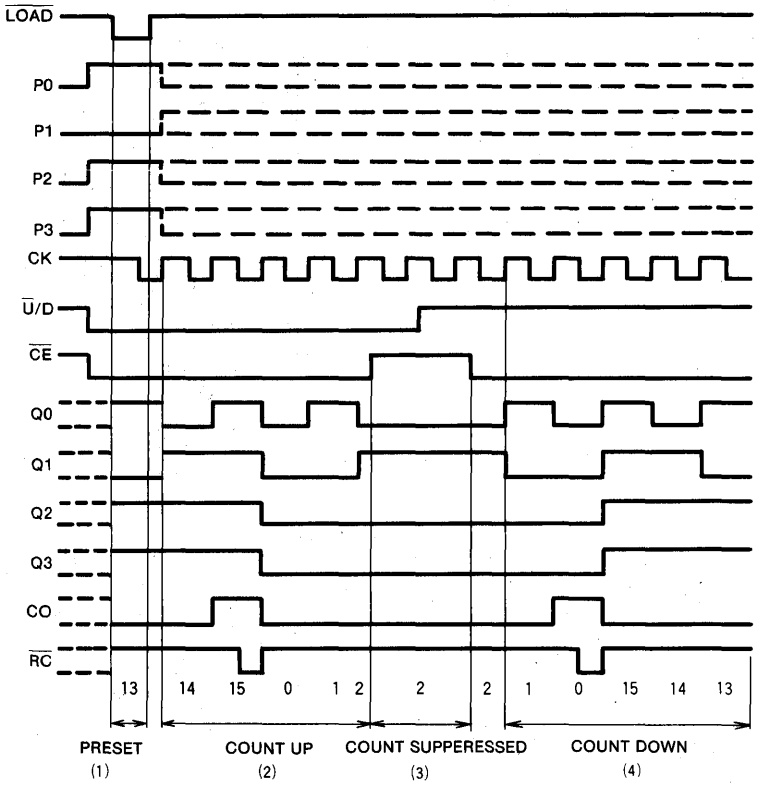
Inputs				Outputs			
$\overline{LOAD}$	$\overline{CE}$	$\overline{U}$/D	CK	Q0	Q1	Q2	Q3
L	X	X	X	P0	P1	P2	P3
H	L	L	↑	Count up			
H	L	H	↑	Count down			
H	H	X	X	Count suppressed			

Note 1 : ↑ : Change from low to high
X : Irrelevant

Inputs			Output
$\overline{CE}$	$CO_{(1)}$	CK	$\overline{RC}$
L	H	L	L
L	H	H	H
H	X	X	H
X	L	X	H

(1) Output CO is generated by the following logic equation.
$CO = \overline{Q0} \cdot \overline{Q1} \cdot \overline{Q2} \cdot \overline{Q3} \cdot (\overline{U}/D)$ ..... Count up
$CO = \overline{Q0} \cdot \overline{Q1} \cdot \overline{Q2} \cdot \overline{Q3} \cdot (\overline{U}/D)$ ..... Count down

TIMING DIAGRAM



The contents of timing diagram
(1) Preset to 13
(2) Count up 14, 15, 0, 1, 2
(3) Count suppressed
(4) Count down 1, 0, 15, 14, 13

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC192P/FP/DP

PRESETTABLE BCD UP/DOWN COUNTER WITH RESET

DESCRIPTION

The M74HC192 is a semiconductor integrated circuit consisting of a synchronous decimal up/down counter with reset and preset inputs.

FEATURES

- High-speed: clock frequency 30MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC192 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS192.

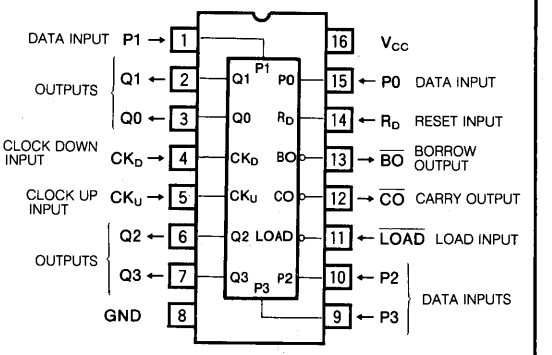
The count input consists of independent clock up input CK_U and clock down input CK_D. When load input $\overline{LOAD}$ and CK_D are both high for count up, count pulses are applied to CK_U, and when $\overline{LOAD}$ and CK_U are both high for count down, count pulses are applied to CK_D, and then the number of count pulses is output at Q0 through Q3 in BCD code in sync with the count pulses. The counter is enabled when CK_U or CK_D changes from low to high.

The preset function operates irrespective of the count pulse. When data is pupplied to preset inputs P0 through P3 and load input $\overline{LOAD}$ is set low, the signal at P0 through P3 is output at Q0 through Q3 and presets the counter, irrespective of CK_U and CK_D. When the number greater than ten is preset, the counter operates in accordance with the state transition table.

When direct reset input R_D is high, the reset function sets Q1 through Q3 low, irrespective of other inputs.

The carry output $\overline{CO}$ will become low only when 9 appears at Q0 through Q3 and CK_U is low during count up. The borrow output $\overline{BO}$ will become low only when 0 appears at Q0 through Q3 and CK_D is low. $\overline{CO}$ and $\overline{BO}$ are connected to CK_U and CK_D in the next state for a cascade connection. (See application examples)

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTION TABLE (Note 1)

Inputs				Outputs					
R_D	$\overline{LOAD}$	CK_U	CK_D	Q0	Q1	Q2	Q3	$\overline{CO}$	$\overline{BO}$
H	X	X	X	L	L	L	L	H	H*
L	L	X	X	P0	P1	P2	P3	H*	H*
L	H	X	X	Count suppressed				H*	H*
L	H	↑	H	Count up				H*	H*
L	H	H	↑	Count down				H*	H*

Note 1 : ↑ : Change from low to high

* : Normally set high, but becomes low under the following condition.

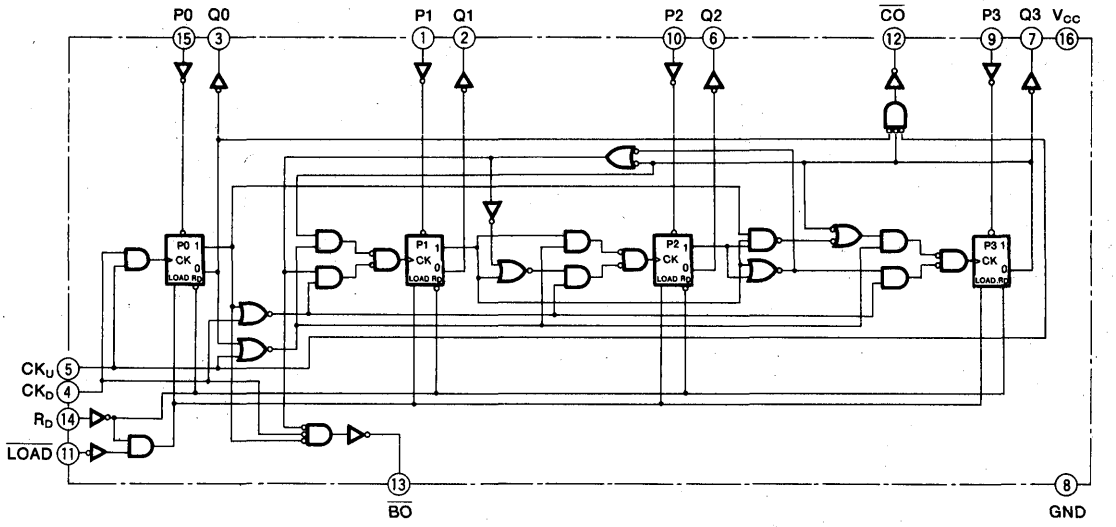
$\overline{CO} = \overline{Q0 \cdot Q3 \cdot CK_U}$ ..... Count up

$\overline{BO} = \overline{Q0 \cdot \overline{Q1} \cdot \overline{Q2} \cdot \overline{Q3} \cdot CK_D}$ ..... Count down

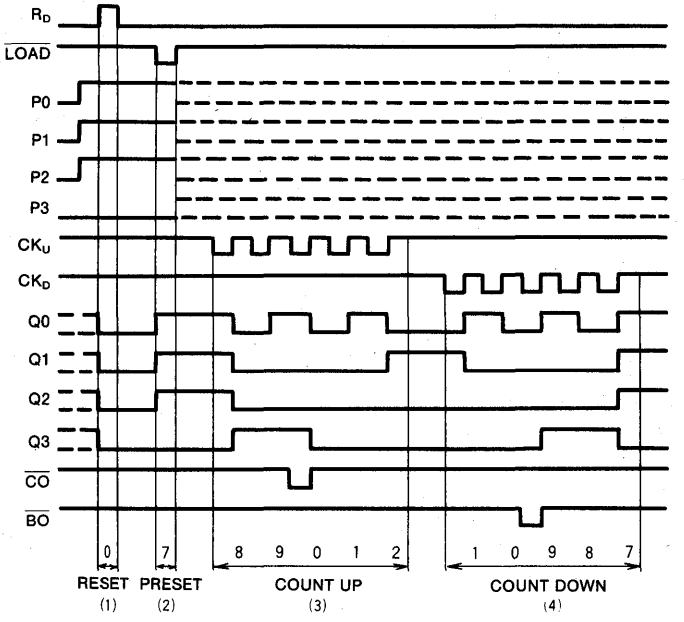
X : Irrelevant

PRESETTABLE BCD UP/DOWN COUNTER WITH RESET

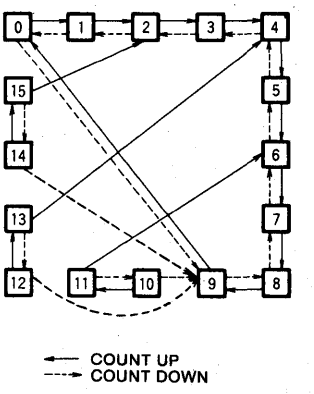
LOGIC DIAGRAM



TIMING DIAGRAM



STATE TRANSITION DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC192FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC192DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	high-level output voltage	V_I = V_{IH}, V_{IL} / I_{OH} = −20μA	2.0	1.9			1.9		V
		I_{OH} = −20μA	4.5	4.4			4.4		
		I_{OH} = −20μA	6.0	5.9			5.9		
		I_{OH} = −4.0mA	4.5	4.18			4.13		
		I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL} / I_{OL} = 20μA	2.0			0.1		0.1	V
		I_{OL} = 20μA	4.5			0.1		0.1	
		I_{OL} = 20μA	6.0			0.1		0.1	
		I_{OL} = 4.0mA	4.5			0.26		0.33	
		I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	20			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_U – $\overline{CO}$)				26	ns
t_{PHL}					24	ns
t_{PLH}	High-level to low-level output propagation time (CK_D – $\overline{BO}$)				24	ns
t_{PHL}					24	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_U, CK_D – Q0, Q1, Q2, Q3)				40	ns
t_{PHL}					52	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LOAD}$ – Q0, Q1, Q2, Q3)				42	ns
t_{PHL}					55	ns
t_{PHL}	High-level to low-level output propagation time (R_D – Q0, Q1, Q2, Q3)				47	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

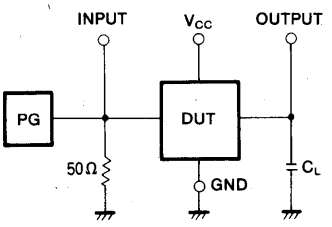
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	3			2.5		MHz
			4.5	18			14		
			6.0	20			16		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_U – $\overline{CO}$)		2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
t_{PHL}			2.0			130		163	ns
			4.5			26		33	
			6.0			22		28	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_D – $\overline{BO}$)		2.0			130		163	ns
			4.5			26		33	
			6.0			22		28	
t_{PHL}			2.0			130		163	ns
			4.5			26		33	
			6.0			22		28	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_U, CK_D – Q0, Q1, Q2, Q3)		2.0			215		269	ns
			4.5			43		54	
			6.0			37		46	
t_{PHL}			2.0			275		344	ns
			4.5			55		69	
			6.0			47		59	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LOAD}$ – Q0, Q1, Q2, Q3)		2.0			230		280	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			290		363	ns
			4.5			58		73	
			6.0			49		61	
t_{PHL}	High-level to low-level output propagation time (R_D – Q0, Q1, Q2, Q3)		2.0			265		331	ns
			4.5			53		66	
			6.0			45		56	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

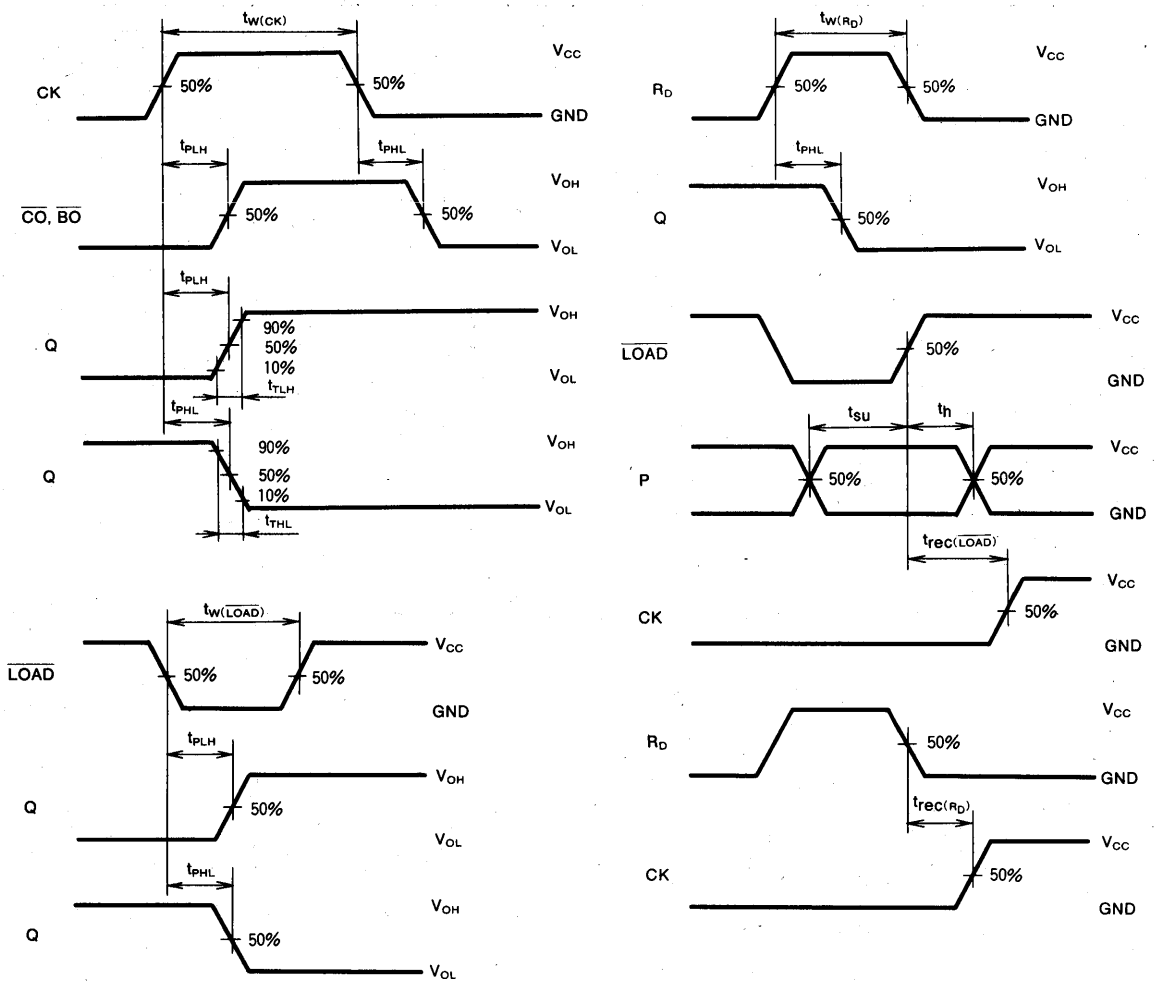
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{w(CK)}$	Clock pulse width		2.0	110			138		ns
			4.5	22			28		
			6.0	19			24		
$t_{w(\overline{LOAD})}$	$\overline{LOAD}$ pulse width		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
$t_{w(R_D)}$	Reset pulse width		2.0	260			325		ns
			4.5	52			65		
			6.0	45			56		
t_{su}	P setup time with respect to $\overline{LOAD}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			22		
t_h	P hold time with respect to $\overline{LOAD}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{rec(\overline{LOAD})}$	$\overline{LOAD}$ recovery time with respect to CK		2.0						ns
			4.5						
			6.0						
$t_{rec(R_D)}$	R_D recovery time with respect to CK		2.0	10			10		ns
			4.5	10			10		
			6.0	10			10		

Note 4 : Test Circuit



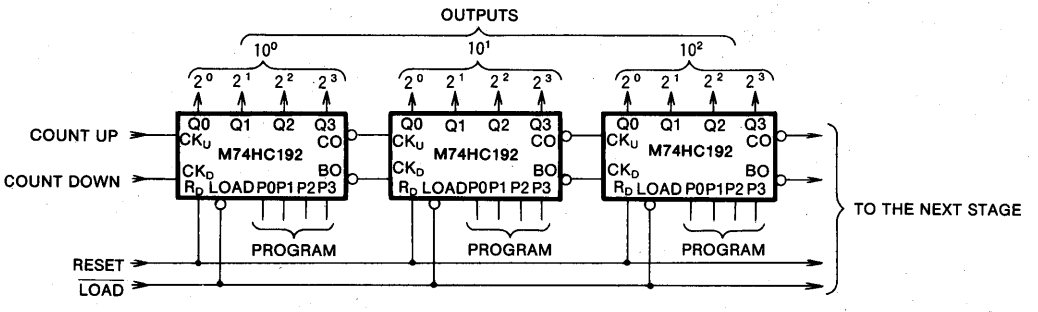
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



APPLICATION EXAMPLE

CONFIGURATION OF AN ASYNCHRONOUS BASE 10^n COUNTER



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC193P/FP/DP

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER WITH RESET

DESCRIPTION

The M74HC193 is a semiconductor integrated circuit consisting of a synchronous hexadecimal (4-bit binary) up/down counter with reset and preset inputs.

FEATURES

- High-speed: clock frequency 30MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC193 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS193.

The count input consists of independent clock up input CK_U and clock down input CK_D. When load input $\overline{LOAD}$ and CK_D are both high for count up, count pulses are applied to CK_U, and when $\overline{LOAD}$ and CK_U are both high for count down, count pulses are applied to CK_D, and then the number of count pulses is output at Q0 through Q3 in 4-bit pure binary code in sync with the count pulses. The counter is enabled when CK_U or CK_D changes from low to high.

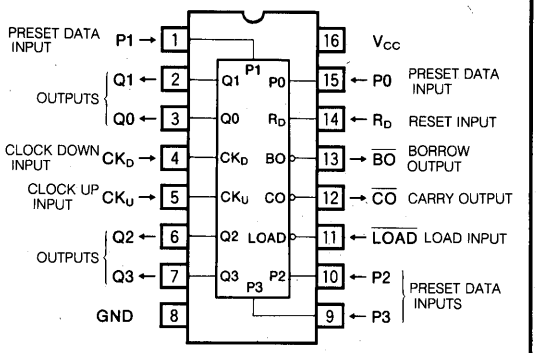
The preset function operates irrespective of the count pulse. When data is supplied to preset inputs P0 through P3 and load input $\overline{LOAD}$ is set low, the signal at P0 through P3 is output at Q0 through Q3 and presets the counter, irrespective of CK_U and CK_D.

The reset function sets Q1 through Q3 low, irrespective other inputs when reset input R_D is high.

The carry output $\overline{CO}$ will become low only when 15 appears at Q0 through Q3 and CK_U is low during count up. The borrow output $\overline{BO}$ will become low only when 0 appears at Q0 through Q3 and CK_D is low. $\overline{CO}$ and $\overline{BO}$ are connected to CK_U and CK_D in the next stage for a cascade connection.

(See application examples)

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTION TABLE (Note 1)

Inputs				Outputs					
R_D	$\overline{LOAD}$	CK_U	CK_D	Q0	Q1	Q2	Q3	$\overline{CO}$	$\overline{BO}$
H	X	X	X	L	L	L	L	H	H*
L	L	X	X	P0	P1	P2	P3	H*	H*
L	H	X	X	Count suppressed				H*	H*
L	H	↑	H	Count up				H*	H*
L	H	H	↑	Count down				H*	H*

Note 1 : ↑ : Change from low to high

* : Normally set high, but becomes low under the following condition.

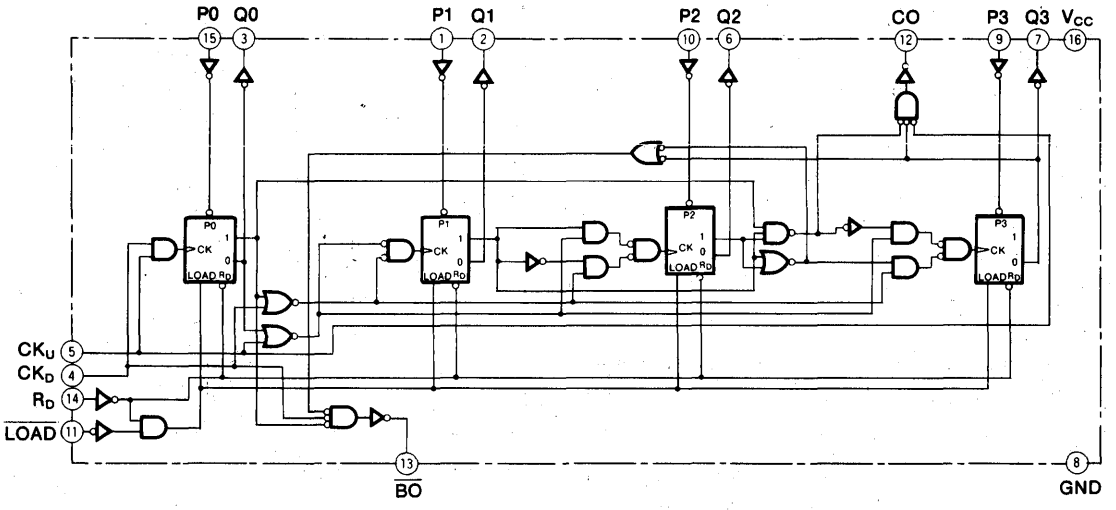
$\overline{CO}=\underline{Q0 \cdot Q1 \cdot Q2 \cdot Q3 \cdot \overline{CK_U}}$···Count up

$\overline{BO}=\underline{\overline{Q1} \cdot \overline{Q1} \cdot \overline{Q2} \cdot \overline{Q3} \cdot \overline{CK_D}}$···Count down

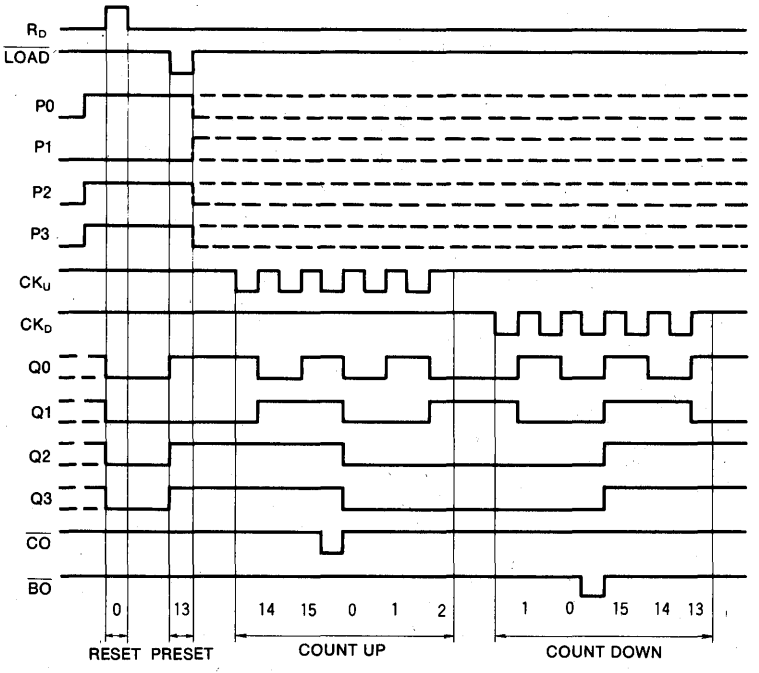
X : Irrelevant

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER WITH RESET

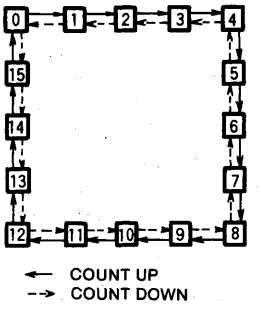
LOGIC DIAGRAM



TIMING DIAGRAM



STATE TRANSITION DIAGRAM



MITSUBISHI ELECTRIC

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER WITH RESET

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage	−0.5∼V_{CC}+0.5	V	
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC193FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC193DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Typ	Max	−40∼+85℃ Min	Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER WITH RESET

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	20			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($CK_U - \overline{CO}$)				26	ns
t_{PHL}					24	ns
t_{PLH}	High-level to low-level output propagation time ($CK_D - \overline{BO}$)				24	ns
t_{PHL}					24	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_U, CK_D – Q0, Q1, Q2, Q3)				40	ns
t_{PHL}					52	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LOAD}$ – Q0, Q1, Q2, Q3)				42	ns
t_{PHL}					55	ns
t_{PHL}	High-level to low-level output propagation time (R_D – Q0, Q1, Q2, Q3)				47	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

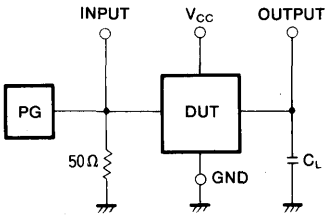
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	3			2.5		MHz
			4.5	18			14		
			6.0	20			16		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($CK_U - \overline{CO}$)		2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
t_{PHL}			2.0			130		163	ns
			4.5			26		33	
			6.0			22		28	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($CK_D - \overline{BO}$)		2.0			130		163	ns
			4.5			26		33	
			6.0			22		28	
t_{PHL}			2.0			130		163	ns
			4.5			26		33	
			6.0			22		28	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_U, CK_D – Q0, Q1, Q2, Q3)		2.0			215		269	ns
			4.5			43		54	
			6.0			37		46	
t_{PHL}			2.0			275		344	ns
			4.5			55		69	
			6.0			47		59	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LOAD}$ – Q0, Q1, Q2, Q3)		2.0			230		280	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			290		363	ns
			4.5			58		73	
			6.0			49		61	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ – Q0, Q1, Q2, Q3)		2.0			265		331	ns
			4.5			53		66	
			6.0			45		56	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

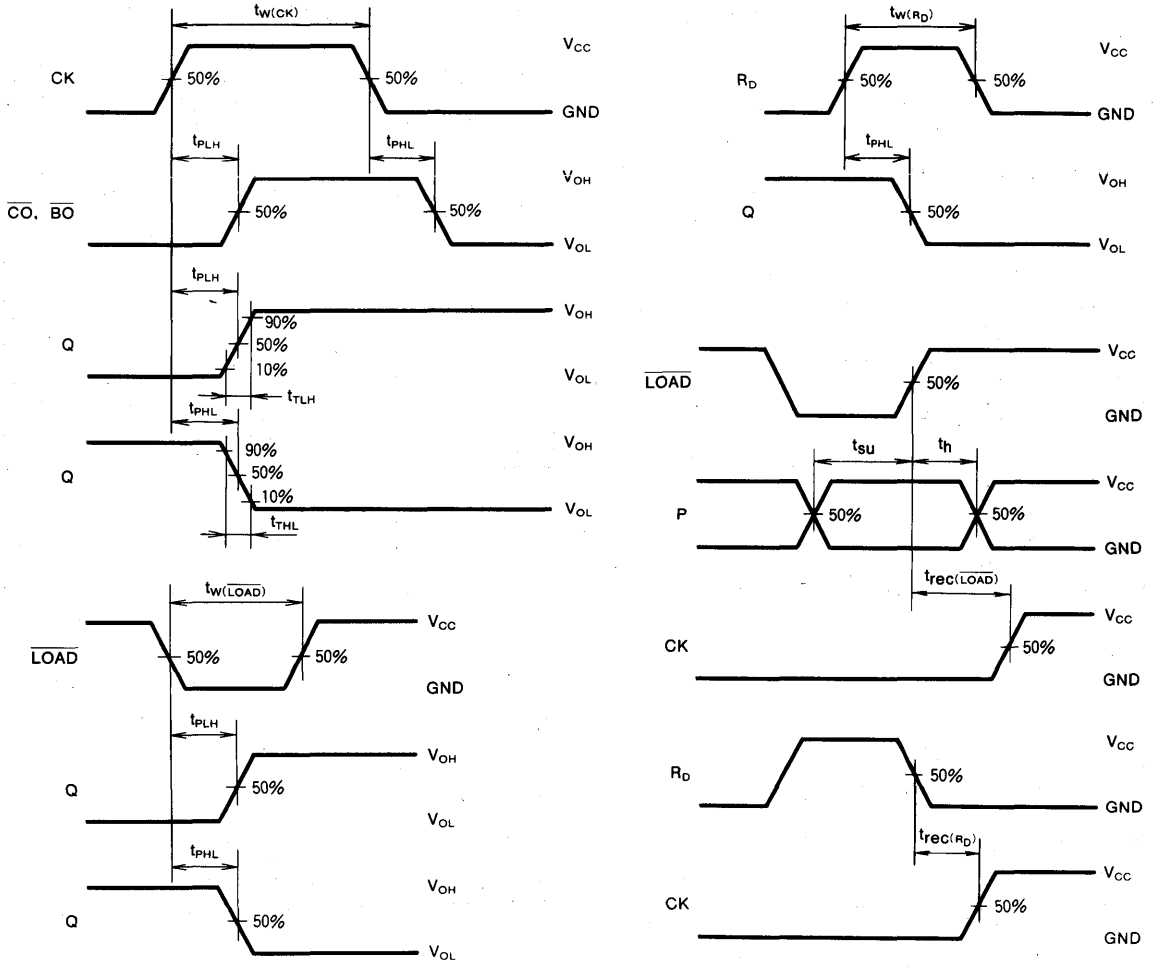
Symbol	Parameter	Test conditions	Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{w(CK)}$	Clock pulse width		2.0	110			138		ns
			4.5	22			28		
			6.0	19			24		
$t_{w(\overline{LOAD})}$	$\overline{LOAD}$ pulse width		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
$t_{w(R_D)}$	Reset pulse width		2.0	130			163		ns
			4.5	26			33		
			6.0	22			28		
t_{su}	P setup time with respect to $\overline{LOAD}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			22		
t_h	P hold time with respect to $\overline{LOAD}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{rec(\overline{LOAD})}$	$\overline{LOAD}$ recovery time with respect to CK		2.0						ns
			4.5						
			6.0						
$t_{rec(R_D)}$	R_D recovery time with respect to CK		2.0	10			10		ns
			4.5	10			10		
			6.0	10			10		

Note 4 : Test Circuit



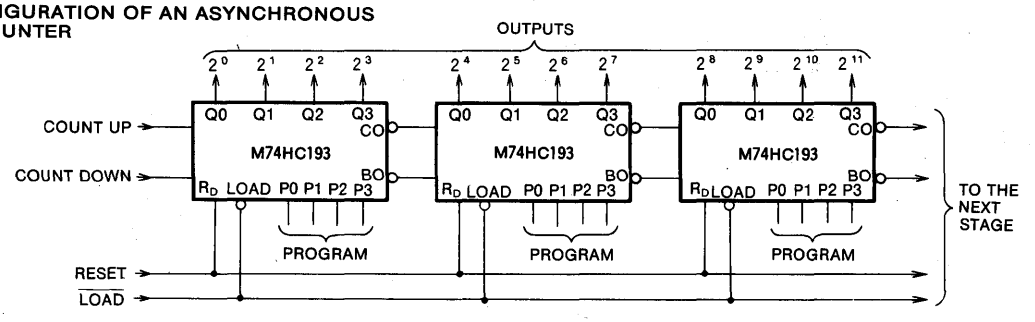
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



APPLICATION EXAMPLE

CONFIGURATION OF AN ASYNCHRONOUS 2^n COUNTER



MITSUBISHI ELECTRIC

M74HC194P/FP/DP

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

DESCRIPTION

The M74HC194 is a semiconductor integrated circuit consisting of a 4-bit bidirectional serial/parallel-input serial/parallel-output shift register with direct reset input.

FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC194 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS194.

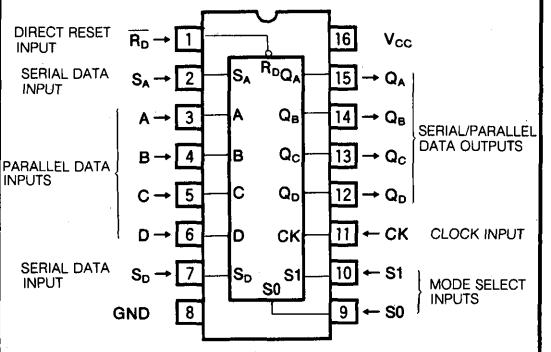
This device is usable as a serial input-serial/parallel output and parallel input-serial/parallel output shift register will the mode select inputs S0 and S1.

When S0 is maintained high and S1 is low, serial data supplied at serial data input S_A will be shifted sequentially to outputs Q_A through Q_D in synchronous with the clock pulse applied at clock input CK. When S0 is maintained low and S1 is high, serial data supplied at serial data input S_D will be shifted sequentially to outputs Q_D through Q_A in synchronous with the clock pulse applied at CK.

When S0 and S1 are both maintained high, parallel data supplied at inputs A through D are simultaneously shifted to Q_A through Q_D by a single clock pulse. When S0 and S1 are both maintained low, none of the flip flops will change state, even if clock pulse is applied at CK.

Left-shift, right-shift and parallel data reading operation take place when the clock pulse changes from low to high. When the direct reset input $\overline{R_D}$ is low, Q_A through Q_D will become low, irrepsective of other inputs.

PIN CONFIGURATION (TOP VIEW)



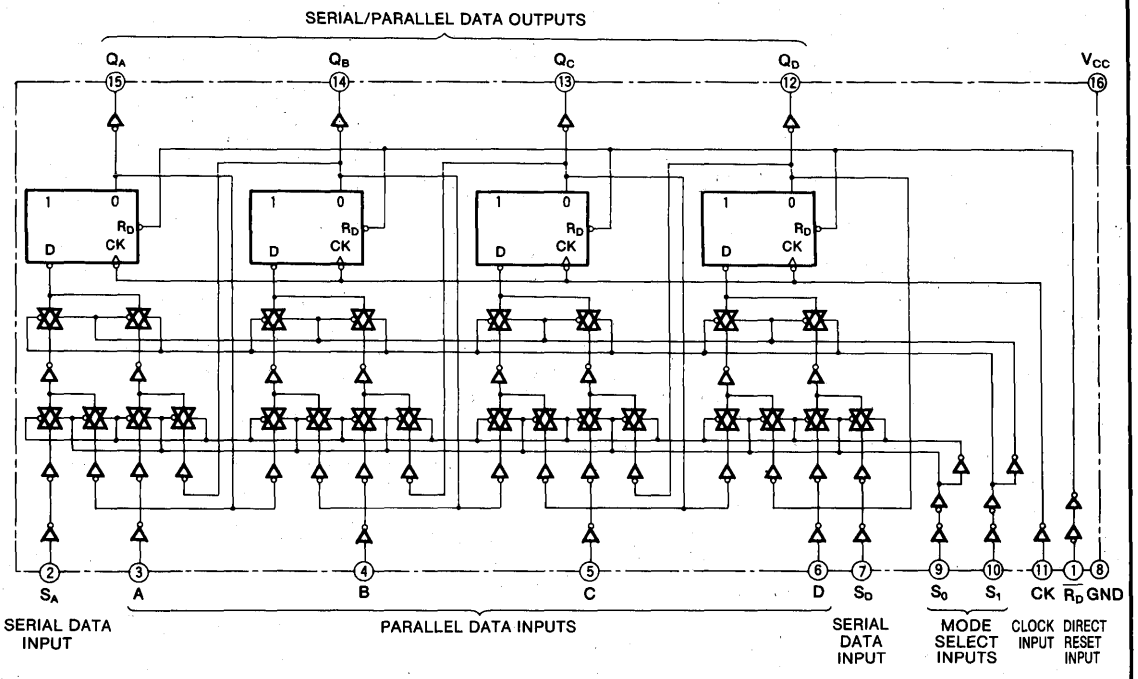
Outline 16P4 16P2N 16P2P

FUNCTION TABLE (Note 1)

Operating mode	Inputs							Outputs			
	$\overline{R_D}$	S0	S1	CK	S_A	S_D	A~D	Q_A	Q_B	Q_C	Q_D
Reset	L	X	X	X	X	X	X	L	L	L	L
Right shift	H	H	L	↑	L	X	X	L	Q_A^0	Q_B^0	Q_C^0
	H	H	L	↑	H	X	X	H	Q_A^0	Q_B^0	Q_C^0
Left-shift	H	L	H	↑	X	L	X	Q_B^0	Q_C^0	Q_D^0	L
	H	L	H	↑	X	H	X	Q_B^0	Q_C^0	Q_D^0	H
Parallel read	H	H	H	↑	X	X	A~D	A	B	C	D
Clock inhibit	H	L	L	X	X	X	X	Q_A^0	Q_B^0	Q_C^0	Q_D^0

Note 1 : ↑ : Change from low to high
X : Irrelevant
Q^0 : Output state of Q before clock input changed

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC194FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC194DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 2～6V, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				24	ns
t_{PHL}	output propagation time (CK − Q)				24	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				25	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

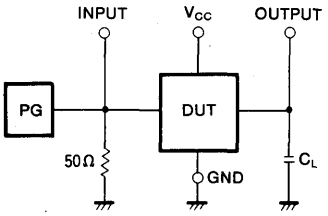
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	6			5		MHz
			4.5	30			24		
			6.0	35			28		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			145		183	ns
			4.5			29		37	
			6.0			25		31	
t_{PHL}			2.0			145		183	ns
			4.5			29		37	
			6.0			25		31	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				127				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

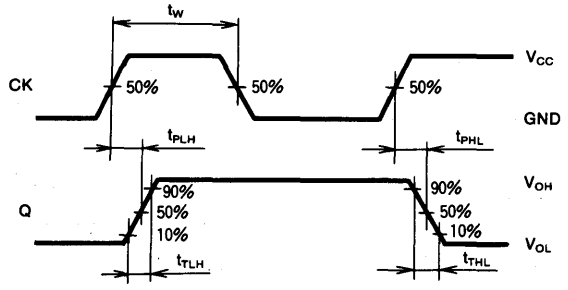
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{R_D}$ Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	A, B, C, D setup time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_{su}	S0, S1, setup time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_{su}	S_A, S_D setup time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	A, B, C, D hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_h	S0, S1 hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_h	S_A, S_D hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{R_D}$ recovery time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

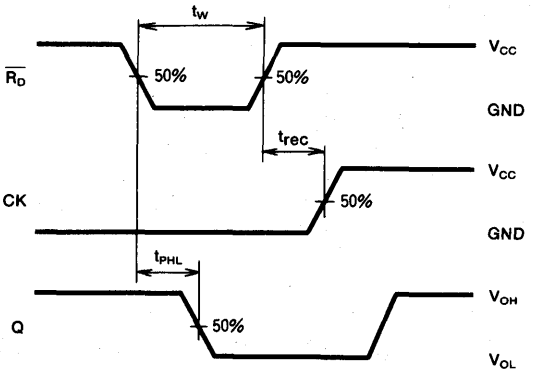
Note 4 : Test Circuit

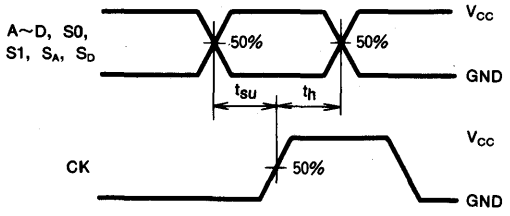


(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







M74HC195P/FP/DP

4-BIT UNIVERSAL SHIFT REGISTER

DESCRIPTION

The M74HC195 is a semiconductor integrated circuit consisting of a 4-bit serial/parallel-input serial/parallel-output shift register with direct reset input.

FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

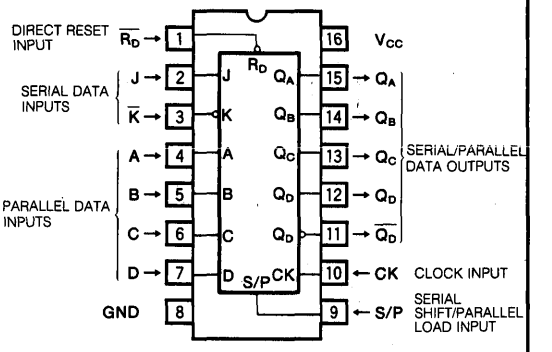
Use of silicon gate technology allows the M74HC195 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS195.

This device is usable as a serial input- serial/parallel output and parallel input- serial/parallel output shift register with the serial shift/parallel load input S/P. When S/P is maintained high, serial data supplied at serial data inputs J and $\overline{K}$ will be shifted sequentially to serial/parallel outputs Q_A through Q_D in synchronous with the clock pulse supplied at clock input CK. The first stage flip flop at J and $\overline{K}$ functions as a J-$\overline{K}$ flip flop. When serial data is supplied from one line, J and $\overline{K}$ are connected and function as a serial input pin. When S/P is maintained low, parallel data supplied at parallel data inputs A through D will be output at Q_A through Q_D by a single clock pules applied at CK. The shift or parallel reading operation take place when CK changes from low to high.

The last-stage flip flop has complementary outputs Q_D and $\overline{Q}_D$.

When direct reset input R_D is low, Q_A through Q_D will become low and $\overline{Q}_D$ will become high, irrespective of other inputs.

PIN CONFIGURATION (TOP VIEW)



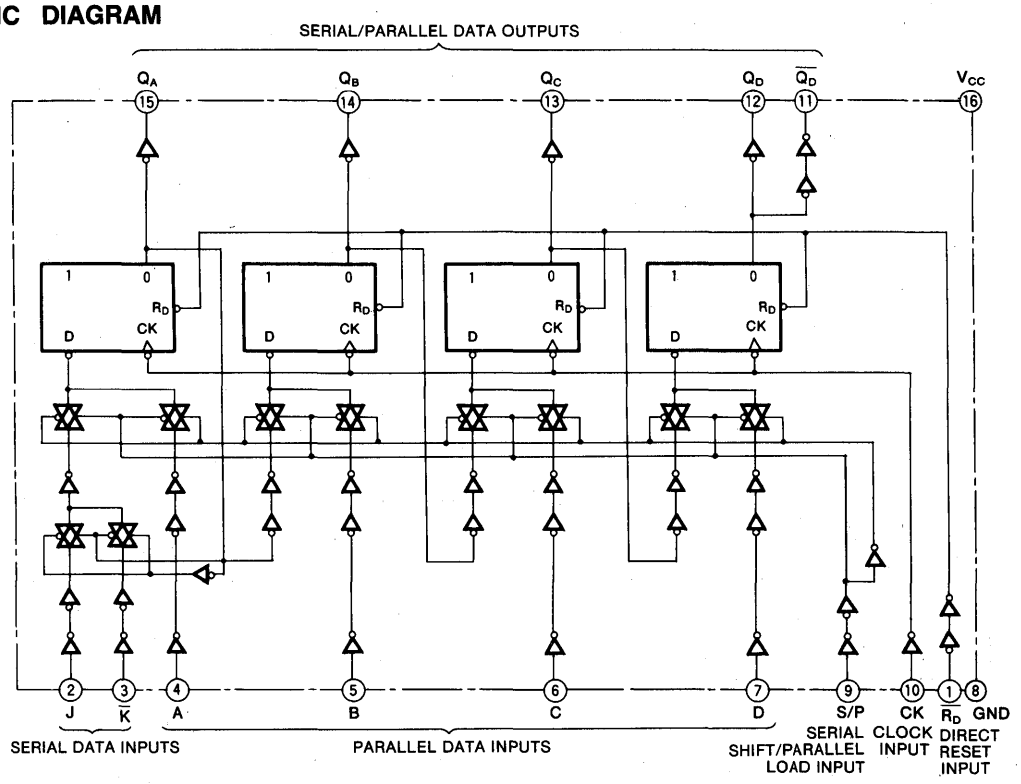
Outline 16P4, 16P2N, 16P2P

FUNCTION TABLE (Note 1)

Operating mode	Inputs						Outputs				
	CK	$\overline{R_D}$	S/P	J	$\overline{K}$	A~D	Q_A	Q_B	Q_C	Q_D	$\overline{Q_D}$
Reset	X	L	X	X	X	X	L	L	L	L	H
Right shift	↑	H	H	H	H	X	H	Q_A^0	Q_B^0	Q_C^0	$\overline{Q_C}^0$
	↑	H	H	L	L	X	L	Q_A^0	Q_B^0	Q_C^0	$\overline{Q_C}^0$
	↑	H	H	H	L	X	$\overline{Q_A}^0$	Q_A^0	Q_B^0	Q_C^0	$\overline{Q_C}^0$
	↑	H	H	L	H	X	Q_A^0	Q_A^0	Q_B^0	Q_C^0	$\overline{Q_C}^0$
Parallel read	↑	H	L	X	X	A~D	A	B	C	D	$\overline{D}$

Note 1 : ↑ : Change frome low to high
X : Irrelevant
Q^0 : Output state of Q before clock input changed
$\overline{Q}^0$: Output state of $\overline{Q}$ before clock input changed

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC195FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC195DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

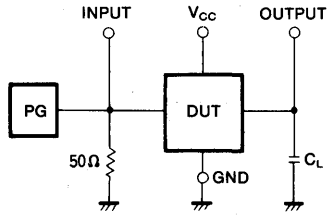
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				24	ns
t_{PHL}	output propagation time (CK − Q)				24	ns
t_{PLH}	Low-level to high-level and high-level to low-level				24	ns
t_{PHL}	output propagation time (CK − $\overline{Q_D}$)				24	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				25	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − $\overline{Q_D}$)				25	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	6			5		MHz
			4.5	30			24		
			6.0	35			28		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			145		183	ns
			4.5			29		37	
			6.0			25		31	
t_{PHL}			2.0			145		183	ns
			4.5			29		37	
			6.0			25		31	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − $\overline{Q_D}$)		2.0			145		183	ns
			4.5			29		37	
			6.0			25		31	
t_{PHL}			2.0			145		183	ns
			4.5			29		37	
			6.0			25		31	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − $\overline{Q_D}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				152				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit

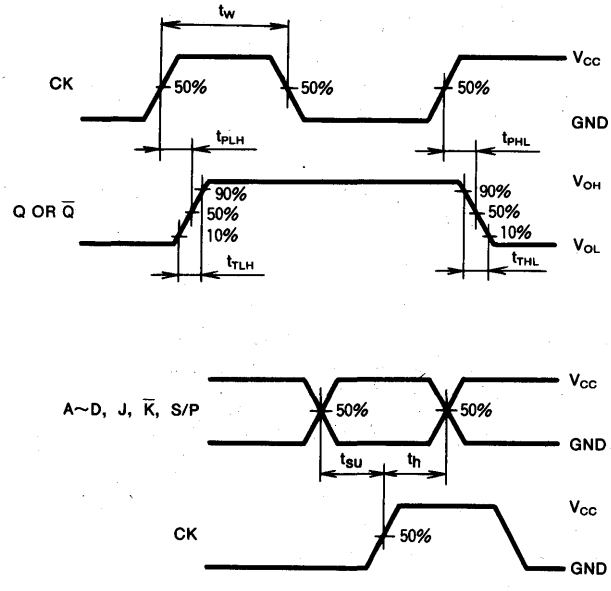


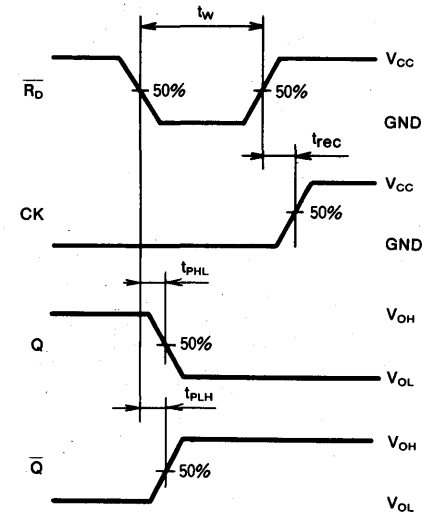
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{R_D}$ clock pulse width	2.0	80			101		ns
		4.5	16			20		
		6.0	14			17		
t_{su}	A, B, C, D setup time with respect to CK	2.0	100			126		ns
		4.5	20			25		
		6.0	17			21		
t_{su}	J, $\overline{K}$ setup time with respect to CK	2.0	100			126		ns
		4.5	20			25		
		6.0	17			21		
t_{su}	S/P setup time with respect to CK	2.0	100			126		ns
		4.5	20			25		
		6.0	17			21		
t_h	A, B, C, D hold time with respect to CK	2.0	0			0		ns
		4.5	0			0		
		6.0	0			0		
t_h	J, $\overline{K}$ hold time with respect to CK	2.0	0			0		ns
		4.5	0			0		
		6.0	0			0		
t_h	S/P hold time with respect to CK	2.0	0			0		ns
		4.5	0			0		
		6.0	0			0		
t_{rec}	$\overline{R_D}$ recovery time with respect to CK	2.0	5			5		ns
		4.5	5			5		
		6.0	5			5		

TIMING DIAGRAM





MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC221P/FP/DP

DUAL MONOSTABLE MULTIVIBRATOR

DESCRIPTION

The M74HC221 is a semiconductor integrated circuit consisting of two monostable multivibrators with direct reset inputs.

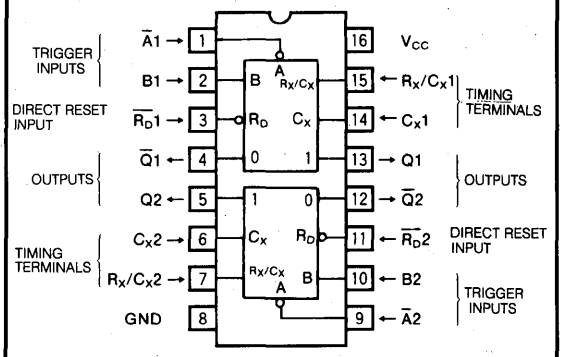
FEATURES

- Direct reset input can interrupt output pulses.
- High-speed: 28ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

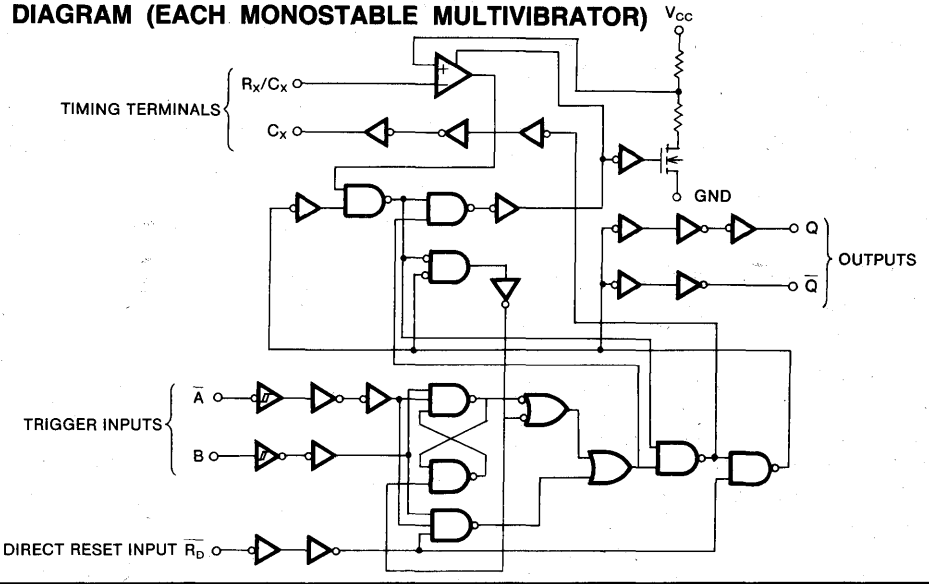
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC221 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS221.

When external resistor R_X and electrostatic capacitor C_X are connected to timing terminals R_X/C_X and C_X as shown in Fig. 1, and trigger pulses are applied at input $\overline{A}$ or B, positive pulses will appear at Q and negative pulses, at $\overline{Q}$. (Fig.2-(a)) The pulse width t_{WQ} is set by R_X and C_X. The trigger is applied when $\overline{A}$ changes from high-level to low-level or when B changes from low-level to high-level.

When direct reset input $\overline{R_D}$ is low, Q will be reset low and $\overline{Q}$ will be reset high, irrespective of the output state, allowing output pulses to be narrower by $\overline{R_D}$. (Fig.2-(b)). When $\overline{R_D}$ changes from low-level to high-level while $\overline{A}$ is low and B is high, the trigger is applied and Q and $\overline{Q}$ change state.

LOGIC DIAGRAM (EACH MONOSTABLE MULTIVIBRATOR)



FUNCTION TABLE (Note 1)

Inputs			Outputs	
$\overline{R_D}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
⎍ : Positive one-shot operation
⎎ : Negative one-shot operation
X : Irrelevant

OPERATION

1. How to use the timing terminals

Resistor R_X and capacitor C_X are connected to timing terminals R_X/C_X and C_X, as shown in Fig. 1. If C_X is polar, the positive lead should be connected to the R_X/C_X side, and the negative lead to the C_X side. A diode is connected to prevent latchup.

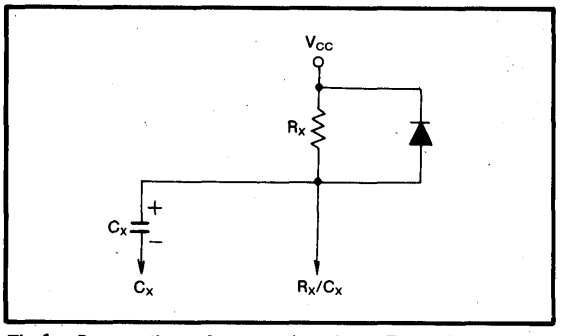


Fig.1 Connection of external resistor R_X and capacitor C_X to timing terminals R_X/C_X and C_X

2. Output pulse width t_{WQ}

The output pulse width t_{WQ} is determined as follows:
when $C_X > 100000pF$, $R_X \geqq 10k\Omega$
$t_{WQ} = 0.46C_X \cdot R_X$ (ns)
C_X is given in pF, and R_X in kΩ.

3. Output pulse width control

The output pulse width is controlled in the following two ways.

3—1 Normal use

Fig.2-(a) is the directions as ordinary monostable multivibrator operation and the output pulse width t_{WQ} can be set by using the formula and figure shown in section 2 above.

3—2 Shortening of the output pulse width with $\overline{R_D}$ signal

As shown in Fig.2-(b), the output pulse which has been generated by the trigger signal can be terminated with the $\overline{R_D}$ signal and it is possible to shorten its width as required.

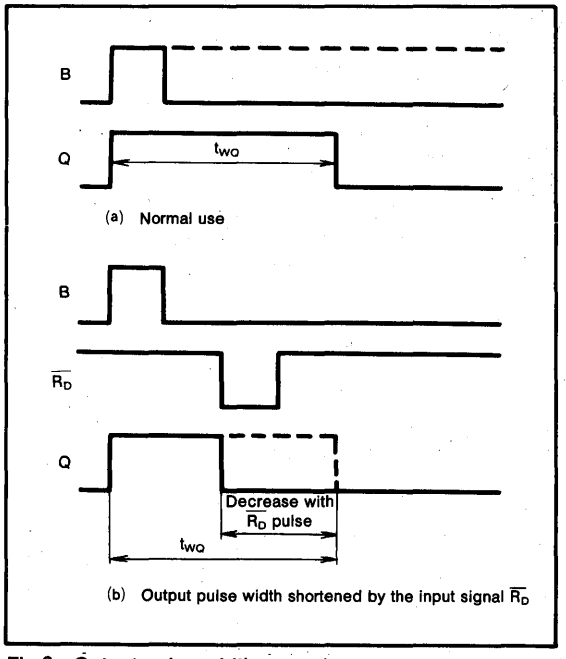


Fig.2 Output pulse width control

4. Precautions for use

4—1 The lead lengths of external resistor R_X and capacitor C_X should be as short as possible (less than 3cm) to minimize stray wiring capacitance and to prevent misoperation due to noise. Care should also be taken to isolate this circuit from noise sources as far as possible.

4—2 Insert a capacitor of 0.01 ~ 0.1μF with good high-frequency characteristics between V_{CC} and GND.

4—3 Output pulses may be generated when power is switched on.

4—4 Capacitor discharge when the power is turned off may cause thermal breakdown or latchup, so a diode should be connected as shown in Fig. 1.

M74HC237P/FP/DP

1-OF-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

DESCRIPTION

The M74HC237 is a semiconductor integrated circuit consisting of a 3-bit binary to 8-line decoder/demultiplexer with address latch.

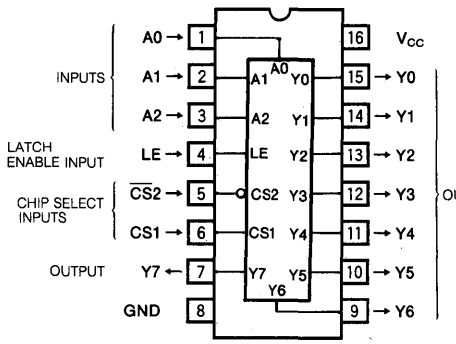
FEATURES

- Built-in address latch
- High-speed: 18ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



16P4
Outline 16P2N
16P2P

FUNCTIONAL DESCRIPTION

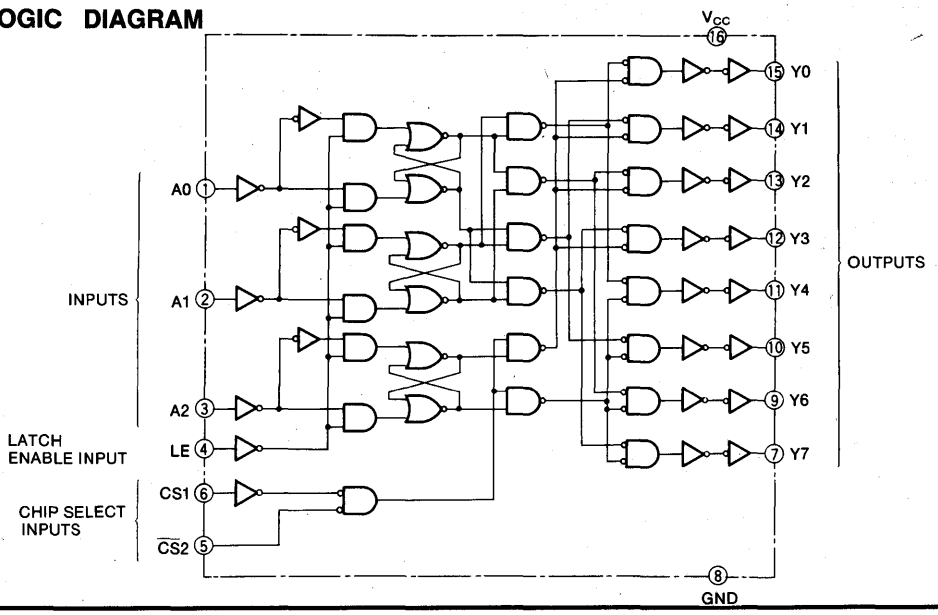
Use of silicon gate technology allows the M74HC237 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS237.

The M74HC237 consists of a 3-bit binary to 8-line decoder/demultiplexer with an address latch to store the signals of inputs A0 through A2. When latch-enable input LE is low, a 3-bit binary code, applied to inputs A0 through A2, goes through the latch and becomes the decoder input signal. In this case, the output Y0 through Y7 corresponding to this value will become high and other outputs will all become low. When LE is high, the A0 through A2 signals existing immediately prior to the high-level setting will be stored in the latch. In this case, those stored contents will not change even if A0 through A2 are changed.

In this case, chip select inputs CS1 and $\overline{CS2}$ should be maintained at high and low, respectively. When CS1 and $\overline{CS2}$ are in conditions other than those given above, all outputs will become low.

When operated as a 1-of-8 demultiplexer, CS1 or $\overline{CS2}$ is used as a data input and A0 through A2 are used as the selecting inputs.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs						Outputs							
LE	CS1	$\overline{CS2}$	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	$Y0^0$	$Y1^0$	$Y2^0$	$Y3^0$	$Y4^0$	$Y5^0$	$Y6^0$	$Y7^0$

Note 1 : X : Irrelevant
Y^0 : Output state Y before LE changed to high

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC237FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC237DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				41	ns
t_{PHL}	output propagation time (A − Y)				32	ns
t_{PLH}	Low-level to high-level and high-level to low-level				35	ns
t_{PHL}	output propagation time ($\overline{CS2}$ − Y)				25	ns
t_{PLH}	Low-level to high-level and high-level to low-level				35	ns
t_{PHL}	output propagation time (CS1 − Y)				27	ns
t_{PLH}	Low-level to high-level and high-level to low-level				44	ns
t_{PHL}	output propagation time (LE − Y)				33	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

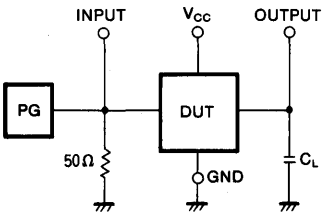
Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)		2.0			235		296	ns
			4.5			47		59	
			6.0			40		50	
t_{PHL}			2.0			185		233	ns
			4.5			37		47	
			6.0			31		40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS2}$ − Y)		2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PHL}			2.0			145		183	ns
			4.5			29		37	
			6.0			25		31	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CS1 − Y)		2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PHL}			2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − Y)		2.0			250		315	ns
			4.5			50		63	
			6.0			43		54	
t_{PHL}			2.0			190		239	ns
			4.5			38		48	
			6.0			32		41	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				105				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

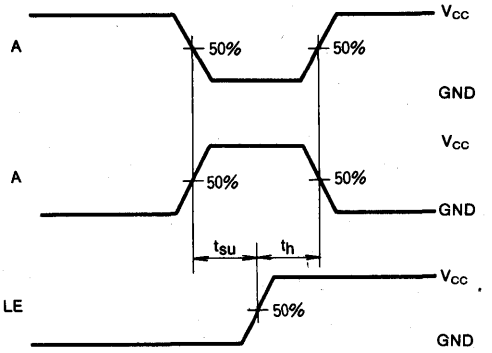
TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Latch enable pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	A setup time with respect to LE		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	A hold time with respect to LE		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		

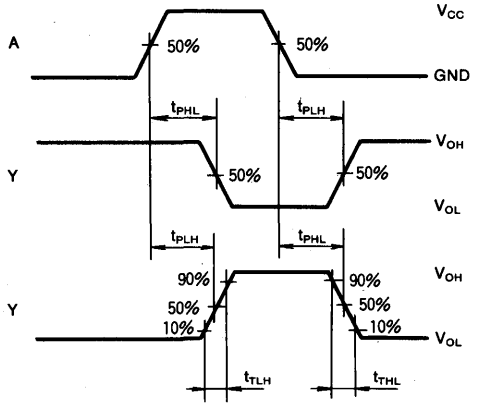
Note 4 : Test Circuit

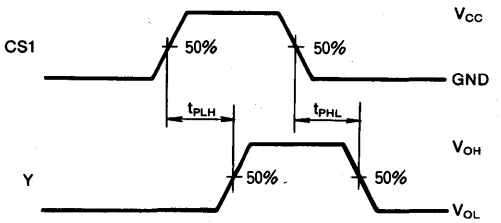


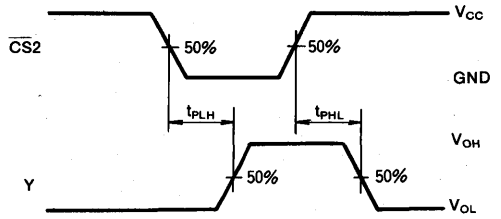
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

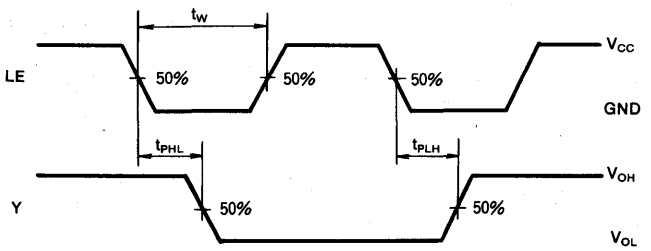


TIMING DIAGRAM









PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC238P/FP/DP

1-OF-8 DECODER/DEMULTIPLEXER

DESCRIPTION

The M74HC238 is a semiconductor integrated circuit consisting of a 3-bit binary-to-octal decoder/demultiplexer with chip select inputs.

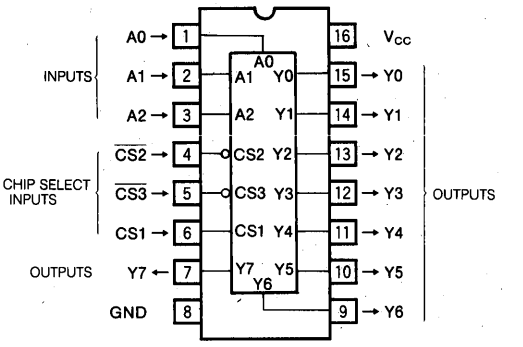
FEATURES

- Three chip select inputs
- Expandable to 24 outputs without external components
- High-speed: 18ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC238 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS238.

When operated as a decoder, a 3-bit binary code are applied to inputs A0, A1 and A2, one of outputs Y0 through Y7 corresponding to this value will become high and the other outputs will all become low.

In this case, chip select input CS1 should be maintained at high while $\overline{CS2}$ and $\overline{CS3}$ should be maintained at low.

When CS1, $\overline{CS2}$ and $\overline{CS3}$ are in conditions other than those given above, all outputs will become low irrespective of A0 through A2.

When operated as a 1-of-8 demultiplexer, CS1, $\overline{CS2}$ or $\overline{CS3}$ is used as data input and A0 through A2 input are used as selecting input.

FUNCTION TABLE (Note 1)

Inputs					Outputs							
CS1	$\overline{CSX}$	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	H	H	L	L	L	H	L	L	L	L
H	L	H	L	L	L	L	L	L	H	L	L	L
H	L	H	L	H	L	L	L	L	L	H	L	L
H	L	H	H	L	L	L	L	L	L	L	H	L
H	L	H	H	H	L	L	L	L	L	L	L	H

Note 1 : $\overline{CSX} = \overline{CS2} + \overline{CS3}$
X : Irrelevant

MITSUBISHI ELECTRIC

M74HC240P/FP/DWP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC240 is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC240 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS240.

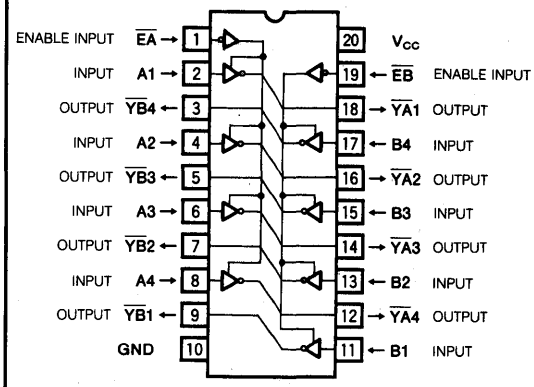
The M74HC240 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{E}$ is low and input A (or B) is low then output $\overline{Y}$ will become high. However, if A (or B) is high then $\overline{Y}$ will become low.

When $\overline{E}$ is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

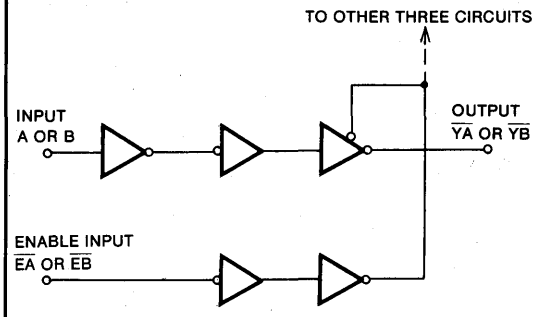
All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$ of the two blocks.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

LOGIC DIAGRAM (EACH BUFFER)



FUNCTION TABLE (Note 1)

Inputs		Output
A, B	$\overline{EA}$, $\overline{EB}$	$\overline{YA}$, $\overline{YB}$
L	L	H
H	L	L
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC240FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC240DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Typ	Max	−40∼+85℃ Min	Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

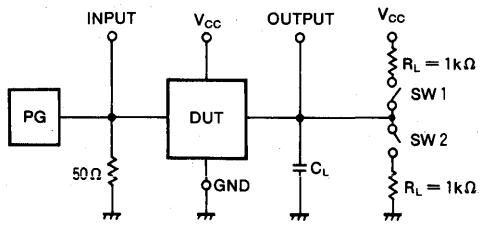
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				18	ns
t_{PHL}	output propagation time (A − $\overline{YA}$, B − $\overline{YB}$)				18	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}	($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)				25	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 4)			28	ns
t_{PZH}	($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)				28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
	high-level to low-level		6.0			10		13	
t_{THL}	output transition time		2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{YA}$, B − $\overline{YB}$)	C_L = 50pF (Note 4)	2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = V_{CC}, $\overline{EB}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				57				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

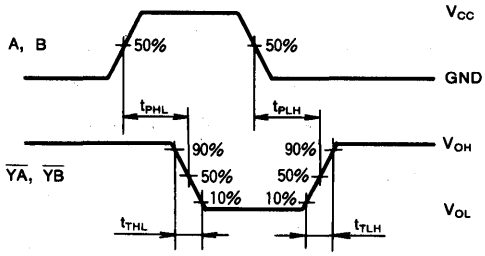
Note 4 : Test Circuit

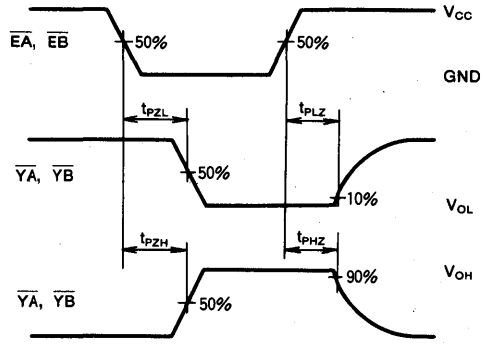


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

M74HC240-1P/FP/DWP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC240-1 is a semiconductor integrated circuit consisting of two blocks of 3-state inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 7ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC240-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS240.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC240-1 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{E}$ is low and input A (or B) is low then output $\overline{Y}$ will become high. However, if A (or B) is high then $\overline{Y}$ will become low.

When $\overline{E}$ is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

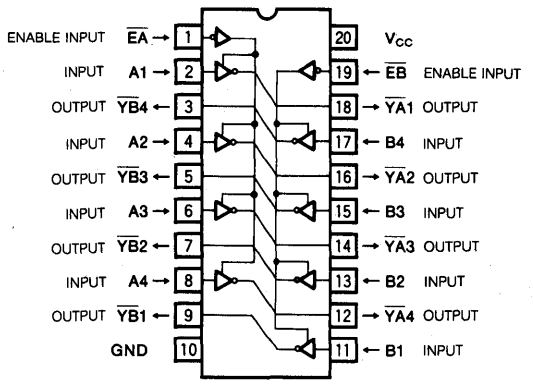
All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$ of the two blocks.

FUNCTION TABLE (Note 1)

Inputs		Output
A, B	$\overline{EA}$, $\overline{EB}$	$\overline{YA}$, $\overline{YB}$
L	L	H
H	L	L
X	H	Z

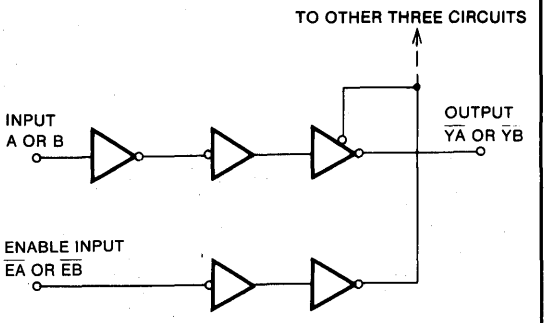
Note 1 : Z : High impedance
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

LOGIC DIAGRAM (EACH BUFFER)



OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC240-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC240-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, I_{OH} = −20μA	2.0	1.9			1.9		V
		V_I = V_{IL}, I_{OH} = −20μA	4.5	4.4			4.4		
		V_I = V_{IL}, I_{OH} = −20μA	6.0	5.9			5.9		
		V_I = V_{IL}, I_{OH} = −24mA	4.5	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	2.0			0.1		0.1	V
		V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	4.5			0.1		0.1	
		V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	6.0			0.1		0.1	
		V_I = V_{IH}, V_{IL}, I_{OL} = 24mA	4.5			0.39		0.5	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}	6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND	6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

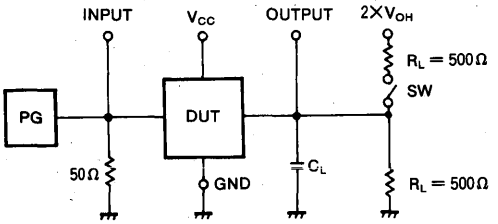
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{YA}$, B − $\overline{YB}$)				14	ns
t_{PHL}					14	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 5 pF (Note 4)			18	ns
t_{PHZ}					18	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 50pF (Note 4)			21	ns
t_{PZH}					21	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A−$\overline{YA}$, B−$\overline{YB}$)		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PHL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHZ}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PZH}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = V_{CC}, $\overline{EB}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)				43				

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

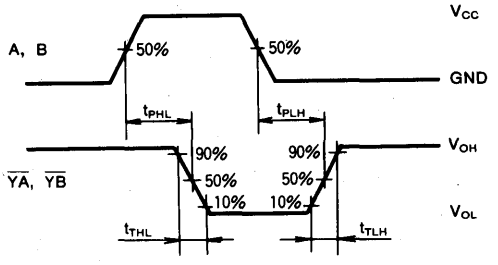
Note 4 : Test Circuit

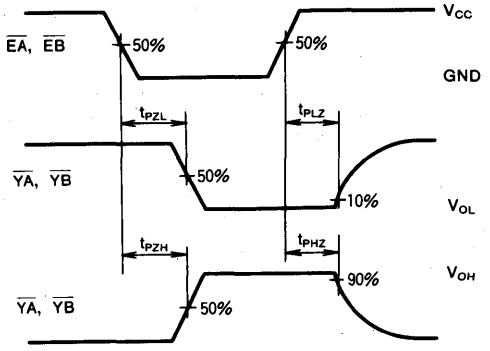


Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 3ns$, $t_f = 3ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HCT240P/FP/DWP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT240 is a semiconductor integrated circuit consisting of two blocks of 3-state inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- TTL level input V_{IL} = 0.8V max V_{IH} = 2.0V min
- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 15 74LSTTL loads
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT240 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS240.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT240 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{E}$ is low and input A (or B) is low then output $\overline{Y}$ will become high. However, if A (or B) is high then $\overline{Y}$ will become low.

When $\overline{E}$ is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

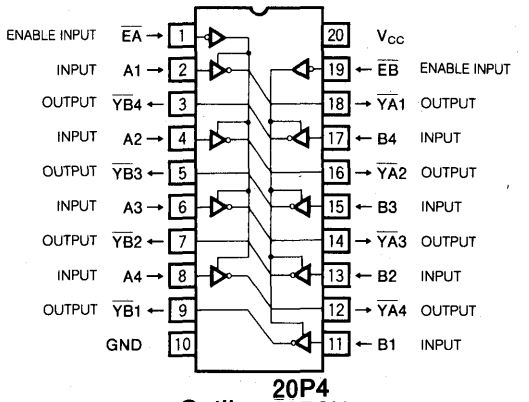
All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$ of the two blocks.

FUNCTION TABLE (Note 1)

Inputs		Output
A, B	$\overline{EA}$, $\overline{EB}$	$\overline{YA}$, $\overline{YB}$
L	L	H
H	L	L
X	H	Z

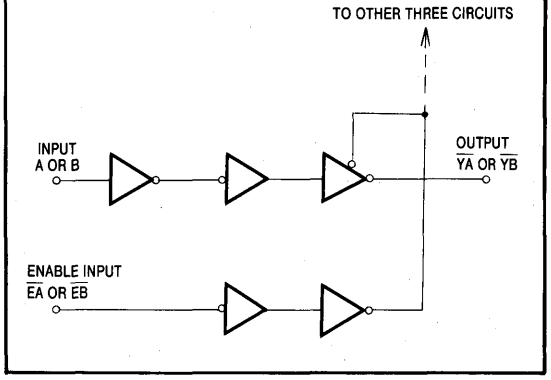
Note 1 : Z : High impedance
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



20P4
Outline 20P2N
20P2V

LOGIC DIAGRAM (EACH BUFFER)



OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC240FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC240DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, |I_O| = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_{CC}−0.1V, V_{CC}−0.1V, |I_O| = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −6.0mA, V_{CC} = 4.5V	4.18			4.13		
			I_{OH} = −7.2mA, V_{CC} = 5.5V	5.18			5.13		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 6.0mA, V_{CC} = 4.5V			0.26		0.33	
			I_{OL} = 7.2mA, V_{CC} = 5.5V			0.26		0.33	
I_{IH}	High-level input current	V_I = 5.5V				0.1		1.0	μA
I_{IL}	High-level input current	V_I = 0V				−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				4.0		40.0	μA
$\triangle I_{CC}$	Maximum quiescent state supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all others are fixed at V_{CC} or GND.

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12	ns
t_{THL}					12	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{YA}$, B − $\overline{YB}$)				23	ns
t_{PHL}					23	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 5 pF (Note 5)			27	ns
t_{PHZ}					27	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 50pF (Note 5)			32	ns
t_{PZH}					32	

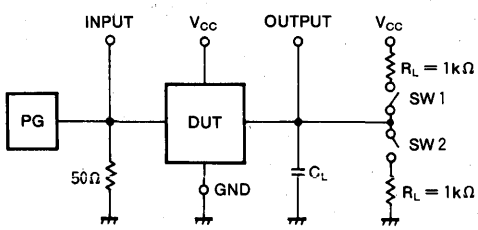
SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40∼+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40∼+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12		15	ns
t_{THL}					12		15	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{YA}$, B − $\overline{YB}$)	C_L = 50pF (Note 5)			23		29	ns
t_{PHL}					23		29	
t_{PLH}		C_L = 150pF (Note 5)			38		48	ns
t_{PHL}					38		48	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 50pF (Note 5)			32		40	ns
t_{PHZ}					32		40	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 50pF (Note 5)			32		40	ns
t_{PZH}					32		40	
t_{PZL}		C_L = 150pF (Note 5)			47		59	
t_{PZH}					47		59	
C_I	Input capacitance				10		10	pF
C_O	Off-sate output capacitance	$\overline{EA}$ = $\overline{EB}$ = V_{CC}			15		15	
C_{PD}	Power dissipation capacitance (Note 4)			42				

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

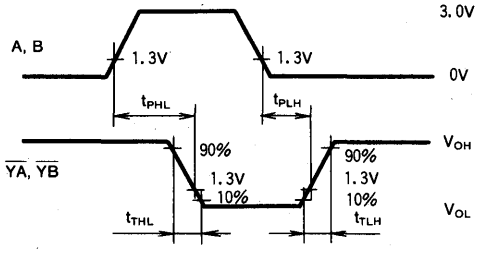
Note 5 : Test Circuit

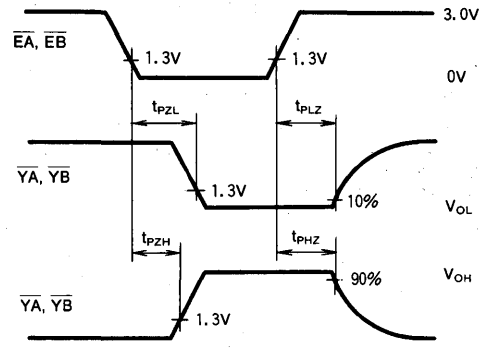


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HCT240-1P/FP/DWP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/ LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT240-1 is a semiconductor integrated circuit consisting of two blocks of 3-state inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- TTL level input V_{IL} = 0.8V max V_{IH} = 2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 9ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40∼+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT240-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS240.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

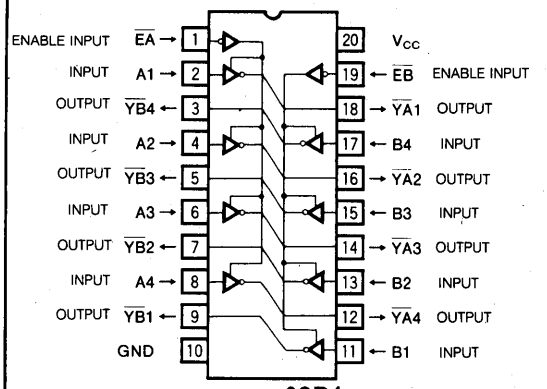
The M74HCT240-1 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{E}$ is low and input A (or B) is low then output $\overline{Y}$ will become high. However, if A (or B) is high then $\overline{Y}$ will become low.

When $\overline{E}$ is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

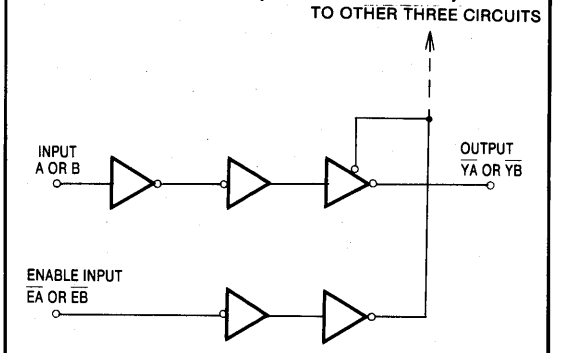
All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$ of the two blocks.

PIN CONFIGURATION (TOP VIEW)



20P4
Outline 20P2N
20P2V

LOGIC DIAGRAM (EACH BUFFER)



FUNCTION TABLE (Note 1)

Inputs		Output
A, B	$\overline{EA}$, $\overline{EB}$	$\overline{YA}$, $\overline{YB}$
L	L	H
H	L	L
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/ LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC240-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC240-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.39		0.5	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

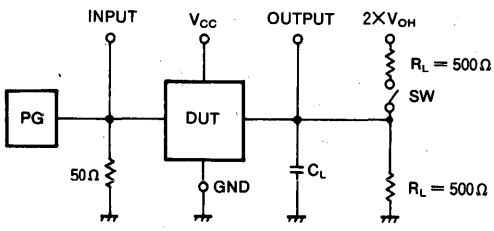
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{YA}$, B − $\overline{YB}$)				14	ns
t_{PHL}					14	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 5 pF (Note 5)			18	ns
t_{PHZ}					18	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 50pF (Note 5)			21	ns
t_{PZH}					21	

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40∼+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40∼+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12		15	ns
t_{THL}					12		15	
t_{PLH}	Low-level to high-level and output propagation time (A − $\overline{YA}$, B − $\overline{YB}$)				15		19	ns
t_{PHL}					15		19	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)				23		29	ns
t_{PHZ}					23		29	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)				23		29	ns
t_{PZH}					23		29	
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = V_{CC}, $\overline{EB}$ = V_{CC}			15		15	
C_{PD}	Power dissipation capacitance (Note 4)							

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

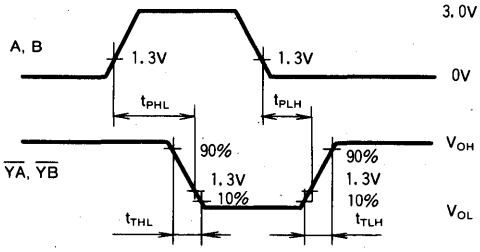
Note 5 : Test Circuit

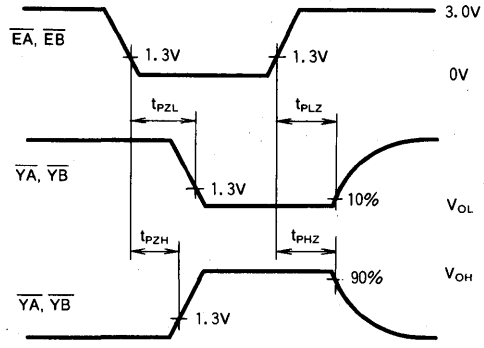


Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 3ns$, $t_f = 3ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC241P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC241 is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

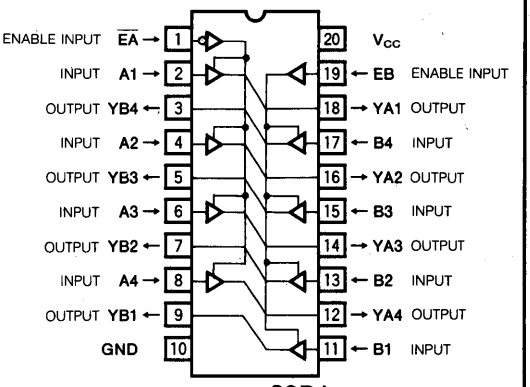
Use of silicon gate technology allows the M74HC241 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS241.

The M74HC241 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{EA}$ is low and input A is low then output YA will become low. However, if A is high then YA will become high. Inverted in the other block, a high enable input EB signal causes operation the same as that just described with input B signal output at YB.

When $\overline{EA}$ is high or EB is low then all Y within the block will become high-impedance state, irrespective of A or B.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4 20P2N 20P2V

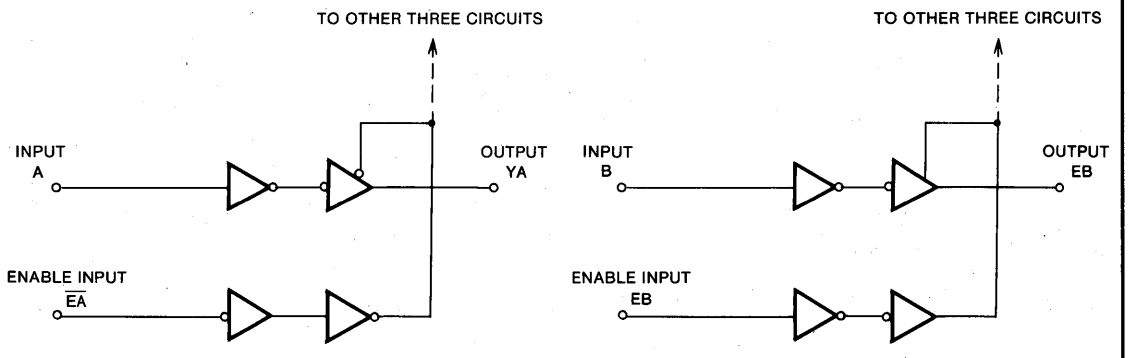
FUNCTION TABLE (Note 1)

Inputs		Output
A	$\overline{EA}$	YA
L	L	L
H	L	H
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

Inputs		Output
B	EB	YB
L	H	L
H	H	H
X	L	Z

LOGIC DIAGRAM (EACH BUFFER)



OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC241FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC241DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

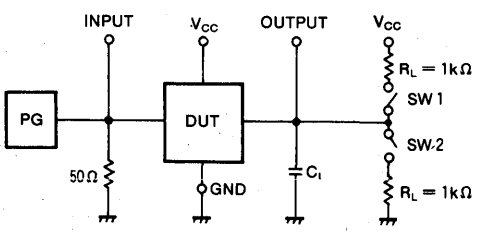
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (A − YA, B − YB)				20	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}	($\overline{EA}$ − YA, EB − YB)				25	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 4)			28	ns
t_{PZH}	($\overline{EA}$ − YA, EB − YB)				28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)	C_L = 50pF (Note 4)	2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PLH}		C_L = 150pF (Note 4)	2.0			165		208	ns
			4.5			33		42	
			6.0			28		35	
t_{PHL}			2.0			165		208	ns
			4.5			33		42	
			6.0			28		35	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, EB − YB)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, EB − YB)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = V_{CC}, EB = GND				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				59				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

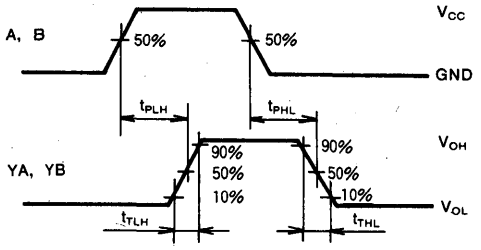
Note 4 : Test Circuit

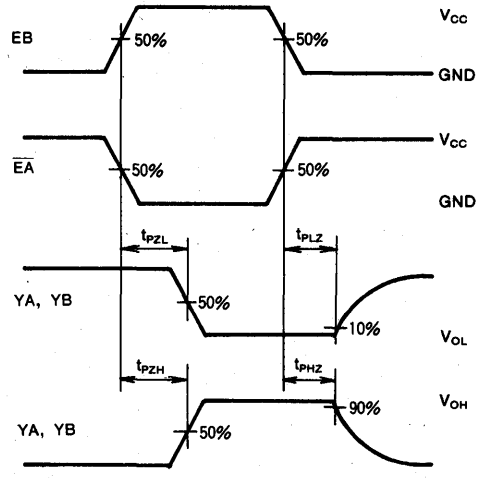


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC241-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC241-1 is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

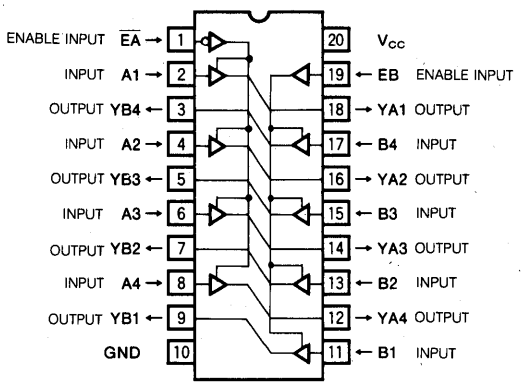
FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 8ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC241-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS241.

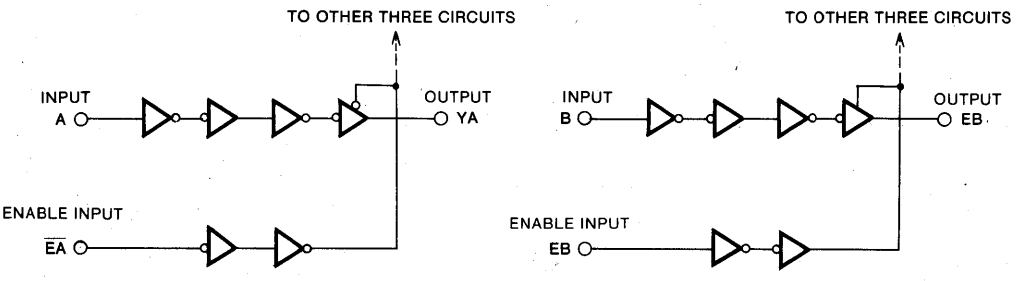
The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC241-1 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{EA}$ is low and input A is low then output YA will become low. However, if A is high then YA will become high. Inverted in the other block, a high enable input EB signal causes operation the same as that just described with input B signal output at YB.

When $\overline{EA}$ is high or EB is low then all Y within the block will become high-impedance state, irrespective of A or B.

LOGIC DIAGRAM (EACH BUFFER)



OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

FUNCTION TABLE (Note 1)

Inputs		Output
A	$\overline{EA}$	YA
L	L	L
H	L	H
X	H	Z

Inputs		Output
B	EB	YB
L	H	L
H	H	H
X	L	Z

Note 1 : Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC241-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC241-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Typ	Max	Limits −40∼+85℃ Min	Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltnge	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.98			3.84		
V_{OL}	Low-level output voltnge	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.39		0.5	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input cuuent	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output cuuent	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

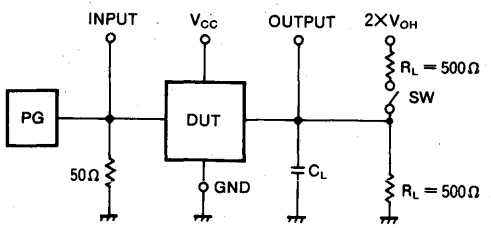
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)				16	ns
t_{PHL}					16	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, EB − YB)	C_L = 5 pF (Note 4)			18	ns
t_{PHZ}					18	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, EB − YB)	C_L = 50pF (Note 4)			21	ns
t_{PZH}					21	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)		2.0			90		115	ns
			4.5			18		23	
			6.0			15		20	
t_{PHL}			2.0			90		115	
			4.5			18		23	
			6.0			15		25	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, EB − YB)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHZ}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, EB − YB)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PZH}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = V_{CC}, EB = GND				15		15	
C_{PD}	Power dissipation capacitance (Note 3)				43				

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

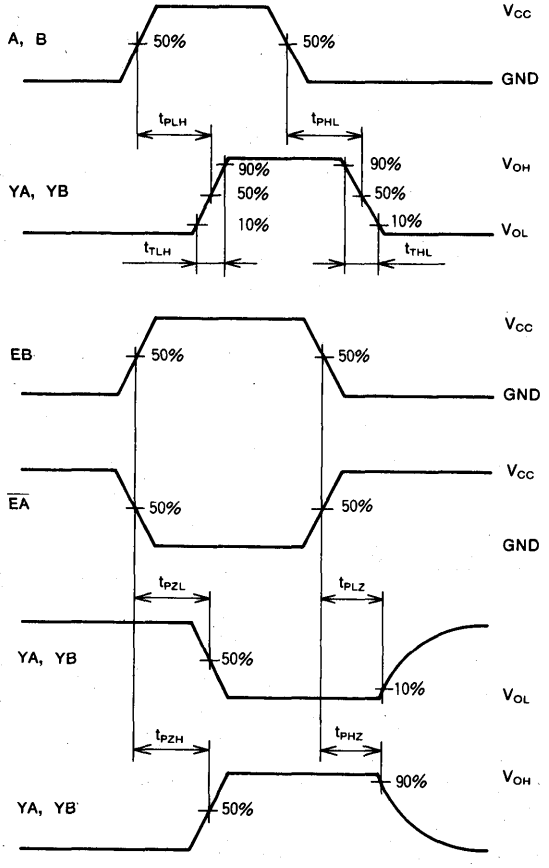
Note 4 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 3ns$, $t_f = 3ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HCT241P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT241 is a semiconductor integrated circuit consisting of two blocks of 3-state noninverting buffers each with four independent circuits that share a common enable input.

FEATURES

- TTL level input V_{IL}=0.8V max V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 15 74LSTTL loads
- Wide operating temperature range: T_a=−40∼+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

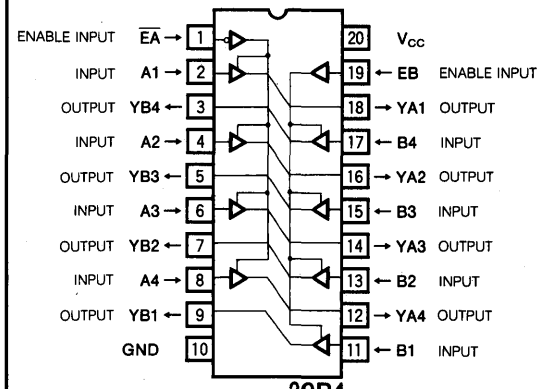
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT241 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS241.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT241 consists of two independent blocks with each block containging four buffers.

PIN CONFIGURATION (TOP VIEW)

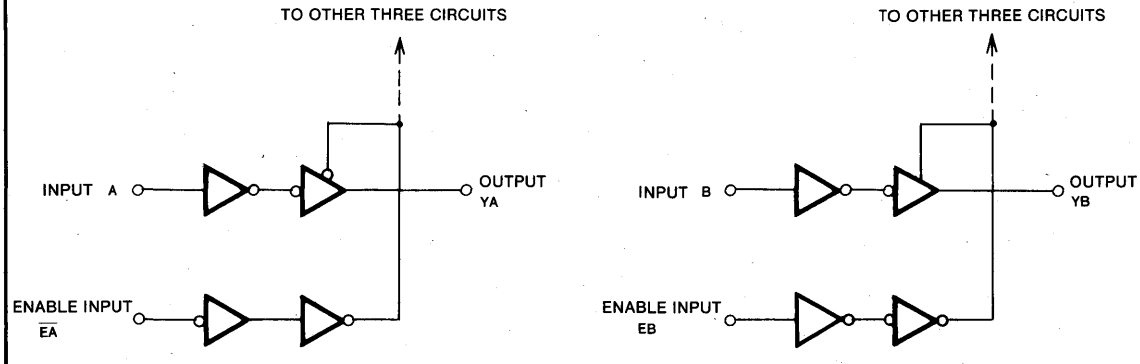


Outline 20P4 20P2N 20P2V

When enable input $\overline{EA}$ is low and input A is low then output YA will become low. However, if A is high then YA will become high. Inverted in the other block, a high enable input EB signal causes operation the same as that just described with input B signal output at YB.

When $\overline{EA}$ is high or EB is low then all Y within the block will become high-impedance state, irrespective of A or B.

LOGIC DIAGRAM (EACH BUFFER)



OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inputs		Output
A	$\overline{EA}$	YA
L	L	L
H	L	H
X	H	Z

Inputs		Output
B	EB	YB
L	H	L
H	H	H
X	L	Z

Note 1 : Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HCT241FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HCT241DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5		5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature range	−40		+85	℃
t_r, t_f	Input risetime, falltime	0		500	ns

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −6.0mA, V_{CC} = 4.5V	4.18			4.13		
			I_{OH} = −7.2mA, V_{CC} = 5.5V	5.18			5.13		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 6.0mA, V_{CC} = 4.5V			0.26		0.33	
			I_{OL} = 7.2mA, V_{CC} = 5.5V			0.26		0.33	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				4.0		40.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3), I_O = 0μA				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

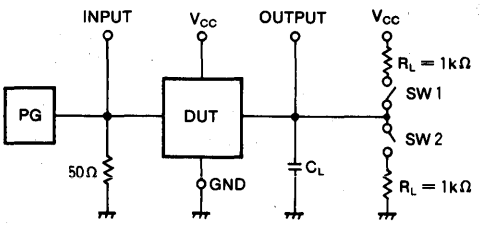
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12	ns
t_{THL}					12	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)				25	ns
t_{PHL}					25	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, EB − YB)	C_L = 5 pF (Note 5)			27	ns
t_{PHZ}					27	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, EB − YB)	C_L = 50pF (Note 5)			32	ns
t_{PZH}					32	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12		15	ns
t_{THL}					12		15	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)	C_L = 50pF (Note 5)			25		32	ns
t_{PHL}					25		32	ns
t_{PLH}		C_L = 150pF (Note 5)			40		51	ns
t_{PHL}					40		51	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, EB − YB)	C_L = 50pF (Note 5)			32		40	ns
t_{PHZ}					32		40	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, EB − YB)	C_L = 50pF (Note 5)			32		40	ns
t_{PZH}					32		40	ns
t_{PZL}		C_L = 150pF (Note 5)			47		59	ns
t_{PZH}					47		59	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = V_{CC}, EB = GND			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)			44				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

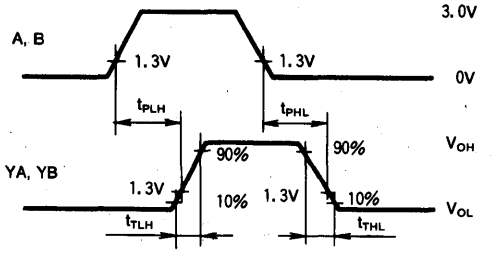
Note 5 : Test Circuit

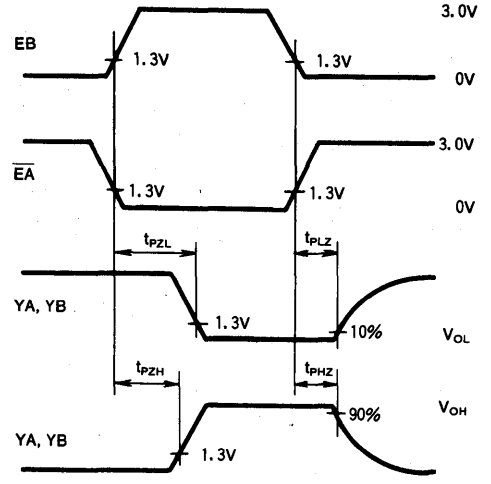


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HCT241-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT241-1 is a semiconductor integrated circuit consisting of two blocks of 3-state noninverting buffers each with four independent circuits that share a common enable input.

FEATURES

- TTL level input V_{IL}=0.8V max V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

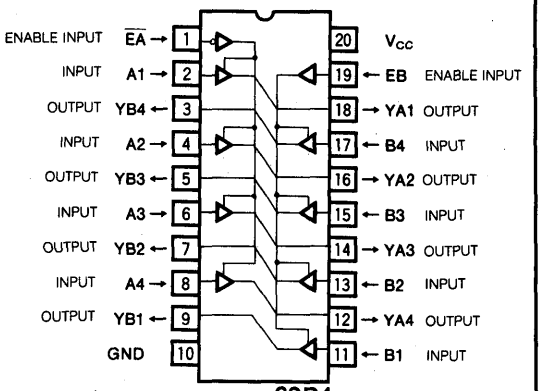
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT241-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS241.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

PIN CONFIGURATION (TOP VIEW)



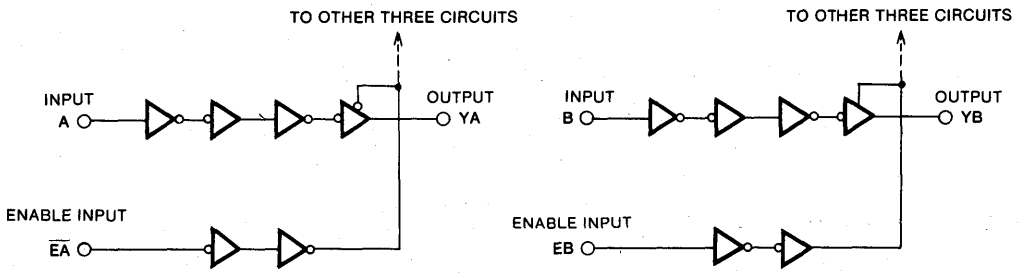
Outline 20P4 20P2N 20P2V

The M74HCT241-1 consists of two independent blocks with each block containging four buffers.

When enable input $\overline{EA}$ is low and input A is low then output YA will become low. However, if A is high then YA will become high. Inverted in the other block, a high enable input EB signal causes operation the same as that just described with input B signal output at YB.

When $\overline{EA}$ is high or EB is low then all Y within the block will become high-impedance state, irrespective of A or B.

LOGIC DIAGRAM (EACH BUFFER)



OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inputs		Output
A	$\overline{EA}$	YA
L	L	L
H	L	H
X	H	Z

Inputs		Output
B	EB	YB
L	H	L
H	H	H
X	L	Z

Note 1 : Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HCT241-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HCT241-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.39		0.5	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)				16	ns
t_{PHL}					16	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, EB − YB)	C_L = 5 pF (Note 5)			18	ns
t_{PHZ}					18	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, EB − YB)	C_L = 50pF (Note 5)			21	ns
t_{PZH}					21	

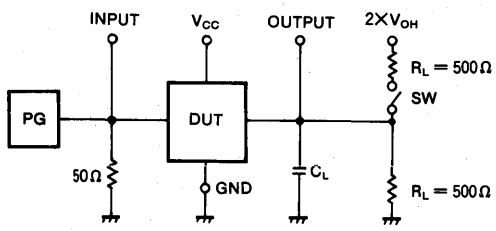
SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40∼+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40∼+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12		15	ns
t_{THL}					12		15	
t_{PLH}	Low-level to high-level and output propagation time (A − YB, B − YB)				18		23	ns
t_{PHL}					18		23	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, EB − YB)				23		29	ns
t_{PHZ}					23		29	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, EB − YB)				23		29	ns
t_{PZH}					23		29	
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = V_{CC}, $\overline{EB}$ = V_{CC}			15		15	
C_{PD}	Power dissipation capacitance (Note 4)							

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

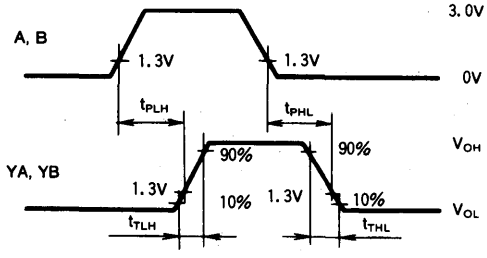
Note 5 : Test Circuit

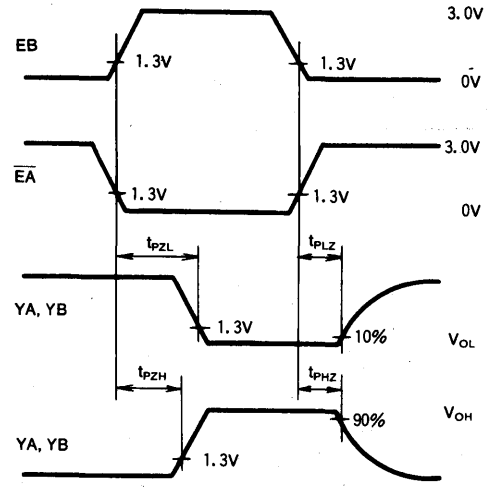


Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

M74HC242P/FP/DP

QUADRUPLE 3-STATE INVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC242 is a semiconductor integrated circuit consisting of four bus transceivers with inverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

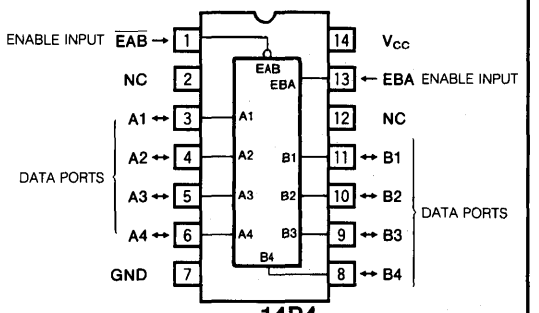
Use of silicon gate technology allows the M74HC242 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS242.

Two buffers with 3-state inverted outputs have their inputs and outputs mutually connected and can be used as buffers in both bidirectional.

The input/output direction is controlled by enable inputs $\overline{EAB}$ and EBA.

When $\overline{EAB}$ and EBA are both low, the data ports A will become input terminals and the data ports B will become output terminals. When $\overline{EAB}$ and EBA are both high, B will become output terminals and A will become output terminals. Whichever the case, the inverted signals of the input terminals will appear at the output terminals. When $\overline{EAB}$ is high and EBA is low or when $\overline{EAB}$ is low and EBA is high, A and B will both become high-impedance state and they will be separated.

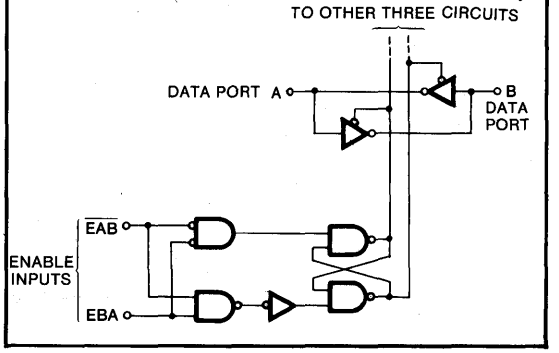
PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

NC : NO CONNECTION

LOGIC DIAGRAM (EACH TRANSCEIVER)



FUNCTION TABLE (Note 1)

Inputs		Outputs	
$\overline{EAB}$	EBA	A	B
H	H	$\overline{O}$	I
L	H	Z	Z
H	L	Z	Z
L	L	I	$\overline{O}$

Note 1 : I : Input terminal
$\overline{O}$: Output terminal (inverted outputs)
Z : High impedance

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC242FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC242DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	input risetime, faiitime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	2.0	1.9			1.9		V
		V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	4.5	4.4			4.4		
		V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	6.0	5.9			5.9		
		V_I = V_{IH}, V_{IL} ; I_{OH} = −6.0mA	4.5	4.18			4.13		
		V_I = V_{IH}, V_{IL} ; I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	2.0			0.1		0.1	V
		V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	4.5			0.1		0.1	
		V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	6.0			0.1		0.1	
		V_I = V_{IH}, V_{IL} ; I_{OL} = 6.0mA	4.5			0.26		0.33	
		V_I = V_{IH}, V_{IL} ; I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}	6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND	6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

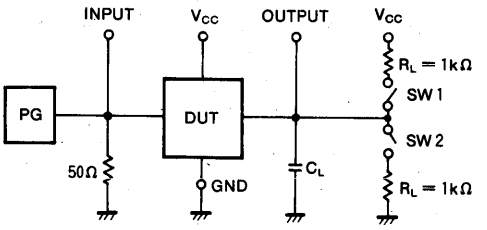
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				18	ns
t_{PHL}					18	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EAB}$ − A, B, EBA − B, A)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{EAB}$ − A, B, EBA − B, A)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)	C_L = 50pF (Note 4)	2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EAB}$ − A, B, EBA − B, A)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EAB}$ − A, B, EBA − B, A)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance					15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				58				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

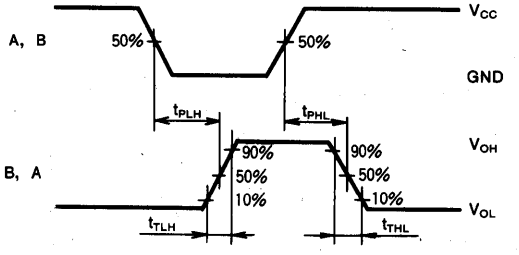
Note 4 : Test Circuit

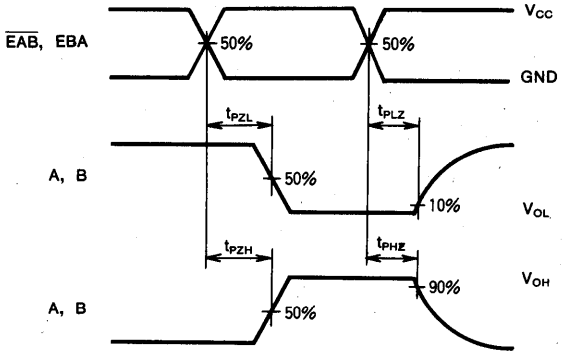


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

M74HC243P/FP/DP

QUADRUPLE 3-STATE NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC243 is a semiconductor integrated circuit consisting of four bus transceivers with noninverted outputs.

FEATURFEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC243 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS243.

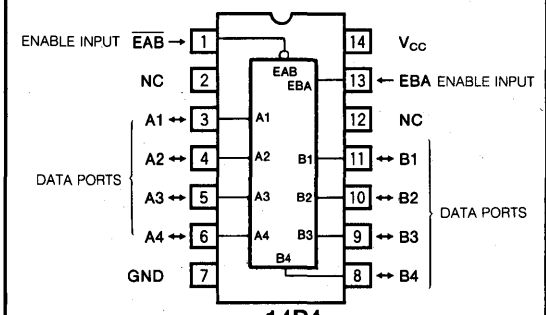
Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers ia both directions.

The input/output direction is controlled by enable inputs $\overline{EAB}$ and EBA.

When $\overline{EAB}$ and EBA are both low, the data prots A will become input terminals and the data ports B will become output terminals. When $\overline{EAB}$ and EBA are both high, B will become input terminals and A will become output terminals.

Whichever the case, the same signals as at the input terminals will appear at the output terminals. When $\overline{EAB}$ is high and EBA is low or when $\overline{EAB}$ is low and EBA is high, A and B will both become high-impedance state and they will be separated.

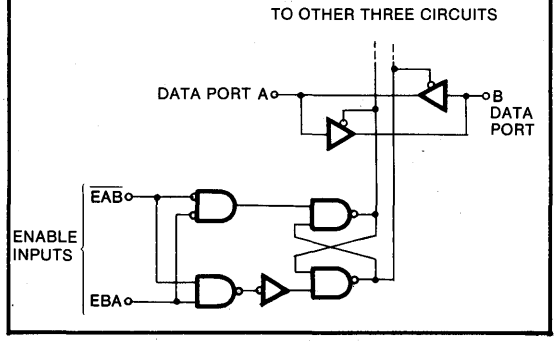
PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

NC : NO CONNECTION

LOGIC DIAGRAM (EACH TRANSCEIVER)



FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{EAB}$	EBA	A	B
H	H	O	I
L	H	Z	Z
H	L	Z	Z
L	L	I	O

Note 1 : I : Input terminal
O : Outputs
Z : High impedance

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC243FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC243DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

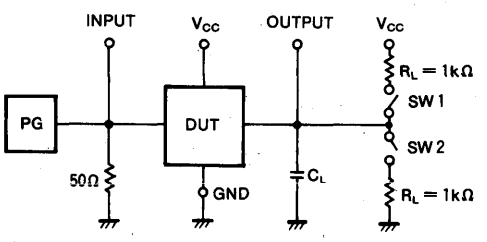
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				18	ns
t_{PHL}					18	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EAB}$ − A, B, EBA − B, A)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{EAB}$ − A, B, EBA − B, A)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)	C_L = 50pF (Note 4)	2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EAB}$ − A, B, EBA − B, A)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EAB}$ − A, B, EBA − B, A)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance					15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				71				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

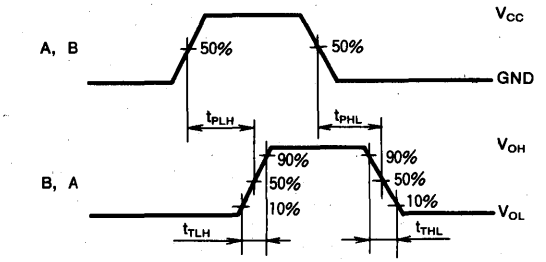
Note 4 : Test Circuit

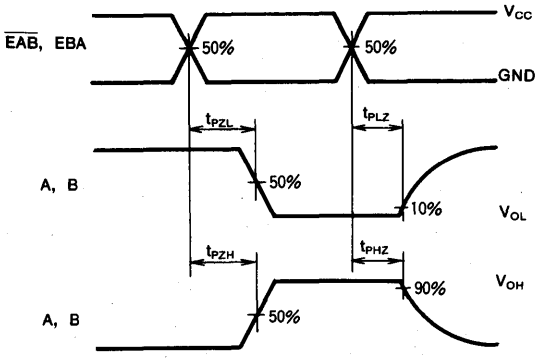


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC244P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC244 is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC244 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS244.

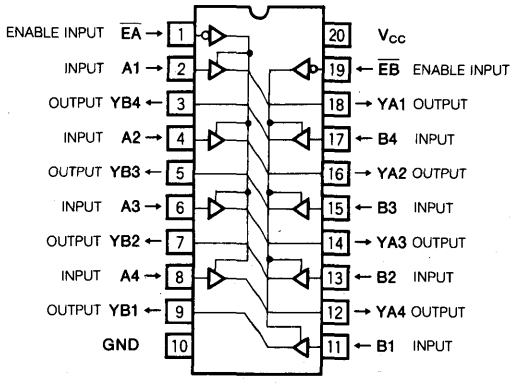
The M74HC244 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{E}$ is low and input A (or B) is low then output Y will become low. However, if A (or B) is high then Y will become high.

When $\overline{E}$ is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

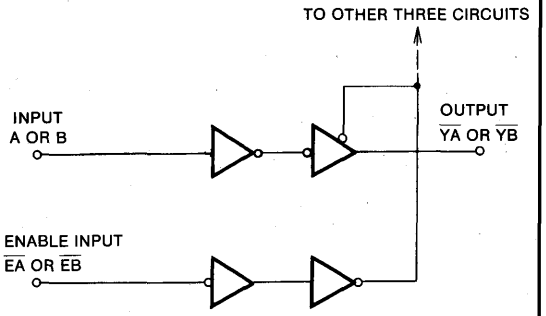
All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$ of the two blocks.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

LOGIC DIAGRAM (EACH BUFFER)



FUNCTION TABLE (Note 1)

Inputs		output
A, B	$\overline{EA}$, $\overline{EB}$	YA, YB
L	L	L
H	L	H
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC244FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC244DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −6.0mA	4.5	4.18			4.13		
		I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IL} ; I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 6.0mA	4.5			0.26		0.33	
		I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}	6.0			0.5		5.0	μA
I_{OZL}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = GND	6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

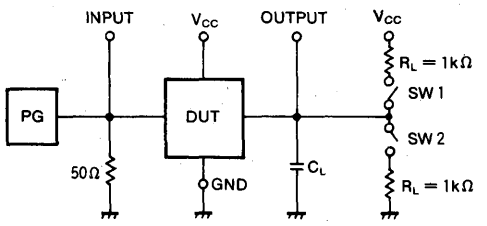
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)				20	ns
t_{PHL}					20	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)	C_L = 50pF (Note 4)	2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PLH}		C_L = 150pF (Note 4)	2.0			165		208	ns
			4.5			33		42	
			6.0			28		35	
t_{PHL}			2.0			165		208	ns
			4.5			33		42	
			6.0			28		35	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = V_{CC}, $\overline{EB}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				57				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

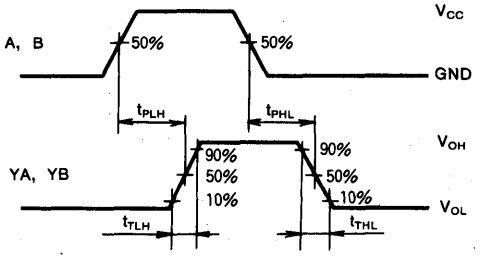
Note 4 : Test Circuit

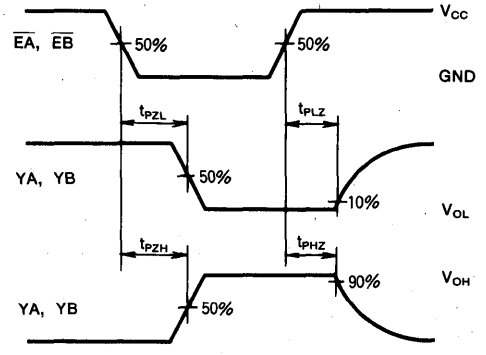


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

M74HC244-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC244-1 is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 8ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC244-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS244.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

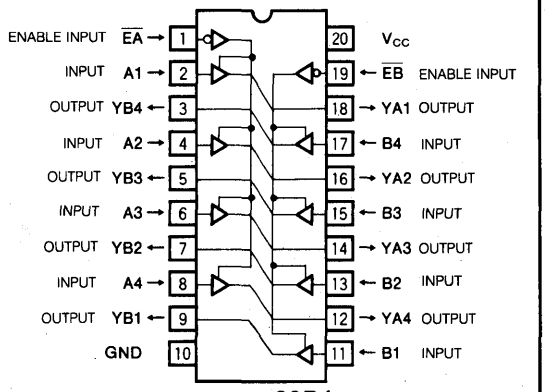
The M74HC244-1 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{E}$ is low and input A (or B) is low then output Y will become low. However, if A (or B) is high then Y will become high.

When $\overline{E}$ is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

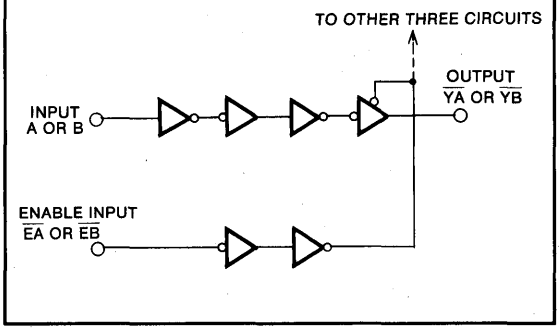
All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$ of the two blocks.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

LOGIC DIAGRAM (EACH BUFFER)



FUNCTION TABLE (Note 1)

Inputs		output
A, B	$\overline{EA}$, $\overline{EB}$	YA, YB
L	L	L
H	L	H
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC244-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC244-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits					Unit
					25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.39		0.5	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

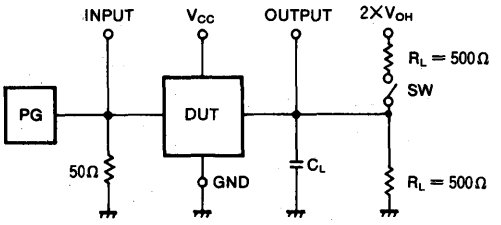
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)				16	ns
t_{PHL}					16	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 5 pF (Note 4)			18	ns
t_{PHZ}					18	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 50pF (Note 4)			23	ns
t_{PZH}					23	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)		2.0			90		115	ns
			4.5			18		23	
			6.0			15		20	
t_{PHL}			2.0			90		115	
			4.5			18		23	
			6.0			15		20	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHZ}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PZH}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = V_{CC}, $\overline{EB}$ = GND				15		15	
C_{PD}	Power dissipation capacitance (Note 3)				43				

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

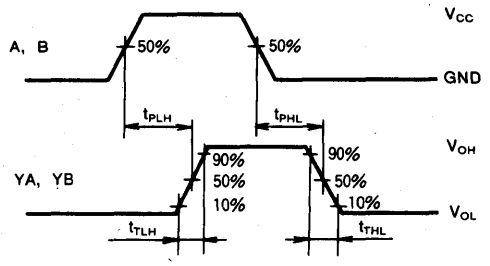
Note 4 : Test Circuit

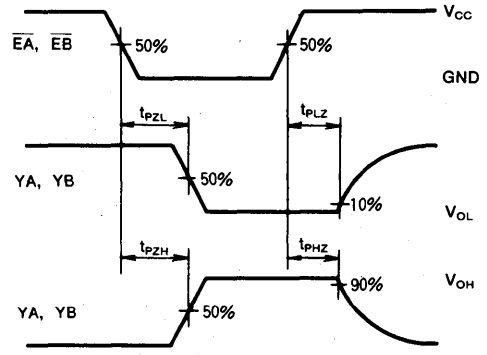


Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HCT244P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT244 is a semiconductor integrated circuit consisting of two blocks of 3-state non-invering buffers each with four independent circuits that share a common enable input.

FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT244 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS244.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed COMS. In that case, no pull-up resistros are required.

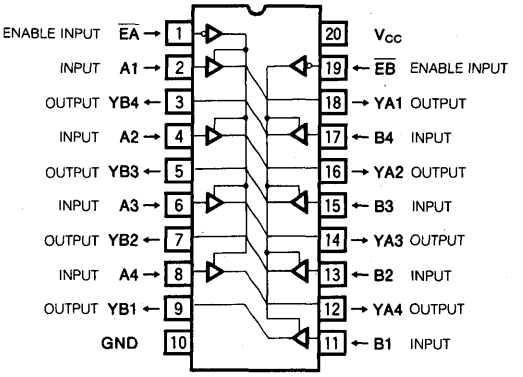
The M74HCT244 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{E}$ is low and input A (or B) is low then output Y will become low. However, if A (or B) is high then Y will become high.

When $\overline{E}$ is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

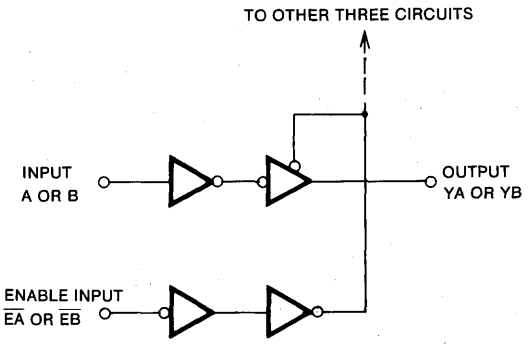
All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$ of the two blocks.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

LOGIC DIAGRAM (EACH BUFFER)



FUNCTION TABLE (Note 1)

Inputs		Output
A, B	$\overline{EA}$, $\overline{EB}$	YA, YB
L	L	L
H	L	H
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HCT244FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HCT244DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5		5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature range	−40		+85	℃
t_r, t_f	Input risetime, falltime	0		500	ns

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V, |I_O| = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, |I_O| = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −6.0mA, V_{CC} = 4.5V	4.18			4.13		
			I_{OH} = −7.2mA, V_{CC} = 5.5V	5.18			5.13		
V_{OL}	Low-level output voltage	V_I = V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 6.0mA, V_{CC} = 4.5V			0.26		0.33	
			I_{OL} = 7.2mA, V_{CC} = 5.5V			0.26		0.33	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				4.0		40.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3), I_O = 0μA				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12	ns
t_{THL}					12	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)				25	ns
t_{PHL}					25	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 5 pF (Note 5)			27	ns
t_{PHZ}					27	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 50pF (Note 5)			32	ns
t_{PZH}					32	ns

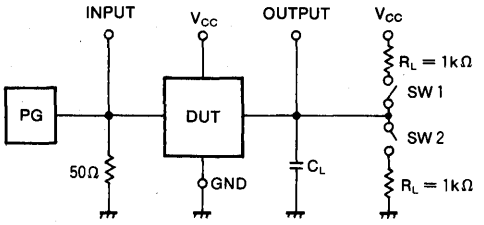
SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40∼+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40∼+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12		15	ns
t_{THL}					12		15	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)	C_L = 50pF (Note 5)			25		32	ns
t_{PHL}					25		32	ns
t_{PLH}		C_L = 150pF(Note 5)			40		51	ns
t_{PHL}					40		51	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 50pF (Note 5)			32		40	ns
t_{PHZ}					32		40	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 50pF (Note 5)			32		40	ns
t_{PZH}					32		40	ns
t_{PZL}		C_L = 150pF (Note 5)			47		59	ns
t_{PZH}					47		59	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = $\overline{EB}$ = V_{CC}			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)			45				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

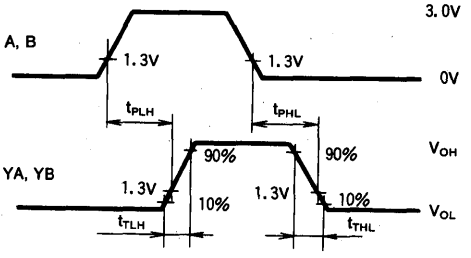
Note 5 : Test Circuit

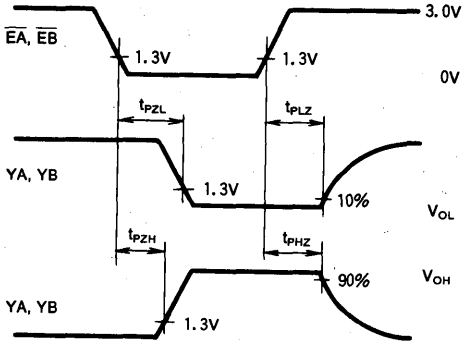


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HCT244-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT244-1 is a semiconductor integrated circuit consisting of two blocks of 3-state non-invering buffers each with four independent circuits that share a common enable input.

FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40∼+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT244-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS244.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed COMS. In that case, no pull-up resistors are required.

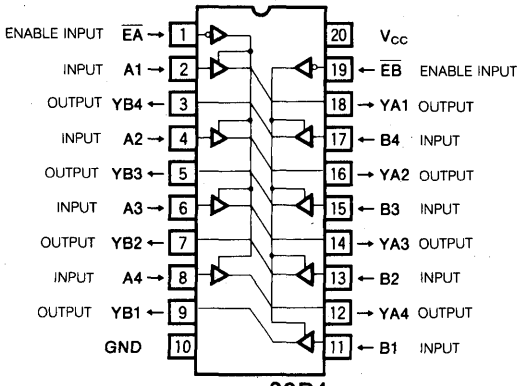
The M74HCT244-1 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{E}$ is low and input A (or B) is low then output Y will become low. However, if A (or B) is high then Y will become high.

When $\overline{E}$ is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

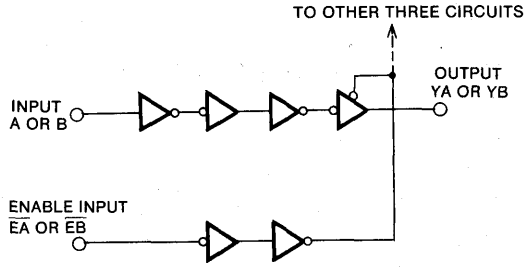
All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$ of the two blocks.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

LOGIC DIAGRAM (EACH BUFFER)



FUNCTION TABLE (Note 1)

Inputs		Output
A, B	$\overline{EA}$, $\overline{EB}$	YA, YB
L	L	L
H	L	H
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HCT244-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HCT244-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.39		0.5	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 5)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				16	ns
t_{PHL}	output propagation time (A − YA, B − YB)				16	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 5)			18	ns
t_{PHZ}	($\overline{EA}$ − YA, $\overline{EB}$ − YB)				18	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 5)			23	ns
t_{PZH}	($\overline{EA}$ − YA, $\overline{EB}$ − YB)				23	ns

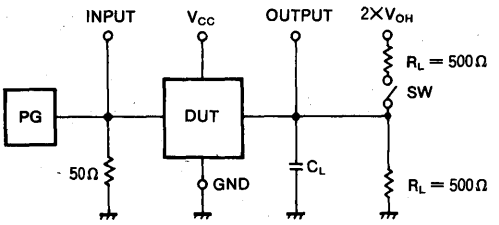
SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40∼+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40∼+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12		15	ns
t_{THL}					12		15	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)				18		23	ns
t_{PHL}					18		23	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)				23		29	ns
t_{PHZ}					23		29	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)				23		29	ns
t_{PZH}					23		29	
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = V_{CC}, $\overline{EB}$ = V_{CC}			15		15	
C_{PD}	Power dissipation capacitance (Note 4)							

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

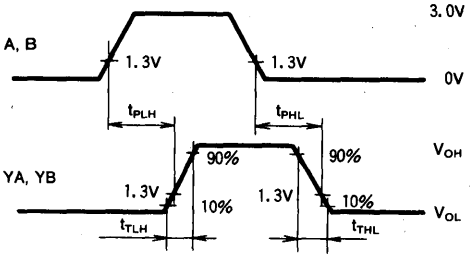
Note 5 : Test Circuit

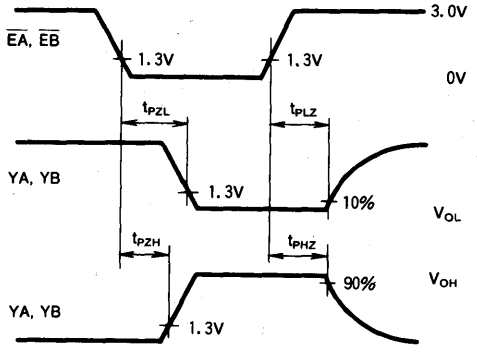


Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 3ns$, $t_f = 3ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

M74HC245P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC245 is a semiconductor integrated circuit consisting of eight transceivers with noninverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC245 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS245.

Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals.

When DIR is low, B will become input terminals and A will become output terminals.

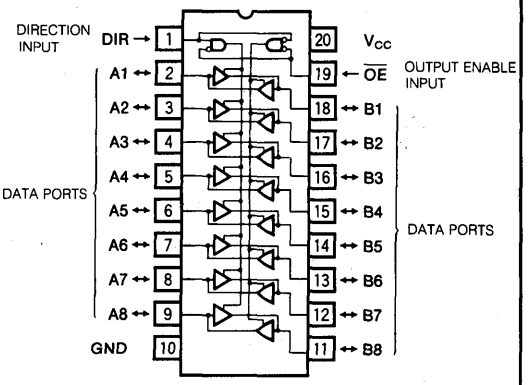
When output enable input $\overline{OE}$ is high, A and B will both become a high-impedance state and they will be separated.

FUNCTION TABLE (Note 1)

Inputs		Outputs	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

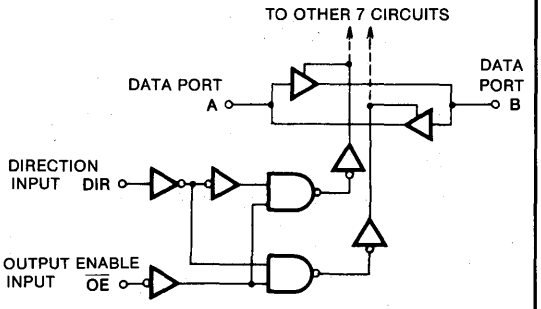
Note 1 : I : Input terminal
O : Output terminal (noninverted output)
Z : High impedance (A and B are separated)
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

LOGIC DIAGRAM (EACH TRANSCEVIER)



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC245FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC245DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

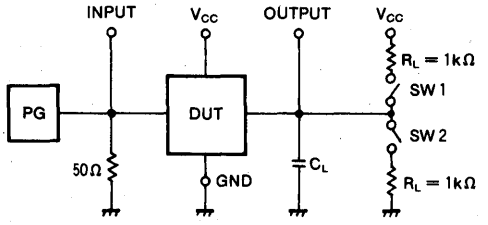
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				21	ns
t_{PHL}					21	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 5 pF (Note 4)			42	ns
t_{PHZ}					42	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)			42	ns
t_{PZH}					42	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)	C_L = 50pF (Note 4)	2.0			110		140	ns
			4.5			22		28	
			6.0			19		24	
t_{PHL}			2.0			110		140	ns
			4.5			22		28	
			6.0			19		24	
t_{PLH}		C_L = 150pF (Note 4)	2.0			195		245	ns
			4.5			39		49	
			6.0			34		43	
t_{PHL}			2.0			195		245	ns
			4.5			39		49	
			6.0			34		43	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)	2.0			172		208	ns
			4.5			43		52	
			6.0			41		50	
t_{PHZ}			2.0			172		208	ns
			4.5			43		52	
			6.0			41		50	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)	2.0			184		224	ns
			4.5			46		56	
			6.0			41		50	
t_{PZH}			2.0			184		224	ns
			4.5			46		56	
			6.0			41		50	
t_{PZL}		C_L = 150pF (Note 4)	2.0			216		260	ns
			4.5			54		65	
			6.0			47		57	
t_{PZH}			2.0			216		260	ns
			4.5			54		65	
			6.0			47		57	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				58				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

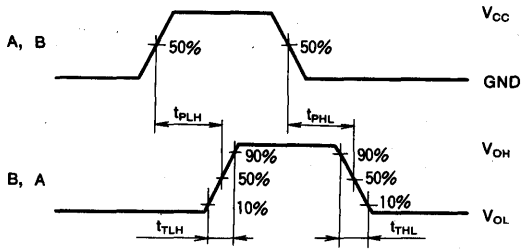
Note 4 : Test Circuit

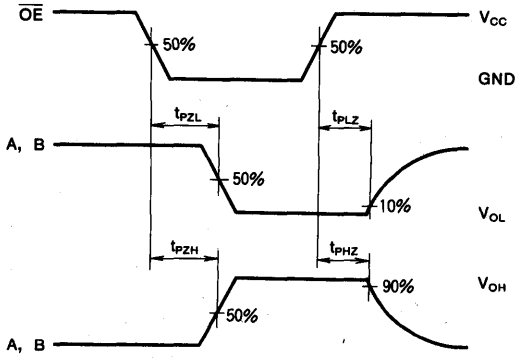


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

M74HC245-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC245-1 is a semiconductor integrated circuit consisting of eight bus transceivers with noninverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 8ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC245-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS245.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

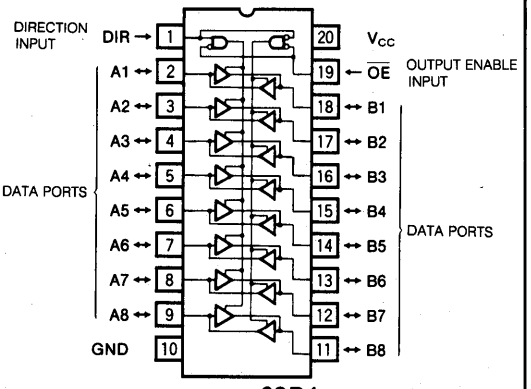
Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

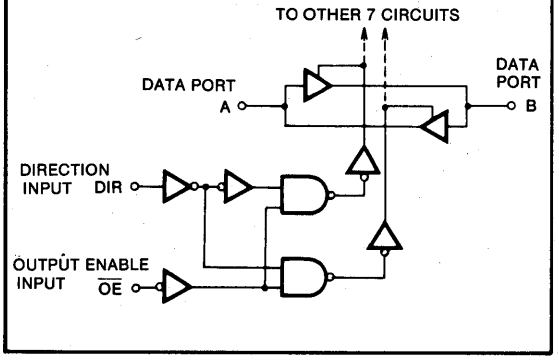
When output enable input $\overline{OE}$ is high, A and B will both become a high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

LOGIC DIAGRAM (EACH TRANSCEVIER)



FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

Note 1 : I : Input terminal
O : Output terminal (noninverted output)
Z : High impedance (A and B are separated)
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC245-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC245-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
					25℃			−40∼+85℃	
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.39		0.5	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

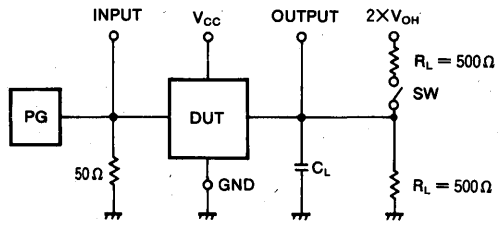
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				15	ns
t_{PHL}					15	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)		2.0			85		105	ns
			4.5			17		21	
			6.0			14		18	
t_{PHL}			2.0			85		105	
			4.5			17		21	
			6.0			14		18	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PHZ}			2.0			150		190	
			4.5			30		38	
			6.0			26		33	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PZH}			2.0			150		190	
			4.5			30		38	
			6.0			26		33	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)								

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

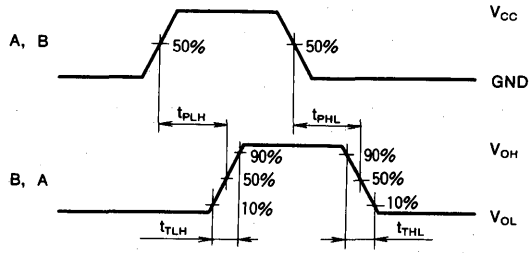
Note 4 : Test Circuit

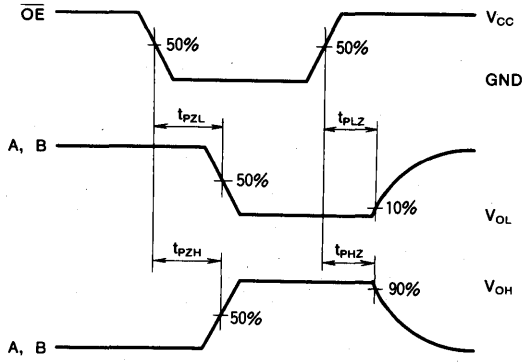


Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 3ns$, $t_f = 3ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HCT245-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT245-1 is a semiconductor integrated circuit consisting of eight transceivers with noninverted outputs.

FEATURES

- TTL level inputs V_{IL}=0.8 max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40∼+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT245-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS245.

The circuit is designed to suppress the increased switching noise that normally occrus at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

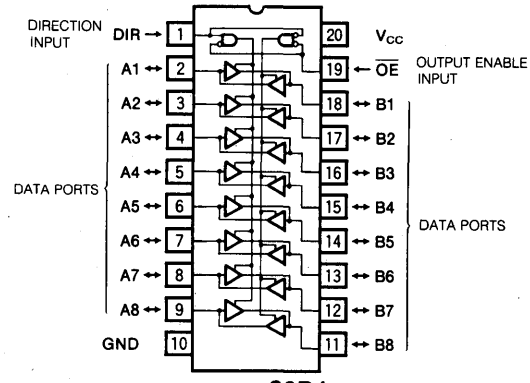
Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

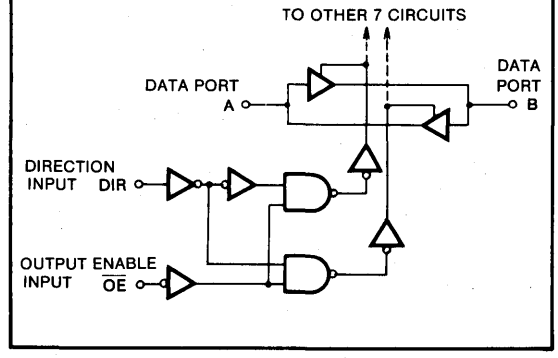
When output enable input $\overline{OE}$ is high, A and B will both become a high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

LOGIC DIAGRAM (EACH TRANSCEVIER)



FUNCTION TABLE (Note 1)

Inputs		Outputs	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

Note 1 : I : Input terminal
O : Output terminal (noninverted output)
Z : High impedance (A and B are separated)
X : Irrelevant

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HCT245-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HCT245-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.39		0.5	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

OCTAL 3-STATE
NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 5)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				15	ns
t_{PHL}	output propagation time (A − B, B − A)				15	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 5)			25	ns
t_{PHZ}	($\overline{OE}$ − A, B)				25	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 5)			28	ns
t_{PZH}	($\overline{OE}$ − A, B)				28	ns

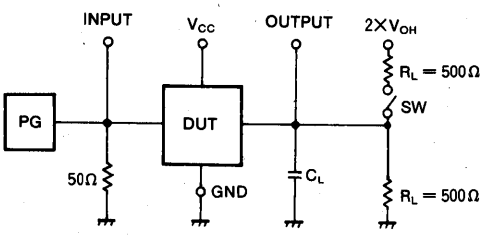
SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40∼+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40∼+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12		15	ns
t_{THL}					12		15	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				17		21	ns
t_{PHL}					17		21	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)				30		38	ns
t_{PHZ}					30		38	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)				30		38	ns
t_{PZH}					30		38	
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	
C_{PD}	Power dissipation capacitance (Note 4)							

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

OCTAL 3-STATE
NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

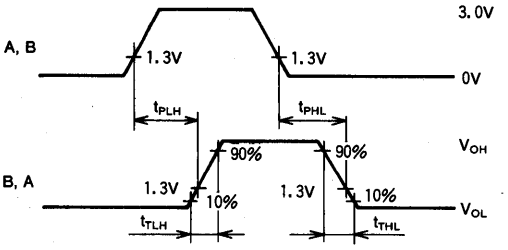
Note 5 : Test Circuit

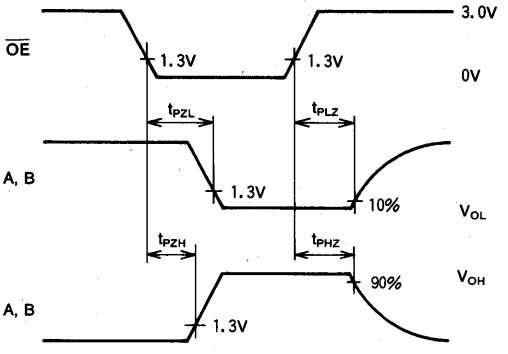


Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 3ns$, $t_f = 3ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC251P/FP/DP

8-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC251 is a semiconductor integrated circuit consisting of an 8-line to 1-line data selector/multiplexer with 3-state outputs.

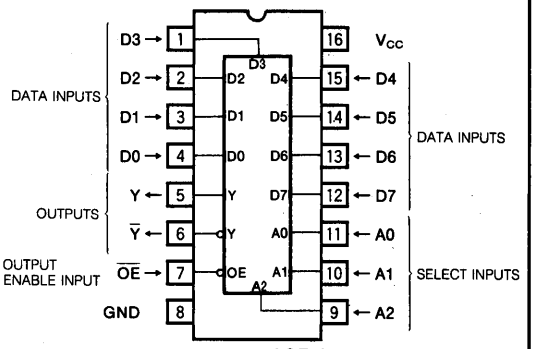
FEATURES

- High-speed: 20ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

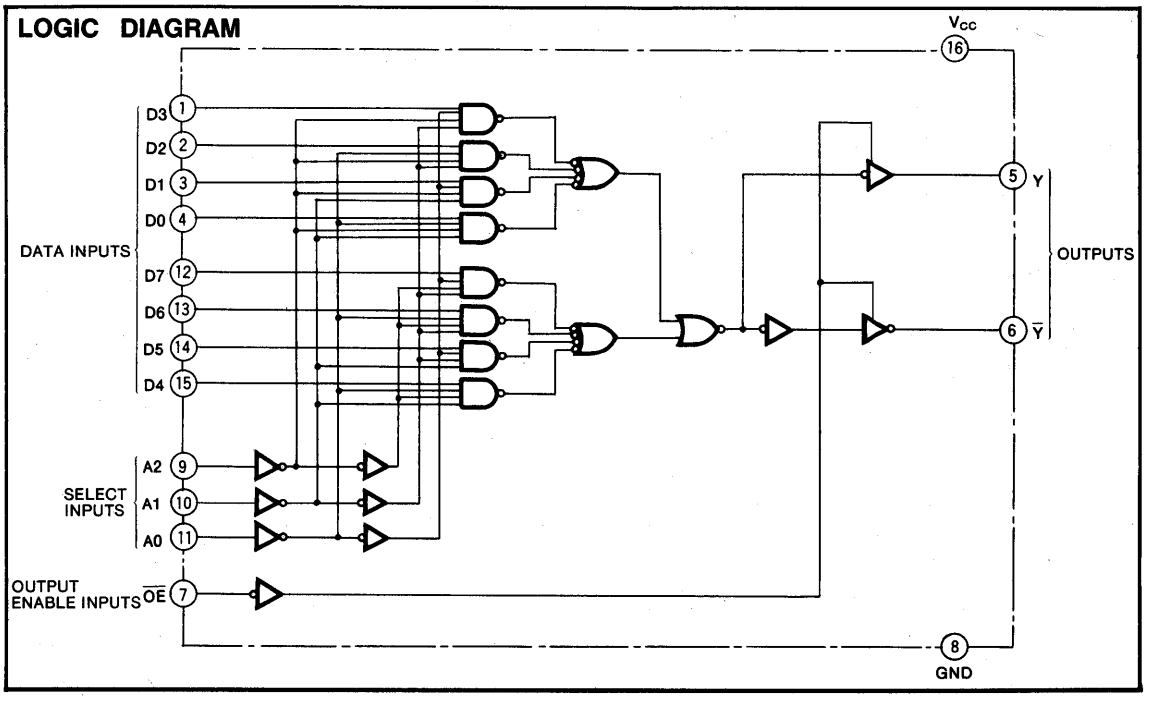
Use of silicon gate technology allows the M74HC251 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS251.

The M74HC251 consists of data selector functions for selecting one of eight input line signals and multiplexer functions for converting 8-bit parallel data into serial data using time-division.

The 8-line signal is applied to data inputs D0 through D7, and after one of the data inputs has been selected by select inputs A0 through A2, that input signal will be output at Y or an inverted signal will be output at Y. By applying 8-bit parallel data to D0 through D7, and connecting the output of a synchronous octal counter to A0 through A2, D0 through D7 data will be output at Y synchronous with the clock pulse in the order of D0-D7. When output-enable input $\overline{OE}$ is high, all outputs will become a high-impedance state irrespective of other inputs.

M74HC251 has the same functions and pin connections as the M74HC151, but the former has a 3-state output.

LOGIC DIAGRAM



8-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

Inputs												Output	
A2	A1	A0	$\overline{OE}$	D0	D1	D2	D3	D4	D5	D6	D7	Y	$\overline{Y}$
X	X	X	H	X	X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	L	H
L	L	L	L	H	X	X	X	X	X	X	X	H	L
L	L	H	L	X	L	X	X	X	X	X	X	L	H
L	L	H	L	X	H	X	X	X	X	X	X	H	L
L	H	L	L	X	X	L	X	X	X	X	X	L	H
L	H	L	L	X	X	H	X	X	X	X	X	H	L
L	H	H	L	X	X	X	L	X	X	X	X	L	H
L	H	H	L	X	X	X	H	X	X	X	X	H	L
H	L	L	L	X	X	X	X	L	X	X	X	L	H
H	L	L	L	X	X	X	X	H	X	X	X	H	L
H	L	H	L	X	X	X	X	X	L	X	X	L	H
H	L	H	L	X	X	X	X	X	H	X	X	H	L
H	H	L	L	X	X	X	X	X	X	L	X	L	H
H	H	L	L	X	X	X	X	X	X	H	X	H	L
H	H	H	L	X	X	X	X	X	X	X	L	L	H
H	H	H	L	X	X	X	X	X	X	X	H	H	L

Note 1 : X : Irrelevant
Z : High impedance

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC251FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC251DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				29	ns
t_{PHL}	output propagation time (D − Y)				29	ns
t_{PLH}	Low-level to high-level and high-level to low-level				32	ns
t_{PHL}	output propagation time (D − $\overline{Y}$)				32	ns
t_{PLH}	Low-level to high-level and high-level to low-level				35	ns
t_{PHL}	output propagation time (A − Y)				35	ns
t_{PLH}	Low-level to high-level and high-level to low-level				35	ns
t_{PHL}	output propagation time (A − $\overline{Y}$)				35	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 4)			35	ns
t_{PHZ}	($\overline{OE}$ − Y)				35	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 15pF (Note 4)			26	ns
t_{PZH}	($\overline{OE}$ − Y)				26	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 4)			40	ns
t_{PHZ}	($\overline{OE}$ − $\overline{Y}$)				40	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 15pF (Note 4)			27	ns
t_{PZH}	($\overline{OE}$ − $\overline{Y}$)				27	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

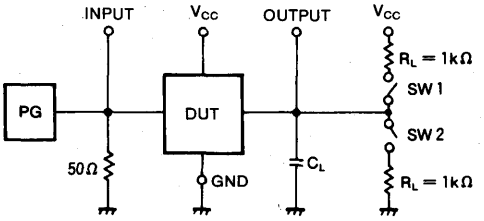
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Y)		2.0			195		244	ns
			4.5			39		49	
			6.0			33		41	
t_{PHL}			2.0			195		244	ns
			4.5			39		49	
			6.0			33		41	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($D - \overline{Y}$)		2.0			185		231	ns
			4.5			37		46	
			6.0			32		40	
t_{PHL}			2.0			185		231	ns
			4.5			37		46	
			6.0			32		40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)		2.0			205		256	ns
			4.5			41		51	
			6.0			35		44	
t_{PHL}			2.0			205		256	ns
			4.5			41		51	
			6.0			35		44	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($A - \overline{Y}$)		2.0			205		256	ns
			4.5			41		51	
			6.0			35		44	
t_{PHL}			2.0			205		256	ns
			4.5			41		51	
			6.0			35		44	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)		2.0			195		244	ns
			4.5			39		49	
			6.0			33		41	
t_{PHZ}			2.0			195		244	ns
			4.5			39		49	
			6.0			33		41	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)		2.0			145		181	ns
			4.5			29		36	
			6.0			25		31	
t_{PZH}			2.0			145		181	ns
			4.5			29		36	
			6.0			25		31	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Y}$)		2.0			220		275	ns
			4.5			44		55	
			6.0			37		46	
t_{PHZ}			2.0			220		275	ns
			4.5			44		55	
			6.0			37		46	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃) (continued)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			150		188	ns
			4.5			30		38	
			6.0			26		33	
t_{PZH}			2.0			150		188	ns
			4.5			30		38	
			6.0			26		33	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				67				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

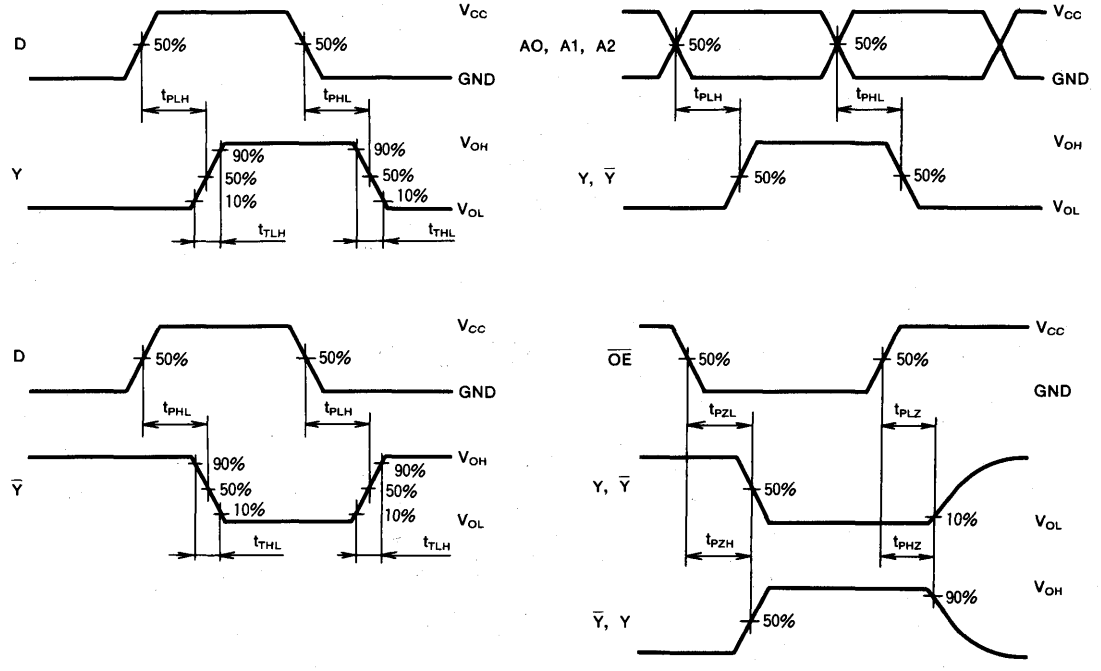
Note 4 : Test Circuit



Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC253P/FP/DP

DUAL 4-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC253 is a semiconductor integrated circuit consisting of two 4-line to 1-line data selectors/multiplexrs with 3-state outputs.

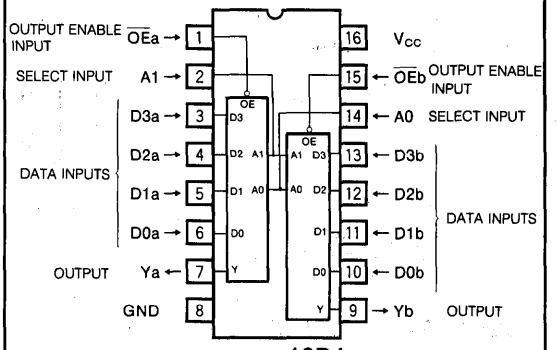
FEATURES

- High-speed: 18ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4 16P2N 16P2P

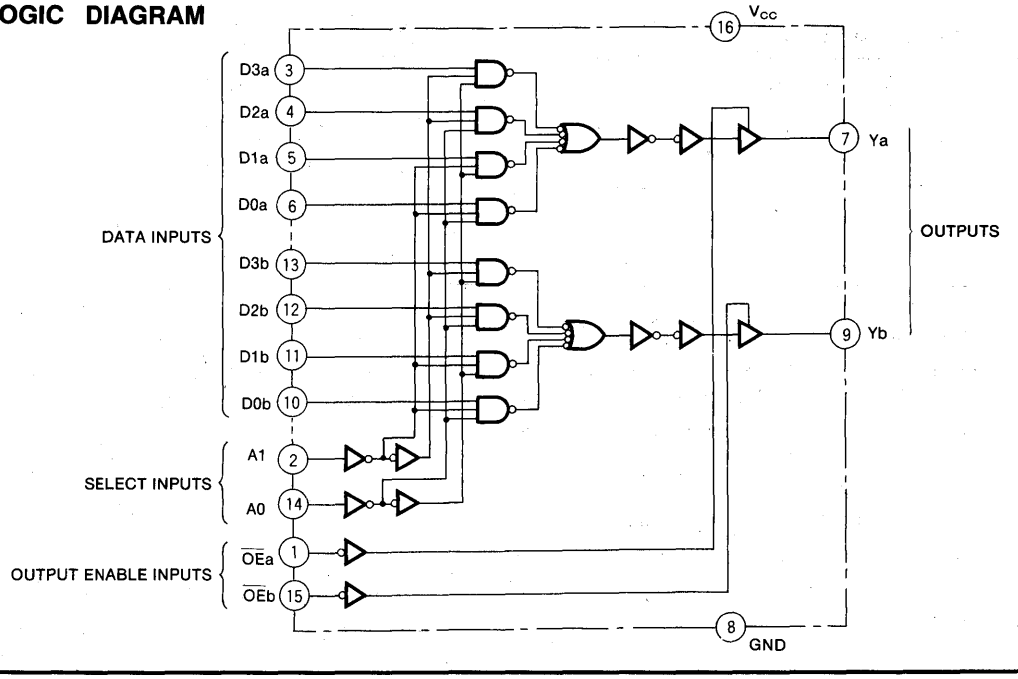
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC253P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS253.

The M74HC253 consists of data selector functions for selecting one of four input line signals and multiplex functions for converting 4-bit parallel data into serial data using time-division.

The 4-line signal is applied to data inputs D0 through D7, and after one of the data inputs has been selected by select inputs A0 and A1, that input signal will be output at Y. By applying 4-bit parallel data to D0 through D3, and connecting the output of a synchronous quadruple counter to A0 and A1, D0 through D3 data will be output at Y synchronous with the clock pulse in the order of D0-D3. Slelct inputs A are common to the two circuits while the output-enable inputs $\overline{OE}$ are independent. When $\overline{OE}$ is high, Y will become a high-impedance state irrespective of other inputs.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

DUAL 4-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

Inputs							Output
A1	A0	D0	D1	D2	D3	$\overline{OE}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Note 1 : X : Irrelevant
Z : High impedance

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC253FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC253DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

DUAL 4-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

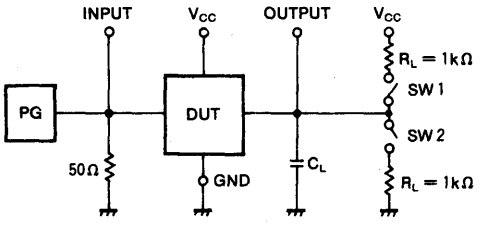
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Y)				23	ns
t_{PHL}					23	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)				30	ns
t_{PHL}					30	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)	C_L = 5 pF (Note 4)			27	ns
t_{PHZ}					27	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)	C_L = 15pF (Note 4)			18	ns
t_{PZH}					18	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Y)		2.0			126		158	ns
			4.5			28		35	
			6.0			23		29	
t_{PHL}			2.0			126		158	ns
			4.5			28		35	
			6.0			23		29	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)		2.0			158		198	ns
			4.5			35		44	
			6.0			30		38	
t_{PHL}			2.0			158		198	ns
			4.5			35		44	
			6.0			30		38	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)		2.0			135		169	ns
			4.5			30		38	
			6.0			25		31	
t_{PHZ}			2.0			135		169	ns
			4.5			30		38	
			6.0			25		31	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)		2.0			90		113	ns
			4.5			20		25	
			6.0			17		21	
t_{PZH}			2.0			90		113	ns
			4.5			20		25	
			6.0			17		21	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				61				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

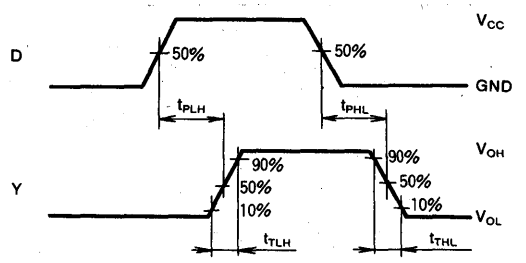
Note 4 : Test Circuit

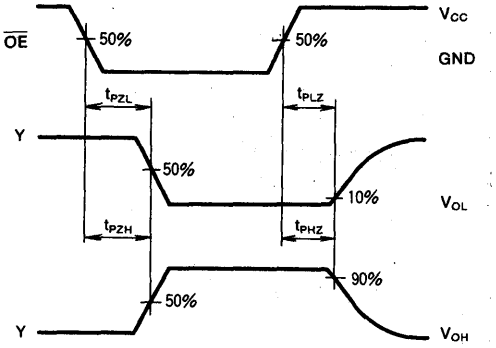


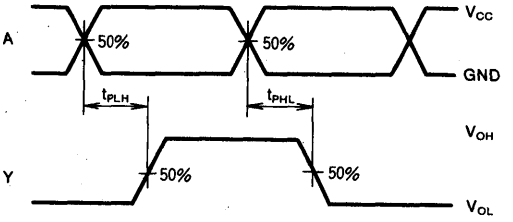
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







M74HC257P/FP/DP

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC257 is a semiconductor integrated circuit consisting of four 2-line to 1-line data selectors/multiplexers with 3-state outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

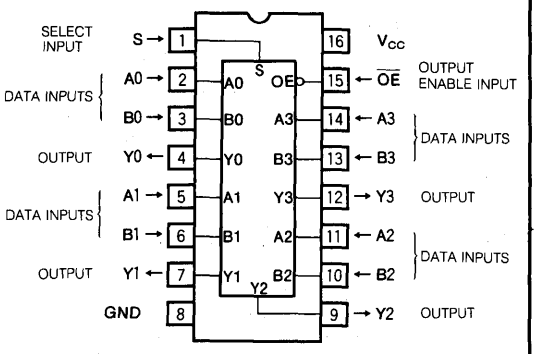
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC257 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS257.

The M74HC257 consists of four circuits each containing date selector functions for selecting one of two input line signals and multiplexer functions for converting 2-bit parallel data into serial data using time-division.

PIN CONFIGURATION (TOP VIEW)

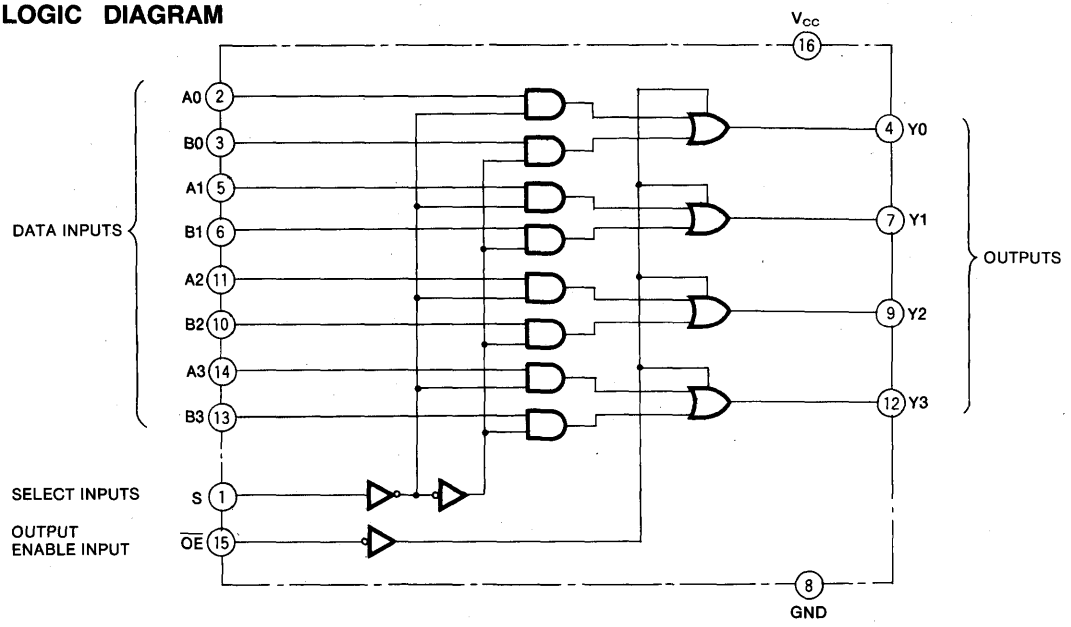


Outline 16P4, 16P2N, 16P2P

The 2-line signal is applied to data inputs A and B, and after one of the data inputs has been selected by select input S, it is output at pin Y. By applying 2-bit parallel data to A and B, and connecting the output of a binary counter to S, A and B date will be output at Y synchronous with the clock pulse in the order A-B. Both S and output-enable input $\overline{OE}$ are common to all four circuits.

When $\overline{OE}$ is high, all outputs Y will become high impedance state irrespective of other inputs.

LOGIC DIAGRAM



QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

Inputs				Output
$\overline{OE}$	S	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Note 1 : X : Irrelevant
Z : High impedance

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC257FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC257DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				18	ns
t_{PHL}	output propagation time (A, B−Y)				18	ns
t_{PLH}	Low-level to high-level and high-level to low-level				29	ns
t_{PHL}	output propagation time (S−Y)				29	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 4)			23	ns
t_{PHZ}	($\overline{OE}$−Y)				23	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 4)			20	ns
t_{PZH}	($\overline{OE}$−Y)				20	ns

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

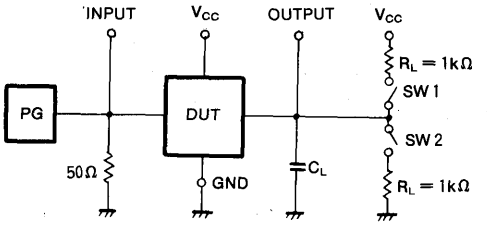
SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B−Y)	C_L = 50pF (Note 4)	2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S−Y)	C_L = 50pF (Note 4)	2.0			160		200	ns
			4.5			32		40	
			6.0			27		34	
t_{PHL}			2.0			160		200	ns
			4.5			32		40	
			6.0			27		34	
t_{PLH}		C_L = 150pF (Note 4)	2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PHL}			2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$−Y)	C_L = 50pF (Note 4)	2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
t_{PHZ}			2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$−Y)	C_L = 50pF (Note 4)	2.0			110		140	ns
			4.5			22		28	
			6.0			19		24	
t_{PZH}			2.0			110		140	ns
			4.5			22		28	
			6.0			19		24	
t_{PZL}		C_L = 150pF (Note 4)	2.0			160		200	ns
			4.5			32		40	
			6.0			27		34	
t_{PZH}			2.0			160		200	ns
			4.5			32		40	
			6.0			27		34	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitace	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

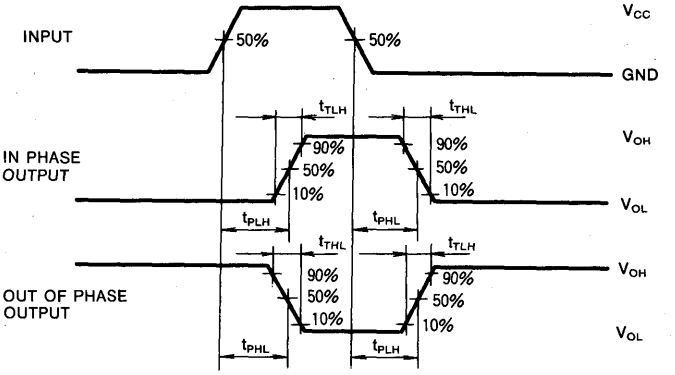
Note 4 : Test Circuit

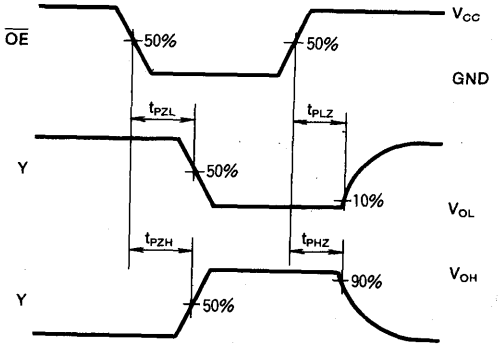


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC258P/FP/DP

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC258 is a semiconductor integrated circuit consisting of four 2-line to 1-line data selectors/multiplexers with 3-state outputs.

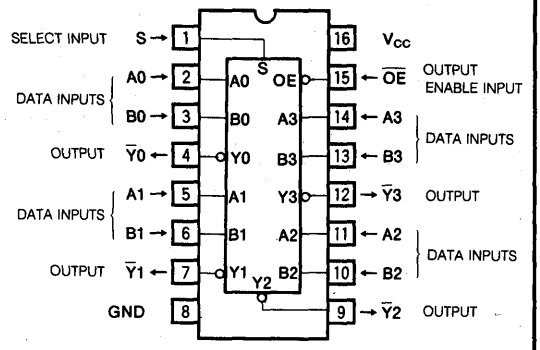
FEATURES

- High-fanout 3-state output (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N
16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC258P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS258.

The M74HC258 consists of four circuits each containing data selector functions for selecting one of two input line signals and multiplexer functions for converting 2-bit parallel data into serial data using time-division.

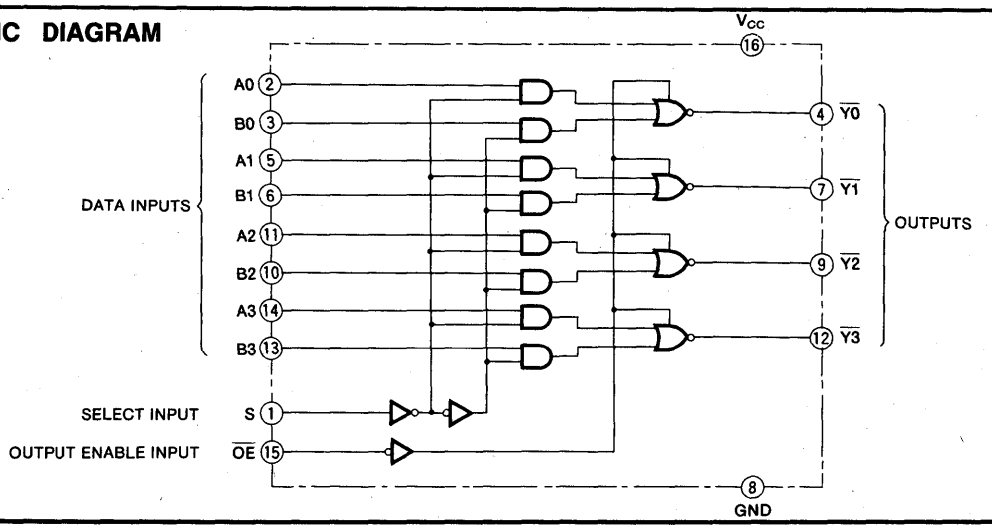
The 2-line signals are applied to data inputs A and B, and after one of the data inputs has been selected by select input S, it is output at pin $\overline{Y}$. By applying 2-bit parallel data to A and B, and connecting the output of a binary counter to S, the data at A and B will be inverted and sequentially output at $\overline{Y}$ in synchronous with the clock pulse in the order A-B. S and output-enable input $\overline{OE}$ are common to all four circuits. When $\overline{OE}$ is high, all outputs Y will become high impedance state irrespective of other inputs.

FUNCTION TABLE (Note 1.)

Inputs				Output
$\overline{OE}$	S	A	B	$\overline{Y}$
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

Note 1 : X : Irrelevant
Z : High impedance

LOGIC DIAGRAM



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QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC258FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC258DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − $\overline{Y}$)				18	ns
t_{PHL}					18	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S − $\overline{Y}$)				18	ns
t_{PHL}					18	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

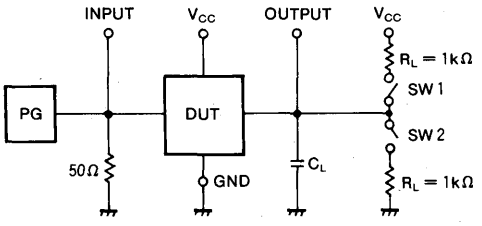
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃) (Continued)

Symbol	Parameter	Test conditions	Limits					Unit
				25℃			−40~+85℃	
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output eaable time to low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

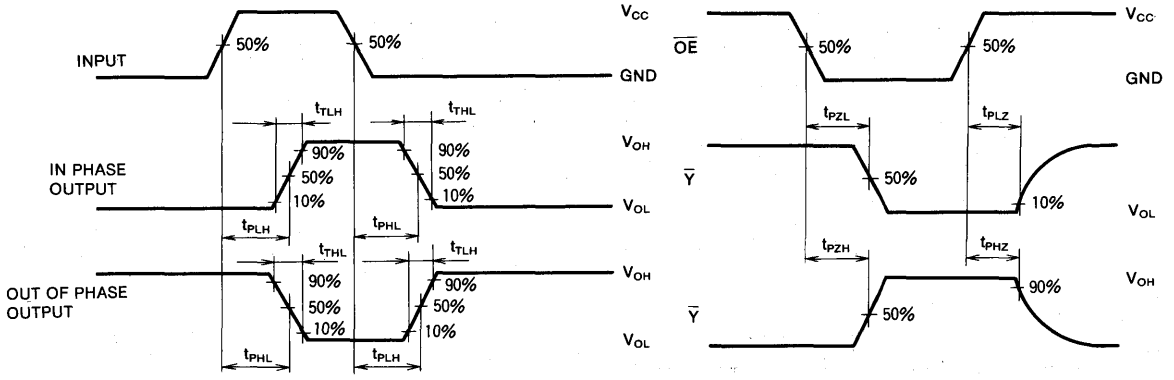
Note 4 : Test Circuit



Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC259P/FP/DP

8-BIT ADDRESSABLE LATCH/1-OF-8 DECODER

DESCRIPTION

The M74HC259 is a semiconductor integrated circuit consisting of eight latches and a demultiplexer which designates the latches with a 3-bit binary code.

FEATURES

- High-speed: 18ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2～6V
- Wide operating temperature range: T_a=−40～+85℃

APPLICATION

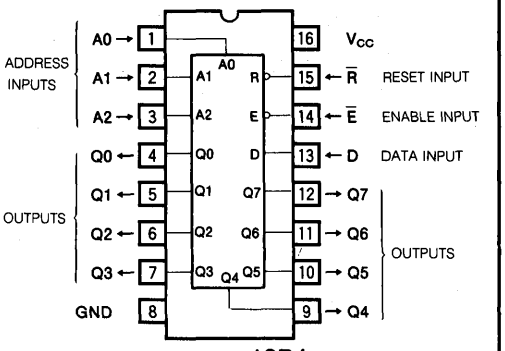
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC259 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS259.

The M74HC259 consists of a 3-bit binary-to-octal demultiplexer and eight latchs. The following operational modes can be selected by combining the enable input $\overline{E}$ and reset input $\overline{R}$.

PIN CONFIGURATION (TOP VIEW)

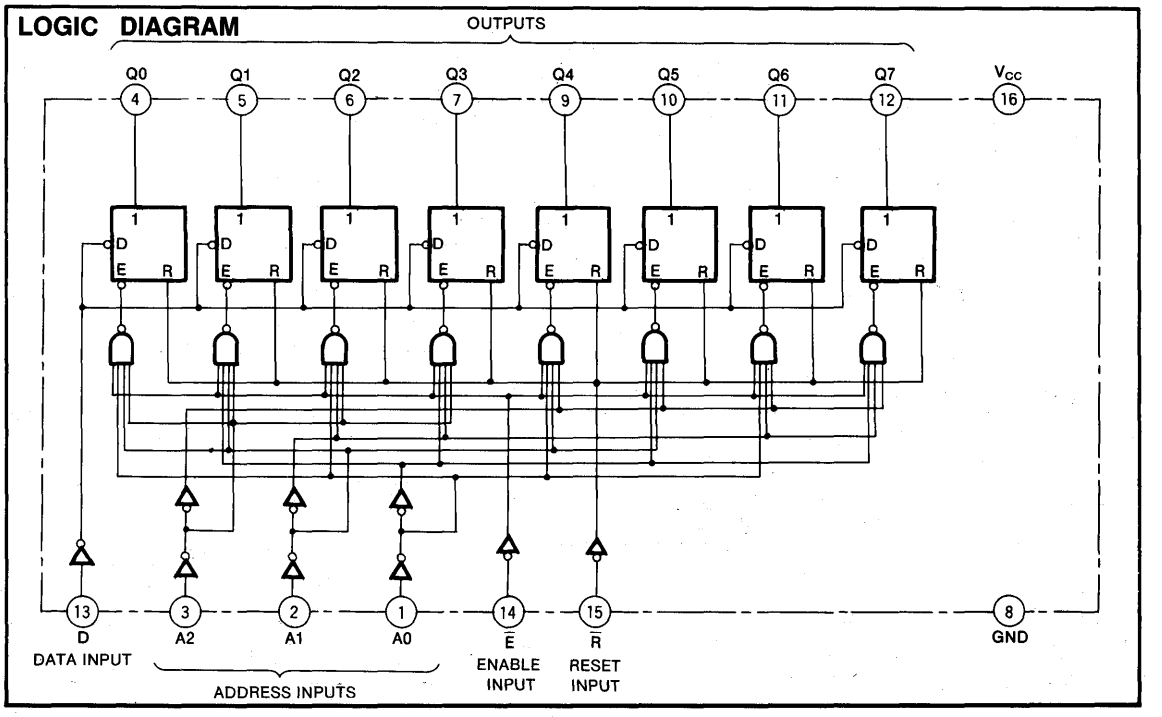


Outline 16P4, 16P2N, 16P2P

(1) 3-bit binary-to-octal decoder/demultiplexer ($\overline{E}$ low, $\overline{R}$ low)
(2) Addressable latch ($\overline{E}$ low, $\overline{R}$ high)
(3) Data input inhibit ($\overline{E}$ high, $\overline{R}$ high)
(4) Direct reset ($\overline{E}$ high, $\overline{R}$ low)

When this device is used as a 3-bit binary-to-octal decoder/demultiplexer, and the select inputs A0～A2 are designated by a 3-bit binary number, the same signal as the data

LOGIC DIAGRAM



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input D will appear in one of the outputs Q0～Q7 corresponding to that number and all the other outputs will be low. The latch does not operate in this mode. When used as an addressable latch and inputs A0～A2 are designated as above, the corresponding latch will be selected and the same signal as D will appear in the output.
When $\overline{E}$ changes from low to high (data inhibit mode), the information from the data input D immediately before the change will be latched. When $\overline{E}$ is low, the signal appearing in Q will be also changed if the signal D is changed.
In the data input inhibit mode, Q0～Q7 will not change even if D is changed and the status before $\overline{E}$ is high will be held.
In the direct reset mode, all outputs will be reset to low, irrespective of the status of D or A0～A2.

FUNCTION TABLE (Note 1)

Operation mode	Inputs						Outputs							
	$\overline{R}$	$\overline{E}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Direct reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
3-bit binary-to-octal decoder/demultiplexer	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	H	L	L	L	L	L	L	L	L	L	L
	L	L	H	H	L	L	L	H	L	L	L	L	L	L
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	L	L	L	H	H	H	L	L	L	L	L	L	L	L
	L	L	H	H	H	H	L	L	L	L	L	L	L	H
Data input suspension	H	H	X	X	X	X	$Q0^0$	$Q1^0$	$Q2^0$	$Q3^0$	$Q4^0$	$Q5^0$	$Q6^0$	$Q7^0$
Addressable latch	H	L	L	L	L	L	L	$Q1^0$	$Q2^0$	$Q3^0$	$Q4^0$	$Q5^0$	$Q6^0$	$Q7^0$
	H	L	H	L	L	L	H	$Q1^0$	$Q2^0$	$Q3^0$	$Q4^0$	$Q5^0$	$Q6^0$	$Q7^0$
	H	L	L	H	L	L	$Q0^0$	L	$Q2^0$	$Q3^0$	$Q4^0$	$Q5^0$	$Q6^0$	$Q7^0$
	H	L	H	H	L	L	$Q0^0$	H	$Q2^0$	$Q3^0$	$Q4^0$	$Q5^0$	$Q6^0$	$Q7^0$
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	H	L	L	H	H	H	$Q0^0$	$Q1^0$	$Q2^0$	$Q3^0$	$Q4^0$	$Q5^0$	$Q6^0$	L
	H	L	H	H	H	H	$Q0^0$	$Q1^0$	$Q2^0$	$Q3^0$	$Q4^0$	$Q5^0$	$Q6^0$	H

Note 1 : X : Irrelevant
Q^0 : Output state Q before enable input changes

ABSOLUTE MAXIMUM RATINGS (T_a = −40～+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+7.0	V
V_I	Input voltage		−0.5～V_{CC}+0.5	V
V_O	Output voltage		−0.5～V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65～+150	℃

Note 2 : M74HC259FP, T_a = −40～+70℃ and T_a = 70～85℃ are derated at −6mW/℃.
M74HC259DP, T_a = −40～+50℃ and T_a = 50～85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40～+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)				32	ns
t_{PHL}					32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Q)				38	ns
t_{PHL}					38	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{E}$ − Q)				35	ns
t_{PHL}					35	
t_{PHL}	High-level to low-level output propagation time ($\overline{R}$ − Q)				27	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

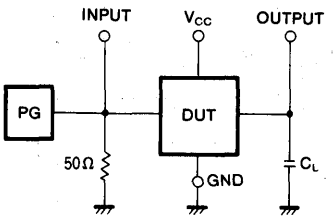
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)		2.0			180		225	ns
			4.5			37		46	
			6.0			32		40	
t_{PHL}			2.0			180		225	
			4.5			37		46	
			6.0			32		40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Q)		2.0			220		275	ns
			4.5			43		54	
			6.0			37		46	
t_{PHL}			2.0			220		275	
			4.5			43		54	
			6.0			37		46	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{E}$ − Q)		2.0			200		250	ns
			4.5			40		50	
			6.0			35		44	
t_{PHL}			2.0			200		250	
			4.5			40		50	
			6.0			35		44	
t_{PHL}	High-level to low-level output propagation time ($\overline{R}$ − Q)		2.0			150		190	ns
			4.5			31		39	
			6.0			26		32	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				27				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

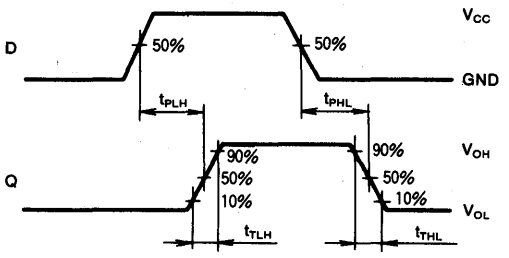
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{E}$, $\overline{R}$ pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
t_{su}	A, D setup time with respect to $\overline{E}$		2.0	100			125		ns
			4.5	20			25		
			6.0	15			19		
t_h	A, D hold time with respect to $\overline{E}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		

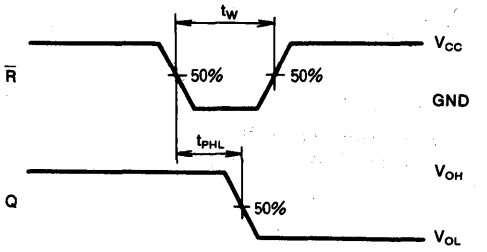
Note 4 : Test Circuit

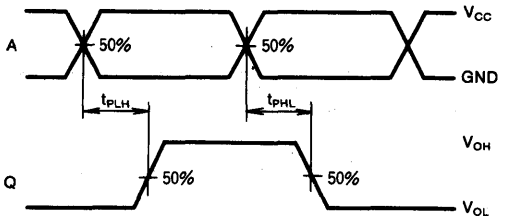


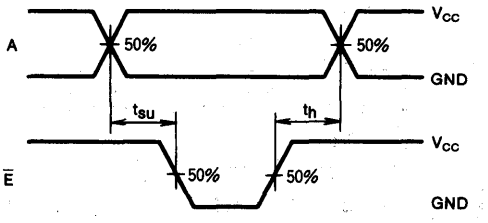
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

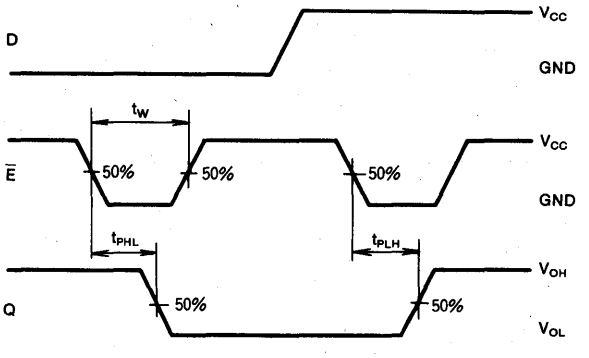
TIMING DIAGRAM

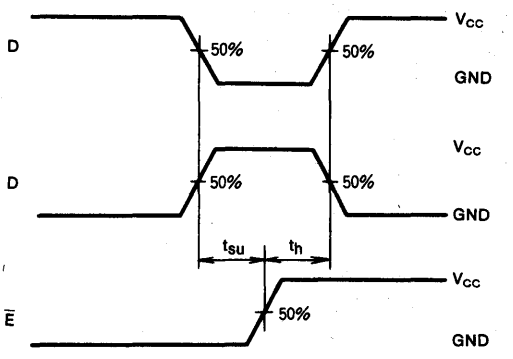












M74HC266P/FP/DP

QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE

DESCRIPTION

The M74HC266 is a semiconductor integrated circuit consisting of four 2-input exclusive NOR gates.

FEATURES

- High-speed: 9ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC266 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS266.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When both inputs A and B are either high or low, the output Y will become high, and when the levels of A and B are opposite, the output Y will become low.

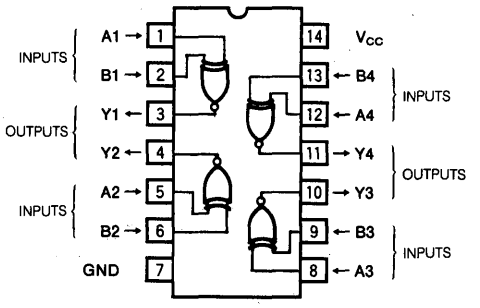
Note that the outputs of M74HC266 and 74LS266 differ in that the outputs of the M74HC266 is not open drain.

This device of some makers is named 74HC7266.

FUNCTION TABLE

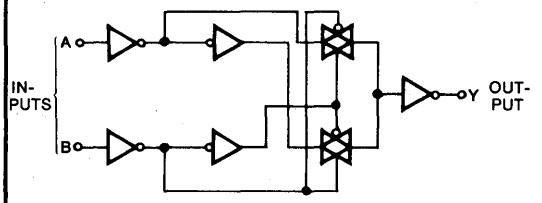
Inputs		Output
A	B	Y
L	L	H
H	L	L
L	H	L
H	H	H

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

LOGIC DIAGRAM (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC266FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC266DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

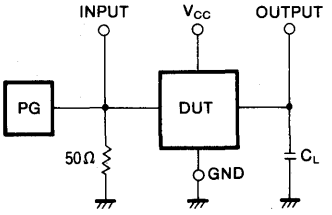
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				20	ns
t_{PHL}					20	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			120		151	ns
			4.5			24		30	
			6.0			20		26	
t_{PHL}			2.0			120		151	ns
			4.5			24		30	
			6.0			20		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				38				pF

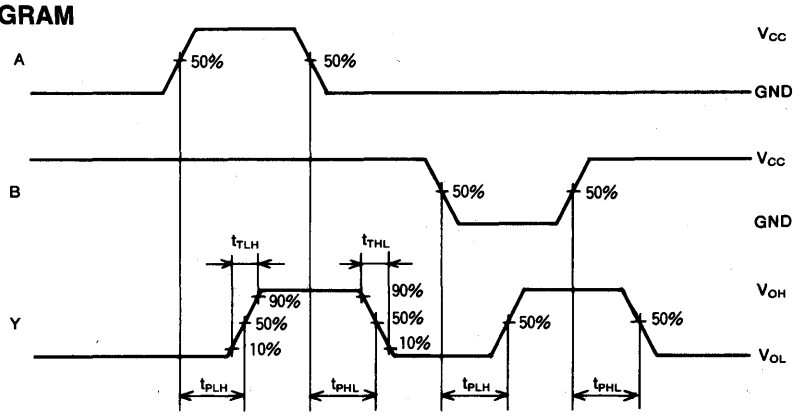
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC266AP/FP/DP

QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE WITH OPEN-DRAIN OUTPUTS

DESCRIPTION

The M74HC266A is a semiconductor integrated circuit consiting of four 2-input exclusive NOR gates with open-drain outputs.

FEATURES

- Open drain outputs
- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

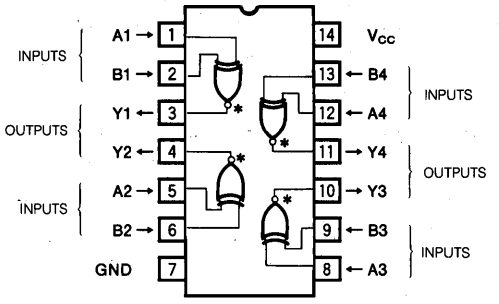
Use of silicon gate technology allows the M74HC266A to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS266.

Open-drain outputs permit a versatile selection of high output impedances by means of externally connected load resistors. This makes "AND ties" a possibility, unlike the case of normal gates.

When both inputs A and B are either high or low, the output Y will become high, and when the levels of A and B are opposite, the output Y will become low.

Note that, unlike 74LS266, voltages higher than V_{CC} must not be applied to the output.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

* : Open-drain output

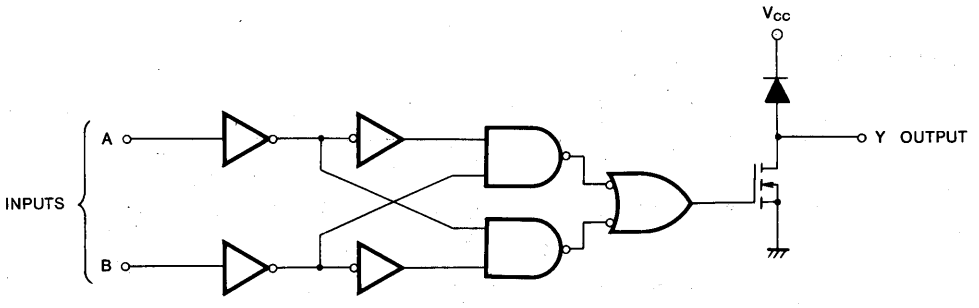
For application requiring normal outputs, another device, the M74HC266 is available with the same functions and pin configuration.

This device of some makers is named 74HC266.

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
H	L	L
L	H	L
H	H	H

LOGIC DIAGRAM (EACH GATE)



MITSUBISHI ELECTRIC

QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE WITH OPEN-DRAIN OUTPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 1 : M74HC266AFP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC266ADP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
					25℃		−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA (Note 3)		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA (Note 3)		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_O	Maximum output leakage current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
		V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{THL}	High-level to low-level output transition time	R_L = 1kΩ C_L = 15pF (Note 3)			10	ns
t_{PLH}	Low-level to high-level and high-level to low-level	R_L = 1kΩ, C_L = 5pF (Note 3)			23	ns
t_{PHL}	output propagation time	R_L = 1kΩ, C_L = 15pF (Note 3)			17	ns

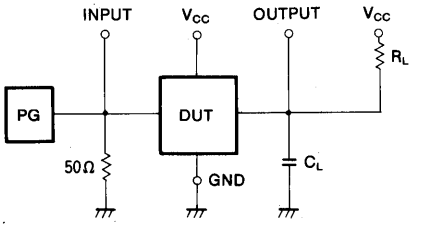
QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE WITH OPEN-DRAIN OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{THL}	High-level to low-level output transition time	R_L = 1kΩ, C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			125		155	ns
			4.5			25		31	
			6.0			23		26	
t_{PHL}			2.0			100		125	ns
			4.5			20		25	
			6.0			17		21	
C_I	Input capacitance					10		10	pF
C_O	Output capacitance	A = B = V_{CC}, GND				10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				16				pF

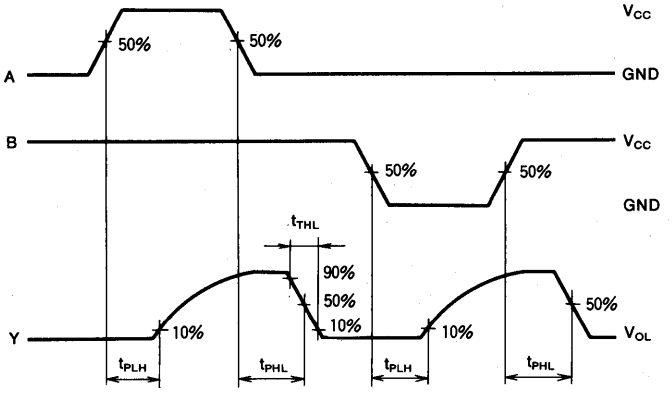
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC273P/FP/DWP

OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

The M74HC273 is a semiconductor integrated circuit consisting of eight positive-edge triggered D-type flip flops with common clock and direct reset inputs.

FEATURES

- High-speed: (clock frequency) 40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

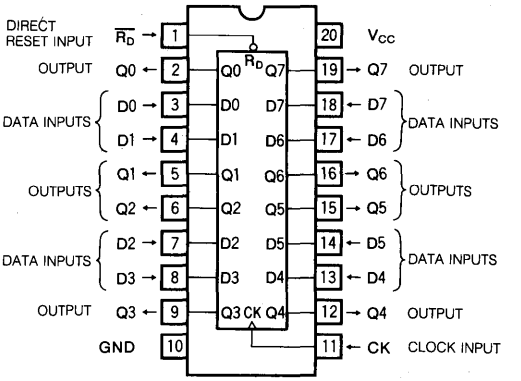
Use of silicon gate technology allows the M74HC273 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS273.

The M74HC273 contains eight edge-triggered D-type flip flops with common direct reset input $\overline{R_D}$ and common clock input CK.

When CK changes from low-level to high-level, the signals just previously input at D appears at output Q in accordance with the function table given.

When $\overline{R_D}$ is low, all outputs Q will become low, irrespective of other inputs. When used as a D-type flip flop, $\overline{R_D}$ should be maintained high.

PIN CONFIGURATION (TOP VIEW)



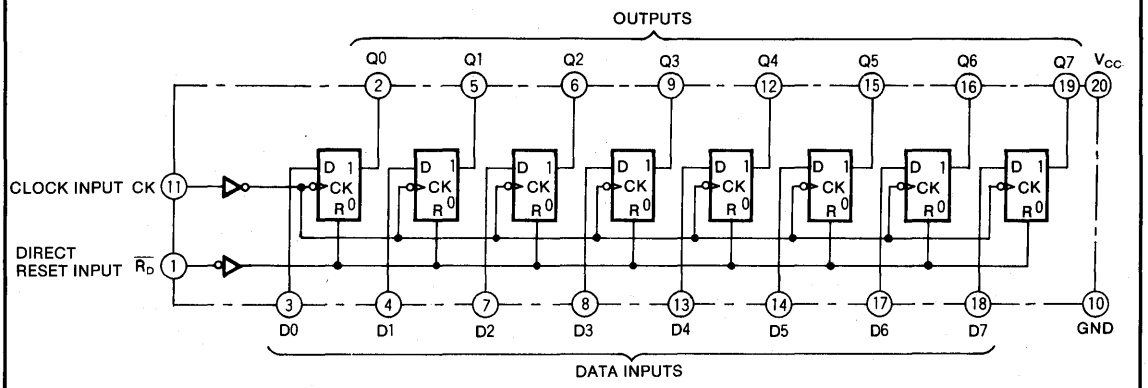
Outline 20P4, 20P2N, 20P2V

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{R_D}$	CK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q^0
H	↓	X	Q^0

Note 1 : ↑ : Change from low to high
↓ : Change from high to low
Q^0 : Output state Q befor clock input changed
X : Irrelevant

LOGIC DIAGRAM



OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC273FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC273DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
					25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				27	ns
t_{PHL}					27	ns
t_{PHL}	High-level and high-level to low-level ($\overline{R_D}$ − Q)				27	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

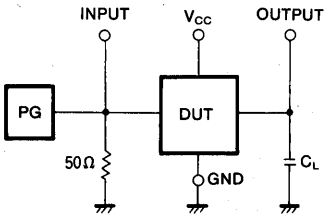
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
t_{PHL}			2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				65				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

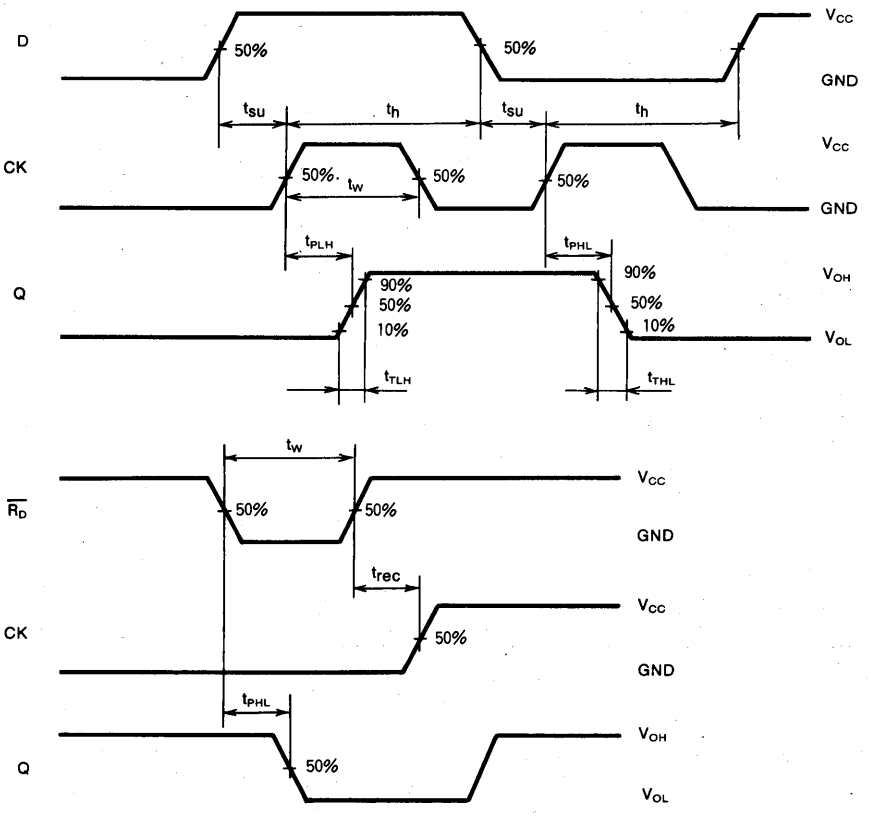
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	D hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{R_D}$ recovery time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC279P/FP/DP

QUADRUPLE R-S LATCH

DESCRIPTION

The M74HC279 is a semiconductor integrated circuit consisting of four R-S flip flops.

FEATURES

- High speed: 15ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC279 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS279.

Two of the 4 circuits have set inputs $\overline{S_1}$ and $\overline{S_2}$ and reset input $\overline{R}$ and the other 2 circuits have set input $\overline{S}$ and reset input $\overline{R}$.

When $\overline{S_1}$ or $\overline{S_2}$ or both are low or $\overline{S}$ is low, the output Q will become high, and when R is low, the output Q will become low. When $\overline{S_1}$ or $\overline{S_2}$ or both are low and $\overline{R}$ is low, the output will become high but when each of the inputs simultaneously become high, the status of Q connot be predetermined.

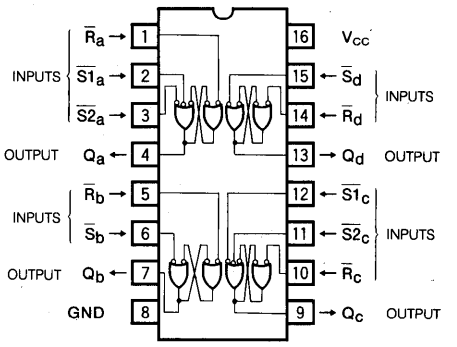
FUNCTION TABLE (Note 1)

Inputs		Output
$\overline{S}$*	$\overline{R}$	Q
H	H	Q^0
H	L	L
L	H	H
L	L	H

Note 1 : Q^0 : Output state Q before input conditions are set

* : When $\overline{S}$ consists of two inputs, H indicates $\overline{S_1}$ and $\overline{S_2}$ are both high, L indicates either $\overline{S_1}$ or $\overline{S_2}$ is low.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

M74HC280P/FP/DP

9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

DESCRIPTION

The M74HC280 is a semiconductor integrated circuit consisting of a 9-bit parity generator/checker.

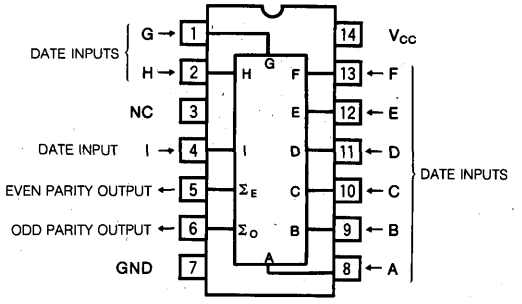
FEATURES

- High-speed: 20ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

NC : NO CONNECTION

FUNCTIONAL DESCRIPTION

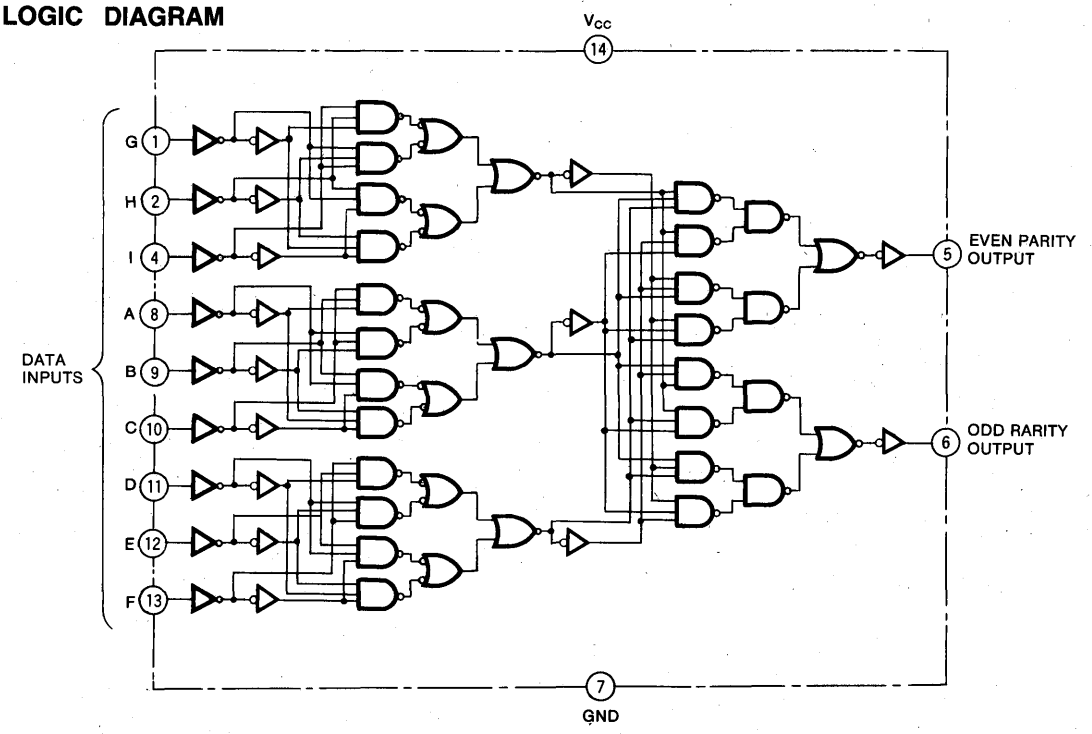
Use of silicon gate technology allows the M74HC280 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS280.

The M74HC280 combines the functions of a 9-bit parity generator and a parity checker. When used as a parity generator, applying 9-bit data to date inputs A through I will result in a generation of parity output to the even parity output or the odd parity output depending upon the number of high values in the data input. See the Function Table for details. When used as a parity checker, one bit from among the 9 bits of data input is used as an odd or even parity designation and the remaining eight bits are used as date.

FUNCTION TABLE

Number of date input high values	EVEN PARITY	ODD PARITY
Even	H	L
Odd	L	H

LOGIC DIAGRAM



9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 1 : M74HC280FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC280DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
				25℃			−40∼+85℃			
			V_{CC}(V)	Min	Typ	Max	Min	Max		
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5			V
			4.5	3.15			3.15			
			6.0	4.2			4.2			
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5		V
			4.5			1.35		1.35		
			6.0			1.8		1.8		
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9			V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

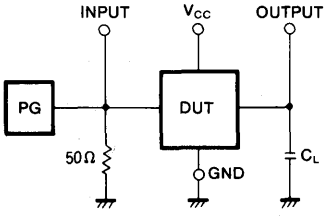
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				35	ns
t_{PHL}					35	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time A~I— EVEN PARITY ODD PARITY		2.0			205		258	ns
			4.5			41		52	
			6.0			35		44	
t_{PHL}			2.0			205		258	ns
			4.5			41		52	
			6.0			35		44	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				92				pF

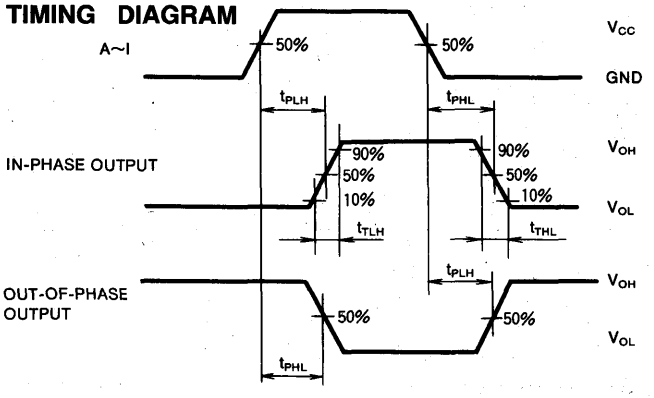
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC283P/FP/DP

4-BIT BINARY FULL ADDER WITH FAST CARRY

DESCRIPTION

The M74HC283 is a semiconductor integrated circuit consisting of a 4-bit full adder.

FEATURES

- High-speed: 30ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

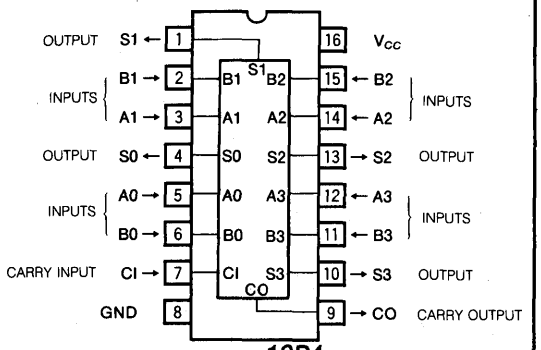
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC283 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS283.

The M74HC283 is a 4-bit binary full adder. When 4-bit binary values applied inputs A0~A3 and B0~B3, and the carry signal from the previous stage is applied to carry input CI, the corresponding sum output for the respective bits will appear at S0~S3 and the carry output will appear at C0.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N
16P2P

FUNCTION TABLE (Note 1)

Inputs			Outputs	
C_{K-1}	A_K	B_K	S_K	C_K
L	L	L	L	L
L	H	L	H	L
L	L	H	H	L
L	H	H	L	H
H	L	L	H	L
H	H	L	L	H
H	L	H	L	H
H	H	H	H	H

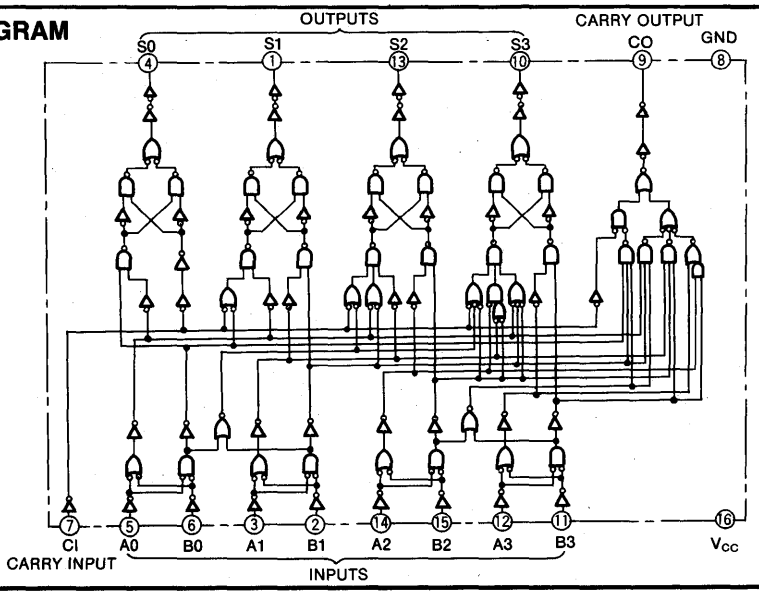
Note 1 : S_K and C_K are sum and carry outputs generated by the sum of addends A_K and B_K and carry input C_{K-1}. Their values are given by the following logical equations.

$S_K = A_K \oplus B_K \oplus C_{K-1}$ ⊕=Exclusive OR

$C_K = A_K \cdot B_K + (A_K + B_K) \cdot C_{K-1}$ +=OR

k=0~3 ·=AND

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC283FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC283DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
					25℃			−40∼+85℃	
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

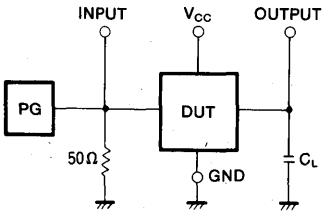
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CI − SK)				38	ns
t_{PHL}					38	
t_{PHL}	Low-level to high-level and high-level to low-level output propagation time (A_K, B_K − S_K)				49	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CI − CO)				31	ns
t_{PHL}					31	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A_K, B_K − CO)				41	ns
t_{PHL}					41	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		90	ns
			4.5			15		18	
			6.0			13		16	
t_{THL}			2.0			75		90	ns
			4.5			15		18	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CI − S_K)		2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PHL}			2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PHL}	high-level to low-level output propagation time (A_K, B_K − S_K)		2.0			270		340	ns
			4.5			54		68	
			6.0			46		58	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CI − CO)		2.0			175		220	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		220	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A_K, B_K − CO)		2.0			225		280	ns
			4.5			45		56	
			6.0			38		48	
t_{PHL}			2.0			225		280	ns
			4.5			45		56	
			6.0			38		48	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

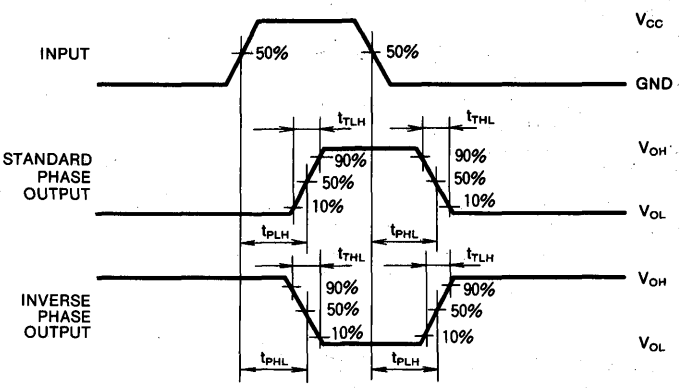
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



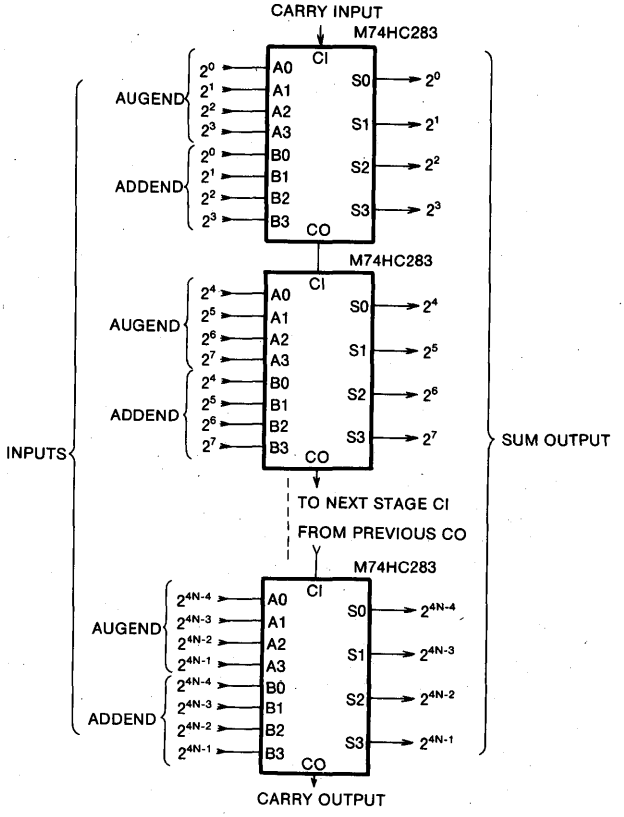
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



APPLICATION EXAMPLE

The 4N-bit binary parallel adder using N pieces of the M74HC283 is shown in the following.



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC298P/FP/DP

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH OUTPUT LATCH

DESCRIPTION

The M74HC298 is a semiconductor integrated circuit consisting of four 2- to 1-line multiplexer with temporary storage and common selector and clock inputs.

FEATURES

- High-speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC298 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS298.

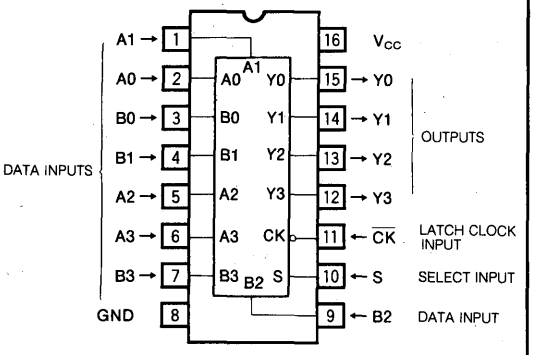
When selector input S is set low, data input B will be selected and when S is set high, data input A will be selected. When latch clock input $\overline{CK}$ changes from high to low level, the selected data will appear at output Y. Since negative-edge trigger D-type flip flops are used for temporary storage, the state of Y is not affected by the state of A or B while $\overline{CK}$ is high or low.

FUNCTION TABLE (Note 1)

Inputs				Output
$\overline{CK}$	S	B	A	Y
↓	L	L	X	L
↓	L	H	X	H
↓	H	X	L	L
↓	H	X	H	H

Note 1 : ↓ : Change from high to low level (negative-edge trigger)
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC299P/FP/DWP

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS

DESCRIPTION

The M74HC299 is a semiconductor integrated circuit consisting of an 8-bit serial/parallel-input, serial/parallel-output shift register with 3-state outputs and a direct reset input.

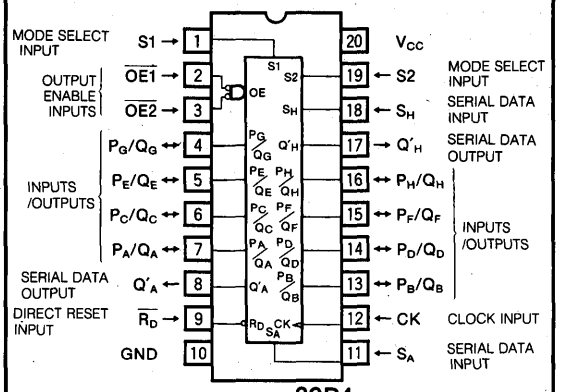
FEATURES

- High-speed: 40MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4 20P2N 20P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC299 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS299.

Use of mode select inputs S1 and S2 allows the device to operate in the following modes.

(1) Parallel read S1="H" S2="H"
(2) Right shift S1="H" S2="L"
(3) Left shift S1="L" S2="H"
(4) Clock inhibit S1="L" S2="L"

In the parallel data-read mode, 8-bit parallel data applied at parallel I/O pins P_A/Q_A~P_H/Q_H will be stored in the flip flops when clock input CK changes from low-level to high-level.

In the right-shift mode, serial data applied at serial data input S_A will be right-shifted from P_A/Q_A to P_H/Q_H by one bit each time the clock input CK changes from low-level to high-level.

In the left-shift mode, serial data applied at serial data input S_H will be left-shifted from P_H/Q_H to P_A/Q_A by one bit each time the clock input CK changes from low-level to high-level.

In the clock inhibit mode, the clock pulse input is suppressed at each flip flop and the state of flip flop will not change and the previous states of the flip flops will be maintained. When $\overline{OE1}$ or $\overline{OE2}$ is high, P_A~P_H will become high-impedance state Z. Changing $\overline{OE1}$ or $\overline{OE2}$ will not affect the contents of the flip flops.

When direct reset input $\overline{R_D}$ is low, each flip flop will be reset low, irrespective of other inputs.

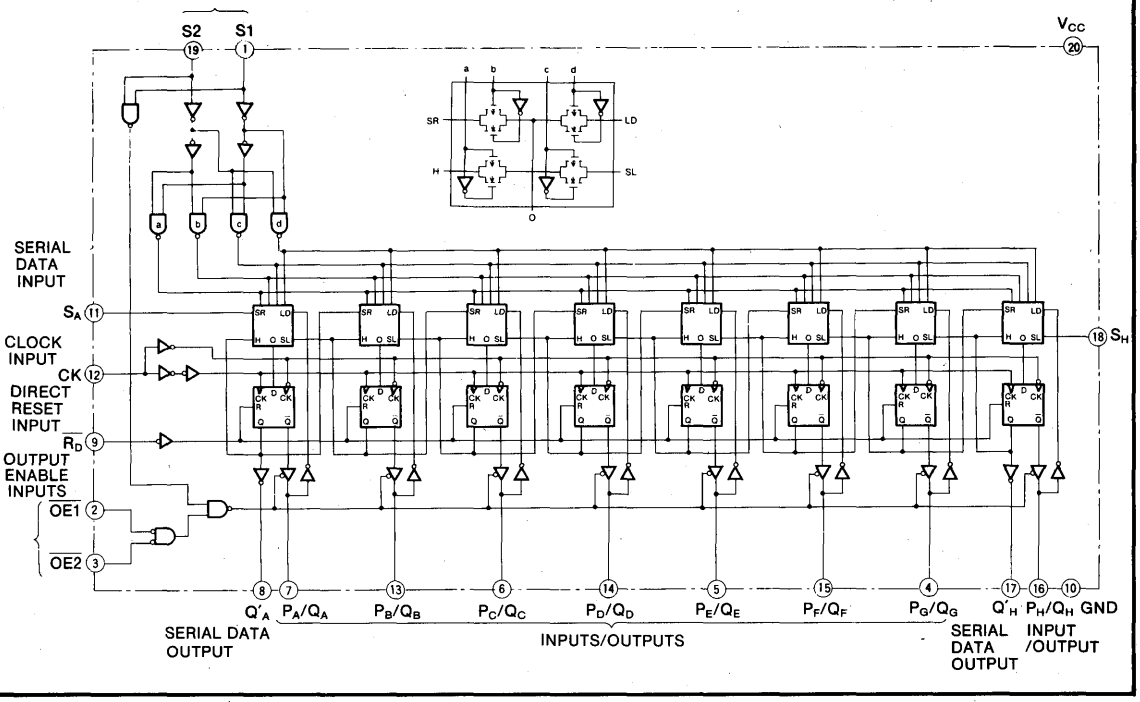
Serial data outputs Q'_A and Q'_H are used to extend the number of bits.

See Application Example.

MITSUBISHI ELECTRIC

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Operation mode	Inputs								Parallel data I/O								Serial data outputs	
	$\overline{R_D}$	CK	S1	S2	S_A	S_H	$\overline{OE1}$	$\overline{OE2}$	P_A/Q_A	P_B/Q_B	P_C/Q_C	P_D/Q_D	P_E/Q_E	P_F/Q_F	P_G/Q_G	P_H/Q_H	Q'_A	Q'_H
Direct reset	L	X	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L
	L	X	X	L	X	X	L	L	L	L	L	L	L	L	L	L	L	L
Righ shift	H	↑	H	L	L	X	L	L	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	L	Q_G^0
	H	↑	H	L	H	X	L	L	H	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	H	Q_G^0
Left shift	H	↑	L	H	X	L	L	L	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	L	Q_B^0	L
	H	↑	L	H	X	H	L	L	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	H	Q_B^0	H
Parallel read	H	↑	H	H	X	X	L	L	P_A	P_B	P_C	P_D	P_E	P_F	P_G	P_H	P_A	P_H
Clock inhibit	H	X	L	L	X	X	L	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	Q_A^0	Q_H^0
	H	L	X	X	X	X	L	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	Q_A^0	Q_H^0
Output disable	X	X	X	X	X	X	H	L	Z	Z	Z	Z	Z	Z	Z	Z	Q_A^0	Q_H^0
(P_A/Q_A~P_H/Q_H are the high -impedance state.)	X	X	X	X	X	X	L	H	Z	Z	Z	Z	Z	Z	Z	Z	Q_A^0	Q_H^0
	X	X	X	X	X	X	H	H	Z	Z	Z	Z	Z	Z	Z	Z	Q_A^0	Q_H^0

Note 1 : Qn^0: Output state before input condisions are set.
X : Irrelevant
↑ : Change from low to high level (positive-edge trigger)
Pn : P_A/Q_A~P_H/Q_H operate as inputs. Q'_A and Q'_H are in the same state as P_A and P_H, respectively.
Z : High-impedance state. The flip flops are held in the same state as before P_A/Q_A~P_H/Q_H become the high-impedance state.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current (Q_A∼Q_H)		±35	mA
I_O	Output currents (Q'_A∼Q'_H)		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC299FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −6mW/℃.
M74HC299DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
	High-level output voltnge (P_A/Q_A～P_H/Q_H)	V_I = V_{IH}, V_{IL}	I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
	high-level output voltnge (Q'_A, Q'_H)	V_I = V_{IH}, V_{IL}	I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
	Low-level output voltnge (P_A/Q_A～P_H/Q_H)	V_I = V_{IH}, V_{IL}	I_{OL} = 6.0mA	4.5		0.26		0.33	
			I_{OL} = 7.8mA	6.0		0.26		0.33	
	Low-level output voltnge (Q'_A, Q'_H)	V_I = V_{IH}, V_{IL}	I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0		−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0		0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0		−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND; I_O = 0μA		6.0		4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	25			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q'_A, Q'_H)				35	ns
t_{PHL}					35	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q'_A, Q'_H)				40	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q_A～Q_H)				35	ns
t_{PHL}					35	ns
t_{PLH}	High-level to low-level output propagation time ($\overline{R_D}$ − Q_A～Q_H)				40	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q_A～Q_H)	C_L = 5pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q_A～Q_H)	C_L = 50pF (Note 4)			35	ns
t_{PZH}					35	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	25			20		
			6.0	29			23		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($CK - Q'_A$, Q'_H)		2.0			170		210	ns
			4.5			38		48	
			6.0			35		44	
t_{PHL}			2.0			170		210	ns
			4.5			38		48	
			6.0			35		44	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D} - Q'_A$, Q'_H)		2.0			200		250	ns
			4.5			44		55	
			6.0			38		46	
t_{PHL}	Low-level to high-level and high-level to low-level output propagation time ($CK - Q_A \sim Q_H$)		2.0			170		210	ns
			4.5			38		48	
			6.0			35		44	
t_{PHL}			2.0			170		210	ns
			4.5			38		48	
			6.0			35		44	
t_{PLH}		C_L = 150pF (Note 4)	2.0			206		260	ns
			4.5			46		57	
			6.0			39		49	
t_{PHL}			2.0			206		260	ns
			4.5			46		57	
			6.0			39		49	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D} - Q_A \sim Q_H$)	C_L = 50pF (Note 4)	2.0			200		250	ns
			4.5			44		55	
			6.0			38		46	
		C_L = 150pF (Note 4)	2.0			236		295	ns
			4.5			52		65	
			6.0			46		57	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE} - Q_A \sim Q_H$)	C_L = 50pF (Note 4)	2.0			160		200	ns
			4.5			32		40	
			6.0			28		34	
t_{PHZ}			2.0			160		200	ns
			4.5			33		40	
			6.0			28		34	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE} - Q_A \sim Q_H$)		2.0			160		200	ns
			4.5			32		40	
			6.0			28		34	
t_{PZH}			2.0			160		200	ns
			4.5			32		40	
			6.0			28		34	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃) (Continued)

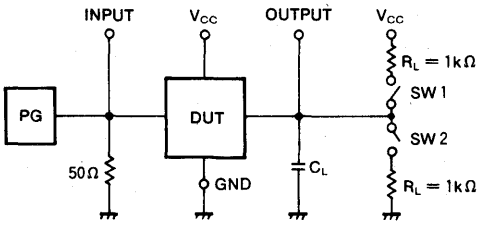
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q_A, Q_H)	C_L = 150pF (Note 4)	2.0			220		275	ns
			4.5			44		55	
			6.0			37		47	
t_{PZH}			2.0			220		275	ns
			4.5			44		55	
			6.0			37		47	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	OE=V_{CC}							pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{R_D}$ pulse width		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_{su}	S_A, S_H setup time with respect to CK		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	S_A, S_H hold time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		
t_{rec}	$\overline{R_D}$ recovery time with respect to CK		2.0	10			10		ns
			4.5	10			10		
			6.0	10			10		

Note 4 : Test Circuit

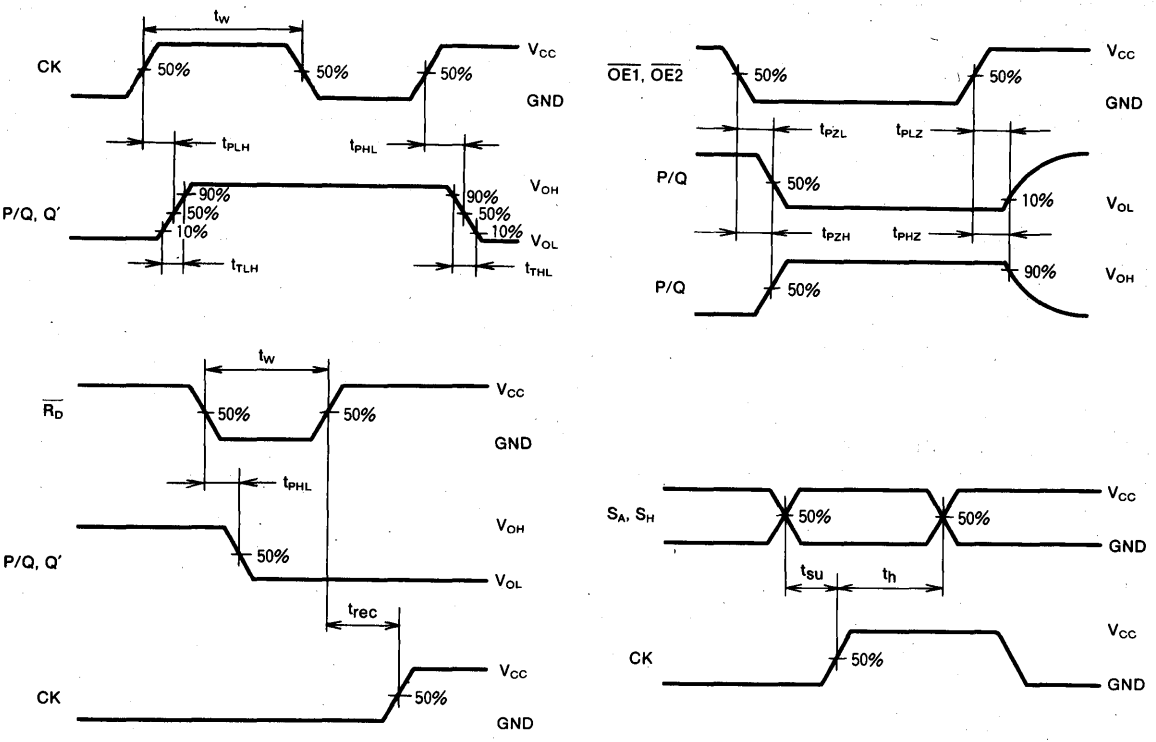


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS

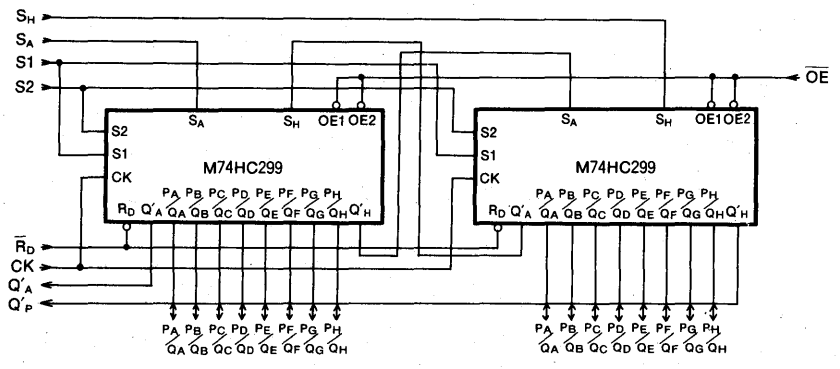
TIMING DIAGRAM



APPLICATION EXEAMPLE

The following is an example of a 16-bit shift register using two M74HC299s.

In the same way, by using N ICs, 8N-bit shift register is configured.



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC323P/FP/DWP

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS

DESCRIPTION

The M74HC323 is a semiconductor integrated circuit consisting of an 8-bit serial/parallel-input, serial/parallel-output shift register with 3-state outputs and a synchronous reset input.

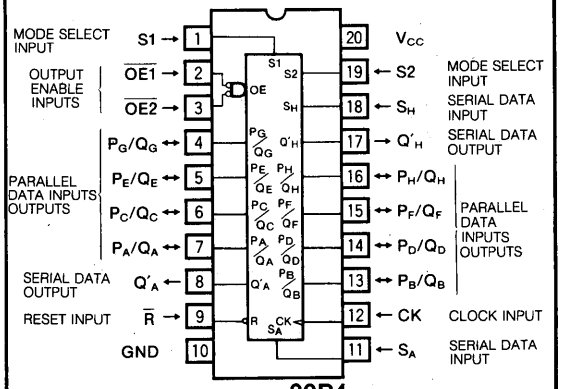
FEATURES

- High speed: 40MHz clock frequency typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC323 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS323.

Use of mode select inputs S1 and S2 allows the device to operate in the following modes.

(1) Parallel read S1="H" S2="H"
(2) Right shift S1="H" S2="L"
(3) Left shift S1="L" S2="H"
(4) Clock inhibit S1="L" S2="L"

In the parallel data-read mode, 8-bit parallel data applied at parallel data I/O pins P_A/Q_A~P_H/Q_H will be stored in the flip flops when the clock input CK changes from low-level to high-level. In the right-shift mode, serial data applied at serial data input S_A will be right-shifted from P_A/Q_A to P_H/Q_H by one bit each time the clock input CK changes from low-level to high-level. In the left-shift mode, serial data applied at serial data input S_H will be left-shifted from P_H/Q_H to P_A/Q_A by one bit each time the clock input CK changes from low-level tb high-level.

In the clock inhibit mode, the clock pulse input is suppressed at each flip flop and the state of flip flop will not change and the previous states of the flip flops will be maintained. When $\overline{OE1}$ or $\overline{OE2}$ is high, P_A/Q_A~P_H/Q_H will become the high-impedance state Z. Changing $\overline{OE1}$ or $\overline{OE2}$ will not affect the contents of the flip flops.

When reset input $\overline{R}$ is low and CK changes from low-level to high-level, all flip flops will become low.

Serial data output Q'_A and Q'_H are used to extend the number of bits.

FUNCTION TABLE (Note 1)

Operation mode	Inputs								Parallel data I/O								Serial data outputs	
	$\overline{R}$	CK	S1	S2	S_A	S_H	$\overline{OE1}$	$\overline{OE2}$	P_A/Q_A	P_B/Q_B	P_C/Q_C	P_D/Q_D	P_E/Q_E	P_F/Q_F	P_G/Q_G	P_H/Q_H	Q'_A	Q'_H
Reset	L	↑	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L
	L	↑	X	L	X	X	L	L	L	L	L	L	L	L	L	L	L	L
Right shift	H	↑	H	L	L	X	L	L	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	L	Q_G^0
	H	↑	H	L	H	X	L	L	H	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	H	Q_G^0
Left shift	H	↑	L	H	X	L	L	L	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	L	Q_B^0	L
	H	↑	L	H	X	H	L	L	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	H	Q_B^0	H
Parallel read	H	↑	H	H	X	X	L	L	P_A	P_B	P_C	P_D	P_E	P_F	P_G	P_H	P_A	P_H
Clock inhibit	H	X	L	L	X	X	L	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	Q_A^0	Q_H^0
	H	L	X	X	X	X	L	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	Q_A^0	Q_H^0
Output disable	X	X	X	X	X	X	H	L	Z	Z	Z	Z	Z	Z	Z	Z	Q_A^0	Q_H^0
(P_A/Q_A~P_H/Q_H are the high-impedance state.)	X	X	X	X	X	X	L	H	Z	Z	Z	Z	Z	Z	Z	Z	Q_A^0	Q_H^0
	X	X	X	X	X	X	H	H	Z	Z	Z	Z	Z	Z	Z	Z	Q_A^0	Q_H^0

Note 1 : Qn^0: Output state before input conditions are set.
X : Irrelevant
↑ : Change from low to high-level (positive-edge trigger)
Pn : P_A/Q_A~P_H/Q_H operate as inputs. Q'_A and Q'_H are in the same state as P_A and P_H.
Z : High-impedance state. The flip flops are held in the same state as before P_A/Q_A~P_H/Q_H become the high-impedance state.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC354P/FP/DWP

8-INPUT DATA SELECTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC354 is a semiconductor integrated circuit consisting of an 8-line to 1-line date selector/multiplexer with 3-state outputs.

FEATURES

- High-speed: 32ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃
- 3-state outputs

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC354 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS354.

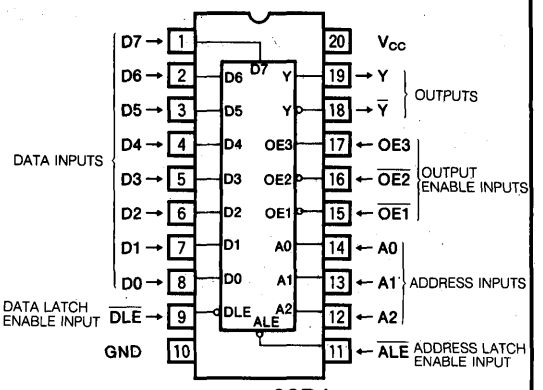
The M74HC354 consists of a circuit containing data selector function for selecting one of eight input line signals and multiplexer function for converting 8-bit parallel date into serial data using time-division.

The 8-line signals are applied to data inputs D0 through D7, and after one of the data inputs has been selected by address input A0, A1 and A2, it is output at pin Y, and the inverted signal is output at pin $\overline{Y}$.

By applying 8-bit parallel data to D0 through D7, and connecting the output of an octal synchronous counter to A0, A1 and A2, parallel data will be output at Y synchronous with the clock pulse in the order D0 through D7.

When the data latach-eanble input $\overline{DLE}$ is low, the input data is stored in the data latch. When address latch-enable input $\overline{ALE}$ is low, the address data is stored in the address latch. When the output-enable input $\overline{OE1}$, $\overline{OE2}$ is high or OE3 is low, then Y and $\overline{Y}$ will become high impedance state, irrespective of other inputs.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

FUNCTION TABLE (Note 1)

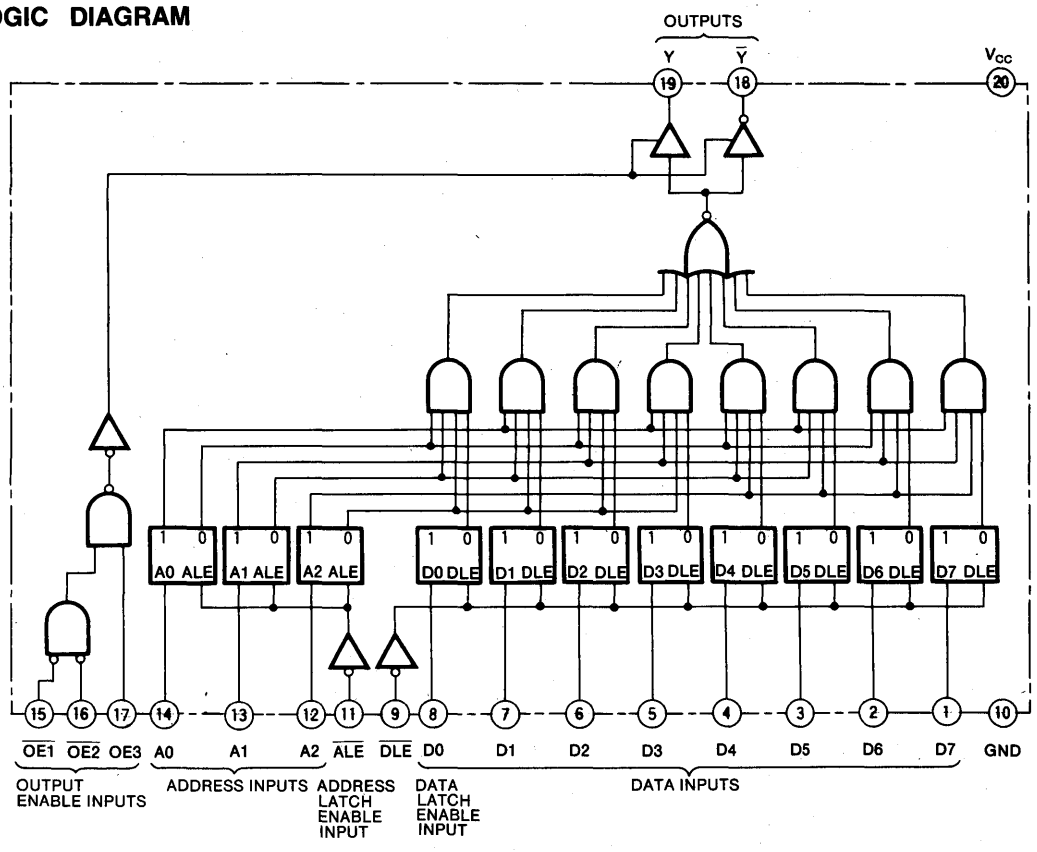
Inputs							Outputs	
A2	A1	A0	$\overline{DLE}$	$\overline{OE1}$	$\overline{OE2}$	OE3	Y	$\overline{Y}$
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	H	L	L	H	D0	$\overline{D0}$
L	L	H	H	L	L	H	D1	$\overline{D1}$
L	H	L	H	L	L	H	D2	$\overline{D2}$
L	H	H	H	L	L	H	D3	$\overline{D3}$
H	L	L	H	L	L	H	D4	$\overline{D4}$
H	L	H	H	L	L	H	D5	$\overline{D5}$
H	H	L	H	L	L	H	D6	$\overline{D6}$
H	H	H	H	L	L	H	D7	$\overline{D7}$
L	L	L	L	L	L	H	D0n	$\overline{D0n}$
L	L	H	L	L	L	H	D1n	$\overline{D1n}$
L	H	L	L	L	L	H	D2n	$\overline{D2n}$
L	H	H	L	L	L	H	D3n	$\overline{D3n}$
H	L	L	L	L	L	H	D4n	$\overline{D4n}$
H	L	H	L	L	L	H	D5n	$\overline{D5n}$
H	H	L	L	L	L	H	D6n	$\overline{D6n}$
H	H	H	L	L	L	H	D7n	$\overline{D7n}$

Note 1 : X : Irrelevant
Z : High impedance
D0n~D7n: Data inputs before $\overline{DLE}$ is changed to low

MITSUBISHI ELECTRIC

8-INPUT DATA SELECTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC354FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC354DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

8-INPUT DATA SELECTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
				25℃			−40∼+85℃			
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-leveloutput current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				46	ns
t_{PHL}	output propagation time (D − Y, $\overline{Y}$)				46	ns
t_{PLH}	Low-level to high-level and high-level to low-level				53	ns
t_{PHL}	output propagation time ($\overline{DLE}$ − Y, $\overline{Y}$)				53	ns
t_{PLH}	Low-level to high-level and high-level to low-level				56	ns
t_{PHL}	output propagation time (A − Y, $\overline{Y}$)				56	ns
t_{PLH}	Low-level to high-level and high-level to low-level				58	ns
t_{PHL}	output propagation time ($\overline{ALE}$ − Y, $\overline{Y}$)				58	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 4)			32	ns
t_{PHZ}	(OE, $\overline{OE}$ − Y, $\overline{Y}$)				32	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 4)			24	ns
t_{PZH}	(OE, $\overline{OE}$ − Y, $\overline{Y}$)				24	ns

8-INPUT DATA SELECTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Y, $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			235		294	ns
			4.5			47		59	
			6.0			40		50	
t_{PHL}			2.0			235		294	ns
			4.5			47		59	
			6.0			40		50	
t_{PLH}		C_L = 150pF (Note 4)	2.0			275		344	ns
			4.5			55		68	
			6.0			46		58	
t_{PHL}			2.0			275		344	ns
			4.5			55		68	
			6.0			46		58	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{DLE}$ − Y, $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			270		337	ns
			4.5			54		68	
			6.0			46		58	
t_{PHL}			2.0			270		337	ns
			4.5			54		68	
			6.0			46		58	
t_{PLH}		C_L = 150pF (Note 4)	2.0			310		387	ns
			4.5			62		78	
			6.0			52		66	
t_{PHL}			2.0			310		357	ns
			4.5			62		78	
			6.0			52		66	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y, $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			285		356	ns
			4.5			57		71	
			6.0			48		60	
t_{PHL}			2.0			285		356	ns
			4.5			57		71	
			6.0			48		60	
t_{PLH}		C_L = 150pF (Note 4)	2.0			325		406	ns
			4.5			65		81	
			6.0			55		69	
t_{PHL}			2.0			325		406	ns
			4.5			65		81	
			6.0			55		69	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{ALE}$ − Y, $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			300		375	ns
			4.5			60		75	
			6.0			51		64	
t_{PHL}			2.0			300		375	ns
			4.5			60		75	
			6.0			51		64	
t_{PLH}		C_L = 150pF (Note 4)	2.0			340		425	ns
			4.5			68		85	
			6.0			58		72	
t_{PHL}			2.0			340		425	ns
			4.5			68		85	
			6.0			58		72	

8-INPUT DATA SELECTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃) (Continued)

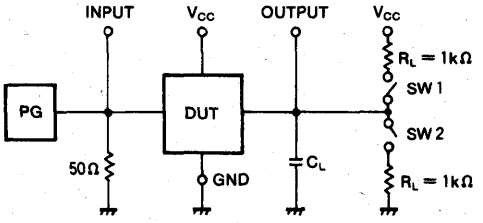
Symbol	Parameter	Test conditions	Limits					Unit
				25℃			−40~+85℃	
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{PLZ}	Output disable time from low-level and high-level (OE, $\overline{OE}$ − Y, $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			165		206	ns
			4.5			33		40	
			6.0			28		35	
t_{PHZ}			2.0			165		206	ns
			4.5			33		40	
			6.0			28		35	
t_{PZL}	Output enable time to low-level and high-level (OE, $\overline{OE}$ − Y, $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
t_{PZH}			2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
t_{PZL}		C_L = 150pF (Note 4)	2.0			165		206	ns
			4.5			33		41	
			6.0			28		35	
t_{PZH}			2.0			165		206	ns
			4.5			33		41	
			6.0			28		35	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = "H"				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
				25℃			−40~+85℃	
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Address latch enable pulse width Data latch enable pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	15			18		
t_{su}	D setup time with respect to $\overline{DLE}$ A setup time with respect to $\overline{ALE}$		2.0	50			60		ns
			4.5	10			13		
			6.0	10			13		
t_h	$\overline{DLE}$ hold time with respect to D $\overline{ALE}$ hold time with respect to A		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

Note 4 : Test Circuit

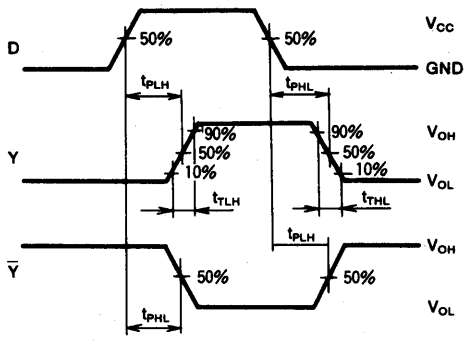


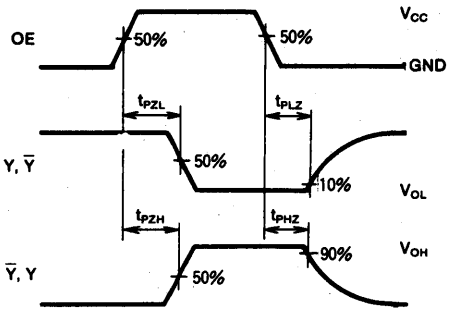
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

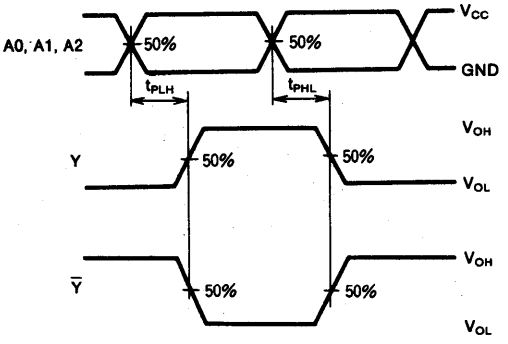
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

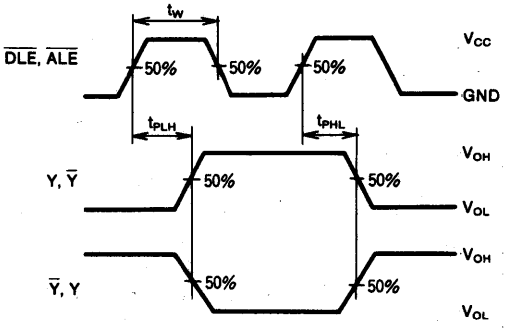
8-INPUT DATA SELECTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

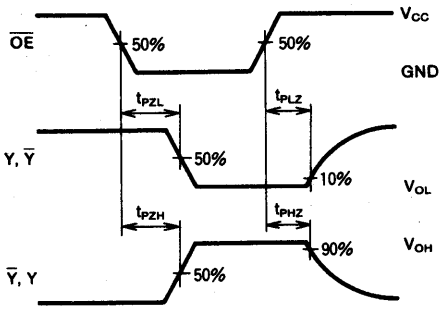
TIMING DIAGRAM

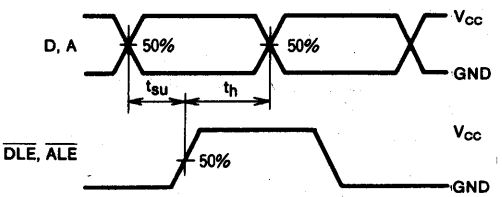












PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC356P/FP/DWP

8-INPUT DATA SELCTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC356 is a semiconductor integrated circuit consisting of an 8-line to 1line data selector/multiplexer with 3-state outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 35ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃
- 3-state outputs

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC356 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS356.

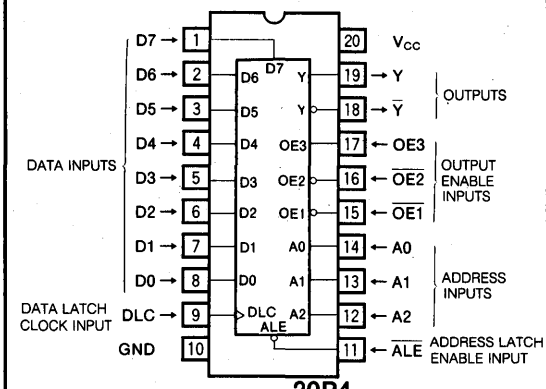
The M74HC356 consists of a circuit containing data selector function for selecting one of eight input line signals and multiplexer function for converting 8-bit parallel data into serial data using time-division.

The 8-line signals are applied to data inputs D0 and D7, and after one of the data inputs has been selected by address input A0, A1 and A2, it is output at pin Y, and the inverted signal is output at pin $\overline{Y}$.

By applying 8-bit parallel data to D0 through D7, and connecting the output of an octal synchronous counter to A0, A1 and A2, parallel data will be output at Y synchronous with the clock pulse in the order D0 through D7.

D0 through D7 all contain edge-triggered flip flops. Input data is sent to the data latch by the rising edge of data latch clock DLC. The address data is stored in the address latch when the address latch enable input $\overline{ALE}$ is low. When the output enable input $\overline{OE1}$, $\overline{OE2}$ is high or OE3 is low then Y and $\overline{Y}$ will become high impedance state irrespective of other inputs.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

FUNCTION TABLE (Note 1)

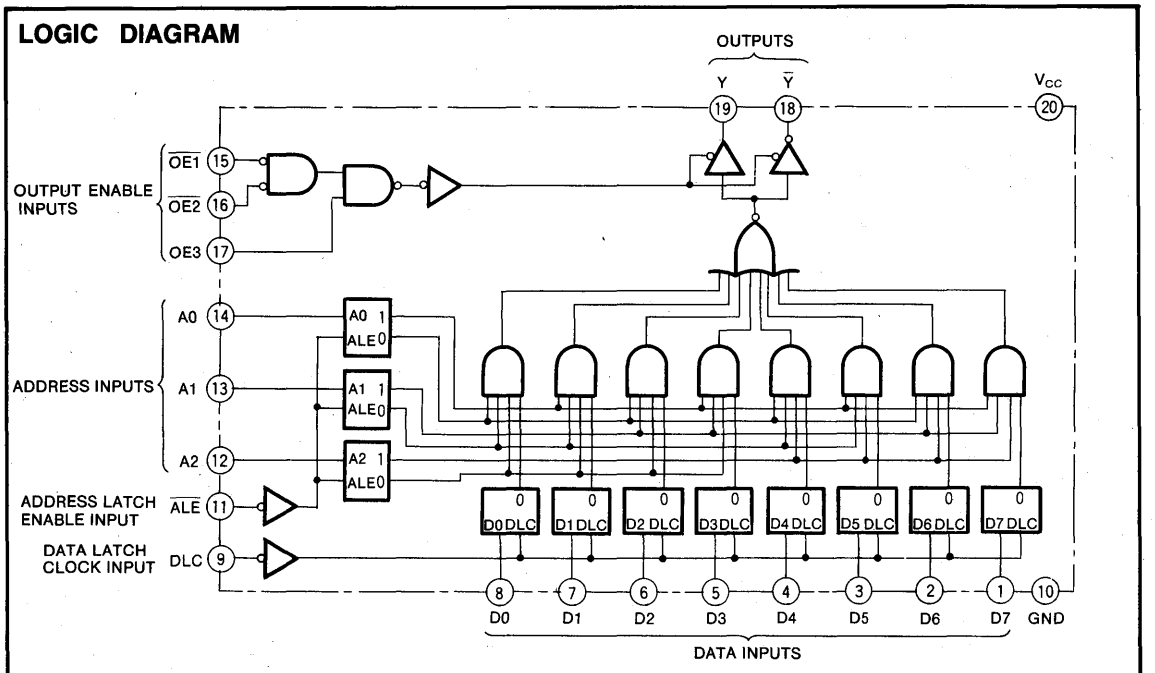
Inputs							Outputs	
A2	A1	A0	DLC	$\overline{OE1}$	$\overline{OE2}$	OE3	Y	$\overline{Y}$
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	D0n	$\overline{D0n}$
L	L	H	↑	L	L	H	D1n	$\overline{D1n}$
L	H	L	↑	L	L	H	D2n	$\overline{D2n}$
L	H	H	↑	L	L	H	D3n	$\overline{D3n}$
H	L	L	↑	L	L	H	D4n	$\overline{D4n}$
H	L	H	↑	L	L	H	D5n	$\overline{D5n}$
H	H	L	↑	L	L	H	D6n	$\overline{D6n}$
H	H	H	↑	L	L	H	D7n	$\overline{D7n}$
L	L	L	X	L	L	H	D0p	$\overline{D0p}$
L	L	H	X	L	L	H	D1p	$\overline{D1p}$
L	H	L	X	L	L	H	D2p	$\overline{D2p}$
L	H	H	X	L	L	H	D3p	$\overline{D3p}$
H	L	L	X	L	L	H	D4p	$\overline{D4p}$
H	L	H	X	L	L	H	D5p	$\overline{D5p}$
H	H	L	X	L	L	H	D6p	$\overline{D6p}$
H	H	H	X	L	L	H	D7p	$\overline{D7p}$

Note 1 : X : Irrelevant
Z : High impedance
Dn : Each data input D at the rise of DLC
Dp : Each data input D at the rise of previous DLC

MITSUBISHI ELECTRIC

8-INPUT DATA SELCTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC356FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC356DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

8-INPUT DATA SELCTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 6.0mA	4.5		0.26		0.33	
			I_{OL} = 7.8mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0		−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0		0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0		−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0		4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				50	ns
t_{PHL}	output propagation time (DLC − Y, $\overline{Y}$)				50	ns
t_{PLH}	Low-level to high-level and high-level to low-level				56	ns
t_{PHL}	output propagation time (A − Y, $\overline{Y}$)				56	ns
t_{PLH}	Low-level to high-level and high-level to low-level				58	ns
t_{PHL}	output propagation time ($\overline{ALE}$ − Y, $\overline{Y}$)				58	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 4)			32	ns
t_{PHZ}	(OE, $\overline{OE}$ − Y, $\overline{Y}$)				32	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 4)			24	ns
t_{PZH}	(OE, $\overline{OE}$ − Y, $\overline{Y}$)				24	ns

8-INPUT DATA SELCTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Output disable time from low-level and high-level (DLC − Y, $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			225		318	ns
			4.5			51		63	
			6.0			43		53	
t_{PHL}			2.0			225		318	ns
			4.5			51		63	
			6.0			43		53	
t_{PLH}		C_L = 150pF (Note 4)	2.0			295		369	ns
			4.5			59		73	
			6.0			50		63	
t_{PHL}			2.0			295		369	ns
			4.5			59		73	
			6.0			50		63	
t_{PLH}	Output enable time to low-level and high-level (A − Y, $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			285		356	ns
			4.5			57		71	
			6.0			48		60	
t_{PHL}			2.0			235		356	ns
			4.5			57		71	
			6.0			48		60	
t_{PLH}		C_L = 150pF (Note 4)	2.0			325		406	ns
			4.5			65		81	
			6.0			55		69	
t_{PHL}			2.0			325		406	ns
			4.5			65		81	
			6.0			55		69	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{ALE}$ − Y, $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			300		375	ns
			4.5			60		75	
			6.0			51		64	
t_{PHL}			2.0			300		375	ns
			4.5			60		75	
			6.0			51		64	
t_{PLH}		C_L = 150pF (Note 4)	2.0			340		425	ns
			4.5			68		85	
			6.0			58		72	
t_{PHL}			2.0			340		425	ns
			4.5			68		85	
			6.0			58		72	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$, OE − Y, $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			165		206	ns
			4.5			33		41	
			6.0			28		35	
t_{PHZ}			2.0			165		206	ns
			4.5			33		41	
			6.0			28		35	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃) (Continue)

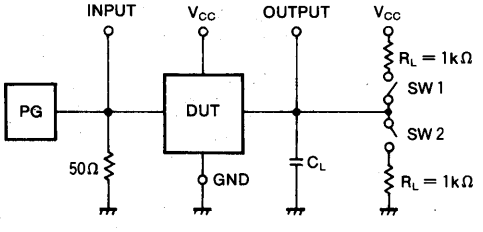
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$, $\overline{OE}$ − Y, $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
t_{PZH}			2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
t_{PZL}		C_L = 150pF (Note 4)	2.0			165		206	ns
			4.5			33		41	
			6.0			28		35	
t_{PZH}			2.0			165		206	ns
			4.5			33		41	
			6.0			28		35	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Address latch enable pulse width Data latch clock pulse width	2.0	80			100		ns
		4.5	16			20		
		6.0	15			18		
t_{su}	D setup time with respect to DLC A setup time with respect to $\overline{ALE}$	2.0	50			50		ns
		4.5	10			10		
		6.0	10			10		
t_h	DLC hold time with respect to D $\overline{ALE}$ hold time with respect to A	2.0	5			5		ns
		4.5	5			5		
		6.0	5			5		

Note 4 : Test Circuit

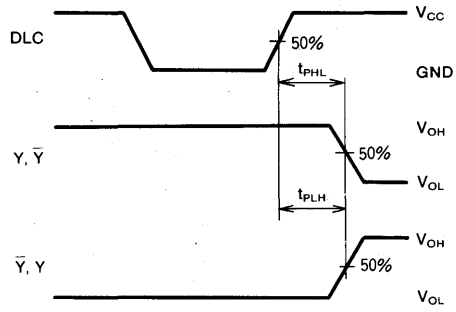


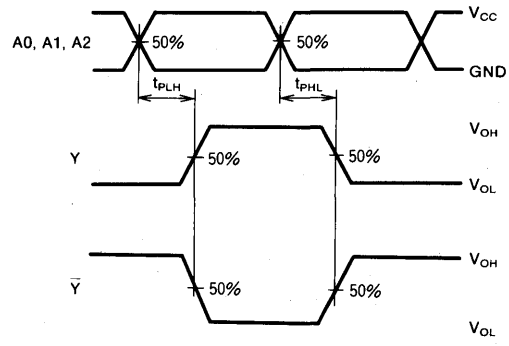
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

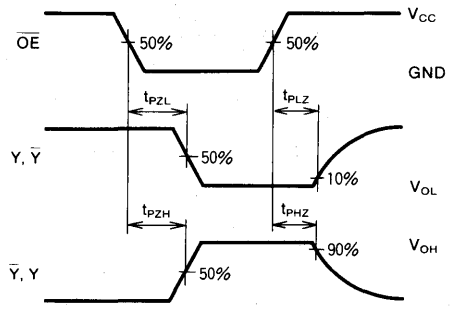
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

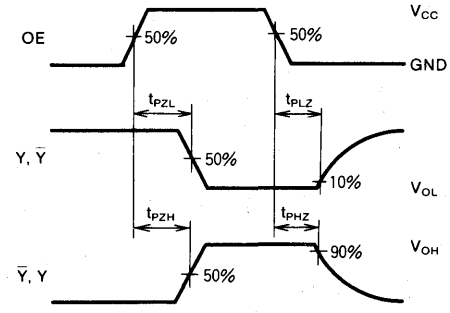
8-INPUT DATA SELCTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

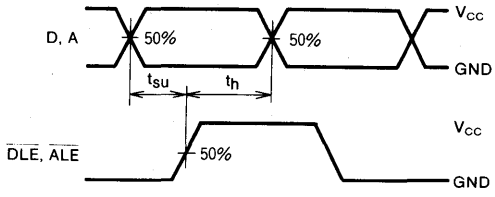
TIMING DIAGRAM

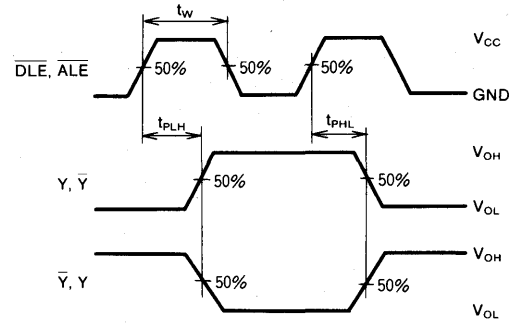












M74HC365P/FP/DP

HEX 3-STATE NONINVERTING BUFFER WITH COMMON ENABLES

DESCRIPTION

The M74HC365 is a semiconductor integrated circuit consisting of six buffers with 3-state noninverted outputs and common enable inputs.

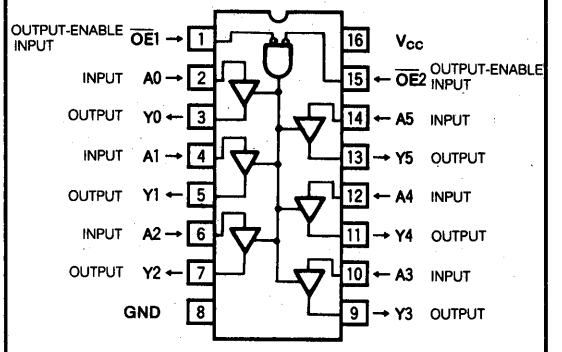
FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC365 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS365.

The M74HC365 consists of six 3-state buffers with output-enable inputs common to all circuits.

When output-enable inputs $\overline{OE1}$ and $\overline{OE2}$ are both low, outputs Y will become enable state. If input A is high, a high-level signal will be output to Y and if input A is low, a low-level signale will be output to Y.

When at least one of input $\overline{OE1}$ or $\overline{OE2}$ is high, Y will become high-impedance state.

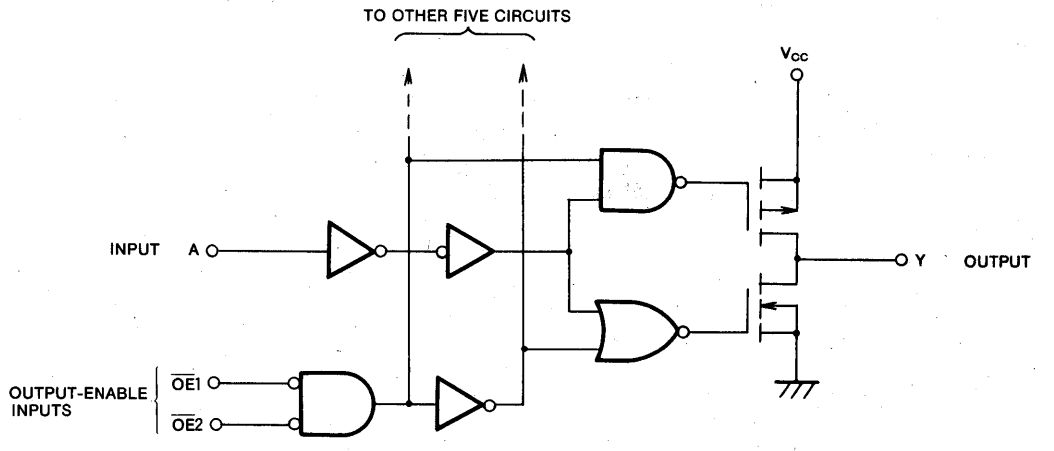
A version of the M74HC356 with an inverted output, the M74HC366, is also available.

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Note 1 : X : Irrelevant
Z : High impedance

LOGIC DIAGRAM (EACH BUFFER)



HEX 3-STATE NONINVERTING BUFFER WITH COMMON ENABLES

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output cuurent per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC365FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃
M74HC365DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
					25℃			−40∼+85℃	
				V_{CC}(V)	Min	Typ	ax	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

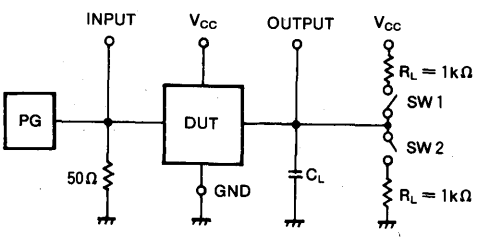
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)				22	ns
t_{PHL}					22	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)	C_L = 5 pF (Note 4)			36	ns
t_{PHZ}					36	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)			40	ns
t_{PZH}					40	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)	C_L = 50pF (Note 4)	2.0			105		130	ns
			4.5			24		30	
			6.0			19		24	
t_{PHL}			2.0			105		130	ns
			4.5			24		30	
			6.0			19		24	
t_{PLH}		C_L = 150pF (Note 4)	2.0			135		168	ns
			4.5			29		36	
			6.0			24		30	
t_{PHL}			2.0			135		168	ns
			4.5			29		36	
			6.0			24		30	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)	2.0			175		218	ns
			4.5			44		55	
			6.0			37		46	
t_{PHZ}			2.0			175		218	ns
			4.5			44		55	
			6.0			37		46	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)	2.0			230		287	ns
			4.5			44		55	
			6.0			35		43	
t_{PZH}			2.0			230		287	ns
			4.5			44		55	
			6.0			35		43	
t_{PZL}		C_L = 150pF (Note 4)	2.0			245		306	ns
			4.5			53		66	
			6.0			41		51	
t_{PZH}			2.0			245		306	ns
			4.5			53		66	
			6.0			41		51	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				49				pF

Note 3 : C_{DP} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

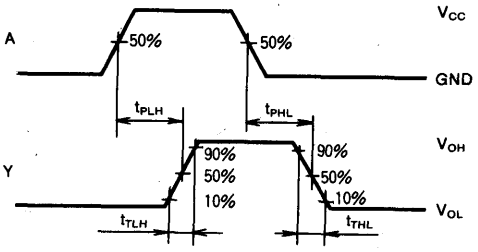
Note 4 : Test Circuit

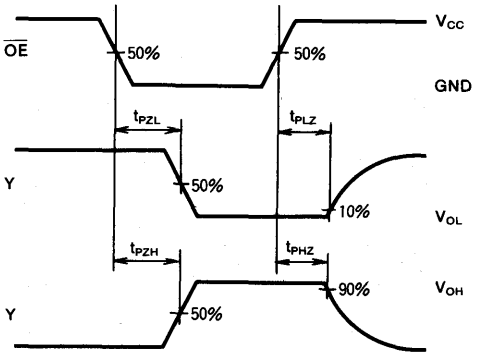


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC366P/FP/DP

HEX 3-STATE INVERTING BUFFER WITH COMMON ENABLES

DESCRIPTION

The M74HC366 is a semiconductor integrated circuit consisting of six buffers with 3-state inverted outputs and common enable inputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

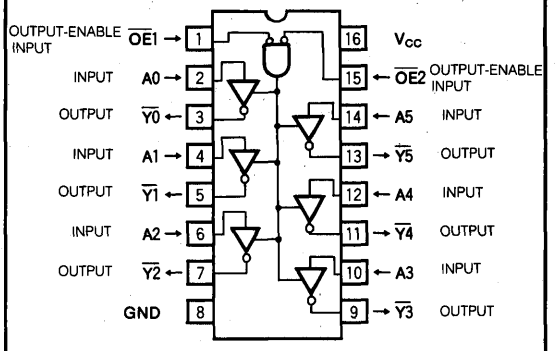
Use of silicon gate technology allows the M74HC366 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS366.

The M74HC366 consists of six 3-state buffers with output-enable inputs common to all circuits.

When output-enable inputs $\overline{OE1}$ and $\overline{OE2}$ are both low, outputs $\overline{Y}$ will become enable state. If input A is high, a low-level signal will be output to $\overline{Y}$ and if input A is low, a high-level signal will be output to $\overline{Y}$.

When at least one of input $\overline{OE1}$ or $\overline{OE2}$ is high, $\overline{Y}$ will become high-impedance state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

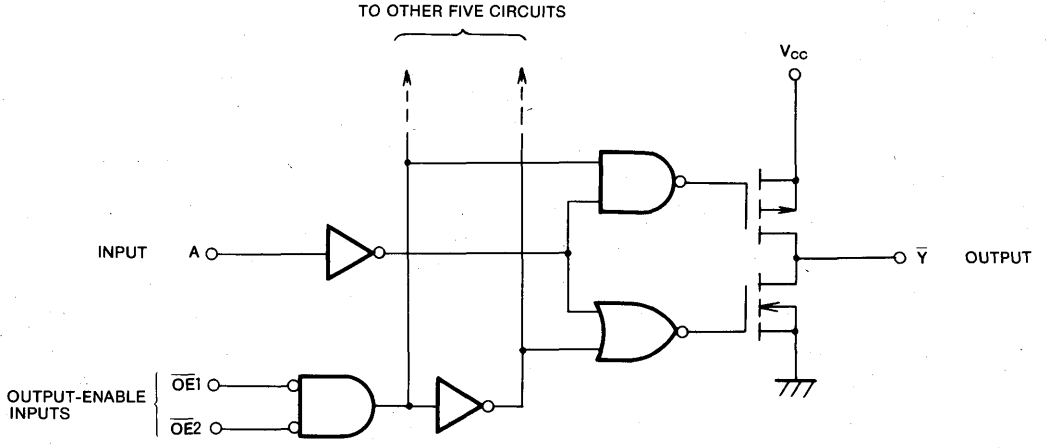
A version of the M74HC366 with a non-inverted output, the M74HC365, is also available.

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE1}$	$\overline{OE2}$	A	$\overline{Y}$
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Note 1 : X : Irrelevant
Z : High impedance

LOGIC DIAGRAM (EACH BUFFER)



MITSUBISHI ELECTRIC

HEX 3-STATE INVERTING BUFFER WITH COMMON ENABLES

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC366FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC366DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, I_{OH} = −20μA	2.0	1.9			1.9		V
		V_I = V_{IL}, I_{OH} = −20μA	4.5	4.4			4.4		
		V_I = V_{IL}, I_{OH} = −20μA	6.0	5.9			5.9		
		V_I = V_{IL}, I_{OH} = −6.0mA	4.5	4.18			4.13		
		V_I = V_{IL}, I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	2.0			0.1		0.1	V
		V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	4.5			0.1		0.1	
		V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	6.0			0.1		0.1	
		V_I = V_{IH}, V_{IL}, I_{OL} = 6.0mA	4.5			0.26		0.33	
		V_I = V_{IH}, V_{IL}, I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}	6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND	6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				18	ns
t_{PHL}	output propagation time (A − $\overline{Y}$)				18	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 4)			36	ns
t_{PHZ}	($\overline{OE}$ − $\overline{Y}$)				36	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 4)			40	ns
t_{PZH}	($\overline{OE}$ − $\overline{Y}$)				40	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			82		102	ns
			4.5			19		24	
			6.0			16		20	
t_{PHL}			2.0			82		102	ns
			4.5			19		24	
			6.0			16		20	
t_{PLH}		C_L = 150pF (Note 4)	2.0			107		134	ns
			4.5			26		32	
			6.0			22		27	
t_{PHL}			2.0			107		134	ns
			4.5			26		32	
			6.0			22		27	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			175		218	ns
			4.5			44		55	
			6.0			37		46	
t_{PHZ}			2.0			175		218	ns
			4.5			44		55	
			6.0			37		46	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			230		287	ns
			4.5			44		55	
			6.0			35		43	
t_{PZH}			2.0			230		287	ns
			4.5			44		55	
			6.0			35		43	
t_{PZL}		C_L = 150pF (Note 4)	2.0			245		306	ns
			4.5			53		66	
			6.0			41		51	
t_{PZH}			2.0			245		306	ns
			4.5			53		66	
			6.0			41		51	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				46				pF

Note 3 : C_{DP} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

M74HC367P/FP/DP

HEX
3-STATE NONINVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

DESCRIPTION

The M74HC367 is a semiconductor integrated circuit consisting of six buffers with 3-state noninverted outputs, the 4-bit and 2-bit sections having common enable inputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

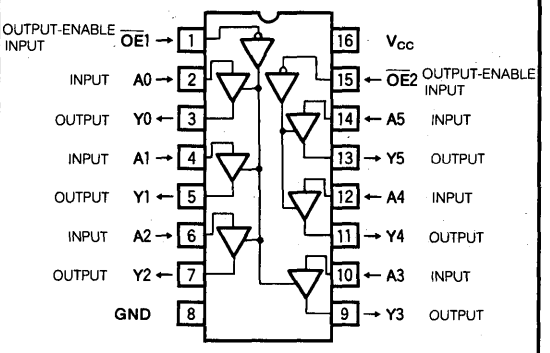
Use of silicon gate technology allows the M74HC367 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS367.

The M74HC367 consists of six 3-state buffers with output-enable inputs common to the 2-bit and 4-bit sections.

When output-enable input $\overline{OE}$ is low, outputs Y will become enable state. If input A is high, a high-level signal will be output to Y and if input A is low, a low-level signale will be output to Y.

When $\overline{OE}$ is high-level, Y will become high-impedance state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N
16P2P

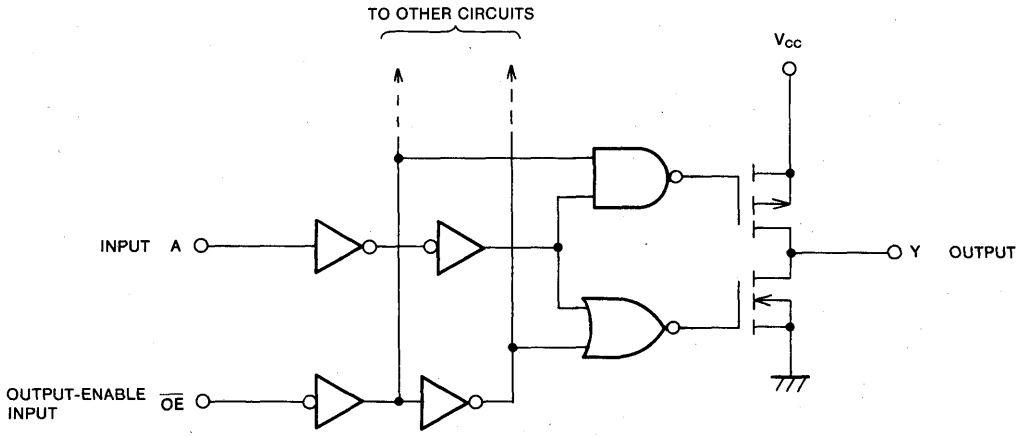
A version of the M74HC367 with an inverted output, the M74HC368, is also available.

FUNCTION TABLE (Note 1)

Inputs		Output
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

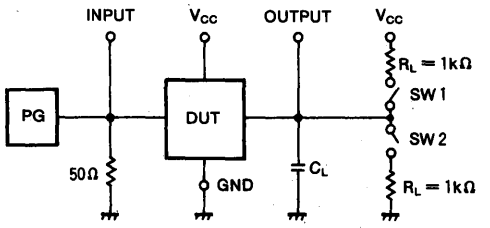
Note 1 : X : Irrelevant
Z : High impedance

LOGIC DIAGRAM (EACH BUFFER)



MITSUBISHI ELECTRIC

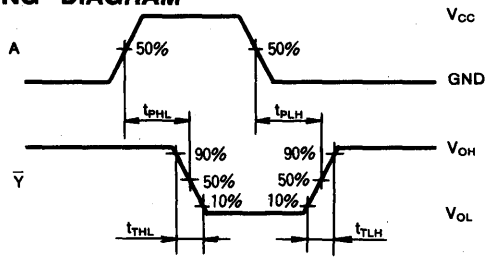
Note 4 : Test Circuit

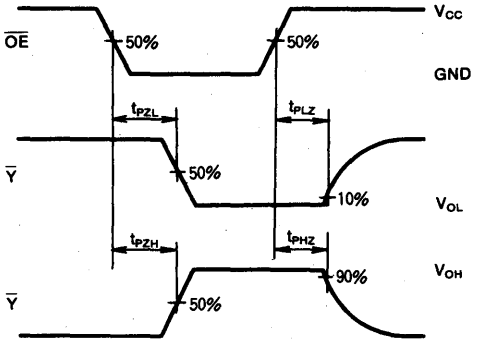


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





HEX
3-STATE NONINVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC367FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃
M74HC367DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −6.0mA	4.5	4.18			4.13		
		I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IL} ; I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 6.0mA	4.5			0.26		0.33	
		I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}	6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND	6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

HEX
3-STATE NONINVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)				22	ns
t_{PHL}					22	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)	C_L = 5 pF (Note 4)			33	ns
t_{PHZ}					33	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)			37	ns
t_{PZH}					37	ns

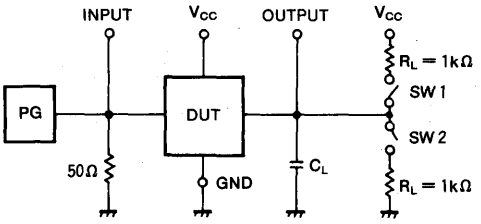
SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)	C_L = 50pF (Note 4)	2.0			105		130	ns
			4.5			24		30	
			6.0			19		24	
t_{PHL}			2.0			105		130	ns
			4.5			24		30	
			6.0			19		24	
t_{PLH}		C_L = 150pF (Note 4)	2.0			135		168	ns
			4.5			29		36	
			6.0			24		30	
t_{PHL}			2.0			135		168	ns
			4.5			29		36	
			6.0			24		30	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)	2.0			117		146	ns
			4.5			35		44	
			6.0			31		39	
t_{PHZ}			2.0			117		146	ns
			4.5			35		44	
			6.0			31		39	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)	2.0			172		216	ns
			4.5			38		47	
			6.0			35		43	
t_{PZH}			2.0			172		216	ns
			4.5			38		47	
			6.0			35		43	
t_{PZL}		C_L = 150pF (Note 4)	2.0			187		233	ns
			4.5			46		57	
			6.0			42		52	
t_{PZH}			2.0			187		233	ns
			4.5			46		57	
			6.0			42		52	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				47				pF

Note 3 : C_{DP} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

HEX
3-STATE NONINVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

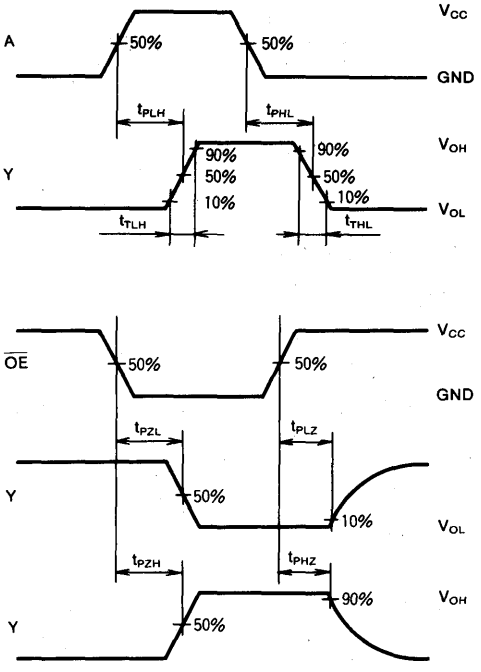
Note 4 : Test Circuit



Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC368P/FP/DP

HEX 3-STATE INVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

DESCRIPTION

The M74HC368 is a semiconductor integrated circuit consisting of six buffers with 3-state inverted output, the 4-bit and 2-bit sections having common enable inputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

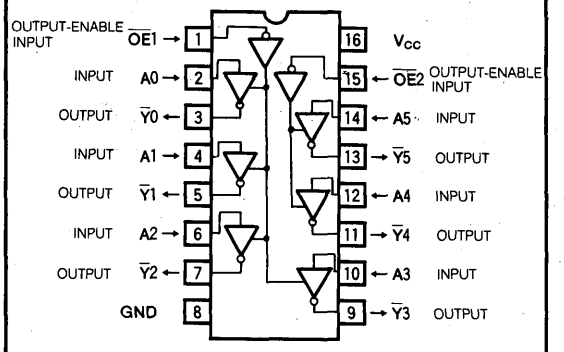
Use of silicon gate technology allows the M74HC368 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS368.

The M74HC368 consists of six 3-state buffers with output-enable inputs common to the 2-bit and 4-bit sections.

When output-enable input $\overline{OE}$ is low, outputs $\overline{Y}$ will become enable state. If input A is high, a low-level signale will be output to $\overline{Y}$ and if input A is low, a high-level signal will be output to $\overline{Y}$.

When $\overline{OE}$ is high, $\overline{Y}$ will become high-impedance state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

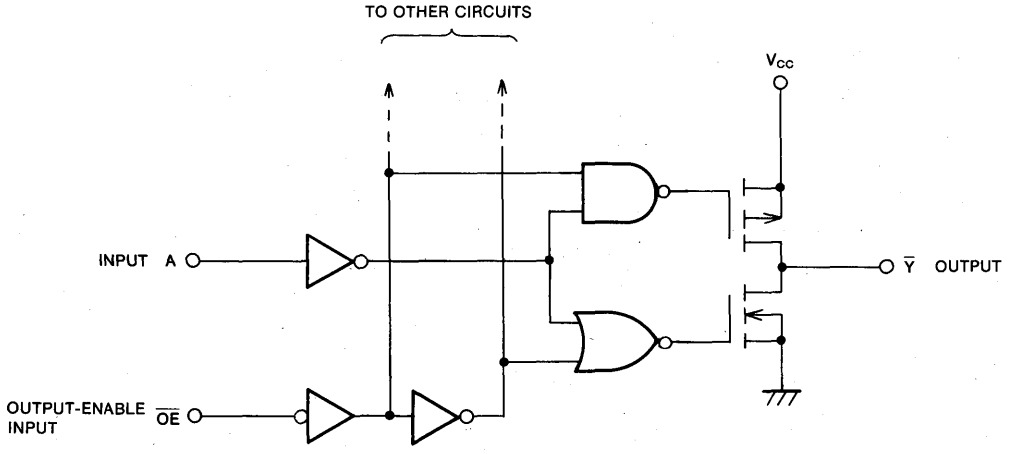
A version of the M74HC368 with a noninverted output, the M74HC367, is also available.

FUNCTION TABLE (Note 1)

Inputs		Output
$\overline{OE}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

Note 1 : X : Irrelevant
Z : High impedance

LOGIC DIAGRAM (EACH BUFFER)



MITSUBISHI ELECTRIC

HEX 3-STATE INVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC368FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃
M74HC368DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
					25℃		−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

HEX 3-STATE INVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)				18	ns
t_{PHL}					18	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 5 pF (Note 4)			33	ns
t_{PHZ}					33	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)			37	ns
t_{PZH}					37	ns

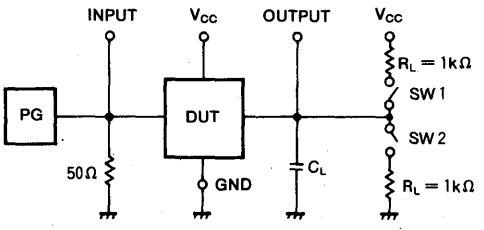
SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			82		102	ns
			4.5			19		24	
			6.0			16		20	
t_{PHL}			2.0			82		102	ns
			4.5			19		24	
			6.0			16		20	
t_{PLH}		C_L = 150pF (Note 4)	2.0			107		134	ns
			4.5			26		32	
			6.0			22		27	
t_{PHL}			2.0			107		134	ns
			4.5			26		32	
			6.0			22		27	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			117		146	ns
			4.5			35		44	
			6.0			31		39	
t_{PHZ}			2.0			117		146	ns
			4.5			35		44	
			6.0			31		39	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			172		216	ns
			4.5			38		47	
			6.0			35		43	
t_{PZH}			2.0			172		216	ns
			4.5			38		47	
			6.0			35		43	
t_{PZL}		C_L = 150pF (Note 4)	2.0			187		233	ns
			4.5			46		57	
			6.0			42		52	
t_{PZH}			2.0			187		233	ns
			4.5			46		57	
			6.0			42		52	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				44				pF

Note 3 : C_{DP} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

HEX 3-STATE INVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

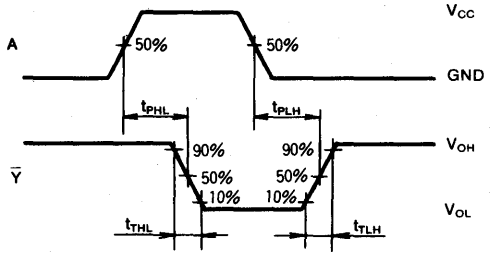
Note 4 : Test Circuit

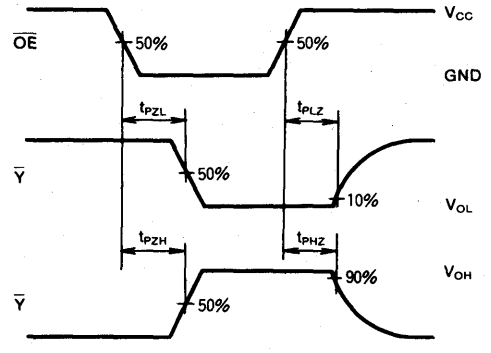


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC373P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC373 is a semiconductor integrated circuit consisting of eight 3-state output D-type latches with common latch-enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

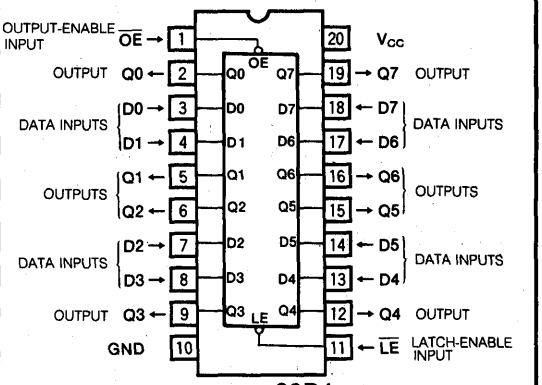
Use of silicon gate technology allows the M74HC373 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS373.

The M74HC373 consists of eight D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.

When $\overline{LE}$ is high, the data at input D appears at output Q through the latch and the Q state follows changes in the D state. When $\overline{LE}$ changes from high-level to low-level, the data existing immediatry prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected .

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

When $\overline{OE}$ is high, all outputs Q will become high-impedance state.

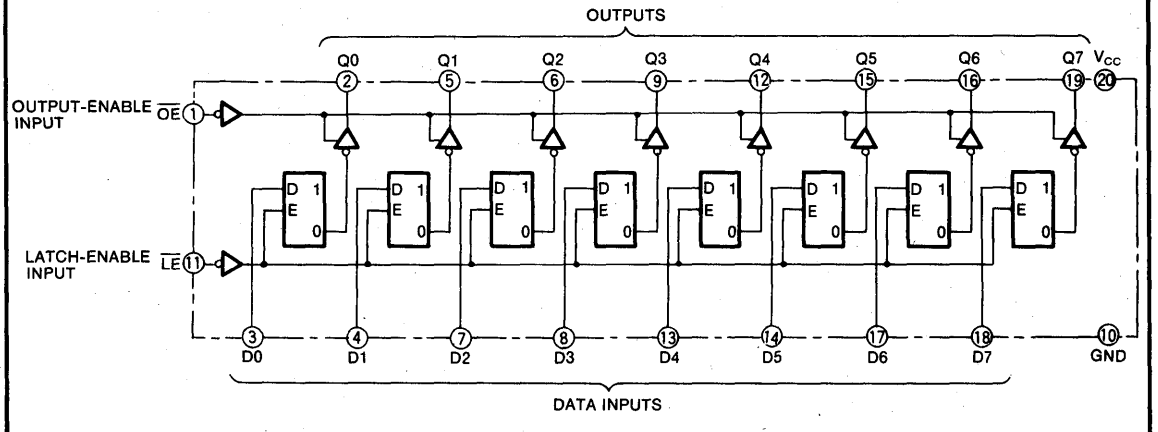
A version of the M74HC373 with the same pin connections and an inverted output, the M74HC533, is also available.

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q^0
H	X	X	Z

Note 1 : Q_0: Output state Q before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Not 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC373FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC373DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 6.0mA	4.5		0.26		0.33	
			I_{OL} = 7.8mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)				25	ns
t_{PHL}					25	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)				30	ns
t_{PHL}					30	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

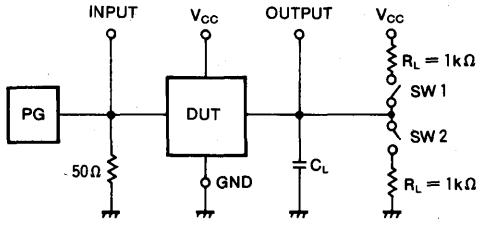
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D− Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PLH}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PHL}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)	C_L = 50pF (Note 4)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}		C_L = 150pF (Note 4)	2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PHL}			2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Output disabled capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				57				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Latch enable pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to $\overline{LE}$		2.0	75			90		ns
			4.5	15			18		
			6.0	13			16		
t_h	D hold time with respect to $\overline{LE}$		2.0	50			60		ns
			4.5	10			12		
			6.0	9			11		

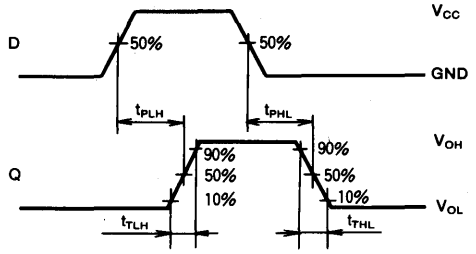
Note 4 : Test Circuit

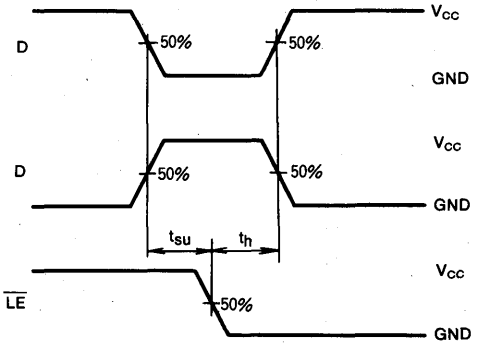


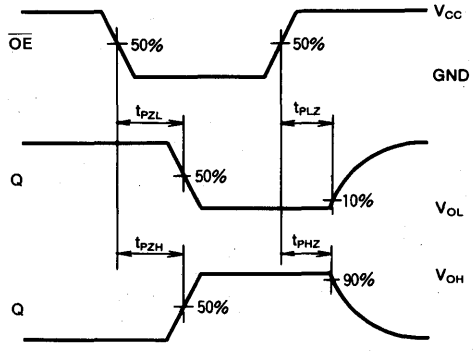
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

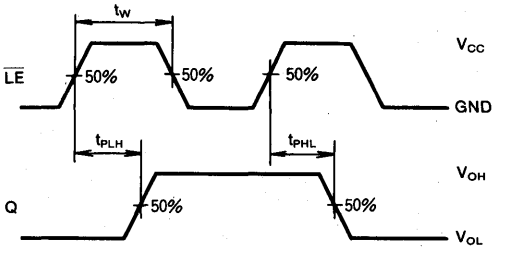
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM









MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC373-1P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC373-1 is a semiconductor integrated circuit consisting of eight 3-state output D-type latches with common latch-enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 9ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC373-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS373.

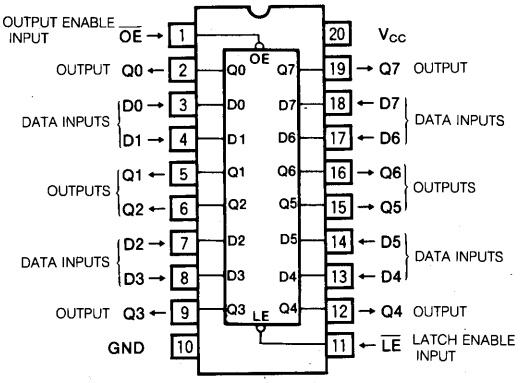
The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC373-1 consists of eight D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.

When $\overline{LE}$ is high, the data at input D appears at output Q through the latch and the Q state follows changes in the D state. When $\overline{LE}$ changes from high-level to low-level, the data existing immediatry prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected .

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

When $\overline{OE}$ is high, all outputs Q will become high-impedance state.

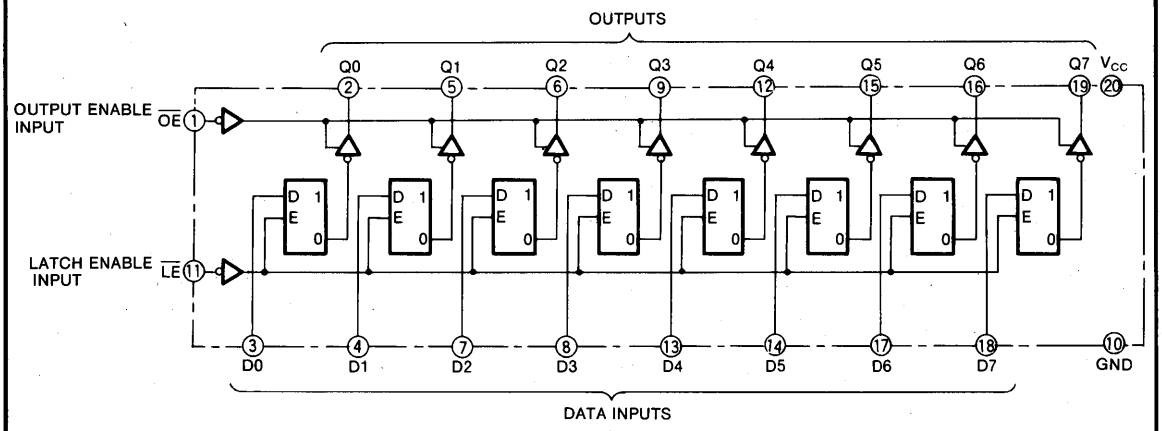
A version of the M74HC373-1 with the same pin connections and an inverted output, the M74HC533-1, is also available.

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q^0
H	X	X	Z

Note 1 : Q^0: Output state Q before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

LOGIC DIAGRAM



OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼+150	℃

Note 2 : M74HC373-1FP , T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC373-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltnge	V_O = 0.1V, V_{CC} − 0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.98			3.84		
V_{OL}	Low-level output voltnge	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.39		0.5	
I_{IH}	High-level inputcurrent	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)				18	ns
t_{PHL}					18	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)				21	ns
t_{PHL}					21	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 5 pF (Note 4)			20	ns
t_{PHZ}					20	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)			23	
t_{PZH}					23	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

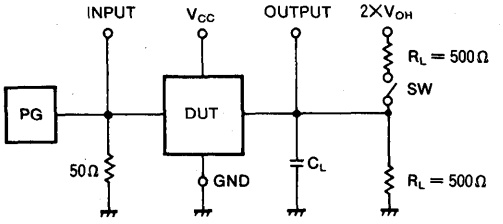
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)		2.0			100		125	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		125	
			4.5			20		25	
			6.0			17		21	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)		2.0			125		155	ns
			4.5			25		31	
			6.0			21		26	
t_{PHZ}			2.0			125		155	
			4.5			25		31	
			6.0			21		26	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)		2.0			125		155	ns
			4.5			25		31	
			6.0			21		26	
t_{PZH}			2.0			125		155	
			4.5			25		31	
			6.0			21		26	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)								

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Latch enable pulse width		2.0	60			75		ns
			4.5	12			15		
			6.0	10			13		
t_{su}	D setup time with respect to $\overline{LE}$		2.0	50			65		ns
			4.5	10			13		
			6.0	9			11		
t_h	D hold time with respect to $\overline{LE}$		2.0	25			30		ns
			4.5	5			6		
			6.0	5			6		

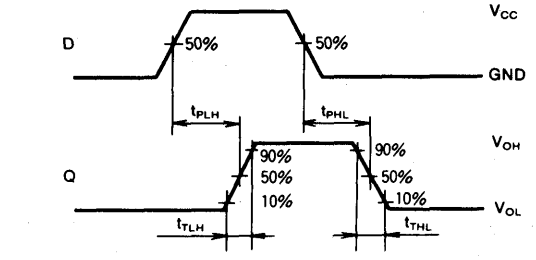
Note 4 : Test Circuit

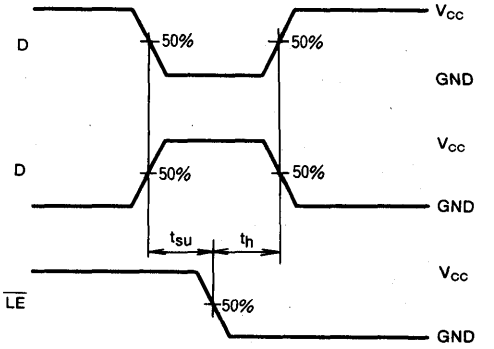


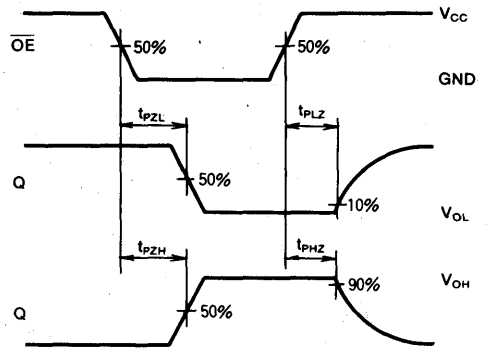
Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

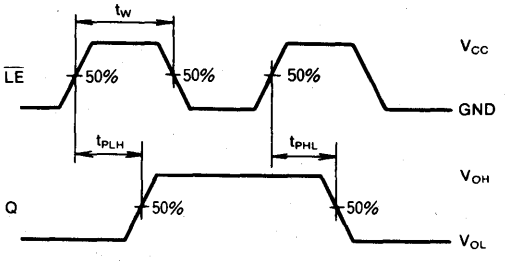
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM









MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HCT373-1P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT373-1 is a semiconductor integrated circuit consisting of eight 3-state output D-type latches with common latch-enable input and output-enable input.

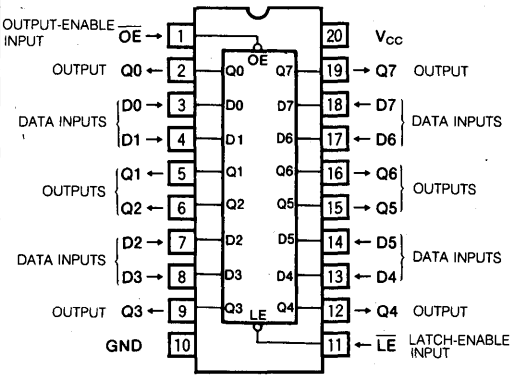
FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 11ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40∼+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4 20P2N 20P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT373-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS373.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT373-1 consists of eight D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.

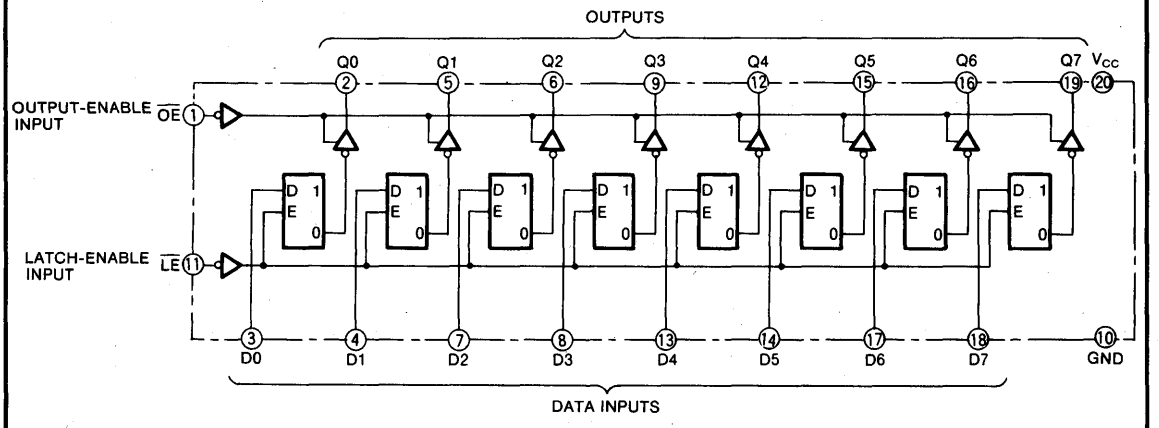
When $\overline{LE}$ is high, the data at input D appears at output Q through the latch and the Q state follows changes in the D state. When $\overline{LE}$ changes from high-level to low-level, the data existing immediatry prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected .

When $\overline{OE}$ is high, all outputs Q will become high-impedance state.

A version of the M74HCT373-1 with the same pin connections and an inverted output, the M74HCT533-1, is also available.

LOGIC DIAGRAM



OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q^0
H	X	X	Z

Note 1 : Q_0: Output state Q before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Not 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HCT373-1FP, T_a = −40~+75℃ and T_a = 75~85℃ are derated at −7mW/℃.
M74HCT373-1DWP, T_a = −40~+80℃ and T_a = 80~85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	$V_I = V_{IL}$	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.98			3.84		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.39		0.5	
I_{IH}	High-level input current	$V_I = V_{CC}$				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	
I_{OZH}	Off-state high-level output current	$V_I = V_{IH}$, V_{IL}, $V_O = V_{CC}$				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	$V_I = V_{IH}$, V_{IL}, V_O = GND				−0.5		−5.0	
I_{CC}	Quiescent supply current	$V_I = V_{CC}$, GND, I_O = 0μA				5.0		50.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 5)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				18	ns
t_{PHL}	output propagation time (D − Q)				18	ns
t_{PLH}	Low-level to high-level and high-level to low-level				21	ns
t_{PHL}	output propagation time ($\overline{LE}$ − Q)				21	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 5)			20	ns
t_{PHZ}	($\overline{OE}$ − Q)				20	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 5)			23	ns
t_{PZH}	($\overline{OE}$ − Q)				23	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12		15	ns
t_{THL}					12		15	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)				20		25	ns
t_{PHL}					20		25	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)				17		21	ns
t_{PHL}					17		21	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)				25		31	ns
t_{PHZ}					25		31	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)				25		31	ns
t_{PZH}					25		31	
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE} = V_{CC}$			15		15	
C_{PD}	Power dissipation capacitance (Note 4)							

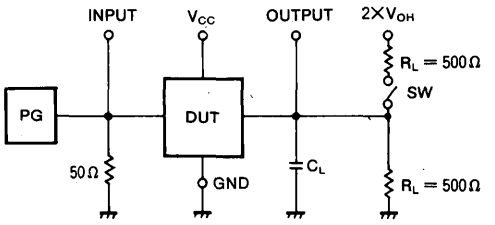
Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −40∼+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40∼+85℃		
			Min	Typ	Max	Min	Max	
t_w	Latch enable pulse with		12			15		ns
t_{su}	D setup time with respect to $\overline{LE}$		10			13		ns
t_h	D hold time with respect to $\overline{LE}$		5			6		ns

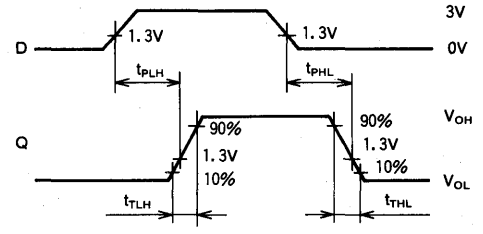
Note 4 : Test Circuit

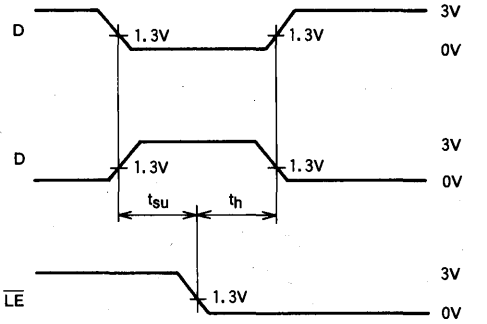


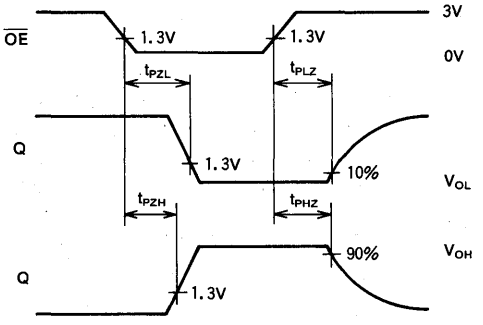
Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

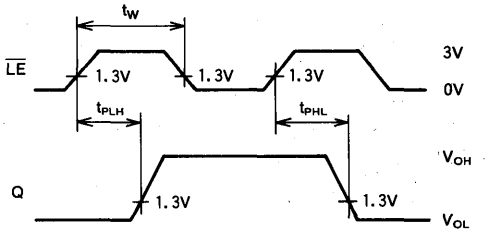
(1) The pulse generator (PG) has the following characteristics (10%∼90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM









MITSUBISHI ELECTRIC

M74HC374P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC374 is a semiconductor integrated circuit consisting of eight positive-edge-triggered 3-state output D-type flip-flops with common clock and output-enable input.

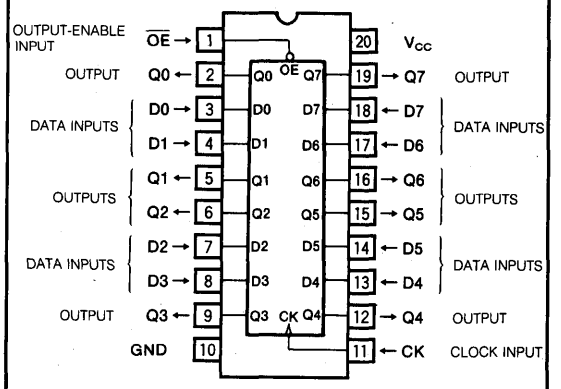
FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: (Clock frequency) 65MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC374 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS374.

The M74HC374 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{OE}$.

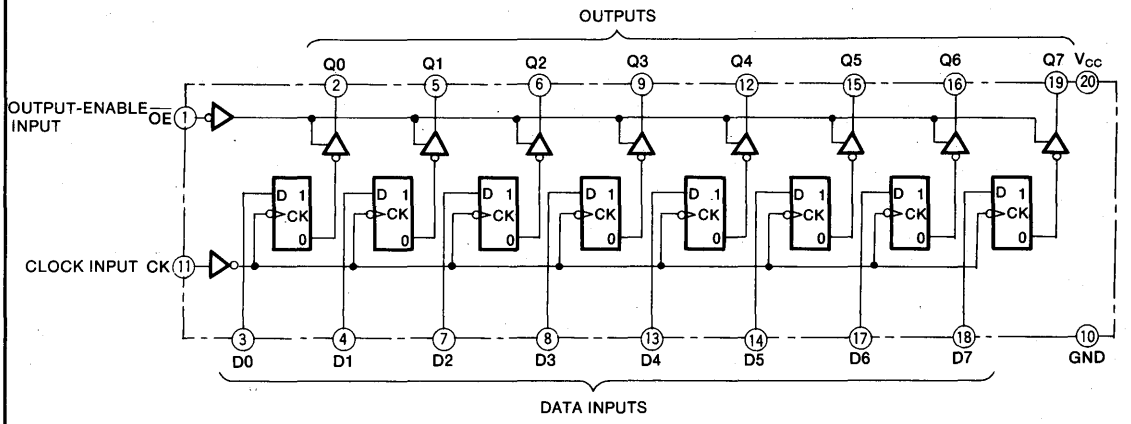
When CK changes from low-level to high-level, the signals just previously input at D is stored in the flip-flop.

When $\overline{OE}$ is low, the signal stored in the flip-flop will be output to Q.

When $\overline{OE}$ is high, all outputs Q will become high-impedance state. The contents stored in the flip-flop will not be affected even if $\overline{OE}$ changes.

A version of the M74HC374 with the same pin connections and an inverted output, the M74HC534, is also available.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q^0
L	H	X	Q^0
L	↓	X	Q^0
H	X	X	Z

Note 1 : Q^0: Output state Q before clock input changed
Z : High inmpedance
X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC374FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC374DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 6.0mA	4.5		0.26		0.33	
			I_{OL} = 7.8mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				32	ns
t_{PHL}					32	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

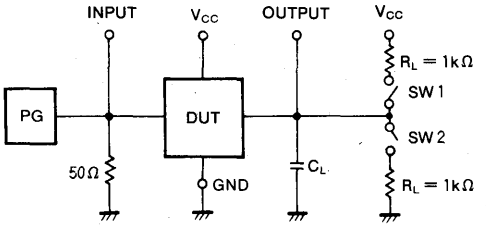
Symbol	Parameter	Test conditions	Limits					Unit
				25℃			−40~+85℃	
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	6			5		MHz
			4.5	30			24		
			6.0	35			28		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)	C_L = 50pF (Note 4)	2.0			180		227	ns
			4.5			36		45	
			6.0			31		39	
t_{PHL}			2.0			180		227	ns
			4.5			36		45	
			6.0			31		39	
t_{PLH}		C_L = 150pF (Note 4)	2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				63				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	Limits 25℃ Min	Typ	Max	−40~+85℃ Min	Max	Unit
t_w	Clock pluse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to CK		2.0	75			90		ns
			4.5	15			18		
			6.0	13			16		
t_h	D hold time with respect to CK		2.0	50			60		ns
			4.5	10			12		
			6.0	9			11		

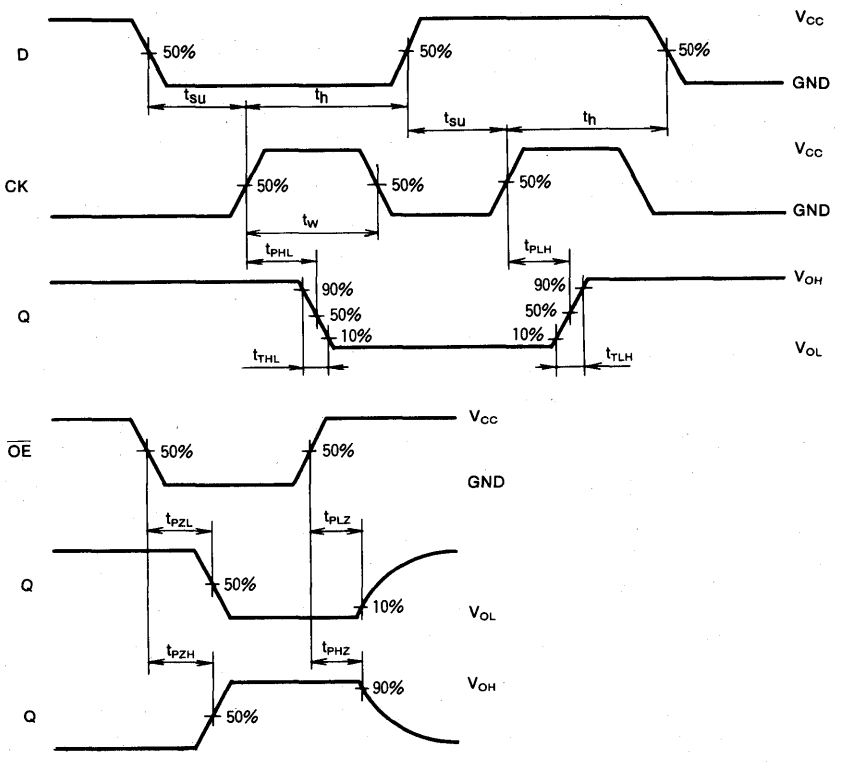
Note 4 : Test Circuit



Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC374-1P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC374-1 is a semiconductor integrated circuit consisting of eight positive-edge-triggered 3-state output D-type flip-flops with common clock and output-enable input.

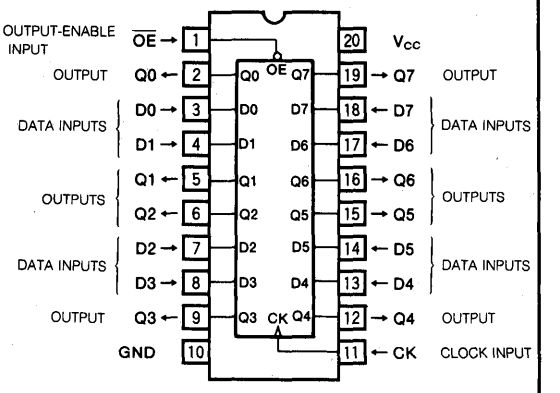
FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: (clock frequency) 60MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC374-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS374.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC374-1 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{OE}$.

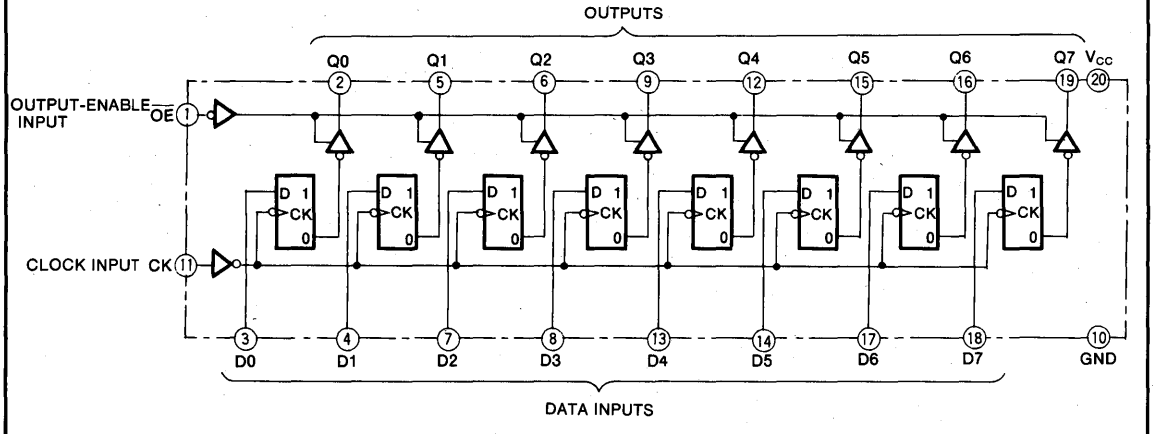
When CK changes from low-level to high-level, the signals just previously input at D is stored in the flip-flop.

When $\overline{OE}$ is low, the signal stored in the flip-flop will be output to Q.

When $\overline{OE}$ is high, all outputs Q will become high-impedance state. The contents stored in the flip-flop will not be affected even if $\overline{OE}$ changes.

A version of the M74HC374-1 with the same pin connections and an inverted output, the M74HC534-1, is also available.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q^0
L	H	X	Q^0
L	↓	X	Q^0
H	X	X	Z

Note 1 : Q^0: Output state Q before clock input changed
Z : High inmpedance
X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC374-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC374-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.39		0.5	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				20	ns
t_{PHL}					20	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 5 pF (Note 4)			20	ns
t_{PHZ}					20	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)			23	ns
t_{PZH}					23	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

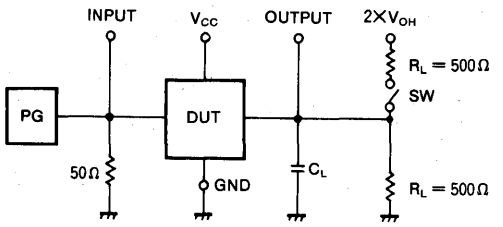
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	6			5		MHz
			4.5	32			26		
			6.0	38			31		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			110		140	ns
			4.5			22		28	
			6.0			19		24	
t_{PHL}			2.0			110		140	
			4.5			22		28	
			6.0			19		24	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)		2.0			125		155	ns
			4.5			25		31	
			6.0			21		26	
t_{PHZ}			2.0			125		155	
			4.5			25		31	
			6.0			21		26	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)		2.0			125		155	ns
			4.5			25		31	
			6.0			21		26	
t_{PZH}			2.0			125		155	
			4.5			25		31	
			6.0			21		26	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)								

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop)
The power dissipated during operation under no-load conditions is calculated using the following formula;
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Clock pluse width		2.0	60			75		ns
			4.5	12			15		
			6.0	10			13		
t_{su}	D setup time with respect to CK		2.0	50			65		ns
			4.5	10			13		
			6.0	9			11		
t_h	D hold time with respect to CK		2.0	25			30		ns
			4.5	5			6		
			6.0	5			6		

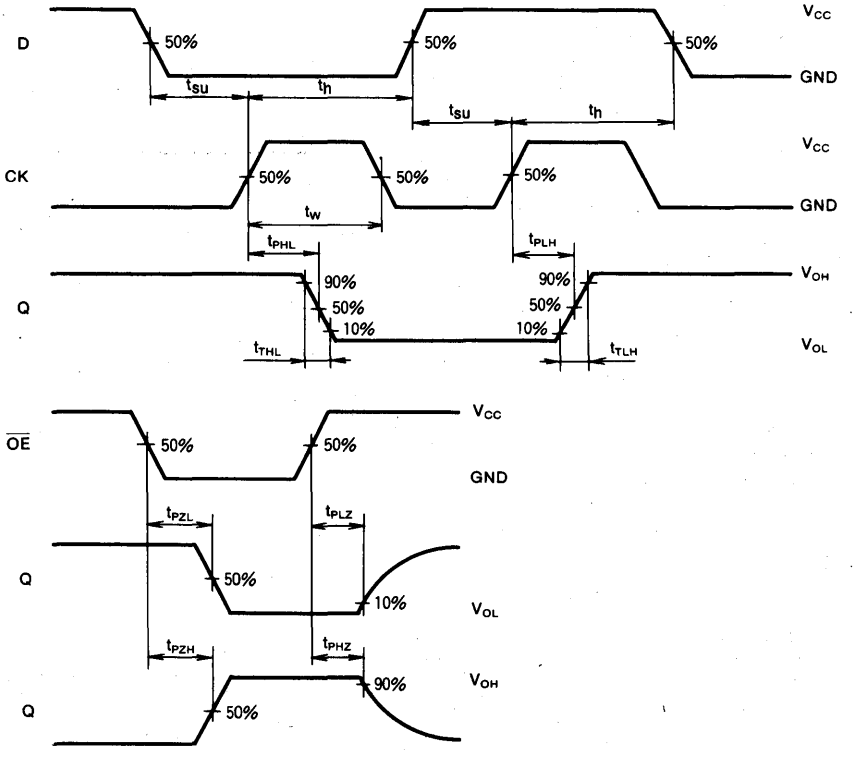
Note 4 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HCT374-1P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT374-1 is a semiconductor integrated circuit consisting of eight positive-edge-triggered 3-state output D-type flip-flops with common clock and output-enable input.

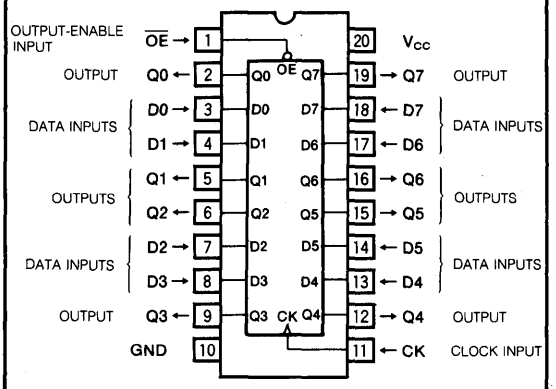
FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V mim
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: (Clock frequency) 55MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40∼+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT374-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS374.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT374-1 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{OE}$.

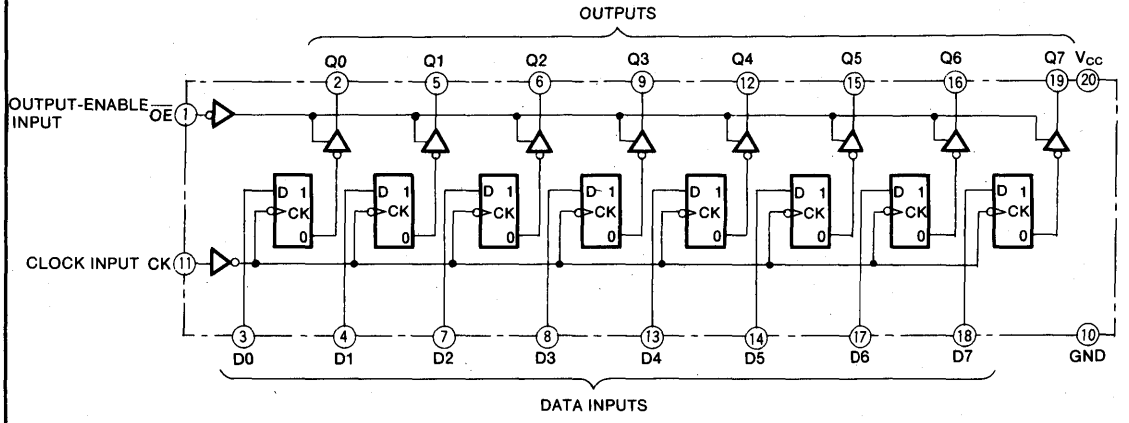
When CK changes from low-level to high-level, the signals just previously input at D is stored in the flip-flop.

When $\overline{OE}$ is low, the signal stored in the flip-flop will be output to Q.

When $\overline{OE}$ is high, all outputs Q will become high-impedance state. The contents stored in the flip-flop will not be affected even if $\overline{OE}$ changes.

A version of the M74HCT374-1 with the same pin connections and an inverted output, the M74HCT534-1, is also available.

LOGIC DIAGRAM



OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q^0
L	H	X	Q^0
L	↓	X	Q^0
H	X	X	Z

Note 1 : Q^0: Output state Q before clock input changed
Z : High inmpedance
X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HCT374-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HCT374-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.39		0.5	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 5)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (CK − Q)				20	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 5)			20	ns
t_{PHZ}	($\overline{OE}$ − Q)				20	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 5)			23	ns
t_{PZH}	($\overline{OE}$ − Q)				23	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
			Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 5)	32			26		MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				12		15	ns
t_{THL}					12		15	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				22		28	ns
t_{PHL}					22		28	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)				25		31	ns
t_{PHZ}					25		31	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)				25		31	ns
t_{PZH}					25		31	
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	
C_{PD}	Power dissipation capacitance (Note 4)							

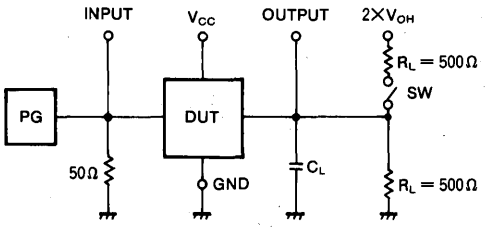
Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			Min	Typ	Max	Min	Max	
t_w	Clock pluse width		12			15		ns
t_{su}	D setup time with respect to CK		10			13		ns
t_h	D hold time with respect to CK		5			6		ns

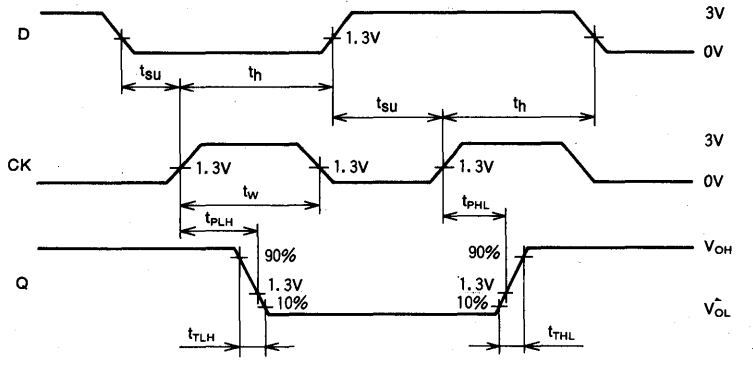
Note 5 : Test Circuit

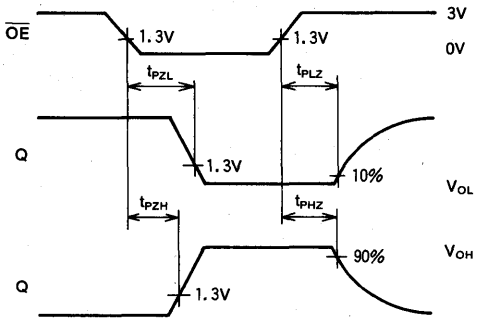


Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

M74HC375P/FP/DP

DUAL 2-BIT TRANSPARENT LATCH

DESCRIPTION

The M74HC375 is a semiconductor integrated circuit consisting of four bistable latches with outputs Q and $\overline{Q}$.

FEATURES

- High-speed: 14ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

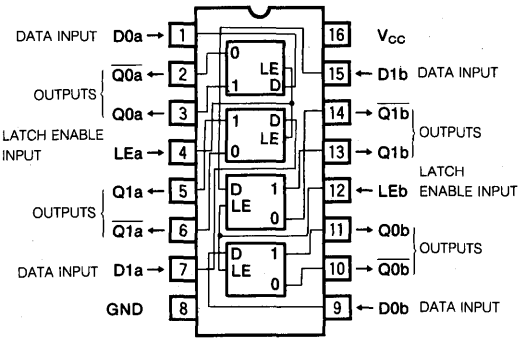
Use of silicon gate technology allows the M74HC375 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS375.

The use of buffered outputs improves the input-to output transfer characteristics and minimizes output impedance variations with respect to input voltage variations.

The M74HC375 has four D-type latches, and is provided with enable inputs LE common to two circuits each. When LE is high, the infromation from the data input D will appear in the outputs Q and $\overline{Q}$. When the D signal changes, the signal that appears in outputs Q and $\overline{Q}$ also will change. When LE changes from high to low, the status of D immediately before the change will be latched will LE is low, Q and $\overline{Q}$ will not change even if D changes.

A unit, the M74HC75, having the same functions and electrical characteristics as the M74HC375 is also available.

PIN CONFIGURATION (TOP VIEW)



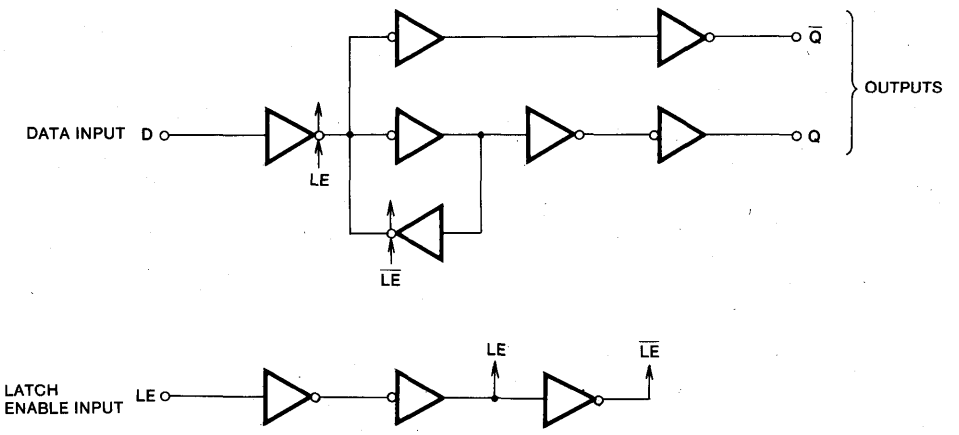
16P4
Outline 16P2N
16P2P

FUNCTION TABLE (Note 1)

Inputs		Outputs	
LE	D	Q	$\overline{Q}$
H	H	H	L
H	L	L	H
L	X	Q^0	$\overline{Q^0}$

Note 1 : Q^0, $\overline{Q^0}$: Output state Q, $\overline{Q}$ before input condition is set
X : Irrelevant

LOGIC DIAGRAM (EACH LATCH)



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC375FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC375DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level outnput voltage	V_I = V_{IH}, V_{IL} I_{OH} = −20μA	2.0	1.9			1.9		V
		V_I = V_{IH}, V_{IL} I_{OH} = −20μA	4.5	4.4			4.4		
		V_I = V_{IH}, V_{IL} I_{OH} = −20μA	6.0	5.9			5.9		
		V_I = V_{IH}, V_{IL} I_{OH} = −4.0mA	4.5	4.18			4.13		
		V_I = V_{IH}, V_{IL} I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level outnput voltage	V_I = V_{IH}, V_{IL} I_{OL} = 20μA	2.0			0.1		0.1	V
		V_I = V_{IH}, V_{IL} I_{OL} = 20μA	4.5			0.1		0.1	
		V_I = V_{IH}, V_{IL} I_{OL} = 20μA	6.0			0.1		0.1	
		V_I = V_{IH}, V_{IL} I_{OL} = 4.0mA	4.5			0.26		0.33	
		V_I = V_{IH}, V_{IL} I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				23	ns
t_{PHL}	output propagation time (D − Q)				23	ns
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (D − $\overline{Q}$)				20	ns
t_{PLH}	Low-level to high-level and high-level to low-level				27	ns
t_{PHL}	output propagation time (LE − Q)				27	ns
t_{PLH}	Low-level to high-level and high-level to low-level				23	ns
t_{PHL}	output propagation time (LE − $\overline{Q}$)				23	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

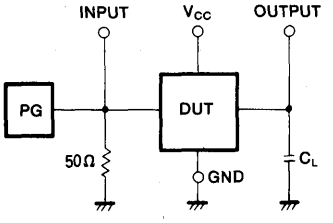
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)		2.0			125		156	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		156	ns
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Q}$)		2.0			110		138	ns
			4.5			22		28	
			6.0			19		24	
t_{PHL}			2.0			110		138	ns
			4.5			22		28	
			6.0			19		24	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − Q)		2.0			145		181	ns
			4.5			29		36	
			6.0			25		31	
t_{PHL}			2.0			145		181	ns
			4.5			29		36	
			6.0			25		31	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − $\overline{Q}$)		2.0			125		156	ns
			4.5			25		31	
			6.0			22		28	
t_{PHL}			2.0			125		156	ns
			4.5			25		31	
			6.0			22		28	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				66				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

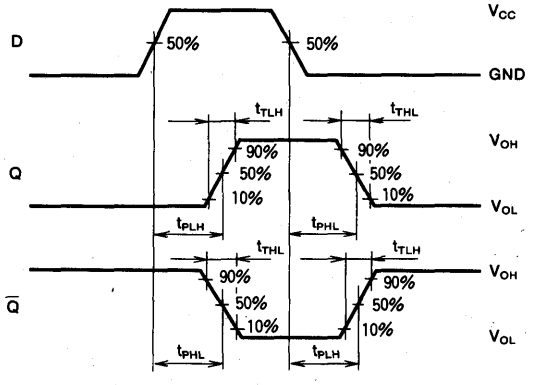
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	LE pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
t_{su}	D setup time with respect to LE		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	D hold time with respect to LE		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

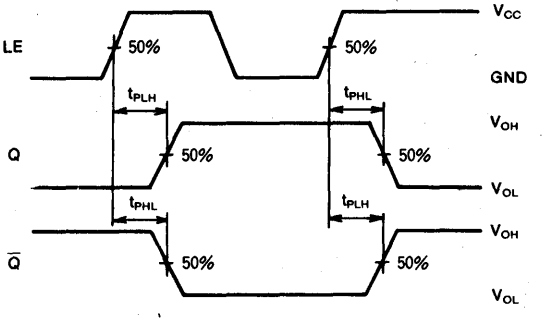
Note 4 : Test Circuit

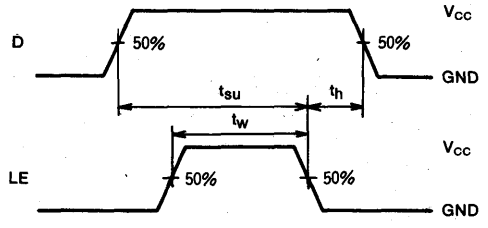


(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC377P/FP/DWP

OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND ENABLE

DESCRIPTION

The M74HC377 is a semiconductor integrated circuit consisting of eight positive-edge triggered D-type flip flops with common clock and enable inputs.

FEATURES

- High-speed: (clock frequency)40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

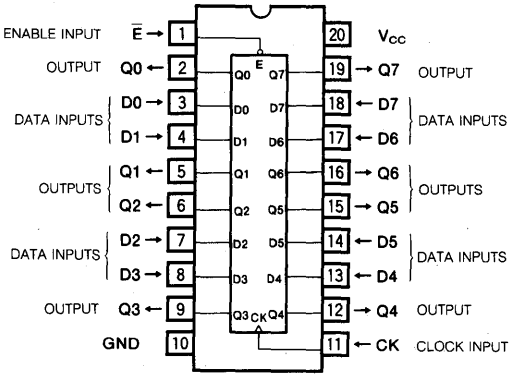
Use of silicon gate technology allows the M74HC377 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS377.

The M74HC377 contains eight D-type flip flops with common clock and enable inputs.

When CK changes from low-level and high-level, the signals just previously input at D appears at outputs Q in accordance with function table given.

When $\overline{E}$ is high, the output does not change, irrespective of other inputs. Changing $\overline{E}$ from high to low, or from low to high does not cause misoperation.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{E}$	CK	D	Q
H	X	X	Q^0
L	↑	H	H
L	↑	L	L
X	L	X	Q^0

Note 1 : ↑ : Change from low to high
Q^0 : Output state Q before input conditions are set
X : Irrelevant

M74HC390P/FP/DP

DUAL 4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷5 SECTIONS

DESCRIPTION

The M74HC390 is a semiconductor integrated circuit consisting of two asynchronous decade counters with direct reset input.

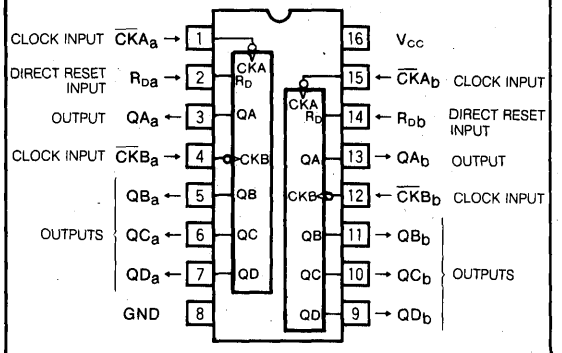
FEATURES

- High-speed: (clock frequency) 60MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



16P4
Outline 16P2N
16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC390 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS390.

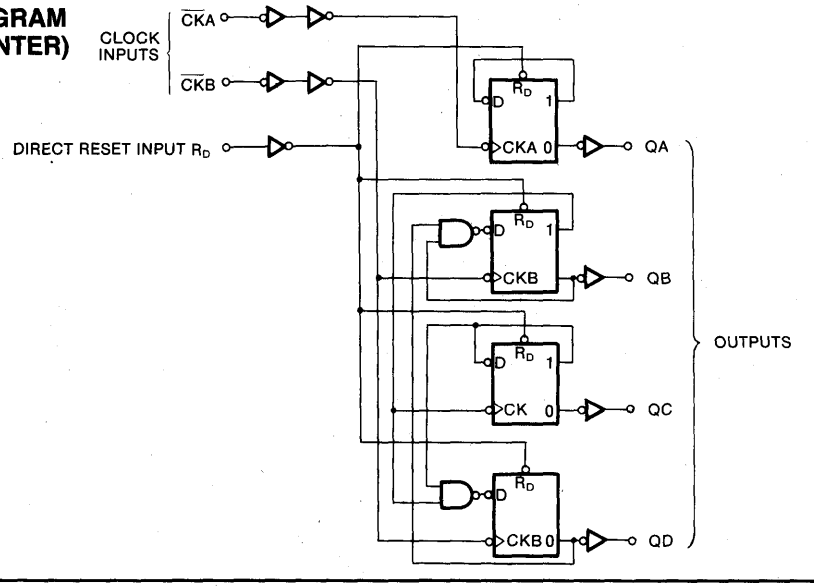
Each decade counter consists of a binary counter and a divide-by-5 counter. When using a binary counter, by applying the count pulse to clock input $\overline{CKA}$ a frequency-demultiplied signal will be output to QA. When using a divide-by-5 counter, by applying the count pulse to clock input $\overline{CKB}$ a frequency-demultiplied signal will be output to QB through QD.

When using the decade counter to output BCD code from QA through QD, connect QA and $\overline{CKB}$ together and apply the count pulse to $\overline{CKA}$. When outputting a signal with a 50% duty cycle from QA, connect QD and $\overline{CKA}$ together and apply the count pulse to $\overline{CKB}$.

Counting takes place when the clock input changes from high-level to low-level.

When direct reset input R_D is high, QA through QB will become low irrespective of other inputs. Maintain the low-level state when counting.

LOGIC DIAGRAM (EACH COUNTER)



MITSUBISHI ELECTRIC

DUAL 4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷5 SECTIONS

FUNCTION TABLE (Note 1)

Inputs		Outputs			
$\overline{CK}$	R_D	QA	QB	QC	QD
X	H	L	L	L	L
↓	L	Count			

Note 1 : ↓ : Change from high to low level
X : Irrelevant

Count number	QA	QB	QC	QD
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

With QA and $\overline{CK}$B connected and $\overline{CK}$A used as input.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC390FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC390DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

DUAL 4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷5 SECTIONS

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0		−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0		4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$A − QA)				20	ns
t_{PHL}					20	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$A − QC, with QA and $\overline{CK}$B connected)				50	ns
t_{PHL}					50	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$B − QB)				21	ns
t_{PHL}					21	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$B − QC)				32	ns
t_{PHL}					32	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$B − QD)				21	ns
t_{PHL}					21	ns
t_{PHL}	High-level to low-level output propagation time (R_D − QA, QB, QC, QD)				28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

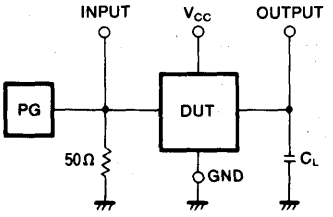
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}A - QA$)		2.0			120		150	ns
			4.5			24		30	
			6.0			21		26	
t_{PHL}			2.0			120		150	ns
			4.5			24		30	
			6.0			21		26	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}A - QC$, with QA and $\overline{CK}B$ connected)		2.0			290		360	ns
			4.5			58		72	
			6.0			50		62	
t_{PHL}			2.0			290		360	ns
			4.5			58		72	
			6.0			50		62	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}B - QB$)		2.0			130		160	ns
			4.5			26		33	
			6.0			22		28	
t_{PHL}			2.0			130		160	ns
			4.5			26		33	
			6.0			22		28	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}B - QC$)		2.0			185		230	ns
			4.5			37		46	
			6.0			32		40	
t_{PHL}			2.0			185		230	ns
			4.5			37		46	
			6.0			32		40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}B - QD$)		2.0			130		160	ns
			4.5			26		33	
			6.0			22		28	
t_{PHL}			2.0			130		160	ns
			4.5			26		33	
			6.0			22		28	
t_{PHL}	High-level to low-level output propagation time ($R_D - QA$, QB, QC, QD)		2.0			165		210	ns
			4.5			33		41	
			6.0			28		35	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				46				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per counter)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

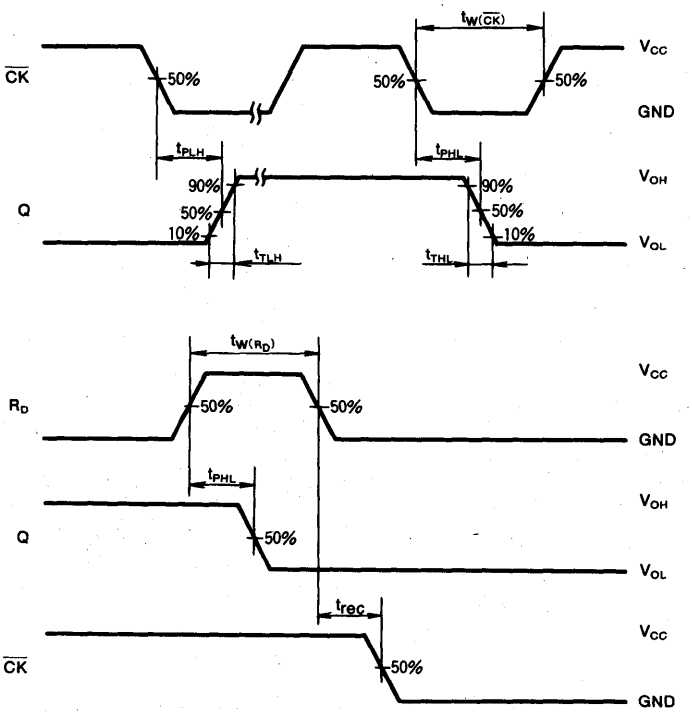
Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{w(\overline{CK})}$	Clock pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
$t_{w(R_D)}$	Direct reset pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
t_{rec}	R_D recovery time with respect to $\overline{CK}$		2.0	50			65		ns
			4.5	10			13		
			6.0	9			11		

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC393P/FP/DP

DUAL 4-STAGE BINARY RIPPLE COUNTER

DESCRIPTION

The M74HC393 is a semiconductor integrated circuit consisting of two asynchronous 4-bit binaly (hexadecimal) counters with direct reset input.

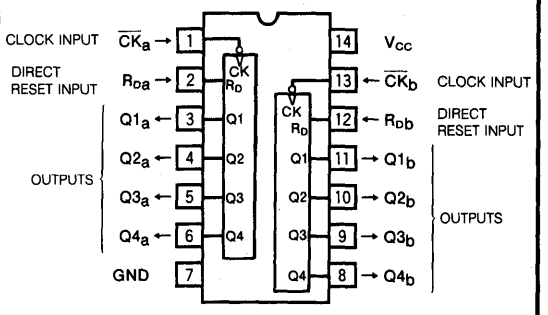
FEATURES

- High-speed: (clock frequency) 60MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



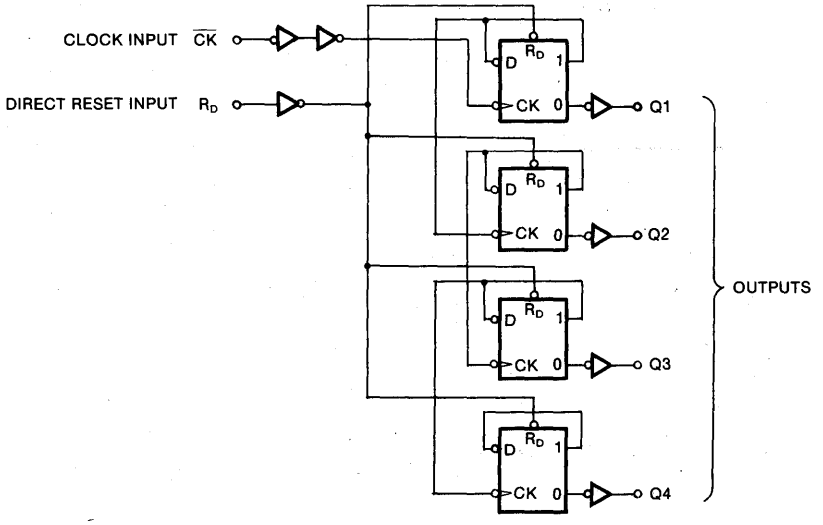
Outline 14P4, 14P2N, 14P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC393 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS393.

When the count pulse is applied to clock input $\overline{CK}$, a binary code will be output to Q1 through Q4. Counting takes place when the clock input changes from high-level to low-level. When direct reset input R_D is high, Q1 through Q4 will become low irrespective of other inputs. Maintain the low-level state when counting.

LOGIC DIAGRAM (EACH COUNTER)



FUNCTION TABLE (Note 1)

Inputs		Outputs			
$\overline{CK}$	R_D	Q1	Q2	Q3	Q4
X	H	L	L	L	L
↓	L	Count			

Note 1 : ↓ : Change from high to low level
X : Irrelevant

Count number	Q1	Q2	Q3	Q4
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC393FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC393DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0		−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0		4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$−Q1)				20	ns
t_{PHL}					20	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$−Q2)				35	ns
t_{PHL}					35	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$−Q3)				42	ns
t_{PHL}					42	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$−Q4)				50	ns
t_{PHL}					50	ns
t_{PHL}	High-level to low-level output propagation time (R_D−Q1, Q2, Q3, Q4)				28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

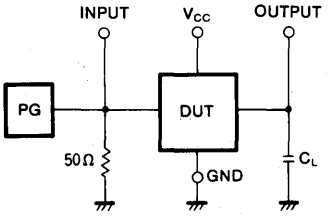
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$–Q1)		2.0			120		150	ns
			4.5			24		30	
			6.0			21		26	
t_{PHL}			2.0			120		150	ns
			4.5			24		30	
			6.0			21		26	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$–Q2)		2.0			190		240	ns
			4.5			38		47	
			6.0			32		40	
t_{PHL}			2.0			190		240	ns
			4.5			38		47	
			6.0			32		40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$–Q3)		2.0			240		300	ns
			4.5			48		60	
			6.0			41		51	
t_{PHL}			2.0			240		300	ns
			4.5			48		60	
			6.0			41		51	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$–Q4)		2.0			290		360	ns
			4.5			58		72	
			6.0			50		62	
t_{PHL}			2.0			290		360	ns
			4.5			58		72	
			6.0			50		62	
t_{PHL}	High-level to low-level output propagation time (R_D–Q1, Q2, Q3, Q4)		2.0			165		210	ns
			4.5			33		41	
			6.0			28		35	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				41				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per counter)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

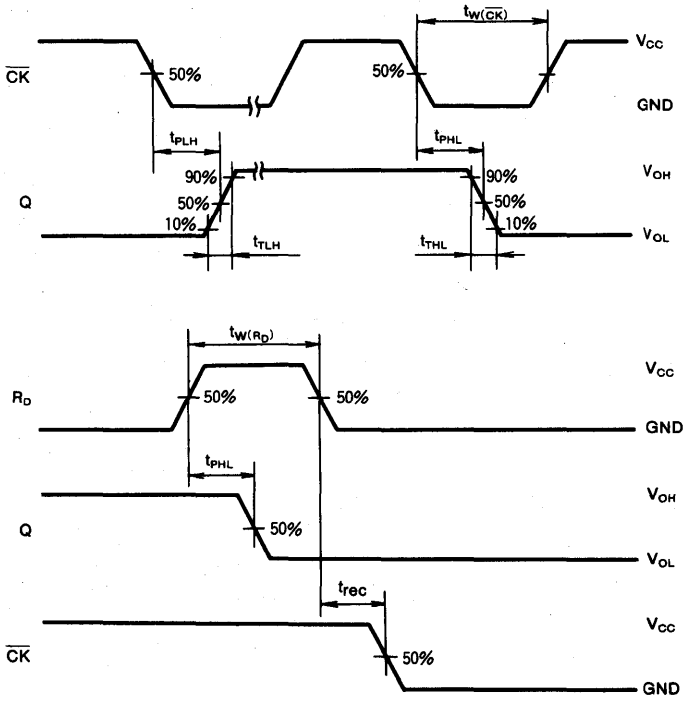
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{w(\overline{CK})}$	Clock pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
$t_{w(R_D)}$	Direct reset pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
t_{rec}	R_D recovery time with respect to $\overline{CK}$		2.0	50			65		ns
			4.5	10			13		
			6.0	9			11		

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC533P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC533 is a semiconductor integrated circuit consisting of eight 3-state output D-type latches with common latch-enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

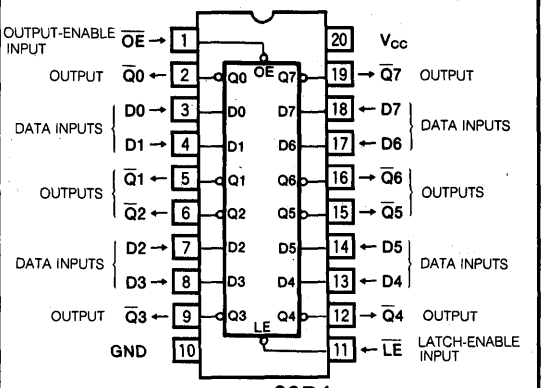
Use of silicon gate technology allows the M74HC533 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS533.

The M74HC533 contains of eight D-type latch with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.

When $\overline{LE}$ is high, the signals of data input D will go through the latch and be output to inverted output $\overline{Q}$. When the state of D changes, the state of $\overline{Q}$ will also change. When $\overline{LE}$ changes from high-level to low-level, the data existing immediately prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected.

PIN CONFIGURATION (TOP VIEW)



20P4
Outline 20P2N
20P2V

When $\overline{OE}$ is high, all outputs $\overline{Q}$ will become high-impedance state.

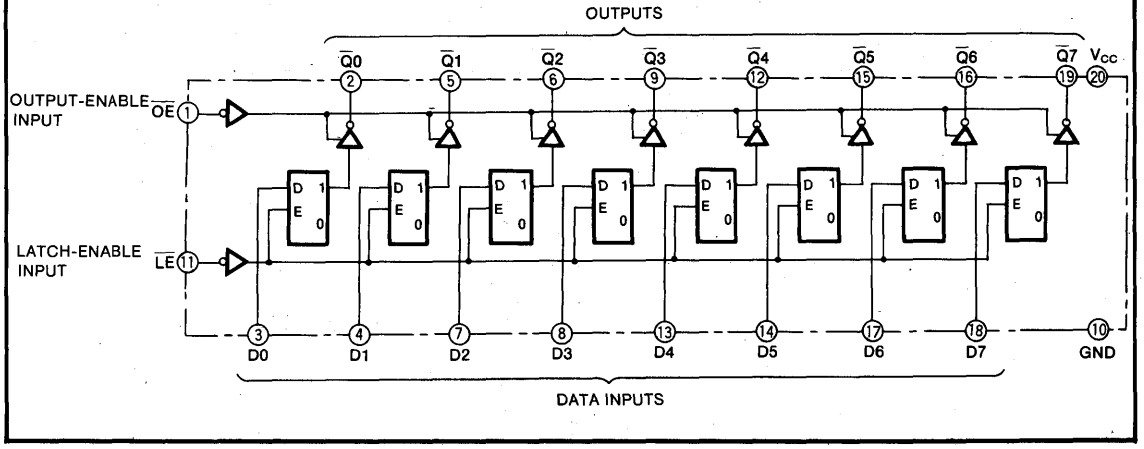
A version of the M74HC533 with the same pin connections and a noninverted output, the M74HC373, is also available.

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}^0$: Output state $\overline{Q}$ before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC533FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC533DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time (D − $\overline{Q}$)				25	ns
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time ($\overline{LE}$ − $\overline{Q}$)				30	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}	($\overline{OE}$ − $\overline{Q}$)				25	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 4)			28	ns
t_{PZH}	($\overline{OE}$ − $\overline{Q}$)				28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

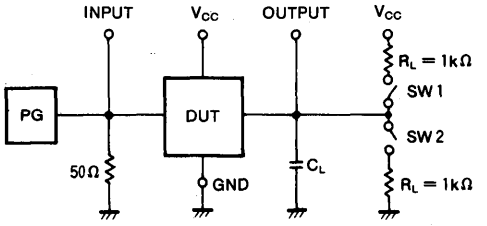
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D− $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PLH}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PHL}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}		C_L = 150pF (Note 4)	2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PHL}			2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				57				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENT (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
				25℃			−40~+85℃	
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Latch enable pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to $\overline{LE}$		2.0	75			90		ns
			4.5	15			18		
			6.0	13			16		
t_h	D hold time with respect to $\overline{LE}$		2.0	50			60		ns
			4.5	10			12		
			6.0	9			11		

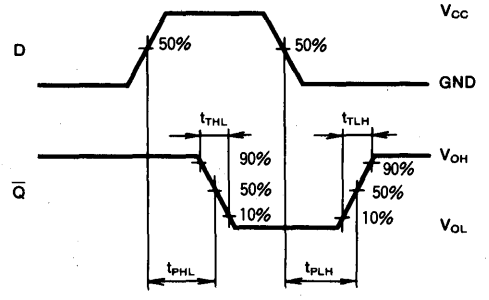
Note 4 : Test Circuit

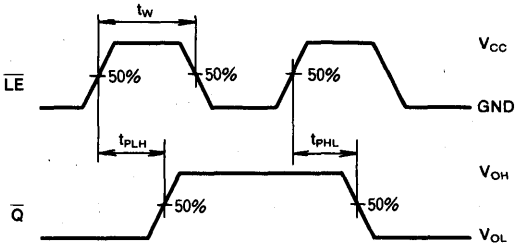


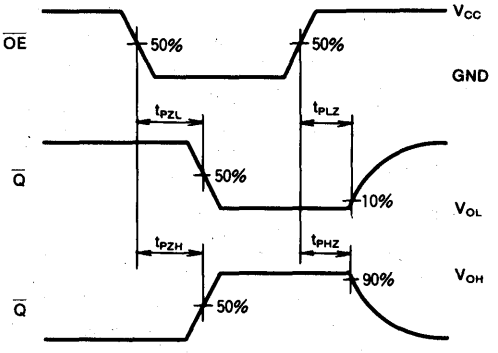
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

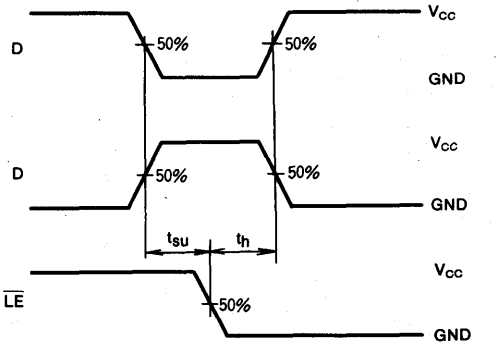
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM









PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC533-1P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC533-1 is a semiconductor integrated circuit consisting of eight 3-state output D-type latches with common latch-enable input and output-enable input.

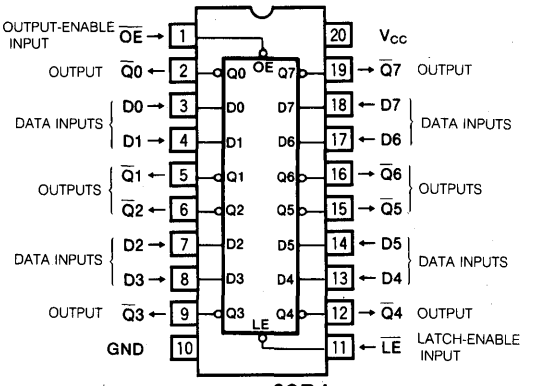
FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 9ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



20P4
Outline 20P2N
20P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC533-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS533.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC533-1 consists of eight D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.

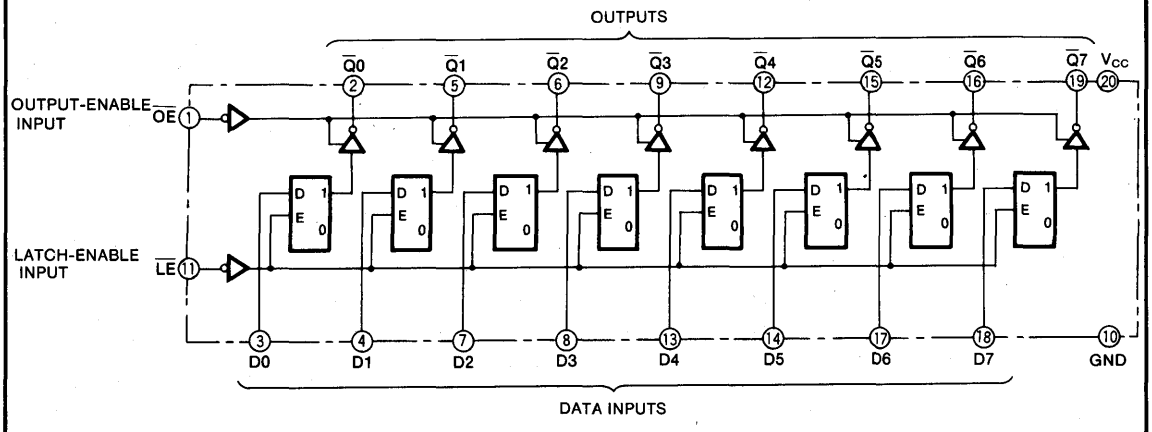
When $\overline{LE}$ is high, the signals of data input D will go through the latch and be output to inverted output $\overline{Q}$. When the state of D changes, the state of $\overline{Q}$ will also change. When $\overline{LE}$ changes from high-level to low-level, the data existing *immediately prior to the change at D will be stored in the* latch.

Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected.

When $\overline{OE}$ is high, all outputs $\overline{Q}$ will become high-impedance state.

A version of the M74HC533-1 with the same pin connections and a noninverted output, the M74HC373-1, is also available.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}^0$: Output state $\overline{Q}$ before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC533-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC533-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.39		0.5	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Q}$)				18	ns
t_{PHL}					18	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − $\overline{Q}$)				21	ns
t_{PHL}					21	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 5 pF (Note 4)			20	ns
t_{PHZ}					20	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)			23	ns
t_{PZH}					23	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Q}$)		2.0			100		125	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		125	
			4.5			20		25	
			6.0			17		21	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − $\overline{Q}$)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)		2.0			125		155	ns
			4.5			25		31	
			6.0			21		26	
t_{PHZ}			2.0			125		155	
			4.5			25		31	
			6.0			21		26	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)		2.0			125		155	ns
			4.5			25		31	
			6.0			21		26	
t_{PZH}			2.0			125		155	
			4.5			25		31	
			6.0			21		26	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)								

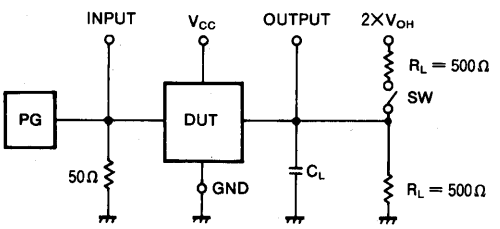
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENT (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W	Latch enable pulse width	2.0	60			75		ns
		4.5	12			15		
		6.0	10			13		
t_{su}	D setup time with respect to $\overline{LE}$	2.0	50			65		ns
		4.5	10			13		
		6.0	9			11		
t_h	D hold time with respect to $\overline{LE}$	2.0	25			30		ns
		4.5	5			6		
		6.0	5			6		

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

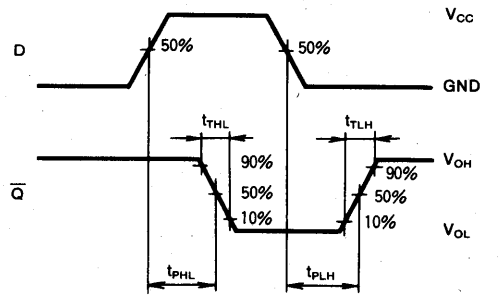
Note 4 : Test Circuit

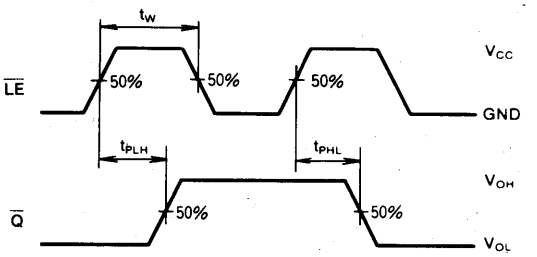


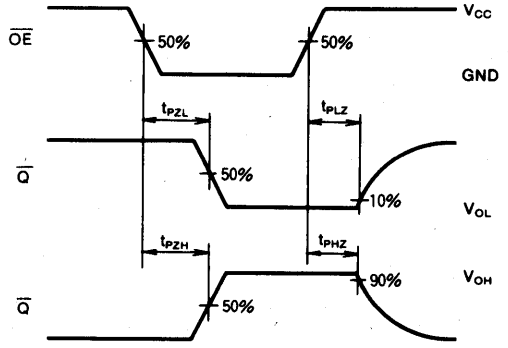
Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

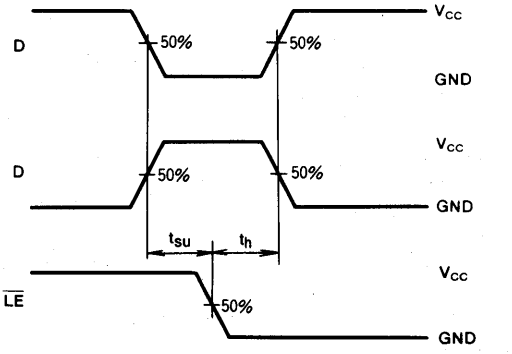
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM









PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HCT533-1P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUT

DESCRIPTION

The M74HCT533-1 is a semiconductor integrated circuit consisting of eight 3-state output D-type latches with common latch-enable input and output-enable input.

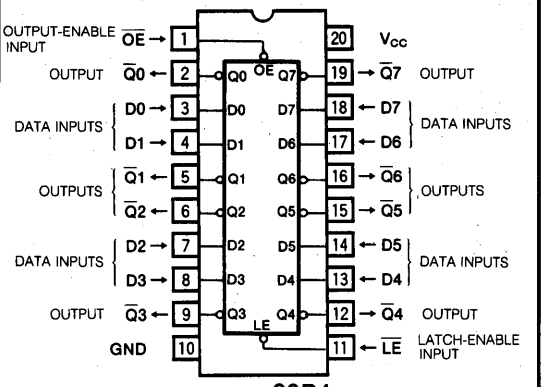
FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 11ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



20P4
Outline 20P2N
20P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT533-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS533.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT533-1 contains of eight D-type latch with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.

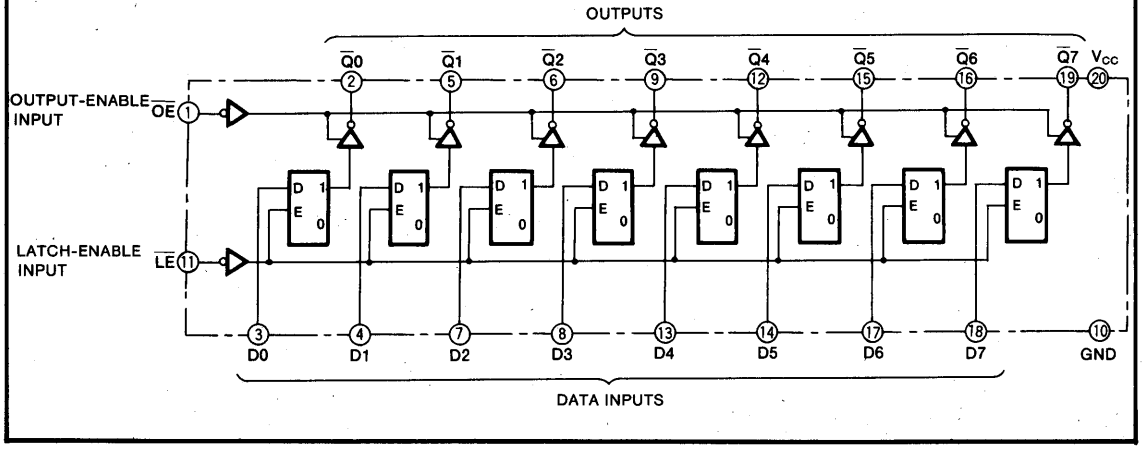
When $\overline{LE}$ is high, the signals of data input D will go through the latch and be output to inverted output $\overline{Q}$. When the state of D changes, the state of $\overline{Q}$ will also change. When $\overline{LE}$ changes from high-level to low-level, the data existing immediately prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected.

When $\overline{OE}$ is high, all outputs $\overline{Q}$ will become high-impedance state.

A version of the M74HCT533-1 with the same pin connections and a noninverted output, the M74HCT373-1, is also available.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUT

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}^0$: Output state $\overline{Q}$ before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HCT533-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HCT533-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUT

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	$V_I = V_{IL}$	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.98			3.84		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.39		0.5	
I_{IH}	High-level input current	$V_I = V_{CC}$				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	
I_{OZH}	Off-state high-level output current	$V_I = V_{IH}$, V_{IL}, $V_O = V_{CC}$				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	$V_I = V_{IH}$, V_{IL}, V_O = GND				−0.5		−5.0	
I_{CC}	Quiescent supply current	$V_I = V_{CC}$, GND, I_O = 0μA				5.0		50.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 5)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				18	ns
t_{PHL}	output propagation time (D − $\overline{Q}$)				18	ns
t_{PLH}	Low-level to high-level and high-level to low-level				21	ns
t_{PHL}	output propagation time ($\overline{LE}$ − $\overline{Q}$)				21	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5pF (Note 5)			20	ns
t_{PHZ}	($\overline{OE}$ − $\overline{Q}$)				20	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 5)			23	ns
t_{PZH}	($\overline{OE}$ − $\overline{Q}$)				23	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12		15	ns
t_{THL}					12		15	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Q}$)				20		25	ns
t_{PHL}					20		25	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − $\overline{Q}$)				23		29	ns
t_{PHL}					23		29	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)				25		31	ns
t_{PHZ}					25		31	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)				25		31	ns
t_{PZH}					25		31	
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	
C_{PD}	Power dissipation capacitance (Note 4)							

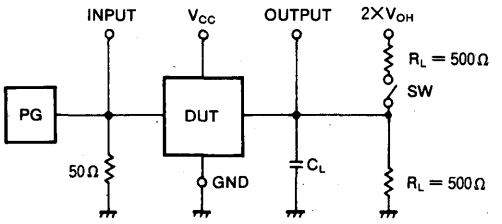
Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUT

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			Min	Typ	Max	Min	Max	
t_w	Latch enable pluse width		12			15		ns
t_{su}	D setup time with respect to $\overline{LE}$		10			13		ns
t_h	D hold time with respect to $\overline{LE}$		5			6		ns

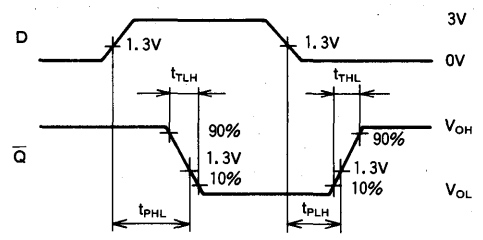
Note 5 : Test Circuit

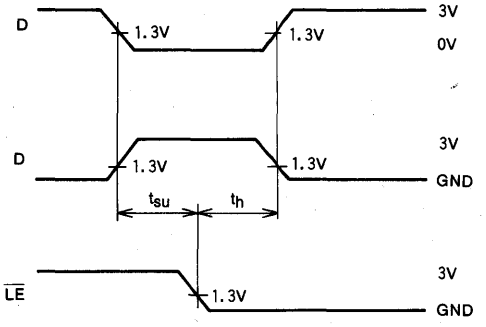


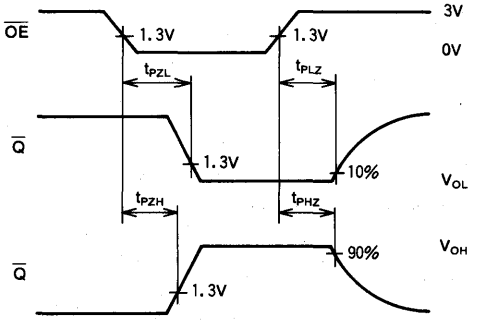
Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

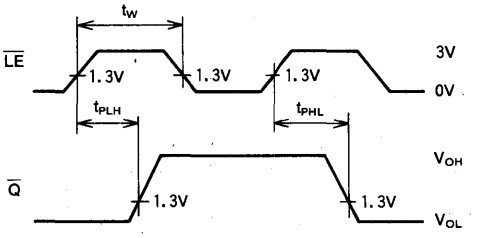
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM









M74HC534P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC534 is a semiconductor integrated circuit consisting of eight edge-triggered 3-state output D-type flip-flops with common clock input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC534 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS534.

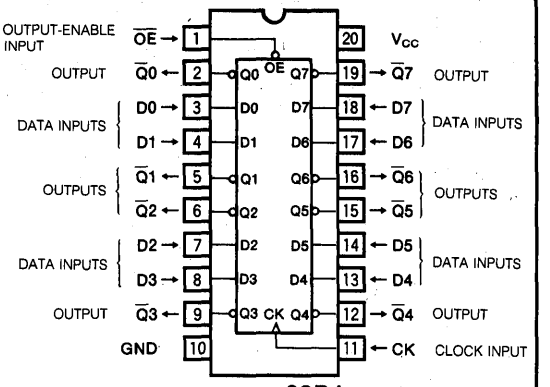
The M74HC534 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{OE}$.

When CK changes from low-level to high-level, the signals just previously input at D is stored in the flip-flop.

When output-enable input $\overline{OE}$ is low, the signals stored in the flip-flop will be output to $\overline{Q}$.

When OE is high, all outputs $\overline{Q}$ will become high-impedance state. The contents stored in the flip-flop are not affected even if $\overline{OE}$ is changed.

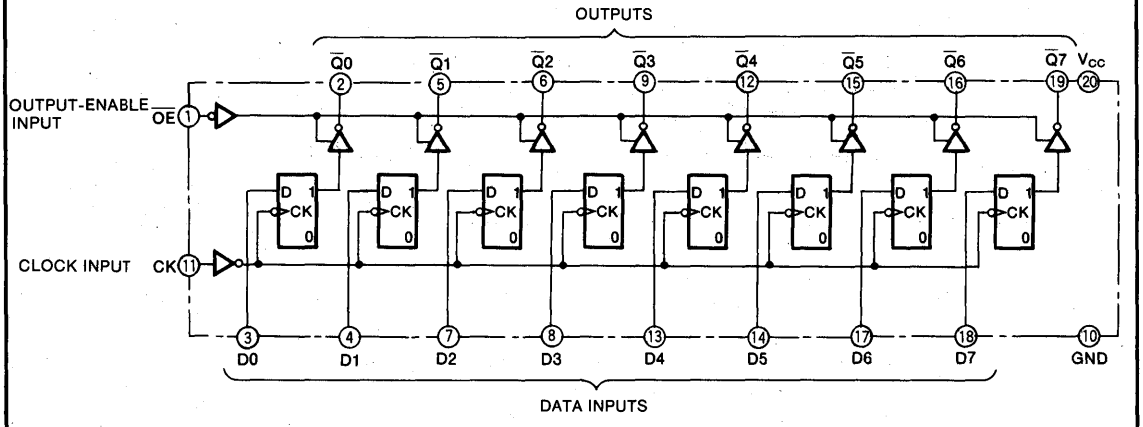
PIN CONFIGURATION (TOP VIEW)



20P4
Outline 20P2N
20P2V

A version of the M74HC534 with the same pin connections and a noninverted output, the M74HC374, is also available.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	L	H
L	↑	H	L
L	L	X	$\overline{Q}^0$
L	H	X	$\overline{Q}^0$
L	↓	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
Z : High impedance
X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC534FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC534DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − $\overline{Q}$)				32	ns
t_{PHL}					32	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

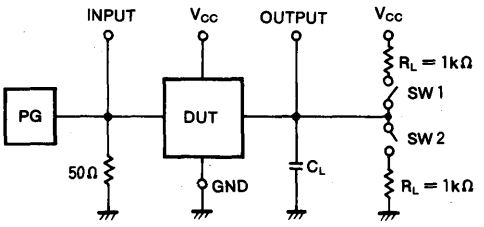
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	6			5		MHz
			4.5	30			24		
			6.0	35			28		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			180		227	ns
			4.5			36		45	
			6.0			31		39	
t_{PHL}			2.0			180		227	ns
			4.5			36		45	
			6.0			31		39	
t_{PLH}		C_L = 150pF (Note 4)	2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				63				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to CK		2.0	75			90		ns
			4.5	15			18		
			6.0	13			16		
t_h	D hold time with respect to CK		2.0	50			60		ns
			4.5	10			12		
			6.0	9			11		

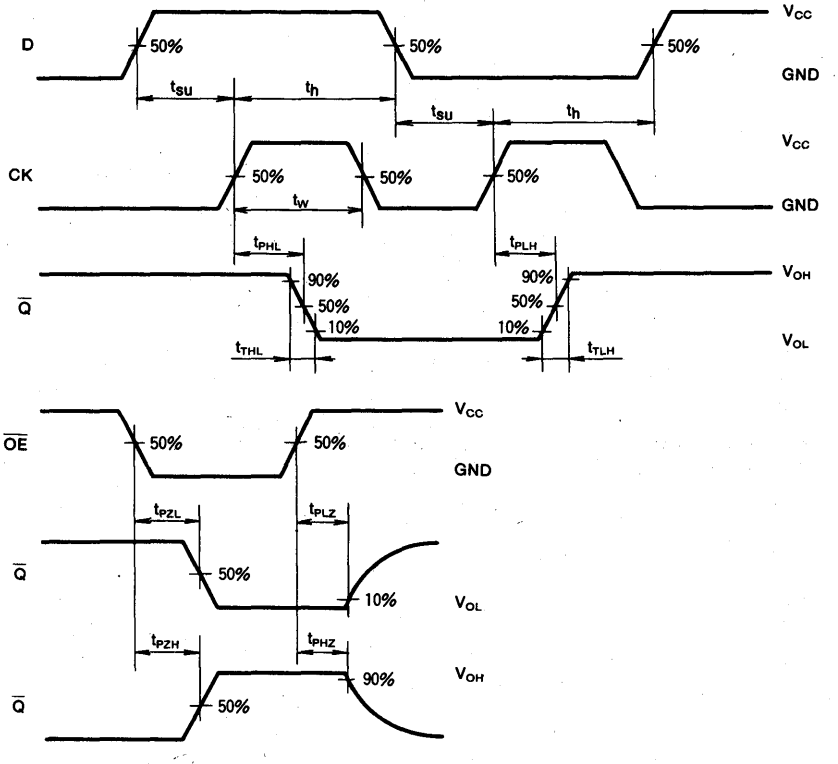
Note 4 : Test Circuit



Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC534-1P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC534-1 is a semiconductor integrated circuit consisting of eight edge-triggered 3-state output D-type flip-flops with common clock input and output-enable input.

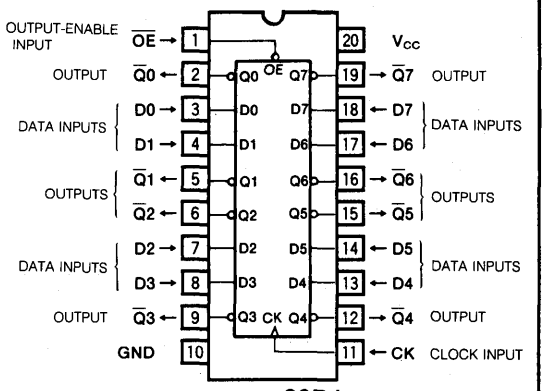
FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: (clock frequency) 60MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC534-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS534.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC534-1 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{OE}$.

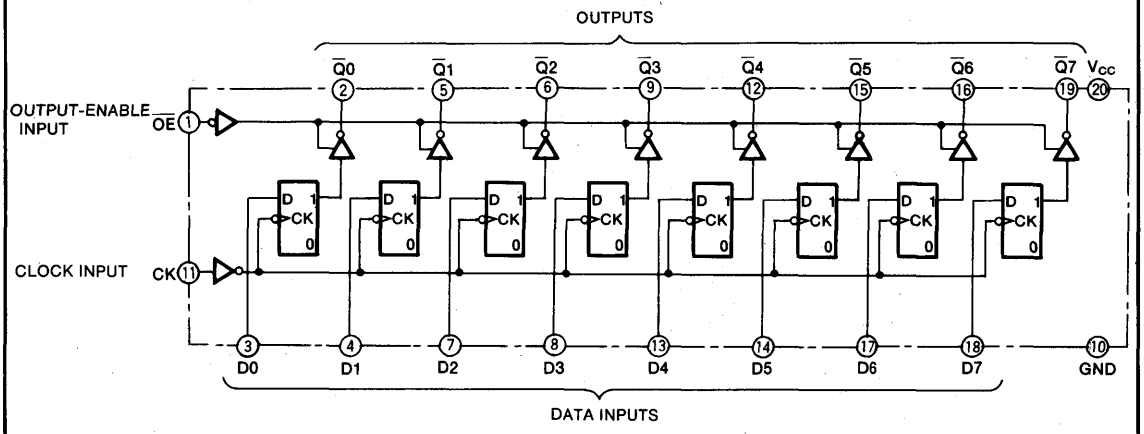
When CK changes from low-level to high-level, the signals just previously input at D stores in the flip-flop.

When output-enable input $\overline{OE}$ is low, the signals stored in the flip-flop will be output to $\overline{Q}$.

When $\overline{OE}$ is high, all outputs $\overline{Q}$ will become high-impedance state. The contents stored in the flip-flop will not be affected even if $\overline{OE}$ is changed.

A version of the M74HC534-1 with the same pin connections and a noninverted output, the M74HC374-1, is also available.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	L	H
L	↑	H	L
L	L	X	$\overline{Q}^0$
L	H	X	$\overline{Q}^0$
L	↓	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
Z : High impedance
X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC534-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC534-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.39		0.5	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	yp	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − $\overline{Q}$)				20	ns
t_{PHL}					20	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 5 pF (Note 4)			20	ns
t_{PHZ}					20	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)			23	ns
t_{PZH}					23	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

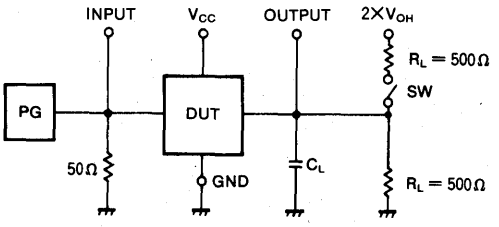
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	6			5		MHz
			4.5	32			26		
			6.0	38			31		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − $\overline{Q}$)		2.0			110		140	ns
			4.5			22		28	
			6.0			19		24	
t_{PHL}			2.0			110		140	
			4.5			22		28	
			6.0			19		24	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)		2.0			125		155	ns
			4.5			25		31	
			6.0			21		26	
t_{PHZ}			2.0			125		155	
			4.5			25		31	
			6.0			21		26	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)		2.0			125		155	ns
			4.5			25		31	
			6.0			21		26	
t_{PZH}			2.0			125		155	
			4.5			25		31	
			6.0			21		26	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)								

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Clock pulse width		2.0	60			75		ns
			4.5	12			15		
			6.0	10			13		
t_{su}	D setup time with respect to CK		2.0	50			65		ns
			4.5	10			13		
			6.0	9			11		
t_h	D hold time with respect to CK		2.0	25			30		ns
			4.5	5			6		
			6.0	5			6		

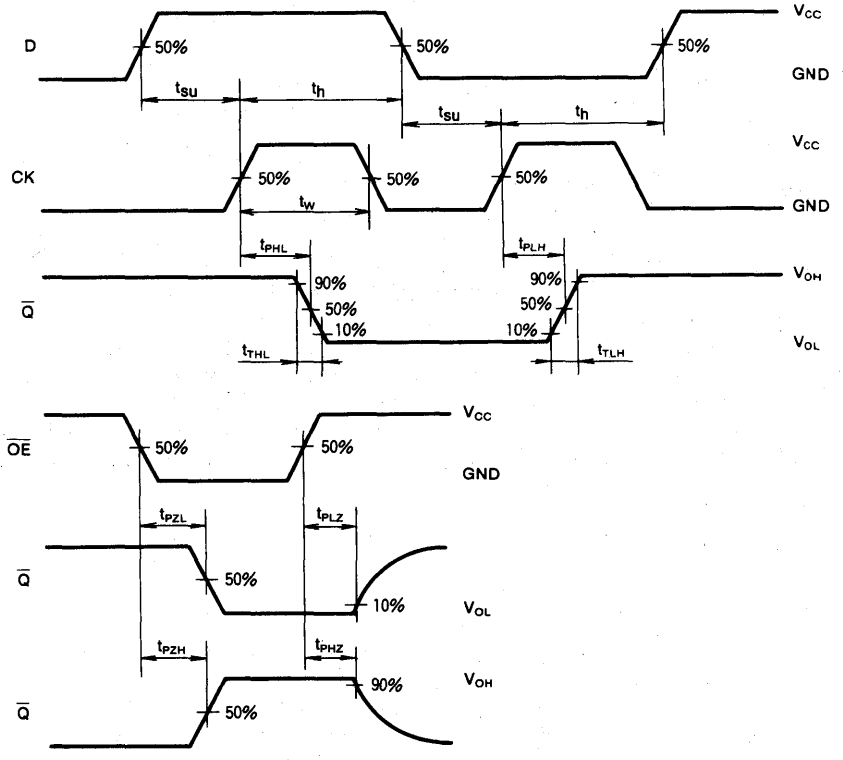
Note 4 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

M74HCT534-1P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT534-1 is a semiconductor integrated circuit consisting of eight edge-triggered 3-state output D-type flip-flops with common clock input and output-enable input.

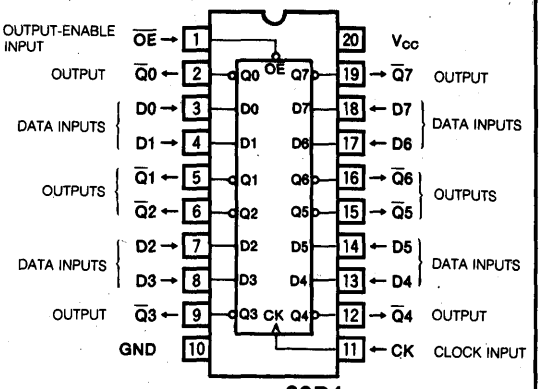
FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: (Clock frequency) 55MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT534-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS534.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT534-1 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{OE}$.

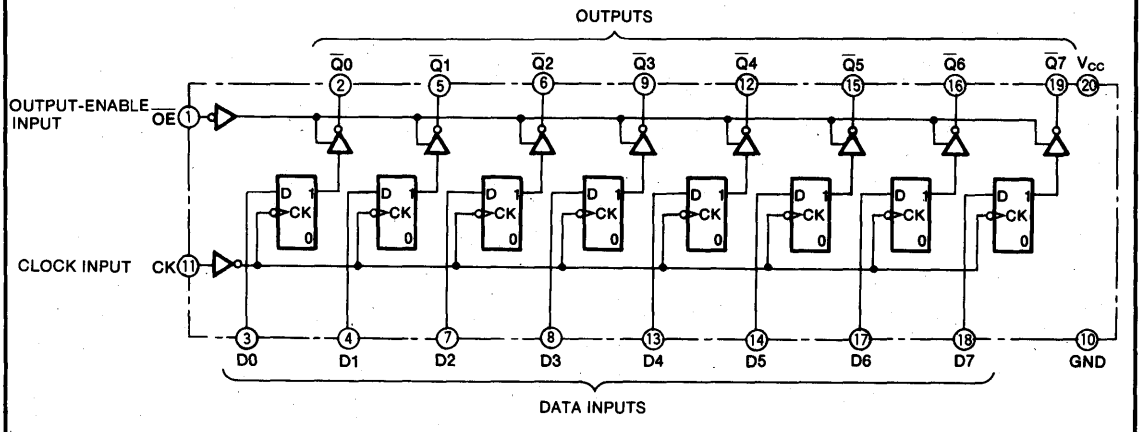
When CK changes from low-level to high-level, the signals just previously input at D is stored in the flip-flop.

When output-enable input $\overline{OE}$ is low, the signals stored in the flip-flop will be output to $\overline{Q}$.

When OE is high, all outputs $\overline{Q}$ will become high-impedance state. The contents stored in the flip-flop are not affected even if $\overline{OE}$ is changed.

A version of the M74HCT534-1 with the same pin connections and a noninverted output, the M74HCT374-1, is also available.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	L	H
L	↑	H	L
L	L	X	$\overline{Q}^0$
L	H	X	$\overline{Q}^0$
L	↓	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
Z : High impedance
X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HCT534-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HCT534-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.39		0.5	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 5)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − $\overline{Q}$)				20	ns
t_{PHL}					20	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 5 pF (Note 5)			20	ns
t_{PHZ}					20	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 5)			23	ns
t_{PZH}					23	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
			Min	Typ	Max	Min	Max	
fmax	Maximum clock frequency	C_L = 50pF (Note 5)	32			26		MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				12		15	ns
t_{THL}					12		15	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − $\overline{Q}$)				22		28	ns
t_{PHL}					22		28	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)				25		31	ns
t_{PHZ}					25		31	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)				25		31	ns
t_{PZH}					25		31	
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	
C_{PD}	Power dissipation capacitance (Note 4)							

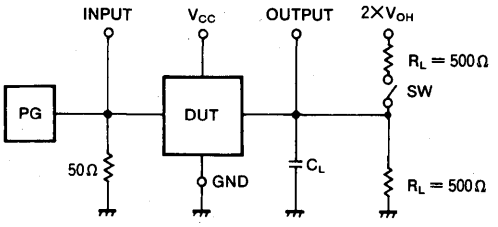
Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			Min	Typ	Max	Min	Max	
t_w	Clock pluse width		12			15		ns
t_{su}	D setup time with respect to CK		10			13		ns
t_h	D hold time with respect to CK		5			6		ns

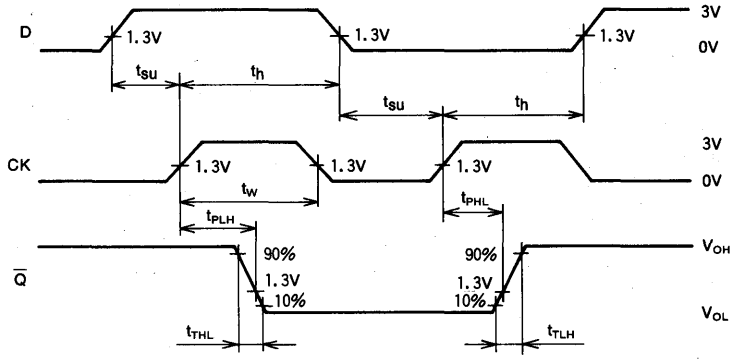
Note 5 : Test Circuit

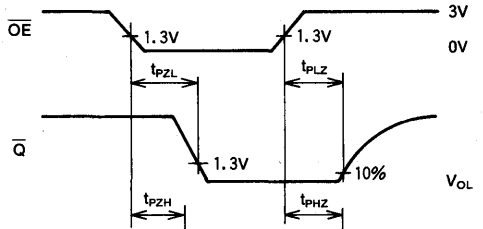


Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC540P/FP/DWP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC540 is a semiconductor integrated circuit consisting of 3-state inverting buffers each with eight independent circuits that share a common enable inputs.

FEATURES

- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC540 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS540.

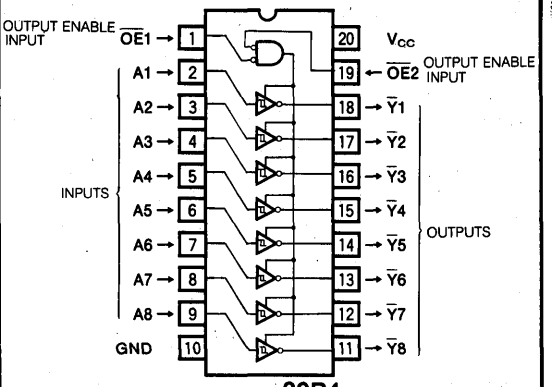
The M74HC540 has hysteresis characteristics in the input circuits and inverting 3-state outputs with a high noise margin.

When the output enable inputs $\overline{OE1}$ and $\overline{OE2}$ are both low, and an input A is low, then the corresponding output $\overline{Y}$ will become high: when A is high, $\overline{Y}$ will become low.

When either $\overline{OE1}$ or $\overline{OE2}$ is high, all outputs will become the high-impedance state, irrespective of A.

The input and output pins are arranged for facilitated board layout (data flow-through pin out).

PIN CONFIGURATION (TOP VIEW)



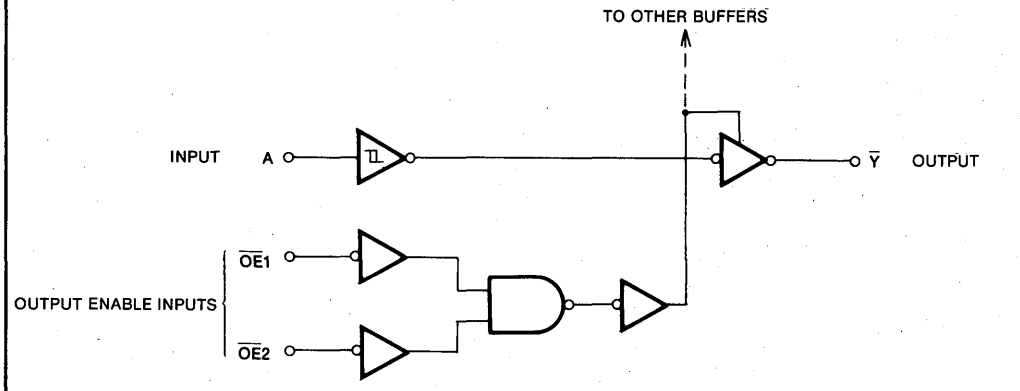
Outline 20P4, 20P2N, 20P2V

FUNCTION TABLE (Note 1)

Inputs			Output
A	$\overline{OE1}$	$\overline{OE2}$	$\overline{Y}$
L	L	L	H
H	L	L	L
X	L	H	Z
X	H	L	Z
X	H	H	Z

Note 1 : Z : High impedance
X : Irrelevant

LOGIC DIAGRAM (EACH BUFFER)



OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC540FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC540DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, I_{OH} = −20μA	2.0	1.9			1.9		V
		V_I = V_{IL}, I_{OH} = −20μA	4.5	4.4			4.4		
		V_I = V_{IL}, I_{OH} = −20μA	6.0	5.9			5.9		
		V_I = V_{IL}, I_{OH} = −6.0mA	4.5	4.18			4.13		
		V_I = V_{IL}, I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	2.0			0.1		0.1	V
		V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	4.5			0.1		0.1	
		V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	6.0			0.1		0.1	
		V_I = V_{IH}, V_{IL}, I_{OL} = 6.0mA	4.5			0.26		0.33	
		V_I = V_{IH}, V_{IL}, I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}	6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND	6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

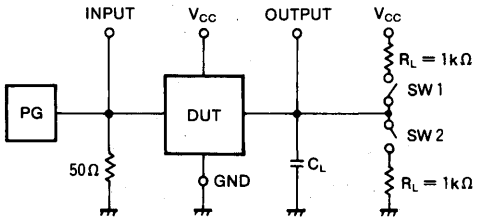
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)				18	ns
t_{PHL}					18	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		126	
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 4)	2.0			150		190	
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		190	
			4.5			30		38	
			6.0			26		32	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				40				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

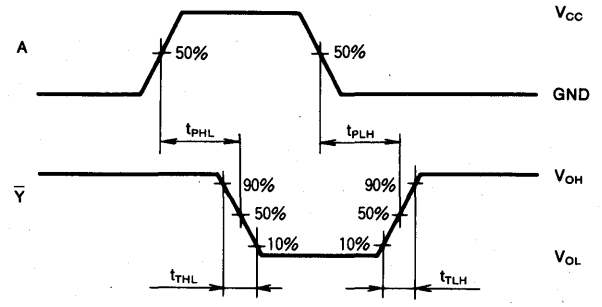
Note 4 : Test Circuit

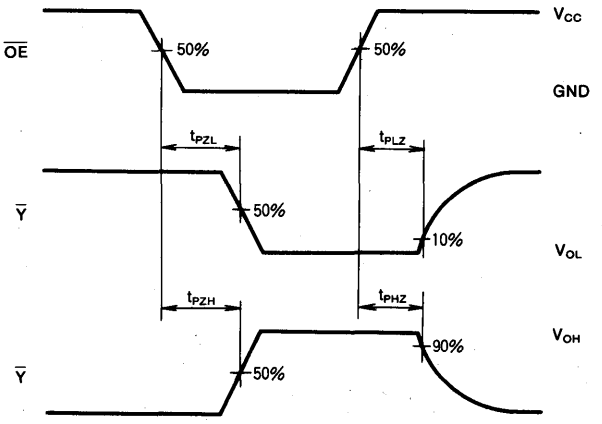


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC541P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC541 is a semiconductor integrated circuit consisting of 3-state non-inverting buffers each with eight independent circuits that share a common enable inputs.

FEATURES

- High-speed: 14ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC541 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS541.

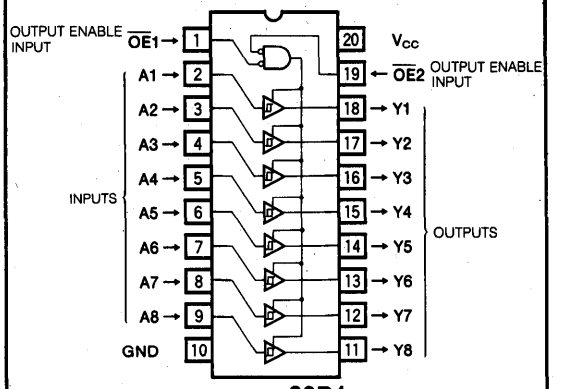
The M74HC541 has hysteresis characteristics in the input circuits and noninverting 3-state outputs with a high noise margin.

When the output enable inputs $\overline{OE1}$ and $\overline{OE2}$ are both low, and an input A is low, then the corresponding output Y will become low; when A is high, Y will become high.

When either $\overline{OE1}$ or $\overline{OE2}$ is high, all outputs will become the high-impedance state, irrespective of A.

The input and output pins are arranged for facilitated board layout (data flow-through pin out).

PIN CONFIGURATION (TOP VIEW)



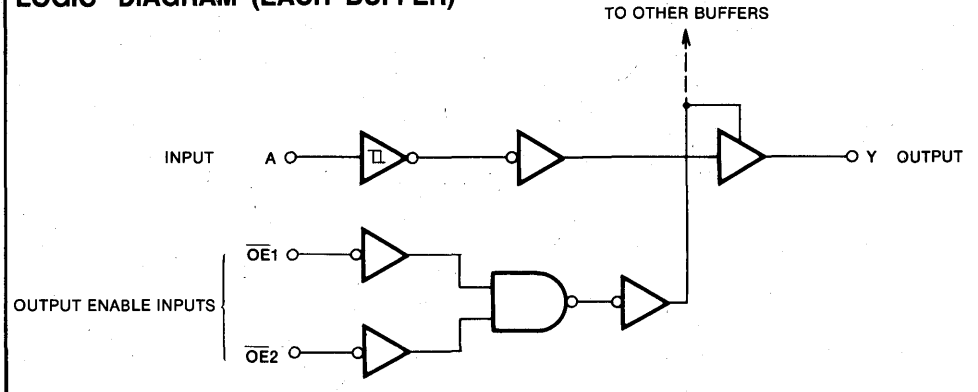
Outline 20P4, 20P2N, 20P2V

FUNCTION TABLE (Note 1)

Inputs			Output
A	$\overline{OE1}$	$\overline{OE2}$	Y
L	L	L	L
H	L	L	H
X	L	H	Z
X	H	L	Z
X	H	H	Z

Note 1 : Z : High impedance
X : Irrelevant

LOGIC DIAGRAM (EACH BUFFER)



OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC541FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC541DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −6.0mA	4.5	4.18			4.13		
		I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IL} ; I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 6.0mA	4.5			0.26		0.33	
		I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}	6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND	6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

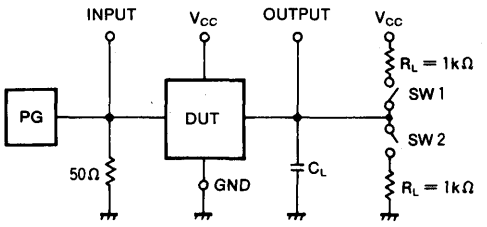
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)				20	ns
t_{PHL}					20	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)	C_L = 50pF (Note 4)	2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
t_{PLH}		C_L = 150pF (Note 4)	2.0			165		208	
			4.5			33		42	
			6.0			28		35	
t_{PHL}			2.0			165		208	
			4.5			33		42	
			6.0			28		35	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				44				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

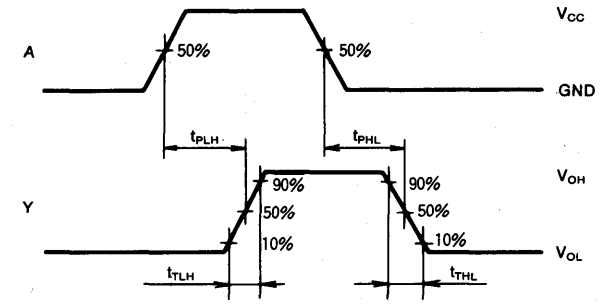
Note 4 : Test Circuit

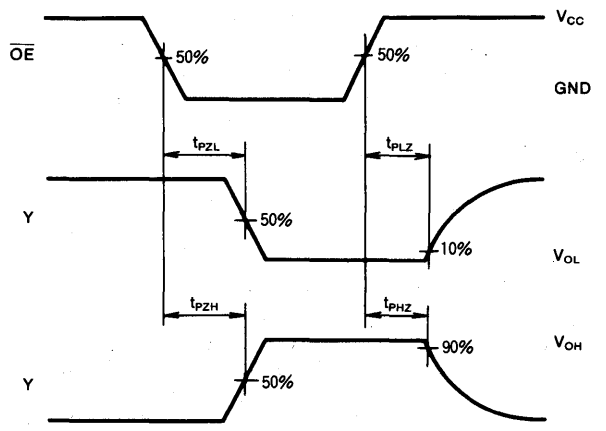


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC563P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC563 is a semiconductor integrated circuit consisting of eight three-state-output D-type latches with common latch-enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC563 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS563.

The M74HC563 consists of eight D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.

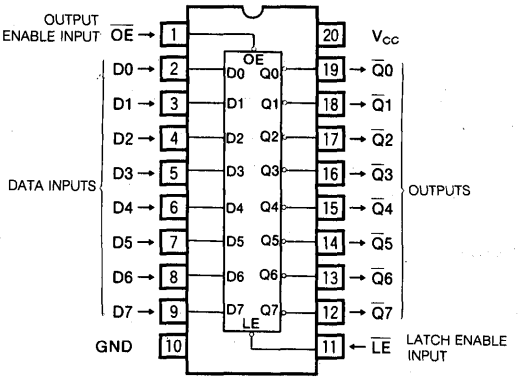
When $\overline{LE}$ is high, the signals of data input D will go through the latch and be output to inverted output $\overline{Q}$. When the state of D changes, the state of $\overline{Q}$ will also change. When $\overline{LE}$ changes from high-level to low-level, the data existing immediately prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected.

When $\overline{OE}$ is high, all outputs $\overline{Q}$ will become high-impedance state.

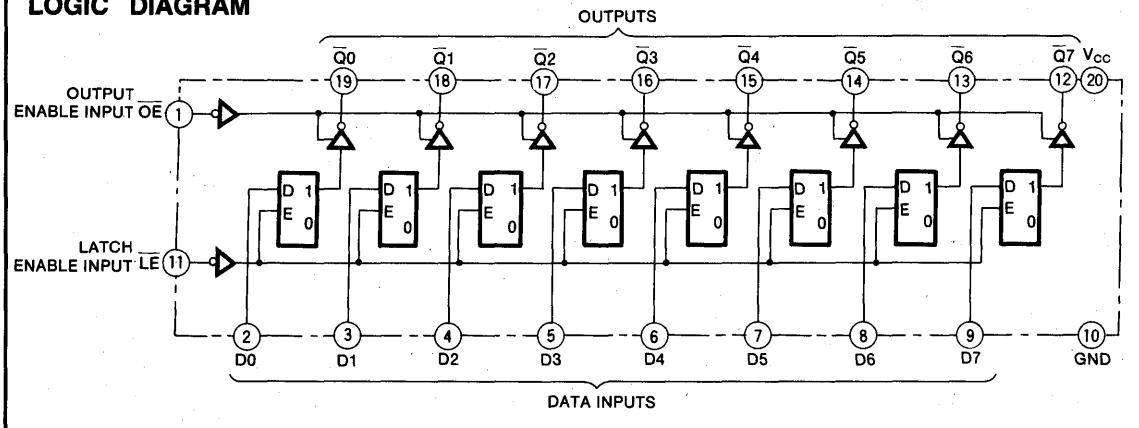
A version of the M74HC563 with the same pin connections and a noninverted output, the M74HC573, is also available.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}^0$: Output state $\overline{Q}$ before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC563FP, T_a = −40~+75℃ and T_a = 75~85℃ are derated at −7mW/℃.
M74HC563DWP, T_a = −40~+80℃ and T_a = 80~85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Q}$)				25	ns
t_{PHL}					25	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − $\overline{Q}$)				30	ns
t_{PHL}					30	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

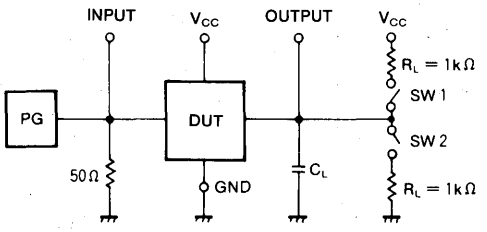
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D− $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PLH}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PHL}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}		C_L = 150pF (Note 4)	2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PHL}			2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Latch enable pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to $\overline{LE}$		2.0	75			90		ns
			4.5	15			18		
			6.0	13			16		
t_h	D hold time with respect to $\overline{LE}$		2.0	50			60		ns
			4.5	10			12		
			6.0	9			11		

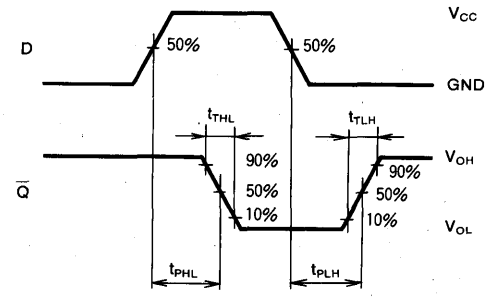
Note 4 : Test Circuit

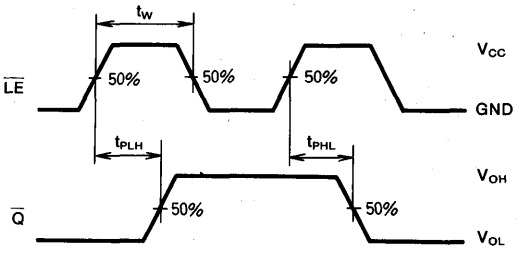


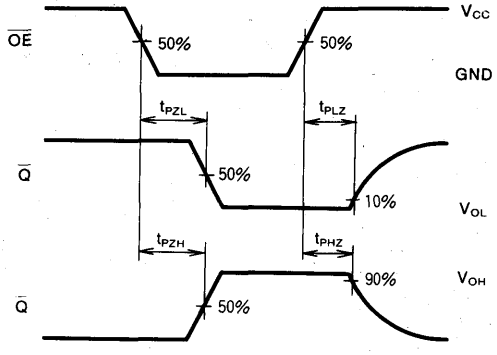
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

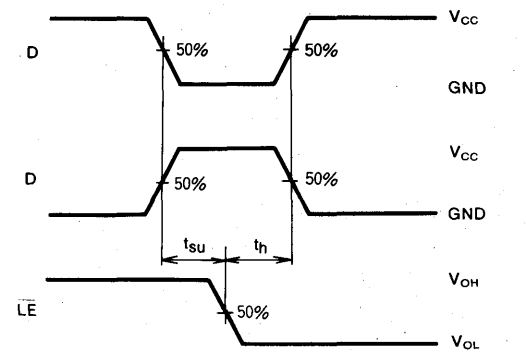
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM









MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC564P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC564 is a semiconductor integrated circuit consisting of eight edge-triggered D-type flip-flops with 3-state outputs, common clock input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: (clock frequency) 40MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC564 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS564.

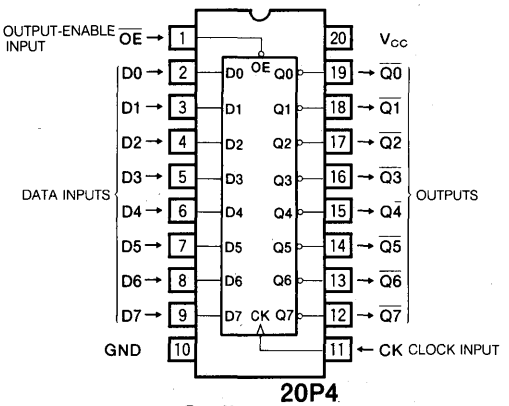
The M74HC564 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{OE}$.

When CK changes from low-level to high-level, the signals just previously input at D stores in the flip-flop.

When output-enable input $\overline{OE}$ is low, the signals stored in the flip-flop will be inverted and output to $\overline{Q}$.

When the $\overline{OE}$ is high, all outputs $\overline{Q}$ will become high impedance state. Even if $\overline{OE}$ is changed, the contents stored in the flip-flop will not be affected.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

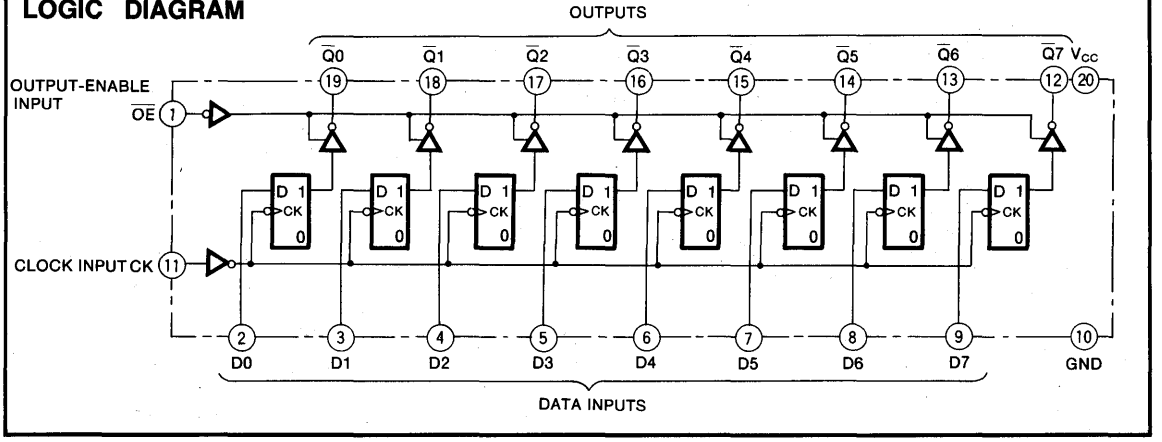
A version of the M74HC564 with the same pin connections and a noninverted output, the M74HC574, is also available.

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	L	H
L	↑	H	L
L	L	X	$\overline{Q}^0$
L	H	X	$\overline{Q}^0$
L	↓	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}^0$: Output state $\overline{Q}$ before CK changed
Z : High impedance
X : Irrelevant
↑ : Change from low-level to high-level
↓ : Change from high-level to low-level

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC564FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC564DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level innput current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − $\overline{Q}$)				32	ns
t_{PHL}					32	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

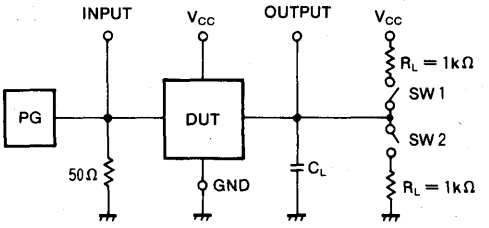
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	6			5		MHz
			4.5	30			24		
			6.0	35			28		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			180		227	
			4.5			36		45	
			6.0			31		39	
t_{PHL}			2.0			180		227	ns
			4.5			36		45	
			6.0			31		39	
t_{PLH}		C_L = 150pF (Note 4)	2.0			230		290	
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	
			4.5			46		58	
			6.0			39		49	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)	2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)								

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Clock pulse width	2.0	80			101		ns
		4.5	16			20		
		6.0	14			17		
t_{su}	D setup time with respect to CK	2.0	75			90		ns
		4.5	15			18		
		6.0	13			16		
t_h	D hold time with respect to CK	2.0	50			60		ns
		4.5	10			12		
		6.0	9			11		

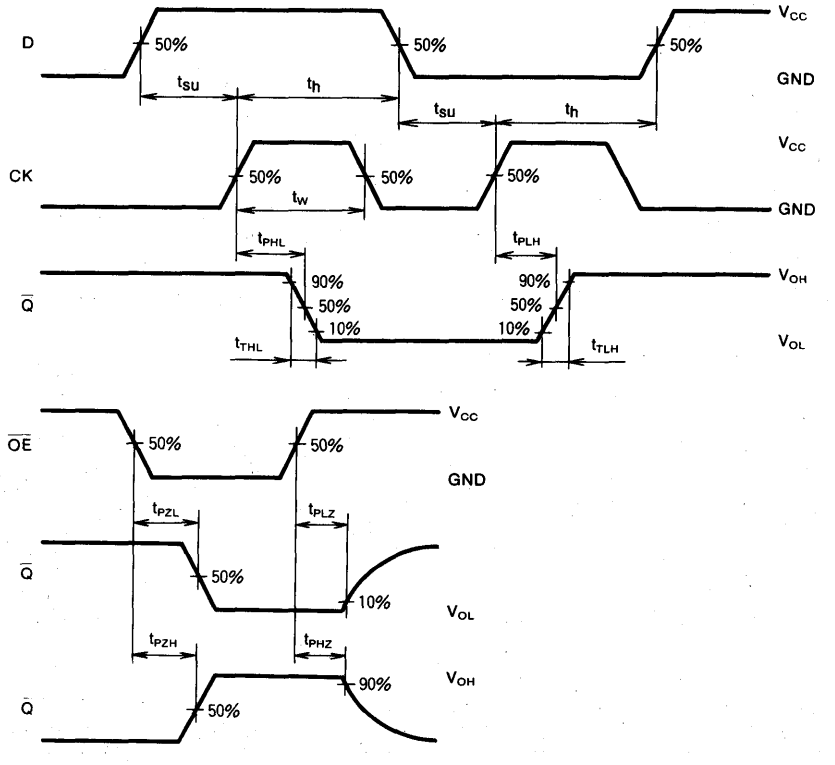
Note 4 : Test Circuit



Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC573P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC573 is a semiconductor integrated circuit consisting of eight 3-state output D-type latches with common enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC573P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS573.

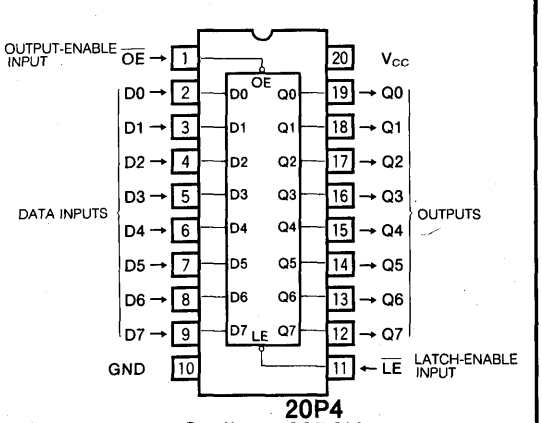
The M74HC573 cosists of eight D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common all circuits.

When $\overline{LE}$ is high, the signals of data input D will go through the latch and be output to Q. When the state of D changes, the state of Q will also change. When $\overline{LE}$ changes from high-level to low-level, the data existing immediatery piror to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected.

When output enable input $\overline{OE}$ is high, all outputs Q will become high impedance state.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

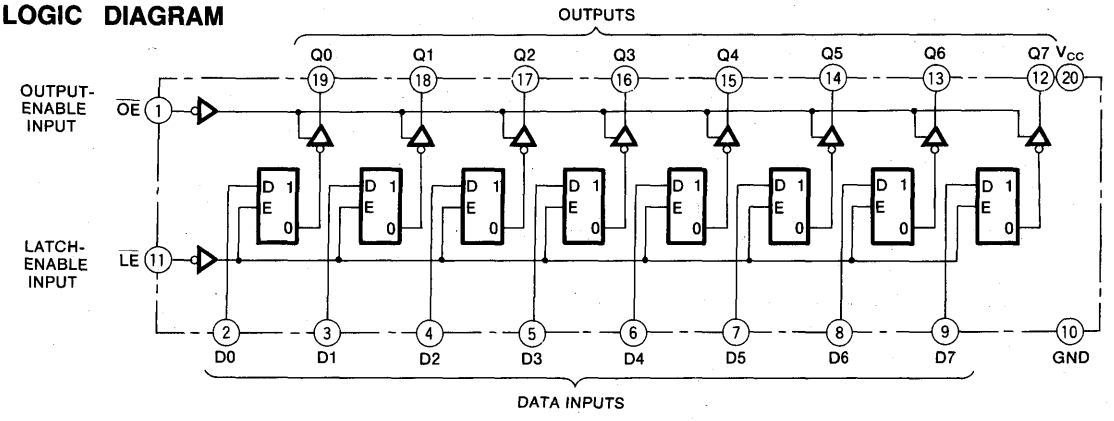
A version of the M74HC573 with the same pin connections and an inverted output, the M74HC563, is also available.

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q^0
H	X	X	Z

Note 1 : Q^0 : Output state Q before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

LOGIC DIAGRAM



OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC573FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC573DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Typ	Max	−40∼+85℃ Min	Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)				19	ns
t_{PHL}					19	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)				20	ns
t_{PHL}					20	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 5 pF (Note 4)			20	ns
t_{PHZ}					20	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)			25	ns
t_{PZH}					25	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

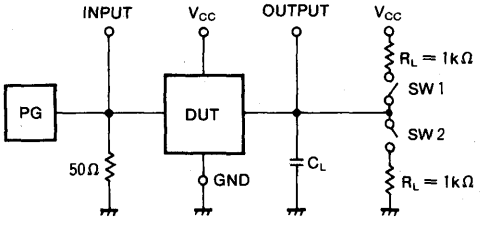
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)	C_L = 50pF (Note 4)	2.0			110		138	ns
			4.5			22		28	
			6.0			19		24	
t_{PHL}			2.0			110		138	
			4.5			22		28	
			6.0			19		24	
t_{PLH}		C_L = 150pF (Note 4)	2.0			150		188	
			4.5			30		38	
			6.0			26		33	
t_{PHL}			2.0			150		188	
			4.5			30		38	
			6.0			26		33	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)	C_L = 50pF (Note 4)	2.0			115		143	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		143	
			4.5			23		29	
			6.0			20		25	
t_{PLH}		C_L = 150pF (Note 4)	2.0			155		194	
			4.5			31		47	
			6.0			27		34	
t_{PHL}			2.0			155		194	
			4.5			31		47	
			6.0			27		34	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			125		156	ns
			4.5			25		31	
			6.0			21		27	
t_{PHZ}			2.0			125		156	
			4.5			25		31	
			6.0			21		27	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
t_{PZH}			2.0			140		175	
			4.5			28		35	
			6.0			24		30	
t_{PZL}		C_L = 150pF (Note 4)	2.0			180		225	
			4.5			36		45	
			6.0			31		39	
t_{PZH}			2.0			180		225	
			4.5			36		45	
			6.0			31		39	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)								

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Latch enable pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to $\overline{LE}$		2.0	75			95		ns
			4.5	15			19		
			6.0	13			16		
t_h	D hold time with respect to $\overline{LE}$		2.0	25			31		ns
			4.5	5			6		
			6.0	4			5		

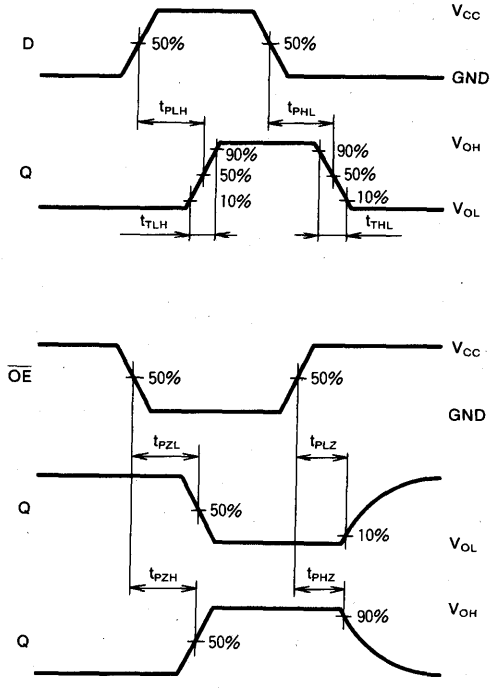
Note 4 : Test Circuit

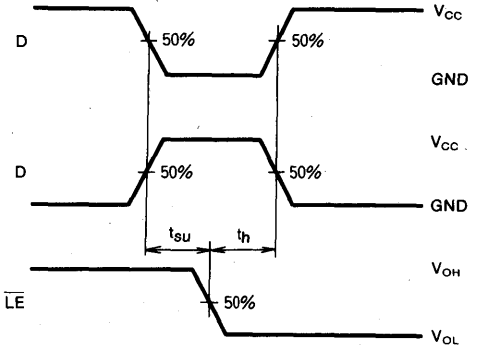


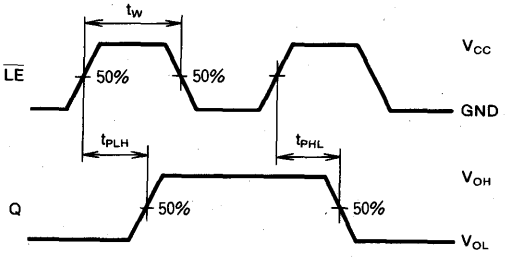
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC574P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC574 is a semiconductor integrated circuit consisting of eight edge-triggered D-type flip-flops with 3-state outputs, common clock input and output-enable input.

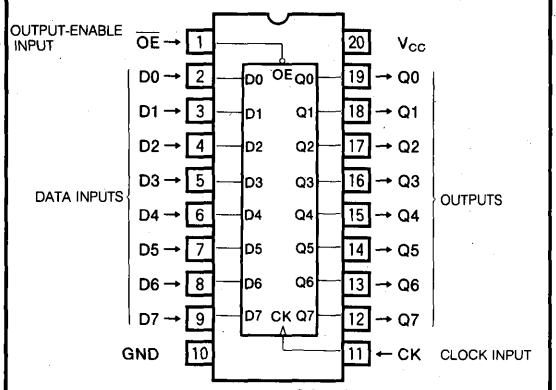
FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: (clock frequency) 65MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC574 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS574.

The M74HC574 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{OE}$.

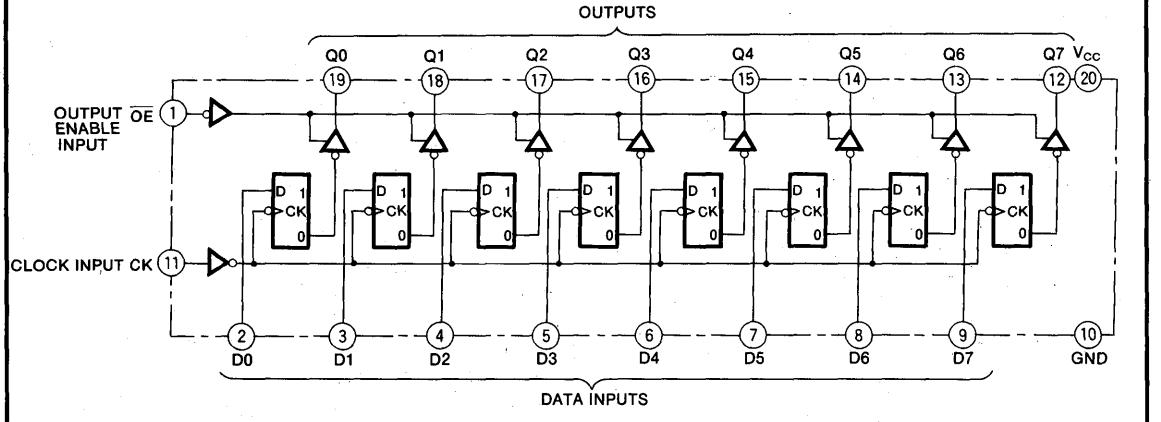
When CK changes from low-level to high-level, the signals just previously input at D stores in the flip-flop.

When output-enable input $\overline{OE}$ is low, the signals stored in the flip-flop will be output to Q.

When $\overline{OE}$ is high, all outputs Q will become high impedance state. Even if $\overline{OE}$ is changed, the contents stored in the flip-flop will not be affected.

A version of the M74HC574 with the same pin connections and an inverted output, the M74HC564, is also available.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q^0
L	H	X	Q^0
L	↓	X	Q^0
H	X	X	Z

Note 1 : Q^0: Output state Q before CK changed
Z : High impedance
X : Irrelevant
↑ : Change from low-level to high-level
↓ : Change from high-level to low-level

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC574FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC574DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 6.0mA	4.5		0.26		0.33	
			I_{OL} = 7.8mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0		−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0		0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0		−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0		4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				32	ns
t_{PHL}					32	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

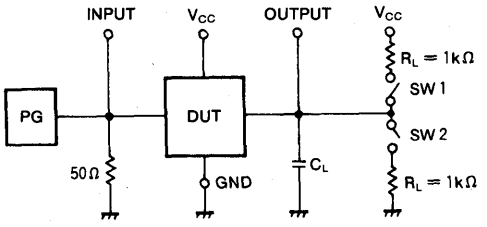
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency		2.0	6			5		MHz
			4.5	30			24		
			6.0	35			28		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)	C_L = 50pF (Note 4)	2.0			180		227	ns
			4.5			36		45	
			6.0			31		39	
t_{PHL}			2.0			180		227	ns
			4.5			36		45	
			6.0			31		39	
t_{PLH}		C_L = 150pF (Note 4)	2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to CK		2.0	75			90		ns
			4.5	15			18		
			6.0	13			16		
t_h	D hold time with respect to CK		2.0	50			60		ns
			4.5	10			12		
			6.0	9			11		

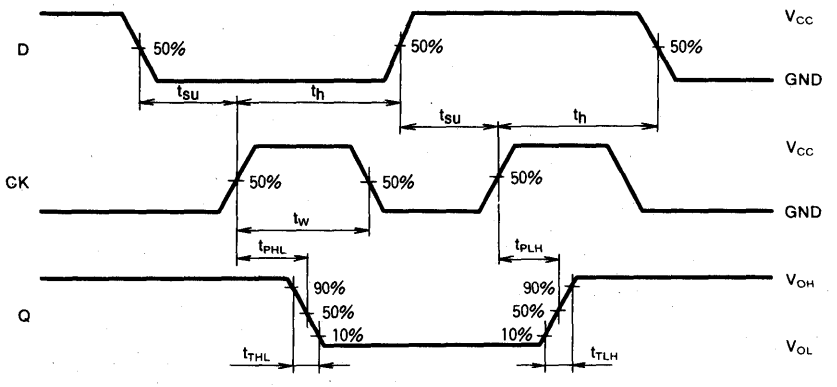
Note 4 : Test Circuit

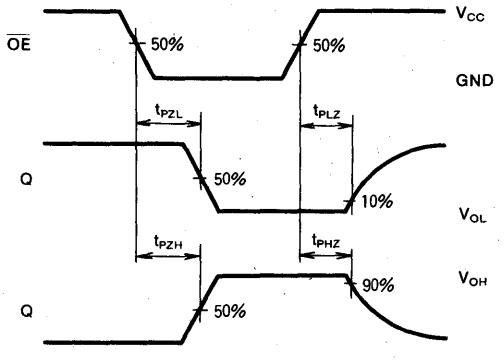


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

M74HC595P/FP/DP

8-BIT SERIAL-INPUT/SERIAL-OR PARALLEL-OUTPUT SHIFT REGISTER WITH LATCHED 3-STATE OUTPUTS

DESCRIPTION

The M74HC595 is a semiconductor integrated circuit consisting of an 8-bit serial input/parallel output shift register with 3-state output latch.

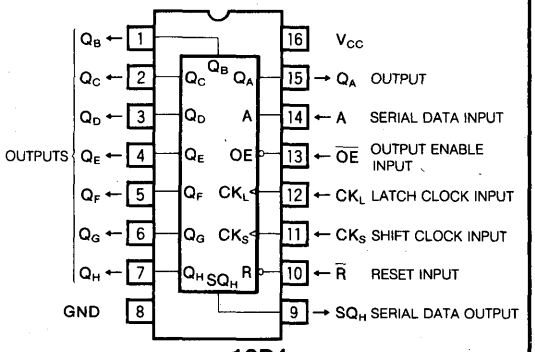
FEATURES

- High-speed: (clock frequency) 30MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads (Q_A–Q_H)
  10 74LSTTL loads (SQ_H)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N
16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC595 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS595.

Each bit of shift register consists of two flip flops with independent clocks for shift and latch.

The clock inputs contain independent shift clock input CKs and latch clock input CK_L. Shift and latch operations take place when the inputs change from low-level to high-level.

Serial data input A is data input of the first shift register. When A is high and a pulse is applied to CKs, the high-level signal will be shifted in order. When A is low and a pulse is applied to CKs, the low-level signal will be shifted in order.

When a pulse is applied to CK_L, the contents of the shift register existing at that time will be stored in the latch register and appear at outputs Q_A through Q_H. Q_A through Q_H are buffered 3-state outputs.

To extend the number of bits, serial data output SQ_H is used to output the eighth bit of the shift register.

By connecting CKs and CK_L, the shift register state delayed by 1 clock cycle is output at Q_A through Q_H.

When reset input $\overline{R}$ is low, shift register and SQ_H will be reset. To reset Q_A through Q_H to low-level, CK_L must be changed from low-level to high-level after the shift register is reset by $\overline{R}$.

When output-enable input $\overline{OE}$ is high, Q_A through Q_H will becom high impedance state, but SQ_H is not changed. Even if $\overline{OE}$ is changed, shift operation is not affected.

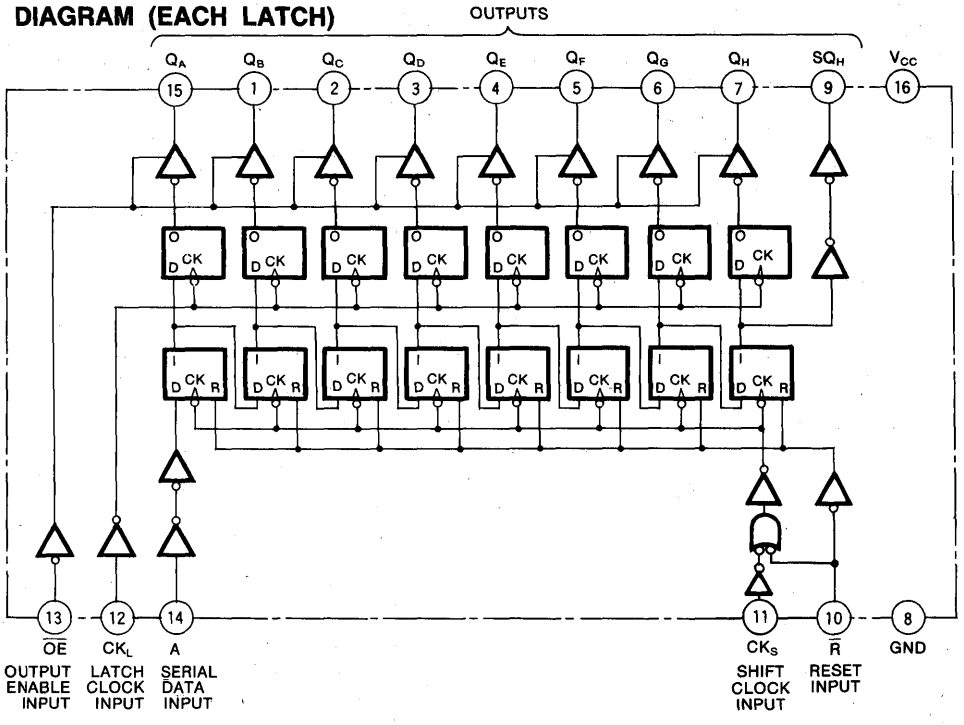
FUNCTION TABLE (Note 1)

Operation mode		Inputs					Outputs								Serial data output SQ_H
		$\overline{R}$	CK_S	CK_L	A	$\overline{OE}$	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G	Q_H	
Reset	Shift t_1	L	X	X	X	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	L
	Latch t_2	X	X	↑	X	L	L	L	L	L	L	L	L	L	L
Shift latch operation	Shift t_1	H	↑	X	H	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	q_G^0
	Latch t_2	H	X	↑	X	L	H	q_A^0	q_B^0	q_C^0	q_D^0	q_E^0	q_F^0	q_G^0	q_G^0
	Shift t_1	H	↑	X	L	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	q_G^0
	Latch t_2	H	X	↑	X	L	L	q_A^0	q_B^0	q_C^0	q_D^0	q_E^0	q_F^0	q_G^0	q_G^0
3 -state		X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	q_H

Note 1. ↑ : Change from low-level to high-level
Q^0 : Output state Q before clock input is changed
X : Irrelevant
q^0 : Contents of shift register before clock input changed
q : Contents of shift register
t_1, t_2 : t_2 is set after t_1 is set
Z : High impedance

8-BIT SERIAL-INPUT/SERIAL-OR PARALLEL-OUTPUT SHIFT REGISTER WITH LATCHED 3-STATE OUTPUTS

LOGIC DIAGRAM (EACH LATCH)



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5∼+7.0	V
V_I	Input voltage			−0.5∼V_{CC}+0.5	V
V_O	Output voltage			−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current		V_I < 0V	−20	mA
			V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current		V_O < 0V	−20	mA
			V_O > V_{CC}	20	
I_O	Output current per output pin	Q_A∼Q_H		±35	mA
		SQ_H		±25	
I_{CC}	Supply/GND current		V_{CC}, GND	±75	mA
P_d	Power dissipation		(Note 2)	500	mW
Tstg	Storage temperature range			−65∼+150	℃

Note 2 : M74HC595FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC595DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

MITSUBISHI ELECTRIC

8-BIT SERIAL-INPUT/SERIAL-OR PARALLEL-OUTPUT SHIFT REGISTER WITH LATCHED 3-STATE OUTPUTS

ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Test conditions		Limits					Unit
					25℃			−40～+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage		V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage		V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	Q_A～Q_H	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
				I_{OH} = −20μA	4.5	4.4			4.4		
				I_{OH} = −20μA	6.0	5.9			5.9		
				I_{OH} = −6.0mA	4.5	4.18			4.13		
				I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	Q_A～Q_H	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
				I_{OL} = 20μA	4.5		0.1		0.1	
				I_{OL} = 20μA	6.0		0.1		0.1	
				I_{OL} = 6.0mA	4.5		0.26		0.33	
				I_{OL} = 7.8mA	6.0		0.26		0.33	
V_{OH}	High-level output voltage	SQ_H	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
				I_{OH} = −20μA	4.5	4.4			4.4		
				I_{OH} = −20μA	6.0	5.9			5.9		
				I_{OH} = −4.0mA	4.5	4.18			4.13		
				I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	SQ_H	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
				I_{OL} = 20μA	4.5		0.1		0.1	
				I_{OL} = 20μA	6.0		0.1		0.1	
				I_{OL} = 4.0mA	4.5		0.26		0.33	
				I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current		V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current		V_I = 0V		6.0		−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current		V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0		0.5		5.0	μA
I_{OZL}	Off-state low-level output current		V_I = V_{IH}, V_{IL}, V_O = GND		6.0		−0.5		−5.0	μA
I_{CC}	Quiescent supply current		V_I = V_{CC}, GND, I_O = 0μA		6.0		4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time (SQ_H)	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time (Q_A − Q_H)	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_S − SQ_H)	C_L = 15pF (Note 4)			35	ns
t_{PHL}					35	
t_{PHL}	High-level to low-level output propagation time ($\overline{R}$ − SQ_H)				30	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_L − Q_A～Q_H)	C_L = 50pF (Note 4)			30	ns
t_{PHL}					30	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q_A～Q_H)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level (OE − Q_A～Q_H)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	

8-BIT SERIAL-INPUT/SERIAL-OR PARALLEL-OUTPUT SHIFT REGISTER WITH LATCHED 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-leveland high-level to low-level output transition time (SQ_H)		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{TLH}	Low-level to high-level and high-level to low-level output propagation time (Q_A~Q_H)		2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($CK_S - SQ_H$)		2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PHL}			2.0			210		265	
			4.5			42		53	
			6.0			36		45	
t_{PHL}	High-level and low-level output propagation time ($\overline{R} - SQ_H$)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($CK_L - Q_A$~Q_H)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	
			4.5			35		44	
			6.0			30		37	
t_{PLH}		C_L = 150pF (Note 4)	2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PHL}			2.0			225		284	
			4.5			45		57	
			6.0			38		48	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE} - Q_A$~Q_H)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	

8-BIT SERIAL-INPUT/SERIAL-OR PARALLEL-OUTPUT SHIFT REGISTER WITH LATCHED 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q_A~Q_H)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q_A~Q_H)	C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance (Q_A~Q_H)					15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				287				pF

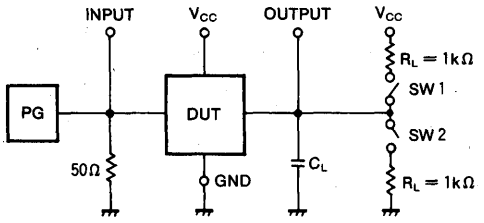
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits						Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{W(CK_S)}$	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{W(CK_L)}$	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{W(\overline{R})}$	Reset pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	A setup time with respect to CK_S		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_{su}	CK_S setup time with respect to CK_L		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	A hold time with respect to CK_S		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		
t_{rec}	R recovery time with respect to CK_S		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		

8-BIT SERIAL-INPUT/SERIAL-OR PARALLEL-OUTPUT SHIFT REGISTER WITH LATCHED 3-STATE OUTPUTS

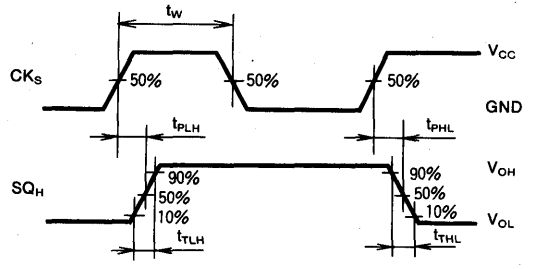
Note 4 : Test Circuit

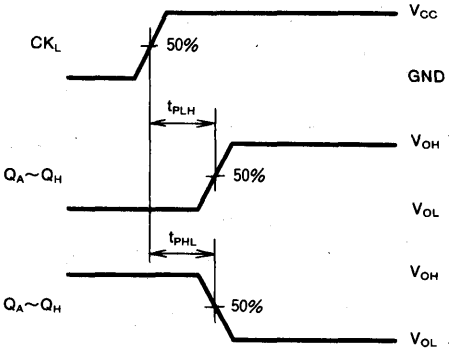


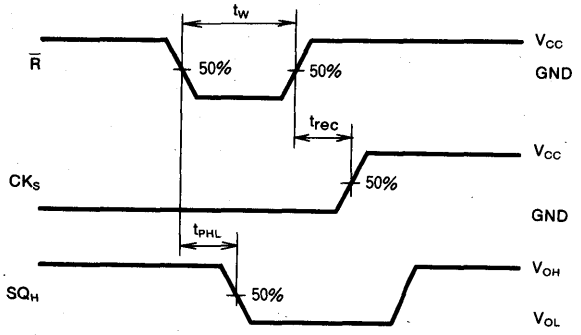
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

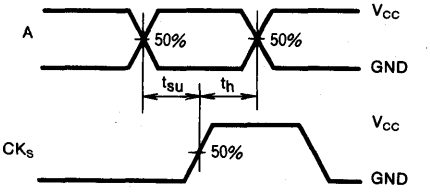
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

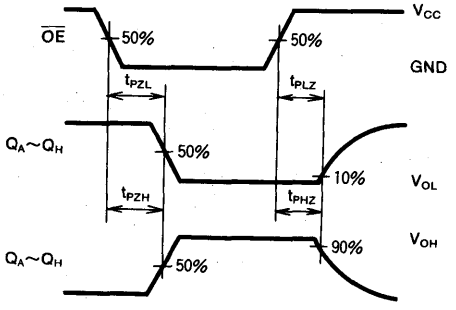
TIMING DIAGRAM

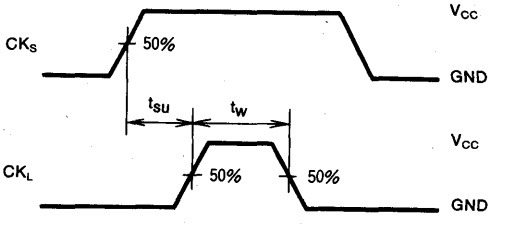












MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC597P/FP/DP

8-BIT SERIAL-OR PARALLEL -INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH INPUT LATCH

DESCRIPTION

The M74HC597 is a semiconductor integrated circuit consisting of an 8-bit serial-input/parallel-input with latch, serial-output shift register.

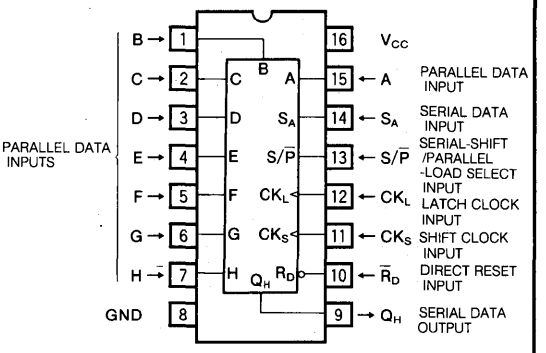
FEATURES

- Serial-input/parallel-input with latch, serial output
- High-speed: 30MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

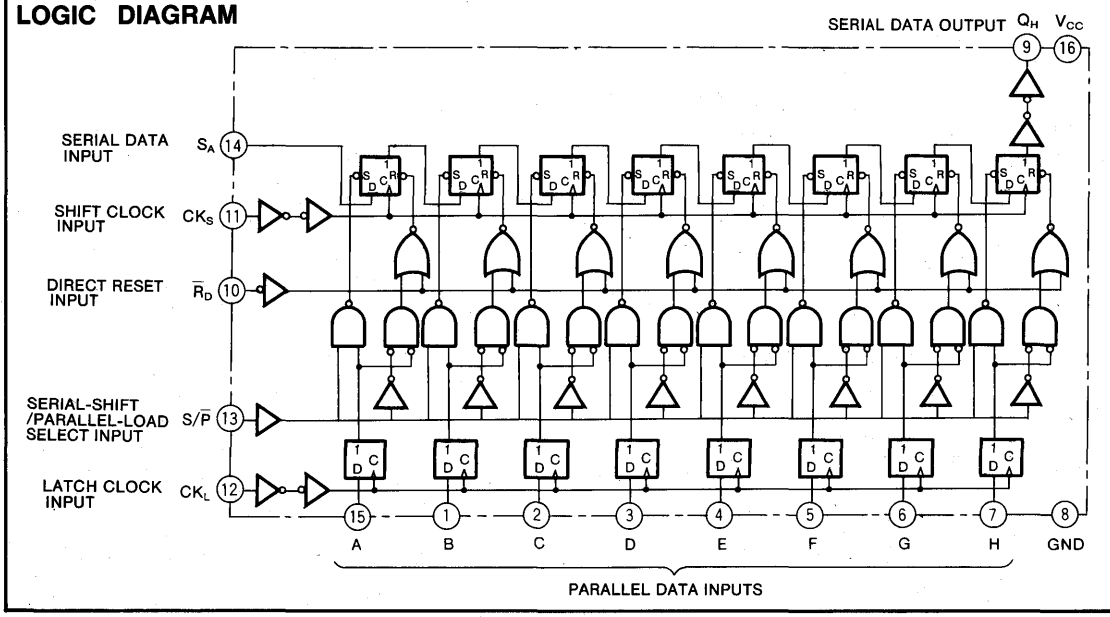
Use of silicon gate technology allows the M74HC597 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS597.

The mode select input S/$\overline{P}$ is used to select either serial or parallel input. When S/$\overline{P}$ is high and serial data input S_A is applied, the data in the 8-bit flip flops will be shifted serially in sync with the clock pulse CK_S. When the latch clock pulse CK_L is applied, parallel data applied at A~H will be stored in the input latch without affecting the contents of the shift register.

Next, S/$\overline{P}$ is low and the parallel data latched at A~H will be loaded in sync with the next clock pulse input at CK_L. Serial data transfer is suppressed while parallel data is loaded. Shift or load operations are performed at the rising edge when CK_L changes from low-level to high-level.

When direct reset input $\overline{R_D}$ is low, the shift register will be reset and serial data output Q_H will become low, irrespective of other inputs.

LOGIC DIAGRAM



8-BIT SERIAL-OR PARALLEL -INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH INPUT LATCH

FUNCTION TABLE (Note 1)

Inputs						Output	
$\overline{R_D}$	$S/\overline{P}$	CK_L	CK_S	S_A	A~H	Q_H	
L	X	X	X	X	X	L	Shift register is reset. Input latch is not affected.
H	H	↑	X	X	a-h	no change	Parallel data is stored in the input latch. Shift register is not affected.
H	L	↑	X	X	a-h	h	Parallel data is stored in the input latch and loaded to the shift register.
H	L	X	X	X	X	h_L	Parallel data stored in the input latch is loaded in the shift register.
H	H	X	↑	L	X	Q_{Gn}	Low-level data is serially shifted into the shift register.
H	H	X	↑	H	X	Q_{Gn}	High-level data is serially shifted into the shift register.
H	H	↑	X	L, H	a-h	Q_{Gn}	Serial data is shifted into the shift register and parallel data is stored in the input latch.
H	H	X	↑	L, H	a-h	Q_{Gn}	

Note 1 : ↑ : Change from low to high level
X : Irrelevant
a~h indicate logic level of inputs A~H.
h_L indicates logic level stored in the input latch H.
Q_{Gn} indicates logic level of data in the shift register G before shift clock changed.

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65~+150	℃

Note 2 : M74HC597FP, T_a = −40~+70℃ and T_a = 70~85℃ are derated at −6mW/℃.
M74HC597DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

8-BIT SERIAL-OR PARALLEL -INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH INPUT LATCH

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltnge	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				35	ns
t_{PHL}	output propagation time (CK_L − Q_H)				35	ns
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (CK_S − Q_H)				30	ns
t_{PHL}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R}_D$ − Q_H)				30	ns
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (S/$\overline{P}$ − Q_H)				30	ns

8-BIT SERIAL-OR PARALLEL -INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH INPUT LATCH

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($CK_L - Q_H$)		2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PHL}			2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($CK_S - Q_H$)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}	High-level to low-level output propagation time ($\overline{R}_D - Q_H$)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($S/\overline{P} - Q_H$)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

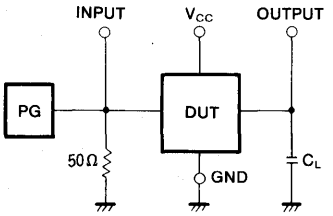
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

8-BIT SERIAL-OR PARALLEL -INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH INPUT LATCH

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Pulse width (CK_S, CK_L, $S/\overline{P}$, $\overline{R_D}$)		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{su(CK_L)}$	A~H setup time with respect to CK_L		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
$t_{su(CK_S)}$	S_A setup time with respect to CK_S		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
$t_{su(CK_S)}$	$S/\overline{P}$ setup time with respect to CK_S		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
$t_{h(CK_L)}$	A~H hold time with respect to CK_L		2.0	25			32		ns
			4.5	5			6		
			6.0	4			5		
$t_{h(CK_S)}$	S_A hold time with respect to CK_S		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		
$t_{h(CK_S)}$	$S/\overline{P}$ hold time with respect to CK_S		2.0						ns
			4.5						
			6.0						
$t_{rec(\overline{R_D})}$	$\overline{R_D}$ recovery time with respect to CK_S		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		

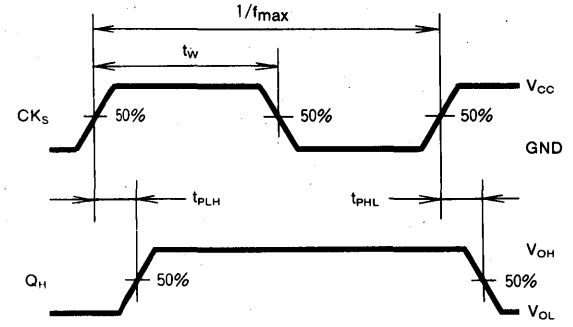
Note 4 : Test Circuit

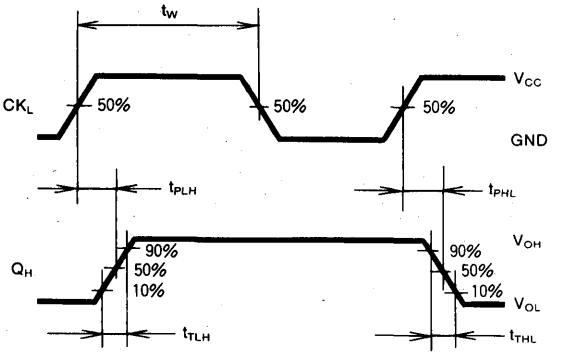


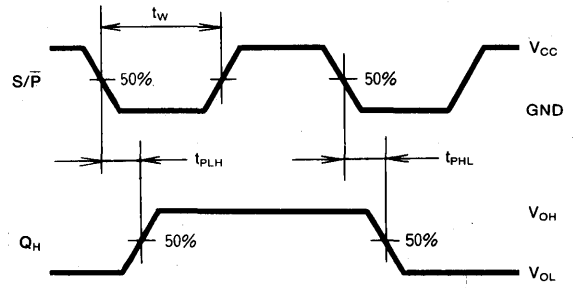
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

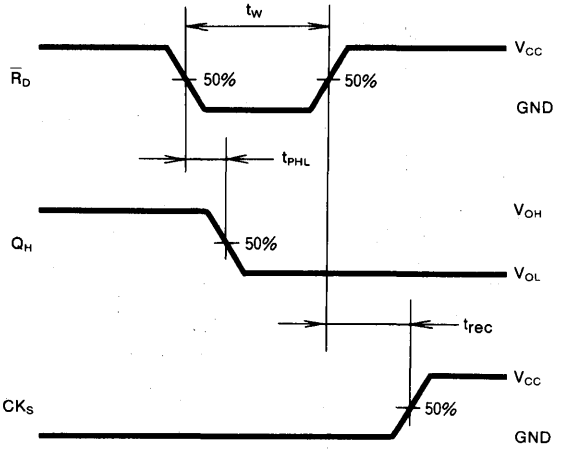
8-BIT SERIAL-OR PARALLEL -INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH INPUT LATCH

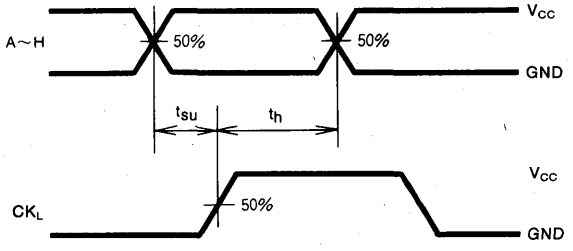
TIMING DIAGRAM

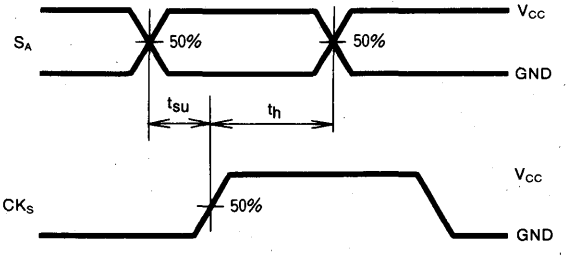


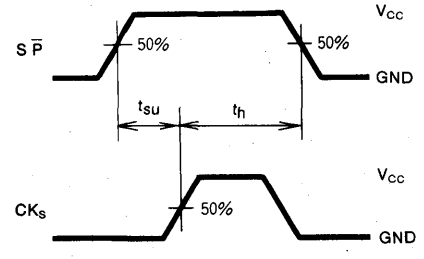












M74HC640P/FP/DWP

OCTAL 3-STATE INVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC640 is a semiconductor integrated circuit consisting of eight transceivers with inverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13 ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC640 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS640.

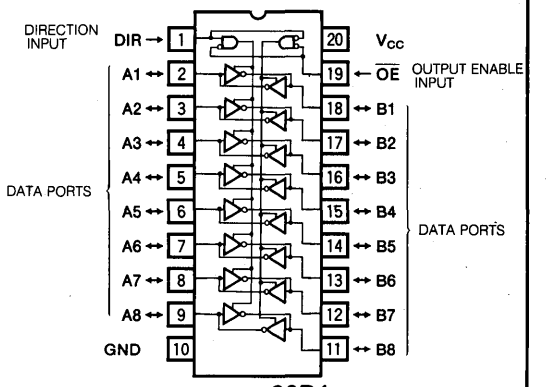
Two buffers with 3-state inverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

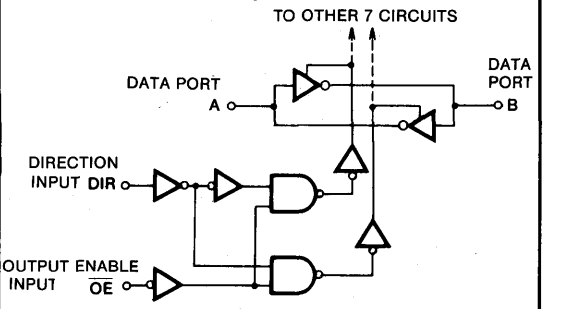
When output enable input $\overline{OE}$ is high, A and B will both become a high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

LOGIC DIAGRAM (EACH TRANSCEIVER)



FUNCTION TABLE (Note 1)

Inputs		Outputs	
$\overline{OE}$	DIR	A	B
L	L	$\overline{O}$	I
L	H	I	$\overline{O}$
H	X	Z	Z

Note 1 : I : Input terminal
$\overline{O}$: Output terminal (inverted output)
Z : High impedance (A and B are separated)
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC640FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC640DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −6.0mA	4.5	4.18			4.13		
		I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 6.0mA	4.5			0.26		0.33	
		I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}	6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND	6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

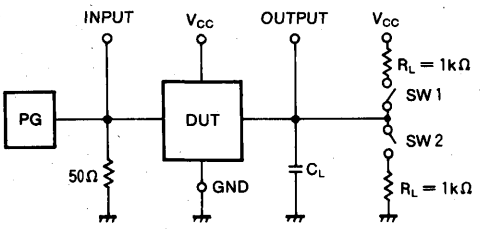
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				21	ns
t_{PHL}					21	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 5 pF (Note 4)			42	ns
t_{PHZ}					42	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)			42	ns
t_{PZH}					42	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)	C_L = 50pF (Note 4)	2.0			110		140	ns
			4.5			22		28	
			6.0			19		24	
t_{PHL}			2.0			110		140	ns
			4.5			22		28	
			6.0			19		24	
t_{PLH}		C_L = 150pF (Note 4)	2.0			195		245	ns
			4.5			39		49	
			6.0			34		43	
t_{PHL}			2.0			195		245	ns
			4.5			39		49	
			6.0			34		43	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)	2.0			172		208	ns
			4.5			43		52	
			6.0			41		50	
t_{PHZ}			2.0			172		208	ns
			4.5			43		52	
			6.0			41		50	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)	2.0			184		224	ns
			4.5			46		56	
			6.0			41		50	
t_{PZH}			2.0			184		224	ns
			4.5			46		56	
			6.0			41		50	
t_{PZL}		C_L = 150pF (Note 4)	2.0			216		260	ns
			4.5			54		65	
			6.0			47		57	
t_{PZH}			2.0			216		260	ns
			4.5			54		65	
			6.0			47		57	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				53				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

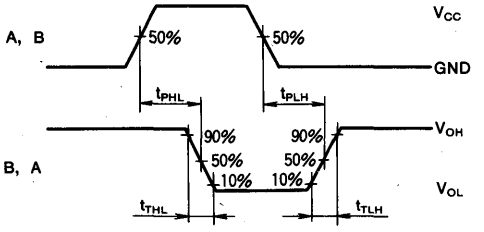
Note 4 : Test Circuit

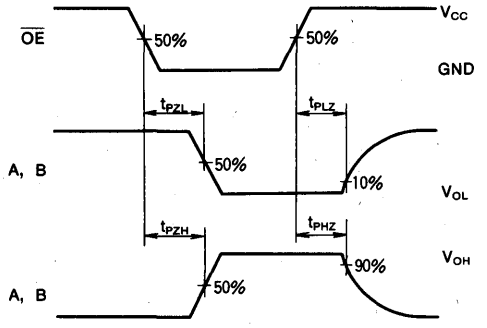


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC640-1P/FP/DWP

OCTAL 3-STATE INVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC640-1 is a semiconductor integrated circuit consisting of eight bus transceivers with inverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 8 ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC640-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS640.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

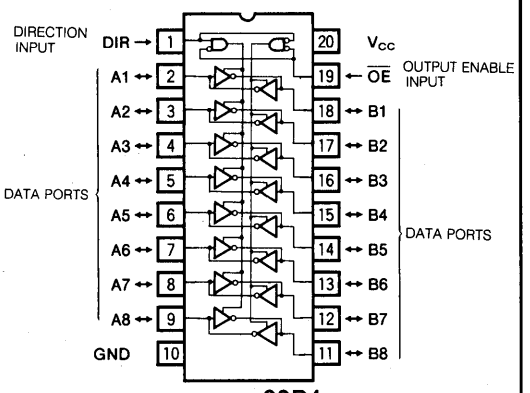
Two buffers with 3-state inverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

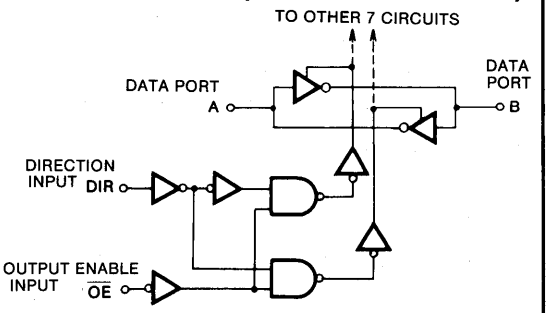
When output enable input $\overline{OE}$ is high, A and B will both become a high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

LOGIC DIAGRAM (EACH TRANSCEIVER)



FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{OE}$	DIR	A	B
L	L	$\overline{O}$	I
L	H	I	$\overline{O}$
H	X	Z	Z

Note 1 : I : Input terminal
$\overline{O}$: Output terminal (inverted output)
Z : High impedance (A and B are separated)
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC640-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC640-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	2.0	1.9			1.9		V
		V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	4.5	4.4			4.4		
		V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	6.0	5.9			5.9		
		V_I = V_{IH}, V_{IL} ; I_{OH} = −24mA	4.5	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	2.0			0.1		0.1	V
		V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	4.5			0.1		0.1	
		V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	6.0			0.1		0.1	
		V_I = V_{IH}, V_{IL} ; I_{OL} = 24mA	4.5			0.39		0.5	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}	6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND	6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

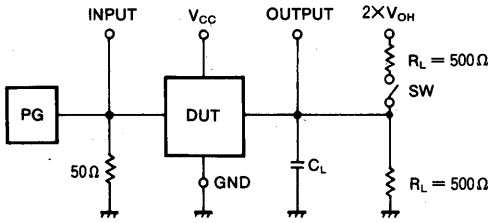
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				15	ns
t_{PHL}	output propagation time (A − B, B − A)				15	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}	($\overline{OE}$ − A, B)				25	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 4)			28	ns
t_{PZH}	($\overline{OE}$ − A, B)				28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)		2.0			85		105	ns
			4.5			17		21	
			6.0			14		18	
t_{PHL}			2.0			85		105	
			4.5			17		21	
			6.0			14		18	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PHZ}			2.0			150		190	
			4.5			30		38	
			6.0			26		33	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PZH}			2.0			150		190	
			4.5			30		38	
			6.0			26		33	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)								

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

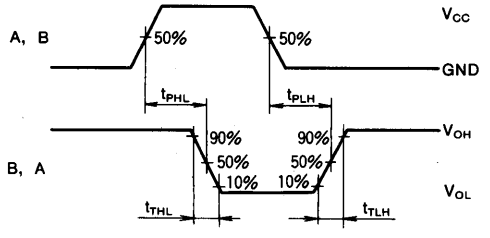
Note 4 : Test Circuit

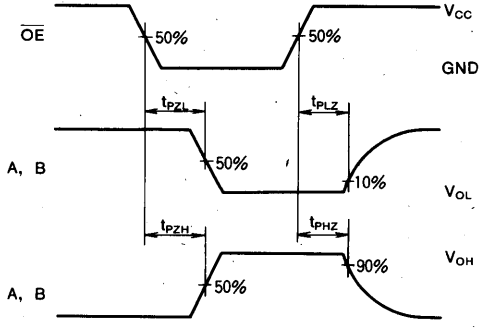


Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HCT640-1P/FP/DWP

OCTAL 3-STATE INVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT640-1 is a semiconductor integrated circuit consisting of eight transceivers with inverted outputs.

FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 10 ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40∼+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT640-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS640.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

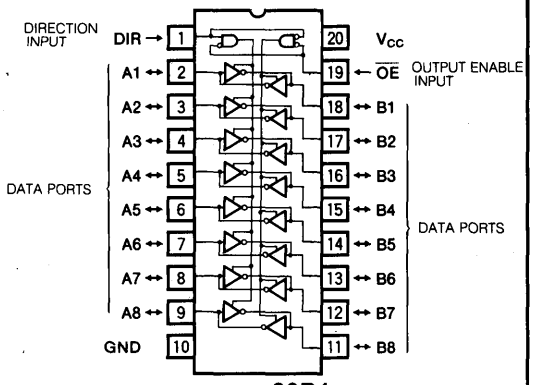
Two buffers with 3-state inverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

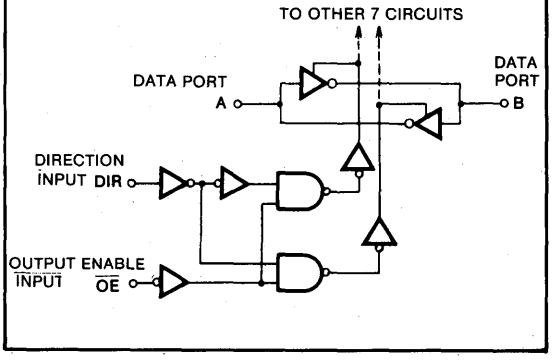
When output enable input $\overline{OE}$ is high, A and B will both become a high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

LOGIC DIAGRAM (EACH TRANSCEIVER)



FUNCTION TABLE (Note 1)

Inputs		Outputs	
$\overline{OE}$	DIR	A	B
L	L	$\overline{O}$	I
L	H	I	$\overline{O}$
H	X	Z	Z

Note 1 : I : Input terminal
$\overline{O}$: Output terminal (inverted output)
Z : High impedance (A and B are separated)
X : Irrelevant

OCTAL 3-STATE INVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HCT640-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HCT640-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.39		0.5	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

OCTAL 3-STATE INVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				15	ns
t_{PHL}					15	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 5 pF (Note 5)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 5)			28	ns
t_{PZH}					28	ns

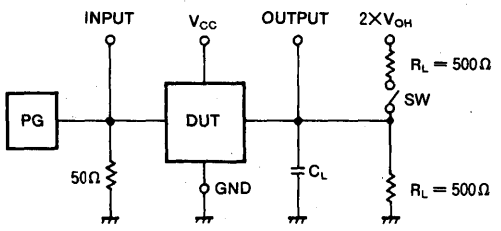
SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40∼+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40∼+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12		15	ns
t_{THL}					12		15	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				17		21	ns
t_{PHL}					17		21	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)				30		38	ns
t_{PHZ}					30		38	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)				30		38	ns
t_{PZH}					30		38	
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	
C_{PD}	Power dissipation capacitance (Note 4)							

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

OCTAL 3-STATE INVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

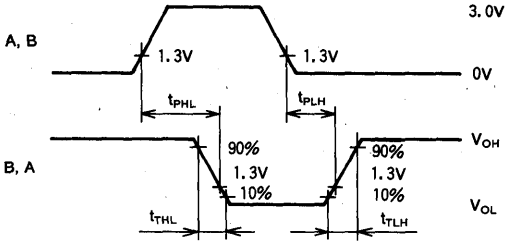
Note 5 : Test Circuit

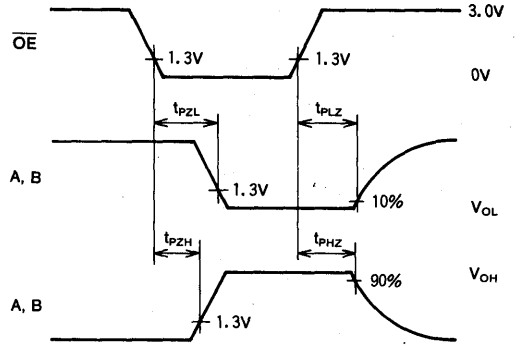


Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 3ns$, $t_f = 3ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC643P/FP/DWP

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC643 is a semiconductor integrated circuit consisting of eight transceivers with inverted and noninverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC643 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS643.

Two buffers with 3-state inverted and noninvertered outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The Input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

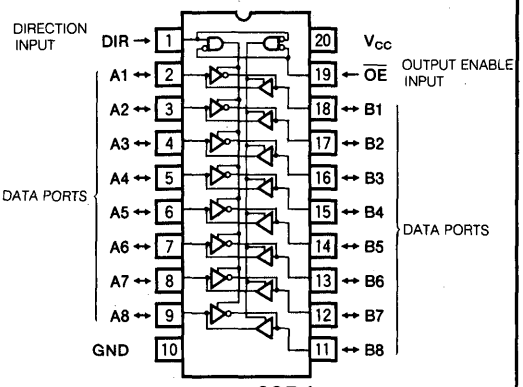
When output enable input $\overline{OE}$ is high, A and B will both become a high-impedance state and they will be separated.

FUNCTION TABLE (Note 1)

Inputs		Outputs	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	$\overline{O}$
H	X	Z	Z

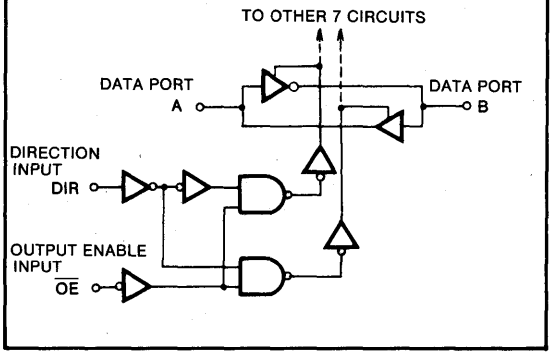
Note 1 : I : Input terminal
O : Output terminal (noninverted output)
$\overline{O}$: Output terminal (inverted output)
Z : High impedance (A and B are separated)
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

LOGIC DIAGRAM (EACH TRANSCEIVER)



OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC643FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC643DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Typ	Max	−40∼+85℃ Min	Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

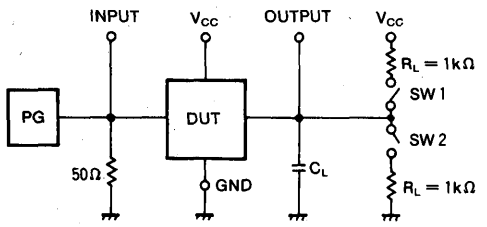
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				21	ns
t_{PHL}	output propagation time (A − B, B − A)				21	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 4)			42	ns
t_{PHZ}	($\overline{OE}$ − A, B)				42	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 4)			42	ns
t_{PZH}	($\overline{OE}$ − A, B)				42	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
	high-level to low-level		6.0			10		13	
t_{THL}	output transition time		2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)	C_L = 50pF (Note 4)	2.0			110		140	ns
			4.5			22		28	
			6.0			19		24	
t_{PHL}			2.0			110		140	ns
			4.5			22		28	
			6.0			19		24	
t_{PLH}		C_L = 150pF (Note 4)	2.0			195		245	ns
			4.5			39		49	
			6.0			34		43	
t_{PHL}			2.0			195		245	ns
			4.5			39		49	
			6.0			34		43	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)	2.0			172		208	ns
			4.5			43		52	
			6.0			41		50	
t_{PHZ}			2.0			172		208	ns
			4.5			43		52	
			6.0			41		50	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)	2.0			184		224	ns
			4.5			46		56	
			6.0			41		50	
t_{PZH}			2.0			184		224	ns
			4.5			46		56	
			6.0			41		50	
t_{PZL}		C_L = 150pF (Note 4)	2.0			216		260	ns
			4.5			54		65	
			6.0			47		57	
t_{PZH}			2.0			216		260	ns
			4.5			54		65	
			6.0			47		57	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				55				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

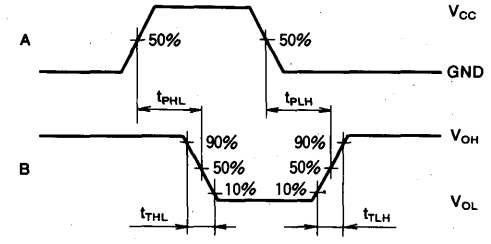
Note 4 : Test Circuit

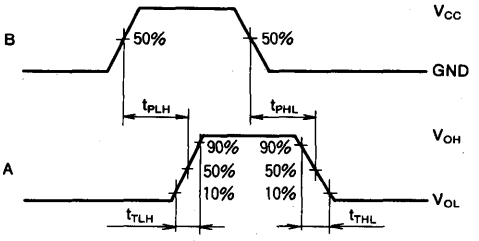


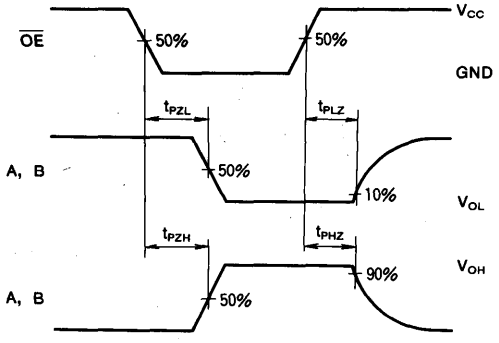
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC643-1P/FP/DWP

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC643-1 is a semiconductor integrated circuit consisting of eight bus transceivers with inverted and noninverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 8ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, Ta=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: Ta=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC643-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS643.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

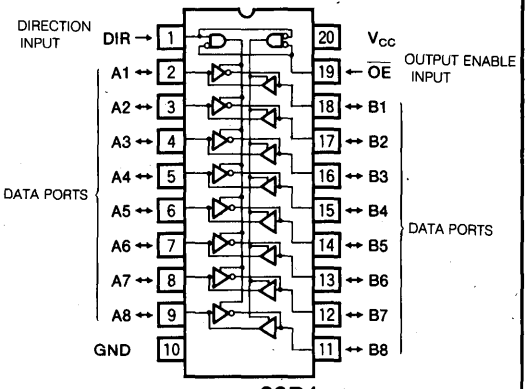
Two buffers with 3-state inverted and noninvertered outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The Input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

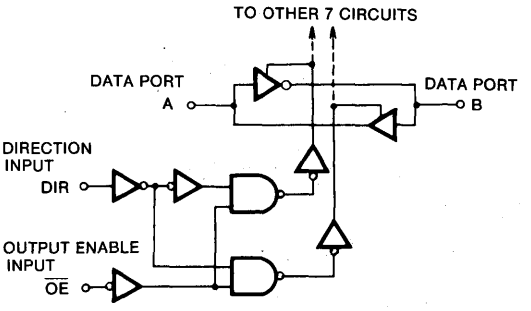
When output enable input $\overline{OE}$ is high, A and B will both become a high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N, 20P2V

LOGIC DIAGRAM (EACH TRANSCEIVER)



FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	$\overline{O}$
H	X	Z	Z

Note 1 : I : Input terminal
O : Output terminal (noninverted output)
$\overline{O}$: Output terminal (inverted output)
Z : High impedance (A and B are separated)
X : Irrelevant

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC643-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC643-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 5.5V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.39		0.5	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

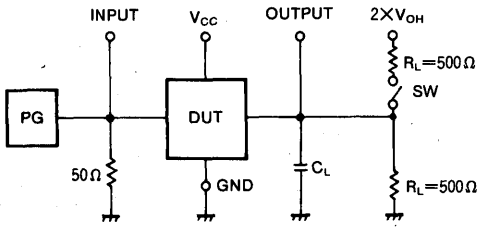
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				15	ns
t_{PHL}					15	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)		2.0			85		105	ns
			4.5			17		21	
			6.0			14		18	
t_{PHL}			2.0			85		105	
			4.5			17		21	
			6.0			14		18	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PHZ}			2.0			150		190	
			4.5			30		38	
			6.0			26		33	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PZH}			2.0			150		190	
			4.5			30		38	
			6.0			26		33	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

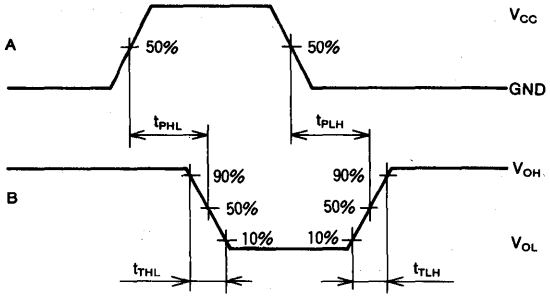
Note 4 : Test Circuit

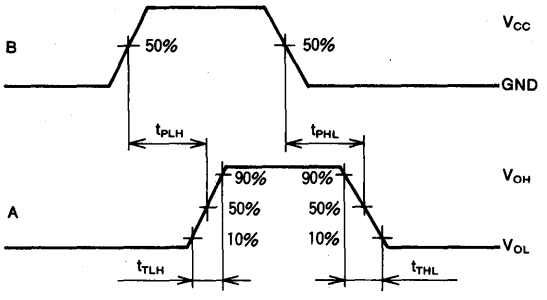


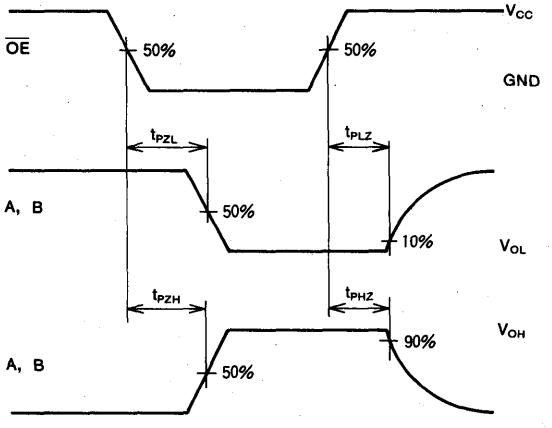
Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HCT643-1P/FP/DWP

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT643-1 is a semiconductor integrated circuit consisting of eight transceivers with inverted and noninverted outputs.

FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT643-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS643.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

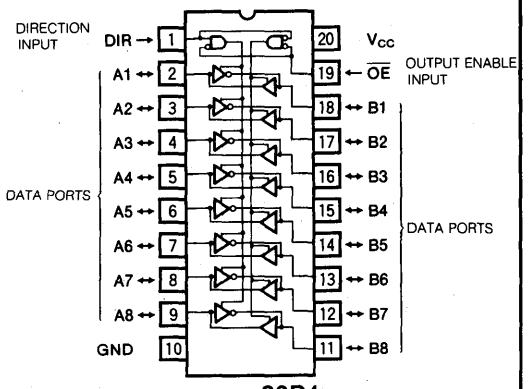
Two buffers with 3-state inverted and noninvertered outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The Input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

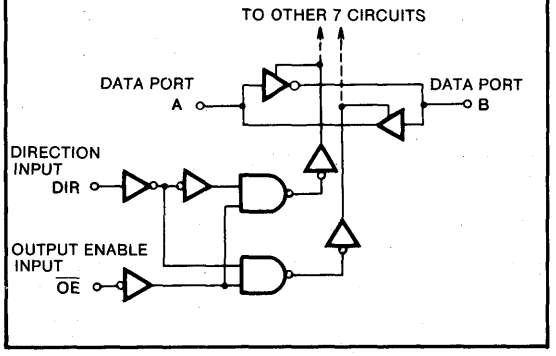
When output enable input $\overline{OE}$ is high, A and B will both become a high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

LOGIC DIAGRAM (EACH TRANSCEIVER)



FUNCTION TABLE (Note 1)

Inputs		Outputs	
$\overline{OE}$	DIR	A	B
L	L	O	$\overline{O}$
L	H	I	$\overline{O}$
H	X	Z	Z

Note 1 : I : Input terminal
O : Output terminal (noninverted output)
$\overline{O}$: Output terminal (inverted output)
Z : High impedance (A and B are separated)
X : Irrelevant

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HCT643-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HCT643-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.39		0.5	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				15	ns
t_{PHL}					15	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 5 pF (Note 5)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 5)			28	ns
t_{PZH}					28	ns

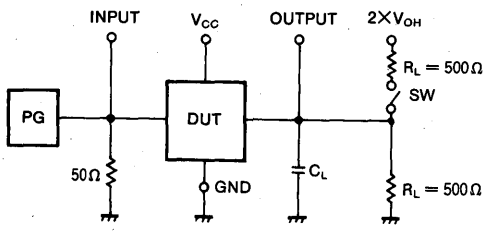
SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40∼+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40∼+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12		15	ns
t_{THL}					12		15	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				17		21	ns
t_{PHL}					17		21	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)				30		38	ns
t_{PHZ}					30		38	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)				30		38	ns
t_{PZH}					30		38	
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	
C_{PD}	Power dissipation capacitance (Note 4)							

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

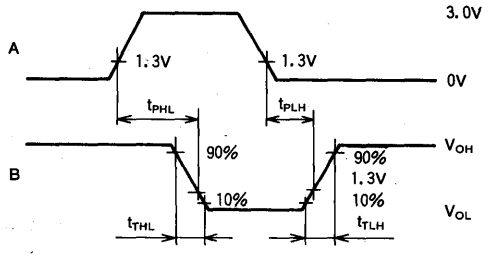
Note 5 : Test Circuit

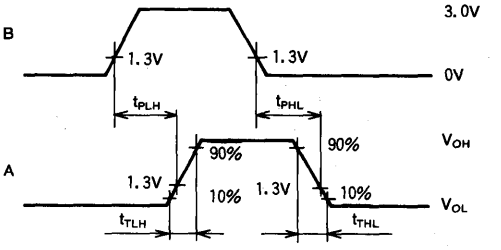


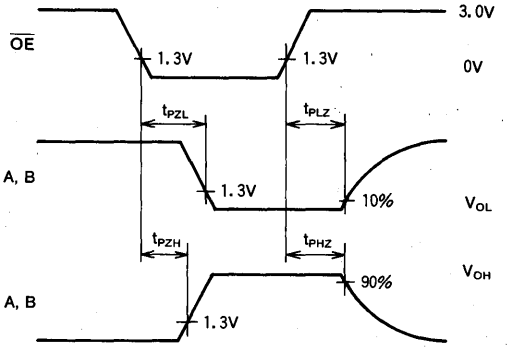
Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







MITSUBISHI ELECTRIC

M74HC645P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC645 is a semiconductor integrated circuit consisting of eight transceivers with noninverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC645 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS645.

Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals.

When DIR is low, B will become input terminals and A will become output terminals.

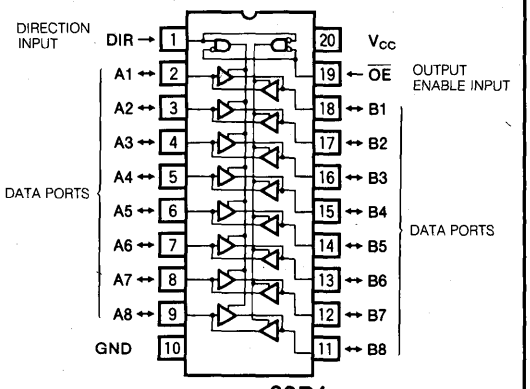
When output enable input $\overline{OE}$ is high, A and B will both become a high-impedance state and they will be separated.

FUNCTION TABLE (Note 1)

Inputs		Outputs	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

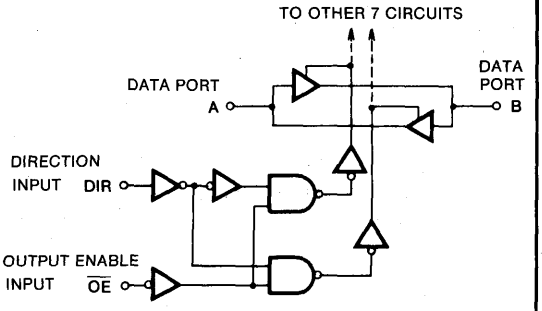
Note 1 : I : Input terminal
O : Output terminal (noninverted output)
Z : High impedance (A and B are separated)
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

LOGIC DIAGRAM (EACH TRANSCEIVER)



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC645FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC645DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits −40∼+85℃ Min	Limits −40∼+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

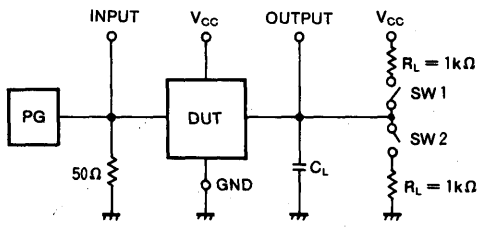
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				21	ns
t_{PHL}					21	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 5 pF (Note 4)			42	ns
t_{PHZ}					42	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)			42	ns
t_{PZH}					42	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)	C_L = 50pF (Note 4)	2.0			110		140	ns
			4.5			22		28	
			6.0			19		24	
t_{PHL}			2.0			110		140	ns
			4.5			22		28	
			6.0			19		24	
t_{PLH}		C_L = 150pF (Note 4)	2.0			195		245	ns
			4.5			39		49	
			6.0			34		43	
t_{PHL}			2.0			195		245	ns
			4.5			39		49	
			6.0			34		43	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)	2.0			172		208	ns
			4.5			43		52	
			6.0			41		50	
t_{PHZ}			2.0			172		208	ns
			4.5			43		52	
			6.0			41		50	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)	2.0			184		224	ns
			4.5			46		56	
			6.0			41		50	
t_{PZH}			2.0			184		224	ns
			4.5			46		56	
			6.0			41		50	
t_{PZL}		C_L = 150pF (Note 4)	2.0			216		260	ns
			4.5			54		65	
			6.0			47		57	
t_{PZH}			2.0			216		260	ns
			4.5			54		65	
			6.0			47		57	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				58				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

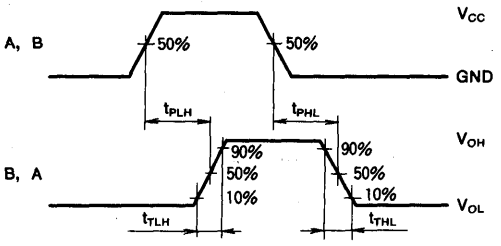
Note 4 : Test Circuit

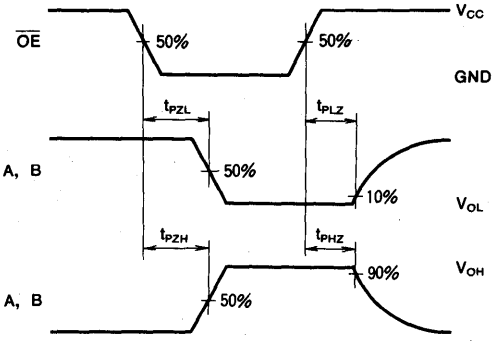


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC645-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC645-1 is a semiconductor integrated circuit consisting of eight bus transceivers with noninverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 8ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC645-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS645.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

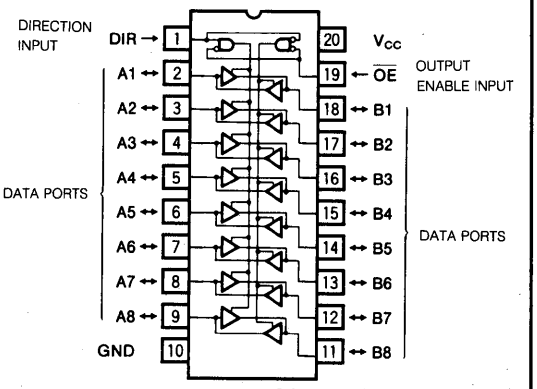
Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

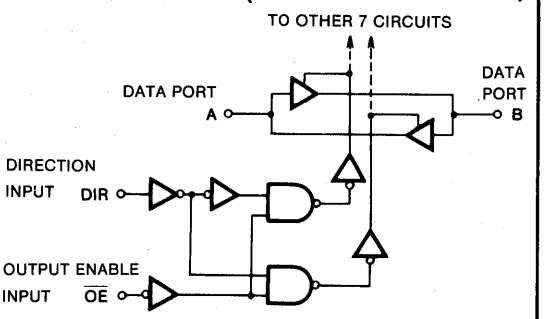
When output enable input $\overline{OE}$ is high, A and B will both become a high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N
20P2V

LOGIC DIAGRAM (EACH TRANSCEIVER)



FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

Note 1 : I : Input terminal
O : Output terminal (noninverted output)
Z : High impedance (A and B are separated)
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC645-1FP, T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HC645-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
					25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.39		0.5	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

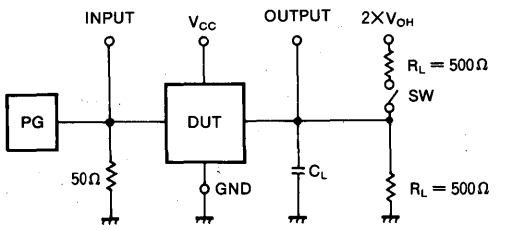
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				15	ns
t_{PHL}					15	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)		2.0			85		105	ns
			4.5			17		21	
			6.0			14		18	
t_{PHL}			2.0			85		105	
			4.5			17		21	
			6.0			14		18	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PHZ}			2.0			150		190	
			4.5			30		38	
			6.0			26		33	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PZH}			2.0			150		190	
			4.5			30		38	
			6.0			26		33	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)								

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

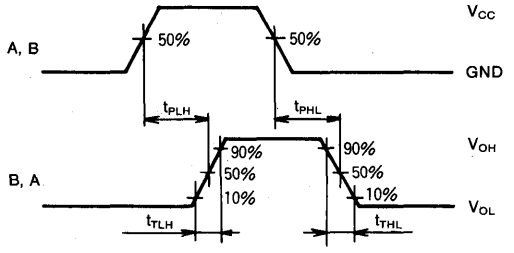
Note 4 : Test Circuit

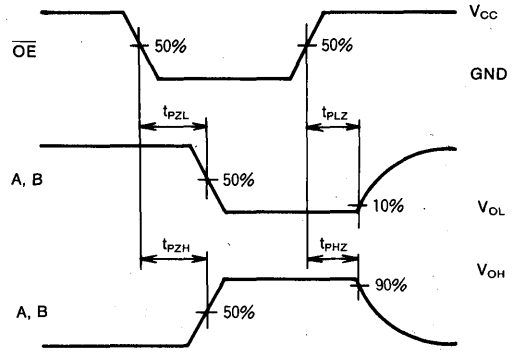


Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 3ns$, $t_f = 3ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HCT645-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT645-1 is a semiconductor integrated circuit consisting of eight three-state noninverted bus transceivers.

FEATURES

- TTL level input V_{IL}=0.8V max V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40∼+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT645-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS645.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

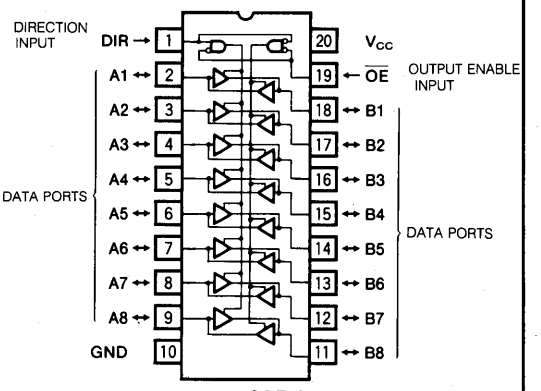
Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

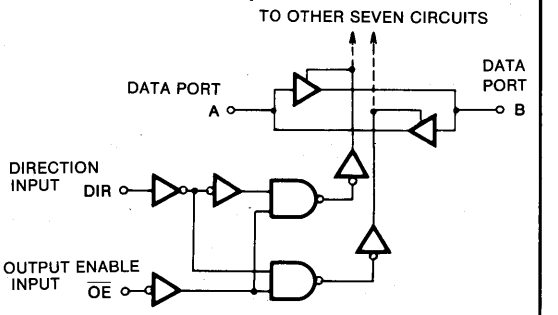
When output enable input $\overline{OE}$ is high, A and B will both become a high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW)



20P4
Outline 20P2N
20P2V

LOGIC DIAGRAM (EACH TRANSCEIVER)



FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

Note 1 : I : Input
O : Output (noninverting output)
Z : High impedance (A and B are isolated)
X : Irrelevant

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼+150	℃

Note 2 : M74HCT645-1FP , T_a = −40∼+75℃ and T_a = 75∼85℃ are derated at −7mW/℃.
M74HCT645-1DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC} − 0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	high-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.98			3.84		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.39		0.5	
I_{IH}	high-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

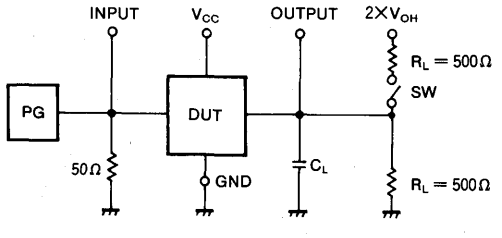
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				15	ns
t_{PHL}					15	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 5 pF (Note 5)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 5)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12		15	ns
t_{THL}					12		15	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				17		21	ns
t_{PHL}					17		21	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)				30		38	ns
t_{PHZ}					30		38	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)				30		38	ns
t_{PZH}					30		38	
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	
C_{PD}	Power disipation capacitance (Note 4)							

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

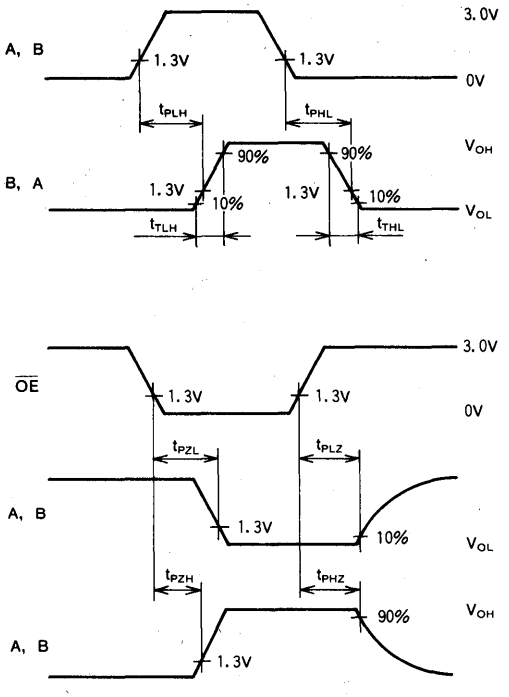
Note 5 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



PRELIMINARY
Notice: This is not a final specification. Some parametric limits are Subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC646P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC646 is a semiconductor integrated circuit consisting of eight bus transceivers with noninverted outputs.

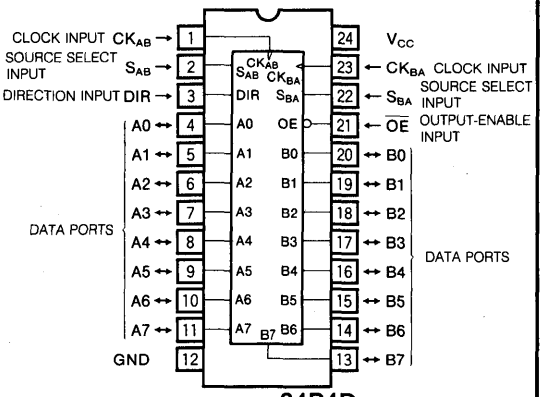
FEATURES

- High-fanout 3-state outputs (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 70MHz clock frequency typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D
24P2
24P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC646 to maintain of the low power dissipation and high noise margin the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS646.

The M74HC646 consists of eight bidirectional buffers by interconnecting the I/O buffers of two D-type flip flops with 3-state noninverted outputs. The I/O direction is controlled by output-enable input $\overline{OE}$ and direction input DIR. The signals are routed from input to output or from the flip flop to output by source select inputs S_{AB} and S_{BA}.

None of the signals are inverted.

When $\overline{OE}$ is low and DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When S_{AB} goes low, the signal A, which was stored in flip frop (A) as Q_A when S_{AB} was high, appears at B. When S_{AB} is held low and when clock input CK_{AB} changes from low to high, the signal present at A is stored in flip flop (A). When S_{AB} is held high and when CK_{AB} changes from low to high, the signal present at A is inverted and stored in flip flop (A). At the same time, the signal Q_A which was stored in flip frop (A), appears at B.

When $\overline{OE}$ and DIR are both low, the I/O direction is reversed: B will become input terminals and A will become output terminals. When S_{BA} goes low, the signal B, Which was stored in flip flop (B) as Q_B when S_{BA} was high, appears at A. When S_{BA} is held low and clock input CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B).

When S_{BA} is held high and CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B). At the same time, the signal Q_B which was stored in flip flop (B), appears at A.

When $\overline{OE}$ is high, both A and B will become high impedance state and they will be separated. When CK_{AB} changes from low to high, the signal present at A is stored in flip flop (A). When CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B).

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

FUNCTION TABLE (Note 1)

Control inputs						Data ports				Flip flop		Operational description
$\overline{OE}$	DIR	CK_{AB}	CK_{BA}	S_{AB}	S_{BA}	A		B		$\overline{Q_A}$	$\overline{Q_B}$	
H	X	X	X	X	X		X		X	$\overline{Q_A}^0$	$\overline{Q_B}^0$	The output of data ports A and B are disabled.
H	X	↑	X	X	X		L		X	$\overline{Q_A}^0$	X	Data ports A and B are stroed by the flip flops at the rising edge of CK_{AB} and CK_{BA}. The output of data ports A and B is disabled.
H	X	↑	X	X	X	I	H	I	X	$\overline{Q_A}^0$	X	
H	X	X	↑	X	X		X		L	X	$\overline{Q_B}^0$	
H	X	X	↑	X	X		X		H	X	$\overline{Q_B}^0$	
L	H	X	X*	L	X		L		L	$\overline{Q_A}^0$	$\overline{Q_B}^0$	The output of data port B is enabled. (Note 2) 1) When S_{AB} is low, data port A appears at data port B. The state of the flip flop (A) is unchanged.
L	H	X	X*	L	X		H		H	$\overline{Q_A}^0$	$\overline{Q_B}^0$	
L	H	X	X*	H	X		X		Q_A^0	$\overline{Q_A}^0$	$\overline{Q_B}^0$	2) When S_{AB} is high, the output of flip flop (A) appears at data port B.
L	H	↑	X*	L	X	I	L	O	L	$\overline{Q_A}^0$	$\overline{Q_B}^0$	3) When S_{AB} is low, the data port A appears at data port B and is stored in flip flop (A) at the rising edge of CK_{AB}.
L	H	↑	X*	L	X		H		H	$\overline{Q_A}^0$	$\overline{Q_B}^0$	
L	H	↑	X*	H	X		L		Q_A^0	$\overline{Q_A}^0$	$\overline{Q_B}^0$	4) When S_{AB} is high, the data port A is stored in flip flop (A) at the rising edge of CK_{AB}, and the output of flip flop (A) appears at data port B.
L	H	↑	X*	H	X		H		Q_A^0	$\overline{Q_A}^0$	$\overline{Q_B}^0$	
L	L	X*	X	X	L		L		L	$\overline{Q_A}^0$	$\overline{Q_B}^0$	The output of data port A is enabled. (Note 3) 1) When S_{BA} is low, the data port B appears at data port A. The state of flip flop (B) is unchanged.
L	L	X*	X	X	L		H		H	$\overline{Q_A}^0$	$\overline{Q_B}^0$	
L	L	X*	X	X	H		Q_B^0		X	$\overline{Q_A}^0$	$\overline{Q_B}^0$	2) When S_{BA} is high, the output of flip flop (B) appears at data port A.
L	L	X*	↑	X	L	O	L	I	L	$\overline{Q_A}^0$	$\overline{Q_B}^0$	3) When S_{BA} is low, the data port B appears at data port A and is stored is flip flop (B) at the rising edge of CK_{AB}.
L	L	X*	↑	X	L		H		H	$\overline{Q_A}^0$	$\overline{Q_B}^0$	
L	L	X*	↑	X	H		Q_B^0		L	$\overline{Q_A}^0$	$\overline{Q_B}^0$	4) When S_{BA} is high, the data port B is stored in flip flop (B) and the output of flip flop (B) appears at data port A.
L	L	X*	↑	X	H		Q_B^0		H	$\overline{Q_A}^0$	$\overline{Q_B}^0$	

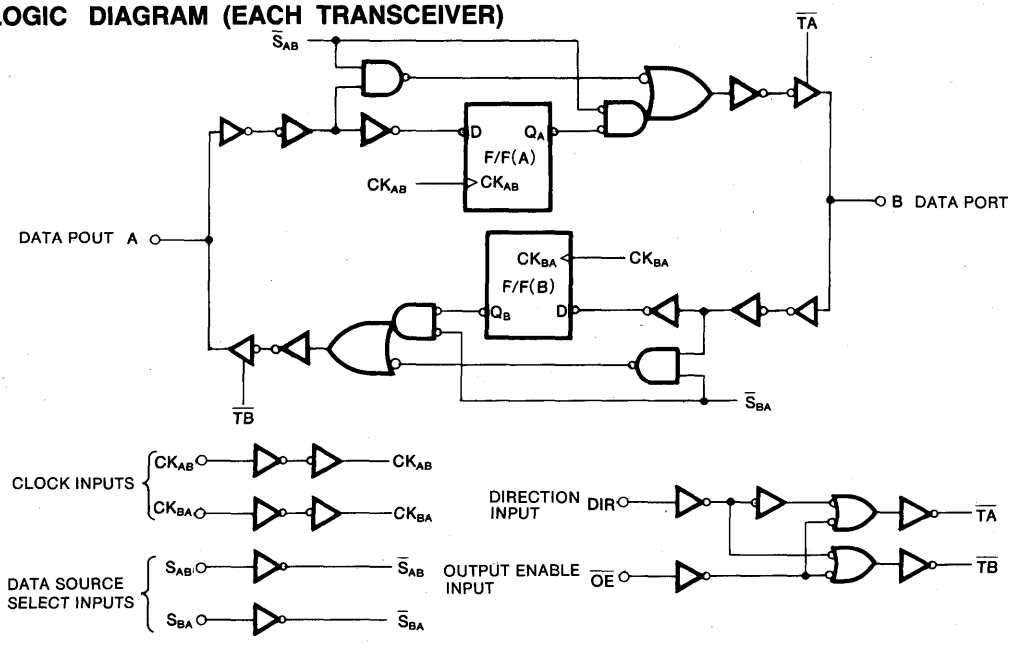
Note 1 : X : Irrelevant
↑ : Change from low to high
Q_A^0, Q_B^0 : Output state of flip flops before the rise of CK_{AB} and CK_{BA}.
I : Input terminal of data port
O : Output terminal of data port
* : As CK_{AB} and CK_{BA} are not selected by the I/O directional signal, data from data ports A and B can be stored in the corresponding flip flops at the rising edge of CK_{AB} or CE_{BA}.

Note 2 : The output at port B is given by :
$B = (A \cdot \overline{S_{AB}}) + (Q_A \cdot S_{AB})$

Note 3 : The output at port B is given by:
$A = (B \cdot \overline{S_{BA}}) + (Q_B \cdot S_{BA})$

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

LOGIC DIAGRAM (EACH TRANSCEIVER)



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 4)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 4 : M74HC646FP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.
M74HC646DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Typ	Max	−40～+85℃ Min	Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
f_{max}	Maximum clock frequency	C_L = 50pF (Note 6)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 6)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				30	ns
t_{PHL}					30	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_{AB} − B, CK_{BA} − A)				40	ns
t_{PHL}					40	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S_{AB} − B, S_{BA} − A)				30	ns
t_{PHL}					30	ns
t_{PLZ}	Output disable time from low-level and high-level (DIR − A, B)	C_L = 5pF (Not 6)			30	ns
t_{PHZ}					30	ns
t_{PZL}	Output enable time to low-level and high-level (DIR − A, B)	C_L = 50pF (Note 6)			33	ns
t_{PZH}					33	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 5pF (Note 6)			30	ns
t_{PHZ}					30	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 6)			33	ns
t_{PZH}					33	ns

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 6)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)		2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PLH}		C_L = 150pF (Note 6)	2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PHL}			2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_{AB} − B, CK_{BA} − A)	C_L = 50pF (Note 6)	2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PHL}			2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PLH}		C_L = 150pF (Note 6)	2.0			270		340	ns
			4.5			54		68	
			6.0			46		58	
t_{PHL}			2.0			270		340	ns
			4.5			54		68	
			6.0			46		58	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S_{AB} − B, S_{BA} − A)	C_L = 50pF (Note 6)	2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PLH}		C_L = 150pF (Note 6)	2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PHL}			2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PLZ}	Output disable time from low-level and high-level (DIR − A, B)	C_L = 50pF (Note 6)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHZ}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

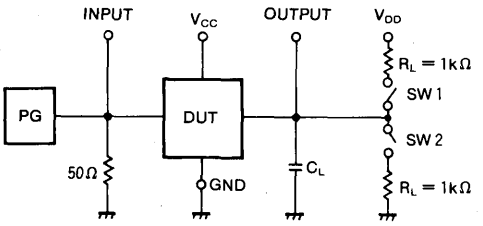
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{PZL}	Output enable time to low-level and high-level (DIR − A, B)	C_L = 50pF (Note 6)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZH}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZL}		C_L = 150pF (Note 6)	2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PZH}			2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 6)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHZ}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZH}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZL}		C_L = 150pF (Note 6)	2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PZH}			2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 5)								pF

Note 5 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W	CK_{AB}, CK_{BA} pulse width	2.0	80			101		ns
		4.5	16			20		
		6.0	14			17		
t_{su}	A, B setup time with respect to CK_{AB}, CK_{BA}	2.0	100			125		ns
		4.5	20			25		
		6.0	17			21		
t_h	A, B hold time with respect to CK_{AB}, CK_{BA}	2.0	0			0		ns
		4.5	0			0		
		6.0	0			0		

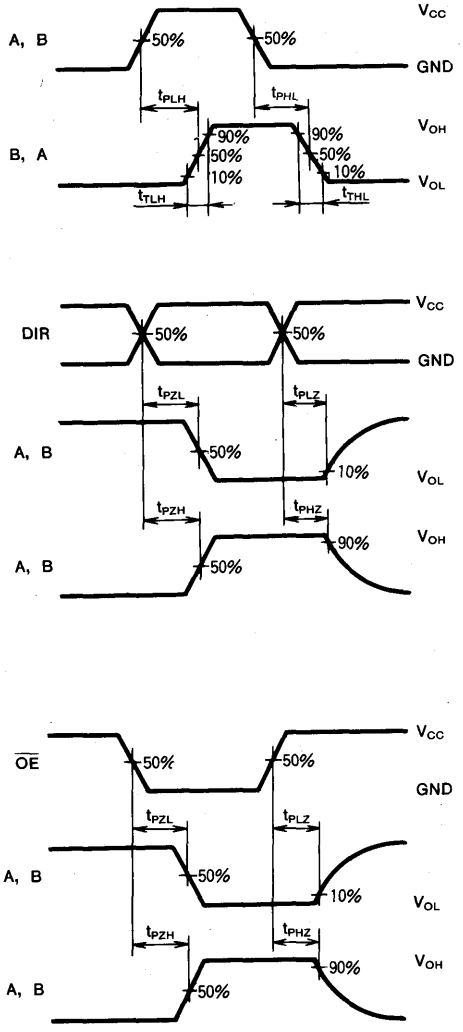
Note 6 : Test Circuit

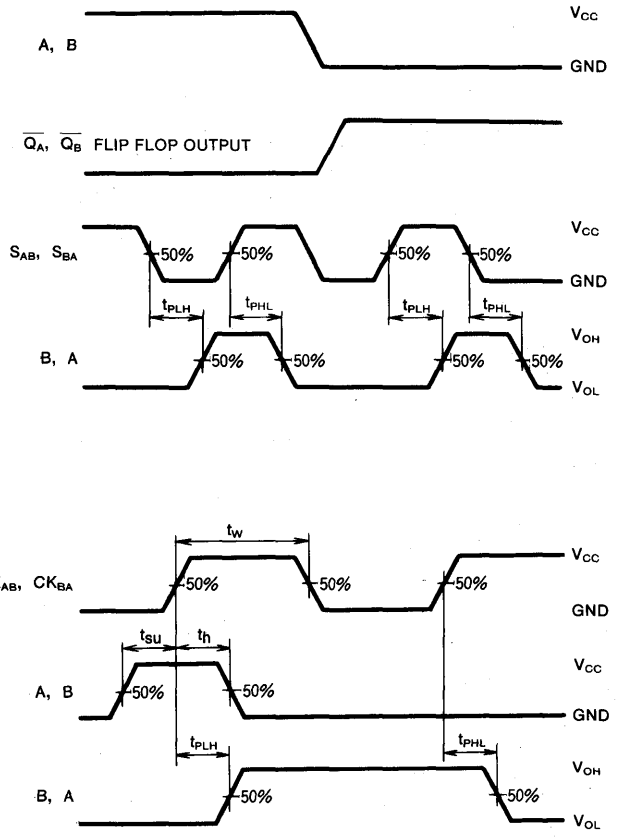


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC648P/FP/DWP

OCTAL 3-STATE INVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC648 is a semiconductor integrated circuit consisting of eight bus transceivers with inverted outputs.

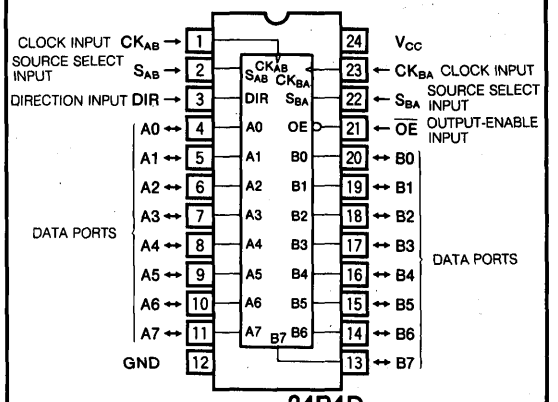
FEATURES

- High fon-out 3-state outputs (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 70MHz clock frequency typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D 24P2 24P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC648 to maintain the low power dissipation and high noise margin of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS648.

The M74HC648 consists of eight bidirectional buffers by interconnecting the I/O buffers of two D-type flip flops with 3-state inverted outputs. The I/O direction is controlled by output-enable input $\overline{OE}$ and direction input DIR. The signals are routed from input to output or from the flip flop to output by source select inputs S_{AB} and S_{BA}. The input signals are inverted when they appear at the output.

When $\overline{OE}$ is low and DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When S_{AB} goes low, the inverted signal A, which was stored in flip flop (A) as Q_A when S_{AB} was high, appears at B. When SAB is held low and when clock input CK_{AB} changes from low to high, the signal present at A is stored in flip flop (A). When S_{AB} is held high and when CK_{AB} changes from low to high, the signal present at A is inverted and stored in flip flop (A). At the same time, the inverted signal $\overline{Q_A}$ which was stored in flip flop (A), appears at B.

When $\overline{OE}$ and DIR are both low, the I/O direction is reversed: B will become input terminals and A will become output terminals. When S_{BA} goes low, and the inverted signal B, which was stored in flip flop (B) as Q_B when S_{BA} was high, appears at A. When S_{BA} is held low and clock input CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B).

When S_{BA} is held high and CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B).At the same time, the inverted signal $\overline{Q_B}$ which was stored in flip flop (B), appears at A.

When $\overline{OE}$ is high, both A and B will become high impedance state and they will be separated. When CK_{AB} changes from low to high, the signal present at A is stored in flip flop (A). When CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B).

MITSUBISHI ELECTRIC

OCTAL 3-STATE INVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

FUNCTION TABLE (Note 1)

Control inputs						Data ports				Flip Flop		Operational description
$\overline{OE}$	DIR	CK_{AB}	CK_{BA}	S_{AB}	S_{BA}	A		B		Q_A	Q_B	
H	X	X	X	X	X		X		X	Q_A^0	Q_B^0	The output of data ports A and B are disabled.
H	X	↑	X	X	X		L		X	Q_A^0	X	Data ports A and B are stored by the flip flops at the rising edge of CK_{AB} and CK_{BA}. The output of data ports A and B is disabled.
H	X	↑	X	X	X	I	H	I	X	Q_A^0	X	
H	X	X	↑	X	X		X		L	X	Q_B^0	
H	X	X	↑	X	X		X		H	X	Q_B^0	
L	H	X	X*	L	X		L		H	Q_A^0	Q_B^0	The output of data port B is enabled. (Note 2) 1) When S_{AB} is low, the data port A appears at data port B. The state of the flip flop (A) is unchanged.
L	H	X	X*	L	X		H		L	Q_A^0	Q_B^0	
L	H	X	X*	H	X		X		$\overline{Q_A^0}$	Q_A^0	Q_B^0	2) When S_{AB} is high, the output of flip flop (A) appears at data port B.
L	H	↑	X*	L	X	I	L	O	H	Q_A^0	Q_B^0	3) When S_{AB} is low, the data port A appears at data port B and is stored in flip flop (A) at the rising edge of CK_{AB}.
L	H	↑	X*	L	X		H		L	Q_A^0	Q_B^0	
L	H	↑	X*	H	X		L		$\overline{Q_A^0}$	Q_A^0	Q_B^0	4) When S_{AB} is high, the data port A is stored in flip flop (A) at the rising edge of CK_{AB}, and the output of flip flop (A) appears at data port B.
L	H	↑	X*	H	X		H		$\overline{Q_A^0}$	Q_A^0	Q_B^0	
L	L	X*	X	X	L		H		L	Q_A^0	Q_B^0	The output of data port A is enabled. (Note 3) 1) When S_{BA} is low, the data port B appears at data port A. The state of flip flop (B) is unchanged.
L	L	X*	X	X	L		L		H	Q_A^0	Q_B^0	
L	L	X*	X	X	H		$\overline{Q_B^0}$		X	Q_A^0	Q_B^0	2) When S_{BA} is high, the output of flip flop (B) appears at data port A.
L	L	X*	↑	X	L	O	H	I	L	Q_A^0	Q_B^0	3) When S_{BA} is low, the data port B appears at data port A and is stored in flip flop (B) at the rising edge of CK_{AB}.
L	L	X*	↑	X	L		L		H	Q_A^0	Q_B^0	
L	L	X*	↑	X	H		$\overline{Q_B^0}$		L	Q_A^0	Q_B^0	4) When S_{BA} is high, the data port B is stored in flip flop (B) and the output of flip flop (B) appears at data pout A.
L	L	X*	↑	X	H		$\overline{Q_B^0}$		H	Q_A^0	Q_B^0	

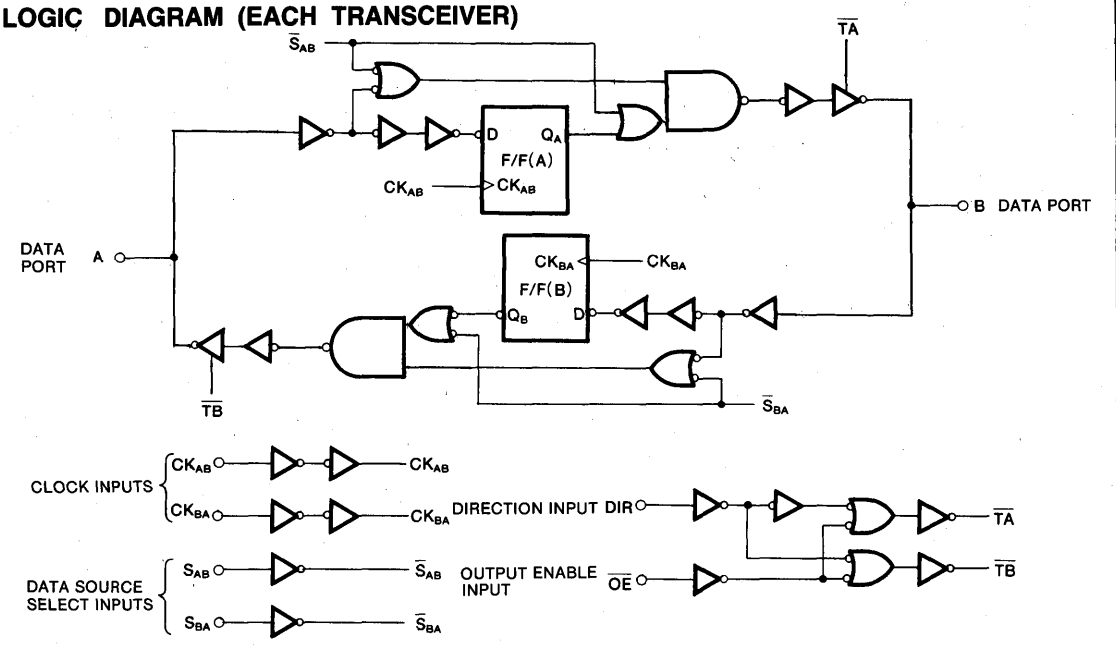
Note 1 : X : Irrelevant
↑ : Change from low to high
Q_A^0, Q_B^0 : Output state of flip flops before the rising edge of CK_{AB} and CK_{BA}.
I : Input terminal of data port
O : Output terminal data port
* : As CK_{AB} and CK_{BA} are not selected by the I/O direction signal, data from data ports A and B can be stored in the corresponding flip flops at the rising edge of CK_{AB} or CK_{BA}.

Note 2 : The outnput at data port B is given by:
$B = (\overline{A} \cdot \overline{S_{AB}}) + (\overline{Q_A} \cdot S_{AB})$

Note 3 : The output at data port B is given by:
$A = (\overline{B} \cdot \overline{S_{BA}}) + (\overline{Q_B} \cdot S_{BA})$

OCTAL 3-STATE INVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

LOGIC DIAGRAM (EACH TRANSCEIVER)



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 4)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 4 : M74HC648FP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.
M74HC648DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

MITSUBISHI ELECTRIC

OCTAL 3-STATE INVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9			V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 6)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 6)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				30	ns
t_{PHL}					30	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_{AB} − B, CK_{BA} − A)				40	ns
t_{PHL}					40	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S_{AB} − B, S_{BA} − A)				30	ns
t_{PHL}					30	ns
t_{PLZ}	Output disable time from low-level and high-level (DIR − A, B)	C_L = 5pF (Note 6)			30	ns
t_{PHZ}					30	ns
t_{PZL}	Output enable time to low-level and high-level (DIR − A, B)	C_L = 50pF (Note 6)			33	ns
t_{PZH}					33	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 5pF (Note 6)			30	ns
t_{PHZ}					30	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 6)			33	ns
t_{PZH}					33	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 6)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)		2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PLH}		C_L = 150pF (Note 6)	2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PHL}			2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_{AB} − B, CK_{BA} − A)	C_L = 50pF (Note 6)	2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PHL}			2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PLH}		C_L = 150pF (Note 6)	2.0			270		340	ns
			4.5			54		68	
			6.0			46		58	
t_{PHL}			2.0			270		340	ns
			4.5			54		68	
			6.0			46		58	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S_{AB} − B, S_{BA} − A)	C_L = 50pF (Note 6)	2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PLH}		C_L = 150pF (Note 6)	2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PHL}			2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PLZ}	Output disable time from low-level and high-level (DIR − A, B)	C_L = 50pF (Note 6)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHZ}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{PZL}	Output enable time to low-level and high-level (DIR − A, B)	C_L = 50pF (Note 6)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZH}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZL}		C_L = 150pF (Note 6)	2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PZH}			2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 6)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHZ}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZH}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZL}		C_L = 150pF (Note 6)	2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PZH}			2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 5)								pF

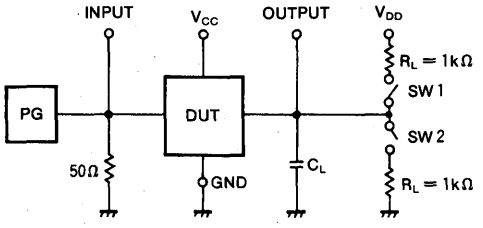
Note 5 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK_{AB}, CK_{BA} pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	A, B setup time with respect to CK_{AB}, CK_{BA}		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	A, B hlod time with respect to CK_{AB}, CK_{BA}		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		

OCTAL 3-STATE INVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

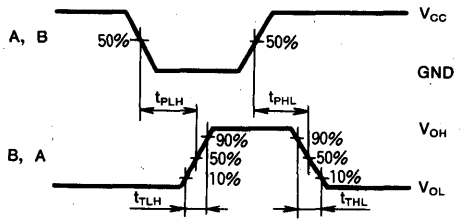
Note 6 : Test Circuit

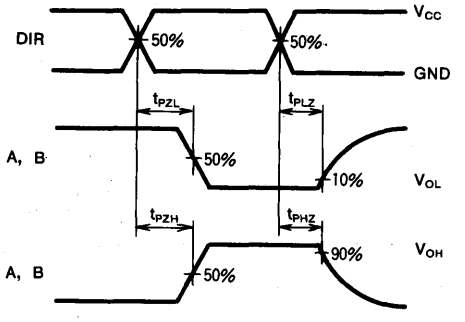


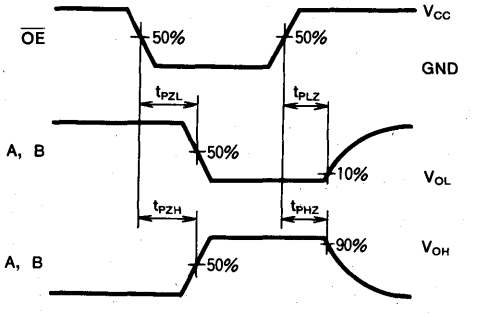
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

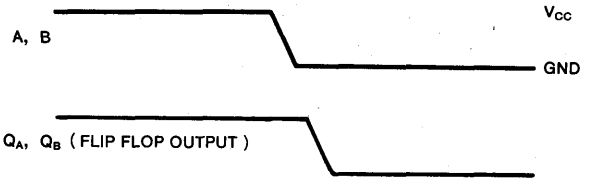
(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

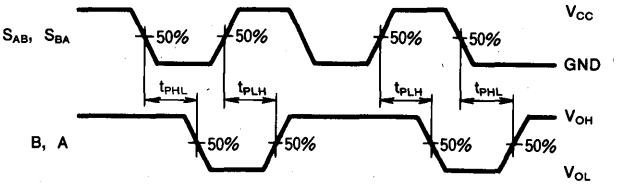
TIMING DIAGRAM

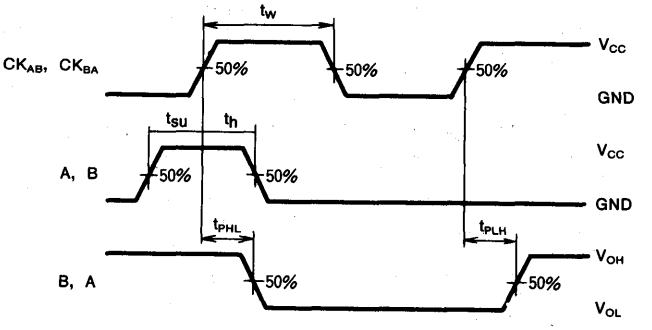












MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC669P/FP/DP

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

DESCRIPTION

The M74HC669 is a semiconductor integrated circuit consisting of a 4-bit binary synchronous counter with up/down control and synchronous preset inputs.

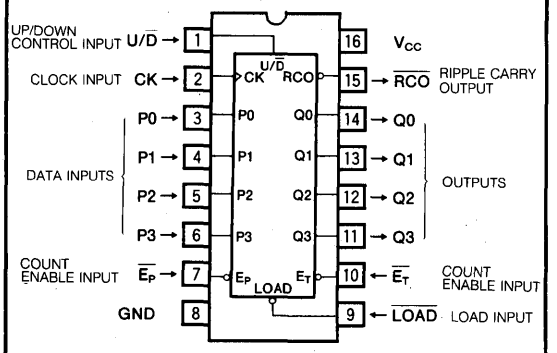
FEATURES

- Up/down control and synchronous preset inputs
- Enable input and ripple-carry output allow cascade connection
- High-speed: 45 MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC699 to maintain the low power dissipation and high noise margin of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS699.

The preset function, up/down control and enable function operate in synchronous with the rising edge of the clock. To preset the counter to a specific value, Load input $\overline{LOAD}$ is set to low-level and the corresponding data is applied to data inputs P0 through P3, the new count appears at outputs Q0 throgh Q3 in synchronous with the rising edge of the next clock input at CK.

Up/down control is possible when $\overline{LOAD}$ is high-level and count enable inputs $\overline{E_P}$ and $\overline{E_T}$ are both low-level. The count increases when control input U/$\overline{D}$ is high-level, and decreases when U/$\overline{D}$ is low-level.

The ripple carry output $\overline{RCO}$ will become low when the count reaches 15 (1111_2) going up or 0 (0000_2) going down. $\overline{E_P}$, $\overline{E_T}$ and $\overline{RCO}$ are used in cascade connections of the counter in synchronous from when the counter is used as a 2^n counter.

Counting is inhibited when $\overline{LOAD}$ is high-level, and when either $\overline{E_P}$ or $\overline{E_T}$ is high-level.

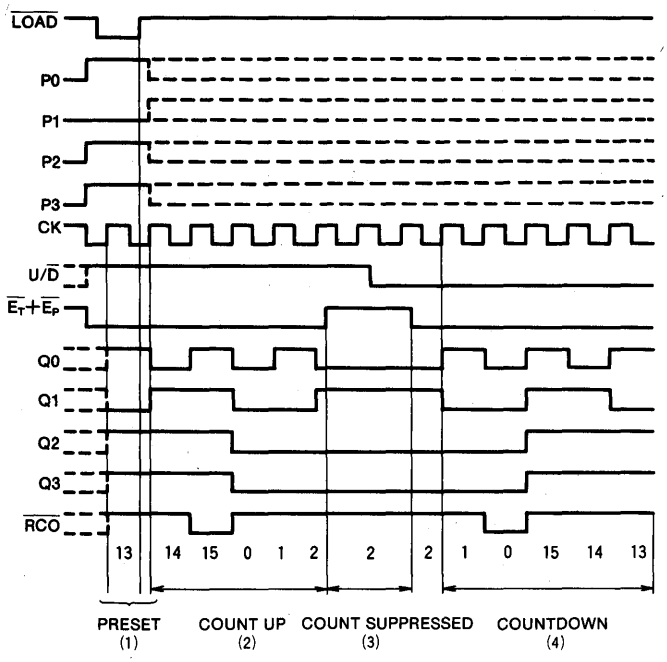
FUNCTION TABLE (Note 1)

Inputs					Outputs				
$\overline{LOAD}$	$\overline{E_P}$	$\overline{E_T}$	U/$\overline{D}$	CK	Q0	Q1	Q2	Q3	$\overline{RCO}$*
L	X	X	X	↑	P0	P1	P2	P3	H
H	L	L	H	↑	Count up				H
H	L	L	L	↑	Count down				H
H	H	X	X	X	Count spperessed				H
H	X	H	X	X					

Note 1 : ↑ : Change from low to high
X : Irrelevant
* : $\overline{RCO}$ is normally high, but when $\overline{E_T}$ is low, the count is increasing, and Q0, Q1, Q2 and Q3 are high, then $\overline{RCO}$ will become low. It also will become low when the count is decreasing and Q0, Q1, Q2 and Q3 are low.

$\overline{RCO}$=Q0 · Q1 · Q2 · Q3 · (U/$\overline{D}$) · $\overline{E_T}$
$\overline{RCO}$=$\overline{Q0}$ · $\overline{Q1}$ · $\overline{Q2}$ · $\overline{Q3}$ · (U/$\overline{D}$) · E_T

TIMING DIAGRAM



TIMING DIAGRAM
(1) Preset to 13
(2) The count up sequence is 14, 15, 0, 1, 2
(3) Count suppressed
(4) The count down sequences is 1, 0, 15, 14, 13.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC670P/FP/DP

4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC670 is a semiconductor integrated circuit consisting of a 4-word by 4-bit register file with 3-state outputs.

FEATURES

- Independent inputs for read and write addresses allow simultaneous reading and writing.
- Read-enable and output-control inputs
- High-speed: 21 ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃
- 3-state outputs

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC670 to maintain the low power dissipation and high noise margin the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS670.

The M74HC670 has sixteen flip flops for storage and has discrete enable, address and output-enable inputs for both reading and writing. One word can be read while another is written enabling high-speed data transfer. The use of 3-state outputs enables "AND" ties.

- Writing method

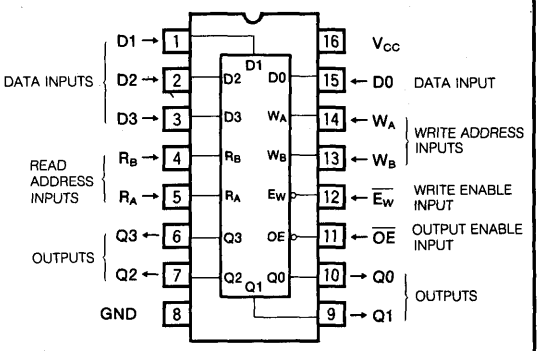
By selecting a word using write address input WA and WB and applying date to the date inputs D0, D1, D2 and D3, writing into each bit is performed.

For writing the write-enable input $\overline{EW}$ must be held low. When $\overline{EW}$ is high, no date will be written.

- Reading method

When a word is selected by read address inputs RA and RB, the contents of each bit appear at the outputs Q0, Q1, Q2 and Q3. For reading the output-enable input $\overline{OE}$ must be held low. When $\overline{OE}$ is high, all outputs will become high-impedance state irrespective of other inputs.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTION TABLE (Note 1) WRITTING FUNCTION

Inputs			Outputs			
			Word			
W_A	W_B	$\overline{E_W}$	0	1	2	3
X	X	H	Q^0	Q^0	Q^0	Q^0
L	L	L	Q=D	Q^0	Q^0	Q^0
H	L	L	Q^0	Q=D	Q^0	Q^0
L	H	L	Q^0	Q^0	Q=D	Q^0
H	H	L	Q^0	Q^0	Q^0	Q=D

READING FUNCTION

Inputs			Outputs			
R_A	R_B	$\overline{OE}$	Q0	Q1	Q2	Q3
X	X	H	Z	Z	Z	Z
L	L	L	W_0B_0	W_0B_1	W_0B_2	W_0B_3
H	L	L	W_1B_0	W_1B_1	W_1B_2	W_1B_3
L	H	L	W_2B_0	W_2B_1	W_2B_2	W_2B_3
H	H	L	W_3B_0	W_3B_1	W_3B_2	W_3B_3

Note 1 : Q^0 : The contents of the word do not change.
Q=D : The input data is written to the specified word.
W_XB_Y : Word X bit Y
X : Irrelevant
Z : High impedance

M74HC688P/FP/DWP

8-BIT EQUALITY COMPARATOR

DESCRIPTION

The M74HC688 is a semiconductor integrated circuit consisting of an 8-bit digital comparator with a cascade input.

FEATURES

- High-speed: 28ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC},min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

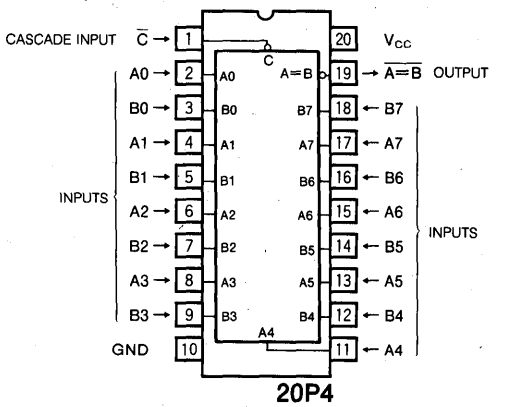
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC688 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS688.

When cascade input $\overline{C}$ is low and two 8-bit binary A and B are applied to comparison inputs A0~A7 and B0~B7, the output $\overline{A=B}$ will become low when A=B and the output will become high when A>B or A<B.

When $\overline{C}$ is high, $\overline{A=B}$ will become high irrespective of A0 ~A7 or B0~B7.

PIN CONFIGURATION (TOP VIEW)



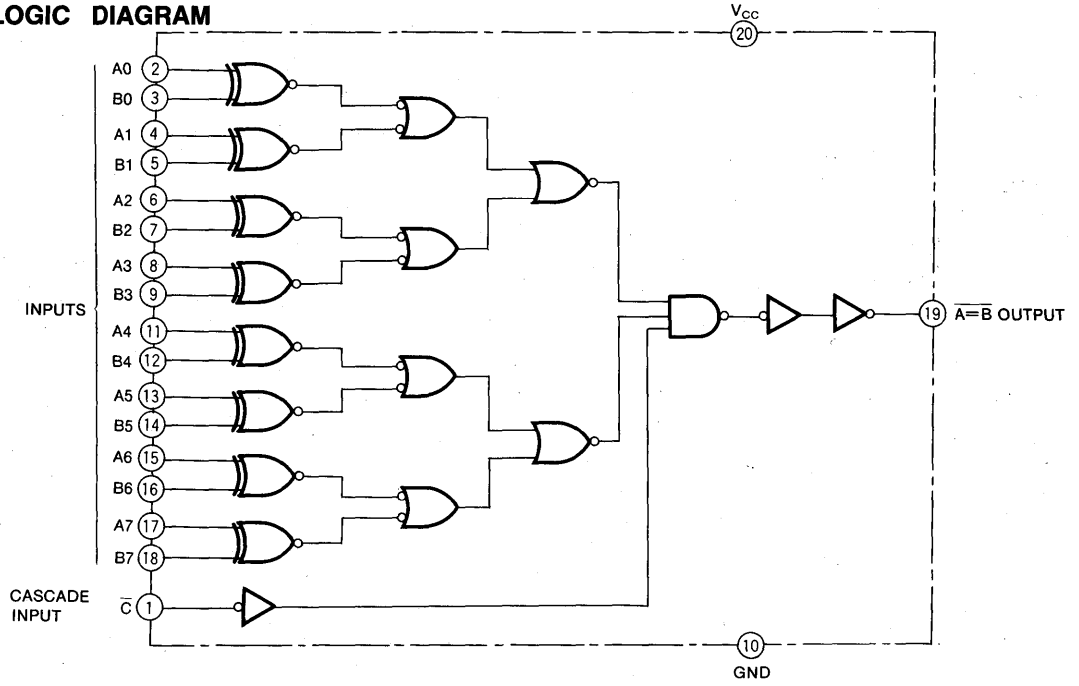
20P4
Outline 20P2N
20P2V

FUNCTION TABLE (Note 1)

Inputs		Output
A, B	$\overline{C}$	$\overline{A=B}$
A=B	L	L
A>B	L	H
A<B	L	H
X	H	H

Note 1 : X : Irrelevant

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC688FP, T_a = −40∼+75℃ and T_a = 75∼80℃ are derated at −7mW/℃.
M74HC688DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
					25℃			−40∼+85℃	
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

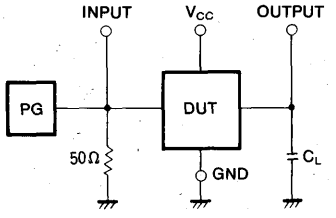
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − $\overline{A=B}$)				38	ns
t_{PHL}					38	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{C}$ − $\overline{A=B}$)				22	ns
t_{PHL}					22	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − $\overline{A=B}$)		2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PHL}			2.0			210		265	
			4.5			42		53	
			6.0			36		45	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{C}$ − $\overline{A=B}$)		2.0			120		151	ns
			4.5			24		30	
			6.0			20		26	
t_{PHL}			2.0			120		151	
			4.5			24		30	
			6.0			20		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				32				pF

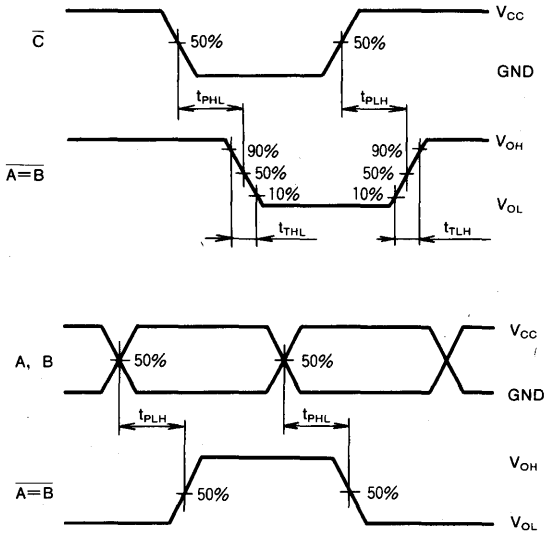
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC4002P/FP/DP

DUAL 4-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74HC4002 is a semiconductor integrated circuit consisting of two 4-input positive-logic NOR gates, usable as negative-logic NAND gates.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4002 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

Buffered outputs Y improve input-to -output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

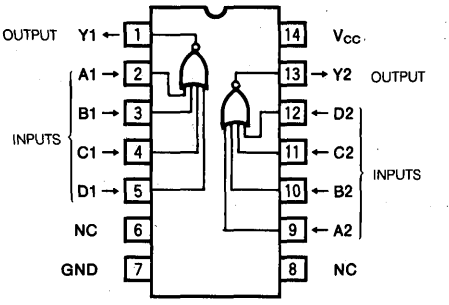
When all inputs A, B, C and D are low, the output Y will become high, and when at least one of the inputs is high, the output Y will become low.

FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	L
L	H	L
H	H	L

N = B + C + D

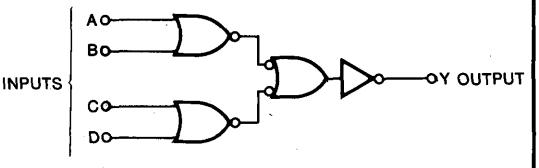
PIN CONFIGURATION (TOP VIEW)



14P4
Outline 14P2N
14P2P

NC : NO CONNECTION

LOGIC DIAGRAM (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC4002FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC4002DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −4.0mA	4.5	4.18			4.13		
		I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 4.0mA	4.5			0.26		0.33	
		I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

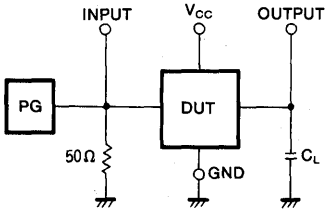
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				20	ns
t_{PHL}					20	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			120		151	ns
			4.5			24		30	
			6.0			20		26	
t_{PHL}			2.0			120		151	ns
			4.5			24		30	
			6.0			20		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				31				pF

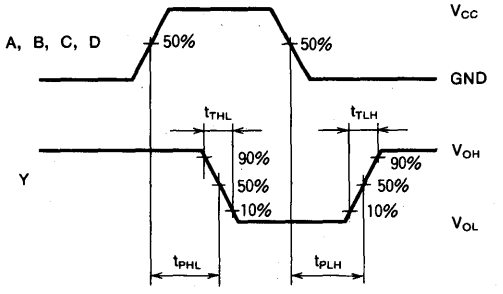
Note 2 : C_{PD} is the internal capacitance of the IC calculated from the operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are Subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC4017P/FP/DP

DECADE COUNTER/DIVIDER

DESCRIPTION

The M74HC4017 is a semiconductor integrated circuit consisting of a decimal counter with direct reset input and decode output.

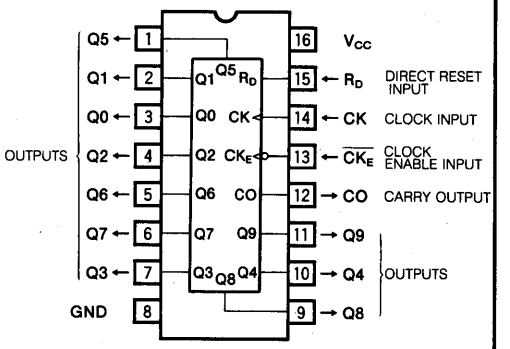
FEATURES

- High-speed: (clock frequency)40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4017 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS4017.

The M74HC4017 is a decade Johnson counter with decoded outputs, in which only one output is high at any time, the other outputs remaining at low.

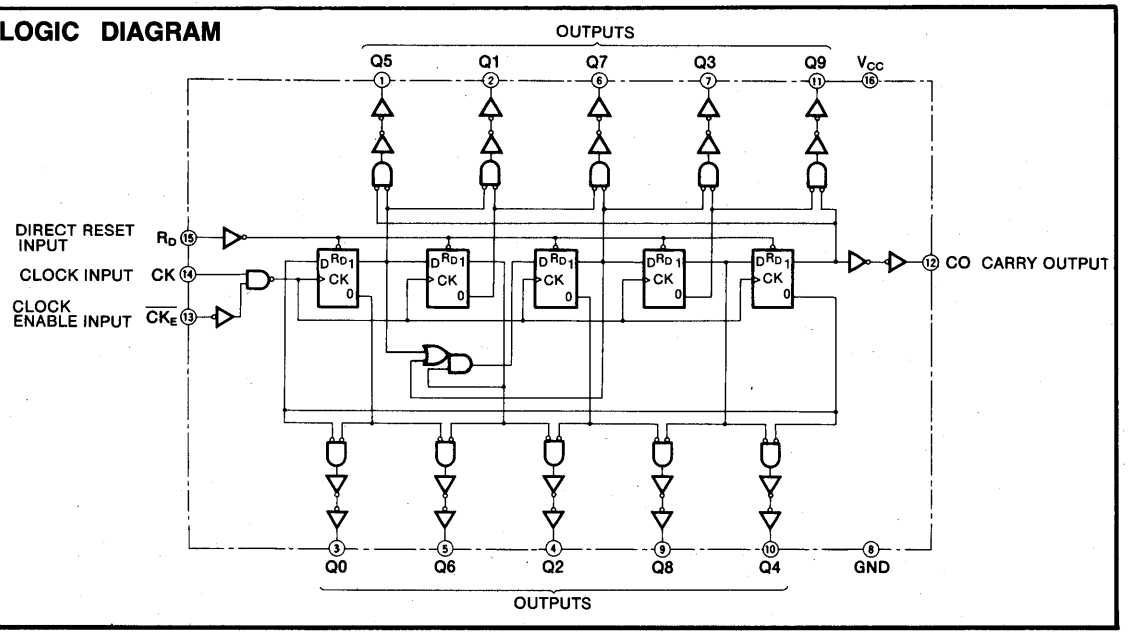
When clock enable input $\overline{CK_E}$ and direct reset input R_D are both held low, a pulse is applied to clock input CK, one output of Q0 through Q9 which corresponds to the number of counting pulses will become high. Counting takes place when CK changes from low-level to high-level.

When R_D is held low and CK is high, a clock pulse is applied to $\overline{CK_E}$, one output of Q0 through Q9 which corresponds to number of counting pulses will become high. Counting take place when $\overline{CK_E}$ changes from high-level to low-level.

When R_D is high, Q0 and carry-output CO both will become high, and Q1 through Q9 will become low, irrespective of other inputs.

When Q0 through Q4 are high, CO will become high, and when Q5 through Q9 are high, CO will become low, providing an output wavefrom with a 50% duty cycle.

LOGIC DIAGRAM

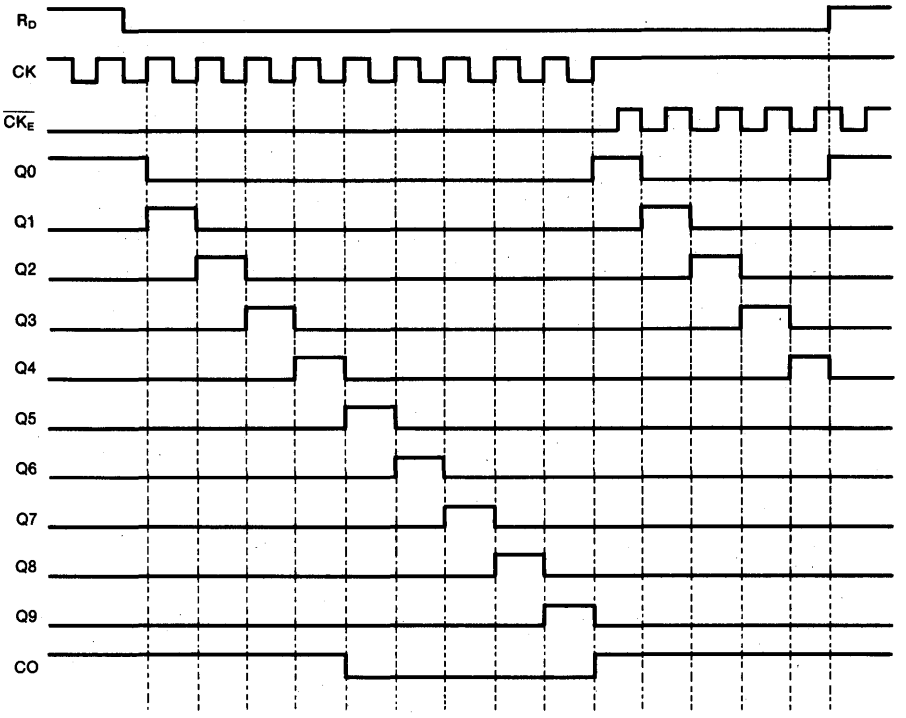


FUNCTION TABLE (Note 1)

Inputs			High-level output pin
CK	$\overline{CK_E}$	R_D	
X	X	H	Q0
X	H	L	Qn
L	X	L	
↑	L	L	Q_{n+1} (Counter operation)
↑	H	L	Qn
↓	X	L	
X	↑	L	
L	↓	L	
H	↓	L	Q_{n+1} (Counter operation)

Note 1 : X : Irrelevant
↑ : Change from low to high
↓ : Change from high to low
Qn : Indicates output pin which is high before the input condition is set.
n : 0 through 9, but when n is 9, Qn+1 becomes Q0.

OPERATIONAL TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC4017FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC4017DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				40	ns
t_{PHL}	output propagation time (CK − Q)				40	ns
t_{PLH}	Low-level to high-level and high-level to low-level				40	ns
t_{PHL}	output propagation time (CK − CO)				40	ns
t_{PLH}	Low-level to high-level and high-level to low-level				40	ns
t_{PHL}	output propagation time (R_D − Q)				40	ns
t_{PLH}	Low-level to high-level output propagation time (R_D − CO)				40	ns
t_{PLH}	Low-level to high-level and high-level to low-level				44	ns
t_{PHL}	output propagation time ($\overline{CK_E}$ − Q)				44	ns
t_{PLH}	Low-level to high-level and high-level to low-level				44	ns
t_{PHL}	output propagation time ($\overline{CK_E}$ − CO)				44	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

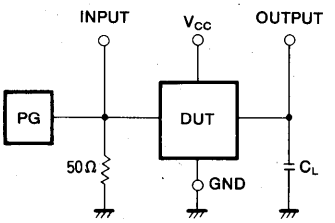
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	4			3		MHz
			4.5	20			16		
			6.0	24			19		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − CO)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (R_D − Q)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PLH}	Low-level to high-level output propagation time (R_D − CO)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK_E}$ − Q)		2.0			250		315	ns
			4.5			50		63	
			6.0			43		54	
t_{PHL}			2.0			250		315	ns
			4.5			50		63	
			6.0			43		54	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK_E}$ − CO)		2.0			250		315	ns
			4.5			50		63	
			6.0			43		54	
t_{PHL}			2.0			250		315	ns
			4.5			50		63	
			6.0			43		54	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

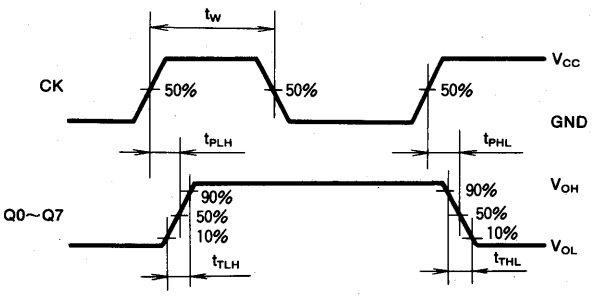
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{CK_E}$, R_D pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	$\overline{CK_E}$ setup time with respect to CK		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
t_{su}	CK setup time with respect to $\overline{CK_E}$		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
t_h	$\overline{CK_E}$ hold time with respect to CK		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
t_h	CK hold time with respect to $\overline{CK_E}$		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
t_{rec}	R_D recovery time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_{rec}	R_D recovery time with respect to $\overline{CK_E}$		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		

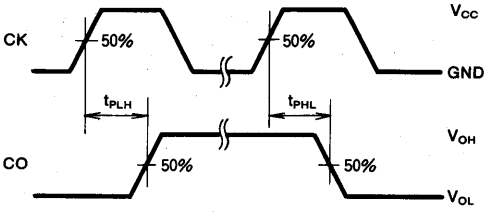
Note 4 : Test Circuit

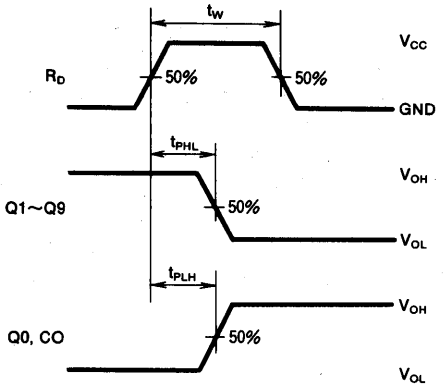


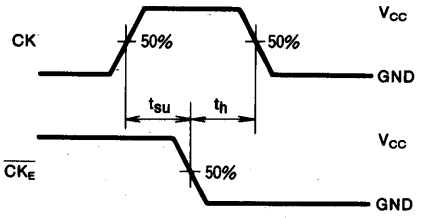
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

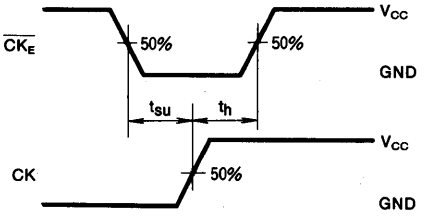
TIMING DIAGRAM

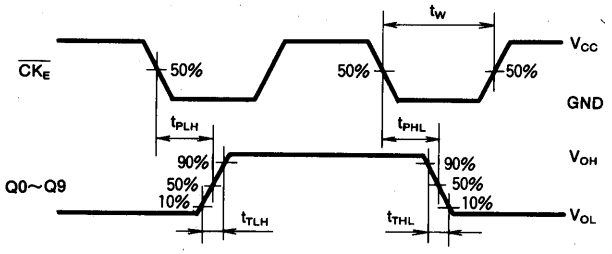


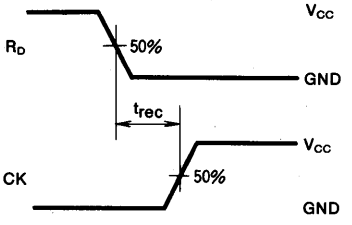


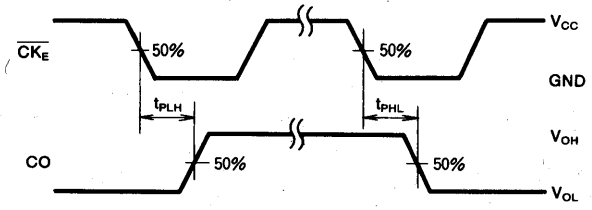

t_W
V_{CC}
R_D
50%
50%
GND
t_{PHL}
V_{OH}
Q1~Q9
50%
V_{OL}
t_{PLH}
V_{OH}
Q0, CO
50%
V_{OL}

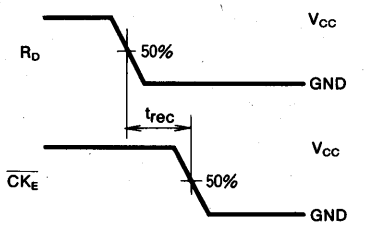

V_{CC}
CK
50%
50%
GND
t_{su}
t_h
V_{CC}
$\overline{CK_E}$
50%
GND


V_{CC}
$\overline{CK_E}$
50%
50%
GND
t_{su}
t_h
V_{CC}
CK
50%
GND


t_W
V_{CC}
$\overline{CK_E}$
50%
50%
50%
GND
t_{PLH}
t_{PHL}
V_{OH}
90%
90%
Q0~Q9
50%
50%
10%
10%
V_{OL}
t_{TLH}
t_{THL}


V_{CC}
R_D
50%
GND
t_{rec}
V_{CC}
CK
50%
GND


V_{CC}
$\overline{CK_E}$
50%
50%
GND
t_{PLH}
t_{PHL}
V_{OH}
CO
50%
50%
V_{OL}


V_{CC}
R_D
50%
GND
t_{rec}
V_{CC}
$\overline{CK_E}$
50%
GND

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC4020P/FP/DP

14-STAGE BINARY RIPPLE COUNTER

DESCRIPTION

The M74HC4020 is a semiconductor integrated circuit consisting of an asynchronous 14-stage binary counter with a direct reset input.

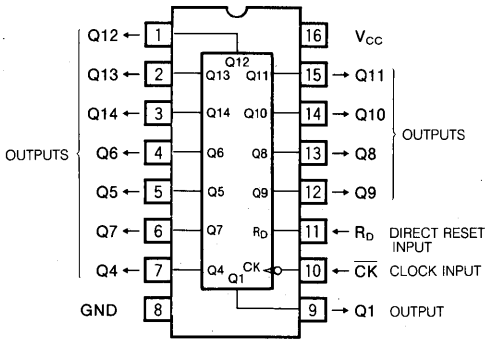
FEATURES

- High-speed: (clock-frequency) 40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N
16P2P

FUNCTIONAL DESCRIPTION

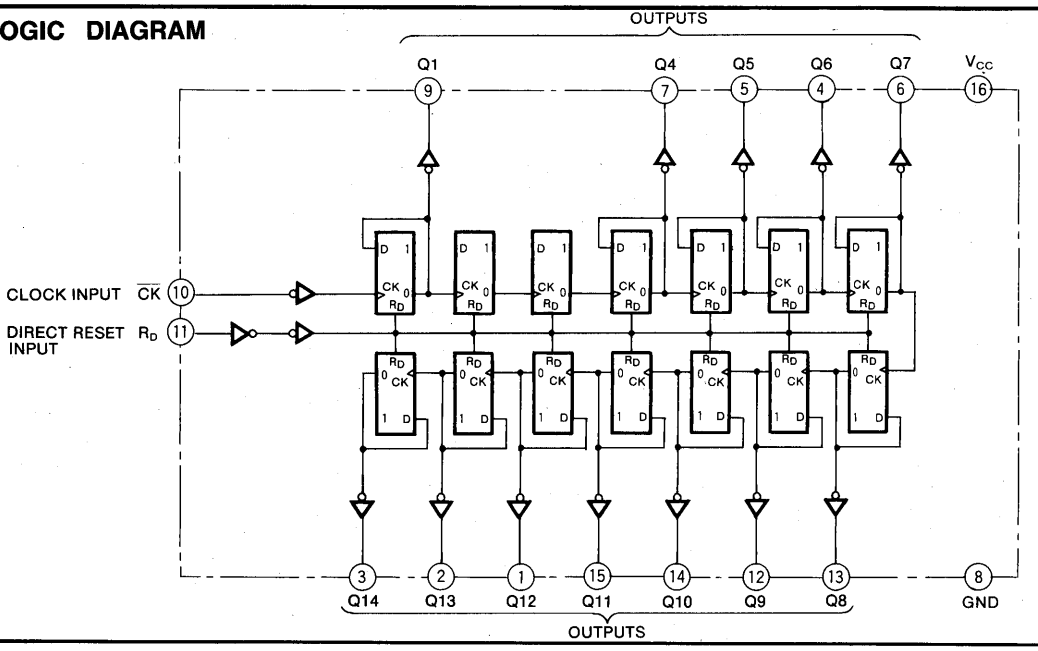
Use of silicon gate technology allows the M74HC4020 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to LSTTL.
The M74HC4020 contains a 14-stage master-slave flip-flop with independent outputs Q1 and Q4~Q14 at each flip-flop. When operated as a counter, the direct reset input R_D should be held low and a clock pulse applied at clock input $\overline{CK}$.
Counting takes place when $\overline{CK}$ changes from high-level to low-level. When R_D is set high, all flip-flops will be cleared and all outputs Q1 and Q4~Q14 will become low irrespective of $\overline{CK}$.

FUNCTION TABLE (Note 1)

Inputs		Output state
$\overline{CK}$	R_D	
X	H	All outputs are low-level
↑	L	No change
↓	L	Advance counter

Note 1 : X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC4020FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC4020DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q1)				35	ns
t_{PHL}					35	ns
t_{PHL}	High-level to low-level output propagation time (R_D − Q1, Q4~Q14)				40	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

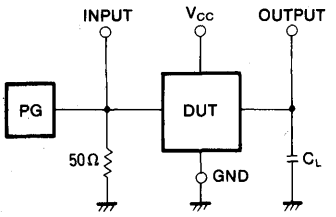
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	4			3		MHz
			4.5	20			16		
			6.0	24			19		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q1)		2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PHL}			2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PHL}	High-level to low-level output propagation time (R_D − Q1, Q4~Q14)		2.0			240		302	ns
			4.5			48		60	
			6.0			41		51	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

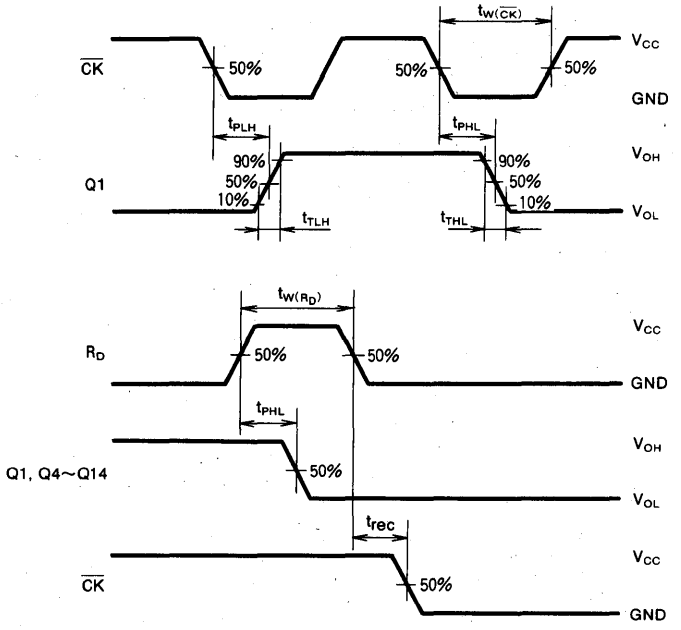
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W	$\overline{CK}$, R_D pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{rec}	R_D recovery time with respect to $\overline{CK}$		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are Subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC4022P/FP/DP

OCTAL COUNTER/DIVIDER

DESCRIPTION

The M74HC4022 is a semiconductor integrated circuit consisting of an octal counter with reset input and decode output.

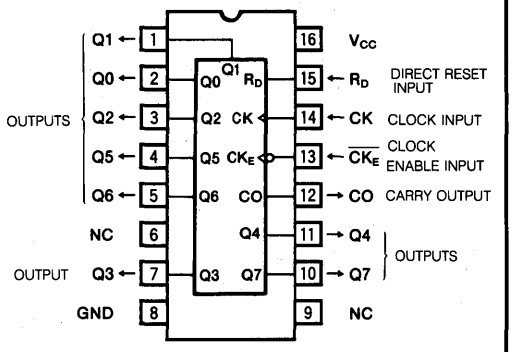
FEATURES

- High-speed: (clock frequency)40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



16P4
Outline 16P2N
16P2P NC : NO CONNECTION

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4022 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS4022.

The M74HC4022 is an octal Johnson counter with a decodered outputs, in which only one output in high at any time, the other outputs remaining at low.

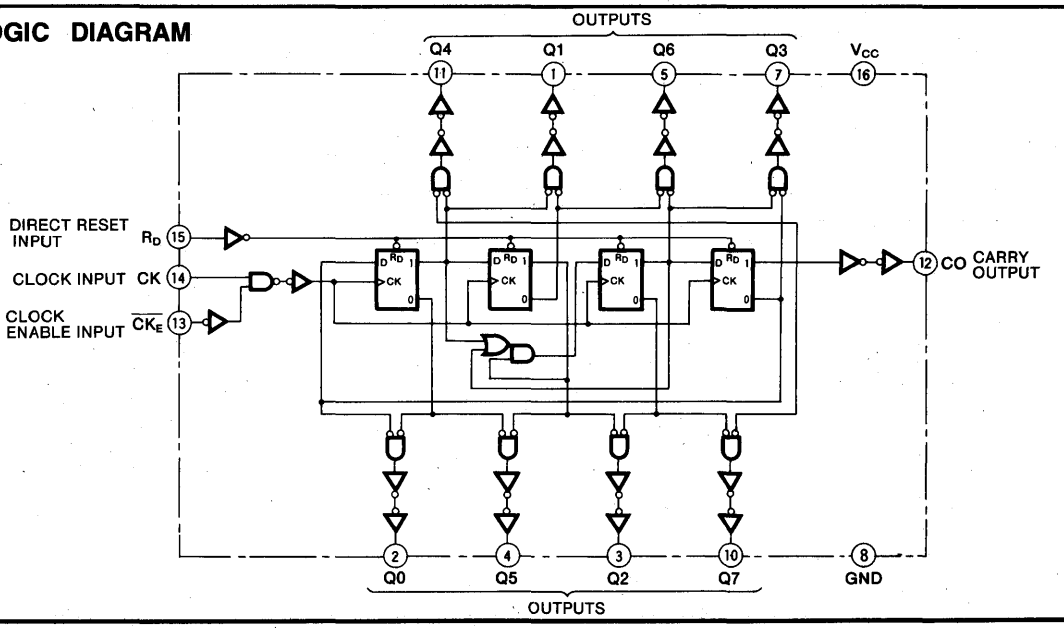
When clock enable input $\overline{CK_E}$ and direct reset input R_D are both held low, a clock pulse is applied to clock input CK, one output of Q0 through Q7 which corresponds to the number of counting pulses will become high. Counting takes place when CK changes from low-level to high-level.

When R_D is held low and CK is high, a clock pulse is applied to $\overline{CK_E}$, one output of Q0 though Q7 which corresponds to the number of counting pulses will become high. Counting takes place when $\overline{CK_E}$ changes from high-level to low-level.

When R_D is high, Q0 and carry-output CO will become high, and Q1 through Q7 will become low, irrespective of other inputs.

When Q0 through Q3 are high, CO will become high, and when Q4 through Q7 are high, CO will become low, providing an output wavefrom with a 50% duty cycle.

LOGIC DIAGRAM

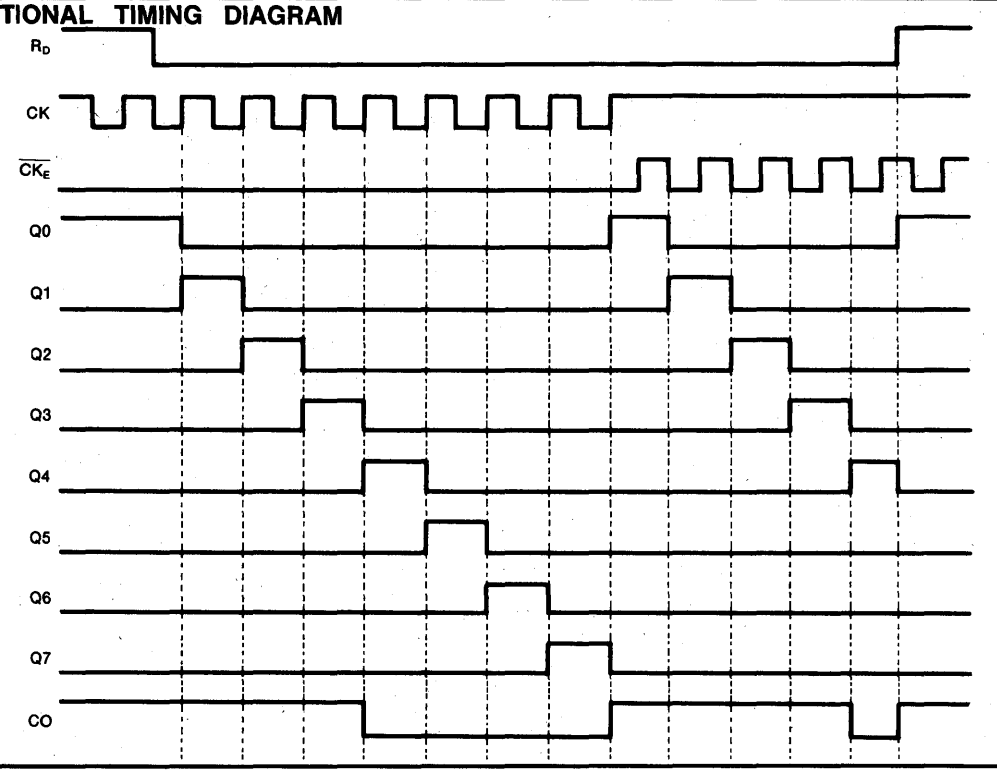


FUNCTION TABLE (Note 1)

Inputs			High-level output pin
CK	$\overline{CK_E}$	R_D	
X	X	H	Q0
X	H	L	Qn
L	X	L	
↑	L	L	Q_{n+1} (Counter operation)
↑	H	L	Qn
↓	L	L	
X	↑	L	
L	↓	L	
H	↓	L	Q_{n+1} (Counter operation)

Note 1 : X : Irrelevant
↑ : Change from low to high
↓ : Change from high to low
Qn : Indicates output pin which is high before the input condition is set.
n : 0 through 7, but when n is 7, Qn+1 becomes Q0.

OPERATIONAL TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC4022FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC4022DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				40	ns
t_{PHL}					40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − CO)				40	ns
t_{PHL}					40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (R_D − Q)				40	ns
t_{PHL}					40	
t_{PLH}	Low-level to high-level output propagation time (R_D − CO)				40	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK_E}$ − Q)				44	ns
t_{PHL}					44	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK_E}$ − CO)				44	ns
t_{PHL}					44	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

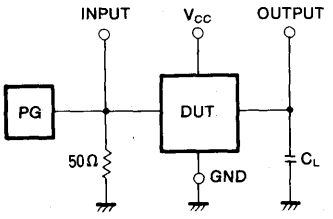
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	4			3		MHz
			4.5	20			16		
			6.0	24			19		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − CO)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (R_D − Q)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PLH}	Low-level to high-level output propagation time (R_D − CO)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK_E}$ − Q)		2.0			250		315	ns
			4.5			50		63	
			6.0			43		54	
t_{PHL}			2.0			250		315	ns
			4.5			50		63	
			6.0			43		54	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK_E}$ − CO)		2.0			250		315	ns
			4.5			50		63	
			6.0			43		54	
t_{PHL}			2.0			250		315	ns
			4.5			50		63	
			6.0			43		54	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

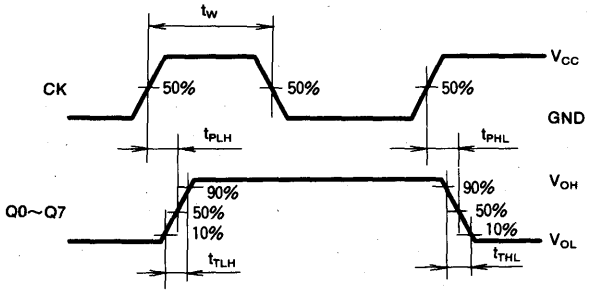
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{CK_E}$, R_D pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	$\overline{CK_E}$ setup time with respect to CK		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
t_{su}	CK setup time with respect to $\overline{CK_E}$		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
t_h	$\overline{CK_E}$ hold time with respect to CK		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
t_h	CK hold time with respect to $\overline{CK_E}$		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
t_{rec}	R_D recovery time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_{rec}	R_D recovery time with respect to $\overline{CK_E}$		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		

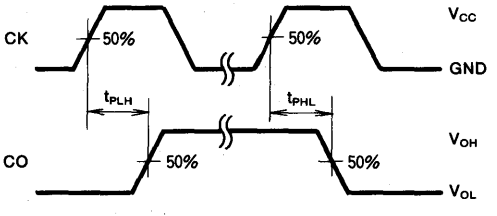
Note 4 : *Test Circuit*

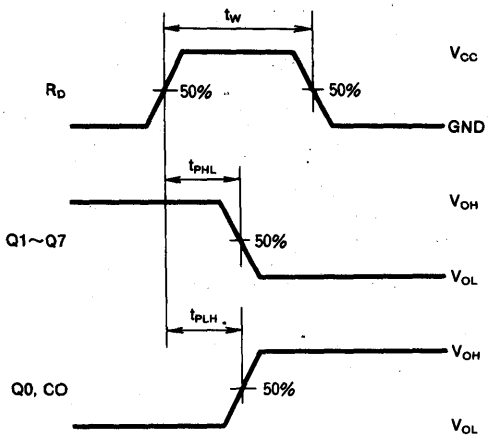


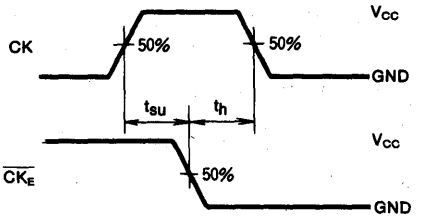
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

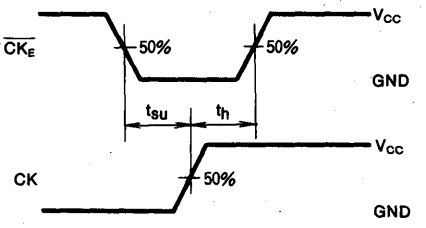
TIMING DIAGRAM

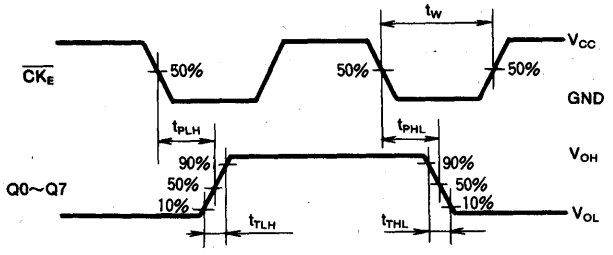


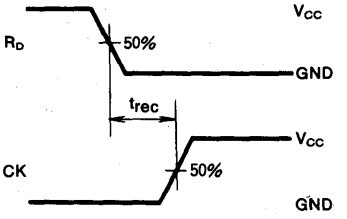


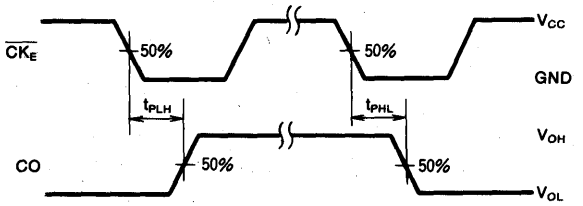


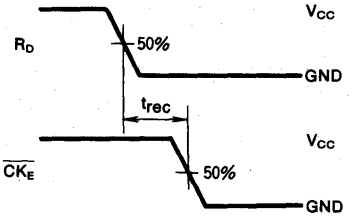












MITSUBISHI ELECTRIC

M74HC4024P/FP/DP

7-STAGE BINARY RIPPLE COUNTER

DESCRIPTION

The M74HC4024 is a semiconductor integrated circuit consisting of an asynchronous 7-stage binary counter with direct reset input.

FEATURES

- High-speed: (clock frequency) 70MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4024 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

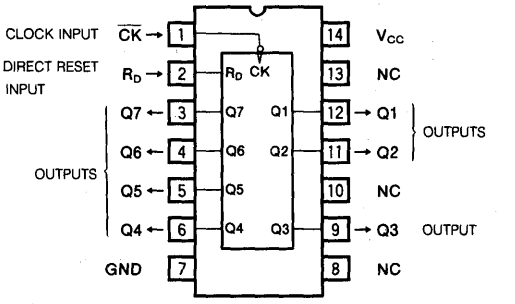
The M74HC4024 consists of a 7-stage master-slave flip-flop with independent output signals at each flip-flop.

When used as a counter, the direct reset input R_D is maintained low and the clock pulse applied at clock input $\overline{CK}$.

The counter operates when $\overline{CK}$ changes from high-level to low-level, and pure binary codes will appear at each output Q.

When direct reset input R_D is high, all flip-flop will be cleared and Q1 through Q7 all will become low irrespective of $\overline{CK}$.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

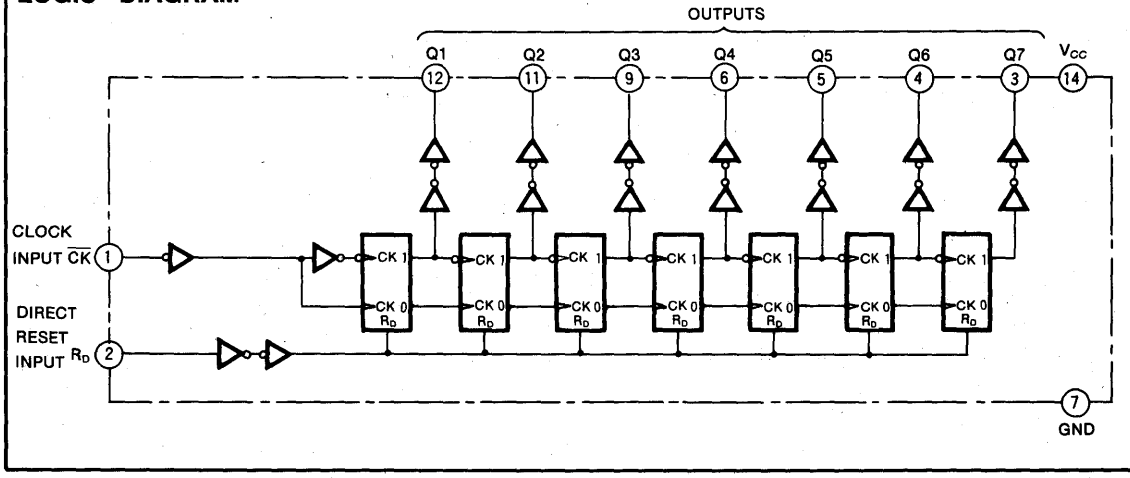
NC : NO CONNECTION

FUNCTION TABLE (Note 1)

Inputs		Output state
$\overline{CK}$	R_D	
X	H	All outputs are low-level
↑	L	No change
↓	L	Proceed to next state (counter operation)

Note 1 : X : Irrelevant
↑ : Change from low-level to high-level
↓ : Change from high-level to low-level

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC4024FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC4024DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q1)				35	ns
t_{PHL}					35	ns
t_{PHL}	High-level to low-level output propagation time (R_D − Q1~Q7)				35	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

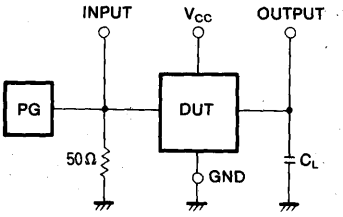
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q1)		2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PHL}			2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PHL}	High-level to low-level output propagation time (R_D − Q1~Q7)		2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				60				pF

Note 3 : C_{DP} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load condition is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENT (V_{CC} = 2~6V, T_a = −40~+85℃)

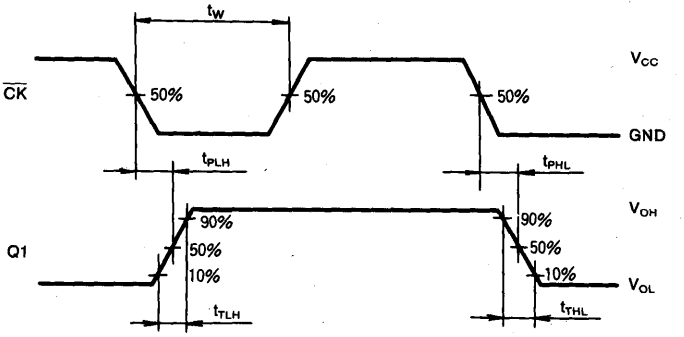
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W	$\overline{CK}$, R_D clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{rec}	R_D recovery time with respect to $\overline{CK}$		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		

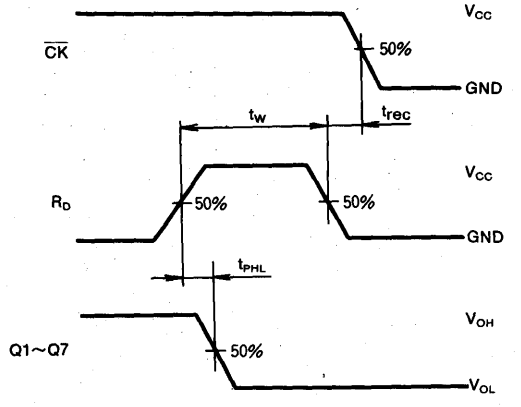
Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC4040P/FP/DP

12-STAGE BINARY RIPPLE COUNTER

DESCRIPTION

The M74HC4040 is a semiconductor integrated circuit consisting of an asynchronous 12-stage binary counter with a direct reset input.

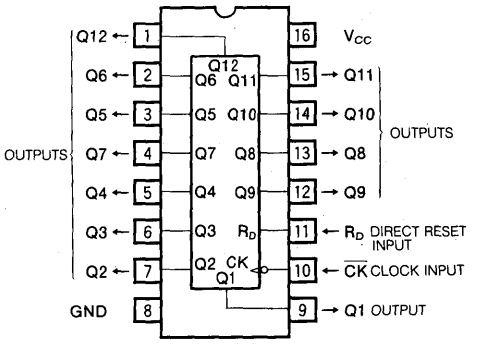
FEATURES

- High-speed: (clock frequency) 40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



16P4
Outline 16P2N
16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4040 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to LSTTL.

The M74HC4040 contains a 12-state master-slave flip-flop with independent outputs Q1~Q12 at each flip-flop.

When operated as a counter, the direct reset input R_D should be held low and a clock pulse applied at clock input $\overline{CK}$.

Counting takes place when $\overline{CK}$ changes from high-level to low-level, and pure binary code outputs appear at each outputs Q1~Q12.

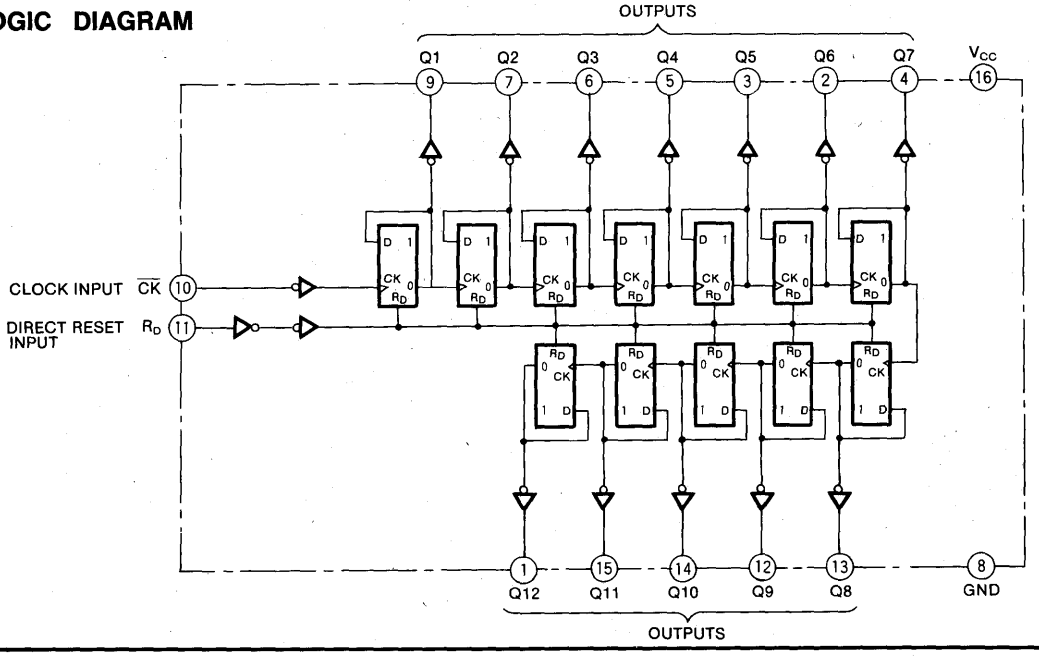
When R_D is set high, all flip-flops will be cleared and all outputs Q1~Q12 will become low irrespective of $\overline{CK}$.

FUNCTION TABLE (Note 1)

Inputs		Output state
$\overline{CK}$	R_D	
X	H	All outputs are low-level
↑	L	No change
↓	L	Advance counter

Note 1 : X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC4040FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC4040DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q1)				35	ns
t_{PHL}					35	ns
t_{PHL}	High-level to low-level output propagation time (R_D − Q1~Q12)				40	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

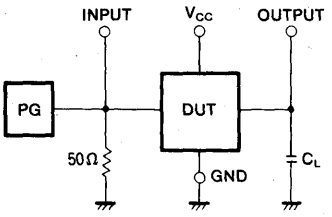
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	4			3		MHz
			4.5	20			16		
			6.0	24			19		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q1)		2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PHL}			2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PHL}	High-level to low-level output propagation time (R_D − Q1~Q12)		2.0			240		302	ns
			4.5			48		60	
			6.0			41		51	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

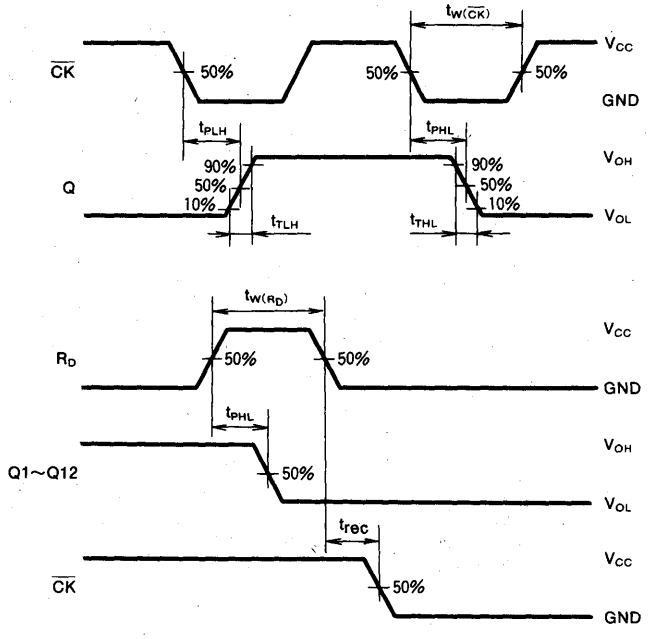
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, R_D pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{rec}	R_D recovery time with respect to $\overline{CK}$		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC4049BP/FP/DP

HEX INVERTING BUFFER/LOGIC-LEVEL DOWN CONVERTER

DESCRIPTION

The M74HC4049B is a semiconductor integrated circuit consisting of 6 built-in buffer/converter circuits with inverting outputs.

FEATURES

- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4049B to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

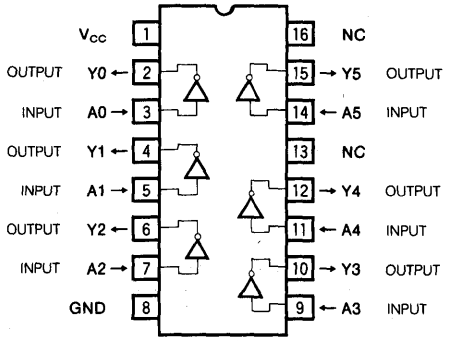
Unlike ordinary input protection circuits, inputs can be applied up to GND+15V, irrespective of V_{CC}, allowing the circuit to be used as logic-level converter from CMOS to high-speed CMOS/LSTTL logic circuits.

When input A is high, the output Y will become low, and when input A is low, the output Y will become high.

FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

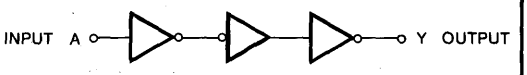
PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

NC : NO CONNECTION

LOGIC DIAGRAM (EACH BUFFER)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~+18	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC4049BFP, T_a = −40~+70℃ and T_a = 70~85℃ are derated at −6mW/℃
M74HC4049BDP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		15	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, I_{OH} = −20μA	2.0	1.9			1.9		V
		V_I = V_{IL}, I_{OH} = −20μA	4.5	4.4			4.4		
		V_I = V_{IL}, I_{OH} = −20μA	6.0	5.9			5.9		
		V_I = V_{IL}, I_{OH} = −6.0mA	4.5	4.18			4.13		
		V_I = V_{IL}, I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, I_{OL} = 20μA	2.0			0.1		0.1	V
		V_I = V_{IH}, I_{OL} = 20μA	4.5			0.1		0.1	
		V_I = V_{IH}, I_{OL} = 20μA	6.0			0.1		0.1	
		V_I = V_{IH}, I_{OL} = 6.0mA	4.5			0.26		0.33	
		V_I = V_{IH}, I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
		V_I = 15V	6.0			0.5		5.0	
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = 15V, GND, I_O = 0μA	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

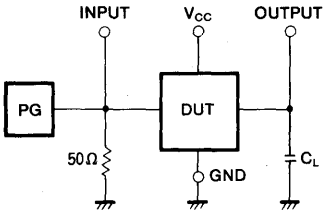
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time	C_L = 50pF (Note 3)	2.0			85		100	ns
			4.5			17		20	
			6.0			15		18	
t_{PHL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}		C_L = 50pF (Note 3)	2.0			127		150	ns
			4.5			25		30	
			6.0			22		27	
t_{PHL}			2.0			112		142	ns
			4.5			22		28	
			6.0			19		24	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				34				pF

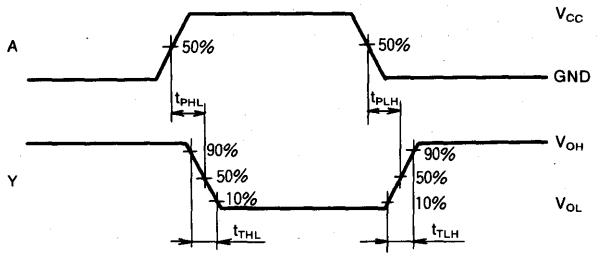
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC4050BP/FP/DP

HEX NONINVERTING BUFFER/LOGIC-LEVEL DOWN CONVERTER

DESCRIPTION

The M74HC4050B is a semiconductor integrated circuit consisting of 6 built-in buffer/converter circuits with noninverting outputs.

FEATURES

- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4050B to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

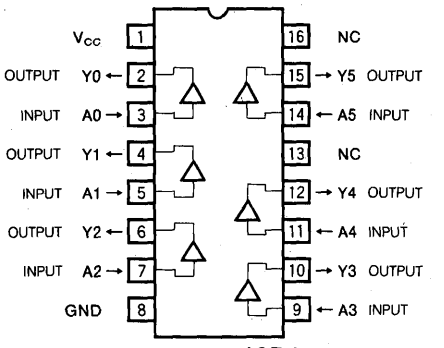
Unlike ordinary input protection circuits, inputs can be applied up to GND+15V, irrespective of V_{CC}, allowing the circuit to be used as logic-level converter from CMOS to high-speed CMOS/LSTTL logic circuits.

When input A is high, the output Y will become high, and when input A is low, the output Y will become low.

FUNCTION TABLE

Input	Output
A	Y
L	L
H	H

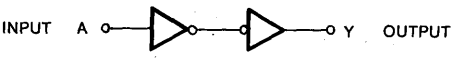
PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

NC : NO CONNECTION

LOGIC DIAGRAM (EACH BUFFER)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~+18	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC4050BFP, T_a = −40~+70℃ and T_a = 70~85℃ are derated at −6mW/℃.
M74HC4050BDP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

HEX NONINVERTING BUFFER/LOGIC-LEVEL DOWN CONVERTER

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		15	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −6.0mA	4.5	4.18			4.13		
		I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IL}, I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 6.0mA	4.5			0.26		0.33	
		I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
		V_I = 15V	6.0			0.5		5.0	
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = 15V, GND, I_O = 0μA	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

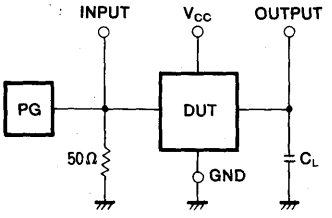
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time	C_L = 50pF (Note 3)	2.0			85		100	ns
			4.5			17		20	
			6.0			15		18	
t_{PHL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}		C_L = 50pF (Note 3)	2.0			127		150	ns
			4.5			25		30	
			6.0			22		27	
t_{PHL}			2.0			112		142	ns
			4.5			22		28	
			6.0			19		24	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				32				pF

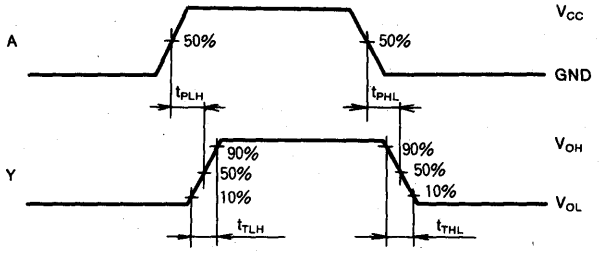
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC4051P/FP/DP

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

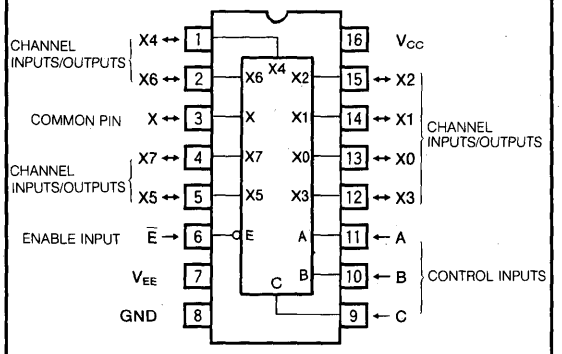
DESCRIPTION

The M74HC4051 is a semiconductor integrated circuit consisting of a multiplexer/demultiplexer which is capable of selecting between 8 analog switches with 3-input digital signal.

FEATURES

- Low on-state resistance
- High off-state resistance: more than $10^9\Omega$, typ.
- Excellent conductance linearity. Distortion 0.05% typ.
- Enable input
- High-speed: 18ns typ. (C_L = 50pF, V_{CC} = 4.5V, V_{EE} = GND)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, V_{EE}=GND, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Wide operating voltage range: $V_{CC}-V_{EE}$=2~12V
  V_{CC}-GND=2~6V
- Wide operating temperature range: T_a=−40~+85℃

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N
16P2P

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

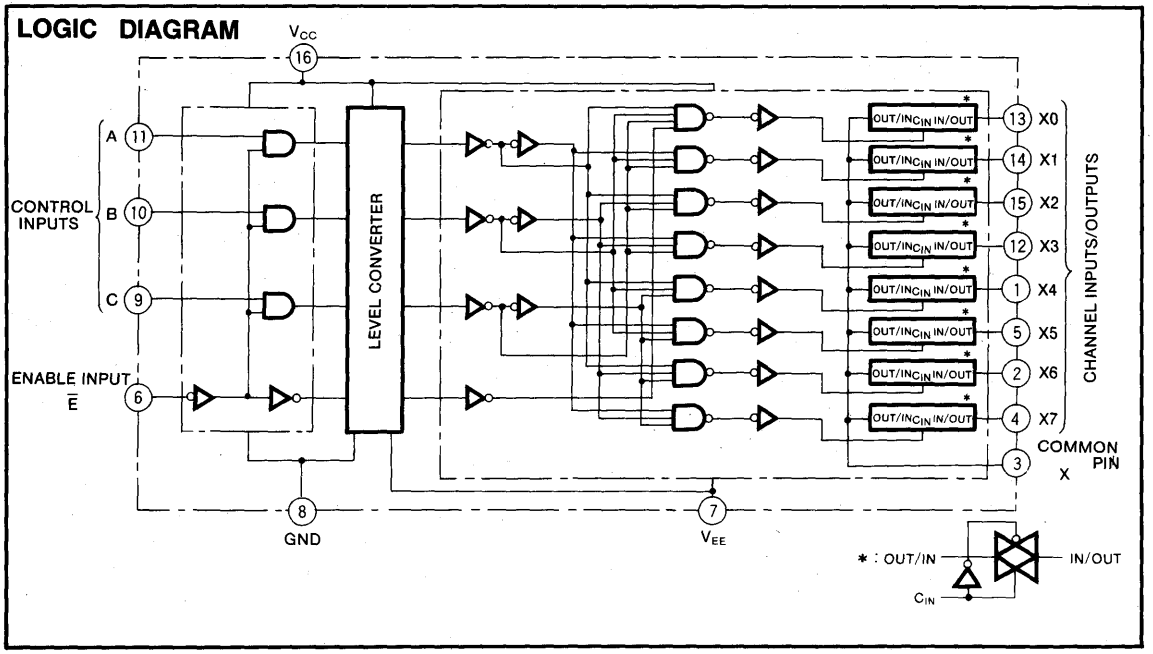
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4051 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

When a three-bit binary code is applied at control inputs A, B and C, the impedance between the common pin X and the selected channel X0 through X7 will become low-impedance state, and the other channels will become high-impedance state. In this case, when enable input $\overline{E}$ is high, all channels X0 through X7 will become high-impedance state, irrespective of other inputs.

Analog signals of amplitude V_{CC}-V_{EE} greater than logic amplitude V_{CC}-GND at A, B and C can be switched.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Enable input	Control inputs			Switch between channel input/output and common pin							
$\overline{E}$	C	B	A	X0	X1	X2	X3	X4	X5	X6	X7
L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	H	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	L	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
L	L	H	H	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
L	H	L	L	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
L	H	L	H	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
L	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
H	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Note 1 : X : Irrelevant
ON : Impedance between Xn and X is low. (n : 0~7)
OFF : Impedance between Xn and X is high. (n : 0~7)

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_{EE}			−7.0~+0.5	V
V_I	Input voltage	Control inputs, enable input	−0.5~V_{CC}+0.5	V
		I/O channels, common pin	V_{EE}−0.5~V_{CC}+0.5	
$V_{I/O}$	Input to output voltage		±0.5	V
V_O	Output voltage		V_{EE}−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_O	Output current per gate		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65~+150	℃

Note 2 : M74HC4051FP, T_a = −40~+70℃ and T_a = 70~85℃ are derated at −6mW/℃.
M74HC4051DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter			Limits			Unit
				Min	Typ	Max	
V_{CC}	Supply voltage			2.0		6.0	V
V_{EE}				0		−6.0	V
V_I	Input voltage	Control input, enable input		0		V_{CC}	V
		Channel input/output, common pin		V_{EE}		V_{CC}	
V_O	Output voltage			V_{EE}		V_{CC}	V
Topr	Ambient operating temperature			−40		+85	℃
t_r, t_f	Input risetime, falltime		V_{CC} = 2.0V	0		1000	ns
			V_{CC} = 4.5V	0		500	
			V_{CC} = 6.0V	0		400	

MITSUBISHI ELECTRIC

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits					Unit
					25℃			−40～+85℃		
			V_{EE}(V)	V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	Refer to R_{ON} specification	—	2.0	1.5			1.5		V
			—	4.5	3.15			3.15		
			—	6.0	4.2			4.2		
V_{IL}	Low-level input voltage	Refer to R_{ON} specification	—	2.0			0.5		0.5	V
			—	4.5			1.35		1.35	
			—	6.0			1.8		1.8	
R_{ON}	On-state resistance	$V_I = V_{IH}$ V_{IL}, $I_S = 0.1$mA V_{IS} = GND～V_{CC} (Test circuit 1)	GND	4.5			170		215	Ω
			−4.5	4.5			85		106	
			−6.0	6.0			50		63	
		$V_I = V_{IH}$ V_{IL}, $I_S = 0.1$mA V_{IS} = GND, V_{CC} (Test circuit 1)	GND	2.0						Ω
			GND	4.5			85		106	
			−4.5	4.5			63		78	
			−6.0	6.0			37		47	
ΔR_{ON}	On-state resistance variation (switch-to-switch in the same package)	$V_I = V_{IH}$, V_{IL} V_{IS} = GND～V_{CC}	GND	4.5						Ω
			−4.5	4.5						
			−6.0	6.0						
$I_{IZ(OFF)}$	Switch-off leakage current	$V_I = V_{IH}$, V_{IL}, V_{IS} = GND, V_{CC} $V_{OS} = V_{CC}$, GND	GND	6.0			±0.1		±1.0	μA
			−6.0	6.0			±0.2		±2.0	
$I_{IZ(ON)}$	Switch-on leakage current	$V_I = V_{IH}$, V_{IL}, V_{IS} = GND, V_{CC}	GND	6.0			±0.2		±2.0	μA
			−6.0	6.0			±0.4		±4.0	
I_{IH}	High-level input current	$V_I = 6$V	—	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	$V_I = 0$V	—	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent power dissipation	$V_I = V_{CC}$, GND, $I_O = 0\mu$A	GND	6.0			4.0		40.0	μA
			−6.0	6.0			8.0		80.0	

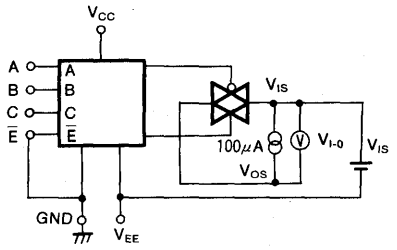
SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	V_{EE}(V)	V_{CC}(V)	Limits 25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
f_{max}	Maximum propagation frequency R_L = 1kΩ, V_{IS} = 1.6VRMS	C_L = 50pF (Test circuit 2)	−4.5	4.5						MHz
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (X0~X7 − X, X − X0~X7)	R_L = 1kΩ C_L = 50pF (Test circuit 3)	GND	2.0			60		75	ns
			GND	4.5			12		15	
			−4.5	4.5						
			−6.0	6.0						
t_{PHL}			GND	2.0			60		75	ns
			GND	4.5			12		15	
			−4.5	4.5						
			−6.0	6.0						
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B, C − X)	R_L = 1kΩ C_L = 50pF (Test circuit 8)	GND	2.0			370		465	ns
			GND	4.5			74		93	
			−4.5	4.5						
			−6.0	6.0						
t_{PHL}			GND	2.0			370		465	ns
			GND	4.5			74		93	
			−4.5	4.5						
			−6.0	6.0						
t_{PLZ}	Low-level and high-level output disable time (A, B, C − X0~X7 / $\overline{E}$ − X, X0~X7)	R_L = 1kΩ C_L = 50pF (Test circuit 4)	GND	2.0			290		365	ns
			GND	4.5			58		73	
			−4.5	4.5						
			−6.0	6.0						
t_{PHZ}			GND	2.0			290		365	ns
			GND	4.5			58		73	
			−4.5	4.5						
			−6.0	6.0						
t_{PZL}	Low-level and high-level output enable time (A, B, C − X0~X7 / $\overline{E}$ − X, X0~X7)		GND	2.0			345		435	ns
			GND	4.5			69		87	
			−4.5	4.5						
			−6.0	6.0						
t_{PZH}			GND	2.0			345		435	ns
			GND	4.5			69		87	
			−4.5	4.5						
			−6.0	6.0						
	Sine wave propagation dissipation	V_{IS} = 1.6VRMS R_L = 10kΩ (Test circuit 5)	−4.5	4.5						%
	Feedthrough (switch off)	V_{IS} = 1.6VRMS R_L = 10kΩ C_L = 50pF (Test circuit 2)	−4.5	4.5						MHz
	Crosstalk (control input, enable input-to-switch output)	R_L = 10kΩ R_l = 1kΩ C_L = 50pF (Test circuit 6)	−4.5	4.5						mV_{P-P}
	Crosstalk (switch-to-switch)	R_L = 1kΩ, C_L = 50pF (Test circuit 7)	−4.5	4.5						MHz
C_I	Input capacitance — Control input						10		10	pF
	Input capacitance — Channel input/output									
	Input capacitance — Common pin									
C_I	Feedthrough capacitance									pF
C_{PD}	Power dissipation capacitance (Note 3)									pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

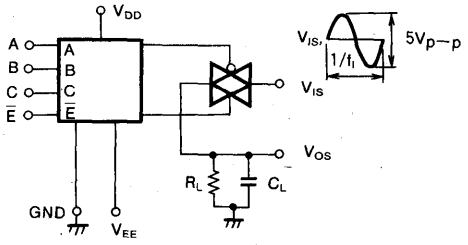
Test Circuit

1. *On-state resistance*

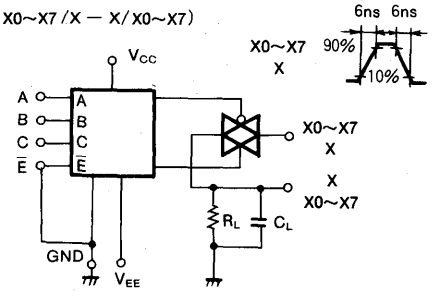


$$R_{ON} = \frac{V_{I-O}}{10^{-4}} (\Omega)$$

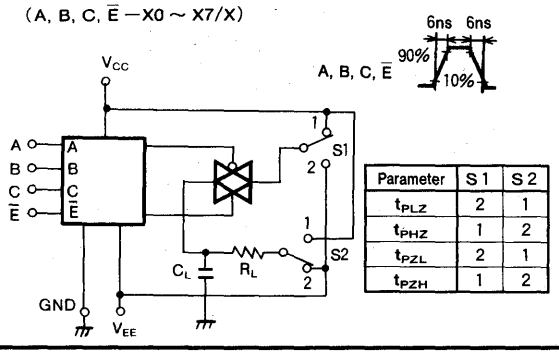
2. *Maximum propagation frequency, fiedthrough (switch off)*



3. Low-level to high-level and high-level to low-level propagation time
(X0~X7 /X − X/ X0~X7)

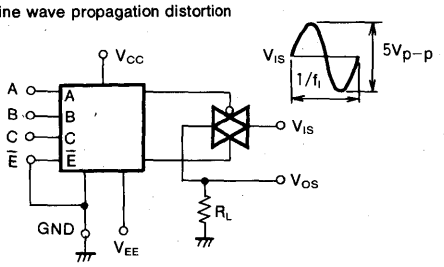


4. Low-level to high-level and high-level to low-level output propagation time, output enable, disable time
(A, B, C, $\overline{E}$ −X0 ~ X7/X)

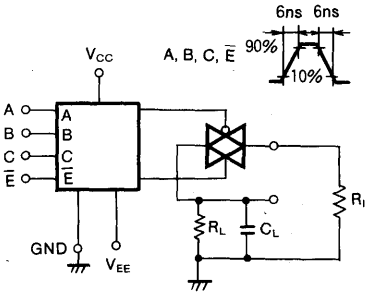


Parameter	S1	S2
t_{PLZ}	2	1
t_{PHZ}	1	2
t_{PZL}	2	1
t_{PZH}	1	2

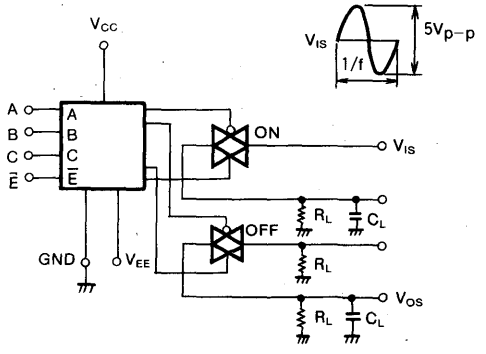
5. Sine wave propagation distortion



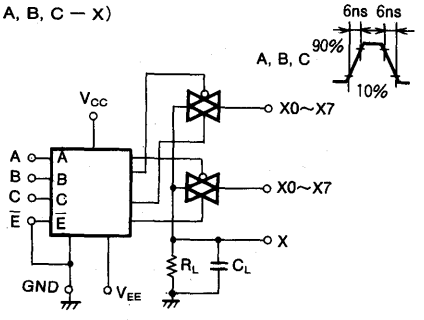
6. Crosstalk (control input enable input)



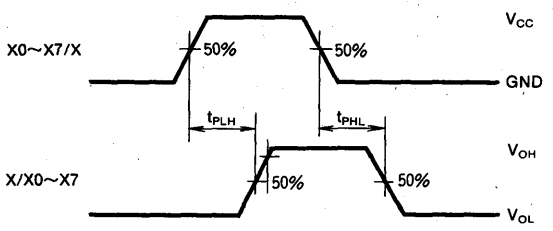
7. Crosstalk (switch-to-switch)

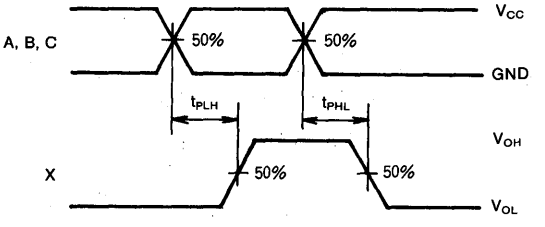


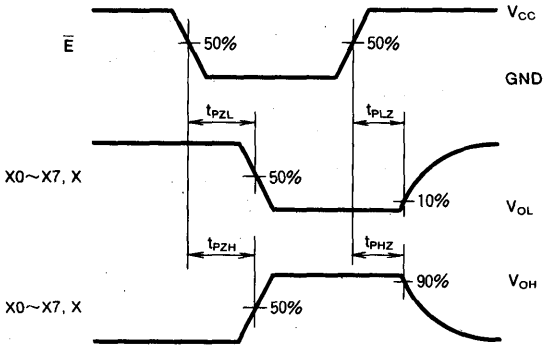
8. Low-level to high-level and high-level to low-level propagation time (A, B, C − X)

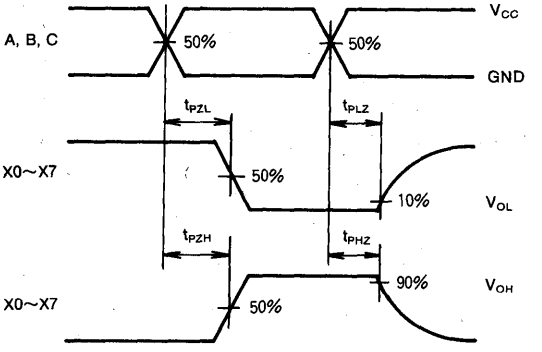


TIMING DIAGRAM









MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC4052P/FP/DP

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION

The M74HC4052 is a semiconductor integrated circuit consisting of two multiplexer/demultiplexers capable of selecting between 4 analog switches with 2-input digital signal.

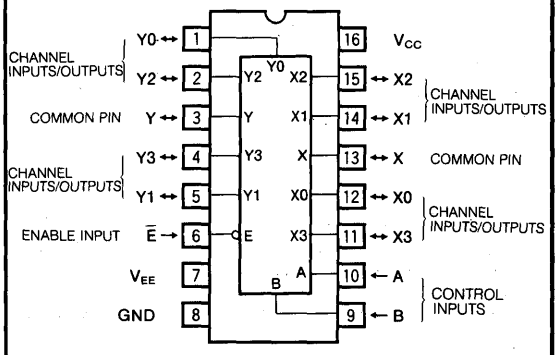
FEATURES

- Low on-state registance
- High off-state resistance: more than $10^9\Omega$, typ.
- Excellent conductance linearity
- Enable input
- High-speed: 28ns typ. (C_L = 50pF, V_{CC} = 4.5V, V_{EE} = GND)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, V_{EE}=GND, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Wide operating voltage range: $V_{CC}-V_{EE}$=2~12V
  V_{CC}−GND=2~12V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



16P4
Outline 16P2N
16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4052 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

When a two-bit binary code is applied at control inputs A and B, the impedance between common pin X and the selected channel X0 through X3 will become low, and the other channels will become high-impedance state. The impedance between common pin Y and channels Y0 through Y3 is controlled in the same way. In this case, when enable input $\overline{E}$ is high, all channels X0 through X3 and Y0 through Y3 will become high-impedance state, irrespective of other inputs.

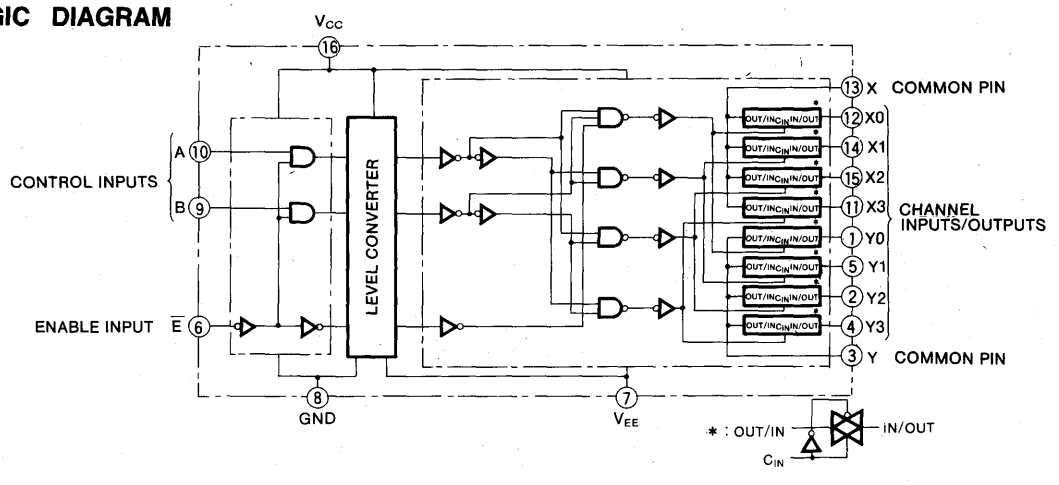
Analog signals of amplitude $V_{CC} - V_{EE}$ greater than logic amplitude V_{CC}−GND at A and B can be switched.

FUNCTION TABLE (Note 1)

Enable input	Control inputs		Switch between channel input/output and common pin			
$\overline{E}$	B	A	X0, Y0	X1, Y1	X2, Y2	X3, Y3
L	L	L	ON	OFF	OFF	OFF
L	L	H	OFF	ON	OFF	OFF
L	H	L	OFF	OFF	ON	OFF
L	H	H	OFF	OFF	OFF	ON
H	X	X	OFF	OFF	OFF	OFF

Note 1 : X : Irrelevant
ON : Impedance between Xn and X, and between Yn and Y is low. (n : 0~3)
OFF : Impedance between Xn and X, and btween Yn and Y is high. (n : 0~3)

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_{EE}			−7.0∼+0.5	V
V_I	Input voltage	Control inputs, enable inputs	−0.5∼V_{CC}+0.5	V
		I/O channels, common pins	V_{EE}−0.5∼V_{CC}+0.5	
$V_{I/O}$	Input to output voltage		±0.5	V
V_O	Output voltage		V_{EE}−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_O	Output current per gate		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼+150	℃

Note 2 : M74HC4052FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC4052DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2.0		6.0	V
V_{EE}			0		−6.0	V
V_I	Input voltage	Control input, enable input	0		V_{CC}	V
		Channel input/output, common pin	V_{EE}		V_{CC}	
V_O	Output voltage		V_{EE}		V_{CC}	V
Topr	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits					Unit
					25℃			−40∼+85℃		
			V_{EE}(V)	V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	Refer to R_{ON} specification	—	2.0	1.5			1.5		V
			—	4.5	3.15			3.15		
			—	6.0	4.2			4.2		
V_{IL}	Low-level input voltage	Refer to R_{ON} specification	—	2.0			0.5		0.5	V
			—	4.5			1.35		1.35	
			—	6.0			1.8		1.8	
R_{ON}	On-state resistance	V_I = V_{IH} V_{IL}, I_S = 0.1mA V_{IS} = GND∼V_{CC} (Test circuit 1)	GND	4.5			170		215	Ω
			−4.5	4.5			85		106	
			−6.0	6.0			50		63	
		V_I = V_{IH} V_{IL}, I_S = 0.1mA V_{IS} = GND, V_{CC} (Test circuit 1)	GND	2.0						Ω
			GND	4.5			85		106	
			−4.5	4.5			63		78	
			−6.0	6.0			37		47	
ΔR_{ON}	On-state resistance variation (switch-to-switch in the same package)	V_I = V_{IH}, V_{IL} V_{IS} = GND∼V_{CC}	GND	4.5						Ω
			−4.5	4.5						
			−6.0	6.0						
$I_{IZ(OFF)}$	Switch-off leakage current	V_I = V_{IH}, V_{IL}, V_{IS} = GND, V_{CC} V_{OS} = V_{CC}, GND	GND	6.0			±0.1		±1.0	μA
			−6.0	6.0			±0.2		±2.0	
$I_{IZ(ON)}$	Switch-on leakage current	V_I = V_{IH}, V_{IL}, V_{IS} = GND, V_{CC}	GND	6.0			±0.2		±2.0	μA
			−6.0	6.0			±0.4		±4.0	
I_{IH}	High-level input current	V_I = 6V	—	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	—	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent power dissipation	V_I = V_{CC}, GND, I_O = 0μA	GND	6.0			4.0		40.0	μA
			−6.0	6.0			8.0		80.0	

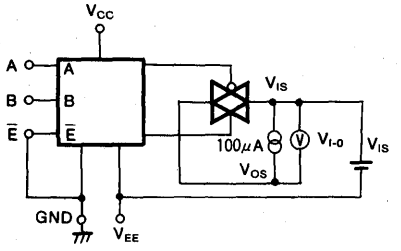
SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	V_{EE}(V)	V_{CC}(V)	Limits 25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
f_{max}	Maximum propagation frequency R_L = 1kΩ, V_{IS} = 1.6VRMS	C_L = 50pF (Test circuit 2)	−4.5	4.5						MHz
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (X0~X3−X, X−X0~X3 Y0~Y3−Y, Y−Y0~Y3)	R_L = 1kΩ C_L = 50pF (Test circuit 3)	GND	2.0			60		75	ns
			GND	4.5			12		15	
			−4.5	4.5						
			−6.0	6.0						
t_{PHL}			GND	2.0			60		75	ns
			GND	4.5			12		15	
			−4.5	4.5						
			−6.0	6.0						
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − X, Y)	R_L = 1kΩ C_L = 50pF (Test circuit 8)	GND	2.0			370		465	ns
			GND	4.5			74		93	
			−4.5	4.5						
			−6.0	6.0						
t_{PHL}			GND	2.0			370		465	ns
			GND	4.5			74		93	
			−4.5	4.5						
			−6.0	6.0						
t_{PLZ}	Low-level and high-level output disable time (A, B−X0~X3,Y0~Y3 $\overline{E}$−X, X0~X3, Y, Y0~Y3)	R_L = 1kΩ C_L = 50pF (Test circuit 4)	GND	2.0			290		365	ns
			GND	4.5			58		73	
			−4.5	4.5						
			−6.0	6.0						
t_{PHZ}			GND	2.0			290		365	ns
			GND	4.5			58		73	
			−4.5	4.5						
			−6.0	6.0						
t_{PZL}	Low-level and high-level output enable time (A, B−X0~X3, Y0~Y3 $\overline{E}$−X, X0~X3, Y, Y0~Y3)		GND	2.0			345		435	ns
			GND	4.5			69		87	
			−4.5	4.5						
			−6.0	6.0						
t_{PZH}			GND	2.0			345		435	ns
			GND	4.5			69		87	
			−4.5	4.5						
			−6.0	6.0						
	Sine wave propagation distortion	V_{IS} = 1.6VRMS R_L = 10kΩ (Test circuit 5)	−4.5	4.5						%
	Feedthrough (switch off)	V_{IS} = 1.6VRMS R_L = 10kΩ C_L = 50pF (Test circuit 2)	−4.5	4.5						MHz
	Crosstalk (control input, enable input-to-switch outputs)	R_L = 10kΩ R_I = 1kΩ C_L = 50pF (Test circuit 6)	−4.5	4.5						mV_{P-P}
	Crosstalk (switch-to-switch)	R_L = 1kΩ, C_L = 50pF (Test circuit 7)	−4.5	4.5						MHz
C_I	Input capacitance — Control input						10		10	pF
	Input capacitance — Channel input/output									
	Input capacitance — Common pin									
C_I	Feedthrough capacitance									pF
C_{PD}	Power dissipation capacitance (Note 2)									pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

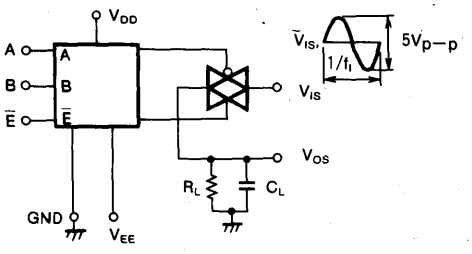
Test Circuit

1. On-state resistance

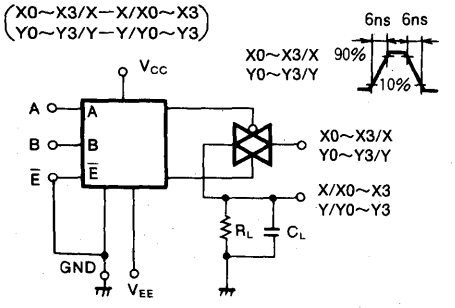


$$R_{ON} = \frac{V_{I-O}}{10^{-4}} (\Omega)$$

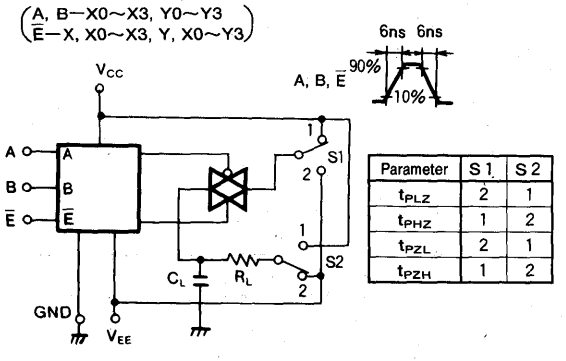
2. Maximum propagation frequency, fieldthrough (switch off)



3. Low-level to high-level and high-level to low-level propagation time

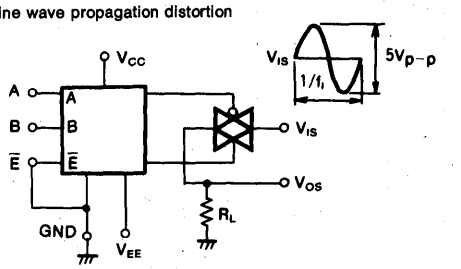


4. Low-level to high-level and high-level to low-level output propagation time, output enable, disable time

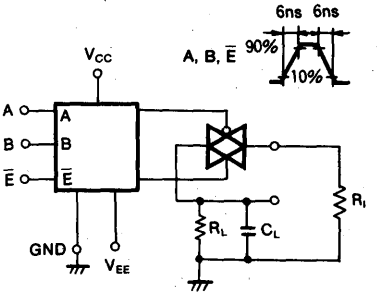


Parameter	S1	S2
t_{PLZ}	2	1
t_{PHZ}	1	2
t_{PZL}	2	1
t_{PZH}	1	2

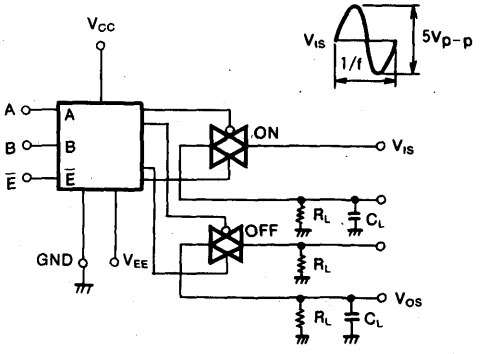
5. Sine wave propagation distortion



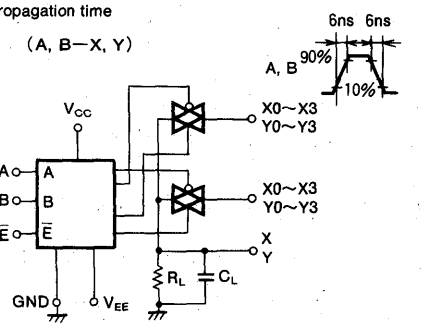
6. Crosstalk (control input, enable input)



7. Crosstalk (switch-to-switch)

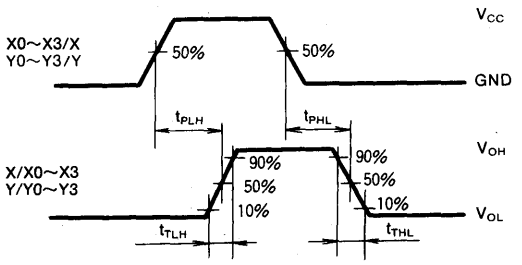


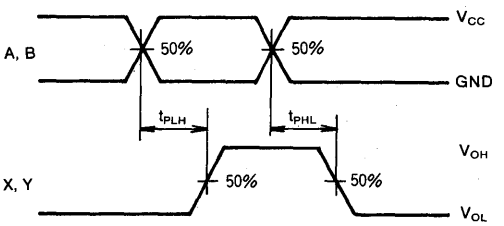
8. Low-level to high-level and high-level to low-level propagation time

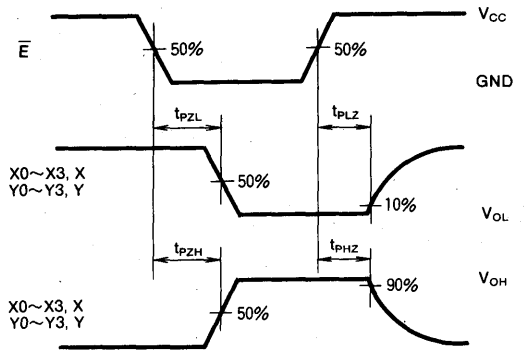


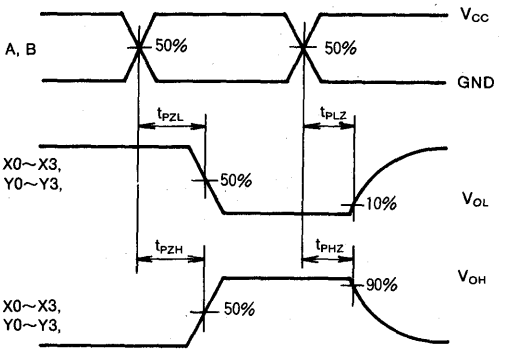
MITSUBISHI ELECTRIC

TIMING DIAGRAM









PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC4053P/FP/DP

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION

The M74HC4053 is a semiconductor integrated circuit consisting of three multiplexers/demultiplexers capable of selecting between 2 analog switches.

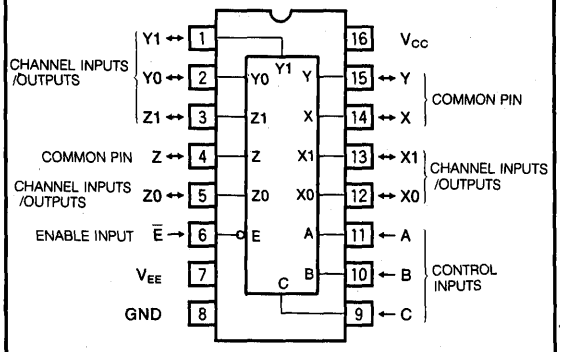
FEATURES

- Low on-state resistance
- High off-state resistance: more than $10^9\Omega$, typ.
- Excellent conductance linearity
- Enable input
- High-speed: 28ns typ. (C_L = 50pF, V_{CC} = 4.5V, V_{EE} = GND)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, V_{EE}=GND, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Wide operating voltage range: $V_{CC}-V_{EE}$=2~6V
  V_{CC}-GND=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



16P4
Outline 16P2N
16P2P

Analog signals of amplitude V_{CC}-V_{EE} greater than logic amplitude V_{CC}-GND at A, B and C can be switched.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4053 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS4053.

When a one-bit binaly code is applied at control inputs A, B and C, the impedance between the common pin and the selected channel will become low, and the other channels will become high-impedance state.

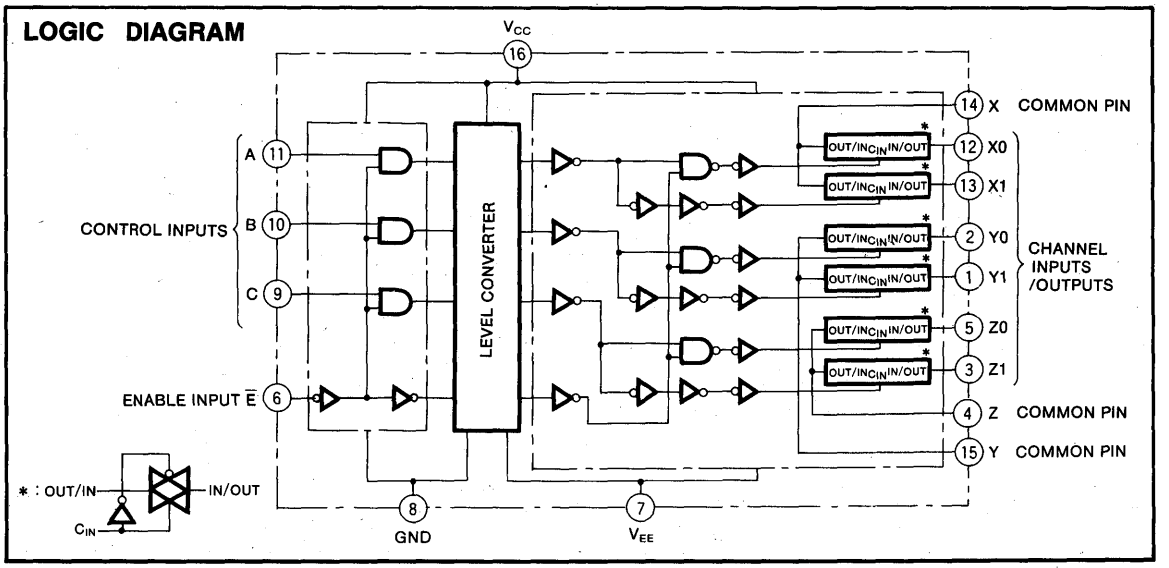
In this case, when enable input $\overline{E}$ is high, all channels will become high-impedance state, irrespective of other inputs.

FUNCTION TABLE (Note 1)

Enable input	Control inputs	Switches between chanel inputs/outputs and common pin	
$\overline{E}$	A, B, C	X0, Y0, Z0	X1, Y1, Z1
L	L	ON	OFF
L	H	OFF	ON
H	X	OFF	OFF

Note 1 : X : Irrelevant
ON : Impedance between Xn and X, Yn and Zn and Z is low (n : 0, 1)
OFF : Impedance between Xn and X, Yn and Y, and Zn and Z is high (n : 0, 1)

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_{EE}			−7.0∼+0.5	V
V_I	Input voltage	Control input, enable input	−0.5∼V_{CC}+0.5	V
		Channel input/output, common pin	V_{EE}−0.5∼V_{CC}+0.5	V
$V_{I/O}$	Input to output voltage		±0.5	V
V_O	Output voltage		V_{EE}−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_O	Output current per gate		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼+150	℃

Note 2 : M74HC4053FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC4053DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2.0		6.0	V
V_{EE}			0		−6.0	V
V_I	Input voltage	Control input, enable input	0		V_{CC}	V
		Channel input/output, common pin	V_{EE}		V_{CC}	
V_O	Output voltage		V_{EE}		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits					Unit
					25℃			−40∼+85℃		
			V_{EE}(V)	V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	Refer to R_{ON} specification	—	2.0	1.5			1.5		V
			—	4.5	3.15			3.15		
			—	6.0	4.2			4.2		
V_{IL}	Low-level input voltage	Refer to R_{ON} specification	—	2.0			0.5		0.5	V
			—	4.5			1.35		1.35	
			—	6.0			1.8		1.8	
R_{ON}	On-state resistance	V_I = V_{IH} V_{IL}, I_S = 0.1mA V_{IS} = GND∼V_{CC} (Test circuit 1)	GND	4.5			170		215	Ω
			−4.5	4.5			85		106	
			−6.0	6.0			50		63	
		V_I = V_{IH} V_{IL}, I_S = 0.1mA V_{IS} = GND, V_{CC} (Test circuit 1)	GND	2.0						Ω
			GND	4.5			85		106	
			−4.5	4.5			63		78	
			−6.0	6.0			37		47	
ΔR_{ON}	On-state resistance variation (switch-to-switch in the same package)	V_I = V_{IH}, V_{IL} V_{IS} = GND∼V_{CC}	GND	4.5						Ω
			−4.5	4.5						
			−6.0	6.0						
$I_{IZ(OFF)}$	Switch-off leakage current	V_I = V_{IH}, V_{IL}, V_{IS} = GND, V_{CC} V_{OS} = V_{CC}, GND	GND	6.0			±0.1		±1.0	μA
			−6.0	6.0			±0.2		±2.0	
$I_{IZ(ON)}$	Switch-on leakage current	V_I = V_{IH}, V_{IL}, V_{IS} = GND, V_{CC}	GND	6.0			±0.2		±2.0	μA
			−6.0	6.0			±0.4		±4.0	
I_{IH}	High-level input current	V_I = 6V	—	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	—	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent power dissipation	V_I = V_{CC}, GND, I_O = 0μA	GND	6.0			4.0		40.0	μA
			−6.0	6.0			8.0		80.0	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

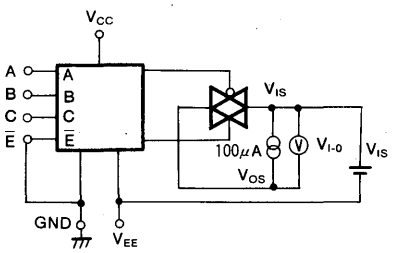
Symbol	Parameter	Test conditions	V_{EE}(V)	V_{CC}(V)	Limits 25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
f_{max}	Maximum propagation frequency R_L = 1kΩ, V_{IS} = 1.6VRMS	C_L = 50pF (Test circuit 2)	−4.5	4.5						MHz
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (X0, X1−X/X−X0, X1 Y0, Y1−Y/Y−Y0, Y1 Z0, Z1−Z/Z−Z0, Z1)	R_L = 1kΩ C_L = 50pF (Test circuit 3)	GND	2.0			60		75	ns
			GND	4.5			12		15	
			−4.5	4.5						
			−6.0	6.0						
t_{PHL}			GND	2.0			60		75	ns
			GND	4.5			12		15	
			−4.5	4.5						
			−6.0	6.0						
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A−X B−Y C−Z)	R_L = 1kΩ C_L = 50pF (Test circuit 8)	GND	2.0			370		465	ns
			GND	4.5			74		93	
			−4.5	4.5						
			−6.0	6.0						
t_{PHL}			GND	2.0			370		465	ns
			GND	4.5			74		93	
			−4.5	4.5						
			−6.0	6.0						
t_{PLZ}	Low-level and high-level output disable time (A−X0, X1/$\overline{E}$−X, X0, X1 B−Y0, Y1/$\overline{E}$−Y, Y0, Y1 C−Z0, Z1/$\overline{E}$−Z, Z0, Z1)	R_L = 1kΩ C_L = 50pF (Test circuit 4)	GND	2.0			290		365	ns
			GND	4.5			58		73	
			−4.5	4.5						
			−6.0	6.0						
t_{PHZ}			GND	2.0			290		365	ns
			GND	4.5			58		73	
			−4.5	4.5						
			−6.0	6.0						
t_{PZL}	Low-level and high-level output enable time (A−X0, X1/$\overline{E}$−X, X0, X1 B−Y0, Y1/$\overline{E}$−Y, Y0, Y1 C−Z0, Z1/$\overline{E}$−Z, Z0, Z1)		GND	2.0			345		435	ns
			GND	4.5			69		87	
			−4.5	4.5						
			−6.0	6.0						
t_{PZH}			GND	2.0			345		435	ns
			GND	4.5			69		87	
			−4.5	4.5						
			−6.0	6.0						
	Sine wave propagation dissipation	V_{IS} = 1.6VRMS R_L = 10kΩ (Test circuit 5)	−4.5	4.5						%
	Feedthrough (switch off)	V_{IS} = 1.6VRMS R_L = 10kΩ C_L = 50pF (Test circuit 2)	−4.5	4.5						MHz
	Crosstalk (control input, enable input-to-switch output)	R_L = 10kΩ R_l = 1kΩ C_L = 50pF (Test circuit 6)	−4.5	4.5						mV_{P-P}
	Crosstalk (switch-to-switch)	R_L = 1kΩ, C_L = 50pF (Test circuit 7)	−4.5	4.5						MHz
C_I	Input capacitance — Control input						10		10	pF
	Input capacitance — Channel input/output									
	Input capacitance — Common pin									
C_r	Feedthrough capacitance									pF
C_{PD}	Power dissipation capacitance (Note 2)									pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

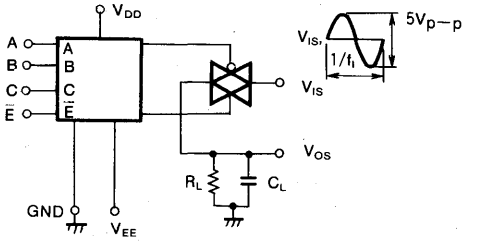
Test Circuit

1. On-state resistance

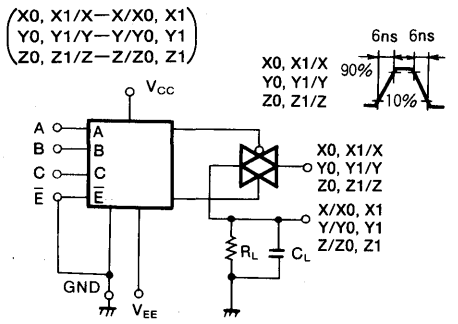


$$R_{ON} = \frac{V_{I-O}}{10^{-4}} (\Omega)$$

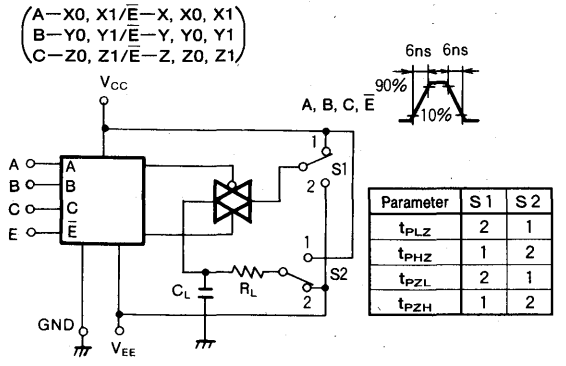
2. Maximum propagation frequency, fieldthrough (switch off)



3. Low-level to high-level and high-level to low-level propagation time

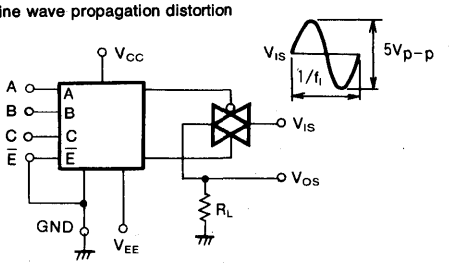


4. Low-level to high-level and high-level to low-level output propagation time, output enable, disable time

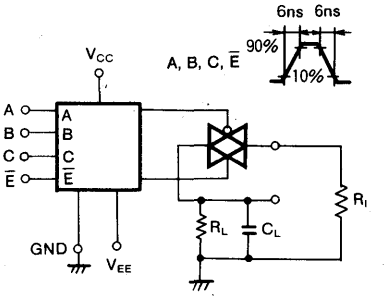


Parameter	S1	S2
t_{PLZ}	2	1
t_{PHZ}	1	2
t_{PZL}	2	1
t_{PZH}	1	2

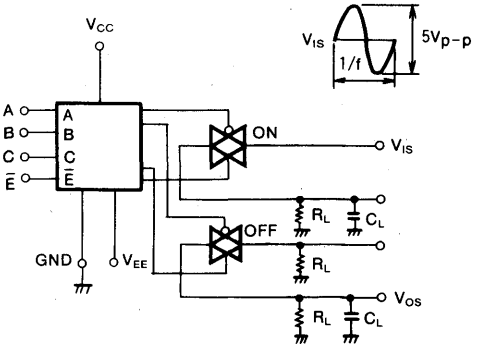
5. Sine wave propagation distortion



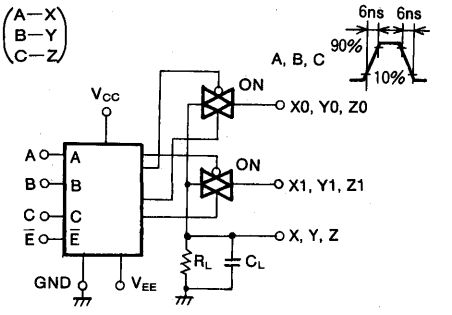
6. Crosstalk (control input, enable input)



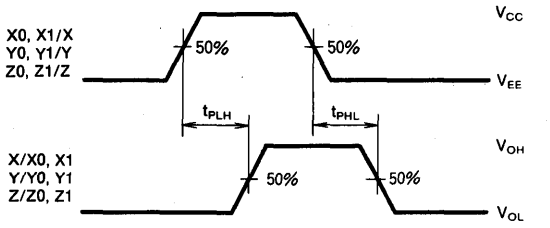
7. Crosstalk (switch-to-switch)

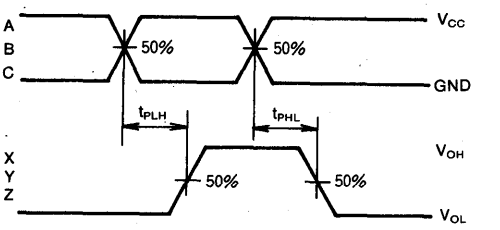


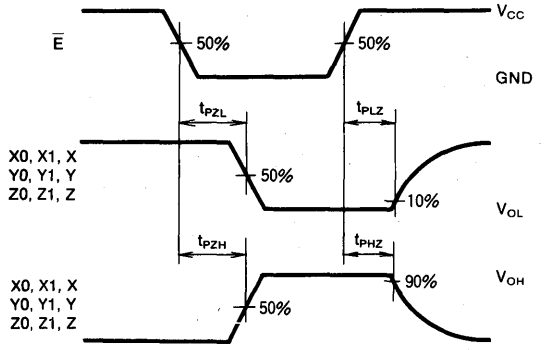
8. Low-level to high-level and high-level to low-level propagation time

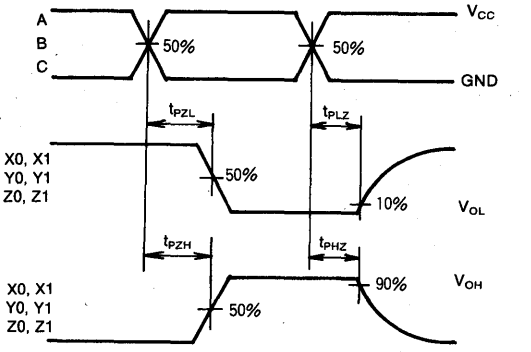


TIMING DIAGRAM









M74HC4066P/FP/DP

QUADRUPLE ANALOG SWITCH/MULTIPLEXER/DEMULTIPLEXER WITH ENHANCED ON-RESISTANCE LINEARITY

DESCRIPTION

The M74HC4066 is a semiconductor integrated circuit consisting of four independent bidirectional analog switches.

FEATURES

- Low on-state resistance 60Ω typ. (V_{CC}=6V)
- High off-state resistance: more than 10^9Ω, typ.
- Excellent conductance linearity: Variation 0.05% typ.
- High speed: 12ns typ. (C_L=50pF, V_{CC}=6V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

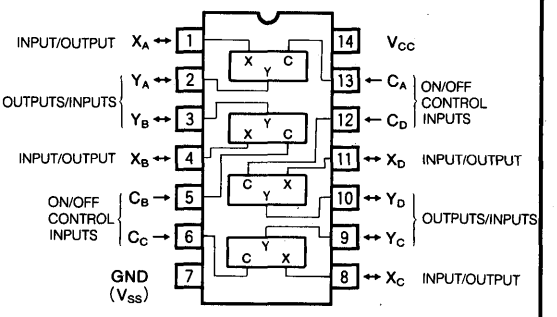
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4066 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

On/off control inputs C_A, C_B, C_C and C_D change the impedance between the switch inputs/outputs X_A-Y_A, X_B-Y_B, X_C-Y_C, and X_D-Y_D.

When control input C_A, C_B, C_C, and C_D are high, the impedance between the corresponding switch inputs/outputs will become low, and when C_A, C_B, C, and C_D are low, the impedance will become high.

PIN CONFIGURATION (TOP VIEW)

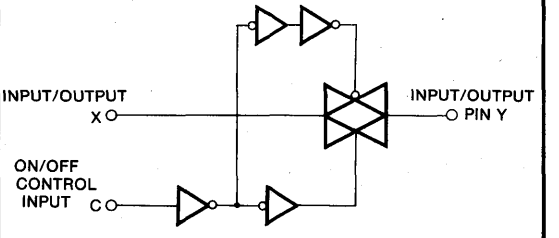


Outline 14P4, 14P2N, 14P2P

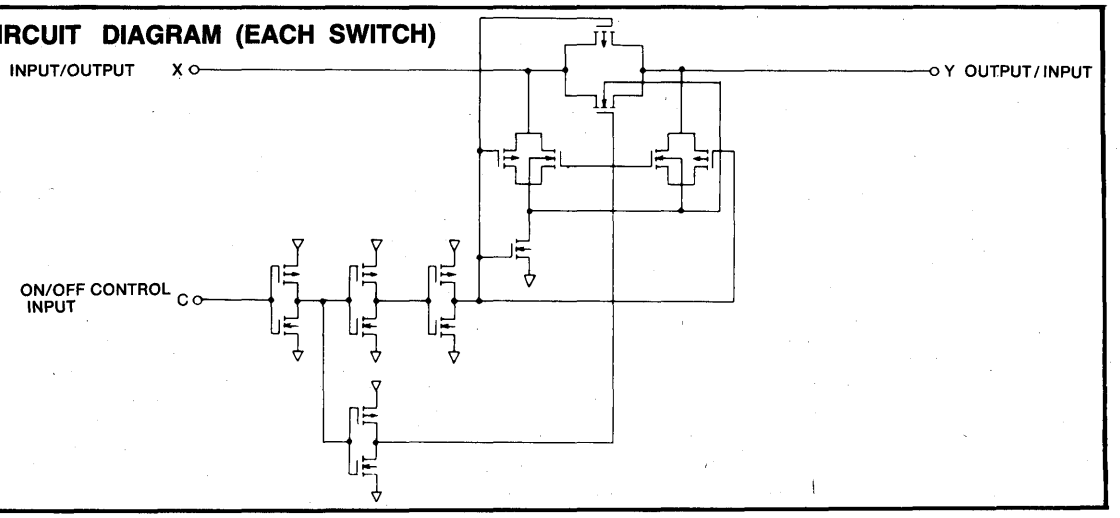
FUNCTION TABLE (Note 1)

Inputs	Input/output-to-output/input impedance
C	(V_{CC}= 4.5, 6V)
H	60~100Ω
L	>10^9Ω (typ.)

LOGIC DIAGRAM (EACH SWITCH)



CIRCUIT DIAGRAM (EACH SWITCH)



QUADRUPLE ANALOG SWITCH/MULTIPLEXER/DEMULTIPLEXER WITH ENHANCED ON-RESISTANCE LINEARITY

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
$V_{I/O}$	Input to output voltage		±0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_O	Output current per gate		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature		−65∼+150	℃

Note 2 : M74HC4066FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC4066DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage (control)	Refer to R_{ON} specification	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage (control)	$\|I_{OFF}\| \leqq 1.0\mu A$	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
R_{ON}	On-state resistance	V_{CTL} = V_{IH}	2.0		1000				Ω
		V_{IS} = 0∼V_{CC} (Test circuit 1)	4.5		100	170		215	
		I_S=100μA	6.0		70	140		180	
ΔR_{ON}	On-state resistance variation (switch-to-switch in the same pacage)	V_{CTL} = V_{IH}	2.0		50				Ω
		I_S = 100μA	4.5		3				
		Switch-to-switch	6.0		2				
$I_{IZ(OFF)}$	Switch-off leakage current	V_{CTL} = V_{IL}	6.0			±0.1		±1.0	μA
		V_{IS} = 6V, V_{OS} = 0V							
		V_{IS} = 0V, V_{OS} = 6V							
$I_{IZ(ON)}$	Switch-on leakage current	V_{CTL} = V_{IH}	6.0			±0.1		±1.0	μA
		V_{IS} = 0V∼6V							
		V_{OS} = OPEN							
I_{IH}	High-level input current (control)		6.0			0.1		1.0	μA
I_{IL}	Low-level input current (control)		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent power dissipation	V_{CTL} = V_{CC}, GND	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

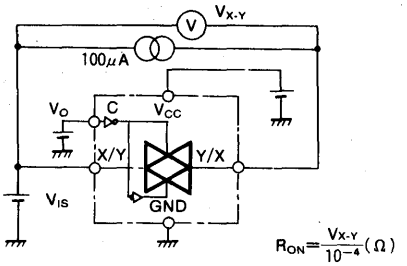
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$f_{max(I/O)}$	Maximum prapagation frequency	V_{SS} = −2.5V V_{IS} = 0.88V RMS R_L = 1kΩ (Test circuit 2) C_L = 50pF $20log_{10}V_O/V_I$ = −3dB	2.5		30				MHz
$f_{max(C)}$	Maximum control frequency	R_L = 1kΩ C_L = 15pF (Test circuit 3) V_{OS} = 1/2V_{CC}	2.0 4.5 6.0		29 30 35				MHz
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (X − Y, Y − X)	R_L=10kΩ C_L=50pF (Test circuit 4)	2.0 4.5 6.0		14 5 4	50 10 9		65 13 11	ns
t_{PHL}			2.0 4.5 6.0		11 5 4	50 10 9		65 13 11	ns
t_{PLZ}	Low-level and high-level output disable time (C − X, C − Y)	R_L = 1kΩ C_L = 50pF (Test circuit 5)	2.0 4.5 6.0		16 11 10	115 23 20		145 29 25	ns
t_{PHZ}			2.0 4.5 6.0		21 13 12	115 23 20		145 29 25	ns
t_{PZL}	Low-level and high-level output enable time (C − X, C − Y)	R_L = 1kΩ C_L = 50pF (Test circuit 5)	2.0 4.5 6.0		29 10 8	115 23 20		145 29 25	ns
t_{PZH}			2.0 4.5 6.0		27 10 8	115 23 20		145 29 25	ns
	Sine wave propagation distortion	V_{SS}=−2.5V V_{IS} = 0.88V RMS R_L = 10kΩ f_I = 1kHz (Test circuit 6)	2.5		0.02				%
	Feedthrough (switch off)	V_{SS} = −2.5V V_{IS} = 0.88V RMS R_L = 1kΩ (Test circuit 2) C_L = 50pF $20log_{10}V_{OS}/V_{IS}$ = −50dB	2.5		1.0				MHz
	Crosstalk (control input-to-switch outputs)	R_I = 1kΩ R_L = 10kΩ (Test circuit 7) C_L = 50pF	2.0 4.5 6.0		10 20 25				mV
	Crosstalk (switch-to-switch)	V_{SS} = −2.5V V_{IS} = 0.88V RMS R_L = 1kΩ (Test circuit 8) C_L = 50pF $20log_{10}V_{OS}/V_{IS}$ = −50dB	2.5		1.5				MHz
$C_{I(C)}$	Input capacitance	Control input			4	10		10	pF
$C_{I(X,Y)}$		Input/output, output/input (Test circuit 9)							pF
$C_{X-Y,Y-X}$	Feedthrough capacitance	(Test circuit 9)							pF
C_{PD}	Power dissipation capacitance (Note 2)				9				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

QUADRUPLE ANALOG SWITCH/MULTIPLEXER/DEMULTIPLEXER WITH ENHANCED ON-RESISTANCE LINEARITY

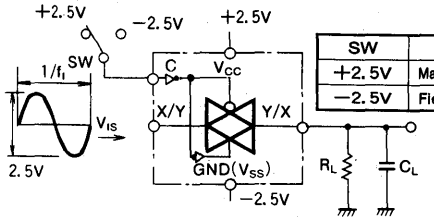
Test Circuit

1. On-state resistance



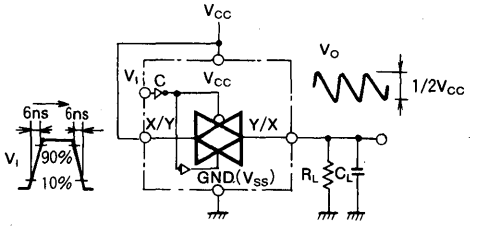
$$R_{ON}=\frac{V_{X-Y}}{10^{-4}}(\Omega)$$

2. Maximum propagation frequency, fieldthrough (switch off)

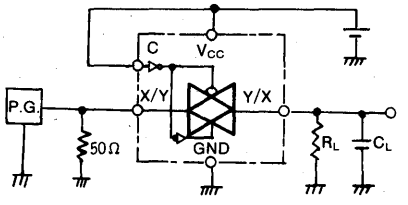


SW	Test parameter
+2.5V	Maximum propagation frequency
−2.5V	Fieldthrough

3. Maximum control frequency

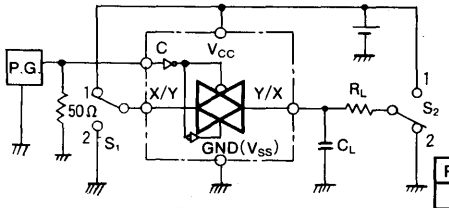


4. Low-level to high-level and high-level to low-level output propagation time (X−Y, Y−X)



(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=6ns, t_f=6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

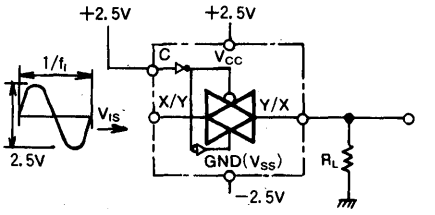
5. Output enable, disable time (C−X, C−Y)



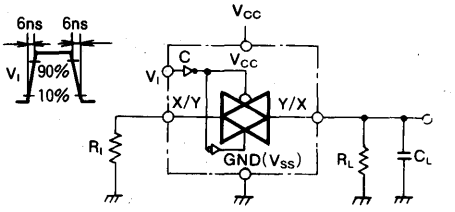
(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=6ns, t_f=6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

Parameter	S1	S2
t_{PLZ}	2	1
t_{PHZ}	1	2
t_{PZL}	2	1
t_{PZH}	1	2

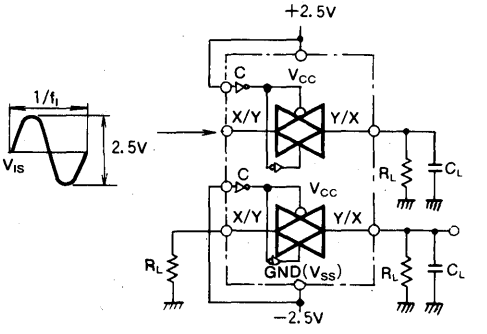
6. Sine wave propagation distortion



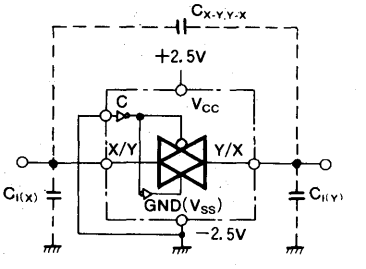
7. Crosstalk (control input-to-switch-input)



8. Crosstalk (switch-to-switch)



9. Input capacitance, fieldthrough capacitance



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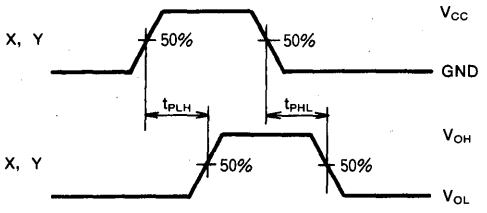
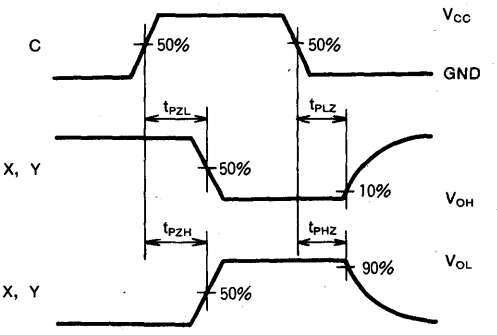
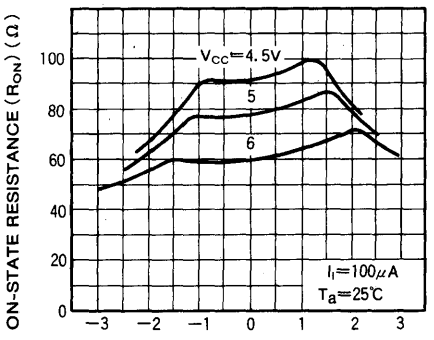
TIMING DIAGRAM

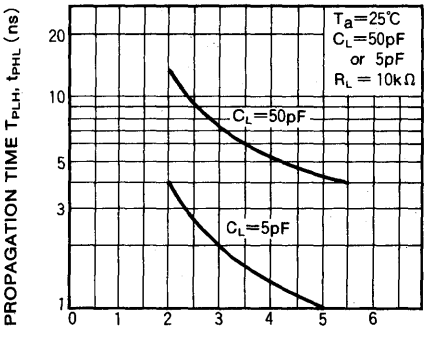




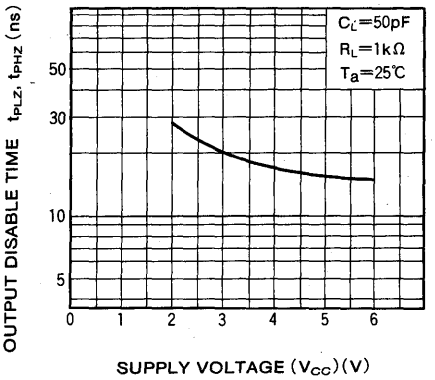
ON-STATE RESISTANCE
— INPUT VOLTAGE (TYP.)



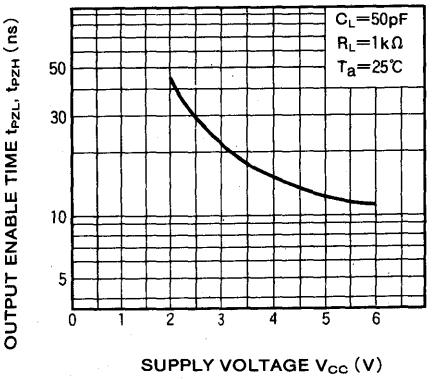
PROPAGATION TIME
— SUPPLY VOLTAGE (TYP.)



OUTPUT DISABLE TIME
— SUPPLY VOLTAGE (TYP.)



OUTPUT ENABLE TIME
— SUPPLY VOLTAGE (TYP.)



M74HC4075P/FP/DP

TRIPLE 3-INPUT OR GATE

DESCRIPTION

The M74HC4075 is a semiconductor integrated circuit consisting of three 3-input positive-logic OR gates, usable as negative-logic AND gates.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4075 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

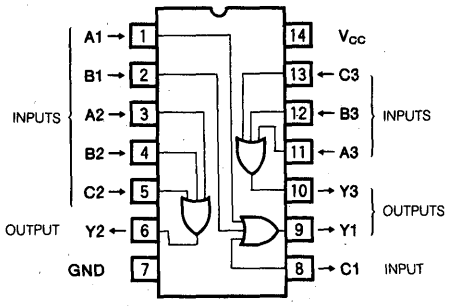
When all inputs A, B and C are low, the output Y will become low, and when at least one of the inputs is high, the output Y will become high.

FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	L
H	L	H
L	H	H
H	H	H

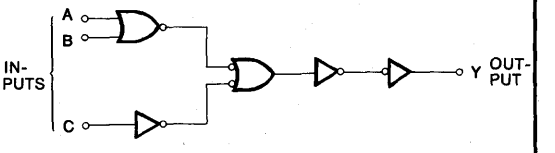
N = B + C

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

LOGIC DIAGRAM (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC4075FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC4075DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

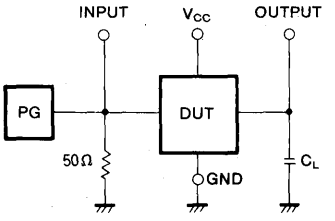
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				20	ns
t_{PHL}					20	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				31				pF

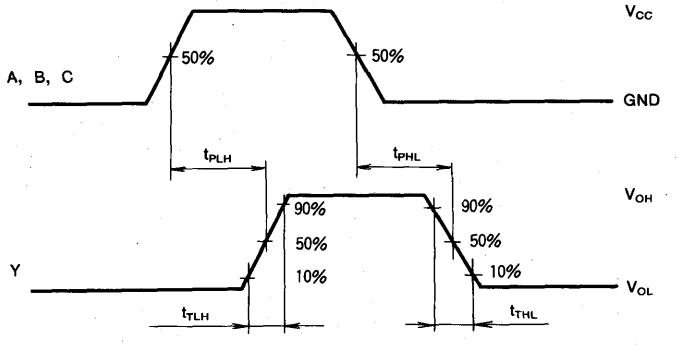
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC4078P/FP/DP

8-INPUT POSITIVE NOR/OR GATE

DESCRIPTION

The M74HC4078 is a semiconductor integrated circuit consisting of an 8-input positive-logic NOR/OR gates, usable as a negative-logic NAND/AND gate.

FEATURES

- High-speed: 16ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4078 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

Buffered outputs Y and X improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

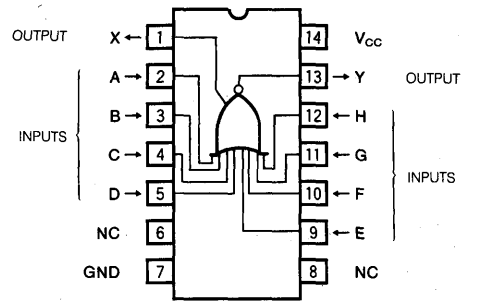
When all inputs A through H are low, output Y will become high and output X will become low. When at least one of the inputs is high, output Y will become low and output X will become high.

FUNCTION TABLE

Inputs		Outputs	
A	N	Y	X
L	L	H	L
H	L	L	H
L	H	L	H
H	H	L	H

N = B + C + D + E + F + G + H

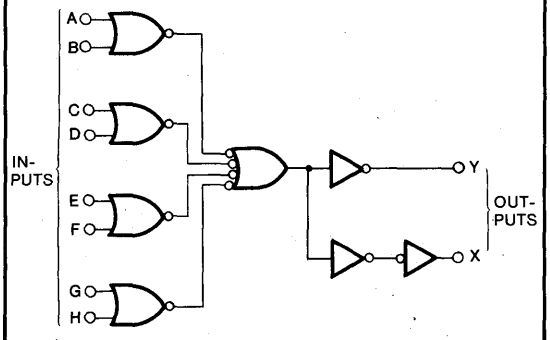
PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

NC : NO CONNECTION

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC4078FP, T_a = −40~+60℃ and T_a = 60~85℃ are derated at −6mW/℃.
M74HC4078DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

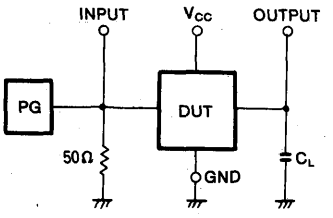
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Tye	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 3)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				22	ns
t_{PHL}	output propagation time (A~H − Y)				22	ns
t_{PLH}	Low-level to high-level and high-level to low-level				24	ns
t_{PHL}	output propagation time (A~H − X)				24	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A~H − Y)		2.0			130		165	ns
			4.5			26		33	
			6.0			22		28	
t_{PHL}			2.0			130		165	ns
			4.5			26		33	
			6.0			22		28	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A~H − X)		2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
t_{PHL}			2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				75				pF

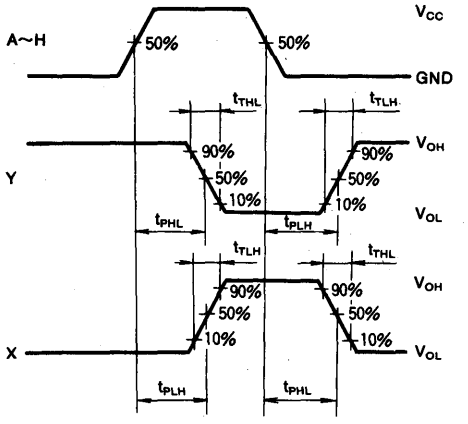
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load condition is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC4511P/FP/DP

BCD-TO SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER

DESCRIPTION

The M74HC4511 is a semiconductor integrated circuit consisting of a BCD seven-segment decoder/driver.

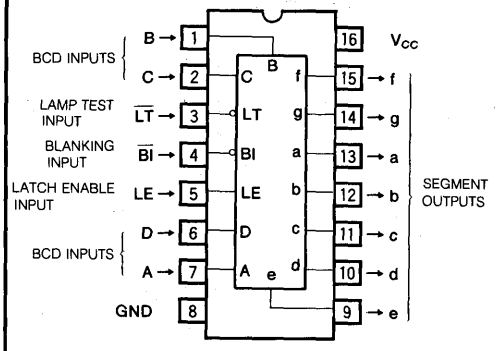
FEATURES

- Contained latch for BCD input
- Blanking input
- High-speed: 55ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

FUNCTIONAL DESCRIPTION

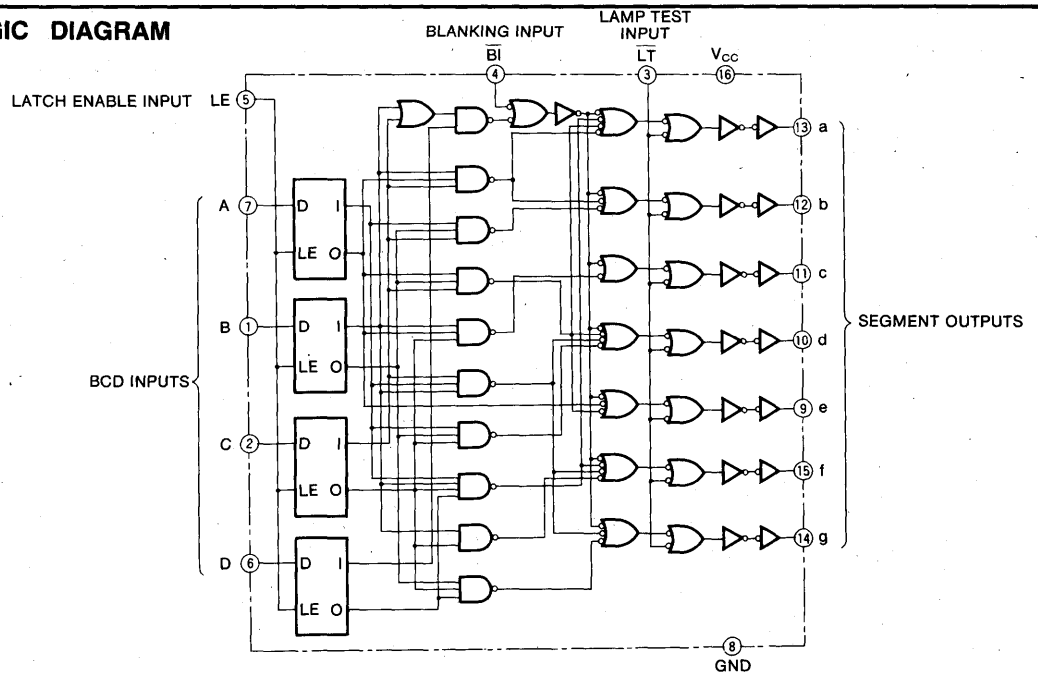
Use of silicon gate technology allows the M74HC4511 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

When BCD code is applied to BCD (binary coded decimal) inputs A through D, the corresponding segment outputs a through g will become high. When each output is connected to a seven-segment display device, numeric characters are displayed as shown in the displayed character table.

When latch enable input LE changes from low-level to high-level, the signals existing immediately prior to the change at A through D will be stored in the latch. When the blanking input $\overline{BI}$ is low, a through g will become low, and display will be put out, irrespective of A through D.

When lamp test input $\overline{LT}$ is low, a through g will become high irrespective of other inputs, and all display segments will be lighted for visual inspection.

LOGIC DIAGRAM



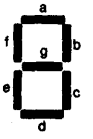
BCD-TO SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER

FUNCTION TABLE (Note 1)

	Inputs							Outputs						
Decimal value or function	LE	$\overline{LT}$	$\overline{BI}$	D	C	B	A	a	b	c	d	e	f	g
0	L	H	H	L	L	L	L	H	H	H	H	H	H	L
1	L	H	H	L	L	L	H	L	H	H	L	L	L	L
2	L	H	H	L	L	H	L	H	H	L	H	H	L	H
3	L	H	H	L	L	H	H	H	H	H	H	L	L	H
4	L	H	H	L	H	L	L	L	H	H	L	L	H	H
5	L	H	H	L	H	L	H	H	L	H	H	L	H	H
6	L	H	H	L	H	H	L	L	L	H	H	H	H	H
7	L	H	H	L	H	H	H	H	H	H	L	L	L	L
8	L	H	H	H	L	L	L	H	H	H	H	H	H	H
9	L	H	H	H	L	L	H	H	H	H	L	L	H	H
10	L	H	H	H	L	H	L	L	L	L	L	L	L	L
11	L	H	H	H	L	H	H	L	L	L	L	L	L	L
12	L	H	H	H	H	L	L	L	L	L	L	L	L	L
13	L	H	H	H	H	L	H	L	L	L	L	L	L	L
14	L	H	H	H	H	H	L	L	L	L	L	L	L	L
15	L	H	H	H	H	H	H	L	L	L	L	L	L	L
Latch	↑	H	H	X	X	X	X	a^0	b^0	c^0	d^0	e^0	f^0	g^0
Blanking	X	H	L	X	X	X	X	L	L	L	L	L	L	L
Lamp test	X	L	X	X	X	X	X	H	H	H	H	H	H	H

Note 1 : X : Irrelevant
↑ : Change from low to high
a^0~g^0 : Output state of a~g when latch enable pulse is applied.

Definition of character segments



DISPLAYED CHARACTERS

Decimal number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Displayed character	0	1	2	3	4	5	6	7	8	9						

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin	When output is high	−35	mA
		When output is low	25	
I_{CC}	Supply/GND current	V_{CC}	150	mA
		GND	−50	
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC4511FP, T_a = −40~+70℃ and T_a = 70~85℃ are derated at −6mW/℃.
M74HC4511DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

BCD-TO SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				100	ns
t_{PHL}	output propagation time (A∼D − a∼g)				100	ns
t_{PLH}	Low-level to high-level and high-level to low-level				100	ns
t_{PHL}	output propagation time (LE − a∼g)				100	ns
t_{PLH}	Low-level to high-level and high-level to low-level				100	ns
t_{PHL}	output propagation time ($\overline{BI}$ − a∼g)				100	ns
t_{PLH}	Low-level to high-level and high-level to low-level				100	ns
t_{PHL}	output propagation time ($\overline{LT}$ − a∼g)				100	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

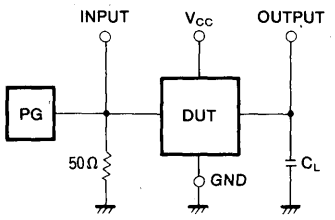
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A~D − a~g)		2.0			600		756	ns
			4.5			120		151	
			6.0			102		129	
t_{PHL}			2.0			600		756	ns
			4.5			120		151	
			6.0			102		129	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − a~g)		2.0			600		756	ns
			4.5			120		151	
			6.0			102		129	
t_{PHL}			2.0			600		756	ns
			4.5			120		151	
			6.0			102		129	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{BI}$ − a~g)		2.0			600		756	ns
			4.5			120		151	
			6.0			102		129	
t_{PHL}			2.0			600		756	ns
			4.5			120		151	
			6.0			102		129	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LT}$ − a~g)		2.0			600		756	ns
			4.5			120		151	
			6.0			102		129	
t_{PHL}			2.0			600		756	ns
			4.5			120		151	
			6.0			102		129	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

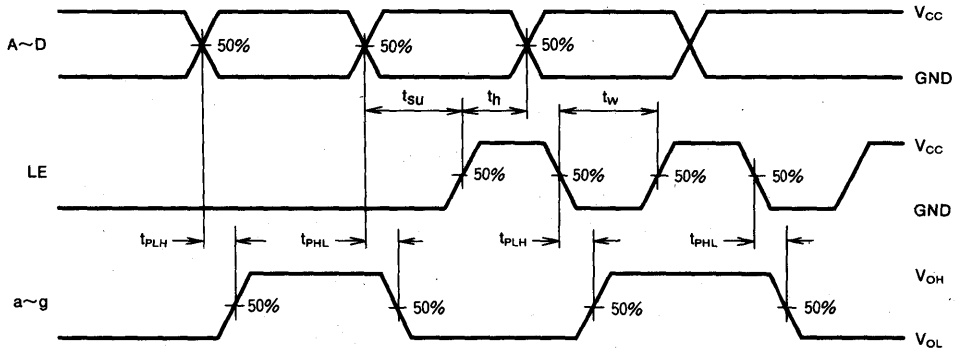
Symbol	Parameter	Test conditions	Limits						Unit
			25℃			−40~+85℃			
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W	LE pulse width	2.0	80			101		ns
		4.5	16			20		
		6.0	14			17		
t_{SU}	A~D setup time with respect to LE	2.0	100			126		ns
		4.5	20			25		
		6.0	17			21		
t_h	A~D hold time with respect to LE	2.0	0			0		ns
		4.5	0			0		
		6.0	0			0		

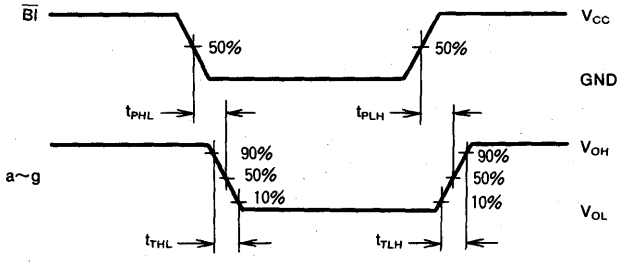
Note 4 : Test Circuit

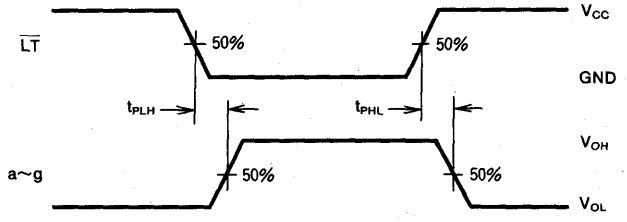


(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC4514P/FP/DWP

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("H" LEVEL OUTPUT)

DESCRIPTION

The M74HC4514 is a semiconductor integrated circuit consisting of a 4-bit binary to 16-line decoder/demultiplexer with address latch.

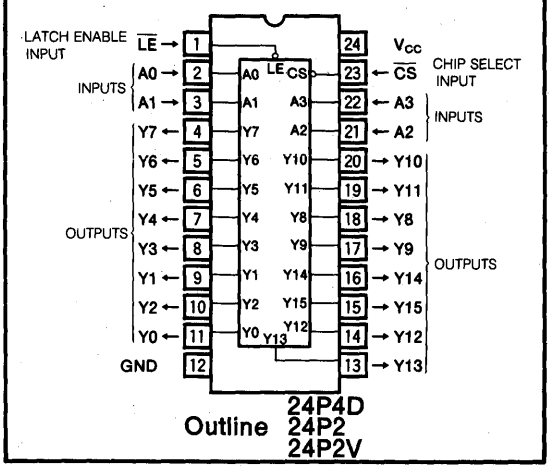
FEATURES

- High-speed: 24ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D 24P2 24P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4514 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

The M74HC4514 consists of a 4-bit binary to 16-line decoder/demultiplexer with an address latch to store the signals of inputs A0 through A3. When latch-enable input $\overline{LE}$ is high, a 4-bit binary code, applied to inputs A0 through A3, goes through the latch and will become a decoder input signal, the corresponding output Y0 through Y15 will become high, and all the other outputs will become low. When $\overline{LE}$ is low, the signals existing immdiately prior to the change at A0 through A3 will be stored in the latch, and the latch contents do not change even if A0 through A3 are changed. In this case, chip select input $\overline{CS}$ is maintained low. When $\overline{CS}$ is high, Y0 through Y15 all will become low. When operated as a 1-of-16 demultiplexer, $\overline{CS}$ is used as the data input and A0 through A3 are used as the select inputs.

FUNCTION TABLE (Note 1)

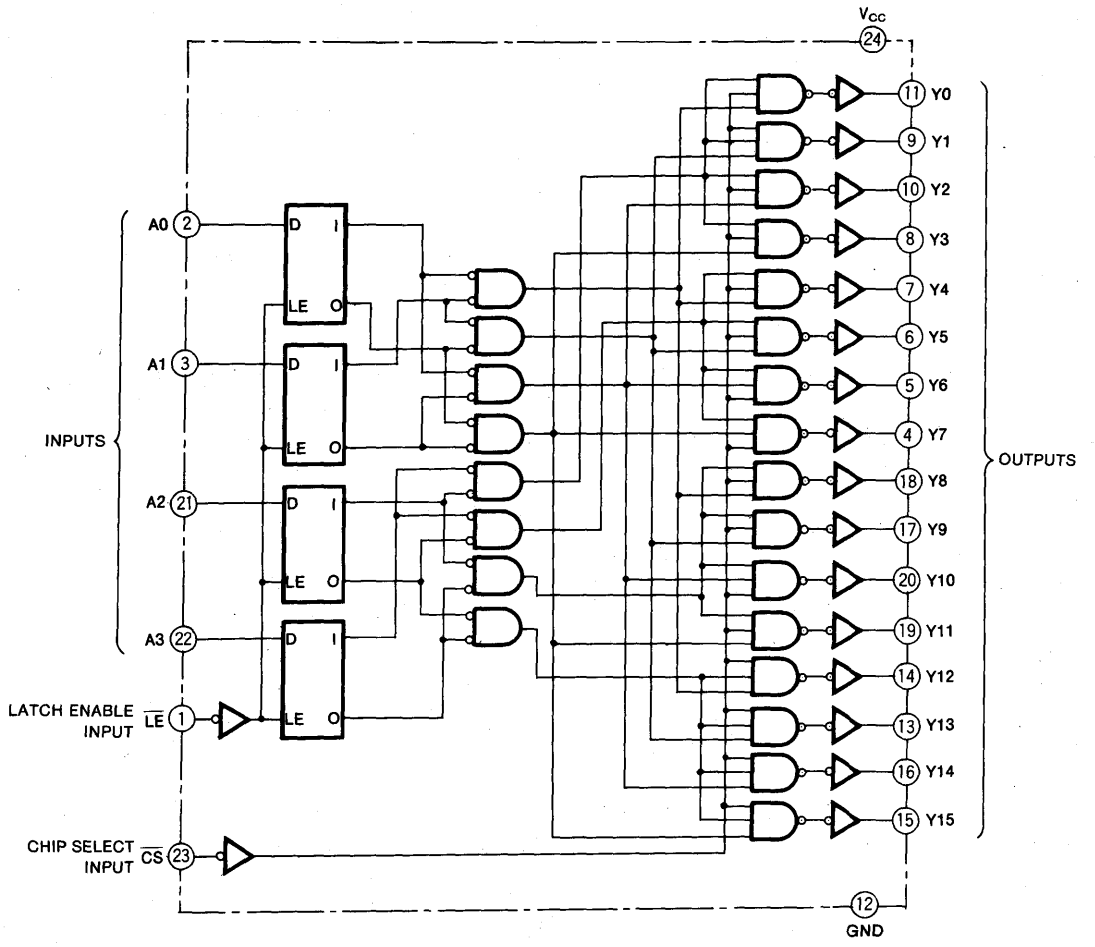
Inputs						Outputs															
$\overline{LE}$	$\overline{CS}$	A3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15
H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
H	L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
H	L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
H	L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
H	L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
X	H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	X	X	X	X	$Y0^0$	$Y1^0$	$Y2^0$	$Y3^0$	$Y4^0$	$Y5^0$	$Y6^0$	$Y7^0$	$Y8^0$	$Y9^0$	$Y10^0$	$Y11^0$	$Y12^0$	$Y13^0$	$Y14^0$	$Y15^0$

Note 1 : X : Irrelevant
Y^0 : Output state Y before $\overline{LE}$ change to low-level

MITSUBISHI ELECTRIC

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("H" LEVEL OUTPUT)

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC4514FP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.
M74HC4514DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("H" LEVEL OUTPUT)

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
				25℃			−40∼+85℃			
				V_{CC}(V)	Min	Typ	Max	Min	Typ	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	high-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time ($\overline{CS}$ − Y)				30	ns
t_{PLH}	Low-level to high-level and high-level to low-level				40	ns
t_{PHL}	output propagation time (A − Y)				30	ns
t_{PLH}	Low-level to high-level and high-level to low-level				40	ns
t_{PHL}	output propagation time ($\overline{LE}$ − Y)				30	ns

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("H" LEVEL OUTPUT)

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

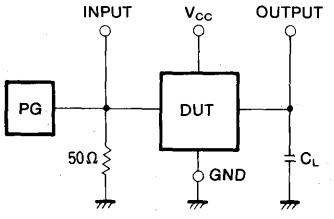
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS}$ − Y)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Y)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W	$\overline{LE}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	A setup time with respect to $\overline{LE}$		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	A hold time with respect to $\overline{LE}$		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

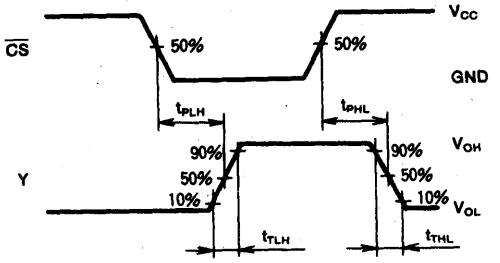
Note 4 : Test Circuit

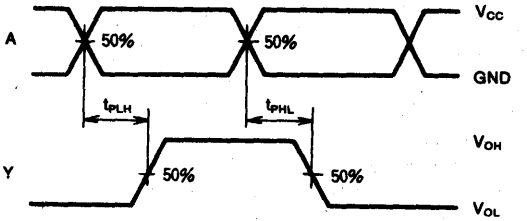


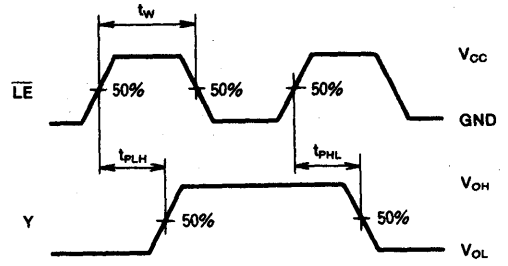
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

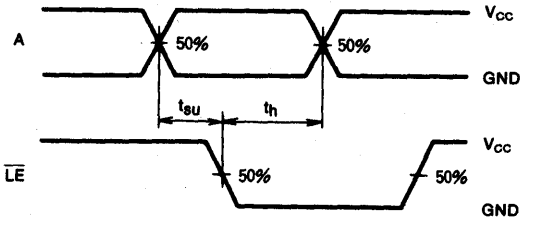
1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("H" LEVEL OUTPUT)

TIMING DIAGRAM









PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC4515P/FP/DWP

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("L" LEVEL OUTPUT)

DESCRIPTION

The M74HC4515 is a semiconductor integrated circuit consisting of a 4-bit binary to 16-line decoder/demultiplexer with address latch.

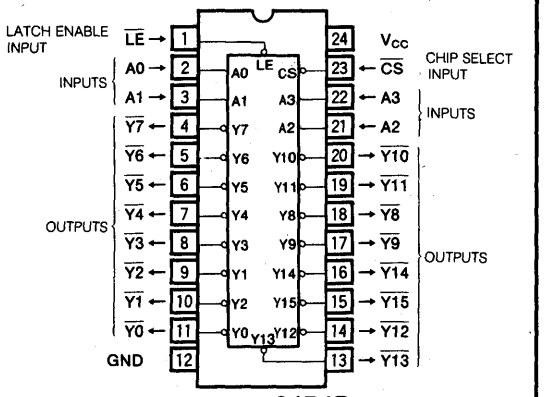
FEATURES

- High-speed: 24ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D 24P2 24P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4515 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

The M74HC4515 consists of a 4-bit binary to 16-line decoder/demultiplexer with an address latch to store the signals of inputs A0 through A3. When latch enable input $\overline{LE}$ is high, a 4-bit binary code, applied to inputs A0 through A3, goes through the latch and will become a decoder input signal, the corresponding output $\overline{Y0}$ through $\overline{Y15}$ will become low and all the other outputs will become high. When $\overline{LE}$ is high, the signals existing immediately prior to the change at A0 through A3 will be stored in the latch, and the latch contents do not change even if A0 through A3 are changed. In this case, chip select input $\overline{CS}$ is maintained low.

When $\overline{CS}$ is high, $\overline{Y0}$ through $\overline{Y15}$ all will become high. When operated as a 1-of-16 demultiplexer, $\overline{CS}$ is used as the data input and A0 through A3 are used as the select inputs.

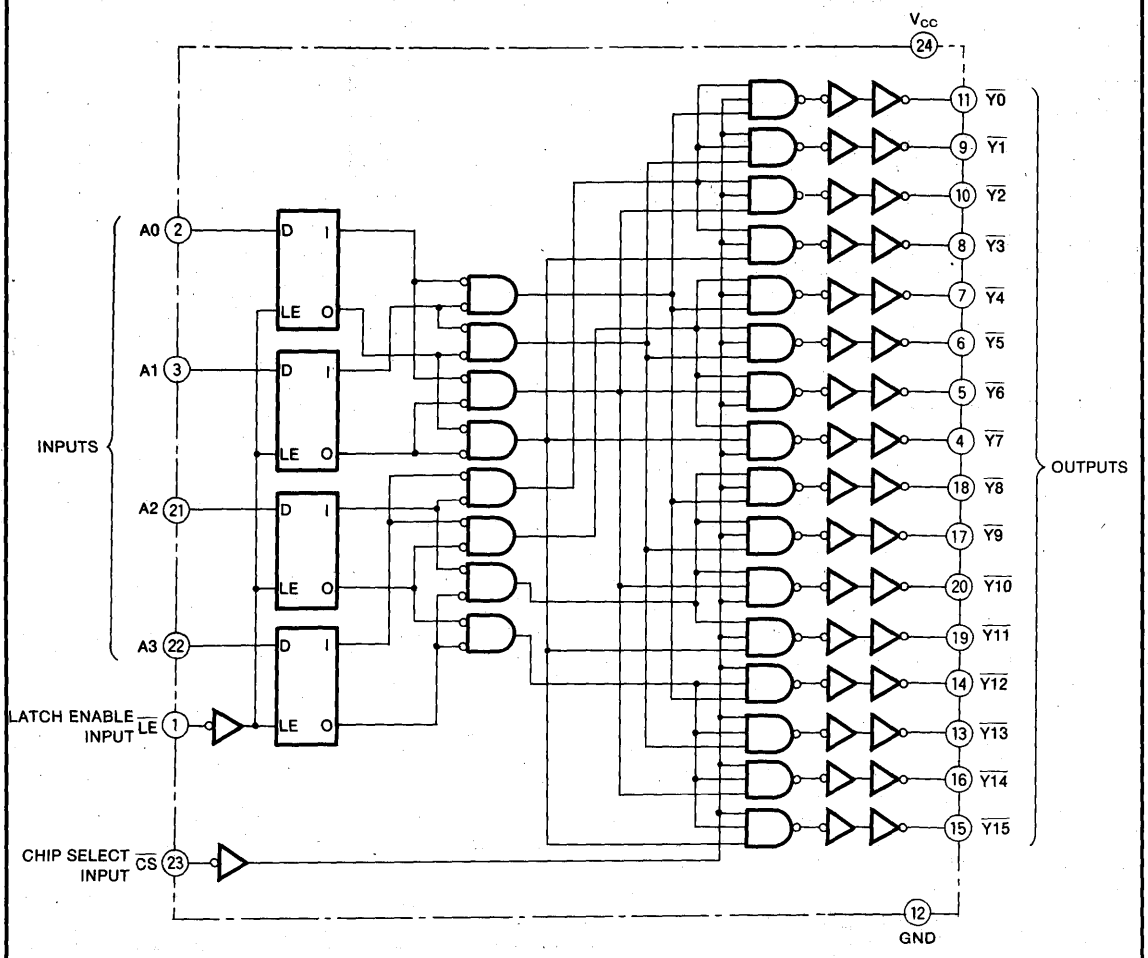
FUNCTION TABLE (Note 1)

Inputs						Outputs															
$\overline{LE}$	$\overline{CS}$	A3	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$	$\overline{Y10}$	$\overline{Y11}$	$\overline{Y12}$	$\overline{Y13}$	$\overline{Y14}$	$\overline{Y15}$
H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
H	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
H	L	H	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
H	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
H	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
H	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	X	X	X	X	$\overline{Y0}^0$	$\overline{Y1}^0$	$\overline{Y2}^0$	$\overline{Y3}^0$	$\overline{Y4}^0$	$\overline{Y5}^0$	$\overline{Y6}^0$	$\overline{Y7}^0$	$\overline{Y8}^0$	$\overline{Y9}^0$	$\overline{Y10}^0$	$\overline{Y11}^0$	$\overline{Y12}^0$	$\overline{Y13}^0$	$\overline{Y14}^0$	$\overline{Y15}^0$

Note 1 : X : Irrelevant
$\overline{Y}^0$: Output state Y before $\overline{LE}$ changed to low-level

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("L" LEVEL OUTPUT)

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC4515FP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.
M74HC4515DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("L" LEVEL OUTPUT)

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS}$ − $\overline{Y}$)				30	ns
t_{PHL}					30	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)				40	ns
t_{PHL}					30	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − $\overline{Y}$)				40	ns
t_{PHL}					30	ns

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("L" LEVEL OUTPUT)

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

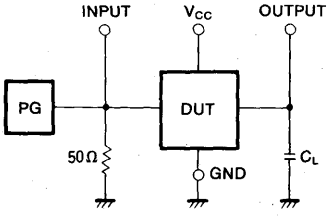
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS}$ − $\overline{Y}$)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − $\overline{Y}$)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
C_I	Input capacitance					10		10	pF
C_{PD}	Powerdissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{LE}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	A setup time with respect to $\overline{LE}$		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	A hold time with respect to $\overline{LE}$		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

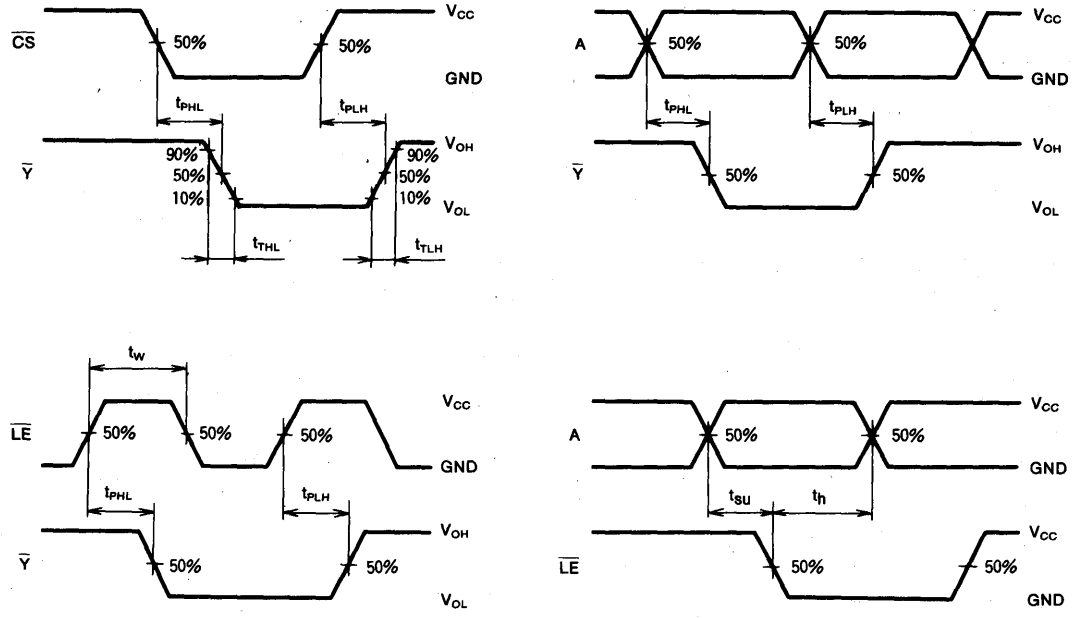
Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("L" LEVEL OUTPUT)

TIMING DIAGRAM



PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC4538P/FP/DP

DUAL PRECISION MONOSTABLE MULTIVIBRATOR (RETRIGGERABLE RESETTABLE)

DESCRIPTION

The M74HC4538 is a semiconductor integrated circuit, consisting of two retriggerable monostable multivibrators with direct reset inputs.

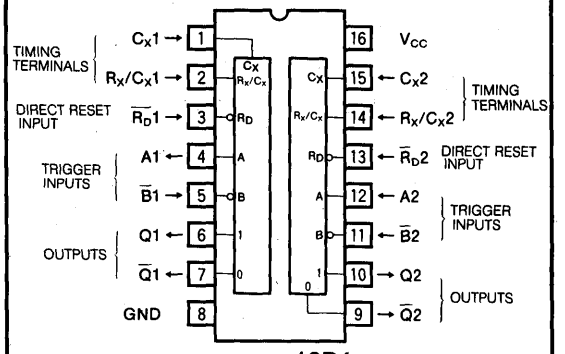
FEATURES

- Retriggerable multivibrator can generate wide output pulses.
- Direct reset input can interrupt output pulses.
- High speed: 30ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4 16P2N 16P2P

FUNCTIONAL DESCRIPTION

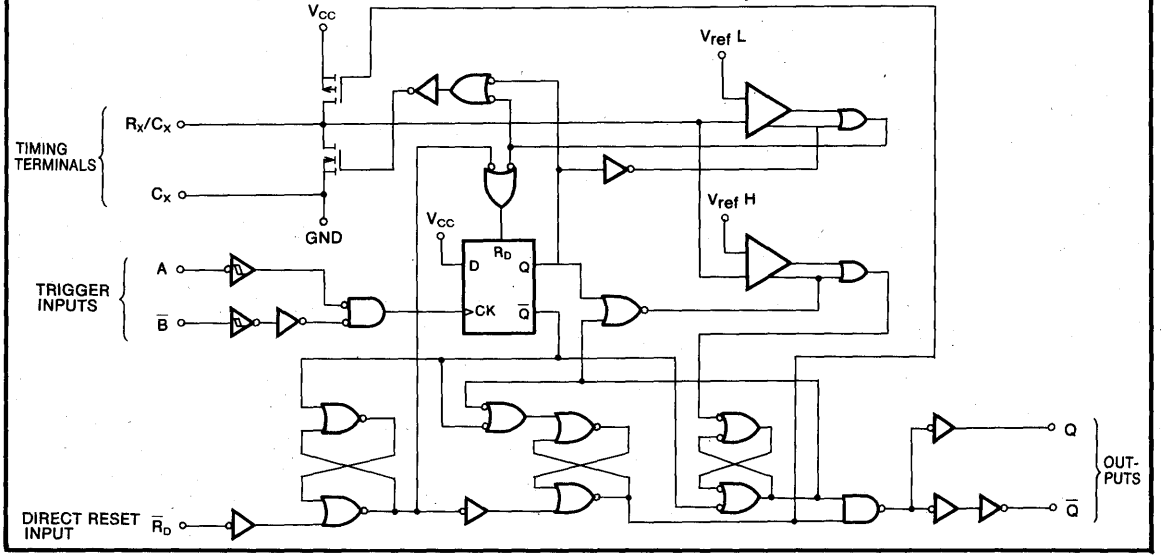
Use of silicon gate technology allows the M74HC4538 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

Trigger input with built-in Schmitt trigger circuit prevents the occurrence of incorrect oscillations even when input signals having slow rise and fall times are applied.

When external resistor R_X and electrostatic capacitor C_X are connected to timing terminals R_X/C_X and C_X as shown in Fig. 1, and trigger pulses are applied at input A or $\overline{B}$, positive pulses will appear at Q and negative pulses, at $\overline{Q}$. (Fig.2-(a)) The pulse width t_{WQ} is set by R_X and C_X. The trigger is applied when A changes from low-level to high-level or when $\overline{B}$ changes from high-level to low-level. The retrigger function is used to obtain longer pulse width and output pulses can be extended by retriggering at A or $\overline{B}$ before the output pulse is completed. (Fig.2-(b)).

When direct reset input $\overline{R_D}$ is low, Q will be reset low and $\overline{Q}$ will be reset high, irrespective of the output state, allowing output pulses to be narrower by R_D. (Fig.2-(c)).

LOGIC DIAGRAM (EACH MONOSTABLE MULTIVIBRATOR)



MITSUBISHI ELECTRIC

DUAL PRECISION MONOSTABLE MULTIVIBRATOR (RETRIGGERABLE RESETTABLE)

FUNCTION TABLE (Note 1)

Inputs			Outputs	
A	B	$\overline{R_D}$	Q	$\overline{Q}$
↑	H	H	⎍	⎎
X	L	H	L	H
H	X	H	L	H
L	↓	H	⎍	⎎
X	X	L	L	H

Note 1 : X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level
⎍ : Positive one-shot operation
⎎ : Negative one-shot operation

OPERATION

1. How to use the timing terminals

Resistor R_X and capacitor C_X are connected to timing terminals R_X/C_X and C_X, as shown in Fig. 1. If C_X is polar, the positive lead should be connected to the R_X/C_X side, and the negative lead to the C_X side. A diode is connected to prevent latchup.

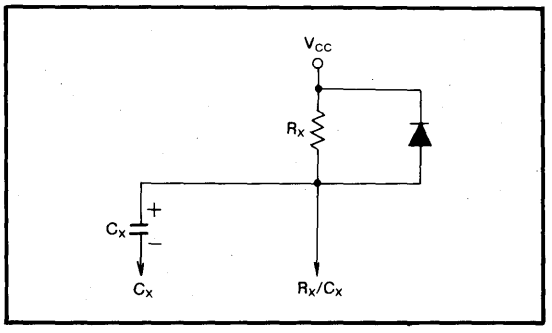


Fig.1 Connection of external resistor R_X and capacitor C_X to timing terminals C_X and R_X/C_X

2. Output pulse width t_{WQ}

The output pulse width t_{WQ} is determined as follows:
When $C_X > 100000pF$, $R_X \geqq 10k\Omega$
$t_{WQ} = 0.72\ C_X \cdot R_X$ (ns)
C_X is givin in pF, and R_X in $k\Omega$.

3. Output pulse width control

The output pulse width can be controlled in the following three ways.

3—1 Normal use
Fig.2-(a) is the directions as ordinary monostable multivibrator operation and the output pulse width t_{WQ} can be set by using the formula and figure shown in section 2 above.

3 — 2 Extention of the output pulse width with retrigger function
As shown in Fig.2-(b), the output pulse width can be extended at will by applying additional trigger pulses before the output pulse is completed.

3—3 Shortening of the output pulse width with $\overline{R_D}$ signal
As shown in Fig.2-(c), the output pulse which has been generated by the trigger signal can be terminated with the $\overline{R_D}$ signal and it is possible to shorten its width as required.

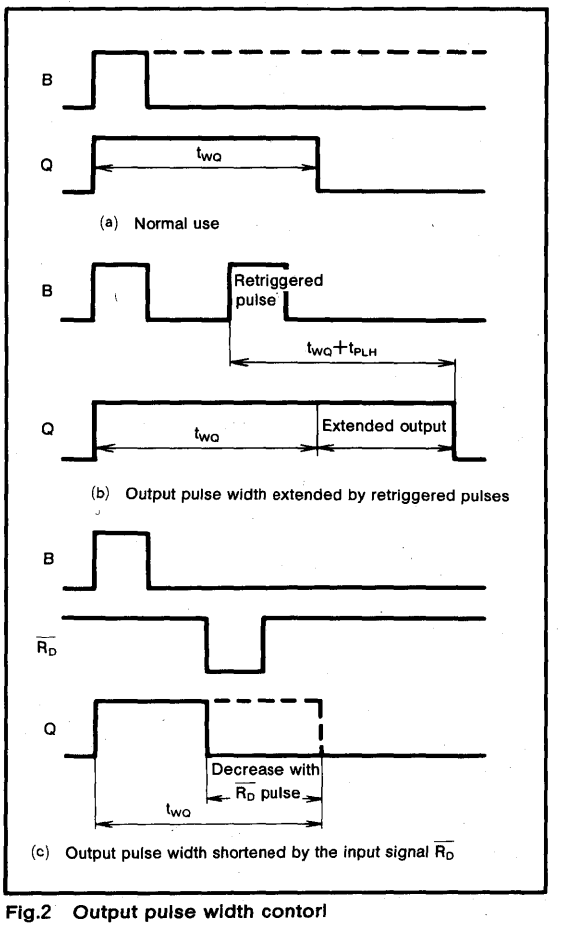


Fig.2 Output pulse width contorl

4. Precautions for use

4—1 Additional trigger pulses must be applied at least t_{rr} later after the previous trigger pulse has been applied. The retrigger pulse during this period is ineffective.

4—2 The lead lengths of external resistor R_X and capacitor C_X should be as short as possible (less than 3cm) to minimize stray wiring capacitance and to prevent misoperation due to noise. Care should also be taken to isolate this circuit from noise sources as far as possible.

4—3 Insert a capacitor of $0.01 \sim 0.1 \mu F$ with good high-frequency characteristics between V_{CC} and GND.

4—4 Output pulses may be generated when power is switched on.

4—5 Capacitor discharge when the power is turned off may cause thermal breakdown or latchup, so a diode should be connected as shown in Fig. 1.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC4543P/FP/DP

BCD-TO SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER FOR LIQUID-CRYSTAL DISPLAYS

DESCRIPTION

The M74HC4543 is a semiconductor integrated circuit consisting of a seven-segment BCD decoder/driver, enable to drive liquid-crystal displays.

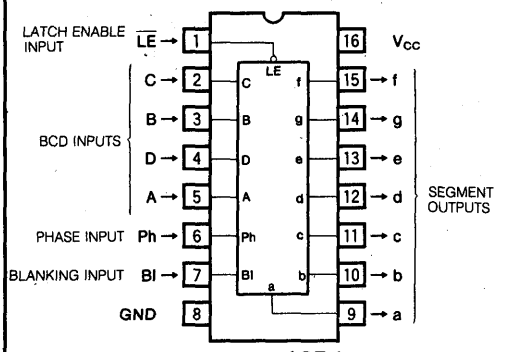
FEATURES

- Contained latch for BCD input
- Blanking input
- High-speed: 45ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4 16P2N 16P2P

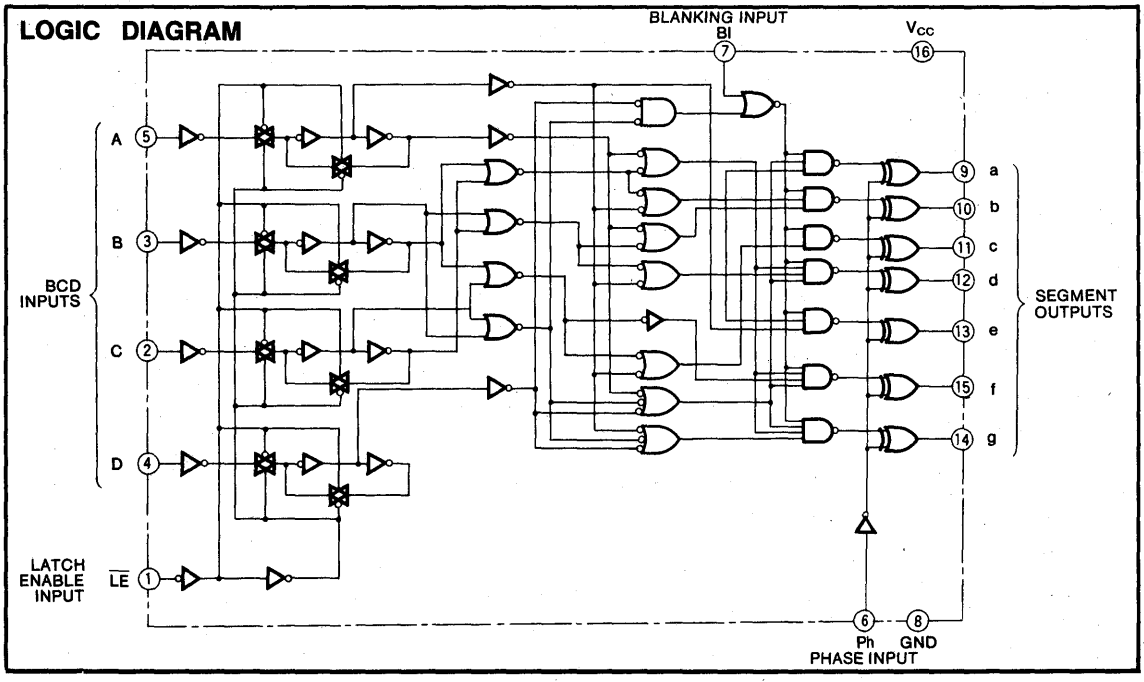
FUNCTIONAL DESCRIPTION

When BCD code is applied to BCD (binary coded decimal) inputs A through D, the corresponding segment outputs a through g will become high. When each output is connected to a seven-segment display device, numeric characters are displayed as shown in the displayed character table.

When latch enable input $\overline{LE}$ changes from high-level to low-level, the signals existing immediately prior to the change at A through D will be stored in the latch. When blanking input B1 is high, a~g will become low irrespective of A through D, and display will be put out.

When phase input Ph is high, outputs a through g will be changed. To drive a liquid-crystal display device, the common square wave signal must be applied to Ph and the common backplane of display device. (See Application Example.) To drive other display devices, Ph must be set to low or high, and additional components must be connected to the segment outputs to increase the drive current.

LOGIC DIAGRAM



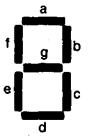
BCD-TO SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER FOR LIQUID-CRYSTAL DISPLAYS

FUNCTION TABLE (Note 1)

	Inputs							Outputs						
Decimal value or function	$\overline{LE}$	Ph	BI	D	C	B	A	a	b	c	d	e	f	g
0	H	L	L	L	L	L	L	H	H	H	H	H	H	L
1	H	L	L	L	L	L	H	L	H	H	L	L	L	L
2	H	L	L	L	L	H	L	H	H	L	H	H	L	H
3	H	L	L	L	L	H	H	H	H	H	H	L	L	H
4	H	L	L	L	H	L	L	L	H	H	L	L	H	H
5	H	L	L	L	H	L	H	H	L	H	H	L	H	H
6	H	L	L	L	H	H	L	H	L	H	H	H	H	H
7	H	L	L	L	H	H	H	H	H	H	L	L	L	L
8	H	L	L	H	L	L	L	H	H	H	H	H	H	H
9	H	L	L	H	L	L	H	H	H	H	H	L	H	H
10	H	L	L	H	L	H	L	L	L	L	L	L	L	L
11	H	L	L	H	L	H	H	L	L	L	L	L	L	L
12	H	L	L	H	H	L	L	L	L	L	L	L	L	L
13	H	L	L	H	H	L	H	L	L	L	L	L	L	L
14	H	L	L	H	H	H	L	L	L	L	L	L	L	L
15	H	L	L	H	H	H	H	L	L	L	L	L	L	L
Latch	L	L	L	X	X	X	X	a^0	b^0	c^0	d^0	e^0	f^0	g^0
Blanking	X	L	H	X	X	X	X	L	L	L	L	L	L	L
DITTO	†	H	†	†				The output levels shown above are inverted.						

Note 1 : X : Irrelevant
a^0~g^0 : Output state of a~g when latch enable pulse is applied.
† : Same combination as above

Definitions of character segments



DISPLAYED CHARACTERS

Decimal value	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Displayed character	0	1	2	3	4	5	6	7	8	9						

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC4543FP, T_a = −40~+70℃ and T_a = 70~85℃ are derated at −6mW/℃.
M74HC4543DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

BCD-TO SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER FOR LIQUID-CRYSTAL DISPLAYS

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Typ	Max	−40~+85℃ Min	Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −0.4mA	4.5	3.98			3.84		
			I_{OH} = −0.52mA	6.0	5.48			5.34		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 0.4mA	4.5			0.26		0.33	
			I_{OL} = 0.52mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				66	ns
t_{PHL}	output propagation time (A~D − a~g)				66	ns
t_{PLH}	Low-level to high-level and high-level to low-level				66	ns
t_{PHL}	output propagation time ($\overline{LE}$ − a~g)				66	ns
t_{PLH}	Low-level to high-level and high-level to low-level				41	ns
t_{PHL}	output propagation time (BI − a~g)				41	ns
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (Ph − a~g)				30	ns

BCD-TO SEVEN-SEGMENT
LATCH/DECODER/DISPLAY DRIVER FOR LIQUID-CRYSTAL DISPLAYS

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

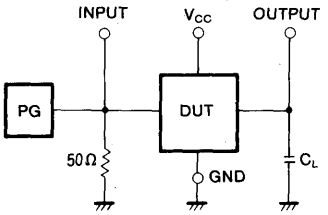
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A~D − a~g)		2.0			385		480	ns
			4.5			77		96	
			6.0			66		82	
t_{PHL}			2.0			385		480	ns
			4.5			77		96	
			6.0			66		82	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − a~g)		2.0			385		480	ns
			4.5			77		96	
			6.0			66		82	
t_{PHL}			2.0			385		480	ns
			4.5			77		96	
			6.0			66		82	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (BI − a~g)		2.0			240		300	ns
			4.5			48		60	
			6.0			41		51	
t_{PHL}			2.0			240		300	ns
			4.5			48		60	
			6.0			41		51	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (Ph − a~g)		2.0			175		220	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		220	ns
			4.5			35		44	
			6.0			30		37	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

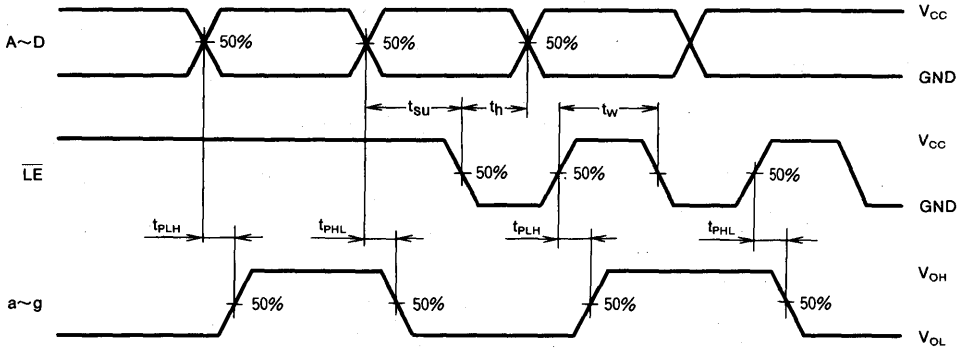
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W	$\overline{LE}$ pulse width		2.0	75			95		ns
			4.5	15			19		
			6.0	13			16		
t_{su}	A~D setup time with respect to $\overline{LE}$		2.0	75			95		ns
			4.5	15			19		
			6.0	13			16		
t_h	A~D hold time with respect to $\overline{LE}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		

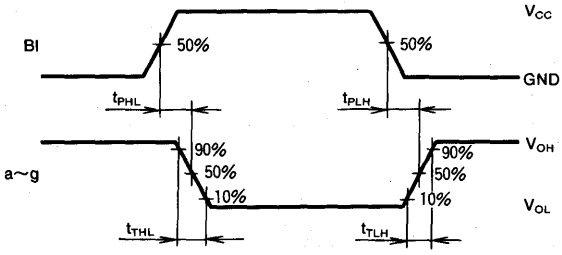
Note 4 : Test Circuit

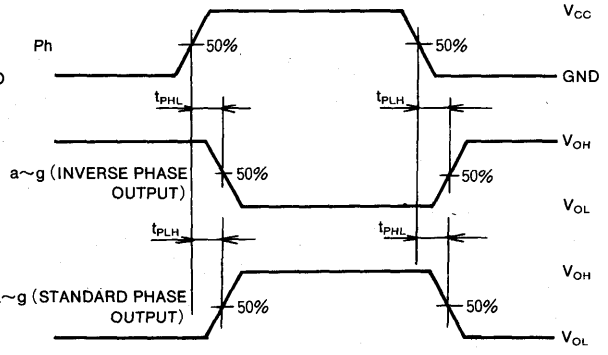


(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM

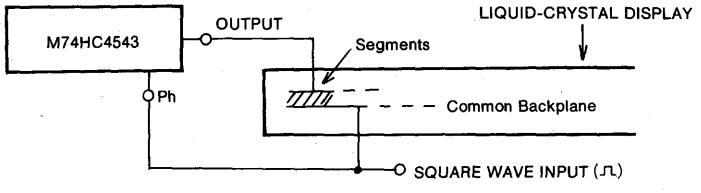






APPLICATION EXAMPLE

LIQUID-CRYSTAL DISPLAY DRIVER



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