1995 MITSUBISHI SEMICONDUCTORS SOUND PROCESSOR ICs

MITSUBISHI ELECTRIC

MITSUBISHI SEMICONDUCTORS 1995

SOUND PROCESSOR ICs

DATA BOOK

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GUIDANCE 1

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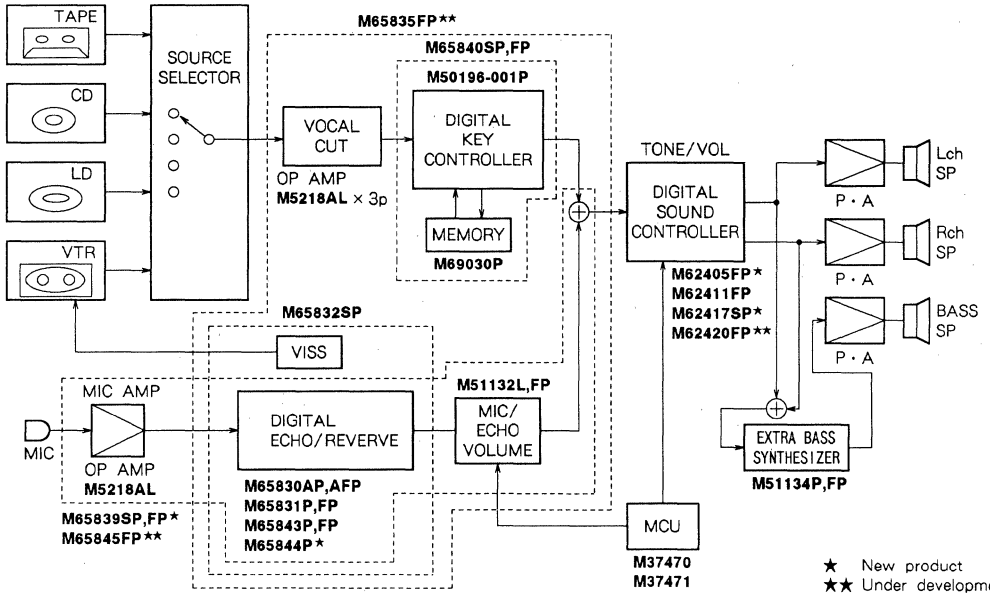
★ : New product ★★ : Under development

APPLICATION EXAMPLES

KARAOKE SOUND PROCESSORS

- These integrated circuits process iternal signals digitally. They are superior in performance and versatility to conventional analog processors.
- A great variety of products are available, including one with video search function and another with a built-in micro-phone amplifier. A suitable one can be selected according to the specifications of the system.
- The most advanced technologies are used to produce these ICs, such as fine processing. A mass storage memory and microcomputer unit are built-in, and digital processors and analog processors are installed in mixture. These ICs are a step toward the development of the "system-on-chip."

KARAOKE PLAYER BLOCK DIAGRAM



KARAOKE SOUND PROCESSOR LIST

◎ Stereo or two channels ★ New product ★★ Under development

Type name	Echo			Key control		Around function									Control system	Vcc	Icc	Outline
	Delay time	Band	RAM (BIT)	Variation range (One step= one half tone)	RAM (BIT)	Surround	Mic amp	ALC	Mic volume	Echo volume	Vocal cut	Bass boost	Line mixing	VCR song selection				
M65830P,FP	131ms	3kHz	16K	–	–										3-line serial	5V	16mA	24P4/ 24P2W
M65830AP, AFP	131ms	3kHz	16K	–	–										2 bit parallel	5V	16mA	24P4/ 24P2W-A
M65831P,FP	197ms	7kHz	48K	–	–										3-line serial, or 4bit parallel	5V	16mA	24P4/ 24P2W-A
M65832SP	139ms	3kHz	18K	–	–							◎	◎	○	4 bit parallel	5V	40mA	48P4B
M65839SP, FP★	131ms	3kHz	16K	–	–		◎	◎	◎	○			◎		3-line serial, or DC voltage	5V	40mA	36P4E/ 36P2R-A
M65835FP★★	139ms	3kHz	18K	-4~+3 -20~+20	32K				○	○	◎	◎	◎	○	Built-in control MCU	5V	65mA	100P6S-A
M65840SP, FP★	–	–	–	-20~+20 steps	32K								○		3-line serial	5V	30mA	28P4B/ 28P2W-A
M65843P,FP	125ms	2kHz	10K	–	–										–	5V	13mA	24P4/ 24P2W-A
M65844P★	150ms	1kHz	4K	–	–										–	5V	30mA	14P4
M65845FP★★	150ms	1kHz	4K	–	–		◎	◎			◎		◎		–	5V	40mA	36P2R
M65846FP★★	131ms	3kHz	16K	–	–	◎				○			◎		3-line serial, or 3bit parallel	5V	40mA	32P2W-A

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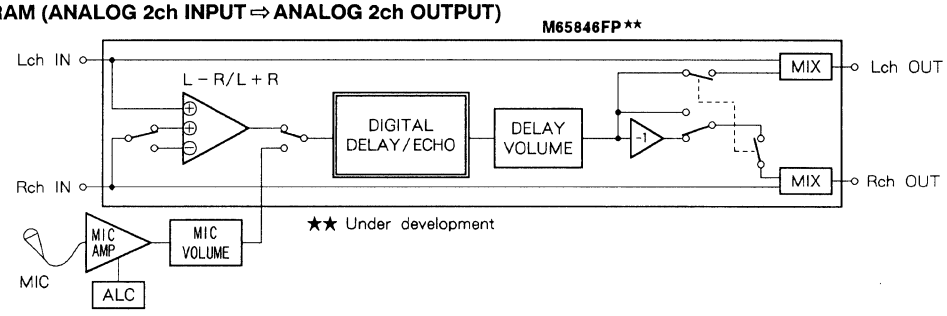
APPLICATION EXAMPLES

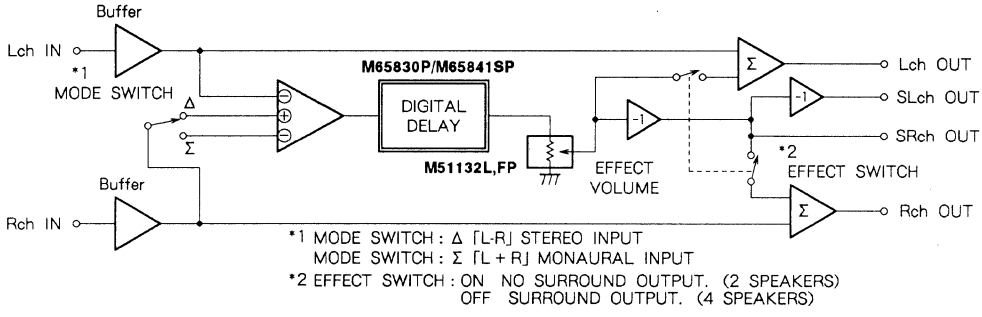
SURROUND PROCESSOR

- A wide choice of products are available, such as Dolby prologic surround processoes, surround processors and reverve sound processors. A suitable one can be selected according to the application.
  (televisions, audio-visual system amplifier, etc.)
- The Dolby prologic surround system can be formed with only two chips : a decoder and digital delay circuit.
- The digital delay circuit and digital reverve circuit for the surround system have all necessary functions built-in : an input/output low-pass filter, analog-digital/digital-analog converter, and memory.

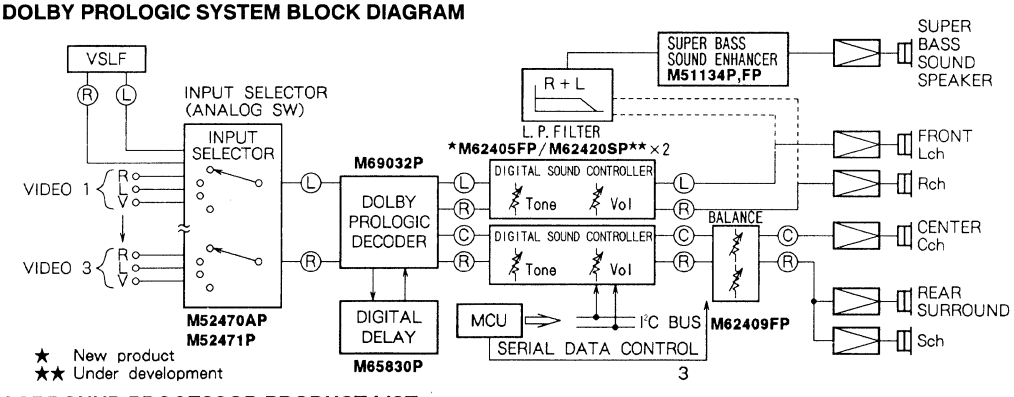
DIGITAL SURROUND/ECHO SOUND CONTROLLING COMBINATION LARGE-SCALE INTEGRATED CIRCUIT BLOCK DIAGRAM (ANALOG 2ch INPUT ⇨ ANALOG 2ch OUTPUT)



SURROUND PROCESSOR BLOCK DIAGRAM (ANALOG 2ch INPUT ⇨ ANALOG 4ch OUTPUT)



DOLBY PROLOGIC SYSTEM BLOCK DIAGRAM



SORROUND PROCESSOR PRODUCT LIST

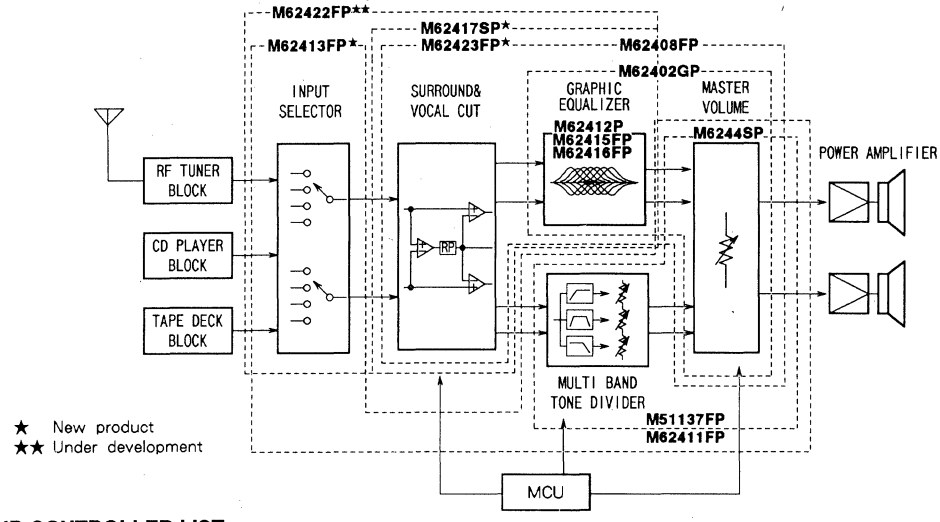
★★ Under development

Type name	Function	Features	Outline
M50198P,FP	Single chip digital delay	Built-in 8K bit SRAM Delay time 5 msec, one step 5~40msec, 80 μ sec	24P4/24P2W-A
M65830P,FP	Single chip digital delay	Built-in 16K bit SRAM Delay time 0.5msec, one step 0.5~32msec	24P4/24P2W-A
M65841SP	Digital reverve	Built-in 40K bit SRAM, 163.8 msec max, High-performance version of M50194AP. Reverve : delay time is output to 5 lines.	40P4B
M69032P	Dolby prologic decoder	Input automatic balance, modified dolby B function and noise reduction function are built-in. Dolby prologic surround system can be formed with two chips when this IC is combined with digital delay circuit M65830P	56pin SDIP
M65846FP**	Single chip surround processor	Built-in 16K bit SRAM, digital delay, delay volume, and line mixing amplifier Four modes (disco, hall, live and echo) are available.	32P2W-A

APPLICATION EXAMPLES

SOUND CONTROLLERS

SOUND CONTROLLER BLOCK DIAGRAM (FOR HOME AUDIO SYSTEMS AND PORTABLE AUDIO SYSTEMS)



SOUND CONTROLLER LIST

Vcc : 2 SUPPLY TYPE FOR HOME AUDIO SYSTEMS

★ New product ★★ Under development

Type name	Supply voltage Vcc(V)	Supply voltage VDD(V)	ICC (mA)	Master volume	Tone control (bass/treble, G·EQ)	Optional functions	Maximum output voltage (Vrms)	Distortion (%)	S/N ratio (dB)	Micro-computer interface	Outline
M62402GP	±7	5	60	VCA + DAC (8bit DAC)	· 7-Band graphic equalizer	· Bass boost · Mute	3.5	0.005	min 90dB Vo=1Vrms No=30μV	3-line	100P6S-A
M62408FP	±7	5	60	R – ladder + zero-cross	· 5-Band graphic equalizer	· Bass boost · Surround · Vocal cut · Mute	3.0	0.005	min 96dB Vo=1Vrms No=15μV	3-line	100P6S-A
M62417SP★	±7	5	22	–	· Bass, treble	· Bass boost · Surround · Vocal cut · Mute	3.0	0.02	min 94dB Vo=1Vrms No=20μV	3-line	32P4B
M62422FP★★	±7	5	25	–	· Bass, mid treble	· Bass boost · Surround · Vocal cut · With key control adapter	3.0	0.005	min 94dB Vo=1Vrms No=20μV	2-line	42P2R-A
M62423FP★	±7	5	22	–	· Bass, mid treble	· Bass boost · Surround · Vocal cut · Mute	3.0	0.02	min 94dB Vo=1Vrms No=20μV	3-line	42P2R-A

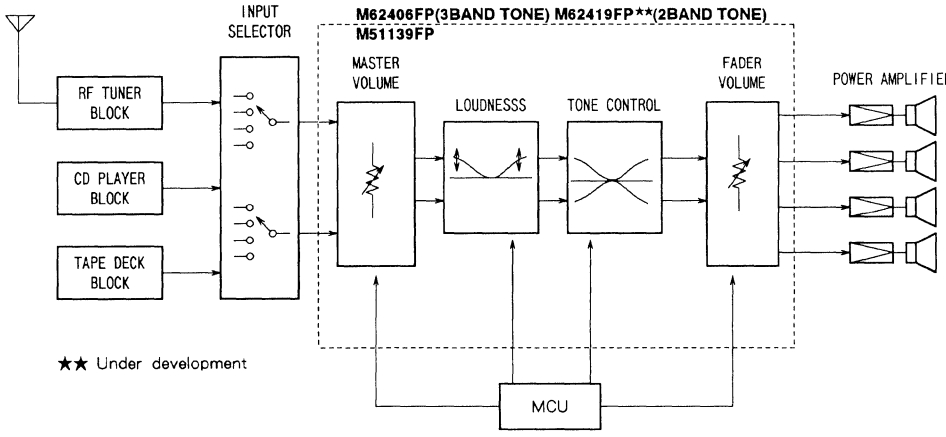
Vcc : 1 SUPPLY TYPE FOR PORTABLE AUDIO SYSTEMS

Type name	Supply voltage Vcc(V)	Supply voltage VDD(V)	ICC (mA)	Master volume	Tone controlle (bass/treble, G·EQ)	Optional functions	Maximum output voltage (Vrms)	Distortion (%)	S/N ratio (dB)	Micro-computer interface	Outline
M51137FP	9	Internal power supply	38	VCA + DAC (8bit + DAC)	· 3-band	· Extra bass	2.5	0.002	min 100dB Vo=1Vrms No=10μV	3-line	42P2R-A
M62411FP	9	Internal power supply	38	VCA + DAC (8bit + DAC)	· 3-band	· Extra bass	2.5	0.002	min 100dB Vo=1Vrms No=10μV	3-line	42P2R-A
M62412P★	10.7	–	15	–	· 3-band preset type	–	2.5	0.002	min 94.9dB Vo=1Vrms No=18μV	–	16P4
M62413FP	9	Internal power supply	45	VCA + DAC (8bit + DAC)	· 3-band	· Output port · Input selector · Extra bass	2.5	0.002	min 100dB Vo=1Vrms No=10μV	3-line	64P6N-A
M62414SP	9	Internal power supply	17	VCA + DAC (7bit + DAC)	–	· Output port	2.0	0.001	min 100.9dB Vo=1Vrms No=9μV	2-line	20P4B
M62415FP★★	9	–	29	–	· 3-band preset type	· LED driver	2.5	0.005	min 106.9dB Vo=1Vrms No=4.5μV	–	24P4D
M62416FP★★	7	Vcc/2	15	–	· 3-band	–	2.5	0.005	min 101.9dB Vo=1Vrms No=8μV	3-line	24P2Q-A

APPLICATION EXAMPLES

SOUND CONTROLLERS

SOUND CONTROLLER BLOCK DIAGRAM (FOR CAR AUDIO SYSTEMS)

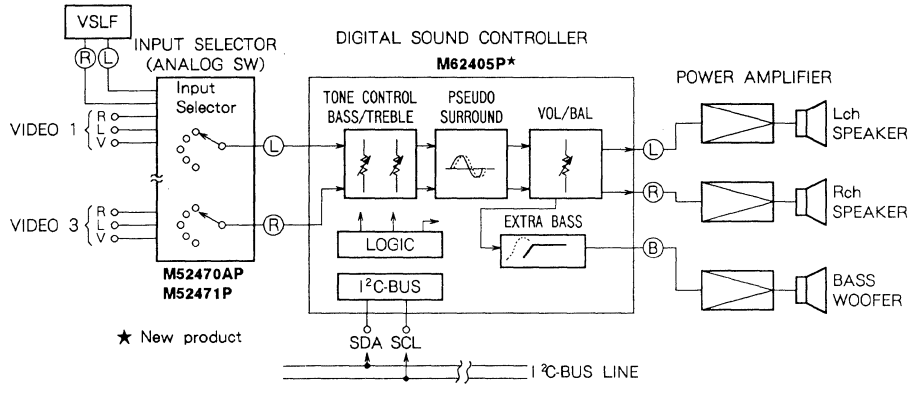


Vcc : 1 POWER SUPPLY TYPE FOR CAR AUDIO SYSTEMS

★★ Under development

Type name	Supply voltage		ICC (mA)	Master volume	Tone control (bass/treble, G·EQ)	Optional functions	Maximum output voltage (Vrms)	Distortion (%)	S/N ratio (dB)	Micro-computer interface	Outline
	VCC(V)	VDD(V)									
M51139FP	8	5	15	R – ladder + zero-cross	· Bass, mid treble	· Fader · Loudness	1.8	0.005	min 88dB VO=1Vrms NO=40μV	3-line	60P6-B
M62406FP	8	5	38	R – ladder + zero-cross	· Bass, mid treble	· Fader · Loudness	1.3	0.01	min 96dB VO=1Vrms NO=15μV	3-line	64P6N-A
M62409FP	8	5	10	R – ladder + zero-cross	–	· Loudness	2.2	0.003	min 96dB VO=1Vrms NO=15μV	3-line	32P2U-B
M62419FP**	8	5	35	R – ladder	· Bass, treble	· Fader	2.2	0.003	min 96dB VO=1Vrms NO=15μV	2-line	42P2R-A

SOUND CONTROLLER BLOCK DIAGRAM (FOR TVs)



Vcc : 1 POWER SUPPLY TYPE FOR TVs

★ New product ★★ Under development

Type name	Supply voltage		ICC (mA)	Master volume	Tone control (bass/treble, G·EQ)	Optional functions	Maximum output voltage (Vrms)	Distortion (%)	S/N ratio (dB)	Micro-computer interface	Outline
	VCC(V)	VDD(V)									
M62405P*	9	5	25	R – ladder	· Bass, treble	· Bass boost · Surround	1.7	0.02	min 90dB VO=1Vrms NO=30μV	I²C Bus	52P4B
M62420SP**	9	5	20	R – ladder	· Bass, treble		1.7	0.02	min 90dB VO=1Vrms NO=30μV	I²C Bus	20P4B

APPLICATION EXAMPLES

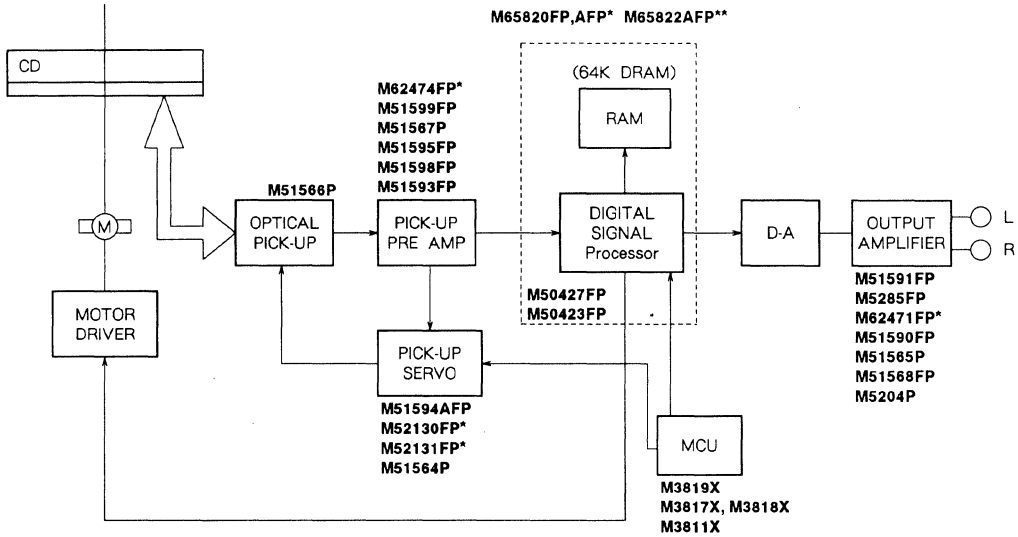
ELECTRONIC VOLUME, GRAPHIC EQUALIZER

Type name	Function	Features	Supply voltage Vcc(V)	Circuit current Icc(mA)	Outline
M5206P	Linear control dual VCA	• Log1 linear control can be selected • Controls right output and left output independently • High voltage resistance (Vcc = ± 18V)	± 15	4.3	14P4
M5207L01/ M5207L05	Linear control Dual VCA	• Linear control • Controls left output and right output independently	9(L01) ±15(L05)	4.3	10P5
M5222L,P,FP	Low voltage dual VCA	• Operates at low voltages • Amplifies logarithmically according to control voltage • Controls right output and left output at the same time	3	3.6	8P5 8P4 8P2S-A
M5241L	Logarithmic control dual VCA	• Adjusts bias current with external resistance • Controls right output and left output independently	± 15	3.8	10P5
M5282FP	Electronic volume with microphone amplifier	• Has a built-in microphone amplifier • Operaters at low voltages • Voltage input, voltage output	5	8.7	10P2-C
M5283P	Dual VCA for high-fidelity systems	• Low noise V_{NO} = 4μVrms • Low distortion THD = 0.004% • Controls right output and left output independently	± 15	30	16P4
M5226P,FP	5-element graphic equalizer	• 5 resonant elements + buffer amplifier	9	5.2	16P4 16P2S-A
M5227P,FP	5-element graphic equalizer	• 5 resonant elements + buffer amplifier	± 15	8.0	16P4 16P2S-A
M5229P,FP	7-element graphic equalizer	• 7 resonant elements + buffer amplifier	± 15	11.0	20P4 20P2N-A
M5243P,FP	3-element dual graphic equalizer	• (3 resonant elements + buffer amplifier) × 2ch	6~12	9.0	20P4 20P2N-A
M5289P,FP	7-element graphic equalizer	• 7 resonant elements + buffer amplifier • Low noise	± 15	18	20P4 20P2N-A
M51134P,FP	Sub-harmonizer for extra bass control	• The output level can be set according to the input level • Using envelope detection circuit • Has a built-in VCA circuit	12	12	20P4 20P2N-A
M62403P,FP	Automatic power switch with equalizer control	• High input signal detecting sensitivity : 3mVrms • Has a built-in LED drive circuit	6	7	16P4 16P2N-A
M62404P,FP	Analog switch with built-in amplifier	• Used to switch among three modes • Low-noise, low-distortion	12	12.7	20P4 20P2N-A
M51132L,FP	Dual VCA · balance	• Low-noise, low-distortion • Maximum input voltage : 3.4Vrms	12	10	14P5A 16P2N-A
M51523AL	Dual VCA	• Low-noise, low-distortion • Excellent temperature characteristics	12	12	14P5A

APPLICATION EXAMPLES

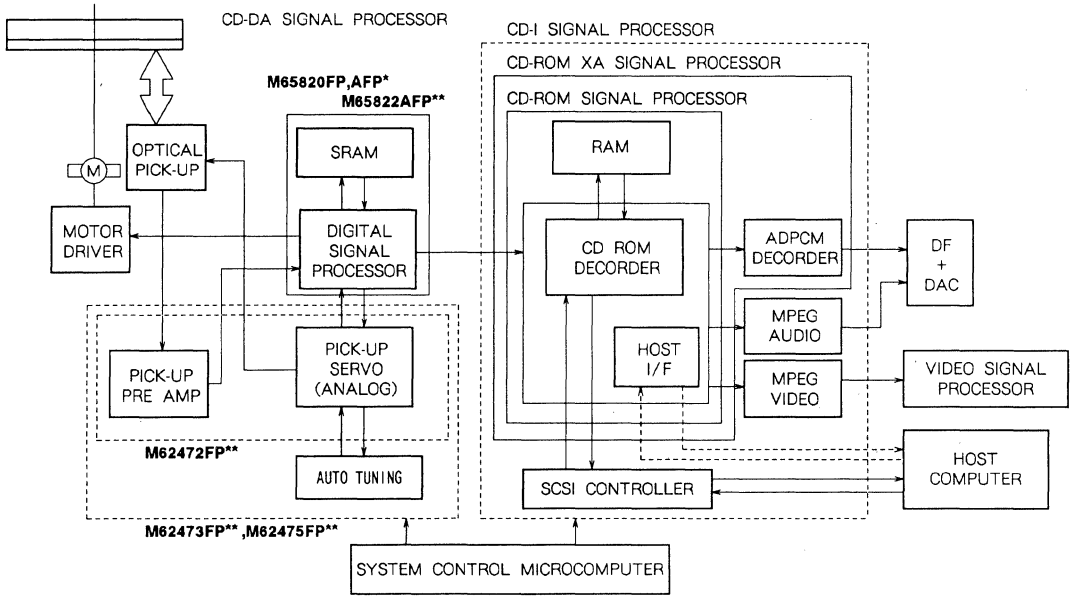
CD PLAYER LSI KIT

CD PLAYER BLOCK DIAGRAM



★ New product ★★ Under development

CD-ROM PLAYER SYSTEM BLOCK DIAGRAM



★ New product ★★ Under development

APPLICATION EXAMPLES

DIGITAL SIGNAL PROCESSORS FOR CD PLAYERS (DIGITAL SIGNAL PROCESSING LSIs)

Type name	Built-in functions								Vcc (V)	Icc (mA)	Outline
	Memory	EFM-PLL	CLV servo	Digital filter	Digital output	Q register	Jitter margin	Pick up servo			
M50423FP	External 64K DRAM	○ (unadjusted)	○	2FS/4FS 27th/59th	○	○	±8	×	5	18	80P6-B
M50427FP	External 64K DRAM	○ (unadjusted)	○	2FS 27th	×	×	±8	×	5	15	72P6-B
M65820FP	Built-in 32K SRAM	○ (unadjusted)	○	2FS/4FS 27th/59th	○	○	±8	×	5	18	80P6N-A
M65820AFP*	Built-in 32K SRAM	○ (unadjusted)	○	2FS/4FS 27th/59th	○	○	±8	×	5	16	80P6N-A
M65822AFP**	Built-in 18K SRAM	○ (unadjusted)	○	4FS 95th	○	○	±8	×	5	40	42P2R-A

PICKUP PREAMPLIFIERS FOR CD PLAYERS

Type name	Built-in functions								Vcc (V)	Icc (mA)	Outline
	PD	IV Amp.	HF Amp.	FE Amp.	TE Amp.	APC circuit	HF OK	MR			
M51566P	○	○	×	×	×	×	×	×	+5/±5	3.5/±4	10C2-C
M51567P	×	○	○	○	○	×	○	○	+5/±5	18/±18	24P2Q-A
M51593FP	×	○	○	○	○	○	×	×	+5/±5	6/±12	20P2E-A
M51595FP	×	○	○	○	○	○	○	○	+5	17	24P2Q-A
M51598FP	×	○	○	○	○	×	○	○	+5	17	24P2Q-A
M51599FP	×	○	○	○	○	×	○	○	±5	±19	24P2Q-A
M62474FP*	×	○	○	○	○	×	○	○	+5	17	24P2Q

OPTICAL PICKUP SERVO CONTROLS FOR CD PLAYERS

Type name	Built-in functions								Vcc (V)	Icc (mA)	Outline
	FE Amp.	FSR/FS/TE/TS/SS circuit	T. HLD	SHOCK	RESET circuit	APC circuit	HFOK circuit	MR circuit			
M51564P	×	○	○	○	×	×	×	×	+5/±5	13/+4 −12	36P2R-A
M51594AFP	○	○	×	×	○	○ (SW only)	×	×	+5/±5	13/+4 −12	42P2R-A
M52130FP*	×	○	○	○	×	×	○	○	+5/±5	17/+17 −16	42P2R-A
M52131FP*	○	○	×	×	○	○ (SW only)	×	×	+5/±5	13/+4 −12	42P2R-A
M62472FP**	○	○	×	×	○	○	○	○	+5	28	42P2R

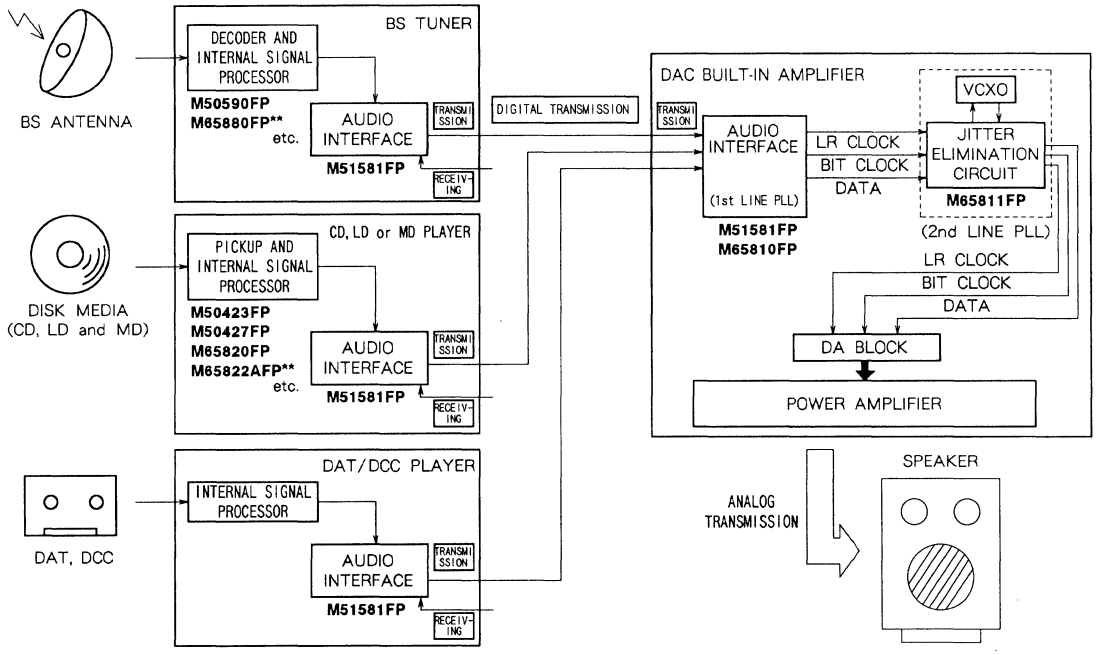
OUTPUT AMPLIFIERS FOR CD PLAYERS

Type name	Built-in functions							Vcc (V)	Icc (mA)	Outline
	LPF amp	Deglicher circuit	De-emphasis circuit	Mute circuit	Headphone amplifier	Buffer amplifier	Reference voltage output			
M51565P	○	○	○	○	○	×	×	±5	43	32P4B
M51568FP	○	×	○	○	○	×	○	5	6.3	24P2Q-A
M51590FP	○	×	×	×	×	○	○	9	5.1	20P2N-A
M51591FP	○	×	○	○	×	×	○	9	5.1	28P2W-A
M62471FP*	○	×	×	○	○	×	○	3	10	24P2Q-A
M5204P	×	×	×	○	○	○	×	±5	±11	20P4B
M5285FP	×	×	×	○	×	○	×	±5	±11	16P2S-A

★ : New product ★★ : Under development

APPLICATION EXAMPLES

DIGITAL AUDIO INTERFACE
SYSTEM BLOCK DIAGRAM



★★ Under development

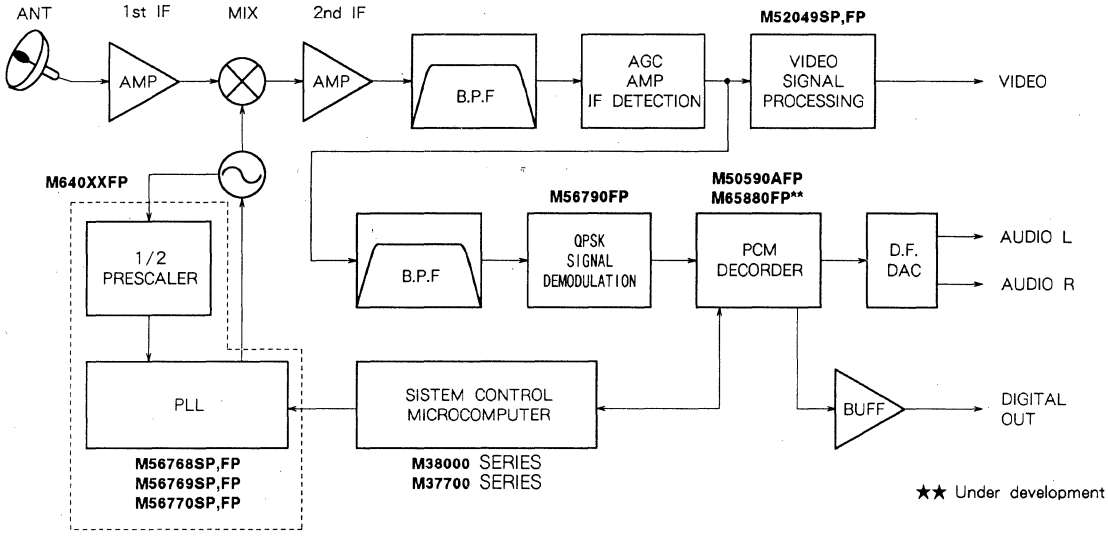
DIGITAL AUDIO INTERFACE LIST

Type name	Functions				Standard electric characteristics		Outline
	Function name	PLL	Mute function	Other	Vcc(V)	Icc(V)	
M51581FP	Digital audio interface transmission and reception	External VCO	Provided	• Optical coaxial input • Can be controlled with microcomputer • I²S format can be used • U-bit/C-bit interface provided	5	16	44P6W-B
M65810FP	Digital audio interface reception	Built-in	Provided	•Optical coaxial input •Can be controlled with microcomputer •U-bit/V-bit/C-bit interface provided •Word clock signal output is possible	5	20	36P2R-A
M65811FP	Jitter absorber for digital audio systems	External VCXO	Provided	• Master clock frequency can be selected from between 384.256fs • Able to output master clock signals of 128fs,64fs and 2fs (word clock) and of 1fs (LR clock)	5	6	28P2U-A

APPLICATION EXAMPLES

BS/CS TUNER LSI KIT

BS/CS TUNER SISTEM BLOCK DIAGRAM



IC FOR BS/CS TUNER

Type name	Function	Features	Outline
M56790FP	BS/CS QPSK decoder	· Requires far fewer external components, compared with conventional ones · Clock signal generation circuit is built-in for PCM decoder The frequency can be selected from between 36.864MHz and 18.432MHz · Built-in LPF for COSTASLOOP · Built-in AGC amplifier · Unadjusted · Single 5V power supply	24P2Q-A
M50590AFP	BS PCM decoder	· Main clock frequency can be selected from between 36.864MHz and 12.288MHz · Clock frequency output for digital filter : 768fs~128fs · Built-in 4K bit SRAM · Built-in clock signal regeneration PLL · Forced muting can be turned on by using control codes · Built-in output signal selection circuit	72P6-B
M65880FP**	BS/CS PCM decoder	· Small package (44pins) · Main clock frequency can be selected from between 36.864MHz and 18.432MHz · Clock frequency output for digital filter : 768fs~192fs · Built-in 2K bit SRAM · Built-in clock signal regeneration PLL · Phase error voltage polarity can be determined for PLL control · Clock signals can be regenerated based on QPSK/bit stream input (switchable) · Built-in selecter for double decoder · Able to identify master frame	44P6N-A

★★ : Under development

APPLICATION EXAMPLES

OTHERS GENERAL-PURPOSE AUDIO ICs

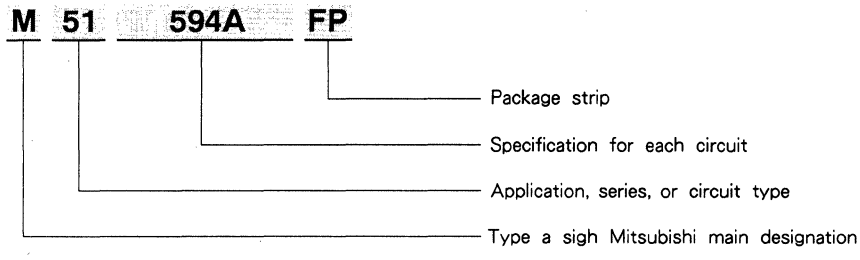
Application	Type name	Function	Standard electrical characteristics		Outline	Remarks
			Vcc (V)	Icc (mA)		
Recording/ playback preamplifiers	**M51141P**	Dual Recording/Playback Amplifier with ALC	3	4	20P2	
	M51166P	Dual Recording/Playback Amplifier with ALC	9	6	18P4	
	M51167AP,AFP	Single Chip Recording/Playback Amplifier	9	20	36P4E/36P2R-A	
	M51167BP,BFP	Single Chip Recording/Playback Amplifier	9	20	36P4E/36P2R-A	
	M52122FP	Single Chip Recording/Playback Amplifier	6	38	42P2R-A	with automatic adjusting function
	M62451FP★	Single Chip Recording/Playback Amplifier	6	42	56P6N-A	with automatic adjusting function
	M51524L,P,FP	Auto reverse preamplifier with music sensor	8	9	20P5A/24P4D /24P2N-B	
	M51525P,FP,GP	Auto reverse preamplifier with music sensor	8	9	24P4D/24P2N-B /24P2Q-A	
Preamplifiers	**M5219L,P,FP**	Dual Low Noise Pre-Amplifier	± 22.5	3.5	8P5C/8P4/8P2	S/N = 77dB
	M5220L,P,FP	Dual Low Noise Pre-Amplifier	± 22.5	4.0	8P5/8P4/8P2	S/N = 83dB
Others	**M51143AL**	Music Selector	6	3.5	8P5	
	M5280L,P,FP	Ground Isolator Amplifier	12	6.3	8P5/8P4 /8P2S-A	Car audio chassis ground noise reduction
	M54418P	Tape Selector	8-23	15	16P4	
	M62302P,FP	A-D converter for AV lever meter	5	6	14P4/14P2N	4bit logarithmic compression type

★ : New product

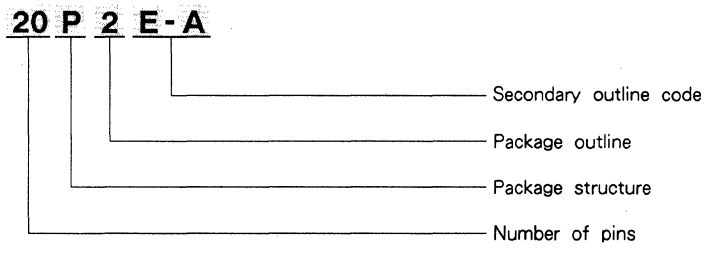
ORDERING INFORMATION

The type codes and package outline of the Mitsubishi semiconductor integrated circuits are outlined below for your reference.

Example 1) Products



Example 2) Package



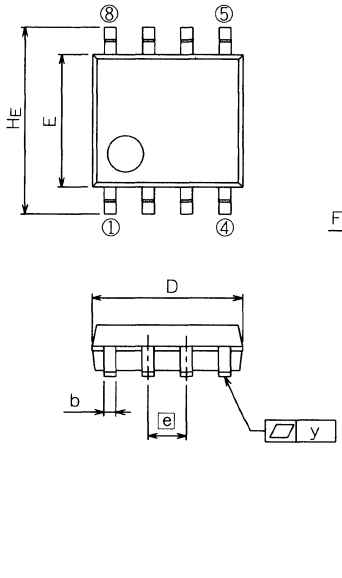
PACKAGE OUTLINES

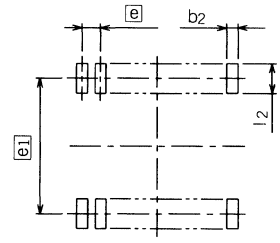
8P2S-A

Plastic 8pin 225mil SOP

EIAJ Package Code	JEDEC Code	Weight(g)
*SOP008-P-0225	—	0.07

Scale : 4/1





Recommended Mount Pad

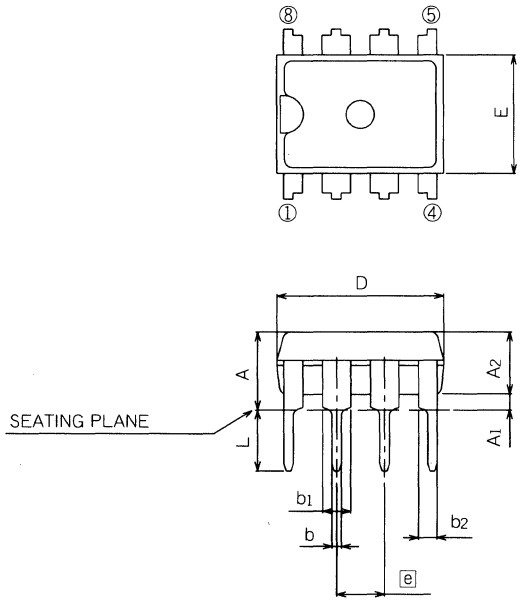
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.9
A1	0.05	—	—
A2	—	1.5	—
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	4.8	5.0	5.2
E	4.2	4.4	4.6
e	—	1.27	—
HE	5.9	6.2	6.5
L	0.2	0.4	0.6
L1	—	0.9	—
y	—	—	0.1
θ	0°	—	10°
b2	—	0.76	—
e1	—	5.72	—
l2	1.27	—	—

8P4

Plastic 8pin 300mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
*DIP008-P-0300	—	0.5

Scale : 2.5/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.5
A1	0.51	—	—
A2	—	3.3	—
b	0.4	0.5	0.6
b1	1.4	1.5	1.8
b2	0.9	1.0	1.3
c	0.22	0.27	0.34
D	8.7	8.9	9.1
E	6.15	6.3	6.45
e	—	2.54	—
e1	—	7.62	—
L	3.0	—	—
θ	0°	—	15°

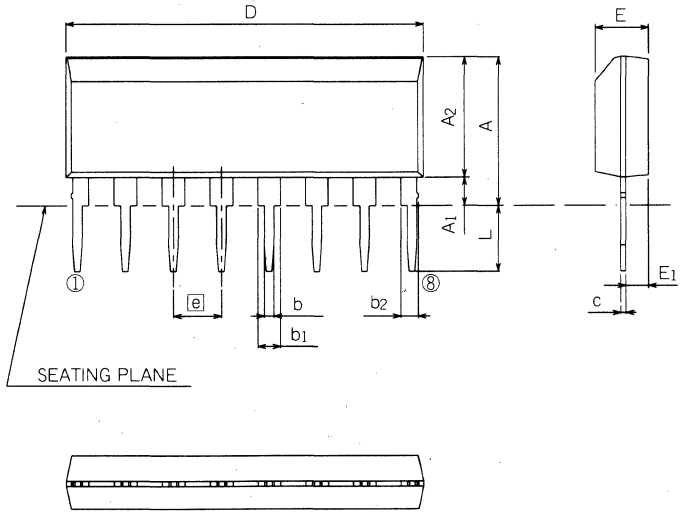
PACKAGE OUTLINES

8P5

Plastic 8pin 340mil SIP

EIAJ Package Code	JEDEC Code	Weight(g)
*SIP008-P-0340	—	0.73

Scale : 2.5/1



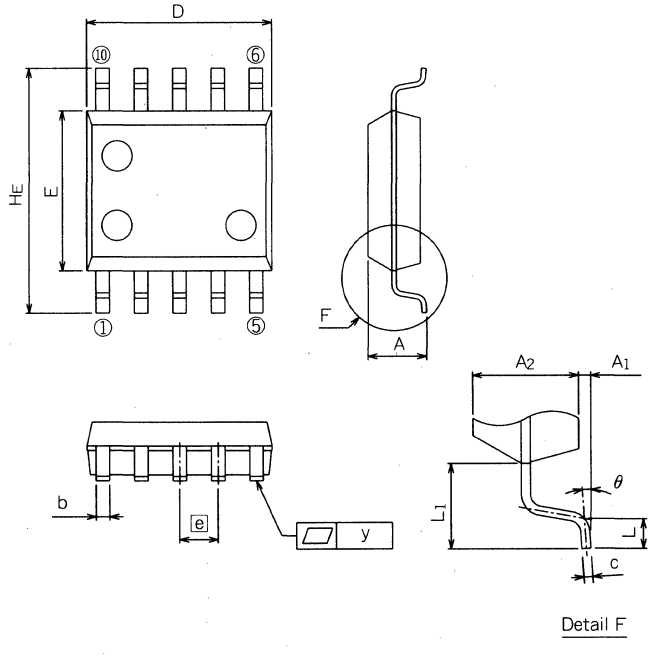
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	8.3
A1	1.2	—	—
A2	—	6.4	—
b	0.4	0.5	0.6
b1	1.1	1.2	1.5
b2	0.75	0.85	1.15
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	2.6	2.8	3.0
E1	1.1	1.2	1.3
e	—	2.54	—
L	3.0	—	—

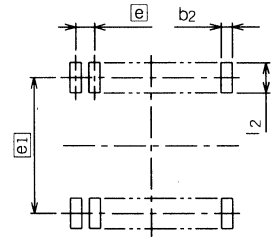
10C2-C

Plastic(Clear resin)10pin 300mil SOP

EIAJ Package Code	JEDEC Code	Weight(g)
*SOP010-P-0300	—	0.12

Scale : 4/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.15
A1	0.05	—	—
A2	—	1.75	—
b	0.4	0.45	0.55
c	0.13	0.15	0.2
D	5.93	6.13	6.33
E	5.1	5.3	5.5
e	—	1.27	—
HE	7.82	8.12	8.42
L	0.3	0.5	0.7
L1	—	1.41	—
y	—	—	0.1
θ	0°	—	10°
b2	—	0.76	—
e1	—	7.62	—
l2	1.27	—	—

MITSUBISHI ELECTRIC

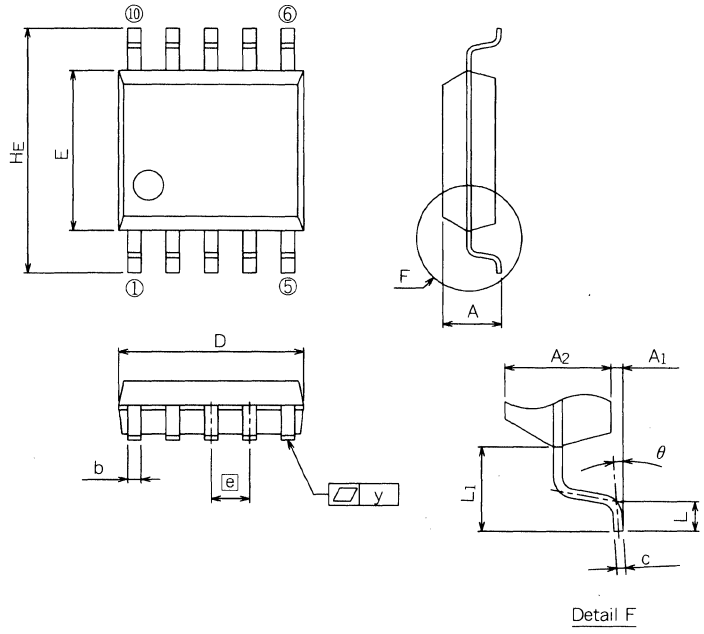
PACKAGE OUTLINES

10P2-C

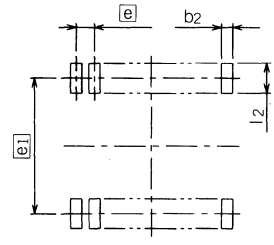
Plastic 10pin 300mil SOP

EIAJ Package Code	JEDEC Code	Weight(g)
*SOP010-P-0300	—	0.12

Scale : 4/1



Detail F



Recommended Mount Pad

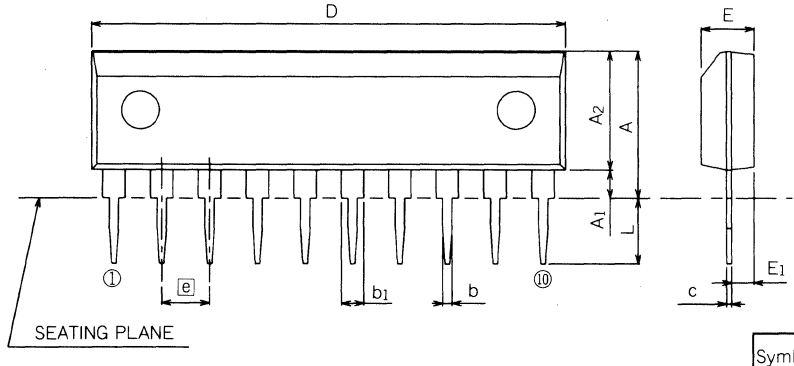
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.15
A_1	0.05	—	—
A_2	—	1.75	—
b	0.4	0.45	0.55
c	0.13	0.15	0.2
D	5.93	6.13	6.33
E	5.1	5.3	5.5
e	—	1.27	—
H_E	7.82	8.12	8.42
L	0.3	0.5	0.7
L_1	—	1.41	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.76	—
e1	—	7.62	—
l_2	1.27	—	—

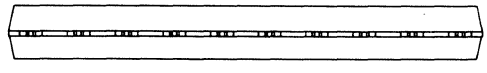
10P5

Plastic 10pin 340mil SIP

EIAJ Package Code	JEDEC Code	Weight(g)
*SIP010-P-0340	—	0.94

Scale : 2.5/1





Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	8.3
A_1	1.2	—	—
A_2	—	6.3	—
b	0.4	0.5	0.6
b_1	1.1	1.2	1.5
c	0.22	0.27	0.34
D	25.03	25.23	25.43
E	2.6	2.8	3.0
E_1	1.1	1.2	1.3
e	—	2.54	—
L	3.0	—	—

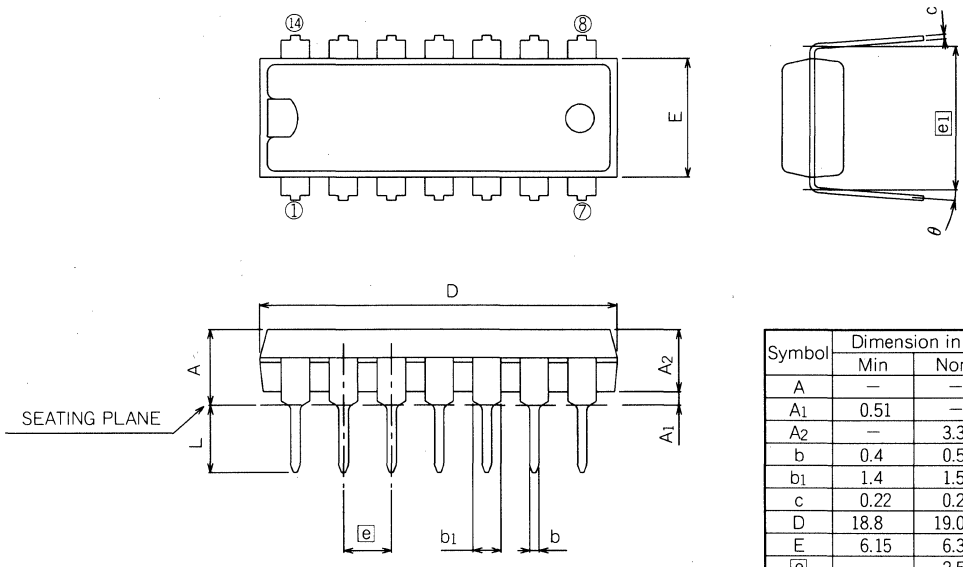
PACKAGE OUTLINES

14P4

Plastic 14pin 300mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
*DIP014-P-0300	—	1.0

Scale : 2.5/1



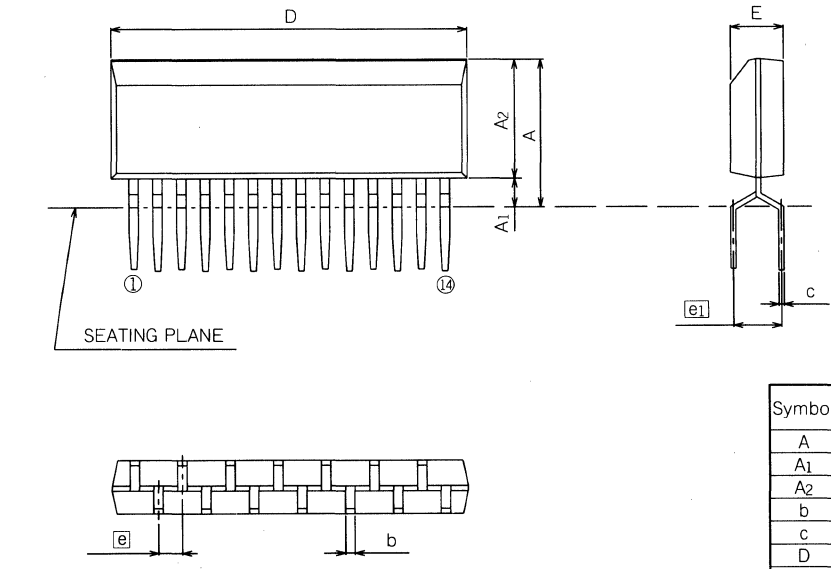
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b	0.4	0.5	0.6
b_1	1.4	1.5	1.8
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	6.15	6.3	6.45
e	—	2.54	—
e_1	—	7.62	—
L	3.0	—	—
θ	0°	—	15°

14P5A

Plastic 14pin 325mil ZIP

EIAJ Package Code	JEDEC Code	Weight(g)
*ZIP014-P-0325	—	0.74

Scale : 2.5/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	8.3
A_1	0.9	—	—
A_2	—	6.3	—
b	0.4	0.5	0.6
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	2.6	2.8	3.0
e	—	1.27	—
e_1	—	2.54	—
L	2.8	—	—

MITSUBISHI ELECTRIC

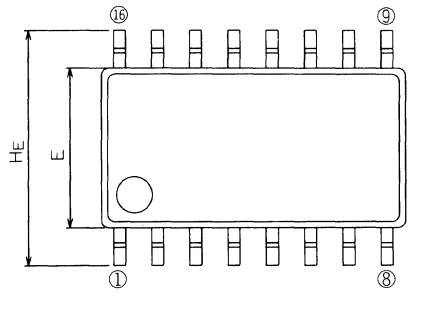
PACKAGE OUTLINES

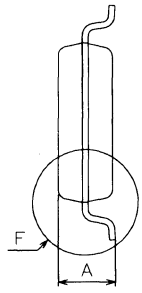
16P2N-A

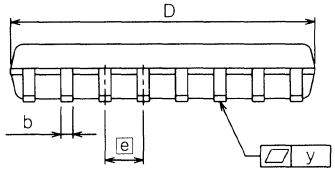
Plastic 16pin 300mil SOP

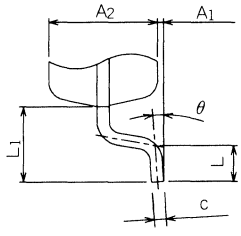
EIAJ Package Code	JEDEC Code	Weight(g)
*SOP016-P-0300	–	0.2

Scale : 4/1

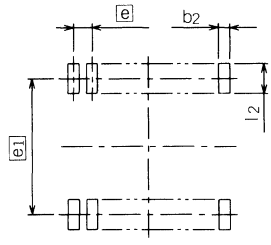








Detail F



Recommended Mount Pad

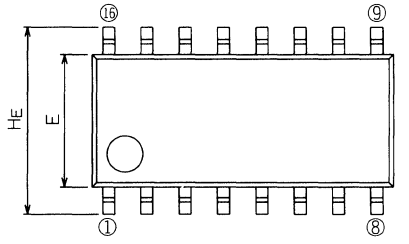
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.1
A_1	0	0.1	0.2
A_2	–	1.8	–
b	0.35	0.4	0.5
c	0.18	0.2	0.25
D	10.0	10.1	10.2
E	5.2	5.3	5.4
e	–	1.27	–
H_E	7.5	7.8	8.1
L	0.4	0.6	0.8
L_1	–	1.25	–
y	–	–	0.1
θ	0°	–	8°
b_2	–	0.76	–
e_1	–	7.62	–
l_2	1.27	–	–

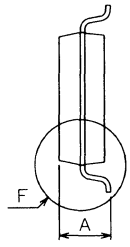
16P2S-A

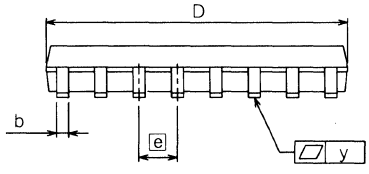
Plastic 16pin 225mil SOP

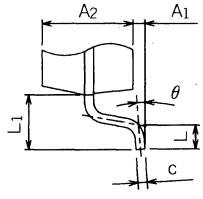
EIAJ Package Code	JEDEC Code	Weight(g)
*SOP016-P-0225	–	0.15

Scale : 4/1

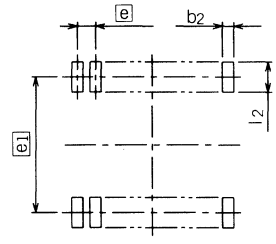








Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.9
A_1	0.05	–	–
A_2	–	1.5	–
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	9.8	10.0	10.2
E	4.2	4.4	4.6
e	–	1.27	–
H_E	5.9	6.2	6.5
L	0.2	0.4	0.6
L_1	–	0.9	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.76	–
e_1	–	5.72	–
l_2	1.27	–	–

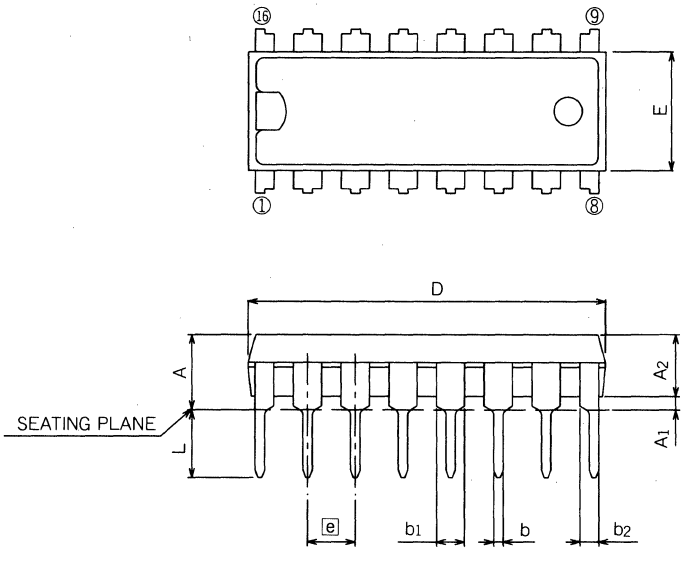
PACKAGE OUTLINES

16P4

Plastic 16pin 300mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
*DIP016-P-0300	—	1.0

Scale : 2.5/1



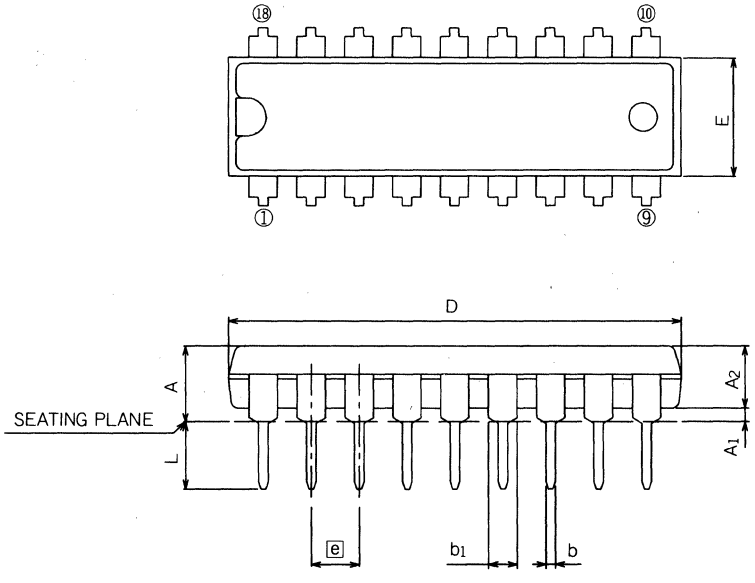
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b	0.4	0.5	0.6
b_1	1.4	1.5	1.8
b_2	0.9	1.0	1.3
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	6.15	6.3	6.45
e	—	2.54	—
e_1	—	7.62	—
L	3.0	—	—
θ	0°	—	15°

18P4

Plastic 18pin 300mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
*DIP018-P-0300	—	1.3

Scale : 2.5/1



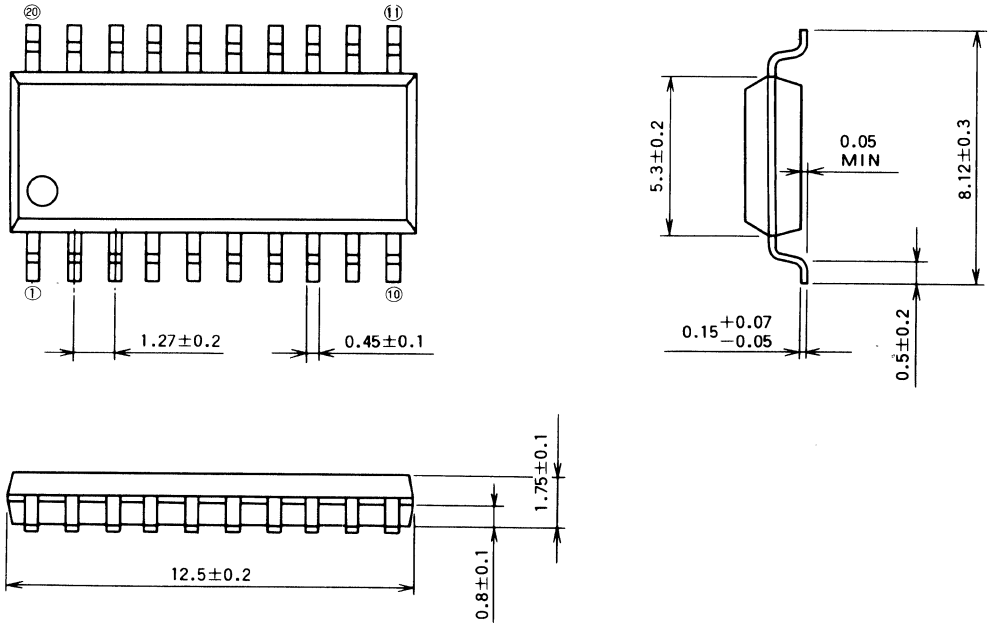
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b	0.4	0.5	0.6
b_1	1.4	1.5	1.8
c	0.22	0.27	0.34
D	23.8	24.0	24.2
E	6.15	6.3	6.45
e	—	2.54	—
e_1	—	7.62	—
L	3.0	—	—
θ	0°	—	15°

MITSUBISHI ELECTRIC

PACKAGE OUTLINES

20P2 Plastic 20pin 300mil (200mil body) SOP

Dimension in mm

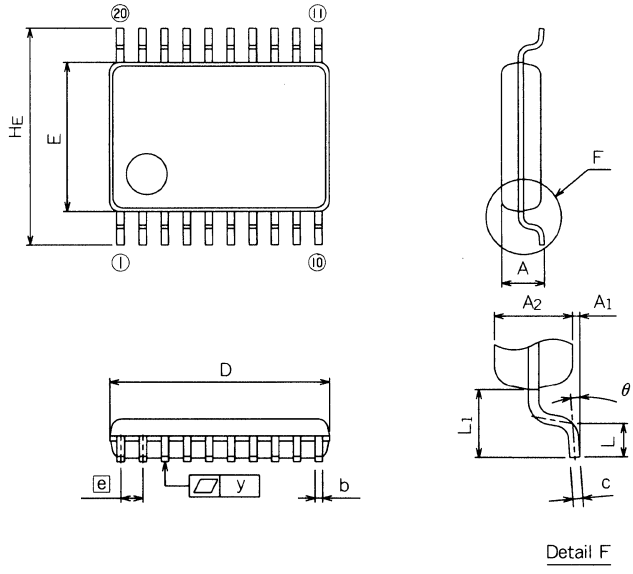


20P2E−A

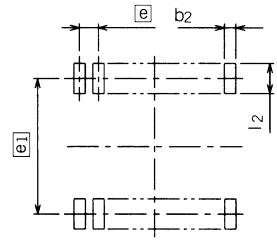
Plastic 20pin 225mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)
SSOP020-P-0225	—	0.08

Scale : 4.5/1



Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.45
A_1	0	0.1	0.2
A_2	—	1.15	—
b	0.17	0.22	0.32
c	0.13	0.15	0.2
D	6.4	6.5	6.6
E	4.3	4.4	4.5
e	—	0.65	—
H_E	6.2	6.4	6.6
L	0.3	0.5	0.7
L_1	—	1.0	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.35	—
e_1	—	5.8	—
l_2	1.0	—	—

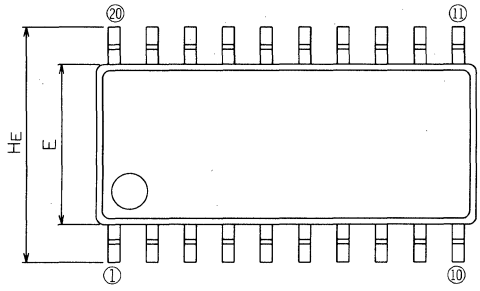
PACKAGE OUTLINES

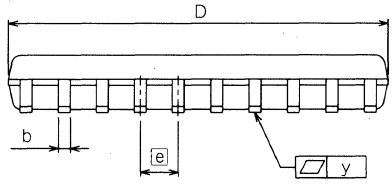
20P2N-A

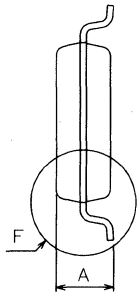
Plastic 20pin 300mil SOP

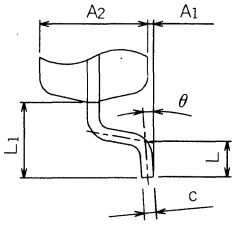
EIAJ Package Code	JEDEC Code	Weight(g)
*SOP020-P-0300	–	0.26

Scale : 4/1

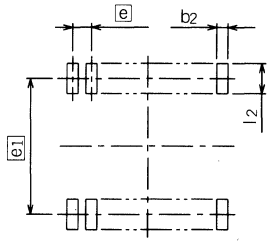








Detail F



Recommended Mount Pad

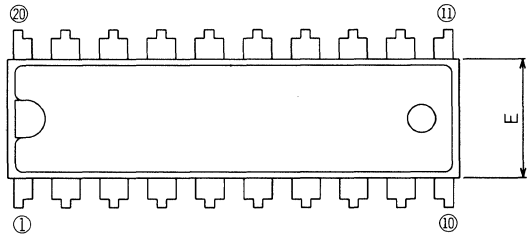
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.1
A1	0	0.1	0.2
A2	–	1.8	–
b	0.35	0.4	0.5
c	0.18	0.2	0.25
D	12.5	12.6	12.7
E	5.2	5.3	5.4
e	–	1.27	–
HE	7.5	7.8	8.1
L	0.4	0.6	0.8
L1	–	1.25	–
y	–	–	0.1
θ	0°	–	8°
b2	–	0.76	–
e1	–	7.62	–
l2	1.27	–	–

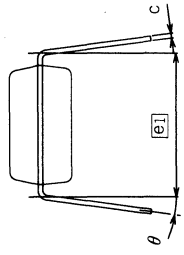
20P4

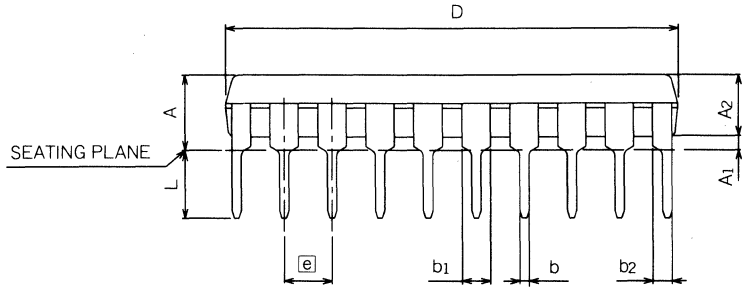
Plastic 20pin 300mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
*DIP020-P-0300	–	1.3

Scale : 2.5/1







Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	4.5
A1	0.51	–	–
A2	–	3.3	–
b	0.4	0.5	0.6
b1	1.4	1.5	1.8
b2	0.9	1.0	1.3
c	0.22	0.27	0.34
D	23.8	24.0	24.2
E	6.15	6.3	6.45
e	–	2.54	–
e1	–	7.62	–
L	3.0	–	–
θ	0°	–	15°

MITSUBISHI ELECTRIC

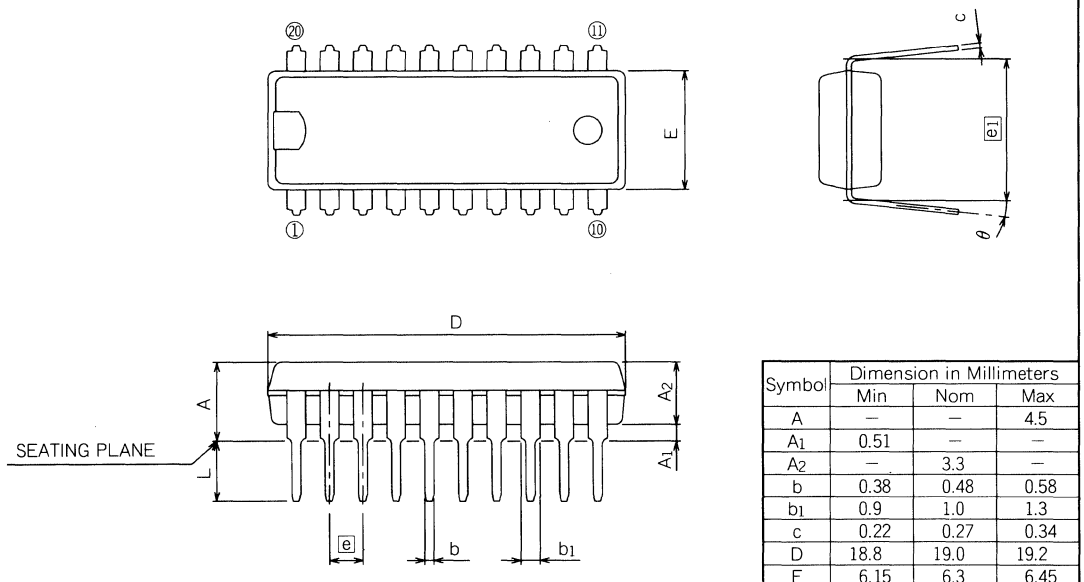
PACKAGE OUTLINES

20P4B

Plastic 20pin 300mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)
SDIP020-P-0300	—	1.0

Scale : 2.5/1



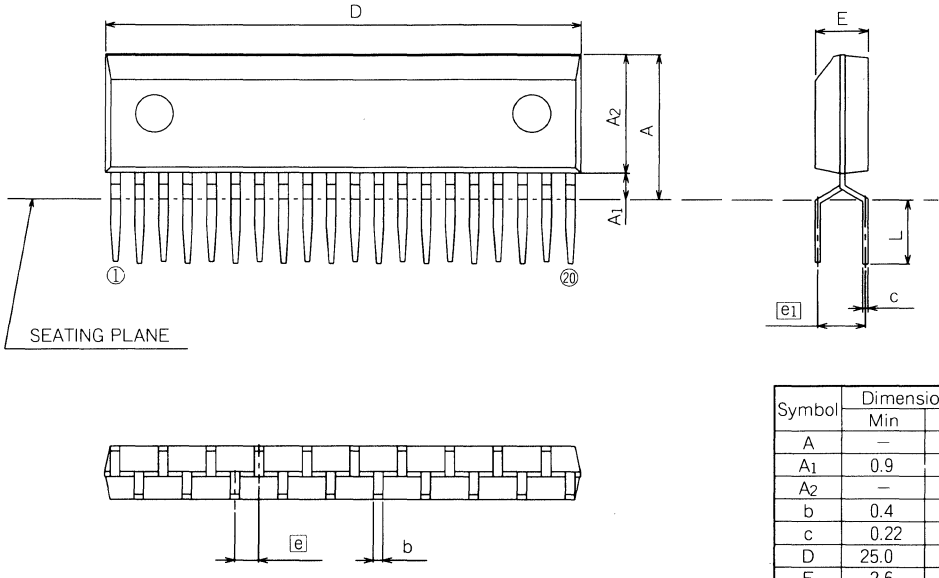
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b	0.38	0.48	0.58
b_1	0.9	1.0	1.3
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	6.15	6.3	6.45
e	—	1.778	—
e1	—	7.62	—
L	3.0	—	—
θ	0°	—	15°

20P5A

Plastic 20pin 325mil ZIP

EIAJ Package Code	JEDEC Code	Weight(g)
*ZIP014-P-0325	—	1.0

Scale : 2.5/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	8.3
A_1	0.9	—	—
A_2	—	6.3	—
b	0.4	0.5	0.6
c	0.22	0.27	0.34
D	25.0	25.2	25.4
E	2.6	2.8	3.0
e	—	1.27	—
e1	—	2.54	—
L	2.8	—	—

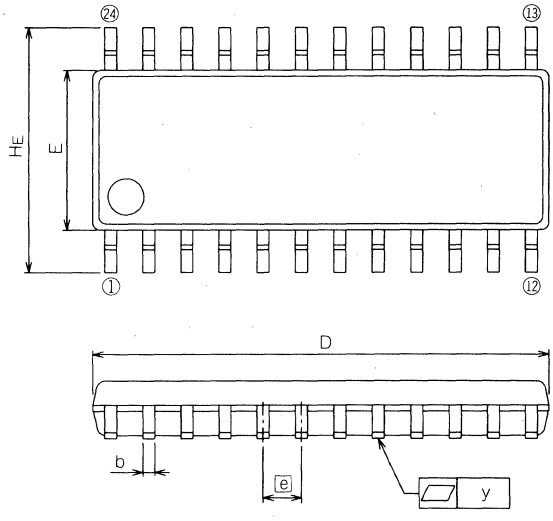
PACKAGE OUTLINES

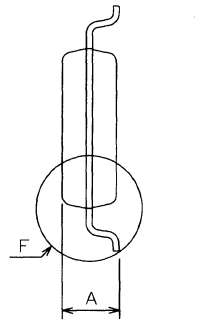
24P2N−B

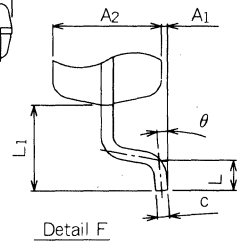
Plastic 24pin 300mil SOP

EIAJ Package Code	JEDEC Code	Weight(g)
*SOP024-P-0300	—	

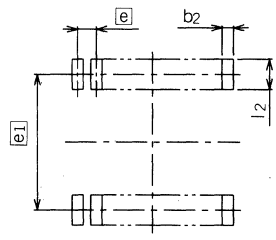
Scale : 4/1







Detail F



Recommended Mount Pad

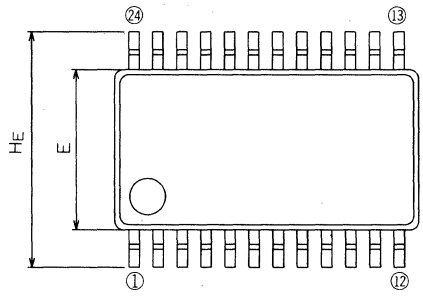
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.1
A_1	0	0.1	0.2
A_2	—	1.8	—
b	0.35	0.4	0.5
c	0.18	0.2	0.25
D	14.92	15.02	15.12
E	5.2	5.3	5.4
e	—	1.27	—
H_E	7.82	8.12	8.42
L	0.3	0.5	0.7
L_1	—	1.41	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.76	—
e1	—	7.62	—
l_2	1.27	—	—

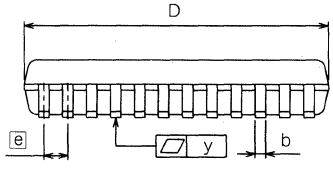
24P2Q−A

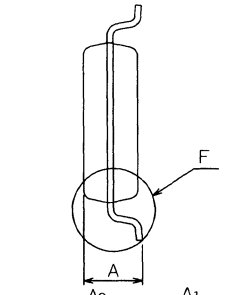
Plastic 24pin 300mil SSOP

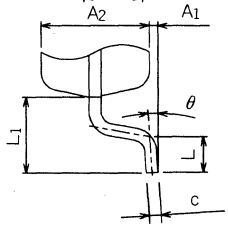
EIAJ Package Code	JEDEC Code	Weight(g)
SSOP024-P-0300	—	0.2

Scale : 4/1

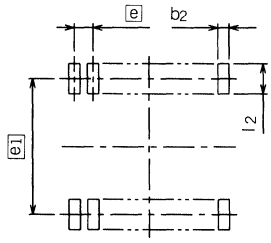








Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.1
A_1	0	0.1	0.2
A_2	—	1.8	—
b	0.3	0.35	0.45
c	0.18	0.2	0.25
D	10.0	10.1	10.2
E	5.2	5.3	5.4
e	—	0.8	—
H_E	7.5	7.8	8.1
L	0.4	0.6	0.8
L_1	—	1.25	—
y	—	—	0.1
θ	0°	—	8°
b_2	—	0.5	—
e1	—	7.62	—
l_2	1.27	—	—

MITSUBISHI ELECTRIC

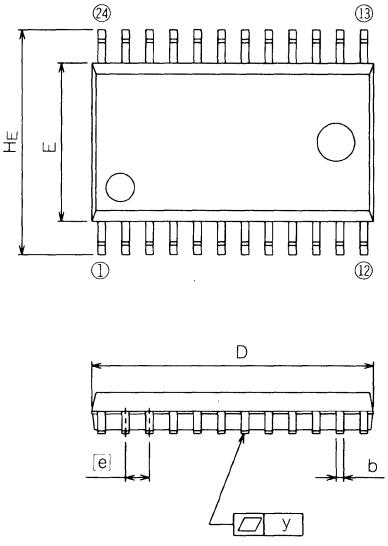
PACKAGE OUTLINES

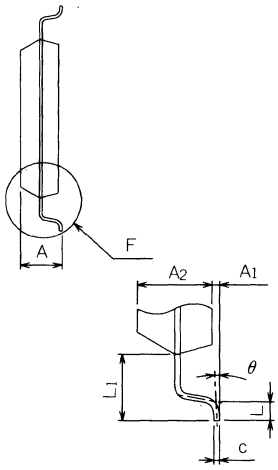
24P2W-A

Plastic 24pin 450mil SOP

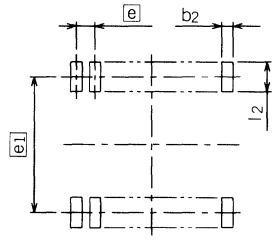
EIAJ Package Code	JEDEC Code	Weight(g)
*SOP024-P-0450	–	0.5

Scale : 2.5/1





Detail F



Recommended Mount Pad

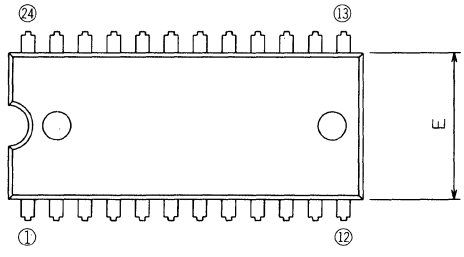
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A_1	0.05	–	–
A_2	–	2.0	–
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	14.8	15.0	15.2
E	8.2	8.4	8.6
e	–	1.27	–
H_E	11.63	11.93	12.23
L	0.3	0.5	0.7
L_1	–	1.765	–
y	–	–	0.15
θ	0°	–	10°
b_2	–	0.76	–
e1	–	11.43	–
l_2	1.27	–	–

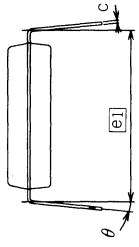
24P4

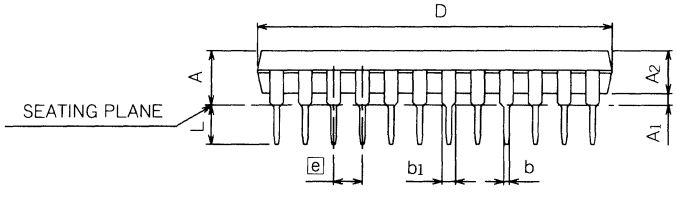
Plastic 24pin 600mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
*DIP024-P-0600	–	3.3

Scale : 1.5/1







Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.5
A_1	0.51	–	–
A_2	–	3.8	–
b	0.4	0.5	0.6
b_1	1.1	1.2	1.5
c	0.22	0.27	0.34
D	30.9	31.1	31.3
E	12.85	13.0	13.15
e	–	2.54	–
e1	–	15.24	–
L	3.0	–	–
θ	0°	–	15°

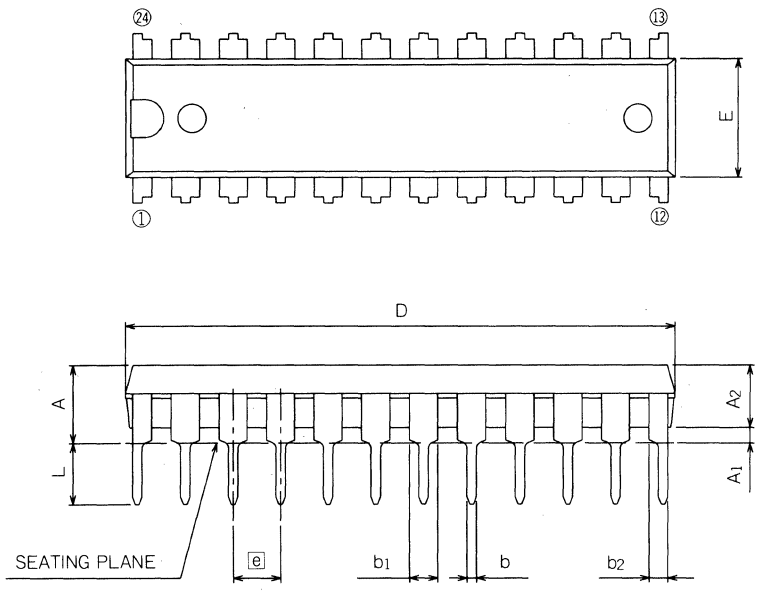
PACKAGE OUTLINES

24P4D

Plastic 24pin 300mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
*DIP024-P-0300	–	1.6

Scale : 2.5/1



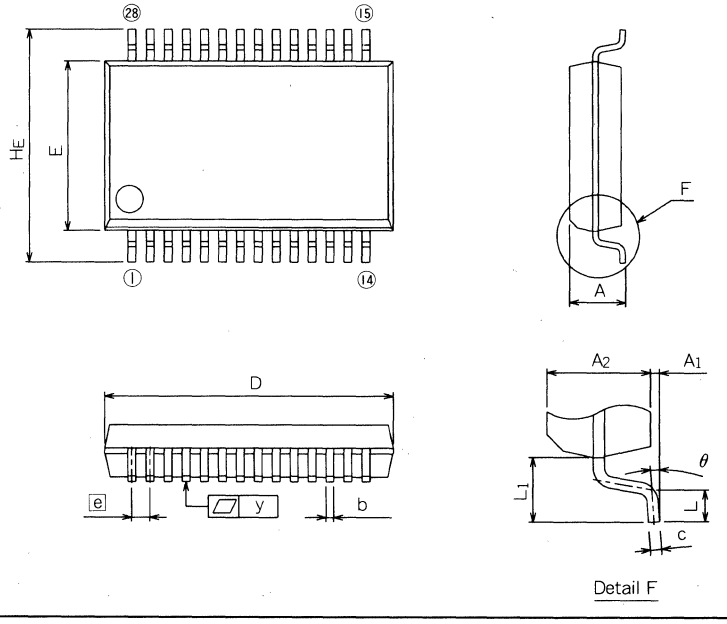
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	4.5
A_1	0.51	–	–
A_2	–	3.3	–
b	0.4	0.5	0.6
b_1	1.4	1.5	1.8
b_2	0.9	1.0	1.3
c	0.22	0.27	0.34
D	29.0	29.2	29.4
E	6.15	6.3	6.45
e	–	2.54	–
e_1	–	7.62	–
L	3.0	–	–
θ	0°	–	15°

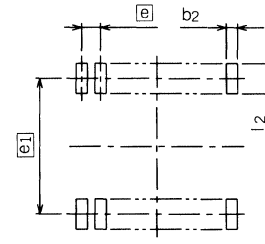
28P2U-A

Plastic 28pin 375mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)
SSOP028-P-0375	–	0.48

Scale : 3/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.65
A_1	0.1	0.2	0.3
A_2	–	2.3	–
b	0.3	0.35	0.45
c	0.23	0.25	0.3
D	12.7	12.8	12.9
E	7.4	7.5	7.6
e	–	0.8	–
H_E	10.0	10.3	10.6
L	0.5	0.7	0.9
L_1	–	1.4	–
y	–	–	0.1
θ	0°	–	8°
b_2	–	0.5	–
e_1	–	9.53	–
l_2	1.27	–	–

MITSUBISHI ELECTRIC

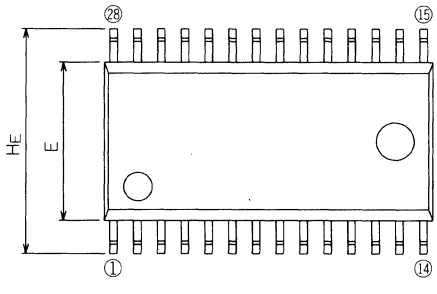
PACKAGE OUTLINES

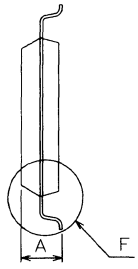
28P2W-A

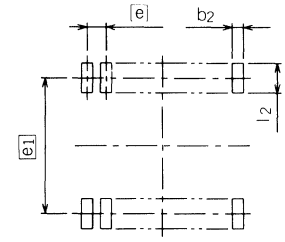
Plastic 28pin 450mil SOP

EIAJ Package Code	JEDEC Code	Weight(g)
*SOP028-P-0450	–	0.58

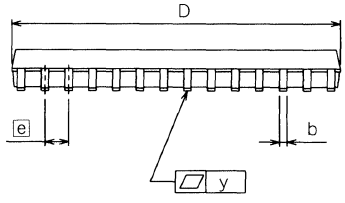
Scale : 2.5/1

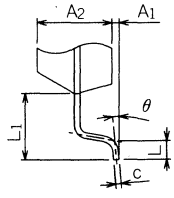






Recommended Mount Pad





Detail F

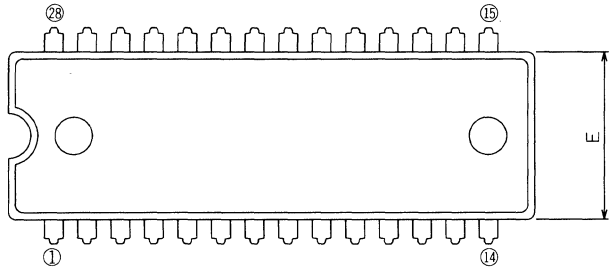
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A1	0.05	–	–
A2	–	2.0	–
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	–	1.27	–
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	–	1.765	–
y	–	–	0.15
θ	0°	–	10°
b2	–	0.76	–
e1	–	11.43	–
l2	1.27	–	–

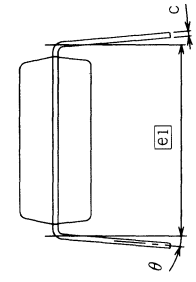
28P4B

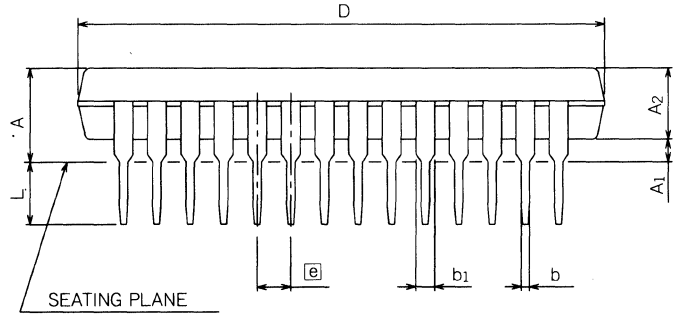
Plastic 28pin 400mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)
SDIP028-P-0400	–	2.2

Scale : 2.5/1







Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.08
A1	0.51	–	–
A2	–	3.8	–
b	0.35	0.45	0.55
b1	0.9	1.0	1.3
c	0.22	0.27	0.34
D	27.8	28.0	28.2
E	8.75	8.9	9.05
e	–	1.778	–
e1	–	10.16	–
L	3.0	–	–
θ	0°	–	15°

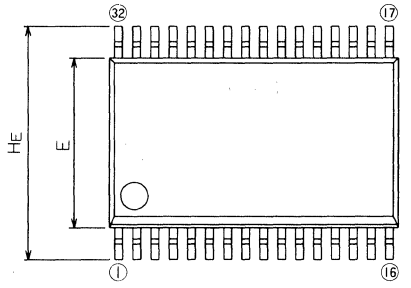
PACKAGE OUTLINES

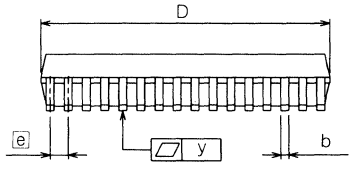
32P2U-B

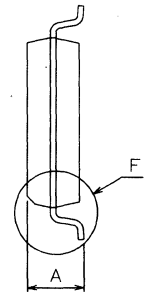
Plastic 32pin 375mil SSOP

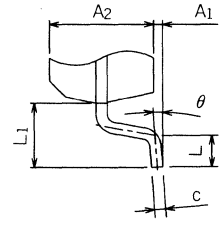
EIAJ Package Code	JEDEC Code	Weight(g)
SSOP032-P-0375	—	0.51

Scale : 3/1

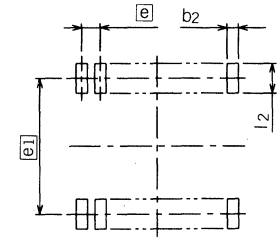








Detail F



Recommended Mount Pad

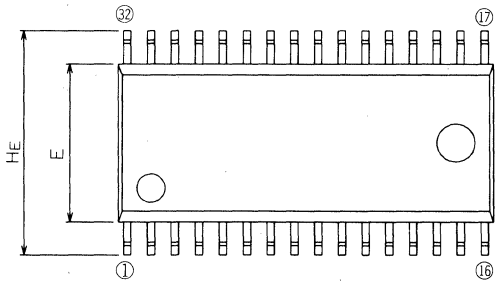
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.55
A1	0	0.1	0.2
A2	—	2.3	—
b	0.3	0.35	0.45
c	0.23	0.25	0.3
D	12.7	12.8	12.9
E	7.4	7.5	7.6
e	—	0.8	—
HE	10.0	10.3	10.6
L	0.5	0.7	0.9
L1	—	1.4	—
y	—	—	0.1
θ	0°	—	8°
b2	—	0.5	—
e1	—	9.53	—
l2	1.27	—	—

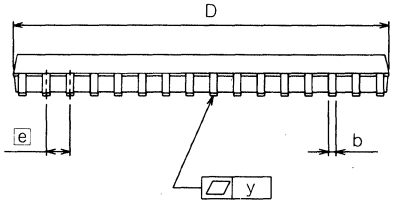
32P2W-A

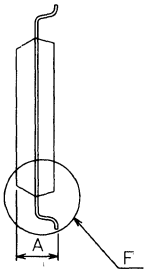
Plastic 32pin 450mil SOP

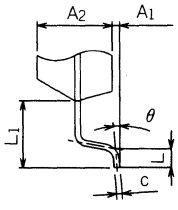
EIAJ Package Code	JEDEC Code	Weight(g)
*SOP032-P-0450	—	0.67

Scale : 2.5/1

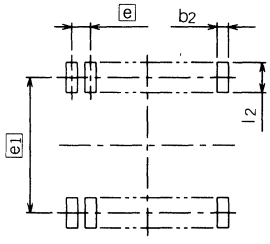








Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.4
A1	0.05	—	—
A2	—	2.0	—
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	19.8	20.0	20.2
E	8.2	8.4	8.6
e	—	1.27	—
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	—	1.765	—
y	—	—	0.15
θ	0°	—	10°
b2	—	0.76	—
e1	—	11.43	—
l2	1.27	—	—

MITSUBISHI ELECTRIC

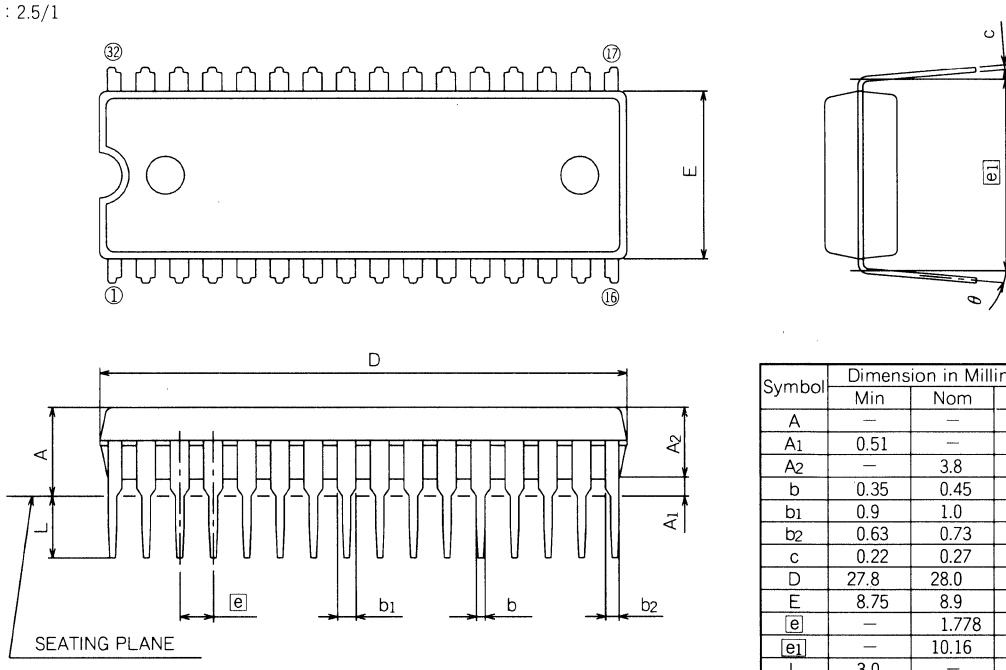
PACKAGE OUTLINES

32P4B

Plastic 32pin 400mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)
SDIP032-P-0400	—	2.2

Scale : 2.5/1



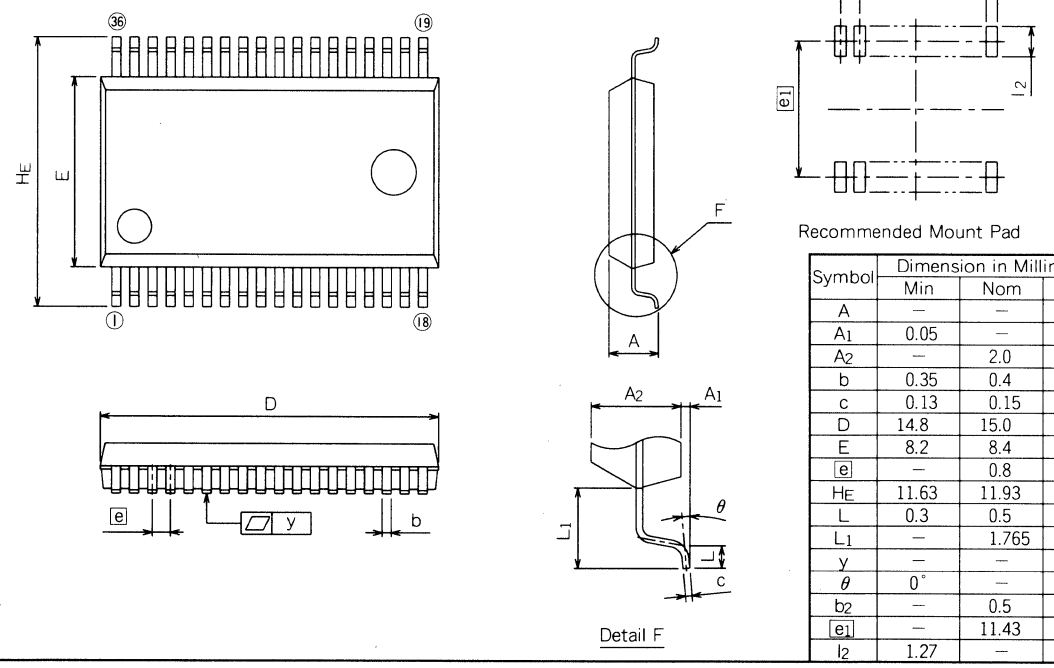
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	5.08
A_1	0.51	—	—
A_2	—	3.8	—
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	27.8	28.0	28.2
E	8.75	8.9	9.05
e	—	1.778	—
e_1	—	10.16	—
L	3.0	—	—
θ	0°	—	15°

36P2R−A

Plastic 36pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)
SSOP036-P-0450	—	0.53

Scale : 3/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.4
A_1	0.05	—	—
A_2	—	2.0	—
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	14.8	15.0	15.2
E	8.2	8.4	8.6
e	—	0.8	—
H_E	11.63	11.93	12.23
L	0.3	0.5	0.7
L_1	—	1.765	—
y	—	—	0.15
θ	0°	—	10°
b_2	—	0.5	—
e_1	—	11.43	—
l_2	1.27	—	—

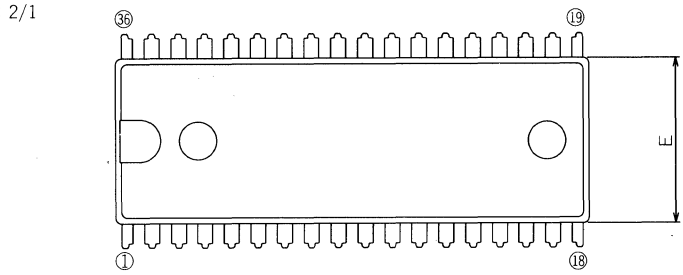
PACKAGE OUTLINES

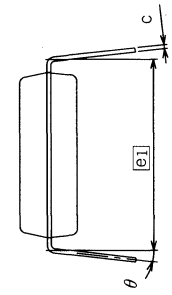
36P4E

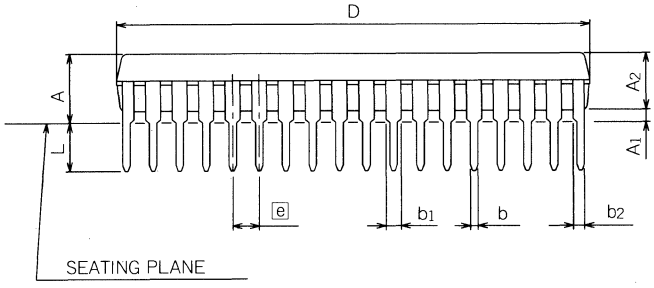
Plastic 36pin 500mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)
SDIP036-P-0500	—	3.0

Scale : 2/1







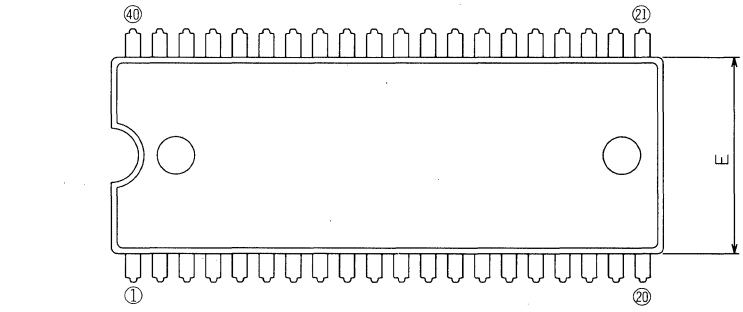
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	5.08
A_1	0.51	—	—
A_2	—	3.8	—
b	0.4	0.5	0.6
b_1	0.9	1.0	1.3
b_2	0.65	0.75	1.05
c	0.22	0.27	0.34
D	31.3	31.5	31.7
E	10.85	11.0	11.15
e	—	1.778	—
e_1	—	12.7	—
L	3.0	—	—
θ	0°	—	15°

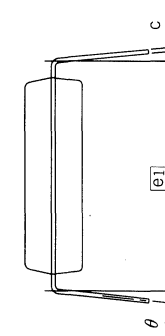
40P4B

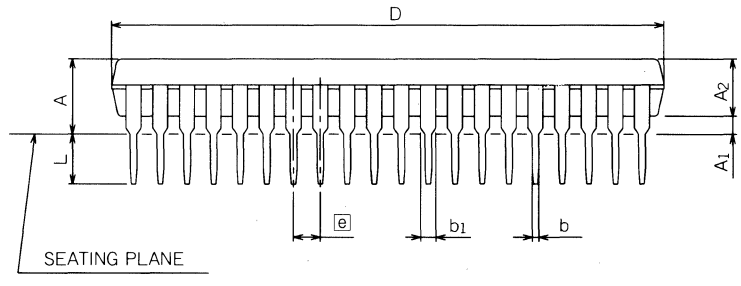
Plastic 40pin 600mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)
SDIP040-P-0600	—	4.1

Scale : 2/1







Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	5.5
A_1	0.51	—	—
A_2	—	3.8	—
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
c	0.22	0.27	0.34
D	36.5	36.7	36.9
E	12.85	13.0	13.15
e	—	1.778	—
e_1	—	15.24	—
L	3.0	—	—
θ	0°	—	15°

MITSUBISHI ELECTRIC

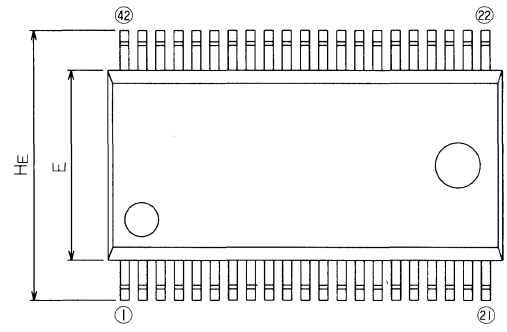
PACKAGE OUTLINES

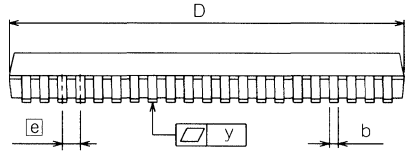
42P2R−A

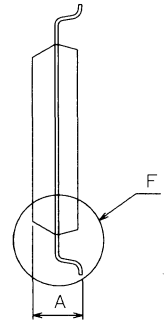
Plastic 42pin 450mil SSOP

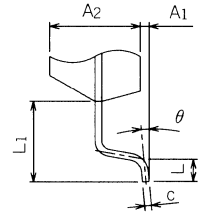
EIAJ Package Code	JEDEC Code	Weight(g)
SSOP042-P-0450	—	0.63

Scale : 3/1

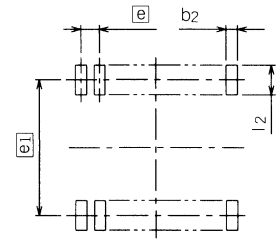








Detail F



Recommended Mount Pad

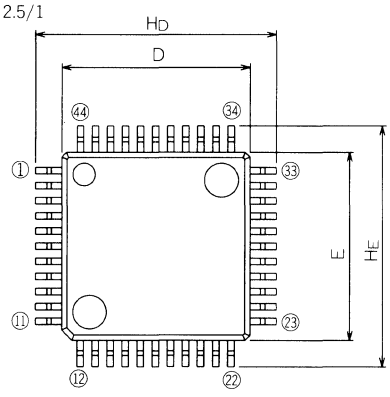
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.4
A1	0.05	—	—
A2	—	2.0	—
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	—	0.8	—
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	—	1.765	—
y	—	—	0.15
θ	0°	—	10°
b2	—	0.5	—
e1	—	11.43	—
l2	1.27	—	—

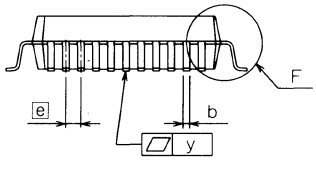
44P6N−A

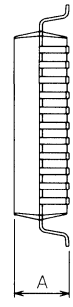
Plastic 44pin 10×10mm body QFP

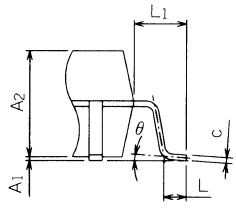
EIAJ Package Code	JEDEC Code	Weight(g)
*QFP044-P-1010	—	0.59

Scale : 2.5/1

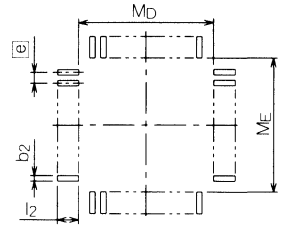








Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A1	0	0.1	0.2
A2	—	2.8	—
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	9.8	10.0	10.2
E	9.8	10.0	10.2
e	—	0.8	—
HD	12.5	12.8	13.1
HE	12.5	12.8	13.1
L	0.4	0.6	0.8
L1	—	1.4	—
y	—	—	0.1
θ	0	—	10
b2	—	0.5	—
l2	1.3	—	—
MD	—	10.6	—
ME	—	10.6	—

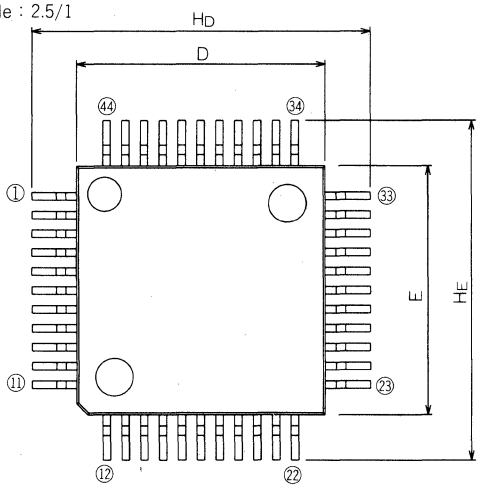
PACKAGE OUTLINES

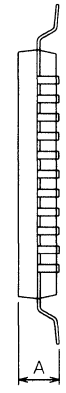
44P6W-B

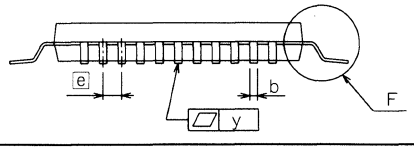
Plastic 44pin 13.2×13.2mm body QFP

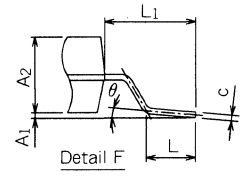
EIAJ Package Code	JEDEC Code	Weight(g)
—	—	0.76

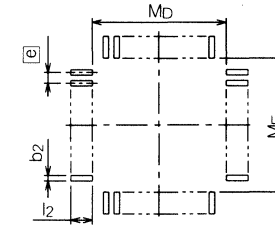
Scale : 2.5/1











Recommended Mount Pad

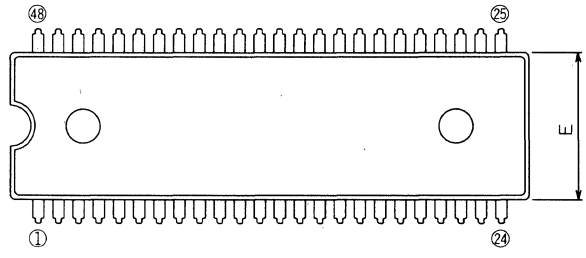
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.45
A_1	0.05	—	—
A_2	—	2.0	—
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	13.0	13.2	13.4
E	13.0	13.2	13.4
e	—	1.0	—
H_D	17.7	18.0	18.3
H_E	17.7	18.0	18.3
L	1.1	1.3	1.5
L_1	—	2.4	—
y	—	—	0.15
θ	0°	—	10°
b_2	—	0.7	—
l_2	2.0	—	—
M_D	—	14.4	—
M_E	—	14.4	—

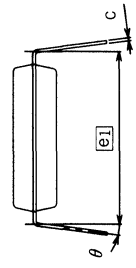
48P4B

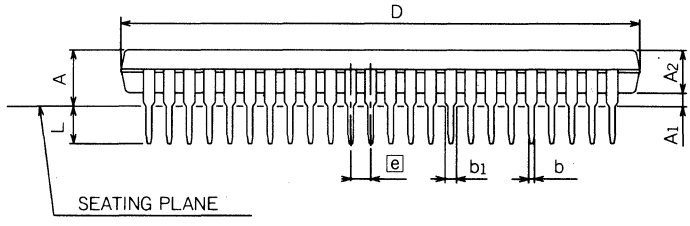
Plastic 48pin 600mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)
SDIP048-P-0600	—	5.1

Scale : 1.5/1







Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	5.5
A_1	0.51	—	—
A_2	—	3.8	—
b	0.4	0.5	0.6
b_1	0.9	1.0	1.3
c	0.22	0.27	0.34
D	45.65	45.85	46.05
E	12.85	13.0	13.15
e	—	1.778	—
e1	—	15.24	—
L	3.0	—	—
θ	0°	—	15°

MITSUBISHI ELECTRIC

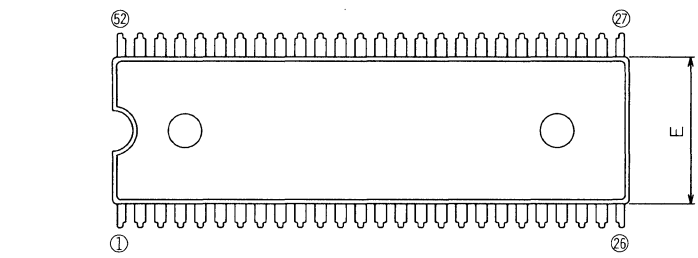
PACKAGE OUTLINES

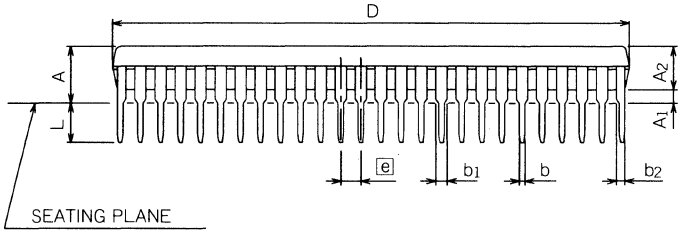
52P4B

Plastic 52pin 600mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)
SDIP052-P-0600	—	5.1

Scale : 1.5/1





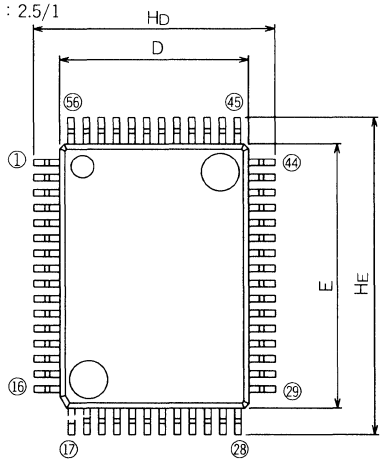
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	5.5
A_1	0.51	—	—
A_2	—	3.8	—
b	0.4	0.5	0.6
b_1	0.9	1.0	1.3
b_2	0.65	0.75	1.05
c	0.22	0.27	0.34
D	45.65	45.85	46.05
E	12.85	13.0	13.15
e	—	1.778	—
e1	—	15.24	—
L	3.0	—	—
θ	0°	—	15°

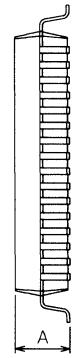
56P6N-A

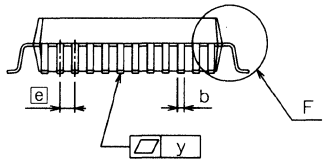
Plastic 56pin 10×14mm body QFP

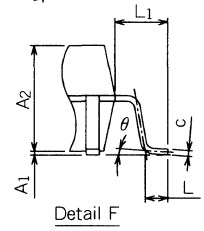
EIAJ Package Code	JEDEC Code	Weight(g)
*QFP056-P-1014	—	0.79

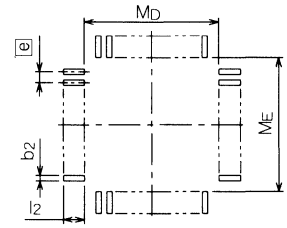
Scale : 2.5/1











Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A_1	0	0.1	0.2
A_2	—	2.8	—
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	9.8	10.0	10.2
E	13.8	14.0	14.2
e	—	0.8	—
HD	12.5	12.8	13.1
HE	16.5	16.8	17.1
L	0.4	0.6	0.8
L1	—	1.4	—
y	—	—	0.1
θ	0°	—	10°
b2	—	0.5	—
l2	1.3	—	—
MD	—	10.6	—
ME	—	14.6	—

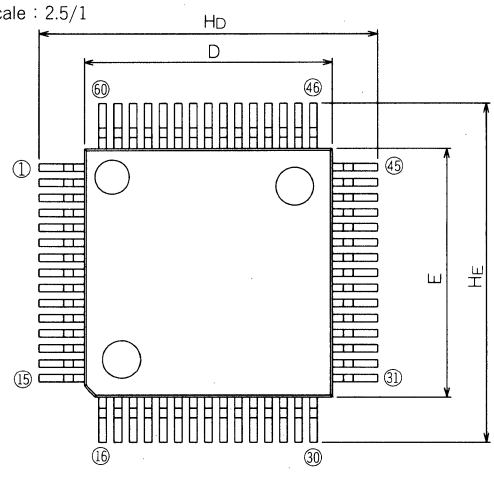
PACKAGE OUTLINES

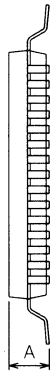
60P6-B

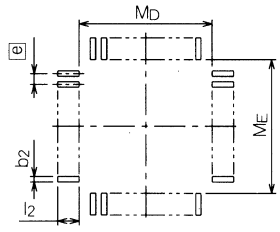
Plastic 60pin 13.2×13.2mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)
—	—	0.76

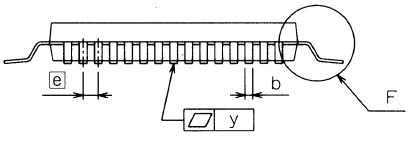
Scale : 2.5/1

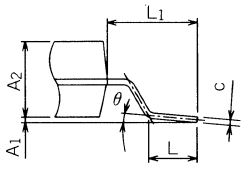






Recommended Mount Pad





Detail F

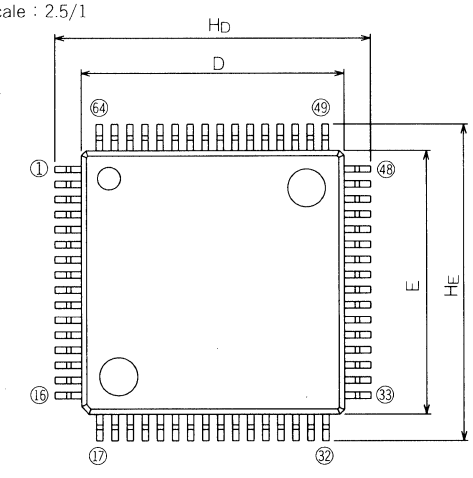
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.45
A_1	0.05	—	—
A_2	—	2.0	—
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	13.0	13.2	13.4
E	13.0	13.2	13.4
e	—	0.8	—
H_D	17.7	18.0	18.3
H_E	17.7	18.0	18.3
L	1.1	1.3	1.5
L_1	—	2.4	—
y	—	—	0.15
θ	0°	—	10°
b_2	—	0.5	—
l_2	2.0	—	—
M_D	—	14.4	—
M_E	—	14.4	—

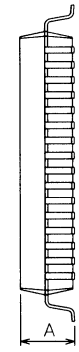
64P6N-A

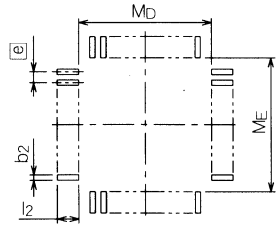
Plastic 64pin 14×14mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)
*QFP064-P-1414	—	1.11

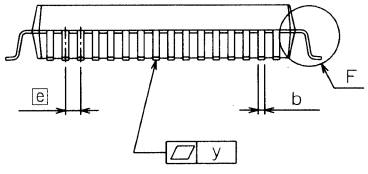
Scale : 2.5/1

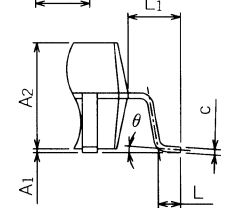






Recommended Mount Pad





Detail F

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A_1	0	0.1	0.2
A_2	—	2.8	—
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	13.8	14.0	14.2
e	—	0.8	—
H_D	16.5	16.8	17.1
H_E	16.5	16.8	17.1
L	0.4	0.6	0.8
L_1	—	1.4	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.5	—
l_2	1.3	—	—
M_D	—	14.6	—
M_E	—	14.6	—

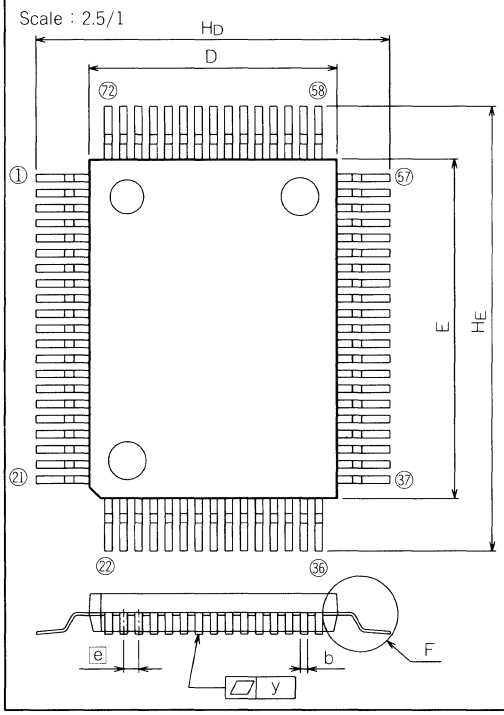
MITSUBISHI ELECTRIC

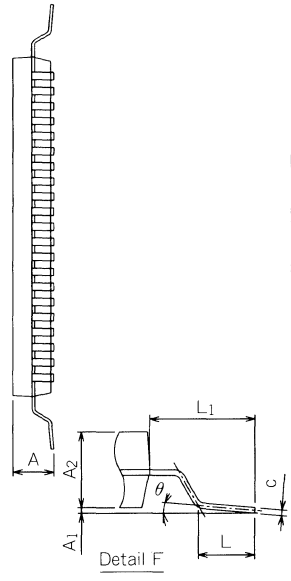
PACKAGE OUTLINES

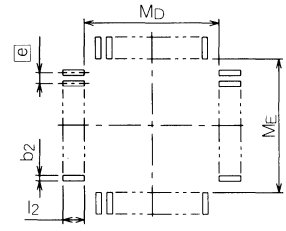
72P6-B

Plastic 72pin 13.2×18mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)
—	—	1.06







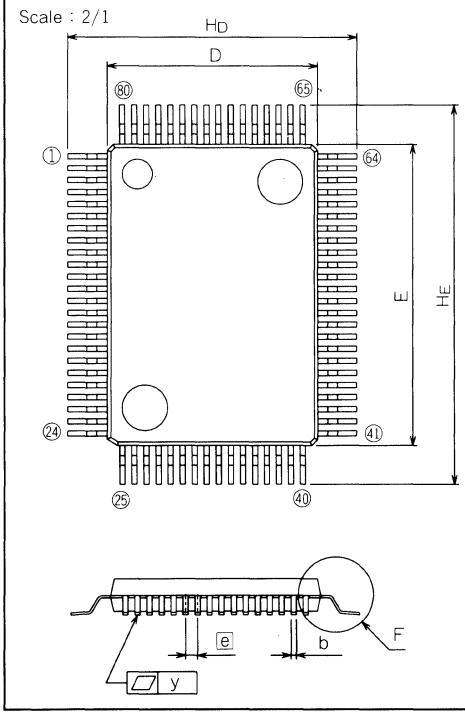
Recommended Mount Pad

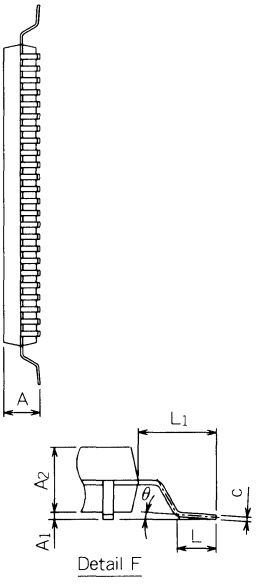
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.45
A_1	0.05	—	—
A_2	—	2.0	—
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	13.0	13.2	13.4
E	17.8	18.0	18.2
e	—	0.8	—
H_D	18.5	18.8	19.1
H_E	23.3	23.6	23.9
L	1.3	1.5	1.7
L_1	—	2.8	—
y	—	—	0.15
θ	0°	—	10°
b_2	—	0.5	—
l_2	2.2	—	—
M_D	—	14.8	—
M_E	—	19.6	—

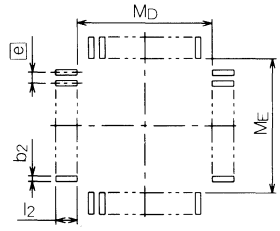
80P6-B

Plastic 80pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)
*QFP080-P-1420	—	1.28







Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.6
A_1	0.05	—	—
A_2	—	2.15	—
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	—	0.8	—
H_D	18.9	19.2	19.5
H_E	24.9	25.2	25.5
L	1.1	1.3	1.5
L_1	—	2.6	—
y	—	—	0.15
θ	0°	—	10°
b_2	—	0.5	—
l_2	2.0	—	—
M_D	—	15.6	—
M_E	—	21.6	—

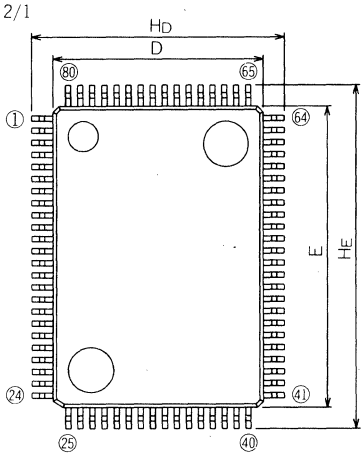
PACKAGE OUTLINES

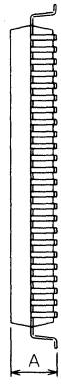
80P6N-A

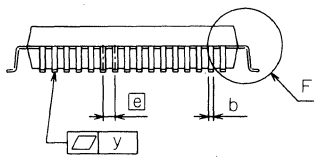
Plastic 80pin 14×20mm body QFP

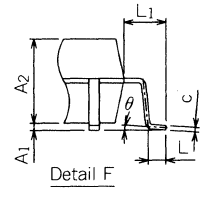
EIAJ Package Code	JEDEC Code	Weight(g)
*QFP080-P-1420	–	1.58

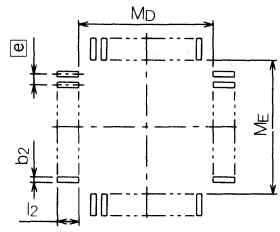
Scale : 2/1











Recommended Mount Pad

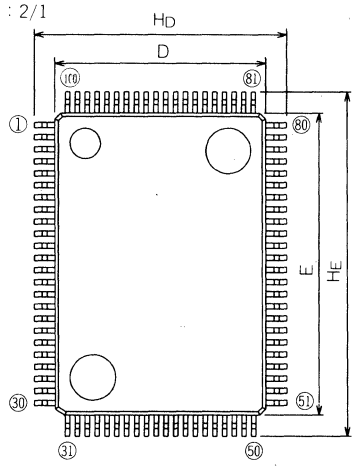
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A_1	0	0.1	0.2
A_2	–	2.8	–
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.8	–
H_D	16.5	16.8	17.1
H_E	22.5	22.8	23.1
L	0.4	0.6	0.8
L_1	–	1.4	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.5	–
l_2	1.3	–	–
M_D	–	14.6	–
M_E	–	20.6	–

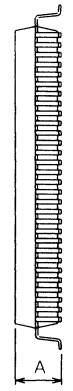
100P6S-A

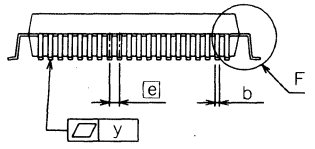
Plastic 100pin 14×20mm body QFP

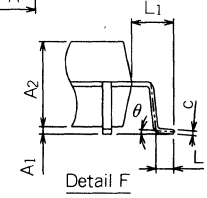
EIAJ Package Code	JEDEC Code	Weight(g)
*QFP100-P-1420	–	1.58

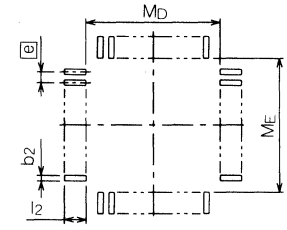
Scale : 2/1











Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A_1	0	0.1	0.2
A_2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
H_D	16.5	16.8	17.1
H_E	22.5	22.8	23.1
L	0.4	0.6	0.8
L_1	–	1.4	–
y	–	–	0.1
θ	0	–	10
b_2	–	0.35	–
l_2	1.3	–	–
M_D	–	14.6	–
M_E	–	20.6	–

MITSUBISHI ELECTRIC

KARAOKE PROCESSOR (ECHO, KEY CONTROLLER)

2

M65830AP,AFP

DIGITAL ECHO (DIGITAL DELAY)

DESCRIPTION

The M65830 CMOS IC is used to add echoes to karaoke * singing.

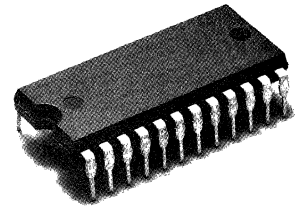
It is optimal to provide the echo effect function for karaoke players, such as radio cassette recorders, mini audio components and television sets.

This IC can be used in digital surround systems because it generates a highly precise short delay when equipped with an improved master clock function.

* Karaoke : Recorded music to accompany live singing

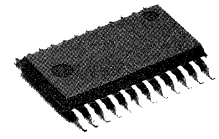
FEATURES

- Delay time can be variable in four lengths between 81.9 msec and 131.1msec
- Delay time is set with 2-bit parallel data
- Built-in A-D, D-A converters, input/output low-pass filter, and 16K bit delay memory
- High sound quality is assured by simple system construction, due to A-D, D-A converters with ADM (Adaptive Delta Modulation) system
  - Output noise voltage : − 80dBV (typ)
  - Total harmonic distortion : 1.2% (typ)
- Built-in mute circuit



Outline 24P4(AP)

2.54mm pitch 600mil DIP
(13.0mm × 31.1mm × 3.8mm)



Outline 24P2W-A(AFP)

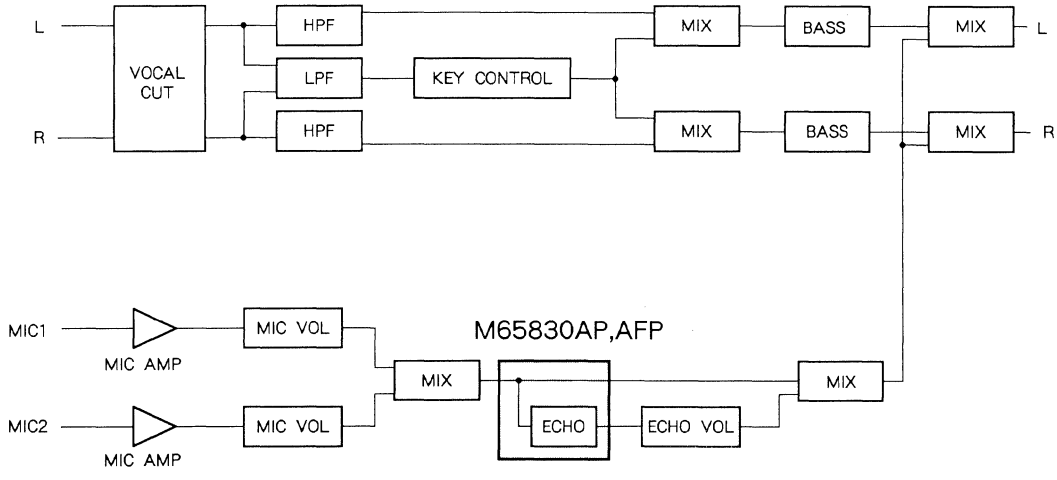
1.27mm pitch 450mil SOP
(8.4mm × 15.0mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

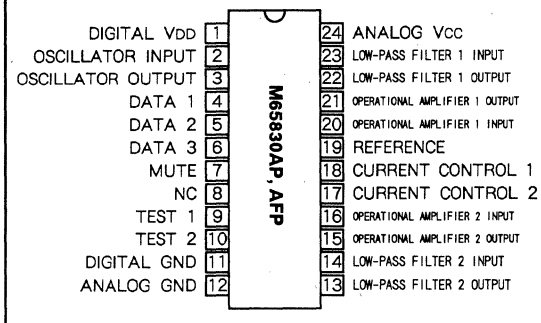
Supply voltage range ····· V_{CC}, V_{DD} = 4.5~5.5V

Rated supply voltage ····· V_{CC}, V_{DD} = 5V

SYSTEM CONFIGURATION

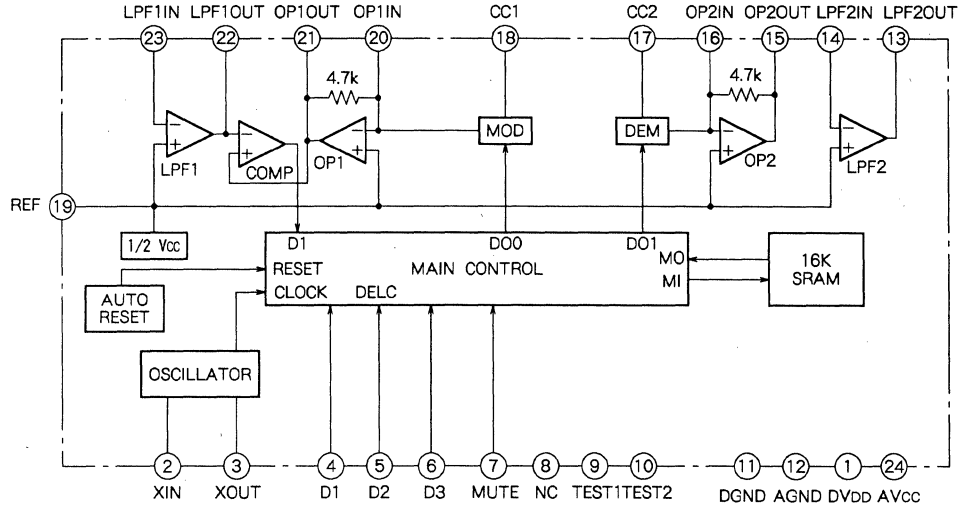


PIN CONFIGURATION



Outline 24P4(AP)
24P2W-A(AFP)
NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Name	I/O	Function
①	V_{DD}	Digital power supply	–	
②	X_{IN}	Oscillator input	I	Ceramic oscillator or external clock is connected
③	X_{OUT}	Oscillator output	O	Ceramic oscillator is connected Set to open when external clock is used
④	D1	Data 1	I	Delay time setting data 1 is input
⑤	D2	Data 2	I	Delay time setting data 2 is input
⑥	D3	Data 3	I	Delay time setting data 3 is input Normally set to "L"
⑦	MUTE	Mute	I	Mute control L = Mute
⑧	NC	No connection	–	No external connection
⑨	TEST1	Test 1	I	Normally set to "L"
⑩	TEST2	Test 2	I	Normally set to "L"
⑪	D GND	Digital GND	–	
⑫	A GND	Analog GND	–	
⑬	LPF2 OUT	Low-pass filter 2 output	O	Forms output low-pass filter with external capacitor and resistor
⑭	LPF2 IN	Low-pass filter 2 input	I	
⑮	OP2 OUT	Operational amplifier 2 output	O	Forms demodulating integrator with external capacitor
⑯	OP2 IN	Operational amplifier 2 input	I	
⑰	CC2	Current control 2	–	Demodulator ADM control
⑱	CC1	Current control 1	–	Modulator ADM control
⑲	REF	Reference	–	Analog reference voltage = 1/2Vcc
⑳	OP1 IN	Operational amplifier 1 input	I	Forms modulating integrator with external capacitor and resistor
㉑	OP1 OUT	Operational amplifier 1 output	O	
㉒	LPF1 OUT	Low-pass filter 1 output	O	Forms input low-pass filter with external capacitor and resistor
㉓	LPF1 IN	Low-pass filter 1 input	I	
㉔	Vcc	Analog power supply	–	

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{CC}	Supply voltage		6.5	V
I_{CC}	Circuit current		100	mA
P_d	Power dissipation	M65830AP	1	W
		M65830AFP	0.8	
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−40∼+125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Analog supply voltage		4.5	5	5.5	V
V_{DD}	Digital supply voltage		4.5	5	5.5	V
V_{CC}-V_{DD}	Potential difference V_{CC}, V_{DD}		−0.3	0	0.3	V
f_{ck}	Clock frequency		450	500	550	kHz
V_{IH}	Input voltage ("H" level)		0.7V_{DD}	–	V_{DD}	V
V_{IL}	Input voltage ("L" level)		0	–	0.3V_{DD}	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, f = 1kHz, V_i = 100mVrms, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	No signals	5	13	35	mA
Gv	Voltage gain between input and output	R_L = 47k Ω	−3.5	−0.5	2.5	dB
V_{Omax}	Maximum output voltage	THD = 10%	0.7	1	–	Vrms
THD	Total harmonic distortion	30kHz LPF	–	1.2	3.0	%
No	Output noise voltage	DIN−AUDIO	–	−85	−70	dBV
SVRR	Power suppression ratio	△Vcc = −20dBV, f = 100Hz	–	−40	−25	dB

FUNCTION

(1) Sampling frequency fs

Sampling frequency is obtained with the following formula :

fs = 1/4 Clock frequency(Hz)

When clock frequency fck is 500kHz, sampling frequency is :

fs = 1/4 × 500kHz = 125kHz

(2) Delay time Td

Delay time can be varied in four lengths by using pin ④D1 and ⑤D2.

(Condition : fs = 125kHz)

④D1	⑤D2	Delay time(msec)
H	H	81.9
L	H	98.3
H	L	114.7
L	L	131.1

(3) Mute

Output can be muted depending on the status of MUTE pin ⑦

⑦MUTE	Mode
H	Normal mode
L	Mute mode

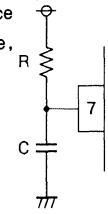
We recommend that, to prevent noise during power supply, output be muted by connection as shown in the diagram. The muting time is determined depending on the resistance and capacitance. The relationship between muting time, capacitance (C) and resistance (R) is as shown below :

Muting time(t mute) ≒ 0.92 × CR(sec)

When capacitance is 10 μF and resistance is 150kΩ :

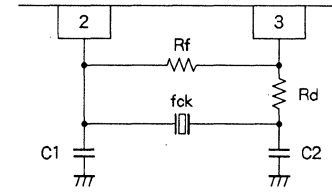
t mute ≒ 0.92 × 10 μ × 150k = 1.38(sec)

Mute time is approximately 1.4 seconds.



(4) Oscillation circuit

M65830AP,AFP has a built-in oscillation buffer. An oscillation circuit can be formed by connecting the ceramic oscillator to resistors and capacitors as shown below :



When frequency fck = 500kHz(Clock CSB500E by Murata Mfg. Co., Ltd. FCR500K3 by TDK Co., Ltd.), we recommend that resistance and capacitance be applied as follows :

Rf = 1MΩ

Rd = 3.3kΩ

$C_1 = C_2$ = 330pF

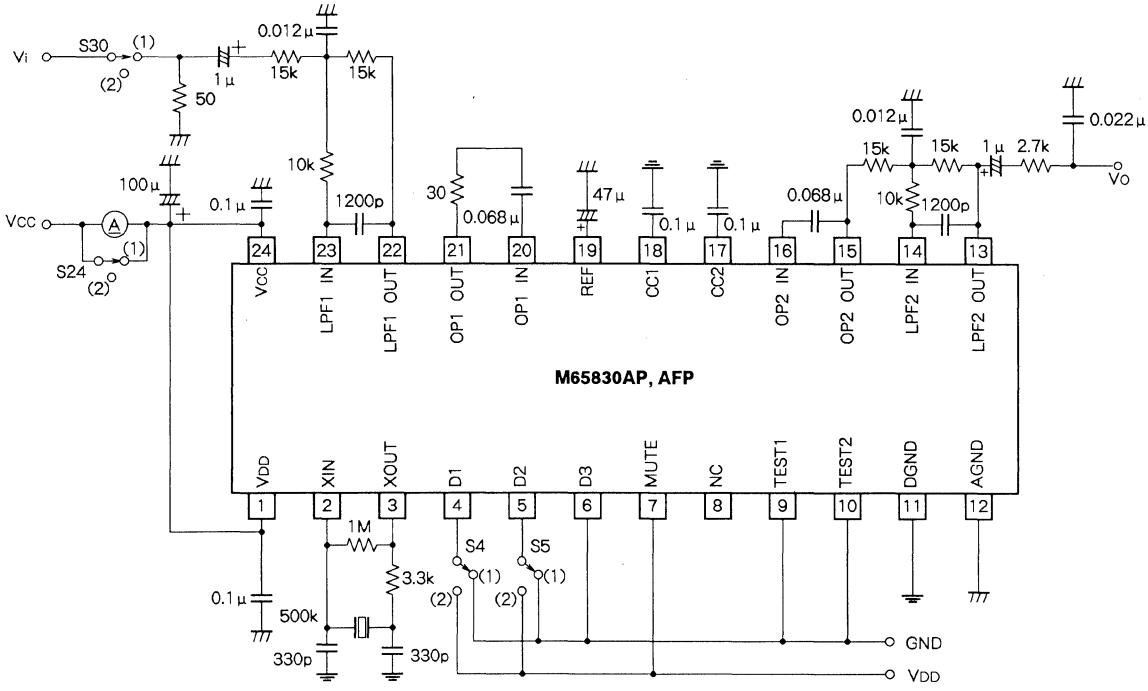
Please note that resistance and capacitance are different depending on the oscillator's manufacturer and frequency, as well as the environment where the oscillation circuit is used (e.g. the capacity of the circuit board and wiring).

TEST CONDITIONS

Symbol	Parameter	S4	S5	S24	S30	Remark
I_{CC}	Circuit current	×	×	2	2	No signals
G_V	Voltage gain	×	×	1	1	$G_V = 20\log(V_O/V_I)$
T_{d1}	Delay time	2	2	1	1	Refer to (2)
T_{d2}		1	2	1	1	
T_{d3}		2	1	1	1	
T_{d4}		1	1	1	1	
V_{omax}	Maximum output voltage	×	×	1	1	30kHz LPF, THD = 10%
THD	Total harmonic distortion	×	×	1	1	30kHz LPF
N_O	Output noise voltage	×	×	1	1	DIN AUDIO, V_I = 0mVrms
SVRR	Power suppression ratio	×	×	1	2	ΔV_{CC} = − 20dBV, f = 100Hz

×···1 or 2

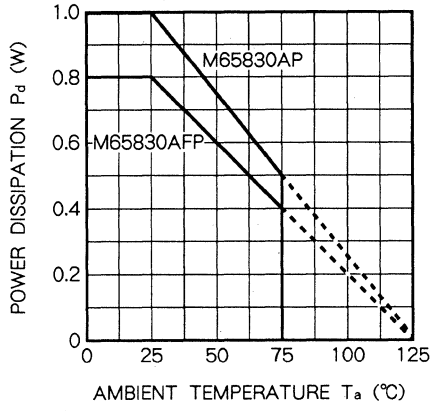
TEST CIRCUIT



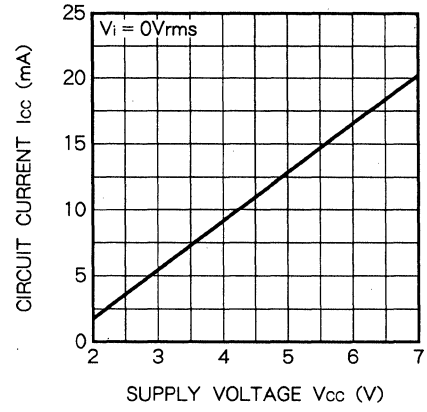
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

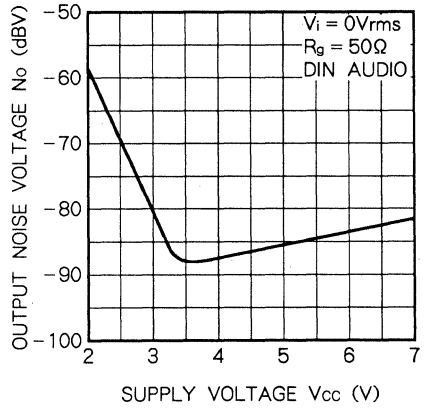
THERMAL DERATING (MAXIMUM RATING)



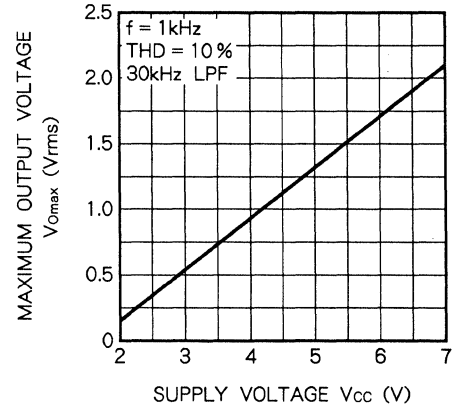
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



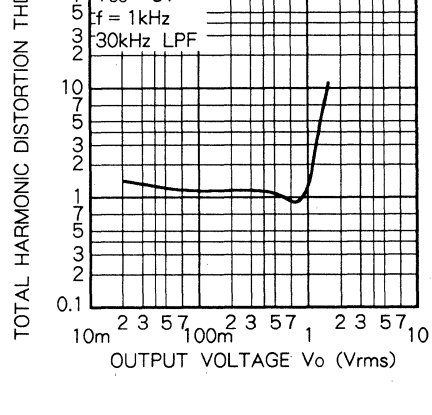
OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



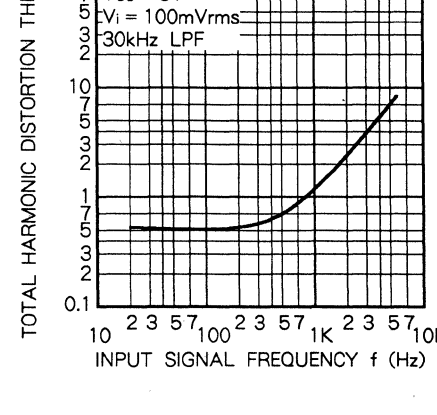
MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



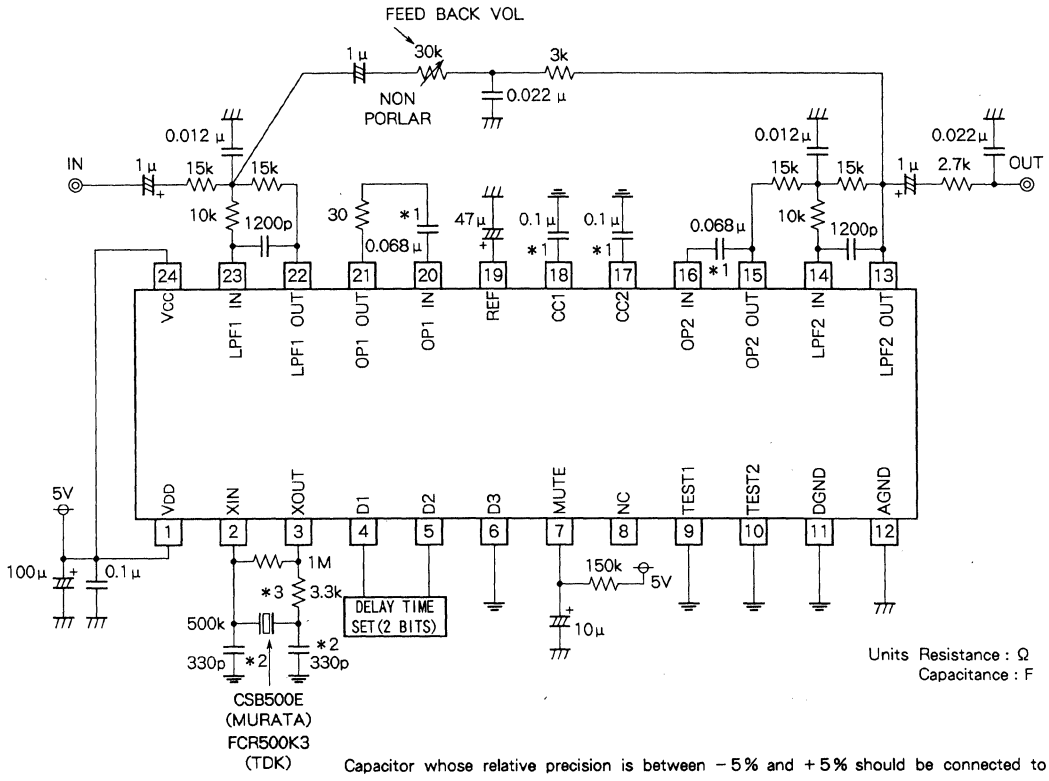
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL FREQUENCY



APPLICATION EXAMPLE



Capacitor whose relative precision is between −5% and +5% should be connected to *1

Capacitors at *2 and resistors at *3 should be selected depending on the frequency of the ceramic oscillator and the environment where the oscillation circuit is used

M65831P,FP

DIGITAL ECHO (DIGITAL DELAY)

DESCRIPTION

The M65831 is an IC developed for producing echo effects added to voice signals picked up by microphone for karaoke applications.

The IC has the largest memory among the digital delay series. As it's design is aimed at high performance, it is best suited to provide radio cassette tape recorders and miniature unit audio systems with quality echo function.

Being pin compatible with the M65830AP, AFP and M65843P, FP, the M65831P, FP is suitable for upgrading the series.

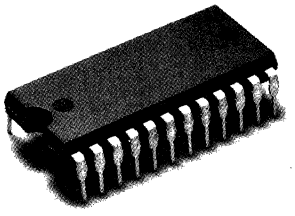
FEATURES

- Built-in input/output filters, A-D and D-A converters, and memory realize a delay system with only a single chip
- Capable of composing low-noise and low-distortion delay system at low cost by ADM system
  (No = – 92dB typ, THD = 0.5% typ)
- Control mode selections available from 2 kinds : easy mode using parallel data and microcomputer mode using serial data
- Sleep mode can be selected to stop IC functions
- Built-in automatic reset circuit

RECOMMENDED OPERATING CONDITIONS

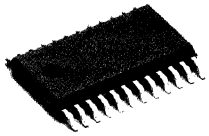
Supply voltage range ····· V_{CC}, V_{DD} = 4.5~5.5V

Rated supply voltage ····· V_{CC}, V_{DD} = 5.0V



Outline 24P4(P)

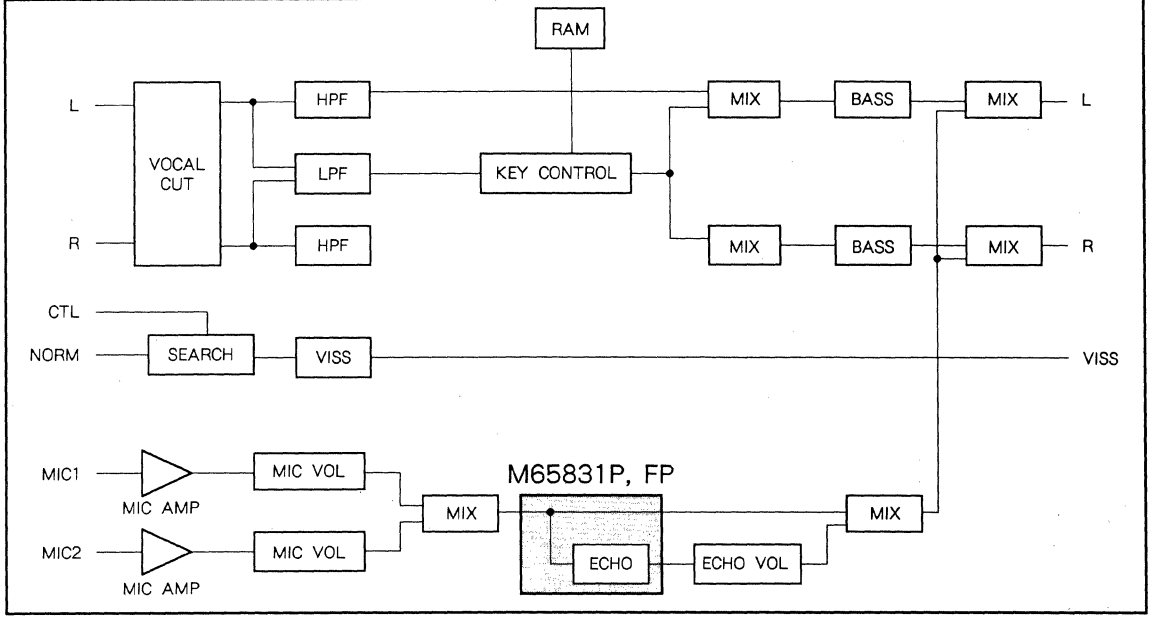
2.54mm pitch 600mil DIP
(13.0mm × 31.1mm × 3.8mm)



Outline 24P2W-A(FP)

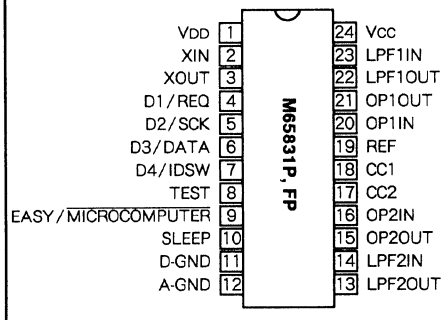
1.27mm pitch 450mil SOP
(8.4mm × 15.0mm × 2.0mm)

SYSTEM CONFIGURATION



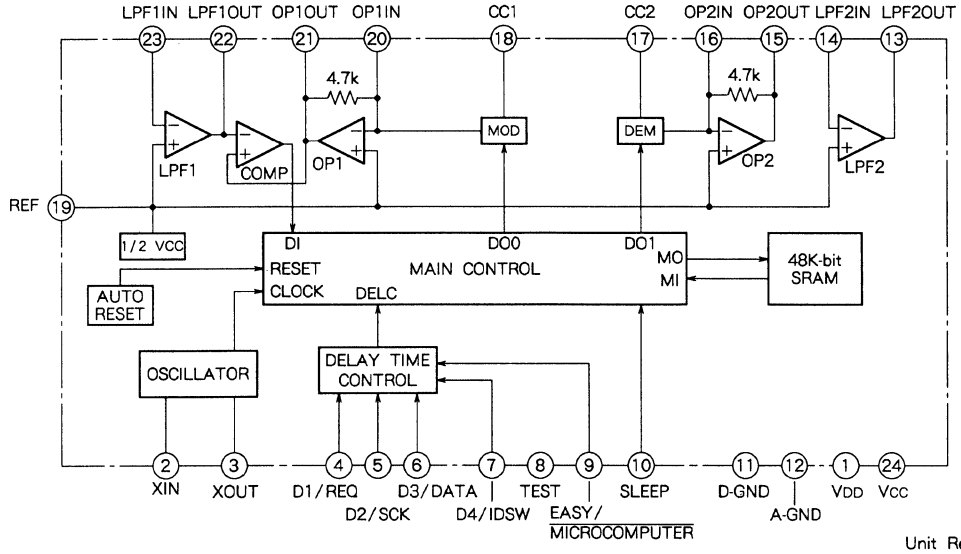
MITSUBISHI ELECTRIC

PIN CONFIGURATION



Outline 24P4(P)
24P2W-A(FP)

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

PIN DESCRIPTION

Pin No.	Symbol	Name	I/O	Function
①	V_{DD}	Digital V_{DD}	–	Supply voltage
②	X_{IN}	Oscillator input	I	Connects to 2MHz ceramic filter or inputs an external clock
③	X_{OUT}	Oscillator output	O	Connects to 2MHz ceramic filter
④	D1/REQ	Delay1/Request	I	Easy mode : inputs D1 data Microcomputer mode : inputs request data
⑤	D2/SCK	Delay2/Shift clock	I	Easy mode : inputs D2 data Microcomputer mode : inputs shift clock
⑥	D3/DATA	Delay3/Serial data	I	Easy mode : inputs D3 data Microcomputer mode : inputs serial data
⑦	D4/IDSW	Delay4/ID switch	I	Easy mode : inputs D4 data Microcomputer mode : controls ID code
⑧	TEST	Test	I	L = normal mode
⑨	EASY/$\overline{\text{Microcomputer}}$	Easy/$\overline{\text{Microcomputer}}$	I	H = easy mode L = Microcomputer mode
⑩	SLEEP	Sleep	I	H = sleep mode L = normal mode
⑪	D GND	Digital GND	–	Connects to analog GND at one point
⑫	A GND	Analog GND	–	Connects to analog GND
⑬	LPF2 OUT	Low pass filter2 output	O	Forms low pass filter with external C,R
⑭	LPF2 IN	Low pass filter2 input	I	
⑮	OP2 OUT	OP-AMP2 output	O	Forms integrator with external C,R
⑯	OP2 IN	OP-AMP2 input	I	
⑰	CC2	Current control 2	–	
⑱	CC1	Current control 1	–	
⑲	REF	Reference	–	= 1/2Vcc
⑳	OP1 IN	OP-AMP1 input	I	Forms integrator with external C,R
㉑	OP1 OUT	OP-AMP1 output	O	
㉒	LPF1 OUT	Low pass filter1 output	O	Forms low pass filter with external C,R
㉓	LPF1 IN	Low pass filter1 input	I	
㉔	V_{CC}	Analog V_{CC}	–	Supply voltage

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		6.5	V
I_{CC}	Circuit current		100	mA
P_d	Power dissipation	M65831P	1	W
		M65831FP	650	mW
T_{opr}	Operating temperature		−20～+75	℃
T_{stg}	Storage temperature		−40～+125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
f_{ck}	Clock frequency		1	2	3	MHz
V_{IH}	High input voltage		0.7V_{DD}	−	V_{DD}	V
V_{IL}	Low input voltage		0	−	0.3V_{DD}	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, f = 1kHz, V_i = 100mVrms, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
I_{CC}	Circuit current			−	16.0	40.0	mA
Gv	Voltage gain	R_L = 47kΩ		−3.5	−0.5	2.5	dB
V_{Omax}	Maximum output voltage	THD = 10%		0.7	1	−	Vrms
THD	Output distortion	30kHz LPF	fs = 500kHz	−	0.3	1.0	%
			fs = 250kHz	−	0.5	1.5	
No	Output noise voltage	DIN−AUDIO (Low sampling)		−	−92	−75	dBV
SVRR	Supply voltage rejection ratio	V_{CC} = − 20dBV, f = 100Hz		−	−40	−25	dB
TMUTE	Mute time	Upon changing delay time		508	528	548	ms
		Upon cancelling sleep mode		508	528	548	
I_{CCS}	Circuit current (Sleep mode)	Sleep mode		−	12.0	30.0	mA

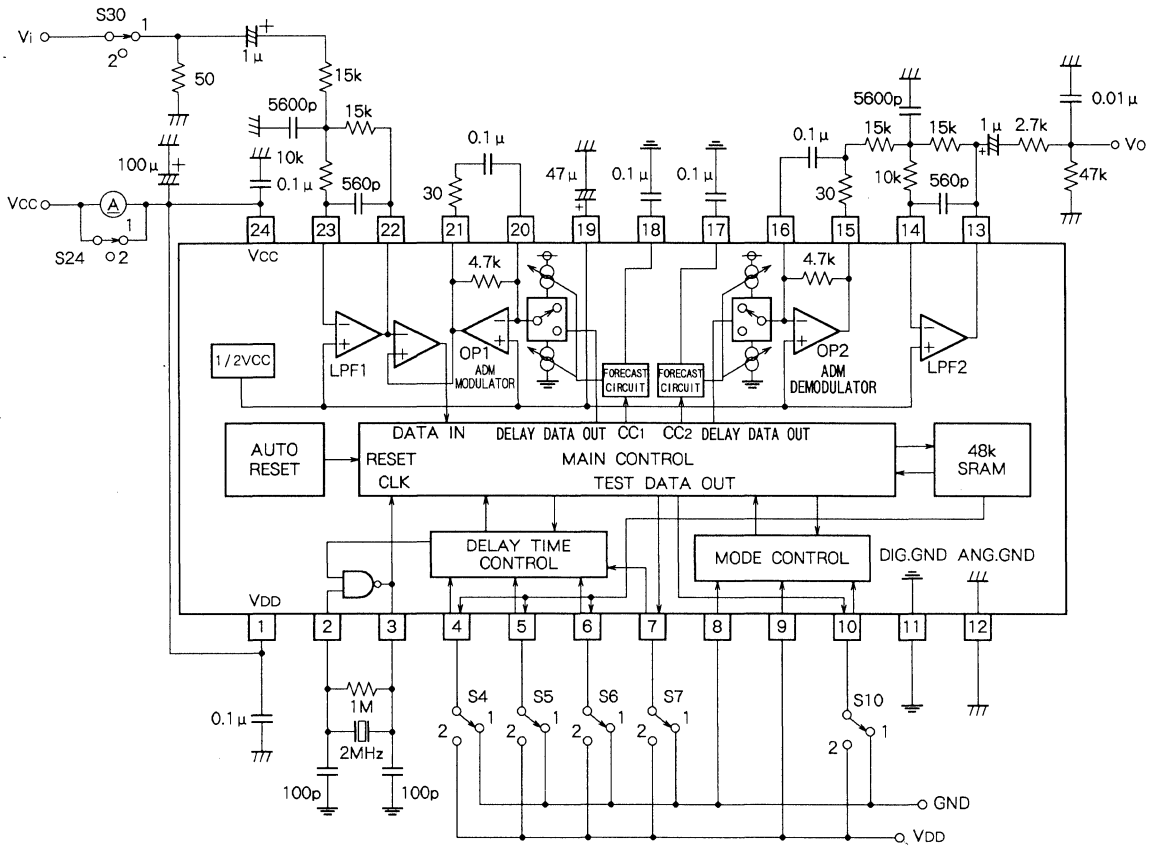
TEST CONDITION

SWITCH CONDITIONS

*···1 or 2

Symbol	Parameter	Sampling frequency	S 4	S 5	S 6	S 7	S 10	S 24	S 30	Remark
Icc	Circuit current	–	1	1	1	1	1	2	2	No signal
Gv1	Voltage gain	500kHz	*	*	*	1	1	1	1	Gv = 20log(Vo/Vi)
Gv2		250kHz	*	*	*	2	1	1	1	
Tda	Delay time	500kHz	1	1	1	1	1	1	1	
Tdb			2	1	1	1	↓	↓	↓	
Tdc			1	2	1	1	↓	↓	↓	
Tdd			2	2	1	1	↓	↓	↓	
Tde			1	1	2	1	↓	↓	↓	
Tdf			2	1	2	1	↓	↓	↓	
Tdg			1	2	2	1	↓	↓	↓	
Tdh			2	2	2	1	↓	↓	↓	
Tdi		250kHz	1	1	1	2	↓	↓	↓	
Tdj			2	1	1	2	↓	↓	↓	
Tdk			1	2	1	2	↓	↓	↓	
Tdl			2	2	1	2	↓	↓	↓	
Tdm			1	1	2	2	↓	↓	↓	
Tdn			2	1	2	2	↓	↓	↓	
Tdo			1	2	2	2	↓	↓	↓	
Tdp			2	2	2	2	1	1	1	
Vomax1	Maximum output voltage	500kHz	*	*	*	1	1	1	1	30kHz L. P. F THD = 10%
Vomax2		250kHz	*	*	*	2	1	1	1	
THD1	Total harmonic distortion	500kHz	*	*	*	1	1	1	1	30kHz L. P. F THD = 10%
THD2		250kHz	*	*	*	2	1	1	1	
No1	Output noise voltage	500kHz	*	*	*	1	1	1	2	DIN AUDIO Rg = 50 Ω Vi = 0mVrms
No2		250kHz	*	*	*	2	1	1	2	
SVRR	Supply voltage rejection ratio	–	*	*	*	*	1	1	2	△Vcc = – 20dBv, f = 100Hz
MUTE T	Mute time	–	2 ↓ 1	*	*	*	1	1	1	Upon changing delay time
MUTE S		–	*	*	*	*	2 ↓ 1	1	1	Upon cancelling sleep mode

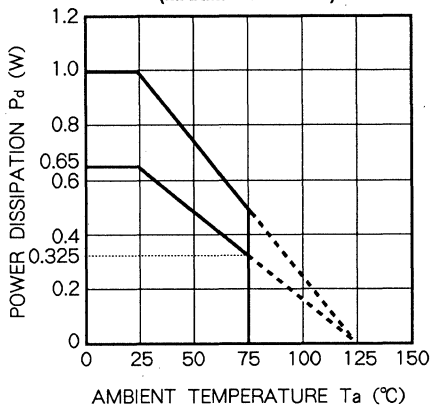
TEST CONDITION



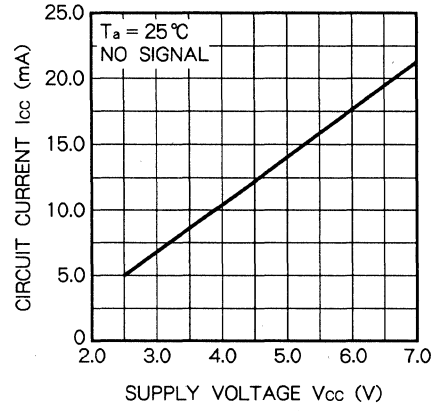
Units Resistance : Ω
Capacitance : F

TYPICAL CHARATERISTICS

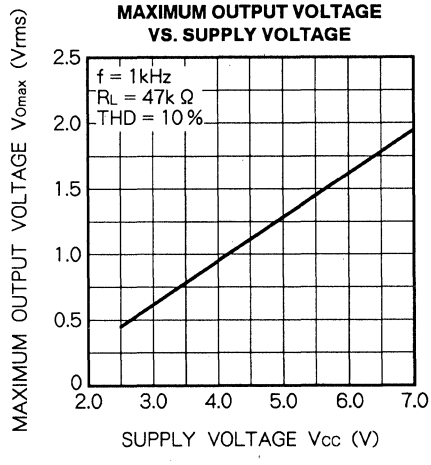
THERMAL DERATING
(MAXIMUM RATING)



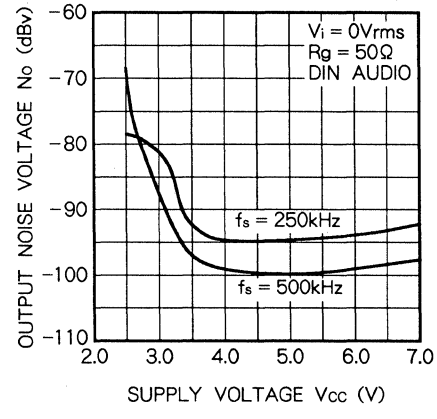
CIRCUIT CURRENT VS.
SUPPLY VOLTAGE



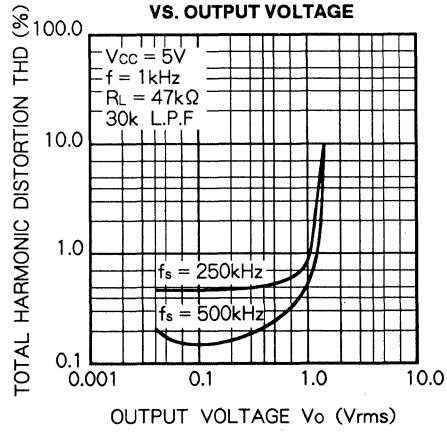
MAXIMUM OUTPUT VOLTAGE
VS. SUPPLY VOLTAGE



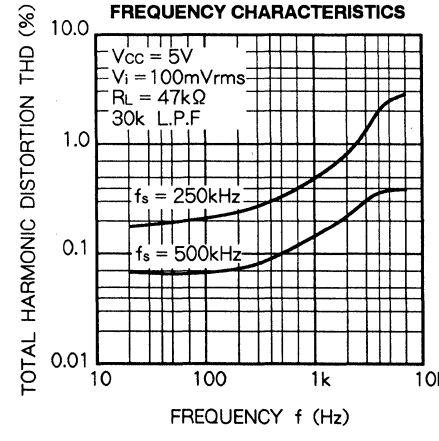
OUTPUT NOISE VOLTAGE
VS. SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION
VS. OUTPUT VOLTAGE



TOTAL HARMONIC DISTORTION VS.
FREQUENCY CHARACTERISTICS



OPERATION

1. DELAY TIME

D4	D3	D2	D1	fs	Td
L	L	L	L	500	12.3
			H		24.6
		H	L		36.9
			H		49.2
	H	L	L		61.4
			H		73.7
		H	L		86.0
			H		98.3
H	L	L	L	250	110.6
			H		122.9
		H	L		135.2
			H		147.5
	H	L	L		159.7
			H		172.0
		H	L		184.3
			H		196.6

fs = sampling frequency (kHz)
Td = delay time (msec)

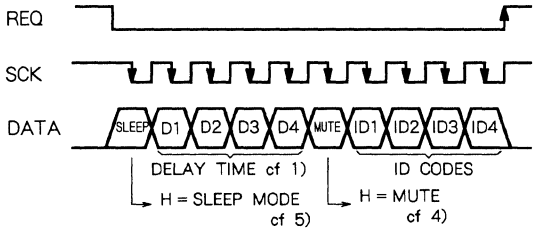
2. EASY MODE (EASY/$\overline{\text{Microcomputer}}$ = H)

D1, D2, D3, D4 and sleep are for easy mode

D1, D2, D3, D4 } delay time cf 1)

SLEEP cf 5)

3.MICROCOMPUTER MODE (EASY/$\overline{\text{Microcomputer}}$ = L)



TIMING DIAGRAM

This TIming chart shows that delay time is set by serial data from $\overline{\text{Microcomputer}}$.

DATA signal is latched at the falling edge of SCK signal, the last ten data are set at the rising edge of REQ signal when ID codes are satisfied.

* { ID1, ID3 : L
ID2 : H
ID4 : equal to IDSW

4. MUTING

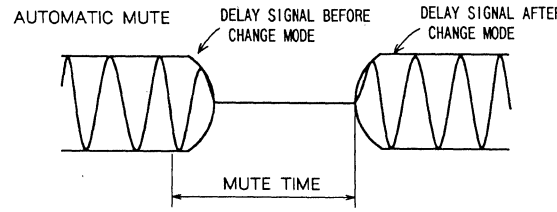
(1) Easy mode

Automatic mute upon changing delay time, cancelling SLEEP mode and power-on

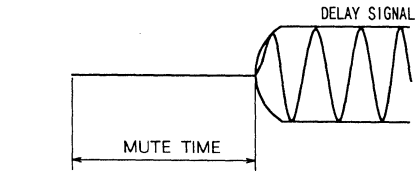
(2) Microcomputer mode

MUTE = H : mute

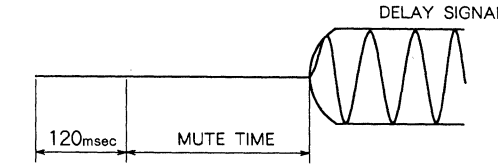
MUTE = L : automatic mute



(a) UPON CHANGING DELAY TIME



(b) UPON CANCELLING SLEEP MODE



(c) UPON POWER-ON

5. SLEEP MODE

Sleep data is

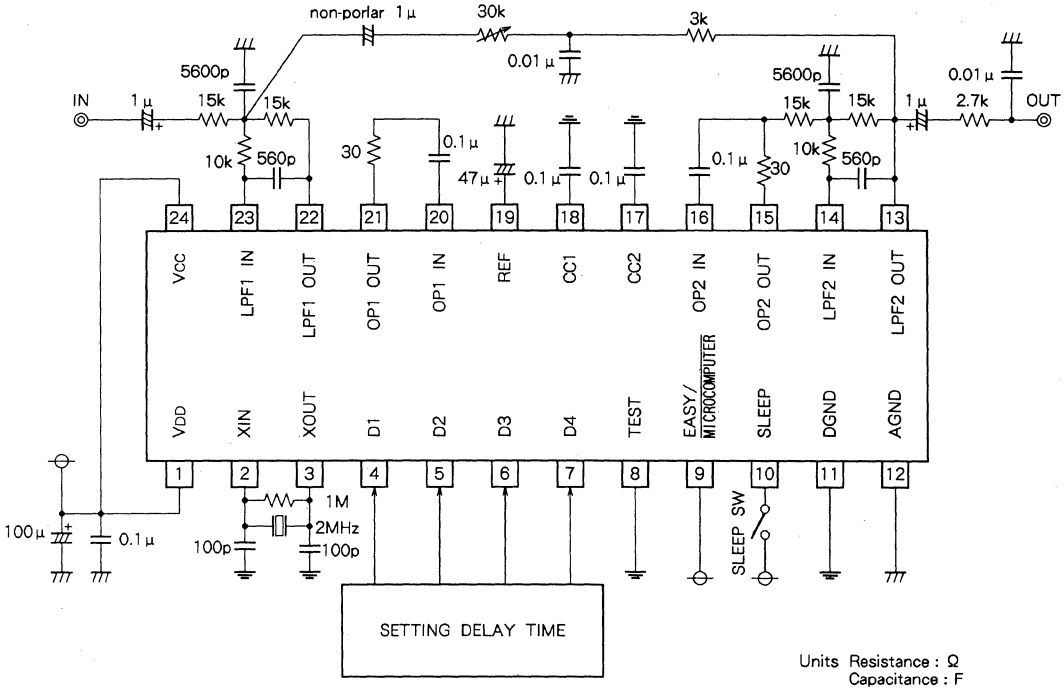
{ H : clock and RAM stop to reduce circuit current (sleep mode)
L : normal operation

6. SYSTEM RESET

Automaticaly reset power-on. The reset time is about 120msec. Delay time is set at 147.5msec.

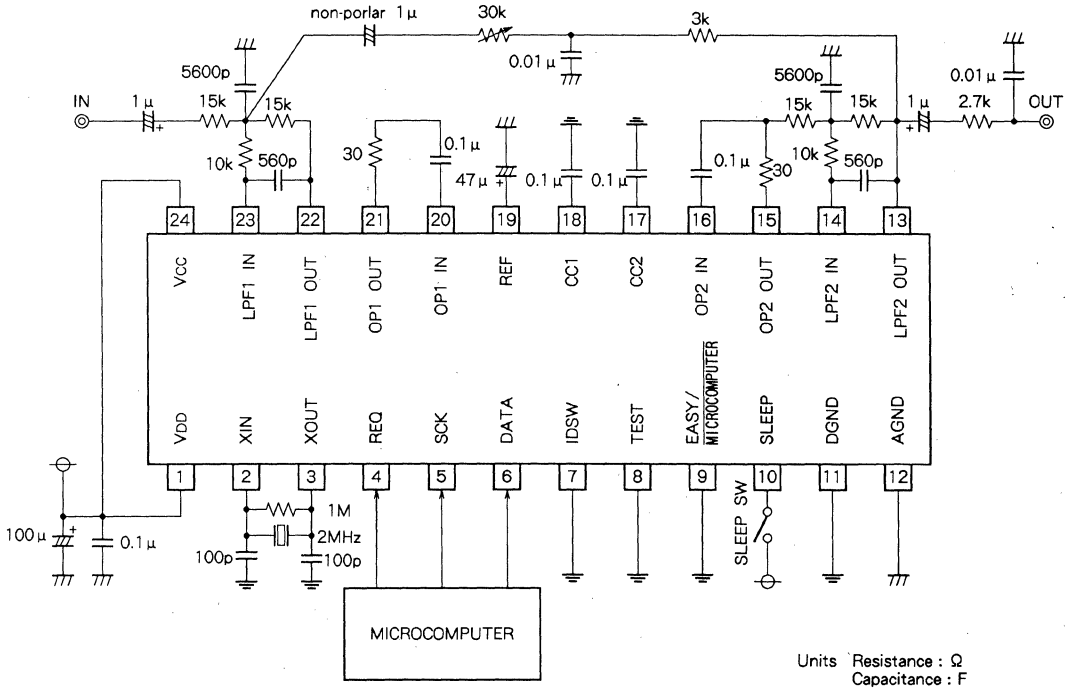
APPLICATION EXAMPLE

1. EASY MODE



Units Resistance : Ω
Capacitance : F

2. MICROCOMPUTER MODE



Units Resistance : Ω
Capacitance : F

M65832SP

DIGITAL ECHO WITH VCR VOICE MIXER

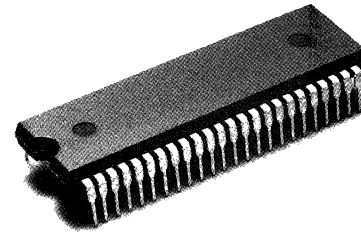
DESCRIPTION

The M65832SP is a CMOS IC designed for VCR karaoke applications.

The IC has a music blank detector, which is necessary for lead-in detection on VCR, as well as echo effects, which are added to voice signals picked up by microphone. The result of detection is output as VISS signals, so that existing microcomputer software can be used without any modification.

FEATURES

- Built-in input/output low pass filters, A−D, D−A converters, and memory facilitate forming of digital echo system
- Four channels of line inputs : Hi-Fi, L, R and normal
  Each provided with bass booster
- MIX output for after recording
- Built-in mixer for mixing microphone, echo, and line signals
- Includes power on reset circuit



Outline 48P4B

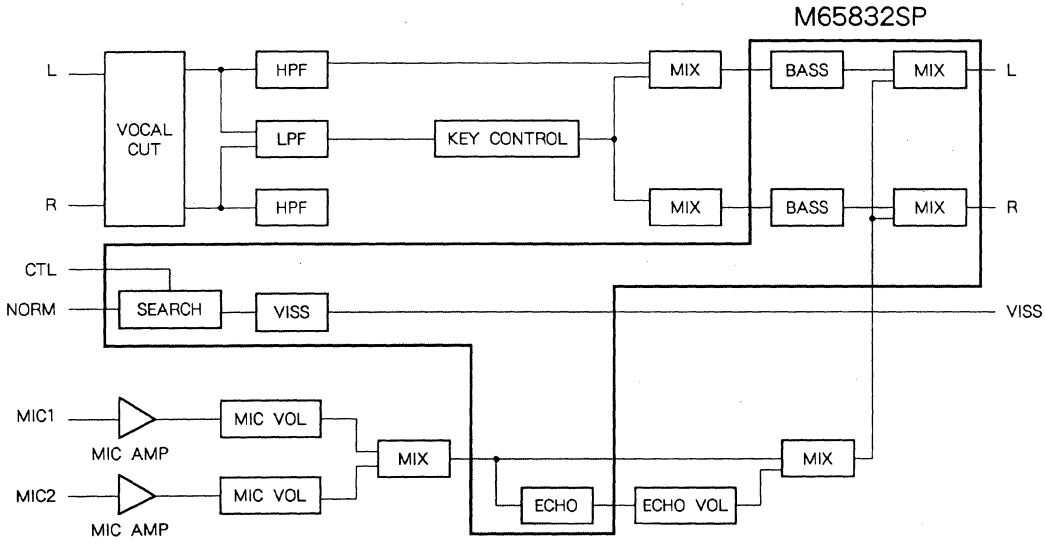
1.778mm pitch 600mil SDIP
(13.0mm × 45.85mm × 3.8mm)

RECOMMENDED OPERATING CONDITIONS

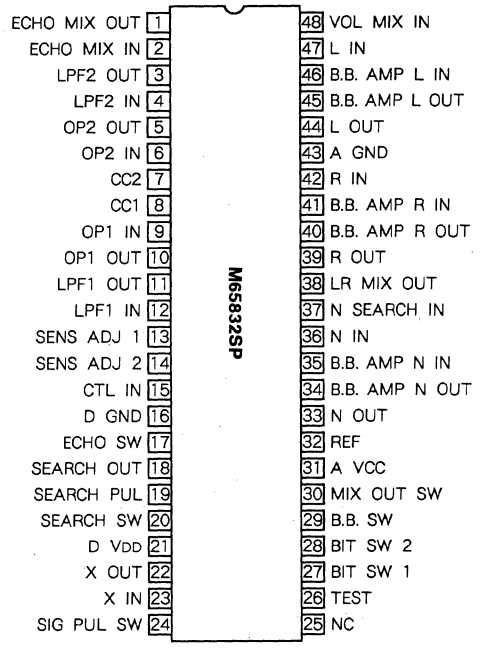
Supply voltage range ..... V_{CC}, V_{DD} = 4.5~5.5V

Rated supply voltage ..... V_{CC}, V_{DD} = 5V

SYSTEM CONFIGURATION



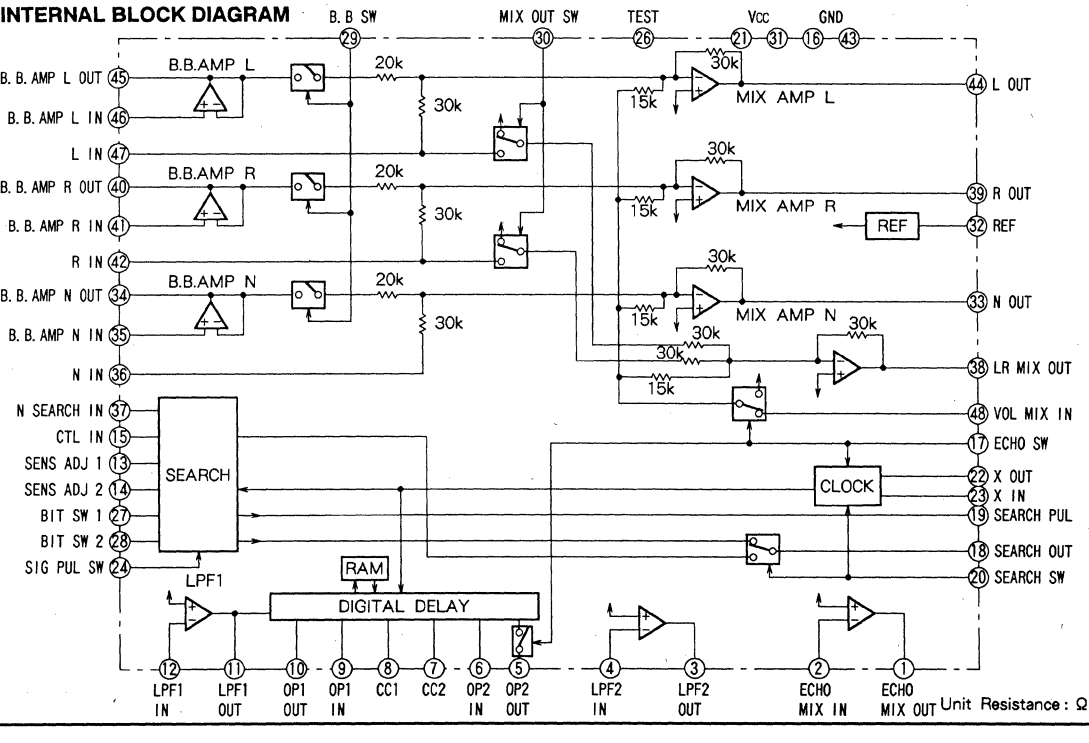
PIN CONFIGURATION



Outline 48P4B

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6.5	V
I_{CC}	Circuit current	100	mA
P_d	Power dissipation	1.4	W
T_{opr}	Operating temperature	− 20 ~ + 75	℃
T_{stg}	Storage temperature	− 40 ~ + 125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
f_{ck}	Clock frequency		3.9	4	4.1	MHz
V_{IH}	High input voltage	Pin ⑰, ⑳, ㉔, ㉗, ㉘, ㉙, ㉚	0.7V_{DD}	−	V_{DD}	V
V_{IL}	Low input voltage	Pin ⑰, ⑳, ㉔, ㉗, ㉘, ㉙, ㉚	0	−	0.3V_{DD}	V
f_{CL}	CTL input frequency		45	−	3.0k	Hz

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, f = 1kHz, V_i = − 22dBV, fck = 4MHz, Ta = 25℃, unless otherwise noted)

Symbol		Parameter	Test conditions		Limits			Unit
					Min	Typ	Max	
I_{CC}		Circuit current			−	40	60	mA
CS	Line	Channel separation	DIN-AUDIO		60	70	−	dB
G_V	Line	Voltage gain			− 3	0	3	dB
G_V	Line	Voltage gain	Pin ㊽ input, LR mix input		3	6	9	dB
V_{omax}	Line	Maximum output voltage	THD = 0.1 %		− 1	3	−	dBV
N_O	Line	Output noise voltage	DIN-AUDIO, R_g = 620Ω		−	− 100	− 95	dBV
THD	Line	Total harmonic distortion	30kHz LPF		−	0.02	0.05	%
f_R	Line	Roll off frequency			300	400	500	Hz
G_{VB}	Line	Bass boost voltage gain	f = 100Hz		5	7	9	dB
V_{PB}	Line	Switching noise voltage	DIN-AUDIO		−	15	30	mV_{P-P}
V_{PL}	Line	Switching noise voltage	L・R OUT, MIX OUT, DIN-AUDIO		−	15	30	mV_{P-P}
Z_i	Line	Input impedance	Pin ㊼, ㊷, ㊱		20	30	−	kΩ
Z_o	Line	Output impedance			−	−	200	Ω
G_V	Delay	Voltage gain			− 3	0	3	dB
V_{imax}	Delay	Maximum input voltage	THD = 10 %		− 3	0	−	dBV
N_O	Delay	Output noise voltage	DIN-AUDIO		−	− 90	− 70	dBV
THD	Delay	Total harmonic distortion	30kHz LPF		−	1.8	3.0	%
T_D	Delay	Delay time			137	139	141	ms
V_{DET}	Search	Detect voltage	Pin ⑭ output		220	320	420	mV_{P-O}
V_{CTL}	Search	CTL input voltage			± 0.9	−	± 2.5	V
V_{CTLNO}	Search	CTL noise protect level			−	−	± 0.3	V
T_C	Search	Music detection pulse number	Real time 10sec	Pin ㉔ = H	512	−	−	bit
				Pin ㉔ = L	2048	−	−	bit
T_D	Search	No music detection pulse number	Pin ㉗ = H, pin ㉘ = L		88	90	92	bit
			Pin ㉗ = L, pin ㉘ = L		36	38	40	bit
			Pin ㉗ = L, pin ㉘ = H		58	60	62	bit
			Pin ㉗ = H, pin ㉘ = H		48	50	52	bit
T_W	Search	VISS signal output pulse number			59	61	63	bit
D_{VISS}	Search	VISS signal duty ratio	Pin ⑰ = H, pin ⑳ = L		20	25	30	%
D_{SOUT}	Search	SEARCH OUT duty ratio	Pin ⑰ = H, pin ⑳ = L		40	50	60	%
Z_{iCTL}	Search	CTL input impedance			30	50	−	kΩ
V_{OH}	Search	SEARCH High output voltage	⑱, ⑲ pin, I_{OH} = − 2mA		3.6	−	−	V
V_{OL}	Search	SEARCH Low output voltage	⑱, ⑲ pin, I_{OL} = 2mA		−	−	1.3	V

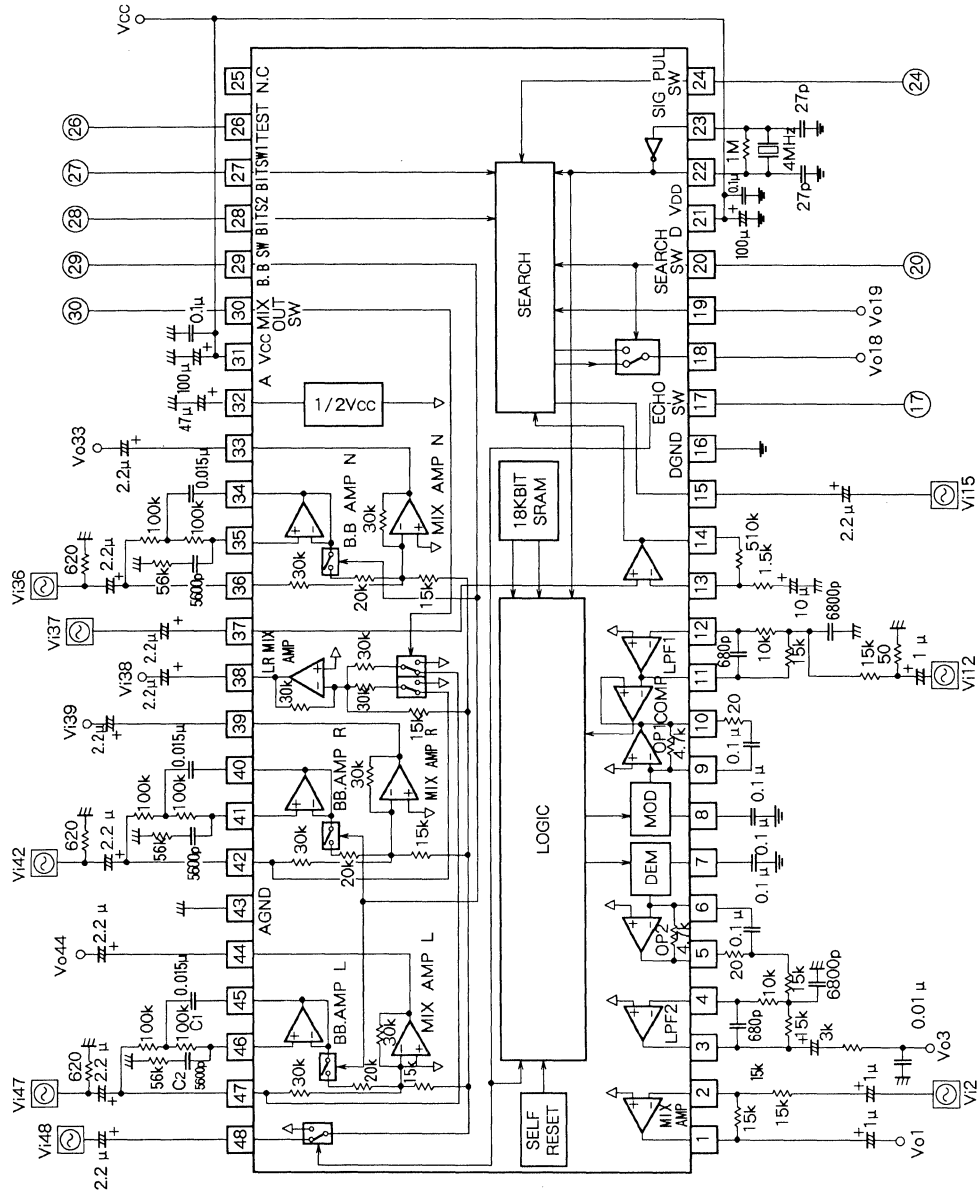
TEST CONDITIONS

Block	Symbol	Parameter	Input	Output	Setting pin conditions 17	20	24	26	27	28	29	30	Remark	
Line	ICC	Circuit current	–	–	H	L	H	L	L	L	L	H	No signal	
	CS	Channel separation	Vi42	Vo44	L	L	H	L	L	L	L	H	DIN–AUDIO	
			Vi47	Vo39										
			Vi42	Vo33										
	GV	Voltage gain	Vi47	Vo44	L	L	H	L	L	L	L	H		
			Vi42	Vo39										
			Vi36	Vo33										
	GV	Voltage gain (MIX)	Vi48	Vo44	H	L	H	L	L	L	L	L		
			Vi48	Vo39										
			Vi48	Vo33										
			Vi47,42	Vo38										
	Vomax	Maximum output voltage	Vi47	Vo44	L	L	H	L	L	L	L	H	THD = 0.1 %	
			Vi42	Vo39										
			Vi36	Vo33										
	NO	Output noise voltage	–	Vo44	L	L	H	L	L	L	L	H	DIN–AUDIO, R_g = 620 Ω, No signal	
			–	Vo39										
			–	Vo33										
	THD	Total harmonic distortion	Vi47	Vo44	L	L	H	L	L	L	L	H	30kHz L.P.F	
			Vi42	Vo39										
			Vi36	Vo33										
	fR	Roll off frequency	Vi47	Vo44	L	L	H	L	L	L	H	H		
			Vi42	Vo39										
			Vi36	Vo33										
	GVB	Bass boost voltage gain	Vi47	Vo44	L	L	H	L	L	L	H	H	f = 100Hz	
			Vi42	Vo39										
			Vi36	Vo33										
	VPB	Switching bass boost noise voltage	–	Vo44	L	L	H	L	L	L	L⇔H	H	DIN–AUDIO, No signal	
			–	Vo39										
			–	Vo33										
	VPL	Switching line noise voltage	–	Vo44	H⇔L	L	H	L	L	L	L	H	DIN–AUDIO, No signal	
			–	Vo39										
			–	Vo33										
			–	Vo38	H	L	H	L	L	L	L	H⇔L		
Delay	GV	Voltage gain	Vi12	Vo3	H	L	H	L	L	L	L	H		
	Vimax	Maximum input voltage											THD = 10 %	
	NO	Output noise voltage	–										DIN–AUDIO, No signal	
	THD	Total harmonic distortion	Vi12										30kHz L.P.F.	
	TD	Delay time												
Search	VDET	Detect voltage	Vi37	PIN⑭,㉚	H	L	H	H	L	L	L	Monitor	㉘pin=H(test mode), ㉚pin=Monitor	Note1
	VCTL	CTL input level	Vi15	Vo18	H	H	H	L	L	L	L	H	GND standard, with ±	Note2
	VCTLNO	CTL input noise level											GND standard, with ±	Note3
	TC	Music detection pulse number	Vi37 Vi15	Vo18,19	H	L	H	L	L	L	L	H	㉔pin = H 512 pulse over	Note4
					H	L	L	L	L	L	L	H	㉔pin = L 2048 pulse over	
	TD	No music detection pulse number			H	L	H	L	H	L	L	H	㉗pin=H, ㉘pin=L 90±2bit	Note5
					H	L	H	L	L	L	L	H	㉗pin=L, ㉘pin=L 38±2bit	
					H	L	H	L	L	H	L	H	㉗pin=L, ㉘pin=H 60±2bit	
					H	L	H	L	H	H	L	H	㉗pin=H, ㉘pin=H 50±2bit	
	TW	VISS output pulse number			H	L	H	L	L	L	L	H		Note6
	DVISS	VISS duty ratio												Note7
	DSOUT	SEARCH OUT duty ratio											⑰ pin = H, ⑳ pin = L	Note8

Note 1. Input a sine wave signal (f = 10kHz) from Vi37 and measure the positive amplitude of pin⑭ when pulses are produced at pin㉚. (By making arrangements that pin㉘= H test mode, it becomes possible to monitor the output of the internal comparator at pin⑰.)

2. Input a pulse signal or sine wave signal (f = 100Hz, 1.8Vpp) from Vi15. Conditions are unfaulty if Vo18 produces pulses.
3. Input a pulse signal or sine wave signal (f = 100Hz, 0.6Vpp) from Vi15. Conditions are unfaulty if Vo18 produces pulses.
4. Input a signal from Vi15 as explained in Note 2 and produce VISS (duty : 25 ± 5%) for a moment (as the unit is in the music detection state when it is powered up.)
   Turn off the Vi15 input and open the connection between pin㉜ REF and GND. (Internal reset).
   Input signals as explained in Notes 1 and 2 simultaneously. Turn off only the Vi37 input when at least 512 or 2048 pulses (make selection according to the polarity of pin㉔) have been input from Vi37. Conditions are unfaulty if pin⑱ produces VISS (duty : 25 ± 5%).
5. Follow the same procedures as explained in Note 4 until the turning off of the Vi37 input. Count the number of control (Vi15) pulses from that point to the instance that VISS (duty : 25 ± 5%) is produced or pin⑲ goes from L to H.
6. Count the number of pulses when VISS (duty : 25 ± 5%) is being produced.
7. Measure the duty ratio of the VISS (duty : 25 ± 5%) signal.
8. Measure the duty ratio of pulses output through pin⑱ when VISS (duty : 25 ± 5%) is not produced.

TEST CIRCUIT



Units Resistance : Ω
Capacitance : F

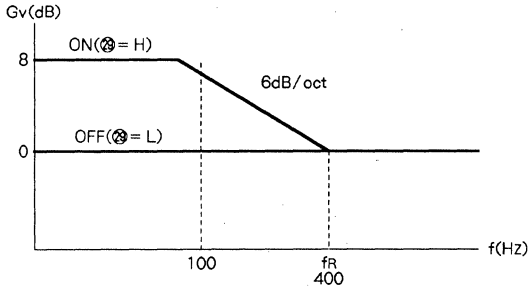
FUNCTION

1. Bass boost circuit

It is provided with three input pins for Hi-Fi VCR audio Lch (L), Rch (R) and normal track audio (N), and bass boost circuit is provided to each pin.

Maximum boost volume is 8dB and the slope characteristic is constant at −6dB/oct. Roll-off frequency f_R is variable by external C and R.

ON/OFF buss boost is controlled by H/L of pin ㉓.



f_R is set to 400Hz in the standard circuit example in application example. To change f_R, use C_1 and C_2 as inverse proportion constants.

$$C_1' = 0.015\,\mu \times \frac{400}{f_R'}\ (F)$$

$$C_2' = 5600p \times \frac{400}{f_R'}\ (F)$$

2. Digital delay circuit

It is a delay circuit havaing the delay time of 139.9msec which uses sampling frequency of 125kHz in A-D and D-A conversion. Appropriate signal bandwidth is around 3kHz.

Delay time is not varialbe. Master clock is not variable either since it is commonly used by music detection when the music interval search function described in 5) is use.

3. Echo mixing amplifier, echo volume, feedback

Built-in OP amplifier connected to ①~② pins is used for echo mixing. Gain of microphone real sound is determined by R_1/R_2 and is set to 0dB in this example. Echo gain is determined by R_1/R_3 and is also set to 0dB.

Echo volume is VR1 inserted right before R_3, which attenuates echo.

Set the feedback to an optimum point using partially fixed resistor VR2.

4. Line mixing amplifier

Microphone echo audio signal which is generated by mixing the real soud and echo is output to pin ①.

It is connected to the built-in line mixing amplifier through pin ㊽ for mixing with L, R and N. ON/OFF of echo and clock is possible by combining pin ⑰ echo switch and pin ⑳ search switch (refer to e)).

Gain in mixing is internally fixed to 6dB for the microphone system and 0dB for the line system.

Since the signal which is generated by mixing L and R is output to pin ㊳, it can be used, for example, for Karaoke using Hi-Fi audio and postrecording using normal track audio.

5. Music interval search

Music interval search circuit is provided for searching the VCR tape head. It is designed so that the ordinary VISS microcomputer software can be used by means of searching no signal section in the normal track and outputting the search result as a VISS signal.

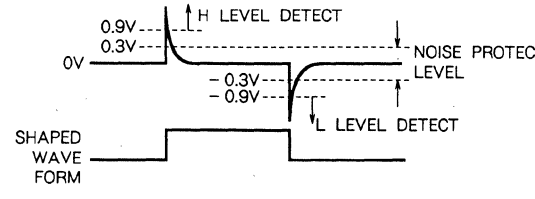
Music interval search function consists of the following function blocks: a) control track signal waveform shaping, b) normal track signal reference level comparison, c) music detection, d) no music detection, and e) VISS signal generation.

(1) Control track signal waveform shaping

M65832SP is provided with a control signal input pin which detects music by detecting real time on the tape recording using the control signal recorded on the VCR control track and outputs VISS signal.

Since the control signal input pin has a built-in waveform shaping circuit, derivative waveform can be input directly. Positive pulse of 0.9V or more for the 0V reference input is detected as a leading of H level and negative pulse of −0.9V or below is detected as a trailing of L level.

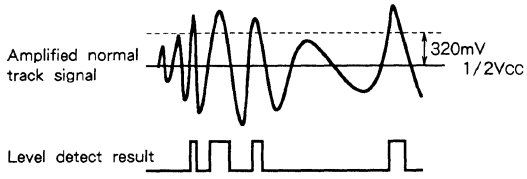
Signal within ±0.3V is not detected to prevent misdetection of noise.



(2) Normal track signal reference level comparison

Normal track audio signal is also input to the pin ㉗ signal reference level comparison circuit for music detection. Signal reference level comparison circuit consists of amplifier and level comparator. Level comparator outputs a pulse when an amplitude of 320mV or more for the no signal level is input. The amplifier can set gain in the range of 0~60dB using an external resistor. Apparent detection level of the level comparator can be determined by setting the gain.

In other words, apparent detection level when the gain is set to 20, 40, and 60dB is 32, 3.2, and 0.32mV respectively.



Amplifier gain G_V is determined by R_4 and R_5 as follows:

$$G_V = R_4 + R_5/R_4 \text{ (times)}$$

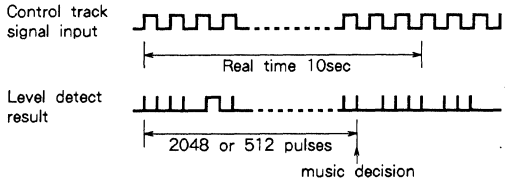
R_5 is appropriate at hundreds of kΩ.

Detected signal low-cut frequency fc is determined by R_4 and C_3 as follows:

$$fc = 1/2\pi\ R_4 \cdot C_3 \text{ (Hz)}$$

(3) Music detection

To search a music interval, it is necessary to judge if it is a music or not. This judgment is made by counting the control track signal and monitoring real time on the tape recording for approx 10 seconds. If the number of pulses in the level detection obtained in b) is 2048 or 512 or more (can be switched by L/H of pin ㉔), it is judged as a music. Since the control track signal is used for monitoring, 10 seconds in real time on the tape recording can always be monitored even if the tape is run at a high speed.

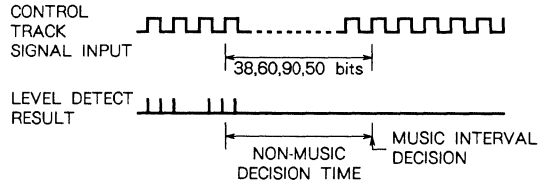


(4) No music detection

No music is judged when no pulse in level detection in b) is detected for a prescribed time after a music was detected.

Like the music detection, judgment is made by counting the control signal and monitoring real time on the tape recording. Real time can be selected by changing the polarity of pin ㉗ and pin ㉘.

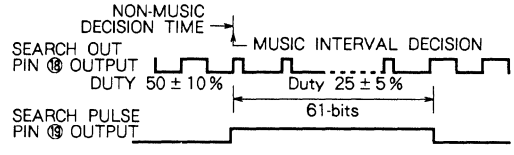
PIN㉗	PIN㉘	CONTROL PULSE No.	real time on tape recording NTSC	PAL
L	L	38(bits)	1.27	1.52(sec)
L	H	60	2.00	2.40
H	L	90	3.00	3.60
H	H	50	1.67	2.00



(5) VISS signal generation

Music interval is recognized at the point where no music is detected after a music was detected, and VISS signal is output. VISS signal which is originally recorded on the control track is ignored, and it is output after converted into a control signal of 50% duty. Therefore, duplicate operation by VISS signal generated in music detection can be prevented.

Since the result of music detection is also output to pin ⑲ during the VISS output, this function can also be applied to music detection without using VISS.



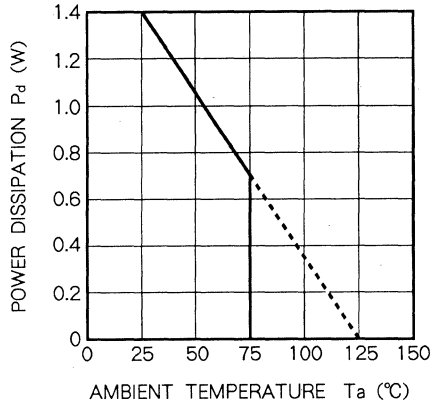
ON/OFF of echo and music interval search circuit can be selected by combining H/L of pin ⑰ echo switch and pin ⑳ search switch.

In other cases than ⑰ = H and ⑳ = L, control track input signal is directly output after waveform shaping.

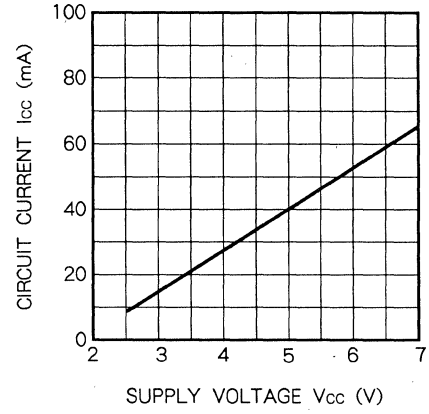
Therefore, real VISS signal recorded in the control track can be sent to MCU.

TYPICAL CHARACTERISTICS

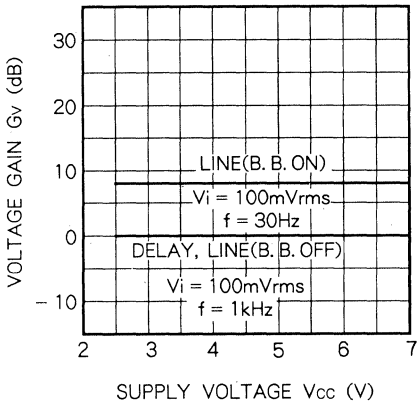
THERMAL DERATING (MAXIMUM RATING)



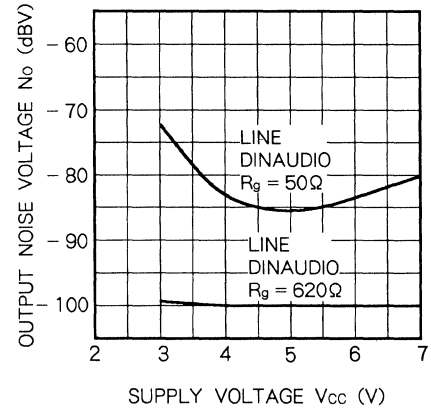
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



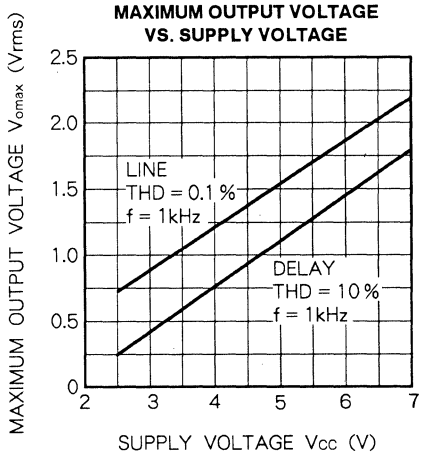
VOLTAGE GAIN VS. SUPPLY VOLTAGE



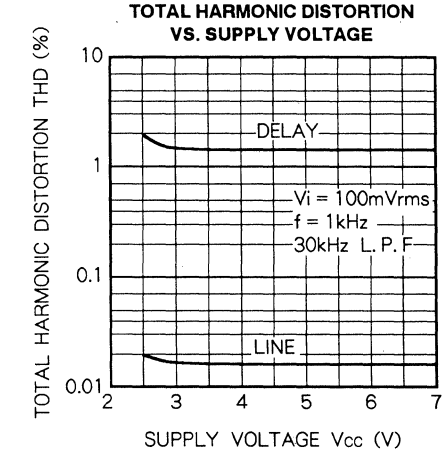
OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



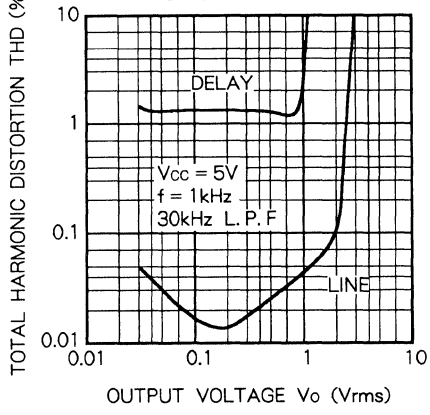
MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



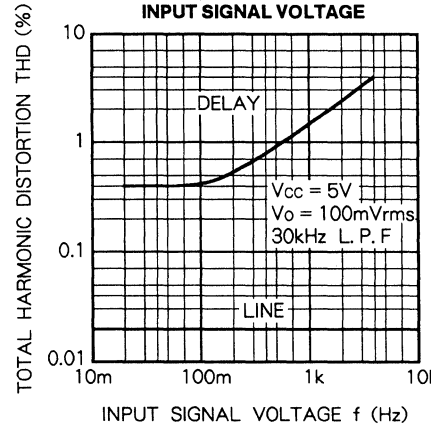
TOTAL HARMONIC DISTORTION VS. SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



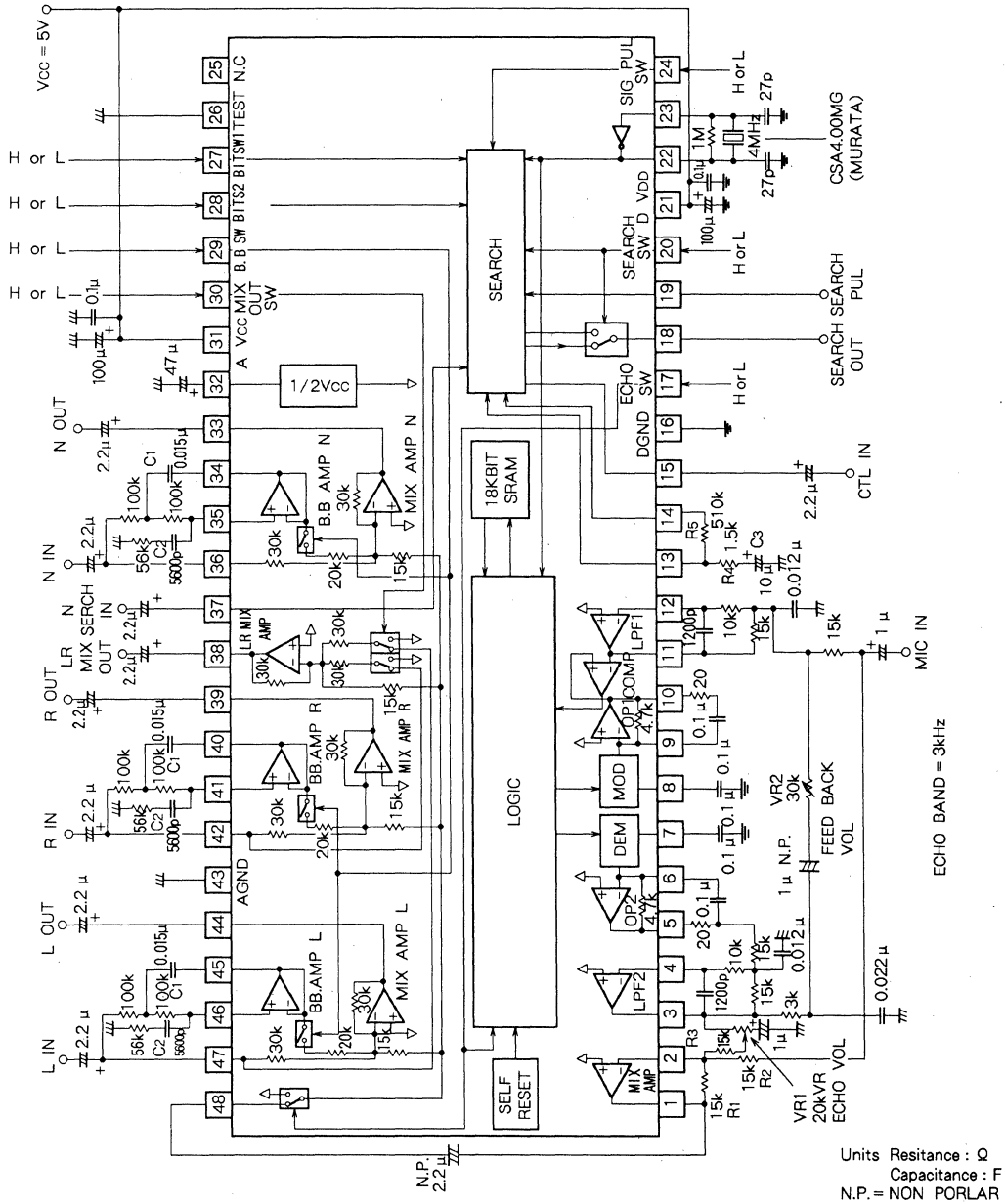
TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE



ECHO & MUSIC INTERVAL SEARCH OPERATING MODE

PIN ⑰ ECHO SW	PIN ⑳ SEAR SW	KARAOKE	OPERATING MODE	Int. CLOCK	PIN ⑱ SEARCH OUT	PIN ⑲ SEARCH PULSE	PIN ㊽ MIX IN
L	–	OFF	ECHO OFF MUS-SEAR OFF	stop	Through output a shaped wave signal from PIN ⑮ input signal	L Fixed	MUTE
H	H	ON	ECHO ON MUS-SEAR ON VISS non-gen	run		H pulse output after music searched	operate
	L		ECHO ON MUS-SEAR ON VISS generate		VISS output after music searched		

APPLICATION EXAMPLE



MITSUBISHI ELECTRIC

M65835FP

SINGLE CHIP KARAOKE PROCESSOR

DESCRIPTION

M65835FP is the semiconductor IC for a karaoke processor based on the silicon gate CMOS process. Provided with the 3-line non-tune detection circuit with the digital echo and bass boost, M65835FP is a single chip processor IC designed specially for hi-fi VCR karaoke systems.

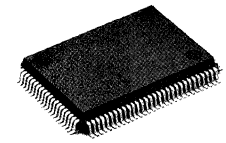
FEATURES

Key control unit

- Contains 32-K bits SRAM.
- Contains the HPF mixing amplifier for stereo.
- Capable of varying the basic key from +3 to −4 and in the expanded mode from +20 to −20.
- Capable of key scanning with the aid of the incorporated microcomputer.
- Provided with auto resetting function, which detects tune intervals and returns the key to the original.
- Provided with LED drive function, which lights LED's corresponding to key UP and DOWN.

Echo unit

- Contains 18-K bits SRAM.
- Contains variable microphone and echo volumes controlled by the microcomputer.
- Contains the line mixing amplifier.
- Maximum delay time: 140 ms; band: 6 kHz



Outline 100P6S-A

0.65mm pitch QFP
(20.0mm × 14.0mm × 2.8mm)

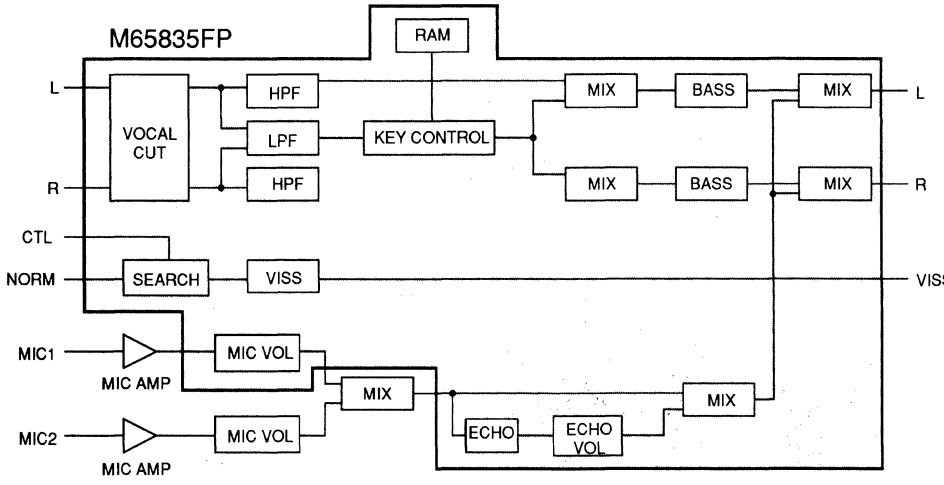
Others

- Provided with three channels for line input, namely hi-fi left and right channels and normal channel, each of which is provided with the bass boost circuit.
- Capable of tune selection meeting VCR requirements based on the tune interval detection and pseudo-VISS generation circuit.
- Capable of cutting off the vocal input in the stereo mode.

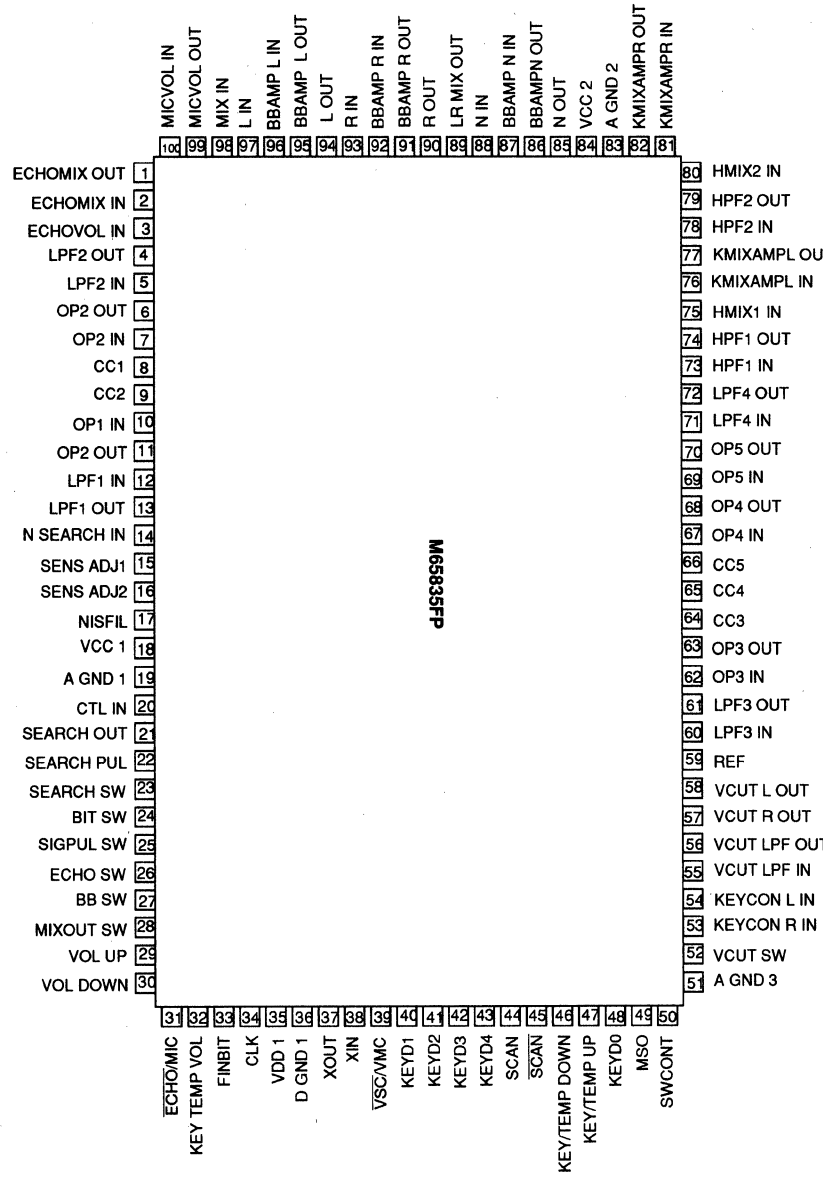
RECOMMENDED OPERATING CONDITIONS

Operating voltage range ..... 4.5 ~ 5.5V
Rated line voltage 5V

SYSTEM CONFIGURATION

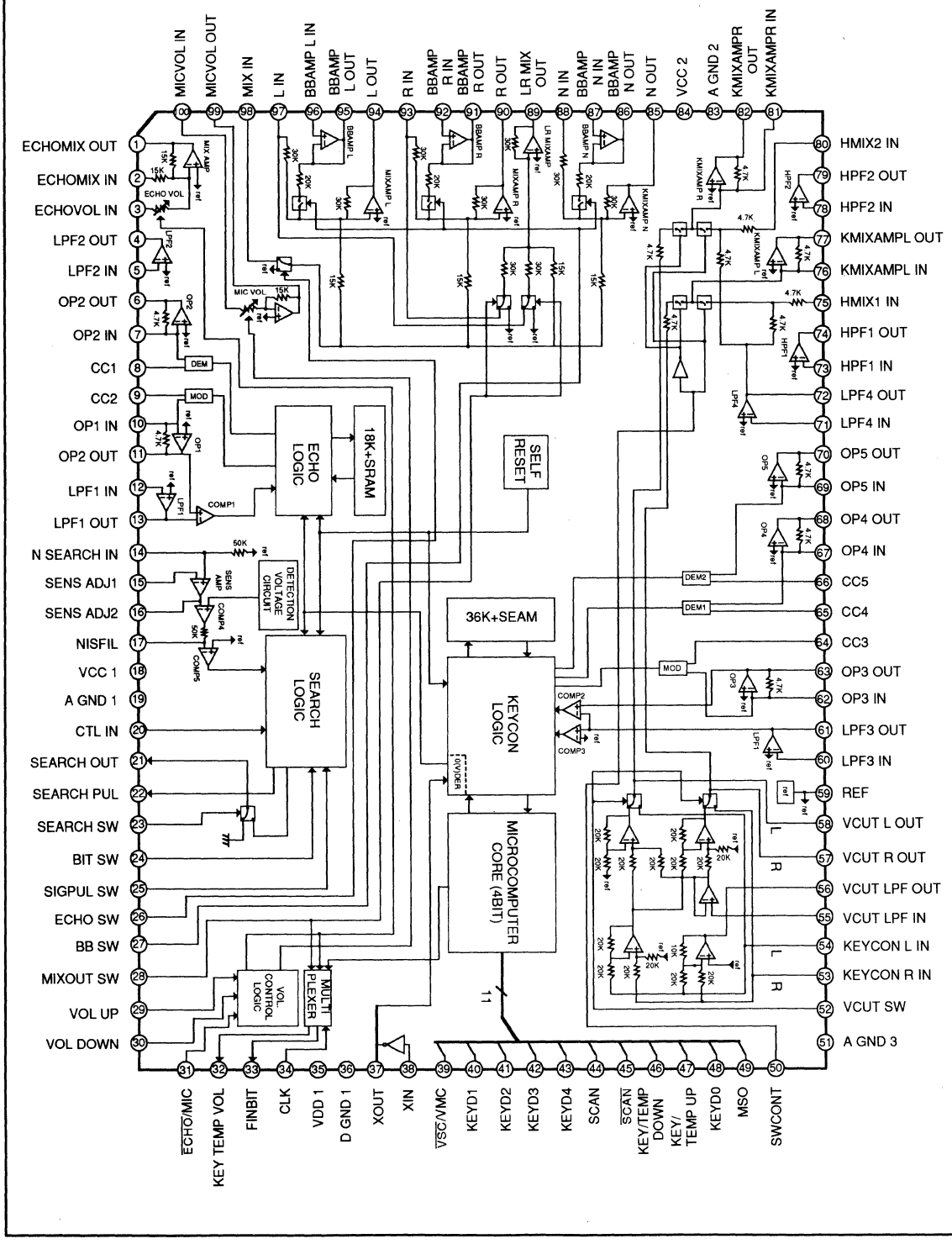


PIN CONFIGULATION



Outline 100P 6S-A

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Name	I/O	Function
①	ECHOMIX OUT	Echo mix output	O	Constitute the mix amplifier circuit with external CR.
②	ECHOMIX IN	Echo mix input	I	
③	ECHOVOL IN	Echo volume input	I	Echo volume input.
④	LPF2 OUT	Low-pass filter 2 output	O	Constitute the low-pass filter on the echo output side with external CR.
⑤	LPF2 IN	Low-pass filter 2 input	I	
⑥	OP2 OUT	Operation amplifier 2 output	O	Constitute the echo demodulation integrator with external C.
⑦	OP2 IN	Operation amplifier 2 input	I	
⑧	CC1	Current control 1	–	Demodulator ADM control.
⑨	CC2	Current control 2	–	Modulator ADM control.
⑩	OP1 IN	Operation amplifier 1 input	I	Constitute the echo modulation integrator with external C.
⑪	OP1 OUT	Operation amplifier 1 output	O	
⑫	LPF1 IN	Low-pass filter 1 input	I	Constitute the low-pass filter on the echo input side with external CR.
⑬	LPF1 OUT	Low-pass filter 1 output	O	
⑭	N SEARCH IN	Normal search input	I	Input normal signals.
⑮	SENS ADJ1	Sensitivity adjustment 1	–	Adjust non-tune detection sensitivity with external CR.
⑯	SENS ADJ2	Sensitivity adjustment 2	–	
⑰	NISFIL	Noise filter	I	Terminal to install the tune counter input signal noise removal filter.
⑱	A VCC 1	Analog supply voltage 1	–	
⑲	A GND 1	Analog ground 1	–	
⑳	CTL IN	Control input	I	Inputs control signals.
㉑	SEARCH OUT	Search output	O	
㉒	SEARCH PUL	Search pulse output	O	
㉓	SEARCH SW	Search switch	I	L: VISS generation present, H: VISS generation absent
㉔	BIT SW	Tune interval detection switch	I	Sets tune interval detection time switching data. H: 110 bits; L: 90 bits
㉕	SIGPUL SW	Tune detection pulse switch	I	L: 8192 pulses, 4096 pulses
㉖	ECHO SW	Echo switch	I	L: echo OFF; H: echo ON
㉗	BB SW	Bass boost switch	I	L: BB OFF; H: BB ON
㉘	MIXOUT SW	Mix output switch	I	L: LR mix output; H: mix output OFF
㉙	VOL UP	Volume UP input	I	Volume increases one step each time an L pulse is counted. "L" is fixed when external volume is provided.
㉚	VOL DOWN	Volume DOWN input	I	Volume decreased one step each time an L pulse is counted. "L" is fixed when external volume is provided.
㉛	$\overline{\text{ECHO}}$/MIC	Echo/microphone selector switch	I	Echo/microphone selector switch. Selects microphone or echo volume control. L: echo; H: microphone. "L" is fixed when external volume is provided.
㉜	KEY TEMP VOL	Key tempo and volume output	O	Serially outputs information as to the key tempo and volumes.
㉝	FIN BIT	Final bit mark output	O	Output "H" pulses after outputting the final bit of the serial data explained above.
㉞	CLK	Clock input	I	Clock input terminal to read key tempo and volume information.
㉟	VDD 1	Digital supply voltage 1	–	
㊱	D GND 1	Digital ground 1	–	
㊲	XOUT	Oscillator output	O	
㊳	XIN	Oscillator input	I	
㊴	$\overline{\text{VSC}}$/VMC	VSC/VMC selector switch	I	L: VSC mode; H: VMC mode
㊵	KEYD 1	Key drive 1	O	Lights LED when KD1 is selected.
㊶	KEYD 2	Key drive 2	O	Lights LED when KD2 or KU1 is selected.
㊷	KEYD 3	Key drive 3	O	Lights LED when KD3 or KU2 is selected.
㊸	KEYD 4	Key drive 4	O	Lights LED when KD4 or KU3 is selected.
㊹	SCAN	Scan line (digit)	O	When AO = "H", LED: KD1, KD2, KD3 and KD4 scan: TU, TD and TCS
㊺	$\overline{\text{SCAN}}$	Scan line (digit)	O	When $\overline{\text{AO}}$ = "H", LED: KU1, KU2, and KU3 scan: KU, KD and ARS
㊻	KEY/TEMP DOWN	Key and tempo input	I	KD: key becomes one step lower each time this is pushed. TD: tempo becomes one step lower each time this is pushed.

Pin No.	Symbol	Name	I/O	Function
㊼	KEY/TEMP UP	Key and tempo input	I	KU: key becomes one step higher each time this is pushed. TU: tempo becomes one step higher each time this is pushed.
㊽	KEYD 0	Key drive 0	O	Lights LED ("L") when there is no change in key.
㊾	MSO	Mute output	O	Mute signal outputs from the microcomputer
㊿	SWCONT	Switch control input	I	
(51)	A GND 3	Analog ground 3	—	
(52)	VCUT SW	Vocal cutoff switch	I	L: vocal cutoff OFF (through output) H: vocal cutoff ON
(53)	KY R IN	Key control R input	I	Input Rch signals.
(54)	KY L IN	Key control L input	I	Input Lch signals.
(55)	VCUT LPF IN	Vocal cutoff LPF input	I	Terminal to install vocal cutoff LPF
(56)	VCUT LPF OUT	Vocal cutoff LPF output	O	
(57)	VCUT R OUT	Vocal cutoff R output	O	
(58)	VCUT L OUT	Vocal cutoff L output	O	
(59)	REF	Reference	—	Output reference voltage (1/2 Vcc)
(60)	LPF3 IN	Low-pass filter 3 input	I	Constitute the low-pass filter on the key control input side with external CR.
(61)	LPF3 OUT	Low-pass filter 3 output	O	Constitute the low-pass filter on the key control side with external CR.
(62)	OP3 IN	Operation amplifier 3 input	I	Constitute the key control modulation integrator with external CR.
(63)	OP3 OUT	Operation amplifier 3 output	O	
(64)	CC 3	Current control 3	–	
(65)	CC 4	Current control 4	–	
(66)	CC 5	Current control 5	–	
(67)	OP4 IN	Operation amplifier 4 input	I	Constitute the key control modulation integrator with external CR.
(68)	OP4 OUT	Operation amplifier 4 output	O	
(69)	OP5 IN	Operation amplifier 5 input	I	Constitute the key control modulation integrator with external CR.
(70)	OP5 OUT	Operation amplifier 5 output	O	
(71)	LPF4 IN	Low-pass filter 4 input	I	Constitute the key control low-pass filter with external CR.
(72)	LPF4 OUT	Low-pass filter 4 output	O	
(73)	HPF1 IN	High-pass filter 1 input	I	Constitute the key control high-pass filter (Lch) with external CR.
(74)	HPF1 OUT	High-pass filter 1 output	O	
(75)	HMIX1 IN	High-pass 1 mix input	I	Terminal to mix and input HPF 1 outputs.
(76)	KMIXAMPL IN	Key mix amplifier L input	I	Constitute the key control Lch-side mix amplifier with external C.
(77)	KMIXAMPL OUT	Key mix amplifier L output	O	
(78)	HPF2 IN	High-pass filter 2 input	I	Constitute the key control high-pass filter (Rch) with external CR.
(79)	HPF2 OUT	High-pass filter 2 output	O	
(80)	HMIX2 IN	High-pass 2 mix input	I	Terminal to mix and input HPF 2 outputs
(81)	KMIXAMPR IN	Key mix amplifier R input	I	Constitute the key control Rch-side mix amplifier with external C.
(82)	KMIXAMPR OUT	Key mix amplifier R output	O	
(83)	A GND 2	Analog ground 2	–	
(84)	VCC 2	Analog supply voltage 2	–	
(85)	N OUT	Nch output	O	
(86)	BBAMP N OUT	Bus boost Nch output	O	Constitute the bus boost circuit (Nch) with external CR.
(87)	BBAMP N IN	Bus boost Nch input	I	
(88)	N IN	Nch input	I	
(89)	LR MIX OUT	LR mix output	O	
(90)	R OUT	Rch output	O	
(91)	BBAMP R OUT	Bus boost Rch output	O	Constitute the bus boost circuit (Rch) with external CR.
(92)	BBAMP R IN	Bus boost Rch input	I	
(93)	R IN	Rch input	I	
(94)	L OUT	Lch output	O	
(95)	BBAMP L OUT	Bus boost Lch output	O	Constitute the bus boost circuit (Lch) with external CR.
(96)	BBAMP L IN	Bus boost Lch input	I	
(97)	L IN	Lch input	I	
(98)	MIX IN	Mix input	I	Input echo volume output signals.
(99)	MICVOL OUT	Microphone volume output	O	Microphone volume output
(100)	MICVOL IN	Microphone volume input	I	Microphone volume input

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6.5	V
I_{CC}	Circuit current	120	mA
P_d	Power dissipation	1400	mW
T_{opr}	Operating temperature	−20~70	°C
T_{stg}	Storage temperature	−40~125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
AVcc	Analog supply voltage		4.5	5.0	5.5	V
DVDD	Digital supply voltage		4.5	5.0	5.5	V
△Vcc	Potential difference between A Vcc and D VDD		−0.3	0	0.3	V
fck	Clock frequency		15.5	16.0	16.5	MHz
V_{IH}	Input voltage ("H" level)	㉓,㉔,㉕,㉖,㉗,㉘,㉛,㉞,㊿,㊿② pin	0.7 VDD	–	VDD	V
V_{IL}	Input voltage ("L" level)		0	–	0.3VDD	V
fcL	CTL input frequency	Pin ㉖ = H	30	–	3.0k	Hz

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, f = 1 kHz, Vi = 200mVrms, fck = 16MHz, Ta = 25°C unless otherwise noted)

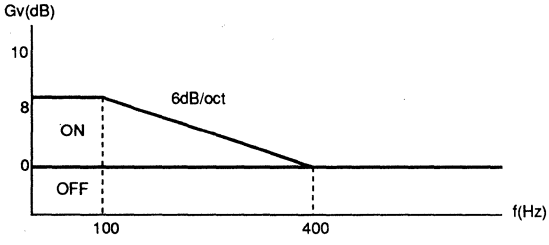
Block name	Symbol	Parameter	Test conditions	Limits			Unit
				Min	Typ	Max	
Total system	I_{CC}	Circuit current	No signals present	–	65	75	mA
Line	CS	Channel separation	DIN-AUDIO	60	70	–	dB
	Gv	I/O voltage gain		−2	0	2	dB
	Gv	I/O voltage gain		4	6	8	dB
	V_{OMAX}	Maximum output voltage	THD = 0.1 %	−1	3	–	dBv
	No	Output noise voltage	DIN-AUDIO, Rg = 620 Ω	–	−100	−95	dBv
	THD	Total harmonics distortion	30 kHzL.P.F.	–	0.02	0.05	%
	fR	Bass boost roll-off frequency		300	400	500	Hz
	GvB	Bass boost voltage gain	f = 100 Hz	5	7	9	dB
	VPB	Bass boost switching noise voltage	DIN-AUDIO	–	15	30	mV_{pp}
	VPL	Line switching noise voltage	L•R OUT,MIX OUT,DIN-AUDIO	–	15	30	mV_{pp}
	Zi	Input impedance		20	30	–	kΩ
	Zo	Output impedance		–	–	200	Ω
Echo	Gv	I/O voltage gain		−2	0	2	dB
	Vimax	Maximum input voltage	THD = 10 %	−3	0	–	dBv
	No	Output noise voltage	DIN-AUDIO, Rg = 51 Ω	–	−90	−70	dBv
	THD	Total harmonics distortion	30 kHzL.P.F.	–	1.8	3.0	%
	TD	Delay time		137	139	141	msec
Search	VDET	Internal detection sensitivity	Pin ⑯ output amplitude	240	320	400	mVpo
	VCTL	CTL input voltage	With reference to GND	±0.9	–	±2.5	V
	VCTLNO	CTL noise protect level		–	–	±0.3	V
	Tc	No. of tune detection pulses	Play time: approx.20 s, Pin ㉕ = H	4096	–	–	pulse
			Play time: approx.20 s, Pin ㉕ = L	8192	–	–	pulse
	TD	Tune interval detection time	Pin ㉔ = H	98	110	102	bit
			Pin ㉔ = L	88	90	92	bit
	TW	No. of VISS output pulses		59	61	63	bit
	DVISS	VISS duty		20	25	30	%
	DSOUT	Search OUT duty	Pin ㉓ = L, Pin ㉖ = H	40	50	60	%
	NOCE	Echo cross talk level during search	N SEARCH IN = 50mVrms, f=6kHz,DIN-AUDIO,Rg=51Ω	–	−70	−50	dBv
	NOCL	Line cross talk level during search	N SEARCH IN = 50mVrms, f=6kHz,DIN-AUDIO,Rg=620Ω	–	−75	−55	dBv
	VOH	Search H output voltage	㉑,㉒ pin IOH = −2mA	3.6	–	–	V
	VOL	Search L output voltage	㉑,㉒ pin IOL = 2mA	–	–	1.3	V

Block name	Symbol	Parameter	Test conditions	Limits			Unit
				Min	Typ	Max	
Key control	NOM	Output noise voltage (VMC)	FO (TO,KO), DIN-AUDIO and Rg = 51 Ω	–	–82	–65	dBv
	NOS	Output noise voltage (VSC)	FO (TO,KO), DIN-AUDIO and Rg = 51 Ω	–	–70	–57	dBv
	THDM	Total harmonics distortion(VMC)	FO (TO,KO), 3 kHz L.P.F.	–	0.8	2.0	%
	THDS	Total harmonics distortion (VSC)	FO (TO,KO), 3 kHz L.P.F.	–	1.8	3.0	%
	GV	I/O voltage gain		–6	0	6	dB
	VOmax	Maximum output voltage	THD = 10 %, 30 kHz L.P.F.	–3	0	–	dBv
Vocal cutoff	NO	Output noise voltage	Pin ㊷ = H, DIN-AUDIO, Rg = 51 Ω	–	–88	–72	dBv
	GV	I/O voltage gain	With input given via single channel	–3	0	3	dB
	VOmax	Maximum output voltage	With input given via single channel THD=10 %, 30 kHz L.P.F.	–1	3	–	dBv
	GVREJ	Vocal cutoff ratio	With L and R inputs given	20	24	–	dB
Echo volume	Gve 0	I/O voltage gain 0 dB	Voltage gain set to 0 dB	–1.0	0.0	1.0	dB
	Gve –2	I/O voltage gain –2 dB	Voltage gain set to –2 dB	–3.0	–2.0	–1.0	dB
	Gve –4	I/O voltage gain –4 dB	Voltage gain set to –4 dB	–5.0	–4.0	–3.0	dB
	Gve –6	I/O voltage gain –6 dB	Voltage gain set to –6 dB	–7.0	–6.0	–5.0	dB
	Gve –8	I/O voltage gain –8 dB	Voltage gain set to –8 dB	–9.0	–8.0	–7.0	dB
	Gve –10	I/O voltage gain –10 dB	Voltage gain set to –10 dB	–12.0	–10.0	–9.0	dB
	Gve –15	I/O voltage gain –15 dB	Voltage gain set to –15 dB	–17.0	–15.0	–13.0	dB
	Gve –∞	I/O voltage gain –∞ dB	Voltage gain set to –∞ dB	–	–60.0	–40.0	dB
Microphone volume	Gve 6	I/O voltage gain 6 dB	Voltage gain set to 6 dB	4.5	6.0	7.5	dB
	Gve 3	I/O voltage gain 3 dB	Voltage gain set to 3 dB	1.5	3.0	4.5	dB
	Gve 0	I/O voltage gain 0 dB	Voltage gain set to 0 dB	–1.5	0.0	1.5	dB
	Gve –3	I/O voltage gain –3 dB	Voltage gain set to –3 dB	–4.5	–3.0	–1.5	dB
	Gve –6	I/O voltage gain –6 dB	Voltage gain set to –6 dB	–7.5	–6.0	–4.5	dB
	Gve –10	I/O voltage gain –10 dB	Voltage gain set to –10 dB	–12.0	–10.0	–8.5	dB
	Gve –15	I/O voltage gain –15 dB	Voltage gain set to –15 dB	–17.0	–15.0	–13.0	dB
	Gve –∞	I/O voltage gain –∞ dB	Voltage gain set to –∞ dB	–	–60.0	–40.0	dB

FUNCTIONAL DESCRIPTION

(1) Bass boost

Pin ㉗ BBSW = H. When bass boost is ON, BBSW = L; when OFF, flat.



M65835FP is provided with 3 input terminals for 3 lines: vocal Lch (L) and Rch (R) and normal track vocal (N). The bass boost circuit is inserted into each line.

The maximum voltage gain is 8 dB, and the slope characteristics are constant at –6 dB/oct. The roll-off frequency, fR, however, can be varied via external C and R.

Bass boost is turned ON/OFF via H/L of pin ㉗.

fR is set at 400Hz in the example applied circuit. To change fR, change C1 and C2 assuming these as inverse proportional constants.

$$C1' = 0.015\mu \times \frac{400}{fR'} \text{ (F)}$$

$$C2' = 5600\ P \times \frac{400}{fR'} \text{ (F)}$$

(2) Digital delay circuit

This has delay time of 139.3 ms with the sampling frequency during A-D and D-A conversion at 125 kHz. The signal band is set at 6kHz in the example applied circuit.

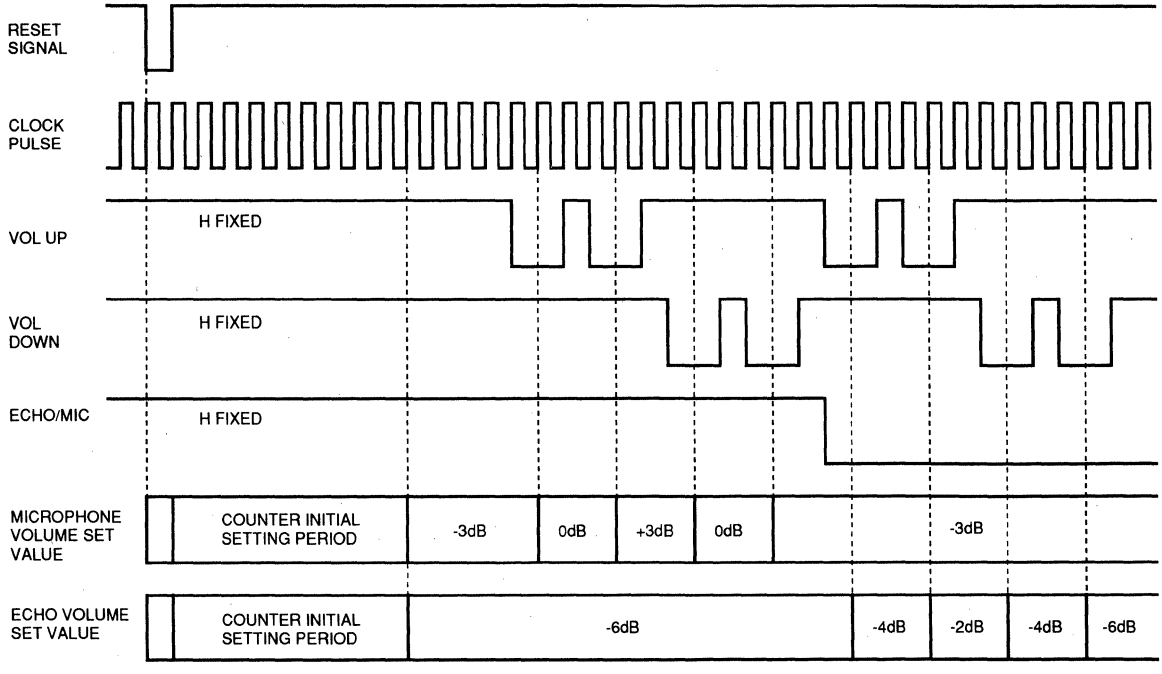
Delay time cannot be changed. When tune intervel detection is being carried out, the master clock is shared for tune interval detection, and therefore the master clock cannot be chaged, either.

(3) Volume

After reset, the incorported counter carries out initial setting of volumes. Initial set values depend on whether the VOL UP terminal (pin ㉙), VOL DOWN terminal (pin ㉚) and ECHO/MIC terminal (pin ㉛) are fixed to H ot L. (See below.)

VOL UP terminal (pin ㉙) VOL DOWN terminal (pin ㉚) ECHO/MIC terminal (pin ㉛)	Echo volume	Microphone volume
L	Maximum (0 dB)	Maximum (+6 dB)
H	–6dB	–3dB

Volume is increased/decreased by detecting the L level input via the push switch as clock pulse build-up. This detection point gives the boundary beyond which the volume is varied.



VOLUME INCREMENT

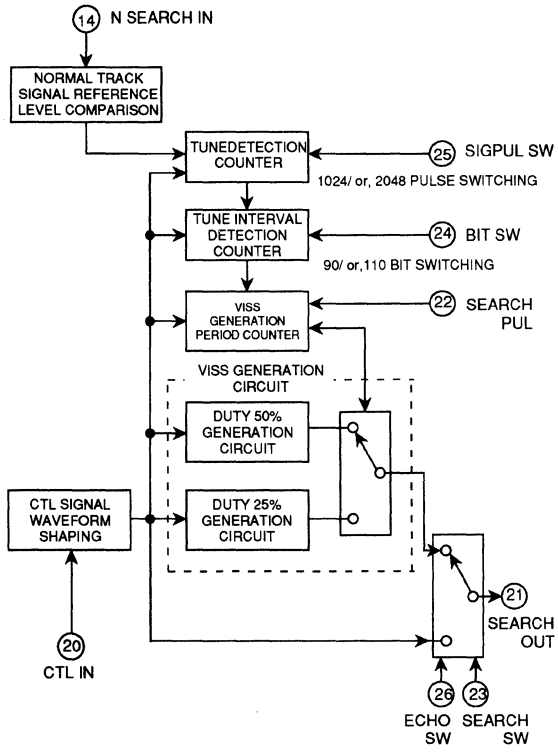
Echo volume (dB)

Level	D11	D12	D13
–∞	L	L	L
–15	H	L	L
–10	L	H	L
–8	H	H	L
–6	L	L	H
–4	H	L	H
–2	L	H	H
0	H	H	H

Microphone volume (dB)

Level	D8	D9	D10
–∞	L	L	L
–15	H	L	L
–10	L	H	L
–6	H	H	L
–3	L	L	H
0	H	L	H
3	L	H	H
6	H	H	H

(4) Non-tune detection block diagram



(5)Music interval search

Music interval search circuit is provided for searching the VCR tape head. It is designed so that the ordinary VISS microcomputer software can be used by means of searching no signal section in the normal track and outputting the search result as a VISS signal.

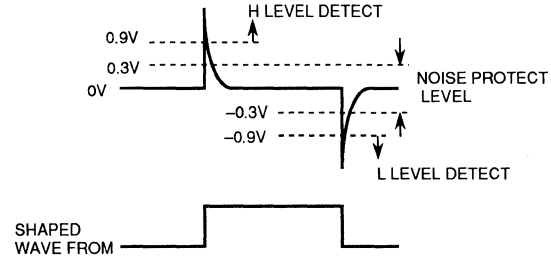
Music interval search function consists of the following function blocks, a) control track signal waveform shaping, b) normal track signal reference level comparison, c) music detection, d) no music detection, and e) VISS signal generation.

a) Control track signal waveform shaping

M65835FP is provided with a control signal input pin which detects music by detecting real time on the tape recording using the control signal recorded on the VCR control track and outputs VISS signal.

Since the control signal input pin has a built-in waveform shaping circuit, derivative waveform can be input directly. Positive pulse of 0.9V or more for the 0V reference input is detected as a leading of H level and nagative pulse of –0.9V or below detected as a trailing of L level.

Signal within ± 0.3V is not detected to prevent misdetection of noise.

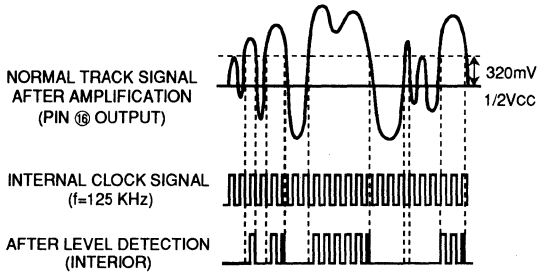


b) Normal track signal reference level comparison

Normal track audio signal is also input to the pin ㊲ signal reference level comparison circuit for music detection.

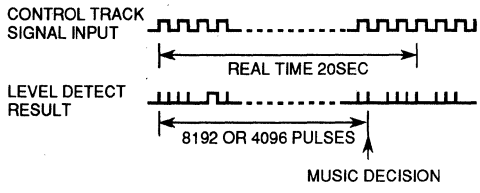
Signal reference level comparison circuit consists of amplifier and level comparator. Level comparator outputs a pulse when an amplitude of 320mV or more for the no signal level is input. The amplifier can set gains in the range of 0~60dB using an external resistor. Apparent detection level of the level comparator can be determined by setting the gain.

In other words, apparent detection level when the gain is set to 20, 40 and 60dB is 32, 3.2, and 0.32mV respectively.



c) Music detection

To search a music interval, it is necessary to judge if it is a music or not. This judgment is made by counting the control track signal and monitoring real time on the tape recording for approx 20 seconds. If the number of pulses in the level detection obtained in b) is 8192 or 4096 or more (can be switched by L/H of pin ㉓), it is judged as a music. Since the control track signal is used for monitoring, 20 seconds in real time on the tape recording can always be monitored even if the tape is run at a high speed.

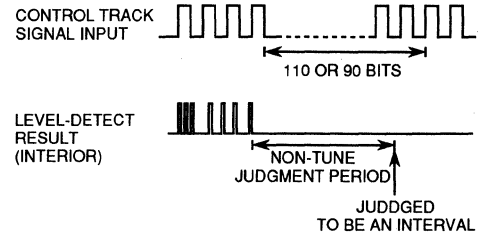


d) Non-tune detection

After a part of the tape is judged to have a tune, if none of the level detection pulses in b) above is present for a period corresponding to the number of the bits of the control pulses shown below, that part where none of the level detection pulses is found is judged to be non-tune.However, if even a single pulse of level detection in b) is present, the counter indicating the judgment of non-tune is reset.

During monitoring non-tune, the control signals are counted and judged based on time recorded on the tape as in the case of tune detection. For the monitoring period 110 ord 90 bits can be chosen (switchable via L/H of pin 24).

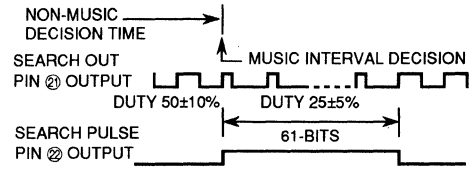
Pin 24	No. of non-tune detection control pulses
H	110 bits
L	90 bits



e) VISS signal generation

Music interval is recognized at the point where no music is detected after a music was detected, and VISS signal is output. VISS signal which is originally recorded on the control track is ignored, and it is output after converted into a control signal of 50% duty. Therefore, duplicate operation by VISS signal generated in music detection can be prevented.

Since the result of music detection is also output to pin ㉒ during VISS output, this function can also be applied to music detection without using VISS.



ON/OFF of echo and music interval search circuit can be selected by combining H/L of pin ㉛ echo switch and pin ㉓ search switch.

In other cases than pin ㉛ = H and pin ㉓ = L, control track input signal is directly output after waveform shaping.

Therefore, real VISS signal recorded in the control track can be sent to MCU.

ECHO AND TUNE INTERVAL DETECTION OPERATION MODES

Pin ㉛ echo switch	Pin ㉓ search switch	Karaoke	Operation mode	Internal clock	Pin ㉑ search OUT	Pin ㉒ search PULSE	Pin ㊽ Mixin
L	—	OFF	Echo OFF Tune interval detection OFF	Stops	Through output follows the shaping of pin ⑭ input waveform.	L fixed	Mute
H	H	ON	Echo ON Tune interval detection ON No VISS generated	Operates		Output "H" for the VISS genera-tion period after tune interval de-tection.	Input possible
	L		Echo ON Tune interval detection ON VISS generated		Generates VISS after tune interval detection. During other periods, duty 50%		

This tune interval detection is possible for the range from 30 to 3 kHz of the control track signal input frequency.

EXPLANATION OF OPERATION AT 3 KHZ OR GREATER OF CONTROL FREQUENCY

Although the advisable control input frequency is 30 to 3 kHz, inputting signals of 3 kHz or greater may cause the duty ratio to be 25 and 50%, which is outside the specifications.
When the control input frequency is 3.5 kHz or gerater, the H period for pin ㉑ search OUT pulses becomes as follows because of the internal circuit design:

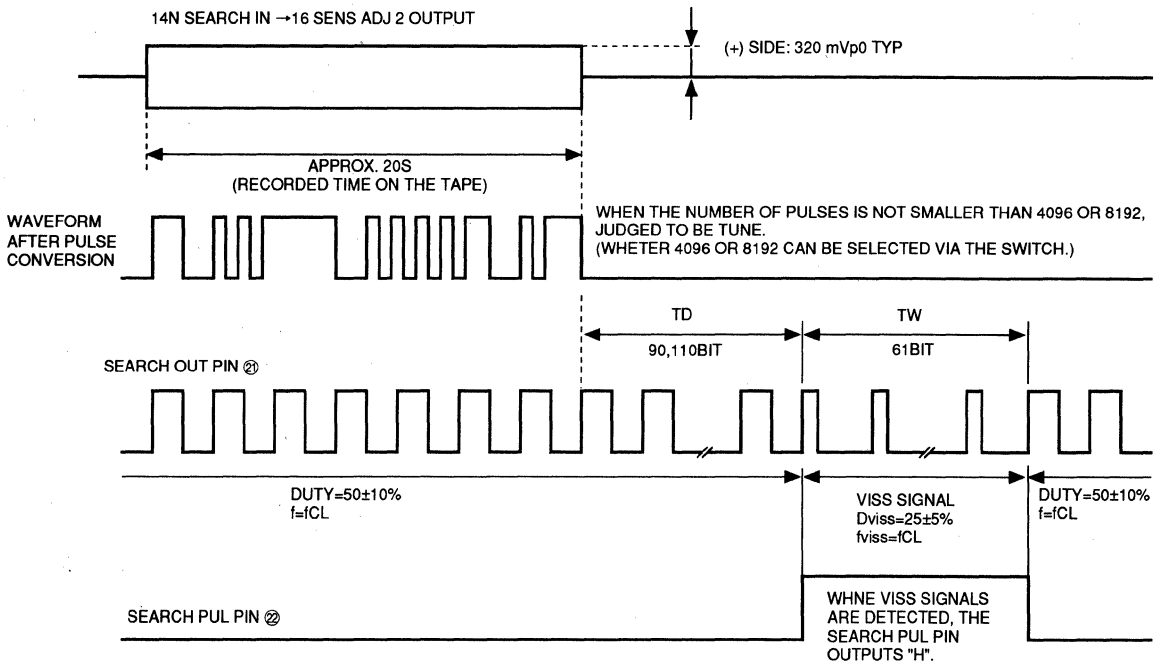
25% (VISS signal) pulse = 64 ms
50% (other than VISS) pulse = 128 ms

The period thus becomes constant. Accordingly, the greater the control input frequency, the shorter the period and the greater the duty ratio. Thus the duty ratios when the frequency is 3 kHz or greater are as shown in the table below.

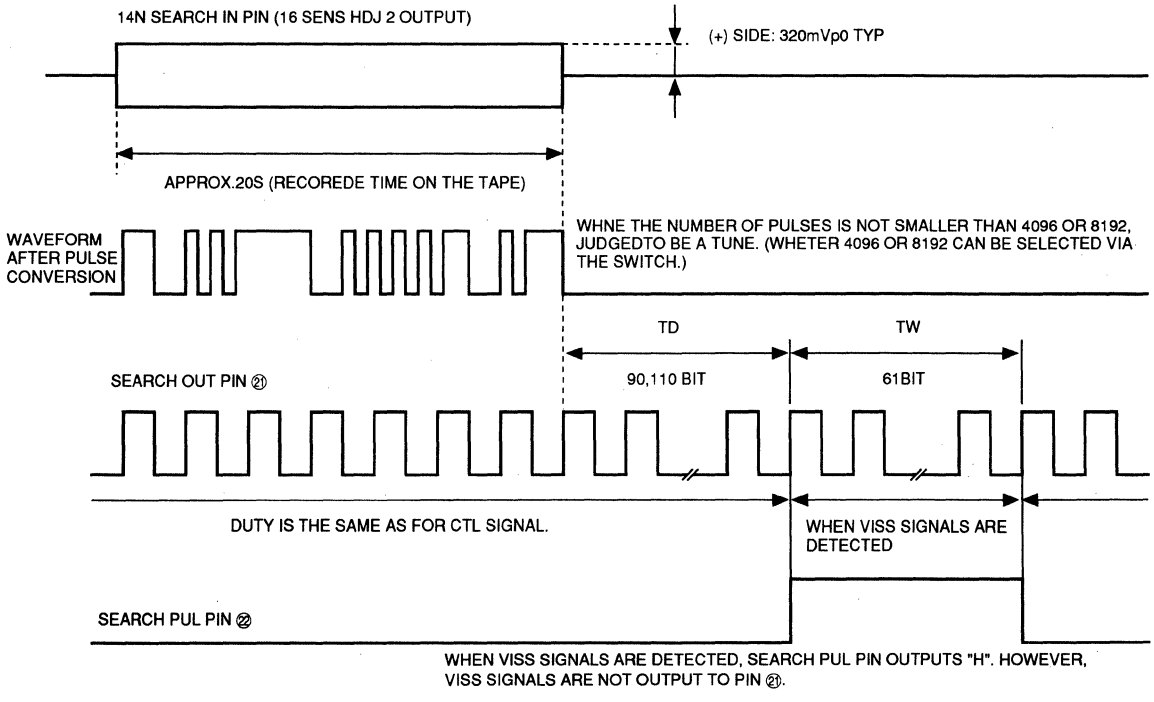
CTL input frequency	25% pulse duty ratio	50% pulse duty ratio
4kHz	25.6%	51.2%
5kHz	32.0%	64.0%
6kHz	38.4%	76.8%
7kHz	44.8%	89.6%

(6) Non-tune detection operation timing

a) Pin ㉓ search SW = L and pin ㉔ echo SW = H



b) Pin ㉓ search SW = H and pin ㉔ echo SW = H



(7) Key control

There are two major modes to change the key; VMC (variable music control) and VSC (variable speed control).

VMC provides relatively small variable range but maintains high sound quality, which is mainly used key control orchestra music for singing (called KARAOKE). On the other hand VSC provides lower sound quality but variable key range as wide as ±1 octorve or more, which is used key compensation in reproduction of source music in double speed.

Switching of VMC and VSC is made by TCS ON (VMC) and OFF (VSC), but it is necessary to make a reset in switching of mode since it is determined simultaneously with cancellation of reset. Since noise may be generated in the analog system when resetting, it is recommended to mute the output stage at each mode switching.

In both modes, the key is changed in matrix by S7 and S9 switches KD/KU (referred to as key direction) and S8 and S10 switches SD/SU (referred to as speed direction), as shown in Table 1 and 2.

Key direction and speed direction are merely the names to indicate directions on the matrix and do not represent any special functional difference.

Remarks:
Fø indicates no change in musical intervals
(i.e., equal to the input frequency).
F+x indicates that musical intervals become higher by
(semitone X x gradation).
F-x indicates that musical intervals become lower by
(semitone X x gradation).
In the present IC semitone is set at approx. 6.25% and thus the magnitude of change in musical interval is as follows:

$F+x : (1.0625)^x$ (Hz)

$F-x : \frac{1}{(1.0625)^x}$ (Hz)

Key is changed a chromatic per step. Since chromatic corresponds to approx. 6.25% of frequency, key change frequency fo at F+n for the input frequency fi is caluculated by the following equation:

$fo = fi*(1.0625)^n$

For example, fo when fi = 1 kHz and the key is F+3 is as follows:

fo = 1.2 kHz.

Table 1 VMC

	KD4	KD3	KD2	KD1	K0	KU1	KU2	KU3	
TU3	F–7	F–6	F–5	F–4	F–3	F–2	F–1	F0	
TU2	F–6	F–5	F–4	F–3	F–2	F–1	F0	F+1	↑ TU
TU1	F–5	F–4	F–3	F–2	F–1	F0	F+1	F+2	
T0	F–4	F–3	F–2	F–1	F0	F+1	F+2	F+3	
TD1	F–3	F–2	F–1	F0	F+1	F+2	F+3	F+4	↓ TD
TD2	F–2	F–1	F0	F+1	F+2	F+3	F+4	F+5	
TD3	F–1	F0	F+1	F+2	F+3	F+4	F+5	F+6	
				← KD		→ KU			

(Function moves in these directions when switches KD, KU, TD and TU are ON.)

Table 2 VSC

	KD2	KD1	K0	KU1	KU2	
TU12	F–20	F–18	F–16	F–14	F–12	
TU7	F–11	F–9	F–8	F–7	F–5	↑ TU
TU4	F–6	F–5	F–4	F–3	F–2	
TU2	F–4	F–3	F–2	F–1	F0	
T0	F–2	F–1	F0	F+1	F+2	↓ TD
TD3	F+1	F+2	F+3	F+4	F+5	
TD7	F+5	F+7	F+8	F+9	F+11	
TD12	F+13	F+14	F+16	F+18	F+20	
		← KD		→ KU		

Same operation is made in both of key direction and speed direction if the key variation is same in VMC or VSC mode. However, for equal variation, VMC provides higher sound quality with low distortion and noise than VSC does.

Pressing KD and KU at the same time sets the key direction to KO.Pressing TD and TU at the same time sets the speed direction to SO.With "H"(5 VDC)applied to either pin 46 KEY/TEMP DOWN or pin 47 KEY/TEMP UP, both key and speed directions are set to KO and SO.

(8) Key scan

Up and down of key and speed is controlled by inputting scan signal output from pin ㊹ SCAN and pin ㊺ $\overline{\text{SCAN}}$ to pin ㊻ KEY/TEMP DOWN and pin ㊼ KEY/TEMP UP.

They have chattering prevention function against pushbutton switches.

Chattering prevention period is approx. 32ms logically. Since one point change only one point even if the switch is kept being pressed.

To control these switches using microcomputer, etc., it is necessary to use transister switchese. Example is shown in Fig.1.

Time to turn the switch ON and inteval between ON's should be set to 100ms or more to avoide the chattering prevention period securely.

They should also be set to 100ms or more for the abovementioned simultaneous pressing of switches and K0 and S0 setting by application of "H" voltage.

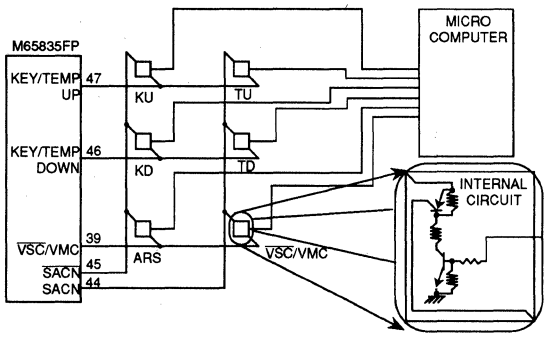


Fig. 1 Example control by a microcomputer

Note: When transistor switches are used, there is no need for diodes to prevent signal interference.When transistor switches are used together with mechanical switches and wired short, diodes must be inserted on the sides of the mechanical switches and wired short. Fig. 2 shows such a case.

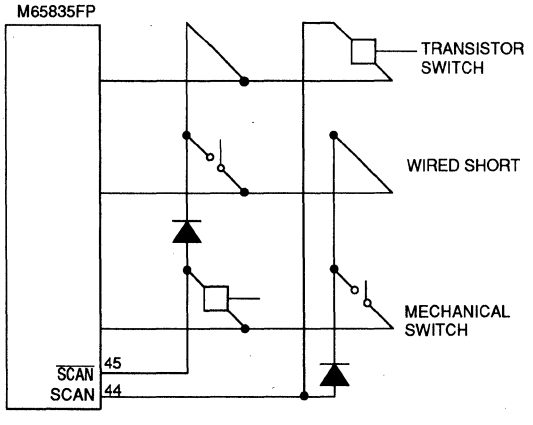


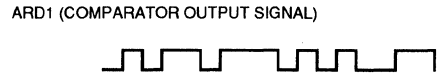
Fig. 2 Anti-interference measure

(9) Auto reset

Auto reset is function to set the key direction to K0 and the speed direction to S0 automatically when an interval between tunes is detected by the input to ARD1.

Output is signal from the comparator is input to ARD1.

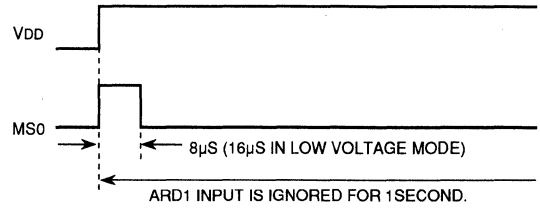
Signal as shown in the following is input when a tune is being played.



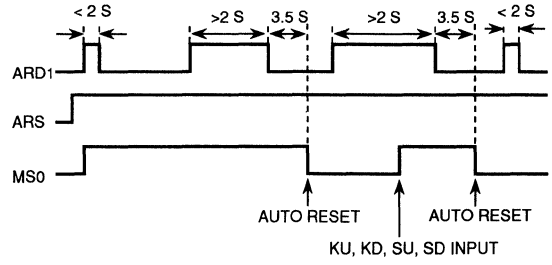
No signal state is detected if the signal level is "L" for 2 seconds and interval is detected if it is "L" for further 1.5 seconds.

Accordingly, auto reset is activated when "L" signal for 3.5 seconds in total is detected.

a) Input to ARD1 for 1 second is ignored when the power is turned ON.

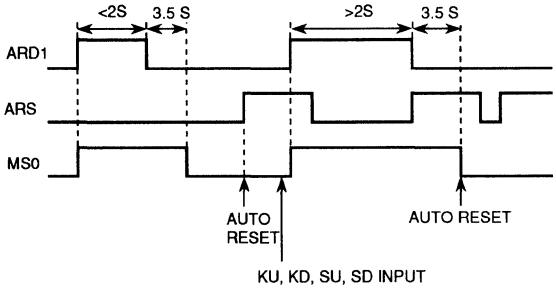


b) Timing during normal operation is as shown in the following figure.



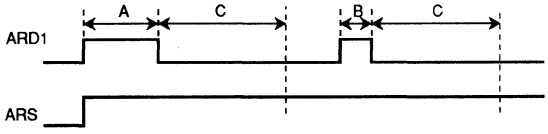
It is judged that a tune is being played when the ARD1 input is "H" for 2 or more seconds, and if no signal is detected for 3.5 or more seconds after that, auto reset is made. When auto reset is made, MS0 output "L". If the key is changed by any key input of KU, KD, SU or SD, "H" is input to ARD1 and MS0 also outputs "H".

c) Operation of auto reset for ARS change is shown in the following figure



Auto reset is not made ARS is "L". The internal flag is however definite. Therefore, auto reset is made at the point when ARS is changed to "H".

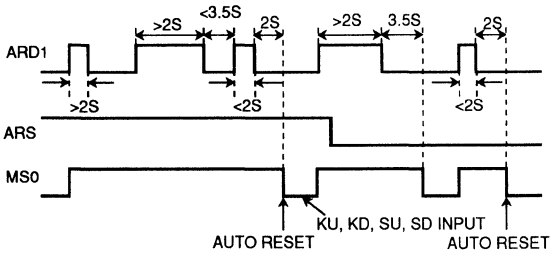
d) Operation when a key input is made (Key direction or speed direction) is shown in the following figure.



A; 2 SECONDS B; SHORTER THAN 2 SECONDS
C; 3.5 SECONDS

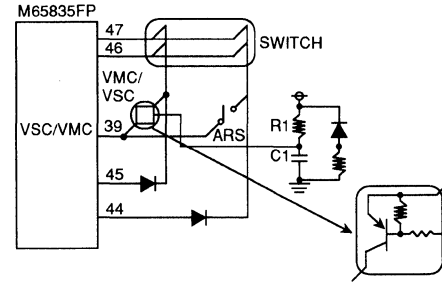
When an effective key input is made, flag to cancel auto reset is cleared each time when ARD1="H" is satisfied for 2 seconds. Accordingly, auto reset is made if an effective key input is made in period A, but it is not made even if any effective key input is made in period B or C.

e) Affection by noise shown in the following figure.



As shown in the figure, when ARD1 is "H" for 2 or more seconds and then "H" is input for shorter than 2 seconds, auto reset is made undersirably in 2 seconds after the "H" input. Therefore, if a noise of shorter than 2 seconds is periodically input at an interval of 2 seconds, auto reset timing is postponed.
In the following section, precautions on using auto reset in VMC mode are described.
VMC and VSC mode setting is read in when reset is canceled. ARS switch and VMC control (TCS) switches are connected to the same pin ㊴. When using auto reset in VMC mode, VMC mode should be selected by turning the TCS switch ON when resetting, and TCS switch shold be turned OFF and ARS switch ON during normal operation.

If TCS switch is not turned OFF, inputting of ARS switch is regarded as double pressing and auto reset is not activated. Circuit where countermeasure for this is taken is shown in the following figure.

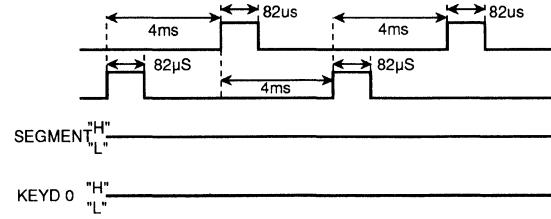


Set the time constance for R1 and C1 sufficiently larger than the time constance for reset signal.
VMC mode is allowed to be recognized by delaying the timing in scanning using the capacitor and the resister.

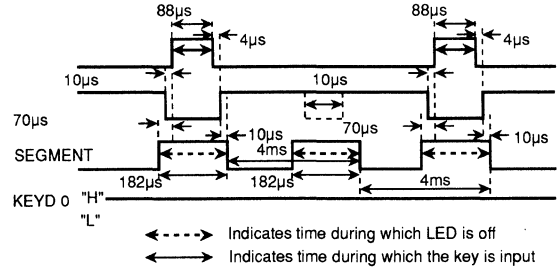
(10) LED drive

To display the key direction, pin ㊽ KEYD0, pin ㊵ KEYD2, pin ㊶ KEYD2, pin ㊷ KEYD3, pin ㊸ KEYD4 and scan signal output pins ㊹ SCAN and ㊺ SCAN are used. When the key direction is at center (K0), pin ㊽ KEYD0 is "L" and the LED is lit statically. When it is not at center (K0), pin ㊹ is "H" and the LED is dynamically lit according to pin ㊵~㊸ and the scan signal output pins ㊹ and ㊺.
Timing for dynamic lighting is as shown in the following figure.

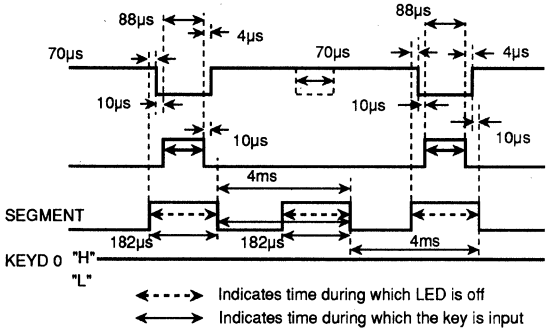
a) The diagram below indicates the timing when the key direction is toward the center.



b) The diagram below indicates the timing when the key direction is upward.



c) The diagram below indicates the timing when the key direction is downward.



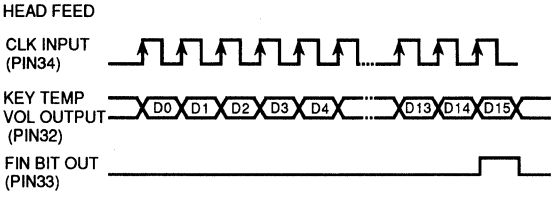
Note: Time indicated in this diagram is dislocated by 160 μs at most when interruption occurs and by several 10 μs in the key direction.

(11) Vocal cutoff circuit operation

Vocal cutoff can be actuated by controlling pin ㉜ (VCUT SW).

SW polarity	Vocal cutoff operation
L	OFF (through output)
H	ON

(12) Relationship between serial data and clock key, tempo and volume information is made serial by switching the incorporated mutiplexer and output from pin ㉜. (The multiplexer can be switched by inputting the clock via pin ㉞.)



Data serially output is set as follows.

D0: key information	D8 : microphone volume
D1: 〃	D9 : 〃
D2: 〃	D10 : 〃
D3: 〃	D11 : echo volume
D4: 〃	D12 : 〃
D5: tempo information	D13 : 〃
D6: 〃	D14 : free data (continually outputs "L")
D7: 〃	D15 : 〃

The present IC does not incorporate a register.
Therefore, key UP/ DOWN and volume UP/DOWN operation during data output causes information different from the IC interior setting to be output.

key information

	D0	D1	KD2	KD1	K0
F−20	L	L	L	L	L
F−18	L	L	L	L	H
F−16	L	L	L	H	L
F−14	L	L	L	H	H
F−13	L	L	H	L	L
F−12	L	L	H	L	H
F−11	L	L	H	H	L
F − 9	L	L	H	H	H
F − 8	L	H	L	L	L
F − 7	L	H	L	L	H
F − 6	L	H	L	H	L
F − 5	L	H	L	H	H
F − 4	L	H	H	L	L
F − 3	L	H	H	L	H
F − 2	L	H	H	H	L
F − 1	L	H	H	H	H
F 0	H	L	L	L	L
F + 1	H	L	L	L	H
F + 2	H	L	L	H	L
F + 3	H	L	L	H	H
F + 4	H	L	H	L	L
F + 5	H	L	H	L	H
F + 6	H	L	H	H	L
F + 7	H	L	H	H	H
F + 8	H	H	L	L	L
F + 9	H	H	L	L	H
F+11	H	H	L	H	L
F+13	H	H	L	H	H
F+14	H	H	H	L	L
F+16	H	H	H	L	H
F+18	H	H	H	H	L
F+20	H	H	H	H	H

Tempo information

(In VMC mode)

	D5	D6	D7
TD 3	L	L	H
TD 2	L	H	L
TD 1	L	H	H
T 0	H	L	L
TU 1	H	L	H
TU 2	H	H	L
TU 3	H	H	H

(In VSC mode)

	D5	D6	D7
TD 12	L	L	L
TD 7	L	L	H
TD 3	L	H	L
T 0	L	H	H
TU 2	H	L	L
TU 4	H	L	H
TU 7	H	H	L
TU 12	H	H	H

Microphone volume information

	D8	D9	D10
−∞dB	L	L	L
−15dB	L	L	H
−10dB	L	H	L
−6dB	L	H	H
−3dB	H	L	L
0dB	H	L	H
+3dB	H	H	L
+6dB	H	H	H

Echo volume information

	D11	D12	D13
−∞dB	L	L	L
−15dB	L	L	H
−10dB	L	H	L
−8dB	L	H	H
−6dB	H	L	L
−4dB	H	L	H
−2dB	H	H	L
0dB	H	H	H

D14 and 15 always take L level.

TEST CONDITIONS

Block name	Symbol	Parameter	Input	Output	Switch conditions 23	24	25	26	27	28	31	52	SW29	SW30	SW39	SW40	Remarks
Total system	Icc	Circuit current	—	—	L	L	H	H	L	H	L	L	—	—	(2)	(2)	No signals present
Line	CS	Channel separation	Vi 93	Vo 94	↓	↓	↓	L	↓	↓	↓	↓	—	—	↓	↓	DIN-AUDIO
			Vi 97	Vo 90	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
			Vi 93	Vo 85	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
	Gv	I/O voltage gain	Vi 97	Vo 94	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
			Vi 93	Vo 90	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
			Vi 88	Vo 85	↓	↓	↓	L	↓	H	↓	↓	—	—	↓	↓	
	Gv	I/O voltage gain (MIX)	Vi 98	Vo 94	↓	↓	↓	H	↓	L	↓	↓	—	—	↓	↓	
			Vi 98	Vo 90	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
			Vi 98	Vo 85	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
			Vi 97,93	Vo 89	↓	↓	↓	H	↓	L	↓	↓	—	—	↓	↓	
	V_{omax}	Maximum output voltage	Vi 97	Vo 94	↓	↓	↓	L	↓	H	↓	↓	—	—	↓	↓	THD=0.1%
			Vi 93	Vo 90	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
			Vi 88	Vo 85	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
	No	Output noise voltage	—	Vo 94	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	DIN-AUDIO, Rg=620Ω and no signals
			—	Vo 90	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
			—	Vo 85	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
	THD	Output distortion factor	Vi 97	Vo 94	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	30kHz LPF
			Vi 93	Vo 90	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
			Vi 88	Vo 85	↓	↓	↓	↓	L	↓	↓	↓	—	—	↓	↓	
	f_R	Bass boost roll-off frequency	Vi 97	Vo 94	↓	↓	↓	↓	H	↓	↓	↓	—	—	↓	↓	
			Vi 93	Vo 90	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
			Vi 88	Vo 85	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
	G_{vB}	Bass boost voltage gain	Vi 97	Vo 94	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	f=100Hz
			Vi 93	Vo 90	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
			Vi 88	Vo 85	↓	↓	↓	↓	H	↓	↓	↓	—	—	↓	↓	
	V_{PB}	Bass boost switching noise voltage	—	Vo 94	↓	↓	↓	↓	L⇔H	↓	↓	↓	—	—	↓	↓	DIN-AUDIO and no signals present
			—	Vo 90	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
			—	Vo 85	↓	↓	↓	L	L⇔H	↓	↓	↓	—	—	↓	↓	
	V_{PL}	Line switching noise voltage	—	Vo 94	↓	↓	↓	H⇔L	L	↓	↓	↓	—	—	↓	↓	DIN-AUDIO and no signals present
			—	Vo 90	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	
			—	Vo 85	↓	↓	↓	H⇔L	↓	H	↓	↓	—	—	↓	↓	
			—	Vo 89	L	L	H	H	L	H⇔L	L	L	—	—	(2)	(2)	

Block name	Symbol	Parameter	Input	Output	Switch conditions												Remarks	
					23	24	25	26	27	28	31	52	SW29	SW30	SW39	SW40		
Echo	GV	I/O voltage	Vi 12	Vo 4	L	L	H	H	L	H	L	L	—	—	(2)	(2)		
	V_{imax}	Maximum input voltage															THD=10%	
	NO	Output noise voltage	—														DIN-AUDIO and no signals present	
	THD	Output distortion factor	Vi 12														30kHz LPF	
	TD	Delay time																
Search	VDET	Internal detection sensitivity	Vi 14	Pin ⑯	L	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	Pin ⑯ output	Note 1
	V_{CTL}	CLT input voltage	Vi 20	Vo 21	H	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	GND reference	Note 2
	V_{CTLNO}	CLT noise protect level																Note 3
	TC	No. of tune detection pulses	Vi 14 Vi 20	Vo 21 Vo 22	L	↓	H	↓	↓	↓	↓	↓	—	—	↓	↓	Pin ㉕=H; 4096 or more pulses	Note 4
					↓	L	L	↓	↓	↓	↓	↓	—	—	↓	↓	Pin ㉕=L; 8192 or more pulses	
	TD	Tune interval detection time			↓	H	H	↓	↓	↓	↓	↓	—	—	↓	↓	Pin ㉔=H; 90±2 bits	Note 5
					↓	L	↓	↓	↓	↓	↓	↓	—	—	↓	↓	Pin ㉔=L; 110±2 bits	
	TW	No. of VISS output pulses			↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓		Note 6
	DVISS	VISS duty			↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓		Note 7
	DSOUT	Search OUT duty			L	L	H	H	L	H	L	L	—	—	(2)	(2)		Note 8

Note 1. Input sine wave (f = 10 kHz) from vi14 and measure pin ⑯.

2. Input pulses or sine wave (f = 100 Hz; 1.8 Vpp) from vi20: If pulses generate from Vo21, operation is normal.

3. Input pulses or sine wave (f = 100 Hz; 1.8 Vpp) from vi20. If pulses do not generate from Vo21, operation si normal.

4. Input Vi20 signals as in Note 2 above so as to temporarily generate VISS (duty 25±5%). (This is because the operation after power ON is in the tune detection mode.) Stop Vi20 input and change pin ㊾ REF from GND to OPEN. (Internal reset)
   Input signals as in Notes 1 and 2 at the same time.
   When 4096 or 8192 or more pulses (choose either depending on the polarity of pin ㉕) have finishied being input, stop Vi14 input only. If VIss generates from pin ㉑ (duty 25±5%), operation is normal.

5. Follow the same procedures as in Note 4 and count control pulses (Vi20) from when Vi14 inut is stopped until the moment VISS (duty 25±5%) generates or pin ㉒ changes from L to H.

6. Count pulses when VISS (duty 25±5%) generates.

7. Measure VISS (duty 25 ±5%) signal duty ratio.

8. Measure pin ㉑ output pulse duty ratio during other periods than when VISS (duty 25±5%) generates.

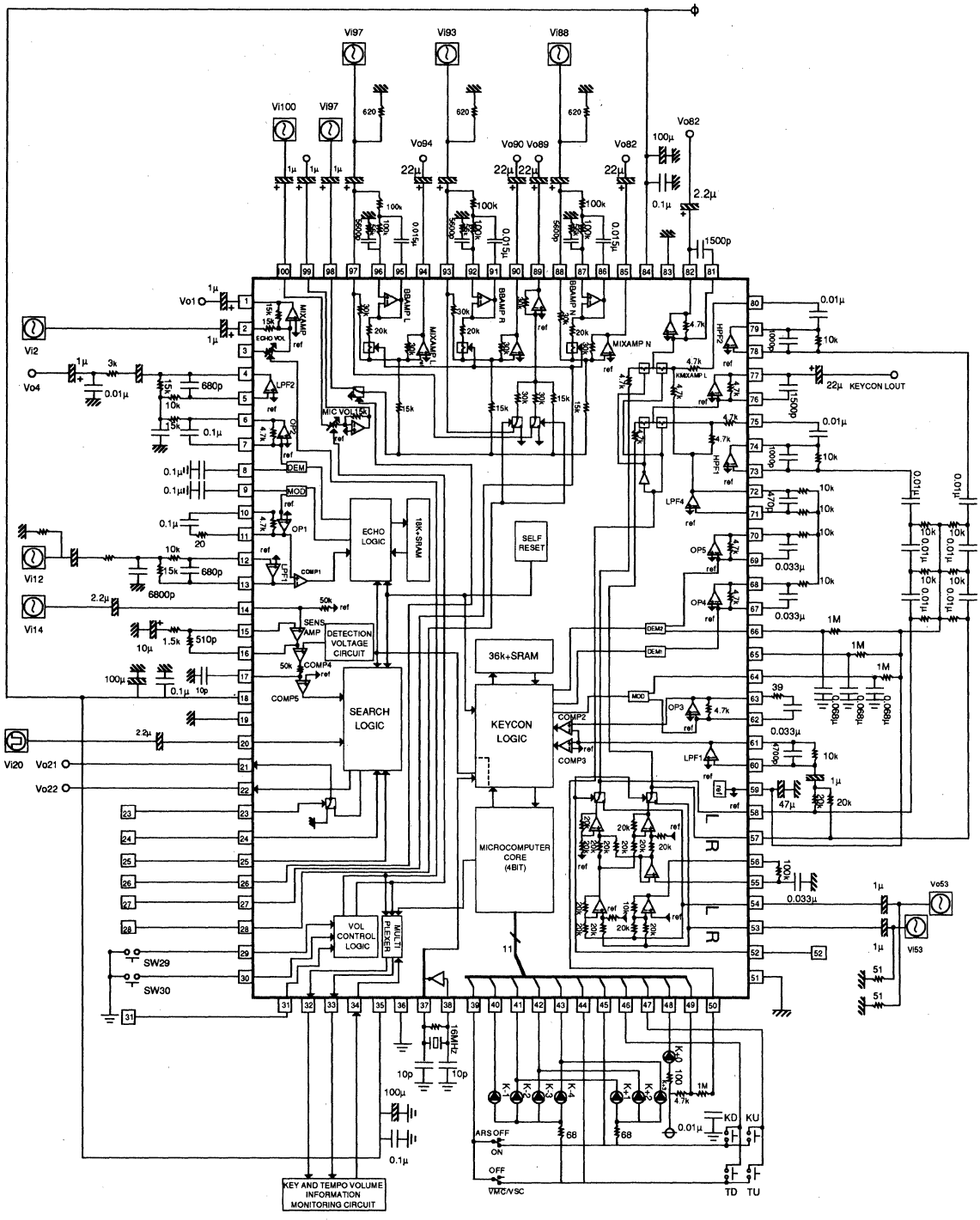
Block name	Symbol	Parameter	Input	Output	Switch conditions 23	24	25	26	27	28	31	52	SW29	SW30	SW39	SW40	Remarks	
Key control	NOM	Output noise voltage (VMC)	—	Vo 77	L	L	L	H	L	L	L	L	—	—	(2)	(2)	F0(T0,K0), DIN-AUDIO and Rg=51Ω	Note 9
			—	Vo 82	↓	↓	↓	↓	↓	↓	↓	↓	—	—	(2)	↓		
	NOS	Output noise voltage (VSC)	—	Vo 77	↓	↓	↓	↓	↓	↓	↓	↓	—	—	(1)	↓	F0(T0,K0), DIN-AUDIO and Rg=51Ω	
			—	Vo 82	↓	↓	↓	↓	↓	↓	↓	↓	—	—	(1)	↓		
	THDM	Total harmonic distortion (VMC)	Vi 53	Vo 77	↓	↓	↓	↓	↓	↓	↓	↓	—	—	(2)	↓	F0(T0,K0), 30kHz LPF	
			Vi 54	Vo 82	↓	↓	↓	↓	↓	↓	↓	↓	—	—	(2)	↓		
	THDS	Total harmonic distortion (VSC)	Vi 53	Vo 77	↓	↓	↓	↓	↓	↓	↓	↓	—	—	(1)	↓	F0(T0,K0), 30kHz LPF	
			Vi 54	Vo 82	↓	↓	↓	↓	↓	↓	↓	↓	—	—	(1)	↓		
	GV	I/O voltage gain	Vi 53	Vo 77	↓	↓	↓	↓	↓	↓	↓	↓	—	—	(2)	↓		
			Vi 54	Vo 82	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓		
	VOMAX	Maximum output voltage	Vi 53	Vo 77	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	THD=10%, 30kHz LPF	
			Vi 54	Vo 82	↓	↓	↓	↓	↓	↓	↓	L	—	—	↓	↓		
Vocal cutoff	NO	Output noise voltage	—	Vo 57	↓	↓	↓	↓	↓	↓	↓	H	—	—	↓	↓	DIN-AUDIO, Rg=51Ω	
			—	Vo 58	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓		
	GV	I/O voltage gain	Vi 53	Vo 57	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	Input via single channel	
			Vi 54	Vo 58	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓		
	VOMAX	Maximum output voltage	Vi 53	Vo 57	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	Input via single channel, THD=10%, 30kHz LPF	
			Vi 54	Vo 58	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓		
	GVREJ	Vocal cutoff removal ratio	Vi 53,54	Vo 57,58	↓	↓	↓	↓	↓	↓	↓	H	—	—	↓	↓	L and R input	
Echo volume	GVE 0	I/O voltage gain 0	Vi 3	Vi 1	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	Voltage gain 0 dB set	Note 10
	−2	−2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	−2	
	−4	−4	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	−4	
	−6	−6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	−6	
	−8	−8	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	−8	
	−10	−10	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	−10	
	−15	−15	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	−15	
	↓ −∞	↓ −∞	Vi 3	Vi 1	↓	↓	↓	↓	↓	L	↓	↓	—	—	↓	↓	↓ −∞	
Microphone volume	GVE 6	I/O voltage gain 6	Vi 100	Vi 99	↓	↓	↓	↓	↓	H	↓	↓	—	—	↓	↓	Voltage gain 6 dB set	Note 11
	3	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	3	
	0	0	↓	↓	↓	↓	↓	↓	L	L	L	↓	—	—	↓	↓	0	
	−3	−3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	−3	
	−6	−6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	−6	
	−10	−10	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	−10	
	−15	−15	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	—	—	↓	↓	−15	
	↓ −∞	↓ −∞	Vi 100	Vi 99		L	L	H		H	L	L		—		(2)	↓ −∞	

Note 9. For VMC/VSC switching, turn the present IC power OFF first. Then switch the mode and turn power ON.

10. When pin ㉛ ECHO/MIC SW is "L", press SW29 and SW30 to turn echo volume up/down.

11. When pin ㉛ ECHO/MIC SW is "H", press SW29 and SW30 to turn microphone volume up/down.

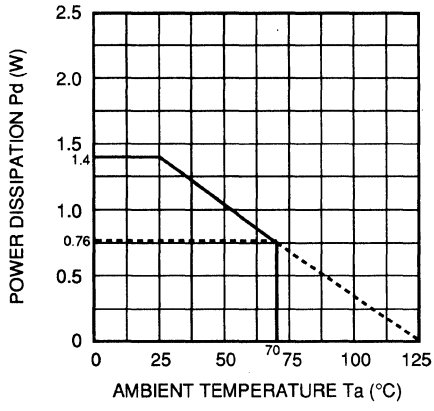
TEST CIRCUIT



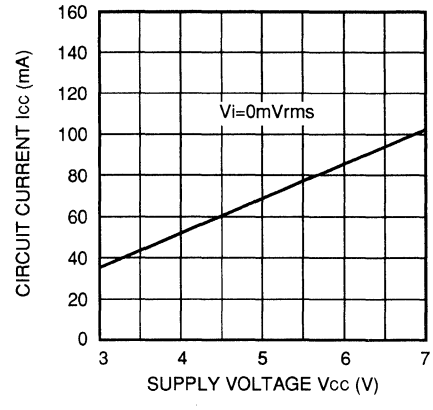
MITSUBISHI ELECTRIC

TYPICAL CHARACTERISTICS

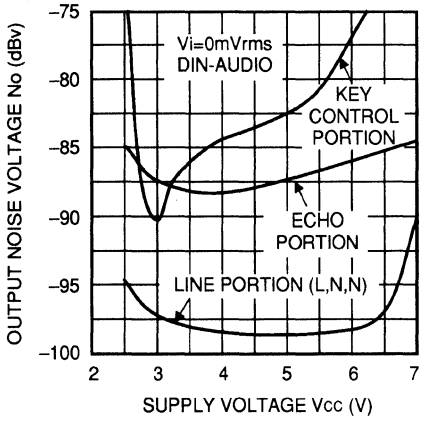
THERMAL DERATING (MAXIMUM RATING)



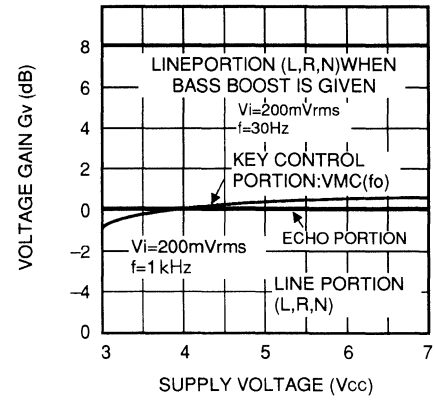
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



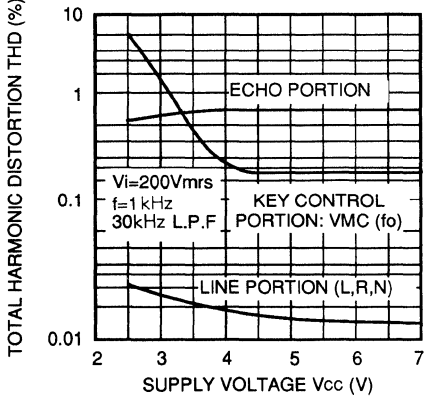
OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



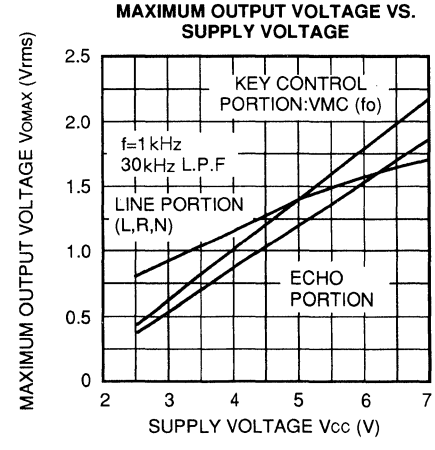
VOLTAGE GAIN VS. SUPPLY VOLTAGE



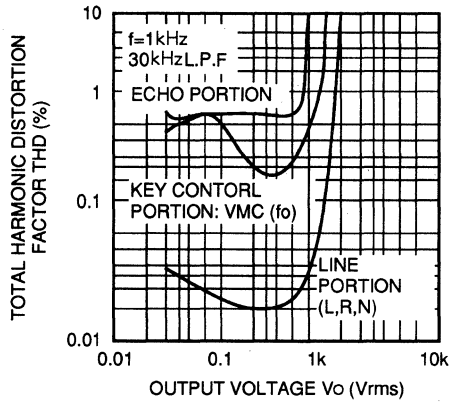
TOTAL HARMONIC DISTORTION VS. SUPPLY VOLTAGE



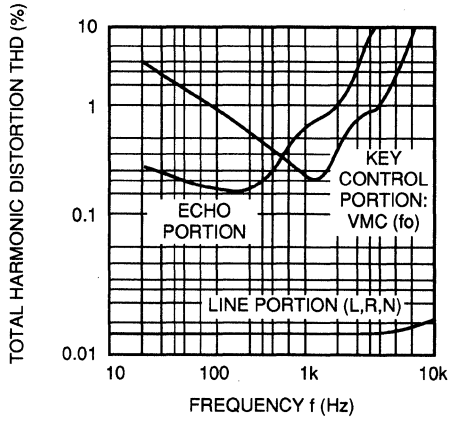
MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



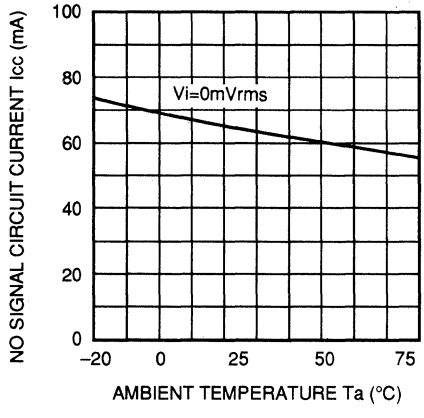
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



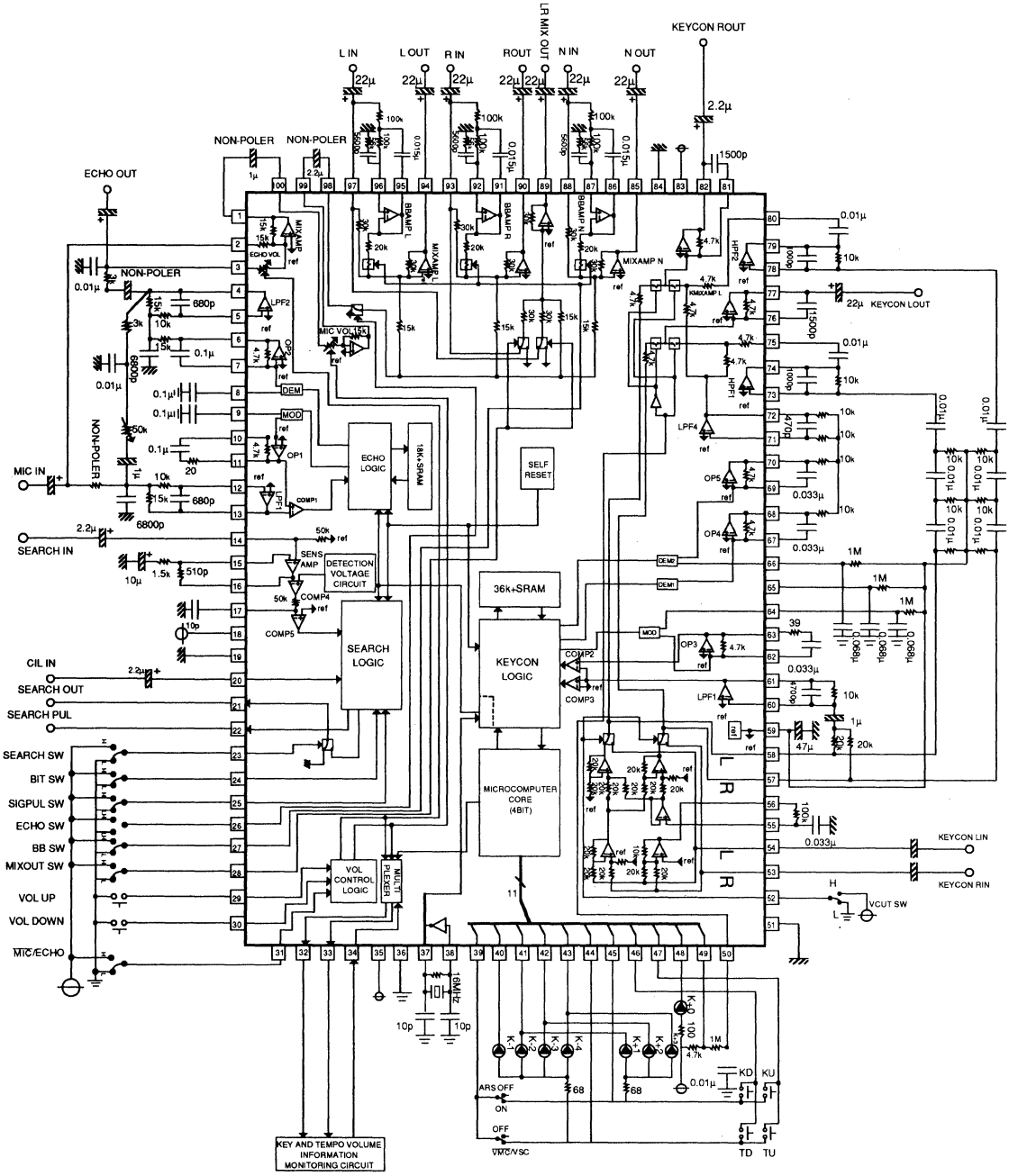
TOTAL HARMONIC DISTORTION VS. FREQUENCY



NO SIGNAL CIRCUIT CURRENT VS. AMBIENT TEMPERATURE

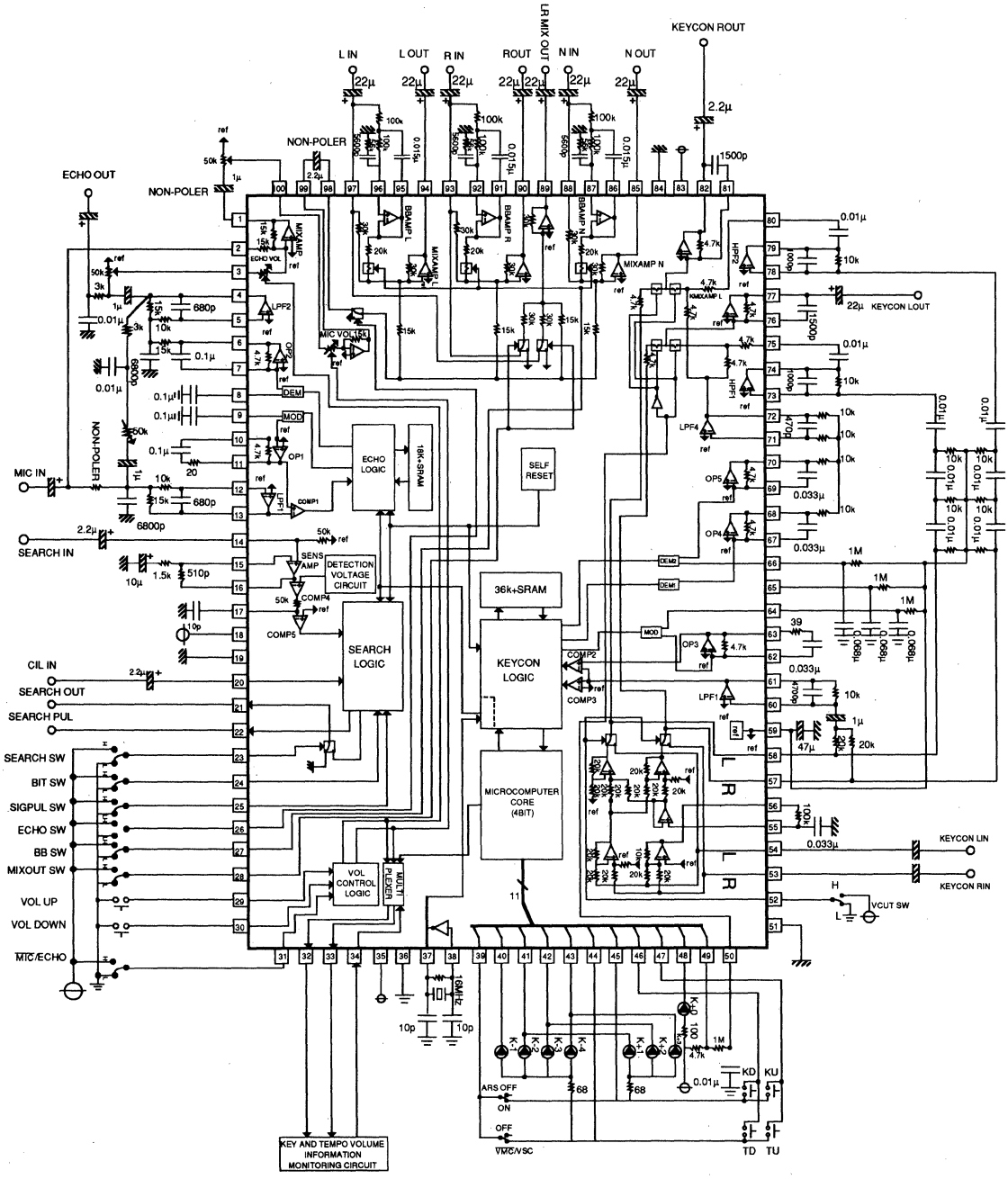


APPLICATION EXAMPLE



APPLICATION EXAMPLE

Built-in volume



M65839SP,FP

DIGITAL ECHO WITH BUILT-IN MICROPHONE MIXING CIRCUIT

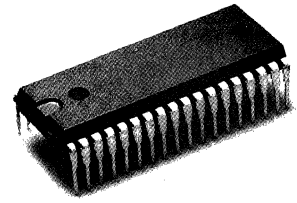
DESCRIPTION

The M65839 is a CMOS IC having microphone peripheral circuits of "Karaoke" equipment packaged on a single chip.

It contains not only an echo generator for voice through microphones but also ALC-equipped microphone amplifiers, microphone volumes, echo volumes, and line-mixing amplifiers, enabling reduction in the number of external parts and in the packaging area.

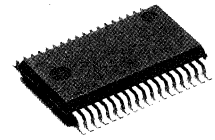
FEATURES

- Two microphone-mixing lines, microphone volumes, echo volume, digital echo, and line-mixing amplifiers are contained, enabling microphone peripheral circuits of "karaoke" equipment to be packaged on one chip
- Low noise due to digital echo with 16k-bit RAM
- High-performance microphone volumes and echo volume due to combined resistance-ladder attenuator and A/D converter (allowing serial control from microcomputer)
- Adaptable to excessively high input due to ALC-equipped microphone amplifiers
- Single 5V power supply
- Built-in auto power-ON reset circuit



Outline 36P4E(SP)

1.778mm pitch 500mil SDIP
(11.0mm × 31.5mm × 3.8mm)



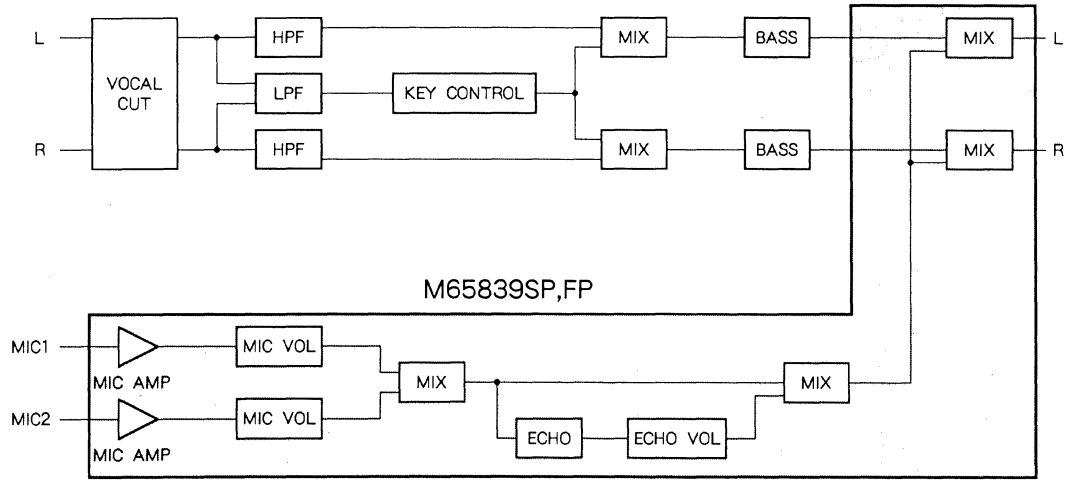
Outline 36P2R-A(FP)

0.8mm pitch 450mil SSOP
(8.4mm × 15.0mm × 2.0mm)

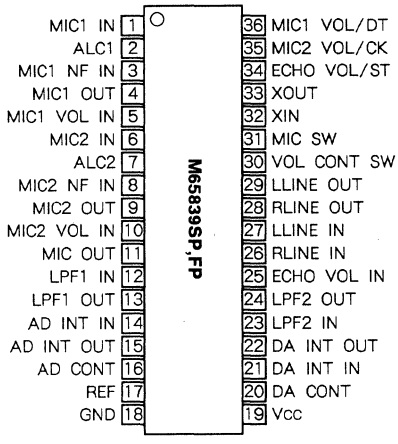
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 4.5~5.5V
Rated supply voltage ..... V_{CC} = 5V

SYSTEM CONFIGURATION

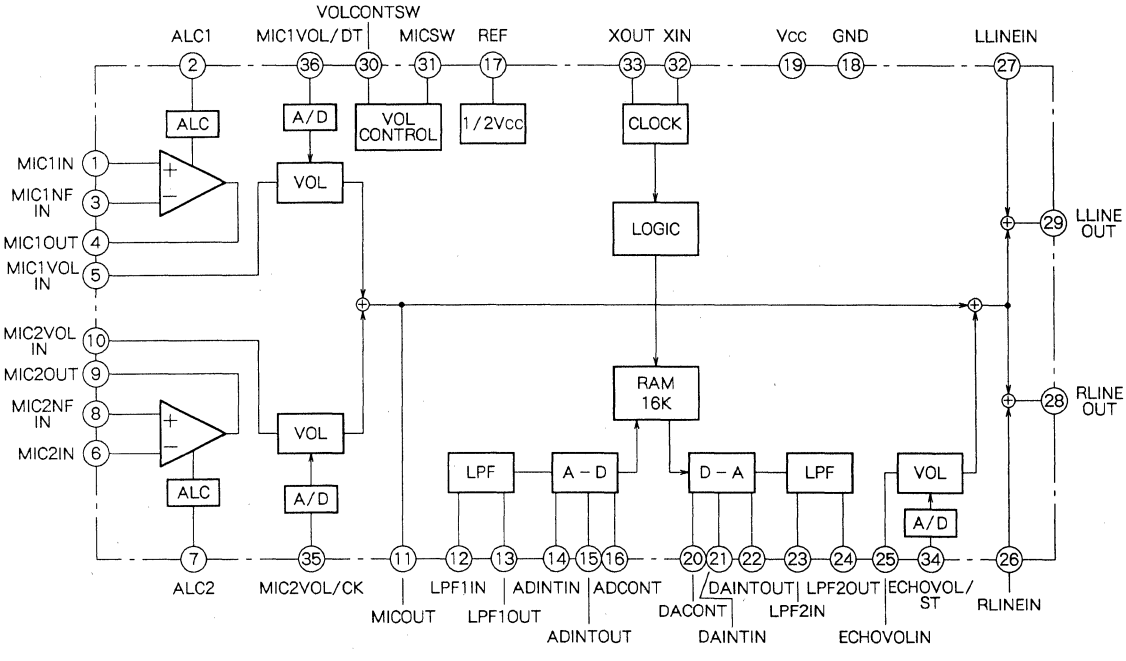


PIN CONFIGURATION



Outline 36P4E(SP)
36P2R-A(FP)

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin No.	Symbol	Name	Function	
①	MIC1IN	Microphone 1 input	To connect MIC1	
②	ALC1	ALC1 control	To connect ALC attack/recovery time setting capacitor	
③	MIC1NFIN	Microphone 1 negative feedback input	To set amplifier gain of MIC1 by feedback circuit	
④	MIC1OUT	Microphone 1 outpt		
⑤	MIC1VOLIN	Microphone 1 volume input	To connect capacitor to reduce noise generated at time of volume change	
⑥	MIC2IN	Microphone 2 input	To connect MIC2	
⑦	ALC2	ALC2 control	To connect ALC attack/recovery time setting capacitor	
⑧	MIC2NFIN	Microphone 2 negative feedback input	To set amplifier gain of MIC2 by feedback circuit	
⑨	MIC2OUT	Microphone 2 output		
⑩	MIC2VOLIN	Microphone 2 volume input	To connect capacitor to reduce noise renerated at time of volume change	
⑪	MICOUT	Microphone output	Mixing output of MIC1 and MIC2	
⑫	LPF1IN	Low-pass filter 1 input	Digital echo pre-filter before A/D conversion	
⑬	LPF1OUT	Low-pass filter 1 output		
⑭	ADINTIN	A/D integrator input	To form A/D conversion integrator by connecting external capacitor	
⑮	ADINTOUT	A/D integrator output		
⑯	ADCONT	A/D control	To determine adaptive time constant of A/D converter with ADM system	
⑰	REF	Reference power output	To connect 1/2 Vcc output and filter capacitor	
⑱	GND	Grounding		
⑲	Vcc	Power supply		
⑳	DACONT	D/A control	To determine adaptive time constant of D/A converter with ADM system	
㉑	DAINTIN	D/A integrator input	To form D/A conversion integrator by connecting external capacitor	
㉒	DAINTOUT	D/A integrator output		
㉓	LPF2IN	Low-pass filter 2 input	Digital echo post-filter before D/A conversion	
㉔	LPF2OUT	Low-pass filter 2 output		
㉕	ECHOVOLIN	Echo volume input	To connect capacitor to reduce noise generated at time of volume change	
㉖	RLINEIN	R-channel line input		
㉗	LLINEIN	L-channel line input		
㉘	RLINEOUT	R-channel line output	Mixing output for microphone system and line	
㉙	LLINEOUT	L-channel line output		
㉚	VOLCONTSW	Volume control system select SW	L : control by DC voltage H : control by serial bus	
㉛	MICSW	Microphone SW	L : MIC OFF H : MIC ON	
㉜	XIN	Clock generator input	To connect 1MHz ceramic filter	
㉝	XOUT	Clock generator output		
			VOLCONTSW = L	VOLCONTSW = H
㉞	ECHOVOL/ST	Echo volume control/strobe	Echo volume control by DC voltage	Strobe input to serial bus
㉟	MIC2VOL/CK	MIC2 volume control/clock	MIC2 volume control by DC voltage	Clock input to serial bus
㊱	MIC1VOL/DT	MIC1 volume control/data	MIC1 volume control by DC voltage	Data input to serial bus

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6.0	V
I_{CC}	Circuit current	100	mA
V_i	Input voltage	−0.3～V_{CC} + 0.3	V
P_d	Power dissipation	1100	mW
T_{opr}	Operating temperature	−20～+75	℃
T_{stg}	Storage temperature	−40～+125	℃

RECOMMENDED OPERATING CONDITIONS

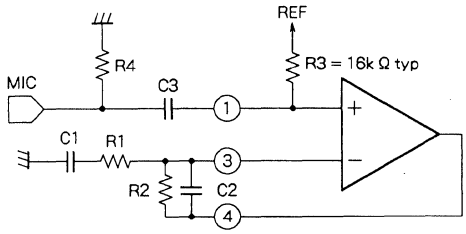
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IL}	Input voltage ("L" level)	Serial bus input	0	−	1	V
V_{IH}	Input voltage ("H" level)	Serial bus input	4	−	V_{CC}	V
f_{ck}	Clock frequency		0.95	1	1.05	MHz

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, f=1kHz, V_i=−15dBm, f_{ck}=1MHz, Ta=25℃, 0dBm=775mVrms, unless othwewise noted)

Block name	Symbol	Parameter	Test conditions	Limits			Unit
				Min	Typ	Max	
Total system	I_{CC}	Circuit current	No signal	−	20	40	mA
Microphone amplifier	G_{VO}	Bare amplifier gain	V_O = − 15dBm	55	60	−	dB
	THD1	Distortion	V_O = − 15dBm, without ALC	−	0.1	0.3	%
	THD2	Distortion	V_i = − 25dBm, with ALC operated	−	3.0	4.5	%
	THD3	Distortion	V_i = − 15dBm, with ALC operated	−	1.8	3.5	%
	V_{OALC}	ALC operating voltage		− 10	− 8	− 6	dBm
	T_{ALCAT}	ALC attack time	C = 4.7μF	25	40	55	msec
	T_{ALCRE}	ALC recovery time	C = 4.7μF	0.4	0.7	1.0	sec
	V_{OMAX}	Maximum output voltage	THD = 10%	1	4	−	dBm
	N_O	Output noise voltage	G_V = 37dB, f = 100～5kHz	−	− 75	− 70	dBm
	Z_i	Input impedance		10	16	25	kΩ
Microphone echo volume	G_V	I/O voltage gain	Volume max.	− 3	0	3	dB
	ATTMAX	Maximum attenuation	Volume min.	−	− 72.5	− 67.5	dB
	THD	Distortion	Volume max.	−	0.02	0.05	%
	V_{iMAX}	Maximum input voltage	THD = 10%, volume center	5	9	−	dBm
	V_{OMAX}	Maximum output voltage	THD = 10%, volume max.	3	7	−	dBm
	N_O	Output noise voltage	JIS-A	−	− 92	− 87	dBm
	Z_i	Input impedance		12	20	32	kΩ
Digital echo	T_d	Delay time	fs = 125kHz	129	131	133	msec
	G_V	I/O voltage gain		− 3	0	3	dB
	THD	Distortion		−	1.3	3	%
	V_{OMAX}	Maximum output voltage	THD = 10%	1	5	−	dBm
	N_O	Output noise voltage	JIS-A	−	− 85	− 70	dBm
Line	G_V	I/O voltage gain		− 3	0	− 3	dB
	THD	Distortion		−	0.02	0.05	%
	V_{OMAX}	Maximum output voltage	THD = 10%	4	8	−	dBm
	N_O	Output noise voltage	JIS-A	−	− 91	− 86	dBm
	Z_i	Input impedance		20	32	50	kΩ

FUNCTION DESCRIPTION

(1) Microphone amplifier



The gain (Gv), low cutoff frequency (fcl) and high cutoff frequency (fch) of microphone amplifier are expressed as follows

$$Gv = \frac{R1 + R2}{R1}, \quad fcl = \frac{1}{2\pi R1 \cdot C1}, \quad fch = \frac{1}{2\pi R2 \cdot C2}$$

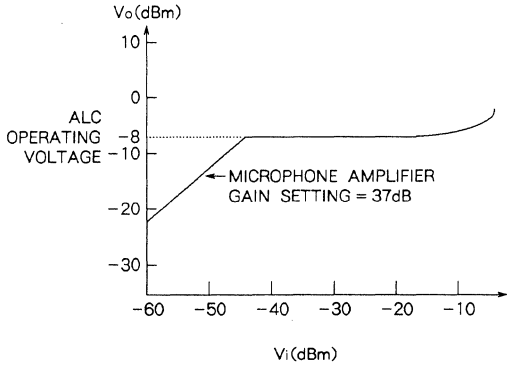
The appropriate value of R2 is 50 to 500kΩ.
Assuming Gv = 37dB, fcl = 210Hz, fch = 5.5kHz, for instance, the constants take following values :

R1 = 2.2k Ω, R2 = 150k Ω, C1 = 0.33 μ F, C2 = 200pF

The low frequency can also be determined by C3 and R3. However, R3 is an internal resistance of LSI and fluctuates largely. Therefore, the low frequency should be set to a value little lower than the low cut-off frequency (fc1), using the smallest R3 value (10kΩ) in the fluctuating range. For the above example, C3 = 0.15μF

To minimize click noise generated when connecting or disconnecting a microphone, it is recommended to connect R4 (600 Ω ~ 10k Ω) in the circuit.

(2) ALC level diagram



(3) Microphone/echo volume

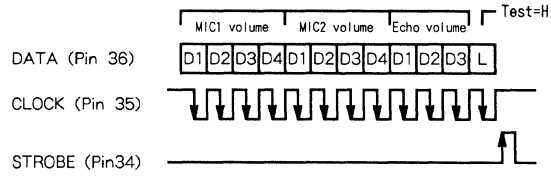
Microphone volume attenuation (Pin 30 = L)

DC voltage control (V)	Serial bus control				Attenuation (dB)
	D1	D2	D3	D4	
5.0	H	H	H	H	0
4.25	H	H	H	L	2
4.0	H	H	L	H	4
3.75	H	H	L	L	6
3.5	H	L	H	H	7
3.25	H	L	H	L	8
3.0	H	L	L	H	9
2.75	H	L	L	L	10
2.5	L	H	H	H	11
2.25	L	H	H	L	12
2.0	L	H	L	H	13
1.8	L	H	L	L	14
1.6	L	L	H	H	16
1.4	L	L	H	L	18
1.2	L	L	L	H	20
1.0	L	L	L	L	∞
0.0					

Echo volume attenuation (Pin 30 = L)

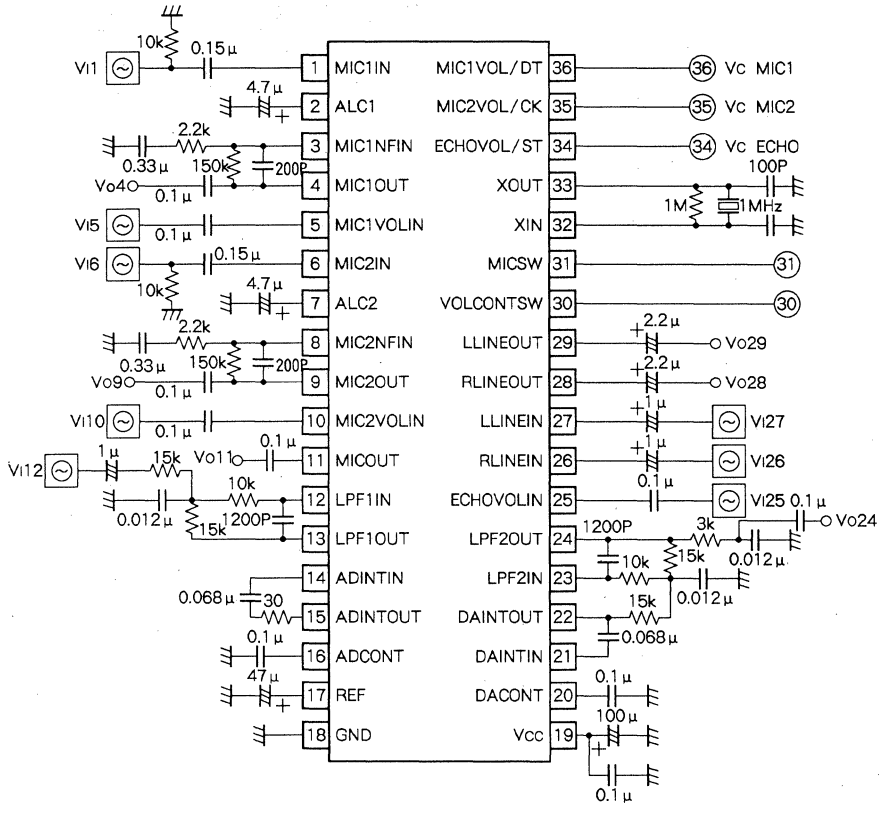
DC voltage control (V)	Serial bus control			Attenuation (dB)
	D1	D2	D3	
5.0	H	H	H	0
4.0	H	H	L	2
3.5	H	L	H	4
3.0	H	L	L	6
2.5	L	H	H	8
2.0	L	H	L	10
1.6	L	L	H	15
1.2	L	L	L	∞
0.0				

Serial bus transfer format (Pin 30 = H)



Microphone volume is set to 10dB, and echo volume to 6dB by auto power-ON reset circuit.(Pin 30 = H)

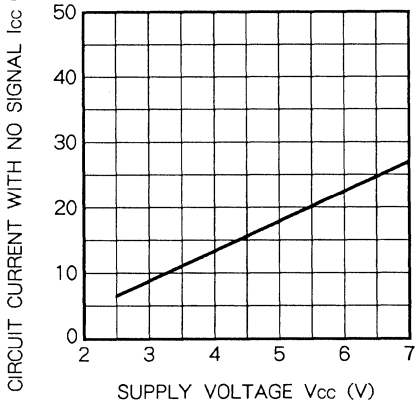
TEST CIRCUIT



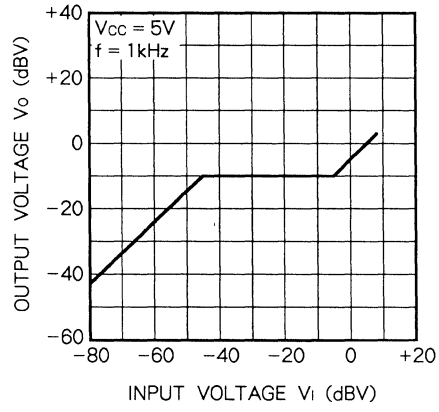
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

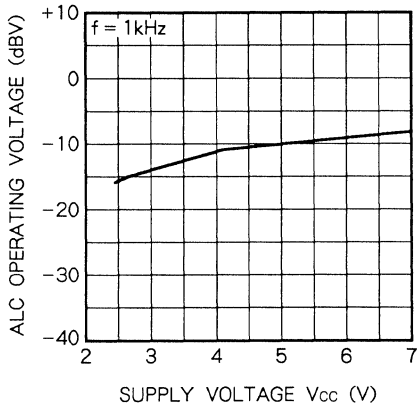
CIRCUIT CURRENT WITH NO SIGNAL VS. SUPPLY VOLTAGE



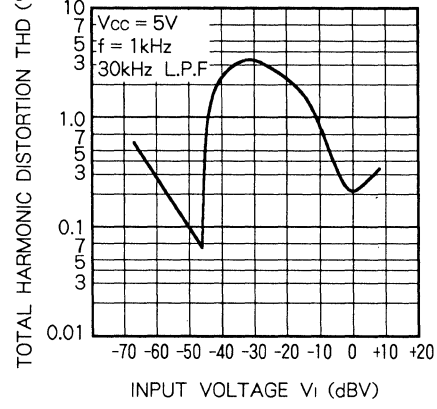
MICROPHONE AMPLIFIER OUTPUT VOLTAGE VS. INPUT VOLTAGE



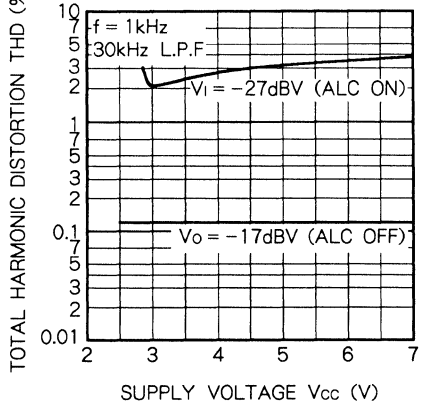
MICROPHONE AMPLIFIER ALC OPERATING VOLTAGE VS. SUPPLY VOLTAGE



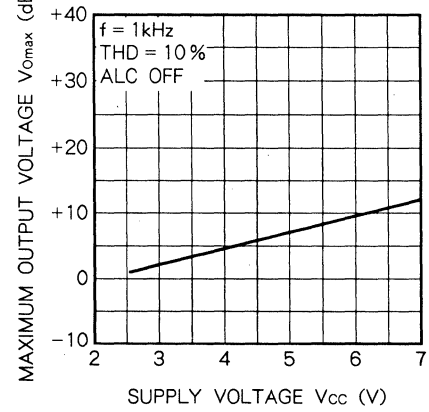
MICROPHONE AMPLIFIER TOTAL HARMONIC DISTORTION VS. INPUT VOLTAGE



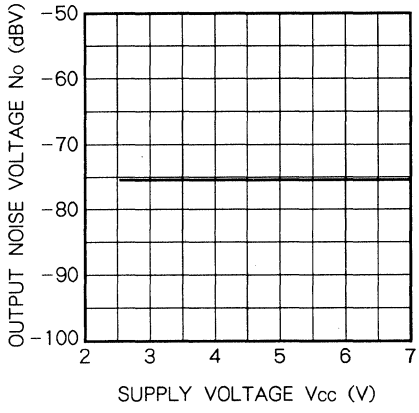
MICROPHONE AMPLIFIER TOTAL HARMONIC DISTORTION VS. SUPPLY VOLTAGE



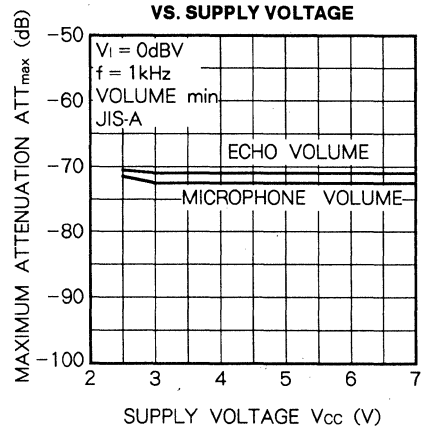
MICROPHONE AMPLIFIER MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



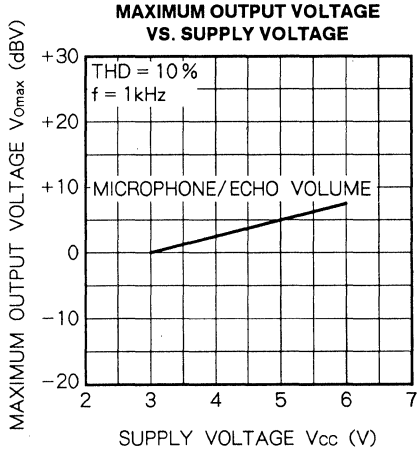
MICROPHONE AMPLIFIER OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



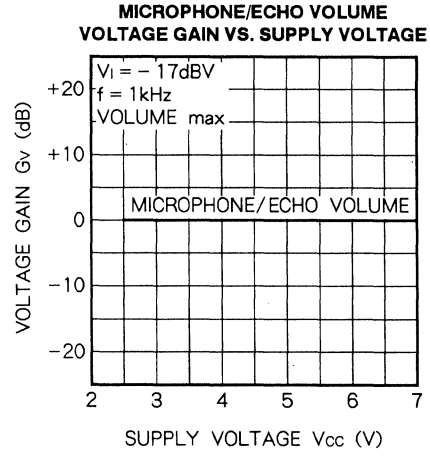
MICROPHONE/ECHO VOLUME MAXIMUM ATTENUATION VS. SUPPLY VOLTAGE



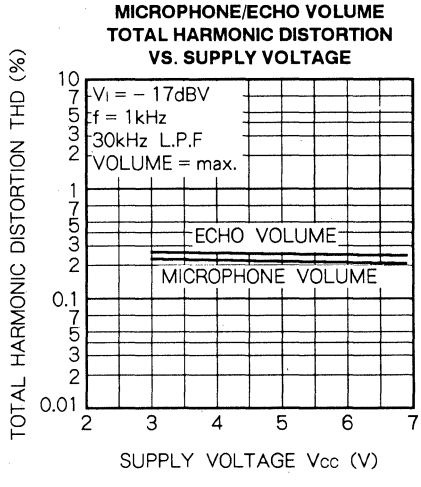
MICROPHONE/ECHO VOLUME MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



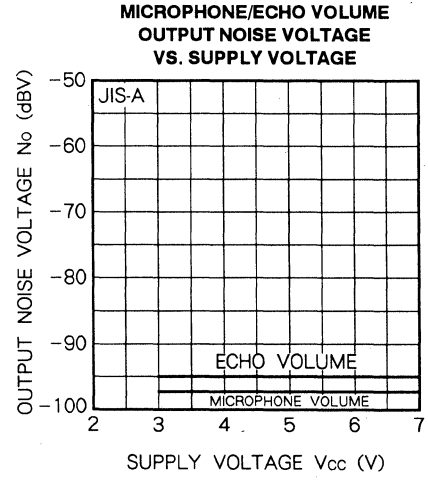
MICROPHONE/ECHO VOLUME VOLTAGE GAIN VS. SUPPLY VOLTAGE



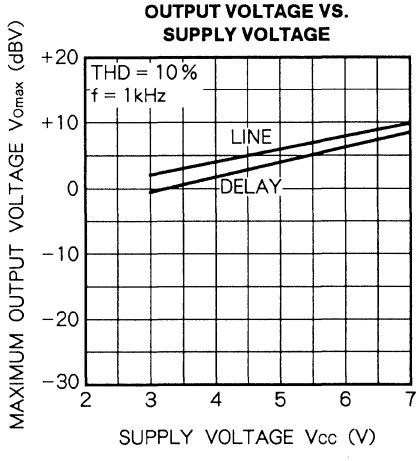
MICROPHONE/ECHO VOLUME TOTAL HARMONIC DISTORTION VS. SUPPLY VOLTAGE



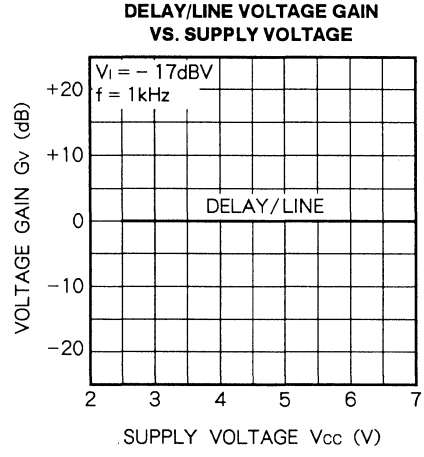
MICROPHONE/ECHO VOLUME OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



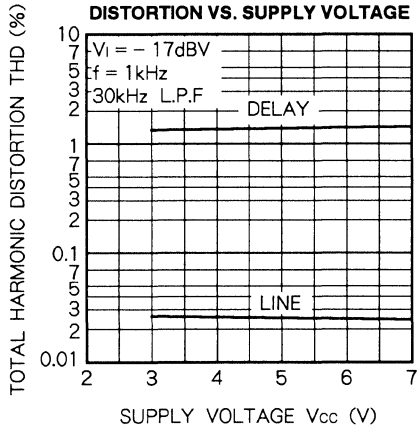
DELAY/LINE MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



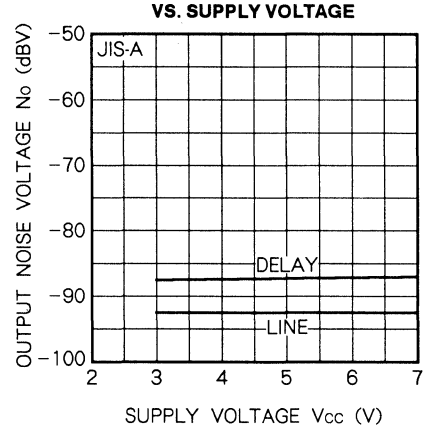
DELAY/LINE VOLTAGE GAIN VS. SUPPLY VOLTAGE



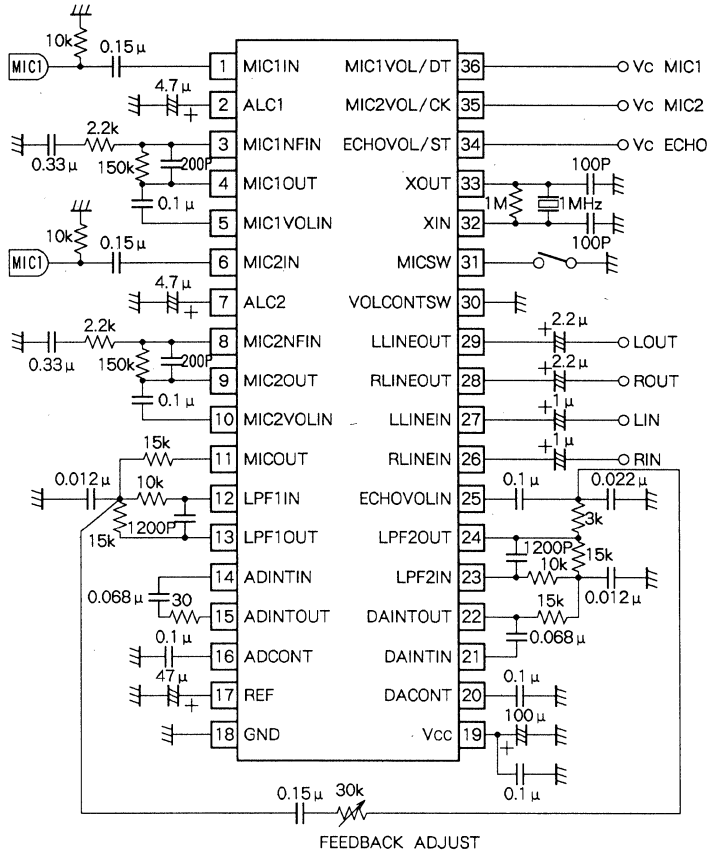
DELAY/LINE TOTAL HARMONIC DISTORTION VS. SUPPLY VOLTAGE



DELAY/LINE OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

M65840SP,FP

SINGLE CHIP DIGITAL KEY CONTROL

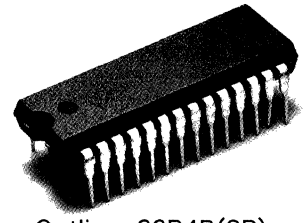
DESCRIPTION

The M65840 is Complementary Metal Oxide Semiconductor Integrated Circuit is used to control the key of music in karaoke* players.

This single chip has all functions necessary for key control.

It is optimal for use in karaoke players, such as radio cassette recorders, mini audio components and video cassette recorders.

* Karaoke : Recorded music to accompany live singing



Outline 28P4B(SP)

1.778mm pitch 400mil SDIP
(8.9mm × 28.0mm × 3.8mm)

Outline 28P2W-A(FP)

1.27mm pitch 450mil SOP
(8.4mm × 17.5mm × 2.0mm)

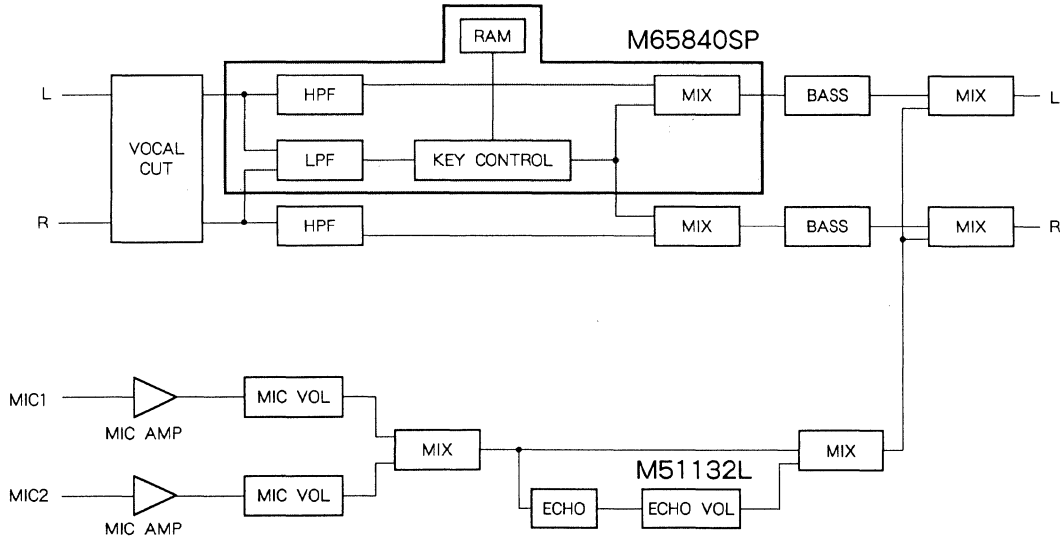
FEATURES

- All functions necessary for digital key control, such as input/output low-pass filter, A-D, D-A converter, 32k-bit SRAM and control logic circuit, are built in one chip
- Low noise by digital key control
  Output noise voltage ····· − 84dBm (typ)
- Key is controlled in 32 steps from − 20 ~ + 20 by microcomputer (One point corresponds to a semitone.)
- Single power supply (5V)
- Built-in automatic reset circuit (The IC is reset as power is turned on.)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC} = 4.5~5.5V
Rated supply voltage ····· V_{CC} = 5V

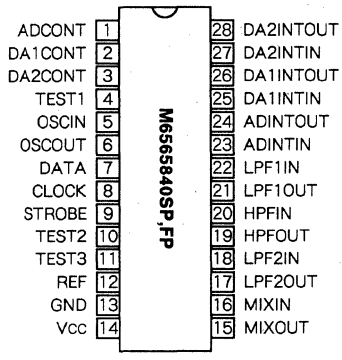
SYSTEM CONFIGURATION



M65840SP,FP

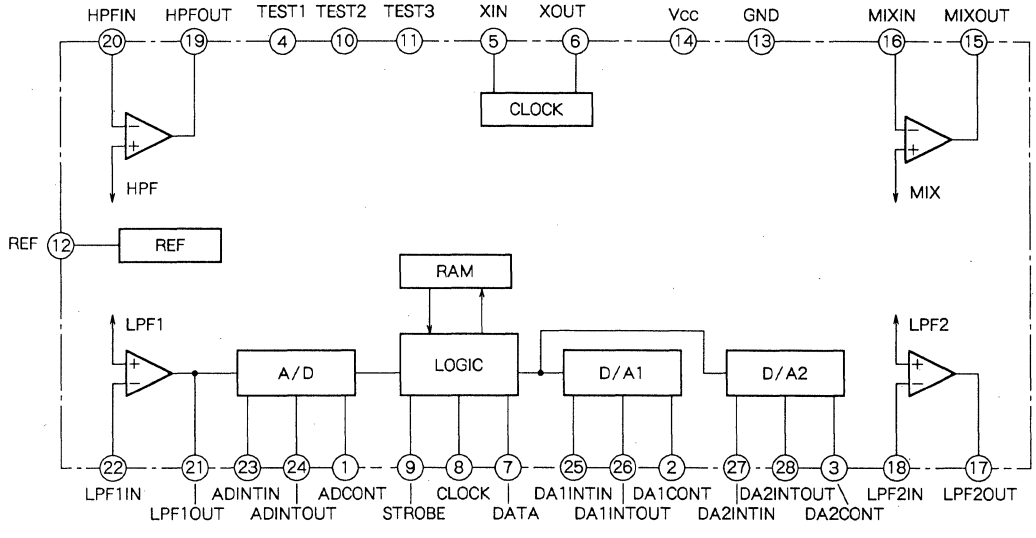
SINGLE CHIP DIGITAL KEY CONTROL

PIN CONFIGURATION



Outline 28P4B(SP)
28P2W-A(FP)

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin No.	Symbol	Name	Function
①	ADCONT	A/D control	Determines adaptive time constant for A/D conversion by ASM system
②	DA1CONT	D/A1 control	Determines adaptive time constant for D/A1 conversion by ASM system
③	DA2CONT	D/A2 control	Determines adaptive time constant for D/A2 conversion by ASM system
④	TEST1	Test	L : Normal mode H : Test mode
⑤	X_{IN}	Oscillator input	Connected to 16MHz ceramic filter
⑥	X_{OUT}	Oscillator output	
⑦	DATA	Data	Data input via serial bus
⑧	CLOCK	Clock	Clock input via serial bus
⑨	STROBE	Strobe	Strobe input via serial bus
⑩	TEST2	Test	
⑪	TEST3	Test	
⑫	REF	Reference power supply output	Output 1/2V_{CC} Connected to filter C
⑬	GND	Ground	
⑭	V_{CC}	Power supply	
⑮	MIXOUT	Mix output	Combines key-controlled low-pass signal and through high-pass signal
⑯	MIXIN	Mix input	
⑰	LPF2OUT	Low-pass filter 2 output	Post-filters following D/A conversion for key control
⑱	LPF2IN	Low-pass filter 2 input	
⑲	HPFOUT	High-pass filter output	High-pass through filter
⑳	HPFIN	High-pass filter input	
㉑	LPF1OUT	Low-pass filter 1 output	Pre-filters precedent to A/D conversion for key control
㉒	LPF1IN	Low-pass filter 1 input	
㉓	ADINTIN	A/D integrator input	Forms A/D conversion integrator with external C
㉔	ADINTOUT	A/D integrator output	
㉕	DA1INTIN	D/A1 integrator input	Forms D/A1 conversion integrator with external C
㉖	DA1INTOUT	D/A1 integrator output	
㉗	DA2INTIN	D/A2 integrator input	Forms D/A2 conversion integrator with external C
㉘	DA2INTOUT	D/A2 integrator output	

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6.0	V
I_{CC}	Circuit current	100	mA
V_i	Input voltage	−0.3~V_{CC} + 0.3	V
P_d	Power dissipation	800(SP) /600(FP)	mW
T_{opr}	Operating temperature	−20~+75	℃
T_{stg}	Storage temperature	−40~+125	℃

RECOMMENDED OPERATIONAL CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IL}	Input voltage ("L" level)	Serial pass input	−	−	1	V
V_{IH}	Input voltage ("H" level)	Serial pass input	4	−	−	V
f_{ck}	Clock frequency		15.5	16	16.5	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, f = 1kHz, V_i = − 15dBm, fck = 16MHz (when key is F0), Ta = 25℃ unless otherwise noted)

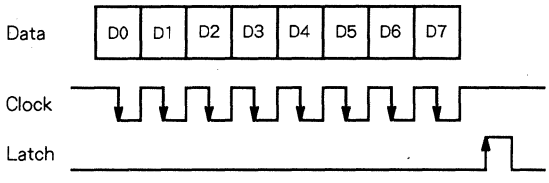
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	No signals	−	19	50	mA
Gv	Voltage gain		−3	0	3	dB
THD	Output distortion	Vo = − 15dBm, 30kHz LPF	−	0.8	2	%
No	Output noise voltage	JIS-A	−	−84	−70	dBm
V_{Omax}	Maximum output voltage	THD = 10%	−1	2	−	dBm

0dBm = 775mVrms

FUNCTION

Key Control System :

3-line clocked serial pass control



Key control variations

D0	D1	D2	D3	D4	VMC	VSC
H	H	H	H	H		F + 20
L	H	H	H	H		F + 18
H	L	H	H	H		F + 16
L	L	H	H	H		F + 14
H	H	L	H	H		F + 13
L	H	L	H	H		F + 11
H	L	L	H	H		F + 9
L	L	L	H	H	F + 8	F + 8
H	H	H	L	H	F + 7	F + 7
L	H	H	L	H	F + 6	F + 6
H	L	H	L	H	F + 5	F + 5
L	L	H	L	H	F + 4	F + 4
H	H	L	L	H	F + 3	F + 3
L	H	L	L	H	F + 2	F + 2
H	L	L	L	H	F + 1	F + 1
L	L	L	L	H	F 0	F 0
H	H	H	H	L	F − 1	F − 1
L	H	H	H	L	F − 2	F − 2
H	L	H	H	L	F − 3	F − 3
L	L	H	H	L	F − 4	F − 4
H	H	L	H	L	F − 5	F − 5
L	H	L	H	L	F − 6	F − 6
H	L	L	H	L	F − 7	F − 7
L	L	L	H	L	F − 8	F − 8
H	H	H	L	L		F − 9
L	H	H	L	L		F − 11
H	L	H	L	L		F − 12
L	L	H	L	L		F − 13
H	H	L	L	L		F − 14
L	H	L	L	L		F − 16
H	L	L	L	L		F − 18
L	L	L	L	L		F − 20

D5	VSC/VMC
H	VSC
L	VMC

D6	MUTE
H	MUTE
L	NORMAL

D7	TEST
H	TEST
L	NORMAL

Note 1. VMC ensures better sound quality in key variation between −4 and +4, while VSC is suitable for key variation beyond this range.

2. Sampling frequency for A-D, D-A conversion is different between VMC and VSC. Noise may be produced when VMC is switched to VSC or the other way around. We recommend that mute be provided as shown above (D6) to prevent it.

3. When power is turned on, key is set to F0 and mode is set to VMC by automatic reset function.

APPLICATION DIRECTIONS

① Input level

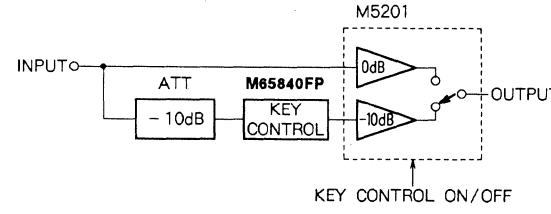
The maximum output voltage at low-pass filters, high-pass filters and mixing amplifier is 1.2Vrmsmin(+4dBm), and that at digital key control circuit is 0.7Vrmsmin(−1dBm).

Therefore, the adequate reference signal level is approximately 150mVrms(−14dBm).

When the reference signal is on this level, voltage at the head rooms is 18dB and 13dB, respectively.

The voltage at low-pass filters, high-pass filters and mixing amplifier can be attenuated or amplified within a limit of ± 10dB according to external constants. This mechanism can be used to obtain an adequate reference signal level.

When connected to operational amplifier M5201 having a switch as shown below, this IC is able to handle inputs at large amplitude(2Vrms), such as those from compact discs and laser discs, as well as ensures better sound quality when the key control is off.



② Power

Connect a filter capacitor of at least 47μF and a pass control of approximately 0.1μF near power-GND pin (within a radius of 2cm)

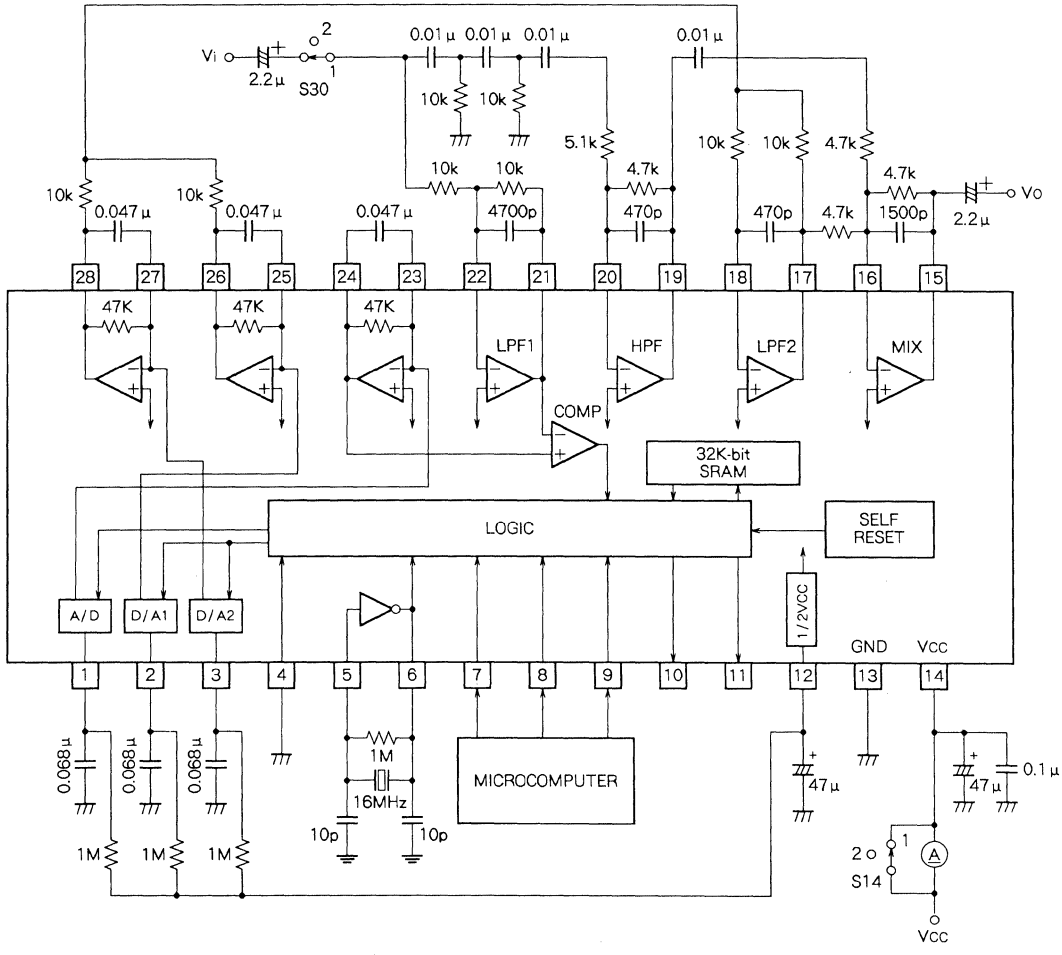
TEST CONDITIONS

SWITCHING CONDITIONS

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	SWITCH		
			14	30	
Icc	Circuit current	No signal	2	2	
Gv	Voltage gain between input and output		1	1	Gv = 20log(Vo/Vi)
THD	Output distortion	30KHz L.P.F	1	1	
No	Output noise voltage	JIS-A	2	2	
Vomax	Maximum output voltage	30KHz L. P. F THD=10%	1	1	

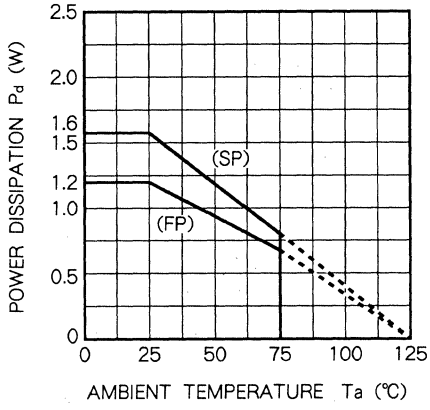
TEST CIRCUIT



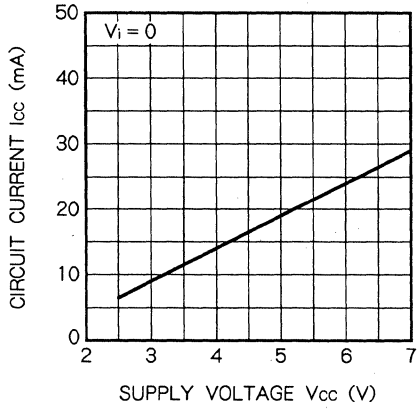
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

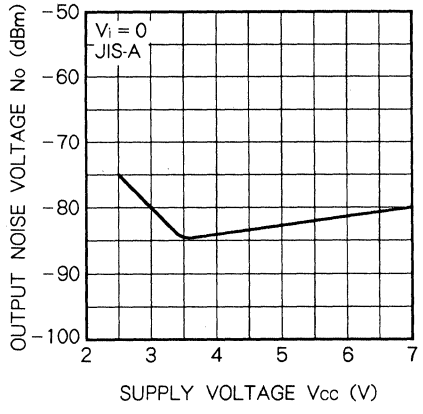
THERMAL DERATING
(MAXIMUM RATING)



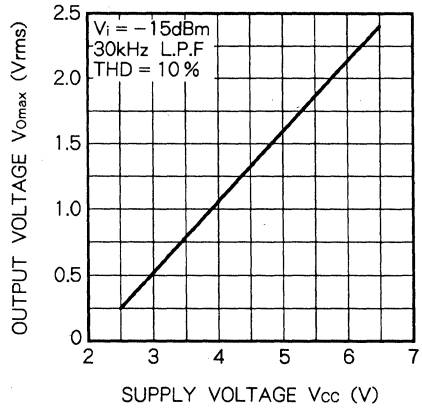
CIRCUIT CURRENT
VS. SUPPLY VOLTAGE



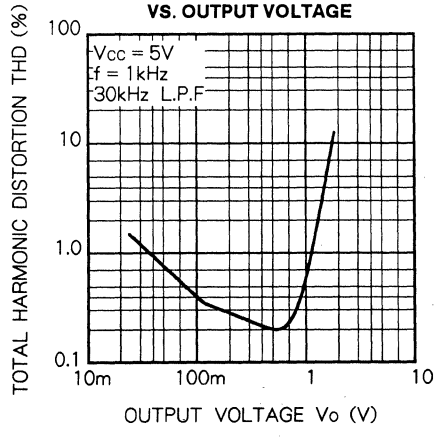
OUTPUT NOISE VOLTAGE
VS. SUPPLY VOLTAGE



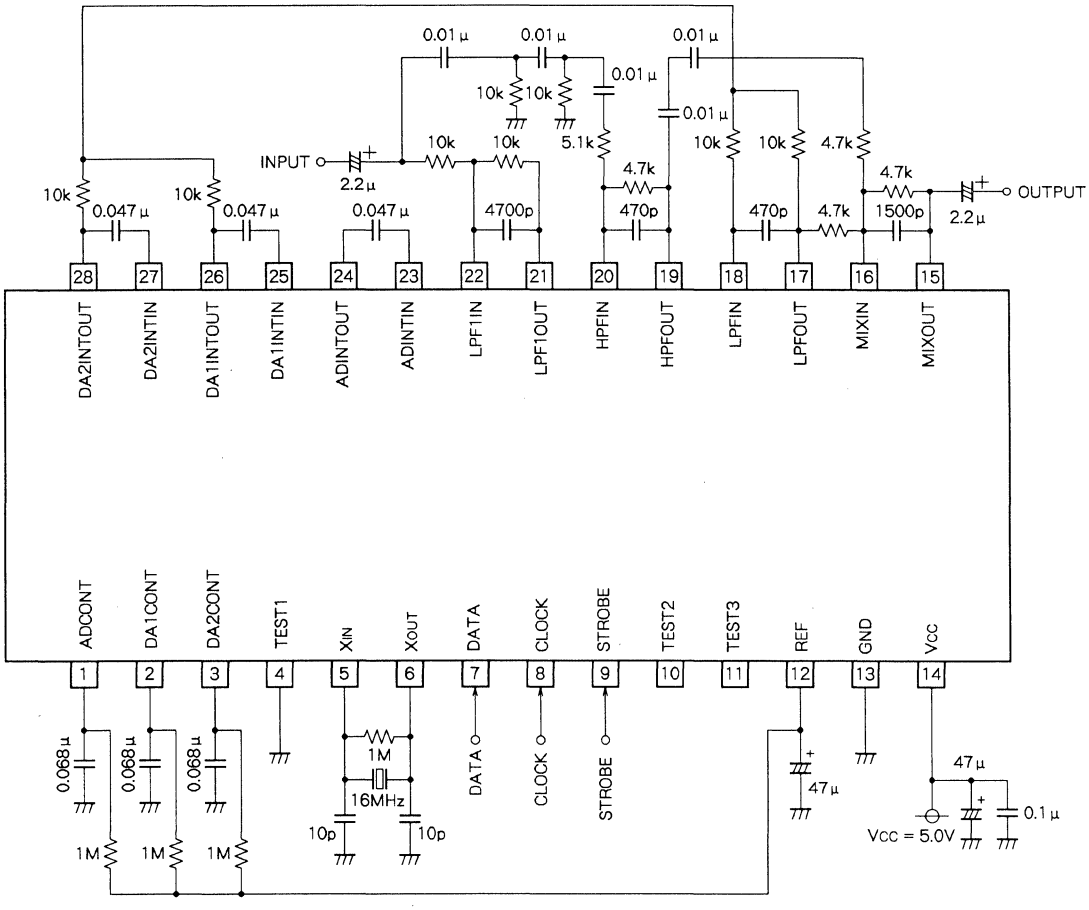
MAXIMUM OUTPUT VOLTAGE
VS. SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION
VS. OUTPUT VOLTAGE



APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

M65843P,FP

DIGITAL ECHO (DIGITAL DELAY)

DESCRIPTION

The M65843 is a CMOS IC for generating echo to be added to the voice through a "karaoke" microphone.

It is suitable for application to the echo generator of a radio cassette player, mini component stereo set, TV etc.

Increased master clock frequency assures high-performance short delay, enabling the IC to be used for digital surround.

FEATURES

- Fixed delay time of 125msec (with external clock set at 320kHz)
- Built-in A-D, D-A converters, input/output low-pass filter, and 10K bit delay memory
- High sound quality is assured by simple system construction, due to A-D, D-A converters with ADM (Adaptive Delta Modulation) system
  - Output noise voltage : – 80dBV (typ)
  - Total harmonic distortion : 1.7% (typ)
- Built-in mute circuit

Outline 24P4(P)

2.54mm pitch 600mil DIP
(13.0mm × 31.1mm × 3.8mm)

Outline 24P2W-A(FP)

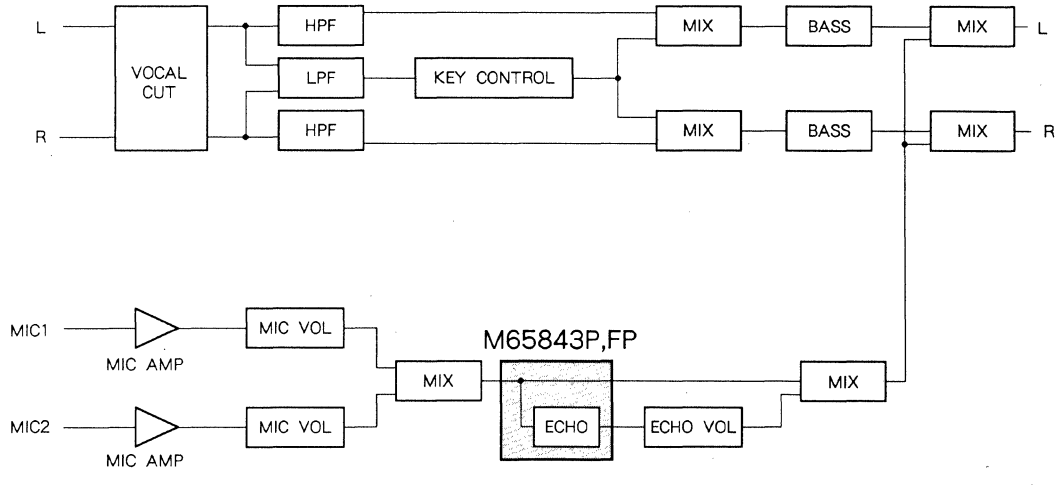
1.27mm pitch 450mil SOP
(8.4mm × 15.0mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC}, V_{DD} = 4.5~5.5V

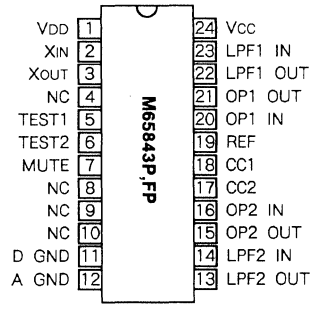
Rated supply voltage ····· V_{CC}, V_{DD} = 5V

SYSTEM CONFIGURATION



MITSUBISHI ELECTRIC

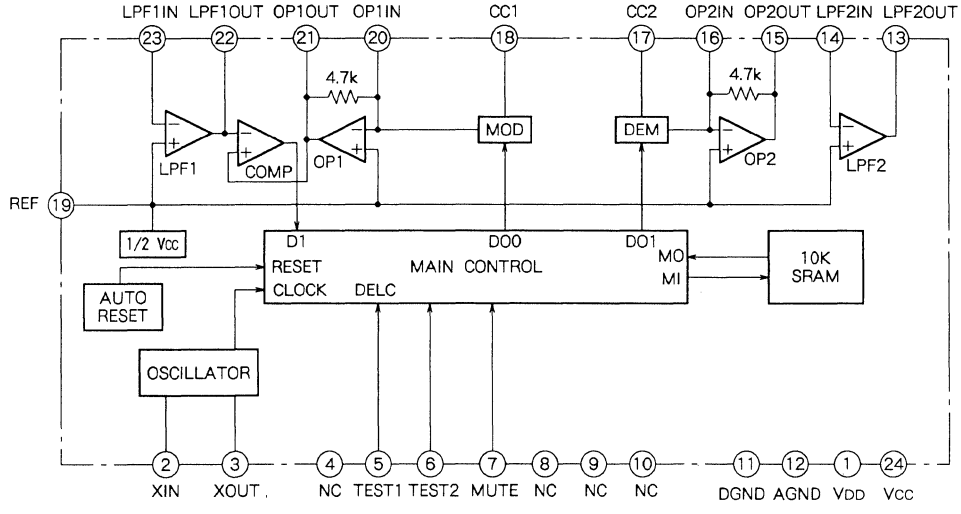
PIN CONFIGURATION



Outline 24P4(P)
24P2W-A(FP)

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Name	I/O	Function
①	V_{DD}	Digital power supply	–	
②	X_{IN}	Clock generator input	I	To connect 320kHz ceramic oscillator
③	X_{OUT}	Clock generator output	O	Open when external clock is used
④	NC	No connection	–	Connection of external device is inhibited
⑤	TEST1	Test1	I	Fixed at "H"
⑥	TEST2	Test2	I	Fixed at "L"
⑦	MUTE	Mute	I	Mute control, L = Mute mode
⑧	NC	No connection	–	Connection of external device is inhibited
⑨	NC	No connection	–	Connection of external device is inhibited
⑩	NC	No connection	–	Connection of external device is inhibited
⑪	D GND	Digital GND	–	
⑫	A GND	Analog GND	–	
⑬	LPF2 OUT	Low-pass filter 2 output	O	To form output-side low-pass filter by connecting external capacitor and resistor
⑭	LPF2 IN	Low-pass filter 2 input	I	
⑮	OP2 OUT	Operational amplifier 2 output	O	To form demodulating integrator by connecting external capacitor
⑯	OP2 IN	Operational amplifier 2 input	I	
⑰	CC2	Current control 2	–	ADM control of demodulator
⑱	CC1	Current control 1	–	ADM control of modulator
⑲	REF	Reference	–	Analog reference voltage = 1/2Vcc
⑳	OP1 IN	Operational amplifier 1 input	I	To form modulating integrator by connecting external capacitor and resistor
㉑	OP1 OUT	Operational amplifier 1 output	O	
㉒	LPF1 OUT	Low-pass filter 1 output	O	To form input-side low-pass filter by connecting external capacitor and resistor
㉓	LPF1 IN	Low-pass filter 1 input	I	
㉔	Vcc	Analog power supply	–	

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃ unless otherwise noted)

Symbol	Parameter		Ratings	Unit
Vcc	Supply voltage		6.5	V
Icc	Circuit current		100	mA
P_d	Power dissipation	M65843P	1	W
		M65843FP	0.8	
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−40∼+125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Vcc	Analog supply voltage		4.5	5	5.5	V
V_{DD}	Digital supply voltage		4.5	5	5.5	V
Vcc-V_{DD}	Vcc − V_{DD} potential difference		−0.3	0	0.3	V
f_{ck}	Clock frequency		280	320	475	kHz
V_{IH}	Input voltage ("H" level)		0.7V_{DD}	–	V_{DD}	V
V_{IL}	Input voltage ("L" level)		0	–	0.3V_{DD}	V

ELECTRICAL CHARACTERISTICS (Vcc = 5V, f = 1kHz, V_i = 100mVrms, Ta = 25℃ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Icc	Circuit current	No signal input	–	13	35	mA
Gv	I/O voltage gain	R_L = 47kΩ	−2.5	0.5	3.5	dB
V_{Omax}	Max. output voltage	THD = 10%	0.7	1	–	Vrms
THD	Distortion factor	30kHz LPF	–	1.7	3.0	%
No	Output noise voltage	DIN−AUDIO	–	−80	−65	dBV
SVRR	Supply voltage reduction ratio	△Vcc = −20dBV, f = 100Hz	–	−40	−25	dB

FUNCTION

(1) Sampling frequency fs

The sampling frequency can be calculated by the following equation :

fs = Clock frequency/4(Hz)

For clock frequency (fck) = 320kHz, the calculated sampling frequency is :

fs = 320kHz/4 = 80kHz

(2) Delay time Td

For fck = 320kHz(fs = 80kHz), the calculated delay time is :

T_d = 125msec

(3) Mute

Output can be muted by setting the MUTE terminal(⑦Pin) appropriately

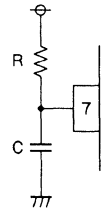
⑦MUTE	Mode
H	Normal mode
L	Mute mode

It is recommended to mute the output, as illustrated on the right, to prevent noise from being generated when power is turned ON. The muting period is determined by the resistor and capacitor connected to : pin, and calculated by the following equation :

Muting period(t mute) ≒ 0.96 × CR(sec)

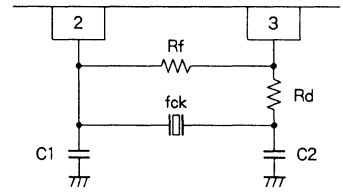
For C = 10 μF, R = 150k Ω, the calculated muting period is about 1.4sec :

t mute ≒ 0.96 × 10 μ × 150k = 1.38(sec)



(4) Clock generator

The M65843P, FP contains an oscillation buffer, so that a clock generator circuit can be formed by connecting a ceramic oscillator, resistors and capacitors as shown below.



For a ceramic oscillator with fck = 320kHz (CSB320D, manufactured by Murata Mfg. Co.), recommended resistance and capacitance values are :

Rf = 1M Ω

Rd = 6.8k Ω

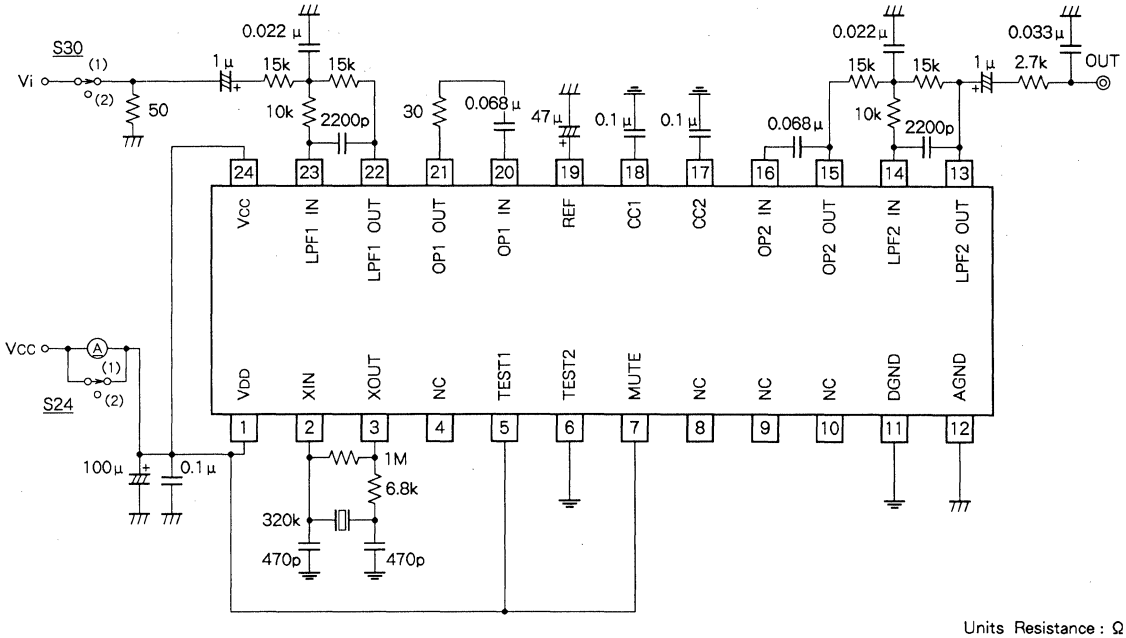
$C_1 = C_2$ = 470pF

Note that the above values vary according to the oscillator used, the oscillation frequency, and the constitutional environment of clock generator circuit (such as the capacity of substrate and wiring).

TEST CONDITIONS

Symbol	Parameter	S24	S30	Remark
Icc	Circuit current	2	2	No signal input
Gv	Voltage gain	1	1	Gv = 20log(Vo/Vi)
Td	Delay time	1	1	
Vomax	Max. output voltage	1	1	30kHzLPF, THD = 10 %
THD	Total harmonic distortion factor	1	1	30kHzLPF
No	Output noise voltage	1	2	DIN AUDIO, Vi = 0mVrms
SVRR	Supply voltage reduction ratio	1	2	ΔVcc = – 20dBV, f = 100Hz

TEST CIRCUIT

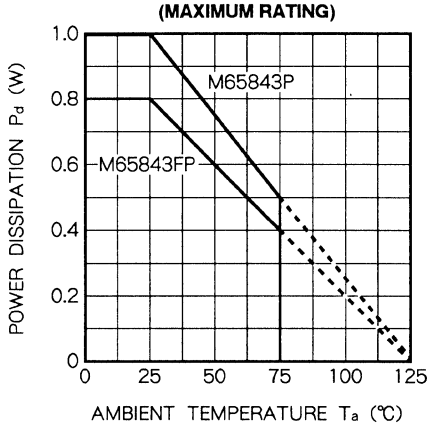


Units Resistance : Ω
Capacitance : F
: Analog GND
: Digital GND

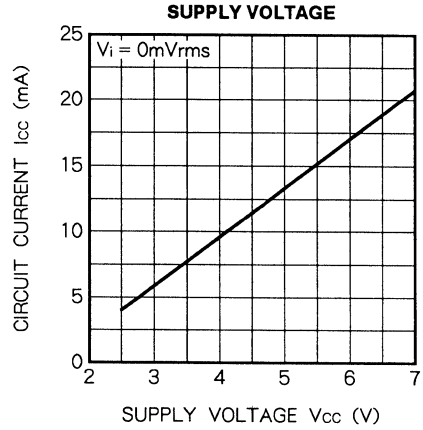
MITSUBISHI ELECTRIC

TYPICAL CHARACTERISTICS

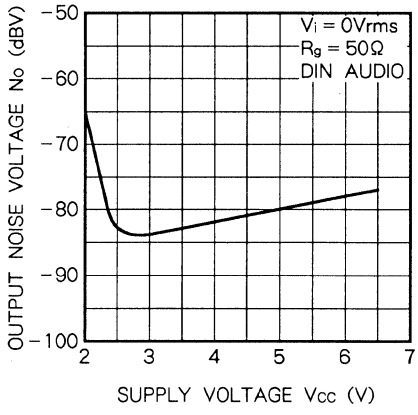
THERMAL DERATING (MAXIMUM RATING)



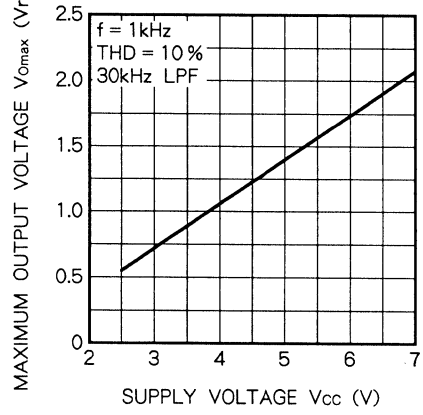
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



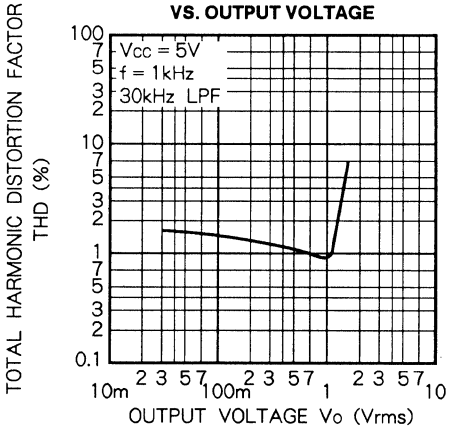
OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



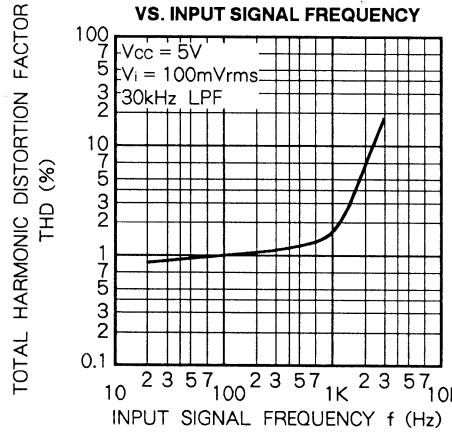
MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



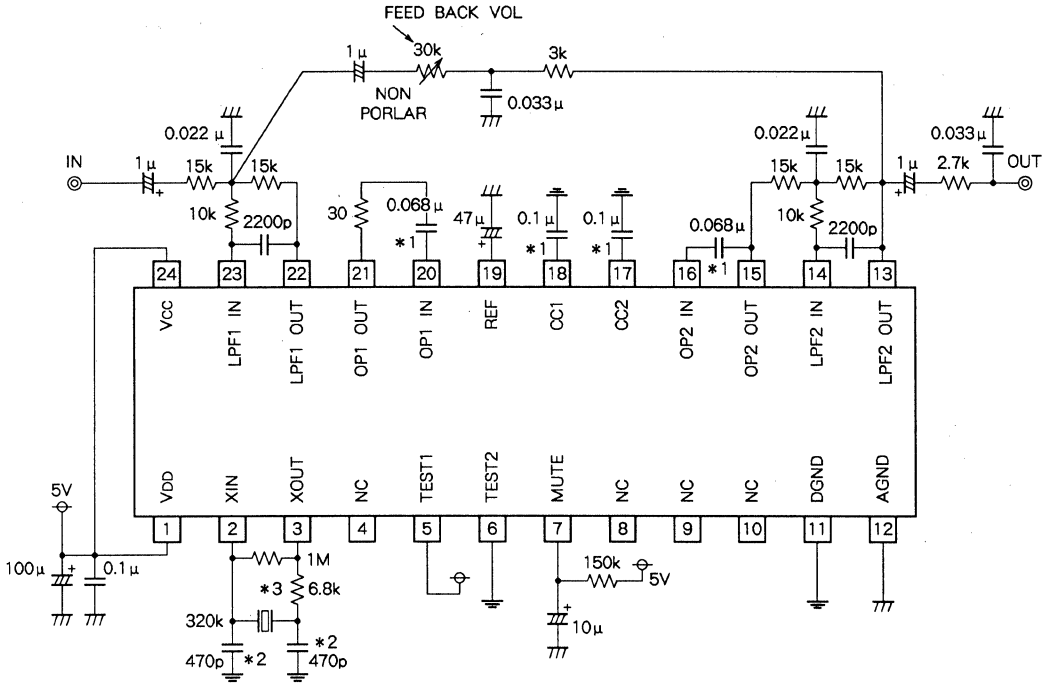
TOTAL HARMONIC DISTORTION FACTOR VS. OUTPUT VOLTAGE



TOTAL HARMONIC DISTORTION FACTOR VS. INPUT SIGNAL FREQUENCY



APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F
⏚ : Analog GND
⏚ : Digital GND

The capacitance marked * 1 shall have a relative accuracy within ± 5 %.

Note that the capacitance marked * 2 and resistance marked * 3 vary according to the oscillation frequency of ceramic oscillator, and the constitutional environment of the clock generator.

M65844P

DIGITAL ECHO (DIGITAL DELAY)

DESCRIPTION

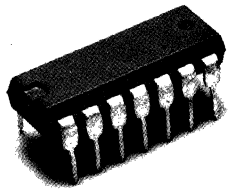
The M65844P is a CMOS IC for generating echo to be added to the voice through a "karaoke" microphone.

It is designed for the lowest price of models in the same series, and is suitable for application to the echo generator of a radio cassette player, mini-component stereo set, TV etc.

Increased master clock frequency assures high-performance short delay, enabling the IC to be used for digital surround.

FEATURES

- All functions necessary for generating digital echo are contained, enabling production of low-priced echo generator.
- C-R oscillation circuit is provided for a master clock.
- Built-in auto power-ON reset circuit.
- No control signal is required.
- Delay time = 150 msec (with master clock set at 220 kHz)
- Small 14-pin DIP package (14P4)



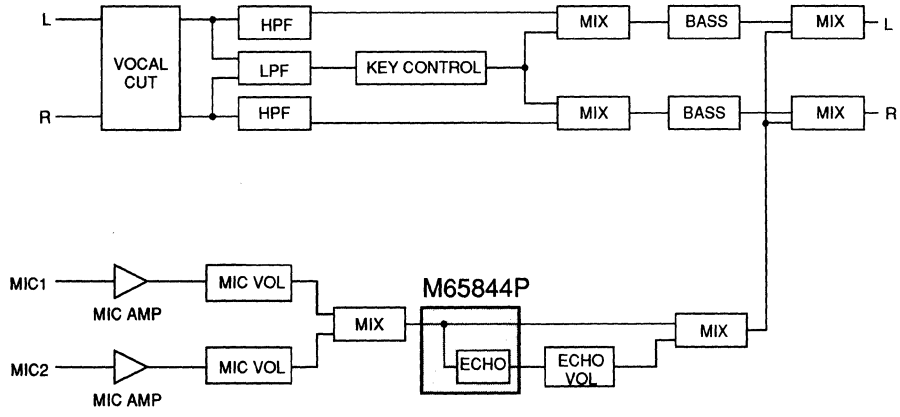
Outline 14P4

2.54mm pitch 300mil DIP
(6.3mm × 19.0mm × 3.3mm)

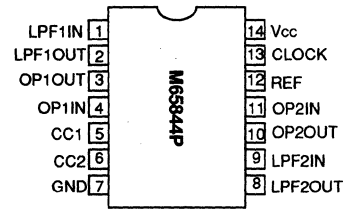
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... 4.5 ~ 5.5 V
Rated supply voltage ..... 5 V

SYSTEM CONFIGURATION

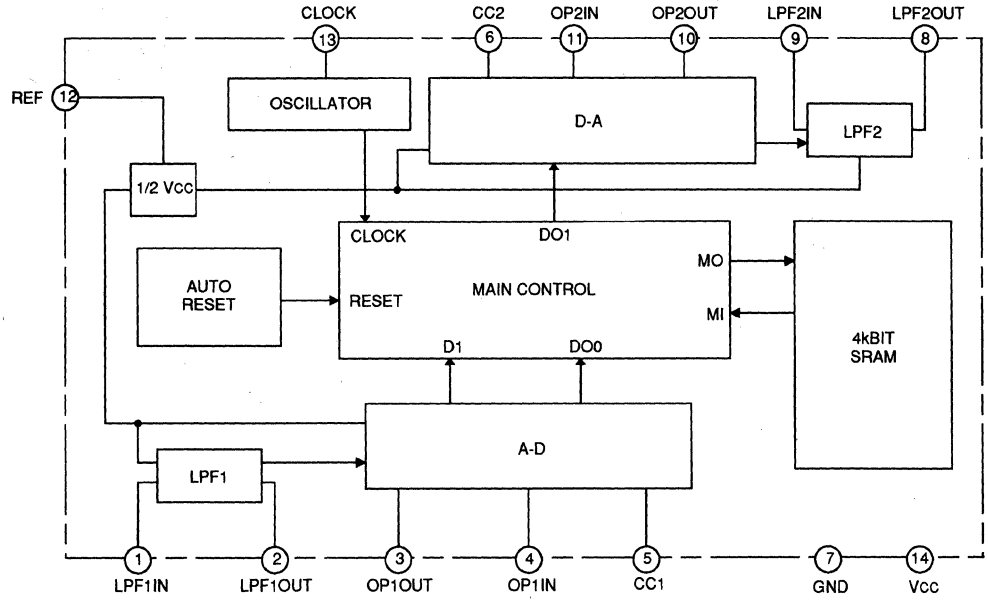


PIN CONFIGURATION



Outline 14P4

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin No.	Symbol	Name	I/O	Function
①	LPF1 IN	Low pass filter 1 input	I	To form input-side low pass filter by connecting external capacitor and resistor
②	LPF1 OUT	Low pass filter 1 output	O	
③	OP1 OUT	Operational amplifier 1 output	O	To form A-D conversion integrator by connecting external capacitor
④	OP1 IN	Operational amplifier 1 input	I	
⑤	CC1	Current control 1	–	ADM control of A-D converter
⑥	CC2	Current control 2	–	ADM control of D-A converter
⑦	GND	GND	–	
⑧	LPF2 OUT	Low pass filter 2 output	O	To form output-side low pass filter by connecting external capacitor and resistor
⑨	LPF2 IN	Low pass filter 2 input	I	
⑩	OP2 OUT	Operational amplifier 2 output	O	To form D-A conversion integrator by connecting external capacitor
⑪	OP2 IN	Operational amplifier 2 input	I	
⑫	REF	Reference	–	Analog reference voltage ≒ 1/2 Vcc
⑬	CLOCK	Clock generator input	I	To form clock generator by connecting external capacitor and resistor (220 kHz typ.)
⑭	Vcc	Supply votlage	–	To apply 4.5 ~ 5.5 V power (Rated voltage: 5V)

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6.5	V
I_{CC}	Circuit current	100	mA
P_d	Power dissipation	1.2	W
T_{opr}	Operating temperature	–20~75	°C
T_{stg}	Storage temperature	–40~125	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
f_{CK}	Clock frequency		100	220	2500	kHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, f = 500 Hz, Vi = 100 mVrms, fck = 220 kHz, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	No signal input	–	30	60	mA
Gv	Voltage gain	RL=47kΩ	–3.5	–0.5	2.5	dB
V_{omax}	Maximum output voltage	THD=10%	0.7	1.0	–	Vrms
THD	Total harmonic distortion	30kHz LPF	–	5.0	8.0	%
No	Output noise voltage	DIN–AUDIO	–	–75	–55	dBV

FUNCTION DESCRIPTION

(1) Sampling frequency fs

The sampling frequency can be calculated by the following equation:

fs = Clock frequency/8 (Hz)

For clock frequency (fck) = 220 kHz, the calculated sampling frequency is:

fs = 220 kHz/8 = 27.5 kHz

(2) Delay time Td

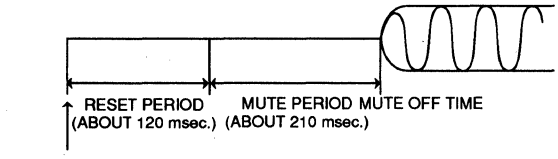
The delay time can be calculated by the equation:

Td = N/fs (N = the number of memory bits = 4,096)

When fck = 220 kHz (fs = 27.5 kHz), Td can be set at 150 msec.

(3) Mute

When power is turned on, the mute function works automatically to prevent noise generation. (Here, however, "mute" means the function which prevents noise generation after the reset time.)



(a) WHEN POWER IS ON

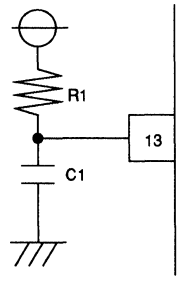
(4) Clock generator circuit

The M65844P includes an oscillation buffer, so that a clock generator circuit can be formed by connecting a resistor and a capacitator, as shown below.

The clock frequency can be calculated using the following equation.

Clock frequency (fck) ≒ K/R1 Hz

K is the coefficient, and changes according to the value for capacitator C1, as shown below.



fck (Hz)	C1 (F)	fck value
100k~400k	100p	fck=0.91X10¹⁰/R1
400k~1M	56p	fck=1.4X10¹⁰/R1
1M~2.5M	33p	fck=2.2X10¹⁰/R1

Also, the typical delay times and constants for the clock generator circuits are as shown below.

Delay time	fck (Hz)	R1 (Ω)	C1 (F)
100msec	320k	27k	100p
150msec	220k	39k	100p

(5) Signal bands

The signal frequency band can be changed by changing the constants for each of the input/output low pass filters (LPF1, LPF2).

Signal frequency band decision circuit

Signal band	External R (R2, 3, 4, 8, 9, 10)
1kHz	33kΩ
2kHz	16kΩ

Examples of application circuit changes

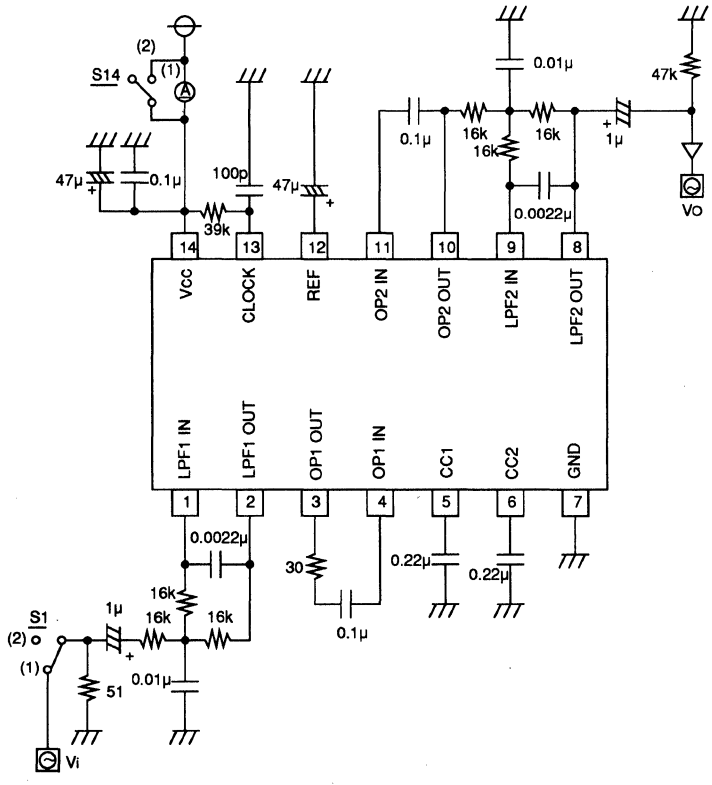
(Changes of output noise voltage and distortion when delay time and signal band have been changed)

Signal band / Delay time	1kHz		2kHz	
	Output noise voltage	Distortion	Output noise voltage	Distortion
100msec	–90dBV	2.2%	–85dBV	3.3%
150msec	–80dBV	4.0%	–79.5dBV	5.3%

Test conditions

No.	Parameter	Symbol	S1	S14	Remarks
1	Circuit current	Icc	2	2	No-signal time
2	Voltage gain between input and output	Gv	1	1	Gv=20 log (Vo/Vi)
3	Maximum output voltage	V_{omax}	1	1	THD=10%
4	Output distortion	THD	1	1	30kHz L.P.F
5	Output noise voltage	No	2	1	DIN AUDIO

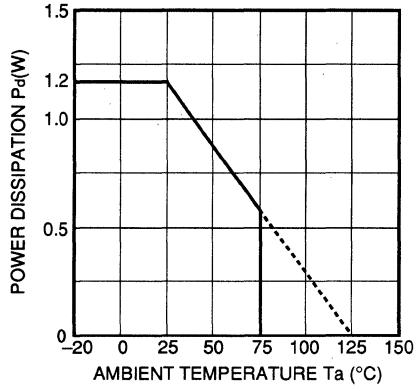
TEST CIRCUIT



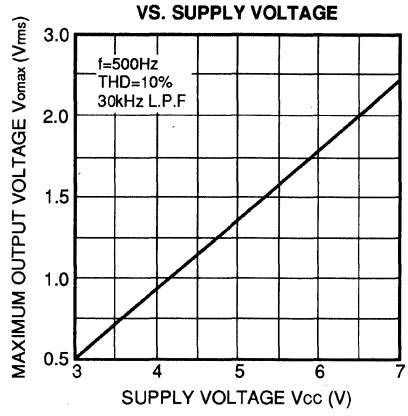
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

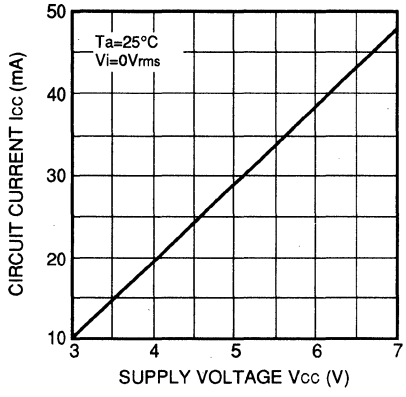
THERMAL DERATING
(MAXIMUM RATING)



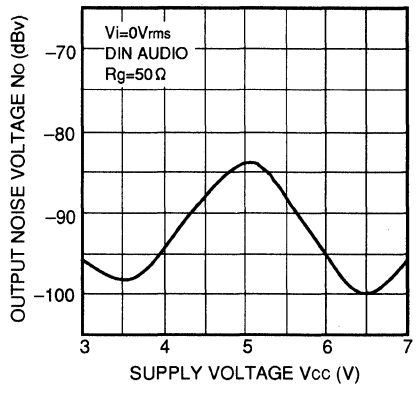
MAXIMUM OUTPUT VOLTAGE
VS. SUPPLY VOLTAGE



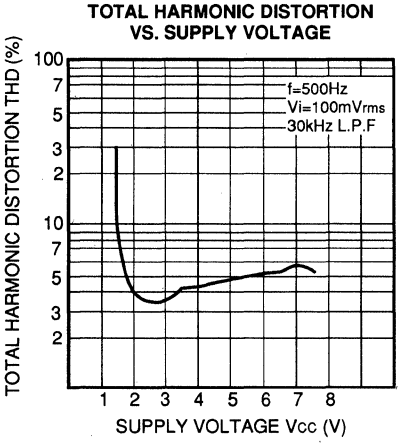
CIRCUIT CURRENT
VS. SUPPLY VOLTAGE



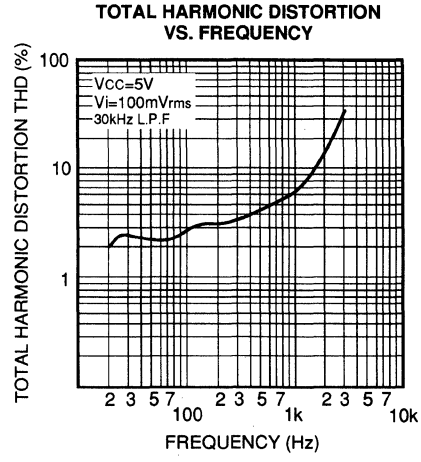
OUTPUT NOISE VOLTAGE
VS. SUPPLY VOLTAGE



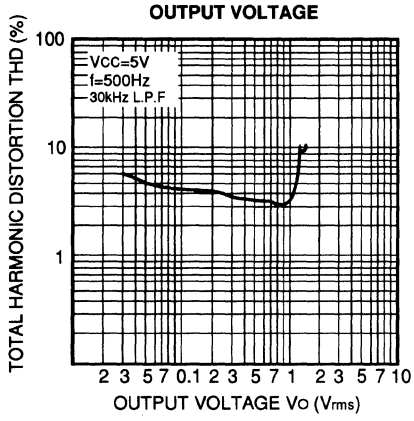
TOTAL HARMONIC DISTORTION
VS. SUPPLY VOLTAGE



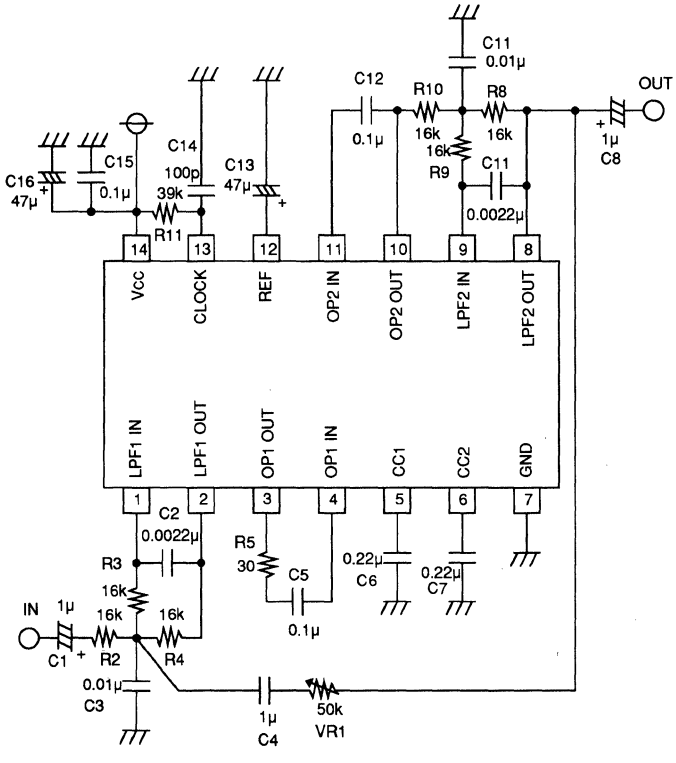
TOTAL HARMONIC DISTORTION
VS. FREQUENCY



TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

M65845FP

SINGLE CHIP MICROPHONE AND ECHO

DESCRIPTION

The M65845FP is an LSI built-in a microphone peripheral circuit and echo generation circuit for "karaoke" equipment.

It is suitable for application to the microphone mixing and echo generating functions of not only "karaoke" equipment but also a radio cassette player, TV, VCR, mini-component stereo set etc.

FEATURES

- Two microphone-mixing lines, vocal cut circuit, digital echo, and line-mixing amplifier are contained, enabling single-chip package of microphone peripheral circuit of "karaoke" equipment.
- Low noise due to digital echo with 4k bit RAM
- ALC-equipped microphone amplifiers permit excessively high input. ALC operating voltage can be set as desired.
- Vocal cut circuit of complete stereo construction
- Single 5V power supply
- Built-in auto power-ON reset circuit

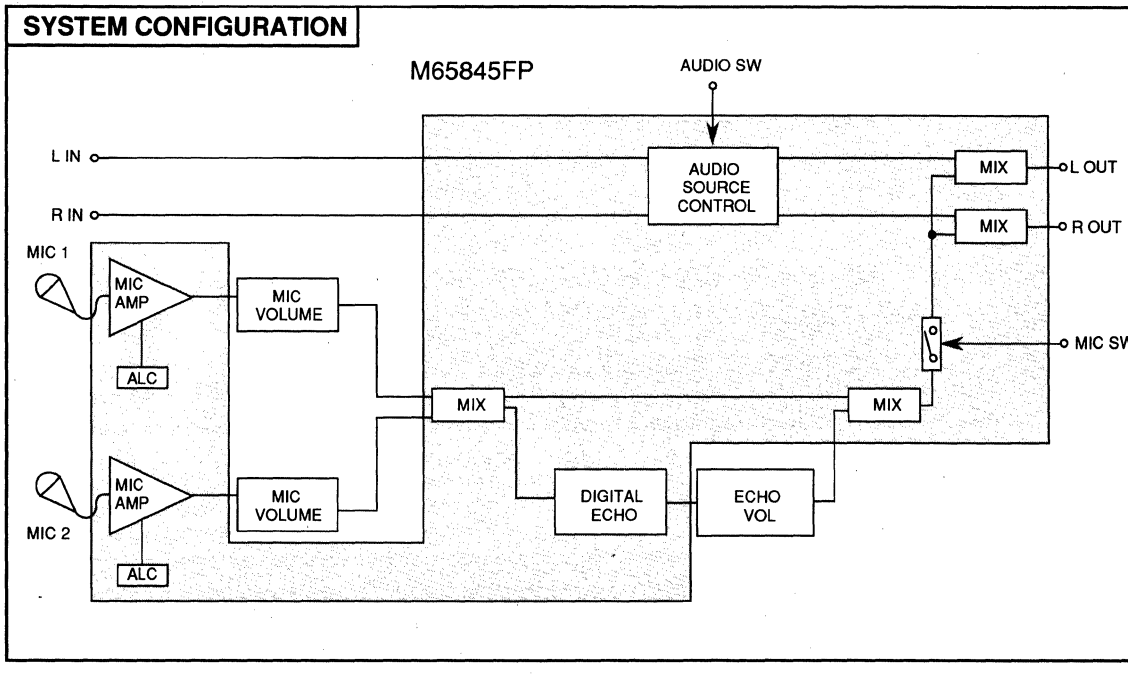
Outline 36P2R-A

0.8mm pitch 450mil SSOP
(8.4mm × 15.0mm × 2.0mm)

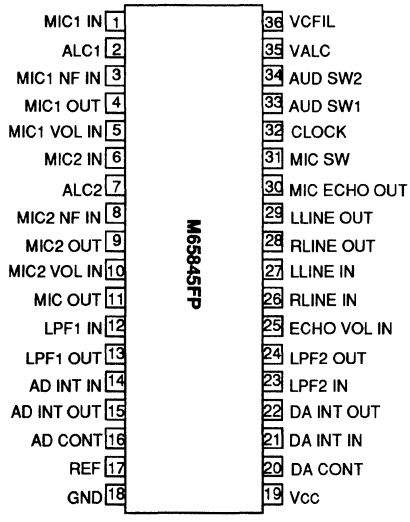
RECOMMENDED OPERATING CONDITIONS

Supply voltage range	Vcc =4.5 ~ 5.5V
Rated supply voltage	Vcc =5V
Clock frequency	100~ 2500kHz
Rated clock frequency	220kHz
L input voltage	1V
H input voltage	4V

SYSTEM CONFIGURATION

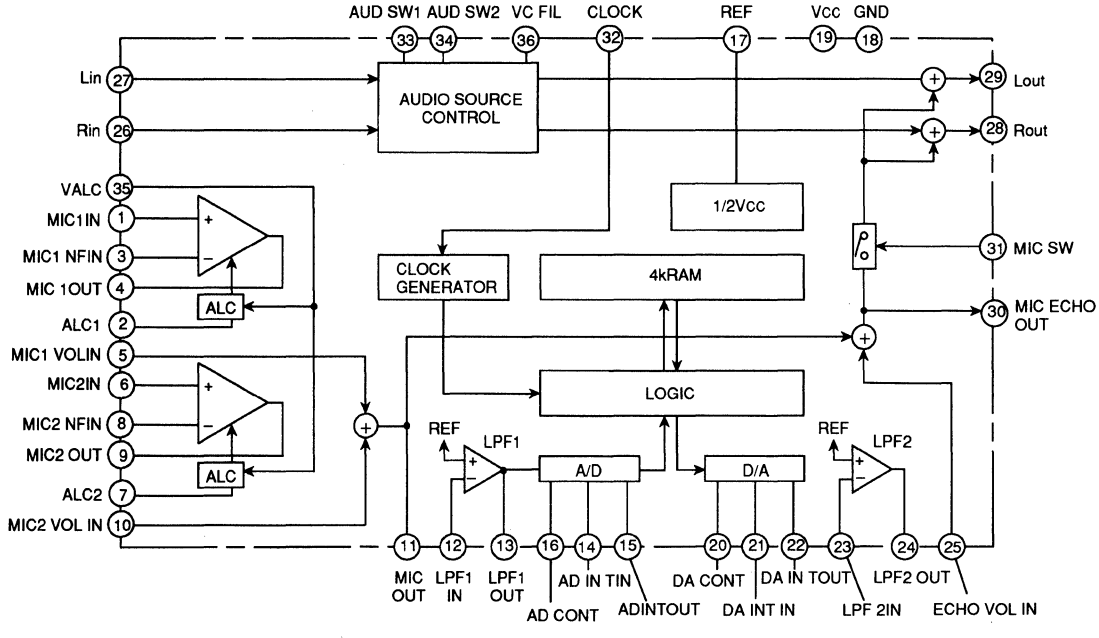


PIN CONFIGURATION



Outline 36P2R-A

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Name	Function
①	MIC1 IN	Microphone 1 input	To connect MIC1
②	ALC1	ALC1 control	To connect ALC attack/recovery time setting capacitor
③	MIC1 NF IN	Microphone 1 negative feedback input	To set amplifier gain of MIC1 by feedback circuit
④	MIC 1OUT	Microphone 1 output	
⑤	MIC1 VOL IN	Microphone 1 volume input	To input signal attenuated by external microphone volume
⑥	MIC2 IN	Microphone 2 input	To connect MIC2
⑦	ALC2	ALC 2 control	To connect ALC attack/recovery time setting capacitor
⑧	MIC2 NF IN	Microphone 2 negative feedback input	To set amplifier gain of MIC2 by feedback circuit
⑨	MIC2 OUT	Microphone 2 output	
⑩	MIC2 VOL IN	Microphone 2 volume input	To input signal attenuated by external microphone volume
⑪	MIC OUT	Microphone output	Mixing output of MIC1 and MIC2
⑫	LPF1 IN	Low-pass filter 1 input	To form pre-filter before A/D conversion for digital echo
⑬	LPF1 OUT	Low-pass filter 1 output	
⑭	AD INT IN	A/D integrator input	To form A/D conversion integrator by connecting external capacitor
⑮	AD INT OUT	A/D integrator output	
⑯	AD CONT	A/D control	To determine adaptive time constant of A/D converter with ADM system
⑰	REF	Reference power output	To connect 1/2 Vcc output and filter capacitor
⑱	GND	Grounding	
⑲	Vcc	Power supply	
⑳	DA CONT	D/A control	To determine adaptive time constant of D/A converter with ADM system
㉑	DA INT IN	D/A integrator input	To form D/A conversion integrator by connecting external capacitor
㉒	DA INT OUT	D/A integrator output	
㉓	LPF2 IN	Low-pass filter 2 input	To form post-filter after D/A conversion for digital echo
㉔	LPF2 OUT	Low-pass filter 2 output	
㉕	ECHO VOL IN	Echo volume input	To input signal attenuated by external echo volme
㉖	RLONE IN	R-channel line input	
㉗	LLINE IN	L-channel line input	
㉘	RLINE OUT	R-channel line output	Mixing output for microphone system and line
㉙	LLINE OUT	L-channel line output	
㉚	MIC ECHO OUT	Microphone echo output	Mixing output of original voice through microphone and echo signal
㉛	MIC SW	Microphone SW	L: MIC OFF H: MIC ON
㉜	CLOCK	Clock	C-R clock generator with built-in oscillation buffer
㉝	AUD SW1	Audio SW 1	Audio selector SW: audio signal is selected by setting these switches to L or H
㉞	AUD SW2	Audio SW 2	
㉟	VALC	ALC operating voltage setting terminal	To set ALC operating voltage according to applied voltage
㊱	VCFIL	Vocal cut filter	To pass components with lower frequency than vocal frequency band

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6.5	V
I_{CC}	Circuit current	100	mA
V_I	Input voltage	−0.3～V_{CC}+0.3	V
P_d	Power dissipation	1250	mW
T_{opr}	Operating temperature	−20～+75	°C
T_{stg}	Storage temperature	−40～+125	°C

RECOMMENDED OPERATING CONDITIONS

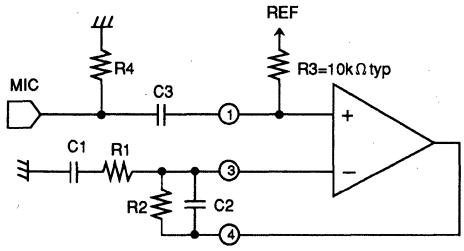
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IL}	Input voltage ("L" level)	Pin ㉝, ㉞	0	–	1	V
V_{IH}	Input voltage ("H" level)		4	–	V_{CC}	V
fck	Clock frequency	Clock frequency determines the delay time for echo. Refer to "FUNCTIONAL DESCRIPTION" paragraph.	320	500	2000	kHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, f = 500 Hz, V_I = 100mVrms, fck = 220 kHz, Ta = 25°C, unless otherwise noted)

Blok	Symbol	Parameter	Test conditions	Limits			Unit
				Min	Typ	Max	
Entire system	I_{CC}	Circuit current	No signal input	–	30	60	mA
Microphone amplifier	Gvo	Amplifier open loop gain	V_O=−17dBV	−55	60	–	dB
	THD1	Total harmonic distortion	V_O=−17dBV, with ALC not operated	–	0.2	0.5	%
	THD2	Total harmonic distortion	V_I=−27 dBV, with ALC operated	–	3.0	6.0	%
	VoALC	ALC operating voltage measurement error	Measurement : −10 to +3 dBV	−3	0	+3	dB
	TALCAT	ALC attack time	C=4.7μF	25	40	55	msec
	TALCRE	ALC recovery time	C=4.7μF	0.7	1	1.3	sec
	VoMAX	Maximum output voltage	THD=10%	−1	2	–	dBV
	No	Output noise voltage	Gv=37dB, f=100～5kHz	–	−72	−67	dBV
	Zi	Input impedance		5	10	20	kΩ
Microphone echo volume	Gv	I-O voltage gain	Maximum volume	−3	0	+3	dB
Digital echo	Td	Delay time	fs=27.5kHz	–	150	–	msec
	Gv	Voltage gain		−3	0	+3	dB
	THD	Total harmonic distortion		–	5	8	%
	VoMAX	Maximum output voltage	THD=10%	−3	0	–	dBV
	No	Output noise voltage	JIS–A	–	−75	−55	dBV
Line	Gv	Voltage gain		−3	0	+3	dB
	THD	Total harmonic distortion		–	0.05	0.1	%
	VoMAX	Maximum output voltage	THD=10%	1	4	–	dBV
	No	Output noise voltage	JIS–A, MICSW=off	–	−92	−88	dBV
	Zi	Input impedance		10	20	40	kΩ
Vocal cut	No	Output noise voltage	JIS–A, vocal cut ON	–	−88	−72	dBV
	Gv	Voltage gain	Single-channel input	−3	0	+3	dB
	VoMAX	Maximum output voltage	THD=10%	1	4	–	dBV
	GREJ	Vocal rejection ratio		20	24	–	dB

FUNCTION DESCRIPTION

(1) Microphone amplifier



The gain (Gv), low cut-off frequency (fcl), and high cut-off frequency (fch) of microphone amplifier are expressed as follows:

$$Gv = \frac{R1 + R2}{R1} \qquad fcl = \frac{1}{2\pi R1 \cdot C1} \qquad fch = \frac{1}{2\pi R2 \cdot C2}$$

The appropriate value of R2 is 50k ~ 500kΩ.

Assuming Gv = 37dB, fcl = 210Hz, fch = 5.5 kHz, for instance, the constants take the following values:

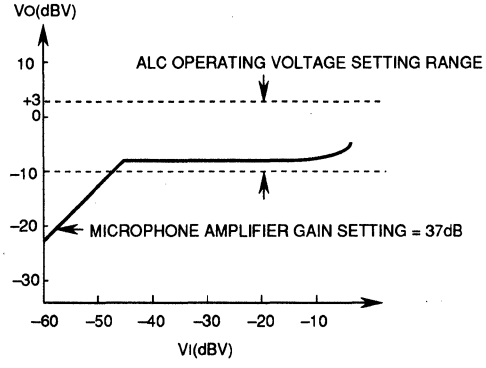
R1 = 2.2kΩ, R2 = 150kΩ, C1 = 0.33μF, C2 = 200 pF

The low cut-off frequency can also be determined by C3 and R3. However, R3 is an internal resistance of LSI and fluctuates largely. Therefore, the low frequency should be set at a value little lower than the low cut-off frequency (fcl), using the smallest R3 value (5 kΩ) in the fluctuating range. For the example given above,

C3 = 0.22μF

To minimize click noise generated when connecting or disconnecting a microphone, it is recommended to connect R4 (600Ω ~ 10 kΩ) in the circuit.:

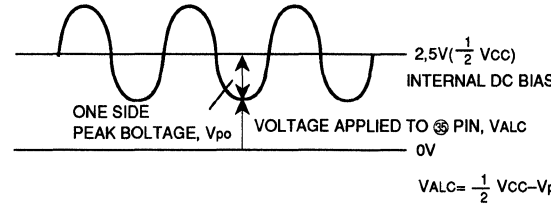
(2)ALC level diagram



(3)ALC operating voltage setting

ALC operating voltage can be set at a desired value between -10 and +3dBV by varying the DC voltage applied to pin ㉟ (ALC operating voltage setting terminal).

(Setting method)



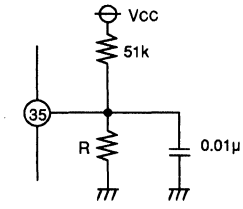
$V_{ALC} = \frac{1}{2} V_{CC} - V_{po}$

To set ALC operating voltage at −5dB (Vcc = 5V)

−5dBV=0.56Vrms=1.59Vp-p=0.8Vp-o

VALC=2.5−0.8=1.7V

Since the input impedance at pin ㉟ is high at 1 MΩ or more, it is possible to provide ALC operating voltage by dividing resistance.



When Vcc = 5 V

ALC operating voltage (dBV)	Voltage applied to pin ㉟ VALC (V)	Resistance R (Ω)
+3	0.50	5.6k
0	1.09	15k
−2	1.38	20k
−4	1.61	24k
−6	1.79	27k
−8	1.94	33k
−10	2.05	36k

(4)Microphone SW

Signals sent to microphone and echo systems can be shut off by setting the state of pin ㉛ (MIC SW) to L level.

(5)Audio source selection

Desired audio source operation mode suitable to each "karaoke" software can be selected by the audio SW.

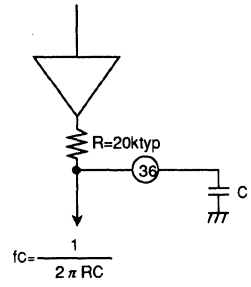
㉝ AUDSW1; D1	㉞ AUDSW2; D2	Operation mode
L	L	Stereophone
L	H	L-ch. monophonic
H	L	R-ch. monophonic
H	H	Vocal cut

① Stereophone
Audio signal is output directly through 2 channel lines.

② Lch. monophonic
Audio signal from L channel of the source is output through 2 channel lines. This mode allows reproduction of the sound of a multiplex "karaoke" softwere, or the main sound of a laser disc.

③ Rch. monophonic
Audio signal from R channel of the source is output through 2 channel lines. This mode allows reproduction of the reference vocal of a multiplex "karaoke" software, or the sub sound of a laser disc.

④ Vocal cut
The components of the same phase and same sound volume in the L and R channels are attenuated.
Since the vocal cut circuit has a complete stereo construction, it provides stereophonic effect even after vocal cut processing.
The low-pass cut-off frequency (fc) is determined by the capacitance connected to pin ㊱ (vocal cut filter) as shown in the illustration below.
This mode also allows components with lower frequency than the vocal band to pass through the filter, to compensate insufficient low-pitch sound.



For fc = 50 Hz, the capacitance (C) is 0.15μF
Note: The internal resistance of each LSI may differ in the range of about ±30%

(6)Digital echo

The delay time (Td) for echo is determined by the clock frequency (fck) at pin ㉜ (clock).

$$\text{Sampling frequency } fs = \frac{1}{8} \times fck$$

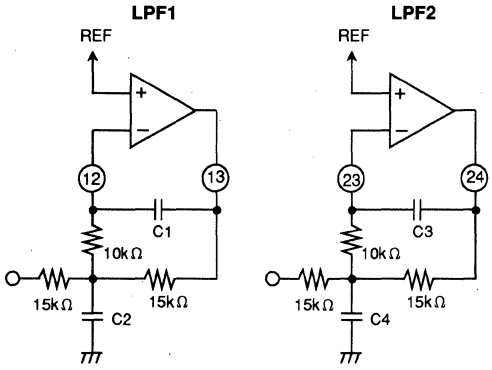
$$Td = \frac{N}{fs} = 8 \times \frac{N}{fck}$$

(N = the number of memory bits = 4096)
For fck = 220 kHz, the delay time (Td) is 150 msec.

It is necessary to change the LPF setting (signal pass band, fsig) of digital echo according to the clock frequency. (Refer to the table below.)

The S/N ratio increases when LPF setting is lower than the optimum signal pass band, and decreases when the setting is higher than the optimum signal pass band.

Clock frequency fck (kHz)	Sampling frequency fs (kHz)	Delay time Td (msec)	Optimum signal pass band fsig (kHz)	LPF constant	
				C1, C3	C2, C4
160~320	20~40	205~102	0.7	5600p	56000p
320~520	40~65	102~63	1	3900p	39000p
520~880	65~110	63~37	2	1800p	18000p
880~1240	110~155	37~26	3	1200p	12000p
1240~1600	155~200	26~20	7	560p	5600p



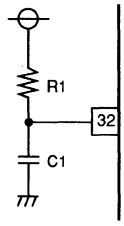
(7) Clock generator circuit

The M65845FP includes an oscillation buffer, so that a clock generator circuit can be formed by connecting a resistor and a capacitator, as shown in the diagram on the right.

The optimum resistance value, R1, can be calculated using the following equation.

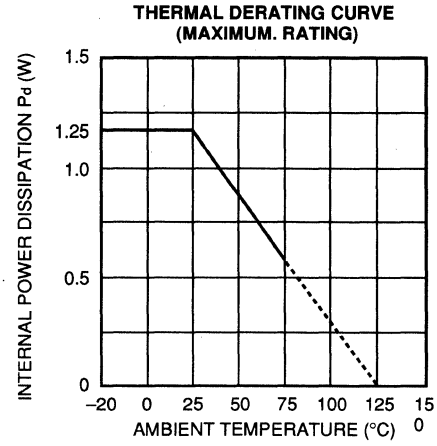
Optimum resistance value (R1)≒K/fck Hz

K is the coefficient, and changes according to the value for capacitor C1, as shown below.

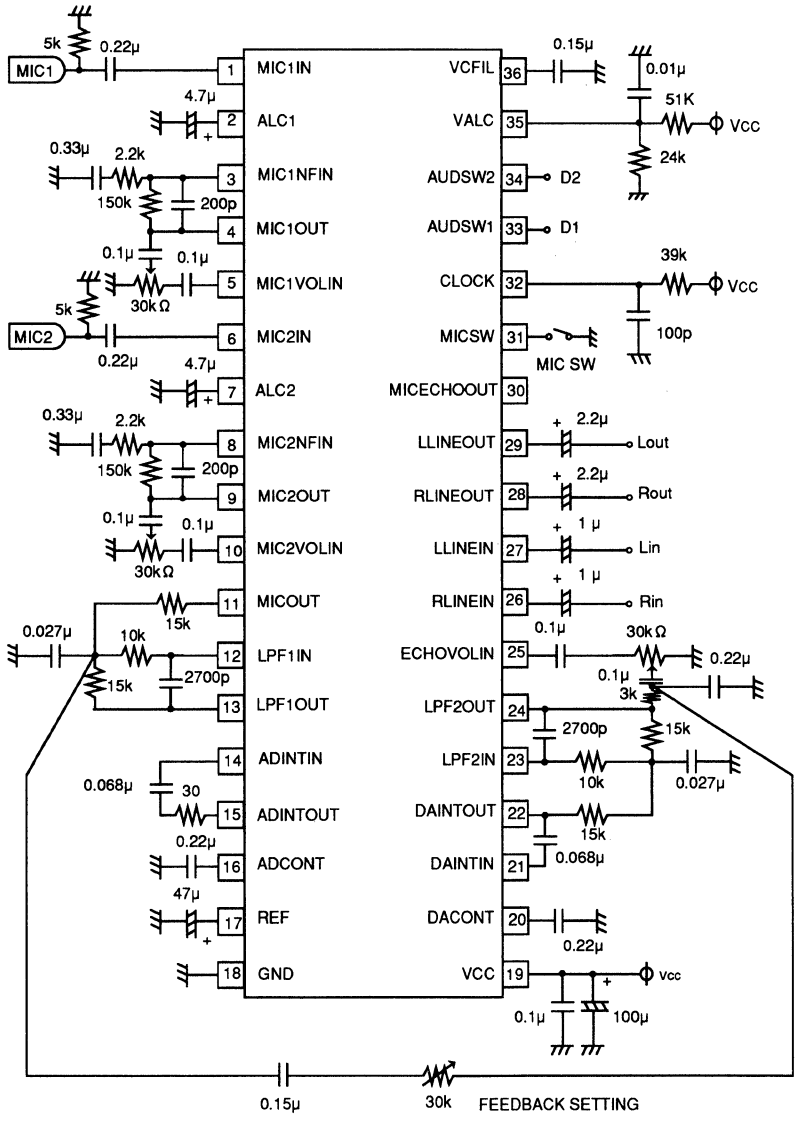


fck (Hz)	C1 (F)	R1 value
100k~400k	100p	R1=0.9×10¹⁰/fck
400k~1M	56p	R1=1.4×10¹⁰/fck
1M~2.5M	33p	R1=2.2×10¹⁰/fck

TYPICAL CHARACTERISTICS



APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

SURROUND PROCESSOR

3

M50198P,FP
DIGITAL DELAY

DESCRIPTION

The M50198 is a CMOS IC developed for producing surround effects in applications such as TV sets and video disc players.

The IC's design is based on the M50199P of the same series. The M50198 however, built-in memory and a comparator, which used to be placed externally. This makes it possible to configure a digital delay system with only a single chip.

The M50198 offers enhanced easiness in applications. It, for example, employs a microcomputer interface as a means of selecting delay time.

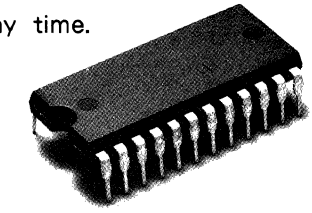
FEATURES

- Built-in memory and comparator realize a delay system with only a single chip
- Capable of producing low-noise and low-distortion delay effects by ADM system
- Offers 9 kinds of delay time up to 40ms
- Capable of setting delay time through microcomputer interface
- Built-in auto mute function prevents digital noise from occurring when changing delay time setting
- Built-in power-on-reset circuit further reduces the number of external components

RECOMMENDED OPERATING CONDITIONS

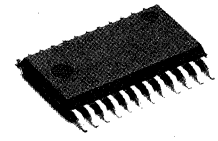
Supply voltage range ..... V_{CC}, V_{DD} = 4.5~5.5V

Rated supply voltage ..... V_{CC}, V_{DD} = 5V



Outline 24P4(P)

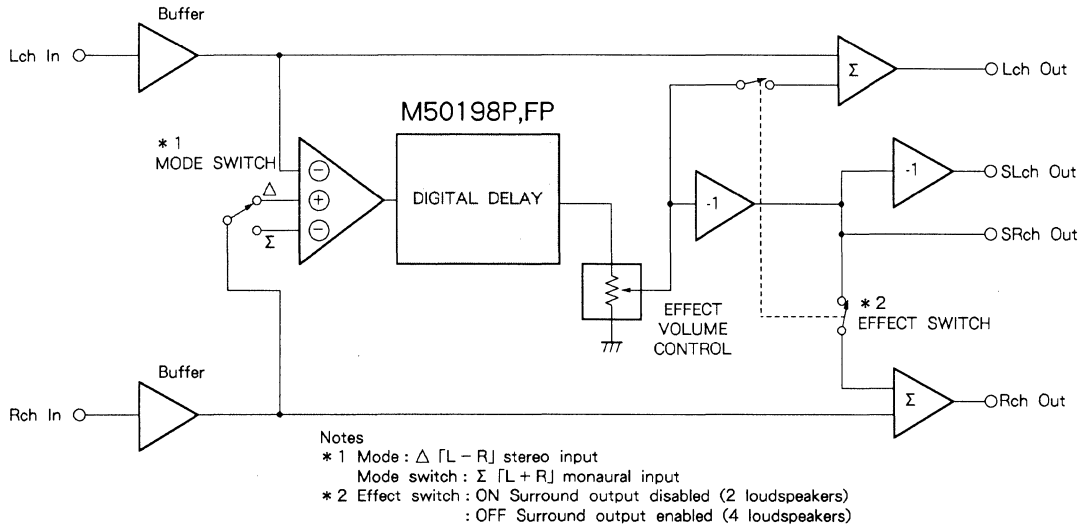
2.54mm pitch 600mil DIP
(13.0mm × 31.1mm × 3.8mm)



Outline 24P2W-A(FP)

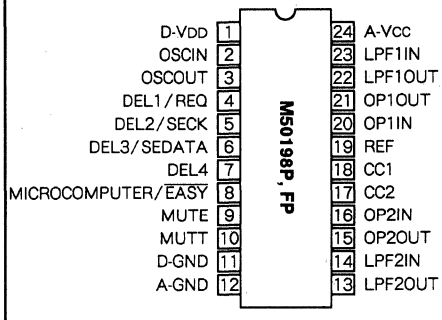
1.27mm pitch 450mil SOP
(8.4mm × 15.0mm × 2.0mm)

SYSTEM CONFIGURATION



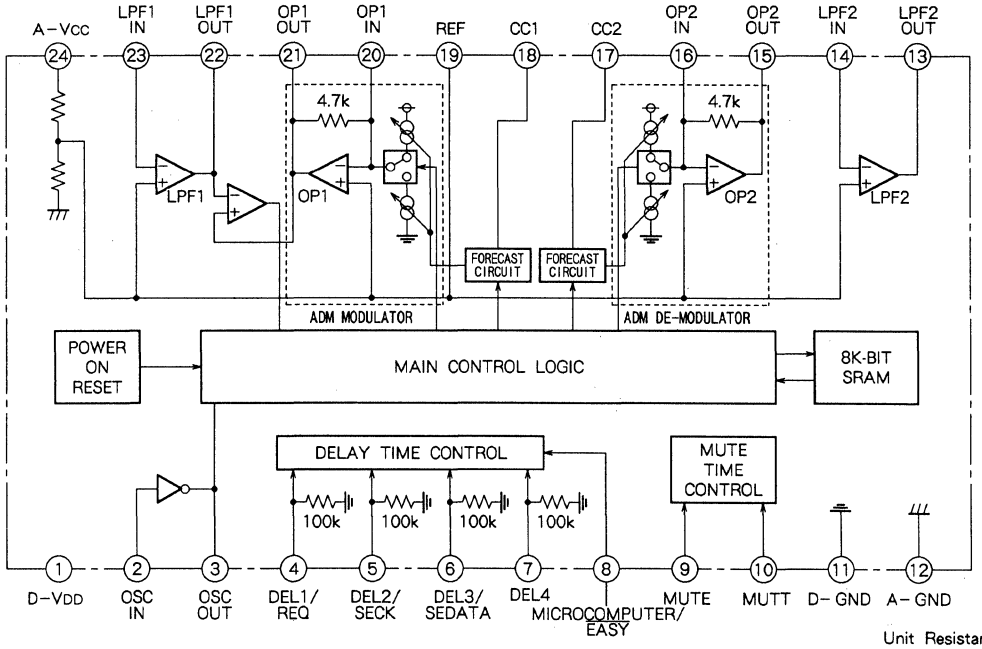
Notes
* 1 Mode : Δ ⌈L − R⌋ stereo input
Mode switch : Σ ⌈L + R⌋ monaural input
* 2 Effect switch : ON Surround output disabled (2 loudspeakers)
: OFF Surround output enabled (4 loudspeakers)

PIN CONFIGURATION



Outline 24P4(P)
24P2W-A(FP)

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

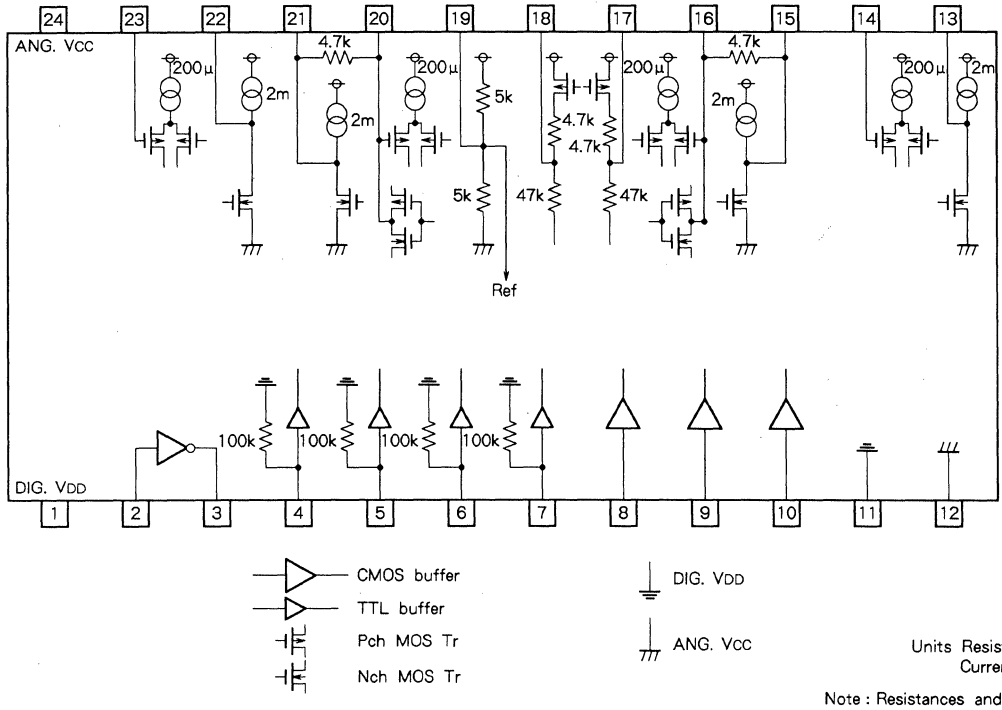
IN FUNCTIONS

Function	Symbol	Function outline
Reference voltage generator	REF	Generates reference voltage of analog circuit (1/2Vcc)
Low pass filter	LPF1, LPF2	Cuts unnecessary high frequency noise
Adaptive delta modulator	OP1, CC1	Converts analog signal to digital signal
Adaptive delta demodulator	OP2, CC2	Converts digital signal to analog signal
Forecast circuit		Makes the ADM operate the best suited then improves S/N ration and distortion
Clock generator circuit		Generates the master clock, Typical frequency is 3.27MHz
Delay time control circuit		Controls 9 delay time modes
Main control logic circuit		Controls ADM circuits and internal memory
Mute control circuit		Controls mute time
Power-on-reset circuit		Sends a reset signal at power on
8K-bit SRAM		Stores digital signal to create delay time

PIN DESCRIPTION

Pin No.	Name	Symbol	Function	Typical output DC voltage
①	Digital V_{DD}	D – V_{DD}	Supply voltage 4.5~5.5V (Typical 5V)	–
②	Oscillator input	OSC IN	Connects to 3.27MHz ceramic filter or inputs external clock	–
③	Oscillator output	OSC OUT	Connects to 3.27MHz ceramic filter	–
④	DEL1/REQ	DEL1/REQ	Uses DEL1 terminal in easy mode and REQ terminal in microcomputer mode	–
⑤	DEL2/SECK	DEL2/SECK	Uses DEL2 terminal in easy mode and SECK terminal in microcomputer mode	–
⑥	DEL3/SEDATA	DEL3/ SEDATA	Uses DEL3 terminal in easy mode and SEDATA terminal in microcomputer mode	–
⑦	DEL4	DEL4	Controls 80 µsec mode	–
⑧	Microcomputer/$\overline{EASY}$	Microcomputer/ $\overline{EASY}$	Controls microcomputer mode and manual mode	–
⑨	MUTE control	MUTE	Controls mute function	–
⑩	MUTE time control	MUTT	Controls mute time	–
⑪	Digital GND	D – GND	Connects to analog GND at one point	0
⑫	Analog GND	A – GND	Connects to analog GND	0
⑬	Low pass filter 2 output	LPF2 OUT	Forms low pass filter with external C, R	2.5V
⑭	Low pass filter 2 input	LPF2 IN		2.5V
⑮	OP-AMP 2 output	OP2 OUT	Forms integrator with external C	2.5V
⑯	OP-AMP 2 input	OP2 IN		2.5V
⑰	Current control 2	CC2		0.7V (V_{in} = 0)
⑱	Current control 1	CC1		
⑲	Reference	REF	= 1/2Vcc	2.5V
⑳	OP-AMP 1 input	OP1 IN	Forms integrator with external C	2.5V
㉑	OP-AMP 1 output	OP1 OUT		2.5V
㉒	Low pass filter 1 output	LPF1 OUT	Forms low pass filter with external C, R	2.5V
㉓	Low pass filter 1 input	LPF1 IN		2.5V
㉔	Analog Vcc	A – Vcc	Supply voltage 4.5~5.5V (Typical 5V)	–

I/O INTERFACE



ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		6.5	V
I_{CC}	Circuit current		70	mA
P_d	Power dissipation	M50198P	1000	mW
		M50198FP	650	mW
T_{opr}	Operating temperature	M50198P	−20∼+75	℃
		M50198FP	−20∼+65	℃
T_{stg}	Storage temperature		−40∼+125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
f_{ck}	Clock frequency		2	3.27	6	MHz
V_{IH}	High input voltage	CMOS input pin ＊1	0.7V_{DD}	−	V_{DD}	V
		TTL input pin ＊2	2.2	−	V_{DD}	V
V_{IL}	Low input voltage	CMOS input pin ＊1	−	−	0.3V_{DD}	V
		TTL input pin ＊2	−	−	0.8	V
f_{SECK}	Microcomputer mode serial clock		−	−	4	MHz

＊1 CMOS input pin : 2, 8, 9, 10
＊2 TTL input pin : 4, 5, 6, 7

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, f = 1kHz, V_i = 100mVrms, fcs = 3.27MHz, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CCO}	Circuit Current		–	45	65	mA
G_V	Voltage gain	R_L = 47k Ω	– 3.5	– 0.5	2.5	dB
V_{Omax}	Maximum output voltage	THD = 10 %	0.7	1.2	–	Vrms
THD	Output distortion	30kHz LPF, Fs = 409kHz	–	0.3	1	%
		30kHz LPF, Fs = 204kHz	–	0.8	2	%
No	Output noise voltage	DIN Audio, Rg = 50 Ω, 0Vrms	–	– 92	– 70	dBV
SVRR	Supply voltage rejection ratio	△Vcc = – 20dBV, f = 100Hz	–	– 40	– 25	dB
T_{MUTE}	Mute time	SHORT mute	70	75	80	ms
		LONG mute	310	315	320	

DELAY TIME

(1) EASY MODE (Microcomputer/$\overline{EASY}$ = L)

Pin name *2					Sampling frequency (kHz)	Delay time *1 (msec)
μ-COM/$\overline{EASY}$	DEL1	DEL2	DEL3	DEL4		
L	L	L	L	L	409	5.0
	H	H	L	L		10.0
	H	L	L	L		15.0
	L	H	L	L		20.0
	H	L	H	L	204	25.1
	L	L	H	L		30.1
	L	H	H	L		35.1
	H	H	H	L		40.1
	X	X	X	H	409	0.078

(X : Don't care)

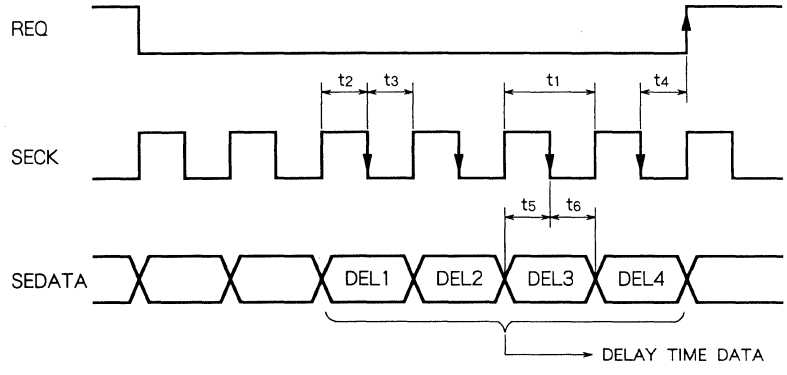
* 1 fck = 3.27MHz

* 2 DEL1, DEL2, DEL3 and DEL4 are input pins with pull-down.

(2) Microcomputer mode:Serial data input

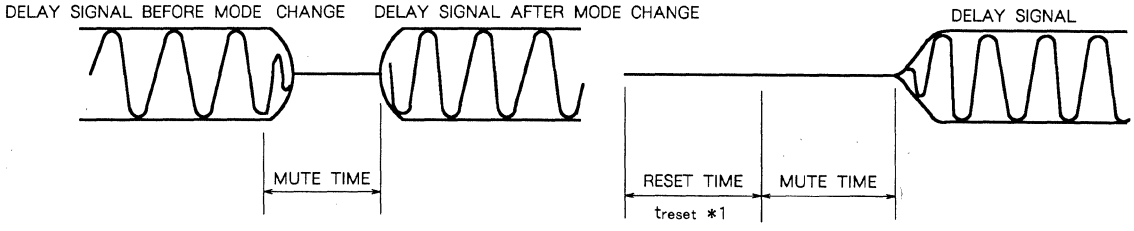
(Microcomputer/$\overline{EASY}$ = H)

The time chart shown is microcomputer mode. When REQ signal is low-level, SEDATA signal is latched at the falling edge of the SECK signal, and the last four delay time mode data are set at the rising edge of the REQ signal.



Symbol	Min	Typ	Max	Unit	Remark
t_1	250			nsec	$f_{SECK} < 4MHz$
t_2	100			nsec	
t_3	100			nsec	
t_4	100			nsec	
t_5	100			nsec	
t_6	100			nsec	

MUTING



(a) Waveforms of the signal re-initialiyed upon change of delay time mode

(b) Waveforms of the signal re-initialiyed at power on

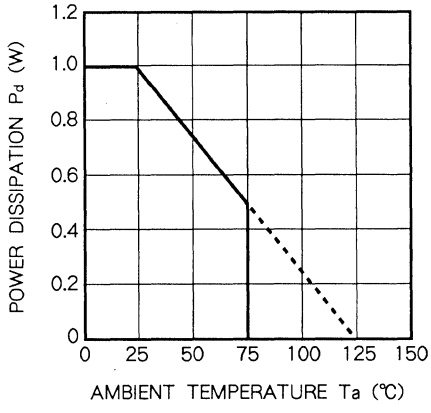
*1 : $t_{reset} = 2.5 \times C_{19}$ (μF) (C_{19} is an external condenser of 19th terminal)

Pin name		Mute mode	Mute time (msec)
MUTE	MUTT TIME		
L	L	SHORT mute	80
	H	LONG mute	320
H	X	Manual	–

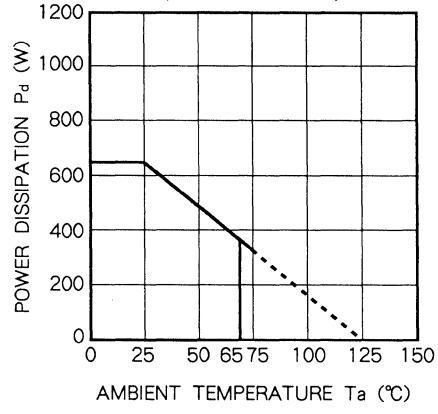
X : Don't care

TYPICAL CHARACTERISTICS

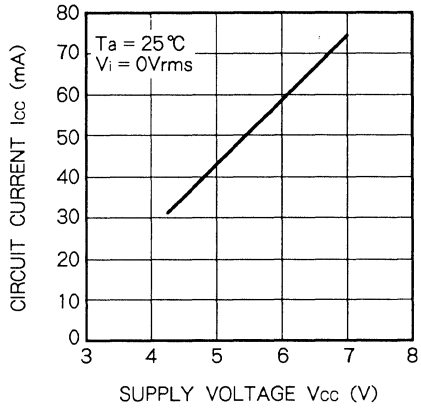
THERMAL DERATING (M50198P) (MAXIMUM RATING)



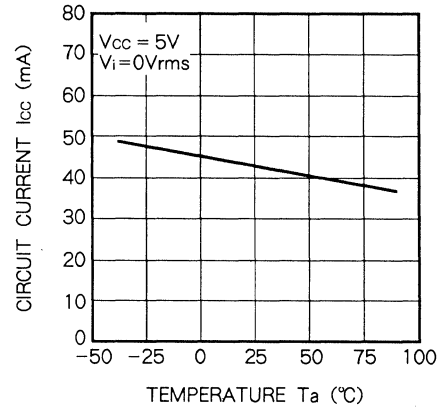
THERMAL DERATING (M50198FP) (MAXIMUM RATING)



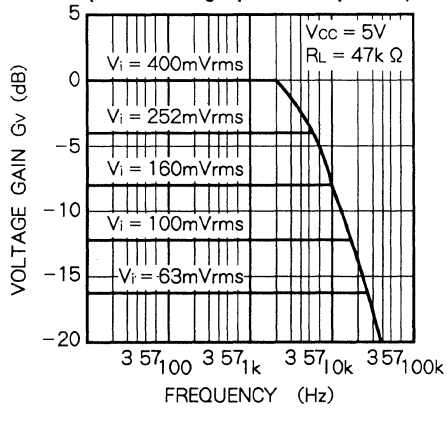
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



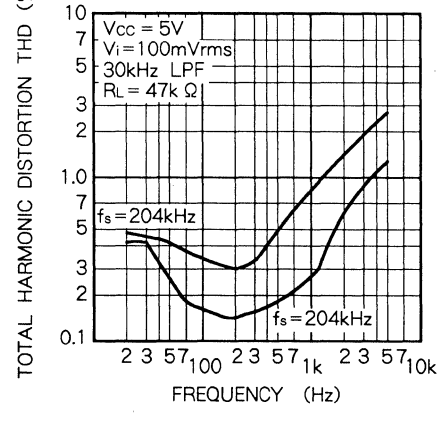
CIRCUIT CURRENT VS. TEMPERATURE



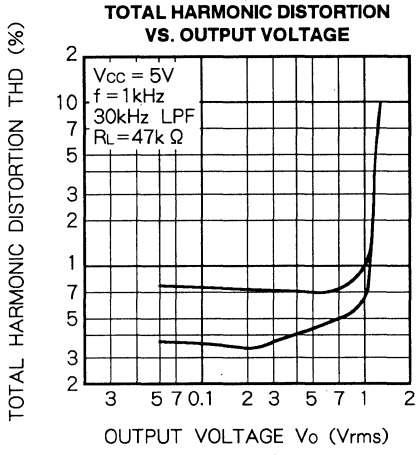
VOLTAGE GAIN VS. FREQUENCY (Not including input and output LPF)



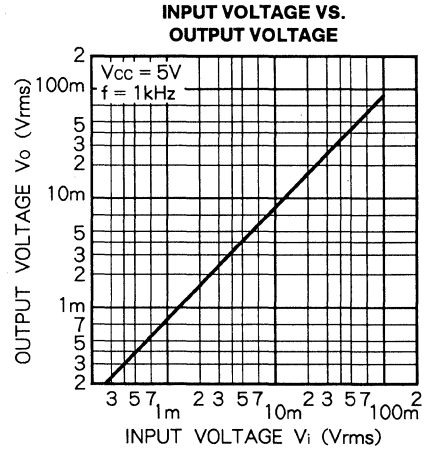
TOTAL HARMONIC DISTORTION VS. FREQUENCY



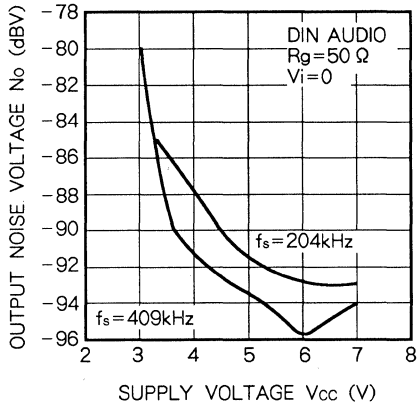
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



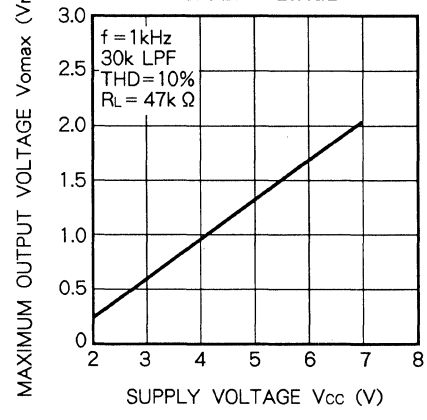
INPUT VOLTAGE VS. OUTPUT VOLTAGE



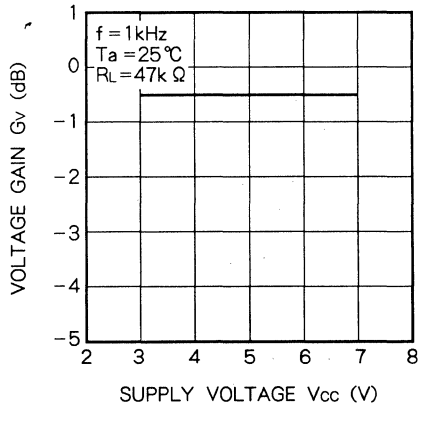
OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



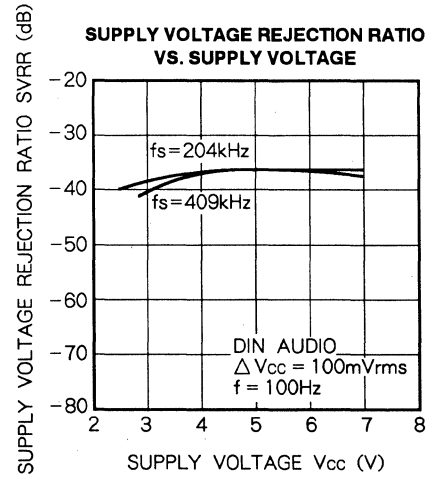
MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE

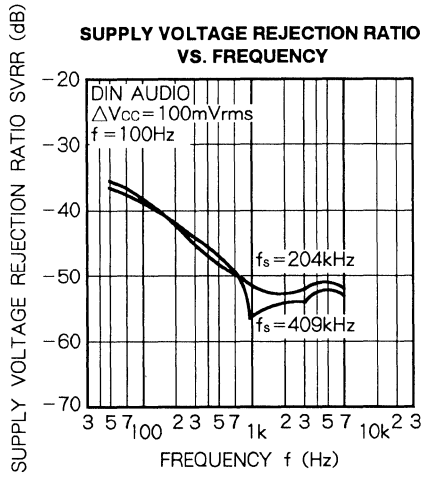


VOLTAGE GAIN VS. SUPPLY VOLTAGE

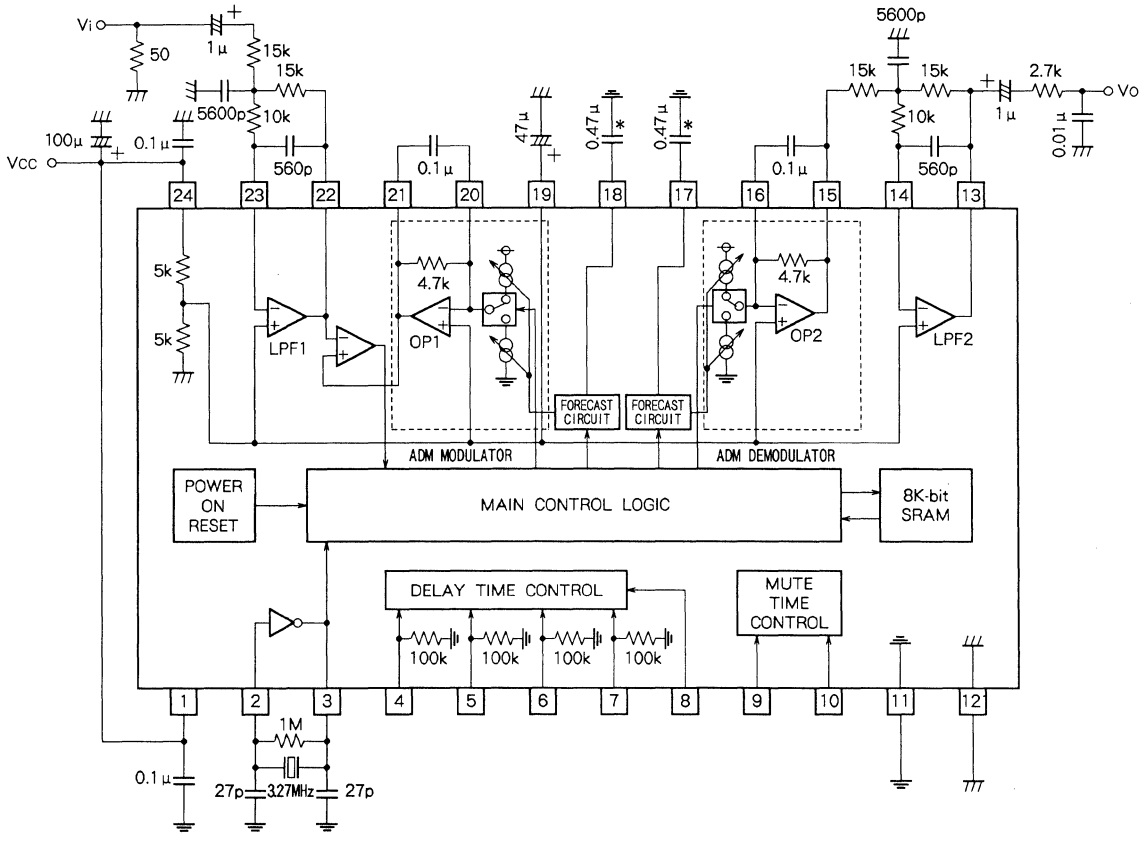


SUPPLY VOLTAGE REJECTION RATIO VS. SUPPLY VOLTAGE





APPLICATION EXAMPLE



Units Resistance : Ω
Capasitance : F

* : Uses high-quality film condenser
(Less than ±5%)

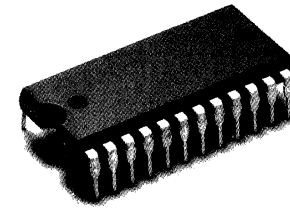
M65830P,FP
DIGITAL DELAY

DESCRIPTION

The M65830 is a CMOS IC developed to produce surround effects on TV sets and video disc players. Among the series, it has the highest degree of freedom in the selection of delay time, so it permits fine adjustments when mounted on a set.

FEATURES

- Selection of delay time in a range between 0.5msec and 32.0msec in 64 increments of 0.5msec
- Selection of delay time is controlled by serial data
- Built-in A-D, D-A converters, input/output low-pass filter, and 16K bit memory
- High sound quality is assured by simple system construction, due to A-D, D-A converters with ADM (Adaptive Delta Modulation) system
  - Output noise voltage : − 95.0dBV (typ)
  - Total harmonic distortion : 0.2% (typ)



Outline 24P4(P)

2.54mm pitch 600mil DIP
(13.0mm × 31.1mm × 3.8mm)

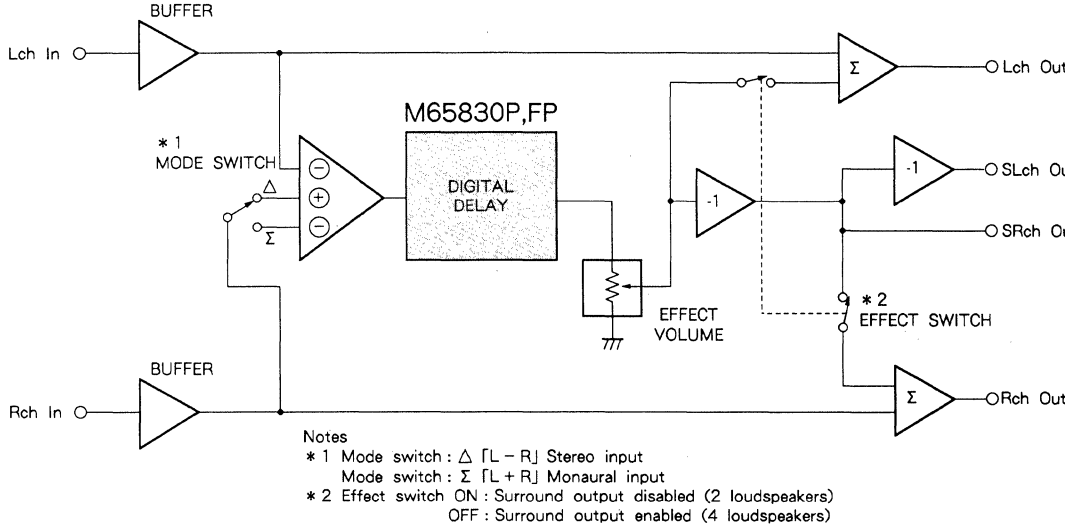
Outline 24P2W-A(FP)

1.27mm pitch 450mil SOP
(8.4mm × 15.0mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC}, V_{DD} = 4.5~5.5V
Rated supply voltage ····· V_{CC}, V_{DD} = 5V

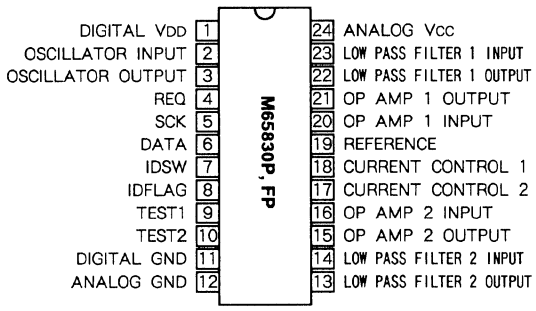
SYSTEM CONFIGURATION



Notes
*1 Mode switch : Δ 「L − R」 Stereo input
Mode switch : Σ 「L + R」 Monaural input
*2 Effect switch ON : Surround output disabled (2 loudspeakers)
OFF : Surround output enabled (4 loudspeakers)

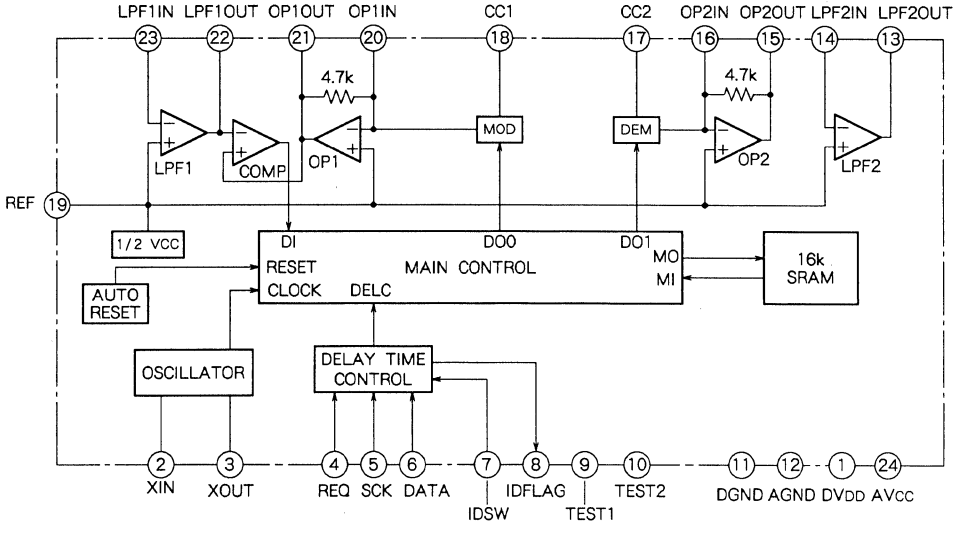
MITSUBISHI ELECTRIC

PIN CONFIGURATION



Outline 24P4(P)
24P2W-A(FP)

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Name	I/O	Function
①	V_{DD}	Digital power supply	–	
②	X_{IN}	Oscillator input	I	Connect a 2MHz ceramic oscillator
③	X_{OUT}	Oscillator output	O	Input an external clock, if used, to pin ②
④	REQ	Request	I	Data request input
⑤	SCK	Shift clock	I	Serial data shift clock input
⑥	DATA	Data	I	Serial data input
⑦	IDSW	ID switch	I	External input pin for 4th bit of ID code
⑧	IDFLAG	ID flag	O	Data input checking pulse and serial data output
⑨	TEST1	Test 1	–	L = normal mode
⑩	TEST2	Test 2	–	L = normal mode
⑪	D GND	Digital GND	–	
⑫	A GND	Analog GND	–	
⑬	LPF2 OUT	Low pass filter 2 output	O	Make up, with external C and R, a low pass filter on the output end
⑭	LPF2 IN	Low pass filter 2 input	I	
⑮	OP2 OUT	OP amp 2 output	O	Make up, with an external C, an integrator for demodulation
⑯	OP2 IN	OP amp 2 input	I	
⑰	CC2	Current control 2	–	Demodulator ADM control
⑱	CC1	Current control 1	–	Modulator ADM control
⑲	REF	Reference	–	Analog reference voltage = 1/2V_{CC}
⑳	OP1 IN	OP amp 1 input	I	Make up, with external C and R, an integrator for demodulation
㉑	OP1 OUT	OP amp 1 output	O	
㉒	LPF1 OUT	Low pass filter 1 output	O	Make up, with external C and R, a low pass filter on the input end
㉓	LPF1 IN	Low pass filter 1 input	I	
㉔	V_{CC}	Analog power supply	–	

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{CC}	Supply voltage		6.5	V
I_{CC}	Circuit current		100	mA
P_d	Power dissipation	M65830P	1	W
		M65830FP	0.8	
T_{opr}	Operating temperature		−20～+75	℃
T_{stg}	Storage temperature		−40～+125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Analog supply voltage		4.5	5	5.5	V
V_{DD}	Digital supply voltage		4.5	5	5.5	V
V_{CC}-V_{DD}	Voltage difference between V_{CC} and V_{DD}		−0.3	0	0.3	V
f_{ck}	Clock frequency		1	2	3	MHz
V_{IH}	Input voltage (H level)		0.7V_{DD}	–	V_{DD}	V
V_{IL}	Input voltage (L level)		0	–	0.3V_{DD}	V
f_{Sck}	Serial clock		–	–	4.0	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, f = 1kHz, Vo = 100mVrms, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	No signal	–	16	35	mA
Gv	Input/output voltage gain	R_L = 47kΩ	−3.5	−0.5	2.5	dB
V_{Omax}	Max. output voltage	THD = 10%	0.7	1	–	Vrms
THD	Output distortion	30kHz LPF	–	0.2	1.0	%
No	Output noise voltage	DIN-AUDIO	–	−95	−75	dBV
SVRR	Power suppression ratio	△V_{CC} = −20dBV, f = 100Hz	–	−40	−25	dB
IccS	Sleep current	Current flowing under sleep mode condition	–	12	30	mA

FUNCTION DESCRIPTION

(1) Delay time

D6	D5	D4	D3	D2	D1	Delay time(ms)
L	L	L	L	L	L	0.5
					H	1.0
				H	L	1.5
					H	2.0
			H	L	L	2.6
					H	3.1
				H	L	3.6
					H	4.1
		H	L	L	L	4.6
					H	5.1
				H	L	5.6
					H	6.1
			H	L	L	6.7
					H	7.2
				H	L	7.7
					H	8.2
	H	L	L	L	L	8.7
					H	9.2
				H	L	9.7
					H	10.2
			H	L	L	10.8
					H	11.3
				H	L	11.8
					H	12.3
		H	L	L	L	12.8
					H	13.3
				H	L	13.8
					H	14.3
			H	L	L	14.8
					H	15.4
				H	L	15.9
					H	16.4

D6	D5	D4	D3	D2	D1	Delay time(ms)
H	L	L	L	L	L	16.9
					H	17.4
				H	L	17.9
					H	18.4
			H	L	L	18.9
					H	19.5
				H	L	20.0
					H	20.5
		H	L	L	L	21.0
					H	21.5
				H	L	22.0
					H	22.5
			H	L	L	23.0
					H	23.6
				H	L	24.1
					H	24.6
	H	L	L	L	L	25.1
					H	25.6
				H	L	26.1
					H	26.6
			H	L	L	27.1
					H	27.6
				H	L	28.2
					H	28.7
		H	L	L	L	29.2
					H	29.7
				H	L	30.2
					H	30.7
			H	L	L	31.2
					H	31.7
				H	L	32.3
					H	32.8

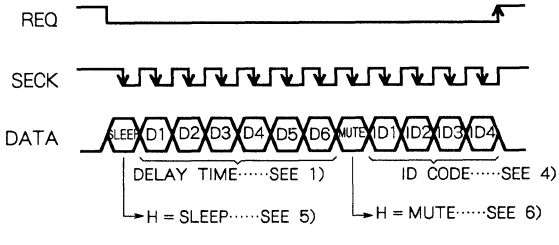
Note. D1~D6 for delay time setting correspond to D1~D6 in serial data (see (3))

(2) Sampling frequency fs

fs = 500kHz (if master clock frequency f_{ck} = 2MHz)

(3) Delay time setting

Delay time can be controlled by means of serial data inputted in the following timing from a microcomputer.



DATA is read at the negative-going edge of SCK. The last 12 bits are loaded at the positive-going edge of REQ.

(4) ID code and IDSW pins

ID code is used to control each IC in case more than one pieces of the M65830P, FP are used or other ICs are concurrently used.

IDSW is the control pin for reading serial data.

If an ID code inputted does not meet the following conditions 1 or 2, or an ID code is inputted to an external setting pin other than that indicated below (pin ⑦IDSE), the IC cannot read serial data, and the previous setting conditions remain in effect.

ID CODE SETTING TABLE

Condition	External setting pin	ID code				DATA READ
	Pin ⑦ IDSW	ID1	ID2	ID3	ID4	
1	L	L	L	H	L	Enabled
2	H	L	L	H	H	Enabled

(5) Sleep mode

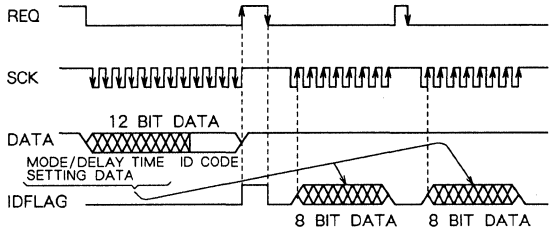
In sleep mode, ① the output is muted ; ② the internal input clock stops ; and ③ memory operation stops, so the IC becomes inactive. This mode is controlled by serial data SLEEP in the following manner : "H" : sleep mode ; "L" : normal mode.

(6) Muting

If serial data MUTE is "H," the IC compulsively performs the mute function ; if "L," muted condition is canceled.

(7) IDFLAG

The IDFLAG pin outputs a "H" signal if serial data from microcomputer or the like is correctly inputted. In addition, this pin, for checking purposes, outputs serial data containing information about the currently set operation mode.



(8) Reset

The IC is reset automatically when powered up. Then approximately 120msec later (provided that Vcc = 5V and C connected to pin ⑲ = 47μF), the reset state is automatically released. At this point delay time is set to 20.0msec.

※About reset time

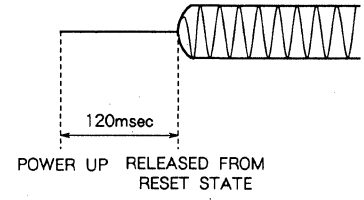
The factors that determine the IC's reset time is the internal resistance R of the IC and the value of capacitor C connected to pin ⑲(REF). The reset time is obtained by the following equation.

Reset time = 2.5 × C [μF]

Example : If external capacitor C connected to pin 19 = 47μF and Vcc = 5V :

Reset time = 2.5 × 47 = 117.5 [msec]

* Accordingly, reset time will be approximately 120msec.

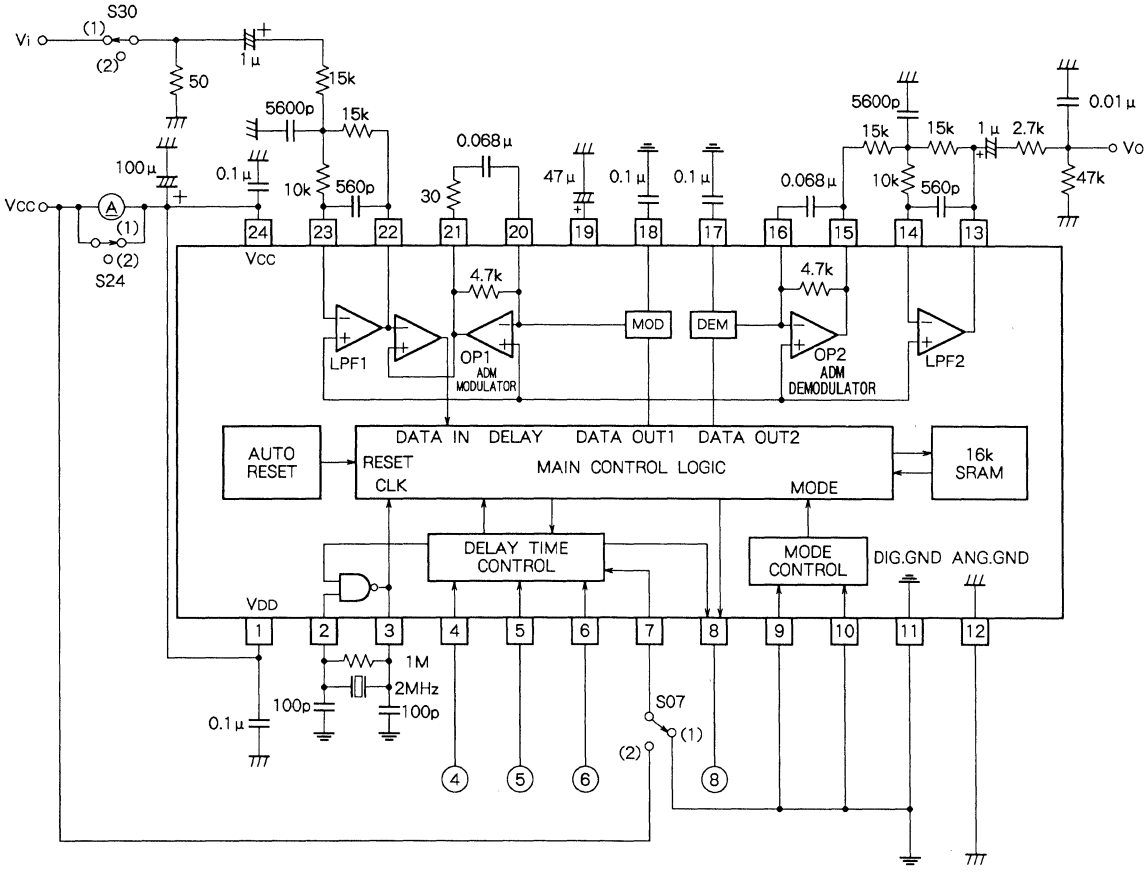


TEST CONDITIONS

Symbol	Parameter	Conditions	Pin			Switch			Remark
			4	5	6	S7	S24	S30	
Icco	Circuit current	No signal	*	*	*	#	2	2	
Gv	Voltage gain		*	*	*	#	1	1	Gv = 20log(Vo/Vi)
Td	Delay time		*	*	*	#	1	1	See 1)
Vomax	Max. output voltage	THD = 10% 30kHz L. P. F	*	*	*	#	1	1	
THD	Total high-harmonic distortion	30kHz L. P. F	*	*	*	#	1	1	
No	Output noise voltage	Vi = 0mVrms DIN AUDIO	*	*	*	#	1	2	
SVRR	Power suppression ratio	f = 100Hz △Vcc = − 20dBV	*	*	*	#	1	2	
Iccs	Sleep current	Sleep mode selected	*	*	*	#	1	1	

*……Set to "L" or "H" after serial data is inputted (See 3)
#……1 or 2 {See the ID code setting table in (See 4)}

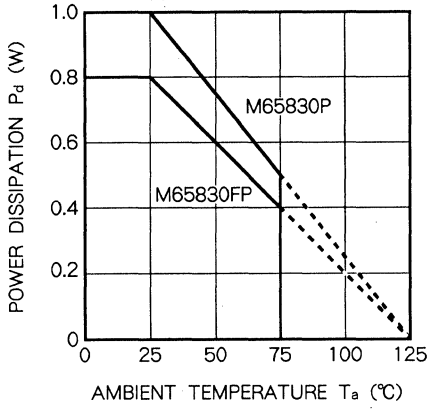
TEST CIRCUIT



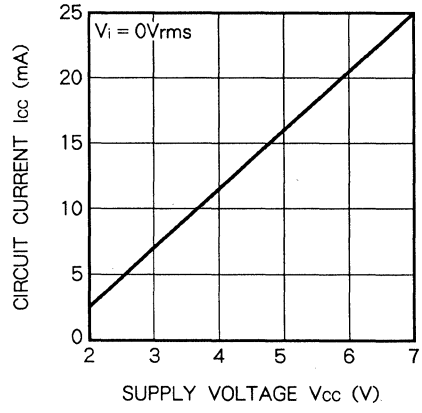
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

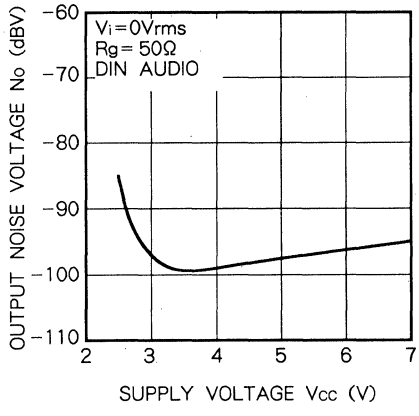
THERMAL DERATING (MAXIMUM RATING)



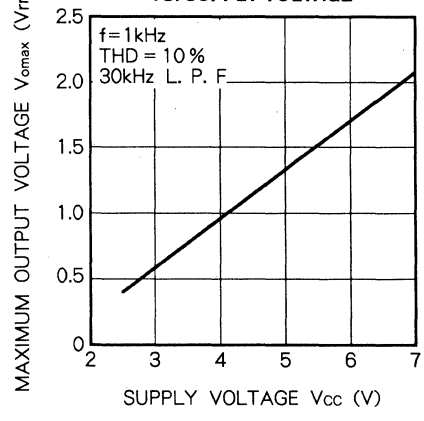
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



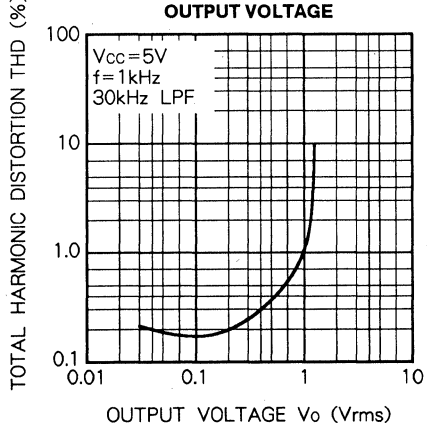
OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



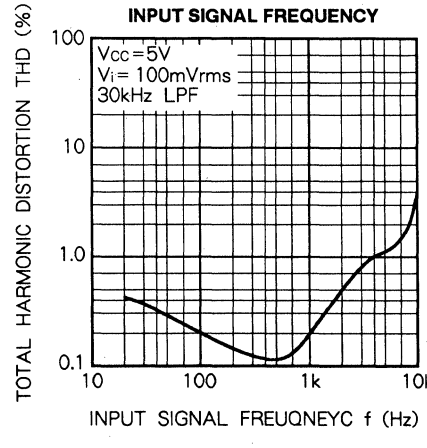
MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



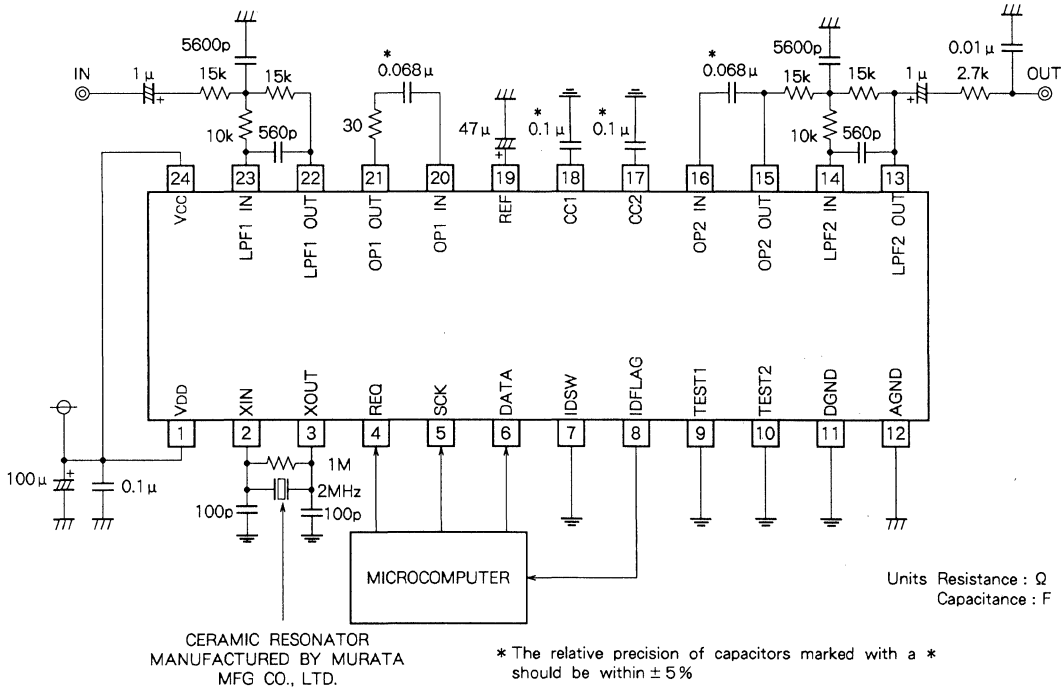
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL FREQUENCY



APPLICATION EXAMPLE



CERAMIC RESONATOR
MANUFACTURED BY MURATA
MFG CO., LTD.

* The relative precision of capacitors marked with a * should be within ± 5%

M65841SP

DIGITAL REVERBE (DIGITAL DELAY)

DESCRIPTION

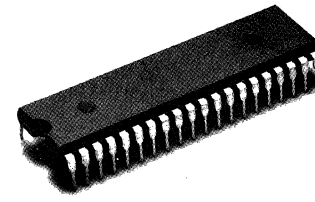
The M65841SP is an IC to generate reverberation effect.

With synthesized outputs for five digital delay lines, this IC is capable of producing the same reverberation effect as that in a church and bathroom, and is suitable for application to the reverbe unit of mini-component stereo sets, laser disc players, "karaoke" equipment, electronic musical instruments etc.

Since this IC is a higher-performance and pin-compatible version of the conventional M-50194AP, it can replace the conventional one easily to improve the performance.

FEATURES

- Built-in input low-pass filter and memory
- Reverbe, echo or surround mode is selectable.
  - Reverbe mode ····· short : Five lines for 41.0~82.0msec
    Long : Five for 82.0~163.8msec
  - Echo mode ····· Eight steps for 20.5~163.8msec
  - Surround mode ····· Eight steps for 4.1~41.0msec
  - Feedback amount is adjustable for each mode.
- ADM digital delay allows a low-cost delay system with wide dynamic range and low distortion.
  (Reverbe mode : DR = 88dB as standard, THD = 0.7% as standard, Surround mode : DR = 92dB as standard, THD = 0.3% as standard)
- Operation mode and delay time can be selected in two modes, easy mode in which operation mode and delay time are controlled by 5-bit parallel data, and microcomputer mode in which they are controlled by serial data.



Outline 40P4B

1.778mm pitch 600mil SDIP
(13.0mm × 36.7mm × 3.8mm)

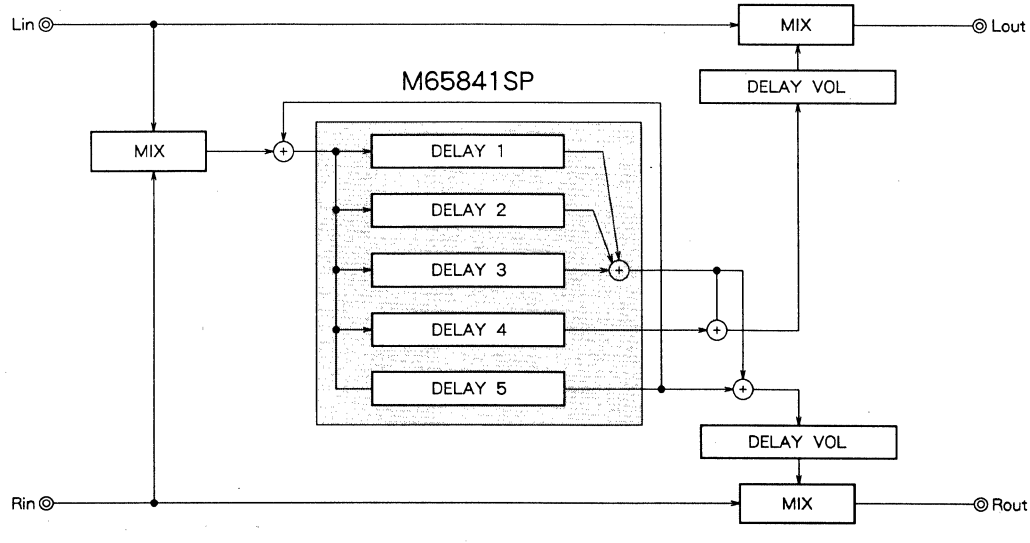
- Built-in auto mute function prevents noise generation when power is turned ON and when delay time is changed.
- Built-in auto reset circuit

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC}, V_{DD} = 4.5~5.5V

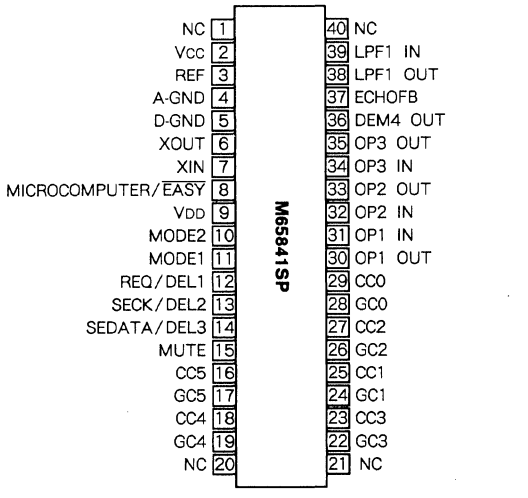
Rated supply voltage ····· V_{CC}, V_{DD} = 5V

SYSTEM CONFIGURATION



MITSUBISHI ELECTRIC

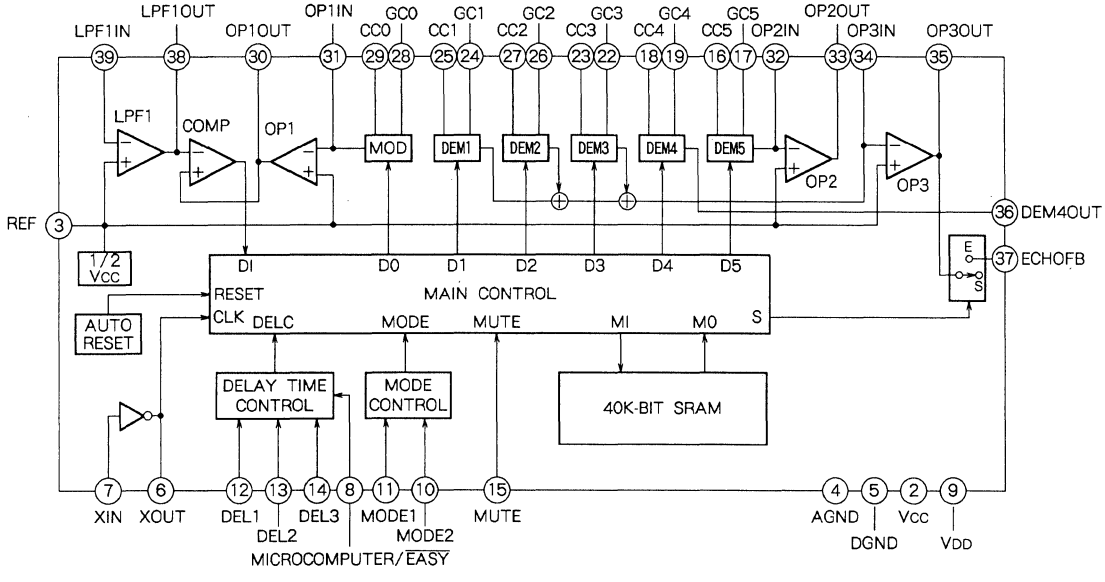
PIN CONFIGURATION



Outline 40P4B

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Name	I/O	Function	Standard output voltage
①	NC		–		–
②	V_{CC}	Analog power supply	–	To apply 4.5V to 5.5V (rating : 5V)	5V
③	REF	Reference	–	Analog regerence voltage ≒ 1/2V_{CC}	2.5V
④	A GND	Analog GND	–		–
⑤	D GND	Digital GND	–		–
⑥	X_{OUT}	Clock generator output	O		–
⑦	X_{IN}	Clock generator input	I		–
⑧	MICROCOMPUTER/$\overline{EASY}$	Microcomputer/$\overline{EASY}$	I	H = Microcomputer mode : control by serial data L = Easy mode : control by parallel data	–
⑨	V_{DD}	Digital power supply	–	To apply 4.5V to 5.5V (rating 5V)	5V
⑩	MODE2	Mode 2	I	Reverbe/echo/surround mode selection input Refer to the paragraph of FUNCTIONAL DESCRIPTION, item (1). In the microcomputer mode, fix the pin at L(Mode 2) H(Mode 1).	–
⑪	MODE1	Mode 1	I		–
⑫	REQ/DEL1	Request/delay 1	I ↓	H=Microcomputer mode:data request signal input L=Easy mode:control time setting data 1 input	–
⑬	SECK/DEL2	Serial clock/delay 2	I ↓	H=Microcomputer mode:serial data shift clock input L=Easy mode:delay time setting data 2 input	–
⑭	SEDATA/DEL3	Serial clock/delay 3	I ↓	H=Microcomputer mode:serial data input L=Easy mode:delay time setting data 3 input	–
⑮	MUTE	Mute	I ↓	Mute control, H = mute	–
⑯	CC5	Current control 5	–	ADM control of demodulator 5	0.4V when no signal
⑰	GC5	Gain control 5	–	Gain control of demodulator 5	
⑱	CC4	Current control 5	–	ADM control of demodulator 4	
⑲	GC4	Gain conrol 4	–	Gain control of demodulator 4	
⑳	NC		–		–
㉑	NC		–		–
㉒	GC3	Gain control 3	–	Gain conrol of demodulator 3	0.4V when no signal
㉓	CC3	Current control 3	–	ADM control of demodulator 3	
㉔	GC1	Gain control 1	–	Gain control of demodulator 1	
㉕	CC1	Current control 1	–	ADM control of demodulator 1	
㉖	GC2	Gain control 2	–	Gain control of demodulator 2	
㉗	CC2	Current control 2	–	ADM control of demodulator 2	
㉘	GC0	Gain control 0	–	Gain control of modulator 0	
㉙	CC0	Current control 0	–	ADM control of modulator 0	
㉚	OP1 OUT	Operational amplifier 1 output	O	To form modulating integrator by connecting external capacitor and resistor	2.5V
㉛	OP1 IN	Operational amplifier 1 input	I		2.5V
㉜	OP2 IN	Operational amplifier 2 input	I	To form demodulating integrator by connecting external capacitor and resistor	2.5V
㉝	OP2 OUT	Operational amplifier 2 output	O		2.5V
㉞	OP3 IN	Operational amplifier 3 input	I	To form demodulating integrator by connecting external capacitor and resistor	2.5V
㉟	OP3 OUT	Operational amplifier 3 output	O		2.5V
㊱	DEM4 OUT	DEM4 output	O	Demodulator 4 output	–
㊲	ECHOFB	Echo feedback	O	Feedback control for echo mode	2.5V
㊳	LPF1 OUT	Low-pass filter 1 output	O	To form input low-pass filter by connecting external capacitor and resistor	2.5V
㊴	LPF1 IN	Low-pass filter 1 input	I		2.5V
㊵	NC		–		–

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6.5	V
I_{CC}	Circuit current	150	mA
P_d	Power dissipation	1.7	W
T_{opr}	Operating temperature	−20~75	℃
T_{stg}	Storage temperature	−40~125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{CC}~V_{DD}	V_{CC}-V_{DD} potential difference		−0.3	0	0.3	V
f_{ck}	Clock frequency		3	4	6	MHz
V_{IH}	Input voltage (H level)		0.7V_{DD}	−	V_{DD}	V
V_{IL}	Input voltage (L level)		0	−	0.3V_{DD}	V
f_{SECK}	Microcomputer mode serial clock		−	−	4	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, f = 1kHz, V_i = 100mVrms, f_{ck} = 4MHz, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min	Typ	Max	
I_{CC}	Circuit current	No signal input			−	30	60	mA
V_{REF}	Reference voltage				2.0	2.5	3.0	V
G_V	I-O voltage gain	R_L = 47k Ω			−2.5	−0.5	1.5	dB
G_r	Low level I-O voltage gain	V_i = 2mVrms			−3.5	−0.5	2.5	dB
V_{Omax}	Maximum output voltage	THD = 10%			0.7	1.0	−	Vrms
THD	Output distortion	30kHz LPF	Reverbe mode	fs = 500kHz	−	0.3	1.0	%
			Echo mode	fs = 250kHz	−	0.7	1.5	%
			Surround mode	fs = 1MHz	−	0.3	1.0	%
No	Output noise voltage	Low sample rate side DIN-AUDIO	Reverbe mode	Average	−	−88	−75	dBv
				± peak	−	200	800	μV
			Echo mode	Average	−	−92	−80	dBv
				± peak	−	100	400	μV
			Surround mode	Average	−	−92	−85	dBv
				± peak	−	100	230	μV
SVRR	Supply voltage reduction ratio	△ V_{CC} = −20dBv, f = 100Hz			−	−40	−25	dB
tMUTE	Mute time	Reverbe/echo mode			515	520	525	msec
		Surround mode			122	127	132	msec
tM1	Mute operation time (Internal delay time change)	Reverbe/echo mode At time of (a) changing delay time, and (b) turning on power			257	260	263	msec
tM2	Mute operation time (Mute OFF)				257	260	263	msec
tM1	Mute operation time (Internal delay time change)	Surround mode At time of (a) changing delay time, and (b) turning on power			61	64	67	msec
tM2	Mute operation time (Mute OFF)				61	64	67	msec
I_{IHA}	Input leak current (H level)	V_i = 5V, pins 8, 10, 11			−	−	1	μA
I_{ILA}	Input leak current (L level)	V_i = 0V, pin 8, 10, 11			−	−	−1	μA
R_{PD}	Pulldown resistance	Pins 12, 13, 14, 15			25	50	75	kΩ

FUNCTION DESCRIPTION

(1) Operation mode

MODE1 (Pin ⑪)	MODE2 (Pin ⑩)	Mode	ECHOFB Output
L	H	Surround mode	OFF
H	H	Echo mode	ON
H	L	Reverbe mode	OFF
L	L	Test mode	–

(2) Delay time

DEL1	DEL2	DEL3	Surround mode		Echo mode		Reverbe mode	
			f_s	T_d	f_s	T_d	f_s	T_d
L	L	L	1M	4.1	500k	20.5	500k	81.9
H	H	L		10.2		41.0		49.2
H	L	L		14.3		61.4		61.4
L	H	L		20.5		81.9		69.6
H	L	H	1M	24.6	250k	98.3	250k	41.0
L	L	H		30.7		122.9		163.8
L	H	H		34.8		139.3		98.3
H	H	H		41.0		163.8		122.9
								139.3
								81.9

f_s = Sampling frequency (Hz)
T_d = Delay time (msec)

Note 1. In the reverbe mode, delay time changes according to the polarity at DEL3 (and independent of the polarity at DEL 1 or DEL2).

(3) Easy mode

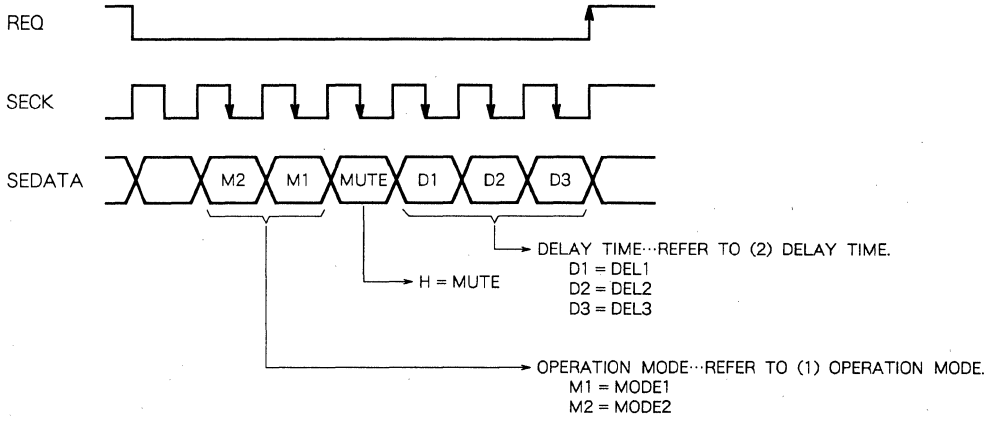
When microcomputer/$\overline{EASY}$ = L, operation mode and delay time can be controlled by parallel data input to each terminal

pin MODE1, MODE2) Operation mode···Refer to (1) Operation mode.

DEL1, DEL2, DEL3) Delay time···Refer to (2) Delay time.

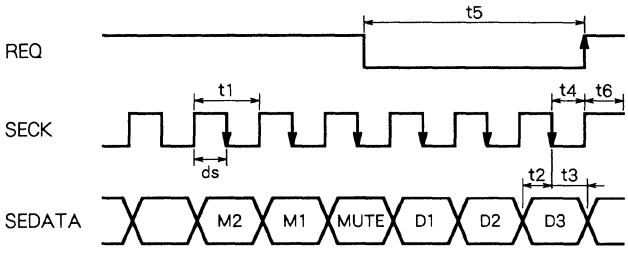
(4) Microcomputer mode

When microcomputer/$\overline{EASY}$ = H, operation mode and delay time can be controlled by serial data input at the following timing.



SEDATA is read at each fall of SECK, with the last six bits loaded at rise of REQ.

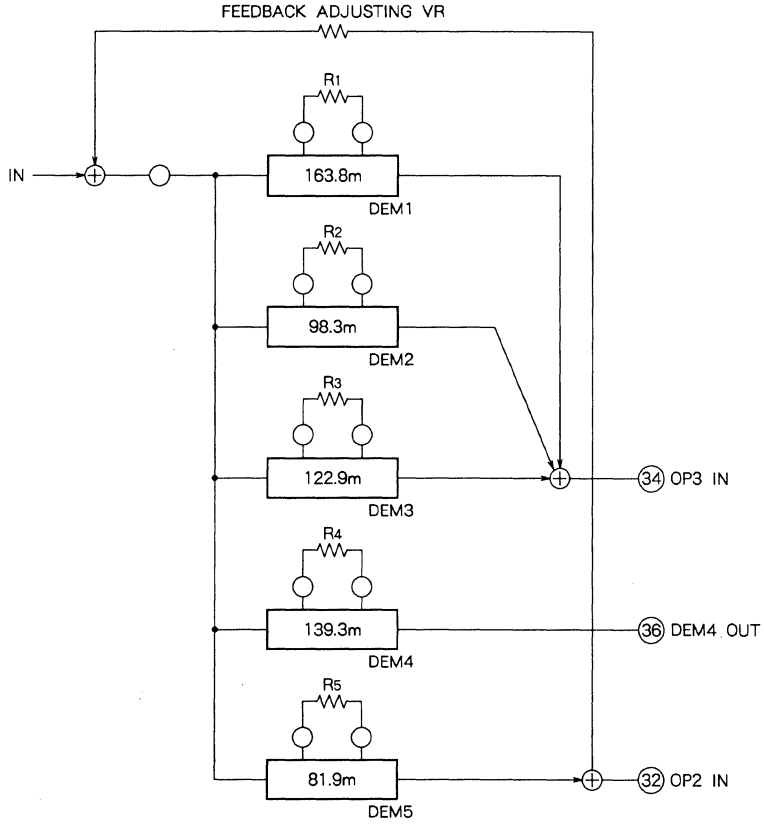
Input timing of REQ, SECK and SEDATA in the micro-computer mode is shown below :



Symbol	Name	min	typ	max	Unit
t1	SECK clock duration	250	–	–	nsec
ds	SECK pulse duty	–	50	–	%
t2	SEDATA setup time	100	t1/2	–	nsec
t3	SEDATA hold time	100	t1/2	–	nsec
t4	REQ hold time	100	–	–	nsec
t5	REQ pulse duration	100	–	–	nsec

Note. No specification for t6

(5) Reverbe construction



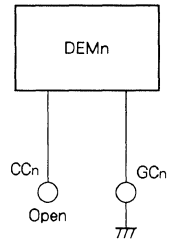
R1~R5 : Delay gain adjusting resistors
(Each delay time value is at fs = 250kHz)

(6) Selection of demodulator

Allocation of demodulator and delay time (msec)

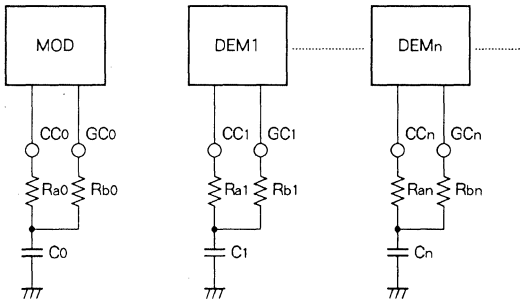
Demodulator	Surround mode	Echo mode	Reverbe mode	
			fs=500kHz	fs=250kHz
DEM1	–	–	81.9	163.8
DEM2	4.1~41.0	20.5~163.8	49.2	98.3
DEM3	–	–	61.4	122.9
DEM4	–	–	69.6	139.3
DEM5	–	–	41.0	81.9

Each modulator is turned OFF when connected as follows in the reverbe mode, so that unnecessary delay time can be eliminated.



However, demodulator 2 is used in the surround/echo mode. Therefore, demodulator 2 cannot be turned OFF if operation mode is switched over from the surround/echo mode to reverbe mode.

(7) Gain setting



The gain of DEMn (demodulator n) is determined by the ratio to R_{b0} connected to the modulator.

$$A_n = \frac{R_{b0}}{R_{bn}}$$

$$R_{an} = \frac{R_{bn}}{10}$$

$$C_n = A_n \cdot C_0$$

Typical constants on the modulator side :

R_{a0} = 7.5k Ω

R_{b0} = 75k Ω

C_0 = 0.33 μ F

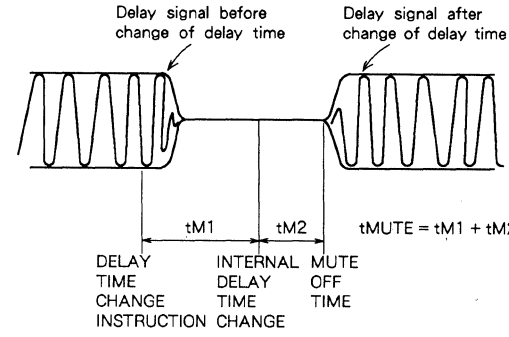
However, the gain in the surround/echo mode is determined by R_{b2} because demodulator 2 is used.

(8) Feedback output

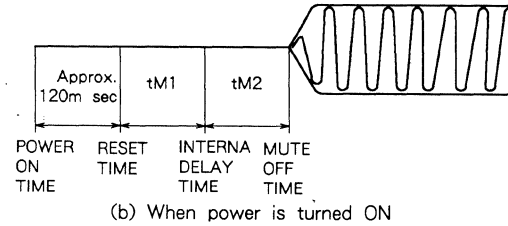
In the echo mode, signal is output from ECHOFB. Therefore, optimum multiple delay can automatically be obtained by feeding back the signal through appropriate feedback resistance from ECHOFB to the input side.

There is no feedback output in the surround or reverbe mode.

(9) Muting



(a) When delay time is changed



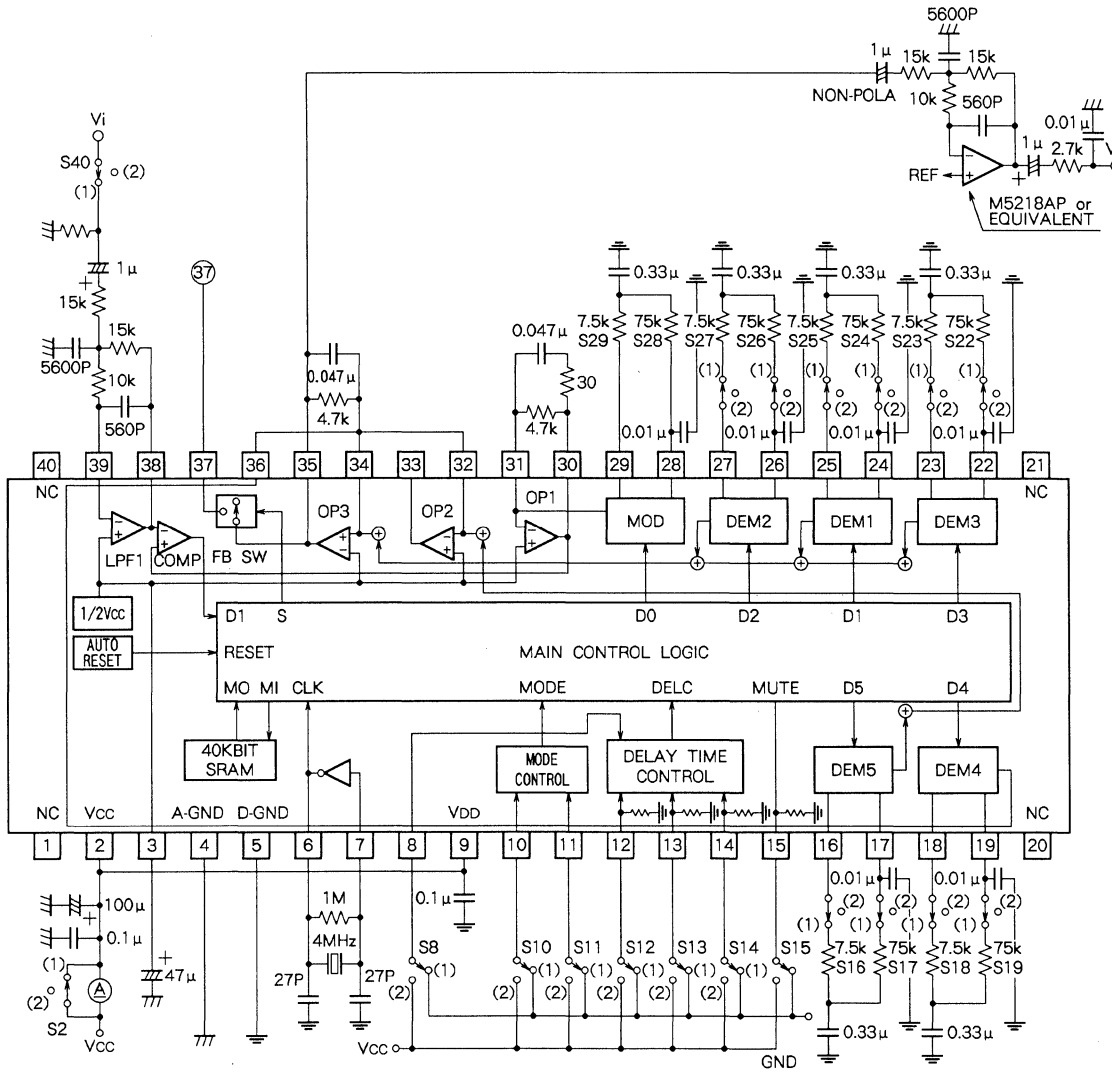
(b) When power is turned ON

(10) Reset

When reset circuit is activated, operation mode is switched to the echo mode, and Td is set to 163.8msec.

$$\begin{cases} \text{MODE1} = \text{H} \\ \text{MODE2} = \text{H} \end{cases} \qquad \begin{cases} \text{DEL1} = \text{H} \\ \text{DEL2} = \text{H} \\ \text{DEL3} = \text{H} \\ \text{MUTE} = \text{L} \end{cases}$$

TEST CIRCUIT



Units Resistance : Ω
Capacitance : F

TEST CONDITIONS

Switch setting

※···See the note under the table. *···1 or 2

Symbol	Parameter	Mode	Sampling frequency	S02	S08	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S22	S23	S24	S25	S26	S27	S40	Remark
Icco	Circuit current	Surround/echo/reverbe		2	1	*	*	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	No signal
Gvs	Voltage gain	Surround	1MHz	1	↓	2	1	*	*	*	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1	Gv = 20log (Vo/Vi) In the reverbe mode, measurement is made for individual demodulators.
Gve1		Echo	500kHz	↓	↓	2	2	*	*	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Gve2		Echo	250kHz	↓	↓	2	2	*	*	2	↓	↓	↓	↓	↓	1	1	1	1	1	1	↓	
Gvr1		Reverbe	500kHz	↓	↓	1	2	1	1	1	↓	↓	↓	↓	↓	※	※	※	※	※	※	↓	
Gvr2		Reverbe	250kHz	↓	↓	1	2	1	1	2	↓	↓	↓	↓	↓	※	※	※	※	※	※	↓	
Tdsa	Delay time	Surround	1MHz	↓	↓	2	1	1	1	1	↓	↓	↓	↓	↓	1	1	1	1	1	1	↓	Refer to FUNCTIONAL DESCIPTION. In the reverbe mode, measurement is made for individual demodulators.
Tdsb				↓	↓	↓	↓	2	2	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Tdsc				↓	↓	↓	↓	2	1	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Tdsd				↓	↓	↓	↓	1	2	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Tdse				↓	↓	↓	↓	2	1	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Tdsf				↓	↓	↓	↓	1	1	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Tdsg				↓	↓	↓	↓	1	2	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Tdsh				↓	↓	↓	1	2	2	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Tdea		Echo	500kHz	↓	↓	↓	2	1	1	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Tdeb				↓	↓	↓	↓	2	2	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Tdec				↓	↓	↓	↓	2	1	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Tded				1	1	2	2	1	2	1	1	1	1	1	1	1	1	1	1	1	1	1	
Tdee			250kHz	1	1	2	2	2	1	2	1	1	1	1	1	1	1	1	1	1	1	1	
Tdef				↓	↓	2	↓	1	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Tdeg				↓	↓	2	↓	1	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Tdeh				↓	↓	2	↓	2	2	2	↓	1	1	1	1	1	1	1	1	1	1	↓	
Tdra		Reverbe	500kHz	↓	↓	1	↓	1	1	1	↓	2	2	2	2	2	2	1	1	2	2	↓	
Tdrb				↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	2	2	2	2	1	1	↓	
Tdrc				↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	2	2	1	1	↓	↓	2	2	↓	
Tdrd				↓	↓	↓	↓	↓	↓	↓	↓	2	2	1	1	2	2	↓	↓	↓	↓	↓	
Tdre				↓	↓	↓	↓	↓	↓	1	↓	1	1	2	2	↓	↓	2	2	↓	↓	↓	
Tdrf			250kHz	↓	↓	↓	↓	↓	↓	2	↓	2	2	↓	↓	↓	↓	1	1	2	2	↓	
Tdrg				↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	2	2	2	2	1	1	↓	
Tdrh				↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	2	2	1	1	↓	↓	2	2	↓	
Tdri				↓	↓	↓	↓	↓	↓	↓	↓	2	2	1	1	2	2	↓	↓	↓	↓	↓	
Tdrj				↓	↓	1	2	1	1	2	↓	1	1	2	2	2	2	2	2	2	2	↓	

Switching setting (Cont.)

※···See the under the table. *···1 or 2

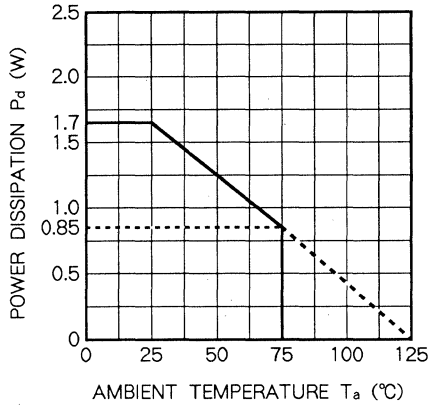
Symbol	Parameter	Mode	Sampling frequency	S02	S08	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S22	S23	S24	S25	S26	S27	S40	Remark
V_{Omaxs}	Maximum output voltage	Surround	1MHz	↓	↓	2	1	*	*	*	↓	↓	↓	1	1	1	1	1	1	1	1	↓	30kHz L.P.F THD = 10% In the reverbe mode, measurement is made for individual demodulators.
V_{Omaxe1}		Echo	500kHz	↓	↓	2	2	*	*	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
V_{Omaxe2}			250kHz	↓	↓	2	2	*	*	2	1	1	1	1	1	1	1	1	1	1	1	↓	
V_{Omaxr1}		Reverbe	500kHz	↓	↓	1	2	1	1	1	↓	※	※	※	※	※	※	※	※	※	※	↓	
V_{Omaxr2}			250kHz	1	1	1	2	1	1	2	1	※	※	※	※	※	※	※	※	※	※	1	
THDs	Higher harmonic distortion	Surround	1MHz	1	1	2	1	*	*	*	1	1	1	1	1	1	1	1	1	1	1	1	30kHz L.P.F In the reverbe mode, measurement is made for individual demodulators.
THDe1		Echo	500kHz	↓	↓	2	2	*	*	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
THDe2			250kHz	↓	↓	2	2	*	*	2	↓	↓	↓	1	1	1	1	1	1	1	1	↓	
THDr1		Reverbe	500kHz	↓	↓	1	2	1	1	1	↓	↓	↓	※	※	※	※	※	※	※	※	↓	
THDr2			250kHz	↓	↓	1	2	1	1	2	↓	↓	↓	※	※	※	※	※	※	※	※	1	
Nos	Output noise voltage	Surround	1MHz	↓	↓	2	1	*	*	*	↓	↓	↓	1	1	1	1	1	1	1	1	2	DIN AUDIO V_i = 0mVrms
Noe1		Echo	500kHz	↓	↓	2	2	*	*	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Noe2			250kHz	↓	↓	2	2	*	*	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Nor1		Reverbe	500kHz	↓	↓	1	2	1	1	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Nor2			250kHz	↓	↓	1	2	1	1	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	2	
SVRR	Supply voltage reduction ratio	Suround/echo/ reverbe		↓	↓	*	*	*	*	*	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1	$\triangle V_{CC}$=-20dBV, f=100Hz
MUTEs	Muting time	Surround	1MHz	↓	↓	2	1	2↓1	2↓1	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
MUTEe		Echo	500kHz 250kHz	↓	↓	2	2	2↓1	2↓1	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
MUTEr		Reverbe	500kHz 250kHz	1	1	1	2	1	1	2↓1	1	1	1	1	1	1	1	1	1	1	1	1	

Note. ※ indicates that measurement is made for individual demodulators in the reverbe mode.
For demodulator 2 (DEM2), measurement is made with the following switch setting. Use equivalent switch setting for measuring each of other demodulators 1 through 5.

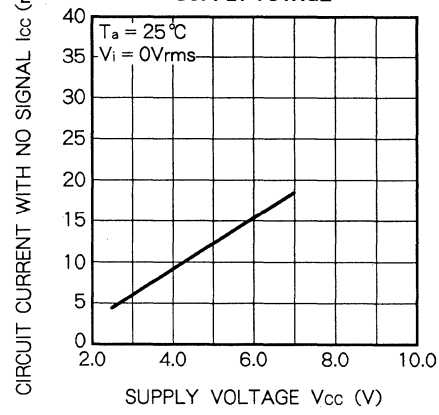
S16	S17	S18	S19	S22	S23	S24	S25	S26	S27
2	2	2	2	2	2	2	2	1	1

TYPICAL CHARACTERISTICS

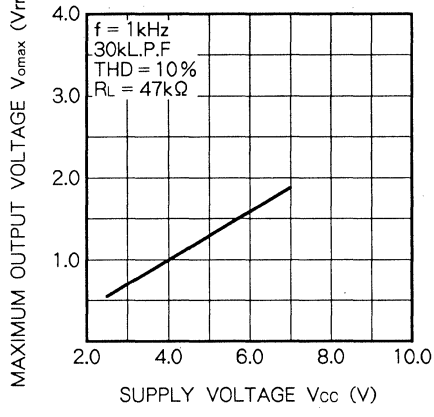
THERMAL DERATING



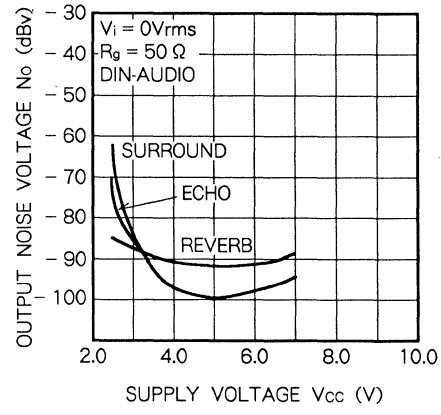
CIRCUIT CURRENT WITH NO SIGNAL VS. SUPPLY VOTAGE



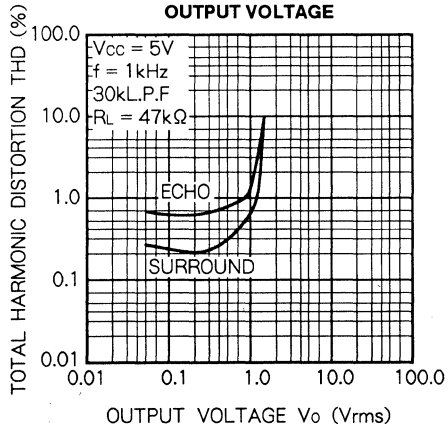
MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



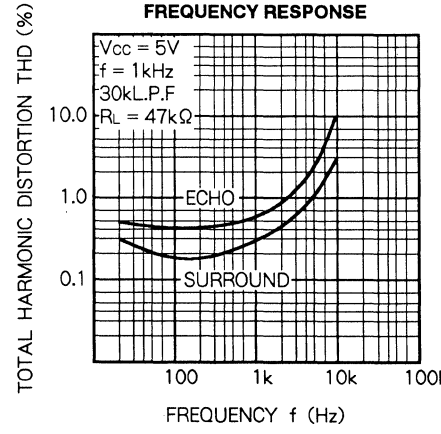
OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE

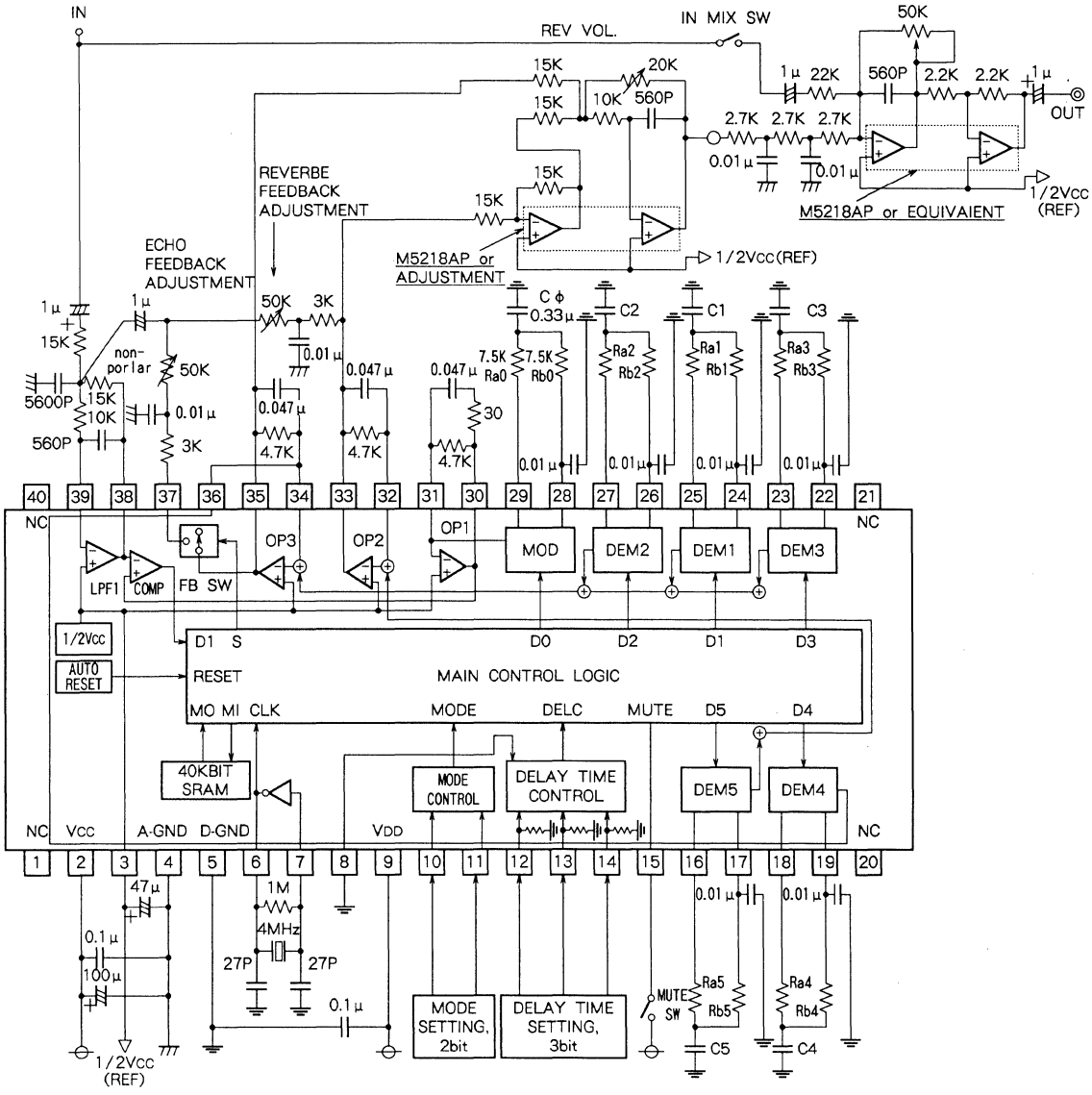


TOTAL HARMONIC DISTORTION VS. FREQUENCY RESPONSE



APPLICATION EXAMPLE

Easy mode 1ch. OUT



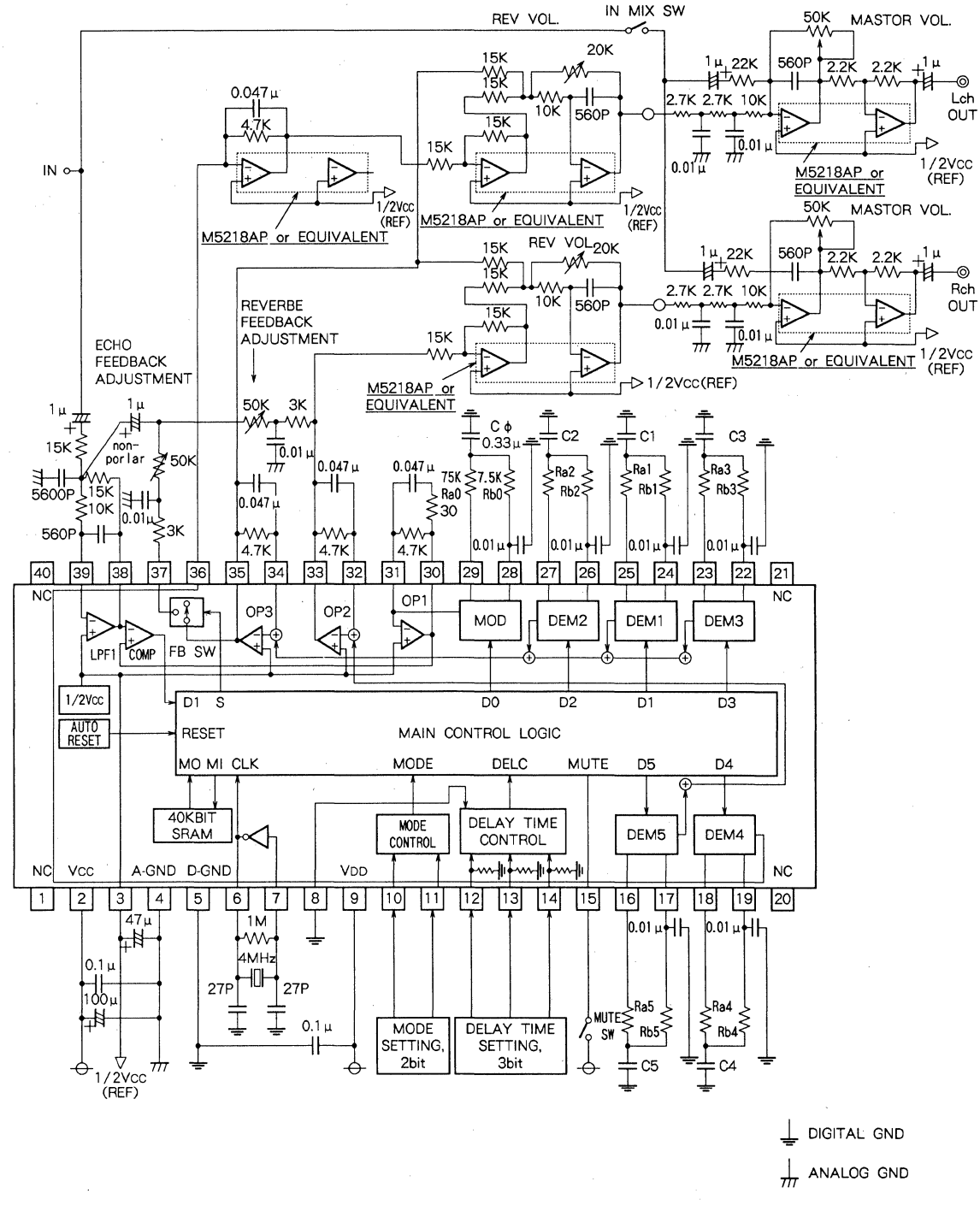
DIGITAL GND

ANALOG GND

Units Resistance : Ω
Capacitance : F

APPLICATION EXAMPLE

Easy mode 2ch. OUT



Units Resistance : Ω
Capacitance : F

MITSUBISHI ELECTRIC

M65846FP

SINGLE CHIP SURROUND PROCESSOR

DESCRIPTION

This CMOS LSI is for producing surround effects with a built-in delay circuit and mixing amplifiers. The device is suitable for adding surround effects to CD radio cassette players and miniature component stereo sets.

FEATURES

- Built-in digital delay, delay volume controller, and line mixing amplifiers make it possible to construct a surround-sound or echo system using only one chip.
- Low noise and low distortion are realized by a digital delay with built-in 16-kbit RAM.
- Two control modes, microcomputer mode and easy mode, are available to choose from. In the easy mode, disco, hall, live, and echo operation modes are preset.
- An auto mute function is built in to suppress shock noise occurring at powering up and changing mode.
- An auto reset circuit is built in, which functions at power up.
- 5V single power supply.

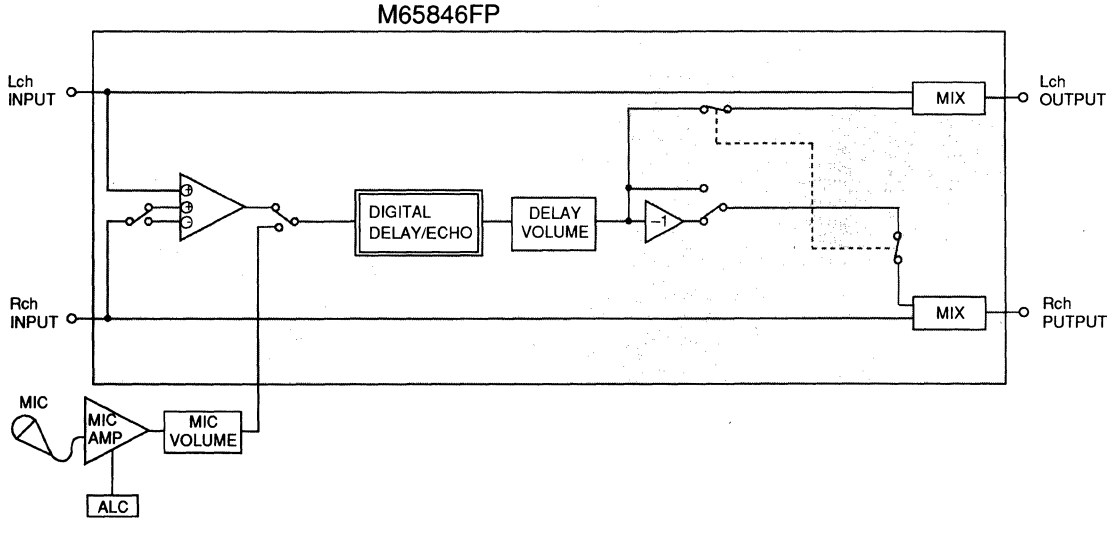
Outline 32P2W-A

1.27mm pitch 450mil SOP
(8.4mm × 20.0mm × 2.0mm)

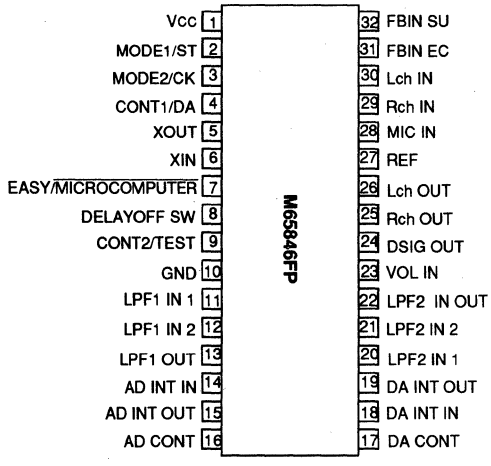
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 4.5 ~ 5.5V
Rated supply voltage ..... V_{CC} =5V
Rated clock frequency 4MHz

SYSTEM CONFIGURATION

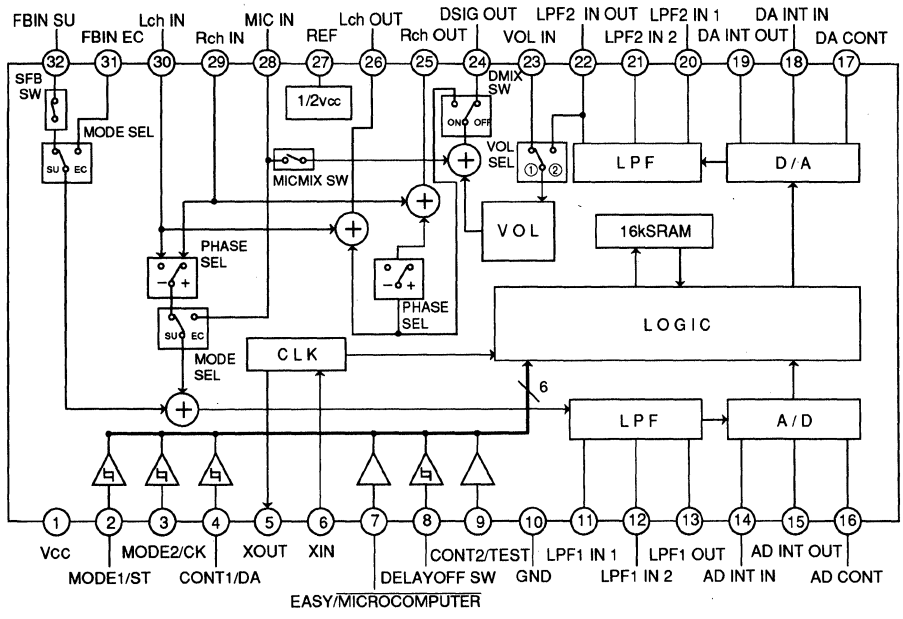


PIN CONFIGURATION



Outline 32P2W-A

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Name	I/O	Function
①	Vcc	Power supply	–	
②	MODE1/ST	Mode selector 1/Strobe	I↓	Easy mode: Input of mode setting data 1 Microcomputer mode: Strobe input via serial bus
③	MODE2/CK	Mode selector 2/clock	I↓	Easy mode: Input of mode setting data 2 Microcomputer mode: Clock input via serial bus
④	CONT1/DA	Control 1/data	I↓	Easy mode: Input of control data 1 Microcomputer mode: Data input via serial bus
⑤	XOUT	Oscillator output	O	Connect a 4-MHz ceramic filter
⑥	XIN	Oscillator input	I	
⑦	EASY/$\overline{\text{MICROCOMPUTER}}$	Easy/Microcomputer	I↓	H: Easy mode L: Microcomputer mode
⑧	DELAYOFF SW	Delay off switch	I↓	H: Delay off mode L: Normal mode
⑨	CONT2/TEST	Control 2/Test	I↓	Easy mode: Input of control data 2 Microcomputer mode: Fixed to L
⑩	GND	Ground	–	
⑪	LPF1 IN 1	Low pass filter 1 input 1	I	Prefilter placed before A/D converter for digital delay
⑫	LPF1 IN 2	Low pass filter 1 input 2	I	
⑬	LPF1 OUT	Low pass filter 1 output	O	
⑭	AD INT IN	A/D integrator input	I	With an external capacitor, these construct an integrator used as A/D converter
⑮	AD INT OUT	A/D integrator output	O	
⑯	AD CONT	A/D control	–	Determines an adaptive time constant for ADM A/D conversion
⑰	DA CONT	D/A control	–	Determines an adaptive time constant for ADM D/A conversion
⑱	DA INT IN	D/A integrator input	I	With an external capacitor, these construct an integrator used as D/A converter
⑲	DA INT OUT	D/A integrator output	O	
⑳	LPF 2 IN 1	Low pass filter 2 input 1	I	Postfilter placed after D/A converter for digital delay
㉑	LPF 2 IN 2	Low pass filter 2 input 2	I	
㉒	LPF 2 OUT	Low pass filter 2 output	O	
㉓	VOL IN	Volume input	I	Volume input
㉔	DSIG OUT	Delay signal output	O	Delay signal output
㉕	Rch OUT	R-ch output	O	R-ch mixing output
㉖	Lch OUT	L-ch output	O	L-ch mixing output
㉗	REF	Reference	–	1/2 Vcc output. Connect a filter capacitor.
㉘	MIC IN	Microphone input	I	Microphone input
㉙	Rch IN	R-ch input	I	R-ch input
㉚	Lch IN	L-ch input	I	L-ch input
㉛	FBIN EC	Feedback input of echo effect	I	Feedback signal input of echo effect
㉜	FBIN SU	Feedback input of surround-sound effect	I	Feedback signal input of surround-sound effect

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6.5	V
I_{CC}	Circuit current	100	mA
P_d	Power dissipation	650	mW
T_{opr}	Operating temperature	−20~+75	°C
T_{stg}	Storage temperature	−40~+125	°C

RECOMMENDED OPERATING CONDITIONS

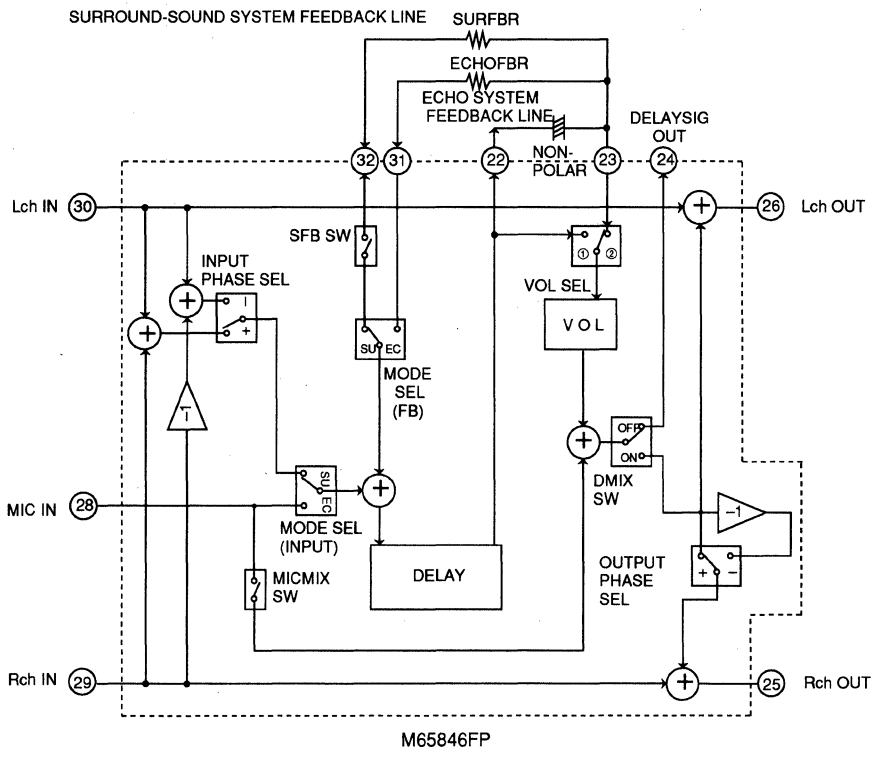
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	Input voltage ("H" level)	⑦ ⑨	0.7V_{CC}	–	V_{CC}	V
		② ③ ④ ⑧	2.2	–	V_{CC}	
V_{IL}	Input level ("L" level)	⑦ ⑨	0	–	0.3V_{CC}	V
		② ③ ④ ⑧	0	–	0.8	
f_{ck}	Clock frequency		3	4	5	MHz

ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vcc=5V, f=1kHz, Vi=200mVrms, and fck=4MHz unless otherwise noted)

Symbol		Parameter	Test conditions	Limits			Unit
				Min	Typ	Max	
Icc	All blocks	Circuit current	With no signal	–	32	70	mA
Td	Digital delay	Delay time	See 11-4-1, Delay Time Control for delay time setting	5.3	12.3	11.3	msec
				11.4	18.4	25.4	
				23.8	32.8	41.8	
				32.0	41.0	50.0	
				40.2	49.2	58.2	
				88.3	98.3	108.3	
				116.1	131.1	146.1	
Gv		Input-output gain		–3	0	3	dB
THD		Output distortion	Td=12.3msec 30kHz LPF	–	0.3	0.6	%
			Td=18.4msec 30kHz LPF	–	0.3	0.6	
			Td=32.8msec 30kHz LPF	–	0.5	1.0	
			Td=42.0msec 30kHz LPF	–	0.6	1.2	
			Td=49.2msec 30kHz LPF	–	0.6	1.2	
			Td=98.3msec 30kHz LPF	–	1.0	2.0	
			Td=131.1msec 30kHz LPF	–	1.5	3.0	
Vomax		Maximum output voltage	30kHz LPF THD=10%	0.7	1.0	–	Vrms
No		Output noise voltage	Td=12.3msec Vi=0mVrms JIS-A	–	–92	–80	dBV
			Td=18.4msec Vi=0mVrms JIS-A	–	–92	–80	
			Td=32.8msec Vi=0mVrms JIS-A	–	–92	–80	
			Td=42.0msec Vi=0mVrms JIS-A	–	–90	–75	
			Td=49.2msec Vi=0mVrms JIS-A	–	–90	–75	
			Td=98.3msec Vi=0mVrms JIS-A	–	–87	–72	
			Td=131.1msec Vi=0mVrms JIS-A	–	–85	–70	
Gv	Delay voltage	Input-output gain	Volume max.	0	3	6	dB
ATTMAX		Maximum attenuation	DELAYOFF MODE Volume min.	–	–70	–60	dB
THD		Output distortion	30kHz LPF	–	0.1	0.3	%
Vomax		Maximum output voltage	Volume max. 30kHz LPF THD=10%	1.1	1.4	–	Vrms
No		Output noise voltage	DELAYOFF MODE JIS-A	–	–98	–90	dBV
Gv	Line amplifier	Input-output gain		–3	0	–3	dB
THD		Output distortion	30kHz LPF	–	0.01	0.03	%
VoMax		Maximum output voltage	30kHz LPF ZOUT=10kΩ THD=10%	1.2	1.8	–	Vrms
No		Output noise voltageLime amplifier	DELAYOFF MODE JIS-A	–	–98	–90	dBV
CS		Channel separation	DMIXSWOFF LchIN f=400Hz RchOUT JIS-A	–	–80	–60	dB
Zi		Input impedance		21	30	–	kΩ

FUNCTIONAL DESCRIPTION

Block configuration



M65846FP

• DELAY

Creates seven kinds of delay signals between 12.3 msec and 131.1 msec.

• VOL

Sets volume attenuation in 8 steps between +3 dB and -∞ .

• INPUT PHASE SEL(IPS)

Selectes the L + R signal(+ line)or L-R signal(- line) of the input mixing amplifier.

• OUTPUT PHASE SEL(OPS)

Whether to make the R channel of the VOL output signal in-phase (+ line)or antiphase (- line)with respect to the L channel is selected.

• MODE SEL(MOS)

INPUT : Selects between input mixing amplifier signal(SU line)and microphone input signal(EC line).

FB : Selects between inputting feedback signals to surround-sound and echo lines.

*These two MODE SELs synchronize in operation.

• DMIX SW(MIX)

Selector switch for turning on/off of delay signal mixing.(Delay signals are output via pin ㉔ DSIGOUT under mixing off condition.)

• MICMIX SW(MIC)

Selector switch for turning on/off of microphone signal mixing.

• SFB SW(SFS)

Selector switch for turning feedback on/off in surround-sound mode.

(Echo mode always carries out feedback.)

• VOL SEL

Selects in easy mode between outputting delay signals to pin ㉒ LPF2OUT(line ①) with the polarities of pins ④ CONT 1 AND ① CONT ② and making direct connections in the IC(line ②).

(The selector is fixed to line ① in microcomputer mode.)

CONTROL MODE

⑦ EASY/ MICROCOMPUTER	② MODE1/ ST	③ MODE2/ CK	④ CONT1/ DA	⑨ CONT2/ TEST	Control mode	Internal VOL setting	Operation mode
L	Serial data input			L	Microcomputer mode In this mode control is carried out by serial data inputted to pins ②, ③, and ④. 8-step VOL setting is available (with VOL SEL set to line ①). Insert a capacitor between pins ㉒ and ㉓ (see 12-1).	8-step setting by serial data	–
	–			H	Test mode	–	Test mode
H	L	L	L	L	Easy mode 1 In this mode control is carried out by parallel data inputted to pins ② and ③. Fixed setting for VOL in each mode (with VOL SEL set to line ①). Insert an external capacitor between pins ㉒ and ㉓ (see 12-2-1).	0dB	Disco mode
	L	H				0dB	Hall mode
	H	L				0dB	Live mode
	H	H				–3dB	Echo mode
	L	L	L	H	Easy mode 2 In this mode control is carried out by parallel data inputted to pins ② and ③.An external VOL is used to make adjustments for VOL setting only in echo mode (with VOL SEL set to line ②). In other modes, fixed setting is made for VOL (with VOL SEL set to line ②) Insert a VOL between pins ㉒ and ㉓ (see 12-2-2).	0dB	Same as above.
	L	H				0dB	
	H	L				0dB	
	H	H				+3dB	
	L	L	H	L	Easy mode 3 In this mode control is carried out by parallel data inputted to pins ② and ③. In all the modes, an external VOL is used to make adjustments for VOL setting (with VOL SEL set to line ①). Insert a VOL between pins ㉒ and ㉓ (see 12-2-3).	+3dB	Same as above.
	L	H					
	H	L					
	H	H					
	*	*	H	H	Test mode	–	Test mode

OPERATION MODE SETTINGS (EASY MODE)

If ⑦ EASY/ microcomputer=H,operation mode settings as shown in table below are available by parallel data given to each pin.

Operation mode settings

Symbol	Control pin			DELAY TIME (Sampling frequency)	Status of each selector and switch						Delay LPF cut-off frequency
	② MODE 1	③ MODE 2	⑧ DELAY OFF SW		MODE SEL	INPUT PHASE SEL	OUTPUT PHASE SEL	SFB SW	DMIX SW	MIC MIX SW	
Disco mode	L	L	L	18.4 msec (667kHz)	SU line	– line	– line	ON	ON	ON	7.0kHz
			H	Through outputs of input signals (R-ch IN and L-ch IN) (with clock off).							
Hall mode	L	H	L	49.2 msec (333kHz)	SU line	– line	– line	ON	ON	ON	
			H	Through outputs of input signals (R-ch IN and L-ch IN) (with clock off).							
Live mode	H	L	L	32.8 msec (500kHz)	SU line	+ line	– line	OFF	ON	ON	
			H	Through outputs of input signals (R-ch IN and L-ch IN) (with clock off).							
Echo mode	H	H	L	131.1 msec (125kHz)	EC line	+ line	+ line		ON	ON	3.0kHz
			H	Through outputs of input signals. (Delay signals are output at pin ㉔.)							

If pin ⑧ DELAY OFF SW is at H, the delay off mode takes place and input signals are transmitted as through outputs.

∗ Values for DELAY TIME and sampling frequencies are those obtained under the condition fck=4MHz.

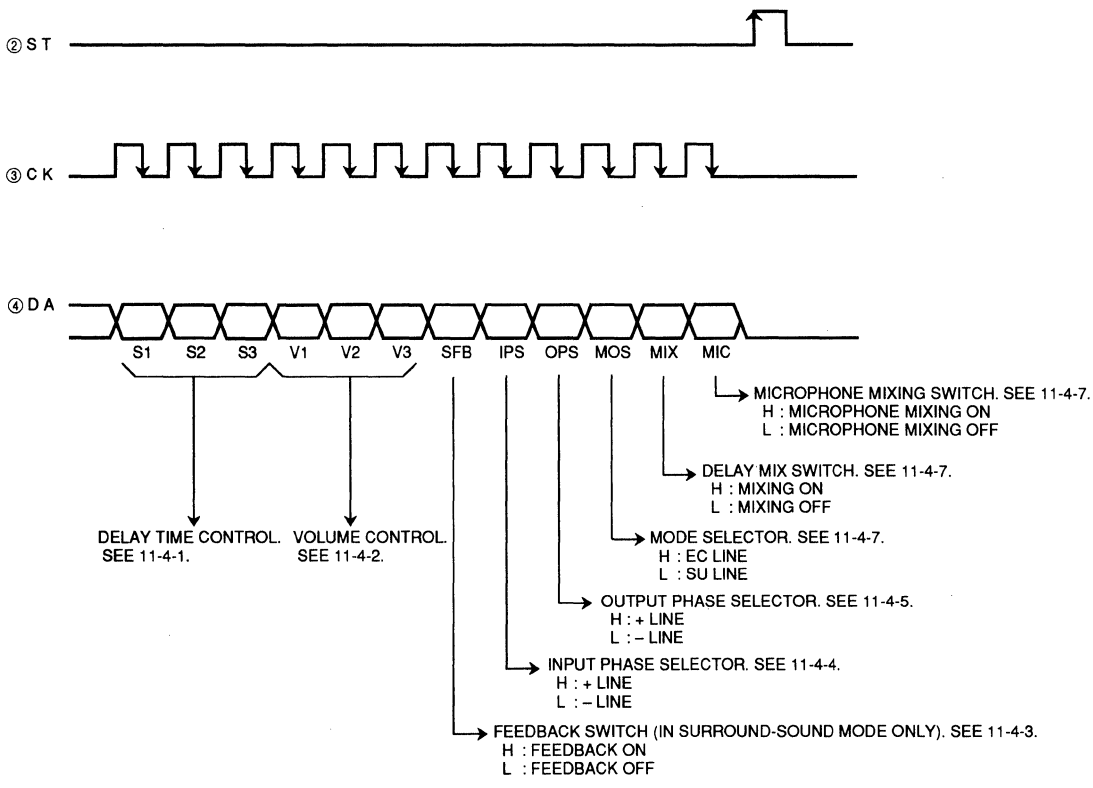
VOL Settings (The table below shows setting values of internal VOL in each mode.)

Control mode / Operation mode		Easy mode 1	Easy mode 2	Easy mode 3
	④ CONT1	L	L	H
	⑨ CONT2	L	H	L
Disco mode		0 dB	0 dB	+3 dB
Hall mode		0 dB	0 dB	
Live mode		0 dB	0 dB	
Echo mode		–3 dB	+3 dB	

∗ VOL attenuation in easy mode 3 and easy mode 2(echo mode)is controlled by an external VOL.

OPERATION MODE SETTINGS (MICROCOMPUTER MODE)

If ⑦ EASY/ microcomputer=L, operation mode is controlled by 12-bit serial data inputted in accordance with the following timing.



DA(data)is read at the falling edge of CK(clock). Preceding 12 bits are loaded at the rising edge of ST(strobe).

DELAY TIME CONTROL

Control Data			DELAY TIME	Delay LPF
S1	S2	S3	(Sampling frequency)	cut-off frequency
L	L	L	12.3 msec (1MHz)	7.0kHz
L	L	H	18.4 msec (667kHz)	
L	H	L	32.8 msec (500kHz)	
L	H	H	41.0 msec (400kHz)	
H	L	L	49.2 msec (333kHz)	
H	L	H	98.3 msec (167kHz)	3.0kHz
H	H	L	131.3 msec (125kHz)	
H	H	H	Delay off mode	(with clock off)

* When powered up, the auto reset function makes settings:S1=L, S2=L, and S3=L.

VOLUME CONTROL

Control Data			VOL attenuation
V1	V2	V3	
H	H	H	+3dB
H	H	H	0dB
H	L	H	–3dB
H	L	L	–6dB
L	H	H	–9dB
L	H	L	–12dB
L	L	L	–15dB
L	L	L	$-\infty$

* When powered up, the auto reset function makes settings:V1=L, V2=L, and V3=L

FEEDBACK SWITCH (In surround mode only)

Control Data	Operation switch	Remark
SFB	SFB SW	
L	OFF	Feedback OFF
H	ON	Feedback ON

* When powered up, the auto reset function makes setting:SFB=L.

INPUT PHASE SELECTOR

Control Data	Operation selector	Remark
IPS	INPUT PHASESEL	
L	– line	L–R signal is selected
H	+ line	L+R signal is selected

* When powered up, the auto reset function makes setting:IPS=L.

OUTPUT PHASE SELECTOR

Control Data	Operation selector	Remark
OPS	INPUT PHASESEL	
L	– line	L and R channels are in antiphase
H	+ line	L and R channels are in phase

* When powered up, the auto reset function makes setting:OPS=L.

MODE SELECTOR

Control Data	Operation selector
MOS	MODESEL
L	SU line
H	EC line

* When powered up, the auto reset function makes setting:MOS=L.

DELAY MIX SWITCH

Control Data	Operation switch	Remark
MIX	DMIXSW	
L	OFF	Mixing OFF
H	ON	Mixing ON

* When powered up, the auto reset function makes setting:MIX=L.

MICROPHONE MIXING SWITCH

Control Data	Operation switch	Remark
MIC	MICMIXSW	
L	OFF	Microphone mixing OFF
H	ON	Microphone mixing ON

* When powered up, the auto reset function makes setting:MIC=L.

DELAY OFF MODE

The delay off mode is for the MIX amplifier to avoid the influences of digital noise when the digital delay is not in use.

- In easy mode(pin⑦=H) : If DELAY OFF SW(pin⑧)=H, delay off mode takes place.)

Operation mode	⑧ DELAY OFFSW	IC operation
Disco	H	Clock and delay function stopped. (through outputs of input signals)
Hall		
Live		
Echo	H	DMIXSW=OFF (Through outputs of input signals)

* In echo mode delay signals are output at pin ㉔.

- In microcomputer mode(pin⑦=L) : If DELAY OFF SW(pin⑧)=H, or S1=S2=S3=H in serial data, the delay off mode takes place.)

Serial data S1=S2=S3	⑧ DELAY OFFSW	IC operation
H	L	Clock and delay function stopped. (Through outputs of input signals)
—	H	

AUTO RESET

Settings are reset automatically when the IC is powered up. The reset state is automatically canceled approximately 120 msec*1 after powering up(Vcc=5V and the capacitor connected to pin C ㉗ =47μF).

By auto reset, operation mode settings become as follows.

- Easy mode(pin ⑦ =H)

  MODE 1=Polarity of pin ②

  MODE 2=Polarity of pin ③

- Microcomputer mode(pin ⑦ =L)

  S1=L V1=L SFB=L MOS=L

  S2=L V2=L IPS=L MIX=L

  S3=L V3=L OPS=L MIC=L

*1About reset time

Reset time is determined by the IC's internal resistance and the value of the capacitor connected to pin ㉗. It is obtained by the following equation.

Reset time(msec)=2.5×C(μF)

Example:If C=47μF,

Reset time=2.5×47=117.5(msec)

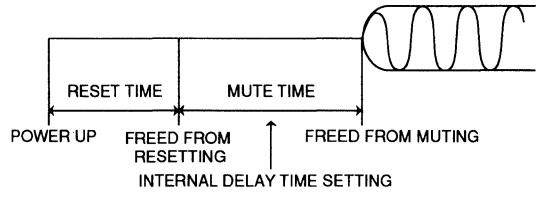
As shown above, reset time is approximately 120 msec.

AUTO MUTE FUNCTION

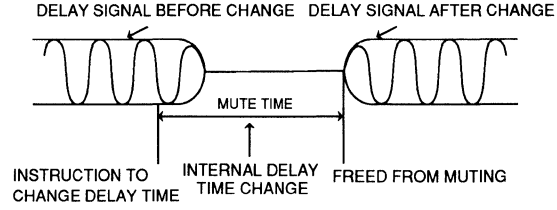
The IC carries out auto mute function at the time of powering up, delay time setting change, and canceling delay off mode, in order to suppress shock noise that the digital delay may produce.

- At power up

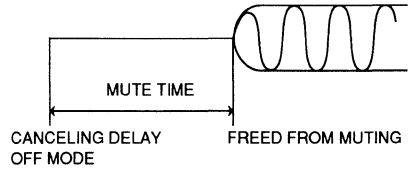
  * Transient noise common with power up occurs.



- At delay time setting change



- At canceling delay off mode

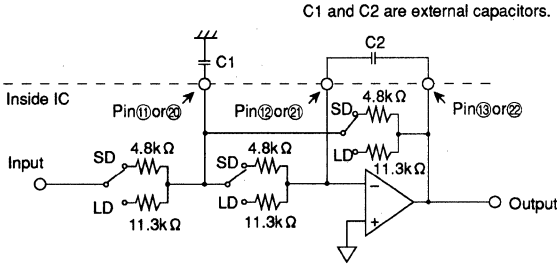


Mute time changes depending on set(or preset)delay time.

DELAY TIME	Mute time
12.3~49.2 msec	123 msec
98.3, 131.1 msec	328 msec

INPUT AND OUTPUT LPFS FOR THE DIGITAL DELAY

The input and output LPFs for the digital delay are configured as shown in figure below.



The accuracy of the internal resistance of the IC is approximately ±30%.

DELAY TIME	S W
12.3~49.2 msec	SD line (SHORT DELAY)
98.3, 131.1 msec	LD line (LONG DELAY)

Cut-off frequencies(fc)are given as follows.

• Short delay(SD)

$$fc=\frac{1}{2\pi\times4.8k\Omega\times\sqrt{C1\times C2}}$$

• Long delay(LD)

$$fc=\frac{1}{2\pi\times11.3k\Omega\times\sqrt{C1\times C2}}$$

Quality factor(Q)is given by the following equation for both short and long delays.

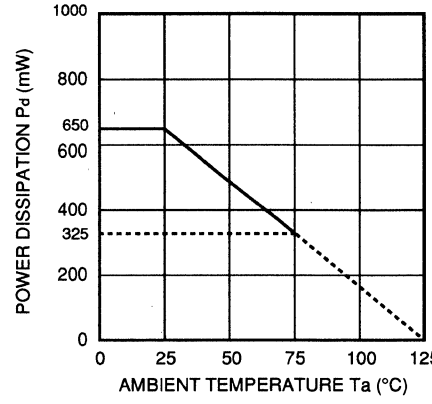
$$Q=\frac{1}{3}\sqrt{\frac{C1}{C2}}$$

External capacitors determine the cut-off frequencies. Under the condition C1=0.01μF and C2=0.0022μF, constants set to the M65846FP are:

Short delay:fc=7.0kHz;Q=0.71

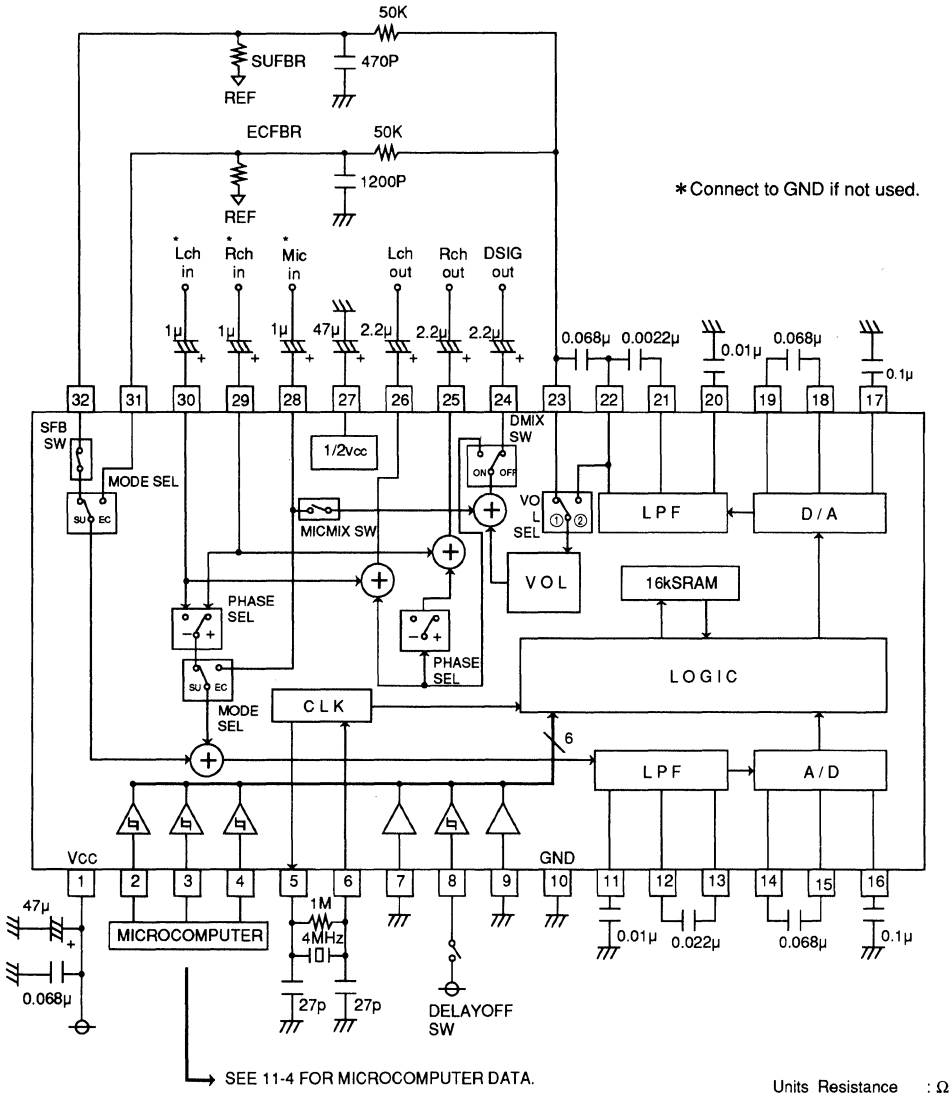
Long delay:fc=3.0kHz

THERMAL DERATING CURVE



APPLICATION EXAMPLES

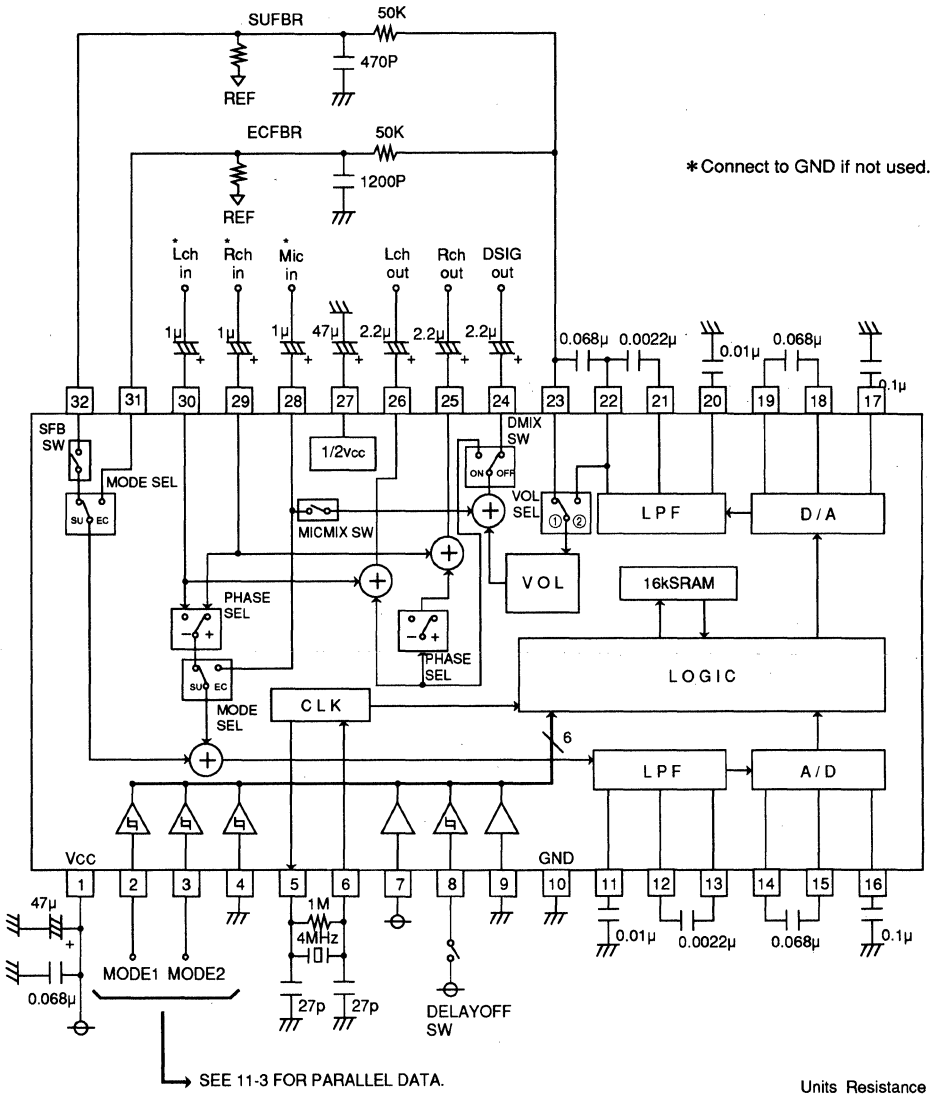
Microcomputer mode



Units Resistance : Ω

Capacitance : F

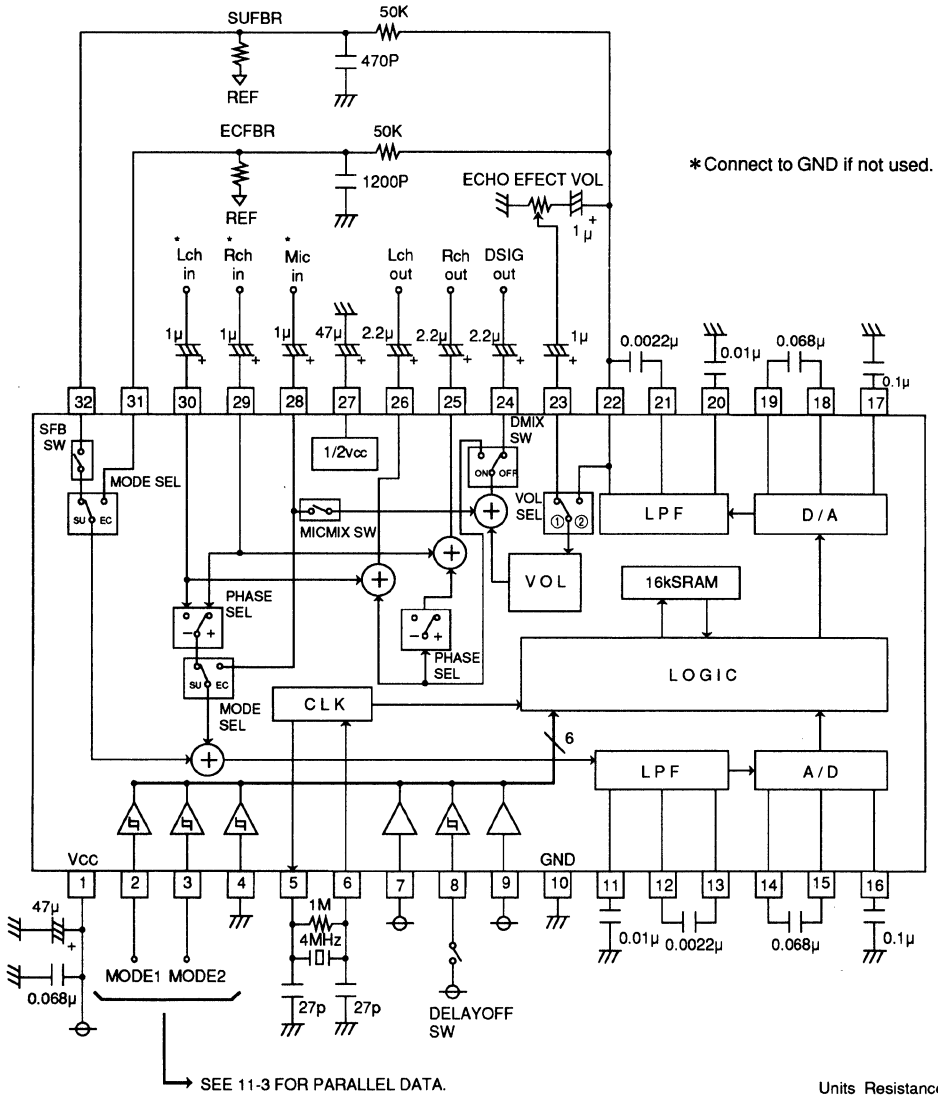
Easy mode 1



Units Resistance : Ω
Capacitance : F

Operation mode	VOL set value	VOL SEL operation
Disco mode	0dB	Line ①
Hall mode	0dB	
Live mode	0dB	
Echo mode	–3dB	

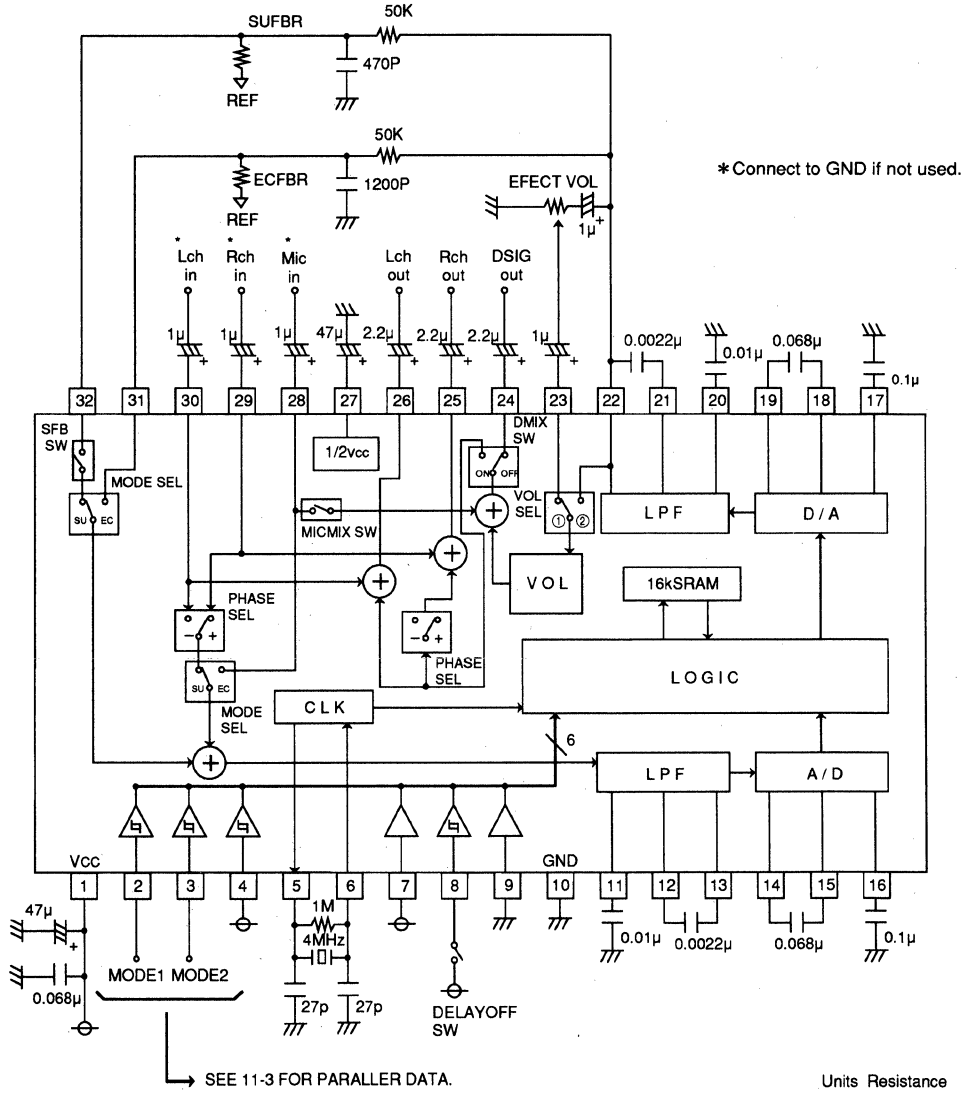
Easy mode 2



Units Resistance : Ω
Capacitance : F

Operation mode	VOL set value	VOL SEL operation
Disco mode	0dB	Line ②
Hall mode	0dB	
Live mode	0dB	
Echo mode	Adjust by ECHO EFFECT VOL.	Line ①

Easy mode 3



Units Resistance : Ω
Capacitance : F

Operation mode	VOL set value	VOL SEL operation
Disco mode	Adjust by EFFECT VOL.	Line ①
Hall mode		
Live mode		
Echo mode		

M69032P

DOLBY PRO LOGIC SURROUND DECODER

DESCRIPTION

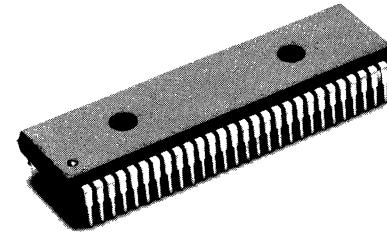
M69032P IC was developed for dolby pro logic surround systems.

This IC has almost all functions necessary for dolby pro logic surround decoders, such as input autobalanc, noise sequencer and adaptive matrix. By combining this IC with M65830P digital delay IC, a 2 chip dolby prologic surround system can be formed.

Note : This device is produced under the license of dolby laboratories licensing corporation. dolby and □□ are the registered trademarks of dolby laboratories licensing corporation.

FEATURES

- Has almost all functions necessary for dolby prologic surround decoders
- Input autobalance
- Input buffer
- Noise sequencer ;
  controls noise generator in sequence with 2-bit digital data
- Adaptive matrix
- Center mode control
  Switches between ON and OFF, as well as between NORMAL, PHANTOM and WIDEBAND
- Modified dolby B type noise reduction
- Operation mode control
  4-channel (left, right, center, surround), 3-channel (left, right, and center), 2-channel (input through)
- L + R output and L − R output



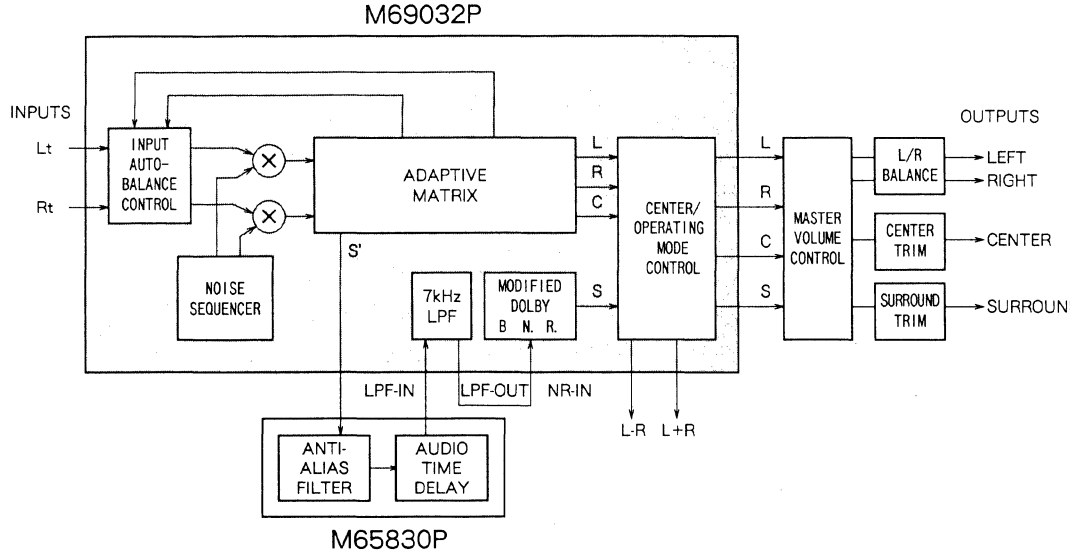
Outline 56SDIP

RECOMMENDED OPERATING CONDITIONS

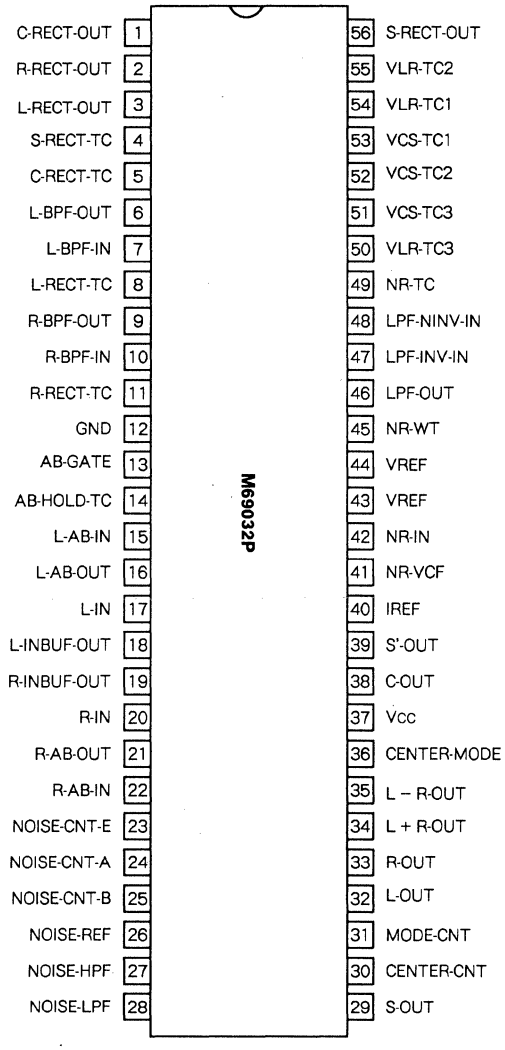
Supply voltage range ..... V_{CC} = 9~13V

Rated supply voltage ..... V_{CC} = 12V

SYSTEM CONFIGURATION

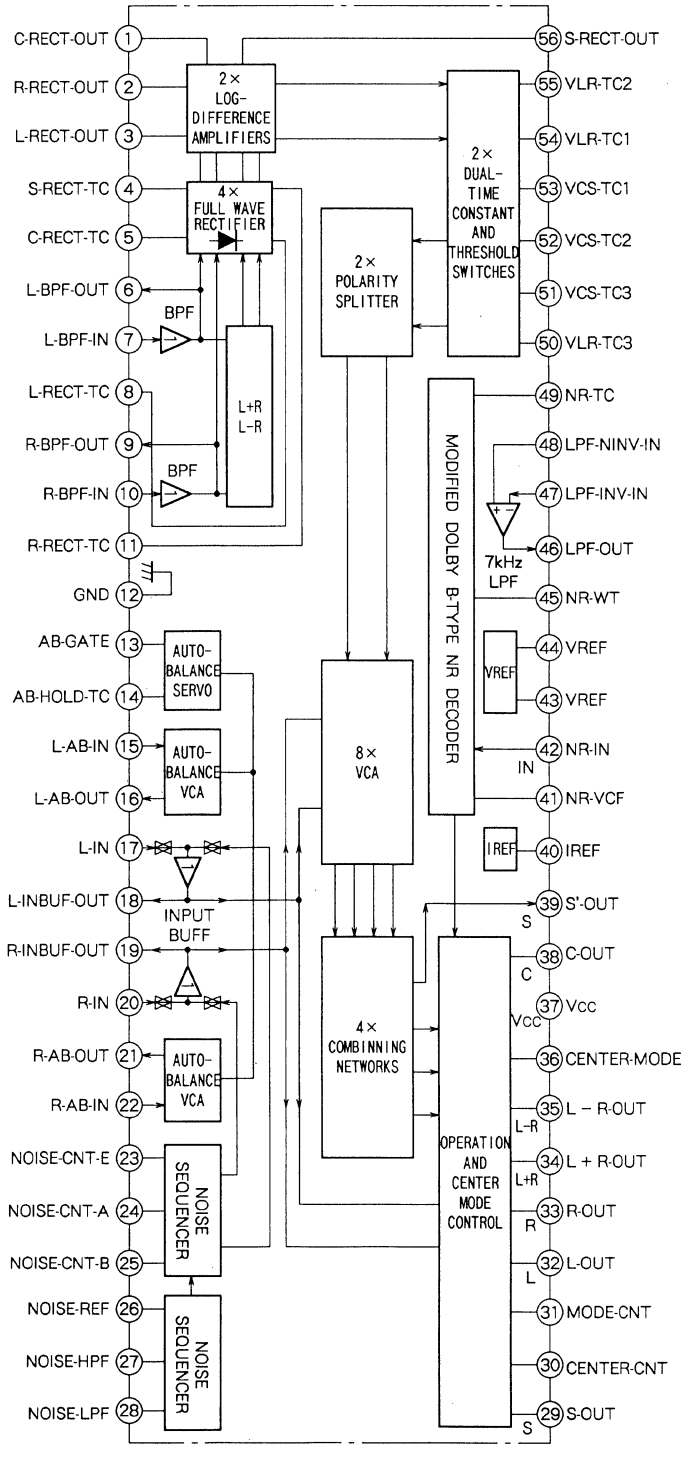


PIN CONFIGURATION



Outline 56SDIP

IC INTERNAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	15	V
P_d	Power dissipation	700	mW
T_{opr}	Operating temperature	−20～+75	℃
T_{stg}	Storage temperature	−40～+125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{op}	Supply voltage			9.0	12.0	13.0	V
I_{CC}	Circuit current		No signal	−	34.0	40.0	mA
V_{ref}	Reference voltage		No signal	3.5	4.0	4.4	V
$V_{c\text{-}2ch}$	Control SW threshold	2ch mode	MODE-CNT PIN	0.0	−	0.8	V
$V_{c\text{-}3ch}$		3ch mode	MODE-CNT PIN	−	OPEN	−	−
$V_{c\text{-}4ch}$		4ch mode	MODE-CNT PIN	3.8	−	7.0	V
$V_{c\text{-}con}$		Center on/off	CENTER-CNT PIN	2.4	−	7.0	V
$V_{c\text{-}cof}$			CENTER-CNT PIN	0.0	−	0.8	V
$V_{c\text{-}non}$		Noise seq. on/off	NOISE-CNT-E PIN	0.0	−	0.8	V
$V_{c\text{-}nof}$			NOISE-CNT-E PIN	3.2	−	7.0	V
$V_{c\text{-}nsH}$		Noise seq. channel select H	NOISE-CNT-A and NOISE-CNT-B PIN	3.2	−	7.0	V
$V_{c\text{-}nsL}$		Noise seq. channel select L	NOISE-CNT-A and NOISE-CNT-B PIN	0.0	−	0.8	V

ELECTRICAL CHARACTERISTICS (Ta = 25℃, Vcc = 12V, 0dB Reference is 300mV/1kHz at C-OUT, unless otherwise noted)

1. MODIFIED B NOISE REDUCTION (0dB Reference is 300mV/100Hz at S-OUT)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
GV-NR	Voltage gain	V_{in} = 0dBd, f = 100Hz	−	9.0	−	dB
Dec1	Decode Responce	V_{in} = 0dBd, f = 1kHz	−1.6	−0.1	1.4	dB
Dec2		V_{in} = −15dBd, f = 1.4kHz	−3.0	−1.5	0.0	dB
Dec3		V_{in} = −20dBd, f = 1.4kHz	−4.9	−3.4	−1.9	dB
Dec4		V_{in} = −40dBd, f = 5kHz	−6.8	−5.3	−3.8	dB
THD-NR	T.H.D	V_{in} = 0dBd, f = 1kHz	−	0.07	0.3	%
HR-NR	Headroom	V_{CC} = 9V at THD = 1%	15.0	17.0	−	dB
SN-NR	S.N Ratio	R_g = 0Ω, weighted CCIR/ARM	76	82	−	dB

2. NOISE SEQUENCER

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{no}	Output noise level			−15	−12.5	−10	dB
$V_{no\text{-}L}$	Output noise level accuracy relative to Cch	L ch		−0.5	0.0	0.5	dB
$V_{no\text{-}R}$		R ch		−0.5	0.0	0.5	dB
$V_{no\text{-}S'}$		S' ch		−0.5	0.0	0.5	dB

3. ADAPTIVE MATRIX

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Vol	Output level accuracy relative to Cch L, R, S'ch out		− 0.5	0	0.5	dB
Mr	Matrix rejection relative to Lch R, C, S'ch out		25.0	40.0	−	dB
THD-AM	T.H.D L, R, C, S'ch out		−	0.02	0.20	%
HR-AM	Headroom L, R, C, S'ch out	Vcc = 9V at T.H.D = 1 %	15.0	15.7	−	dB
SN-AM	Signal to noise ratio L, R, C, S'ch out	R_g = 0 Ω, weighted CCIR/ARM	76	83	−	dB

4. AUTO BALANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CPR	Capture range		−	± 5	−	dB
CER	Error collection		−	± 4	−	dB
THD-AB	T.H.D Lt, Rt, out		−	0.03	0.20	%
HR-AB	Headroom Lt, Rt, out	Vcc = 9V at T.H.D = 1 %	15.0	17.0	−	dB
SN-AB	S/N Lt, Rt, out	R_g = 0 Ω, weighted CCIR/ARM	78	83	−	dB

5. L+R & L−R OUTPUT

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Vol-OP	Output level accuracy relative to Cch L + R, L−R ch		−1.0	0	1.0	dB
THD-OP	T.H.D		−	0.02	0.20	%
HR-OP	Headroom	Vcc = 9V at T.H.D = 1 %	15.0	17.0	−	dB
SN-OP	S/N	R_g = 0 Ω, weighted CCIR/ARM	76	92	−	dB

FUNCTION DIAGRAMS

1. OPERATION MODE

Mode \ Pin name (Pin No)	MODE-CNT (Pin ㉛)	Note
2CH (Lt,Rt,S')	L	S' = Lt − Rt or Noise
3CH (L,C,R,S')	High Z	S' = Lt − Rt or Noise
4CH (L,C,R,S'S)	H	

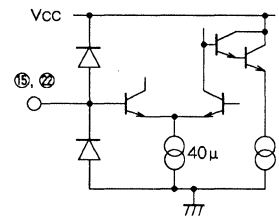
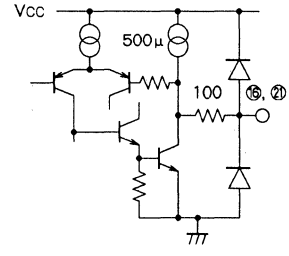
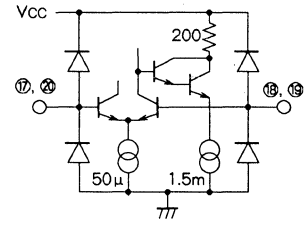
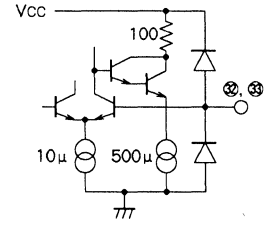
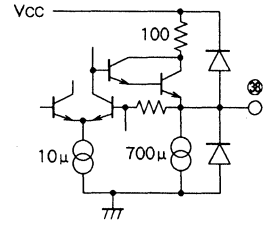
2. CENTER MODE

Mode \ Pin name (Pin No)	CENTER-CNT (Pin ㉚)	CENTER-MODE (Pin ㉘)
Center off	L	X
Normal	H	0.22 µF
Phantom	H	OPEN
Wideband	H	10 µF

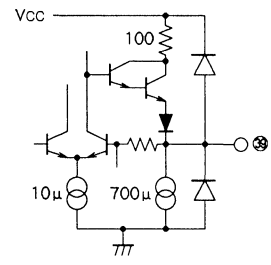
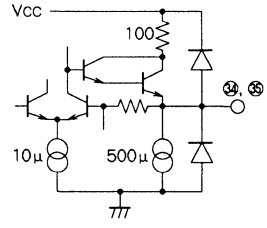
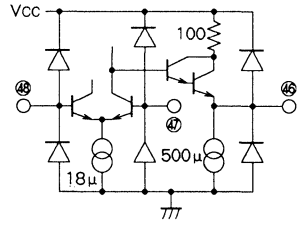
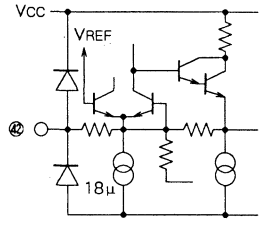
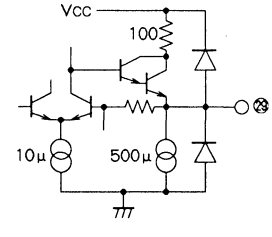
3. NOISE SEQUENCER

Mode \ Pin name (Pin No)	NOISE-CNT-E (Pin ㉓)	NOISE-CNT-A (Pin ㉔)	NOISE-CNT-B (Pin ㉕)
Signal select	H	X	X
Noise L	L	L	L
Noise C	L	L	H
Noise R	L	H	L
Noise S	L	H	H

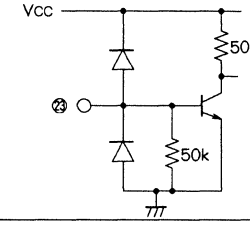
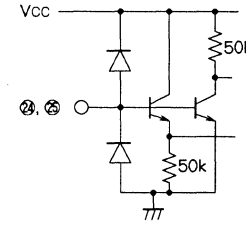
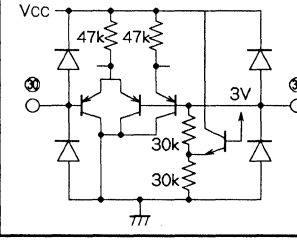
PIN DESCRIPTION

Pin No.	Name	Function	Voltage	Description	Equivalent circuit
⑮	L – AB – IN	Autobalance, L-ch input	4V	Autobalance amplifier input pins Noninverting operational amplifier is applied to these pins. To provide DC bias, pull them up by connecting external resistance (R111, 112 : 22kΩ~75kΩ) to $V_{ref.}$	
㉒	R – AB – IN	Autobalance, R-ch input	4V		
⑯	L – AB – OUT	Autobalance, L-ch output	4V	Autobalance amplifier output pins. They are controlled from adaptive martrix, so that signals are output with the imbalance between right and left corrected. They are normally direct-connected to, respectively, L-IN and R-IN described below.	
㉑	R – AB – OUT	Autobalance, R-ch output	4V		
⑰	L – IN	L-ch input	4V	Adaptive matrix input circuit. Noniverting operational amplifier is applied to the input pins. To provide DC bias, pull them up by connecting external resistance (22kΩ~75kΩ) to V_{REF} if they are not directly connected to the autobalance output pins described above.	
⑳	R – IN	R-ch input	4V		
⑱	L – INBUF – OUT	L-ch input Buffer output	4V		
⑲	R – INBUF – OUT	R-ch input Buffer output	4V		
㉜	L – OUT	L-ch output	4V	These pins output R-/L-channel inputs as they are when the operation mode is 2-channel. If the mode is 3-channel, these pins output Dolby 3 stereo R-/L-channel signals. When the mode is 4-channel, they output Dolby prologic R-/L-channel signals.	
㉝	R – OUT	R-ch output	4V		
㊳	C – OUT	C-ch output	4V	Does not output any signals when the operation mode is 2-channel or when the center mode is OFF or set to PHANTOM.	

PIN DESCRIPTION (continued)

Pin No.	Name	Function	Voltage	Description	Equivalent circuit
㊴	S'– OUT	Sorround channel output	4V	Sorround channel output precedent to delay generator. Always outputs signals, irrespective of the operation mode (2-/3-/4-channel).	
㉞	L + R – OUT	L-channel and R-channel summing output	4V	Pin L + R – OUT outputs the sum of L-channel and R-channel signals that do not go through adaptive matrix. Pin L + R – OUT outputs the difference between them. These pin always output signals, irrespective of the operation mode (2-/3-/4-channel).	
㉟	L – R – OUT	L-channel and R-channel subtraction output	4V		
㊼	LPF – INV – IN	LPF inverted input	4V	Operational amplifier. This amplifier forms a 7kHz low-pass filter (LPS) with external components. Connect the noninverted input pin to VREF to from an LPS in the inverting amplifier style, and input signals by AC coupling (or by DC coupling if surround output is directly connected to LPS without delay generator).	
㊽	LPF – NINV – IN	LPF noninverted input	4V		
㊻	LPF – OUT	LPF output	4V		
㊷	NR – IN	Modified B-type noise reduction input	4V	B-type noise reduction input pin. Connect directly to LPF-OUT in normal cases as shown in the application example. To input signals directly, connect by AC coupling, because noninverting operational amplifier is applied to this pin. Please note that the input/output phase is inverted at 180° in this case.	
㉙	S – OUT	Surround output	4V	This pin outputs surround signals decoded by modified B-type noise reduction. Outputs signals only when the mode is 4-channel. (Outputs 4-V DC in the 2- or 3-channel mode.) There is a gain of approximately 9dB between this output and noise reduction input. When connecting delay genetator behind modified B-type noise reduction, lower the gain by approximately 9dB at the LPF.	

PIN DESCRIPTION (continued)

Pin No.	Name	Function	Voltage	Description	Equivalent circuit
㉓	NOISE – CNT – E	Signal noise selection		This pin controls the switchover between adjusting noise and signal. Control input voltage should be between 0V~8V.	
㉔	NOISE – CNT – A	Noise output destination selection		These pin switches adjusting noise output destination according to 2-bit digital data. Control input voltage should be between 0V~8V.	
㉕	NOISE – CNT – B	Noise output destination selection			
㉚	CENTER – CNT	C-ch channel ON/OFF switching		Controls the center channel (ON/OFF). Control input voltage should be between 0V~8V.	
㉛	MODE – CNT	2-/3-/4-channel switching		Controls the operation mode (2-/3-/4-channel). Control input voltage should be between 0V~8V. Set to open in the 3-channel mode.	

TEST CONDITIONS

1) Mode sequence

Noise	PPVI 5	PPVI 6	PPVI 7
OFF	H	X	X
L	L	L	L
C	L	L	H
R	L	H	L
S'	L	H	H

Channel mode	PPVI 3
2ch	L
3ch	Open
4ch	H

CENTER	PPVI 4	K9
OFF	L	X
ON	H	X
P	H	OFF
W	H	ON

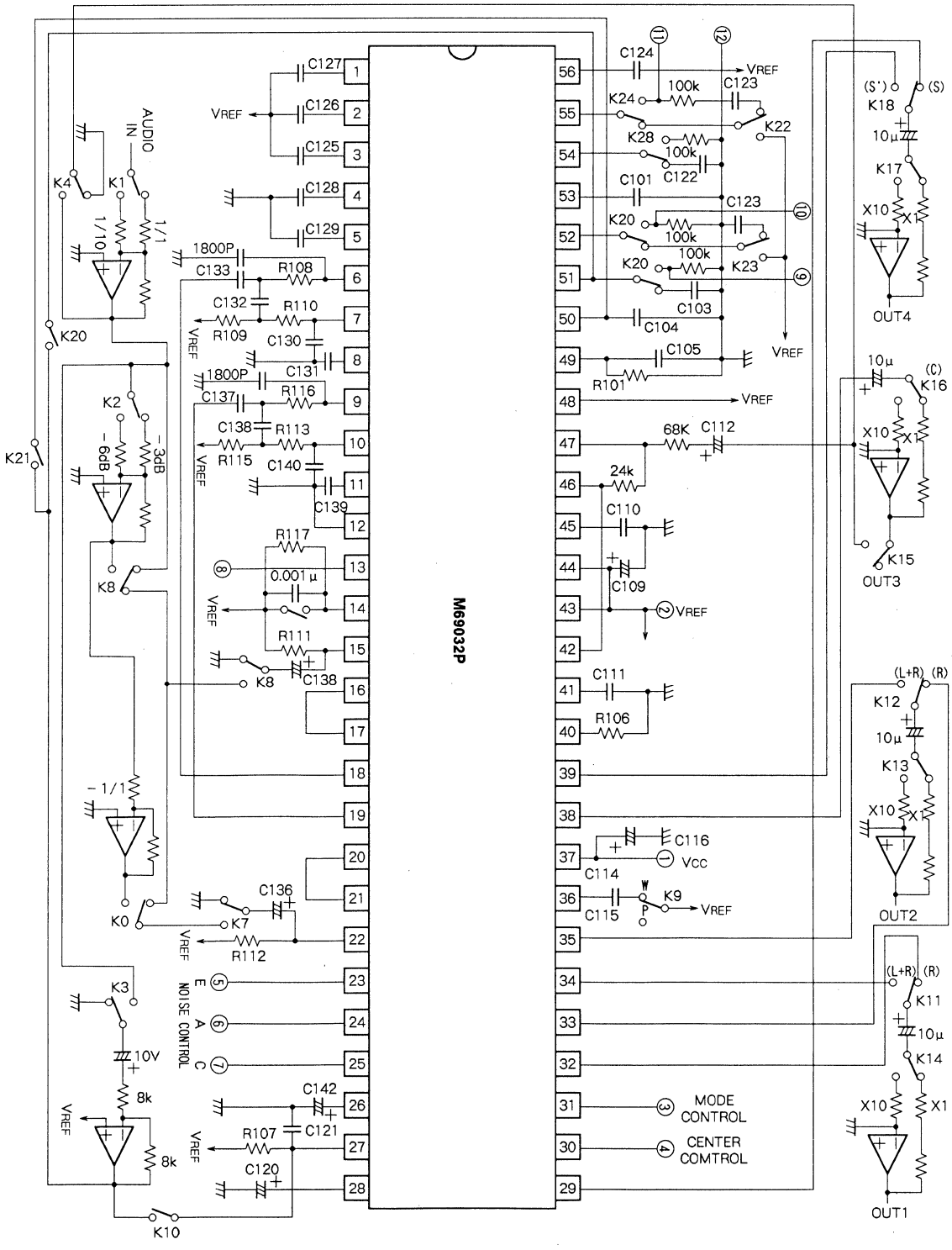
Auto balance	K19
OFF	ON
ON	OFF

Note1. For noise sequencer, set K10 to ON except for V_{NO}(white noise).

2) Input selection switch conditions

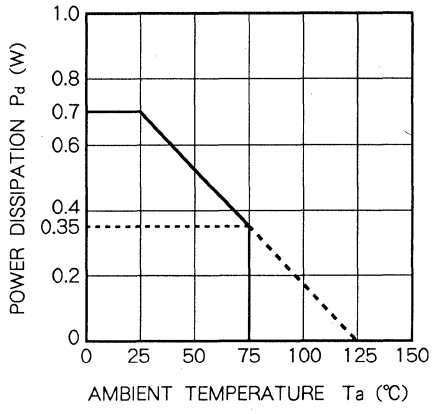
Function	K1	K2	K3	K4	K5	K6	K7	K8	K10	K20	K21
OFF	X	X	X	OFF	X	X	OFF	OFF	OFF	OFF	OFF
ATT 1/1	OFF	X	X	X	X	X	X	X	X	X	X
ATT 1/10	ON	X	X	X	X	X	X	X	X	X	X
L	X	X	X	OFF	OFF	X	OFF	ON	OFF	OFF	OFF
C	X	OFF	X	OFF	ON	OFF	ON	ON	OFF	OFF	OFF
R	X	X	X	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
S'	X	OFF	X	OFF	ON	ON	ON	ON	OFF	OFF	OFF
S : Dolby	X	X	X	ON	X	X	OFF	OFF	OFF	OFF	OFF
LL : Collection level	X	OFF	X	OFF	ON	ON	ON	ON	OFF	OFF	OFF
CP : Capture range	X	ON	X	OFF	ON	ON	ON	ON	OFF	OFF	OFF
CNT1 : Field through	X	X	ON	OFF	X	X	OFF	OFF	OFF	ON	OFF
CNT2 : Field through	X	X	ON	OFF	X	X	OFF	OFF	OFF	OFF	ON

TEST CIRCUIT

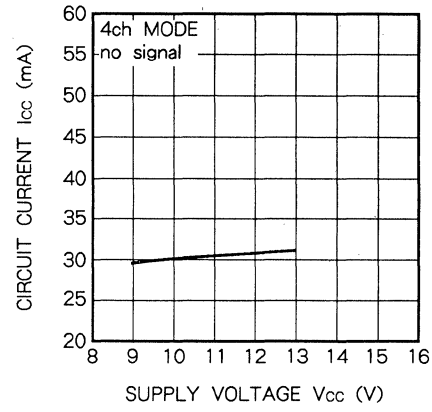


TYPICAL CHARACTERISTICS

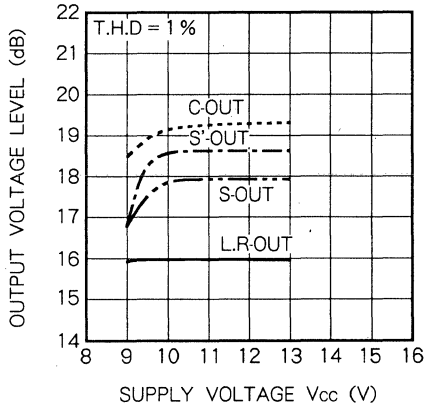
THERMAL DERATING



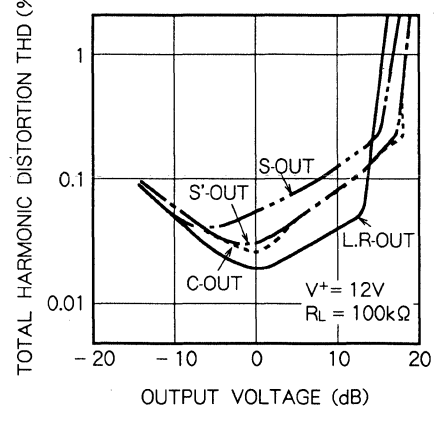
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



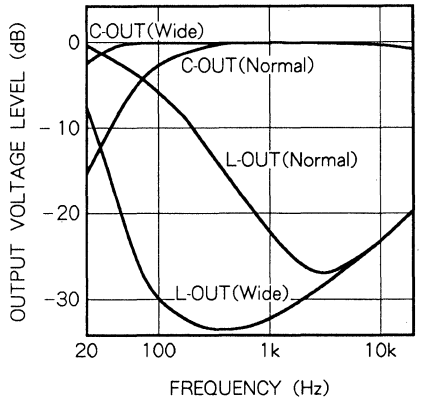
HEAD ROOM CHARACTERISTICS



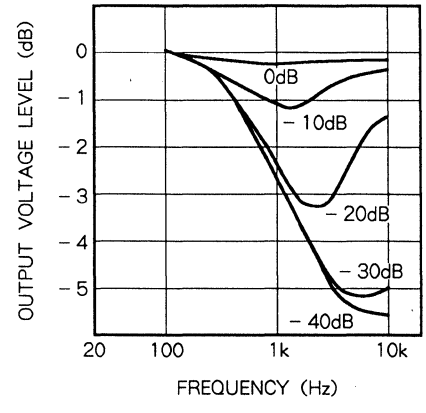
TOTAL HARMONIC DISTORTION VS. SUPPLY VOLTAGE



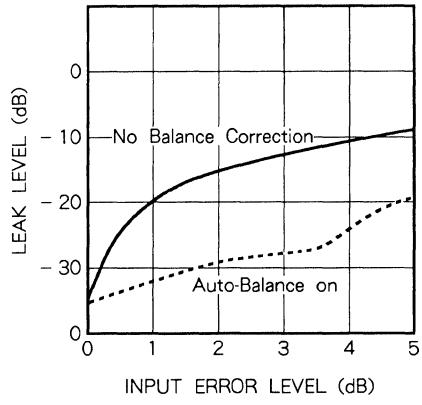
ADAPTIVE MATRIX CHARACTERISTICS (C-IN)



MODIFIED B TYPE NOISE REDUCTION DECODING CHARACTERISTICS



AUTOBALANCE CHARACTERISTICS



OPTIONAL PARTS LIST

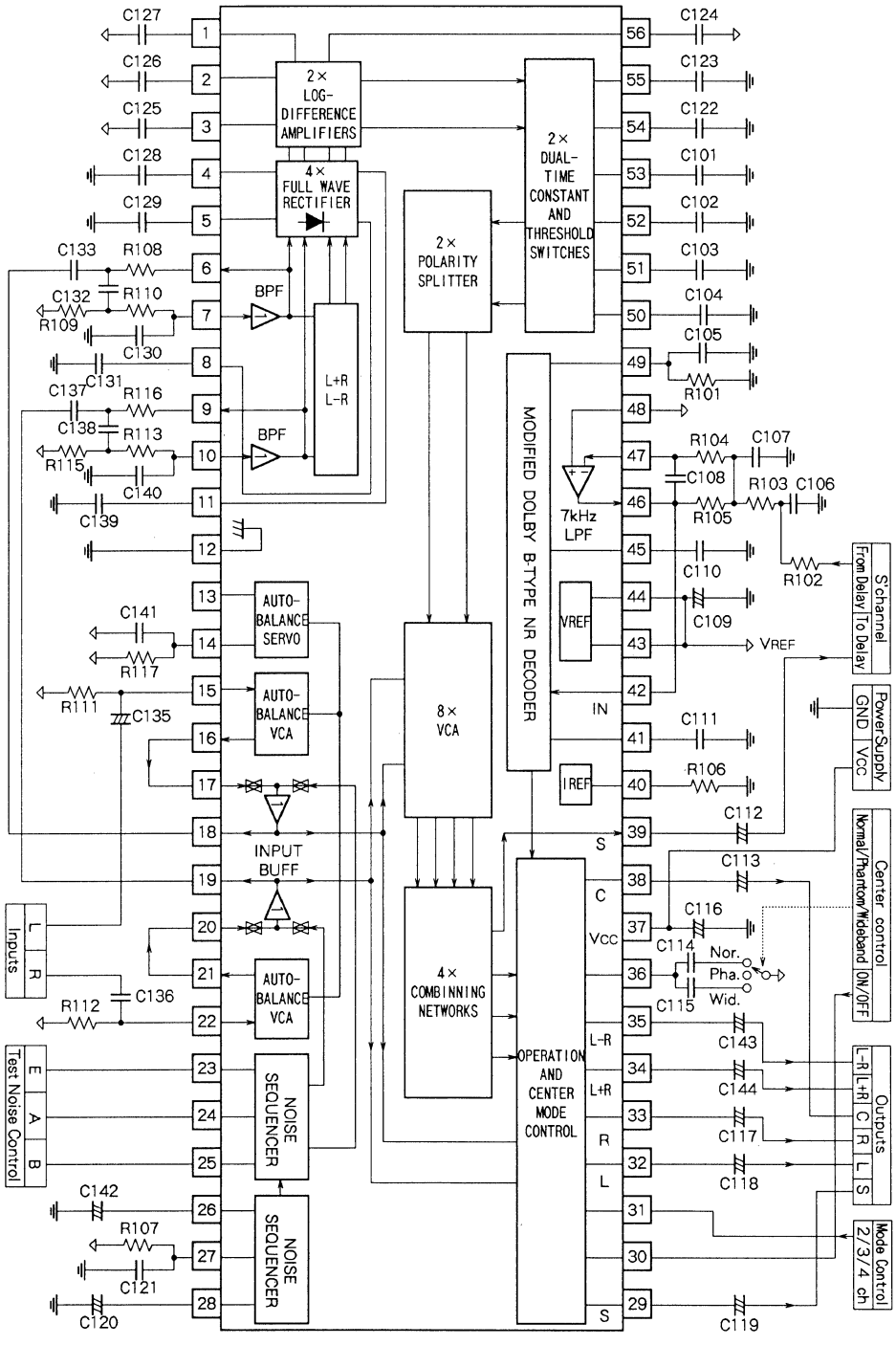
1. M69032P application circuits

PARTS NO.	VALUE	TOL.		PARTS NO.	VALUE	TOL.		PARTS NO.	VALUE	TOL.
C 101	4.7μF	20%		C 123	0.22μF	10%		R 101	330kΩ	10%
C 102	0.22μF	10%		C 124	0.1μF	20%		R 102	8.2kΩ	
C 103	0.22μF	10%		C 125	0.1μF	20%		R 103	8.2kΩ	5%
C 104	0.22μF	10%		C 126	0.1μF	20%		R 104	8.2kΩ	5%
C 105	0.68μF	10%		C 127	0.1μF	20%		R 105	15kΩ	5%
C 106	5600pF	10%		C 128	0.022μF	5%		R 106	100kΩ	1%
C 107	4700pF	10%		C 129	0.022μF	5%		R 107	100kΩ	5%
C 108	470pF	10%		C 130	680pF	5%		R 108	7.5kΩ	5%
C 109	220μF	10%	≧ 150μF	C 131	0.047μF	5%		R 109	15kΩ	5%
C 110	0.047μF	5%		C 132	0.1μF	5%		R 110	47kΩ	5%
C 111	5600pF	5%		C 133	0.1μF	5%		R 111	22kΩ	
C 112	10μF			C 135	10μF			R 112	22kΩ	
C 113	10μF			C 136	10μF			R 113	47kΩ	5%
C 114	0.22μF	10%		C 137	0.1μF	5%		R 115	15kΩ	5%
C 115	10μF	10%		C 138	0.1μF	5%		R 116	7.5kΩ	5%
C 116	100μF		≧ 100μF	C 139	0.047μF	5%		R 117	10MΩ	10%
C 117	10μF			C 140	680pF	5%				
C 118	10μF			C 141	10μF	20%	Low leak			
C 119	10μF			C 142	10μF					
C 120	22μF	10%		C 143	10μF					
C 121	4700pF	5%		C 144	10μF					
C 122	4.7μF	20%								

2. M69032P & M65830P application circuits

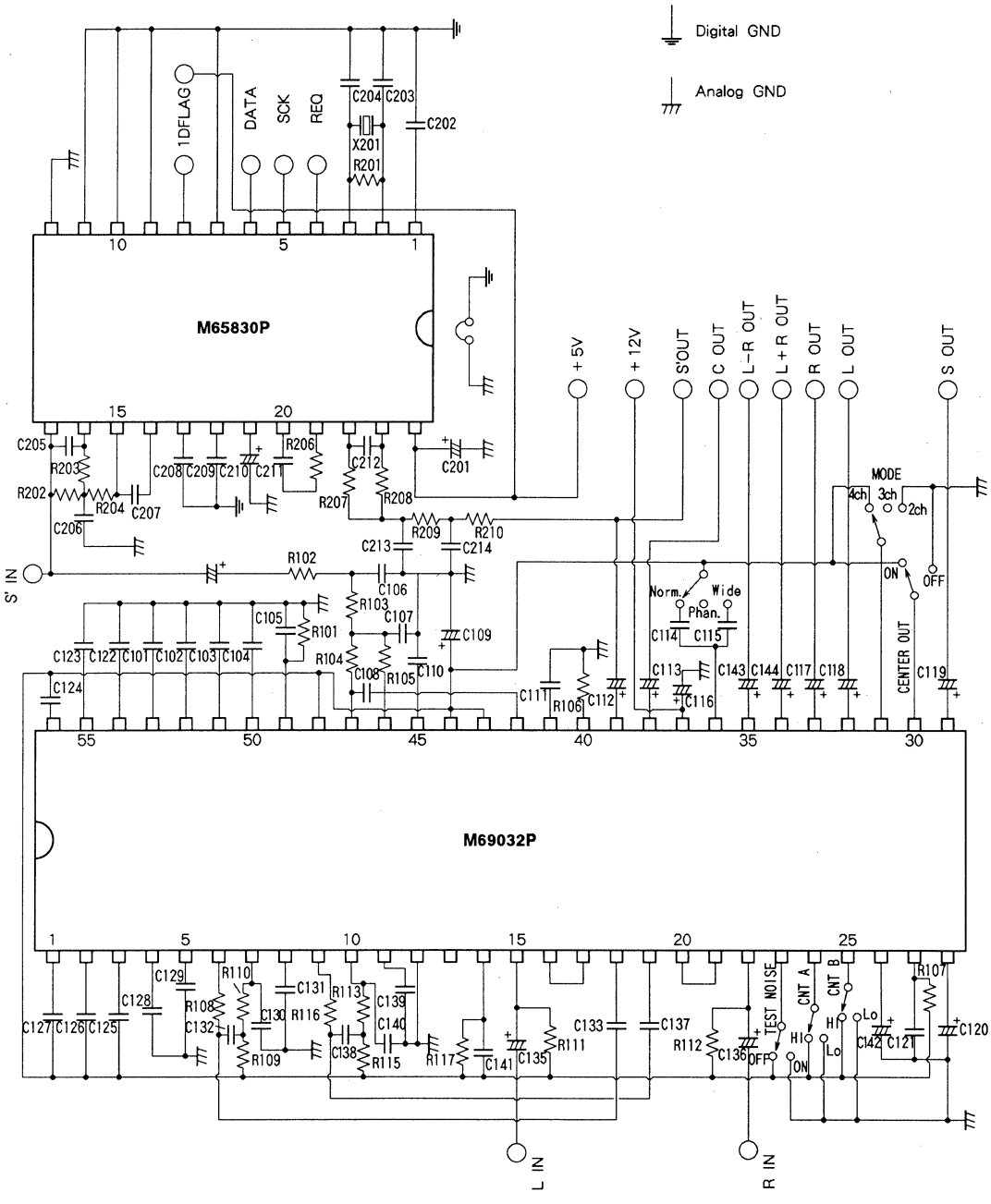
PARTS NO.	VALUE	TOL.		PARTS NO.	VALUE	TOL.		PARTS NO.	VALUE	TOL.
C 101	4.7μF	20%		C 131	0.047μF	5%		R 101	330kΩ	10%
C 102	0.22μF	10%		C 132	0.1μF	5%		R 102	short	
C 103	0.22μF	10%		C 133	0.1μF	5%		R 103	15kΩ	5%
C 104	0.22μF	10%		C 135	10μF			R 104	15kΩ	5%
C 105	0.68μF	10%		C 136	10μF			R 105	15kΩ	5%
C 106	open			C 137	0.1μF	5%		R 106	100kΩ	1%
C 107	2200pF	10%		C 138	0.1μF	5%		R 107	100kΩ	5%
C 108	470pF	10%		C 139	0.047μF	5%		R 108	7.5kΩ	5%
C 109	220μF	10%	≧ 150μF	C 140	680pF	5%		R 109	15kΩ	5%
C 110	0.047μF	5%		C 141	10μF	20%	Low leak	R 110	47kΩ	5%
C 111	5600pF	5%		C 142	10μF			R 111	22kΩ	
C 112	1μF			C 143	10μF			R 112	22kΩ	
C 113	10μF			C 144	10μF			R 113	47kΩ	5%
C 114	0.22μF	10%						R 115	15kΩ	5%
C 115	10μF	10%						R 116	7.5kΩ	5%
C 116	100μF		≧ 100μF	C 201	100μF			R 117	10MΩ	10%
C 117	10μF			C 202	0.1μF			R 201	1MΩ	
C 118	10μF			C 203	100pF			R 202	15kΩ	
C 119	10μF			C 204	100pF			R 203	18kΩ	
C 120	22μF	10%		C 205	470pF			R 204	15kΩ	
C 121	4700pF	5%		C 206	3300pF			R 205	short	
C 122	4.7μF	20%		C 207	0.068μF			R 206	30Ω	
C 123	0.22μF	10%		C 208	0.1μF			R 207	5.6kΩ	
C 124	0.1μF	20%		C 209	0.1μF			R 208	18kΩ	
C 125	0.1μF	20%		C 210	47μF			R 209	7.5kΩ	
C 126	0.1μF	20%		C 211	0.068μF			R 210	8.2kΩ	
C 127	0.1μF	20%		C 212	470pF					
C 128	0.022μF	5%		C 213	5600pF			X 201	2MHz	
C 129	0.022μF	5%		C 214	5600pF					
C 130	680pF	5%		C 215	1μF					

APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

M69032P & M65830P APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

SOUND CONTROLLER (VOLUME, TONE QUALITY CONTROLLER)

4

M51137FP

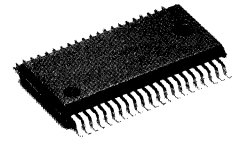
ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR MULTIAMPLIFIER APPLICATIONS

DESCRIPTION

The M51137FP is a Bi-CMOS IC developed for audio-visual systems. It is suitable for multiamplifiers, being used for processing small analog signals in the stage before power amplifier. The IC uses 8-bit serial data transmitted from a microcomputer in order to perform sound control such as master volume control (VCA system), tone control (bass, mid, and treble), and bass boosting. Its applications also include use as a single output and car audio systems.

FEATURES

- Built-in VCA circuit for main volume control
- Variable volume range ····· – 96dB~ + 9dB
- Capability of controlling VCA from external source
- Built-in bass booster enhances heavy bass
- Tone control
  - Treble ····· – 10dB~ + 16dB (2dB/step)
  - Mid ····· – 10dB~ + 10dB (2dB/step)
  - Bass ····· – 10dB~ + 16dB (2dB/step)
  - Bass boost ····· – 10dB~ + 10dB (2dB/step)
- For controlling in each mode, the IC uses built-in microcomputer interface and serial data that regulates volume (8-bit), treble, mid, bass, and bass boost (4-bit)



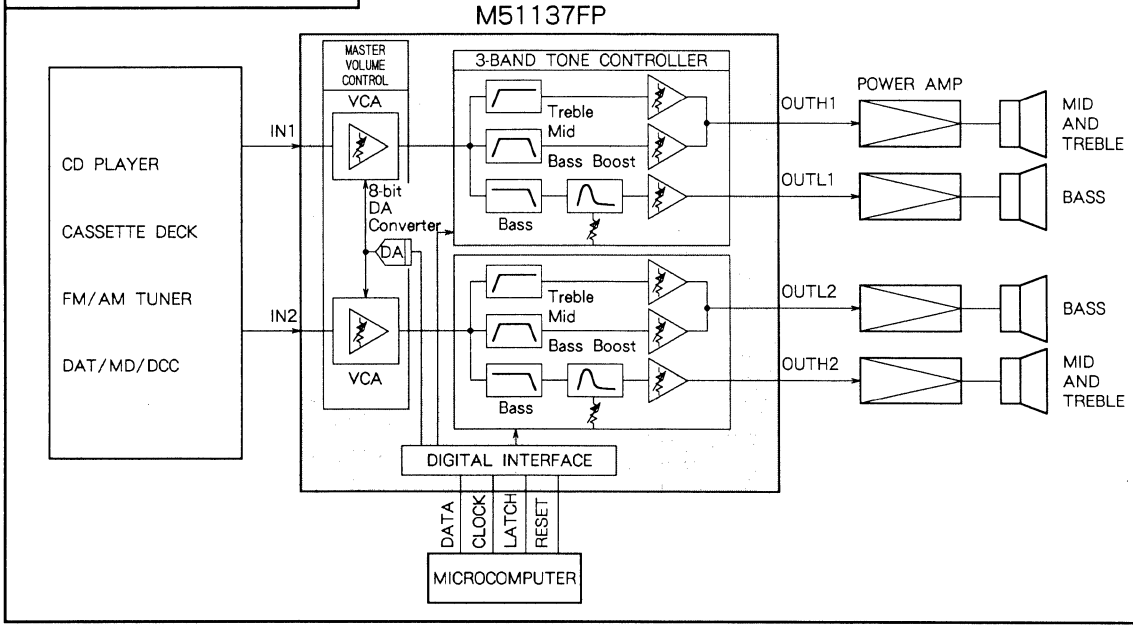
Outline 42P2R-A

0.8mm pitch 450mil SSOP
(8.4mm × 17.5mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· Vcc = 7.5~12V
Rated supply voltage ····· Vcc = 9V

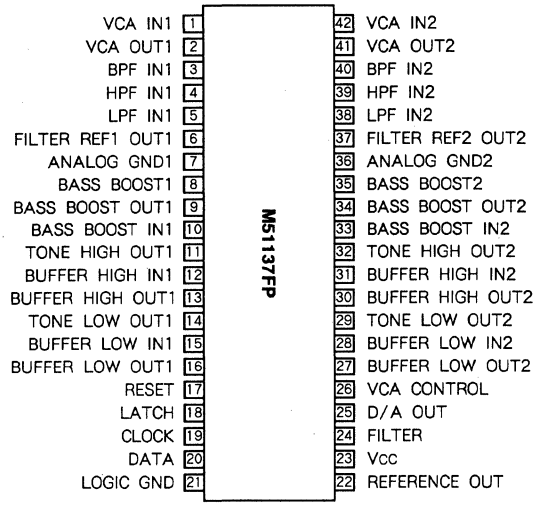
SYSTEM CONFIGURATION



M51137FP

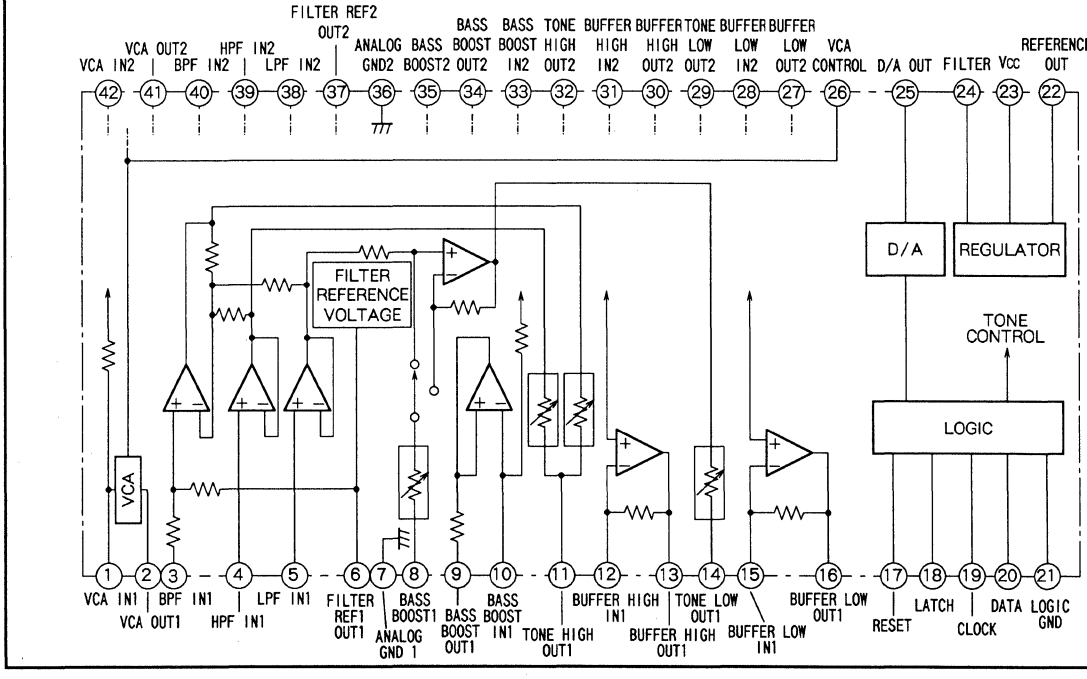
ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR MULTIAMPLIFIER APPLICATIONS

PIN CONFIGURATION



Outline 42P2R-A

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR MULTIAMPLIFIER APPLICATIONS

PIN DESCRIPTION

Pin No.	Name	Function
① (㊷)	VCA IN 1 (2)	Signal input terminal of ch1 (2)
② (㊶)	VCA OUT 1 (2)	Signal output terminal of ch1 (2)
③ (㊵)	BPF IN 1 (2)	BPF input terminal of ch1 (2)
④ (㊴)	HPF IN 1 (2)	HPF input terminal of ch1 (2)
⑤ (㊳)	LPF IN 1 (2)	LPF input terminal of ch1 (2)
⑥ (㊲)	Filter REF 1 (2)	Filter output for analog reference voltage
⑦ (㊱)	Analog GND 1 (2)	Ground of analog circuit
⑧ (㉟)	Bass-boost 1 (2)	Bass-boost gain terminal
⑨ (㉞)	Bass-boost OUT 1 (2)	Bass-boost resonanse Amplifier output
⑩ (㉝)	Bass-boost IN 1 (2)	Bass-boost resonanse Amplifier input
⑪ (㉜)	Tone high OUT 1 (2)	Treble, mid output
⑫ (㉛)	Buffer high IN 1 (2)	Treble, mid buffer input
⑬ (㉚)	Buffer high OUT 1 (2)	Treble, mid buffer output
⑭ (㉙)	Tone low OUT 1 (2)	Bass, bass-boost out
⑮ (㉘)	Buffer low IN 1 (2)	Bass, bass-boost buffer input
⑯ (㉗)	Buffer low OUT 1 (2)	Bass, bass-boost buffer output
⑰	RESET	MUTE. Set Volume minimum and tone control minimum by high level voltage.
⑱	LATCH	Latch signal of serial data from microcomputer to the IC. Operate at rising eges of pulse.
⑲	CLOCK	Clock signal of serial data from microcomputer to the IC. Operate at rising eges of pulse.
⑳	DATA	Serial data input. (LSB first)
㉑	Logic GND	Ground of digital circuit
㉒	REFERENCE OUT	Reference output voltage source. (5.8V typ)
㉓	Vcc	Supply voltage (7.5~12V)
㉔	FILTER	Filter for ripple
㉕	D/A OUT	VCA control voltage source by D/A convertor
㉖	VCA CONTROL	VCA gain control terminal

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	14	V
V_I	Digital input voltage	− 0.3~7.0	V
P_d	Power dissipation	1000 * standard board	mW
K_θ	Thermal derating	10 ($T_a \geqq 25℃$)	mW/℃
T_{opr}	Operating temperature	− 10~+ 70	℃
T_{stg}	Storage temperature	− 40~+ 125	℃

* Standard board
- board size 70mm × 70mm
- board thickness 1.6mm
- board material glass epoxy
- copper pattern
  copper thickness 18μm
  copper size 0.25mm(width) 30mm(length/lead)

ELECTRICAL CHARACTERISTICS

(Ta = 25℃, Vcc = 9V, Control data : FF5550 (volume max/tone flat), f = 1kHz, unless otherwise noted)

Symbol		Parameter	Test conditions: Input condition	Control data	Switch condition: SA	SB1	SB2	SC	Measurement point	Limits: Min	Typ	Max	Unit
Icc	Supply voltage	Circuit current	Quiescent	FF5550	OPEN	OPEN	BPF	a	PIN㉓	26	38	50	mA
VREF		Reference voltage	⇧	⇧	⇧	⇧	⇧	⇧	PIN㉒	5.4	5.8	6.3	V
VFIL		Filter voltage	⇧	⇧	⇧	⇧	⇧	⇧	PIN㉔	8.2	8.9	–	V
IIH	Logic	Level "H" input current	VIH = 4.5V	FF5550	OPEN	OPEN	BPF	b	PIN⑰ PIN⑱ PIN⑲ PIN⑳	0.3	1.0	3.0	μA
IIL		Level "L" input current	VIL = 0.5V	⇧	⇧	⇧	⇧	⇧	⇧	−0.3	0.0	0.3	μA
OFSTM1	Switching offset	Tre/mid switching offset voltage	Quiescent (data switching offset voltage difference)	FFD050 → FF0A50	OPEN	OPEN	BPF	a	PIN⑪ PIN㉜	−20	0	+20	mV
OFSBB1		Boost switching offset voltage 1	⇧	FF5550 → FF5555	⇧	⇧	⇧	⇧	PIN⑧ PIN㉟	−10	0	+10	mV
OFSBB2		Boost switching offset voltage 2	⇧	FF5550 → FF555D	⇧	⇧	⇧	⇧	PIN⑧ PIN㉟	−10	0	+10	mV
CBVT	Channel balance	Total channel balance 1	(Calculation)	–	–	–	–	–	CB + CBT	−3	0	3	dB
CBVM		Total channel balance 2	(Calculation)	–	–	–	–	–	CB + CBM	−3	0	3	dB
CBVB		Total channel balance 3	(Calculation)	–	–	–	–	–	CB + CBBA	−3	0	3	dB
ATT (min)	Electronic volume	Minimum Attenuation level	Vi = −14dBV *1	FF5550	CLOSE	OPEN	BPF	a	A(1), A(2)	7.2	9.0	10.8	dB
CB		Channel balance	⇧	⇧	⇧	⇧	⇧	⇧	A(1)/A(2)	−1.8	0	1.8	dB
THD		Total harmonic distortion	Vi=−14dBV, *1 BPF=400Hz~30kHz	⇧	⇧	⇧	⇧	⇧	A(1), A(2)	–	0.02	0.1	%
No (min)		Noise voltage	Quiescent IHF-A	⇧	OPEN	⇧	⇧	⇧	⇧	–	25.0	56.0	μVrms
THD (max)		Maximum total harmonic distortion	Vi=−3dBV, *1 BPF=400Hz~30kHz	⇧	CLOSE	⇧	⇧	⇧	⇧	–	0.1	1.0	%
ATT (−10)		Attenuation level (−10dB)	Vi = −14dBV *1	9A5550	⇧	⇧	⇧	⇧	⇧	−2.8	−1.0	0.8	dB
ATT (max)		Maximum attenuation level	Vi = −3dBV, *1 IHF-A	005550	⇧	⇧	⇧	⇧	⇧	–	−97	−77	dB
No		Maximum attenuation noise voltage	Quiescent IHF-A	⇧	OPEN	⇧	⇧	⇧	⇧	–	10.0	20.0	μVrms
CT		Cross talk	Vi = −3dBV, *1 IHF-A	FF5550	OPEN/CLOSE CLOSE/OPEN	⇧	⇧	⇧	⇧	–	−90	−70	dB
GVT	TREBLE	Voltage gain	Vi = −5dBV *2	FF5550	OPEN	CLOSE	HPF	a	B(1), B(2)	−19	−17	−15	dB
CBT		Channel balance	⇧	⇧	⇧	⇧	⇧	⇧	B(1)/B(2)	−2	0	+2	dB
THDT		Total harmonic distortion	Vi = −5dBV BPF=400Hz~30kHz	⇧	⇧	⇧	⇧	⇧	B(1), B(2)	–	0.01	0.1	%
NoT		Noise voltage	Quiescent IHF-A	⇧	⇧	OPEN	⇧	⇧	⇧	–	4.0	8.0	μVrms

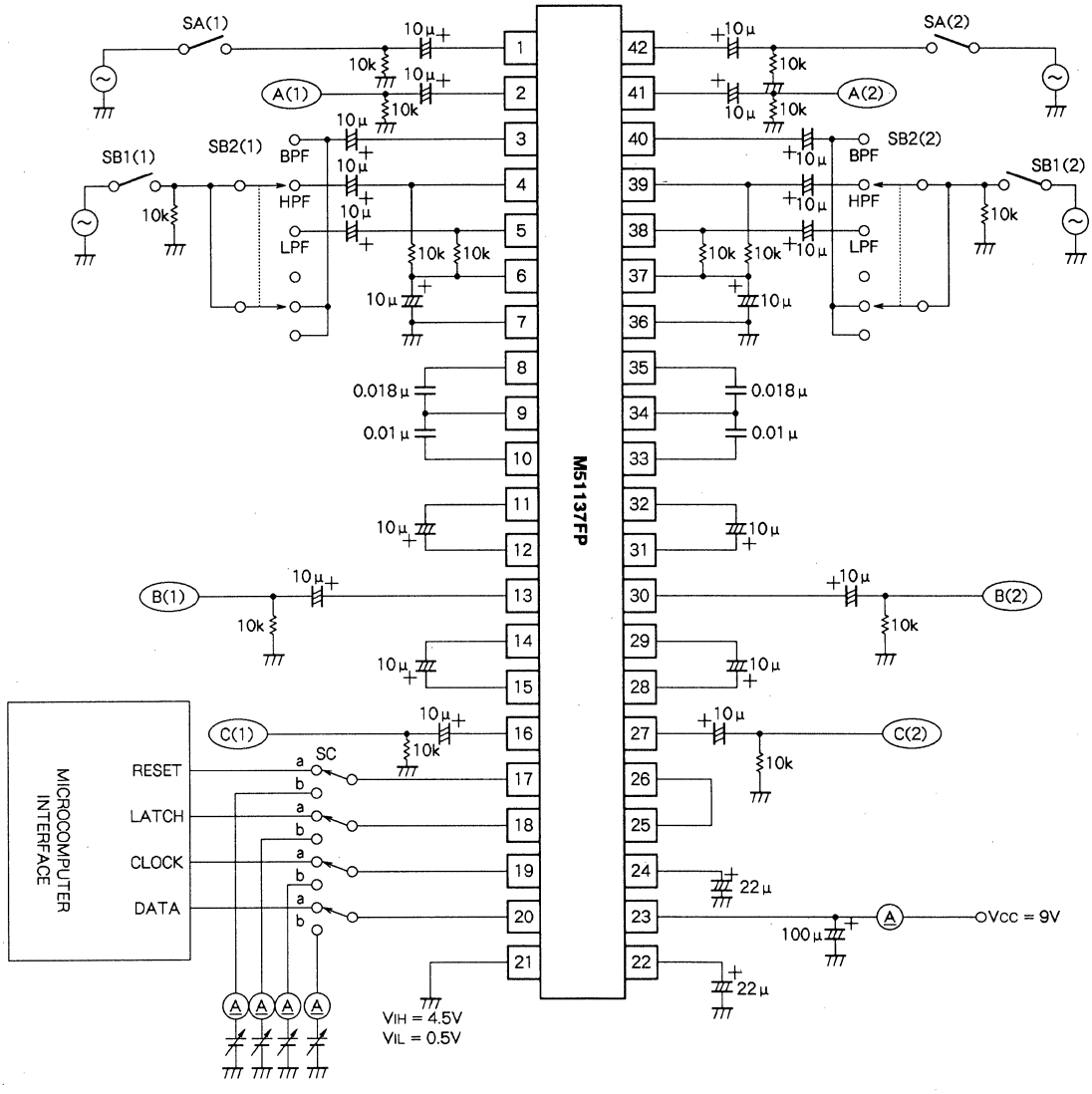
ELECTRICAL CHARACTERISTICS (cont.)

(Ta = 25℃, Vcc = 9V, Control data : FF5550 (volume max/tone flat), f = 1kHz, unless otherwise noted)

Symbol		Parameter	Test conditions: Input condition	Control data	Switch condition: SA	SB1	SB2	SC	Measurement point	Limits: Min	Typ	Max	Unit
THDT max	TREBLE	Maximum total harmonic distortion	Vi=+6dBV, *2 BPF=400Hz～30kHz	FFD550	OPEN	CLOSE	HPF	a	B(1), B(2)	–	0.1	1.0	%
GVT (max)	TREBLE	Maximum voltage gain	Vi = – 5dBV *2	⇧	⇧	⇧	⇧	⇧	⇧	– 3	– 1	+ 1	dB
GVT (min)	TREBLE	Minimum voltage gain	⇧	FF0550	⇧	⇧	⇧	⇧	⇧	– 29	– 27	– 25	dB
CTT	TREBLE	Cross talk	Vi = + 6dBV *2 IHF-A	FFD550	⇧	OPEN/ CLOSE CLOSE/ OPEN	⇧	⇧	⇧	–	– 80	– 60	dB
GVM	MID	Voltage gain	Vi = – 5dBV *3	FF5550	OPEN	CLOSE	BPF	a	B(1), B(2)	– 19	– 17	– 15	dB
CBM	MID	Channel balance	⇧	⇧	⇧	⇧	⇧	⇧	B(1)/ B(2)	– 2	0	+ 2	dB
THDM	MID	Total harmonic distortion	Vi = – 5dBV BPF=400Hz～30kHz	⇧	⇧	⇧	⇧	⇧	B(1), B(2)	–	0.01	0.1	%
NoM	MID	Noise voltage	Quiescent IHF-A	⇧	⇧	OPEN	⇧	⇧	⇧	–	4.0	8.0	μVrms
THDM max	MID	Maximum total harmonic distortion	Vi=+6dBV, *3 BPF=400Hz～30kHz	FF5A50	⇧	CLOSE	⇧	⇧	⇧	–	0.1	1.0	%
GVM (max)	MID	Maximum voltage gain	Vi = – 5dBV *3	⇧	⇧	⇧	⇧	⇧	⇧	– 9	– 7	– 5	dB
GVM (min)	MID	Minimum voltage gain	⇧	FF5050	⇧	⇧	⇧	⇧	⇧	– 29	– 27	– 25	dB
CTM	MID	Cross talk	Vi = + 6dBV, *3 IHF-A	FF5A50	⇧	OPEN/ CLOSE CLOSE/ OPEN	⇧	⇧	⇧	–	– 80	– 60	dB
GVBA	Bass	Voltage gain	Vi = – 5dBV *4	FF5550	OPEN	CLOSE	LPF	a	C(1), C(2)	– 19	– 17	– 15	dB
CBBA	Bass	Channel balance	⇧	⇧	⇧	⇧	⇧	⇧	C(1)/ C(2)	– 2	0	+ 2	dB
THDBA	Bass	Total harmonic distortion	Vi = – 5dBV BPF=400Hz～30kHz	⇧	⇧	⇧	⇧	⇧	C(1), C(2)	–	0.01	0.1	%
NoBA	Bass	Noise voltage	Quiescent IHF-A	⇧	⇧	OPEN	⇧	⇧	⇧	–	4.0	8.0	μVrms
THDBA max	Bass	Maximum total harmonic distortion	Vi=+6dBV, *4 BPF=400Hz～30kHz	FF55D0	⇧	CLOSE	⇧	⇧	⇧	–	0.1	1.0	%
GVBA (max)	Bass	Maximum voltage gain	Vi = – 5dBV *4	⇧	⇧	⇧	⇧	⇧	⇧	– 3	– 1	+ 1	dB
GVBA (min)	Bass	Minimum voltage gain	⇧	FF5500	⇧	⇧	⇧	⇧	⇧	– 29	– 27	– 25	dB
CTBA	Bass	Cross talk	Vi = + 6dBV *4 IHF-A	FF55D0	⇧	OPEN/ CLOSE CLOSE/ OPEN	⇧	⇧	⇧	–	– 80	– 60	dB
THDBB max	Bass	Boost maximum total harmonic distortion	Vi=–10dBV, *4 BPF=400Hz～30kHz	FF55D5	⇧	CLOSE	⇧	⇧	⇧	–	0.1	1.0	dB
GVBB (max)	Bass	Boost maximum voltage gain	Vi = – 10dBV *4 f = 800Hz	FF5555	⇧	⇧	⇧	⇧	⇧	10	– 7	– 5	dB
GVBB (min)	Bass	Boost minimum voltage gain	⇧	FF555D	⇧	⇧	⇧	⇧	⇧	– 29	– 27	– 24	dB

Note : *1 ; Vi is VCA input voltage. *2 ; Vi is HPF input voltage. *3 ; Vi is BPF input voltage. *4 ; Vi is LPF input voltage.

TEST CIRCUIT



Units Resistance : Ω
Capacitance : F

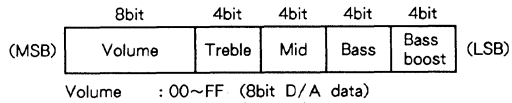
ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR MULTIAMPLIFIER APPLICATIONS

OPERATIONAL DESCRIPTION

1. CONTROL METHOD

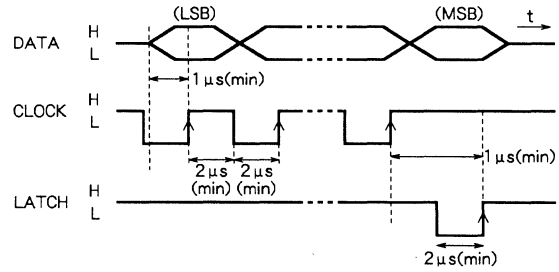
(1) DIGITAL CONTROL SPECIFICATION

Data format



Volume : 00~FF (8bit D/A data)
Treble : 0~D (14 step)
Mid : 0~A (11 step)
Bass : 0~D (14 step)
Bass-boost : 0 (11 step)
1~5
9~D

TIMING DIAGRAM (RECOMMENDED CONDITION)



Note 1. RESET (MUTE) is volume minimum and tone control minimum by "H" level.
Puls width 2µs(min)
2. CLOCK, LATCH functions operates at rising ege of pulse.
3. Recommended input level
"H" level : more than 4V
"L" level : less than 1V
the, threshold voltage (Logic input buffer) is about 2.5V.

CONTROL DATA TABLE

D/A converter for VCA		TREBLE		MID		BASS		BASS-BOOST	
DATA	OUTPUT VOLTAGE	DATA	GAIN	DATA	GAIN	DATA	GAIN	DATA	GAIN
00	V_Z	0	− 10dB	0	− 10dB	0	− 10dB	0	± 0dB
01	$\frac{255V_Z + V_F}{256}$	1	− 8dB	1	− 8dB	1	− 8dB	1	+ 2dB
		2	− 6dB	2	− 6dB	2	− 6dB	2	+ 4dB
		3	− 4dB	3	− 4dB	3	− 4dB	3	+ 6dB
		4	− 2dB	4	− 2dB	4	− 2dB	4	+ 8dB
		5	± 0dB	5	± 0dB	5	± 0dB	5	+ 10dB
		6	+ 2dB	6	+ 2dB	6	+ 2dB	6	−
		7	+ 4dB	7	+ 4dB	7	+ 4dB	7	−
		8	+ 6dB	8	+ 6dB	8	+ 6dB	8	−
		9	+ 8dB	9	+ 8dB	9	+ 8dB	9	− 2dB
		A	+ 10dB	A	+ 10dB	A	+ 10dB	A	− 4dB
		B	+ 12dB	B	−	B	+ 12dB	B	− 6dB
		C	+ 14dB	C	−	C	+ 14dB	C	− 8dB
		D	+ 16dB	D	−	D	+ 16dB	D	− 10dB
FE	$\frac{2V_Z + 254V_F}{256}$	E	−	E	−	E	−	E	−
FF	$\frac{V_Z + 255V_F}{256}$	F	−	F	−	F	−	F	−

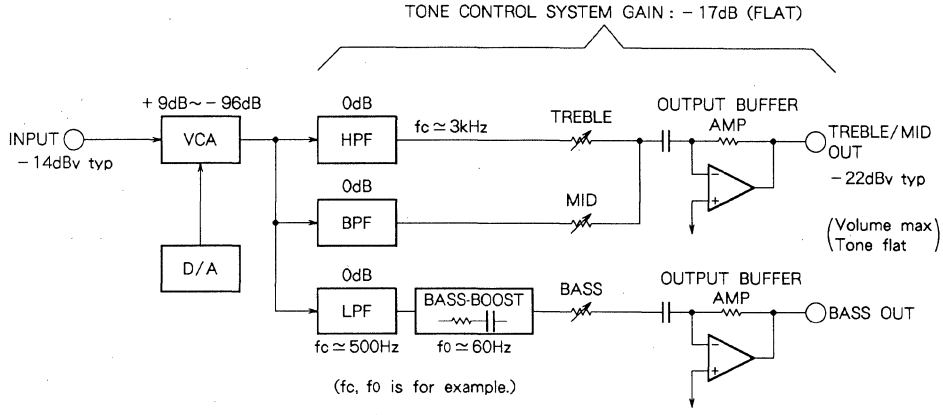
Note typical or designed value. V_Z, V_F is internal power supply voltage.
+ 12dB~+ 16dB of treble and bass are for loudness.

VCA GAIN LEVEL (EXAMPLE)

Control data (D/A converter)	VCA gain level (dB)
0F	(Maximum attenuation)
1F	− 79
2F	− 59
3F	− 44
4F	− 32
5F	− 23
6F	− 15
7F	− 9
8F	− 4
9F	0
AF	+ 3
BF	+ 5
CF	+ 6
DF	+ 7
EF	+ 8
FF	+ 9

(2) SIGNAL PROCESSING SYSTEM

[System] {Total gain : − 8dB (VCA MAX)}

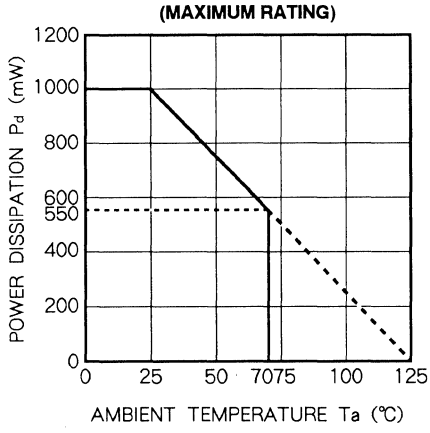


Voltage gain (designed value. Tone control system gain : − 17dB (flat))

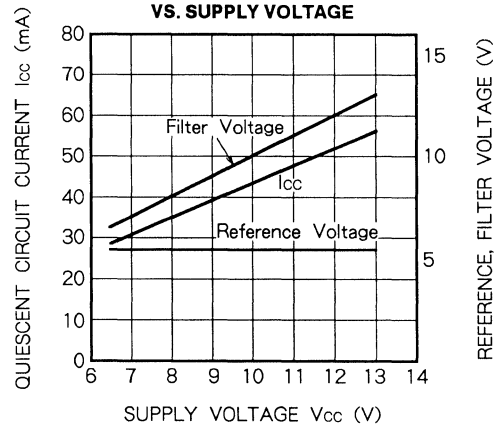
Volume (VCA) : + 9dB ~ − 96dB typ.
Treble : − 10dB ~ 0dB ~ + 10dB (2dB/step)
(+ 12dB, + 14dB, + 16dB for loudness)
Mid : − 10dB ~ 0dB ~ + 10dB (2dB/step)
Bass : − 10dB ~ 0dB ~ + 10dB (2dB/step)
(+ 12dB, + 14dB, + 16dB for loudness)
Bass-boost : − 10dB ~ 0dB ~ + 10dB (2dB/step)

TYPICAL CHARACTERISTICS

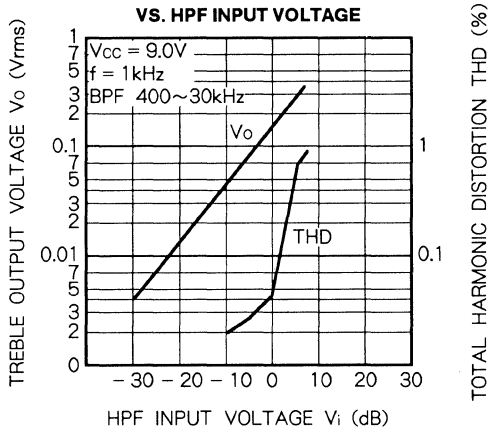
THERMAL DERATING
(MAXIMUM RATING)



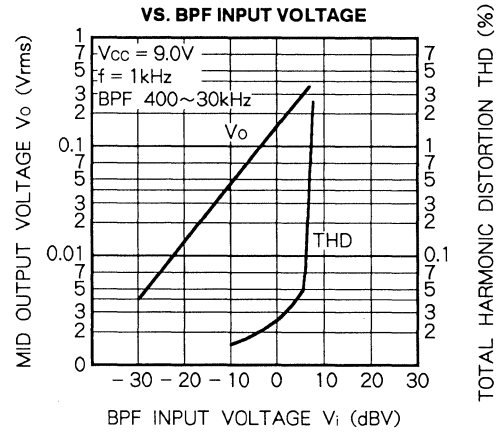
CIRCUIT CURRENT
REFERENCE, FILTER VOLTAGE
VS. SUPPLY VOLTAGE



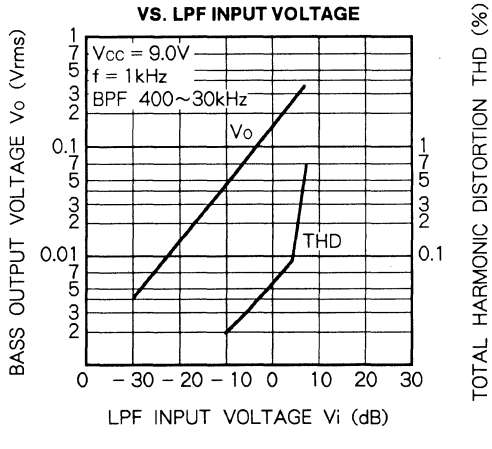
TOTAL HARMONIC DISTORTION
TREBLE OUTPUT VOLTAGE
VS. HPF INPUT VOLTAGE



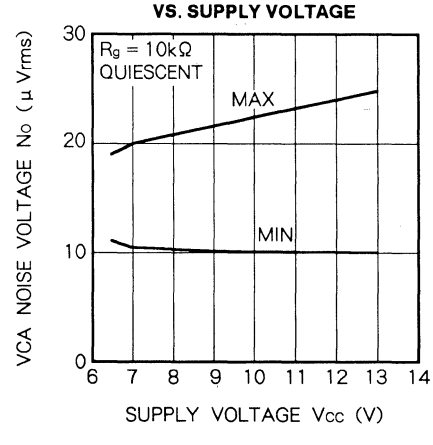
TOTAL HARMONIC DISTORTION
MID OUTPUT VOLTAGE
VS. BPF INPUT VOLTAGE



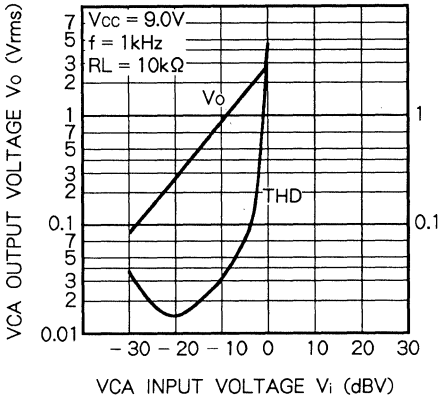
TOTAL HARMONIC DISTORTION
BASS OUTPUT VOLTAGE
VS. LPF INPUT VOLTAGE



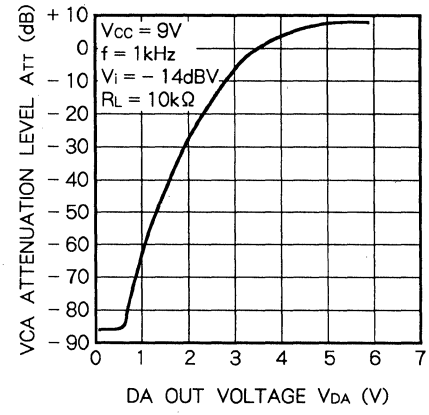
VCA NOISE VOLTAGE
VS. SUPPLY VOLTAGE



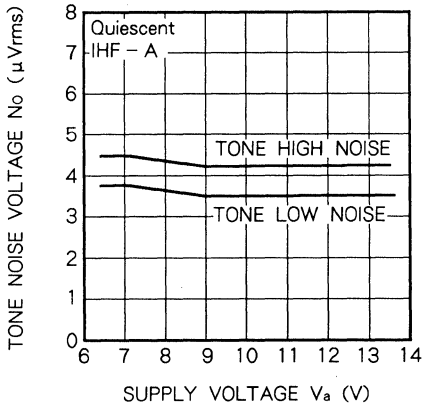
TOTAL HARMONIC DISTORTION VCA OUTPUT VOLTAGE VS. VCA INPUT VOLTAGE



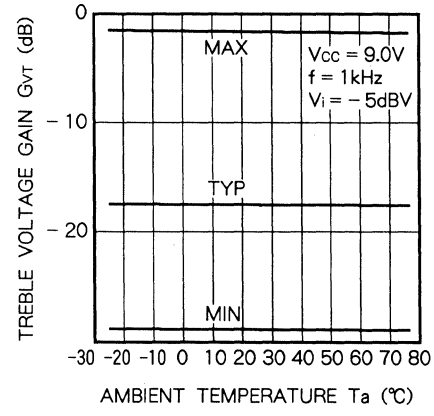
ATTENUATION LEVEL VS. DA OUT VOLTAGE



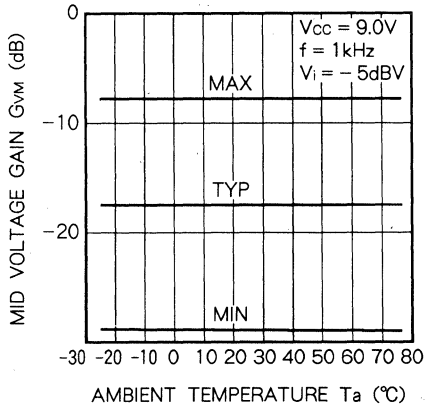
TONE NOISE VOLTAGE VS. SUPPLY VOLTAGE



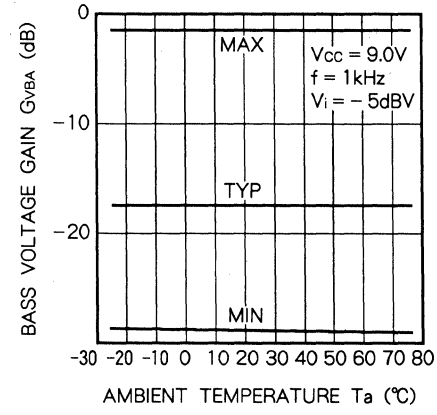
TREBLE VOLTAGE GAIN VS. TEMPERATURE



MID VOLTAGE GAIN VS. TEMPERATURE



BASS VOLTAGE GAIN VS. TEMPERATURE



ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR MULTIAMPLIFIER APPLICATIONS

APPLICATION NOTES

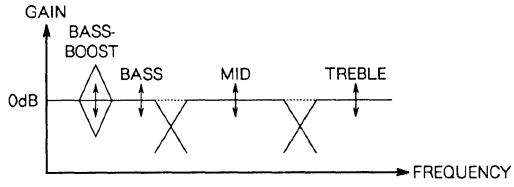
(1) Take care of the heat radiation of PCB.

(2) Take care of a PCB design about digital noise.

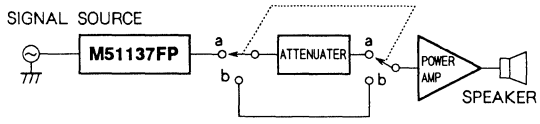
(3) The IC has three GND pins.

(4) Take care of electrostatic damage of ⑥pin and ㊲pin.

(5) Take care of gain characteristics of tone control. The loose attenuation characterestics of filters will disturb the frequency respose in another filtering region.

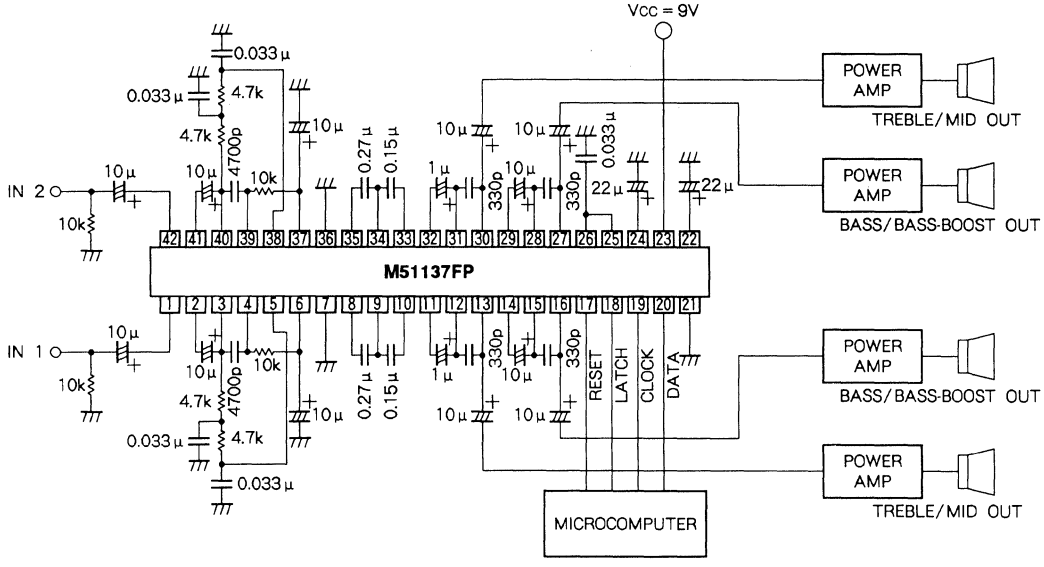


(6) NOISE IMPROVEMENT METHOD



The additional attenuater improves the noise characteristics for small signals.
Volume : Small·····a
Volume : Large·····b

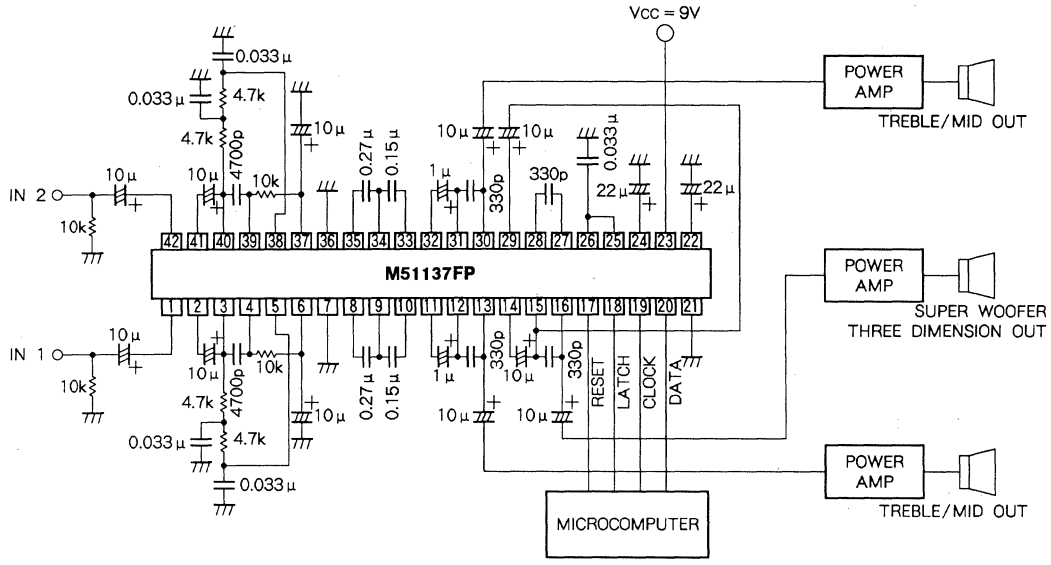
APPLICATION EXAMPLE 1 (Bi-amplifier system)



Units Resistance : Ω
Capacitance : F

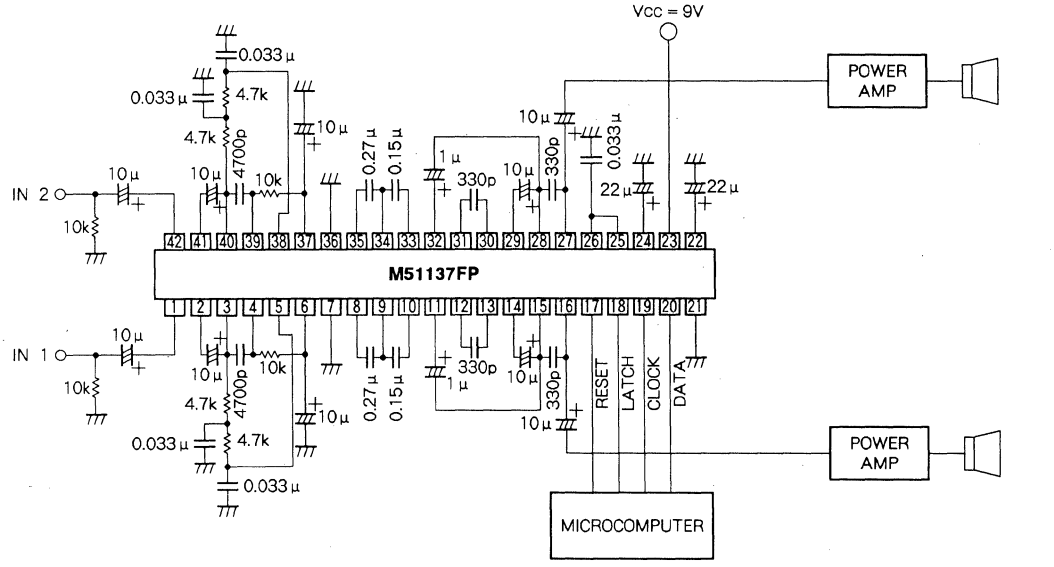
ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR MULTIAMPLIFIER APPLICATIONS

APPLICATION EXAMPLE 2 (Three dimensional type)



Units Resistance : Ω
Capacitance : F

APPLICATION EXAMPLE 3 (Standard type)



Units Resistance : Ω
Capacitance : F

M51139FP

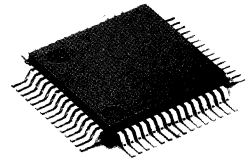
4 SPEAKER SOUND CONTROLLER

DESCRIPTION

The M51139FP is an IC developed for car audio and incorporating master volume, 3-band tone control, fader volume and loud-ness circuit. These blocks are all controlled via serial data. This IC is applicable to home audio and TV, as well as to car audio.

FEATURES

- The front row of power amplifier controls sound volume (master & fader volumes) and sound quality (bass/mid/treble, loudness controls)
- Equipped to process analog sound signals
- Greatly reduces the chirring noise by integrating resistor ladder, CMOS switch, and PMOS input operating amplifier into one chip
- Sound volume and quality are controlled via serial data
- Built-in zero cross detector prevents noise from being generated in sound volume/quality switching
- Output noise voltage····· 4 μVrms(B.W. = 20Hz~20kHz)
- Total harmonics distortion rate····· 0.005 %
- Built-in analog signal reference voltage source (1/2Vcc)



Outline 60P6-B

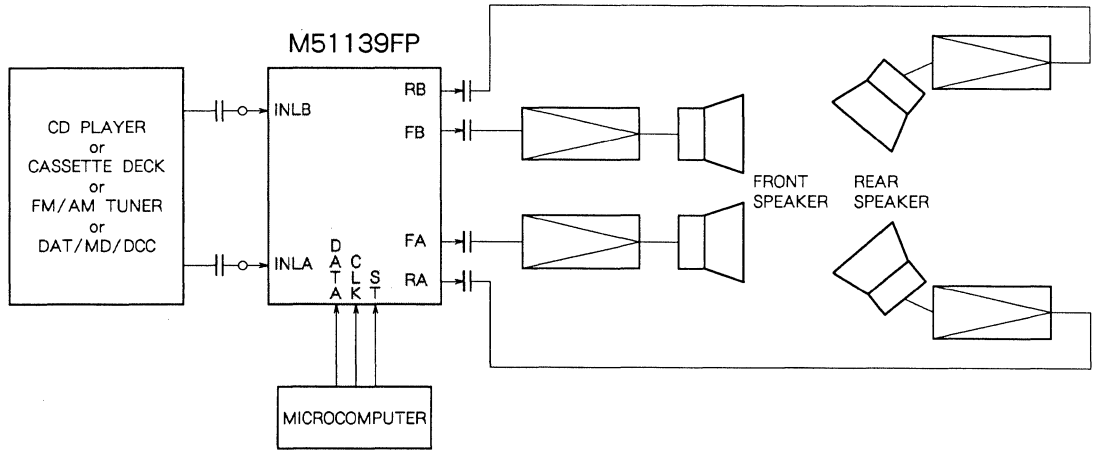
0.8mm pitch QFP
(13.2mm × 13.2mm × 2.0mm)

RECOMMENDED OPERATING CONCITIONS

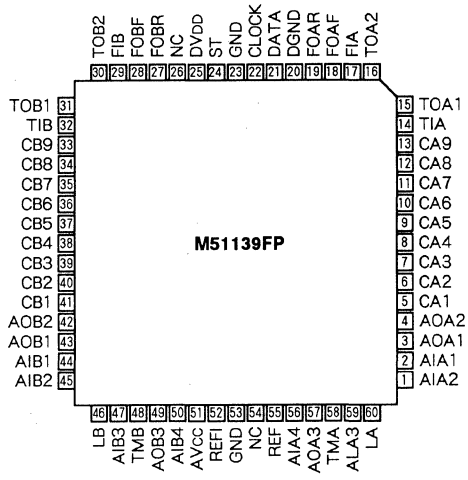
Supply voltage range····· Vcc = 4.5~9V

Rated supply voltage····· Vcc = 8V

SYSTEM CONFIGURATION



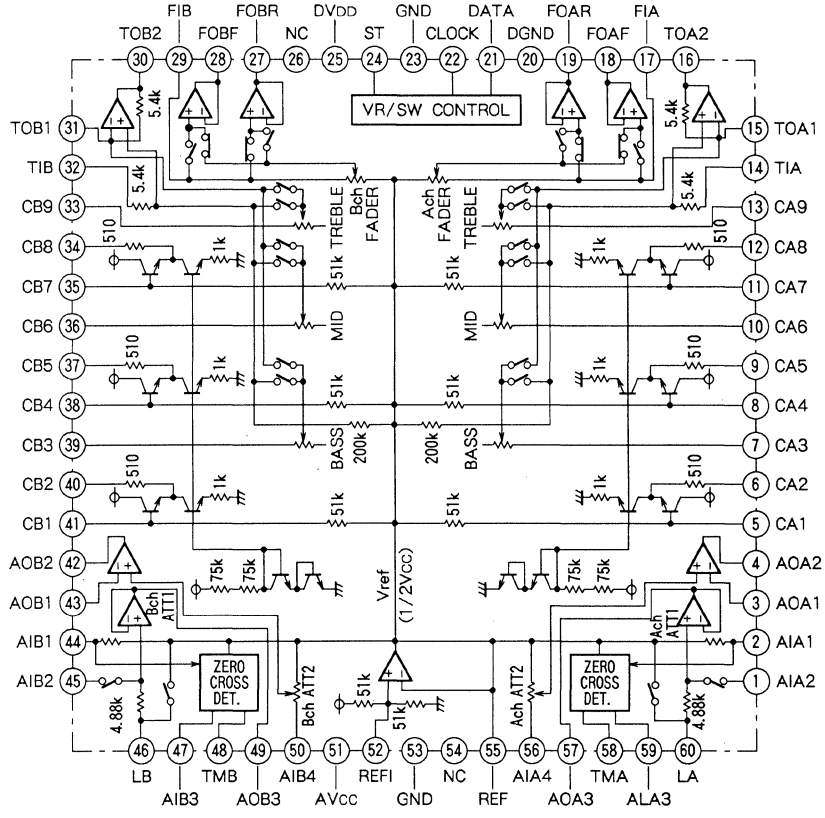
PIN CONFIGURATION



Outline 60P6-B

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin No.	Symbol	Function
①	AIA2	Band-pass filter connection terminal
㊺	AIB2	
㊻	LB	
㊿	LA	
②	AIA1	ATT_1 input terminal
㊹	AIB1	
㊾	AOB3	ATT_1 output terminal
㊼	AOA3	
㊼	AIB3	Zero cross detector input terminal
㊾	AIA3	
㊿	AIB4	ATT_2 input terminal
㊽	AIA4	
③	AOA1	ATT_2 amplifier (−) input terminal
㊸	AOB1	
④	AOA2	ATT_2 output terminal
㊷	AOB2	
⑤~⑬	CA1~CA9	Resonance impedance connection terminal
㉝~㊶	CB9~CB1	
⑭	TIA	Equalizer input terminal
㉜	TIB	
⑮	TOA1	Equalizer amplifier (−) input terminal
㉛	TOB1	
⑯	TOA2	Equalizer amplifier output terminal
㉚	TOB2	
⑰	FIA	Balance amplifier input terminal
㉙	FIB	
⑱	FOAF	Balance amplifier output terminal
⑲	FOAR	
㉗	FOBR	
㉘	FOBF	
⑳	DGND	Logic GND terminal
㉑	DATA	Input terminal for 36-bit serial data
㉒	CLOCK	Shift clock input terminal. Input signal from DATA terminal is inputted into 36-bit shift register at rising edge of shift clock
㉓,㊹	GND	Analog GND terminal
㉔	ST	Strobe signal input terminal. Data inputted in 36-bit shift register is loaded at rising edge of strobe signal
㉕	DVDD	Logic supply terminal
㉖,㊹	N.C.	Non-connection terminal
㊽	TMB	Timer setting terminal
㊽	TMA	
㊶	AVCC	Analog supply terminal
㊷	REFI	Reference amplifier input terminal
㊺	REF	Reference amplifier output terminal

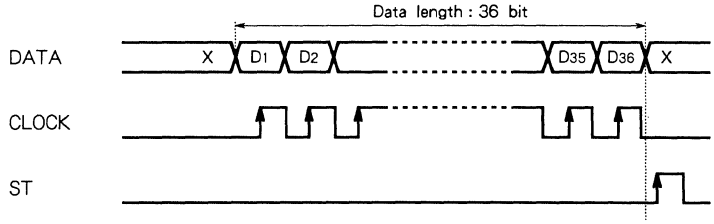
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Power supply voltage	12	V
P_d	Internal power dissipation	850	mW
K_θ	Thermal derating (Ta ≧ 25℃)	8.5	mW/℃
T_{opr}	Operating temperature	− 20 ~ + 75	℃
T_{stg}	Storage temperature	− 40 ~ + 125	℃

ELECTRICAL CHARACTERISTICS (V_{CC} = 8V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
I_{CC}	Operating power supply current	I_{CCA} + I_{CCD}		−	15	30	mA
THD	Total harmonic distortion rate	f = 1kHz, V_{in} = 1Vrms, 0dB		−	0.005	0.02	%
No1	Output noise voltage 1	ATT = − ∞, 20~20kHz		−	4	10	μVrms
No2	Output noise voltage 2	ATT = 0dB, 20~20kHz		−	7	20	μVrms
No3	Output noise voltage 3	at DATA IN, 20~20kHz		−	15	40	μVrms
$V_{O(max)}$	Maximum output voltage	THD = 1 %		1.0	1.8	−	Vrms
CS	Channel separation	f = 1kHz, V_{in} = 1Vrms		80	90	−	dB
$A_{TT(max)}$	Maximum attenuation	ATT = − ∞		85	90	−	dB
V_{IH}	Input voltage	DATA, CLOCK, ST pin	H	2	−	V_{DD}	V
V_{IL}			L	0	−	0.8	V
f_{ck}	Maximum clock frequency	CLOCK pin		−	−	1.5	MHz
G_V	Voltage gain	V_{in} = 1Vrms		−2.8	−0.3	+2.2	dB
G_{BAL}	Balance attenuation	V_{in} = 1Vrms		70	80	−	dB
G_{FD}	Fader attenuation	V_{in} = 1Vrms		70	80	−	dB
G_{BB}	Bass boost	f = 100Hz		+9	+12	+15	dB
G_{BC}	Bass cut	f = 100Hz		−15	−12	−9	dB
G_{MB}	Mid boost	f = 1kHz		+9	+12	+15	dB
G_{MC}	Mid cut	f = 1kHz		−15	−12	−9	dB
G_{TB}	Treble boost	f = 10kHz		+9	+12	+15	dB
G_{TC}	Treble cut	f = 10kHz		−15	−12	−9	dB
G_{LB}	Loudness characteristics	f = 100Hz, ATT = −30dB		+6.5	+9	+11.5	dB
G_{LT}		f = 10kHz, ATT = −30dB		+4	+6	+8	dB

DATA FORMAT



D1~D14 : Main volume setting bit
D15~D18 : Tone (bass) setting bit
D19~D22 : Tone (mid) setting bit
D23~D26 : Tone (treble) setting bit
D27~D30 : Fader volume (balance between front and rear outputs) setting bit
D31 : Bit to choose between front and rear outputs of fader to be controlled
D32 : Bit to switch Loudness ON/OFF
D33~D36 : Address bit

ATTENUATOR 1

ATT_{1B}	D_1	D_2	D_3	D_4	D_5
ATT_{1A}	D_8	D_9	D_{10}	D_{11}	D_{12}
0dB	L	L	L	L	L
− 2dB	H	L	L	L	L
− 4dB	L	H	L	L	L
− 6dB	H	H	L	L	L
− 8dB	L	L	H	L	L
− 10dB	H	L	H	L	L
− 12dB	L	H	H	L	L
− 14dB	H	H	H	L	L
− 16dB	L	L	L	H	L
− 18dB	H	L	L	H	L
− 20dB	L	H	L	H	L
− 22dB	H	H	L	H	L
− 24dB	L	L	H	H	L
− 26dB	H	L	H	H	L
− 28dB	L	H	H	H	L
− 30dB	H	H	H	H	L
− 32dB	L	L	L	L	H
− 34dB	H	L	L	L	H
− 36dB	L	H	L	L	H
− 38dB	H	H	L	L	H
− 40dB	L	L	H	L	H
− 42dB	H	L	H	L	H
− 46dB	L	H	H	L	H
− 50dB	H	H	H	L	H
− 54dB	L	L	L	H	H
− 58dB	H	L	L	H	H
− 62dB	L	H	L	H	H
− 66dB	H	H	L	H	H
− 70dB	L	L	H	H	H
− 74dB	H	L	H	H	H
− 78dB	L	H	H	H	H
− ∞	H	H	H	H	H

ATTENUATOR 2

ATT_{2B}	D_6	D_7
ATT_{2A}	D_{13}	D_{14}
0dB	L	L
− 1dB	L	H
※− 2dB	H	L
※− 3dB	H	H

※2dB・3dB are valid only when ATT is 42dB or less.

TONE	D_{15}	D_{16}	D_{17}	D_{18}
	D_{19}	D_{20}	D_{21}	D_{22}
	D_{23}	D_{24}	D_{25}	D_{26}
12dB	L	H	H	L
10dB	H	L	H	L
8dB	L	L	H	L
6dB	H	H	L	L
4dB	L	H	L	L
2dB	H	L	L	L
0dB	L	L	L	L
0dB	L	L	L	H
− 2dB	H	L	L	H
− 4dB	L	H	L	H
− 6dB	H	H	L	H
− 8dB	L	L	H	H
− 10dB	H	L	H	H
− 12dB	L	H	H	H

Note : Do not input other data than the above.

FADER	D_{27}	D_{28}	D_{29}	D_{30}
0dB	L	L	L	L
− 1dB	H	L	L	L
− 2dB	L	H	L	L
− 3dB	H	H	L	L
− 4dB	L	L	H	L
− 6dB	H	L	H	L
− 8dB	L	H	H	L
− 10dB	H	H	H	L
− 12dB	L	L	L	H
− 14dB	H	L	L	H
− 16dB	L	H	L	H
− 20dB	H	H	L	H
− 30dB	L	L	H	H
− 45dB	H	L	H	H
− 60dB	L	H	H	H
− ∞	H	H	H	H

FADER SELECTION	D_{31}
FRONT	H
REAR	L

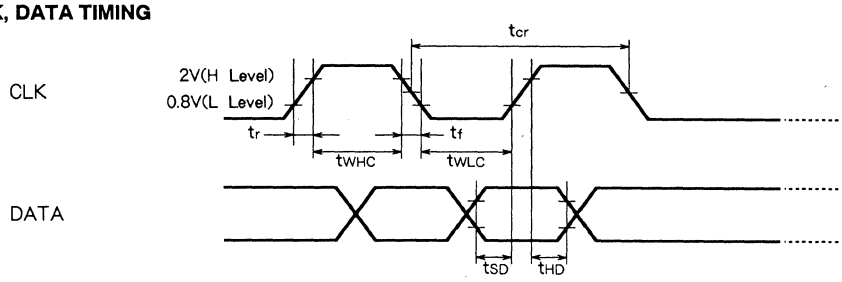
LOUDNESS	D_{32}
ON	H
OFF	L

D_{33}	D_{34}	D_{35}	D_{36}	IC SELECTION
L	L	L	H	M51139FP

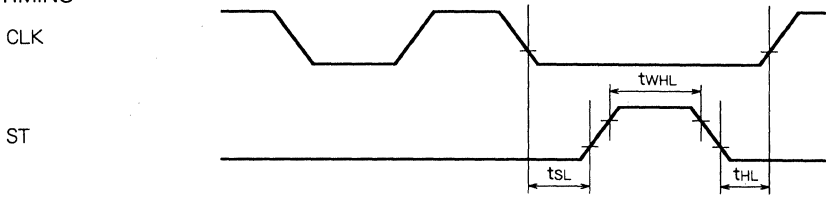
TIMING

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t_{cr}	CLK cycle time	0.8	–	–	μS
t_{WHC}	CLK pulse width ("H" level)	0.3	–	–	μS
t_{WLC}	CLK pulse width ("L" level)	0.3	–	–	μS
t_r	CLK rise time	–	–	0.1	μS
t_f	CLK fall time	–	–		
t_{SD}	DATA setup time	0.2	–	–	μS
t_{HD}	DATA hold time	0.2	–	–	μS
t_{SL}	ST setup time	0.8	–	–	μS
t_{HL}	ST hold time	1	–	–	μS
t_{WHL}	ST "H" pulse width 2V ("H" level)	0.8	–	–	μS

CLK, DATA TIMING

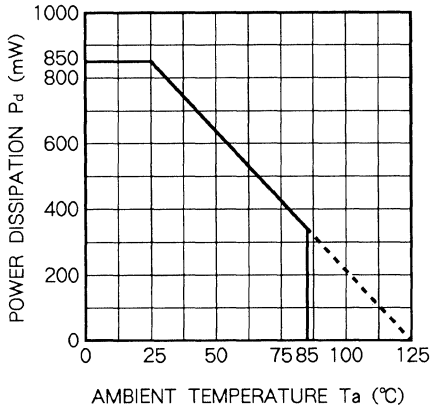


ST TIMING

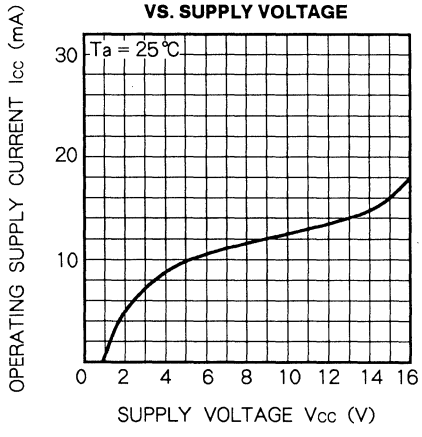


TYPICAL CHARACTERISTICS

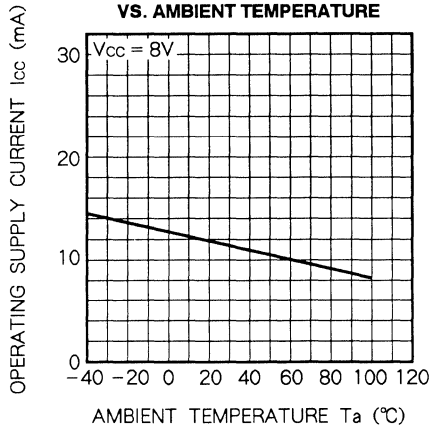
THERMAL DERATING



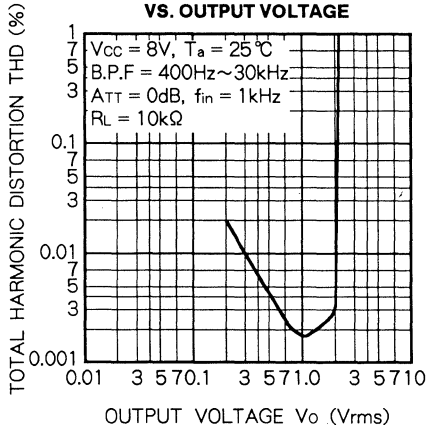
OPERATING SUPPLY CURRENT VS. SUPPLY VOLTAGE



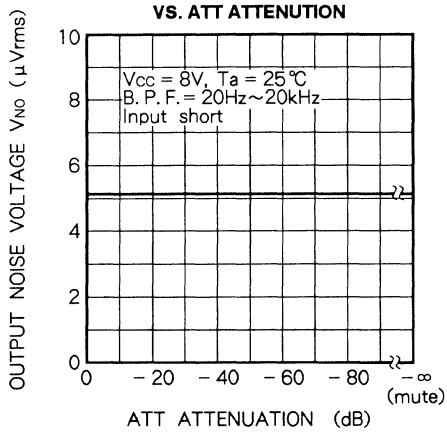
OPERATING SUPPLY CURRENT VS. AMBIENT TEMPERATURE



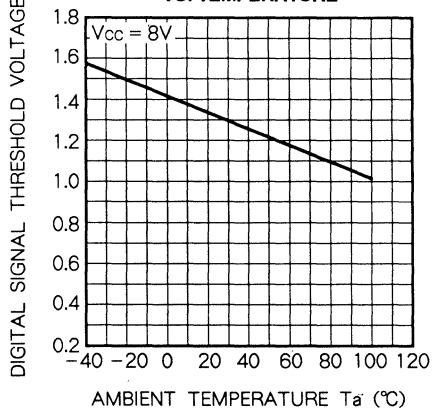
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



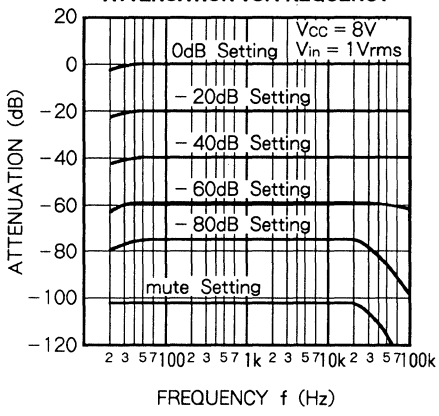
OUTPUT NOISE VOLTAGE VS. ATT ATTENUTION



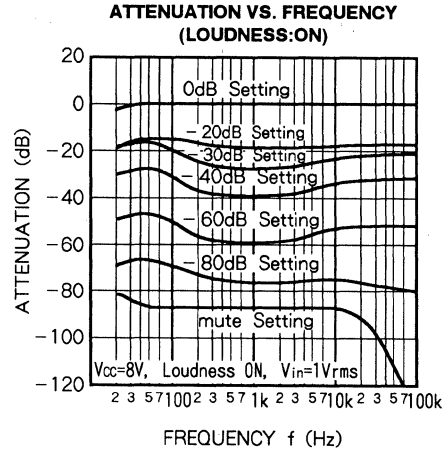
DIGITAL SIGNAL THESHOLD VOLTAGE VS. TEMPERATURE



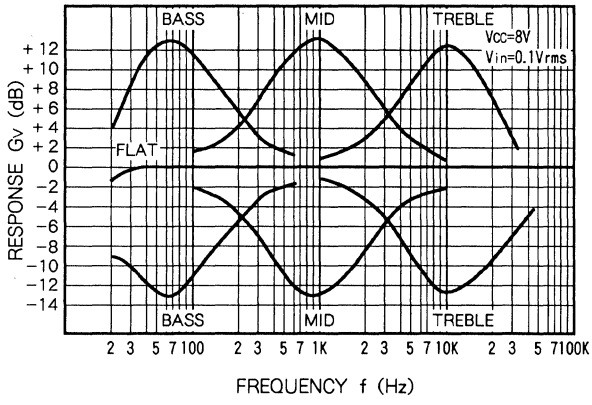
ATTENUATION VS. FREQUENCY



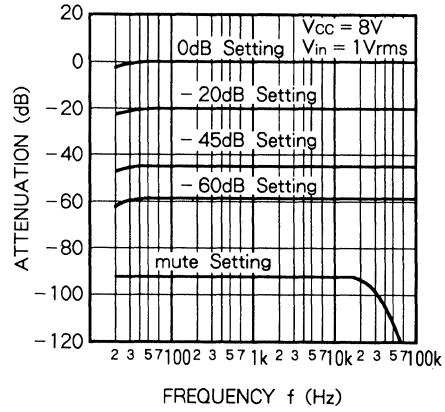
ATTENUATION VS. FREQUENCY (LOUDNESS:ON)



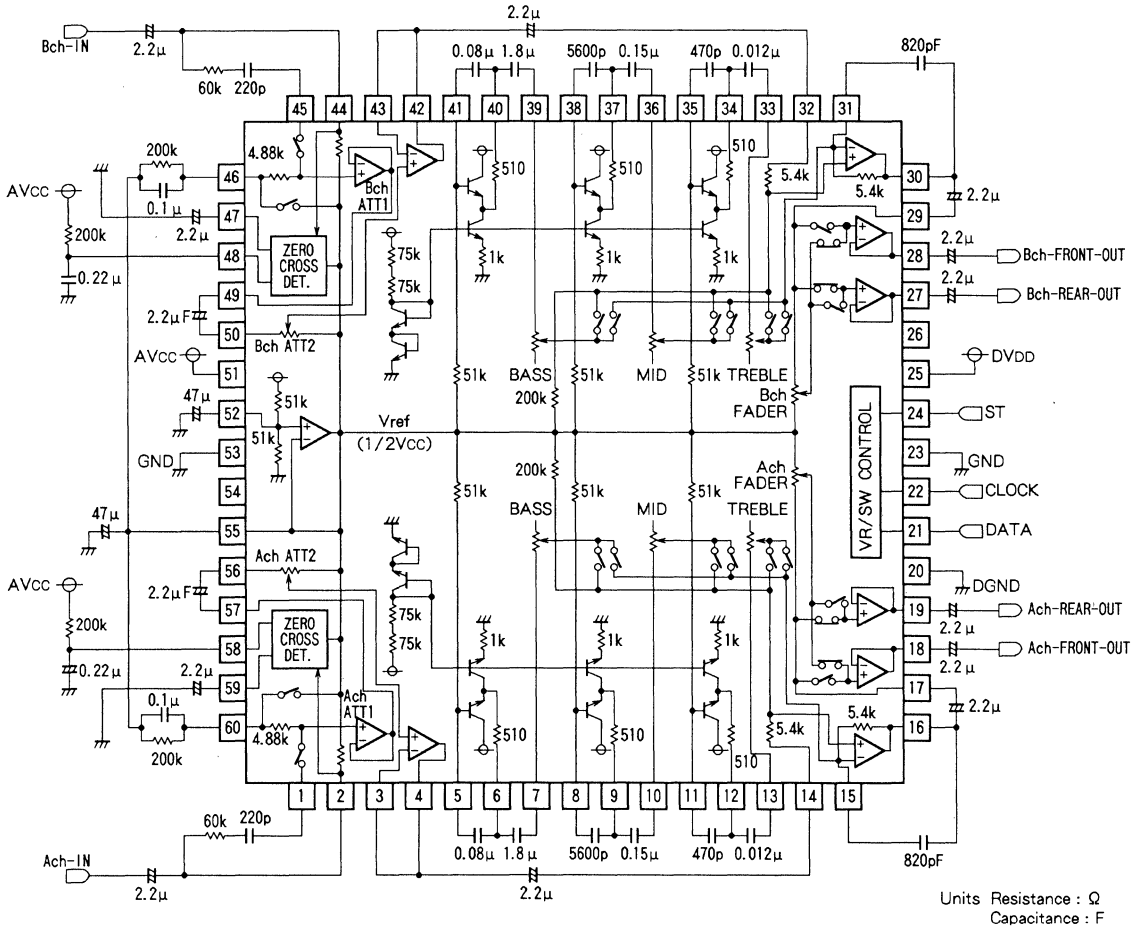
TONE FREQUENCY CHARACTERISTIC



FADER FREQUENCY CHARACTERISTIC



APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

M62402GP

SERIAL DATA CONTROLLED 8-ELEMENT GRAPHIC EQUALIZER

DESCRIPTION

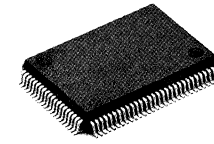
The M62402GP is an IC developed for miniature unit audio systems, has built-in 2 channels of 8-element graphic equalizers and volume controls. These blocks are controlled by serial data.

The volume control consists of a high-performance VCA + 8-bit DAC. This configuration smoothens switching noise occurring when the volume control is operated.

The IC is suitable for use in TV sets, as well as in home-use audio systems.

FEATURES

- Capable of processing analog voice signals with a single chip, a feature required in miniature unit audio systems.
- Small distortion THD = 0.005 %(V_O = 0.5Vrms)
- Large ATT range ..... 0 ~ – 90dB
- Each function controllable with serial data
- VCA + DAC configuration minimizes switching noise in volume control
- Each element in graphic equalizer capable of independent control in a range between –10dB and ~10dB in 2dB/STEP



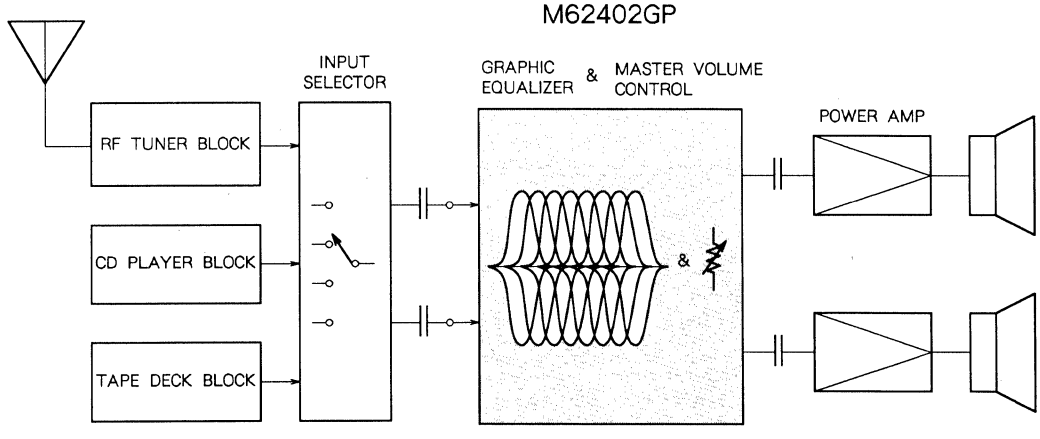
Outline 100P6S-A
0.65mm pitch QFP
(20.0mm × 14.0mm × 2.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC}, V_{EE} = ± 6.5 ~ ± 7.5V
V_{DD} = 4.5 ~ 5.5V

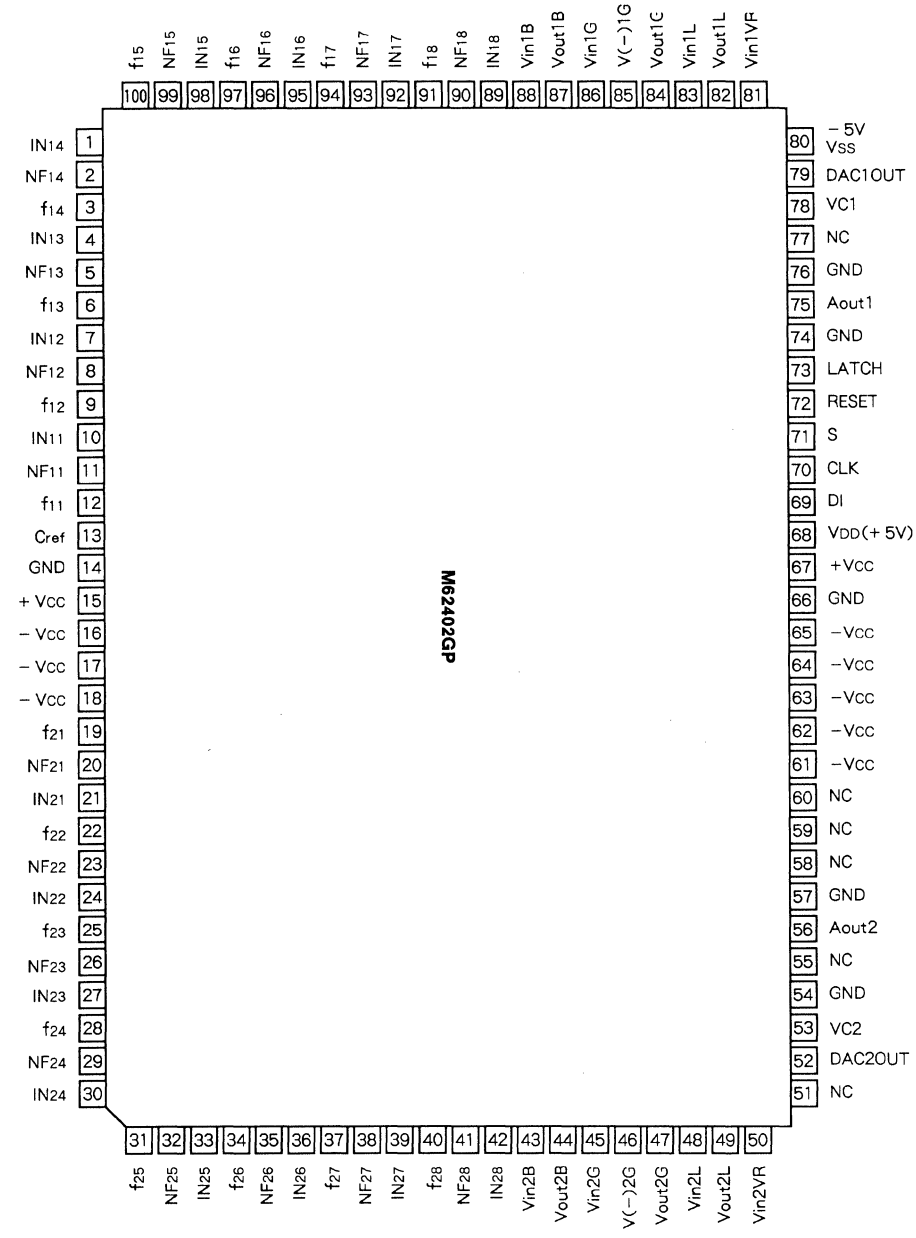
Rated supply voltage ..... V_{CC}, V_{EE} = ± 7V
V_{DD} = 5V

SYSTEM CONFIGURATION



MITSUBISHI ELECTRIC

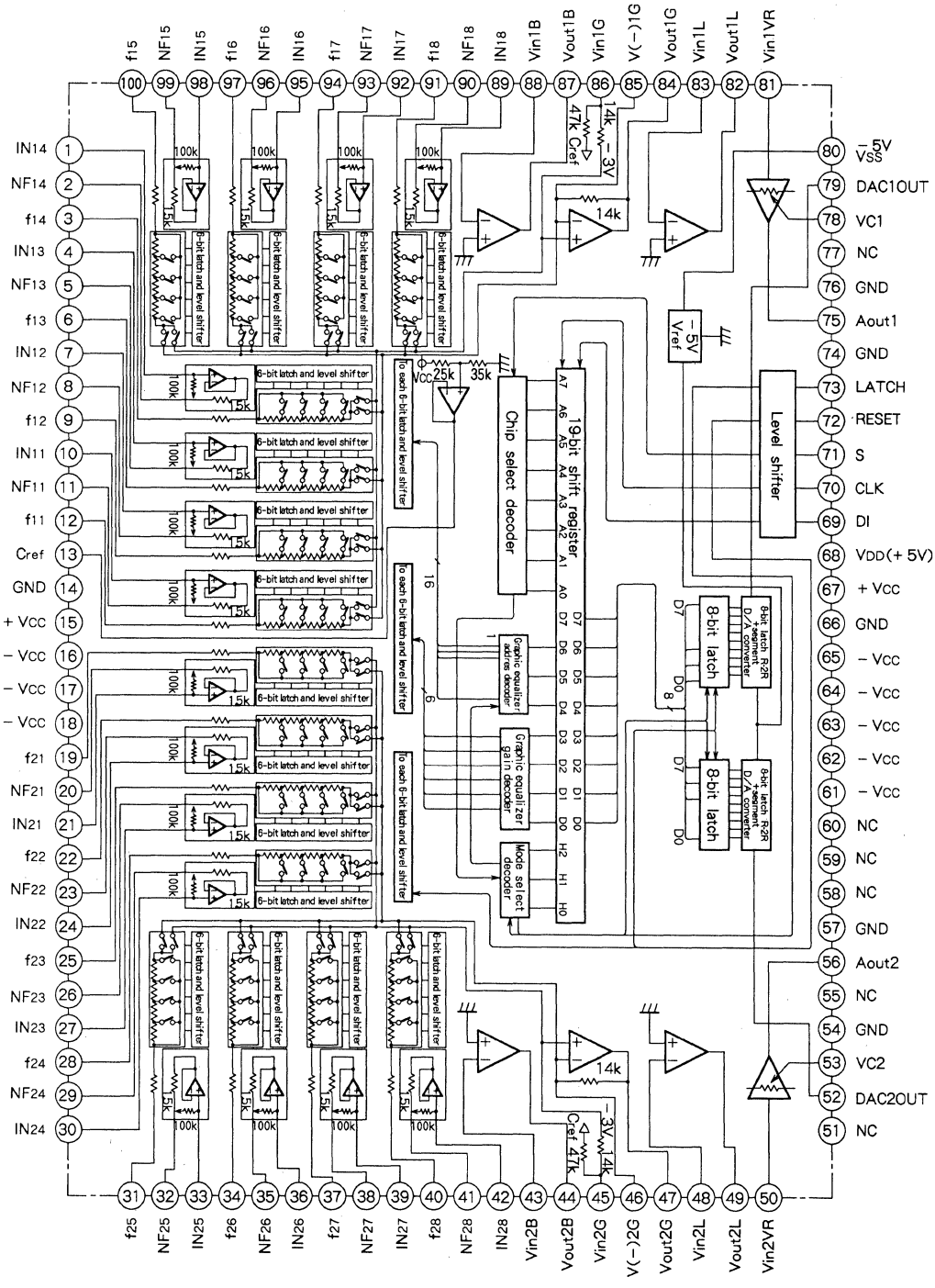
PIN CONFIGURATION



Outline 100P6S-A

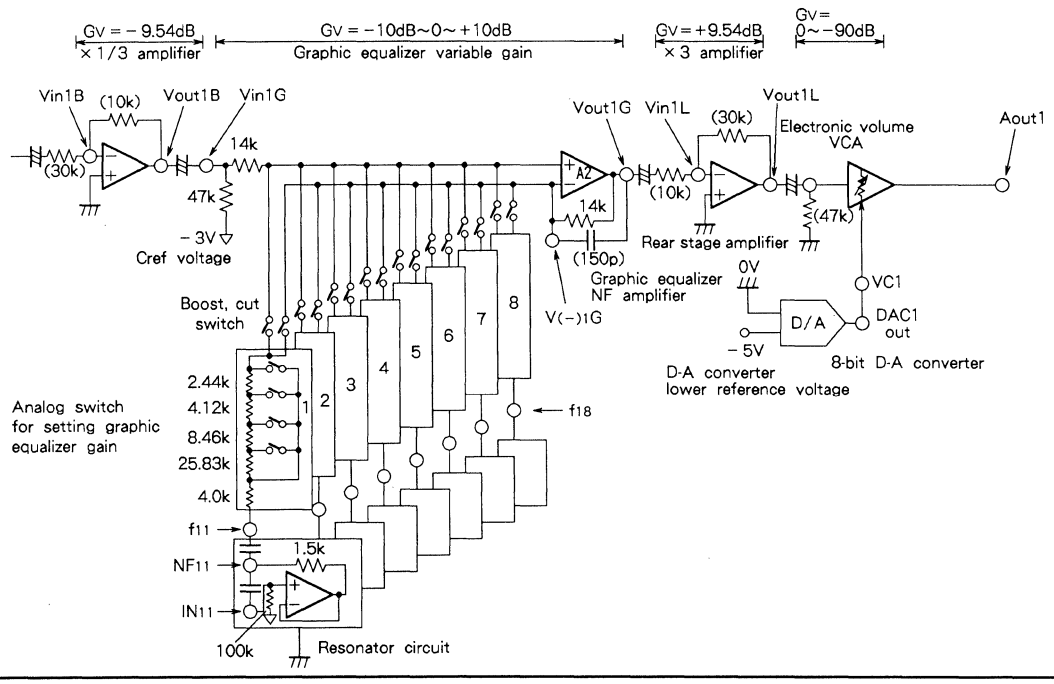
NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM

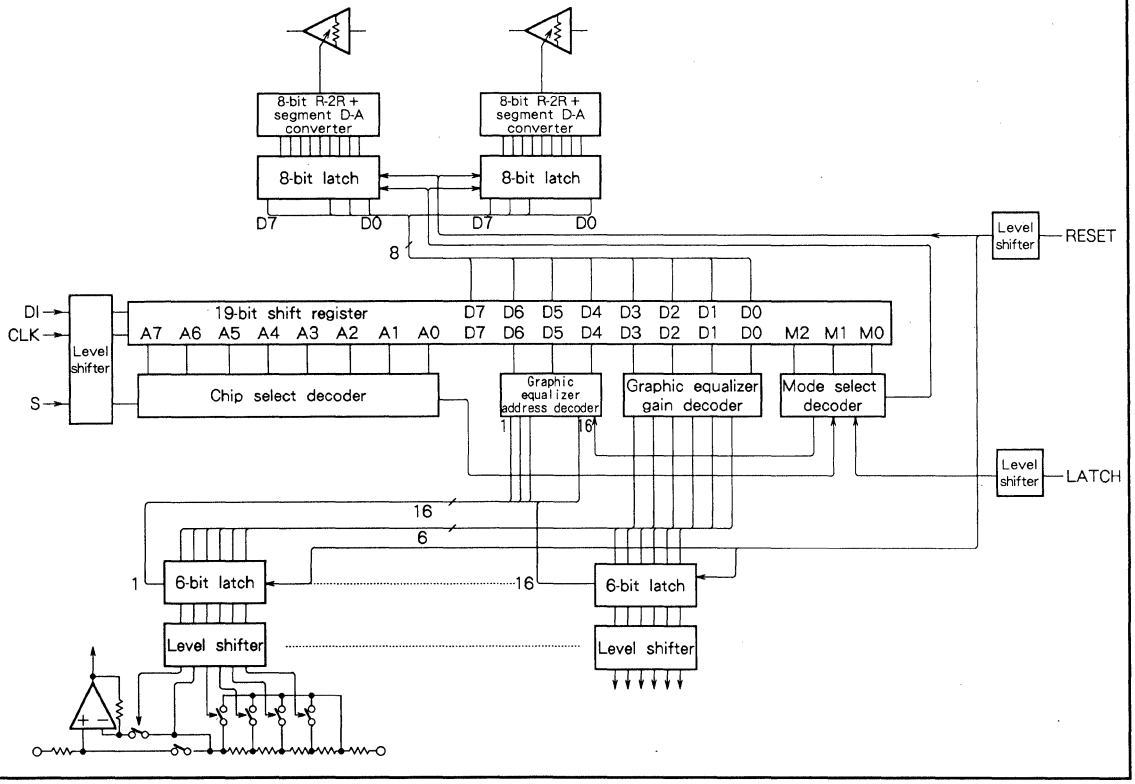


Note : Voltage to ± Vcc and GNDpins must be applied through a common external wire because there are several pins.

BLOCK DIAGRAM (ANALOG SIGNAL CIRCUIT)



BLOCK DIAGRAM (DIGITAL SIGNAL CIRCUIT)



PIN DESCRIPTION

Pin No.	Symbol	Function
㊾	DI	Serial data input. 19-bit serial data is input.
㊿	CLK	Shift clock input pin. When the shift clock rises, the input signal from the DI pin is input to the 19-bit shift register.
㊸	LATCH	The value in the 19-bit shift register is loaded in graphic equalizer and D/A converter when a high level is input.
㊶	S	Select pin when two chips are used. When high level, chip is selected with : When low level, chip is selected with : A0 A1 A2 A3 A4 A5 A6 A7 0 1 1 1 1 1 0 0 A0 A1 A2 A3 A4 A5 A6 A7 0 1 1 1 1 0 0 0
㊷	Reset	When this pin is set to "L", master volume is initialized to ATTmax and graphic equalizer is initialized to flat.
㊽	V_{DD}(+5V)	Logic power supply pin
㊽	Vin1B	Analog input pin (initial stage amplifier input)
㊸	Vin2B	
㊼	Vout1B	Analog output pin (initial stage amplifier input)
㊹	Vout2B	
㊻	Vin1G	Graphic equalizer input pin. DC bias is necessary.
㊺	Vin2G	
㊹	Vout1G	Graphic equalizer output pin.
㊼	Vout2G	
㊺	V(−)1G	Graphic equalizer NF amplifier (−) input pin
㊻	V(−)2G	
㊸	Vin1L	Level shift amplifier input pin
㊽	Vin2L	
㊷	Vout1L	Level shift amplifier output pin
㊾	Vout2L	
㊶	Vin1 VR	Master volume input pin
㊿	Vin2 VR	
㊵	−5V(V_{SS})	D/A converter lower reference voltage monitor pin
㊴	DAC1out	D/A converter output pin
㊷	DAC2out	
㊳	VC1	Master volume control pin
㊸	VC2	
⑬	Cref	Graphic equalizer amplifier bias voltage pin. −3V (typ.) is output (at $-V_{CC} = -7V$). Insert a capacitor (approx. 10μF) between this pin and GND to stabilize the bias voltage.
㊺	Aout1	Analog output pin
㊽	Aout2	
③, ⑥, ⑨, ⑫, ⑲, ㉒, ㉕, ㉘, ㉛, ㉞, ㊲, ㊵, ㊶, ㊹, ㊼, ㊿	f_{nn}	Resonator impedance (band filter) connection pin
①, ④, ⑦, ⑩, ㉑, ㉔, ㉗, ㉚, ㉝, ㉖, ㉙, ㊷, ㊾, ㊽, ㊻, ㊸	IN_{nn}	A band filter is formed by connecting a capacitor to IN_{nn} and NF_{nn}.
②, ⑤, ⑧, ⑪, ⑳, ㉓, ㉖, ㉙, ㉜, ㉟, ㊳, ㊶, ㊿, ㊸, ㊻, ㊹	NF_{nn}	

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	± 8 (16)	V
V_{DD}	Digital power supply	7	V
V_I	Digital input voltage	− 0.3~V_{DD} + 0.3	V
VinG	Graphic equalizer input voltage	− V_{CC}~0.8	V
P_d	Power dissipation	2300 ※	mW
T_{opr}	Operating temperature	−20~+ 75 ※	℃
T_{stg}	Storage temperature	−55~+125	℃

※A 49mm² copper foil is attached.

ELECTRICAL CHARACTERISTICS (ANALOG CIRCUIT) (Ta = 25℃, V_{CC} = ± 7V, V_{DD} = 5V)

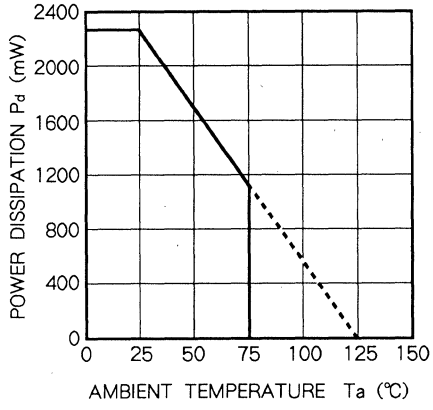
Symbol		Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
+ I_{CC}		Circuit current	Vin = 0	40	60	80	mA
− I_{CC}							mA
I_{DD}			Vin = 0	15	40	90	μA
GV ± 10	Graphic equalizer	Graphic equalizer voltage gain	±10dB f = 1kHz, Vo = 1Vrms, * Each resonance circuit set to resonate at f = 1kHz, * Gain between input pins 86, 45 and graphic equalizer output pins 84, 47	± 8.5	± 10	± 11	dB
GV ± 8			±8dB	± 7	± 8	± 9.5	dB
GV ± 6			±6dB	± 5	± 6	± 7.5	dB
GV ± 4			±4dB	± 3	± 4	± 5.5	dB
GV ± 2			±2dB	± 1	± 2	± 3	dB
GV0			0dB	− 1	0	+ 1	dB
V_{OM1}		Maximum output voltage	THD = 1 %, f = 1kHz, ALL Flat	1.2	1.4		Vrms
THD1		Total harmonic distortion	Vo = 1Vrms, f = 1kHz, ALL Flat		0.005	0.05	%
A_{TTM}	Electronic volume	Maximum attenuation	ATT = − ∞, f = 1kHz, Vi = 0dBm	80	97		dB
A_{TT}		Attenuation error	ATT = 0dB, f = 1kHz, Vi = 0dBm	− 2.3	− 0.3	+ 1.7	dB
Δ A_{TT}		Inter-channel attenuation error	ATT = 0dB, f = 1kHz, Vi = 0dBm		± 0.1	± 2.0	dB
Δ A_{TT} (− 10~ − 30)		Inter-channel error deviation	f = 1kHz, Vi = 0dBm (inter-channel error at −10dB attenuation) − (inter-channel error at −30dB attenuation)	− 2.2	0	2.2	dB
Δ A_{TT} (− 10~ − 60)		Inter-channel error deviation	f = 1kHz, Vi = 0dBm (inter-channel error at −10dB attenuation) − (inter-channel error at −60dB	− 2.2	0	2.2	dB
V_{OM2}		Maximum output voltage	ATT = 0dB, f = 1kHz, THD = 1 %	1.0	1.3		Vrms
V_{IM}		Maximum input voltage	ATT = − 14dB, f = 1kHz, THD = 1 %	2.5	3.5		Vrms
THD2		Total harmonic distortion	ATT = 0dB, f = 1kHz, Vo = 0.5Vrms		0.005	0.05	%
V_{NO}		Output noise voltage	ATT = − ∞, R_g = 0, IHF-A		6.5	30	μVrms
V_{OO}		Output offset voltage	Vi = 0, ATT = − ∞~0dB	− 300		+ 300	mV

Note 1. The graphic equalizer voltage gain ratings − 10dB to 0dB to + 10dB are never reversed.

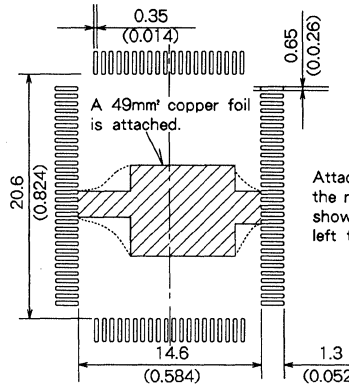
2. A 400Hz HPF and a 30kHz LPF are used when measuring the total harmonic distortion.

TYPICAL CHARACTERISTICS

THERMAL DERATING
(MAXIMUM RATING)



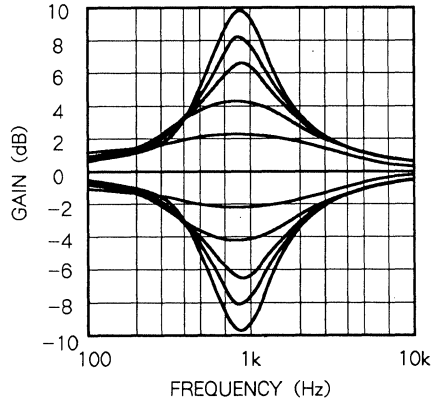
Unit : mm(inch)



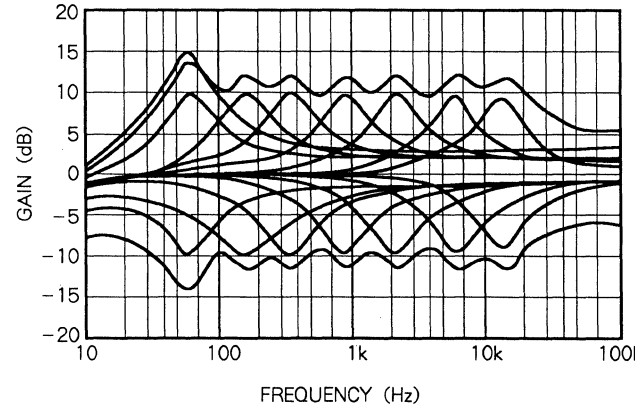
Attach a copper foil around the root of the −Vcc pin as shown by the dotted line at left to improve.

Recommended Mount Pad

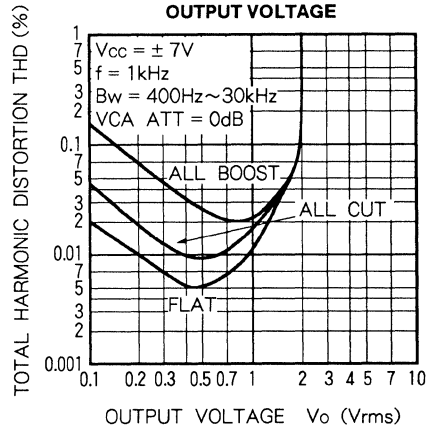
GRAPHIC EQUALIZER(1-ELEMENT) GAIN
VS. FREQUENCY



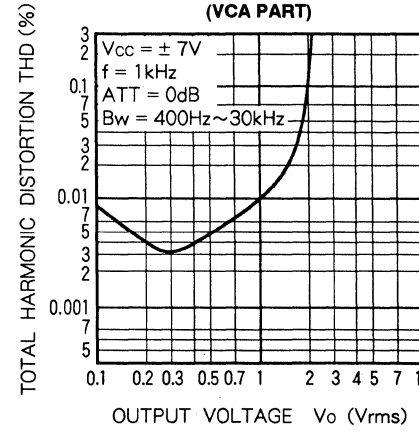
GRAPHIC EQUALIZER GAIN VS. FREQUENCY



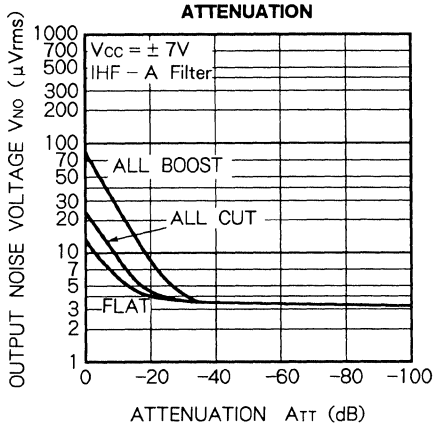
TOTAL HARMONIC DISTORTION VS.
OUTPUT VOLTAGE



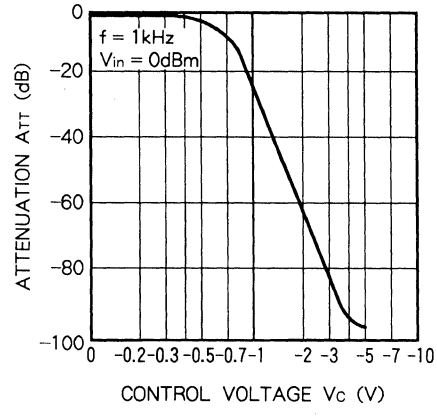
TOTAL HARMONIC DISTORTION VS.
OUTPUT VOLTAGE
(VCA PART)



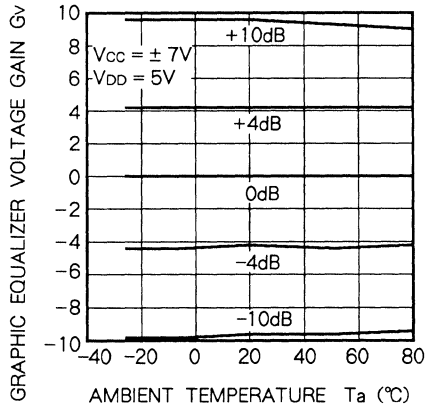
OUTPUT NOISE VOLTAGE VS. ATTENUATION



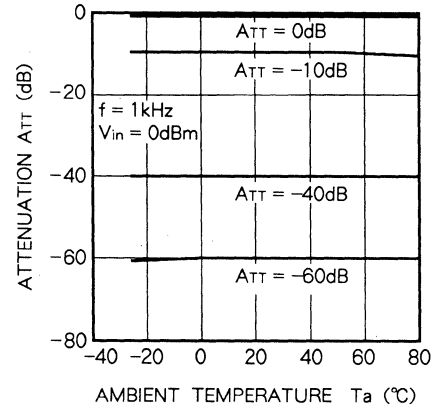
ATTENUATION VS. CONTROL VOLTAGE



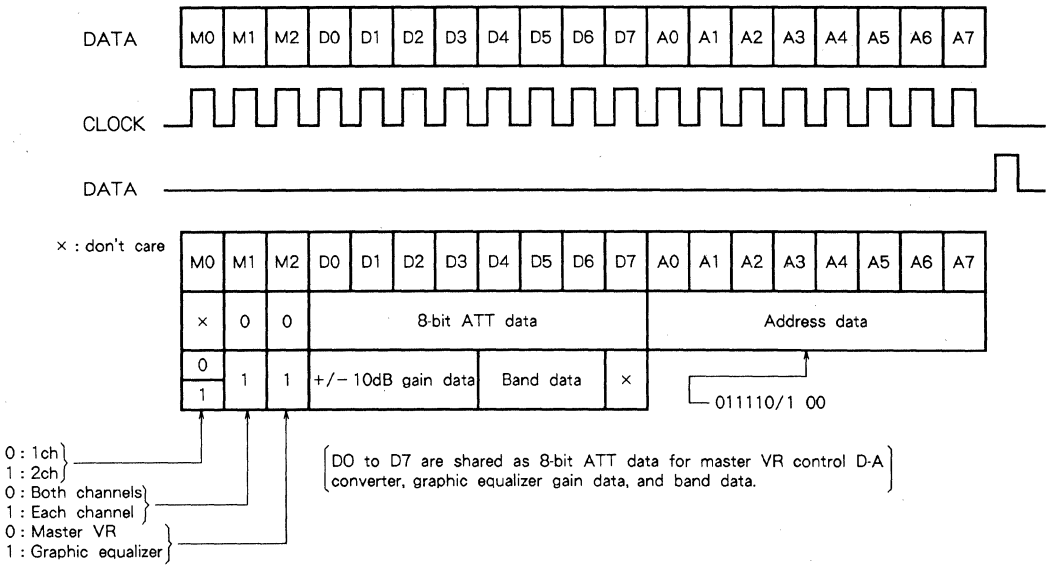
GRAPHIC EQUALIZER VOLTAGE GAIN VS. AMBIENT TEMPERATURE



ATTENUATION VS. AMBIENT TEMPERATURE



DIGITAL DATA INPUT SIGNAL FORMAT



GRAPHIC EQUALIZER GAIN DATA

Code / Gain	D3	D2	D1	D0
10dB	0	1	0	1
8	0	1	0	0
6	0	0	1	1
4	0	0	1	0
2	0	0	0	1
0	0	1	1	0
− 2	1	0	0	1
− 4	1	0	1	0
− 6	1	0	1	1
− 8	1	1	0	0
− 10	1	1	0	1

GRAPHIC EQUALIZER BAND DATA

Code / Band	D6	D5	D4
f 1	0	0	0
f 2	0	0	1
f 3	0	1	0
f 4	0	1	1
f 5	1	0	0
f 6	1	0	1
f 7	1	1	0
f 8	1	1	1

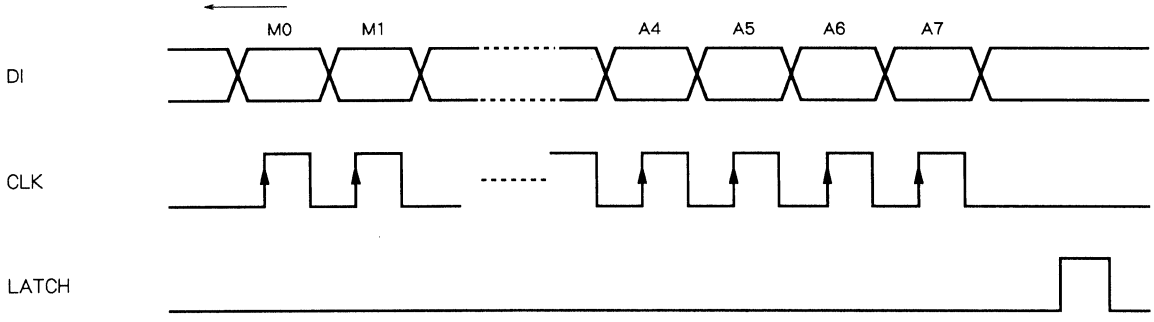
MASTER VR ATT DATA

Code / ATT	D7	D6	D5	D4	D3	D2	D1	D0
ATT max	0	0	0	0	0	0	0	0
					⟆			
ATT 0	1	1	1	1	1	1	1	1

Note : The values are as follows when using under Vcc = ± 7V.

Code / ATT	D7	D6	D5	D4	D3	D2	D1	D0
ATT max	0	0	1	0	0	0	0	0
					⟆			
ATT 0	1	1	1	1	1	1	1	1

RELATIONSHIP BETWEEN DATA AND CLOCK



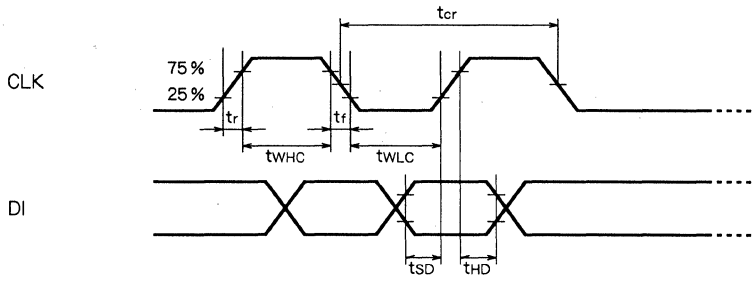
DIGITAL CIRCUIT DC CHARACTERISTICS (Ta = −20~75℃, V_{CC} = ± 7V, V_{DD} = 5V)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IL}	"L" level input voltage	DI, CLK, LATCH, RESET, S pins		0	~	0.2V_{DD}	V
V_{IH}	"H" level input voltage			0.8V_{DD}	~	V_{DD}	V
I_{IL}	"L" level input current	V_I = 0	DI, CLK, LATCH, RESET, S pins	−10	−	10	μA
I_{IH}	"H" level input current	V_I = V_{DD}		−	−	10	μA

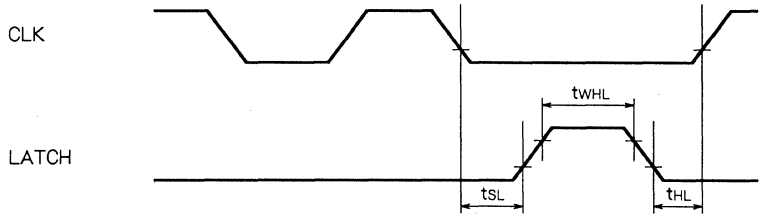
DIGITAL CIRCUIT AC CHARACTERISTICS (Ta = −20~75℃, V_{CC} = ± 7V, V_{DD} = 5V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{cr}	CLK cycle time		2	−	−	μs
t_{WHC}	CLK pulse width("H"level)		0.8	−	−	μs
t_{WLC}	CLK pulse width("L"level)		0.8	−	−	μs
t_r	CLK rise time		−	−	0.2	μs
t_f	CLK fall time		−	−	0.2	μs
t_{SD}	DI setup time		0.4	−	−	μs
t_{HD}	DI hold time		0.4	−	−	μs
t_{SL}	LATCH setup time		0.8	−	−	μs
t_{HL}	LATCH hold time		1	−	−	μs
t_{WHL}	LATCH "H" pulse width		0.8	−	−	μs
t_{MR}	RESET hold time		1	−	−	μs
t_{WLR}	RESET "L" hold pulse width		0.8	−	−	μs

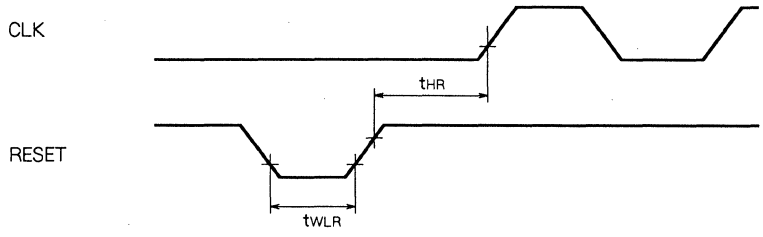
CLK, DI TIMING



LATCH TIMING



RESET TIMING



M62402GP SERIAL DATA MASTER VOLUME ATTENUATION COMPARISON TABLE (REFERENCE) (V_{CC} = ± 7V)

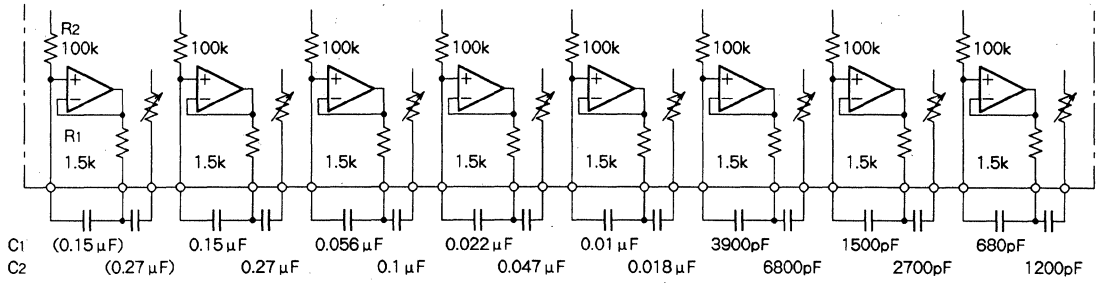
Serial data D7~D0		Master volume attenuation ATT (dB)
1111	1111	0
1110	1010	− 1
	0111	− 2
	0101	− 3
	0011	− 4
	0010	− 5
	0001	− 6
↓	0000	− 7
1101	1111	− 8
	1110	− 9
	1101	− 10
	1100	− 11
	1011	− 12
	1010	− 13
	1001	− 14
	1000	− 15
	0111	− 16
	0110	− 17
	0101	− 18
	0100	− 19
	0011	− 20
	0010	− 21
	0001	− 22
↓	0000	− 23
1100	1111	− 24
	1110	− 25
	1101	− 26
	1100	− 27
	1011	− 28
	1010	− 29
↓	1001	− 30

Serial data D7~D0		Master volume attenuation ATT (dB)
1100	0111	− 31
	0110	− 32
	0101	− 33
	0100	− 34
	0011	− 35
	0010	− 36
↓	0000	− 37
1011	1111	− 38
	1110	− 39
	1101	− 40
	1011	− 41
	1010	− 42
	1001	− 43
	0111	− 44
	0110	− 45
	0100	− 46
	0011	− 47
	0001	− 48
↓	0000	− 49
1010	1110	− 50
	1101	− 51
	1011	− 52
	1001	− 53
	1000	− 54
	0110	− 55
	0100	− 56
	0010	− 57
↓	0001	− 58
1001	1111	− 59
↓	1101	− 60

Serial data D7~D0		Master volume attenuation ATT (dB)
1001	1011	− 61
	1001	− 62
	0111	− 63
	0101	− 64
	0011	− 65
↓	0001	− 66
1000	1111	− 67
	1100	− 68
	1010	− 69
	1000	− 70
	0110	− 71
	0011	− 72
↓	0001	− 73
0111	1110	− 74
	1100	− 75
	1001	− 76
	0111	− 77
	0100	− 78
↓	0001	− 79
0110	1110	− 80
	1100	− 81
	1001	− 82
	0110	− 83
	0011	− 84
↓	0000	− 85
0101	1101	− 86
	1010	− 87
	0110	− 88
	0011	− 89
↓	0000	− 90

Serial data D7~D0		Master volume attenuation ATT (dB)
0100	1100	− 91
	1001	− 92
	0101	− 93
↓	0010	− 94
0011	1110	− 95
↓	↓	↓
0000	0000	ATT M

GRAPHIC EQUALIZER CIRCUIT RESONATOR BLOCK APPLICATION EXAMPLE

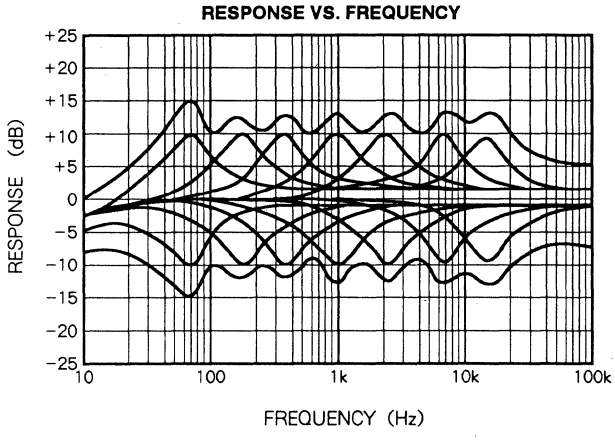


THEORETICALL VALUES

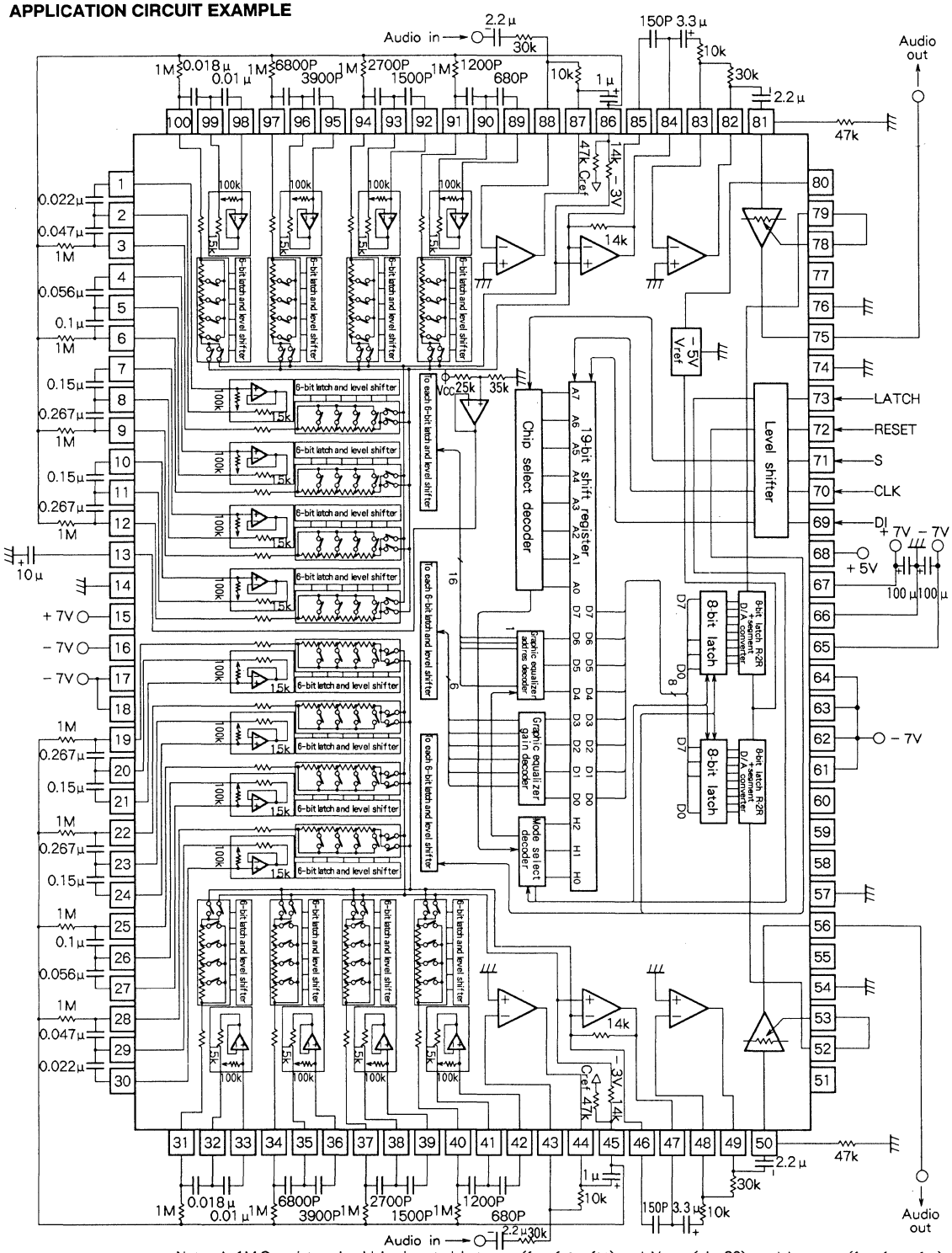
fo	(65Hz)	65Hz	174Hz	404Hz	970Hz	2.5kHz	6.46kHz	14.4kHz
Q	(1.67)	1.67	1.67	1.52	1.66	1.70	1.66	1.68

FREQUENCY CHARACTERISTICS

$$fo = \frac{1}{2\pi\sqrt{R1 \cdot R2 \cdot C1 \cdot C2}}$$

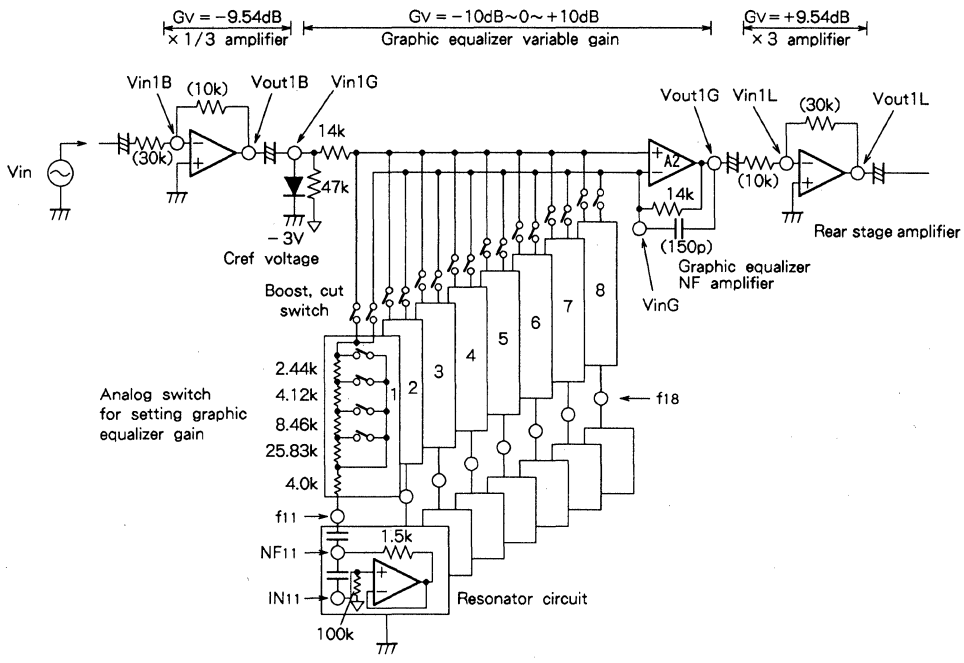


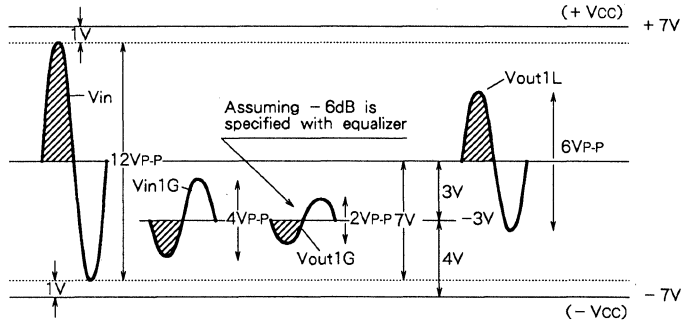
APPLICATION CIRCUIT EXAMPLE



Note : A 1MΩ resistor should be inserted between (f_{11}, f_{12},···f_{20}) and V_{in1G} (pin 86), and between (f_{21}, f_{22},···f_{28}) and V_{in2G} (pin 45) to reduce the noise when switching the graphic equalizer.

USING THE GRAPHIC EQUALIZER AMPLIFIER





The breakdown voltage (between drain and source) of the analog switch used in this IC is approximately 8V. THerefore, the voltage input to the graphic equalizer amplifier (Vin1 or 2G) must satisfy (Vin1 or 2G) − (− Vcc) ≦ 8V − (*).

An equalizer effect can be achieved without lowering the dynamic range by connecting a × 1/3 and × 3 amplifier before and after the graphic equalizer amplifier and shifting the DC voltage to − 1/2Vcc level as shown in the above figure. (The DC voltage of the graphic equalizer is fixed internally at − 1/2Vcc).

The above condition (*) can be satisfied by connecting a diode between the graphic equalizer input pin (Vin1 or 2G) and GND in the direction shown in the figure.

M62403P,FP

AUTOMATIC POWER SWITCH WITH EQUALIZER CONTROL

DESCRIPTION

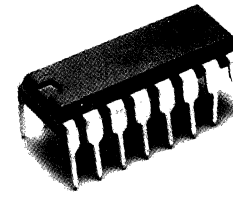
The M62403 is an IC best suited to the amplification of small audio signals, such as are produced by headphone tape cassette players, to distribute to active speakers.

The IC has two functions, auto power switching on/off circuit and atomatic loudness control, which realize low power dissipation of batteries that drive active speakers.

Application of the M62403P,FP include controlling active speakers for small audio systems.

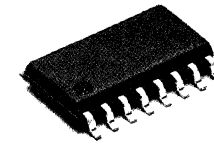
FEATURE

- Wide supply voltage range (Vcc = 3.5~12.5V).
- Auto power control ON/OFF.
- Capable of direct driving of power transistor (PNP type)
- High sensitivity in detection of audio signals (3mVrms typ.)
- Automatically holds in on state for preset time (timer function)
- LED drive pin built-in for alarming operating conditions.
- Supply voltage monitor function for prevention of leakage of battery liquid.
- Automatic loudness controller built-in.
- Capable of controlling frequency characteristics correction time.



Outline 16P4(P)

2.54mm pitch 300mil DIP
(6.3mm × 19.0mm × 3.3mm)



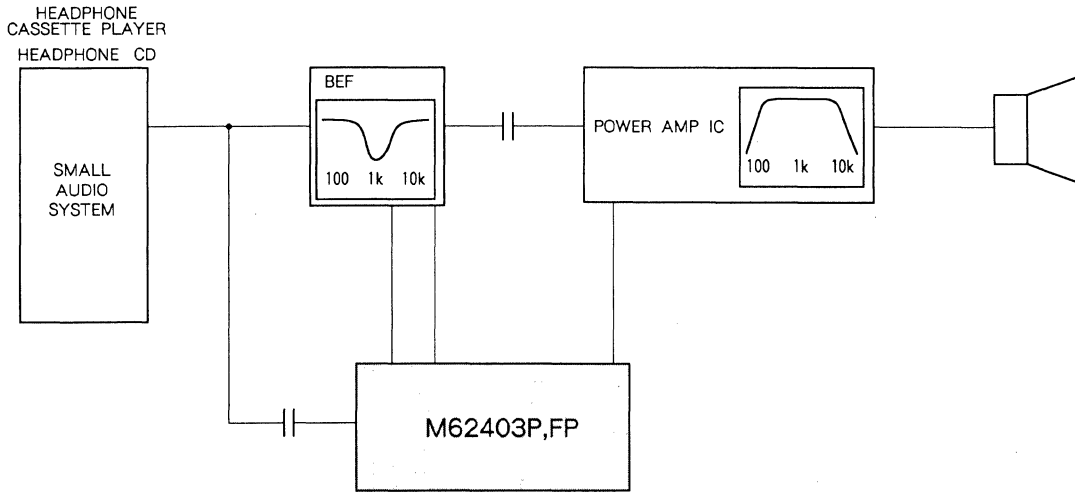
Outline 16P2N-A(FP)

1.27mm pitch 300mil SOP
(5.3mm × 10.1mm × 1.8mm)

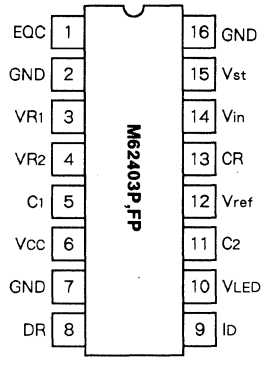
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· Vcc = 3.5~12.5V
Rated supply voltage ····· Vcc = 6V
Rated dissipation voltage ····· 1000mW(P)
500mW(FP)

SYSTEM CONFIGURATION

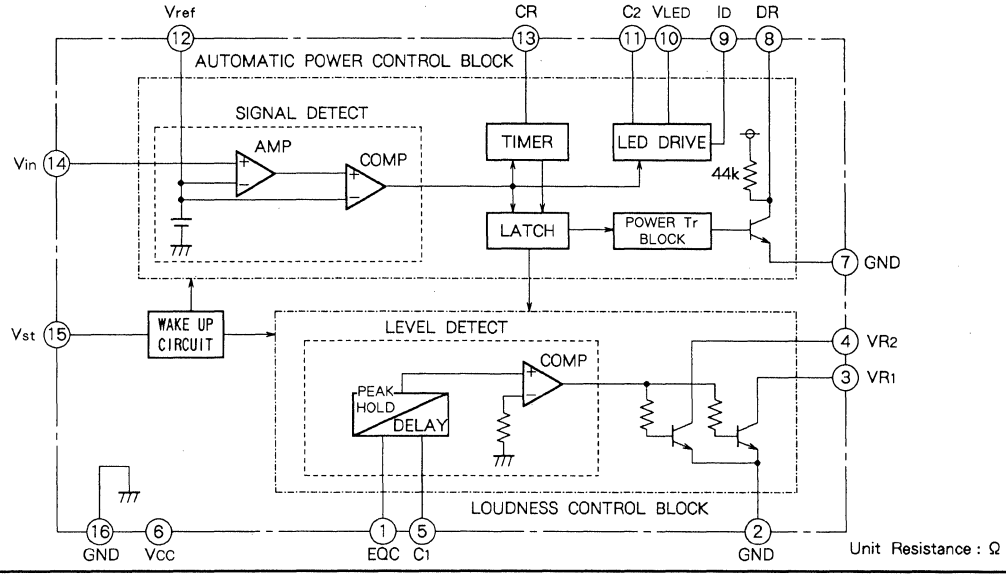


PIN CONFIGURATION



Outline 16P4(P)
16P2N-A(FP)

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	15	V
V_{IN}	Input voltage	15	V
V_{EQC}	Input voltage	± 10(7Vrms)	V
$V_{VR1,2}$	Input voltage	15	V
P_d	Power dissipation	1000(P) / 550(FP)	mW
T_{opr}	Operating temperature	− 20 ~ + 75	℃
T_{stg}	Storage temperature	− 55 ~ + 125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, f = 1kHz, Vst = Vcc, unless otherwise noted)

Symbol		Parameter		V_{CC}(V)	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}		Supply voltage					3.5	−	12.5	V
I_{CC}		Circuit current	Quiescent	6	V_{IN} = 0V		−	500	600	μA
				9	V_{IN} = 0V		−	700	900	μA
			operating	6	V_{IN} = V_{CC}		−	7	14	mA
				9			−	10	20	mA
I_{sink1}	Loudness control	Sink current of C1		6	V_{IN} = V_{CC}, V_{C1} = 1V		1.5	2	2.5	μA
R_{CE}	Loudness control	Resistance of VR1, VR2	max	6	V_{IN} = 2.2V, C_{EQC} = 0.47μF	V_{EQC} = 220mVrms	70	90	−	kΩ
			min			V_{EQC} = 695mVrms	−	100	200	Ω
DRV_{CE}	Power control	Voltage of DR			V_{IN} = V_{ref}		−	−	V_{CC}	V
$DRV_{CE(sat)}$	Power control	Saturation voltage of DR		6	V_{IN} = V_{CC}	I_{DR} = 20mA	−	100	200	mV
				9		I_{DR} = 30mA	−	150	300	mV
I_{source}	Power control	Source current of ID	Quiescent	6	V_{IN} = 0V	I_D = GND	−	−	2	μA
				9			−	−	2	μA
			operating	6	V_{IN} = V_{CC}		3.5	4.5	5.5	mA
				9			6.4	8	9.8	mA
V_S	Power control	Voltage of signal detect		6	C_{IN} = 0.015μF		2	3	4	mVrms
V_{TH}	Power control	Wake up voltage		6			0.2	0.5	0.8	V
I_{CCOFF}		Dead circuit current		6	V_{st} = 0V, V_{IN} = 0V		−	−	10	μA

REFERENCE CHARACTERISTICS (Ta = 25℃, unless otherwise noted)

Symbol		Parameter	Test conditions	Typical	Unit
R①	Loudness control	Resistance of EQC		6.4	kΩ
t_{RHL}	Loudness control	Response speed	$R_{CE1 \text{ or } 2}$ max → $R_{CE1 \text{ or } 2}$ min	0.2	sec
t_{RLH}	Loudness control		$R_{CE1 \text{ or } 2}$ min → $R_{CE1 \text{ or } 2}$ max	5~6	sec
V_{ref}	Power control	Reference voltage	C_{Vref} = 22μF	2.05	V
R⑭	Power control	Resistance of Vin		100	kΩ
t_{ONK}	Power control	Timer	CR = 33μF, 750kΩ	54~72	sec
t_{ONL}	Power control	Off time of LED	C2 = 1μF	50	msec
−	Power control	Limit of frequency	C_{Vref} = 22μF, C_{Vin} = 0.015μF	100~10k(+3dB)	Hz

M62404P,FP

BUILT-IN AMPLIFIER TYPE ANALOG SWITCH

DESCRIPTION

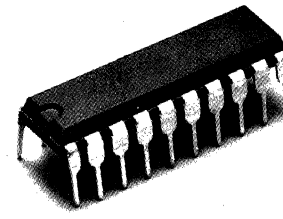
The M62404 is an analog switch IC with a built-in amplifier, which is an optimum device for high-quality sound correction for, example, Hi-Fi VCR applications.

With a voltage applied to the control pin, the IC offers the capability to select tone quality in three modes.

The IC can be used in TV sets, as well as in Hi-Fi VCR.

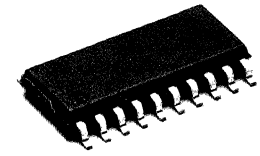
FEATURE

- Low distortion ratio (f = 1kHz, V_O = 1Vrms)
  THD = 0.002%(typ.)
- Low noise (R_g = 2.2kΩ). V_{NI} = 1.7μVrms(typ.)
- 2 channels of 3 mode selectors built-in.
- Can be driven by either single or dual power supply.



Outline 20P4(P)

2.54mm pitch 300mil DIP
(6.3mm × 24.0mm × 3.3mm)



Outline 20P2N-A(FP)

1.27mm pitch 300mil SOP
(5.3mm × 12.6mm × 1.8mm)

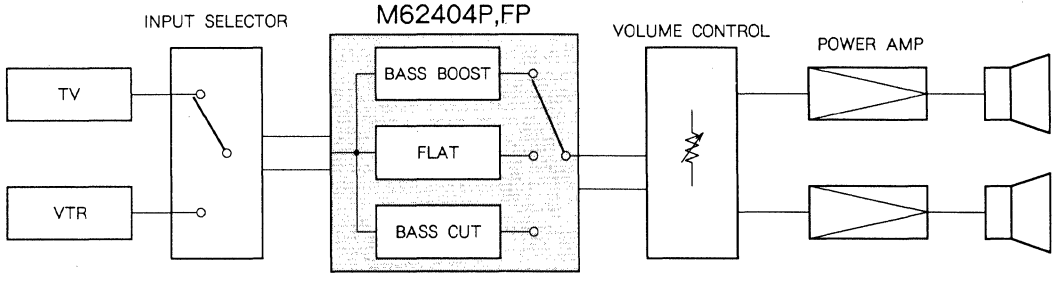
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC}, V_{EE} = ± 4.5~7.5V
or V_{CC} = 9~15V

Rated supply voltage ..... V_{CC}, V_{EE} = ± 6V
or V_{CC} = ± 12V

Rated dissipation voltage ..... 1000mW(P)
550mW(FP)

SYSTEM CONFIGURATION

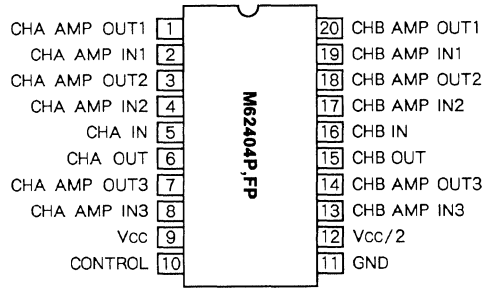


MITSUBISHI ELECTRIC

M62404P,FP

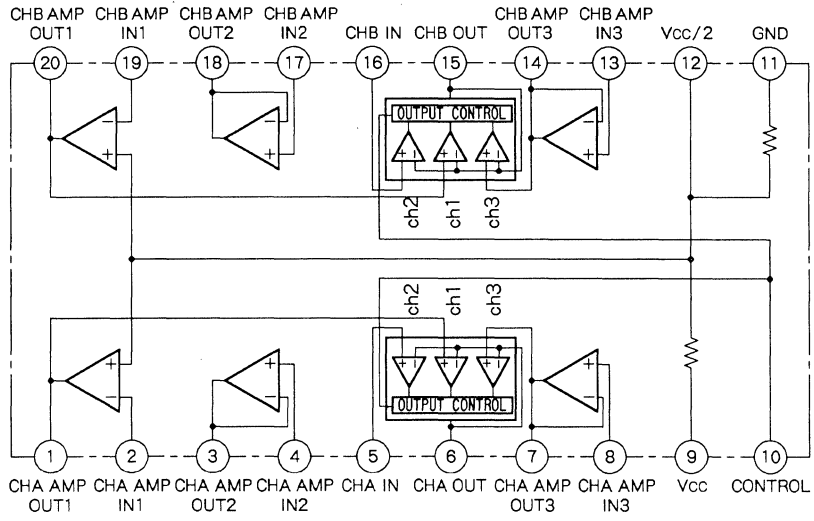
BUILT-IN AMPLIFIER TYPE ANALOG SWITCH

PIN CONFIGURATION



Outline 20P4(P)
20P2N-A(FP)

IC INTERNAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

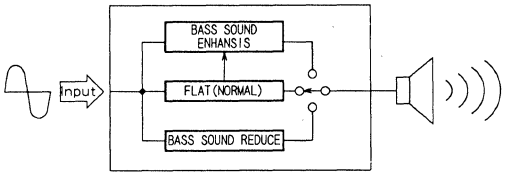
Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	16(±8)	V
P_d	Power dissipation	1000(P)/550(FP)	mW
K_θ	Thermal derating ($T_a \geqq 25$℃)	10.0(P)/5.5(FP)	mW/℃
T_{opr}	Operating temperature	−20~+75	℃
T_{stg}	Storage temperature	−55~+125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC}		Circuit current		−	12.7	−	mA
CT		Crosstalk	f = 1kHz BW : 500Hz~5kHz	−	110	−	dB
V_{IO}	Switch amplifier	Input offset voltage		−	1.0	−	mV
I_B		Input bias current		−	220	−	nA
CS		Channel separation	f = 1kHz BW : 500Hz~5kHz	−	110	−	dB
V_P		Shock noise		−	10	−	mV
THD		Total harmonic distort	f = 1kHz V_O = 1Vrms	−	0.001	−	%
SR		Slew rate		−	2.0	−	V/μsec
V_{OM}		Maximum output voltage	f = 1kHz THD = 0.1%	−	3.1	−	Vrms
V_{NI}		Input referred noise voltage		−	1.7	−	μVrms
I_{Lmax}		Maximum output load current	I_{sink}/I_{source}	1.0	−	2.0	mA
V_{IO}	Buffer amplifier	Input offset voltage		−	1.0	−	mV
I_B		Input bias current		−	40	−	nA
THD		Total harmonic distort	f = 1kHz V_O = 1Vrms	−	0.002	−	%
SR		Slew rate		−	2.5	−	V/μsec
V_{OM}		Maximum output voltage	f = 1kHz THD = 0.1%	−	3.6	−	Vrms
I_{Lmax}		Maximum output load current	I_{sink}/I_{source}	400	−	−	μA
I_B	Inverting amplifier	Input bias current		−	40	−	nA
THD		Total harmonic distort	f = 1kHz V_O = 1Vrms	−	0.002	−	%
V_{OM}		Maximum output voltage	f = 1kHz THD = 0.1%	−	3.6	−	Vrms
I_{Lmax}		Maximum output load current	I_{sink}/I_{source}	400	−	−	μA
ch1	Change voltage			0	−	0.6	V
ch2				1.0	−	5.0	V
ch3				8.0	−	V_{CC}	V

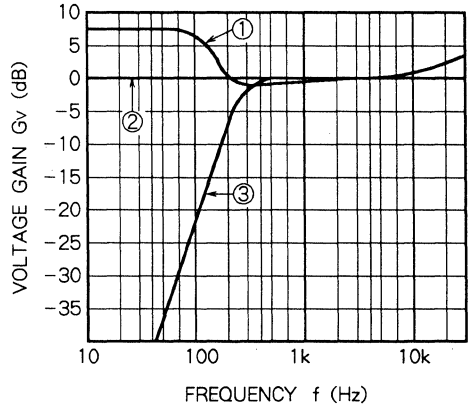
APPLICATION EXAMPLE

M62404P, FP



1. Bass Sound Enhansis ➡ It has powerful sound video tape (Boost) (When video software tape listen)
2. FLAT ➡ Uses normal mode
3. Bass Sound reduce ➡ Reduces noise (When original video software listen for VCR camera)

VOLTAGE GAIN



M62405P

I²C BUS TV ELECTRONIC VOLUME CONTROLLER WITH SURROUND CIRCUIT

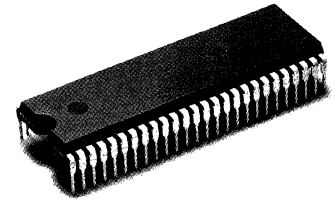
DESCRIPTION

The M62405P is a sound controller developed for TV, it has a built-in volume, tone control, surround and mute circuits. These blocks except the mute circuit are controlled via I²C bus.

The controller is also applicable to other appliances such as home audio.

FEATURES

- Controlled via I²C bus system
- Sound volume, quality (bass & treble/bass boost) and field (surround effect) are adjusted at the front row of power amplifier.
- Geared to analog sound signal processing.
- Serial→parallel extenstion port (5-bit)
- Analog/digital-mixed IC realized by FULL-CMOS.
- Maximum output voltage
  ..... 2.4Vrms(Vcc = 9V, THD = 1%)
- Total harmonic distortion
  .....0.005%(BW=400Hz~30kHz)
- Built-in analog signal reference voltage circuit (1/2Vcc)



Outline 52P4B

1.778mm pitch 600mil SDIP
(13.0mm × 45.85mm × 3.8mm)

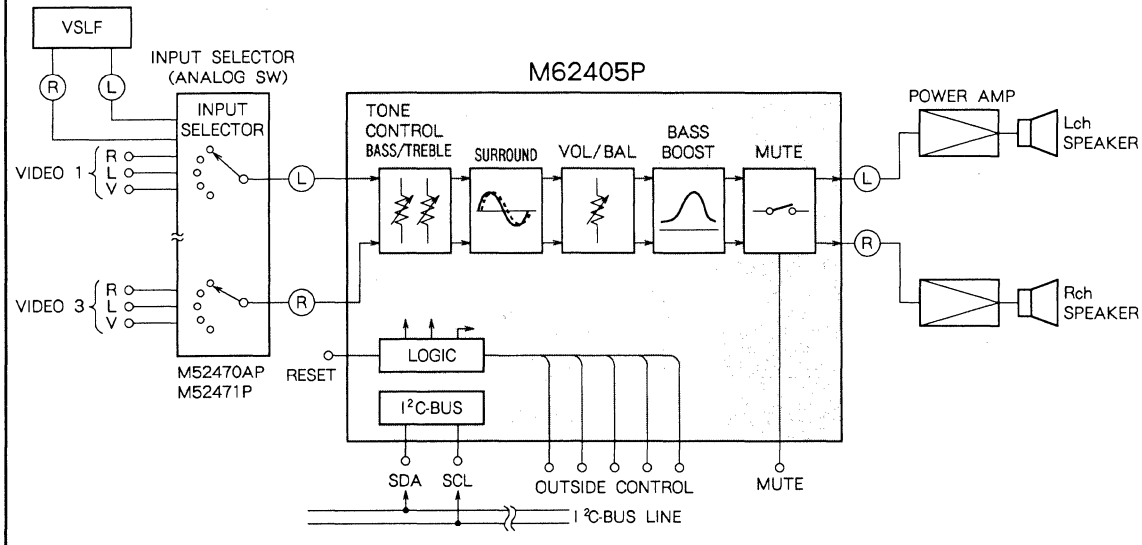
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... Vcc = 5~9V
VDD = 4~6V

Rated supply voltage ..... Vcc = 9V
VDD = 5V

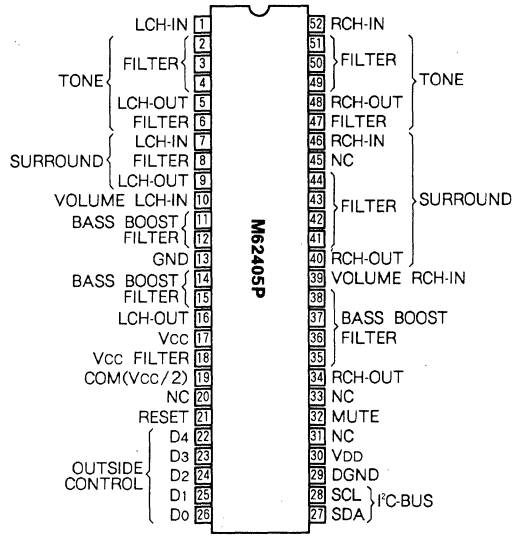
Rated power dissipation 1100mW

SYSTEM CONFIGURATION



I²C BUS TV ELECTRONIC VOLUME CONTROLLER WITH SURROUND CIRCUIT

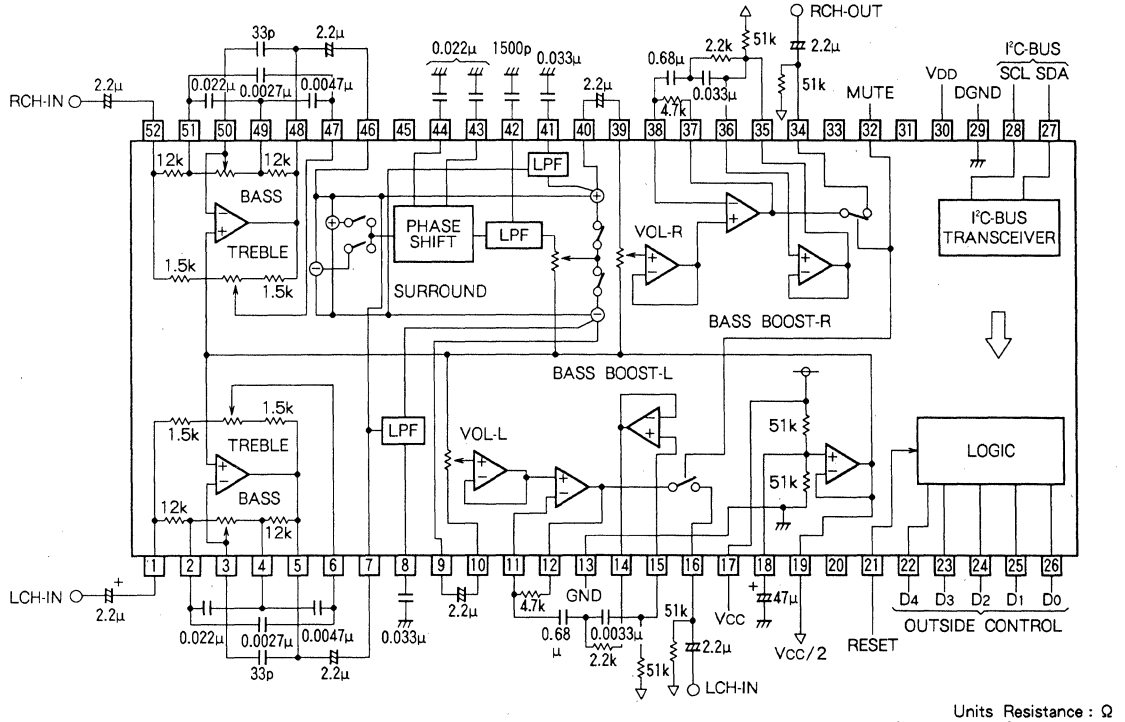
PIN CONFIGURATION



Outline 52P4B

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



Units Resistance : Ω
Capacitance : F

MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin No.	Symbol	Function
① ㊷	IN1 IN2	Tone input terminal
② ③ ④ ⑥	TONE1 FILTER	Connected with capacitor to compose a high/low range band-pass filter
㊶ ㊵ ㊴ ㊼	TONE2 FILTER	
⑤ ㊽	TONE1 OUT TONE2 OUT	Tone output terminal
⑪ ⑫ ⑭ ⑮	BASS BOOST1 FILTER	Connected with resistance and capacitor to compose a resonance circuit
㊸ ㊼ ㊻ ㊺	BASS BOOST2 FILTER	
⑯ ㉞	OUT1 OUT2	Volume, bass boost output terminal
⑦ ㊻	SURROUND1 IN SURROUND2 IN	Surround input terminal
⑧ ㊹ ㊸ ㊷ ㊶	SURROUND FILTER	Surround phase modulation terminal
⑨ ㊵	SURROUND1 OUT SURROUND2 OUT	Surround output terminal
⑩ ㊴	VOLUME1 IN VOLUME2 IN	Volume input terminal
⑰	Vcc	Analog system supply terminal
⑱	FILTER	1/2Vcc input terminal
⑲	Vcc/2	1/2Vcc output terminal
㉑	RESET	Reset terminal (High RESET)
㉒ ㉓ ㉔ ㉕ ㉖	D4 D3 D2 D1 D0	Outside control terminal that converts the serial data of I²C bus into patallel data, and outputs
㉗	SDA	Data signal input terminal
㉘	SCL	Clock signal input terminal
⑬	GND	Analog system GND terminal
㉙	GND	Digital system GND terminal
㉚	VDD	Digital system supply terminal
㉜	MUTE	Mute terminal (High→MUTE ON)

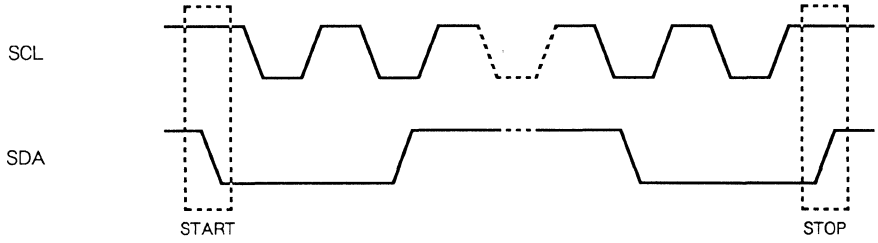
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	10	V
P_d	Power dissipation	1100	mW
K_θ	Thermal derating ($T_a \geqq 25$℃)	11	mW/℃
T_{opr}	Operating temperature	−20 ~ +75	℃
T_{stg}	Storage temperature	−55 ~ +125	℃

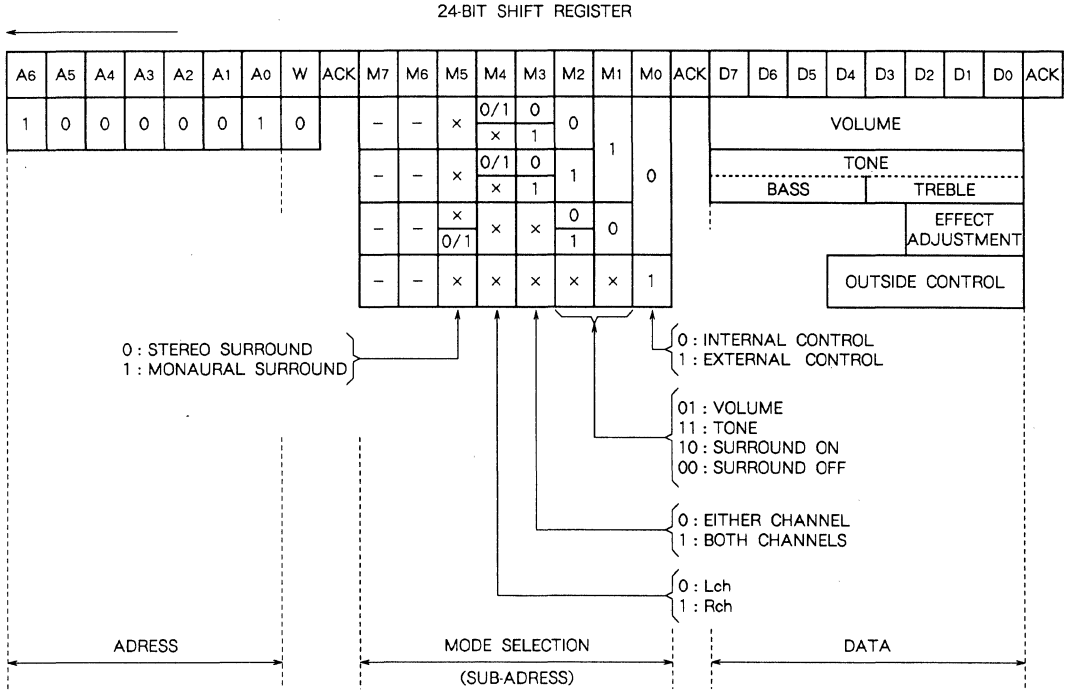
ELECTRICAL CHARACTERISTICS (V_{CC} = 9V, Ta = 25℃, unless otherwise noted)

Symbol		Parameter	Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC}		Circuit current		−	25	−	mA
A_{TT}	Volume	Maximum attenuation	$A_{TT} = -\infty$	−	−90	−80	dB
ΔA_{TT}	Volume	Attenuation error	A_{TT} = 0	−2.0	0	+2.0	dB
A_{TTS}	Volume	Step		−	1.0	−	dB/Step
$G_{(BASS)B}$	Bass/Treble	Bass boost	f=100Hz	9	12	15	dB
$G_{(BASS)C}$	Bass/Treble	Bass cut	f=100Hz	−15	−12	−9	dB
$G_{(TRE)B}$	Bass/Treble	Treble boost	f=10kHz	9	12	15	dB
$G_{(TRE)C}$	Bass/Treble	Treble cut	f=10kHz	−15	−12	−9	dB
G_S	Bass/Treble	Step		−	2.0	−	dB/Step
THD		Total harmonics distortion	f=1kHz, V_O = 0.5Vrms, A_{TT} = 0	−	0.005	0.1	%
V_{NO}		Output noise voltage	A_{TT} = 0, Rg = 0, DIN-AUDIO	−	10	30	μVrms
V_{OM}		Maximum output voltage	THD=1%	−	2.4	−	Vrms

RELATION BETWEEN DATA AND CLOCK



DATA FORMAT



VOLUME CODE

ATT1	D0	D1	D2	D3	D4
0dB	H	H	H	H	H
− 2dB	L	H	H	H	H
− 4dB	H	L	H	H	H
− 6dB	L	L	H	H	H
− 8dB	H	H	L	H	H
− 10dB	L	H	L	H	H
− 12dB	H	L	L	H	H
− 14dB	L	L	L	H	H
− 16dB	H	H	H	L	H
− 18dB	L	H	H	L	H
− 20dB	H	L	H	L	H
− 22dB	L	L	H	L	H
− 24dB	H	H	L	L	H
− 26dB	L	H	L	L	H
− 28dB	H	L	L	L	H
− 30dB	L	L	L	L	H
− 32dB	H	H	H	H	L
− 34dB	L	H	H	H	L
− 36dB	H	L	H	H	L
− 38dB	L	L	H	H	L
− 40dB	H	H	L	H	L
− 42dB	L	H	L	H	L
− 46dB	H	L	L	H	L
− 50dB	L	L	L	H	L
− 54dB	H	H	H	L	L
− 58dB	L	H	H	L	L
− 62dB	H	L	H	L	L
− 66dB	L	L	H	L	L
− 70dB	H	H	L	L	L
− 74dB	L	H	L	L	L
− 78dB	H	L	L	L	L
− ∞	L	L	L	L	L

ATT2	D5	D6
0dB	H	H
− 1dB	L	H
− 2dB	H	L
− 3dB	L	L

TONE CODE

BASS	D4	D5	D6	D7
TREBLE	D0	D1	D2	D3
12dB	H	H	H	H
10dB	L	H	H	H
8dB	H	L	H	H
6dB	L	L	H	H
4dB	H	H	L	H
2dB	L	H	L	H
0dB	H	L	L	H
− 2dB	L	L	L	H
− 4dB	H	H	H	L
− 6dB	L	H	H	L
− 8dB	H	L	H	L
− 10dB	L	L	H	L
− 12dB	H	H	L	L

EFFECT ADJUSTMENT CODE

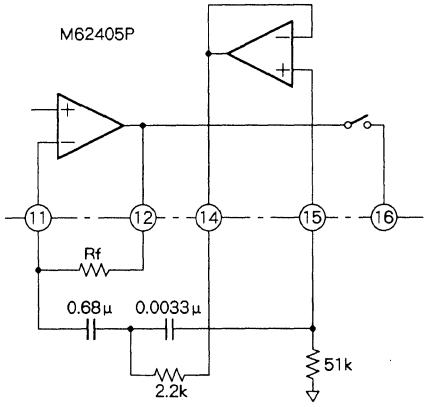
EFFECT	D0	D1	D2
0dB	H	H	H
− 1.5dB	L	H	H
− 3.0dB	H	L	H
− 4.5dB	L	L	H
− 6.0dB	H	H	L
− 7.5dB	L	H	L
− 9.0dB	H	L	L
− 10.5dB	L	L	L

NOTES FOR USE

Exterior bass boost constants

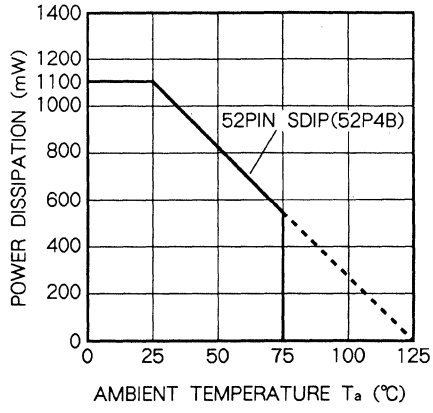
- Set resonance resistance R1 at 2.2k or higher, according to the capacity of resonance amplifier.
- Bass boost gain is 10dB max
- Where f = 100Hz, Gv = 10dB and Q = 1, the respective constant values are as follows :

C1 = 0.68 μ R1 = 2.2k
C2 = 0.033 μ R2 = 51k
Rf = 4.7k

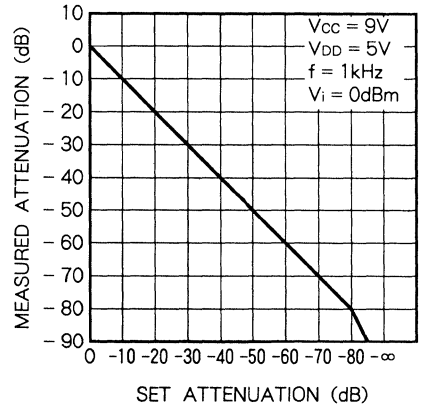


TYPICAL CHARACTERISTICS

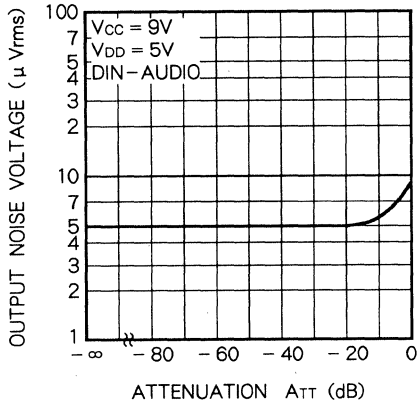
THERMAL DERATING



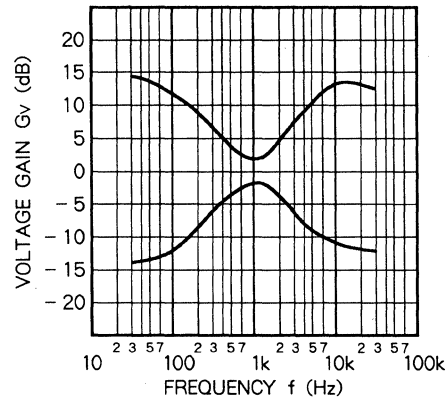
MEASURED ATTENUATION VS. SET ATTENUATION



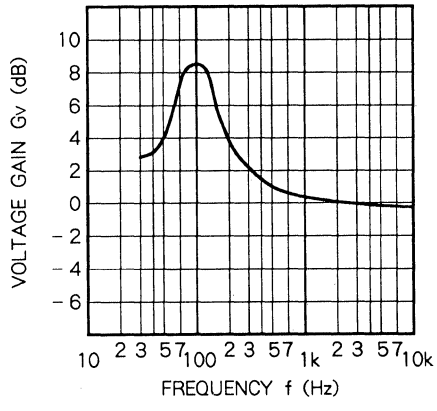
OUTPUT NOISE VOLTAGE VS. ATTENUATION



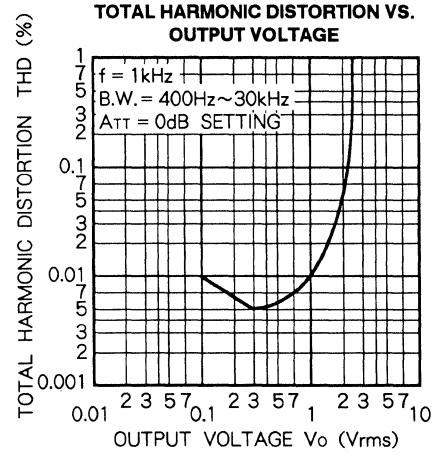
TONE FREQUENCY CHARACTERISTIC



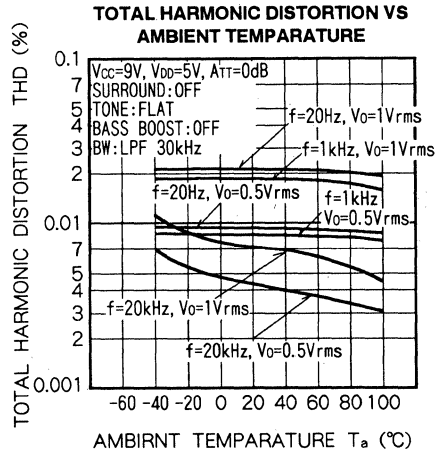
BASS BOOST VOLTAGE GAIN



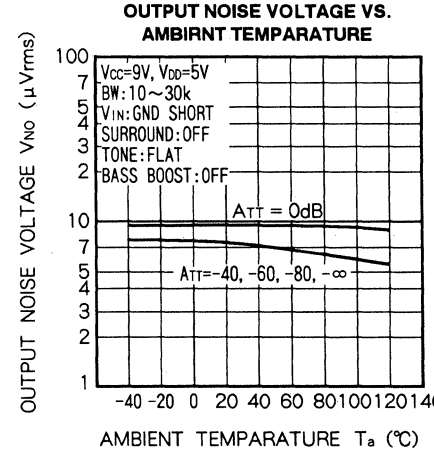
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



TOTAL HARMONIC DISTORTION VS AMBIENT TEMPARATURE



OUTPUT NOISE VOLTAGE VS. AMBIRNT TEMPARATURE



M62406FP

ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR 4 LOUDSPEAKER APPLICATIONS

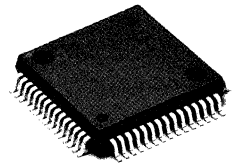
DESCRIPTION

The M62406FP is an IC developed for car audio systems. It contains master volume, loudness, 3-band tone, and fader volume controls. All these blocks are controlled by serial data. As the loudness gain is also variable by serial data, it is possible to set loudness characteristics separately from the value set to the master volume control.

The IC is suitable for use in home-use audio systems and TV sets, as well as in car audio systems.

FEATURES

- Controls sound volume (master and fader volume controls) and tone quality (bass, mid, treble, and loudness controls) at stage before power amplifier.
- Designed for analog voice signal processing.
- Uses serial data to control sound volume and tone quality.
- Full-CMOS IC realizing mixed analog and digital blocks.
- Maximum input voltage ····· 2.8Vrms (V_{CC} = 8V)
- Total harmonic distortion factor ····· 0.005 % (B_W = 400Hz~30kHz)
- Built-in reference voltage (1/2V_{CC}) for analog signals.



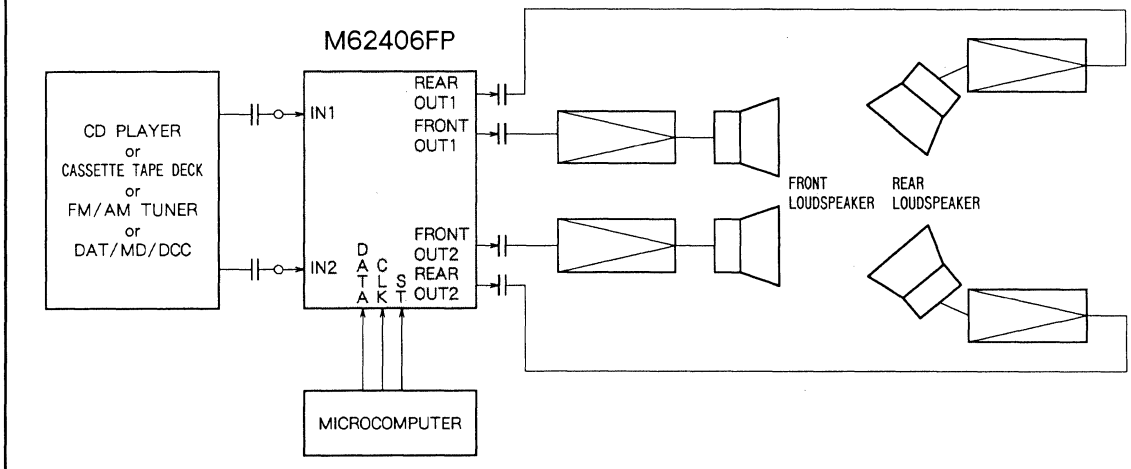
Outline 64P6N-A

0.8mm pitch QFP
(14.0mm × 14.0mm × 2.8mm)

RECOMMENDED OPERATING CONDITIONS

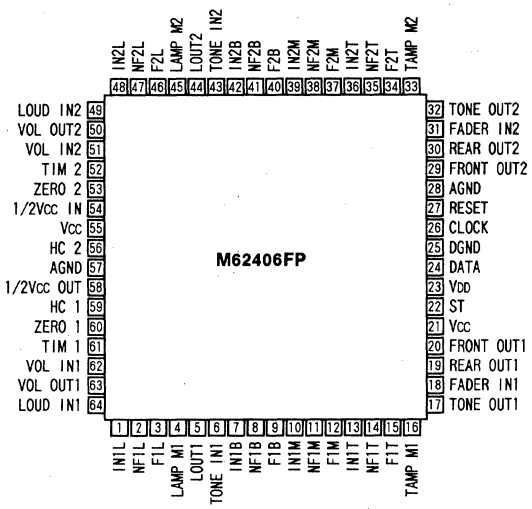
Supply voltage range ····· V_{CC} = 6~9V, V_{DD} = 4.5~5.5V
Rated supply voltage ····· V_{CC} = 8V, V_{DD} = 5V
Rated dissipation voltage ····· 800mW

SYSTEM CONFIGURATION



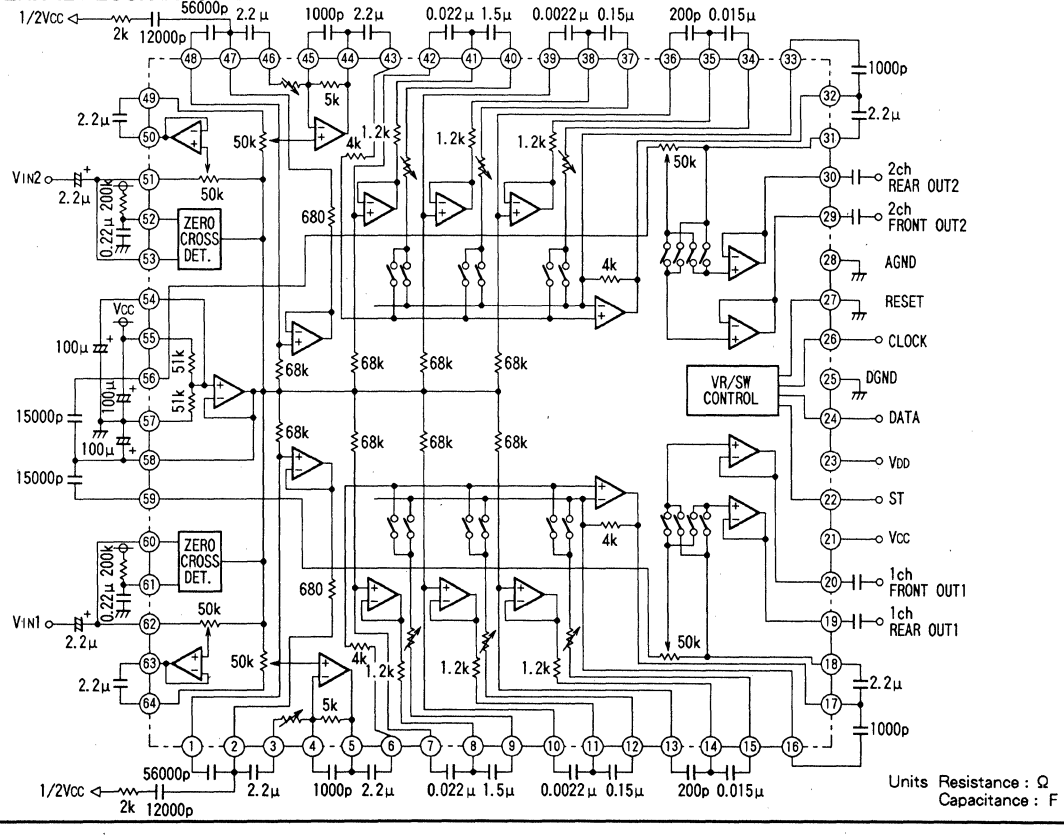
ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR 4 LOUDSPEAKER APPLICATIONS

PIN CONFIGURATION



Outline 64P6N-A

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR 4 LOUDSPEAKER APPLICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

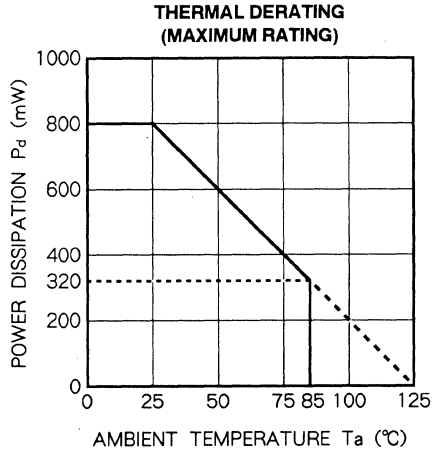
Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	10	V
P_d	Power dissipation	800	mW
K_θ	Thermal derating	8	mW/℃
T_{opr}	Operating temperature	− 30 ~ + 85	℃
T_{stg}	Storage temperature	− 40 ~ + 125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 8V, unless otherwise noted)

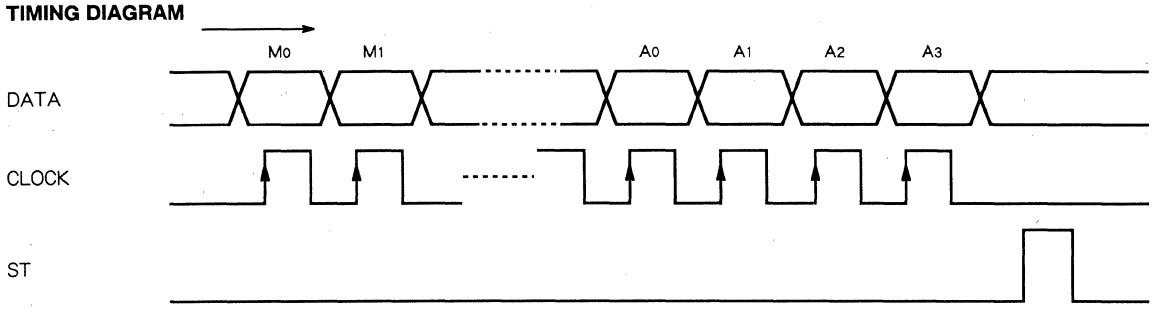
Symbol		Parameter	Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC}		Circuit current		−	35	−	mA
$A_{TT(VOL)}$	ATT	ATT. max	$A_{TT(VOL)}$ = − ∞	−	−90	−80	dB
$\Delta A_{TT(VOL)}$	ATT	ATT. error	$A_{TT(VOL)}$ = 0	−2.0	0	2.0	dB
$G_{(Loud)L}$	LOUDNESS	Voltage gain	V_{in} = 100mVrms, f = 70Hz	9	12	15	dB
$G_{(Loud)H}$	LOUDNESS	Voltage gain	V_{in} = 100mVrms, f = 10kHz	5.7	7.7	9.7	dB
V_{IM}	LOUDNESS	Maximun input voltage	THD=1%	2.0	2.8	−	Vrms
$G_{(BASS)B}$	BASS-MID-TREBLE	Bass boost	f = 100Hz	9	12	15	dB
$G_{(BASS)C}$	BASS-MID-TREBLE	Bass cut	f = 100Hz	−15	−12	−9	dB
$G_{(MID)B}$	BASS-MID-TREBLE	MID boost	f = 1kHz	9	12	15	dB
$G_{(MID)C}$	BASS-MID-TREBLE	MID cut	f = 1kHz	−15	−12	−9	dB
$G_{(TRE)B}$	BASS-MID-TREBLE	Treble boost	f = 10kHz	9	12	15	dB
$G_{(TRE)C}$	BASS-MID-TREBLE	Treble cut	f = 10kHz	−15	−12	−9	dB
$A_{TT(FED)}$	FADER	ATT. max	$A_{TT(FED)}$ = ∞	−	−90	−74	dB
V_{OM}	FADER	Maximum output voltage	THD=1%	1.8	2.2	−	Vrms
THD		Total harmonic distortion	f=1kHz, Vo = 0.5Vrms, loudness = off, $A_{TT(VOL)}$ = 0, $A_{TT(FED)}$ = 0	−	0.003	0.05	%
V_{NO1}		Output noise voltage	$A_{TT(VOL)}$ = 0, $A_{TT(FED)}$ = 0, R_g = 0, BW : 10Hz~20kHz	−	7	15	μVrms
V_{NO2}		Output noise voltage	$A_{TT(VOL)}$ = − ∞, $A_{TT(FED)}$ = − ∞, R_g = 0, BW : 10Hz~20kHz	−	4	8	μVrms
CS		Channel separation	f=1kHz	−	−90	−80	dB

※ For Loudness characteristics and Bass-Treble characteristics, don't consider outside C, R error.

TYPICAL CHARACTERISTICS



TIMING DIAGRAM



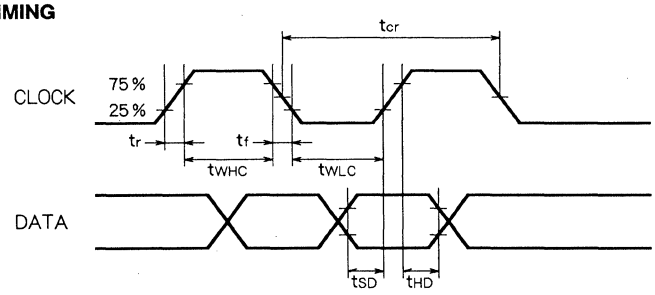
DIGITAL PART DC CHARACTERISTICS (Ta = −30~85℃, V_{CC} = 8V, V_{DD} = 5V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IL}	low-level input voltage	DATA, CLOCK, ST		0	~	0.2V_{DD}	V
V_{IH}	High-level input voltage			0.8V_{DD}	~	V_{DD}	V
I_{IL}	low-level input current	V_I = 0	DATA, CLOCK, ST	−10	−	10	μA
I_{IH}	High-level input current	V_I = V_{DD}		−	−	10	

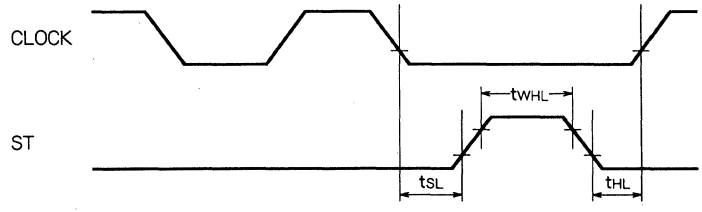
DIGITAL PART AC CHARACTERISTICS (Ta = 30~85℃, V_{CC} = 8V, V_{DD} = 5V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{cr}	CLOCK	Cycle time		2	−	−	μs
t_{WHC}		Pulse width ("H"level)		0.8	−	−	μs
t_{WLC}		Pulse width ("L"level)		0.8	−	−	μs
t_r		Raise time		−	−	0.2	μs
t_f		Fall time		−	−	0.2	μs
t_{SD}	DATA	Set up time		0.4	−	−	μs
t_{HD}		Hold time		0.4	−	−	μs
t_{SL}	ST	Set up time		0.8	−	−	μs
t_{HL}		Hold time		1	−	−	μs
t_{WHL}		Pulse width		0.8	−	−	μs

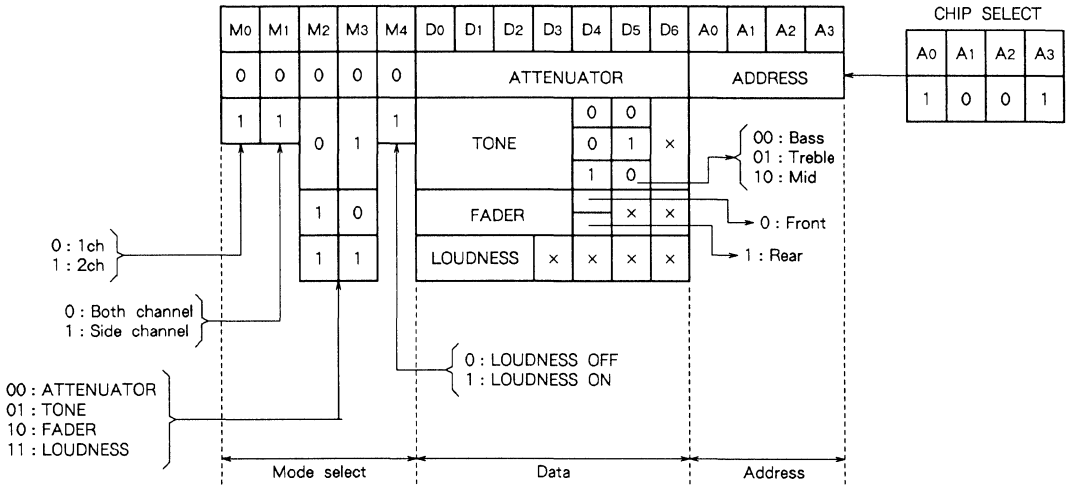
CLOCK, DATA TIMING



ST TIMING



DATA FORMAT



ATTENUATOR CODE

ATT1	D0	D1	D2	D3	D4
0dB	H	H	H	H	H
− 2dB	L	H	H	H	H
− 4dB	H	L	H	H	H
− 6dB	L	L	H	H	H
− 8dB	H	H	L	H	H
− 10dB	L	H	L	H	H
− 12dB	H	L	L	H	H
− 14dB	L	L	L	H	H
− 16dB	H	H	H	L	H
− 18dB	L	H	H	L	H
− 20dB	H	L	H	L	H
− 22dB	L	L	H	L	H
− 24dB	H	H	L	L	H
− 26dB	L	H	L	L	H
− 28dB	H	L	L	L	H
− 30dB	L	L	L	L	H
− 32dB	H	H	H	H	L
− 34dB	L	H	H	H	L
− 36dB	H	L	H	H	L
− 38dB	L	L	H	H	L
− 40dB	H	H	L	H	L
− 42dB	L	H	L	H	L
− 46dB	H	L	L	H	L
− 50dB	L	L	L	H	L
− 54dB	H	H	H	L	L
− 58dB	L	H	H	L	L
− 62dB	H	L	H	L	L
− 66dB	L	L	H	L	L
− 70dB	H	H	L	L	L
− 74dB	L	H	L	L	L
− 78dB	H	L	L	L	L
∞	L	L	L	L	L

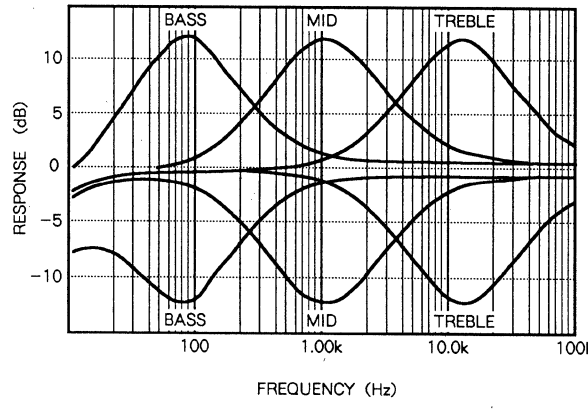
ATT2	D5	D6
0dB	H	H
− 1dB	L	H
− 2dB	H	L
− 3dB	L	L

ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR 4 LOUDSPEAKER APPLICATIONS

TONE CODE

TONE	D_0	D_1	D_2	D_3
12dB	L	H	H	L
10dB	H	L	H	L
8dB	L	L	H	L
6dB	H	H	L	L
4dB	L	H	L	L
2dB	H	L	L	L
0dB	L	L	L	L
0dB	L	L	L	H
− 2dB	H	L	L	H
− 4dB	L	H	L	H
− 6dB	H	H	L	H
− 8dB	L	L	H	H
− 10dB	H	L	H	H
− 12dB	L	H	H	H

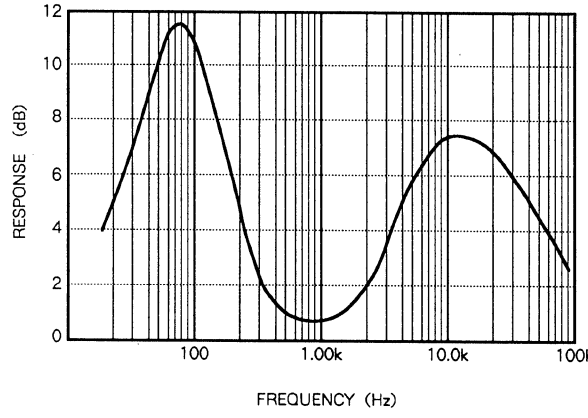
FREQUENCY RESPONSE (TONE)



FADER CODE

FADER	D_0	D_1	D_2	D_3
0dB	H	H	H	H
− 1dB	L	H	H	H
− 2dB	H	L	H	H
− 3dB	L	L	H	H
− 4dB	H	H	L	H
− 6dB	L	H	L	H
− 8dB	H	L	L	H
− 10dB	L	L	L	H
− 12dB	H	H	H	L
− 14dB	L	H	H	L
− 16dB	H	L	H	L
− 20dB	L	L	H	L
− 30dB	H	H	L	L
− 45dB	L	H	L	L
− 60dB	H	L	L	L
− ∞ dB	L	L	L	L

FREQUENCY RESPONSE (LOUDNESS)

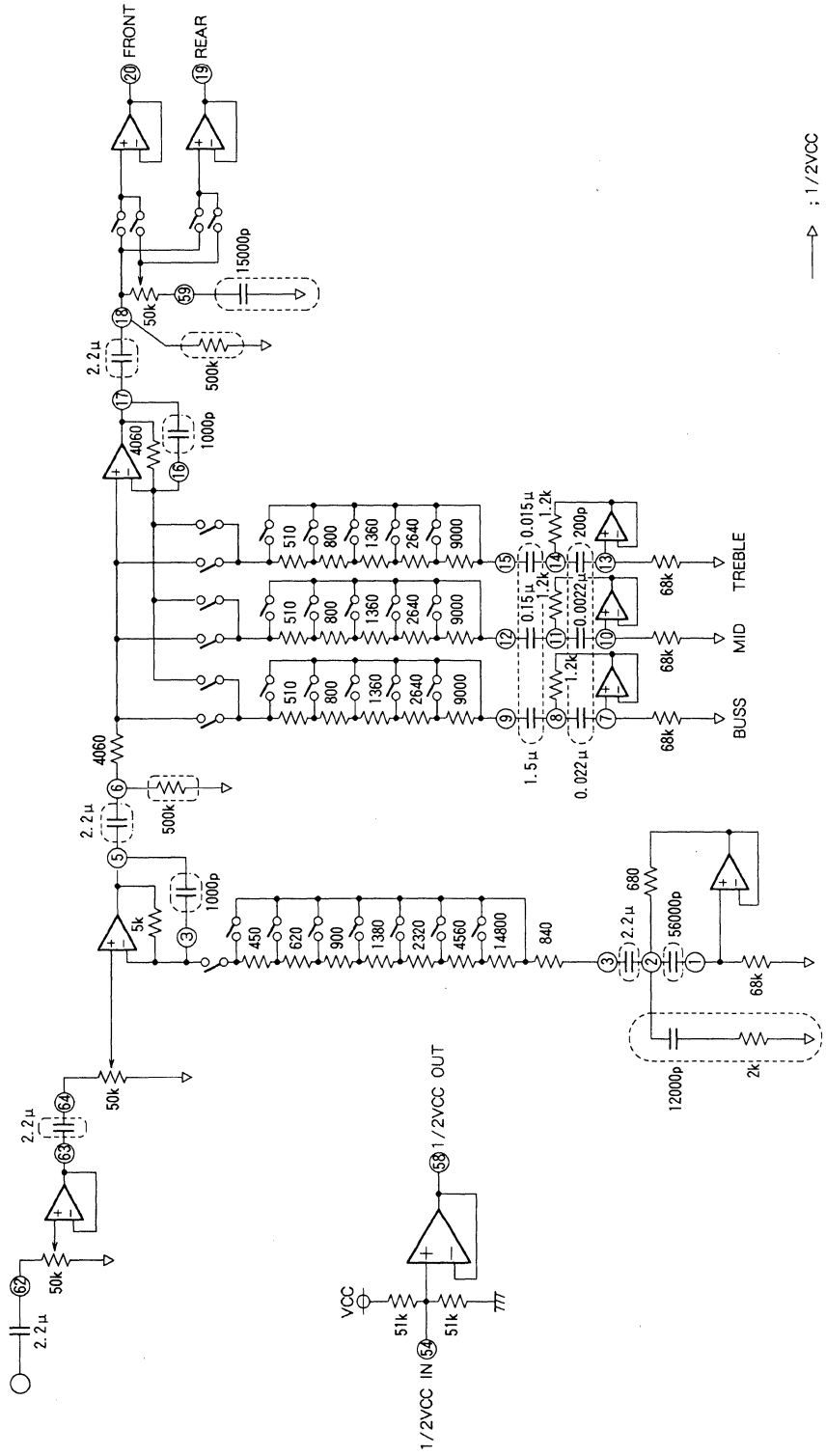


LOUDNESS CODE

LOUDNESS		D_0	D_1	D_2
f = 70Hz	f = 10kHz			
12dB	7.8dB	H	H	H
10.5dB	7.2dB	L	H	H
9dB	6.5dB	H	L	H
7.5dB	5.7dB	L	L	H
6dB	4.8dB	H	H	L
4.5dB	3.7dB	L	H	L
3dB	2.6dB	H	L	L
1.5dB	1.3dB	L	L	L

M62406FP EQUIVALENT CIRCUIRT

(1ch SIDE)



M62408FP

SERIAL DATA CONTROLLED WITH SURROUND 5-ELEMENT GRAPHIC EQUALIZER

DESCRIPTION

The M62408FP sound controller is suitable for use in home audio systems. It has a built-in 5-element graphic equalizer, master volume control and 2 channels of surround muting circuits. All these blocks are controlled by serial data.

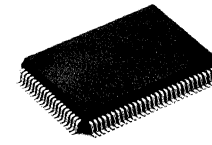
This sound controller is used to process small analog signals in the power amplifier front stage.

FEATURES

- Volume is adjusted by master volume control, sound quality by graphic equalizer and bass boost circuit, and sound field by surround control. All these adjustments are conducted in the power amplifier front stage.
- Processes analog sound signals
- Uses serial data to controls volume, sound quality and souns field.
- Switching noise is reduced by zero cross detection circuit.

Features :

- Maximum output voltage
  ····· 3.5Vrms(V_{CC} = ± 7V, THD = 1 %)
- Total harmonic distortion :
  ·····0.005 %(B.W = 400Hz~30kHz)



Outline 100P6S-A

0.65mm pitch QFP
(20.0mm × 14.0mm × 2.8mm)

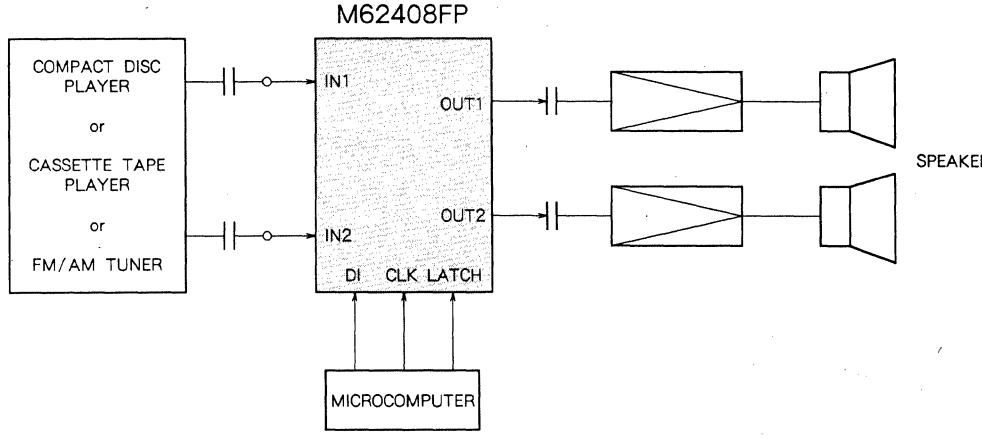
RECOMMENDED OPERATING CONDITIONS

Supply voltage range
·····V_{CC}, V_{EE} = ± 6.5~± 7.5V, V_{DD} = 4~6V

Rated supply voltage····· V_{CC}, V_{EE} = ± 7V, V_{DD} = 5V

Rated power dissipation ·····2300mW

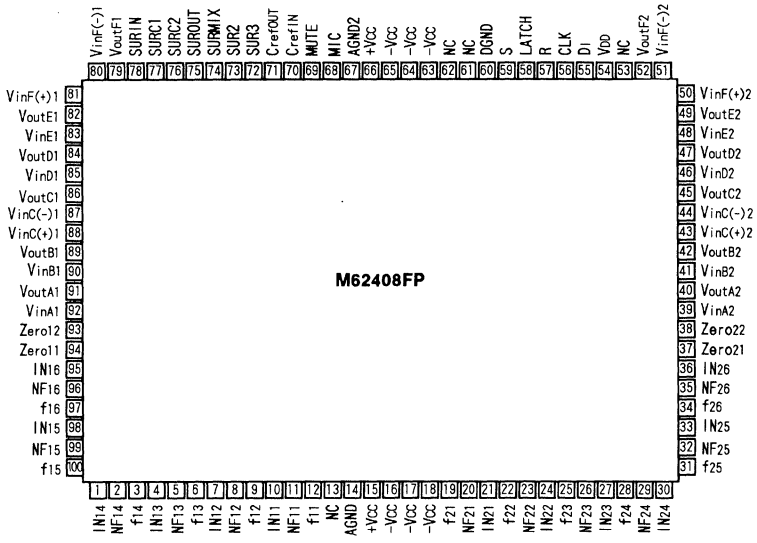
SYSTEM CONFIGURATION



M62408FP

SERIAL DATA CONTROLLED WITH SURROUND 5-ELEMENT GRAPHIC EQUALIZER

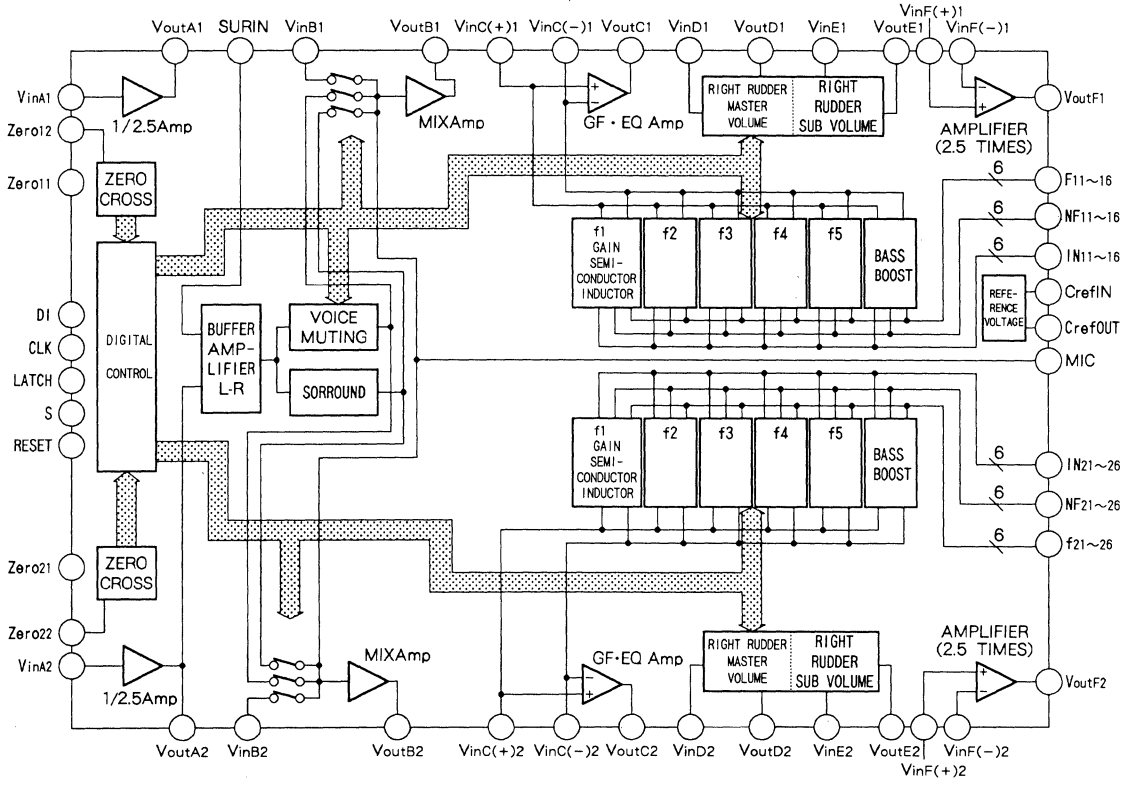
PIN CONFIGURATION



Outline 100P6S-A

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Name	Function
①, ④, ⑦, ⑩, ㉑, ㉔, ㉗, ㉚, ㉝, ㊱, ㊴, ㊽	IN	Adjacent IN pin and NF pin are connected to form band-pass filter
②, ⑤, ⑧, ⑪, ⑳, ㉓, ㉖, ㉙, ㉜, ㉟, ㊲, ㊾	NF	
③, ⑥, ⑨, ⑫, ⑲, ㉒, ㉕, ㉘, ㉛, ㊿	f	Graphic equalizer resonance impedance(band-pass filter) connection pins
㊼	f_{16}	Bus boost resonance impedance (band-pass filter) connection pins
㉞	f_{26}	
㊹	$Zero_{11}$	Used to set timer Relationship between external capacitance (C), resistance (R) and time (T) is $T = 1.2 \cdot C \cdot R(sec)$
㊲	$Zero_{21}$	
㉝	$Zero_{12}$	Detect zero cross Signals are input via capacitor
㊳	$Zero_{22}$	
㊷	V_{inA1}	Amplifier (1/2.5 ; −) input pins
㊴	V_{inA2}	
㊶	V_{outA1}	Amplifier (1/2.5) output pins
㊵	V_{outA2}	
㊵	V_{inB1}	Mix buffer amplifier input pins
㊶	V_{inB2}	
㊾	V_{outB1}	Mix buffer amplifier output pins
㊷	V_{outB2}	
㊽	$V_{inC(+)1}$	Graphic equalizer amplifier (+) input pins
㊸	$V_{inC(+)2}$	
㊼	$V_{inC(-)1}$	Graphic equalizer amplifier (−) input pins
㊹	$V_{inC(-)2}$	
㊻	V_{outC1}	Graphic equalizer amplifier output pins
㊺	V_{outC2}	
㊺	V_{inD1}	Master volume ATT1 input pins
㊻	V_{outD2}	

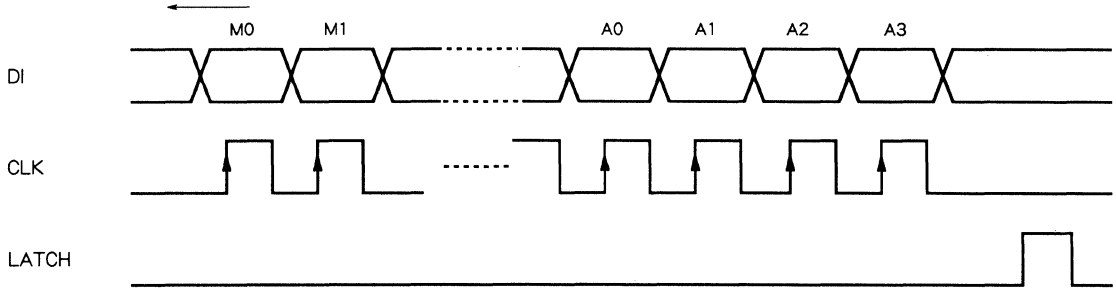
Pin No.	Name	Function
㊹	V_{outD1}	Master volume ATT1 output pins
㊼	V_{outD2}	
㊸	V_{inE1}	Sub volume ATT2 input pins
㊽	V_{inE2}	
㊷	V_{outE1}	Sub volume ATT2 output pins
㊾	V_{outE2}	
㊶	$V_{inF(+)1}$	Amplifier (2.5 times ; +) input pins
㊿	$V_{inF(+)2}$	
㊵	$V_{inF(-)1}$	Amplifier (2.5 times ; −) input pins
㊶	$V_{inF(-)2}$	
㊴	V_{outF1}	Amplifier (2.5 times) output pins
㊲	V_{outF2}	
㊸	SURIN	Sorround input pin
㊼	SURC1	Sorround phase modulating pins
㊸	SURC2	
㊵	SUROUT	Sorround output pin
㊹	SURMIX	Sorround signal mix amplifier input pins
㊳	SUR2	Sorround sound volume setting pins
㊲	SUR3	
㊶	C_{refOUT}	1/2-V_{CC} buffer amplifier output pin
㊵	C_{refIN}	1/2-V_{CC} buffer amplifier input pin
㊾	MUTE	Mute delay time setting pin
㊽	MIC	Microphone signal input pin
⑮, ㊻	+ V_{CC}	Analog system plus side power supply pin
⑯, ⑰, ⑱, ㊸, ㊹, ㊺	− V_{CC}	Analog system minus side power supply pin
㊹	V_{DD}	Digital system power supply pin
㊺	DI	Data signal input pin
㊻	CLK	Clock signal input pin
㊼	R	Reset pin (Low RESET)
㊽	LATCH	Latch signal input pin
㊾	S	Chip select pin
㊿	DGND	Digital system GND pin
⑭, ㊼	AGND	Analog system GND pin

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	± 8 (16)	V
P_d	Power dissipation	2300(Note 1)	mW
K_θ	Thermal derating ($T_a \geqq 25$℃)	23(Note 1)	mW/℃
T_{opr}	Operation temperature	−20～+ 75	℃
T_{stg}	Storage temperature	−40～+125	℃

Note 1. Copper foil 49mm² is added.

RELATIONSHIP BETWEEN DATA AND CLOCK PULSE



DIGITAL SECTION DIRECT CURRENT CHARACTERISTICS (V_{CC} = ± 7V, V_{DD} = 5V, Ta = −20～75℃)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IL}	Input voltage ("L" level)	DI, CLK, LATCH, RESET and S pins		0	～	0.2V_{DD}	V
V_{IH}	Input voltage ("H" level)			0.8V_{DD}	～	V_{DD}	V
I_{IL}	Input current ("L" level)	V_I = 0	DI, CLK, LATCH, RESET and S pins	−10	−	10	μA
I_{IH}	Output voltag ("H" level)	V_I = V_{DD}		−	−	10	μA

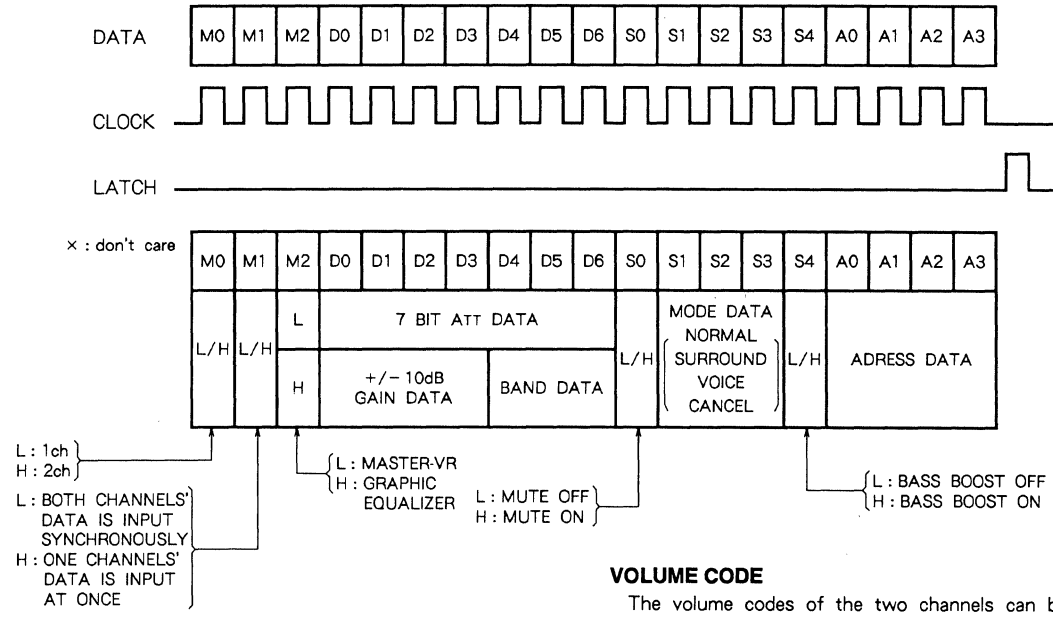
ELECTRICAL CHARACTERISTICS (V_{CC} = 8V, Ta = 25℃, unless otherwise noted)

Block name	Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
Graphic equalizer	G_{V10}	Graphic equalizer voltage gain	±10dB; f = 1kHz, V_O = 1Vrms, ※All resonance circuits are set to f = 1kHz	±9	±10	±11.5	dB
	G_{V8}		±8dB	±7	±8	±9.5	dB
	G_{V6}		±6dB	±5	±6	±7.5	dB
	G_{V4}		±4dB	±3	±4	±5.5	dB
	G_{V2}		±2dB	±1	±2	±3	dB
	G_{V0}		0dB	−1	0	+1	dB
	V_{OM1}	Maximum output voltage	THD = 1%, f = 1kHz, ALL Flat	1.6	2.0	−	Vrms
	THD1	Total harmonics distortion	V_O = 1Vrms, f = 1kHz, ALL Flat	−	0.005	0.05	%
Electronic volume section	A_{TTM}	Minimum attenuation	(Master VR A_{TT} = −∞) f = 1kHz	−	−90	−80	dB
	A_{TT}	Attenuation error	(Master VR A_{TT} = 0) f = 1kHz	−1.0	0	+1.0	dB
	Δ A_{TT}	Attenuation error between channels	(Master VR A_{TT} = 0) f = 1kHz, THD = 1%	−1.0	0	+1.0	dB
	V_{OM2}	Maximum output voltage	(Master VR A_{TT} = 0) f = 1kHz, THD = 1%	1.0	1.4	−	Vrms
	V_{IM}	Maximum input voltage	(Master VR A_{TT} = 0) f = 1kHz, THD = 1%	1.0	1.4	−	Vrms
	THD2	Total harmonic distortion	(Master VR A_{TT} = 0) f = 1kHz, V_O = 1Vrms, ALL Flat	−	0.005	0.05	%
General	V_{IM2}	Maximum input voltage	A_{TT} = 0, f = 1kHz, Flat, THD = 1%	3.0	3.5	−	Vrms
	V_{IM3}		A_{TT} = 0, f = 1kHz BOOST (one element), THD = 1%	0.8	1.0	−	Vrms
	V_{OM3}	Maximum output voltage	A_{TT} = 0, f = 1kHz, Flat, THD = 1%	3.0	3.5	−	Vrms
	V_{OM4}		A_{TT} = 0, f = 1kHz BOOST (one element), THD = 1%	3.0	3.5	−	Vrms
	I_{OM}	Maximum output current		−	±10	−	mA
	CS	Channel separation	f = 1kHz, MIC pin : V_{COM} and short circuit, V_{in} = +10dBm	−	−70	−60	dB
	Mute	Muting	V_{in} = +10dBm	−	−80	−70	dB
	V_{NO1}	Output noise current	A_{TT} = −∞, IHF-A	−	5	15	μVrms
	V_{NO2}		ATT = 0, Normal mode, GF・EQ : Flat, IHF-A	−	−	30	μVrms
	I_{CC}	Circuit current	V_{in} = 0	20	45	66	mA
	I_{DD}		V_{in} = 0	1	2	3.3	mA

M62408FP

SERIAL DATA CONTROLLED WITH SURROUND 5-ELEMENT GRAPHIC EQUALIZER

DIGITAL DATA INPUT SIGNAL FORMAT



MODE SELECTION (S1~S3)

Mode	S1	S2	S3
Normal	L	L	L
Surround 1	L	L	H
Surround 2	H	L	H
Surround 3	L	H	H
Voice cancel	H	H	H

IC SELECTION (A_0~A_3)

Code bits A_0~A_3 are used to select IC

S pin	A_0	A_1	A_2	A_3
High level	H	H	L	H
Low level	H	L	L	H

Note1. Bit A_1 is used to select data when 2 chips are used.

VOLUME CODE

The volume codes of the two channels can be set independently of each other within a range of 0dB ~ −83dB (adjustable by the unit of 1dB) as well as to −∞. Data can be simultaneously set to the channels.

ATT_1	D_2	D_3	D_4	D_5	D_6
0dB	H	H	H	H	H
− 2dB	L	H	H	H	H
− 4dB	H	L	H	H	H
− 6dB	L	L	H	H	H
− 8dB	H	H	L	H	H
− 10dB	L	H	L	H	H
− 12dB	H	L	L	H	H
− 14dB	L	L	L	H	H
− 16dB	H	H	H	L	H
− 18dB	L	H	H	L	H
− 20dB	H	L	H	L	H
− 22dB	L	L	H	L	H
− 24dB	H	H	L	L	H
− 26dB	L	H	L	L	H
− 28dB	H	L	L	L	H
− 30dB	L	L	L	L	H
− 32dB	H	H	H	H	L
− 34dB	L	H	H	H	L
− 36dB	H	L	H	H	L
− 38dB	L	L	H	H	L
− 40dB	H	H	L	H	L
− 44dB	L	H	L	H	L
− 48dB	H	L	L	H	L
− 52dB	L	L	L	H	L
− 56dB	H	H	H	L	L
− 60dB	L	H	H	L	L
− 64dB	H	L	H	L	L
− 68dB	L	L	H	L	L
− 72dB	H	H	L	L	L
− 76dB	L	H	L	L	L
− 80dB	H	L	L	L	L
−∞dB	L	L	L	L	L

ATT_2	D_0	D_1
0dB	H	H
− 1dB	L	H
− 2dB	H	L
− 3dB	L	L

GRAPHIC EQUALIZER GAIN DATA

The graphic equalizer gain data of the two channels can be set independently of each other within a range of −10dB ~ +10dB(adjustable by the unit of 2dB). Data can be simultaneously set to both channels.

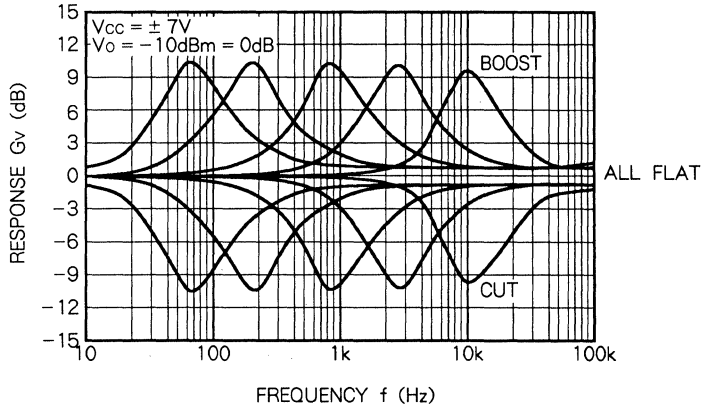
Gain \ Code	D_3	D_2	D_1	D_0
10dB	L	H	L	H
8dB	L	H	L	L
6dB	L	L	H	H
4dB	L	L	H	L
2dB	L	L	L	H
0dB	L	H	H	L
− 2dB	H	L	L	H
− 4dB	H	L	H	L
− 6dB	H	L	H	H
− 8dB	H	H	L	L
− 10dB	H	H	L	H

GRAPHIC EQUALIZER BAND DATA

Gain \ Code	D_6	D_5	D_4
f1	L	L	L
f2	L	L	H
f3	L	H	L
f4	L	H	H
f5	H	L	L

GRAPHIC EQUALIZER

FREQUENCY CHARACTERISTICS

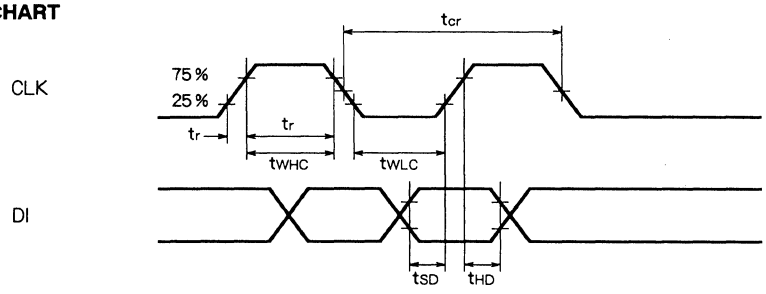


DIGITAL SECTION ALTERNATING CURRENT CHARACTERISTICS

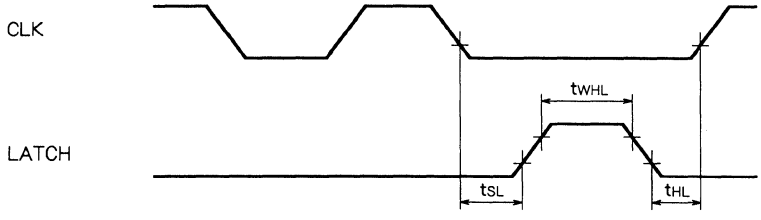
(V_{CC} = ± 7V, V_{DD} = 5V, Ta = −20~75℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t_{cr}	CLK cycle time	2	–	–	μs
t_{WHC}	CLK pulse width("H" level)	0.8	–	–	μs
t_{WLC}	CLK pulse width("L" level)	0.8	–	–	μs
t_r	CLK rise time	–	–	0.2	μs
t_f	CLK fall time				μs
t_{SD}	DI setup time	0.4	–	–	μs
t_{HD}	DI hold time	0.4	–	–	μs
t_{SL}	LATCH setup time	0.8	–	–	μs
t_{HL}	LATCH hold time	1	–	–	μs
t_{WHL}	LATCH "H" pulse width	0.8	–	–	μs
t_{HR}	RESET hold time	1	–	–	μs
t_{WLR}	RESET "L" pulse width	0.8	–	–	μs

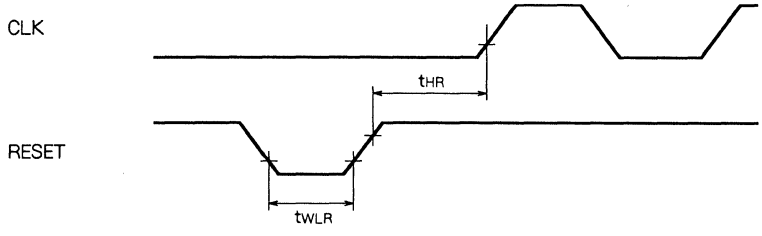
CLK, DI TIMING CHART



LATCH TIMING CHART



RESET TIMING CHART

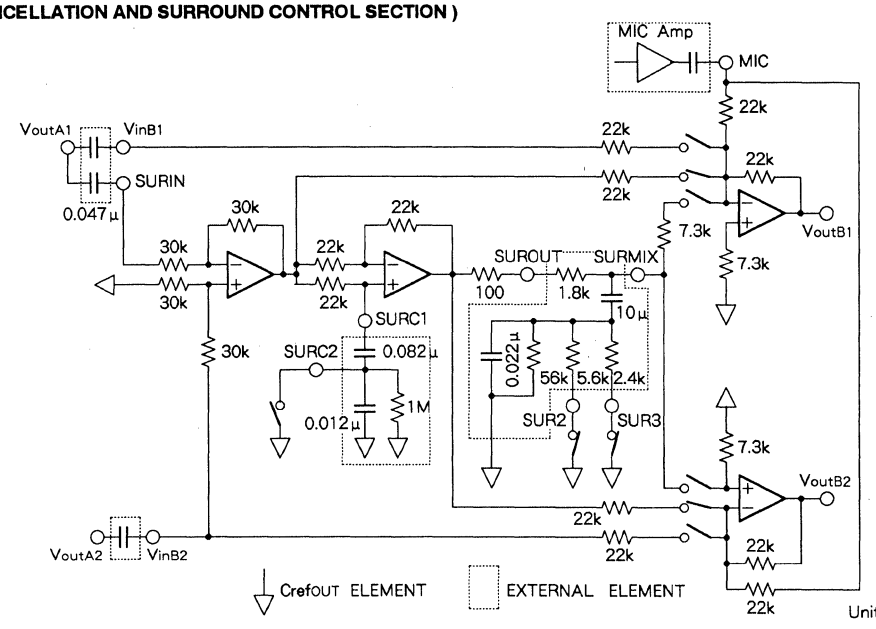


OPERATION

Voice cancellation and surround control function

The voice cancellation and surround sound control section consists of a differential amplifier, phase shifter and mixing amplifier as shown below :

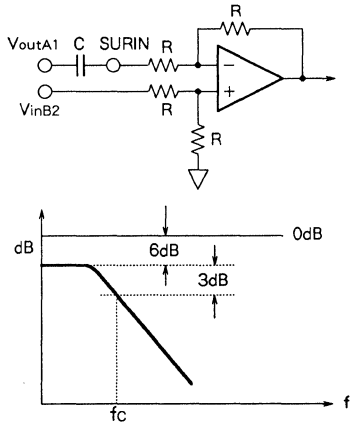
(VOICE CANCELLATION AND SURROUND CONTROL SECTION)



1-1. VOICE CANCEL

Voice output is canceled by removing channel 1/channel 2 in-phase signal components with differential amplifier. Not to remove low-pass component signals, the differential amplifier frequency characteristics are adjusted with external capacitance :

① In-phass input rejecting frequency setting

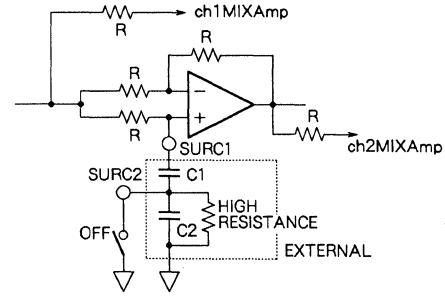


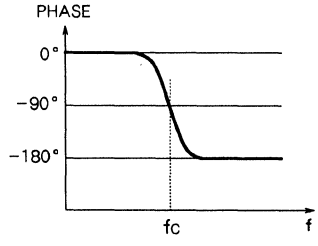
In-phass input rejecting frequency is set according to capacitance connected between VoutA1 pin and SURIN pin.

$$\text{Formura : } fc = \frac{1}{2\pi CR} \quad \text{(Built-in resistance : 30k}\Omega\text{)}$$

② Phase shifter frequency adjustment

Stereophonic playback can be simulated by inputting differential amplifier output signals to mixing amplifier. To channel 1, signals are input as they are, while the phase of those input to channel 2 is shifted 180 degrees by phase.





$$f_s = \frac{1}{2\pi CR}$$

(BUILT-IN RESISTANCE : 22kΩ)

$$C = \frac{C_1 \cdot C_2}{C_1 + C_2}$$

1-2. SURROUND CONTROL

As shown in the equivalent circuit diagram on 4-68, the circuit is simplified by using a single block for both surround control and voice cancellation.

Surround effects are obtained by (1) producing channel 1 /channel 2 differential signals with differential amplifier, (2) shifting the phase by 180 degrees with phase shifiter in the first stage, and (3) adding the differential signals to main signals with mixing amplifier.

The mixing ratio of surround sound signals to main signals can be selected at the user's option from among three levels (up to approx. 2 : 1). The mode can be selected by the mode selection function.

① Phase shifter frequency setting

The phase shifter frequency can be adjusted in the same way as when voice signals are to be canceled. Only capacitance C_1 is provided because the internal switch of pin $SURC_2$ comes on.

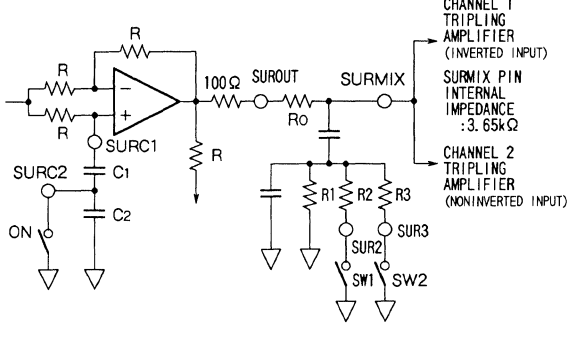
$$f_s = \frac{1}{2\pi C_1 R} \quad \text{(Built-in resistance : 22k Ω)}$$

② Mixing ratio adjustment for sorround effects

Surround sound effects are adjusted by setting SUROUT pin output to a correct level with resistance partial voltage and by applying the output to SURMIX pin.

The channel 1 output is added to the inverted input of mixing amplifier, while the channel 2 output is added to its noninverted input. The phase is adjusted to that of main signals.

Signals input to SURMIX pin are added after tripled by mixing amplifier.



Mode	SW1	SW2
SUR1 mode	OFF	OFF
SUR2 mode	ON	OFF
SUR3 mode	OFF	ON

Relationship between SUROUT pin output V_{SUROUT} (SUROUT pin open) and SURMIX pin input level V_{SURMIX} (external setting as described above) is expressed with the equation below :

(In the SUR1 mode :)

$$V_{SURMIX1} = \frac{(R_1 // 3.65k\,\Omega)}{(100\,\Omega + R_O) + (R_1 // 3.65k\,\Omega)} \cdot V_{SUROUT}$$

(In the SUR2 mode :)

$$V_{SURMIX2} = \frac{(R_1 // R_2 // 3.65k\,\Omega)}{(100\,\Omega + R_O) + (R_1 // R_2 // 3.65k\,\Omega)} \cdot V_{SUROUT}$$

(In the SUR3 mode :)

$$V_{SURMIX3} = \frac{(R_1 // R_3 // 3.65k\,\Omega)}{(100\,\Omega + R_O) + (R_1 // R_3 // 3.65k\,\Omega)} \cdot V_{SUROUT}$$

For example, when R_O = 1.8k Ω, R_1 = 56k Ω, R_2 = 5.6k Ω, R_3 = 2.4k Ω as shown on P12

$V_{SURMIX1} = 0.643V_{SUROUT}$

$V_{SURMIX2} = 0.528V_{SUROUT}$

$V_{SURMIX3} = 0.426V_{SUROUT}$

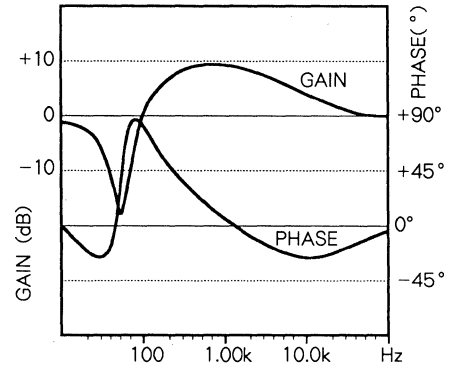
The signals are tripled by mix amplifier and output as follows :

Mode	SUR signal level	Mixing ratio to main signals
SUR1 mode	$1.929V_{SUROUT}$	1 : 1.929
SUR2 mode	$1.584V_{SUROUT}$	1 : 1.584
SUR3 mode	$1.278V_{SUROUT}$	1 : 1.278

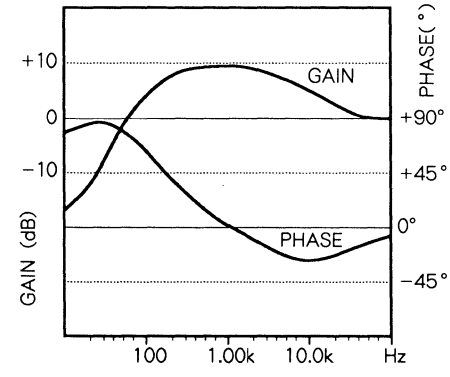
Note1. Load connected between SUROUT pin and CrefOUT pin should be at least 2.7kΩ.

Frequency characteristics in the SUR1 mode (Example)

● Channel 1 (V_{OUT}/V_{IN}-f ; no signals in the channel 2)

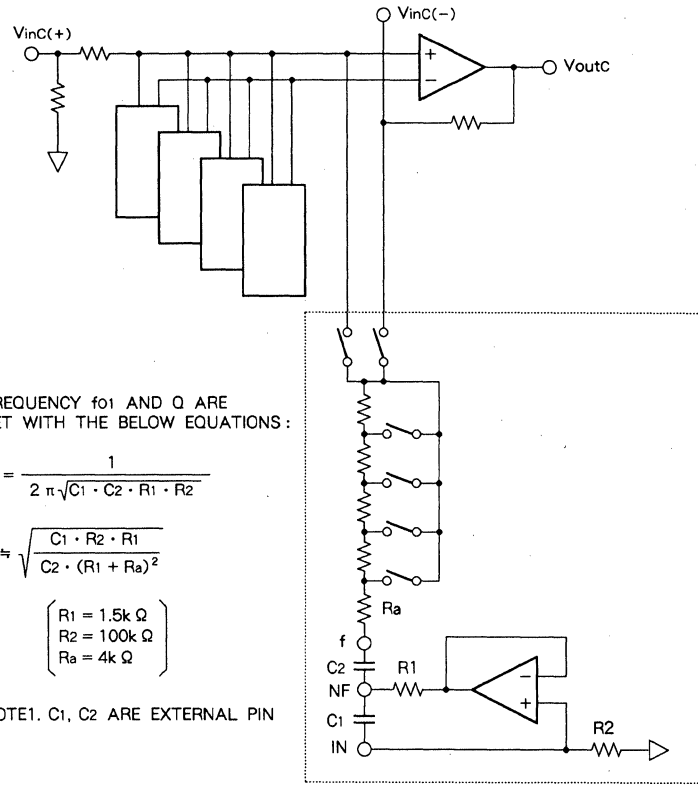


● Channel 2 (V_{OUT}/V_{IN}-f ; no signals in the channel 1)



GRAPHIC EQUALIZER

Graphic equalizer is designed such that the voltage of operational amplifier under resonation can be adjusted in a range between −10dB and +10dB by the unit of 2dB. This adjustment uses semiconductor inductor resonance circuits (5bands, 2 channel) and the switching of rudder resistance.



FREQUENCY f_{o1} AND Q ARE SET WITH THE BELOW EQUATIONS:

$$f_o = \frac{1}{2\pi\sqrt{C_1 \cdot C_2 \cdot R_1 \cdot R_2}}$$

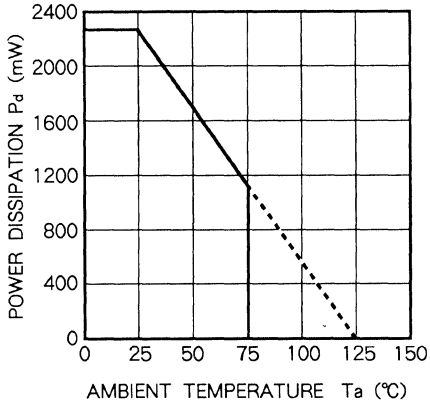
$$Q \fallingdotseq \sqrt{\frac{C_1 \cdot R_2 \cdot R_1}{C_2 \cdot (R_1 + R_a)^2}}$$

$R_1 = 1.5k\,\Omega$
$R_2 = 100k\,\Omega$
$R_a = 4k\,\Omega$

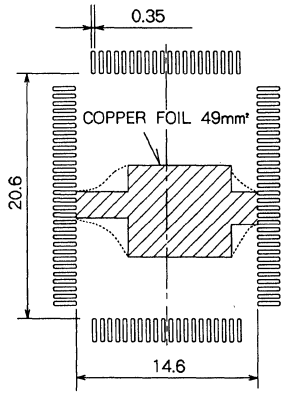
NOTE1. C_1, C_2 ARE EXTERNAL PIN

TYPICAL CHARACTERISTICS

THERMAL DERATING

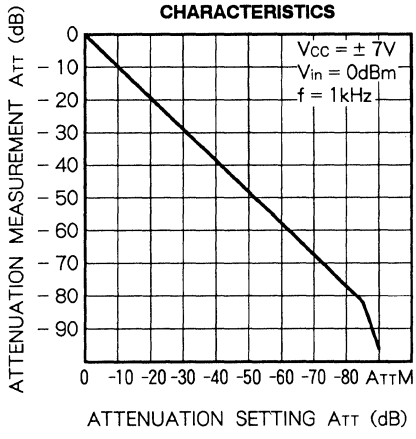


Unit : mm

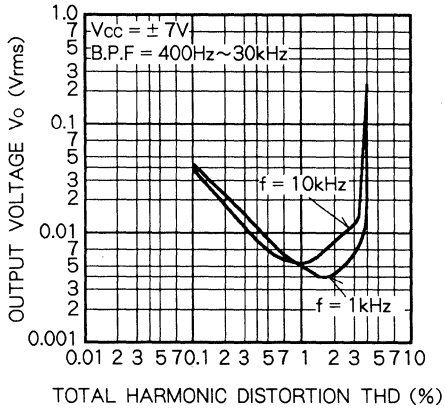


To ensure adequate radiation from integrated circuit, apply copper foil as widely as possible to −Vcc pin root.

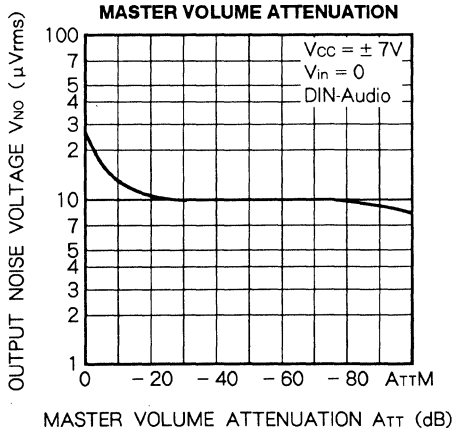
MASTER VOLUME ATTENUATION CHARACTERISTICS



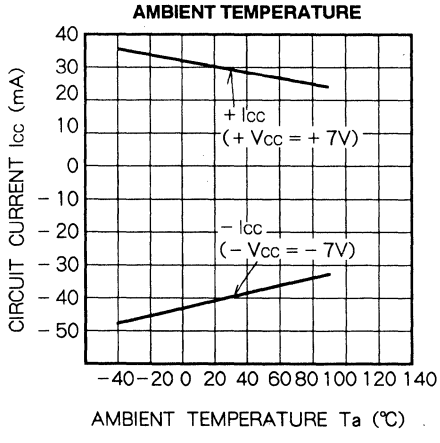
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



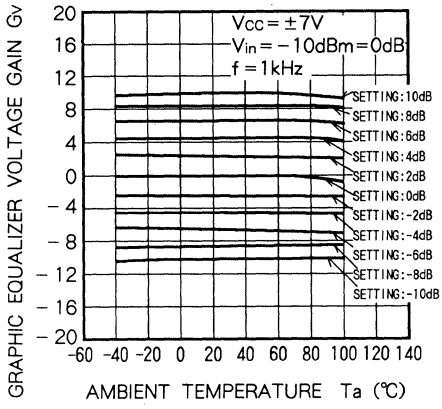
OUTPUT NOISE VOLTAGE VS. MASTER VOLUME ATTENUATION



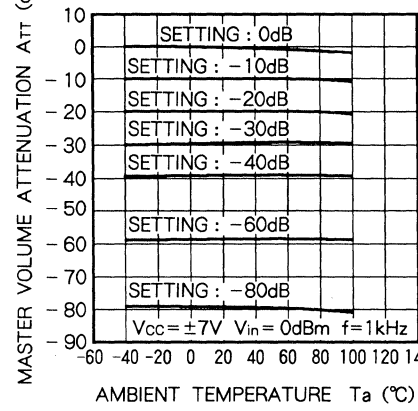
CIRCUIT CURRENT VS. AMBIENT TEMPERATURE



GRAPHIC EQUALIZER VOLTAGE GAIN VS. AMBIENT TEMPERATURE



MASTER VOLUME ATTENUATION VS. AMBIENT TEMPERATURE



M62409FP

SERIAL DATA CONTROLLED ELECTONIC VOLUME CONTROL

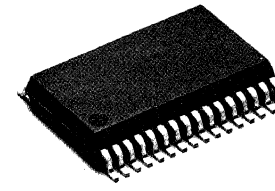
DESCRIPTION

The M62409FP is an electronic volume control employing ladder network resistors. The IC been developed for car audio systems and is controlled by serial data.

The IC is suitable for use in home-use audio systems and TV sets, as well as in car audio systems.

FEATURES

- Controls sound volume (master volume control) and tone quality (loudness control) at the stage before power amplifier.
- Designed for analog voice signal processing.
- Uses serial data to control sound volume and tone quality.
- Address code selector pin.
- Full-CMOS IC realizing mixed analog and digital blocks.
- Maximum input voltage ····· 2.8Vrms(V_{CC} = 8V)
- Total harmonic distortion factor ····· 0.003 %
  (B.W. = 400Hz~30kHz)
- Built-in reference voltage (1/2V_{CC}) for analog signals.



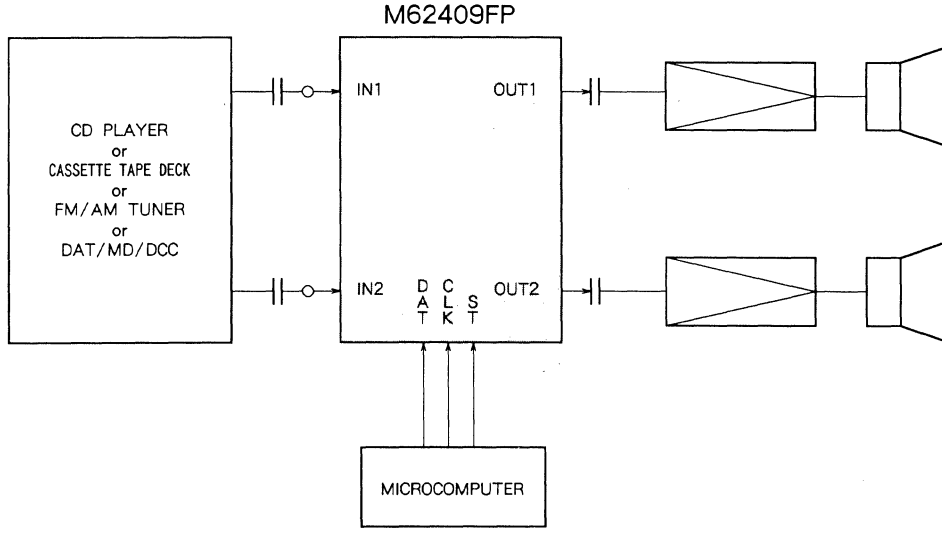
Outline 32P2U-B

0.8mm pitch 375mil SSOP
(7.5mm × 12.8mm × 2.3mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC} = 5~9V, V_{DD} = 4.5~5.5V
Rated supply voltage ····· V_{CC} = 8V, V_{DD} = 5V
Rated dissipation voltage ····· 790mW

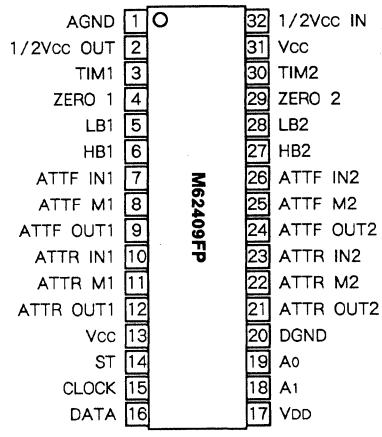
SYSTEM CONFIGURATION



M62409FP

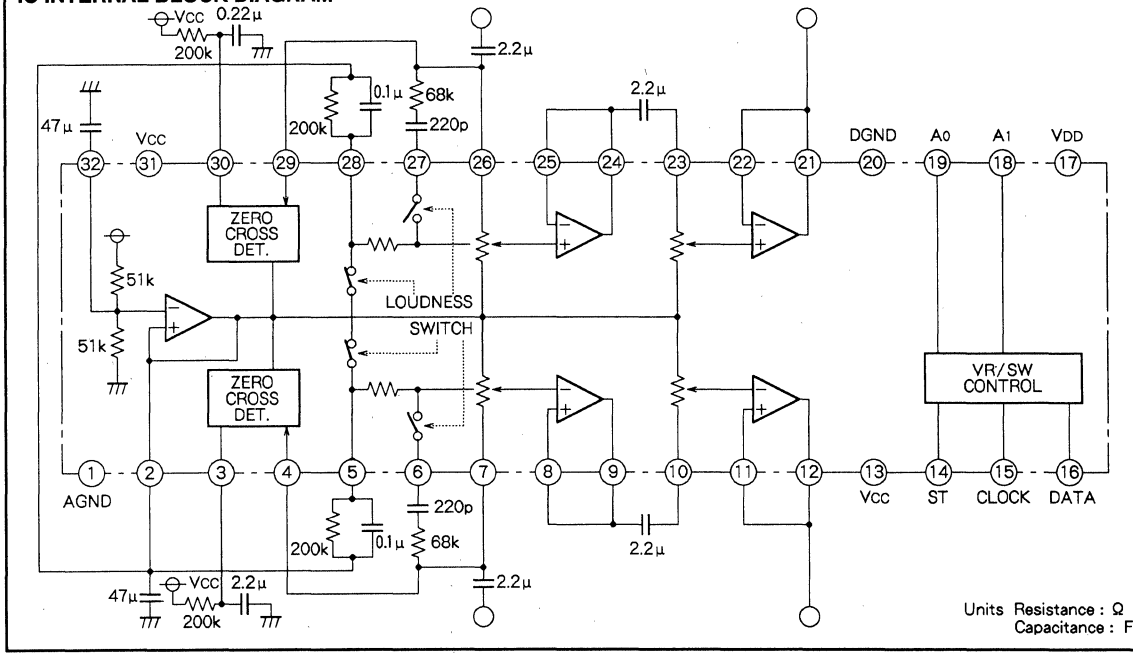
SERIAL DATA CONTROLLED ELECTONIC VOLUME CONTROL

PIN CONFIGURATION



Outline 32P2U-B

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

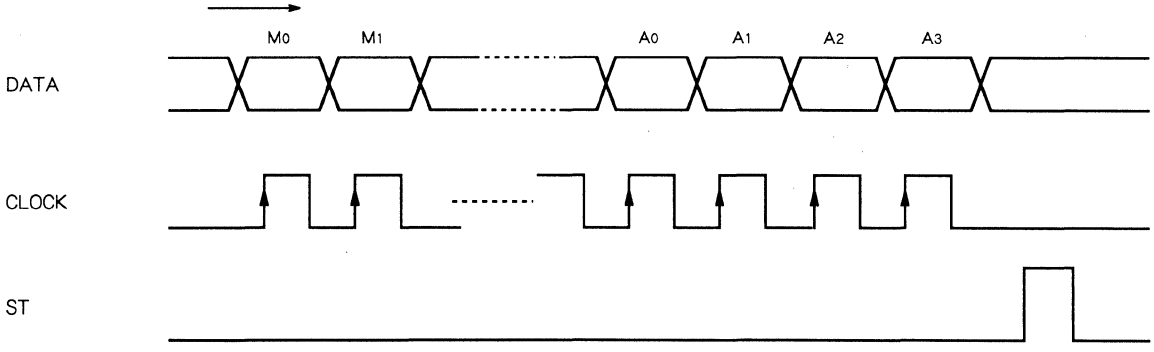
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	10	V
P_d	Power dissipation	790	mW
K_θ	Thermal derating	7.9	mW/℃
T_{opr}	Operating temperature	− 30 ~ + 85	℃
T_{stg}	Storage temperature	− 40 ~ + 125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 8V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC}	Circuit current			−	14	−	mA
$A_{TT(VOL)}$	ATT	ATT max.	$A_{TT(VOL)} = -\infty$	−	− 90	− 80	dB
$\Delta A_{TT(VOL)}$	ATT	ATT error	$A_{TT(VOL)} = 0$	−2.0	0	2.0	dB
G_{LB}	LOUDNESS	Voltage gain	f = 100Hz, A_{TT} = −30dB	6.5	9	11.5	dB
G_{LT}	LOUDNESS	Voltage gain	f = 10kHz, A_{TT} = −30dB	4	6	8	dB
V_{OM}	LOUDNESS	Maximun input voltage	THD = 1 %	2.0	2.8	−	Vrms
V_{OM}	Maximun output voltage		THD = 1 %	1.5	2.2	−	Vrms
THD	Total harmonic distortion		f = 1kHz, V_O = 0.5Vrms, loundness = off, $A_{TT(VOL)}$ = 0	−	0.003	0.05	%
V_{NO1}	Output noise voltage		$A_{TT(VOL)}$ = 0, Rg = 0, BW : 10Hz~20kHz	−	5	15	μVrms
V_{NO2}	Output noise voltage		$A_{TT(VOL)} = -\infty$, Rg = 0, BW : 10Hz~20kHz	−	4	8	μVrms
CS	Channel separation		f = 1kHz	−	− 90	− 80	dB

TIMING DIAGRAM



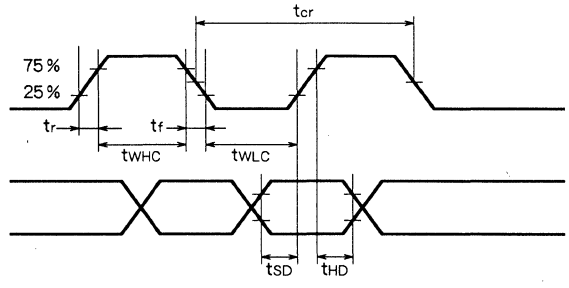
DIGITAL PART DC CHARACTERISTICS (Ta = −30~85℃, V_{CC} = 8V, V_{DD} = 5V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IL}	Low-level input voltage	DATA, CLOCK, ST		0	~	0.2V_{DD}	V
V_{IH}	High-level input voltage			0.8V_{DD}	~	V_{DD}	V
I_{IL}	Low-level input current	V_I = 0	DATA, ST, CLOCK	−10	−	10	μA
I_{IH}	High-level input current	V_I = V_{DD}		−	−	10	μA

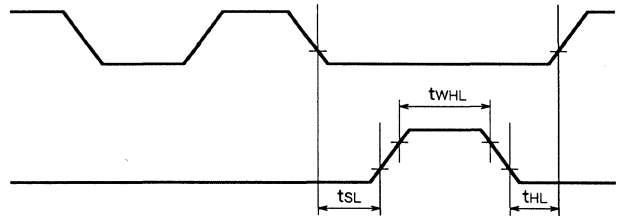
DIGITAL PART AC CHARACTERISTICS (Ta = −30~85℃, V_{CC} = 8V, V_{DD} = 5V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{cr}	CLOCK	Cycle time		2	−	−	μs
t_{WHC}		Pulse width("H"level)		0.8	−	−	μs
t_{WLC}		Pulse width("L"level)		0.8	−	−	μs
t_r		Raise time		−	−	0.2	μs
t_f		Fall time		−	−	0.2	μs
t_{SD}	DATA	Set up time		0.4	−	−	μs
t_{HD}		Hold time		0.4	−	−	μs
t_{SL}	ST	Set up time		0.8	−	−	μs
t_{HL}		Hold time		1	−	−	μs
t_{WHL}		Pulse width		0.8	−	−	μs

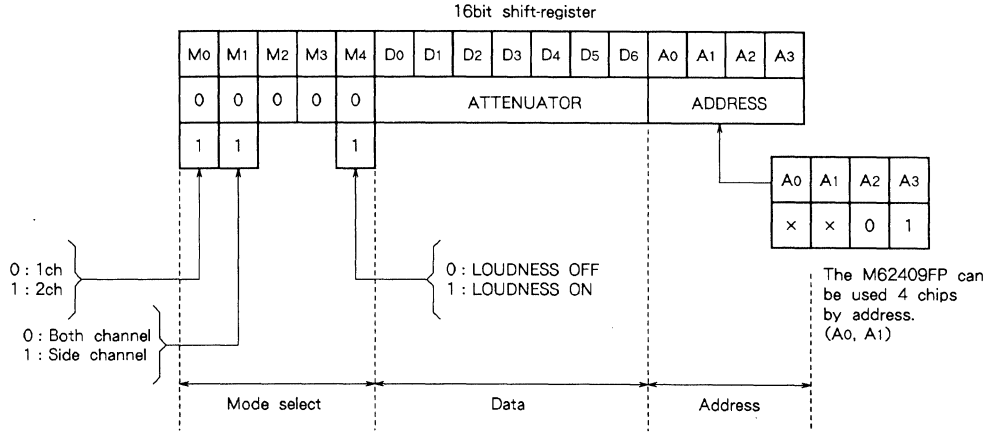
DATA, CLOCK TIMING



ST TIMING



DATA FORMAT

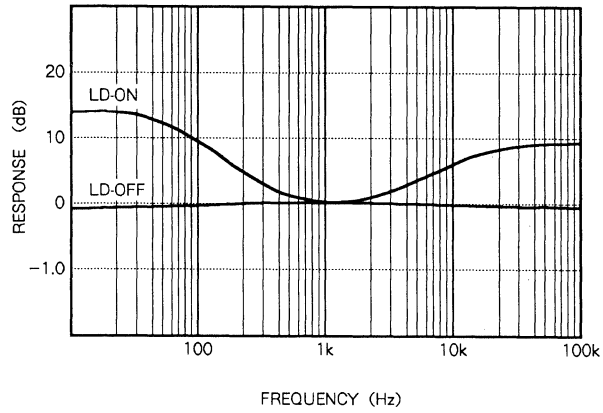


ATTENUATOR CODE

ATT1	D0	D1	D2	D3	D4
0dB	H	H	H	H	H
− 2dB	L	H	H	H	H
− 4dB	H	L	H	H	H
− 6dB	L	L	H	H	H
− 8dB	H	H	L	H	H
− 10dB	L	H	L	H	H
− 12dB	H	L	L	H	H
− 14dB	L	L	L	H	H
− 16dB	H	H	H	L	H
− 18dB	L	H	H	L	H
− 20dB	H	L	H	L	H
− 22dB	L	L	H	L	H
− 24dB	H	H	L	L	H
− 26dB	L	H	L	L	H
− 28dB	H	L	L	L	H
− 30dB	L	L	L	L	H
− 32dB	H	H	H	H	L
− 34dB	L	H	H	H	L
− 36dB	H	L	H	H	L
− 38dB	L	L	H	H	L
− 40dB	H	H	L	H	L
− 42dB	L	H	L	H	L
− 46dB	H	L	L	H	L
− 50dB	L	L	L	H	L
− 54dB	H	H	H	L	L
− 58dB	L	H	H	L	L
− 62dB	H	L	H	L	L
− 66dB	L	L	H	L	L
− 70dB	H	H	L	L	L
− 74dB	L	H	L	L	L
− 78dB	H	L	L	L	L
− ∞	L	L	L	L	L

ATT2	D5	D6
0dB	H	H
− 1dB	L	H
− 2dB	H	L
− 3dB	L	L

FREQUENCY RESPONSE (LOUDNESS)



M62411FP

ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR MULTIAMPLIFIER APPLICATIONS

DESCRIPTION

The M62411FP is a Bi-CMOS IC developed for audio-visual systems. It is suitable for multiamplifiers, being used for processing small analog signals in the stage before power amplifier. The IC uses 8-bit serial data transmitted from a microcomputer in order to perform sound control such as master volume control (VCA system), tone control (bass, mid, and treble), and bass boosting. Its applications also include use as a single output and car audio systems.

FEATURES

- Built-in VCA circuit for main volume control
- Variable volume range ..... – 96dB ~ + 9dB
- Capability of controlling VCA from external source
- Built-in bass booster enhances heavy bass
- Tone control
  - Treble ..... – 10dB ~ + 16dB (2dB/step)
  - Mid ..... – 10dB ~ + 10dB (2dB/step)
  - Bass ..... – 10dB ~ + 16dB (2dB/step)
  - Bass boost ..... – 10dB ~ + 10dB (2dB/step)
- For controlling in each mode, the IC uses built-in microcomputer interface and serial data that regulates volume (8-bit), treble, mid, bass, and bass boost (4-bit)

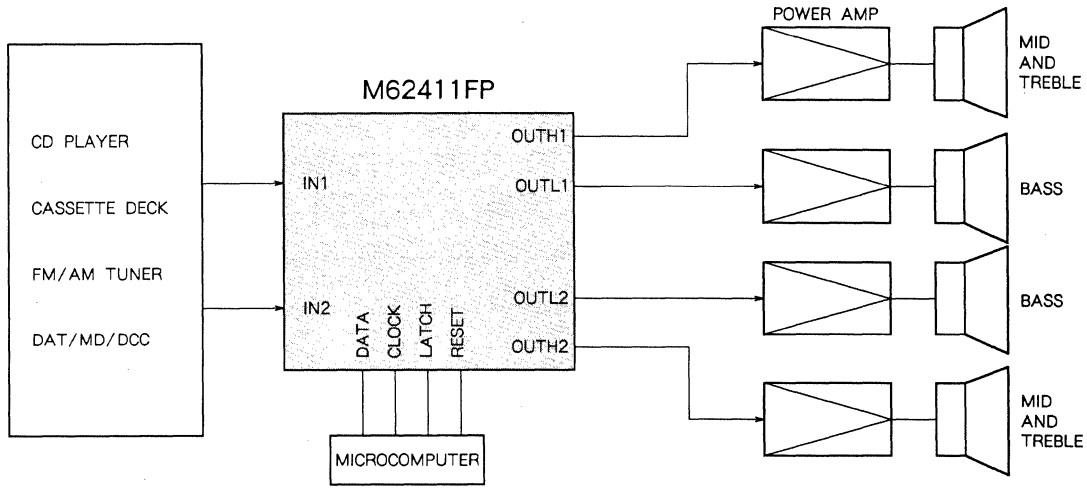
Outline 42P2R-A

0.8mm pitch 450mil SSOP
(8.4mm × 17.5mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 7.5 ~ 12V
Rated supply voltage ..... V_{CC} = 9V

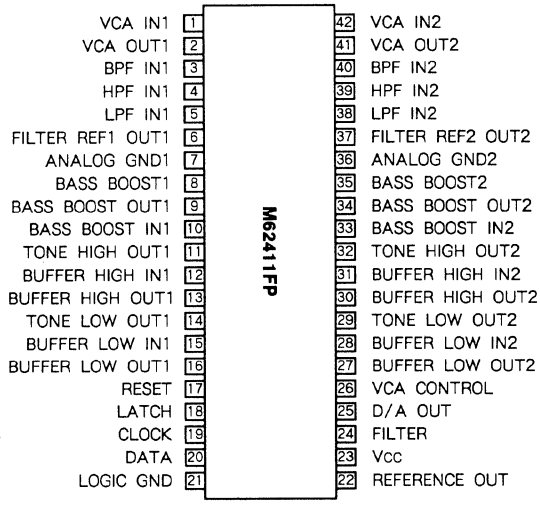
SYSTEM CONFIGURATION



MITSUBISHI ELECTRIC

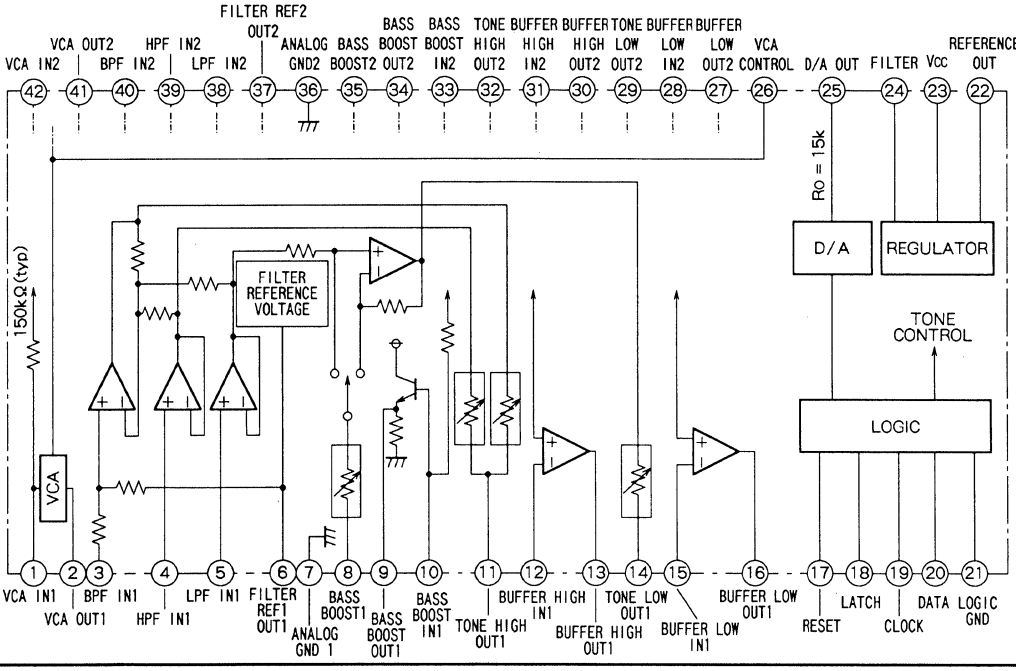
ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR MULTIAMPLIFIER APPLICATIONS

PIN CONFIGURATION



Outline 42P2R-A

IC INTERNAL BLOCK DIAGRAM



ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR MULTIAMPLIFIER APPLICATIONS

PIN DESCRIPTION

Pin No.	Name	Function
① (㊷)	VCA IN 1 (2)	Signal input terminal of ch1 (2)
② (㊶)	VCA OUT 1 (2)	Signal output terminal of ch1 (2)
③ (㊵)	BPF IN 1 (2)	BPF input terminal of ch1 (2)
④ (㊴)	HPF IN 1 (2)	HPF input terminal of ch1 (2)
⑤ (㊳)	LPF IN 1 (2)	LPF input terminal of ch1 (2)
⑥ (㊲)	Filter REF 1 (2)	Filter output for analog refference voltage
⑦ (㊱)	Analog GND 1 (2)	Ground of analog circuit
⑧ (㉟)	Bass-boost 1 (2)	Bass-boost gain terminal
⑨ (㉞)	Bass-boost OUT 1 (2)	Bass-boost resonanse Amplifier output
⑩ (㉝)	Bass-boost IN 1 (2)	Bass-boost resonanse Amplifier input
⑪ (㉜)	Tone high OUT 1 (2)	Treble, mid output
⑫ (㉛)	Buffer high IN 1 (2)	Treble, mid buffer input
⑬ (㉚)	Buffer high OUT 1 (2)	Treble, mid buffer output
⑭ (㉙)	Tone low OUT 1 (2)	Bass, bass-boost out
⑮ (㉘)	Buffer low IN 1 (2)	Bass, bass-boost buffer input
⑯ (㉗)	Buffer low OUT 1 (2)	Bass, bass-boost buffer output
⑰	RESET	MUTE. Set Volume minimum and tone control minimum by high level voltage.
⑱	LATCH	Latch signal of serial data from micro-computer to the IC. Operate at rising eges of pulse.
⑲	CLOCK	Clock signal of serial data from micro-computer to the IC. Operate at rising eges of pulse.
⑳	DATA	Serial data input.(LSB first)
㉑	Logic GND	Ground of digital circuit
㉒	REFERENCE OUT	Refference output voltage source.(5.8Vtyp)
㉓	Vcc	Supply voltage (7.5V~12V)
㉔	FILTER	Filter for ripple
㉕	D/A OUT	VCA control voltage source by D/A convertor
㉖	VCA CONTROL	VCA gain control terminal

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	14	V
V_I	Digital input voltage	− 0.3~7.0	V
P_d	Power dissipation	1000 * standard board	mW
K_θ	Thermal derating	10 ($T_a \geqq 25$℃)	mW/℃
T_{opr}	Operating temperature	− 10~+ 70	℃
T_{stg}	Storage temperature	− 40~+ 125	℃

* Standard board
- board size 70mm × 70mm
- board thickness 1.6mm
- board material glass epoxy
- copper pattern
  copper thickness 18μm
  copper size 0.25mm(width) 30mm(length/lead)

ELECTRICAL CHARACTERISTICS

(Ta = 25℃, Vcc = 9V, Control data : FF5550 (volume max/tone flat), f = 1kHz, unless otherwise noted)

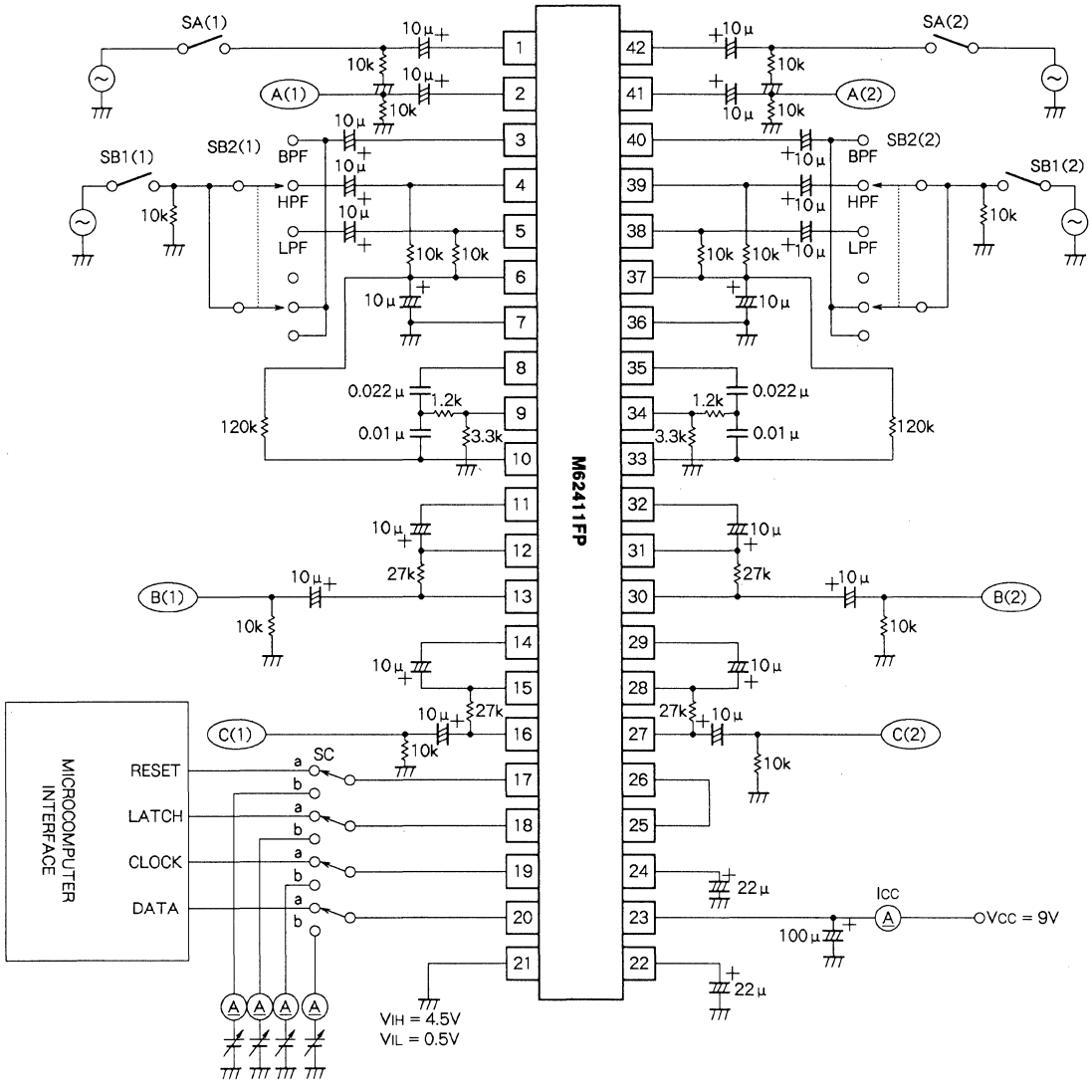
Symbol		Parameter	Test conditions: Input condition	Control data	Switch condition: SA	SB1	SB2	SC	Measurement point	Limits: Min	Typ	Max	Unit
I_{CC}	Supply voltage	Circuit current	Quiescent	FF5550	OPEN	OPEN	BPF	a	PIN㉓	26	38	50	mA
V_{REF}		Reference voltage	⇧	⇧	⇧	⇧	⇧	⇧	PIN㉒	5.4	5.8	6.3	V
V_{FIL}		Filter voltage	⇧	⇧	⇧	⇧	⇧	⇧	PIN㉔	8.2	8.9	–	V
I_{IH}	Logic	level "H" input current	V_{IH} = 4.5V	FF5550	OPEN	OPEN	BPF	b	PIN⑰ PIN⑱ PIN⑲ PIN⑳	0.3	1.0	3.0	μA
I_{IL}		level "L" input current	V_{IL} = 0.5V	⇧	⇧	⇧	⇧	⇧	⇧	−0.3	0.0	0.3	μA
OFSTM1	Switching offset	Tre/mid switching offset voltage	Quiescent (data switching offset voltage difference)	FFD050 → FF0A50	OPEN	OPEN	BPF	a	PIN⑪ PIN㉜	−20	0	+20	mV
OFSBB1		Boost switching offset voltage 1	⇧	FF5550 → FF5555	⇧	⇧	⇧	⇧	PIN⑧ PIN㉟	−10	0	+10	mV
OFSBB2		Boost switching offset voltage 2	⇧	FF5550 → FF555D	⇧	⇧	⇧	⇧	⇧	−10	0	+10	mV
CBVT	Channel balance	Total channel balance 1	(Calculation)	–	–	–	–	–	CB + CBT	−3	0	3	dB
CBVM		Total channel balance 2	(Calculation)	–	–	–	–	–	CB + CBM	−3	0	3	dB
CBVB		Total channel balance 3	(Calculation)	–	–	–	–	–	CB + CBBA	−3	0	3	dB
ATT (min)	Electronic volume	Minimum Attenuation level	V_i = −14dBV *1	FF5550	CLOSE	OPEN	BPF	a	A(1), A(2)	7.2	9.0	10.8	dB
CB		Channel balance	⇧	⇧	⇧	⇧	⇧	⇧	A(1)/ A(2)	−1.8	0	1.8	dB
THD		Total harmonic distortion	V_i=−14dBV, *1 BPF=400Hz～30kHz	⇧	⇧	⇧	⇧	⇧	A(1), A(2)	–	0.02	0.1	%
No (min)		Noise voltage	Quiescent IHF-A	⇧	OPEN	⇧	⇧	⇧	⇧	–	25.0	56.0	μVrms
THD (max)		Maximum total harmonic distortion	V_i=−3dBV, *1 BPF=400Hz～30kHz	⇧	CLOSE	⇧	⇧	⇧	⇧	–	0.1	1.0	%
ATT (−10)		Attenuation level (−10dB)	V_i = −14dBV *1	9A5550	⇧	⇧	⇧	⇧	⇧	−2.8	−1.0	0.8	dB
ATT (max)		Maximum attenuation level	V_i = −3dBV, *1 IHF-A	005550	⇧	⇧	⇧	⇧	⇧	–	−97	−77	dB
No		Maximum attenuation noise voltage	Quiescent IHF-A	⇧	OPEN	⇧	⇧	⇧	⇧	–	10.0	20.0	μVrms
CT		Cross talk	V_i = −3dBV, *1 IHF-A	FF5550	OPEN/ CLOSE CLOSE/ OPEN	⇧	⇧	⇧	⇧	–	−90	−70	dB
GVT	Treble	Voltage gain	V_i = −18dBV *2	FF5550	OPEN	CLOSE	HPF	a	B(1), B(2)	−6	−4	−2	dB
CBT		Channel balance	⇧	⇧	⇧	⇧	⇧	⇧	B(1)/ B(2)	−2	0	+2	dB
THDT		Total harmonic distortion	V_i = −18dBV BPF=400Hz～30kHz	⇧	⇧	⇧	⇧	⇧	B(1), B(2)	–	0.01	0.1	%
NoT		Noise voltage	Quiescent IHF-A	⇧	⇧	OPEN	⇧	⇧	⇧	–	11.0	22.0	μVrms

ELECTRICAL CHARACTERISTICS (Cont.)
(Ta = 25℃, Vcc = 9V, Control data : FF5550 (volume max/tone flat), f = 1kHz, unless otherwise noted)

Symbol		Parameter	Test conditions: Input condition	Control data	Switch condition: SA	SB1	SB2	SC	Measurement point	Limits: Min	Typ	Max	Unit
THDT max	Treble	Maximum total harmonic distortion	Vi=-5dBV, BPF=400Hz~30kHz *2	FFD550	OPEN	CLOSE	HPF	a	B(1), B(2)	–	0.1	1.0	%
GVT (max)		Maximum voltage gain	Vi = – 18dBV *2	⇧	⇧	⇧	⇧	⇧	⇧	10	12	14	dB
GVT (min)		Minimum voltage gain	⇧	FF0550	⇧	⇧	⇧	⇧	⇧	– 16	– 14	– 12	dB
CTT		Cross talk	Vi = – 5dBV *2 IHF-A	FFD550	⇧	OPEN/CLOSE CLOSE/OPEN	⇧	⇧	⇧	–	– 80	– 60	dB
GVM	Mid	Voltage gain	Vi = – 18dBV *3	FF5550	OPEN	CLOSE	BPF	a	B(1), B(2)	– 6.0	– 4.0	– 2.0	dB
CBM		Channel balance	⇧	⇧	⇧	⇧	⇧	⇧	B(1)/B(2)	– 2	0	+ 2	dB
THDM		Total harmonic distortion	Vi = – 18dBV BPF=400Hz~30kHz	⇧	⇧	⇧	⇧	⇧	B(1), B(2)	–	0.01	0.1	%
NoM		Noise voltage	Quiescent IHF-A	⇧	⇧	OPEN	⇧	⇧	⇧	–	11.0	22.0	μVrms
THDM max		Maximum total harmonic distortion	Vi=+1dBV, BPF=400Hz~30kHz *3	FF5A50	⇧	CLOSE	⇧	⇧	⇧	–	0.1	1.0	%
GVM (max)		Maximum voltage gain	Vi = – 18dBV *3	⇧	⇧	⇧	⇧	⇧	⇧	– 4.0	– 6.0	– 8.0	dB
GVM (min)		Minimum voltage gain	⇧	FF5050	⇧	⇧	⇧	⇧	⇧	– 16	– 14	– 12	dB
CTM		Cross talk	Vi = – 5dBV, IHF-A *3	FF5A50	⇧	OPEN/CLOSE CLOSE/OPEN	⇧	⇧	⇧	–	– 80	– 60	dB
GVBA	Bass	Voltage gain	Vi = – 18dBV *4	FF5550	OPEN	CLOSE	LPF	a	C(1), C(2)	– 6	– 4	– 2	dB
CBBA		Channel balance	⇧	⇧	⇧	⇧	⇧	⇧	C(1)/C(2)	– 2	0	+ 2	dB
THDBA		Total harmonic distortion	Vi = – 18dBV BPF=400Hz~30kHz	⇧	⇧	⇧	⇧	⇧	C(1), C(2)	–	0.01	0.1	%
NoBA		Noise voltage	Quiescent IHF-A	⇧	⇧	OPEN	⇧	⇧	⇧	–	8.0	16.0	μVrms
THDBA max		Maximum total harmonic distortion	Vi=-5dBV, BPF=400Hz~30kHz *4	FF55D0	⇧	CLOSE	⇧	⇧	⇧	–	0.1	1.0	%
GVBA (max)		Maximum voltage gain	Vi = – 18dBV *4	⇧	⇧	⇧	⇧	⇧	⇧	10	12	14	dB
GVBA (min)		Minimum voltage gain	⇧	FF5500	⇧	⇧	⇧	⇧	⇧	– 16	– 14	– 12	dB
CTBA		Cross talk	Vi = – 5dBV *4 IHF-A	FF55D0	⇧	OPEN/CLOSE CLOSE/OPEN	⇧	⇧	⇧	–	– 80	– 60	dB
THDBB max		Boost maximum total harmonic distortion	Vi=-10dBV, BPF=400Hz~30kHz *4	FF55D5	⇧	CLOSE	⇧	⇧	⇧	–	0.1	1.0	dB
GVBB (max)		Boost maximum voltage gain	Vi = – 10dBV *4	FF5555	⇧	⇧	⇧	⇧	⇧	4	6	8	dB
GVBB (min)		Boost minimum voltage gain	⇧	FF555D	⇧	⇧	⇧	⇧	⇧	– 16	– 14	– 12	dB

*1 : Vi is VCA input voltage *2 : Vi is HPF input voltage *3 : Vi is BPF input voltage *4 : Vi is LPF input voltage

TEST CIRCUIT



Units Resistance : Ω
Capacitance : F

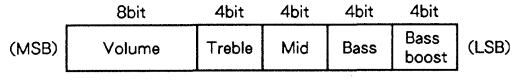
ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR MULTIAMPLIFIER APPLICATIONS

OPERATIONAL DESCRIPTION

1. CONTROL METHOD

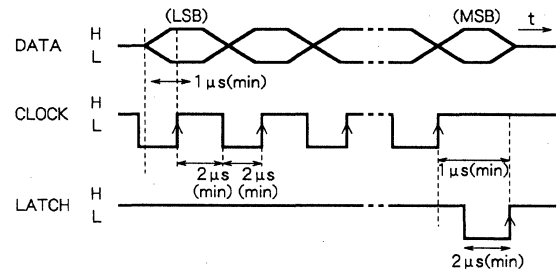
(1) DIGITAL CONTROL SPECIFICATION

Data format



Volume : 00~FF (8bit D/A data)
Treble : 0~D (14step)
Mid : 0~A (11step)
Bass : 0~D (14step)
Bass-boost : 0 (11step)
1~5
9~D

Timing diagram (Recommended condition)



Note 1. RESET (MUTE) is volume minimum and tone control minimum by "H"level.
Puls width 2µs (min)
2. CLOCK, LATCH functions operates at rising ege of pulse.
3. Recommended input level
"H"level : more than 4V
"L"level : less than 1V
the, threshold voltage (Logic input buffer) is about 2.5V.

CONTROL DATA TABLE

D/A converter for VCA		TERBLE		MID		BASS		BASS-BOOST	
DATA	OUTPUT VOLTAGE	DATA	GAIN	DATA	GAIN	DATA	GAIN	DATA	GAIN
00	V_Z	0	− 10dB	0	− 10dB	0	− 10dB	0	± 0dB
01	$\frac{255V_Z + V_F}{256}$	1	− 8dB	1	− 8dB	1	− 8dB	1	+ 2dB
		2	− 6dB	2	− 6dB	2	− 6dB	2	+ 4dB
		3	− 4dB	3	− 4dB	3	− 4dB	3	+ 6dB
		4	− 2dB	4	− 2dB	4	− 2dB	4	+ 8dB
		5	± 0dB	5	± 0dB	5	± 0dB	5	+ 10dB
		6	+ 2dB	6	+ 2dB	6	+ 2dB	6	−
		7	+ 4dB	7	+ 4dB	7	+ 4dB	7	−
		8	+ 6dB	8	+ 6dB	8	+ 6dB	8	−
		9	+ 8dB	9	+ 8dB	9	+ 8dB	9	− 2dB
		A	+ 10dB	A	+ 10dB	A	+ 10dB	A	− 4dB
		B	+ 12dB	B	−	B	+ 12dB	B	− 6dB
		C	+ 14dB	C	−	C	+ 14dB	C	− 8dB
		D	+ 16dB	D	−	D	+ 16dB	D	− 10dB
FE	$\frac{2V_Z + 254V_F}{256}$	E	−	E	−	E	−	E	−
FF	$\frac{V_Z + 255V_F}{256}$	F	−	F	−	F	−	F	−

Note Typical or designed value. V_Z, V_F is internal power supply voltage.
+ 12dB~+ 16dB of treble and bass are for loudness.

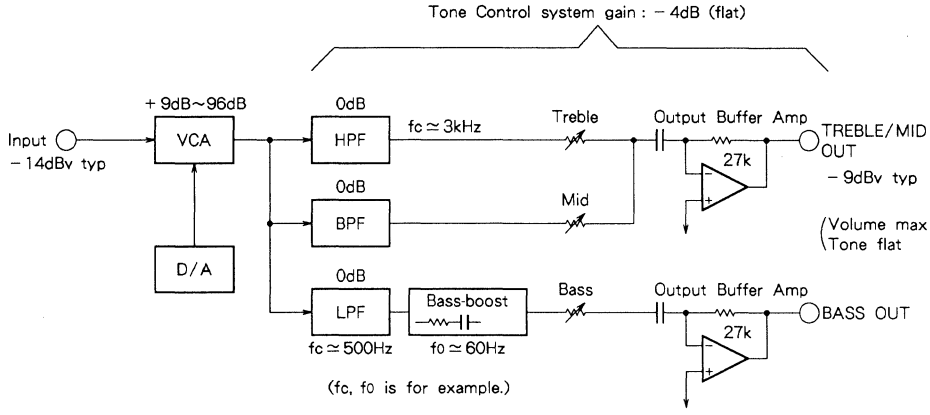
MITSUBISHI ELECTRIC

VCA GAIN LEVEL (EXAMPLE)

Control data (D/A converter)	VCA gain level (dB)
0F	(Maximum attenuation)
1F	− 79
2F	− 59
3F	− 44
4F	− 32
5F	− 23
6F	− 15
7F	− 9
8F	− 4
9F	0
AF	+ 3
BF	+ 5
CF	+ 6
DF	+ 7
EF	+ 8
FF	+ 9

(2) SIGNAL PROCESSING SYSTEM

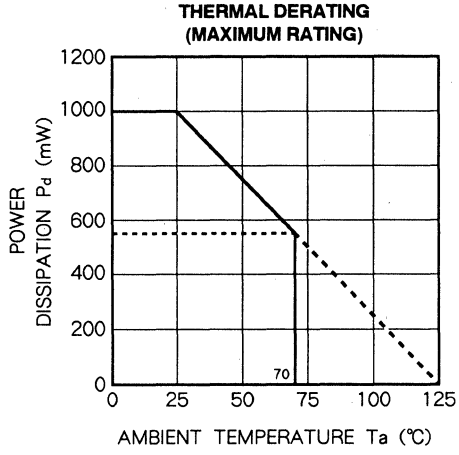
[System] {Total gain : + 5dB (VCA MAX)}



Voltage gain (designed value. Tone control system gain : − 4dB (flat))

Volume (VCA) : + 9dB~ − 96dB typ.
Treble : − 10dB~0dB~ + 10dB (2dB/step)
(+ 12dB, + 14dB, + 16dB for loudness)
Mid : − 10dB~0dB~ + 10dB (2dB/step)
Bass : − 10dB~0dB~ + 10dB (2dB/step)
(+ 12dB, + 14dB, + 16dB for loudness)
Bass-boost : − 10dB~0dB~ + 10dB (2dB/step)

TYPICAL CHARACTERISTICS



APPLICATION NOTES

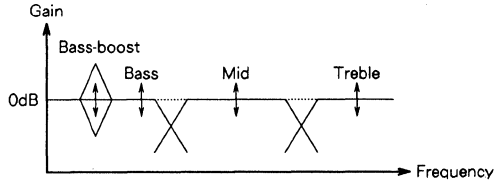
(1) Take care of the heat radiation of PCB.

(2) Take care of a PCB design about digital noise.

(3) The IC has three GND pins.

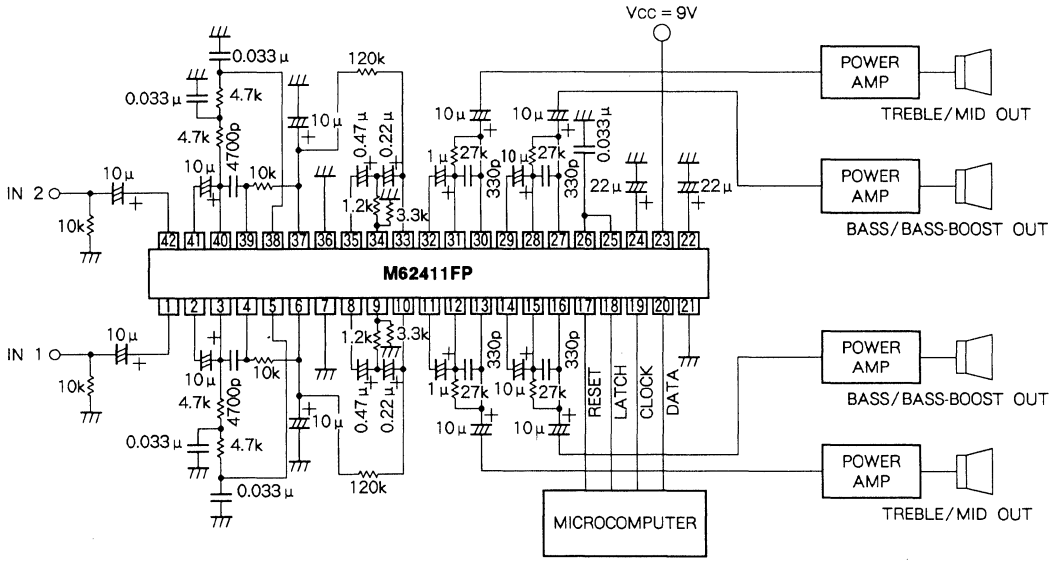
(4) Take care of electrostatic damage of ⑥pin and ㊲pin.

(5) Take care of gain characteristics of tone control. The loose attenuation characterestics of filters will disturb the frequency respose in another filtering region.



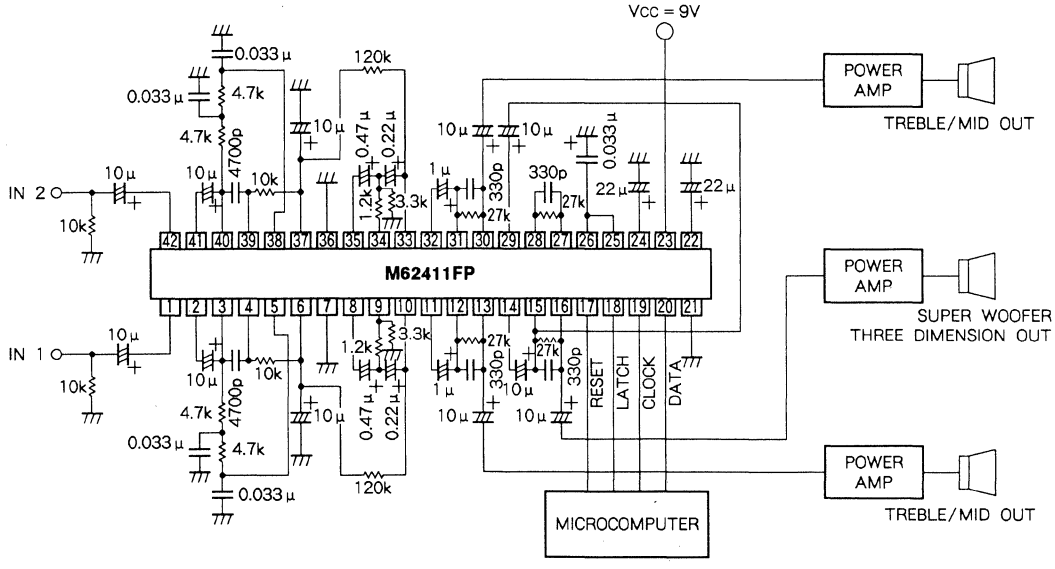
ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR MULTIAMPLIFIER APPLICATIONS

APPLICATION EXAMPLE 1 (Bi-amplifier system)



Units Resistance : Ω
Capacitance : F

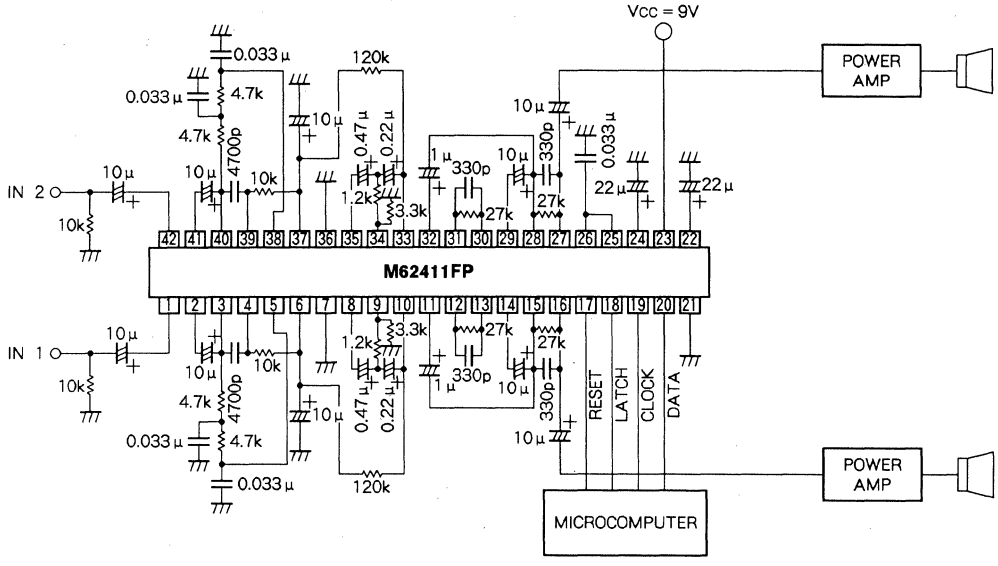
APPLICATION EXAMPLE 2 (Three dimensional type)



Units Resistance : Ω
Capacitance : F

ELECTRONIC VOLUME CONTROL WITH TONE CONTROLLER FOR MULTIAMPLIFIER APPLICATIONS

APPLICATION EXAMPLE 3 (Standard type)



Units Resistance : Ω
Capacitance : F

MITSUBISHI ELECTRIC

M62412P

2CH 4 MODE PRESET EQUALIZER

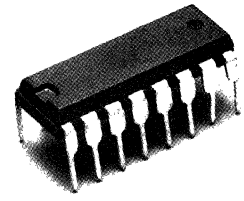
DESCRIPTION

The M62412P is a preset equalizer IC developed for mini compo and radio cassette units.

This IC having sound effects of 4 modes, "Normal", "Rock", "Pops" and "Classic". These modes are selected by combining DC levels of the 2 control terminals.

FEATURES

- Can be realized preset equalizer at external capacitors of 3 pieces per channel.
- Sound effects of 4 modes can be selected at 2 switches.



Outline 16P4

2.54mm pitch 300mil DIP

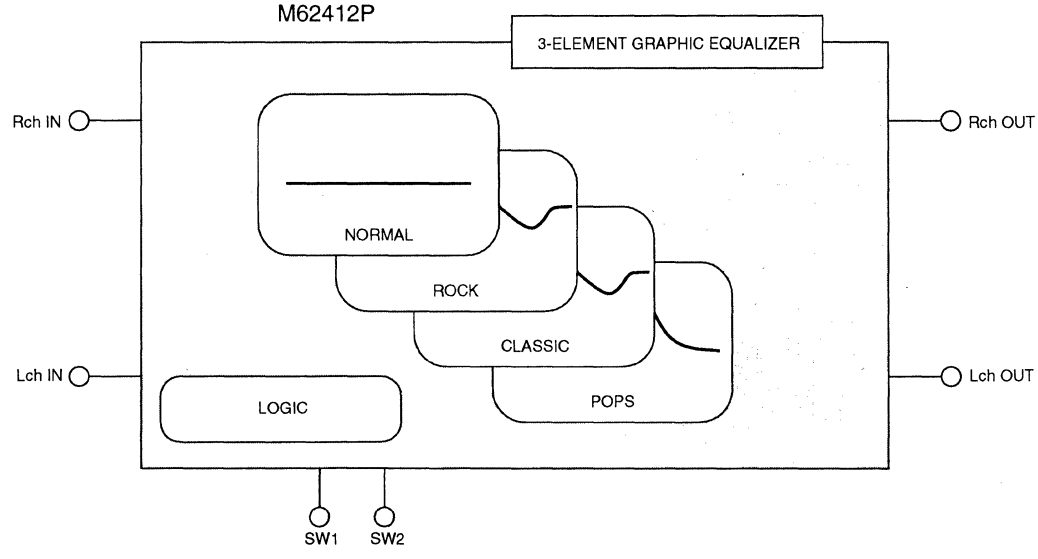
(6.3mm×19.0mm×3.3mm)

RECOMMENDED OPERATING CONDITIONS

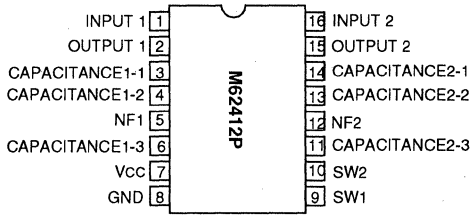
Supply voltage range ..... Vcc = 8 ~ 13 V

Rated supply voltage ..... Vcc = 10.7 V

SYSTEM CONFIGURATION

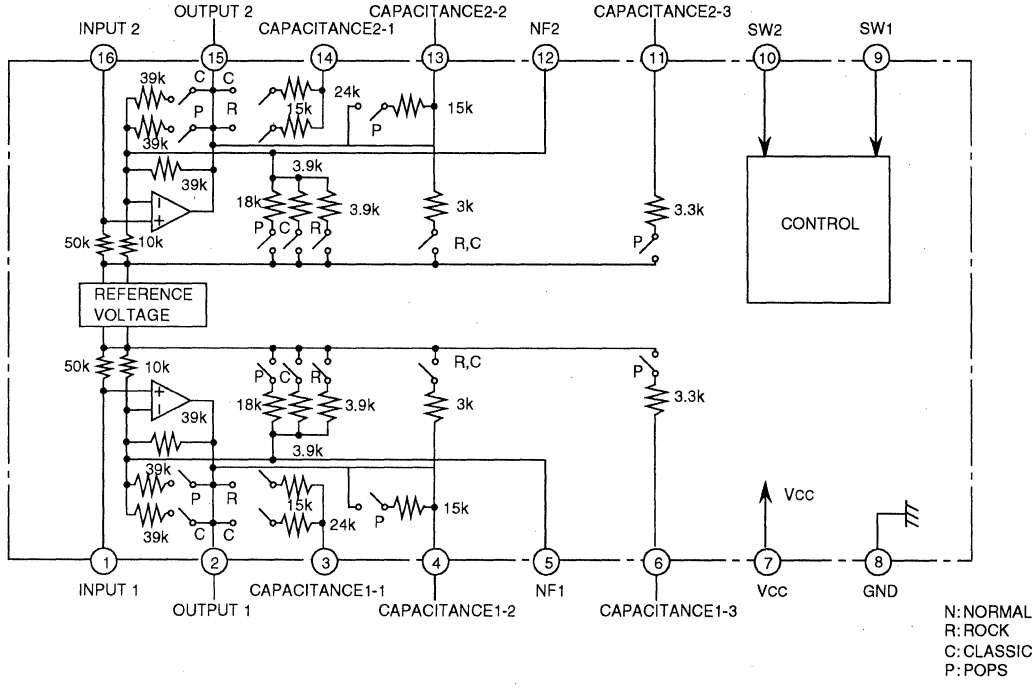


PIN CONFIGURATION



Outline 16P4

IC INTERNAL BLOCK DIAGRAM



Units Resistance : Ω

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{ccmax}	Supply voltage	14	V
P_d	Power dissipation (Ta≦25℃)	1000	mW
K_θ	Thermal derating (Ta>25℃)	10.0	mW/℃
T_{opr}	Operating temperature	−20～75	°C
T_{stg}	Storage temperature	−40～125	°C
V_I	Switch input voltage range	−0.3～V_{cc} 0.3	V

SWITCH CONDITIONS (L≦1.0 V, H≧3.5 V)

	SW 1 ⑨pin	SW 2 ⑩pin
Normal	L	L
Rock	L	H
Classic	H	L
Pops	H	H

ELECTRICAL CHARACTERISTICS (Normal, Vcc = 10.7 V, f = 1 kHz, Vi = 56 mVrms unless otherwise noted)

Symbol		Parameter	Test conditions	Switchs									Limits			Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9	Min	Typ	Max	
Icc		Circuit current	Quiescent	L	L	2	1	1	2	1	1	2	4.8	8.0	11.2	mA
G (Normal)	Normal	Output voltage gain		L	L	1	1	1	1	1	1	1	11.8	13.8	15.8	dB
V_{OM} (Normal)	Normal	Maximum output voltage	R_L = 7.5kΩ THD = 1%	L	L	1	1	1	1	1	1	1	2.0	2.5	–	V_{rms}
THD (Normal)	Normal	Total harmonic distortion	BW : 400～30kHz	L	L	1	1	1	1	1	1	1	–	0.013	0.1	%
V_{NO} (Normal)	Normal	Output noise voltage	R_g = 10kΩ Quiescent, IHF-A	L	L	2	1	1	1	1	1	2	–	20	40	μV_{rms}
G (ROCK)	ROCK	Output voltage gain		L	H	1	1	1	1	1	1	1	20.2	23.2	26.2	dB
V_{OM} (ROCK)	ROCK	Maximum output voltage	R_L = 7.5kΩ THD = 1%	L	H	1	1	1	1	1	1	1	2.0	2.7	–	V_{rms}
THD (ROCK)	ROCK	Total harmonic distortion	BW : 400～30kHz	L	H	1	1	1	1	1	1	1	–	0.025	0.1	%
V_{NO} (ROCK)	ROCK	Output noise voltage	R_g = 10kΩ Quiescent, IHF-A	L	H	2	1	1	1	1	1	2	–	30	60	μV_{rms}
G (CLASSIC)	CLASSIC	Output voltage gain		H	L	1	1	1	1	1	1	1	16.8	19.8	22.8	dB
V_{OM} (CLASSIC)	CLASSIC	Maximum output voltage	R_L = 7.5kΩ THD = 1%	H	L	1	1	1	1	1	1	1	2.0	2.7	–	V_{rms}
THD (CLASSIC)	CLASSIC	Total harmonic distortion	BW : 400～30kHz	H	L	1	1	1	1	1	1	1	–	0.023	0.1	%
V_{NO} (CLASSIC)	CLASSIC	Output noise voltage	R_g = 10kΩ Quiescent, IHF-A	H	L	2	1	1	1	1	1	2	–	27	54	μV_{rms}
G (POPS)	POPS	Output voltage gain		H	H	1	1	2	1	2	1	1	14.5	17.5	20.5	dB
V_{OM} (POPS)	POPS	Maximum output voltage	R_L = 7.5kΩ THD = 1%	H	H	1	1	2	1	2	1	1	2.0	2.7	–	V_{rms}
THD (POPS)	POPS	Total harmonic distortion	BW : 400～30kHz	H	H	1	1	2	1	2	1	1	–	0.013	0.1	%
V_{NO} (POPS)	POPS	Output noise voltage	R_g = 10kΩ Quiescent, IHF-A	H	H	2	1	2	1	2	1	2	–	18	36	μV_{rms}
CS_{ep}		Channel separation	R_g = 10kΩ IHF-A	L	L	2	1	1	1	1	1	2	–	−75	−65	dB
R_i		Input resistor		L	L	1	1↓2	1	1	1	1↓2	1	35	50	–	kΩ

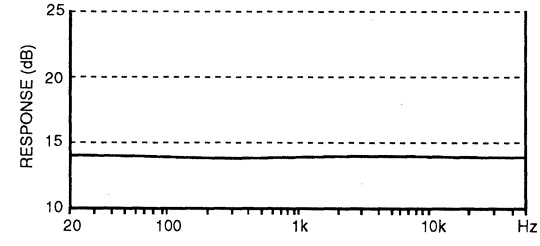
FUNCTION DESCRIPTION

ELECTRICAL CHARACTERISTICS OF APPLICATION EXAMPLE (Normal, Vcc = 10.7 V, f = 1 kHz, Vi = 0.1 Vrms, f = 1 kHz unless otherwise noted)

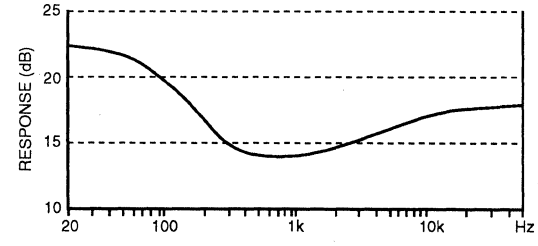
Symbol	Parameter			Conditions	Data	Unit
Icc	Circuit current			Vcc = 10.7V	8.0	mA
G(Normal)B	Preset mode	Normal voltage gain	BASS	f = 80Hz	14	dB
G(Normal)M			MID	f = 1kHz	14	dB
G(Normal)T			TREBLE	f = 10kHz	14	dB
G(ROCK)B		Rock voltage gain	BASS	f = 80Hz	20	dB
G(ROCK)M			MID	f = 1kHz	14	dB
G(ROCK)T			TREBLE	f = 10kHz	16	dB
G(CLASSIC)B		Classic voltage gain	BASS	f = 80Hz	16	dB
G(CLASSIC)M			MID	f = 1kHz	14	dB
G(CLASSIC)T			TREBLE	f = 10kHz	16	dB
G(POPS)B		Pops voltage gain	BASS	f = 80Hz	12	dB
G(POPS)M			MID	f = 1kHz	16	dB
G(POPS)T			TREBLE	f = 10kHz	14	dB
VOM	Maximum output voltage			THD = 1%, f = 1kHz	2.5	Vrms
THD	Total harmonic distortion			f = 1kHz, Vo = 0.5Vrms BW = 400Hz~30kHz	0.02	%
VNO	Output noise voltage			Rg = 10kΩ, BW : IHF-A	20.0	μVrms
CSep	Channel separation			f = 1kHz, BW : IHF-A	−75	dB
Ri	Input resistor				50	kΩ

SOUND CONTROL SPECK OF APPLICATION EXAMPLE

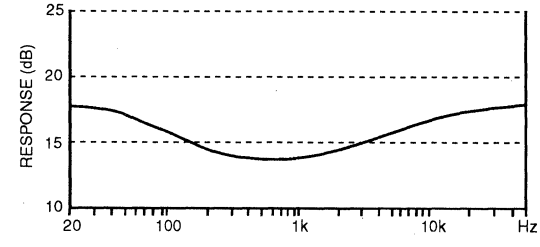
NORMAL



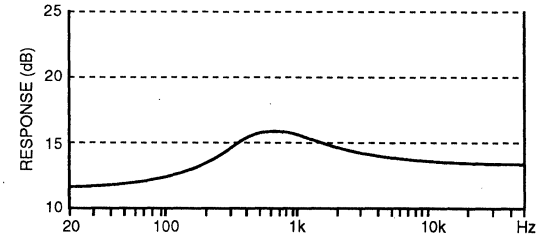
ROCK



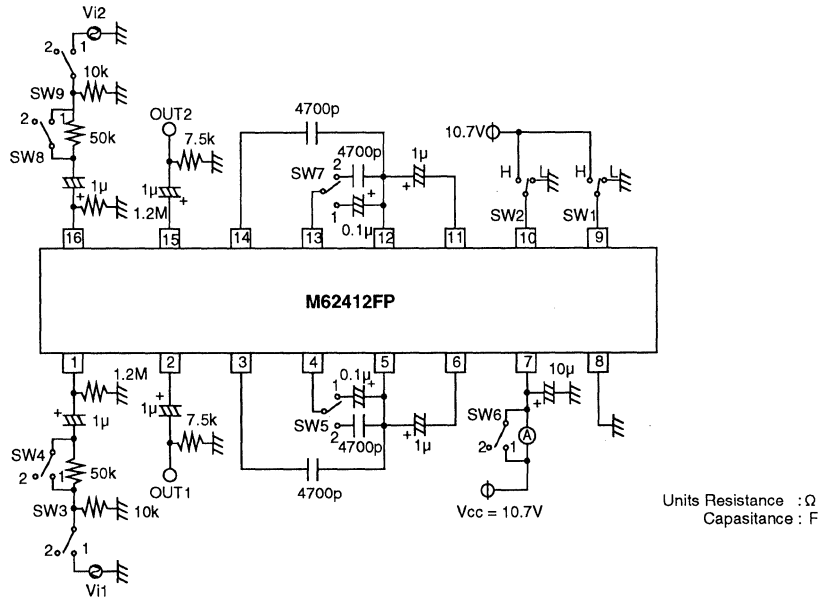
CLASSIC



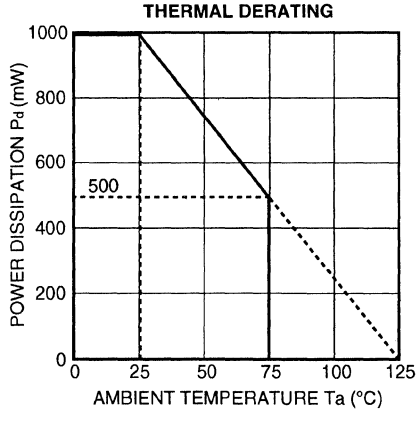
POPS

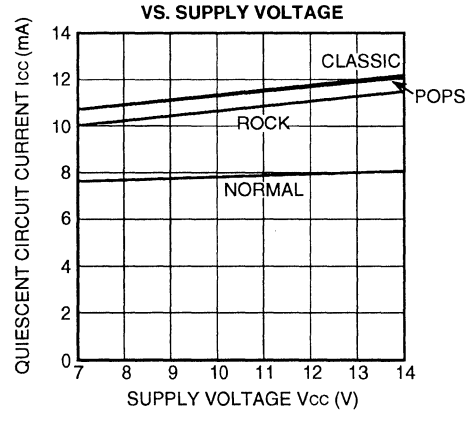


TEST CIRCUIT

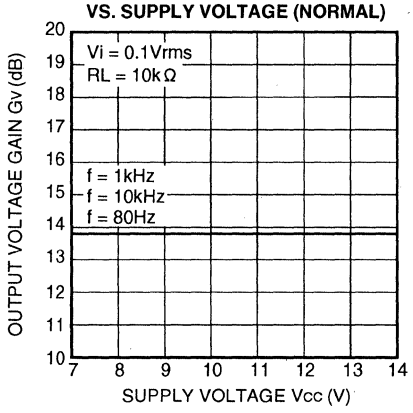


TYPICAL CHARACTERISTICS

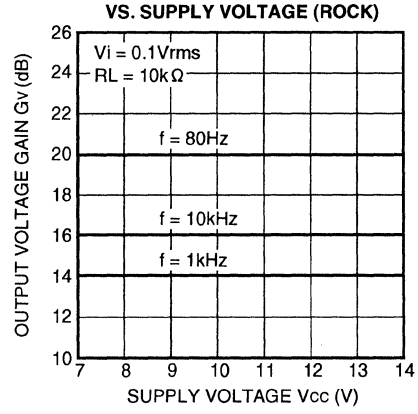




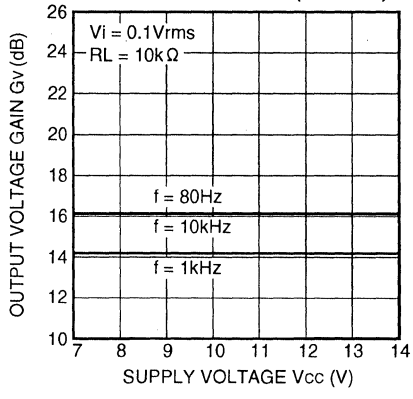
OUTPUT VOLTAGE GAIN
VS. SUPPLY VOLTAGE (NORMAL)



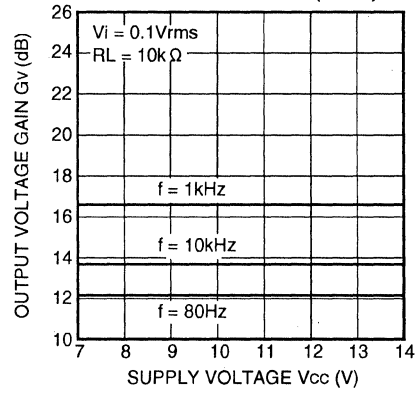
OUTPUT VOLTAGE GAIN
VS. SUPPLY VOLTAGE (ROCK)



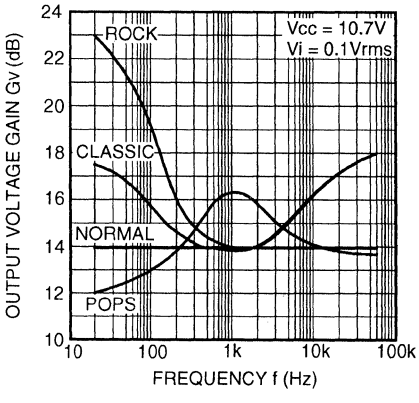
OUTPUT VOLTAGE GAIN
VS. SUPPLY VOLTAGE (CLASSIC)



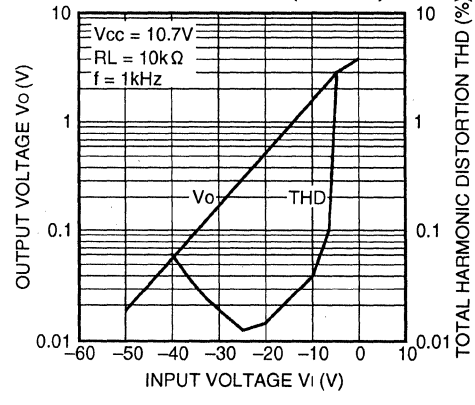
OUTPUT VOLTAGE GAIN
VS. SUPPLY VOLTAGE (POPS)



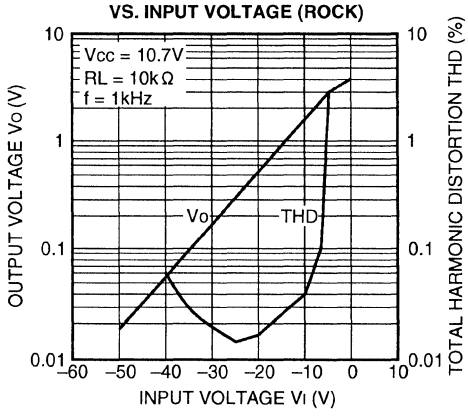
OUTPUT VOLTAGE GAIN
VS. FREQUENCY



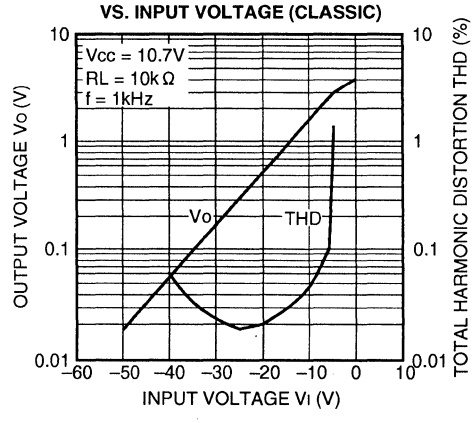
TOTAL HARMONIC DISTORTION
OUTPUT VOLTAGE
VS. INPUT VOLTAGE (NORMAL)



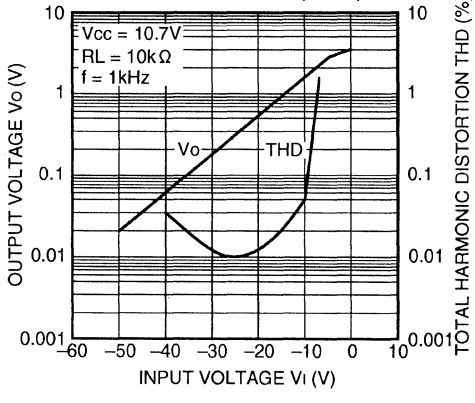
TOTAL HARMONIC DISTORTION OUTPUT VOLTAGE VS. INPUT VOLTAGE (ROCK)



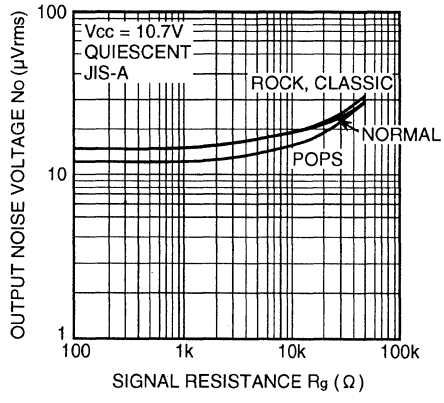
TOTAL HARMONIC DISTORTION OUTPUT VOLTAGE VS. INPUT VOLTAGE (CLASSIC)



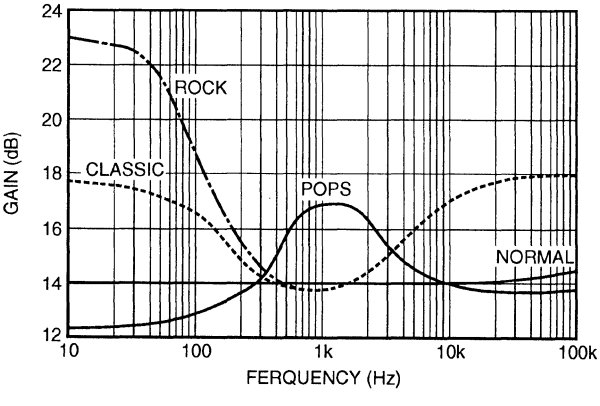
TOTAL HARMONIC DISTORTION OUTPUT VOLTAGE VS. INPUT VOLTAGE (POPS)



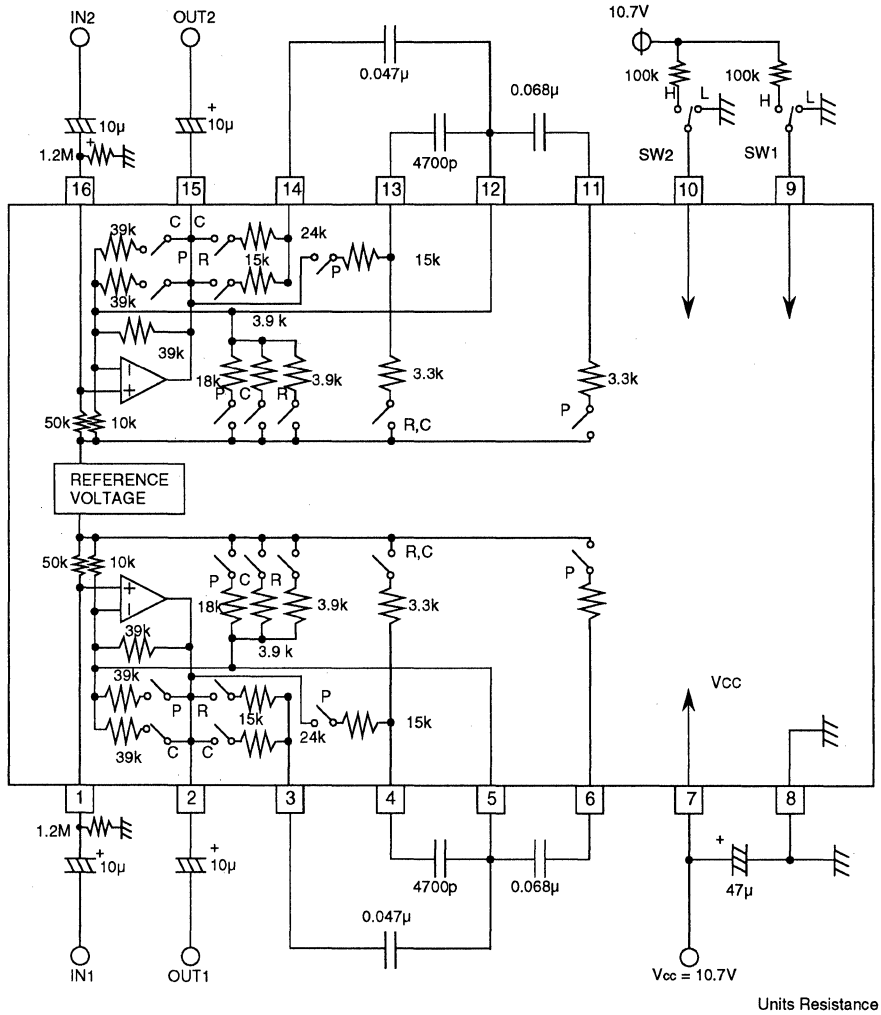
OUTPUT NOISE VOLTAGE VS. SIGNAL RESISTANCE



FREQUENCY CHARACTERISTICS



APPLICATION EXAMPLE



Units Resistance :Ω
Capasitance : F

M62413FP

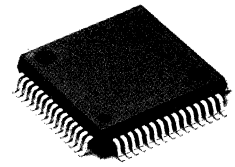
ELECTRONIC SOUND CONTROL WITH ELECTRONIC VOLUME FOR MULTIPLE SOURCES

DESCRIPTION

The M62413FP Integrated Circuit is developed for audio-visual equipment.
It being used for controls sound in the power amplifier front stage.
This IC having are 2 channel input selector with 4 inputs, master volume control [by the VCA (voltage controlled amplifier) system], tone controls (bass, mid, treble) and super bass that IC can be operated by using serial data from microcomputer.
This IC can be applied to not only audio systems but also TV.

FEATURES

- Built-in electronic volume circuit for main volume control
- Volume variation range····· – 96dB~ + 9dB
- With built-in bus boost circuit, bass can be intensified
- Sound control
  - Treble ····· – 10dB~ + 16dB(2dB/step)
  - Mid····· – 10dB~ + 10dB(2dB/step)
  - Bass ····· – 10dB~ + 16dB(2dB/step)
  - Super bass····· – 12dB~ + 12dB(2dB and 3dB/step)
- Volume is controlled by 8-bit serial data from micro-computer
  Treble, mid, bass and super bass are controlled each by 4-bit serial data
- Built-in microcomputer interface circuit
- Built-in selector circuit (4 inputs)
- Built-in output ports (9 lines)

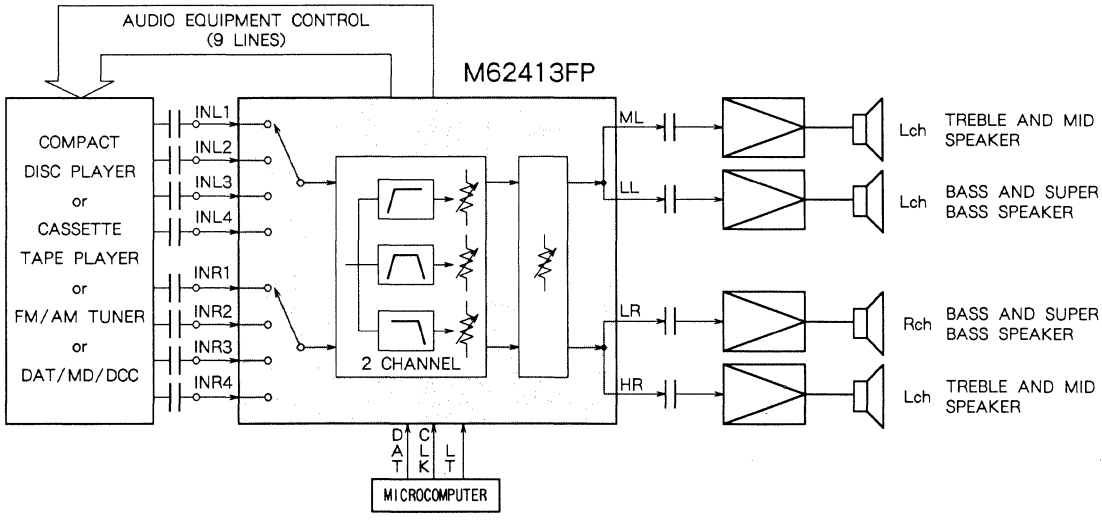


Outline 64P6N-A
0.8mm pitch QFP
(14.0mm × 14.0mm × 2.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range····· V_{CC} = 7.5~12V
Rated supply voltage····· V_{CC} = 9V

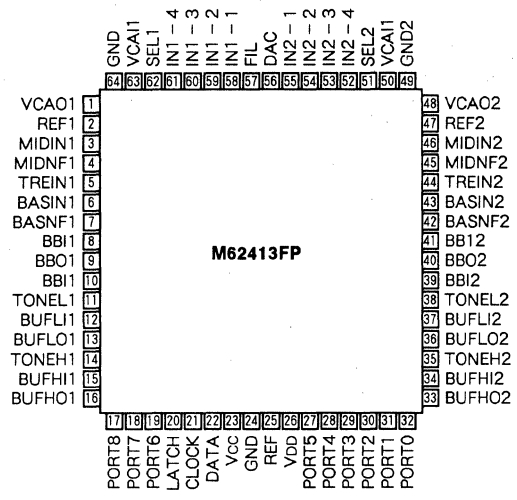
SYSTEM CONFIGURATION



M62413FP

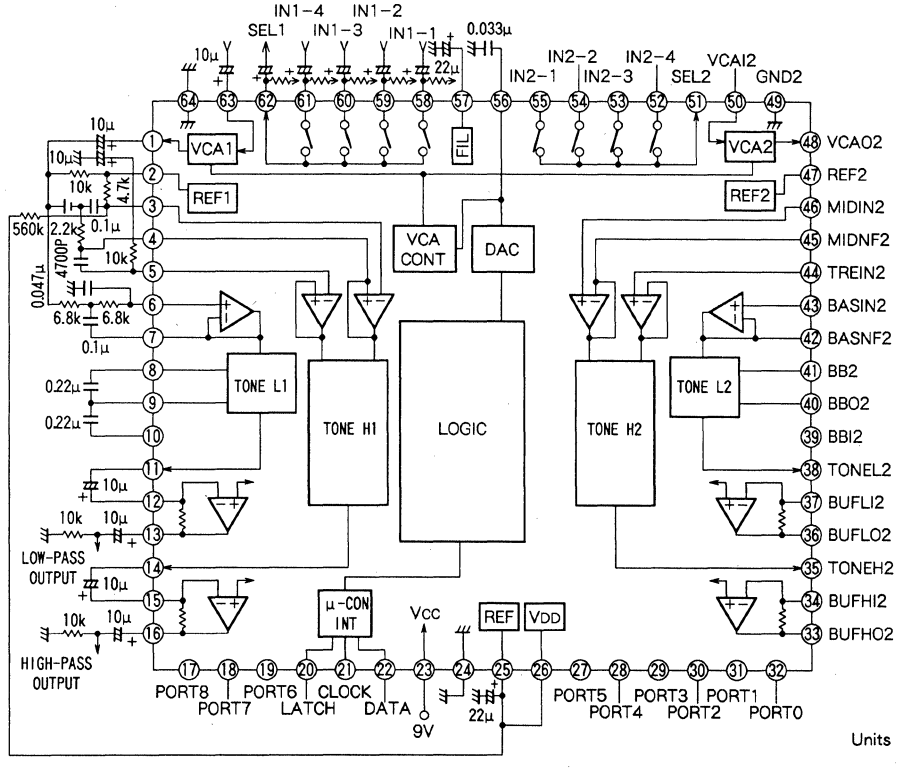
ELECTRONIC SOUND CONTROL WITH ELECTRONIC VOLUME FOR MULTIPLE SOURCES

PIN CONFIGURATION



Outline 64P6N-A

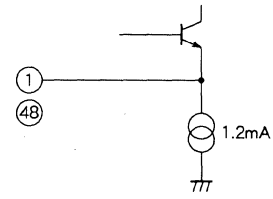
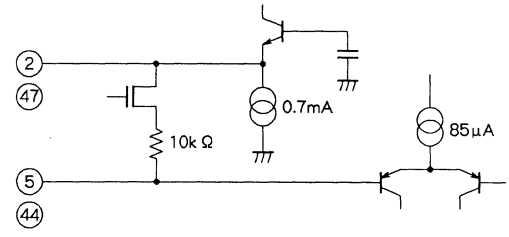
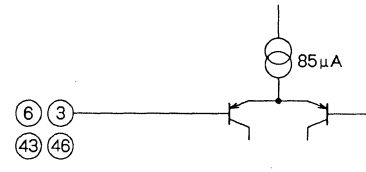
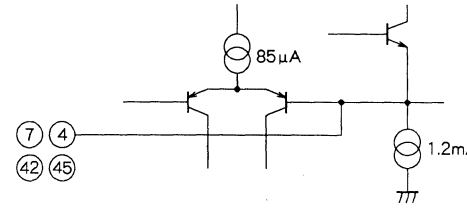
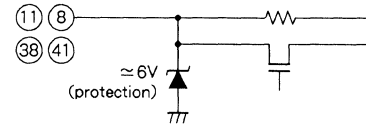
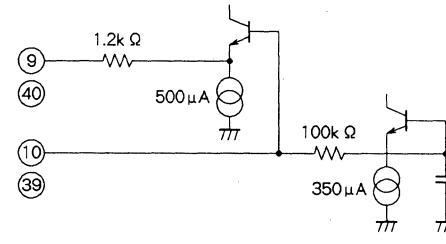
IC INTERNAL BLOCK DIAGRAM



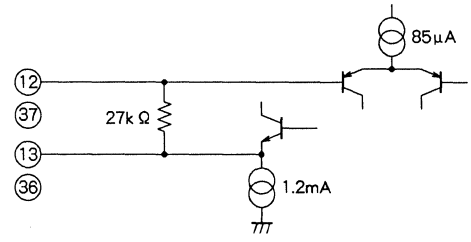
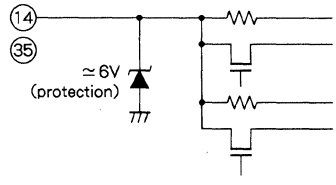
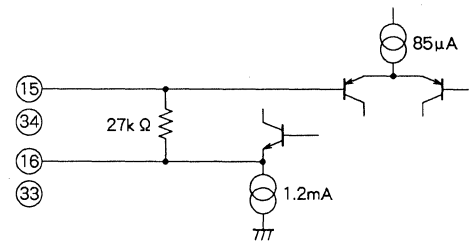
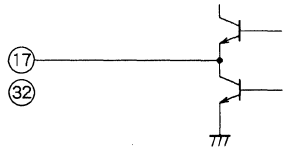
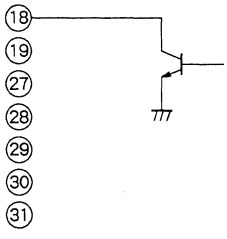
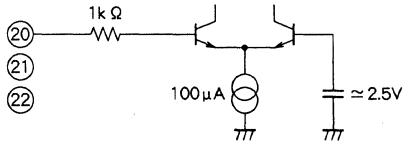
Units Resistance : Ω
Capacitance : F

MITSUBISHI ELECTRIC

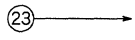
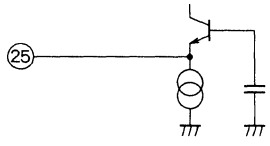
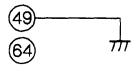
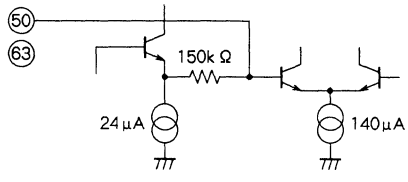
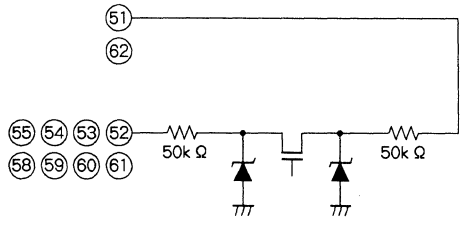
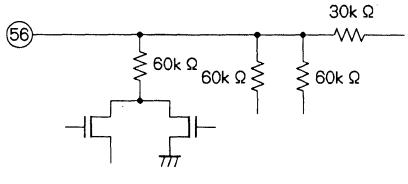
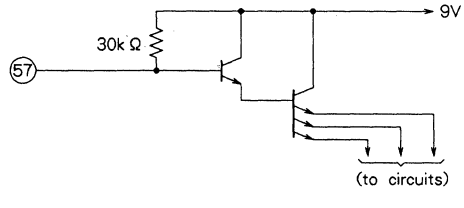
PIN DESCRIPTION

Pin No.	Symbol	DC voltage(V)	I/O	Equivalent circuit
① ㊽	VCAO1 VCAO2	3.5	O	
② ㊼	REF1 REF2	3.5	O	
⑤ ㊹	TREIN1 TREIN2	–	I	
③ ㊻ ⑥ ㊸	MIDIN1 MIDIN2 BISIN1 BISIN2	–	I	
④ ㊺ ⑦ ㊷	MIDNF1 MIDNF2 BASNF1 BASNF2	–	I	
⑧ ㊶	BBI1 BBI2	1.75	–	
⑪ ㊳	TONEL1 TONEL2	1.75	O	
⑨ ㊵	BBO1 BBO2	2.3	O	
⑩ ㊴	BBI1 BBI2	3.0	I	

PIN DESCRIPTION (Continued)

Pin No.	Symbol	DC voltage(V)	I/O	Equivalent circuit
⑫ ㊲	BUFLI1 BUFLI2	3.5	I	
⑬ ㊱	BUFLO1 BUFLO2	3.5	O	
⑭ ㉟	TONEH1 TONEH2	1.75	O	
⑮ ㉞	BUFHI1 BUFHI2	3.5	I	
⑯ ㉝	BUFHO1 BUFHO2	3.5	O	
⑰ ㉜	PORT8 PORT0	H : 4.4 L : 0	O	
⑱ ⑲ ㉗ ㉘ ㉙ ㉚ ㉛	PORT7 PORT6 PORT5 PORT4 PORT3 PORT2 PORT1	–	O	
⑳ ㉑ ㉒	LATCH CLOCK DATA	–	I	

PIN DESCRIPTION (Continued)

Pin No.	Symbol	DC voltage(V)	I/O	Equivalent circuit
㉓	Vcc	9	–	
㉔	GND	0	–	
㉕	REF	5.8	O	
㉖	VDD	–	I	
㊾ ㊹	GND GND	0	–	
㊿ ㊸	VCAI2 VCAI1	3.9	I	
㊶ ㊷	SEL1 SEL2	–	O	
㊷ ㊶ ㊸ ㊵ ㊹ ㊾ ㊺ ㊽	IN2 – 1 IN1 – 1 IN2 – 2 IN1 – 2 IN2 – 3 IN1 – 3 IN2 – 4 IN1 – 4	–	I	
㊻	DAC	0~5.8	O	
㊼	FIL	8.9	I	

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	14	V
V_i	Digital input voltage	− 0.3~7.0	V
P_d	Power dissipation	1000*Standard circuit board	mW
K_θ	Thermal derating	10	mW/℃
T_{opr}	Operating temperature	− 10~+ 70	℃
T_{stg}	Storage temperature	− 40~+ 125	℃

ELECTRICAL CHARACTERISTICS

(Ta = 25℃, V_{CC} = 9V, control data (volume maximum/tone flat) and f = 1kHz unless otherwise noted)

Block name	Symbol	Parameter	Test conditions: Input condition	Number of data	SW conditions: SA1	SA2	SB1	SB2	SC1	SC2	SD	Test point	Limits: Min	Typ	Max	Unit
Power supply	I_{CC}	Circuit current	Quiecet	1	0FF	0FF	0FF	0FF	0FF	0FF	a	PIN23	33	45	57	mA
	V_{REF}	Reference voltage	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN25	5.3	5.8	6.3	V
	V_{FIL}	Filter voltage	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN57	8.2	8.9	−	V
Logic input	I_{IH}	"H" level input current	V_{IH} = 4.5V	−	⇧	⇧	⇧	⇧	⇧	⇧	b	PIN20 PIN21 PIN22	0.3	1	3	μA
	I_{IL}	"L" level input current	V_{IL} = 0.5V	−	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	− 0.3	0	0.3	μA
	V_{IH}	"H" level input voltage	(Recommended condition)	−	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	3.6	4.5	5	V
	V_{IL}	"L" level input voltage	(Recommended condition)	−	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	0	0.5	1.4	V
Logic output	V_{PTH}	PORT0	I_{OH} = − 1mA	1	0FF	0FF	0FF	0FF	0FF	0FF	a	PIN32	3.5	4.4	−	V
	V_{PTL}		I_{OL} = 4mA	2	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN32	−	0.3	0.5	
	I_{P1H}	PORT1	V_{OH} = 9V	1	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN31	−	0	20	μA
	V_{P1L}		I_{OL} = 5mA	3	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN31	−	0	0.5	V
	I_{P2H}	PORT2	V_{OH} = 9V	1	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN30	−	0	20	μA
	V_{P2L}		I_{OL} = 5mA	4	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN30	−	0	0.5	V
	I_{P3H}	PORT3	V_{OH} = 9V	1	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN29	−	0	20	μA
	V_{P3L}		I_{OL} = 5mA	5	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN29	−	0	0.5	V
	I_{P4H}	PORT4	V_{OH} = 9V	1	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN28	−	0	20	μA
	V_{P4L}		I_{OL} = 5mA	6	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN28	−	0	0.5	V
	I_{P5H}	PORT5	V_{OH} = 9V	1	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN27	−	0	20	μA
	V_{P5L}		I_{OL} = 5mA	7	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN27	−	0	0.5	V
	I_{P6H}	PORT6	V_{OH} = 9V	1	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN19	−	0	20	μA
	V_{P6L}		I_{OL} = 5mA	8	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN19	−	0	0.5	V
	I_{P7H}	PORT7	V_{OH} = 9V	1	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN18	−	0	20	μA
	V_{P7L}		I_{OL} = 5mA	9	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN18	−	0	0.5	V
	V_{P8H}	PORT8	I_{OH} = − 1mA	1	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN17	3.5	4.4	−	V
	V_{P8L}		I_{OL} = 4mA	10	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN17	−	0.3	0.5	
	I_{P8OPEN}		V_O = 0V~5V	11	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN17	− 20	−	20	μA
Selector	G_{VS}	Gain	V_i = − 25dBV	12~15	ON	ON	⇧	⇧	⇧	⇧	⇧	A(1), A(2)	− 1.0	0	1.0	dB
	THDs	Total harmonic distortion	Vi=-25dBV, 400Hz~30kHz	12~15	⇧	⇧	⇧	⇧	⇧	⇧	⇧	A(1), A(2)	−	0.01	0.1	%
	THDsmax	Maximum total harmonic distortion	Vi=-14dBV, 400Hz~30kHz	12~15	⇧	⇧	⇧	⇧	⇧	⇧	⇧	A(1), A(2)	−	0.1	1.0	%
Switching offset	OFSTM1	Treble/mid switching offset voltage	No signals (measure of data switching offset)	16→17	0FF	0FF	⇧	⇧	⇧	⇧	⇧	PIN14 PIN35	− 20	0	+ 20	mV
	OFSBB1	Boost switching offset voltage 1	⇧	1→18	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN8 PIN41	− 10	0	+ 10	mV
	OFSBB2	Boost switching offset voltage 2	⇧	1→19	⇧	⇧	⇧	⇧	⇧	⇧	⇧	PIN8 PIN41	− 10	0	+ 10	mV

ELECTRICAL CHARACTERISTICS (Continued)

Block name	Symbol	Parameter	Test conditions: Input condition	Number of data	SW conditions: SA 1	SA 2	SB 1	SB 2	SC 1	SC 2	SD	Test point	Limits: Min	Typ	Max	Unit
Channel balance	CBVT	Total channel balance 1	–	–	–	–	–	–	–	–	–	CB + CBT	− 3	0	3	dB
	CBVM	Total channel balance 2	–	–	–	–	–	–	–	–	–	CB + CBM	− 3	0	3	dB
	CBVB	Total channel balance 3	–	–	–	–	–	–	–	–	–	CB + CBBA	− 3	0	3	dB
Electronic volume	ATT(min)	Minimum attenuation level	Reference①Vi=−14dBV	1	OFF	OFF	ON	ON	OFF	OFF	a	B(1),B(2)	7.2	9	10.8	dB
	CB	Channel balance	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	B(1)/B(2)	− 1.8	0	1.8	dB
	THD	Total harmonic distortion	Vi = − 14dBV, BPF = 400Hz~30kHz①	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	B(1),B(2)	–	0.02	0.1	%
	No(min)	Noise voltage	Quiecet, JIS − A	⇧	⇧	⇧	OFF	OFF	⇧	⇧	⇧	⇧	–	25	56	μVrms
	THDmax	Maximum total harmonic distortion	Vi = − 3dBV, BPF = 400Hz~30kHz①	1	⇧	⇧	ON	ON	⇧	⇧	⇧	⇧	–	0.1	1.0	%
	ATT(−10)	Attenuation(−10dB)	Reference①Vi=−14dBV	20	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	− 2.8	− 1.0	0.8	dB
	ATT(max)	Maximum attenuation	Vi = − 3dBV, JIS − A①	21	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	–	− 97	− 77	dB
	No	Noise voltage under maximum attenuation	Quiecet, JIS − A	21	⇧	⇧	OFF	OFF	⇧	⇧	⇧	B(1),B(2)	–	10	20	μVrms
	CT	Crosstalk	Vi = − 3dBV, JIS − A①	1	⇧	⇧	OFF ON	ON OFF	⇧	⇧	⇧	B(1) B(2)	–	− 90	− 70	dB
Treble	GVT	Gain	Reference②Vi=−14dBV	1	OFF	OFF	OFF	OFF	ON ab=ON	ON ab=ON	a	D(1),D(2)	− 6	− 4	− 2	dB
	CBT	Channel balance	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	D(1)/D(2)	− 2	0	+ 2	dB
	THDH	Total harmonic distortion	⇧ BPF = 400Hz~30kHz	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	D(1),D(2)	–	0.01	0.1	%
	NoT	Noise voltage	Quiecet, JIS − A	1	⇧	⇧	⇧	⇧	OFF	OFF	⇧	⇧	–	11	22	μVrms
	THDTmax	Maximum total harmonic distortion	Vi = − 6dBV, BPF = 400Hz~30kHz②	22	⇧	⇧	⇧	⇧	ON ab=ON	ON ab=ON	⇧	⇧	–	0.1	1	%
	GVT(max)	Maximum gain	Reference②Vi=−14dBV	22	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	+ 10	+ 12	+ 14	dB
	GVT(min)	Minimum gain	⇧	23	⇧	⇧	⇧	⇧	⇧	⇧	⇧	D(1),D(2)	− 16	− 14	− 12	dB
	CTT	Crosstalk	Reference Vi=−6dBV JIS-A②	22	⇧	⇧	⇧	⇧	OFF ON	ON OFF	⇧	D(1) D(2)	–	− 80	− 60	dB
Mid	GVM	Gain	Reference③Vi=−14dBV	1	OFF	OFF	OFF	OFF	ON ab=ON	ON ab=ON	a	D(1),D(2)	− 6	− 4	− 2	dB
	CBM	Channel balance	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	D(1)/D(2)	− 2	0	+ 2	dB
	THDM	Total harmonic distortion	⇧ BPF = 400Hz~30kHz	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	D(1),D(2)	–	0.01	0.1	%
	NoM	Noise voltage	Quiecet, JIS − A	1	⇧	⇧	⇧	⇧	OFF	OFF	⇧	⇧	–	11	22	μVrms
	THDMmax	Maximum total harmonic distortion	Vi = 0dBV, BPF = 400Hz~30kHz③	24	⇧	⇧	⇧	⇧	ON ab=ON	ON ab=ON	⇧	⇧	–	0.1	1	%
	GVM(max)	Maximum gain	Reference③Vi=−14dBV	24	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	+ 4	+ 6	+ 8	dB
	GVM(min)	Minimum gain	⇧	25	⇧	⇧	⇧	⇧	⇧	⇧	⇧	D(1),D(2)	− 16	− 14	− 12	dB
	CTM	Crosstalk	Reference Vi=−6dBV JIS-A③	24	⇧	⇧	⇧	⇧	OFF ON	ON OFF	⇧	D(1) D(2)	–	− 80	− 60	dB
Bass	GVBA	Gain	Reference④Vi=−14dBV	1	OFF	OFF	OFF	OFF	ON C=ON	ON C=ON	a	C(1),C(2)	− 6	− 4	− 2	dB
	CBBA	Channel balance	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	C(1)/C(2)	− 2	0	+ 2	dB
	THDBA	Total harmonic distortion	⇧ BPF = 400Hz~30kHz	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	C(1),C(2)	–	0.01	0.1	%
	NoBA	Noise voltage	Quiecet, JIS − A	1	⇧	⇧	⇧	⇧	OFF	OFF	⇧	⇧	–	10	20	μVrms
	THDBAmax	Maximum total harmonic distortion	Vi = − 6dBV, BPF = 400Hz~30kHz④	26	⇧	⇧	⇧	⇧	ON C=ON	ON C=ON	⇧	⇧	–	0.1	1	%
	GVBA(max)	Maximum gain	Reference④Vi=−14dBV	26	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	10	12	14	dB
	GVBA(min)	Minimum gain	⇧	27	⇧	⇧	⇧	⇧	⇧	⇧	⇧	C(1),C(2)	− 16	− 14	− 12	dB
	CTBA	Crosstalk	Reference Vi=−6dBV JIS-A④	26	⇧	⇧	⇧	⇧	OFF ON	ON OFF	⇧	C(1) C(2)	–	− 80	− 60	dB
	THDBBmax	Boost maximum total harmonic distortion	Vi = − 22dBV, BPF = 400Hz~30kHz④	28	⇧	⇧	⇧	⇧	ON C=ON	ON C=ON	⇧	C(1),C(2)	–	0.1	1	%
	GVBB(max)	Boost maximum total harmonic gain	Vi = − 10dBV④	18	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	10	12	14	dB
	GVBB(min)	Boost minimum total harmonic gain	⇧	19	⇧	⇧	⇧	⇧	⇧	⇧	⇧	C(1),C(2)	− 22	− 20	− 18	dB

Note 1. Vi : Input voltage ①= VCA, ②= HPF, ③= BPF, ④= LPF

DIGITAL CONTROL SPECIFICATIONS

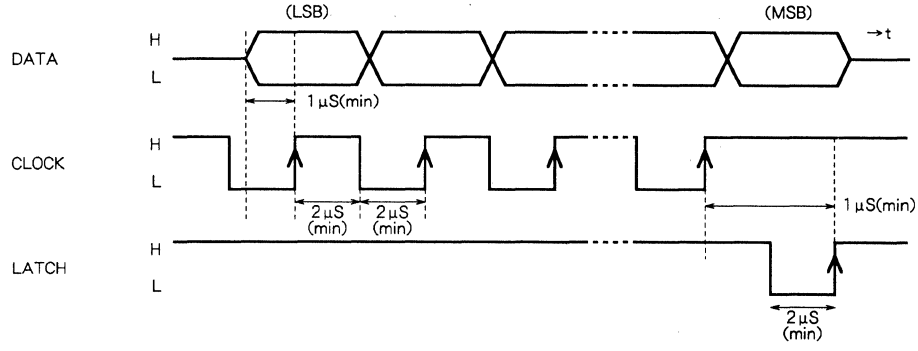
Data format (Refer to data setting table in the next page)

	8bit	4bit	4bit	4bit	4bit	4bit									2bit		
MSB	Volume	Treble	Mid	Bass	Super bass	SEL				PORT 0	PORT 1	PORT 2	PORT 3	PORT 4	PORT 5	PORT 6	PORT 7	PORT8		LSB
						1	2	3	4									1	2	

VOLUME : 00~FF (8BIT D/A DATA)
TREBLE : 0~D (14 STEPS)
MID : 0~A (11 STEPS)
BASS : 0~D (14 STEPS)
SUPER BASS : 0
1~5
9~D

SEL : 4BITS FOR INPUT SWITCHING
PORT0 : TTL OUTPUT
PORT1~7 : OPEN COLLECTOR OUTPUT
PORT8 : 2BITS ; 3-STATE OUTPUT

TIMING CHART (Recommended conditions)



Note 1. CLOCK and LATCH are operat at rising edges of pulse.
2. Logic input buffer threshold voltage is about 2.5V.

VCA, tone data setting table

D/A converter for VCA		Treble		Mid		Bass		Super bass	
Data	Setting	Data	Setting	Data	Setting	Data	Setting	Data	Setting
00	V_Z	0	− 10dB	0	− 10dB	0	− 10dB	0	± 0dB
01	$\frac{255V_Z + V_F}{256}$	1	− 8dB	1	− 8dB	1	− 8dB	1	− 2dB
⋮	⋮	2	− 6dB	2	− 6dB	2	− 6dB	2	+ 4dB
		3	− 4dB	3	− 4dB	3	− 4dB	3	+ 6dB
		4	− 2dB	4	− 2dB	4	− 2dB	4	+ 9dB
		5	± 0dB	5	± 0dB	5	± 0dB	5	+ 12dB
		6	+ 2dB	6	+ 2dB	6	+ 2dB	6	−
		7	+ 4dB	7	+ 4dB	7	+ 4dB	7	−
		8	+ 6dB	8	+ 6dB	8	+ 6dB	8	−
		9	+ 8dB	9	+ 8dB	9	+ 8dB	9	− 2dB
		A	+ 10dB	A	+ 10dB	A	+ 10dB	A	− 4dB
		B	+ 12dB	B	−	B	+ 12dB	B	− 6dB
		C	+ 14dB	C	−	C	+ 14dB	C	− 9dB
		D	+ 16dB	D	−	D	+ 16dB	D	− 12dB
FE	$\frac{2V_Z + 254V_F}{256}$	E	−	E	−	E	−	E	−
FF	$\frac{V_Z + 255V_F}{256}$	F	−	F	−	F	−	F	−

Note 1. All data is design values. V_Z and V_F are internal power supply voltages. Between +12dB and +16dB of treble and bass are for loudness control.
2. Data is shown by the hexadecimal notation.

Input selector, output port data setting table

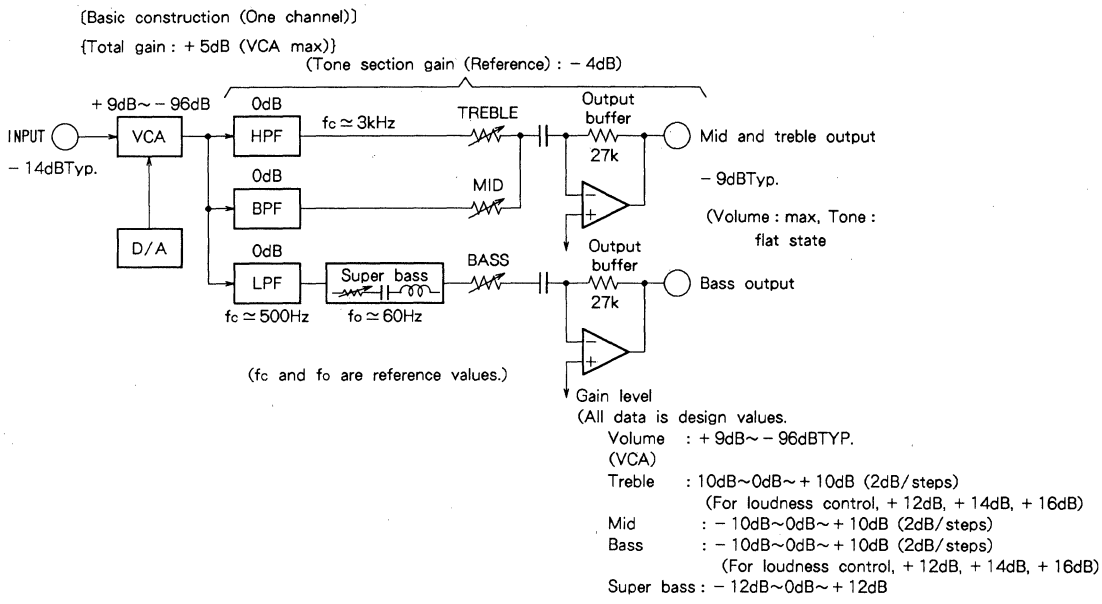
SELECTOR					PORT 0		PORT 1~7		PORT8		
Data				Input mode	Data	Output TTLOUT	Data	Output open collector	Data		Output
1	2	3	4						1	2	
L	L	L	H	IN1 − 4, IN2 − 4	H	H(TTL)	H	OPEN	H	H	H(TTL)
L	L	H	L	IN1 − 3, IN2 − 3	L	L(TTL)	L	CLOSE	H	L	L(TTL)
L	H	L	L	IN1 − 2, IN2 − 2	−	−	−	−	L	Note3	High Inpedance
H	L	L	L	IN1 − 1, IN2 − 1	−	−	−	−	−	−	−

Note 3. "L" or "H"

VCA attenuation (Reference)

Control data (D/A converter)	VCA attenuation (dB)
0F	(maximum attenuation)
1F	− 79
2F	− 59
3F	− 44
4F	− 32
5F	− 23
6F	− 15
7F	− 9
8F	− 4
9F	0
AF	+ 3
BF	+ 5
CF	+ 6
DF	+ 7
EF	+ 8
FF	+ 9

ANALOG SIGNAL PROCESSING



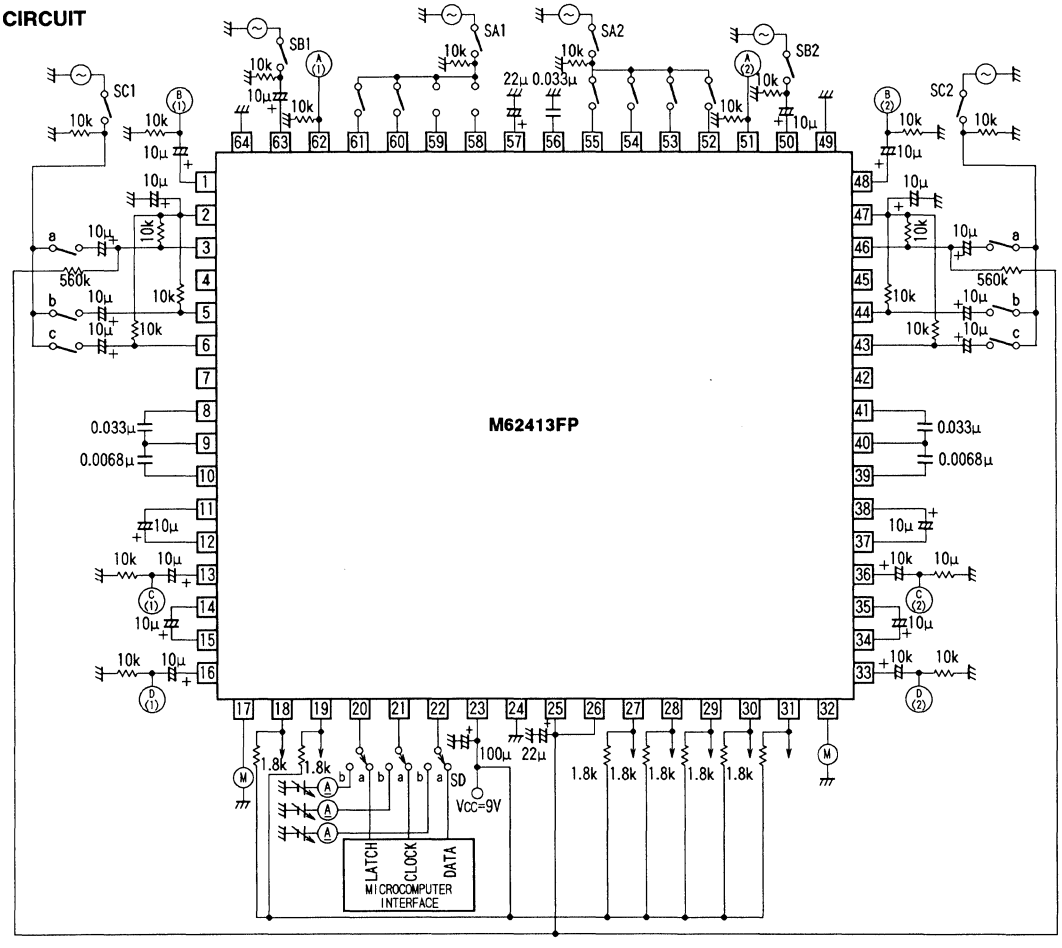
Data setting table

Data No.	Control data																			
	Volume, tone (indicate hexadecimal)						Input selector and output port (indicate binaries)													
	VCA		Treble	Mid	Bass	Super bass	Input selector				PORT 0	PORT 1	PORT 2	PORT 3	PORT 4	PORT 5	PORT 6	PORT 7	PORT 8	
1	F	F	5	5	5	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0	1	↓	↓	↓	↓	↓	↓	↓	↓
3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1	0	1	↓	↓	↓	↓	↓	↓	↓
4	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1	0	1	↓	↓	↓	↓	↓	↓
5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1	0	1	↓	↓	↓	↓	↓
6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1	0	1	↓	↓	↓	↓
7	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1	0	1	↓	↓	↓
8	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1	0	1	↓	↓
9	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1	0	↓	1
10	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1	1	0
11	↓	↓	↓	↓	↓	↓	0	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0	0
12	↓	↓	↓	↓	↓	↓	1	0	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1	1
13	↓	↓	↓	↓	↓	↓	0	1	0	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
14	↓	↓	↓	↓	↓	↓	↓	0	1	0	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
15	↓	↓	5	5	↓	↓	↓	↓	0	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
16	↓	↓	D	0	↓	↓	↓	↓	↓	0	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
17	↓	↓	0	A	↓	0	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
18	↓	↓	5	5	↓	5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
19	F	F	↓	↓	↓	D	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
20	9	8	↓	↓	↓	0	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
21	0	0	5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
22	F	F	D	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
23	↓	↓	0	5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
24	↓	↓	5	A	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
25	↓	↓	↓	0	5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
26	↓	↓	↓	5	D	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
27	↓	↓	↓	↓	0	0	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
28	F	F	5	5	D	5	0	0	0	0	1	1	1	1	1	1	1	1	1	1

M62413FP

ELECTRONIC SOUND CONTROL WITH ELECTRONIC VOLUME FOR MULTIPLE SOURCES

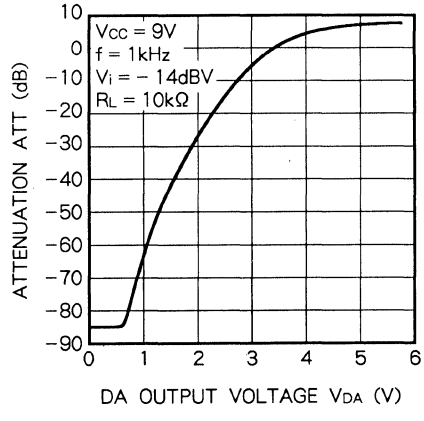
TEST CIRCUIT



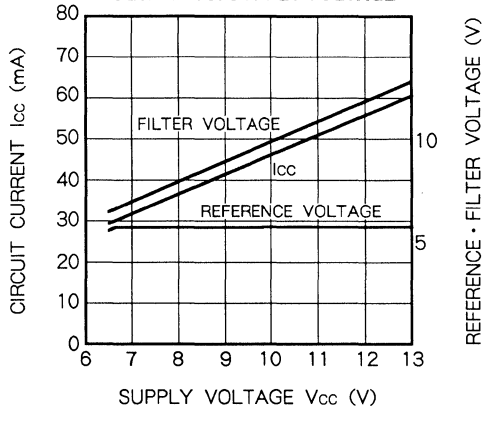
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

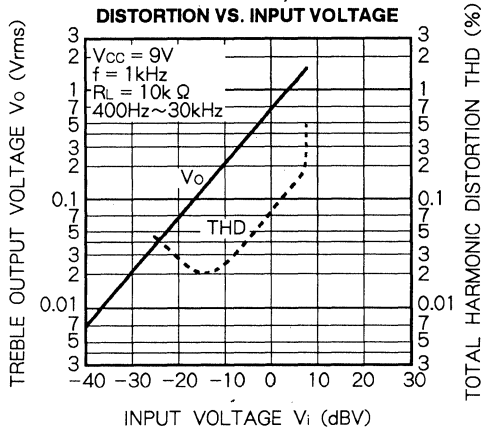
VCA ATTENUATION VS. DA OUTPUT VOLTAGE



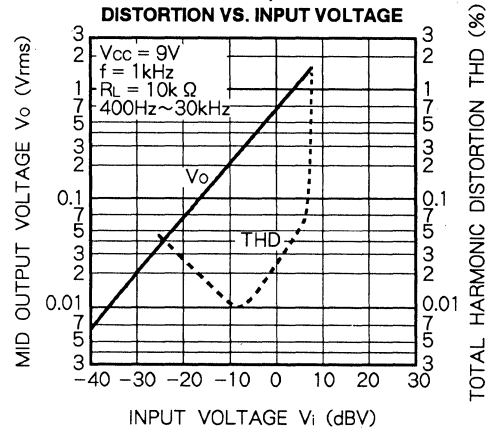
CIRCUIT CURRENT, REFERENCE·FILTER VOLTAGE VS. SUPPLY VOLTAGE



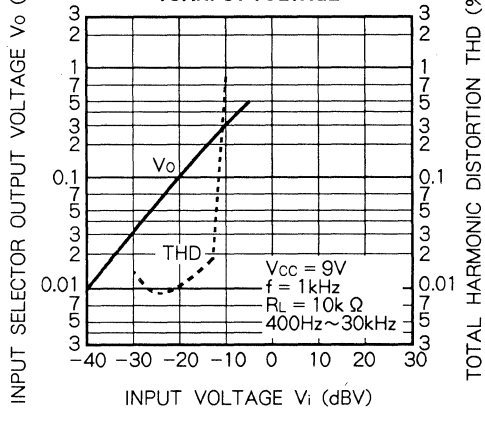
TREBLE OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION VS. INPUT VOLTAGE



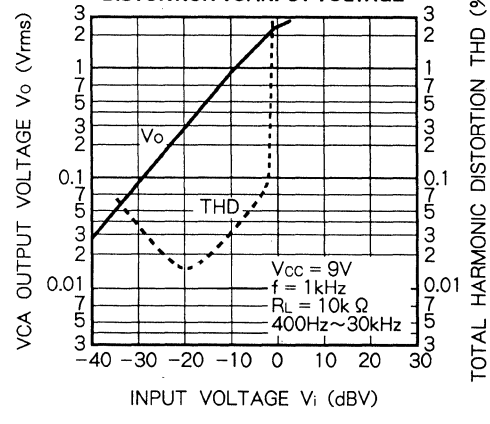
MID OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION VS. INPUT VOLTAGE



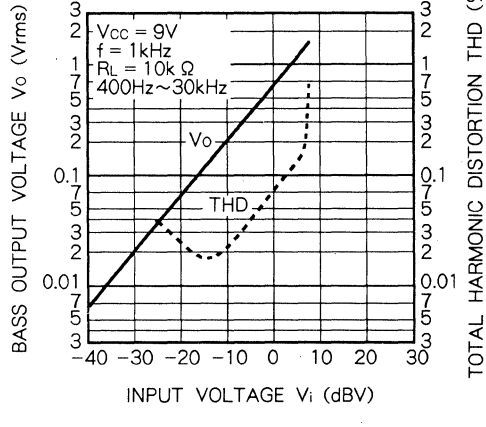
INPUT SELECTOR OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION VS. INPUT VOLTAGE



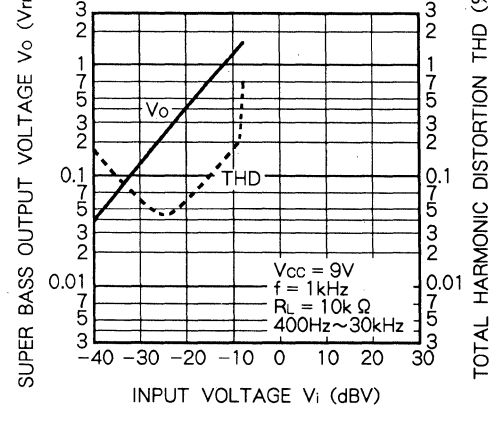
VCA OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION VS. INPUT VOLTAGE



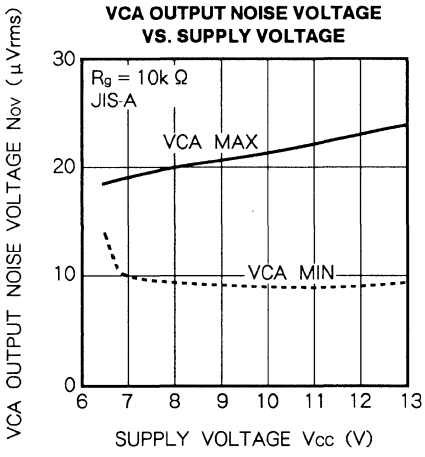
BASS OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION VS. INPUT VOLTAGE



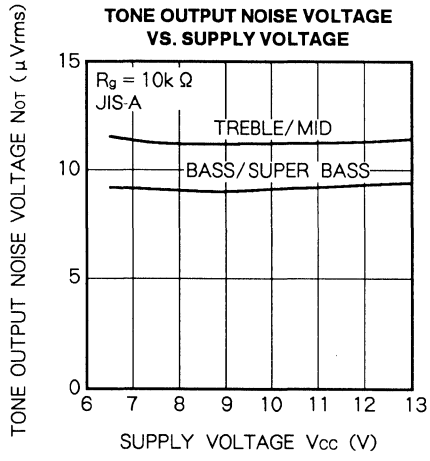
SUPER BASS OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION VS. INPUT VOLTAGE



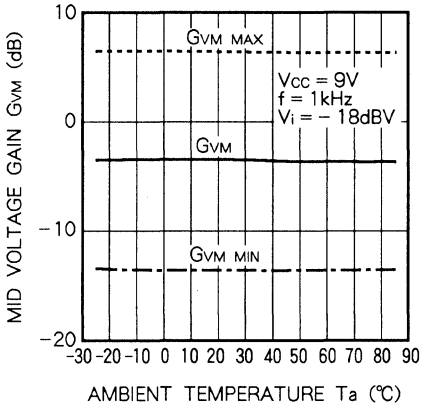
VCA OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



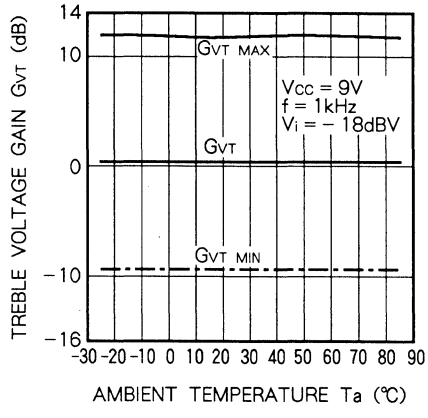
TONE OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



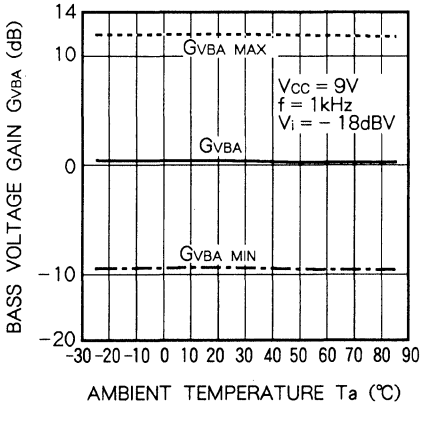
MID VOLTAGE GAIN VS. AMBIENT TEMPERATURE



TREBLE VOLTAGE GAIN VS. AMBIENT TEMPERATURE



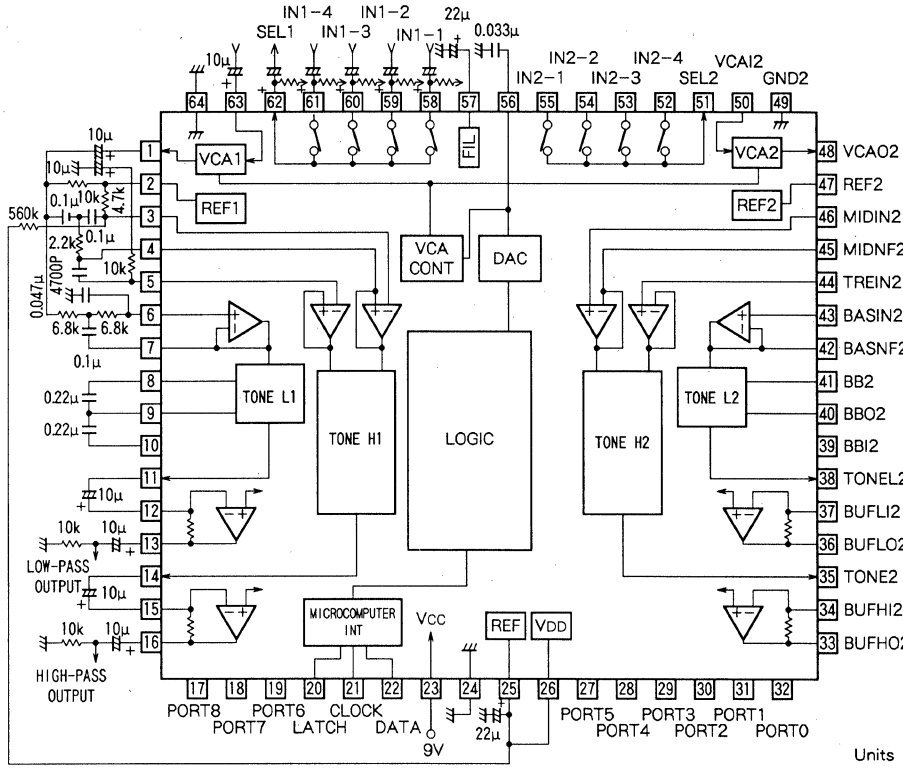
BASS VOLTAGE GAIN VS. AMBIENT TEMPERATURE



M62413FP

ELECTRONIC SOUND CONTROL WITH ELECTRONIC VOLUME FOR MULTIPLE SOURCES

APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

M62414SP

2CH, 4 OUTPUT ELECTRONIC VOLUME WITH MICROCOMPUTER INTERFACE

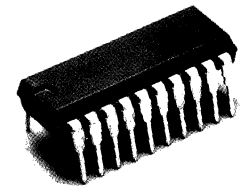
DESCRIPTION

The M62414SP voltage controlled amplifier integrated circuit was developed for electronic volume control in audio-visual equipment. It is used as the main volume control in the power amplifier front stage.

This IC has 2 modes : One is connected to a microcomputer interface circuit and controlled by serial data. The other is controlled by external direct current voltage. This IC also has 4 built-in output ports, enabling various applications such as car audio equipment.

FEATURES

- Built-in VCA circuit for volume control
- Volume adjustable range ····· – 105dB~0dB
- VCA maximum gain switchable between 0dB or – 6dB
- VCA can be controlled externally
- Open collector type output ports (NPN transistors)
- Maximum allowable input ····· 2Vrms
- Built-in microcomputer interface circuit controlled by 8-bit serial data
- Communication with microcomputer via two lines (CLOCK and DATA)

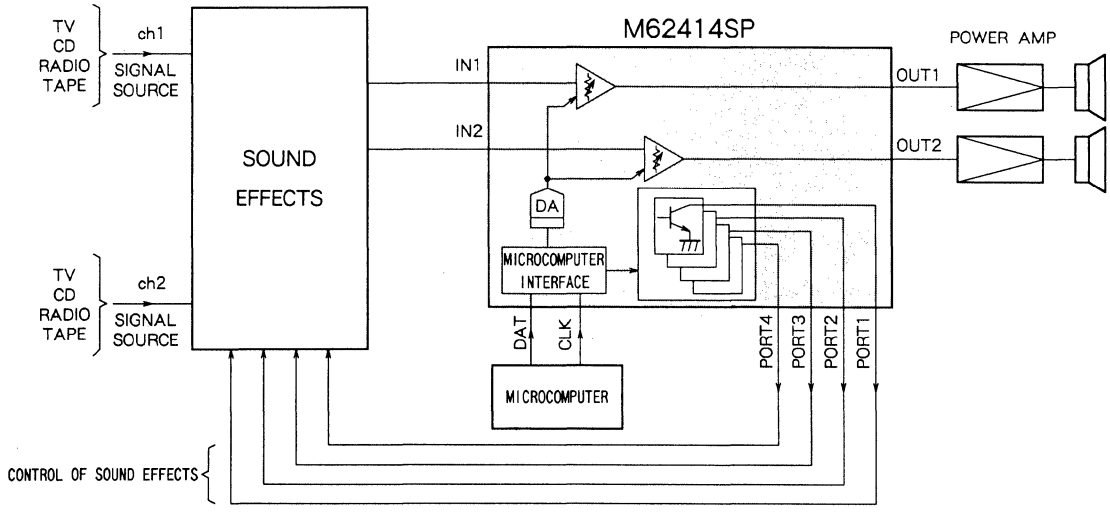


Outline 20P4B
1.778mm pitch 300mil SDIP
(6.3mm × 19.0mm × 3.3mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC} = 7~13V
Rated supply voltage ····· V_{CC} = 9V

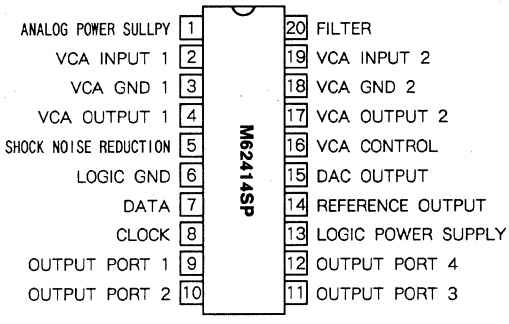
SYSTEM CONFIGURATION



M62414SP

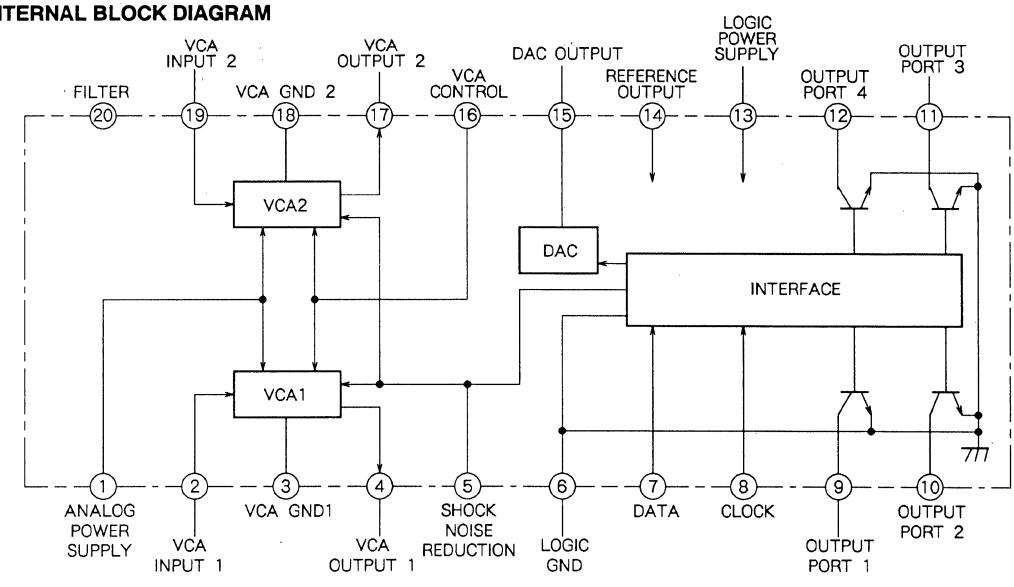
2CH, 4 OUTPUT ELECTRONIC VOLUME WITH MICROCOMPUTER INTERFACE

PIN CONFIGURATION



Outline 20P4B

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin No.	Name	Function
①	Analog power supply	Applies 7V~13V.(Rated voltage : 9V)
②	VCA input 1	Channel 1 signal input pin
③	VCA GND1	Grounding
④	VCA output 1	Channel 1 singnal output pin
⑤	Shock noise reduction	Shock noise generated by VCA gain switching is reduced with external capacitor
⑥	Logic GND	Grounding
⑦	DATA	Serial data transimission from microcomputer to IC (LSB first)
⑧	CLOCK	Clock pulses for serial data transmission from microcomputer to IC (LSB first)
⑨	Output port 1	Open collector output pin 1
⑩	Output port 2	Open collector output pin 2
⑪	Output port 3	Open collector output pin 3
⑫	Output port 4	Open collector output pin 4
⑬	Logic power supply	Applies 7V~13V.(Rated voltage : 9V)
⑭	Reference output	Reference voltage output pin (4V typ)
⑮	DAC output	Voltage output pin for VCA control
⑯	VCA control	VCA control pin (0~4V)
⑰	VCA output 2	Channel 2 singnal output pin
⑱	VCA GND2	Grounding
⑲	VCA input 2	Channel 2 signal input pin
⑳	Filter	For power supply ripple removal

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{CC(max)}$	Supply voltage	+ 15	V
P_d	Power dissipation	1000	mW
K_θ	Thermal derating	10.0	mW/℃
T_{opr}	Operating temperature	−20~+75	℃
T_{stg}	Storage temperature	−40~+125	℃

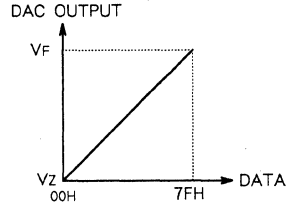
ELECTRICAL CHARACTERISTICS (V_{CC} = 9V, f = 1kHz, V_{in} = 1Vrms, unless otherwise noted)

Block	Symbol	Parameter	Test conditions	Control data 1 Mode select="0"	Control data 2 Mode select = "1" D0	D1	D2	D3	D4	D5	D6	Limits Min	Typ	Max	Unit
Power supply	IccA	Circuit current (analog)	No signals	7FH	0	0	0	0	0	0	0	6	13	25	mA
	IccL	Circuit current (logic)	No signals	7FH	0	0	0	0	0	0	0	5	11	23	mA
Electronic volume	ATT(min)	Minimum attenuation		7FH	0	0	0	0	0	0	0	−2	0	+2	dB
	ATT-6	Attenuation (−6dB)	VCA GAIN = −6dB	7FH	0	0	0	0	0	0	1	−8	−6	−4	dB
	ATT(max)	Maximum attenuation	Vin = 2Vrms, JIS-A	00H	0	0	0	0	0	0	1	−	−105	−85	dB
	CB	Channel balance		7FH	0	0	0	0	0	0	0	−2	0	+2	dB
	THD	Total harmonic distortion	15kHz LPF	7FH	0	0	0	0	0	0	0	−	0.03	0.1	%
	Ri	Input resistance		7FH	0	0	0	0	0	0	0	50	150	−	kΩ
	No(min)	Output noise voltage (min)	Rg=10kΩ, no signals, JIS-A	7FH	0	0	0	0	0	0	0	−	9	20	μVrms
	No(max)	Output noise voltage (max)	Rg=10kΩ, no signals, JIS-A	00H	0	0	0	0	0	0	0	−	4.8	10	μVrms
	Vimax	Maximum input voltage	THD = 1%	7FH	0	0	0	0	0	0	0	1	2	−	Vrms
	Vomax	Maximum output voltage	THD = 1%	7FH	0	0	0	0	0	0	0	1	2	−	Vrms
	CT	Cross talk	Rg=0Ω Vin=2Vrms, JIS-A	7FH	0	0	0	0	0	0	0	−	−102	−80	dB
PORT 1~4	IOH	Output port high level current	VOH = 9V	7FH	0	0	0	0	0	0	0	0	−	10	μA
	VOL	Output port low level voltage	IOL = 5mA	7FH	1	1	1	1	0	0	0	0	0.15	0.5	V
Logic input	ICH	CLOCK input current	VCH = 5V									0.3	1.0	3.0	μA
	ICL		VCL = 0V									−0.3	0.0	0.3	μA
	IDH	DATA input current	VDH = 5V									0.3	1.0	3.0	μA
	IDL		VDL = 0V									−0.3	0.0	0.3	μA
	VCH	CLOCK	"H"level voltage	Recommended conditions								3.5	−	5.5	V
	VCL		"L"level voltage	Recommended conditions								0.0	−	1.5	V
	VDH	DATA	"H"level voltage	Recommended conditions								3.5	−	5.5	V
	VDL		"L"level voltage	Recommended conditions								0.0	−	1.5	V

DIGITAL CONTROL SPECIFICATIONS

Data format

	D7	D6	D5	D4	D3	D2	D1	D0	
DATA 1 (MSB)	MODE SELECT 0			DAC DATA (7 bit)					(LSB)
DATA 2 (MSB)	MODE SELECT 1	VCA GAIN	"0"	"0"	OUT4	OUT3	OUT2	OUT1	(LSB)

	Signal name	Function
D0	DAC	DAC data (7 bits) For VCA control voltage output 00H~7FH 
D1		
D2		
D3		
D4		
D5		
D6		
D7	Mode select	"0" : Data 1 is selected

	Signal name	Function
D0	OUT1	For control of output port 1 "0" : High impedance "1" : Current intake
D1	OUT2	For control of output port 2 "0" : High impedance "1" : Current intake
D2	OUT3	For control of output port 3 "0" : High impedance "1" : Current intake
D3	OUT4	For control of output port 4 "0" : High impedance "1" : Current intake
D4	Not defined	D4 set to "0" D5 set to "0"
D5		
D6	VCA GAIN	"0" VCA gain···0dB "1" VCA gain···– 6dB
D7	Mode select	"1" : Data 2 is selected

Note 1. When power is turned on, internal data is reset to "0"

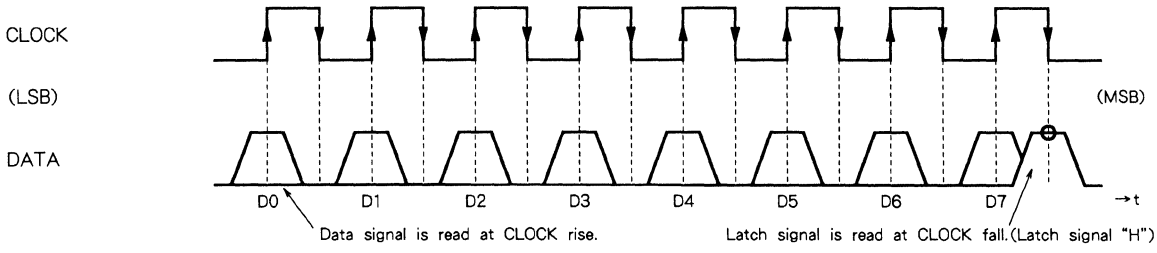
DATA SETTING TABLE

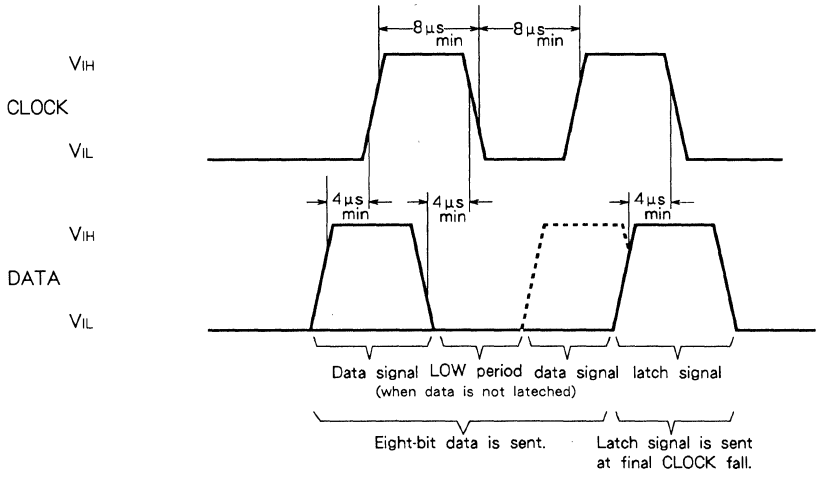
VCA D/A converter	Data	00	01	----------	7E	7F
	Setting	V_Z	$\frac{127V_Z + V_F}{128}$	----------	$\frac{2V_Z + 126V_F}{128}$	$\frac{V_Z + 127V_F}{128}$

Note 2. V_Z is in reference to GND potential. V_F is based on the reference output (⑭pin).

DATA TIMING (Recommended conditions)

* Data communication : LSB first





Note 1. Set CLOCK input and DATA input V_{IL} and V_{IH} to between 0V and 5.5V.
2. Logic input buffer threshold voltage is approximately 2.5V.

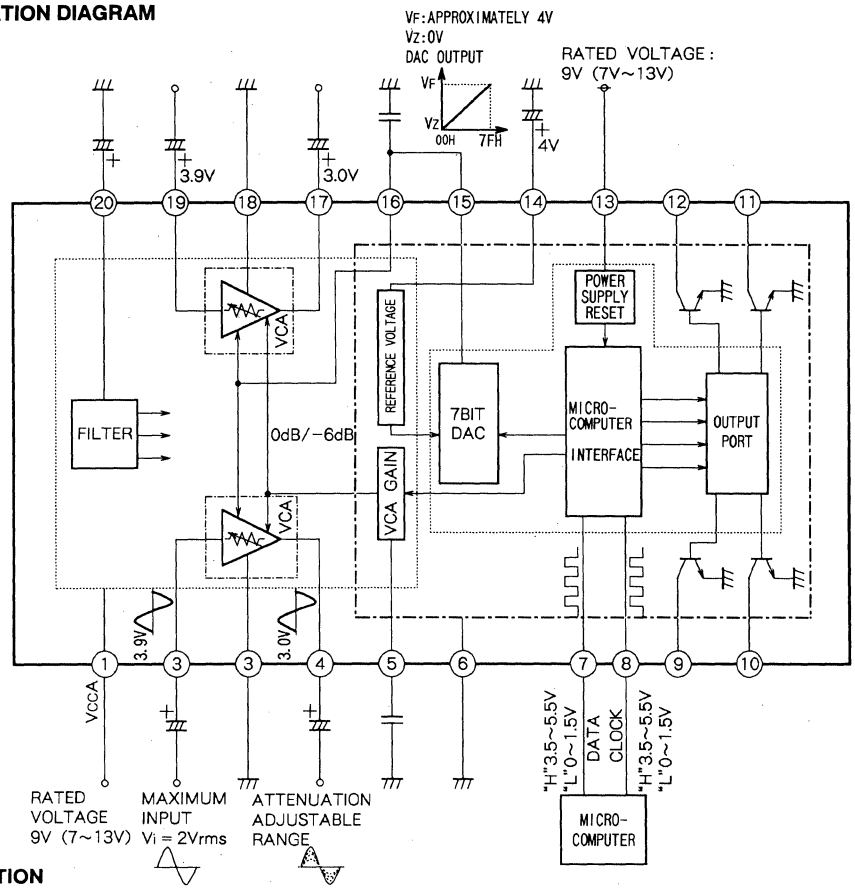
VCA ATTENUATION (Reference)

VCA gain(max = 0dB)	
Control data (D/A converter)	VCA attenuation (dB)
2FH	−14.0
37H	−9.0
3FH	−6.0
47H	−4.0
4FH	−2.5
57H	−1.5
5FH	−1.0
67H	−0.5
6FH	0
7FH	0

Note 3. At the data switching points of 0FH→10H, 1FH→20H, 2FH→30H, 3FH→40H, 4FH→50H, 5FH→60H, 6FH→70H, DAC error becomes large. Care should be taken when these switch points are used continuosly.

VCA gain(max = − 6dB)	
Control data (D/A converter)	VCA attenuation (dB)
0FH	Maximum attenuation
17H	−74
1FH	−61
27H	−52
2FH	−44
37H	−37
3FH	−29
47H	−24
4FH	−20
57H	−17
5FH	−14
67H	−11
6FH	−9
77H	−7
7FH	−6

BLOCK OPERATION DIAGRAM



BASIC OPERATION

(1) VCA block : This block consists of a VCA circuit, and handles main analog signals.

①Input signals are output after attenuated by the VCA circuit.

②VCA maximum gain can be set to 0dB or − 6dB

- MAX gain 0dB : In areas where attenuation is small, signals are attenuated little by little.(In areas where attenuation is large, signals are attenuated largely in response to conrolled voltage variation.
- MAX gain − 6dB : In areas where attenuation is large, signals are attenuated more modestly in responese to controlled voltage variation than when the maximum gain is set to 0dB.

To finely control signals, set maximum gain to 0dB where attenuation is small, and to − 6dB where attenuation is large.

③VCA circuit is controlled by DC voltage applied to pin ⑯. Control DC voltage is output from the 7bit D-A converter in the IC.

(2) Control block : This block processes data from microcomputer to control functions.

①When power is turned on, resetting signal is output from reset circuit, and internal logoc is automatically set to the following conditions : DAC control data, 00H (maximum attenuation), VCA gain, 0dB, and output port, high-impedance. Reset is not canceled unitil supply voltage exceeds 4V, therefore, start data transmission after supply voltage reaches the recommended operational range.

②Functions are controlled with 8bit serial data from microcomputer. To control DAC, select data 1 (mode select "0"). To set output port and VCA gain, select data 2 (mode select "1"). For data setting details, refer to digital control specifications on page 9.

(3) Output port block : This block includes 4 output ports.

①The ports are the current intake open collector type (NPN transistors).

②After power is turned on, the status of output ports is retained at high impedance until first data arrives.

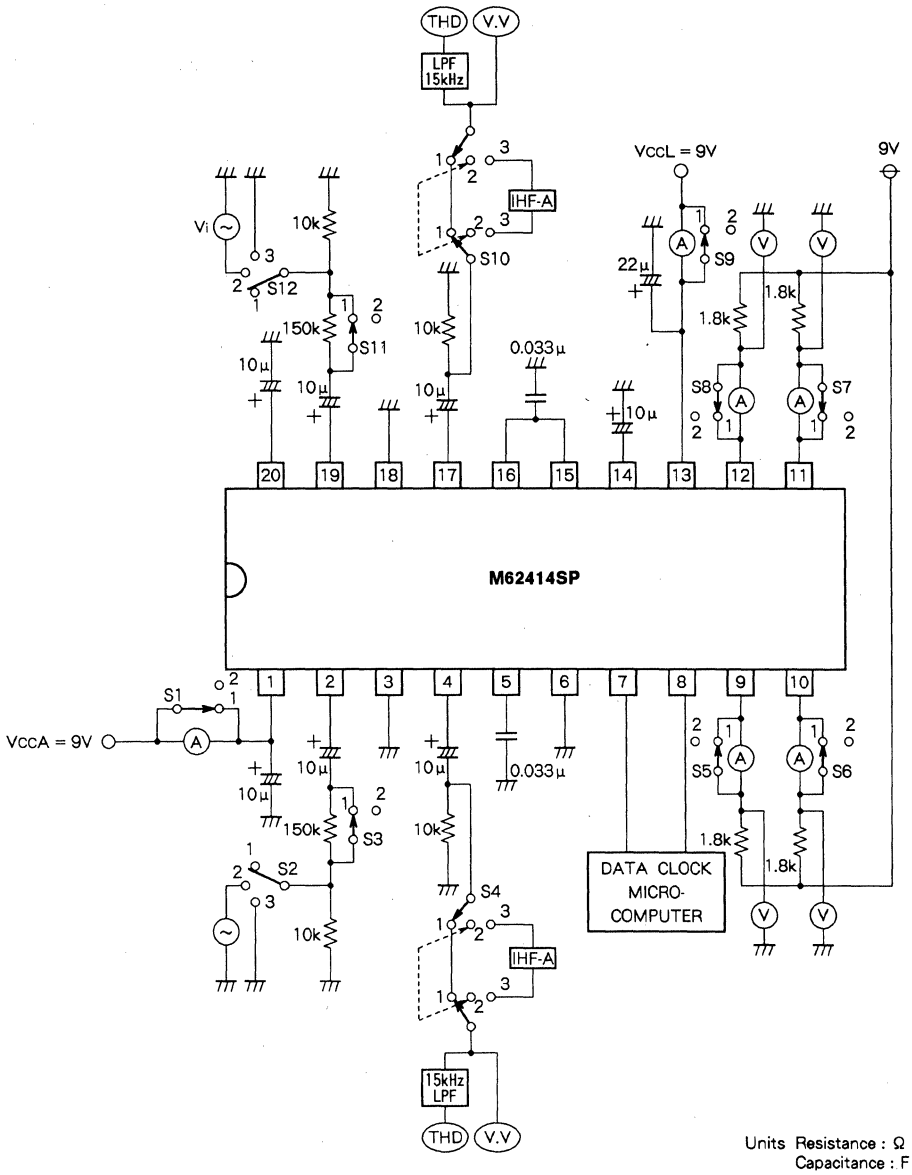
③Four output ports can be set independently according to control data.

SWITCHING CONDITIONS AND TEST METHODS

Symbol	Parameter	Switching conditions												Test method
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	
I_{CCA}	Circuit currnet (analog)	2	1	1	1	1	1	1	1	1	1	1	1	Current that runs at pin① is measured when there are no signals.
I_{LLL}	Circuit current (logic)	1	1	1	1	1	1	1	1	2	1	1	1	Current that runs at pin⑬ is measured when there are no signals.
$A_{TT(min)}$	Minimum attenuation	1	2	1	1	1	1	1	1	1	1	1	2	Measured when $A_{TT}(dB) = 20\log(V_O/V_i)$ $A_{TT(max)}$: IHF-A in
A_{TT-6}	Attenuation (−6dB)	1	2	1	1	1	1	1	1	1	1	1	2	
$A_{TT(max)}$	Maximum attenuation	1	2	1	3	1	1	1	1	1	3	1	2	
CB	Channel balance	1	2	1	1	1	1	1	1	1	1	1	2	$CB(dB) = A_{TTch1} - A_{TTch2}$
THD	Total harmonic	1	2	1	1	1	1	1	1	1	1	1	2	15kHz LPF in
R_i	Input resistance	1	2	1→2	1	1	1	1	1	1	1	1→2	2	$R_i(k\Omega) = 150/(V_{o1}/V_{o2-1})$ V_{o1} : S3 and S11→1 V_{o2} : S3 and S11→2
$N_{O(min)}$	Output noise voltage (min)	1	1	1	3	1	1	1	1	1	3	1	1	No signals, IHF-A
$N_{O(max)}$	Output noise voltage (max)	1	1	1	3	1	1	1	1	1	3	1	1	No signals, IHF-A
$V_{i(max)}$	Maximum input voltage	1	2	1	1	1	1	1	1	1	1	1	2	Input signal voltage at 1% output distortion
$V_{O(max)}$	Maximum output voltage	1	2	1	1	1	1	1	1	1	1	1	2	Output signal voltag at 1% output distortion
CT	Crosstalk	1	3 2	1	3 2	1	1	1	1	1	2 3	1	2 3	IHF-A in CT(dB) = 20log (V_O(Vrms) /2(Vrms))
I_{OH}	Output port high level current	1	1	1	1	2	2	2	2	1	1	1	1	Current is measured at pins⑨,⑩,⑪ and ⑫ when the status of output ports is "high impedance."
V_{OL}	Output port low level voltage	1	1	1	1	1	1	1	1	1	1	1	1	Current is measured at pins⑨,⑩,⑪ and ⑫ when output ports takes in current.
ICH	LOCK input current	1	1	1	1	1	1	1	1	1	1	1	1	Current is measured at pin⑧.
ICL		1	1	1	1	1	1	1	1	1	1	1	1	Current is measured at pin⑦.
IDH	DATA input current	1	1	1	1	1	1	1	1	1	1	1	1	
IDL		1	1	1	1	1	1	1	1	1	1	1	1	
VCH	CLOCK H level voltage	1	1	1	1	1	1	1	1	1	1	1	1	
VCL	CLOCK L level voltage	1	1	1	1	1	1	1	1	1	1	1	1	
VDH	DATA H level voltage	1	1	1	1	1	1	1	1	1	1	1	1	
VDL	DATA L level voltage	1	1	1	1	1	1	1	1	1	1	1	1	

Note 1. When two switching conditions are specified, the item should be measured under both conditions.

TEST CIRCUIT

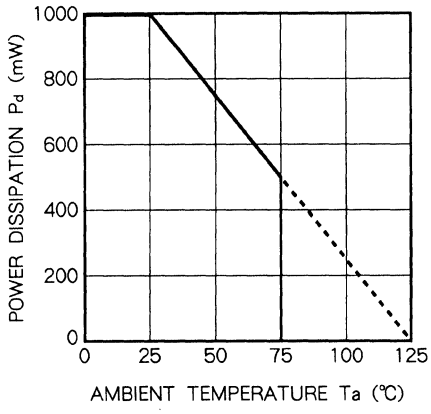


Units Resistance : Ω
Capacitance : F

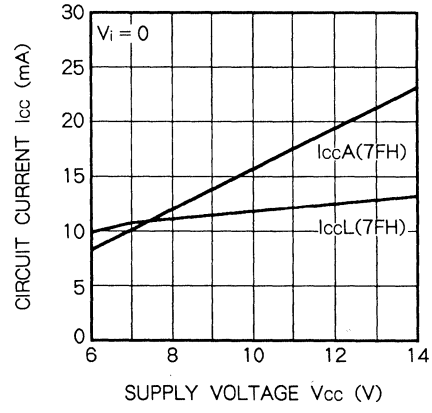
MITSUBISHI ELECTRIC

TYPICAL CHARACTERISTICS

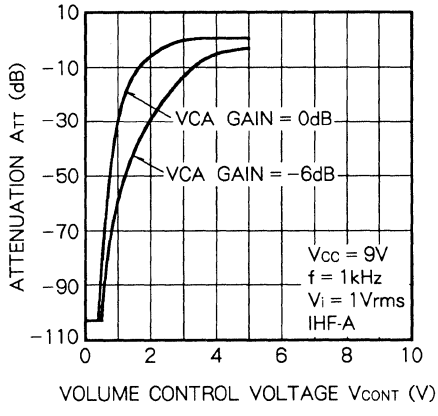
THERMAL DERATING



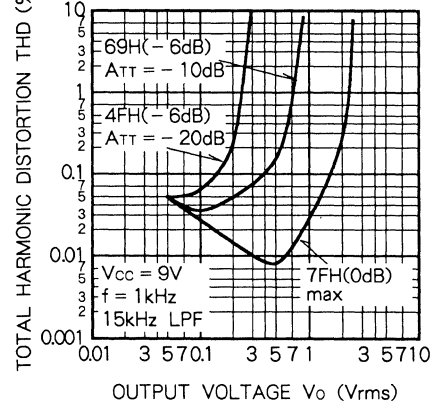
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



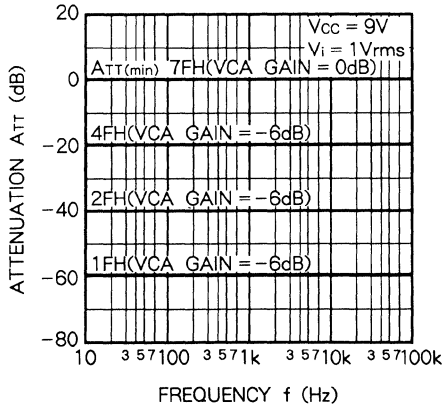
ATTENUATION VS. VOLUME CONTROL VOLTAGE



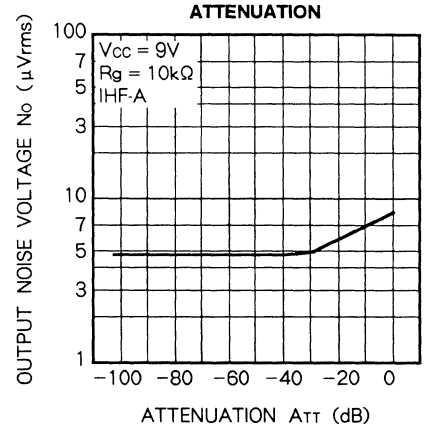
TOTAL HORMONIC DISTORTION VS. OUTPUT VOLTAGE



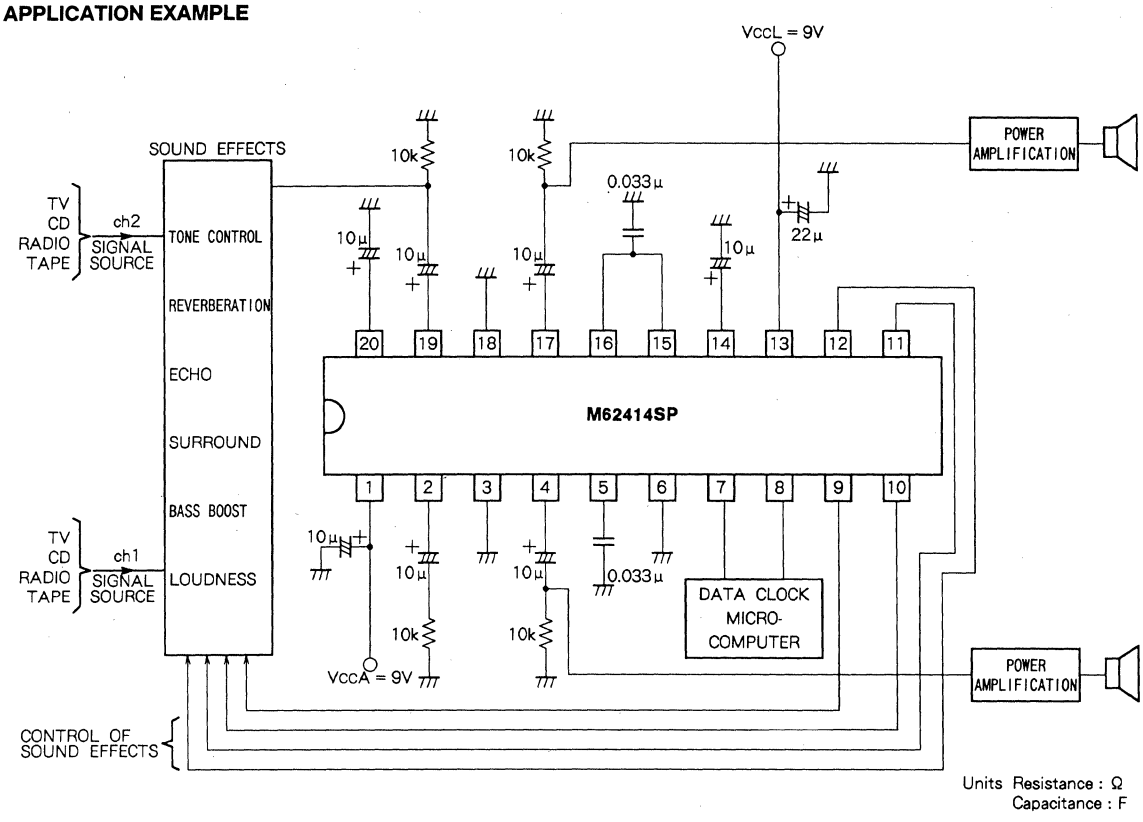
ATTENUATION VS. FREQUENCY



OUTPUT NOISE VOLTAGE VS. ATTENUATION



APPLICATION EXAMPLE



OPERATION DESCRIPTION

(1) Design circuit board to ensure sufficient radiation.

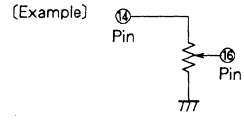
(2) This IC includes an analog section and digital section. Design circuit boards to prevent digital noise jumping and runaround crosstalk.

(3) Set all GND pins to GND potential. Take care that GND pins do not interfere with each other to prevent disconnection between analog section and digital section.

(4) Apply approximately equal voltage to pin① (VccA) pin and pin⑬ (VccL). (Pay attention to power supply rise and fall.)

(5) When supply voltage is low, internal reset circuit is on. Set operational functions after supply voltage reaches the recommended operational range.

(6) When external DC voltage is applied to VCA, set the input voltage to between approximately 0V~4V. It is recommended that pin⑭ voltage be used as the 4V referebce voltage.



M62415P,FP

2 CH 4 MODE PRESET EQUALIZER

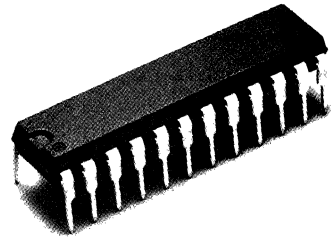
DESCRIPTION

The M62415 is preset equalizer IC's developed for stereo set, radio cassette, and audio equipments.

Output character of 4 modes, "Normal, Rock, Pops and Classic". The selection one can be choiced via 4 control terminals.

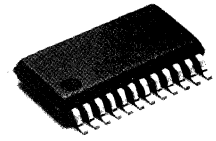
FEATURES

- Sound controller of preset typ for 3-element graphic equalizer.
- It can be controlled by 4-easy control switches.
- Equiped with output ports for drive in LED.
- These function housed in 24-pin dual inline package (300mil DIP)
- Low noise V_{NO} (flot) = 4.5μVrms (typ)
- Low distortion THD = 0.005% (typ)



Outline 24P4D (P)

2.54mm pitch 300mil DIP
(6.3mm×29.2mm×3.3mm)



Outline 24P2Q-A (FP)

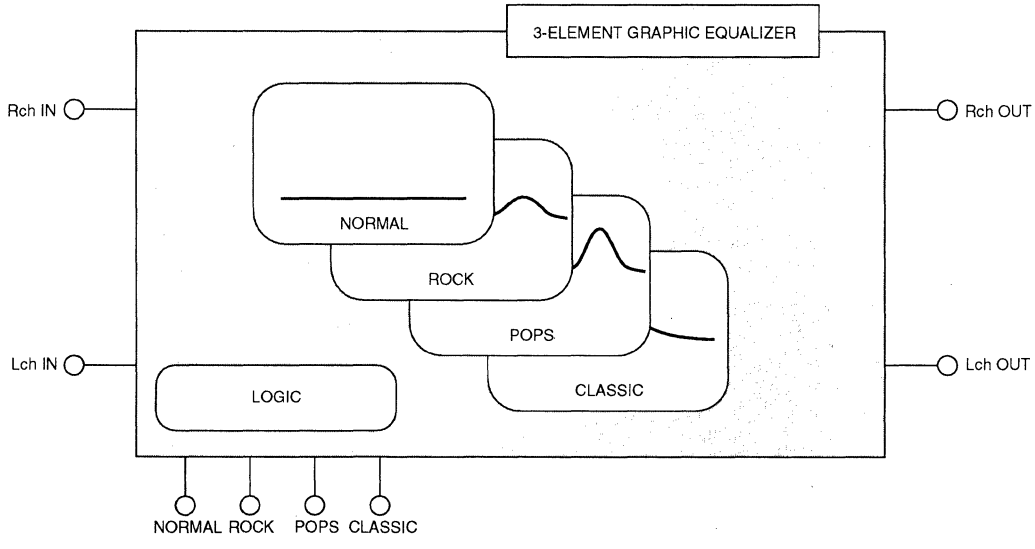
0.8mm pitch 300mil SSOP
(5.3mm×10.1mm×1.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 6.0 ~ 13.0 V
Rated supply voltage ..... V_{CC} = 9.0 V

SYSTEM CONFIGURATION

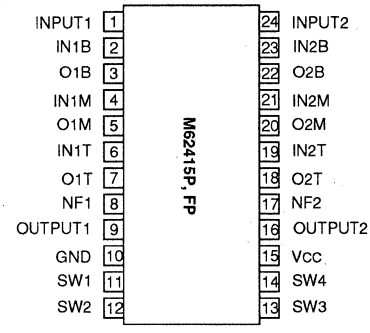
M62415P, FP



M62415P,FP

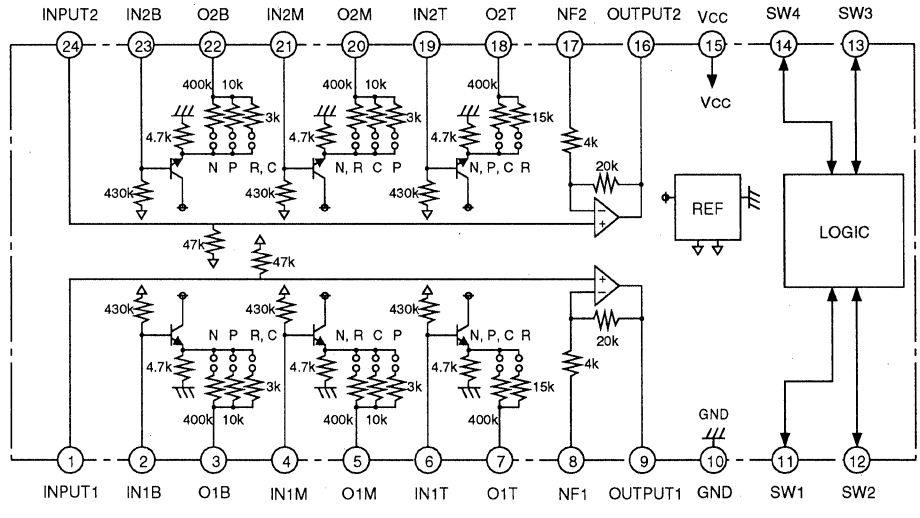
2 CH 4 MODE PRESET EQUALIZER

PIN CONFIGURATION



Outline 24P4D (P)
24P2Q-A (FP)

IC INTERNAL BLOCK DIAGRAM



N: NORMAL
R: ROCK
P: POPS
C: CLASSIC

Unit Resistance : Ω

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

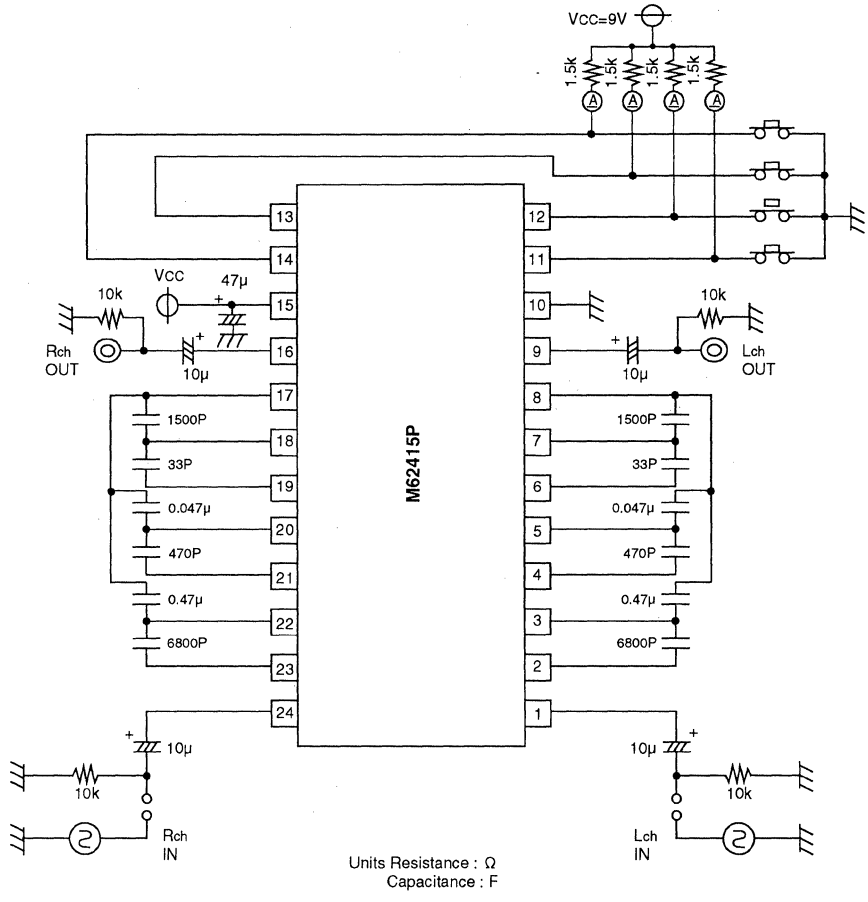
Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	14	V
K_θ	Thermal derating (Ta≧25℃)	11.5	mW/℃
P_d	Power dissipation	1150	mW
T_{opr}	Operage temperature range	−20～+75	°C
T_{stg}	Storage temperature	−40～+125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 9 V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter			Test conditions	Limits			Unit
					Min	Typ	Max	
I_{DD}	Circuit current			V_{CC} = 9V	14	23	32	mA
G(Normal)B	Pre set mode	Normal	BASS	f = 80Hz	−2	1	4	dB
G(Normal)M			MID	f = 1kz	−2	1	4	dB
G(Normal)T			TREBLE	f = 10kHz	−2	1	4	dB
G(ROCK)B		ROCK	BASS	f = 80Hz	8	11	14	dB
G(ROCK)M			MID	f = 1kz	−1	2	5	dB
G(ROCK)T			TREBLE	f = 10kHz	3	6	9	dB
G(POPS)B		POPS	BASS	f = 80Hz	3	6	9	dB
G(POPS)M			MID	f = 1kz	8	11	14	dB
G(POPS)T			TREBLE	f = 10kHz	0	3	6	dB
G(CLASSIC)B		CLASSIC	BASS	f = 80Hz	8	11	14	dB
G(CLASSIC)M			MID	f = 1kz	4	7	10	dB
G(CLASSIC)T			TREBLE	f = 10kHz	−1	2	5	dB
V_{OM}	Maximum output voltage			THD = 1%, f = 1kHz, Normal mode	2	2.5	−	V_{rms}
THD	Total harmonic distortion			f = 1kHz, V_O = 0.5V_{rms} Normal mode	−	0.005	0.05	%
V_{NO}	Output noise voltage			Rg = 10kΩ, BW : IHF-A Normal mode	−	4.5	10.0	μV_{rms}
CS_{ep}	Channel separation			f = 1kHz, Rg = 10kΩ, Normal mode BW : DIN AUDIO	−	−80	−65	dB
I_{LED}	Maximum LED drive current			Seted switchs, Rp = 1.5kΩ	4.5	5.6	−	mA

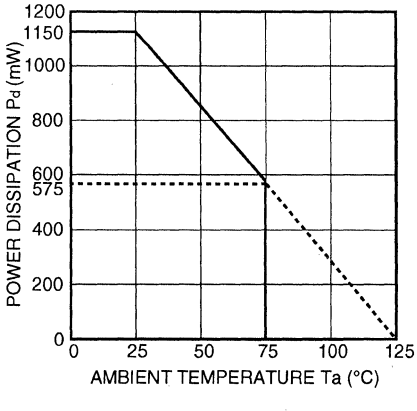
Note. These are forbid that switchs operate at the same time.

TEST CIRCUIT

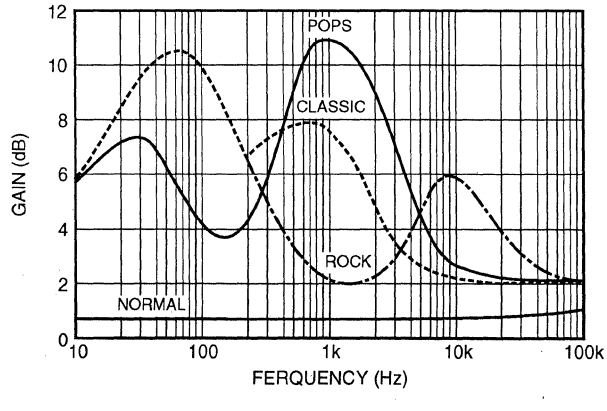


TYPICAL CHARACTERISTICS

THERMAL DERATING

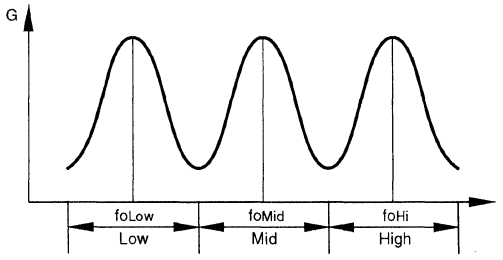


FREQUENCY CHARACTERISTICS



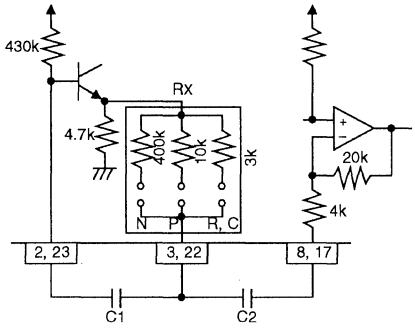
APPLICATION NOTE

Frequency characteristics



N: NORMAL
R: ROCK
C: CLASSIC
P: POPS

(1) Low band

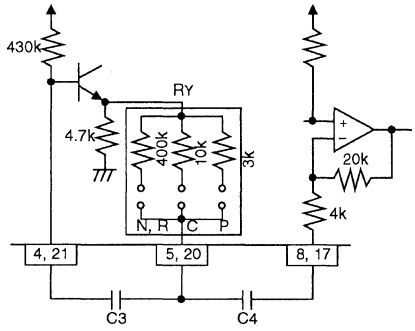


$$f_{oLow} \simeq \frac{1}{2\pi\sqrt{C1 \cdot C2 \cdot Rx \cdot 430k}} \text{ [Hz]}$$

$$Q_{Low} \simeq \sqrt{\frac{C1 \cdot Rx \cdot 430k}{C2\,(Rx + 4k)^2}}$$

$$G_{Rock} \simeq 20\log\frac{20k + 4k + Rx}{4k + Rx} \text{ [dB]}$$

(2) Mid band

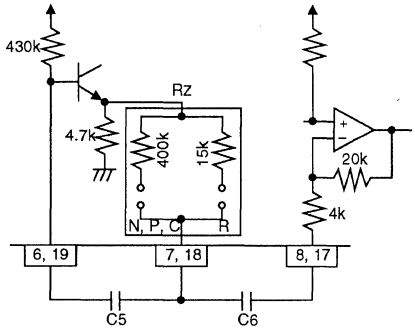


$$f_{oMid} \simeq \frac{1}{2\pi\sqrt{C3 \cdot C4 \cdot RY \cdot 430k}} \text{ [Hz]}$$

$$Q_{Mid} \simeq \sqrt{\frac{C3 \cdot Rx \cdot 430k}{C4\,(RY + 4k)^2}}$$

$$G_{Mid} \simeq 20\log\frac{20k + 4k + RY}{4k + RY} \text{ [dB]}$$

(3) Hi band

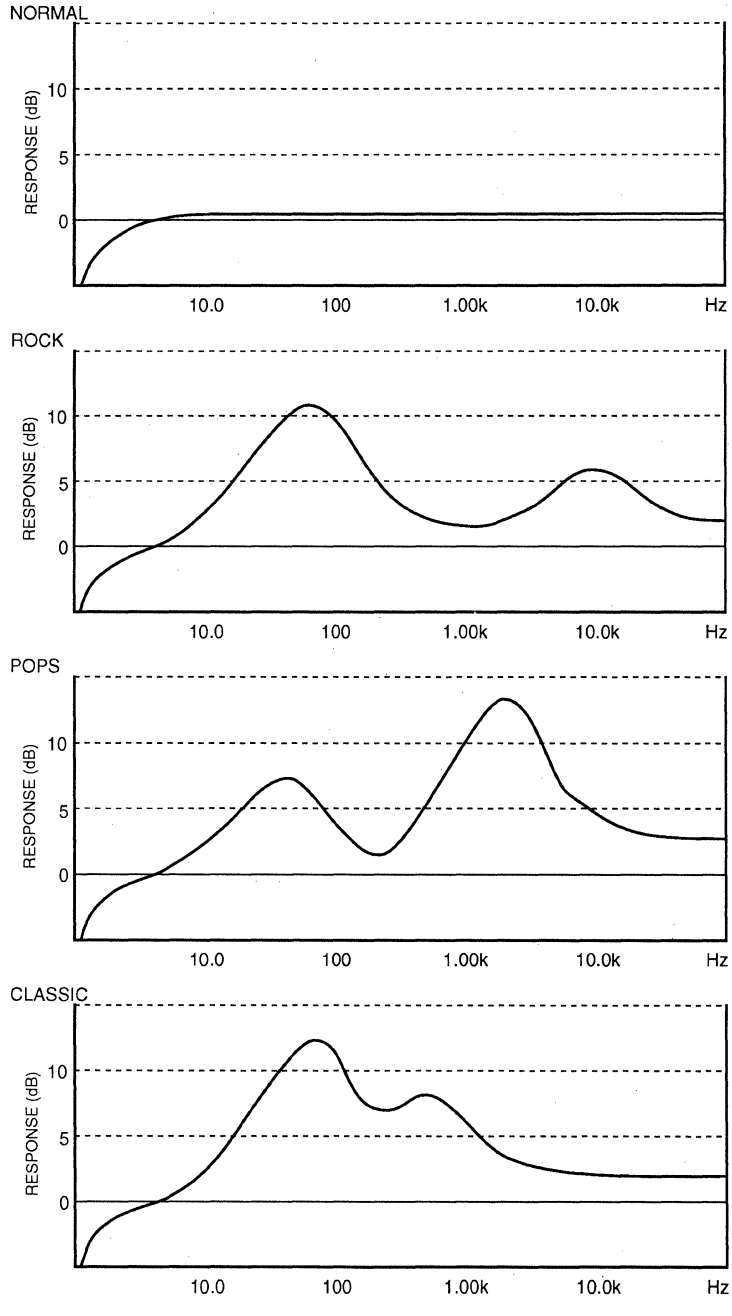


$$f_{oHi} \simeq \frac{1}{2\pi\sqrt{C5 \cdot C6 \cdot Rz \cdot 430k}} \text{ [Hz]}$$

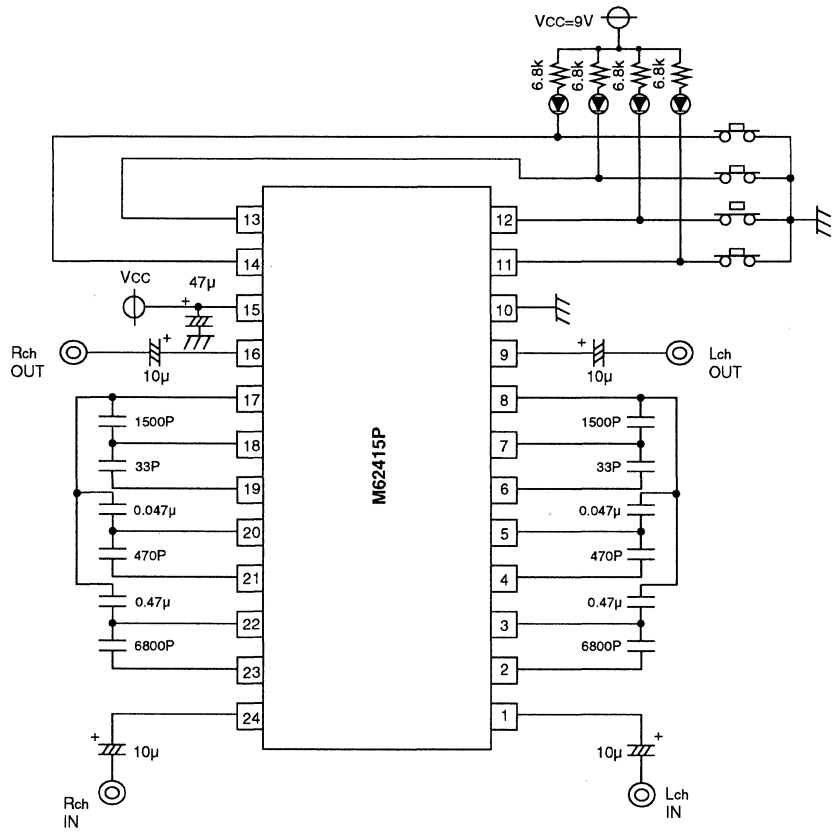
$$Q_{Hi} \simeq \sqrt{\frac{C5 \cdot Rz \cdot 430k}{C6\,(Rz + 4k)^2}}$$

$$G_{Hi} \simeq 20\log\frac{20k + 4k + Rz}{4k + Rz} \text{ [dB]}$$

SOUND CONTROL SPECK



APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

M62416FP

3-ELEMENT GRAPHIC EQUALIZER WITH MICROCOMPUTER INTERFACE

DESCRIPTION

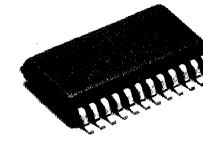
The M62416FP is a tone controller IC.

The IC has a resonance circuitry and is, with 8-bit serial data sent from a microcomputer, capable of performing 2 channel, 3 band tone control.

It is best suited to preset tone control applications.

FEATURES

- Housed in 24-pin shrink package (SSOP)
- Built-in microcomputer interface circuit controlled by 8-bit serial data
- Built-in 2 channel, 3 band tone control.
- Low noise: V_{NO} = 10 μV_{rms} (typ.) <IHF-A>
- Low distortion factor: THD = 0.03% (typ.)



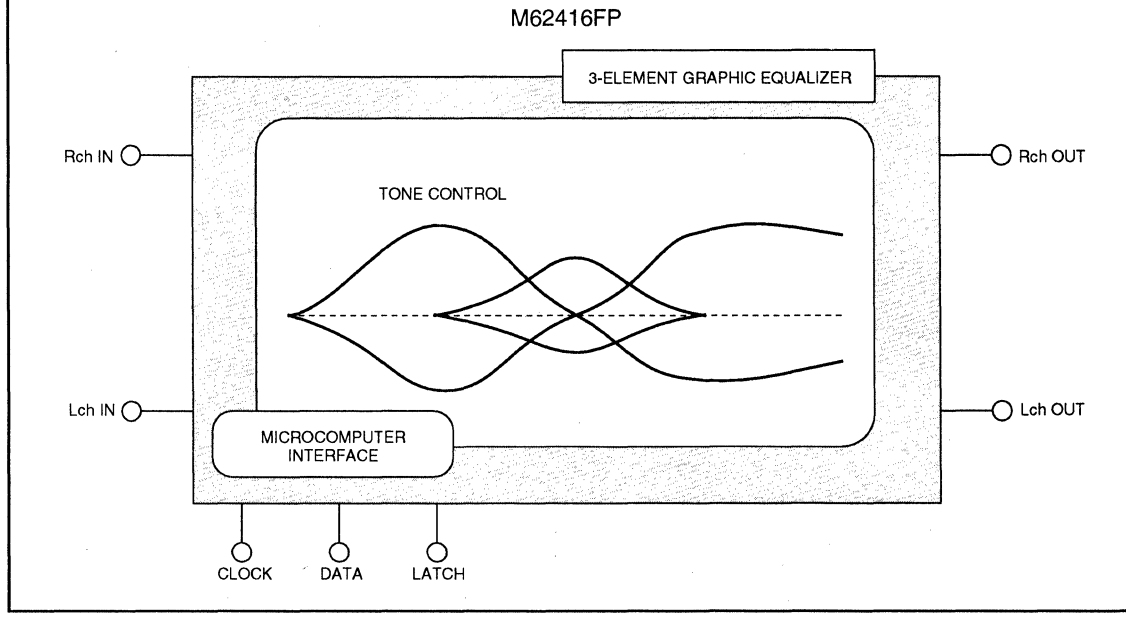
Outline 24P2Q-A

0.8mm pitch 300mil SSOP
(5.3mm×10.1mm×1.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... Vcc = 6.0 ~ 12.0 V
Rated supply voltage ..... Vcc = 7 V

SYSTEM CONFIGURATION

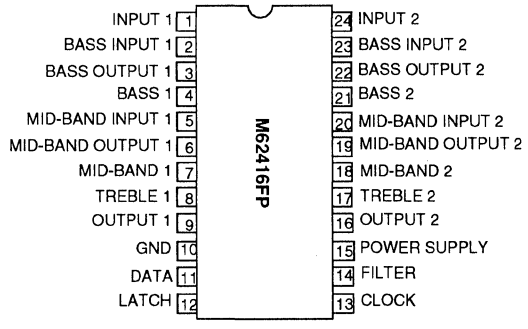


MITSUBISHI ELECTRIC

M62416FP

3-ELEMENT GRAPHIC EQUALIZER WITH MICROCOMPUTER INTERFACE

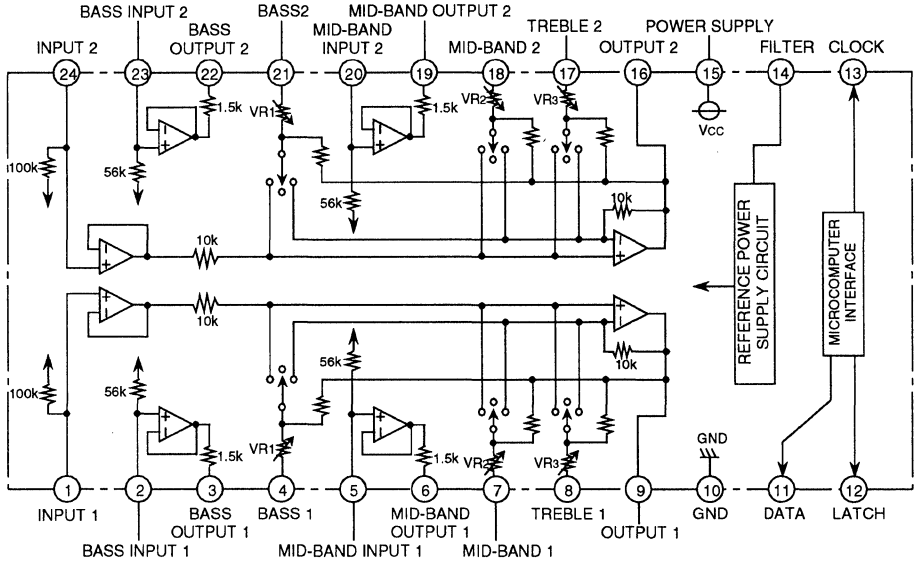
PIN CONFIGURATION



Outline 24P2Q-A

NC : NO CONNECTION

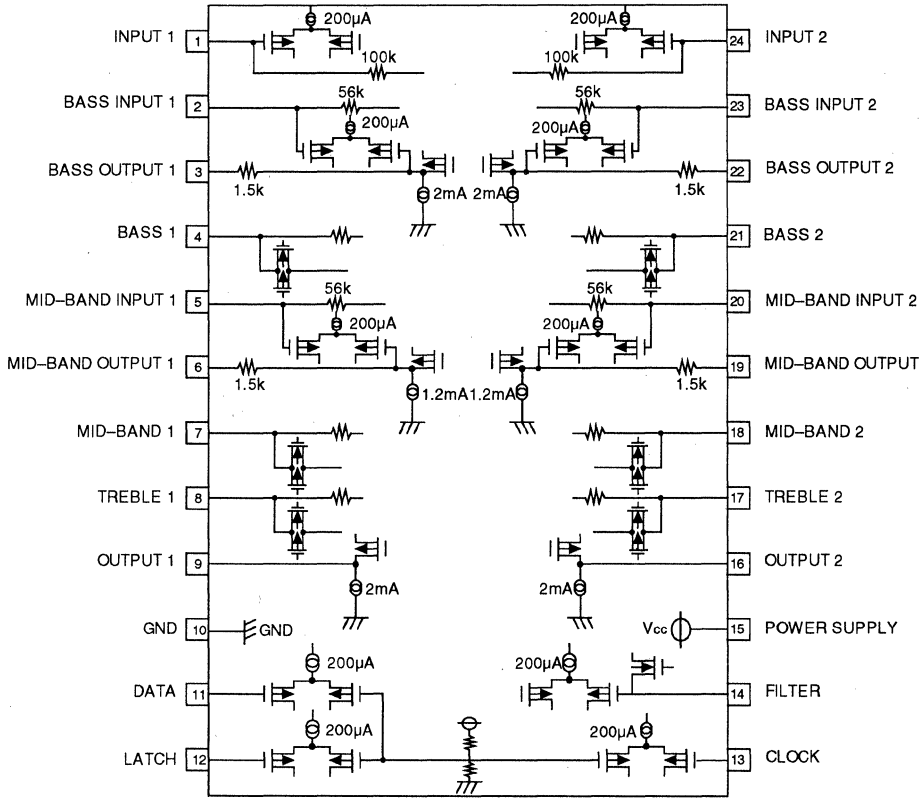
IC INTERNAL BLOCK DIAGRAM



VR1: ±3dB; 22.7k, ±6dB; 8.5k, +9dB; 4k
VR2: ±3dB; 22.7k, ±6dB; 8.5k
VR3: ±3dB; 24.2k, ±6dB; 10k, +9dB; 5.5k

Units Resistance : Ω
Capacitance : F

INPUT/OUTPUT FORM (Design values are indicated in figure.)



Units Resistance : Ω
Capacitance: F

PIN DESCRIPTION

Pin No.	Name	Function
① (㉔)	Input 1 (2)	Ch 1 (2) signal input
② (㉓)	Bass input 1 (2)	Bass resonance amp input
③ (㉒)	Bass output 1 (2)	Bass resonance amp output
④ (㉑)	Bass 1 (2)	Bass gain selection
⑤ (⑳)	Mid-band input 1 (2)	Mid-band resonance amp input
⑥ (⑲)	Mid-band output 1 (2)	Mid-band resonance amp output
⑦ (⑱)	Mid-band 1 (2)	Mid-band gain selection
⑧ (⑰)	Treble 1 (2)	Treble gain selection
⑨ (⑯)	Output 1 (2)	Ch 1 (2) signal output
⑩	GND	Ground
⑪	Data	Input of control data sent from μ-COM to IC Receives data in sync with clock
⑫	Latch	Data latch of serial data sent from μ-COM to IC Operates at falling edges.
⑬	Clock	Clock used to transmit serial data from μ-COM to IC Operates at rising edges.
⑭	Filter	Removal of ripples in power source
⑮	Power Supply	Applies 6 ~ 12 V (rating: 7 V)

ABSOLUTE MAXIMUM RATINGS

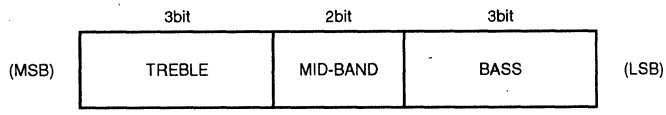
Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	14	V
P_d	Power dissipation	540	mW
k_θ	Thermal derating (Ta≧25℃)	5.4	mW/℃
T_{opr}	Operating temperature range	−20~75	°C
T_{stg}	Storage temperature	−55~125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25℃, Vcc = 7 V, f = 1 kHz, and flat, unless otherwise noted)

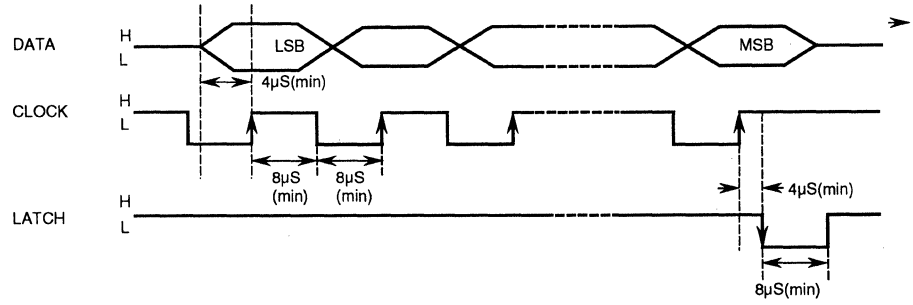
Symbol	Parameter			Test conditions	Limits			Unit
					Min	Typ	Max	
I_{CC}	Circuit current			Quiescent	13	23	33	mA
GV(flat)	Voltage gain				–	0	–	dB
G(Bass)B	Tone	Bass	Boost (max.)		–	9	–	dB
G(Bass)C			Cut (max.)		–	−6	–	dB
G(MID)B		Mid-band	Boost (max.)		–	6	–	dB
G(MID)C			Cut (max.)		–	−3	–	dB
G(Tre)B		Treble	Boost (max.)		–	9	–	dB
G(Tre)C			Cut (max.)		–	−6	–	dB
Gstep		Control step			–	3	–	dB
V_{OM}	Maximum output voltage			THD = 1%	1.5	2.0	–	V_{rms}
THD	Total harmonic distortion			V_O = 0.5V_{rms}	–	0.03	0.3	%
V_{NO}	Output noise voltage			Rg = 10kΩ, filter: IHF-A	–	10	23	μV_{rms}
CS_{ep}	Channel separation			Filter: IHF-A	–	−90	−70	dB

DIGITAL CONTROL SPECIFICATIONS

Data format



Timing diagram (recommended conditions)



Note: 1. CLOCK operates at rising edges of pulse.
2. LATCH operates at falling edges of pulse.
3. Recommended input level
"H" level : more than 4V
"L" level : less than 1V

DATA SETTING TABLE

Treble

	Data			Gain
	D5	D6	D7	
Boost	H	H	H	9dB
	H	H	L	6dB
	H	L	H	3dB
Flat	L	L	L	0dB
Cut	L	L	H	−3dB
	L	H	L	−6dB

Mid-band

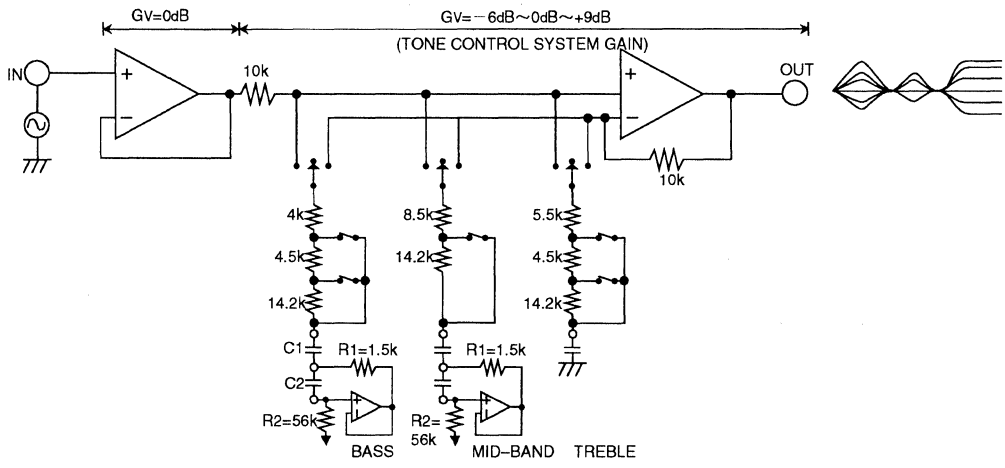
	Data		Gain
	D3	D4	
Boost	H	H	6dB
	H	L	3dB
Flat	L	L	0dB
Cut	L	H	−3dB

Bass

	Data			Gain
	D0	D1	D2	
Boost	H	H	H	9dB
	H	H	L	6dB
	H	L	H	3dB
Flat	L	L	L	0dB
Cut	L	L	H	−3dB
	L	H	L	−6dB

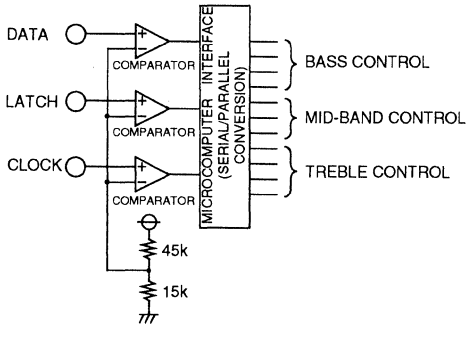
FUNCTION DESCRIPTION

(1) Tone block: Processes main analog signals.



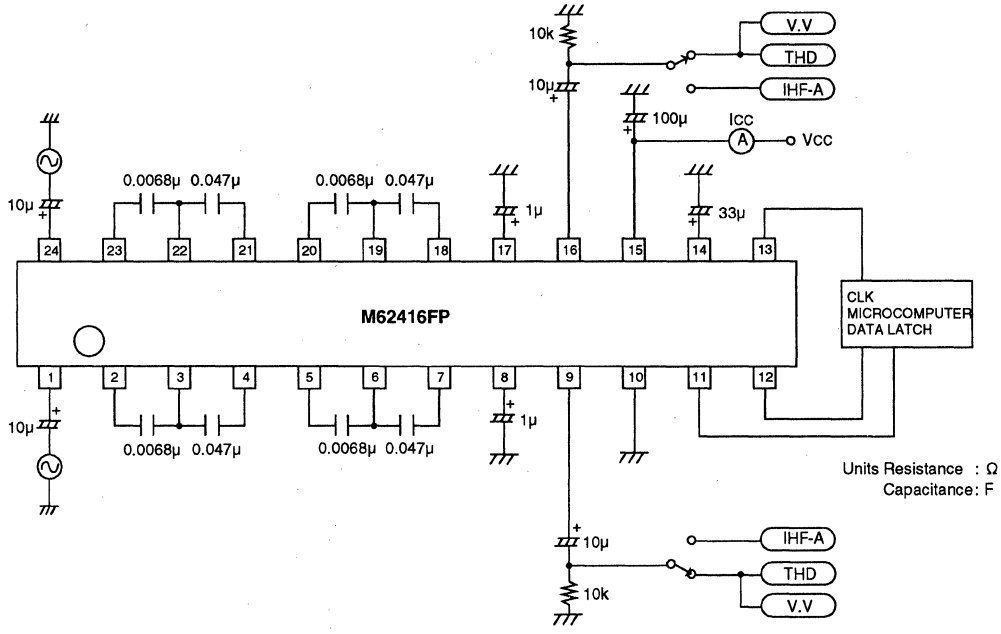
1) Input signals are separated into bass, mid, and treble bands. Resonance circuits (band-pass filters) separate signals into bass and mid bands, while treble is separated by a CR filter. These separated signals are boosted or cut by making selection from internal gain setting resistors.
2) Tone control step.
   Bass : −6dB ~ 0dB ~ 9dB 3dB/step
   Mid-band: −3dB ~ 0dB ~ 6dB 3dB/step
   Treble: −6dB ~ 0dB ~ 9dB 3dB/step
3) Gain control in each band is performed by means of serial data sent from a microcomputer.

(2) Control block: Processes data transmitted from a microcomputer to control the gain in each band.

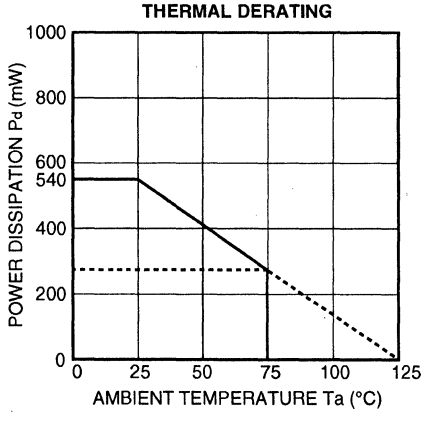


1) Send initialization data at power up, because the internal logic is unstable at power up.
2) 8-bit serial data is used for control by microcomputer. For data settings, see Digital Control Specifications on page 6.

TEST CIRCUIT

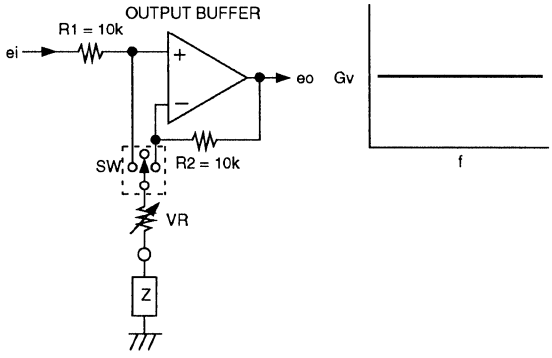


TYPICAL CHARACTERISTICS



(1) Flat boost cut

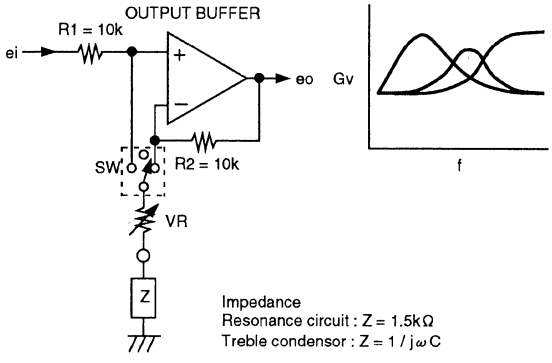
(a) Flat



SW is center position, the frequency characteristics will be level regardless of the resonance circuit.

●Z is an impedance in the resonance circuit.

(b) Boost



When the SW is in boost position, the resonance circuit is connected to the NF loop of the output buffer amplifier.
The gain Av is

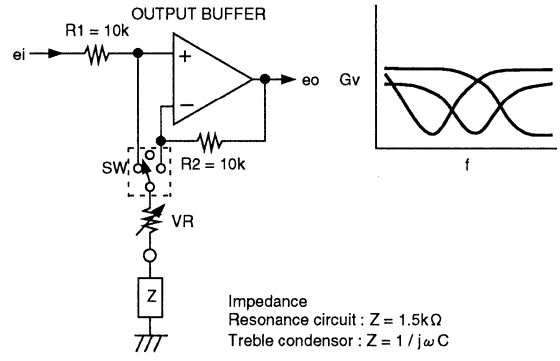
$$Av = \frac{R2 + Z + VR}{Z + VR}$$

The output voltage eo is

$$eo = Av \cdot ei = \frac{R2 + Z + VR}{Z + VR}\ ei$$

When Z is smallest, the gain in resonance is the greatest, and the optional frequency is then boosted.

(c) Cut



When the SW is in cut position, the resonance circuit is connected to the input side of the output buffer amplifier.
The gain Av is

$$ei' = \frac{VR + Z}{R1 + VR + z}\ ei \quad AV = 1 \text{ and}$$

The output voltage eo is

$$eo = Av \cdot ei' = \frac{VR + Z}{R1 + VR + z}\ ei$$

When Z is smallest, the gain in resonance is the greatest, and the optional frequency is then cut.

(2) Resonance circuit

The simulated inductor circuit converts L in the R, L, C serial resonance circuit into a CR pin by the buffer functions of active pins such as resisters. Operational amplifiers, works in a almost the same way as the R, L, C serial resonance circuit.

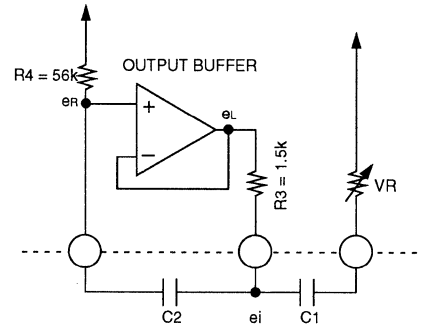


Fig.1 Tone control circuit

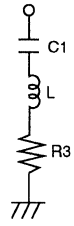


Fig.2 Equivalant circuit

(a) Frequency fo

The L, R, C resonance frequency fo is

$$fo = \frac{1}{2\pi\sqrt{LC}} \quad \text{.....Equation No.1}$$

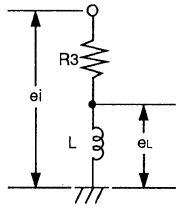


Fig.3

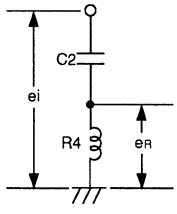


Fig.4

When the voltage ei is supplied to resonance circuit as shown in Fig.3

$$eL = \frac{j\omega L}{R3 + j\omega L} ei$$

if ei is then supplied to the pins C1, R4 as shown in Fig.4

$$eR = \frac{j\omega C2 \cdot R4}{1 + j\omega C2 \cdot R4} ei = \frac{j\omega C2 \cdot R3 \cdot R4}{R3 + j\omega C2 \cdot R3 \cdot R4}$$

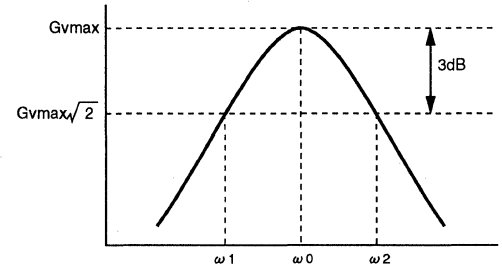
$L = C2 \cdot R3 \cdot R4$ When $eL = eR$ .....Equation No.2

If eR is replaced by eL and L serial circuit, R3 and C1 are automatically connected in order to keep the value of eR stable, a buffer amplifier should be used. The buffer amplifier is equivalent to an impedance. By equations No.1 and No.2, the resonance frequency, fo is

$$fo = \frac{1}{2\pi\sqrt{C1 \cdot C2 \cdot R3 \cdot R4}}$$

(b) Shape of resonance

About Shape of resonance, Q is defined by the ratio of ωo ($\omega o = 2\pi fo$) and the frequency band width $\omega 2 - \omega 1$, ($Gmax/\sqrt{2}$)

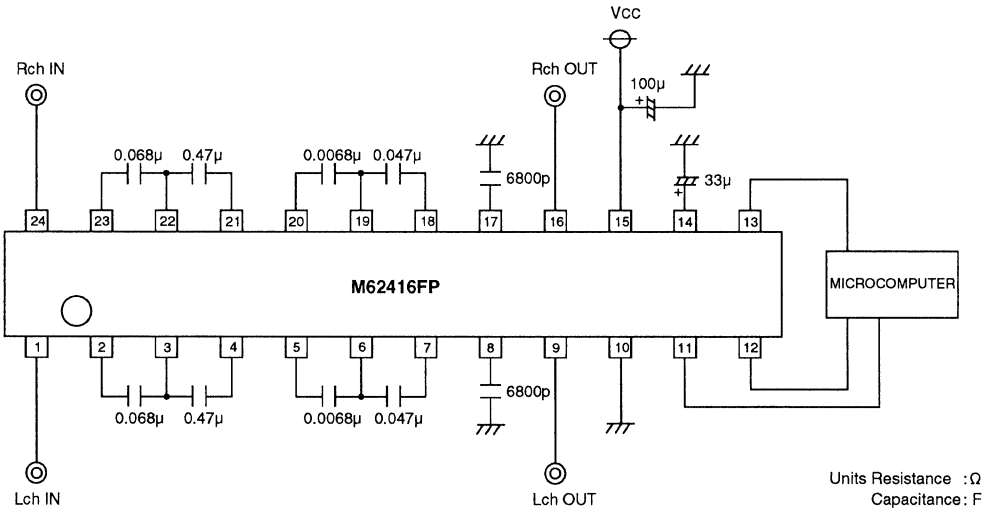


The value of Q is found by the following equation ;

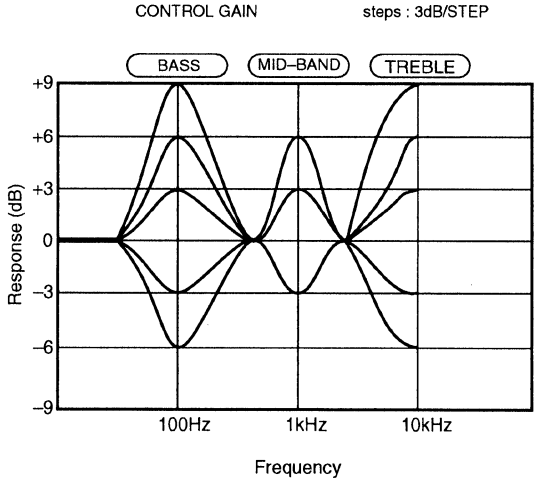
$$Q = \sqrt{\frac{C2 \cdot R4}{C1 \cdot R3}}$$

The greater the value of Q the narrower the frequency band width, and vice versa. The M62416FP is composed of R3, R4, so Q is defined by selecting the external condensor.

APPLICATION EXAMPLE



Frequency response



M62417SP

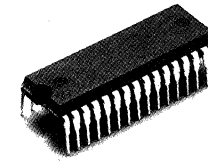
DIGITAL SOUND CONTROLLER FOR MINIATURE UNIT AUDIO SYSTEMS, TV TONE QUALITY/SOUND FIELD CONTROL

DESCRIPTION

The M62417SP is a digital sound controller IC for miniature unit audio systems.
The IC, with serial data sent from a microcomputer, makes it easy to realize karaoke functions (voice canceling) and tone quality/sound field control such as surround and 2-band tone control.

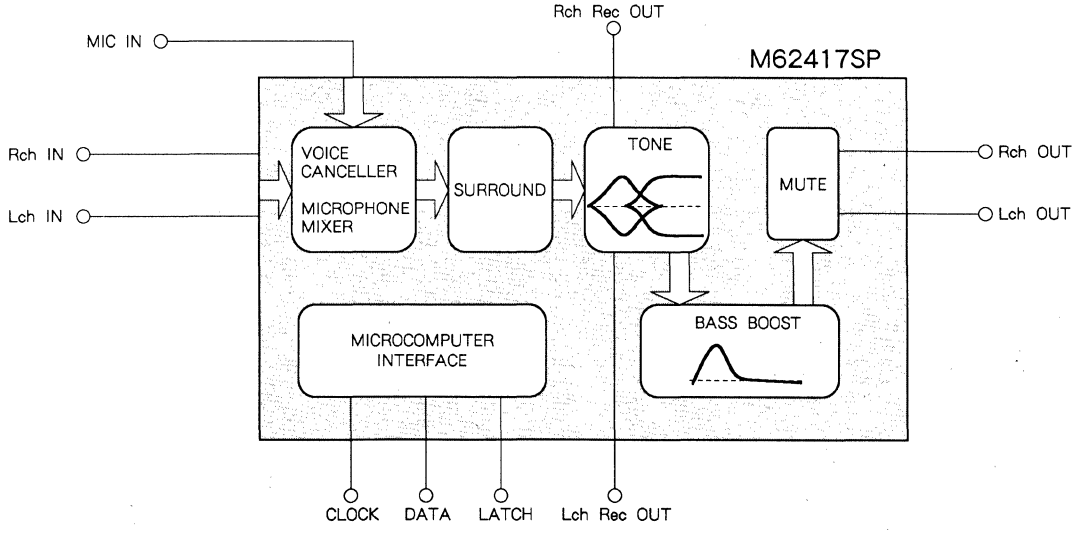
FEATURES

- 32-pin shrink DIP
- Capable of controlling each function by serial data
  - Bass/treble ..... 0, ± 3, ± 6, ± 10dB
  - Surround ..... [ON/OFF]
  - Bass boost ..... [ON/OFF]
  - Voice canceling ..... [ON/OFF]
  - Mute ..... [ON/OFF]



Outline 32P4B
1.778mm pitch 400mil SDIP
(8.9mm × 28.0mm × 3.8mm)

SYSTEM CONFIGURATION

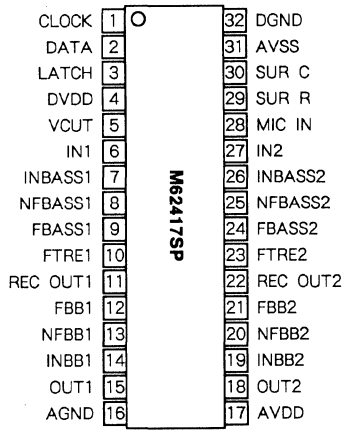


MITSUBISHI ELECTRIC

M62417SP

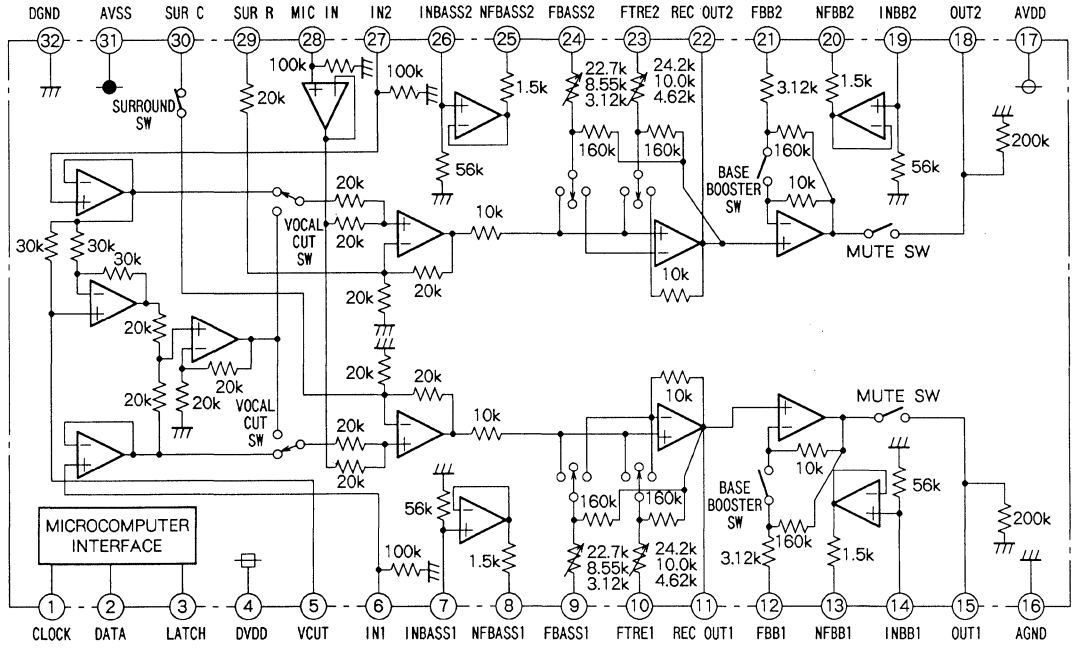
DIGITAL SOUND CONTROLLER FOR MINIATURE UNIT AUDIO SYSTEMS, TV TONE QUALITY/SOUND FIELD CONTROL

PIN CONFIGURATION



Outline 32P4B

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

PIN DESCRIPTION

Pin No.	Symbol	Function
①	CLOCK	Clock input for serial data transmission
②	DATA	Control data input. Receives data in sync with CLOCK
③	LATCH	Trigger input for data writing. Data is written at positive-going edges
④	DVDD	Power supply to internal logic circuits
⑤	VCUT	Capacitive impedance (band-pass filter) connection pin for vocal cut
⑥	IN1	Channel 1 input
⑦	INBASS1	Input of resonant buffer amp in base section
⑧	NFBASS1	Output of resonant buffer amp in base section
⑨	FBASS1	Resonant impedance (band-pass filter) connection pin for base section
⑩	FTRE1	Resonant impedance (band-pass filter) connection pin for treble section
⑪	REC OUT1	REC output of channel 1
⑫	FBB1	Input of bass boosting resonant buffer amp
⑬	NFBB1	Output of bass boosting resonant buffer amp
⑭	INBB1	Resonant impedance (band-pass filter) connection pin for bass boosting
⑮	OUT1	Channel 1 output
⑯	AGND	Ground of internal analog circuit
⑰	AVDD	Positive power supply to internal analog circuit
⑱	OUT2	Channel 2 output
⑲	INBB2	Input of bass boosting resonant buffer amp
⑳	NFBB2	Output of bass boosting resonant buffer amp
㉑	FBB2	Resonant impedance (band-pass filter) connection pin for bass boosting
㉒	REC OUT2	REC output of channel 2
㉓	FTRE2	Resonant impedance (band-pass filter) connection pin for treble section
㉔	FBASS2	Resonant impedance (band-pass filter) connection pin for base section
㉕	NFBASS2	Output of resonant buffer amp in base section
㉖	INBASS2	Input of resonant buffer amp in base section
㉗	IN2	Channel 2 input
㉘	MIC IN	Microphone input
㉙	SUR R	External C connection pin for setting time constant for surround
㉚	SUR C	External C connection pin for setting time constant for surround
㉛	AVSS	Negative power supply to internal analog circuits
㉜	DGND	Ground of internal logic circuits

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
AV_{DD}, AV_{SS}	Analog supply voltage	± 8.5	V
DV_{DD}	Digital supply voltage	7.0	V
P_d	Power dissipation (Ta ≦ 25℃)	1250	mW
K_θ	Thermal derating (Ta > 25℃)	9.5	mW/℃
T_{opr}	Operating temperature	−20～+75	℃
T_{stg}	Storage temperature	−55～+125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, AV_{DD} = 7V, AV_{SS} = − 7V, DV_{DD} = 5V, unless otherwise noted.

Tone control and bass boost are set to 0dB.)

(1) Power supply characteristics

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
AI_{DD}	Circuit current of analog positive power supply	Current at pin ㉜ with AV_{DD} = 7V, AV_{SS} = − 7V No signal	−	22	−	mA
AI_{SS}	Circuit current of analog negative power supply	Circuit current at pin ⑰ with AV_{DD} = 7V, AV_{SS} = − 7V No signal	−	− 22	−	mA
DI_{DD}	Circuit current of digital power supply	Current at pin ④ with DV_{DD} = 5V No signal	−	1	−	μA

(2) Characteristics of the digital block

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IL}	Input voltage ("L" level)	CLOCK, DATA, LATCH pins		0	−	0.3·DV_{DD}	V
V_{IH}	Input voltage ("H" level)			0.7·DV_{DD}	−	DV_{DD}	V
I_{IL}	Output voltage ("L" level)	V_{IN} = 0	CLOCK, DATA, LATCH pins	−10	−	10	μA
I_{IH}	Input current ("H" level)	V_{IN} = DV_{DD}		−	−	10	μA
F_{CIK}	CLOCK frequency			−	−	250	kHz
t_{WHC}	CLOCK pulse width			4.0	−	−	μS
t_{SD}	DATA setup time			1.0	−	−	μS
t_{HD}	DATA hold time			1.0	−	−	μS
t_{WHI}	LATCH pulse width			2.0	−	−	μS
t_{SI}	LATCH setup time			1.0	−	−	μS

(3) Input/Output characteristics

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
R_{IN}	Input resistance	Pin ⑥, ㉗, Ta = 25℃		50	100	200	kΩ
V_{IM}	Max. input voltage	Input to pin ⑥, ㉗, ㉘, output from pin ⑮, ⑱		3.0	4.0	–	Vrms
V_{ODC}	Output pin voltage	Pin ⑮, ⑱, no signal		−0.15	0	0.15	V
V_{RECDC}		Pin ⑪, ㉒, no signal		−0.1	0	0.1	V
G_V	Pass gain	V_{IN} = 1Vrms, flat. pin ⑥, ㉗ − ⑮, ⑱ gains		−1	0	1	dB
V_{ONO}	Output noise voltage	JIS-A filter, no signal, R_g = 10k Ω	pin ⑮, ⑱	–	7.0	20	μVrms
V_{RECNO}			pin ⑪, ㉒	–	5.5	15	μVrms
THD	Distortion factor	pin ⑮, ⑱. V_O = 0.5Vrms, R_L = 30k Ω		–	0.02	0.8	%
THD_{REC}		pin ⑪, ㉒. V_O = 0.5Vrms, R_L = 10k Ω		–	0.01	0.4	%
CT	Crosstalk between channels	Between pin ⑥, ㉗ − ⑱, ⑮ lines, V_O = 1Vrms, R_L = 30k Ω		−60	−70	–	dB
CT_{REC}		Between pin ⑥, ㉗ − ㉒, ⑪ lines, V_O = 1Vrms, R_L = 10k Ω		−60	−70	–	dB

(4) Tone control characteristics

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
G_{BOOST1}	Tone control voltage gain	3dB	f = 1KHz, V_O = 1Vrms, Input pin ⑥, ㉗ − output pin ⑮, ⑱ gain	2	3	4	dB
G_{BOOST2}		6dB		5	6	7	dB
G_{BOOST3}		10dB		8.5	10	11.5	dB
G_{CUT1}		−3dB		−4	−3	−2	dB
G_{CUT2}		−6dB		−7	−6	−5	dB
G_{CUT3}		−10dB		−11.5	−10	−8.5	dB
B_{ALTON}	Balance between channels	f = 1kHz, V_O = 1Vrms, Each of boost and cut conditions		−1	0	+1	dB

(5) Bass boost characteristics

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
G_{DD}	Bass boost voltage gain	f = 1kHz, V_O = 1Vrms Pin ⑮, ⑱	8.5	10	11.5	dB
B_{ALDD}	Graphic equalizer balance between channels	f = 1kHz, V_O = 1Vrms, Defference in pin ⑮ − ⑱ gain	−1	0	+1	dB

(6) Microphone amplifier input/output characteristics

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
R_{micin}	Input resistance	Pin ㉘	50	100	200	kΩ
V_{IMmic}	Max. input voltage	FLAT, R_L = 30kΩ, THD = 1 %, Measure input at pin ㉘, outputs at pin ⑮, ⑱	3.0	4.0	–	Vrms
G_{Vmic}	Pass gain	pin ⑮, ⑱ − ㉘ voltage gains, V_O = 0.5Vrms, R_L = 30KΩ	−1	0	2	dB
THD_{mic}	Distortion factor	pin ⑮, ⑱ V_O = 0.5Vrms, R_L = 30KΩ	–	0.02	0.8	%
B_{ALmic}	Balance between channels	Difference in voltage gain between pin ⑮, ⑱	−1	0	1	dB

DIGITAL CONTROL SPECIFICATIONS

Digital format

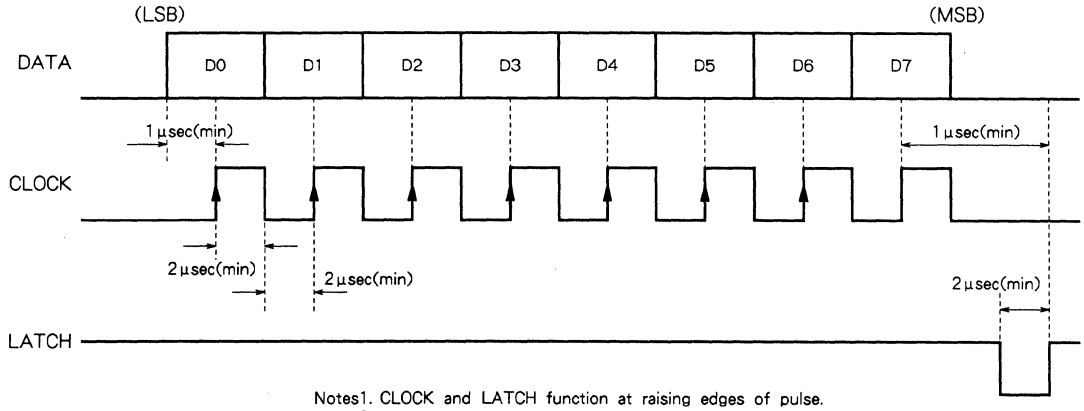
	D7	D6	D5	D4	D3	D2	D1	D0	
DATA 0 (MSB)	MODE SELECT 0	BASS BOOST OFF/ON	SURROUND OFF/ON	OUTPUT MUTE OFF/ON	VOCAL CUT OFF/ON	——	——	——	(LSB)
DATA 1 (MSB)	MODE SELECT 1	TONE CONTROL MODE 01 : BASS 10 : TREBLE		——	——	BOOST/CUT VOLUME			(LSB)

	Signal name	Function		Signal name	Function
D0	–	Fixed to "0"	D0	Tone boosting/ cutting volume	See table below
D1	–	Fixed to "0"	D1		
D2	–	Fixed to "0"	D2		
D3	Vocal cut	Vocal cut disabled by "0" Vocal cut enabled by "1"	D3	–	Fixed to "0"
D4	Output mute	Output mute disabled by "0" Output mute enabled by "1"	D4	–	Fixed to "0"
D5	Sorround	Sorround disabled by "0" Sorround enabled by "1"	D5	Tone control mode	See table below
D6	Bass boost	Bass boost disabled by "0" Bass boost enabled by "1"	D6		
D7	Mode select	Data 0 is selected by "0"	D7	Mode select	Data 1 is selected by "1"

D2	D1	D0	Boosting / cutting volume	D2	D1	D0	Boosting / cutting volume
0	0	0	+0dB	1	0	0	−0dB
0	0	1	+3dB	1	0	1	−3dB
0	1	0	+6dB	1	1	0	−6dB
0	1	1	+10dB	1	1	1	−10dB

D5	D6	Mode
0	1	Bass
1	0	Treble

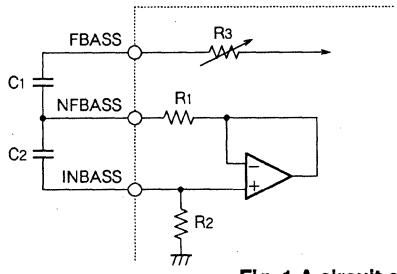
DATA TIMING (Recommended conditions)



Notes1. CLOCK and LATCH function at raising edges of pulse.
2. High level : 3.5V min. ; Low level : 1.5V max.

FUNCTION DESCRIPTION

(1) Tone controller equivalent circuit



CENTER FREQUENCY

$10 = 1/2\pi\sqrt{C1 \cdot C2 \cdot R1 \cdot R2}$ [Hz]

$Q = \sqrt{(C2 \cdot R2) / (C1 \cdot R1)}$

EXAMPLE : BASS BAND (f = 150Hz)
R1 = 1.5k Ω, R2 = 56k Ω
C1 = 0.82 μ, C2 = 0.015 μ

Fig. 1 A circuit equivalent to the inside of the tone controller

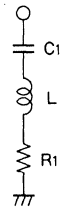
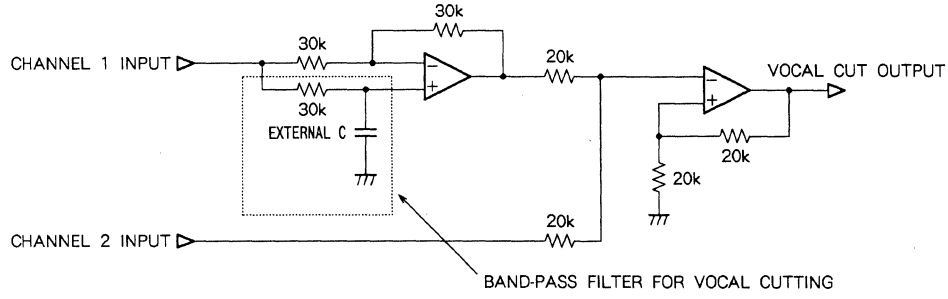


Fig. 2 is equivalent to Fig.1. To convert compoment constants, the equation below is used.

$L = C2 \cdot R1 \cdot R2$

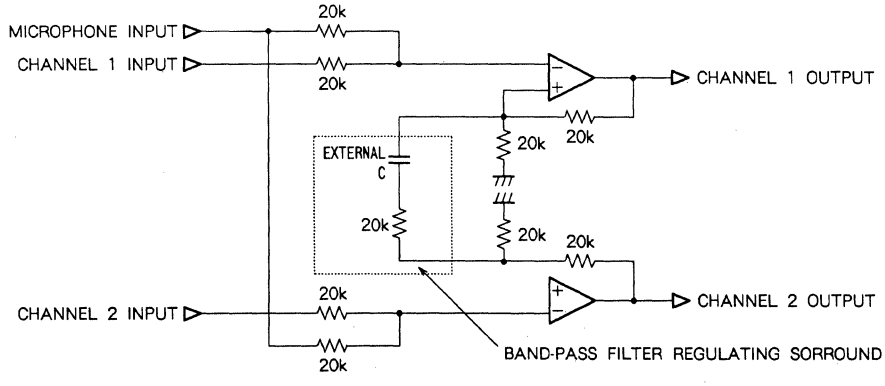
Fig. 2 An equivalent circuit using L

(2) Vocal cut block equivalent circuit

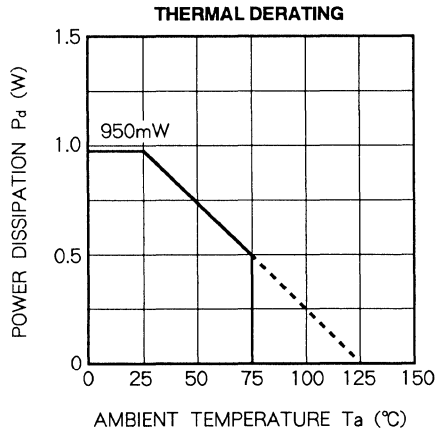


Note. The vocal cut output is monaural.

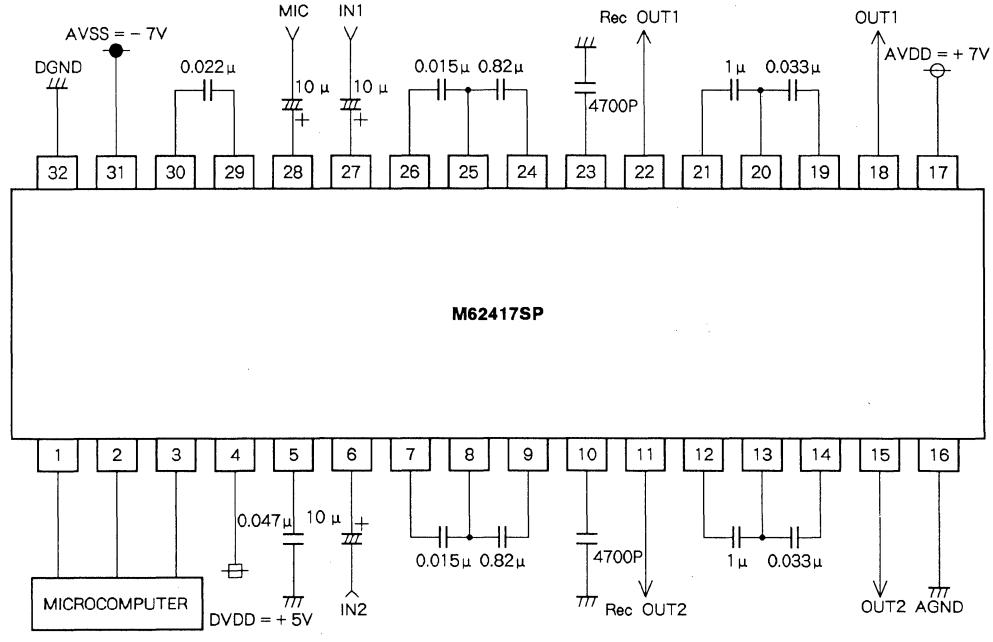
(3) Surround block equivalent circuit



TYPICAL CHARACTERISTICS



APPLICATION EXAMPLE



Unit Capacitance : F

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

M62419FP

ELECTRONIC VOLUME IC WITH 4 SPEAKER TONE CONTROLLER

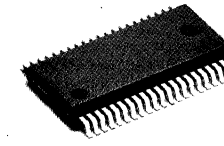
DESCRIPTION

The M62419FP is an IC developed for car audio, it has a built-in 4ch input selector, master volume, loudness, tone control and fader volume blocks. All of these blocks are controlled via serial data.

This IC is also applicable to other appliances such as home audio and TV.

FEATURES

- Designed to adjust the gain of each source at the input selection switch section
- Sound volume (master & fader) and quality (bass & treble, loudness) are controlled at the front row of power
- Geared to analog sound signal processing
- Sound volume and quality are adjusted via serial data
- Analog/digital-mixed IC realized by FULL-CMOS
- Maximum input voltage ..... 2.8Vrms (V_{CC} = 8V)



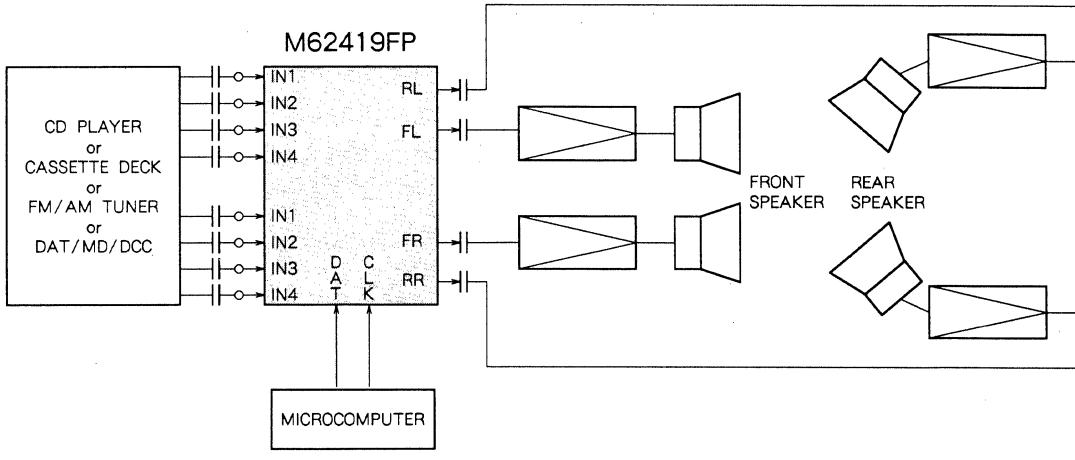
Outline 42P2R-A

0.8mm pitch 450mil SSOP
(8.4mm × 17.5mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 6~9V, V_{DD} = 4~6V
Rated supply voltage ..... V_{CC} = 8V, V_{DD} = 5V
Rated power dissipation 280mW

SYSTEM CONFIGURATION



MITSUBISHI ELECTRIC

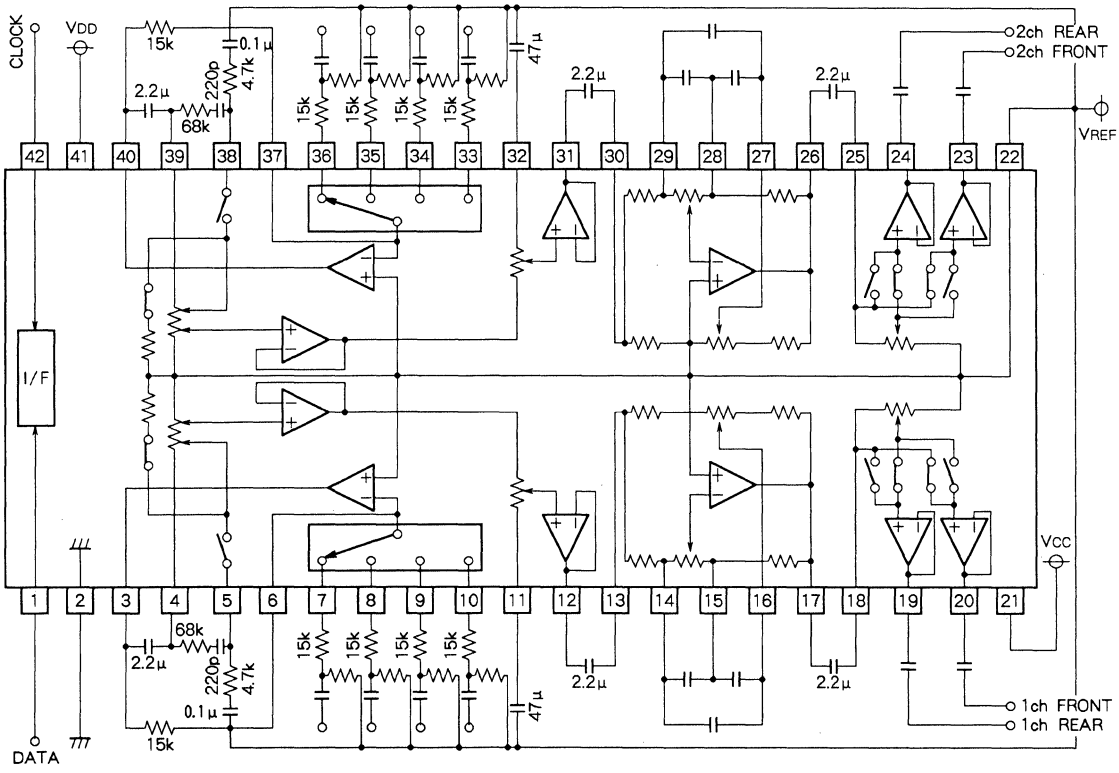
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}, V_{DD}	Supply voltage	10, 7	V
P_d	Power dissipation	990	mW
T_{opr}	Operating temperature	−30 ~ +85	℃
T_{stg}	Storage temperature	−55 ~ +125	℃

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current		−	35	−	mA
A_{TT}(VOL)	Maximum attenuation	A_{TT}(VOL) = −∞	−	−90	−80	dB
ΔATT(VOL)	Attenuation error	A_{TT}(VOL) = 0	−2.0	0	2.0	dB
V_{IM}	Maximum input voltage	THD = 1%	2.0	2.8	−	μVrms
G(Bass)B	Bass boost	f = 100Hz	9	12	15	dB
G(Bass)C	Bass cut	f = 100Hz	−15	−12	−9	dB
G(Tre)B	Treble boost	f = 10kHz	9	12	15	dB
G(Tre)C	Treble cut	f = 10kHz	−15	−12	−9	dB
A_{TT}(FED)	Maximum attenuation	A_{TT}(FED) = −∞	−	−80	−74	dB
V_{OM}	Maximum output voltage	THD = 1%	1.8	2.2	−	Vrms
$V_{NO}1$	Output noise voltage	A_{TT}(VOL)=0, A_{TT}(FED)=0, Rg=0, DIN-AUDIO	−	9	18	μVrms
$V_{NO}2$		A_{TT}(VOL)=−∞, A_{TT}(FED)=−∞, Rg=0, DIN-AUDIO	−	5.5	11	μVrms
THD	Total harmonic distortion	f = 1kHz, Vo = 0.5Vrms, Loudness = OFF, A_{TT}(VOL) = 0, A_{TT}(FED) = 0	−	0.003	0.05	%
CS	Channel separation	f = 1kHz	−	−90	−80	dB

APPLICATION EXAMPLE



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M62420SP

I²C BUS TV ELECTRONIC VOLUME IC WITH TONE CONTROLLER

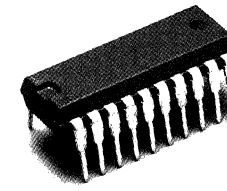
DESCRIPTION

The M62420SP is a dual channel sound volume/quality controller, is controlled via I²C bus. The volume section is designed to control the 2 channels either simultaneously or respectively in steps of 1dB. It incorporates the ladder resistance mechanism to reduce noise and distortion.

The tone control section is capable of controlling the tone within ±12dB in steps of 2dB. The Q value is adjustable by changing the exterior C value.

FEATURES

- Serial data control
  - Volume 0~−80dB(1dB/step), −∞
    (Independent control of respective channels)
  - Tone control(Treble/Bass) ±12dB(2dB/step)
- Low noise and low distortion
- Built-in reference voltage circuit

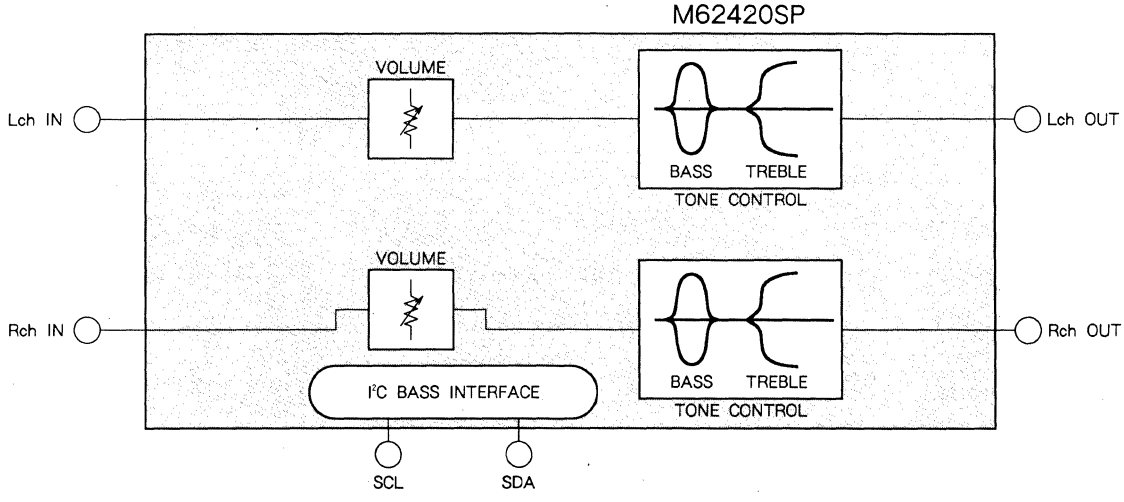


Outline 20P4B
1.778mm pitch 300mil SDIP
(6.3mm × 19.0mm × 3.3mm)

RECOMMENDED OPERATING CONDITIONS

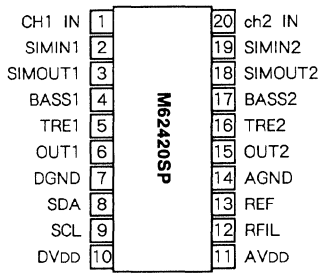
Supply voltage range ..... V_{CC} = 8~10V
V_{DD} = 4.5~5.5V
Rated supply voltage ..... V_{CC} = 9V
V_{DD} = 5V

SYSTEM CONFIGURATION



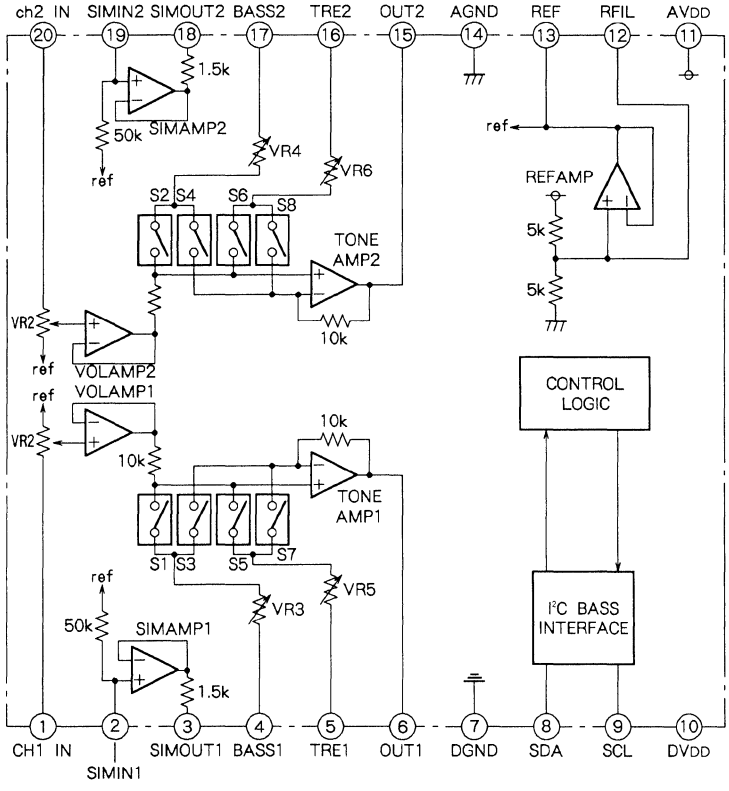
MITSUBISHI ELECTRIC

PIN CONFIGURATION



Outline 20P4B

IC INTERNAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{DD}	Supply voltage	10	V
P_d	Power dissipation (Ta ≦ 25℃)	750	mW
T_{opr}	Operating temperature	− 20 ~ + 75	℃
T_{stg}	Storage temperature	− 40 ~ + 125	℃

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{DD}	Circuit current		−	35	−	mA
V_{IM}	Maximum input voltage		−	2	−	Vrms
ATTmin	Minimum attenuation		−	0	−	dB
ATTmax	Maximum attenuation		−	90	−	dB
G_{BBm}	Maximum bass boost		−	+ 12	−	dB
G_{BCm}	Maximum bass cut		−	− 12	−	dB
G_{TBm}	Maximum treble boost		−	+ 12	−	dB
G_{TCm}	Maximum treble cut		−	− 12	−	dB
Vom	Maximum output voltage		−	2	−	Vrms
THD	Total harmonic distortion		−	0.05	0.1	%
No	Noise		−	8.5	30	μVrms
CS	Channel separation		−	80	−	dB

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M62422FP

3-ELEMENT GRAPHIC EQUALIZER WITH BUILT-IN SURROUND FOR KARAOKE FUNCTIONS

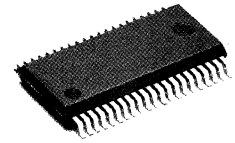
DESCRIPTION

The M62422FP is an IC of 2 power supply system and for tone control applications.

The IC, in addition to the 3-element graphic equalizer, has a vocal canceller, microphone mixer, and analog surround circuitry built in. It can be used in surround systems and vocal and microphone mixing blocks in karaoke equipment, as well as in tone control blocks in a variety of audio equipment. Furthermore, the key control signal input/output pins of the IC facilitate signal connections with the key control block.

FEATURES

- 42-pin shrink SOP package
- Low distortion factor. THD = 0.01% (Vi = 0.5 Vrms)
- Capable of controlling each function by serial data.
  - Bass/mid-band/treble
  - Bass boost ..... 0, ±3, ±6, ±10 dB
  - Surround ..... ON/OFF
  - Vocal cut ..... ON/OFF
  - Selection in sound multiplex mode ..... L only/R only
  - Key control signal output for karaoke applications
- Through output of signals in non-effect mode
- Signal output for digital surround
- Microphone-mixing input circuit



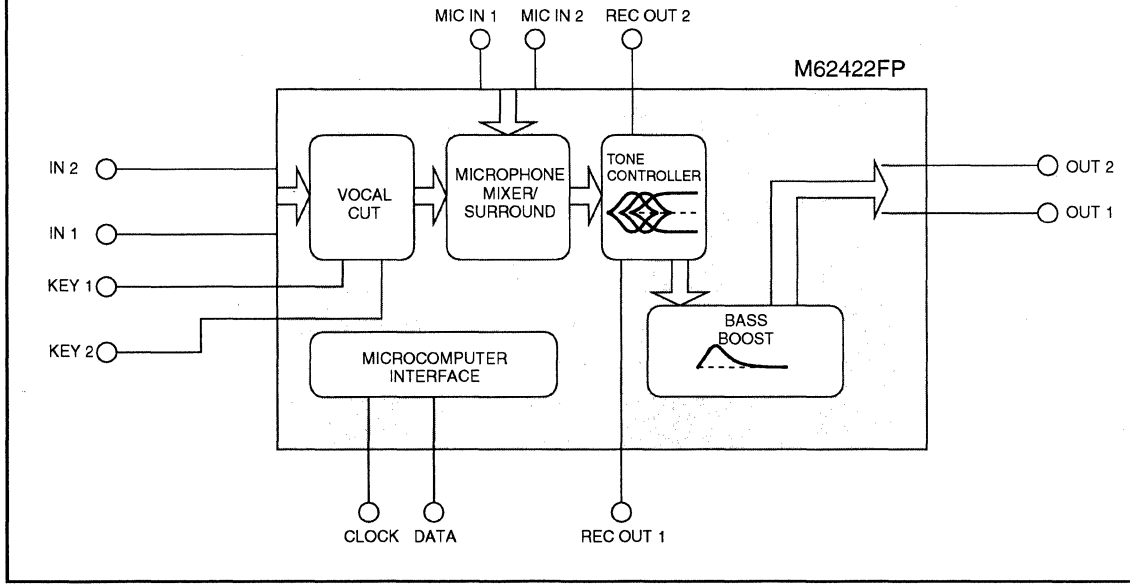
Outline 42P2R-A

0.8mm pitch 450mil SSOP
(8.4mm×17.5mm×2.0mm)

RECOMMENDED OPERATING CONDITIONS

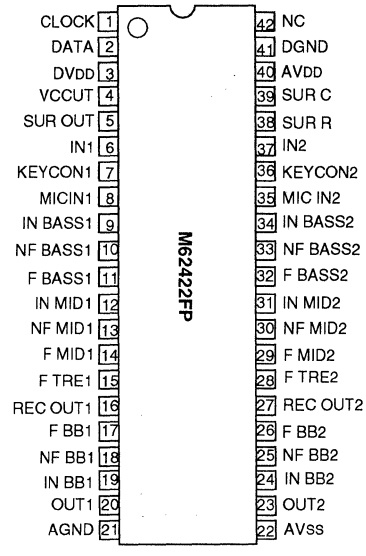
Supply voltage range ..... V_{CC} 5.0 ~ 7.0 V
V_{SS} −7.0 ~ −5.0 V
V_{DD} 4.5 ~ 5.5 V
Rated supply voltage ..... V_{CC} 6.5 V
V_{SS} −6.5 V
V_{DD} 5.0 V

SYSTEM CONFIGURATION



3-ELEMENT GRAPHIC EQUALIZER WITH BUILT-IN SURROUND FOR KARAOKE FUNCTIONS

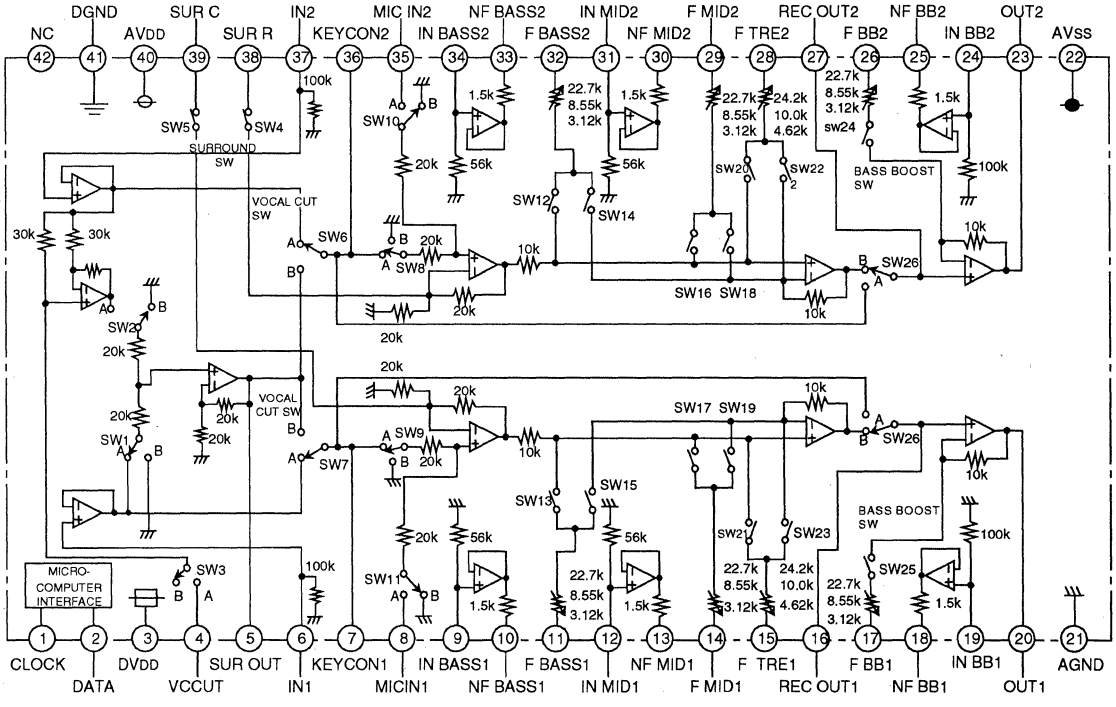
PIN CONFIGURATION



Outline 42P2R-A

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin No.	Symbol	Function
①	CLOCK	Clock input for serial data transmission
②	DATA	Control data input. Receives data in sync with CLOCK.
③	DV_{DD}	Power supply to internal logic circuit
④	VCUT	Capacitive impedance (band-pass filter) connection pin for vocal cut
⑤	SUROUT	Outputs L – R or L + R surround signals. Signals from which vocal part is cut are also output at this pin.
⑥	IN1	Channel 1 input
⑦	KEYCON1	Output to key controller
⑧	MICIN1	Microphone input for karaoke function
⑨	INBASS1	Input of resonant buffer amp in base section
⑩	NFBASS1	Output of resonant buffer amp in base section
⑪	FBASS1	Resonant impedance (band-pass filter) connection pin for base section
⑫	INMID1	Input of resonant buffer amp in mid-band section
⑬	NFMID1	Output of resonant buffer amp in mid-band section
⑭	FMID1	Resonant impedance (band-pass filter) connection pin for mid-band section
⑮	FTRE1	Resonant Impedance (band-pass filter) connection pin for treble section
⑯	REC OUT1	REC output of channel 1
⑰	FBB1	Input of bass boosting resonant buffer amp
⑱	NFBB1	Output of bass boosting resonant buffer amp
⑲	INBB1	Resonant impedance (band-pass filter) connection pin for bass boost section
⑳	OUT1	Channel 1 output
㉑	AGND	Ground of internal analog circuit
㉒	AV_{SS}	Negative power supply to internal analog circuit
㉓	OUT2	Channel 2 output
㉔	INBB2	Input of bass boosting resonant buffer amp
㉕	NFBB2	Output of bass boosting resonant buffer amp
㉖	FBB2	Resonant impedance (band-pass filter) connection pin for bass boost section
㉗	REC OUT2	REC output of channel 2
㉘	FTRE2	Resonant Impedance (band-pass filter) connection pin for treble section
㉙	FMID2	Resonant impedance (band-pass filter) connection pin for mid-band section
㉚	NFMID2	Output of resonant buffer amp in mid-band section
㉛	INMID2	Input of resonant buffer amp in mid-band section
㉜	FBASS2	Resonant impedance (band-pass filter) connection pin for base section
㉝	NFBASS2	Output of resonant buffer amp in base section
㉞	INBASS2	Input of resonant buffer amp in base section
㉟	MIC IN2	Microphone input
㊱	KEYCON2	Output to key controller
㊲	IN2	Channel 2 input
㊴	SUR R	External C connection pin for setting time constant for suround effects
㊳	SUR C	External C connection pin for setting time constant for suround effects
㊵	AV_{DD}	Positive power supply to internal analog circuits
㊶	DGND	Ground of internal logic circuits
㊷	non-connect	No connection

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
AV_{DD},AV_{SS}	Analog supply voltage	±7.5	V
DV_{DD}	Digital supply voltage	7.0	V
P_d	Power dissipation (Ta≦25℃)	950	mW
K_θ	Thermal derating (Ta>25℃)	9.5	mW/℃
T_{opr}	Operating temperature	–20~75	°C
T_{stg}	Storage temperature	–55~125	°C

ELECTRICAL CHARACTERISTICS (T_a = 25℃, AV_{DD} = 7 V, AV_{SS} = –7 V, DV_{DD} = 5 V, unless otherwise noted. Tone control and bass boost are set to 0 dB.)

(1) Power supply characteristics

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
AI_{DD}	Circuit current of analog positive power supply	Current at pin ㊵ with AV_{DD} = –6.5 V, AV_{SS} = –6.5 V No signal	–	25	–	mA
AI_{SS}	Circuit current of analog negative power supply	Current at pin ㉒ with AV_{DD} = –6.5 V, AV_{SS} = –6.5 V No signal	–	–25	–	mA
DI_{DD}	Circuit current of digital power supply	Current at pin ③ with DV_{DD} = 5 V No signal	–	20	–	μA

(2) Input/Output characteristics

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
R_{in}	Input resistance	Pin ⑥, ㊲, Ta = 25℃		35	50	65	kΩ
VIM	Max. input volatge	Input to pin ⑥, ㊲, output from pin ⑳, ㉓ Input to pin ⑧, ㉟, output from pin ⑳, ㉓ RL = 10kΩ, THD = 1%		2.5	3.5	–	V_{rms}
V_{odc}	Output pin voltage	Pin ⑳, ㉓, no signal		–0.15	0	0.15	V
V_{recdc}		Pin ⑯, ㉗, no signal		–0.1	0	0.1	V
Gv	Pass gain	V_{in} = 1 V_{rms}, flat, pin ⑥, ㊲ - ⑳, ㉓ gains		–2	0	2	dB
V_{ono}	Output noise voltage	JIS-A filter No signal Rg = 10kΩ	Pin ⑳, ㉓	–	7.0	20	μV_{rms}
V_{recno}			Pin ⑯, ㉗	–	5.5	15	μV_{rms}
THD	Distortion factor	Pin ⑳, ㉓ V_O = 0.5 V_{rms}, R_L = 10kΩ		–	0.01	0.05	%
THD_{rec}		Pin ⑯, ㉗ V_O = 0.5 V_{rms}, R_L = 10kΩ		–	0.01	0.05	%
CT	Crosstalk between channels	V_O = 1 V_{rms}, R_L = 10kΩ Between pin ⑥, ㊲ - ㉓, ⑳ lines		–80	–90	–	dB
CT_{rec}		V_O = 1 V_{rms}, R_L = 10kΩ Between pin ⑥, ㊲ - ㉗, ⑯ lines		–80	–90	–	dB

(3) Tone control characteristics

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
Gboost1	Tone control voltage gain	3dB	f = 1 kHz, V_O = 1 V_{rms} Input pin ⑥, ㊲ - output pin ⑳, ㉓ gains	2	3	4	dB
Gboost2		6dB		5	6	7	dB
Gboost3		10dB		8.5	10	11.5	dB
Gcut1		–3dB		–4	–3	–2	dB
Gcut2		–6dB		–7	–6	–5	dB
Gcut3		–10dB		–11.5	–10	–8.5	dB
BAL_{ton}	Balance between channels	f = 1 kHz, V_O = 1 V_{rms} Each of boost and cut conditions		–1	0	1	dB

(4) Bass boost characteristics

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
Gboost1	Bass boost voltage gain	3dB	f = 1 kHz, V_O = 1 V_{rms} Input pin ⑥, ㊲ - output pin ⑳, ㉓ gains	2	3	4	dB
Gboost2		6dB		5	6	7	dB
Gboost3		10dB		8.5	10	11.5	dB
BAL_{ton}	Balance between channels	f = 1 kHz, V_O = 1 V_{rms} Under boosted condition		–1	0	1	dB

DATA INPUT FORMAT

Three kinds of input format options are available by changing slot settings of D5, D6, and D7.

(1)

←—Input direction

D0	D1	D2	D3	D4	D5	D6	D7
SW1 1: A side 0: B side	SW2 1: A side 0: B side	SW3 1: A side 0: B side	SW4, 5 1: A side 0: B side	Empty slot	0	0	0

(2)

D0	D1	D2	D3	D4	D5	D6	D7
SW6, 7 1: A side 0: B side	SW8, 9 1: A side 0: B side	SW10, 11 1: A side 0: B side	SW26, 27 1: A side 0: B side	Empty slot	0	0	1

(3)

D0	D1	D2	D3	D4	D5	D6	D7
* Slots for tone control		* Slots for tone boost/cut and bass boost			0	1	0

* Switches 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, and 25 are operated according to the result of decoding setting code.

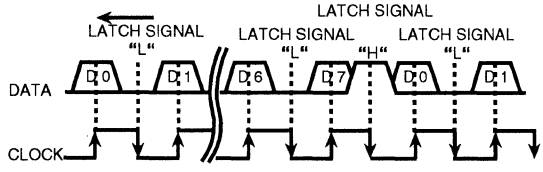
Setting code (tone control)

	D0	D1
BASS-BOOST	0	0
BASS	0	1
MID	1	0
TREBLE	1	1

Setting code (tone boost/cut and bass boost)

		D2	D3	D4
BOOST	0dB	0	0	0
	3dB	0	0	1
	6dB	0	1	0
	10dB	0	1	1
CUT	0dB	1	0	0
	−3dB	1	0	1
	−6dB	1	1	0
	−10dB	1	1	1

RELATIONSHIPS BETWEEN DATA AND CLOCK



Data signals are read at raising edges of pulse.
Latch signals are read at falling edges of pulse.

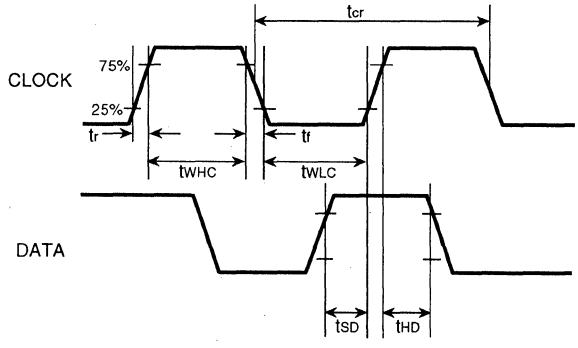
DIGITAL BLOCK INPUT CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IL}	Input voltage ("L" level)	DATA and CLOCK pins		0	~	$0.2V_{DD}$	V
V_{IH}	Input voltage ("H" level)			$0.8V_{DD}$	~	V_{DD}	
I_{IL}	Input current ("L" level)	$V_I = 0$	DATA and CLOCK pins	−10	–	10	μA
I_{IH}	Input current ("H" level)	$V_I = V_{DD}$		–	–	10	

DIGITAL BLOCK TIMING REGULATION

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t_{cr}	CLOCK cycle time	4	–	–	μ sec
t_{WHC}	CLOCK pulse width ("H" level)	1.6	–	–	
t_{WLC}	CLOCK pusle width ("L" level)	1.6	–	–	
t_r	CLOCK rise time	–	–	0.4	
t_f	CLOCK fall time	–	–	0.4	
t_{SD}	DATA setup time	0.8	–	–	
t_{HD}	DATA hold time	0.8	–	–	

CLOCK AND DATA TIMING



FUNCTION DESCRIPTION

(1) Tone controller equivalent circuit

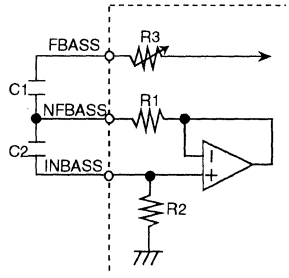


Fig.1 A circuit equivalent to the inside of the tone controller

Center frequency

$$f0 = 1 / 2\pi\sqrt{C1 \cdot C2 \cdot R1 \cdot R2}\ [Hz]$$

$$Q = \sqrt{(C2 \cdot R2) / (C1 \cdot R1)}$$

Example: Bass band (f = 150Hz)

R1 = 1.5kΩ , R2 = 56kΩ

C1 = 1.5μ , C2 = 0.01μ

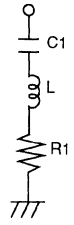
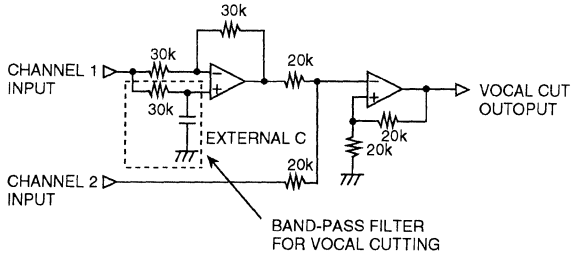


Fig.2 An equivalent circuit using L

(2) Vocal cut block equivalent circuit

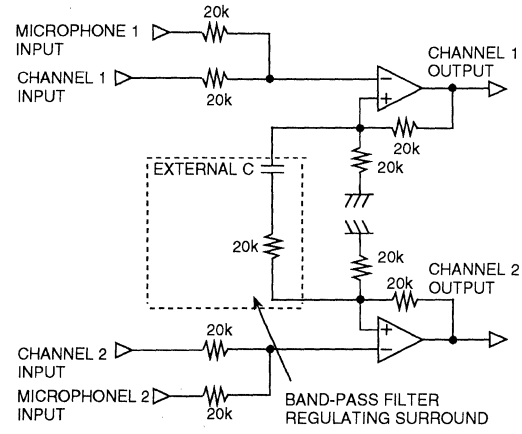


Note: The vocal cut output is monaural.

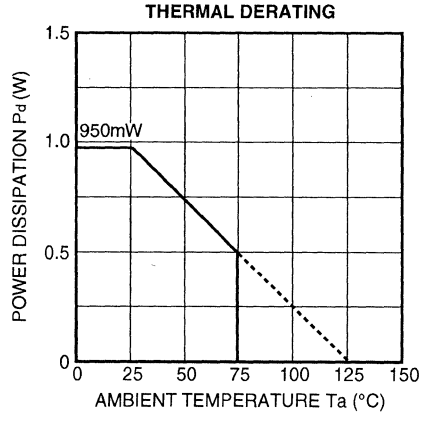
Fig.2 is equivalent to Fig.1. To convert component constants, the equation below is used.

L = C2 · R1 · R2

(3) Surround block equivalent circuit



TYPICAL CHARACTERISTICS

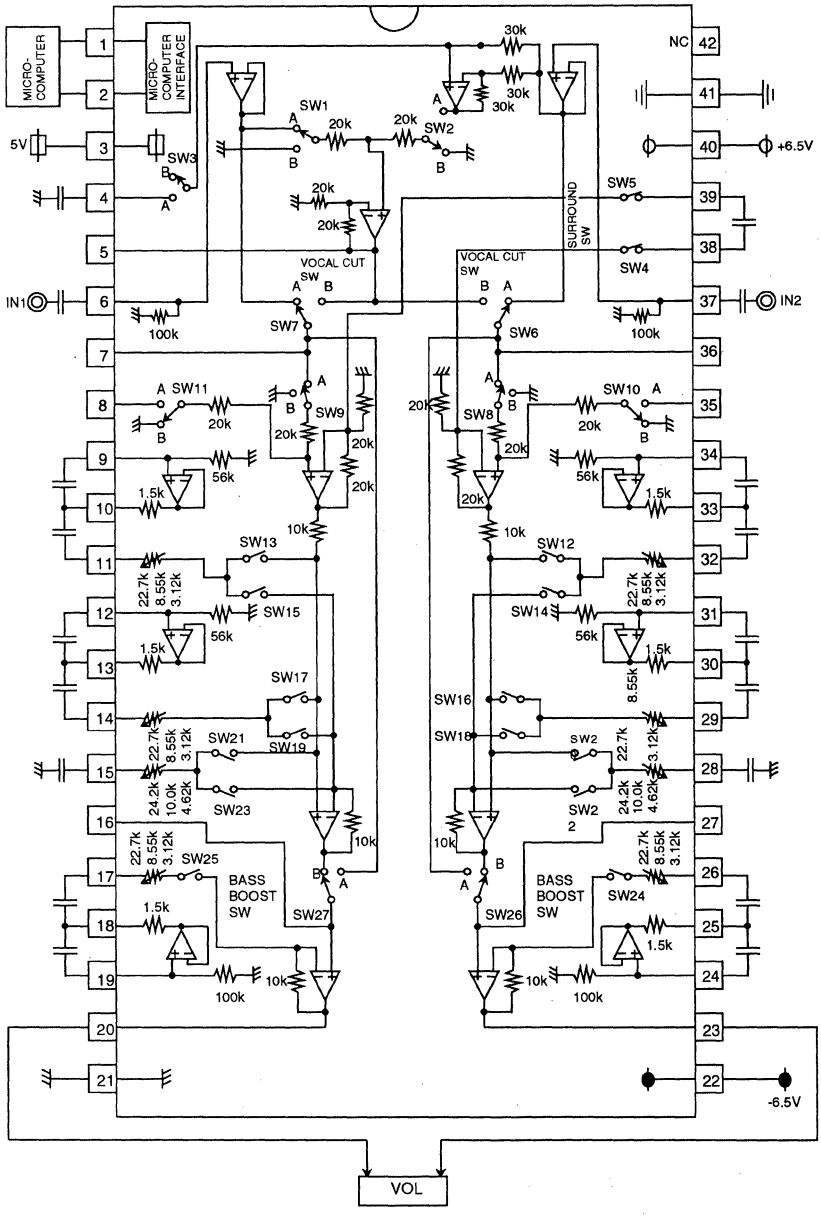


APPLICATION EXAMPLE

(1) M62422FP analog surround mode

Switch settings

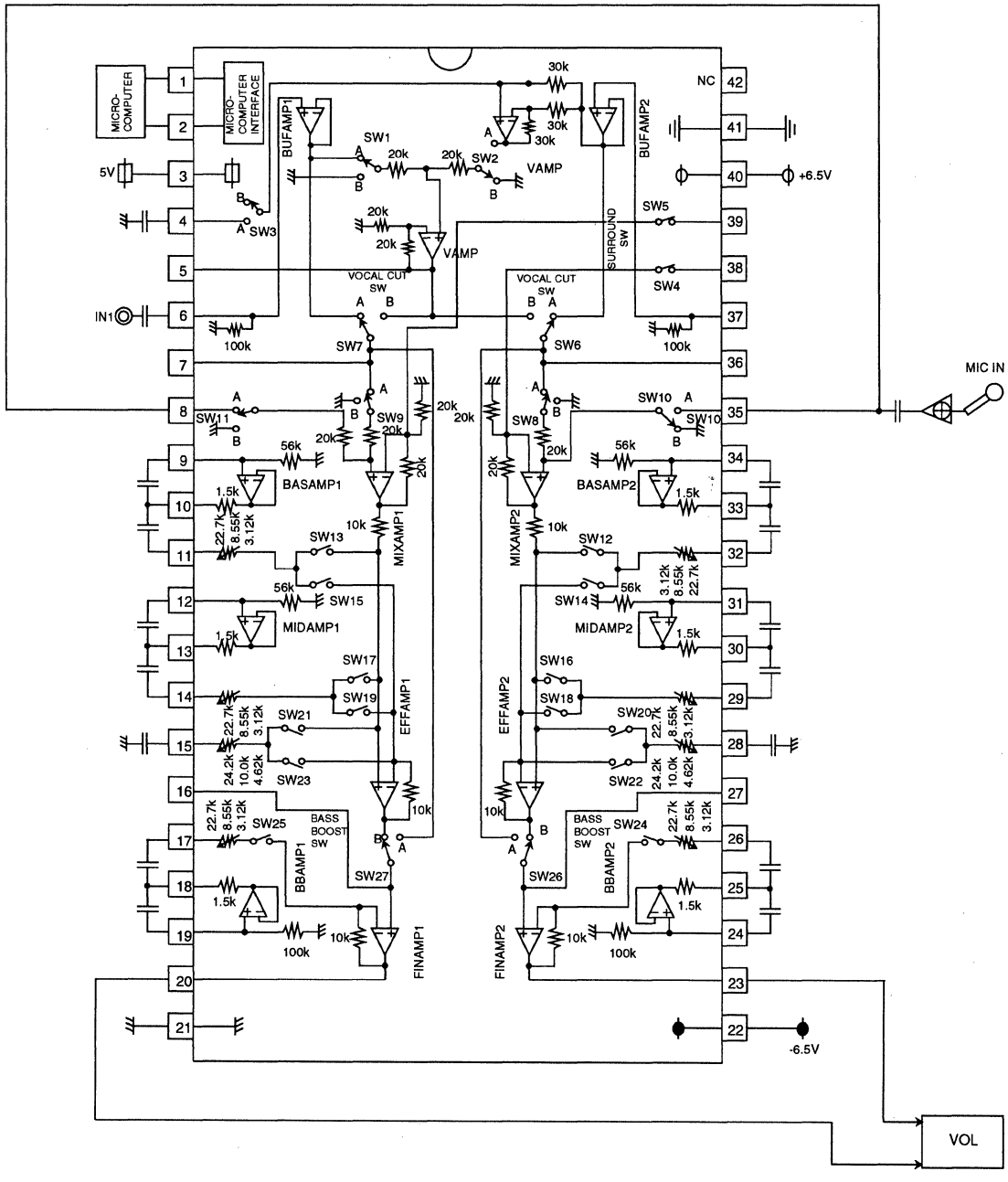
	SW1	SW2	SW3	SW4 SW5	SW6 SW7	SW8 SW9	SW10 SW11
Polarity	×	×	×	ON	A	A	B



(2) M62422FP sound-multiplex karaoke channel 1

Switch settings

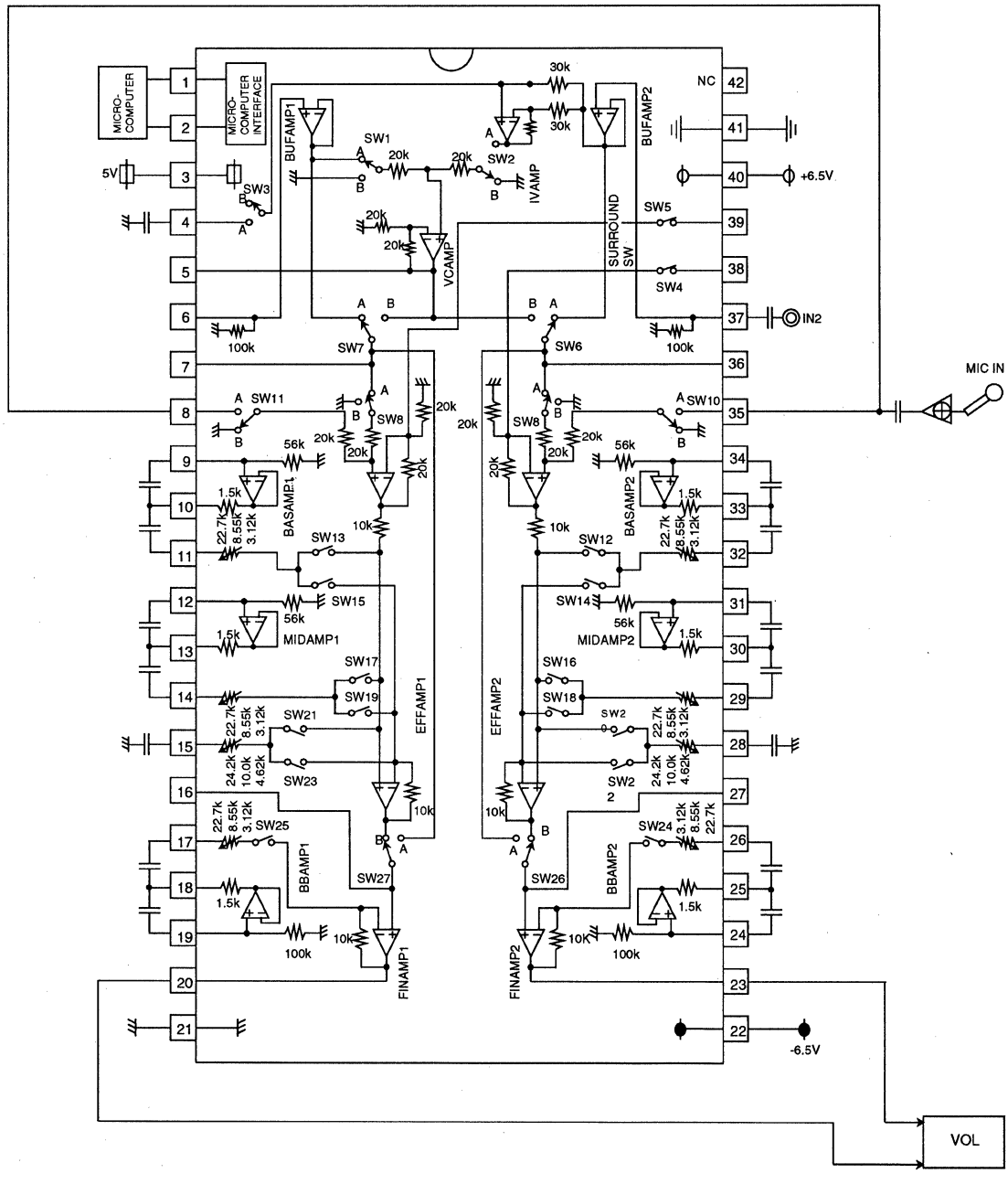
	SW1	SW2	SW3	SW4 SW5	SW6 SW7	SW8 SW9	SW10 SW11
Polarity	A	B	B	OFF	B	A	A



(3) M62422FP sound-multiplex karaoke channel 2

Switch settings

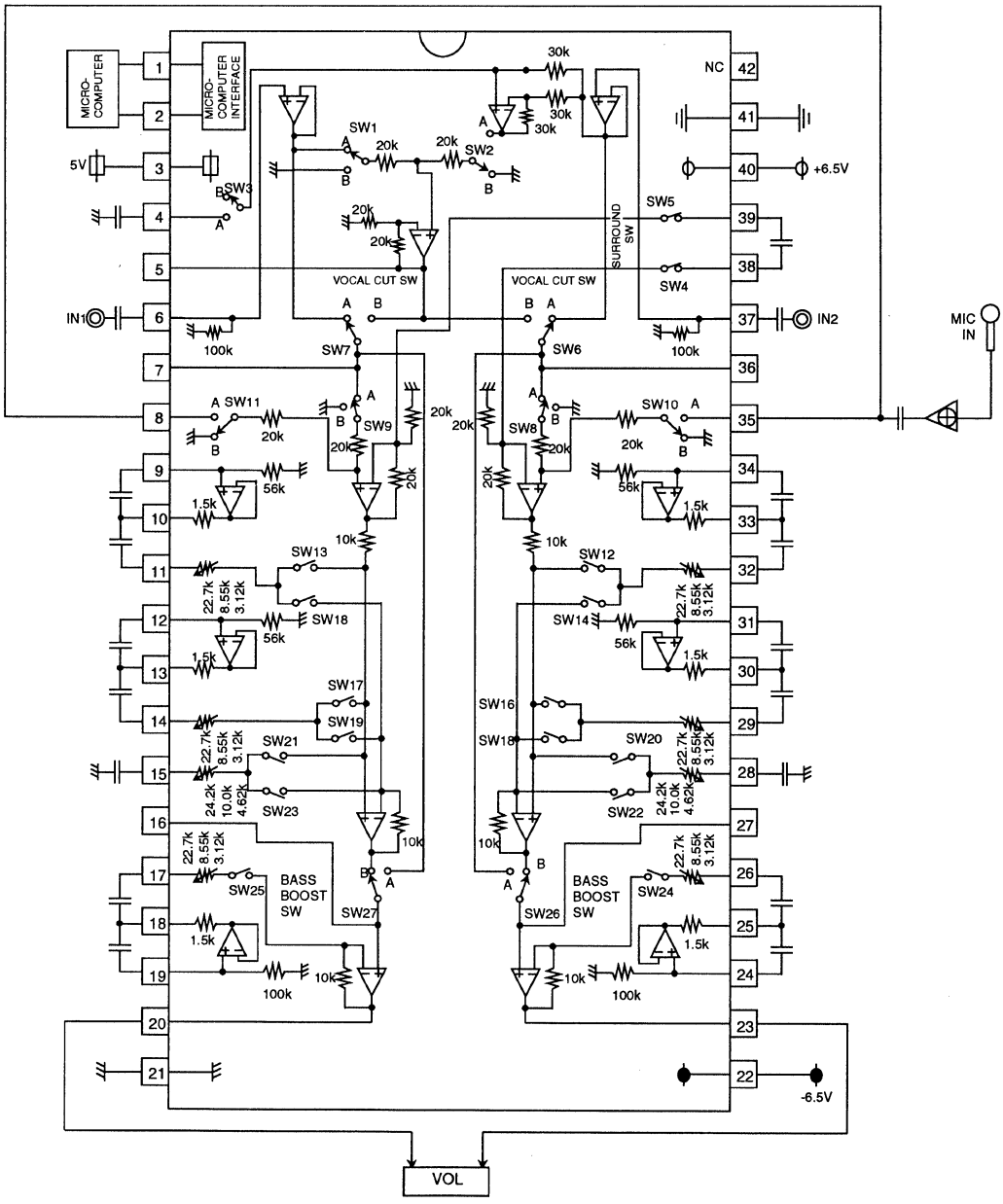
	SW1	SW2	SW3	SW4 SW5	SW6 SW7	SW8 SW9	SW10 SW11
Polarity	B	A	B	OFF	B	A	A



(4) M62422FP stereo karaoke

Switch settings

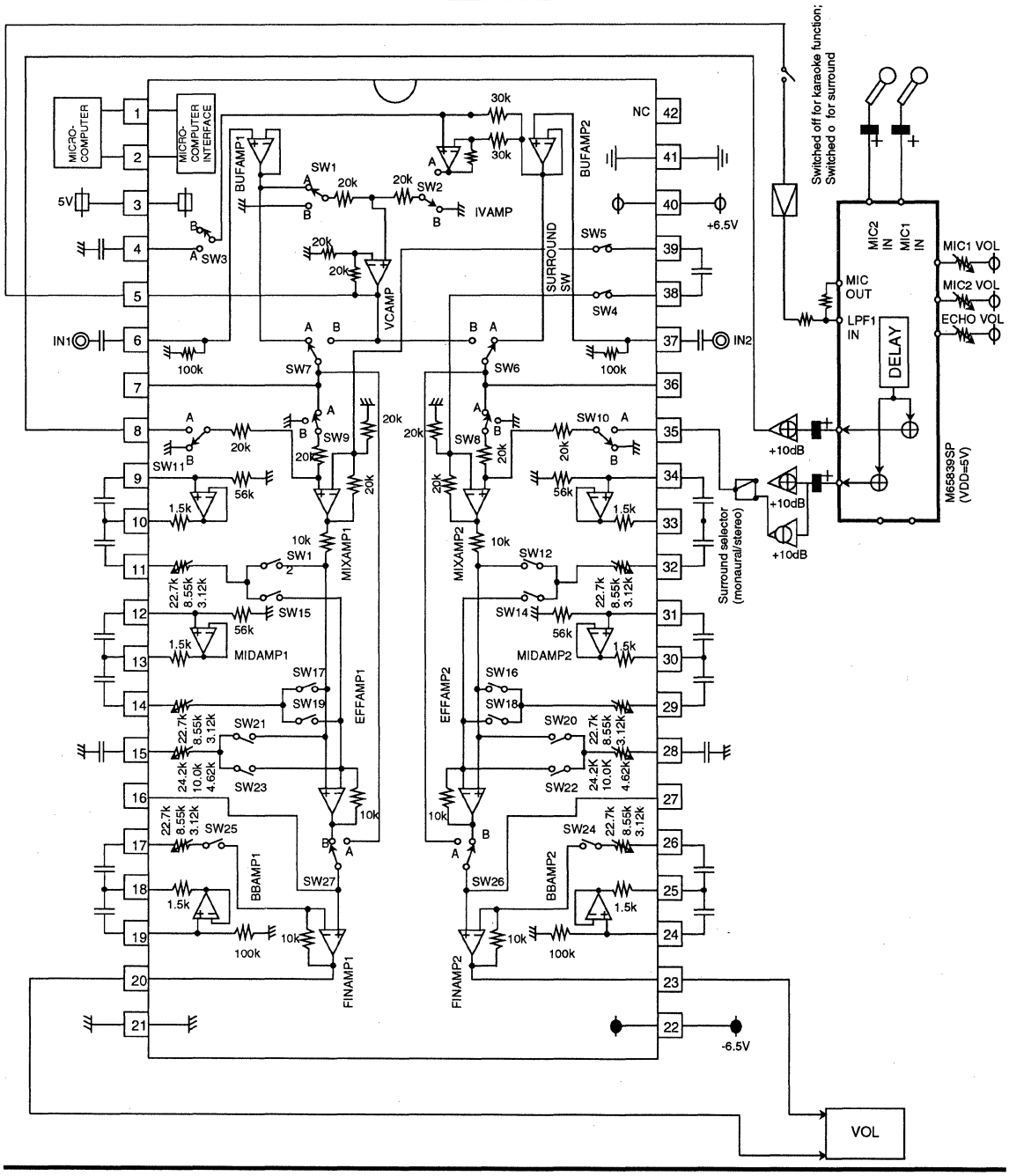
		SW1	SW2	SW3	SW4 SW5	SW6 SW7	SW8 SW9	SW10 SW11
Polarity	Vocal cut enabled	A	A	A	OFF	B	A	A
	Vocal cut disabled	×	×	×	OFF	A	A	A



(5) M62422FP + M65839SP stereo karaoke with echo effects (Supporting digital surround)

Switch settings

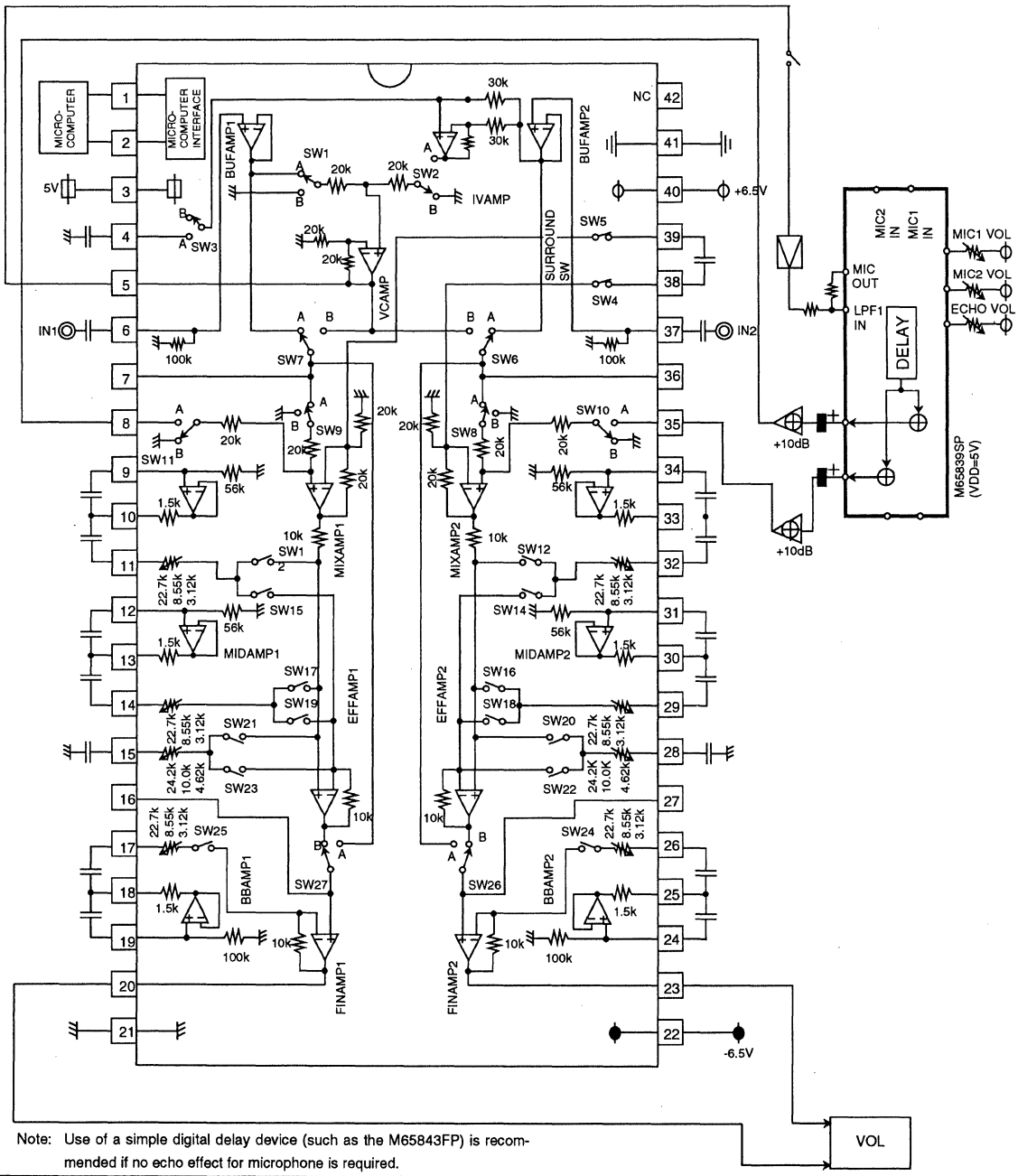
		SW1	SW2	SW3	SW4 SW5	SW6 SW7	SW8 SW9	SW10 SW11
Polarity	Vocal cut enabled	A	A	A	OFF	B	A	A
	Vocal cut disabled	×	×	×	↑	A	↑	↑



(6) M62422FP + M65839SP digital surround (Monaural)

Switch settings

		SW1	SW2	SW3	SW4 SW5	SW6 SW7	SW8 SW9	SW10 SW11
Polarity	Vocal cut enabled	A	A	A	OFF	B	A	A
	Vocal cut disabled	×	×	×	↑	A	↑	↑

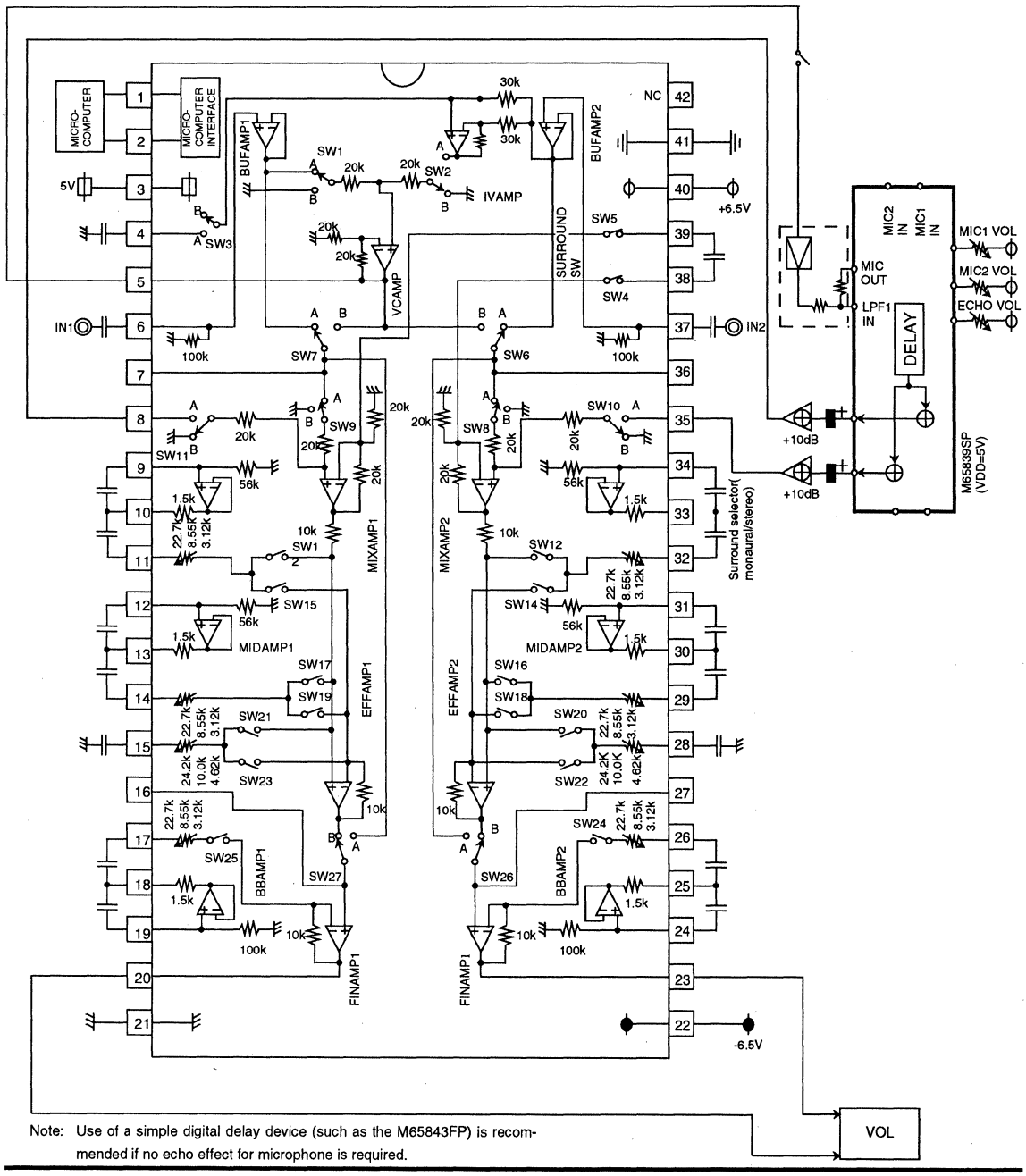


Note: Use of a simple digital delay device (such as the M65843FP) is recommended if no echo effect for microphone is required.

(7) M62422FP + M65839SP digital surround (Stereo)

Switch settings

		SW1	SW2	SW3	SW4 SW5	SW6 SW7	SW8 SW9	SW10 SW11
Polarity	Vocal cut enabled	A	A	A	OFF	B	A	A
	Vocal cut disabled	×	×	×	↑	A	↑	↑

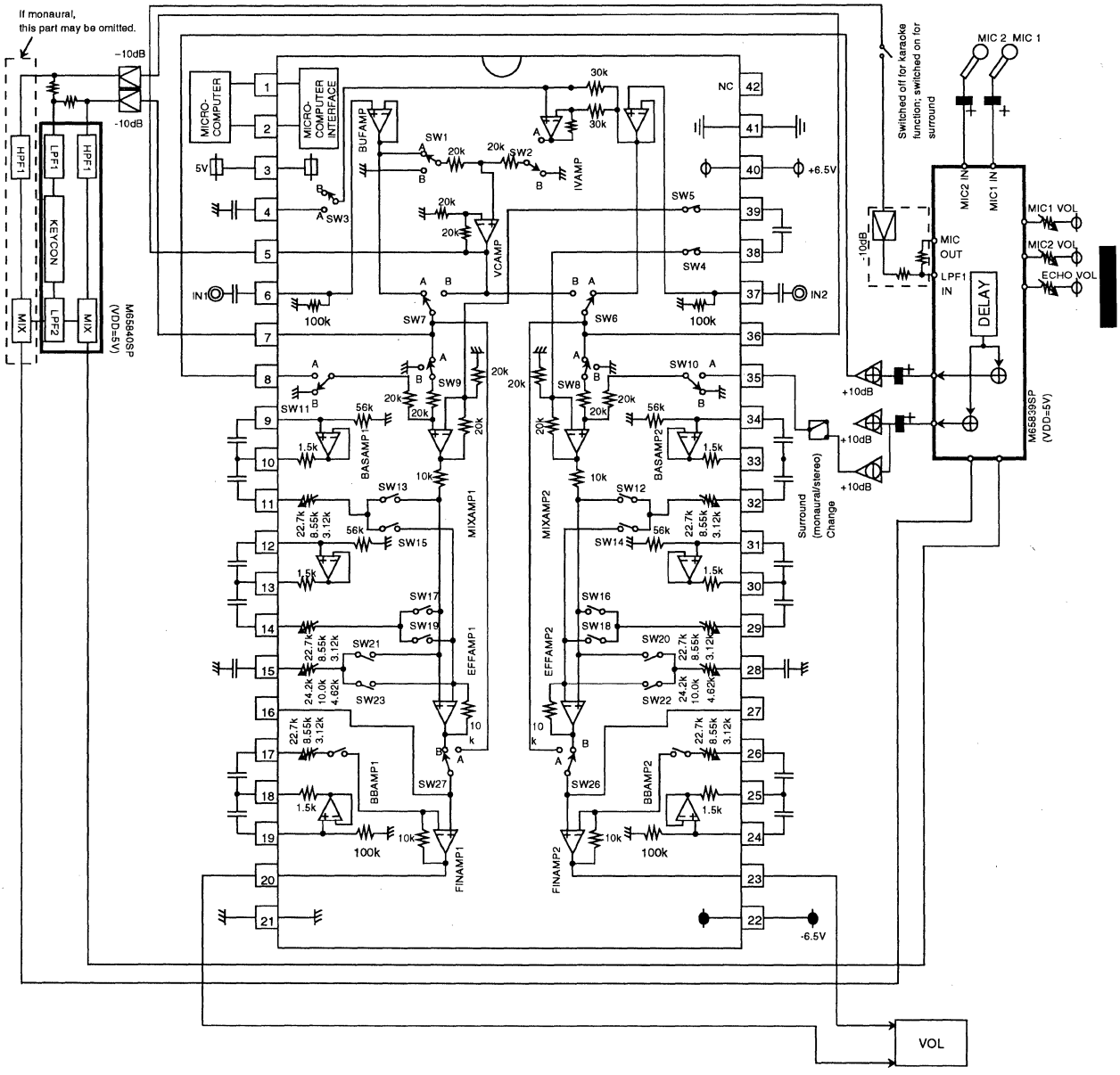


Note: Use of a simple digital delay device (such as the M65843FP) is recommended if no echo effect for microphone is required.

(8) M62422FP + M65839SP + M65840SP stereo karaoke with echo effects and key control

Switch settings

		SW1	SW2	SW3	SW4 SW5	SW6 SW7	SW8 SW9	SW10 SW11
Polarity	Vocal cut disabled	A	A	A	OFF	B	B	A
	Vocal cut enabled	×	×	×	OFF	A	B	A



Note: As the dynamic range the M65840FP can cover is narrow, a-12-dB attenuator is recommended.

M62423FP

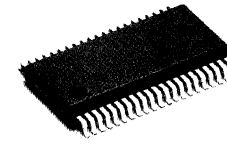
DIGITAL SOUND CONTROLLER FOR MINIATURE UNIT AUDIO SYSTEMS, WITH KARAOKE

DESCRIPTION

The M62423FP is a digital sound controller IC for miniature unit audio systems. The IC, with serial data sent from a microcomputer, makes it easy to realize karaoke functions (voice canceling) and tone quality/sound field control such as surround and 3-band tone control.

FEATURES

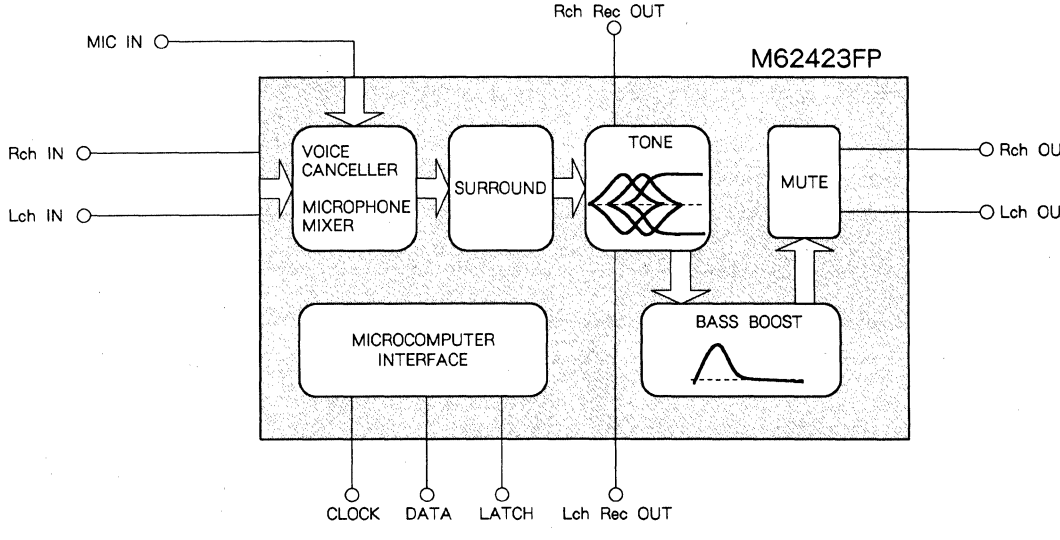
- 32-pin shrink DIP
- Capable of controlling each function by serial data
  - Bass/treble/Mid ····· 0, ± 3, ± 6, ± 10dB
  - Surround ····· [ON/OFF]
  - Bass boost ····· [ON/OFF]
  - Voice canceling ····· [ON/OFF]
  - Mute ····· [ON/OFF]



Outline 42P2R-A

0.8mm pitch 450mil SSOP
(8.4mm × 17.5mm × 2.0mm)

SYSTEM CONFIGURATION

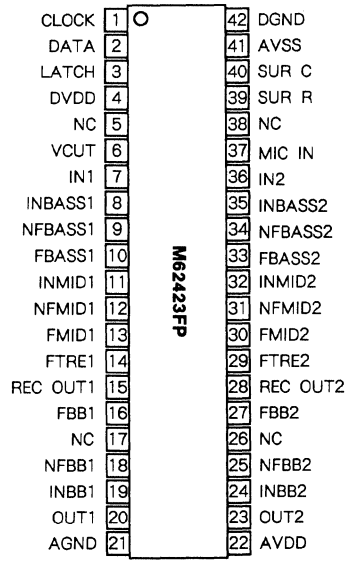


MITSUBISHI ELECTRIC

M62423FP

DIGITAL SOUND CONTROLLER FOR MINIATURE UNIT AUDIO SYSTEMS, WITH KARAOKE

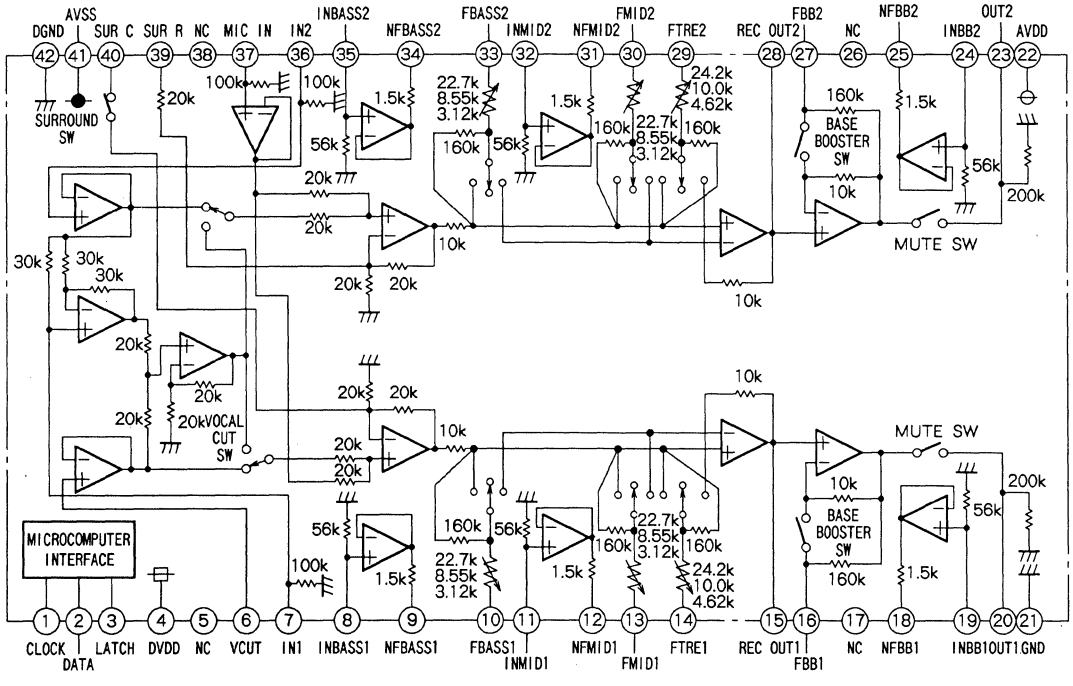
PIN CONFIGURATION



Outline 42P2R-A

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
AV_{DD}, AV_{SS}	Analog supply voltage	± 8.5	V
DV_{DD}	Digital supply voltage	7.0	V
P_d	Power dissipation (Ta ≦ 25℃)	1250	mW
K_θ	Thermal derating (Ta > 25℃)	9.5	mW/℃
T_{opr}	Operating temperature	−20~+75	℃
T_{stg}	Storage temperature	−55~+125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, AV_{DD} = 7V, AV_{SS} = − 7V, DV_{DD} = 5V, unless otherwise noted. Tone control and bass boost are set to 0dB.)

(1) Power supply characteristics

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
AI_{DD}	Circuit current of analog positive power supply	Current at pin ㉘ with AV_{DD} = 7V, AV_{SS} = − 7V No signal	−	22	−	mA
AI_{SS}	Circuit current of analog negative power supply	Circuit current at pin ㉑ with AV_{DD} = 7V, AV_{SS} = − 7V No signal	−	− 22	−	mA
DI_{DD}	Circuit current of digital power supply	Current at pin ④ with DV_{DD} = 5V No signal	−	0	−	μA

(2) Characteristics of the digital block

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IL}	Input voltage ("L" level)	CLOCK, DATA, LATCH pins		0	−	0.3•DV_{DD}	V
V_{IH}	Input voltage ("H" level)			0.7•DV_{DD}	−	DV_{DD}	V
I_{IL}	Output voltage ("L" level)	V_{IN} = 0	CLOCK, DATA, LATCH pins	−10	−	10	μA
I_{IH}	Input current ("H" level)	V_{IN} = DV_{DD}		−	−	10	μA
F_{CIK}	CLOCK frequency			−	−	250	kHz
t_{WHC}	CLOCK pulse width			4.0	−	−	μS
t_{SD}	DATA setup time			1.0	−	−	μS
t_{HD}	DATA hold time			1.0	−	−	μS
t_{WHI}	LATCH pulse width			2.0	−	−	μS
t_{SI}	LATCH setup time			1.0	−	−	μS

(3) Input/Output characteristics

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
R_{IN}	Input resistance	Pin ⑦, ㊱, Ta = 25℃	50	100	200	kΩ
V_{IM}	Max. input voltage	Input to pin ⑦, ㊱, ㊲, output from pin ⑳, ㉓	3.0	4.0	–	Vrms
V_{ODC}	Output pin voltage	Pin ⑳, ㉓, no signal	−0.15	0	0.15	V
V_{RECDC}		Pin ⑮, ⑱, no signal	−0.1	0	0.1	V
G_V	Pass gain	V_{IN} = 1Vrms, flat. pin ⑳, ㉓ − ⑦, ㊱ gains	−1	0	1	dB
V_{ONO}	Output noise voltage	JIS-A filter, no signal, Rg = 10k Ω, pin ⑳, ㉓	–	7.0	20	μVrms
V_{RECNO}		JIS-A filter, no signal, Rg = 10k Ω, pin ⑮, ㉘	–	5.5	15	μVrms
THD	Distortion factor	pin ⑳, ㉓. V_O = 0.5Vrms, R_L = 30k Ω	–	0.02	0.8	%
THD_{REC}		pin ⑮, ㉘. V_O = 0.5Vrms, R_L = 10k Ω	–	0.01	0.4	%
CT	Crosstalk between channels	Between pin ⑦, ㊱ − ⑳, ㉓ lines, V_O = 1Vrms, R_L = 30k Ω	−60	−65	–	dB
CT_{REC}		Between pin ⑦, ㊱ − ⑮, ㉘ lines, V_O = 1Vrms, R_L = 10k Ω	−60	−65	–	dB

(4) Tone control characteristics

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
G_{BOOST1}	Tone control voltage gain	3dB	f = 1kHz, V_O = 1Vrms, Input pin ⑦, ㊱ − output pin ⑳, ㉓ gain	2	3	4	dB
G_{BOOST2}		6dB		5	6	7	dB
G_{BOOST3}		10dB		8.5	10	11.5	dB
G_{CUT1}		−3dB		−4	−3	−2	dB
G_{CUT2}		−6dB		−7	−6	−5	dB
G_{CUT3}		−10dB		−11.5	−10	−8.5	dB
B_{ALTON}	Balance between channels	f = 1kHz, V_O = 1Vrms, Each of boost and cut conditions		−1	0	+1	dB

(5) Bass boost characteristics

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
G_{DD}	Bass boost voltage gain	f = 1kHz, V_O = 1Vrms Pin ⑳, ㉓, R_L = 3.3k	8.5	10	11.5	dB
B_{ALDD}	Graphic equalizer balance between channels	f = 1kHz, V_O = 1Vrms, Defference in pin ⑳ − ㉓ gain	−1	0	+1	dB

(6) Microphone amplifier input/output characteristics

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
R_{micin}	Input resistance	Pin ㉘	50	100	200	kΩ
V_{IMmic}	Max. input voltage	FLAT, R_L = 30kΩ, THD = 1 %, Measure input at pin ㊲, outputs at pin ⑳, ㉓	3.0	4.0	–	Vrms
G_{Vmic}	Pass gain	pin ⑳, ㉓ − ㊲ voltage gains, V_O = 0.5Vrms, R_L = 30kΩ	−2	0	2	dB
THD_{mic}	Distortion factor	pin ⑳, ㉓ V_O = 0.5Vrms, R_L = 30kΩ	–	0.02	0.8	%
B_{ALmic}	Balance between channels	Difference in voltage gain between pin ⑳, ㉓	−1	0	1	dB

DIGITAL CONTROL SPECIFICATIONS

Digital format

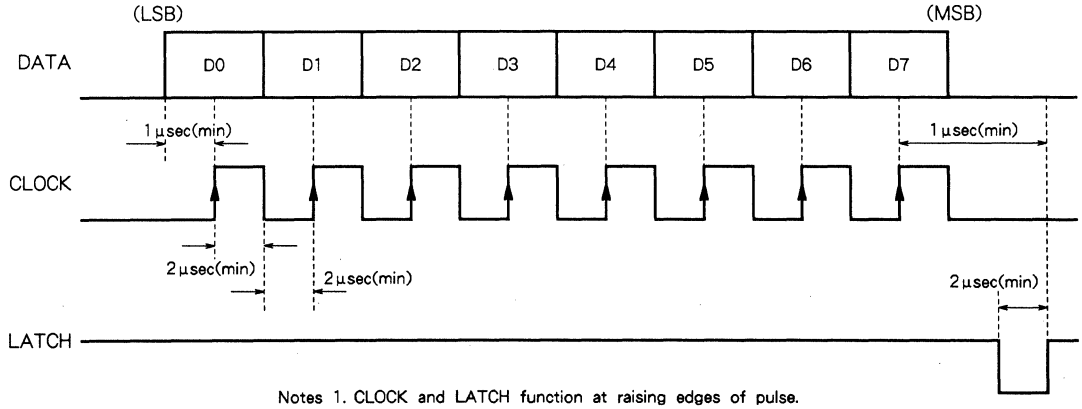
	D7	D6	D5	D4	D3	D2	D1	D0	
DATA 0 (MSB)	MODE SELECT 0	BASS BOOST OFF/ON	SURROUND OFF/ON	OUTPUT MUTE OFF/ON	VOCAL CUT OFF/ON	——	——	——	(LSB)
DATA 1 (MSB)	MODE SELECT 1	TONE CONTROL MODE 01 : BASS 10 : TREBLE 11 : MID		——	——	BOOST/CUT VOLUME			(LSB)

	Signal name	Function		Signal name	Function
D0	–	Fixed to "0"	D0	Tone boosting/ cutting volume	See table below
D1	–	Fixed to "0"	D1		
D2	–	Fixed to "0"	D2		
D3	Vocal cut	Vocal cut disabled by "0" Vocal cut enabled by "1"	D3	–	Fixed to "0"
D4	Output mute	Output mute disabled by "0" Output mute enabled by "1"	D4	–	Fixed to "0"
D5	Sorround	Sorround disabled by "0" Sorround enabled by "1"	D5	Tone control mode	See table below
D6	Bass boost	Bass boost disabled by "0" Bass boost enabled by "1"	D6		
D7	Mode select	Data 0 is selected by "0"	D7	Mode select	Data 1 is selected by "1"

D2	D1	D0	Boosting / cutting volume	D2	D1	D0	Boosting / cutting volume
0	0	0	+0dB	1	0	0	−0dB
0	0	1	+3dB	1	0	1	−3dB
0	1	0	+6dB	1	1	0	−6dB
0	1	1	+10dB	1	1	1	−10dB

D5	D6	Mode
0	1	Bass
1	0	Treble
1	1	MID

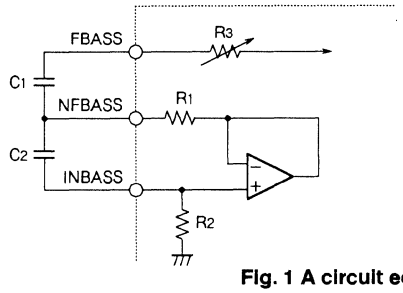
DATA TIMING (Recommended conditions)



Notes 1. CLOCK and LATCH function at raising edges of pulse.
2. High level : 3.5V min. ; Low level : 1.5V max.

FUNCTION DESCRIPTION

(1) Tone controller equivalent circuit



CENTER FREQUENCY

$10 = 1/2\pi\sqrt{C1 \cdot C2 \cdot R1 \cdot R2}$ [Hz]

$Q = \sqrt{(C2 \cdot R2) / (C1 \cdot R1)}$

EXAMPLE : BASS BAND (f = 150Hz)
R1 = 1.5k Ω, R2 = 56k Ω
C1 = 0.82 μ, C2 = 0.015 μ

Fig. 1 A circuit equivalent to the inside of the tone controller

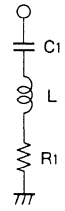
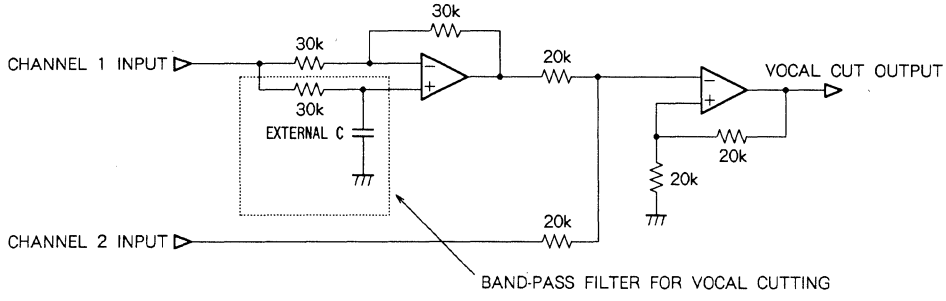


Fig. 2 is equivalent to Fig.1. To convert compoment constants, the equation below is used.

$L = C2 \cdot R1 \cdot R2$

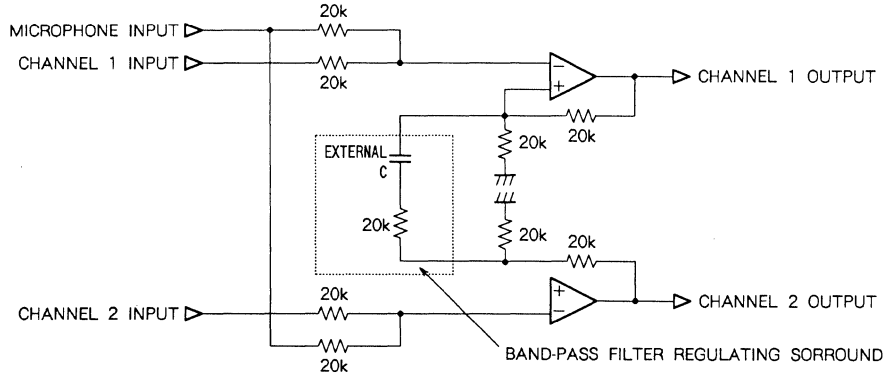
Fig. 2 An equivalent circuit using L

(2) Vocal cut block equivalent circuit

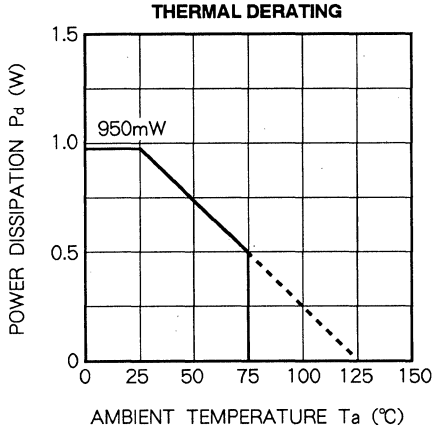


Note. The vocal cut output is monaural.

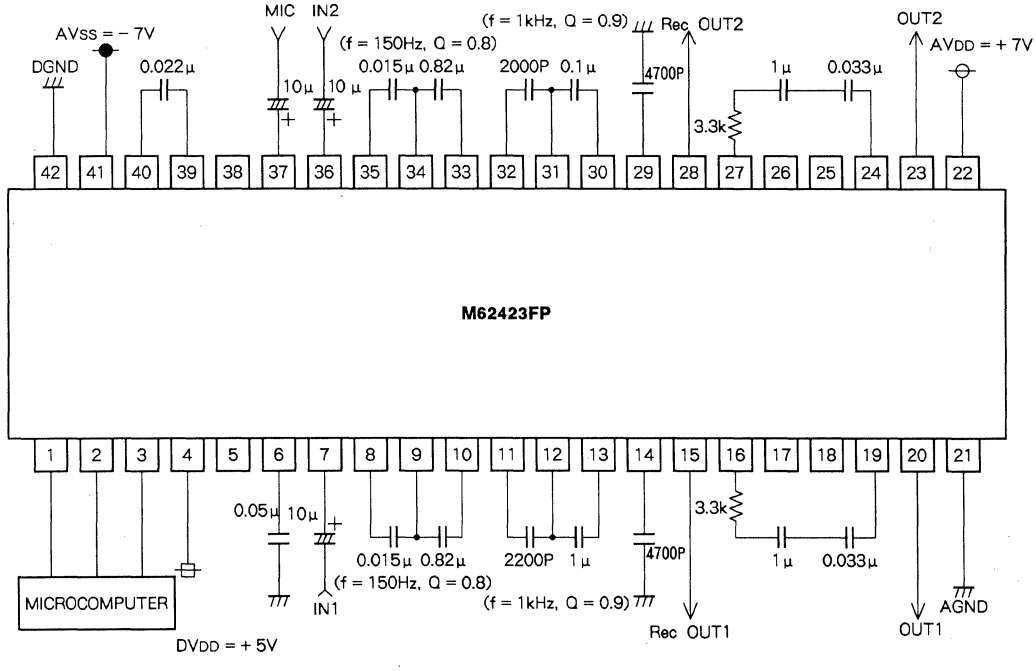
(3) Surround block equivalent circuit



TYPICAL CHARACTERISTICS



APPLICATION EXAMPLE



Unit Capacitance : F

M51132L,FP

2 CHANNEL ELECTRONIC VOLUME•BALANCE

DESCRIPTION

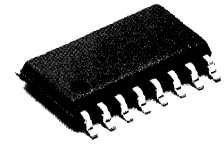
The M51132 is a VCA (Voltage Controlled Amplifier) IC developed as an electronic volume control for audio-visual equipment. The IC is used to process small analog signals at the stage before power amplifier. Right/left independent volume control or right/left simultaneous volume control can be selected by DC voltages. Its built-in pass through function, in combination with an ALC amplifier, offers the capability of automatic level control.

FEATURES

- Two control modes can be selected.
  (Left/right independent volume control mode or left/right simultaneous volume + balance control mode).
- Pass through switch is included to output the input signal as it is, irrespective of the volume/balance control voltages.
- Shock noise reduction pin is provided to reduce pass through switch on/off shock noise.
- Built-in reference supply voltage circuit
  ..... output current 10mA (typ)
- Maximum input ..... 3.4Vrms (typ)
  (f = 1kHz, THD = 1%)
- Low distortion ..... 0.005% (typ)
- Good channel separation ..... 102dB (typ)
  (f = 1kHz, Vo = 2Vrms, IHF − A)

Outline 14P5A(L)

1.27mm pitch 325mil ZIP
(2.8mm × 19.0mm × 6.3mm)



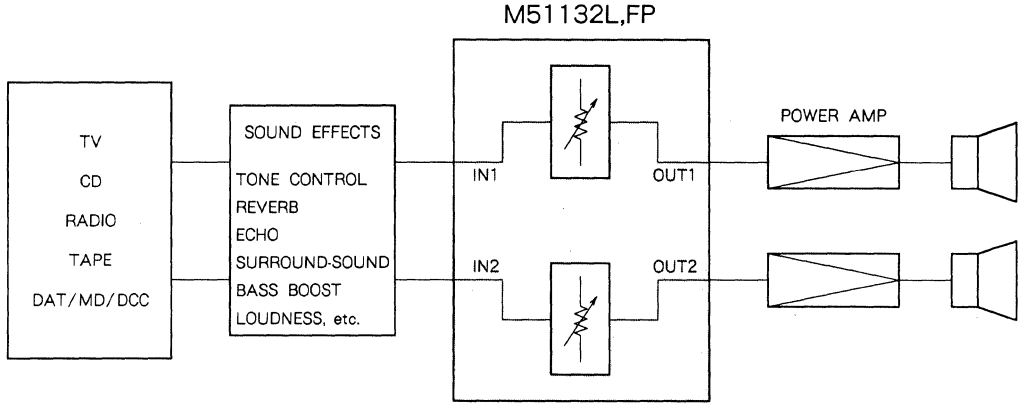
Outline 16P2N-A(FP)

1.27mm pitch 300mil SOP
(5.3mm × 10.1mm × 1.8mm)

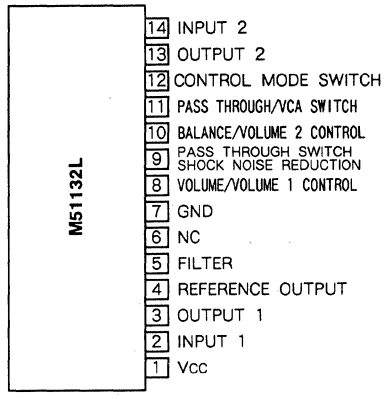
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 8~15V
Rated supply voltage ..... V_{CC} = 12V

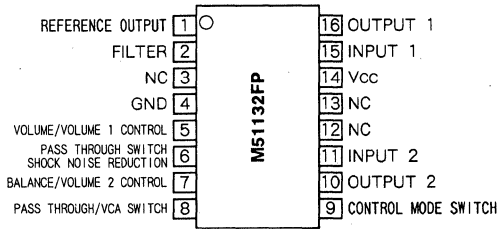
SYSTEM CONFIGURATION



PIN CONFIGURATION



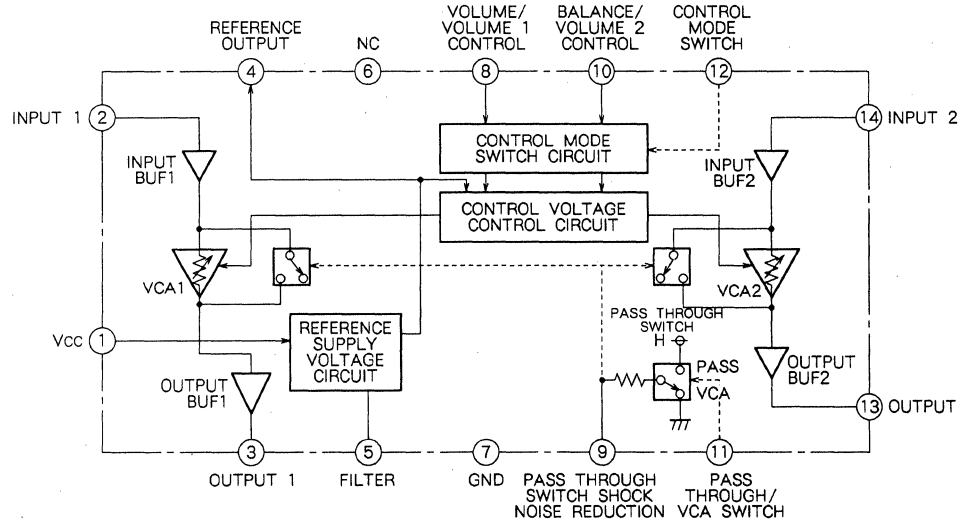
Outline 14P5A(L)



Outline 16P2N-A(FP)

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM (M51132L)



PIN DESCRIPTION

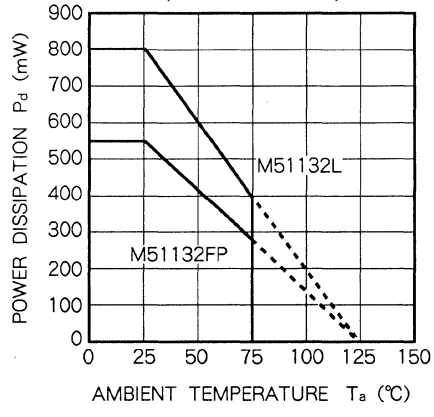
Pin No.	Name	Function	Typical DC voltage
①	Vcc	DC 8~15V is applied (rated voltage 12V)	
②	Input 1	Maximum input 3.4Vrms (typ.)	5.5V
③	Output 1		4.8V
④	Reference supply voltage output	Maximum output current 10mA(typ.)built-in short circuit protection circuit	5.2V
⑤	Filter		12V
⑥	No connection	Can be used for wire repeater to GND, etc.	
⑦	GND		
⑧	Volume/ volume 1 control	Left/right simultaneous volume or channel 1 volume is controlled by this value in the range of 0 to 5.2V DC.	
⑨	Pass through switch shock noise reduction	Transit noise to the ear is softened by slowly switching between pass through and VCA with time constant when the pass through switch is turned on/off. The time constant is determined by externally connected capacitor. T(sec) = 1.2 × C × 20k	5.2V for pass through and 0V for VCA
⑩	Balance/ volume 2 control	Balance or channel 2 volume is controlled with 0 to 5.2V.	
⑪	Pass through/VCA switch	Operates as VCA with 0V, and passes through the input to output with 5.2V.	
⑫	Control mode switch	Operates as channel 1 volume at pin ⑧ and as channel 2 volume at pin ⑩ with 0V. Operates as channel 1 and channel 2 simultaneous volume at pin ⑧ and as balance at pin ⑩ with 5.2V.	
⑬	Output 2		4.8V
⑭	Input 2	Maximum input 3.4Vrms (typ)	5.5V

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

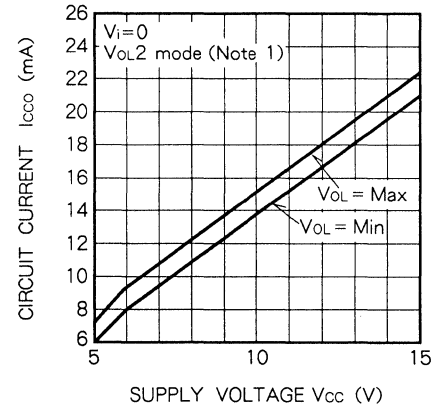
Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Quiescent	15.5	V
I_{CC}	Circuit current		40	mA
P_d	Power dissipation	When mounted on PC board	800(L) / 550(FP)	mW
K_θ	Thermal derating	Ta ≧ 25℃	8.0(L) / 5.5(FP)	mW/℃
T_{opr}	Operating temperature		−20~+75	℃
T_{stg}	Storage temperature		−40~+125	℃

TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)

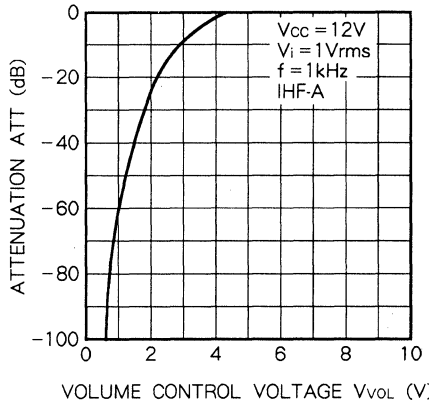


CIRCUIT CURRENT VS. SUPPLY VOLTAGE

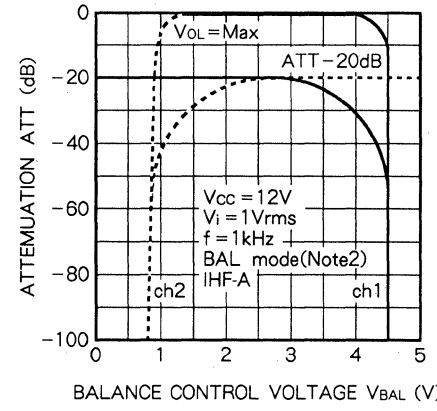


Note 1. VOL2 mode is left/right independent volume control mode.

ATTENUATION VS. VOLUME VOLTAGE CONTROL

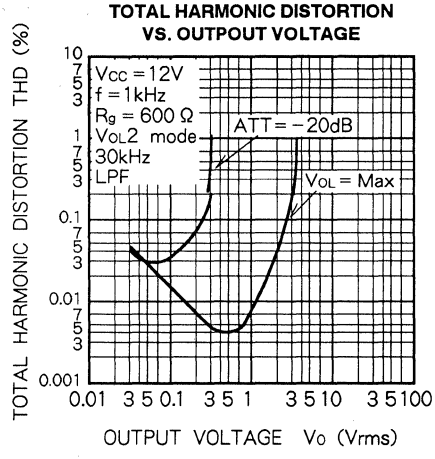


ATTENUATION VS. BALANCE CONTROL VOLTAGE

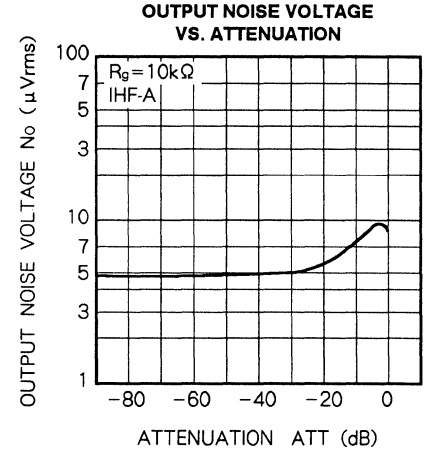


Note 2. BAL mode is left/right simultaneous volume and balance control mode.

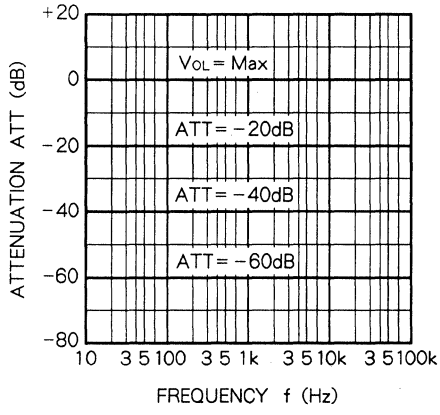
TOTAL HARMONIC DISTORTION VS. OUTPOUT VOLTAGE



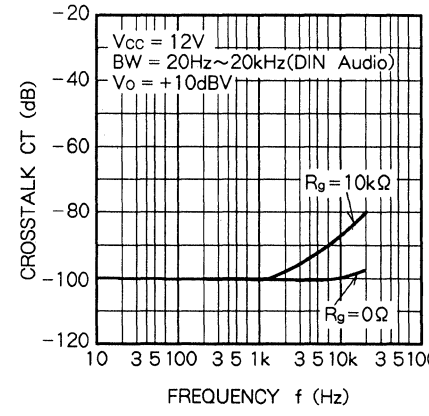
OUTPUT NOISE VOLTAGE VS. ATTENUATION



ATTENUATION VS. FREQUENCY CHARACTERISTICS

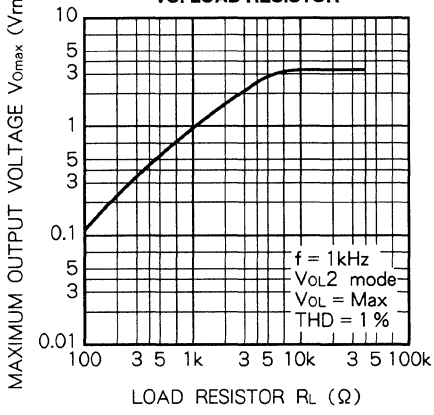


CROSSTALK VS. FREQUENCY CHARACTERISTICS

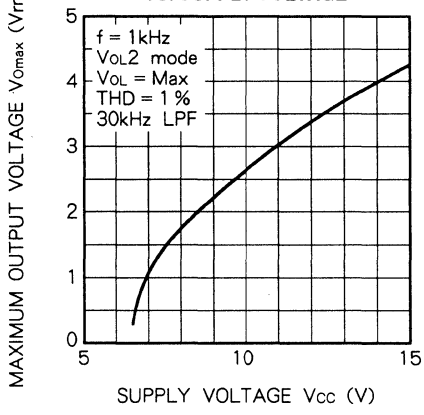


MITSUBISHI ELECTRIC

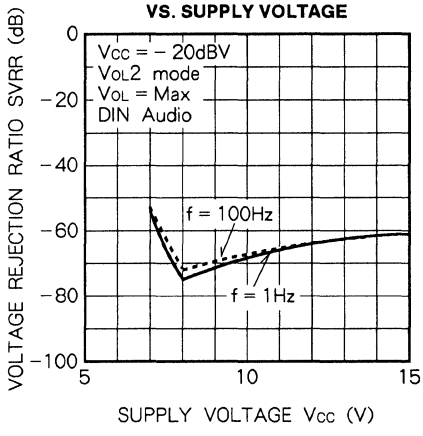
MAXIMUM OUTPUT VOLTAGE VS. LOAD RESISTOR



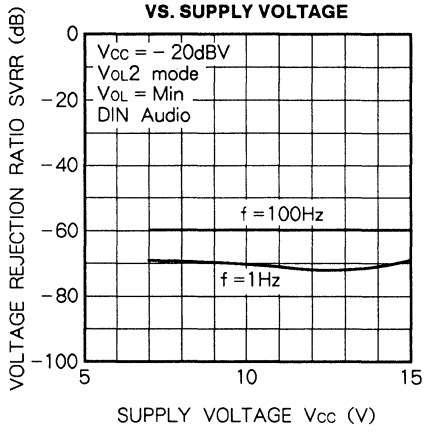
MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



VOLTAGE REJECTION RATIO VS. SUPPLY VOLTAGE



VOLTAGE REJECTION RATIO VS. SUPPLY VOLTAGE

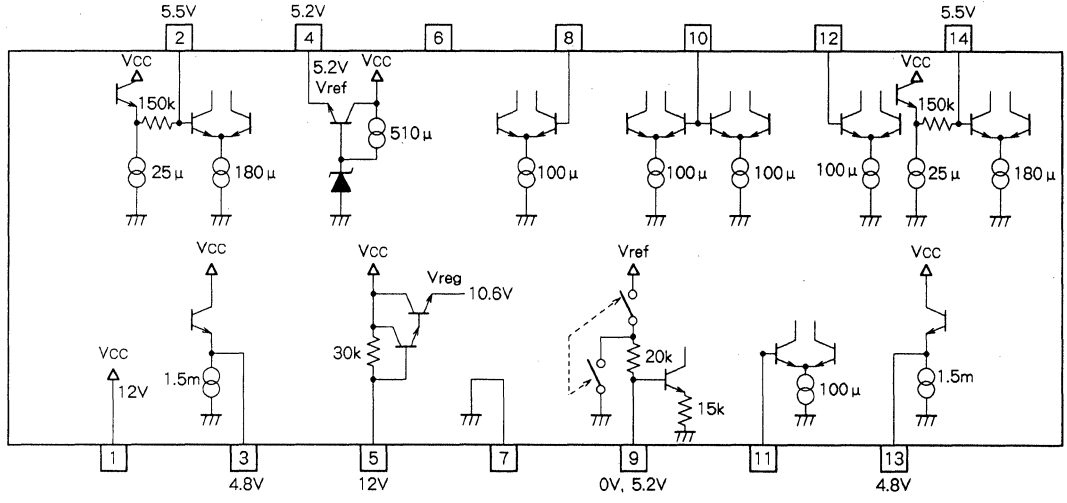


ELECTRICAL CHARACTERISTICS (Ta = 25℃, Vcc = 12V, f = 1kHz, Vi = 1Vrms, Volume Max, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Icco	Circuit current	In quiescent state, volume : min	9	17	30	mA
ATTo	Attenuation		−2	0	+2	dB
Att−∞		Vi = 2Vrms, IHF-A, volume : min		−105	−85	dB
CB	Channel balance		−2	0	+2	dB
THD	Total harmonic distortion	15kHz, LPF		0.01	0.1	%
Ri	Input resistor		5.0	150		kΩ
BAL	Balance attenuation	Vi = 2Vrms, IHF-A		−105	−85	dB
Nomin	Output noise voltage	Rg=10kΩ, in quiescent state, IHF-A, volume:min		4.8	10	μVrms
Nomax		Rg=10kΩ, in quiescent, IHF-A		9	20	μVrms
Vimax	Maximum input voltage	THD = 1%, volume : center	2	3.4		Vrms
Vomax	Maximum output voltage	THD = 1%	2	3.4		Vrms
CT	Crosstalk	Rg = 0Ω, Vi = 2Vrms, IHF-A		−102	−80	dB
GVP	Pass through voltage gain	Volume : min	−1.2	+0.8	+2.8	dB
CBP	Pass through channel balance	Volume : min	−2	0	+2	dB

Note 3. The volume max is the condition in which the same voltage as Vr is applied to pin ⑧.
4. The volume center is the condition in which the same voltage as Vr/2 is applied to pin ⑧.
5. The volume min is the condition in which pin ⑧ is connected to GND.

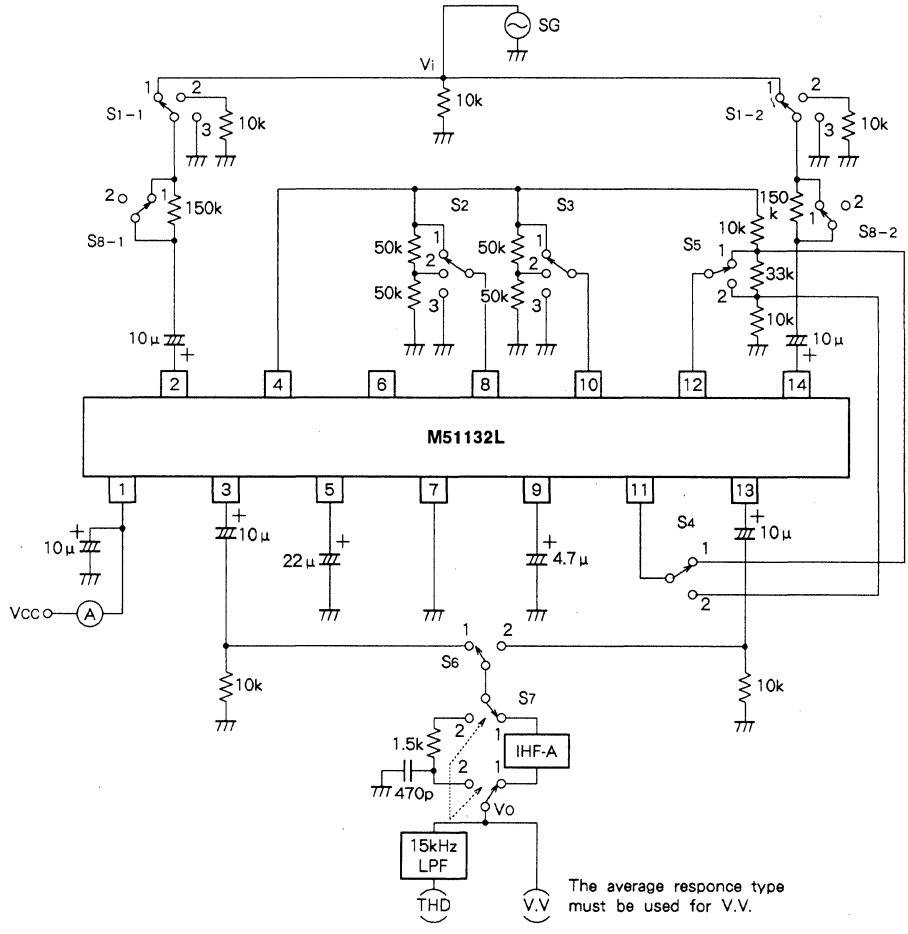
I/O INTERFACE (M51132L)



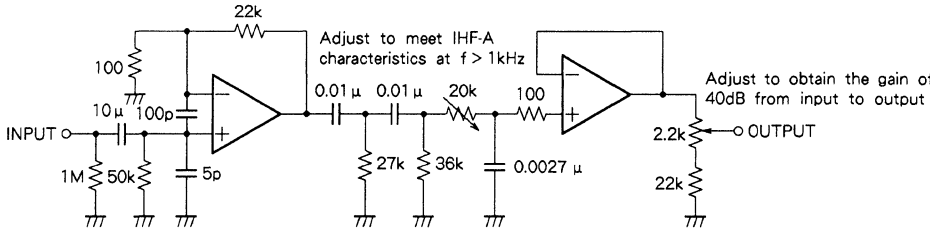
Note 6. All resistors, voltages, currents are shown in typical values.

Units Resistance : Ω
Voltage : V
Current : A

TEST CIRCUIT (M51132L)



The IHF-A filter can be replaced with the following circuit.
Example of IHF-A filter equivalent circuit (Note that the output is multiplied by 100).



Units Resistance : Ω
Capcitance : F

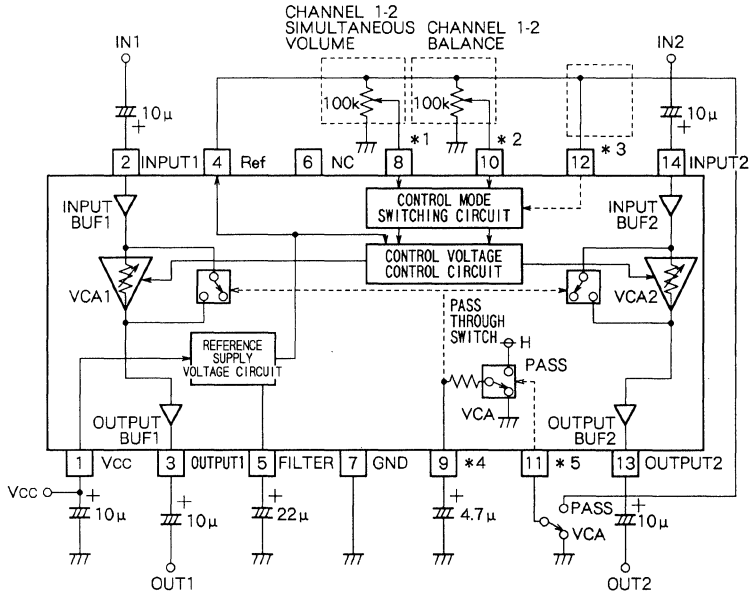
SWITCH CONDITION AND TEST METHOD

Symbol	Parameter	Switch										Test method
		S_{1-1}	S_{1-2}	S_2	S_3	S_4	S_5	S_6	S_7	S_{8-1}	S_{8-2}	
I_{CCO}	Circuit current	2	2	3	3	2	2	1	2	1	1	Measure the current flowing to pin ① in quiescent state
ATT_O	Attenuation	1	1	1	1/2	2	2/1	1/2	2	1	1	Obtain from the quation $ATT(dB) = 20\log(V_O/V_i)$ $ATT\text{-}\infty$ is IHF-A in
$A_{tt-\infty}$		1	1	3	3/2	2	2/1	1/2	1	1	1	
CB	Channel balance	1	1	1	1/2	2	2/1	1→2	2	1	1	$CB(dB) = ATT_{ch1} - ATT_{ch2}$
THD	Total harmonic distortion	1	1	1	1/2	2	2/1	1/2	2	1	1	15kHz LPF in
R_i	Input resistor	1	1	1	1	2	2	1/2	2	1→2	1→2	Given the output as V_{O1} when $S_8 \rightarrow 1$ and the output as V_{O2} when $S_8 \rightarrow 2$ $R_i(k\Omega) = 150/(V_{O1}/V_{O2} - 1)$
BAL	Balance attenuation	1	1	1	1/3	2	1	1/2	1	1	1	$BAL(dB) = 20\log(V_O/V_i)$
N_{Omin}	Output noise voltage	2	2	3	3/2	2	2/1	1/2	1	1	1	IHF-A in
N_{Omax}		2	2	1	1/2	2	2/1	1/2	1	1	1	IHF-A in
V_{imax}	Maximum input voltage	1	1	2	2	2	2/1	1/2	2	1	1	Input signal voltage when the output distortion rate is 1%.
V_{Omax}	Maximum output voltage	1	1	1	1/2	2	2/1	1/2	2	1	1	Output signal voltage when the output distortion rate is 1%.
C_T	Crosstalk	3/1	1/3	1	1	2	2	1/2	1	1	1	IHF-A in $C_T(dB) = 20\log$ $(V_O(Vrms)/2(Vrms))$
G_{VP}	Pass through voltage gain	1	1	3	3	1	2	1/2	2	1	1	$G_{VP}(dB) = 20\log(V_O/V_i)$
C_{BP}	Pass through cnannel balance	1	1	3	3	1	2	1→2	2	1	1	$C_{BP}(dB) = G_{Vpch1} - G_{Vpch2}$

Note 7. If the parameter is separated into two rows. All the switching conditions in the upper row and all the switching conditions in the lower row are measured.

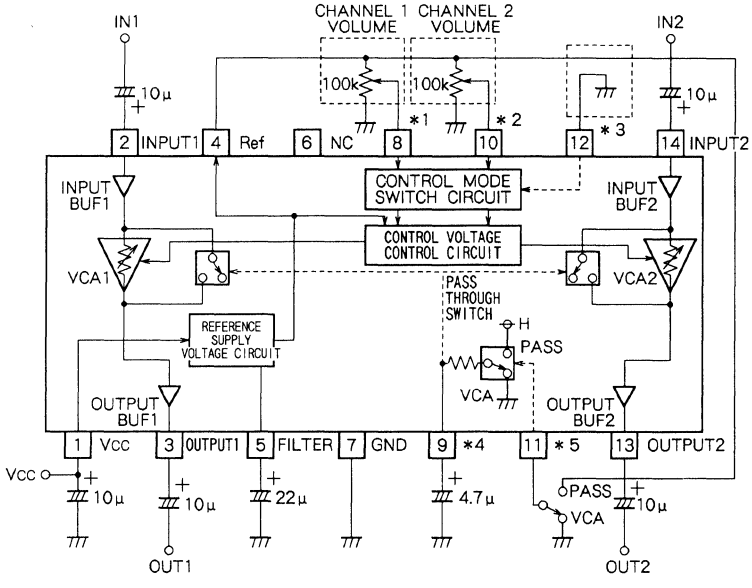
APPLICATION EXAMPLES (M51132L)

(a) Control by left/right simultaneous variable volume and balancer



*1 Volume/volume 1 control
*2 Balance/volume 2 control
*3 Control mode switch
*4 Pass through switch shock noise reduction
*5 Pass through/VCA switch

(b) Control by left/right independent volume



*1 Volume/volume 1 control
*2 Balance/volume 2 control
*3 Control mode switch
*4 Pass through switch shock noise reduction
*5 Pass through/VCA switch

Different between example (a) and (b)

Pin No.	Example (a)	Example (b)
⑧	Volume control	ch1 volume control
⑩	Balance control	ch2 volume control
⑫	Connected to pin ④	GND

Units Resistance : Ω
Capasitance : F

M51134P,FP

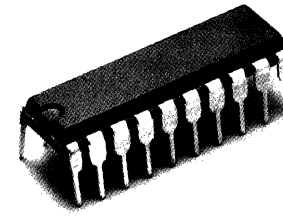
SUB-HORMONIZER FOR BASS EMPHASIS

DESCRIPTION

The M51134 is an IC developed for audio-visual applications to emphasize heavy bass. The IC is used to produce sound effects at the stage before power amplifier.

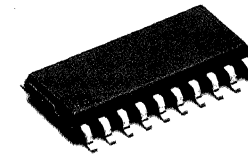
The M51134 offers capability of converting desired frequency into its half by setting a constant of external filter. The built-in VCA is also capable of level setting controlled by an externals source.

The IC is also suitable for 3-D systems.



Outline 20P4(P)

2.54mm pitch 300mil DIP
(6.3mm × 24.0mm × 3.3mm)



Outline 20P2N-A(FP)

1.27mm pitch 300mil SOP
(5.3mm × 12.6mm × 1.8mm)

FEATURES

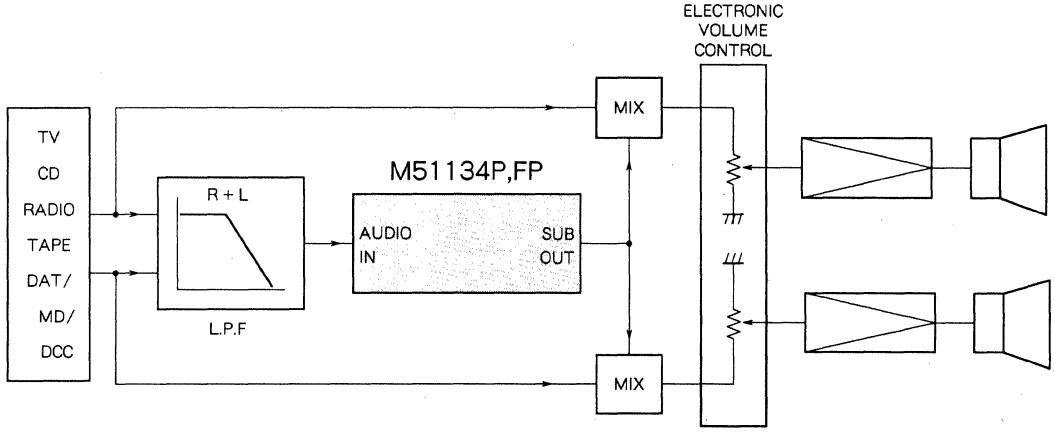
- Input sensitivity variable by input sensitivity adjust pin
- Built-in 5V regulator for single power supply
- Envelope detector facilitates level setting matching input level
- Capability of controlling VCA from external source facilitates level settings at will
- Maximum input voltage 3Vrms
- Low noise ..... – 92dBv
- Built-in OP-amp for low pass filter
- Built-in voltage control amplifier (VCA)
- Built-in Flip-Flop circuit for 1/2 frequency divider

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC1} = 7~15V, V_{CC2} = 4.5~5.5V

Rated supply voltage ..... V_{CC1} = 12V, V_{CC2} = 5V

SYSTEM CONFIGURATION

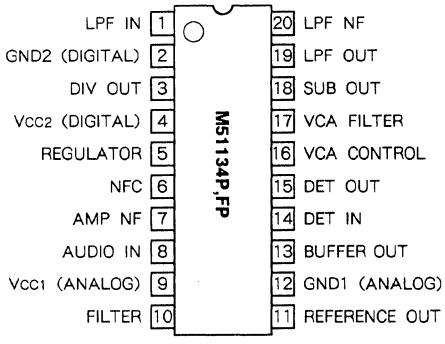


MITSUBISHI ELECTRIC

M51134P,FP

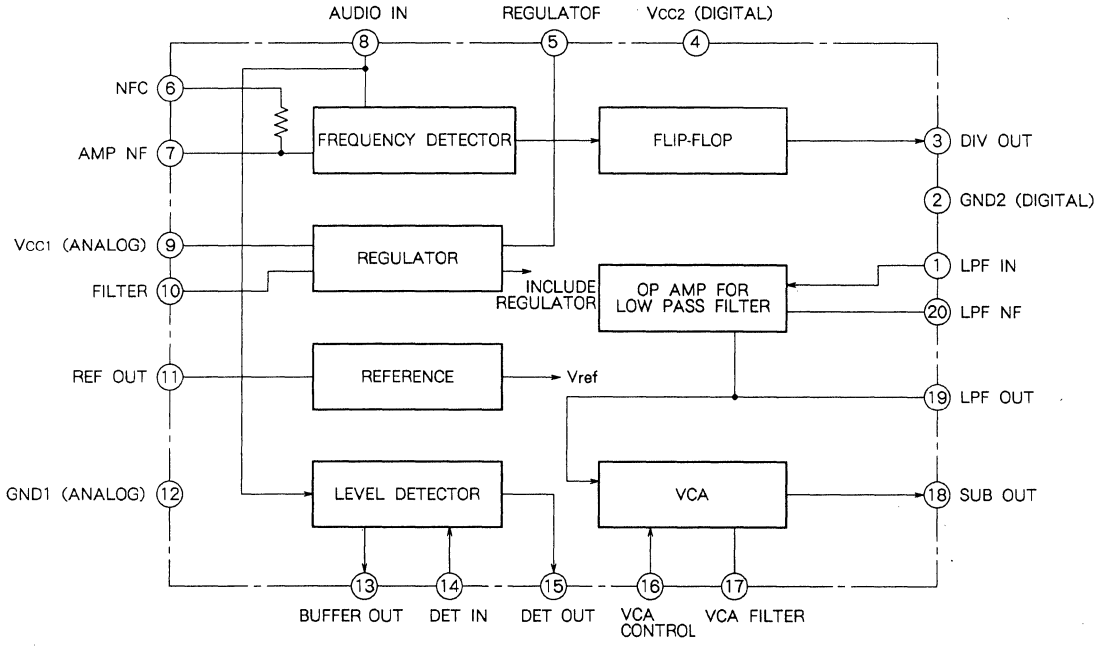
SUB-HORMONIZER FOR BASS EMPHASIS

PIN CONFIGURATION



Outline 20P4(P)
20P2N-A(FP)

IC INTERNAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC1}	Supply voltage (analog)	+ 16	V
V_{CC2}	Supply voltage (digital)	+ 5.5	V
P_d	Power dissipation	800(P)/500(FP)	mW
K_θ	Thermal derating	8.0(P)/5.0(FP)	mW/℃
T_{opr}	Operating temperature	−20∼+75	℃
T_{stg}	Storage temperature	−40∼+125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC1} = 12V, V_{CC2} = 5V, f = 100Hz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC1}	Quiescent circuit current	Quiescence	−	12	22	mA
I_{CC2}	Quiescent circuit current	Quiescence	−	0.95	2.5	mA
V_{imn}	Minimum detect input voltage		−	− 55	− 40	dBV
V_{ore}	Response output voltage range		35	47	−	dB
THD	Total harmonic distortion	V_i = − 10dBV	−	1.3	2.5	%
T_{rsp}	Response time		−	2.5	3.5	mS
V_{iMAX}	Maximum input voltage	THD = 2.0%	+ 4	+ 10	−	dBV
V_{OMAX}	Maximum output voltage	THD = 2.0%	1.8	2.5	−	Vrms
N_O	Output noise voltage	DIN AUDIO	−	− 93	− 83	dBV

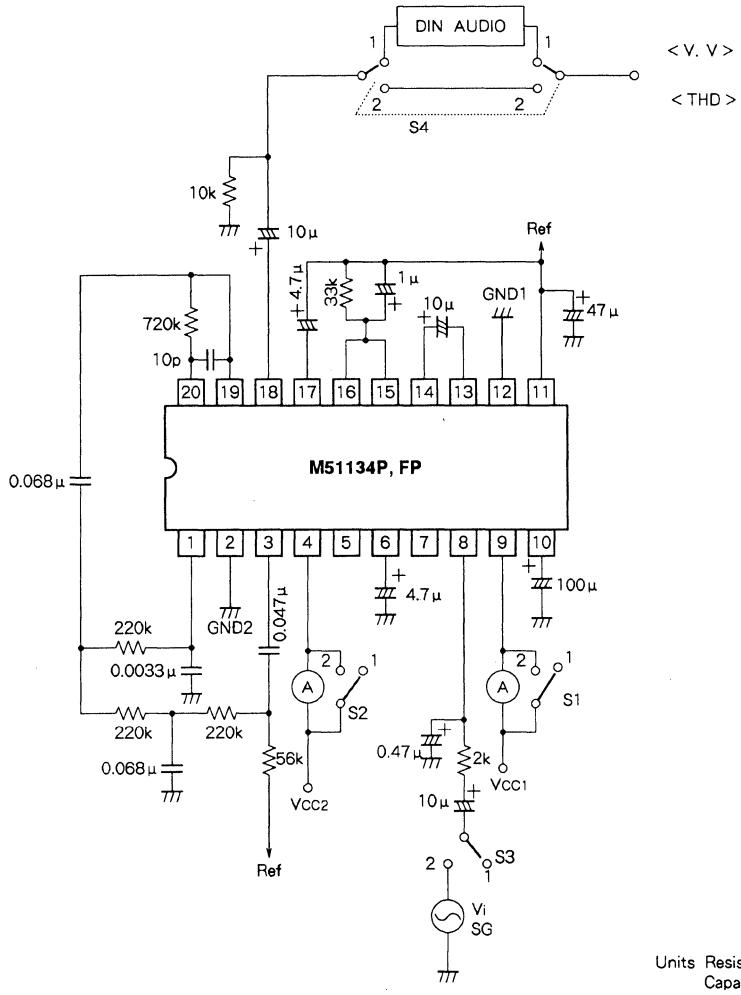
TEST METHOD

Symbol	SW1	SW2	SW3	SW4	Conditions
I_{CC1}	1	2	1	2	Measure circuit current at pin⑨ for quiescent state.
I_{CC2}	2	1	1	2	Measure circuit current at pin④ for quiescent state.
V_{imn}	2	2	2	2	Measure minimum input voltage at pin③ output.
V_{ore}	2	2	2	2	Measure difference in output voltage at V_{omax} and V_{imin}.
THD	2	2	2	2	Measure distortion with f = 100Hz, V_i = − 10dBV
T_{rsp}	2	2	2	2	Measure delay time between input signal and output signal.
V_{imax}	2	2	2	2	Measure output voltage with THD = 2%
V_{omax}	2	2	2	2	Measure input voltage with THD = 2%
N_O	2	2	2	1	DIN AUDIO

M51134P,FP

SUB-HORMONIZER FOR BASS EMPHASIS

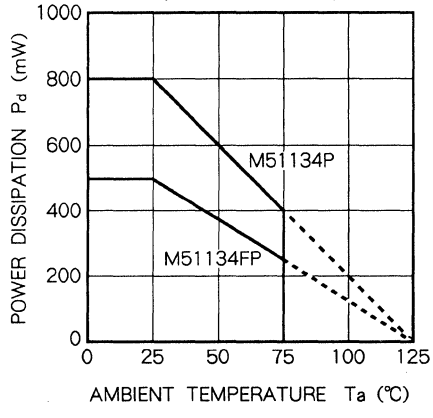
TEST CIRCUIT



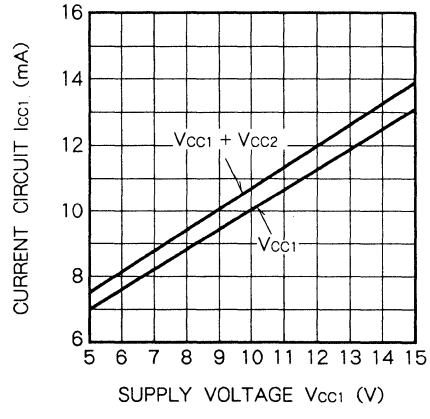
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

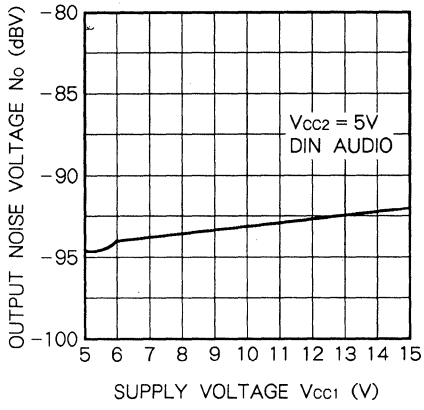
THERMAL DERATING (MAXIMUM RATING)



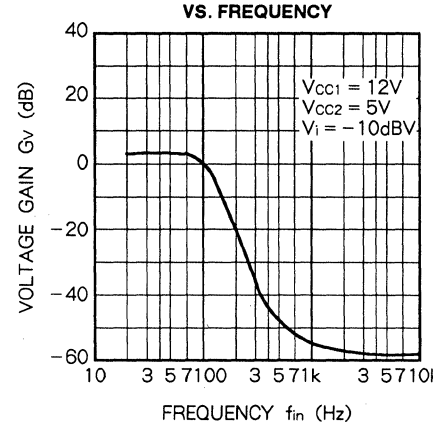
QUIESCENT CIRCUIT CURRENT VS. SUPPLY VOLTAGE



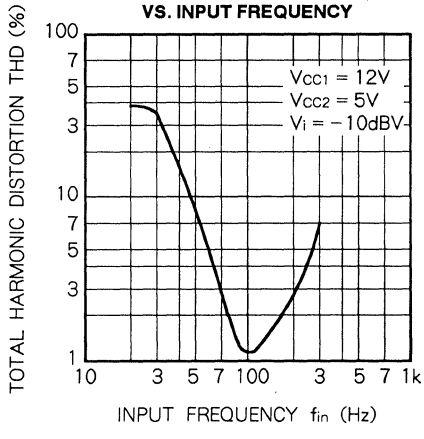
OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



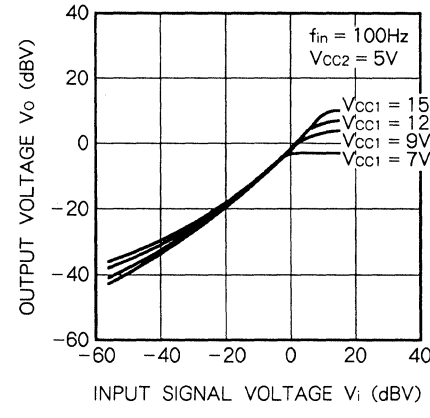
VOLTAGE GAIN VS. FREQUENCY



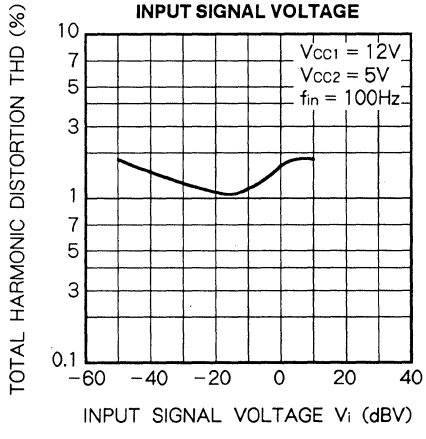
TOTAL HARMONIC DISTORTION VS. INPUT FREQUENCY



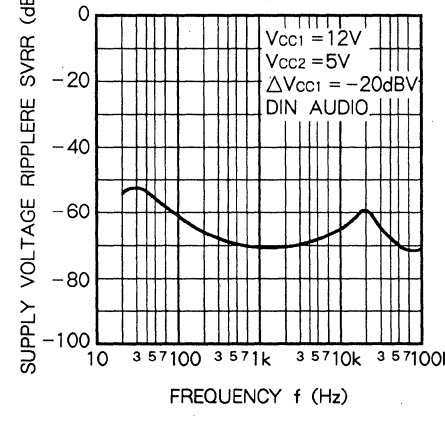
OUTPUT VOLTAGE VS. INPUT SIGNAL VOLTAGE



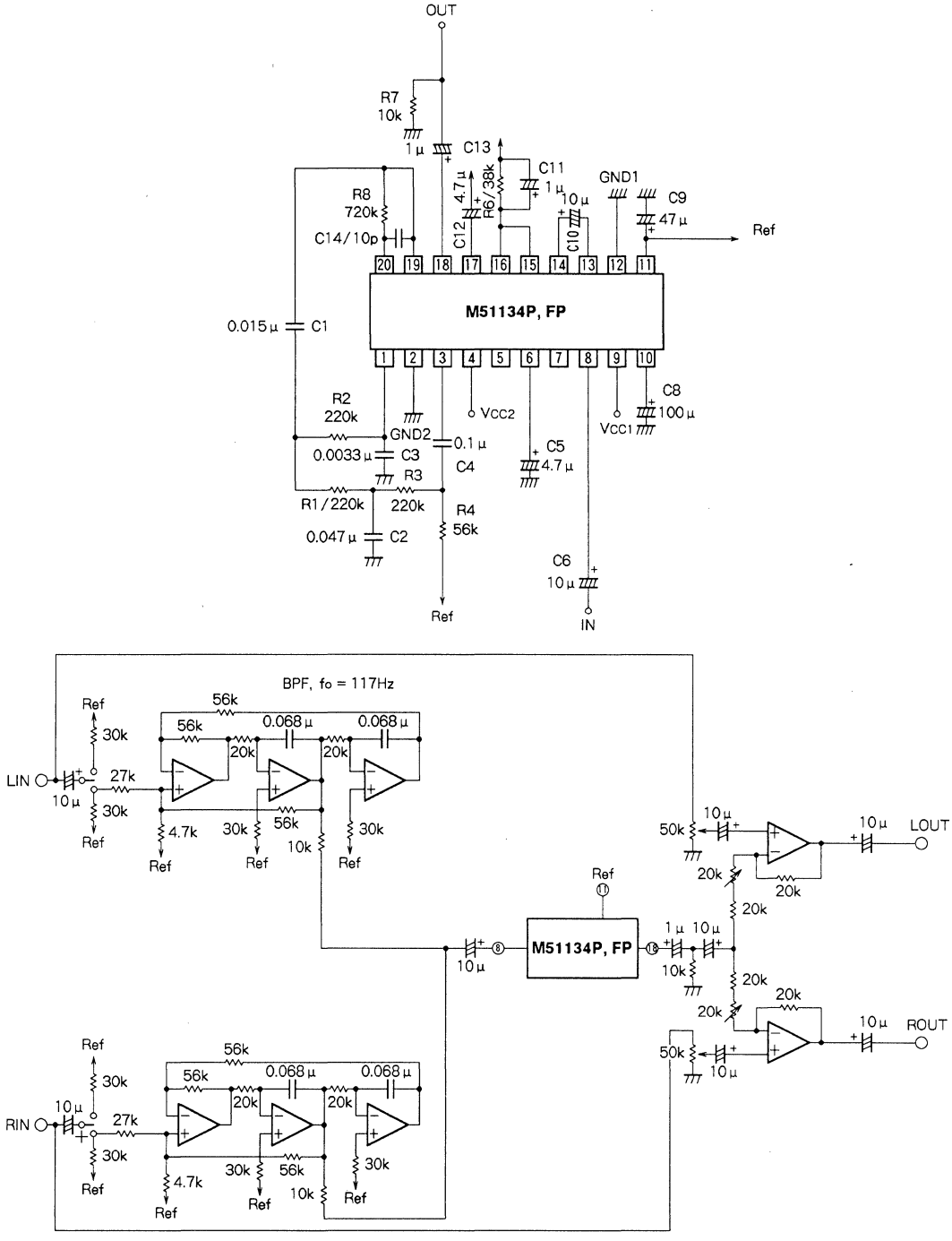
TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE



SUPPLY VOLTAGE REGULATIN RATIO VS. FREQUENCY



APPLICATION EXAMPLE



It's neccessary to chech input BPF and Built-in LPF cut off frequency at the system.

Units Resistance : Ω
Capasitance : F

M51523AL
DUAL ELECTRONIC VOLUME

DESCRIPTION

The M51523AL is an electronic volume control IC of dual channel configuration. The IC varies attenuation of the right and left channels and the balance between them. The M51523AL also has a built-in temperature-compensated reference voltage supply operating on a DC voltage, making the device useful as a control voltage souce.

FEATURES

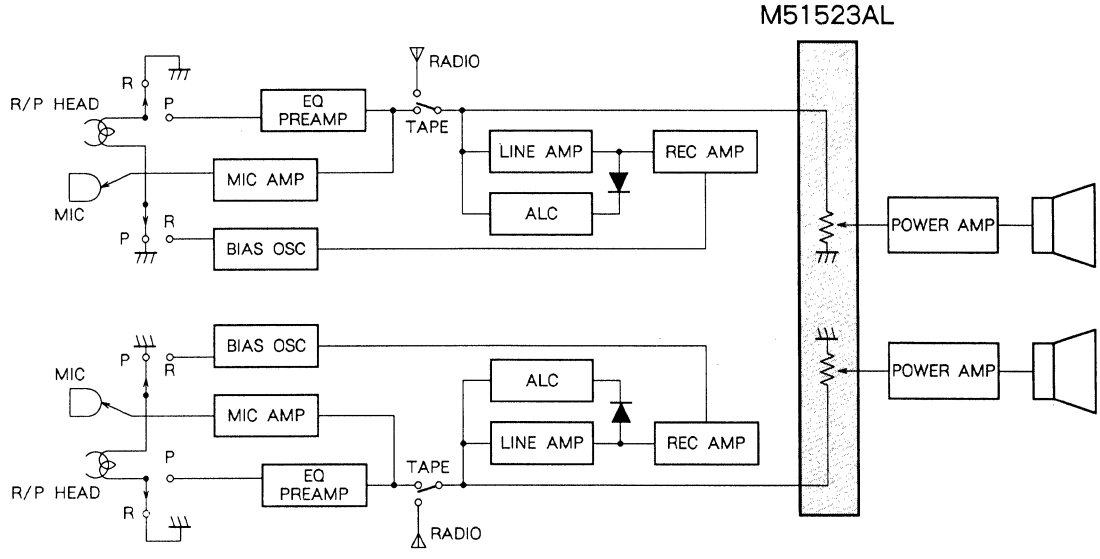
- High attenuation ..... 92dB (typ)
  (f = 1kHz, V_i = 150mV, IHF-A network)
- Low distortion ratio ..... 0.015% (typ)
  (f = 1kHz, V_i = 150mV, at maximum volume)
- Low noise ..... 3.6 μVrms (typ)
  (IHF-A network at minimum volume)
- Built-in stabilized power supply circuit makes device strong to fluctuations in supply voltage.
- Good temperature characteristics.
- Built-in balance circuit

Outline 14P5A
1.27mm pitch 325mil ZIP
(2.8mm × 19.0mm × 6.3mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 8~16V
Rated supply voltage 12V

SYSTEM CONFIGURATION

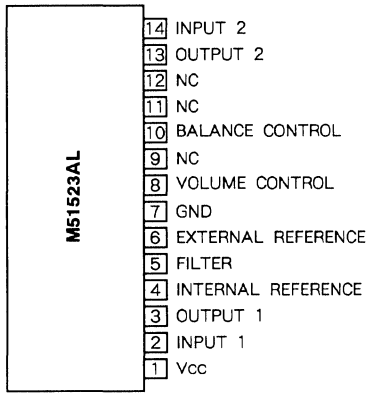


MITSUBISHI ELECTRIC

M51523AL

DUAL ELECTRONIC VOLUME

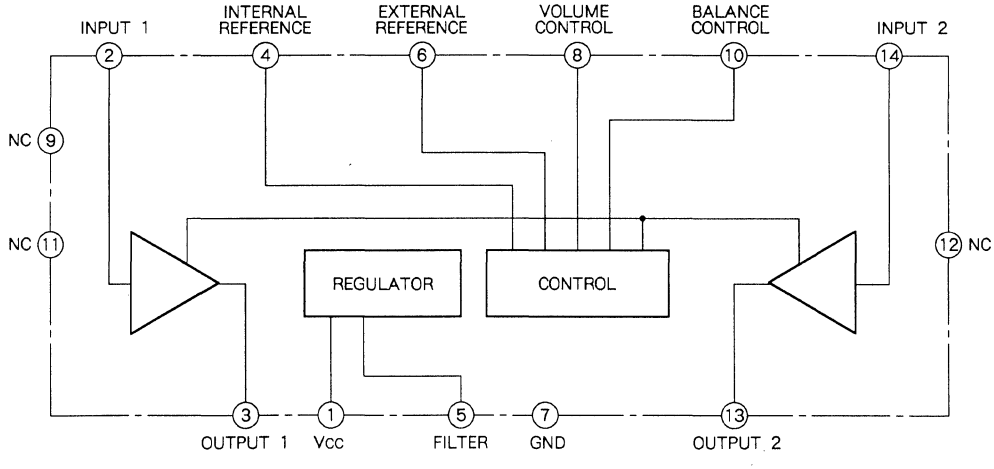
PIN CONFIGURATION



Outline 14P5A

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



M51523AL

DUAL ELECTRONIC VOLUME

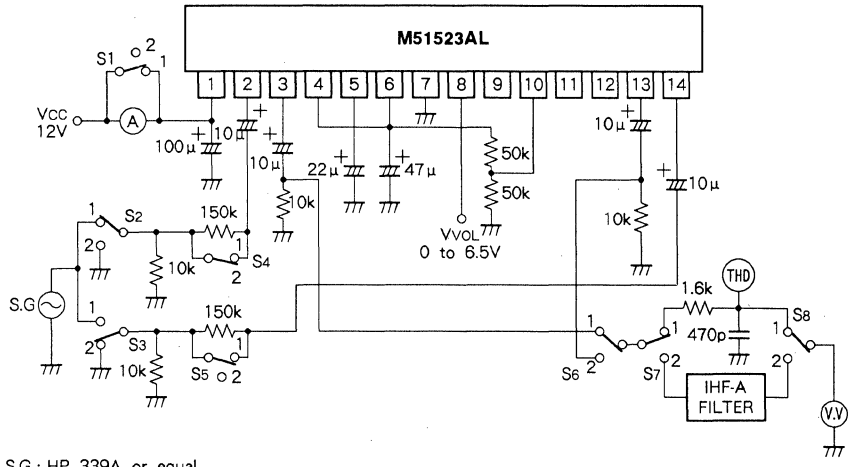
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Paramater	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Quiescent	18	V
I_{CC}	Circuit current		30	mA
P_d	Power dissipation		550	mW
K_θ	Thermal derating	$T_a \geqq 25$℃	5.5	mW/℃
T_{opr}	Operating temperature		−20～+75	℃
T_{stg}	Storage temperature		−40～+125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 12V, f = 1kHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CCO}	Quiescent circuit current	V_{VOL} = 0V, V_i = 0	7	12	20	mA
ATT	Attenuation level	V_{VOL} = 0V, V_i = 150mVrms IHF-A network	83	92	–	dB
C.B	Channel balance	V_{VOL} = 2.8V, V_i = 1Vrms	−3	0	3	dB
THD	Total harmonic distortion	V_{VOL} = 6.5V, V_i = 150mVrms	–	0.015	0.1	%
R_i	Input resistance	V_{VOL} = 6.5V, V_i = 1Vrms	50	150	–	kΩ
$V_{i(max)}$	Maximum input voltage	THD = 1%	1.0	1.5	–	Vrms
N_O	Output noise voltage	V_i = 0, IHF-A network	–	3.6	10	μVrms
$N_{O(r)}$	Residual output noise voltage	V_i = 150mVrms, IHF-A network	–	3.6	10	μVrms

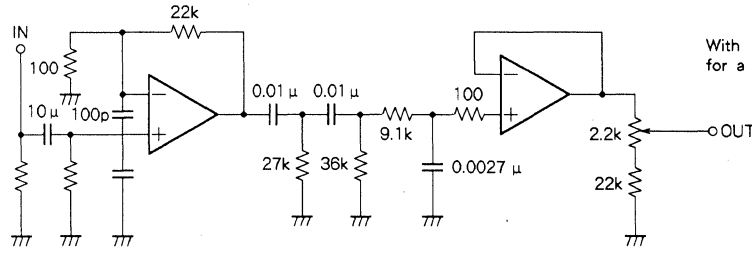
TEST CIRCUIT



Note 1. S.G : HP 339A or equal
THD : HP 339A or equal
V.V : Kikusui Model 1635 or equal
2. A low noise power supply (V_{CC},V_{EE}) should be used(< 2μV).

Units Resistance : Ω
Capacitance : F

● When the specified IHF-A filter is not used, see the following circuit for correct modifications.
Note that output is increased by a factor of 100X.



With 1kHz at input, adjust for a gain at output of 40dB.

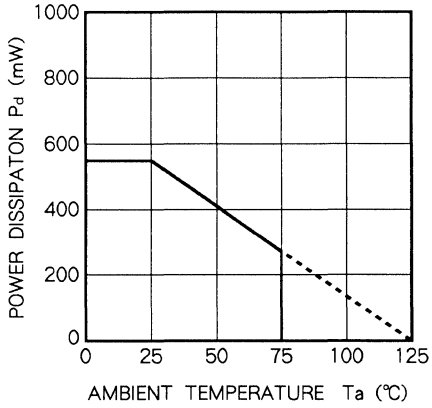
MITSUBISHI ELECTRIC

TEST METHODS (Ta = 25℃, V_{CC} = 12V, f = 1kHz, unless otherwise noted)

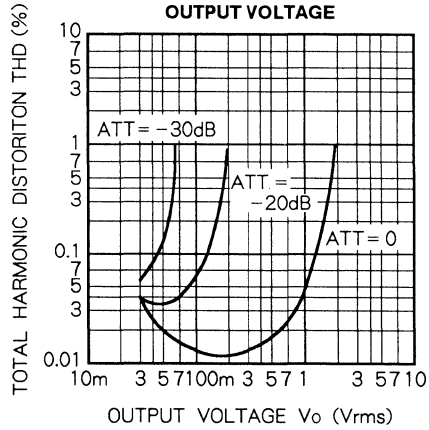
Symbol	Switch codition								Method
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	
I_{CCO}	2	2	2	1	1	–	1	1	Measure with ammeter.
ATT	1	1	1	1	1	1 2	1	1	Varying V_{VOL} from 0 to 6.5V, calculate using ATT = 20 log(V_O/V_i)(dB)
C.B	1	1	1	1	1	1 2	1	1	Channel balance at 2.8V volume level
THD	1	1	1	1	1	1 2	1	1	At f = 1kHz, V_O = 1Vrms, and maximum volume, measure with distortion meter.
R_i	1	1	1	1→2 1	1 1→2	1 2	1	1	Measure output when S_4 = 1 as V_{O1}, when S_4 = 2 as V_{O2} calculate using R_i = 150/(V_{O1}/V_{O2} − 1)(kΩ)
$V_{i(max)}$	1	1	1	1	1	1 2	1	1	At f = 1kHz, the input voltage when the output distortion rateis 1% at maximum volume.
N_O	1	2	2	1	1	1 2	2	2	Minimum volume level, R_g = 10kΩ, IHF-A filter
$N_{O(r)}$	1	1	1	1	1	1 2	2	2	Minimum volume level, R_g = 10kΩ, IHF-A filter

TYPICAL CHARACTERISTICS

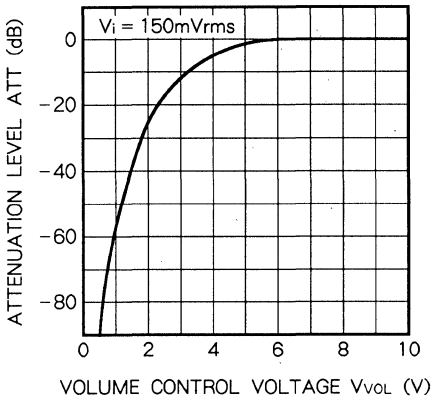
THERMAL DERATING (MAXIMUM RATING)



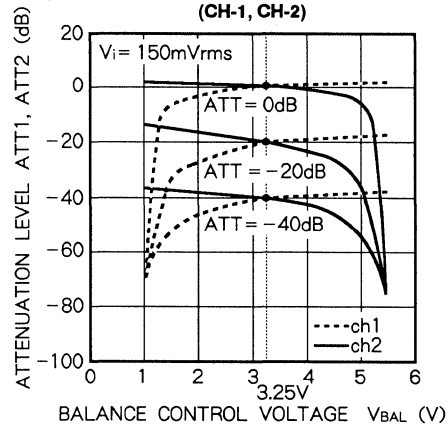
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



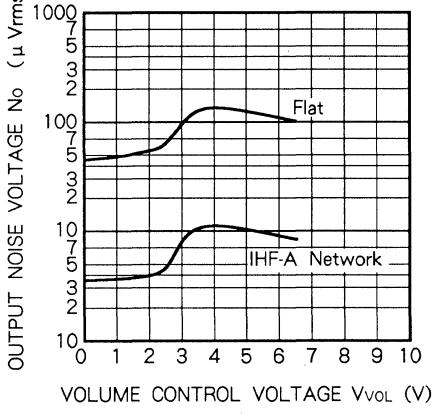
ATTENUATION LEVEL VS. VOLUME CONTROL VOLTAGE



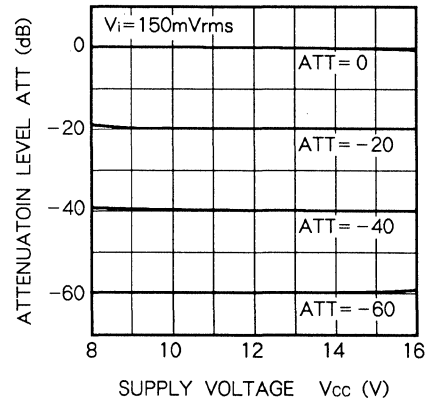
ATTENUATION LEVEL VS. BALANCE CONTROL VOLTAGE (CH-1, CH-2)



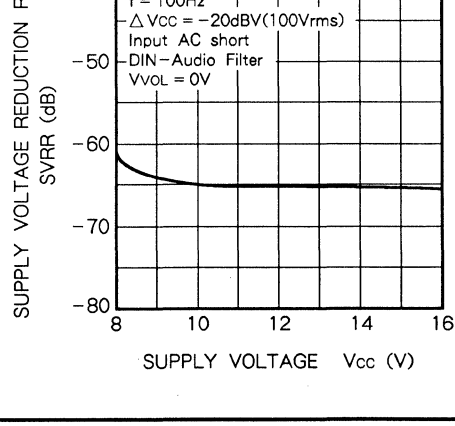
OUTPUT NOISE VOLTAGE VS. VOLUME CONTROL VOLTAGE



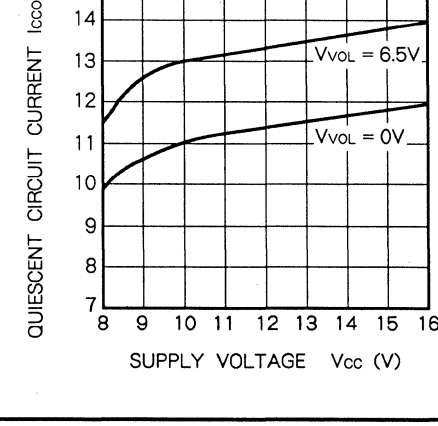
ATTENUATION LEVEL VS. SUPPLY VOLTAGE



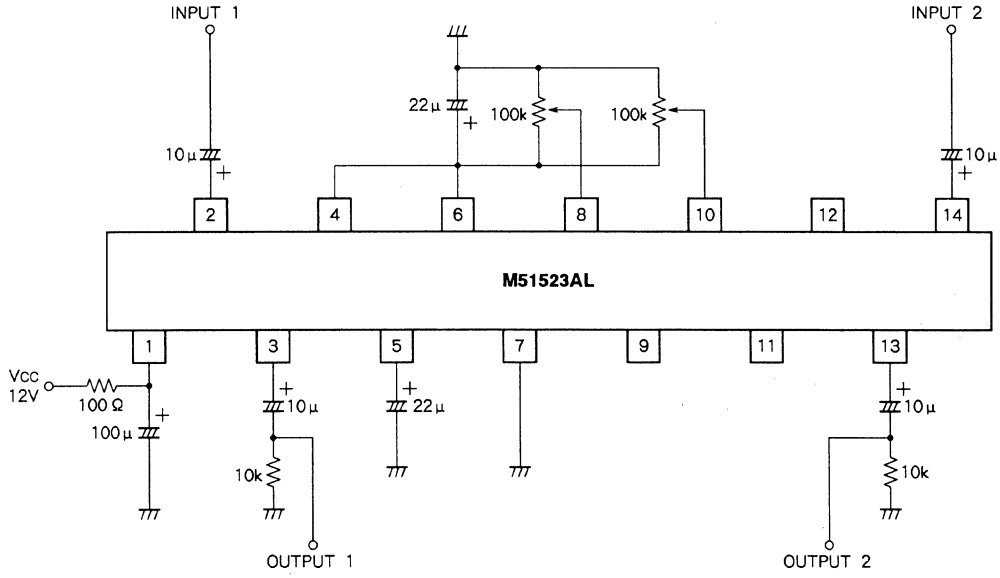
SUPPLY VOLTAGE REDUCTION RATIO VS. SUPPLY VOLTAGE



QUIESCENT CIRCUIT CURRENT VS. SUPPLY VOLTAGE



APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

M5206P

LINEAR CONTROL DUAL VCA IC

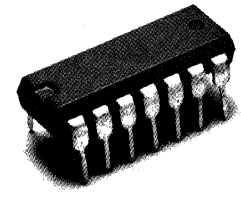
DESCRIPTION

The M5206P has 2 channels of built-in linear controlled VCA (Voltage controlled amplifier). These channels can be controlled independently.

The ICs applications include radio cassette tape recorders, car audio systems, and Hi-Fi VCR.

FEATURES

- Contains 2 channels of VCAs and each of them has an built-in control pin.
- Linear control type VCA (attenuates proportionally to the control voltage with excellent linearity) ····· V_C = 5Vmax
- Large maximum input voltage ····· V_i = 8Vrms(THD = 1 %)
- Large ATT range ····· ATT = 0 ~ − 100dB
- Single power source and double-power source are both available COM terminal ($V_{CC}/2$ terminals are incorporated).
- High pressure proof ····· V_{CC} = ± 18V(36V)
- LOG control pin built-in as is with M5222 and M5241.



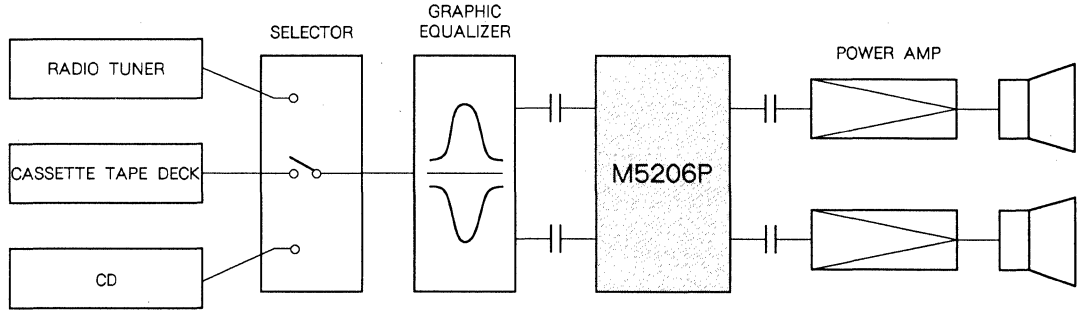
Outline 14P4

2.54mm pitch 300mil DIP
(6.3mm × 19.0mm × 3.3mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC}, V_{EE} = ± 7 ~ ± 16V
Rated supply voltage ····· V_{CC}, V_{EE} = ± 15V
Linear control voltage range ····· LINE V_C = 0 ~ 5V
Log control voltage range ····· LOG V_C = 0V ~ 350mV

SYSTEM CONFIGURATION

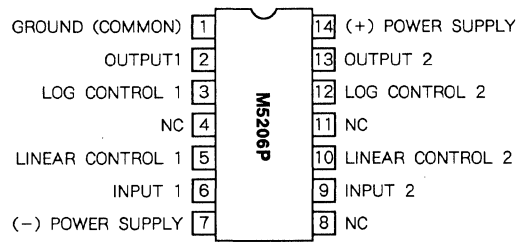


MITSUBISHI ELECTRIC

M5206P

LINEAR CONTROL DUAL VCA IC

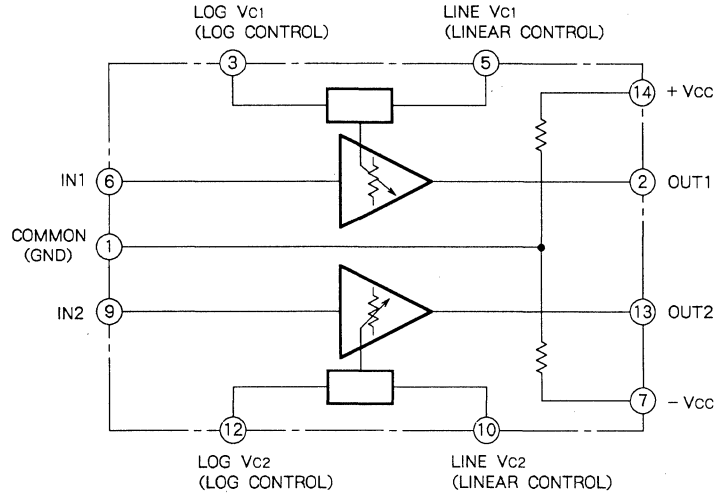
PIN CONFIGURATION



Outline 14P4

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Name	Symbol	Function
①	COM (GND)	COM (GND)	Vcc/2 is produced inside of the IC by resistive potential dividing and is supplied to pin①. Connect to GND when used by double-power sources. Use it as a midpoint potential pin when used by the single power source.
②	Ch1 output	OUT1	This is an output pin on ch1 side. Input signals from ch1 input pin is output to this pin as current signals.
③	Ch1 LOG control	Log V_{C1}	This is a Log control pin on ch1 side. Applying voltage (0V~350mV) between this pin and the COM pin will change the output logarithmically. About 100 nA of bias current is required.
④	Not connected	NC	This pin is not connected.
⑤	Ch1 linear control	LINE V_{C1}	This is a linear control pin on ch1 side. Applying DC voltage (0V~5V) between this pin and the COM pin will change the output linearly. About 100 nA of bias current is required.
⑥	Ch1 input	IN1	This is an input pin on ch1 side. Input is converted into current signals by input resistor R_1 to be input to this pin.
⑦	(−) power	− Vcc	This is a power pin on minus side. This has the lowest potential in this IC.
⑧	Not connected	NC	This is the power pin on plus side.
⑨	Ch2 input	IN2	This is an input pin on ch2 side. Input is converted into current signals by input resistor R_1 to be input to this pin.
⑩	Ch2 linear control	LINE V_{C2}	This is a linear control pin on ch2 side. Applying DC voltage (0V~5V) between this pin and the COM pin will change the output linearly. About 100 nA of bias current is required.
⑪	Not connected	NC	This pin is not connected
⑫	Ch2 LOG control	Log V_{C2}	This is a Log control pin on ch2 side. Applying voltage (0V~350mV) between this pin and the COM pin will change the output logarithmically. About 100 nA of bias current is required.
⑬	Ch2 output	OUT2	This is an output pin on ch2 side. Input signals from ch2 input pin is output to this pin as current signals.
⑭	(+) supply voltage	+ Vcc	This is the power pin on plus side.

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

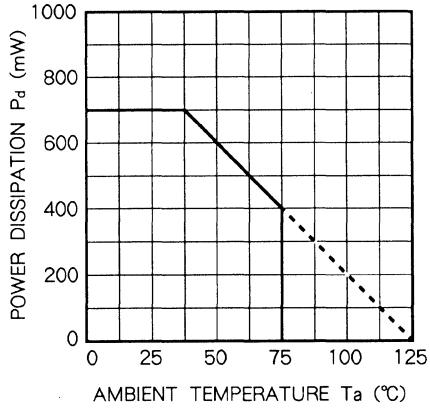
Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	± 18 (36)	V
P_d	Power dissipation	700	mW
K_θ	Thermal derating	7	mW/℃
T_{opr}	Operating temperature	− 20~ + 75	℃
T_{stg}	Storage temperature	− 55~ + 125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, Vcc = ± 15V, Vc (LINE) = 5V, Vc (LOG) = 0V, unless otherwise noted)

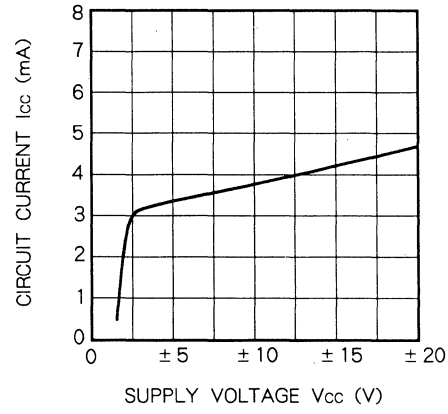
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Icc	Circuit current	Vi = 0V	–	4.3	7.5	mA
VIM	Maximum input voltage	f = 1kHz, THD = 1 %	5.6	8.0	–	Vrms
Ioo	Output offset current	Vi = 0V	–	± 0.3	± 2.0	μ A
Δ ATT1	Attenuation error	f = 1kHz, Vi = + 10dBm	– 1.0	0.5	2.0	dB
Δ ATT2	Attenuation deviation between channels	f = 1kHz, Vi = + 10dBm	–	± 0.3	± 2.0	dB
ATT1	Logarithm maximum attenuation	f = 1kHz, Vi = + 10dBm, Vc (LOG) = 350mV	–	– 100	– 85	dB
ATT2	Linear maximum attenuation	f = 1kHz, Vi = + 10dBm, Vc (LINE) = 0V	–	– 100	– 85	dB
THD	Total harmonic distortion	f = 1kHz, Vo = 1Vrms	–	0.15	1.0	%
CS	Channel separation	f = 1kHz, BW : 10Hz~30kHz	–	70	–	dB
HR	Hum rejection	f = 120Hz	–	57	–	dB
VNo	Output noise voltage	Vi = 0V, BW : 10Hz~30kHz	–	60	120	μ Vrms

TYPICAL CHARACTERISTICS

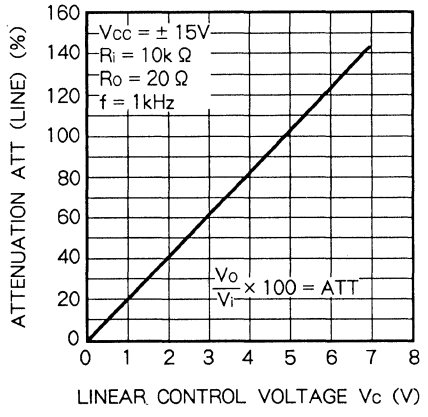
THERMAL DERATING (MAXIMUM RATING)



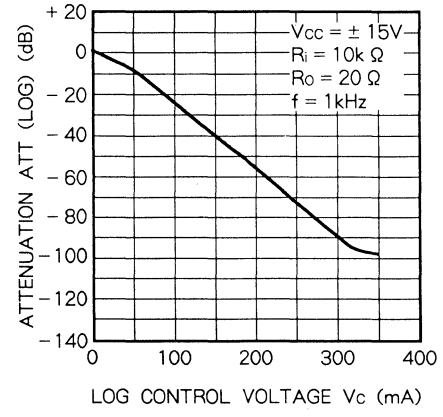
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



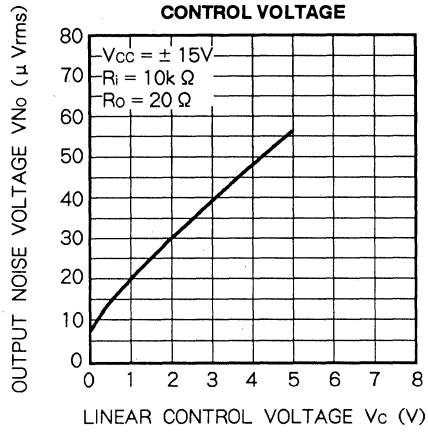
ATTENUATION VS. CONTROL VOLTAGE



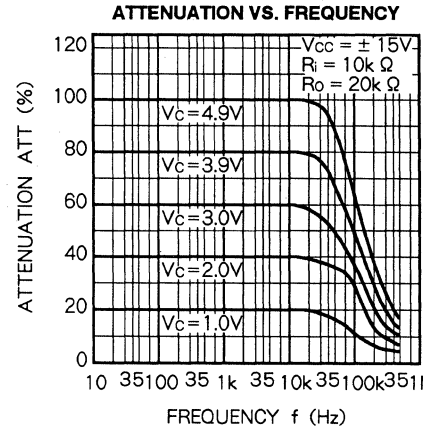
ATTENUATION VS. CONTROL VOLTAGE



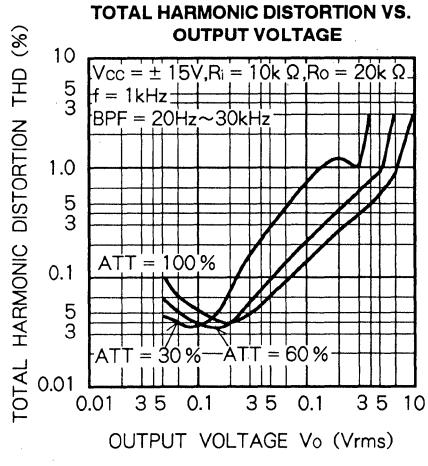
OUTPUT NOISE VOLTAGE VS. CONTROL VOLTAGE



ATTENUATION VS. FREQUENCY

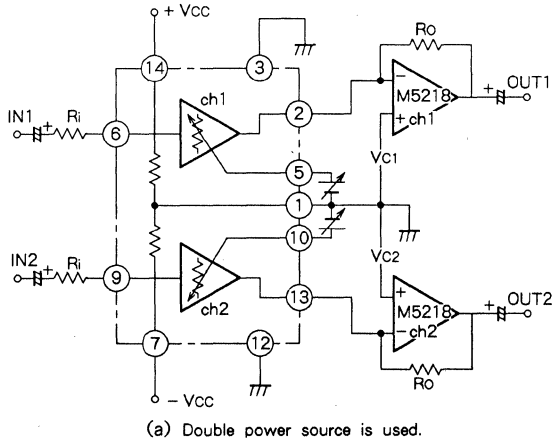


TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE

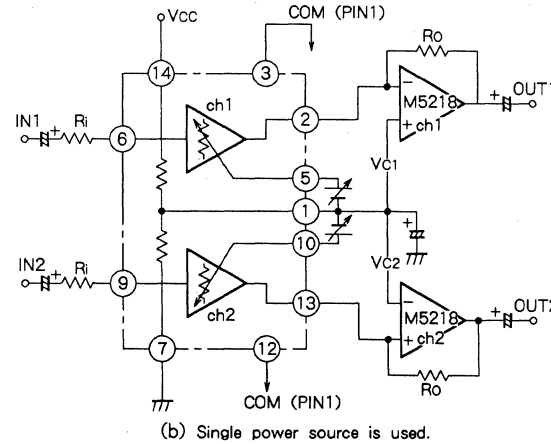


APPLICATION EXAMPLE

Standard application example

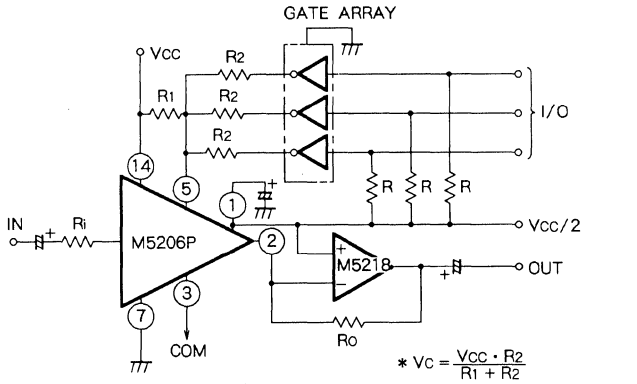


(a) Double power source is used.



(b) Single power source is used.

MITSUBISHI ELECTRIC

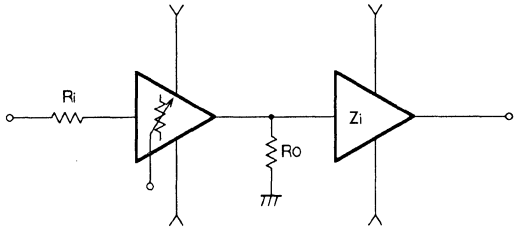


$* V_C = \frac{V_{CC} \cdot R_2}{R_1 + R_2}$

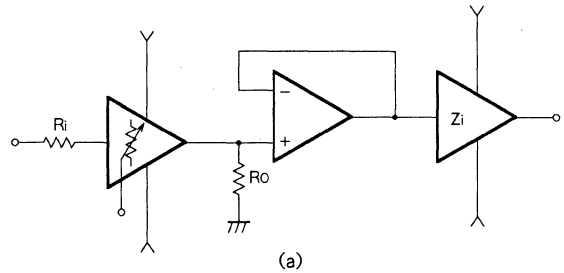
* R IS A PULL-UP RESISTOR

NOTES

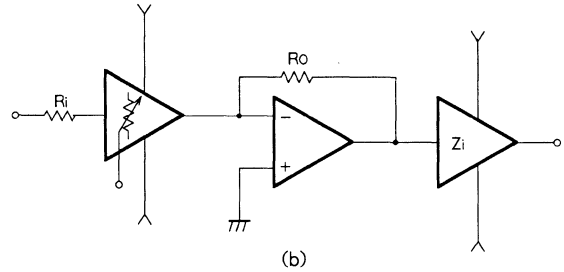
1. Selecting $R_O = 2R_i$ will valance the internal differential circuit (when $V_{C\ LINE} = 5V$ and $V_{C\ LOG} = 0V$), providing 0dB of one time amplifier.
2. Output circuit is a float output type based on collector connections of transistors PNP and NPN, and it is requred to set the potential at one end of external resistor R_O. (See the "Mechanism of I/O Voltage and Current Conversion" section.)
3. M5206P uses amplifiers of class A and class B for the "voltage ↔ current" conversion. Unlike M5222 and M5241, the maximum input current value is not determined by its limit value, however, there exists a maximum value because of the saturation of output transistor. Therefore, to input large signals select larger input/output resistances and decrease the input current.
   Since using larger resistance will increase the noise, select some proper resistance value according to the use of the IC.
4. The voltage gain is determined by V_C, R_i, and R_O so that it may be affected by the value of input impedance connected to the next. (Z_i is inserted in parallel with R_O to decrease the impedance.) (See following figure)



Generally, a buffer amplifier of transistor or operational amplifier is connected. (See following figures (a),(b))



(a)

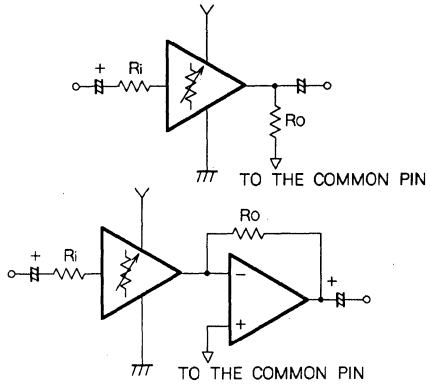


(b)

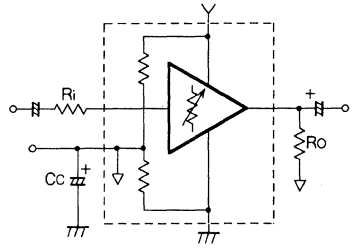
Note the following differences. In the circuit in Figure (a), its input signal has the antiphase, the potential of the output pin may be changed by the signals, and the maximum output voltage is also affected by the residual voltage in the output circuit. (About 1V of residual voltage will be generated form the + Vcc as well as the − Vcc.) In the circuit in Figure (b), any input signal has the equal phase, the potential of the output pin is fixed, and the residual voltage in the output circuit does not have any influence.

5. Cautions when using the single power supply :

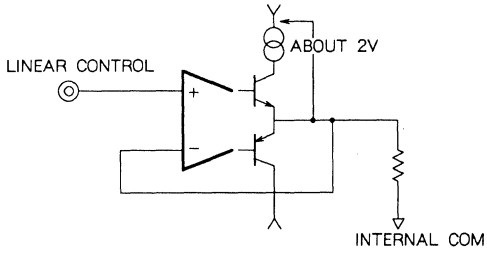
- Set the one end voltage of the Ro to COMMON potential.



- Connect a capacitor Cc between the COMMON pin and the Ground to decrease the impedance of the COM pin.

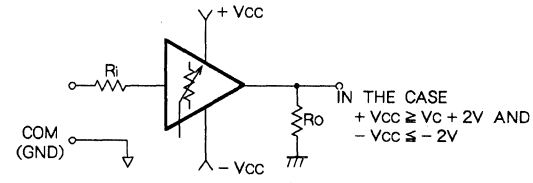


6. The range of supply voltage is widely affected by the range of the control voltage. A stage of current mirror circuit is connected to the output push-pull circuit of the control circuit to that at least 2V of residual voltage from the Vcc is needed (Vcc ≧ Vc + 2V). At least 2V is needed for the − Vcc operation.

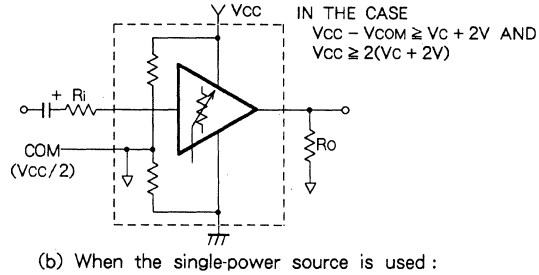


This IC contains a midpoint voltage generator. If the single power source is used, set (Vcc − Vcom) becomes larger than (Vc + 2V).(Vcom is usually Vcc/2V).

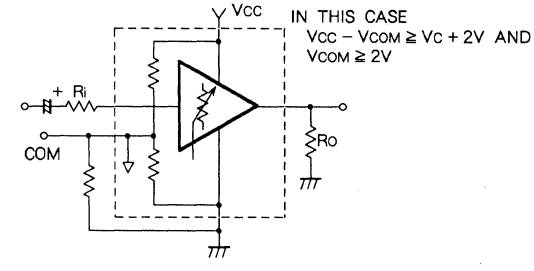
At least 2V of potential Vcom is needed between the ground and the COM pin for proper operation. To make the value of the Vcc small, use an external resistor for shifting the level of the Vcom.



(a) When the double-power source is used :



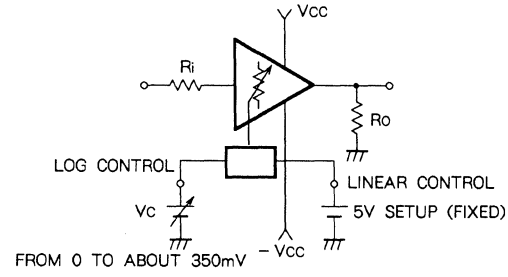
(b) When the single-power source is used : (without any change)



(c) When the single-power source is used (Vcom level is sifted) :

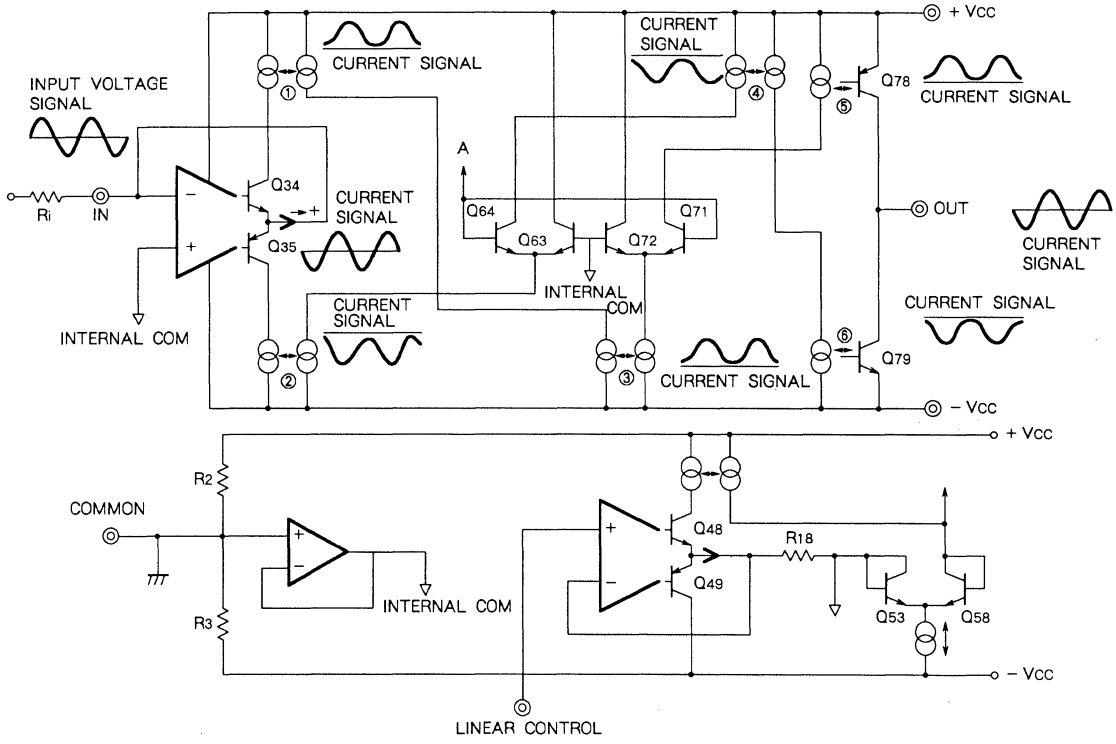
7. In case of using the LOG control of the M5206P, logarithmical attenuation, as that in M5222 and M5241, can be done because of the existence of the LOG control pin in this IC.

Following figure shows the connection of this case. The control of the attenuation is done by supplying the puls voltage Vc to the COMMON pin. Supply 5V to the linear control pin.(5V is the required condition for obtaining the 0dB of attenuation by the liner control voltage.)



8. To obtain the attenuation chracteristics using the linear control pin of M5206P, the LOG control pin should be shorted with the COM pin or it should be biased by the COM pin potential.

OPERATION CIRCUIT



BASIC OPERATION PRINCIPLES

M5206P is a VCA (Voltage Controlled Amplifier) IC which accepts and outputs electric current. This converts input signals to current signals using an external resistor and sends them to the current mirror output circuit through a differential circuit. These current signals are converted again to voltage signals by an external output resistor, therefore, it works as if a voltage I/O device. The attenuation is controlled by the control voltage Vc while changing the balance (changing the gm) in the differential circuit.

The following describes the basic operation of the IC.

1. Mechanism of I/O voltage and current conversions

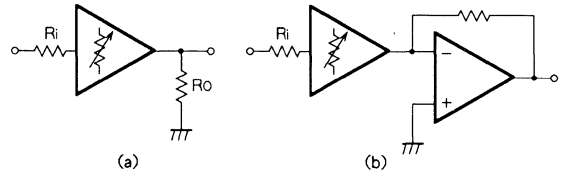
As shown in the block diagram, the input circuit is a voltage / current conversion circuit with operational amplifier configration. By connecting an external input resistor R_I, the input voltage V_i is supplied to the inside of the IC as the input current i_i ($= V_i/R_I$). (The phase will be reversed.)

The current sent is divided into half waves by the push-pull circuit (Q_{34} and Q_{35}) in the input operational amplifier and they are sent as the current signals to the output circuit by current mirrors ① to ⑥ and differential circuits (Q_{63}, Q_{64}, Q_{71}, and Q_{72}).

The output circuit forms a current composition circuit with the current mirror configuration. Resulting (composed) current signals can be obtained from the output pin.

These current signals can be obtained as output signals Vo using the external output resistor.

It is required to set some proper DC electric potential at one end of the output resistor because the output circuit has the float output type due to the collector connection of PNP and NPN transistors.



As shown in the above figure, there are two methods for the setup :

(1) Set the one end of the Ro pin to the equal potential to COM (GMD when the double-power source is used).

(2) Use a current/voltage conversion circuit based on an operational amplifier.

Note that obtained output signals in (a) have the antiphase to input signals and that in (b) have the equal phase to input signals.

2. Attenuation mechanism

The output control is done by supplying positive voltage to the Vc pin of the COM pin.

The gain of this circuit is changed by changing the current distribution for the differential circuit, which can be done by giving a fixed potential from the COM pin to one of the base (Q_{63}, Q_{72}) of the differential circuit and giving the control voltage Vc to another base (Q_{64}, Q_{71}) through the control circuit.

If the external control voltage is directly supplied to the base (Q_{64}, Q_{71}), the characteristics of the attenuation versus control voltage will change logarithmically as explained below, however, it will be changed to the linear caracteristics by inserting a control circuit.

This is one of the major features of the IC.

(1) Basic mechanism of the attenuation

Input signal V_i is converted to the current signal $i_i = (= V_i / R)$ by the input resistor R_i.

This signal is divided into half waves by push-pull circuits Q34 and Q35 and each half-wave is sent to the differential circuit by current mirrors ① to ③.

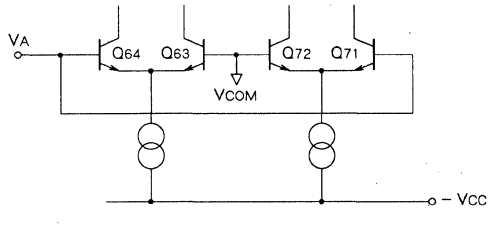
When the differential circuit is balanced (base potentials are equal), collector current in Q_{63} and Q_{64}, Q_{71} and Q_{72} become eual and the current sent by current mirrors ① to ③ is divided equally at this point. This current is sent to the output pin by current mirrors ④ to ⑥, half-waves are composed, and output current $i_i/2$ is obtained.

Here, select $R_O = 2R_i$ to get

$$V_O = i_i/2 \cdot R_O = i_i/2 \cdot 2R_i = i_i \cdot R_i = V_i$$

which means an amplifier with gain 1.

Let us observe the attenuation characteristics with this resistor selection where the COM potential is provided to the base for Q_{63} and Q_{72} and V_A to the base for Q_{64} and Q_{71}. The current signal having been divided into half waves by the push-pull circuit is shown as i_i+ and i_i-.($i_i = i_i+ + i_i-$)



Each value of V_{BE} in the differential stage is as follows :

$$V_{BE63} \fallingdotseq \frac{kt}{q} \ln\left(\frac{I_{C63}}{I_S}\right)$$

$$V_{BE64} \fallingdotseq \frac{kt}{q} \ln\left(\frac{I_{C64}}{I_S}\right)$$

$$V_{BE71} \fallingdotseq \frac{kt}{q} \ln\left(\frac{I_{C71}}{I_S}\right)$$

$$V_{BE72} \fallingdotseq \frac{kt}{q} \ln\left(\frac{I_{C72}}{I_S}\right)$$

k : Bolztman's constant
T : Absolute temperature
q : Electric charge
Is : Saturation current

The above equations result in the following :

$$\Delta V_{BE} = V_A - V_{COM}$$

$$= V_{BE64} - V_{BE63} = \frac{kt}{q} \ln\left(\frac{I_{C64}}{I_{C63}}\right)$$

$$= V_{BE71} - V_{BE72} = \frac{kt}{q} \ln\left(\frac{I_{C71}}{I_{C72}}\right)$$

Here, equations below are valid,

$I_{C63} + I_{C64} = I_i -$

$I_{C71} + I_{C72} = I_i +$

Therefore,

$$V_A - V_{COM} = \frac{kt}{q} \ln \frac{I_{C64}}{i_i - I_{C64}}$$

$$V_A - V_{COM} = \frac{kt}{q} \ln \frac{I_{C71}}{i_i - I_{C71}}$$

When the double-power source is used, $V_{COM} = 0V$.

For simplicity, it is noted as $V_{COM} = 0$.

As a result, the following equations are obtained :

$$I_{C64} = i_i - \cdot \frac{\exp(\frac{q}{kt} \cdot V_A)}{1 + \exp(-\frac{q}{kt} \cdot V_A)}$$

$$= i_i - \cdot \frac{1}{1 + \exp(-\frac{q}{kt} \cdot V_A)}$$

$$I_{C71} = i_i + \cdot \frac{1}{1 + \exp(-\frac{q}{kt} \cdot V_A)}$$

Thus, the current shown in the following equation flows into the output pin :

$$i_o = I_{C78} + I_{C79}$$

$$= I_{C64} + I_{C71} = \frac{i_i}{1 + \exp(-\frac{q}{kt} \cdot V_A)}$$

Its again will be as follows :

$$\frac{V_O}{V_i} = \frac{i_o \cdot R_O}{I_i \cdot R_i} = \frac{i_o \cdot 2R_i}{I_i \cdot R_i}$$

$$= \frac{2}{1 + \exp(-\frac{q}{kt} \cdot V_A)}$$

Now, convert this into dB :

$$ATT = 20 \log \left(\frac{2}{1 + \exp(-\frac{q}{kt} \cdot V_A)} \right)$$

and when $V_A = 0$, ATT = 0dB.

Also, when $1 \ll \exp\left(-\frac{q}{kt} \cdot V_A\right)$

$$ATT \fallingdotseq -\frac{20}{\ln 10} \cdot \left(-\frac{q}{kt} \cdot V_A\right) + 20 \log 2$$

showing the attenuation changes logarithmically for the Vc change.

(2) Linear control mechanism

As explained above, the attenuation changes logarithmically for the potential difference of base in the differential circuit. However, by supplying control voltage through the linear control circuit, the attenuation fot the control voltage can change linearly.

The control circuit consists of an operational amplifier, current mirrors, and differential circuits, as indicated in the block diagram.

As first, supplied control voltage Vc is converted into the control current Ic by R_{18}.

$$I_C = \frac{V_C}{R_{18}}$$

Differential circuits Q_{53} and Q_{58} are biased by the constant current I and when

$$I_{C53} = I_{C58} = \frac{1}{2}$$

the differential circuits are balanced. (When Vc = 5V)

That is the potential V_A at the point A will be equal to that of V_{COM}.

$$V_A = V_{COM} - V_{BE53} + V_{BE58} = V_{COM}$$

Remembering of the previous section, the attenuation becomes 1dB or one time of gain. Suppose the control voltage Vc is supplied to the linear control pin.

Each value for V_{BE} will be as follows :

$$V_{BE53} \fallingdotseq \frac{kt}{q} \ln \frac{I_{C53}}{I_S}$$

$$V_{BE58} \fallingdotseq \frac{kt}{q} \ln \frac{I_{C58}}{I_S}$$

$$V_A - V_{COM} = V_{BE58} - V_{BE53}$$

$$= \frac{kt}{q} \ln \frac{I_{C58}}{I_{C53}}$$

When the double-power source is used, $V_{COM} = 0$.
For simplicity, it is noted as $V_{COM} = 0$.

$$V_A = \frac{kt}{q} \ln \frac{I_{C58}}{I_{C53}}$$

Since I_{C53} and I_{C58} are as follows,

$$I_{C53} = I_C = \frac{V_C}{R_{18}}$$

$$I_{C58} = I - I_{53} = I - \frac{V_C}{R_{18}}$$

and

$$V_A = \frac{kt}{q} \ln \frac{I - \frac{V_C}{R_{18}}}{\frac{V_C}{R_{18}}}$$ is obtained.

If the substitutes the equation for the gain obtained before, the following equation is given :

$$\frac{V_O}{V_i} = \frac{2}{1 + \exp\left(-\frac{q}{kt} \cdot V_A\right)}$$

$$= \frac{2}{1 + \exp\left(-\frac{q}{kt} \cdot \frac{kt}{q} \ln \frac{I - (V_C / R_{18})}{V_C / R_{18}}\right)}$$

$$= \frac{2}{I \cdot R_{18}} \cdot V_C$$

Thus , you may have an excellent temperature characteristics as well as the attenuation which is proportional to the Vc change.

This control circuit also as has the compensation function when the amount of attenuation is not enough (i. e. the gain does not become 0 when Vc = 0) due to the offset voltage of differential circuits.

M5207L01/M5207L05
LINEAR CONTROL DUAL VCA IC

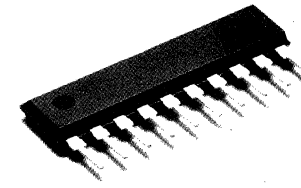
DESCRIPTION

The M5207L is a variable gm-type VCA (Voltage Control Amplifier) IC designed for linear controlled electronic volume control. The IC offers capability of controlling each channel independently.

Its applications include radio cassette tape recorders, car audio systems, and Hi-Fi VCR.

FEATURES

- 2 channels of VCA with independent control terminal are built-in.
- Linear control type VCA (attenuates proportionally to the control voltage with excellent linearity).
  ····· M5207L01 ; V_C = 1Vmax
  M5207L05 ; V_C = 5Vmax
- High maximum input voltage····· V_i = 8Vrms(THD = 1 %)
- ATT range is large····· ATT = 0 ~ – 100dB
- Single power source and two power source are both available COM terminal ($V_{CC/2}$ terminals are built-in).
- High pressure proof····· V_{CC} = ± 18V (36V)
- M5207L01·····Output is set to 100% (0dB) for the input when the control voltage is 1V.
- M5207L05·····Output is set to 100% (0dB) for the input when the control voltage is 5V.



Outline 10P5

2.54mm pitch 340mil SIP
(2.8mm × 25.23mm × 6.3mm)

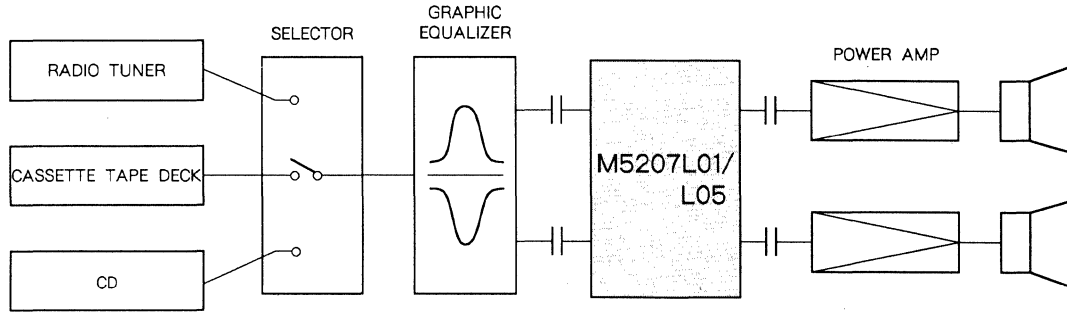
RECOMMENDED OPERATING CONDITIONS (M5207L01/M5207L05)

Supply voltage range····· V_{CC}, V_{EE} = ± 7 ~ ± 16V
or V_{CC} = 4 ~ 32V

Rated supply voltage····· V_{CC}, V_{EE} = ± 15V or V_{CC} = 9V

Range of linear control voltage···· V_{CC} = 0 ~ 1V, V_{EE} = 0 ~ 5V

SYSTEM CONFIGURATION

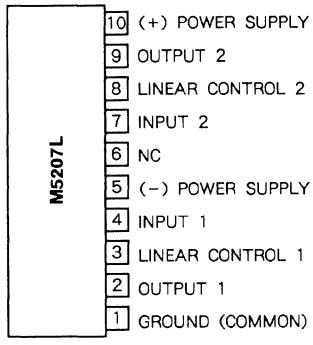


MITSUBISHI ELECTRIC

M5207L01/M5207L05

LINEAR CONTROL DUAL VCA IC

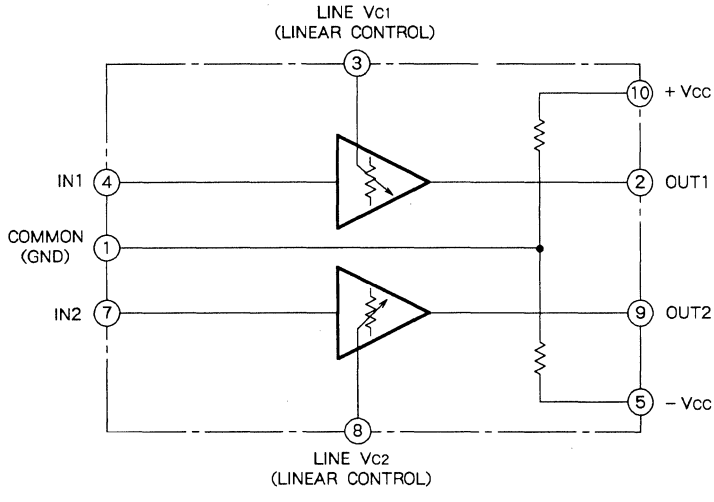
PIN CONFIGURATION



Outline 10P5

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Name	Symbol	Function
①	COM terminal (GND)	COM (GND)	Vcc/2 is produced inside IC by resistive potential dividing and is output to terminal 1. Connect to GND when used by two power sources. Use it as a midpoint potential when used by single power source.
②	ch1 output	OUT1	This is an output terminal on ch1 side. Signal input from ch1 input terminal is output to this terminal as a current signal.
③	ch1 linear control	LINE V_{C1}	This is a linear control terminal on ch1 side. Output changes linearly by providing DC voltage of 0V~1V (M5207L01) or 0V~5V (M5207L05) between this terminal and COM terminal.
④	ch1 input	IN1	This is an input terminal on ch1 side. Input is converted into current signal by input resistor R to be input to this terminal.
⑤	(−) power	$-V_{CC}$	This is a power terminal on minus side. This has the lowest potential in this IC.
⑥	Not connected	NC	This terminal is kept OPEN.
⑦	ch2 input	IN2	This is an input terminal on ch2 side. Input is converted into current signal by input resistor R to be input to this terminal.
⑧	ch2 linear control	LINE V_{C2}	This is a linear control terminal on ch2 side. Output changes by providing DC voltage of 0V~1V (M5207L01) or 0V~5V (M5207L05) between this terminal and COM terminal. Approximately 100nA is neccessary as bias current.
⑨	ch2 output	OUT2	This is an output terminal on ch2 side. Signal input from ch2 input is output to this terminal as current signal.
⑩	(+) supply voltage	$+V_{CC}$	This is a power terminal on plus side.

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	± 18 (36)	V
P_d	Power dissipation	800	mW
K_θ	Thermal derating (Ta ≧ 25℃)	8	mW/℃
T_{opr}	Operating temperature	− 20~ + 75	℃
T_{stg}	Storage temperature	− 55~ + 125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = + 9V, $V_{C\ (LINE)}$ = 1V, unless otherwise noted)

M5207L01

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	V_i = 0V	−	3.5	8.0	mA
V_{IM}	Maximum input voltage	f = 1kHz, THD = 1 %	2.0	2.3	−	Vrms
I_{OO}	Output offset current	V_i = 0V	−	± 0.3	± 2.0	μ A
Δ ATT_1	Attenuation error	f = 1kHz, V_i = + 10dBm	− 1.0	0.5	2.0	dB
Δ ATT_2	Attenuation deviation between channels	f = 1kHz, V_i = + 10dBm	−	± 0.3	± 2.0	dB
ATT_M	Linear maximum attenuation	f = 1kHz, V_i = + 10dBm, $V_{C\ (LINE)}$ = 0V	−	− 100	− 85	dB
THD	Total harmonic distortion	f = 1kHz, V_O = 1Vrms	−	0.15	1.0	%
CS	Channel separation	f = 1kHz, BW : 10Hz~30kHz	−	70	−	dB
HR	Hum rejection	f = 120Hz	−	57	−	dB
V_{NO}	Output noise voltage	V_i = 0V, BW : 10Hz~30kHz	−	60	120	μ Vrms

ELECTRICAL CHARACTERISTICS (T_a = 25℃, V_{CC} = ± 15V, $V_{C\ (LINE)}$ = 5V, unless otherwise noted)

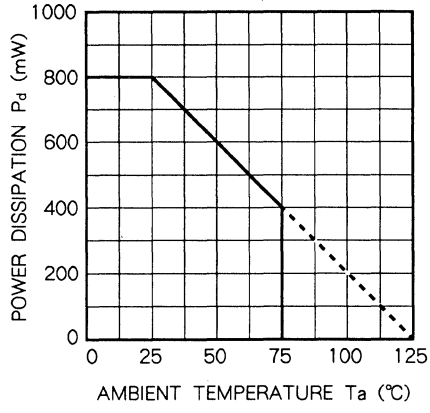
M5207L05

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	V_i = 0V	–	4.3	10.0	mA
V_{IM}	Maximum input voltage	f = 1kHz, THD = 1%	5.6	8.0	–	Vrms
I_{OO}	Output offset current	V_i = 0V	–	± 0.3	± 2.0	μA
Δ ATT_1	Attenuation error	f = 1kHz, V_i = + 10dBm	– 1.0	0.5	2.0	dB
Δ ATT_2	Attenuation deviation between channels	f = 1kHz, V_i = + 10dBm	–	± 0.3	± 2.0	dB
ATT_M	Linear maximum attenuation	f = 1kHz, V_i = + 10dBm, $V_{C\ (LINE)}$ = 0V	–	– 100	– 85	dB
THD	Total harmonic distortion	f = 1kHz, V_O = 1Vrms	–	0.15	1.0	%
CS	Channel separation	f = 1kHz, BW : 10Hz~30kHz	–	70	–	dB
HR	Hum rejection	f = 120Hz	–	57	–	dB
V_{NO}	Output noise voltage	V_i = 0V, BW : 10Hz~30kHz	–	60	120	μVrms

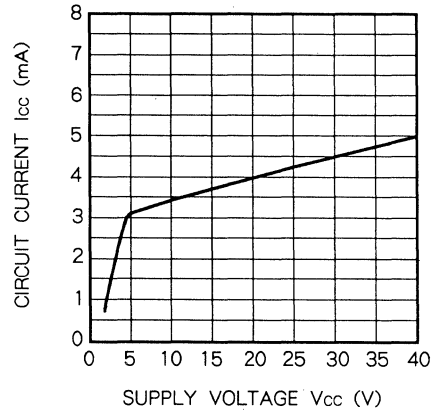
TYPICAL CHARACTERISTICS

M5207L01

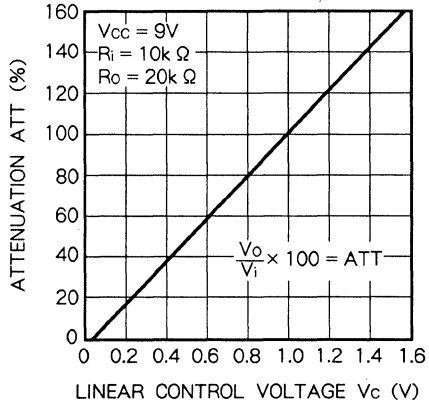
THERMAL DERATING (MAXIMUM RATING)



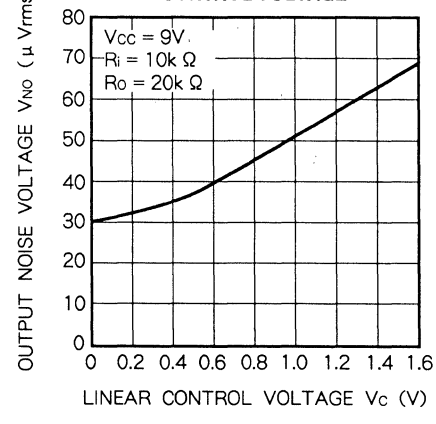
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



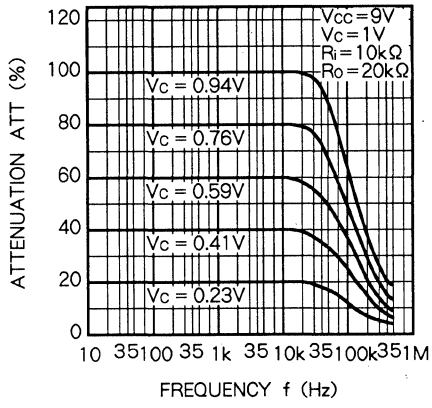
ATTENUATION VS. CONTROL VOLTAGE



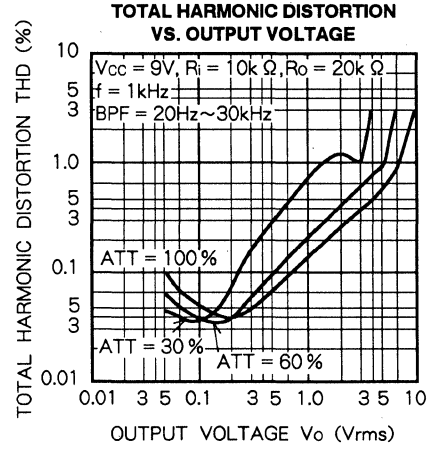
OUTPUT NOISE VOLTAGE VS. CONTROL VOLTAGE



ATTENUATION VS. FREQUENCY

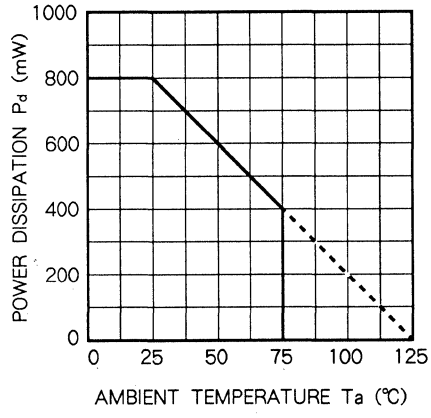


TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE

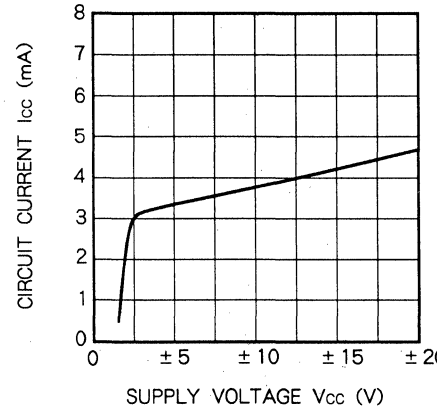


M5207L05

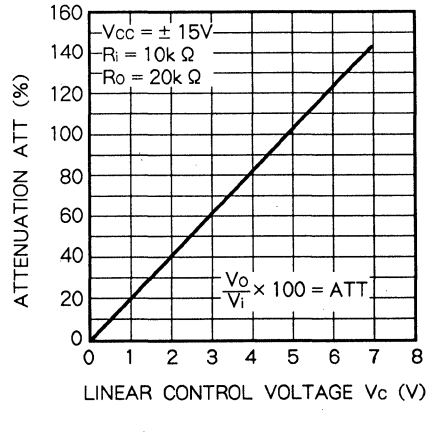
THERMAL DERATING (MAXIMUM RATING)



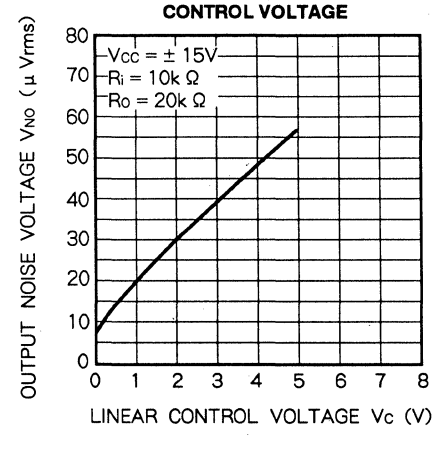
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



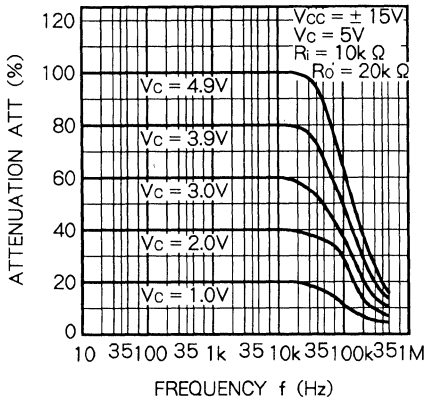
ATTENUATION VS. CONTROL VOLTAGE



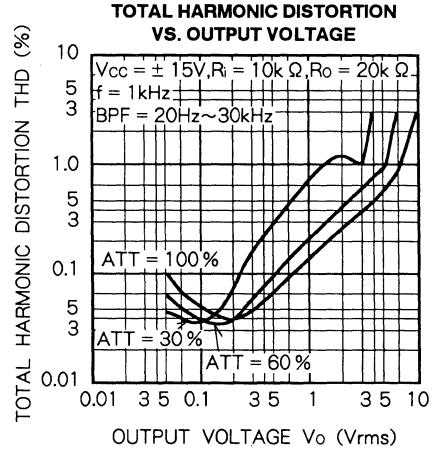
OUTPUT NOISE VOLTAGE VS. CONTROL VOLTAGE



ATTENUATION VS. FREQUENCY

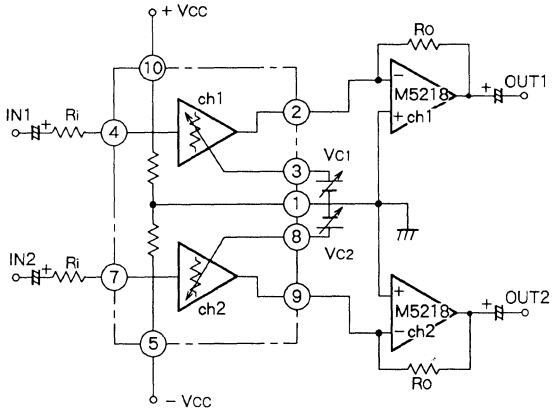


TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE

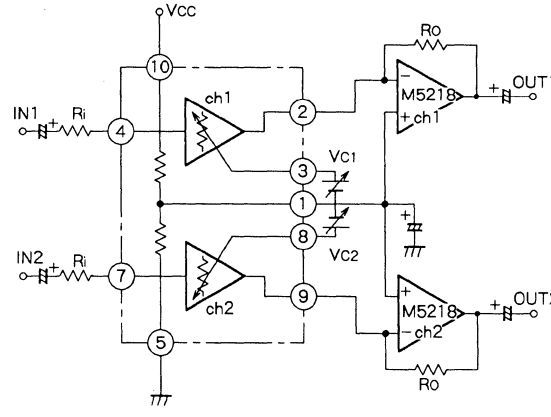


EXAMPLE OF APPLICATION CIRCUIT

(1) Example of standard application circuit

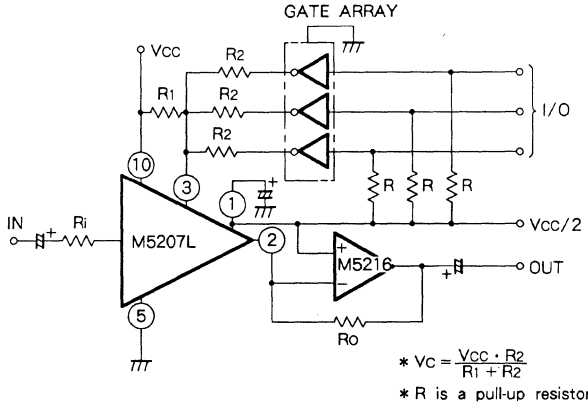


(a) 2 power sources are used



(b) Single power source is used

(2) Example of programmable ATT circuit

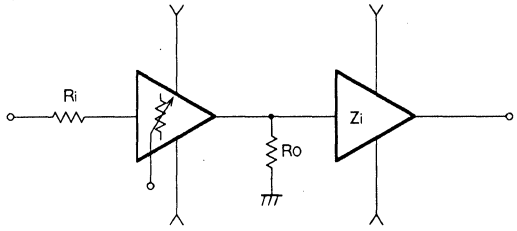


$* Vc = \frac{Vcc \cdot R2}{R1 + R2}$

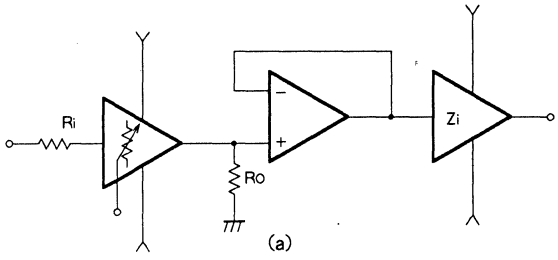
* R is a pull-up resistor

NOTES

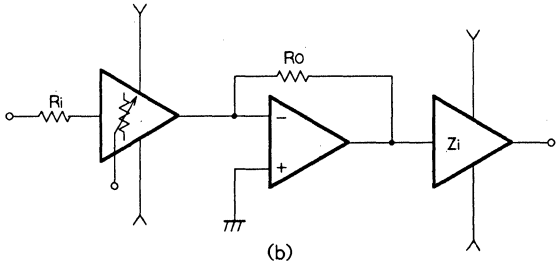
1. Internal differential circuit is balanced (when Vc = 5V for M5207L05, Vc = 1V for M5207L01) by selecting Ro = 2Ri, which makes 0dB and one time amplifier.
2. Output circuit is a float output by collector connection of transistors PNP and NPN, and it is necessary to set the potential at one end of external resistor Ro. (Refer to the section of [mechanism of I/O voltage and current conversion].)
3. M5207L uses class "A" or "B" amplifier for voltage ↔ current conversion. Maximum input current is not limited like M5222 or M5241, but there exists a maximum value because of saturation of output transistor. Therefore, it is possible to input large signal by decreasing the input current by selecting larger input and output resistance. Set the resistance value according to usages because the larger the resistance becomes, the larger the noise also becomes.
4. Voltage gain is determined by Vc, Ri and Ro, and it may be affected by the value of input impedance connected next. (Z_i is inserted in parallel with Ro to decrease the impedance.) (See following figure)



Usually, buffer amplifier of transistor or operational amplifier is connected. (See following figures (a), (b))



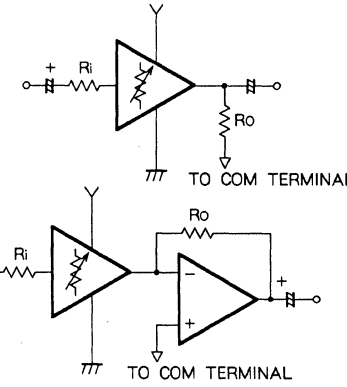
(a)



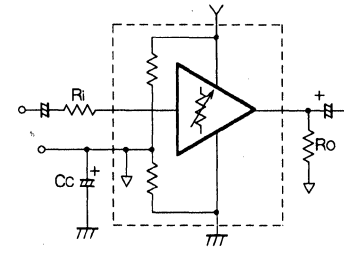
(b)

In the circuit in Figure (a), input signal has antiphase, potential of output terminal varies by the signal, and the maximum output voltage is also affected by residual voltage in the output circuit (residual voltage of approximately 1V from + Vcc and − Vcc is generated). Whereas, in the circuit in Figure (b), input signal has equal phase, potential of output terminal is fixed, and residual voltage in the output circuit does not affect at all. Pay attention to the difference.

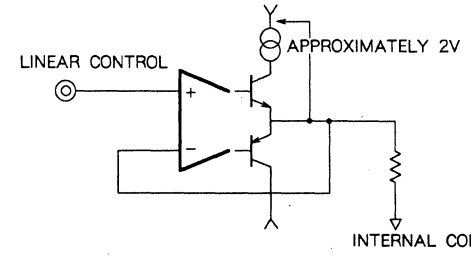
5. Note when used by single power source
   - Set one end of Ro to COMMON potential.



   - Connect condenser Cc between COM terminal and ground to reduce impedance of COM terminal.



6. Range of supply voltage is affected largely by the range of control voltage. A stage of current mirror circuit is connected to the output push-pull circuit of control circuit and residual voltage of 2V from Vcc at the lowest is necessary, which means Vcc ≧ Vc + 2V. 2V at the lowest is enough for operation of − Vcc.

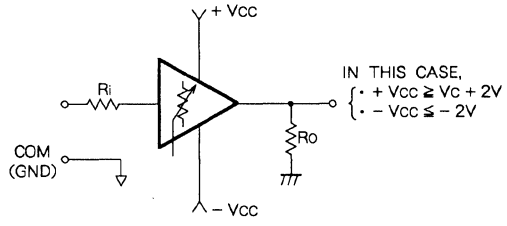


M5207L01/M5207L05

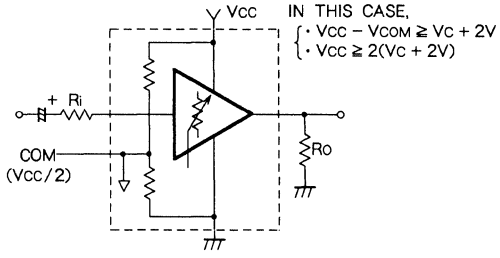
LINEAR CONTROL DUAL VCA IC

This IC incorporates a midpoint voltage generator. Set $V_{CC} - V_{COM}$ (V_{COM} is usually $V_{CC}/2$) larger than $V_C + 2V$ when used by single power source.

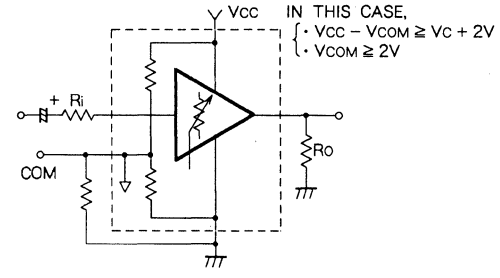
2V potential V_{COM} from ground to COMMON terminal is enough for operation. It is also possible to set V_{CC} low by shifting the level of V_{COM} by an external resistor.



(a) When two power sources are used

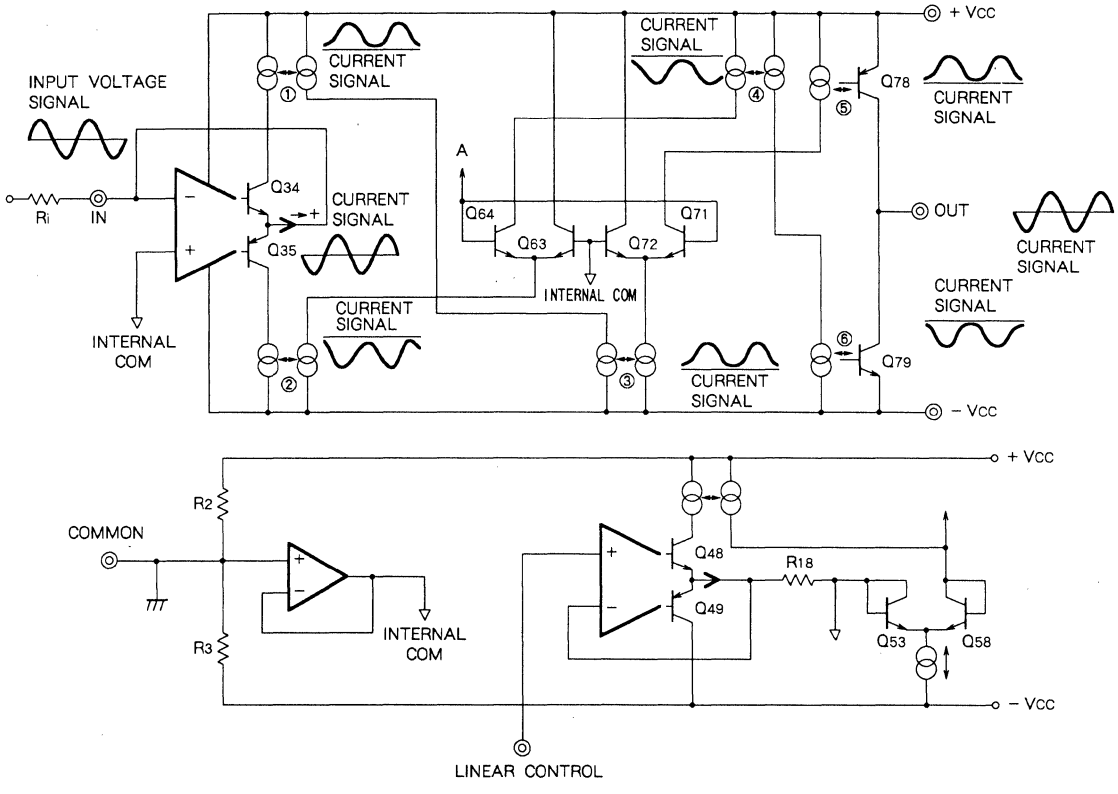


(b) When single power source is used (with no modification)



(c) When single power source is used (when V_{COM} is shifted in level)

OPERATION CIRCUIT



BASIC PRINCIPLE OF OPERATION

M5207L is a VCA (Voltage Controlled Amplifier) IC which inputs current and outputs current. This IC converts input signal to current signal by an external input resistor and sends to the current mirror output circuit through differential circuit. This current signal is converted again to voltage signal by an external output resistor and works as voltage input or voltage output apparently. Attenuation is controlled by control voltage Vc by changing balance in differential circuit (changing gm).

Its basic principle of operation is explained briefly in the following.

1. Mechanism of I/O voltage and current conversion

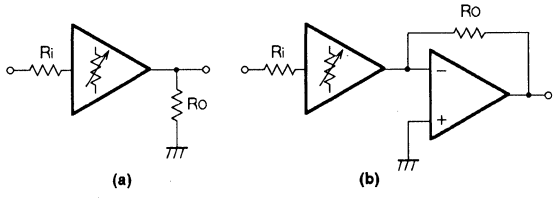
Input circuit is a voltage and current conversion circuit using operational amplifier as shown in the block diagram. Input voltage V_I is sent inside the IC as input current $i_i = V_I/R_I$ by an external resistor R_I.(Phase is reversed.) The current sent is divided into half waves by push-pull circuit (Q_{34}, Q_{35}) in the input operational amplifier and is sent to the output circuit as current signal by current mirrors ①~⑥ and differential circuits (Q_{63}, Q_{64}, Q_{71}, Q_{72}).

Output circuit forms a current composition circuit using current mirrors and the composed current signal is obtained at the output terminal.

This current signal is obtained as output signal V_O by the external output resistor.

It is, however, necessary to set DC electric potential at one end of output resistor because the output circuit is a float circuit by collector connection of PNP and NPN transistors.

There are two methods for the setup : set R_O terminal to equal potential to COM (GND when two power sources are used) ; set by current and voltage conversion circuit using operational amplifier, as shown in the following figures.



Note that the output signal obtained in (a) has antiphase to the input signal and that in (b) has equal phass to the input signal.

2. Mechanism in attenuation

Output is controlled by adding positive voltage for COM terminal to Vc terminal.

Change the current allocation of differential circuit and gain of this circuit by providing a fixed potential to one base (Q_{63}, Q_{72}) of differential circuit from COM terminal and providing control voltage Vc to another base (Q_{64}, Q_{71}) through the control circuit.

When external control voltage is provided to the bases of Q_{64} and Q_{71} directly, attenuation vs control voltage characteristic changes indexically as explained in the following, but the chraracteristic is converted to linear characteristic by inserting a control circuit.

This is the main feature of this IC.

(1) Basic mechanism of attenuation

Input signal V_I is converted to current signal i_i ($=\frac{V_I}{R}$) by input resistor R_I.

This current is divided into half waves by push-pull circuit Q_{34} and Q_{35} and each is sent to the differential circuit by current mirrors ①, ②, ③.

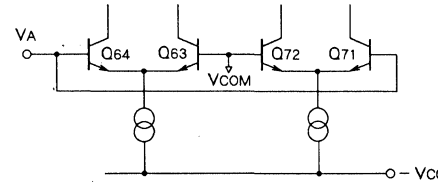
When the differential circuit is balanced (base potentials are equal), collector current of Q_{63} and Q_{64}, Q_{71} and Q_{72} becomes equal and the current sent by current mirrors ①, ②, ③ is divided equally here. This current is sent to the output terminal by current mirrors ④, ⑤, ⑥ and half waved currents are compounded and output current $i_i/2$ is obtained.

Here, select $R_O = 2R_I$ to get

$$V_O = i_i/2 \cdot R_O = i_i/2 \cdot 2R_I = i_i \cdot R_I = V_I$$

which means an amplifier with gain 1.

Let's see attenuation characteristics with this resistance selection when COM potential is provided to the bases of Q_{63} and Q_{72} and V_A to the bases of Q_{64} and Q_{71}. Current signal divided into half waves by push-pull circuit is expressed in i_i+ and i_i- ($i_i = i_i+ + i_i-$)



Each value of V_{BE} in the differential stage is :

$$V_{BE63} \fallingdotseq \frac{kt}{q} \ln\left(\frac{I_{C63}}{I_S}\right)$$

$$V_{BE64} \fallingdotseq \frac{kt}{q} \ln\left(\frac{I_{C64}}{I_S}\right)$$

$$V_{BE71} \fallingdotseq \frac{kt}{q} \ln\left(\frac{I_{C71}}{I_S}\right)$$

$$V_{BE72} \fallingdotseq \frac{kt}{q} \ln\left(\frac{I_{C72}}{I_S}\right)$$

k : Boltzman's constant
T : Absolute temperature
q : Electric charge
I_S : Saturation current

The above equations result in

$$\Delta V_{BE} = V_A - V_{COM}$$

$$= V_{BE64} - V_{BE63} = \frac{kt}{q} \ln\left(\frac{I_{C64}}{I_{C63}}\right)$$

$$= V_{BE71} - V_{BE72} = \frac{kt}{q} \ln \left(\frac{I_{C71}}{I_{C72}} \right)$$

Here,

$I_{C63} + I_{C64} = I_i +$

$I_{C71} + I_{C72} = I_i -$

Therefore,

$$V_A - V_{COM} = \frac{kt}{q} \ln \frac{I_{C64}}{i_i - I_{C64}}$$

$$V_A - V_{COM} = \frac{kt}{q} \ln \frac{I_{C71}}{i_i - I_{C71}}$$

It is supposed that $V_{COM} = 0$ to simplify the equation because $V_{COM} = 0V$ when two power sources are output terminal :

Therefore,

$$I_{C64} = i_i - \cdot \frac{\exp(\frac{q}{kt} \cdot V_A)}{1 + \exp(-\frac{q}{kt} \cdot V_A)}$$

$$= i_i - \cdot \frac{1}{1 + \exp(-\frac{q}{kt} \cdot V_A)}$$

$$I_{C71} = i_i + \cdot \frac{1}{1 + \exp(-\frac{q}{kt} \cdot V_A)}$$

And current shown in the following equation flows to the output terminal :

$$i_o = I_{C78} + I_{C79}$$

$$= I_{C64} + I_{C71} = \frac{i_i}{1 + \exp(-\frac{q}{kt} \cdot V_A)}$$

whose gain is :

$$\frac{V_O}{V_i} = \frac{i_o \cdot R_O}{I_i \cdot R_i} = \frac{i_o \cdot 2R_O}{I_i \cdot R_i} = \frac{2}{1 + \exp(-\frac{q}{kt} \cdot V_A)}$$

Convert is into dB :

$$ATT = 20 \log \left(\frac{2}{1 + \exp(-\frac{q}{kt} \cdot V_A)} \right)$$

ATT = 0dB when $V_A = 0$

When $1 \ll \exp(-\frac{q}{kt} \cdot V_A)$

$$ATT \fallingdotseq -\frac{20}{\ln 10} \cdot (-\frac{q}{kt} \cdot V_A) + 20 \log 2$$

and this shows that attenuation characteristic changes indexically for Vc change.

(2) Linear control mechanism

Attenuation changes indexically for the potential difference of bases in differential circuit as explained above. Attenuation for control voltage changes linearly by providing control voltage through the linear control circuit.

Control circuit consists of operational amplifier, current mirrors and differential circuits as shown in the block diagram.

First, control voltage Vc provided is converted into control current Ic by R_{18}.

$$I_C = \frac{V_C}{R_{18}}$$

And differential circuits Q_{53} and Q_{58} are biased by constant current I, When $I_{C53} = I_{C58} = \frac{1}{2}$

the differential circuit is balanced. (when Vc = 5V for M5207L05, and Vc = 1V for M5207L01)

This means that the potential V_A at point A becomes equal to that of V_{COM}

$$V_A = V_{COM} - V_{BE53} + V_{BE58} = V_{COM}$$

Comparing it with the former section, attenuation becomes 0dB or one time gain. Suppose that control voltage Vc is added to the linear control terminal here.

Each value of V_{BE} in the differential circuit here is :

$$V_{BE53} \fallingdotseq \frac{kt}{q} \ln \frac{I_{C53}}{I_S}$$

$$V_{BE58} \fallingdotseq \frac{kt}{q} \ln \frac{I_{C58}}{I_S}$$

$$V_A - V_{COM} = V_{BE58} - V_{BE53} = \frac{kt}{q} \ln \frac{I_{C58}}{I_{C53}}$$

It is supposed that $V_{COM} = 0$ to simplify the equation because V_{COM} is 0V when two power sources are used.

$$V_A = \frac{kt}{q} \ln \frac{I_{C58}}{I_{C53}}$$

And I_{C53} and I_{C58} are respectively :

$$I_{C53} = I_C = \frac{V_C}{R_{18}}$$

$$I_{C58} = I - I_{53} = I - \frac{V_C}{R_{18}}$$

and

$$V_A = \frac{kt}{q} \ln \frac{I - \frac{V_C}{R_{18}}}{\frac{V_C}{R_{18}}}$$ is obtained.

Substitute it for the equation of gain obtained in the former section :

$$\frac{V_O}{V_i} = \frac{2}{1 + \exp(-\frac{q}{kt} \cdot V_A)}$$

$$= \frac{2}{1 + \exp(-\frac{q}{kt} \cdot \frac{kt}{q} \ln \frac{I - (V_C/R_{18})}{V_C/R_{18}})}$$

$$= \frac{2}{I \cdot R_{18}} \cdot V_C$$

and excellent temperature characteristic and attenuation proportional to Vc can be obtained.

This control circuit also has a system to compensate for short of attenuation (gain does not become 0 when Vc = 0) by offset voltage of differential circuit.

M5222L,P,FP

DUAL VCA FOR LOW VOLTAGE ELECTRONIC VOLUME CONTROL

DESCRIPTION

The M5222 is a dual VCA designed as an electronic volume control capable of operating in a wide supply voltage range between 1.8V~20V.

The IC is an optimum device for electronic equipment requiring low voltage operation, such as video movie systems.

FEATURES

- Capable of operating at low voltage ····· Vcc = 1.8~20V
- Two built-in channels
  ····· Simultaneous control of both channels is possible with Vc(control) at pin ⑤
- Logarithmic response VCA
  ····· Logarithmic response equivalent to A-curve volume
- Large ATT range ····· 0dB(Vc ≒ 0)~ − 90dB (Vc ≒ − 270mV)(typ)
- High maximum input voltage
  ····· Vi = 1.0Vrms(typ)(@ Vcc = 3V)
- Low distortion ratio ····· THD = 0.05%
- Similar characteristics between 2 channels

Outline 8P5(L)

2.54mm pitch 340mil SIP
(2.8mm × 19.0mm × 6.4mm)

Outline 8P4(P)

2.54mm pitch 300mil DIP
(6.3mm × 8.9mm × 3.3mm)

Outline 8P2S-A(FP)

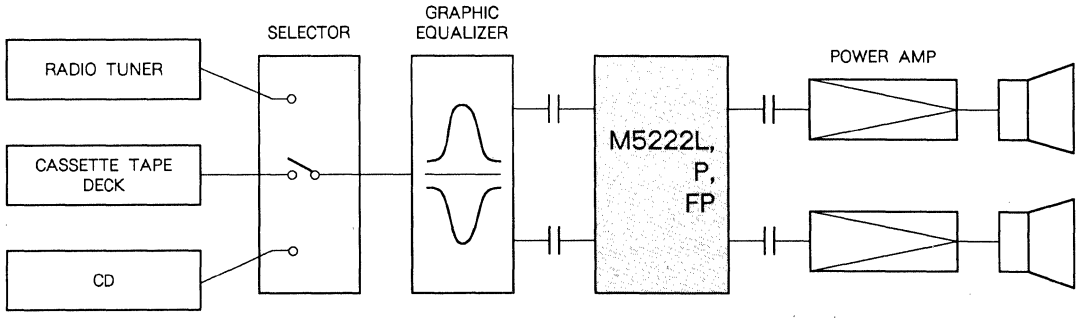
1.27mm pitch 225mil SOP
(4.4mm × 5.0mm × 1.5mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· Vcc = 1.8~20V

Rated dissipation voltage
····· 800(L), 625(P), 440(FP)mW

SYSTEM CONFIGURATION

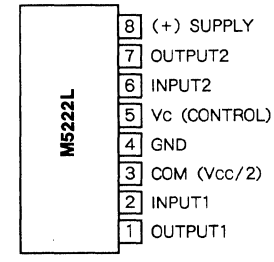


MITSUBISHI ELECTRIC

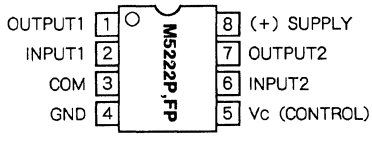
M5222L,P,FP

DUAL VCA FOR LOW VOLTAGE ELECTRONIC VOLUME CONTROL

PIN CONFIGURATION

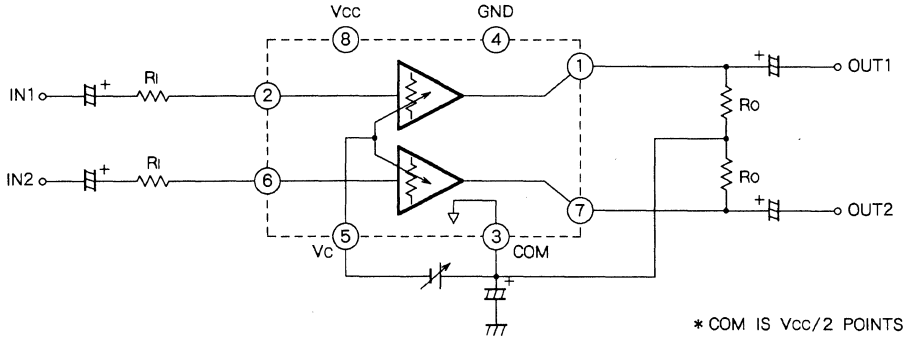


Outline 8P5 (L)



Outline 8P4(P)
8P2S-A(FP)

IC INTERNAL BLOCK DIAGRAM



Note 1. RI is used to convert input voltage to current.
2. RO is an output resistor used to convert the currentoutput signal to voltage. Connect this output with COM pin 3 to fix the DC output potential.
3. The COM pin is used for making a 1/2pint supply voltage within the IC. It is used in connecting RO and in Vc control.

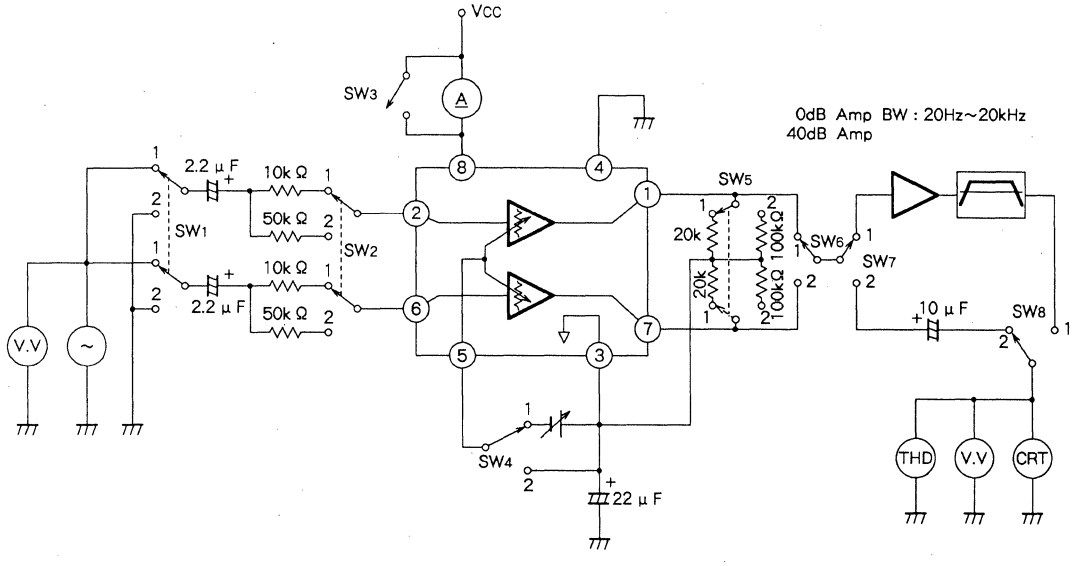
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	20	V
P_d	Power dissipation	800(SIP)/625(DIP)/440(FP)	mW
K_θ	Thermal derating (Ta ≧ 25℃)	8(SIP)/6.25(DIP)/4.4(FP)	mW/℃
T_{opr}	Operating temperature	− 20 ~ + 75	℃
T_{stg}	Storage temperature	− 55 ~ + 125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Vcc	Limits Min	Limits Typ	Limits Max	Unit
I_{CC}	Circuit current	V_i = 0, V_C = 0		3V	2.5	3.6	5.5	mA
V_{iM1}	Maximum input voltage	f = 1kHz, V_C = 0, THD = 1 %	R_I = 10k Ω, R_O = 20k Ω	3V	0.7	1.0	−	Vrms
V_{iM2}	Maximum input voltage		R_I = 50k Ω, R_O = 100k Ω	9V	2.3	3.4	−	Vrms
ATT_M	Maximum attenuation	R_I = 10k Ω, R_O = 20k Ω, V_C = − 270mV		3V	80	90	−	dB
ATT_{O1}	Attenuation error	f = 1kHz, V_C = 0, V_i = 0dBm	R_I = 10k Ω, R_O = 20k Ω	3V	− 4.4	− 1.4	+ 1.6	dB
ATT_{O2}	Attenuation error		R_I = 50k Ω, R_O = 100k Ω	9V	− 5.0	− 2.0	+ 1.0	dB
Δ ATT	Attenuation deviation between channels	f = 1kHz, V_C = 0, V_i = 0dBm, R_I = 10k Ω, R_O = 20k Ω		3V	−	0.1	3.0	dB
V_{NO1}	Noise output voltage	V_C = 0, R_I = 10k Ω, R_O = 20k Ω, BW = 20Hz~20kHz		3V	−	30	60	μ Vrms
V_{NO2}	Noise output voltage	ATT = − 40dB, R_I = 10k Ω, R_O = 20k Ω, BW = 20Hz~20kHz		3V	−	5	−	μ Vrms

TEST CIRCUIT



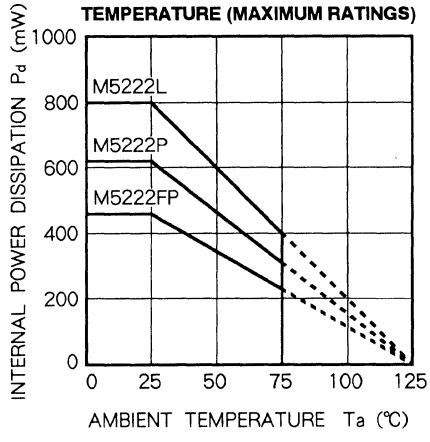
SWITCH MATRIX

Parameter		SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
ICC		2	1	OFF	2	1	1/2	2	2
VIM	1	1	1	ON	2	1	1/2	1	1
	2	1	2	ON	2	2	1/2	1	1
ATTM		1	1	ON	1	1	1/2	2	2
ATT	01	1	1	ON	2	1	1/2	2	2
	02	1	2	ON	2	2	1/2	2	2
VNO	1	2	1	ON	2	1	1/2	1	1
	2	2	1	ON	1	1	1/2	1	1

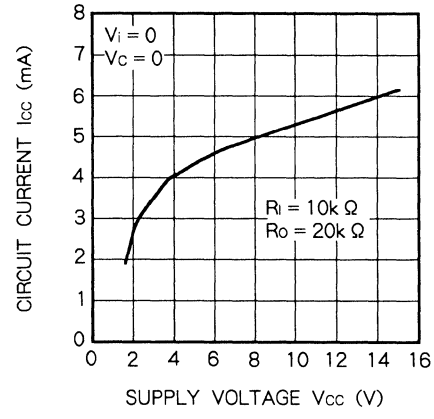
Note 1. Use 0dB amplification when measuring VIM
2. Use 40dB amplification when measuring VNO
3. VNO = measurement value/100 (40dB) (μ Vrms)

TYPICAL CHARACTERISTICS

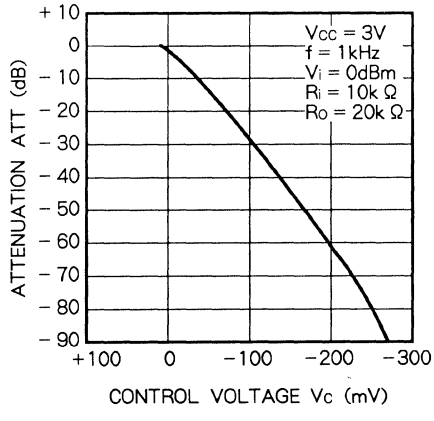
POWER DISSIPATION VS. AMBIENT TEMPERATURE (MAXIMUM RATINGS)



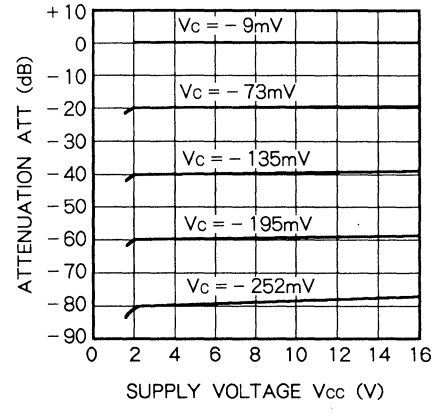
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



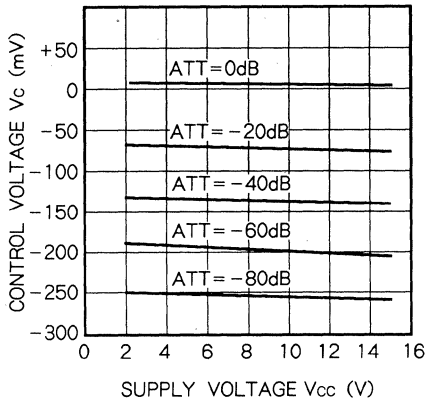
ATTENUATION VS. CONTROL VOLTAGE



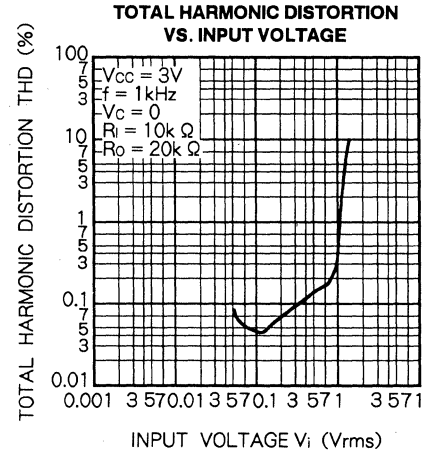
ATTENUATION VS. SUPPLY VOLTAGE



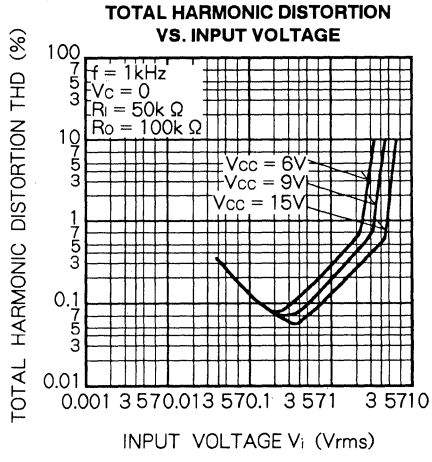
CONTROL VOLTAGE VS. SUPPLY VOLTAGE



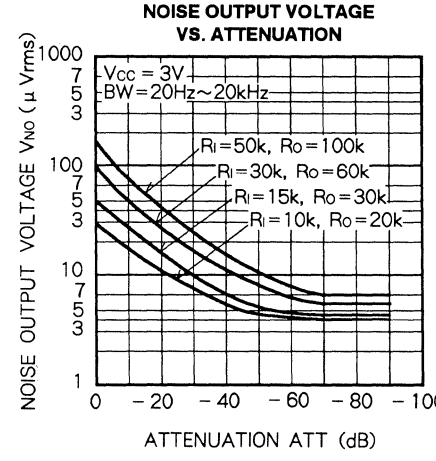
TOTAL HARMONIC DISTORTION VS. INPUT VOLTAGE



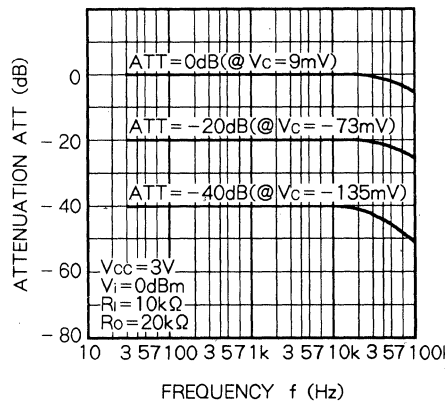
TOTAL HARMONIC DISTORTION VS. INPUT VOLTAGE



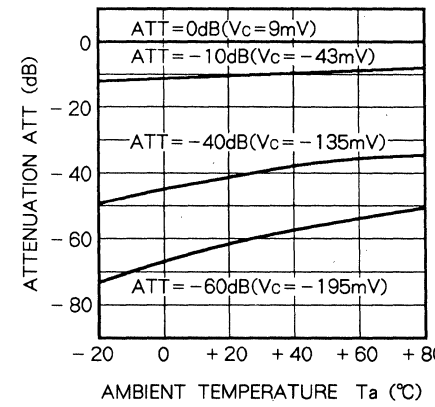
NOISE OUTPUT VOLTAGE VS. ATTENUATION



ATTENUATION VS. FREQUENCY

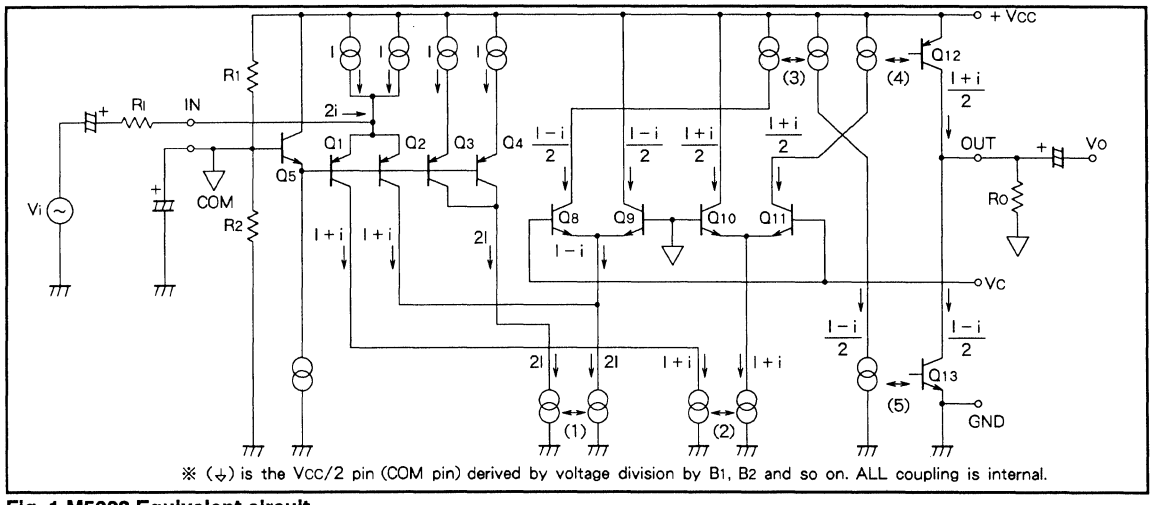


ATTENUATION VS. AMBIENT TEMPERATURE



BASIC PRINCIPLE OF OPERATION

The M5222 is a current input, current output type of VCA IC. This amplifier uses the principle by which changing the balance of the differential circuit with external control voltage Vc will change gm. The circuit is also called a variable transconductance (variable gm) OP amp. The basic principle of operation will be simply explained below.



※ (⏚) is the Vcc/2 pin (COM pin) derived by voltage division by B1, B2 and so on. ALL coupling is internal.

Fig. 1 M5222 Equivalent circuit

Basic voltage-current conversion mechanism for input and output

Applying the input signal V_i which flows through external input resistor R_I results in a change to a current signal at input terminal IN. The V_{BE} level shift of R_1, R_2, Q_5, Q_1, and Q_2 will cause input pin IN to become ground level by means of $V_{CC}/2$ in terms of direct current and to become ground level by means of the externally-connected capacitor in terms of alternating current. The signal input in this way will be sent to the output pin as a current signal by the current mirror and differential circuit. By taking this current signal through the externally-connected output resistor (load resistor), the signal can go through a current-to-voltage conversion and be obtained as output signal V_o.

The output transistors combine the currents by means of the joined PNP and NPN collector circuits. Basically, the DC potential floats and is not determined in this joining of currents. This is why one end of externally-connected resistor R_o is connected to the $V_{CC}/2$ pin and the DC level ($V_{CC}/2$) at the time of no signal is set.

Basic mechanism of attenuation

The output is controlled by means of changing the control voltage applied to the Vc pin with respect to the COM pin ($V_{CC}/2$ pin). By applying voltage from the COM pin to the base of one side of a differential circuit and applying voltage from the Vc pin to the other base, the current distribution of the differential circuit is changed and the gain of this circuit is changed.

Let us first consider when Vc equals zero (Vc − COM is shorted). Input signal V_i is converted to current by input resistor R_I and the i currents ($2i = V_i/R_I$) flow through the collectors of Q_1 and Q_2. When the current flowing in Q_i becomes $I + i$, the overall emitter current of the differential circuit consisting of Q_{10} and Q_{11} will also be determined as $I + i$ by means of current mirror (2). Since the base potential of Q_{10} and Q_{11} is the same, the current will be divided equally and current $(I + i)/2$ will flow in each of Q_{10} and Q_{11}. The current of current mirror (4) will also be determined as $(I + i)/2$ because of this.

Since the current of current mirror (1) is determined as $2I$ by the current flowing in Q_3 and Q_4, the total of the current flowing in Q_2 and the current flowing in differential circuit Q_8, Q_9 will also be $2I$. The current from Q_2 which will become $I + i$ flows here and as a result, the overall emitter current of the differential circuit will be $2I - (I + i) = I - i$. This current is devided the same way as in the differential circuit consisting of Q_{10} and Q_{11} with current $(I - i)/2$ flowing in each of Q_8 and Q_9. From this, the current of current mirror (3) is determined as $(I - i)/2$ and the current of current mirror (5) becomes $(I + i)/2$.

Now, current $(I - i)/2$ from current mirror (4) flows in transistor Q_{12} of the output stage. Since the current flowing in transistor Q_{13} from current mirror (5) is held at $(I - i)/2$, connecting output resistor R_o between the output pin and the COM pin will result in current i flowing through R_o and providing a voltage signal $V_o = i \cdot R_o$.

Here, by selecting $R_o = 2R_I$, $V_o = i \cdot R_o = 2i \cdot R_I = V_i$ and the amplifier will have a gain of 1.

Next, we will consider case of when control voltage Vc is applied with regard to the selection of this resistance.

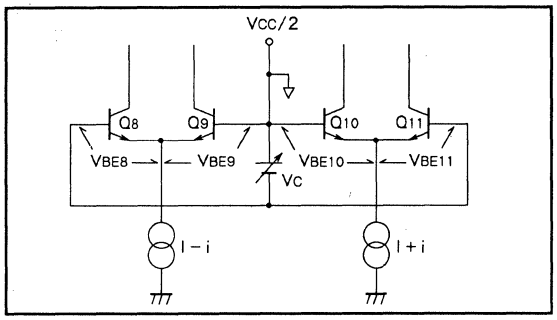


Fig. 2 Differential circuit

The values of V_{BE} of the differential stage will be as follows :

$$V_{BE8} \fallingdotseq \frac{kT}{q} \ln\left(\frac{I_{C8}}{I_S}\right)$$

$$V_{BE9} \fallingdotseq \frac{kT}{q} \ln\left(\frac{I_{C9}}{I_S}\right)$$

$$V_{BE10} \fallingdotseq \frac{kT}{q} \ln\left(\frac{I_{C10}}{I_S}\right)$$

$$V_{BE11} \fallingdotseq \frac{kT}{q} \ln\left(\frac{I_{C11}}{I_S}\right)$$

where,
- I_S : the saturation current
- k : the Boltzmann constant
- q : the amount of electric charge on the electrons
- T : the absolute temperature

From this,

$$-V_C = V_{BE8} - V_{BE9} = \frac{kT}{q} \ln \frac{I_{C8}}{I_{C9}}$$

$$-VC = V_{BE11} - V_{BE10} = \frac{kT}{q} \ln \frac{I_{C11}}{I_{C10}}$$

Here

$$I_{C8} + I_{C9} \fallingdotseq I - i$$

$$I_{C10} + I_{C11} \fallingdotseq I + i$$

$$-V_C = \frac{kT}{q} \ln \frac{I_{C8}}{I - i - I_{C8}}$$

$$-V_C = \frac{kT}{q} \ln \frac{I_{C11}}{I+i - I_{C11}}$$

The current flowing through Q_8 and Q_{11} will be

$$I_{C8} = \frac{(I - i)\exp(-\frac{q}{kT}V_C)}{1 + \exp(-\frac{q}{kT}\ V_C)} = \frac{I - i}{1 + \exp(\frac{q}{kT}V_C)}$$

$$I_{C11} = \frac{(I + i)\exp(-\frac{q}{kT}\ V_C)}{1 + \exp(-\frac{q}{kT}\ V_C)} = \frac{I - i}{1 + \exp(\frac{q}{kT}V_C)}$$

Current I_{C11} is the current of current mirror (4), and I_{C8} will be the same as the current of current mirror (5).

At this time, the current that will flow through the output pin will be the same as that in the explanation when Vc was equal to zero, and is expressed as

$$io = \frac{2i}{1 + \exp(\frac{q}{kT} \cdot V_C)}$$

The gain will be

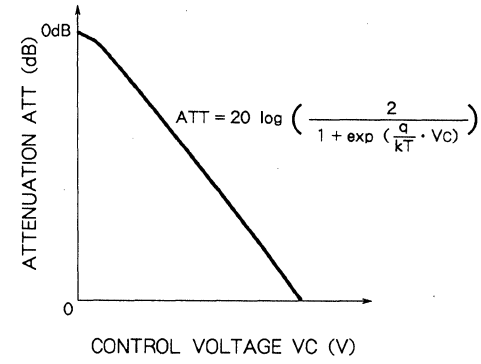
$$\frac{V_O}{V_i} = \frac{io \cdot R_O}{2i \cdot R_I} = \frac{2}{1 + \exp(\frac{q}{kT} \cdot V_C)}$$

and when calculated in dB,

$$ATT = 20 \log \left(\frac{2}{1 + \exp\ (\frac{q}{kT} \cdot V_C)}\right)$$

As in the graph below, the attenuation will change logarithmically with respect to the change of Vc.

ATTENUATION VS. CONTROL VOLTAGE



Setting and connection of input/output resistance

As explained above, the input signal is converted to current, but since the transistor of the input stage is biased at a fixed current of I = 76 μ A, the maximum value of the input current is determined at the least upper bound of I (Fig.3). Accordingly, when a large signal is input it is necessary to select a large input/output resistance and decrease the input current. Note that increasing the resistance will also increase the noise distortion factor, so the value of the setting should be made to suit the particular application.

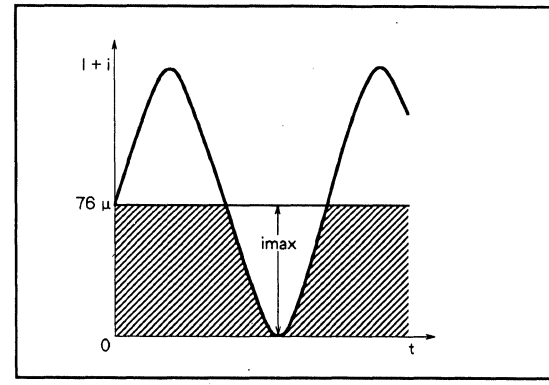


Fig. 3 Maximum current signal

MITSUBISHI ELECTRIC

The M5222 has a floating-type output stage with the collectors of Q_{12} and Q_{13} joined as shown in FIG. 4. Here, the difference of the combined currents will become the output current that will flow through the load. Note that it is necessary to set the DC potential of this output pin by externally-connected resistor R_O and that it is generally DC-connected to the $V_{CC}/2$ pin (or to pin (3)).

In terms of AC, it is necessary to set the output pin to ground level so that capacitor C is required. Since the voltage gain (amount of attenuation) is determined by R_O, the value of the input impedance connected to the next stage is sometimes affected. (Placing Z_I in parallel with R_O will lower the impedance.) Generally, a buffer amplifier composed of a transistor or OP amp connected.

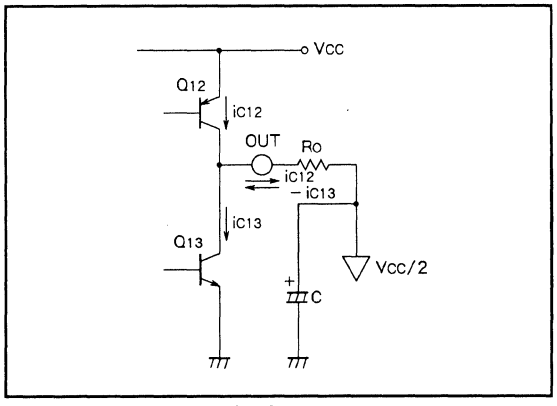


Fig. 4 Equivalent circuit of output stage

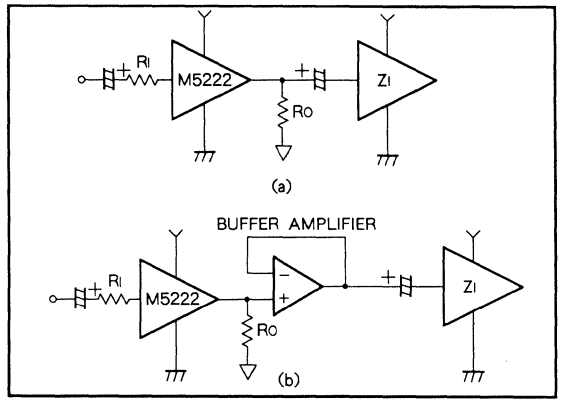
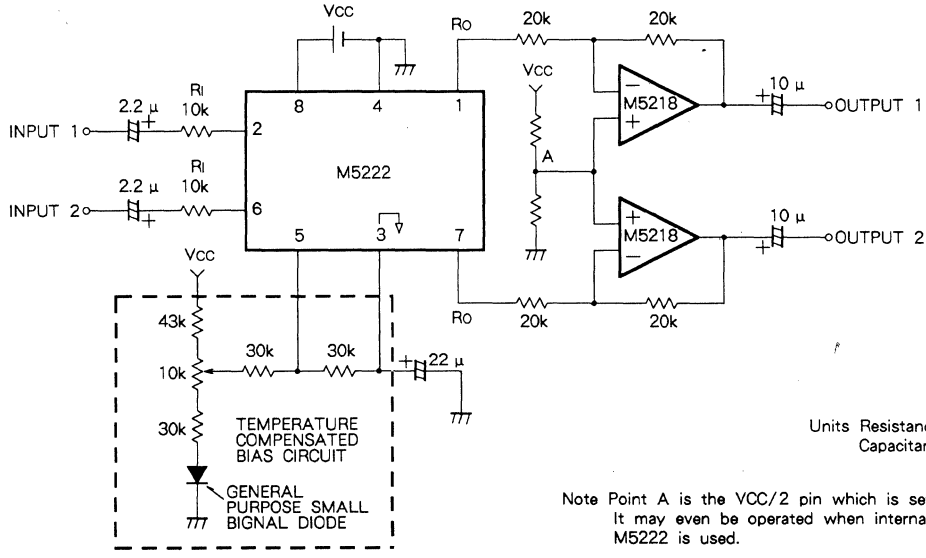


Fig. 5 Connection example

APPLICATION EXAMPLES

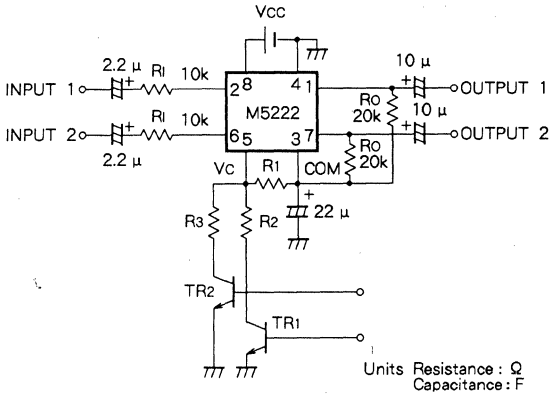
(1) TEMPERATURE COMPENSATED BIAS AND OUTPUT BUFFER CIRCUITS



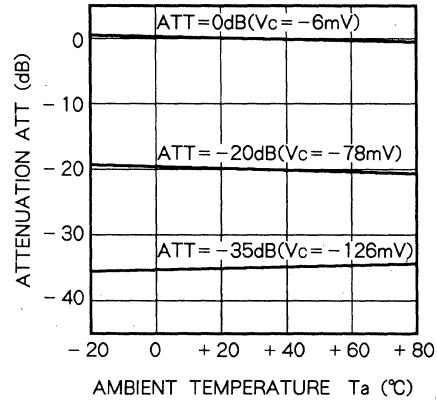
Units Resistance : Ω
Capacitance : F

Note Point A is the VCC/2 pin which is set externally. It may even be operated when internal pin 3 of M5222 is used.

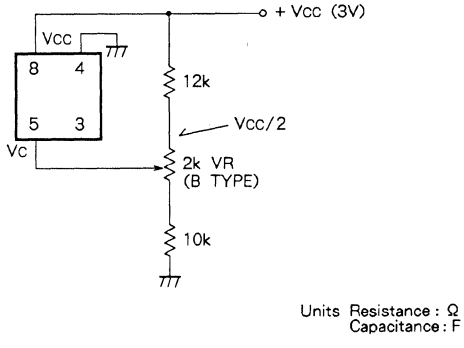
(2) PROGRAMMABLE ATTENUATION CIRCUIT



ATTENUATION VS. AMBIENT TEMPERATURE (TEMPERATURE COMPENSATION)

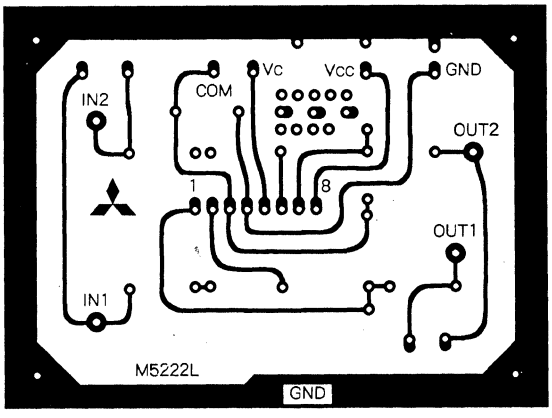


(3) CONTROL APPLICATION WITH EXISTING VOLTAGE CONTROL

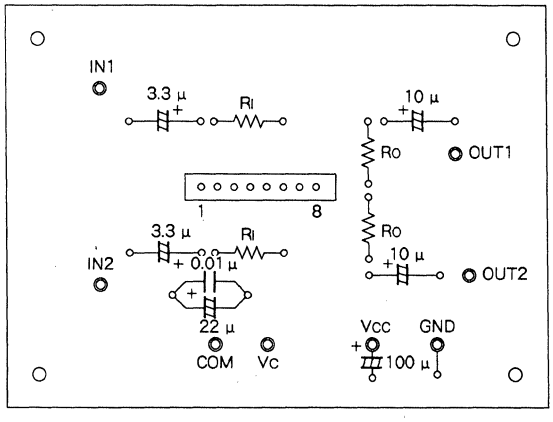


PRINTED CIRCUIT BOARD FOR CIRCUIT TESTING

PRINTED CIRCUIT BOARD WIRING DIAGRAM (COPPER FOIL SIDE)



(PARTS SIDE)



M5241L

DUAL VCA FOR ELECTRONIC VOLUME CONTROL

DESCRIPTION

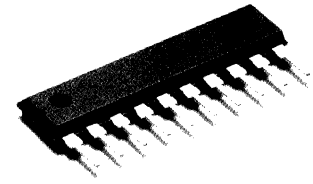
The M5241L is an optimum logarithmic VCA for controlling the volume of analog audio signals.

Each channel has a control pin and capable of independent operation.

The IC can be used in radio cassette tape recorders, car audio systems, and Hi-Fi VCR.

FEATURES

- Independent control terminal is provided 2 channels of VCA are incorporated
  ..... ch1 and ch2 can be controlled separately by V_C control (pin ⑥, ⑦)
- Maximum input voltage is large
  ..... V_i = 3Vrms(when THD = 0.5 %)
- Low distortion ..... THD = 0.02 %(when V_O = 1Vrms)
- Large ATT range ..... 0 ~ – 100dB
- S/N(dynamic range) is large 94dB
  (when ATT = 0dB, R_I = 15k Ω, R_O = 30k Ω, R_C = 1.8k Ω)
- Logarithmic response VCA
  ..... Logarithmic response equivalent to A-curve volume control
- Bias current controllable can be adjusted with external resistor
- Can be operated with a single power supply
  ..... Built-in COM pin③ V_{CC}/2 bias pin



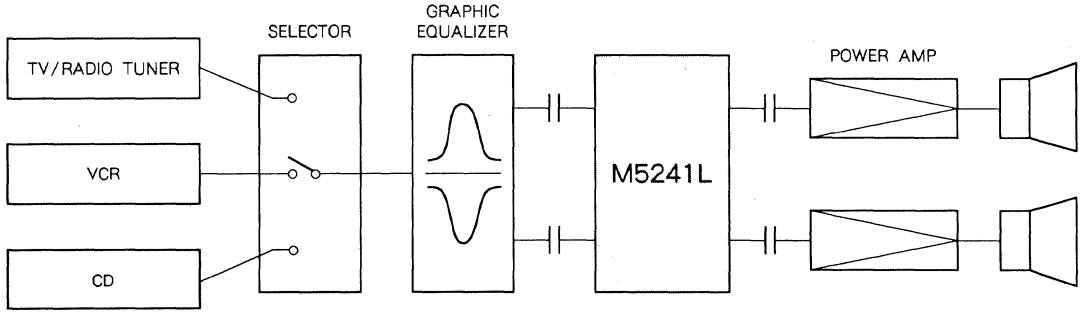
Outline 10P5

2.54mm pitch 340mil SIP
(2.8mm × 25.23mm × 6.3mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC}, V_{EE} = ± 7 ~ ± 18V

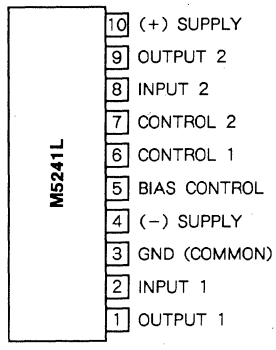
SYSTEM CONFIGURATION



M5241L

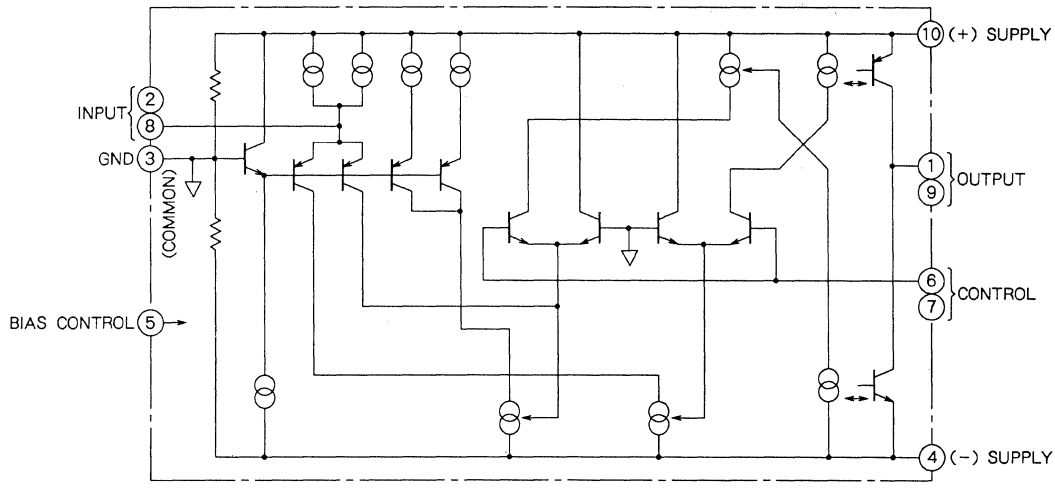
DUAL VCA FOR ELECTRONIC VOLUME CONTROL

PIN CONFIGURATION



Outline 10P5

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

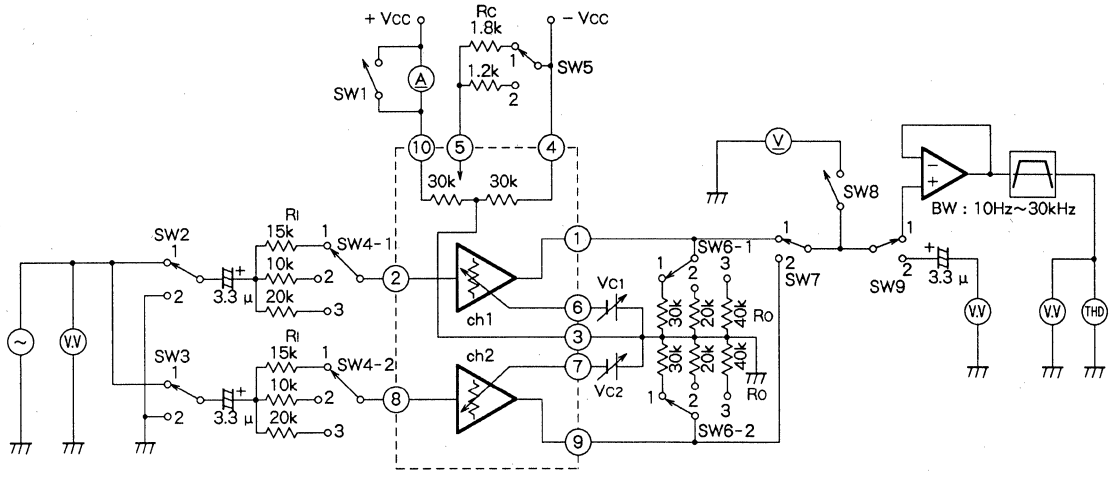
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	± 18 (36)	V
P_d	Power dissipation	800	mW
K_θ	Thermal derating (Ta ≧ 25℃)	8	mW/℃
T_{opr}	Operating temperature	− 20 ~ + 75	℃
T_{stg}	Storage temperature	− 55 ~ + 125	℃

ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}=±15V, R_i=15kΩ, R_O=30kΩ, R_C=1.8kΩ, V_C=0V unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
I_{CC}	Circuit current	V_i = 0V		2.5	3.8	6.5	mA
V_{IM1}	Maximum input voltage		f = 1kHz THD = 0.5 %	2.4	3.0	−	Vrms
V_{IM2}		R_i = 20kΩ, R_O = 40kΩ		−	4.2	−	Vrms
V_{IM3}		R_i = 10kΩ, R_O = 20kΩ, R_C = 1.2kΩ		−	2.5	−	Vrms
ATT_M	Maximum attenuation	V_i = + 10dBm, f = 1kHz, V_C = − 300mV		−	− 102	− 85	dB
ATT	Attenuation error	V_i = + 10dBm, f = 1kHz		− 2.0	− 0.5	+ 3.0	dB
Δ ATT	Attenuation deviation between channels	V_i = + 10dBm, f = 1kHz		−	± 0.1	± 3.0	dB
I_{OO}	Output offset current	V_i = 0V		−	± 5	± 20	μA
THD1	Total harmonic distortion	ATT = 0dB (V_C=0), V_O=1Vrms	f = 1kHz, filter BW :10Hz~30kHz	−	0.02	0.1	%
THD2		ATT=−10dB (V_C=−43mV), V_i=1Vrms		−	0.04	−	%
THD3		ATT=−20dB (V_C=−76mV), V_i=1Vrms		−	0.06	−	%
CC	Channel separation	f = 1kHz		−	73	−	dB
HR	Hum rejection	f = 120Hz		−	48	−	dB
V_{NO1}	Noise output voltage	ATT = 0dB (V_C = 0)	BW :10Hz~30kHz	−	57	120	μVrms
V_{NO2}		ATT=−40dB (V_C=−138mV)		−	8.5	−	μVrms
V_{NO3}		ATT=0dB (V_C=0), V_O=1Vrms, R_O=20kΩ, R_C=1.2kΩ		−	38	−	μVrms

TEST CIRCUIT

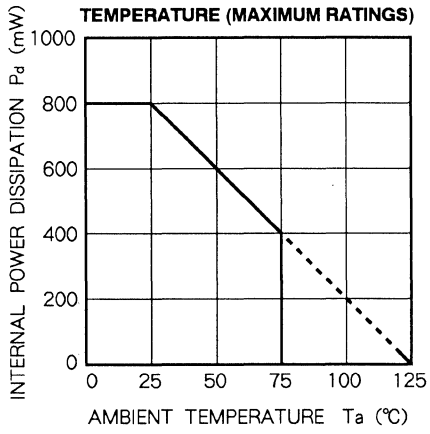


SWITCH MATRIX

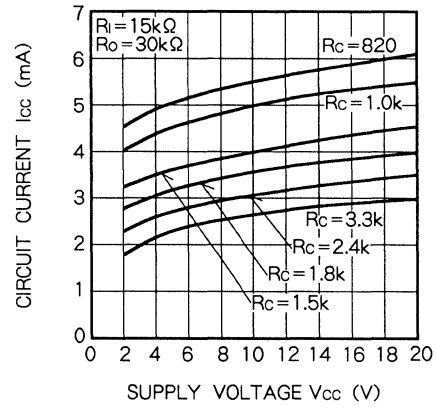
Parameter		SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	$V_{C1,2}$
Circuit current	I_{CC}	OFF	2	2	1	1	1	–	OFF	2	0V
Maximum input voltage	V_{IM1}	ON	1	1	1	1	1	1/2	OFF	1	0V
	V_{IM2}	ON	1	1	3	1	3	1/2	OFF	1	0V
	V_{IM3}	ON	1	1	2	2	2	1/2	OFF	1	0V
Maximum attenuation	ATT_M	ON	1/2	2/1	1	1	1	1/2	OFF	2	-300mV
Attenuation error	ATT	ON	1	1	1	1	1	1/2	OFF	2	0V
Attenuation diviation	Δ ATT	ON	1	1	1	1	1	1/2	OFF	2	0V
Output offset current	I_{OO}	ON	2	2	1	1	1	1/2	ON	2	0V
Total harmonic distortion	THD_1	ON	1/2	2/1	1	1	1	1/2	OFF	1	0V
	THD_2	ON	1/2	2/1	1	1	1	1/2	OFF	1	-43mV
	THD_3	ON	1/2	2/1	1	1	1	1/2	OFF	1	-76mV
Noise output voltage	V_{NO1}	ON	2	2	1	1	1	1/2	OFF	1	0V
	V_{NO2}	ON	2	2	1	1	1	1/2	OFF	1	-138mV
	V_{NO3}	ON	2	2	2	2	2	1/2	OFF	1	0V
Channel separation	C.C	ON	2/1	1/2	1	1	1	1/2	OFF	2	0V

TYPICAL CHARACTERISTICS

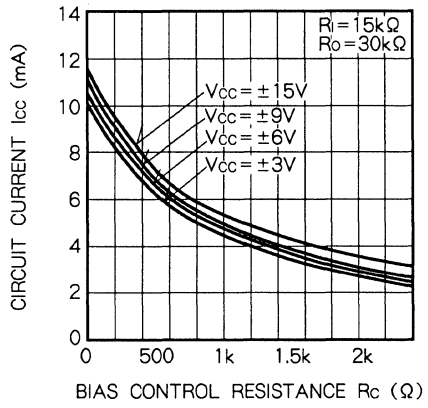
POWER DISSIPATION VS. AMBIENT TEMPERATURE (MAXIMUM RATINGS)



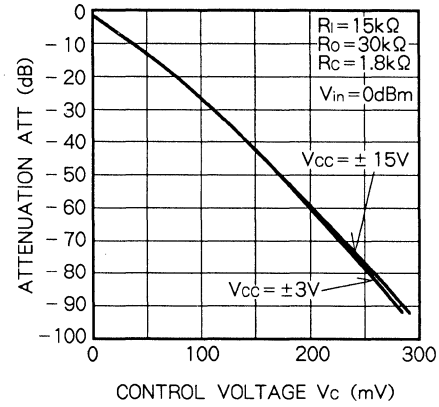
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



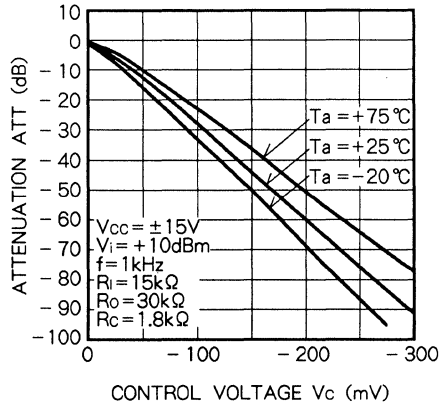
CIRCUIT CURRENT VS. BIAS CONTROL RESISTANCE



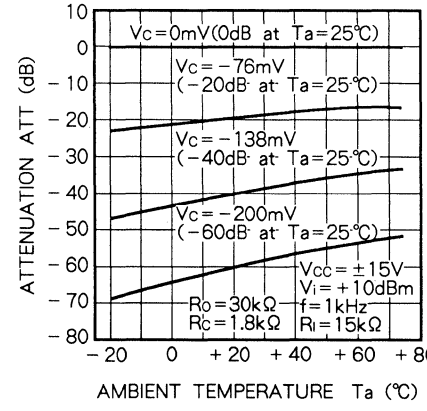
ATTENUATION VS. CONTROL VOLTAGE



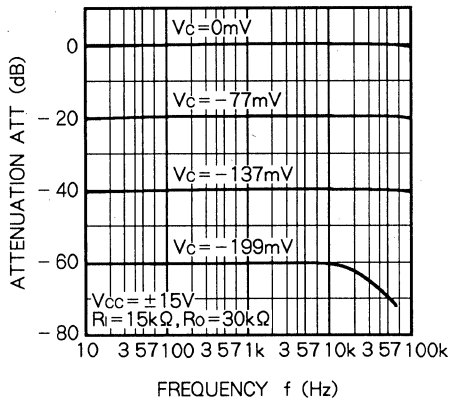
ATTENUATION VS. CONTROL VOLTAGE



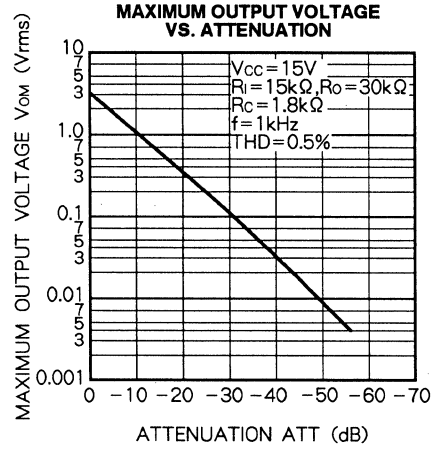
ATTENUATION VS. AMBIENT TEMPERATURE



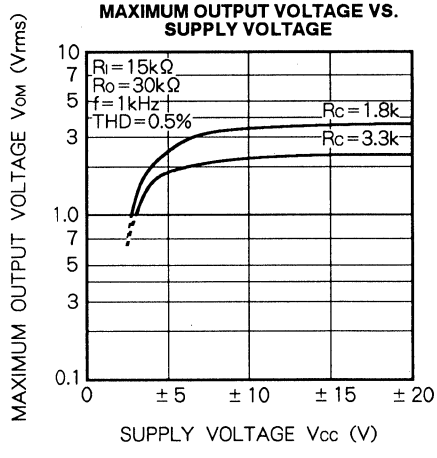
ATTENUATION VS. OUTPUT VOLTAGE



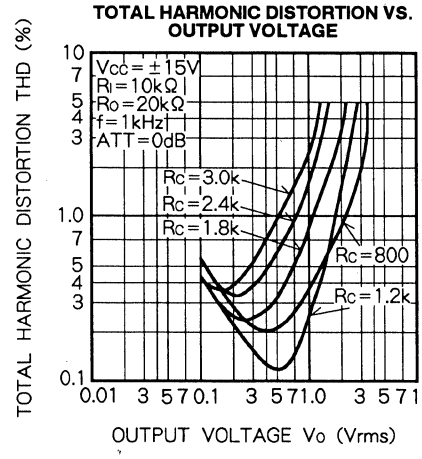
MAXIMUM OUTPUT VOLTAGE VS. ATTENUATION



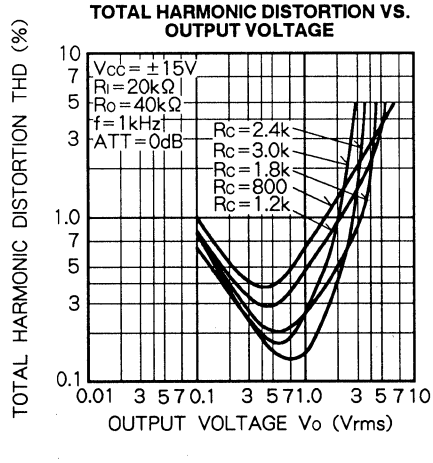
MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



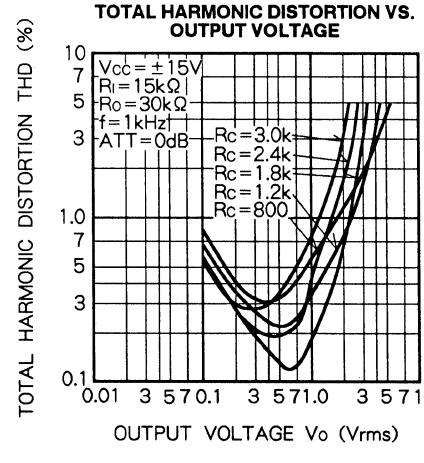
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



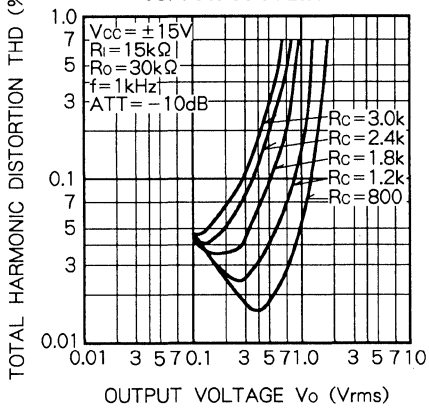
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



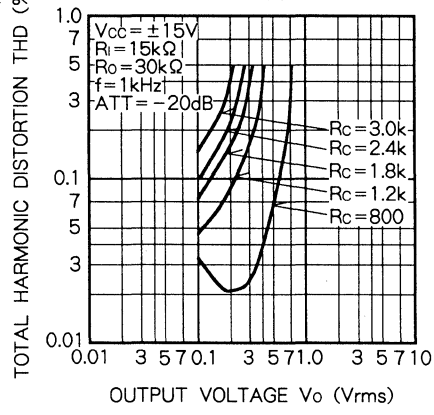
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



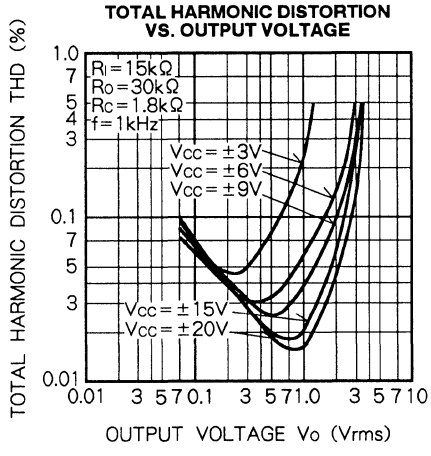
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



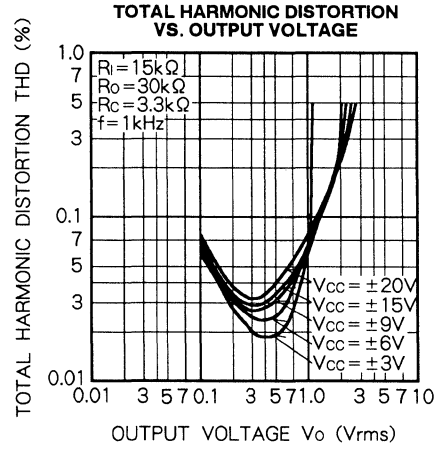
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



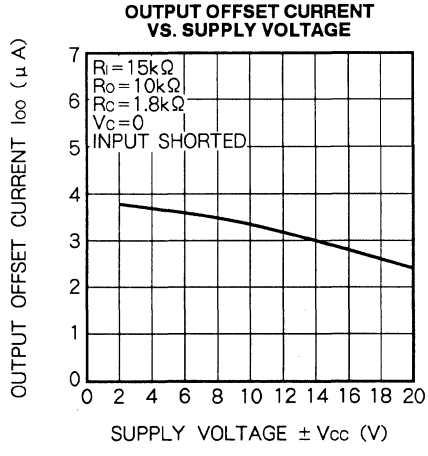
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



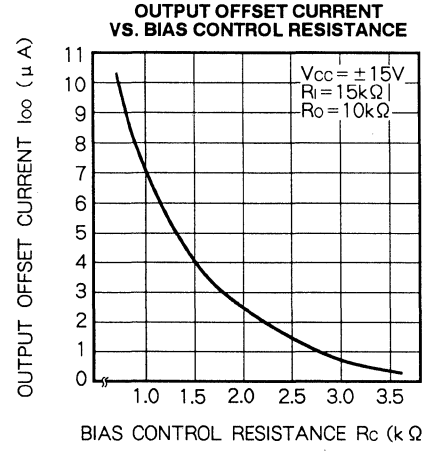
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



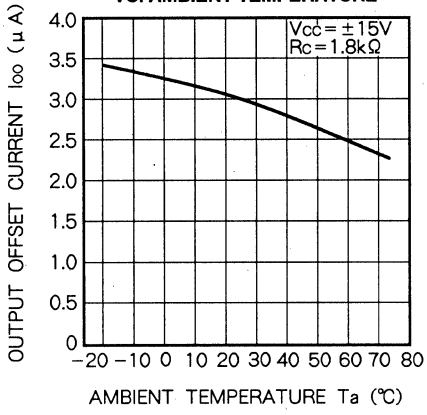
OUTPUT OFFSET CURRENT VS. SUPPLY VOLTAGE



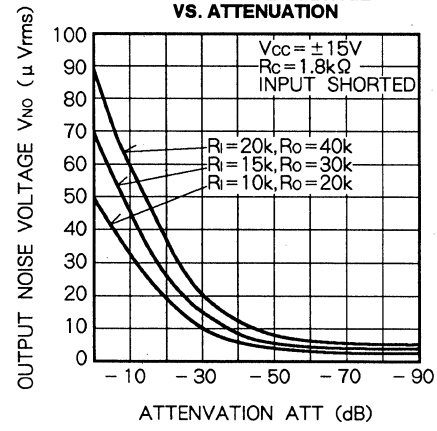
OUTPUT OFFSET CURRENT VS. BIAS CONTROL RESISTANCE



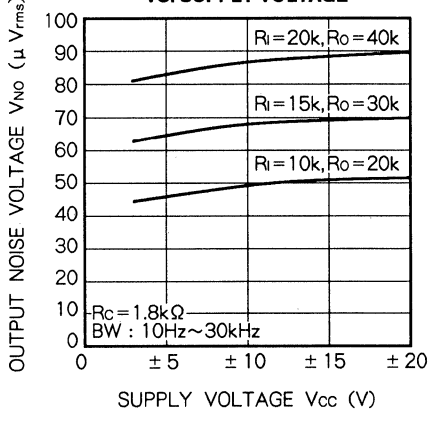
OUTPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE



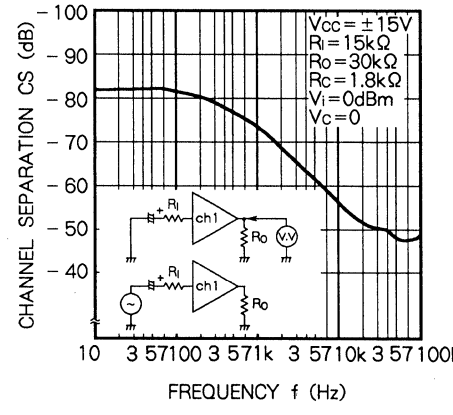
OUTPUT NOISE VOLTAGE VS. ATTENUATION



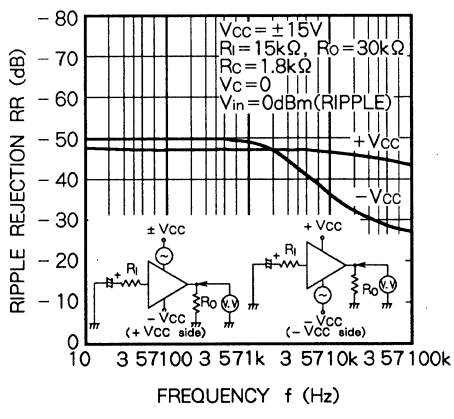
OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



CHANNEL SEPARATION VS. FREQUENCY



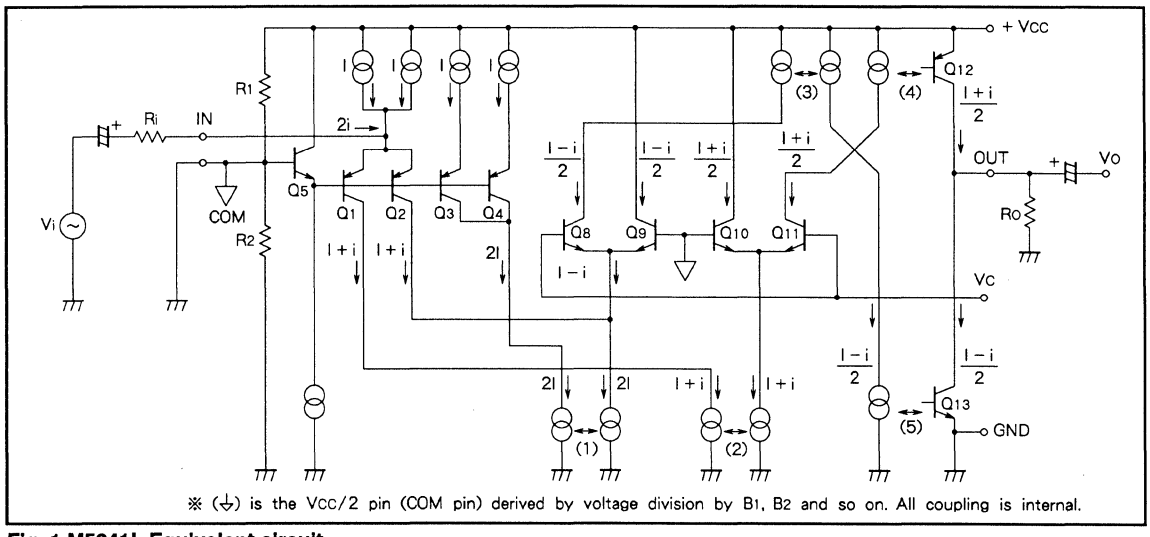
RIPPLE REJECTION VS. FREQUENCY



MITSUBISHI ELECTRIC

BASIC PRINCIPLE OF OPERATION

The M5241L is a current input, current output type of VCA IC. This amplifier uses the principle by which changing the balance of the differential circuit with external control voltage Vc will change gm. The circuit is also called a variable transconductance (variable gm) OP amp. The basic principle of operation will be simply explained below.



※ (⏚) is the Vcc/2 pin (COM pin) derived by voltage division by B1, B2 and so on. All coupling is internal.

Fig. 1 M5241L Equivalent circuit

Basic voltage-current conversion mechanism for input and output

Applying the input signal V_i which flows through external input resistor R_I results in a change to a current signal at input terminal IN. The V_{BE} level shift of Q_1, Q_2 and Q_5 will cause input pin IN to become ground level. The signal input in this way will be sent to the output pin as a current signal by the current mirror and differential circuit. By taking this current through the externally-connected output resistor (load resistor), the signal can go through a current-to-voltage conversion and be obtained as output signal V_O. The output transistors combine the currents by means of the joined PNP and NPN collector circuits. Basically, the DC potential floats and is not determined in this joining of currents. This is why one end of externally-connected resistor R_O is connected to ground and the DC level at the time of no signal is set.

Basic mechanism of attenuation

The output is controlled by means of changing the control voltage applied to the Vc pin with respect to the COM pin ($V_{CC}/2$ pin). By applying voltage from the COM pin to the base of one side of a differential circuit and applying voltage from the Vc pin to the other base, the current distribution of the differential circuit is changed and the gain of this circuit is changed.

Let us first consider when Vc equals zero (Vc − COM is shorted). Input signal V_i is converted to current by input resistor R_I and the i currents ($2i = V_i/R_I$) flow through the collectors of Q_1 and Q_2. When the current flowing in Q_i becomes I + i, the overall emitter current of the differential circuit consisting of Q_{10} and Q_{11} will also be determined as I + i by means of current mirror (2). Since the base potential of Q_{10} and Q_{11} is the same, the current will be divided equally and current (I + i) / 2 will flow in each of Q_{10} and Q_{11}. The current of current mirror (4) will also be determined as (I + i) / 2 because of this.

Since the current of current mirror (1) is determined as 2I by the current flowing in Q_3 and Q_4, the total of the current flowing in Q_2 and the current flowing in differential circuit Q_8, Q_9 will also be 2I. The current from Q_2 which will become I + i flows here and as a result, the overall emitter current of the differential circuit will be 2I − (I + i) = I − i. This current is devided the same way as in the differential circuit consisting of Q_{10} and Q_{11} with current (I − i) / 2 flowing in each of Q_8 and Q_9. From this, the current of current mirror (3) is determined as (I − i) / 2 and the current of current mirror (5) becomes (I + i) / 2.

Now, current (I − i) / 2 from current mirror (4) flows in transistor Q_{12} of the output stage. Since the current flowing in transistor Q_{13} from current mirror (5) is held at (I − i) / 2, connecting output resistor R_O between the output pin and the COM pin will result in current i flowing through R_O and providing a voltage signal $V_O = i \cdot R_O$.

Here, by selecting $R_O = 2R_I$, $V_O = i \cdot R_O = 2I \cdot R_I = V_I$ and the amplifier will have a gain of 1.

Next, we will consider case of when control voltage Vc is applied with regard to the selection of this resistance.

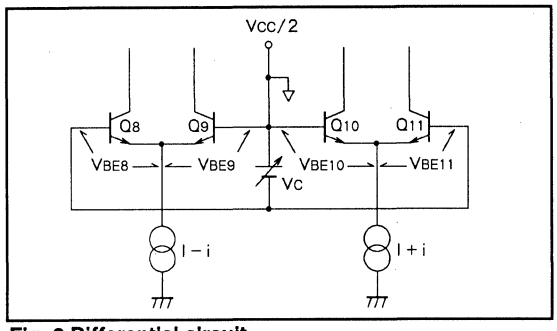


Fig. 2 Differential circuit

The values of V_{BE} of the differential stage will be as follows :

$$V_{BE8} \fallingdotseq \frac{kT}{q} \ln \left(\frac{I_{C8}}{I_S}\right)$$

$$V_{BE9} \fallingdotseq \frac{kT}{q} \ln \left(\frac{I_{C9}}{I_S}\right)$$

$$V_{BE10} \fallingdotseq \frac{kT}{q} \ln \left(\frac{I_{C10}}{I_S}\right)$$

$$V_{BE11} \fallingdotseq \frac{kT}{q} \ln \left(\frac{I_{C11}}{I_S}\right)$$

where, (I_S : the saturation current
k : the Boltzmann constant
q : the amount of electric charge on the electrons
T : the absolute temperature)

From this,

$$-V_C = V_{BE8} - V_{BE9} = \frac{kT}{q} \ln \left(\frac{I_{C8}}{I_{C9}}\right)$$

$$-V_C = V_{BE11} - V_{BE10} = \frac{kT}{q} \ln \left(\frac{I_{C11}}{I_{C10}}\right)$$

Here,

$$I_{C8} + I_{C9} \fallingdotseq I - i$$

$$I_{C10} + I_{C11} \fallingdotseq I + i$$

$$-V_C = \frac{kT}{q} \ln \frac{I_{C8}}{I - i - I_{C8}}$$

$$-V_C = \frac{kT}{q} \ln \frac{I_{C11}}{I + i - I_{C11}}$$

The current flowing through Q_8 and Q_{11} will be

$$I_{C8} = \frac{(I - i)\exp(-\frac{q}{kT}V_C)}{1 + \exp(-\frac{q}{kT}V_C)} = \frac{I - i}{1 + \exp(-\frac{q}{kT}V_C)}$$

$$I_{C11} = \frac{(I + i)\exp(-\frac{q}{kT}V_C)}{1 + \exp(-\frac{q}{kT}V_C)} = \frac{I + i}{1 + \exp(-\frac{q}{kT}V_C)}$$

Current I_{C11} is the current of current mirror (4), and I_{C8} will be the same as the current of current mirror (5).

At this time, the current that will flow through the output pin will be the same as that in the explanation when V_C was equal to zero, and is expressed as

$$i_o = \frac{2i}{1 + \exp(\frac{q}{kT} \cdot V_C)}$$

The gain will be

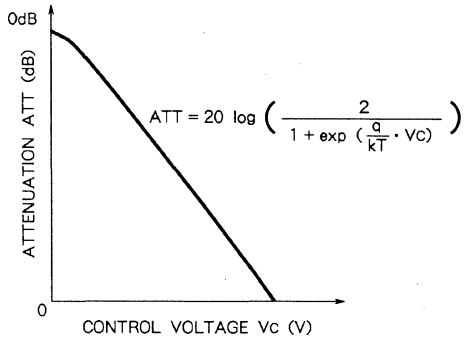
$$\frac{V_o}{V_i} = \frac{i_o \cdot R_o}{2i \cdot R_i} = \frac{2}{1 + \exp(\frac{q}{kT} \cdot V_C)}$$

and when calculated in dB,

$$ATT = 20 \log \left(\frac{2}{1 + \exp(\frac{q}{kT} \cdot V_C)}\right)$$

As in the graph below, the attenuation will change logarithmically with respect to the change of V_C.

ATTENUATION VS. CONTROL VOLTAGE



Setting and connection of input/output resistance

As explained above, the input signal is converted to current, but since the transistor of the input stage is biased at a fixed current ($I \fallingdotseq 170\ \mu A$ when $R_C = 1.8k\Omega$), the maximum value of the input current is determined at the least upper bound of I (Fig. 3). Accordingly, when a large signal is input, it is necessary to decrease the value of bias-control resistor R_C, select a large input/output resistance and decrease the input current. Note that decreasing the value of bias-control resistor R_C and increasing the input/output resistance will change the characteristic of the noise distortion factor, so set the values to suit the specific application.
(See characteristic curve)

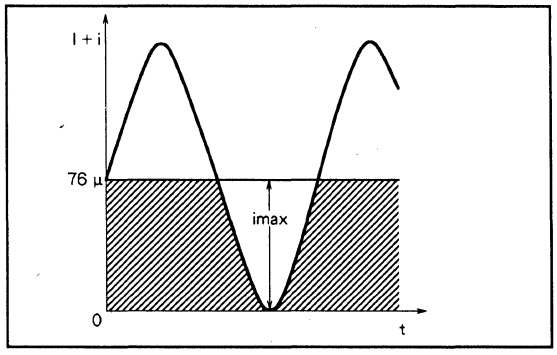


Fig. 3 Maximum current signal

MITSUBISHI ELECTRIC

Since the voltage gain (amount of attenuation) is determined by load resistor Ro through which the output current is taken, the value of the input impedance connected to the next stage is sometimes affected. (Placing Zi in parallel with Ro will lower the impedance.) Generally, a buffer amplifier composed of a transistor or OP amp is connected as shown in Fig. 4 (b).

The basic principle of operation on the 2-way power supply system has been explained thus far. Note that it is necessary to set COM pin (Vcc/2) to ground level by means of capacitor Co when a single power supply is used.

For operation on a single power supply, see the basic principle of operation for M5222. For connection, see application examples.

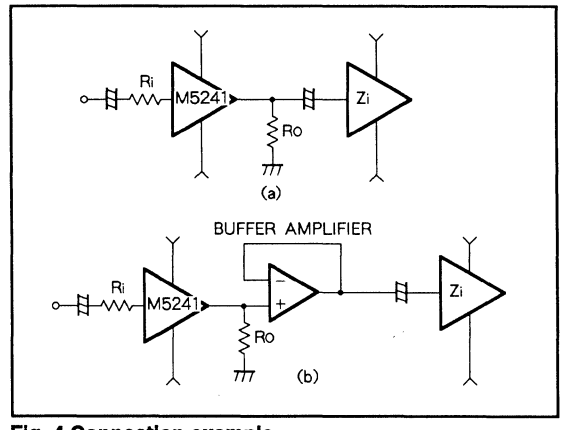
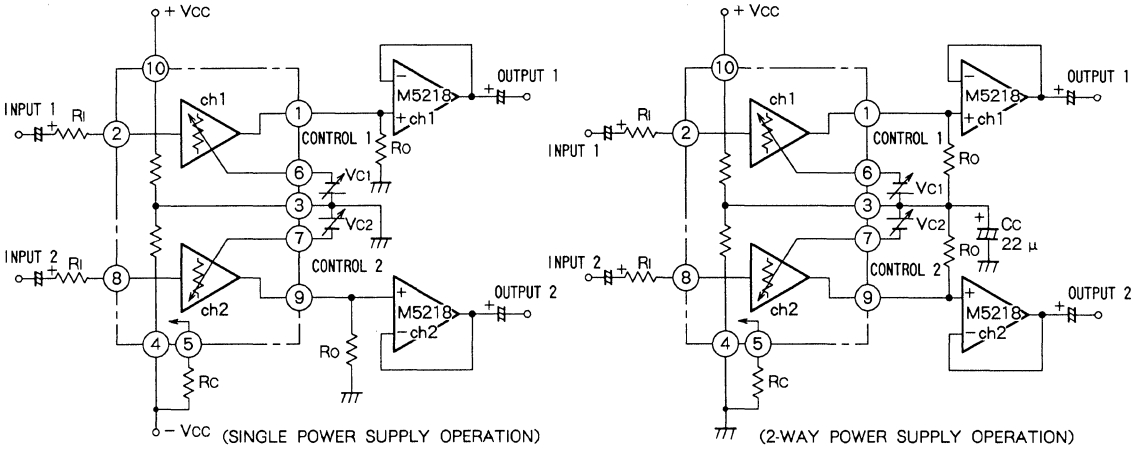


Fig. 4 Connection example

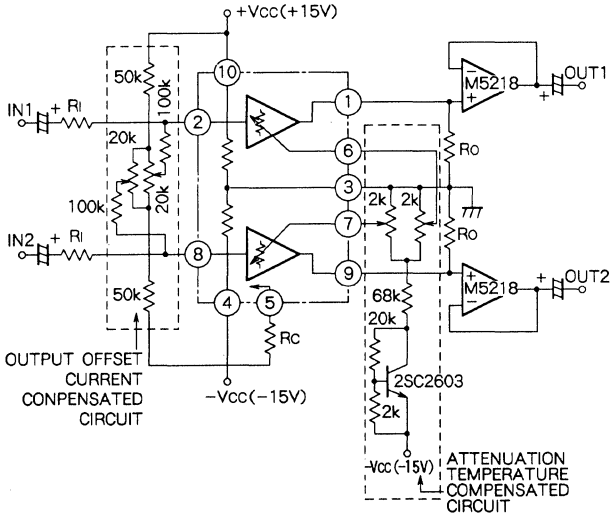
APPLICATION CIRCUIT

(1) TYPICAL APPLICATION EXAMPLE

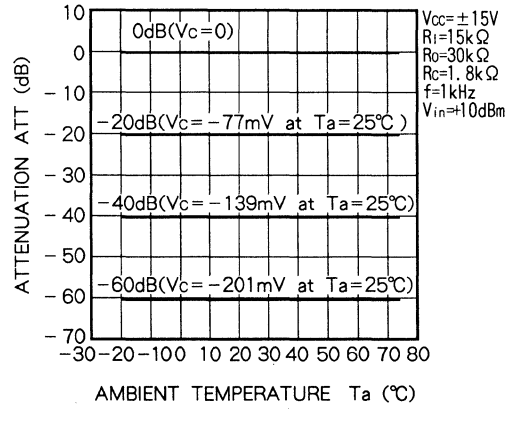


* When Vc = 0V, attenuation of 0dB is obtained by selecting Ro = 2R1.

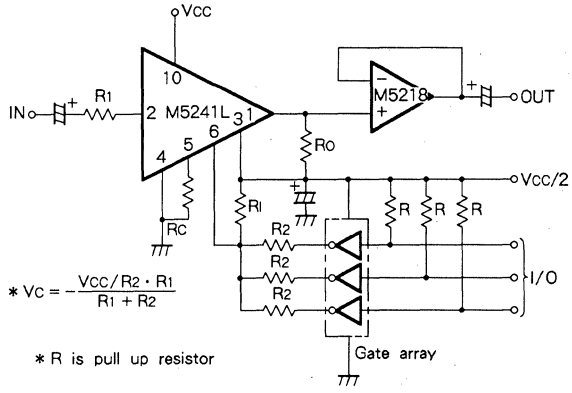
(2) TEMPERATURE COMPENSATED, OUTPUT OFFSET COMPESATED CIRCUITS



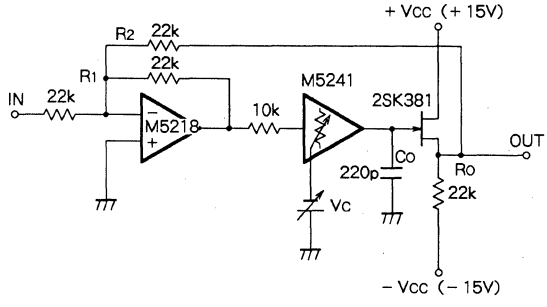
ATTENUATION VS. AMBIENT TEMPERATURE (TEMPERATURE COMPENSATED)



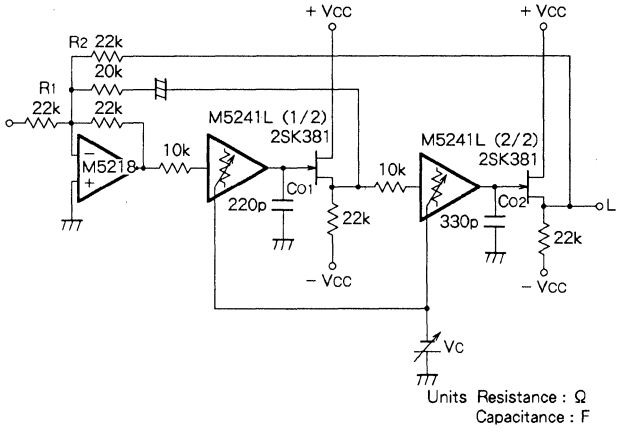
PROGRAMMABLE ATTENUATION CIRCUIT



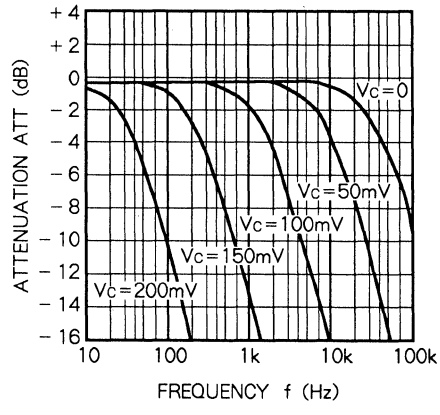
VCF(FIRST-ORDER LOW-PASS FILTER)



VCF(SECOND-ORDER LOW-PASS FILTER)

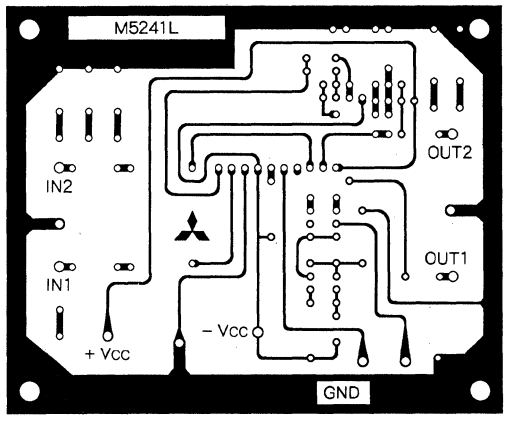


ATTENUATION VS. FREQUENCY RESPONSE (FIRST-ORDER LOW-PASS FILTER)

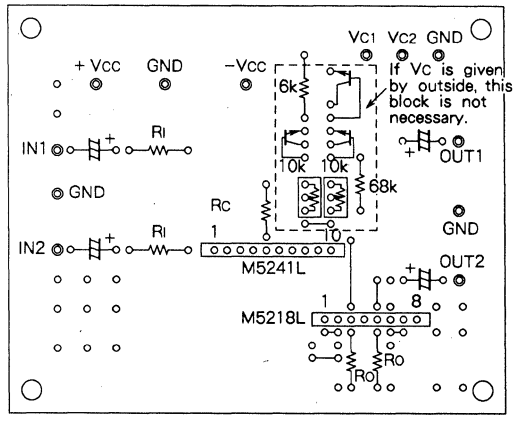


PRINTED CIRCUIT BOARD FOR CIRCUIT TESTING

PC BOARD PARTS-PLACEMENT DIAGRAM (COPPER FOIL SIDE)



PC BOARD PARTS-PLACEMENT DIAGRAM (PARTS SIDE)



MITSUBISHI ELECTRIC

M5282FP

ELECTRONIC VOLUME CONTROL WITH MICROPHONE AMPLIFIER

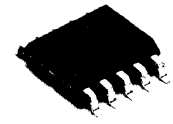
DESCRIPTION

The M5282FP is an optimum IC for fade-in/fade-out control of video camera's input voice signals. The IC containes a linear-control VCA and low-noise OP amp.

Its applications cover general audio equipment and electronic musical instruments, such as voice volume controls in video cameras and 8mm cameras.

FEATURES

- Efficient VCA and OP amp are provided independently
- Voltage input/output type VCA
- Voltage gain can be set externally (OP amp section)
- Large ATT range ..... 0dB ~ − 82dB
- Built-in Vcc/2 bias terminal
- Can operate with low voltage (Vcc = 4.8V)



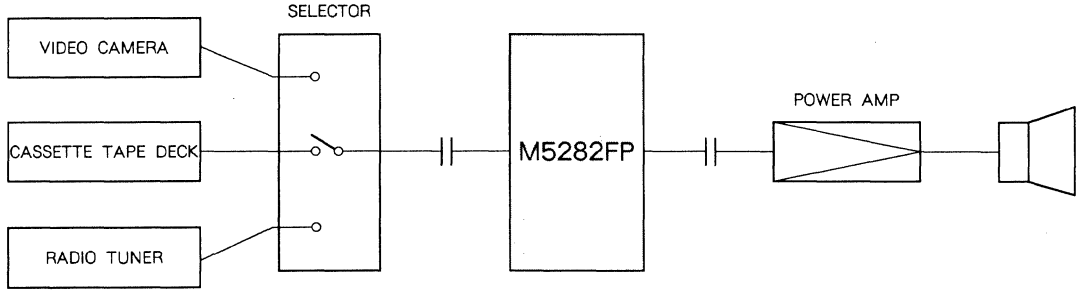
Outline 10P2-C

1.27mm pitch 300mil SOP
(5.3mm × 6.13mm × 1.75mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... Vcc = 4.6 ~ 15V

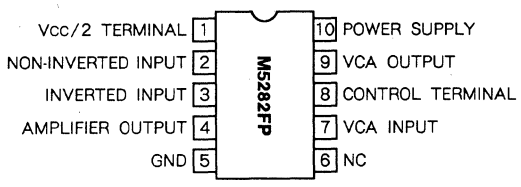
SYSTEM CONFIGURATION



M5282FP

ELECTRONIC VOLUME CONTROL WITH MICROPHONE AMPLIFIER

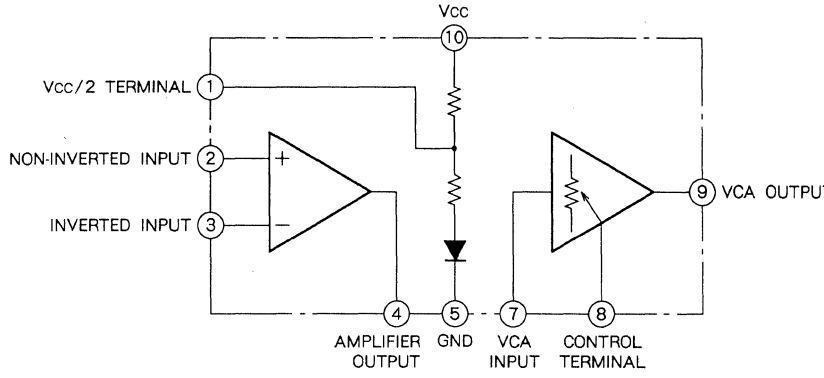
PIN CONFIGURATION



Outline 10P2-C

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin No.	Name	Symbol	Function
①	Vcc/2	Vcc/2 (COM)	Vcc/2 is obtained in the IC using divided voltage and is output to terminal ①. This can be used for the mid-point potential setup in the mike amplifier.
②	Mike amplifier non-inverted input	Amp + IN	This is the non-inverted input terminal of the mike amplifier. The mike amplifier's mid-point potenial is determined by connecting this terminal to terminal ① (Vcc/2 terminal) via a resistor (about 47kΩ). If you use this IC as a non-inverted amplifier, enter signals into this terminal. About 120nA (typ.) will be output from the IC as the input bias current.
③	Mike amplifier inverted input	Amp − IN	This is the output terminal of the mike amplifier. The feedback is applied from output terminal ④ of the mike amplifier to this terminal. The gain will be determined by the constant between this terminal and the output. About 120nA (typ.) will be output from the IC as the input bias current.
④	Mike amplifier output	Amp OUT	This is the output terminal of the mike amplifier. Input signals (having been set externally and arbitrary) whose gain has been doubled are output to this terminal.
⑤	Connected	GND	This is the GND terminal with the lowest IC. When you use this terminal, connect it to the ground.
⑥	Not connected	NC	This terminal is left open.
⑦	VCA input	VCA IN	VCA input terminal. If signals are input to this terminal from the mike amplifier's output, use a coupling capacitor (DC cutting capacitor).
⑧	Control	Vc	VCA control terminal. VCA output can be changed by applying DC voltage to this terminal. About 400nA of bias current is required for this terminal.
⑨	VCA output	VCA OUT	VCA output terminal
⑩	Power supply	Vcc	Power supply terminal at the HIGH side.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	15	V
P_d	Power dissipation	440	mW
K_θ	Thermal derating ($T_a \geqq 25℃$)	4.40	mW/℃
T_{opr}	Operating temperature	− 20 ~ + 75	℃
T_{stg}	Storage temperature	− 40 ~ + 125	℃

ELECTRICAL CHARACTERISTICS

ELECTRIC VOLUME (VCA) CHARACTERISTICS (V_{CC} = 4.8V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
ATT	Attenuation error	V_C = 4.8V, V_I = − 10dBm, f = 1kHz	− 2.0	− 0.3	+ 2.0	dB
ATT_M	Maximum attenuation	V_C = 0V, V_I = − 10dBm, f = 1kHz	− 77	− 82	−	dB
V_{IM}	Maximum input voltage	f = 1kHz, THD = 0.2%, V_C = 4.8V	0.6	0.7	−	Vrms
THD	Total harmonic distortion	f = 1kHz, V_O = 0.5Vrms, V_C = 4.8V	−	0.06	0.2	%
V_{NO}	Output noise voltage	Rg = 0, V_C = 4.8V	−	19	50	μ Vrms

MIKE AMPLIFIER CHARACTERISTICS (V_{CC} = 4.8V, V_C = 4.8V, Ta = 25℃, 40dB Amp., unless otherwise noted)

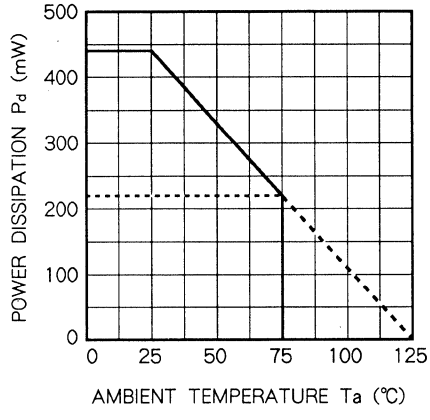
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OM}	Maximum output voltage	THD = 0.2%	0.6	0.7	−	Vrms
THD	Total harmonic distortion	V_O = 0.5Vrms, f = 1kHz	−	0.01	0.2	%
V_{IN}	Input referred noise voltage	Rg = 1kΩ	−	0.5	1.0	μ Vrms

TOTAL (VCA+MIKE AMP.) CHARACTERISTICS (V_{CC} = 4.8V, Ta = 25℃, unless noted)

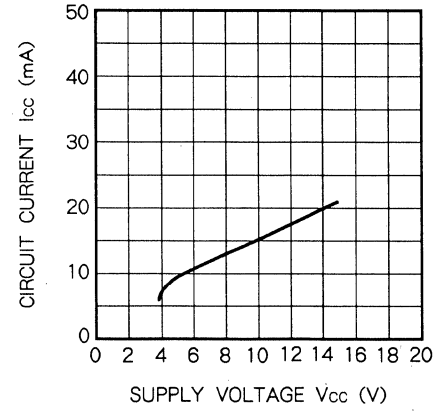
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	V_{IN} = 0	–	8.7	13.0	mA
V_{OM}	Maximum output voltage	f = 1kHz, THD = 0.2%	0.6	0.7	–	Vrms
THD	Total harmonic distortion	f = 1kHz, V_O = 0.5Vrms	–	0.06	0.2	%
V_{NO}	Output noise voltage	R_g = 1kΩ	–	60	120	μ Vrms
S/N	Signal to noise voltage (1)	R_g = 1kΩ, V_i = 3.5mVrms	69	75	–	dB
S/N	Signal to noise voltage (2)	R_g = 1kΩ, V_i = 0.3mVrms	48	54	–	dB

TYPICAL CHARACTERISTICS

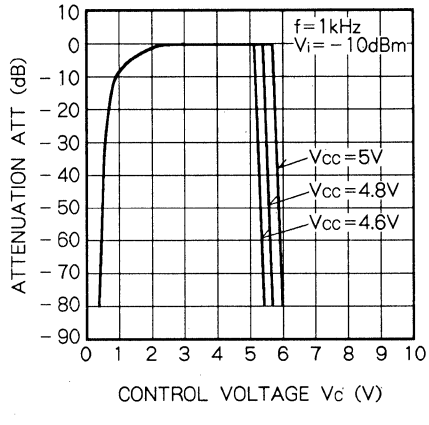
THERMAL DERATING (MAXIMUM RATING)



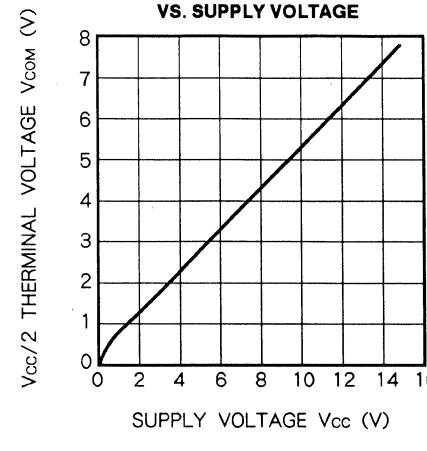
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



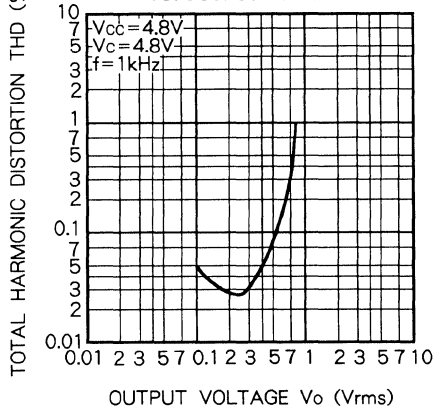
ATTENUATION VS. CONTROL VOLTAGE



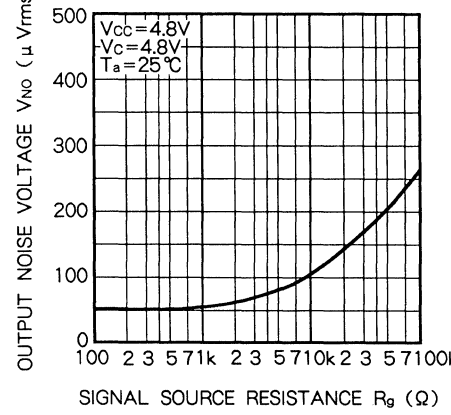
Vcc/2 THERMINAL VOLTAGE VS. SUPPLY VOLTAGE



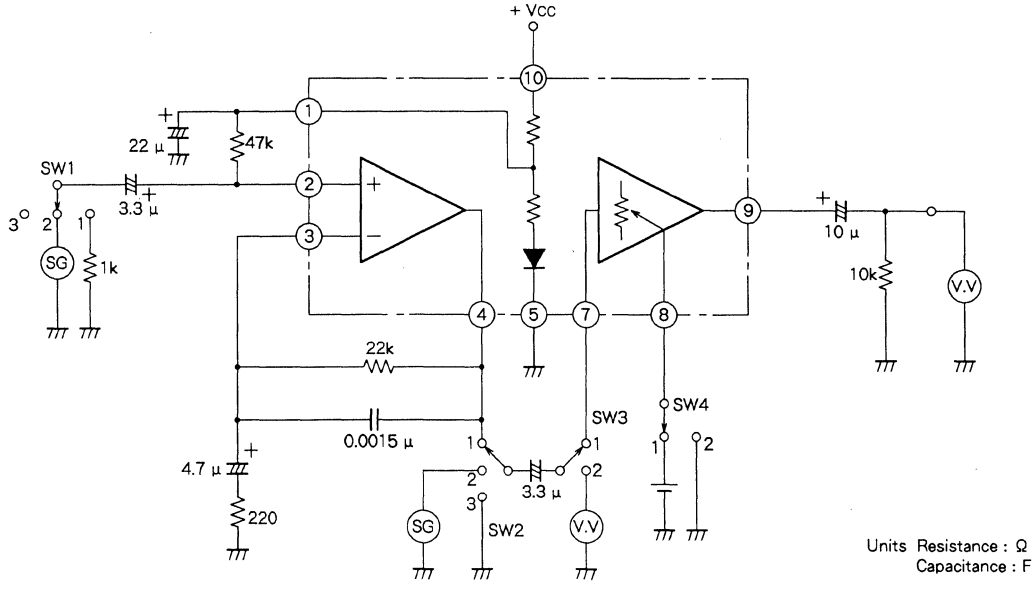
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



OUTPUT NOISE VOLTAGE VS. SIGNAL SOURCE RESISTANCE



TEST CIRCUIT



Units Resistance : Ω
Capacitance : F

Switch matrix electronic volume (VCA) chracteristics

	SW1	SW2	SW3	SW4
ATT	1	2	1	1
ATT_M	1	2	1	2
V_{OM}	1	2	1	1
THD	1	2	1	1
V_{NO}	1	3	1	1

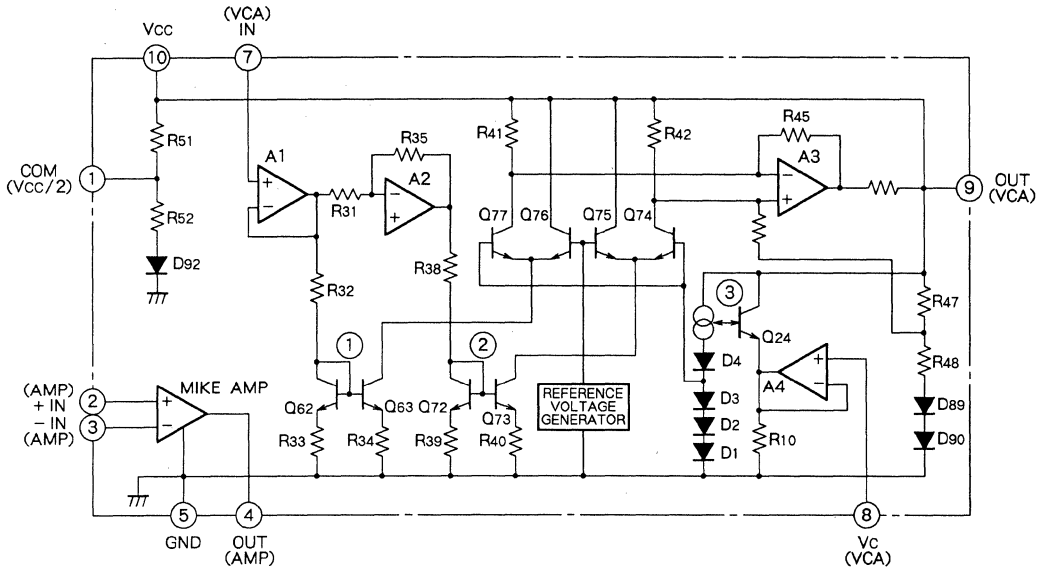
Mike amplifier chracteristics

	SW1	SW2	SW3	SW4
V_{OM}	2	1	2	1
THD	2	1	2	1
V_{NO}	1	1	2	1

TOTAL (VCA+Mike Amp.) Chracteristics

	SW1	SW2	SW3	SW4
I_{CC}	3	1	1	1
V_{OM}	2	1	1	1
THD	2	1	1	1
V_{NO}	1	1	1	1

DESCRIPTION OF OPERATIONS (BLOCK DIAGRAM)



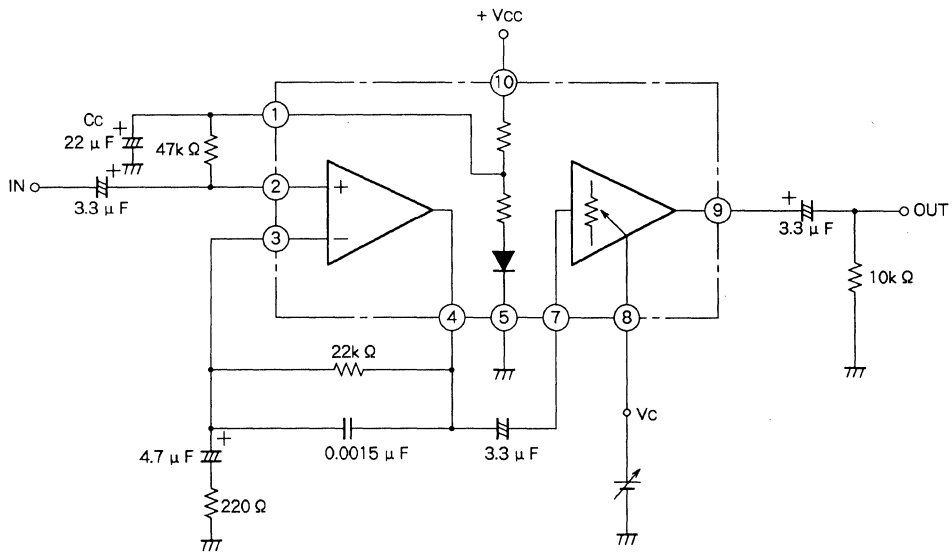
This section shows the basic block diagram of the M5282FP and descrides its operations.

Input signals from the VCA (terminal ⑦) flow via the buffer amplifier A_1 and are converted to in-phase current signals by R_{32}. Also, the input voltage which has been inverted by the input amplifier A_2 is converted into current signals by R_{36}. These signals are sent to the differential circuits (consisting of Q_{74} to Q_{77}) by current mirrors ① and ②.

Collectors of Q_{74} and Q_{77} in the differential circuit are connected to the next differential amplifier's + and − inputs, respectively. The potential of Q_{74} collector is determined by the current sent from current mirrors of Q_{72} and Q_{73} and resistor R_{42}. The potential of Q_{77} collector becomes the same due to the differential amplifier A_3 and the same current flows into R_{41} and R_{42}. Current signals sent to differential circuits Q_{77} and Q_{76} are antiphase, resulting in the difference between the current of R_{41} and that of collector Q_{77}. This will be voltage converted by the differential amplifier A_3 to be output.

The DC potential of the V_C terminal is given to R_{10} by the buffer amplifier A_4, converted into the current, and sent to D_1 to D_3 by the current mirror ③. The $VF = kT/q \cdot \ln IF/IS$) for this current is generated and given to the base of Q_{74} and Q_{77}. By changing the balance of differential circuits Q_{74}, Q_{75}, Q_{76} and Q_{77}, the attenuation chracteristics can be obtained because the gm changes.

APPLICATION EXAMPLE



NOTE ON USAGE

1. 0dB and one time of amplification are obtained while internal differential circuits are gathered to the Q_{77} and Q_{74} side (see the OPERATING DESCRIPTION BLOCK DIAGRAM) on the VCA section (control voltage is about 3V, see the ATTENUATION VS. CONTROL VOLTAGE graph).
2. Signal phase input to VCA IN is output to VCA OUT.
3. Although the control voltage can be given in the range of 0 to Vcc, the voltage needed for the attenuation change is from 0.5V to 3V (see the ATTENUATION VS. CONTROL VOLTAGE). Therefore, it is recommended that the IC be used within the range of 0V to 5V.
4. About 400nA (typ) of bias current is needed for the control terminal.
5. The Vcc/2 terminal level-shifts the VF of the diode to cancel out the unbalance the left voltages of the up- and down-side mike amplifiers.
6. To decrease the impedance of the COM terminal (Vcc/2 terminal), connect the capacitor Cc between the COM AND GND terminals.

M5283P

DUAL VCA IC FOR Hi-Fi ELECTRONIC VOLUME CONTROL

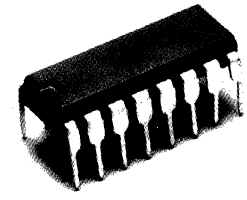
DESCRIPTION

The M5283P has 2 channels of built-in high-performance VCA designed to produce a wide dynamic range, low distortion ratio, and high S/N ratio.

The IC is an optimum device for Hi-Fi stereo sets, cassette tape recoders, Hi-Fi TV sets, VCR, and electronic musical instruments.

FEATURES

- Low distortion ····· THD = 0.003 % (V_O = 1 Vrms)
- Independent control terminal
- 2 channels of VCA are built-in
  ch1 and ch2 can be controlled separately by Vc control
- Maximum input voltage is large ····· V_i = 7Vrms
  (when THD = 1 %)
- Large ATT range ····· 0 ~ − 90dB
- S/N (dynamic range) is large ····· 85dB
  (V_i = 150mVrms · IHF-A filter)



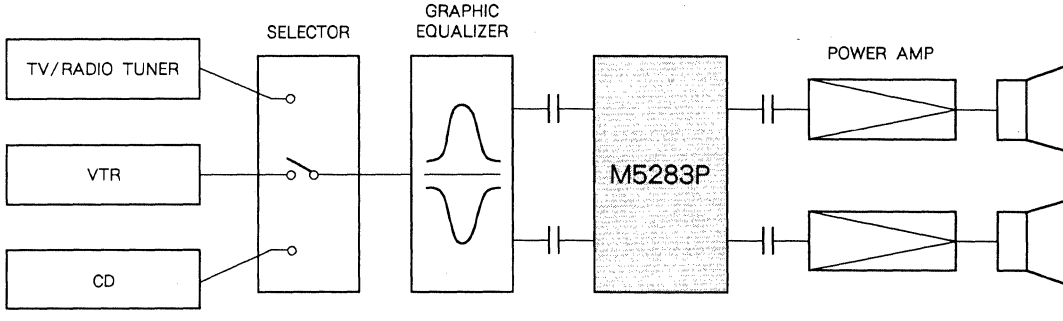
Outline 16P4

2.54mm pitch 300mil DIP
(6.3mm × 19.0mm × 3.3mm)

RECOMMENDED OPERATING CONDITION

Supply voltage range ····· V_{CC}, V_{EE} = ± 7 ~ ± 16V

SYSTEM CONFIGURATION

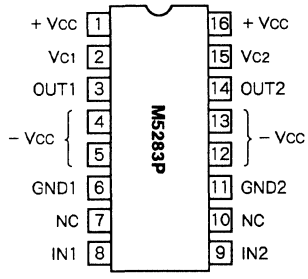


MITSUBISHI ELECTRIC

M5283P

DUAL VCA IC FOR Hi-Fi ELECTRONIC VOLUME CONTROL

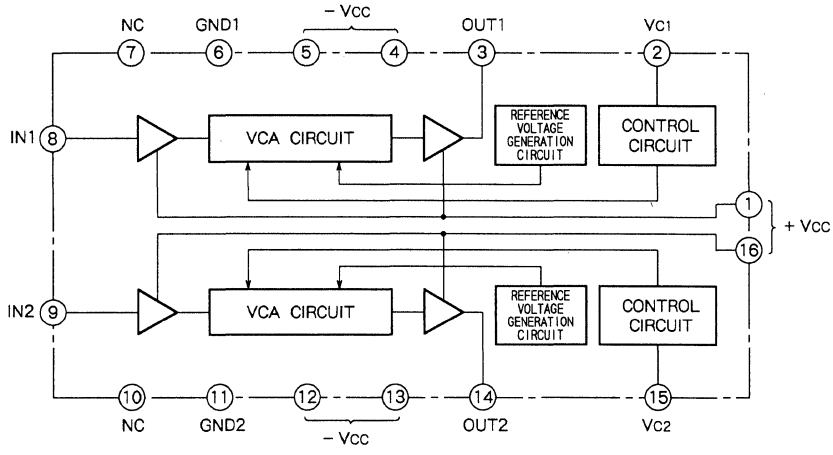
PIN CONFIGURATION



Outline 16P4

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Name	Symbol	Function
①	(+) power terminal on ch1 side	(+)Vcc	This is (+) supply voltage terminal on ch1 side. Connect to pin ⑯ externally.
②	ch1 control	Vc1	It controls signal on ch1 side. It controls signal by providing this terminal with voltage of 0~5V. Approximately 25nA (TYP) is necessary as bias current.
③	ch1 output	OUT1	This is an output terminal on ch1 side.
④	(−) power	(−)Vcc	pin ④, pin ⑤, pin ⑫ and pin ⑬ are connected internally. Add copper film for radiation at the foot of these pins for use.
⑤			
⑥	ch1 ground	GND1	This is a ground terminal on ch1 side. Connect to GND2 (pin ⑪) externally. Connect to GND wiring.
⑦	Not connected	NC	This terminal is kept OPEN.
⑧	ch1 input	IN1	This is an input terminal on ch1 side. Insert a resistor of approximately 47k~100k Ω between GND and this input terminal (pin ⑧) for DC bias.
⑨	ch2 input	IN2	This is an input terminal on ch2 side. Insert a resistor of approximately 47k~100k Ω between GND and this input terminal (pin ⑨) for DC bias.
⑩	Not connected	NC	This terminal is kept OPEN.
⑪	ch2 ground	GND2	This is a ground terminal on ch2 side. Connect to GND1 (pin ⑥) externally. Connect to GND wiring.
⑫	(−) power	(−)Vcc	pin ④, pin ⑤, pin ⑫ and pin ⑬ are connected internally. Add copper film for radiation at the foot of these pins for use.
⑬			
⑭	ch2 output	OUT2	This is an output terminal on ch2 side.
⑮	ch2 control	Vc2	It controls signal on ch2 side. It controls signal by providing this terminal with voltage of 0~5V. Approximately 25nA (TYP) is necessary as bias current.
⑯	(+) power terminal on ch2 side	(+)Vcc	This is (+) supply voltage terminal on ch2 side. Connect to pin ① externally.

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
Vcc	Supply voltage	± 18	V
Pd	Power dissipation (Ta = 25℃)	2.0 **	W
Vc	Control voltage	0~Vcc − 1.5	V
Topr	Operating temperature	−20~+75	℃
Tstg	Storage temperature	−40~+125	℃

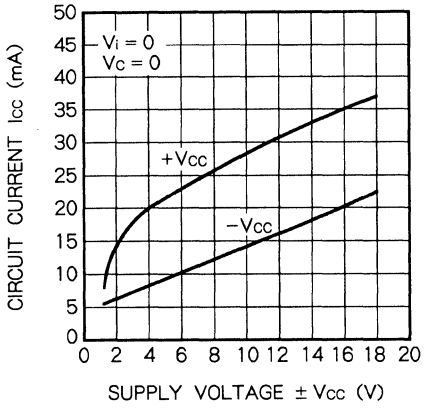
** : Add copper film of 400mm²

ELECTRICAL CHARACTERISTICS (Vcc = ± 15V, Vc = 5V, Ta = 25℃, unless otherwise noted)

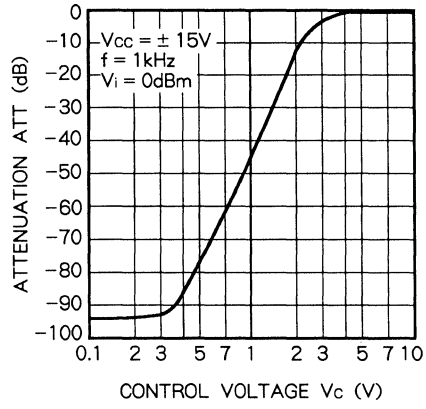
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Icc	Circuit current	Vi = 0	−	34	50	mA
VOM	Maximum output voltage	Vc = 5V, THD = 1 %, f = 1kHz, RL = 10k Ω	4	5	−	Vrms
VIM	Maximum input voltage	Vc = 3V, THD = 1 %, f = 1kHz	6	7	−	Vrms
ATT	Attenuation error	Vc = 5V, Vi = 0dBm, f = 1kHz	− 2.3	− 0.3	+ 1.7	dB
Δ ATT	Attenuation deviation between channels	Vc = 5V, Vi = 0dBm, f = 1kHz	−	± 0.1	± 3.0	dB
ATTM	Maximum attenuation	Vc = 0V, Vi = 0dBm, f = 1kHz	80	95	−	dB
THD	Total harmonic distortion	f = 1kHz, Vo = 1Vrms, Vc = 5V	−	0.003	0.05	%
CS	Channel separation	f = 1kHz, Vc = 5V, Vi = 0dBm	−	85	−	dB
VNO	Output noise voltage	Rg = 0, Vc = 5V, IHF-A FILTER	−	6.5	30	μVrms
Ivc	Control bias current	Vi = 0, Vc = 5V	−	25	500	nA

TYPICAL CHARACTERISTICS

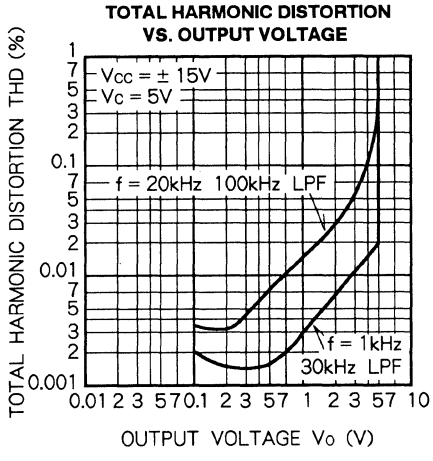
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



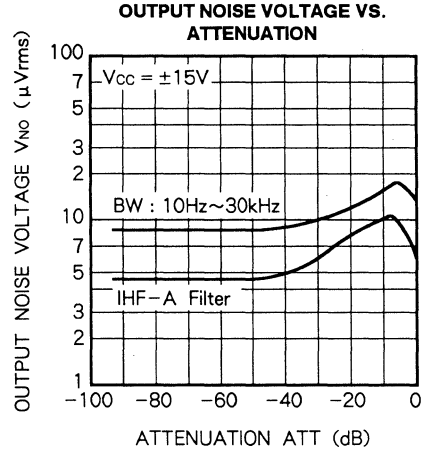
ATTENUATION VS. CONTROL VOLTAGE



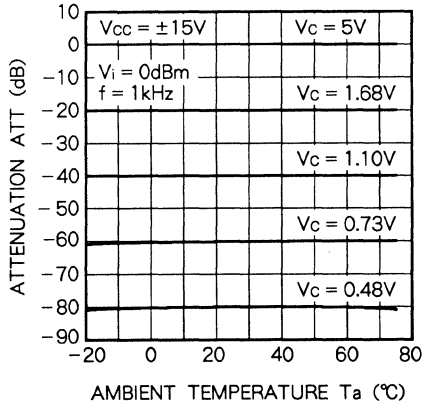
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



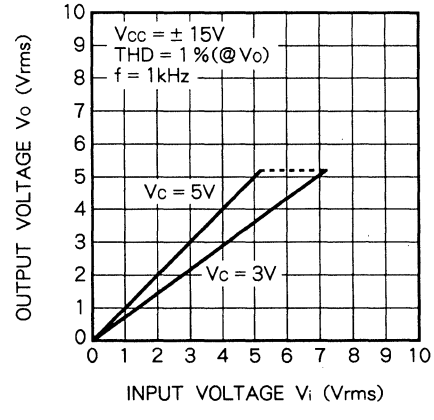
OUTPUT NOISE VOLTAGE VS. ATTENUATION



ATTENUATION VS. AMBIENT TEMPERATURE



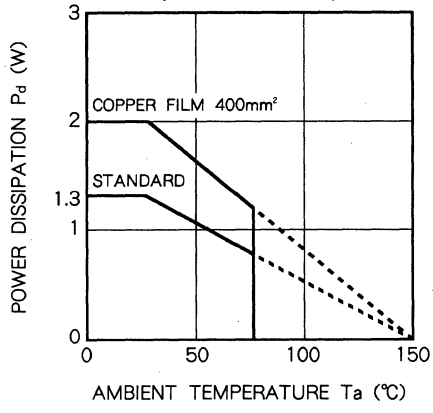
OUTPUT VOLTAGE VS. INPUT VOLTAGE



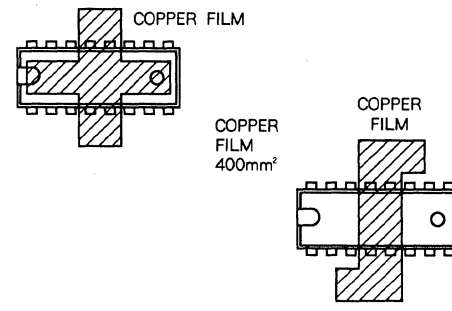
NOTES

(Note 1) **Radiation**

THERMAL DERATING (MAXIMUM RATING)



Example of layout of PC board



Circuit current for M5283P is large to improve various characteristics such as total harmonic distortion and noise voltage.(typ = 34mA). It consumes, therefore, large power and it is necessary to take thermal deration into consideration in layout of PC board. Add copper film as widely as possible at the foot of − Vcc terminal to improve radiation (thermal diffusion) of IC.

Power dissipation Pd becomes 1.3W when copper film cannot be added widely to improve radiation or when copper film for radiation cannot be applied. Calculate maximum power by ± Vcc × Iccmax and take ambient temperature and Vcc applied voltage into consideration for use within the above limit of Pd.

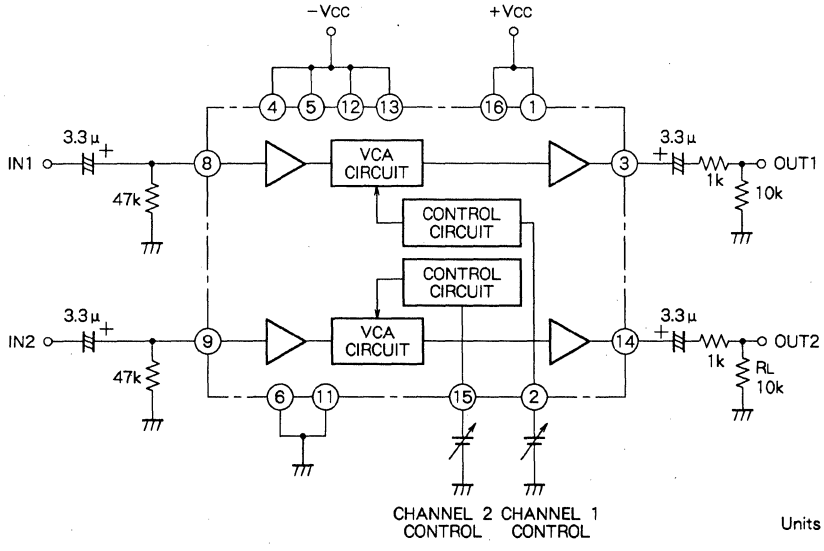
(Note 2) + Vcc terminal pin ①, pin ⑯, and GND terminal pin ⑥, pin ⑪ are not connected internally. Connect them externally before use.

(Note 3) Control terminal (pin ②, pin ⑮) sinks approximately 25nA (typ) of bias current.

(Note 4) M5283P becomes 0dB and one time amplifier when + 5V is applied to the control terminal (pin ②, pin ⑮). Signal attenuates by decreasing the voltage of control terminal.

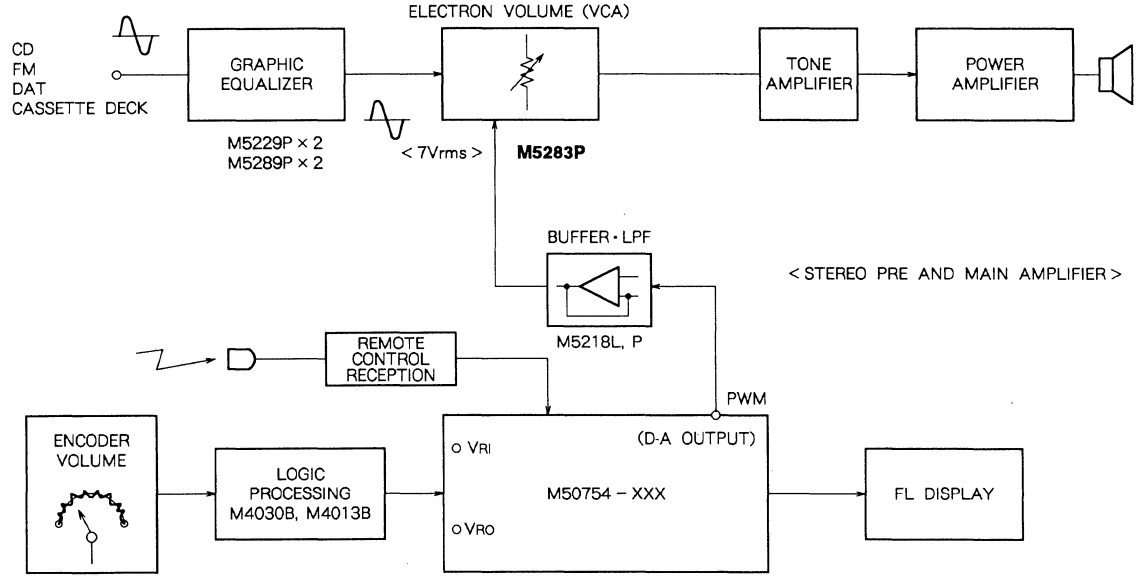
(Note 5) Input signal is output to the output terminal with equal phase.

Example of application circuit



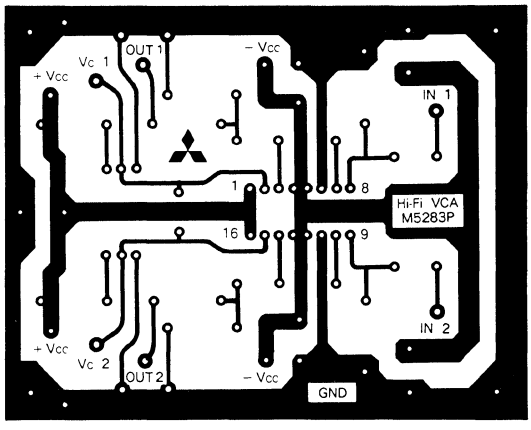
Units Resistance : Ω
Capacitance : F

Application block diagram

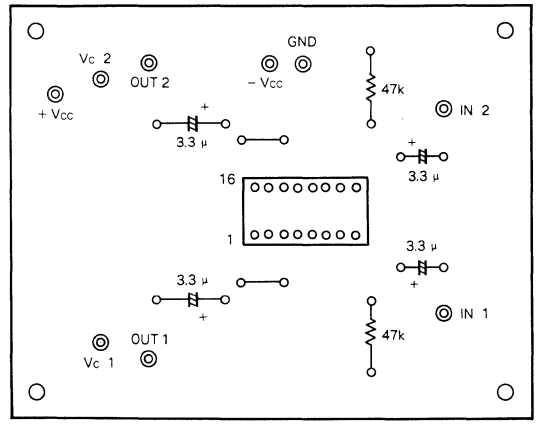


PC BOARD FOR CIRCUIT EXPERIMENT

PC BOARD WIRING DIAGRAM
(ON COPPER FILM SIDE)



(ON THE SIDE OF PARTS INSERTION)



M5226P,FP

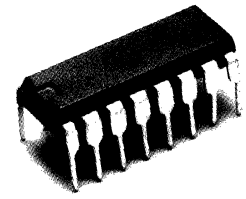
5-ELEMENT GRAPHIC EQUALIZER IC

DESCRIPTION

The M5226 is a 5-element graphic equalizer IC best suited to audio systems. It has a built-in 5-element resonance circuits with transistor system and an output OP amp. The IC can be used in hybrid ICs and compact sets of high-density assemblies. Its applications include radio cassette tape players, car audio systems, and music centers.

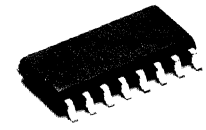
FEATURES

- The number of part can be reduced drastically for compact size.
- Graphic equalizer can be easily composed
- Low distortion ..... THD = 0.02% (typ)
  @ Flat input short
- Low noise ..... V_{NO} = 5μVrms (typ)
  @ f = 1kHz, Flat
- Large allowable input voltage ..... V_i = 2.3Vrms (typ)
  @ V_{CC} = 9V, f = 1kHz, Flat



Outline 16P4(P)

2.54mm pitch 300mil DIP
(6.3mm × 19.0mm × 3.3mm)



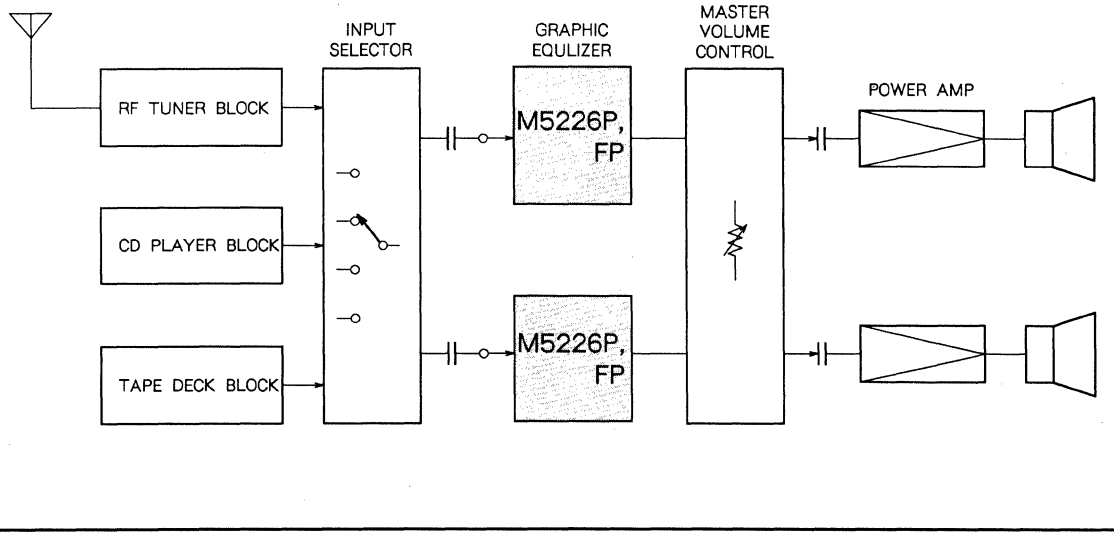
Outline 16P2S-A(FP)

1.27mm pitch 225mil SOP
(4.4mm × 10.0mm × 1.5mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 4~20V
Rated supply voltage ..... V_{CC} = 20V
Rated power dissipation ..... 700mW (P)
550mW(FP)

SYSTEM CONFIGURATION

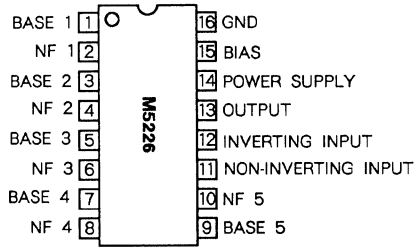


MITSUBISHI ELECTRIC

M5226P,FP

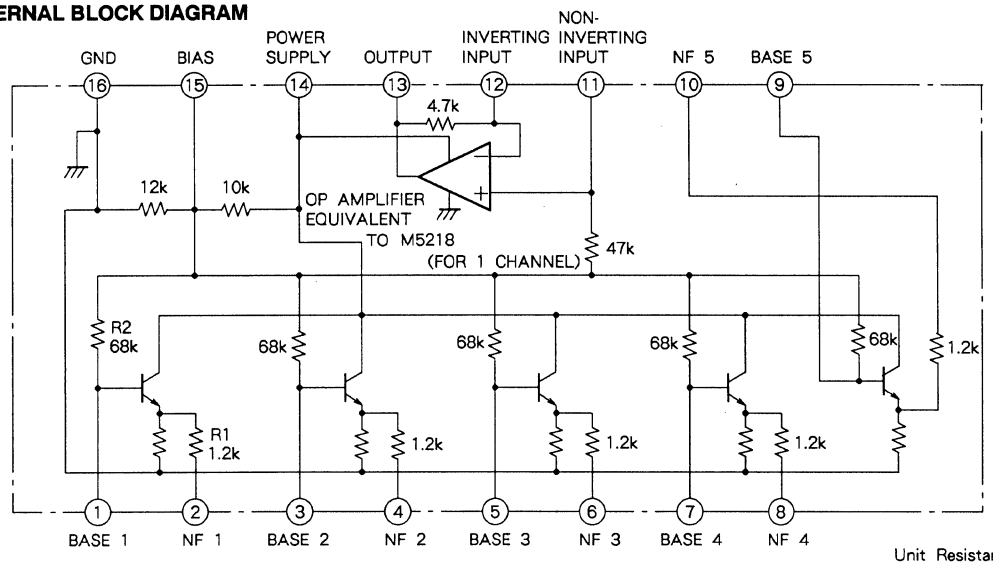
5-ELEMENT GRAPHIC EQUALIZER IC

PIN CONFIGURATION



Outline 16P4(P)
16P2S-A(FP)

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

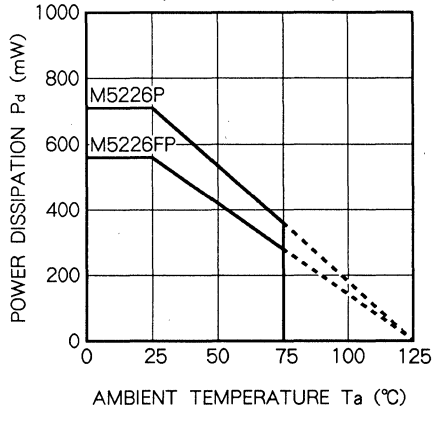
Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	20	V
I_{LP}	Load current	30	mA
P_d	Power dissipation	550(FP)/1000(DIP)	mW
T_{opr}	Operating temperature	−20～+75	℃
T_{stg}	Storage temperature	−55～+125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 9V)

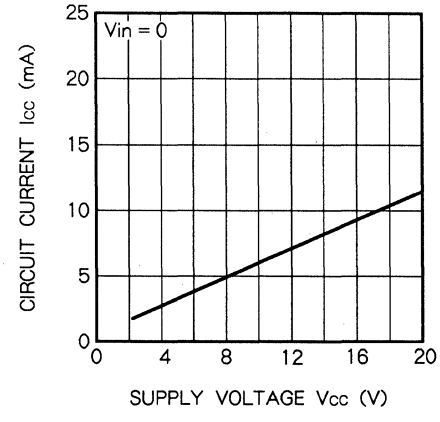
Symbol	Parameter		f (Hz)	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
I_{CC}	Circuit current		−	V_{in} = 0	3.0	5.2	8.0	mA
$G_{V(FLAT)}$	Voltage gain	Flat	1k	V_{in} = −10dBm	−3.8	−0.8	+2.2	dB
$G_{V(BOOST)}$	Voltage gain	Boost	108	V_{in} = −10dBm	7.2	9.7	11.2	dB
			343		7.2	9.7	11.2	
			1.08k		7.2	9.7	11.2	
			3.43k		7.2	9.7	11.2	
			10.8k		7.2	9.7	11.2	
$G_{V(CUT)}$	Voltage gain	Cut	108	V_{in} = −10dBm	−12.8	−11.3	−8.8	dB
			343		−12.8	−11.3	−8.8	
			1.08k		−12.8	−11.3	−8.8	
			3.43k		−12.8	−11.3	−8.8	
			10.8k		−12.8	−11.3	−8.8	
THD	Total harmonic distortion		1k	V_{in} = 1Vrms	−	0.02	0.1	%
V_{NO}	Output noise voltage		Input short BW : 10Hz～30kHz (3dB) flat		−	5.0	20	μVrms

TYPICAL CHARACTERISTICS

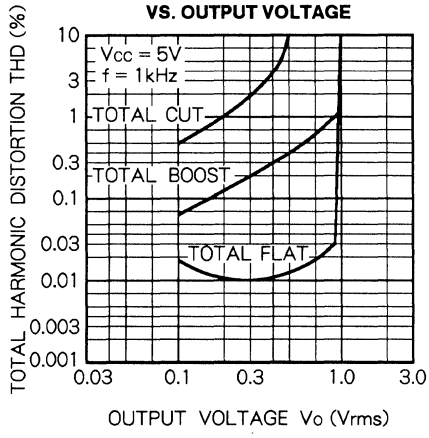
THERMAL DERATING (MAXIMUM RATING)



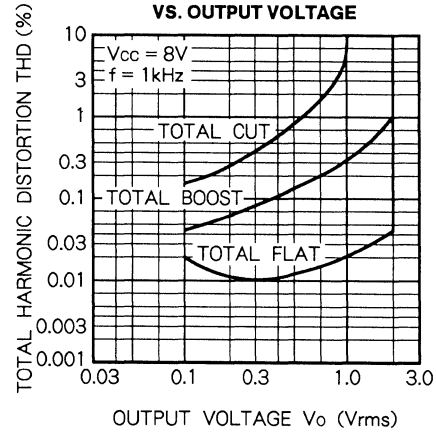
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



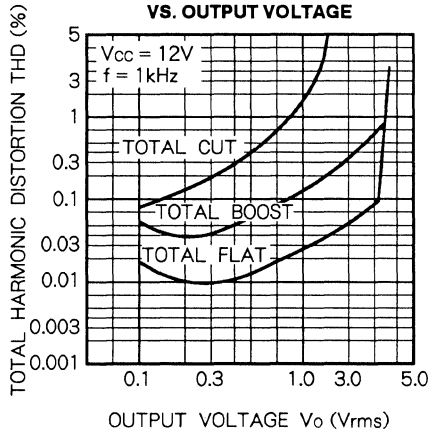
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



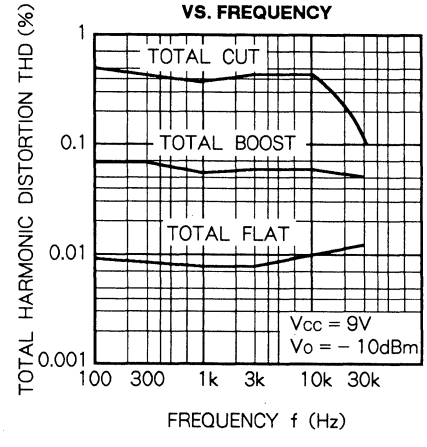
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



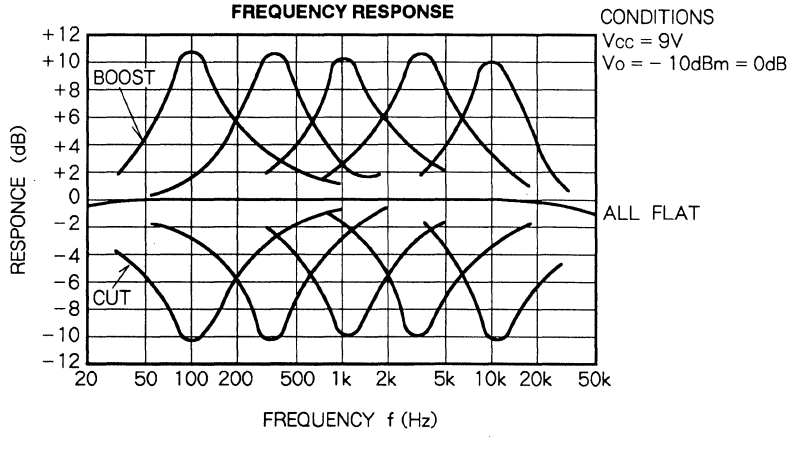
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



TOTAL HORMONIC DISTORTION VS. FREQUENCY

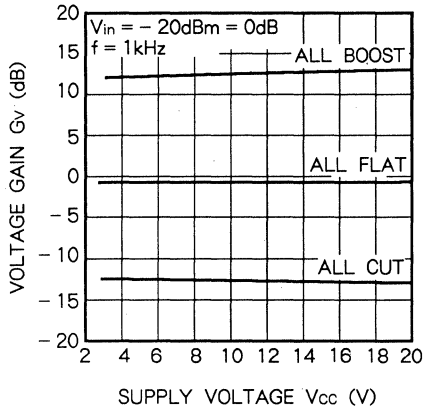


FREQUENCY RESPONSE

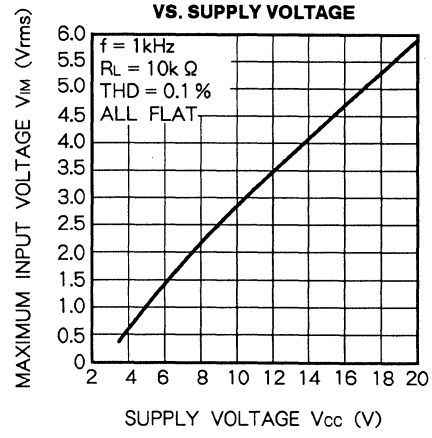


CONDITIONS
Vcc = 9V
Vo = – 10dBm = 0dB

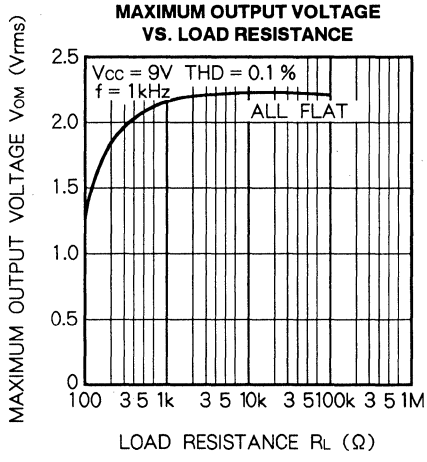
VOLTAGE GAIN VS. SUPPLY VOLTAGE



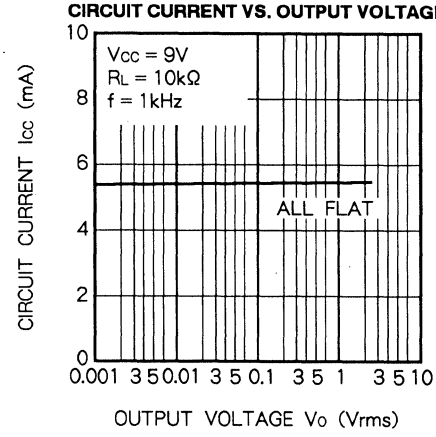
MAXIMUM INPUT VOLTAGE VS. SUPPLY VOLTAGE



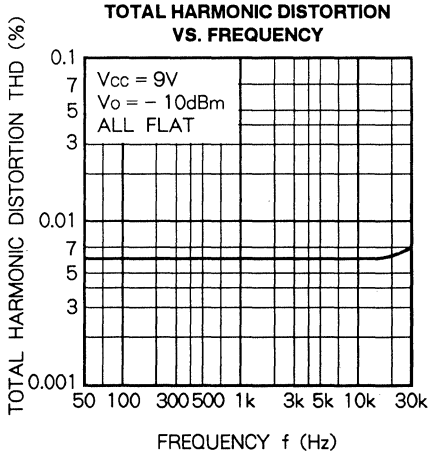
MAXIMUM OUTPUT VOLTAGE VS. LOAD RESISTANCE



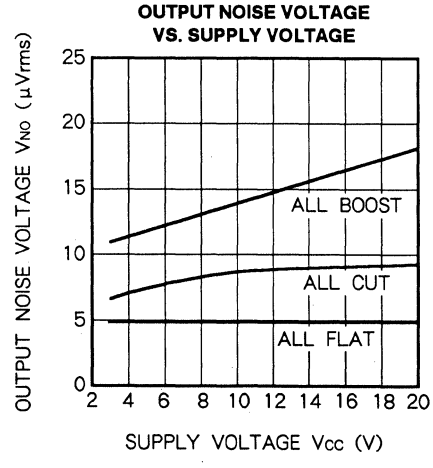
CIRCUIT CURRENT VS. OUTPUT VOLTAGE



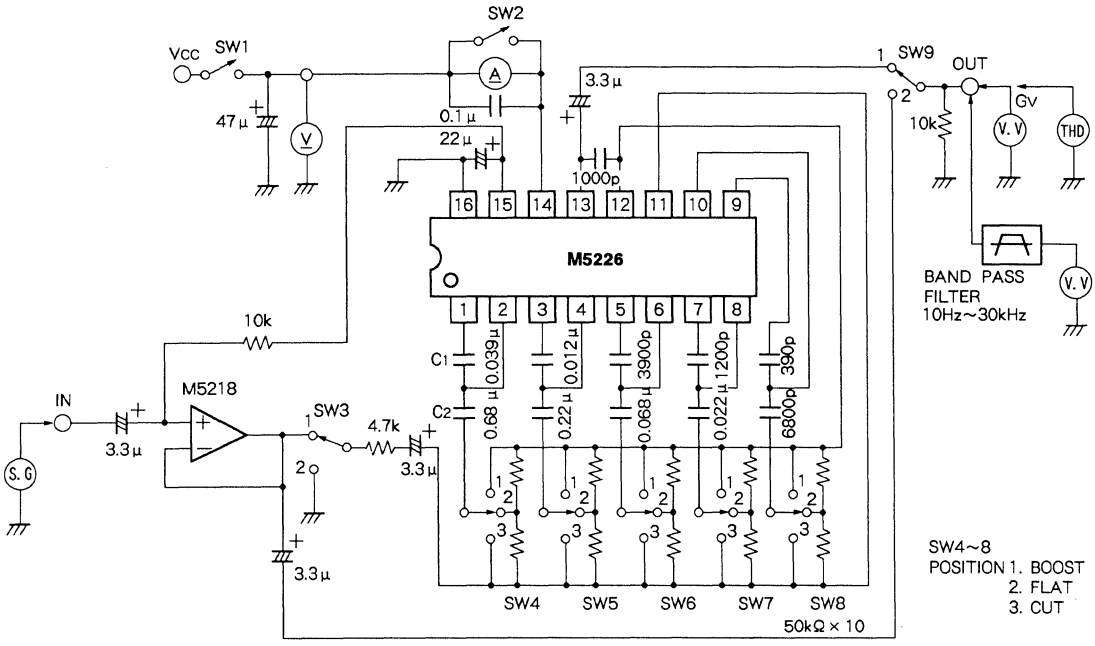
TOTAL HARMONIC DISTORTION VS. FREQUENCY



OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



TEST CIRCUIT (Circuit current Icc, Voltage gain Gv, Total harmonic distortion THD, Output noise voltage VNO)



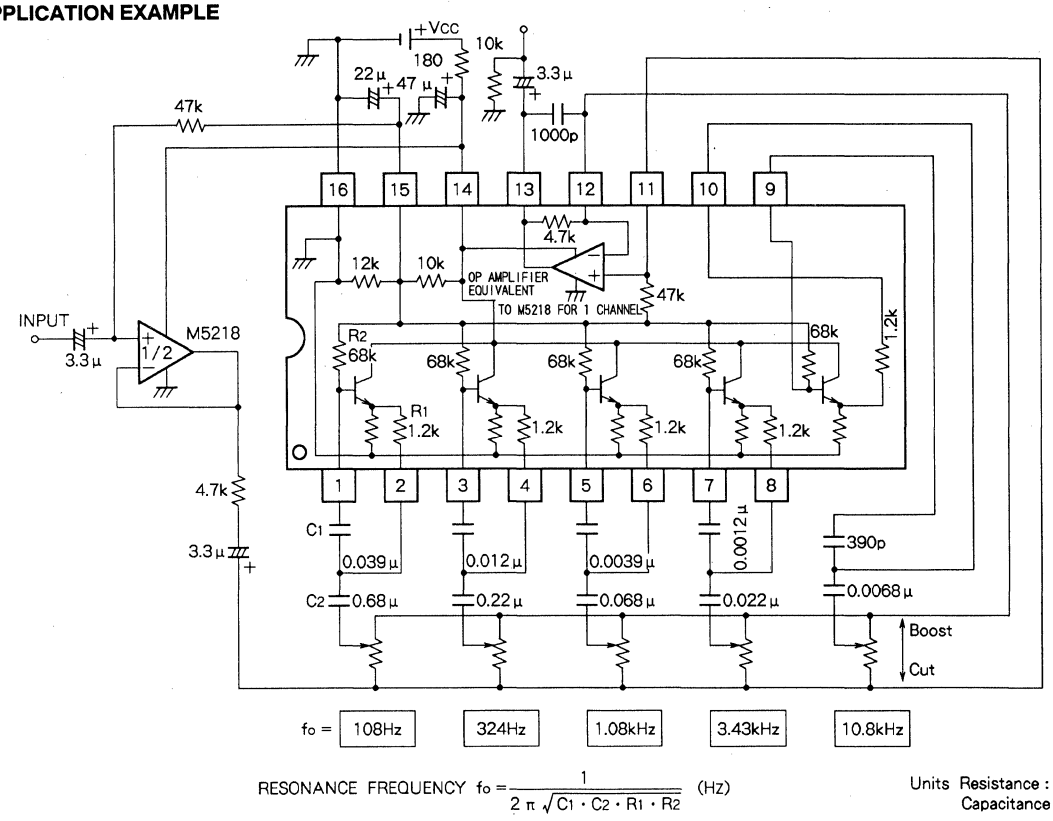
Units Resistance : Ω
Capacitance : F

TEST CIRCUIT SWITCH MATRIX

Test item		SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9
Icc		OFF	1	○	○	○	○	○	1
GV(FLAT)		ON	1	2	2	2	2	2	1
GV(BOOST)	f = 108Hz	ON	1	1	2	2	2	2	1
	f = 343Hz	ON	1	2	1	2	2	2	1
	f = 1.08kHz	ON	1	2	2	1	2	2	1
	f = 3.43kHz	ON	1	2	2	2	1	2	1
	f = 10.8kHz	ON	1	2	2	2	2	1	1
GV(CUT)	f = 108Hz	ON	1	3	2	2	2	2	1
	f = 343Hz	ON	1	2	3	2	2	2	1
	f = 1.08kHz	ON	1	2	2	3	2	2	1
	f = 3.43kHz	ON	1	2	2	2	3	2	1
	f = 10.8kHz	ON	1	2	2	2	2	3	1
THD		ON	1	2	2	2	2	2	1
VNO(ALLFLAT)		ON	2	2	2	2	2	2	1

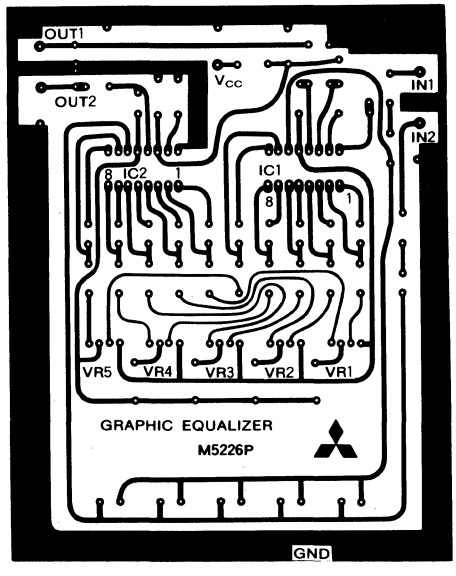
Note : The mark "○" applies to both 1 and 2

APPLICATION EXAMPLE

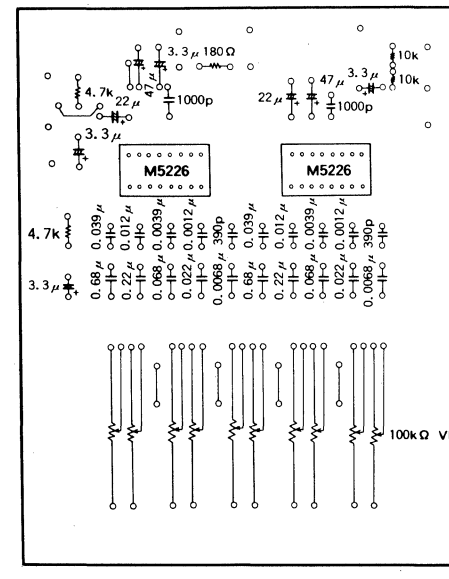


PRINTED CIRCUIT BOARD FOR CIRCUIT TESTING (TYPICAL APPLICATION EXAMPLE)

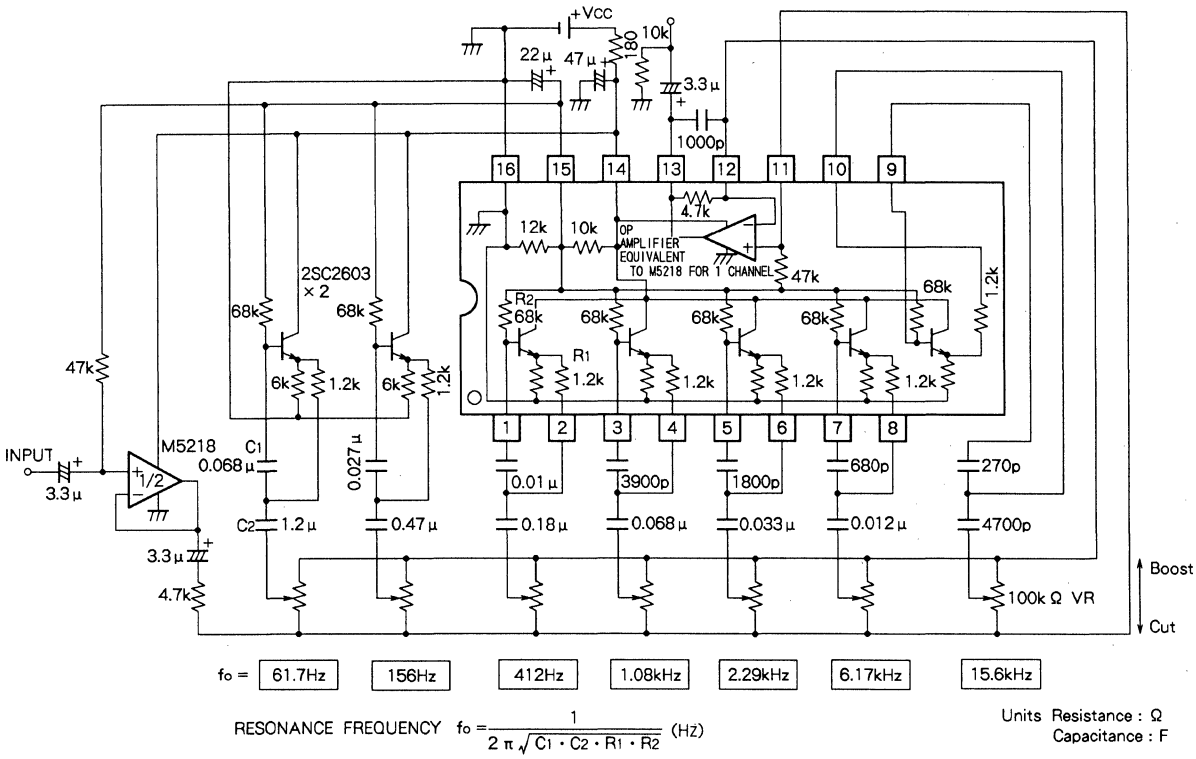
PC BOAD PARTS-PLACEMENT DIAGRAM (COPPER FOIL SIDE)



PC BOAD PARTS-PRACEMENT-DIAGRAM (PARTS SIDE)



APPLICATION EXAMPLE (7-ELEMENT)



M5227P,FP

Hi-Fi 5-ELEMENT GRAPHIC EQUALIZER IC

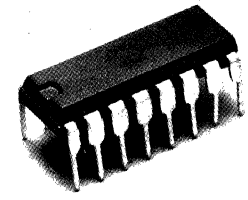
DESCRIPTION

The M5227 is a 5-element graphic equalizer IC best suited to Hi-Fi audio systems. It has 5-element resonance circuits with OP amp system and an output OP amp.

The IC can be used in compact sets of high-density assemblies, modules, and hybrid ICs. Its applications cover Hi-Fi setereo sets, radio cassette tape players, car audio systems, music centers, and electronic musical instruments.

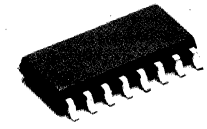
FEATURES

- High withstand voltage and wide supply voltage range ..... V_{CC} = ± 2 ~ ± 18V(4~36V)
- Low distortion ..... THD = 0.002 % (typ) @f = 1kHz, Flat, V_O = 5Vrms
- Low noise ..... V_{NO} = 6 μVrms (typ) @Flat input short
- Variable Gv by external resistance ..... Gv = ± 12dB (typ)
- Single power (use GND pin⑮ for V_{CC}/2)
- Large allowable input voltage ..... V_{IM} = 9.5Vrms (typ) @f = 1kHz, THD = 1 %, Flat



Outline 16P4(P)

2.54mm pitch 300mil DIP
(6.3mm × 19.0mm × 3.3mm)



Outline 16P2S-A(FP)

1.27mm pitch 225mil SOP
(4.4mm × 10.0mm × 1.5mm)

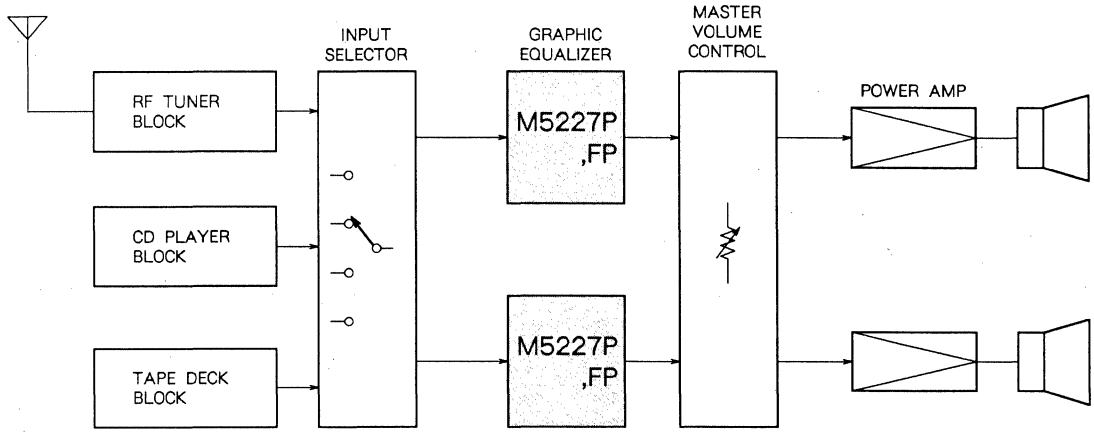
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC}, V_{EE} = ± 2 ~ ± 18V or V_{CC} = 4~36V

Rated supply voltage ..... V_{CC}, V_{EE} = ± 15V or V_{CC} = 30V

Rated power dissipation ..... 1000mW(P) 550mW(FP)

SYSTEM CONFIGURATION

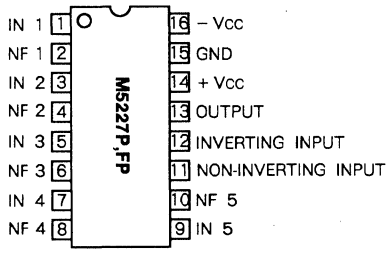


MITSUBISHI ELECTRIC

M5227P,FP

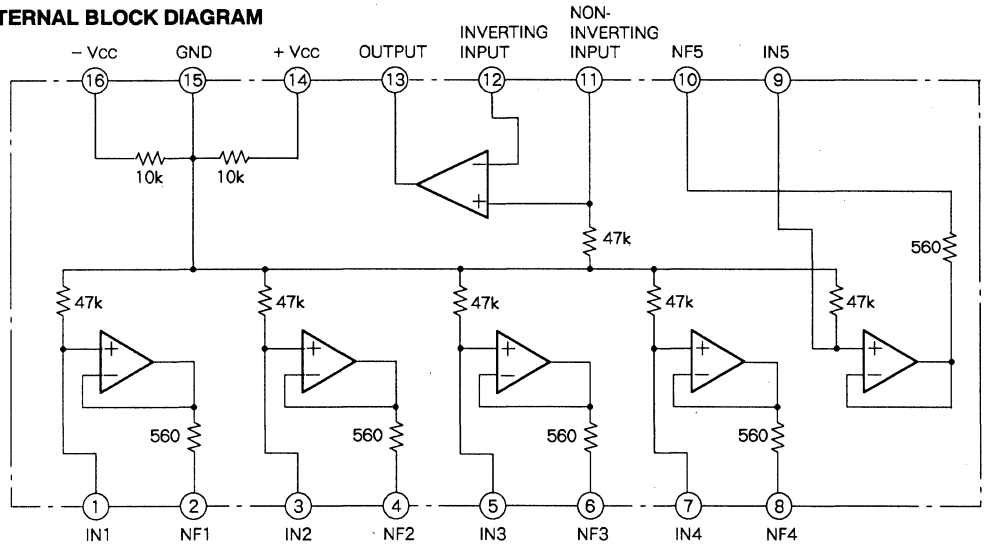
HI-Fi 5-ELEMENT GRAPHIC EQUALIZER IC

PIN CONFIGURATION



Outline 16P4(P)
16P2S-A(FP)

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

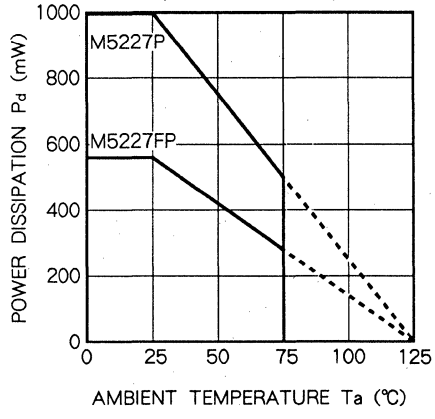
Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	36(± 18)	V
I_{LP}	Load current	50	mA
P_d	Power dissipation	1000(DIP)/550(FP)	mW
T_{opr}	Operating temperature	− 20～+ 75	℃
T_{stg}	Storage temperature	− 55～+ 125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = ± 15V)

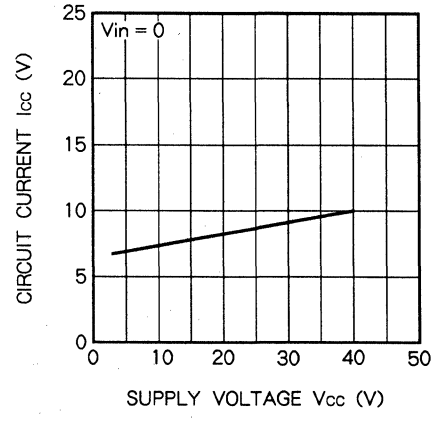
Symbol	Parameter	Test Conditions		Limits			Unit
		f (Hz)		Min	Typ	Max	
I_{CC}	Circuit current	−	V_{in} = 0	6	9	12	mA
$G_{V(FLAT)}$	Voltage gain flat	1k	V_{in} = − 10dBm	− 2.3	− 0.3	+1.7	dB
$G_{V(BOOST)}$	Voltage gain boost (Response)	108	V_{in} = − 10dBm $V_{O(FLAT)}$ = 0dB	9.5	12.0	13.5	dB
		343		9.5	12.0	13.5	
		1.08k		9.5	12.0	13.5	
		3.43k		9.5	12.0	13.5	
		10.8k		9.5	12.0	13.5	
$G_{V(CUT)}$	Voltage gain cut (Response)	108	V_{in} = − 10dBm $V_{O(FLAT)}$ = 0dB	−13.5	−12.0	− 9.5	dB
		343		−13.5	−12.0	− 9.5	
		1.08k		−13.5	−12.0	− 9.5	
		3.43k		−13.5	−12.0	− 9.5	
		10.8k		−13.5	−12.0	− 9.5	
THD	Distortion ratio	1k	V_{in} = 5Vrms Flat	−	0.002	0.1	%
V_{NO}	Output noise voltage	Input short BW : 10Hz～30kHz Flat		−	6	25	μVrms
V_{OM}	Maximum output voltage	1k	THD = 1 %, Flat	7	9.5	−	Vrms

TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)



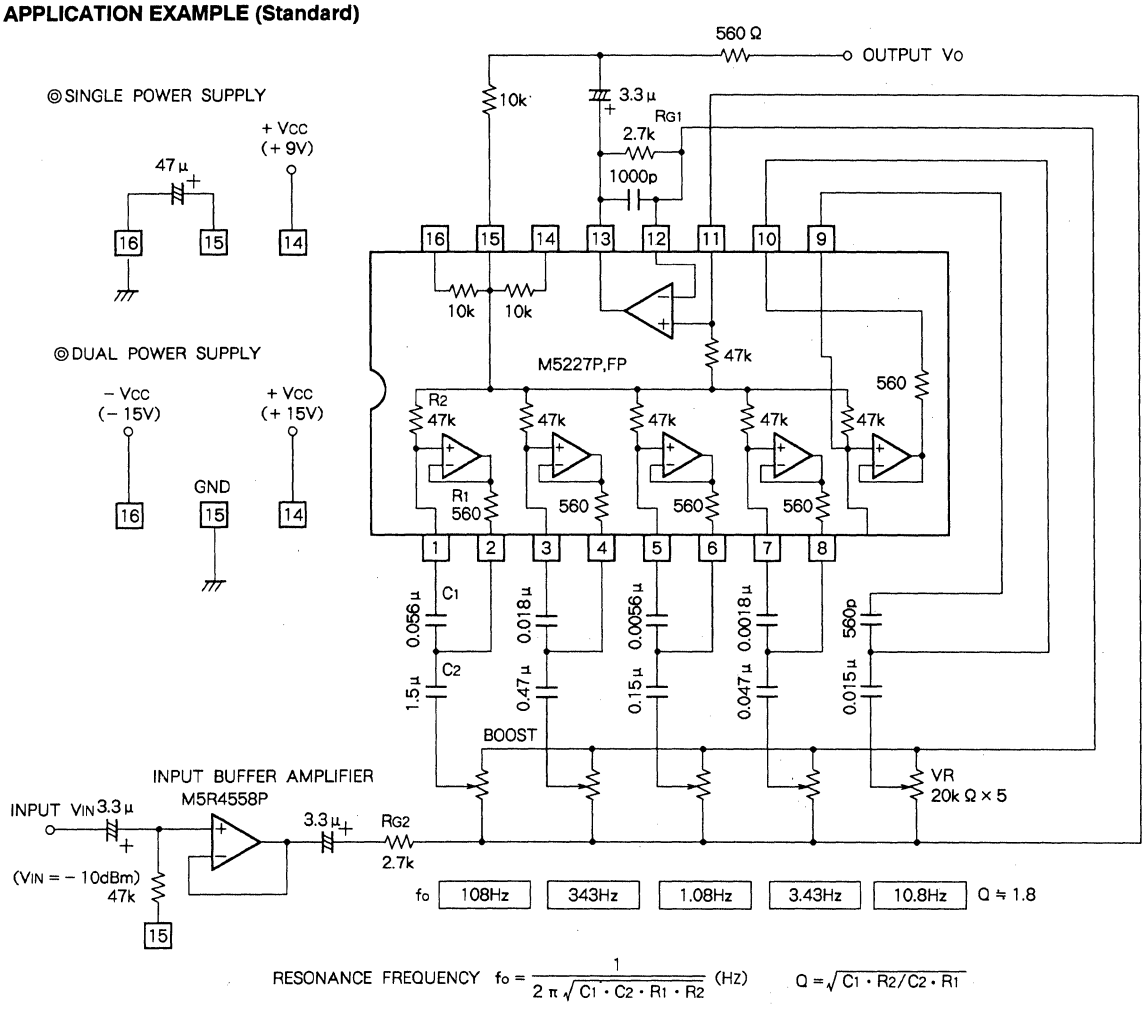
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



M5227P,FP

Hi-Fi 5-ELEMENT GRAPHIC EQUALIZER IC

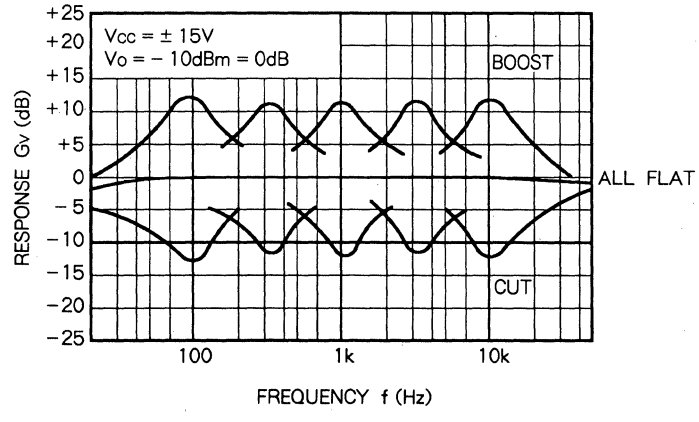
APPLICATION EXAMPLE (Standard)



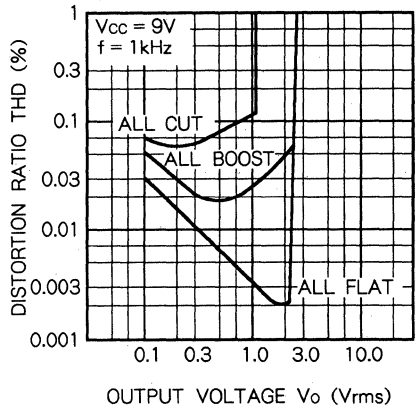
$$\text{RESONANCE FREQUENCY } f_o = \frac{1}{2\pi\sqrt{C_1 \cdot C_2 \cdot R_1 \cdot R_2}} \text{ (Hz)} \qquad Q = \sqrt{C_1 \cdot R_2 / C_2 \cdot R_1}$$

Units Resistance : Ω
Capacitance : F

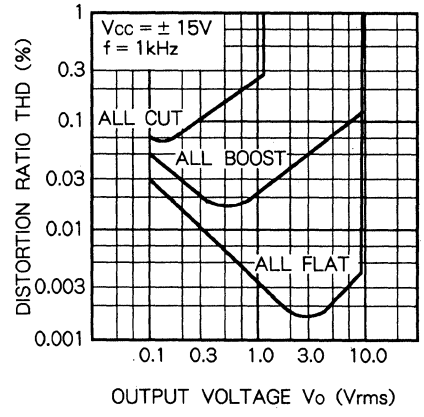
FREQUENCY CHARACTERISTICS



THD – Vo



THD – Vo

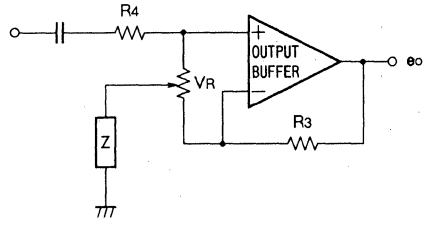


OPERATION DESCRIPTION

The M5227P consists of 5 resonance circuits and an output amplifier, and can also from a graphic equalizer, which has optional resonance frequency f_o, by the externally connecting condensor C_1, C_2 of variable resistance and a resonance circuit. The impedance is minimized by resonating and the semiconductor, which is adopted in the resonance circuit, can therefore vary the frequency gain.

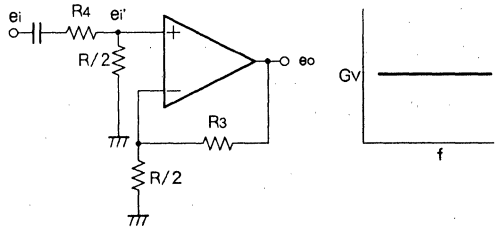
1. Flat boost cut

The resonance frequency gain can be altered by varying the external variable register.



Z is an impedance in the resonance circuit

(1) Flat



R/2 is resistance at the center of VR

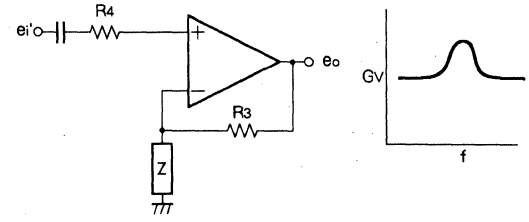
When the variable register is in center position, the equivalent circuit as in the above diagram can be obtained. At this stage if R_3, R_4 are set at the same level of resistance, then

$$e_i' = \frac{R/2}{R_4 + R/2} \cdot e_i, \quad A_V = \frac{R_3 + R/2}{R/2}$$

$$e_o = A_V' \cdot e_i' = e_i$$

and, the frequency characteristics will be level regardless of the resonance circuit.

(2) Boost



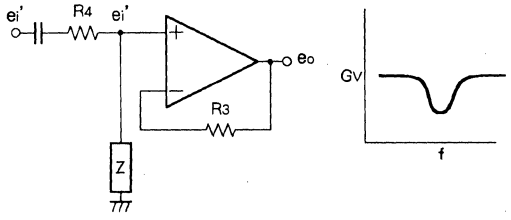
When the variable register is in boost position, the resonance circuit is connected to the NF loop of the output buffer amplifier. At this stage, R is much smaller than R_3, R_4, so it can be disregarded.

The gain Av is $A_V = \frac{R_3 + 4}{Z}$ and,

the output voltage e_o is $e_o = A_V \cdot e_i = \frac{R_3 + Z}{Z} \cdot e_i$

When Z is smallest, the gain in resonance is the greatest, and the optional frequency is then boosted.

(3) Cut



When the variable register is in cut position, the resonance circuit is connected to the input side of the output buffer amplifier. When R is disregarded as the boost.

$e_i' = \frac{Z}{R_4 + Z} \cdot e_i$, $A_V = 1$ and

the output voltage e_o is $e_o = A_V \cdot e_i' = \frac{Z}{R_4 + Z} \cdot e_i$

When Z is smallest, the gain in resonance is the greatest, and the optional frequency is then cut.

2. Resonance circuit

The semiconductor inductor converts L in the R, L, C serial resonance circuit into a CR pin by the buffer functions of active pins such as registers, operational amplifiers, and works in almost the same way as the R, L, C serial resonance circuit.

The R, L, C resonance frequency

f_o is $f_o = 1/2\pi\sqrt{LC}$ ·····Equation No. 1

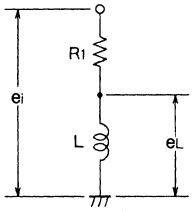


Fig. 1

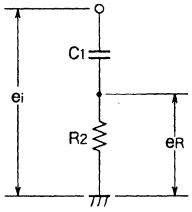


Fig. 2

When the voltage e_i is supplied to the resonance circuit as shown in Fig. 1, $e_L = j\omega L \cdot e_i/(R_1 + j\omega L)$

If e_i is then supplied to the pins C_1, R_2 as shown in Fig. 2,

When $e_L = e_R$, $L = C_1 \cdot R_1 \cdot R_2$·····Equation No. 2

But, if e_R is replaced by L of the R and L serial circuit, R_1 and C_1 are automatically connected in a parallel mannder, and the value of e_R will be changed. So, in order to keep the value of e_R stable, a buffer amplifier should be used. The buffer amplifier is equivalent to an impedance.

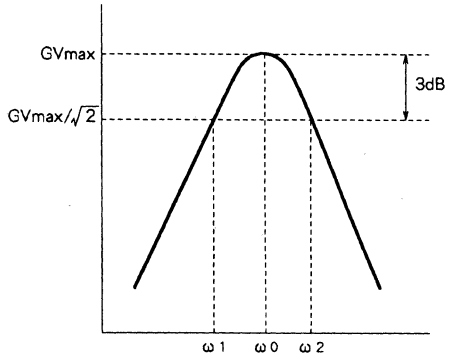
By equations 1 and 2, the resonance frequency, f_o is

$f_o = 1/2\pi\sqrt{C_1 \cdot C_2 \cdot R_1 \cdot R_2}$

The buffer amplifier in the resonance circuit of the M5227 is composed of operational amplifiers.

3. Angle of maximum resonance

The angle of maximum resonance, Q, is defined by the ratio of ω_o ($\omega_o = 2\pi f_o$) and the frequency band width, $\omega_2 - \omega_1$, $(Gmax/\sqrt{2})$.



The value of Q is found by the following equation :

$Q = \sqrt{C_1 \cdot R_2/C_2 \cdot R_1}$

The greater the value of Q, the narrower the frequency band width, and vice versa.

The M5227 is composed of R_1, R_2, so Q is defined by selecting the external condensor.

M5229P,FP

Hi-Fi 7-ELEMENT GRAPHIC EQUALIZER IC

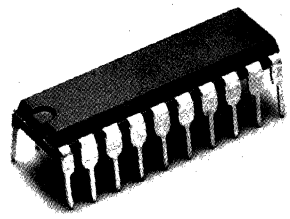
DESCRIPTION

The M5229 is a 7-element graphic equalizer IC best suited to Hi-Fi audio systems. It has 7-element resonance circuits with OP amp system and an output OP amp.

The IC can be used in compact sets of high-density assemblies, modules, and hybrid ICs. Its applications cover Hi-Fi stereo sets, radio cassette tape players, car audio systems, music centers, and electronic instruments.

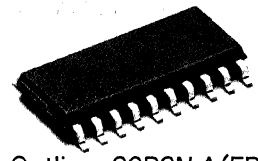
FEATURES

- High withstand voltage and wide supply voltage range ..... $V_{CC} = \pm 2 \sim \pm 18V(4 \sim 36V)$
- Low distortion ..... THD = 0.002 %(typ) (@ f = 1kHz, Flat, V_O = 5Vrms)
- Low noise ..... V_{NO} = 9 μ Vrms(typ) (@ Flat, input short)
- Variable Gv by external resistance ..... Gv = ± 12dB(typ)
- Single power (use GND pin ⑲ for Vcc/2 pin)
- Large allowable input voltage ..... V_{IM} = 9.5Vrms(typ) (@ f = 1kHz, THD = 1 %, Flat)



Outline 20P4(P)

2.54mm pitch 300mil DIP
(6.3mm × 24.0mm × 3.3mm)



Outline 20P2N-A(FP)

1.27mm pitch 300mil SOP
(5.3mm × 12.6mm × 1.8mm)

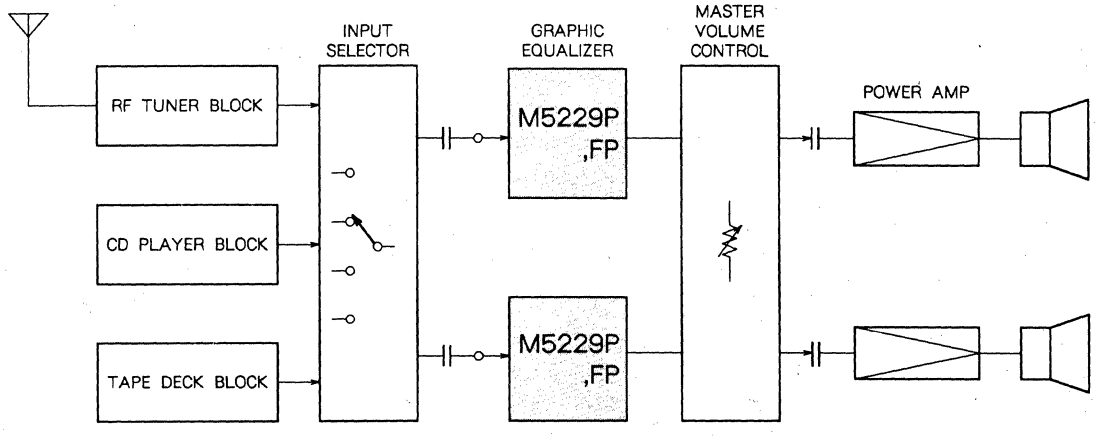
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC}, $V_{EE} = \pm 2 \sim \pm 18V$ or $V_{CC} = 4 \sim 36V$

Rated supply voltage ..... V_{CC}, $V_{EE} = \pm 15V$ or $V_{CC} = 30V$

Rated power dissipation ..... 1000mW(DIP) 550mW(FP)

SYSTEM CONFIGURATION

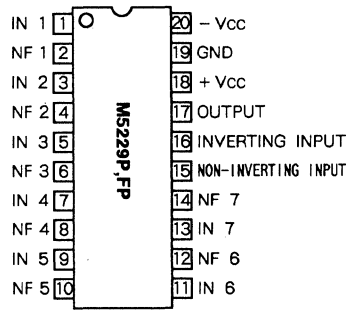


MITSUBISHI ELECTRIC

M5229P,FP

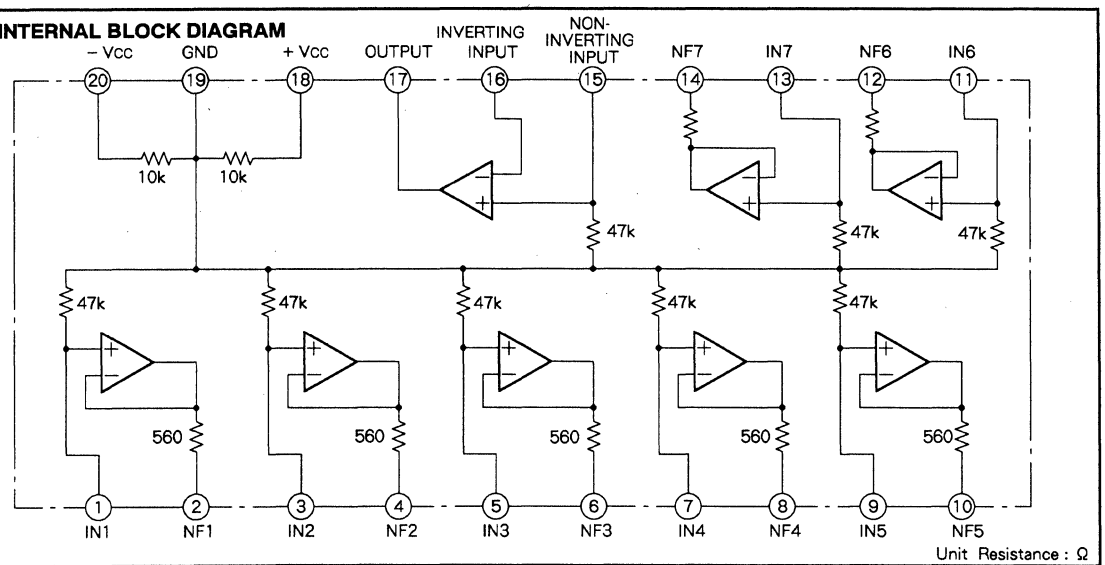
Hi-Fi 7-ELEMENT GRAPHIC EQUALIZER IC

PIN CONFIGURATION



Outline 20P4(P)
20P2N-A(FP)

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

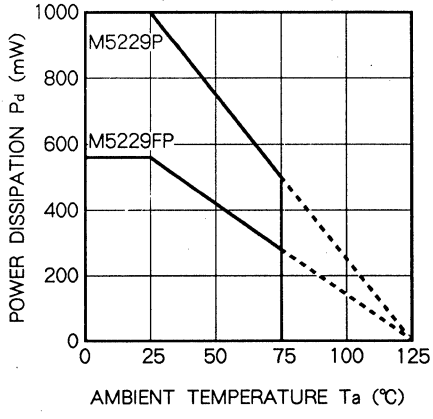
Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	36 (± 18)	V
I_{LP}	Load current	50	mA
P_d	Power dissipation	1000(DIP)/550(FP)	mW
T_{opr}	Operating temperature	− 20~ + 75	℃
T_{stg}	Storage temperature	− 55~ + 125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = ± 15V)

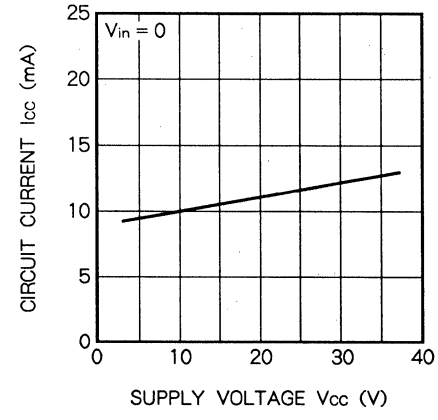
Symbol	Parameter		f (Hz)	Test conditions	Limit Min	Limit Typ	Limit Max	Unit
I_{CC}	Ciucuit current		−	V_{in} = 0	8	12	16	mA
G_V (FLAT)	Voltage Gain	Flat	1k	V_{in} = − 10dBm	− 2.3	− 0.3	+ 1.7	dB
$G_{V(BOOST)}$		Boost (Response)	60	V_{in} = − 10dBm, V_O (FLAT) = 0dB	9.0	12.0	14.0	dB
			120		9.0	12.0	14.0	
			360		9.0	12.0	14.0	
			1k		9.0	12.0	14.0	
			2.5k		9.0	12.0	14.0	
			6.7k		9.0	12.0	14.0	
			15.7k		9.0	12.0	14.0	
G_V (CUT)		Cut (Response)	60	V_{in} = − 10dBm, V_O (FLAT) = 0dB	− 14.0	− 12.0	− 9.0	dB
			120		− 14.0	− 12.0	− 9.0	
			360		− 14.0	− 12.0	− 9.0	
			1k		− 14.0	− 12.0	− 9.0	
			2.5k		− 14.0	− 12.0	− 9.0	
			6.7k		− 14.0	− 12.0	− 9.0	
			15.7k		− 14.0	− 12.0	− 9.0	
V_{OM}	Maximum output voltage		1k	THD = 1 %, Flat	7	9.5	−	Vrms
THD	Distortion ratio		1k	V_O = 5Vrms, Flat	−	0.002	0.1	%
V_{NO}	Output noise voltage		Input short BM : 10Hz~30kHz, Flat		−	9	35	μVrms

TYPICAL CHARACTERISTICS

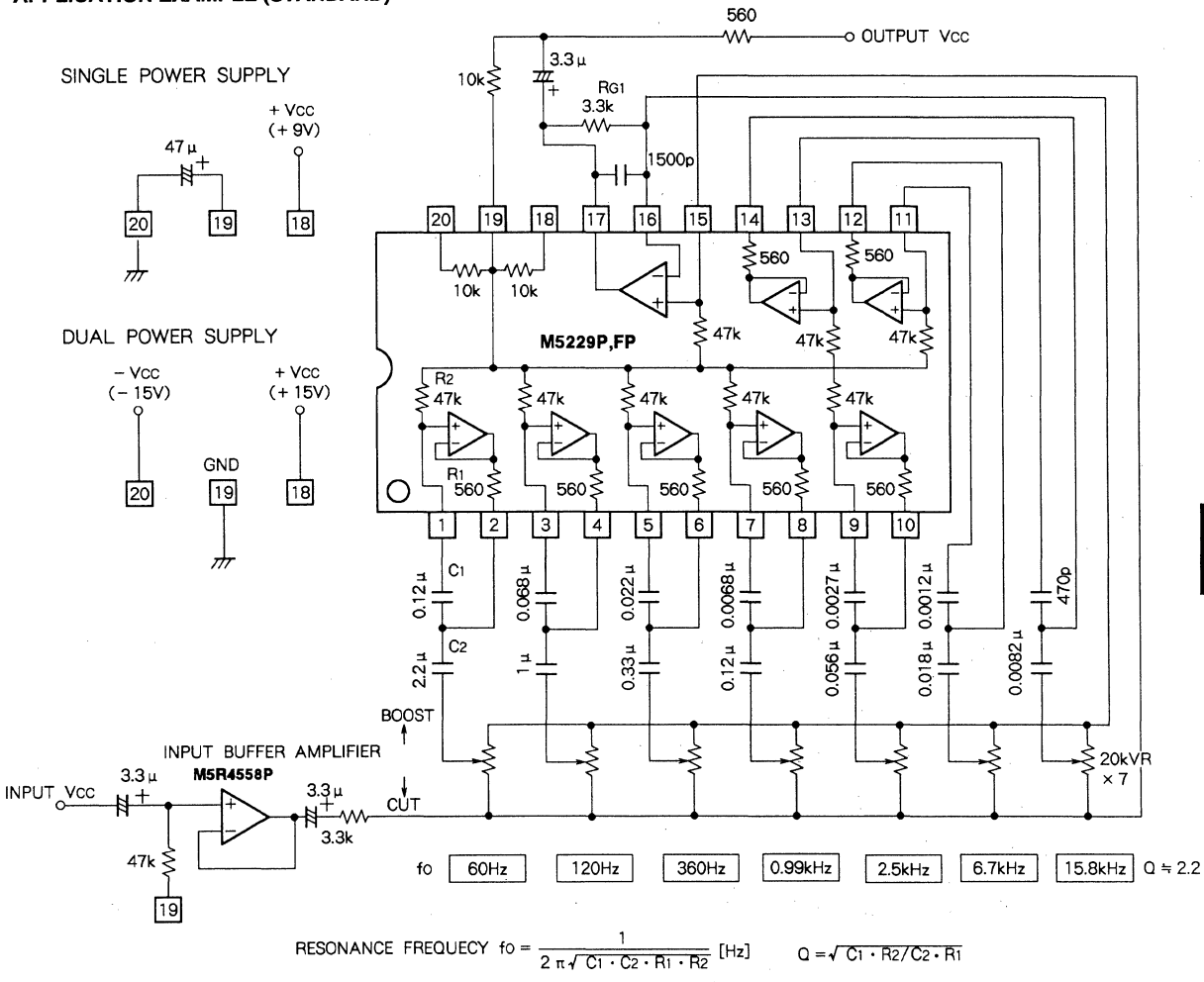
THERMAL DERATING (MAXIMUM RATING)



CIRCUIT CURRENT VS. SUPPLY VOLTAGE



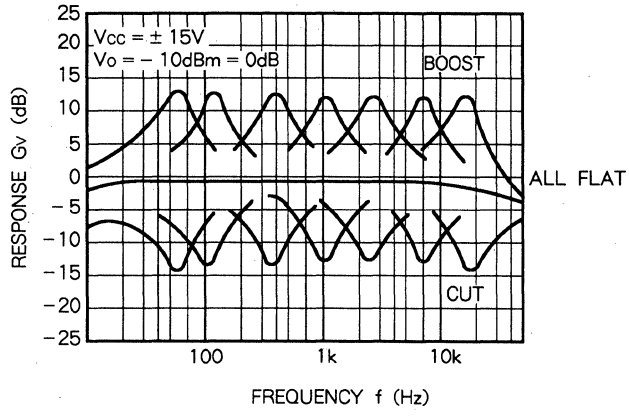
APPLICATION EXAMPLE (STANDARD)



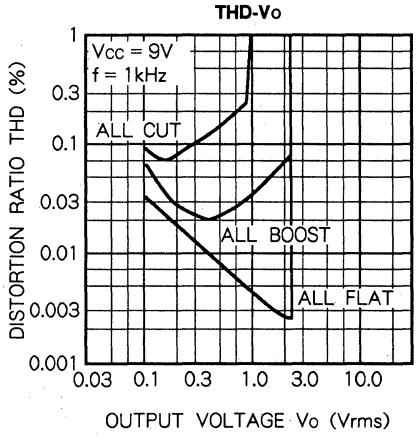
$$\text{RESONANCE FREQUECY } fo = \frac{1}{2\pi\sqrt{C1 \cdot C2 \cdot R1 \cdot R2}} \text{ [Hz]} \qquad Q = \sqrt{C1 \cdot R2 / C2 \cdot R1}$$

Units Resistance : Ω
Capacitance : F

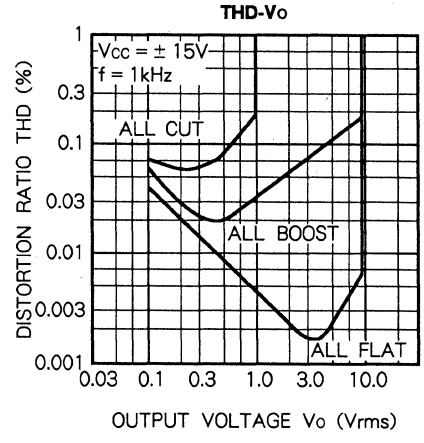
FREQUENCY CHARACTERISTICS



THD-Vo



THD-Vo

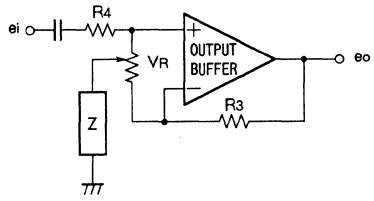


OPERATION DESCRIPTION

The M5229 consists of 7 resonance circuits and an output amplifier, and can also form a graphic epualizer, which has optional resonance frequency, fo, by the externally connecting condensor C_1, C_2 of variable resistance and a resonance circuit. The impedance is minimized by resonating and the semiconductor inductor, which is adopted in the resonance circuit, can therefore vary the frequency gain.

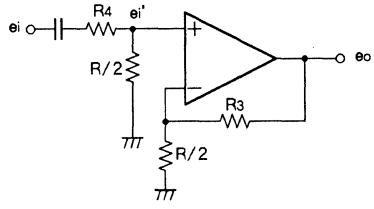
1. Flat boost cut

The resonance frequency gain can be altered by varying the external variable register.

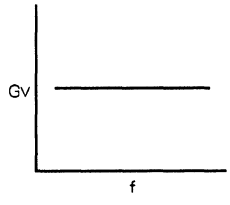


Z is an impedance in the resonance circuit

(1) Flat



R/2 is resistance at the center of VR



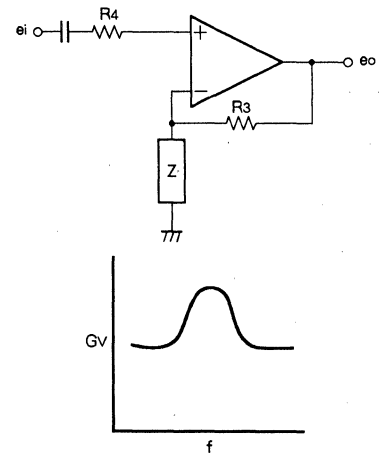
When the variable register is in center position, the equivalant circuit as in the above diagram can be obtained. At this stage if R_3, R_4 are set at the same level of resistance, then

$$ei' = \frac{R/2}{R_4 + R/2} \cdot ei, \quad Av = \frac{R_3 + R/2}{R/2}$$

$$eo = Av \cdot ei' = ei$$

and, the frequency characteristics will be level regardless of the resonance circuit.

(2) Boost



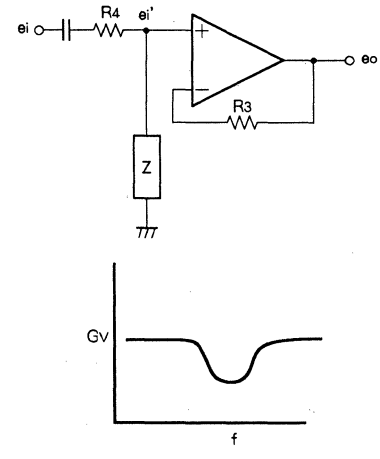
When the variable register is in boost position, the resonance circuit is connected to the NF loop of the output buffer amplifier. At this stage, R is much smaller than R_3, R_4, so it can be disregarded.

The gain Av is $Av = \frac{R_3 + Z}{Z}$ and,

the output voltage eo is $eo = Av \cdot ei = \frac{R_3 + Z}{Z} \cdot ei$

When Z is smallest, the gain in resonance is the greatest, and the optional frequency is then boosted.

(3) Cut



When the variable register is in cut position, the resonance circuit is connected to the input side of the output buffer amplifier. When R is disregarded as the boost,

$e_i' = \frac{Z}{R_4 + Z} \cdot e_i \cdot Av = 1$ and,

the output voltage e_o is $e_o = Av \cdot e_i' = \frac{Z}{R_4 + Z} \cdot e_i$

When Z is smallest, the gain in resonance is the greatest, and the optional frequency is then cut.

2. Resonance circuit

The semiconductor inductor converts L in the R, L, C serial resonance circuit into a CR pin by the buffer functions of active pins such as registers, Operational amplifiers, and works in a almost the same way as the R, L, C serial resonance circuit.

The R, L, C resonance frequency fo is

$fo = 1/2\,\pi\sqrt{LC}$ ·····Equation No.1

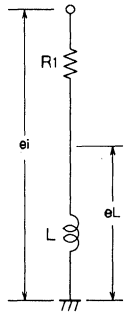


Fig. 1

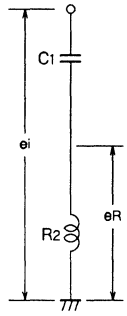


Fig. 2

When the voltage e_i is supplied to the resonance circuit as shown in Fig. 1.

$e_L = j\omega L \cdot e_i / (R_1 + j\omega L)$

If e_i is then supplied to the pins C_1, R_2 as shown in Fig.2,

$e_R = e_i \cdot j\omega C_1 \cdot R_2 / C_1 + j\omega C_1 \cdot R_2$

$= j\omega C_1 \cdot R_1 \cdot R_2 / CR_1 + j\omega C_1 \cdot R_1 \cdot R_2$

When $e_L = e_R$, $L = C_1 \cdot R_1 \cdot R_2$·····Equation No.2

But if e_R is replaced by L of the R and L serial circuit, R_1 and C_1 are automatically connected in a parallel manner, and the value of e_R will be changed. So, in order to keep the value of e_R stable, a buffer amplifier should be used. The buffer amplifier is equivalent to an impedance.

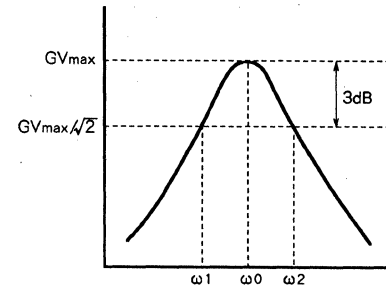
By epuations 1 and 2, the resonance frequency, fo is

$fo = 1/2\,\pi\sqrt{C_1 \cdot C_2 \cdot R_1 \cdot R_2}$

The buffer amplifier in the resonance circuit of the M5229 is composed of operational amplifiers.

3. Angle of maximum resonance

The angle of maximum resonance, Q, is defined by the ratio of ωo ($\omega o = 2$ fo) and the frequency band width, $\omega 2$-$\omega 1$, ($Gmax/\sqrt{2}$)



The value of Q is found by the following equation ;

$Q = \sqrt{C_1 \cdot R_2 / C_2 \cdot R_1}$

The greater the value of Q, the narrower the frequency band width, and vice versa.

The M5229 is composed of R_1, R_2, so Q is defined by selecting the external condensor.

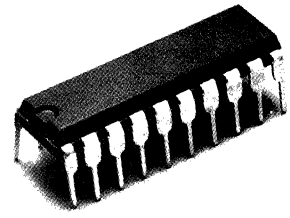
M5243P,FP

3-ELEMENT (SIMPLE 4-ELEMENT) DUAL CHANNEL GRAPHIC EQUALIZER IC

DESCRIPTION

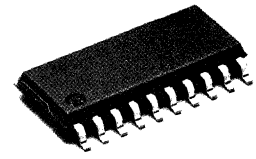
The M5243 is a dual channel 3-element graphic equalizer IC best suited to Hi-Fi audio systems. Each channel incorporates 3-elements of transistor-based resonance circuits and an output OP amp.

Applications cover radio cassette tape recorders, car stereo sets, and portable stereo systems.



Outline 20P4(P)

2.54mm pitch 300mil DIP
(6.3mm × 24.0mm × 3.3mm)



Outline 20P2N-A(FP)

1.27mm pitch 300mil SOP
(5.3mm × 12.6mm × 1.8mm)

FEATURES

- It is possible to stereo (dual-channel) with single IC
- Large capacitor take off by reference voltage circuit self-contained
- Variable Gv by external resistance
- Low noise ····· V_{NO} FLAT = 4 μVrms(typ)
- Low distortion ratio ····· THD = 0.004 %(typ)

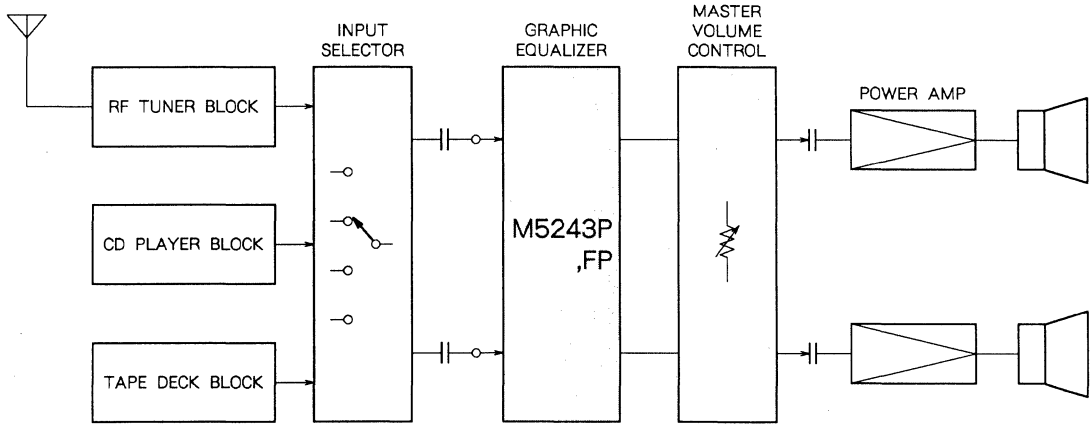
Type(marking)	Recommended supply voltage	Type(marking)	Recommended supply voltage
M5243P06	4.0~6.0V	**M5243FP06**	4.0~6.0V
M5243P75	5.0~7.5V	**M5243FP75**	5.0~7.5V
M5243P09	6.0~9.0V	**M5243FP09**	6.0~9.0V
M5243P12	8.0~12.0V	**M5243FP12**	8.0~12.0V

(@ f = 1kHz, Flat)

RECOMMENDED OPERATING CONDITIONS

Rated disspation voltage ····· 1000mW(P)
550mW(FP)

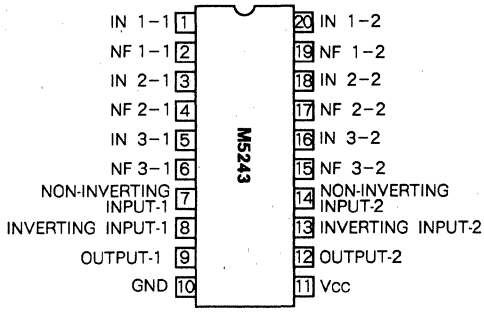
SYSTEM CONFIGURATION



M5243P,FP

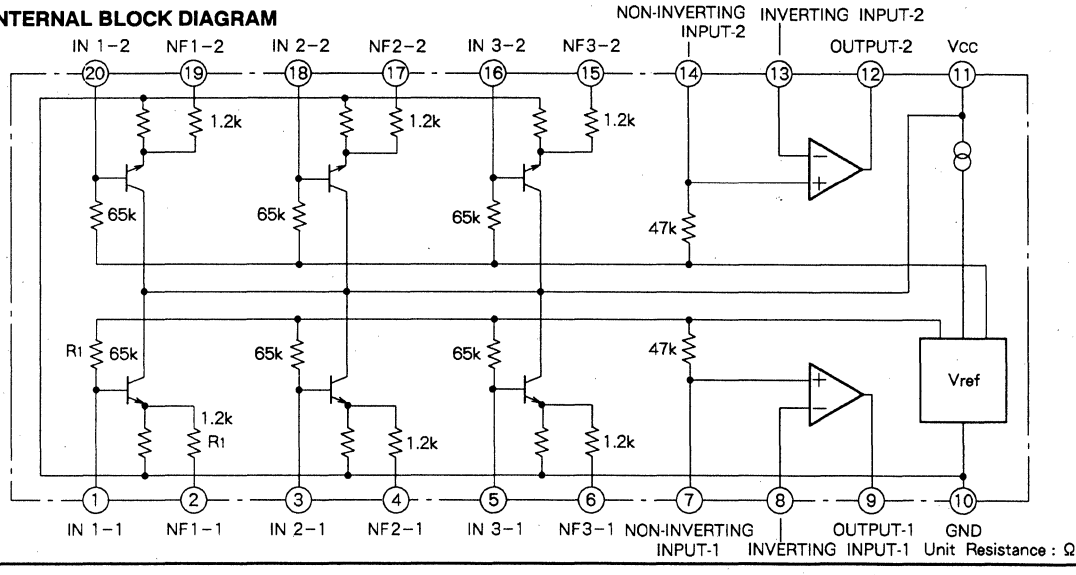
3-ELEMENT (SIMPLE 4-ELEMENT) DUAL CHANNEL GRAPHIC EQUALIZER IC

PIN CONFIGURATION



Outline 20P4(P)
20P2N-A(FP)

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

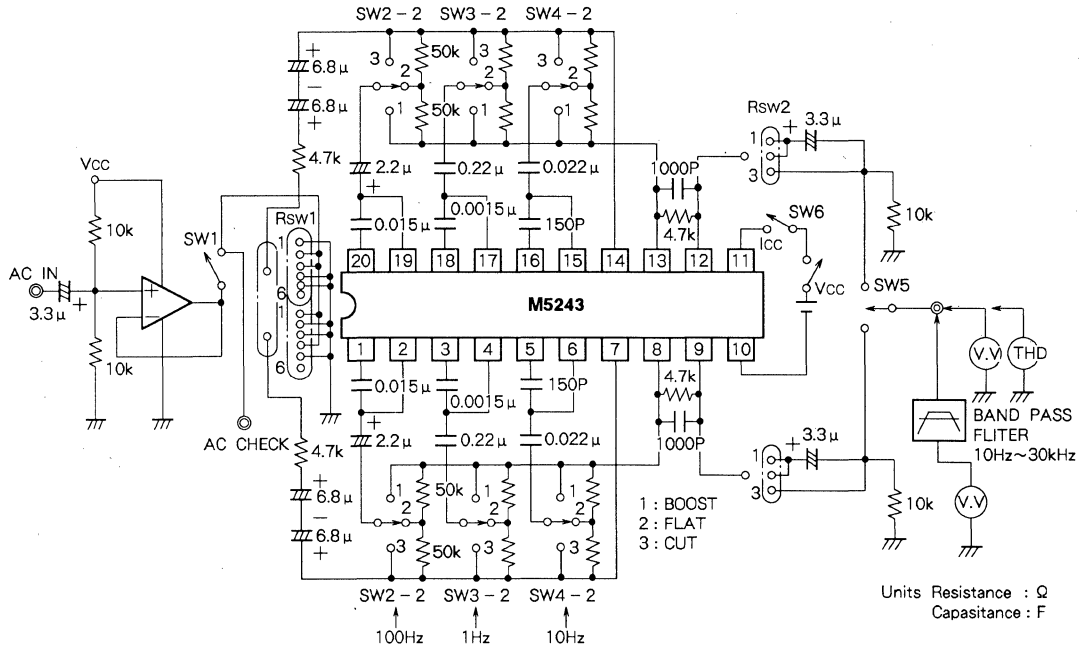
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	20	V
I_{LP}	Load current	30	mA
P_d	Power dissipation	FP ; 550/P ; 1	mW/W
T_{opr}	Operating temperature	− 20 ~ + 75	℃
T_{stg}	Strage temperature	− 55 ~ + 125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃)

Symbol	Parameter		Test conditions		Limits			Unit
				f(Hz)	Min	Typ	Max	
I_{CC}	Circuit current			−	5.0	7.5	12.0	mA
$G_{V\ (FLAT)}$	Voltege gain	Flat	V_i = − 10dBm, R_g = 4.7k Ω	1k	− 2.0	− 0.5	1.0	dB
$G_{V(BOOST)}$		Boost		100	8.0	10.0	12.0	
				1k	8.0	10.0	12.0	
				10k	8.8	10.0	12.0	
$G_{V\ (CUT)}$		Cut		100	−13.0	−11.0	− 9.0	
				1k	−13.0	−11.0	− 9.0	
				10k	−13.0	−11.0	− 9.0	
THD	Total harmonic distortion		V_i = 1Vrms, All flat	1k	−	0.004	0.1	%
V_{OM}	Maximum output voltage	**M5243X06**	THD = 0.1 %, All flat	1k	0.5	1.0	−	Vrms
		M5243X75			1.0	1.5	−	
		M5243X09			1.5	1.9	−	
		M5243X12			2.0	2.9	−	
CS	Channel separation		V_i = − 10dBm, All flat	1k	60	75	−	dB
RR	Ripple rejection		V_i = − 10dBm, All flat	120	55	65	−	dB
V_{NO}	Output noise voltage		All flat BW : 10Hz~30kHz	−	−	4	15	μVrms
V_M	Middle point voltage	**M5243X06**		−	2.1	3.0	3.9	V
		M5243X75			2.7	3.75	4.8	
		M5243X09			3.5	4.5	5.5	
		M5243X12			5.0	6.0	7.0	

STANDARD TEST CIRCUIT

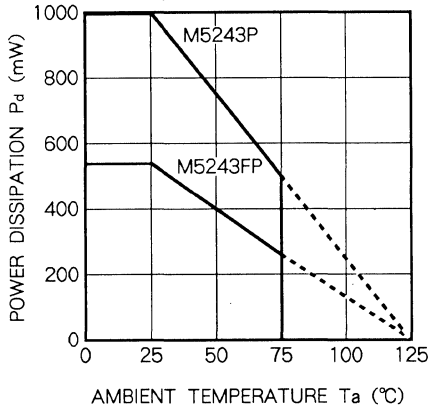


SWITCH MATRIX

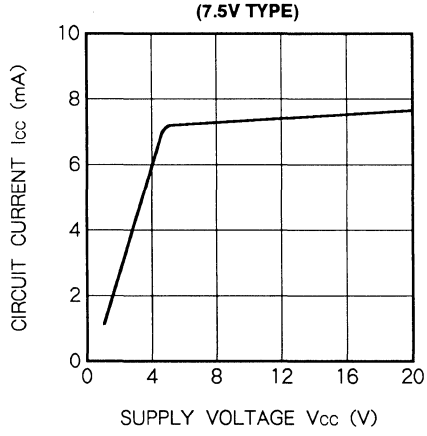
Parameter				Vcc	Rsw1	Rsw2	SW1	SW2-1	SW3-1	SW4-1	SW2-2	SW3-2	SW4-2	SW5	SW6	Remarks
Circuit current			Icc	ON	–	ch1 or 2	–	–	–	–	–	–	–	–	OFF	
Voltage gain	GV(FLAT)	ch1		ON	ch1	ch1	ON	2	2	2	–	–	–	ch1	ON	
		ch2		ON	ch2	ch2	ON	–	–	–	2	2	2	ch2	ON	
	GV(BOOST)	ch1	100Hz	ON	ch1	ch1	ON	1	2	2	–	–	–	ch1	ON	
			1kHz	ON	ch1	ch1	ON	2	1	2	–	–	–	ch1	ON	
			10kHz	ON	ch1	ch1	ON	2	2	1	–	–	–	ch1	ON	
		ch2	100Hz	ON	ch2	ch2	ON	–	–	–	1	2	2	ch2	ON	
			1kHz	ON	ch2	ch2	ON	–	–	–	2	1	2	ch2	ON	
			10kHz	ON	ch2	ch2	ON	–	–	–	2	2	1	ch2	ON	
	GV(CUT)	ch1	100Hz	ON	ch1	ch1	ON	3	2	2	–	–	–	ch1	ON	
			1kHz	ON	ch1	ch1	ON	2	3	2	–	–	–	ch1	ON	
			10kHz	ON	ch1	ch1	ON	2	2	3	–	–	–	ch1	ON	
		ch2	100Hz	ON	ch2	ch2	ON	–	–	–	3	2	2	ch2	ON	
			1kHz	ON	ch2	ch2	ON	–	–	–	2	3	2	ch2	ON	
			10kHz	ON	ch2	ch2	ON	–	–	–	2	2	3	ch2	ON	
Maximum output voltage VOM		ch1		ON	ch1	ch1	ON	2	2	2	–	–	–	ch1	ON	
		ch2		ON	ch2	ch2	ON	–	–	–	2	2	2	ch2	ON	
Total harmonic distortion THD (FLAT)		ch1		ON	ch1	ch1	ON	2	2	2	–	–	–	ch1	ON	BOOST : SW2~4① CUT : SW 2~4③
		ch2		ON	ch2	ch2	ON	–	–	–	2	2	2	ch2	ON	
Output noise voltage VNO (FLAT)		ch1		ON	VNO	ch1	OFF	2	2	2	–	–	–	ch1	ON	
		ch2		ON	VNO	ch2	OFF	–	–	–	2	2	2	ch2	ON	
Channel separation CS		ch1		ON	ch1	ch1	ON	2	2	2	–	–	–	ch1	ON	
		ch2		ON	ch2	ch2	ON	–	–	–	2	2	2	ch2	ON	
Ripple rejection RR		ch1		ON	HR	ch1	OFF	2	2	2	–	–	–	ch1	ON	
		ch2		ON	HR	ch2	OFF	–	–	–	2	2	2	ch2	ON	
Middle point voltage VM		ch1		ON	VM	VM	OFF	–	–	–	–	–	–	ch1	ON	
		ch2		ON	VM	VM	OFF	–	–	–	–	–	–	ch2	ON	

TYPICAL CHARACTERISTICS

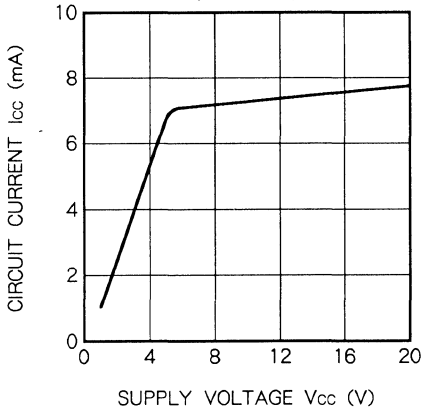
THERMAL DERATING (MAXIMUM RATING)



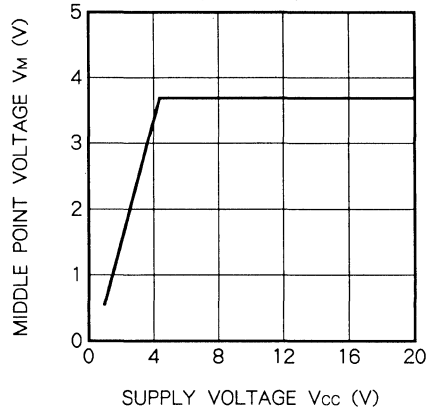
CIRCUIT CURRENT VS. SUPPLY VOLTAGE (7.5V TYPE)



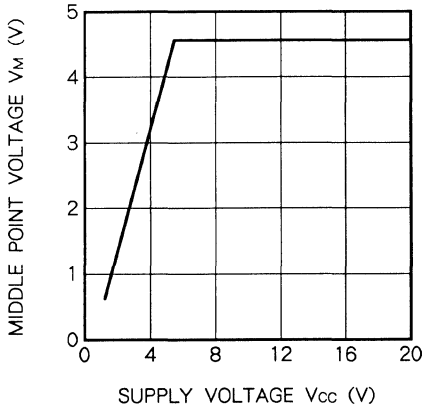
CIRCUIT CURRENT VS. SUPPLY VOLTAGE (9.0V TYPE)



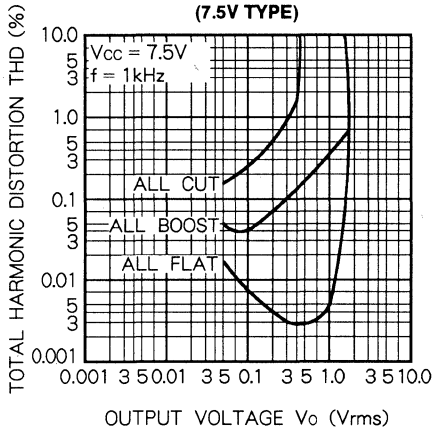
MIDDLE POINT VOLTAGE VS. SUPPLY VOLTAGE (7.5V TYPE)



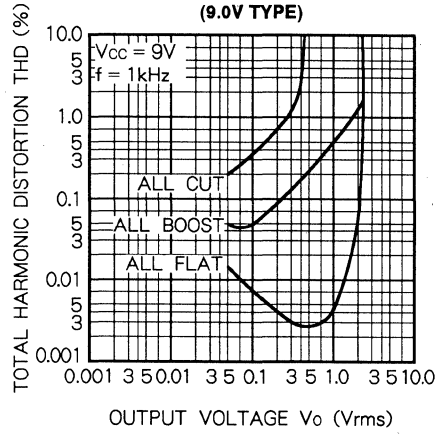
MIDDLE POINT VOLTAGE VS. SUPPLY VOLTAGE (9.0V TYPE)



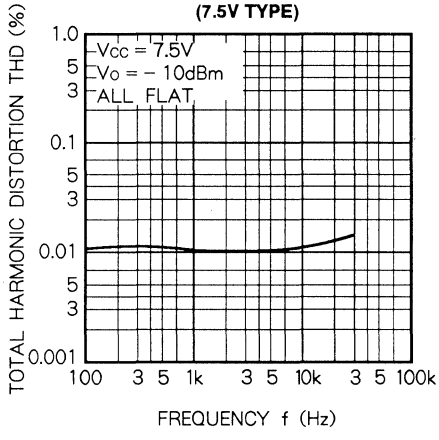
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE (7.5V TYPE)



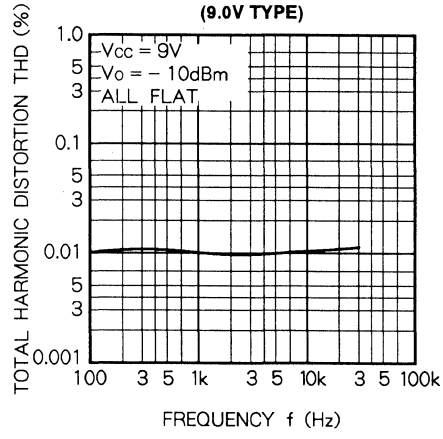
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE (9.0V TYPE)



TOTAL HARMONIC DISTORTION VS. FREQUENCY (7.5V TYPE)

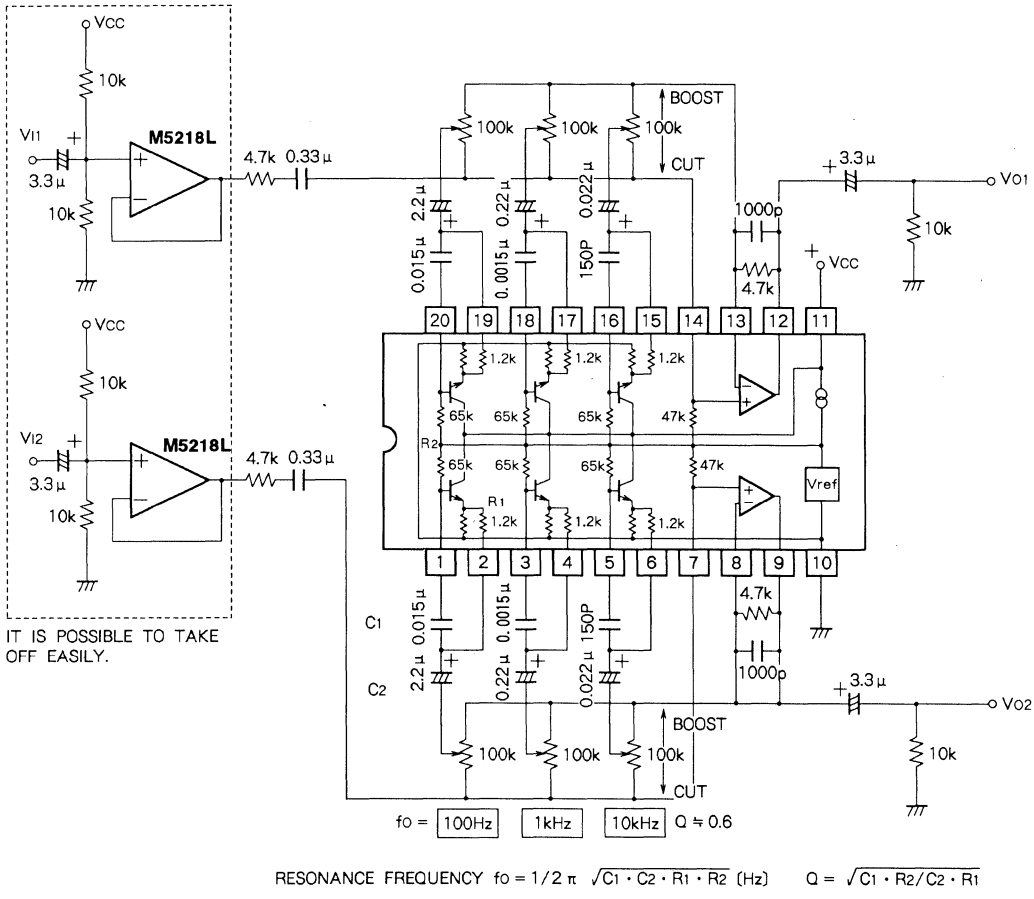


TOTAL HARMONIC DISTORTION VS. FREQUENCY (9.0V TYPE)



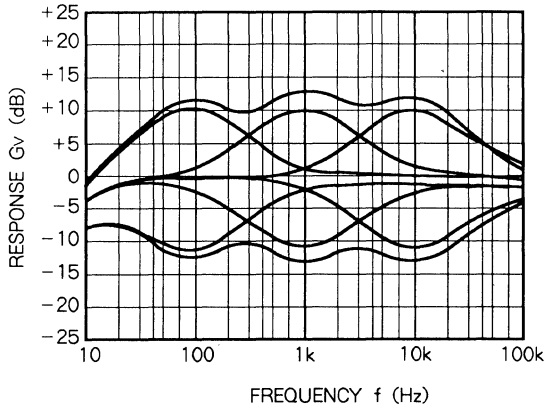
APPLICATION EXAMPLE – 1

3-Element graphic equalizer (Dual channel)



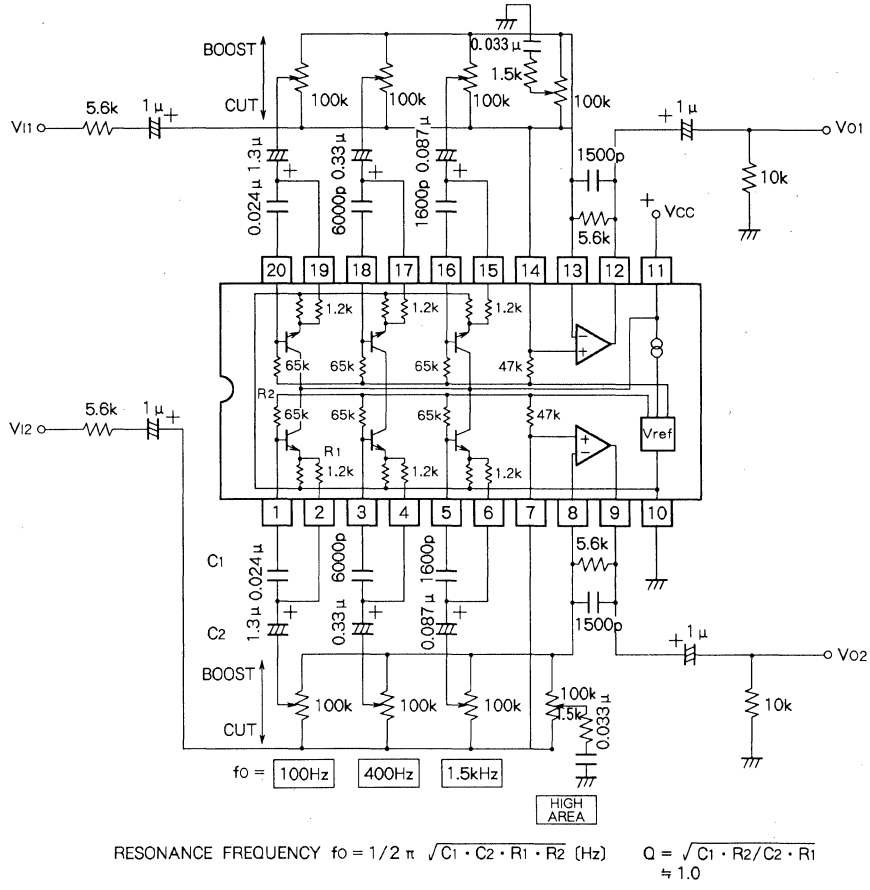
RESONANCE FREQUENCY $f_O = 1/2\pi \sqrt{C_1 \cdot C_2 \cdot R_1 \cdot R_2}$ (Hz) $Q = \sqrt{C_1 \cdot R_2 / C_2 \cdot R_1}$

FREQUENCY RESPONSE



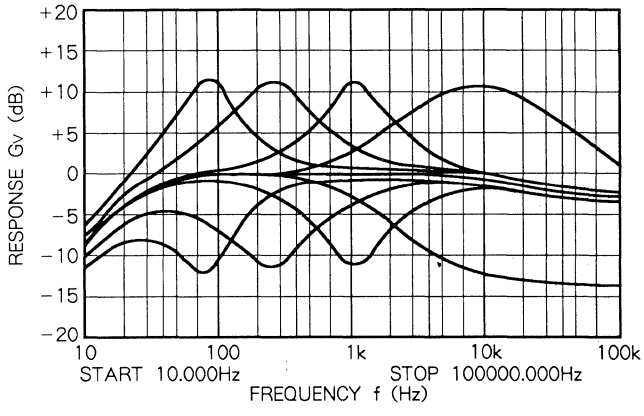
APPLICATION EXAMPLE – 2

Simplicity 4-element graphic equalizer (Dual channel)



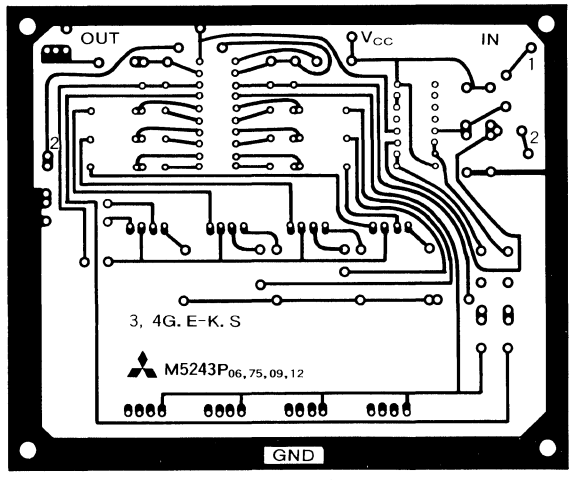
RESONANCE FREQUENCY $f_0 = 1/2\pi \sqrt{C_1 \cdot C_2 \cdot R_1 \cdot R_2}$ (Hz) $Q = \sqrt{C_1 \cdot R_2 / C_2 \cdot R_1} \fallingdotseq 1.0$

FREQUENCY RESPONSE

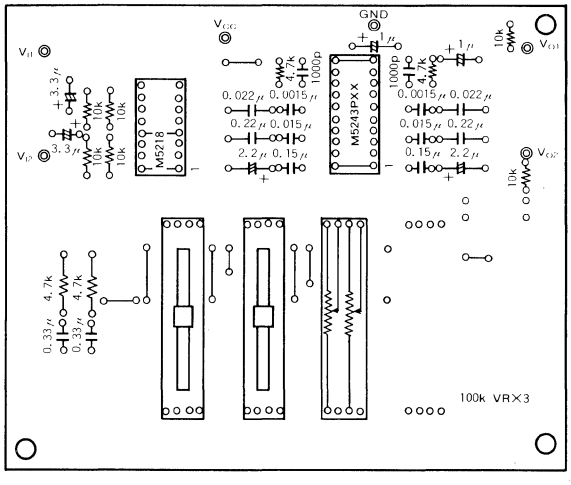


PCB FOR CIRCUIT TESTING

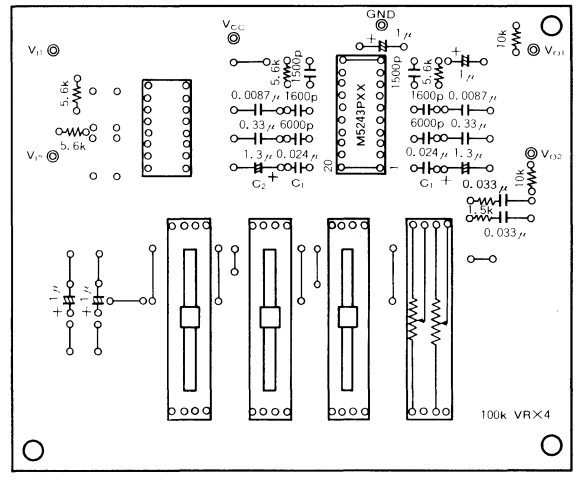
COPPER FOIL SIDE



(TYPICAL APPLICATION EXAMPLE)



(SIMMPLICITY 4-ELEMENT GRAPHIC EQUALIZER)



M5289P,FP

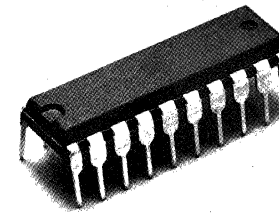
Hi-Fi 7-ELEMENT GRAPHIC EQUALIZER IC

DESCRIPTION

The M5289 is a 7-element graphic equalizer IC best suited to Hi-Fi audio systems. It has a built-in 7-element of transistor-based resonance circuits and an output OP amp.
The IC can be used in compact sets of high-density assemblies, modules, and hybrid ICs. Its applications cover Hi-Fi stereo sets, portable radio cassette tape players, car audio systems, music centers, and electronic instruments.

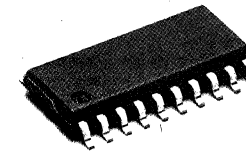
FEATURES

- Low distortion
  ····· THD = 0.001 %(M5289P), 0.003 %(M5289FP)(typ)
  (@f = 1kHz, Flat)
- Low noise ····· V_{NO} Flat = 3.5 μ Vrms(typ)
  High pressure proof (V_{CC} = ± 15V)
- Dynamic range is large ····· V_{OM} = 9.2Vrms(M5289P),
  2.0Vrms(M5289FP)(typ)
- Capable of being driven by single power supply single power (use GND pin ⑲ for V_{CC}/2 pin)
- Variable Gv by external resistance



Outline 20P4(P)

2.54mm pitch 300mil DIP
(6.3mm × 24.0mm × 3.3mm)



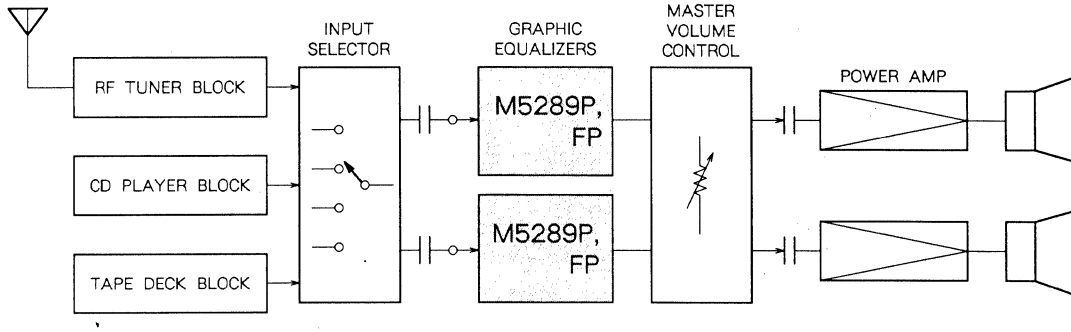
Outline 20P2N-A(FP)

1.27mm pitch 300mil SOP
(5.3mm × 12.6mm × 1.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC}, V_{EE} = ± 2 ~ ± 15V(4~30V)
Rated supply voltage ····· V_{CC}, V_{EE} = ± 15V
Rated power dissipation ····· 1000mW(P)
550mW(FP)

SYSTEM CONFIGURATION

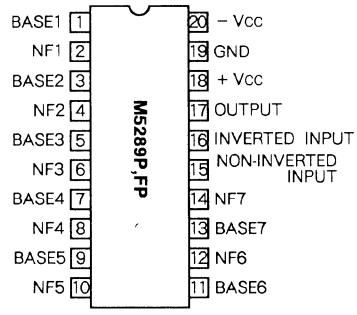


MITSUBISHI ELECTRIC

M5289P,FP

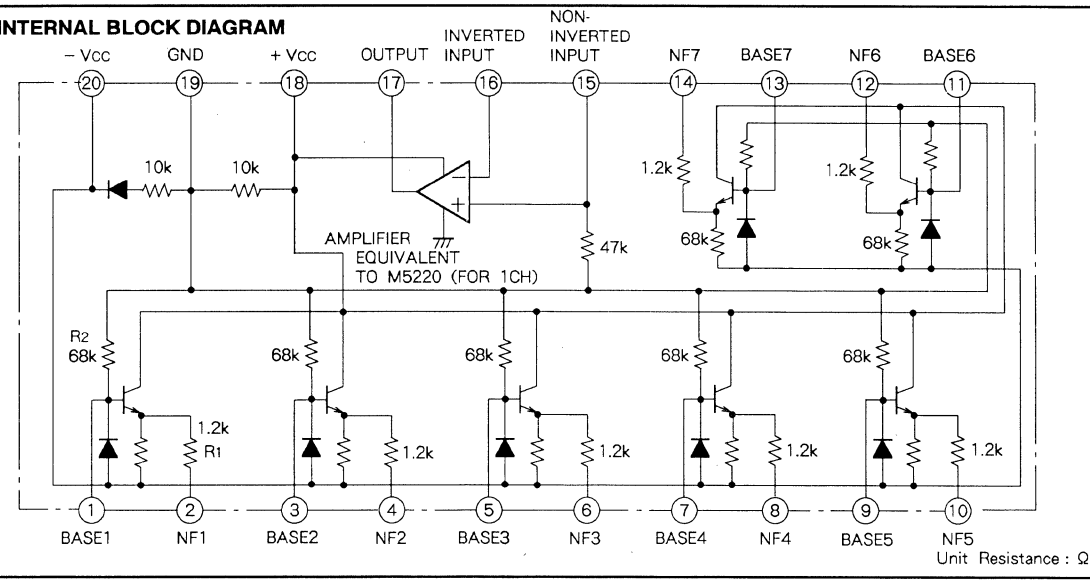
Hi-Fi 7-ELEMENT GRAPHIC EQUALIZER IC

PIN CONFIGURATION



Outline 20P4(P)
20P2N-A(FP)

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

M5289P,FP

Hi-Fi 7-ELEMENT GRAPHIC EQUALIZER IC

ABSOLUTE MAXIMUM RATING (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	36 (± 18)	V
I_{LP}	Load current	50	mA
P_d	Power dissipation	1000(P)/550(FP)	mW
T_{opr}	Operating temperature	− 20 ~ + 75	℃
T_{stg}	Storage temperature	− 55 ~ + 125	℃

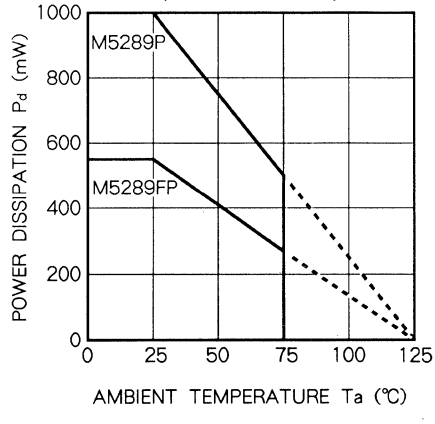
ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = ± 15V (M5289P), + 9V (M5289FP), unless otherwise noted)

Symbol	Parameter		Test conditions		f = (Hz)	Limits Min	Limits Typ	Limits Max	Unit
Icc	Circuit current		V_{in} = 0	V_{CC} = + 9V	−	4.4	6.8	10.5	mA
				V_{CC} = ±15V		11.3	17.8	24.5	
G_V (FLAT)	Voltage gain	Flat	V_{in} = − 10dBm		1k	− 3.0	− 0.5	+ 1.8	dB
$G_{V(BOOST)}$		Boost	V_{in} = − 10dBm, V_O (FLAT) = 0dB		61.7	7.5	10.5	13.1	dB
					156	7.5	10.5	13.1	
					412	7.5	10.5	13.1	
					1.08k	7.5	10.5	13.1	
					2.29k	7.5	10.5	13.1	
					6.17k	7.5	10.5	13.1	
					15.6k	7.5	10.5	13.1	
G_V (CUT)		Cut	V_{in} = − 10dBm, V_O (FLAT) = 0dB		61.7	− 13.1	− 10.5	− 7.5	dB
					156	− 13.1	− 10.5	− 7.5	
					412	− 13.1	− 10.5	− 7.5	
					1.08k	− 13.1	− 10.5	− 7.5	
					2.29k	− 13.1	− 10.5	− 7.5	
					6.17k	− 13.1	− 10.5	− 7.5	
					15.6k	− 13.1	− 10.5	− 7.5	
V_{OM}	Maximum output voltage		THD = 1 %	**M5289P**	1k	6.7	9.2	−	Vrms
				M5289FP		1.2	2.2	−	
THD	Total harmonic distortion		V_O = 1Vrms	**M5289P**	1k	−	0.001	0.05	%
				M5289FP		−	0.003	0.1	
V_{NO}	Output noise voltage		Input short BM : 10Hz ~ 30kHz flat			−	3.5	13.0	μ Vrms

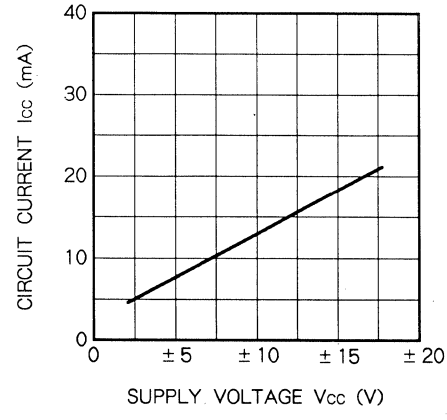
* Single power source V_{CC} = + 9V is standard for M5289FP because the power dissipation is limited to 550mW.

TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)

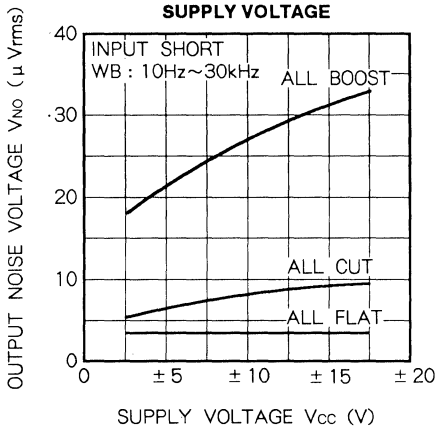


CIRCUIT CURRENT VS. SUPPLY VOLTAGE

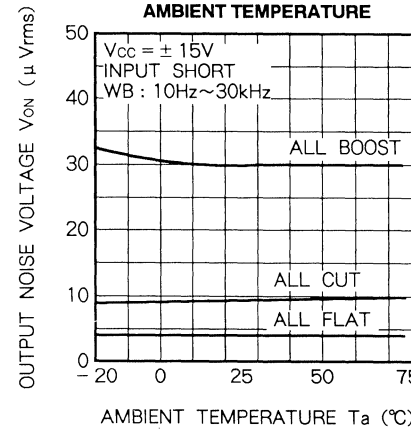


MITSUBISHI ELECTRIC

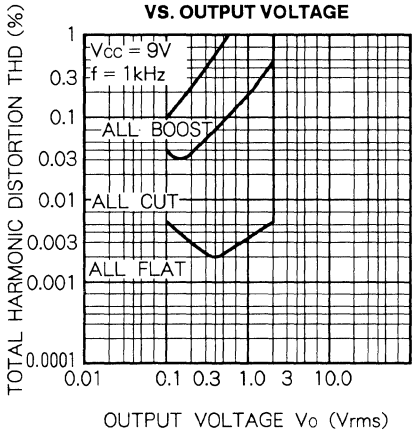
OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



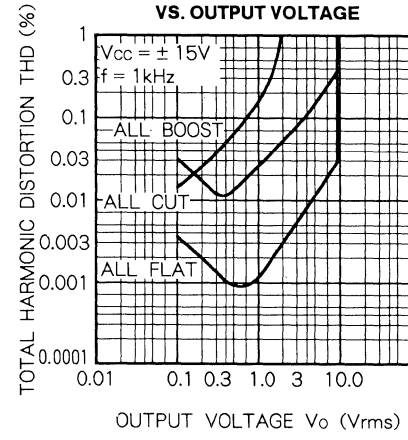
OUTPUT NOISE VOLTAGE VS. AMBIENT TEMPERATURE



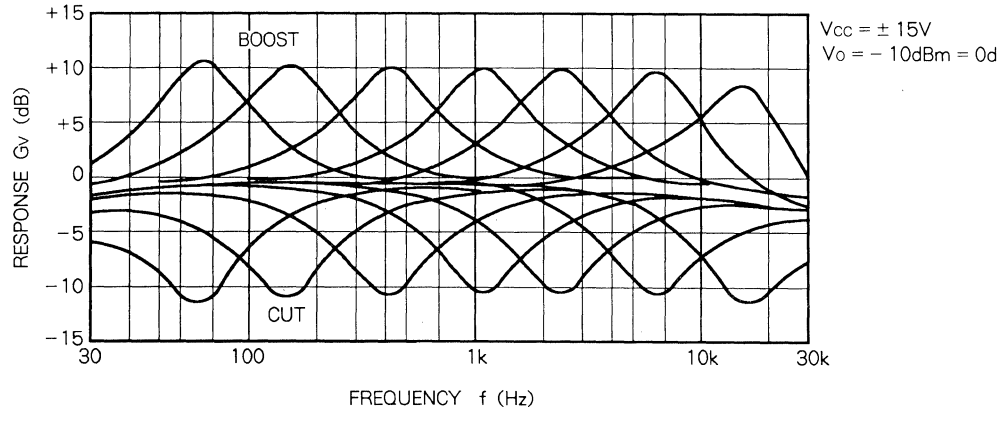
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



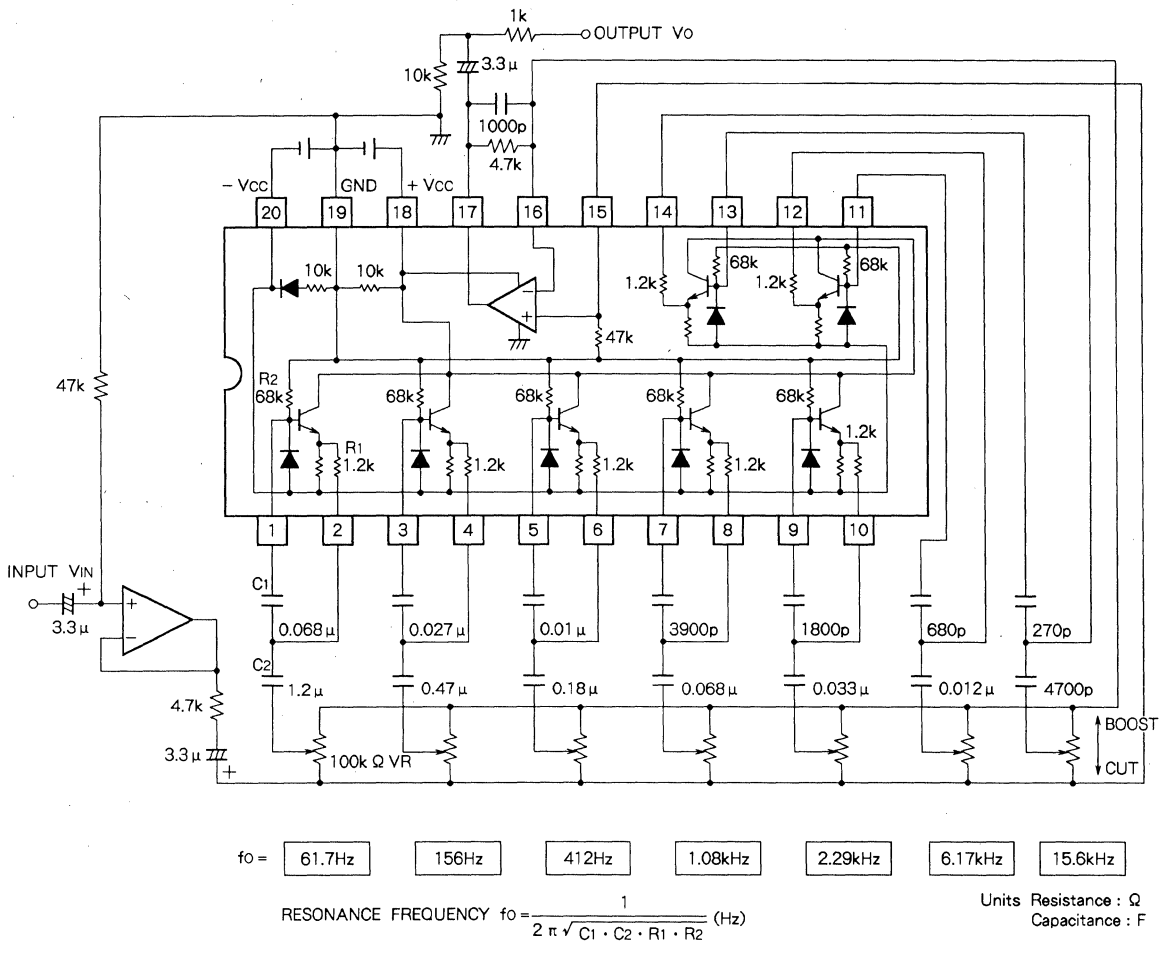
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



FREQUENCY CHARACTERISTIC



APPLICATION EXAMPLE



fo =	61.7Hz	156Hz	412Hz	1.08kHz	2.29kHz	6.17kHz	15.6kHz

RESONANCE FREQUENCY $fo = \frac{1}{2\pi\sqrt{C1 \cdot C2 \cdot R1 \cdot R2}}$ (Hz)

Units Resistance : Ω
Capacitance : F

1. M5289FP

Maximum rating of power dissipation P_d for M5289FP is 550mW. We recommend that you take notice of thermal deration well for your application.

CD LSI KIT

5

M50423FP

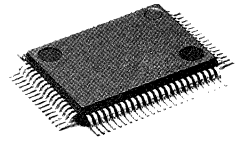
CD PLAYER DIGITAL SIGNAL PROCESSOR

DESCRIPTION

The M50423FP is a CMOS IC developed for compact disc (CD) sound reproducing applications. It has adjustment-free PLL, error correction circuitry, etc. and is used in a CD digital signal processing section. Applications include also CD-ROM and CD-G, as well as CD-DA.

FEATURES

- Adjustment free EFM-PLL circuit (built-in VCO)
- ±8 frames jitter margin
- Easy-to-handle CLV servo commands
- Subcode parallel/serial interface
- Selection available from 2 times and 4 times over sampling
- 18/20bit output available (with 4 times oversampling)
- Dual DAC output available (with 4 times oversampling)



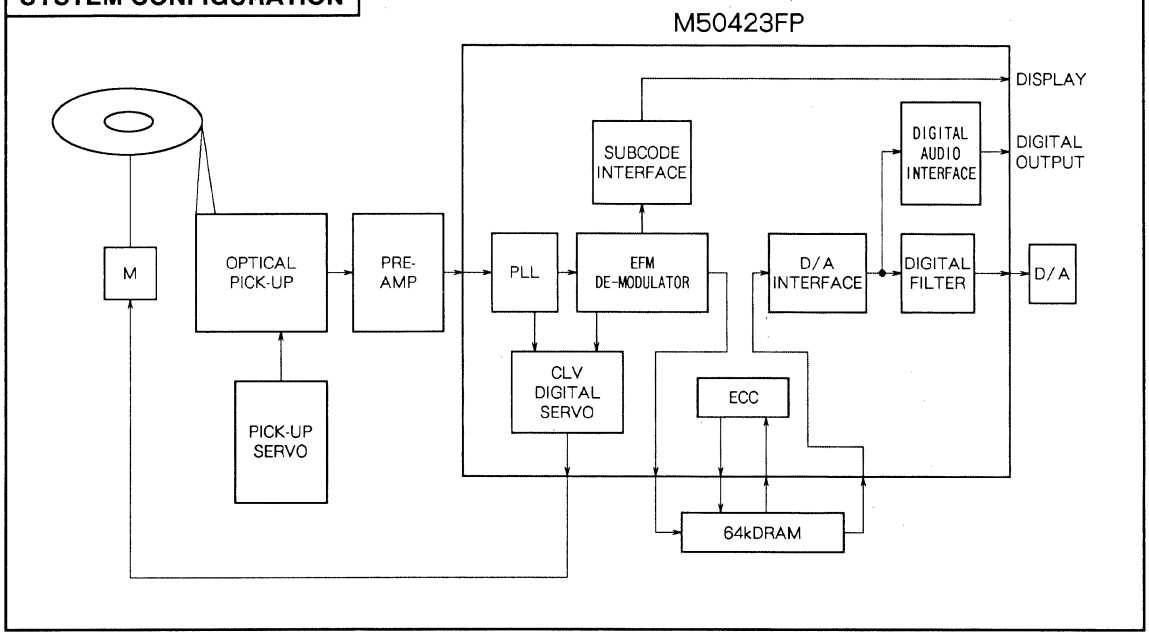
Outline 80P6-B

0.8mm pitch QFP
(20.0mm × 14.0mm × 2.15mm)

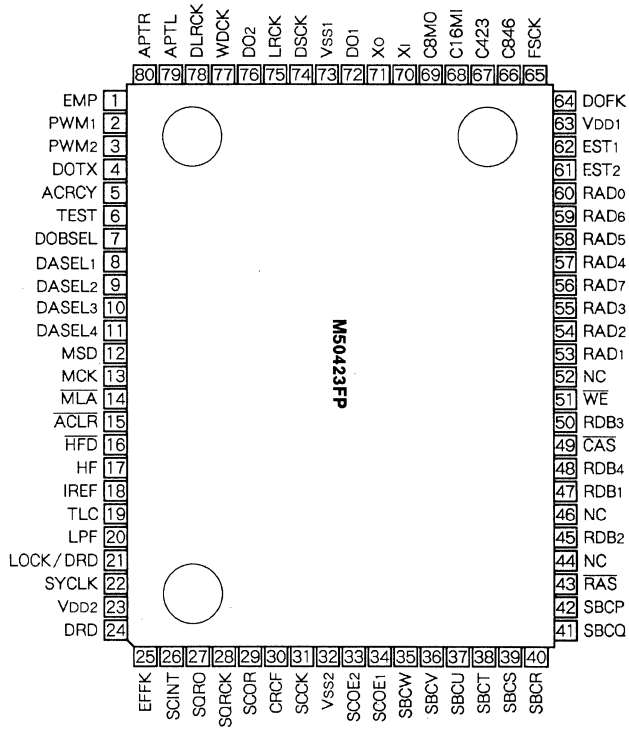
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{DD} = 4.5~5.5V
Rated supply voltage ..... V_{DD} = 5V
Rated power dissipation 90mW

SYSTEM CONFIGURATION



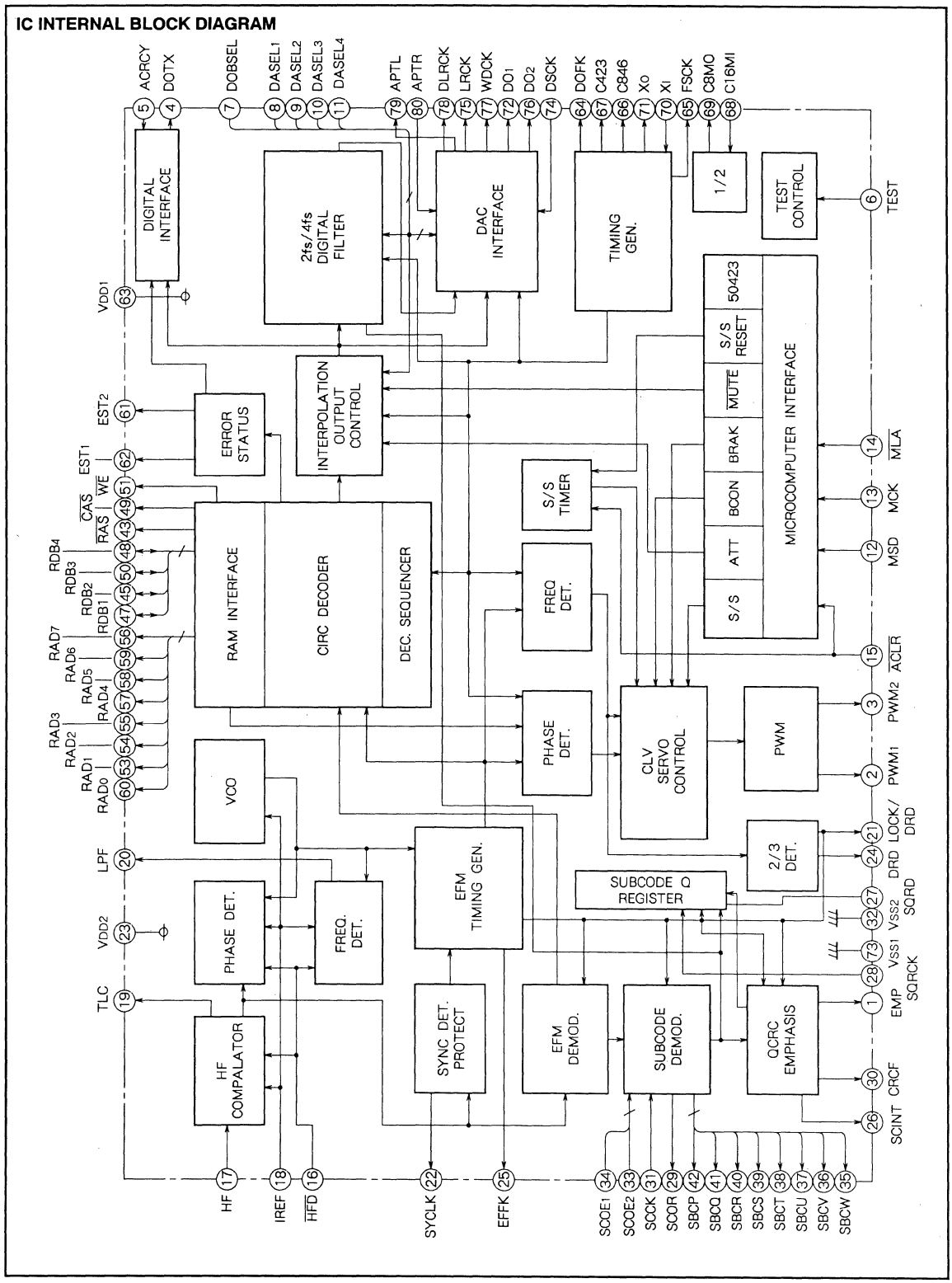
PIN CONFIGURATION



Outline 80P6-B

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Name	I/O	Function
EMP	O	Emphasis flag output. Emphasis = 1
PWM_1	O	Disc motor driving PWM output 1.−
PWM_2	O	Disc motor driving PWM output 2. +
DOTX	O	Output of digital interface
ACRCY	I	Clock accuracy input
TEST	I	Test control input. Normal = 0
DOBSEL	I	Data bit select 18bit = 1
$DASEL_1$	I	DAC interface format select 1
$DASEL_2$	I	DAC interface format select 2
$DASEL_3$	I	DAC interface format select 3
$DASEL_4$	I	DAC interface format select 4
MSD	I	Microcomputer interfece serial data input
MCK	I	Microcomputer interface shift cloc input
$\overline{MLA}$	I	Microcomputer interface data latch clock
$\overline{ACLR}$	I	Microcomputer interface register clear input
$\overline{HFD}$	I	High frequency signal detect
HF	I	High frequency signal input
IREF	I	Current referance
TLC	O	Output from slicon level control
LPF	I/O	PLL loop filter
LOCK/ DRD	O	Lock status/Disc rotation down signal output
SYCLK	O	Frame lock status output. Lock = 1
V_{DD2}	I	V_{DD} for data slicer and VCO
DRD	O	Disc rotation down signal output.
EFFK	O	EFM frame clock output duty ≒ 50 %
SCINT	O	Interrupt output of subcode Q
SQRO	O	Subcode Q register output
SQRCK	I	Subcode Q register
SCOR	O	Subcode sync output. S_0 + S_1
CRCF	O	Subcode Q CRC check flag output. CROCK = 1
SCCK	I	Shift clock input for serial subcode data output
V_{SS2}	I	Ground. 0V
$SCOE_2$	I	Enable input of subcode T∼Wch output. 0 : High Z
$SCOE_1$	I	Enable input of subcode P∼Sch output. 0 : High Z
SBCW	O	Subcode Wch output
SBCV	O	Subcode Vch output
SBCU	O	Subcode Uch output
SBCT	O	Subcode Tch output
SBCS	O	Subcode Sch output
SBCR	O	Subcode Rch output

Name	I/O	Function
SBCQ	O	Subcode Qch output
SBCP	O	Subcode Pch output. Pch∼Wch serial data output
$\overline{RAS}$	O	Row address strobe to RAM
NC	−	NO CONNECTION
RDB_2	I/O	Data input/output 2 to RAM
NC	−	NO CONNECTION
RDB_1	I/O	Data input/output 1 to RAM
RDB_4	I/O	Data input/output 4 to RAM
$\overline{CAS}$	O	Column address strobe signal output to RAM
RDB_3	I/O	Data input/output 3 to RAM
$\overline{WE}$	O	Write enable output to RAM
NC	−	NO CONNECTION
RAD_1	O	Address output 1 to RAM
RAD_2	O	Address output 2 to RAM
RAD_3	O	Address output 3 to RAM
RAD_7	O	Address output 7 to RAM
RAD_4	O	Address output 4 to RAM
RAD_5	O	Address output 5 to RAM
RAD_6	O	Address output 6 to RAM
RAD_0	O	Address output 0 to RAM
EST_2	O	Error status 2, Error to be interpolated detected at C2
EST_1	O	Error status 1, Error detected at C1
V_{DD1}	I	Power supply 5V
DOFK	O	OSC frame clock output. 7. 35kHz, duty=50%
FSCK	O	Clock output 44.1kHz (fs)
C846	O	Clock output. 8 4672MHz
C423	O	Clock output. 4 2336MHz
C16MI	I	1/2 divider input with internal feedback resistor
C8MO	O	1/2 divider output
X_I	I	Crystal oscillator input with internal feedback resistor
X_O	O	Crystal oscillator output
DO_1	O	Dual DAC Rch serial data output
V_{SS1}	I	Ground 0V
DSCK	O	Data shift clock to DAC
LRCK	O	Lch/Rch clock to DAC or APTL clock
DO_2	O	Dual DAC Lch serial data output
WDCK	O	Word clock to DAC or APTL clock
DLRCK	O	Lch/Rch clock
APTL	O	DAC sampling clock Lch
APTR	O	DAC sampling clock Rch

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Uniit
V_{DD}-V_{SS}	Supply voltage		− 0.3 ~ + 7.0	V
V_I	Input voltage	(R_P = 0 Ω)	V_{SS}-0.3 ≦ V_I ≦ V_{DD}+0.3	V
V_O	Output voltage	(R_P = 0 Ω)	V_{SS}-0.3 ≦ V_O ≦ V_{DD}	V
V_P	Pull up voltage		V_P ≦ V_{DD} + 2mA * R_P	V
T_{opr}	Operating temperature		−10 ~ +70	℃
T_{stg}	Storage temperature		−40 ~ +125	℃
P_d	Power dissipation		350	mW

R_P : Pull up resistor

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Applied pin	Limits			Unit
				Min	Typ	Max	
V_{DD}	Supply voltage			4.5	5.0	5.5	V
V_{IH1}	High-level input voltage 1		2)	V_{DD} *0.5	−	V_{DD}	V
V_{IH2}	High-level input voltage 2		1)	V_{DD} *0.7	−	V_{DD}	V
V_{IL1}	Low-level input voltage 1		2)	V_{SS}	−	V_{DD} *0.08	V
V_{IL2}	Low-level input voltage 2		1)	V_{SS}	−	V_{DD} *0.3	V
f_{OSC}	Oscillation frequency (X'tal)			−	8.46	−	MHz
f_{VCO}	Oscillation frequency (VCO)			−	8.64	−	MHz

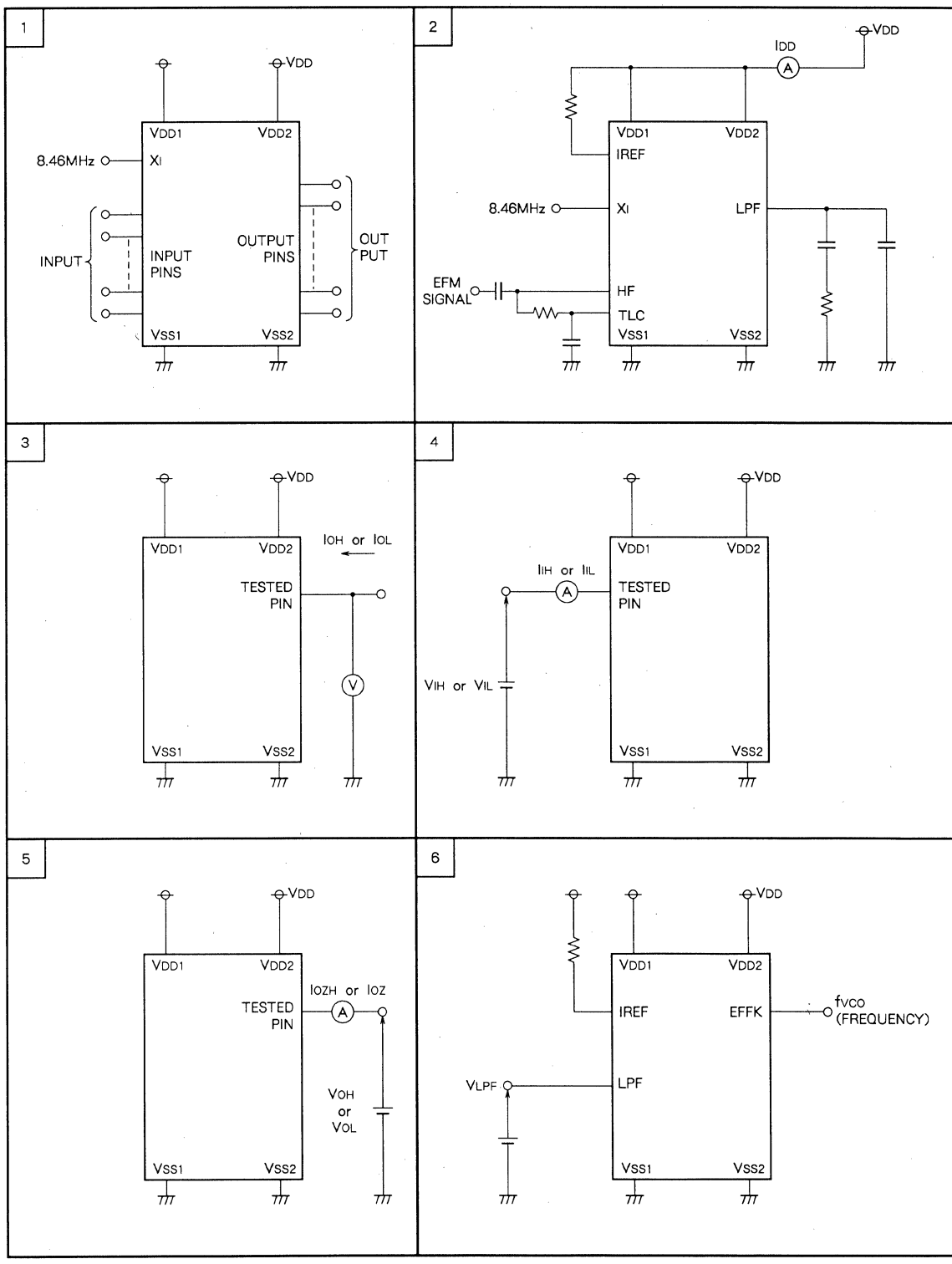
Note 1. Applied pin
1) DASEL1 ~ DASEL4, ACRCY, DOBSEL, TEST
2) $\overline{HFD}$, SCOE1, SCOE2, SCCK, MSD, MCK, $\overline{MLA}$, $\overline{ACLR}$, RDB1 ~ RDB4, SQRCK

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{DD} = 5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Applied pin	Test circuit	Limits			Unit
					Min	Typ	Max	
V_{DD}	Supply voltage	T_a = − 10 ~ + 70℃		1	4.5	5.0	5.5	V
I_{DD}	Circuit control	f_{OSC} = 8.4672MHz f_{VCO} = 8.6436MHz		2	−	18	40	mA
V_{OH}	High-level output voltage	V_{DD}=4.5V, I_{OH} = −0.8mA	3)	3	3.5	−	−	V
V_{OL}	Low-level output voltage	V_{DD}=4.5V, I_{OL} = 0.8mA	3)	3	−	−	0.4	V
I_{IH}	High-level intput current	V_{IH} = 4.5V	4)	4	−	−	2	μA
I_{IL}	Low-level intput current	V_{IL} = 0.5V	4)	4	−	−	− 2	μA
I_{OZH}	Off state high-level output current	V_{OH} = 4.5V	5)	5	−	−	2	μA
I_{OZL}	Off state low-level output current	V_{OL} = 0.5V	5)	5	−	−	− 2	μA
f_{VCO1}	VCO (EFFK) free running frequency	V_{LPF} = 1.0V		6	−	−	3.0	kHz
f_{VCO2}		V_{LPF} = 2.5V		6	7.8	9.5	−	kHz
f_{VCO3}		V_{LPF} = 4.0V		6	9.5	−	−	kHz

Note 2. Applied pin
3) Output and input/output pin except XO, TLC, LPF
4) Input pin except XI, C16MI, IREF
5) RDB1 ~ RDB4, SBCP ~ SBCW

TEST CIRCUIT



FUNCTIONAL DESCRIPTION

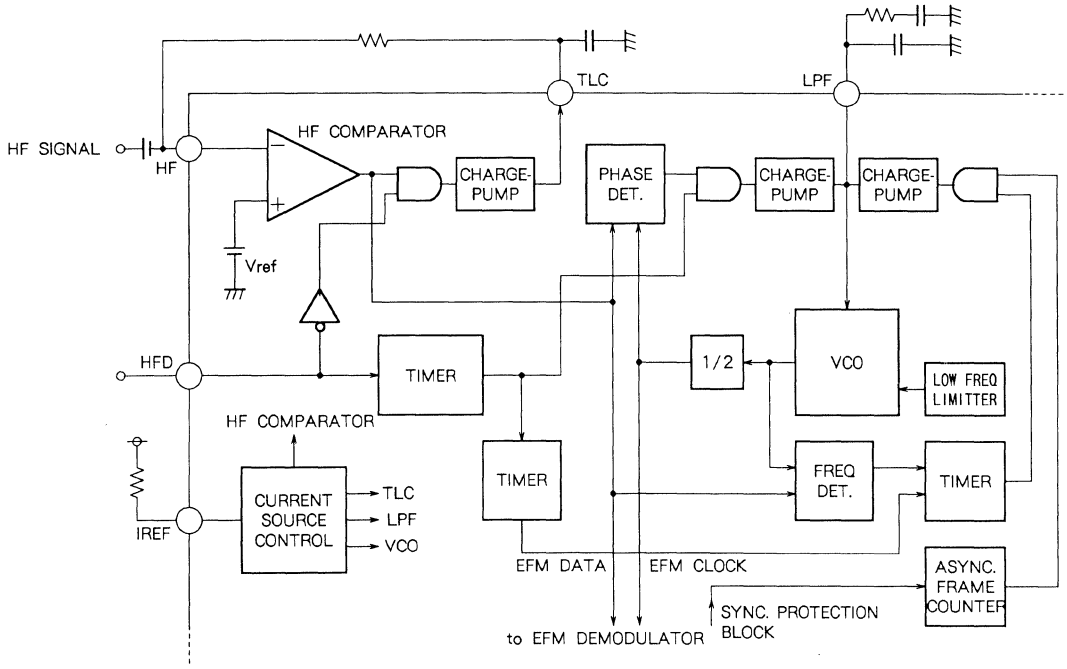
1. Data slicing/PLL

The M50423FP has an analog front-end for incoming HF (EFM) signal. Using CMOS-Analog technology, the front-end comprises an automatic slice level control circuit and EFM-PLL circuit with internal adjust-free VCO. The block-diagram shows the analog front-end. The HF signal is sliced by the HF comparator and a DC level is feed back from TLC to HF through the external CR. If HFD goes High because of a defect an disc, then TLC time off and holds the DC level.

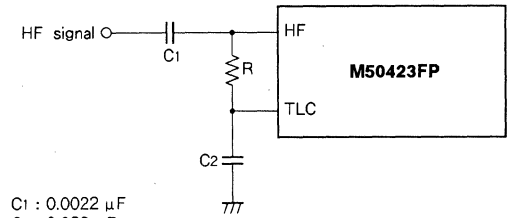
EFM-PLL extracts the EFM clock signal from the HF signal. The PLL circuit has a phase/frequency comparator not provides the M50423FP with a wide capture/lock range. There is no need to adjust the VCO. LPF is the charge-pump output and same-time control voltage input to the VCO. LPF turns off when HFD goes High.

IREF is the reference current input used to determine the current of charge pumps TLC and LPF, operating point of HF comparator, and VCO free running frequency. If IREF is connected to a noisy power supply through a resistor, VCO is modulated and the error-rate increases. Therefore, power supply noise at IREF must be held to a minimum.

BLOCK DIAGRAM (Data slicing/PLL)



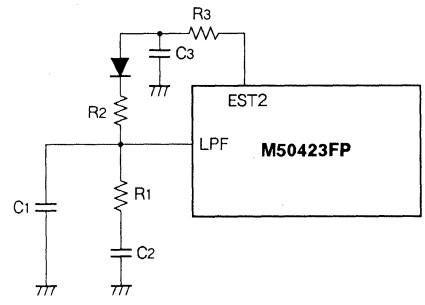
(1) Automatic slice level control



C1 : 0.0022 µF
C2 : 0.022 µF
R : 33k Ω
Vin : HF0.5VP-P Min

The slice level control circuit is formed by connecting a resistor and capacitors to the HF (High-Frequency signal input) and TLC (slice level control oputput) pins.

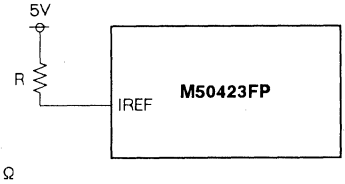
(2) PLL



C1 : 470pF
C2 : 0.15 µF
C3 : 1 µF
R1 : 2.2k Ω
R2 : 2.2M Ω
R3 : 1k Ω

Since the adjustment-free VCO is built in, the adjustment-free PLL circuit can be formed by connecting a resistor and capacitors to the LPF (low-pass filter) pin.

(3) Reference current



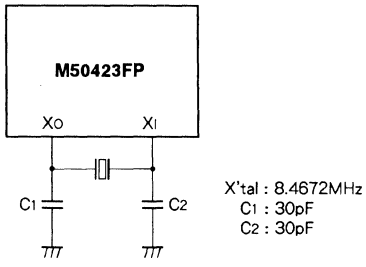
R : 120k Ω

A resistor must be connected between the IREF pin and V_{DD} in order to set the reference current used in determining the current values of the TLC pin and LPF pin, the comparator operating current of the slice level control circuit, and the VCO free-run frequency.

2. Demodulation/Decoding

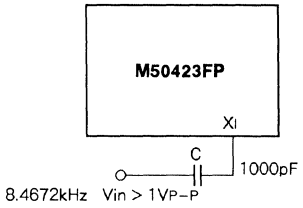
The EFM signal converted to logic level and the EFM clock extracted from the EFM signal are input to the demodulator and decoder block. The EFM demodulator must be synchronized to the EFM clock. The decoder uses the clock from the X'tal oscillator. Jitter between the EFM signal and output of the decoder is absorbed by external RAM.

(1) Clock generator



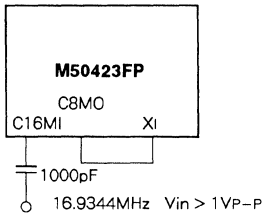
X'tal : 8.4672MHz
C1 : 30pF
C2 : 30pF

(a) The oscillation circuit can be formed by connecting a X'tal oscillator (8.4672MHz) and load capacitors to pins XI and XO.



(b) When the system contains a clock (8.4672MHz), the clock can be input to pin XI via a capacitor without using the X'tal oscillator.

If the input signal is logic level, the capacitor is not necessary



(c) When the system contains a clock (8.4672 × 2 = 16.9344MHz), the internal 1/2 divider can be used by connecting pin XI to pin C8MO and inputting the clock to pin C16MI via a capacitor.

The 1/2 divider between C16MI and C8MO can be used for any purpose, independent of other functions.

(2) Frame Synchronization

EFM demodulating is done by Programmable Logic Array conversion table. The demodulator must be synchronized to EFM signal for each frame. The frame sync protection circuit holds the synchronization and prevents false synchronization of the demodulator when bit-slipping or missynchronization occurs.

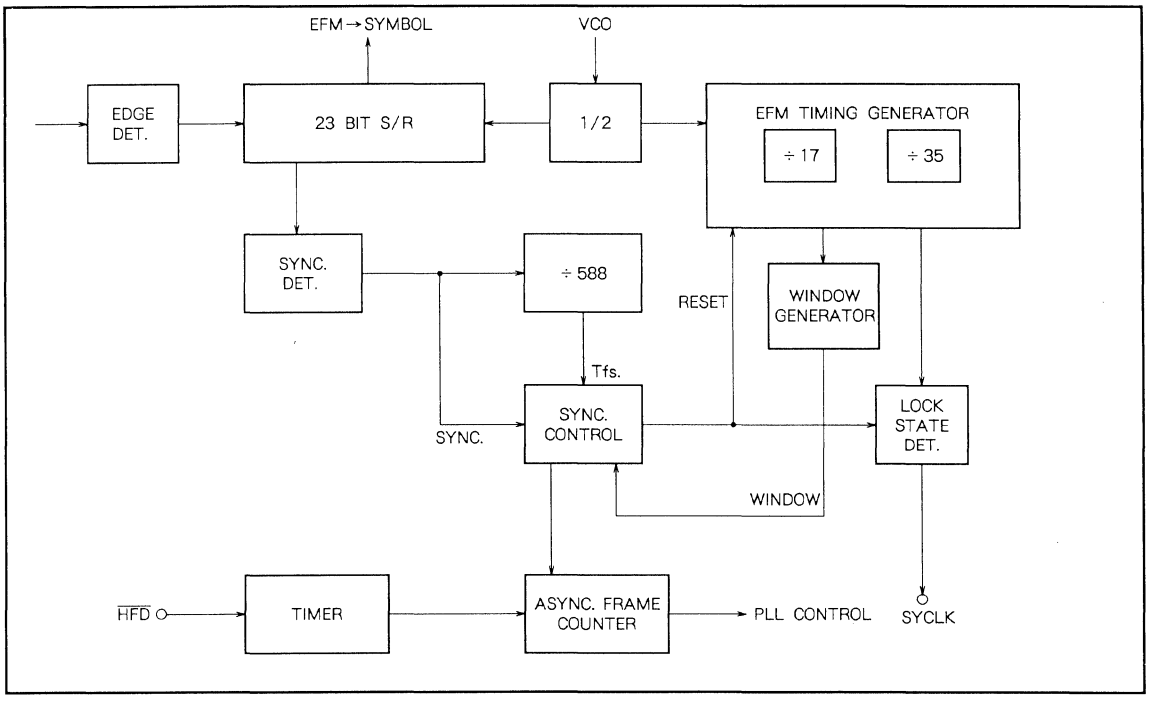


Fig. 1 Frame synchronization block diagram

The generating condition of the counter reset signal (Reset) in the EFM timing generator is indicated as follows:

Reset = (Sync * Tfs) + (Sync * Window)

* : Logical product

\+ : Logical sum

Sync : Synchronizing signal

Tfs : Detection signal of synchronizing signal space = 588

Window : Window signal ± 7ck

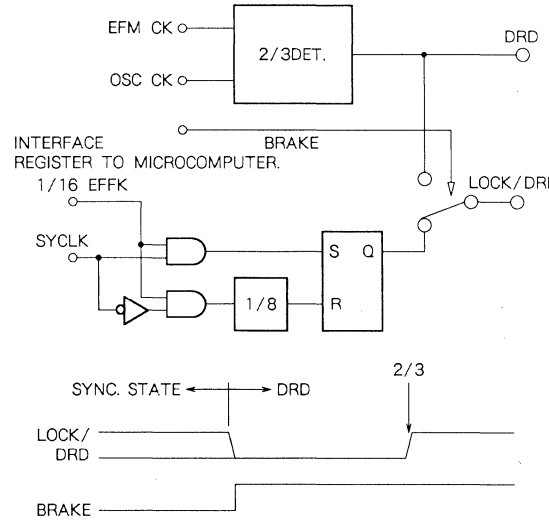
In the synchronous state, sync and Tfs generate simultaneously and sync comes to the center of the window. At this time, 1 is output to the SYCLK pin.

Frame sync status is output to SYCLK pin.

The SYCLK output includes some bounce even when the sync pattern is lost because of a defect an the disc. Hence, there is a need for debouncing the sync status signal for it to be monitored by the system control microcomputer.

Debouncing is in the M50423FP by monitoring the frame sync status at 1/16 EFM frame clock intervals and then outputting the result to the LOCK/DRD pin. If the monitored status is locked then output is High. Eight continuous unlocked outputs becomes Low.

LOCK/DRD pin outputs DRD signal (see Sec. 3) when the discmotor is braking by the command from microcomputer. The following pages contain the block diagram and the output timing.



(3) Subcode demodulation

Among data converted from 14-bits EFM signal to 8-bit symbols, subcodes P, Q, R, S, T, U, V and W are output to pins SBCP - SPCW respectively. When the subcode synchronizing patterns S_0 or S_1 is detected as synchronizing signal of subcode data, the synchronizing signals are output to the SCOR pin.

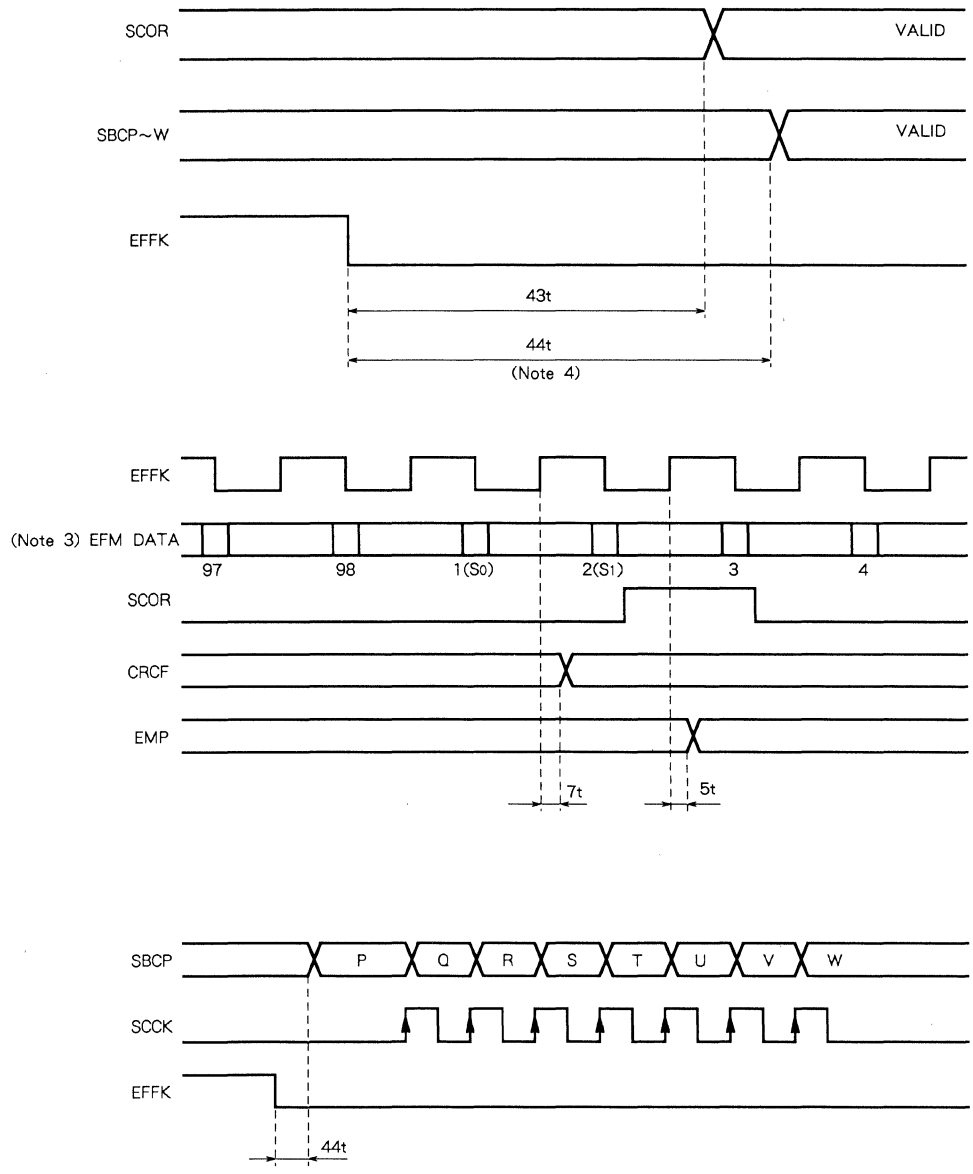
Pins SBCP - SBCW are a Three - State output system controlled by pins, $SCOE_1$ and $SCOE_2$ as shown in the table below.

A CRC check is made for the Q channel data, and if the data is correct, a 1 is output to the CRCF pin. The EMP pin displays whether or not emphasis is present. The subcode data is not only output in parallel, but also can be obtained serially via SBCP, by inputting a clock to SCCK.

Subcode output timing are shown Fig. 2.

SUBCODE DEMODULATION

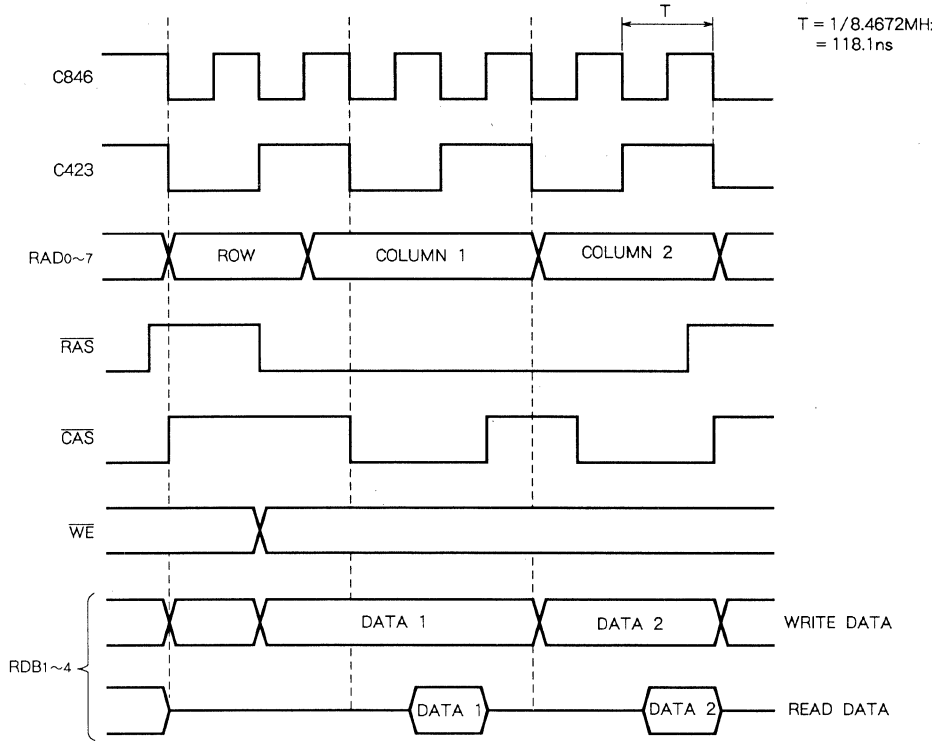
$SCOE_1$	$SCOE_2$	SBCP	SBCQ	SBCR	SBCS	SBCT	SBCR	SBCV	SBCW
0	0	High-impedance				High-impedance			
1	0	P	Q	R	S	High-impedance			
0	1	High-impedance				T	U	V	W
1	1	P	Q	R	S	T	U	V	W



Note 3. Subcode block No. in the EFM data
4. t : Oscillating frequency (VCO)
(typically : 1/8.6436MHz = 115.7ns.)
5. When input frequency to SCCK is more than 8ck, SBCP becomes 0.

Fig. 2 Subcode output timing

(a) Symbol data/flag, read/write timing



(b) C1/C2 flag, read/write timing

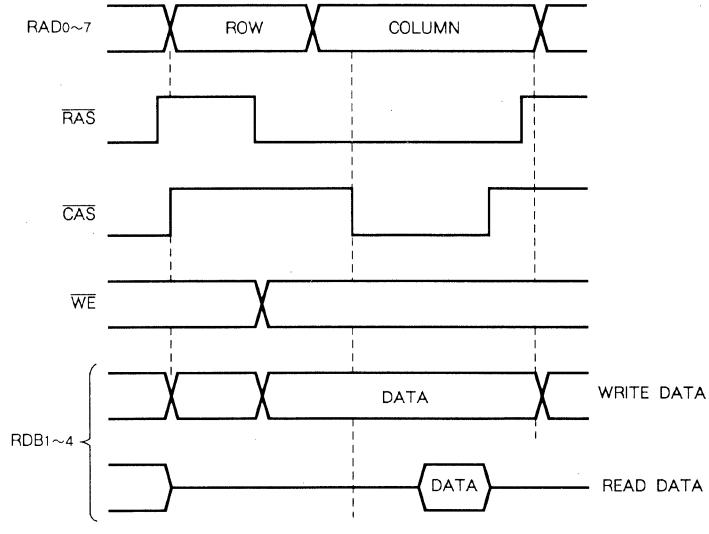


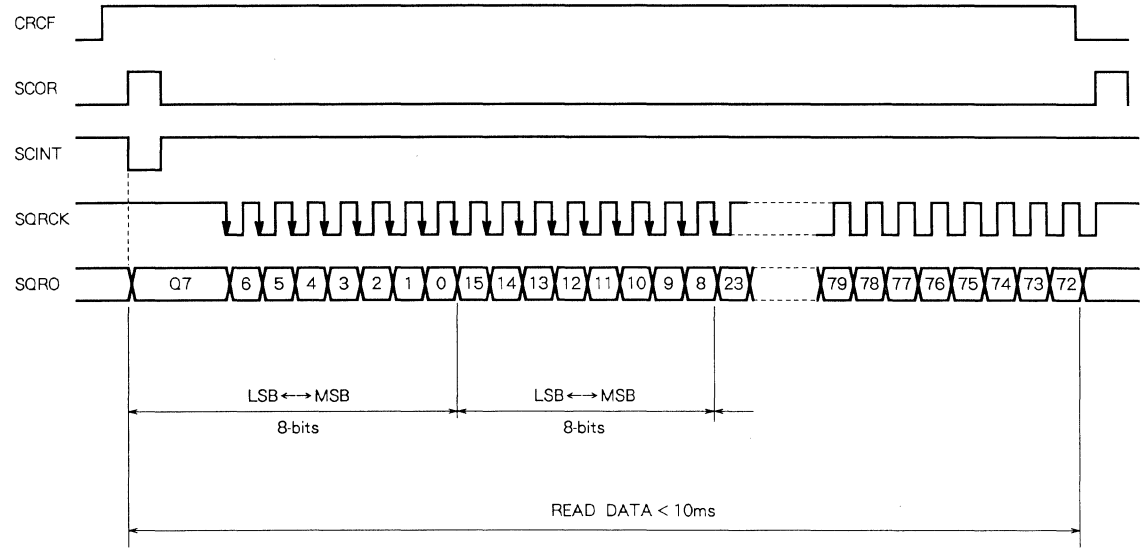
Fig. 3 RAM interface timing

(4) Subcode Q register

Subcode Q-channel data are output to SBCQ pin.

The M50423FP stores the Q data in an 80-bit shift register and if CRC is OK, the system control microcomputer can access the Q data from the SBCQ pin by inputting the read-out clock to SQRCK pin. If the CRC check is OK, the M50423FP outputs the interrupt signal to the micro-computer from SCINT, synchronaized with SCOR (Subcode sync.) signal.

Timing chart



(5) RAM interface/CIRC decoding

A 64K (4 × 16K) /256K (4 × 64K) dynamic RAM is needed as the external memory for temporary storage to process CIRC decoding (C1 decoding, C2 decoding, unscramble and de-interleave) and output interpolation.

By using a 64K/256K RAM, jitter is absorbed up to ±8 frames (max.).

Fig. 3 shows the timing for reading from and writing to the RAM.

Dowing CIRC decoding, double error correction is used for both C1 and C2 decoding.

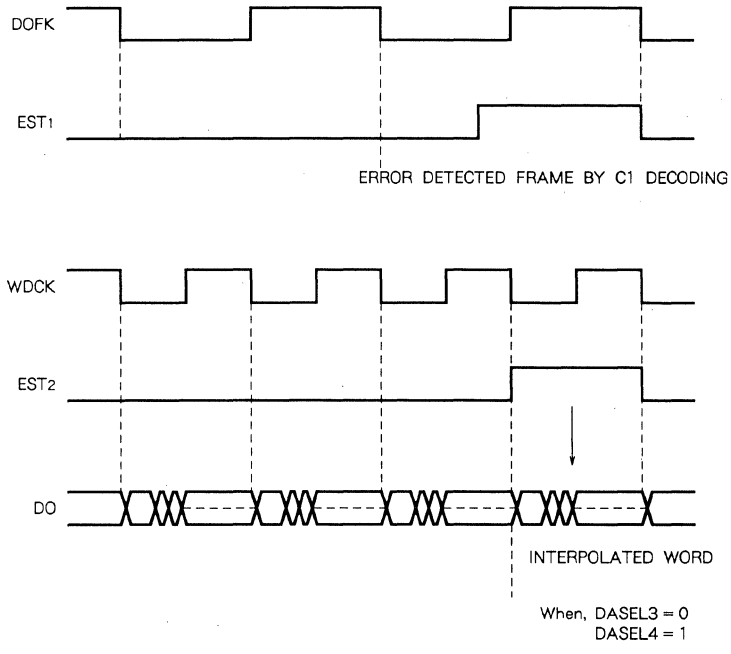
When correction is not possible, average interpolation or pre-hold interpolation is perfomed.

Error states which are detected during decoding are output to pins EST_1 and EST_2.

When an error is detected by C1 decoding, 1 is output to pin EST_1. When an error word is judged incorrectable by C2 decoding, a "1"is output to pin EST_2.

The output timings for pins EST_1 and EST_2 are as follows:

Timing chart

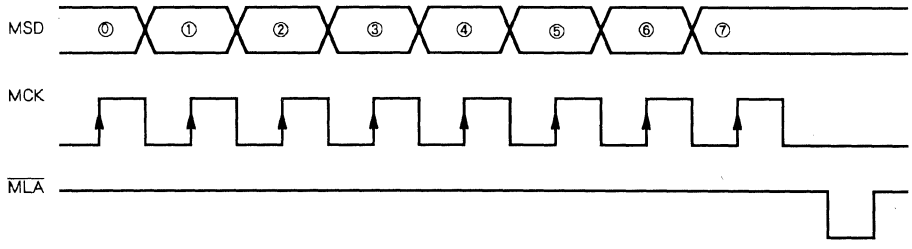


3. Microcomputer Interface

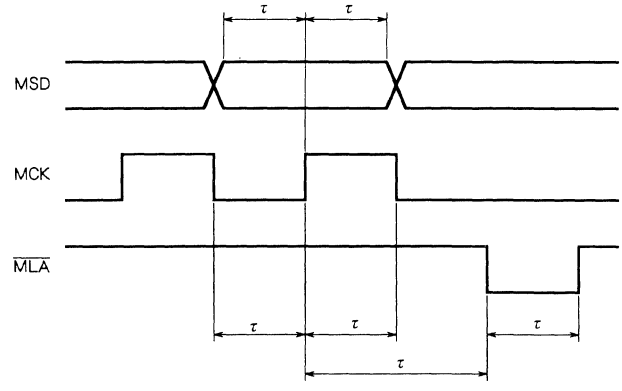
CLV servo, MUTE, and ATT system are controlled by serial commands from the microcomputer.

The timing, names, and functions of each control register are as follows :

Timing chart



⓪ DUMMY (Don't care)	X
① S/S(START/STOP) register	start = 1
② BCON(BRAKECONTROL) register	enable = 1
③ BRAK (BRAKE) register	brake = 1
④ ATT (ATTENUATE) register	−12dB = 1
⑤ $\overline{\text{MUTE}}$ register	muting = 0
⑥ S/S timer reset register	reset = 1
⑦ IC code	M50423FP = 1



τ min : 500ns

Function of microcomputer interface register

Register No.	Register name	Function	Operation		Note
			0	1	
⓪	DUMMY	Don't care	–	–	
①	S/S (START/STOP)	Controls START/STOP of the disk motor	DISC MOTOR STOP (OFF)	DISC MOTOR START (ON)	0 by $\overline{ACLR}$
②	BCON (BRAKECONTROL)	Determines if BRAKE control is necessary	BRAKE 0.3sec.	BRAKE is controlled by BRAK register	0 by $\overline{ACLR}$
③	BRAK (BRAKE)	Controls BRAKE	BRAKE OFF (MOTOR OFF)	BRAKE ON	When BCON = 1
④	ATT (ATTENUATE)	Sets attenuation (−12dB)	0dB	− 12dB	When MUTE = 1
⑤	MUTE	Sets the muting	− ∞ dB	0dB	0 by $\overline{ACLR}$
⑥	S/S timer reset	Resets the S/S timer which sets the time of KICK and BRAKE to 0.3sec.	S/S timer enable	S/S timer disable	1 by $\overline{ACLR}$
⑦	IC code	Distinguishes the command to the M50423FP	–	Excuting command	0 is code for M51564P

Examples of system control are as follows :

Operation \ Register name	⓪ DUMMY	① S/S	② BCON	③ BRAK	④ ATT	⑤ $\overline{MUTE}$	⑥ S/S timer reset	⑦ IC code
								0
MUTE						0		1
ATT					1	1		1
0.3sec.KICK→CLV		1					0	1
0.3sec.BRAKE→MOTOR OFF		0	0				0	1
BRAKE		0	1	1			0	1
MOTOR OFF		0	1	0			0	1
0.3sec. timer disable							1	1
MOTOR off (without 0.3sec. BRAKE)		0	0				1	1
CLV (without 0.3sec. KICK)		1	0				1	1
The following is example of the most simplified system control sequence.								
STOP		0	0	0	0	0	1	1
0.3sec. KICK→CLV		1	0	0	0	0	0	1
PLAY		1	0	0	0	1	0	1
FF/FR		1	0	0	1	1	0	1
PLAY		1	0	0	0	1	0	1
0.3sec. BRAKE→STOP		0	0	0	0	0	0	1

* The blanks mean "Don't care"or that other commands can be used simultaneously.
* KICK period can be extended by repetition of start procedure.
* The software developed on the M50421P/M50422P can be utilized on the M50423FP (upward compatible). However, when using this software, the following functions on the M50423FP are not available : subcode Q-register, subcode Q-interrupt signal LOCK/DRD output.

When the M50423FP detects that the number of rotations is less than 2/3 that of the normal play state, it output the disc rotation deterioration signal to the DRD pin.

By using this signal in the following stop sequence, the disc can be correctly stopped.

Operation or μ-COM Operation \ Register name	⓪ DUMMY	① S/S	② BCON	③ BRAK	④ ATT	⑤ $\overline{MUTE}$	⑥ S/S timer reset	⑦ IC code
PLAY		1	0	0	0	1	0	1
BRAKE		0	1	1	0	0	0	1
($\overline{HFD}$: H checking by microcomputer)								
(Measuring t_{DRD} (DRD : 0→1) after BRAKE start								
(Stop $\overline{HFD}$ checking and) additional BRAKE time 2 × t_{DRD}								
MOTOR OFF		0	1	0	0	0	0	1

The DRD signal is output to both the DRD pin and also the LOCK/DRD pin during the braking period.

In order to re-initiative the microcomputer interface register execute $\overline{ACLR}$ (M50423FP clear) immediately after turning the power on.

4. Digital filter

The M50423FP converts the sampling frequency of audio data from 44.1kHz (fs) to 88.2kHz (2fs) or 176.4kHz (4fs) by an overflow limited, FIR linear-phase digital filter.

Digital filter selection is done using pins DASEL1~DASEL4. Table1 shows the digital filter and DAC interface mode. Digital filter pass mode with no interpolation of umcorrectable data is designed for non-audio applications such as CD-ROM or CD-1. The digital filter pass mode with interpolation is used external precision digital filter applications.

Fig. 4 (a) shows the characteristics of the 2fs digital filter.

Fig.4 (b) shows the characteristics of the 4fs digital filter.

5. D-A Converter Interface

The M50423FP has many different DAC Interface formats. The desired format is selected using pins DASEL1~DASEL4.

Timing signals, data and clock automatically change to correspond to which digital filter, fs (pass) / 2fs / 4fs, is chosen.

If the 4fs digital filter mode is selected then the dual DAC mode and 18-bits data out mode are available.

Table 1 shows the interface modes.

Fig. 5 (a) ~Fig. 5 (e) show the timings if interface to DAC.

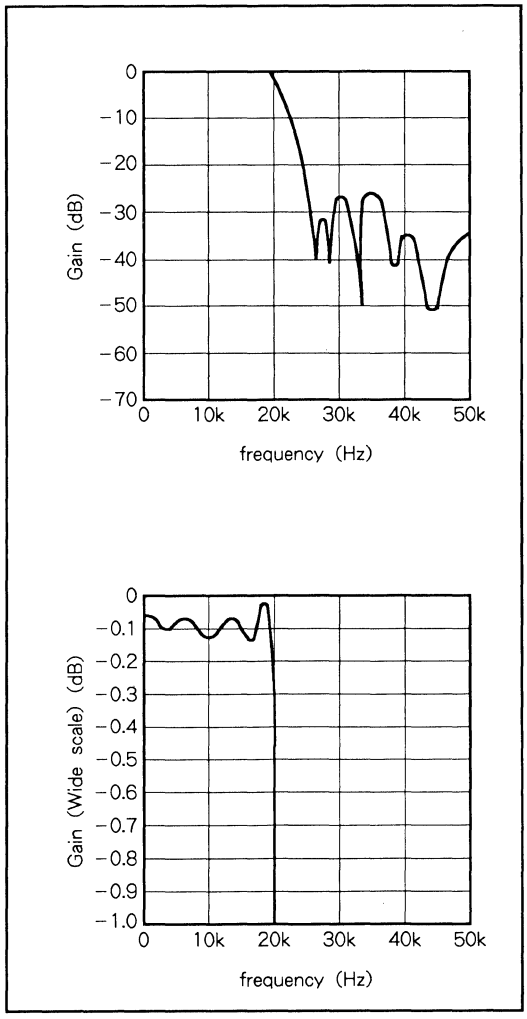


Fig. 4 (a) Frequency characteristics of the digital filter (Sampling frequency 88.2kHz:2fs)

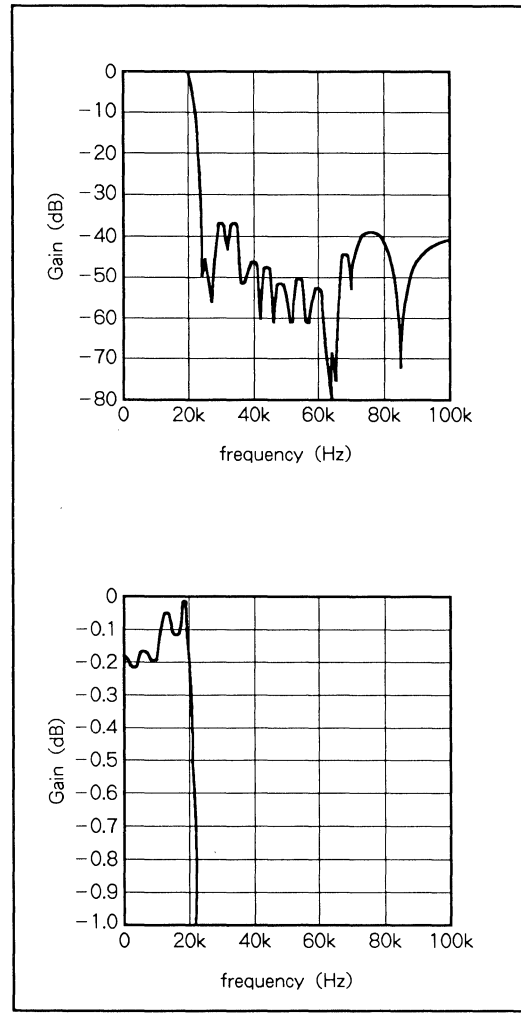


Fig. 4 (b) Frequency characteristics of the digital filter (Sampling frequency 176.4kHz:4fs)

Table 1 DAC interface modes

MODE	DASEL 1	DASEL 2	DASEL 3	DASEL 4	DF	MSB/LSB 1st	Note	Timing chart
1	0	0	0	0	2fs	MSB 1st		Fig. 5 (a)
2	0	0	0	1	(fs)	MSB 1st	Bypass filter	Fig. 5 (a)
3	1	0	0	0	2fs	LSB 1st		Fig. 5 (b)
4	1	0	0	1	(fs)	LSB 1st	Bypass filter	Fig. 5 (b)
5	1	0	1	0	4fs	MSB 1st		Fig. 5 (c)
6	1	0	1	1	4fs	MSB 1st	Dual DAC	Fig. 5 (d)
7	0	1	0	1	(fs)	MSB 1st	No interpolation	Fig. 5 (a)
8	1	1	0	0	2fs	MSB 1st		Fig. 5 (e)
9	1	1	0	1	(fs)	MSB 1st	Bypass filter	Fig. 5 (e)

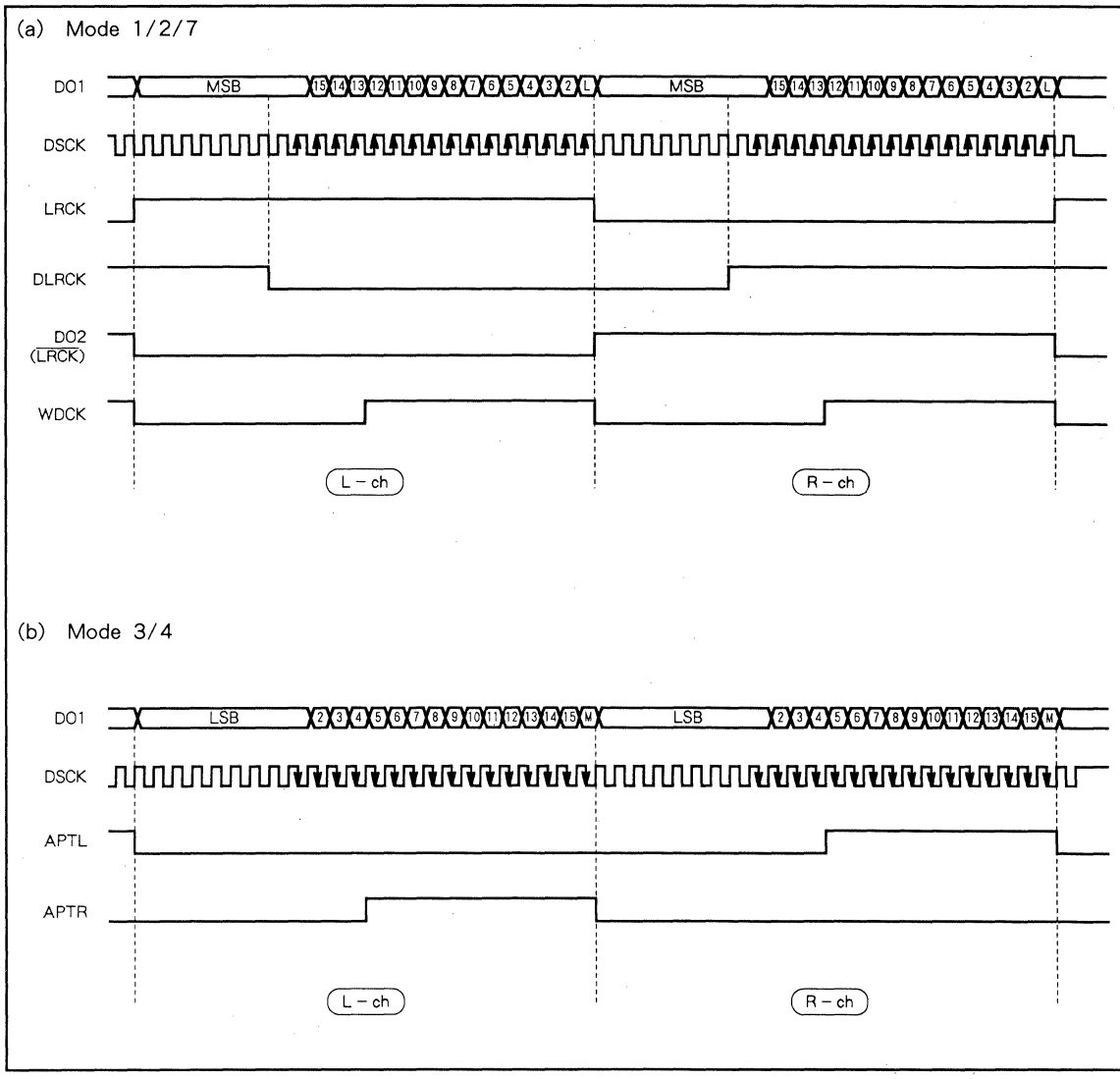


Fig. 5 DAC interface timing chart

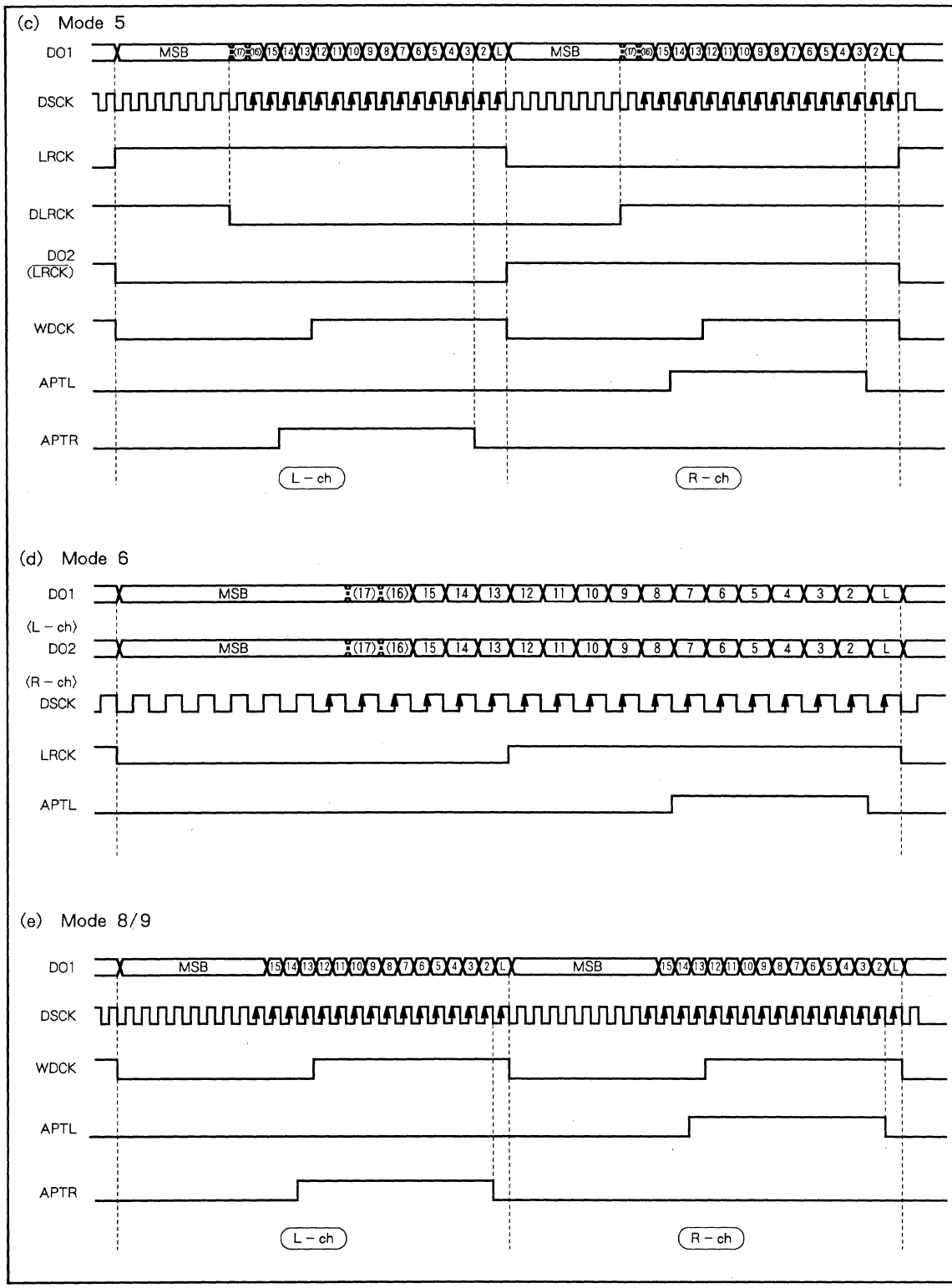


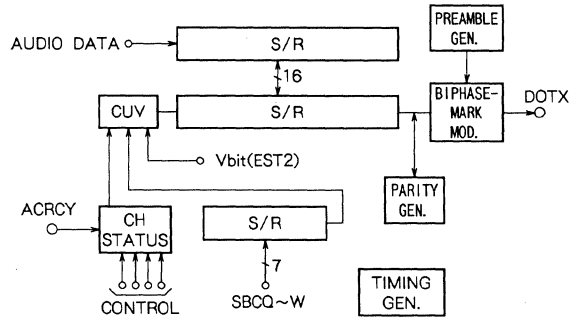
Fig. 5 DAC interface timing chart

6. Digital interface output

The M50423FP outputs digital interface signal conforming to EIAJ CP-340 or IEC formats.

The block diagram shows the digital interface and Fig. 6 shows the timings. Channel status clock accuracy can handle variable pitch control and can be set using the ACRCY pin.

The clock accuracy is level II when ACRCY pin is Low, and level III when ACRCY pin is High.



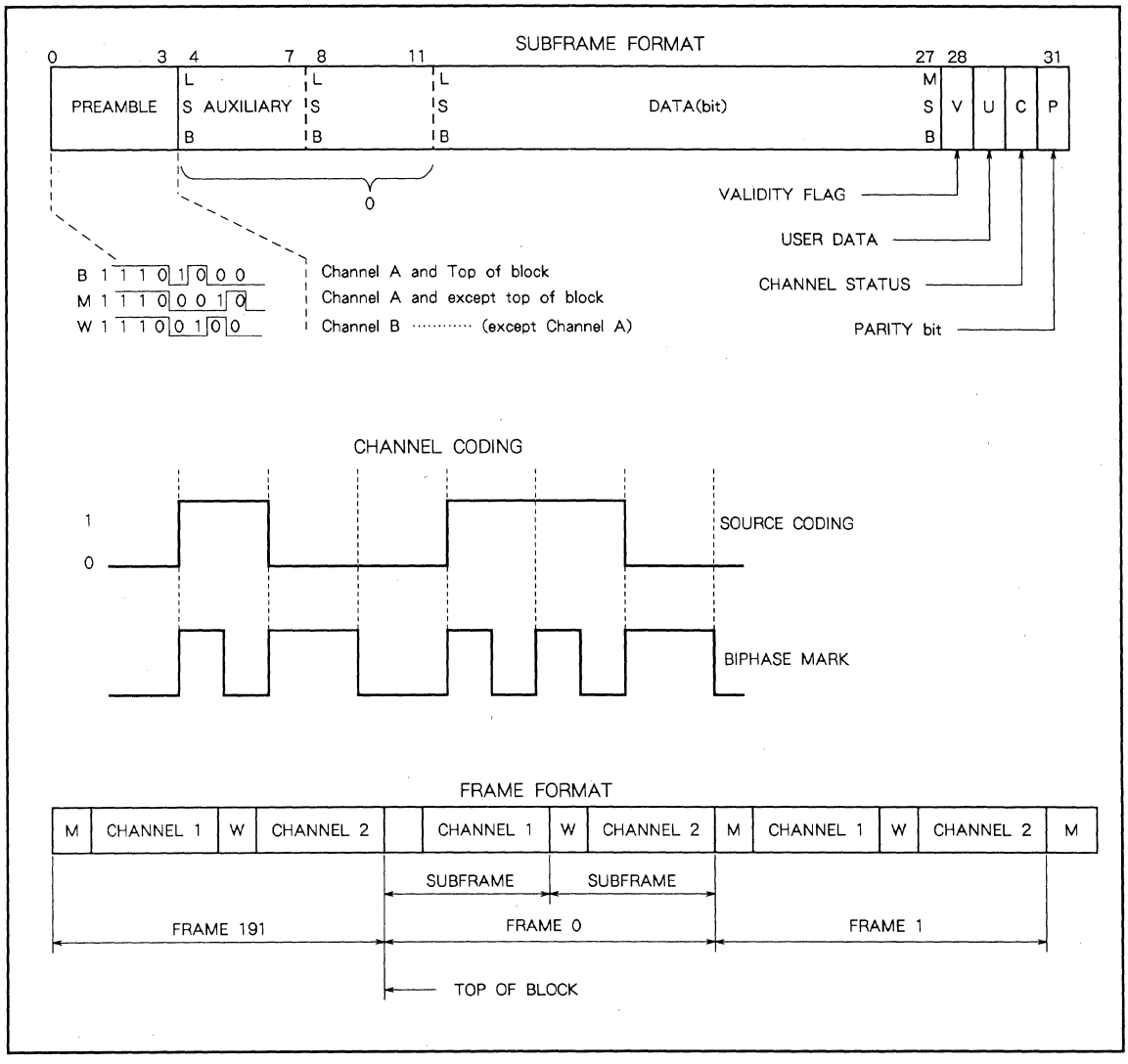


Fig. 6 Timing

7. CLV servo control circuit

CLV servo control circuit operates using two signals. The first is the frequency difference beween EFM-clock and X'tal -clock. The second is the phase difference beween write-frame address and read-frame address of the external 64K or 256K RAM. Motor control signals are output to PWM_1 (− signal) and PWM_2 (+ signal).

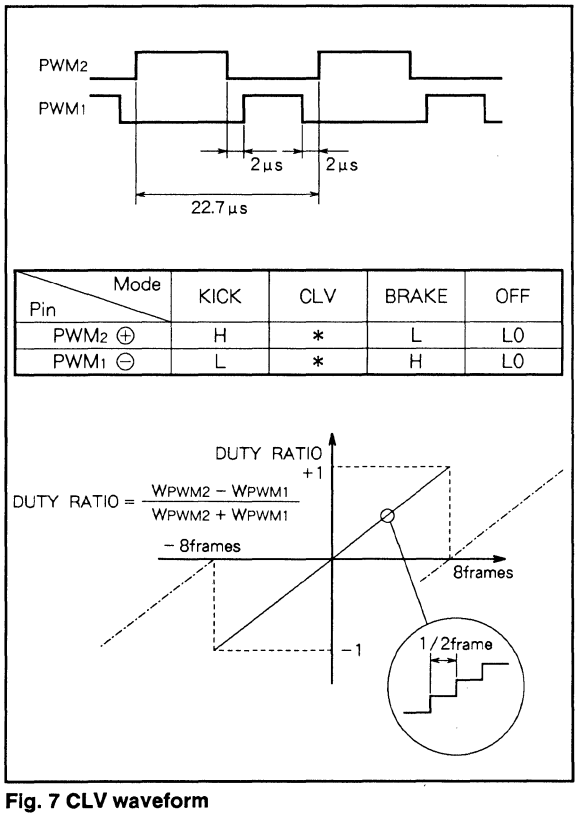
Because these singals are internally phase compensated, the CLV servo control circuit can be easily composed using current drivers on pins PWM_1 and PWM_2.

Fig. 7 shows the CLV wave form and its duty cycle when the CIRC decoding block addressing write-frame address and the read-frame address exceeds ± 8frames.

When this occurs the duty cycle of the CLV waveforms will be reset to 0.

The disc motor can be driven by PWM waveforms directly or it can be driven by an analog signal that can be generated by integrating the PWM waveforms.

By using an analog signal, it is possible to adjust the servo loop-gain by varying direct external component values. But in the case of PWM waveforms, the servo loop-gain is determined by motor torque, and the rotating moment of the disc, turntable, and disc clamper.



Pin \ Mode	KICK	CLV	BRAKE	OFF
PWM_2 ⊕	H	*	L	L0
PWM_1 ⊖	L	*	H	L0

Fig. 7 CLV waveform

M50427FP

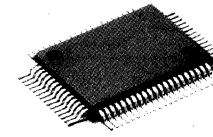
CD PLAYER DIGITAL SIGNAL PROCESSOR

DESCRIPTION

The M50427FP is a CMOS IC developed for compact disc (CD) sound reproducing applications. It has adjustment-free PLL, error correction circuitry, etc. and is used in a CD digital signal processing section. Applications include also CD-ROM and CD-G, as well as CD-DA.

FEATURES

- Adjustment free EFM-PLL circuit (built-in VCO)
- ± 8 frames jitter margin
- Easy-to-handle CLV servo commands
- Subcode parallel/serial interface
- 2 times over sampling
- Capable of double speed sound reproduction



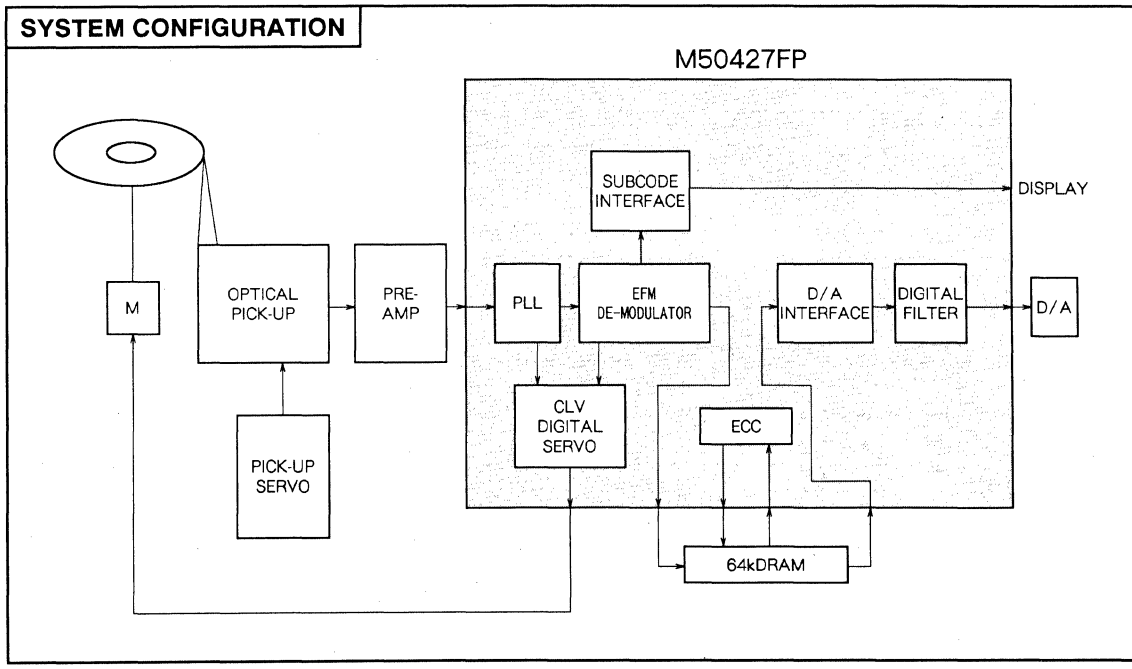
Outline 72P6-B

0.8mm pitch QFP
(18.0mm × 13.2mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

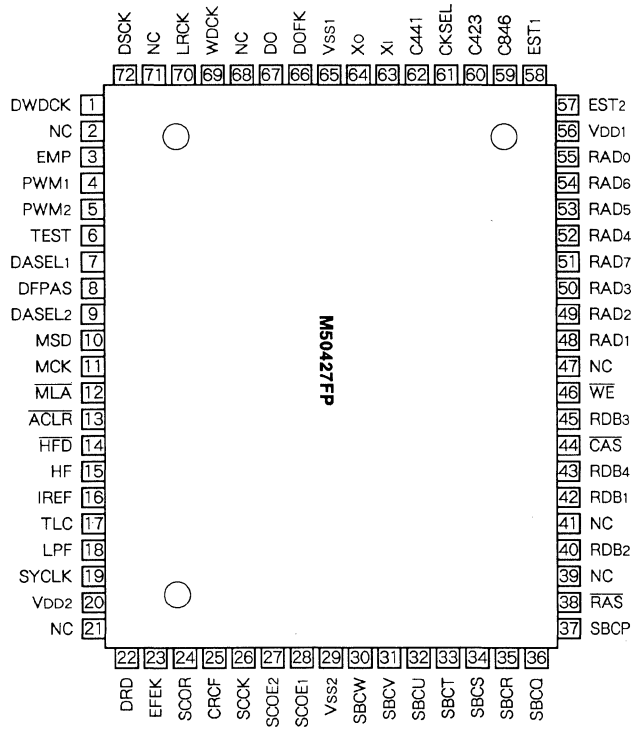
Supply voltage range ..... V_{DD} = 4.5~5.5V
Rated voltage range ..... V_{DD} = 5V
Rated power dissipation 90mW

SYSTEM CONFIGURATION



MITSUBISHI ELECTRIC

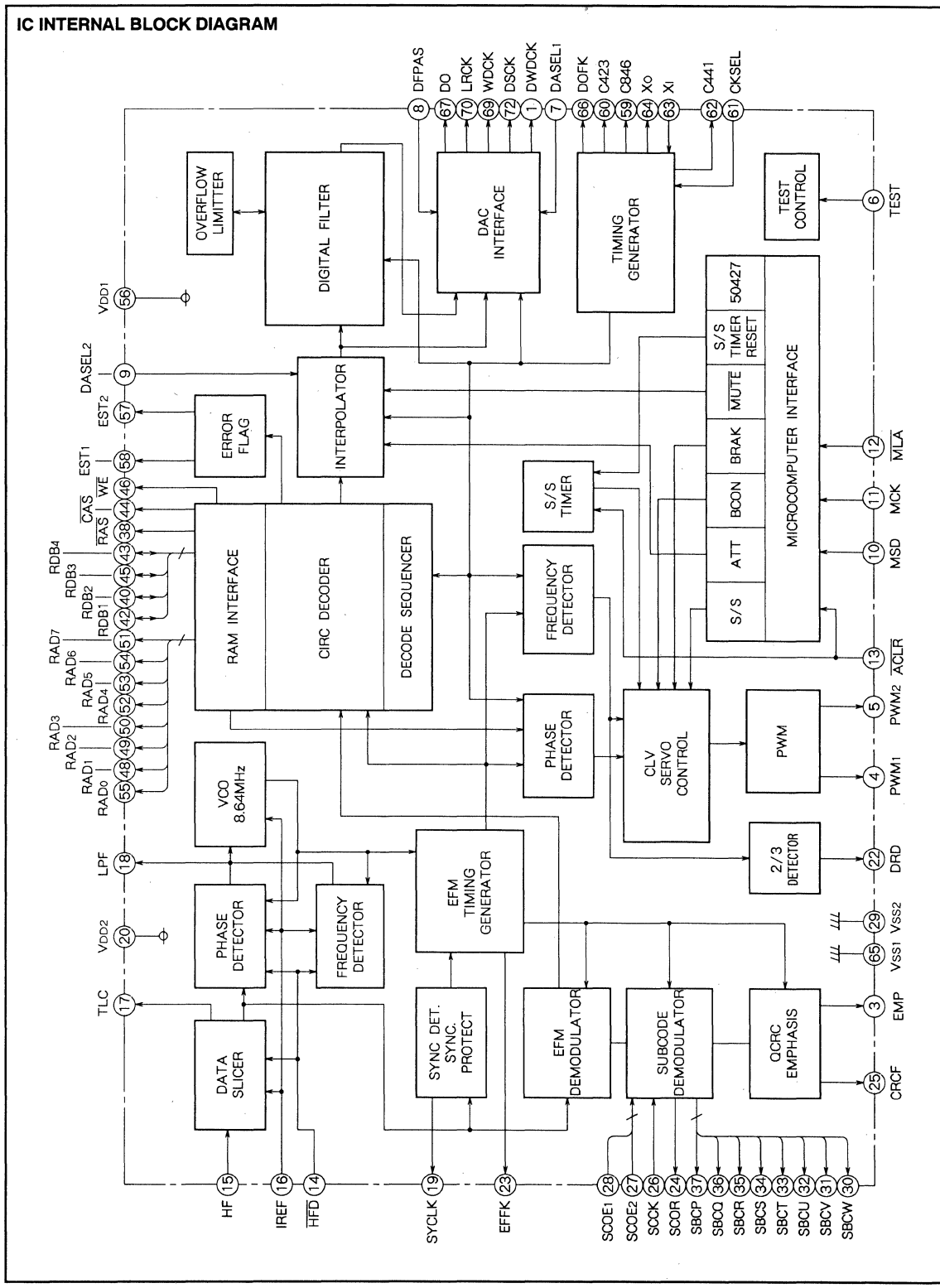
PIN CONFIGURATION



Outline 72P6-B

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Name	I/O	Function
DWDCK	O	Mode3 word clock to DAC
EMP	O	Emphasis flag output, Emphasis = 1
PWM_1	O	Disc motor driving PWM output 1, −
PWM_2	O	Disc motor driving PWM output 2, +
TEST	I	Test control input, Normal = 0
$DASEL_1$	I	DAC interface format select 1
DFPAS	I	Digital filter pass select, Bypass = 1
$DASEL_2$	I	DAC interface format select 2
MSD	I	Microcomputer interface serial data input
MCK	I	Microcomputer interface shift clock input
$\overline{MLA}$	I	Microcomputer interface data latch clock input
$\overline{ACLR}$	I	Microcomputer interface register clear input, All clear = 0 SS timer reset = 1 MUTE, S/S, BCON = 0 become
$\overline{HFD}$	I	High frequency detect
HF	I	High frequency input
IREF	I	Current referance
TLC	O	Output from slice level control
LPF	I/O	PLL loop filter
SYCLK	O	Frame lock status output, Lock = 1
V_{DD2}	I	V_{DD} for data slicer and VCO
DRD	O	Low disc rotation status
EFFK	O	EFM frame clock duty = 50 %
SCOR	O	Subcode sync output $S_0 + S_1$
CRCF	O	Subcode Q, CRC check flag output CROCK = 1
SCCK	I	Shift clock input for serial subcode data output
$SCOE_2$	I	Enable input of subcode T∼Wch output 0 : High Z
$SCOE_1$	I	Enable input of subcode P∼Sch output 0 : High Z
V_{SS2}	I	Ground
SBCW	O	Subcode Wch output
SBCV	O	Subcode Vch output
SBCU	O	Subcode Uch output
SBCT	O	Subcode Tch output
SBCS	O	Subcode Sch output
SBCR	O	Subcode Rch output

Name	I/O	Function
SBCQ	O	Subcode Qch output
SBCP	O	Subcode Pch output Pch∼Wch serial data output
$\overline{RAS}$	O	Row address strobe output to RAM
RDB_2	I/O	Data input/output 2 to RAM
RDB_1	I/O	Data input/output 1 to RAM
RDB_4	I/O	Data input/output 4 to RAM
$\overline{CAS}$	O	Column address strobe output to RAM
RDB_3	I/O	Data input/output 3 to RAM
$\overline{WE}$	O	Write enable output to RAM
RAD_1	O	Address output 1 to RAM
RAD_2	O	Address output 2 to RAM
RAD_3	O	Address output 3 to RAM
RAD_7	O	Address output 7 to RAM
RAD_4	O	Address output 4 to RAM
RAD_5	O	Address output 5 to RAM
RAD_6	O	Address output 6 to RAM
RAD_0	O	Address output 0 to RAM
V_{DD1}	I	Power supply 5V
EST_2	O	Error status 2, Error to be interpolated detected at C2 decoder = 1
EST_1	O	Error status 2, Error detected at C1 decoder = 1
C846	O	Clock output 8.4672MHz
C423	O	Clock output 4.2336MHz, duty = 50 %
CKSEL	I	Crystal selector input L = 8.4672MHz H = 16.9344MHz
C441	O	Clock output 44.1kHz (crystal = 16.9344MHz)
X_I	I	Crystal oscillator input with internal feedback resister
X_O	O	Crystal oscillator output
V_{SS1}	I	Ground
DOFK	O	OSC frame clock output 7.35kHz, duty = 50 %
DO	O	Serial data output to DAC
WDCK	O	Word clock to DAC or APTL clock
LRCK	O	Lch/Rch clock to DAC or APTR clock
DSCK	O	Data shift clock to DAC

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}-V_{SS}	Supply voltage		− 0.3～+ 7.0	V
V_I	Input voltage	(R_P = 0 Ω)	V_{SS}-0.3≦ V_I ≦ V_{DD}+0.3	V
V_O	Output voltage	(R_P = 0 Ω)	V_{SS}-0.3 ≦ V_O ≦ V_{DD}	V
V_P	Pull up voltage		V_P ≦ V_{DD} + 2mA * R_P	V
T_{opr}	Operating temperature		−10～+70	℃
T_{stg}	Storage temperature		−40～+125	℃
P_d	Power dissipation		350	mW

R_P : Pulling up resistor

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Applied pin	Limits			Unit
				Min	Typ	Max	
V_{DD}	Supply voltage			3.5	5.0	5.5	V
V_{IH1}	High-level input voltage 1		2)	V_{DD} *0.5	−	V_{DD}	V
V_{IH2}	High-level input voltage 2		1)	V_{DD} *0.7	−	V_{DD}	V
V_{IL1}	Low-level input voltage 1		2)	V_{SS}	−	V_{DD} *0.08	V
V_{IL2}	Low-level input voltage 2		1)	V_{SS}	−	V_{DD} *0.3	V
f_{OSC}	Oscillation frequency (X'tal)			−	8.46	−	MHz
f_{VCO}	Oscillation frequency (VCO)			−	8.64	−	MHz

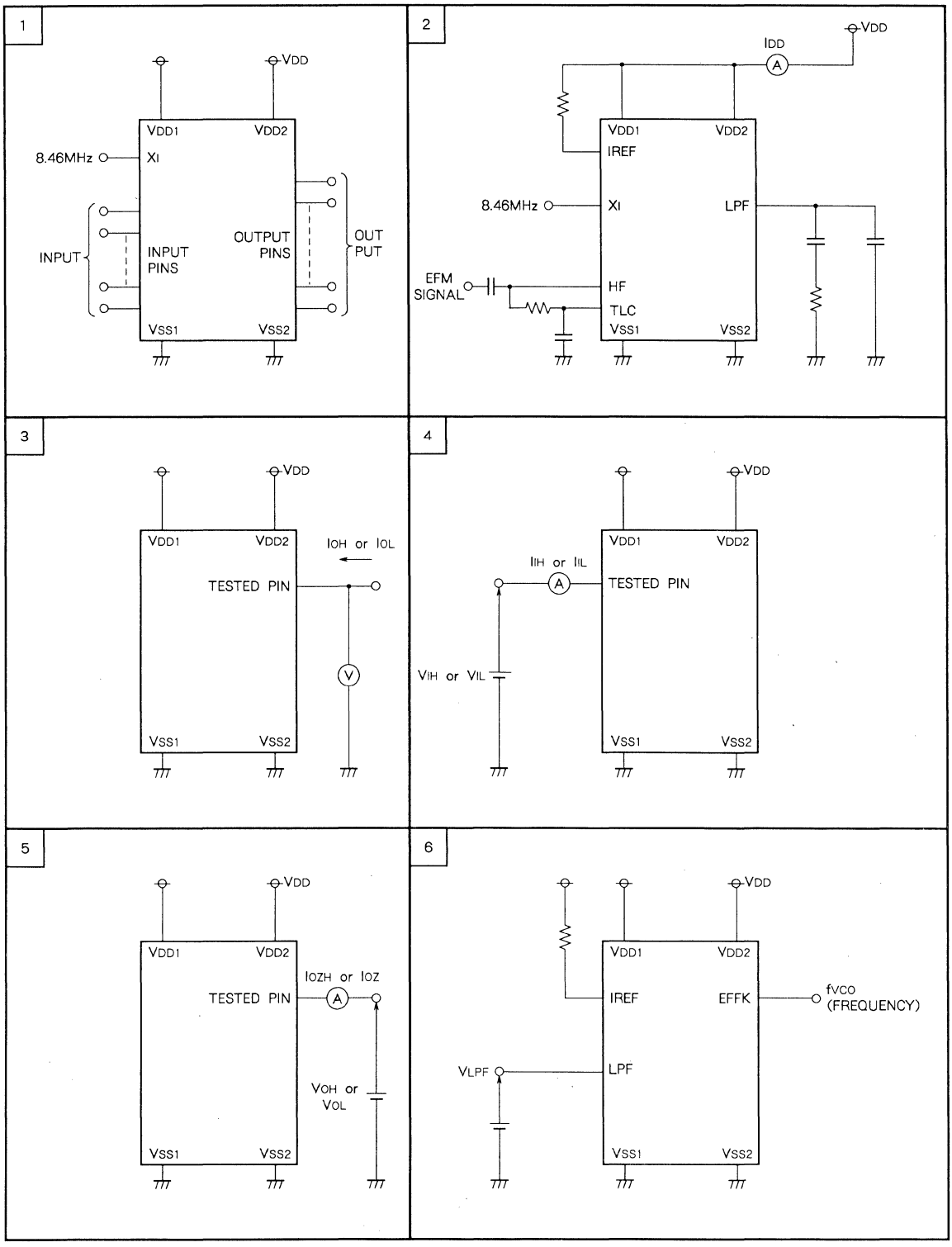
Note 1. Applied pin
1) DASEL1, DFPAS, DASEL2, CKSEL, TEST
2) HFD, SCOE1, SCOE2, SCCK, MSD, MCK, MLA, ACLR, RDB1～RDB4

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{DD} = 5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Applied pin	Test circuit	Limits			Unit
					Min	Typ	Max	
V_{DD}	Supply voltage	T_a = − 10～+ 70℃		1	3.5	5.0	5.5	V
I_{DD}	Circuit current	f_{OSC} = 8.4672MHz f_{VCO} = 8.6436MHz		2	−	15	30	mA
V_{OH}	High-level output voltage	V_{DD}=4.5V, I_{OH}= −0.8mA	3)	3	3.5	−	−	V
V_{OL}	Low-level output voltage	V_{DD}=4.5V, I_{OL}=0.8mA	3)	3	−	−	0.4	V
I_{IH}	High-level input current	V_{IH}=4.5V	4)	4	−	−	2	μA
I_{IL}	Low-level input current	V_{IL}=0.5V	4)	4	−	−	− 2	μA
I_{OZH}	Off state high-level output current	V_{OH}=4.5V	5)	5	−	−	2	μA
I_{OZL}	Off state low-level output current	V_{OL}=0.5V	5)	5	−	−	− 2	μA
f_{VCO1}	VCO (EFFK) Free running frequency	V_{LPF}= 1.0V		6	−	−	3.0	kHz
f_{VCO2}		V_{LPF}= 2.5V		6	8.0	10.0	−	kHz
f_{VCO3}		V_{LPF}= 4.0V		6	11.0	−	−	kHz

Note 2. Applied pin
3) Output and input/output pin except XO, TLC, LPF
4) Input pin except XI, IREF
5) RDB1～RDB4, SBCP～SBCW

TEST CIRCUIT



FUNCTIONAL DESCRIPTION

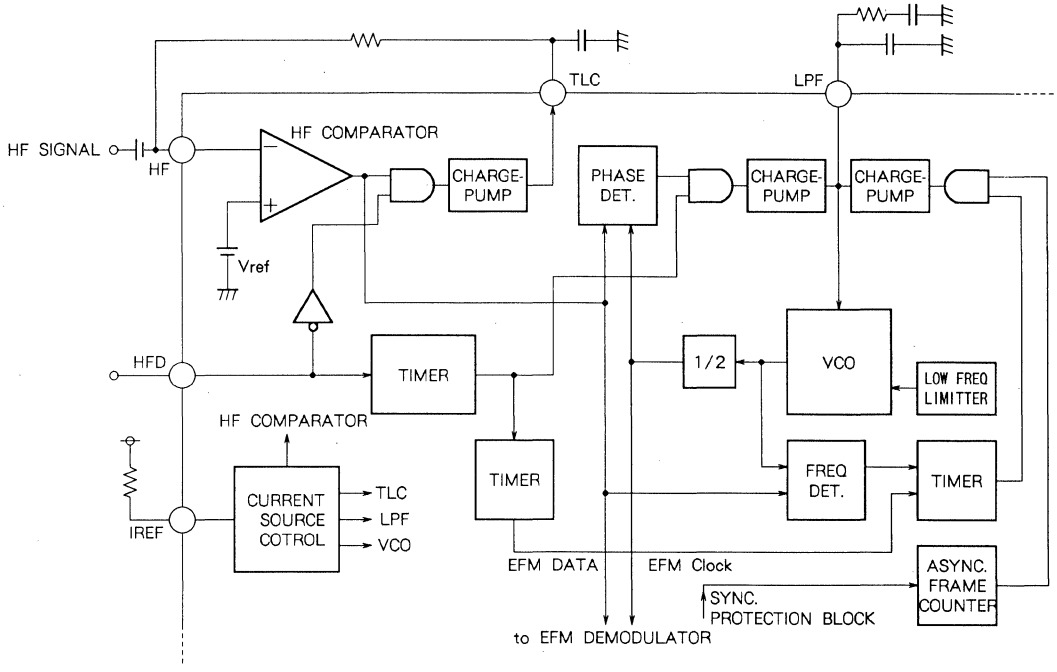
1. Data slicing/PLL

The M50427FP has an analog front-end for incoming EFM (HF) signal. Using CMOS-Analog technology, the front-end comprises an automatic slice level control circuit and EFM-PLL circuit with internal adjust-free VCO. The HF signal is sliced by the HF comparator and a DC level is feed back from TLC to HF through the external CR. If HFD goes High because of a defect an disc, then TLC froms off and holds the DC level. The block-diagram shows the analog front-end.

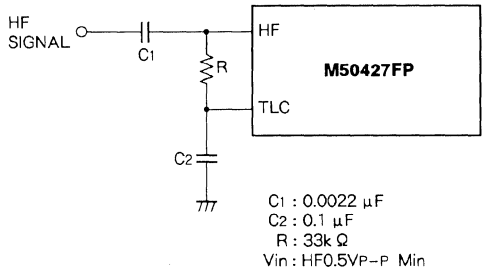
EFM-PLL extracts the EFM clock signal from the HF signal. The PLL circuit has a phase/frequency comparator providing the M50427FP with a wide capture/lock range. There is no need to adjust the VCO. LPF is the charge-pump output and same-time control voltage input to the VCO. LPF froms off state if HFD goes high.

IREF is the reference current input used to determine the current of charge pumps of TLC and LPF, operating point of HF comparator and VCO free running frequency. If IREF is connected to a noisy power supply through a resistor, VCO is modulated and the error-rate increases. Therefore, power supply noise at IREF must be held to a minimum.

BLOCK DIAGRAM (Data slicing/PLL)

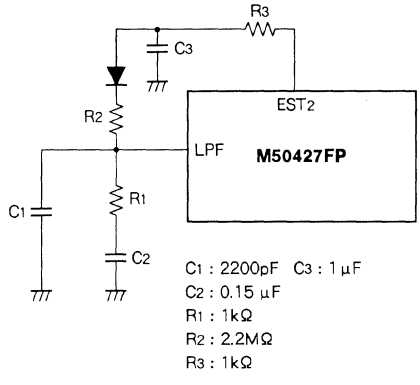


(1) Automatic slice level control



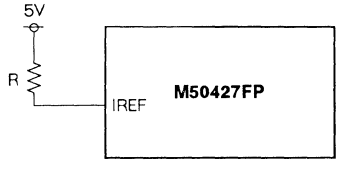
The slice level control circuit is formed by connecting a resistor and capacitors to the HF (High-Frequency signal input) pin and TLC (slice level control output) pin.

(2) PLL



Since the adjustment-free VCO is built in, the adjustment-free PLL circuit can be formed by connecting a resistor and capacitors to the LPG (low-pass filter) pin.

(3) Reference current

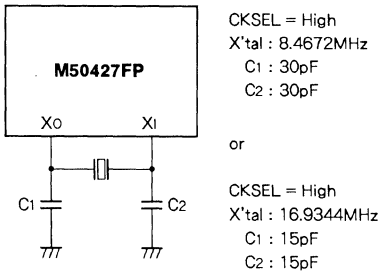


R : 51k Ω

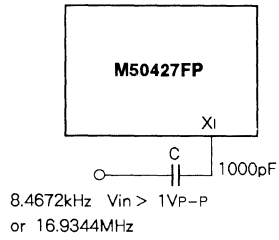
Connect the resistor between the IREF pin and V_{DD} to set the reference current that determines the current values of the TLC pin and LPG pin, the comparator operating current of the slice level control circuit and the VOC free-run frequency.

2. Demodulation/Decoding

(1) Clock generator



(a) The oscillation circuit can be formed by connecting the X'tal osillator (8.4672MHz or 16.9344MHz) and load capacitors to pins X_I and X_O.



b) When the system contains a clock (8.4672MHz or 16.9344MHz), the clock can be input to pin X_I via a capacitor without using the X'tal oscillator.

If the input signal is the logical level, the capacitor is not necessary.

(2) Frame Synchronization

The EFM signal is demodulated by synchronizing the demodulation circuit at frame level. The block diagram shows this frame synchronization control part.

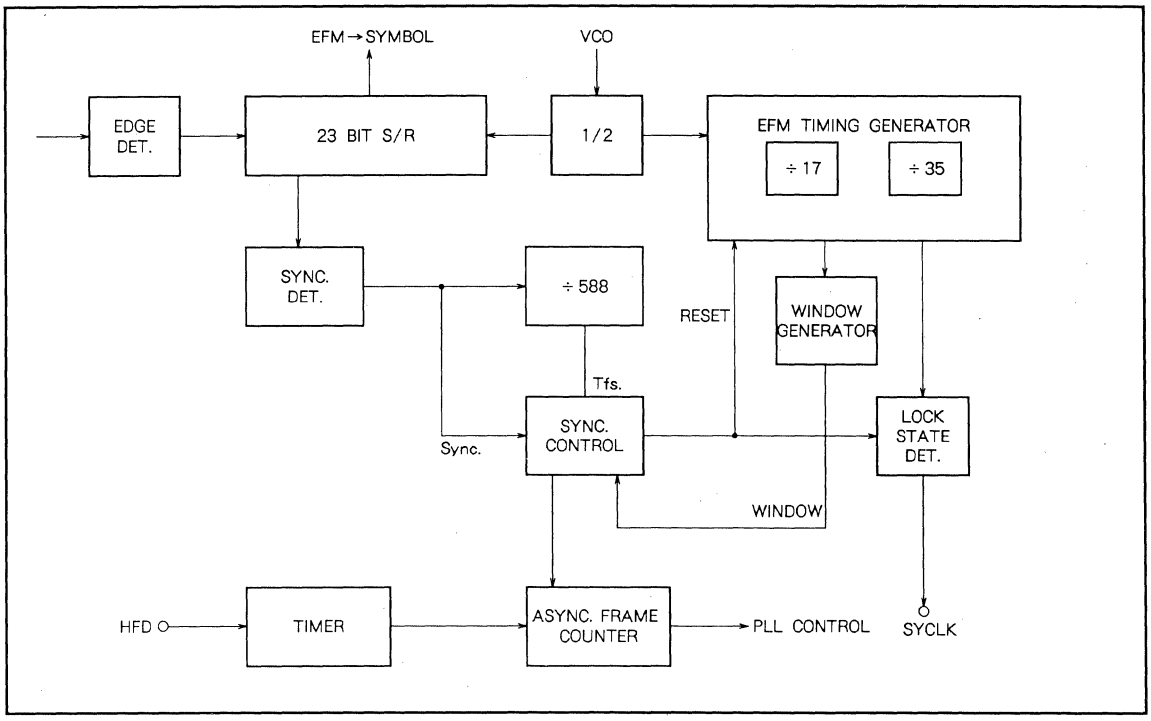


Fig. 1 Frame synchronization block diagram

The generating condition of the counter reset signal (Reset) in the EFM timing generator part is indicated as follows :

Reset = Sync * Tfs + Sync * Window

* : Logical product

\+ : Logical sum

Sync. : Synchronizing signal

Tfs : Detection signal of synchronizing signal space = 588

Window : Window signal ± 7ck

In the synchronous state, Sync and Tfs generate simultaneously and Sync comes to the center of the window. At this time, 1 is output to the SYCLK pin.

(3) Subcode demodulation

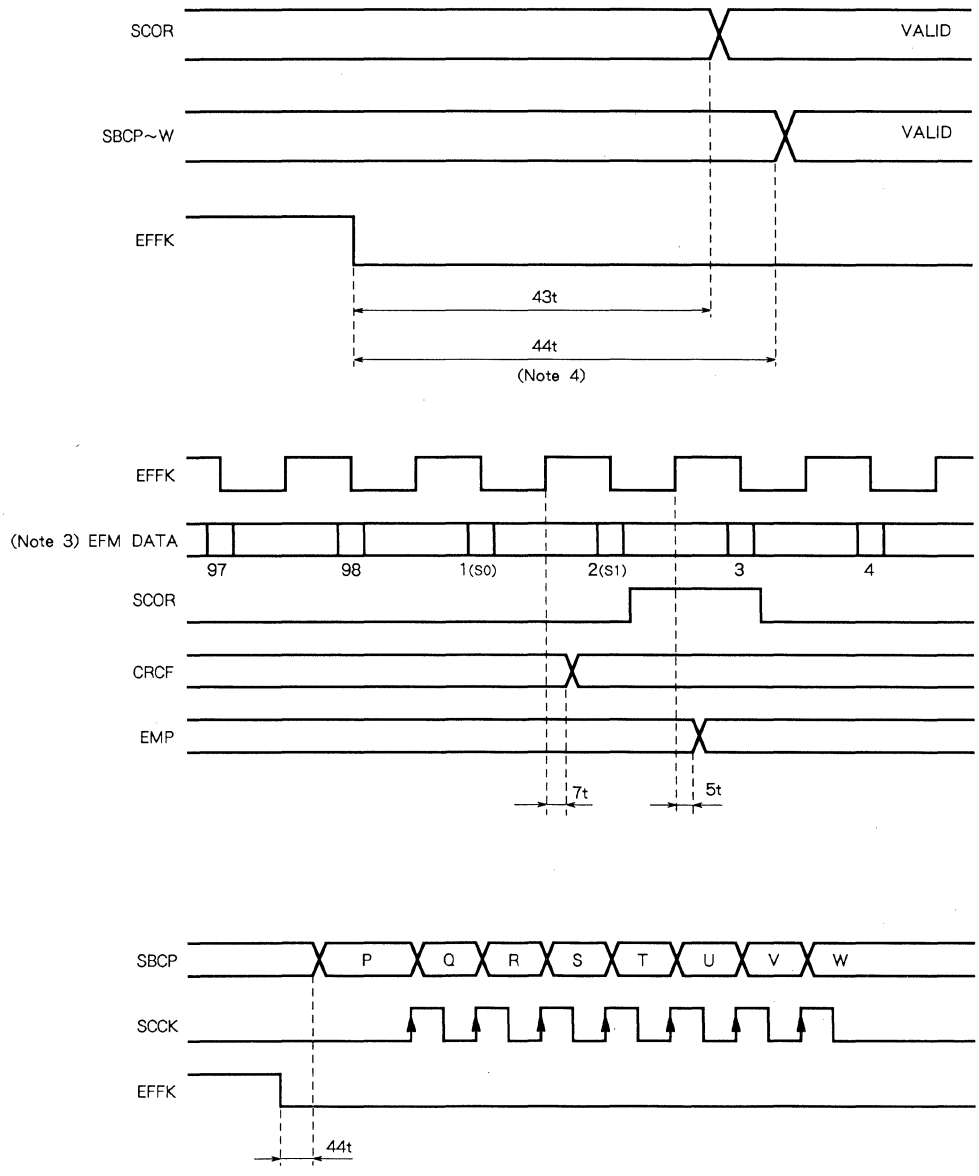
Among data converted from 14-bit EFM signals to 8-bit symbols, subcode P, Q, R, S, T, U, V and W are output to pins SBCP - SPCW respectively. When the subcode synchronizing patterns S0 or S1 are detected as the synchronizing signals of the subcode data, the synchronizing signal are output to the SCOR pin. The pins SBCP-SBCW are a Three-State output system and control the output by 4-bit through two external pins $SCOE_1$ and $SCOE_2$.

SUBCODE DEMODULATION

$SCOE_1$	$SCOE_2$	SBCP	SBCQ	SBCR	SBCS	SBCT	SBCU	SBCV	SBCW
0	0	High-impedance				High-impedance			
1	0	P	Q	R	S	High-impedance			
0	1	High-impedance				T	U	V	W
1	1	P	Q	R	S	T	U	V	W

A CRC check is made for the Q channel data and if the data is correct, 1 is output to the CRCF pin. Whether or not there is emphasis is output to the EMP pin. The subcode data is not only output in parallel but also can be obtained serialy via pin SBCP by inputting a clock to pin SCCK.

Fig. 2 shows the timing of each signal.



Notes 3. Subcode block No. in the EFM data

4. t : Oscillating frequency (VCO)
(Average : 1/8.6436MHz = 115.7ns.)

5. When input to SCCK is more than 8ck, SBCP becomes 0.

Fig. 2 Subcode output timing

(4) RAM interface/CIRC decoding

A 64K/256K dynamic RAM is used as the external memory for temporary storage process CIRC decoding (C1 decoding, C2 decoding, unscramble and de-interleave) and output interpotion.

By using a 64K/256K RAM, jitter is absorbed up to ±8 frames (max.).

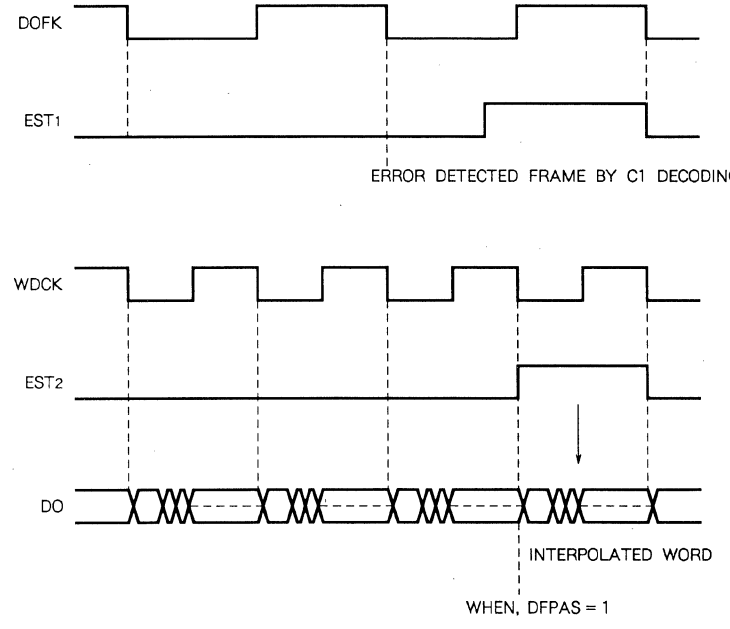
Fig. 3 shows the timing for reading from and writing to the RAM.

In CIRC decoding, double error correction is done for both C1 and C2 decoding. When correction is not possible, average interpolation or pre-hold interpolation is performed. Error states which are detected during, decoding are output to pins EST_1 and EST_2.

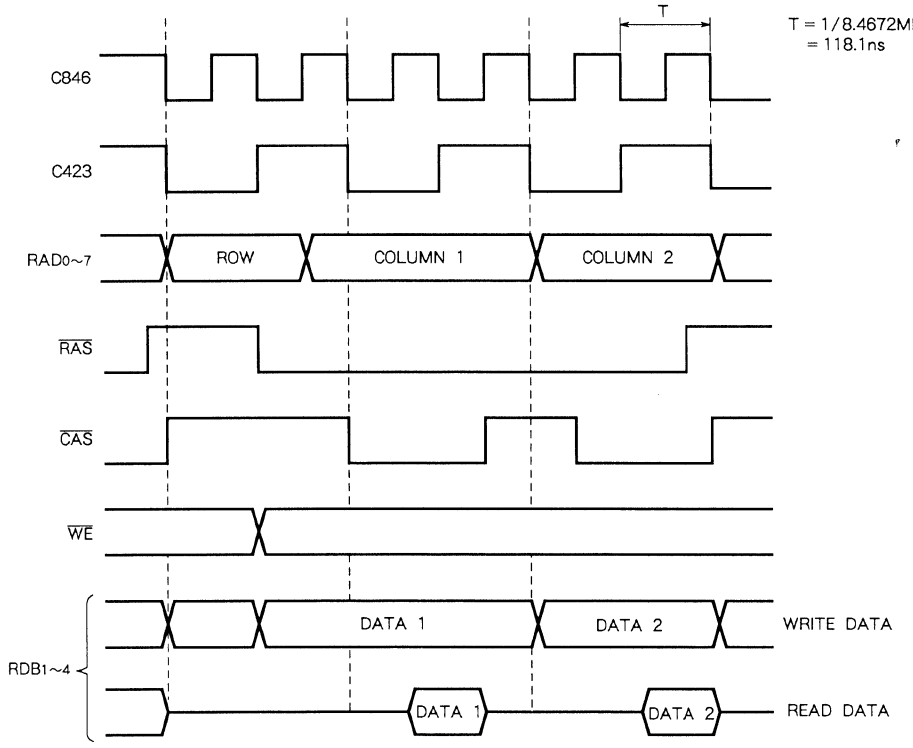
When an error is detected by C1 decoding, 1 is output to pin EST_1. When an error word is judged un-correctable by C2 decoding, 1 is output to pins EST_2.

The output timings for pins EST_1 and EST_2 are as follows:

Timing chart



(a) Symbol data/flag, read/write timing



(b) C1/C2 flag, read/write timing

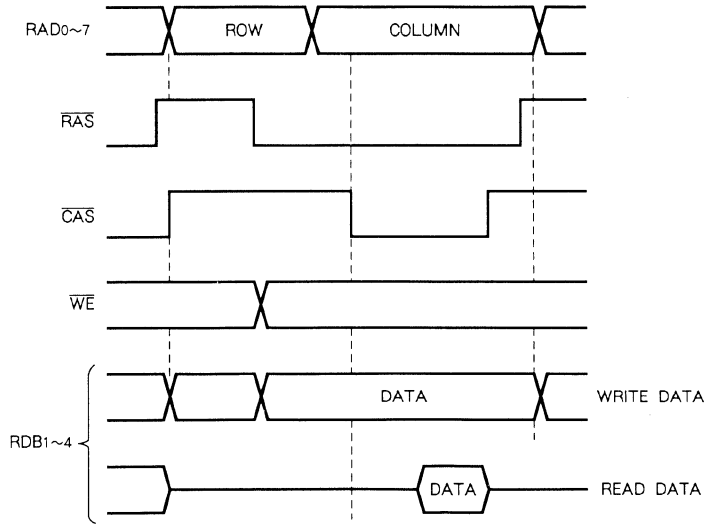
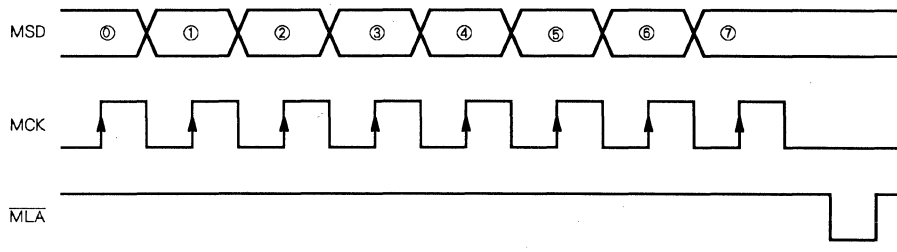


Fig. 3 RAM interface timing

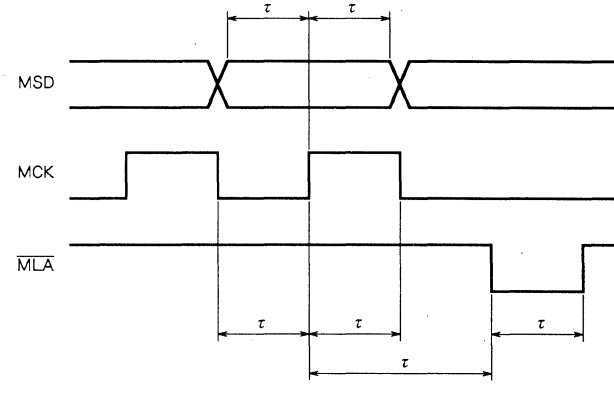
3. Microcomputer interface

CLV servo, MUTE and ATT system control is done by serial command from the microcomputer. The timing, and names and functions of each control register are as follows :

Timing chart



⓪ DUMMY (Don't care)	X
① S/S(START/STOP) register.	start = 1
② BCON(BRAKECONTROL) register.	enable = 1
③ BRAK(BRAKE) register.	brake = 1
④ ATT(ATTENUATE) register.	−12dB = 1
⑤ $\overline{\text{MUTE}}$ register.	mute = 0
⑥ S/S timer reset register.	reset = 1
⑦ IC code.	M50427FP = 1



τ min ∗ 500ns

Function of Interface resisters

Register No.	Register name	Function	Operation		Note
			0	1	
⓪	DUMMY	Don't care	–	–	
①	S/S (START/STOP)	Controls START/STOP of the disk motor	DISC MOTOR STOP (OFF)	DISC MOTOR START (ON)	0 by $\overline{ACLR}$
②	BCON (BRAKECONTROL)	Determines if BRAKE control is necessary	BRAKE 0.3sec.	BRAKE is controlled by BRAK register	0 by $\overline{ACLR}$
③	BRAK (BRAKE)	Controls BRAKE	BRAKE OFF (MOTOR OFF)	BRAKE ON	When BCON = 1
④	ATT (ATTENUATE)	Sets attenuation (−12dB)	0dB	− 12dB	When MUTE = 1
⑤	MUTE	Sets the muting	$-\infty$ dB	0dB	0 by $\overline{ACLR}$
⑥	S/S timer reset	Resets the S/S timer which sets the time of KICK and BRAKE to 0.3sec	S/S timer enable	S/S timer disable	1 by $\overline{ACLR}$
⑦	IC code	Distinguishes the command to the M50427FP	–	Executing command	0 is code for servo IC

Examples of system control are as follows :

Operation \ Register name	⓪ DUMMY	① S/S	② BCON	③ BRAK	④ ATT	⑤ $\overline{MUTE}$	⑥ S/S timer reset	⑦ IC code
								0
MUTE						0		1
ATT					1	1		1
0.3sec.KICK→CLV		1					0	1
0.3sec.BRAKE→MOTOR OFF		0	0				0	1
BRAKE		0	1	1			0	1
MOTOR OFF		0	1	0			0	1
0.3sec. timer disable							1	1
MOTOR off(without 0.3sec. BRAKE)		0	0				1	1
CLV (without 0.3sec. KICK)		1	0				1	1
The following is example of the most simplified system control sequence.								
STOP		0	0	0	0	0	1	1
0.3sec. KICK→CLV		1	0	0	0	0	0	1
PLAY		1	0	0	0	1	0	1
FF/FR		1	0	0	1	1	0	1
PLAY		1	0	0	0	1	0	1
0.3sec. BRAKE→STOP		0	0	0	0	0	0	1

* The blanks mean "Don't care" or that other commands can be used simultaneously.

When the M50427FP detects whether the number of rotations is 2/3 that of the normal play state and outputs the disk rotation deterioration signal to the DRD pin.

The rotation of the disk can be correctly stopped by means of the following stop sequence.

Operation or μ-COM Operation \ Register name	⓪ DUMMY	① S/S	② BCON	③ BRAK	④ ATT	⑤ $\overline{MUTE}$	⑥ S/S timer reset	⑦ IC code
PLAY		1	0	0	0	1	0	1
BRAKE		0	1	1	0	0	0	1
($\overline{HFD}$: H checking by microcomputer)								
(Measuring t_{DRD} (DRD : 0→1) after BRAKE start								
(Stop $\overline{HFD}$ checking and) additional BRAKE time 2 × t_{DRD}								
MOTOR OFF		0	1	0	0	0	0	1

To re-initiative the microcomputer interface register, after power supply on, execute $\overline{ACLR}$ (M50427FP clear).

4. Digital filter

The sampling frequency of the data is coverted from 44.1 kHz to 88.2kHz by the digital filter.

The filter is a 27-tap FIR phase linear filter and includes an overflow limitter.

The digital filter can be by-passed by means of the DFPAS pin. At this time, all the D-A interface timing signals are changed according to the sampling frequency (44.1kHz).

Fig. 4 shows the characteristics of the digital filter.

5. Interface to the D-A converter

The interface to the D-A converter is via the MSB first or LSB first serial data and timing signals. Interface mode selection is done by the $DASEL_1$ and $DASEL_2$. The data and the timing signals are as follows :

MODE	DASEL 2	DASEL 1	DO	DSCK	WDCK	LRCK	DWDCK
0	0	0	MSB 1st	DATA SHIFT CLOCK	Word clock	L/R clock	–
1	0	1	LSB 1st	DATA SHIFT CLOCK	Lch sampling clock	Rch sampling clock	–
2	1	0	MSB1st Without interpolation	DATA SHIFT CLOCK	Word clock	L/R clock	–
3	1	1	MSB 1st	DATA SHIFT CLOCK	Lch sampling clock	Rch sampling clock	Word clock

Fig. 5 (a) shows the timing diagram of mode0 and mode2 (without interpolation).

Fig. 5 (b) shows the timing diagram of mode1.

Fig. 5 (c) shows the timing diagram of mode2.

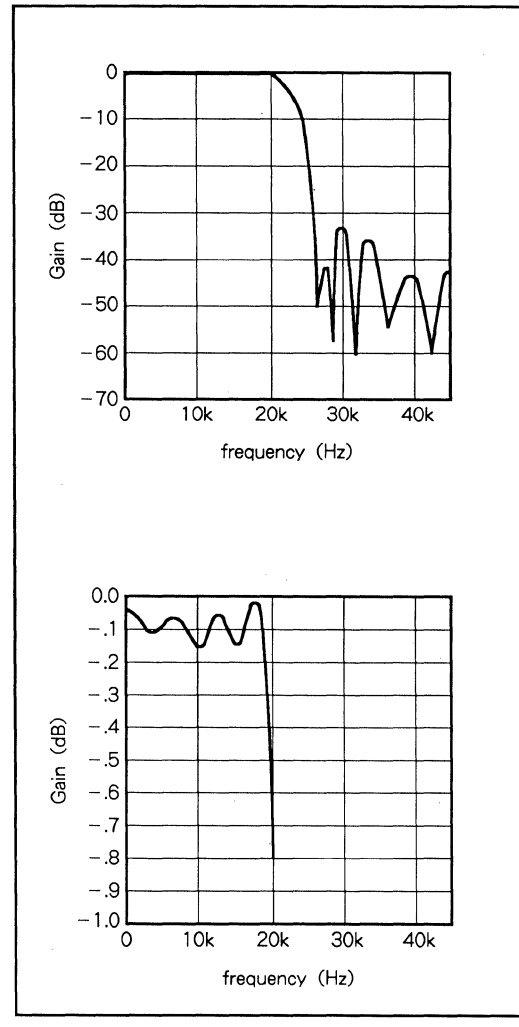
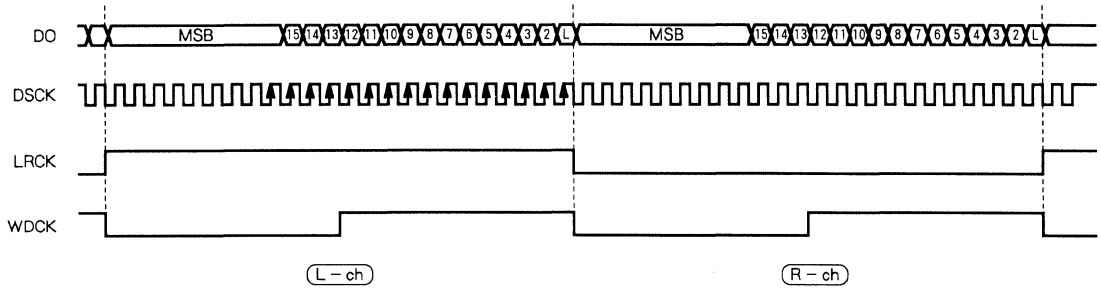


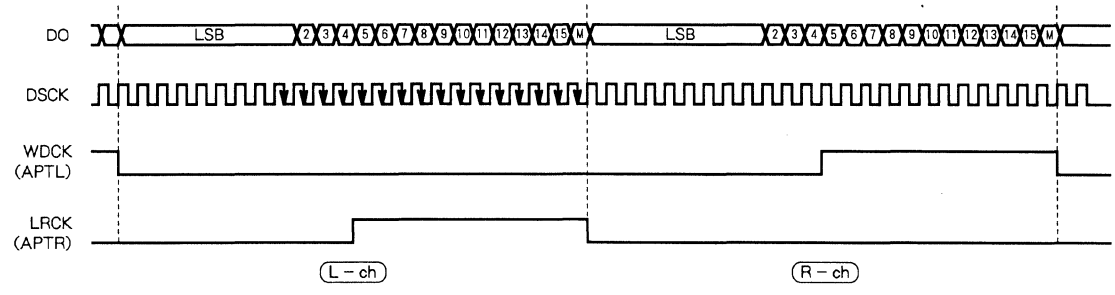
Fig. 4 Frequency characteristics of the digital filter

(a) Mode 0/2



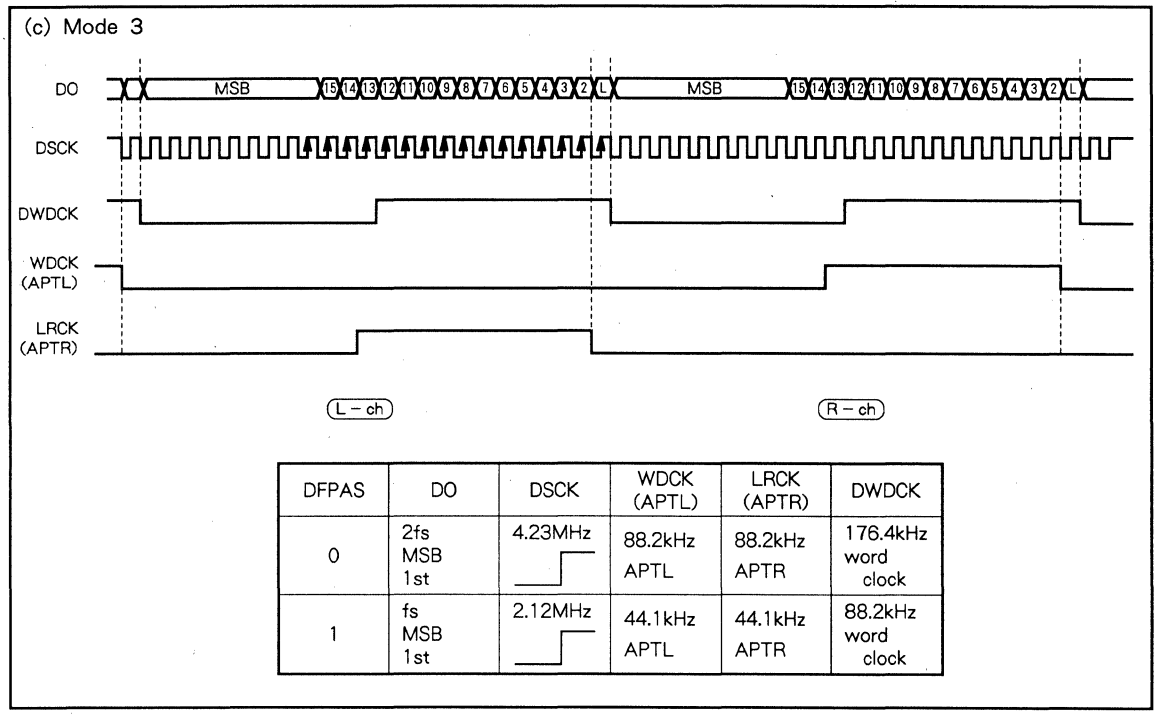
DFPAS	DO	DSCK	WDCK	LRCK
0	2fs MSB 1st	4.23MHz	176.4kHz word clock	88.2kHz L/R clock
1	fs MSB 1st	2.12MHz	88.2kHz word clock	44.1kHz L/R clock

(b) Mode 1



DFPAS	DO	DSCK	WDCK (APTL)	LRCK (APTR)
0	2fs LSB 1st	4.23MHz	88.2kHz APTL	88.2kHz APTR
1	fs LSB 1st	2.12MHz	44.1kHz APTL	44.1kHz APTR

Fig. 5 DAC interface timing

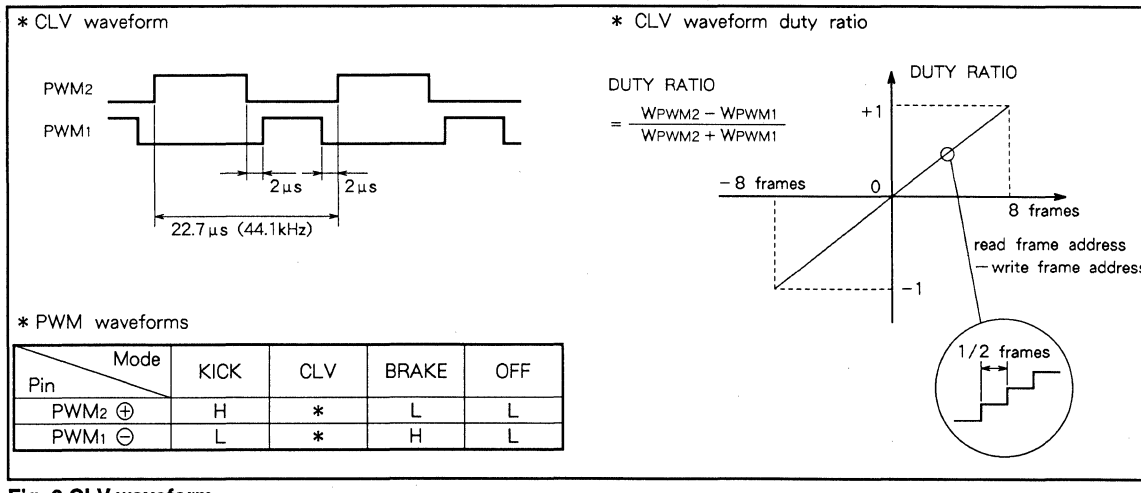


DFPAS	DO	DSCK	WDCK (APTL)	LRCK (APTR)	DWDCK
0	2fs MSB 1st	4.23MHz	88.2kHz APTL	88.2kHz APTR	176.4kHz word clock
1	fs MSB 1st	2.12MHz	44.1kHz APTL	44.1kHz APTR	88.2kHz word clock

Fig. 5 DAC interface timing

6. CLV servo control

CLV servo control circuit operates using two signals. The first is the frequency difference of EFM clock and X'tal clock. The second is the phase difference of write frame address and read frame address of external, 64K/256K RAM. The M50427FP has CLV servo control circuit internal phase compensated.



Pin \ Mode	KICK	CLV	BRAKE	OFF
PWM2 ⊕	H	*	L	L
PWM1 ⊖	L	*	H	L

Fig. 6 CLV waveform

MITSUBISHI ELECTRIC

M65820FP

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN MEMORY

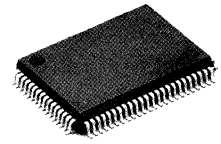
DESCRIPTION

The M65820FP is a CMOS IC developed for compact disc (CD) sound reproducing applications. It has memory, adjustment-free PLL, error correction circuitry, etc. and is used in a CD digital signal processing section.

Applications include also CD-ROM and CD-G, as well as CD-DA.

FEATURES

- Adjustment free EFM-PLL circuit (built-in VCO)
- ± 8 frames jitter margin
- Easy-to-handle CLV servo commands
- Built-in memory for interleaving
- Subcode parallel/serial interface
- Selection available from 2 times and 4 times over sampling
- 18-bit output available (with 4 times oversampling)
- Dual DAC output available (with 4 times oversampling)



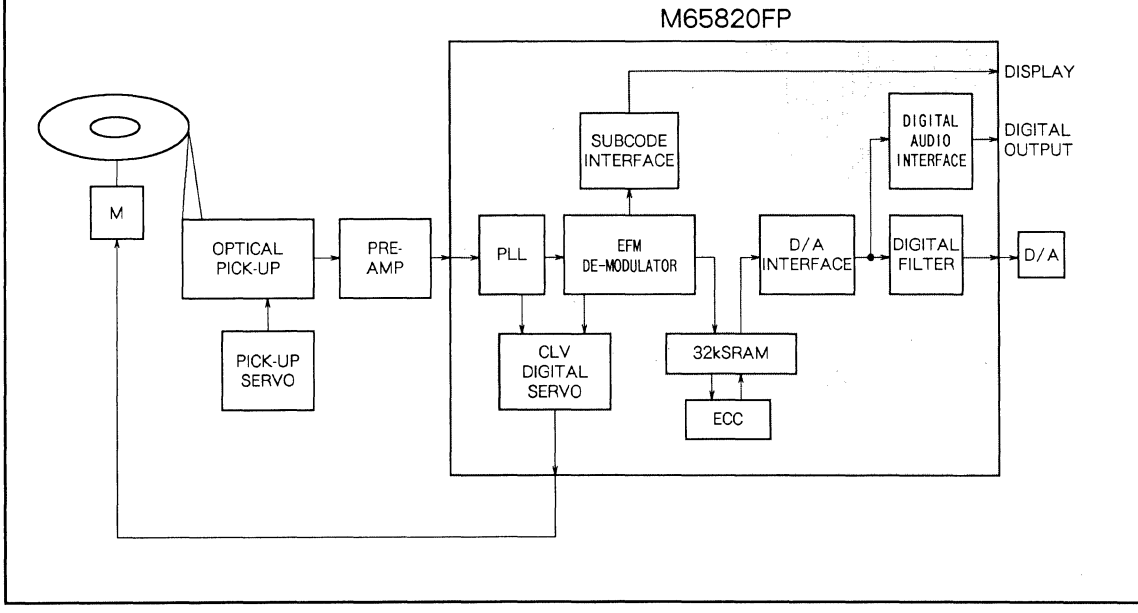
Outline 80P6N-A

0.8mm pitch QFP
(20.0mm × 14.0mm × 2.8mm)

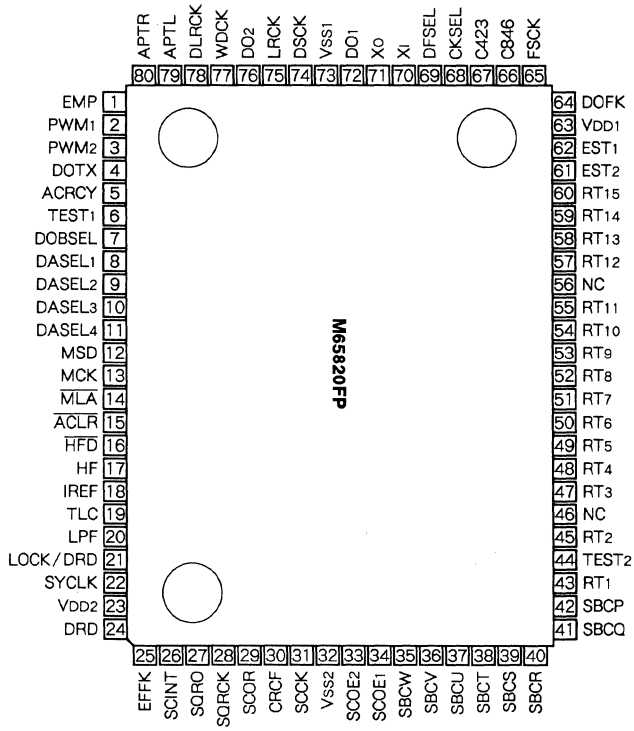
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{DD} = 4.5~5.5V
Rated supply voltage ..... V_{DD} = 5V
Rated power dissipation 100mW

SYSTEM CONFIGURATION



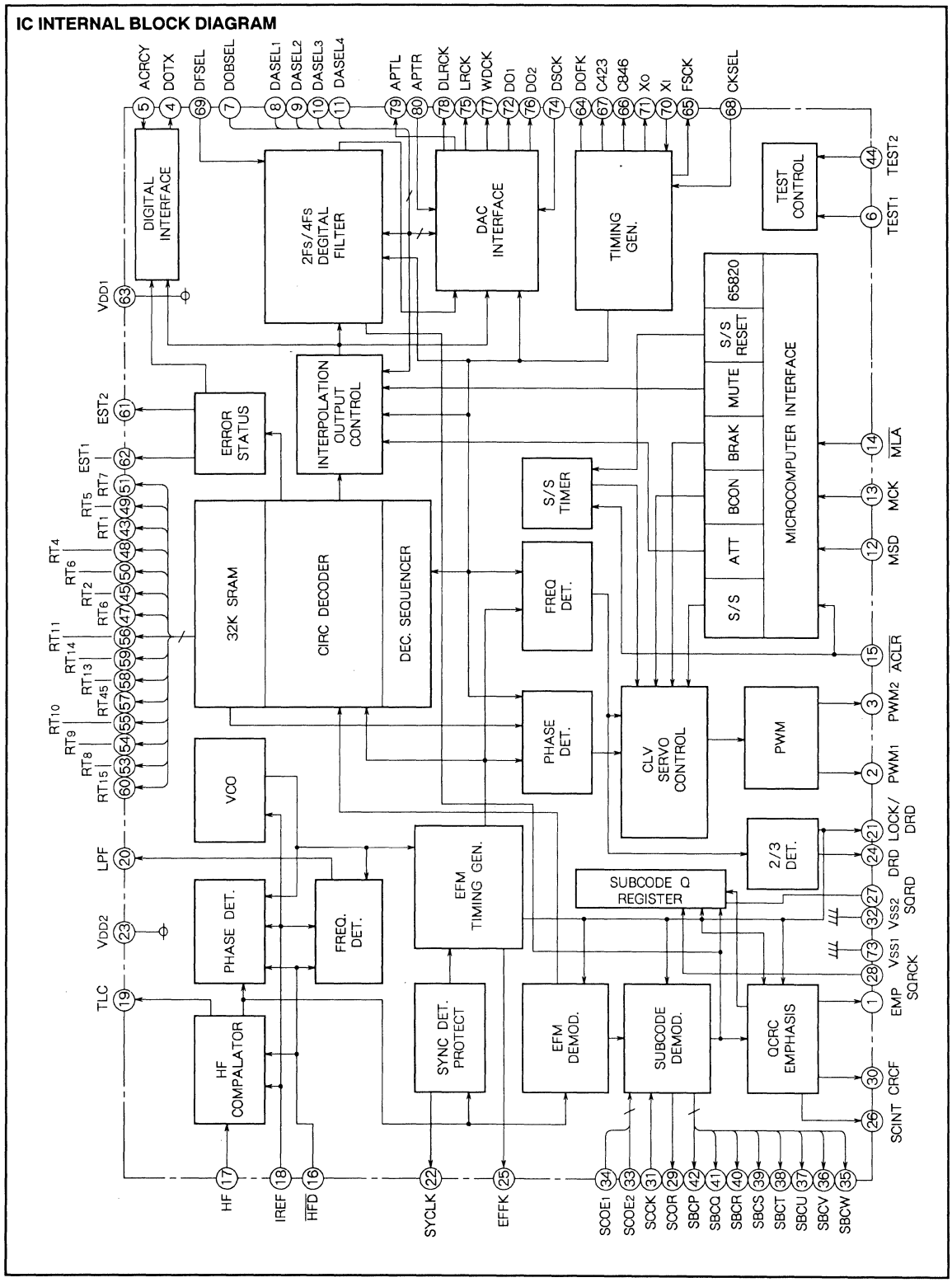
PIN CONFIGURATION



Outline 80P6N-A

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Name	I/O	Function
EMP	O	Emphasis flag output Emphasis = 1
PWM_1	O	Disk motor driving PWM output 1 −
PWM_2	O	Disk motor driving PWM output 2 +
DOTX	O	Output of digital interface
ACRCY	I	Clock accuracy input
$TEST_1$	I	Test control input Normal = 0
DOBSEL	I	Data bit select 18-bit = 1
$DASEL_1$	I	DAC interface format select 1
$DASEL_2$	I	DAC interface format select 2
$DASEL_3$	I	DAC interface format select 3
$DASEL_4$	I	DAC interface format select 4
MSD	I	Microcomputer interfece serial data input
MCK	I	Microcomputer interface shift cloc input
$\overline{MLA}$	I	Microcomputer interface data latch clock
$\overline{ACLR}$	I	Microcomputer interface register clear input
$\overline{HFD}$	I	High frequency signal detect
HF	I	High frequency signal input
IREF	I	Current referance
TLC	O	Output from slicon level control
LPF	I/O	PLL loop filter
LOCK/DRD	O	Lock status/Disc rotation down signal output
SYCLK	O	Frame lock status output. Lock = 1
V_{DD2}	I	V_{DD} for data slicer and V_{CO}
DRD	O	Disc rotation down signal output.
EFFK	O	EFM frame clock output duty ≒ 50 %
SCINT	O	Interrupt output of subcode Q
SQRO	O	Subcode Q register output
SQRCK	I	Subcode Q register
SCOR	O	Subcode sync output. $S_0 + S_1$
CRCF	O	Subcode Q CRC check flag output. CROCK = 1
SCCK	I	Shift clock input for serial subcode data output
V_{SS2}	I	Ground. 0V
$SCOE_2$	I	Enable input of subcode T∼Wch output 0 : High Z
$SCOE_1$	I	Enable input of subcode P∼Sch output 0 : High Z
SBCW	O	Subcode Wch output
SBCV	O	Subcode Vch output
SBCU	O	Subcode Uch output
SBCT	O	Subcode Tch output
SBCS	O	Subcode Sch output
MSD	O	Subcode Rch output

Name	I/O	Function
SBCQ	O	Subcode Qch output
SBCP	O	Subcode Pch output Pch∼Wch serial data output
RT_1	O	For internal RAM Test
$TEST_2$	I	Test control input Normal = 0 or open
RT_2	O	For internal RAM Test
NC	−	NO CONNECTION
RT_3	O	For internal RAM Test
RT_4	O	For internal RAM Test
RT_5	O	For internal RAM Test
RT_6	O	For internal RAM Test
RT_7	O	For internal RAM Test
NC	−	NO CONNECTION
RT_8	O	For internal RAM Test
RT_9	O	For internal RAM Test
RT_{10}	O	For internal RAM Test
RT_{11}	O	For internal RAM Test
RT_{12}	O	For internal RAM Test
RT_{13}	O	For internal RAM Test
RT_{14}	O	For internal RAM Test
RT_{15}	O	For internal RAM Test
EST_2	O	Error status 2. Error to be interpolated detected at C2
EST_1	O	Error status 1. Error detected at C1
V_{DD1}	I	Power supply 5V
DOFK	O	OSC frame clock output 7.35kHz duty=50%
FSCK	O	Clock output 44.1kHz (fs)
C846	O	Clock output 8.4672MHz
C423	O	Clock output 4.2336MHz
CKSEL	I	Crystal selector input 0 : 16.9344MHz 1 : 8.4672MHz
DFSEL	I	DF Attenuate selector input 1:-0.63dB 0:0dB
X_I	I	Crystal oscilLator input with internal feedback resistor
X_O	O	Crystal oscilLatoor output
DO_1	O	Dual DAC Rch serial data output
V_{SS1}	I	Ground 0V
DSCK	O	Data shift clock to DAC
LRCK	O	Lch/Rch clock to DAC or APTR clock
DO_2	O	Dual DAC Rch serial data output
WDCK	O	Word clock to DAC or APTL clock
DLRCK	O	Lch/Rch clock
APTL	O	DAC sampling clock Lch
APTR	O	DAC sampling clock Rch

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Uniit
V_{DD}-V_{SS}	Supply voltage		− 0.3～+ 7.0	V
V_I	Input voltage	(R_P = 0 Ω)	V_{SS}−0. 3≦V_I≦V_{DD}+0. 3	V
V_O	Output voltage		V_{SS}≦ V_O ≦ V_{DD}	V
V_P	Pull up voltage		V_P≦ V_{DD} + 2mA * R_P	V
T_{opr}	Operating temperature		−10～+70	℃
T_{stg}	Storage temperature		−40～+125	℃
P_d	Power dissipation		350	mW

R_P : Pull up resistor

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Applied pin	Limits			Unit
				Min	Typ	Max	
V_{DD}	Supply voltage			4.5	5.0	5.5	V
V_{IH1}	High-level input voltage 1		2)	V_{DD} *0.5	−	V_{DD}	V
V_{IH2}	High-level input voltage 2		1)	V_{DD} *0.7	−	V_{DD}	V
V_{IL1}	Low-level input voltage 1		2)	V_{SS}	−	V_{DD} *0.08	V
V_{IL2}	Low-level input voltage 2		1)	V_{SS}	−	V_{DD} *0.3	V
f_{OSC}	Oscillation frequency (X'tal)			−	8.46	−	MHz
f_{VCO}	Oscillation frequency (VCO)			−	8.64	−	MHz

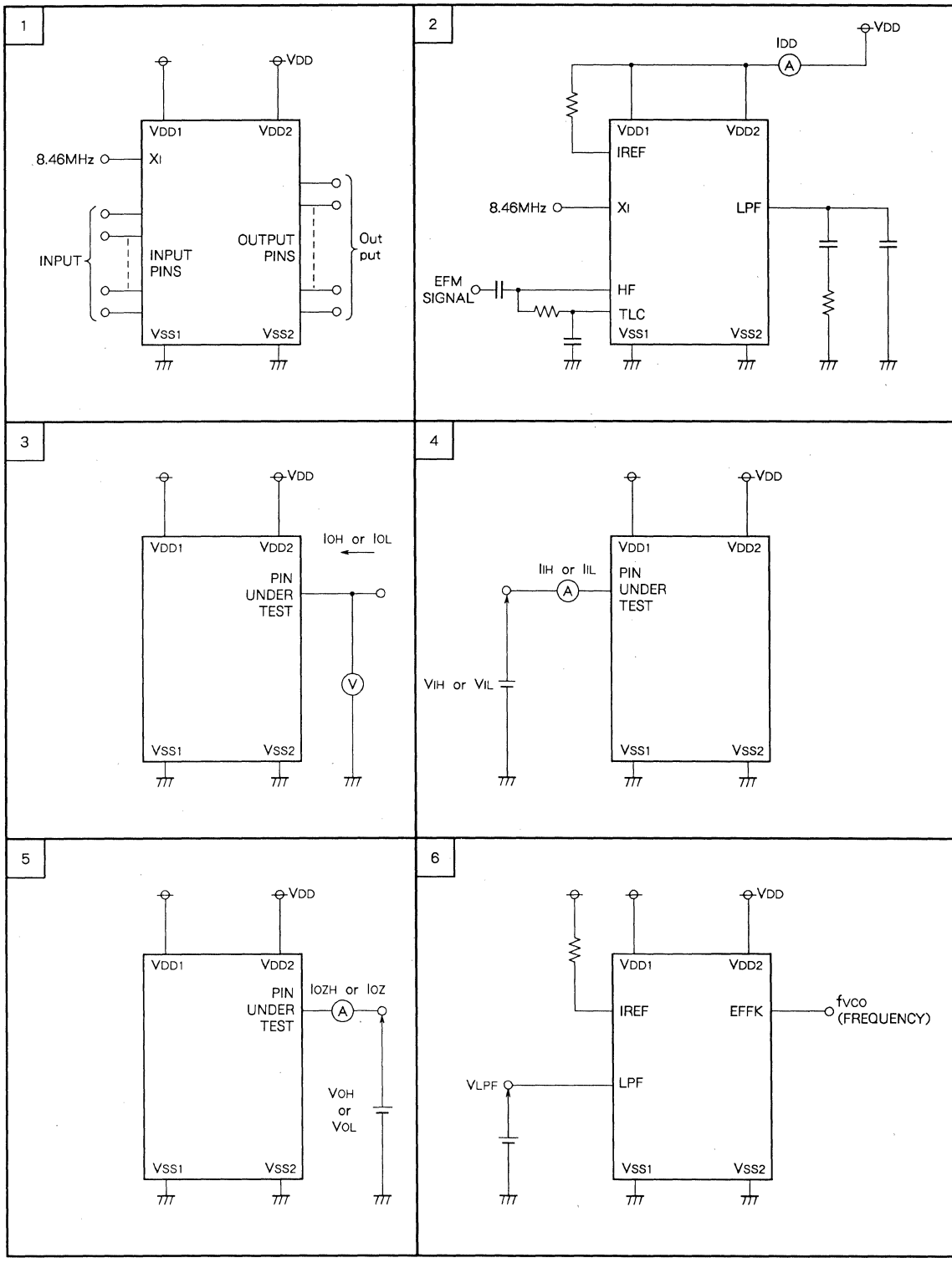
Note 1. Applied pin
1) DASEL1～DASEL4, ACRCY, DOBSEL, CKSEL, TEST1, TEST2
2) $\overline{HFD}$, SCOE1, SCOE2, SCCK, MSD, MCK, $\overline{MLA}$, $\overline{ACLR}$, SQRCK

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{DD} = 5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Applied pin	Test circuit	Limits			Unit
					Min	Typ	Max	
V_{DD}	Supply voltage	Ta = − 10～+ 70℃		1	4.5	5.0	5.5	V
I_{DD}	Circuit current	f_{OSC} = 8.4672MHz f_{VCO} = 8.6436MHz		2	−	−	40	mA
V_{OH}	High-level output voltage	V_{DD}=4.5V, I_{OH}= −0.8mA	3)	3	3.5	−		V
V_{OL}	Low-level output voltage	V_{DD}=4.5V, I_{OL}= 0.8mA	3)	3	−	−	0.4	V
I_{IH}	High-level intput current	V_{IH}= 4.5V	4)	4	−	−	2	μA
I_{IL}	Low-level intput current	V_{IL}= 0.5V	4)	4	−	−	− 2	μA
I_{OZH}	Off state high-level output current	V_{OH}= 4.5V	5)	5	−	−	2	μA
I_{OZL}	Off state low-level output current	V_{OL}= 0.5V	5)	5	−	−	− 2	μA
f_{VCO1}	VCO (EFFK) free running frequency	V_{LPF}= 1.0V		6	−	−	3.0	kHz
f_{VCO2}		V_{LPF}= 2.5V		6	6.5	7.35	−	kHz
f_{VCO3}		V_{LPF}= 4.0V		6	8.0	−	−	kHz

Note 2. Applied pin
3) Output and input/output pin except XO, TLC, LPF
4) Input pin except XI, IREF
5) SBCP～SBCW

TEST CIRCUIT



FUNCTIONAL DESCRIPTION

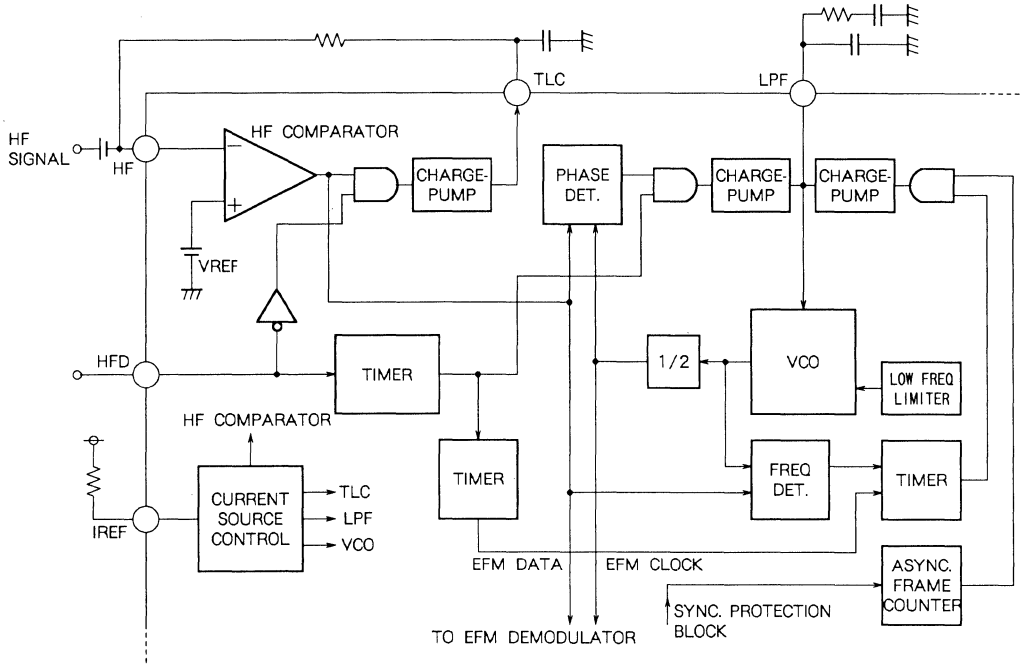
1. Data slicing/PLL

The M65820FP has an analog front-end for incoming HF (EFM) signal. Using CMOS-Analog technology, the front-end comprises an automatic slice level control circuit and EFM-PLL circuit with internal adjust-free VCO. The block-diagram shows the analog front-end. The HF signal is sliced by the HF comparator and a DC level is feed back from TLC to HF through the external CR. If HFD goes High because of a defect an disc, then TLC time off and holds the DC level.

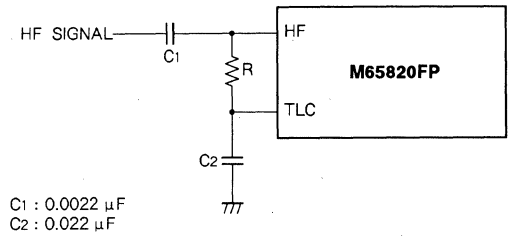
EFM-PLL extracts the EFM clock signal from the HF signal. The PLL circuit has a phase/frequency comparator providing the M65820FP with a wide capture/lock range. There is no need to adjust the VCO. LPF is the charge-pump output and same-time control voltage input to the VCO. LPF froms off if HFD goes High.

IREF is the reference current input used to determine the current of charge pumps of TLC and LPF, operating point of HF comparator and VCO free running frequency. If IREF is connected to a noisy power supply through a resistor, VCO is modulated and the error-rate increases. Therefore, power supply noise at IREF must be held to a minimum.

BLOCK DIAGRAM (Data slicing/PLL)



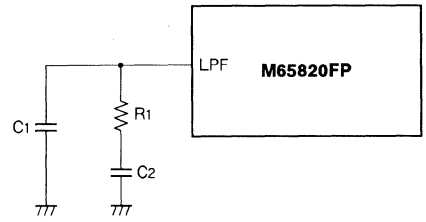
(1) Automatic slice level control



C1 : 0.0022 μF
C2 : 0.022 μF
R : 33k Ω
Vin : HF0.5VP-P Min

The slice level control circuit is formed by connecting a resistor and capacitors to the HF (High-Frequency signal input) and TLC (slice level control oputput) pins.

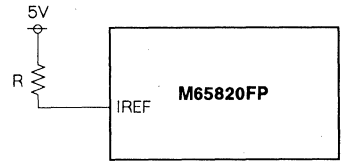
(2) PLL



C1 : 470pF
C2 : 0.15 μF
R1 : 2.2k Ω

Since the adjustment-free VCO is built in, the adjustment-free PLL circuit can be formed by connecting a resistor and capacitors to the LPF (low-pass filter) pin.

(3) Reference current



R : 100k Ω

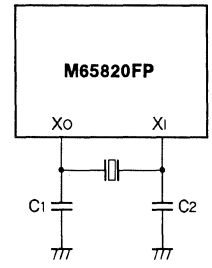
A resistor must be connected between the IREF pin and V_{DD} in order to set the reference current used in determining the current values of the TLC pin and LPF pin, the comparator operating current of the slice level control circuit, and the VCO free-run frequency.

2. Demodulation/Decoding

The EFM signal converted to logic level and the EFM clock extracted from the EFM signal are input to the demodulator and decoder block.

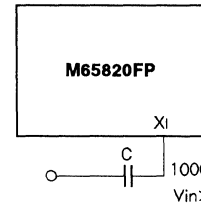
The EFM demodulator must be synchronized to the EFM clock. The decoder uses the clock from the X'tal oscillator. Jitter between the EFM signal and output of the decoder is absorbed by external RAM.

(1) Clock generator



CKSEL = H
X'tal : 8.4672MHz
C1 : 30pF
C2 : 30pF
or
CKSEL = L
X'tal : 16.9344MHz
C1 : 10pF
C2 : 10pF

(a) The oscillation circuit can be formed by connecting a X'tal oscillator(8.4672MHz or 16.9334MHz) and load capacitors to pins X_I and X_O.



(b) When the system contains a clock (8.4672MHz or 16.9334MHz), the clock can be input to pin X_I via a capacitor without using the X'tal oscillator. If the input signal is logic level, the capacitor is not necessary.

(2) Frame synchronization

EFM demodulating is done by Programmable Logic Array Conversion table. The demodulator must be synchronized to the EFM signal for each frame. The frame sync protection circuit holds the synchronization ever if the sync pattern is lost and prevents false synchronization of the demodulator when bit-slipping or mis-synchronization occurs.

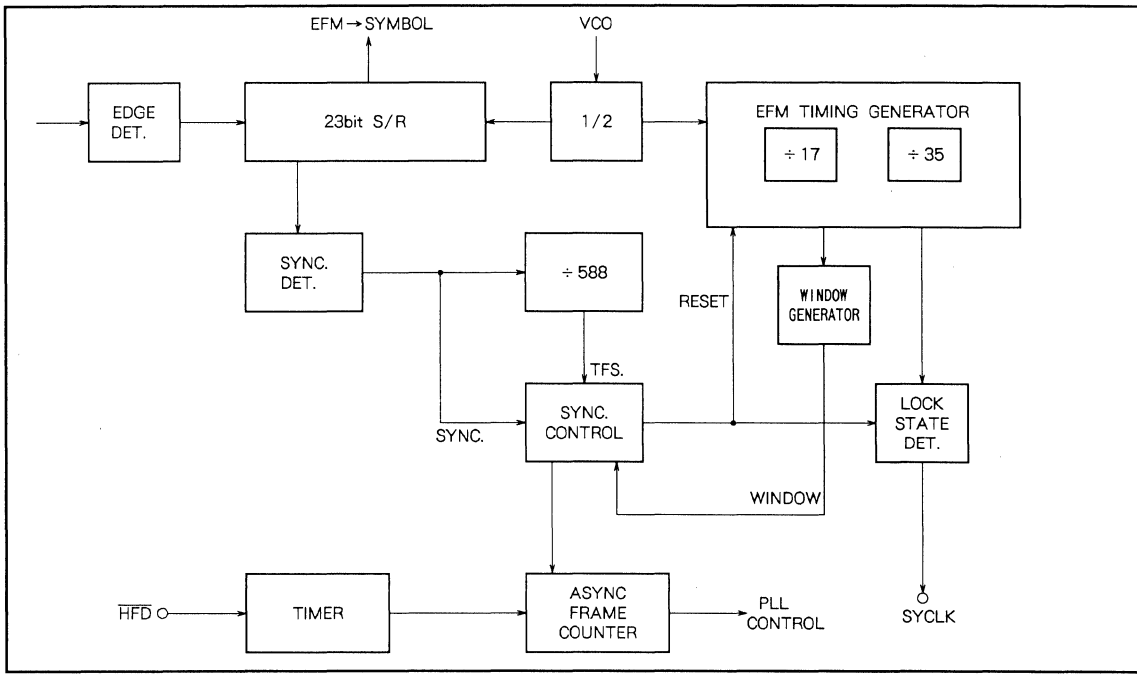


Fig. 1 Frame synchronization block diagram

The generating condition of the counter reset signal (Reset) in the EFM timing generator is indicated as follows:

Reset = (Sync * Tfs) + (Sync * Window)

* : Logical product

\+ : Logical sum

Sync : Synchronizing signal

Tfs : Detection signal of synchronizing signal space = 588

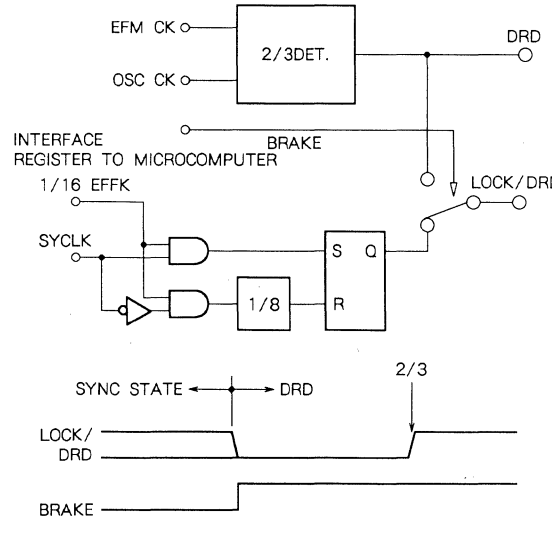
Window : Window signal ± 7ck

In the synchronous state, Sync and Tfs generate simultaneously and Sync comes to the center of the window. At this time, 1 is output to the SYCLK pin.

Frame sync status is output to the SYCLK pin. The SYCLK output includes some bounce when the sync pattern is lost because of a defect an disc. Hence, there is a need for debouncing the sync status signal to monitor by the system control microcomputer.

This debouncing is in the M65820FP by monitoring the frame sync status at 1/16 EFM frame clock intervals and then outputting the result to the LOCK/DRD pin. If the monitored status is locked then output is High, Eight. Unlocked outputs becomes Low.

LOCK/DRD pin outputs DRD signal (see Sec. 3) when the disnotor is braking by command from microcomputer. The following pages contain the block diagram and the output timing.



(3) Subcode demodulation

Among data converted from 14-bits EFM signal to 8-bits symbols, subcodes P, Q, R, S, T, U, V and W are output to pins SBCP-SPCW repectively. When the subcode synchronizing patterns S_0 or S_1 is detected as synchronizing signals of subcode data, the synchonizing signals are output to the SCOR pin.

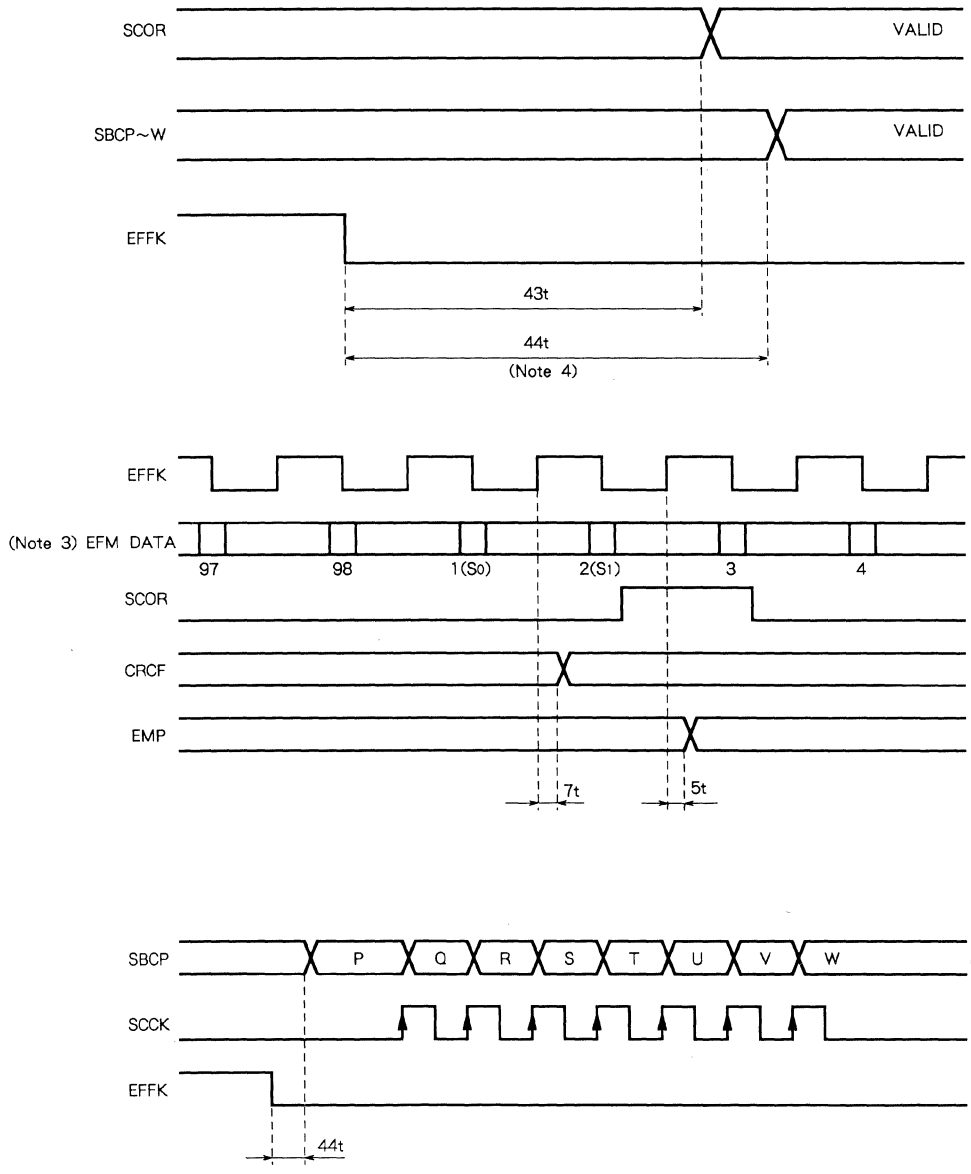
Pins SBCP-SBCW are a Three-State output system controlled by pins $SC0E_1$ and $SC0E_2$ as shown in the table below.

A CRC check is deve for the Q channel data, and if the data is correct, a 1 is output to the CRCF pin. The EMP pin displays whether or not emphasis is present. The subcode data is not only output in parallel, but also can be obtained serially via SBCP, by inputting a clock to SCCK.

Subcode output timing are shown Fig. 2.

SUBCODE DEMODULATION

$SC0E_1$	$SC0E_2$	SBCP	SBCQ	SBCR	SBCS	SBCT	SBCU	SBCV	SBCW
0	0	High-impedance				High-impedance			
1	0	P	Q	R	S	High-impedance			
0	1	High-impedance				T	U	V	W
1	1	P	Q	R	S	T	U	V	W



Note 3. Subcode block No. in the EFM data
4. t : Oscillating frequency (VCO)
(typically : 1/8.6436MHz = 115.7ns.)
5. When input frequency to SCCK is more than 8ck, SBCP becomes 0.

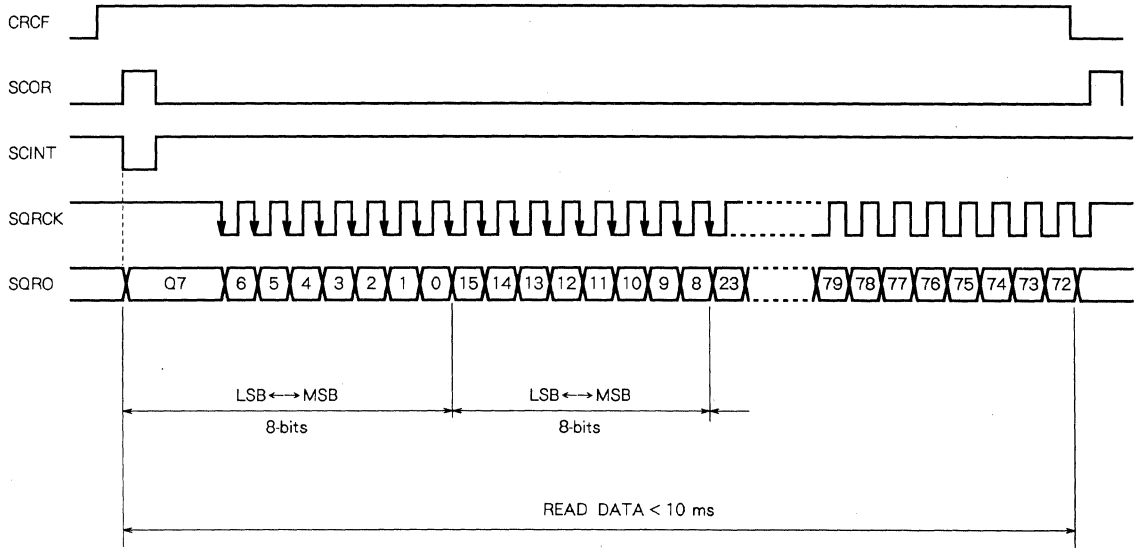
Fig. 2 Subcode output timing

(4) Subcode Q register

Subcode Q-channel data are output to SBCQ pin.

The M65820FP stores the Q data in an 80-bit shift register. If CRC is OK, the system control microcomputer can access the Q data from the SBCQ pin by inputting the read-out clock to SQRCK pin. If the CRC check is OK, the M65820FP outputs the interrupt signal to the microcomputer from SCINT, synchronized with SCOR (Subcode sync) signal.

Timing chart



(5) CIRC decoding

A 32K-bit Static RAM is needed as internal memory for temporary storage to process CIRC decoding (C1 decoding, C2 decoding, unscramble and de-interleave) and output interpolation. By using a 32K RAM, jitter is absorbed up to ± 8 frames (max.).

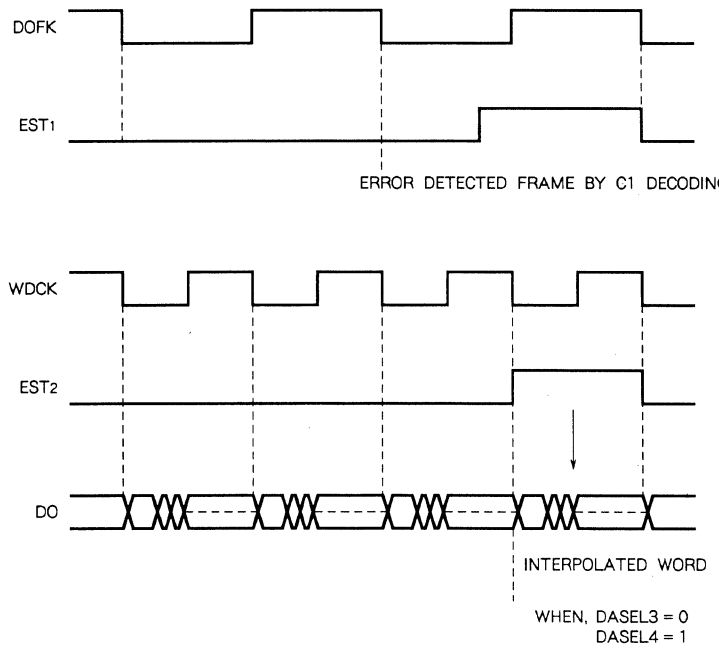
When CIRC decoding, double error correction is used for both C1 and C2 decoding.

When correction is not possible, average interpolation or pre-hold interpolation is perfomed. Error states detected during decoding are output to pins EST_1 and EST_2.

When an error is detected by C1 deoding, a 1 is output to pin EST_1. When an error word is judged imcorrectable by C2 decoding, a 1 is output to pin EST_2.

The putput timings for pins EST1 and EST2 are as follows :

Timing chart

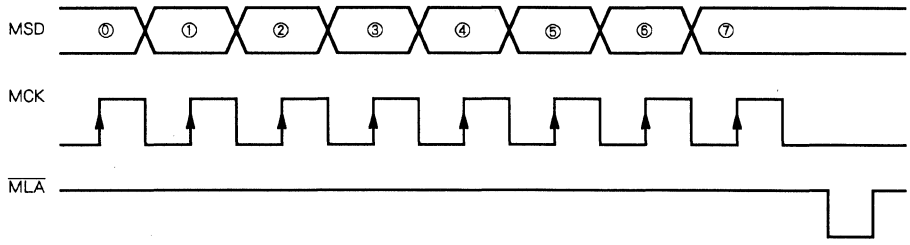


3. Microcomputer Interface

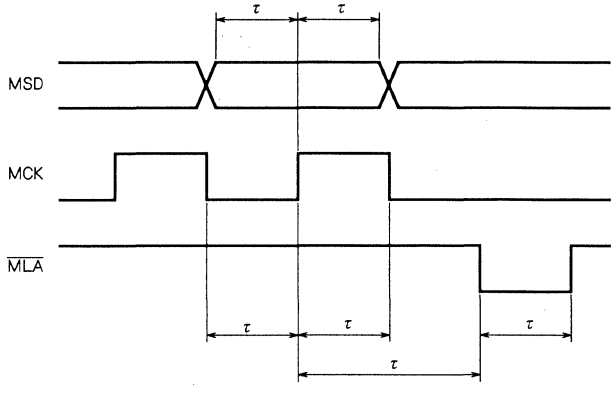
CLV servo, MUTE, and ATT system are controlled by serial commands from the microcomputer.

The timing, names, and functions of each control register are as follows :

Timing chart



⓪ DUMMY (Don't care).	X
① S/S (START/STOP) register.	start = 1
② BCON (BRAKECONTROL) register.	enable = 1
③ BRAK (BRAKE) register.	brake = 1
④ ATT (ATTENUATE) register.	−12dB = 1
⑤ $\overline{\text{MUTE}}$ register.	muting = 0
⑥ S/S timer reset register.	reset = 1
⑦ IC code.	M65820FP = 1



τ min : 500ns

Function of microcomputer interface registers

Register No.	Register name	Function	Operation		Note
			0	1	
⓪	DUMMY	Don't care	–	–	
①	S/S (START/STOP)	Controls START/STOP of the disk motor	DISC MOTOR STOP (OFF)	DISC MOTOR START (ON)	0 by $\overline{ALCR}$
②	BCON (BRAKECONTROL)	Determines if BRAKE control is necessary	BRAKE 0.3sec.	BRAKE is controlled by BRAKE register	0 by $\overline{ALCR}$
③	BRAK (BRAKE)	Controls BRAKE	BRAKE OFF (MOTOR OFF)	BRAKE ON	When BCON = 1
④	ATT (ATTENUATE)	Sets attenuation (−12dB)	0dB	−12dB	When MUTE = 1
⑤	MUTE	Sets the muting	−∞dB	0dB	0 by $\overline{ALCR}$
⑥	S/S timer reset	Resets S/S timer which sets time of KICK and BRAKE to 0.3sec.	S/S timer enable	S/S timer disable	1 by $\overline{ALCR}$
⑦	IC code	Distinguishes command to the M65821FP	–	Executing command	0 is code for M51564P

Examples of system control are as follows :

Operation \ Register name	⓪ DUMMY	① S/S	② BCON	③ BRAK	④ ATT	⑤ $\overline{MUTE}$	⑥ S/S timer reset	⑦ IC code
								0
MUTE						0		1
ATT					1	1		1
0.3sec.KICK→CLV		1					0	1
0.3sec.BRAKE→MOTOR OFF		0	0				0	1
BRAKE		0	1	1			0	1
MOTOR OFF		0	1	0			0	1
0.3sec. timer disable							1	1
MOTOR off(without 0.3sec. BRAKE)		0	0				1	1
CLV (without 0.3sec. KICK)		1	0				1	1
The following is example of the most simplified system control sequence.								
STOP		0	0	0	0	0	1	1
0.3sec. KICK→CLV		1	0	0	0	0	0	1
PLAY		1	0	0	0	1	0	1
FF/FR		1	0	0	1	1	0	1
PLAY		1	0	0	0	1	0	1
0.3sec. BRAKE→STOP		0	0	0	0	0	0	1

* The blanks mean "Don't care"or that other commands can be used simultaneously.
* KICK period can be extended by repetition of start procedure.
* Software developed on the M50423FP can be utilized on the M65820FP (fully compatible).
* Software developed on the M50422P/M50427FP can be utilized on the M65820FP (upward compatible). However, when using this software, the following functions on the M65820FP are not available: subcode Q-register, subcode Q-interrupt signal LOCK/DRD output.

When the M65820FP detects that the number of rotations is less than 2/3 that of the normal play state, it outputs the disc rotation deterioration signal to the DRD pin. By using this signal in the following stop sequence, the disc can be correctly stopped.

Operation or μ-COM Operation \ Register name	⓪ DUMMY	① S/S	② BCON	③ BRAK	④ ATT	⑤ $\overline{MUTE}$	⑥ S/S timer reset	⑦ IC code
PLAY		1	0	0	0	1	0	1
BRAKE		0	1	1	0	0	0	1
($\overline{HFD}$: H checking by microcomputer)								
(Measuring t_{DRD} (DRD : 0→1) after BRAKE start								
(Stop $\overline{HFD}$ checking and) additional BRAKE time 2 × t_{DRD}								
MOTOR OFF		0	1	0	0	0	0	1

The DRD signal is output to both the DRD pin and also the LOCK/DRD pin during the braking period.

To reset the microcomputer interface register to the initial state, execute $\overline{ACLR}$ (M65820FP clear) immediately after turning the power on.

4. Digital filter

The M65820FP converts the sampling frequency of audio data from 44.1kHz (fs) to 88.2kHz (2fs) or 176.4kHz (4fs) by an overflow limited, FIR linear-phase digital filter.

Digital filter selection is done using pins DASEL1~DASEL4. Table 1 shows the digital filter and DAC interface mode. Degital filter by pass mode with no interpolation of umcorrectable data is designed for non-audio applications such as CD-ROM or CD-1. The digital filter by pass mode with interpolation is used for external precision digital filter applications.

Fig. 3 (a) shows the characteristics of the 2fs digital filter.

Fig. 3 (b) shows the characteristics of the 4fs digital filter.

5. D-A converter interface

The M65820FP has many different DAC Interface formats. The desired format is selected using pins DASEL1~DASEL4.

Timing signals, data and clocks automatically change to correspond to the digital filter, fs (pass)/2fs/4fs, is selected.

If the 4fs digital filter mode is selected then the dual DAC mode and 18-bit data out mode are available.

Table 1 shows the interface modes.

Fig. 4 (a) ~Fig. 4 (e) show the timings if interface to DAC.

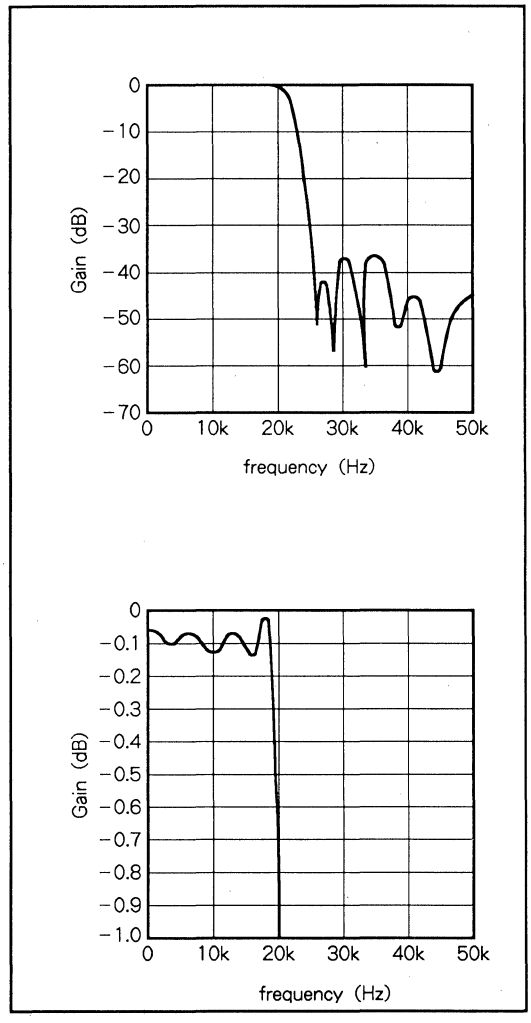


Fig. 3 (a) Frequency characteristics of the digital filter (Sampling frequency 88.2kHz:2fs)

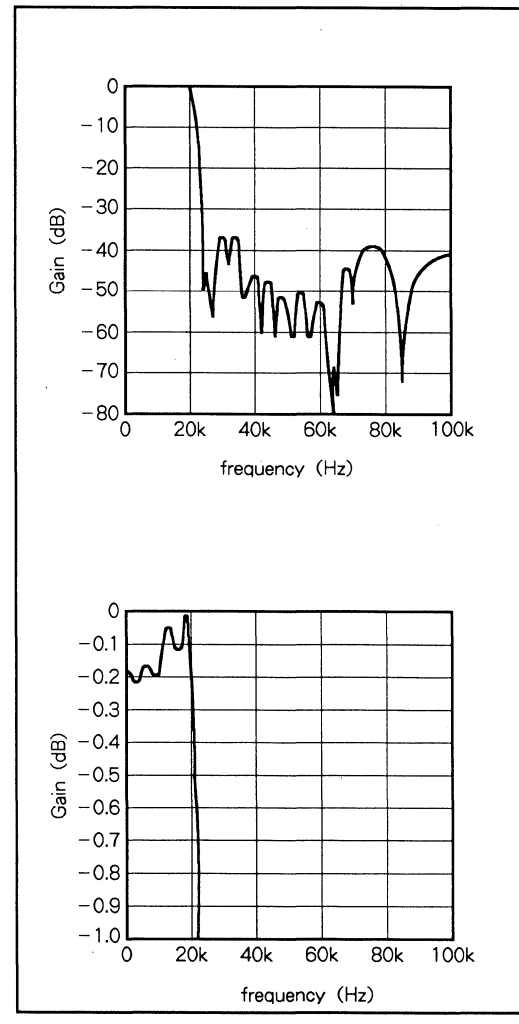


Fig. 3 (b) Frequency characteristics of the digital filter (Sampling frequency 176.4kHz:4fs)

Table 1 DAC Interface modes

MODE	DASEL 1	DASEL 2	DASEL 3	DASEL 4	DF	MSB/LSB 1st	Note	Timing chart
1	0	0	0	0	2fs	MSB 1st		Fig. 4 (a)
2	0	0	0	1	(fs)	MSB 1st	Bypass filter	Fig. 4 (a)
3	1	0	0	0	2fs	LSB 1st		Fig. 4 (b)
4	1	0	0	1	(fs)	LSB 1st	Bypass filter	Fig. 4 (b)
5	1	0	1	0	4fs	MSB 1st		Fig. 4 (c)
6	1	0	1	1	4fs	MSB 1st	Dual DAC	Fig. 4 (d)
7	0	1	0	1	(fs)	MSB 1st	Interpolation	Fig. 4 (a)
8	1	1	0	0	2fs	MSB 1st		Fig. 4 (e)
9	1	1	0	1	(fs)	MSB 1st	Bypass filter	Fig. 4 (e)

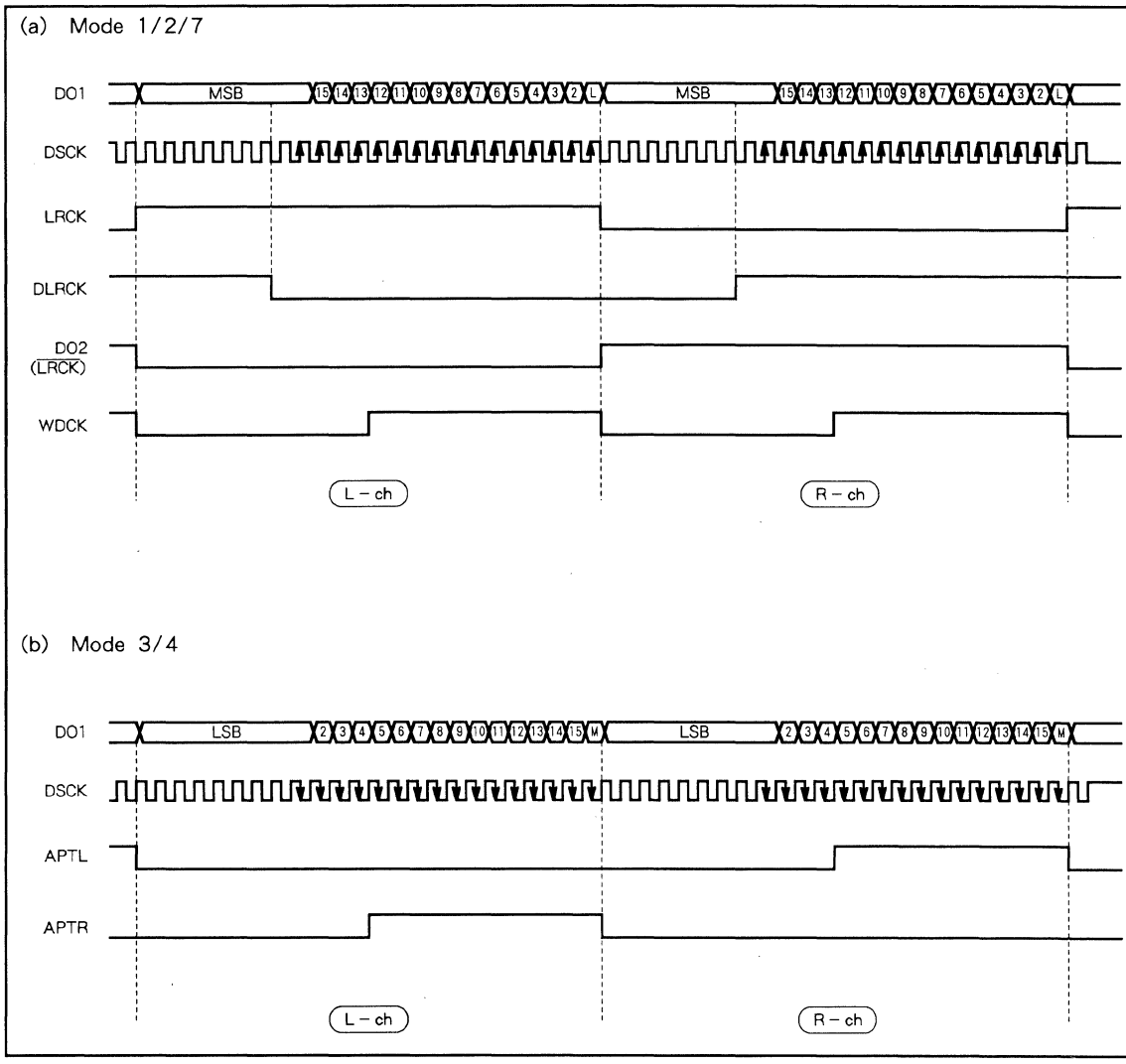


Fig. 4 DAC Interface timing chart

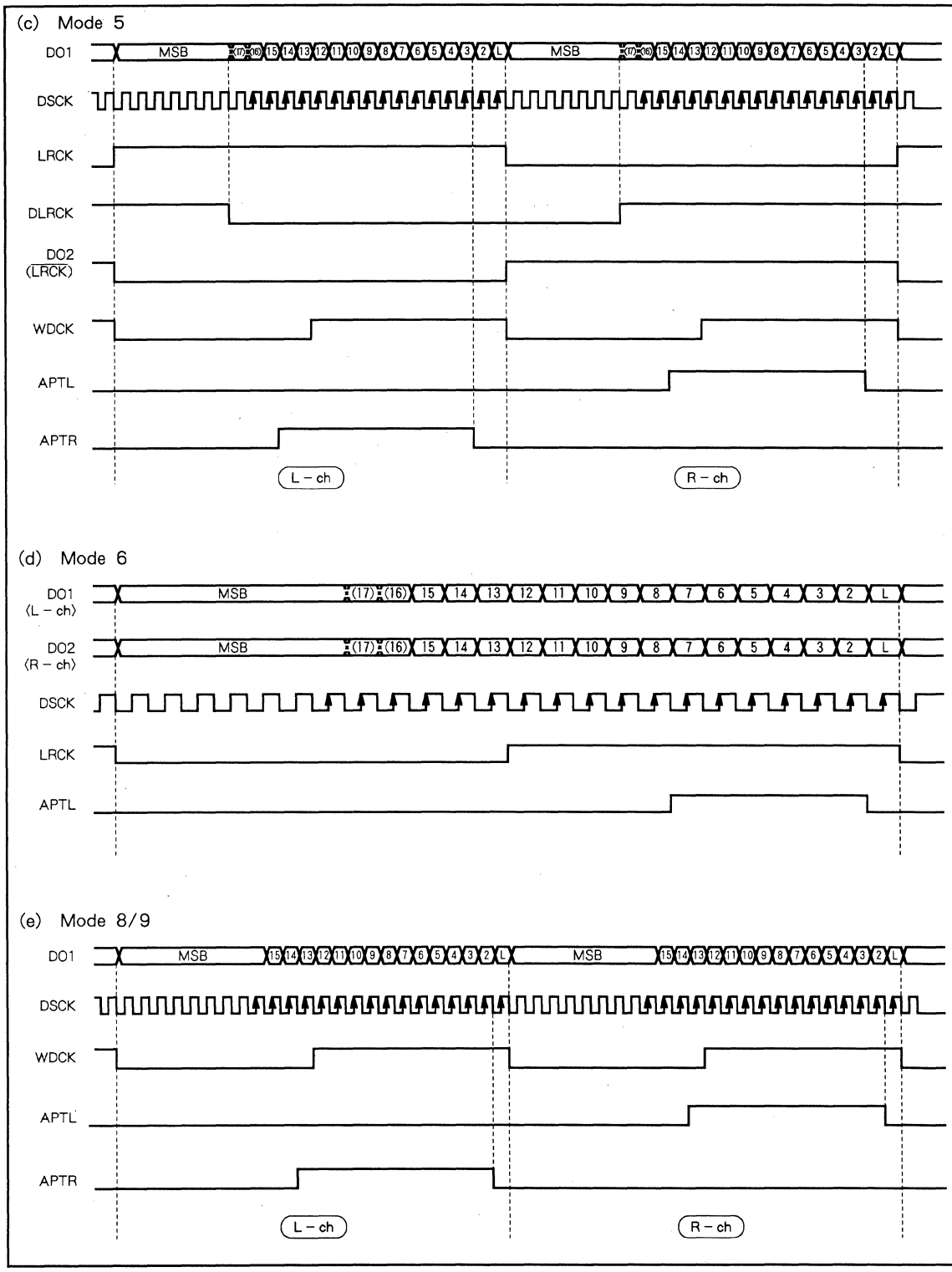
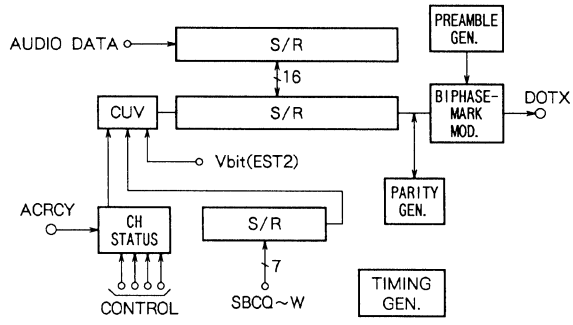


Fig. 4 DAC interface timing chart

6. Digital interface output

The M65820FP outputs digital interface signal conforming to EIAJ CP-340 or IEC formats.

The block diagram shows the digtal interface and Fig. 5 shows the timings. Channel status clock accuracy can handle variable pitch control and can be set using the ACRCY pin. Clock accuracy is level II when ACRCY pin is Low, and level III when ACRCY pin is High.



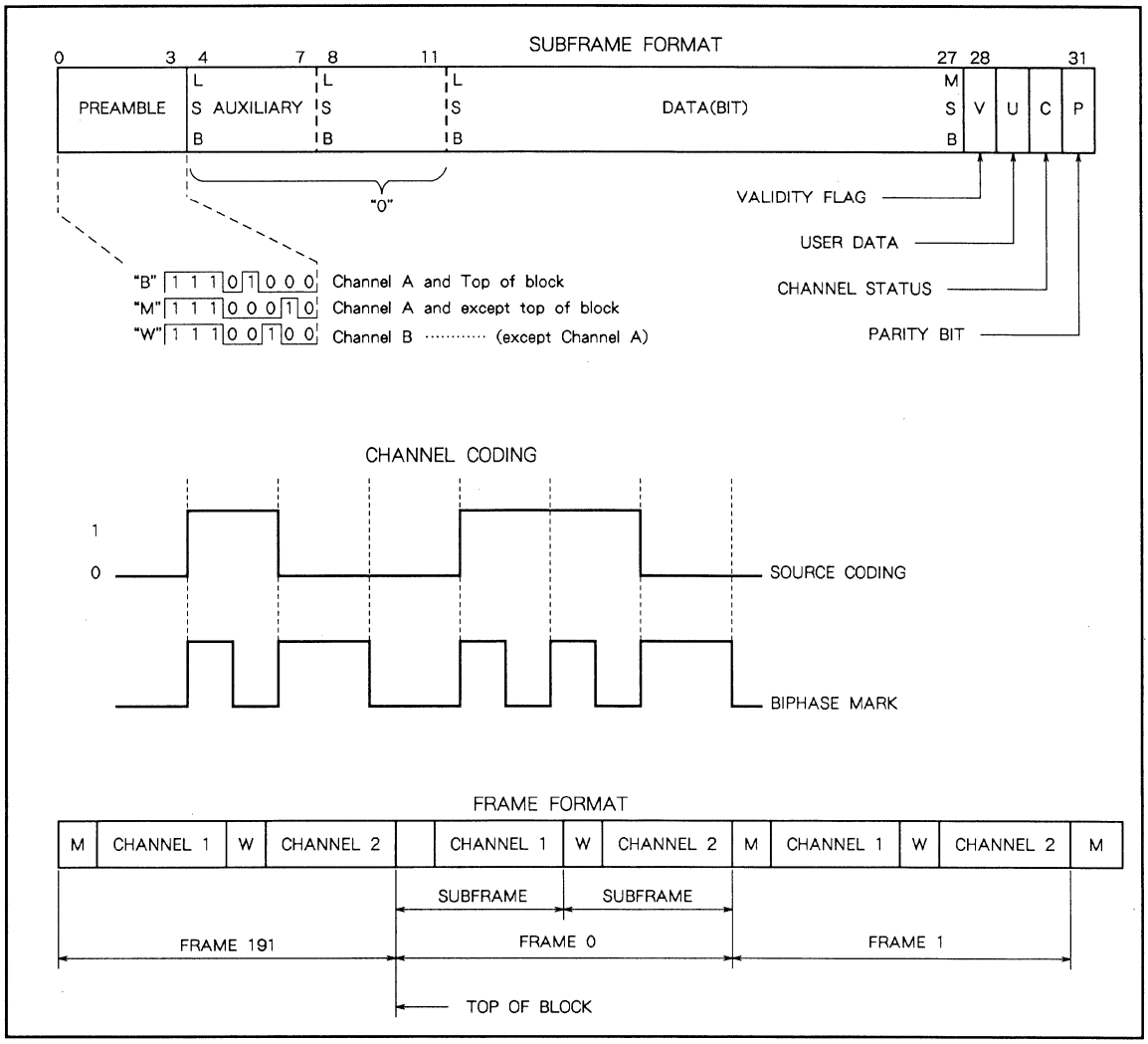


Fig. 5 Timing

7. CLV servo control circuit

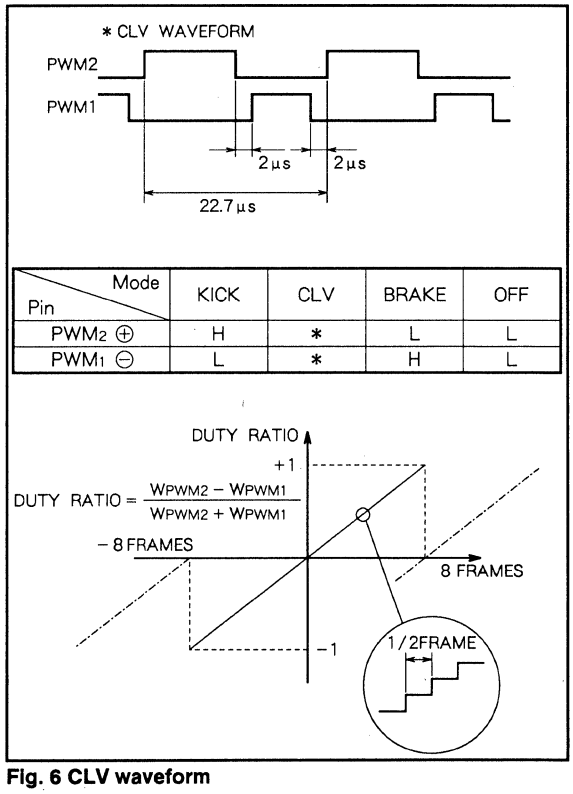
CLV servo control circuit operates using two signals. The first is the frequency difference beween the EFM-clock and X'tal -clock. The second is the phase difference beween the write-frame address and read-frame address of the internal 32k RAM. Motor control signals are output to PWM_1 (− signal) and PWM_2 (+ signal). Because these singals are internally phase compensated, the CLV servo control circuit can be easily formed using current drivers on pins PWM_1 and PWM_2.

Fig. 7 shows the CLV, waveform and its duty cycle when the CIRC decoding block addressing write-frame address and the read-frame address exceeds ± 8frames.

When this occurs the duty cycle of the CLV waveforms will be reset to 0.

The disc motor can be driven by PWM waveforms directly or by an analog signal that can be generated by integratiing the PWM waveforms.

By using an analog signal, it is possible to adjust the servo loop-gain by varying direct external component values. But in the case of PWM waveforms, the servo loop-gain is determined by motor torque, and the rotating moment of the disc, turntable, and disc clamper.



Pin \ Mode	KICK	CLV	BRAKE	OFF
PWM_2 ⊕	H	*	L	L
PWM_1 ⊖	L	*	H	L

Fig. 6 CLV waveform

M65820AFP

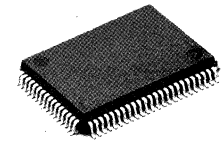
CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN MEMORY

DESCRIPTION

The M65820AFP is a CMOS IC developed for compact disc (CD) sound reproducing applications. It has built-in memory, adjustment-free PLL, error correction circuitry, etc. and is used in a CD digital signal processing section.
Applications include also CD-ROM and CD-G, as well as CD-DA.

FEATURES

- Includes 32k SRAM
- Includes HF comparator
- Non-tuning EFM-PLL circuit (Includes VCO)
- Strong sync. protect
- 2 error correction
- ± 8 frames jitter margin
- Digital CLV servo control
- Includes linear phase digital filter
- MSB/LSB first output DAC interface
- Dual DAC available (with 4 times oversampling)
- 18-bits output avairable (with 4 times oversampling)
- Digital output avairable

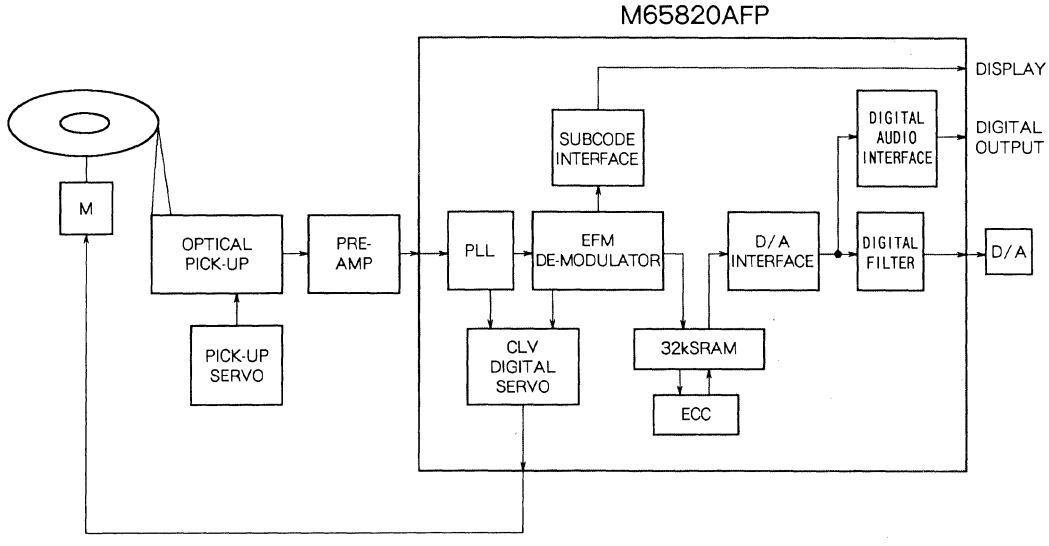


Outline 80P6N-A
0.8mm pitch QFP
(20.0mm × 14.0mm × 2.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{DD} = 4.5~5.5V
Rated supply voltage ····· V_{DD} = 5V
Rated power dissipation ····· 100mW

SYSTEM CONFIGURATION



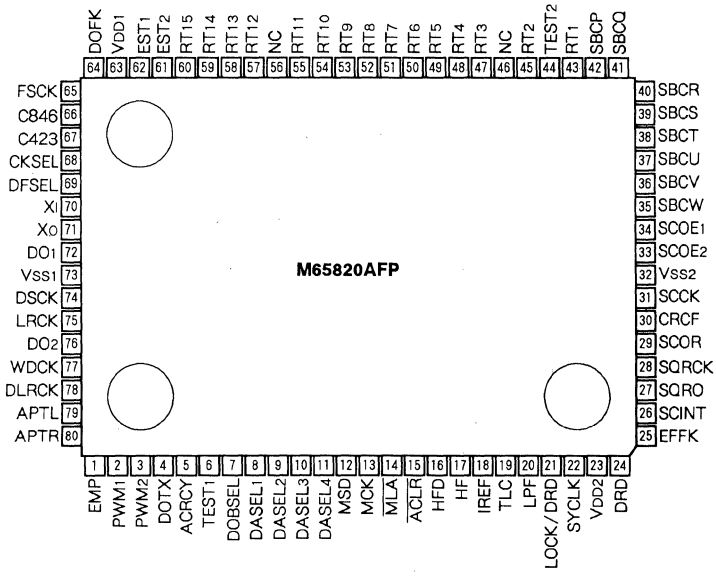
M65820AFP

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN MEMORY

BUILT-IN FUNCTIONS

- Adjustment-free EFM-PLL
  - Slice level control
  - Bit clock generation
  - Adjustment-free VCO
- Demodulation/Decoding
  - EFM demodulation
  - Sync detection/protection/insertion of frame
  - Subcode demodulation (serial output)
  - Subcode CRC check
  - Subcode Q register
  - Emphasis detection
  - ±8 frames of jitter absorption
  - CIRC decoding
    - Unscramble
    - Deinterleave
    - Correction ability C1 : double, C2 : double
  - Interpolation (mean value interpolation and holding preceding value)
  - Possible to inhibit interpolation
  - Mute
  - Attenuation (−12dB)
  - Dual DAC output available
- Digital filter
  - Selection available from 2 times and 4 times over sampling
  - Digital filter through output
  - 18bit output (if quadruple over sampling is selected)
- CLV digital servo
  - Detects low disc revolution
  - PWM output
- Microcomputer interface
  - Mute, attenuation, disc motor ON/OFF, and disc motor brake control
  - Power on reset available
- Digital audio interface
  - Digital out
- Master clock selection
  - Choice from 8.4672 or 16.9344MHz of master clock

PIN CONFIGURATION

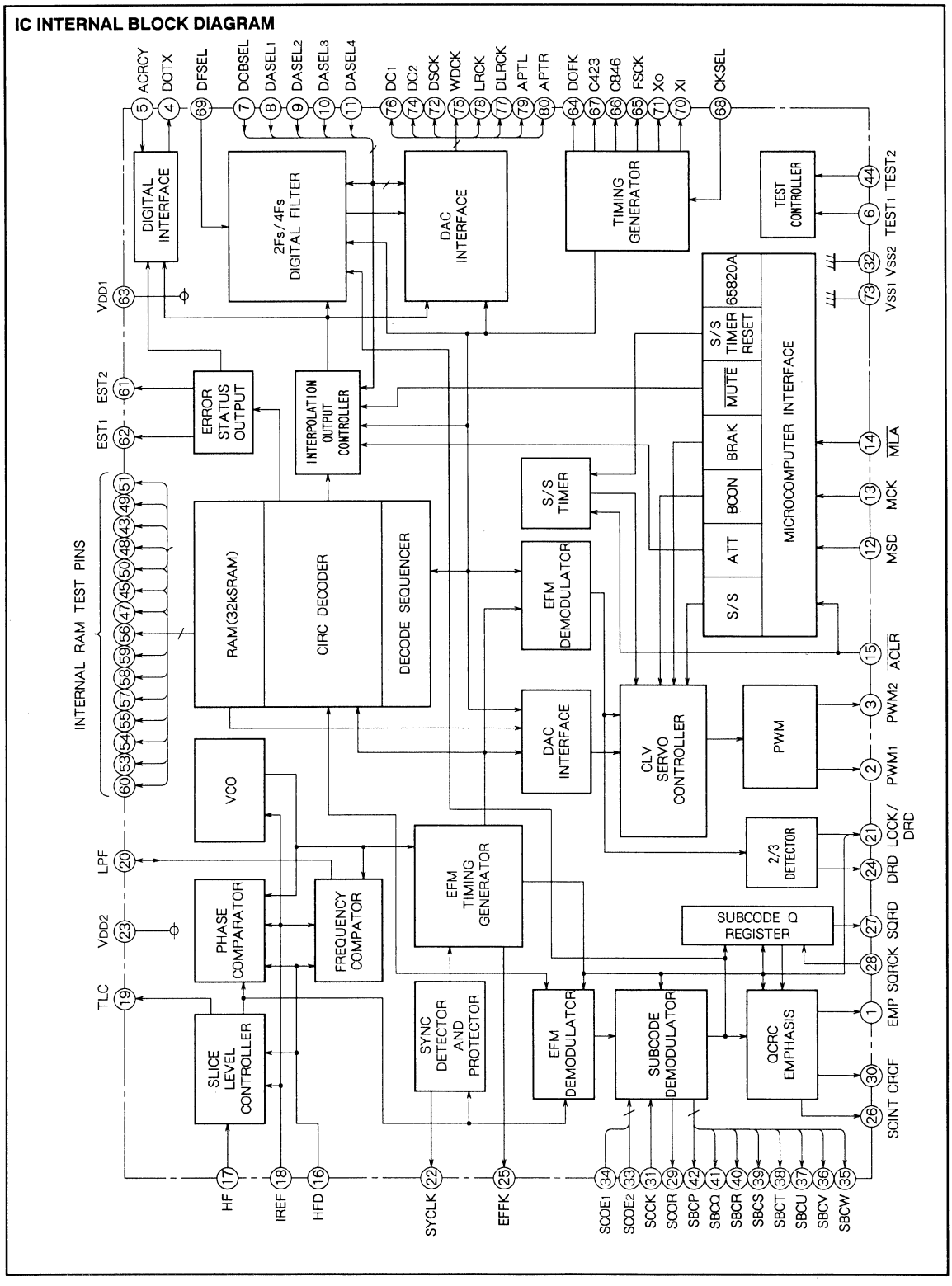


Outline 80P6N-A

NC : NO CONNECTION

MITSUBISHI ELECTRIC

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Name	Type	Function
①	EMP	O	Emphasis code output Set to "H" if emphasis is enabled
②	PWM1	O	PWM output 1 to drive disc motor. − (negative)
③	PWM2	O	PWM output 2 to drive disc motor. + (positive)
④	DOTX	O	Digital out
⑤	ACRCY	I	Digital out channel status Clock accuracy input
⑥	TEST1	I	Test mode selection input,normal reproduction = "L"
⑦	DOBSEL	I	Selection of number of bits for output data, 18bits = "H"
⑧	DASEL1	I	DAC interface selection input 1
⑨	DASEL2	I	DAC interface selection input 2
⑩	DASEL3	I	DAC interface selection input 3
⑪	DASEL4	I	DAC interface selection input 4
⑫	MSD	I	Microcomputer interface serial data input
⑬	MCK	I	Microcomputer interface Shift clcok input
⑭	$\overline{\text{MLA}}$	I	Microcomputer interface Data latch clock input
⑮	$\overline{\text{ACLR}}$	I	Microcomputer interface Register clear input
⑯	HFD	I	Signal input indicating missing of reproduction signal
⑰	HF	I	Reproduction signal input
⑱	IREF	I	Reference current input for detector /PLL circuit
⑲	TLC	O	Slice level control output
⑳	LPF	I/O	PLL loop filter connection pin
㉑	LOCK/ DRD	O	Output of sync state/low disc revolution state
㉒	SYCLK	O	Frame sync state output. Set to "H" if in sync
㉓	VDD2	I	Detector/PLL circuit Power supply dedicated to analog section, 5V
㉔	DRD	O	Low disc revolution state output
㉕	EFFK	O	EFM flame clock output duty ≒ 50 %
㉖	SCINT	O	Signal output to interrupt subcode Q output
㉗	SQRO	O	Subcode Q register output
㉘	SQRCK	I	Subcode Q register Data shift clock input
㉙	SCOR	O	Subcode sync signal output, S0 + S1
㉚	CRCF	O	Outputs CRC check result of subcode Q CRC OK = "H"
㉛	SCCK	I	Shift clock input for subcode serial output
㉜	VSS2	I	GND 0V
㉝	SCOE2	I	Input to enable SBCT~SBCW outputs
㉞	SCOE1	I	Input to enable SBCP~SBCS outputs

Pin No.	Name	Type	Function
㉟	SBCW	O	Subcode Wch output
㊱	SBCV	O	Subcode Vch output
㊲	SBCU	O	Subcode Uch output
㊳	SBCT	O	Subcode Tch output
㊴	SBCS	O	Subcode Sch output
㊵	SBCR	O	Subcode Rch output
㊶	SBCQ	O	Subcode Qch output
㊷	SBCP	O	Subcode Pch output
㊸	RT1	O	Internal memory test pin
㊹	TEST2	I	Test mode selection input,normal reproduction = "L"
㊺	RT2	O	Internal memory test pin
㊻	NC	−	No connection
㊼	RT3	O	Internal memory test pin
㊽	RT4	O	Internal memory test pin
㊾	RT5	O	Internal memory test pin
㊿	RT6	O	Internal memory test pin
(51)	RT7	O	Internal memory test pin
(52)	RT8	O	Internal memory test pin
(53)	RT9	O	Internal memory test pin
(54)	RT10	O	Internal memory test pin
(55)	RT11	O	Internal memory test pin
(56)	NC	−	No connection
(57)	RT12	O	Internal memory test pin
(58)	RT13	O	Internal memory test pin
(59)	RT14	O	Internal memory test pin
(60)	RT15	O	Internal memory test pin
(61)	EST2	O	Error state output 2 C2 decoder uncorrectable = "H"
(62)	EST1	O	Error state output 1 C1 decoder uncorrectable = "H"
(63)	VDD1	I	Power supply, 5V
(64)	DOFK	O	OSC frame clock output 7.35kHz, duty = 50 %
(65)	FSCK	O	Clock output, 44.1kHz,
(66)	C846	O	Clock output, 8.4672MHz
(67)	C423	O	Clock output, 4.2336MHz
(68)	CKSEL	I	Crystal oscillator frequency selection input "H" = 8.4672MHz "L" = 16.9344MHz
(69)	DFSEL	O	Attenuation selection pin for digital filter : "L" = test, "H" = normal
(70)	XI	I	Crystal oscillator input Feedback resistor built in
(71)	XO	O	Crystal oscillator output
(72)	DO1	O	DAC serial data output
(73)	VSS1	O	GND 0V
(74)	DSCK	O	DAC data shift clock output
(75)	LRCK	O	DAC left and right clock output
(76)	DO2	O	DUAL DAC serial data output, Rch
(77)	WDCK	O	DAC word clock
(78)	DLRCK	O	DAC left and right clock output 2
(79)	APTL	O	DAC deglitcher clock L
(80)	APTR	O	DAC deglitcher clock R

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DD}-V_{SS}	Supply voltage	− 0.3 ~ + 7	V
V_I	Input voltage	V_{SS}−0.3 ≦ V_I ≦ V_{DD}+0.3	V
V_O	Output voltage	V_{SS} ≦ V_O ≦ V_{DD}	V
T_{opr}	Operating temperature	−10 ~ +70	℃
T_{stg}	Storage temperature	−40 ~ +125	℃
P_d	Power dissipation	350	mW

RECOMMENDED OPERATING CONDITIONS

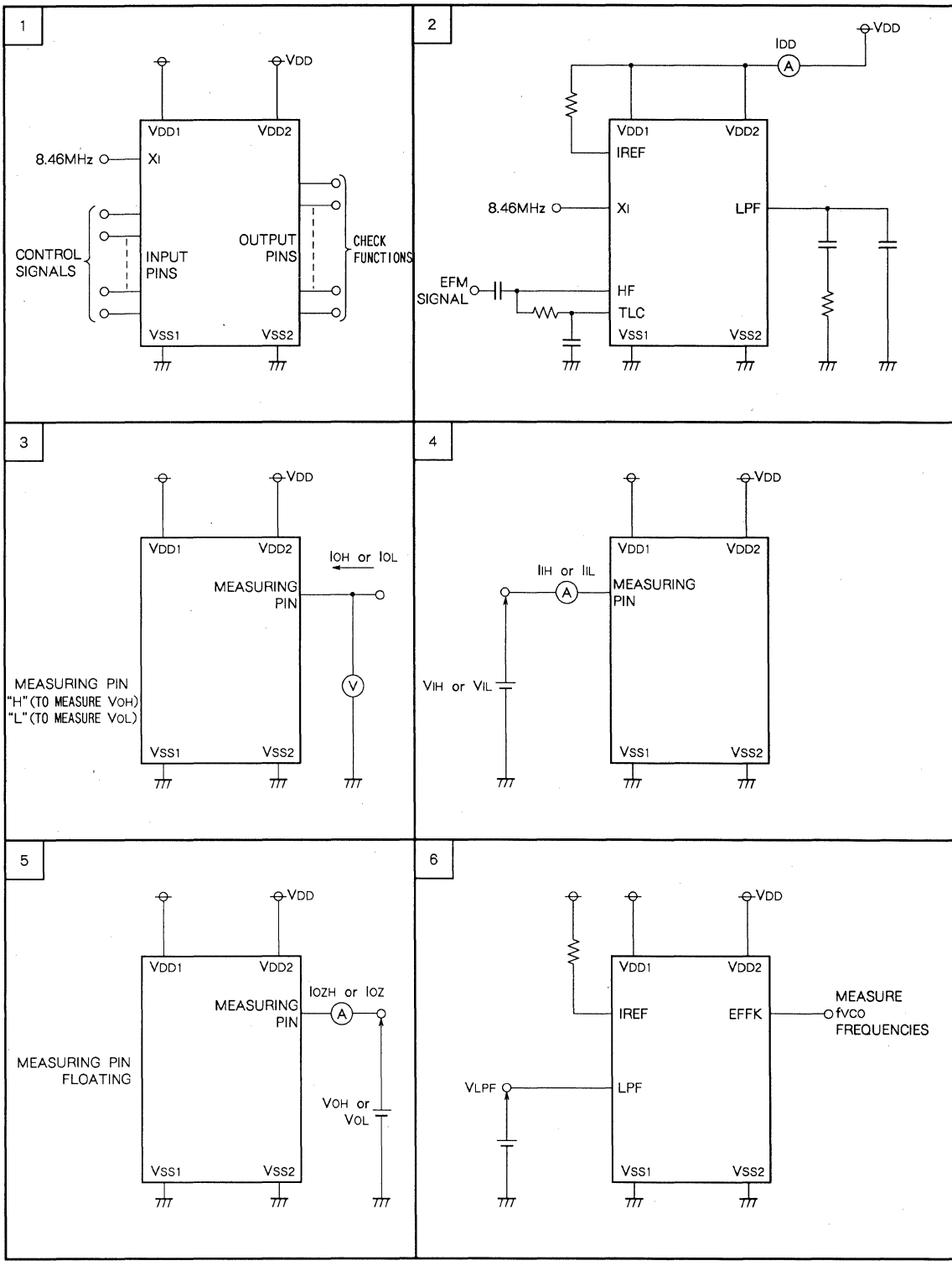
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Supply voltage		4.5	5.0	5.5	V
V_{IH2}	Input voltage 2 ("H" level)		3.5	−	V_{DD}	V
V_{IL2}	Input voltage 2 ("L" level)		V_{SS}	−	1.5	V
f_{OSC}	Oscillation frequency (X'tal)		−	8.46	−	MHz
f_{VCO}	Oscillation frequency (VCO)		−	8.64	−	MHz

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{DD} = 5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Applicable pin	Test circuit	Limits			Unit
					Min	Typ	Max	
V_{DD}	Operating supply voltage	Ta = − 10 ~ + 70℃		1	4.5	5.0	5.5	V
I_{DD}	Supply current	f_{OSC} = 8.4672MHz f_{VCO} = 8.6436MHz See test circuit for pin conditions		2	−	14	−	mA
V_{OH}	Output voltage ("H" level)	V_{DD}=4.5V, I_{OH} = −0.8mA	③	3	3.5	−	−	V
V_{OL}	Output voltage ("L" level)	V_{DD}=4.5V, I_{OL}=0.8mA	③	3	−	−	0.4	V
I_{IH}	Input current ("H" level)	V_{IH}=4.5V	④	4	−	−	2	μA
I_{IL}	Input current ("L" level)	V_{IL}=0.5V	④	4	−2	−	−	μA
I_{OZH}	Output current in off state("H" level)	V_{OH}=4.5V	⑤	5	−	−	2	μA
I_{OZL}	Output current in off state("L" level)	V_{OL}=0.5V	⑤	5	−2	−	−	μA
f_{VCO1}	Free-running frequency	V_{LPF}=1.0V		6	−	−	3.0	kHz
f_{VCO2}		V_{LPF}=2.5V		6	−	7.4	−	kHz
f_{VCO3}		V_{LPF}=4.0V		6	8.0	−	−	kHz

Applicable pins
③Output (O) and input/output (I/O) pins except for XO,TLC, and LPF.
④Input (I) pins except for XI and IRFF
⑤SBCP~SBCW

TEST CIRCUITS



FUNCTIONAL DESCRIPTION

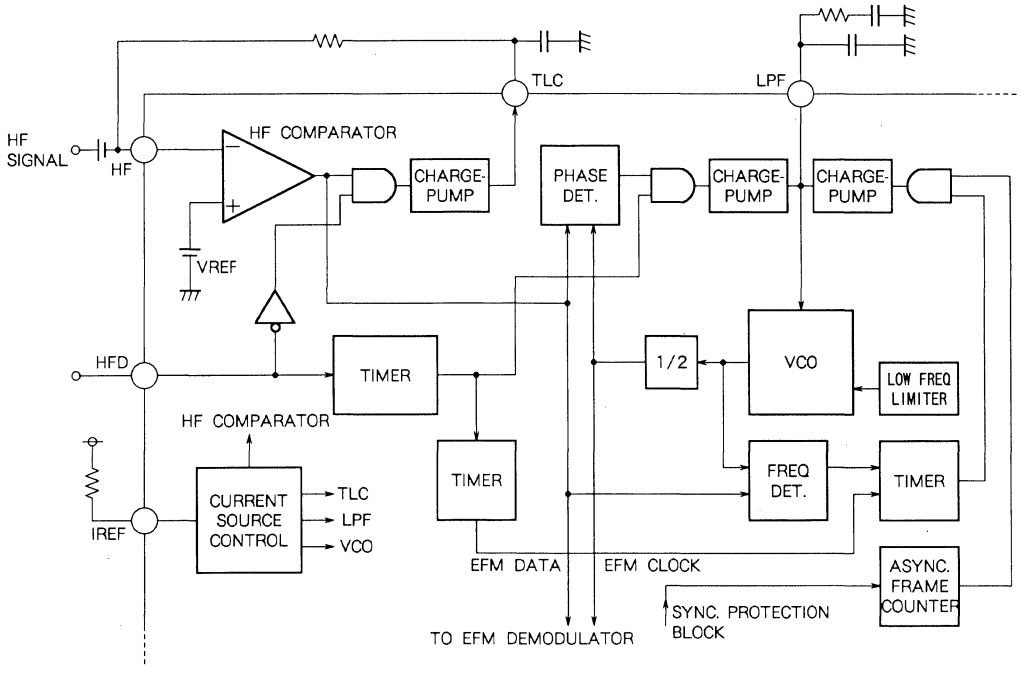
1. Data slicing/PLL

The M65820AFP has an analog front-end for incoming HF (EFM) signal. Using CMOS-Analog technology, the front-end comprises an automatic slice level control circuit and EFM-PLL circuit with internal adjust-free VCO. The block-diagram shows the analog front-end. The HF signal is sliced by the HF comparator and a DC level is feed back from TLC to HF through the external CR. If HFD goes High because of a defect an disc, then TLC time off and holds the DC level.

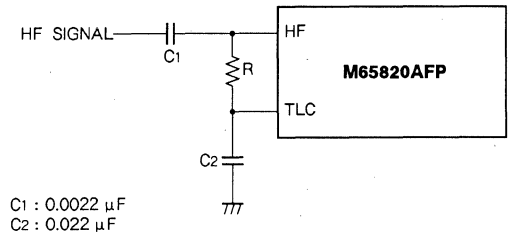
EFM-PLL extracts the EFM clock signal from the HF signal. The PLL circuit has a phase/frequency comparator providing the M65820AFP with a wide capture/lock range. There is no need to adjust the VCO. LPF is the charge-pump output and same-time control voltage input to the VCO. LPF froms off if HFD goes High.

IREF is the reference current input used to determine the current of charge pumps of TLC and LPF, operating point of HF comparator and VCO free running frequency. If IREF is connected to a noisy power supply through a resistor, VCO is modulated and the error-rate increases. Therefore, power supply noise at IREF must be held to a minimum.

BLOCK DIAGRAM (Data slicing/PLL)



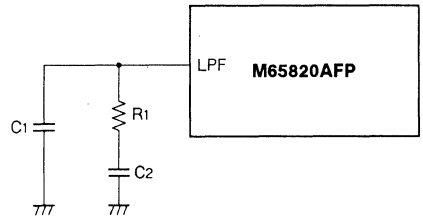
(1) Automatic slice level control



C1 : 0.0022 μF
C2 : 0.022 μF
R : 33k Ω
Vin : HF0.5VP-P Min

The slice level control circuit is formed by connecting a resistor and capacitors to the HF (High-Frequency signal input) and TLC (slice level control oputput) pins.

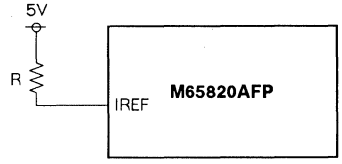
(2) PLL



C1 : 470pF
C2 : 0.15 μF
R1 : 2.2k Ω

Since the adjustment-free VCO is built in, the adjustment-free PLL circuit can be formed by connecting a resistor and capacitors to the LPF (low-pass filter) pin.

(3) Reference current



R : 100k Ω

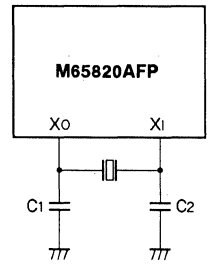
A resistor must be connected between the IREF pin and V_{DD} in order to set the reference current used in determining the current values of the TLC pin and LPF pin, the comparator operating current of the slice level control circuit, and the VCO free-run frequency.

2. Demodulation/Decoding

The EFM signal converted to logic level and the EFM clock extracted from the EFM signal are input to the demodulator and decoder block.

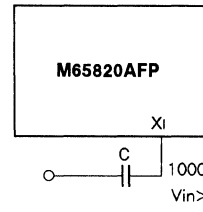
The EFM demodulator must be synchronized to the EFM clock. The decoder uses the clock from the X'tal oscillator. Jitter between the EFM signal and output of the decoder is absorbed by external RAM.

(1) Clock generator



CKSEL = H
X'tal : 8.4672MHz
C1 : 30pF
C2 : 30pF
or
CKSEL = L
X'tal : 16.9344MHz
C1 : 10pF
C2 : 10pF

(a) The oscillation circuit can be formed by connecting a X'tal oscillator(8.4672MHz or 16.9334MHz) and load capacitors to pins X_I and X_O.



(b) When the system contains a clock (8.4672MHz or 16.9334MHz), the clock can be input to pin X_I via a capacitor without using the X'tal oscillator. If the input signal is logic level, the capacitor is not necessary.

(2) Frame synchronization

EFM demodulating is done by Programmable Logic Array Conversion table. The demodulator must be synchronized to the EFM signal for each frame. The frame sync protection circuit holds the synchronization ever if the sync pattern is lost and prevents false synchronization of the demodulator when bit-slipping or mis-synchronization occurs.

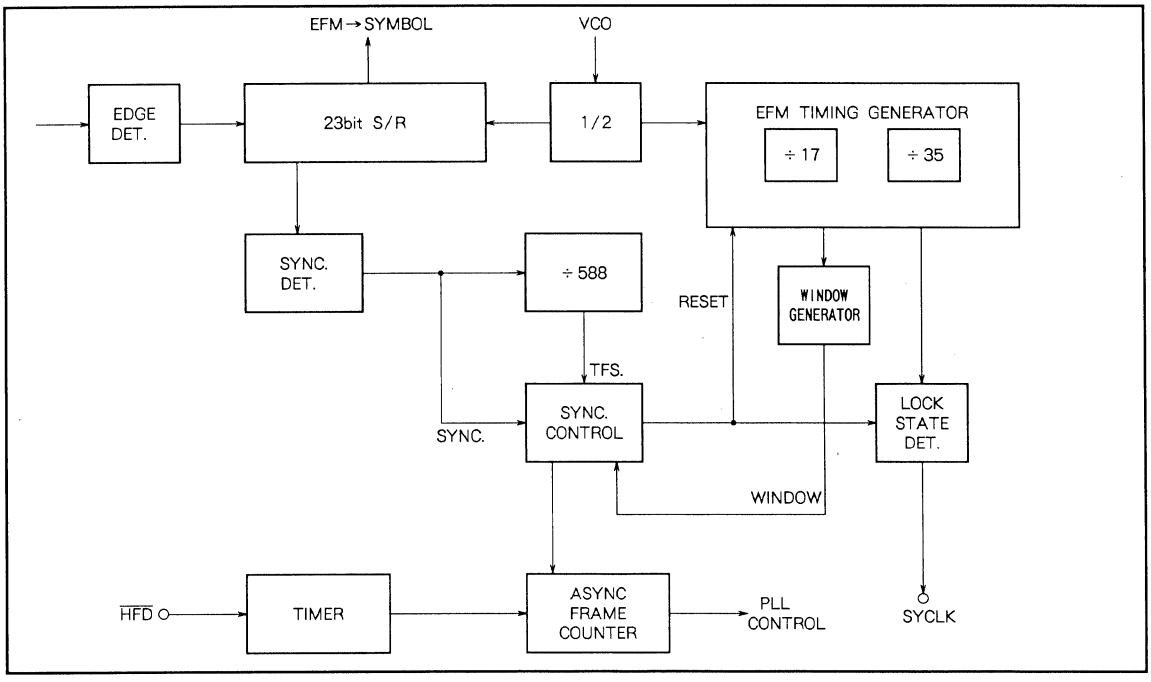


Fig. 1 Frame synchronization block diagram

The generating condition of the counter reset signal (Reset) in the EFM timing generator is indicated as follows:

Reset = (Sync * Tfs) + (Sync * Window)

* : Logical product

\+ : Logical sum

Sync : Synchronizing signal

Tfs : Detection signal of synchronizing signal space = 588

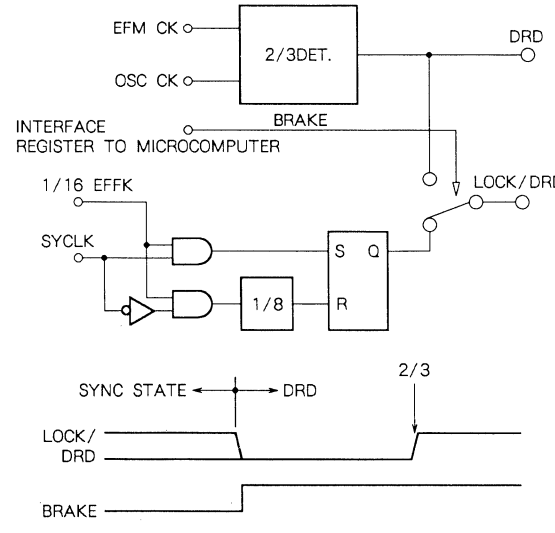
Window : Window signal ± 7ck

In the synchronous state, Sync and Tfs generate simultaneously and Sync comes to the center of the window. At this time, 1 is output to the SYCLK pin.

Frame sync status is output to the SYCLK pin. The SYCLK output includes some bounce when the sync pattern is lost because of a defect an disc. Hence, there is a need for debouncing the sync status signal to monitor by the system control microcomputer.

This debouncing is in the M65820AFP by monitoring the frame sync status at 1/16 EFM frame clock intervals and then outputting the result to the LOCK/DRD pin. If the monitored status is locked then output is High, Eight. Unlocked outputs becomes Low.

LOCK/DRD pin outputs DRD signal (see Sec. 3) when the disnotor is braking by command from microcomputer. The following pages contain the block diagram and the output timing.



(3) Subcode demodulation

Among data converted from 14-bits EFM signal to 8-bits symbols, subcodes P, Q, R, S, T, U, V and W are output to pins SBCP-SPCW repectively. When the subcode synchronizing patterns S_0 or S_1 is detected as synchronizing signals of subcode data, the synchonizing signals are output to the SCOR pin.

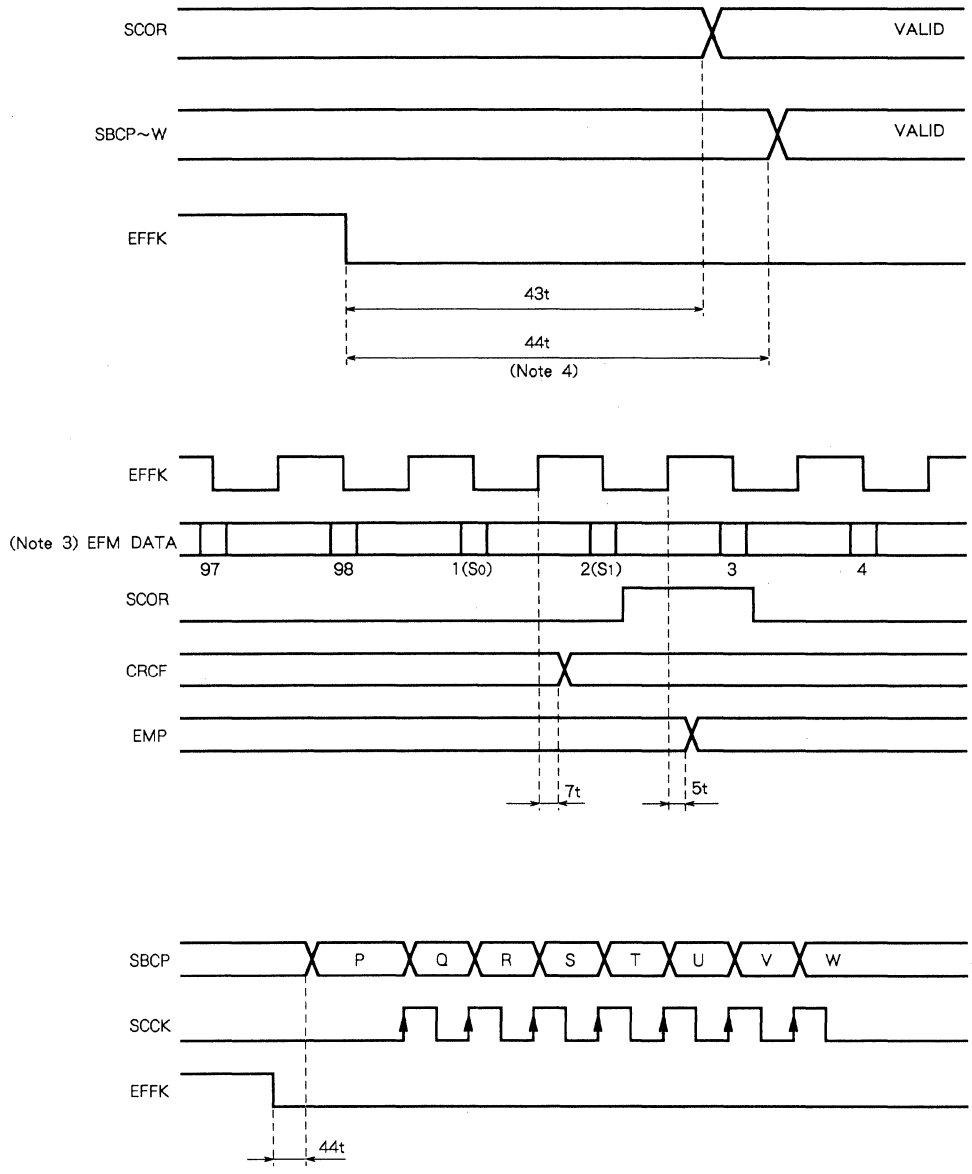
Pins SBCP-SBCW are a Three-State output system controlled by pins $SC0E_1$ and $SC0E_2$ as shown in the table below.

A CRC check is deve for the Q channel data, and if the data is correct, a 1 is output to the CRCF pin. The EMP pin displays whether or not emphasis is present. The subcode data is not only output in parallel, but also can be obtained serially via SBCP, by inputting a clock to SCCK.

Subcode output timing are shown Fig. 2.

SUBCODE DEMODULATION

$SC0E_1$	$SC0E_2$	SBCP	SBCQ	SBCR	SBCS	SBCT	SBCU	SBCV	SBCW
0	0	High-impedance				High-impedance			
1	0	P	Q	R	S	High-impedance			
0	1	High-impedance				T	U	V	W
1	1	P	Q	R	S	T	U	V	W



Note 3. Subcode block No. in the EFM data
4. t : Oscillating frequency (VCO)
(typically : 1/8.6436MHz = 115.7ns.)
5. When input frequency to SCCK is more than 8ck, SBCP becomes 0.

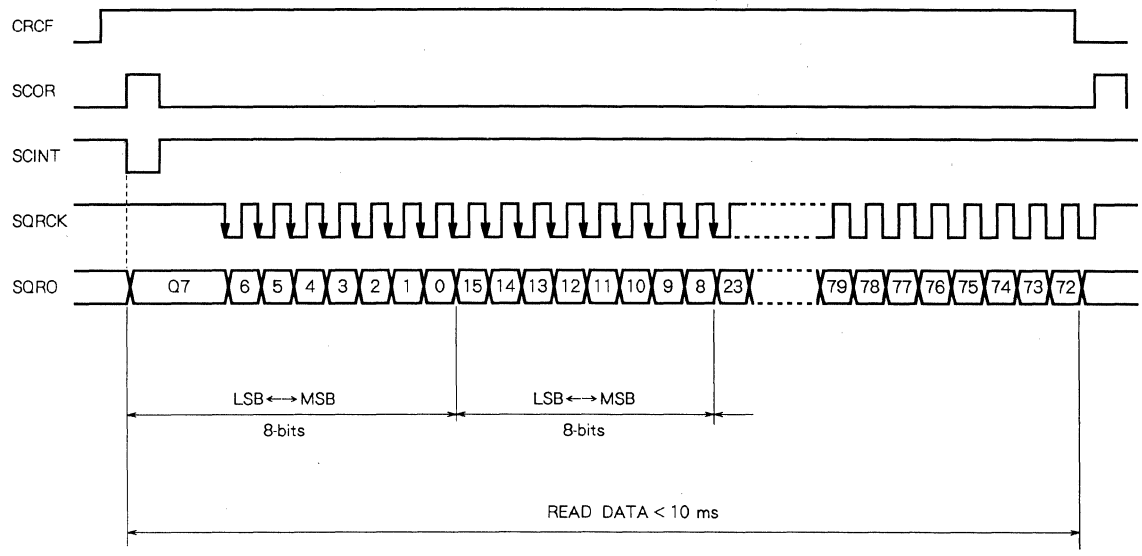
Fig. 2 Subcode output timing

(4) Subcode Q register

Subcode Q-channel data are output to SBCQ pin.

The M65820AFP stores the Q data in an 80-bit shift register. If CRC is OK, the system control microcomputer can access the Q data from the SBCQ pin by inputting the read-out clock to SQRCK pin. If the CRC check is OK, the M65820AFP outputs the interrupt signal to the microcomputer from SCINT, synchronized with SCOR (Subcode sync) signal.

Timing chart



(5) CIRC decoding

A 32K-bit Static RAM is needed as internal memory for temporary storage to process CIRC decoding (C1 decoding, C2 decoding, unscramble and de-interleave) and output interpolation. By using a 32K RAM, jitter is absorbed up to ±8 frames (max.).

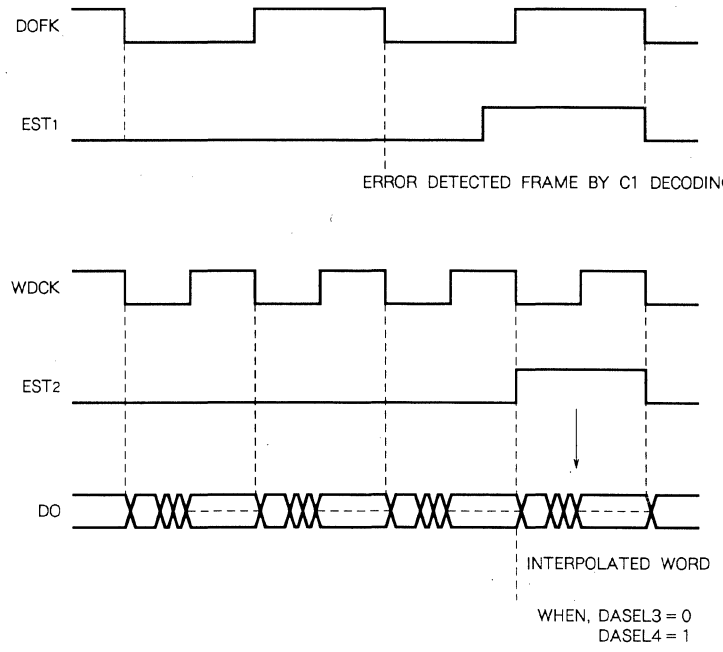
When CIRC decoding, double error correction is used for both C1 and C2 decoding.

When correction is not possible, average interpolation or pre-hold interpolation is perfomed. Error states detected during decoding are output to pins EST_1 and EST_2.

When an error is detected by C1 deoding, a 1 is output to pin EST_1. When an error word is judged imcorrectable by C2 decoding, a 1 is output to pin EST_2.

The putput timings for pins EST1 and EST2 are as follows :

Timing chart

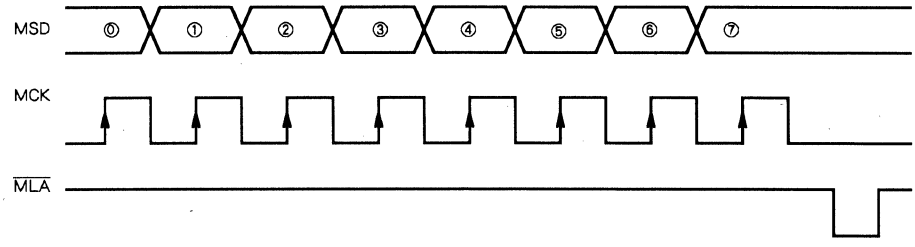


3. Microcomputer interface

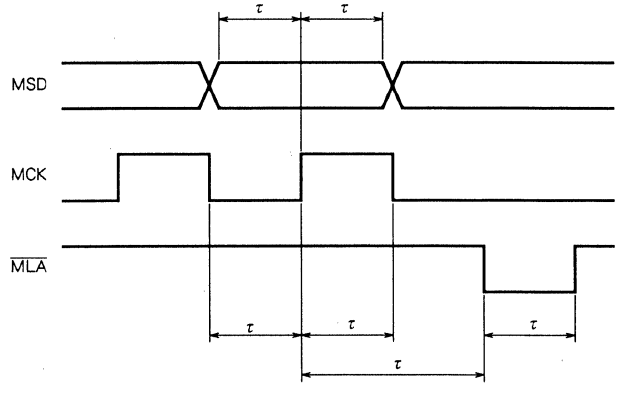
CLV servo, MUTE, and ATT system are controlled by serial commands from the microcomputer.

The timing, names, and functions of each control register are as follows :

Timing chart



⓪ DUMMY (Don't care).	X
① S/S (START/STOP) register.	start = 1
② BCON (BRAKECONTROL) register.	enable = 1
③ BRAK (BRAKE) register.	brake = 1
④ ATT (ATTENUATE) register.	−12dB = 1
⑤ $\overline{\text{MUTE}}$ register.	muting = 0
⑥ S/S timer reset register.	reset = 1
⑦ IC code.	M65820FP = 1



τ min : 500ns

Function of microcomputer interface registers

Register No.	Register name	Function	Operation		Note
			0	1	
⓪	DUMMY	Don't care	–	–	
①	S/S (START/STOP)	Controls START/STOP of the disk motor	DISC MOTOR STOP (OFF)	DISC MOTOR START (ON)	0 by $\overline{ALCR}$
②	BCON (BRAKECONTROL)	Determines if BRAKE control is necessary	BRAKE 0.3sec.	BRAKE is controlled by BRAKE register	0 by $\overline{ALCR}$
③	BRAK (BRAKE)	Controls BRAKE	BRAKE OFF (MOTOR OFF)	BRAKE ON	When BCON = 1
④	ATT (ATTENUATE)	Sets attenuation (−12dB)	0dB	−12dB	When MUTE = 1
⑤	MUTE	Sets the muting	−∞ dB	0dB	0 by $\overline{ALCR}$
⑥	S/S timer reset	Resets S/S timer which sets time of KICK and BRAKE to 0.3sec.	S/S timer enable	S/S timer disable	1 by $\overline{ALCR}$
⑦	IC code	Distinguishes command to the M65821FP	–	Executing command	0 is code for M51564P

Examples of system control are as follows :

Operation \ Register name	⓪ DUMMY	① S/S	② BCON	③ BRAK	④ ATT	⑤ $\overline{MUTE}$	⑥ S/S timer reset	⑦ IC code
								0
MUTE						0		1
ATT					1	1		1
0.3sec.KICK→CLV		1					0	1
0.3sec.BRAKE→MOTOR OFF		0	0				0	1
BRAKE		0	1	1			0	1
MOTOR OFF		0	1	0			0	1
0.3sec. timer disable							1	1
MOTOR off(without 0.3sec. BRAKE)		0	0				1	1
CLV (without 0.3sec. KICK)		1	0				1	1
The following is example of the most simplified system control sequence.								
STOP		0	0	0	0	0	1	1
0.3sec. KICK→CLV		1	0	0	0	0	0	1
PLAY		1	0	0	0	1	0	1
FF/FR		1	0	0	1	1	0	1
PLAY		1	0	0	0	1	0	1
0.3sec. BRAKE→STOP		0	0	0	0	0	0	1

* The blanks mean "Don't care"or that other commands can be use simultaneously.
* KICK period can be extended by repetition of start procedure.
* Software developed on the M50423FP can be utilized on the M65820AFP (fully compatible).
* Software developed on the M50422P/M50427FP can be utilized on the M65820AFP(upward compatible). However, when using this software, the following functions on the M65820AFP are not available: subcode Q-register, subcode Q-interrupt signal LOCK/DRD output.

When the M65820AFP detects that the number of rotations is less than 2/3 that of the normal play state, it outputs the disc rotation deterioration signal to the DRD pin. By using this signal in the following stop sequence, the disc can be correctly stopped.

Operation or microcomputer operation \ Register name	⓪ DUMMY	① S/S	② BCON	③ BRAK	④ ATT	⑤ $\overline{MUTE}$	⑥ S/S timer reset	⑦ IC code
PLAY		1	0	0	0	1	0	1
BRAKE		0	1	1	0	0	0	1
($\overline{HFD}$: H checking by microcomputer)								
(Measuring t_{DRD} (DRD : 0→1) after BRAKE start								
(Stop $\overline{HFD}$ checking and) additional BRAKE time $2 \times t_{DRD}$								
MOTOR OFF		0	1	0	0	0	0	1

The DRD signal is output to both the DRD pin and also the LOCK/DRD pin during the braking period.

To reset the microcomputer interface register to the initial state, execute $\overline{ACLR}$ (M65820AFP clear) immediately after turning the power on.

4. Digital filter

The M65820AFP converts the sampling frequency of audio data from 44.1kHz (fs) to 88.2kHz (2fs) or 176.4kHz (4fs) by an overflow limited, FIR linear-phase digital filter.

Digital filter selection is done using pins DASEL1~DASEL4. Table 1 shows the digital filter and DAC interface mode. Degital filter by pass mode with no interpolation of umcorrectable data is designed for non-audio applications such as CD-ROM or CD-1. The digital filter by pass mode with interpolation is used for external precision digital filter applications.

Fig. 3 (a) shows the characteristics of the 2fs digital filter.

Fig. 3 (b) shows the characteristics of the 4fs digital filter.

5. D-A converter Interface

The M65820AFP has many different DAC Interface formats. The desired format is selected using pins DASEL1~DASEL4.

Timing signals, data and clocks automatically change to correspond to the digital filter, fs (pass)/2fs/4fs, is selected.

If the 4fs digital filter mode is selected then the dual DAC mode and 18-bit data out mode are available.

Table 1 shows the interface modes.

Fig. 4 (a) ~Fig. 4 (e) show the timings if interface to DAC.

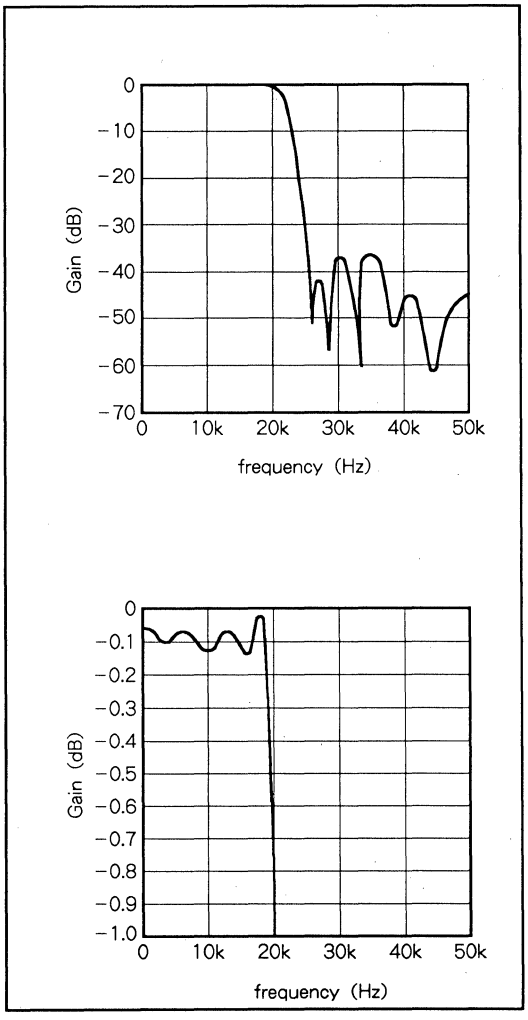


Fig. 3 (a) Frequency characteristics of the digital filter (Sampling frequency 88.2kHz:2fs)

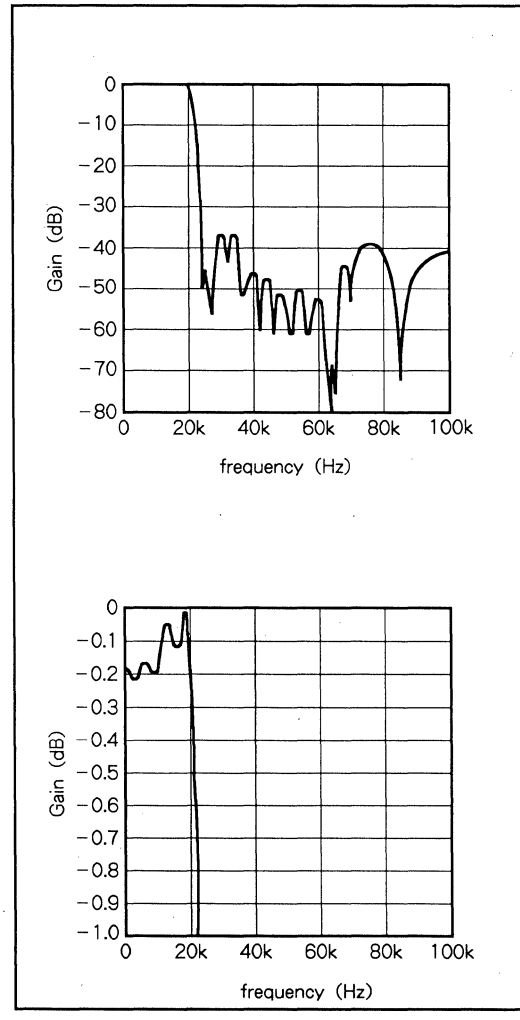


Fig. 3 (b) Frequency characteristics of the digital filter (Sampling frequency 176.4kHz:4fs)

Table 1 DAC interface modes

MODE	DASEL 1	DASEL 2	DASEL 3	DASEL 4	DF	MSB/LSB 1st	Note	Timing chart
1	0	0	0	0	2fs	MSB 1st		Fig. 4 (a)
2	0	0	0	1	(fs)	MSB 1st	Bypass filter	Fig. 4 (a)
3	1	0	0	0	2fs	LSB 1st		Fig. 4 (b)
4	1	0	0	1	(fs)	LSB 1st	Bypass filter	Fig. 4 (b)
5	1	0	1	0	4fs	MSB 1st		Fig. 4 (c)
6	1	0	1	1	4fs	MSB 1st	Dual DAC	Fig. 4 (d)
7	0	1	0	1	(fs)	MSB 1st	Interpolation	Fig. 4 (a)
8	1	1	0	0	2fs	MSB 1st		Fig. 4 (e)
9	1	1	0	1	(fs)	MSB 1st	Bypass filter	Fig. 4 (e)

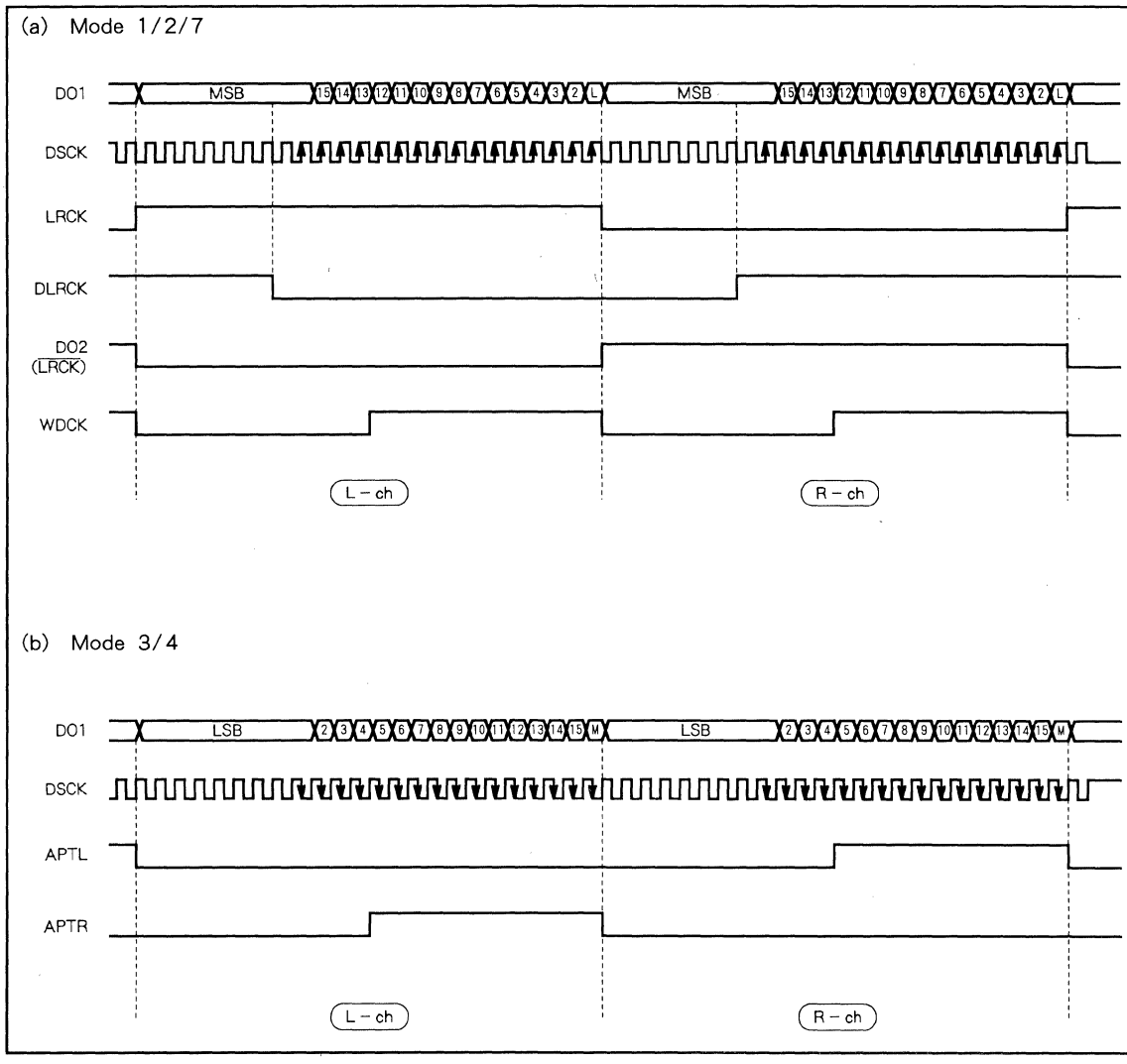


Fig. 4 DAC interface timing chart

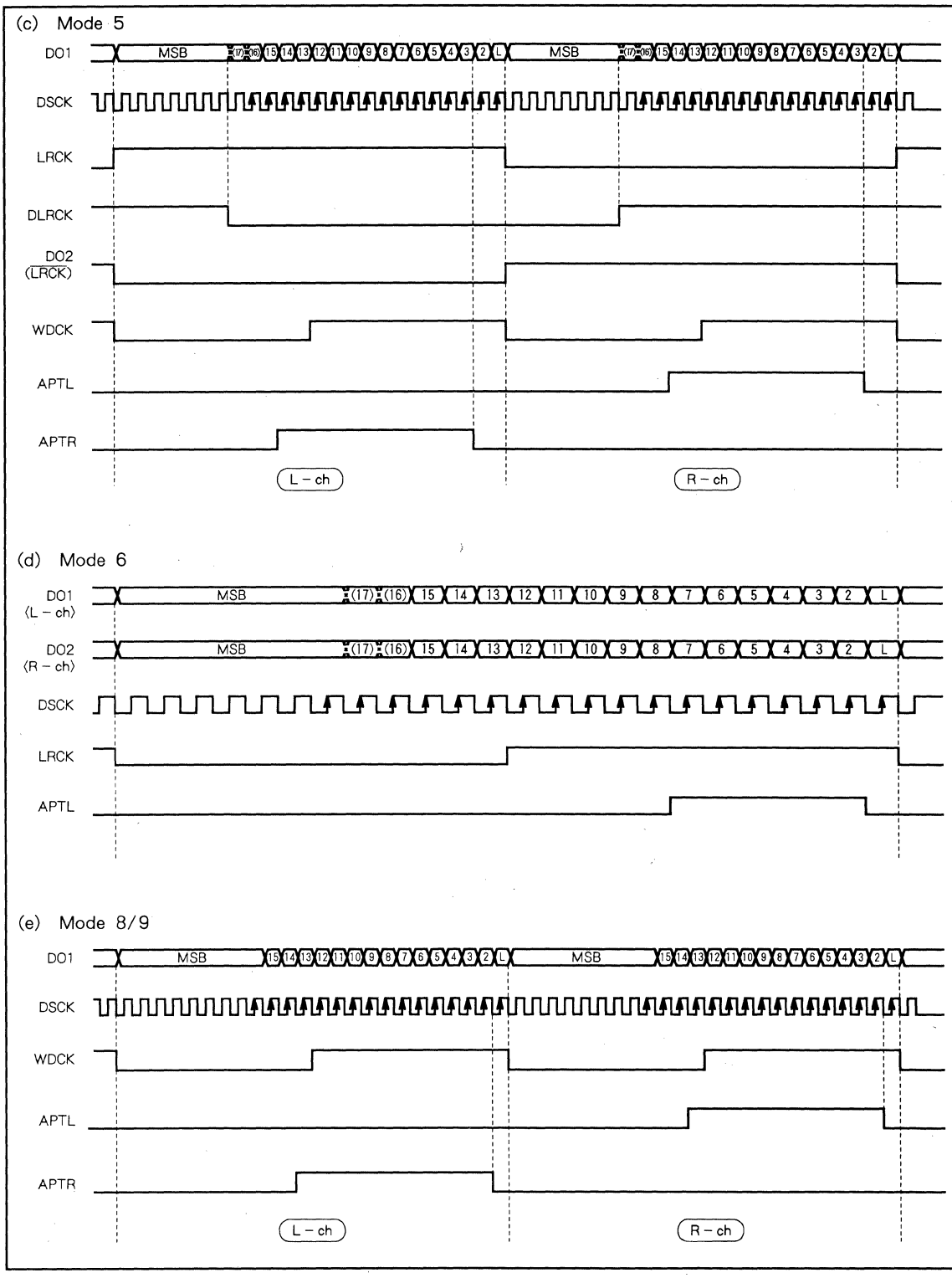
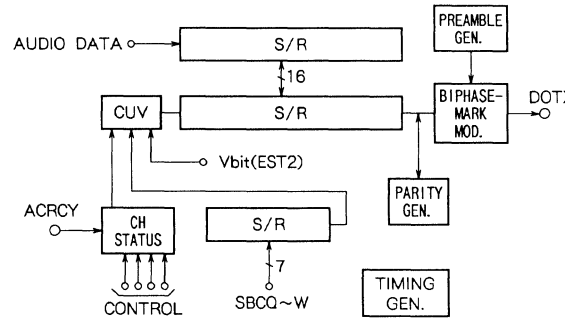


Fig. 4 DAC interface timing chart

6. Digital interface output

The M65820AFP outputs digital interface signal conforming to EIAJ CP-340 or IEC formats.

The block diagram shows the digtal interface and Fig. 5 shows the timings. Channel status clock accuracy can handle variable pitch control and can be set using the ACRCY pin. Clock accuracy is level II when ACRCY pin is Low, and level III when ACRCY pin is High.



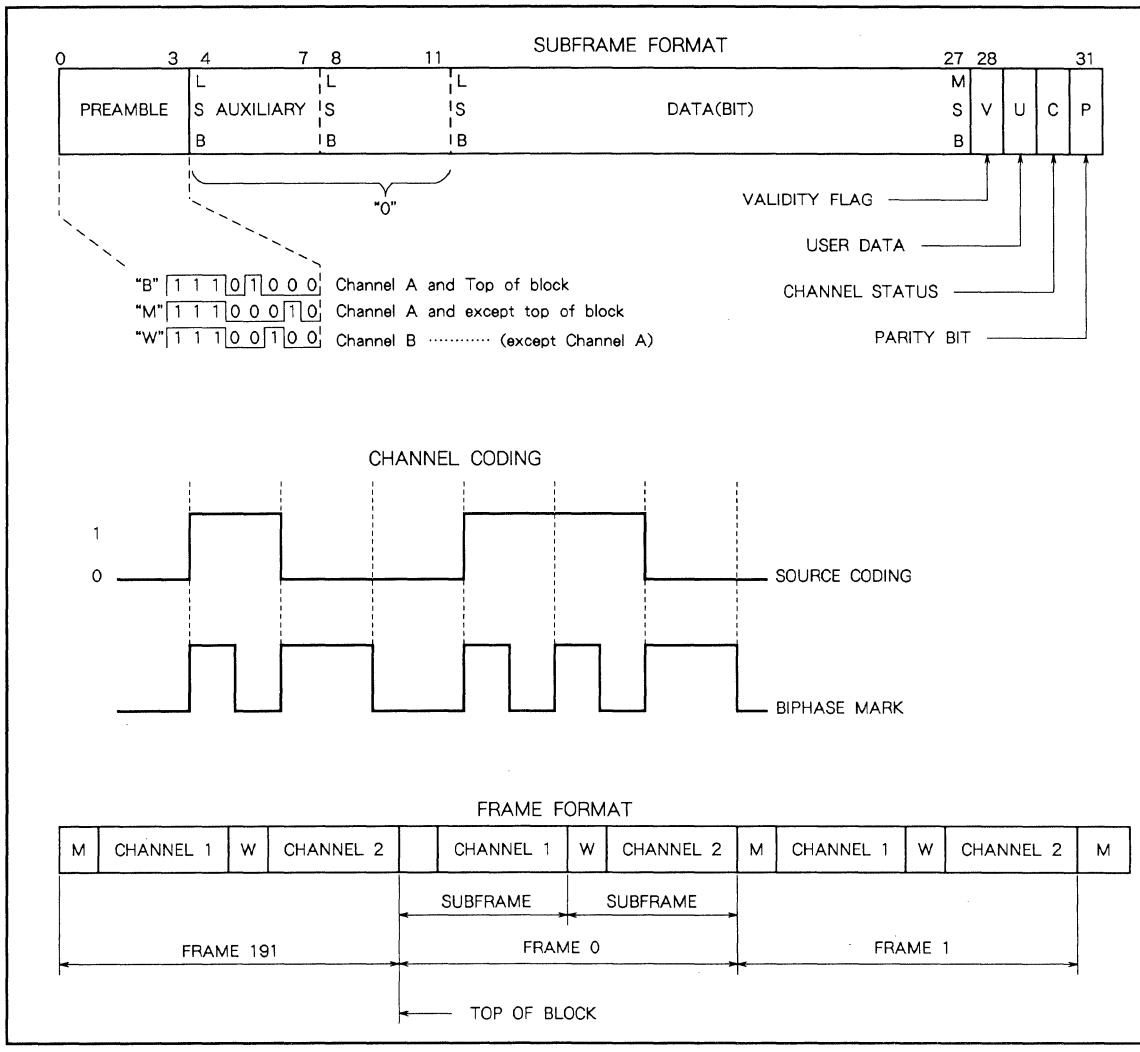


Fig. 5 Timing

7. CLV servo control circuit

CLV servo control circuit operates using two signals. The first is the frequency difference beween the EFM-clock and X'tal -clock. The second is the phase difference beween the write-frame address and read-frame address of the internal 32k RAM. Motor control signals are output to PWM_1 (− signal) and PWM_2 (+ signal). Because these singals are internally phase compensated, the CLV servo control circuit can be easily formed using current drivers on pins PWM_1 and PWM_2.

Fig. 7 shows the CLV, waveform and its duty cycle when the CIRC decoding block addressing write-frame address and the read-frame address exceeds ± 8frames.

When this occurs the duty cycle of the CLV waveforms will be reset to 0.

The disc motor can be driven by PWM waveforms directly or by an analog signal that can be generated by integratiing the PWM waveforms.

By using an analog signal, it is possible to adjust the servo loop-gain by varying direct external component values. But in the case of PWM waveforms, the servo loop-gain is determined by motor torque, and the rotating moment of the disc, turntable, and disc clamper.

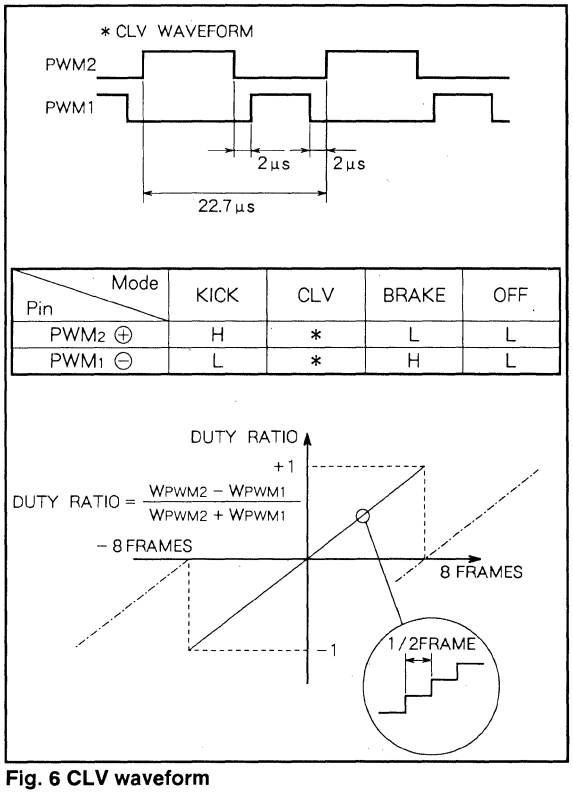


Fig. 6 CLV waveform

M65822AFP

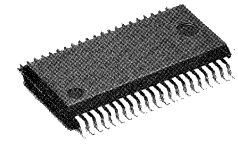
SINGLE CHIP CD PLAYER DIGITAL SIGNAL PROCESSOR

DESCRIPTION

The CMOS IC developed for compact disk playback
This IC is used in the digital signal processing unit for EFM demodulation and error correction or the like
This IC can also be used in CD-ROM and CD-G as well as CD-DA

FEATURES

- Adjustment free EFM-PLL (VCO built-in) with a wide lock range
- Jitter margin ±8 frame
- Easy-to-handle CLV servo command
- Sufficient mute control (zero-cross/fade mute)
- Lch/Rch monaural output
- Attenuation can be designated independently for L & R channels
- Error flag output in one byte
- High-performance 4-Fs digital filter
- 18-bit/20-bit outputs available
- Centralized control by microcomputer serial command
- Lower power dissipation during standby in the sleep mode
- Digital de-emphasis circuit built-in
- Digital silent detector circuit built-in
- Reduced base area by a smaller package

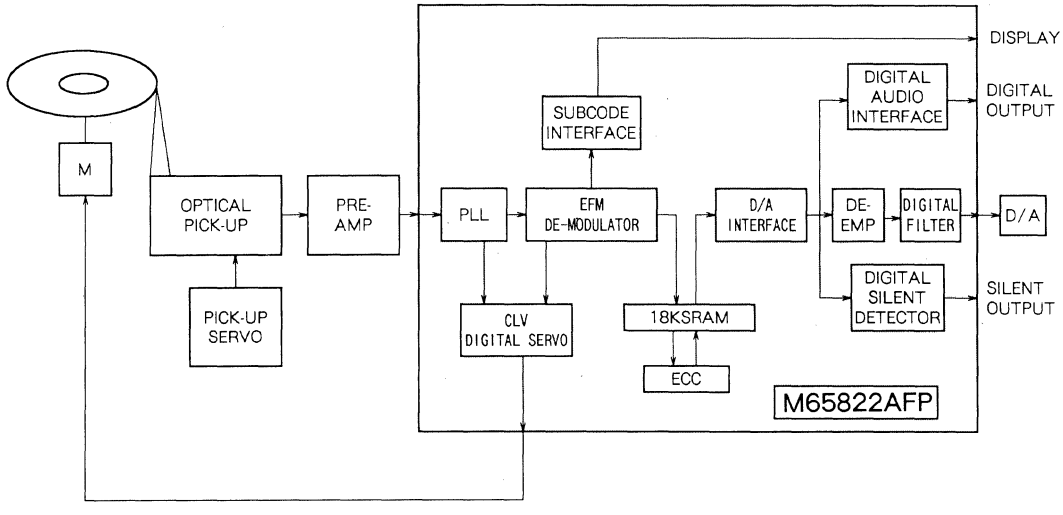


Outline 42P2R-A
0.8mm pitch 450mil SSOP
(8.4mm × 17.5mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{DD} = 4.5~5.5V
Rated supply voltage ..... V_{DD} = 5V
Rated power dissipation 125mW

SYSTEM BLOCK DIAGRAM



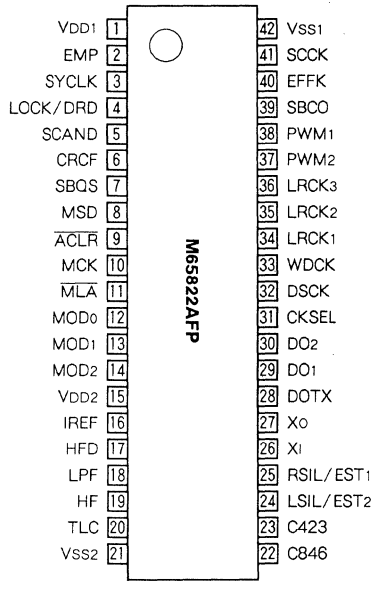
M65822AFP

SINGLE CHIP CD PLAYER DIGITAL SIGNAL PROCESSOR

BUILT-IN FUNCTIONS

- Adjustment free EFM-PLL
  - Slice level control
  - Bit clock generation
  - Adjustment free VCO
- Demodulation & Decoding
  - EFM demodulation
  - Frame sync detection, Protection & interpolation
  - Subcode demodulation (serial)
  - Subcode Q-CRC check
  - Subcode Q register
  - Emphasis detection
  - Jitter absorption ±8 frame
  - CIRC decoding
    - Unscrambling
    - De-interleaving
    - Error-correction capability C1 : Duplex ; C2 : Duplex
  - Interpolation processing (average value Interpolation & previous value hold)
  - Error monitor output
  - Interpolation inhibit
  - Zero cross mute
  - Fade mute
  - Digital attenuator
  - Dual DAC output
  - L/R monaural output
- Digital filter
  - 4 times oversampling phase linear digital filter
  - Digital filter-thru
  - 18-bit/20-bit output (only when a digital filter is used)
- CLV digital servo
  - Low disk rotation detection
  - PWM output
- Digital de-emphasis
  - Automatic detection of emphasis flag
  - Intermnal/external emphasis changeover
- Digital silence detector
  - Audio data silence detection
- Microcomputer interface
  - Mute, attenuation, disk motor ON/OFF, disk motor brake control
  - Digital-OUT ON/OFF, fade mute selection, digital filter thru selection, interpolation inhibit selection, clock precision input, 18-bit output selection, 20-bit output selection, dual DAC selection, stereo/monaural selection
  - Attenuation level control
  - Subcode Q register interface
  - Sleep mode control
- Digital audio interface
  - Digital-OUT ON/OFF
  - Clock precision input
- Master clock changeover
  - Master clock 8.4672MHz/16.9344MHz selectable

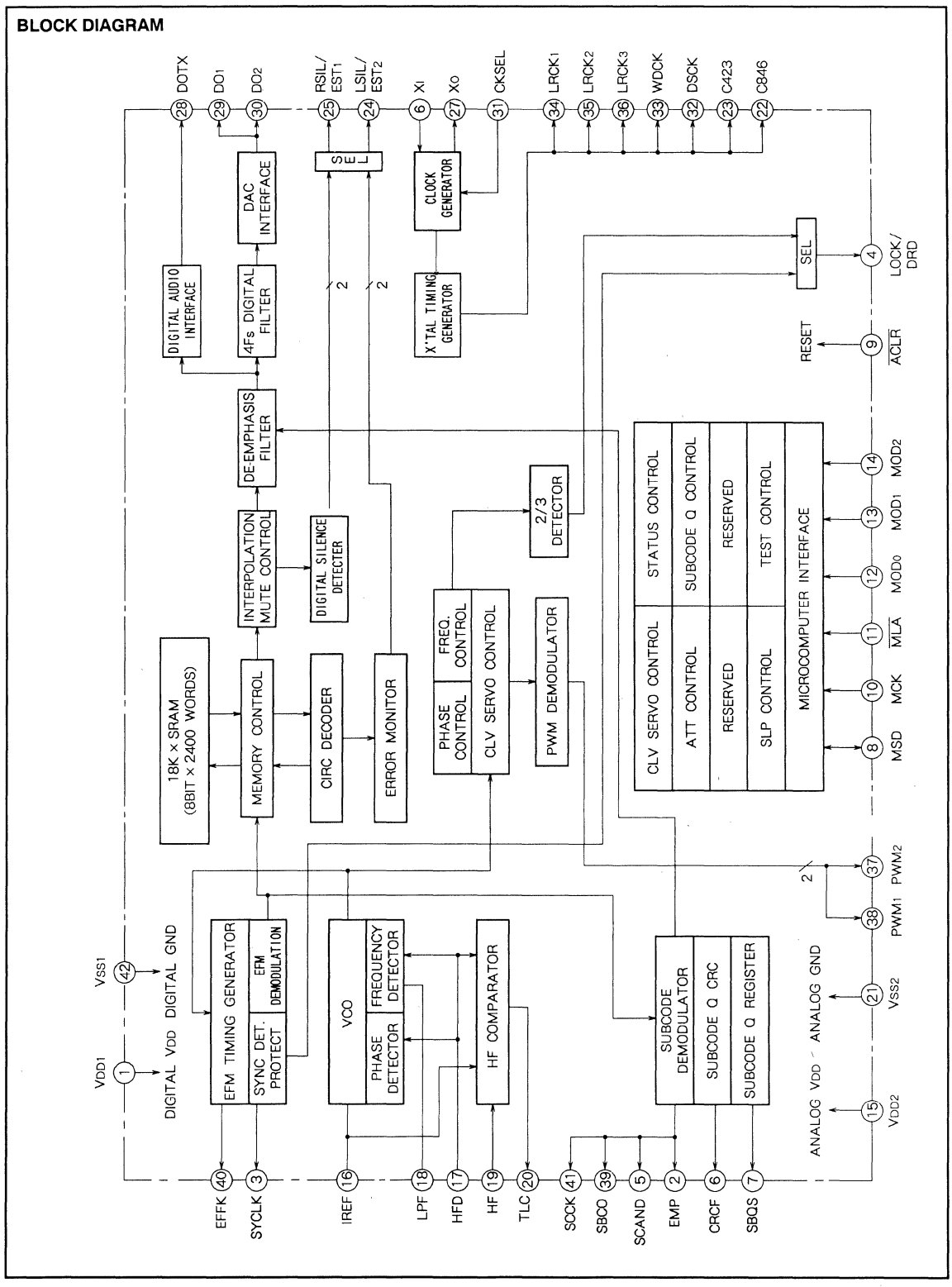
PIN CONFIGURATION



Outline 42P2R-A

MITSUBISHI ELECTRIC

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Name	I/O	Function
①	V_{DD1}	I	Digital system V_{DD}
②	EMP	O	Emphasis output. : "H" for emphasis
③	SYCLK	O	Frame lock status output. Lock = H
④	LOCK/ DRD	O	Sync status & low disk rotation staus output
⑤	SCAND	O	Subcode sync signal output : "H" for sync
⑥	CRCF	O	CRC checked results of subcode Q : CRC OK = H
⑦	SBQS	O	subcode Q register read interrupt signal : "L" for read-around
⑧	MSD	I/O	Microcomputer interface serial data I/O
⑨	$\overline{ALCR}$	I	System reset input : reset = L
⑩	MCK	I	Microcomputer interface shift clock
⑪	$\overline{MLA}$	I	Microcomputer interface latch clock
⑫	MOD_0	I	Microcomputer interface mode 0
⑬	MOD_1	I	Microcomputer interface mode 1
⑭	MOD_2	I	Microcomputer interface mode 2
⑮	V_{DD2}	I	PLL system V_{DD}
⑯	IREF	I	PLL circuit reference current setting
⑰	HFD	I	High frequency signal missing detect input
⑱	LPF	I/O	PLL loop filter
⑲	HF	I	High frequency signal input
⑳	TLC	O	Slice level control output
㉑	V_{SS2}	I	PLL system Vss
㉒	C846	O	Crystal system 8.4672MHz clock output
㉓	C423	O	Crystal system 4.2336MHz clock output

Pin No.	Name	I/O	Function
㉔	LSIL/ EST_2	O	Lch silence data output : error status output 2 : "H" at C_2 decoder error detection
㉕	RSIL/ EST_1	O	Rch silence data output : error status output 1 : "H" at C_1 decoder error detection
㉖	X_I	O	Crystal oscillator input : feedback resistor built in
㉗	X_O	I	Crystal oscillator output
㉘	DOTX	O	Digital-OUT output
㉙	DO_1	O	Audio serial data output for DAC : Lch output at dual DAC mode
㉚	DO_2	O	Rch output at dual DAC mode : LRCK1 inversion at single DAC mode
㉛	CKSEL	I	Master clock selection input (H : 8MHz, L : 16MHz)
㉜	DSCK	O	Data shift clock for DAC
㉝	WDCK	O	Word clock for DAC
㉞	$LRCK_1$	O	LR clock 1 for DAC
㉟	$LRCK_2$	O	LR clock 2 for DAC
㊱	$LRCK_3$	O	LR clock 3 for DAC
㊲	PWM_2	O	Disc motor drive PWM output 2 (acceleration side)
㊳	PWM_1	O	Disc motor drive PWM output 1 (deceleration side)
㊴	SBCO	O	Subcode serial output
㊵	EFFK	O	EFM frame clock output. duty ≒ 50 %
㊶	SCCK	I	Shift clock input for serial subcode data output
㊷	VSS_1	I	Digital system Vss

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Rating	Unit
V_{DD}-V_{SS}	Supply voltage	−0.3～+7	V
V_I	Input voltage	V_{SS}−0.3≦V_I≦V_{DD}+0.3	V
V_O	Output voltage	V_{SS} ≦ V_O ≦ V_{DD}	V
P_d	Power dissipation	350	mW
T_{opr}	Operating temperature	−10～+70	℃
T_{stg}	Storage temperature	−40～+125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	Input voltage ("H" level)		3.5	−	V_{DD}	V
V_{IL}	Input voltage ("L" level)		V_{SS}	−	1.5	V
f_{OSC}	Oscillation frequency (X'tal)		−	8.4672	−	MHz
f_{VCO}	Oscillation frequency (VCO)		−	8.6436	−	MHz

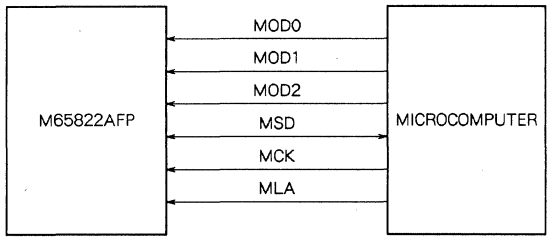
ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{DD} = 5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Supply voltage	Ta = −10～+70℃	4.5	5.0	5.5	V
I_{DD}	Circuit current	f_{OSC} = 8.4672MHz f_{VCO} = 8.6436MHz	−	−	−	mA
V_{OH}	Output voltage ("H" level)	V_{DD}=4.5V, I_{OH}=−0.8mA	3.5	−	−	V
V_{OL}	Output voltage ("L" level)	V_{DD}=4.5V, I_{OL}=0.8mA	−	−	0.4	V
I_{IH}	Input current ("H" level)	V_{IH}=4.5V	−	−	2	μA
I_{IL}	Input current ("L" level)	V_{IL}=0.5V	−	−	−2	μA
I_{OZH}	Output current in OFF-state ("H" level)	V_{OH}=4.5V	−	−	2	μA
I_{OZL}	Output current in OFF-state ("L" level)	V_{OL}=0.5V	−	−	−2	μA
f_{VCO1}	VCO(EFFK) free-running frequency	V_{LPF}=1.0V	−	−	3.0	kHz
f_{VCO2}		V_{LPF}=2.5V	7.8	9.5	−	kHz
f_{VCO3}		V_{LPF}=4.0V	9.5	−	−	kHz

FUNCTION DESCRIPTION

1. MICROCOMPUTER INTERFACE

(1) Connection



Pin No.	Signal name	Contents	I/O
⑫~⑭	MOD0~MOD2	Mode selector pin	I
⑧	MSD	Microcomputer serial data I/O pin	I/O
⑩	MCK	Microcomputer serial clock input pin	I
⑪	MLA	Microcomputer data latch signal input pin	I

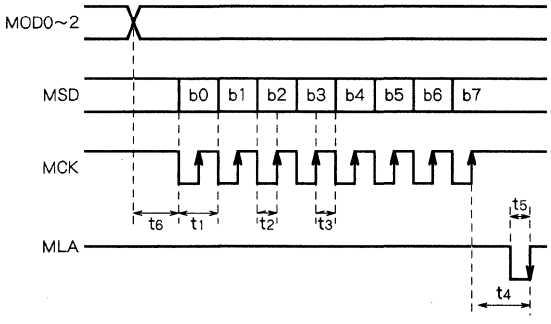
(2) Explanation of modes

Mode	Mode selector pin			Data contents	I/O	Number of bytes
	MOD2	MOD1	MOD0			
0	L	L	L	CLV servo control	I	1
1	L	L	H	Status control	I	2
2	L	H	L	Attenuate register control	I	2
3	L	H	H	Subcode Q register control	O	10
4	H	L	L	RESERVED	–	–
5	H	L	H	RESERVED	–	–
6	H	H	L	Sleep mode	I	0
7	H	H	H	Test mode (for delivery sorting)	I	0

Note : I/O is as viewed from M65822AFP

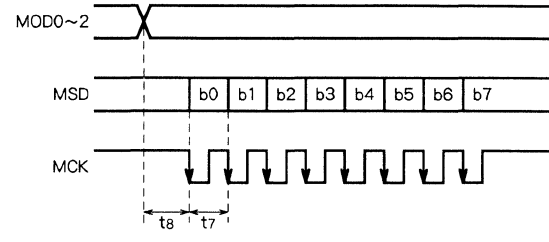
(3) Microcomputer I/O timing

Input timing (M65822AFP⇦Microcomputer)



Symbol	Description	Min	Unit
t_1	Shift clock width	200	nsec
t_2	Shift clock setup time	100	nsec
t_3	Shift clock hold time	100	nsec
t_4	Latch clock setup time	200	nsec
t_5	Latch clock width	200	nsec
t_6	Mode setup time	250	nsec

Output timing (M65822AFP⇨Microcomputer)



Symbol	Description	Min	Unit
t_7	Shift clock width	200	nsec
t_8	Mode setup time	250	nsec

(4) Mode 0:CLV servo control

〔Mode 0 : MOD2~0 = (0, 0, 0)〕

CLV servo, mute, attenuate and fade mute are contrlolled by cotrolling the register in mode 0.

Register name	Function		Register contents							
			b0	b1	b2	b3	b4	b5	b6	b7
DUMMY	Don't care		X							
S/S	Disc motor start/ stop control	Stop		0						
		Start		1						
BCON	Control for disc motor braking	Braking			0					
		No braking			1					
BRAK	Disc motor brake control	Brake OFF				0				
		Brake ON				1				
ATT	−12dB attenuation control	ATT OFF					0			
		ATT ON					1			
MUTE	Mute control	MUTE ON						0		
		MUTE OFF						1		
S/S timer reset	S/S timer (0.3s) reset control	Timer operation							0	
		Timer reset							1	
IC code	Identification signal	Servo								0
		DSP								1
Initial state	Register contents in reset conditions		0	0	0	1	0	0	1	0

(5) Mode 1:Status control

〔Mode 1 : MOD2, 1, 0 = (0, 0, 1)〕

By setting a register in mode 1, it is possible to determine the status required in operating the signal processing unit.

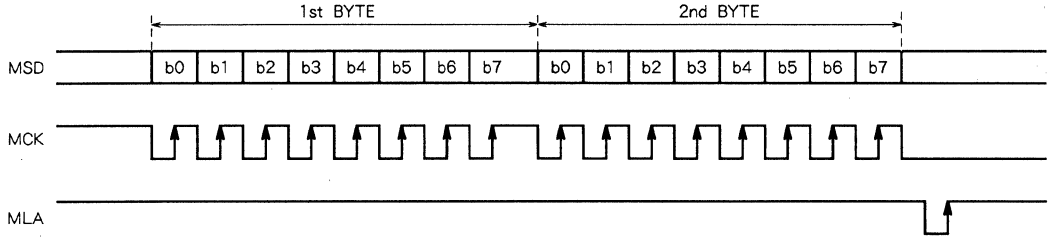
The status register consists of two bytes, and setting is possible by starting up MLA after inputting 2-byte data to DSP.

Register name	Function		Register contents							
			b0	b1	b2	b3	b4	b5	b6	b7
DOUT	Control for use digital-OUT	Used	0							
		Not used	1							
NON-AUDIO	Control for audio or non-audio data	Audio		0						
		Non audio		1						
DFPASS	Controls for digital filter	Used			0					
		Pass			1					
18-BIT	Control for 18-bit output	16-bit output				0				
		18-bit output				1				
20-BIT	Control for 20-bit output	16-bit output data					0			
		20-bit output					1			
DUAL-DAC	Control for single or dual DAC mode	SINGLE						0		
		DUAL						1		
LMONO	Lch monaural output	Stereo							0	
		L-ch monaural							1	
RMONO	Rch monaural output	Stereo								0
		R-ch monaural								1
Initial state	Register contents in reset conditions		0	0	0	0	0	0	0	0

Register name	Function		Register contents							
			b0	b1	b2	b3	b4	b5	b6	b7
FMUTE	Controlling fade mute ON/OFF (See Note)	Fade-out	0							
		Fade-in	1							
FMTC	Controlling the fade mute time	2.2sec		0						
		34.8ms		1						
FMCNT	Fade mute used/not used	Not used			0					
		Used			1					
ZMCM	Controlling zerocross mute or no zerocross mute	Zerocross present				0				
		No Zerocross				1				
ACCK	Oscillation precision input	Level II					0			
		Level III					1			
DDEC	Controlling the presence or absence of digiral de-emphasis	Internal emphasis						0		
		External emphasis						1		
SIL/EST	Controlling silence output and error monitor output	Silence output							0	
		Error monitor output							1	
SILC	Controlling silence output	Stereo								0
		Monaural								1
Initial state	Registers contents in reset conditions		0	0	0	0	0	0	0	0

Note 1. The FMUTE register changing point is detected for operation
- Fade in when "0"changes to "1"
- Fade out when "1"changes to "0"

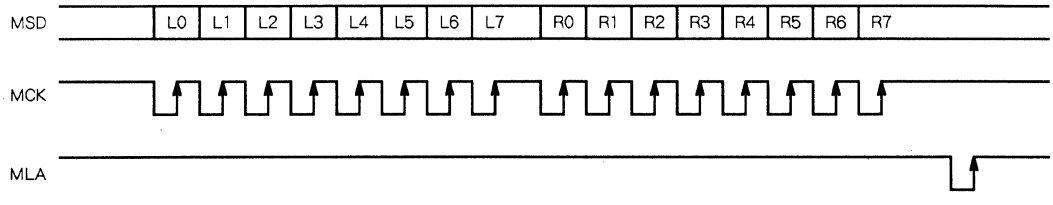
2. When the FMCNT register is "1", the attenuate register becomes effective.
3. The status data input sequence is as follows



(6) Attenuate register control

[Mode 2 : MOD2, 1, 0 = (0, 1, 0)]

The attenuation level can be set independently for L and R channels by using the attenuate register.
This register is set, using 8-bit for L and R channels : this setting is carried out by inputting a clock to the MSD pin with LSB first. from L-channel side.
MSD, MCK, and MLA at this time are shown below :



The relation between the attenuation data and attenuation level is shown in para. 10.(4).

(7) Subcode Q register interface

〔Mode 3 : MOD2, 1, 0 = (0, 1, 1)〕

The data of subcode Q stored in the internal 80-bit register can be read with a serial clock from the microcomputer. When MOD2, 1, 0 = (0, 1, 1), MSD is placed in output conditions, and the register is set by inputting 80 clocks to the MCK pin from SBQS pin rise to the next SBQS fall. The data from the MSD pin is output with MSB & LSB inverted in 8-bit.

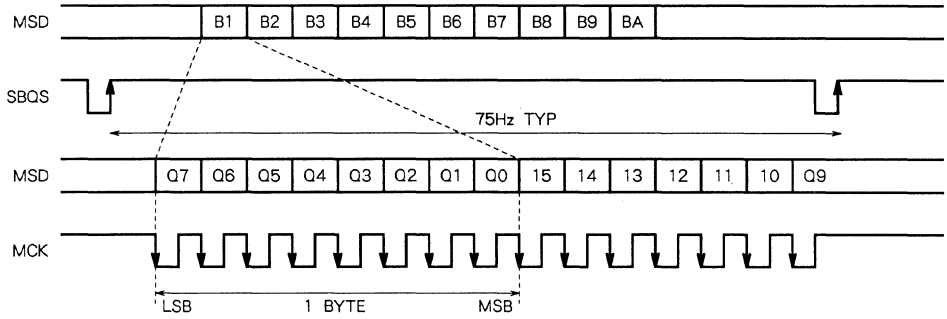
The SBQS pin outputs "L" when the following conditions are satisfied and the internal register is placed in readable conditions.

< Conditions under which the SBQS pin is placed in "L" >

(a) When the CRC checked results is OK

(b) When both subcode sync signals S_0, S_1 are detected in the specified position. (S_0 and S_1)

When both conditions (a), (b) above are satisfied. the SBQS pin outputs "L".

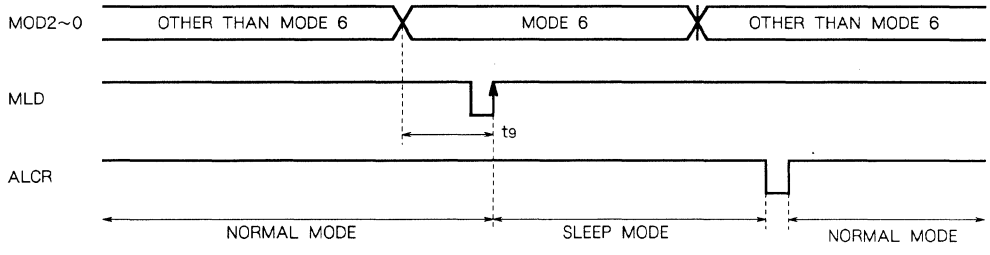


The emphasis information of subcode Q data is output to the EMP pin.

Condition	EMP pin
When no emphasis is present	L
When emphasis is present	H

(8) Sleep mode 〔Mode 6 : MOD2, 1, 0 = (1, 1, 0)〕

The sleep mode is used when LSI is not used : the master clock stops, and the low power dissipation mode is selected. The sleep mode is selected by inputting "L" to the MLA pin when MOD2, 1, 0 = (1, 1, 0). To release to the sleep mode, set the ALCR pin to "L" once and set it to "H" again.



Symbol	Description	Min	Unit
t_g	Set-up time of mode 6 latch signal	250	nsec

(9) Test mode 〔Mode 7 : MOD2, 1, 0 = (1, 1, 1)〕

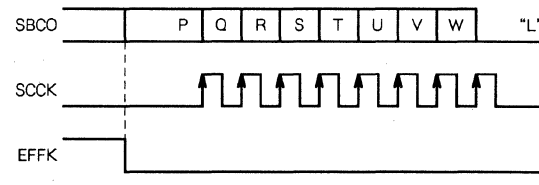
This mode is used when LSIs are tested before shipment : it is a use inhibit mode.

Mode 7 is set by latching with the MLA signal in the same matter as in mode 6 ; even when MOD2~0 is (1, 1, 1) momemtarily when the mode is switched, it is not latched to the inside.

2. SUBCODE INTERFACE

The subcode data (P, Q, R, S, T, U, V, W), can be read from the SBCO pin by inputting a clock to the SCCK pin among the data coverted from 14-bit EFM signal to 8-bit symbol. When both subcod sync patterns S_0, S_1 are detected in the specified position as a sync signal of this subcode, a sync signal is output from the SCAND pin.

If 8 clock or more are input to the SCCK, the SBCO is placed in "L".



3. EFM-PLL CIRCUIT

(1) Data slicing/PLL

The M65822AFP has an analog front-end for incoming HF (EFM) signal. Using CMOS-Analog technology, the front-end comprises an automatic slice level control circuit and EFM-PLL circuit with internal adjust-free VCO. The block-diagram shows the analog front-end. The HF signal is sliced by the HF comparator and a DC level is feed back from TLC to HF through the external CR. If HFD goes High because of a defect an disc, then TLC time off and holds the DC level.

EFM-PLL extracts the EFM clock signal from the HF signal. The PLL circuit has a phase/frequency comparator providing the M65822AFP with a wide capture/lock range. There is no need to adjust the VCO. LPF is the charge-pump output and same-time control voltage input to the VCO. LPF froms off if HFD goes High.

IREF is the reference current input used to determine the current of charge pumps of TLC and LPF, operating point of HF comparator and VCO free running frequency. If IREF is connected to a noisy power supply through a resistor, VCO is modulated and the error-rate increases. Therefore, power supply noise at IREF must be held to a minimum.

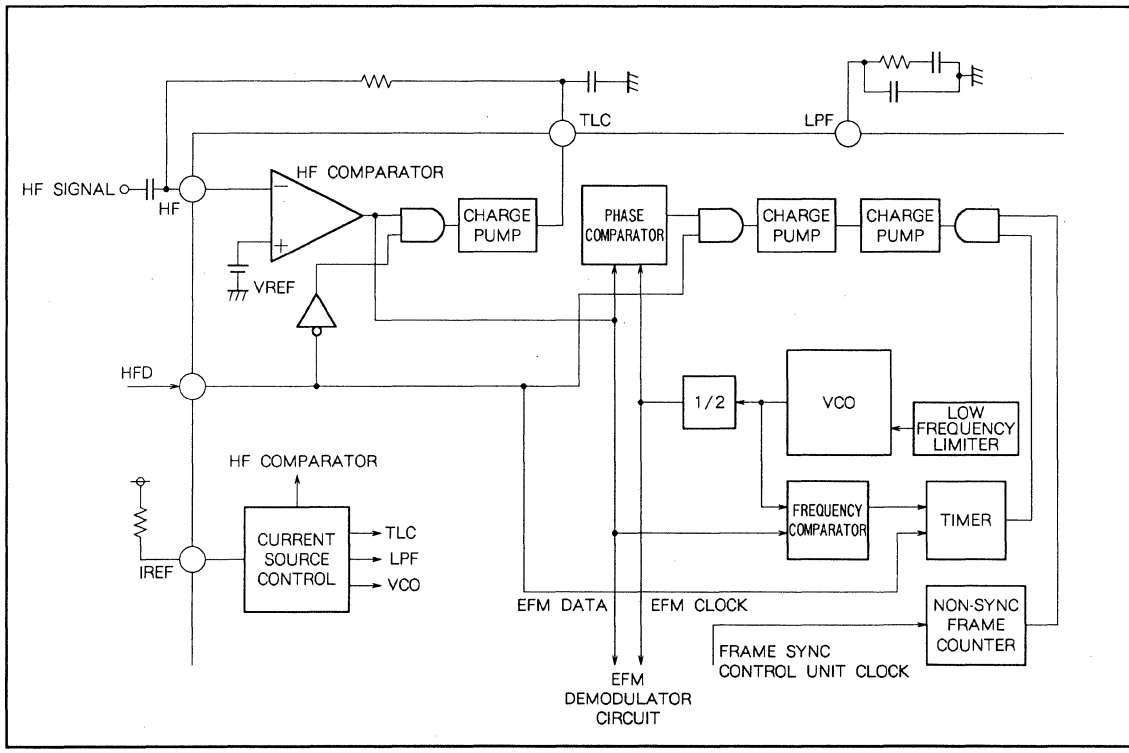
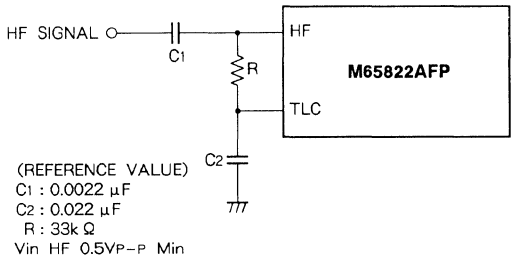


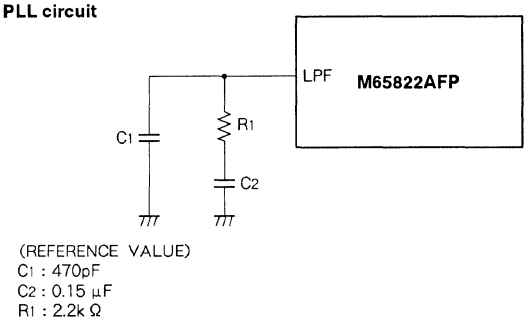
Fig. 1 Block diagram of the analog front end

(2) Slice level control



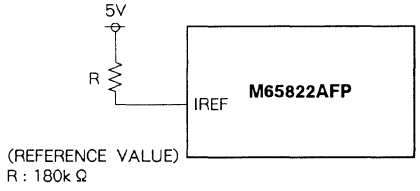
A slice level control circuit can be configured by connecting a resistor and capacitor to HF (playback signal input) pin and TLC (slice level control output) pin.

(3) PLL circuit



VCO built in this PLL circuit, which can be configured just by connecting a resistor and capacitor to LPF (low-pass filter) pin.

(4) Reference current setting



To set the current value of TLC pin and LPF pin, comparator operating current of slice level control circuit and reference current for determining VCO free-running frequency, connect a resistor of (recommended value) 180k-Ω between IREF pin and V_{DD}.

4. EFM DEMODULATOR

EFM signal converted to the logic level and clock reproduced from EFM signal are input to the demodulator block, which is then converted to an 8-bit symbol data.

This EFM signal demodulation is based on the EFM conversion table specified in the RED book.

To demodulate EFM signal, the demodulator circuit should be synchronized in frames for EFM signal.

The sync circuit has a system of protecting sync even when a sync pulse is missing and preventing sync errors in bit slip or re-pull-in from pull-out, thus maintaining stable sync even for disc defects (flaws & stains).

The block diagram for this frame sync control is shown in Fig. 2 below.

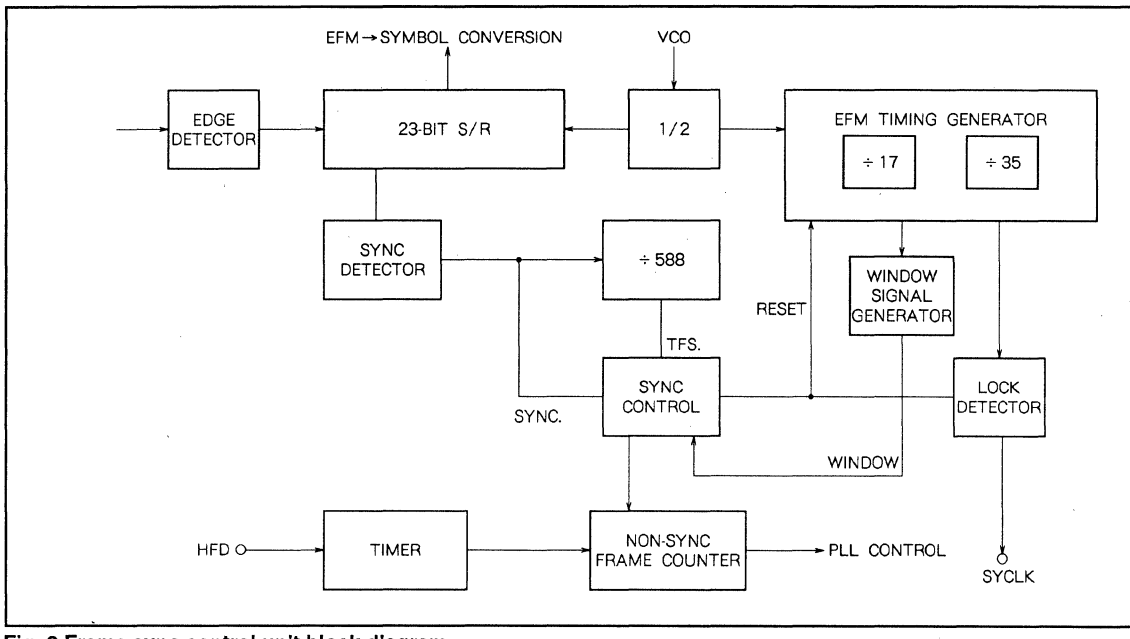


Fig. 2 Frame sync control unit block diagram

In the block diagram above, the conditions of generating counter reset signal, "Reset" in the EFM timing generation unit can be expressed in the following equation.

Reset = Sync * Tfs + Sync * Window

(where : * = Logical product AND + = Logical sum OR)

In this equation, Sync, Tfs and Window mean a sync signal, a detection signal of sync signal spacing (= 588), and ± 7C window signal respectively.

In the synchronizing conditions, Sync and Tfs generate at the same time, and Sync enters the window center. In this state, it follows that "H" is output to SYNCLK pin and EFM signal is synchronizing in frames.

Contents	SYCLK
EFM signal is not in synchronizing in frames	L
EFM signal is synchronizing in frames	H

To monitor a synchronous condition with a control microcomputer, it is necessary to provide a signel from which a short-period missing of sync pattern due to a disc defect, which occurs even in a synchronizing state is eliminated.

In M65822AFP, this signal is allocated to LOCK/DRD pins. When the braking instruction from the microcomputer is not input, the LOCK/DRD pins monitor the synchronizing state in 1/16period of EFM frame clock, outputting the results. If the monitored results are sync, "H" is output, and if they are not sync continuosly 8 times, "L" is output.(When the braking instruction is input from the microcomputer, the LOCK/DRD terminals output a low disc rotation status monitor signal (DRD signal). The details are described later in the CLV servo control paragraph.)

Conditions	Contents	LOCL/DRD
Not in a braking condition	EFM signal is not synchronizing in 1/16 frames	L
	EFM signal is synchronizing in 1/16 frames	H
Braking condition	Low disc rotation status monitor signal 8/DRD signal	DRD signal

5. CLV SERVO CONTROL

(1) PWM control

The CLV servo control circuit controls the disc motor with the frequency difference between the clock reproduced from EFM signal and clock obtained from the standard oscillator, and the address difference in internal RAM writing.

The motor control output is transmitted to PWM_1 (deceleration output) and PWM_2 (acceleration output) pins in PWM waveform.

Since the phase is internally compensated. the CLV servo circuit can be configured by just connecting a driver to the PWM_1 and PWM_2 pins outputs.

Fig. 3, shows the CLV waveform and its duty.

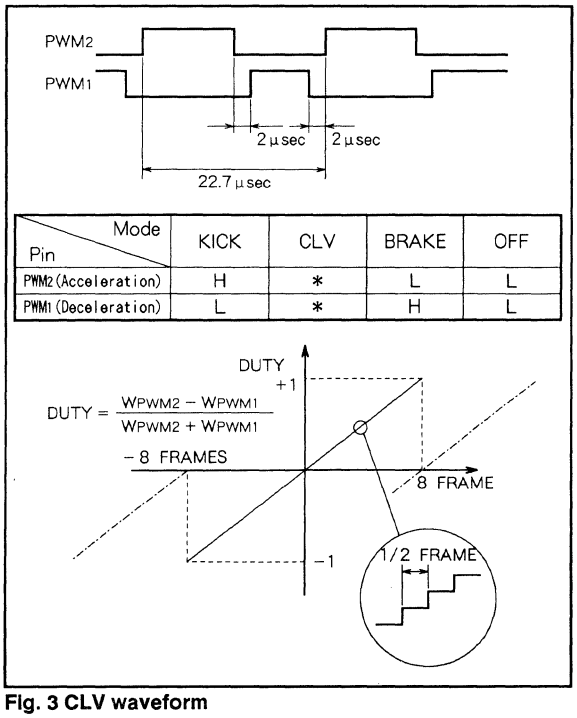
In the CIRC composite section, the duty is reset to 0 where the address difference between built-in RAM wrtie and read exceeds ± 8 frames,

In this figure, the point in which the waveform width of acceleration output and deceleration output is equal is shown as dut "0".

The disc motor can be driven even when the PWM waveform is used directly or even through and analog signal in which PWM_1 & PWM_2 outputs are integrated.

When the disc motor is driven with an analog signal, servo gain can be set externally.

When it is driven with a PWM waveform, however, the PWM waveform cannot adjust the duty from the outside; therefore, the servo chracteristics are determined with the motor torque or disc turntable, disc retaining angular moment, etc.



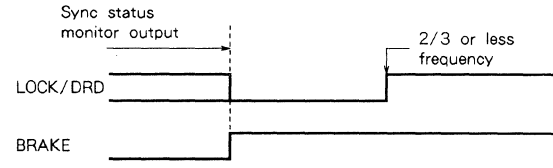
Mode / Pin	KICK	CLV	BRAKE	OFF
PWM2 (Acceleration)	H	*	L	L
PWM1 (Deceleration)	L	*	H	L

Fig. 3 CLV waveform

(2) Low disc rotation control

When playback is suspended, disc rotation should be stopped securely. The LOCK/DRD pin monitors the PLL oscillation frequency the disc is being braked with an instruction from the microcomputer, and outputs "H" if it detects a frequency lower than 2/3 of that in normal playback.

By adjusting the period of a brake signal with this signlal, disc rotation can be stopped.



Conditions	Contents	LOCL/DRD
Not in a braking state	Sync status monitor output	LOCK
Braking state	The PLL oscillation frequency is more than 2/3 of that in normal playback	L
	The PLL oscillation frequency is less than 2/3 of that in normal playback	H

6. ERROR CORRECTION

(1) Correction ability

Both decoders C1, C2 correct dual errors Max.

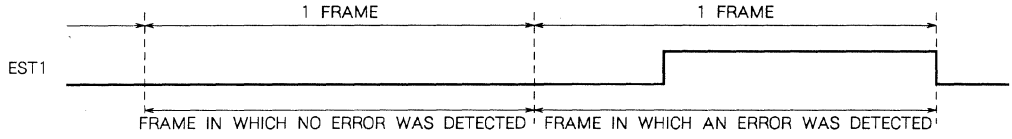
(2) Error monitor output

The error status detected at decoding is output to pins EST_1, EST_2.

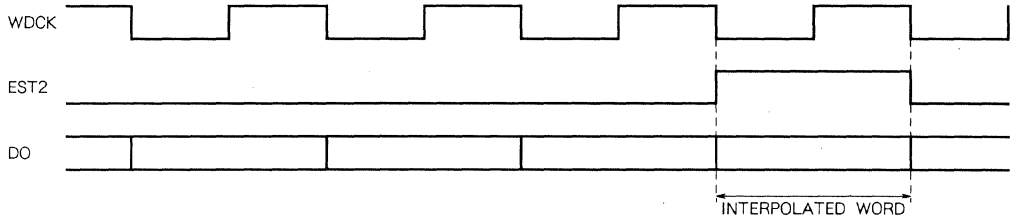
If an error is detected with decoder C1, "H" is output to pin EST_1 for its frame. and "H" is output to pin EST_2 for an erroneous word judged to be uncorrectable with decoder C2 If a non-audio data is selected in mode 1 of microcomputer, interface, no output data is interpolated,and the error status of decorder C2 is output to the data (each byte) detected as uncorrectable.

If an audio data is selected, the error status is output to the interpolated word (2 bytes).

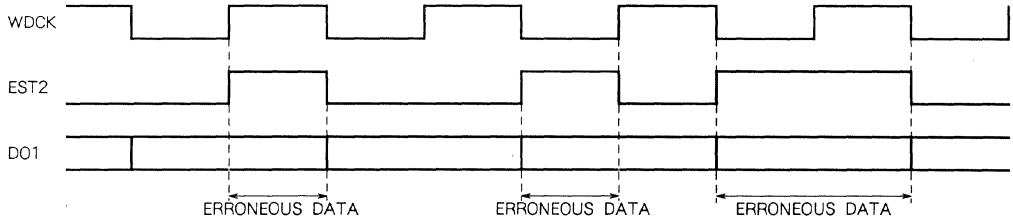
For detailed timing, refer to "D/A Interface"



(a) For audio data



(b) For non-audio data

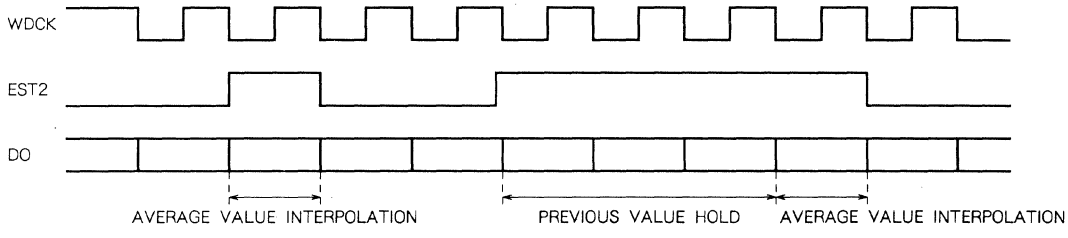


(3) Interpolation

The average value is interpolated or the porevious value hold is interpolated for the word that cannot be corrected by decoder C2, thus preventing noise from generating.

If the anterior and posterior words from which an error was detected prove correct after detection, the average value interpolation is carried out, and in other cases, the previous value hold is carried out.

However, if the non-audio data is selected in mode 1, no interpolation processing is performed . (Refer to "MICROCOMPUTER INTERFACE".)



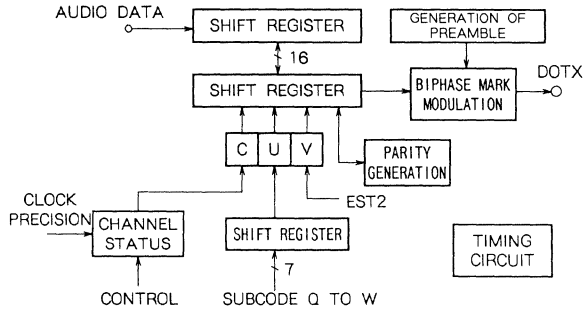
7. DIGITAL OUT

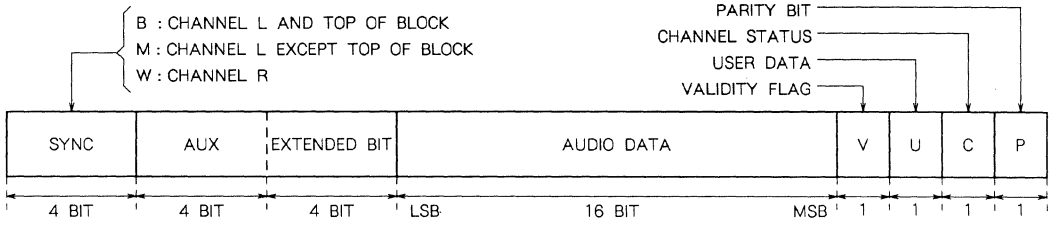
The digital audio signal formatted according to EIAJ Standard CP-340 "Digital Audio Interface" is outputted to DOTX pin.

The validity flag is internally set to "1" automatically when the interpolated word is transmitted.

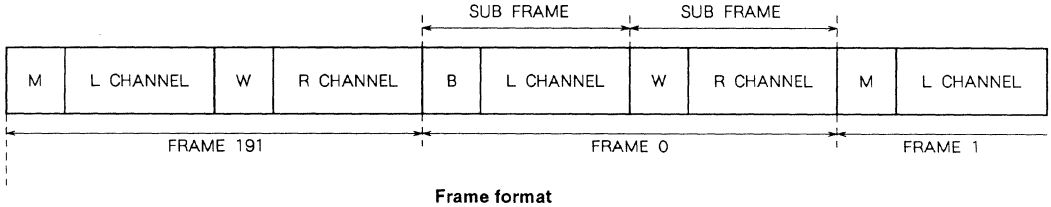
The user data, which is read in the subcode interface circuit, is transmitted. Channel clock precision can be set from the outside so that it is compatible with the validity pitch.

The channel status is set to level III in the validity pitch, mode, and level II is set autometically when it is not in the validity pitch mode.

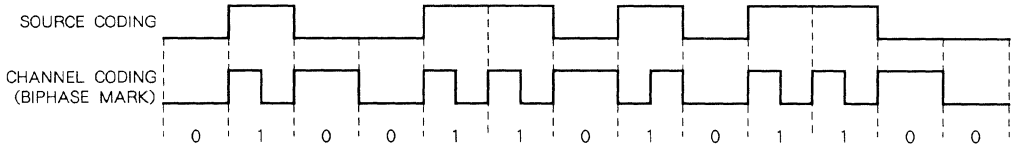




Sub frame format



Frame format



Channel coding (Biphase mark modulation)

If Digital-OUT is not used to prevent spurious radiation, it is possible to turn DOTX pin output "OFF" by setting mode 1 of microcomputer interface.

Channel status clock precision can be set by ACCK register of mode 1 of microcomputer interface.

8. THE DIGITAL FILTER

The data of sampling frequency 44.1kHz is converted to that of sampling frequency 176.4kHz at 4 times over-sampling by FIR phase linear digital filter. It is also possible to output deta of 18-bit and 20-bit that were computed by the digital filter. The digital filter may also pass according to the purposes : a high-precision digital filter is connected externally, and this filter is suitable for signal processing that handles non-audio data, such as CD-ROM as well.

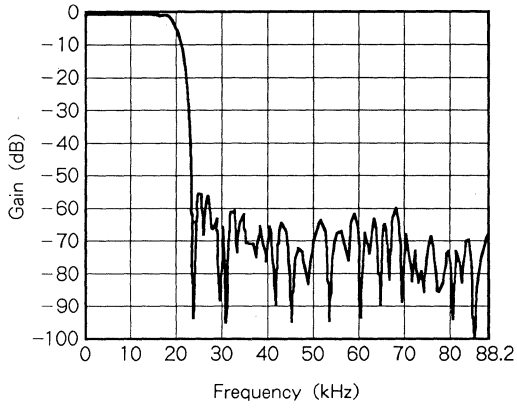
The characteristics in over-sampling are shown in Fig. 4 below.

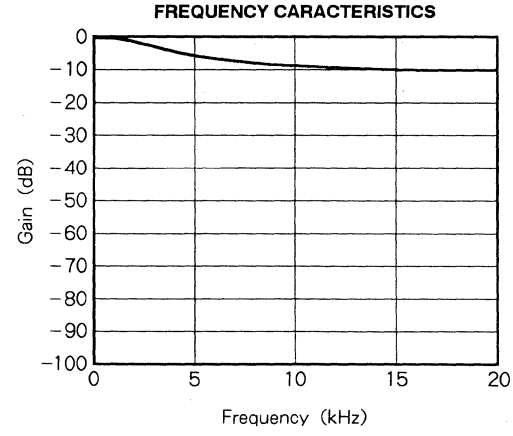
9. DIGITAL DE-EMPHASIS

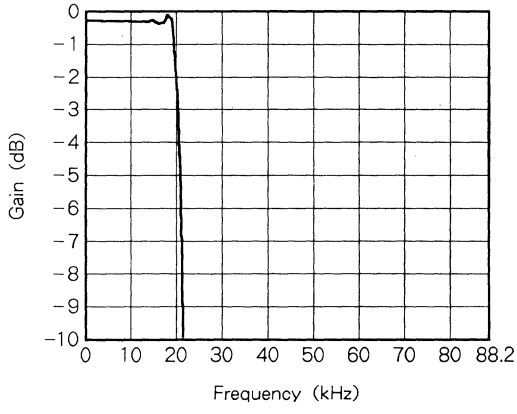
M65822AFP has a built-in digital de-emphsis circuit containing a primary IIR filter. When DDEC bit of the status register is in "L", the source emphasis information is detected : if emphasis is rresent, the de-emphasis ciruit of 50 /15(μ) operates automatically.

When DDEC bit is in "H", the intermal de-emphsis circuit is disabled regardless of presence or absence of emphasis information, and only emphasis information is output from EMP pin. (When DDEC bit is in "L", emphasis information is also output from EMP pin.)

The following is the chracteristic chart for the de-emphsis circuit built in the M65822AFP.







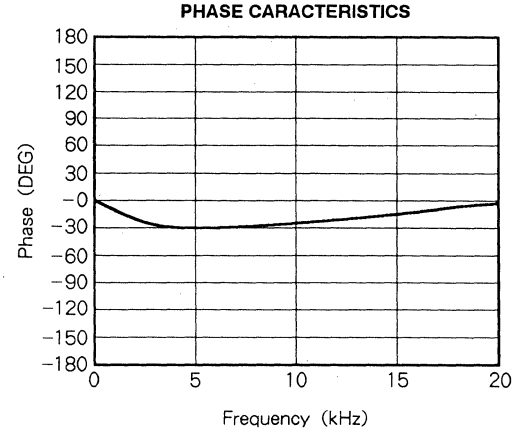


Fig. 4 Characteristic curve of digital filter

10. MUTE CONTROL

(1) Zero cross muting

In the MUTE command is input from the microcomputer, the timing (zero-cross) at which the highest bit changes from "0" to "1" or "1" to "0" is detected, actuating the mute circuit. If zero cross cannot be detected within the specified time, the internal counter counts 34.8msec, forcedly actuating the mute circuit.

If the ZCRC register is set to "1", zero cross is forcedly muted with the MUTE command regardless of the presence or absence of zero cross.

(2) Attenuation control

If the ATT register is set to "1", the audio output is transmitted with − 12dB down.

(3) Automatic fade mute

If the FMCNT register is set to "1", and the FMUTE register setting is changed from "0" to "1", the internal counter operates and the audio data fades in. This data fades out by changing FMUTE register setting from "1" to "0"

Two types of fade time can be set by setting the FMTC register.

Since "FADE MUTE" operates with the level set by the attenuate register as standard, attention should be paid to the attenuate register condition before operation start.

Fade time

FMTC	Fade time
L	2.2sec
H	34.8msec

(4) Control by the attenuate register

If the FMUTE register is set at "1" with the FMCNT register at "0", the audio data attenuates according to the contents of attenuate register, which are shown in Table 2.

Attenuate register control is carried out in 8 bits independently for right (R) and left (L) channels according to the microcomputer interface mode.

As shown in Table 2, the attenuate register is set in 8 bits. However, control up to − 96.3dB is available with internal processing.

Table 1. Attenuation control

No	Coefficient								Attenuation (dB)	No	Coefficient								Attenuation (dB)
	C0	C1	C2	C3	C4	C5	C6	C7			C0	C1	C2	C3	C4	C5	C6	C7	
FF	1	1	1	1	1	1	1	1	− 0.27	CF	1	1	1	1	0	0	1	1	− 18.34
FE	0	1	1	1	1	1	1	1	− 0.56	CE	0	1	1	1	0	0	1	1	− 18.62
FD	1	0	1	1	1	1	1	1	− 0.86	CD	1	0	1	1	0	0	1	1	− 18.92
FC	0	0	1	1	1	1	1	1	− 1.16	CC	0	0	1	1	0	0	1	1	− 19.22
FB	1	1	0	1	1	1	1	1	− 1.48	CB	1	1	0	1	0	0	1	1	− 19.54
FA	0	1	0	1	1	1	1	1	− 1.80	CA	0	1	0	1	0	0	1	1	− 19.86
F9	1	0	0	1	1	1	1	1	− 2.14	C9	1	0	0	1	0	0	1	1	− 20.21
F8	0	0	0	1	1	1	1	1	− 2.50	C8	0	0	0	1	0	0	1	1	− 20.56
F7	1	1	1	0	1	1	1	1	− 2.87	C7	1	1	1	0	0	0	1	1	− 20.93
F6	0	1	1	0	1	1	1	1	− 3.25	C6	0	1	1	0	0	0	1	1	− 21.32
F5	1	0	1	0	1	1	1	1	− 3.66	C5	1	0	1	0	0	0	1	1	− 21.72
F4	0	0	1	0	1	1	1	1	− 4.08	C4	0	0	1	0	0	0	1	1	− 22.14
F3	1	1	0	0	1	1	1	1	− 4.53	C3	1	1	0	0	0	0	1	1	− 22.59
F2	0	1	0	0	1	1	1	1	− 5.00	C2	0	1	0	0	0	0	1	1	− 23.06
F1	1	0	0	0	1	1	1	1	− 5.49	C1	1	0	0	0	0	0	1	1	− 23.56
F0	0	0	0	0	1	1	1	1	− 6.02	C0	0	0	0	0	0	0	1	1	− 24.08
EF	1	1	1	1	0	1	1	1	− 6.30	BF	1	1	1	1	1	1	0	1	− 24.39
EE	0	1	1	1	0	1	1	1	− 6.58	BE	0	1	1	1	1	1	0	1	− 24.64
ED	1	0	1	1	0	1	1	1	− 6.88	BD	1	0	1	1	1	1	0	1	− 24.94
EC	0	0	1	1	0	1	1	1	− 7.18	BC	0	0	1	1	1	1	0	1	− 25.24
EB	1	1	0	1	0	1	1	1	− 7.50	BB	1	1	0	1	1	1	0	1	− 25.56
EA	0	1	0	1	0	1	1	1	− 7.82	BA	0	1	0	1	1	1	0	1	− 25.89
E9	1	0	0	1	0	1	1	1	− 8.16	B9	1	0	0	1	1	1	0	1	− 26.22
E8	0	0	0	1	0	1	1	1	− 8.52	B8	0	0	0	1	1	1	0	1	− 26.58
E7	1	1	1	0	0	1	1	1	− 8.89	B7	1	1	1	0	1	1	0	1	− 26.95
E6	0	1	1	0	0	1	1	1	− 9.28	B6	0	1	1	0	1	1	0	1	− 27.34
E5	1	0	1	0	0	1	1	1	− 9.68	B5	1	0	1	0	1	1	0	1	− 27.74
E4	0	0	1	0	0	1	1	1	− 10.10	B4	0	0	1	0	1	1	0	1	− 28.16
E3	1	1	0	0	0	1	1	1	− 10.55	B3	1	1	0	0	1	1	0	1	− 28.61
E2	0	1	0	0	0	1	1	1	− 11.02	B2	0	1	0	0	1	1	0	1	− 29.08
E1	1	0	0	0	0	1	1	1	− 11.51	B1	1	0	0	0	1	1	0	1	− 29.58
E0	0	0	0	0	0	1	1	1	− 12.04	B0	0	0	0	0	1	1	0	1	− 30.10
DF	1	1	1	1	1	0	1	1	− 12.32	AF	1	1	1	1	0	1	0	1	− 30.38
DE	0	1	1	1	1	0	1	1	− 12.60	AE	0	1	1	1	0	1	0	1	− 30.66
DD	1	0	1	1	1	0	1	1	− 12.90	AD	1	0	1	1	0	1	0	1	− 30.96
DC	0	0	1	1	1	0	1	1	− 13.20	AC	0	0	1	1	0	1	0	1	− 31.26
DB	1	1	0	1	1	0	1	1	− 13.52	AB	1	1	0	1	0	1	0	1	− 31.58
DA	0	1	0	1	1	0	1	1	− 13.84	AA	0	1	0	1	0	1	0	1	− 31.91
D9	1	0	0	1	1	0	1	1	− 14.19	A9	1	0	0	1	0	1	0	1	− 32.25
D8	0	0	0	1	1	0	1	1	− 14.54	A8	0	0	0	1	0	1	0	1	− 32.60
D7	1	1	1	0	1	0	1	1	− 14.91	A7	1	1	1	0	0	1	0	1	− 32.97
D6	0	1	1	0	1	0	1	1	− 15.29	A6	0	1	1	0	0	1	0	1	− 33.36
D5	1	0	1	0	1	0	1	1	− 15.70	A5	1	0	1	0	0	1	0	1	− 33.76
D4	0	0	1	0	1	0	1	1	− 16.12	A4	0	0	1	0	0	1	0	1	− 34.19
D3	1	1	0	0	1	0	1	1	− 16.57	A3	1	1	0	0	0	1	0	1	− 34.63
D2	0	1	0	0	1	0	1	1	− 17.04	A2	0	1	0	0	0	1	0	1	− 35.10
D1	1	0	0	0	1	0	1	1	− 17.54	A1	1	0	0	0	0	1	0	1	− 35.60
D0	0	0	0	0	1	0	1	1	− 18.06	A0	0	0	0	0	0	1	0	1	− 36.12

Table 1. Attenuation control (Continued)

No	Coefficient								Attenuation (dB)	No	Coefficient								Attenuation (dB)
	C0	C1	C2	C3	C4	C5	C6	C7			C0	C1	C2	C3	C4	C5	C6	C7	
9F	1	1	1	1	1	0	0	1	− 36.40	6F	1	1	1	1	0	1	1	0	− 54.46
9E	0	1	1	1	1	0	0	1	− 36.68	6E	0	1	1	1	0	1	1	0	− 54.75
9D	1	0	1	1	1	0	0	1	− 36.98	6D	1	0	1	1	0	1	1	0	− 55.04
9C	0	0	1	1	1	0	0	1	− 37.28	6C	0	0	1	1	0	1	1	0	− 55.34
9B	1	1	0	1	1	0	0	1	− 37.60	6B	1	1	0	1	0	1	1	0	− 55.66
9A	0	1	0	1	1	0	0	1	− 37.93	6A	0	1	0	1	0	1	1	0	− 55.99
99	1	0	0	1	1	0	0	1	− 38.27	69	1	0	0	1	0	1	1	0	− 56.33
98	0	0	0	1	1	0	0	1	− 36.62	68	0	0	0	1	0	1	1	0	− 56.68
97	1	1	1	0	1	0	0	1	− 38.99	67	1	1	1	0	0	1	1	0	− 57.05
96	0	1	1	0	1	0	0	1	− 39.38	66	0	1	1	0	0	1	1	0	− 57.44
95	1	0	1	0	1	0	0	1	− 39.78	65	1	0	1	0	0	1	1	0	− 57.84
94	0	0	1	0	1	0	0	1	− 40.21	64	0	0	1	0	0	1	1	0	− 58.27
93	1	1	0	0	1	0	0	1	− 40.65	63	1	1	0	0	0	1	1	0	− 58.71
92	0	1	0	0	1	0	0	1	− 41.12	62	0	1	0	0	0	1	1	0	− 59.18
91	1	0	0	0	1	0	0	1	− 41.62	61	1	0	0	0	0	1	1	0	− 59.68
90	0	0	0	0	1	0	0	1	− 42.14	60	0	0	0	0	0	1	1	0	− 60.21
8F	1	1	1	1	0	0	0	1	− 42.42	5F	1	1	1	1	1	0	1	0	− 60.48
8E	0	1	1	1	0	0	0	1	− 42.70	5E	0	1	1	1	1	0	1	0	− 60.77
8D	1	0	1	1	0	0	0	1	− 43.00	5D	1	0	1	1	1	0	1	0	− 61.06
8C	0	0	1	1	0	0	0	1	− 43.30	5C	0	0	1	1	1	0	1	0	− 61.37
8B	1	1	0	1	0	0	0	1	− 43.62	5B	1	1	0	1	1	0	1	0	− 61.68
8A	0	1	0	1	0	0	0	1	− 43.95	5A	0	1	0	1	1	0	1	0	− 62.01
89	1	0	0	1	0	0	0	1	− 44.29	59	1	0	0	1	1	0	1	0	− 62.35
88	0	0	0	1	0	0	0	1	− 44.64	58	0	0	0	1	1	0	1	0	− 62.70
87	1	1	1	0	0	0	0	1	− 45.01	57	1	1	1	0	1	0	1	0	− 63.07
86	0	1	1	0	0	0	0	1	− 45.40	56	0	1	1	0	1	0	1	0	− 63.46
85	1	0	1	0	0	0	0	1	− 45.80	55	1	0	1	0	1	0	1	0	− 63.86
84	0	0	1	0	0	0	0	1	− 46.23	54	0	0	1	0	1	0	1	0	− 64.28
83	1	1	0	0	0	0	0	1	− 46.67	53	1	1	0	0	1	0	1	0	− 64.73
82	0	1	0	0	0	0	0	1	− 47.14	52	0	1	0	0	1	0	1	0	− 65.20
81	1	0	0	0	0	0	0	1	− 47.64	51	1	0	0	0	1	0	1	0	− 65.70
80	0	0	0	0	0	0	0	1	− 48.16	50	0	0	0	0	1	0	1	0	− 66.22
7F	1	1	1	1	0	1	1	1	− 48.44	4F	1	1	1	1	0	0	1	0	− 66.50
7E	0	1	1	1	0	1	1	1	− 48.73	4E	0	1	1	1	0	0	1	0	− 66.79
7D	1	0	1	1	0	1	1	1	− 49.02	4D	1	0	1	1	0	0	1	0	− 67.08
7C	0	0	1	1	0	1	1	1	− 49.32	4C	0	0	1	1	0	0	1	0	− 67.39
7B	1	1	0	1	0	1	1	1	− 49.64	4B	1	1	0	1	0	0	1	0	− 67.70
7A	0	1	0	1	0	1	1	1	− 49.96	4A	0	1	0	1	0	0	1	0	− 68.03
79	1	0	0	1	0	1	1	1	− 50.31	49	1	0	0	1	0	0	1	0	− 68.37
78	0	0	0	1	0	1	1	1	− 50.66	48	0	0	0	1	0	0	1	0	− 68.73
77	1	1	1	0	0	1	1	1	− 51.03	47	1	1	1	0	0	0	1	0	− 69.10
76	0	1	1	0	0	1	1	1	− 51.42	46	0	1	1	0	0	0	1	0	− 69.48
75	1	0	1	0	0	1	1	1	− 51.82	45	1	0	1	0	0	0	1	0	− 69.89
74	0	0	1	0	0	1	1	1	− 52.25	44	0	0	1	0	0	0	1	0	− 70.31
73	1	1	0	0	0	1	1	1	− 52.69	43	1	1	0	0	0	0	1	0	− 70.75
72	0	1	0	0	0	1	1	1	− 53.16	42	0	1	0	0	0	0	1	0	− 71.22
71	1	0	0	0	0	1	1	1	− 53.66	41	1	0	0	0	0	0	1	0	− 71.72
70	0	0	0	0	0	1	1	1	− 54.18	40	0	0	0	0	0	0	1	0	− 72.25

Table 1. Attenuation control (Continued)

No	Coefficient								Attenuation (dB)	No	Coefficient								Attenuation (dB)
	C0	C1	C2	C3	C4	C5	C6	C7			C0	C1	C2	C3	C4	C5	C6	C7	
3F	1	1	1	1	1	1	0	0	− 72.81	1F	1	1	1	1	1	0	0	0	− 86.79
3E	0	1	1	1	1	1	0	0	− 72.81	1E	0	1	1	1	1	0	0	0	− 86.79
3D	1	0	1	1	1	1	0	0	− 73.41	1D	1	0	1	1	1	0	0	0	− 86.79
3C	0	0	1	1	1	1	0	0	− 73.41	1C	0	0	1	1	1	0	0	0	− 86.79
3B	1	1	0	1	1	1	0	0	− 74.05	1B	1	1	0	1	1	0	0	0	− 86.79
3A	0	1	0	1	1	1	0	0	− 74.05	1A	0	1	0	1	1	0	0	0	− 86.79
39	1	0	0	1	1	1	0	0	− 74.75	19	1	0	0	1	1	0	0	0	− 86.79
38	0	0	0	1	1	1	0	0	− 74.75	18	0	0	0	1	1	0	0	0	− 86.79
37	1	1	1	0	1	1	0	0	− 75.50	17	1	1	1	0	1	0	0	0	− 91.31
36	0	1	1	0	1	1	0	0	− 75.50	16	0	1	1	0	1	0	0	0	− 91.31
35	1	0	1	0	1	1	0	0	− 76.32	15	1	0	1	0	1	0	0	0	− 91.31
34	0	0	1	0	1	1	0	0	− 76.32	14	0	0	1	0	1	0	0	0	− 91.31
33	1	1	0	0	1	1	0	0	− 77.24	13	1	1	0	0	1	0	0	0	− 91.31
32	0	1	0	0	1	1	0	0	− 77.24	12	0	1	0	0	1	0	0	0	− 91.31
31	1	0	0	0	1	1	0	0	− 78.26	11	1	0	0	0	1	0	0	0	− 91.31
30	0	0	0	0	1	1	0	0	− 78.26	10	0	0	0	0	1	0	0	0	− 91.31
2F	1	1	1	1	0	1	0	0	− 79.43	0F	1	1	1	1	0	0	0	0	− 96.33
2E	0	1	1	1	0	1	0	0	− 79.43	0E	0	1	1	1	0	0	0	0	− 96.33
2D	1	0	1	1	0	1	0	0	− 79.43	0D	1	0	1	1	0	0	0	0	− 96.33
2C	0	0	1	1	0	1	0	0	− 79.43	0C	0	0	1	1	0	0	0	0	− 96.33
2B	1	1	0	1	0	1	0	0	− 80.77	0B	1	1	0	1	0	0	0	0	− 96.33
2A	0	1	0	1	0	1	0	0	− 80.77	0A	0	1	0	1	0	0	0	0	− 96.33
29	1	0	0	1	0	1	0	0	− 80.77	09	1	0	0	1	0	0	0	0	− 96.33
28	0	0	0	1	0	1	0	0	− 80.77	08	0	0	0	1	0	0	0	0	− 96.33
27	1	1	1	0	0	1	0	0	− 82.35	07	1	1	1	0	0	0	0	0	− 96.33
26	0	1	1	0	0	1	0	0	− 82.35	06	0	1	1	0	0	0	0	0	− 96.33
25	1	0	1	0	0	1	0	0	− 82.35	05	1	0	1	0	0	0	0	0	− 96.33
24	0	0	1	0	0	1	0	0	− 82.35	04	0	0	1	0	0	0	0	0	− 96.33
23	1	1	0	0	0	1	0	0	− 84.29	03	1	1	0	0	0	0	0	0	− 96.33
22	0	1	0	0	0	1	0	0	− 84.29	02	0	1	0	0	0	0	0	0	− 96.33
21	1	0	0	0	0	1	0	0	− 84.29	01	1	0	0	0	0	0	0	0	− 96.33
20	0	0	0	0	0	1	0	0	− 84.29	00	0	0	0	0	0	0	0	0	− ∞

11. DIGITAL SILENCE

When SIL/EST bit of the status register is in "L" if the audio data meets the following requirements, the computer regards the current condition as silent, and a silence single is output from RSIL/EST1 & RSIL/EST2 pins.

〈Silence Conditions〉

〔If the sudio data is hexadecimal, and the period of "0000" or "FFFF" continues for at least 200msec, the current condition is regarded as silent. However, if "0000" and "FFFF" are displayed alternately even once within 200msec, it is not regarded as silence.〕

Rch silence information and Lch silence information are output from RSIL/EST1 and LSIL/EST2 pins respectively. If both pins are judged to be silent, "L" is output.

When SIL/EST bit is in "H", the pin becomes an error monitor pin for error correction : C1 error and C2 error are output from RSIL/EST1 and LSIL/EST2 pins respectively.

When SILC bit is in "L", silence information is output independently for R & L channels as explained above.

When SILC bit is in "H", silence information is output from RSIL/EST1 pin if both Lch and Rch audio data sre placed in the silent state.

12. DAC INTERFACE

(1) DAC interface mode table

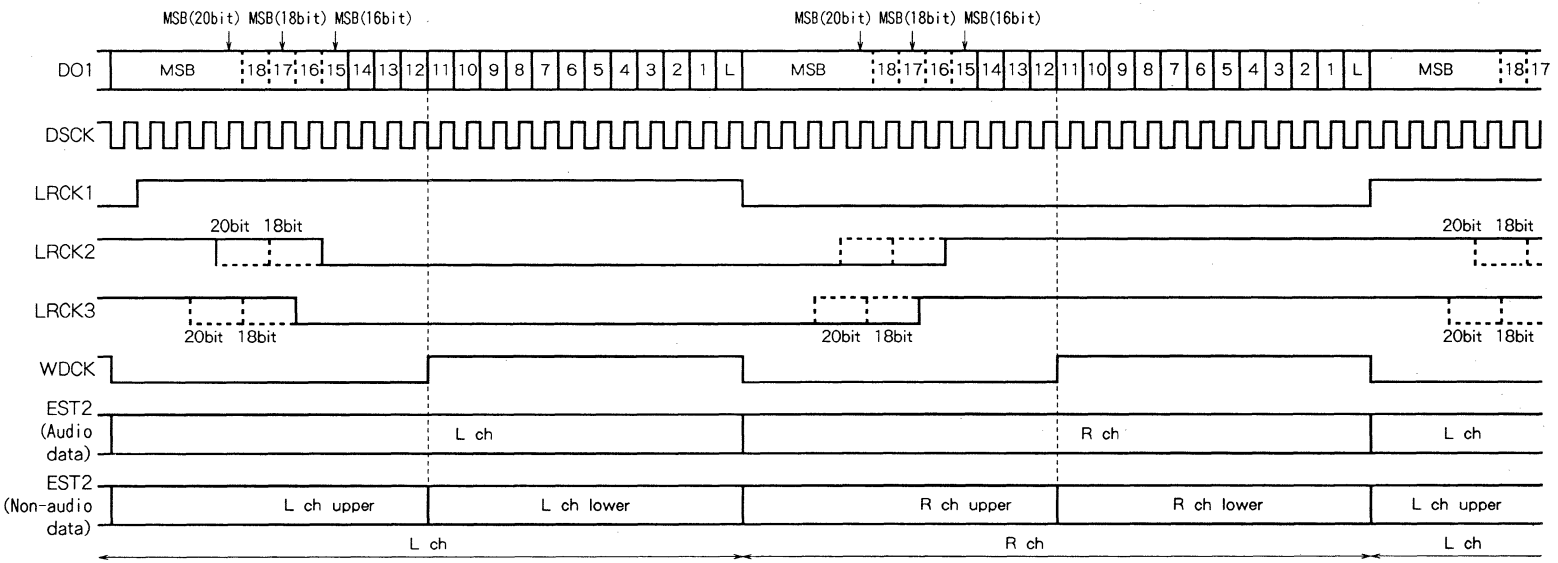
No.	Register name					Operation	Fs
	NON-AUDIO	DFPAS	18BIT	20BIT	DUAL-DAC		
1	L	L	L	L	L	16-bit single DAC	4Fs
2	L	L	L	L	H	16-bit dual DAC	4Fs
3	L	L	H	L	L	18-bit single DAC	4Fs
4	L	L	H	L	H	18-bit dual DAC	4Fs
5	L	L	L	H	L	20-bit single DAC	4Fs
6	L	L	L	H	H	20-bit dual DAC	4Fs
7	L	H	L	L	L	16-bit single DAC	Fs
8	H	H	L	L	L	Non-audio mode	Fs

(2) Stereo/Monaural mode selection

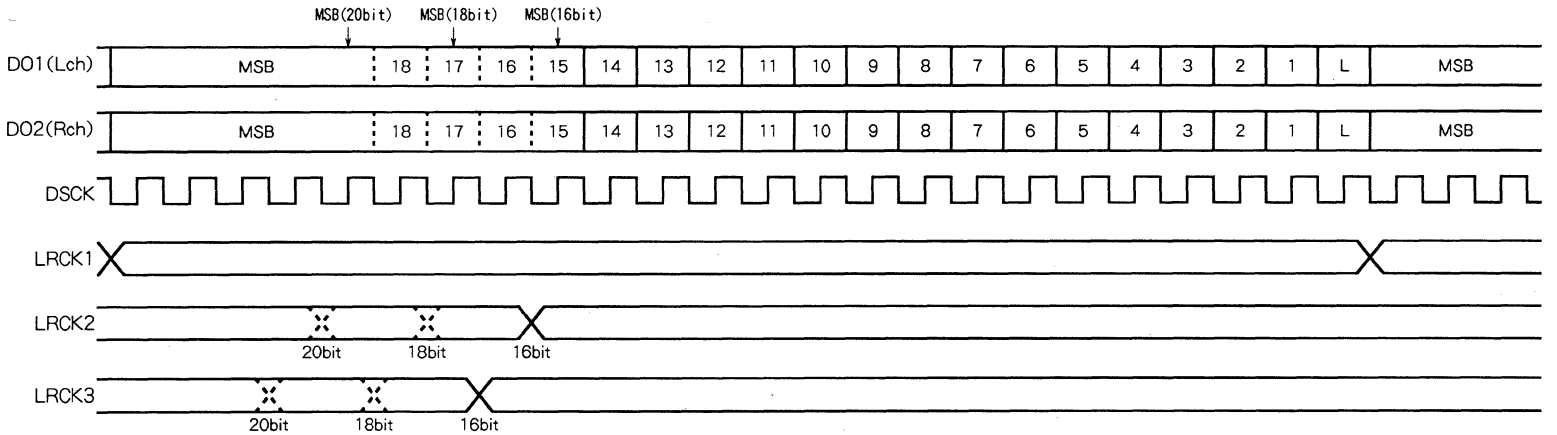
Register name		Operation
LMONO	RMONO	
L	L	Stereo output
H	L	Lch monoural output
L	H	Rch monoural output
H	H	Inhibit

(3) DAC interface time chart

(3-1)Single DAC mode



(3-2)Dual DAC Mode



13 OSCILLATION CIRCUIT

(1) Self-oscillation circuit

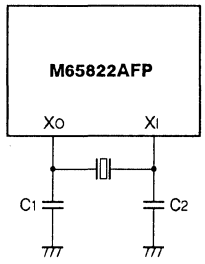
An oscillation circuit can be formed by connecting a 8.4672 MHz or 16.9344MHz crystal oscillator and loading to pins X_I, X_O.

8.4672 (16.9344MHz) shaped from this oscillator is output to C846 pin, and 4.2336MHz (8.4672MHz) divided and generated is output to C423 pin.

The oscillation frequency is selected as follows, using CKSEL pin :

Vibrator	CKSEL	Remarks
8.4672MHz	H	Normal playback mode
16.9344MHz	L	
16.9344MHz	H	Double speed playback mode

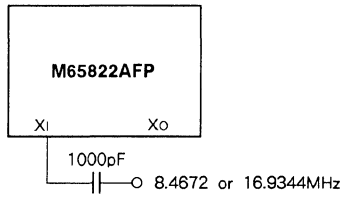
Vibrator	Load capacity value (Reference)
8.4672MHz	30pF
16.9344MHz	15pF



(2) When external clock is used

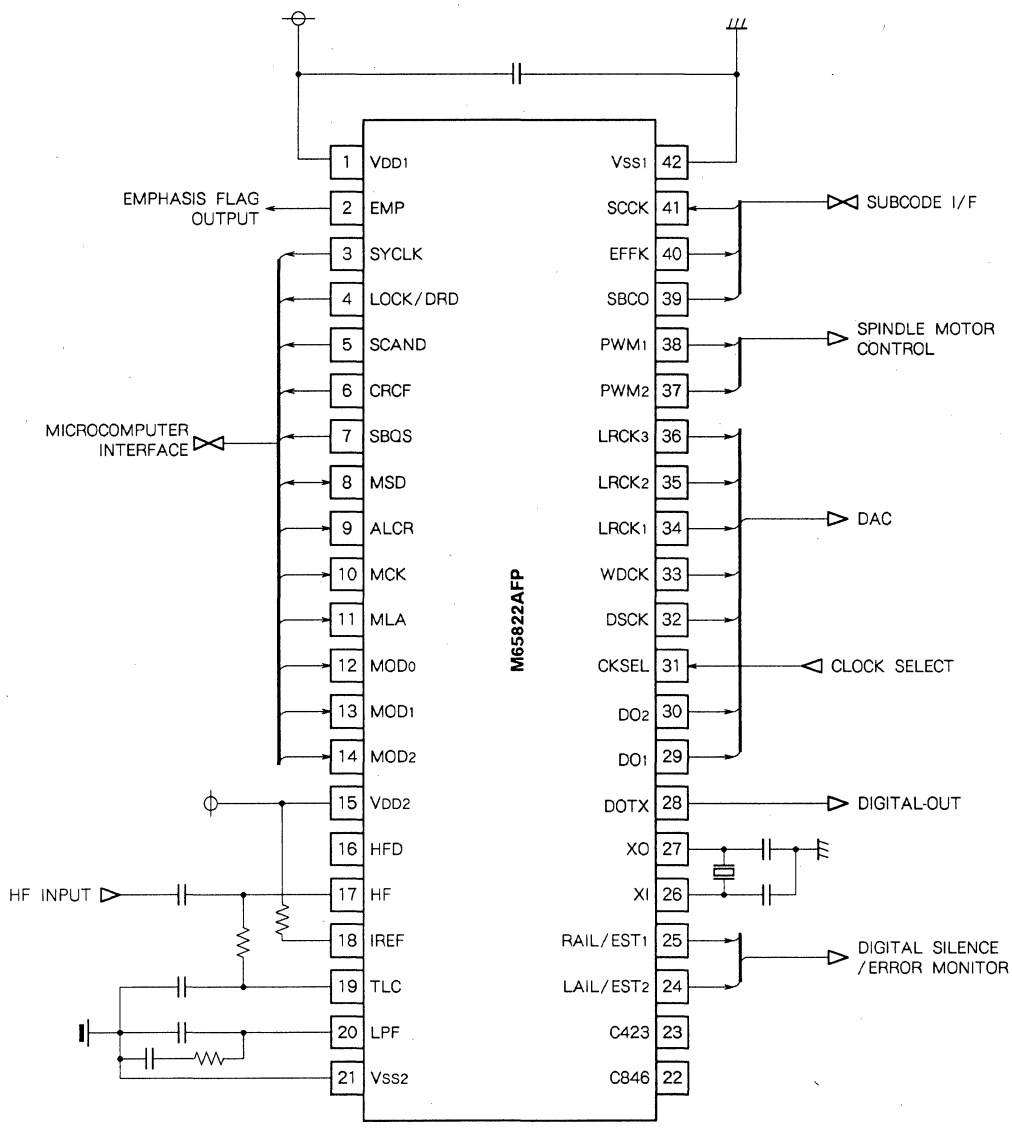
If an 8.4672MHz or 16.9344MHz clock is present inside the system, the data can be input through the capacitor to pin X_I without using a crystal vibrator. (No capacitor is required if the input level corresponds to a logic level.)

The selection of a vibrator according to the crystal clock output and CKSEL pin is the same as in self-oscillation.



External clock	Min.	Max.
V_{IH}	GND	V_{DD}
Amplitude	$1V_{P-P}$	–

APPLICATION EXAMPLE



M51566P

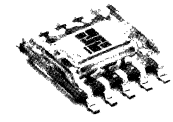
PREAMPLIFIER WITH PHOTODETECTOR FOR OPTICAL PICKUP

DESCRIPTION

The M51566P is a semiconductor integrated circuit developed for CD players.
The IC is housed in a 10-pin clear molded plastic package and contains 6 preamplifiers with divided photodetectors.

FEATURES

- 6 amplifiers with divided photodetectors
- For 3 LASER pickup system
- 2 operation modes can be selected rated supply voltage

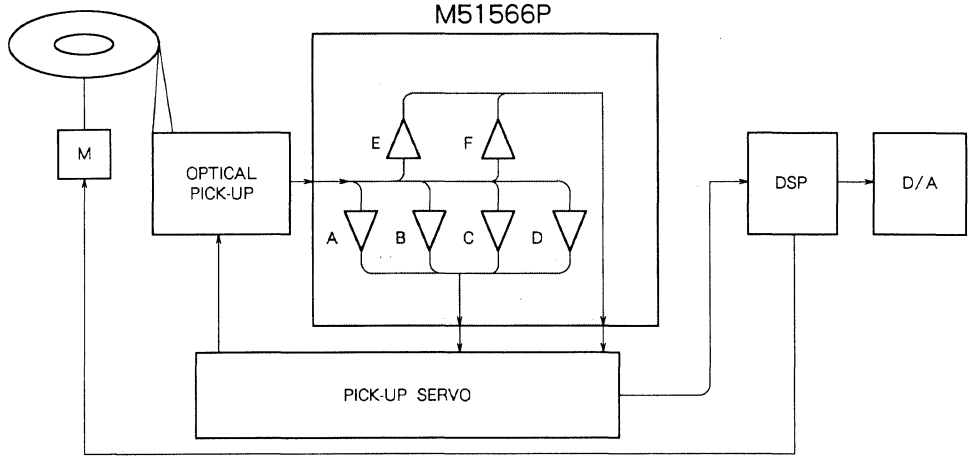


Outline 10C2-C
1.27mm pitch 300mil SOP
(5.3mm × 6.13mm × 1.75mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC}, V_{EE} = ± 4.5~5.5V
or V_{CC} = 4.5~5.5V
Rated supply voltage ..... V_{CC}, V_{EE} = ± 5V or V_{CC} = 5V
Rated power dissipation 20mW

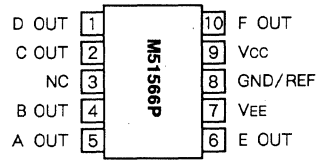
SYSTEM CONFIGURATION



M51566P

PREAMPLIFIER WITH PHOTODETECTOR FOR OPTICAL PICKUP

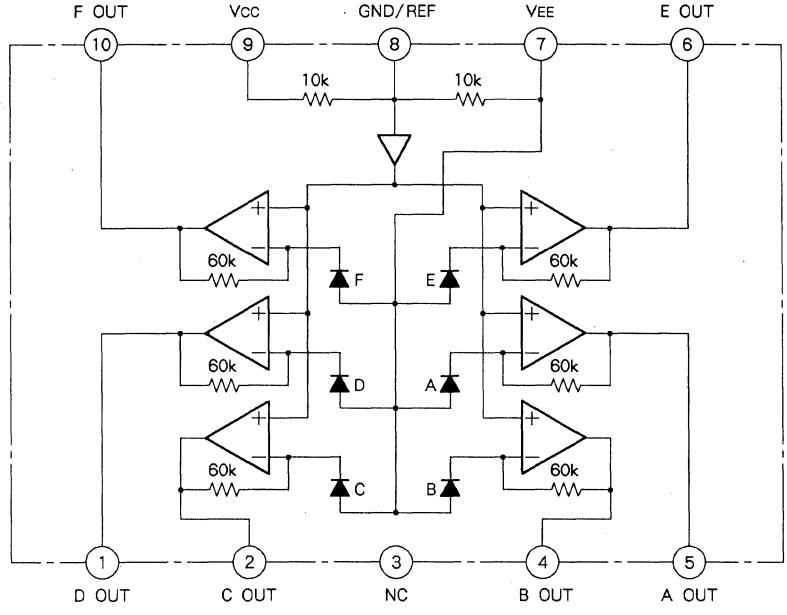
PIN CONFIGURATION



Outline 10C2-C

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6.5	V
V_{EE}		− 6.5	V
P_d	Power dissipation ($T_a \geqq 25$℃)	180	mV
T_{opr}	Operating temperature	− 20 ~ + 65	℃
T_{stg}	Storage temperature	− 40 ~ + 85	℃

ELECTRICAL CHARACTERISTICS

(1) AT SPLIT SUPPLY VOLTAGE (V_{CC} = + 5V, V_{EE} = − 5V, R_L = 10kΩ, Ta = 25℃)

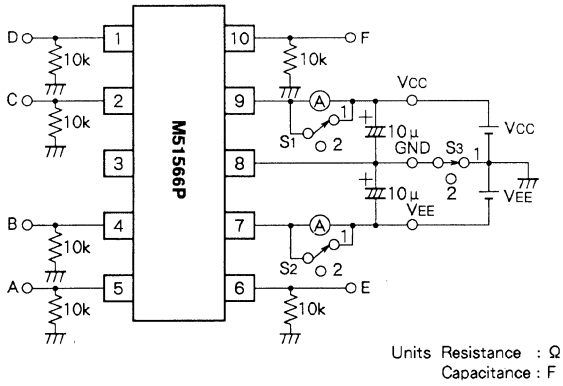
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CCO}	Circuit current	In the dark	−	4	8	mA
I_{EEO}			− 8	− 4	−	mA
V_O	Output voltage	P_O = 5μW, λ = 780nm, Output A~F, without offset voltage	−	100	−	mV
V_{off}	Output offset voltage	In the dark output A~F	−	0	± 60	mV
$\triangle V_{off}$	Delta output offset voltage	(A + C) − (B + D)	−	0	± 40	mV
		E − F	−	0	± 25	mV
fc	Freqiency characteristic	P_O = 5μW, λ = 780nm, 10% modulation, 3 dB down, output A~F	1	3	−	MHz

(2) AT SINGLE SUPPLY VOLTAGE (V_{CC} = 5V, R_L = 10kΩ, Ta = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CCO}	Circuit current	In the dark	−	3.5	7	mA
V_O	Output current	P_O = 5μW, λ = 780nm, Output A~F, without offset voltage	−	100	−	mV
V_{off}	Output offset voltage	In the dark Output A~F	−	0	± 60	mV
$\triangle V_{off}$	Delta output offset voltage	(A + C) − (B + D)	−	0	± 40	mV
		E − F	−	0	± 25	mV
V_O	Frequency characteristic	P_O = 5μW, λ = 780nm, 10%, modulation, 3 dB down, output A~F	1	3	−	MHz

Note : Voltage is the offset from the 8-pin voltage.

TEST CIRCUIT



Units Resistance : Ω
Capacitance : F

SWITCH CONDITIONS

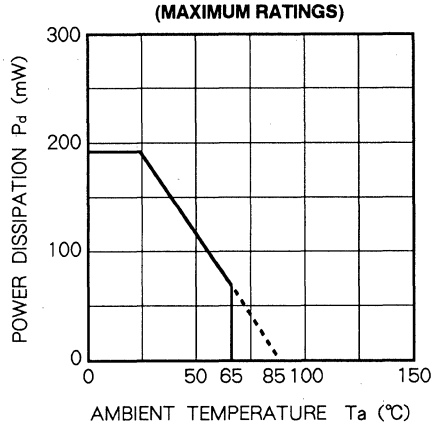
	1	2
S_1	otherwise	I CCO
S_2	otherwise	I EEO
S_3	Split supply voltage	Single supply voltage

V_{CC}, V_{EE} CONDITIONS

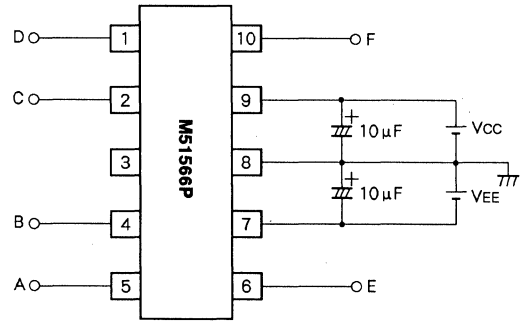
	V_{CC}(V)	V_{EE}(V)
split supply	5	5
single supply	2.5	2.5

TYPICAL CHARACTERISTICS

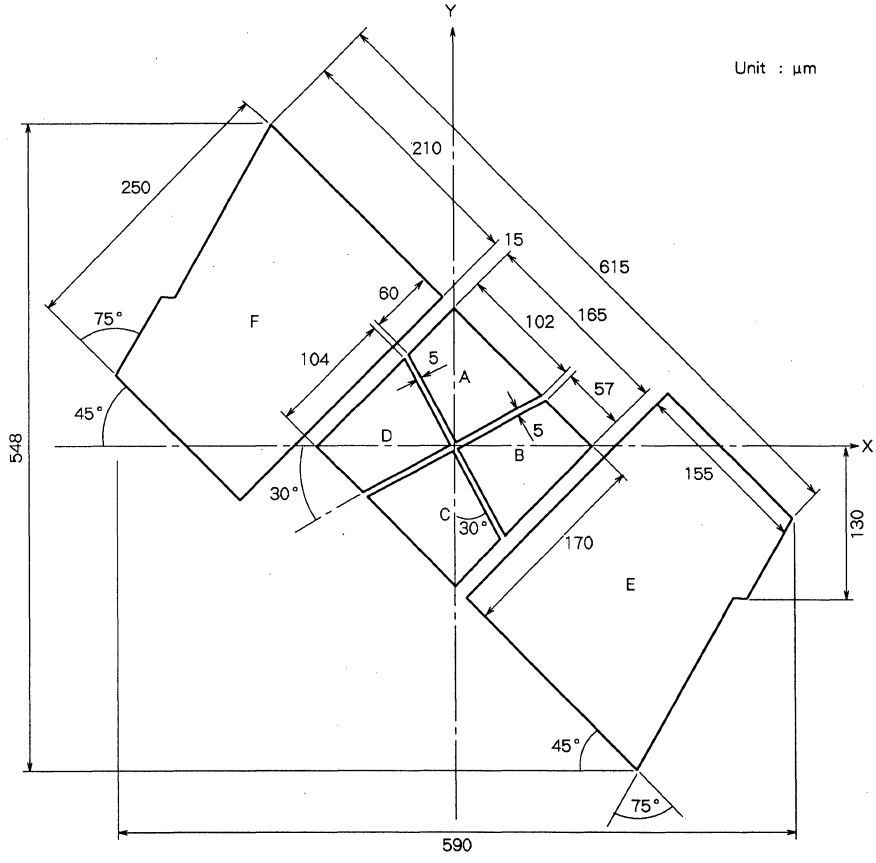
THERMAL DERATING
(MAXIMUM RATINGS)



APPLICATION EXAMPLE



PD SIZE (TYPICAL)



M51567P

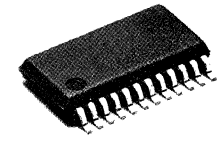
PREAMPLIFIER FOR OPTICAL PICKUP

DESCRIPTION

The M51567P is an optical pickup preamplifier for CD players. It has a built-in I-V amplifiers that convert current signals gained by photodetectors into voltage signals and HF (high frequency), FE (focus error), and TE (tracking error) amplifiers, as well as HFOK, MR, and EFM waveform shaping circuits that output in logic level.

FEATURES

- For 3 laser system
- Combination with M51564P (pickup servo control) offers capability of forming optical pickup servo system operating on 5V single power supply
- Built-in LPF for TE and FE amplifiers to remove unwanted high-frequency components
- E-F balance control pin (pin ⑲)
- Built-in hold capacitor for mirror detection
- External components : 2 chemical capacitors, 2 ceramic capacitors, 1 volume control, and 2 resistors (excluding HF com. section)
- Built-in microminiature 24-pin flat package (0.8mm lead pitch)



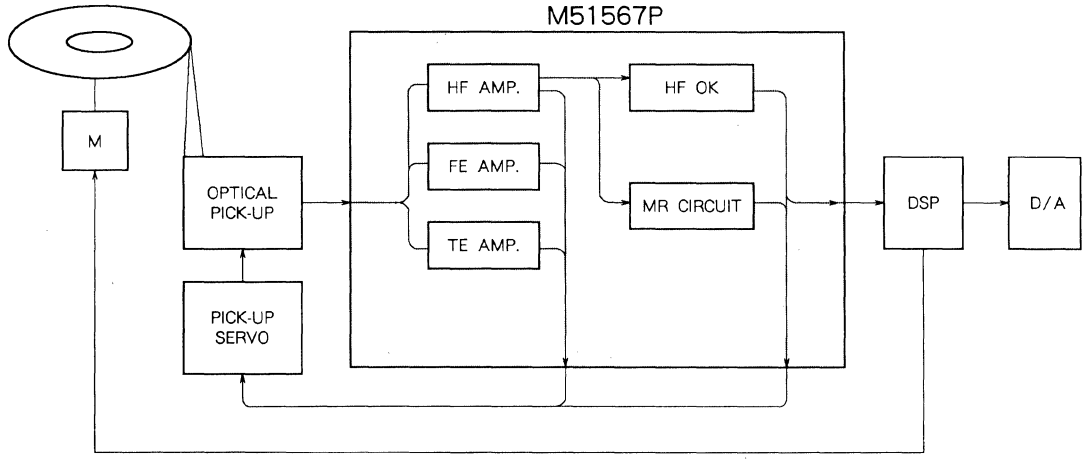
Outline 24P2Q-A

0.8mm pitch 300mil SSOP
(5.3mm × 10.1mm × 1.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 4.75~5.25V
Rated supply voltage ..... V_{CC} = 5V
Rated power dissipation 80mW

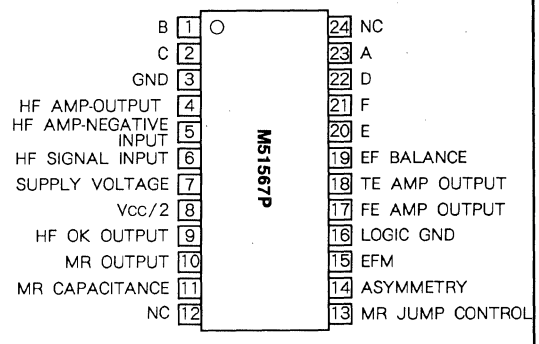
SYSTEM CONFIGURATION



M51567P

PREAMPLIFIER FOR OPTICAL PICKUP

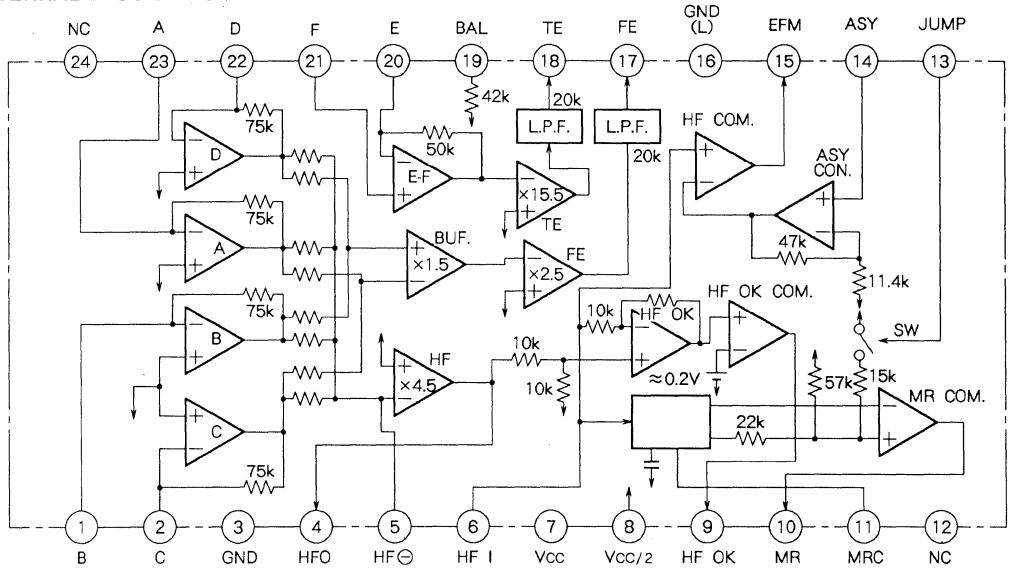
PIN CONFIGURATION



Outline 24P2Q-A

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



Units Resistance : Ω
Capacitance : F

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

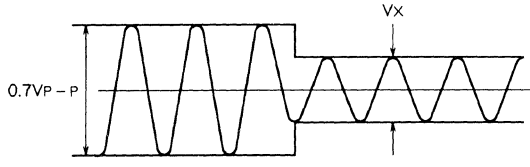
Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	10	V
I_{CC}	Circuit current	40	mA
V_I	Input voltage	0~V_{CC}	V
V_O	Output voltage	0~V_{CC}	V
P_d	Power dissipation	540	mW
T_{opr}	Operating temperature	−20~+75	℃
T_{stg}	Storage temperature	−40~+125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 5V)

Symbol	Block	Parameter	Test conditions	Limits			Unit
				Min	Typ	Max	
G_{VHF}	HF	HF output voltage	Input f=1kHz, A, B, C, D input I_i=2μ A_{P-P}	−	0.7	−	V_{P-P}
f_{HF}	HF	HF frequency	V_i = 50mVrms input, −3dB frequency	−	3	−	MHz
V_{OLA}	HF	HF Low output voltage		−	0.5	1.2	V
V_{OHA}	HF	HF High output voltage		3.2	3.8	−	V
V_{OHF}	HF	Output offset voltage		−40	0	40	mV
G_{VFE}	FE	FE output voltage	f=1kHz, A, C input I_i=2μ A_{P-P}	−	0.55	−	V_{P-P}
f_{FE}	FE	FE frequency		−	20	−	kHz
V_{LAC}	FE	FE Low output voltage	R_L = 10kΩ	−	0.5	1.2	V
V_{HAC}	FE	FE High output voltage	R_L = 10kΩ	3.6	4	−	V
V_{OFE}	FE	Output offset voltage		−50	0	50	mV
G_{VTE1}	TE	TE output voltage	f=1kHz, E input, I_i=2μ A_{P-P}	−	1.55	−	V_{P-P}
f_{TE1}	TE	TE frequency		−	20	−	kHz
V_{LE}	TE	TE Low output voltage	R_L = 10kΩ	−	0.5	1.2	V
V_{HE}	TE	TE High output voltage	R_L = 10kΩ	3.6	4	−	V
V_{OTE}	TE	Output offset voltage		−110	0	110	mV
f_{OK}	HFOK	HFOK frequency	pin⑥ input : 200mVrms Voffset = −0.2V	45	−	−	kHz
V_{HHFOK}	HFOK	High output voltage		3.5	4	−	V
V_{LHFOK}	HFOK	Low output voltage		−	0	0.4	V
V_{THHFOK}	HFOK	Threshold voltage	note 1	−	0.2	−	V
V_{HMR}	MR	High output voltage		3.5	4	−	V
V_{LMR}	MR	Low output voltage		−	0	0.4	V
V_{THMR}	MR	Output level ratio	note 2	−	0.4	−	V
V_{THMJ}	MR (JUMP)	Output level ratio	V⑬ = 2.5V Same to V_{THMR}	−	0.7	−	V
V_{HEFM}	EFM	High output voltage		3.5	4	−	V
V_{LEFM}	EFM	Low output voltage		−	0.2	0.4	V

Note 1. DC voltage is input to A. Threshold voltage is the pin④ voltage when pin⑨ voltage changes from low to high.

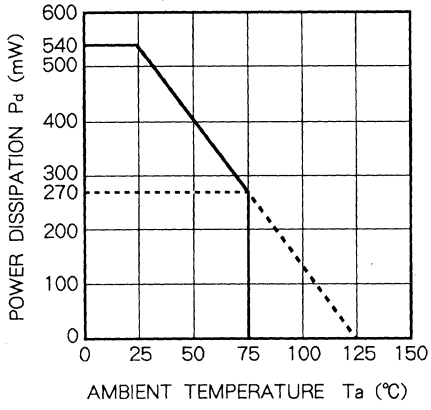
2. Following signal is input to pin⑥. Measure Vx (V_{PP}) when pin⑩ voltage becomes high.



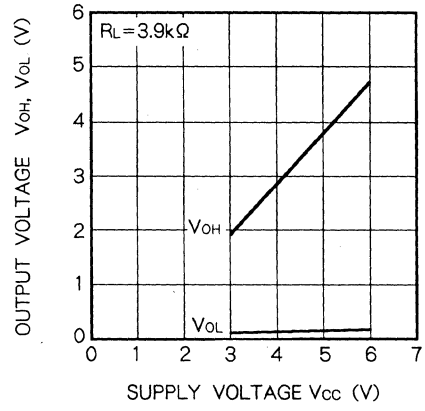
$$\text{Output level ratio} = \frac{Vx}{0.7\ (V_{P-P})}$$

TYPICAL CHARACTERISTICS

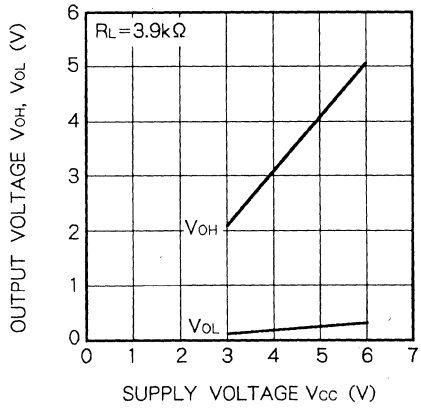
THERMAL DERATING (MAXIMUM RATING)



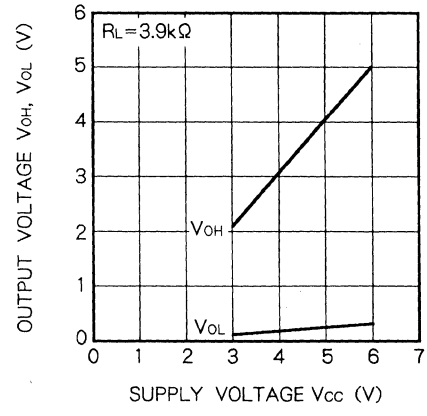
HF AMPLIFIER HIGH/LOW OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



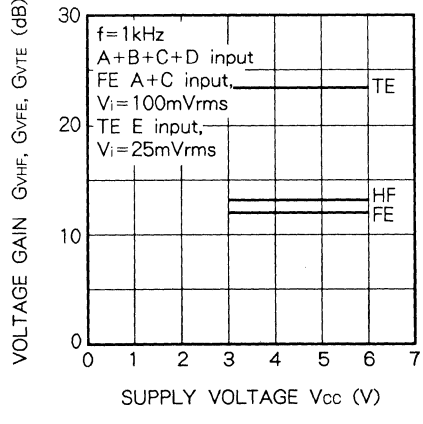
FE AMPLIFIER HIGH/LOW OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



TE AMPLIFIER HIGH/LOW OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



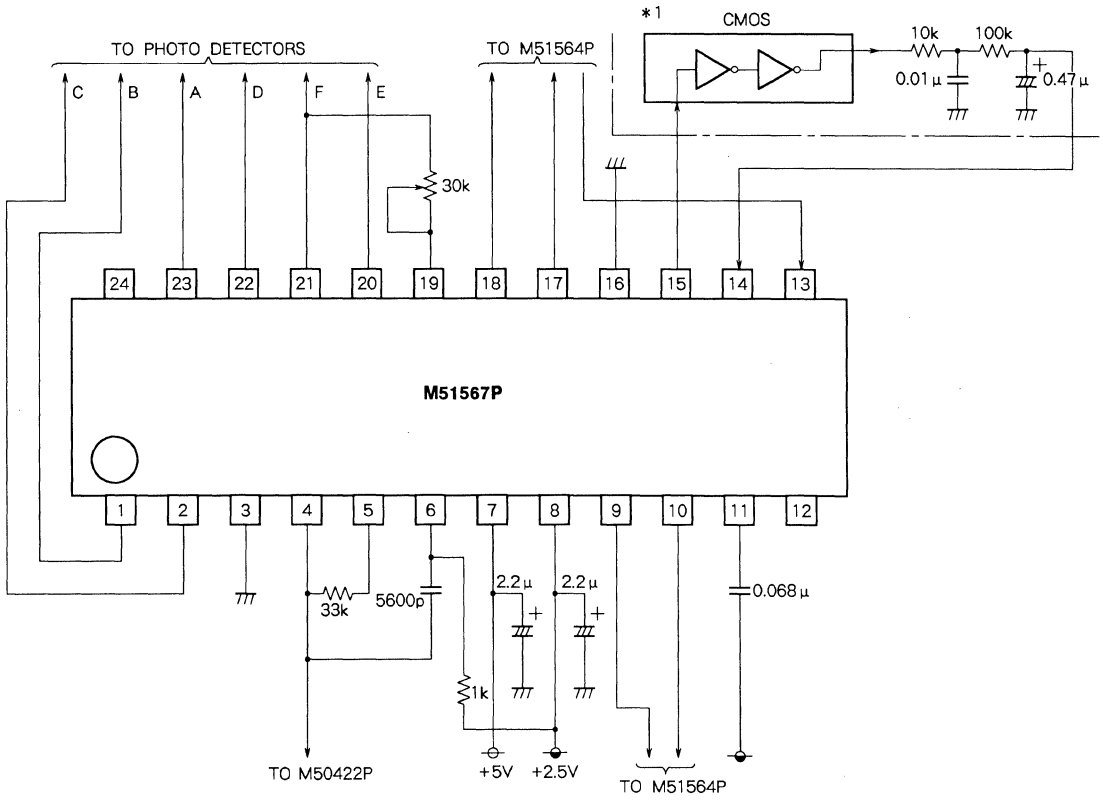
HF, FE, TE VOLTAGE GAIN VS. SUPPLY VOLTAGE



M51567P

PREAMPLIFIER FOR OPTICAL PICKUP

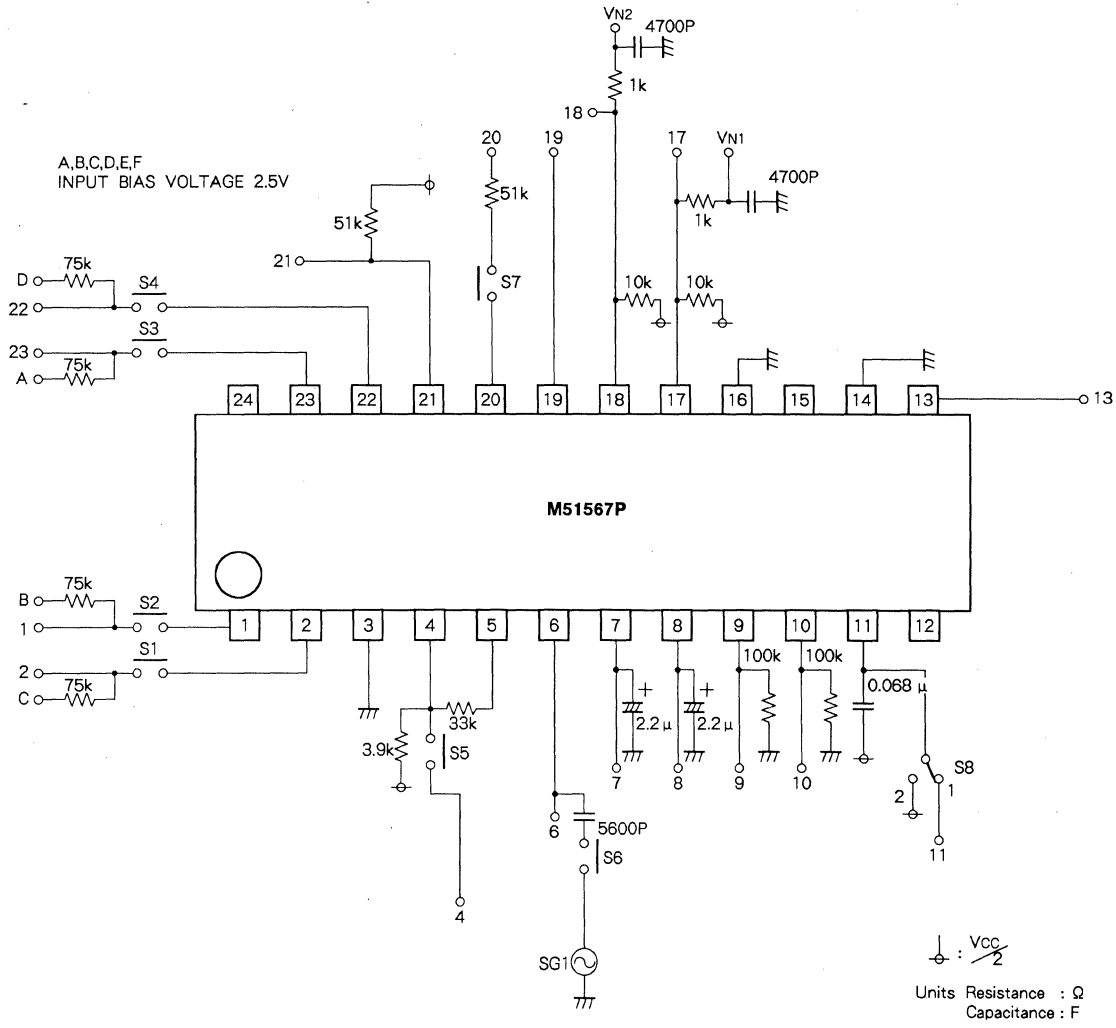
APPLICAION EXAMPLE



* 1 Not used in combination with M50422P (C-MOS digital signal processor). Pin 14 is grounded.

Units Resistance : Ω
Capacitance : F

TEST CIRCUIT



M51593FP

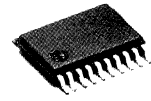
PREAMPLIFIER FOR OPTICAL PICKUP

DESCRIPTION

The M51593FP is a semiconductor integrated circuit developed as an optical pickup preamplifier for CD players. In a microminiature 20-pin flat package, it contains four I-V amplifiers that convent current signals gained by optical pickup photodetectors into voltage signals and also has FE (focus error), TE (tracking error), and RF amplifier, as well as an APC. The IC can be mounted on an optical pickup main assembly.

FEATURES

- Supports 3-laser system.
- Capable of being driven by either single or dual power supply.
- Built-in LPF for TE and FE amplifiers.(to remove unwanted high-frequency components)
- Focus error balance control pin (pin ⑮)
- Built-in housed in microminiature 20-pin flat package. (0.65mm lead pitch))
- Built-in auto power controller (APC)



Outline 20P2E-A

0.65mm pitch 225mil SSOP
(4.4mm × 6.5mm × 1.15mm)

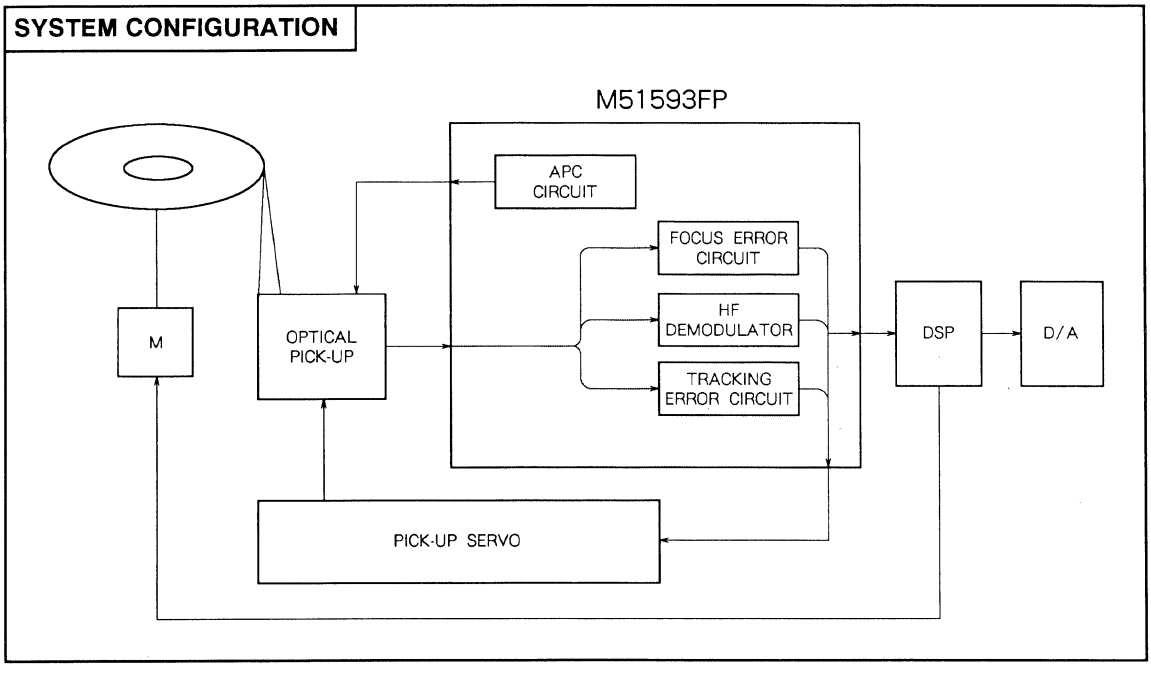
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC}, V_{EE} = ± 5V
(2 split supply voltage)
or V_{CC} = + 5V (single supply voltage)

Rated supply voltage ..... V_{CC}, V_{EE} = ± 4.75 ~ ± 5.25V
or V_{CC} = 4.75 ~ 5.25V

Rated power dissipation 60mW

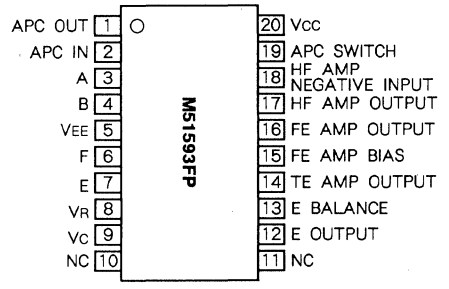
SYSTEM CONFIGURATION



M51593FP

PREAMPLIFIER FOR OPTICAL PICKUP

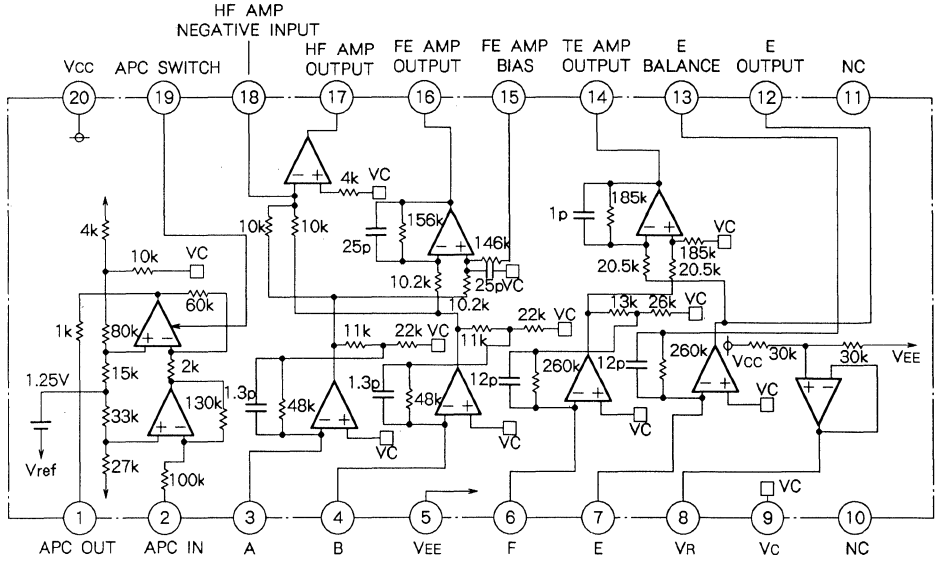
PIN CONFIGURATION



Outline 20P2E-A

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



Units Resistance : Ω
Capacitance : F

MITSUBISHI ELECTRIC

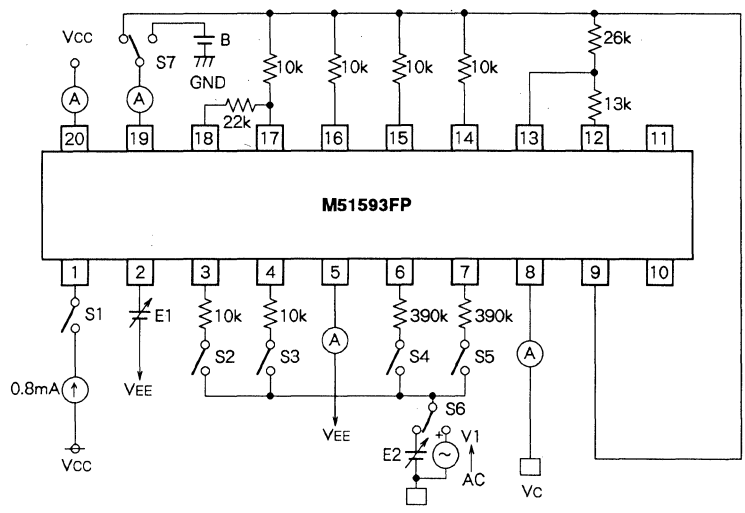
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	+ 6.5	V
V_{EE}		− 6.5	V
I_{CC}	Circuit current	40	mA
V_I	Input voltage	V_{CC} − 0.3	V
V_O	Output voltage	V_{CC} − 0.3	V
P_d	Power dissipation	360	mW/℃
T_{opr}	Operating temperature	− 20 ~ + 75	℃
T_{stg}	Storage temperature	− 40 ~ + 125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 5V, V_{EE} = − 5V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	V_{CC} = 5V, V_{EE} = − 5V V_C = 0V No signal	−	12	20	mA
I_{EE}			− 20	− 12	−	mA
V_{HF-1}	Output voltage		− 80	0	+ 80	mV
V_{HF-2}	Voltage gain	V_i = 2kHz, 40mV$_{P-P}$	28.2	31.2	34.2	dB
f_{CHF}	Frequency characteristics	3dB down	1.5	2.3	−	MHz
V_{HF-3}	Maximum output amplitude high		3.5	4.5	−	V
V_{HF-4}	Maximum output amplitude low		−	− 2.2	− 0.3	V
V_{FE-1}	Output voltage		− 120	0	+ 120	mV
V_{FE-2}	Voltage gain 1	V_i = 1kHz, 32mV$_{P-P}$	39.1	42.1	45.1	dB
V_{FE-3}	Voltage gain 2		39.1	42.1	45.1	dB
V_{FE-4}	Voltage gain balance	$V_4 = V_2 - V_3$	− 3	0	3	dB
f_{CFE}	Frequency characteristics	3dB down	28	40	52	kHz
V_{FE-5}	Maximum output amplitude high		4.2	4.5	−	V
V_{FE-6}	Maximum output amplitude low		−	− 4.5	− 2.2	V
V_{TE-1}	Output voltage		− 120	0	+ 120	mV
V_{TE-2}	Voltage gain 1	V_i = 1kHz, 300mV$_{P-P}$	16.4	19.4	22.4	dB
V_{TE-3}	Voltage gain 2		16.4	19.4	22.4	dB
V_{TE-4}	Voltage gain balance	$V_4 = V_2 - V_3$	− 3	0	3	dB
f_{CTE}	Frequency characteristics	3dB down	28	40	52	kHz
V_{TE-5}	Maximum output amplitude high		4.2	4.5	−	V
V_{TE-6}	Maximum output amplitude low		−	− 4.5	− 2.2	V
V_{APC1}	Output voltage 1		−	− 1.7	− 0.4	V
V_{APC2}	Output voltage 2		− 1.0	0.3	1.6	V
V_{APC3}	Output voltage 3		1.0	2.3	−	V
V_{APC4}	Output voltage 4		4.6	4.8	−	V
V_{APC5}	Output voltage 5	I_i = 0.8mA	−	− 3.0	2.0	V
V_{R-1}	Output voltage 1		− 100	0	100	mV

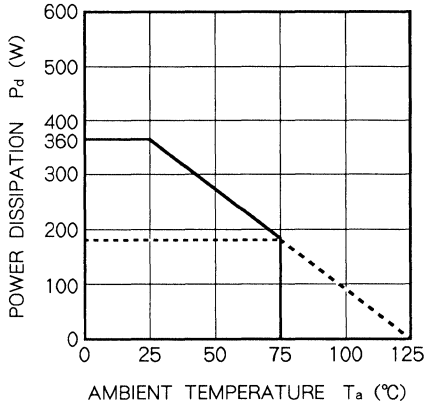
TEST CIRCUIT



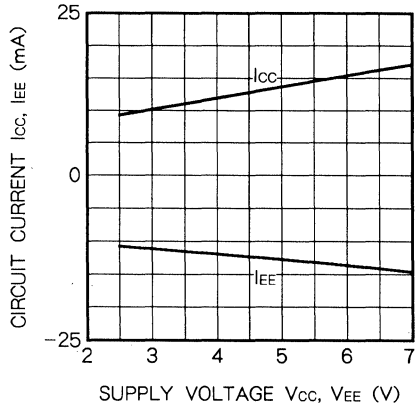
Unit Resistance : Ω

TYPICAL CHARACTERISTICS

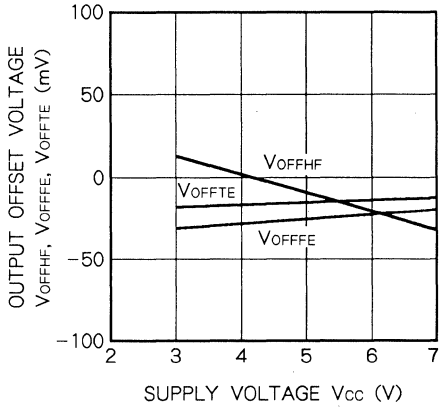
THERMAL DERATING (MAXIMUM RATING)



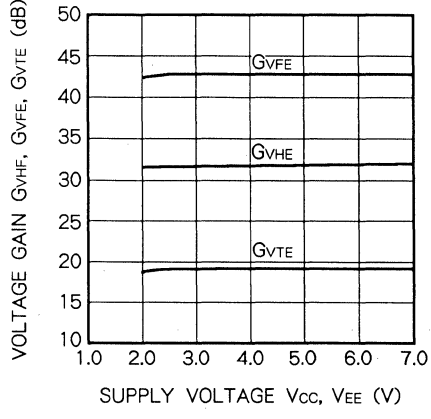
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



OUTPUT OFFSET VOLTAGE VS. SUPPLY VOLTAGE



VOLTAGE GAIN VS. SUPPLY VOLTAGE



M51595FP

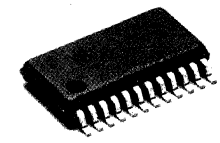
PREAMPLIFIER FOR OPTICAL PICKUP

DESCRIPTION

The M51595FP is an optical pickup preamplifier for CD players. It has a built-in I-V amplifiers that convert current signals gained by photodetectors into voltage signals and HF (high frequency), FE (focus error), and TE (tracking error) amplifiers, as well as HFOK and MR circuits that output in logic level.

FEATURES

- For 3 laser system
- Capable of being driven by either single or dual power supply
- Built-in LPF (fc = 70kHz) for TE and FE amplifiers to remove unwanted high-frequency components
- E-F balance control pin
- Built-in auto power controller (APC)
- Built-in microminiature 24-pin flat package (0.8mm lead pitch)



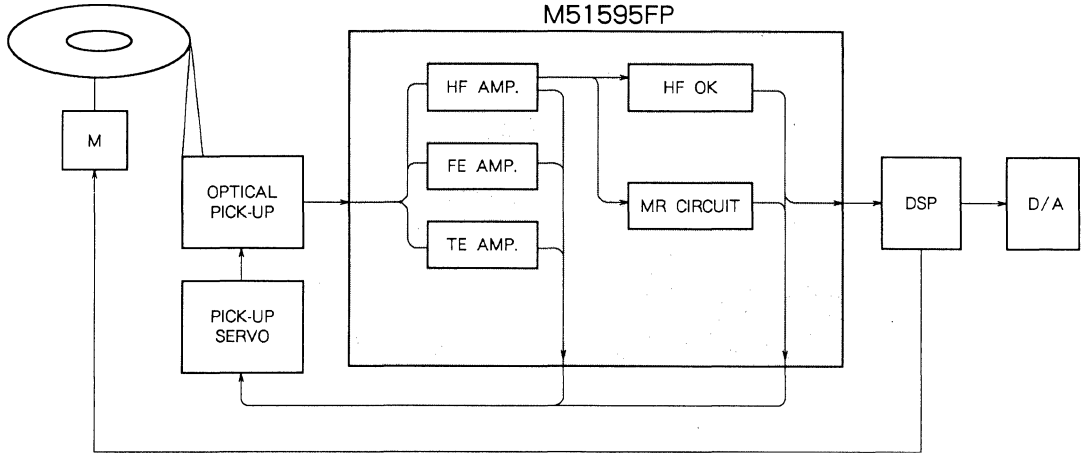
Outline 24P2Q-A

0.8mm pitch 300mil SSOP
(5.3mm × 10.1mm × 1.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC}, V_{EE} = ± 4.75 ~ ± 5.25V
Rated supply voltage ····· V_{CC}, V_{EE} = ± 5V
Rated power dissipation ····· 85mW

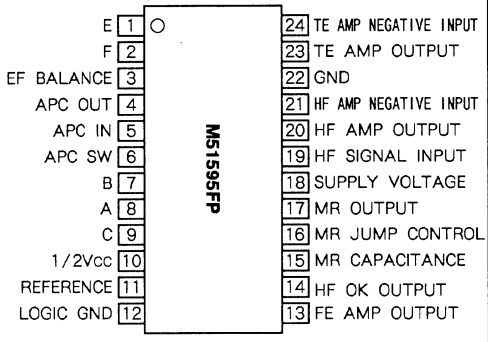
SYSTEM CONFIGURATION



M51595FP

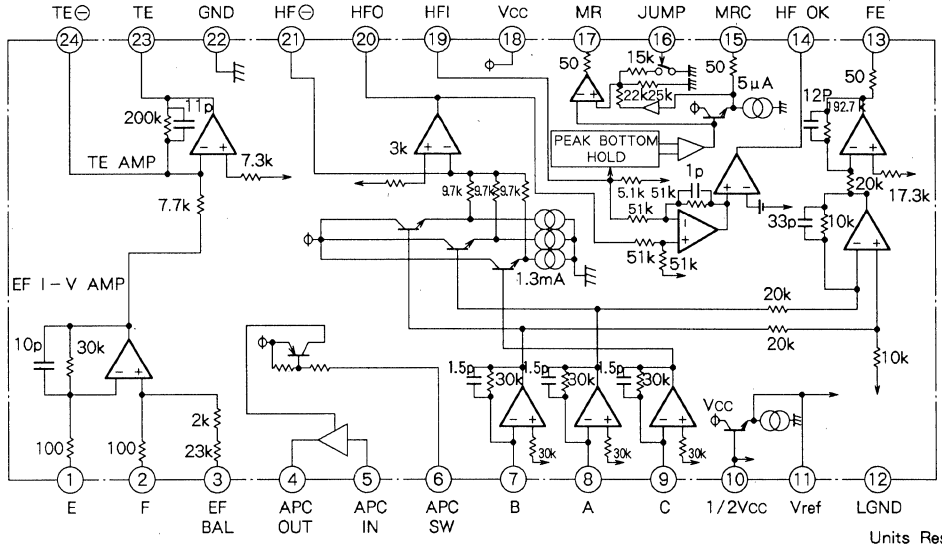
PREAMPLIFIER FOR OPTICAL PICKUP

PIN CONFIGURATION



Outline 24P2Q-A

IC INTERNAL BLOCK DIAGRAM



Units Resistance : Ω
Capacitance : F

MITSUBISHI ELECTRIC

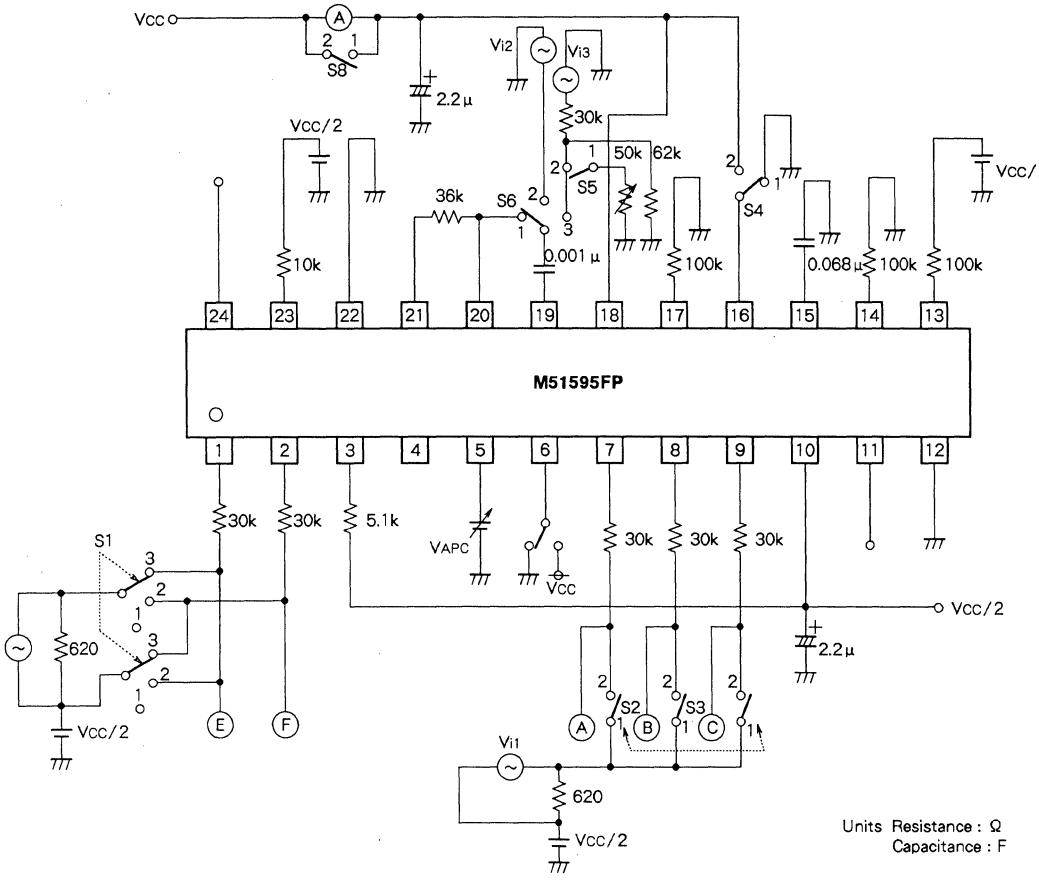
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	13	V
I_{CC}	Circuit current	60	mA
V_I	Input voltage	V_{CC} − 0.3	V
V_O	Output voltage	V_{CC} − 0.3	V
P_d	Power dissipation	540	mW
T_{opr}	Operating temperature	− 20 ~ + 75	℃
T_{stg}	Storage temperature	− 40 ~ + 125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 5V)

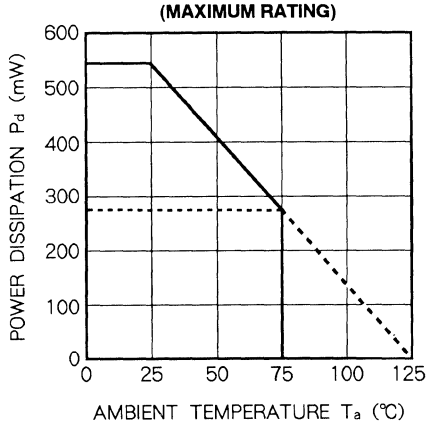
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	No signal	5	17	40	mA
G_{VHF}	HF output voltage	A~C input f = 500kHz, V_i = 100mV$_{P-P}$	0.9	1.1	1.3	V$_{P-P}$
f_{HF}	HF frequency	A~C input f = 2MHz, V_i = 100mV$_{P-P}$	− 5	− 2	−	dB
V_{HHF}	HF high output voltage		3.5	4.2	−	V
V_{OHF}	HF output offset voltage	Input open	− 120	0	+ 120	mV
G_{VFE}	FE output voltage	A input f = 500kHz, V_i = 146mV$_{P-P}$	0.5	0.7	0.9	V$_{P-P}$
V_{HAC}	HF high output voltage	R_L = 10k Ω	3.6	4.1	−	V
V_{LAC}	HF low output voltage	R_L = 10k Ω	−	0.5	1.2	V
V_{OFE}	Output offset voltage	Input open	− 50	0	+ 50	mV
G_{VTE}	TE output voltage	E input f = 1kHz V_i = 38.4mV$_{P-P}$	0.7	1.0	1.3	V$_{P-P}$
V_{HE}	TE high output voltage	RL = 10k Ω	3.6	4.1	−	V
V_{LE}	TE low output voltage	RL = 10k Ω	−	0.5	1.2	V
V_{OTE}	Output offset voltage	Input open	− 100	0	+ 100	V
V_{HOK}	HFOK high output voltage		3.5	4.1	−	V
V_{LOK}	HFOK low output voltage	No signal	−	0	0.4	V
V_{THOK}	Threshold voltage		0.26	0.37	0.48	V
V_{HMR}	MR high output voltage	No signal	3.5	4.1	−	V
V_{LMR}	MR low output voltage		−	0	0.4	V
V_{THN}	Envelope ratio (normal)	f = 500kHz (carrier)	0.26	0.36	0.46	−
V_{THJ}	Envelope ratio (jump)	f = 500kHz (carrier)	0.5	0.6	0.7	−
f_{MRf}	MR frequency	f = 500kHz (carrier) AM mod = 55 %	47	60	−	kHz
V_{APC1}	Output voltage 1	Input V_i = 190mV	4.0	−	−	V
V_{APC2}	Output voltage 2	Input V_i = 90mV	−	0.7	1.2	V
V_{APC3}	Output voltage 3	Input V_i = 160mV	−	2.2	−	V
GV_{APC}	Voltage gain		−	83	−	time

TEST CIRCUIT

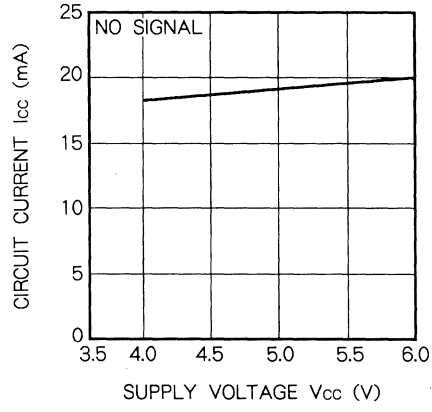


TYPICAL CHARACTERISTICS

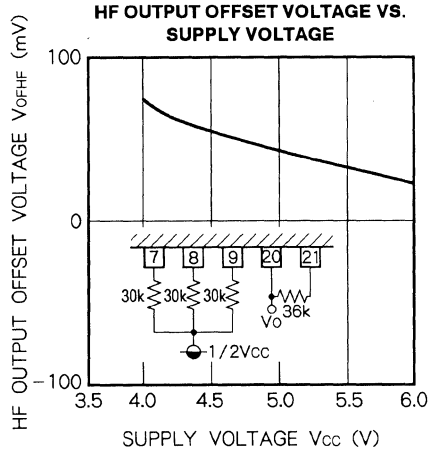
THERMAL DERATING (MAXIMUM RATING)



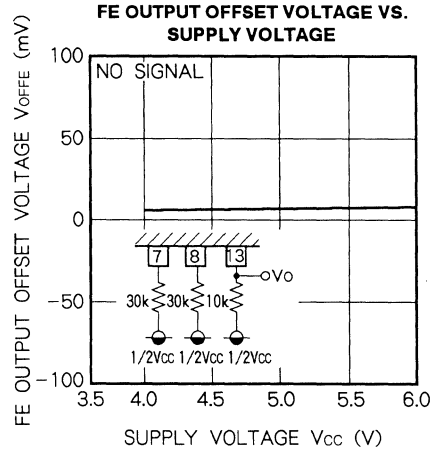
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



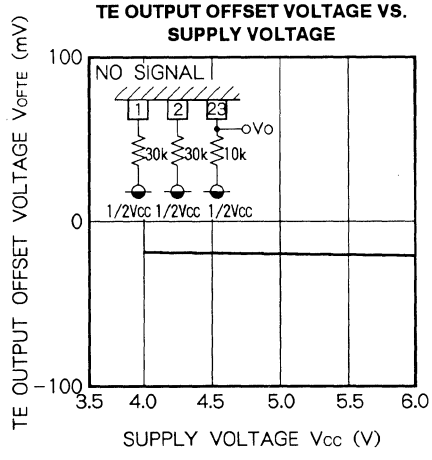
HF OUTPUT OFFSET VOLTAGE VS. SUPPLY VOLTAGE



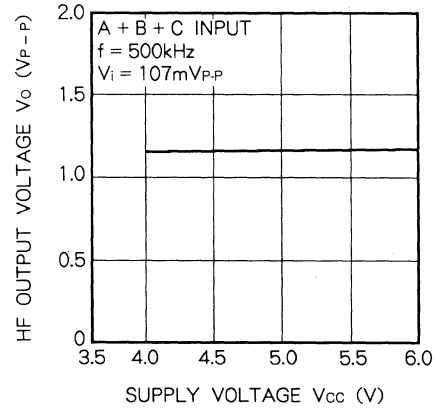
FE OUTPUT OFFSET VOLTAGE VS. SUPPLY VOLTAGE



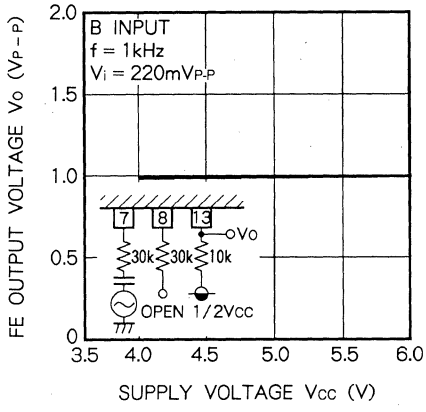
TE OUTPUT OFFSET VOLTAGE VS. SUPPLY VOLTAGE



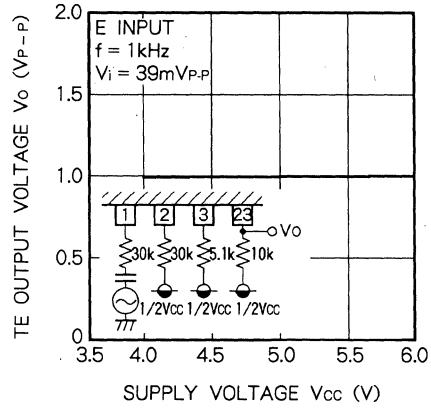
HF OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



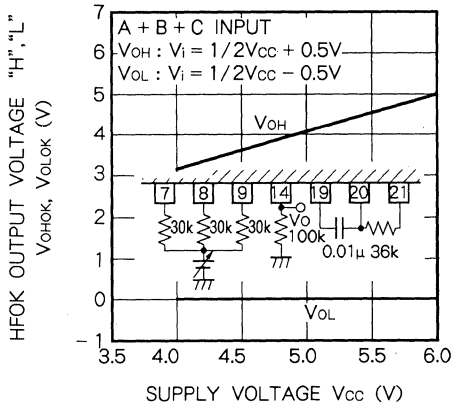
FE OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



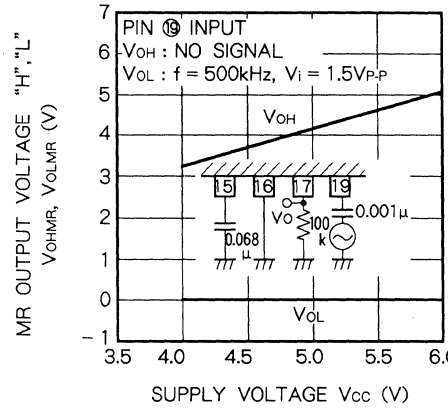
TE OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



HFOK OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



MR OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



M51598FP

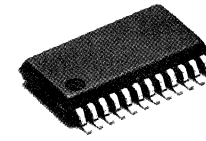
PREAMPLIFIER FOR OPTICAL PICKUP

DESCRIPTION

The M51598FP is an optical pickup preamplifier for CD players. It has a built-in I-V amplifiers that convert current signals gained by photodetectors into voltage signals and HF (high frequency) mixing, FE (focus error), and TE (tracking error) amplifiers, as well as HF signal detector and mirror detector.

FEATURES

- For 3 laser system
- Capable of being driven by either single or dual power supply
- Built-in LPF (fc = 70kHz) for TE and FE amplifiers
- E-F balance control pin (pin ③)
- Built-in focus error balance control pin (pin ⑩)
- External components·····as few as 2 chemical capacitors, 3 ceramic capacitors, 2 volume controls, and 1 resistor
- Built-in microminiature 24-pin flat package (0.8mm lead pitch)



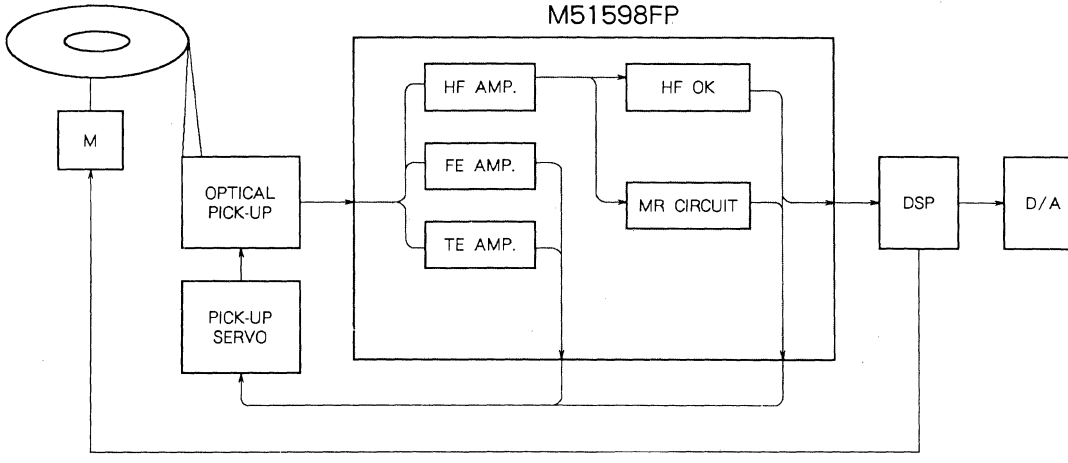
Outline 24P2Q-A

0.8mm pitch 300mil SSOP
(5.3mm × 10.1mm × 1.8mm)

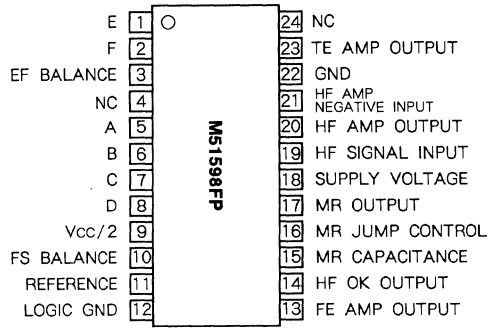
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC} = 4.75~5.25V
Rated supply voltage ····· V_{CC} = 5V
Rated power dissipation ····· 85mW

SYSTEM CONFIGURATION



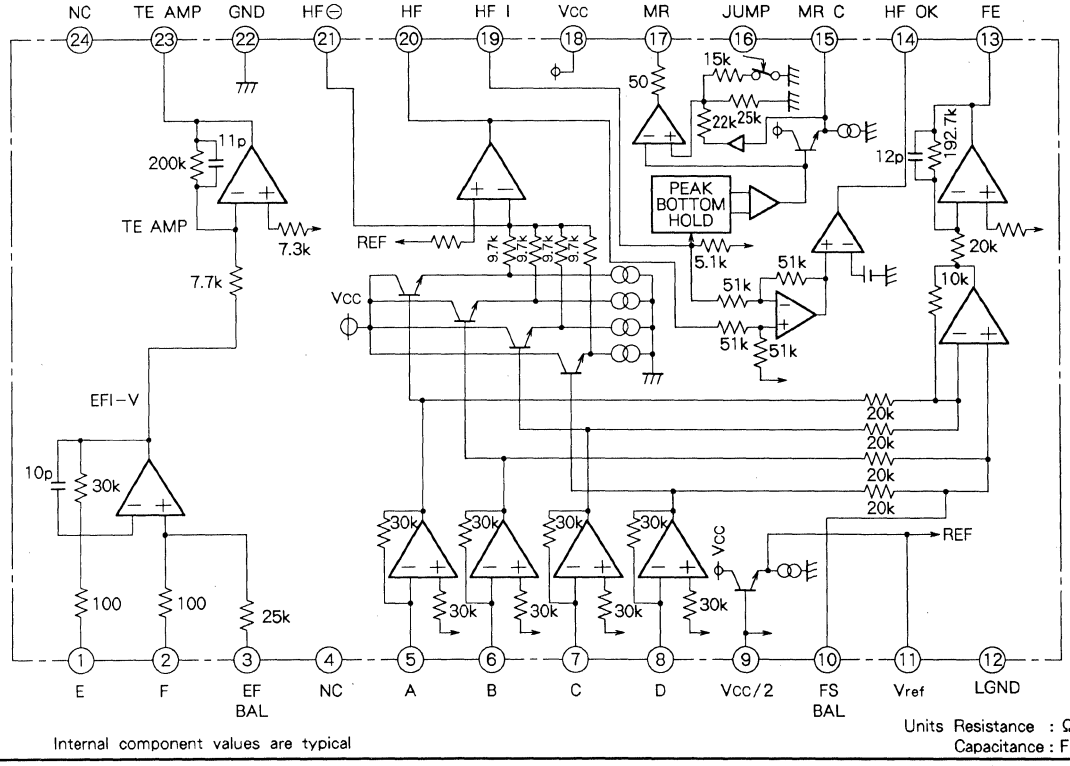
PIN CONFIGURATION



Outline 24P2Q-A

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



Internal component values are typical

Units Resistance : Ω
Capacitance : F

MITSUBISHI ELECTRIC

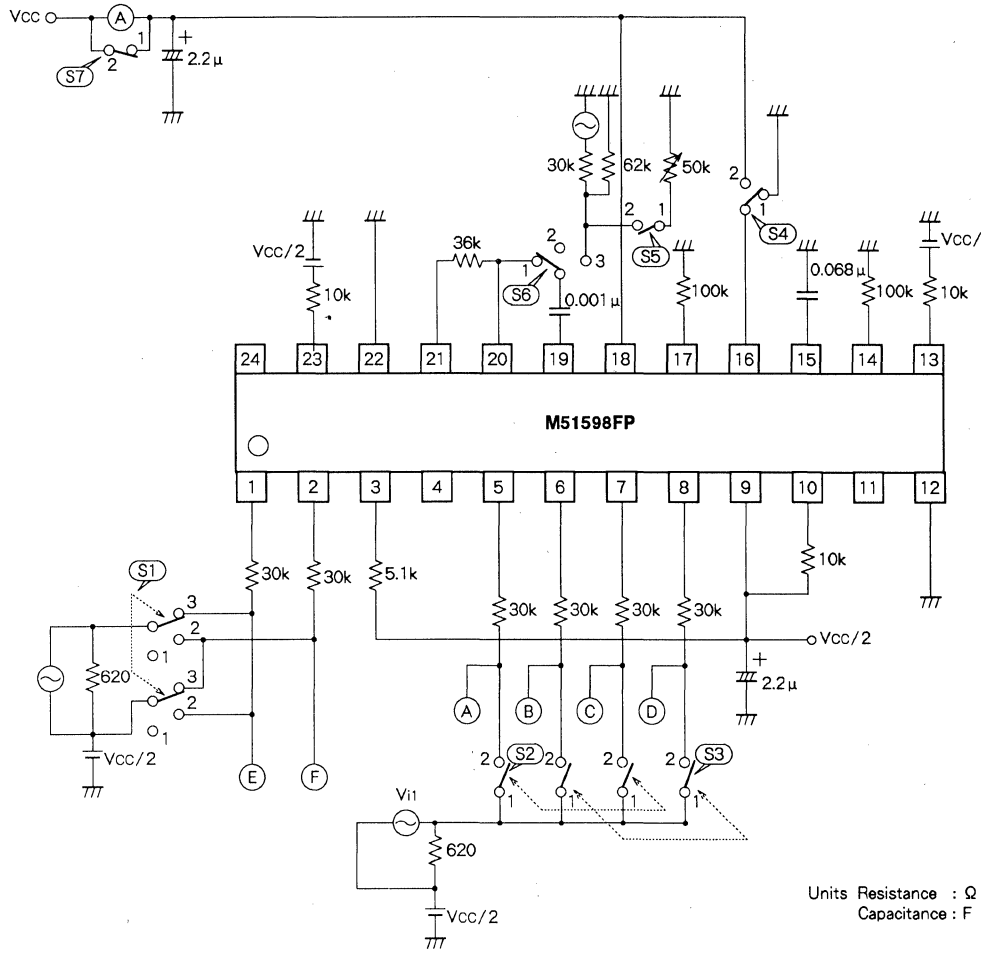
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	10	V
I_{CC}	Circuit current	40	mA
V_I	Input voltage	0~V_{CC}	V
V_O	Output voltage	0~V_{CC}	V
P_d	Power dissipation	540	mW
T_{opr}	Operating temperature	−20~+75	℃
T_{stg}	Storage temperature	−40~+125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 5V)

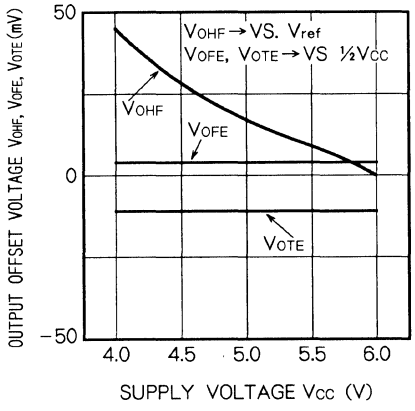
Symbol	Block	Parameter	Test coditions	Limits			Unit
				Min	Typ	Max	
I_{CC}		Circuit current	No signal	−	15	33	mA
G_{VHF}	HF	HF output voltage	A~D input f=500kHz, V_i = 78mV$_{P-P}$	0.9	1.1	1.3	V$_{P-P}$
f_{HF}	HF	HF frequency	A~D inuput f=2MHz, V_i=65mV$_{P-P}$	−5	−2	−	dB
V_{OHA}	HF	HF High output voltage		3.8	4.2	−	V
V_{OHF}	HF	HF output offset voltage	Input open	−120	0	+120	mV
G_{VFE}	FE	FE output voltage	A, C input f=500kHz, V_i=78mV$_{P-P}$	0.5	0.7	0.9	V$_{P-P}$
V_{HAC}	FE	HF High output voltage	R_L = 10kΩ	3.6	4.1	−	V
V_{LAC}	FE	HF Low output voltage	R_L = 10kΩ	−	0.5	1.2	V
V_{OFE}	FE	Output offset voltage	Input open	−50	0	+50	mV
G_{VTE}	TE	TE output voltage	E inuput f=1kHz V_i=38.4mV$_{P-P}$	0.7	1.0	1.3	V$_{P-P}$
V_{HTE}	TE	TE High output voltage	R_L=10kΩ	3.6	4.1	−	V
V_{LE}	TE	TE Low output voltage	R_L=10kΩ	−	0.5	1.2	V
V_{OTTE}	TE	Output offset voltage	Input open	−100	0	+100	mV
V_{HOK}	HFOK	HFOK High output voltage		3.5	4.1	−	V
V_{LOK}	HFOK	HFOK Low output voltge	No signal	−	0	0.4	V
V_{THK}	HFOK	Threshold voltage		0.26	0.37	0.48	V
V_{HMR}	MR	MR High output voltage	No signal	3.5	4.1	−	V
V_{LMR}	MR	MR Low output voltage		−	0	0.4	V
V_{THN}	MR	Envelope ratio (normal)	f = 500kHz (carrier)	0.26	0.36	0.46	−
V_{THJ}	MR	Envelope ratio (jump)	f = 500kHz (carrier)	0.5	0.6	0.7	−
f_{MRf}	MR	MR frequency	f = 500kHz (carrier), AM mod=55%	47	60	−	kHz

TEST CIRCUIT

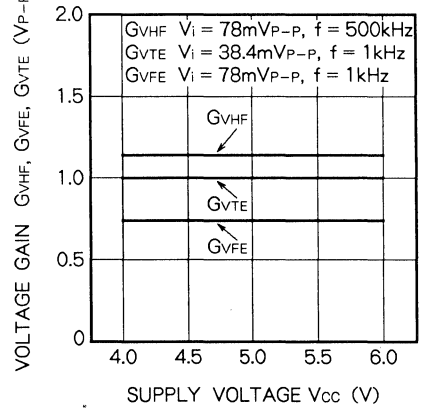


TYPICAL CHARACTERISTICS

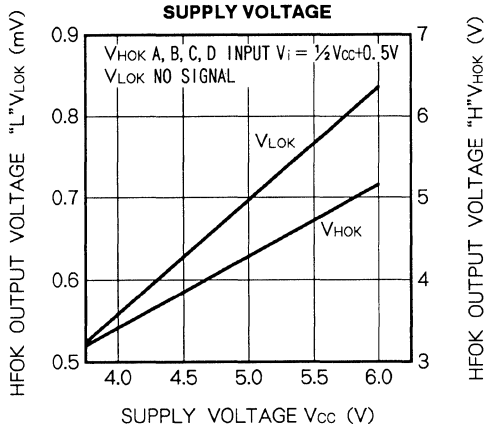
OUTPUT OFFSET VOLTAGE VS. SUPPLY VOLTAGE



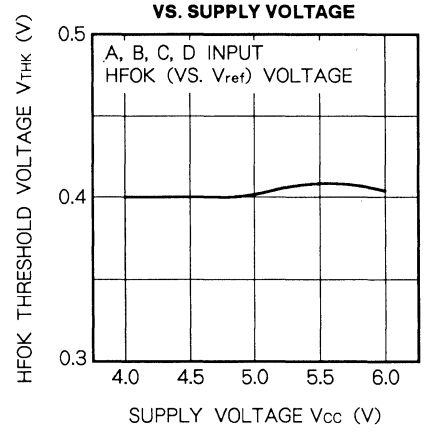
VOLTAGE GAIN VS. SUPPLY VOLTAGE



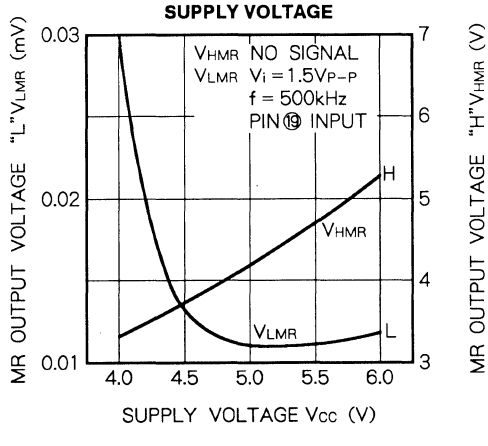
HFOK OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



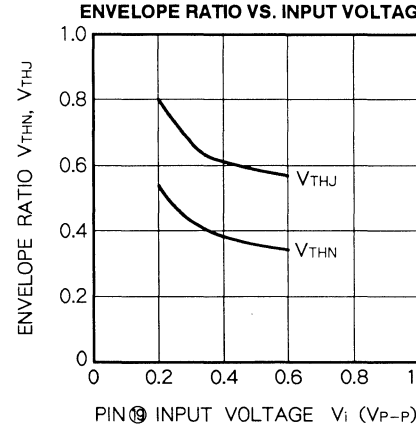
HFOK THRESHOLD VOLTAGE VS. SUPPLY VOLTAGE



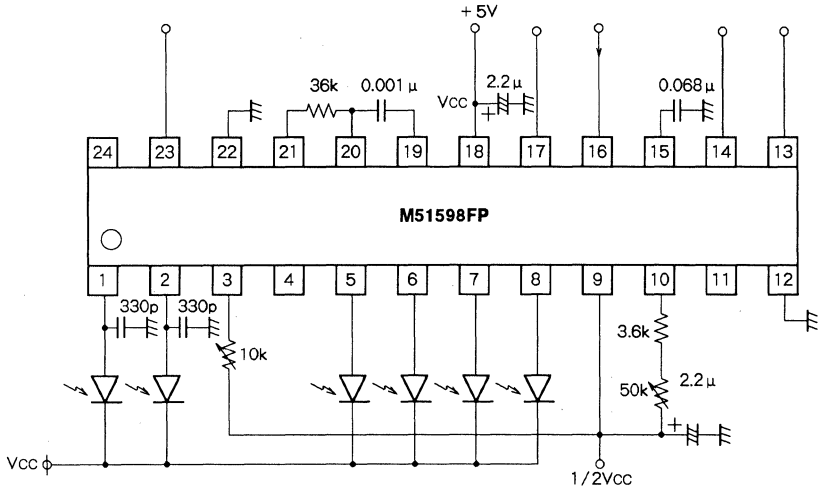
MR HIGH/LOW OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



ENVELOPE RATIO VS. INPUT VOLTAGE



APPLICATION EXAMPLE



Internal component values are typical.

Units Resistance : Ω
Capacitance : F

M51599FP

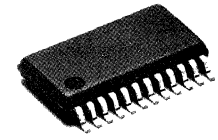
PREAMPLIFIER FOR OPTICAL PICKUP

DESCRIPTION

The M51599FP is an optical pickup preamplifier for CD players. It has a built-in I-V amplifiers that convert current signals gained by photodetectors into voltage signals and HF (high frequency), FE (focus error), and TE (tracking error) amplifiers, as well as HFOK and MR circuits that output in logic level.

FEATURES

- For 3 laser system
- High speed pickup access
  Frequency of mirror circuit : 100kHz typ
- Built-in finger-print circuit
  Variable level of mirror detector
- Built-in LPF for TE and FE amplifiers (fc = 70kHz)
- E-F balance control pin (pin ③)
- Built-in focus error balance control pin (pin ⑩)
- External components : 2 chemical capacitors, 4 ceramic capacitors, 2 volume controls, and 1 resistor
- Built-in microminiature 24-pin flat package (0.8mm lead pitch)



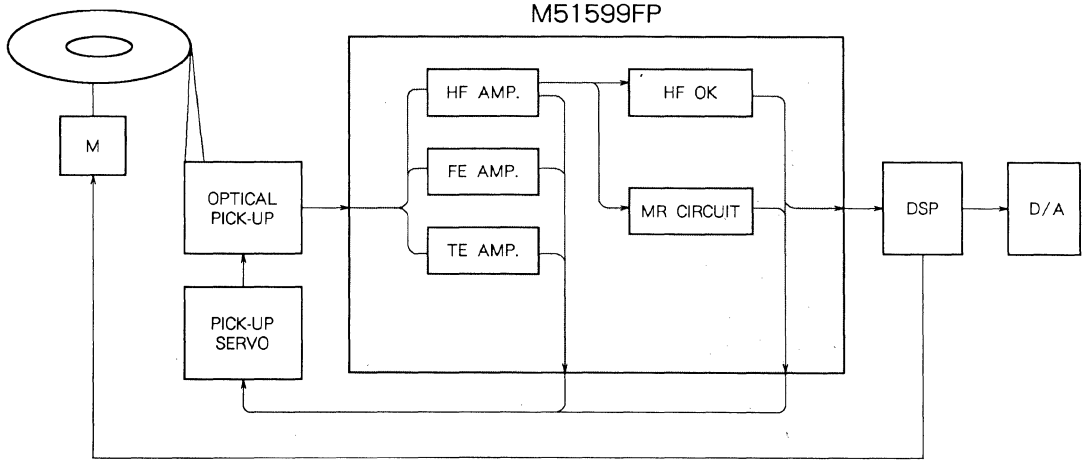
Outline 24P2Q-A

0.8mm pitch 300mil SSOP
(5.3mm × 10.1mm × 1.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC}, V_{EE} = ± 4.75~± 5.25V
Rated supply voltage ····· V_{CC}, V_{EE} = ± 5V
Rated power dissipation ····· 85mW

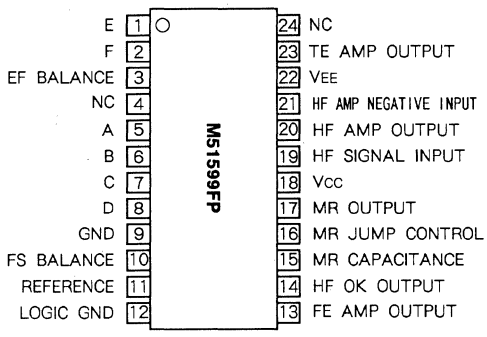
SYSTEM CONFIGURATION



M51599FP

PREAMPLIFIER FOR OPTICAL PICKUP

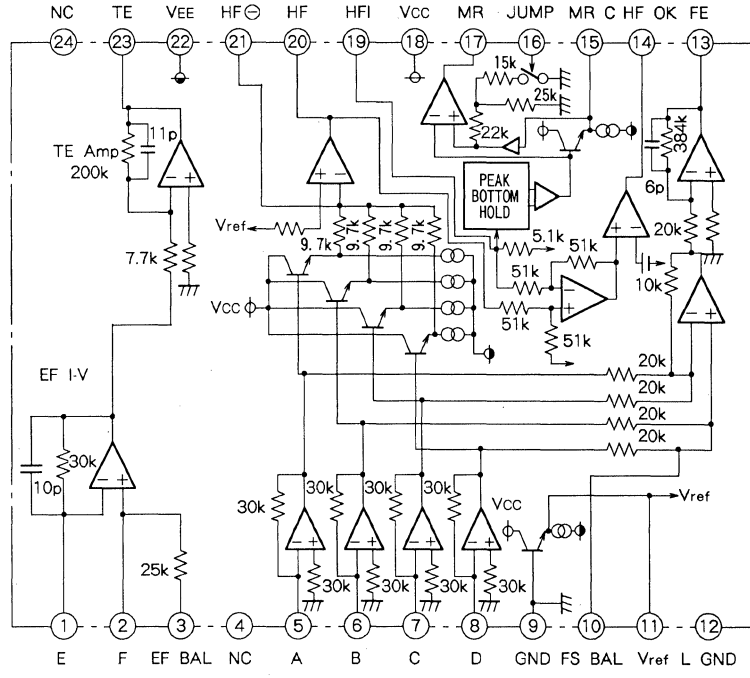
PIN CONFIGURATION



Outline 24P2Q-A

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



Units Resistance : Ω
Capacitance : F

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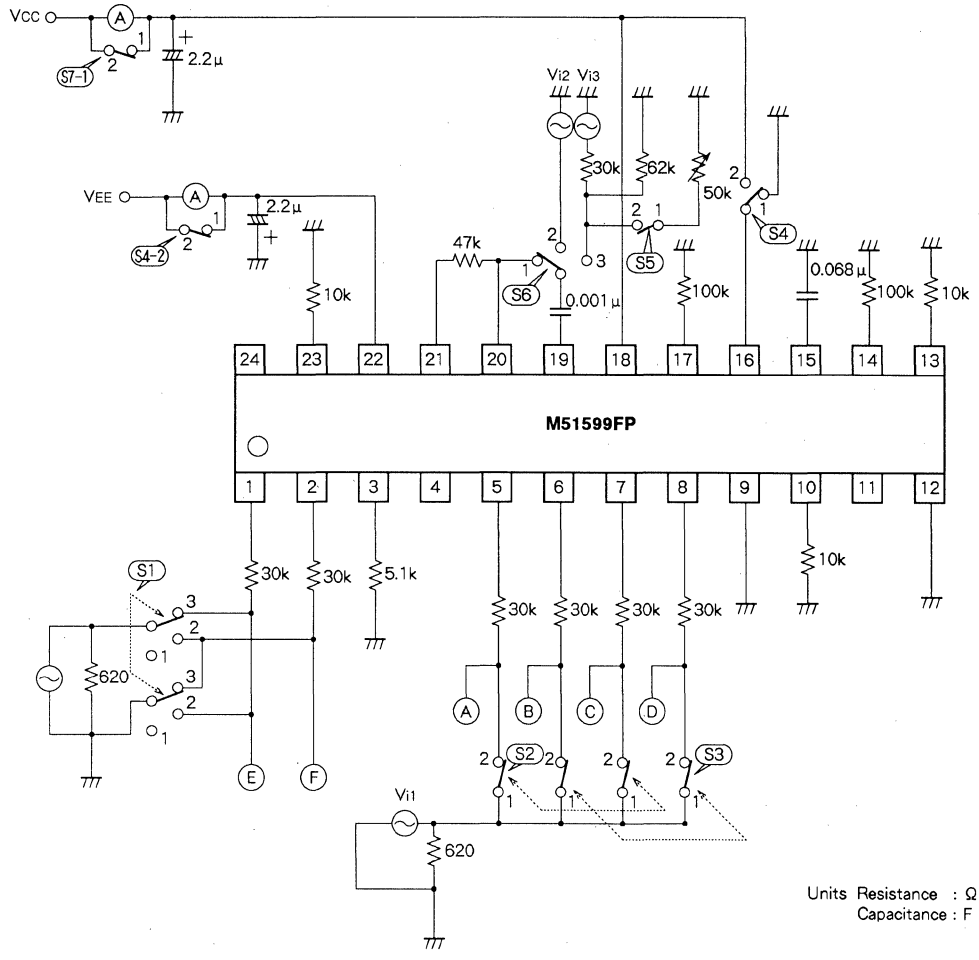
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	13	V
I_{CC}	Circuit current	± 40	mA
V_I	Input voltage	V_{EE} − 0.3~V_{CC} + 0.3	V
V_O	Output voltage	V_{EE} − 0.3~V_{CC} + 0.3	V
P_d	Power dissipation	540	mW
T_{opr}	Operating temperature	−20~+75	℃
T_{stg}	Storage temperature	−40~+125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = ± 5V)

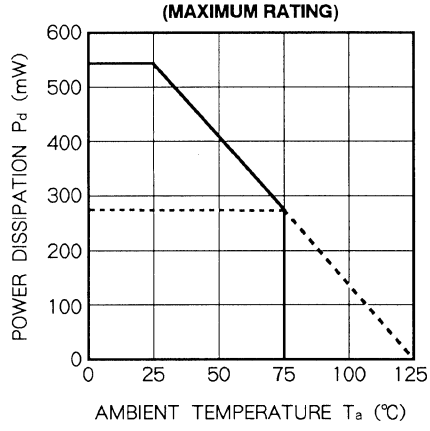
Symbol	Block	Parameter	Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC}		Circuit current	No signal	−	17	34	mA
I_{EE}				− 34	− 17	−	
G_{VHF}	HF	HF output voltage	A~D input f=500kHz, V_i = 78mV_{P-P}	1.35	1.5	1.65	V_{P-P}
f_{HF}	HF	HF frequency	A~D input f=2MHz, V_i=65mV_{P-P}	− 8	− 5	−	dB
V_{OHA}	HF	HF High output voltage		3.5	4.2	−	V
V_{OHF}	HF	HF output noise voltage	Input open	− 140	50	+ 190	mV
G_{VFE}	FE	FE output voltage	A, C input f=500kHz, V_i=78mV_{P-P}	2.1	3.0	3.9	V_{P-P}
V_{HAC}	FE	HF High output voltage	R_L = 10kΩ	3.2	4.0	−	V
V_{LAC}	FE	HF Low output voltage	R_L = 10kΩ	−	− 4.5	− 3.2	V
V_{OFE}	FE	Output offset voltage	Input open	− 195	0	+ 195	mV
G_{VTE}	TE	TE output voltage	E input f=1kHz V_i=38.4mV_{P-P}	0.7	1.0	1.3	V_{P-P}
V_{HE}	TE	TE High output voltage	R_L=10kΩ	3.2	4.0	−	V
V_{LE}	TE	TE Low output voltage	R_L=10kΩ	−	− 4.5	− 3.2	V
V_{OTE}	TE	Output offset voltage	Input open	− 160	0	+ 160	mV
V_{HOK}	HFOK	HFOK High output voltage		3.5	4.1	−	V
VLOK	HFOK	HFOK Low output voltage	No signal	−	0	0.4	V
V_{THK}	HFOK	Threshold voltage		0.26	0.37	0.48	V
V_{THOK}	MR	MR High output voltage	No signal	3.5	4.1	−	V
V_{LMR}	MR	MR Low output voltage		−	0	0.4	V
V_{THN}	MR	Envelope ratio (normal)	f = 500kHz (carrier)	0.26	0.36	0.46	−
V_{THJ}	MR	Envelope ratio (jump)	f = 500kHz (carrier)	0.5	0.6	0.7	−
f_{MRf}	MR	MR frequency	f = 500kHz (carrier), AM mod=55%	47	60	−	kHz

TEST CIRCUIT

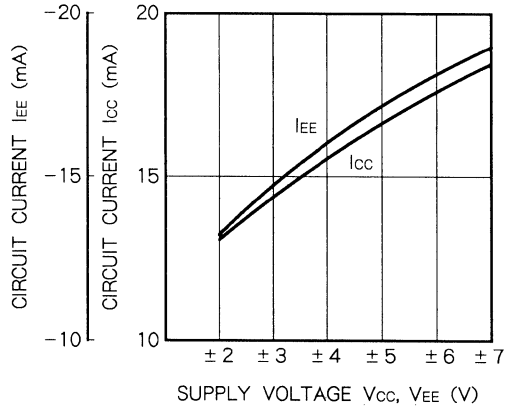


TYPICAL CHARACTERISTICS

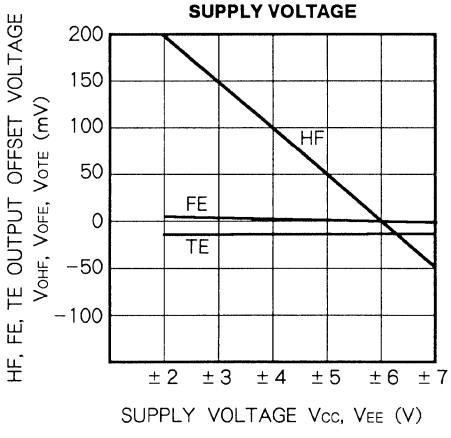
THERMAL DERATING (MAXIMUM RATING)



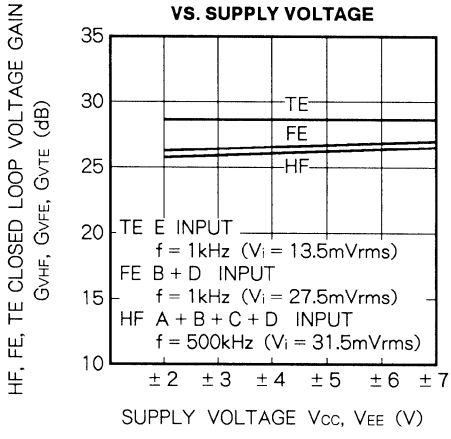
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



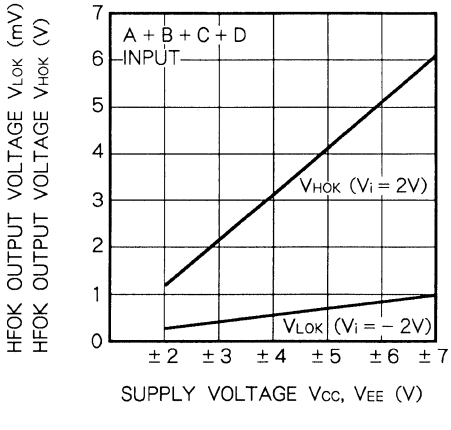
HF, FE, TE OUTPUT OFFSET VOLTAGE VS. SUPPLY VOLTAGE



HF,FE, TE CLOSED LOOP VOLTAGE GAIN VS. SUPPLY VOLTAGE



HFOK OUTPUT VOLTAGE "H" "L" VS. SUPPLY VOLTAGE



M51564P

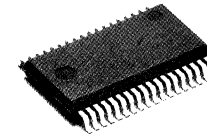
OPTICAL PICKUP SERVO CONTROL

DESCRIPTION

The M51564P is a semiconductor integrated circuit built-in the logic control, servo amplifier and switches required for servo control of CD player pickup.

FEATURES

- The amplifier, switches and logic control, all requirements for optical pickup servo control, are accomodated in a single chip
- Built-in the focus search circuit capable of auto search in both upward and downward directions
- Built-in the serial-parallel data conversion circuit, which alleviates load on the microcomputer
- Is highly applicable to a wide variety of pickup because of variable gain and frequency characteristics accomplished only by changing external parts
- Built-in the Vcc/2 generation circuit so as to permit the use of either double or single power source



Outline 36P2R-A

0.8mm pitch 450mil SSOP
(8.4mm × 15.0mm × 2.0mm)

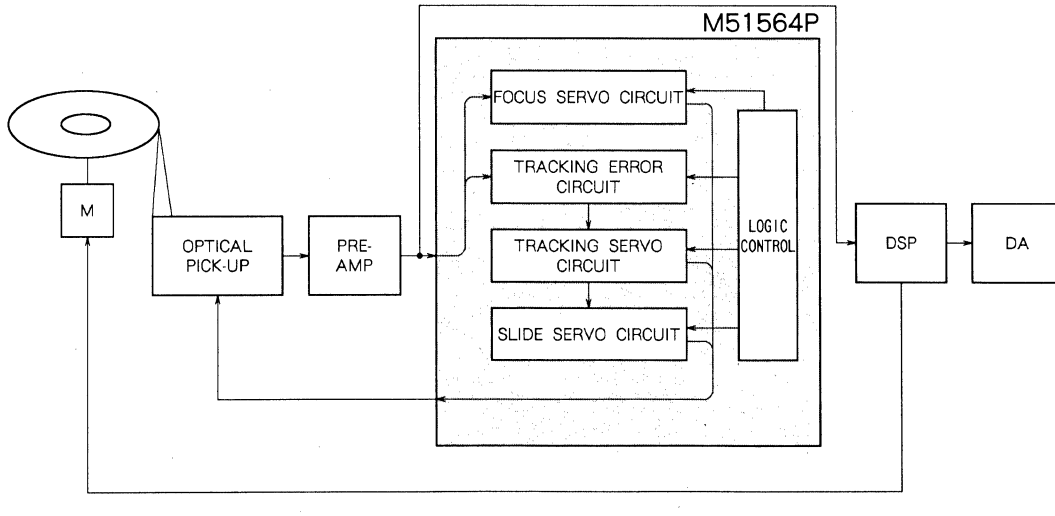
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... Vcc, VEE = ± 4.75~ ± 5.25V
or Vcc = 4.75~5.25V

Rated supply voltage
..... Vcc, VEE = ± 5V (double power source)
or Vcc = + 5V (single power source)

Rated power dissipation 70mW

SYSTEM CONFIGURATION



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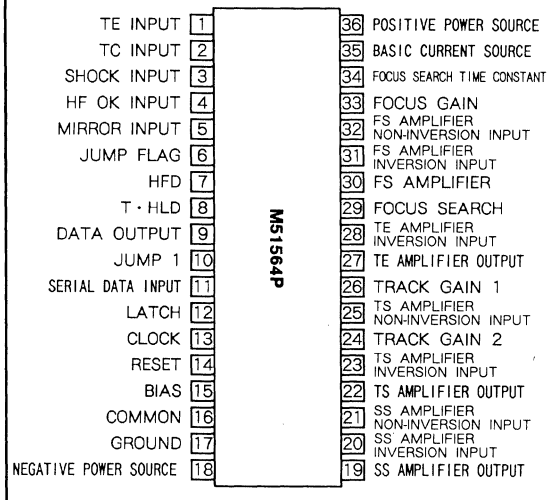
M51564P

OPTICAL PICKUP SERVO CONTROL

BUILT-IN FUNCTIONS

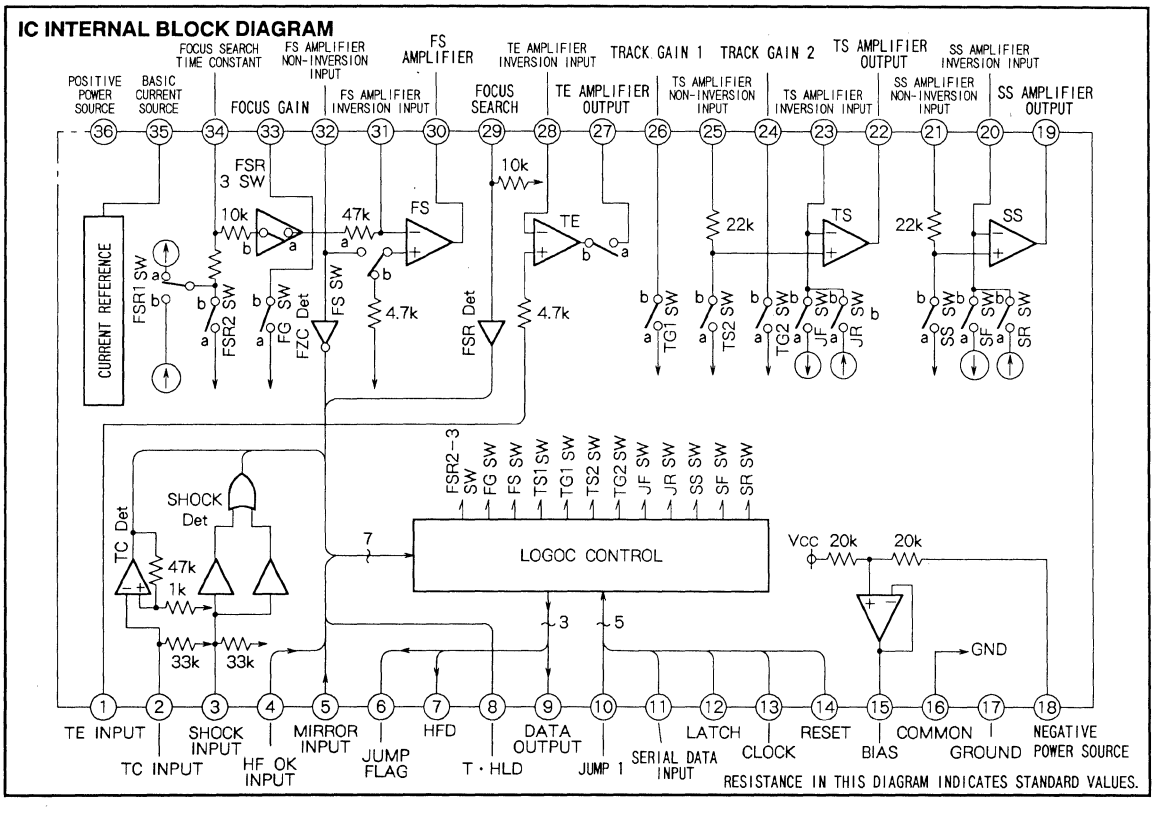
- Focus servo amplifier : FS (Focus Servo Amp.)
- Tracking error amplifier : TE (Tracking Error Amp.)
- Tracking servo amplifier : TS (Tracking Servo Amp.)
- Slide servo amplifier : SS (Slide Servo Amp.)
- Jump and brake switch circuits :
  - TS1 SW, TS2 SW (Tracking Servo Switches)
  - TG1 SW, TG2 SW (Tracking Gain Switches)
  - JF SW, JR SW (Jump Forward/Reverse Switches)
  - SS SW (Slide Servo Switches)
  - SF SW, SR SW (Slide Forward/Reverse Switches)
- Focus search circuit :
  - Focus search switch (FSR1, FSR2, FSR3, FS, FG)
  - Focus search switch (FZR Det)
  - Focus zero cross detector (FZC Det)
- Track cross detector : TC Det (Track Cross Detector)
- Shock detector : Shock Det (Shock Detector)
- Logic controller :
  - Serial→parallel data conversion circuit
  - Jump, brake and focus search controls
- Vcc/2 generation circuit

PIN CONFIGURATION



Outline 36P2R-A

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Block	I/O	Function
①	TE IN	Pre-amplifier input	I	Input terminal for tracking error signals
②	TC IN	↑	I	Input terminals for track cross signals
③	SHOCK IN	↑	I	Input terminals into the shock detection circuit
④	HF OK	↑	I	Input terminals for HF OK signals
⑤	MR	↑	I	Input terminals for disc mirror surface detection signals
⑥	Jump Flag	Output to the pre-amplifier	O	Outputs "H" in jump modes such as TS OFF, JF JR, and BRAKE
⑦	$\overline{HFD}$		O	HFD="H"when MR input="H"and when track servo loop is OFF(TS OFF, JF, and JR)
⑧	T・HLD TS1SW	Track servo	I	Direct control terminal for TS1SW When T-HLD = "H", TS1SW = "b" ; When T-HLD = "L", controller command prevails
⑨	DATA OUT	Microcomputer I/O	O	Interior condition output corresponding to microcomputer commands
⑩	$\overline{JP1}$	↑	I	Control signal for track jump brake pulses. Normally "H"
⑪	MSD	↑	I	Microcomputer serial data Transfers serial data from microcomputer to servo IC. LSB first. 8-bit data
⑫	$\overline{MLA}$	↑	I	Latches serial data from microcomputer to servo IC. Transfers data when this falls
⑬	MCK	↑	I	Clock for serial data transfer from microcomputer to servo IC. Uptakes data at the rising edge
⑭	$\overline{ACLR}$	↑	I	All cleared. Resets all internal registers and flip-flops with signal "L"
⑮	Bias	Power source	O	When power source is single, this outputs Vcc/2 bias power
⑯	COM	↑	I	COMMON terminal. Connected to GND. when positive and negative power is supplied, and to BIAS when power source is single
⑰	GND	↑	I	GND
⑱	V_{EE}	↑	I	Negative power terminal. Connected to GND when power source is single
⑲	SS OUT	Slide servo	O	Operation amplifier SS output
⑳	SS⊖	↑	I	Operation amplifier SS inversion input
㉑	SS⊕	↑	I	Operation amplifier SS non-inversion input
㉒	TS OUT	Track servo	O	Operation amplifier TS output
㉓	TS⊖	↑	I	Operation amplifier TS non-inversion input
㉔	TG2	↑	–	Output of track/gain selector switch TG2. Made open or takes common level
㉕	TS⊕	↑	I	Operation amplifier TS non-inversion input
㉖	TG1	↑	–	Output of track/gain selector switch TG1. Made open or takes common level
㉗	TE OUT	↑	O	Operation amplifier TE output
㉘	TE⊖	↑	I	Operation amplifier TE inversion output
㉙	FSR IN	Focus servo	I	Input into focus search voltage level detector
㉚	FS OUT	↑	O	Operation amplifier FS output
㉛	FS⊖	↑	I	Operation amplifier FS inversion output
㉜	FS⊕	↑	I	Operation amplifier FS non-inversion output
㉝	FG	↑	–	Output of focus/gain selector switch FG. Made open or takes common level
㉞	C・FSR	↑	–	Connects the capacitor determining the time constant of focus search waveform
㉟	I-ref	Constant-current source	I	Terminal to connect current setting resistors of reference current source
㊱	Vcc	Power source	I	Terminal for positive power source

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	+ 6.5	V
V_{EE}		− 6.5	V
V_I	Input voltage Absolute value	| Applied supply voltage | +0.3	V
V_O	Output voltage Absolute value	| Applied supply voltage | +0.3	V
P_d	Power dissipation	560	mW
T_{opr}	Operating temperature	−20～+75	℃
T_{stg}	Storage temperature	−40～+125	℃

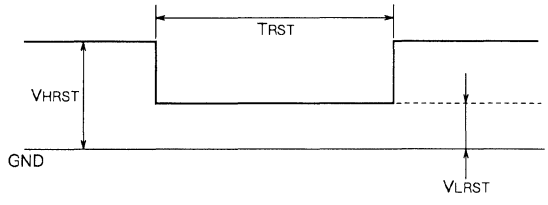
RECOMMENDED OPERATING CONDITIONS (Ta = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage	(±) and single power sources	+ 4.75	+ 5.0	+ 5.25	V
V_{EE}		(±) power source	− 5.25	− 5.0	− 4.75	V
V_{IH}	Input voltage ("H" level)		2.5	–	Vcc	V
V_{IL}	Input voltage ("L" level)		0	–	0.4	V

ELECTRICAL CHARACTERISTICS (V_{CC} = + 5V, V_{EE} = − 5V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	To be reset	−	14	32	mA
I_{EE}	Circuit current	To be reset	−28	−12	−	mA
G_{FS}	FS closed loop voltage gain	f=1kHz, V_i = −10dBm	20	22	24	dB
A_{TTFS}	FS SW attenuation	f=1kHz, V_i = 0dBm	−	−35	−25	dB
R_{ONFG}	FG SW ON resistance	f=1kHz, V_i = 0dBm	−	100	300	Ω
V_{HFS}	FS output voltage H	V_i = 1V, R_L = 220 Ω	2.2	4	−	V
V_{LFS}	FS output voltage L	V_i = −1V, R_L = 220 Ω	−	−4	−2.2	V
V_{FSR+}	FSR reference voltage (+)		0.40	0.45	0.50	V
V_{FSR-}	FSR reference voltage (−)		−0.54	−0.49	−0.44	V
G_{TE}	TE closed loop voltage gain	f=1kHz, V_i = −10dBm	6.8	8.8	10.8	dB
G_{TS}	TS closed loop voltage gain	f=1kHz, V_i = −10dBm	7.8	9.8	11.8	dB
A_{TTTS1}	TS SW attenuation	f=1kHz, V_i = 0dBm	−	−50	−30	dB
A_{TTTS2}			−	−50	−30	dB
R_{ONT1}	TG1SW ON resistance	f=1kHz, V_i = 0dBm	−	50	300	Ω
R_{ONT2}	TG2SW ON resistance	f=1kHz, V_i = 0dBm	−	50	300	Ω
V_{HTS}	TS output voltag H	V_i = 2V, R_L = 220 Ω	2.2	4	−	V
V_{LTS}	TS output voltag L	V_i = −2V, R_L = 220 Ω	−	−4	−2.2	V
G_{SS}	SS closed loop voltage gain	f=1kHz, V_i = −10dBm	11.5	13.5	15.5	dB
A_{TTSS}	SS SW attenuation	f=1kHz, V_i = 0dBm	−	−54	−30	dB
V_{HSS}	SS output voltage H	V_i = 2V, R_L = 220 Ω	2.2	4	−	V
V_{LSS}	SS output voltage L	V_i = −2V, R_L = 220 Ω	−	−4	−2.2	V
V_{SH+}	SHOCK DET reference voltage (+)		0.3	0.4	0.5	V
V_{SH-}	SHOCK DET reference voltage (−)		−0.47	−0.37	−0.27	V
V_{JF}	JF output voltage		1.1	1.4	1.7	V
V_{JR}	JR output voltage		−1.7	−1.4	−1.1	V
V_{SF}	SF output voltage		2.2	2.8	3.4	V
V_{SR}	SR output voltage		−3.4	−2.8	−2.2	V
V_{FCU+}	FZC⊕search reference voltage		0.26	0.29	0.32	V
V_{FCU-}			−0.1	0	0.1	V
V_{FCD+}	FZC⊖search reference voltage		−0.1	0	0.1	V
V_{FCD-}			−0.31	−0.28	−0.25	V
V_{TC+}	TC reference voltage		0	0.1	0.2	V
V_{TC-}			−0.2	−0.1	0	V
V_{HTE}	TE output voltage H	V_i = 2V, R_L = 47k Ω	3.5	4.2	−	V
V_{LTE}	TE output voltage L	V_i = −2V, R_L = 47k Ω	−	−4.2	−3.5	V
V_{OSFS}	FS output offset voltage	Up search	70	130	190	mV
V_{OSTE}	TE output offset voltage		−35	−10	15	mV
V_{OSTS}	TS output offset voltage		−5	20	45	mV
V_{OSSS}	SS output offset voltage		−30	0	30	mV
I_{FSRU}	FSR output current		21	29	37	μA
I_{FSRD}			−32	−25	−8	μA

Note 1. Before taking measurements, whichever of the above, input the reset pulse as shown in the diagram below into terminal ⑭ $\overline{ACLR}$ after turning power on.



T_{RST} : 1 μs min
V_{HRST} : 2.5V min
V_{LRST} : 0.4V max

FUNCTION DESCRIPTION

Setting the built-in constant-current source current level

Focus search (FSR), tracking servo (TS), and slide motor servo (SS)

The current level of the constant-current source for FSR, TS and SS can be set via resistor Rx connected across terminal ㉟~Vcc.

Let the absolute values of the constant-current source current levels for FSR, TS, SS be IFSR, ITS, ISS, respectively. Then

$$I_{FSR} \simeq \frac{1}{8} \cdot \frac{V_{CC} - V_{㉟}}{Rx}$$

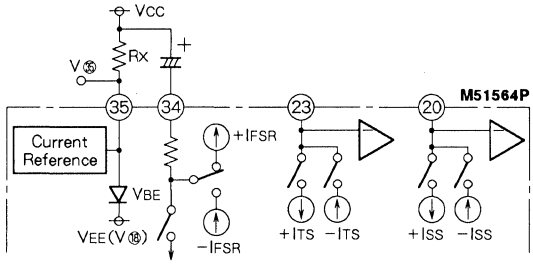
$$I_{TS} \simeq \frac{1}{8} \cdot \frac{V_{CC} - V_{㉟}}{Rx}$$

$$I_{SS} \simeq \frac{1}{4} \cdot \frac{V_{CC} - V_{㉟}}{Rx}$$

where V㉟ is voltage at terminal ㉟. Let voltage at terminal ⑱ (VEE) be V⑱. Then V㉟ can be obtained

V㉟ = V⑱ + VBE (VBE ≃ 0.7V as standard)

Constant-current source block diagram



FSR detector

Current is input from FS OUT (terminal ㉚ output) via resistors or the driver and resistors into FSR IN (terminal ㉙ input). The following are performed during focus search :

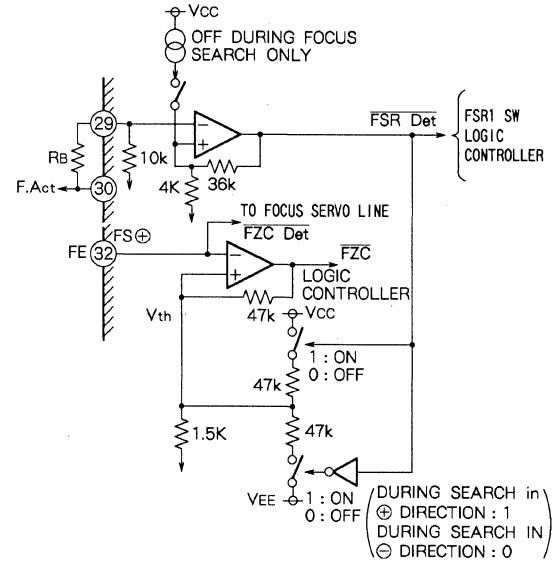
- Automatic switching of focus search direction
- Automatic switching of FZC detection polarity

Focus search always begins from the ⊕ side. The polarity of focus search voltage (⊕ or ⊖) is switched by FSR DET signal via FR1 SW.

INPUT	OUTPUT		
FSR IN level VIN	FSR Det	FSR1 SW mode	FZC Vth level
VIN < Vth	0	Side b : ⊖search voltage developed	Rise 0 / Fall −0.30(V)
VIN > Vth	1	Side a : ⊕search voltage developed	Rise 0.30 / Fall 0(V)

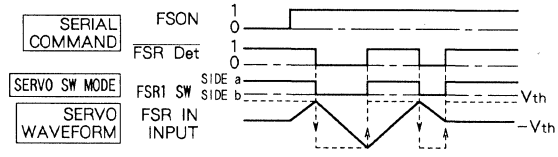
FZC Vth level is the value when the power source is ±5V.

Equivalent circuit

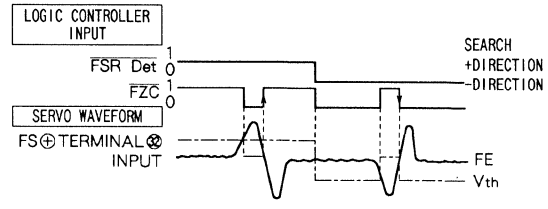


Unit Resistance : Ω

FSR det operation timing chart



FZC Operation timing chart



MITSUBISHI ELECTRIC

Setting the focus search voltage and jump pulse and slide feed voltages

(power source : ± 5V ; RX = 47k Ω)

Setting the focus search voltage

Setting the FSR waveform maximum level V_{FS} (determination of R_B)

$$V_{FS} = \frac{R_A + R_B}{R_A} V_{FSR} \cdots\cdots\cdots\cdots (1)$$

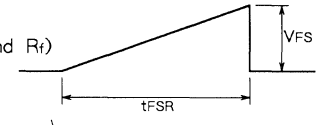
$$\therefore R_B = R_A \left(\frac{V_{FS}}{V_{FSR}} - 1\right)$$

$$= 10 \times 10^3 \left(\frac{V_{FS}}{0.5} - 1\right) \quad (\Omega)$$

(V_{FSR} : FSR Det threshold value ± 0.5V
R_A : FSR IN ㉙ input resistance 10k Ω
R_B : FSR IN ㉙ external resistance)

Setting FSR time t_{FSR} (determination of C_{FSR} and R_f)

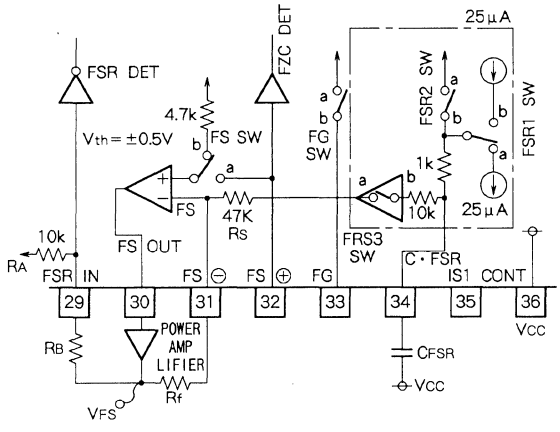
$$t_{FSR} = \frac{C_{FSR}}{I_{FSR}} - \frac{R_S'}{R_f} V_{FS} \cdots\cdots\cdots (2)$$



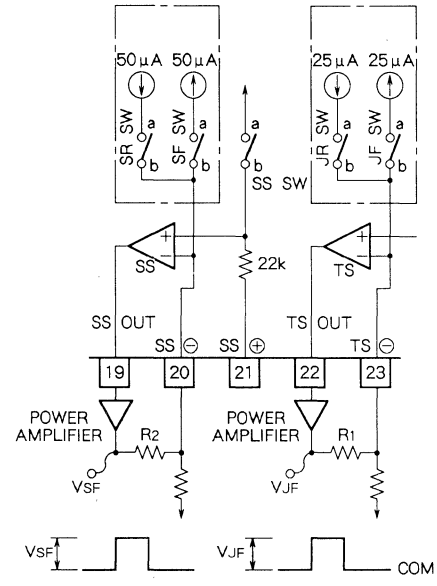
(R_S : FS ⊖ terminal ㉛ internal resistance 47k Ω
R_f : FS Amp external feedback resistance
C_{FSR} : C. FSR terminal ㉞ external capacitor
I_{FSR} : focus search current ± 25 μ A)

Setting jump pulse and slide feed voltages

- Jump pulse voltage V_{JF}
  $V_{JF} = R_1 \times 25\ \mu A$
- Slide feed voltage V_{SF}
  $V_{SF} = R_2 \times 50\ \mu A$



Note. Resistances in the diagram indicate standard values. Current and voltage values are those when the power source is ± 5V and RX = 47k Ω.



Functions of serial command

The logic controller has in itself a 8-bit shift register, which converts (or decodes) serial data from the microcomputer (input into MSD terminal ⑪) into commands for the servo IC.

Data-IN

The upper four bits (D_7 to D_4) of 8-bit data can set the command mode, and the lower four (D_3 to D_0) the command state.

Commands in the same mode can be used at the same time within a data transfer and remains as set until new data is input. Thus the command state does not change even if other modes are chosen.

Serial command function table (X = "1 or 0")

Mode	Input into Data IN terminal ⑪ (MSB ↓)								Output from Data OUT terminal ⑨
	Mode selection				Command state setting				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
FOCUS	0	0	0	0	FS ON	FG	$\overline{\text{FSR EN}}$	×	FS OK
TRACK1 A	0	0	0	1	SHOCK A	BRAKE A	TG2	TG1	SHOCK OUT
TRACK1 B			1		SHOCK B	BRAKE B			
TRACK2	0	0	1	0	TRACK		SLIDE		TC
SERVO OFF	0	1	×	×	×	×	×	×	0
STOP	1	1	×	×	×	×	×	×	0

Note 2. TRACK1 modes 1 and 2 are the same. TG2 and TG1 command states can be set in both TRACK1 A and B modes.
TRACK1 mode A or B determines SHOCK and BRAKE mode A or B. When either A or B is set to "1", the other is automatically released to "0".
SHOCK and BRAKE A and B can be released via TRACK1 A and B.

3. The states of command TRACK (D_3, D_2) and SLIDE (D_1, D_0) in TRACK2 mode are set in 2 bits each.
4. Output from Data OUT terminal ⑨ is automatically switched when the mode is switched.
5. 1 × × × × × × × is used for the command sent to the signal processing LSI, M50422P. During use of this command, the servo IC remains held, or unchanged, retaining the hold condition.

Command function table

Command	Mode	Data			Functions	
FS ON	FOCUS	D_3	1	ON	Starts focus search and turns focus on	
			0	OFF		
FG	↑	D_2	1	CLOSE	Open/close focus gain selector switch, FG SW	
			0	OPEN		
$\overline{\text{FSR EN}}$	↑	D_1	1	INHIBIT	Prohibits automatic focus re-intake D_1 = "1" actuates prohibition	
			0	ENABLE		
SHOCK A	TRACK1 A	D_3	1	ON	Inverts TG1 and TG2 SW's via shock detection (Shock OUT = "1")	
			0	OFF		
SHOCK B	TRACK1 B	D_3	1	ON	Prohibits TG1 and TG2 SW inversion when SHOCK A function + MR input = 1 (this is provided as remedy for flaws)	
			0	OFF		
BRAKE A	TRACK1 A	D_2	1	ON	Provides jump brake (setting) operation Open/closes TS2 SW	
			0	OFF		
BRAKE B	TRACK1 B	D_2	1	ON	Provides jump brake (setting) operation Open/closes TS1 SW	
			0	OFF		
TG2	TRACK1	D_1	1	OPEN	Controls track gain selector switch, TG2 SW	
			0	CLOSE		
TG1	TRACK1	D_0	1	OPEN	Controls track gain selector switch, TG1 SW	
			0	CLOSE		
TRACK	TRACK2	D_3	D_2			
		0	0	TS OFF	Track servo OFF	For the states of TS1, TS2, JF and JR SW's, refer to the Track Function Table
		0	1	TS ON	Track servo ON	
		1	0	JF	Forward jump	
		1	1	JR	Reverse jump	

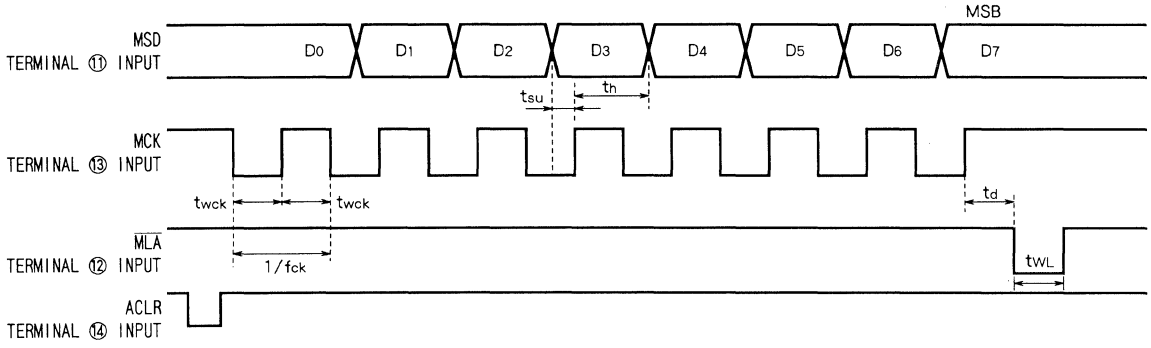
Command function table (Cont.)

Command	Mode	Data			Functions	
		D_1	D_0			
SLIDE	TRACK2	0	0	SS OFF	Slide servo OFF	For SS, SF and SR SW's, refer to the SLIDE Function Table
		0	1	SS ON	Slide servo ON	
		1	0	SF	Forward slide	
		1	1	SR	Reverse slide	
	SERVOOFF				Resets data D_0 to D_3 to "0"	
	STOP				Resets data D_0 to D_3 to "0" (this command is common to the signal processing LSI, M50422P)	

Serial data (MSD) transfer method

With data transferred by "LSD first", sending $\overline{MLA}$ signal, the command is executed.

Serial data input timing chart



Logic input conditions

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{ck}	Clock frequency		–	50	125	kHz
t_{wck}	Clock pulse width		4	20	–	μs
t_{su}	Set-up time		0.1	0.2	–	μs
t_h	Hold time		4	20	–	μs
t_d	Delay time		4	20	–	μs
t_{WL}	Latch pulse width		1	5	–	μs

BRAKE's A and B

With BRAKE A or B command set to "1", jump Brake operation begins, improving the jump setting ability after track jump.

Jump brake operation

- When MR = 1 (terminal ⑤ input), $\overline{TC}$ = "↑ or ↓" (TC Detoutput rise or fall) turns the track servo loop OFF.
- When MR = 0, $\overline{TC}$ = "↑ or ↓" turns the track servo loop ON.

Jump brake truth table

INPUT	OUTPUT	
MR $\overline{TC}$	BRAKE A = "1", the state of TS2 SW	BRAKE B = "1", the state of TS1 SW
1 ↑ ↓	a (track servo OFF)	b (track servo OFF)
0 ↑ ↓	b (track servo ON)	a (track servo ON)

When JF, JR or TS OFF command is effective, jump brake does not operate.

TRACK function table

INPUT			OUTPUT (SW position)			
	Data					
Command	D_3	D_2	TS1 SW	TS2 SW	JF SW	JR SW
TS OFF	0	0	a(servo ON)	a(servo OFF)	b	b
TS ON	0	1	a(servo ON)	b(servo ON)	b	b
JF	1	0	b(servo OFF)	b(servo ON)	a(JF ON)	b
JR	1	1	b(servo OFF)	b(servo ON)	b	a(JR ON)

SLIDE function table

INPUT			OUTPUT (SW position)		
	Data				
Command	D_1	D_0	SS SW	SF SW	SR SW
SS OFF	0	0	a(servo OFF)	b	b
SS ON	0	1	b(servo ON)	b	b
SF	1	0	a(servo OFF)	a(SF ON)	b
SR	1	1	a(servo OFF)	b	a(SR ON)

Direct command function

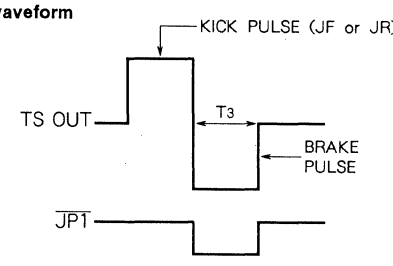
$\overline{JP1}$ signal

During jump of a track and the like operation, two serial data transfers can be omitted so as to decrease delay in microcomputer processing time.

JP1 is normally "1". Switching to $\overline{JP1}$ = "0" when TC (Data OUT) signal = "↑" causes the logic controller to automatically inverse the Jump polarity (JF→JR and JR→JF).

If $\overline{JP1}$ is changed from "0" to "1" upon completion of one-track jump (after given time T_3), JF and JR are automatically ended, thus turning TS and SS on.

Jump T. ACT waveform



$\overline{JP1}$ signal truth table

$\overline{JP1}$ (INPUT)	TRACK2 Mode (0010 D_3 D_2 D_1 D_0) (OUTPUT)							
	TRACK (D_3 D_2)				SLIDE (D_1 D_0)			
	00	01	10	11	00	01	10	11
1	TS OFF	TS ON	JF	JR	SS OFF	SS ON	SF	SR
0	TS OFF	TS ON	JR	JF	SS OFF	SS ON	SF	SR
↑	TS OFF	TS ON	TS ON	TS ON	SS ON	SS ON	SF	SR

Note 6. If $\overline{JP1}$ = "↑" command is input when TS is OFF (001000XX), TS and SS are not turned on.
7. If TS and SS are turned on when $\overline{JP1}$ = "↑", TS and SS are kept ON until the subsequent TRACK2 mode command arrives.

T•HLD

Is the direct control terminal of TS1 SW

T•HLD	Function (OUTPUT)
1	TS1 SW = OPEN
0	Logic control command prevails

When BRAKE TS is off, however, the logic command prevails for TS1 SW.

Logic output function

Data out

This is switched by changing the serial command mode (see the Serial Command Function Table).

Data output corresponds to the serial command mode sent last.

Data out output correspondence table

	Data OUT signal name	Serial command mode (INPUT)
(I)	FS ON	FOCUS (0000XXXX)
(II)	TC	TRACK2 (0010XXXX)
(III)	SHOCK	TRACK1 A (0001XXXX) TRACK1 B (0011XXXX)

(I) FS ON

When HF OK terminal ④ input = "1" and when FS SW = "a" (servo ON), this outputs FS OK = "1".

FS OK truth table

INPUT		OUTPUT
HF OK	FS SW position	FS OK
0	b(servo OFF)	0
1	b(servo OFF)	0
0	a(servo ON)	0
1	a(servo ON)	1

While FS OK = "0", the following hold regardless of the command state :

TS2 SW = "a" (servo OFF)

SS SW = "a" (servo OFF)

(II) TC

Outputs $\overline{TC}$ signals latching MR signals at the edge (rise or fall) of TC Det output TC.

TC = "0" during reset.

(III) SHOCK OUT

Outputs SHOCK Det signals (SHOCK OUT).

TC truth table

INPUT		OUTPUT
MR	$\overline{TC}$	TC
1	↑ or ↓	1
0	↑ or ↓	0

$\overline{HFD}$

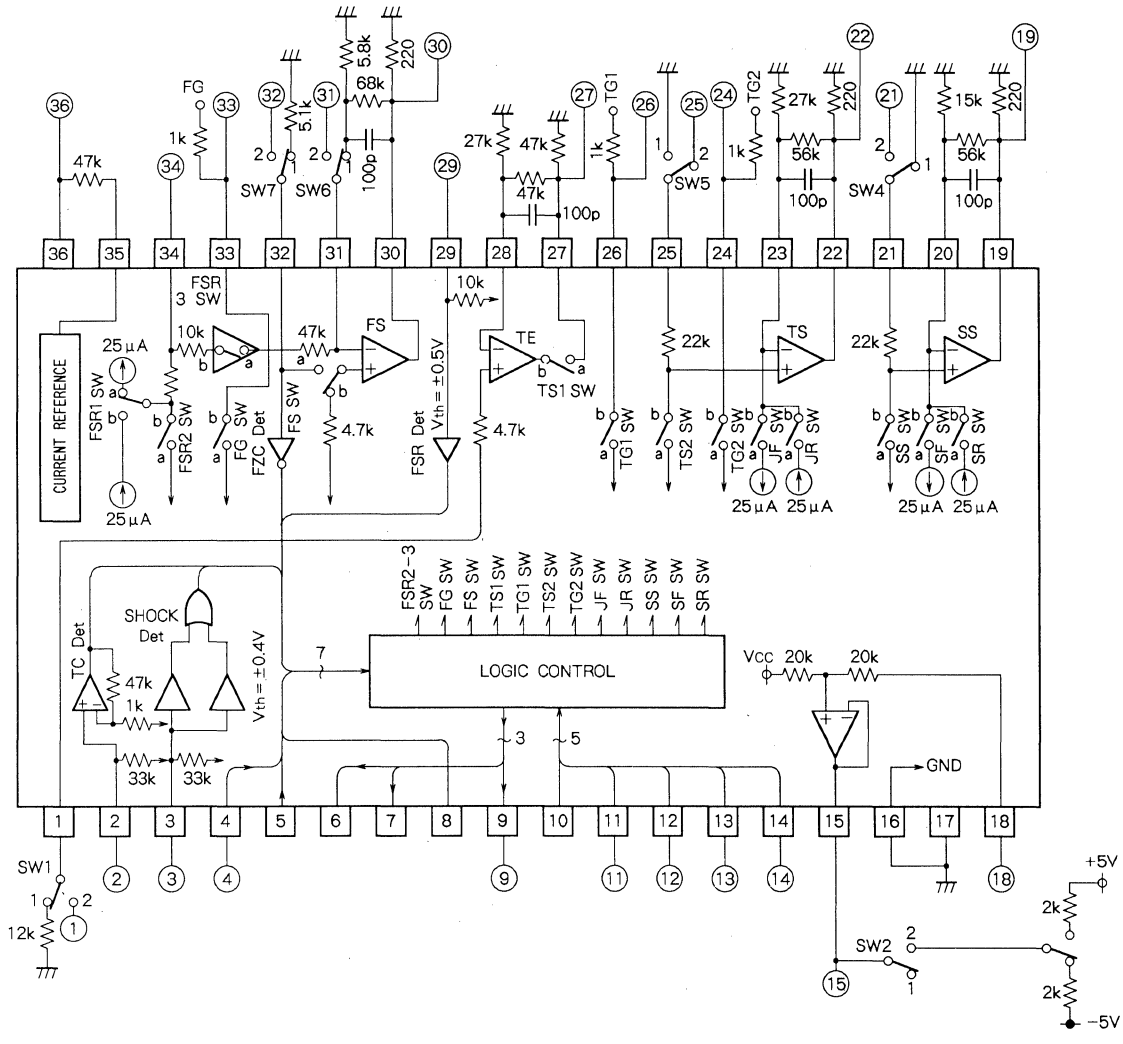
With MR signals (MR = "0" when HF signals are normal) of the pre-amplifiers (M51563P, M51567P, M51599FP) input to MR, this outputs HFD = "1" :

- During track jump
- During HF signal missing part detection (MR signal : MR = "1").

Jump flag

Outputs "1" when the serial command is TS OFF, JF, JR, and BRAKE, and "0" in other conditions.

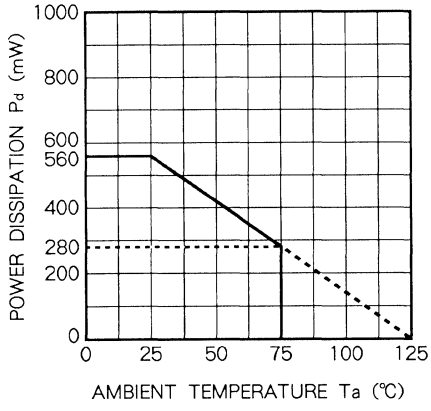
TEST CIRCUIT



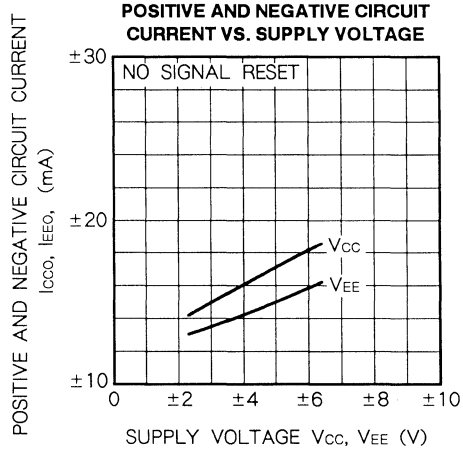
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

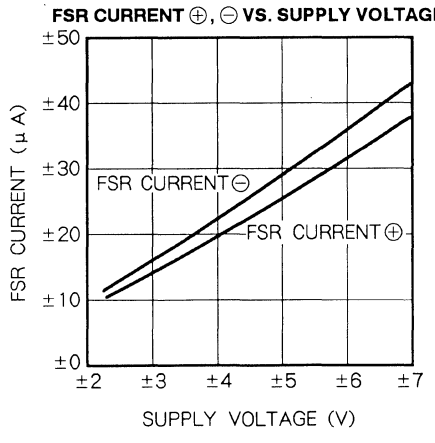
THERMAL DERATING



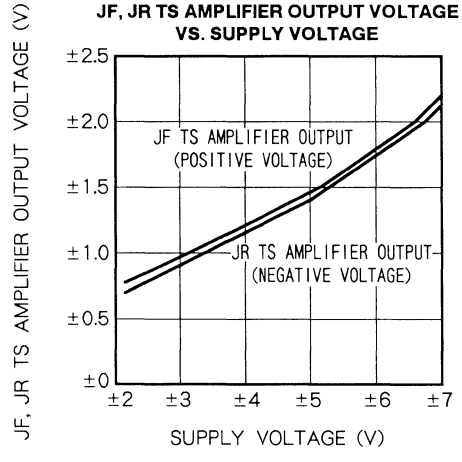
POSITIVE AND NEGATIVE CIRCUIT CURRENT VS. SUPPLY VOLTAGE



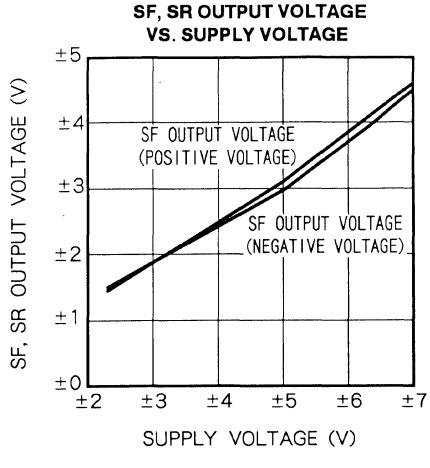
FSR CURRENT ⊕, ⊖ VS. SUPPLY VOLTAGE



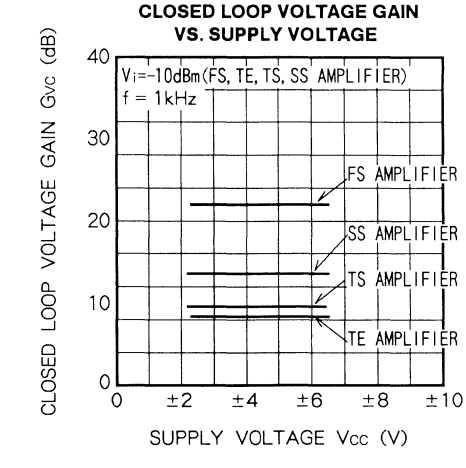
JF, JR TS AMPLIFIER OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



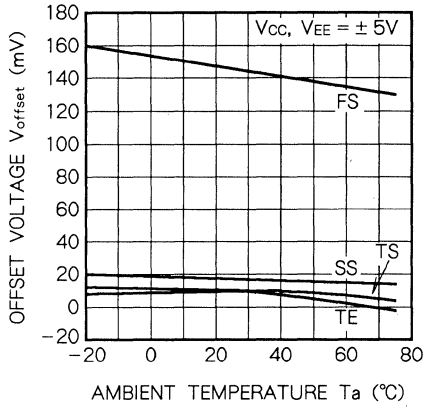
SF, SR OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



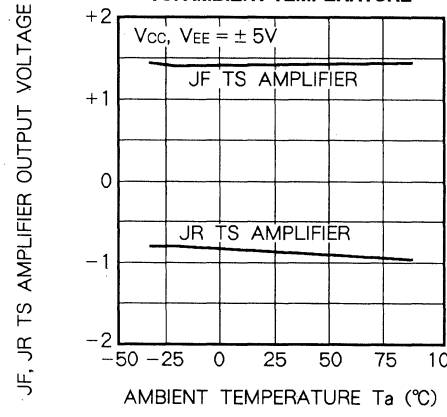
CLOSED LOOP VOLTAGE GAIN VS. SUPPLY VOLTAGE



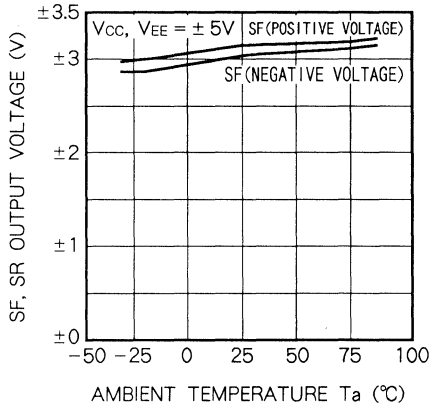
OFFSET VOLTAGE VS. AMBIENT TEMPERATURE



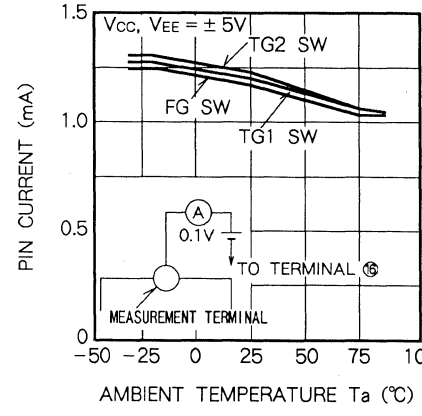
JF, JR TS AMPLIFIER OUTPUT VS. AMBIENT TEMPERATURE



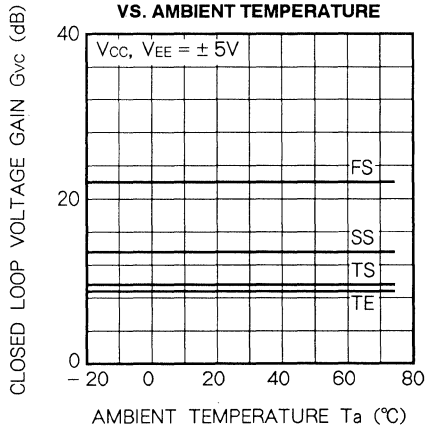
SF, SR OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



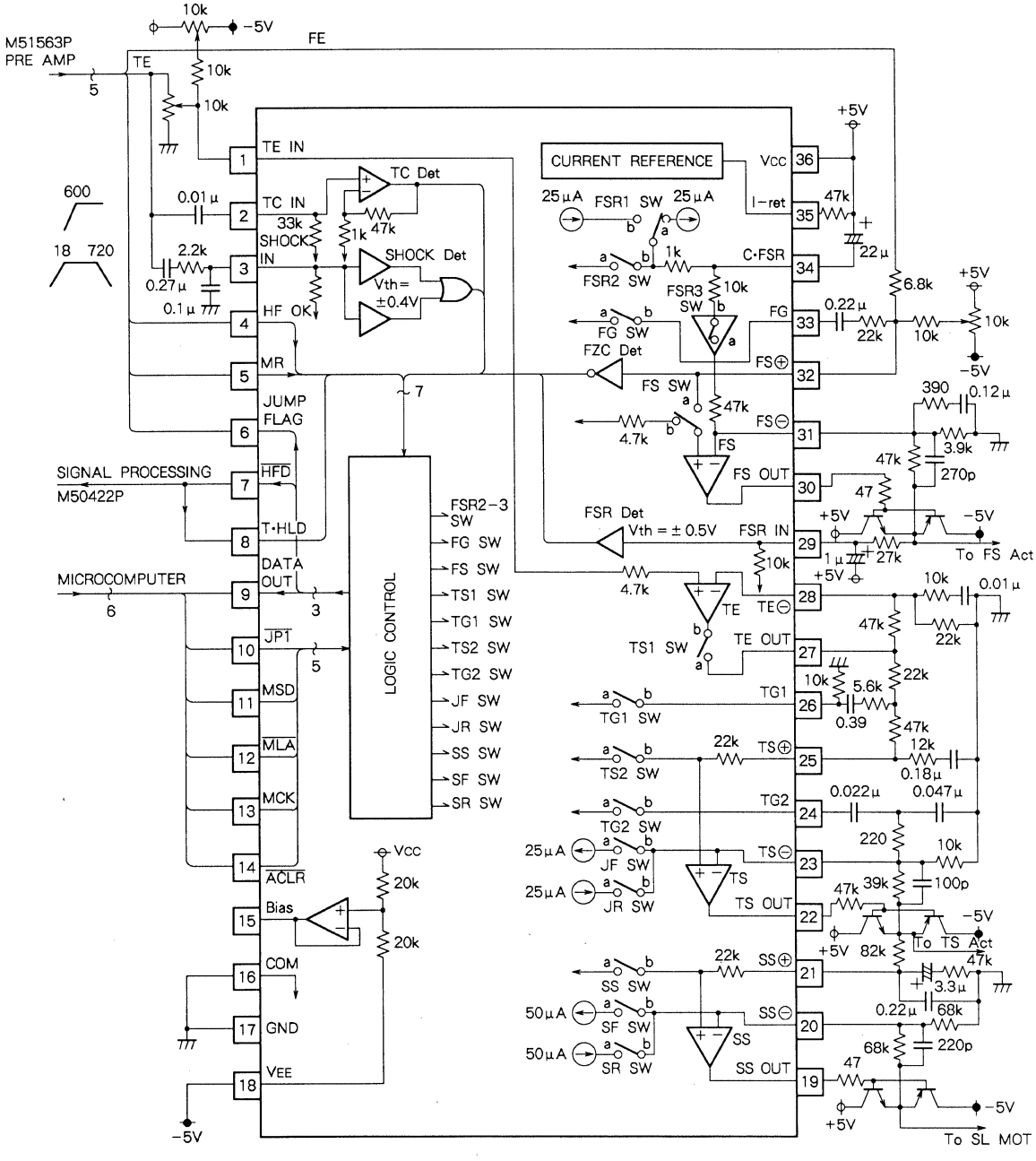
FG, TG1, TG2 SW PIN CURRENT VS. AMBIENT TEMPERATURE



CLOSED LOOP VOLTAGE GAIN VS. AMBIENT TEMPERATURE



APPLICATION EXAMPLE (V_{CC} = ± 5V, V_{EE} = − 5V)



Units Resistance : Ω
Capacitance : F

Note 8. Vth and current values are those when the power source is ± 5V.
Vth with the single −5V power source is used is about half that with ± 5V power source.

M51594AFP

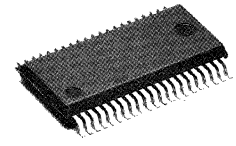
OPTICAL PICKUP SERVO CONTROL

DESCRIPTION

The M51594AFP is a semiconductor integrated circuit with built-in logic control, servo amp, and switches necessary to perform servo control of CD player optical pickups.

FEATURES

- Combination with preamplifier for optical pickup (M51595FP, M51567P, M51599FP, or M51598FP) makes it possible to form a pickup servo control system
- Single chip containing amp, switches, and logic controller necessary for servo control of optical pickup
- Built-in focus search circuit for automatic search up and down
- Built - in serial - to - parallel data converter to reduce microcomputer overloard
- Adaptures for any pickup by changing gain and frequency response of amplifiers with external components
- Built-in Vcc/2 generator to be capable of being driven by either dual or single power supply



Outline 42P2R-A

0.8mm pitch 450mil SSOP
(8.4mm × 17.5mm × 2.0mm)

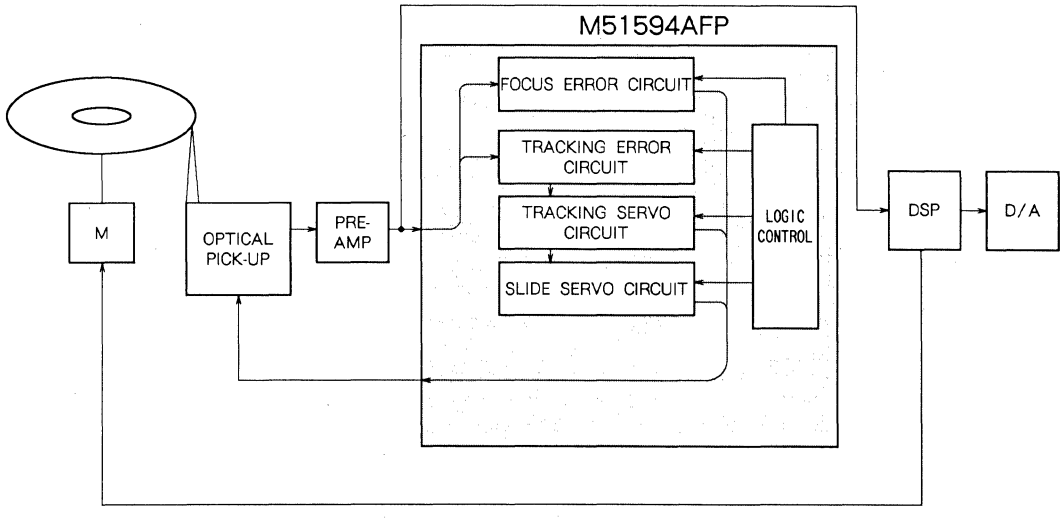
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC}, V_{EE} = ± 4.75~± 5.25V
or V_{CC} = 4.75~5.25V

Rated supply voltage
····· V_{CC}, V_{EE} = ± 5V(Split supply voltage)
or V_{CC} = 5V(Single supply voltage)

Rated power dissipation ····· 70mW

SYSTEM CONFIGURATION



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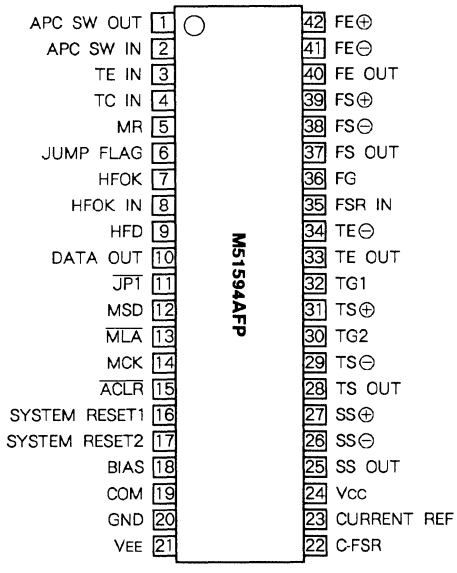
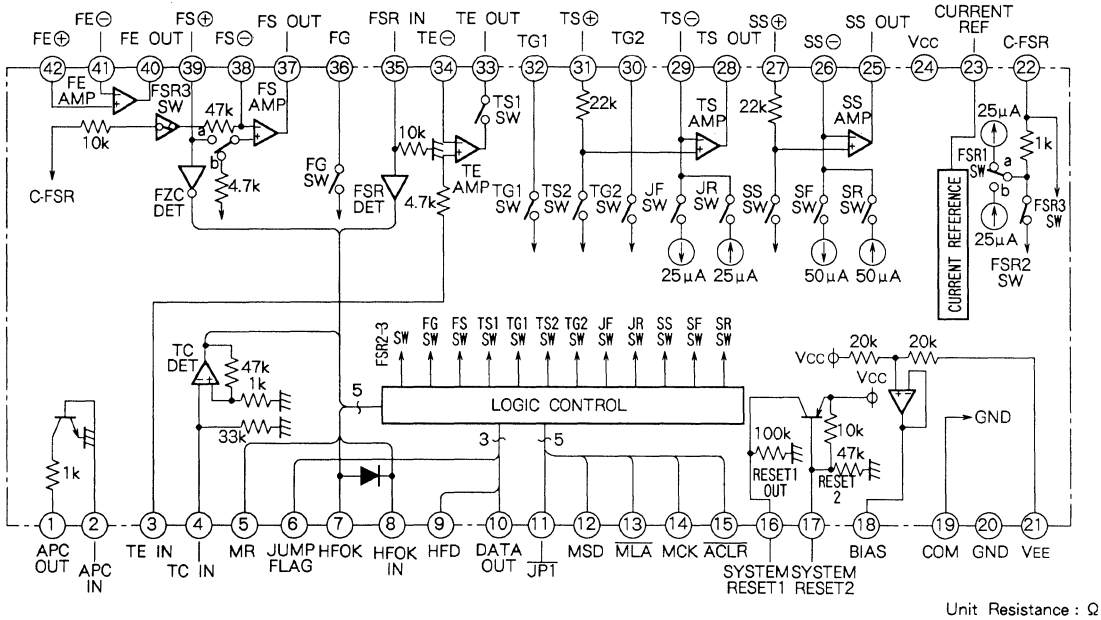
PIN CONFIGURATION



Outline 42P2R-A

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

PIN DESCREPTION

Pin No.	Symbol	Block	I/O	Function
①	APC SW OUT	APC	O	APC SW control output
②	APC SW IN	APC	I	APC SW control input
③	TE IN	Pre Amp. Input	I	Tracking error signal input
④	TC IN	↑	I	Tracking cross signal input
⑤	MR	↑	I	Mirror detected signal input
⑥	JUMP FLAG	Microcomputer I/O	O	Outputs High under Jump function
⑦	HF OK	Pre Amp. Input	I	HF OK signal input
⑧	HFOK IN	Input	I	HF OK signal input
⑨	HFD	Output (DSP)	O	Outputs High, when HF OK Low
⑩	DATA OUT	↑	O	Inner condition output changed by command modes
⑪	$\overline{JP1}$	↑	I	1 Track Jump control signal input (usually High)
⑫	MSD	↑	I	Serial data input (LSB first 8-bit data)
⑬	$\overline{MLA}$	↑	I	Latch signal of serial data from microcomputer to servo IC
⑭	MCK	↑	I	Clock signal of serial data from microcomputer to the servo IC
⑮	$\overline{ACLR}$	↑	I	All clear input (clear inner registers and flip-flops by Low signal)
⑯	SYSTEM RESET	RESET	O	Reset pulse output
⑰	SYSTEM RESET	RESET	I	Reset pulse witdh
⑱	BIAS	Regulated voltage	O	Outputs reference voltage ($\simeq \frac{V_{CC}}{2}$ at signal supply voltage)
⑲	COM	↑	I	COMMON connects to GND at split supply voltage : to pin⑱ at single supply voltage
⑳	GND	↑	I	GND
㉑	V_{EE}	↑	I	Negative supply voltage. At single supply voltage connects to GND
㉒	C-FSR	Focus serve	–	Connects the external capacitor for setting time constant of Focus search
㉓	CURRENT REF	Regulated voltage	I	Connects the external resistance for deciding value of current
㉔	V_{CC}	Supply voltage	I	Positive supply voltage
㉕	SS OUT	Side servo	O	SS Amp. output
㉖	SS⊖	↑	I	SS Amp. negative input
㉗	SS⊕	↑	I	SS Amp. positive input
㉘	TS OUT	Tracking servo	O	TS Amp. output
㉙	TS⊖	↑	I	TS Amp. negative input
㉚	TG2	↑	–	TG2 SW output
㉛	TS⊕	↑	I	TS Amp. positive input
㉜	TG1	↑	–	TG1 SW output
㉝	TE OUT	↑	O	TE Amp. output
㉞	TE⊖	↑	I	TE Amp. negative input
㉟	FSR IN	Focus servo	I	Focus search detector input
㊱	FG	↑	–	FG SW output
㊲	FS OUT	↑	O	FS Amp. output
㊳	FS⊖	↑	I	FS Amp. negative input
㊴	FS⊕	↑	I	FS Amp. positive input
㊵	FE OUT	↑	O	Focus error Amp. output
㊶	FE⊖	↑	I	Focus error Amp. negative input
㊷	FE⊕	↑	I	Focus error Amp. positive input

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	+ 6.5	V
V_{EE}		− 6.5	V
$\|V_I\|$	Input voltage (absolute value)	Applied supply voltage+0.3	V
$\|V_O\|$	Output voltage (absolute value)	Applied supply voltage+0.3	V
P_d	Power dissipation	750	mW
T_{opr}	Operating temperature	−20∼+75	℃
T_{stg}	Storage temperature	−40∼+125	℃

ELECTRICAL CHARACTERISTICS (V_{CC} = + 5V, V_{EE} = − 5V, Ta = 25℃, unless otherwise noted)

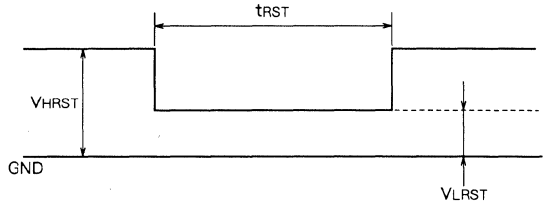
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	RESET	−	14	32	mA
I_{EE}	Circuit current	RESET	−28	−12	−	mA
G_{FE}	FE close loop voltage	f=1kHz, V_i = −10dBm	8	10	12	dB
V_{HFE}	FE output voltage high	V_i = 2V, R_L = 220 Ω	2.2	4	−	V
V_{LFE}	FE output voltage low	V_i = −2V, R_L = 220 Ω	−	−4	−2.2	V
G_{FS}	FS close loop voltage gain	f=1kHz, V_i = 10dBm	20	22	24	dB
A_{TTFS}	FS SW attenuation	f=1kHz, V_i = 0dBm	−	−35	−25	dB
R_{ONFG}	FG SW on resistor	f=1kHz, V_i = 0dBm	−	100	300	Ω
V_{HFS}	FS output voltage high	V_i = 1V, R_L = 220 Ω	2.2	4	−	V
V_{LFS}	FS output voltage low	V_i = −1V, R_L = 220 Ω	−	−4	−2.2	V
V_{FSR+}	FSR reference voltage ⊕	Note "FSR Detector Function"	0.40	0.45	0.50	V
V_{FSR-}	FSR reference voltage ⊖	Note "FSR Detector Function"	−0.54	−0.49	−0.44	V
G_{TE}	TE close loop voltage gain	f=1kHz, V_i = −10dBm	6.8	8.8	10.8	dB
G_{TS}	TS close loop voltage gain	f=1kHz, V_i = −10dBm	7.8	9.8	11.8	dB
A_{TTTS1}	TS SW attenuation	f=1kHz, V_i = 0dBm	−	−50	−30	dB
A_{TTTS2}			−	−50	−30	dB
R_{ONT1}	TG1 SW on resistor	f=1kHz, V_i = 0dBm	−	50	300	Ω
R_{ONT2}	TG2 SW on resistor	f=1kHz, V_i = 0dBm	−	50	300	Ω
V_{HTS}	TS output voltage high	V_i = 2V, R_L = 220 Ω	2.2	4	−	V
V_{LTS}	TS output voltage low	V_i = −2V, R_L = 220 Ω	−	−4	−2.2	V
G_{SS}	SS close loop voltage gain	f=1kHz, V_i = −10dBm	11.5	13.5	15.5	dB
A_{TTSS}	SS SW attenuation	f=1kHz, V_i = 0dBm	−	−54	−30	dB
V_{HSS}	SS output voltage high	V_i = 2V, R_L = 220 Ω	2.2	4	−	V
V_{LSS}	SS output voltage low	V_i = −2V, R_L = 220 Ω	−	−4	−2.2	V
V_{JF}	JF output voltage	Note "TRACK Function"	1.1	1.4	1.7	V
V_{JR}	JR output voltage	Note "TRACK Function"	−1.7	−1.4	−1.1	V
V_{SF}	SF output voltage	Note "SLIDE Function"	2.2	2.8	3.4	V
V_{SR}	SR output voltage	Note "SLIDE Function"	−3.4	−2.8	−2.2	V
V_{FCU+}	FZC⊕ reference voltage	Note "FSR Detector Function"	0.26	0.29	0.32	V
V_{FCU-}			−0.1	0	0.1	V
V_{FCD+}	FZC⊖ reference voltage	Note "FSR Detector Function"	−0.1	0	0.1	V
V_{FCD-}			−0.31	−0.28	−0.25	V
V_{TC+}	TC reference voltage	Note "BRAKE A, BRAKE B Function"	0	0.1	0.2	V
V_{TC-}			−0.2	−0.1	0	V
V_{HTE}	TE output voltage high	V_i = 2V, R_L = 47k Ω	3.5	4.2	−	V
V_{LTE}	TE output voltage low	V_i = −2V, R_L = 47k Ω	−	−4.2	−3.5	V
V_{OSFS}	FS output offset voltage	After up search	70	130	190	mV
V_{OSFE}	FE output offset voltage		−30	0	30	mV
V_{OSTE}	TE output offset voltage		−35	−10	15	mV
V_{OSTS}	TS output offset voltage		−5	20	45	mV
V_{OSSS}	SS output offset voltage		−30	0	30	mV
I_{FSRU}	FSR output current		21	29	37	μA
I_{FSRD}			−32	−25	−8	μA

* 0dBm = 775mVrms

ELECTRICAL CHARACTERISTICS (cont.) (V_{CC} = + 5V, V_{EE} = − 5V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{HSY}	SYSTEM RESET output valtage high	R_L = 20k Ω	4.0	4.9	−	V
V_{LSY}	SYSTEM RESET output valtage low	R_L = 20k Ω	−	0	0.2	V
I_{ALON}	APC SW "ON" output current		0.6	1.0	2.0	mA
I_{ALOF}	APC SW "OFF" output current		−10	0	10	μA

Note 1. Supply voltage turn on and pin ⑮ $\overline{ACLR}$ input reset pulse and next all parameter measures.



t_{RST} : 1 μs min
V_{HRST} : 2.5V min
V_{LRST} : 0.4V max

M51594AFP LOGIC CONTROL FUNCTION DESCRIPTION

1. Serial command function

The M51594AFP has a 8-bit shift resister in the logic control block to convert serial data from microcomputer input through MSD pin ⑫, to internal switch commands.

(1) Data-Input function

Higher 4 bits of the 8-bit data (D_7~D_4) are used to select the command mode. Lower 4 bits (D_3~D_0) set the command state.

Once a command is set, it is held until a new command of the same command mode is input. If an other command mode is selected the command state will not change.

Table 1. Serial command function

X = 1 or 0

Mode Name	MSB Mode Select D_7	D_6	D_5	D_4	Data IN pin ⑫ Input Command State D_3	D_2	D_1	LSB D_0	Data Out pin ⑩ Output
FOCUS	0	0	0	0	FS ON	FG	$\overline{\text{FSR EN}}$	×	$\overline{\text{FS OK}}$
TRACK1 A	0	0	0	1	×	BRAKE A	TG2	TG1	0
TRACK1 B			1		×	BRAKE B			
TRACK2	0	0	1	0	TRACK		SLIDE		TC
SERVO OFF	0	1	×	×	×	×	×	×	0
STOP	1	1	×	×	×	×	×	×	0

Note 2. TRACK1 A and TRACK1 B at the same command mode.
TG2 and TG1 are set by both commands. BRAKE A or B are determined by selecting TRACK1 A or TRACK1 B.
3. Data out (pin ⑩ output) is changed automatically when the command mode is selected.
4. The serial command 10XXXXXX is available of control M50422P/M50423FP/M50427FP (DSP LSI).
When this command input, the command state of M51594FP is not changed.

Table 2. Command function

Command	Command mode	Data			Function
FS ON	FOCUS	D_3	1	ON	Focus search start→ Focus on
			0	OFF	
FG	↑	D_2	1	CLOSE	FG SW for changing focus gain is opened or closed
			0	OPEN	
$\overline{\text{FSR EN}}$	↑	D_1	1	INHIBIT	Inhibit automatic re-search of focus
			0	ENABLE	
BRAKE A	TRACK1 A	D_2	1	ON	Jump break action. TS2 SW is opened or closed
			0	OFF	
BRAKE B	TRACK1 B	D_2	1	ON	Jump break action. TS1 SW is opened or closed
			0	OFF	
TG2	TRACK1	D_1	1	OPEN	TG2 SW for changing TRACK gain is controlled
			0	CLOSE	
TG1	TRACK1	D_0	1	OPEN	TG1 SW for changing TRACK gain is controlled
			0	CLOSE	
TRACK	TRACK2	D_3	D_2		SW states shown in Table 4
		0	0	TS OFF	Track servo off
		0	1	TS ON	Track servo on
		1	0	JF	Forward jump
		1	1	JR	Reverse jump
SLIDE	TRACK2	D_1	D_0		SW states shown in Table 5
		0	0	SS OFF	Slide servo off
		0	1	SS ON	Slide servo on
		1	0	SF	Forward slide
		1	1	SR	Reverse slide
–	SERVO OFF				Data of D_0~D_3 is reset to 0
–	STOP				Data of D_0~D_3 is reset to 0

SETTING CURRENT VALUE OF INTERNAL CURRENT SOURCES

(Focus search (FSR), Tracking servo (TS), Slide motor servo (SS))

Current value of internal current sources (FSR, TS, SS) is set by an external resistor connected between pin ㉓ and Vcc. (Resistance value : Rx)

If the current value of a current source (FSR, TS, SS) is IFSR, ITS, ISS)

$$I_{FSR} \simeq \frac{1}{8} \cdot \frac{V_{CC} - V_{㉓}}{Rx}$$

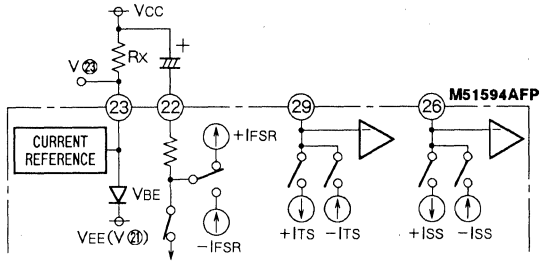
$$I_{TS} \simeq \frac{1}{8} \cdot \frac{V_{CC} - V_{㉓}}{Rx}$$

$$I_{SS} \simeq \frac{1}{4} \cdot \frac{V_{CC} - V_{㉓}}{Rx}$$

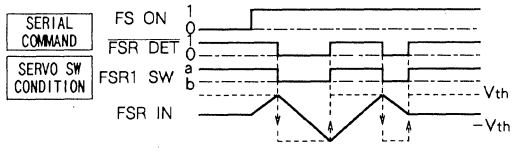
And if the voltage value of pin ㉑ is V ㉑, the voltage value of pin ㉓,

$V_{㉓} = V_{㉑} + V_{BE}$ ($V_{BE} \simeq 0.7V$)

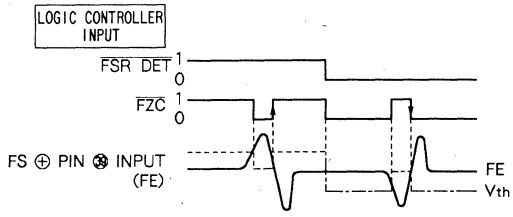
BLOCK DIAGRAM OF CURRENT SOURCES



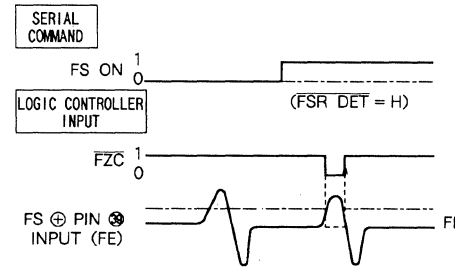
Timing chart of FSR det



Timing chart of FZC



FZC reset



FSR detector

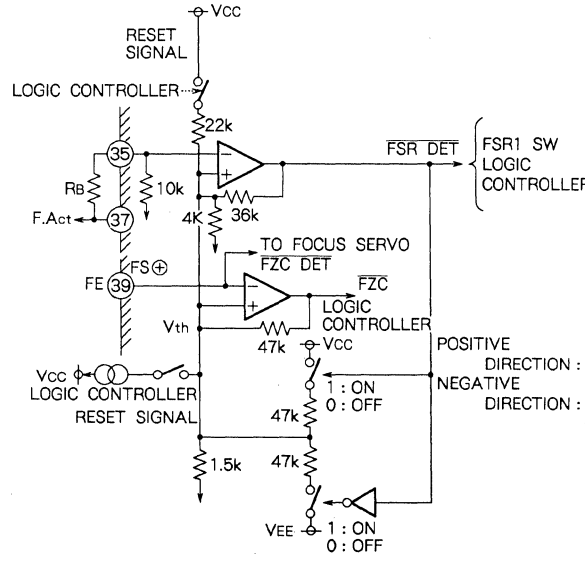
With external resistor (RB) connected between FS OUT (pin ㊲ output) and FSR IN (pin ㉟ input) at FSR function,

1) FSR direction,
2) Threshold voltage polarity of FZC detector are automatically changed.

Focus search always starts from positive voltage side. The direction of FSR is changed by FSR 1 SW controlled by $\overline{FSR\ DET}$ signal.

INPUT	OUTPUT		
FSR IN level VIN	$\overline{FSR\ DET}$	FSR1 SW	At ±5V FZC Vth
VIN > Vth	0	b : Negative direction of FSR	Min −0.30V Max 0V
VIN < Vth	1	a : Positive direction of FSR	0V 0.30V

Equivalent circuit



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(2) How to send serial data(MSD)

The serial command is executed by sending $\overline{MLA}$ signal after sending LSB serial data.

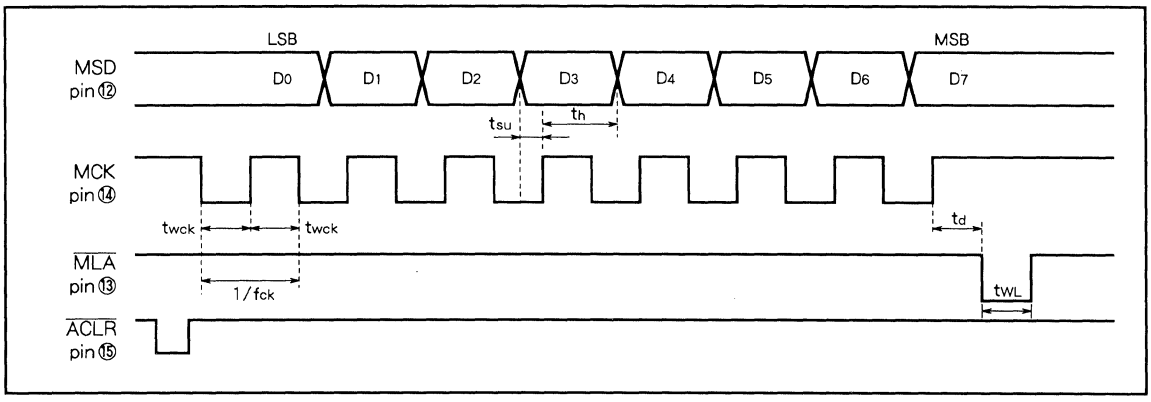


Fig. 1 Serial data input timing chart

2. BRAKE A, BRAKE B

When BRAKE A command or BRAKE B command is set to High (1), Jump brake operates.
This increases the ability to break after track jump

Jump brake action

1) When MR (pin ⑤ input) = 1, Track servo loop goes off at the edge of pulse output from TC Det.
2) When MR (pin ⑤ input) = 0, Track servo loop goes on at the edge of pulse output from TC Det.

Table 3. SW states at jump brake

INPUT	OUTPUT	
MR $\overline{TC}$	BRAKE A = 1 TS2 SW states	BRAKE B = 1 TS1 SW states
1 ⌐¬ 0 ⌐¬	a (TRACK servo OFF) b (TRACK servo ON)	b (TRACK servo OFF) a (TRACK servo ON)

3. TRACK, SLIDE

Table 4. Track function

INPUT			OUTPUT (SW state)			
Command	Data					
	D_3	D_2	TS1 SW	TS2 SW	JF SW	JR SW
TS OFF	0	0	a (servo ON)	a (servo OFF)	b	b
TS ON	0	1	a (servo ON)	b (servo ON)	b	b
JF	1	0	b (servo OFF)	b (servo ON)	a (JF ON)	b
JR	1	1	b (servo OFF)	b (servo ON)	b	a (JR ON)

Table 5. Slide function

INPUT			OUTPUT (SW state)		
Command	Data				
	D_1	D_0	SS SW	SF SW	SR SW
SS OFF	0	0	a (servo OFF)	b	b
SS ON	0	1	b (servo ON)	b	b
SF	1	0	a (servo OFF)	a (SF ON)	b
SR	1	1	a (servo OFF)	b	a (SR ON)

4. Direct command function

$\overline{JP1}$ Input

At one track jump, $\overline{JP1}$ signal allwes two transmissions of serial data to selected and restrains the delay time of microcomputer.

$\overline{JP1}$ is usually high. After microcomputer catches the up signal of data out output (TC singnal), if $\overline{JP1}$ goes down, the polarity of jump direction is automatically. (JF→JR, JR →JF)

After one track jump is finished (after period T3), if $\overline{JP1}$ goes up, Jump ends and the states become TS ON and SS ON.

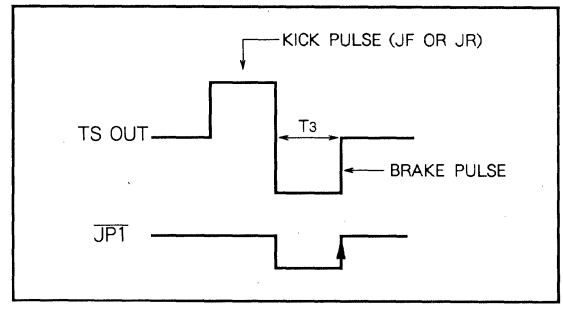


Fig. 2 $\overline{JP1}$ timing chart

Table 6. TRACK, SLIDE states by $\overline{JP1}$ Input

$\overline{JP1}$ (INPUT)	TRACK2 Mode (0010 D_3 D_2 D_1 D_0) (OUTPUT)							
	TRACK (D_3 D_2)				SLIDE (D_1 D_0)			
	00	01	10	11	00	01	10	11
1	TS OFF	TS ON	JF	JR	SS OFF	SS ON	SF	SR
0	TS OFF	TS ON	JR	JF	SS OFF	SS ON	SF	SR
↑	TS OFF	TS ON	TS ON	TS ON	SS ON	SS ON	SF	SR

Note 5. When command mode is TS OFF (001000XX, MSB first), even if $\overline{JP1}$ goes up, states do not become TS ON and SS ON.
6. Change to TS ON and SS ON after $\overline{JP1}$ goes up are held.

5. Logoc output function

(1) Data out

Data out output mode changes at each serial command mode.(shown in Table 1) It is decided by the last sent serial command.

Table 7. Data out output function

	Data Out output name	Serial Command Mode(INPUT)
(I)	FS OK	FOCUS (0000XXXX)
(II)	TC	TRACK2 (0010XXXX)

(I) FS OK

When HF OK (pin ⑦ input) was high and FS SW was closed (servo ON), FS OK is high.

Table 8. FS OK truth

INPUT		OUTPUT
HF OK	FS SW	FS OK
0	b (servo OFF)	0
1	b (servo OFF)	0
0	a (servo ON)	0
1	a (servo ON)	1

Note 7. While FS OK is low, TS2 SW and SS SW are opened regardless of the serial command.

(II) TC

TC pulse is producted by latching MR pulse with pulse edges of TC Det output ($\overline{TC}$). At reset, TC is low.

Table 9. TC output

INPUT		OUTPUT
MR	$\overline{TC}$	TC
1	↑ or ↓	1
0	↑ or ↓	0

(2) $\overline{\text{HFD}}$ (HF defect)

Output is High when HF OK is Low.

(3) Jump flag

Jump flag terminal outputs ; High when serial command is TS OFF or JF or JR or BRAKE. Outputs is low at other times.

6. Focus error amp

This amp is auxiliary.

7. APC switch

The APC circuit supply is controlled by this switch.

8. System reset

This circuit generates the reset pulse at power-on.

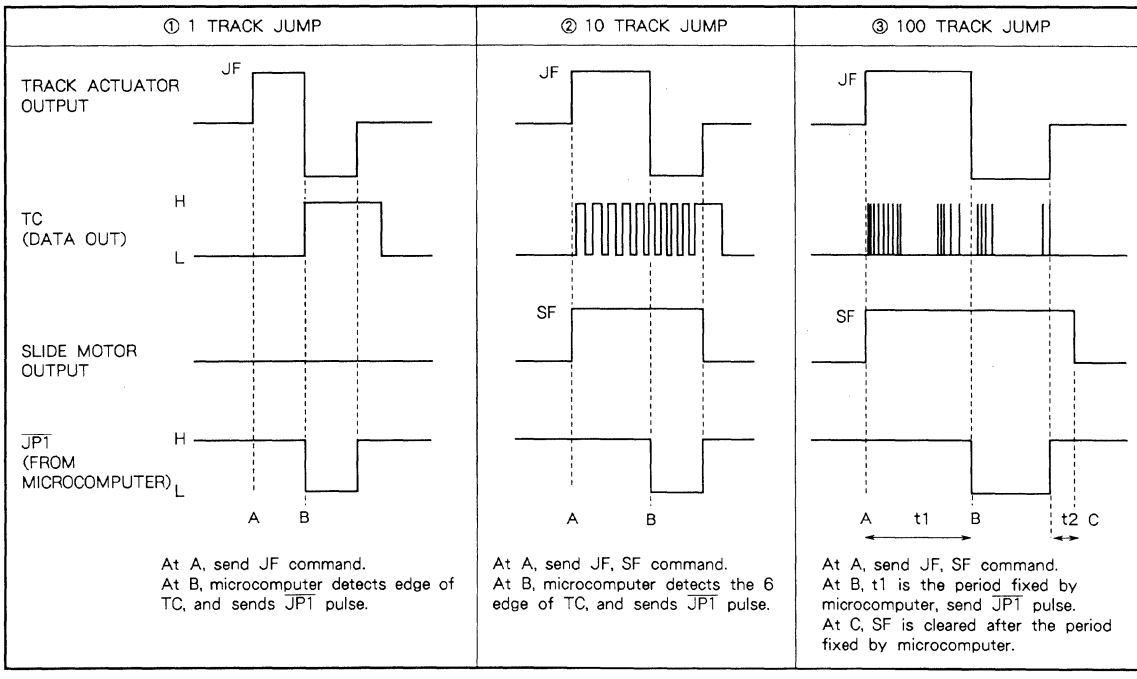
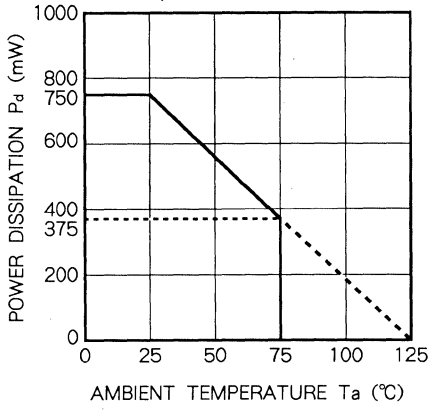


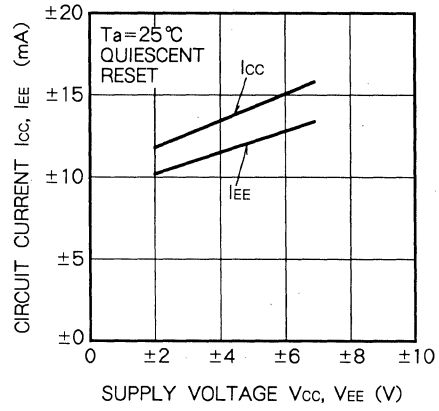
Fig. 3 Example for track jump timing. (Forward jump)

TYPICAL CHARACTERISTICS

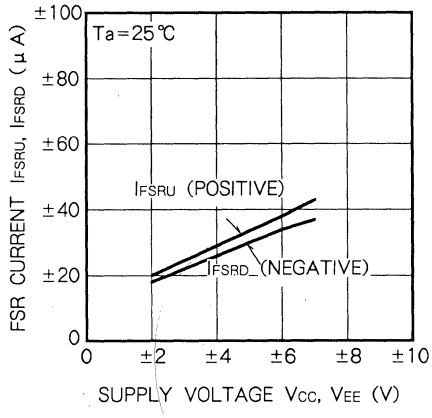
THERMAL DERATING (MAXIMUM RATING)



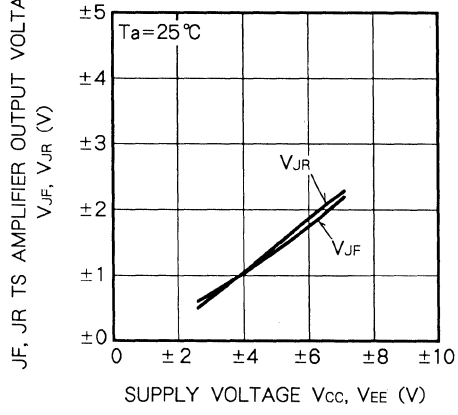
QUIESCENT CIRCUIT CURRENT VS. SUPPLY VOLTAGE



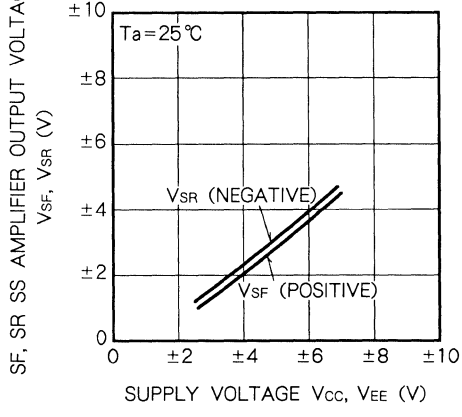
FSR CURRENT VS. SUPPLY VOLTAGE



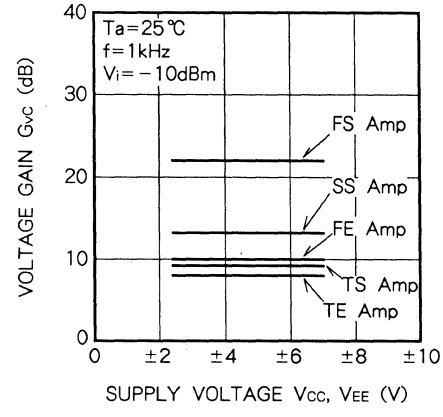
JF, JR, TS AMPLIFIER OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



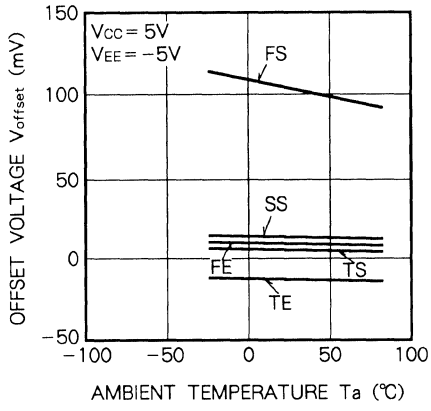
SF, SR SS AMPLIFIER OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



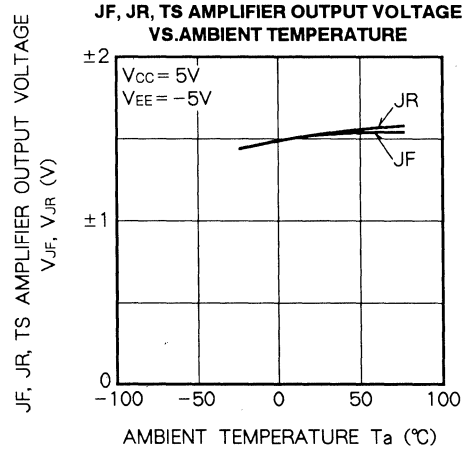
EACH AMPLIFIER VOLTAGE GAIN VS. SUPPLY VOLTAGE



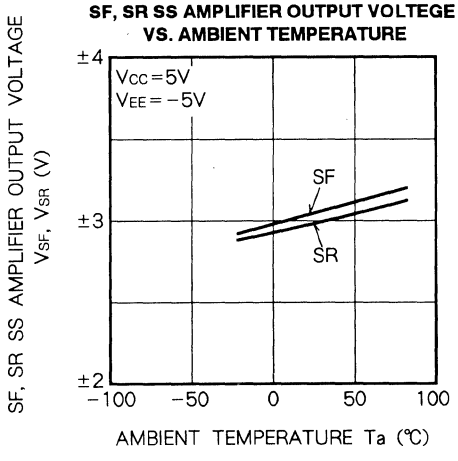
AMPLIFIER OFFSET VOLTAGES VS. AMBIENT TEMPERATURE



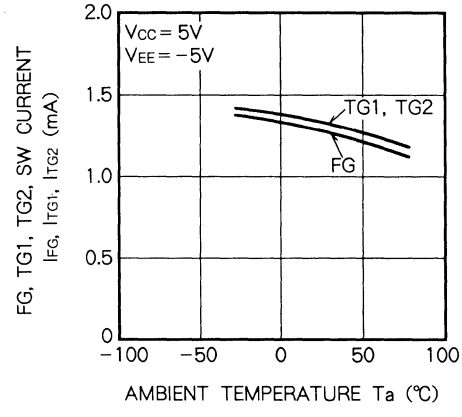
JF, JR, TS AMPLIFIER OUTPUT VOLTAGE VS.AMBIENT TEMPERATURE



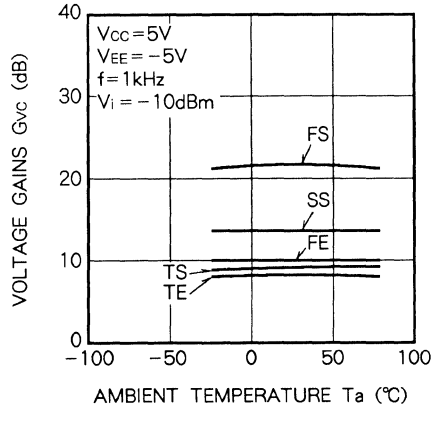
SF, SR SS AMPLIFIER OUTPUT VOLTEGE VS. AMBIENT TEMPERATURE



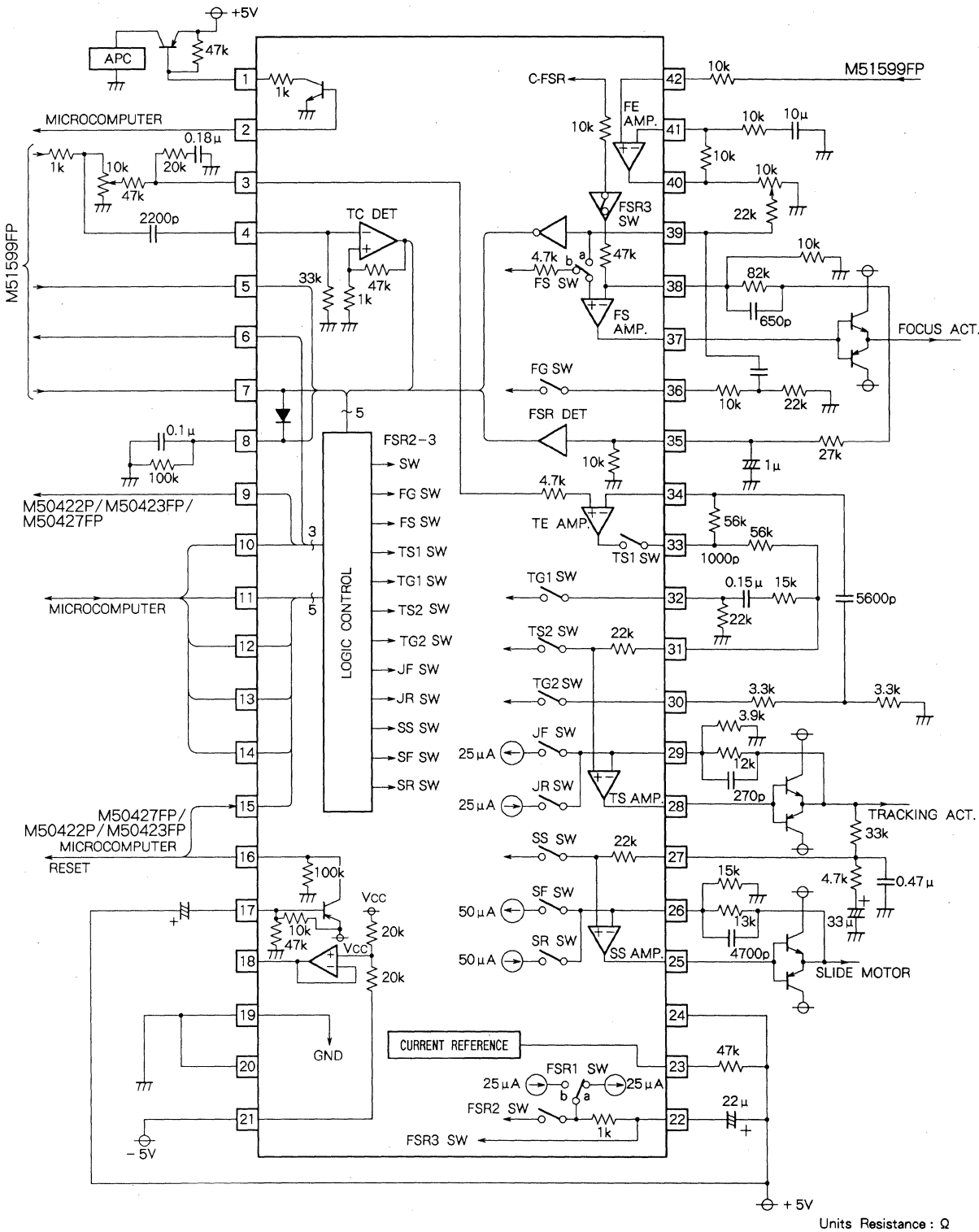
FG, TG1, TG2 CURRENT VS. AMBIENT TEMPERATURE



AMPLIFIER VOLTAGE GAINS VS. AMBIENT TEMPERATURE



APPLICATION EXAMPLE (V_{CC} = + 5V, V_{EE} = − 5V)



Units Resistance : Ω
Capacitance : F

MITSUBISHI ELECTRIC

M52130FP

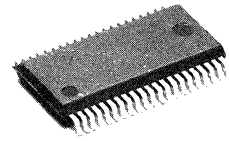
OPTICAL PICKUP SERVO CONTROL

DESCRIPTION

The M52130FP is a semiconductor integrated circuit with built-in logic control, servo amp, and switches necessary to perform servo control of CD player optical pickups.

FEATURES

- Combination with preamplifier for optical pickup (M51599FP or the like) makes it possible to form a pickup servo control system
- Built - in serial - to - parallel data converter to reduce microcomputer overloard
- Adaptures for any pickup by changing gain and frequency response of amplifiers with external components
- Capable of being driven by either dual or single power supply



Outline 42P2R-A

0.8mm pitch 450mil SSOP
(8.4mm × 17.5mm × 2.0mm)

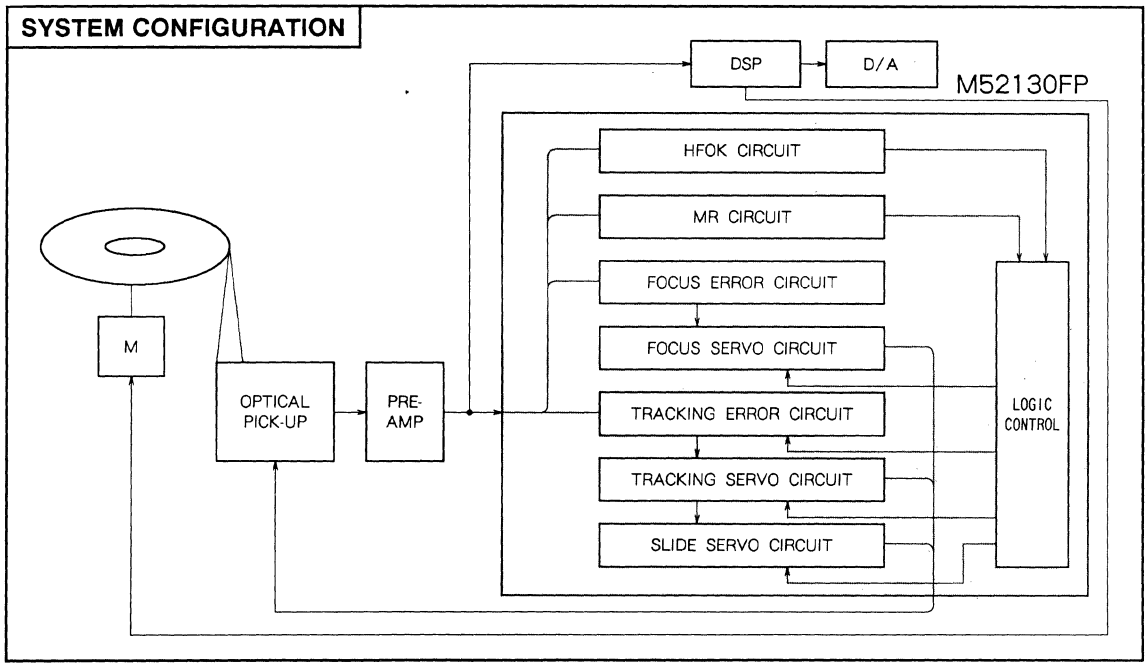
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC}, V_{EE} = ± 4.75 ~ ± 5.25V
or V_{CC} = 4.75 ~ 5.25V

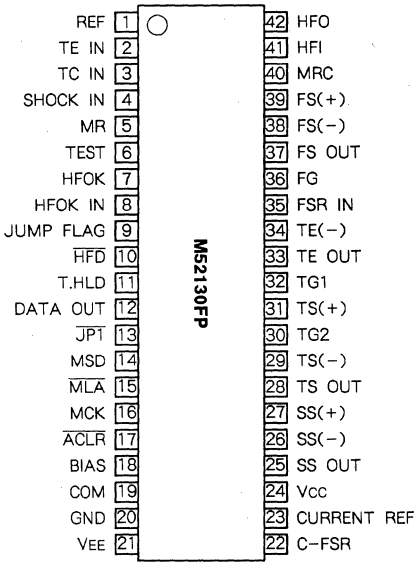
Rated supply voltage ····· V_{CC}, V_{EE} = ± 5V or V_{CC} = 5V

Rated power dissipation ····· 85mW

SYSTEM CONFIGURATION



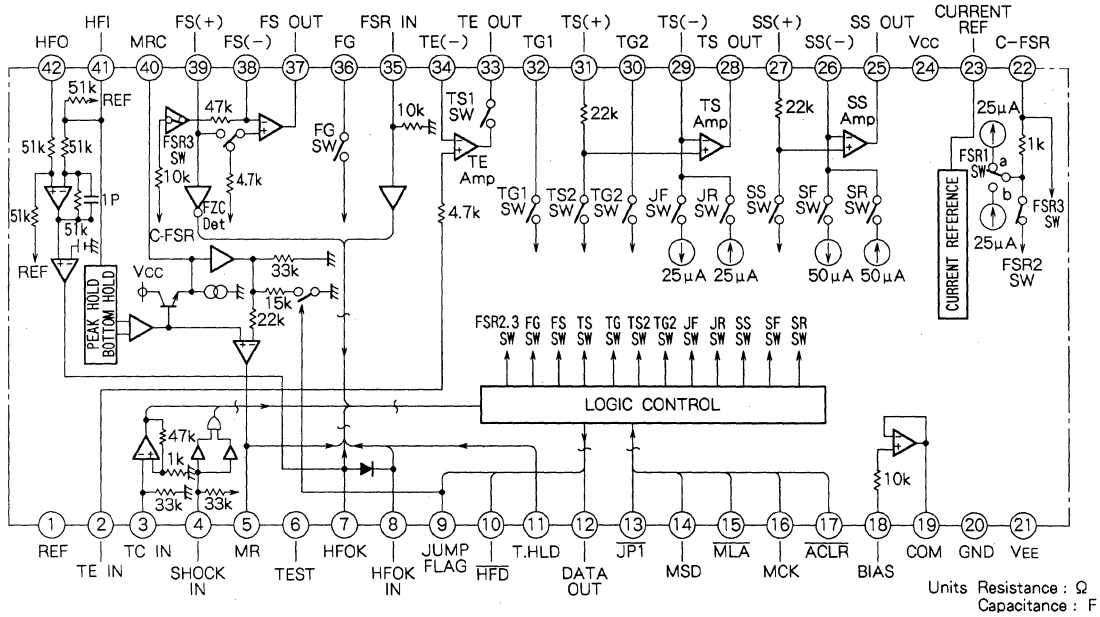
PIN CONFIGURATION



Outline 42P2R-A

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Block	I/O	Function
①	REF	Regulated voltage	I	Inputs reference voltage (MR, HFOK)
②	TE IN	Pre amp. input	I	Tracking error signal input
③	TC IN	↑	I	Track cross signal input
④	SHOCK IN	↑	I	Shock detector signal input
⑤	MR	↑	O	Mirror detected signal output
⑥	TEST	↑	I	Control HF OK and MR output moniter
⑦	HF OK	↑	O	HF OK signal output
⑧	HFOK IN	↑	O	HF OK signal output
⑨	Jump Flag	Microcomputer I/O	O	Outputs high under jump function
⑩	$\overline{\text{HFD}}$	↑	O	Outputs high, when MR = High and Tracking servo loop cuts off
⑪	T · HLD	Tracking servo	I	Direct control pin of TS1 SW
⑫	DATA OUT	Microcomputer I/O	O	Inner condition output changed by command modes
⑬	$\overline{\text{JPT}}$	↑	I	1 Track Jump control signal input (usually high)
⑭	MSD	↑	I	Serial data input (LSB first, 8-bit data)
⑮	$\overline{\text{MLA}}$	↑	I	Latch signal of serial data from microcomputer to servo IC
⑯	MCK	↑	I	Clock signal of serial data from microcomputer to servo IC
⑰	$\overline{\text{ACLR}}$	↑	I	All clear input (clear inner registors and flip-flops by low signal)
⑱	Bias	Regulated voltage	I	Inputs reference voltage from reference of pre Amp.
⑲	COM	↑	O	COMMON. Connects to GND at split supply voltage
⑳	GND	↑	I	GND
㉑	V_{EE}	↑	I	Negative supply voltage, at sinlge supply voltage connects to GND
㉒	C · FSR	↑	–	Connects the external capacitor for time constant of focus search
㉓	I-Ref	Regulated voltage	I	Connects the external resistance for deciding value of current
㉔	V_{CC}	Supply voltage	I	Positive supply voltage
㉕	SS OUT	Slide servo	O	SS amp. output
㉖	SS⊖	↑	I	SS amp. negative input
㉗	SS⊕	↑	I	SS amp. positive input
㉘	TS OUT	Tracking servo	O	TS amp. output
㉙	TS⊖	↑	I	TS amp. negative input
㉚	TG2	↑	–	TG2 SW output
㉛	TS⊕	↑	I	TA amp. positive input
㉜	TG1	↑	–	TG1 SW output
㉝	TE OUT	↑	O	TE amp. output
㉞	TE⊖	↑	I	TE amp. negative input
㉟	FSR IN	Focus servo	I	Focus search detector input
㊱	FG	↑	–	FG SW output
㊲	FS OUT	↑	O	FS amp. output
㊳	FS⊖	↑	I	FS amp. negative input
㊴	FS⊕	↑	I	FS amp. positive input
㊵	MRC	Pre amp. input	–	Connects the external capacitor for time constant of MR
㊶	HFI	↑	I	HF signal input
㊷	HFO	↑	I	HF signal input

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted.)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	+ 6.5	V
V_{EE}		− 6.5	V
V_I	Input voltage (absolute value)	|Applied supply voltage|+0.3	V
V_O	Output voltage (absolute value)	|Applied supply voltage|+0.3	V
P_d	Power dissipetion	750	mW
T_{opr}	Operating rempureture	−20∼+75	℃
T_{stg}	Storauge temperature	−40∼+125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limts			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage	Dual voltage, single voltage	+ 4.75	+ 5.0	+ 5.25	V
V_{EE}		Dual voltage	− 5.25	− 5.0	− 4.75	V
V_{IH}	Input voltage high		2.5	−	V_{CC}	V
V_{IL}	Output voltage low		0	−	0.4	V

ELECTRICAL CHARACTERISTICS (V_{CC} = + 5V, V_{EE} = − 5V, Ta = 25℃, unless otherwise noted)

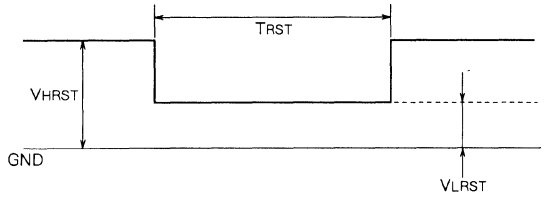
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	RESET	8	17	38	mA
I_{EE}	Circuit current	RESET	−36	−16	−7	mA
V_{FSR+}	FSR reference voltage +		0.32	0.37	0.42	V
V_{FSR-}	FSR reference voltage −		−0.54	−0.49	−0.44	V
I_{FSRU}	FSR output current		21	29	37	μA
I_{FSRD}			−35	−27	−19	μA
V_{FCU+}	FZC⊕ search reference voltage		0.24	0.28	0.32	V
V_{FCU-}			−0.1	0	0.1	V
V_{FCD+}	FZC⊖ search reference voltage		−0.1	0	0.1	V
V_{FCD-}			−0.31	−0.27	−0.23	V
V_{TC+}	TC reference voltage		0	0.1	0.2	V
V_{TC-}			−0.2	−0.1	0	V
V_{HFS}	FS output voltage high	V_i = 2V, R_L = 220 Ω	2.2	4	−	V
V_{LTS}	FS output voltage low	V_i = −2V, R_L = 220 Ω	−	−4	−2.2	V
V_{OSFS}	FS output offset voltage		70	130	190	mV
G_{FS}	FS close loop voltage gain	f=1kHz, V_i = −10dBm	20	22	24	dB
A_{TTFS}	FS SW attenuation	f=1kHz, V_i = 0dBm	−	−35	−25	dB
R_{ONFG}	FG SW on resistor	f=1kHz, V_i = 0dBm	−	50	300	Ω
V_{HTE}	TE output voltage high	V_i = 2V, R_L = 47k Ω	3.5	4.2	−	V
V_{LTE}	TE output voltage low	V_i = −2V, R_L = 47k Ω	−	−4.2	−3.5	V
V_{OSTE}	TE output offset voltage		−35	−10	15	mV
G_{TE}	TE close loop voltage gain	f=1kHz, V_i = −10dBm	6.8	8.8	10.8	dB
V_{HTS}	TS output voltage high	V_i = 2V, R_L = 220 Ω	2.2	4	−	V
V_{LTS}	TS output voltage low	V_i = −2V, R_L = 220 Ω	−	−4	−2.2	V
V_{OSTS}	TS output offset voltage		−5	20	45	mV
G_{TS}	TS close loop voltage gain	f=1kHz, V_i = −10dBm	7.8	9.8	11.8	dB
A_{TTTS1}	TS SW attenuation	f=1kHz, V_i = 0dBm	−	−50	−30	dB
A_{TTTS2}			−	−50	−30	dB
R_{ONT1}	TG1 SW on resistor	f=1kHz, V_i = 0dBm	−	50	300	Ω
R_{ONT2}	TG2 SW on resistor	f=1kHz, V_i = 0dBm	−	50	300	Ω
V_{HSS}	SS output voltage high		2.2	4	−	V
V_{LSS}	SS output voltage low		−	−4	−2.2	V
V_{OSSS}	SS output offset voltage		−30	0	30	mV
G_{SS}	SS close loop voltage gain	f=1kHz, V_i = −10dBm	11.5	13.5	15.5	dB
V_{JF}	JF output voltage		1.0	1.6	2.2	V
V_{JR}	JR output voltage		−2.2	−1.6	−1.0	V

ELECTRICAL CHARACTERISTICS (V_{CC} = + 5V, V_{EE} = − 5V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{SF}	SF output voltage		2.2	3.0	3.8	V
V_{SR}	SR output voltage		−3.8	−3.0	−2.2	V
V_{HOK}	HF OK output voltage high	V_i = ref + 1V	3.5	4.1	−	V
V_{LOK}	HF OK output voltage low	No signal	−	0	0.4	V
V_{THOK}	HF OK threshold voltage		0.29	0.40	0.51	V
V_{HMR}	MR output voltage high		3.5	4.1	−	V
V_{LMR}	MR output voltage low		−	0	0.4	V
C_{MRN}	MR envelop ratio(NORMAL)	f = 500kHz(carrier frequency)	0.26	0.36	0.46	−
C_{MRJ}	MR envelop ratio(JUMP)	f = 500kHz(carrier frequency)	0.5	0.6	0.7	−
f_{MR}	MR frequency characteristics(JUMP)	f=500kHz(carrier frequency), 55% AM modulation	47	60	−	kHz

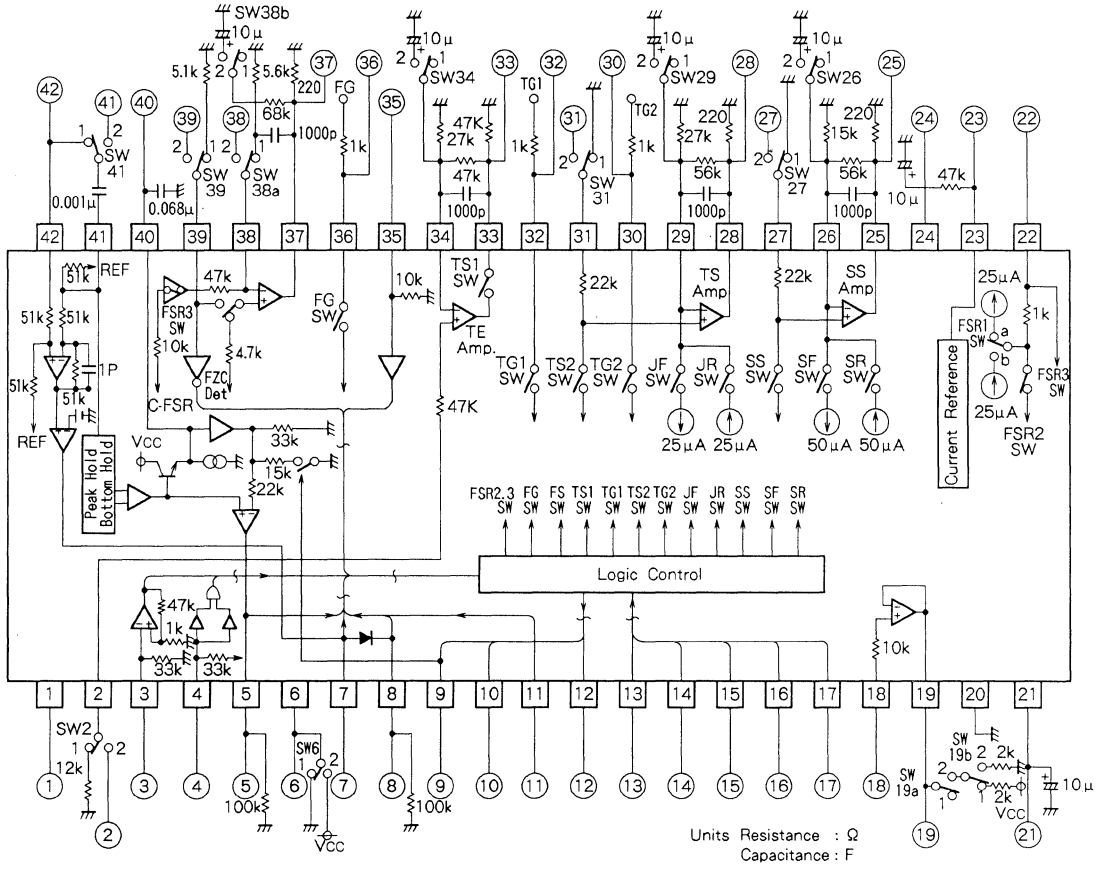
※ 0dBm = 775mVrms

Note 1. After switching voltage sw input pulse to pin ⑰ $\overline{ACLR}$ (under figure)



TRST : min 1 μs
VHRST : min 2.5V
VLRST : max 0.4V

TEST CIRCUIT



Judgement of current value of internal current sources

[Focus search (FSR), Tracking servo (TS), Slide motor servo (SS)] current value of internal current sources (FSR, TS, SS) is judged by an external resistor connected beween pin ㉓ and Vcc. (Resistance value : Rx) If the current value of a current source (FSR, TS, SS) is IFSR, ITS, ISS.

$$I_{FSR} \simeq \frac{1}{8} \cdot \frac{V_{CC} - V_{㉓}}{Rx}$$

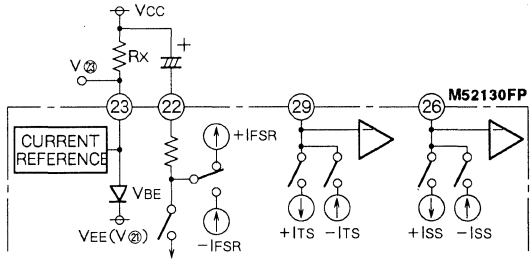
$$I_{TS} \simeq \frac{1}{8} \cdot \frac{V_{CC} - V_{㉓}}{Rx}$$

$$I_{SS} \simeq \frac{1}{4} \cdot \frac{V_{CC} - V_{㉓}}{Rx}$$

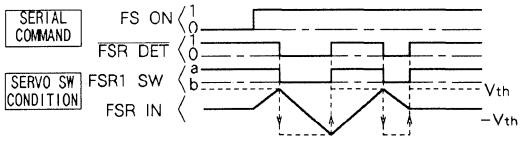
And if the voltage value of pin ㉑ is V 21, the voltage value of pin ㉓,

$$V_{㉓} = V_{㉑} + V_{BE} \quad (V_{BE} \simeq 0.7V)$$

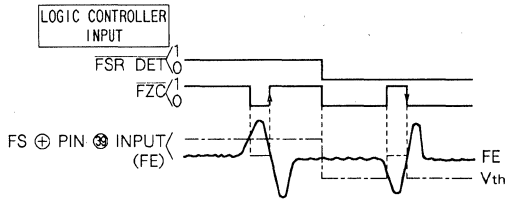
Block diagram of current sources



Timing chart of FRS Det



Timing chart of FZC



FSR detector

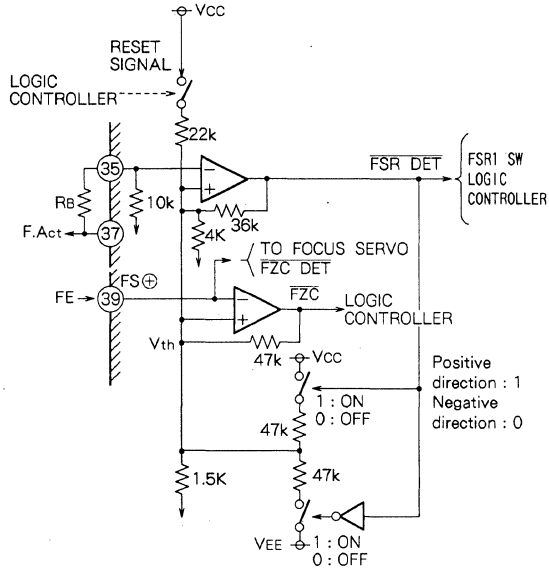
With external resistor (RB) connected between FS OUT (pin ㊲ output) and FSR IN (pin ㉟ input) at FSR function,

1) FSR directrion,
2) will automatically be changed.

Threshold voltage polarity of FZC detector foucus search always starts from positive voltaeg side. The direction of FSR is changed by FSR 1 sw which is controlled by $\overline{\text{FSR DET}}$ signal.

INPUT	OUTPUT		
FSR IN level V_{IN}	$\overline{\text{FSR Det}}$	FSR1 SW	At ±5V FZC V_{th}
$V_{IN} > V_{th}$	0	b:Negative direction of FSR	Min Max −0.30 ~ 0(V)
$V_{IN} < V_{th}$	1	a:Positive direction of FSR	0 ~ 0.30(V)

Equivalent circuit



MITSUBISHI ELECTRIC

1.Serial command function

The M52130FP has a 8-bit shift resister in the lojic control block to convert serial data from microcomputer input through MSD pin ⑭ control commands for internal switches.

(1) Data-Input function

The higher 4 bits of the 8 bit-data (D_7~D_4) can be used to select to command mode, the lower 4 bits (D_3~D_0) to set commands state.

Once a command is set, it is held until a new command of the same command mode is input. If an other command mode is selected the command state will not change.

Table 1 Serial command function table (X = 1 or 0)

Mode Name	MSB Mode Select D_7	D_6	D_5	D_4	Data IN pin ⑭ Input Command State D_3	D_2	D_1	LSB D_0	Data Out pin ⑫ Output
FOCUS	0	0	0	0	FS ON	FG	$\overline{\text{FSR EN}}$	×	FS OK
TRACK1 A	0	0	0	1	SHOCK A	BRAKE A	TG2	TG1	SHOCK OUT
TRACK1 B			1		SHOCK B	BRAKE B			
TRACK2	0	0	1	0	TRACK		SLIDE		TC
SERVO OFF	0	1	×	×	×	×	×	×	0
STOP	1	1	×	×	×	×	×	×	0

Note 2. TRACK1 A and TRACK1 B are the same command mode.
TG2 and TG1 are set by both commands. SHOCKA or B, BRAKE A or B are determined by selecting TRACK1 A or TRACK1 B.
3. Data-Out (pin ⑫ Output) is changed automatically when the command mode is seleted.
4. The serial command 1 0 × × × × × × is available to control of M50422P, M50427P, M65820FP (DSP LSI). When this command is input, the command state of M52130FP is not changed.

Table 2 Command function

Command	Command mode	Data			Function
FS ON	FOCUS	D_3	1	ON	Focus search start → Focus on
			0	OFF	
FG	↑	D_2	1	CLOSE	FG SW, for changing Focus gain, is opened or closed.
			0	OPEN	
$\overline{\text{FSR EN}}$	↑	D_1	1	INHIBIT	Inhibit automatic re-search of Focus
			0	ENABLE	
SHOCK A	TRACK1 A	D_3	1	ON	If SHOCK condition is detected, SHOCK OUT = 1, TG1 SW and TG2 SW are inverted.
			0	OFF	
SHOCK B	TRACK1 B	D_3	1	ON	Same function of SHOCK A. But if MR input was high, TG1 SW and TG2 SW are not inverted.
			0	OFF	
BRAKE A	TRACK1 A	D_2	1	ON	Jump Break action. TS2 SW is opened or closed.
			0	OFF	
BRAKE B	TRACK1 B	D_2	1	ON	Jump Break action. TS1 SW is opened or closed.
			0	OFF	
TG2	TRACK1	D_1	1	OPEN	TG2 SW for changing TRACK gain is controlled.
			0	CLOSE	
TG1	TRACK1	D_0	1	OPEN	TG1 SW for changing TRACK gain is controlled.
			0	CLOSE	
TRACK	TRACK2	D_3	D_2		SW states is shown by table-4.
		0	0	TS OFF	Track servo off
		0	1	TS ON	Track servo on
		1	0	JF	Foward Jump
		1	1	JR	Reverse Jump

Command function (Cont.)

Command	Command mode	Data			Function	
		D_1	D_0			
SLIDE	TRACK2	0	0	SS OFF	Slide servo off	SW states are shown in Table-4.
		0	1	SS ON	Slide servo on	
		1	0	SF	Foward slide	
		1	1	SR	Reverse slide	
	SERVOOFF				Data of D_0~D_3 is reset to "0"	
	STOP				Data of D_0~D_3 is reset to "0"	

(2) How to send serial data (MSD)

The serial command is executed by sending $\overline{MLA}$ signal after sending LSB serial data.

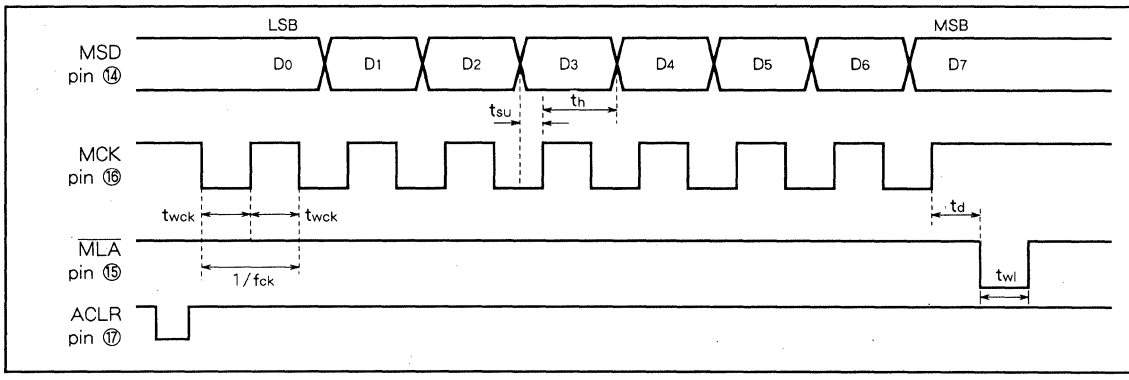


Fig. 1 Serial data input timing chart

2. BRAKE A, BRAKE B

When brake A ocmmand or brake B command is set to high 1, Jump brake operates. Pins increases the ability to break after track jump.

Jump brake action

1) When MR (pin ⑤ Input) = 1, Track servo 100P goes off at the edge of pulse output from TC det.
2) When MR (pin ⑤ Input) = 0, Track servo 100P goes on at the edge of pulse output from TC det.

Table 3 SW states at jump brake

INPUT	OUTPUT	
MR $\overline{TC}$	BRAKE A = 1 TS2 SW state	BRAKE B = 1 TS1 SW state
1 ⌐¬ 0 ⌐¬	a (TRACK servo OFF) b (TRACK servo ON)	b (TRACK servo OFF) a (TRACK servo ON)

3.TRACK, SLIDE

Table 4 Track function

INPUT			OUTPUT (SW state)			
	Data					
Command	D_3	D_2	TS1 SW	TS2 SW	JF SW	JR SW
TS OFF	0	0	a(servo ON)	a(servo OFF)	b	b
TS ON	0	1	a(servo ON)	b(servo ON)	b	b
JF	1	0	b(servo OFF)	b(servo ON)	a(JF ON)	b
JR	1	1	b(servo OFF)	b(servo ON)	b	a(JR ON)

Table 5 Slide function

INPUT			OUTPUT (SW state)		
	Data				
Command	D_1	D_0	SS SW	SF SW	SR SW
SS OFF	0	0	a(servo OFF)	b	b
SS ON	0	1	b(servo ON)	b	b
SF	1	0	a(servo OFF)	a(SF ON)	b
SR	1	1	a(servo OFF)	b	a(SR ON)

4. Direct command function

(1) $\overline{JP1}$ input

At one track jump, $\overline{JP1}$ signal allows two transmissions of serial data to be deleted, and restrains for delay time of microcomputer.

$\overline{JP1}$ is usually high. After microcomputer cotemes the up signal of data out output (TC signal), if $\overline{JP1}$ goes down, the polarity of jump direction is inverted automatically. (JF →JR JR→JF)

After one track jump is finished (after period T3), if $\overline{JP1}$ goes up, Jump end the states being TS ON and SS ON.

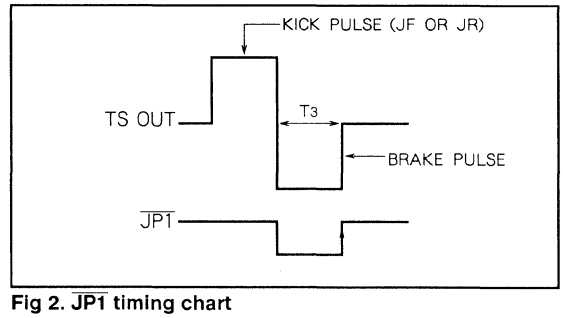


Fig 2. $\overline{JP1}$ timing chart

Table 6 Track, slide states by $\overline{JP1}$ Input

$\overline{JP1}$ (INPUT)	TRACK2 Mode (0 0 10 D_3 D_2 D_1 D_0) (OUTPUT)							
	TRACK (D_3 D_2)				SLIDE (D_1 D_0)			
	00	01	10	11	00	01	10	11
1	TS OFF	TS ON	JF	JR	SS OFF	SS ON	SF	SR
0	TS OFF	TS ON	JR	JF	SS OFF	SS ON	SF	SR
↑	TS OFF	TS ON	TS ON	TS ON	SS ON	SS ON	SF	SR

Note 5. When command mode is TS OFF (001000XX, MSB first), even if $\overline{JP1}$ = goes up, states do not become TS ON and SS ON.
6. Changes to TS ON and SS ON after $\overline{JP1}$ goes up, are held.

(2) T-HLD (Tracking hold) input

This is used for direct control terminal of TS1 SW.

Table 7 T-HLD function

T·HLD	Function (OUTPUT)
1	TS1 SW = OPEN
0	Controlled by Serial Command

Note 7. When BRAKE or TS OFF state are in effect TS1 SW is controlled by Serial Command.

5. Logic output function

(1) Data out

Data out output mode changes at each serial command mode. (shown in Table-1) It is decided by the last sent serial command.

Table 8 Data out output function

	Data Out output name	Serial Command Mode (INPUT)
(I)	FS OK	FOCUS (0000XXXX)
(II)	TC	TRACK2 (0010XXXX)
(III)	SHOCK	TRACK1 A (0001XXXX) TRACK1 B (0011XXXX)

(I) FS OK

When HF OK (pin ⑦ input) was high and FS SW was closed (servo ON), FS OK is high.

Table 9 FS OK truth table

INPUT		OUTPUT
HF OK	FS SW	FS OK
0	b(servo OFF)	0
1	b(servo OFF)	0
0	a(servo ON)	0
1	a(servo ON)	1

Note 8. While FS OK is low, TS2 SW and SS SW are opened, resadles of the Serial Command.

(II) TC

TC pulse is produced by latching MR pulse with pulse edges of TC Det output ($\overline{TC}$). At reset, TC is low.

Table 10 TC output

INPUT		OUTPUT
MR	$\overline{TC}$	TC
1	↑ or ↓	1
0	↑ or ↓	0

(III) SHOCK OUT

Output of SHOCK Det. (SHOCK OUT) appears through data out terminal.

(2) $\overline{HFD}$

1) During track jump
2) During the defection of HF signal (eye pattern). (MR pulse is high), $\overline{HFD}$ terminal output is high.

(3) Jump flag

Jump flag terminal output is high when serial command is TS OFF or JF or JR or BRAKE. Output is low at other times.

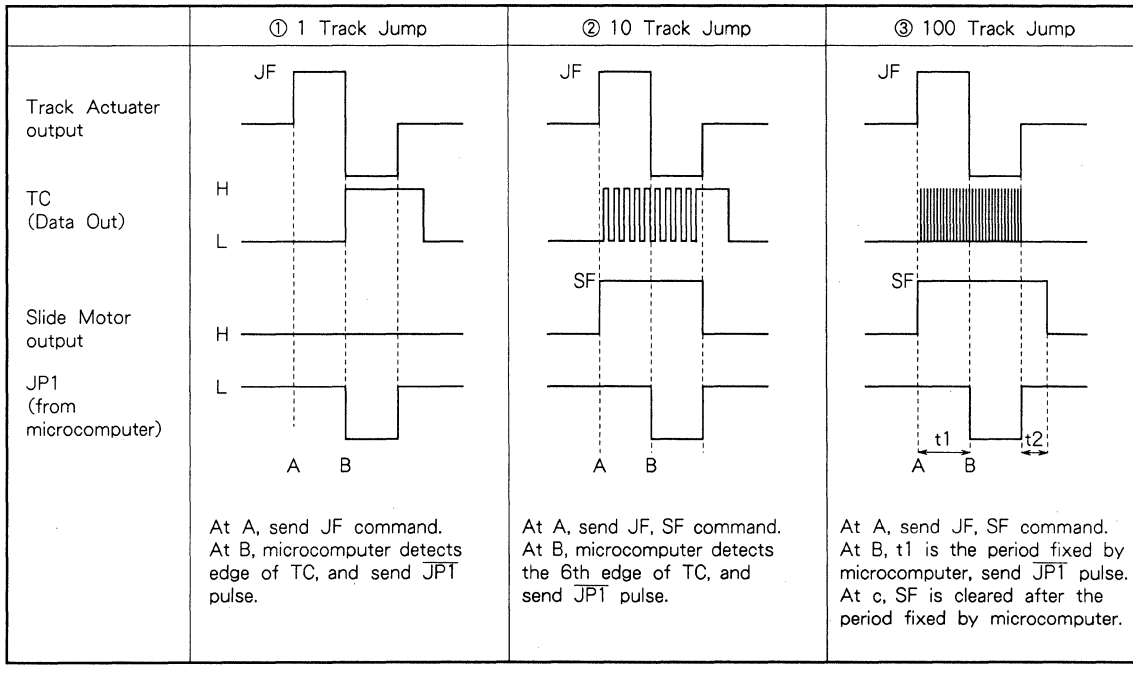
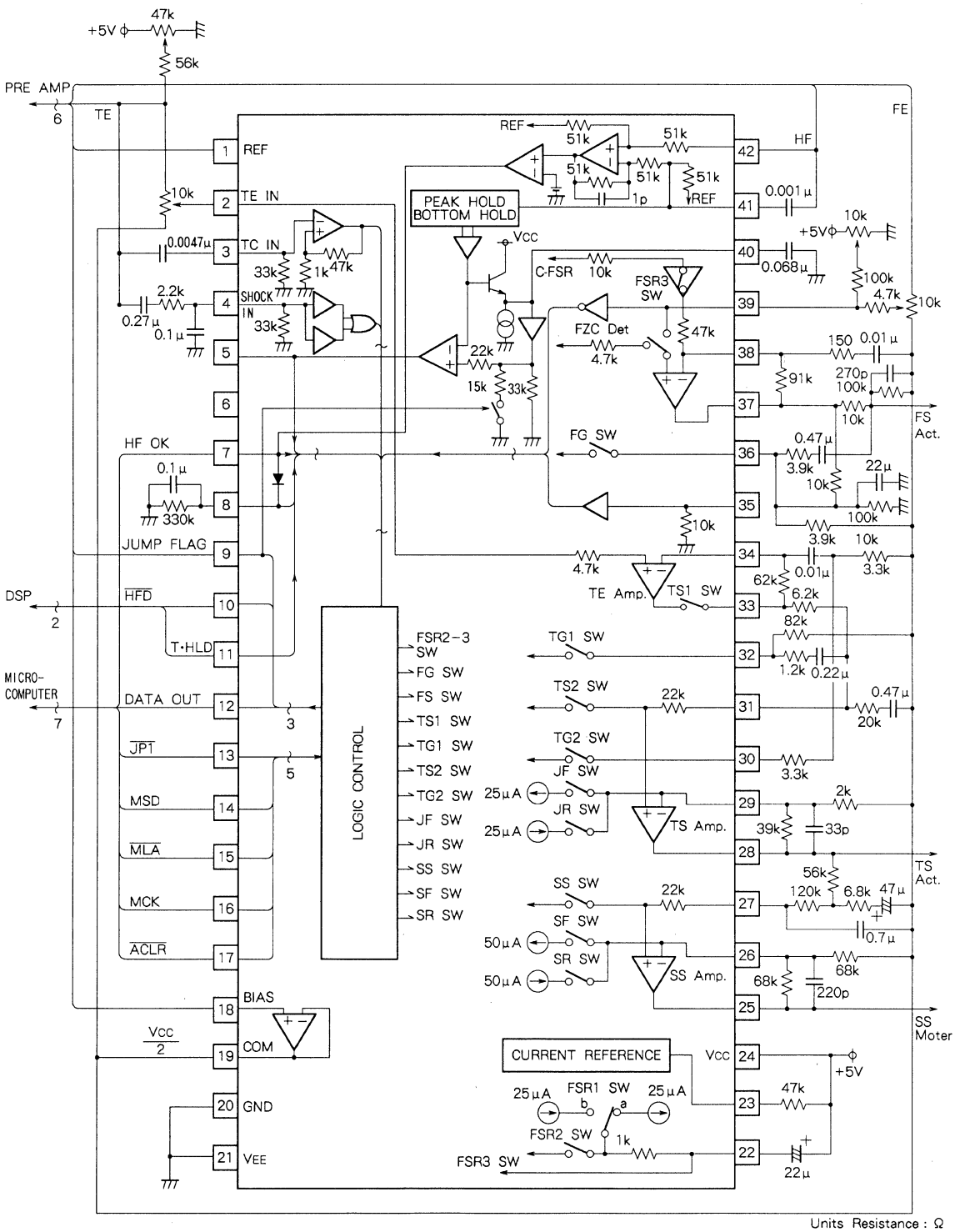


Fig. 3 Example for track jump timing. (Forward jump)

APPLICATION EXAMPLE (V_{CC} = + 5V)



Units Resistance : Ω
Capacitance : F

M52131FP

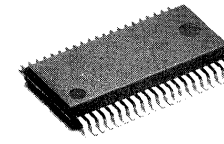
OPTICAL PICKUP SERVO CONTROL

DESCRIPTION

The M52131FP is a semiconductor integrated circuit with built-in logic control, servo amp, and switches necessary to perform servo control of CD player optical pickups.

FEATURES

- Combination with preamplifier for optical pickup (M51599FP or the like) makes it possible to form a pickup servo control system
- Built - in serial - to - parallel data converter to reduce microcomputer overloard
- Adaptures for any pickup by changing gain and frequency response of amplifiers with external components
- Capable of being driven by either dual or single power supply



Outline 42P2R-A

0.8mm pitch 450mil SSOP
(8.4mm × 17.5mm × 2.0mm)

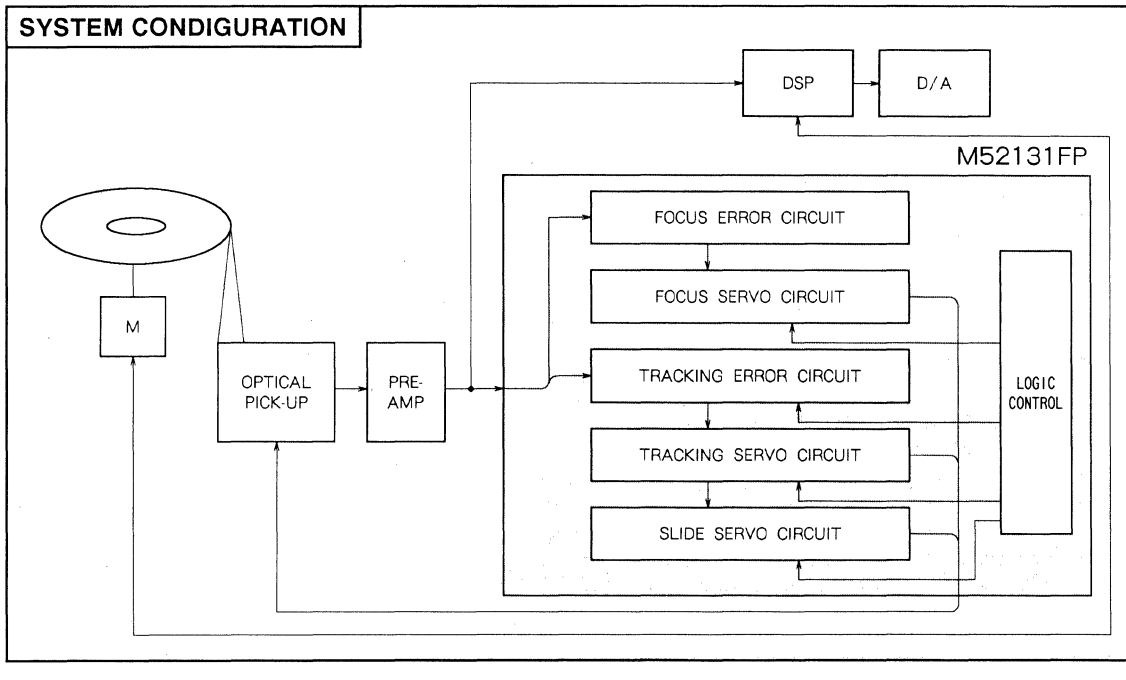
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC}, V_{EE} = ± 4.75~± 5.25V
or V_{CC} = 4.75~5.25V

Rated supply voltage ····· V_{CC}, V_{EE} ± 5V or V_{CC} = 5V

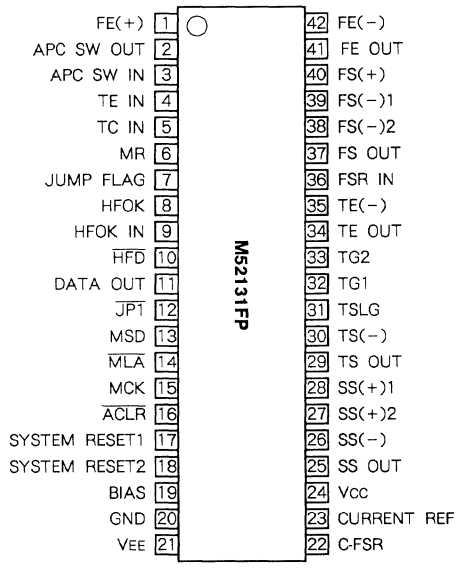
Rated power dissipation ····· 70mW

SYSTEM CONDIGURATION



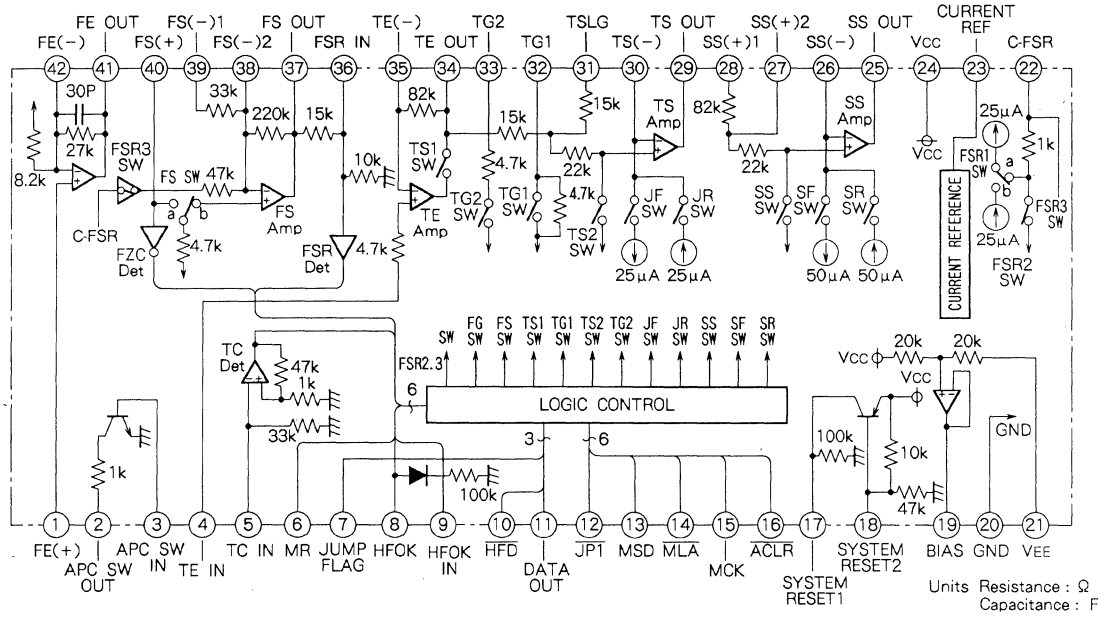
MITSUBISHI ELECTRIC

PIN CONFIGURATION



Outline 42P2R-A

IC INTERNAL BLOCK DIAGRAM



PIN DESCREPTION

Pin No.	Symbol	Block	I/O	Function
①	FE(+)	Focus servo	I	Focus error Amp. positive input
②	APC SW OUT	APC	O	APC SW control output
③	APC SW IN	APC	I	APC SW control input
④	TE IN	Pre Amp. Input	I	Tracking error signal input
⑤	TC IN	↑	I	Tracking cross signal input
⑥	MR	↑	I	Mirror detected signal input
⑦	JUMP FLAG	Microcomputer I/O	O	Outputs High under Jump function
⑧	HF OK	Pre Amp. Input	I	HF OK signal input
⑨	HFOK IN	Input	I	HF OK signal input
⑩	$\overline{\text{HFD}}$	Output (DSP)	O	Outputs High, when HF OK Low
⑪	DATA OUT	↑	O	Inner condition output changed by command modes
⑫	$\overline{\text{JP1}}$	↑	I	1 Track Jump control signal input (usually High)
⑬	MSD	↑	I	Serial data input (LSB first 8-bit data)
⑭	$\overline{\text{MLA}}$	↑	I	Latch signal of serial data from microcomputer to servo IC
⑮	MCK	↑	I	Clock signal of serial data from microcomputer to the servo IC
⑯	$\overline{\text{ACLR}}$	↑	I	All clear input (clear inner registers and flip-flops by Low signal)
⑰	SYSTEM RESET1	RESET	O	Reset pulse output
⑱	SYSTEM RESET2	RESET	I	Reset pulse witdh
⑲	BIAS	Regulated voltage	O	Outputs reference voltage ($\simeq \frac{V_{CC}}{2}$ at signal supply voltage)
⑳	GND	↑	I	GND
㉑	V_{EE}	↑	I	Negative supply voltage. At single supply voltage connects to GND
㉒	C-FSR	Focus serve	–	Connects the external capacitor for setting time constant of Focus search
㉓	CURRENT REF	Regulated voltage	I	Connects the external resistance for deciding value of current
㉔	V_{CC}	Supply voltage	I	Positive supply voltage
㉕	SS OUT	Slide servo	O	SS Amp. output
㉖	SS(−)	↑	I	SS Amp. negative input
㉗	SS(+)2	↑	I	SS Amp. positive input 2
㉘	SS(+)1	↑	I	SS Amp. positive input 1
㉙	TS OUT	Tracking servo	O	TS Amp. output
㉚	TS(−)	↑	I	TS Amp. negative input
㉛	TSLG	↑	I	TS Amp. Rowgain input
㉝	TG2	↑	–	TG2 SW output
㉜	TG1	↑	–	TG1 SW output
㉞	TE OUT	↑	O	TE Amp. output
㉟	TE(−)	↑	I	TE Amp. negative input
㊱	FSR IN	Focus servo	I	Focus search detector input
㊲	FS OUT	↑	O	FS Amp. output
㊳	FS(−)2	↑	I	FS Amp. negative input 2
㊴	FS(−)1	↑	I	FS Amp. negative input 1
㊵	FS(+)	↑	I	FS Amp. positive input
㊶	FE OUT	↑	O	Focus error Amp. output
㊷	FE(−)	↑	I	Focus error Amp. negative input

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	+6.5	V
V_{EE}		−6.5	V
$\|V_I\|$	Input voltage (absolute value)	Applied supply voltage+0.3	V
$\|V_O\|$	Output voltage (absolute value)	Applied supply voltage+0.3	V
P_d	Power dissipation	750	mW
T_{opr}	Operating temperature	−20～+75	℃
T_{stg}	Storage temperature	−40～+125	℃

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, V_{EE} = −5V, Ta = 25℃, unless otherwise noted)

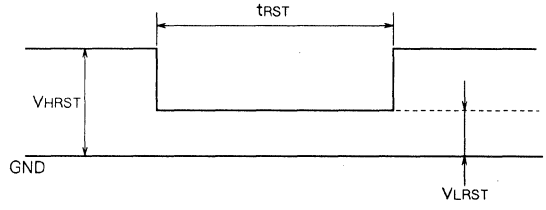
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	RESET	−	14	32	mA
I_{EE}	Circuit current	RESET	−28	−12	−	mA
G_{FE}	FE close loop voltage	f=1kHz, V_i = −10dBm	10.6	12.6	14.6	dB
V_{HFE}	FE output voltage high	V_i = 2V, R_L = 220Ω	2.2	4	−	V
V_{LFE}	FE output voltage low	V_i = −2V, R_L = 220Ω	−	−4	−2.2	V
G_{FS}	FS close loop voltage gain	f=1kHz, V_i = 10dBm	19.6	21.6	23.6	dB
A_{TTFS}	FS SW attenuation	f=1kHz, V_i = 0dBm	−	−35	−25	dB
V_{HFS}	FS output voltage high	V_i = 1V, R_L = 220Ω	2.2	4	−	V
V_{LFS}	FS output voltage low	V_i = −1V, R_L = 220Ω	−	−4	−2.2	V
V_{FSR+}	FSR reference voltage ⊕	Note "FSR Detector Function"	0.40	0.45	0.50	V
V_{FSR-}	FSR reference voltage ⊖	Note "FSR Detector Function"	−0.54	−0.49	−0.44	V
G_{TE}	TE close loop voltage gain	f=1kHz, V_i = −10dBm	6.8	8.8	10.8	dB
G_{TS}	TS close loop voltage gain	f=1kHz, V_i = −10dBm	7.8	9.8	11.8	dB
A_{TTTS1}	TS SW attenuation	f=1kHz, V_i = 0dBm	−	−50	−30	dB
A_{TTTS2}			−	−50	−30	dB
R_{ONT1}	TG1 SW on resistor	f=1kHz, V_i = 0dBm	−	50	300	Ω
R_{ONT2}	TG2 SW on resistor	f=1kHz, V_i = 0dBm	3.9	4.7	5.8	kΩ
V_{HTS}	TS output voltage high	V_i = 2V, R_L = 220Ω	2.2	4	−	V
V_{LTS}	TS output voltage low	V_i = −2V, R_L = 220Ω	−	−4	−2.2	V
G_{SS}	SS close loop voltage gain	f=1kHz, V_i = −10dBm	11.5	13.5	15.5	dB
A_{TTSS}	SS SW attenuation	f=1kHz, V_i = 0dBm	−	−54	−30	dB
V_{HSS}	SS output voltage high	V_i = 2V, R_L = 220Ω	2.2	4	−	V
V_{LSS}	SS output voltage low	V_i = −2V, R_L = 220Ω	−	−4	−2.2	V
V_{JF}	JF output voltage	Note "TRACK Function"	1.1	1.4	1.7	V
V_{JR}	JR output voltage	Note "TRACK Function"	−1.7	−1.4	−1.1	V
V_{SF}	SF output voltage	Note "SLIDE Function"	2.2	2.8	3.4	V
V_{SR}	SR output voltage	Note "SLIDE Function"	−3.4	−2.8	−2.2	V
V_{FCU+}	FZC⊕ reference voltage	Note "FSR Detector Function"	0.26	0.29	0.32	V
V_{FCU-}			−0.1	0	0.1	V
V_{FCD+}	FZC⊖ reference voltage	Note "FSR Detector Function"	−0.1	0	0.1	V
V_{FCD-}			−0.31	−0.28	−0.25	V
V_{TC+}	TC reference voltage	Note "BRAKE A, BRAKE B Function"	0	0.1	0.2	V
V_{TC-}			−0.2	−0.1	0	V
V_{HTE}	TE output voltage high	V_i = 2V, R_L = 47kΩ	3.5	4.2	−	V
V_{LTE}	TE output voltage low	V_i = −2V, R_L = 47kΩ	−	−4.2	−3.5	V
V_{OSFS}	FS output offset voltage	After up search	70	110	170	mV
V_{OSFE}	FE output offset voltage		−30	0	30	mV
V_{OSTE}	TE output offset voltage		−25	0	25	mV
V_{OSTS}	TS output offset voltage		−25	0	25	mV
V_{OSSS}	SS output offset voltage		−30	0	30	mV
I_{FSRU}	FSR output current		21	29	37	μA
I_{FSRD}			−32	−25	−8	μA

ELECTRICAL CHARACTERISTICS (V_{CC} = + 5V, V_{EE} = − 5V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{HSY}	SYSTEM RESET output valtage high	R_L = 20k Ω	4.0	4.9	−	V
V_{LSY}	SYSTEM RESET output valtage low	R_L = 20k Ω	−	0	0.2	V
I_{ALON}	ALPC SW "ON" output current		0.6	1.0	2.0	mA
I_{ALOF}	ALPC SW "OFF"output current		−10	0	10	μA

∗ 0dBm = 775mVrms

Note 1. Supply voltage turn on and pin ⑯ $\overline{ACLR}$ input reset pulse and next all parameter measures.



t_{RST} : 1 μs min

V_{HRST} : 2.5V min

V_{LRST} : 0.4V max

SETTING CURRENT VALUE OF INTERNAL CURRENT SOURCES

(Focus search (FSR), Tracking servo (TS), Slide motor servo (SS))

Current value of internal current sources (FSR,TS, SS) is set by an external resistor connected between pin ㉓ and Vcc. (Resistance value : Rx)

If the current value of a current source (FSR,TS, SS) is IFSR, ITS, ISS.

$$I_{FSR} \simeq \frac{1}{8} \cdot \frac{V_{CC} - V_{㉓}}{R_X}$$

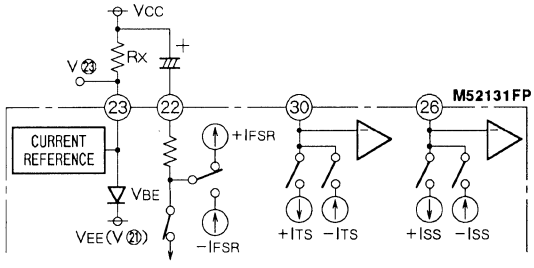
$$I_{TS} \simeq \frac{1}{8} \cdot \frac{V_{CC} - V_{㉓}}{R_X}$$

$$I_{SS} \simeq \frac{1}{4} \cdot \frac{V_{CC} - V_{㉓}}{R_X}$$

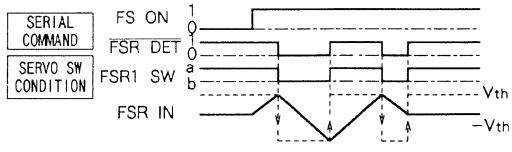
And if the voltage value of pin ㉑ is V ㉑, the voltage value of pin ㉓,

$V_{㉓} = V_{㉑} + V_{BE}$ ($V_{BE} \simeq 0.7V$)

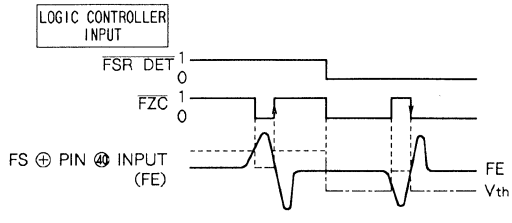
BLOCK DIAGRAM OF CURRENT SOURCES



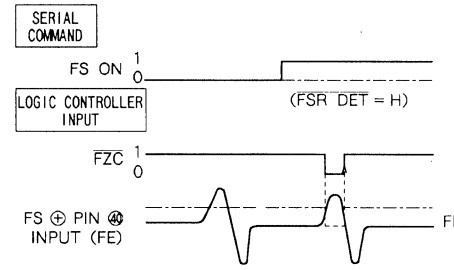
Timing chart of FSR Det



Timing chart of FZC



FZC reset



FSR detector

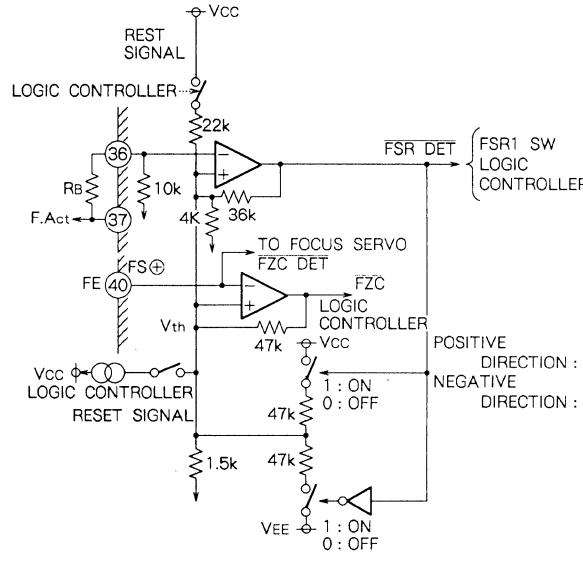
With external resistor (RB) connected between FS OUT (pin ㊲ output) and FSR IN (pin ㊱ input) at FSR function,

1) FSR direction,
2) Threshold voltage polarity of FZC detector are automatically changed.

Focus search always starts from positive voltage side. The direction of FSR is changed by FSR 1 SW controlled by $\overline{FSR\ DET}$ signal.

INPUT	OUTPUT		
FSR IN level VIN	$\overline{FSR\ DET}$	FSR1 SW	At ±5V FZC Vth
VIN > Vth	0	b : Negative direction of FSR	Min −0.30V / Max 0V
VIN < Vth	1	a : Positive direction of FSR	0V 0.30V

Equivalent circuit



M52131FP LOGIC CONTROL FUNCTION DESCRIPTION

1. Serial command function

The M52131FP has a 8-bit shift resister in the logic control Block to convert serial data from microcomputer input through MSD pin ⑬, to internal switch commands.

(1) Data-Input function

Higher 4 bits of the 8-bit data (D_7~D_4) are used to select the command mode. Lower 4 bits (D_3~D_0) set the command state.

Once a command is set, it is held until a new command of the same command mode is input. If an other command mode is selected the command state will not change.

Table 1. Serial command function

× = 1 or 0

Mode name	MSB ↓ Mode select				Data in pin ⑬ input: Command state ↓ LSB				Data out pin ⑪ output
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
FOCUS	0	0	0	0	FS ON	×	$\overline{\text{FSR EN}}$	×	FS OK
TRACK1 A	0	0	0	1	×	BRAKE A	TG2	TG1	0
TRACK1 B			1		×	BRAKE B			
TRACK2	0	0	1	0	TRACK		SLIDE		TC
SERVO OFF	0	1	×	×	×	×	×	×	0
STOP	1	1	×	×	×	×	×	×	0

Note 2. TRACK1 A and TRACK1 B at the same command mode.
TG2 and TG1 are set by both commands. BRAKE A or B are determined by selecting TRACK1 A or TRACK1 B.
3. Data out (pin ⑪ output) is changed automatically when the command mode is selected.
4. The serial command 10XXXXXX is available of control M50422P/M50423FP/M50427FP/M65820FP (DSP LSI). When this command input, the command state of M52131FP is not changed.

Table 2. Command functions

Command	Command mode	Data			Function
FS ON	FOCUS	D_3	1	ON	Focus search start→ Focus on
			0	OFF	
$\overline{\text{FSR EN}}$	↑	D_1	1	INHIBIT	Inhibit automatic re-search of focus
			0	ENABLE	
BRAKE A	TRACK1 A	D_2	1	ON	Jump break action. TS2 SW is opened or closed.
			0	OFF	
BRAKE B	TRACK1 B	D_2	1	ON	Jump break action. TS1 SW is opened or closed.
			0	OFF	
TG2	TRACK1	D_1	1	OPEN	TG2 SW for changing TRACK gain is controlled.
			0	CLOSE	
TG1	TRACK1	D_0	1	OPEN	TG1 SW for changing TRACK gain is controlled.
			0	CLOSE	
TRACK	TRACK2	D_3	D_2		SW states shown in Table 4.
		0	0	TS OFF	Track servo off
		0	1	TS ON	Track servo on
		1	0	JF	Forward jump
		1	1	JR	Reverse jump
SLIDE	TRACK2	D_1	D_0		SW states shown in Table 5.
		0	0	SS OFF	Slide servo off
		0	1	SS ON	Slide servo on
		1	0	SF	Forward slide
		1	1	SR	Reverse slide
–	SERVO OFF				Data of D_0~D_3 is reset to 0
–	STOP				Data of D_0~D_3 is reset to 0

(2) How to send serial data (MSD)

The serial command is executed by sending $\overline{MLA}$ signal after sending LSB serial data.

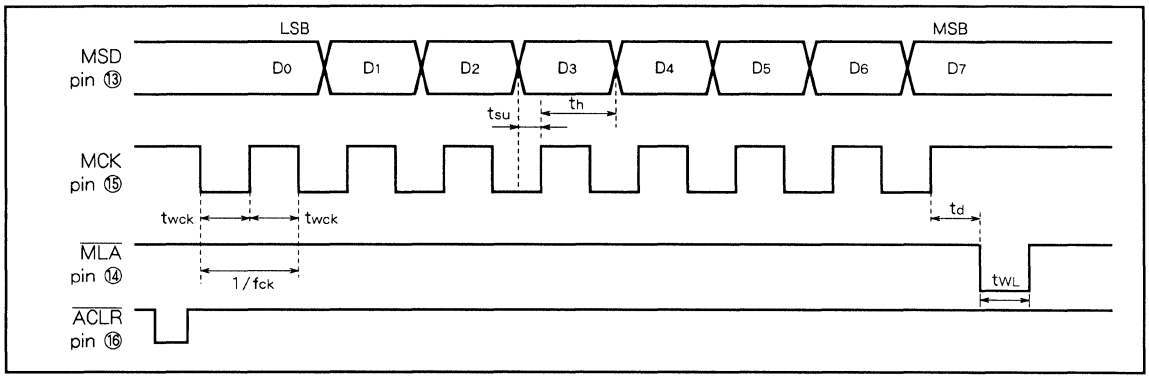


Fig. 1 Serial data input timing chart

2. BRAKE A, BRAKE B

When BRAKE A command or BRAKE B command is set to High (1), Jump Brake operates.

This increases the ability to break after track jump.

Jump brake action

1) When MR (pin ⑥ input) = 1, Track servo loop goes off at the edge of pulse output from TC Det.
2) When MR (pin ⑥ input) = 0, Track servo loop goes on at the edge of pulse output from TC Det.

Table 3. SW states at jump brake

INPUT	OUTPUT	
MR $\overline{TC}$	BRAKE A = 1 TS2 SW states	BRAKE B = 1 TS1 SW states
1 ⌐¬ 0 ⌐¬	a (TRACK servo OFF) b (TRACK servo ON)	b (TRACK servo OFF) a (TRACK servo ON)

3. TRACK, SLIDE

Table 4. Track function

INPUT			OUTPUT (SW state)			
Command	Data					
	D_3	D_2	TS1 SW	TS2 SW	JF SW	JR SW
TS OFF	0	0	a (servo ON)	a (servo OFF)	b	b
TS ON	0	1	a (servo ON)	b (servo ON)	b	b
JF	1	0	b (servo OFF)	b (servo ON)	a (JF ON)	b
JR	1	1	b (servo OFF)	b (servo ON)	b	a (JR ON)

Table 5. Slide function

INPUT			OUTPUT (SW state)		
Command	Data				
	D_1	D_0	SS SW	SF SW	SR SW
SS OFF	0	0	a (servo OFF)	b	b
SS ON	0	1	b (servo ON)	b	b
SF	1	0	a (servo OFF)	a (SF ON)	b
SR	1	1	a (servo OFF)	b	a (SR ON)

4. Direct command function

(1) $\overline{JP1}$ input

At one track jump, $\overline{JP1}$ signal allwes two transmissions of serial data to selected and restrains the delay time of microcomputer.

$\overline{JP1}$ is usually high. After microcomputer catches the up signal of Data out output (TC singnal), if $\overline{JP1}$ goes down, the polarity of jump direction is automatically. (JF→JR, JR →JF)

After noe track jump is finished (after period T3), if $\overline{JP1}$ goes up, Jump ends and the states become TS ON and SS ON.

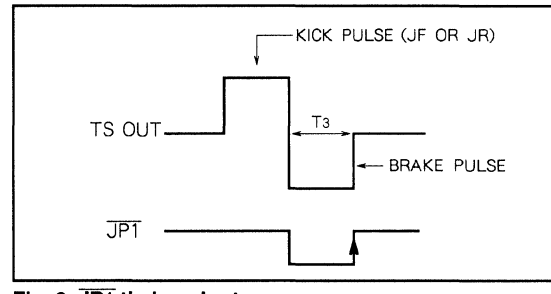


Fig. 2 $\overline{JP1}$ timing chart

Table 6. TRACK, SLIDE states by $\overline{JP1}$ Input

$\overline{JP1}$ (INPUT)	TRACK2 Mode (0 0 1 0 D_3 D_2 D_1 D_0) (OUTPUT)							
	TRACK (D_3 D_2)				SLIDE (D_1 D_0)			
	00	01	10	11	00	01	10	11
1	TS OFF	TS ON	JF	JR	SS OFF	SS ON	SF	SR
0	TS OFF	TS ON	JR	JF	SS OFF	SS ON	SF	SR
↑	TS OFF	TS ON	TS ON	TS ON	SS ON	SS ON	SF	SR

Note 5. When command mode is TS OFF (001000XX, MSB first), even if $\overline{JP1}$ goes up, states do not become TS ON and SS ON.
6. Change to TS ON and SS ON after $\overline{JP1}$ goes up are held.

5. Logoc output function

(1) Data out

Data out output mode changes at each serial command mode.(shown in table 1) It is decided by the last sent serial command.

Table 7. Data out output function

	Data Out output name	Serial Command Mode(INPUT)
(I)	FS OK	FOCUS (0000XXXX)
(II)	TC	TRACK2 (0010XXXX)

(I) FS OK

When HF OK (pin ⑧ Input) was high and FS SW was closed (servo ON), FS OK is high.

Table 8. FS OK truth

INPUT		OUTPUT
HF OK	FS SW	FS OK
0	b (servo OFF)	0
1	b (servo OFF)	0
0	a (servo ON)	0
1	a (servo ON)	1

Note 7. While FS OK is Low, TS2 SW and SS SW are opened regardless of the Serial Command.

(II) TC

TC pulse is producted by latching MR pulse with pulse edges of TC Det output ($\overline{TC}$). At reset, TC is low.

Table 9. TC output

INPUT		OUTPUT
MR	$\overline{TC}$	TC
1	↑ or ↓	1
0	↑ or ↓	0

(2) $\overline{\text{HFD}}$ (HF defect)

Output is High when HF OK is Low.

(3) Jump flag

Jump flag terminal outputs ; High when serial command is TS OFF or JF or JR or BRAKE. Outputs is low at other times.

6. Focus error amp

This Amp is Auxiliary.

7. APC switch

The APC circuit supply is controlled by this switch.

8. System reset

This circuit generates the reset pulse at power-on.

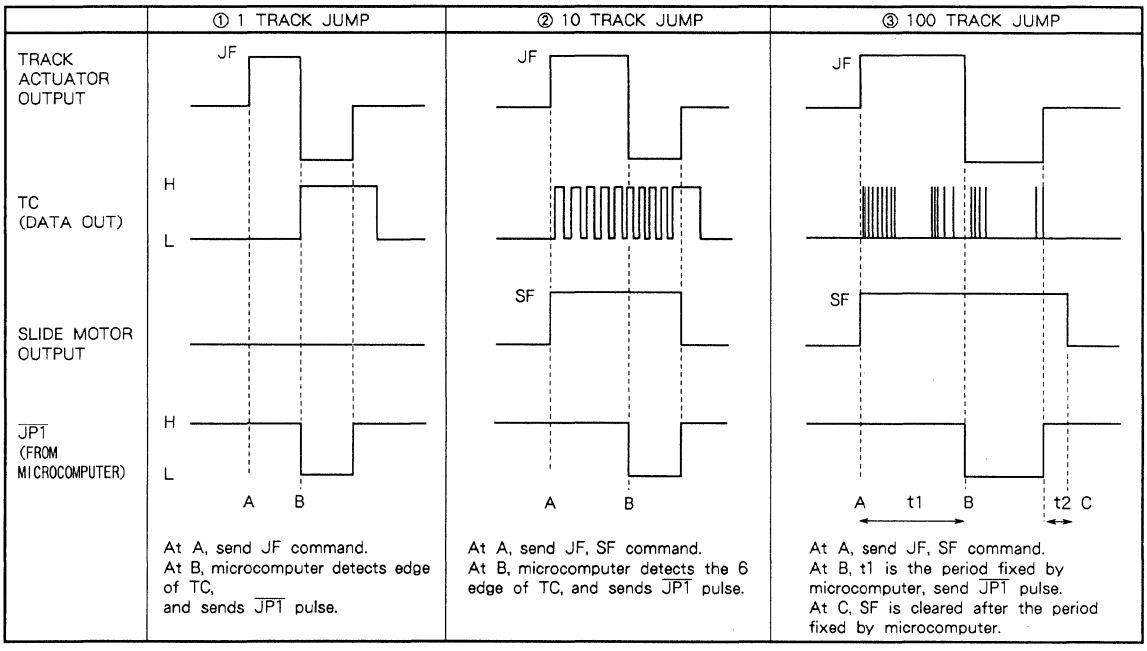
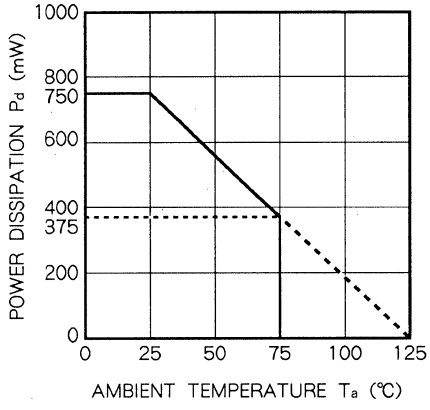


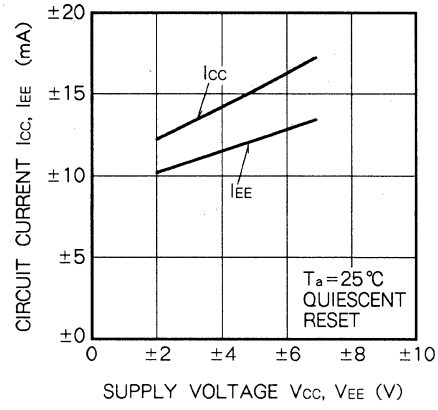
Fig. 3 Example for track jump timing. (Forward jump)

TYPICAL CHARACTERISTICS

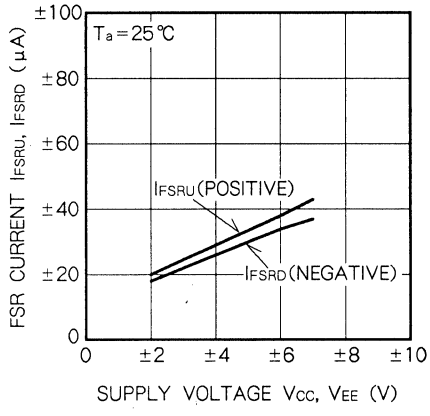
THERMAL DERATING (MAXIMUM RATING)



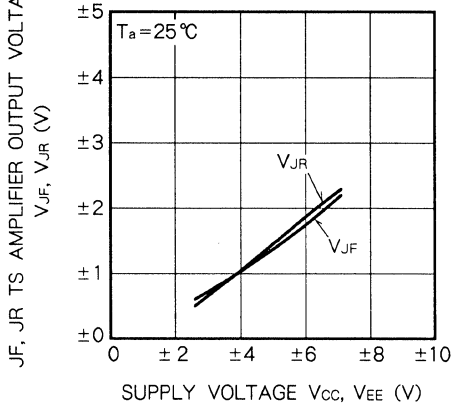
QUIESCENT CIRCUIT CURRENT VS. SUPPLY VOLTAGE



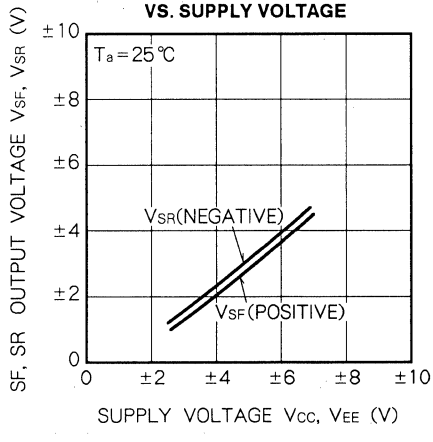
FSR CURRENT VS. SUPPLY VOLTAGE



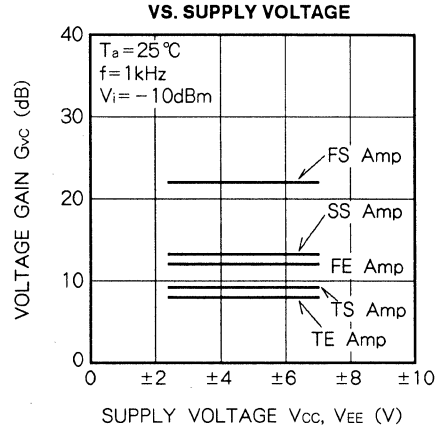
JF, JR, TS AMPLIFIER OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



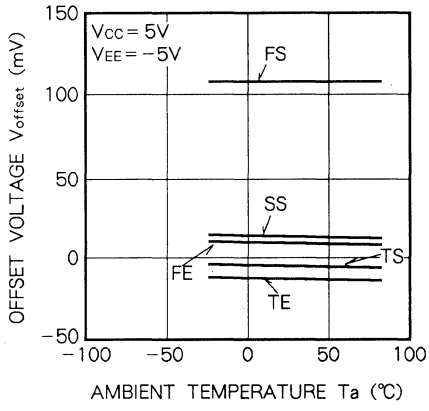
SF, SR OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



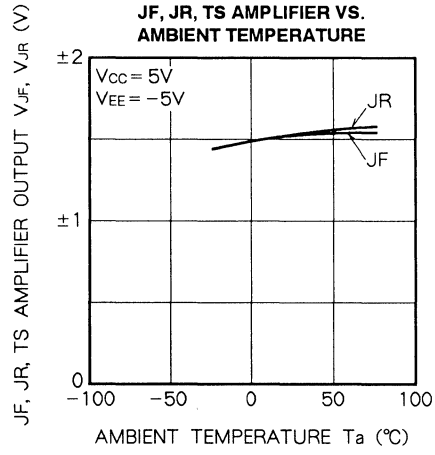
EACH AMPLIFIER VOLTAGE GAIN VS. SUPPLY VOLTAGE



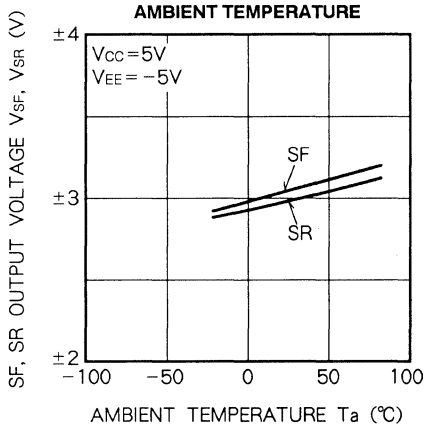
AMPLIFIER OFFSET VOLTAGES VS. AMBIENT TEMPERATURE



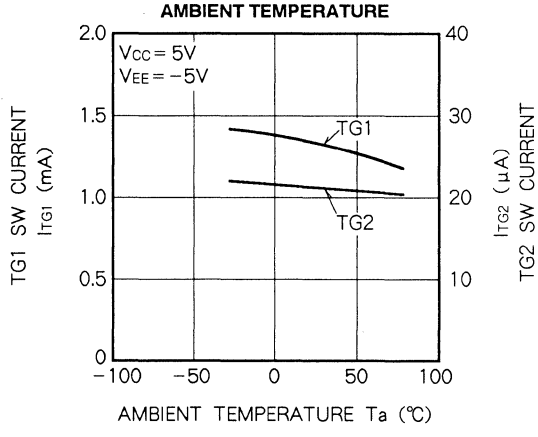
JF, JR, TS AMPLIFIER VS. AMBIENT TEMPERATURE



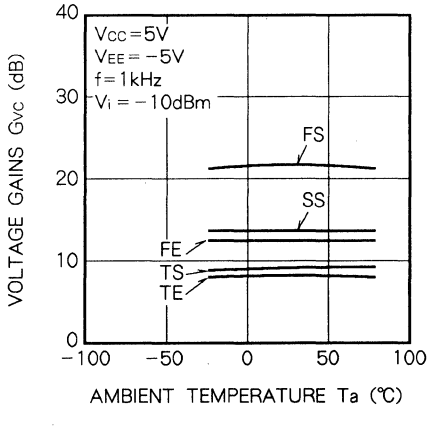
SF, SR OUTPUT VOLTEGE VS. AMBIENT TEMPERATURE



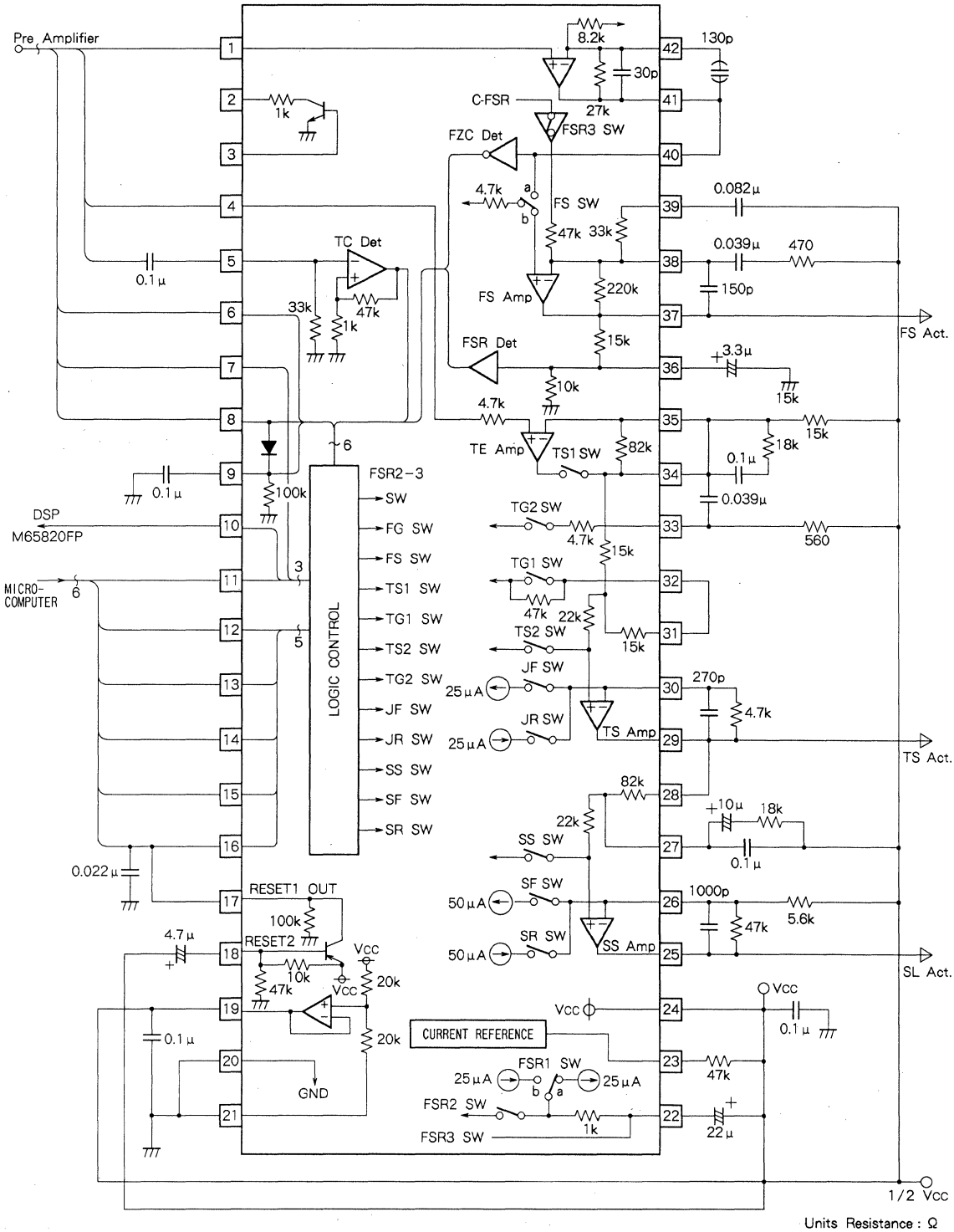
TG1, TG2 CURRENT VS. AMBIENT TEMPERATURE



AMPLIFIER VOLTAGE GAINS VS. AMBIENT TEMPERATURE



APPLICATION EXAMPLE (V_{CC} = + 5V, V_{EE} = − 5V)



Units Resistance : Ω
Capacitance : F

MITSUBISHI ELECTRIC

M51565P

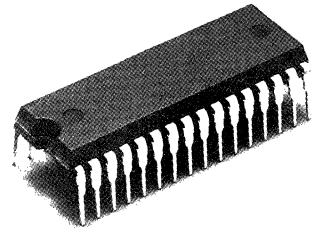
ANALOG OUTPUT AMPLIFIER FOR CD PLAYER

DESCRIPTION

The M51565FP is a semiconductor integrated circuit developed as an analog output amp for use in combination with a D/A converter for digital audio applications such as CD players.

FEATURES

- Combination with D/A converter produces analog output of low distortion
- Built-in driver circuit makes it possible to drive each switch with input of small bias current
- Includes high-speed switch driver for use at sampling frequency 88.2kHz



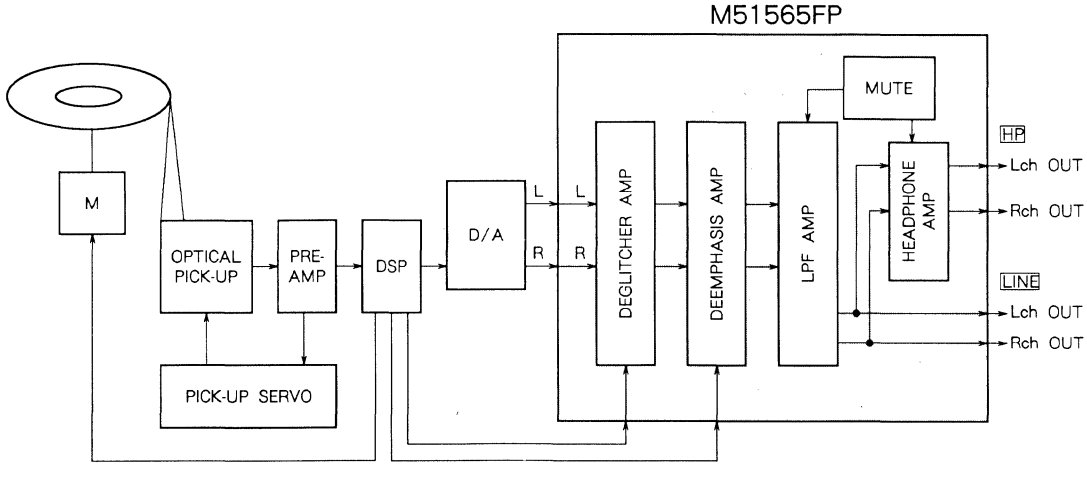
Outline 32P4B

1.778mm pitch 400mil SDIP
(8.9mm × 28.0mm × 3.8mm)

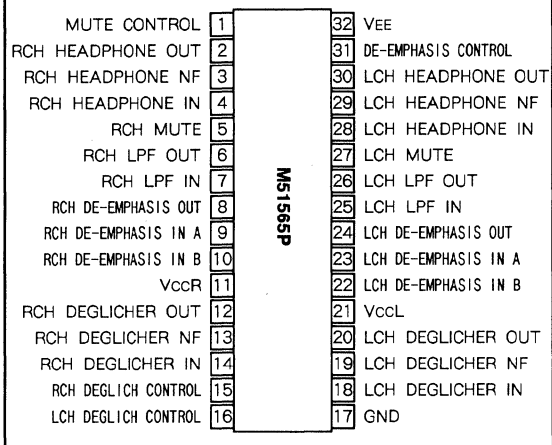
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC}, V_{EE} = ± 4.5~± 5.5V
Rated supply voltage ..... V_{CC}, V_{EE} = ± 5V
Rated power dissipation 215mW

SYSTEM CONFIGURATION

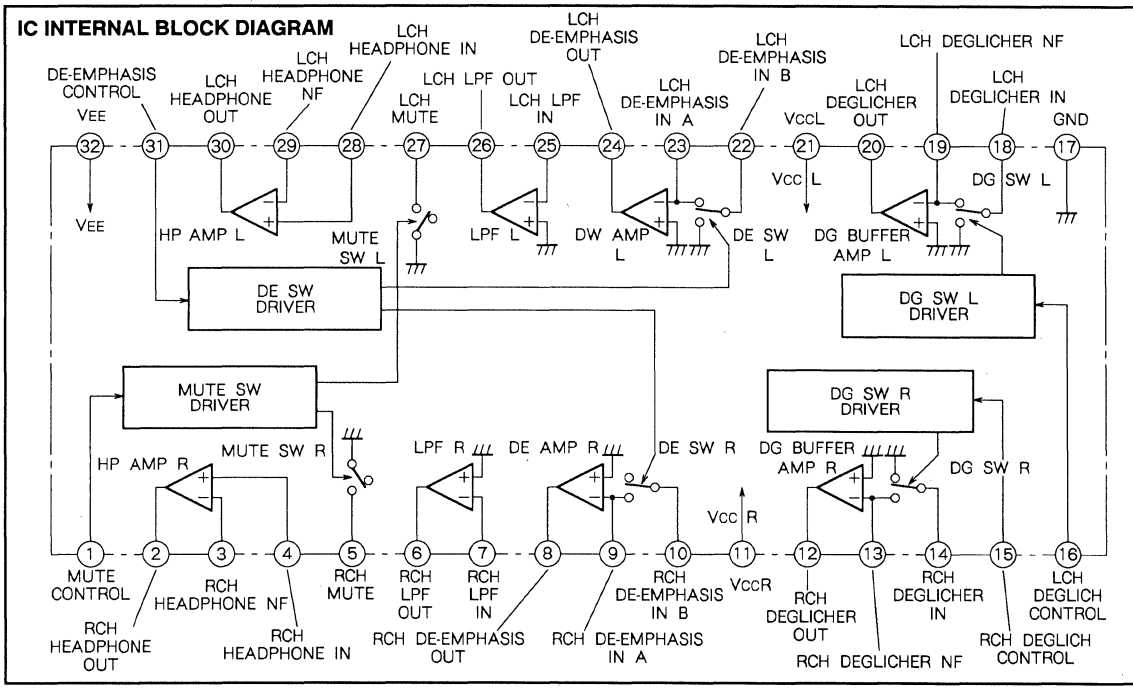


PIN CONFIGURATION



Outline 32P4B

IC INTERNAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

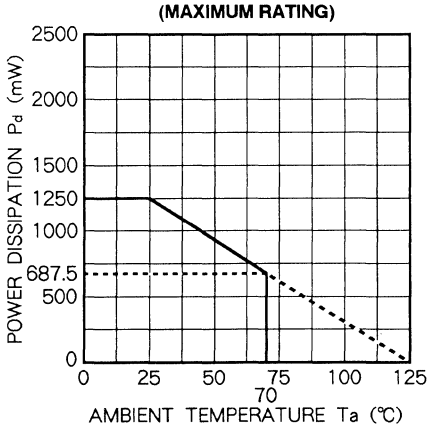
Symbol	Parameter	Ratings	Unit
V_{CC}-V_{EE}	Supply voltage	11	V
I_{CC}, I_{EE}	Circuit current	100	mA
P_d	Power dissipation	1250	mW
K_θ	Thermal derating	12.5	mW/℃
T_{opr}	Operating temperature	−20～+70	℃
T_{stg}	Storage temperature	−40～+125	℃

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{EE} = − 5V, Ta = 25℃, unless otherwise noted)

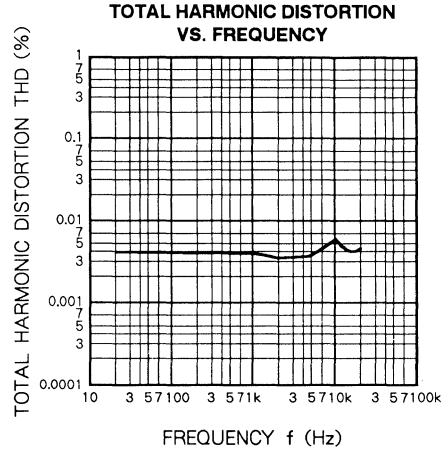
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC}	Circuit current1		I_{CCL} + I_{CCR}, zero input signal	14	43	70	mA
I_{EE}	Circuit current2		zero input signal	− 65	− 40	−12	mA
THD	Line out	Total harmonic distortion	f = 1kHz, full scale, fs = 88.2kHz	−	0.004	0.009	%
S/N	Line out	Signal/noise ratio	JIS-A, f = 1kHz, full scale, fs = 88.2kHz	85	96	−	dB
CS	Line out	Channel seperation	f = 1kHz, full scale, fs = 88.2kHz	70	83	−	dB
ATT	Line out	Mute attenuation	f = 1kHz, full scale, fs = 88.2kHz	6	18	−	dB
V_{OHPMAX}	Headphone amplifier Maximun output voltage		f=1kHz, THD=3%, R_L=30Ω, Gv=20dB, Rs(short circuit protection resistor)=150Ω	0.20	0.33	−	Vrms
I_{BDG}	DG SW bias current		Vin = 5V, pin⑮, ⑯,	−	10	50	μA
V_{IH}	High level input voltage		pin ①, ⑮, ⑯, ㉛	3	−	5	V
V_{IL}	Low level input voltage		pin ①, ⑮, ⑯, ㉛	0	−	1.5	V

TYPICAL CHARACTERISTICS

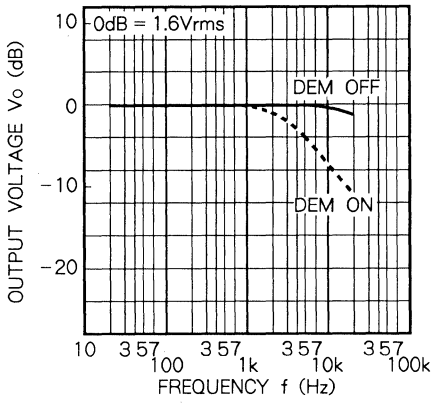
THERMAL DERATING (MAXIMUM RATING)



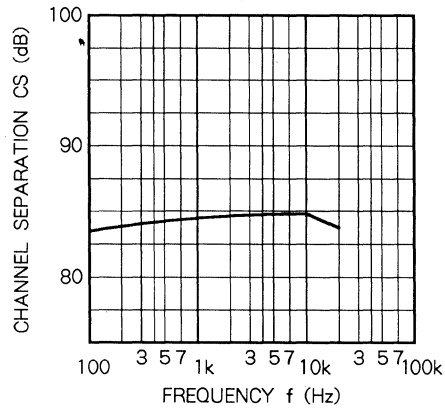
TOTAL HARMONIC DISTORTION VS. FREQUENCY



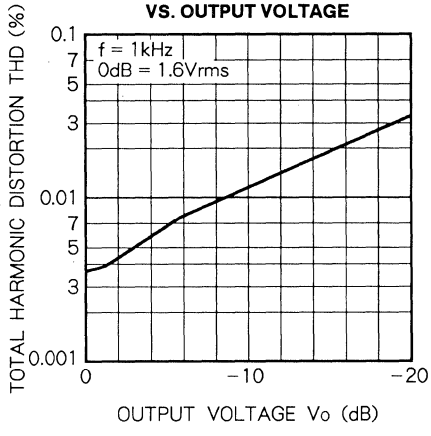
OUTPUT VOLTAGE VS. FREQUENCY



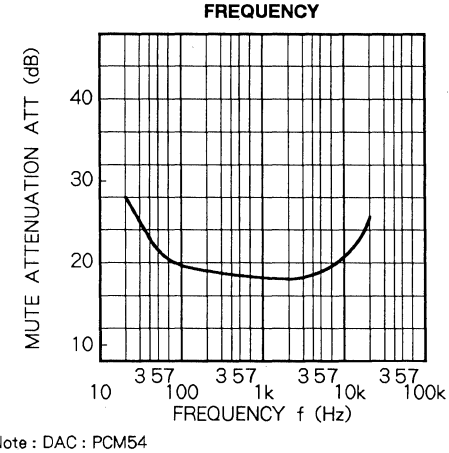
CHANNEL SEPARATION VS. FREQUENCY



TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



MUTE ATTENUATION VS. FREQUENCY

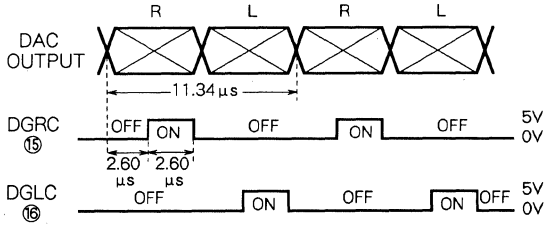


Note : DAC : PCM54
Digital filter : SM5806
Signal processing IC : CX23035
(Application Example 2)

FUNCTIONAL DESCRIPTION

1. Deglicher (DG)

The deglicher consists of analog switch, switch driver and buffer and deglich DAC output. The switch is ON when control signal of pin ⑮ or ⑯.



DEGLICHER TIMING EXAMPLE (fs = 88.2kHz)

2. De-emphasis (DE)

The de-emphasis circuit consists of analog switch, switch driver and OP amp. De-emphasis characteristics on set by the external feedback impedance. The de-emphasis characteristics are changed by the switch is ON when control signal of pin ㉛ is High.

3. Low pass filter (LPF)

The Active LPF consists of inverted amplifier, external resistors and external capacitors.

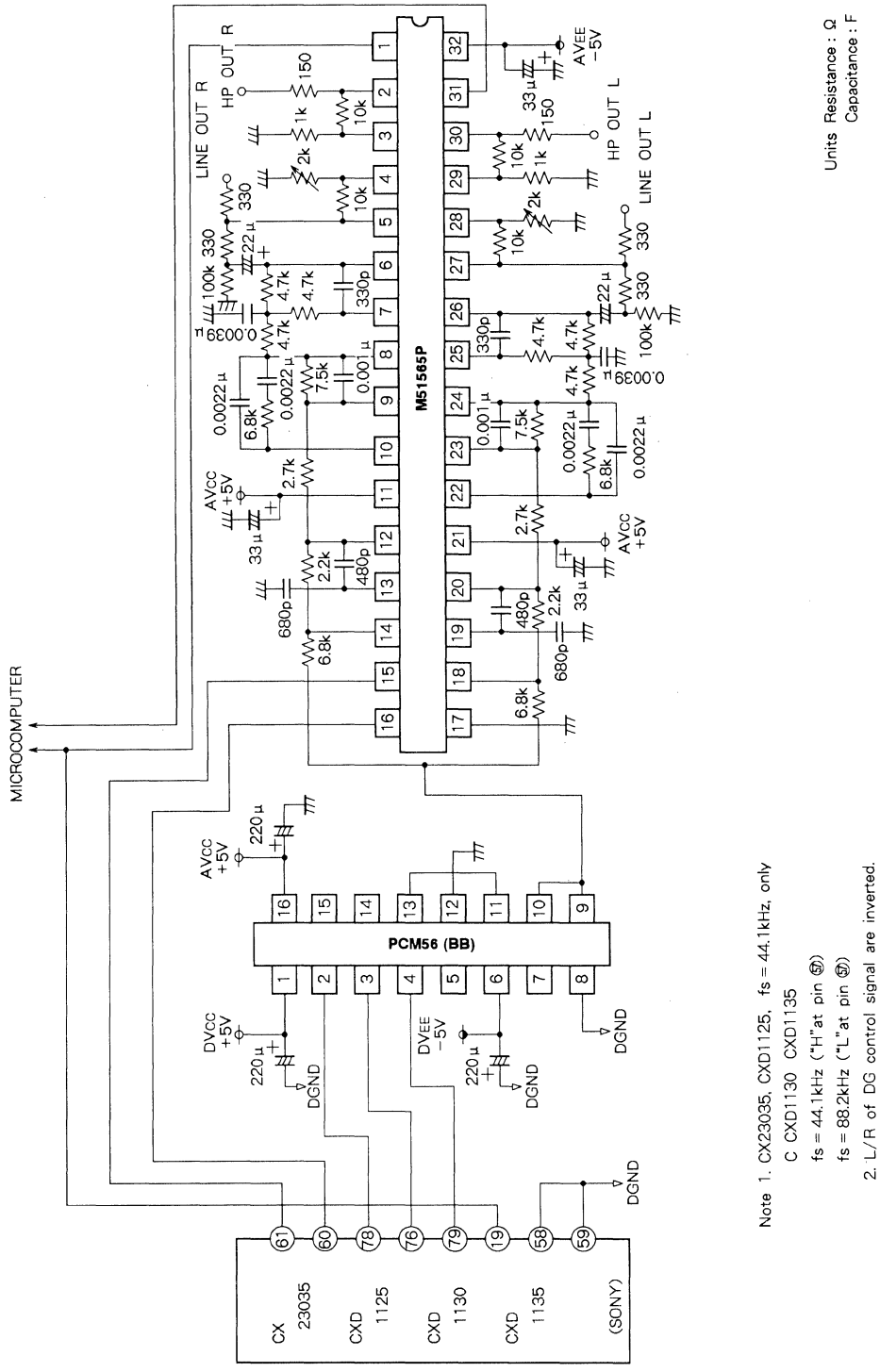
4. Output mute (MUTE)

The output mute circuit operates when the line connected to the output of LPF is grounded by the internal switch. The output mute circuit is ON when control signal of pin ① is High.

5. Headphone amplifier (HP)

The amplifier is for the headphone use and gain is adjustable by the external circuit.

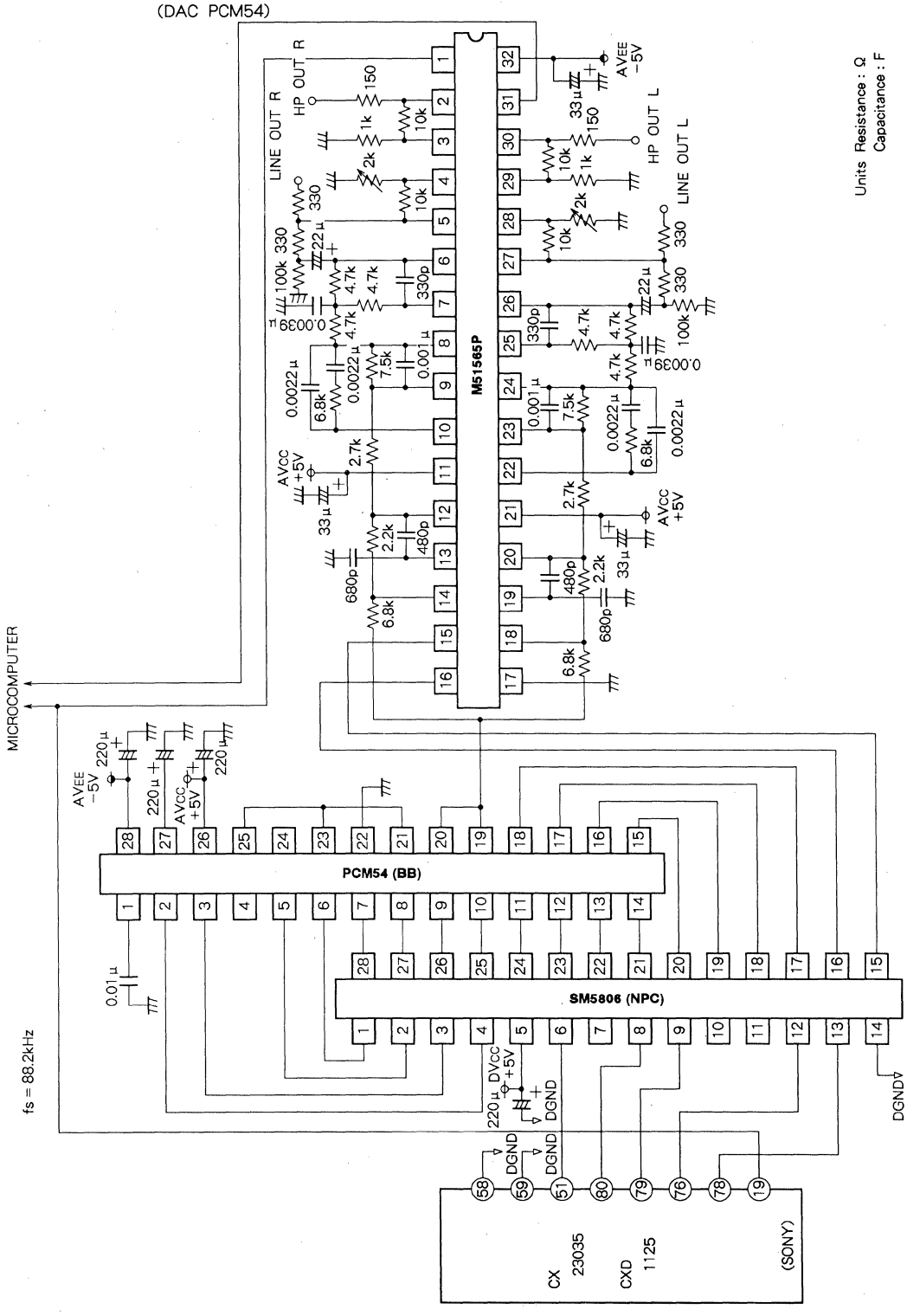
APPLICATION EXAMPLE 1 (Signal Processing IC CX23035/CXD1125/CXD1130/CXD1135) (DAC PCM56)



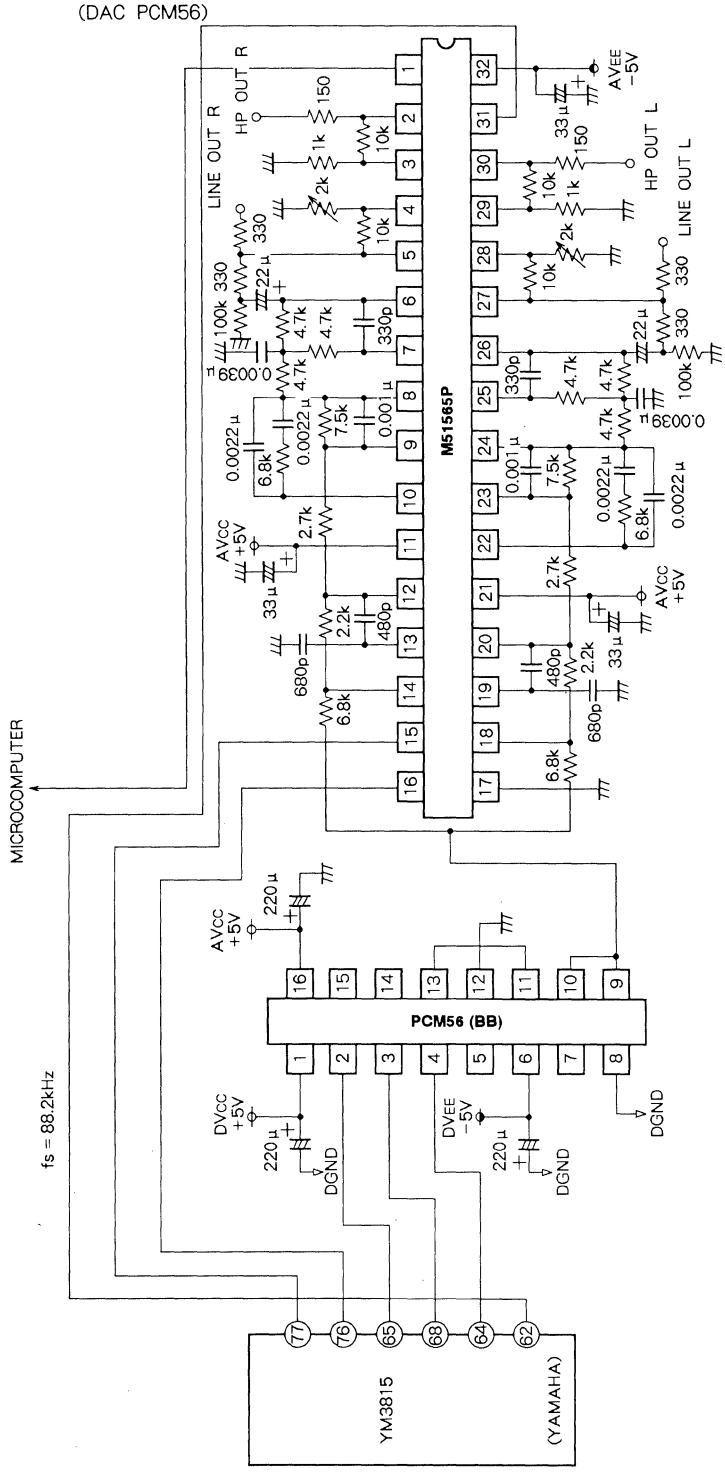
Units Resistance : Ω
Capacitance : F

Note 1. CX23035, CXD1125, fs = 44.1kHz, only
C CXD1130 CXD1135
fs = 44.1kHz ("H" at pin ㊲)
fs = 88.2kHz ("L" at pin ㊲)
2. L/R of DG control signal are inverted.

APPLICATION EXAMPLE 2 (Signal Processing IC CX23035 CXD1125, Digital filter SM5806) (DAC PCM54)

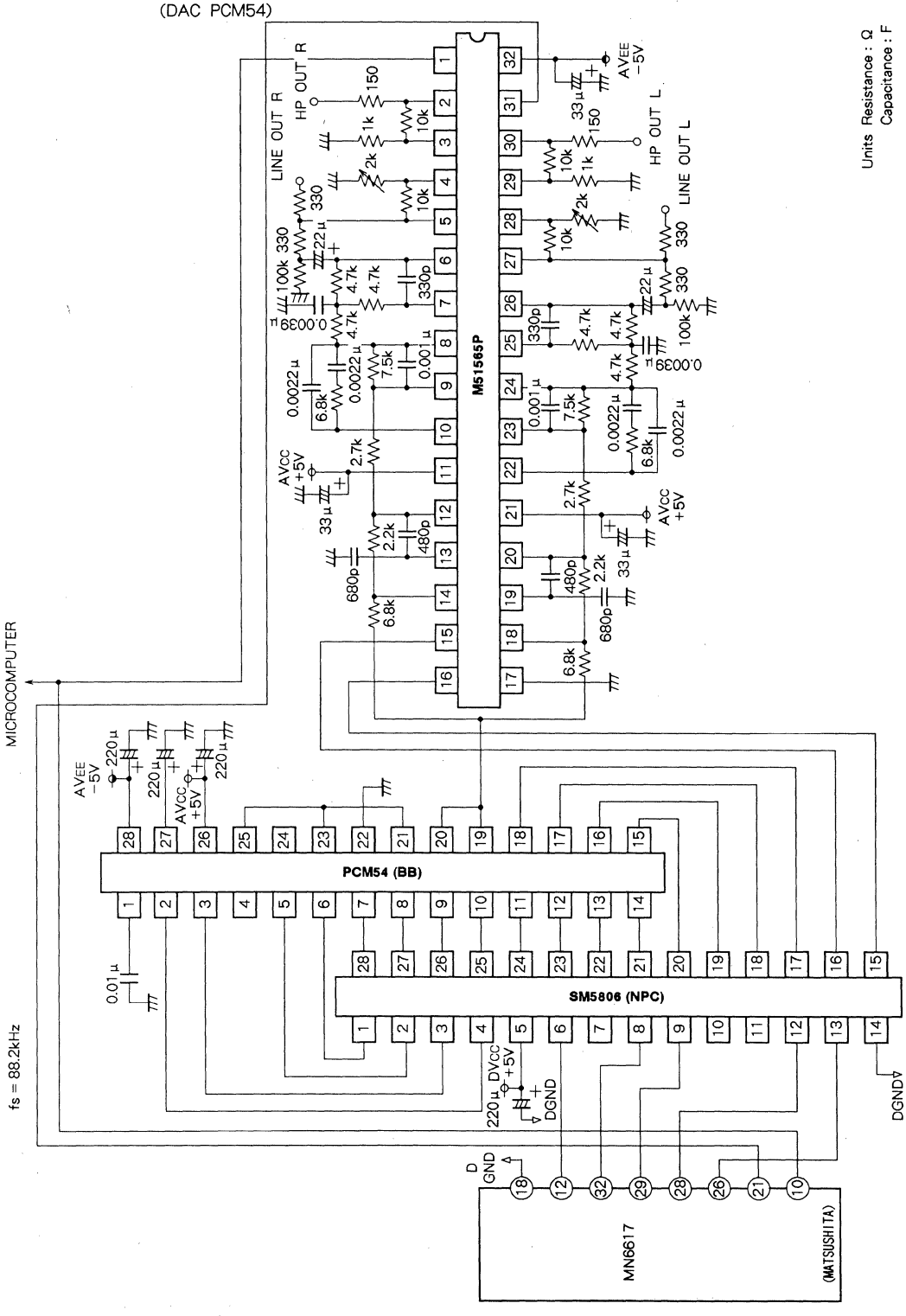


APPLICATION EXAMPLE 3 (Signal Processing IC YM3815)
(DAC PCM56)



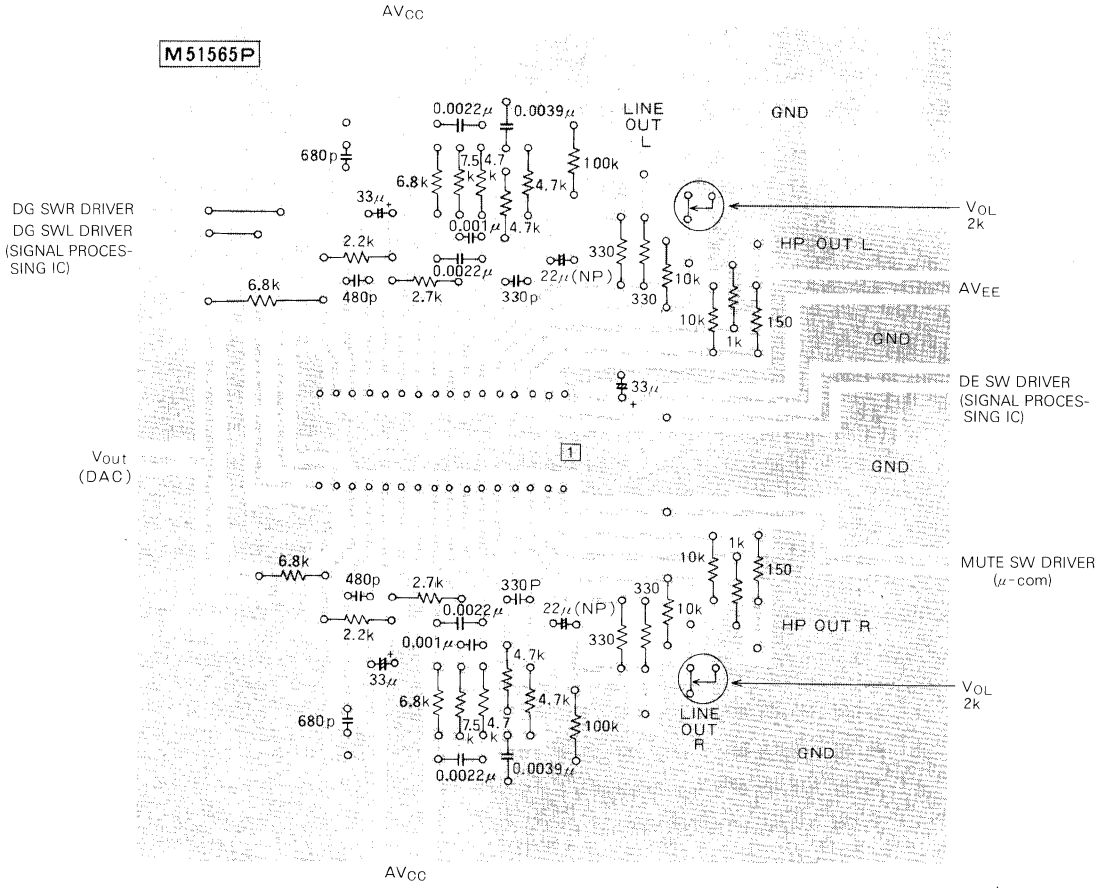
Units Resistance : Ω
Capacitance : F

APPLICATION EXAMPLE 4 (Signal Processing IC MN6617 Digital filter SM5806) (DAC PCM54)



MITSUBISHI ELECTRIC

PRINTED CIRCUIT BOARD LAYOUT : (Foil side)



Note) ● M51565P and DAC are placed nearly as possible.
● Control line pattern of DG SW driver is shielded from other analog system by the ground.

Units Resistance : Ω
Capacitance : F

M51568FP

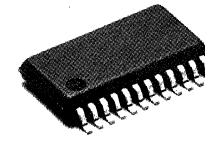
ANALOG OUTPUT AMPLIFIER FOR CD PLAYER

DESCRIPTION

The M51568FP is a semiconductor integrated circuit developed as an analog output amp for digital audio applications such as CD players. It has a built-in headphone amp, its applications include portable apparatuses.

FEATURES

- Low circuit current ..... 6.3mA typ (V_{CC} = 5V)
- Low distortion ..... 0.0012% typ (f = 1kHz)
- Low noise ..... No = 8μVrms typ (JIS-A)
- High power Headphone Amp ..... Po = 13mW typ (V_{CC} = 5.0V, $R_O + R_L$ = 27Ω + 32Ω)



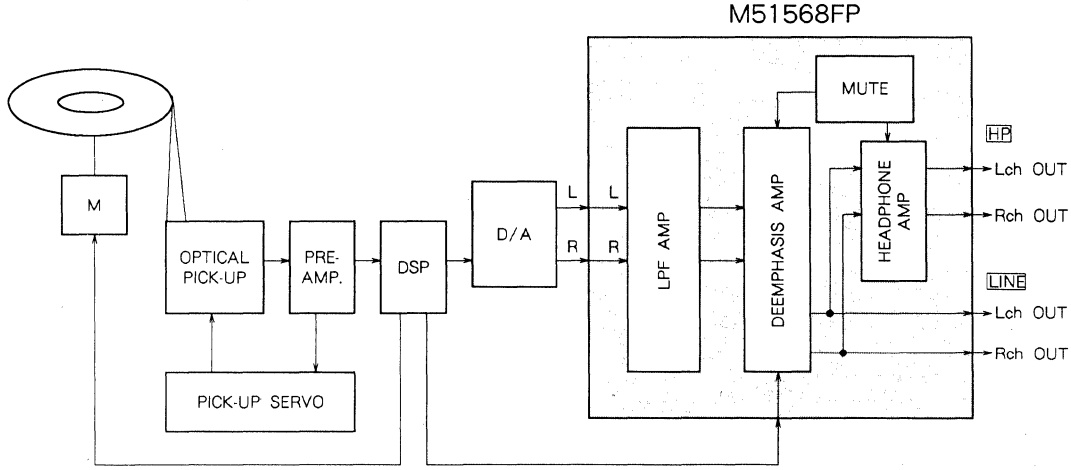
Outline 24P2Q-A

0.8mm pitch 300mil SSOP
(5.3mm × 10.1mm × 1.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 3~5.5V
Rated supply voltage ..... V_{CC} = 5V
Rated power dissipation 31.5mW

SYSTEM CONFIGURATION

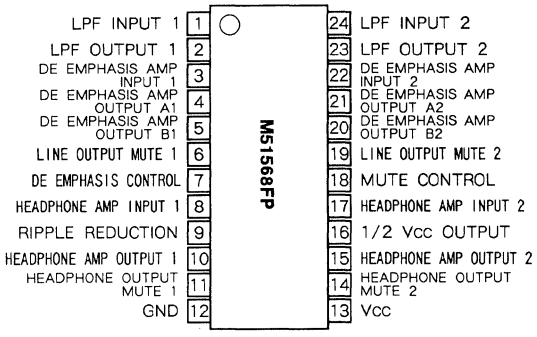


MITSUBISHI ELECTRIC

M51568FP

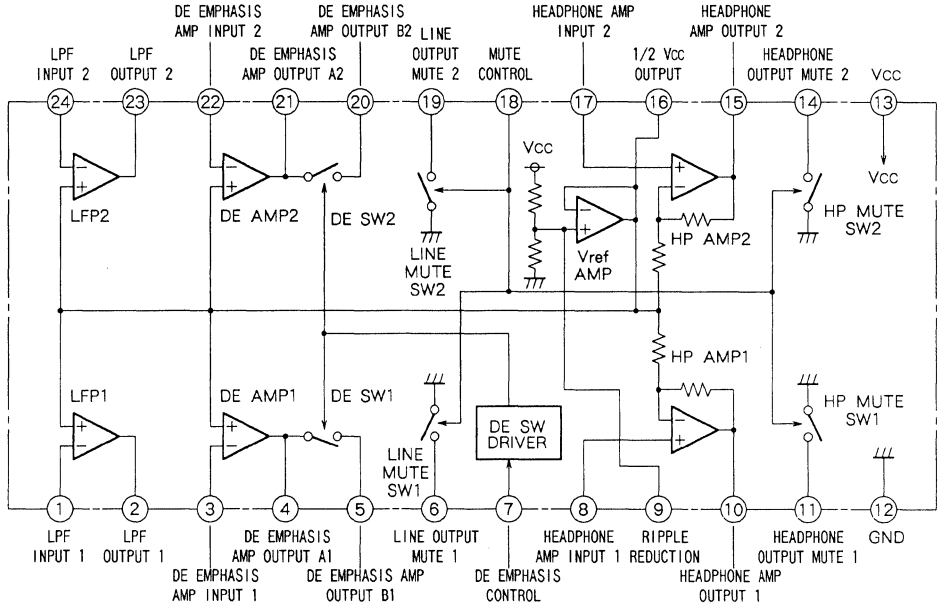
ANALOG OUTPUT AMPLIFIER FOR CD PLAYER

PIN CONFIGURATION



Outline 24P2Q-A

IC INTERNAL BLOCK DIAGRAM



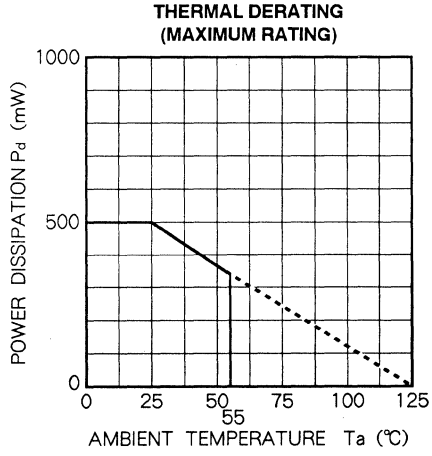
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted.)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6	V
P_d	Power dissipation	500	mW
K_θ	Thermal derating	5	mW/℃
T_{opr}	Operating temperature	− 20 ~ + 55	℃
T_{stg}	Storage temperature	− 40 ~ + 125	℃

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Ta = 25℃, LINE OUT : R_L = 10k Ω)

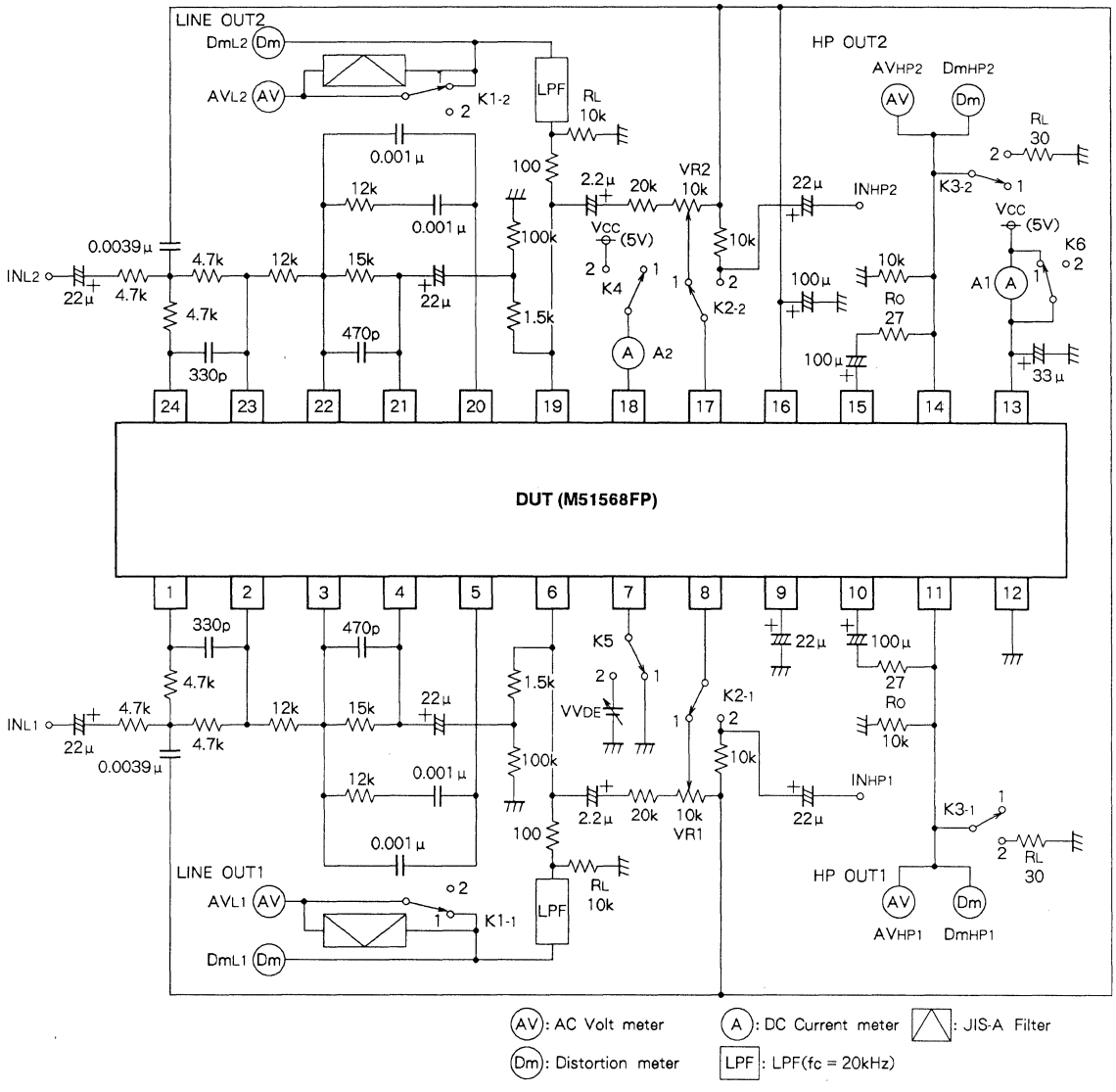
Symbol		Parameter	Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC}		Circuit Current	Quiescent	−	6.3	16	mA
THD	LINE OUT	Total harmonic distortion	f = 1kHz, V_{in} = 750mVrms	−	0.0012	0.006	%
S/N	LINE OUT	Signal/Noise Ratio	JIS-A S : f = 1kHz V_{in} = 750mVrms	85	100	−	dB
CS	LINE OUT	Channel Separation	f = 1kHz, V_{in} = 750mVrms V_{OHP} = 245mVrms	70	85	−	dB
ATT_L	LINE OUT	Mute Attenuation	f = 1kHz, V_{in} = 750mVrms, pin ⑱ = 5V, Ro (short circuit protection resistor) = 1.5k Ω	35	45	−	dB
G_{VHP}	HP OUT	Voltage Gain	f = 2kHz, V_{in} = 47mVrms, R_L = 57 Ω,	17	20	23	dB
V_{OHPmax}	HP OUT	Headphone Amplifier Maximum output voltage	f = 1kHz, THD = 10%, R_L = 30 Ω Ro(short circuit protection resistor) = 27Ω	0.4	0.62	−	Vrms
ATT_{HP}	HP OUT	Mute Attenuation	f = 1kHz, V_{in} = 47mVrms, Ro(short circuit protection resistor) = 27Ω R_L = 30Ω, pin ⑱ = 5V	45	57	−	dB
I_{BM}		Mute control bias current	V_{in} = 5V, pin ⑱	−	13	20	mA
V_{THDE}		De-emphasis control threshold level	pin ⑦	0.9	1.4	1.9	V

TYPICAL CHARACTERISTICS



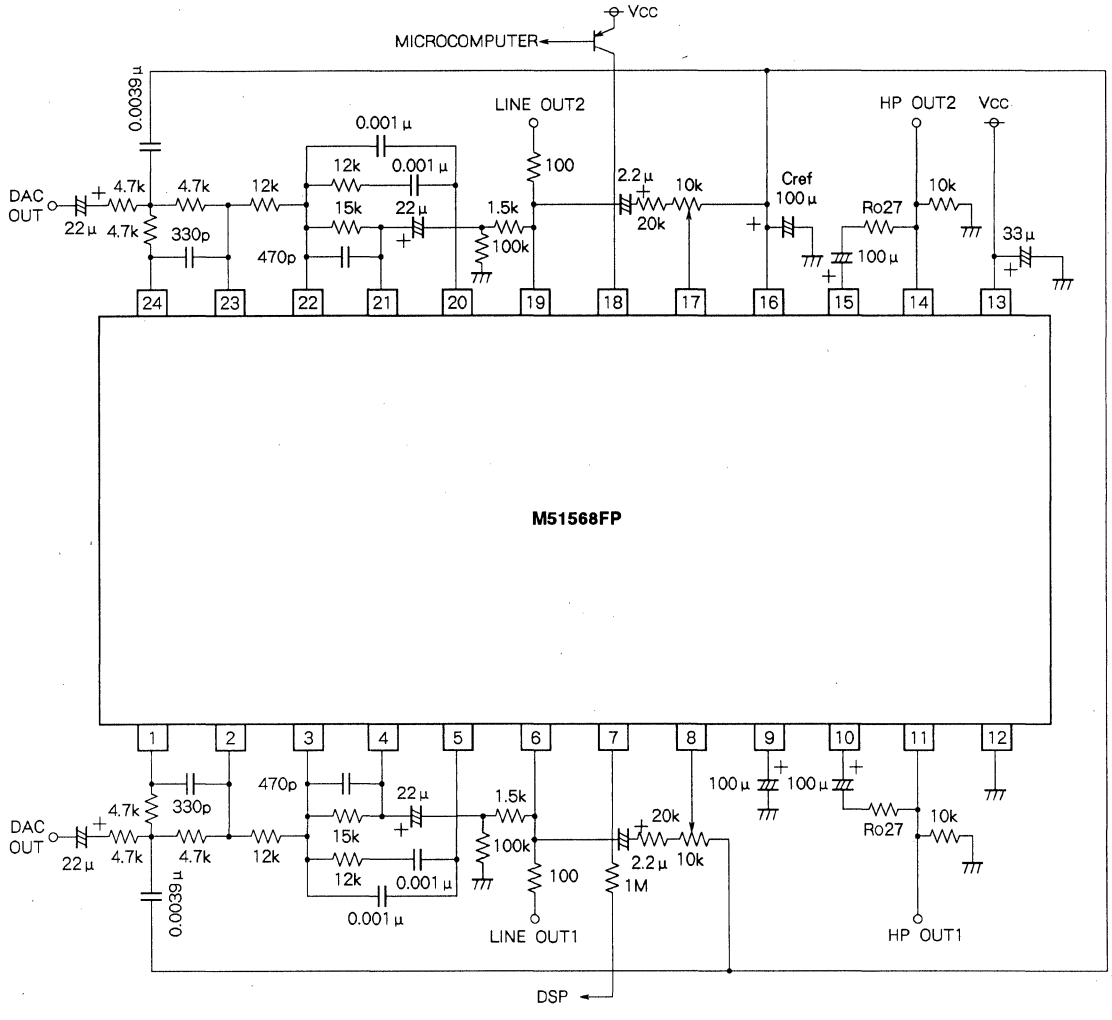
MITSUBISHI ELECTRIC

TEST CIRCUIT



Units Resistance : Ω
Capacitance : F

APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

M51590FP

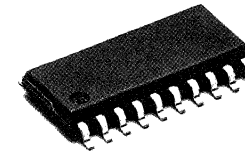
ANALOG OUTPUT AMPLIFIER FOR CD PLAYER

DESCRIPTION

The M51590FP is a semiconductor integrated circuit developed as an analog output amp for digital audio applications such as CD players. It has a built-in buffer amp so that it is capable of being used for a high-output impedance DAC.

FEATURES

- Supports high-output impedance DAC (buffer amp built-in)
- Low current dissipation ..... 5.1mA typ.(V_{CC} = 9V)
- Low distortion ..... 0.001 % typ.(f = 1kHz)



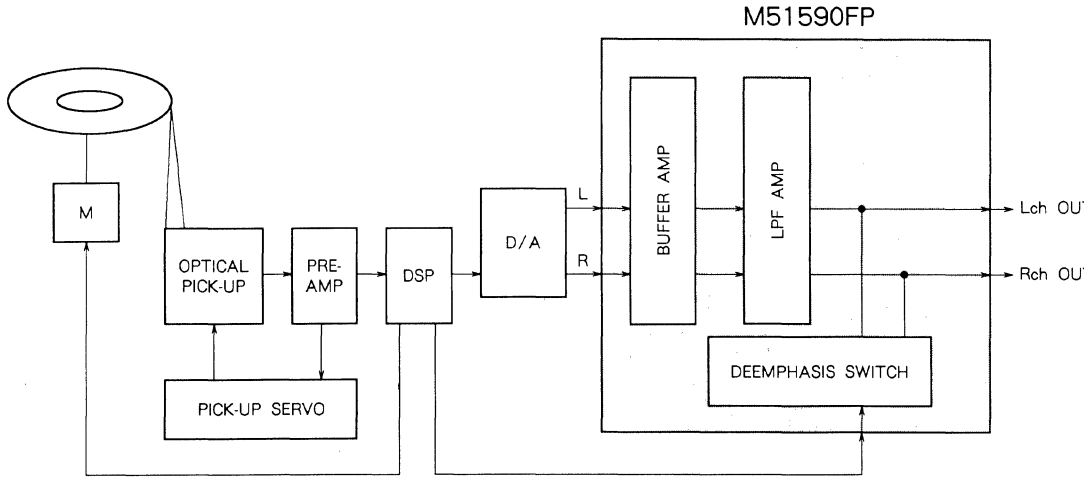
Outline 20P2N-A

1.27mm pitch 300mil SOP
(5.3mm × 12.6mm × 1.8mm)

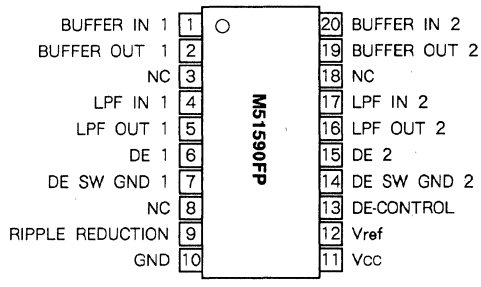
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 3~12V
Rated supply voltage ..... V_{CC} = 9V
Rated power dissipation 46mW

SYSTEM CONFIGURATION



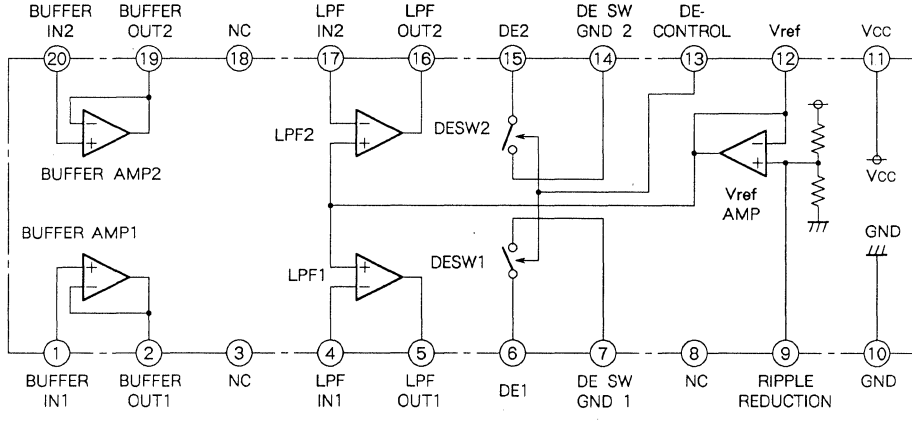
PIN CONFIGURATION



Outline 20P2N-A

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

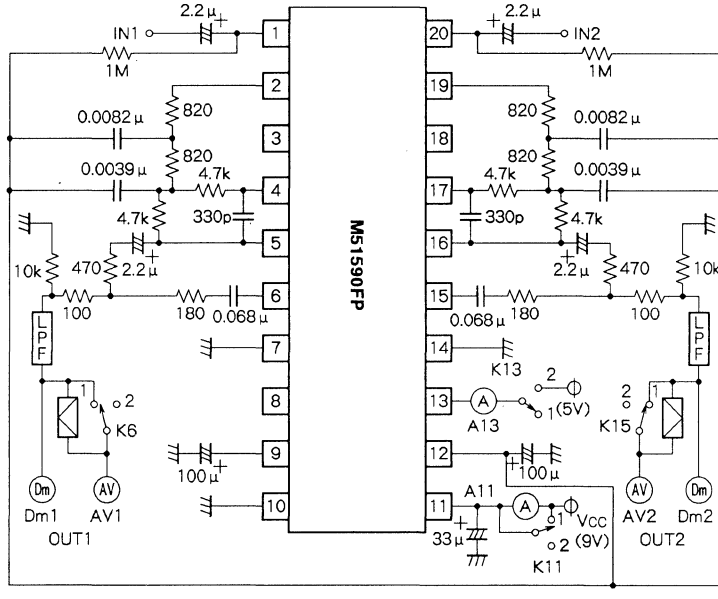
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameters	Ratings	Unit
V_{CC}	Supply voltage	14	V
P_d	Power dissipation	500	mW
K_θ	Thermal derating	5	mW/℃
T_{opr}	Operating temperature	− 20 ~ + 75	℃
T_{stg}	Storage temperature	− 40 ~ + 125	℃

ELECTRICAL CHARACTERISTICS (V_{CC} = 9V, Ta = 25℃, R_L = 10k Ω)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	Quiescent	−	5.1	13	mA
THD	Total harmonic distortion	f = 1kHz, V_{in} = 745mVrms	−	0.001	0.009	%
S/N	Signal/Noise Ratio	S : f = 1kHz, JIS-A V_{in} = 745mVrms	85	100	−	dB
CS	Channel separation	f = 1kHz, V_{in} = 745mVrms	80	95	−	dB
I_{BDE}	De-emphasis control bias current	V_{in} = 5V, pin ⑬	−	7.0	13	mA

TEST CIRCUIT

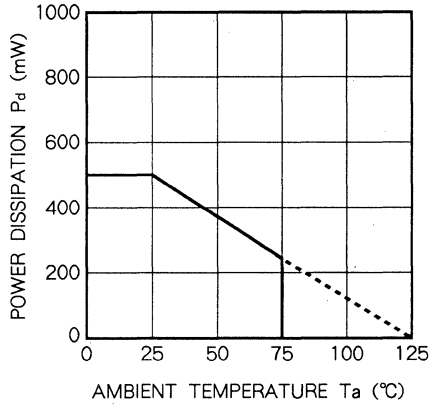


(AV) AC volt meter
(Dm) Distortion meter
(A) DC current meter
: JIS-A Filter
LPF : LPF (fc = 20kHz)

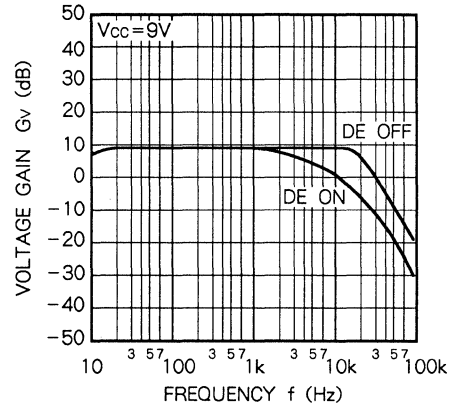
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

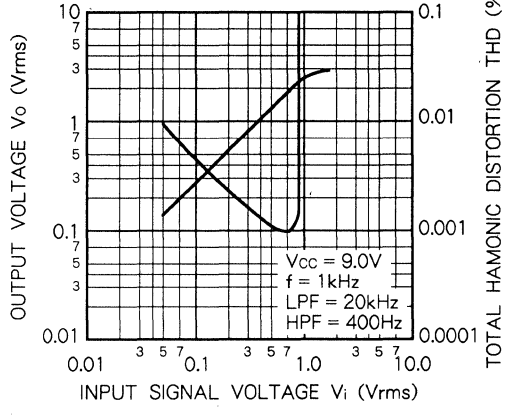
THERMAL DERATING
(MAXIMUM RATING)



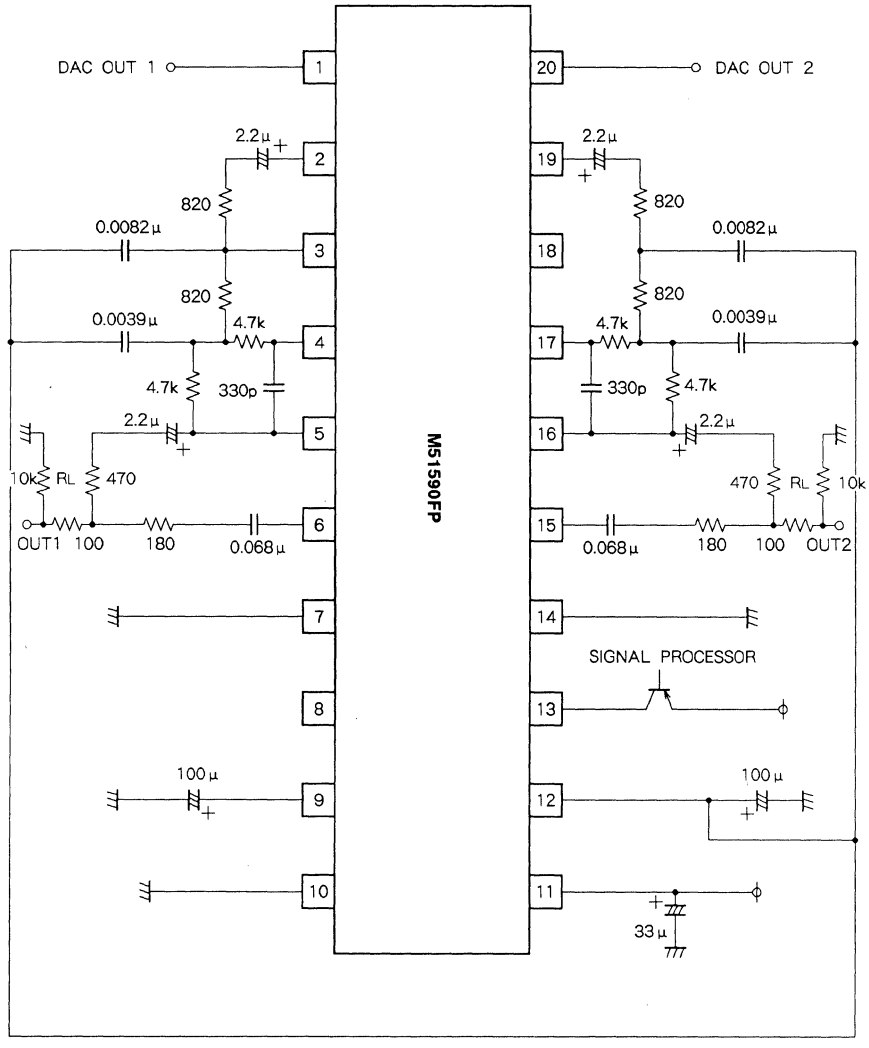
VOLTAGE GAIN VS. FREQUENCY



OUTPUT VOLTAGE, TOTAL
HARMONIC DISTORTION
VS. INPUT SIGNAL VOLTAGE



APPLICATION EXAMPLE



RL = 10k Ω

Units Resistance : Ω
Capacitance : F

M51591FP

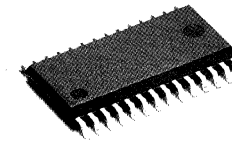
ANALOG OUTPUT AMPLIFIER FOR CD PLAYER

DESCRIPTION

The M51591FP is a semiconductor integrated circuit developed as an analog output amp for digital audio applications such as CD players. The IC also has a double-speed reproduction function.

FEATURES

- Dual speed playback
- Low circuit current ..... 5.1mA (V_{CC} = 9V)
- Low distortion ..... 0.005 % (f = 1kHz)
- Mode change driver output ..... 4mA (typ)



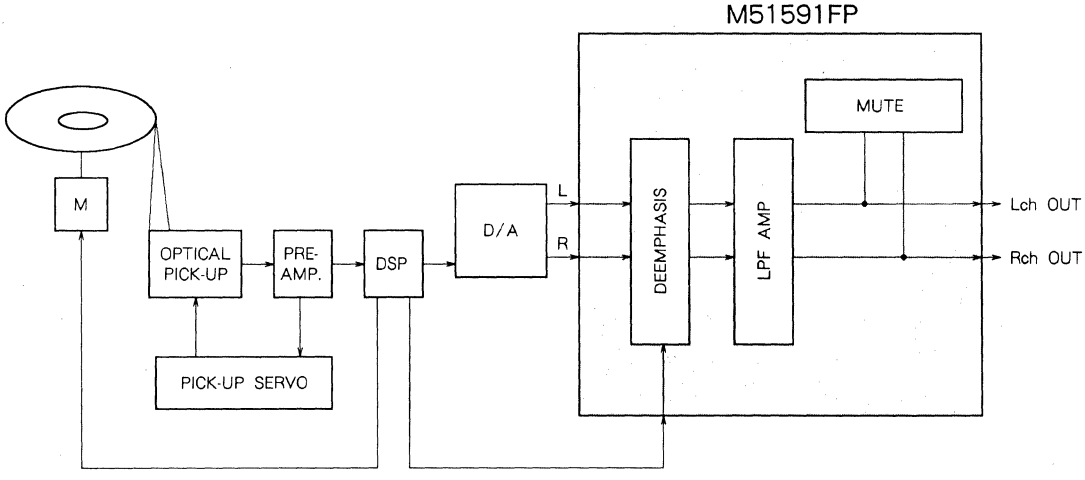
Outline 28P2W-A

1.27mm pitch 450mil SOP
(8.4mm × 17.5mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 3~11V
Rated supply voltage ..... V_{CC} = 9V
Rated power dissipation 46mW

SYSTEM CONFIGURATION

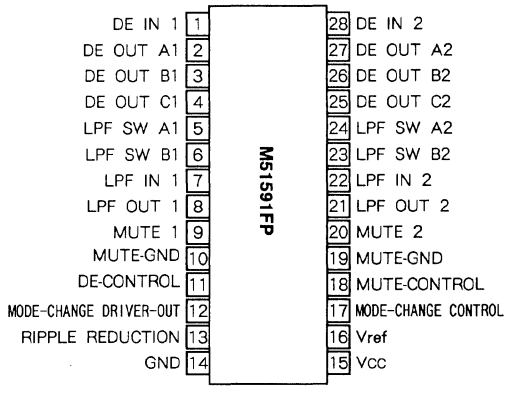


MITSUBISHI ELECTRIC

M51591FP

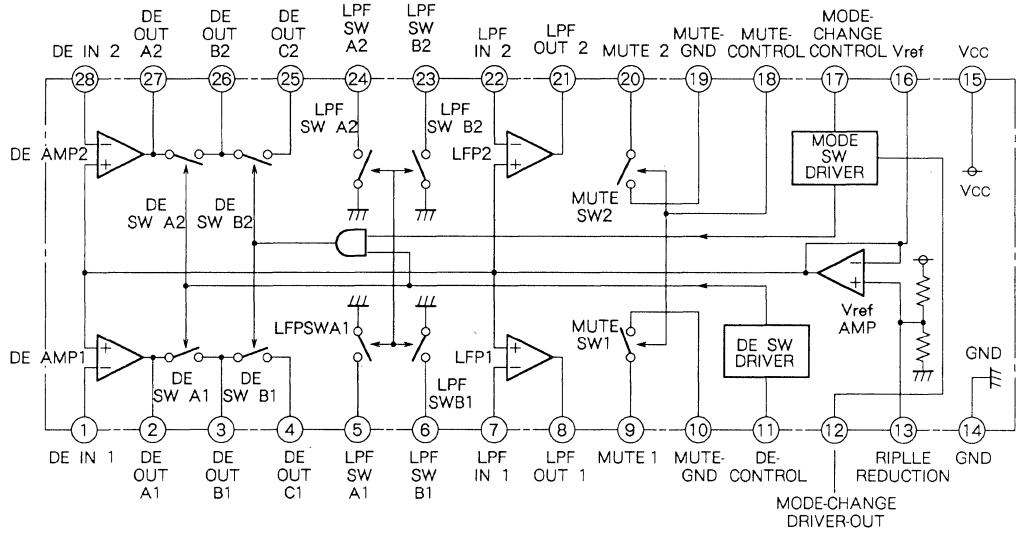
ANALOG OUTPUT AMPLIFIER FOR CD PLAYER

PIN CONFIGURATION



Outline 28P2W-A

IC INTERNAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

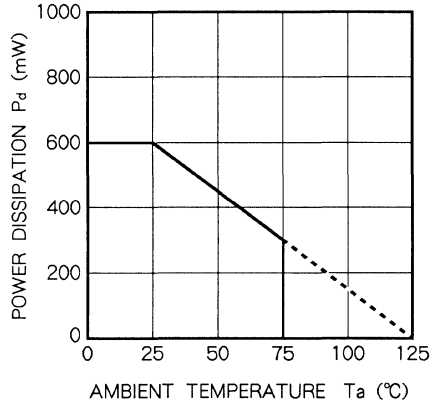
Symbol	Parameters	Ratings	Unit
V_{CC}	Supply voltage	12	V
P_d	Power dissipation	600	mW
K_θ	Thermal derating	6	mW/℃
T_{opr}	Operating temperature	− 20～+ 75	℃
T_{stg}	Storage temperature	− 40～+ 125	℃

ELECTRICAL CHARACTERISTICS (V_{CC} = 9.0V, Ta = 25℃, R_L = 10k Ω)

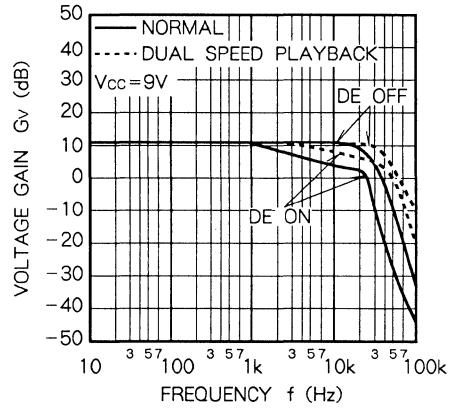
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	Quiescent	−	5.1	13	mA
THD	Total harmoic distortion	f = 1kHz, V_{in} = 450mVrms	−	0.0032	0.01	%
S/N	Signal/Noise ratio	S : f = 1kHz JIS-A V_{in} = 450mVrms	80	90	−	dB
CS	Channel separation	f = 1kHz V_{in} = 450mVrms	70	85	−	dB
A_{TTL}	Mute attenuation	f = 1kHz V_{in} = 450mVrms pin ⑱←5V	40	50	−	dB
I_{BM}	Mute control bias current	pin ⑱←5V	−	7.5	13.0	mA
V_{THDE}	De-emphasis control threshold level	pin ⑪	0.9	1.4	1.9	V
V_{THMO}	Mode change control threshold level	pin ⑰	0.9	1.4	1.9	V
I_{OMD}	Mode change driver out	pin ⑫	2.5	4.0	9.0	mA

TYPICAL CHARACTERISTICS

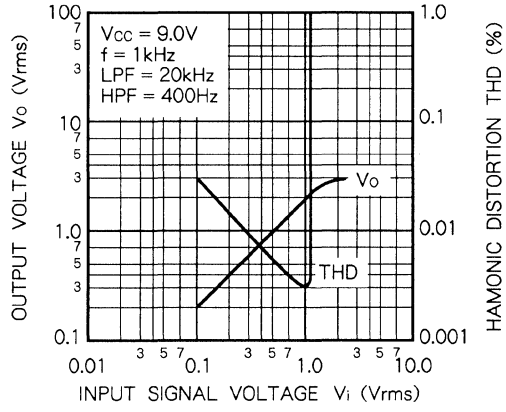
THERMAL DERATING
(MAXIMUM RATING)



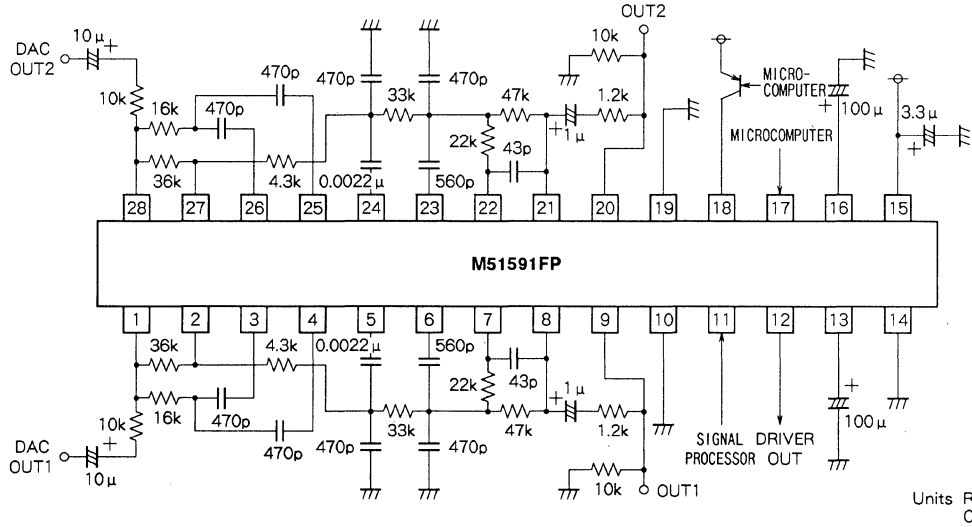
VOLTAGE GAIN VS. FREQUENCY



OUTPUT VOLTAGE TOTAL
HARMONIC DISTORTION



APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

M62471FP

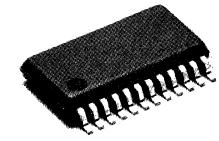
CD PLAYER HEADPHONE AMPLIFIER

DESCRIPTION

The M62471FP is a semiconductor integrated circuit developed to be the headphone amplifier used for digital audio equipment including portable CD, MD, and DCC players. The processor incoporates in itself bass boost, AGC and mute functions, all needed for headphone output.

FEATURES

- High ripple rejection (70dB typ)
- No need for external output capacitors
- Reduced shock noise at start-up
- Bass boost circuit incorporated
- Standby circuit incorporated



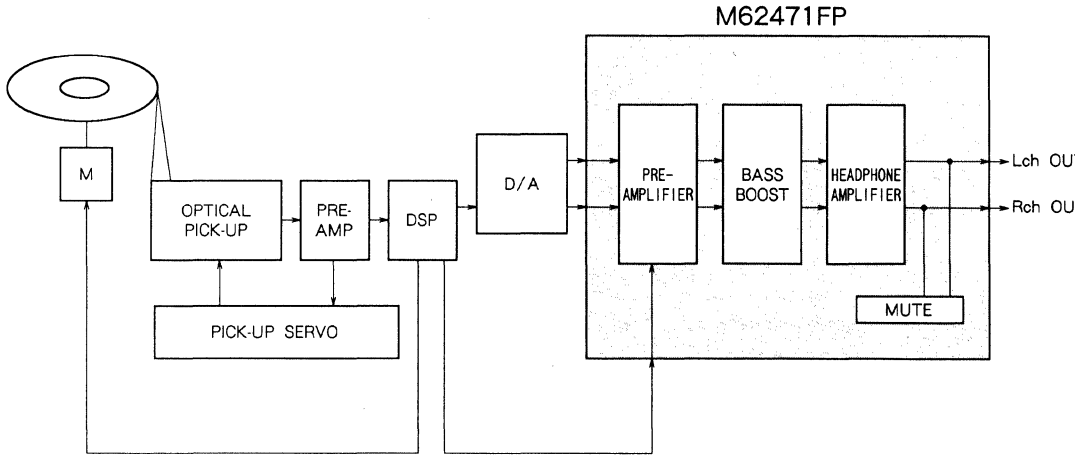
Outline 24P2Q-A

0.8mm pitch 300mil SSOP
(5.3mm × 10.1mm × 1.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... Vcc = 1.8~3.6V
Rated supply voltage ..... Vcc = 3V
Rated output power 30mW

SYSTEM CONFIGURATION

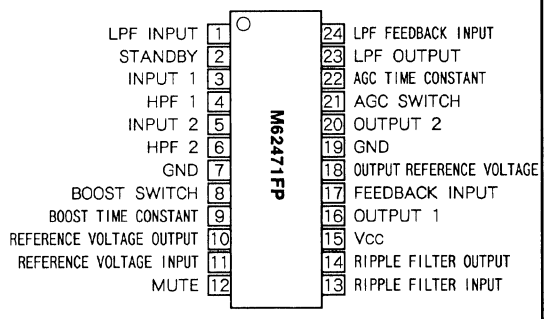


MITSUBISHI ELECTRIC

M62471FP

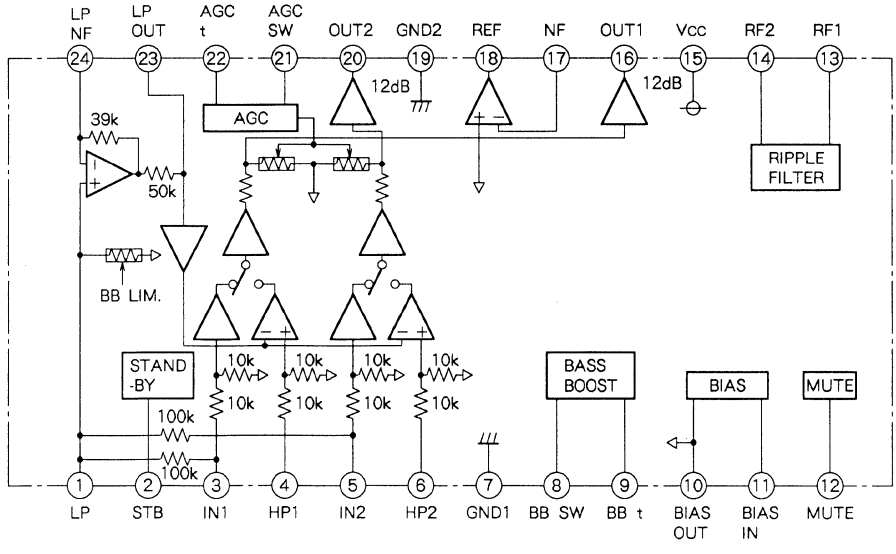
CD PLAYER HEADPHONE AMPLIFIER

PIN CONFIGURATION



Outline 24P2Q-A

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Name	Function
①	LP	LPF input	Connecting a capacitor across paired terminal ⑩ provides bass boost LPF
②	STB	Standby	Application of 1.6V or higher to this terminal operates the internal circuit, and grounding the terminal turns the circuit off
③	IN 1	Input 1	Terminal for input on the L-channel side
④	HP 1	HPF 1	Terminal for input on the L-channel side when bass boost is on
⑤	IN 2	Input 2	Terminal for input on the R-channel side
⑥	HP 2	HPF 2	Terminal for input on the R-channel side when bass boost is on
⑦	GND 1	Ground	
⑧	BB SW	Boost switch	OPEN turns bass boost on, and short across terminal ⑩ turns it off
⑨	BB t	Boost time constant	Time constant terminal for the bass boost output limiter
⑩	BIAS OUT	Reference voltage output	Terminal for outputting reference voltage
⑪	BIAS IN	Reference voltage input	Terminal for inputting reference voltage
⑫	MUTE	Mute	Application of 0.8V to this terminal turns mute on
⑬	RF 1	Ripple filter input	Terminal for input to the ripple filter
⑭	RF 2	Ripple filter output	Terminal for output from the ripple filter
⑮	Vcc	Line voltage	
⑯	OUT 1	Output 1	Terminal for output on the L-channel side
⑰	NF	Feedback input	Terminal for feedback input of the outpout reference voltage amplifier
⑱	REF	Output reference voltage	Terminal for output of the outpout reference voltage amplifier
⑲	GND 2	Ground	
⑳	OUT 2	Output 2	Terminal for output on the R-channel side
㉑	AGC SW	AGC switch	Terminal for AGC input
㉒	AGC t	AGC time constant	Terminal for AGC time constant
㉓	LP OUT	LPF output	Terminal for LPF output
㉔	LP NF	LPF feedback input	Terminal for LPF feedback input. Changes in external resistance changes bass boost gain

FUNCTION LIST

Function	Terminal	Mode	Operation	Remarks
Standby	2 STB	H (Vcc)	Internal circuit ON (Icc = 10mA)	
		L (GND)	Internal circuit OFF (Icc = 0mA)	
Bass boost	8 BB SW	Open	Bass boost ON (bass intensified)	
		Terminal ⑩ short	Bass boost OFF (normal)	
Mute	12 MUTE	H (Vcc)	Mute ON (output OFF)	
		L (GND)	Mute OFF (output ON)	
AGC	21 AGC SW	Output	AGC ON	Short with output using C+R
		Terminal ⑩ short	AGC OFF (normal)	

※ Refer to the example applied circuit

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6	V
P_d	Power dissipation	500	mW
K_θ	Thermal derating ($T_a \geqq 25$℃)	5.0	mW/℃
T_{opr}	Operating temperature	− 20 ~ + 75	℃
T_{stg}	Storage temperature	− 40 ~ + 125	℃

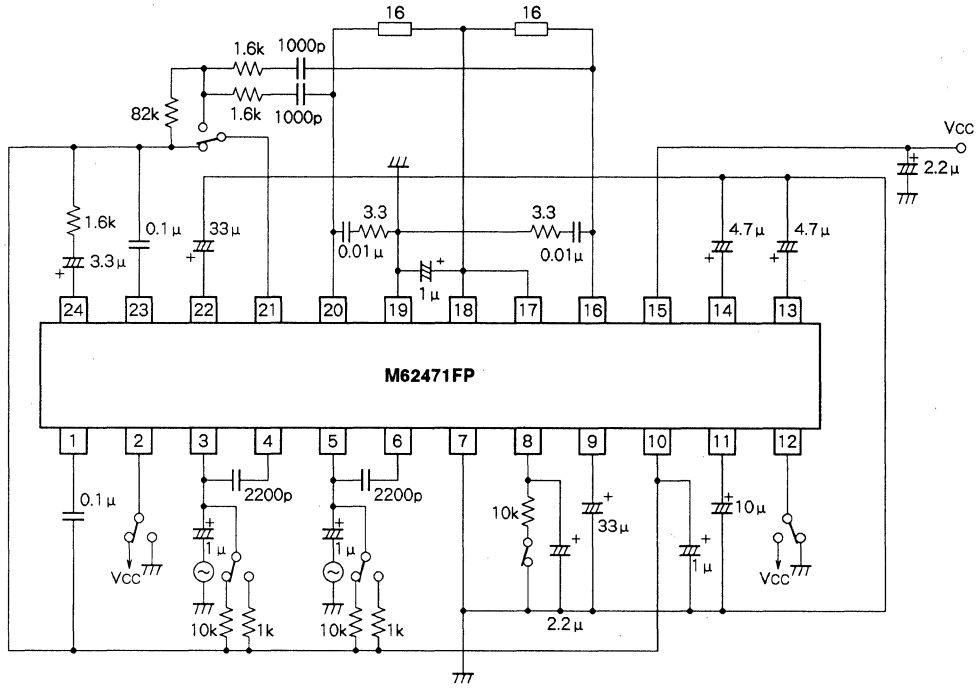
ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0V, R_L = 16 Ω, f = 1kHz, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Icc1	Circuit current	Vin = 0	6	10	15	mA
Icc2	Standby current	Ground terminal ②	−	−	1	μA
Gv	Voltage gain		10	12	14	dB
CB	Channel balance		−1.0	0	1.0	dB
Po	Rated output	THD = 10%	10	25	−	mW
THD	Total harmonics distortion	Vo = 0.3Vrms	−	0.1	0.5	%
VNO1	Output noise voltage 1	Rg = 1k Ω BW = 20~20kHz	−	20	40	μV
VNO2	Output noise voltage 2	Rg = 1k Ω BW = 20~20kHz BB = ON	−	30	60	μV
Rin	Input resistance		9	12	16	kΩ
SVRR1	Ripple rejection 1	Rg=1k Ω 100Hz, -20dBm BW=20~20kHz	64	70	−	dB
SVRR2	Ripple rejection 2	Rg=1k Ω 100Hz, -20dBm BW=20~20kHz BB=ON	59	65	−	dB
BB1	Boost level 1	f = 100Hz Vin = − 22dBm BB = ON	−4.5	−1.5	1.5	dB
BB2	Boost level 2	f = 100Hz Vin = − 32dBm BB = ON	4	7	9	dB
BB3	Boost level 3	f = 100Hz Vin = − 42dBm BB = ON	11	15	18	dB
CS	Channel separation		45	55	−	dB
△V	Output offset voltage	Rg = 10k Ω	−10	−	10	mV
AGC1	Gain control level 1	f = 2kHz Vin = − 62dBm AGC = ON	−10	0	10	dB
AGC2	Gain control level 2	f = 2kHz Vin = − 42dBm AGC = ON	−21	−12	−3	dB
AGC3	Gain control level 3	f = 2kHz Vin = − 22dBm AGC = ON	−34	− 26	−18	dB
ML	Mute level	Vin = − 22dBm (Vo = − 10dBm)	60	−	−	dB
VSTON	Circuit ON voltage	Pin ② voltage	1.6	−	−	V
VSTOFF	Circuit OFF voltage	Pin ② voltage	−	−	0.7	V
VBBON	BB ON voltage	Pin ⑧ voltage − Pin ⑩ voltage	750	−	−	mV
VBBOFF	BB OFF voltage	Pin ⑧ voltage − Pin ⑩ voltage	−	−	350	mV
VMTON	MUTE ON voltage	Pin ⑫ voltage	0.8	−	−	V
VMTOFF	MUTE OFF voltage	Pin ⑫ voltage	−	−	0.2	V

REFERENCE CHARACTERISTICS (V_{CC} = 3.0V, R_L = 16 Ω, Ta = 25℃, unless otherwise noted)

Symbol	Item	conditions		Reference value	Unit
ton	Start-up time			0.3	sec
taon	AGC ON time	f = 2kHz Vin = − 30dBm	Time from when AGC switch is turned ON until Vo = − 39dBm	120	msec
taoff	AGC OFF time		Time from when AGC switch is turned OFF until Vo = − 18dBm	4.0	sec

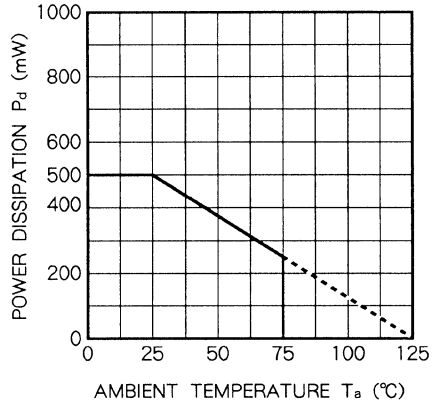
TEST CIRCUIT



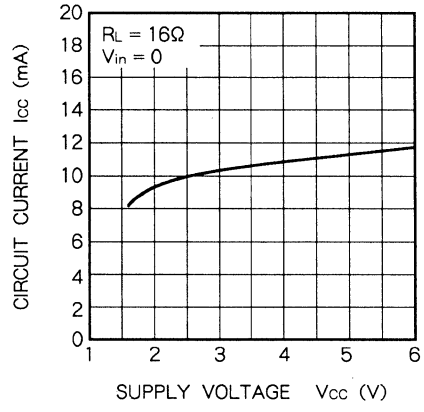
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

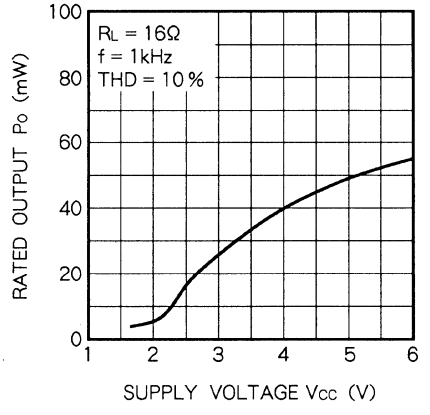
THERMAL DERATING



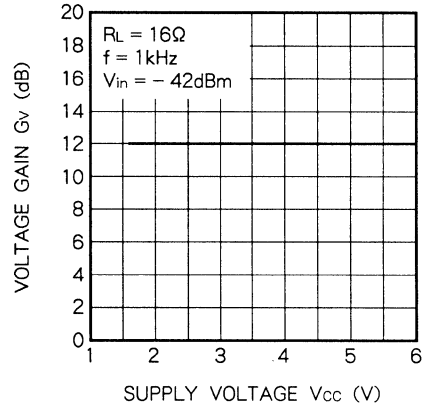
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



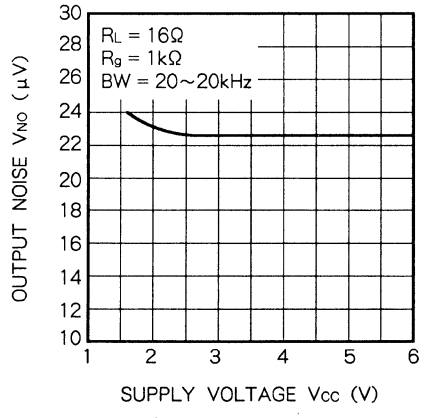
RATED VOLTAGE VS. SUPPLY VOLTAGE



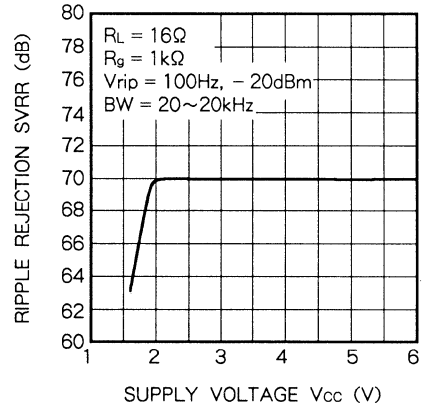
VOLTAGE GAIN VS. SUPPLY VOLTAGE



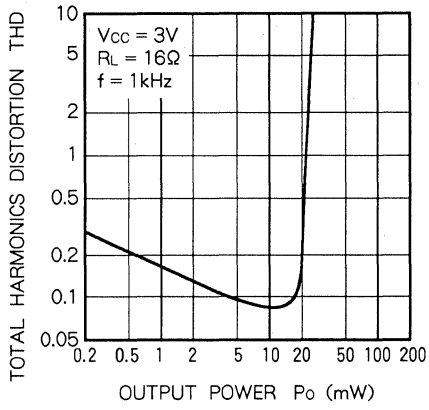
OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



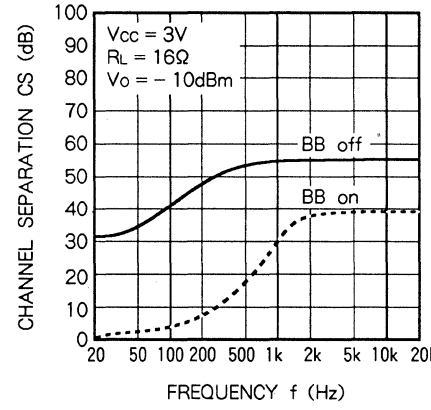
RIPPLE REJECTION VS. SUPPLY VOLTAGE



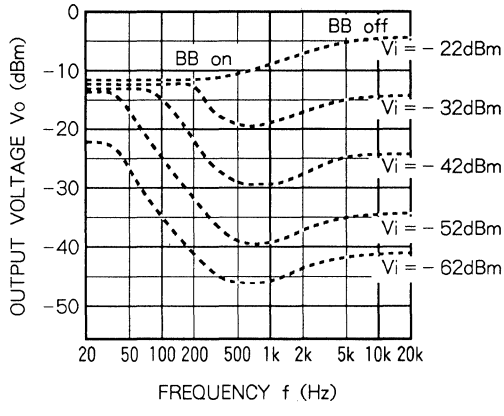
TOTAL HARMONIC DISTORTION VS. OUTPUT POWER



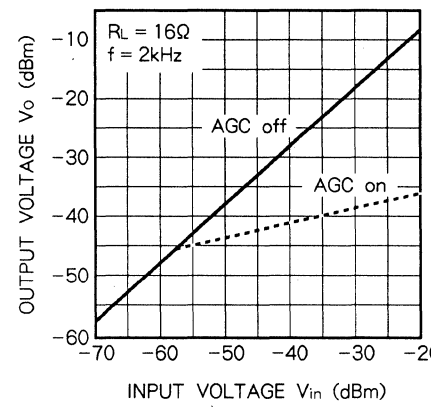
CHANNEL SEPARATION VS. FREQUENCY



OUTPUT VOLTAGE VS. FREQUENCY



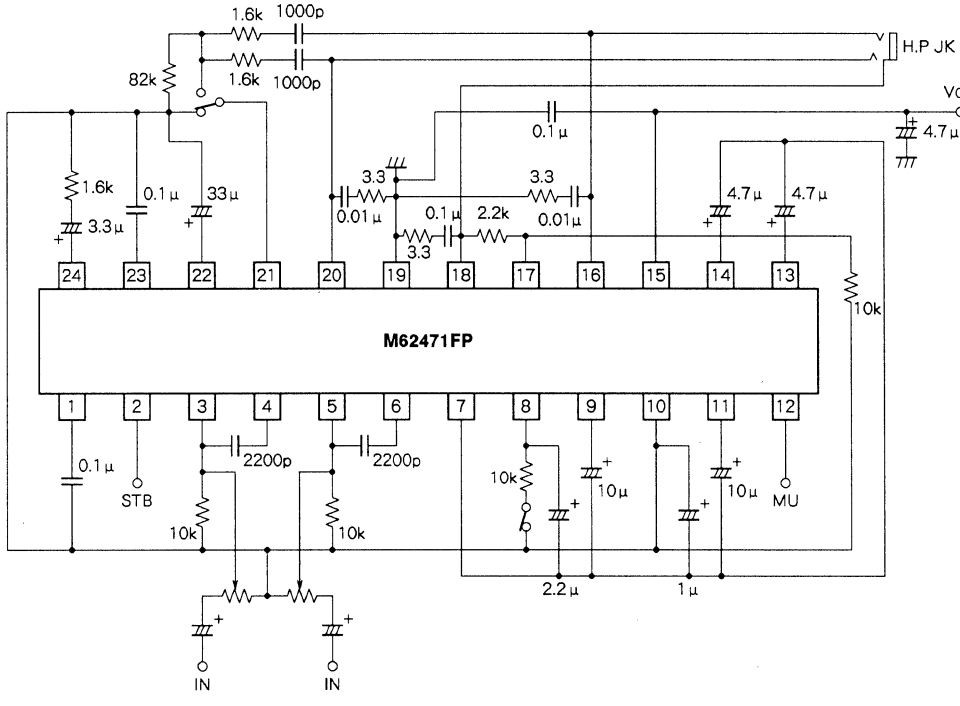
OUTPUT VOLTAGE VS. INPUT VOLTAGE



M62471FP

CD PLAYER HEADPHONE AMPLIFIER

APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

M62472FP

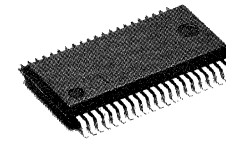
OPTICAL PICKUP SERVO CONTROL

DESCRIPTION

The M62472FP is a semiconductor integrated circuit incorporating the logic control, servo amplifier and switches required for servo control of CD player pickup.

FEATURES

- A pickup servo system can be constructed by pairing the optical pickup pre-amplifier (e. g., M51599FP)
- Incorporates the serial-parallel data conversion circuit, which alleviates load on the microcomputer
- Is highly applicable to a wide variety of pickup because of variable gain and frequency characteristics accomplished only by changing external parts



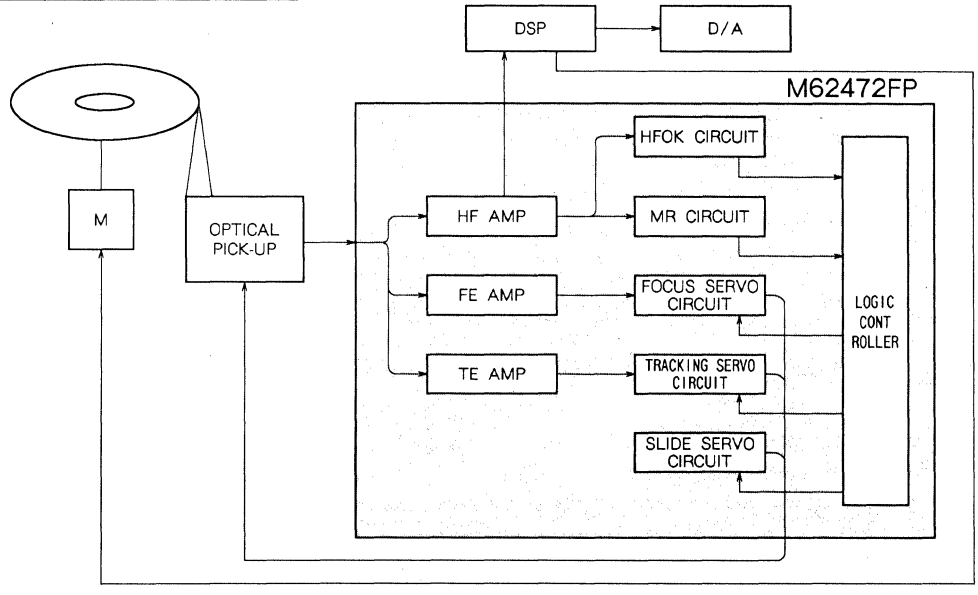
Outline 42P2R-A

0.8mm pitch 450mil SSOP
(8.4mm × 17.5mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 4~6V
Rated supply voltage ..... V_{CC} = 4V
Rated power dissipation 70mW

SYSTEM CONFIGURATION



MITSUBISHI ELECTRIC

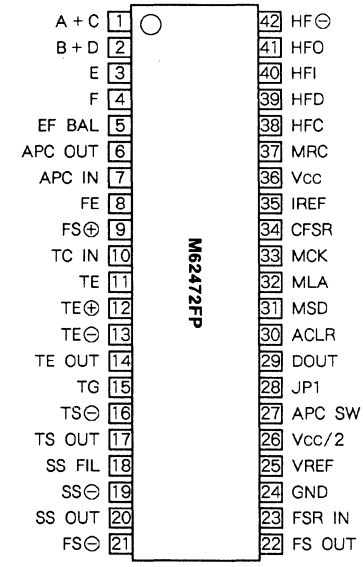
M62472FP

OPTICAL PICKUP SERVO CONTROL

BUILT-IN FUNCTIONS

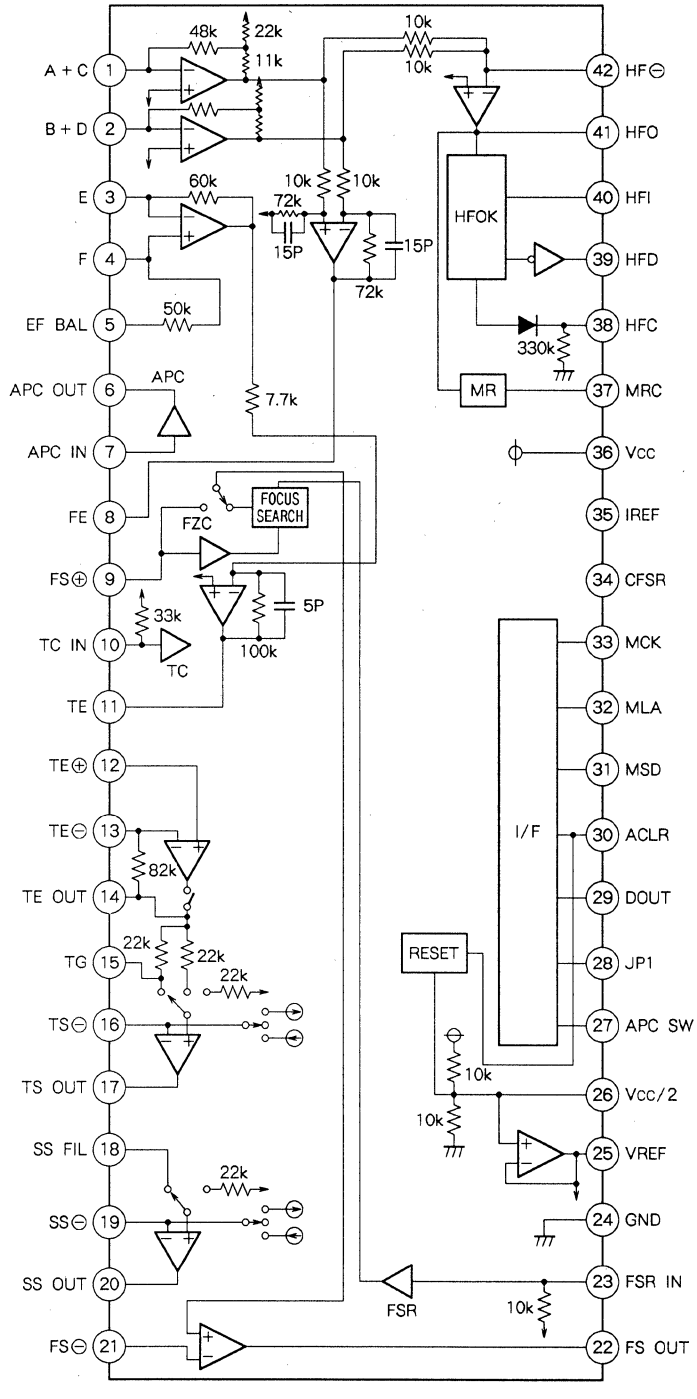
- IV amplifier
- High frequency amplifier : HF
- Focus error amplifier : FE (Focus Error Amp.)
- Focus servo amplifier : FS (Focus Servo Amp.)
- Tracking error amplifier : TE (Tracking Error Amp.)
- Tracking servo amplifier : TS (Tracking Servo Amp.)
- Slide servo amplifier : SS (Slide Servo Amp.)
- HF signal detector
- MR signal detector
- Jump and brake switch circuits :
  - TS1 and TS2 SW's (Tracking Servo Switches)
  - TG1 SW's (Tracking Gain Switches)
  - JF and JR SW's (Jump Forward and Jump Reverse Switches)
  - SS SW (Slide Servo Swith)
  - SF and SR SW's (Slide Forward and Slide Reverse Switches)
- Focus search circuit :
  - Focus search switch (FSR1, FSR2, FSR3, FS)
  - Focus search detector (FSR Det)
  - Focus zero cross detector (FZC Det)
- Track cross detector : TC Det (Track Cross Detector)
- Shock detector : Shock Det (Shock Detector)
- Logic controller :
  - Serial→parallel data conversion circuit
  - Jump, brake and focus search controls
- Vcc/2 generation circuit
- Auto laser power control switch

PIN CONFIGURATION



Outline 42P2R-A

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Block	I/O	Function
①	A + C	IV-Amp	I	IV amplifier input A + C
②	B + D	↑	I	IV amplifier input B + D
③	E	↑	I	IV amplifier input E
④	F	↑	I	IV amplifier input F
⑤	EF BAL	↑	I	EF-IV amplifier balance adjustment
⑥	APC OUT	Laser power switch	O	Laser power control switch output
⑦	APC IN	↑	I	Laser power control switch input
⑧	FE OUT	Focus servo	O	FE amplifier output
⑨	FS⊕	↑	I	FS amplifier non-inversion input
⑩	TC IN	Track servo	I	Track cross signal input
⑪	TE	↑	O	TE amplifier 1 output
⑫	TE⊕	↑	I	TE amplifier 2 non-inversion input
⑬	TE⊖	↑	I	TE amplifier 2 inversion input
⑭	TE OUT	↑	O	TE amplifier 2 output
⑮	TG	↑	I	Track gain selector switch output
⑯	TS⊖	↑	I	TS amplifier inversion input
⑰	TS OUT	↑	O	TS amplifier output
⑱	SS FIL	Slide servo	I	SS amplifier non-inversion input
⑲	SS⊖	↑	I	SS amplifier inversion input
⑳	SS OUT	↑	O	SS amplifier output
㉑	FS⊖	Focus servo	I	FS amplifier inversion input
㉒	FS OUT	↑	O	FS amplifier output
㉓	FSR IN	↑	I	Focus search voltage level detector input
㉔	GND	Power source	I	Ground
㉕	VREF	↑	O	Reference voltage
㉖	Vcc/2	↑	I	Vcc/2
㉗	APC SW	Laser power switch	I	Laser power control switch control terminal
㉘	JPI	Microcomputer I/O	I	Track jump brake pulse control signal. Normally "H"
㉙	DOUT	↑	O	Internal condition output corresponding to microcomputer commands
㉚	ACLR	↑	I	All clear. Clears all internal registers and flipflops. Reset by "L"
㉛	MSD	↑	I	Microcomputer serial data. Serial data transfer from microcomputer to servo. LSB first. 8-bit data
㉜	MLA	↑	I	Serial data latch from microcomputer to servo. Data transfer initiated at the rising edge
㉝	MCK	↑	I	Clock for serial data transfer from microcomputer to servo. Data uptaken at the rising edge
㉞	CFSR	Power source	–	Connects capacitors to determine the time constant of focus search waveform
㉟	IREF	Constant-current power source	I	Terminal to connect current setting resistors for the reference power source
㊱	Vcc	Power source	I	Power terminal
㊲	MRC	Mirror detector	–	Mirror detector time constant terminal
㊳	HFC	HF detector	O	HF signal detector output. Outputs "H" when HF is detected
㊴	HFD	↑	O	HFC inversion output
㊵	HFI	↑	I	HF detector input
㊶	HFO	HF Amp	O	HF amplifier output
㊷	HF⊖	↑	I	HF amplifier non-inversion input

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	+ 6.5	V
$\lvert V_I \rvert$	Input voltage (absolute value)	Applied supply voltage+0.3	V
$\lvert V_O \rvert$	Output voltage (absolute value)	Applied supply voltage+0.3	V
P_d	Power dissipation	750	mA
T_{opr}	Operating temperature	− 20 ~ + 70	℃
T_{stg}	Storage temperature	− 40 ~ + 125	℃

FUNCTION DESCRIPTION

Setting the built-in constant-current source current level

The current level of the constant-current source of focus search (FSR), tracking servo (TS), and slide motor servo (SS), FSR, TS and SS can be set via resistor Rx connected across terminal ㉟~Vcc.

Let the absolute values of the constant-current source current levels for FSR, TS, SS be IFSR, ITS, Iss, respectively. Then

$$I_{FSR} \simeq \frac{1}{8} \cdot \frac{V_{CC} - V_{㉟}}{R_X}$$

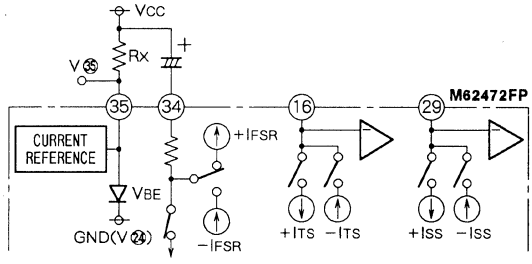
$$I_{TS} \simeq \frac{1}{8} \cdot \frac{V_{CC} - V_{㉟}}{R_X}$$

$$I_{SS} \simeq \frac{1}{4} \cdot \frac{V_{CC} - V_{㉟}}{R_X}$$

where V㉟ is voltage at terminal ㉟. Let voltage at terminal ㉔ (GND) be V㉔. Then V㉟ can be obtained from :

$V_{㉟} = V_{㉔} + V_{BE}$ ($V_{BE} \simeq 0.7V$ as standard)

Constant-current source block diagram



FSR detector

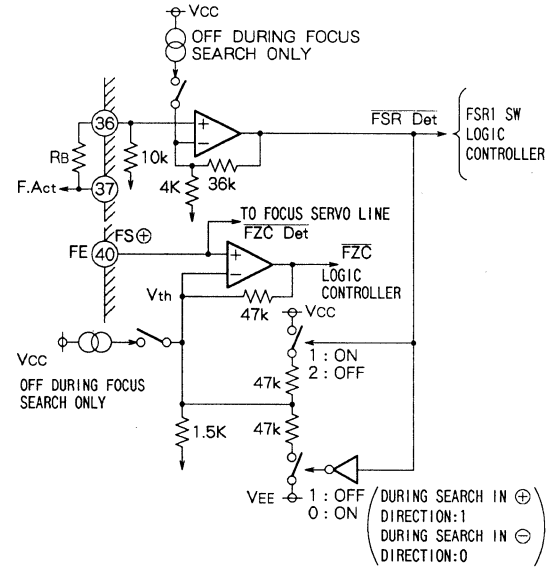
Current is input from FS OUT (terminal ㉒ output) via resistors or the driver and resistors into FSR IN (terminal ㉓ input). The following are performed during focus search :

- Automatic switching of focus search direction
- Automatic switching of FZC detection polarity

Focus search always begins from the ⊕ side. The polarity of focus search voltage (⊕ or ⊖) is switched by FSR DET signal via FSR1 SW.

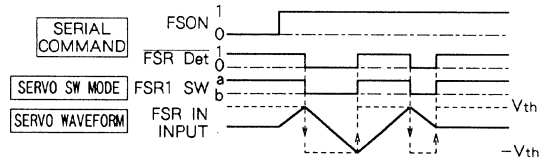
Note 2 : M62472FP provides focus intake on the focus search ⊖ side only.

Equivalent circuit

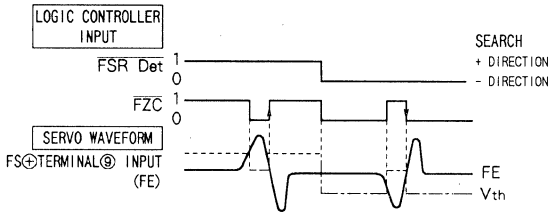


Unit Resistance : Ω

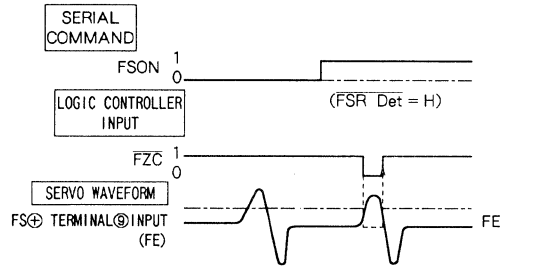
FSR det operation timing chart



FZC operation timing chart



FZC reset



INPUT	OUTPUT		
FSR IN level V_{IN}	FSR Det	FSR1 SW mode	FZC V_{th} level
$V_{IN} > V_{th}$	0	Side b : ⊖search voltage developed	Rise Fall 0 $V_{CC}/2-0.15V$
$V_{IN} < V_{th}$	1	Side a : ⊕search voltage developed	Rise Fall $V_{CC}/2-0.15V$ 0V

Setting the focus search voltage and jump pulse and slide feed voltages (power source : ± 5V, R_X = 47k Ω)

Setting the focus search voltage

Setting the FSR waveform maximum level V_{FS} (determination of R_B)

$$V_{FS} = \frac{R_A + R_B}{R_A} V_{FSR} \cdots\cdots\cdots\cdots (1)$$

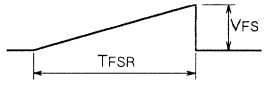
$$\therefore R_B = R_A \left(\frac{V_{FS}}{V_{FSR}} - 1\right)$$

$$= 10 \times 10^3 \left(\frac{V_{FS}}{0.5} - 1\right) \quad (\Omega)$$

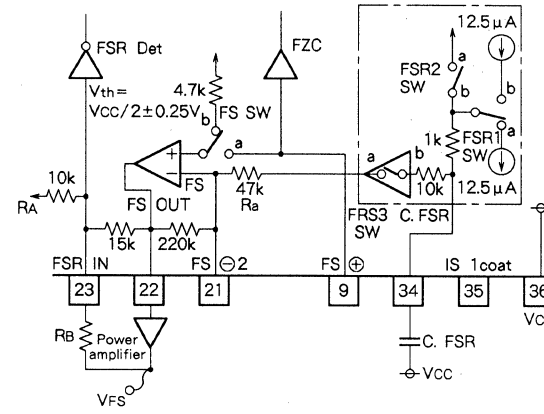
V_{FSR} : FSR Det threshold value ± 0.5V
R_A : FSR IN ㉓ input resistance 10k Ω
R_B : FSR IN ㉓ external resistance

Setting FSR time t_{FSR} (determination of C_{FSR} and R_f)

$$t_{FSR} = \frac{C_{FSR}}{I_{FSR}} - \frac{R_S}{R_F} V_{FS} \cdots\cdots\cdots (2)$$



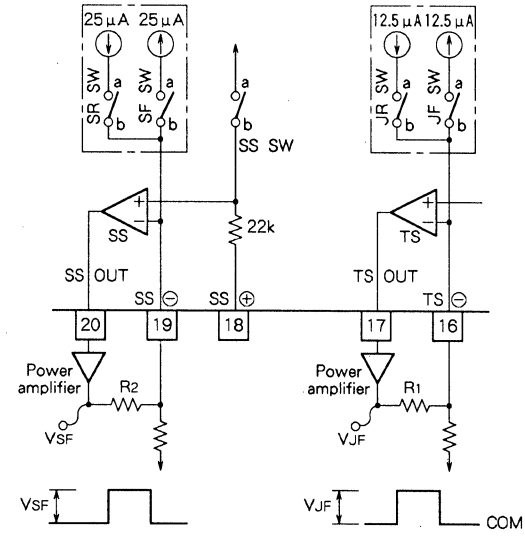
R_S : FS⊖ terminal ㉑ internal resistance 47k Ω
R_f : FS Amp external feedback resistance
C_{FSR} : C. FSR terminal ㉞ external capacitor
I_{FSR} : focus search current ± 25 μ A



Note 3. Resistances in the diagram indicate standard values. Current and voltage values are those when V_{CC} = 5V and R_X = 47k Ω

Setting jump pulse and slide feed voltages

- Jump pulse voltage V_{JF}
  $V_{JF} = R_1 \times 12.5\,\mu A$
- Slide feed voltage V_{SF}
  $V_{FS} = R_2 \times 25\,\mu A$



MITSUBISHI ELECTRIC

Functions of serial command

The logic controller has in itself a 8-bit shift register, which converts (or decodes) serial data from the microcomputer (input into MSD terminal ㉛) into commands for the servo IC. These commands are compatible with those of M52131FP.

Data-IN

The upper four bits (D_7 to D_4) of 8-bit data can set the command mode, and the lower four (D_3 to D_0) the command state.

Commands in the same mode can be used at the same time within a data transfer and remains as set until new data is input. Thus the command state does not change even if other modes are chosen.

Serial command function table (X = "1 or 0")

Mode	MSB → Input into Data IN terminal ㉛								Data OUT terminal setting
	Mode selection				Command state setting				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
FOCUS	0	0	0	0	FS ON	×	FSR EN	×	FS ON
TRACK1 A	0	0	0	1	SHOCK A	BRAKE A	×	TG	SHOCK OUT
TRACK1 B			1		SHOCK B	BRAKE B			
TRACK2	0	0	1	0	TRACK		SLIDE		TC
SERVO OFF	0	1	×	×	×	×	×	×	0
STOP	1	1	×	×	×	×	×	×	0

Note 4. The states of command TRACK (D_3, D_2) and SLIDE (D_1, D_0) in TRACK 2 mode are set in 2-bits each.
5. Output from Data-OUT terminal ㉜ is automatically switched when the mode is switched.
6. "1 × × × × × × ×" is used for the command sent to the signal processing LSI (e.g., M50422P, M50423FP and M65820FP). During use of this command, the servo IC remains held, or unchanged, retaining the hold condition.

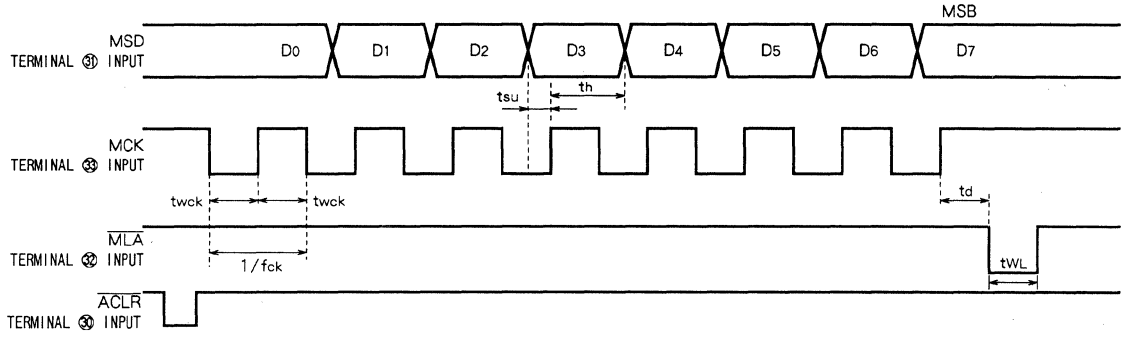
Command function table

Command	Mode	Data			Functions	
FS ON	FOCUS	D_3	1	ON	Starts focus search and turns focus on	
			0	OFF		
$\overline{\text{FSR EN}}$	↑	D_1	1	INHIBIT	Prohibits automatic focus re-intake	
			2	ENABLE	D_1 = "1" actuates prohibition	
BRAKE A	TRACK1 A	D_2	1	ON	Provides jump brake (setting) operation	
			0	OFF	OPEN/CLOSE TS2 SW	
BRAKE B	TRACK1 B	D_2	1	ON	Provides jump brake (setting) operation	
			0	OFF	OPEN/CLOSE TS1 SW	
TG	TRACK1	D_0	1	OPEN	Controls track gain selector switch, TG SW	
			0	CLOSE		
TRACK	TRACK2	D_3	D_2			
		0	0	TS OFF	Track servo OFF	For the states of TS1, TS2, JF and JR SW's, refer to the TRACK function table
		0	1	TS ON	Track servo ON	
		1	0	JF	Forward jump	
		1	1	JR	Reverse jump	
SLIDE	TRACK2	D_1	D_0			
		0	0	SS OFF	Slide servo OFF	For SS, SF and SR SW's, refer to the SLIDE function table
		0	1	SS ON	Slide servo ON	
		1	0	SF	Forward slide	
		1	1	SR	Reverse slide	
–	SERVO OFF				Resets data D_0 to D_3 to "0"	
–	STOP				Resets data D_0 to D_3 to "0" (this command is common to the signal processing LSI, M50427FP)	

Serial data (MSD) transfer method

With data transferred by "LSB first", sending $\overline{MLA}$ signal, the command is executed.

Serial data input timing chart



Logic input conditions

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
f_{ck}	Clock frequency		–	50	125	kHz
t_{wck}	Clock pulse width		4	20	–	μs
t_{su}	Set-up time		0.1	0.2	–	μs
t_h	Hold time		4	20	–	μs
t_d	Delay time		4	20	–	μs
t_{WL}	Latch pulse width		1	5	–	μs

BRAKE's A and B

With BRAKE A or B command set to "1", jump brake operation begins, improving the jump setting ability after track jump.

Jump Brake operation

- When MR = 1, $\overline{TC}$ = "↑"or "↓" (TC Det output rise or fall) turns the track servo loop OFF.
- When MR = 0, $\overline{TC}$ = "↑"or "↓" turns the track servo loop ON.

Jump brake truch table

INPUT	OUTPUT	
MR $\overline{TC}$	BRAKE A = "1", the state of TS2 SW	BRAKE B = "1", the state of TS1 SW
1 ⊓↓	a(track servo OFF)	b(track servo OFF)
0 ⊓↓	b(track servo ON)	a(track servo ON)

When JF, JR or TS OFF command is effective, Jump brakedoes not operate.

TRACK function table

INPUT			OUTPUT (SW position)			
Command	Data					
	D_3	D_2	TS1 SW	TS2 SW	JF SW	JR SW
TS OFF	0	0	a(servo ON)	a(servo OFF)	b	b
TS ON	0	1	a(servo ON)	b(servo ON)	b	b
JF	1	0	b(servo OFF)	b(servo ON)	a(JF ON)	b
JR	1	1	b(servo OFF)	b(servo ON)	b	a(JR ON)

SLIDE function table

INPUT			OUTPUT (SW position)		
Command	Data				
	D_1	D_0	SS SW	SF SW	SR SW
SS OFF	0	0	a(servo OFF)	b	b
SS ON	0	1	b(servo ON)	b	b
SF	1	0	a(servo OFF)	a(SF ON)	b
SR	1	1	a(servo OFF)	b	a(SR ON)

Direct command function

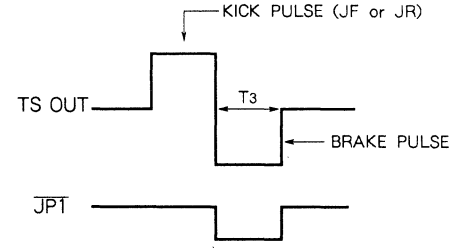
$\overline{JP1}$ signal

Durring jump of a track and the like operation, two serial data transfers can be comitted so as to decrease delay in microcomputer processing time.

$\overline{JP1}$ is normally "1". Switching to $\overline{JP1}$ = "0" when TC (Data Out) signal = "↑" causes the logic controller to automatically inverse the jump polarity (JF→JR and JR→JF).

If $\overline{JP1}$ is changed from "0" to "1" upon completion of one-track jump (after given time T_3), JF and JR are automatically ended, thus turning TS and SS on.

Signal waveform at one-track jump



$\overline{JP1}$ Signal truth table

$\overline{JP1}$ (INPUT)	TRACK 2 mode (0010 D_3 D_2 D_1 D_0) (OUTPUT)							
	TRACK (D_3 D_2)				SLIDE (D_1 D_0)			
	00	01	10	11	00	01	10	11
1	TS OFF	TS ON	JF	JR	SS OFF	SS ON	SF	SR
0	TS OFF	TS ON	JR	JF	SS OFF	SS ON	SF	SR
↑	TS OFF	TS ON	TS ON	TS ON	SS ON	SS ON	SF	SR

Note 7. If $\overline{JP1}$ = "↑" command is input when TS is OFF (001000XX), TS and SS are not turned on.

8. If TS and SS are turned on when $\overline{JP1}$ = "↑", TS and SS are kept ON until the subsequent TRACK 2 mode command arrives.

Logic output function

Data out

This is switched by changing the serial command mode (see the serial command function table). Data output corresponds to the serial command mode sent last.

Data out output correspondence table

	Data out signal name	Serial command mode (input)
(I)	FS ON	FOCUS (0000XXXX)
(II)	TC	TRACK2 (0010XXXX)
(III)	SHOCK	TRACK1 A (0001XXXX) TRACK2 B (0011XXXX)

(I) FS ON

When HFC terminal ⑧ input = "1" and when FS SW = "a" (servo ON), this outputs FS OK = "1".

FS OK truth table

INPUT		OUTPUT
HF OK	FS SW position	FS OK
0	b(servo OFF)	0
1	b(servo OFF)	0
0	a(servo ON)	0
1	a(servo ON)	1

While FS OK = "0", the following hold regardless of the command state :

TS2 SW = "a" (servo OFF)

SS SW = "a" (servo OFF)

(II) TC

Outputs TC signals latching MR signals at the edge (rise or fall) of TC Det output $\overline{TC}$. TC = "0" during reset.

(III) SHOCK OUT

Outputs SHOCK Det signals (SHOCK OUT).

TC truth table

INPUT		OUTPUT
MR	$\overline{TC}$	TC
1	↑ or ↓	1
0	↑ or ↓	0

$\overline{HFD}$

Outputs HFOK inversion signals. (Connect this to HFD terminal of the signal processing LSI M50XXX.)

Jump flag

Outputs "1" when the serial command is TS OFF, JF, JR, and BRAKE, and "0" in other conditions. (Connect this to the jump terminal of the pre amplifier M51XXX.)

ADDITIONAL FUNCTIONS

1. HF signal detecter (HFOK)

Outputs "H" when HF signals are detected (HFC terminal ㉘).

2. MR signal detecter

Detects HF signal envelope and send data to the internal logic controller.

3. APC SW

Incorporates driver transistors for switch transistors so as to turn the APC circuit on/off.

M62474FP

OPTICAL PICKUP PREAMPLIFIER

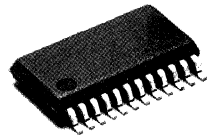
DESCRIPTION

The M62474FP is a semiconductor IC developed to be the preamplifier for CD player optical pickups.

Incorporating in an ultra-compact, 24-pin flat package three IV amplifiers to convert current signals from the pickup photodiodes into voltage, the HF mixmum amplifier, focus error amplifier, tracking error amplifier, and HF signal and mirror detection circuits, the IC can be acccomodated within an optical pickup.

FEATURES

- Adaptable to the 3-beam method
- Operable with either single or double power source
- Incorporates the FE amplifier and TE amplifier LPF (fc = 70 kHz) to discard undesired high-frequency components.
- E-F balance adjustment terminal (No.3) provided
- External parts: chemical capacitor: 2 pcs; ceramic capacitor: 4 pcs, VR: 2 pcs; and resistors: only 2 pcs
- All circuits are accomodated in the ultra-compact 24-pin flat package (read pitch: 0.8 mm)



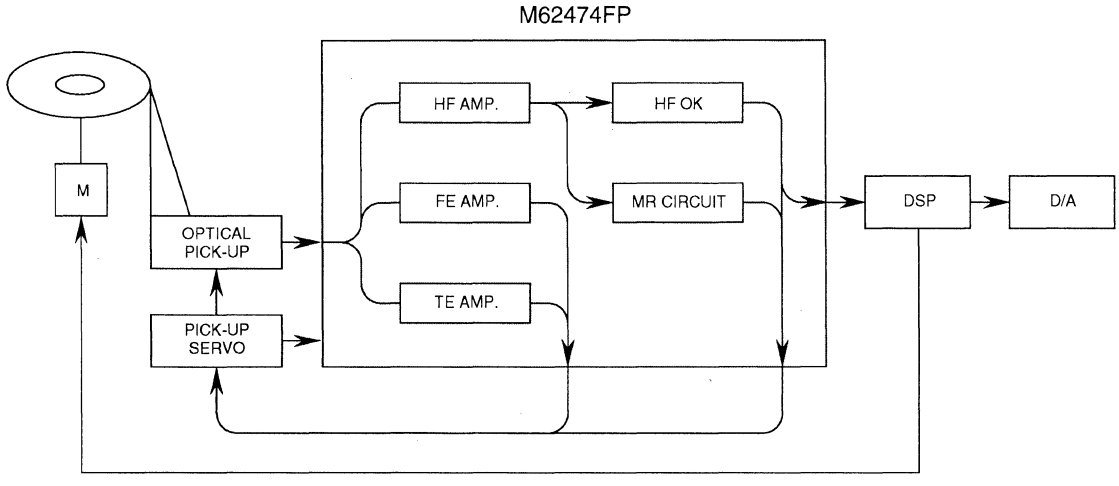
Outline 24P2Q-A

0.8mm pitch 300mil SSOP
(5.3mm×10.1mm×1.8mm)

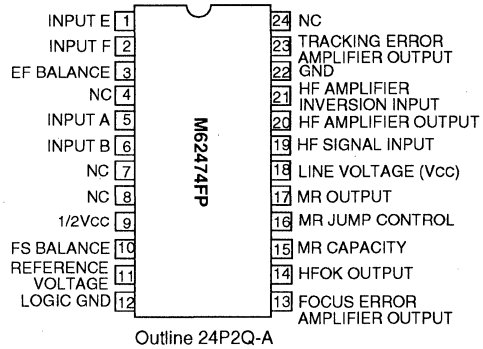
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... 4.75 ~ 5.25 V
Rated power voltage ..... 5 V

SYSTEM CONFIGURATION



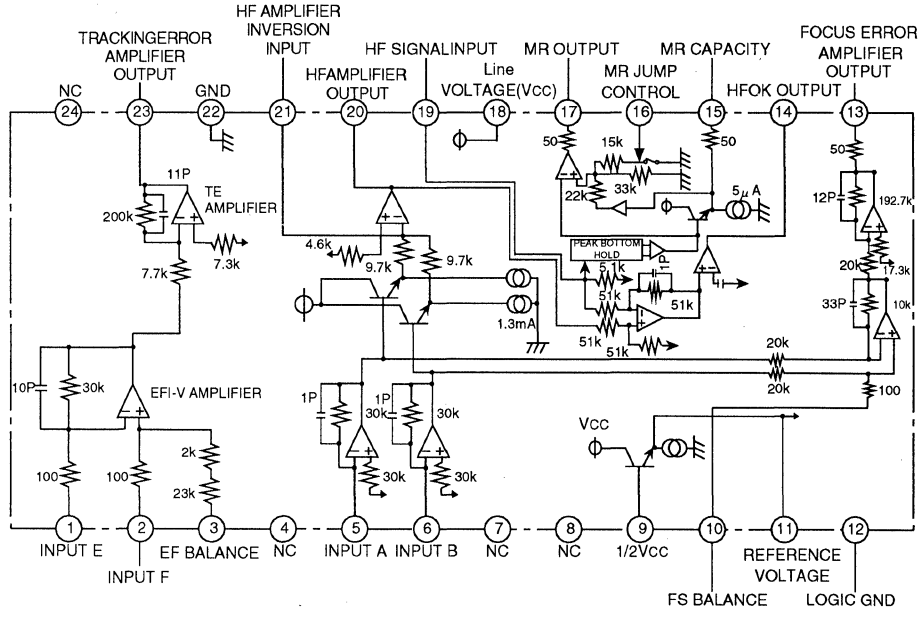
PIN CONFIGURATION



Outline 24P2Q-A

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



Units Resistance : Ω
Capacitance : F

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

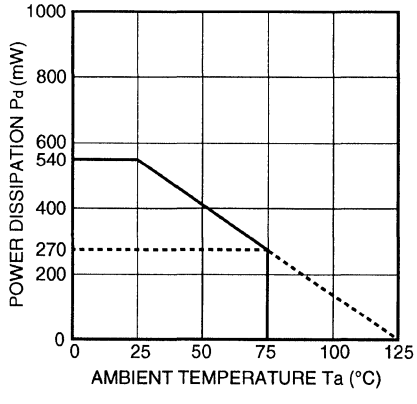
Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	13	V
I_{CC}	Circuit current	60	mA
V_I	Input voltage	Supply voltage −0.3 V	V
V_O	Output voltage	Supply voltage −0.3 V	V
P_d	Power dissipation	540	mW
K_θ	Thermal derating (Ta≧25℃)	5.4	mW/℃
T_{opr}	Operating temperature	−20∼75	°C
T_{stg}	Storage temperature	−40∼125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CCO}	Circuit current		When no signal	6.0	12.5	29.0	mA
G_{VHF}	HF	HF voltage output	V_i = 156mVp-p, f = 500kHz, Input via 30 kΩ to input terminal IV A, B	0.9	1.1	–	Vp-p
f_{HF}	HF	HF frequency characteristics	V_i = 156mVp-p, f = 2MHz, Input via 30 kΩ to input terminal IV A, B	−3	0	–	dB
V_{OHA}	HF	HF output voltage "H"		3.8	4.2	–	V
V_{OHF}	HF	Output offset voltage	Input open (output voltage vs. V_{ref})	−120	0	120	mV
G_{VFE}	FE	FE voltage output	V_i = 156mVp-p, f = 1kHz Input via 30 kΩ to input terminal IV A	0.5	0.7	0.9	Vp-p
V_{HAC}	FE	FE output voltage "H"	RL = 10kΩ	3.6	4.1	–	V
V_{LAC}	FE	FE output voltage "L"	RL = 10kΩ	–	0.5	1.2	V
V_{OFE}	FE	Output offset voltage	Input open	−50	0	50	mV
G_{VTE}	TE	TE voltage output	V_i = 38.4mVp-p, f = 1kHz, Input via 30 kΩ to input terminal IV E	0.7	1.0	1.3	Vp-p
V_{HE}	TE	TE output voltage "H"	RL = 10kΩ	3.6	4.1	–	V
V_{LE}	TE	TE output voltage "L"	RL = 10kΩ	–	0.5	1.2	V
V_{OTE}	TE	Output offset voltage	Input open	−100	0	100	mV
V_{HOK}	HFOK	HFOK output voltage "H"		3.5	4.1	–	V
V_{LOK}	HFOK	HFOK output voltage "L"	When no signal	–	0	0.4	V
V_{THK}	HFOK	Threshold voltage		0.26	0.37	0.48	V
V_{HMR}	MR	MR output voltage "H"	When no signal	3.5	4.1	–	V
V_{LMR}	MR	MR output voltage "L"		–	0	0.4	V
V_{THN}	MR	Envelope level ratio (when NORMAL)	f = 500kHz (carrier)	0.26	0.36	0.46	–
V_{THJ}	MR	Envelope level ratio (when JUMP)	f = 500kHz (carrier)	0.5	0.6	0.7	–
f_{MRf}	MR	MR frequency characteristics (when JUMP)	f = 500kHz (carrier), AM wave, modulation percentage 55%	47	60	–	kHz

TYPICAL CHARACTERISTICS

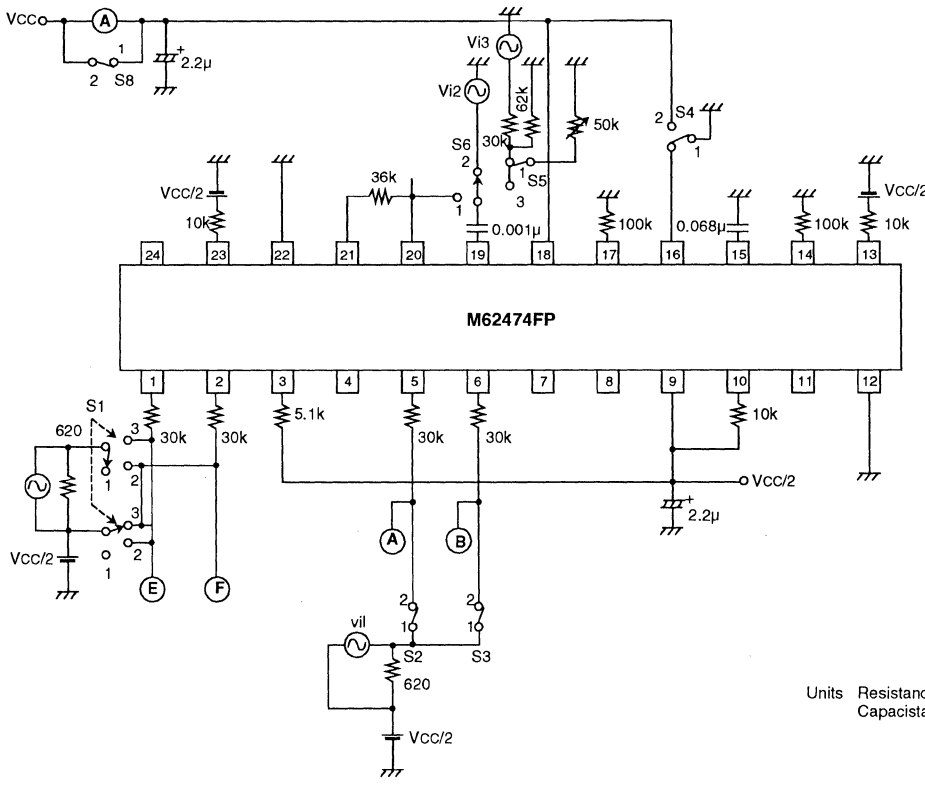
THERMAL DERATING



TEST METHODS (V_{CC} = 5 V, Ta = 25℃, unless otherwise noted)

Parameter	Test conditions	Test point	Switch conditions						
			S1	S2	S3	S4	S5	S6	S7
Circuit current	Measure current when no signal is present.	Ammeter	1	1	1	1	1	1	2
HF voltage output	Input 156 mV_{p-p} sine wave to A and B (f = 500kHz)	20	1	2	2	1	1	1	1
HF frequency characteristics	Input 156 mV_{p-p} sine wave to A and B $20 \log \frac{\text{(output at 2 MHz)}}{\text{(output at 20 kHz)}}$	20	1	2	2	1	1	1	1
HF output voltage "H"	Apply 3 VDC to A and B.	20	1	1	1	1	1	1	1
HF output offset voltage	Output voltage vs. V_{ref} when no signal	20,11	1	1	1	1	1	1	1
FE voltage output	Input 156 mV_{p-p} sine wave to A (f = 1 kHz)	13	1	2	1	1	1	1	1
FE output voltage "H"	Apply 2 VDC to A.	13	1	1	1	1	1	1	1
FE output voltage "L"	Apply 3 VDC to A.	13	1	1	1	1	1	1	1
FE output offset voltage	When no signal	13	1	1	1	1	1	1	1
TE voltage output	Input 38.4 mV_{p-p} sine wave to E (f = 1 kHz)	23	3	1	1	1	1	1	1
TE output voltage "H"	Apply 3 VDC to E.	23	1	1	1	1	1	1	1
TE output voltage "L"	Apply 2 VDC to E.	23	1	1	1	1	1	1	1
TE output offset voltage	When no signal	23	1	1	1	1	1	1	1
HFOK output voltage "H"	Apply 3 VDC to A and B.	14	1	1	1	1	1	1	1
HFOK output voltage "L"	When no signal	14	1	1	1	1	1	1	1
HFOK threshold voltage	Apply DC voltage to A and B. HFD output voltage (vs. V_{ref}) when HFOK is "H"	14,20,11	1	1	1	1	1	1	1
MR output voltage "H"	When no signal	17	1	1	1	1	1	1	1
MR output voltage "L"	Input 1.5 V_{p-p}, f = 500 kHz via capacitor to terminal ⑲	17	1	1	1	1	1	2	1
Envelope level ratio (when NORMAL)	When S5 is "1", input f = 500 kHz, 1.5 V_{p-p}. Adjust 50 k VR so that when S5 is turned to "2", MR output is about to turn to "L" (with pulses generated). Level ratio = $\frac{\text{(input amplitude immediately before "L")}}{1.5\ V_{p-p}}$	17,19	1	1	1	1	1↕2	3	1
Envelope level ratio (when JUMP)	When S5 is "1", input f = 500 kHz, 1.5 V_{p-p}. Adjust 50 k VR so that when S5 is turned to "2", MR output is about to turn to "L" (with pulses generated). Level ratio = $\frac{\text{(input amplitude immediately before "L")}}{1.5\ V_{p-p}}$	17,19	1	1	1	2	1↕2	3	1
MR frequency characteristics	1.5 Vp-p, f = 500 kHz (carrier). Frequency when MR output pulses are about to turn to "L" when AM modulation is put into effect at 55%.	17	1	1	1	2	1	2	1

TEST CIRCUIT



Units Resistance : Ω
Capacistance : F

M5204P

ANALOG OUTPUT AMPLIFIER WITH MUTE FUNCTION

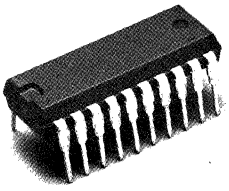
DESCRIPTION

The M5204P is an IC developed for analog voice signal processing for CD player applications. It has a built-in headphone amplifier and mute circuit.

Its applications cover miniature unit audio systems and tape decks, as well as CD players.

FEATURES

- Headphone amplifier built in ..... ILP = ± 40mA
- Large attenuation volume at muting ..... – 65dB (typ.)
- Low distortion ..... 0.004 %, f = 1kHz, 0dBm
- Maximum output voltage ..... 2.4Vrms (V_{CC} ± 5V)



Outline 20P4B

1.778mm pitch 300mil SDIP
(6.3mm × 19.0mm × 3.3mm)

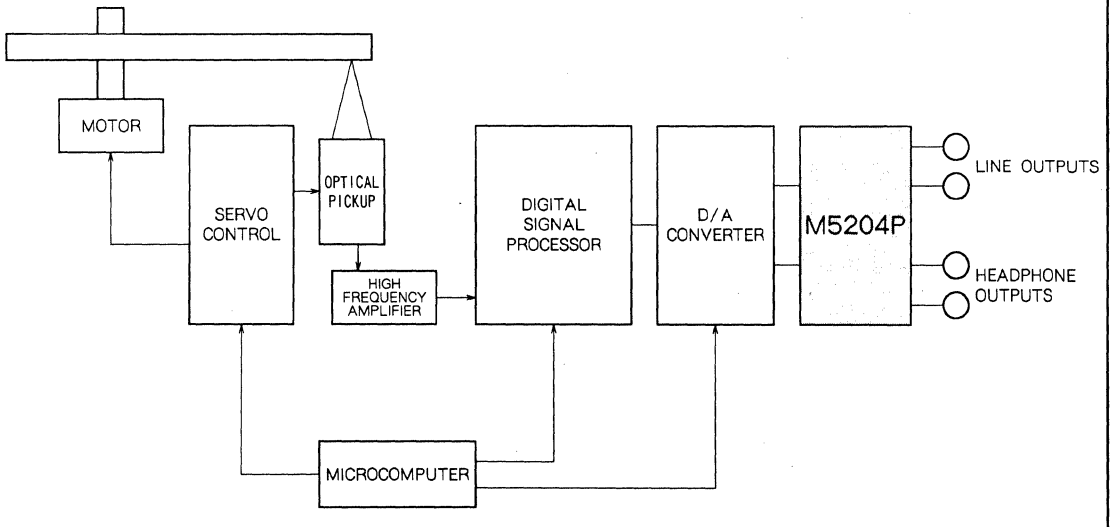
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC}, V_{EE} = ± 2 ~ ± 10V

Rated supply voltage ..... V_{CC}, V_{EE} = ± 5V

Rated power dissipation 1W

SYSTEM CONFIGURATION

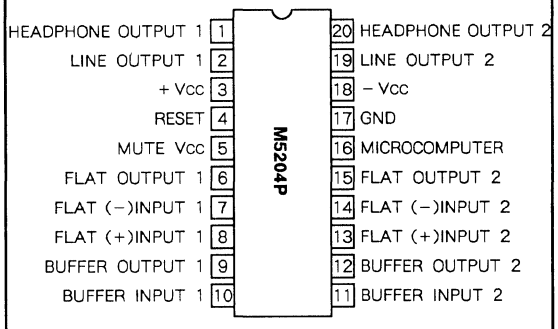


MITSUBISHI ELECTRIC

M5204P

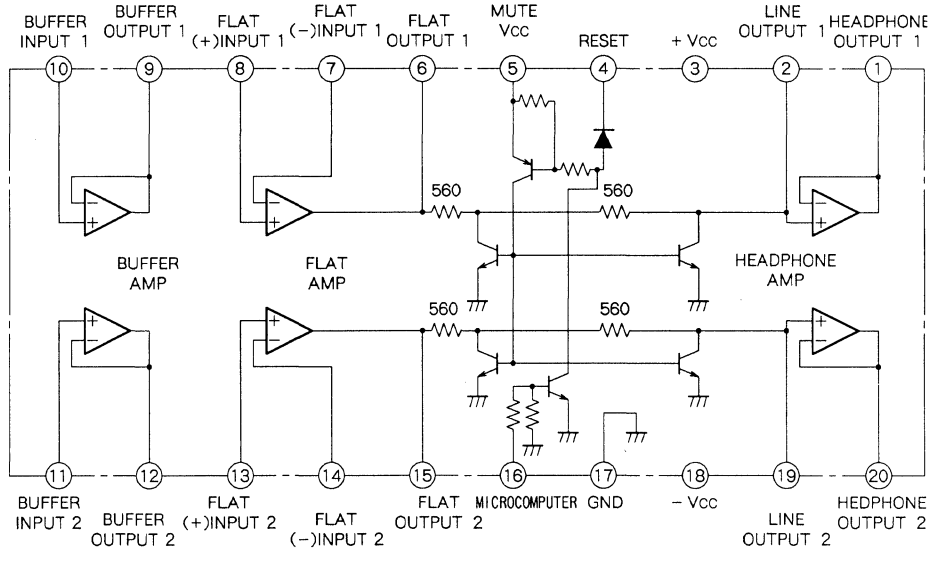
ANALOG OUTPUT AMPLIFIER WITH MUTE FUNCTION

PIN CONFIGURATION



Outline 20P4B

IC INTERNAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

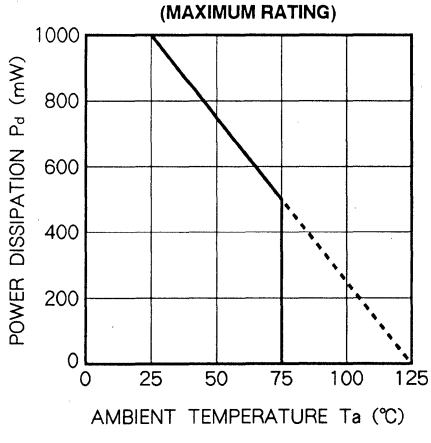
Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	± 10(20)	V
P_d	Power dissipation	1.0	W
K_θ	Thermal derating	10	mW/℃
T_{opr}	Operating temperature	− 20～+ 75	℃
I_{lp}	Lord current	± 40	mA

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = ± 5V)

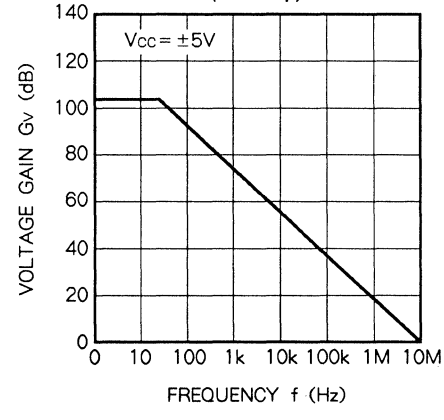
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	V_{in} = 0	5.8	11	16	mA
G_{V1}	Burffer voltage gain 1	f = 1kHz	− 1	0	1	dB
G_{V2}	Line voltage gain 2	f = 1kHz, R_1 = 68k Ω, R_2 = 82k Ω	5.5	6.5	7.5	dB
V_{O1}	Line output voltage 1	f = 1kHz, THD = 0.1 %, R_L = 47k Ω	−	2.4	−	Vrms
V_{O2}	Headphone output voltage 2	f = 1kHz, THD = 1 %, R_L = 30 Ω, R_S = 150 Ω	−	280	−	mVrms
THD	Total harmonic distortion	f = 1kHz, R_L = 47k Ω, V_O = 2Vrms	−	0.009	−	%
		f = 1kHz, R_L = 47k Ω, V_O = 1Vrms	−	0.0035	0.05	
ATT_1	Attenuation 1	f=1kHz, V_{in}=350mVrms, reset pin ④=0. 5V	60	68	−	dB
ATT_2	Attenuation 2	f=1kHz, V_{in}=350mVrms, microcomputer pin⑯=5V	−	68	−	dB
I mute1	Mute current 1	Vmute = 3V, reset pin ④= 0.5V	−	1.5	3	mA
I mute2	Mute current 2	Vmute = 3V, microcomputer pin ⑯= 5V	−	1.7	3	mA
I Microcomputer	I Microcomputer current	Vmute = 3V, microcomputer pin ⑯= 5V	−	90	500	μA
V_{IO}	Offset voltage		−	4	−	mV
CS	Channel separation		−	68	−	dB
V_{NO}	Output noise voltage		−	7	−	μVrms

TYPICAL CHARACTERISTICS

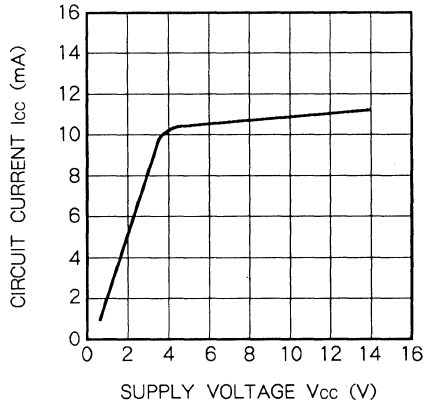
THERMAL DERATING
(MAXIMUM RATING)



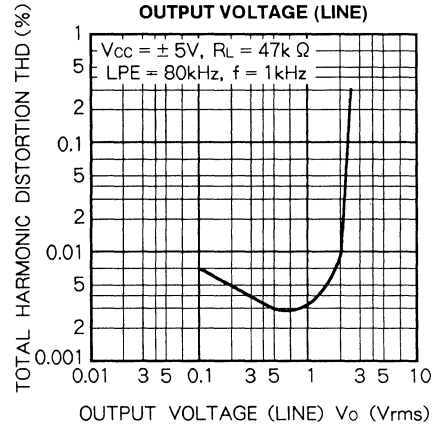
VOLTAGE GAIN VS. FREQUENCY
(Flat Amp)



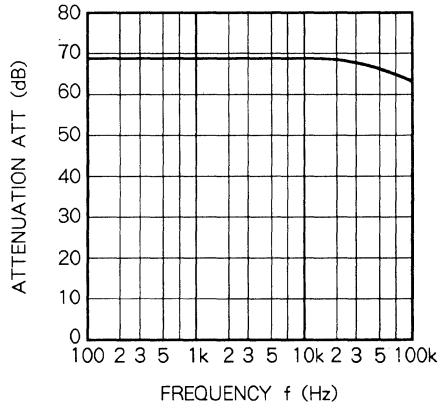
CIRCUIT CURRENT VS. SUPPLY VOLTAEGE



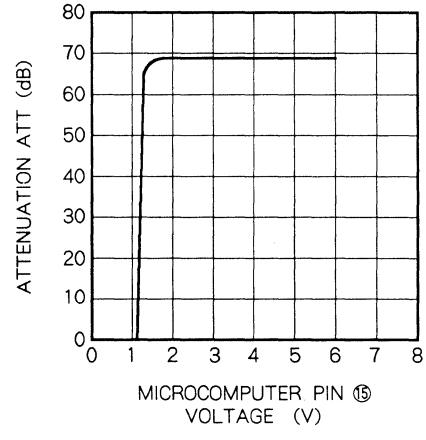
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE (LINE)



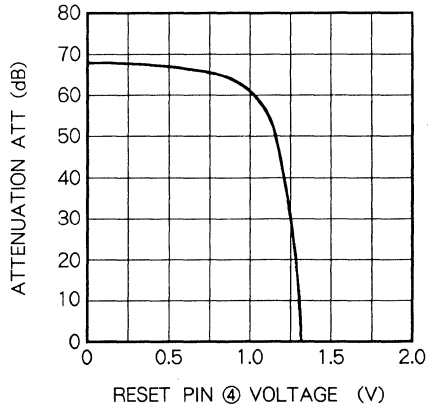
ATTENUATION VS. FREQUENCY



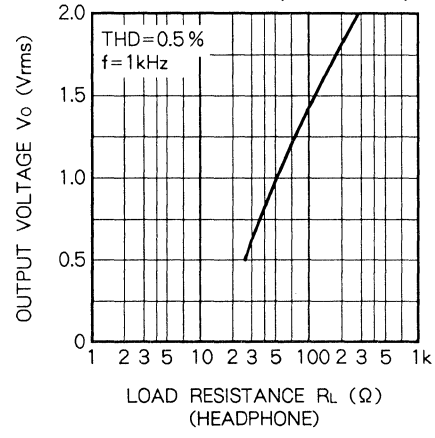
ATTENUATION VS. MICROCOMPUTER PIN ⑮ VOLTAGE



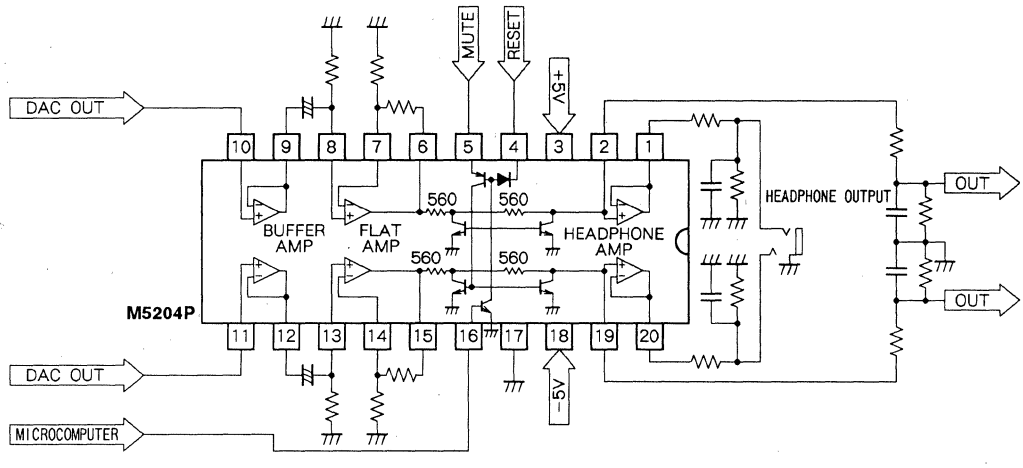
ATTENUATION VS. RESET PIN ④ VOLTAGE



OUTPUT VOLTAGE VS. LOAD RESISTANCE (HEADPHONE)



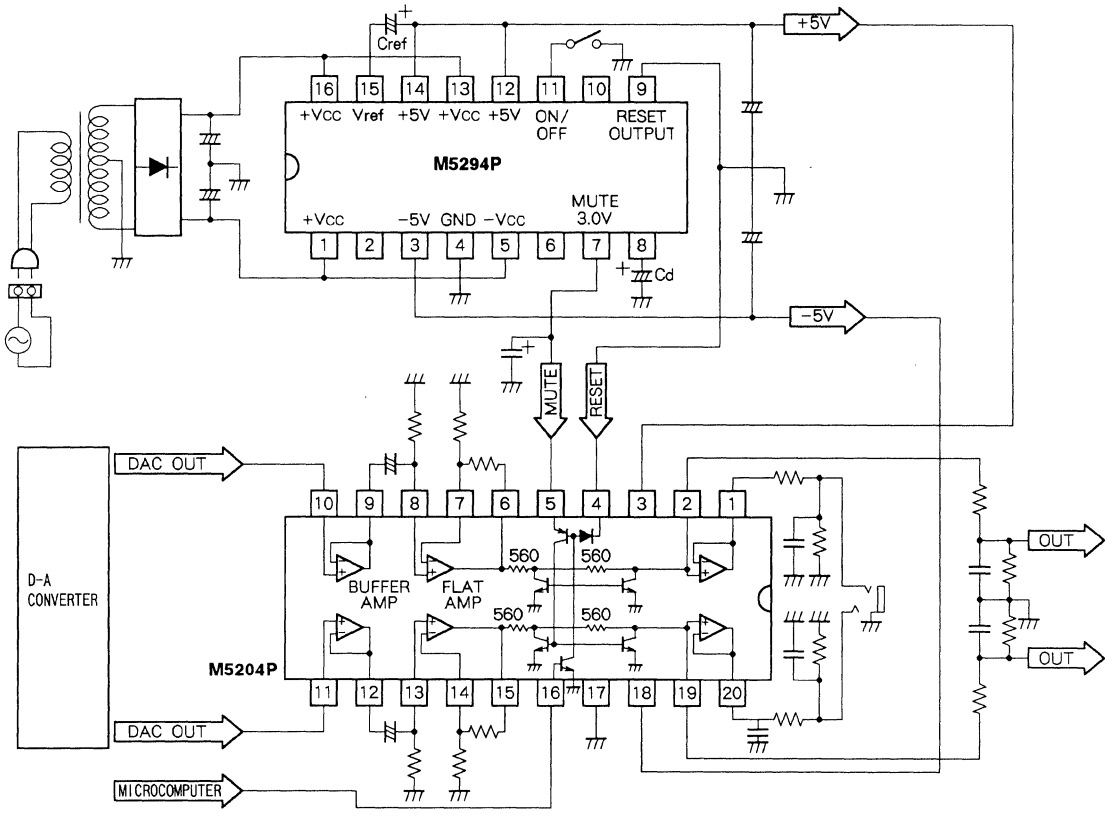
PIN EXPLENATION



PIN DESCRIPTION

Pin No.	Name	Function
①	Headphone output 1	This terminal is output pin for 1ch headphone amplifier.
②	Line output 1	This terminal is output pin for 1ch line amplifier.
③	(+)Vcc	+ Vcc supply line. Usually, + Vcc is 5V.
④	Reset	This is mute control terminal. 0V→mute ON.
⑤	Mute Vcc	Mute supply line. Usually, this terminal voltage to 3V.
⑥	Flat output 1	The feedback resistor insert between the (−) input terminal pin ⑦ and output terminal pin ⑥. It is setting the flat amplifier voltage gain.
⑦	Flat (−) input 1	
⑧	Flat (+) input 1	The coupling capacitor and resistor insert between the pin ⑨ and pin ⑧. It is setting the high pass filter.
⑨	Buffer output 1	These terminal are a buffer amplifier. It is the voltage follower, that gain is 0dB.
⑩	Buffer input 1	
⑪	Buffer input 2	Pin⑨ and ⑩ are 1 channel. Pin⑪ and ⑫ are 2 channel.
⑫	Buffer output 2	
⑬	Flat (+) input 2	The coupling capacitor and resistor insert between the pin ⑬ and pin ⑫. It is setting the high pass filter.
⑭	Flat (−) input 2	The feedback resistor insert between the (−) input terminal pin ⑭ and output terminal pin ⑮. It is setting the flat amplifier voltage gain.
⑮	Flat output 2	
⑯	Microcomputer	This is mute control terminal from microcomputer. It keep the "H" level, when mute circuit active on.
⑰	GND	This is GND terminal.
⑱	(−)Vcc	− Vcc supply line. Usually, − Vcc is − 5V.
⑲	Line output 2	This terminal is output pin for 2ch line amplifier.
⑳	Headphone output 2	This terminal is output pin for 2ch headphone amplifier.

APPLICATION EXAMPLE

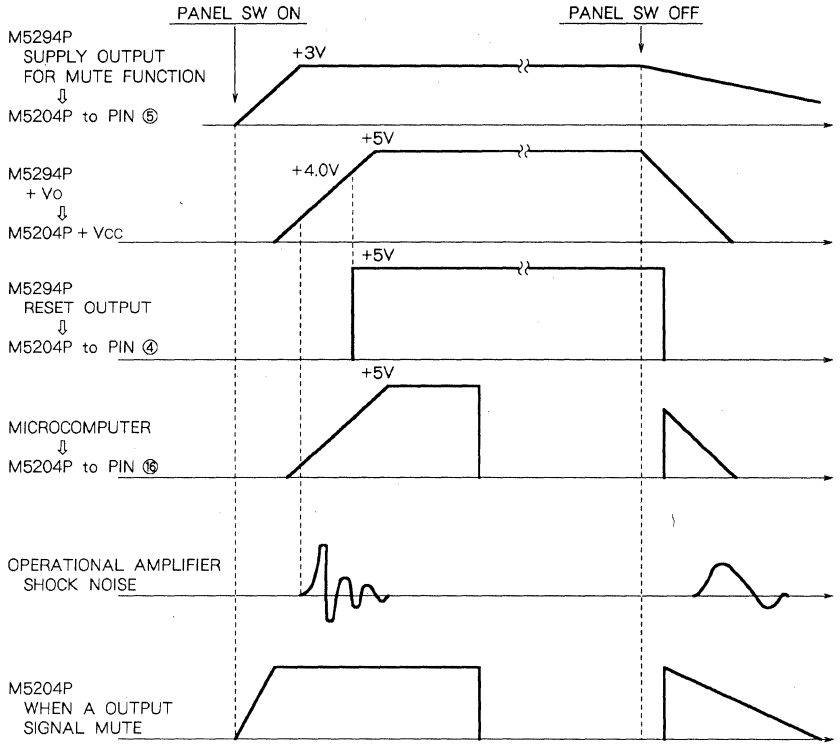


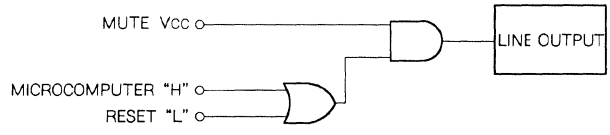
M5294P is a semiconductor integrated circuit designed for dual tracking type voltage regulator, which includes system reset circuit, and 3.0V regulator for mute function.

Since the output voltage (± 5V, 3V) are fixed inside, and this IC includes pull-up registor (10k Ω) of reset output, user can omit the outside parts, ± 5V output is low power dissipation type, that is to say, this is able to operate even if input-output voltage difference is very low status such as 0.2V (@ Io = ± 100mA). Therefor, user can shrink the input transformer.

User can protect to make a noise by means of operating mute to function before power supply (± 5V) of amplifier starts up, since 3.0V regulator for mute function starts up earlier than ± 5V output.

TIMING CHART





M5285FP

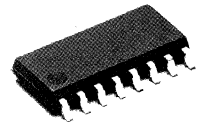
ANALOG OUTPUT AMPLIFIER WITH MUTE FUNCTION

DESCRIPTION

The M5285FP is an IC developed for analog voice signal processing for CD player applications. It has a built-in mute circuit. Its applications cover miniature unit audio systems and tape decks, as well as CD players.

FEATURES

- Large attenuation volume at muting ····· – 65dB(typ)
- Low distortion ····· 0.004 %, f = 1kHz, 0dBm
- Maximum output voltage ····· 2.4Vrms(V_{CC} = ± 5V)



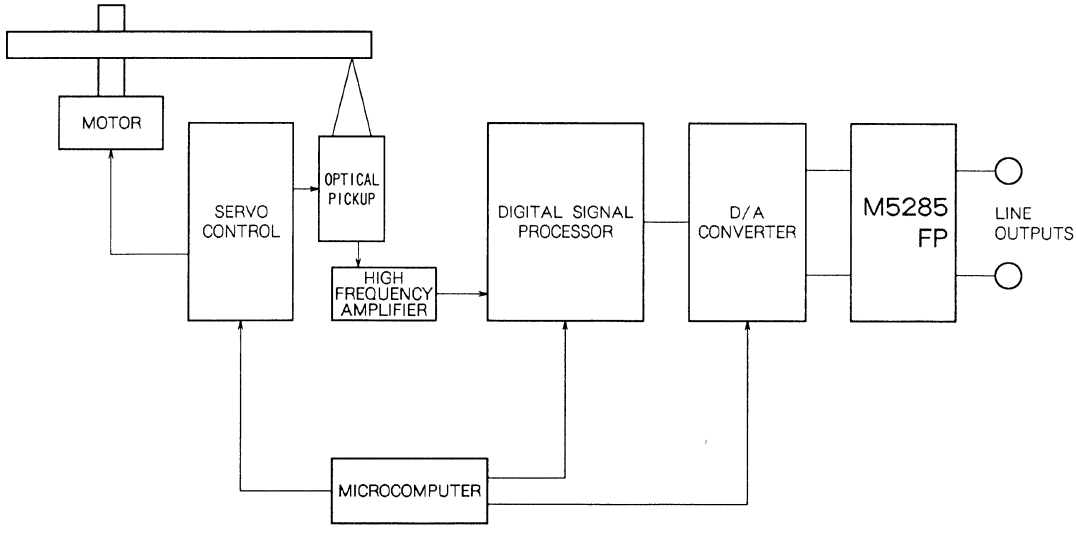
Outline 16P2S-A

1.27mm pitch 225mil SOP
(4.4mm × 10.0mm × 1.5mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· V_{CC}, V_{EE} = ± 2~10V
Rated supply voltage ····· V_{CC}, V_{EE} = ± 5V
Rated power dissipation ····· 1W

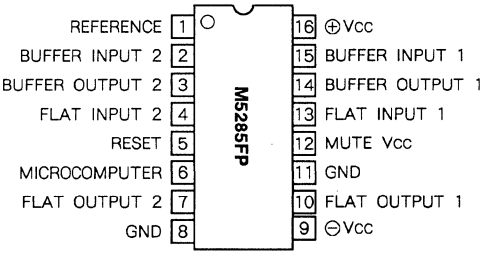
SYSTEM CONFIGURATION



M5285FP

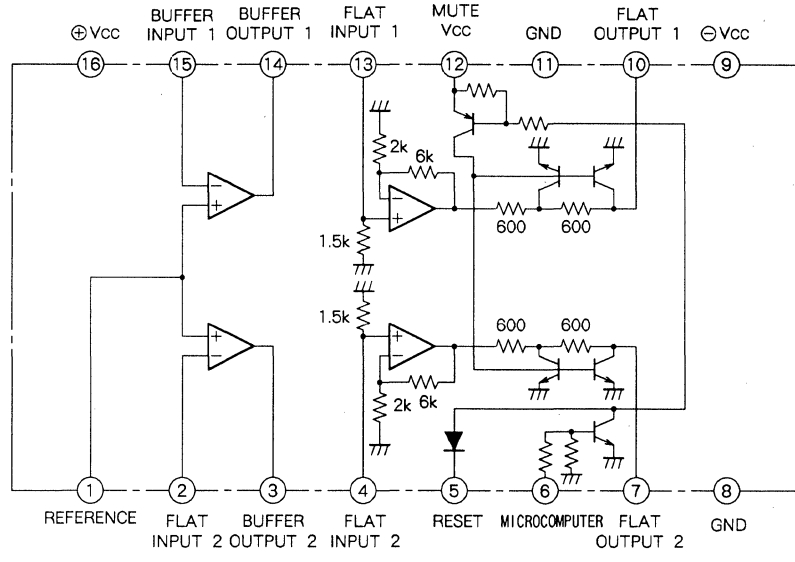
ANALOG OUTPUT AMPLIFIER WITH MUTE FUNCTION

PIN CONFIGURATION



Outline 16P2S-A

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

Note : Pin ⑧ and pin ⑪ not internally connected. Both pin ⑧ and pin ⑪ input be connected to GND.

PIN DESCRIPTION

Pin No.	Name	Function
①	Reference	⊕Input of buffer amplifier
②	Buffer input 2	Buffer Amplifier 2
③	Buffer output 2	
④	Flat input 2	Input pin for flat amplifier 2, Flat amplifier gain is + 12dB
⑤	Reset	Mute controll. 0V→Mute ON
⑥	Microcomputer	Mute control from microcomputer. It keep the high level, When mute circuit active
⑦	Flat output 2	Output pin for flat amplifier 2.
⑧	GND	GND
⑨	⊖Vcc	⊖Vcc supply usually, − Vcc is − 5V
⑩	Flat output 1	Output pin for flat amplifier 1
⑪	GND	GND
⑫	Mute Vcc	Mute supply line. usualiy 3V
⑬	Flat input 1	Input pin for flat amplifier 1. Flat amplifier gain is + 12dB.
⑭	Buffer output 1	Buffer Amplifier 1
⑮	Buffer input 1	
⑯	⊕Vcc	⊕Vcc supply, usually 5V

pin⑧ and pin⑪ are not internally connected. Both pin⑧ and pin⑪ must be connected to GND.

ABSOLUTE MAXMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	± 7.5(15)	V
P_d	Power dissipation	550	mW
K_θ	Thermal derating	5.5	mW/℃
T_{opr}	Operating temperature	− 20∼ + 75	℃

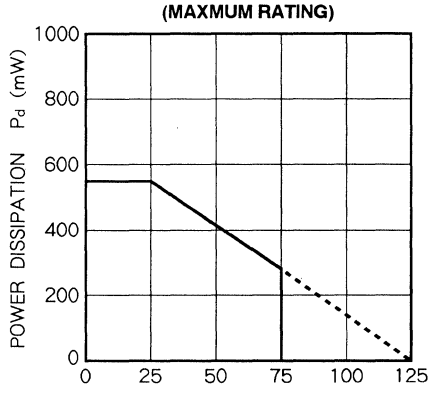
ELECTRICAL CHARACTERISTICS (V_{CC} = ± 5V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Icc	Circuit current	V_{in} = 0	−	11	19	mA
Gv	Voltage gain	f = 1kHz, R_L : No load	11	12	13	dB
THD	Total harmonic distortion	f = 1kHz, R_L = 47k Ω, V_O = 2Vrms BPF : 400Hz∼30kHz	−	0.002	0.005	%
ATT1	Attenuation 1	f=1kHz, V_O = 0dBm(Before muteing) Reset⑤=0V	55	64	−	dB
ATT2	Attenuation 2	f=1kHz, V_O = 0dBm(Before muteing) Reset⑥=5V	55	64	−	dB
I mute1	Mute current 1	Vmute = 3V, reset⑤= 0V	−	2	3.5	mA
I mute2	Mute current 2	Vmute = 3V, microcomputer⑥= 5V	−	2	3.5	mA
I Microcomputer	Microcomputer current	Vmute = 3V, microcomputer⑥= 5V	−	90	300	μA
Vo	Offset voltage		−	3.2	−	mV
CS	Channel separation	Monitor side, LPF : 20kHz Opposite side : f = 1kHz, V_O = 0dBm	−	94	−	dB
VNo	Output noise voltage	* Note	−	12	−	μVrms

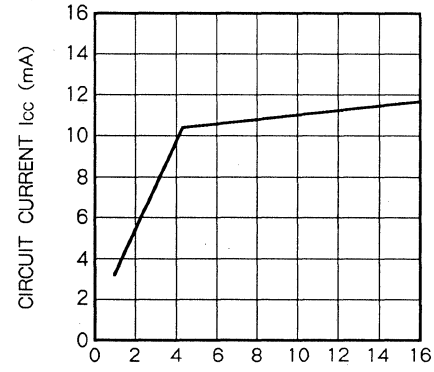
Note : Because Input-referred noise voltage VNI is $\frac{12\mu Vrms}{4}$ = 3μVrms, flat amplifier gain is + 12dB.

TYPICAL CHARACTERISTICS

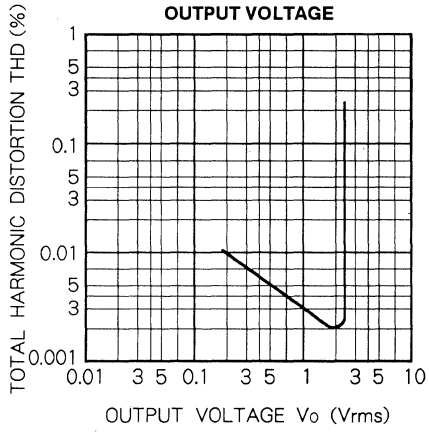
THERMAL DERATING (MAXMUM RATING)



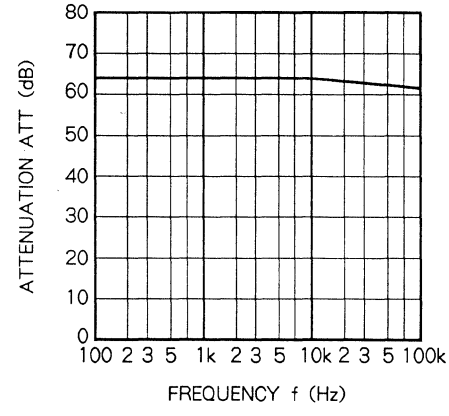
CICUIT CURRENT VS. SUPPLY VOLTAGE



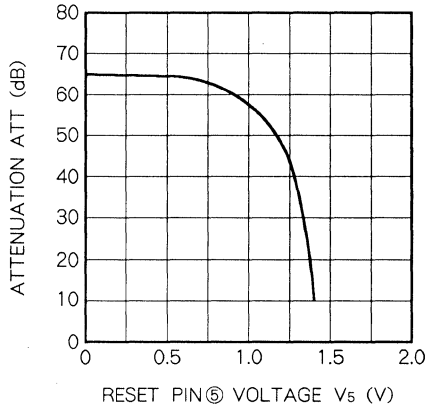
TOTAL HARMONIC DISTRTTION VS. OUTPUT VOLTAGE



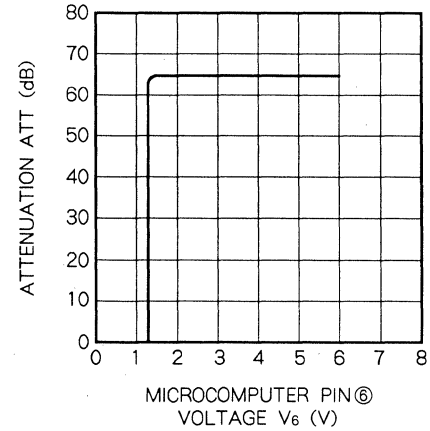
ATTENUATION VS. FREQUENCY



ATTENUATION VS. RESET PIN ⑤ VOLTAGE



ATTENUATION VS. MICROCOMPUTER PIN ⑥ VOLTAGE



DIGITAL AUDIO INTERFACE ICs

6

M51581FP

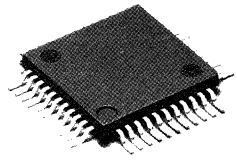
DIGITAL AUDIO INTERFACE (DAI)

DESCRIPTION

The M51581FP is a semiconductor IC for transmitting and receiving signals formed according to a digital audio interface format conforming to the EIAJ standards. It has a variety of functions as it supports both professional and consumer modes and can be applied to the serial copy management systems (SCMS). The IC enables the engineer to configure an optimum digital audio interface for DAT, DCC, MD, and CD-R systems.

FEATURES

- Capable of dealing with audio data up to 24-bit
- Adaptable to both the I²S and non-I²S audio interface formats
- Selection available from three kinds of control methods (microcomputer, easy, and full-transparent modes)
- Two channels of signal input pins for reception
- Feedthrough function equipped
- Level converter for converting the level of received signals into CMOS level (minimum input level : 200mVp-p)
- Supports both consumer and professional modes



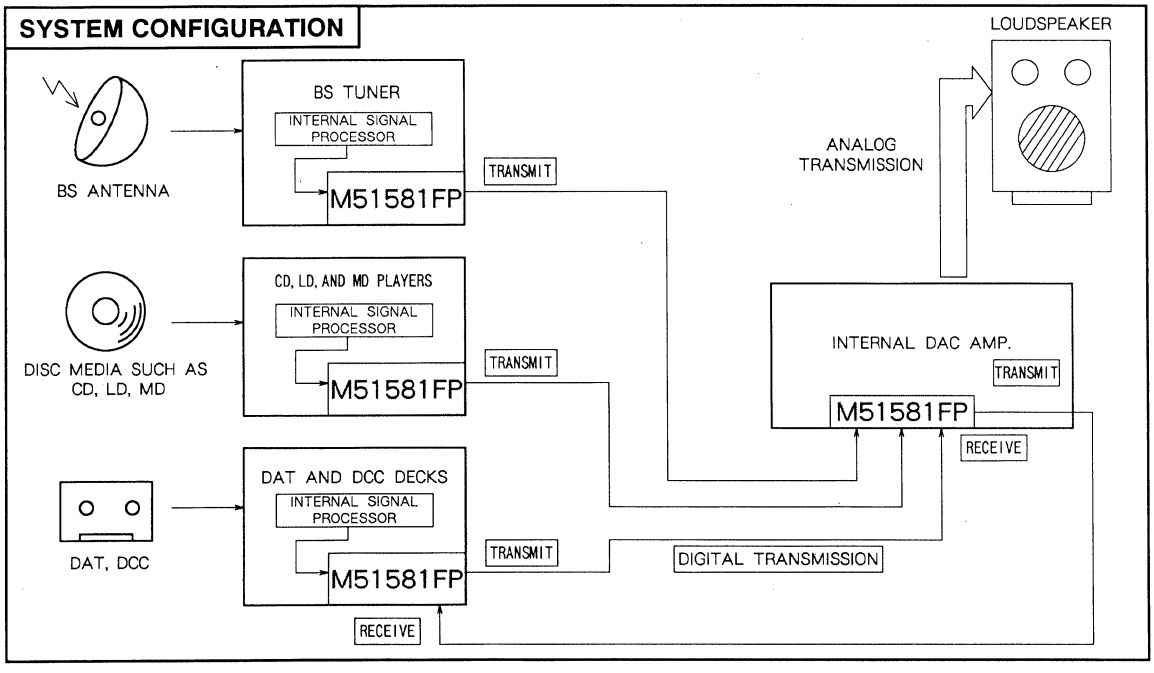
Outline 44P6W-B

1.0mm pitch QFP
(13.2mm × 13.2mm × 2.0mm)

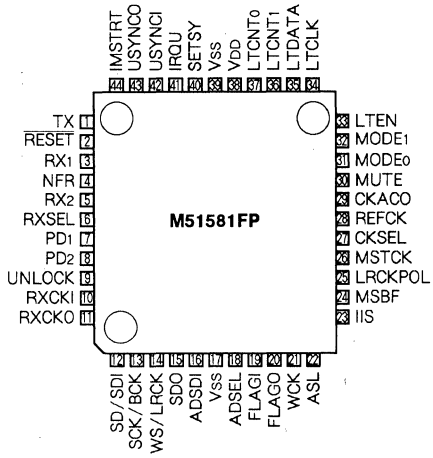
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{DD} = 4.5~5.5V
Rated supply voltage ..... V_{DD} = 5V

SYSTEM CONFIGURATION

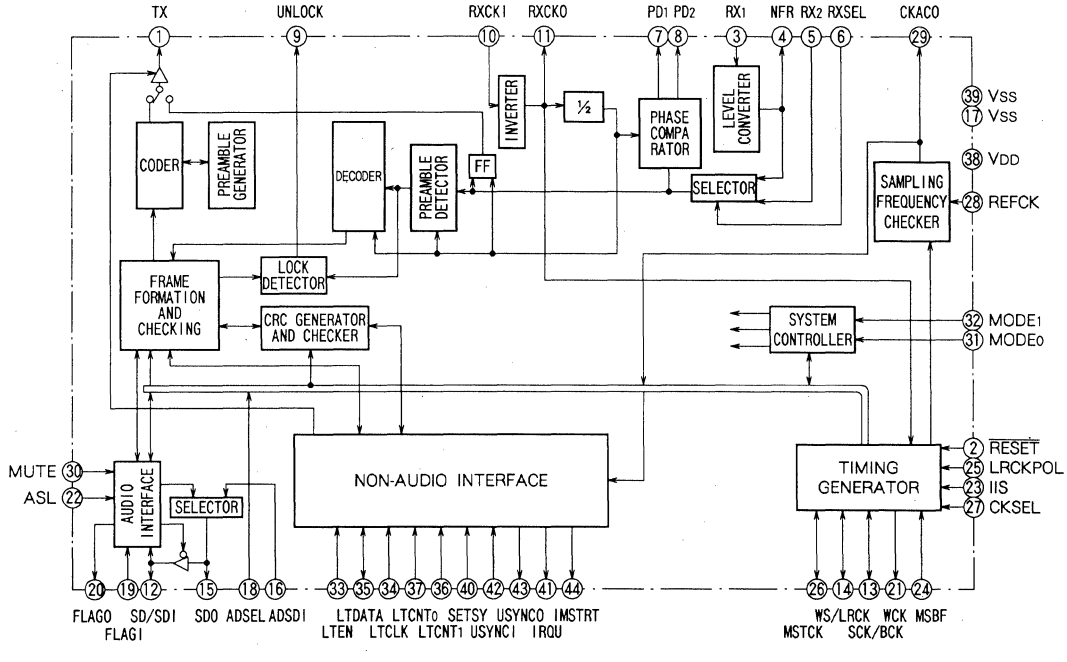


PIN CONFIGURATION



Outline 44P6W-B

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

COMMON PINS (O"and Bi denote tri-state output and bi-directional transmission, respectively.)

Pin No.	Name	I/O	Function
①	TX	O"	Digital audio data output in EIAJ format
②	$\overline{\text{RESET}}$	I	Reset : "0" = reset (in microcomputer mode : fs = 48kHz, TX disabled)
③	RX_1	I	Digital audio data input 1 in EIAJ format : for input via coaxial cable(200mVp-p min.)
④	NFR	O	RX_1 level converter output (Connect a feedback resistor.)
⑤	RX_2	I	Digital audio data input 2 in EIAJ format : for input via optical cable(CMOS level)
⑥	RXSEL	I	RX input selection : "1" = RX_1 ; "0" = RX_2. In microcomputer mode, this pin is for selecting the polarity of RXSEL
⑦	PD_1	O	Output of phase detector for charge pump VCO
⑧	PD_2	O	
⑨	UNLOCK	O	Output of unlock detector : "1" = unlock
⑩	RXCKI	I	VCO clock input (256fs)
⑪	RXCKO	O	VCO clock output ($\overline{\text{RXCKI}}$)
⑫	SD/SDI	Bi/I	Serial audio data input/output (input only except for I^2S format)
⑬	SCK/BCK	Bi	Audio data bit clock input/output
⑭	WS/LRCK	Bi	Audio data word select input/output
⑮	SDO	O	Serial audio data output
⑯	ADSDI	I	Serial audio data input from AD converter
⑰	V_{SS}	–	Ground
⑱	ADSEL	I	Serial audio data source selection : "1" = analog (AD converter) ; "0" = digital (RX) ; in microcomputer mode, this pin is for selecting the polarity of ADSEL
⑲	FLAGI	I	Error flag input
⑳	FLAGO	O	Error flag output
㉑	WCK	O"	Word clock output (2fs at reception)
㉒	ASL	I	Audio data sampling length selection : "1" = 24 bits ; "0" = 16 bits
㉓	IIS	I	Audio data format selection : "1" = I^2S ; "0" = Any other format than I^2S
㉔	MSBF	I	MSB selection : "1" = MSB first ; "0" = LSB first
㉕	LRCKPOL	I	LRCK polarity selection : "1" = Lch→1 ; "0" = Lch→0
㉖	MSTCK	Bi	Master clock input/output (128fs or 256fs)
㉗	CKSEL	I	Master clock frequency selection : "0" = 256fs ; "1" = 128fs
㉘	REFCK	I	Reference clock input for checking the accuracy of sampling frequency (9.408MHz)
㉙	CKACO	O	Checking result output of the accuracy of sampling frequency : "1" = ± 0.14 % or more of frequency error
㉚	MUTE	I	Mute control : "1" = mute ; In microcomputer mode, this pin is for selecting the polarity of mute control
㉛	$MODE_0$	I	Mode selection : ($MODE_1$, $MODE_0$) "0, 0" = microcomputer mode "0, 1" = easy mode "1, 0" = full-transparent mode "1, 1" = test mode
㉜	$MODE_1$	I	
㊳	V_{DD}	–	Power supply
㊴	V_{SS}	–	Ground

EASY MODE (PROFFESIONAL), (at ㊵pin "TYPE"="1")

Pin No.	Name	I/O	Function
㉝	IN/OUT	I	Transmission selection : "1"= receive ; "0"= transmit
㉞	PSL	Bi	Professional audio data sampling length selection:"1"=24 bits; "0"=20 bits
㉟	CRCO	O	CRC checking result output : "1"= error
㊱	TXOE	I	TX output enable : "1"= enable
㊲	FSINSEL	I	fs information selection(in reception) : "0"= fs information on C-bits, "1"= detected fs
㊵	TYPE	Bi	Type information "1"= Type I (professional="1")
㊶	FS_0	Bi	fs information (in transmission : input) / fs information (in reception : output)
㊷	FS_1	Bi	(FS_0, FS_1) "0, 0"= 48kHz default; "0, 1"= 48kHz; "1, 0"= 44.1kHz; "1, 1"= 32kHz / fs information on C-bits(FSINSEL="0"): "0, 0"=48kHz default; "0, 1"=48kHz; "1, 0"=44.1kHz; "1, 1"=32kHz / Detected fs (FSINSEL="1"): 44.1kHz="0, 0"; 48kHz="1, 0"; 32kHz="1, 1"
㊸	PLOCK	Bi	Source lock information : "1"= unlock
㊹	EMP	Bi	Emphasis information : "1"= 50μ/15μsec

EASY MODE (CONSUMER), (at ㊵pin "TYPE"="0")

Pin No.	Name	I/O	Function
㉝	IN/OUT	I	Transmission selection : "1"= receive ; "0"= transmit
㉞	CAT_0	Bi	Category information : (CAT_1, CAT_0) "0, 0"= general; "0, 1"= CD; "1, 0"= BS; "1, 1"= DAT
㉟	CAT_1	Bi	
㊱	TXOE	I	TX output enable : "1"= enable ; "0"= disable (high impedance)
㊲	FSINSEL	I	fs information selection(in reception) : "0"= fs information on C-bits ; "1"= detected fs
㊵	TYPE	Bi	Type information : "0"= Type II (consumer="0")
㊶	FS_0	Bi	fs information (in transmission : input) / fs information (in reception)
㊷	FS_1	Bi	(FS_0, FS_1) "0, 0"= 44.1kHz; "0, 1"= 48kHz; "1, 1"= 32kHz / fs information on C-bits(FSINSEL="0"): "0, 0"=44.1kHz default; "0, 1"=48kHz; "1, 1"=32kHz / Detected fs (FSINSEL="1"): 44.1kHz="0, 0"; 48kHz="1, 0"; 32kHz="1, 1"
㊸	COPY	Bi	Copy information : "1"= enable
㊹	EMP	Bi	Emphasis information : "1"= 50μ/15μsec

MICROCOMPUTER MODE (LT BUS MODE)

Pin No.	Name	I/O	Function
㉝	LTEN	I	LT interface enable : "1" = enable
㉞	LTCLK	I	Bit clock input for LT interface data
㉟	LTDATA	Bi	LT interface data input/output
㊱	$LTCNT_1$	I	LT interface control : ($LTCNT_1$, $LTCNT_0$) "0, 0" = C-bit data "0, 1" = U-bit data "1, 0" = setting "1, 1" = status
㊲	$LTCNT_0$	I	
㊵	SETSY	I	Setting latch clock input
㊶	IRQU	O	U-bit data information message indicator output
㊷	USYNCI	I	U-bit data unit indicator input (in transmission)
㊸	USYNCO	O"	U-bit data unit indicator output (in reception)
㊹	IMSTRT	O	U-bit data message start indicator output

FULL-TRANSPARENT MODE

Pin No.	Name	I/O	Function
㉝	IN/OUT	I	Transmission selection : "1" = receive ; "0" = transmit
㉞	BKSYO	O	C-bit block sink output (preamble "B" detected)
㉟	CRCO	O	CRC check output : "1" = error
㊱	TXOE	I	TX output enable : "1" = enable
㊲	$DETFS_0$	O	Detected fs ($DETFS_0$, $DETFS_1$) 44.1kHz = "0, 0" 48kHz = "1, 0" 32kHz = "1, 1"
㊵	$DETFS_1$	O	
㊶	$CDAT_1$	I	C-bit data input
㊷	CDATO	O	C-bit data output
㊸	$UDAT_1$	I	U-bit data input
㊹	UDATO	O	U-bit data input

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage	−0.3	−	6.5	V
Pd	Power dissipation	−	−	600	mW
V_I	Input voltage	−0.3	−	V_{DD}+0.3	V
V_O	Output voltage	−0.3	−	V_{DD}+0.3	V
I_O	Output current	−	−	± 16	mA
Topr	Operating temperature	−30	−	70	℃
Tstg	Storage temperature	−50	−	125	℃

RECOMMENDED OPERATING CONDITIONS (V_{DD} = 5V, Ta = − 30℃~70℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Supply voltage		4.5	5.0	5.5	V
V_{IL}	Input voltage ("L" level)	V_{DD} = 4.5V	0	−	1.35	V
V_{IH}	Input voltage ("H" level)	V_{DD} = 5.5	3.85	−	V_{DD}	V
tri	Input rise time		−	−	500	ns
tfi	Input fall time		−	−	500	ns
L_I	Input leak current	V_I = 0, V_{DD}	−	−	± 1	μA
I_{OL}	Output current ("L" level)	V_{OL} = 0.4V, V_{DD} = 4.5V	14	−	−	mA
I_{OH}	Output current ("H" level)	V_{OH} = 4.1V, V_{DD} = 4.5V	−	−	− 5	mA
V_{OL}	Output voltage ("L" level)	I_{OL} < 1 μA	4.95	−	−	V
V_{OH}	Output voltage ("H" level)	I_{OH} < − 1 μA	−	−	0.05	V

All inputs are at CMOS level

FUNCTION DESCRIPTION

1. Reset conditions

(1) Reset action

(a) All setting bits are set to 0 (in microcomputer mode)
Transmission mode ADSEL, TEST, BCKPOL, MUTE, RXSEL, TXOE, NOWD = 0

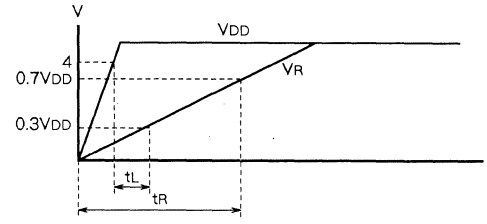
(b) The lock detector is initialized

(c) The sampling frequency accuracy checker is initialized

(2) Master clock

While resetting, the master clock should not necessarily be supplied. (It is also permissible to supply it.)

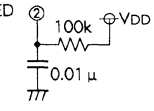
(3) Reset time



RECOMMENDED OPERATING CONDITIONS FOR RESETTING

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
tL	L level hold time	V_{DD} > 4V~V_R < 0.3V_{DD}	50	−	−	μs
tR	L level reset time	V_{DD} = 5V, CR = 100k/0.01 μ	−	1.2	−	ms

RECOMMENDED CIRCUIT



2. RECOMMENDED OPERATING CONDITIONS FOR RX1 INPUT VOLTAGE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IRX1}	RX1 input voltage	fs < 50kHz	200m	−	V_{DD}	V_{P-P}

3. Audio Interface

(1) Format I²S/non-I²S

(2) Number of significant bits 16bits/24bits

(3) Error flag

If one of the following conditions occurs in reception mode, an error flag is sent

- Validity flag = 1(error)
- Parity check result = 1(error)
- PLL does not lock

(4) Preceding-value holding

If the result of parity check is an error, the preceding value in audio data is held

(5) Mute

If PLL is unlocked in reception mode, the signal is muted automatically. In addition, it is possible to mute a signal compulsively with the MUTE pin

4. Non audio Interface

Non audio data includes the following

- Channel status
- User data
- Settings (to set IC operating conditions)
- Status (Monitored IC operating conditions)

Control methods as shown below are available for non audio data

MODE00 – Microcomputer mode

In this mode the M51581FP is controlled by a microcomputer via LT bus by serial data

MODE01 – Easy mode

The M51581FP is controlled by means of dedicated pins

MODE10 – Full-transparent mode

In this mode a microcomputer is used to receive and process all bits of both C and U bits

5. Checking the accuracy of sampling frequency

It is possible by means of the sampling frequency checker to check whether received signals are within approximately ±0.14% of the reference value. With this checking function, recorded patterns on a DAT tape and the like are prevented from shifting. It is also possible to judge to which range of the three reference values (32k, 44.1k, or 48kHz) the sampling frequency of the received signal correspond (fs detection function). If these functions, sampling frequency accuracy check and fs detection, are not used, pin㉘ REFCK does not require the reference clock.

Fix pin㉘ to L in that case.

6. PLL lock detection

In the following conditions, PLL is judged to be unlocked

- No preamble has been detected
- Parity check resulted in two consecutive errors

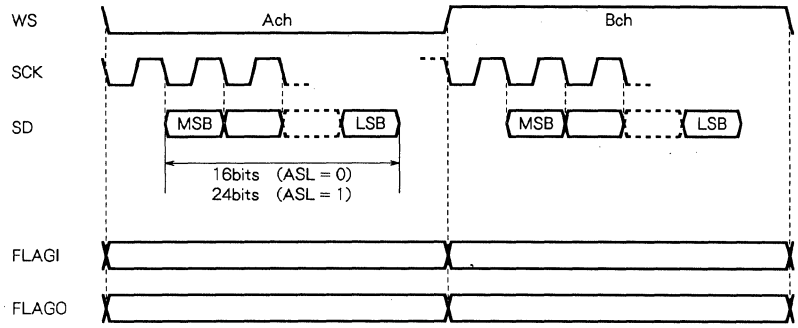
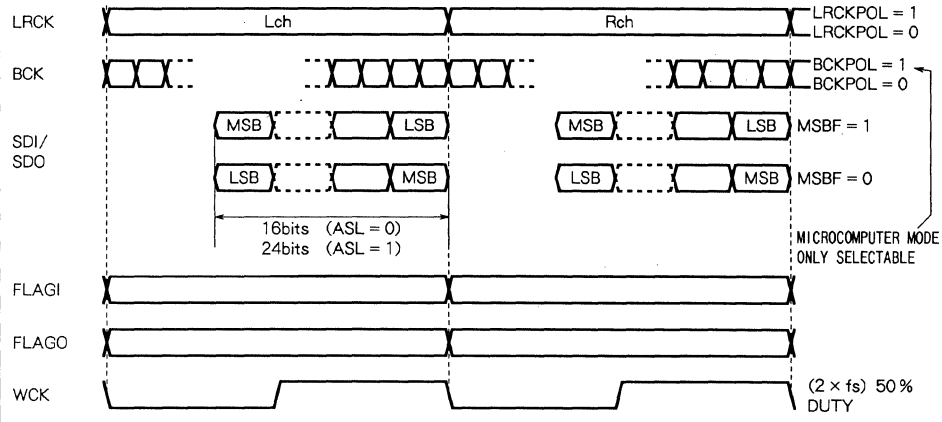
TIMING CHART

1. AUDIO INTERFACE FORMAT

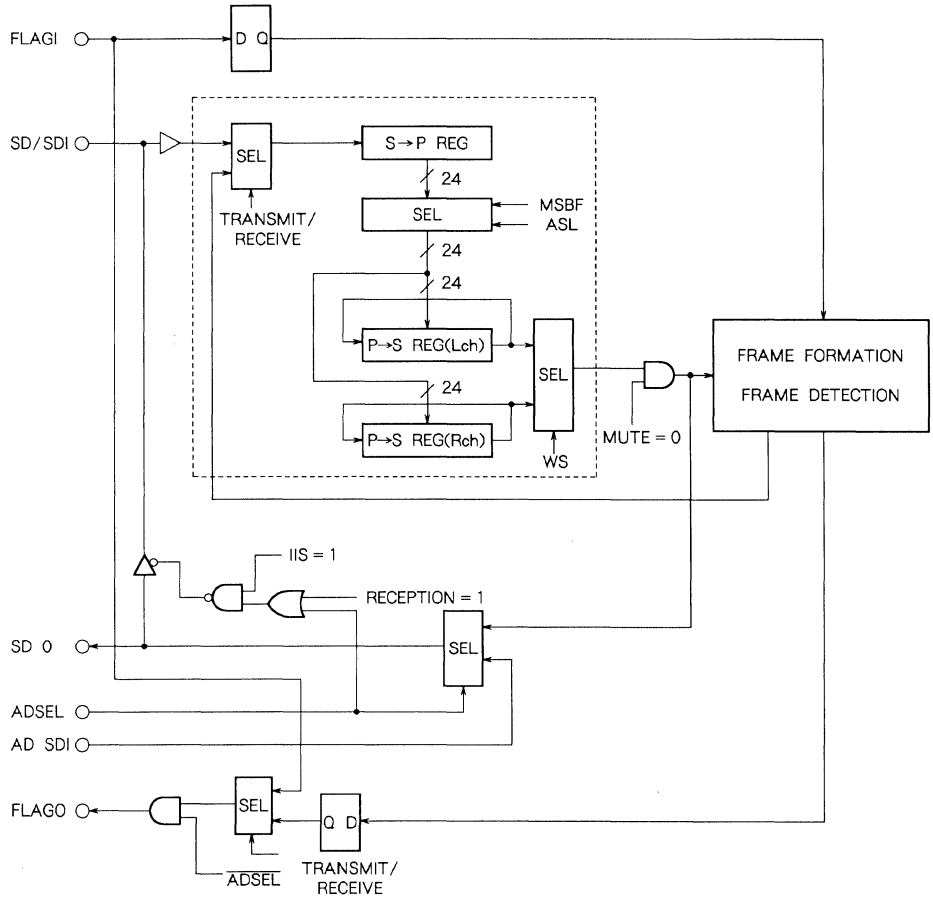
(1) Audio interface format conditions

Selection pin			Format	Audio data	WS/LRCK
IIS	MSBF	LRCKPOL			
1	1	0	I²S	MSB first 16bits (ASL = 0) 24bits (ASL = 1)	Ach = 0 Bch = 1
0	1	0	non-I²S	↑	Lch = 0 Rch = 1
	1	1		↑	Lch = 1 Rch = 0
	0	0		LSB first 16bits (ASL = 0) 24bits (ASL = 1)	Lch = 0 Rch = 1
	0	1		↑	Lch = 1 Rch = 0

(2) Audio interface format timing chart

Format	Timing chart
I²S (IIS = 1)	
non I²S (IIS = 0)	

(3) Audio interface block diagram



(4) Operation status of FLAGO, SD/SDI

DAT operation mode	DAI transmission	ADSEL	I^2S		non-I^2S	
			FLAGO	SD/SDI	FLAGO	SD/SDI
Reproduction	Transmit	"0"	FLAGI	Input	FLAGI	Input
Analog recording	Transmit	"1"	"0"	Output (ADSDI)	"0"	Input
Digital recording	Receive	"0"	Data on received V bits	Output (received data)	Data on received V bits	Input

2. MICROCOMPUTER MODE DATA FORMAT

(1) LTDATA selection

Signal name			Data contents of LTDATA
LTEN	$LTCNT_1$	$LTCNT_0$	
1	0	0	C-bit data
1	0	1	U-bit data
1	1	0	Setting (microcomputer→DAI)
1	1	1	Status (DAI→microcomputer)

(2) Settings (8-bit)

1	2	3	4	5	6	7	8

Bit	Function
1	Transmission selection : "1" = receive, "0" = transmit
2	ADSEL : Serial audio data source selection ; Polarity is determined by ADSEL (pin 18).(Note 1)
3	Test : Fixed to "0" normally
4	BCKPOL:Bit clock(BCK)polarity selection; If this bit is "0," BCK falls at LRCK edges
5	MUTE : Mute control ; Polarity is determined by MUTE(pin 30).(Note 1)
6	RXSEL:RX input selection;Polarity is determined by RXSEL(pin 6) (Note 1)
7	TXOE : TX output enable ; "1" = enable
8	NOWD : Timing control for USYNCI and USYNCO ; "0" = no delay, "1" = 4WS delay

(3) Status (8-bit) (8-bit)

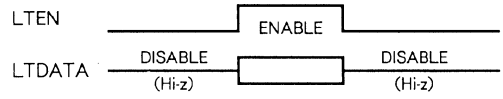
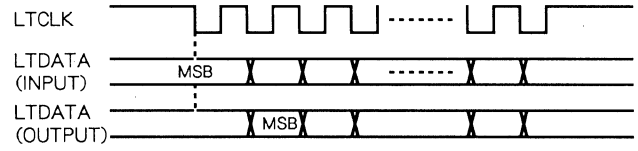
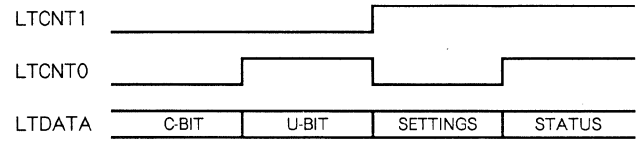
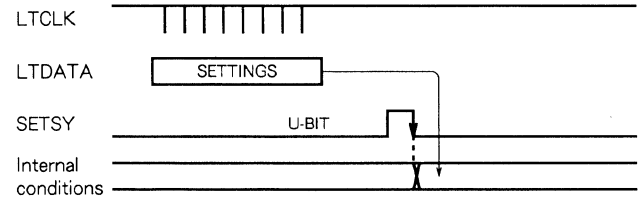
1	2	3	4	5	6	7	8

Bit	Function
1	UNLOCK : PLL unlock information ; "1" = unlock
2	CKACO : Output sampling frequency accuracy check ; "1" = frequency error greater than ± 0.14 %
3	DETFS0 ⎫ Detected fs (DETFS0, DETFS1) 44.1kHz = "0, 0"
4	DETFS1 ⎭ 48kHz = "1, 0", 32kHz = "1, 1"

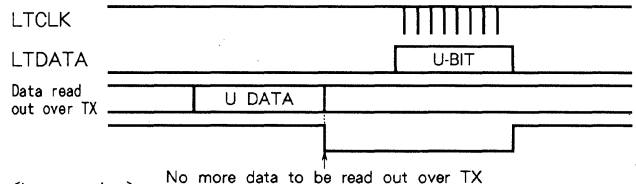
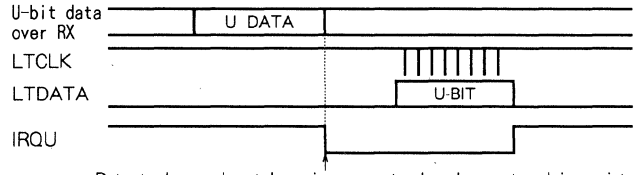
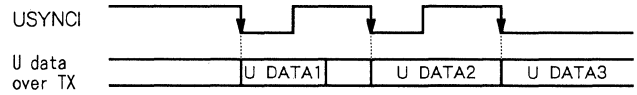
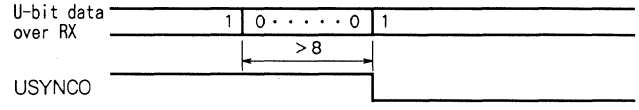
(Note 1) In microcomputer mode, functions listed below are determined by the polarity of both the dedicated pins and setting bits.

Name	Function	Polarity of dedicated pins		Polarity of setting bits	
ADSEL	Serial audio data source selection	ADSEL ⑱ pin	"0"	Bit 2	"1" = analog, "0" = digital
			"1"		"0" = analog, "1" = digital
MUTE	Mute control	MUTE ㉚ pin	"0"	Bit 5	"1" = mute
			"1"		"0" = mute
RXSEL	RX input selection	RXSEL ⑥ pin	"0"	Bit 6	"1" = RX1, "0" = RX2
			"1"		"0" = RX1, "1" = RX2

PIN DESCRIPTION (Microcomputer mode, pins for LT bus)

Pin No.	Name	I/O	Function and timing
㉝	LTEN	I	Enable control signal for LTDATA  When LTEN = 0, the input to LTDATA is enabled while LTCLK is disabled This is used as a selection signal for parallel connection to another system via LT bus
㉞	LTCLK	I	Clock input for shift-in and shift-out of LTDATA Although 8 or 16 clock pulses are handled as a unit, it is permitted to stop at smaller clock pulses if performing mode change by LTCNT0 and LTCNT1 which resets LTCLK
㉟	LTDATA	I/O	Serial data input/output  In data input state, data is taken into the IC at the positive-going edge of LTCLK. In data output state, the first bit is delayed by approximately 100ns at the maximum from the negative-going edge of LTCLK. The second and later bits are shifted out at the negative-going edge of LTCLK Whether to input or output data depends on the mode determined by LTCNT0 and LTCNT1 and on whether the action is to transmit or receive
㊱ ㊲	LTCNT1 LTCNT0	I I	Control signal specifying the data content of LTDATA  Settings : Sets the internal conditions of the IC (transmit/receive, etc.) Status : Monitors the internal conditions of the IC (unlock, etc.) Internal counters and the like are reset at either edge of both signals
㊵	SETSY	I	Latch clock input for settings information sent by LTDATA 

PIN DISCRIPTIONS (Continue)

Pin No.	Name	I/O	Function and timing
㊶	IRQU	O	Output signal specifying the state of the internal register that is the buffer for inputting and outputting U-bit data 〔In transmission〕  〔In reception〕 
㊷	USYNCI	I	Control signal specifying during transmission the timing to read out over TX U data consisting of units of 8 bits and stored in the internal register  Two kinds of timing are available to choose from by means of NOWD in settings data If NOWD = 0, timing is at the negative or positive-going edge of USYNCI with no time delay If NOWD = 1, U-bit data is transmitted at the position 4 fs words after each negative-going edge of USYNCI
㊸	USYNCO	O	Signal output indicating during reception word sink, namely, 9 bits or more consecutive "0"s in U-bit data in received RX signal  Two kinds of timing are available to choose from by means of NOWD as is in the case of USYNCI If NOWD = 0, USYNCO is inverted each time word sink occurs without delay If NOWD = 1, USYNCO is set to "0" after a time delay of 4 fs words from word sink, then set to "1" 2 fs words thereafter
㊹	IMSTRT	O	This signal during reception also indicates word sink similarly to USYNCO. It is output in synchronization with the reading out from LTDATA of 8-bit data preceding word sink During transmission, it is an output signal indicating an occurrence of 9-bits or more consective "0"s in U-bit data read out over TX

• The timing of settings data

Eight-bit settings data inputted through LTDATA is latched by the internal register at the negative-going edge of SETSY and establishes IC operating conditions.

• The timing of status data

Internal operating conditions (PLL lock, etc.) are loaded into the shift register at the negative-going edge of the first bit of LTCLK. They are shifted out bit by bit at the following negative-going edges.

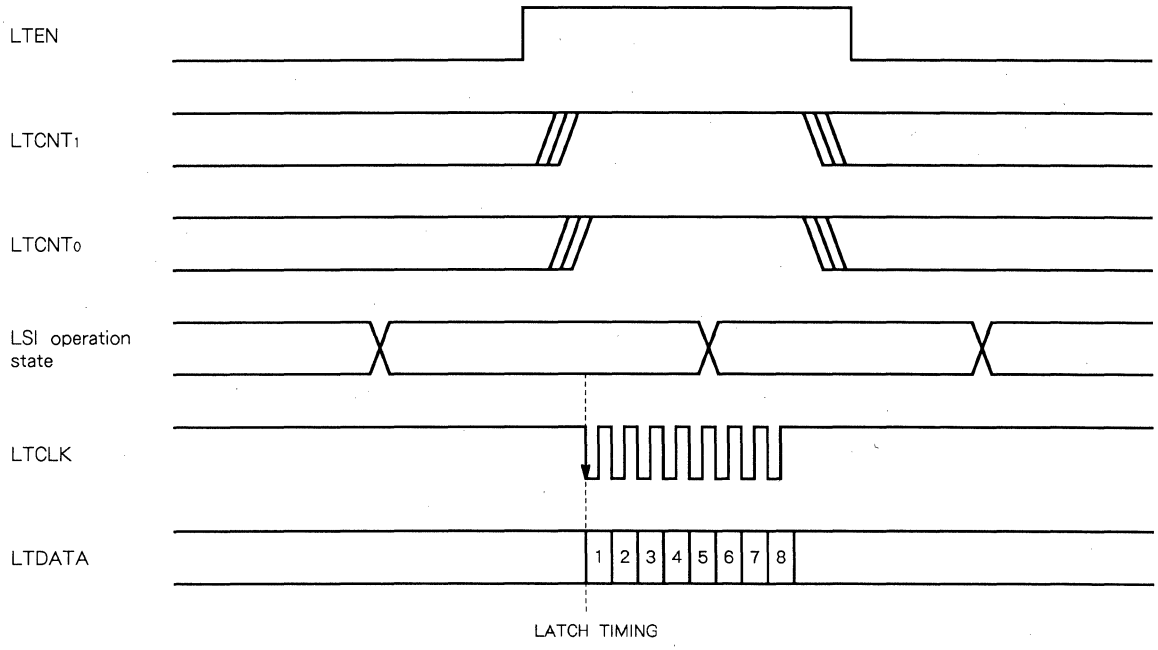
• The timing of C bit

Channel status can be inputted to and output from a block (192 frames) in units of 16 bit. In order for C bit during transmission to be sent over TX in such a manner that another data set is contained in another block, 16 bit of C-bit data entering the IC will be sent over TX at the beginning (the position of preamble "B") of the next block. Regarding 16 bit of data inputted as LTDATA, they will move to other latches within approximately 500ns after the 16th bit has entered, so that the next 16 bit of data can be successively inputted to the IC.

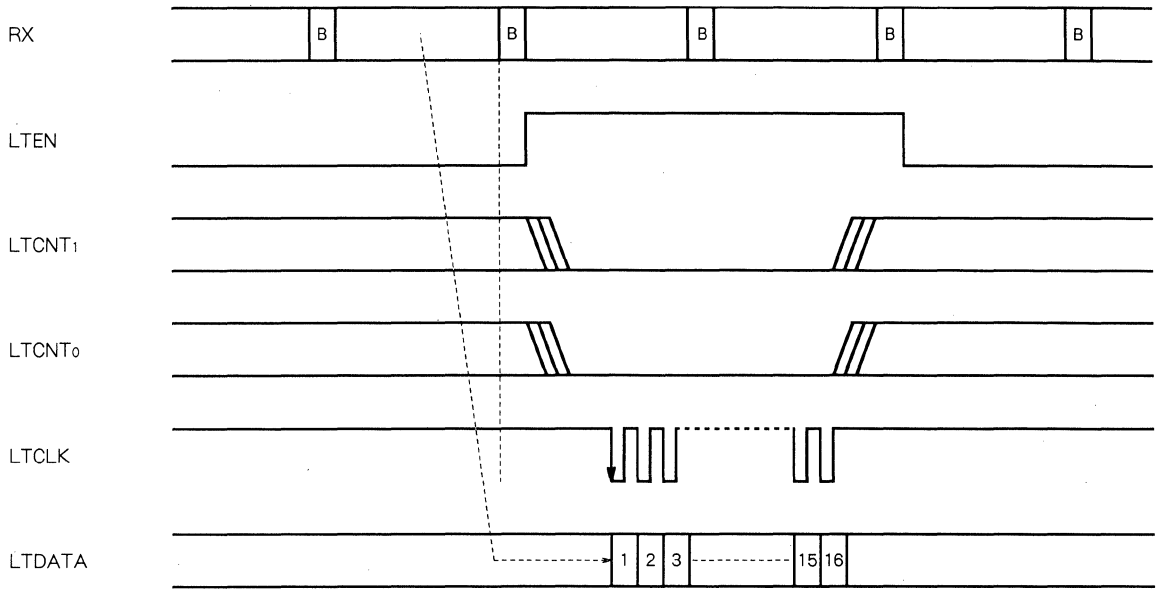
The 16 C bit contained in the previous block and held in internal latches during reception are loaded to the shift register in parallel form at the negative-going edge the first bit of LTCLK. They will be shifted out at the next negative-going edge of LTCLK.

3. DATA READ OUT TIMING (DAI → MICROCOMPUTER)

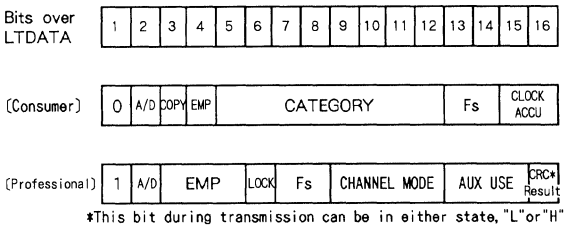
(1) Status



(2) C-bit data (reception mode)



Contents of C-bit data



(3) U-bit data (reception mode)

1) The general form of U-bit data

The general form is suitable for the U-bit data of CD and DAT. In that form as shown in Fig. 1 one unit of U-bit data consists of 8 bits, namely, a sink bit (= 1) at the beginning plus following 7 information bits.

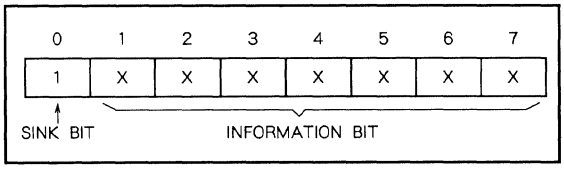


Fig. 1 U-bit data unit structure

Any number of "0"s can be inserted between units during transmission as shown in Fig. 2 If 9 or more "0"s are inserted in succession, the following unit is the start of a message. In other words, more than one units constitute a message and 9 or more "0"s separate messages.

The M51581FP in microcomputer mode is designed to interface in accordance as a rule with the general form of U-bit data.

At the reception block in particular, data is processed unit by unit assuming that U-bit data in received signals is conforming to the general form.

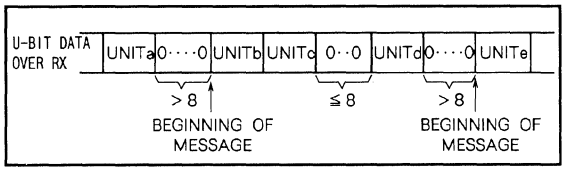


Fig. 2 The general transmission form of U-bit data

2) The structure of the U-bit data registers

The U-bit data registers are 4 pieces of byte registers (8 bits), an outline of which is shown in Fig. 3 Each register has independent addresses for writing and reading data. Data is written according to LTCLK given by a microcomputer. When 8 bits of data are written, the writing address increases by one. On the other hand, data is read based on MSTCK. In reading, one bit is allocated to a subframe in U-bit data sent over TX. When one byte of data is read, the reading address increases by one. The 4 registers are used cyclically as they are counted up.

The timing to read the first bit stored in a register is decided by the USYNCI signal.

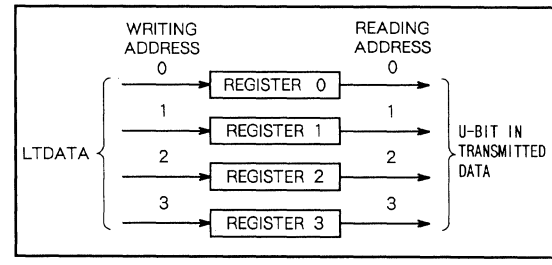


Fig. 3 The structure of U-bit data registers

3) U-Bit data timing during reception

The byte registers during reception are configured in the same way as transmission. Data is written and read based on MSTCK and LTCLK, respectively.

Received U-bit data is stored in the byte registers by information units. IRQU becomes "1" if read/write addresses coincide. This means, if IRQU is "0" new data received is written and is readable by microcomputer.

IMSTRT is "1" during the time between the start of reading the beginning unit of a message and the start of reading the next information unit. Consequently, a microcomputer during reception monitors IMSTRT, or USYNCO, which is explained later, to recognize the beginning of a message and also monitors IRQU to obtain U-bit data through LTDATA by LTCLK.

4) The Timing of USYNCI, USYNCO

As each subframe contains one U-bit, there is a U-bit in every 1/2 period of the LRCK signal. In applications of the IC to R-DAT especially, transmission should be managed so that audio sampling position during one drum turn coincides a U-bit. Since the U-bit read out position is based on USYNCI as explained above, inputting the drum revolution reference signal from the signal processing IC to USYNCI satisfies the requirements for R-DAT.

However, the frequency of the reference signal and the relationship between the positions of the reference signal and audio sampling are not uniform. For this reason, the M51581FP has two modes, which can be selected by NOWD in settings data. The two modes are defined as follows.

〔**In transmission**〕

NOWD = 0

- U-bit are read at both edges of USYNCI
- Reading U-bit starts 1/2 LRCK after an edge of USYNCI

NOWD = 1

- U-bit are read at the negative-going edges of USYNCI
- Reading U-bit starts 9/2 LRCK after a negative-going edge of USYNCI

〔**In reception**〕

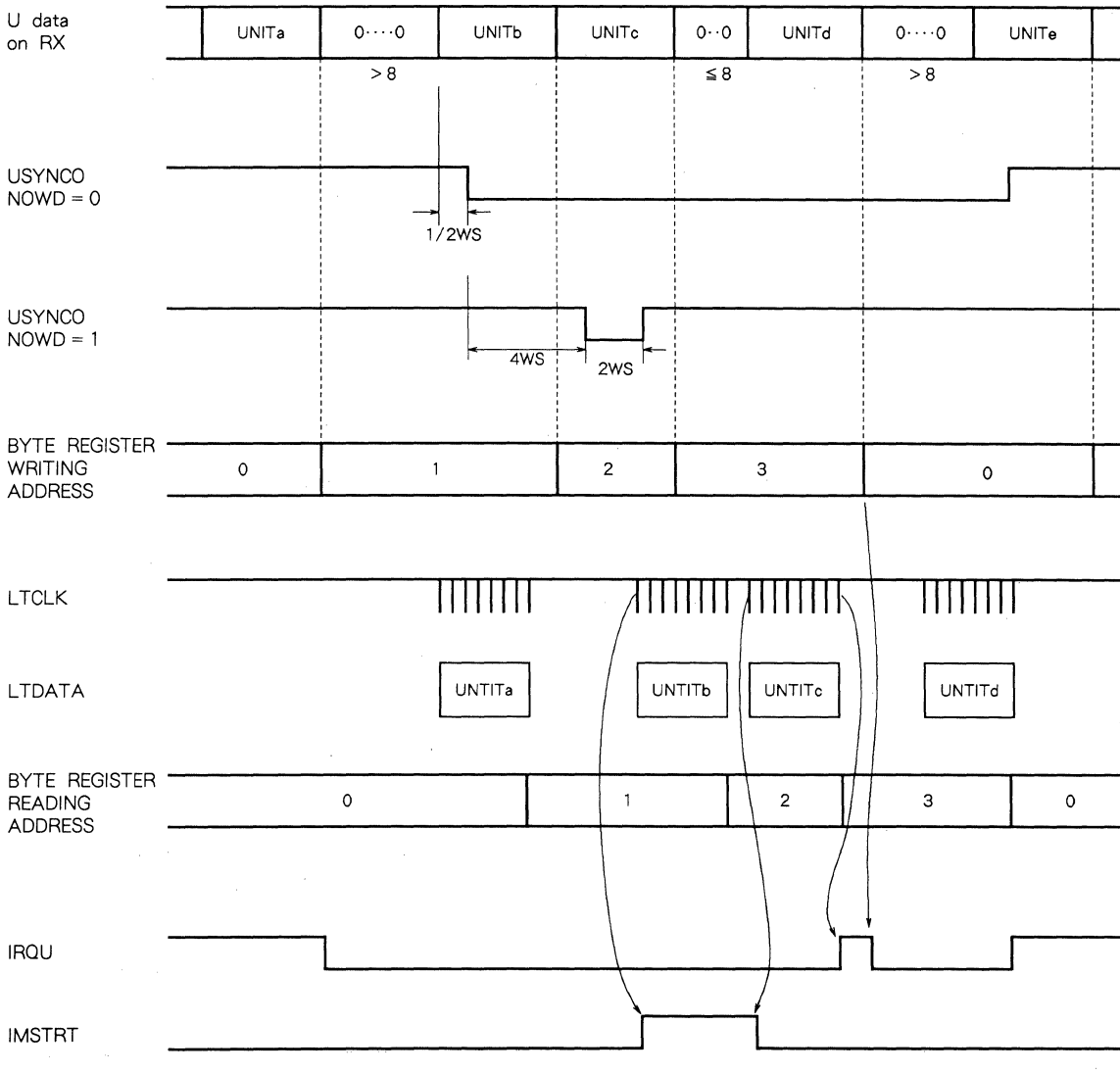
NOWD = 0

- The USYNCO signal is inverted at the beginning of each message
- USYNCO changes at an edge of LRCK following the sink bit of the beginning of a message

NOWD = 1

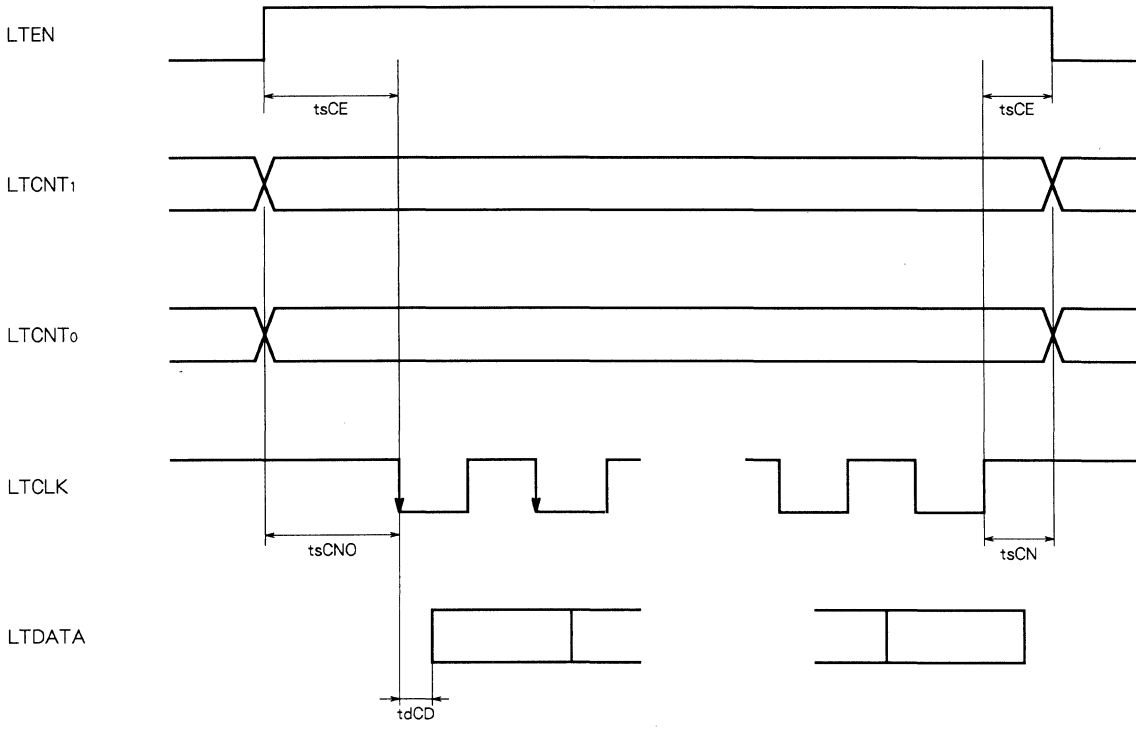
- USYNCO falls at an edge 4 LRCK after the sink bit of the beginning of a message
- USYNCO stays at "0" for a period of 2 LRCK

(4) U-bit data read out timing



(5) Timing limits for reading status, C-bit data, and U-bit data

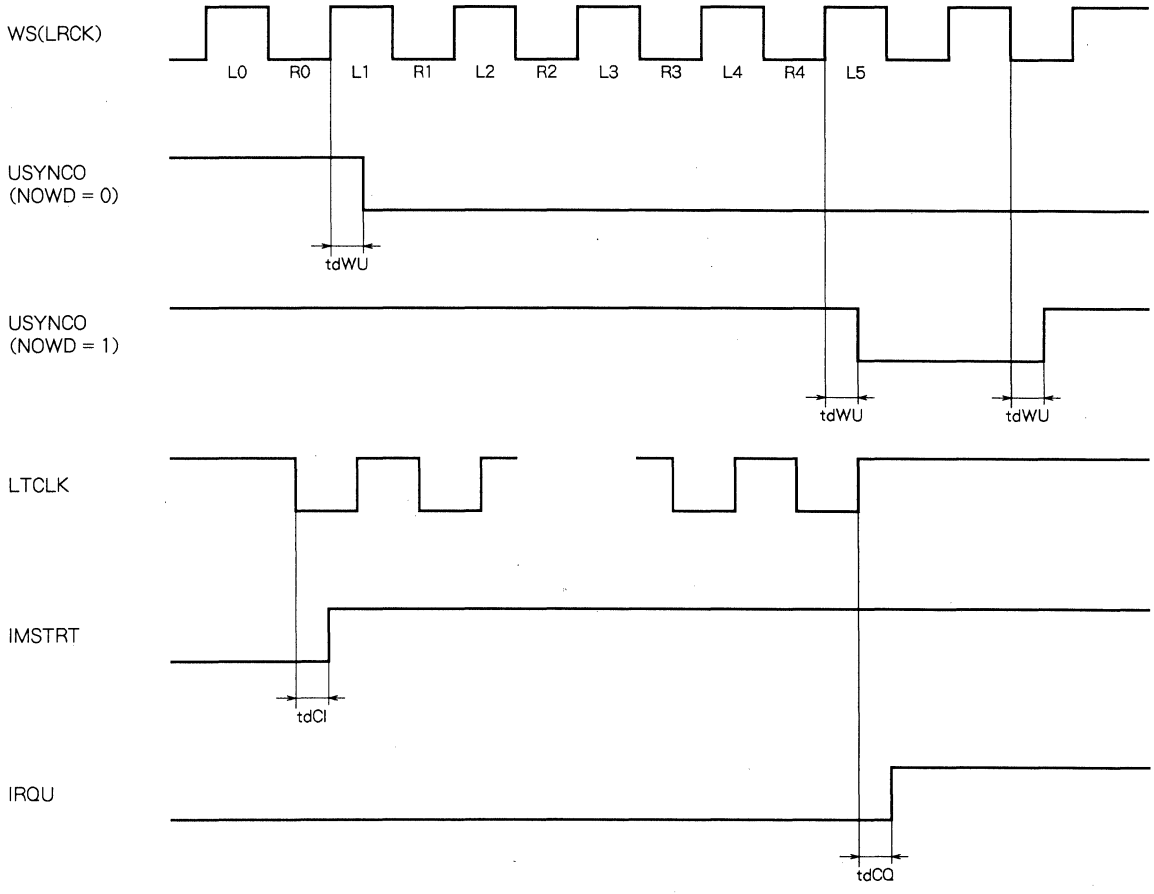
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
tsCEO	Data output LTCLK-LTEN setup time	1000			nsec
tsCE	LTCLK-LTEN setup time	50			nsec
tsCNO	Data output LTCLK-LTCNT setup time	1000			nsec
tsCN	LTCLK-LTCNT setup time	50			nsec
tdCD	LTCLK-LTDATA delay time			250	nsec



Note : As internal registers for data output are set at edges of the LTEN, LTCNT0, and LTCNT1 signals, at least one of these signals must be inverted in advance to read out status, C-bit data, and U-bit data.

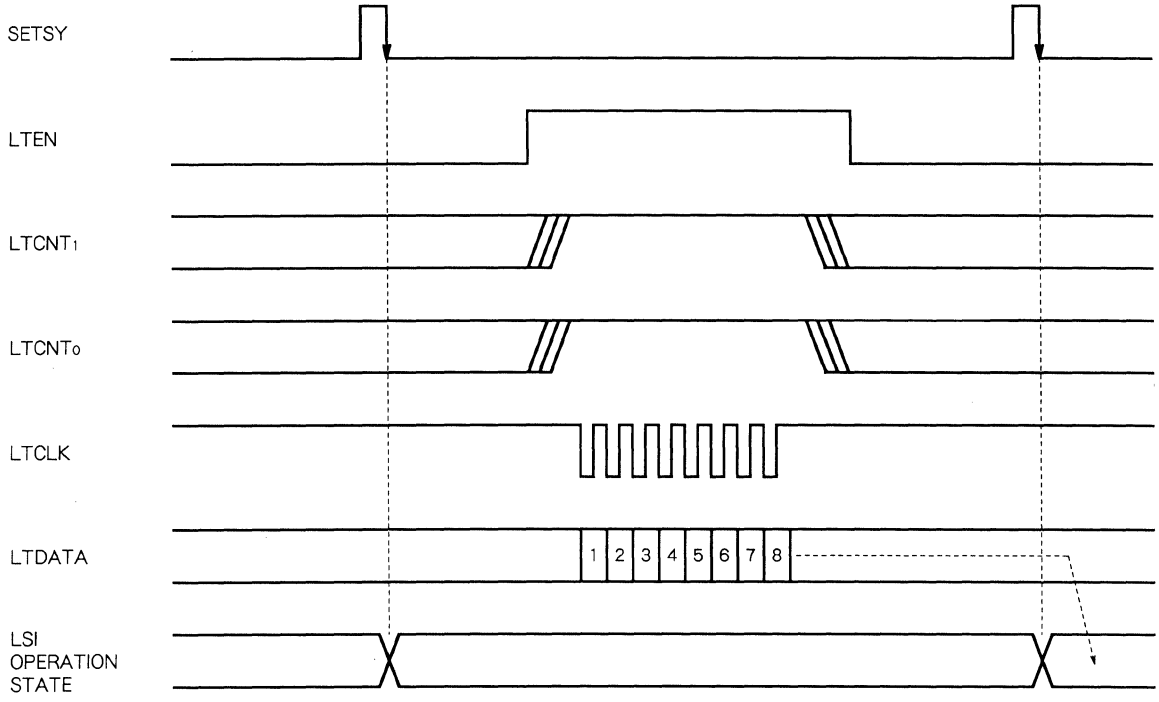
(6) Timing limits of usynco, IRQU, and IMSTRT

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
tdWU	WS-USYNCO delay time			200	nsec
tdCI	LTCLK-IMSTRT delay time			150	nsec
tdCQ	LTCLK-IRQU delay time			150	nsec

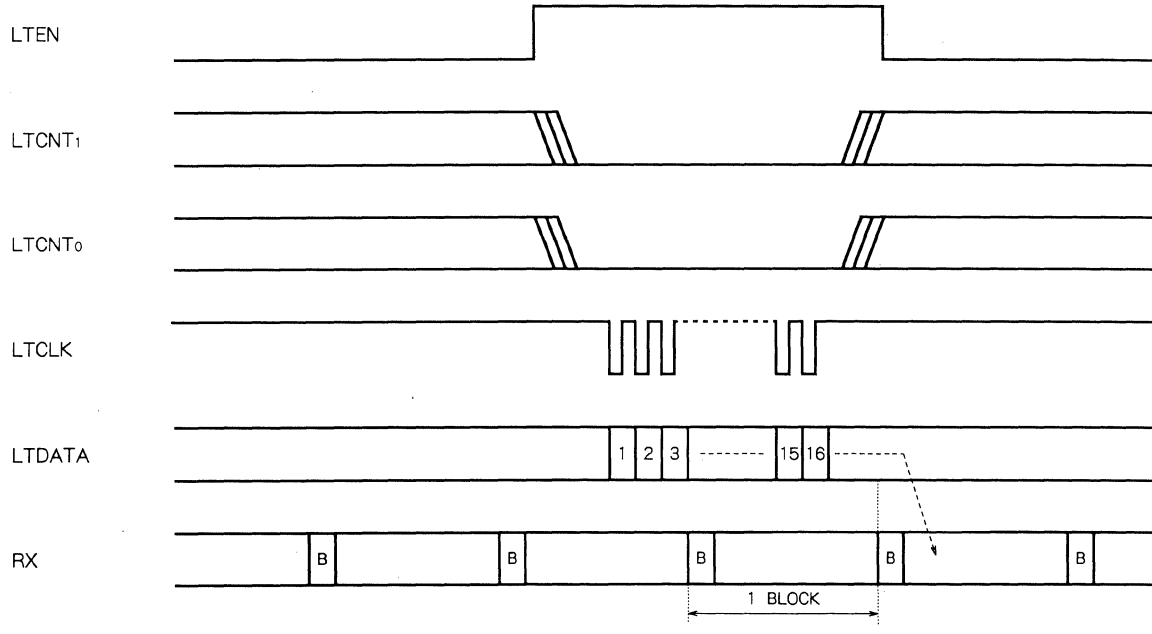


4. DATA WRITING TIMING (MICROCOMPUTER → DAI)

(1) Setting



(2) C-bit data (transmission mode)



(3) U-bit data (transmission mode)

Reading and writing the U-bit data registers are carried out in asynchronization with each other so that IRQU is used as a signal to recognize the state of the two addresses. If both addresses match, IRQU becomes "0". Since there is no more data to be transmitted (read) at this point, priority is given to writing, as a rule.

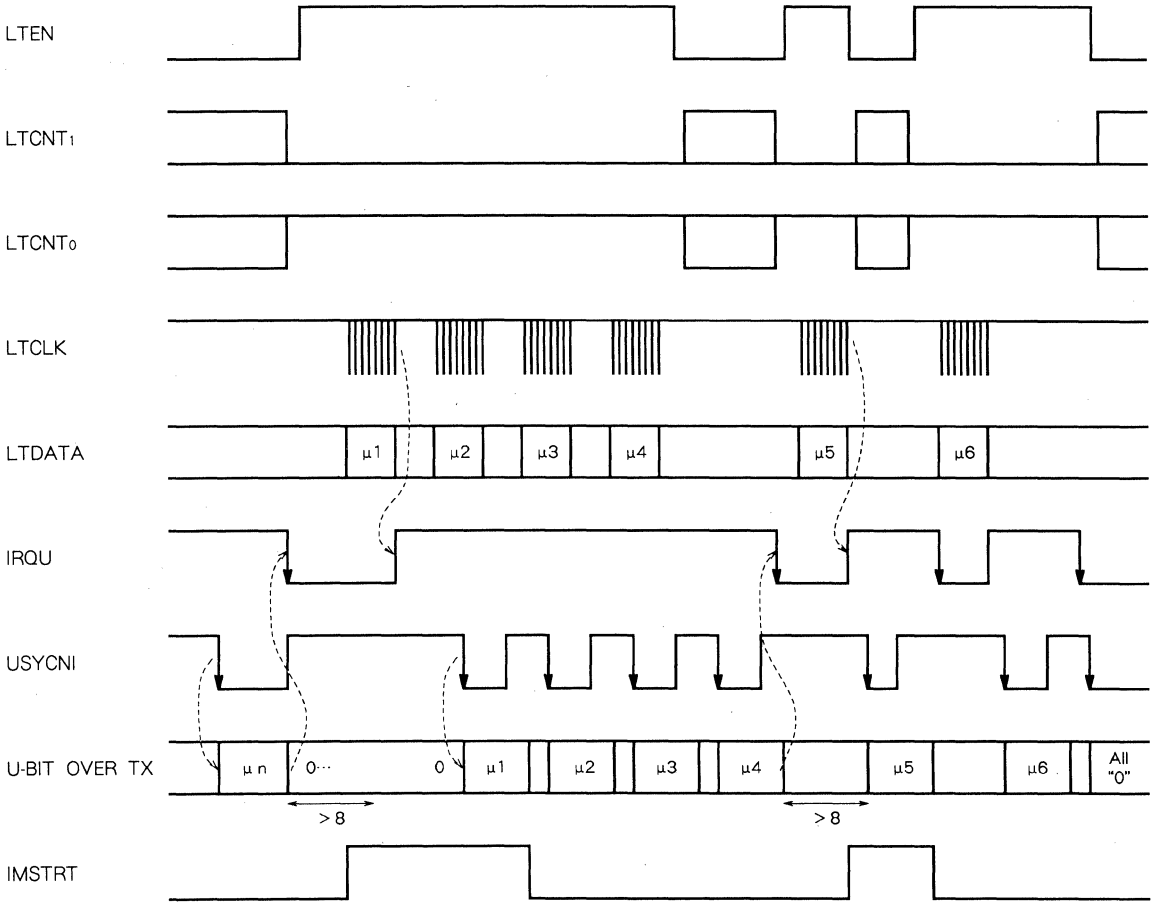
If IRQU = 0 and USYNCI falls (when NOWD = 1), transmission data will be all "0".

IMSTRT is a signal that if 9 or more continuous "0"s are found in U-bit data transmitted over TX stays at "1" until the end of reading the next 1 byte data.

As data is read based on USYNCI, a gap over 9-bit or more in USYNCI lets "0"s be transmitted as data on and after the 9th bit.

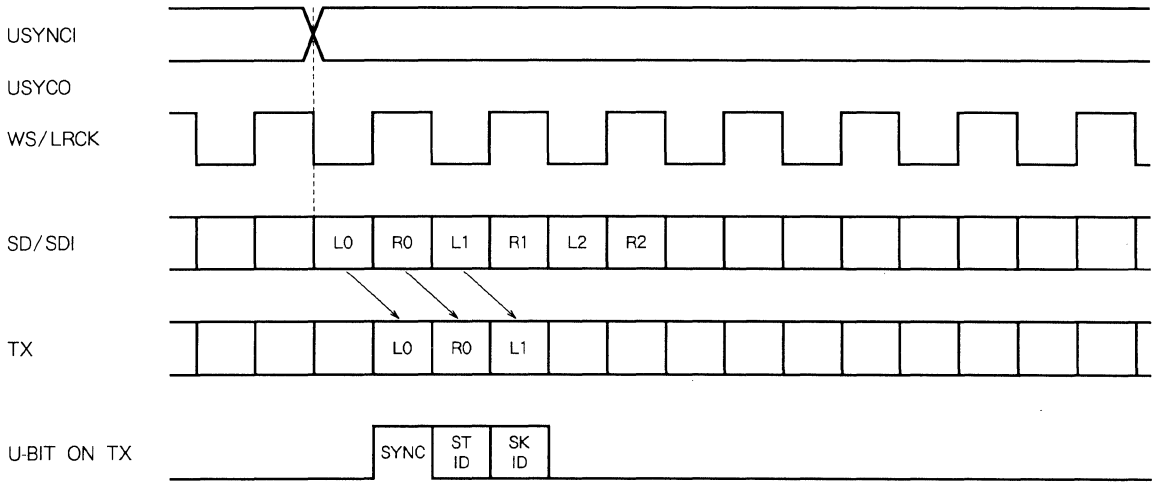
As explained above, the microcomputer, while monitoring IRQU, sends U-bit data to LTDATA by LTCLK. Furthermore, it can send U-bit at any desired positions by controlling USYNCI.

The M51581FP has 4 bytes of internal registers, so it is also possible to input 4 bytes of U-bit consecutively and then transmit them other TX by controlling USYNCI.

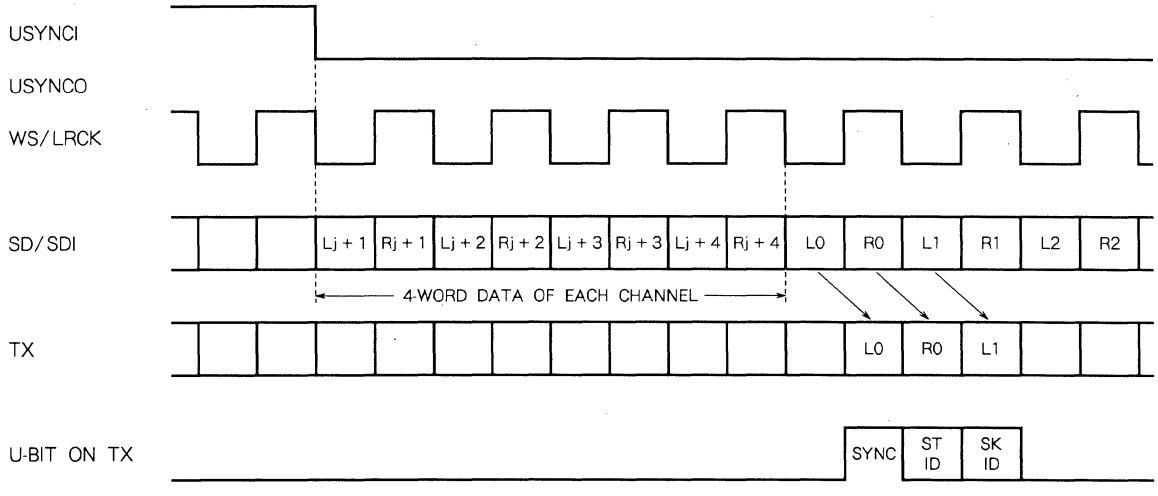


(4) The timing of USYNCI

(a) NOWD = 0

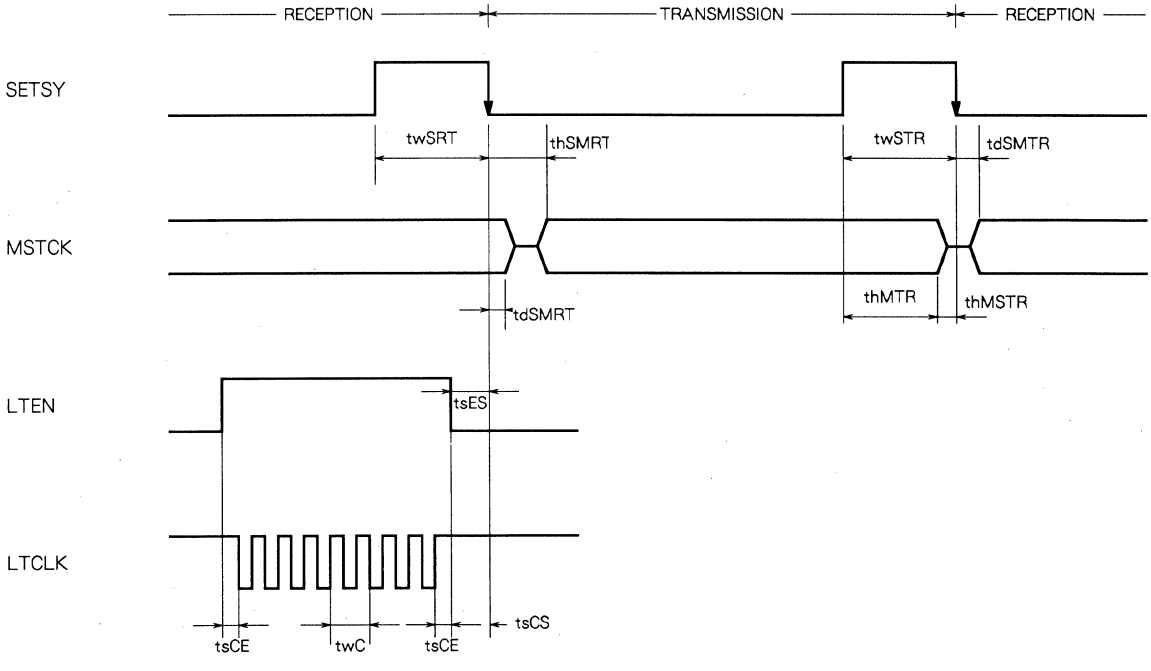


(b) NOWD = 1



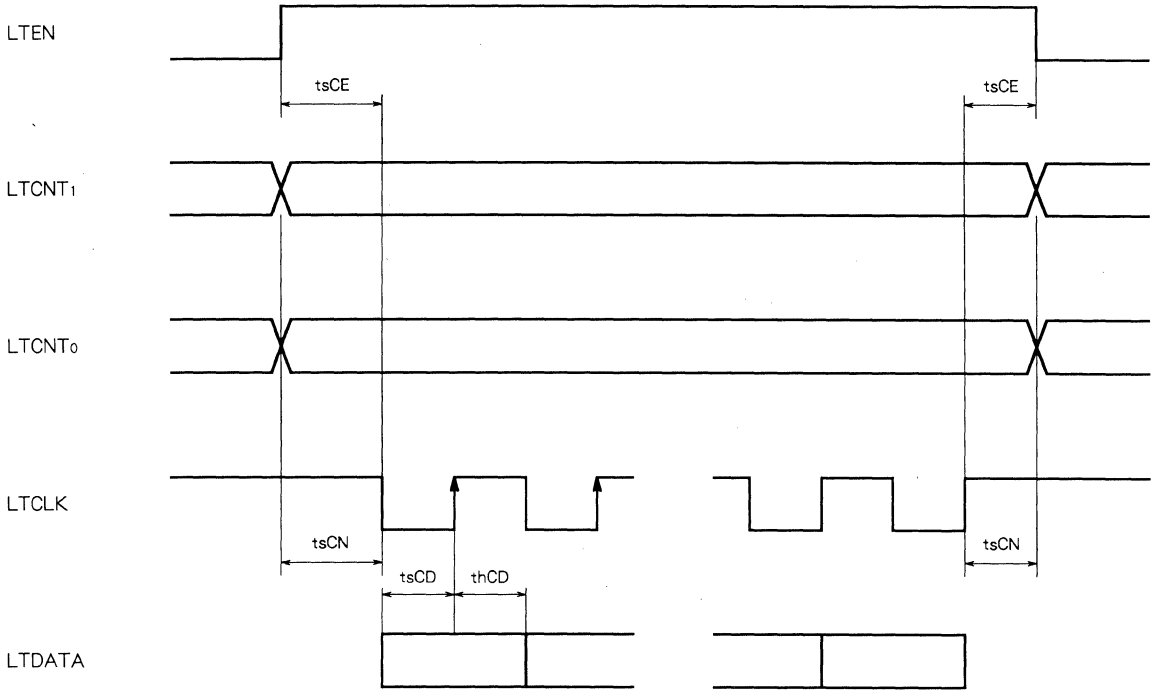
(5) Setting timing limits

Symbol	Parameter	Limits (Unit : sec)			Remark
		Min	Typ	Max	
twSRT	SETSY pulse width at change from R to T	4μ	–	–	Value with an allowance considering the requirement of 4 clock pulses of MSTCK(128fs) in SETCY pulses and a failure of low VCO oscillation frequency
twSTR	SETSY pulse width at change from T to R	1μ	–	–	4 clock pulses under condition of fs = 32kHz assuming that MSTCK is stably supplied during transmission
thMTR	MSTCK hold time at change from T to R	1μ	–	–	4 clock pulses or more of MSTCK (128fs) in SETSY pulses meet the requirement
tdSMRT	SETS – MSTCK delay time at change from R to T	5n	30n	100n	Period taken by the MSTCK pin to shift from output mode to input mode (HI-z)
thMSTR	MSTCK – SETSY hold time at change from T to R	0n	–	–	Value with allowance to avoid interference between MSTCK outputs
thSMRT	SETSY – MSTCK hold time at change from R to T	100n	–	–	
tdSMTR	SETSY – MSTCK delay time at change from T to R	5n	30n	100n	Period taken by the MSTCK pin to shift from input mode (HI-z) to output mode
tsES	LTEN–SETSY setup time	–	–	–	No specification LTEN may be at "H" when SETSY falls
twC	LTCLK clock period	250n	–	–	
tsCE	LTCLK–LTEN setup time	50n	–	–	
tsCS	LTCLK–SETSY setup time	50n	–	–	



(6) Timing limits for writing settings, C-bit data, and U-bit data

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
tsCE	LTCLK–LTEN setup time	50			nsec
tcCN	LTCLK–LTCNT setup time	50			nsec
tsCD	LTCLK–LTDATA setup time	50			nsec
thCD	LTCLK–LTDATA hold time	50			nsec

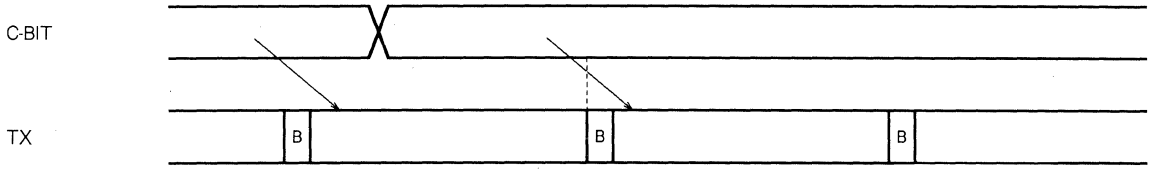


Note : As internal registers for data input are set at edges of the LTCNT0 and LTCNT1 signals, at least one of these signals must be inverted in advance to write settings, C-bit data, and U-bit data.

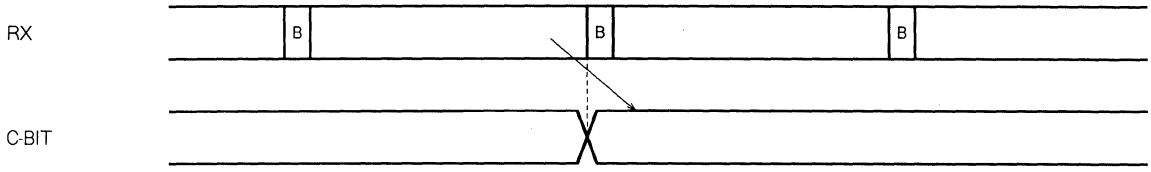
5. C-BIT DATA TIMING (EASY MODE)

(1) C-bit data

(a) In transmission

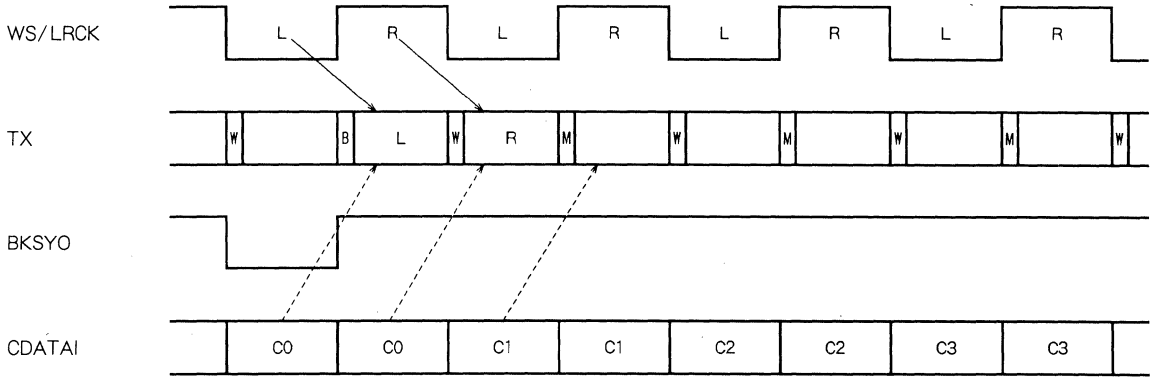


(b) In reception

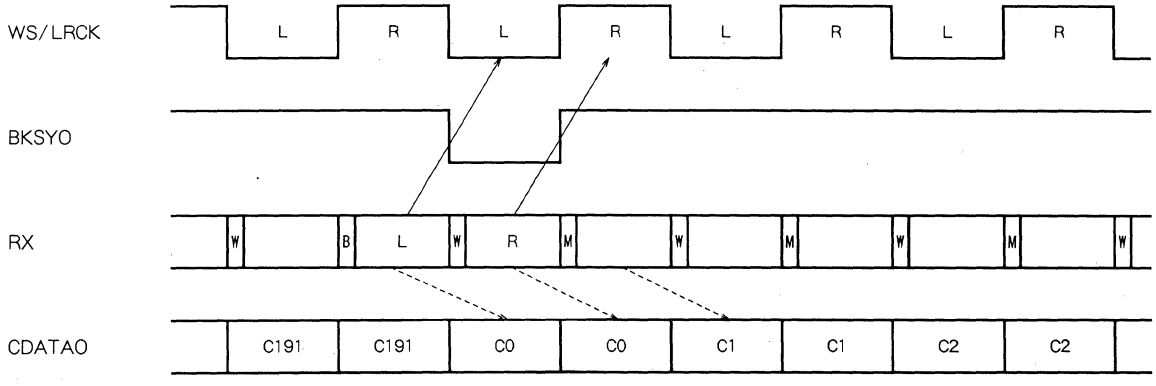


6. C-BIT DATA TIMING (FULL-TRANSPARENT MODE)

(a) In transmission

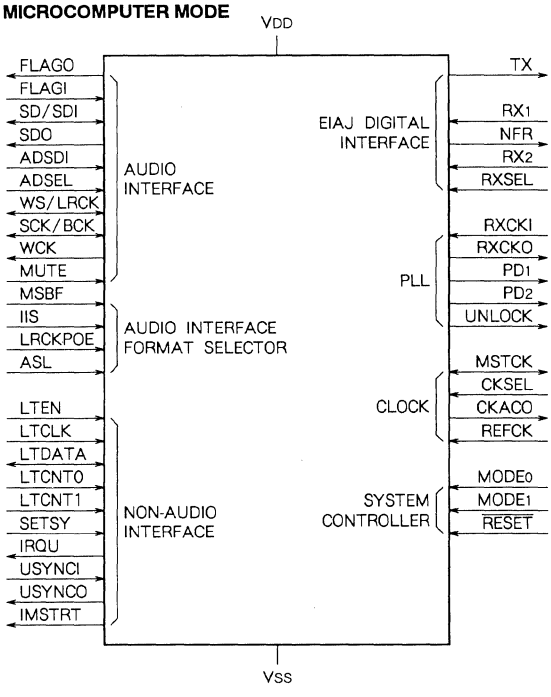


(b) In reception

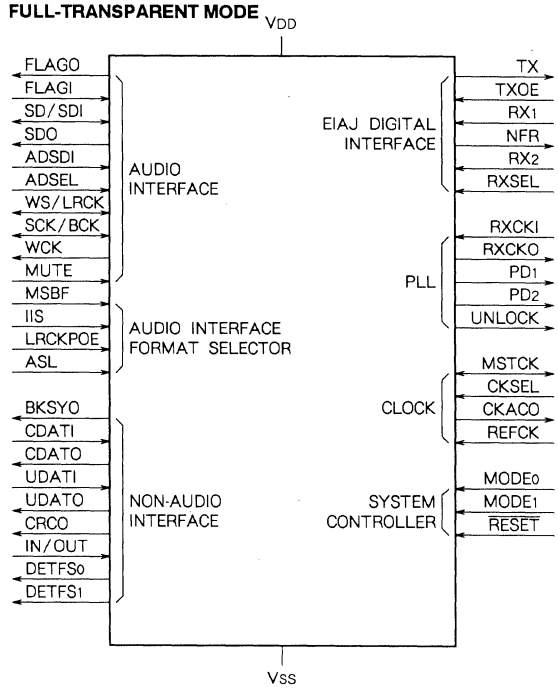


7. INPUT/OUTPUT PIN FORMAT

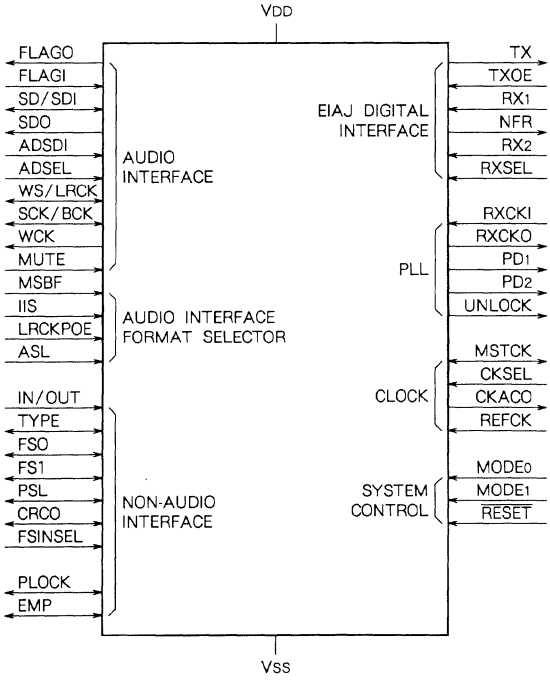
MICROCOMPUTER MODE



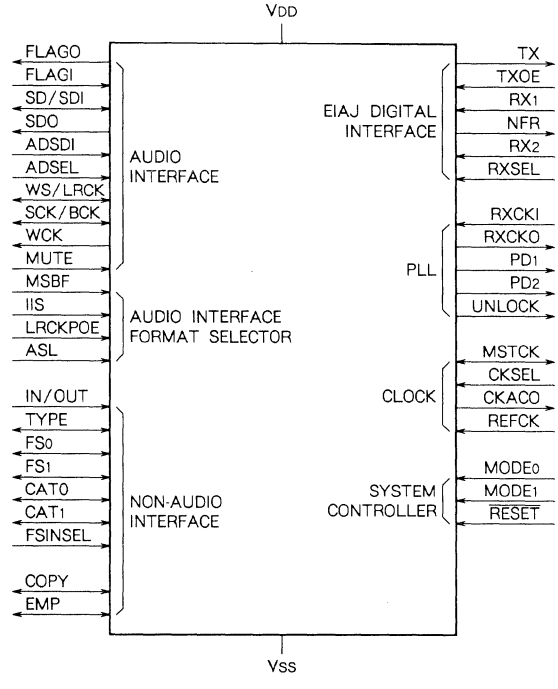
FULL-TRANSPARENT MODE



EASY MODE:PROFESSIONAL

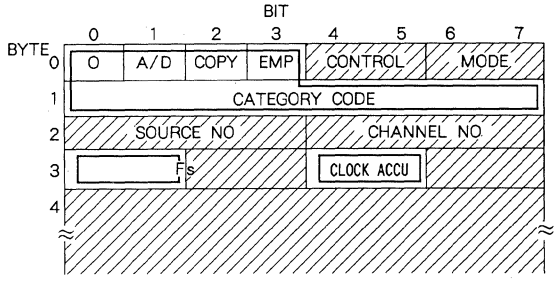


EASY MODE:CONSUMER

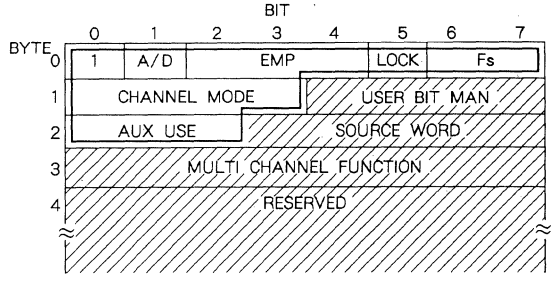


8. C-BIT DATA SUPPORT BIT MAP

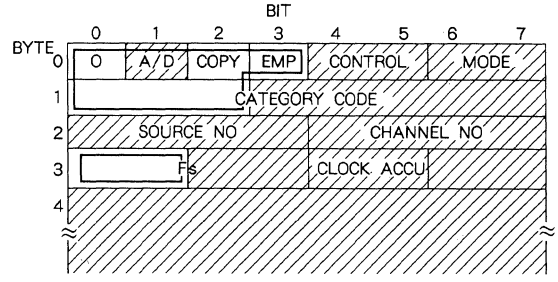
(1) Microcomputer (MODE00), Consumer



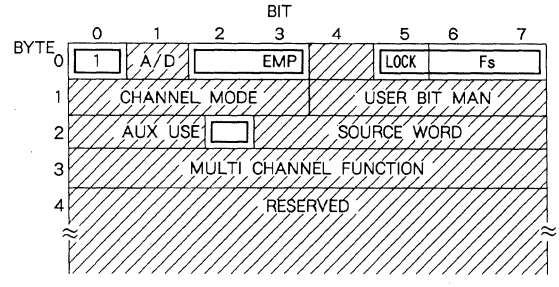
(2) Microcomputer (MODE00), Professional



(3) Easy mode (MODE01), Consumer

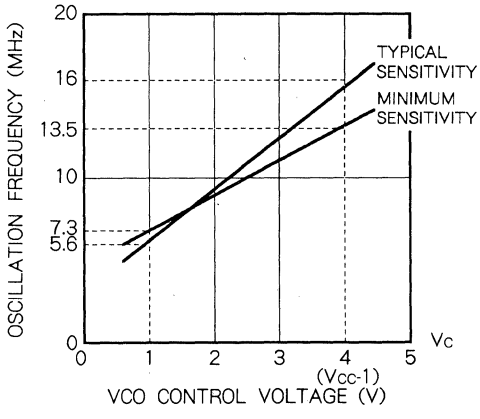


(4) Easy mode (MODE01), Professional

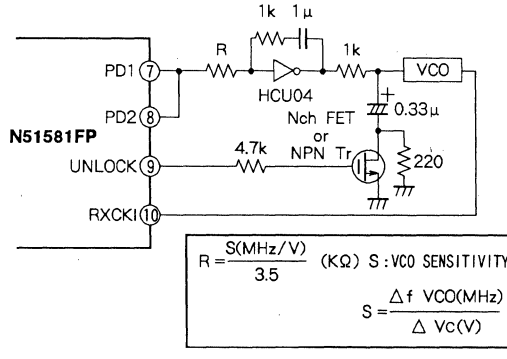


SUPPORT BIT All "0"

9. PLL APPLICATIONS



VCO Sensitivity Characteristics : Received fs = 32~48kHz

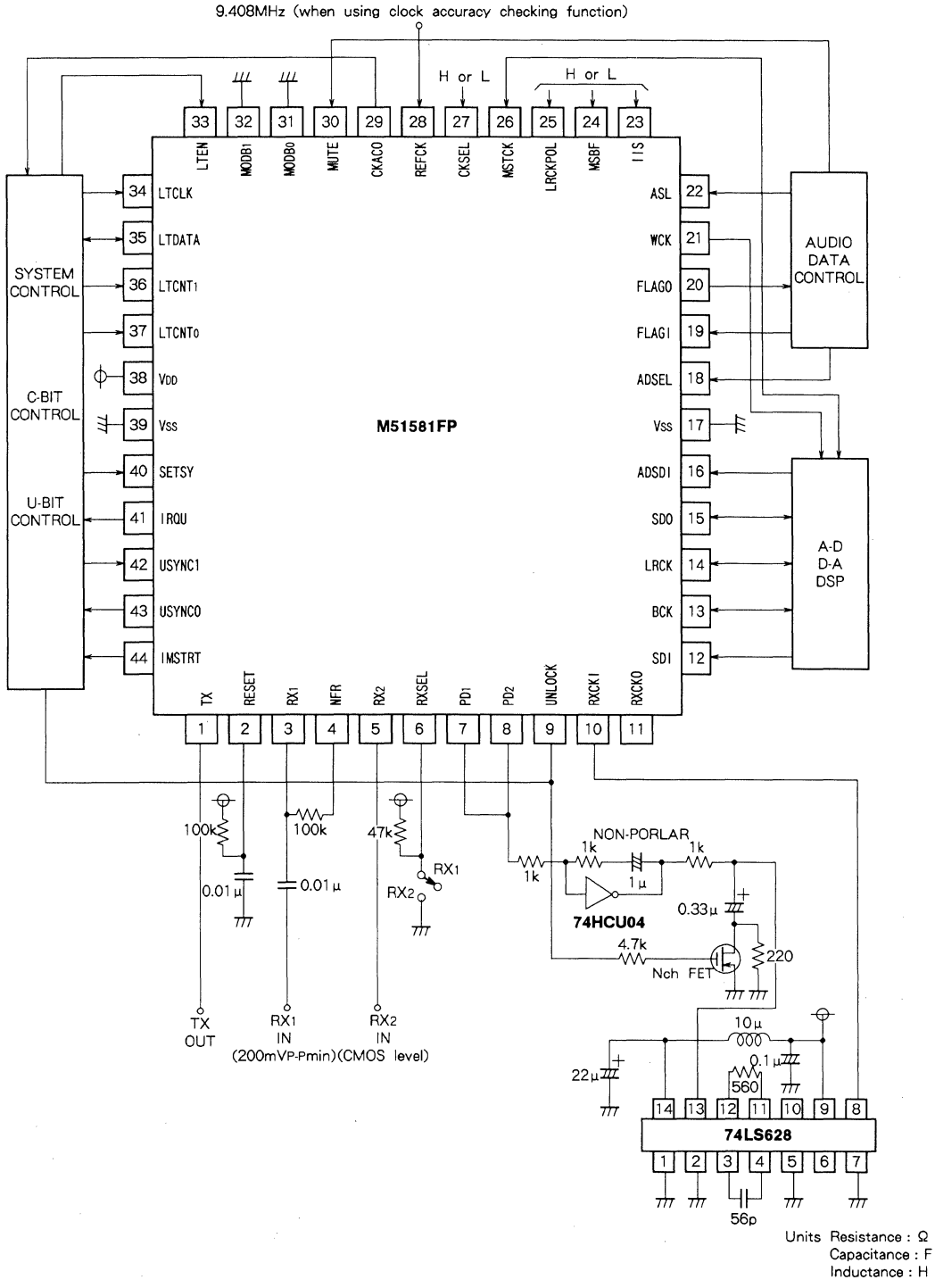


If VCO sensitivity is typical :

$S = \frac{16 - 5.6}{4 - 1} = 3.5(MHz/V)$ So $R = 1k\Omega$

PLL APPLICATION EXAMPLE

10. APPLICATION EXAMPLE (MICROCOMPUTER MODE)



M65810FP

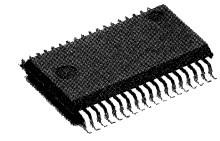
DIGITAL AUDIO INTERFACE RECEIVER

DESCRIPTION

The M65810FP is a semiconductor IC for receiving and decoding digital audio data conforming to the EIAJ (CP-340) standards, transmitted from digital audio equipment such as CD, DAT, DCC, and MD players and BS tuner. It has substantial functions such as built-in input selectors for 6 channels and PLL containing VCO. Furthermore, the IC can read information allotted to serial copy management systems.

FEATURES

- A total of 6 channels of selectable inputs : 3 channels of optical inputs (CMOS level) and 3 channels of coaxial cable inputs (with a built-in converter to change minimum of 400mV$_{PP}$ into CMOS level) (Selected input is output at the feedthrough pin)
- Two kinds of control modes, microcomputer mode using serial data and easy mode using parallel data, are available to choose from as input selection
- Built-in PLL circuit containing VCO
- Selection of master clock from 384fs and 256fs
  Equipped also with dedicated 128fs output pin
- If an error occurs on parity check, the preceding value in audio data is held to prevent noise
- If PLL is unlocked, digital audio data is set to "all 0"to mute
- U and V bits are output at dedicated pins (in micro computer mode)
- Word clock output pin gives capability of dealing with diverse kinds of DA converter ICs



Outline 36P2R-A

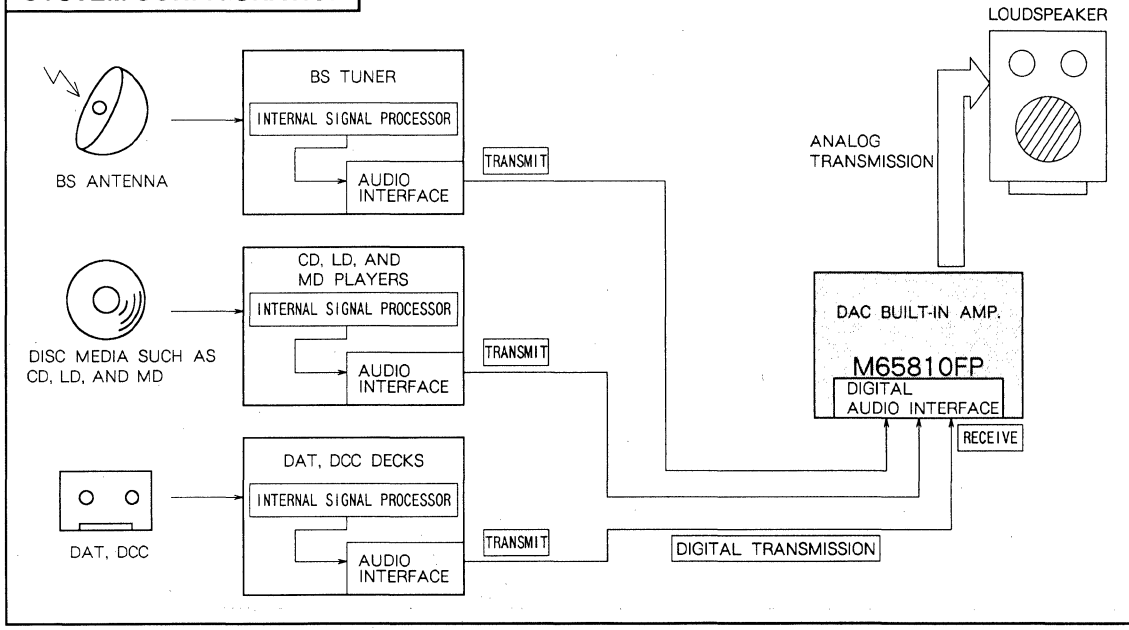
0.8mm pitch 450mil SSOP
(8.4mm × 15.0mm × 2.0mm)

- Outputs C-bit fs information and emphasis information at dedicated pins. The first 32 bits in C-bit data can be read in serial data from in microcomputer mode

RECOMMENDED OPERATING CONDITIONS

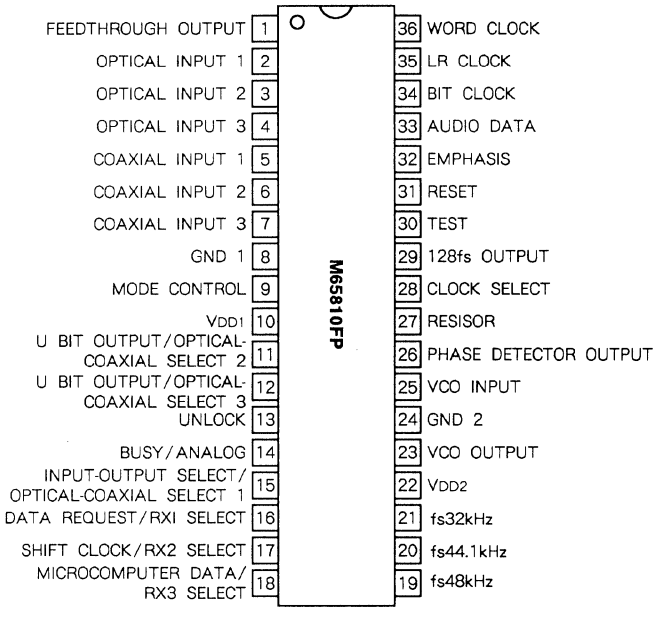
Supply voltage range ..... V_{DD} = 4.75~5.25V
Rated supply voltage ..... V_{DD} = 5V

SYSTEM CONFIGURATION



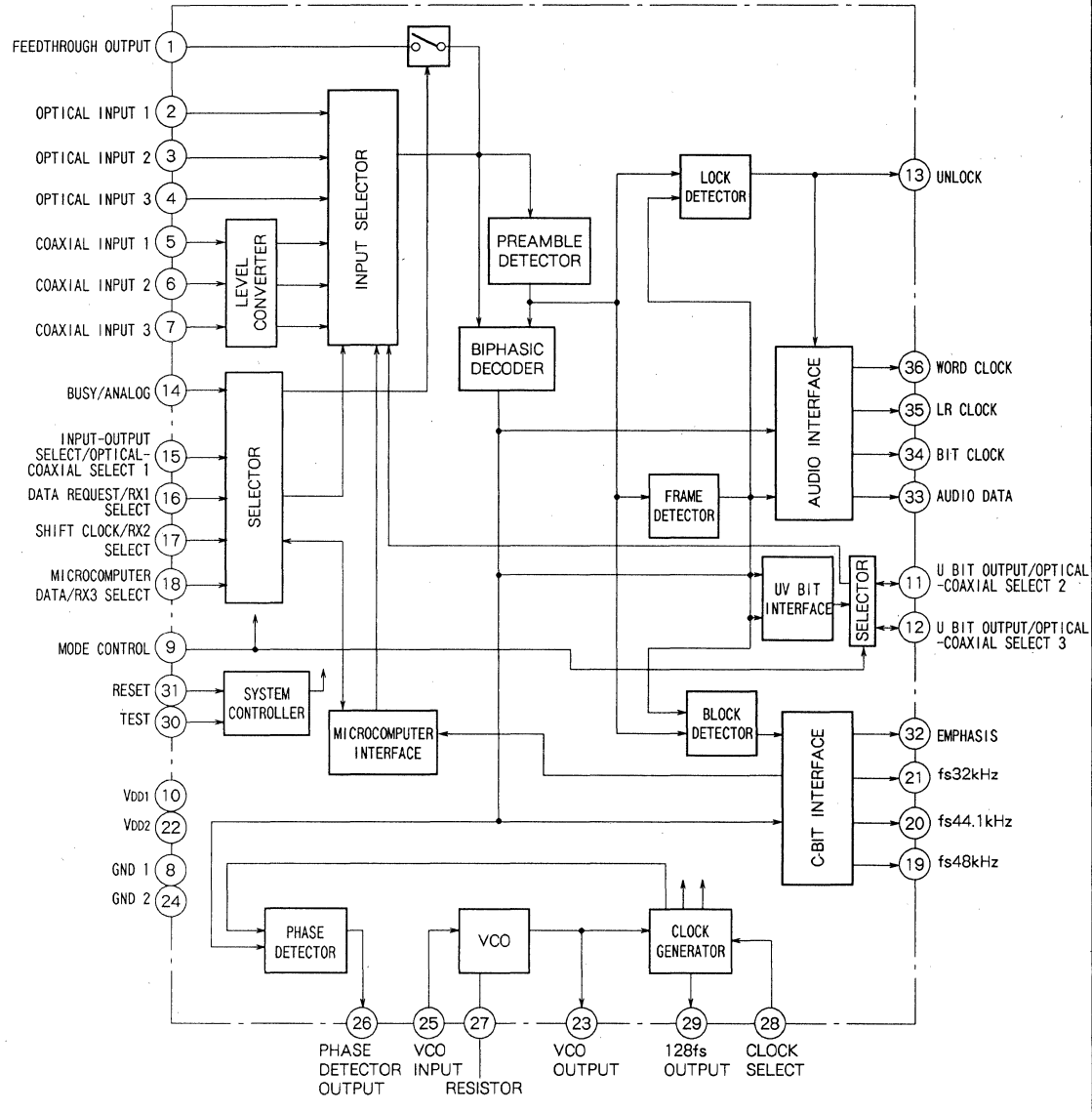
MITSUBISHI ELECTRIC

PIN CONFIGURATION



Outline 36P2R-A

IC INERNAL BLOCK DIAGRAM



PIN DESCRIPTION (I ↓ denotes input with pull-down resistor)

Pin No.	Symbol	Name	I/O	Usage
①	FTO	Feedthrough output	O	Through output of selected RX
②	ORX1	Optical input 1	I	CMOS level inputs
③	ORX2	Optical input 2	I	
④	ORX3	Optical input 3	I	
⑤	CRX1	Coaxial input 1	I	Inputs to internal level converter Minimum input voltage 400mV$_{P-P}$
⑥	CRX2	Coaxial input 2	I	
⑦	CRX3	Coaxial input 3	I	
⑧	VSS1	GND 1	–	
⑨	MODE	Mode control	I	H = microcomputer mode, L = easy mode
⑩	V_{DD1}	V_{DD1}	–	
⑪	UBO/ OCSEL2	U bit output/optical-coaxial select 2	O I	In microcomputer mode:U-bit data output(in synchronization with LRCK) In easy mode : RX1 optical line/coaxial line input selector, H = optical line input
⑫	VBO/ OCSEL3	U bit output/optical-coaxial select 3	O I	In microcomputer mode:V-bit data output(in synchronization with LRCK) In easy mode : RX2 optical line/coaxial line input selector, H = optical line input
⑬	UNLOCK	Unlock	O	PLL unlock information : unlock = H
⑭	BUSY/ANALOG	Busy/analog	O I ↓ /O	In microcomputer mode:modification information about C-bit data contents, modefication=H In easy mode:RX inputs are all shout off on a H pulse and VCO also stops
⑮	IOSEL/OCSEL1	Input-output select/optical-coaxial select 1	I I	In microcomputer mode:data input/output selector, H=microcomputer→DAI, L=DAI→microcomputer In easy mode:RX3 optical line/coaxial line input selector, H=optical line input
⑯	REQ/ RX1SEL	Data request/RX1 select	I ↓ I ↓ /O	In microcomputer mode : data input/output enabled at H In easy mode : RX1 is selected on H pulse and H is held
⑰	SCK/ RX2SEL	Shift clock/RX2 select	I ↓ I ↓ /O	In microcomputer mode : data is shifted on a fall In easy mode : RX2 is selected on H pulse and H is held
⑱	MDATA/ RX3SEL	Microcomputer data/RX3 select	I ↓ /O I ↓ /O	In microcomputer mode : serial data input/output In easy mode : RX3 selected on H pulse and H is held
⑲	FS48	fs48kHz	O	Set by C-bit fs code : 48kHz = L (These are all set to H under unlock condition.)
⑳	FS44	fs44.1kHz	O	Set by C-bit fs code : 44.1kHz = L
㉑	FS32	fs32kHz	O	Set by C-bit fs code : 32kHz = L
㉒	V_{DD2}	V_{DD2}	–	Power supply to VCO
㉓	VCOO	VCO output	O	=384fs or 256fs(according to the polarity of pin ㉘)master clock output
㉔	VSS2	GND 2	–	Ground of VCO. Same voltage as VSS1.
㉕	VCOI	VCO input	I	VCO control voltage input
㉖	PDO	Phase detector output	O	Forms an external loop filter
㉗	R1	Resistor	–	Adusts free-running oscillation frequency by resistor for adjustment of VCO oscillation frequency
㉘	CKSEL	Clock select	I	Master clock frequency selector : H = 384fs, L = 256fs
㉙	128FS	128fs output	O	128fs clock output
㉚	TEST	Test	I	Test pin. Normally fixed to L, TEST = H
㉛	$\overline{\text{RESET}}$	Reset	I	Initialization at power up. RESET = L
㉜	EMP	Emphasis	O	Set by C-bit emphasis code : 50/15 μ sec = H
㉝	ADATA	Audio data	O	16-bit audio data serial output (MSB first)
㉞	BCK	Bit clock	O	Audio data shift clock = 64fs
㉟	LRCK	LR clock	O	= fs
㊱	WCK	Word clock	O	= 2fs (50% duty)

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DD}-V_{SS}	Suply voltage	− 0.3~6.5	V
V_{DD1}-V_{DD2}	Voltage difference between VDD 1 and 2.	± 0.3	V
V_I	Input voltage	V_{SS} − 0.3~V_{DD} + 0.3	V
P_d	Power dissipation	1100	mW
T_{opr}	Operating temerature	− 20~ + 70	℃
T_{stg}	Storage temperature	− 40~ + 125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Suplly voltage		4.75	−	5.25	V
V_{IH}	Input voltage (H level)		0.7V_{DD}	−	V_{DD}	V
V_{IL}	Input voltage (L level)		Vss	−	0.3V_{DD}	V
f_{VCO}	Oscillation frequency (VCO)	CKSEL = L	−	256fs	−	−
f_{VCO}	Oscillation frequency (VCO)	CKSEL = H	−	384fs	−	−
fs	Input signal sampling frequency		32	−	48	kHz

ELECTRICAL CHARACTERISTICS (DC CHARACTERISTICS)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{DD}	Circuit current	When receiving fs = 44.1kHz	−	20	−	mA
V_{OH}	Output voltage (H level)	I_{OH} = − 500 μA	V_{DD-1}	−	−	V
V_{OL}	Output voltage (L level)	I_{OL} = 500 μA	−	−	0.4	V
I_{IN}	Input leak current	V_I = V_{SS}~V_{DD}	−	−	± 1	μA
I_{OL}	Driver current	V_{OL} = 0.5V, pins ⑲⑳㉑	15	−	−	mA
I_{OH}	Driver current	V_{OH} = V_{DD} − 1.5V, pins ⑭⑮⑰⑱	15	−	−	mA
R_{ID}	Input pull-down resistance	Pins ⑭⑮⑰⑱	20	−	100	kΩ

FUNCTION DESCRIPTION

6 channel input selector

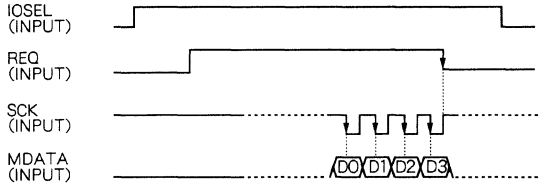
1. Easy mode (MODE=L)

Input		OCSEL 1	OCSEL 2	OCSEL 3	RX1SEL	RX2SEL	RX3SEL	ANALOG
Optical input	ORX1	H	–	–	⌐¬	–	–	–
	ORX2	–	H	–	–	⌐¬	–	–
	ORX3	–	–	H	–	–	⌐¬	–
Coaxial input	CRX1	L	–	–	⌐¬	–	–	–
	CRX2	–	L	–	–	⌐¬	–	–
	CRX3	–	–	L	–	–	⌐¬	–
Analog mode		–	–	–	–	–	–	⌐¬

- RX inputs are selected at the positive-going edge of a H pulse inputted to the RX1SEL to RX3SEL pins. As the H level is held therefrom, they can be used for indicator lamps and the like.
- If a H pulse is inputted to the ANALOG pin, the analog mode takes place at the positive-boing edge of the H pulse. None of RX inputs are acceped and VCO stops.
- If a H pulse is inputted to RX1SEL to RX3SEL in analog mode, a predetermined RX input is selected at the positive-going edge of the H pulse, and VCO oscillation starts.

2. Microcomputer mode (MODE=H)

In microcomputer mode, it is possible to select RX inputs during input mode (IOSEL = H : microcomputer→DAI)



Data is taken into the IC at the negative-going edge of SCK, and then is latched at the negative-going edge of REQ. According to the last 4 bits, selection of RX inputs and control of feedthrough output are carried out.

Input		D1	D2	D3
Optical input	ORX1	H	H	H
	ORX2		H	L
	ORX3		L	H
Coaxial input	CRX1	L	H	H
	CRX2		H	L
	CRX3		L	H
Analog mode		X	L	L

None of RX inputs are accepted and VCO stops in analog mode.

The feedthrough output (FTO) is turned ON/OFF by the polarity of DO.

DO	FTO
L	ON
H	OFF (fixed to L)

3. Input signal voltage range

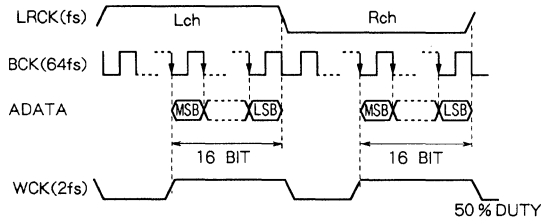
Optical input (ORX1~3)		Coaxial input (CRX1~3)	
L level	H level	Min	Max
$0.3V_{DDmax}$	$0.7V_{DDmin}$	$400mV_{P-P}$	$5V_{P-P}$

Audio Interface

1. Audio format

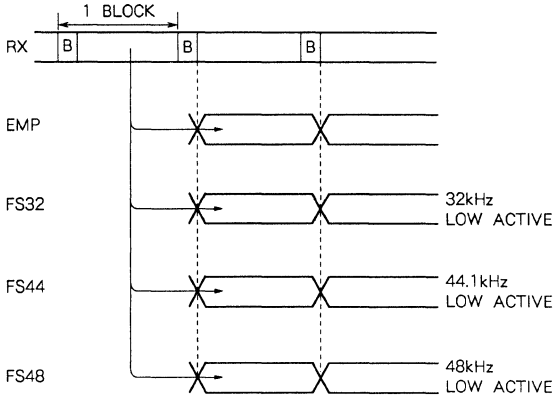
MSB first, last 16 bit

2. Audio data output timing



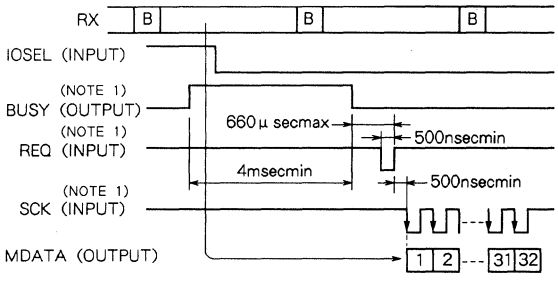
C-Bit data output timing

1. Output through dedicated pins



2.Serial data output in microcomputer mode (MODE=H)

In microcomputer mode, it is possible to read out the first 32 bits in C-bit data during output mode (IOSEL = L : DAI→ microcomputer)



Note 1.BUSY gose high if the first 32 bits in C-bit data change, compared with the previous block. It gose back low if consecutive 2 blocks consist of the same content.

Consequently, the minimum H pulse width of BUSY is 4ms (when fs = 48kHz).

If BUSY gose high, read out C-bit data after detecting the negative-going edge of BUSY because new contents of C-bit data transferred to the output register are the beginning of the next block.

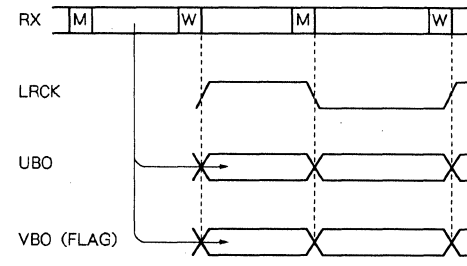
Note 2. As the first 32 bits in C-bit data are loaded to the output register at the inverting edge of REQ, be sure to invent REQ before reading out C-bit data. SCK is taken into the IC only when REQ is high, so that REQ should be constantly retained high while reading.

As BUSY compulsively goes back low at the inverting edge of REQ, let REQ go high within 660 μs (the shortest time at which BUSY may go high next) after a fall of BUSY so as to make sure that next BUSY is detected.

If it is impossible to meet the 660μs requirement due to the timer a microcomputer has, it is recommended to use both kinds of operation, to read with BUSY and to read C-bit data periodically (every several milliseconds to several tens of milliseconds) independently of BUSY.

Note 3. To read out C-bit data, set SCK to high level at the positive-going edge of REQ.

U-Bit/V-bit data output timing



Reset

By resetting after power up, it is possible to arrange the following initial settings.

1. In easy mode

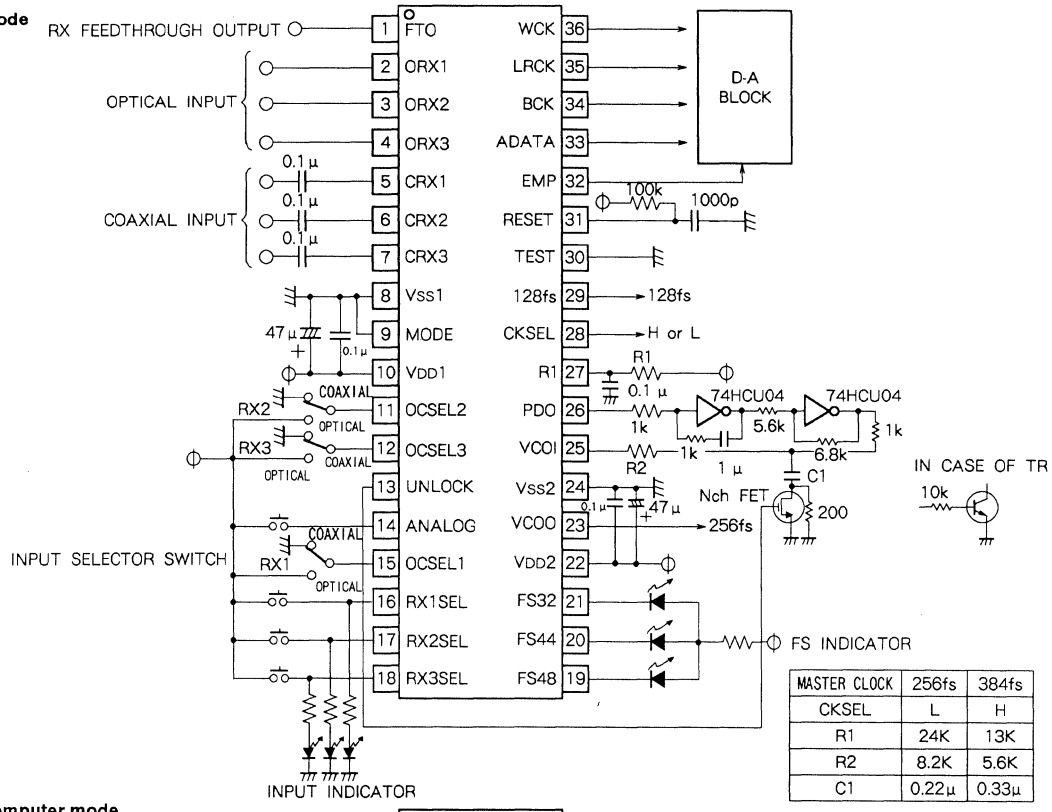
The RX1 input is selected. Optical/coaxial lines are selected by the polarity of OCSEL 1 to 3.

2. In microcomputer mode

The ORX1 (optical line) input is selected.

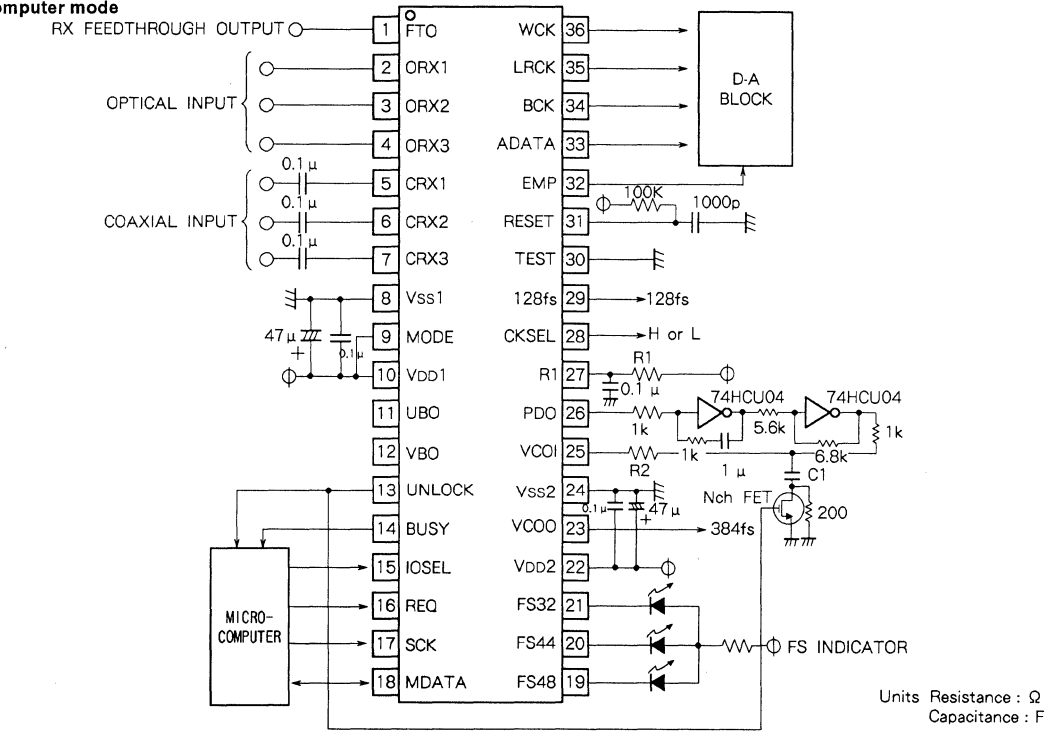
APPLICATION EXAMPLE

1) Easy mode



MASTER CLOCK	256fs	384fs
CKSEL	L	H
R1	24K	13K
R2	8.2K	5.6K
C1	0.22µ	0.33µ

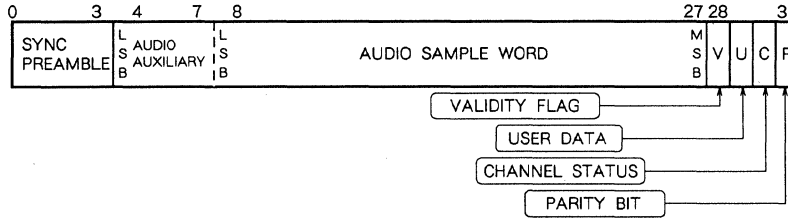
2) Microcomputer mode



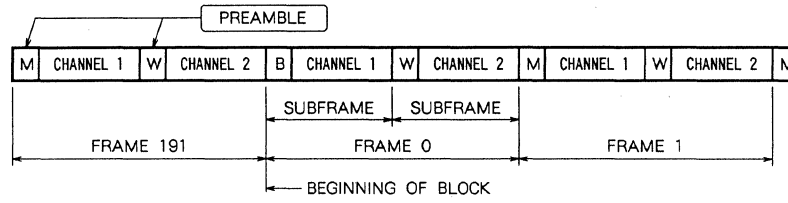
Units Resistance : Ω
Capacitance : F

EIAJ STANDARD FORMAT

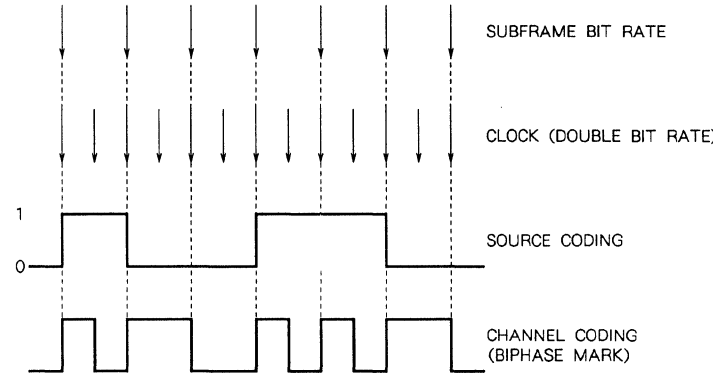
(Fig. 1)
Subframe format



(Fig. 2)
Frame format



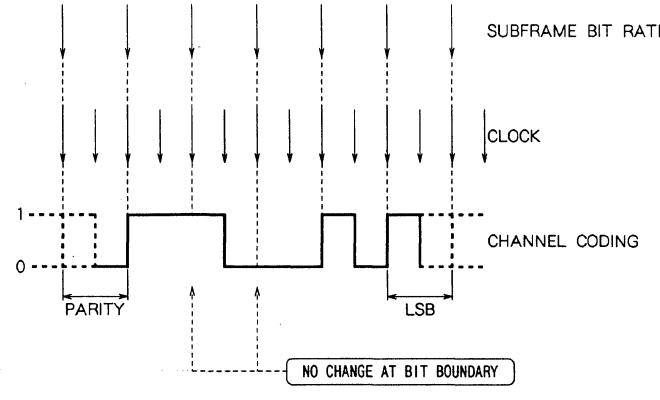
(Fig. 3)
Biphasic mark system



(Table 1) Preamble channel coding

Preamble	Channel coding	
	Precedence symbol : 0	Precedence symbol : 1
"B"	11101000	00010111
"M"	11100010	00011101
"W"	11100100	00011011

(Fig. 4)
Preamble "M"



M65811FP

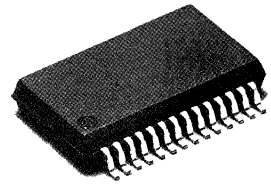
DIGITAL AUDIO JITTER ABSORBER

DESCRIPTION

The M65811FP is a semiconductor IC for removing jitters from digital audio data. To remove jitters, the IC triggers digital audio data, whose oscillation frequency has jitters, by means of jitterless clock generated by an external VCXO.

FEATURES

- Triggers jittered digital audio data, using jitterless clock generated by an external VCXO to remove jitters.
- Built-in phase detector for 2nd channel PLL.
- Selection of two kinds of master clock (384fs or 256fs)
- Outputs master clock and divisions of master clock : 128fs, 64fs (or 32fs), 2fs (word clock) and 1fs (LR clock)
- Accepts 384fs (or 256fs), 128fs, 64fs,(or 32fs), 2fs (word clock), and 1fs (LR clock) generated by the 1st channel PLL. These kinds of clocks generated by the 1st channel PLL can be output as through output.



Outline 28P2U-A

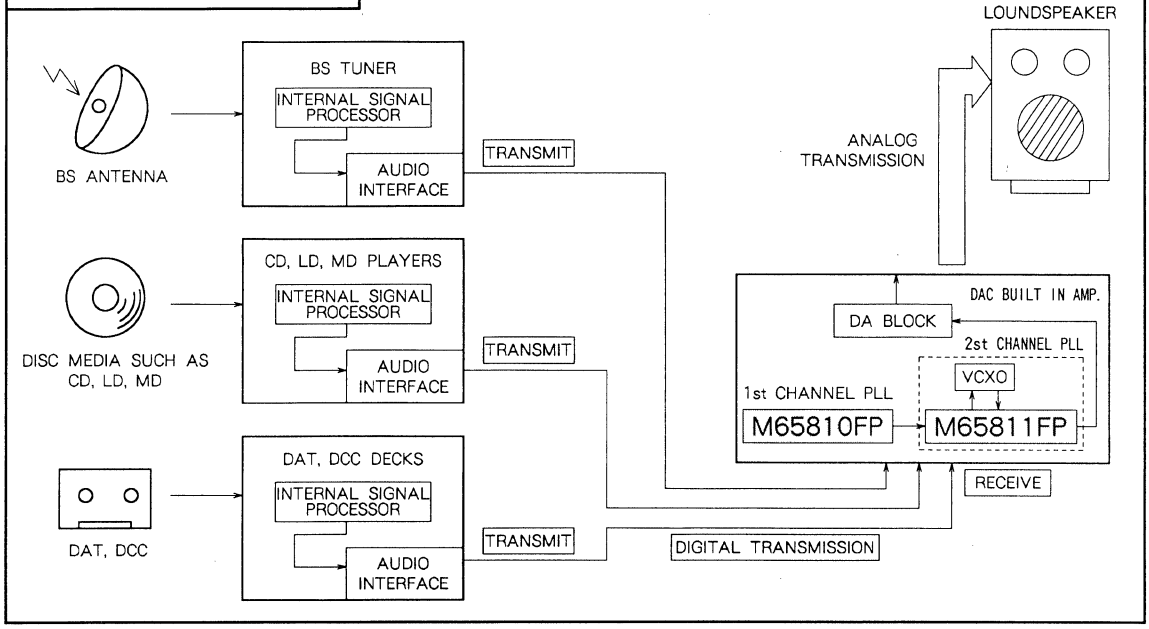
0.8mm pitch 375mil SSOP
(7.5mm × 12.8mm × 2.3mm)

RECOMMENDED OPERATING CONDITIONS

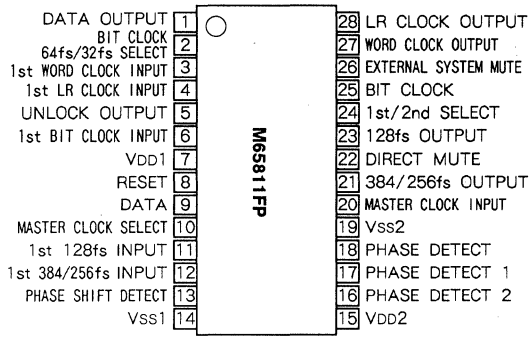
Supply voltage range ..... V_{DD} = 4.5~5.5V

Rated supply voltage ..... V_{DD} = 5V

SYSTEM CONFIGURATION

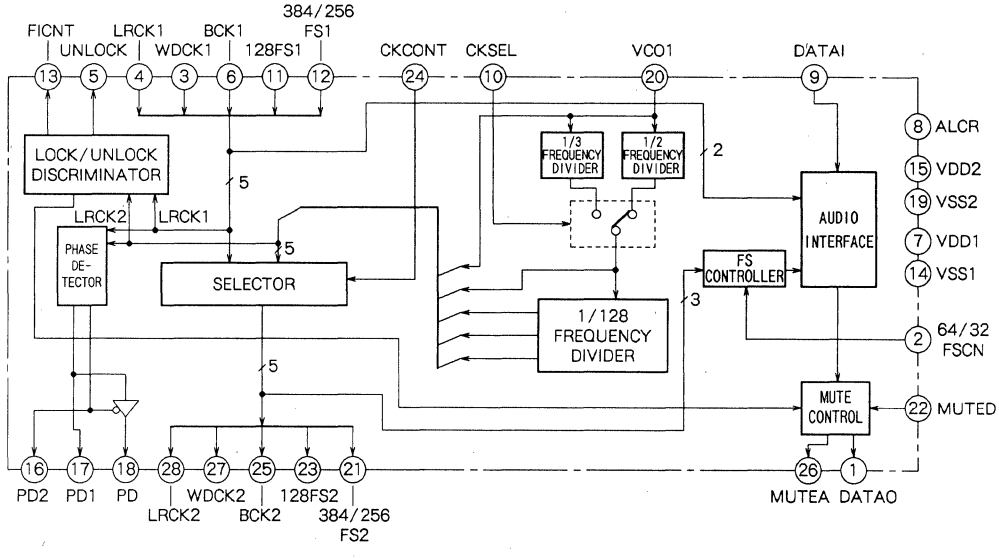


PIN CONFIGURATION



Outline 28P2U-A

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin No.	Symbol	Name	I/O	Function
①	DATA0	Data output	O	Pin㉔= H : 1st data output Pin㉔= L : 2nd data output
②	64/32FSCN	64fs/32fs select	I	Control data rate (L : 64fs, H : 32fs)
③	WDCK1	1st word clock input	I	2fs generated 1st PLL input
④	LRCK1	1st LR clock input	I	1fs generated 1st PLL input
⑤	UNLOCK	Unlock output	O	Unlock signal output (H : unlock L : lock)
⑥	BCK1	1st bit clock input	I	For input 64fs generated by 1st PLL
⑦	$V_{DD}1$		–	V_{DD} for logic gate and I/O buffer
⑧	ALCR	Reset	I	Reset signal input (L : reset)
⑨	DATAI	Data input	I	Data input (Plese input the data at MSB first, and fill the data in latter half of 2fs.)
⑩	CKSEL	Master clock select	I	(L : enable to input 256fs from pin⑳ H : enable to input 384fs flom pin⑳)
⑪	128FS1	1st 128fs input	I	For input 128fs generated by 1st PLL
⑫	384/256FS1	1st 384/256fs input	I	For input 384fs or 256fs generated by 1st PLL
⑬	FICNT	Phase shift detect	O	Phase shift signal output (L : phase shift between 1st and 2nd LR clock)
⑭	$V_{SS}1$		–	GND for logic gate and I/O buffer
⑮	$V_{DD}2$		–	V_{DD} for phase comparator
⑯	PD2	Phase detect 2	O	Phase comparator output (Connects to external 3 state buffer enable.)
⑰	PD1	Phase detect 1	O	Phase comparator output (Connects to external 3 state buffer input.)
⑱	PD	Phase detect	O	Phase comparator output (The built-in 3 state buffer's output.)
⑲	$V_{SS}2$		–	GND for phase comparator
⑳	VCOI	Master clock input	I	For input master clock generated by external VCXO
㉑	384/256FS2	384/256fs output	O	Pin㉔= H : 1st 384/256fs clock output Pin㉔= L : 2nd 384/256fs clock output
㉒	MUTED	Direct mute	I	Compulsory data mute input (H : mute ON L : mute OFF)
㉓	128FS2	128fs output	O	Pin㉔=H:1st 128fs clock output Pin㉔=L:2nd 128fs clock output
㉔	CKCONT	1st/2nd select	I	Switching output data and clocks (L : 2nd PLL's clock, data H : 1st PLL's clock, data)
㉕	BCK2	Bit clock output	O	Pin㉔=H:1st bit clock(64 or 32fs)output Pin㉔=L:2nd 1fs clock(64 or 32fs)output
㉖	MUTEA	External system mute	O	External system mute signal output
㉗	WDCK2	Word clock output	O	Pin㉔= H : 1st 2fs clock output Pin㉔= L : 2nd 2fs clock output
㉘	LRCK2	LR clock output	O	Pin㉔= H : 1st 1fs clock output Pin㉔= L : 2nd 1fs clock output

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DD}-V_{SS}$	Supply voltage	− 0.3~6.5	V
V_I	Input voltage	V_{SS} − 0, 3~V_{DD} + 0.3	V
P_d	Power dissipation	300	mW
T_{opr}	Operation temperature	−20~70	℃
T_{stg}	Storage temperature	−40~125	℃

RECOMMENDED OPERATING CONDITIONS

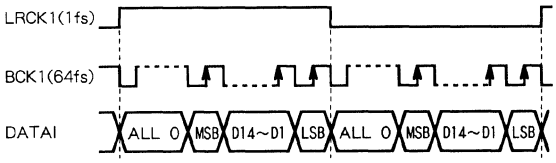
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{IH}	Input voltage ("H" level)		0.7V_{DD}	−	V_{DD}	V
V_{IL}	Input voltage ("L" level)		V_{SS}	−	0.3V_{DD}	V
F_{VCOIN}	Oscillation frequency input	CKSEL = L	−	256fs	−	Hz
F_{VCOIN}	Oscillation frequency input	CKSEL = H	−	384fs	−	Hz
fs	Input sampling frequency		−	64fs	−	Hz

ELECTRIC CHARACTERISTICS (DC)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current		−	6	15	mA
V_{OH}	Output voltage ("H" level)	V_{DD} = 5V, Io < 1 μ A	4.9	−	5	V
V_{OL}	Output voltage ("L" level)		0	−	0.1	V
I_{IN}	Input leak current	Vi = V_{DD} or V_{SS}	− 1	−	+ 1	μ A
V_{IH}	Input voltage	V_{DD} = 5.5V	3.85	−	5.5	V
V_{IL}	Input voltage	V_{DD} = 4.5V	0	−	1.35	V
I_{OH}	Output current	V_{OH} = 4.1V, V_{DD} = 4.5V	−	−	− 5	mA
I_{OL}	Output current		14	−	−	mA

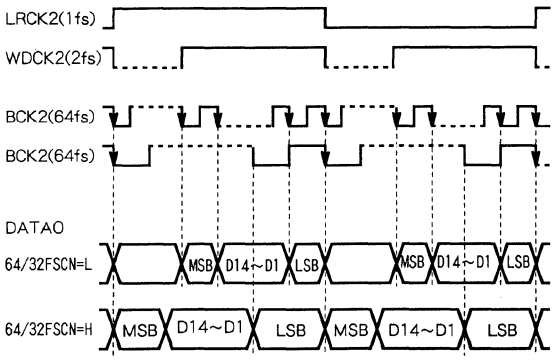
FUNCTION

INPUT DATA FORMAT



- LRCK (fs), BCK (64fs) and DATA are required as 1st PLL signals. 384/256fs, 128fs, and WDCK (2fs) are irrelevant to data input. If not using, fix these input pins to L or H.
- Audio data is taken into the IC in such a manner that the last 16bits from a LRCK edge enter at the positive-going edge of BCK1 with MSB first.

OUTPUT DATA FORMAT



- If 64/32FSCN = L, audio data is output triggered at the negative-going edge of 64fs with MSB first.
- In this case, audio data is output in a format that the last 16bits from a LRCK edge are output. BCK2, a dedicated pin, outputs a 64fs bit clock.

- If 64/32FSCN = H, audio data is output triggered at the negative-going edge of 32fs with MSB first.
- In this case, audio data is output over an entire period of each cycle of LRCK. BCK2 pin outputs a 32fs bit clock.

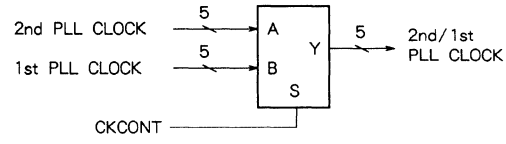
SELECTION OF VCXO

Two kinds of VCXO can be used according to the following combinations.

Recommended VCXO : (for 384fs)
FAR – M2SC – 18M432 – D300 (for 256fs)
FAR – M2SC – 12M288 – D300
Both are made by Fujitsu.

CKSEL	Applicable VCXO
L	256fs
H	384fs

SELECTION OF PLL



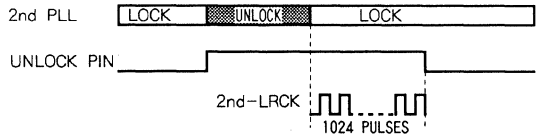
CKCONT	PLL
L	2nd channel
H	1st channel

Operation of 64/32 FSCN is effective even if the 1st PLL is selected.

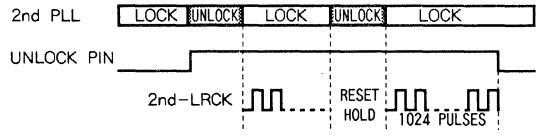
		CKCONT	
		L	H
64/32 FSCN	L	Selects the 2nd-cahnnel 64fs bit clock and 2nd channel data in sync with the clock	Selects the 1st-cahnnel 64fs bit clock and 1st channel data in sync with the clock
	H	Selects the 2nd-cahnnel 32fs bit clock and 2nd channel data in sync with the clock	Selects the 1st-cahnnel 32fs bit clock and 1st channel data in sync with the clock

UNLOCK OPERATION

If PLL is unlocked a "H" signal is output and output data is automatically muted. If the internal circuitry decides that PLL has been locked over consecutive 1024 pulses of 2nd LRCK, the UNLOCK pin goes back low and the unlock state is canceled.



(Occurrence of an unlock state when making lock state judgment)

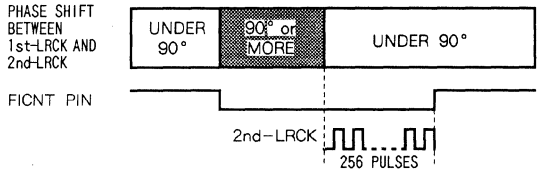


90° PHASE SHIFT DETECTING(FICNT)OPERATION

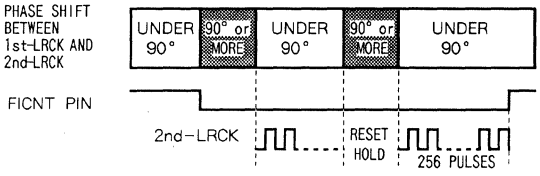
If 90° or more phase shift occurs between 1st LRCK and 2nd LRCK and PLL is about to be unlocked, a "L" signal is output at the FICNT pin.

With this signal it is possible to configure a system that broaden the filter band of the phase detector just before PLL is inlocked.

If 90° or more phase shift does not occur over a period corresponding to 256 pulses of 2nd LRCK, the FICNT pin goes back high.



(Occurrence of 90° or more phase shift when making judgment of under 90° phase shift)

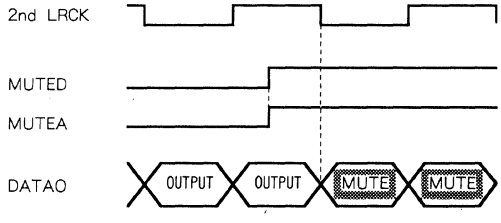


MUTE CONTROL

(1) Forced mute

Data is compulsively muted by applying a positive-going edge to the MUTED pin. Audio data is muted in units of words just after the edge is detected at MUTED.

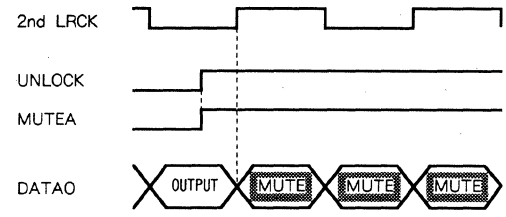
MUTEA goes high in sync with the positive-going edge inputted to MUTED.



(2) Unlocked PLL and MUTE control

If PLL is unlocked the UNLOCK and MUTEA outputs go high, and output data is automatically muted.

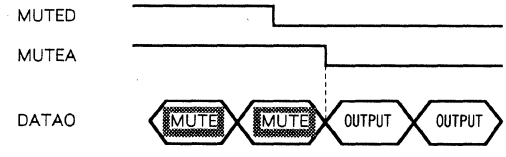
Mute operation is carried out in units of words as in the case of forced mute.



(3) Cancelling mute

Mute is canceled by inputting negative-going edge as the MUTED pin whether it is forced mute or automatic mute.

MUTEA at this point returns to L level at a word break of audio data.



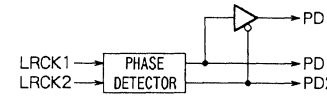
USE OF PHASE DETECTOR OUTPUTS

PD (Pin 13) is the output pin of the 3-state buffer contained in the M65811FP. (See the application example)

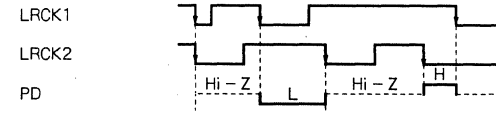
PD1 and PD2 are used to separate power supply and GNDof the 3-state buffer completely from the IC.

An outline of a phase detector is shown in ①, and operation timing is given in ②. The phase detector compares LRCK1 generated by the 1st channel and LRCK2 generated by the 2nd channel to check their phase at the negative-going edge, then outputs their phase error.

① AN OUTLINE OF A PHASE DETECTOR



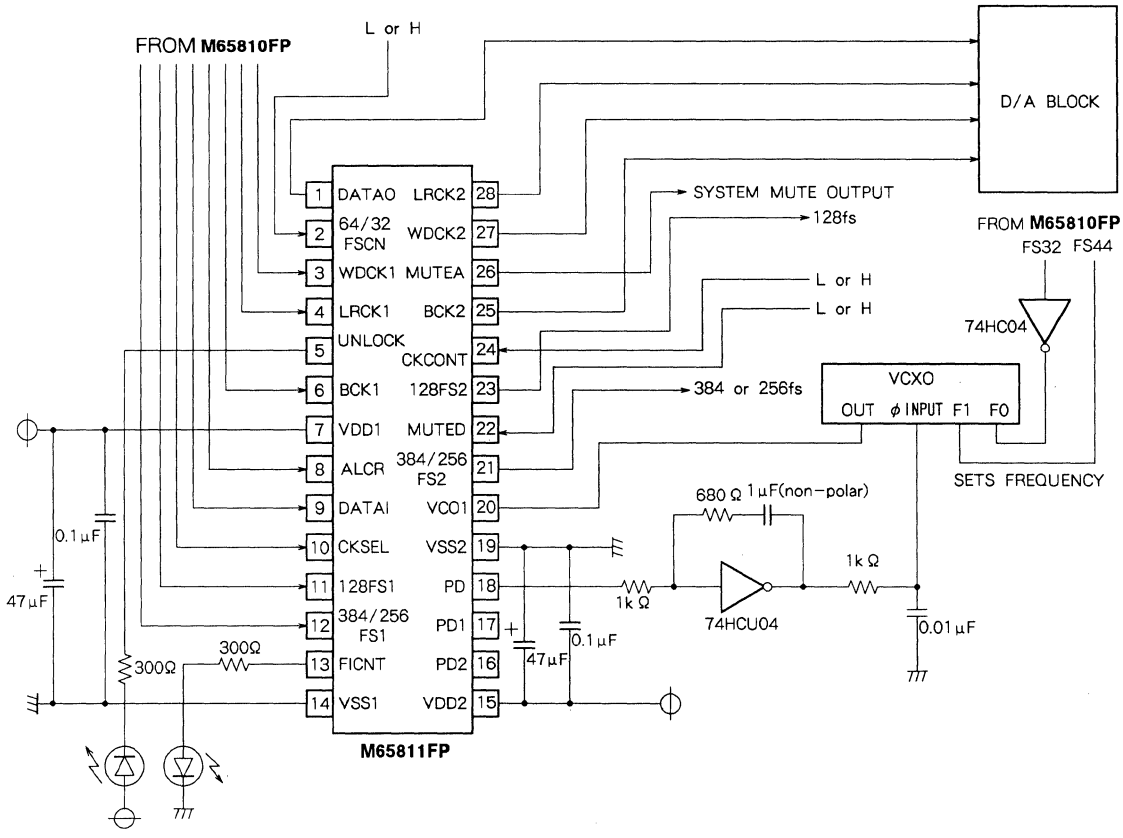
② OPERATION TIMING



USE OF POWER SUPPLY AND GROUND

In the M65811FP, the power supply and ground to the phase detector are separated from that to the clock circuitry in order to minimize influences of clock noise and radiation. Supply a stable power source free from noise and fluctuation to the power supply and ground (pins 15 and 19) dedicated to phase detector outputs.

APPLICATION EXAMPLE



BS/CS TUNER LSI KIT

7

M50590AFP

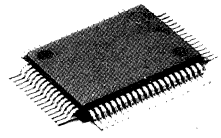
BS PCM SIGNAL DECODER

DESCRIPTION

The M50590AFP is a full-CMOS LSI developed for broadcasting satellite (BS) receivers. It is used in voice signal decoder in BS tuner and in TV and VCR with built-in BS tuner. The IC decodes voice signals from the output data of the QPSK decoder.

FEATURES

- Selectable main clock
  (36.864MHz/12.288MHz)
- Clock outputs for digital filter
  36.864MHz main clock : 768fs/384fs/256fs/192fs/128fs
  12.288MHz main clock : 256fs/128fs
- Built-in 4-Kbit SRAM for deinterleaving
- Possible to select forced muting by control code
- PLL circuit built in for clock regeneration
- Output signal selector built in
  This eliminates the need for an external signal selector, which is used when a digital filter and D-A converter are commonly used within a system.



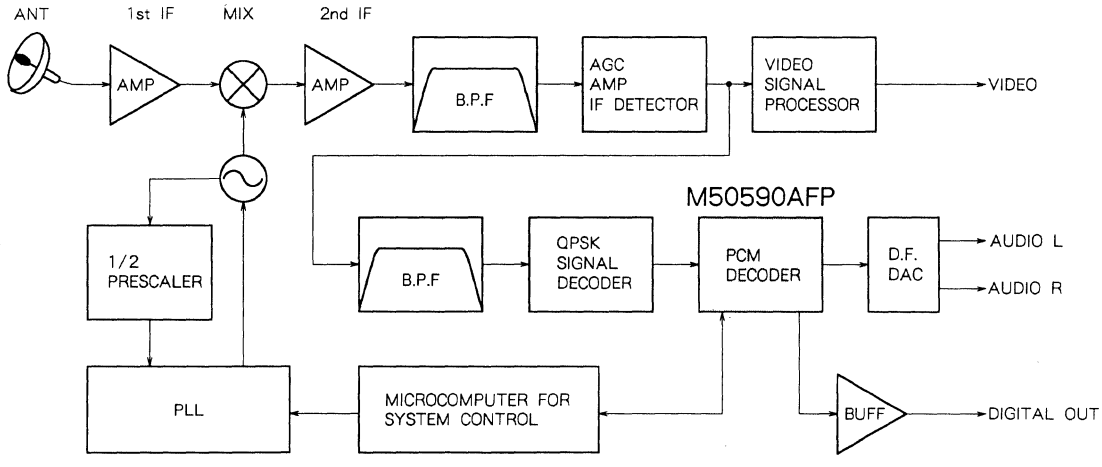
Outline 72P6-B

0.8mm pitch QFP
(18.0mm × 13.2mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{DD} = 4.5~5.5V
Rated supply voltage ..... V_{DD} = 5.0V

SYSTEM CONFIGURATION



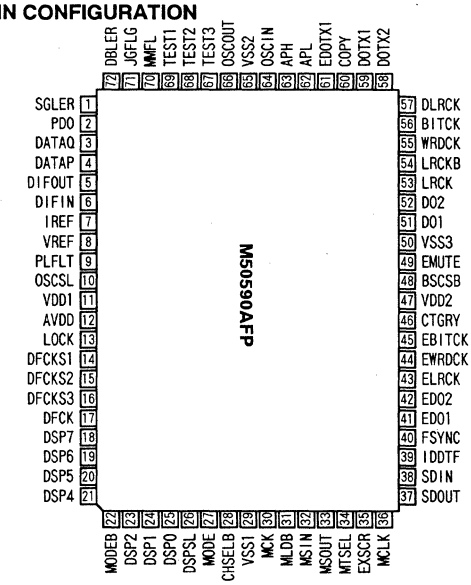
M50590AFP

BS PCM SIGNAL DECODER

BUILT-IN FUNCTIONS

- Differential conversion of QPSK signals. Parallel-to-serial conversion.
- Bit stream input/output
- Frame sync detection and protection
  (Complete coincidence detection mode : forward protection 8F/backward protection 3F)
- Descramble (10-dimensional M series)
- Majority logic for control code (1 time/15F)
- Deinterleaving
- Error detection and correction by BCH (63/56) code
- Data input/output after error detection and correction (Scramble decoder supported)
- Detection and correction of range bit error by BCH (7/3) code
- Detection and output of pay-TV flag
- In mode A : 10→14 bit expansion
- In mode B : upper bits protection
- Data interpolation/preceding value holding for voice data errors
- 8-step soft muting
- D/A converter IF (2 channels)
- Digital audio interface outputs (2 channels) (Compliance with EIAJ CP-340)

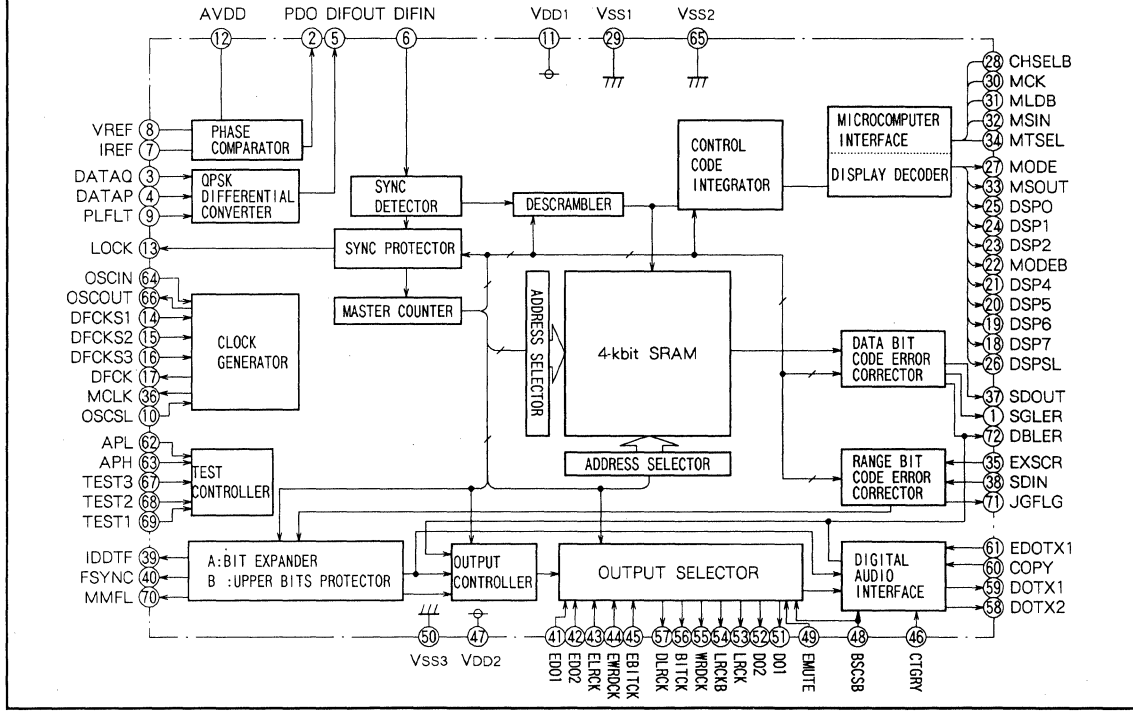
PIN CONFIGURATION



Outline 72P6-B

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin No.	Name	I/O	Function
①	SGLER	O	BCH 63/56 single error detection flag (error⇨ "H")
②	PDO	O	Phase comparator (charge pump) output : VCXO control
③	DATAQ	I	Data Q input pin after QPSK decoding
④	DATAP	I	Data P input pin after QPSK decoding
⑤	DIFOUT	O	Serial data (bit stream) output after differential conversion
⑥	DIFIN	I	Serial data input after differential conversion
⑦	IREF	–	Charge pump reference current setting pin
⑧	VREF	–	VCXO free-running adjusting voltage setting pin
⑨	PLFLT	I	VCXO free-running adjustment mode setting pin (Set to "L" normally)
⑩	OSCSL	I	Clock frequency setting pin "H"36.864MHz "L"12.288MHz
⑪	V_{DD1}	–	Power supply 1 (+5V)
⑫	AVDD	–	Power supply to charge pump (+5V)
⑬	LOCK	O	Sync state detection flag (LOCK⇨ "H")
⑭	DFCKS1	I	Clock setting pin 1 for digital filter
⑮	DFCKS2	I	Clock setting pin 2 for digital filter
⑯	DFCKS3	I	Clock setting pin 3 for digital filter
⑰	DFCK	O	Clock outputs for digital filter 128fs/192fs/256fs/384fs/768fs
⑱	DSP7	O	Test output 7
⑲	DSP6	O	Test output 6
⑳	DSP5	O	Test output 5
㉑	DSP4	O	Test output 4
㉒	MODEB	O	Mode inversion output (Mode A⇨ "H", Mode B⇨ "L")
㉓	DSP2	O	Test output 2
㉔	DSP1	O	Test output 1
㉕	DSP0	O	Test output 0
㉖	DSPSL	O	Test output
㉗	MODE	O	A/B (Mode A⇨ "L", Mode B⇨ "H")
㉘	CHSELB	I	Microcomputer IF : M50590AFP chip select ("L" ⇨select)
㉙	V_{SS1}	–	GND1
㉚	MCK	I	Microcomputer IF : Data shift clock
㉛	MLDB	I	Microcomputer IF : Data load pulse
㉜	MSIN	I	Microcomputer IF : Control data input (serial)
㉝	MSOUT	O	Control code output
㉞	MTSEL	I	Validity of control code muting bit ("H" ⇨valid)
㉟	EXSCR	I	External scramble pin (control by PN signal). Set to "L" normally.
㊱	MCLK	O	2.048MHz master clock output
㊲	SDOUT	O	Serial data output after correction by BCH63/56 code (Scramble supported)
㊳	SDIN	I	Serial data input after correction by BCH63/56 code (Scramble supported)
㊴	IDDTF	O	Window pulse for reading independent data
㊵	FSYNC	O	Frame sync pulse f = 1kHz
㊶	EDO1	I	External serial data input 1
㊷	EDO2	I	External serial data input 2
㊸	ELRCK	I	External LR clock input
㊹	EWRDCK	I	External WORD clock input
㊺	EBITCK	I	External BIT clock input
㊻	CTGRY	I	Digital audio interface Category code setting "L" ⇨general "H" ⇨BS
㊼	V_{DD2}	–	Power supply 2 (+5V)

PIN DESCRIPTION (Continue)

Pin No.	Name	I/O	Function
㊽	BSCSB	I	Output route select signal "L" ⇨M50590AFP signal output "H" ⇨external signal output
㊾	EMUTE	I	External muting input "L" ⇨Muting
㊿	V_{SS3}	–	GND3
(51)	DO1	O	D/A IF : Serial data output 1
(52)	DO2	O	D/A IF : Serial data output 2
(53)	LRCK	O	D/A IF : LR clock output
(54)	LRCKB	O	D/A IF : LR clock inverted output
(55)	WRDCK	O	D/A IF : word clock output
(56)	BITCK	O	D/A IF : Bit clock output
(57)	DLRCK	O	D/A IF : Delayed LR clock output
(58)	DOTX2	O	Digital audio interface : Output 2
(59)	DOTX1	O	Digital audio interface : Output 1
(60)	COPY	I	Digital audio interface Copy bit setting "L" ⇨Copy enabled "H" ⇨Copy disabled
(61)	EDOTX1	I	External digital out input
(62)	APL	I	Sets all output pins to "L" (Test pin. Set to "H" normally)
(63)	APH	I	Sets all output pins to "H" (Test pin. Set to "H" normally)
(64)	OSCIN	I	Clock input pin (12.288MHz/36.864MHz)
(65)	V_{SS2}	–	GND2
(66)	OSCOUT	O	Clock input pin (12.288MHz/36.864MHz)
(67)	TEST3	I	Test mode setting pin 3 (Set to "H" normally)
(68)	TEST2	I	Test mode setting pin 2 (Set to "H" normally)
(69)	TEST1	I	Test mode setting pin 1 (Set to "H" normally)
(70)	MMFL	O	Flag for detection of data inconformity of upper bits in mode B (Errot⇨ "H")
(71)	JGFLG	O	Flag for detection of range bit double error (Error⇨ "H")
(72)	DBLER	O	Flag for detection of BCH 63/65 double error (Error⇨ "H")

DIGITAL FILTER CLOCK SETTING METHOD

Input frequency:36.864MHz

DFCKS1	DFCKS2	DFCKS3	fs	Mode A	DUTY	Mode B	DUTY
L	H	L	128	4.096MHz	1/2	6.144MHz	1/2
H	H	L	192	6.144MHz	1/2	9.216MHz	1/2
L	L	H	256	8.192MHz	1/3	12.288MHz	1/2
H	L	H	384	12.288MHz	1/2	18.432MHz	1/2
L	H	H	768	24.576MHz	1/3	36.864MHz	1/2

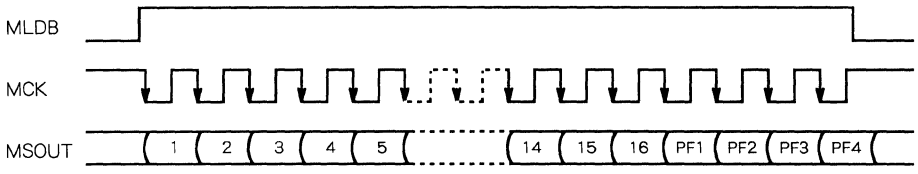
Input frequency:12.288MHz

DFCKS1	DFCKS2	DFCKS3	fs	Mode A	DUTY	Mode B	DUTY
H	L	H	128	4.096MHz	1/2	6.144MHz	1/2
L	H	H	256	8.192MHz	1/3	12.288MHz	1/2

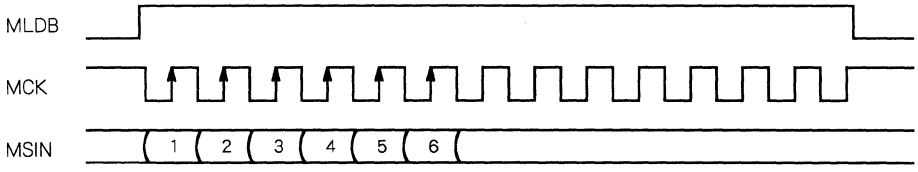
MICROCOMPUTER INTERFACE

1) Reading out control code and pay-TV flag

Control code is output from MSOUT in synchronization with the clock from MCK, and in the sequence of from bit 1 to bit 16. If the number of clock pulses is 16, control code only is output : if 20, a pay-TV flag is output following control code.(1ch~4ch)



2) Writing control data on voice output selector



3) Other notes

- Data transmission is disabled unless CHSELB = "L".
- To read the pay-TV flag, MLDB should be kept at "L" for at least 1 ms.

4) Voice output control data

<table>
<tr><th>No.</th><th>Bit name</th><th>Function</th></tr>
<tr><td>1</td><td>ENB</td><td>"H" : Data after No. 2 bit is valid
"L" : Data after No. 2 bit is invalid</td></tr>
<tr><td>2</td><td>TVAD</td><td>Outputs 1/2⇔Switching between TV voice and additional voice

"H" : DO1/DOTX1→TV voice output
DO2/DOTX2→Additional voice output

"L" : DO2/DOTX2→TV voice output
DO1/DOTX1→Additional voice output
Enabled only when in mode A broadcasting
In mode B, all outputs are TV voice</td></tr>
<tr><td>3</td><td>TVMA</td><td rowspan="2"><table><tr><th>TVMA</th><th>TVSB</th><th>Output</th></tr><tr><td>L</td><td>L</td><td>None</td></tr><tr><td>H</td><td>L</td><td>CH1 + CH1 (Main voice)</td></tr><tr><td>L</td><td>H</td><td>CH2 + CH2 (Sub voice)</td></tr><tr><td>H</td><td>H</td><td>CH1 + CH2 (Main + Sub)</td></tr></table>In double-voice broadcasting, main-sub voice selection data acts on TV voice.</td></tr>
<tr><td>4</td><td>TVSB</td></tr>
<tr><td>5</td><td>ADMA</td><td rowspan="2"><table><tr><th>ADMA</th><th>ADSB</th><th>Output</th></tr><tr><td>L</td><td>L</td><td>None</td></tr><tr><td>H</td><td>L</td><td>CH3 + CH3 (Main voice)</td></tr><tr><td>L</td><td>H</td><td>CH4 + CH4 (Sub voice)</td></tr><tr><td>H</td><td>H</td><td>CH3 + CH4 (Main + Sub)</td></tr></table>In double-voice broadcasting, main-sub voice selection data acts on additional voice.</td></tr>
<tr><td>6</td><td>ADSB</td></tr>
</table>

DIGITAL AUDIO INTERFACE

Channel status (C – bit)

Type II – form I (Home-use digital audio equipment applications)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	①	1	0	0	0	0	②							
16	0	0	0	0	③				④				⑤		0	0
32	0	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	0
⇩	All fixed to "0"															
176	0	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	0

①Copy bit
"0" : Digital copy disabled(㊿pin "H")
"1" : Digital copy enabled(㊿pin "L")

②Category code
"00000000" : Genaral(㊺pin "L")
"00100000" : BS(㊺pin "H")

③Channel number
"0000" : No designation(fixed)

④Sample frequency
"1100" : 32kHz(Mode A)
"0100" : 48kHz(Mode B)

⑤Clock accuracy
"00" : Level II (fixed)

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DD}-V_{SS}	Supply voltage	− 0.3～+ 7.0	V
V_I	Input voltage	V_{SS}−0.3≦V_I≦V_{DD}+0.3	V
V_O	Output voltage	V_{SS} ≦ V_O ≦ V_{DD}	V
P_t	Max. power dissipation	630	mW
T_{opr}	Operating temperature	− 10～+ 70	℃
T_{stg}	Storage temperature	− 40～+ 125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	Input voltage ("H" level)	3.5	−	V_{DD}	V
V_{IL}	Input voltage ("L" level)	V_{SS}	−	1.5	V
V_{OSC}	OSC input amplitude	0.5	−	V_{DD}	V

Note. · Insert a bypass capacitor of capacitance 0.1μF or more between the V_{DD} and V_{SS} pins.
· Oscillation input amplitude is the amplitude of the clock inputted to pin ㉘(OSCIN).

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{DD} = 5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Operating supply voltage	Ta = − 10～70℃	4.5	5.0	5.5	V
I_{DD}	Supply current	In quiescent state : V_{DD} = 5.5V : Input pin : V_{DD}	−	−	65	mA
Input pin 〔＊1〕						
I_{IH1}	Input current ("H" level)	V_{IH1} = V_{DD}	− 2	−	2	μA
I_{IL1}	Input current ("L" level)	V_{IL1} = V_{SS}	− 2	−	2	μA
Input pins (Pull−up) 〔＊2〕						
I_{IH2}	Input current ("H" level)	V_{IH2} = 5.49V	− 1	−	1	μA
I_{IL2}	Input current ("L" level)	V_{IL2} = V_{SS}	− 90	− 60	− 25	μA
Output pin 1 〔＊3〕						
I_{OH1}	Output current ("H" level)	V_{DD} = 4.5V, V_{OH1} = 4.1V	−	−	− 1	mA
I_{OL1}	Output current ("L" level)	V_{DD} = 4.5V, V_{OL1} = 0.4V	1	−	−	mA
Output pins 2 〔＊4〕						
I_{OH2}	Output current ("H" level)	V_{DD} = 4.5V, V_{OH2} = 4.1V	−	−	− 1.2	mA
I_{OL2}	Output current ("L" level)	V_{DD} = 4.5V, V_{OL2} = 0.4V	1.2	−	−	mA
Output pins 3 〔＊5〕						
I_{OZ}	Output leak current	V_I = 0～V_{DD}	−	−	± 2	μA

〔＊1〕 DATAQ, DATAP, DIFIN, PLFLT, OSCSL, DFCKS1, DFCKS2, DFCKS3, EXSCR, SDIN, EDO1, EDO2, ELRCK, EWRDCK, EBITCK, CTGRY, BSCSB, EMUTE, COPY, EDOTX1, APL, APH, TEST3, TEST2, TEST1
〔＊2〕 CHSELB, MCK, MLDB, MSIN, MTSEL
〔＊3〕 SGLER, DIFOUT, LOCK, DSP7, DSP6, DSP5, DSP4, MODEB, DSP2, DSP1, DSP0, DSPSL, MODE, MCLK, SDOUT, IDDTF, FSYNC, DO1, DO2, LRCK, LRCKB, WRDCK, BITCK, DLRCK, MMFL, JGFLG, DBLER, MSOUT
〔＊4〕 DFCK, DOTX2, DOTX1
〔＊5〕 MSOUT

ELECTRICAL CHARACTERISTICS (charge pump)

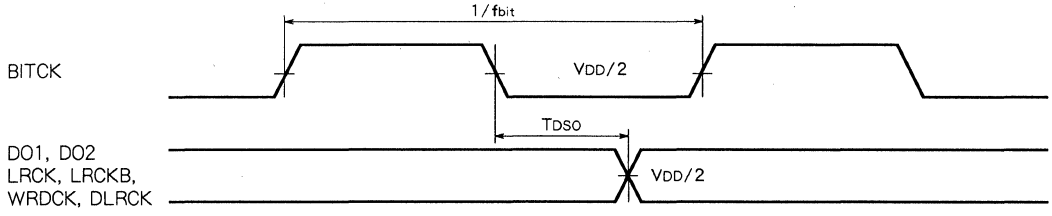
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{PDO}	Output leak current (PLFLT = "L")	V_{DD} = 5.5V, V_{IREF} = 2.0V, V_{PDO} = 0～V_{DD}	−	−	± 2	μA
I_{IREF}	Charge pump reference current	V_{DD} = 5.5V, V_{IREF} = 2.0V	50	75	120	μA

Pins related to charge pump : PDO, IREF, VREF,(PLFLT)

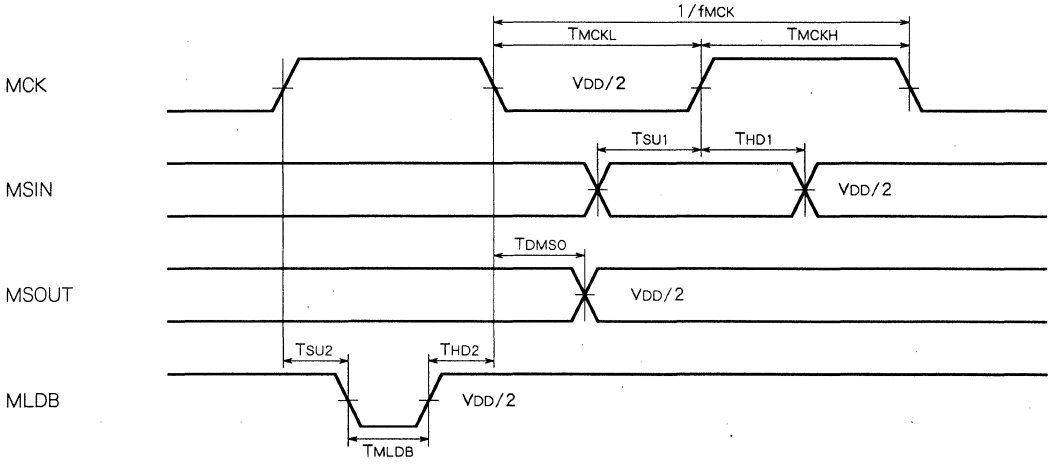
AC CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
D/A IF (DO1, DO2, LRCK, LRCKB, WRDCK, BITCK, DLRCK)						
f_{bit}	Bit clock frequency	fs = 32kHz (A−MODE)	–	64 · fs	–	kHz
		fs = 48kHz (B−MODE)	–	64 · fs	–	kHz
T_{DSO}	Output delay time		–	–	50	ns
Microcomputer interface (MCK, MLDB, MSIN, MSOUT)						
f_{MCK}	Clock frequency		–	–	1	MHz
T_{MCKH} T_{MCKL}	Clock pulse width		300	–	–	ns
T_{SU1} T_{SU2}	Input setup time		200	–	–	ns
T_{HD1} T_{HD2}	Input hold time		200	–	–	ns
T_{MLDB}	MLDB pulse width		300	–	–	ns
T_{DMSO}	Output delay time		–	–	100	ns

Note. The MLDB pulse width is 1m min. Only when reading out the pay-TV flag.



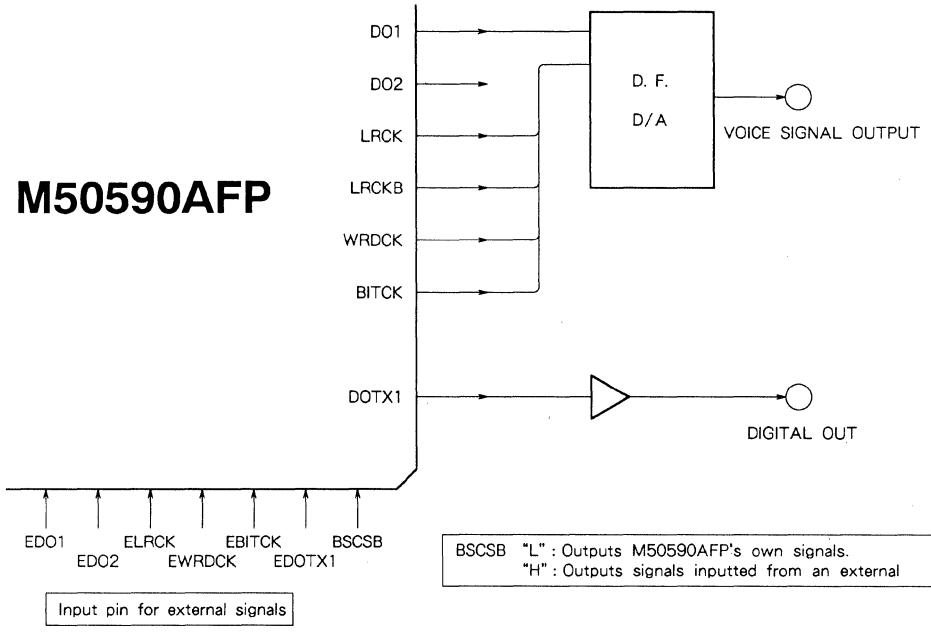
D/A IF TIMING



MICROCOMPUTER INTERFACE

OUTPUT SIGNAL SELECTOR BUILT-IN

No external signal selector is needed for common use in a system of digital filter, D/A converter etc.(See figure below.)



Note. Do not use this function if DOTX2 is used.

M65880FP

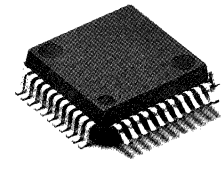
BS/CS PCM SIGNAL DECODER

DESCRIPTION

The M65880FP is a full-CMOS LSI developed for broadcasting satellite (BS/CS) receivers. It is used in voice signal decoder in BS/CS tuner and in TV and VCR with built-in BS/CS tuner. The IC decodes voice signals from the output data of the QPSK decoder.

FEATURES

- Clock regeneration from QPSK signal/bit stream input
- Possible to select the polarity of phase error voltage for PLL control
- Selectable main clock (36.864MHz/18.432MHz)
- Clock outputs for digital filter
  36.864MHz main clock : 768fs/384fs
  18.432MHz main clock : 384fs/192fs
- Master frame discrimination
- Built-in 2-Kbit SRAM for deinterleaving
- Built-in selector for double decoder
- PLL circuit built-in for clock regeneration
- 44-pin compact package



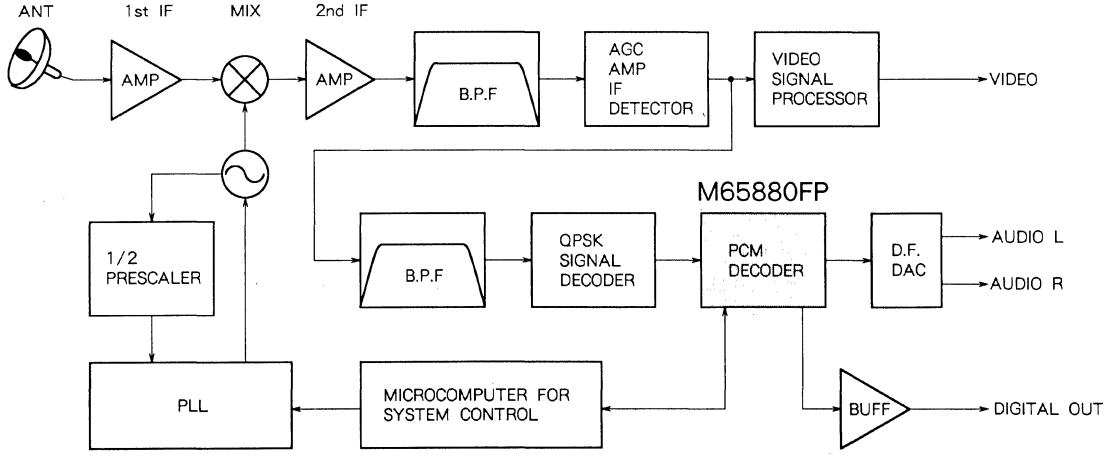
Outline 44P6N-A

0.8mm pitch QFP
(10.0mm × 10.0mm × 2.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{DD} = 4.5~5.5V
Rated supply voltage ..... V_{DD} = 5.0V

SYSTEM CONFIGURATION



MITSUBISHI ELECTRIC

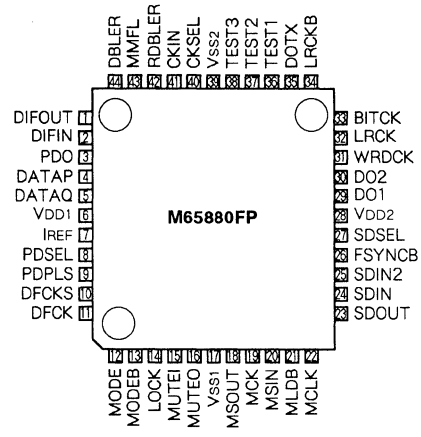
M65880FP

BS/CS PCM SIGNAL DECODER

BUILT-IN FUNCTIONS

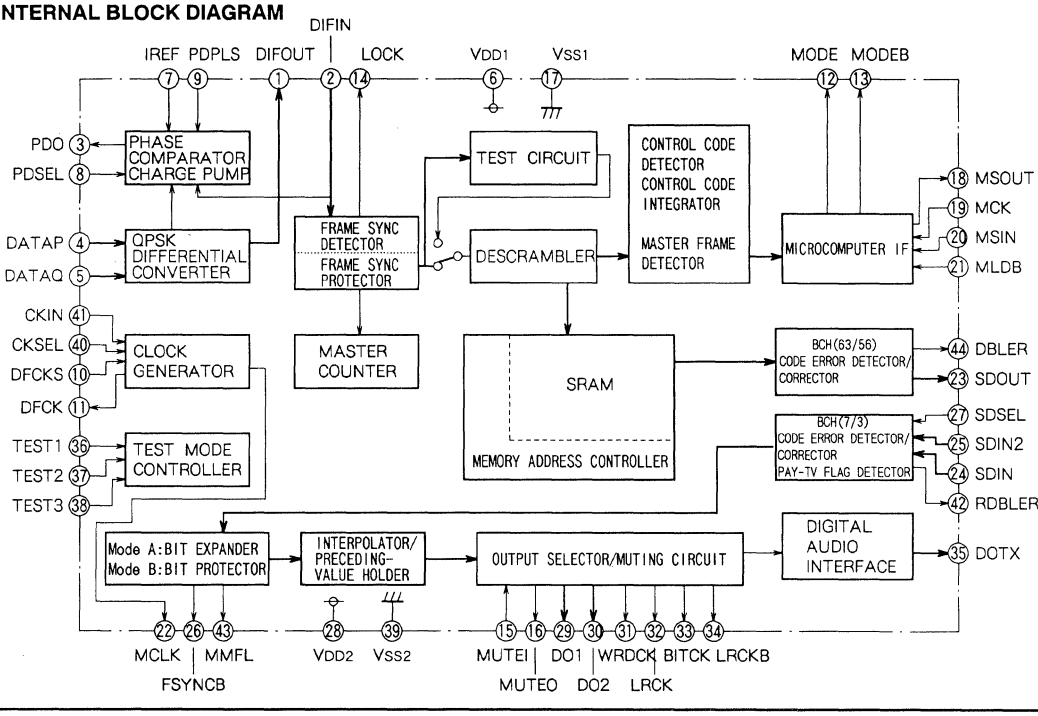
- Differential conversion of QPSK signals. Parallel-to-serial conversion.
- Bit stream input/output
- Frame sync detection and protection
  (Complete coincidence detection mode : forward protection 8F/backward protection 3F)
- Descramble (10-dimensional M series)
- Majority logic for control code (1 time/15F)
- Deinterleaving
- Error detection and correction by BCH (63/56) code
- Data input/output after error detection and correction (Scramble decoder supported)
- Detection and correction of range bit error by BCH (7/3) code
- Detection of pay-TV flag by majority logic (1 time/15F)
- In mode A : 10→14 bit expansion (Supports 8 ranges)
- In mode B : upper bits protection (Supports 8 ranges)
- Data interpolation/preceding value holding for voice data errors
- 8-step soft muting by channel
- D/A converter IF (2 channels)
- Digital audio interface outputs (Compliance with EIAJ CP-340)

PIN CONFIGURATION



Outline 44P6N-A

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Name	I/O	Function
①	DIFOUT	O	Bit stream output after differential conversion and parallel-serial conversion
②	DIFIN	I	Bit stream input (Normally connected to DIFOUT)
③	PDO	O	Phase comparator (charge pump) output for VCXO control
④	DATAP	I	Data P input pin after QPSK decoding
⑤	DATAQ	I	Data Q input pin after QPSK decoding
⑥	V_{DD1}	Power	Power supply pin 1 (+5V)
⑦	IREF	Power	Charge pump reference current setting pin
⑧	PDSEL	I	Phase comparator signal selection L : Bit stream input H : QPSK signal input
⑨	PDPLS	I	Pin to select the polarity of error voltage of phase comparator L : Inverted polarity of M56790FP H : Polarity of M56790FP
⑩	DFCKS	I	Clock frequency selection pin for digital filter (See Table 1) L : 192fs/384fs H : 384fs/768fs
⑪	DFCK	O	Clock output pin for digital filter 192fs/384fs、384fs/768fs
⑫	MODE	O	Broadcasting mode output L : Mode A reception H : Mode B reception
⑬	MODEB	O	Inverted output of broadcasting mode L : Mode B reception H : Mode A reception
⑭	LOCK	O	Sync state detection flag L : Asynchronous state H : Synchronous state
⑮	MUTEI	I	Muting signal input pin L : No muting H : All-channel muting
⑯	MUTEO	O	Muting flag output L : Muting condition not established H : Muting condition established Muting condition : Async : The 16th bit of the control code becomes "H" determined by majority logic : MUTEI outputs H-level OR
⑰	V_{SS1}	GND	Ground pin 1
⑱	MSOUT	O	Microcomputer IF : Serial data output pin
⑲	MCK	I	Microcomputer IF : Shift clock input pin
⑳	MSIN	I	Microcomputer IF : Serial data input pin
㉑	MLDB	I	Microcomputer IF : Serial data load pulse input pin
㉒	MCLK	O	2.048MHz master clock output pin
㉓	SDOUT	O	Output pin for stream data after error detection and correction by BCH (63/56) code Scramble decoder connection pin
㉔	SDIN	I	Input pin 1 for stream data after error detection and correction by BCH (63/56) code Scramble decoder connection pin
㉕	SDIN2	I	Input pin 2 for stream data after error detection and correction by BCH (63/56) code Scramble decoder connection pin
㉖	FSYNCB	O	Frame sync pulse output pin (low active) f = 1kHz
㉗	SDSEL	I	Selection pin for stream data after error detection and correction by BCH (63/56) code For connection of SKYPORT/COATEC double decder
㉘	V_{DD2}	Power	Power supply pin 2 (+5V)
㉙	DO1	O	Serial data output pin 1 for DAC : with MSB 1st and 2'S complement
㉚	DO2	O	Serial data output pin 2 for DAC : with MSB 1st and 2'S complement
㉛	WRDCK	O	Word clock output pin for DAC
㉜	LRCK	O	L−R clock output pin for DAC (Lch : H, Rch : L)
㉝	BITCK	O	Bit clock output pin for DAC

PIN DESCRIPTION (Continued)

Pin No.	Name	I/O	Function
㉞	LRCKB	O	L−R clock output pin for DAC (Lch : L, Rch : H)
㉟	DOTX	O	Digital audio interface output pin
㊱	TEST1	I	TEST mode setting pin 1 (H level in normal use)
㊲	TEST2	I	TEST mode setting pin 2 (H level in normal use)
㊳	TEST3	I	TEST mode setting pin 3 (H level in normal use)
㊴	V_{SS2}	GND	Ground pin 2
㊵	CKSEL	I	Main clock selection pin L : 18.432MHz H : 36.864MHz
㊶	CKIN	I	Main clock input pin (input with C connected)
㊷	RDBLER	O	Output pin for detection of range bit double error
㊸	MMFL	O	Output for detection of incoformity between range bits and upper bits of data in mode B
㊹	DBLER	O	Output for detection of BCH (63/56) double error

DIGITAL FILTER CLOCK SETTING METHOD

Main clock : 18.432MHz CKSEL(40pin) : L

DFCKS	fs	Mode A	DUTY	Mode B	DUTY
L	192	6.144MHz	1/2	9.216MHz	1/2
H	384	12.288MHz	1/3	18.432MHz	1/2

Main clock : 36.864MHz CKSEL(40pin) : H

DFCKS	fs	Mode A	DUTY	Mode B	DUTY
L	384	12.288MHz	1/2	18.432MHz	1/2
H	768	24.576MHz	1/3	36.864MHz	1/2

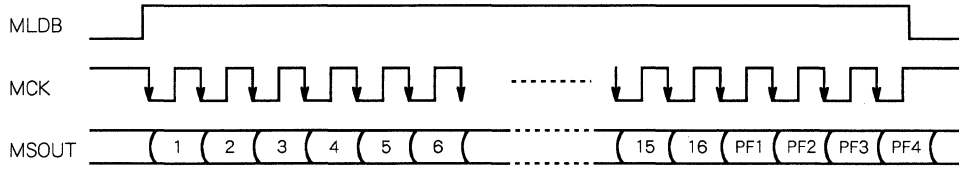
MICROCOMPUTER INTERFACE

1) Reading out control code and pay-TV flag

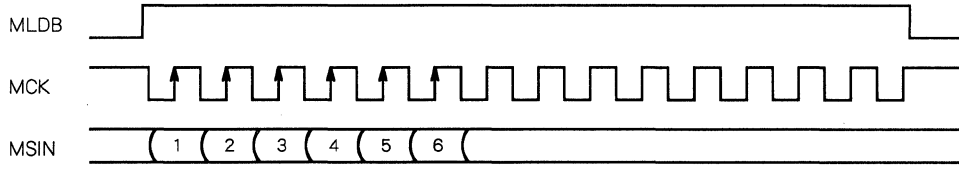
Control code is output from MSOUT in synchronization with the clock from MCK, and in the sequence of from bit 1 to bit 16. If the number of clock pulses inputted from MCK is 16, control code only is output : if 20, a pay-TV flag is output following control code.(1ch~4ch)

The 14th bit (master frame discrimination) of control code is not determined by majority logic.

The pay-TV flag output is the result of majority logic determined by the integration carried our for every 15 frames.



2) Writing voice output control data



3) Voice output control data

No.	Bit name	Function
1	FNCS	Selection of data after No.2 bit "H" : Control data for voice output data
2	TVAD	DO1 / DO2 ⇔ Switching between TV voice and additional voice "H" : DO1 → TV voice output DO2 → Additional voice output "L" : DO2 → TV voice output DO1 → Additional voice output Enabled only when in mode A broadcasting. In mode B, all outputs are TV voice.
3	TVMA	
4	TVSB	
5	ADMA	
6	ADSB	
1	FNCS	Selection of data after No. 2 bit "L" : Muting and DOTX output setting for each channel
2	MT1	"H" : Channel 1 muted
3	MT2	"H" : Channel 2 muted
4	MT3	"H" : Channel 3 muted
5	MT4	"H" : Channel 4 muted
6	DAIS	"L" : DO1 output signal is coded and output at DOTX. "H" : DO2 output signal is coded and output at DOTX.

TVMA	TVSB	Output
L	L	None
H	L	CH1 + CH1 (Main voice)
L	H	CH2 + CH2 (Sub voice)
H	H	CH1 + CH2 (Main + Sub)

In double-voice broadcasting, main-sub voice selection data acts on TV voice.

ADMA	ADSB	Output
L	L	None
H	L	CH3 + CH3 (Main voice)
L	H	CH4 + CH4 (Sub voice)
H	H	CH3 + CH4 (Main + Sub)

In double-voice broadcasting, main-sub voice selection data acts on additional voice.

DIGITAL AUDIO INTERFACE

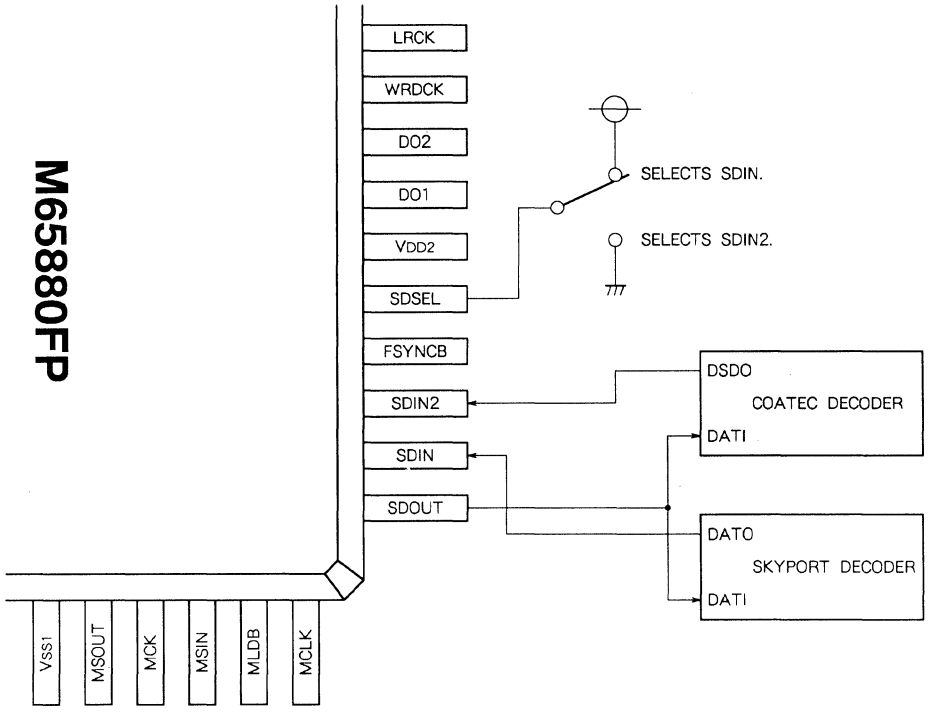
Channel status (C – bit)

Type II – form I (Home-use digital audio equipment applications)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
16	0	0	0	0	①				②				③		0	0
32	0	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	0
⇩																
⇩																
⇩																
⇩							ALL fixed to "0"									
⇩																
⇩																
⇩																
176	0	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	⇨	0

①Channel number
"0000" : No designation (fixed)
②Sample frequency
"1100" : 32kHz(Mode A)
"0100" : 48kHz(Mode B)
③Clock accuracy
"00" : Level II (fixed)

EXAMPLE OF CONNECTIONS WITH DOUBLE DECODER



M56790FP

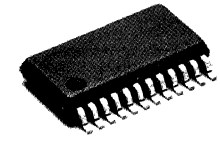
BS/CS QPSK SIGNAL DECODER

DESCRIPTION

The M56790FP is a bipolar IC developed for broadcasting satellite (BS/CS) receivers. It is used in voice signal decoder in BS/CS tuner and in TV and VCR with built-in BS/CS tuner. The IC decodes P and Q 2-bit digital data from signals that have passed a 5.73MHz B.P.F.

FEATURES

- Built-in main clock generator for PCM decoder
  Options from 36.864MHz and 18.432MHz
- Bit clock regenerator for PCM signal decoding
- Built-in LPF for COSTASLOOP
- AGC amp built-in
- Adjustment-free
- 5V single power supply



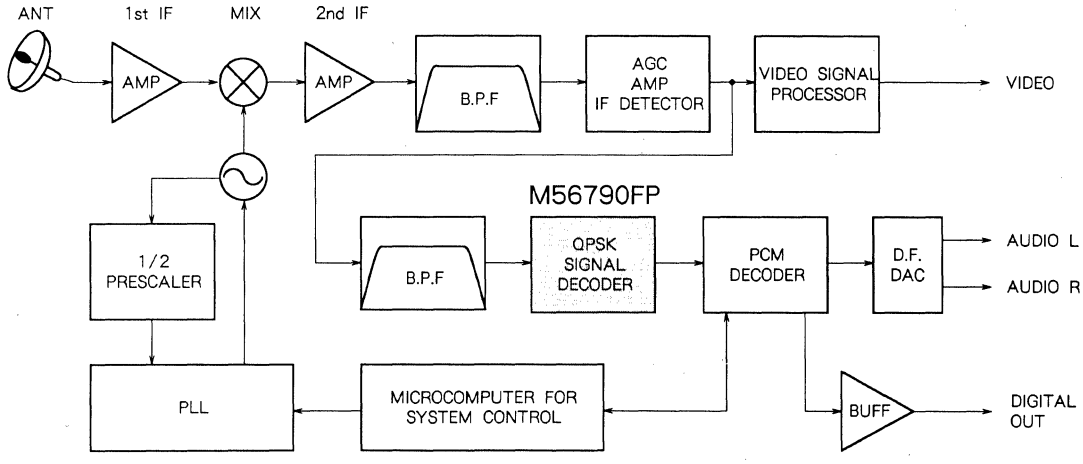
Outline 24P2Q-A

0.8mm pitch 300mil SSOP
(5.3mm × 10.1mm × 1.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 4.5~5.5V
Rated supply voltage ..... V_{CC} = 5.0V
Input signal voltage range ..... 50mV_{P-P}~350mV_{P-P}

SYSTEM CONFIGURATION



MITSUBISHI ELECTRIC

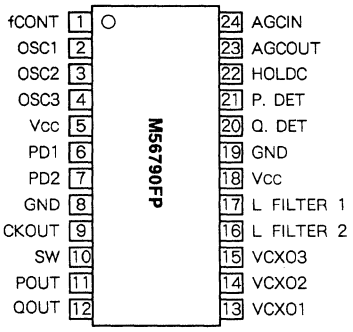
M56790FP

BS/CS QPSK SIGNAL DECODER

BUILT-IN FUNCTIONS

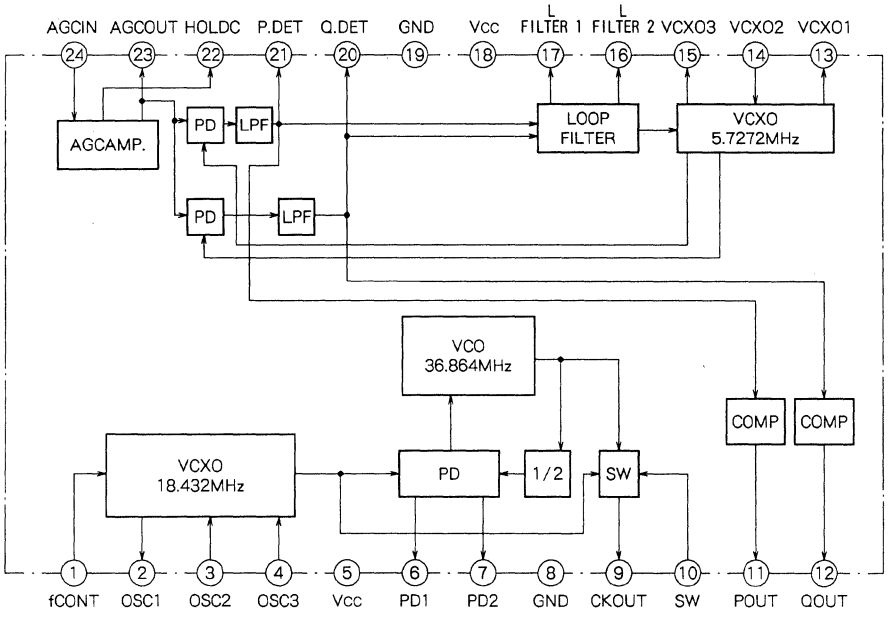
- QPSK signal decoding
- Main clock generation for PCM decoder (36.864MHz/18.432MHz)
- PLL for bit clock regeneration

PIN CONFIGURATION



Outline 24P2Q-A

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Name	Function
①	fCONT	Frequency control of clock output at pin ⑨
② ③ ④	OSC1 OSC2 OSC3	External connection pins of 18.432MHz VCXO Connect X-tal and the like
⑤	V_{CC}	Power supply to CK generator
⑥ ⑦	PD1 PD2	Outputs of phase detector detecting the 18.432MHz VCXO output and the 1/2 division of 36.864MHz VCO
⑧	GND	Ground pin of the CK generator
⑨	CKOUT	Clock output Outputs 18.432MHz or 36.864MHz clock pulses
⑩	SW	Clock output selector switch Selects from 18.432MHz and 36.864MHz clock pulses
⑪ ⑫	POUT QOUT	Comparator outputs after QPSK detection These signals enter the PCM decoder
⑬ ⑭ ⑮	VCXO1 VCXO2 VCXO3	External connection pins of 5.7272MHz VCXO Connect to X-tal, etc
⑯ ⑰	L FILTER 2 L FILTER 1	Loop filter monitor pins
⑱	V_{CC}	Power supply pin of the QPSK decoder
⑲	GND	Ground pin of the QPSK decoder
⑳ ㉑	Q.DET P.DET	QPSK detection outputs
㉒	HOLDC	Connection pin of AGCdet peak hold capacitance
㉓	AGCOUT	AGC output monitoring pin
㉔	AGCIN	AGC input pin Inputs the QPSK signals by linking capacitance

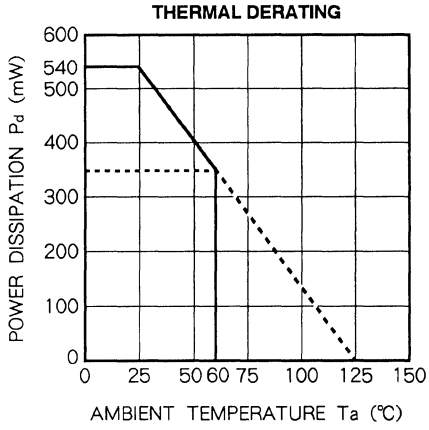
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	+ 6.0	V
I_{CC}	Circuit current	70	mA
P_d	Power dissipation	540	mW
K_θ	Thermal derating	5.4	mW/℃
T_{opr}	Operating temperature	− 10 ~ + 60	℃
T_{stg}	Storage temperature	− 40 ~ + 125	℃

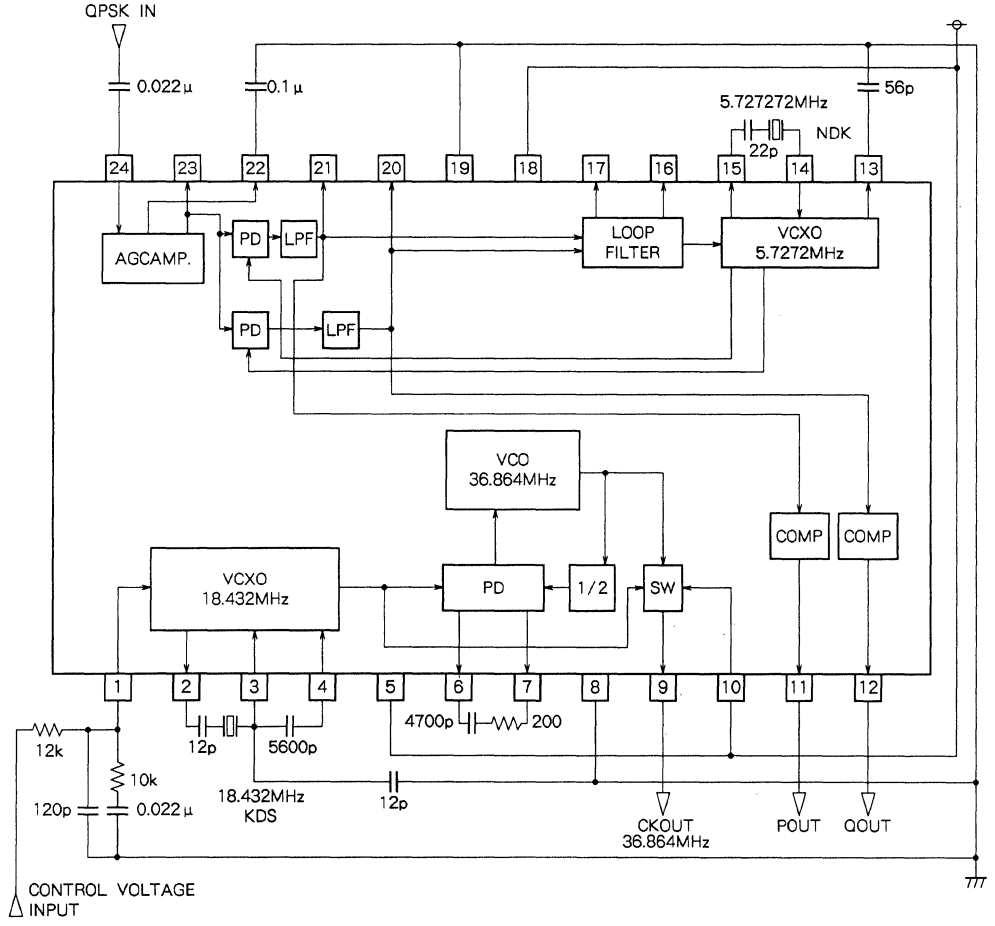
ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 5V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	No signal	32	42	53	mA
f_{cr}	QPSK capture range		+ 400	+ 700	−	Hz
			−	− 1200	− 800	
V_H	High level output voltage	POUT, QOUT	4.5	4.9	−	V
V_L	Low level output voltage	POUT, QOUT	−	0.1	0.5	V
t_r	Rise time	POUT, QOUT	−	100	200	ns
t_f	Fall time	POUT, QOUT	−	50	200	ns
f_f	Free-running frequency of clock output	Difference from 36.864MHz PIN1 = 2.5V	− 7.0	0	5.0	kHz
f_{1c}	Clock output control characteristic 1	Difference from f_f PIN1 = 2.4V	2.0	3.0	4.0	kHz
f_{2c}	Clock output control characteristic 2	Difference from f_f PIN1 = 1.0V	8.0	10.0	−	kHz
f_{3c}	Clock output control characteristic 3	Difference from f_f PIN1 = 4.0V	−	− 40.0	− 6.0	kHz
C_{out}	Clock output amplitude	C_L = 15pF	0.55	0.80	−	V_{P-P}
		C_L = 2pF	1.10	1.50	−	

TYPICAL CHARACTERISTICS



APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

OTHERS

M51141P

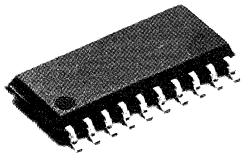
RECORDING AMPLIFIER, ALC CIRCUIT, PLAYBACK PREAMPLIFIER, VOLTAGE DETECTOR, ELECTRONIC SWITCH

DESCRIPTION

The M51141P is a recording and playback preamplifier for portable tape recorders. The IC's built-in preamplifiers for recording and playback, electronic switches for recording / playback selection, and ALC (automatic level controller), which all are necessary for a tape recorder, make it possible to construct a compact tape recorder of higher reliability at a low cost.

FEATURES

- Operates at low supply voltage ..... V_{CC} = 1.6Vmin. for operation
- Capable of controlling recording/playback selection by DC voltage
- Built-in supply voltage detector
- Wide ALC control range ..... 46dB (typ)
- Capable of direct connections of output pins of both recording and playback.



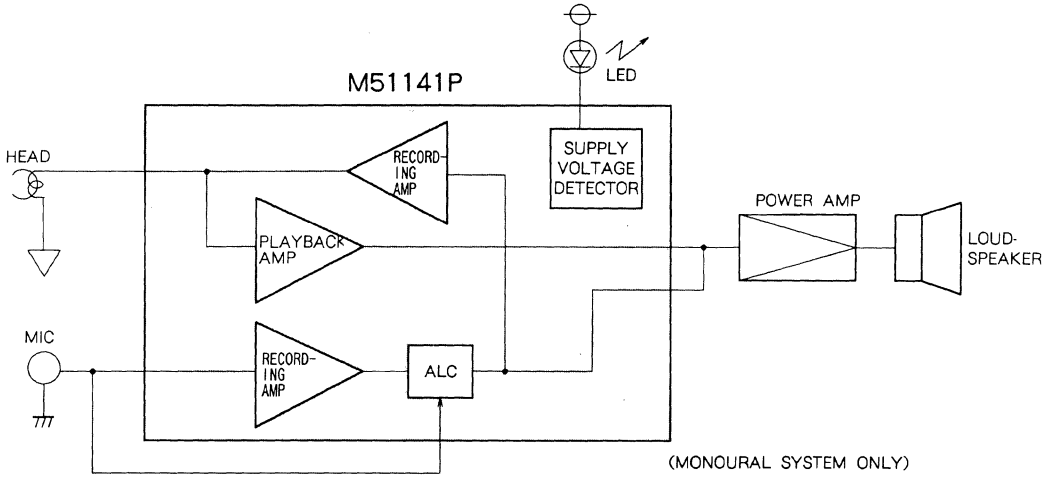
Outline 20P2

1.27mm pitch 200mil SOP
(5.3mm × 12.5mm × 1.75mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 2.0~6.0V
Rated supply voltage ..... V_{CC} = 3.0V

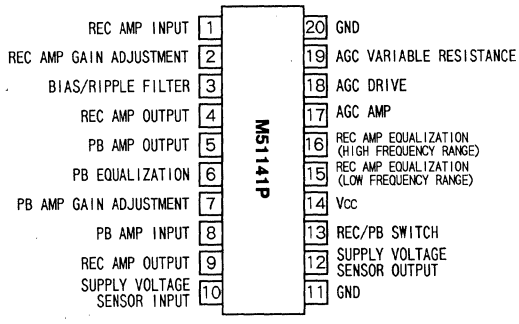
SYSTEM CONFIGURATION



M51141P

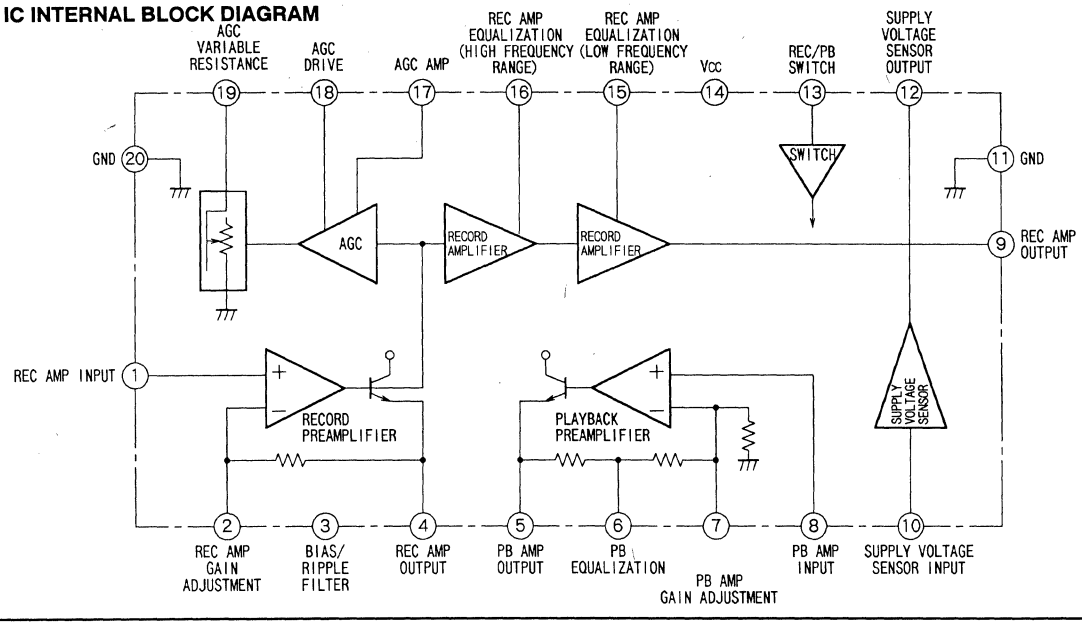
RECORDING AMPLIFIER, ALC CIRCUIT, PLAYBACK PREAMPLIFIER, VOLTAGE DETECTOR, ELECTRONIC SWITCH

PIN CONFIGURATION



Outline 20P2

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

M51141P

RECORDING AMPLIFIER, ALC CIRCUIT, PLAYBACK PREAMPLIFIER, VOLTAGE DETECTOR, ELECTRONIC SWITCH

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	7.5	V
I_{CC}	Circuit current	50	mA
P_d	Power dissipation	200	mW
K_θ	Thermal derating ($T_a \geqq 25$℃)	2	mW/℃
T_{opr}	Operating temperature	−20～+75	℃
T_{stg}	Storage temperature	−40～+125	℃

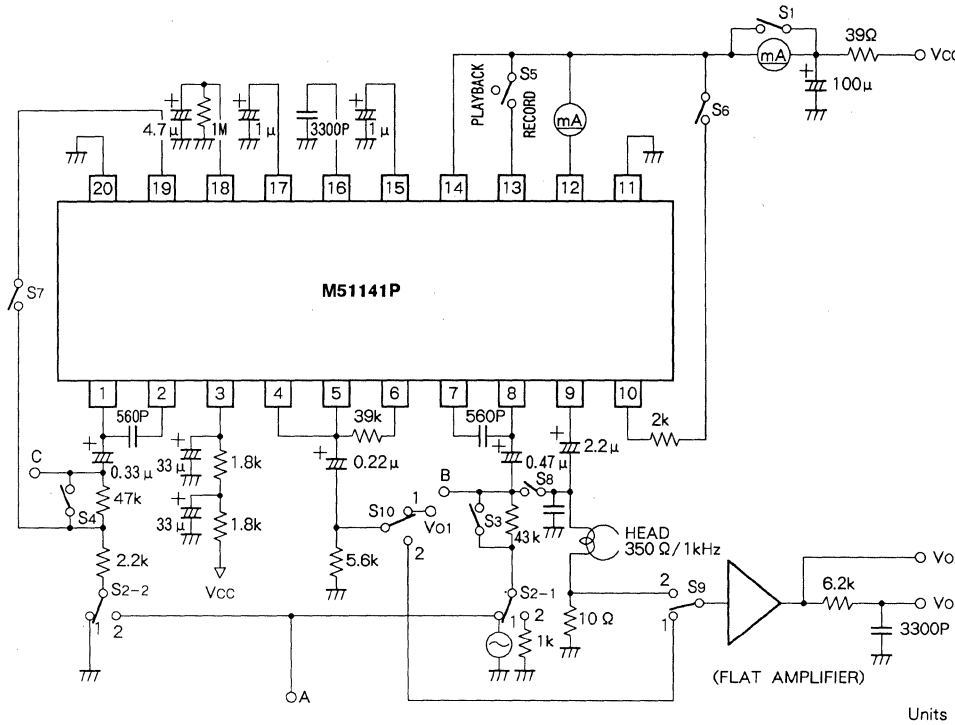
ELECTRICAL CHARACTERISTICS (Ta = 25℃)

	Symbol	Parameter	Vcc(V)	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
Playback preamplifier	I_{CCP}	Quiescent circuit current	3	R_g = 1kΩ, with supply voltage sensor not connected	2.5	4.0	8.0	mA
	G_{VP}	Voltage gain	3	39kΩ connected between pin ⑤ and pin ⑥ f = 1kHz, R_L = 5.6kΩ, V_O = 100mVrms	34	36	38	dB
	V_{OP}	Undistorted output voltage	3	f = 1kHz, R_L = 5.6kΩ THD = 3%	200	400	–	mVrms
			2		–	250	–	mVrms
	THD_P	Total harmonic distortion	3	f = 1kHz, R_L = 5.6kΩ, V_O = 100mVrms	–	0.2	1.0	%
	Z_{IP}	Input impedance	3	f = 1kHz	18	40	84	kΩ
	V_{NIP}	Input referred noise voltage	3	R_g = 1.0kΩ −3dB points at 1kHz and 10kHz, 6dB/octave rolloff	–	0.8	2.0	μVrms
Record preamplifier	I_{CCO}	Quiescent circuit current	3	Supply voltage sensor not connected	2.0	4.0	7.0	mA
	G_{VM}	Voltage gain	3	f = 1kHz, R_L = 5.6kΩ, V_O = 100mVrms	26	28	30	dB
	V_{OM}	Undistorted output voltage	3	f = 1kHz, R_L = 5.6kΩ THD = 3%	300	600	–	mVrms
			2		–	250	–	mVrms
	THD_M	Total harmonic distortion	3	f = 1kHz, R_L = 5.6kΩ, V_O = 100mVrms	–	0.3	1.0	%
	Z_{IM}	Input impedance	3	f = 1kHz, R_L = 5.6kΩ	20	48	95	kΩ
	V_{NIM}	Input-referred noise voltage	3	R_g = 2.2kΩ −3dB points at 1kHz and 10kHz, 6dB/octave rolloff	–	1.0	3.0	μVrms
	L_{OR}	Record signal leakage in playback mode	3	R_g = 0Ω, V_i = −30dBv, f = 1kHz Flat passband; ratio of record signal leakage to playback noise output	–	–	3	dB
Record amplifier	I_{OR}	Record output current	3	f = 1kHz, V_i = −72dBv; Head 350Ω at 1kHz; 1μF at pin ⑮; 3300pF at pin ⑯; 15000pF at head	50	80	130	μA
			2		–	75	–	μA
	I_{ORmax}	Maximum record output current	3	f = 1kHz, THD = 3%, Head 350Ω at 1kHz	300	500	–	μA
			2		200	400	–	μA
	S/N	Record amplifier S/N ratio	3	R_g = 2.2kΩ, V_i = −72dBV −3dB points at 1kHz and 10kHz, 6dB/octave rolloff	–	40	35	dB
AGC circuit		AGC range	3	R_g = 2.2kΩ	40	46	–	dB
		AGC level ratio	3	V_i = −50dBv/−70dBv, R_g = 2.2kΩ, f = 1kHz	–	–	3	dB
			3	V_i = −30dBv/−70dBv, R_g = 2.2kΩ, f = 1kHz	–	–	3	dB
	THD_{AGC}	Total harmonic distortion	3	V_i = −30dBv, R_g = 2.2kΩ, f = 1kHz	–	2	4	%
		AGC attenuation	2/3	V_i = −50dBv, R_g = 2.2kΩ, f = 1kHz	–	–	3	dB
Supply circuit current	$I_{L(ON)}$	Supply voltage sensor current	3	2kΩ between pin ⑩ and Vcc; Current flowing into pin ⑫	6	9	12	mA
	$I_{L(OFF)}$	Supply voltage sensor current	1.8	2kΩ between pin ⑩ and Vcc; Current flowing into pin ⑫	–	–	0.1	mA

M51141P

RECORDING AMPLIFIER, ALC CIRCUIT, PLAYBACK PREAMPLIFIER, VOLTAGE DETECTOR, ELECTRONIC SWITCH

TEST CIRCUIT



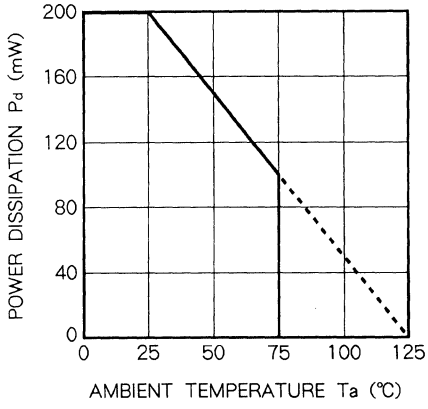
Units Resistance : Ω
Capacitance : F

TEST METHODS

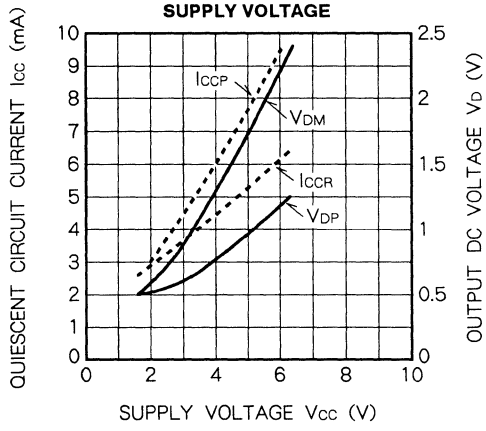
	Parameter	Switch conditions											Input signal measurement points					
		S_1	S_{2-1}	S_{2-2}	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	A	B	C	V_{O1}	V_{O2}	V_{O3}
Playback preamplifier	Quiescent circuit current	OFF	2	2	ON	ON	OFF	OFF	OFF	–	–	1						
	Voltage gain	ON	1	1	↑	↑	↑	↑	↑	OFF	1	↑	V_i			M		
	Undistorted voltage output	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑			↑		
	Input impedance	↑	↑	↑	OFF	↑	↑	↑	↑	↑	↑	↑	↑	M				
	Input-referred noise voltage	↑	2	2	ON	↑	↑	↑	↑	↑	↑	2						M
Record preamplifier	Quiescent circuit current	OFF	1	1	ON	ON	ON	OFF	OFF	OFF	1	1						
	Voltage gain	ON	2	2	↑	↑	↑	↑	↑	↑	↑	↑	V_i			M		
	Undistorted output voltage	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑			↑		
	Input impedance	↑	↑	↑	↑	OFF	↑	↑	↑	↑	↑	↑	↑		M			
	Input-referred noise voltage	↑	1	1	↑	ON	↑	↑	↑	↑	↑	2						M
Record amplifier	Record output current	ON	2	2	ON	ON	ON	OFF	OFF	ON	2	1	V_i				M	
	Maximum record output current	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑				↑	
	Recording S/N ratio	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑					M
AGC circuit	AGC range	ON	2	2	ON	ON	ON	OFF	ON	ON	2	1	V_i				M	
	AGC level ratio	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑				↑	
	Total harmonic distortion	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑				↑	
	Supply voltage sensor current	ON	–	–	ON	ON	ON	ON	–	–	2	1						

TYPICAL CHARACTERISTICS (Ta = 25℃, unless otherwise noted)

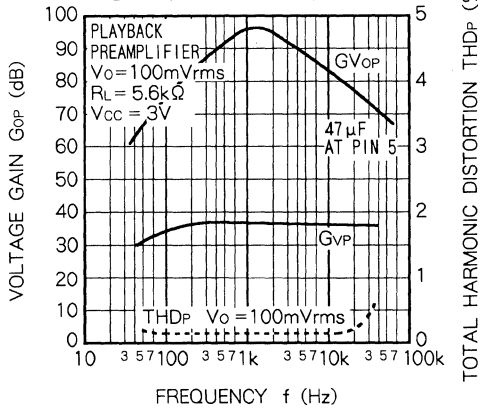
THERMAL DERATING (MAXIMUM RATING)



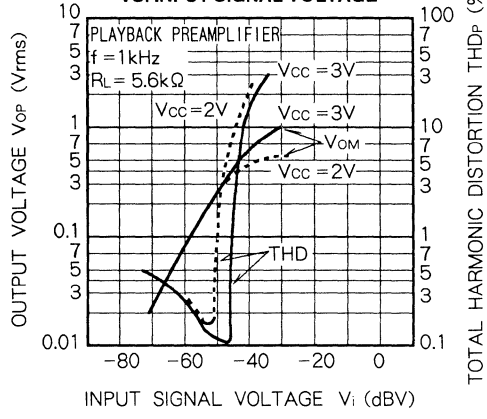
QUIESCENT CIRCUIT CURRENT OUTPUT DC VOLTAGE VS. SUPPLY VOLTAGE



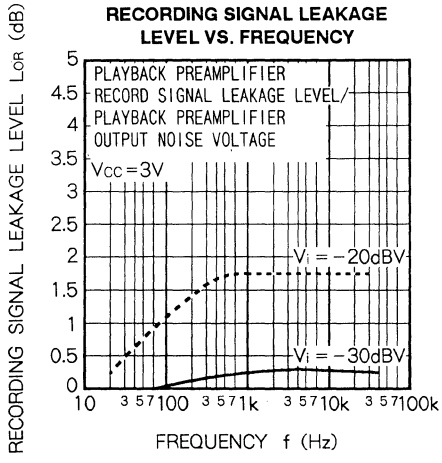
VOLTAGE GAIN,TOTAL HARMONIC DISTORTION VS. FREQUENCY



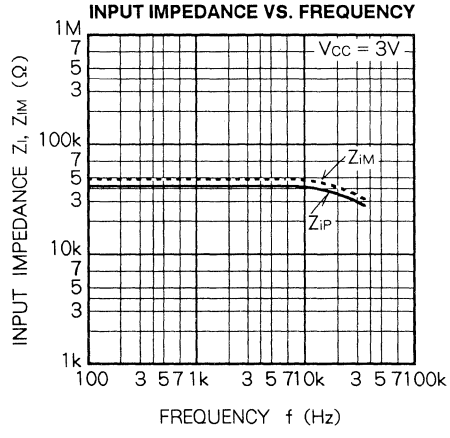
OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE



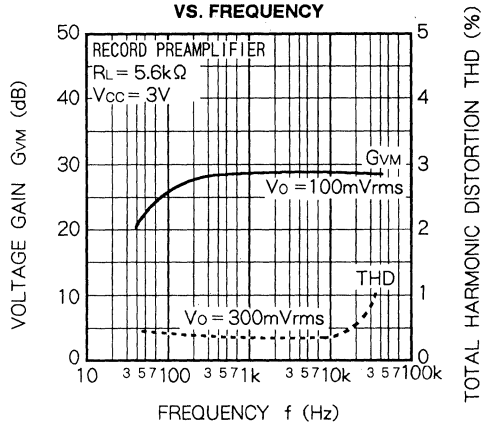
RECORDING SIGNAL LEAKAGE LEVEL VS. FREQUENCY



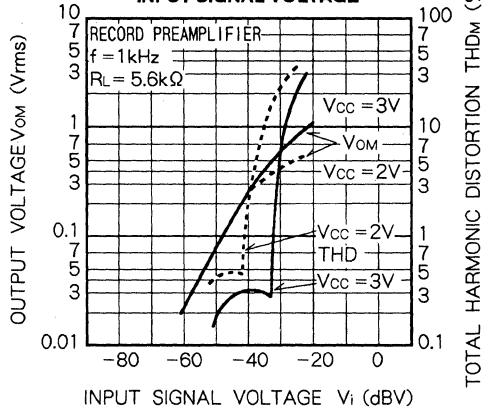
INPUT IMPEDANCE VS. FREQUENCY



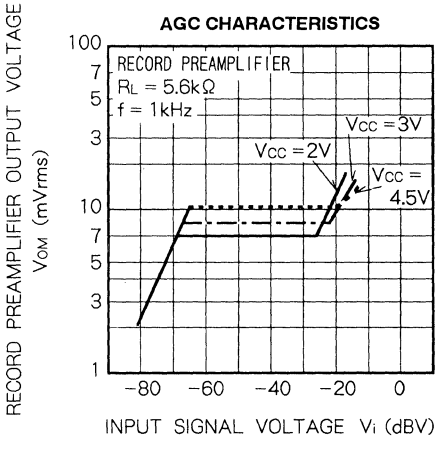
VOLTAGE GAIN, TOTAL HARMONIC DISTORTION VS. FREQUENCY



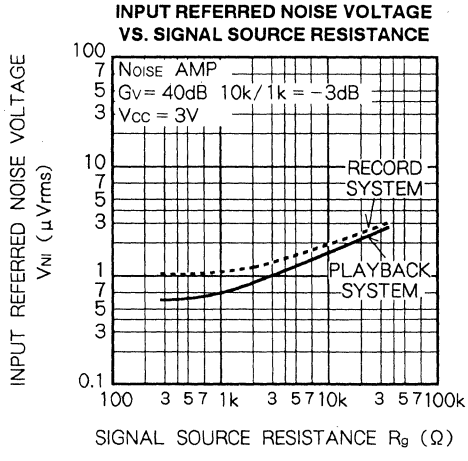
OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE



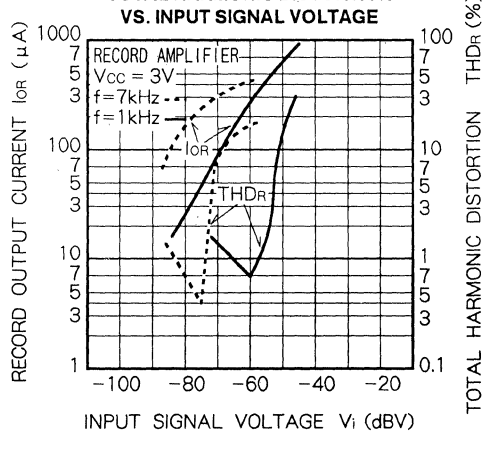
AGC CHARACTERISTICS



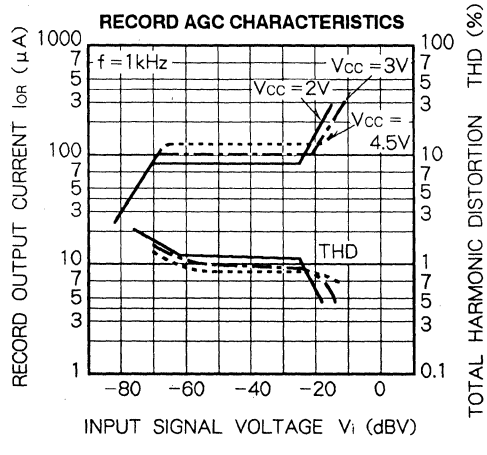
INPUT REFERRED NOISE VOLTAGE VS. SIGNAL SOURCE RESISTANCE



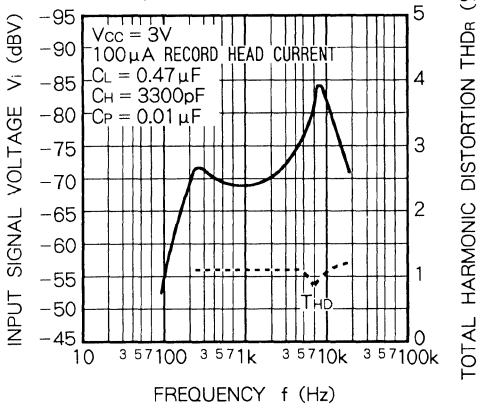
RECORD OUTPUT CURRENT, TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE



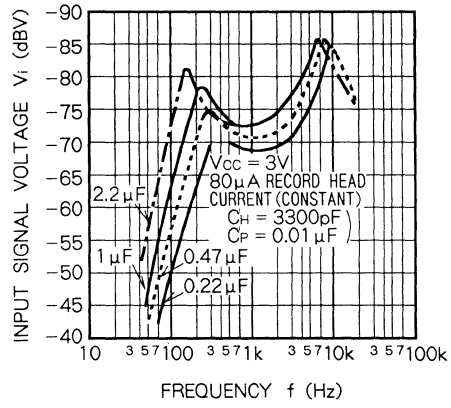
RECORD AGC CHARACTERISTICS



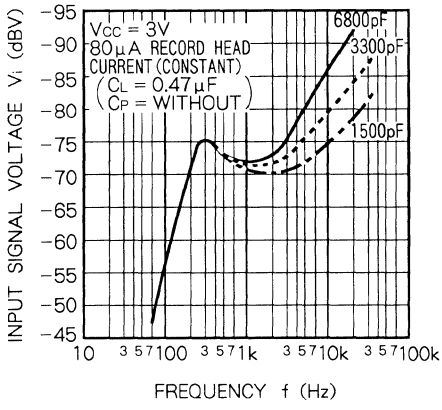
OVERALL RECORD FREQUENCY CHARACTERISTICS



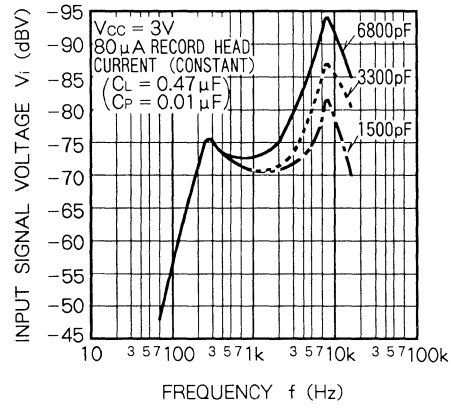
RECORD EQUALIZATION VS. fL CAPACITANCE(CL)



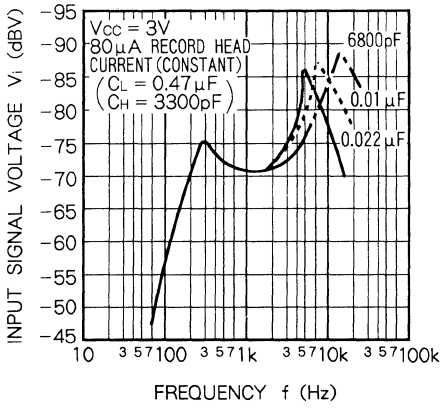
RECORD EQUALIZATION VS. fH CAPACITANCE(CH)



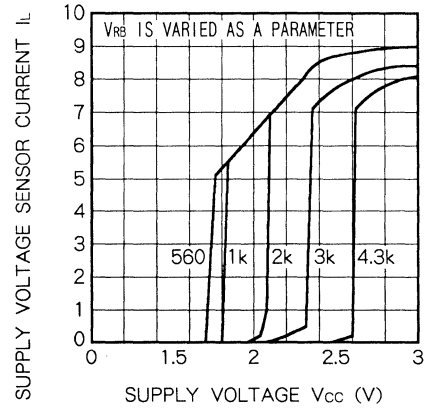
RECORD EQUALIZATION VS. fH CAPACITANCE (CH)



RECORD EQUALIZATION VS. CP (AT RECORD HEAD)

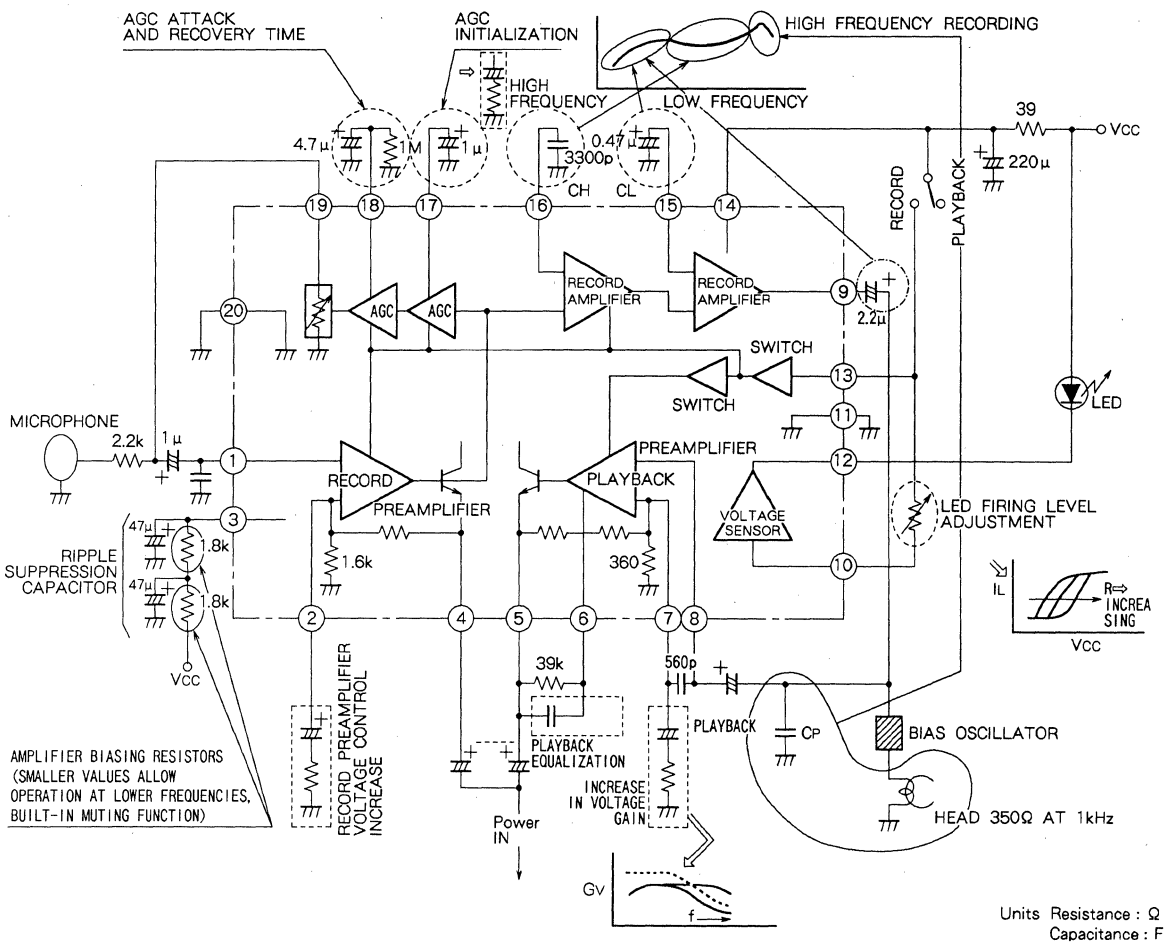


SUPPLY VOLTAGE SENSOR CHARACTERISTICS



APPLICATION EXAMPLE

Frequency response and voltage gain adjustments



Units Resistance : Ω
Capacitance : F

M51162P

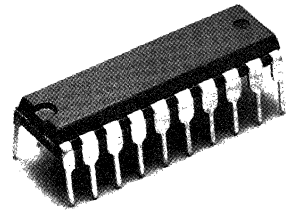
RECORDING/PLAYBACK PREAMPLIFIER FOR STEREO CASSETTE TAPE RECORDER

DESCRIPTION

The M51162P is a recording and playback preamplifier for stereo cassette tape recorders. The IC built-in recording/playback mode selector switches and 2 channels of preamplifiers with an ALC circuit. This configuration realizes compact designs and a system with good channel balance.

FEATURES

- Built-in microphone and equalizer amplifiers with electronic switches.
- Built-in line amplifiers with ALC.
- Low noise ..... 1 μVrms (R_g = 1k Ω)
- Low distortion ratio ..... 0.2% (V_O = 1Vrms)

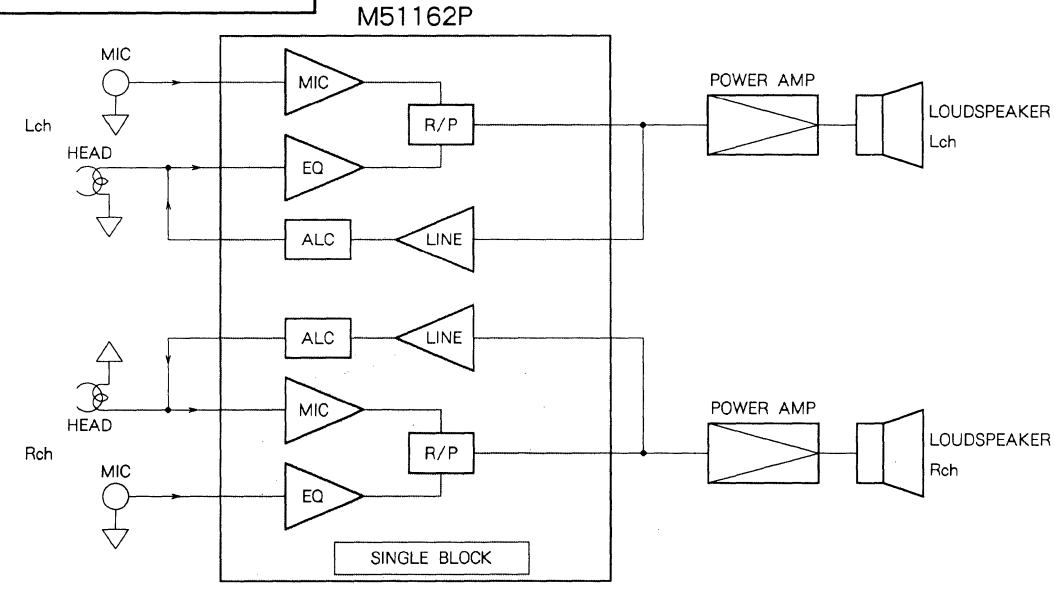


Outline 20P4
2.54mm pitch 300mil DIP
(6.3mm × 24.0mm × 3.3mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 3.5~12V
Rated supply voltage ..... V_{CC} = 9V

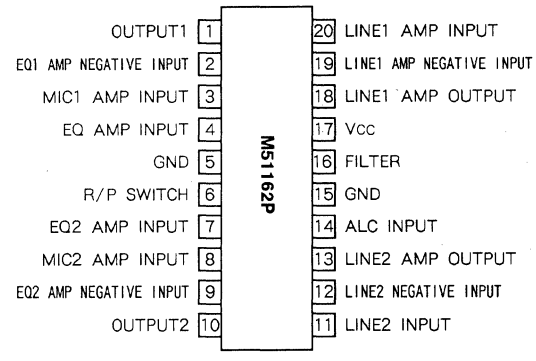
SYSTEM CONFIGURATION



M51162P

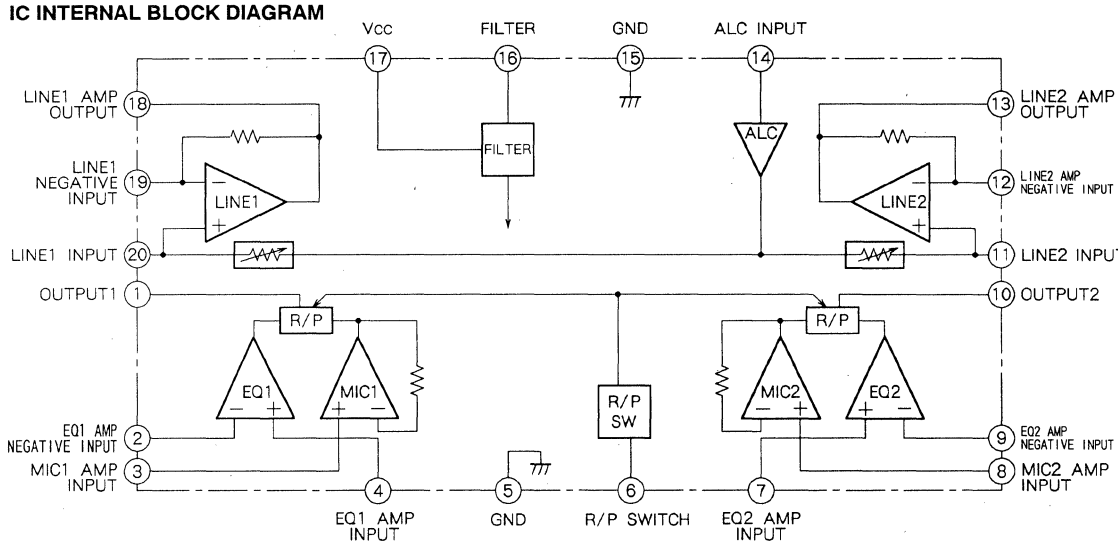
RECORDING/PLAYBACK PREAMPLIFIER FOR STEREO CASSETTE TAPE RECORDER

PIN CONFIGURATION



Outline 20P4

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

M51162P

RECORDING/PLAYBACK PREAMPLIFIER FOR STEREO CASSETTE TAPE RECORDER

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

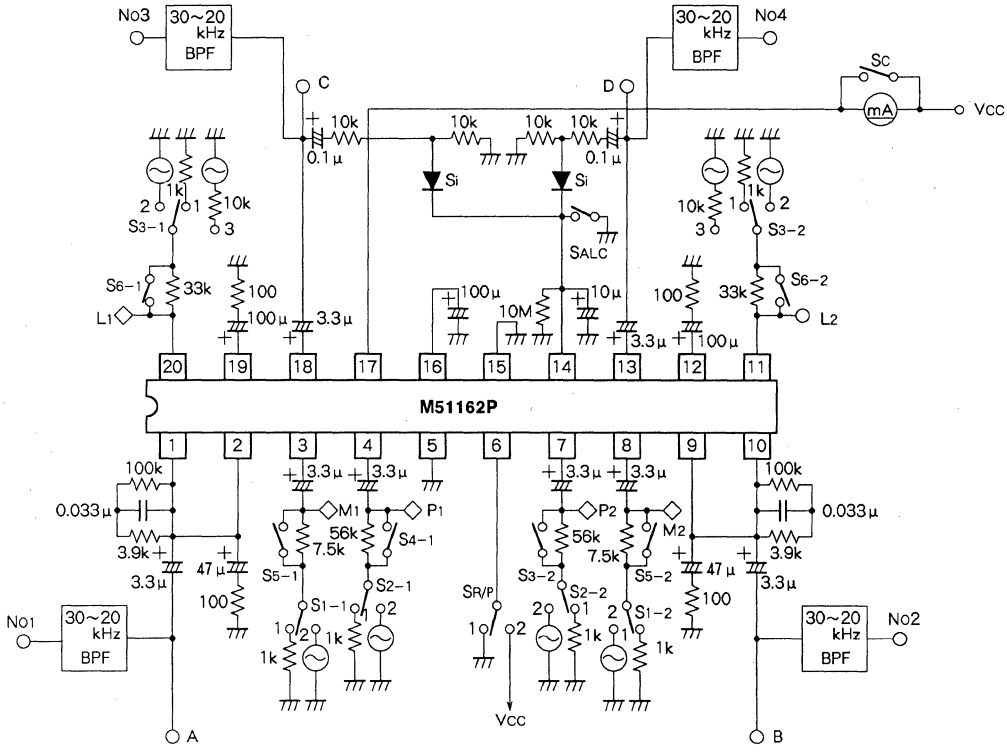
Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	18	V
I_{CC}	Circuit current	100	mA
P_d	Power dissipation	1000	mW
K_θ	Thermal derating ($T_a \geqq 25$℃)	10	mW/℃
T_{opr}	Operating temperature	−20 ~ + 75	℃
T_{stg}	Storage temperature	−40 ~ +125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 9V, f = 1kHz, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CCO}	Quiescent circuit current		Playback mode	5	10	15	mA
G_{VM1}	MIC amplifier CH-1	Voltage gain	V_{OM} = 1Vrms	23	24.5	26	dB
V_{OM1}		Maximum output voltage	THD = 3%	1.5	2.5	−	Vrms
THD_{M1}		Total harmonic distortion	V_{OM} = 1Vrms	−	0.2	0.5	%
Z_{iM1}		Input impedance	M_1 voltage when input = 10mVrms	5	7.5	10	kΩ
N_{iM1}		Equivalent input noise voltage	R_g = 1kΩ, 30~20kHz BPF	−	1	2	μVrms
G_{VP1}	EQ amplifier CH-1	Voltage gain	V_{OP} = 1Vrms	35	38	41	dB
V_{OP1}		Maximum output voltage	THD = 3%	1.5	2.5	−	Vrms
THD_{P1}		Total harmonic distortion	V_{OP} = 1Vrms	−	0.2	0.5	%
Z_{iP1}		Input impedance	P_1 voltage when input = 10mVrms	40	56	75	kΩ
N_{iP1}		Equivalent input noise voltage	R_g = 1kΩ, 30~20kHz BPF	−	1	2	μVrms
G_{VL1}	Line-recording amplifier CH-1	Voltage gain	V_{OL} = 1Vrms	37	40	43	dB
V_{OL1}		Maximum output voltage	THD = 3%	1.9	2.5	−	Vrms
THD_{L1}		Total harmonic distortion	V_{OL} = 1Vrms	−	0.2	0.5	%
Z_{iL1}		Input impedance	L_1 voltage when input = 10mVrms	20	33	45	kΩ
N_{iL1}		Equivalent input noise voltage	R_g = 1kΩ, 30~20kHz BPF	−	1	3	μVrms
ALC_A	ALC circuit	ALC range	From the point ALC is activated until output is 3dB up.	40	46	−	dB
ALC_{THD}		ALC distortion	Input distortion, from the point ALC is activated until input reaches + 20dB.	−	−	1.5	%
ALC_B		ALC balance	The difference in CH-1/CH-2 ALC output level, from the point ALC is activated until input reaches + 20dB.	−	−	3	dB

Note. Electrical characteristics for channel 2 are the same as channel 1.

TEST CIRCUIT



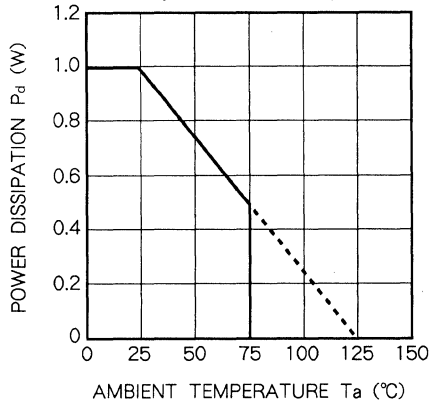
Units Resistance : Ω
Capacitance : F

TEST METHODS

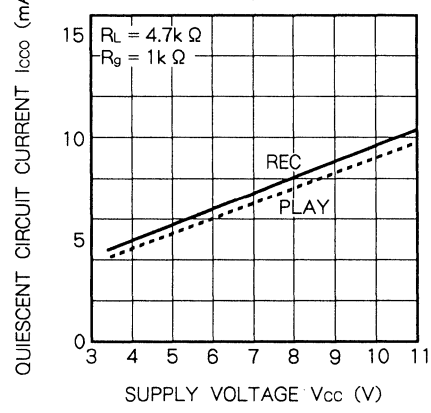
	Parameter	Switch conditions									Test point									
	Symbols	$S_{R/P}$	S_C	$S_{1-1,2}$	$S_{2-1,2}$	$S_{3-1,2}$	$S_{4-1,2}$	$S_{5-1,2}$	$S_{6-1,2}$	S_{ALC}	A	B	C	D	$P_{1,2}$	$M_{1,2}$	$L_{1,2}$	mA	$No_{1,2}$	$No_{3,4}$
	I_{CCO}	1	OFF	1	1	1	ON	ON	ON	OFF								○		
MIC amplifier	$G_{VM1,2}$	2	ON	2	1	1	ON	ON	ON	OFF	○	○								
	$V_{OM1,2}$	↑	↑	↑	↑	↑	↑	↑	↑	↑	○	○								
	$THD_{M1,2}$	↑	↑	↑	↑	↑	↑	↑	↑	↑	○	○								
	$Z_{iM1,2}$	↑	↑	↑	↑	↑	↑	OFF	↑	↑						○				
	$N_{iM1,2}$	↑	↑	↑	↑	↑	↑	ON	↑	↑									○	
EQ amplifier	$G_{VP1,2}$	1	ON	1	2	1	ON	ON	ON	OFF	○	○								
	$V_{OP1,2}$	↑	↑	↑	↑	↑	↑	↑	↑	↑	○	○								
	$THD_{P1,2}$	↑	↑	↑	↑	↑	↑	↑	↑	↑	○	○								
	$Z_{iP1,2}$	↑	↑	↑	↑	↑	OFF	↑	↑	↑					○					
	$N_{iP1,2}$	↑	↑	↑	↑	↑	ON	↑	↑	↑									○	
Line-recording amplifier	$G_{VL1,2}$	2	ON	2	1	2	ON	ON	ON	OFF			○	○						
	$V_{OL1,2}$	↑	↑	↑	↑	↑	↑	↑	↑	↑			○	○						
	$THD_{L1,2}$	↑	↑	↑	↑	↑	↑	↑	↑	↑			○	○						
	$Z_{iL1,2}$	↑	↑	↑	↑	↑	↑	↑	OFF	↑							○			
	$N_{iL1,2}$	↑	↑	↑	↑	↑	↑	↑	ON	↑										○
ALC circuit	ALC_A	2	ON	2	1	3	ON	ON	ON	ON			○	○						
	ALC_{THD}	↑	↑	↑	↑	↑	↑	↑	↑	↑			○	○						
	ALC_B	↑	↑	↑	↑	↑	↑	↑	↑	↑			○	○						

TYPICAL CHARACTERISTICS

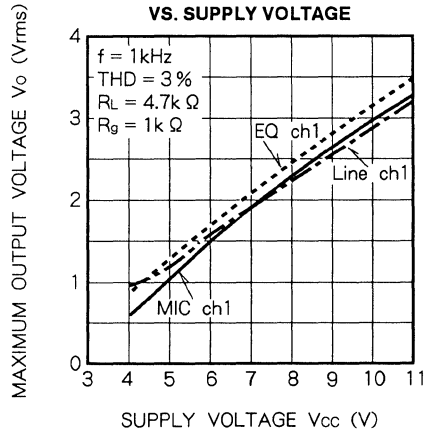
THERMAL DERATING
(MAXIMUM RATING)



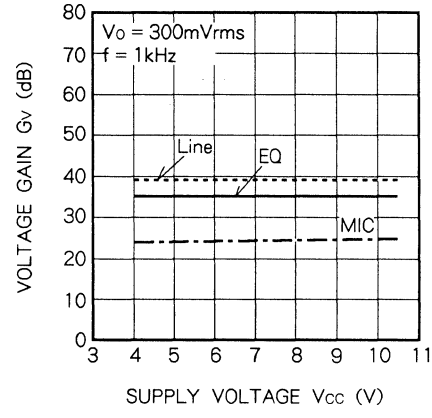
QUIESCENT CIRCUIT CURRENT
VS. SUPPLY VOLTAGE



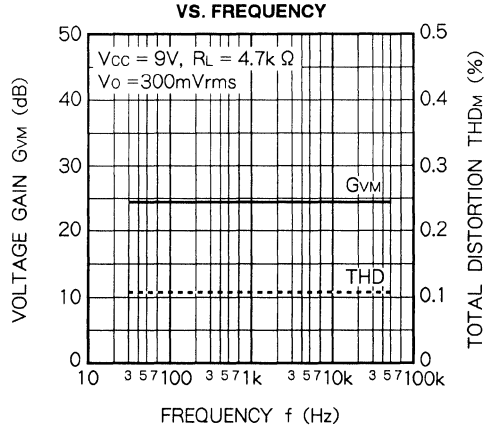
MAXIMUM OUTPUT VOLTAGE
VS. SUPPLY VOLTAGE



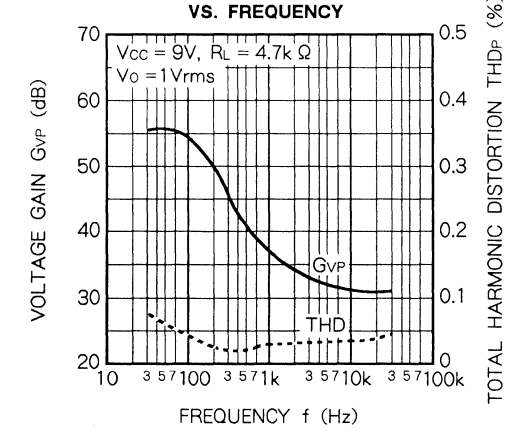
VOLTAGE GAIN VS. SUPPLY VOLTAGE



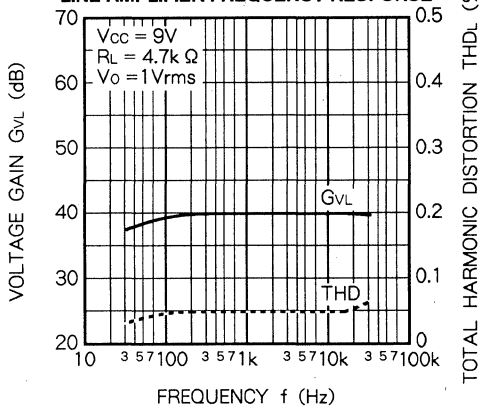
MIC AMPLIFIER VOLTAGE GAIN
VS. FREQUENCY



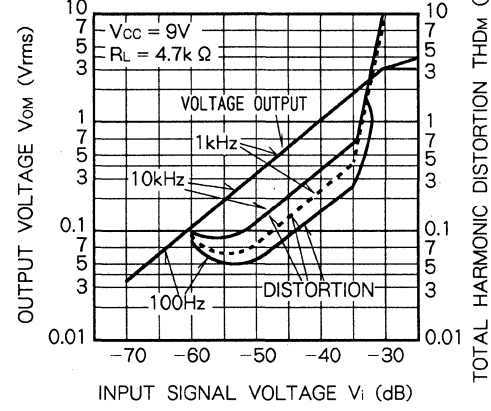
EQ AMPLIFIER VOLTAGE GAIN
VS. FREQUENCY



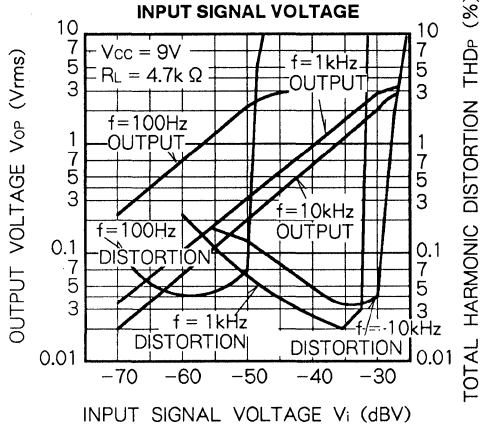
LINE AMPLIFIER FREQUENCY RESPONSE



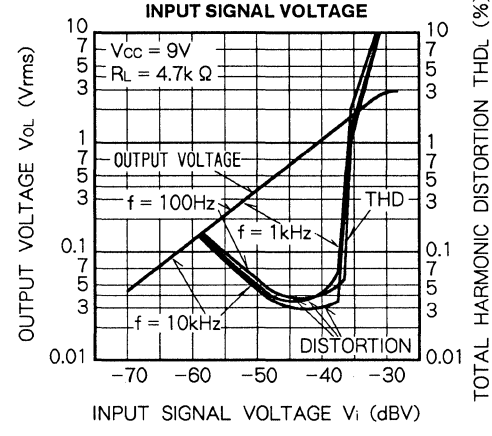
MIC OUTPUT VOLTAGE,TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE



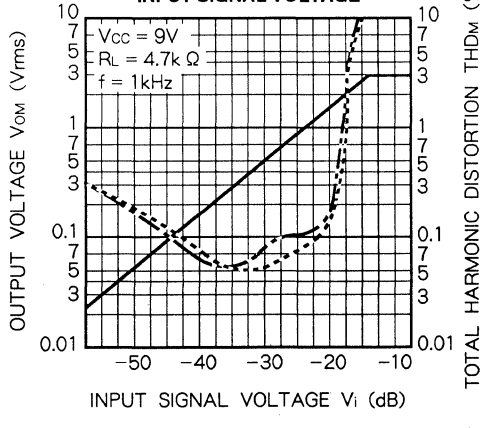
EQ OUTPUT VOLTAGE,TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE



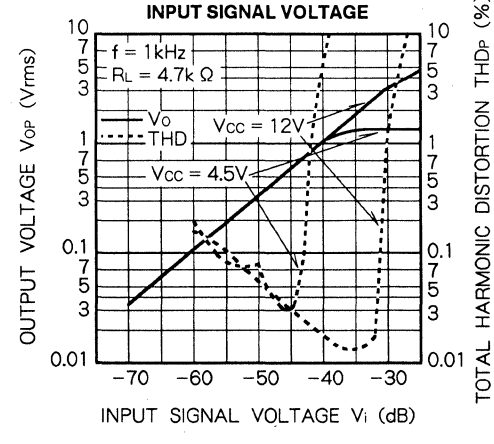
LINE OUTPUT VOLTAGE,TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE



MIC OUTPUT VOLTAGE,TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE



EQ OUTPUT VOLTAGE,TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE

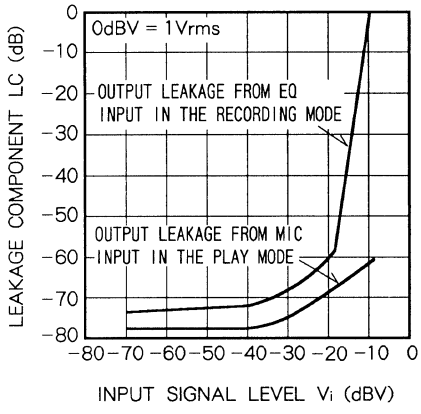


MITSUBISHI ELECTRIC

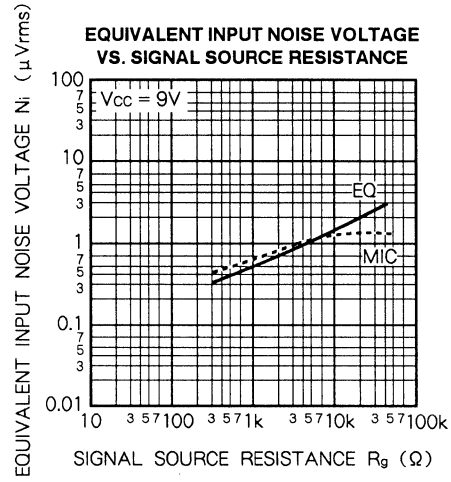
M51162P

RECORDING/PLAYBACK PREAMPLIFIER FOR STEREO CASSETTE TAPE RECORDER

LEAKAGE COMPONENTS VS. INPUT SIGNAL LEVEL CHARACTERISTICS



EQUIVALENT INPUT NOISE VOLTAGE VS. SIGNAL SOURCE RESISTANCE



FUNCTION AND TERMINAL DESCRIPTION

1. EQ amplifier

Normally connected to the input from the magnetic head, this amplifier functions to set equalization for proper playback of the tape being used.

- EQ amp input pins, pin ④ and pin ⑦. Input impedance, 56kΩ typ.
  Negative feedback pins, pin ② and pin ⑨.
  Output pins, pin ① and pin ⑩. (EQ/MIC output is switched by electronic switch.)

2. MIC amplifier

Functions to amplify the input signal from the microphone connection. The circuitry of this amplifier is the same as the EQ amp, and gain is fixed at 24dB.

- MIC amp input pins, pin ③ and pin ⑧. Input impedance 7.5kΩ typ.
  Output pins, pin ① and pin ⑩.

3. Line amplifier

Functions to further amplify the signal received from the EQ, MIC and other amplifiers. Can also be used as the recording amplifier.

- Line amp input pins, pin ⑪ and pin ⑳. Input impedance 33kΩ typ.
  Negative feedback pins, pin ⑫ and pin ⑲
  Output pins, pin ⑬ and pin ⑱

4. ALC circuit

Functions to automatically control the level of the input signal by using a built-in variable resistor.

- ALC circuit input pin, pin ⑭
  Variable resistor pins, pin ⑪ and pin ⑳
  In the playback mode, ALC operations are automatically disabled.

5. R/P switch

Switching between the recording and playback mode is accomplished through a DC voltage signal.

- R/P switch control pin, pin ⑥
  Recording mode : Control voltage, more than 2.2V, more than 100μA current.

Playback mode : Grounded

6. Filter

pin ⑯

7. Power supply

pin ⑰

8. Ground

pin ⑤ and ⑮

M51166P

QUAD RECORDING/PLAYBACK PREAMPLIFIER WITH ALC PEAK DETECTOR FOR DUAL CASSETTE PLAYER

DESCRIPTION

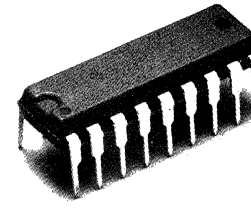
The M51166P is an IC for radio double cassette tape players.

It has a built-in 4 low-noise preamplifiers and 2 channels of ALC.

The built-in peamplifiers are of direct input type. The IC also contains ALC peak detectors and ALC. This configuration makes it possible to construct a recording/playback system with few external parts.

FEATURES

- Four low-noise dual preamplifiers built-in
- High voltage gain 89dB
- Built-in ALC peak detectors
- Easy-to-mount pin configuration grouped into input pins (①~⑨) and output pins (⑩~⑱)



Outline 18P4

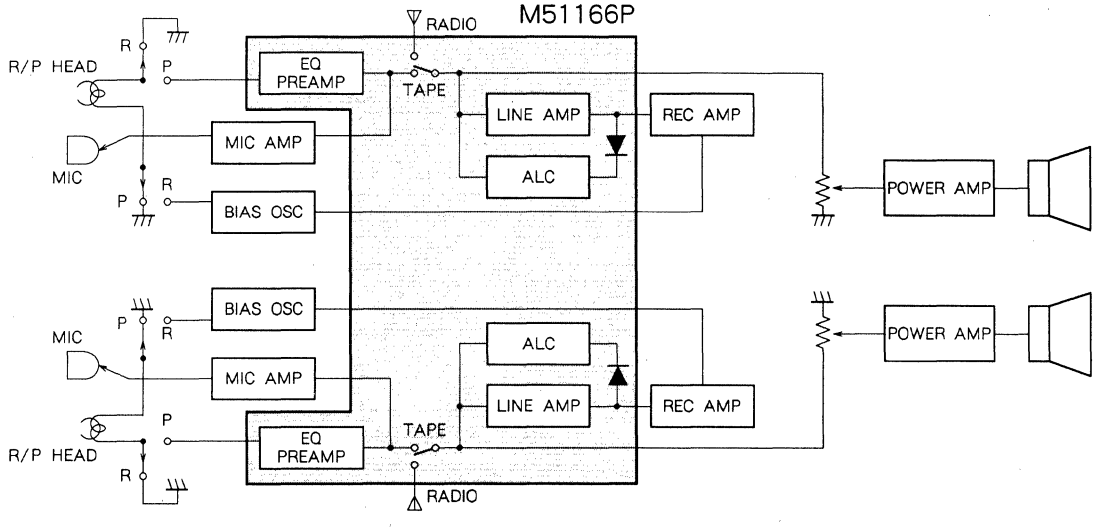
2.54mm pitch 300mil DIP
(6.3mm × 24.0mm × 3.3mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 5~12V

Rated supply voltage ..... V_{CC} = 9V

SYSTEM CONFIGURATION

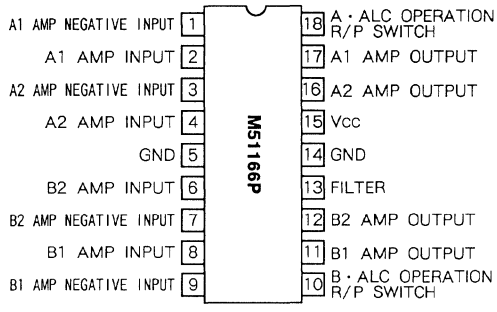


MITSUBISHI ELECTRIC

M51166P

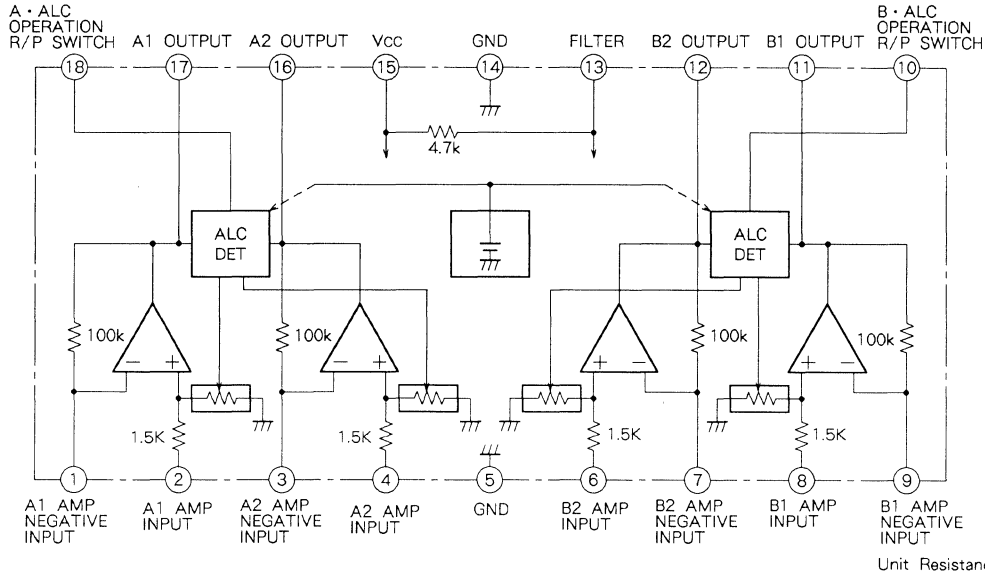
QUAD RECORDING/PLAYBACK PREAMPLIFIER WITH ALC PEAK DETECTOR FOR DUAL CASSETTE PLAYER

PIN CONFIGURATION



Outline 18P4

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

M51166P

QUAD RECORDING/PLAYBACK PREAMPLIFIER WITH ALC PEAK DETECTOR FOR DUAL CASSETTE PLAYER

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

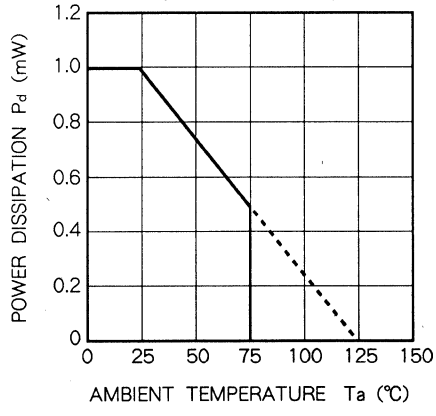
Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Quiescent	15	V
I_{CC}	Circuit current		50	mA
P_d	Power dissipation		1000	mW
K_θ	Thermal derating	$T_a \geqq 25$℃	10	mW/℃
T_{opr}	Operating temperature		−20～+75	℃
T_{stg}	Storage temperature		−40～+125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 9V, R_L = 10kΩ, f = 1kHz, unless otherwise noted)

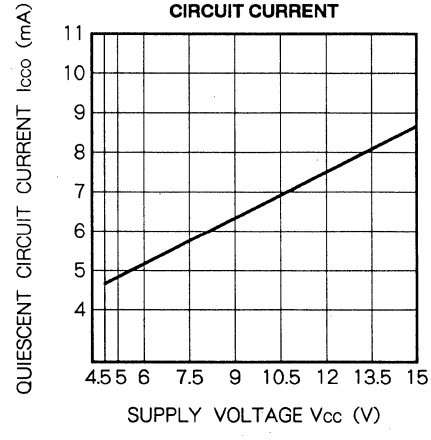
Symbol		Parameter	Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CCO}		Quiescent circuit current		−	6	−	mA
G_{VO}	Amplifiers	Open loop voltage gain	V_O = 1Vrms, C_{NF} = 100 μF	−	89	−	dB
G_{VC}	Amplifiers	Closed loop voltage gain	V_O = 1Vrms, R_{NF} = 240Ω	50	53	55	dB
THD	Amplifiers	Total harmonic distortion	V_O = 1Vrms, R_{NF} = 240Ω	−	0.1	0.6	%
V_O	Amplifiers	Maximum output voltage	THD = 3%	2.0	2.5	−	Vrms
N_i	Amplifiers	Input-referred noise voltage	R_g = 0Ω, BPF (20～20kHz − 3dB)	−	1.5	2.5	μVrms
ALC_A	ALC circulls	ALC range	Input voltage range from start of ALC operation with an output voltage of Vi=−72dBV to the point where the output voltage is 3dB higher. Re=12Ω	40	46	−	dB
ALC_B	ALC circulls	ALC range		0.8	1.05	1.25	Vrms
ALC_{THD}	ALC circulls	ALC distortion	Output voltage and distortion at an input voltage signal of V_i = − 50dBV. R_e = 24Ω	−	0.5	2	%
ALC_1	ALC circulls	ALC output voltage		−	0	2	dB
ALC_2	ALC circulls	ALC balance					

TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)

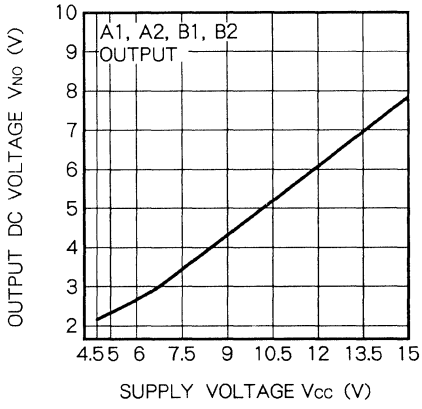


SUPPLY VOLTAGE VS. QUIESCENT CIRCUIT CURRENT

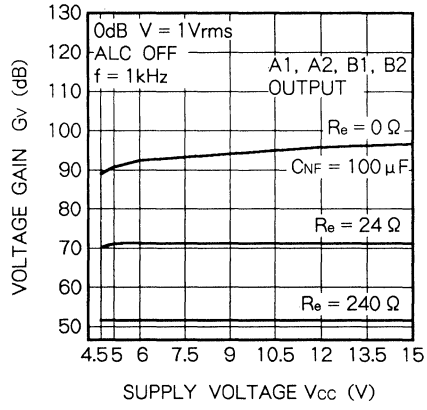


MITSUBISHI ELECTRIC

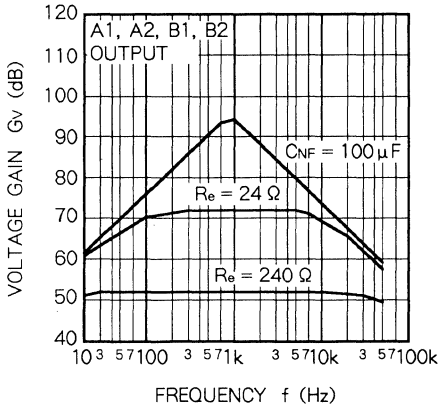
OUTPUT DC VOLTAGE VS. SUPPLY VOLTAGE



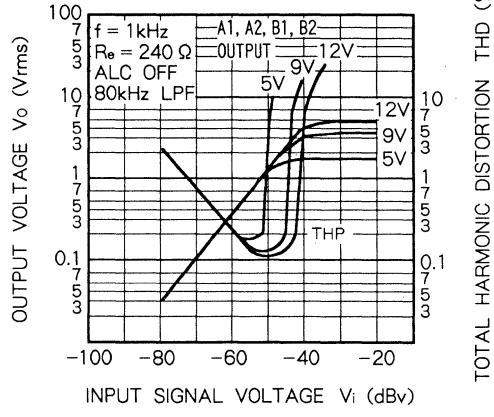
VOLTAGE GAIN VS. SUPPLY VOLTAGE



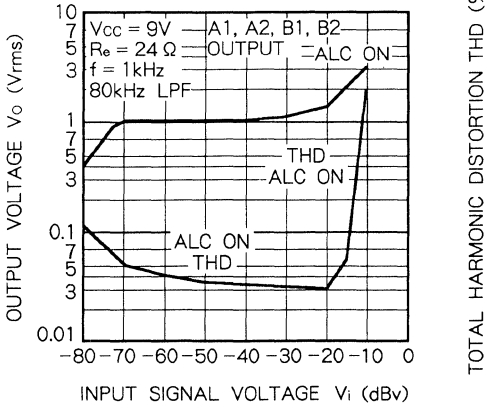
VOLTAGE GAIN VS. FREQUENCY



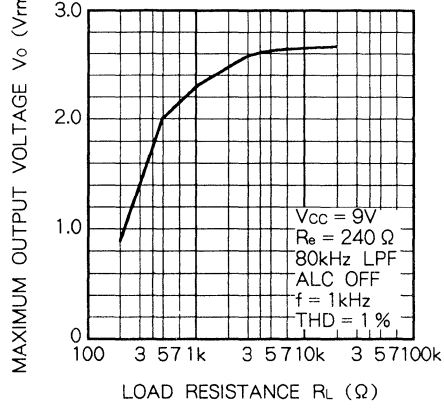
OUTPUT VOLTAGE VS. INPUT SIGNAL VOLTAGE



OUTPUT VOLTAGE VS. INPUT SIGNAL VOLTAGE



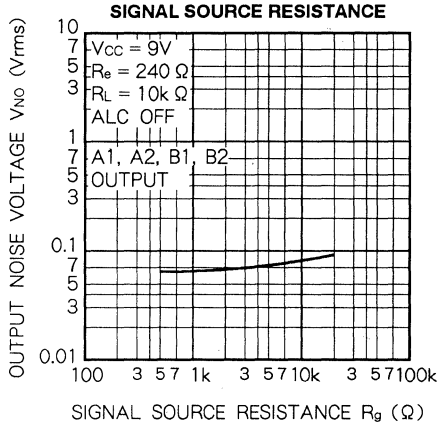
MAXIMUM OUTPUT VOLTAGE VS. LOAD RESISTANCE



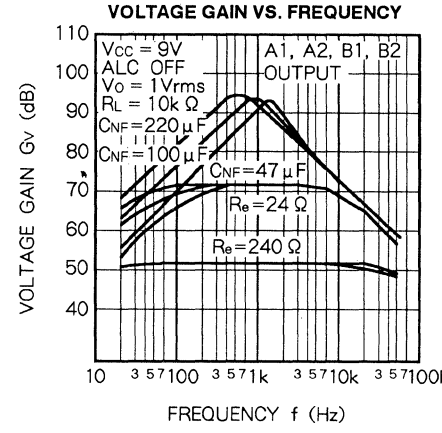
M51166P

QUAD RECORDING/PLAYBACK PREAMPLIFIER WITH ALC PEAK DETECTOR FOR DUAL CASSETTE PLAYER

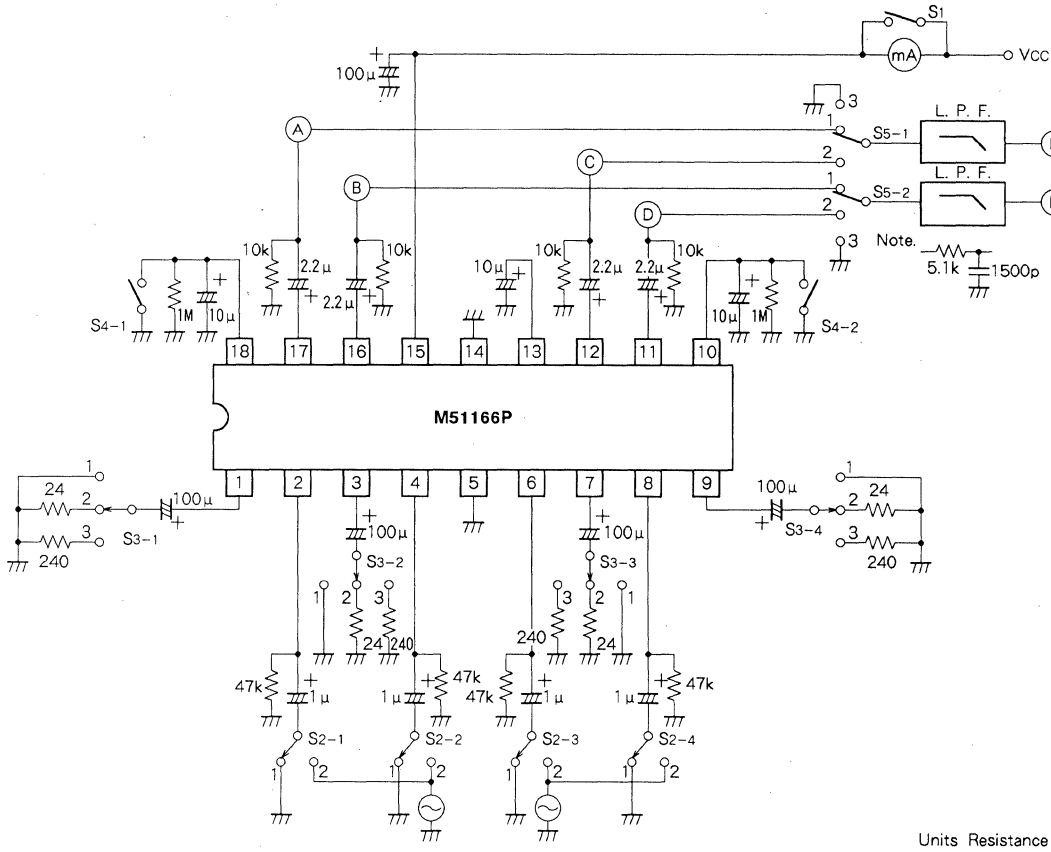
OUTPUT NOISE VOLTAGE VS. SIGNAL SOURCE RESISTANCE



VOLTAGE GAIN VS. FREQUENCY



TEST CIRCUIT



Units Resistance : Ω
Capacitance : F

MITSUBISHI ELECTRIC

M51166P

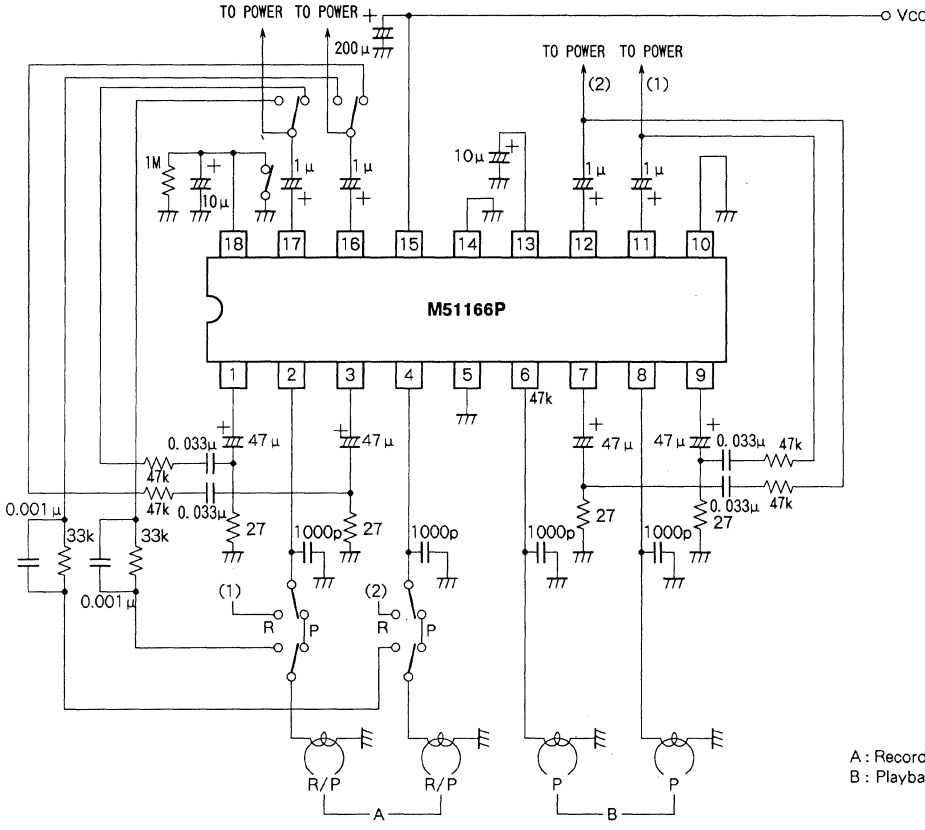
QUAD RECORDING/PLAYBACK PREAMPLIFIER WITH ALC PEAK DETECTOR FOR DUAL CASSETTE PLAYER

TEST METHODS (T_a = 25℃, V_{CC} = 9V, R_L = 10kΩ, f = 1kHz, unless otherwise noted)

Symbol	Test conditions	Switching conditions					Measure point
		S_1	$S_{2\text{-}1,2,3,4}$	$S_{3\text{-}1,2,3,4}$	$S_{4-1,2}$	$S_{5-1,2}$	
I_{CCO}		OFF	1	3	ON	3	mA
G_{VO}	V_i = − 80dBV	ON	2	1	↑	↑	A,B,C,D
G_{VC}	V_i = − 52dBV (2.5mVrms)	↑	↑	3	↑	↑	↑
THD	V_i = − 52dBV (2.5mVrms)	↑	↑	↑	↑	↑	↑
V_O	THD = 3%	↑	↑	↑	↑	↑	↑
N_i	20Hz~20kHz BPF	↑	1	3	ON	1/2	E,F
ALC_A	R_e = 240Ω	↑	2	2	OFF	3	A/B,C/D
ALC_O ALC_{THD}	Output voltage and distortion V_i = − 50dBV	↑	↑	↑	↑	↑	↑
ALC_B	Output voltage ratio V_i = − 50dBV	↑	↑	↑	↑	↑	A/B,C/D

Note 2 : ALC balance (ALC_B) is measure about output voltage ratio for each A side, B side.

APPLICATION EXAMPLE



A : Recording/Playback
B : Playback

Units Resistance : Ω
Capacitance : F

M51167AP,AFP

SINGLE CHIP PREAMPLIFIER FOR DUAL CASSETTE RECORDER

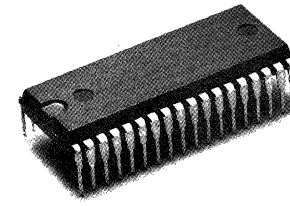
DESCRIPTION

The M51167 is an IC designed for radio CD/cassette tape players.

The IC, in addition to recording and playback preamplifiers (2 ch) for dual cassette, has equalizer selector, program selector, and ALC (automatic level controller) and is, with a single chip, capable of processing audio signals of cassette deck.

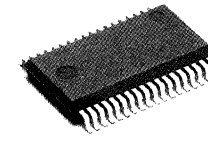
FEATURES

- Built-in electronic switch for double cassette.
- Built-in equalizer switch for both modes.
- 2 channels of high-gain, low-noise equalizer low noise EQ amplifier ..... 1.3μVrms (typ)
- Two built-in Rec amplifier with ALC circuit for noise reduction system.
- Built-in filter circuits for prevention of malfunctioning caused by tape pop up noise at music blank.
- Capable of setting timimg for music blank by means of external CR combination.



Outline 36P4E(AP)

1.778mm pitch 500mil SDIP
(11.0mm × 31.5mm × 3.8mm)



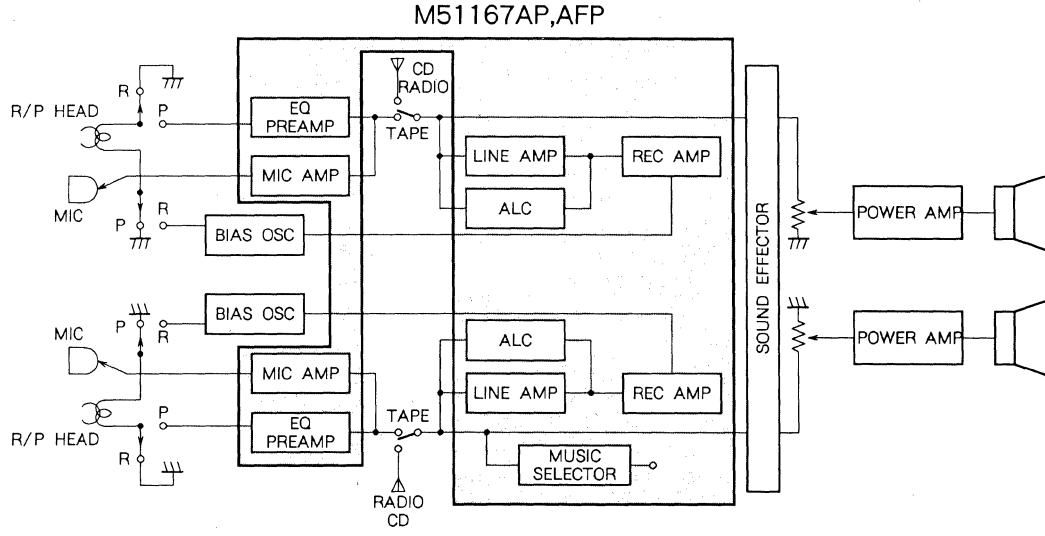
Outline 36P2R-A(AFP)

0.8mm pitch 450mil SSOP
(8.4mm × 15.0mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 5.5~12V
Rated supply voltage ..... V_{CC} = 9V

SYSTEM CONFIGURATION

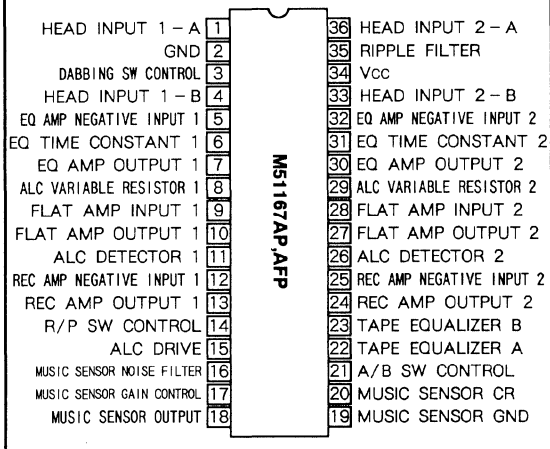


MITSUBISHI ELECTRIC

M51167AP,AFP

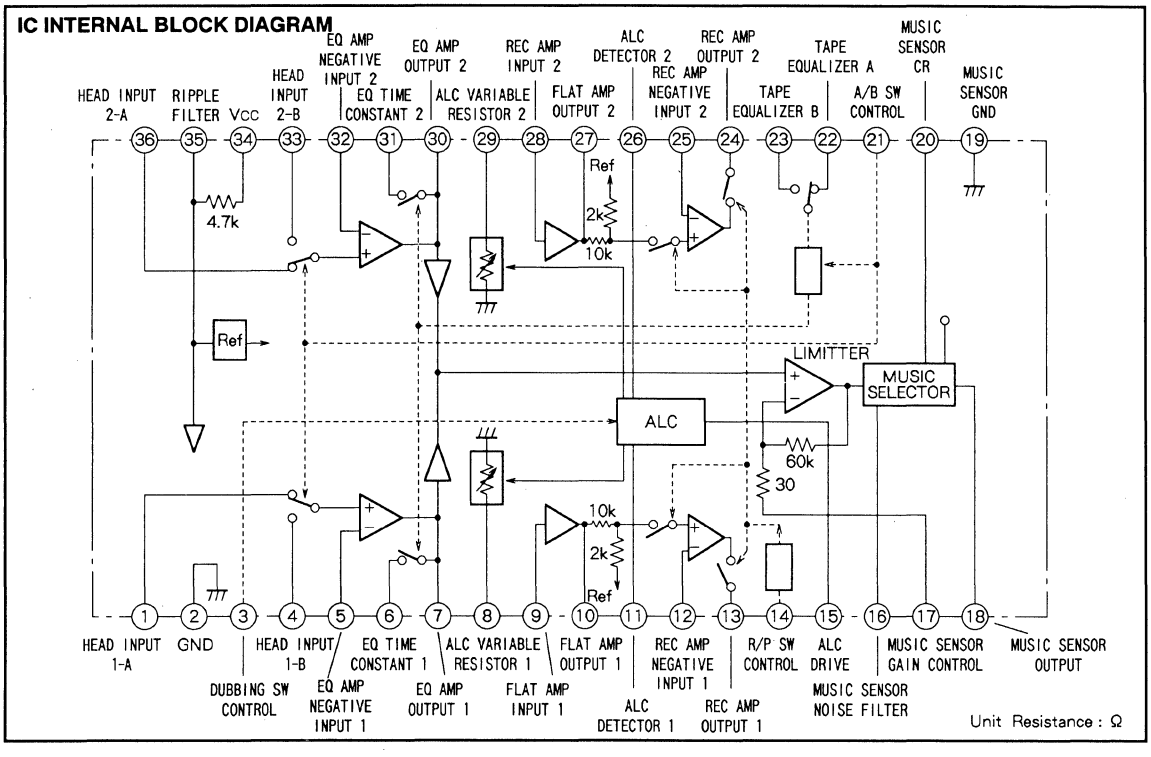
SINGLE CHIP PREAMPLIFIER FOR DUAL CASSETTE RECORDER

PIN CONFIGURATION



Outline 36P4E(AP)
36P2R-A(AFP)

IC INTERNAL BLOCK DIAGRAM



M51167AP,AFP

SINGLE CHIP PREAMPLIFIER FOR DUAL CASSETTE RECORDER

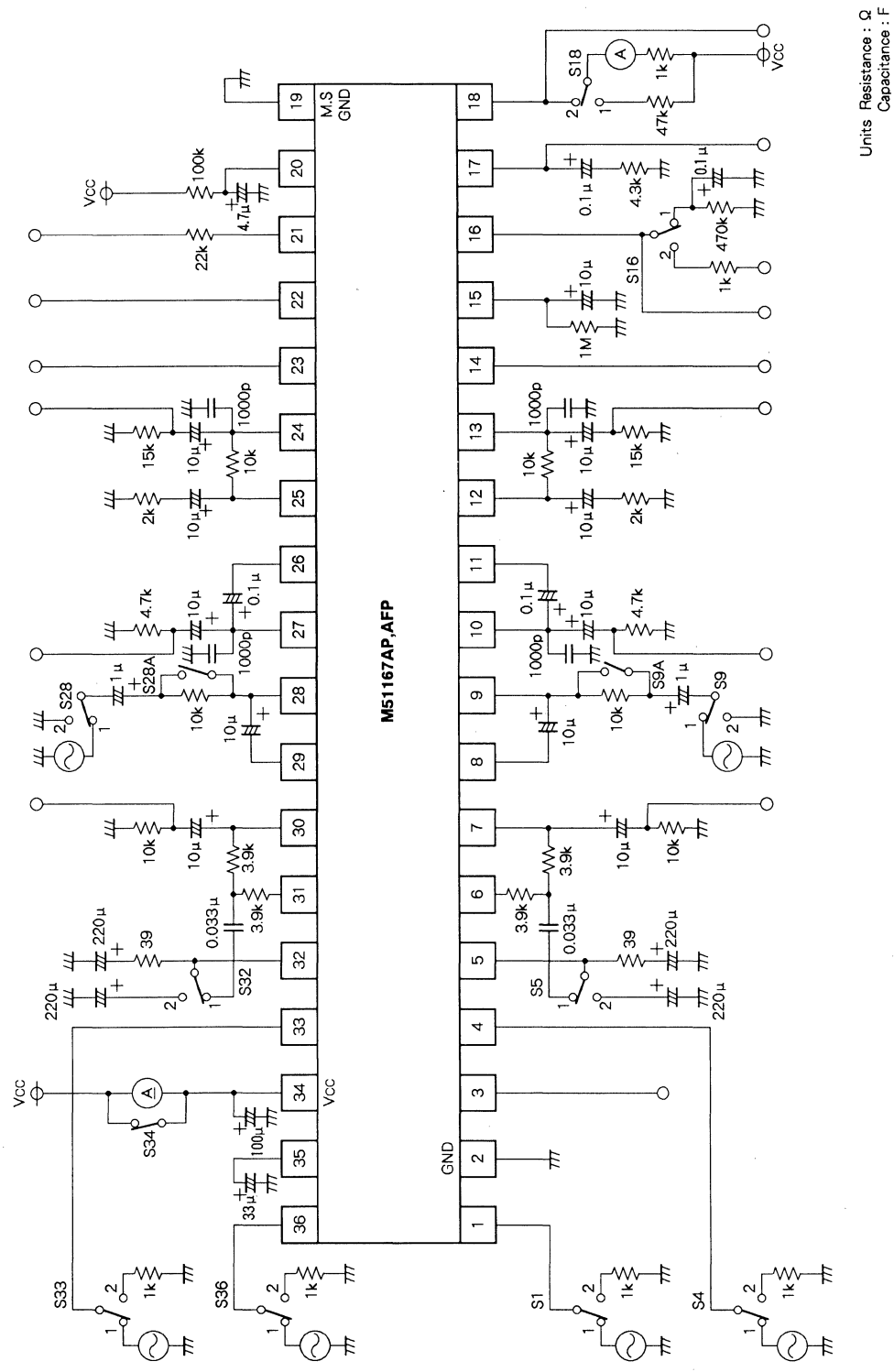
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted, ( ) : M51167AP)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Quiescent	+ 16	V
P_d	Power dissipation		560(1100)	mW
K_θ	Thermal derating	$T_a \geqq 25$℃	5.6(11)	mW/℃
T_{opr}	Operating temperature		−20～+ 75	℃
T_{stg}	Storage temperature		−40～+125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 9V, f = 1kHz, unless otherwise noted)

Symbol	Parameter		Test conditions	Limites			Unit
				Min	Typ	Max	
I_{CCO}		Quiescent circuit current	Quiescence	10	20	30	mA
GvoEQ	EQ Amplifier	Open loop voltage gain	V_i = 0.05Vrms	68	80	–	dB
GvcEQ		Closed loop voltage gain	V_O = 0.5Vrms	40.0	43.0	46.0	dB
THDEQ		Total harmonic distortion	V_O = 0.5Vrms	–	0.05	0.4	%
Vomax		Maximum output voltage	THD = 3%	1.15	1.50	–	Vrms
Ni		Equivalent input noise voltage	BW = 20Hz～20kHz, R_g = 1k Ω	–	1.3	1.9	μVrms
SepEQ		Channel separation	V_O = 0.5Vrms, BW = 20Hz～20kHz	40	65	–	dB
GvcFl	Flat Amplifier	Closed loop voltage gain	V_O = 0.5Vrms	28.3	29.5	30.7	dB
THDFl		Total harmonic distortion	V_O = 0.5Vrms	–	0.03	0.1	%
VomaxF		Maximum output voltage	THD = 3%	1.9	2.3	–	Vrms
NoFL		Output noise voltage	BW = 20Hz～20kHz, R_g = 10k Ω	–	80	160	μVrms
SepFl		Channel separation	V_O = 0.5Vrms, BW = 20Hz～20kHz	40	65	–	dB
GvcRec	Flat-Rec Amplifier	Closed loop voltage gain	V_O = 0.5Vrms	28.8	30.0	31.2	dB
THDRec		Total harmonic distortion	V_O = 0.5Vrms	–	0.02	0.1	%
VomaxR		Maximum output voltage	THD = 3%	1.9	2.4	–	Vrms
NoRec		Output noise voltage	BW = 20Hz～20kHz, R_g = 10k Ω	–	80	160	μVrms
SepRec		Channel separation	V_O = 0.5Vrms, BW = 20Hz～20kHz	40	65	–	dB
VoALC	ALC circuit	ALC output voltage	From the ALC inset point untill input reaches + 10dB	350	450	550	mVrms
THDALC		ALC distortion	Untill input reaches + 10dB	–	0.5	1.5	%
AALC		ALC range	Untill output is 1dB UP	25	30	–	dB
VoL	Music selecter	M.S. output voltage	M.S. output voltage when output is Low	0.0	0.007	0.4	V
BVo		M.S. input current	18-pin input current	–	–	2.0	μA
SVo		M.S. level	EQ output voltage when M.S. output changes to Low from High	−19.5	−23.5	−27.5	dBV
VR/P	SW circuit	R/P mode control voltage	High : Rec mode	3.5	–	5.0	V
			Low : PB mode	0.0	–	1.0	V
VA/B		A/B mode control voltage	High : A mode	3.5	–	5.0	V
			Low : B mode	0.0	–	1.0	V
VEQ		EQ SW control voltage	High : SW ON	3.5	–	5.0	V
			Low : SW OFF	0.0	–	1.0	V
VDA		Dubbing mode control voltage	High : Dubbing ON	3.5	–	5.0	V
			Low : Dubbing OFF	0.0	–	1.0	V

TEST CIRCUIT



TEST METHODS

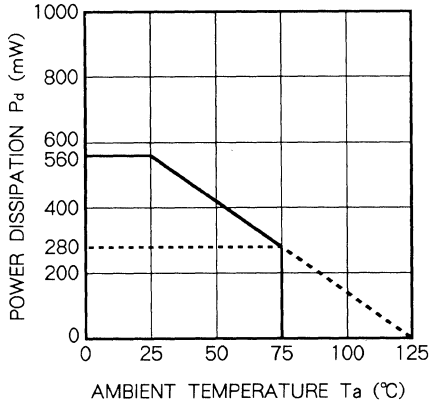
control voltage H = 5V
L = 0V

Symbol	Switch conditions							Control voltage					Input point	Output point	Test method
	S4 (S33)	S5 (S32)	S9 (S28)	S9A (S28A)	S16	S18	S34	3	14	21	22	23			
Icc	2	1	2	OFF	1	1	OFF	H	H	H	H	H		34	
GvoEQ	1	2	2	OFF	1	1	ON	L	L	L	L	L	4	7	Gvo = 20 log (Vo/Vi)
GvcEQ	1	1	2	OFF	1	1	ON	L	L	L	L	L	4	7	Gvc = 20 log (Vo/Vi)
THDEQ	1	1	2	OFF	1	1	ON	L	L	L	L	L	4	7	Vo = 0.5Vrms
VomaxE	1	1	2	OFF	1	1	ON	L	L	L	L	L	4	7	THD = 3%
Ni	2	1	2	OFF	1	1	ON	L	L	L	L	L		7	BW = 20Hz~20kHz
SepEQ	※	1	2	OFF	1	1	ON	L	L	L	L	L	4	30	S4→"1", S33→"2", Vo(7) = 0.5Vrms BW = 20Hz~20kHz
GvcFl	2	1	1	ON	1	1	ON	H	H	L	L	L	9	10	Gvc = 20 log (Vo/Vi)
THDFl	2	1	1	ON	1	1	ON	H	H	L	L	L	9	10	Vo = 0.5Vrms
VomaxF	2	1	1	ON	1	1	ON	H	H	L	L	L	9	10	THD = 3%
NoFl	2	1	2	OFF	1	1	ON	H	H	L	L	L		10	BW = 20Hz~20kHz
SepFl	2	1	※	ON	1	1	ON	H	H	L	L	L	9	27	S9→"1", S28→"2", Vo(7) = 0.5Vrms BW = 20Hz~20kHz
GvcRec	2	1	1	ON	1	1	ON	H	H	L	L	L	9	13	Gvc = 20 log (Vo/Vi)
THDRec	2	1	1	ON	1	1	ON	H	H	L	L	L	9	13	Vo = 0.5Vrms
VomaxR	2	1	1	ON	1	1	ON	H	H	L	L	L	9	13	THD = 3%
NoRec	2	1	2	OFF	1	1	ON	H	H	L	L	L		13	BW = 20Hz~20kHz
SepRec	2	1	※	ON	1	1	ON	H	H	L	L	L	9	24	Vo(13) = 0.5Vrms BW = 20Hz~20kHz
VoALC	2	1	1	OFF	1	1	ON	L	H	L	L	L	9	13	Note 1
THDALC	2	1	1	OFF	1	1	ON	L	H	L	L	L	9	13	Note 2
AALC	2	1	1	OFF	1	1	ON	L	H	L	L	L	9	13	Note 3
VoL	2	1	2	OFF	2	1	ON	L	L	L	L	L		18	Note 4
BVo	2	1	2	OFF	2	2	ON	L	L	L	L	L		18	Note 5
SVo	1	1	2	OFF	1	1	ON	L	L	L	L	L	4	7,18	Note 6
VR/P	2	1	1	ON	1	1	ON	H	※	L	L	L	9	13	Note 7
VA/B	1	1	2	OFF	1	1	ON	L	L	※	L	L	4	7	Note 8
VEQ	1	1	2	OFF	1	1	ON	L	L	L	L	※	4	7	Note 9
VDA	2	1	1	OFF	1	1	ON	※	H	L	L	L	9	13	Note 10

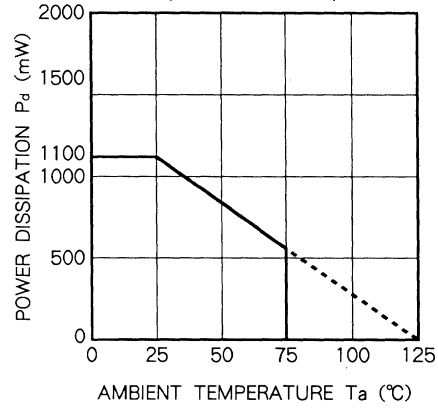
Note 1. Measure output voltage from the ALC inset point until input reaches + 10dB.
2. Measure output distortion from the point ALC is activated until input reaches + 10dB.
3. Input voltage range measured from the output voltage of the starting point to the point where the output voltage becomes 1dB higher.
4. Measure voltage of pin ⑱ after preset pulse enters pin ⑯ at ⑳ msec.
5. Measure current of pin ⑱ after preset pulse enters pin ⑯ at ⑳ msec.
6. Measure output voltage of pin ⑦ when input voltage of pin ④ increases and output of pin ⑱ changes to Low from High.
7. When voltage of pin ⑭ is 4V, output is operating state and voltage of pin ⑭ is 1V, output is noise voltage level.
8. When voltage of pin ㉑ is 1V, output is operating state and voltage of pin ㉑ is 4V, output is noise voltage level.
9. The difference between voltage of pin ㉓ is 4V and 1V is 6dB.
10. When voltage of pin ⑬ is 4V, ALC is operating state and voltage of pin ③ is 1V, ALC is not operating.

TYPICAL CHARACTERISTICS

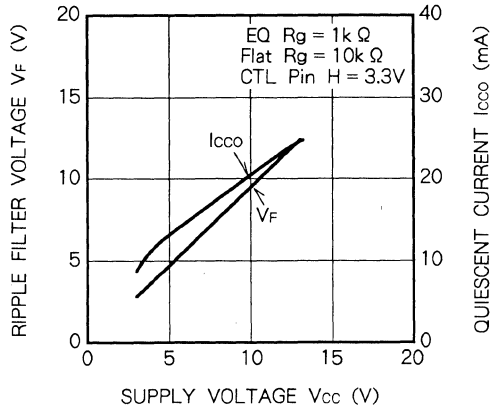
THERMAL DERATING (M51167AFP)
(MAXMUM RATING)



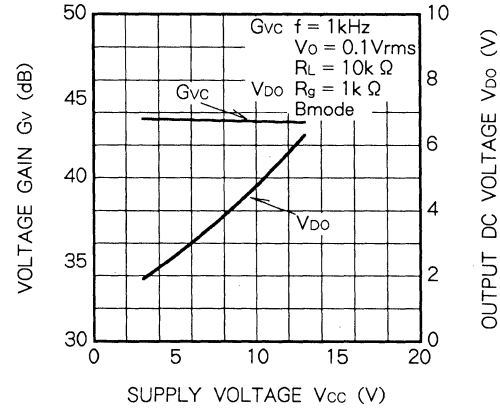
THERMAL DERATING (M51167AP)
(MAXMUM RATING)



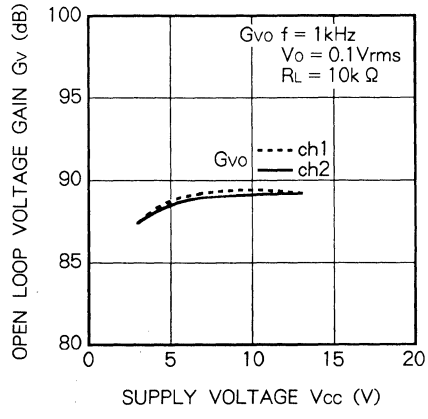
RIPPLE FILTER PIN ⑧ VOLTAGE,
QUIESCENT CIRCUIT CURRENT
VS. SUPPLY VOLTAGE



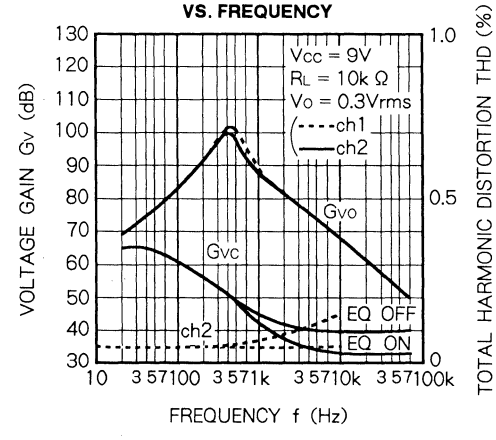
EQ AMPLIFIER CLOSED LOOP VOLTAGE GAIN,
OUTPUT DC VOLTAGE VS. SUPPLY VOLTAGE



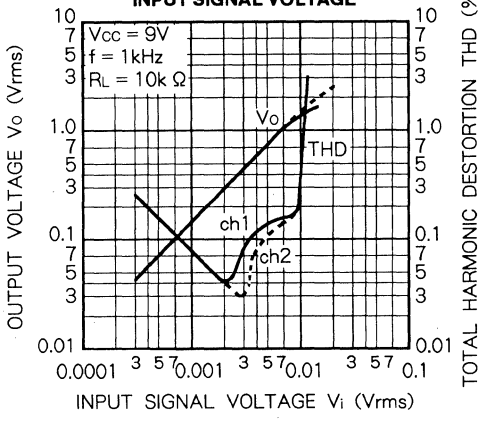
EQ AMPLIFIER OPEN LOOP VOLTAGE
GAIN VS. SUPPLY VOLTAGE



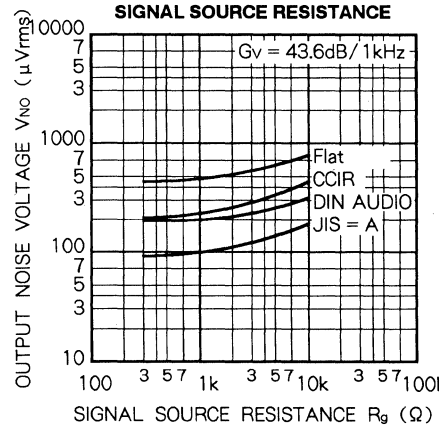
EQ AMPLIFIER VOLTAGE GAIN,
TOTAL HARMONIC DISTORTION
VS. FREQUENCY



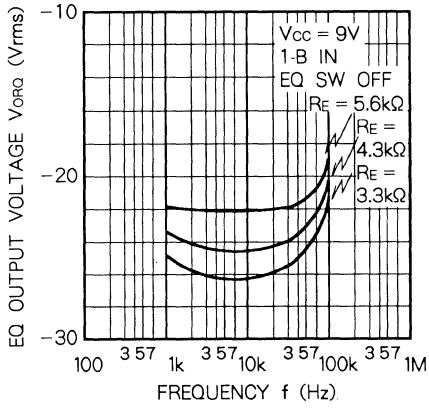
EQ AMPLIFIER OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE



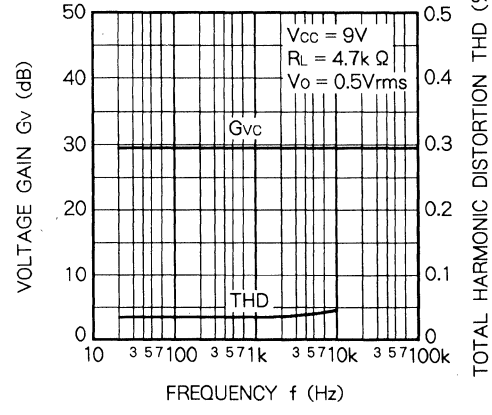
OUTPUT NOISE VOLTAGE VS. SIGNAL SOURCE RESISTANCE



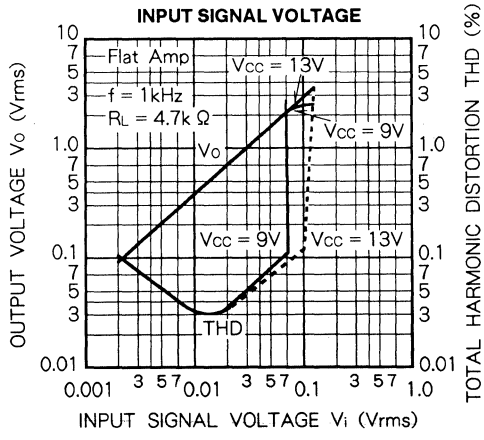
M.S. LEVEL (EQ OUTPUT VOLTAGE) VS. FREQUENCY



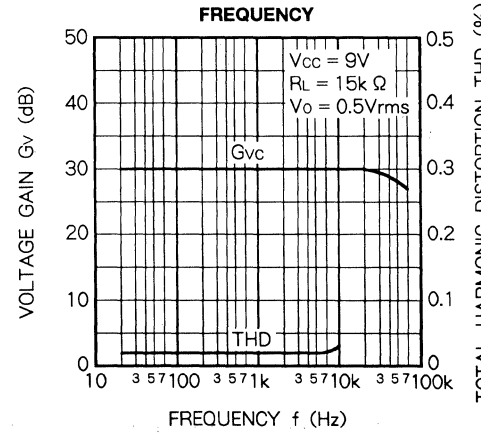
FLAT AMPLIFIER VOLTAGE GAIN, TOTAL HARMONIC DISTORTION VS. FREQUENCY



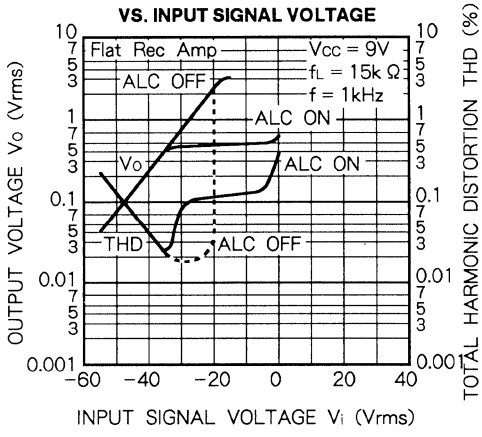
FLAT AMPLIFIER OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE



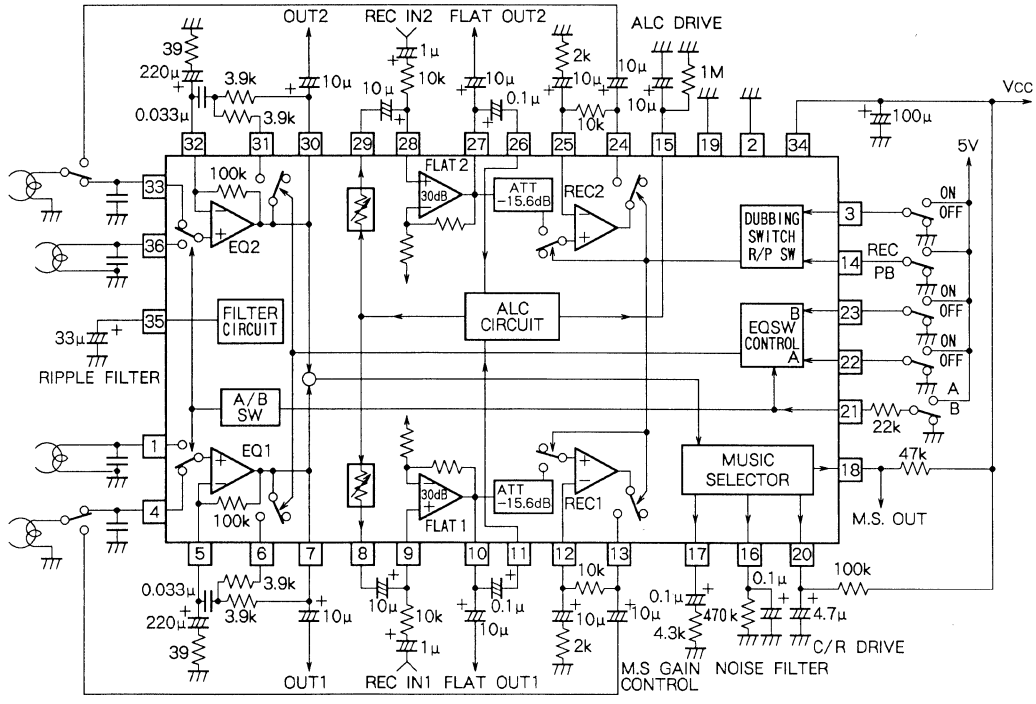
FLAT-REC AMPLIFIER VOLTAGE GAIN, TOTAL HARMONIC DESTORTION VS. FREQUENCY



FLAT-REC AMPLIFIER OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE



APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

OPERATIONAL CHECK LIST

Pin③ (Dubbing control)	H	H	L	L
Pin⑭ (Rec/RB control)	H	L	H	L
Flat amplifier	○	○	○	○
Rec amplifier	○	×	○	×
ALC circuit	OFF	OFF	ON	OFF

M51167BP,BFP

SINGLE CHIP PREAMPLIFIER FOR DUAL CASSETTE RECORDER

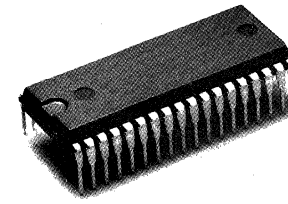
DESCRIPTION

The M51167 is an IC designed for radio CD/cassette tape players.

The IC, in addition to recording and playback preamplifiers (2 ch) for dual cassette, has equalizer selector, music selector, and ALC (automatic level controller) and is, with a single chip, capable of processing audio signals of cassette deck.

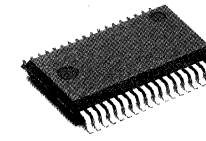
FEATURES

- Built-in electronic switch for double cassette.
- Built-in equalizer switch for both modes.
- Low noise EQ amplifier····· 1.3μVrms (typ)
- Two built-in Rec amplifiers with ALC circuit for noise reduction system
- Built-in filter circuits for prevention of malfunctioning caused by tape pop up noise at music blank.
- Capable of setting timimg for music blank by means of external CR combination.



Outline 36P4E(BP)

1.778mm pitch 500mil SDIP
(11.0mm × 31.5mm × 3.8mm)



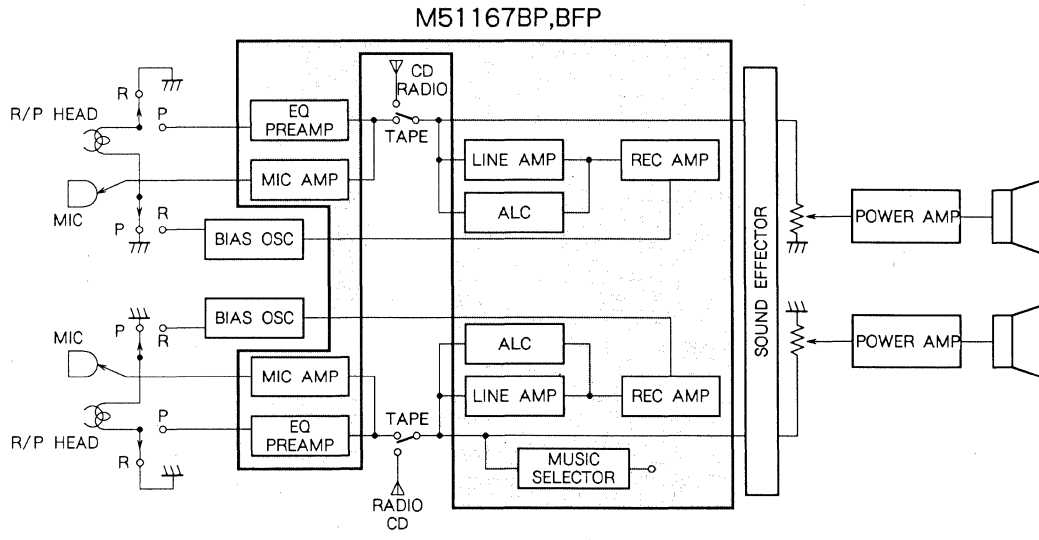
Outline 36P2R-A(BFP)

0.8mm pitch 450mil SSOP
(8.4mm × 15.0mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

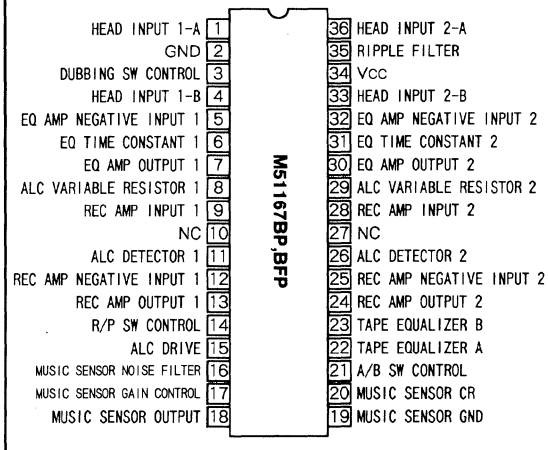
Supply voltage range····· V_{CC} = 5.5~12V
Rated supply voltage····· V_{CC} = 9V

SYSTEM CONFIGURATION



MITSUBISHI ELECTRIC

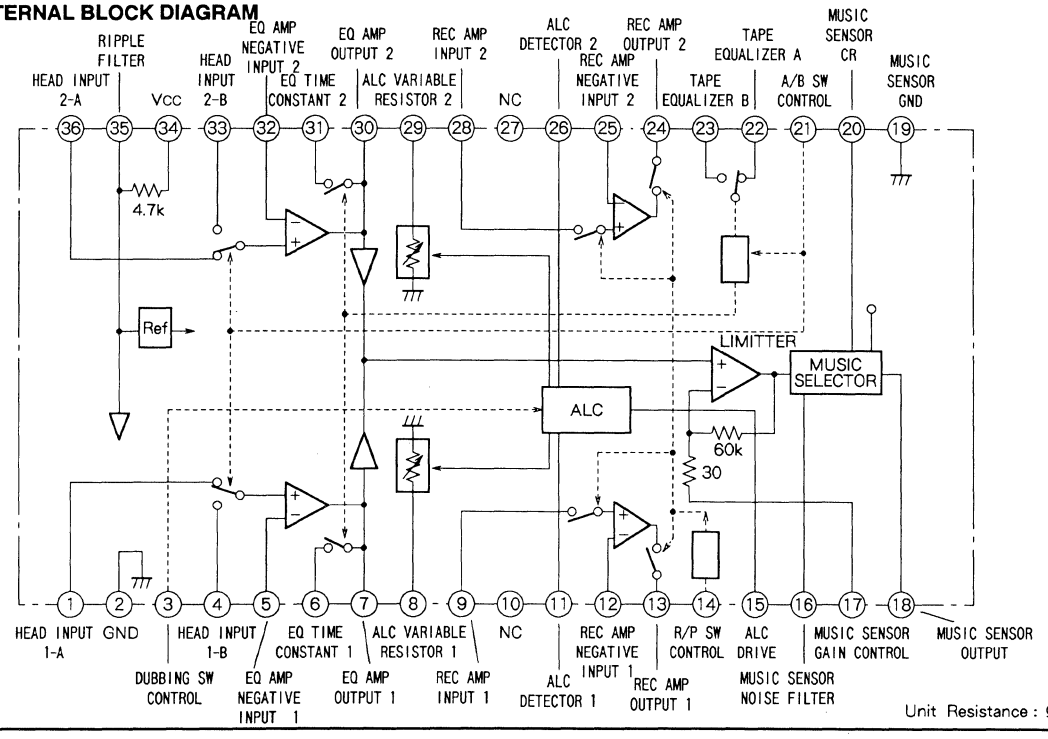
PIN CONFIGURATION



Outline 36P4E(BP)
36P2R-A(BFP)

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



M51167BP,BFP

SINGLE CHIP PREAMPLIFIER FOR DUAL CASSETTE RECORDER

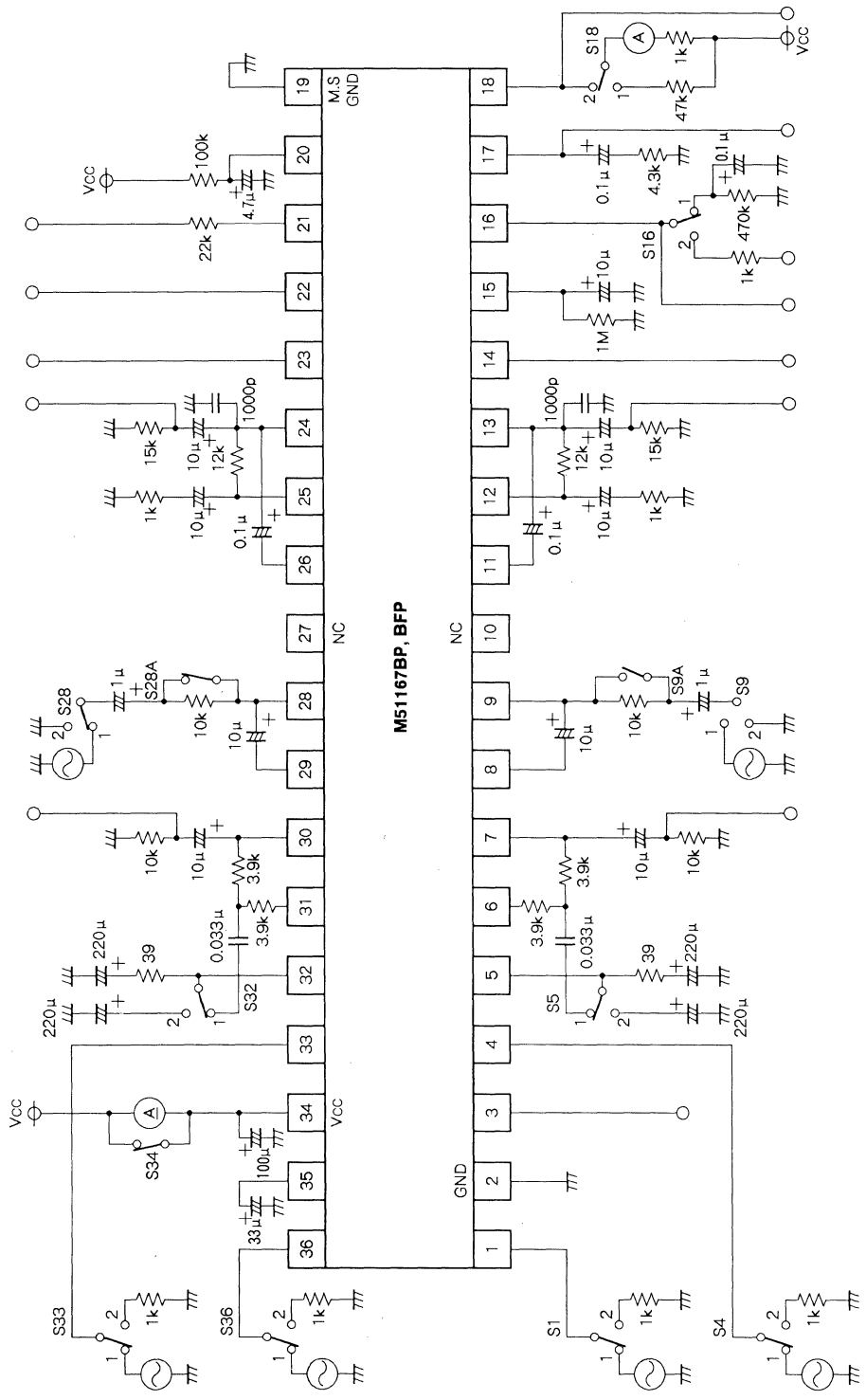
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted, ( ) : M51167BP)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Quiescent	+ 16	V
P_d	Power dissipation		560(1100)	mW
K_θ	Thermal derating	$T_a \geqq 25$℃	5.6(11)	mW/℃
T_{opr}	Operating temperature		−20～+ 75	℃
T_{stg}	Storage temperature		−40～+125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, Vcc = 9V, f = 1kHz, unless otherwise noted)

Symbol		Parameter	Test Conditions	Limits			Unit
				Min	Typ	Max	
Icco	EQ Amplifier	Quiescent circuit current	Quiescence	10	20	30	mA
GvoEQ	EQ Amplifier	Open loop voltage gain	V_i = 0.05mVrms	68	80	−	dB
GvcEQ	EQ Amplifier	Closed loop voltage gain	V_o = 0.5Vrms	40.0	43.0	46.0	dB
THDEQ	EQ Amplifier	Total harmonic distortion	V_o = 0.5Vrms	−	0.05	0.4	%
Vomax	EQ Amplifier	Maximum output voltage	THD = 3%	1.15	1.50	−	Vrms
N_i	EQ Amplifier	Equivalent input noise voltage	BW = 20Hz～20kHz, R_g = 1k Ω	−	1.3	1.9	μVrms
SepEQ	EQ Amplifier	Channel separation	V_o = 0.5Vrms, BW = 20Hz～20kHz	40	65	−	dB
GvcRec	Rec Amplifier	Closed loop voltage gain	V_o = 0.5Vrms	21.0	22.2	23.4	dB
THDRec	Rec Amplifier	Total harmonic distortion	V_o = 0.5Vrms	−	0.01	0.1	%
VomaxR	Rec Amplifier	Maximum output voltage	THD = 3%	1.9	2.4	−	Vrms
NoRec	Rec Amplifier	Output noise voltage	BW = 20Hz～20kHz, R_g = 10k Ω	−	35	70	μVrms
SepRec	Rec Amplifier	Channel separation	V_o = 0.5Vrms, BW = 20Hz～20kHz	50	75	−	dB
VoALC	ALC Circuit	ALC output voltage	From the ALC inset point until input reaches + 10dB	350	450	550	mVrms
THDALC	ALC Circuit	ALC distortion	Until input reaches + 10dB	−	0.5	1.5	%
AALC	ALC Circuit	ALC range	Until output is 1dB UP	25	30	−	dB
VoL	Music selecter	M.S. output voltage	M.S. Output voltage when output is Low	0.0	0.007	0.4	V
BVo	Music selecter	M.S. input current	Pin ⑱ input current	−	−	2.0	μA
SVo	Music selecter	M.S. level	EQ output voltage when M.S. output changes to Low from High	−19.5	−23.5	−27.5	dBV
V R/P	SW Circuit	R/P mode control voltage	High : Rec mode	3.5	−	5.0	V
			Low : PB mode	0.0	−	1.0	
V A/B	SW Circuit	A/B mode control voltage	High : A mode	3.5	−	5.0	V
			Low : B mode	0.0	−	1.0	
V EQ	SW Circuit	EQ SW control voltage	High : SW ON	3.5	−	5.0	V
			Low : SW OFF	0.0	−	1.0	
V DA	SW Circuit	Dubbing mode control voltage	High : Dubbing ON	3.5	−	5.0	V
			Low : Dubbing OFF	0.0	−	1.0	

TEST CIRCUIT



TEST METHODS

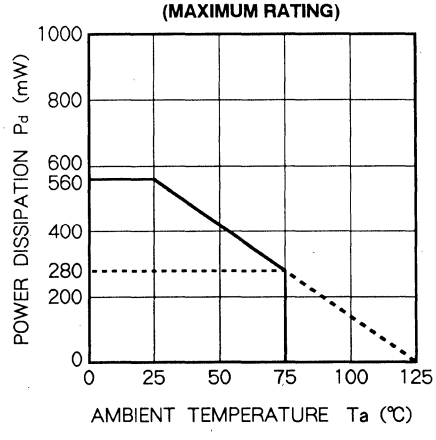
control voltage H = 5V
L = 0V

Symbol	Switch conditions							Control voltage					Input point	Output point	Test method
	S4 (S33)	S5 (S32)	S9 (S28)	S9A (S28A)	S16	S18	S34	3	14	21	22	23			
Icc	2	1	2	OFF	1	1	OFF	H	H	H	H	H		34	
GvoEQ	1	2	2	OFF	1	1	ON	L	L	L	L	L	4	7	Gvo = 20 log (Vo/Vi)
GvcEQ	1	1	2	OFF	1	1	ON	L	L	L	L	L	4	7	Gvc = 20 log (Vo/Vi)
THDEQ	1	1	2	OFF	1	1	ON	L	L	L	L	L	4	7	Vo = 0.5Vrms
VomaxE	1	1	2	OFF	1	1	ON	L	L	L	L	L	4	7	THD = 3%
Ni	2	1	2	OFF	1	1	ON	L	L	L	L	L		7	BW = 20Hz~20kHz
SepEQ	※	1	2	OFF	1	1	ON	L	L	L	L	L	4	30	Vo(7) = 0.5Vrms BW = 20Hz~20kHz
GvcRec	2	1	1	ON	1	1	ON	H	H	L	L	L	9	13	Gvc = 20 log (Vo/Vi)
THDRec	2	1	1	ON	1	1	ON	H	H	L	L	L	9	13	Vo = 0.5Vrms
VomaxR	2	1	1	ON	1	1	ON	H	H	L	L	L	9	13	THD = 3%
NoRec	2	1	2	OFF	1	1	ON	H	H	L	L	L		13	BW = 20Hz~20kHz
SepRec	2	1	※	ON	1	1	ON	H	H	L	L	L	9	24	Vo(13) = 0.5Vrms BW = 20Hz~20kHz
VoALC	2	1	1	OFF	1	1	ON	L	H	L	L	L	9	13	Note 1
THDALC	2	1	1	OFF	1	1	ON	L	H	L	L	L	9	13	Note 2
AALC	2	1	1	OFF	1	1	ON	L	H	L	L	L	9	13	Note 3
Vo L	2	1	2	OFF	2	1	ON	L	L	L	L	L		18	Note 4
BVo	2	1	2	OFF	2	2	ON	L	L	L	L	L		18	Note 5
SVo	1	1	2	OFF	1	1	ON	L	L	L	L	L	4	7,18	Note 6
VR/P	2	1	1	ON	1	1	ON	H	※	L	L	L	9	13	Note 7
VA/B	1	1	2	OFF	1	1	ON	L	L	※	L	L	4	7	Note 8
VEQ	1	1	2	OFF	1	1	ON	L	L	L	L	※	4	7	Note 9
VDA	2	1	1	OFF	1	1	ON	※	H	L	L	L	9	13	Note 10

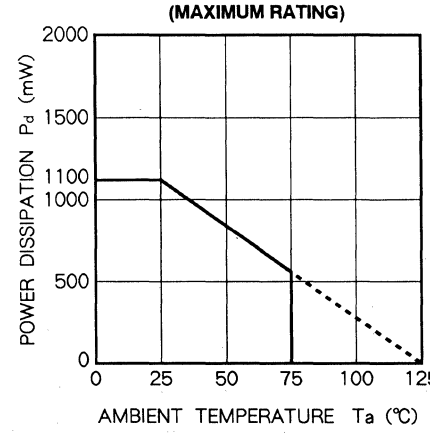
Note 1. Measure output voltage from the ALC inset point until input reaches + 10dB.
3. Input voltage range measured from the output voltage of the starting point to the point where the output voltage becomes 1dB higher.
4. Measure voltage of pin ⑱ after preset pulse enters pin ⑯ at ⑳ msec.
5. Measure current of pin ⑱ after preset pulse enters pin ⑯ at ⑳ msec.
6. Measure output voltage of pin ⑦ when input voltage of pin ④ increases and output of pin ⑱ changes to Low from High.
7. When voltage of pin ⑭ is 4V, output is operating state and voltage of pin ⑭ is 1V, output is noise voltage level.
8. When voltage of pin ㉑ is 1V, output is operating state and voltage of pin ㉑ is 4V, output is noise voltage level.
9. The difference between voltage of pin ㉓ is 4V and 1V is 6dB.
10. When voltage of pin ③ is 4V, ALC is operating state and voltage of pin ③ is 1V, ALC is not operating.

TYPICAL CHARACTERISTICS

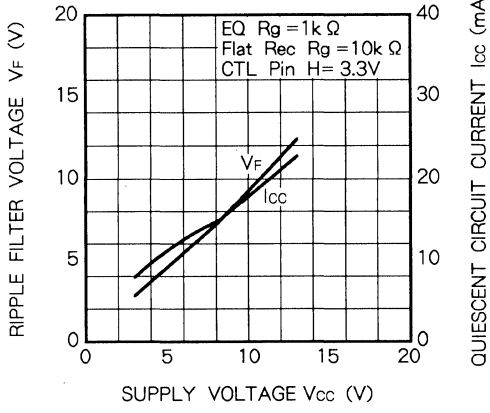
THERMAL DERATING (M51167BFP)
(MAXIMUM RATING)



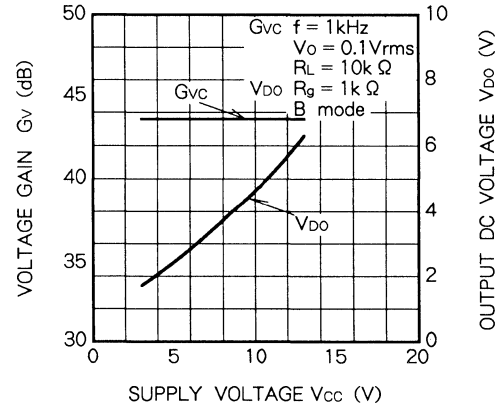
THERMAL DERATING (M51167BP)
(MAXIMUM RATING)



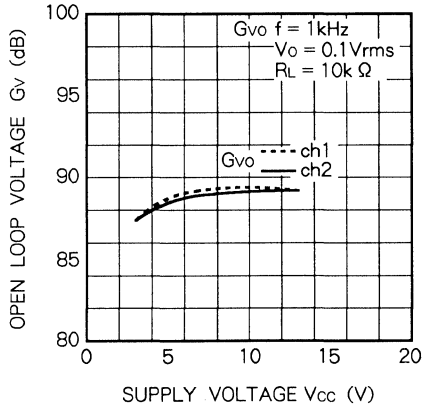
RIPPLE FILTER PIN ⑧ VOLTAGE, QUIESCENT CIRCUIT CURRENT VS. SUPPLY VOLTAGE



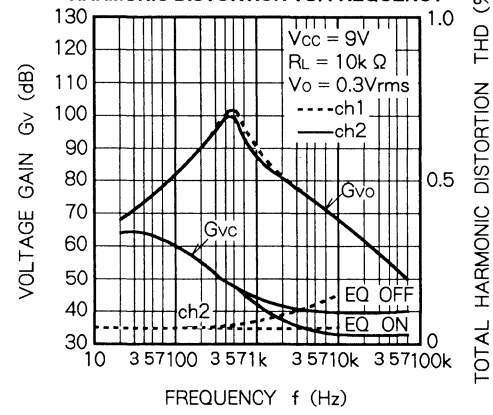
EQ AMPLIFIER CLOSED LOOP VOLTAGE GAIN, OUTPUT DC VOLTAGE VS. SUPPLY VOLTAGE



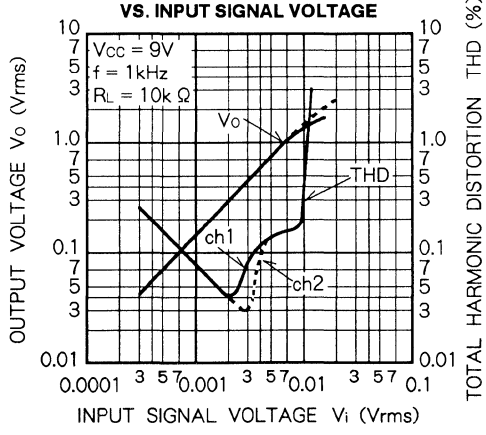
EQ AMPLIFIER OPEN LOOP VOLTAGE GAIN VS. SUPPLY VOLTAGE



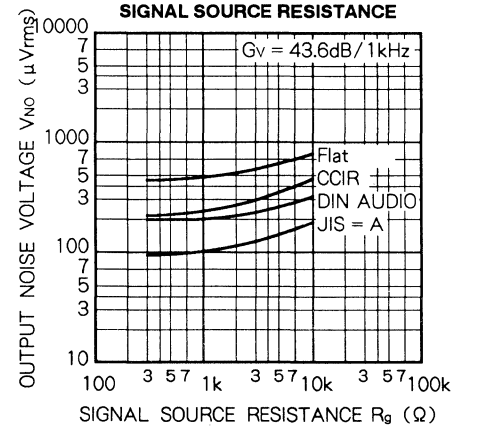
EQ AMPLIFIER VOLTAGE GAIN, TOTAL HARMONIC DISTORTION VS. FREQUENCY



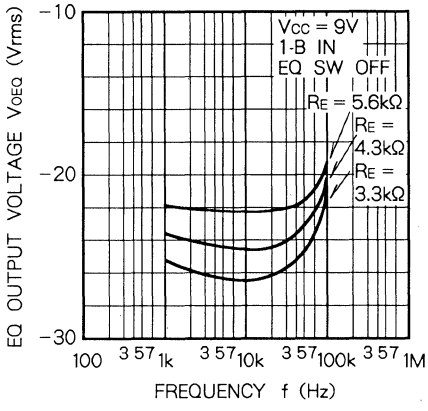
EQ AMPLIFIER OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE



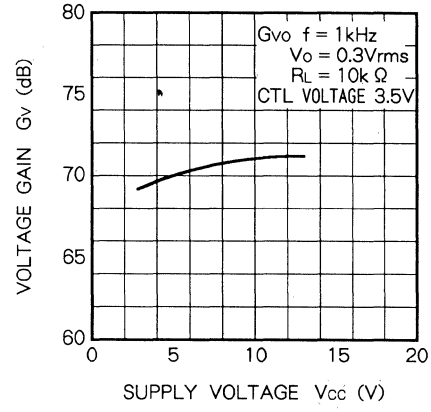
OUTPUT NOISE VOLTAGE VS. SIGNAL SOURCE RESISTANCE



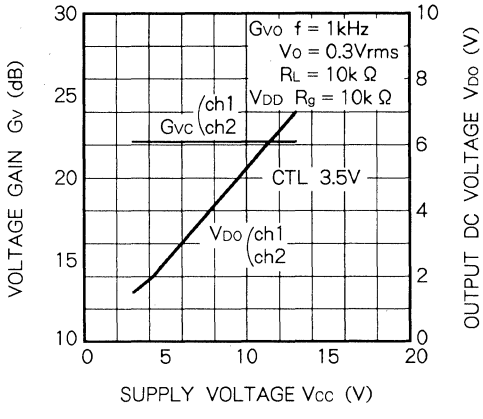
M.S. LEVEL (EQ OUTPUT VOLTAGE) VS. FREQUENCY



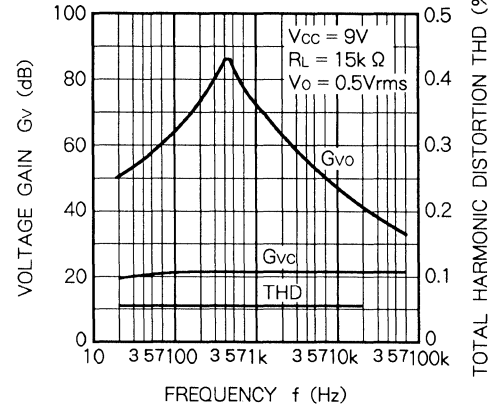
REC AMPLIFIER OPEN VOLTAGE GAIN VS. SUPPLY VOLTAGE



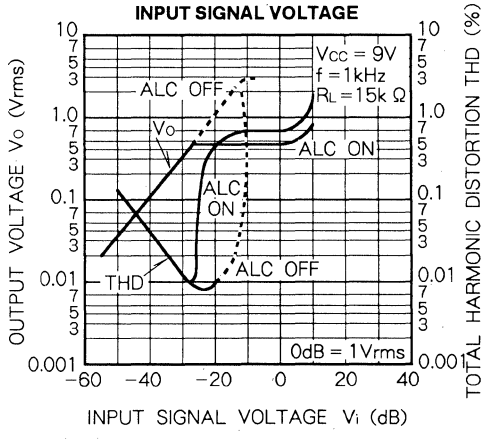
REC AMPLIFIER CLOSED LOOP VOLTAGE GAIN, OUTPUT DC VOLTAGE VS. SUPPLY VOLTAGE



REC AMPLIFIER VOLTAGE GAIN,TOTAL HARMONIC DISTORTION VS. FREQUENCY



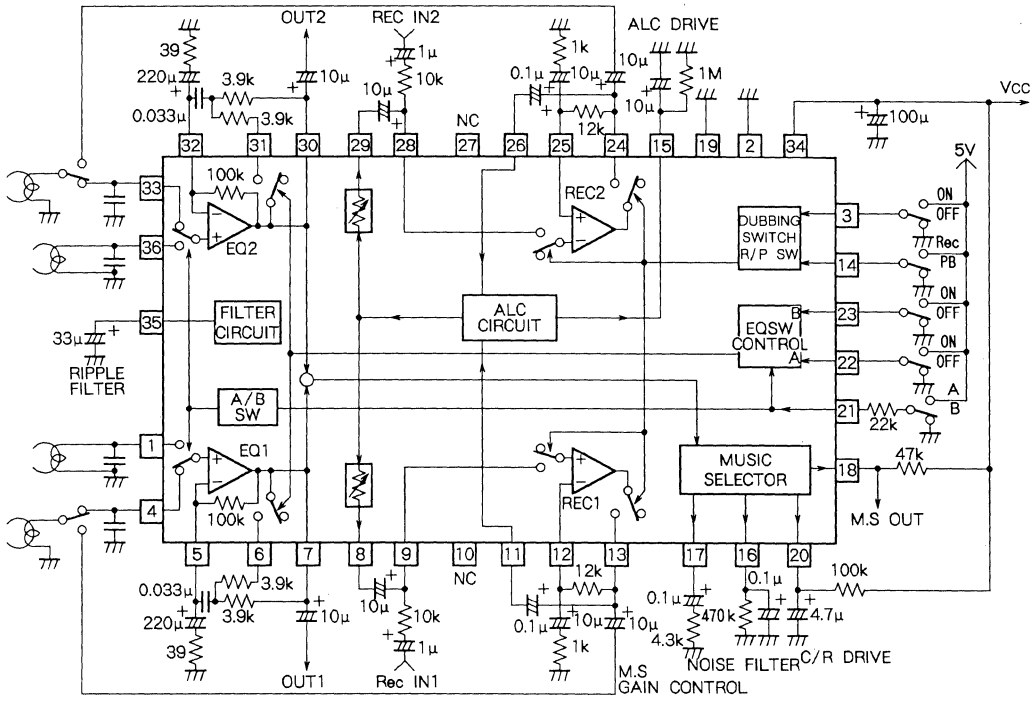
REC AMPLIFIER OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL VOLTAGE



M51167BP,BFP

SINGLE CHIP PREAMPLIFIER FOR DUAL CASSETTE RECORDER

APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

OPERATIONAL CHECK LIST

Pin③ (Dubbing control)	H	H	L	L
Pin⑭ (Rec/RB control)	H	L	H	L
EQ amplifier	○	○	○	○
Rec amplifier	○	×	○	×
ALC circuit	OFF	OFF	ON	OFF

M52122FP

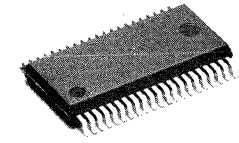
AUTOMATIC ADJUSTMENT-PROVIDED RECORDING AND PLAYING PREAMPLIFIER

DESCRIPTION

The M52122FP is a preamplifier for recording and playing on double-cassette tape becks. With various circuits for automatic adjustment incorporated, including playing level and recording equalizer characteristics adjustments, the IC can streamline the production line of mini-compo and radio cassette units, eliminating convetional adjustment processes.

FEATURES

- Controls based on 16-bit serial data from the microcomputer
- Uses the two-line communication system (DATA and CLK)
- The output ports can be switched, corresponding to the dual cassettes unit to be used
- Incorporates the electronic volume to adjust playing output
- Incorporates the recording amplifier capable of micro-computerized fine adjustment of characteristics (recording equalizer characteristics and recording level adustment).
- Incorporates the line amplifier with ALC function possible to use the noise reduction IC (the amplifier probided with the ATT circuit for line input level adjustment as well)
- Incorporates the voltage output circuit for bias adjustment (in eight steps)



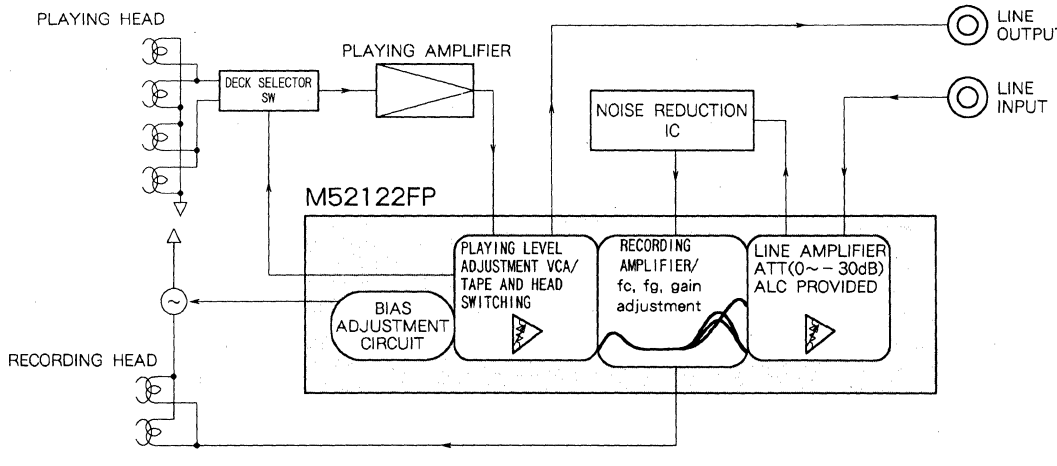
Outline 42P2R-A

0.8mm pitch 450mil SSOP
(8.4mm × 17.5mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC}, V_{EE} = 5.5~7.0V
Rated supply voltage ..... V_{CC}, V_{EE} = ± 6V
Rated power consumption 480mW

SYSTEM CONFIGURATION

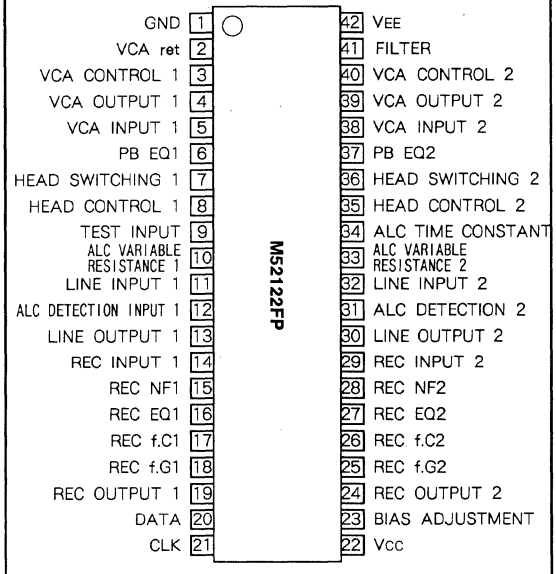


MITSUBISHI ELECTRIC

M52122FP

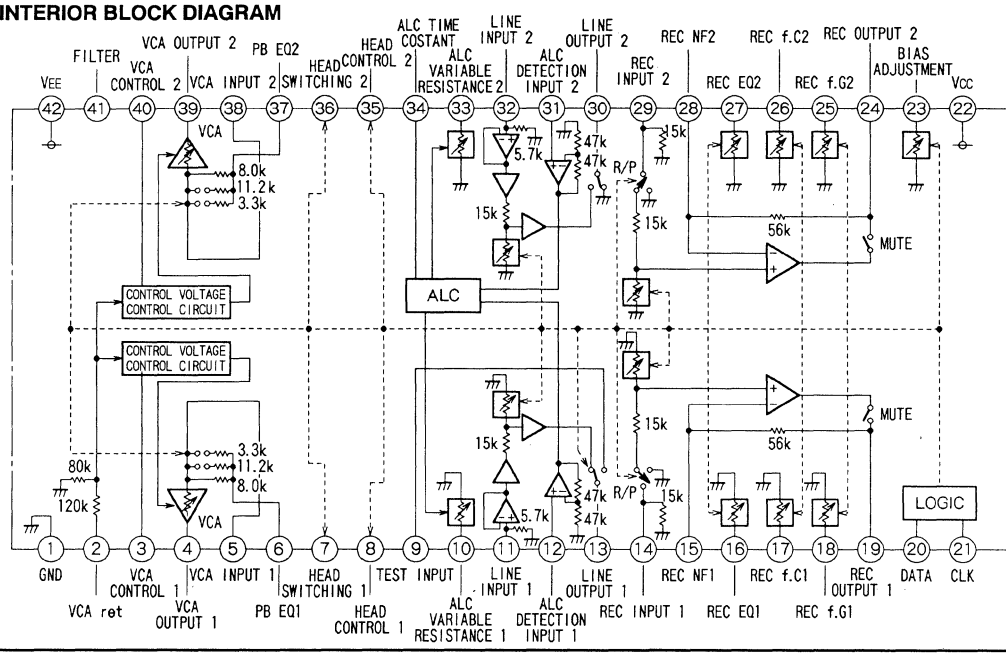
AUTOMATIC ADJUSTMENT-PROVIDED RECORDING AND PLAYING PREAMPLIFIER

PIN CONFIGURATION



Outline 42P2R-A

IC INTERIOR BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	7.5	V
V_{EE}		− 7.5	V
P_d	Power dissipation	1000*Standard circuit board	mW
T_{opr}	Operating temperature	−20～+60	℃
T_{stg}	Storage temperature	−40～+125	℃

ELECTRICAL CHARATERISTICS (V_{CC} = 6V, V_{EE} = − 6.0V, f = 1kHz, Ta = 25℃, unless otherwise noted)

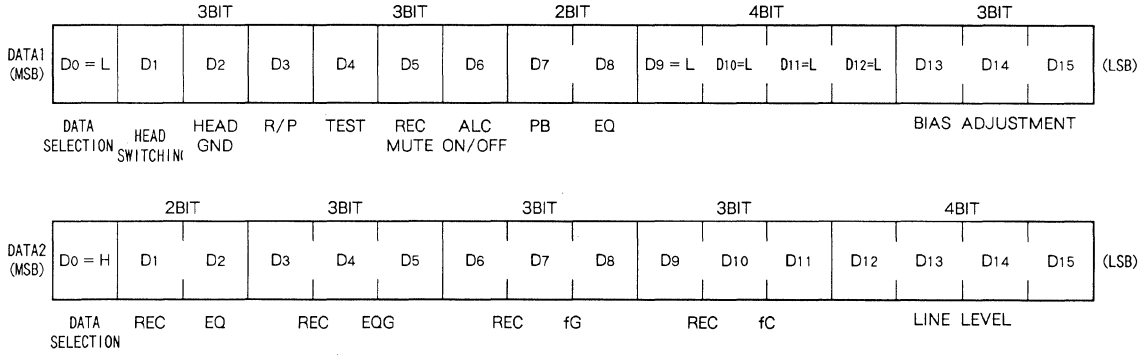
Block	Symbol	Parameter		Test conditions	Limits Min	Limits Typ	Limits Max	Unit
	I_{CC}	Circuit current 1		When no signal after power on	−	38	45	mA
	I_{EE}	Circuit current 2		When no signal after power on	− 45	− 38	−	mA
VCA amplifier	GvcEQ0	Attenuation 0		V_i = 0.5Vrms, Vc = 4.5V, VCAref = 5.0V	− 1	+ 1	+ 3	dB
	GvcEQ1	Attenuation 1		V_i = 0.5Vrms, Vc = 1.85V, VCAref = 5.0V	− 10	− 6	− 2	dB
	THDEQ	Full higjer harmonics distortion factor		V_O = 0.5Vrms	−	0.05	0.4	%
	V_{OmaxE}	Maximum output voltage		When THD = 3%	1.15	1.50	−	Vrms
	Ni	Output noise voltage		BW = 20Hz～20kHz, Rg = 1kΩ	−	40	85	μVrms
	SepEQ	Separation		V_O=0.5Vrms, BW=20Hz～20kHz, Rg=1kΩ	60	85	−	dB
REC amplifier	GvcRec	Closed loop voltage gain		V_O=0.5Vrms, normal condition, gain set to max	4.4	5.6	6.8	dB
	THDRec	Full higher harmonic distortion factor		V_O = 0.5Vrms	−	0.01	0.1	%
	V_{OmaxR}	Maximum output voltage		When THD = 3%	1.9	2.4	−	Vrms
	NoRec	Output noise voltage		BW = 20Hz～20kHz, Rg = 10kΩ	−	35	70	μVrms
	SepRec	Separation		V_O=0.5Vrms, BW=20Hz～20kHz, Rg=10kΩ	50	75	−	dB
ALC	VoALC	ACL output voltage		When ALC level at start + 10dB	40.0	49.0	58.0	mVrms
	THDALC	ALC distortion factor		When ALC level at start + 10dB	−	0.5	1.5	%
	AALC	ALC range		Input level range during ALC on	22	27	−	dB
LINE amplifier	GvcLIN	Closed loop voltage gain		V_O=0.5Vrms, ALC off, gain set to max	− 14	− 12	− 10	dB
	THDLIN	Full higher harmonics distortion factor		V_O=0.5Vrms, ALC off, gain set to max	−	0.01	0.1	%
	V_{OmaxL}	Maximum output voltage		When THD = 3%	1.15	1.5	−	Vrms
	NoLIN	Output noise voltage		BW = 20Hz～20kHz, Rg = 10kΩ	−	15	70	μVrms
	SepLIN	Separation		V_O=0.5Vrms, BW=20Hz～20kHz, Rg=10kΩ	50	75	−	dB
LOGIC input	ICH	CLK input current		VCH = 5V	− 1	0	+ 1	μA
	ICL			VCL = 0V	− 1	− 0.05	+ 1	μA
	IDH	DATA input current		VDH = 5V	− 1	0	+ 1	μA
	IDL			VDL = 0V	− 1	− 0.05	+ 1	μA
	VCH	CLK	H-level voltage	Recommended conditions	3.5	5.0	Vcc	V
	VCL		L-level voltage	Recommended conditions	GND	0.0	1.0	V
	VDH	DATA	H-level voltage	Recommended conditions	3.5	5.0	Vcc	V
	VDL		L-level voltage	Recommended conditions	GND	0	1.0	V
LOGIC output	V_{OH}A/B	Head switching output	H-output voltage	R_{PL} = 24kΩ when data 1 head switching output is set to 0	5.9	6.0	−	V
	V_{OL}A/B		L-output voltage	R_{PL} = 24kΩ when data 1 head switching output is set to 1	−	5.75	− 5.6	V
	V_{OH}GND	Head control output	H-output voltage	R_{PL} = 12kΩ when data 1 head switching output is set to 0	5.9	6.0	−	V
	V_{OL}GND		L-output voltage	R_{PL} = 12kΩ when data 1 head switching output is set to 1	−	5.85	− 5.7	V
EQ NF resistance	REQNF0	EQ NF resistance 0		For data 1, D7 = 0 and D8 = 0	6.40	8.00	9.60	kΩ
	REQNF1	EQ NF resistance 1		For data 1, D7 = 0 and D8 = 1	3.76	4.70	5.64	kΩ
	REQNF2	EQ NF resistance 2		For data 1, D7 = 1 and D8 = 0	1.86	2.33	2.80	kΩ
REC amplifier control	RecG1	Rec gain control 1		For data 2,(D3,D4,D5)=(1,0,0),GVCRec reference	− 3.5	− 2.8	− 2.1	dB
	RecG2	Rec gain control 2		For data 2,(D3,D4,D5)=(1,1,1), GVCRec reference	− 5.3	− 4.6	− 3.9	dB
	RecfG1	Rec fG control 1		For data 2,(D6,D7,D8)=(1,0,0),f=10kHz reference	+ 2.1	+ 2.8	+ 3.5	dB
	RecfG2	Rec fG control 2		For data 2,(D6,D7,D8)=(1,1,1),f=10kHz reference	+ 4.2	+ 4.9	+ 5.6	dB
	RecfC1	Rec fC control 1		For data 2, (D9, D10, D11)=(1, 0, 0), f=10kHz reference	− 2.3	− 1.6	− 0.9	dB
	RecfC2	Rec fC control 2		For data 2, (D9, D10, D11)=(1, 1, 1) f=10kHz reference	− 3.5	− 2.8	− 2.1	dB

ELECTRICAL CHARATERISTICS (cont.)

Block	Symbol	Parameter	Test conditions	Limits			Unit
				Min	Typ	Max	
REC amplifier control	GvcRME	Rec gain metal	For data 2,(D1, D2)=(0, 1)Vo=0.5Vrms f=1kHz	8.7	9.5	10.3	dB
	GvcCr0	Rec gain Cr02	For data 2,(D1, D2)=(1, 0) Vo=0.5Vrms f=1kHz	7.0	7.8	8.6	dB
	GvcR/P	Rec R/P operation	For data 1, output ratio between when D3=0 and D3=1	50	70	–	dB
	GvcMUTE	Rec output muted operation	For data 1, output ratio between when D5=0 and D5=1	60	80	–	dB
LINE amplifier control	GvcTEST	TEST input operation	For data 1, D4=1, Vo=0. 5Vrms, f=1kHz	– 1	0	+ 1	dB
	GvcLC1	LINE level control 1	For data 2, (D12, D13, D14, D15)=(0, 1, 1, 1)	– 16	– 14	– 12	dB
	GvcLC2	LINE level control 2	For data 2, (D12, D13, D14, D15)=(1, 1, 1, 1)	– 32	– 30	– 28	dB
AC bias control	Rbias1	AC bias control resistance 1	For data 1,(D13,D14,D15) = (0,0,1)	67.0	84.5	103	k Ω
	Rbias2	AC bias control resistance 2	For data 1,(D13,D14,D15) = (1,0,0)	12.4	15.6	18.8	k Ω
	Rbias3	AC bias control resistance 3	For data 1,(D13,D14,D15) = (1,1,1)	6.1	7.7	9.3	k Ω

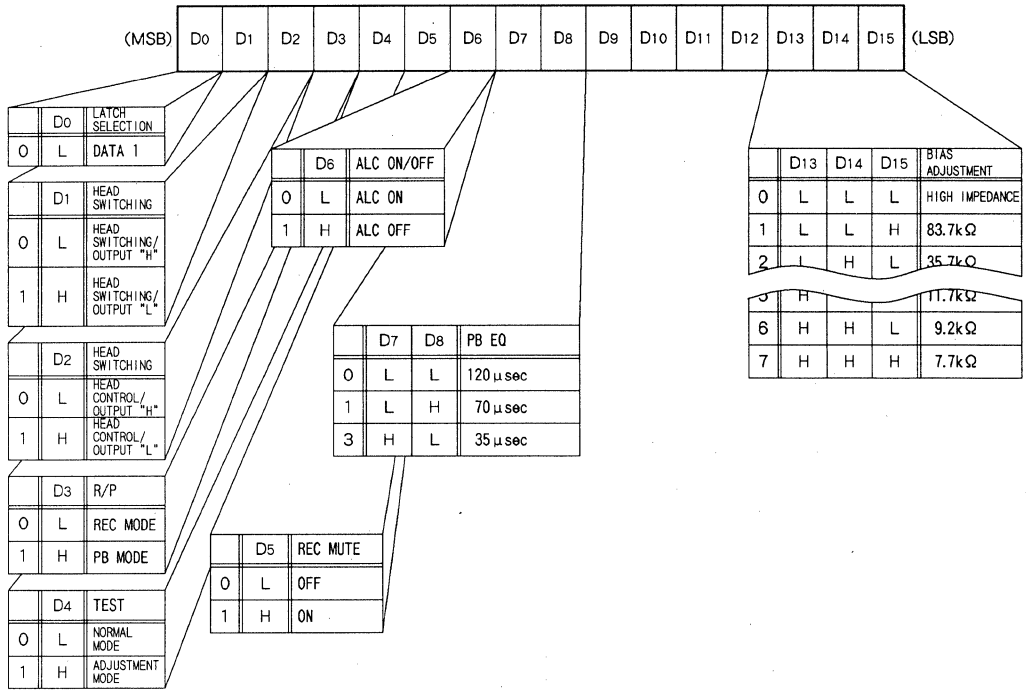
DIGITAL CONTROL SPECIFICATIONS

9-1. Data format

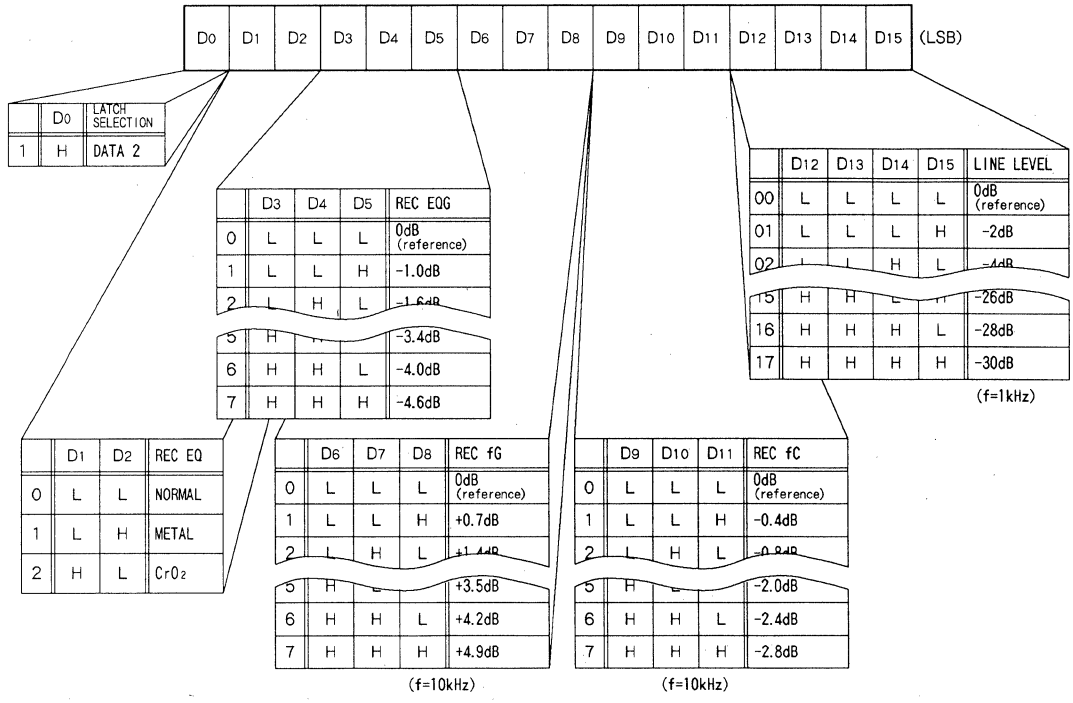


	Signal name	Function		Signal name	Function
Do	Data selection	"L" indicates data group 1	Do	Data selection	"R" indicates data group 2
D1	Head switching	"H" makes pins 7 and 36 "L"	D1	REC EQ (MSB)	D1 D2 L L ···normal L H ···metal H L ···Cr02
D2	Head control	"H" makes pins 8 and 35 "L"	D2	MODE (LSB)	
D3	R/P	"L" makes REC mode	D3	REC EQG (MSB)	REC EQ gain control : 0~7 (8steps)
D4	TEST	"H" connects line input to test input	D4		
D5	REC MUTE	"H" turns REC and MUTE on	D5	(LSB)	
D6	ALC ON/OFF	"H" turns ALC off	D6	REC fG (MSB)	REC fG control : 0~7 (8steps)
D7	PB EQ	D7 D8 L L ···normal L H ···metal/double speed normal H L ···double speed metal	D7		
D8			D8	(LSB)	
D9	(Undefined)	D9 D10 D11 D12 L L L L	D9	REC fC (MSB)	REC fC control : 0~7 (8steps)
D10			D10		
D11			D11	(LSB)	
D12			D12	LINE LEVEL (MSB)	LINE LEVEL control : 0~F (16steps)
D13	Bias adjustment (MSB)	AC bias control resistance volume : 0~7(8steps)	D13		
D14			D14		
D15	(LSB)		D15	(LSB)	

[Reference] Data group 1 data setting chart



[Reference] Data group 2 data setting chart



9-2. Data setting table (Indicated here are design values)

PB EQ MODE

	D_7	D_8	PB EQ MODE
0	L	L	Normal
1	L	H	Metal/double speed normal
2	H	L	Double speed metal

BIAS ADJUSTMENT

	D_{13}	D_{14}	D_{15}	BIAS ADJUSTMENT
0	L	L	L	High impedance
1	L	L	H	84.5kΩ
2	L	H	L	35.7kΩ
3	L	H	H	22.3kΩ
4	H	L	L	15.6kΩ
5	H	L	H	11.7kΩ
6	H	H	L	9.2kΩ
7	H	H	H	7.7kΩ

REC EQ MODE

	D_1	D_2	REC TAPE MODE	LEVEL
0	L	L	Normal	5.6dB
1	L	H	METAL	9.6dB
2	H	L	CrO_2	8.0dB

(f = 1kHz)

REC EQG

	D_3	D_4	D_5	REC G
0	L	L	L	0dB(reference)
1	L	L	H	− 1.0dB
2	L	H	L	− 1.6dB
3	L	H	H	− 2.2dB
4	H	L	L	− 2.8dB
5	H	L	H	− 3.4dB
6	H	H	L	− 4.0dB
7	H	H	H	− 4.6dB

REC fG

	D_6	D_7	D_8	REC fG
0	L	L	L	0dB(reference)
1	L	L	H	+ 0.7dB
2	L	H	L	+ 1.4dB
3	L	H	H	+ 2.1dB
4	H	L	L	+ 2.8dB
5	H	L	H	+ 3.5dB
6	H	H	L	+ 4.2dB
7	H	H	H	+ 4.9dB

(f = 10kHz)

REC fC

	D_9	D_{10}	D_{11}	REC fC
0	L	L	L	0dB(reference)
1	L	L	H	− 0.4dB
2	L	H	L	− 0.8dB
3	L	H	H	− 1.2dB
4	H	L	L	− 1.6dB
5	H	L	H	− 2.0dB
6	H	H	L	− 2.4dB
7	H	H	H	− 2.8dB

(f = 10kHz)

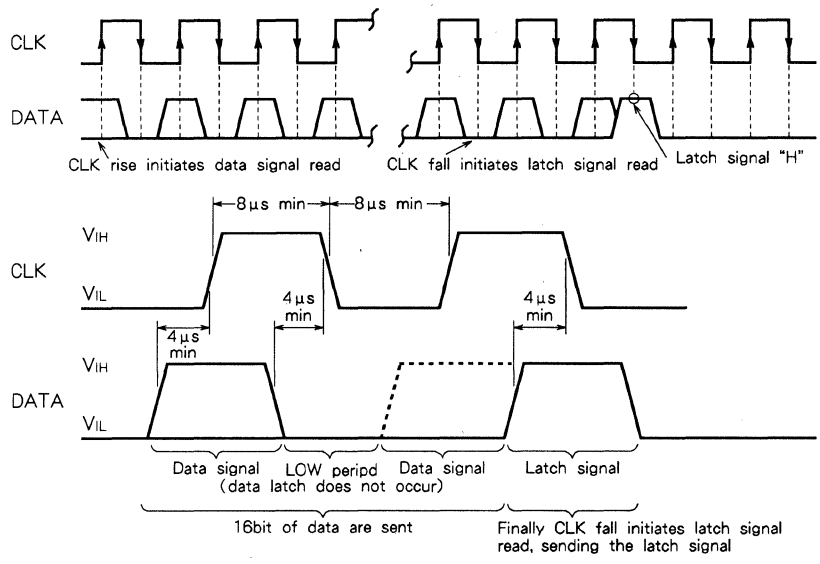
LINE LEVEL

	D_{12}	D_{13}	D_{14}	D_{15}	LINE LEVEL
0	L	L	L	L	0dB(reference)
1	L	L	L	H	− 2dB
2	L	L	H	L	− 4dB
3	L	L	H	H	− 6dB
4	L	H	L	L	− 8dB
5	L	H	L	H	− 10dB
6	L	H	H	L	− 12dB
7	L	H	H	H	− 14dB
8	H	L	L	L	− 16dB
9	H	L	L	H	− 18dB
A	H	L	H	L	− 20dB
B	H	L	H	H	− 22dB
C	H	H	L	L	− 24dB
D	H	H	L	H	− 26dB
E	H	H	H	L	− 28dB
F	H	H	H	H	− 30dB

(f = 1kHz)

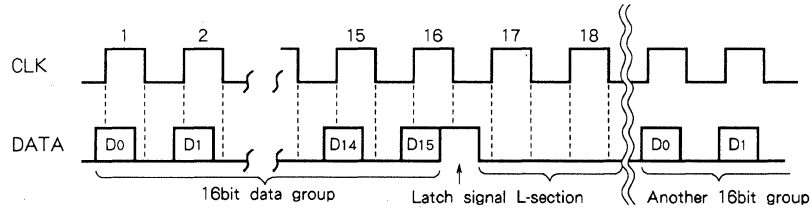
9-3. Data timing (Recommended conditions)

* Data commuication conforms to "MSB first."



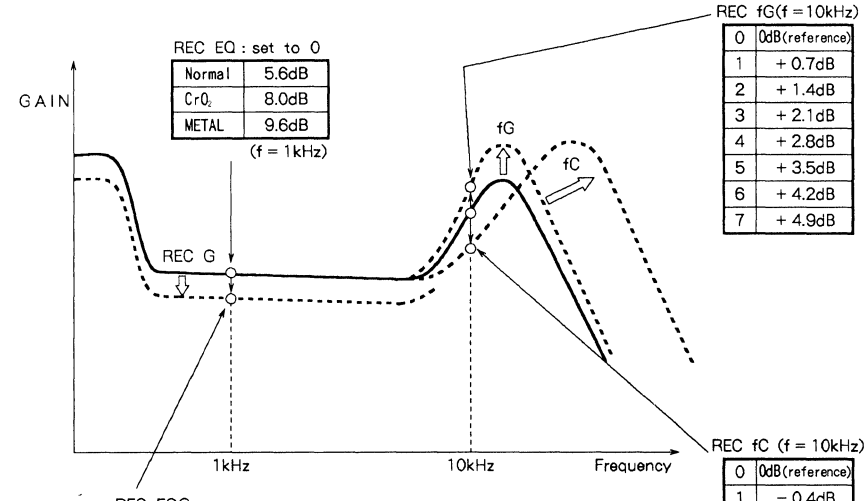
Note : Set V_{IL} and V_{IH} for CLK and DATA input so as to be within the range from GND to V_{CC}

9-4. Data communication specifications



After sending a 16bit data group, make sure to send signal "L", the data signal between two clocks.

[REFERENCE] REQ EQ characterostocs



REC fG(f = 10kHz)

0	0dB(reference)
1	+ 0.7dB
2	+ 1.4dB
3	+ 2.1dB
4	+ 2.8dB
5	+ 3.5dB
6	+ 4.2dB
7	+ 4.9dB

REC fC (f = 10kHz)

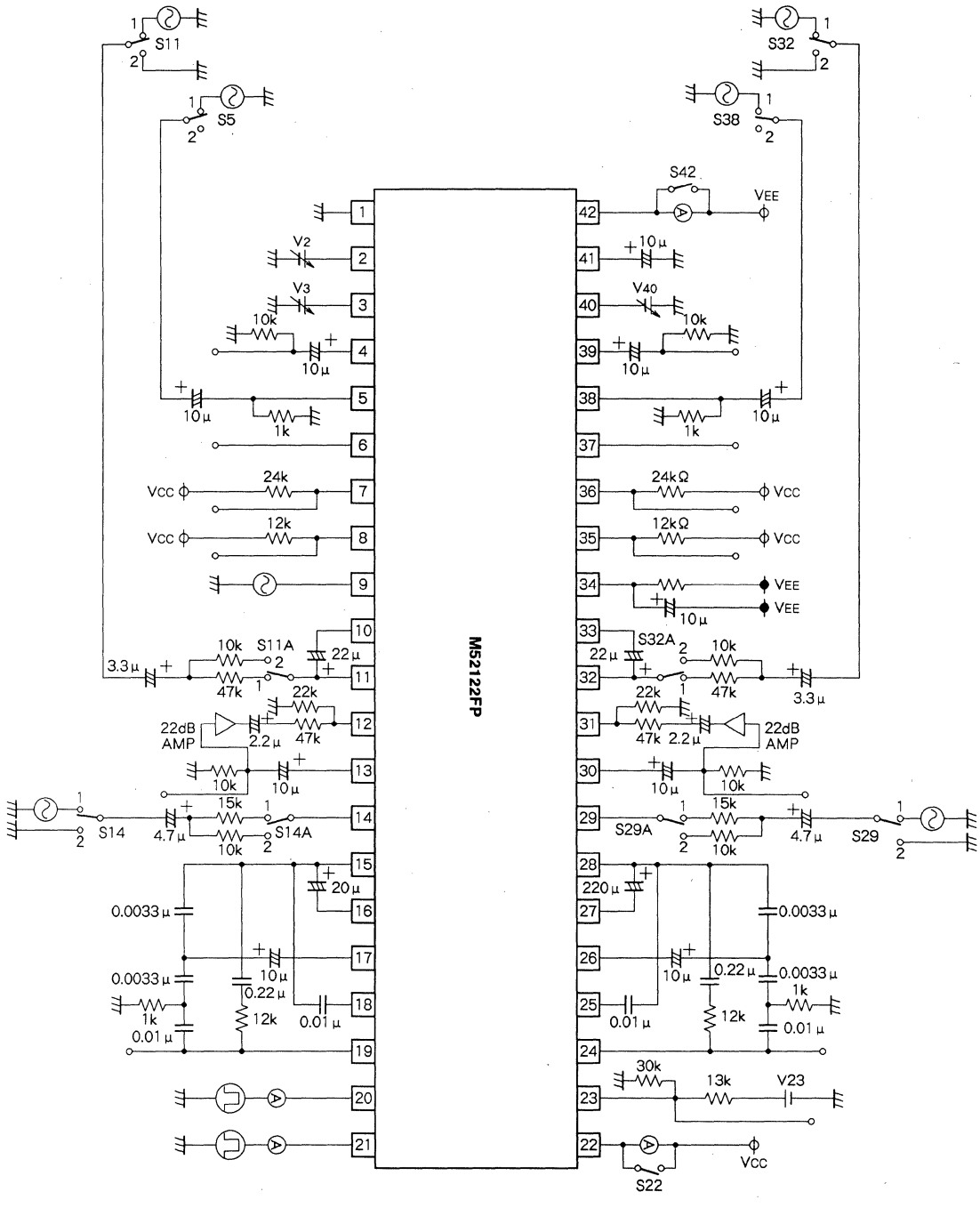
0	0dB(reference)
1	− 0.4dB
2	− 0.8dB
3	− 1.2dB
4	− 1.6dB
5	− 2.0dB
6	− 2.4dB
7	− 2.8dB

REC EQG

0	0dB(reference)
1	1.0dB
2	− 1.6dB
3	2.2dB
4	− 2.8dB
5	3.4dB
6	− 4.0dB
7	− 4.6dB

(f = 1kHz)

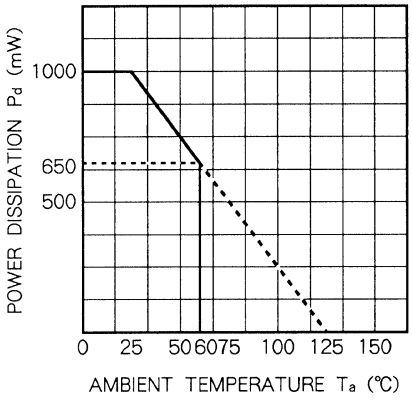
TEST CIRCUIT



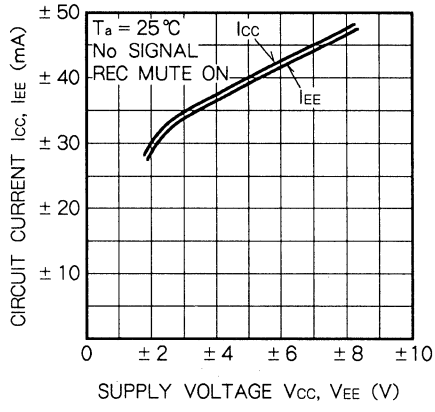
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

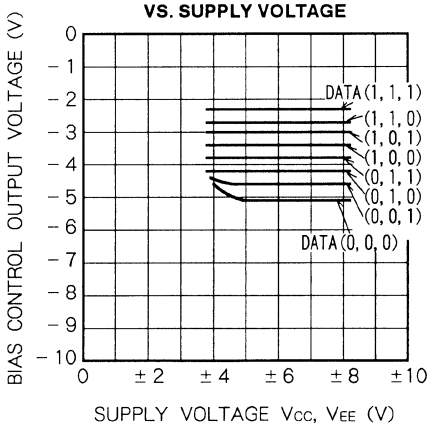
THERMAL DERATING



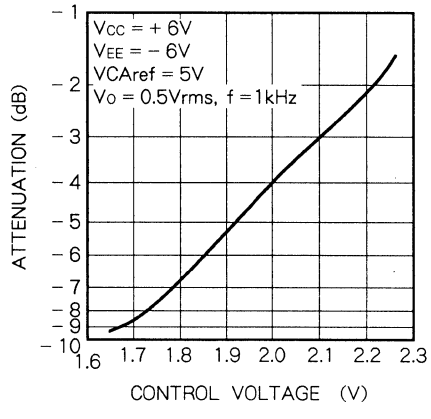
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



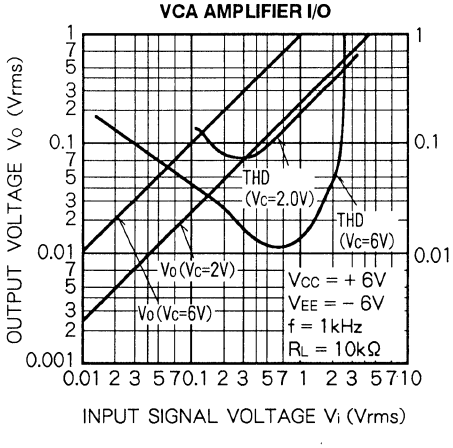
BIAS CONTROL OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



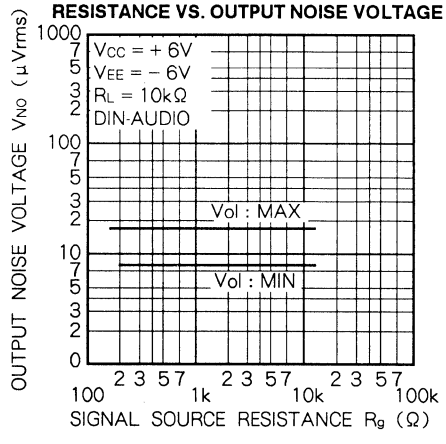
VCA CONTROL VOLTAGE VS. ATTENUATION



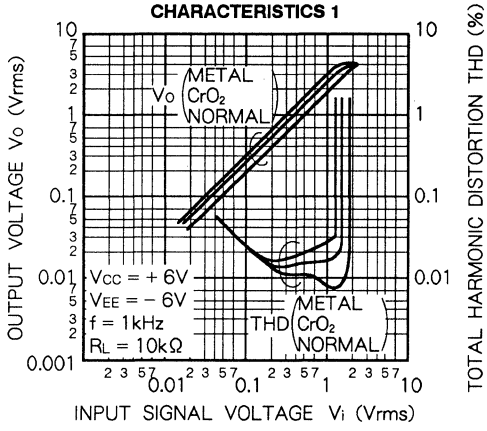
VCA AMPLIFIER I/O



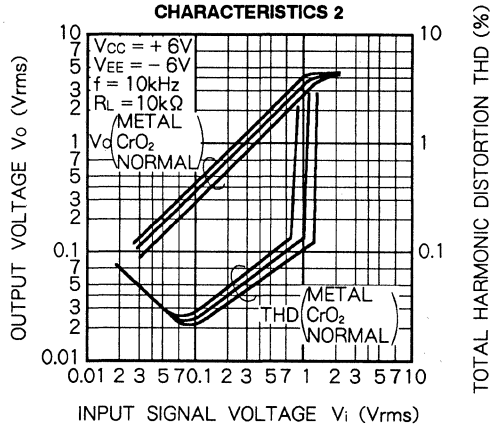
VCA AMPLIFIER SIGNAL SOURCE RESISTANCE VS. OUTPUT NOISE VOLTAGE



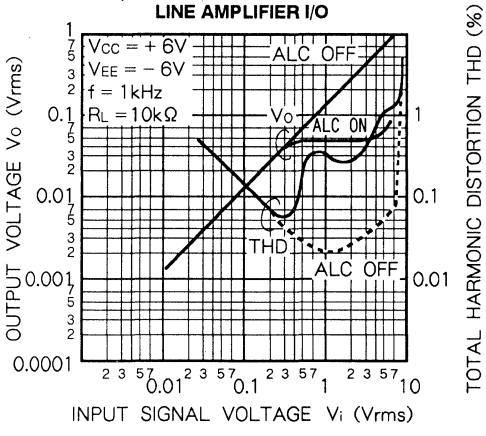
REC AMPLIFIER I/O CHARACTERISTICS 1



REC AMPLIFIER I/O CHARACTERISTICS 2



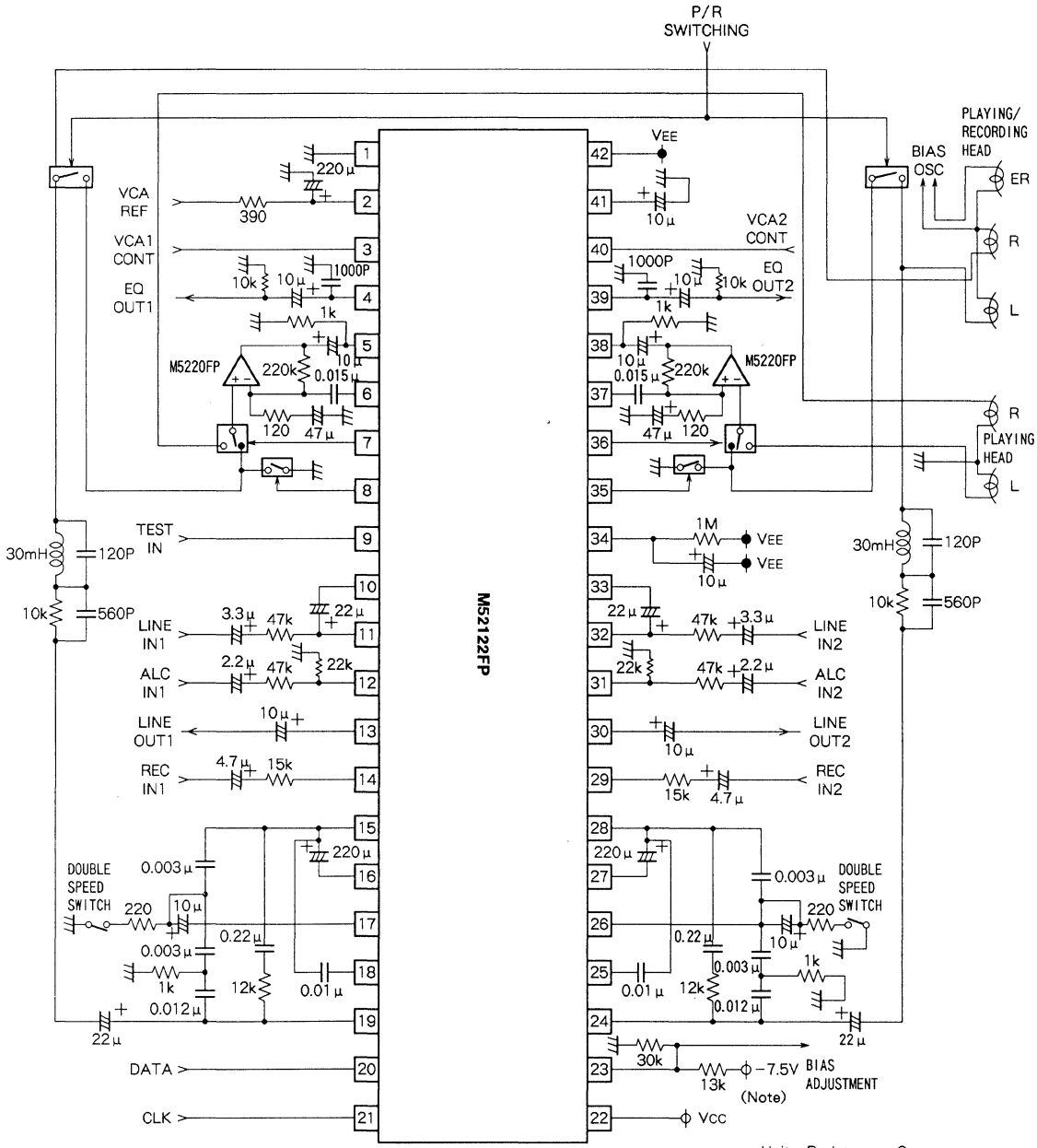
LINE AMPLIFIER I/O



M52122FP

AUTOMATIC ADJUSTMENT-PROVIDED RECORDING AND PLAYING PREAMPLIFIER

APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

Note : Set the resistance and bias adjustment power source voltage so that pin23 terminal voltage is VEE or greater.

M62451FP

AUTOMATIC ADJUSTMENT-PROVIDED RECORDING AND PLAYING PREAMPLIFIER

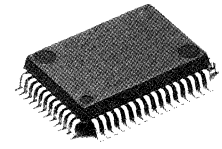
DESCRIPTION

The M62451FP is a single chip preamplifier for recording and playing on dual cassette recorders.

With the low-noise playing preamplifier and various circuits for automatic adjustment incorporated, including playing level and recording equalizer characteristics adjustments, the IC streamlines the production line of stereo set and radio cassette units, eliminating convetional adjustment processes.

FEATURES

- Controls based on 16-bit serial data from the micro-computer
- Uses the two-line communication system (DATA, CLK)
- Built-in the low-noise playing preamplifier with the function of tape mode selection
- Built-in the electronic volume to adjust playing output
- Built-in the recording amplifier capable of microcomputerized fine adjustment of characteristics (recording equalizer characteristics and recording level adjustment).
- Built-in the line amplifier with ALC function possible to use the noise reduction IC (the amplifier provided with the ATT circuit for line input level adjustment as well)
- Built-in the voltage output circuit for bias adjustment (in eight steps)



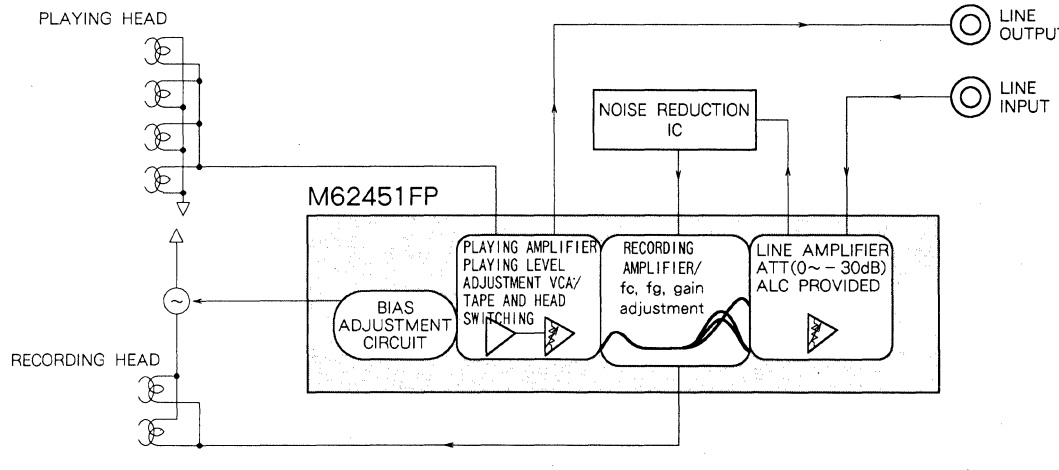
Outline 56P6N-A

0.8mm pitch QFP
(14.0mm × 10.0mm × 2.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC}, V_{EE} = ± 5.5~7.0V
Rated supply voltage ..... V_{CC}, V_{EE} = ± 6.0V
Rated power dissipation 480mW

SYSTEM CONFIGURATION

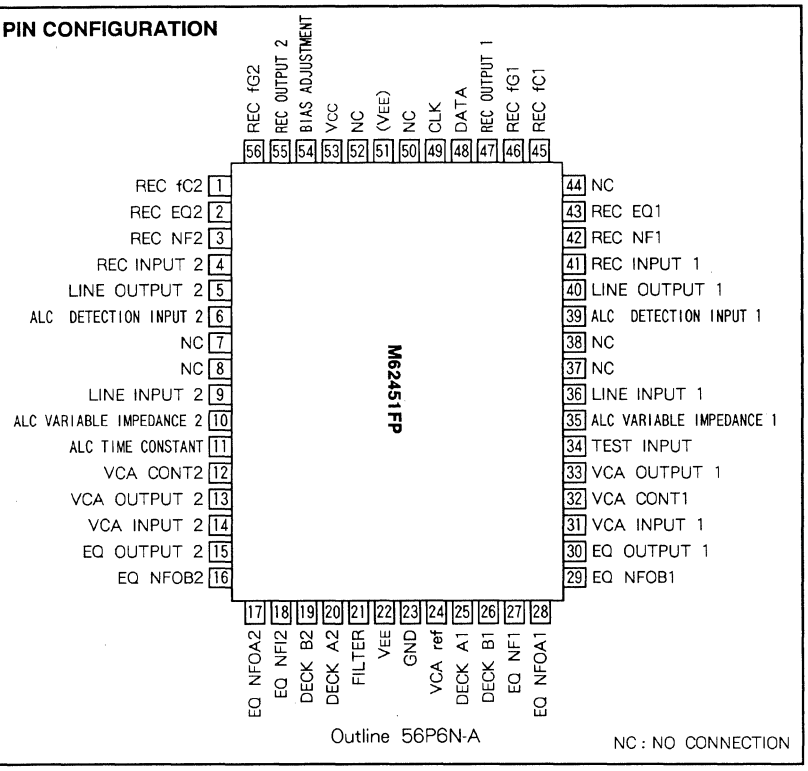


MITSUBISHI ELECTRIC

M62451FP

AUTOMATIC ADJUSTMENT-PROVIDED RECORDING AND PLAYING PREAMPLIFIER

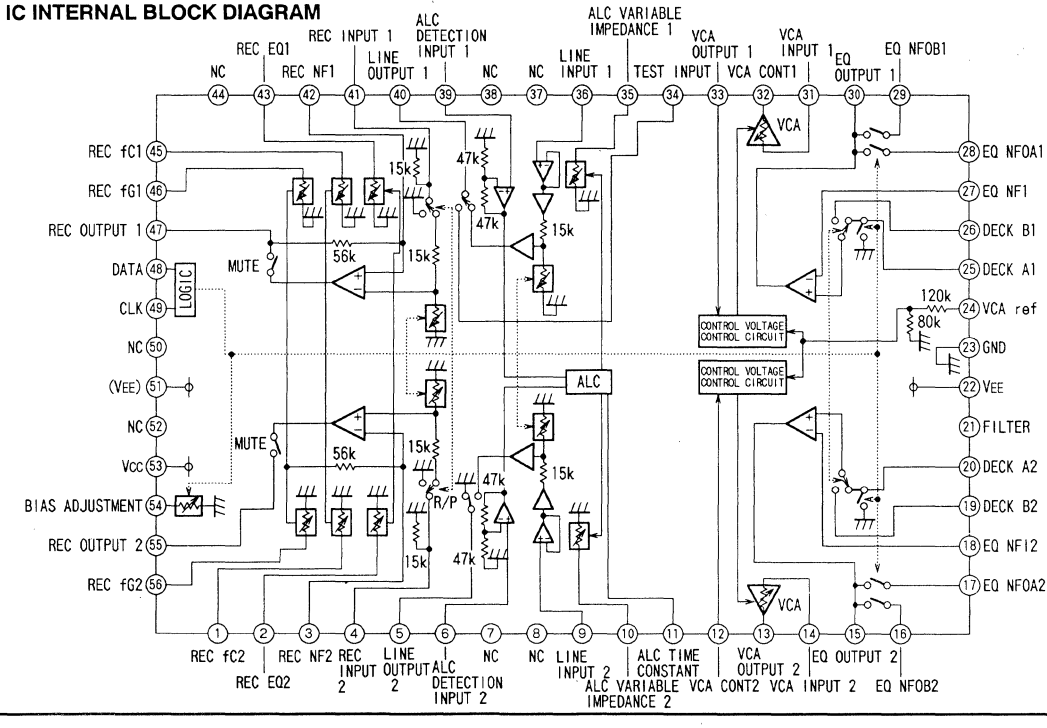
PIN CONFIGURATION



Outline 56P6N-A

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	7.5	V
V_{EE}		−7.5	V
P_d	Power dissipation	1000*Standard circuit board	mW
T_{opr}	Operating temperature	−20～+60	℃
T_{stg}	Storage temperature	−40～+125	℃

ELECTRICAL CHARACTERISTICS (V_{CC} = 6V, V_{EE} = − 6.0V, f = 1kHz, Ta = 25℃, unless otherwise noted)

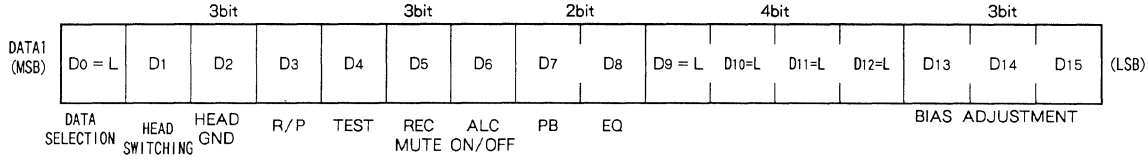
Block	Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
	I_{CC}	Circuit current 1	When no signal after power on	−	38	45	mA
	I_{EE}	Circuit current 2	When no signal after power on	− 45	− 38	−	mA
VCA amplifier	GvcEQ0	Attenuation 0	V_i = 0.5Vrms, Vc = 4.5V, VCAref = 5.0V	− 1	+ 1	+ 3	dB
	GvcEQ1	Attenuation 1	V_i = 0.5Vrms, Vc = 1.85V, VCAref = 5.0V	− 10	− 6	− 2	dB
	THDEQ	Full higher harmonics distortion factor	V_O = 0.5Vrms	−	0.05	0.4	%
	V_{OmaxE}	Maximum output voltage	When THD = 3%	1.15	1.50	−	Vrms
	Ni	Output noise voltage	BW = 20Hz～20kHz, Rg = 1kΩ	−	40	85	μVrms
	SepEQ	Separation	V_O=0.5Vrms, BW=20Hz to 20kHz, Rg=1kΩ	60	85	−	dB
PB amplifier	GvcEQ	Opened loop voltage gain	V_i = 0.05mVrms	68	80	−	dB
	GvcEQ	Closed loop voltage gain	V_O = 0.5Vrms, f = 315Hz, normal	46	49	52	dB
	THDEQ	Full higher harmonic distortion factor	V_O = 0.5Vrms, f = 1kHz, normal	−	0.05	0.4	%
	V_{OmaxE}	Maximum output voltage	When THD = 3%	1.15	1.50	−	Vrms
	Ni	Input-converted noise voltage	BW = 20Hz to 20kHz, Rg = 1kΩ	−	0.8	1.2	μVrms
	SepEQ	Separation	V_O=0.5Vrms, BW=20Hz to 20kHz, Rg=1kΩ	60	85	−	dB
REC amplifier	GvcRec	Closed loop voltage gain	V_O=0.5Vrms, normal condition, gain set to max	4.4	5.6	6.8	dB
	THDRec	Full higher harmonics distortion factor	V_O = 0.5Vrms, f = 1kHz, normal	−	0.01	0.1	%
	V_{OmaxR}	Maximum output voltage	When THD = 3%	1.9	2.4	−	Vrms
	NoRec	Output noise voltage	BW = 20Hz to 20kHz, Rg = 10kΩ	−	35	70	μVrms
	SepRec	Separation	V_O=0.5Vrms, BW=20Hz to 20kHz, Rg=10kΩ	50	75	−	dB
ALC	VoALC	ACL output voltage	When ALC level at start + 10dB	40.0	49.0	58.0	mVrms
	THDALC	ALC distortion factor	When ALC level at start + 10dB	−	0.5	1.5	%
	AALC	ALC range	Input level range during ALC on	22	27	−	dB
LINE amplifier	GvcLIN	Closed loop voltage gain	V_O=0.5Vrms, ALC off, gain set to max	− 14	− 12	− 10	dB
	THDLIN	Full higher harmonics distortion factor	V_O=0.5Vrms, ALC off, gain set to max	−	0.01	0.1	%
	V_{OmaxL}	Maximum output voltage	When THD = 3%	1.15	1.5	−	Vrms
	NoLIN	Output noise voltage	BW = 20Hz to 20kHz, Rg = 10kΩ	−	15	70	μVrms
	SepLIN	Separation	V_O=0.5Vrms, BW=20Hz to 20kHz, Rg=10kΩ	50	75	−	dB
LOGIC input	ICH	CLK input current	VCH = 5V	− 1	0	+ 1	μA
	ICL		VCL = 0V	− 1	0.05	+ 1	μA
	IDH	DATA input current	VDH = 5V	− 1	0	+ 1	μA
	IDL		VDL = 0V	− 1	0.05	+ 1	μA
	VCH	CLK H-level voltage	Recommended conditions	3.5	5.0	Vcc	V
	VCL	CLK L-level voltage	Recommended conditions	GND	0	1.0	V
	VDH	DATA H-level voltage	Recommended conditions	3.5	5.0	Vcc	V
	VDL	DATA L-level voltage	Recommended conditions	GND	0	1.0	V
	Sclk	CLK operation speed		−	50	100	kHz
	tsh	DATA setting time H	Time from data setting until CLK become "H"	2.5	−	−	μsec
	tsl	DATA setting time L	Time from data setting until CLK become "L"	2.5	−	−	μsec

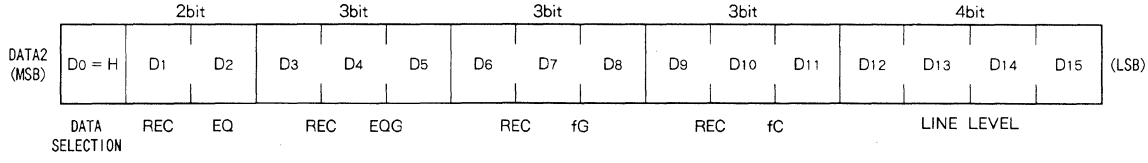
ELECTRICAL CHARACTERISTICS (Cont.)

Block	Symbol	Parameter	Test conditions	Limits			Unit
				Min	Typ	Max	
REC amplifier control	RecG1	Rec gain control 1	For data 2,(D3,D4,D5)=(1,0,0),GVCRec reference	− 3.5	− 2.8	− 2.1	dB
	RecG2	Rec gain control 2	For data 2,(D3,D4,D5)=(1,1,1), GVCRec reference	− 5.3	− 4.6	− 3.9	dB
	RecfG1	Rec fG control 1	For data 2,(D6,D7,D8)=(1,0,0),f=10kHz reference	+ 2.1	+ 2.8	+ 3.5	dB
	RecfG2	Rec fG control 2	For data 2,(D6,D7,D8)=(1,1,1),f=10kHz reference	+ 4.2	+ 4.9	+ 5.6	dB
	RecfC1	Rec fC control 1	For data 2, (D9, D10, D11)=(1, 0, 0), f=10kHz reference	− 2.3	− 1.6	− 0.9	dB
	RecfC2	Rec fC control 2	For data 2, (D9, D10, D11)=(1, 1, 1), f=10kHz reference	− 3.5	− 2.8	− 2.1	dB
	GvcRME	Rec gain metal	For data 2,(D1, D2)=(0, 1)Vo=0.5Vrms f=1kHz	8.7	9.5	10.3	dB
	GvcCr0	Rec gain Cr02	For data 2,(D1, D2)=(1, 0) Vo=0.5Vrms f=1kHz	7.0	7.8	8.6	dB
	GvcR/P	Rec R/P operation	For data 1, output ratio between when D3=0 and D3=1	50	70	−	dB
	GvcMUTE	Rec output muted operation	For data 1, output ratio between when D5=0 and D5=1	60	80	−	dB
LINE amplifier control	GvcTEST	Test input operation	For data 1, D4=1, Vo=0.5Vrms, f=1kHz	− 1	0	+ 1	dB
	GvcLC1	Line level control 1	For data 2, (D12, D13, D14, D15)=(0, 1, 1, 1)	− 16	− 14	− 12	dB
	GvcLC2	Line level control 2	For data 2, (D12, D13, D14, D15)=(1, 1, 1, 1)	− 32	− 30	− 28	dB
AC bias control	Rbias1	AC bias control resistance 1	For data 1,(D13,D14,D15)=(0,0,1)	67.0	84.5	103	kΩ
	Rbias2	AC bias control resistance 2	For data 1,(D13,D14,D15)=(1,0,0)	12.4	15.6	18.8	kΩ
	Rbias3	AC bias control resistance 3	For data 1,(D13,D14,D15)=(1,1,1)	6.1	7.7	9.3	kΩ

DIGITAL CONTROL SPECIFICATIONS

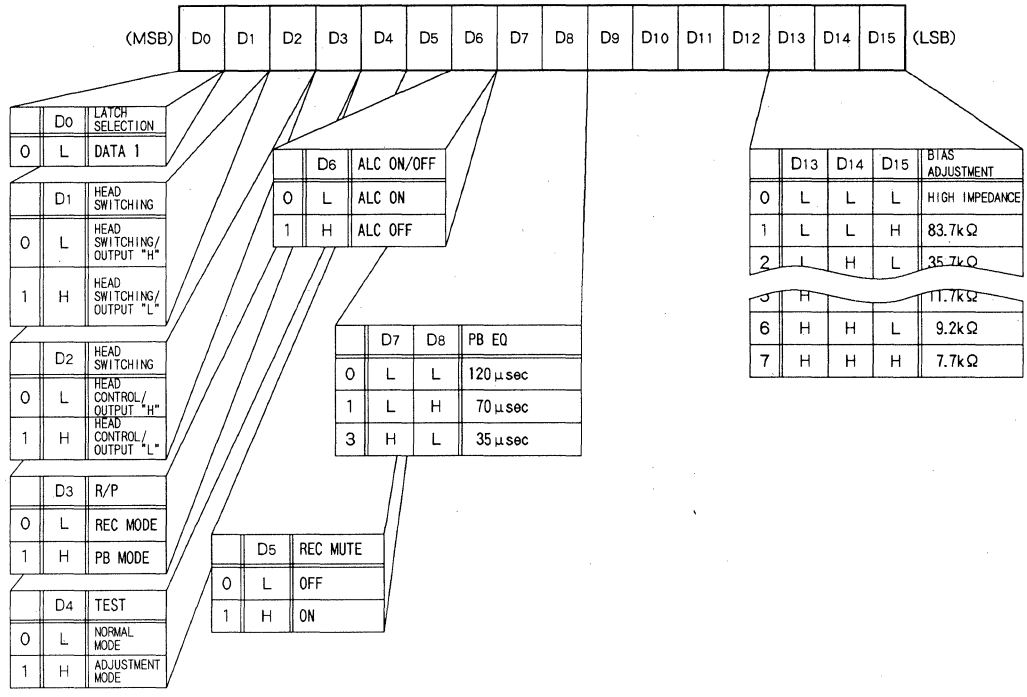
1-1. Data format



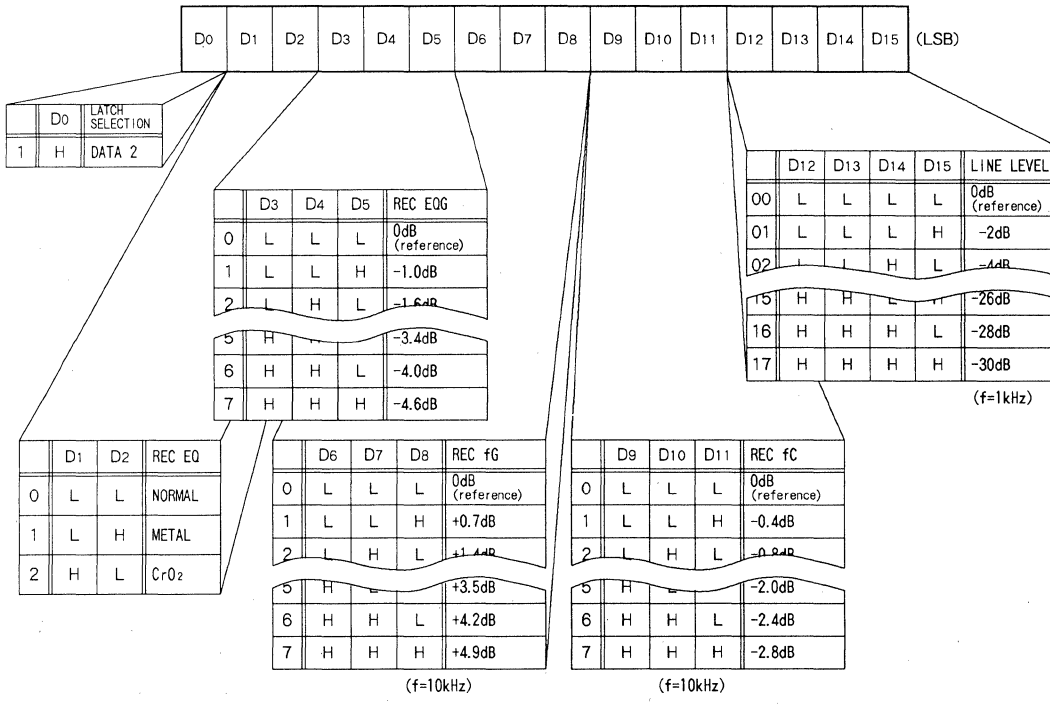


	Signal Name	Function		Signal Name	Function
D0	Data selection	"L" indicates data group 1	D0	Data selection	"R" indicates data group 2
D1	Head switching	"H" turns playing amplifier input to deck B	D1	REC EQ (MSB)	D1 D2 L L ···normal L H ···metal H L ···Cr02
D2	Head control	"H" turns deck A input to GND	D2	MODE (LSB)	
D3	R/P	"L" makes REC mode	D3	REC EQG (MSB)	REC EQ gain control : 0~7 (8steps)
D4	TEST	"H" connects line input to test input	D4		
D5	REC MUTE	"H" turns REC and MUTE on	D5	(LSB)	
D6	ALC ON/OFF	"H" turns ALC off	D6	REC fG (MSB)	REC fG control : 0~7 (8steps)
D7	PB EQ	D7 D8 L L ···normal L H ···metal/double speed normal H L ···double speed metal	D7		
D8			D8	(LSB)	
D9	(Undefined)	D9 D10 D11 D12 L L L L	D9	REC fC (MSB)	REC fC control : 0~7 (8steps)
D10			D10		
D11			D11	(LSB)	
D12			D12	LINE LEVEL (MSB)	LINE LEVEL control : 0~F (16steps)
D13	Bias adjustment (MSB)	AC bias control resistance volume : 0~7(8steps)	D13		
D14			D14		
D15	(LSB)		D15	(LSB)	

[Reference] Data group 1 data setting chart



[Reference] Data group 2 data setting chart



1-2. Data setting table (Indicated here are design values)

PB EQ MODE

	D_7	D_8	PB EQ MODE
0	L	L	Normal
1	L	H	Metal/double speed normal
2	H	L	Double speed metal

BIAS ADJUSTMENT

	D_{13}	D_{14}	D_{15}	BIAS ADJUSTMENT
0	L	L	L	High impedance
1	L	L	H	84.5kΩ
2	L	H	L	35.7kΩ
3	L	H	H	22.3kΩ
4	H	L	L	15.6kΩ
5	H	L	H	11.7kΩ
6	H	H	L	9.2kΩ
7	H	H	H	7.7kΩ

REC EQ MODE

	D_1	D_2	REC TAPE MODE	LEVEL
0	L	L	Normal	5.6dB
1	L	H	METAL	9.6dB
2	H	L	CrO_2	8.0dB

(f = 1kHz)

REC EQG

	D_3	D_4	D_5	REC G
0	L	L	L	0dB(reference)
1	L	L	H	− 1.0dB
2	L	H	L	− 1.6dB
3	L	H	H	− 2.2dB
4	H	L	L	− 2.8dB
5	H	L	H	− 3.4dB
6	H	H	L	− 4.0dB
7	H	H	H	− 4.6dB

REC fG

	D_6	D_7	D_8	REC fG
0	L	L	L	0dB(reference)
1	L	L	H	+ 0.7dB
2	L	H	L	+ 1.4dB
3	L	H	H	+ 2.1dB
4	H	L	L	+ 2.8dB
5	H	L	H	+ 3.5dB
6	H	H	L	+ 4.2dB
7	H	H	H	+ 4.9dB

(f = 10kHz)

LINE LEVEL

	D_{12}	D_{13}	D_{14}	D_{15}	LINE LEVEL
0	L	L	L	L	0dB(reference)
1	L	L	L	H	− 2dB
2	L	L	H	L	− 4dB
3	L	L	H	H	− 6dB
4	L	H	L	L	− 8dB
5	L	H	L	H	− 10dB
6	L	H	H	L	− 12dB
7	L	H	H	H	− 14dB
8	H	L	L	L	− 16dB
9	H	L	L	H	− 18dB
A	H	L	H	L	− 20dB
B	H	L	H	H	− 22dB
C	H	H	L	L	− 24dB
D	H	H	L	H	− 26dB
E	H	H	H	L	− 28dB
F	H	H	H	H	− 30dB

(f = 1kHz)

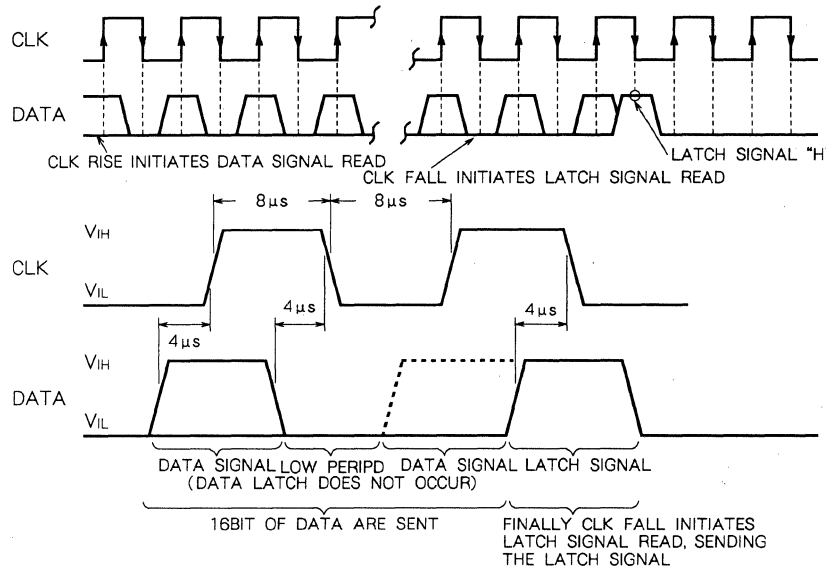
REC fC

	D_9	D_{10}	D_{11}	REC fC
0	L	L	L	0dB(reference)
1	L	L	H	− 0.4dB
2	L	H	L	− 0.8dB
3	L	H	H	− 1.2dB
4	H	L	L	− 1.6dB
5	H	L	H	− 2.0dB
6	H	H	L	− 2.4dB
7	H	H	H	− 2.8dB

(f = 10kHz)

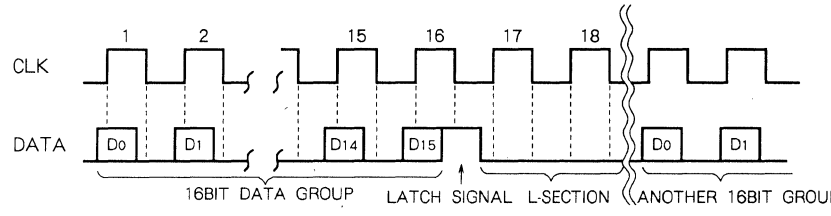
1-3. Data timing (recommended conditions)

* Data commuication conforms to "MSB first."



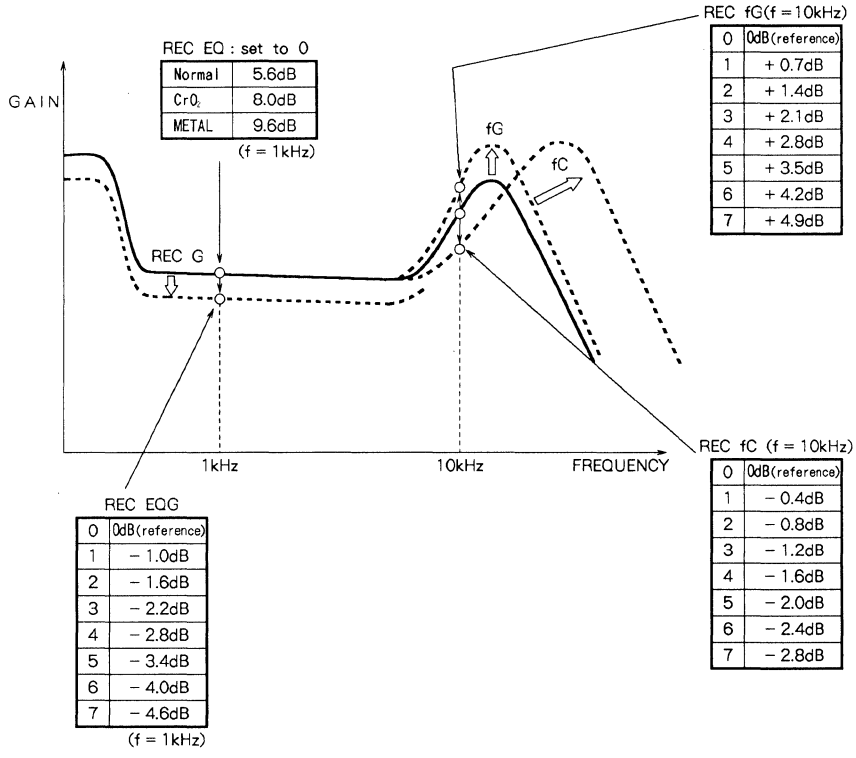
Note : Set V_{IL} and V_{IH} for CLK and DATA input so as to be within the range from GND to V_{CC}

1-4. Data communication specifications



After sending a 16bit data group, make sure to send signal "L", the data signal between two clocks.

[Reference] REQ EQ characteristics



TEST CONDITIONS

Parameter	Switching position						Voltage			Data 1	Data 2	Input terminal	Output terminal	Remark
	S5 (S38)	S11 (S32)	S11A (S32A)	S14 (S29)	S14A (S29A)	S22 (S42)	V2	V3 (V40)	V23					
Icc	2	2	2	2	2	OFF	5.0V	4.5V	-7.5V	When power is turned on			22	
IEE	2	2	2	2	2	OFF	↑	↑	↑	When power is turned on			42	
GvoEQ0	1	2	2	2	2	ON	↑	↑	↑	a0	b0	5 (38)	4 (39)	
GvoEQ1	1	2	2	2	2	↑	↑	1.9V	↑	a0	b0	↑	↑	
THDEQ	1	2	2	2	2	↑	↑	4.5V	↑	a0	b0	↑	↑	
VomaxE	1	2	2	2	2	↑	↑	↑	↑	a0	b0	↑	↑	
Ni	2	2	2	2	2	↑	↑	↑	↑	a0	b0		↑	
SepEQ	*	2	2	2	2	↑	↑	↑	↑	a0	b0	5 (29)	39 (4)	Pin 39 level when S5 is set to "1" and S38 to "2" Pin 4 level when S5 is set to "2" and S38 to "1"
GvcRec	2	2	2	1	1	↑	↑	↑	↑	a0	b0	14 (29)	19 (24)	
THDRec	2	2	2	1	1	↑	↑	↑	↑	a0	b0	↑	↑	
VomaxR	2	2	2	1	1	↑	↑	↑	↑	a0	b0	↑	↑	
NoRec	2	2	2	2	2	↑	↑	↑	↑	a0	b0		↑	
SepRec	2	2	2	*	2	↑	↑	↑	↑	a0	b0	14 (29)	24 (19)	Pin 24 level when S14 is set to "1" and S29 to "2" Pin 19 level when S14 is set to "2" and S29 to "1"
VoALC	2	1	1	2	2	↑	↑	↑	↑	a0	b0	11 (32)	13 (30)	
THDALC	2	1	1	2	2	↑	↑	↑	↑	a0	b0	↑	↑	
AALC	2	1	1	2	2	↑	↑	↑	↑	a0	b0	↑	↑	
GvcLIN	2	1	1	2	2	↑	↑	↑	↑	a6	b0	↑	↑	
THDLIN	2	1	1	2	2	↑	↑	↑	↑	a6	b0	↑	↑	
VomaxL	2	1	1	2	2	↑	↑	↑	↑	a6	b0	↑	↑	
NoLIN	2	2	2	2	2	↑	↑	↑	↑	a6	b0	↑	↑	
SepLIN	2	*	2	2	2	↑	↑	↑	↑	a6	b0	↑	30 (13)	Pin 30 level when S11 is set to "1" and S32 to "2" Pin 13 level when S11 is set to "2" and S32 to "1"
ICH	2	2	2	2	2	↑	↑	↑	↑	a0	b0		21	Pin 21 output when 5V is applied
ICL	2	2	2	2	2	↑	↑	↑	↑	a0	b0		21	Pin 21 output when 0V is applied
IDH	2	2	2	2	2	↑	↑	↑	↑	a0	b0		20	Pin 20 output when 5V is applied
IDL	2	2	2	2	2	↑	↑	↑	↑	a0	b0		20	Pin 20 output when 0V is applied
VohA/B	2	2	2	2	2	↑	↑	↑	↑	a0	b0		7 (36)	
VolA/B	2	2	2	2	2	↑	↑	↑	↑	a1	b0		7 (36)	
VohGND	2	2	2	2	2	↑	↑	↑	↑	a0	b0		8 (35)	
VolGND	2	2	2	2	2	↑	↑	↑	↑	a2	b0		8 (35)	
REQNF0	2	2	2	2	2	↑	↑	↑	↑	a0	b0	6 (37)	5 (38)	$\left\{\frac{V6(37)}{V5(38)} - 1\right\}$ kΩ
REQNF1	2	2	2	2	2	↑	↑	↑	↑	a7	b0	↑	↑	↑
REQNF2	2	2	2	2	2	↑	↑	↑	↑	a8	b0	↑	↑	↑
Rec G1	2	2	2	1	1	↑	↑	↑	↑	a0	b6	14 (29)	19 (24)	Reference : GvcRec
Rec G2	2	2	2	1	1	↑	↑	↑	↑	a0	b9	↑	↑	↑
Rec fG1	2	2	2	1	1	↑	↑	↑	↑	a0	b13	↑	↑	GvcRec (f = 10kHz) Reference : data 2 all "0"
Rec fG2	2	2	2	1	1	↑	↑	↑	↑	a0	b16	↑	↑	↑
Rec fC1	2	2	2	1	1	↑	↑	↑	↑	a0	b20	↑	↑	
Rec fC2	2	2	2	1	1	↑	↑	↑	↑	a0	b23	↑	↑	

TEST CONDITIONS

Parameter	Switching position						Voltage			Data 1	Data 2	Input terminal	Output terminal	Remark
	S5 (S38)	S11 (S32)	S11A (S32A)	S14 (S29)	S14A (S29A)	S22 (S42)	V2	V3 (V40)	V23					
GvcRME	2	2	2	2	2	ON	5.0V	4.5V	-7.5V	a0	b1	14 (29)	19 (24)	
GvcCrO	2	2	2	2	2	↑	↑	↑	↑	a0	b2	↑	↑	
GvcR/P	2	2	2	2	2	↑	↑	↑	↑	a3	b0	↑	↑	
GvcMUTE	2	2	2	2	2	↑	↑	↑	↑	a5	b0	↑	↑	
GvcTEST	2	1	1	2	2	↑	↑	↑	↑	a4	b0	9,11 (32)	13 (30)	
GvcLC1	2	1	1	2	2	↑	↑	↑	↑	a6	b13	11 (32)	13 (30)	
GvcLC2	2	1	1	2	2	↑	↑	↑	↑	a6	b29	↑	↑	
Rbias1	2	2	2	2	2	↑	↑	↑	↑	a9	b0		23	$1/\left\{\frac{7.5 - V23}{13k \cdot V23} - \frac{1}{30k}\right\}$ Ω
Rbias2	2	2	2	2	2	↑	↑	↑	↑	a12	b0		↑	↑
Rbias3	2	2	2	2	2	↑	↑	↑	↑	a15	b0		↑	↑

Data setting table (Data 1)

Mode	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	Remark
a0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Data group 1 : initial
a1		H	↓														Head switching : A→B
a2		L	H	↓													Head A : grounded
a3			L	H	↓												REC input cut off
a4				L	H	↓											LINE input : connected to test input
a5					L	H	↓										REC MUTE : on
a6						L	H		↓								ALC : off
a7							L	↓	H								Metal/double speed normal
a8								H	L							↓	Double speed metal
a9								L							↓	H	Bias adjustment : 82k
a10															H	L	40k
a11														↓	H	H	22.3k
a12														H	L	L	15.7k
a13														H	↓	H	11.8k
a14														H	H	L	9.2k
a15	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	H	H	H	7.7k

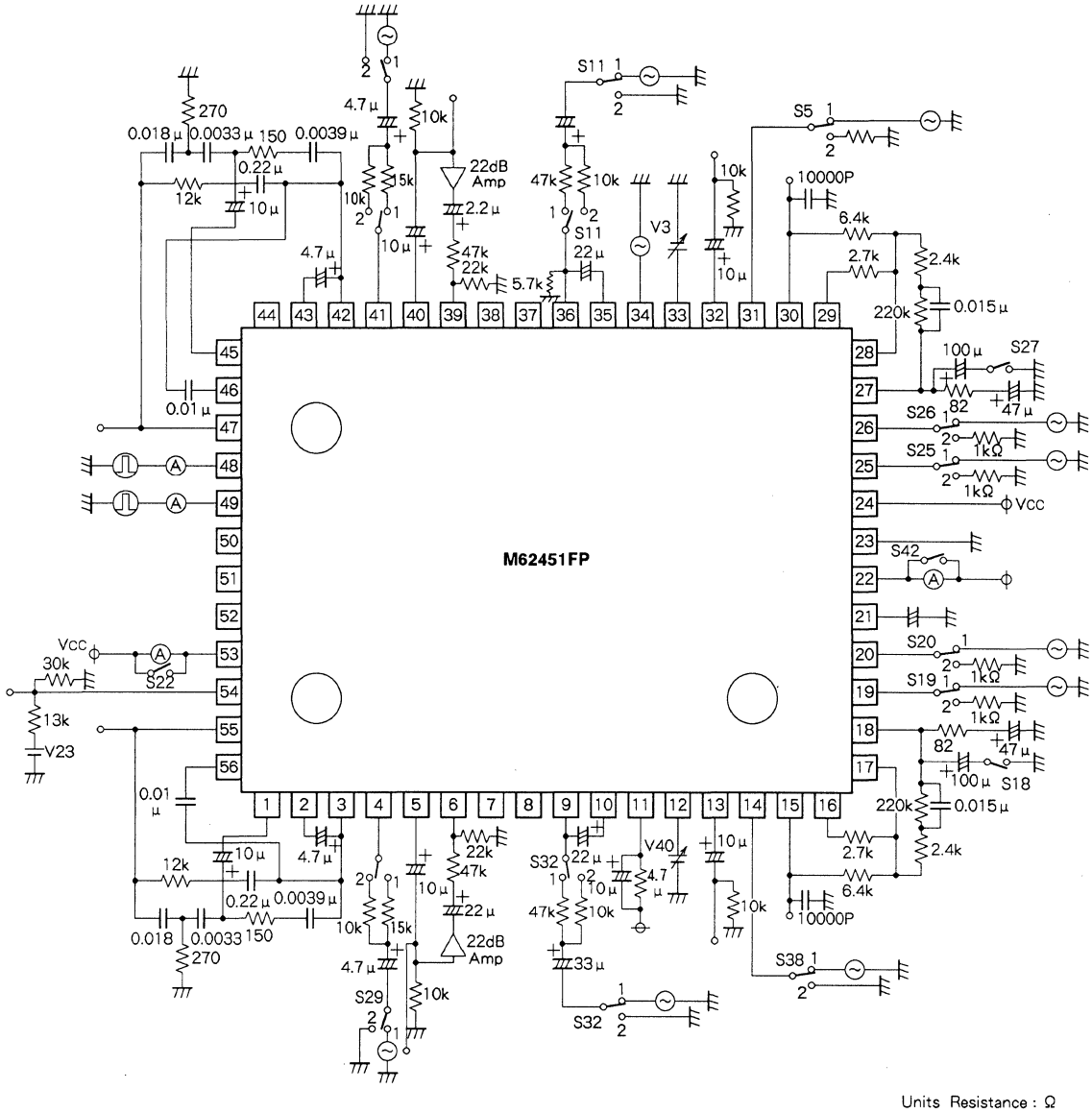
Data setting table (Data 2)

モード	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	Remark
b0	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	
b1		↓	H													H	
b2		H	L			↓									↓	H	
b3		L			↓	H									H	L	
b4					H	L									H	↓	
b5				↓	H	H									H	H	
b6				H	L	L								↓	H	H	
b7				H	↓	H								H	L	L	
b8				H	H	L								H		↓	
b9		↓		H	H	H			↓					H		H	
b10		H		L	L	L		↓	H					H	↓	H	
b11								H	L					H	H	L	
b12							↓	H	H					H	H	↓	
b13							H	L	L					H	H	H	
b14							H	↓	H				↓	H	H	H	
b15							H	H	L				H	L	L	L	
b16		↓	↓				H	H	H			↓				↓	
b17		L	H				L	L	L		↓	H				H	
b18											H	L			↓	H	
b19										↓	H	H			H	L	
b20										H	L	L			H	↓	
b21										H	↓	H			H	H	
b22										H	H	L		↓	H	H	
b23			↓			↓				H	H	H		H	L	L	
b24			L			H				L	L	H		H		↓	
b25										H	↓	L		H		H	
b26							↓	↓	↓	H	H	H		H	↓	H	
b27							H	H	H	L	L	H		H	H	L	
b28										H	↓	L	↓	H	H	↓	
b29	↓	↓	↓	↓	↓	↓	↓	↓	↓	H	H	H	H	H	H	H	

M62451FP

AUTOMATIC ADJUSTMENT-PROVIDED RECORDING AND PLAYING PREAMPLIFIER

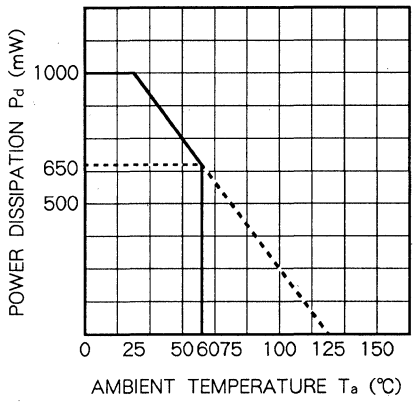
TEST CIRCUIT



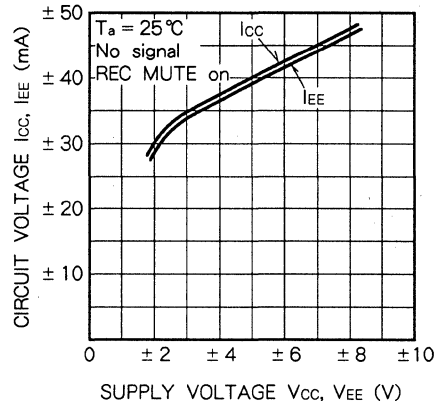
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

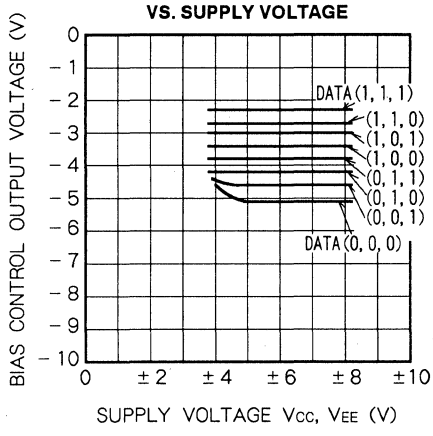
THERMAL DERATING



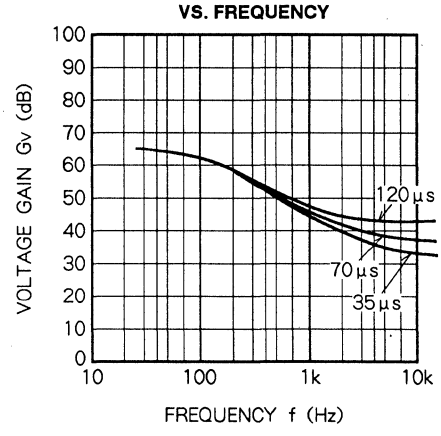
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



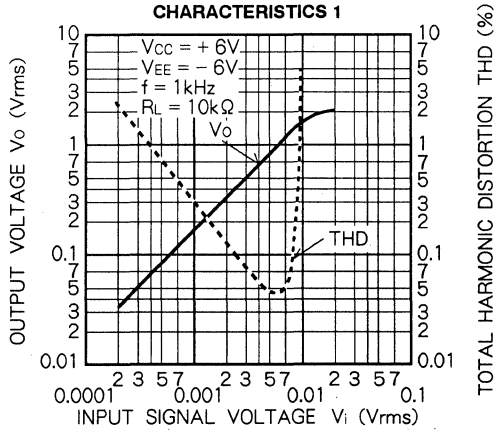
BIAS CONROL OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



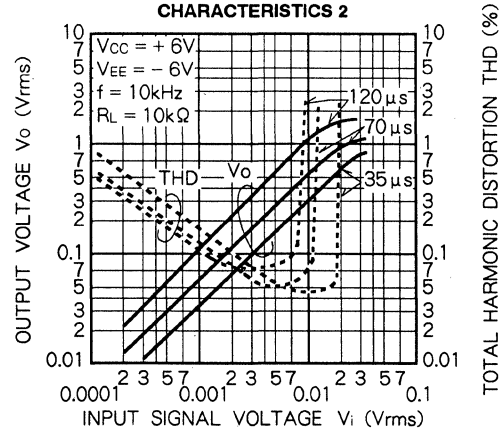
PB EQ AMPLIFIER VOLTAGE GAIN VS. FREQUENCY



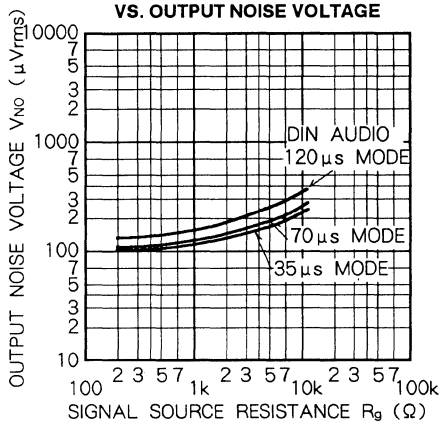
PB EQ AMPLIFIER I/O CHARACTERISTICS 1



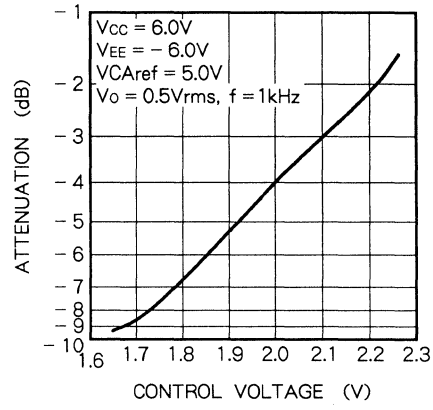
PB EQ AMPLIFIER I/O CHARACTERISTICS 2



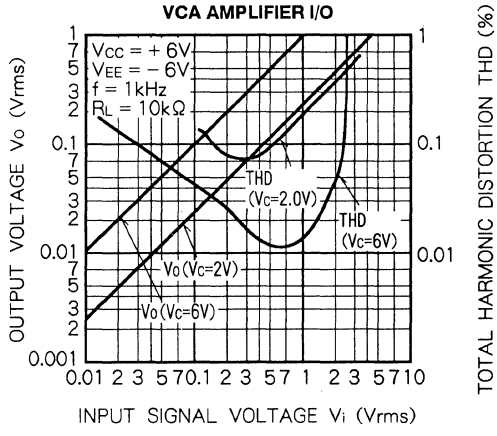
PB EQ AMPLIFIER SIGNAL SOURCE RESISTANCE VS. OUTPUT NOISE VOLTAGE



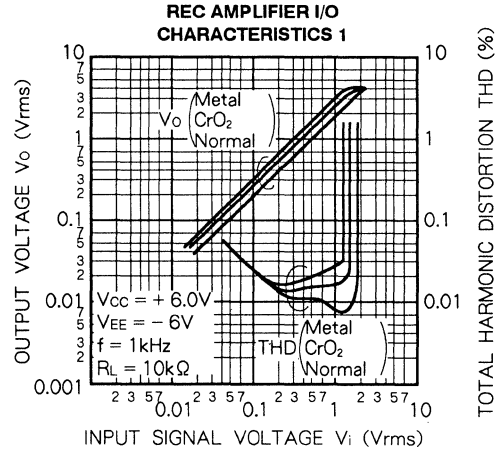
VCA CONTROL VOLTAGE VS. ATTENUATION



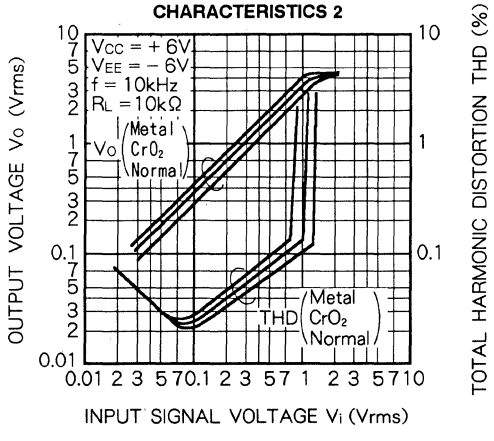
VCA AMPLIFIER I/O



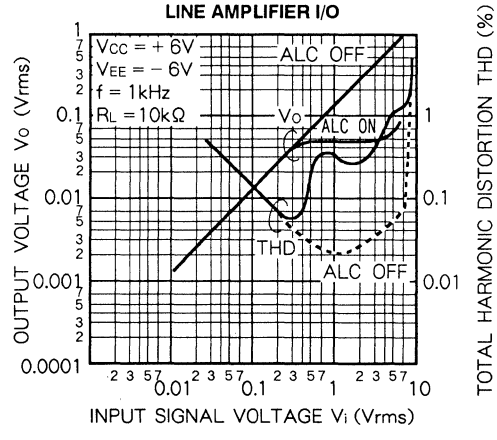
REC AMPLIFIER I/O CHARACTERISTICS 1



REC AMPLIFIER I/O CHARACTERISTICS 2



LINE AMPLIFIER I/O



M51168AP

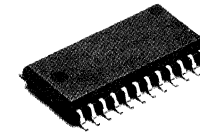
3V SINGLE CHIP, RECORD/PLAYBACK AMPLIFIER •POWER AMPLIFIER

DESCRIPTION

The M51168AP is a recording/playback preamplifier for portable audio systems. It has a built-in headphone power amplifier capable of operating at a low voltage. The IC can form a complete audio amplifier section.

FEATURES

- Built-in playback amplifier, microphone amplifier, line amplifier, ALC amplifier, ripple filter, power amplifier, and earphone amplifier.
- Internal ALC rectifier and LED driver
- Capable of making selection from playback amplifier, power amplifier, and microphone line amplifier, by means of electronic switch.
- Power amplifier and earphone amplifier selectable by electronic switch.
- Built-in battery check circuit (for recording)



Outline 24P2N-B

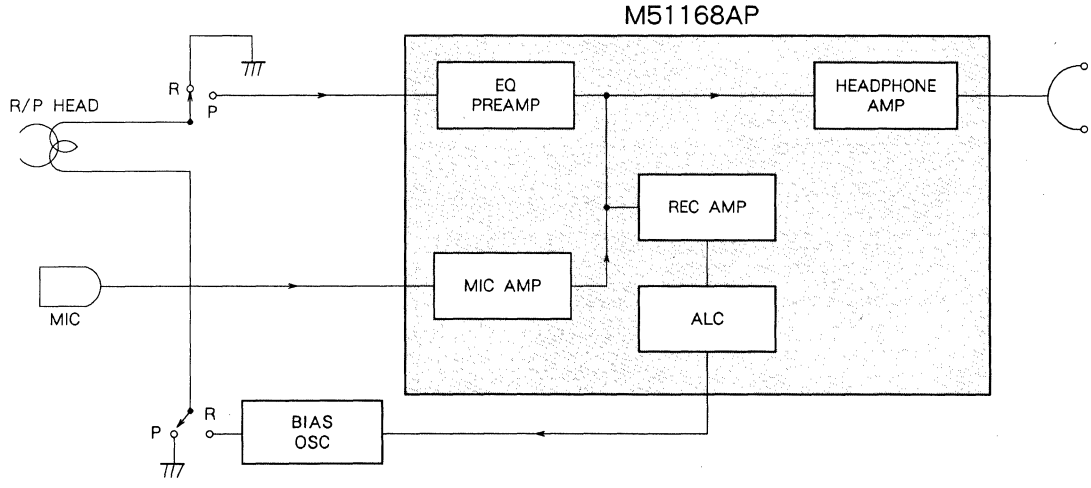
1.27mm pitch 300mil SOP
(5.3mm × 15.02mm × 1.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 1.8~4V

Rated supply voltage ..... V_{CC} = 3V

SYSTEM CONFIGURATION

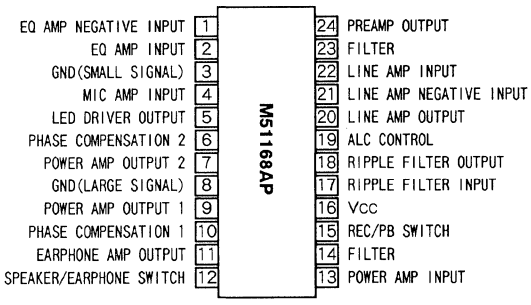


MITSUBISHI ELECTRIC

M51168AP

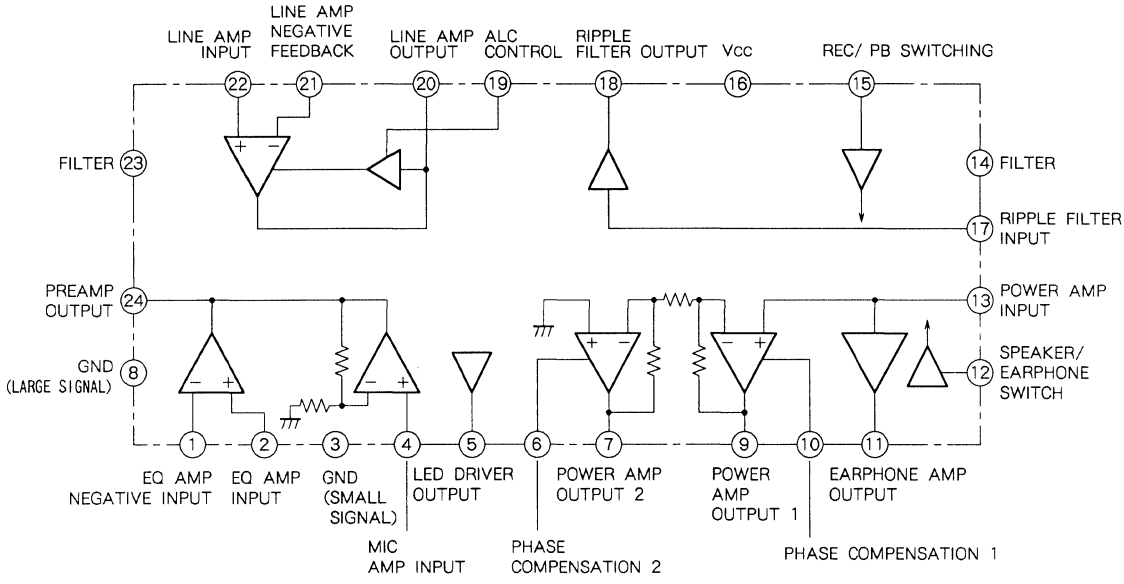
3V SINGLE CHIP, RECORD/PLAYBACK AMPLIFIER •POWER AMPLIFIER

PIN CONFIGURATION



Outline 24P2N-B

IC INTERNAL BLOCK DIAGRAM



M51168AP

3V SINGLE CHIP, RECORD/PLAYBACK AMPLIFIER •POWER AMPLIFIER

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	4.5	V
I_{CC}	Circuit current	300	mA
P_d	Power dissipation	600	mW
K_θ	Thermal derating(Ta ≧ 25℃)	6	mW/℃
T_{opr}	Operating temperature	−20～+60	℃
T_{stg}	Storage temperature	−40～+125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, f = 1kHz, unless otherwise noted)

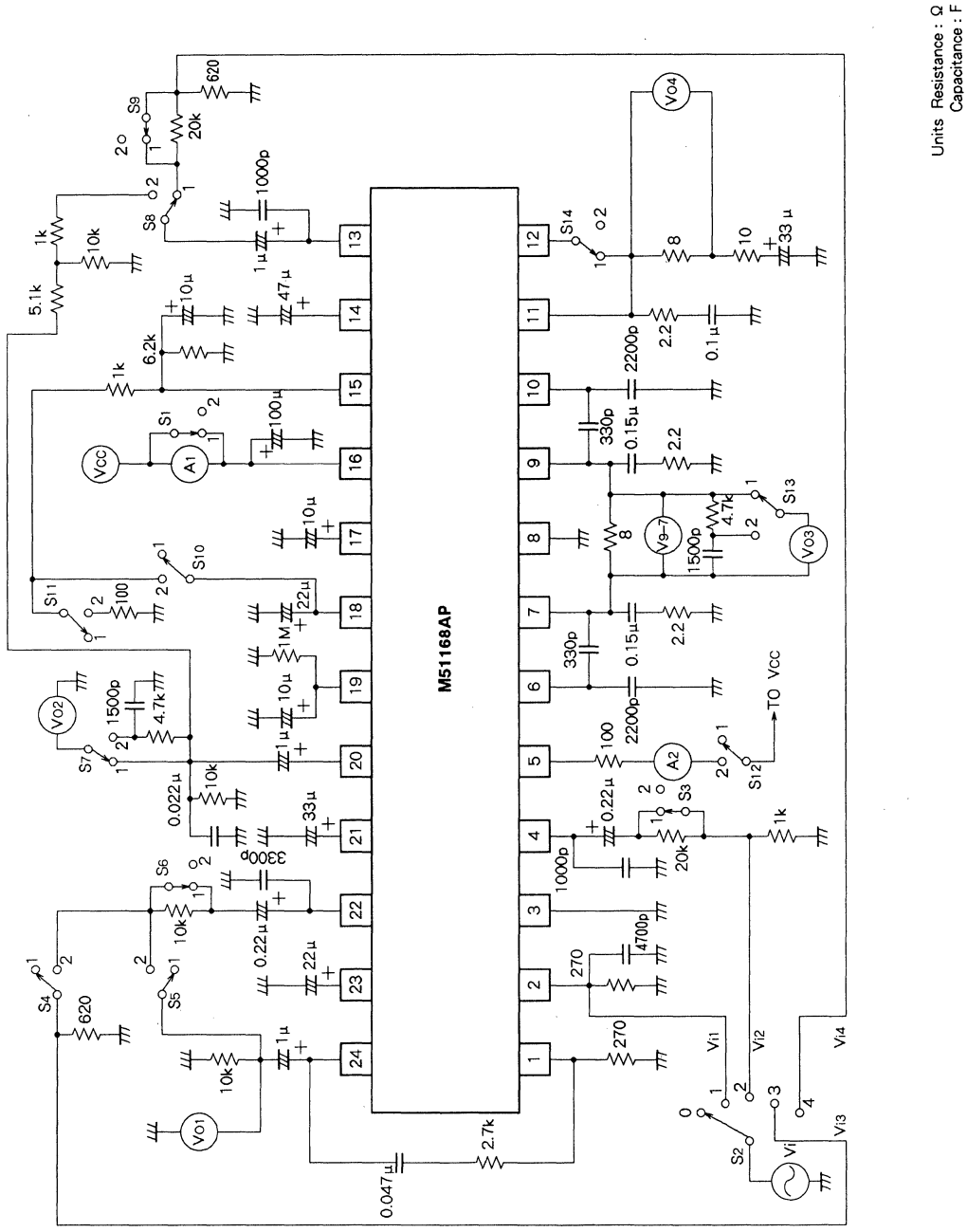
Symbol	Parameter	Test conditions					Limits			Unit
		Vcc	Input	Test point	PB/REC		Min	Typ	Max	
I_{CC1}	Circuit current (1)	3		A_1	PB	Quiescence	−	21	32	mA
I_{CC2}	Circuit current (2)	3		A_1	REC	Quiescence	−	15	23	mA
G_{a1}	Equalizer + line voltage gain	3	V_{i1}	V_{O2}	PB	V_{O2} = 0.3Vrms	62	65	67.5	dB
G_{a2}	Equalizer + line voltage attenuation	2	V_{i1}	V_{O2}	PB	V_{O2} = 0.3Vrms Comparison between G_{a2}/G_{a1}	−2	−0.5	+1	dB
THD_1	Equalizer + line total harmonic distortion	3	V_{i1}	V_{O2}	PB	V_{O2} = 0.3Vrms	−	0.7	1.5	%
G_{b1}	Microphone + line voltage gain	3	V_{i2}	V_{O2}	REC	V_{O2} = 0.1Vrms	59	62	64.5	dB
G_{b2}	Microphone + line voltage attenuation	2	V_{i2}	V_{O2}	REC	V_{O2} = 0.1Vrms Comparison between G_{b2}/G_{b1}	−2	−0.5	+1	dB
THD_2	ALC distortion	3	V_{i2}	V_{O2}	REC	V_{i2} = − 50dBv	−	0.3	1.2	%
ALC	ALC range	3	V_{i2}	V_{O2}	REC		40	46	−	dB
Z_{iM}	Microphone input impedance	3	V_{i2}	V_{O1}	REC	V_{O1} = 0.1Vrms	13	20	−	kΩ
Z_{iL}	Line input impedance	3	V_{i3}	V_{O2}	PB	V_{O2} = 0.3Vrms	20	30	−	kΩ
V_{OML}	Maximum line output voltage	3	V_{i3}	V_{O2}	PB	THD = 3%	0.65	0.85	−	V_{P-P}
G_{c1}	Power voltage gain	3	V_{i4}	V_{O3}	PB	V_{O3} = 0.3Vrms	22.5	25	27	dB
G_{c2}	Power voltage attenuation	2	V_{i4}	V_{O3}	PB	V_{O3} = 0.3Vrms Comparison between G_{c2}/G_{c1}	−1.5	0	+1.5	dB
THD_3	Power total harmonic distortion	3	V_{i4}	V_{O3}	PB	V_{O3} = 0.3Vrms	−	0.6	2.0	%
P_{OM1}	Maximum power output	3	V_{i4}	V_{O3}	PB	THD = 10%	150	250	−	mW
Z_{iP}	Power input impedance	3	V_{i4}	V_{O3}	PB	V_{O3} = 0.3Vrms	13	20	−	kΩ
V_{OFF}	Output offset voltage	3		V_{9-7}	PB	Quiescence	−60	0	+60	mV
G_{d1}	Earphone voltage gain	3	V_{i4}	V_{O4}	REC	V_{O4} = 0.1Vrms	5	7	9	dB
G_{d2}	Earphone voltage attenuation	2	V_{i4}	V_{O4}	REC	V_{O4} = 0.1Vrms Comparison between G_{d2}/G_{d1}	−1.5	0	+1.5	dB
THD_4	Earphone total harmonic distortion	3	V_{i4}	V_{O4}	REC	V_{O4} = 0.2Vrms	−	0.4	1.0	%
P_{OM2}	Maximum earphone output	3	V_{i4}	V_{O4}	REC	THD = 10%	10	14	−	mW
N_{O1}	Equalizer + line + power output noise voltage	3		V_{O3}	PB	BW=20Hz～20kHz	−	12	22	mVrms
N_{O2}	Microphone + line output noise voltage	3		V_{O2}	REC	BW=20Hz～20kHz	−	1.0	1.8	mVrms
I_5	Pin ⑤ current	3		A_2	REC	Quiescence	2	−	−	mA
B.C	Battery checker voltage			Vcc	REC	Quiescence	1.9	2.1	2.3	V

Note : PB : playback, REC : recording

M51168AP

3V SINGLE CHIP, RECORD/PLAYBACK AMPLIFIER •POWER AMPLIFIER

TEST CIRCUIT



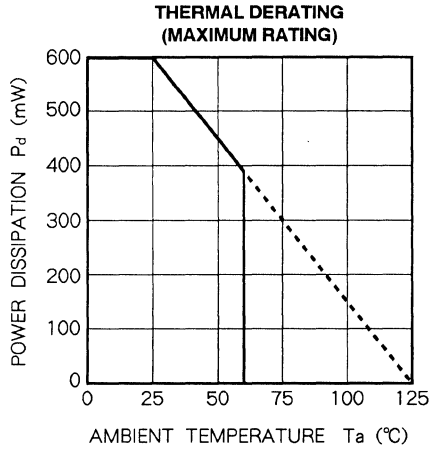
TEST METHODS

Parameter	State of switch														Method
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	
Circuit current (1)	2	0	1	2	1	2	1	1	1	1	2	1	1	1	Read off value for total circuit current for playback on ammeter A_1.
Circuit current (2)	2	0	1	2	1	2	1	1	1	2	1	1	1	2	Read off value for total circuit current for recording on ammeter A_1.
Equalizer + line voltage gain	1	1	1	1	2	2	1	1	1	1	2	1	1	2	$G_{a1} = 20\log(V_{O2}/V_{i1})$ [dB]
Equalizer + line voltage attenuation	1	1	1	1	2	2	1	1	1	1	2	1	1	2	Measure the difference in gain ($G_{a2} - G_{a1}$) [dB] when V_{CC} is 3V and 2V.
Equalizer + line total harmonic distortion rate	1	1	1	1	2	2	1	1	1	1	2	1	1	2	
Microphone + line voltage gain	1	2	1	1	2	2	1	1	1	2	2	1	1	2	$G_{b1} = 20\log(V_{O2}/V_{i2})$ [dB]
Microphone + line voltage attenuation	1	2	1	1	2	2	1	1	1	2	2	1	1	2	Measure the difference in gain ($G_{b2} - G_{b1}$) [dB] when V_{CC} is 3V and 2V.
ALC distortion	1	2	1	1	2	2	1	1	1	2	2	1	1	2	Measure the output distortion when $V_{i2} = -50$dBv
ALC range	1	2	1	1	2	2	1	1	1	2	2	1	1	2	ALC = 20log(V_3/V_1), where the input and output voltages at the rise of ALC are V_1 and V_2 respectively, and the input for $V_{O2} = V_2 + 3$[dB] is V_3.
Microphone input impedance	1	2	1/2	2	1	2	1	1	1	2	2	1	1	2	$Z_{iM} = 20V_2/(V_1 - V_2)$[kΩ], where V_{O1} for S_3 = 1 and 2 are V_1 and V_2 respectively.
Line input impedance	1	3	1	2	1	1/2	1	1	1	1	2	1	1	2	$Z_{iL} = 10V_2/(V_1 - V_2)$[kΩ], where V_{O2} for S_6 = 1 and 2 are is V_1 and V_2 respectively.
Maximum line output voltage	1	3	1	2	1	1	1	1	1	1	2	1	1	2	Measure the value of V_{O2} when distortion is 3%.
Power voltage gain	1	4	1	2	1	2	1	1	1	1	2	1	1	1	$G_{c1} = 20\log(V_{O3}/V_{i4})$ [dB]
Power voltage attenuation	1	4	1	2	1	2	1	1	1	1	2	1	1	1	Find the difference in gain ($G_{c2} - G_{c1}$) [dB] when V_{CC} is 3V and 2V
Power total harmonic distortion	1	4	1	2	1	2	1	1	1	1	2	1	1	1	
Maximum power output	1	4	1	2	1	2	1	1	1	1	2	1	1	1	$P_{OM1} = \frac{(V_{O3})^2}{8}$ when distortion is 10%
Power input impedance	1	4	1	2	1	2	1	1	1/2	1	2	1	1	1	$Z_{iP} = 20V_2/(V_1 - V_2)$[kΩ], where V_{O3} for S_9 = 1 and 2 are V_1 and V_2 prespectively.
Output offset voltage	1	4	1	2	1	2	1	1	1	1	2	1	1	1	Measure DC voltage difference between terminal ⑨ and terminal ⑦.(terminal ⑦ is the standard)
Earphone voltage gain	1	4	1	2	1	2	1	1	1	2	2	1	1	2	$G_{d1} = 20\log(V_{O4}/V_{i4})$ [dB]
Earphone voltage attenuation	1	4	1	2	1	2	1	1	1	2	2	1	1	2	Measure the difference in gain ($G_{d2} - G_{d1}$) [dB] when V_{CC} is 3V and 2V
Earphone total harmonic distortion	1	4	1	2	1	2	1	1	1	2	2	1	1	2	
Maximum earphone output	1	4	1	2	1	2	1	1	1	2	2	1	1	2	$P_{OM2} = \frac{(V_{O4})^2}{8}$ when distortion is 10%
Equalizer + line + power output noise characteristics	1	0	1	1	2	2	1	2	1	1	2	1	2	1	BW = 20Hz~20kHz
Microphone + line output noise voltage	1	0	1	1	2	2	2	1	1	2	2	1	1	2	BW = 20Hz~20kHz
pin ⑤ current	1	0	1	2	1	2	1	1	1	2	2	2	1	2	Read off value on ammeter A_2
Battery checker voltage	1	0	1	2	1	2	1	1	1	2	2	2	1	2	Measure the value of V_{CC} when the value of A_2 becomes 10μA or below, by gradually lowering V_{CC} from 3V.

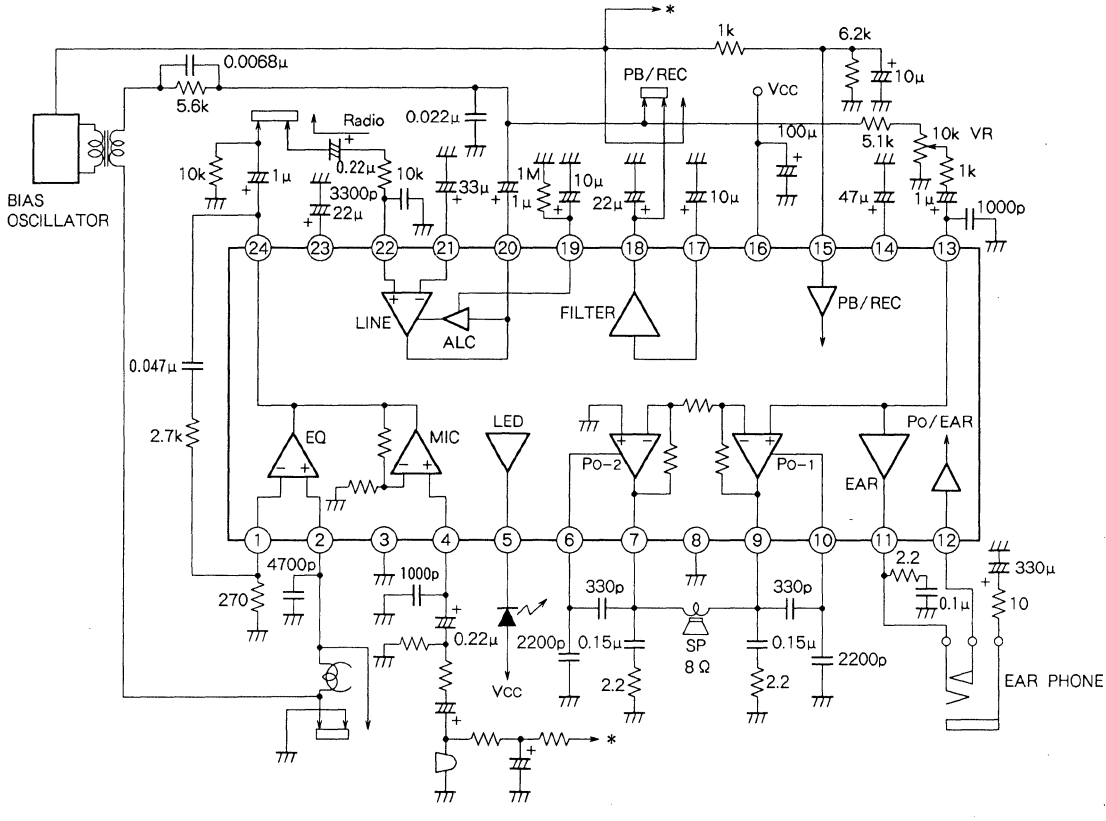
M51168AP

3V SINGLE CHIP, RECORD/PLAYBACK AMPLIFIER ·POWER AMPLIFIER

TYPICAL CHARACTERISTICS



APPLICATION EXAMPLE



M51524L,P,FP

AUTO REVERSE PREAMPLIFIER WITH MUSIC SENSOR

DESCRIPTION

The M51524 is a preamplifier IC developed for car audio systems.

The IC, in additions to 2 channels of high-gain, low-noise preamplifiers, has a lead-in detection function suiting to auto reverse function and is capable of processing analog signals transmitted from the cassteed deck.

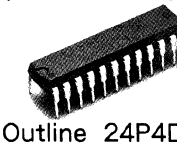
Its applications cover home-use audio systems and portable radio CD/cassette players, as well as car audio systems.

FEATURES

- Built-in electronic switch for forward/reverse selection offers capability of switching 2 channels with a single switch.
- Built-in switch for forward/reverse switching makes it possible to switch 2 channels with a single switch.
- Use of reference voltage of bias circuit eliminates the need for input coupling capacitor.
- 2 channels of high-gain, low-noise preamplifiers built-in.
- Internal direct connections between each preamplifier output and high-gain mixing amplifier, without using coupling capacitor.
- Built-in filter circuits for prevention of malfunctioning caused by tape pop up noise at music blank.
- Built-in reset circuit to reset music selection at power up.
- Capable of setting timing for music blank by means of external CR combination.

Outline 20P5A(L)

1.27mm pitch 325mil ZIP
(2.8mm × 25.2mm × 6.3mm)



Outline 24P4D(P)

2.54mm pitch 300mil DIP
(6.3mm × 29.2mm × 3.3mm)

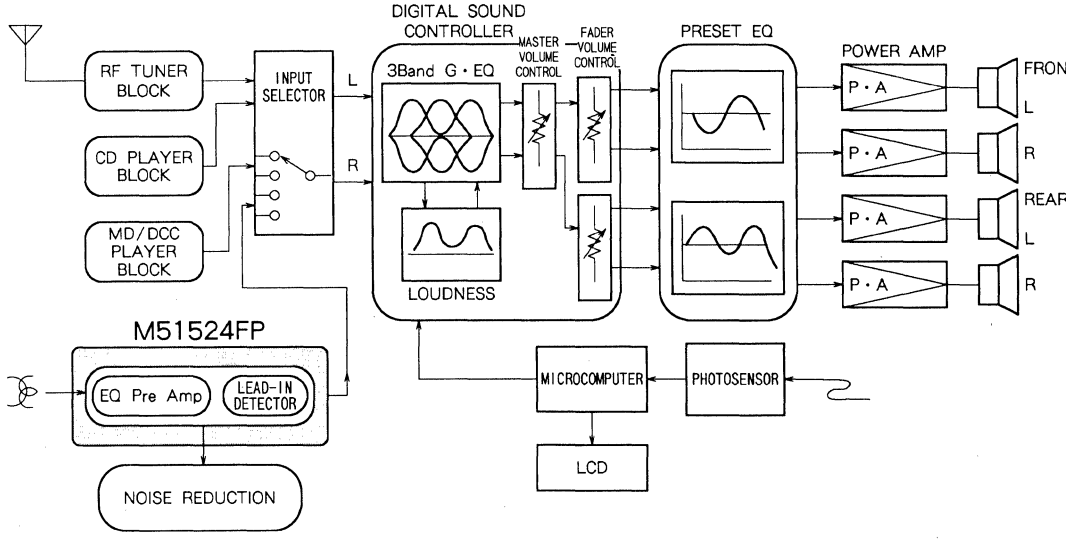
Outline 24P2N-B(FP)

1.27mm pitch 300mil SOP
(5.3mm × 15.02mm × 1.8mm)

RECOMMENDED OPERATING CONDITIONS

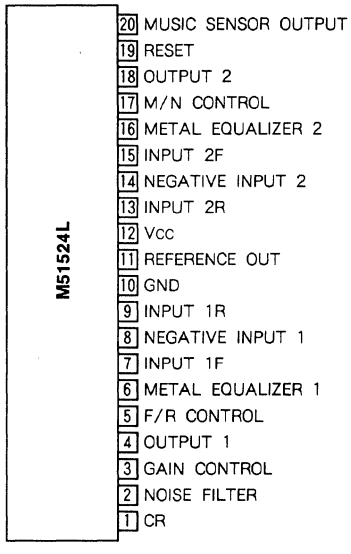
Supply voltage range ..... V_{CC} = 6~15V
Rated supply voltage ..... V_{CC} = 8V

SYSTEM CONFIGURATION

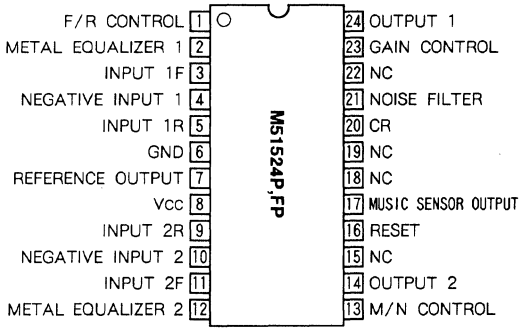


MITSUBISHI ELECTRIC

PIN CONFIGURATION



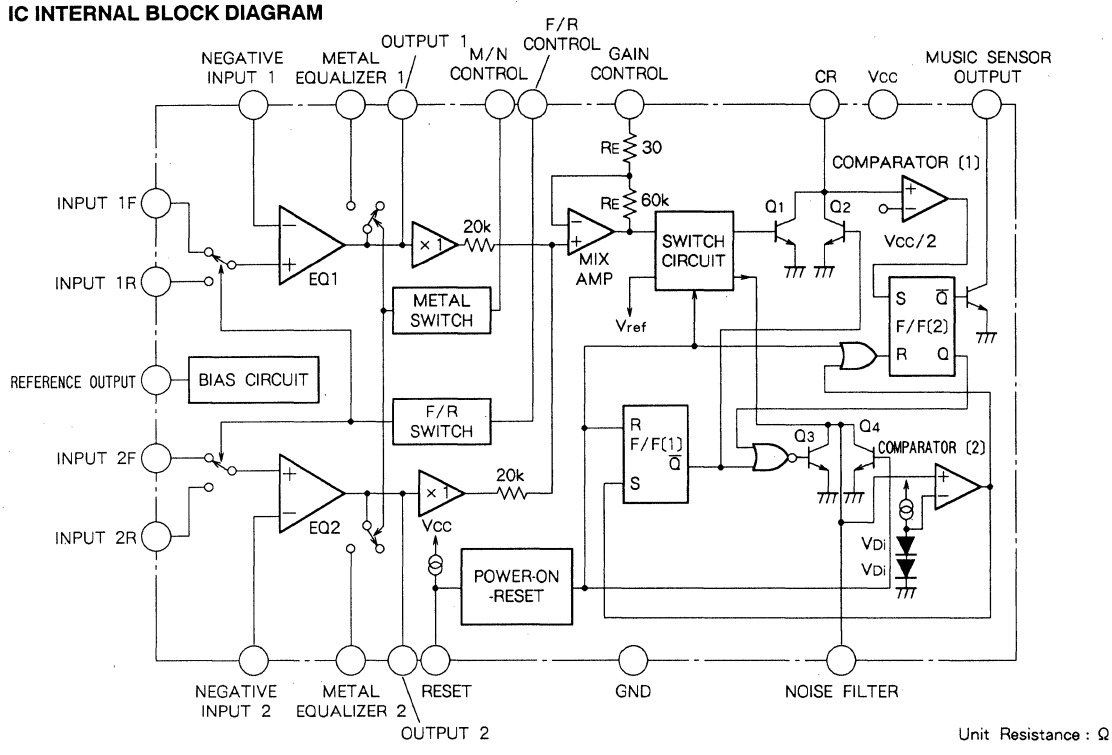
Outline 20P5A(L)



Outline 24P4D(P)
24P2N-B(FP)

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		16	V
I_{CC}	Circuit current		40	mA
P_d	Power dissipation	(M51524L)	800	mW
		(M51524P)	1000	
		(M51524FP)	500	
K_θ	Thermal derating	(M51524L)	8	mW/℃
		(M51524P)	10	
		(M51524FP)	5	
T_{opr}	Operating temperature		− 20∼ + 75	℃
T_{stg}	Storage temperature		− 40∼ + 125	℃

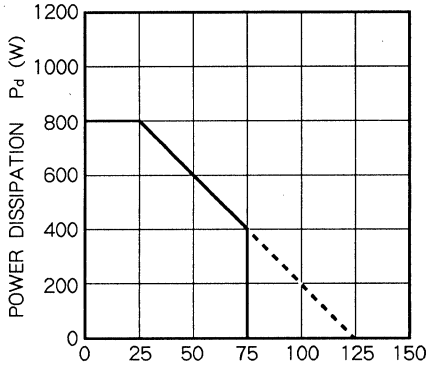
ELECTRICAL CHARACTERISTICS (f = 1kHz, Rg = 620Ω, V_{CC} = 8V, Normal equalizer, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	Quiescent circuit current	−	9	14	mA
G_{VO}	Open loop gain	C_E = 220μF	68	80	−	dB
G_{VC}	Closed loop gain		38.5	40.5	42.5	dB
THD	Total harmonic distortion	V_O = 0.5Vrms	−	0.06	0.2	%
V_{omax}	Maximum output voltage	THD = 1 %	1.5	2.0	−	Vrms
N_O	Output noise voltage	BW = 20Hz∼20kHz	−	85	160	μVrms
Sep	Separation	V_O = 0dBm, BW = 20Hz∼20kHz	45	63	−	dB
CT	Cross talk	V_O = 0dBm, BW = 20Hz∼20kHz	60	78	−	dB
$I_{in1(20)}$	CR circuit input current		−	− 0.1	− 0.6	μA
V_{OL}	Music senser output voltage Low		−	0.15	0.4	V
$V_{th1(20)}$	Comparator (1) threshold voltage		3.5	4.0	4.5	V
$I_{19(16)}$	Reset charging current		− 3	− 9	− 30	μA
$V_{19(16)}$	Reset completion voltage		1.0	1.4	1.7	V
$V_{th19(16)}$	Reset threshold voltage		0.8	1.2	1.7	V
$I_{2(21)}$	Noise filter charging current		− 30	− 60	− 110	μA
$V_{th2(21)}$	Comparator (2) threshold voltage		1.1	1.5	1.7	V
$R_{5(1)}$	Input impedance pin⑤ (1)	$V_{5(1)}$ = 1V	70	100	150	kΩ
$R_{17(13)}$	Input impedance pin⑰ (13)	$V_{17(13)}$ = 1V	70	100	150	kΩ

Note1. ( ) M51524P,FP

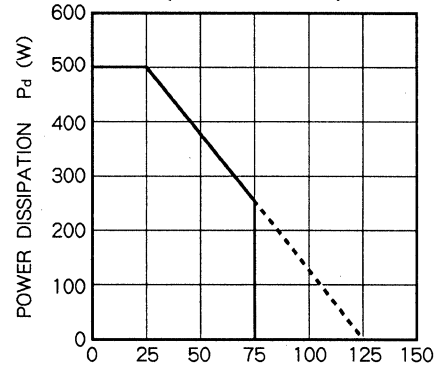
TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)



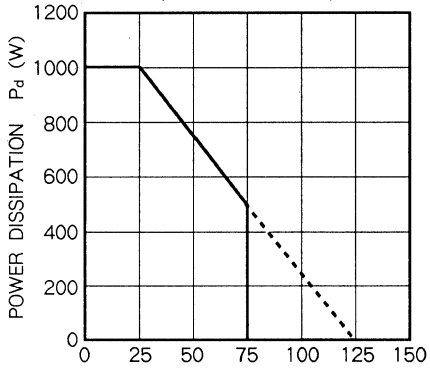
M51524L

THERMAL DERATING (MAXIMUM RATING)



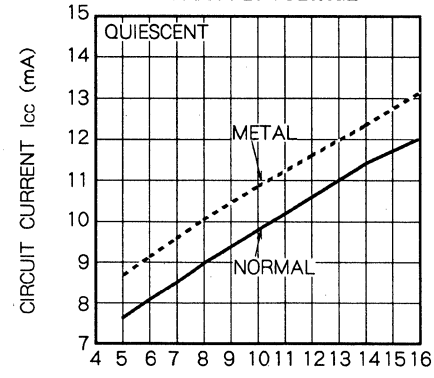
M51524FP

THERMAL DERATING (MAXIMUM RATING)

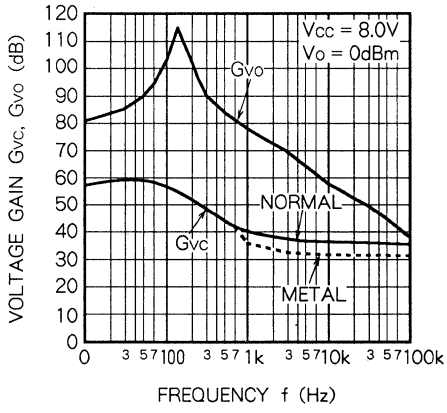


M51524P

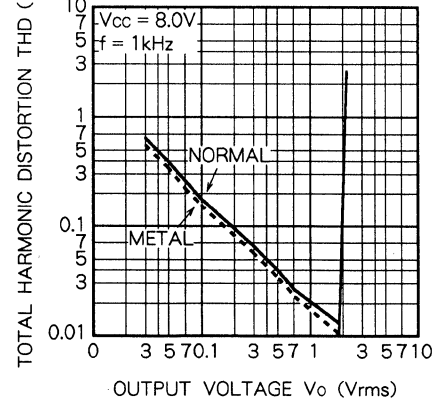
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



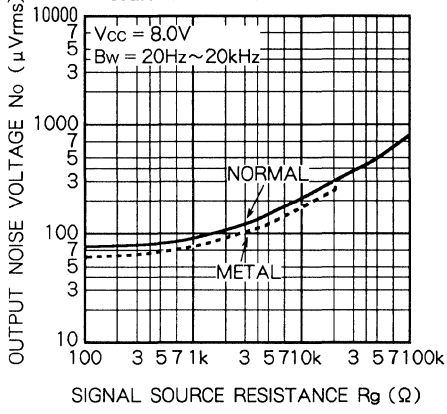
VOLTAGE GAIN VS. FREQUENCY



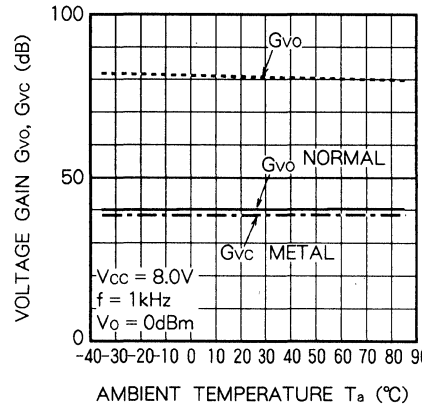
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



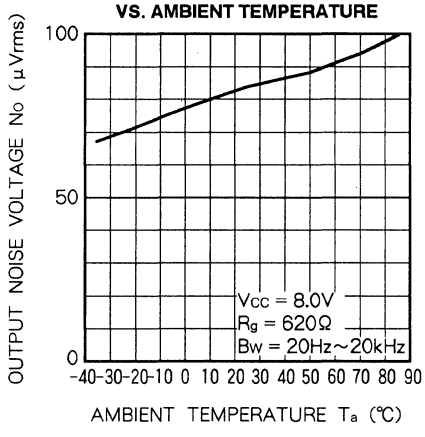
OUTPUT NOISE VOLTAGE VS. SIGNAL SOURCE RESISTANCE



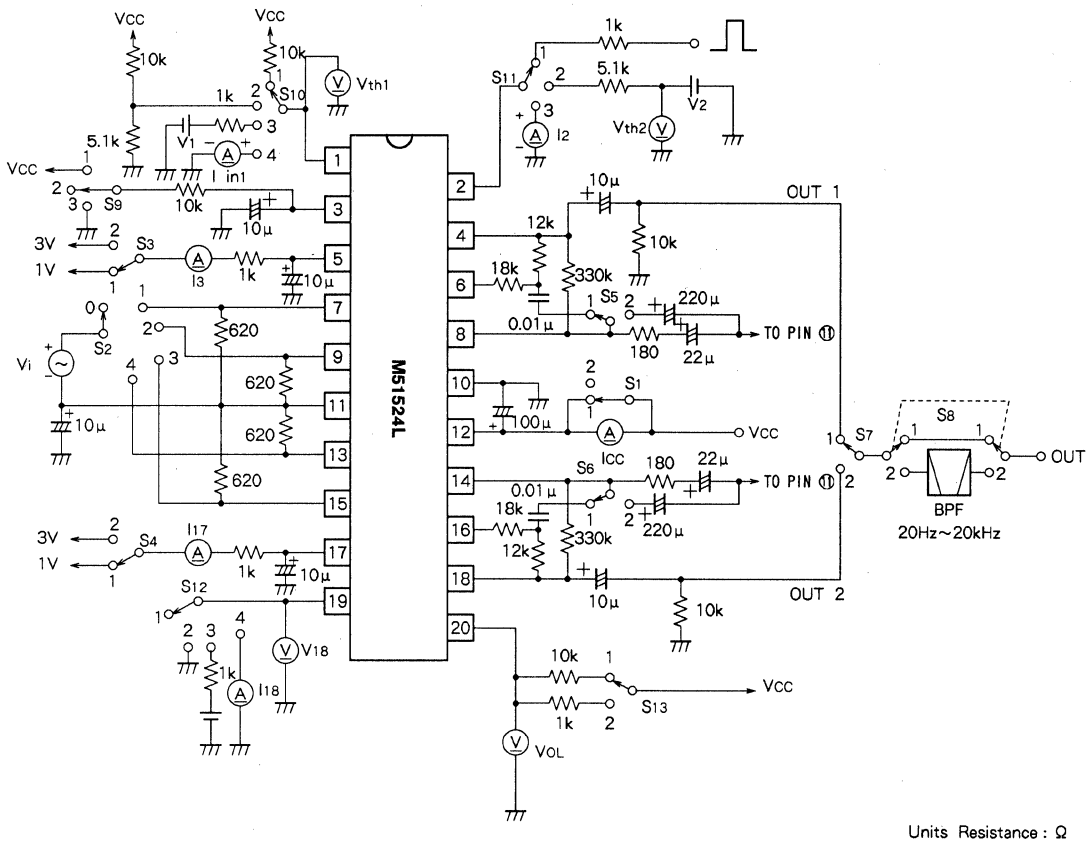
OUTPUT NOISE VOLTAGE VS. AMBIENT TEMPERATURE



OUTPUT NOISE VOLTAGE VS. AMBIENT TEMPERATURE

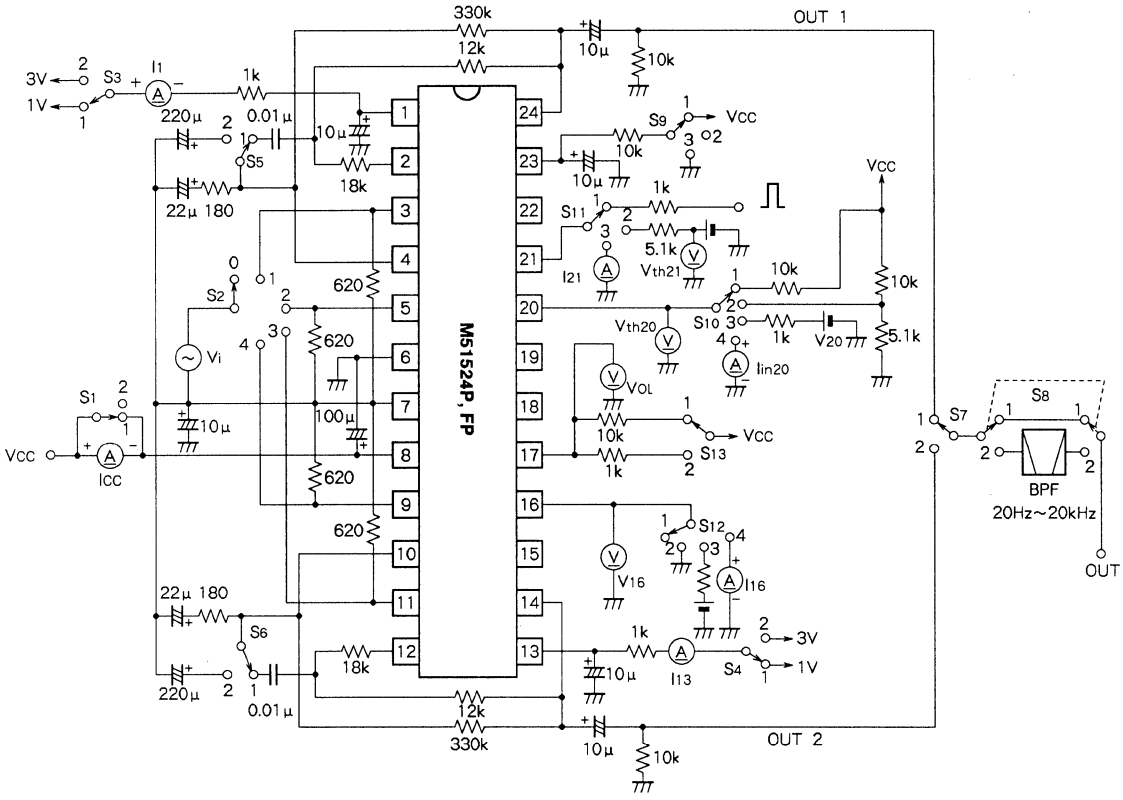


TEST CIRCUIT (M51524L)



Units Resistance : Ω
Capacitance : F

TEST CIRCUIT (M51524P, FP)



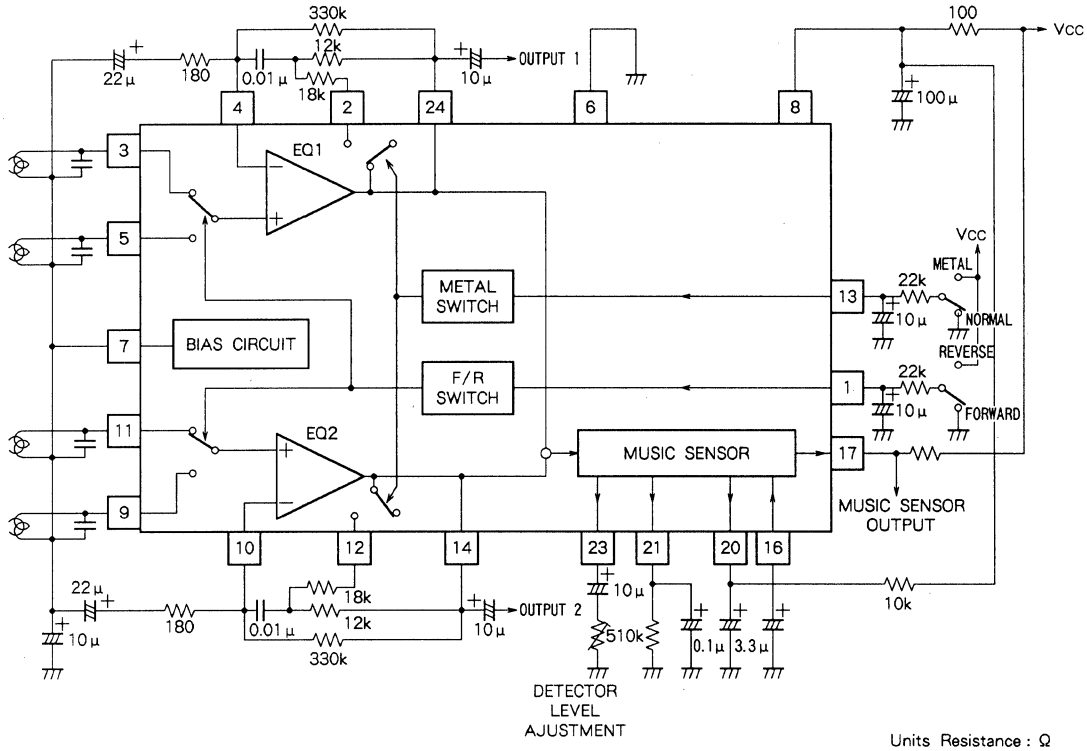
Units Resistance : Ω
Capacitance : F

TEST CONDITIONS

Parameter	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	Methods
I_{CC}	2	0	1	1	1	1	1	1	2	1	1	1	1	Read value on ammeter
G_{VO}	1	1 / 3	1 / 2	1	2 / 1	1 / 2	1 / 2	1	2	1	1	2	1	G_{VO} = 20 log (V_O/V_i)
G_{VC}	1	1 / 3	1	1	1	1	1 / 2	1	2	1	1	2	1	G_{VC} = 20 log (V_O/V_i)
THD	1	1 / 3	1	1	1	1	1 / 2	1	2	1	1	2	1	Read value on distortion meter at V_O = 0.5Vrms
V_{omax}	1	1 / 3	1	1	1	1	1 / 2	1	2	1	1	2	1	Measure output valtage at THD = 1 %
N_O	1	0	1 / 2	1	1	1	1 / 2	2	2	1	1	2	1	BW = 20Hz~20kHz
Sep	1	1 / 3	1	1	1	1	1,2 / 1,2	2	2	1	1	2	1	Measure output voltage when another output voltage is 0dBm. BW = 20Hz~20kHz, Sep = V_O(dB)
CT	1	1 / 3	2 / 4	1,2 / 1,2	1	1	1 / 2	2	2	1	1	2	1	Measure crosstalk between Forward and Reverse V_i = 0dBm, BW = 20Hz~20kHz
$I_{in1(20)}$	1	0	1	1	1	1	1	1	2	4	1	1	2	Measure current of pin①(20) after preset pulse enters to pin②(21)
V_{OL}	1	0	1	1	1	1	1	1	2	4	1	1	2	Measure voltage of pin⑳(17) after preset pulse enters to pin②(21)
$V_{th1(20)}$	1	0	1	1	1	1	1	1	2	3	1	1	1	Measure voltage of pin①(20) when V_1 increases from 1V and output of pin⑳(17) changes to High from Low after preset pulse enters to pin②(21)
$I_{19(16)}$	1	0	1	1	1	1	1	1	2	1	1	4	1	Measure current with pin⑲(16)
$V_{19(16)}$	1	0	1	1	1	1	1	1	2	1	1	1	1	Measure voltage with pin⑲(16)
$V_{th19(16)}$	1	0	1	1	1	1	1	1	2	1	1	3	1	Measure voltage of pin⑲(16) when V_{19} decreases from 2V and output of pin⑳(17) changes to Low from High, after preset pulse enters to pin
$I_{2(21)}$	1	0	1	1	1	1	1	1	3	2	3	*	1	Measere current of pin②(21) after S_{12} changes to 1→2→1
$V_{th2(21)}$	1	0	1	1	1	1	1	1	2	2	2	*	1	Measure supply voltage of pin②(21) when V_2 increases from 0.5V and voltage of pin①(20) changes to High (≃2.7V) from Low, after S_{12} changes to 1→2→1
$R_{5(1)}$	1	0	1	1	1	1	1	1	2	1	1	1	1	Measure current $I_{⑤\ (1)}$ at pin⑤ (1) $P_{⑤\ (1)} = 1/I_{⑤\ (1)}$(kΩ)
$R_{17(13)}$	1	0	1	1	1	1	1	1	2	1	1	1	1	Measure current $I_{⑰(13)}$ at pin⑰(13) $P_{⑰\ (13)} = 1/I_{⑰\ (13)}$(kΩ)

Note 2. ( )M51524P, FP

APPLICATION EXAMPLE (M51524P, FP)



Units Resistance : Ω
Capacitance : F

M51525P,FP,GP

AUTO REVERSE PREAMPLIFIER WITH MUSIC SENSOR

DESCRIPTION

The M51525 is a preamplifier IC developed for car audio systems.

The IC, in additions to 2 channels of high-gain, low-noise preamplifiers, has a lead-in detection function suiting to auto reverse function and is capable of processing analog signals transmitted from the cassteed deck.

Its applications cover home-use audio systems and portable radio CD/cassette players, as well as car audio systems.

FEATURES

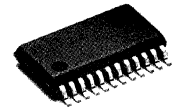
- Frequency characteristics adjust pin for mixing amplifier.
- Built-in electronic switch for forward/reverse selection offers capability of switching 2 channels with a single switch.
- Built-in electronic switch for equalizer selection makes it possible to switch 2 channels with a single switch.
- Use of reference voltage of bias circuit eliminates the need for input coupling capacitor.
- 2 channels of high-gain, low-noise preamplifiers built-in.
- Internal direct connection between each preamplifier output and high-gain mixing amplifier, without using coupling capacitor.
- Built-in filter circuits for prevention of malfunctioning caused by tape pop up noise at music blank.
- Built-in reset circuit to reset music selection at power up.
- Capable of setting timing for music blank by means of external CR combination.

Outline 24P4D(P)

2.54mm pitch 300mil DIP
(6.3mm × 29.2mm × 3.3mm)

Outline 24P2N-B(FP)

1.27mm pitch 300mil SOP
(5.3mm × 15.02mm × 1.8mm)



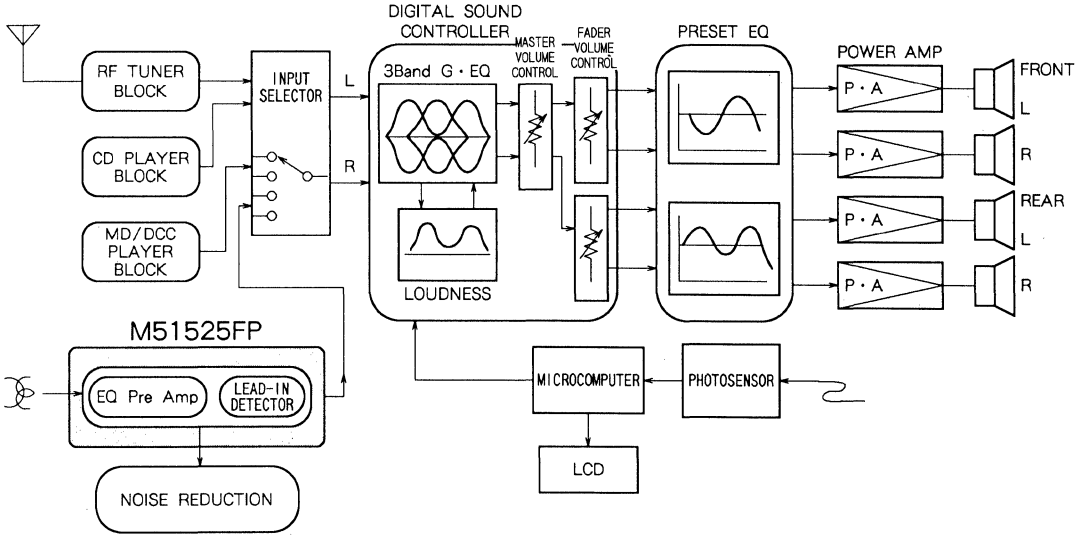
Outline 24P2Q-A(GP)

0.8mm pitch 300mil SSOP
(5.3mm × 10.1mm × 1.8mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 6~15V
Rated supply voltage ..... V_{CC} = 8V

SYSTEM CONFIGURATION

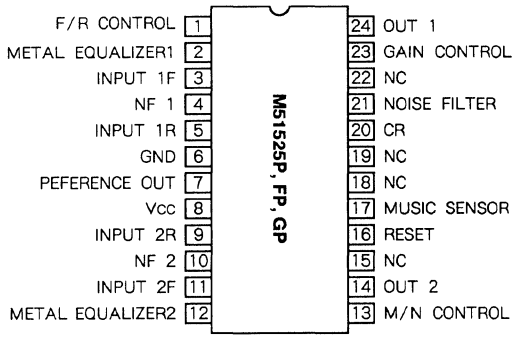


MITSUBISHI ELECTRIC

M51525P,FP,GP

AUTO REVERSE PREAMPLIFIER WITH MUSIC SENSOR

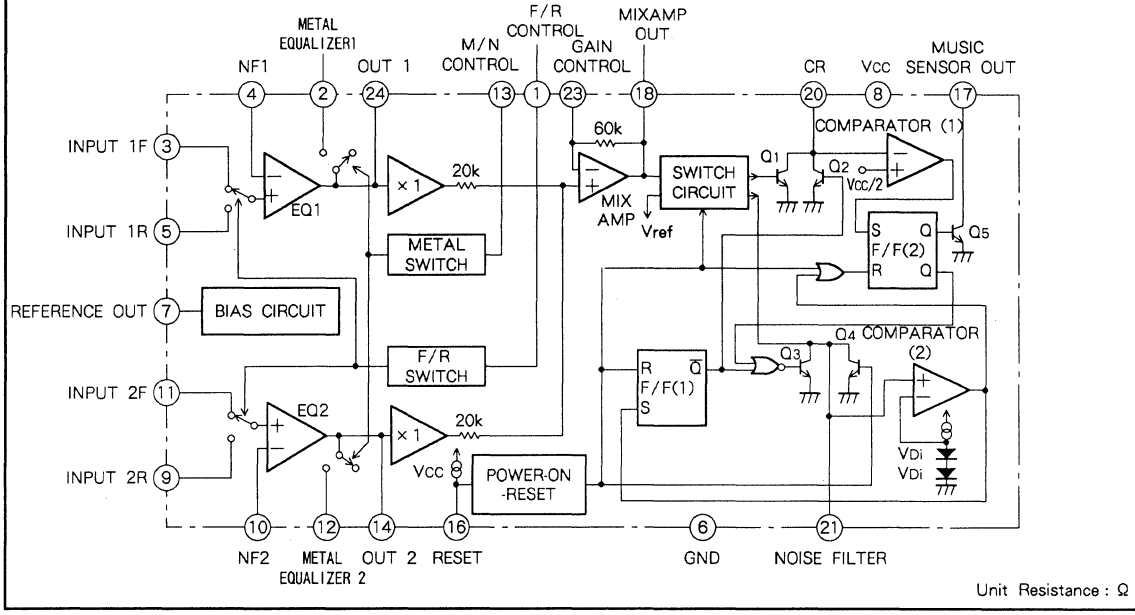
PIN CONFIGURATION



Outline 24P4D(P)
24P2N-B(FP)
24P2Q-A(GP)

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

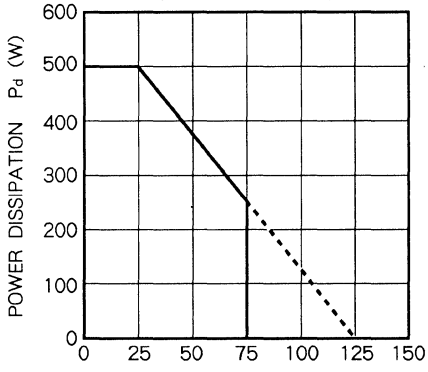
Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		16	V
I_{CC}	Circuit current		40	mA
P_d	Power dissipation	(M51525P)	1000	mW
		(M51525FP)	500	
		(M51525GP)	540	
K_θ	Thermal derating	(M51525P)	10	mW/℃
		(M51525FP)	5	
		(M51525GP)	5.4	
T_{opr}	Operating temperature		− 20∼ + 75	℃
T_{stg}	Storage temperature		− 40∼ + 125	℃

ELECTRICAL CHARACTERISTICS (f = 1kHz, R_g = 620Ω, V_{CC} = 8V, Normal equalizer, Ta = 25℃, unless otherwise noted)

Symbol	Paramter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	Quiescent circuit current	−	9	14	mA
G_{VO}	Open loop gain	C_E = 220μF	68	80	−	dB
G_{VC}	Close loop gain		38.5	40.5	42.5	dB
THD	Total harmonic distortion	V_O = 0.5Vrms	−	0.06	0.2	%
V_{omax}	Maximum output voltage	THD = 1 %	1.5	2.0	−	Vrms
N_O	Output noise voltage	BW = 20Hz∼20kHz	−	85	160	μVrms
Sep	Separation	V_O = 0dBm, BW = 20Hz∼20kHz	45	63	−	dB
CT	Crosstalk	V_O = 0dBm, BW = 20Hz∼20kHz	60	78	−	dB
I_{in20}	CR circuit input current		−	− 0.1	− 0.6	μA
V_{OL}	Music senser output voltage L		−	0.15	0.4	V
V_{th20}	Comparator (1) threshold voltage		3.5	4.0	4.5	V
I_{16}	Reset charging current		− 3	− 9	− 30	μA
V_{16}	Reset completion voltage		1.0	1.4	1.7	V
V_{th16}	Reset threshold voltage		0.8	1.2	1.7	V
I_{21}	Noise filter charging current		− 30	− 60	− 110	μA
V_{th21}	Comparator (2) threshold voltage		1.1	1.5	1.7	V
R_I	Input impedance (pin①)	V_I = 1V	70	100	150	kΩ
R_{13}	Input impedance (pin⑬)	V_{13} = 1V	70	100	150	kΩ

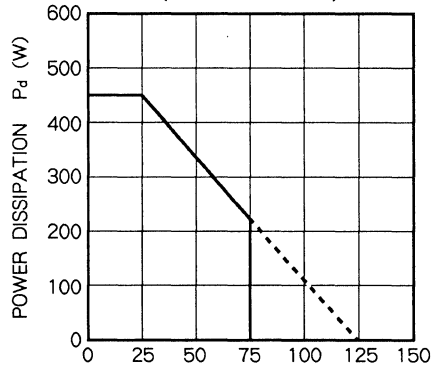
TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)



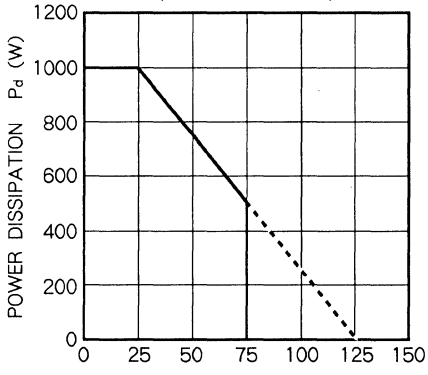
M51525FP

THERMAL DERATING (MAXIMUM RATING)



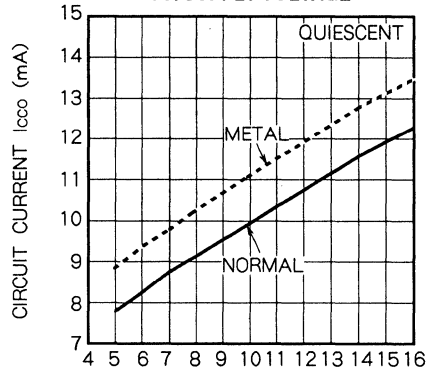
M51525GP

THERMAL DERATING (MAXIMUM RATING)

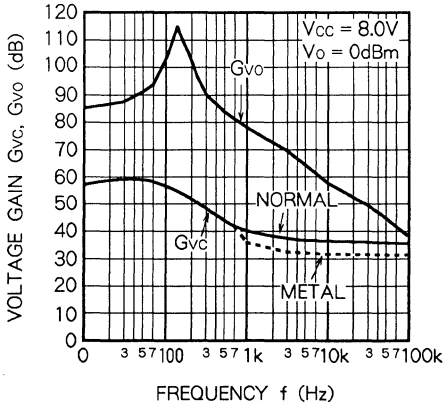


M51525P

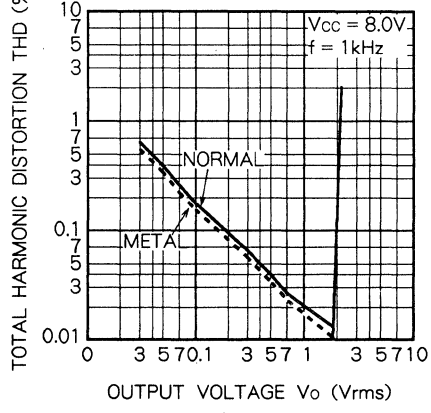
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



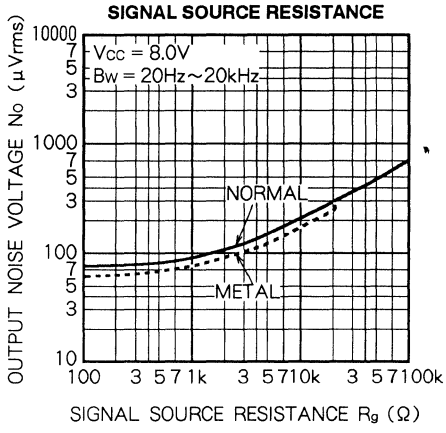
VOLTAGE GAIN VS. FREQUENCY



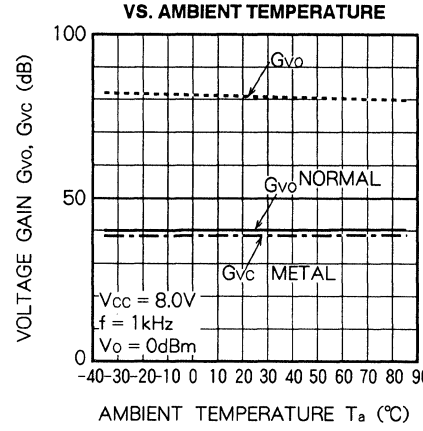
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



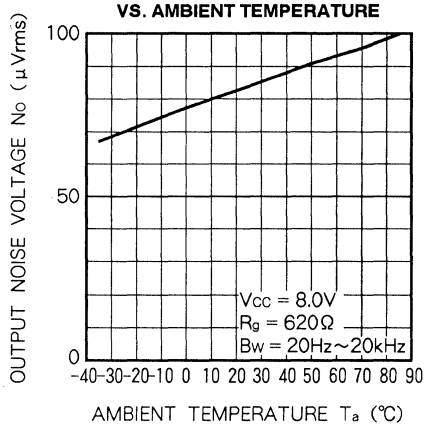
OUTPUT NOISE VOLTAGE VS. SIGNAL SOURCE RESISTANCE



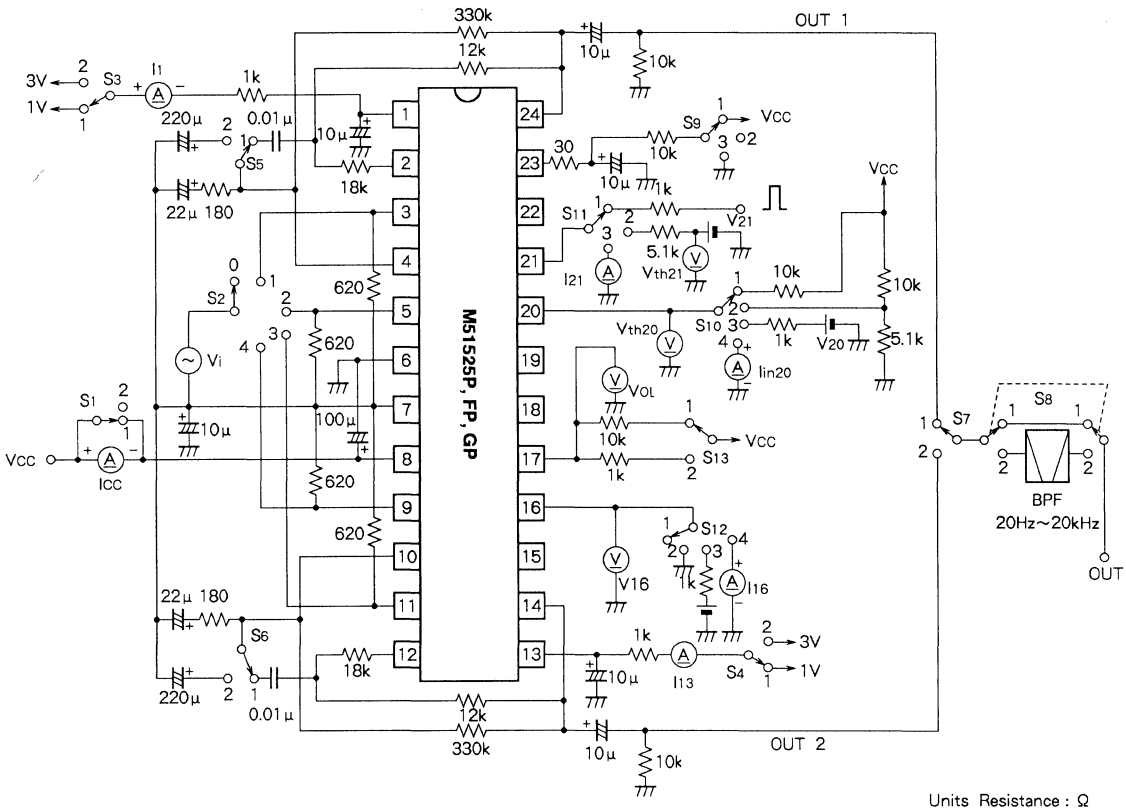
VOLTAGE GAIN VS. AMBIENT TEMPERATURE



OUTPUT NOISE VOLTAGE VS. AMBIENT TEMPERATURE



TEST CIRCUIT



Units Resistance : Ω
Capacitance : F

TEST CONDITIONS

Parameter	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	Methods
I_{CC}	2	0	1	1	1	1	1	1	2	1	1	1	1	Read value on ammeter
G_{VO}	1	1 / 3 / 2 / 4	1 / 2	1	2 / 1	1 / 2	1 / 2	1	2	1	1	2	1	$G_{VO} = 20\ \log(V_O/V_i)$
G_{VC}	1	1 / 3	1	1	1	1	1 / 2	1	2	1	1	2	1	$G_{VC} = 20\ \log(V_O/V_i)$
THD	1	1 / 3	1	1	1	1	1 / 2	1	2	1	1	2	1	Read value on distortion meter at V_O = 0.5Vrms
V_{omax}	1	1 / 3	1	1	1	1	1 / 2	1	2	1	1	2	1	Measure output voltage at THD = 1 %
N_O	1	0	1 / 2	1	1	1	1 / 2	2	2	1	1	2	1	BW = 20Hz~20kHz
Sep	1	1 / 3	1	1	1	1	1,2 / 1,2	2	2	1	1	2	1	Measure output voltage when another output voltage is 0dBm. BW = 20Hz~20kHz, Sep = V_O(dB)
CT	1	1 / 3 / 2 / 4	1,2 / 1,2	1	1	1	1 / 2	2	2	1	1	2	1	Measure crosstalk between forward and reverse V_i = 0dBm, BW = 20Hz~20kHz
I_{in20}	1	0	1	1	1	1	1	1	2	4	1	1	2	Measure current of pin⑳ after preset pulse enters to pin㉑
V_{OL}	1	0	1	1	1	1	1	1	2	4	1	1	2	Measure voltage of pin⑰ after preset pulse enters to pin㉑
V_{th20}	1	0	1	1	1	1	1	1	2	3	1	1	1	Measure voltage of pin⑳ when V_1 increases from 1V and output of pin⑰ changes to High from Low after preset pulse enters to pin㉑
I_{16}	1	0	1	1	1	1	1	1	2	1	1	4	1	Measure current with pin⑯
V_{16}	1	0	1	1	1	1	1	1	2	1	1	1	1	Measure voltage with pin⑯
V_{th16}	1	0	1	1	1	1	1	1	2	1	1	3	1	Measure voltage of pin⑯ when V_{19} decreases from 2V and output of pin⑰ changes to Low from High, after preset pulse enters to pin
I_{21}	1	0	1	1	1	1	1	1	3	2	3	*	1	Measere current of pin㉑ after S_{12} changes to 1→2→1
V_{th21}	1	0	1	1	1	1	1	1	2	2	2	*	1	Measure supply voltage of pin㉑ when V_2 increases from 0.5V and voltage of pin⑳ changes to High (2.7V) from Low, after S_{12} changes to 1→2→1
R_1	1	0	1	1	1	1	1	1	2	1	1	1	1	Measure current I_1 at pin① $R_1 = 1/I_1$ (kΩ)
R_{13}	1	0	1	1	1	1	1	1	2	1	1	1	1	Measure current I_{13} at pin⑬ $R_{13} = 1/I_{13}$ (kΩ)

M5280L,P,FP
GROUND ISOLATOR AMPLIFIER

DESCRIPTION

The M5280 is a ground isolator amplifier for car audio systems. Since the audio equipment in a car uses the body as the ground, noise generated by other electric units flows into the power amplifier as noise current. In the component type audio system (where the grounding point of each unit differs) especially, this noise may be output from a loudspeaker.

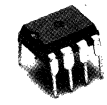
This IC reduces this in-coming noise by using the in-phase input rejection characteristic of the differential amplifier.

FEATURES

- High in-phase input rejection ratio ..... CMRR = 48dB (typ., f = 1kHz)
- Low noise ..... V_{NO} = 6μVrms(typ., BW : 20Hz~30kHz)
- Low distortion ratio ..... THD = 0.002% (typ., f = 1kHz, V_O = 1Vrms)
- Built-in 2 channels (Stereo type)
- Wide supply voltage range ..... V_{CC} = 4V~36V

Outline 8P5(L)

2.54mm pitch 340mil SIP
(2.8mm × 19.0mm × 6.4mm)



Outline 8P4(P)

2.54mm pitch 300mil DIP
(6.3mm × 8.9mm × 3.3mm)

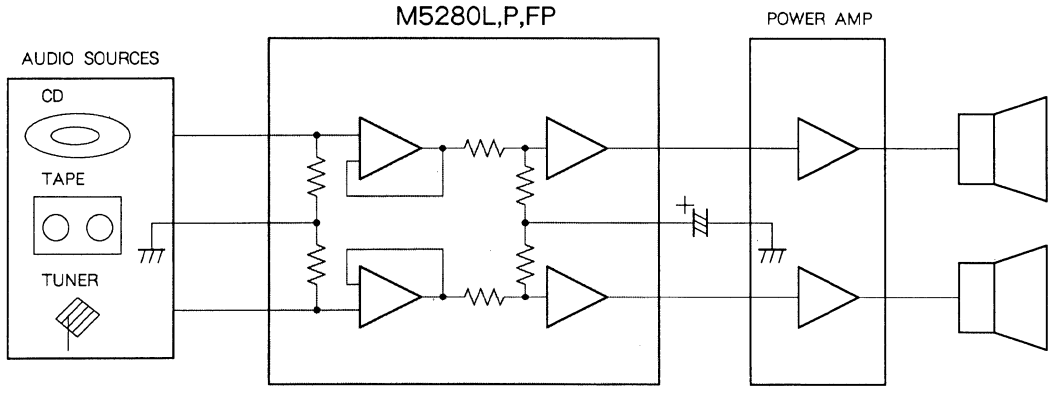
Outline 8P2S-A(FP)

1.27mm pitch 225mil SOP
(4.4mm × 5.0mm × 1.5mm)

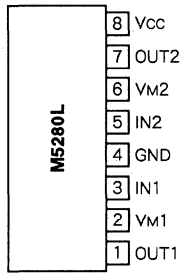
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{CC} = 4~36V
Rate supply voltage ..... V_{CC} = 12V

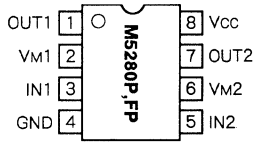
SYSTEM CONFIGURATION



PIN CONFIGURATION

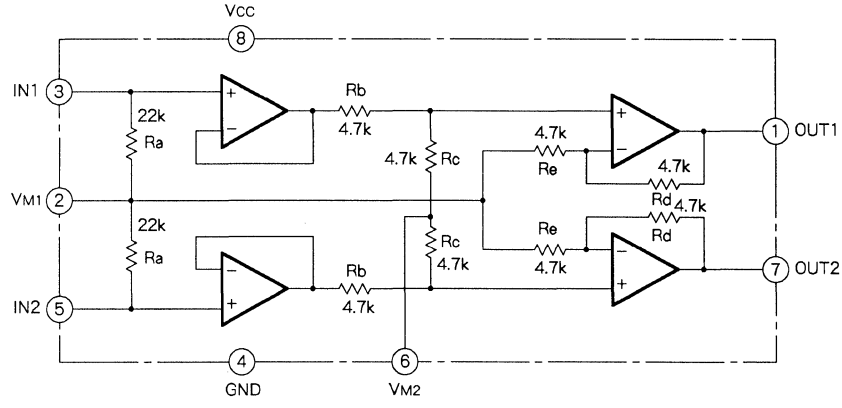


Outline 8P5(L)



Outline 8P4(P)
8P2S-A(FP)

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	36	V
I_{LP}	Load current	30	mA
P_d	Power dissipation	800(L)/625(P)/440(FP)	mW
T_{opr}	Operating temperature	− 20 ~ + 75	℃
T_{stg}	Storage temperature	− 55 ~ + 125	℃

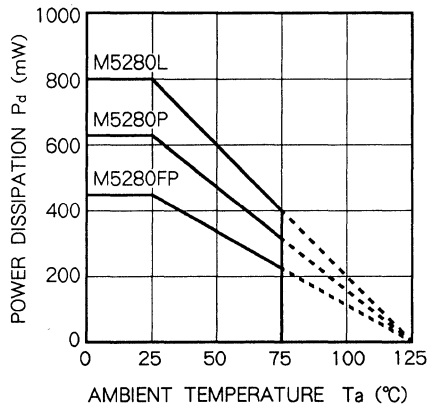
ELECTRICAL CHARACTERISTICS (V_{CC} = 12V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	V_I = 0	3.0	6.3	10.0	mA
V_{IO}	Offset voltage	V_{CC} = ± 6	−	1.0	10.0	mV
SVRR	Supply voltage rejection rate	$SVRR = \frac{\lvert V_{IO1} - V_{IO2} \rvert}{5}$	−	65	200	μ V/V
G_V	Voltage gain	f = 1kHz, V_I = 0dBm	− 1.5	− 0.05	+ 1.5	dB
V_{OM}	Maximum output voltage	f = 1kHz, THD = 0.1 %, V_{CC} = 8V	1.5	1.9	−	Vrms
THD	Total harmonic distortion	f = 1kHz, V_O = 1Vrms	−	0.002	0.03	%
CMRR	Common mode rejection ratio	f = 1kHz	37	48	−	dB
$V_{CM(MAX)}$	Common input voltage width	V_I value when V_{CC}=8V, CMRR=40dB and f=1kHz	1.0	1.9	−	Vrms
CS	Channel separation	f = 1kHz, V_I = − 10dBm	−	70	−	dB
V_{NO}	Output noise voltage	BW : 20Hz~30kHz	−	6	10	μ Vrms
SR	Slew rate		−	2.0	−	V/μ s

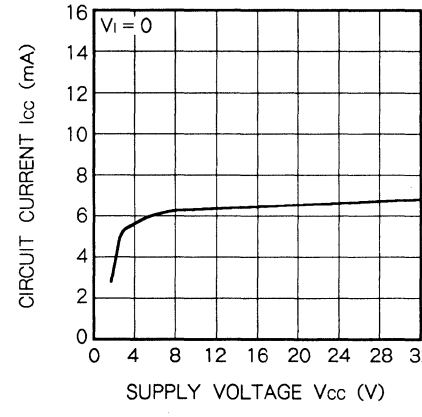
* V_{IO1} (V_{CC} = ± 11V)
  V_{IO2} (V_{CC} = ± 6V)

TYPICAL CHARACTERISTICS

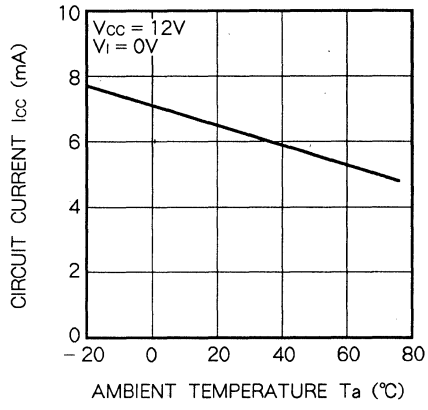
THERMAL DERATING
(MAXIMUM RATING)



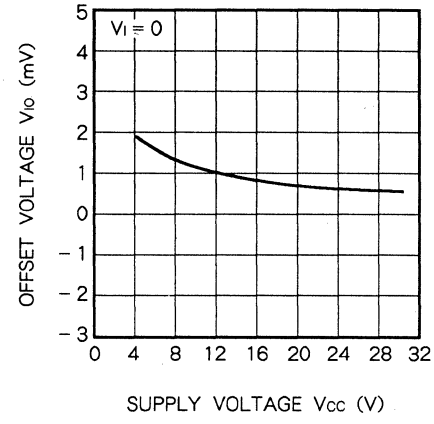
CIRCUIT CURRENT VS.
SUPPLY VOLTAGE



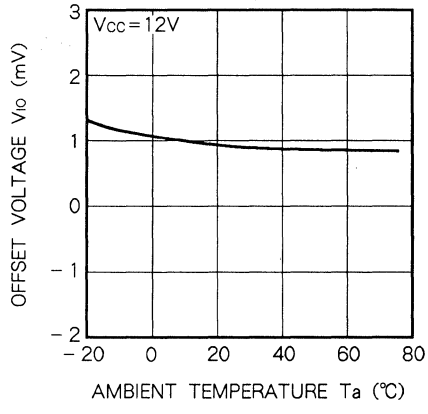
CIRCUIT CURRENT VS. AMBIENT TEMPERATURE



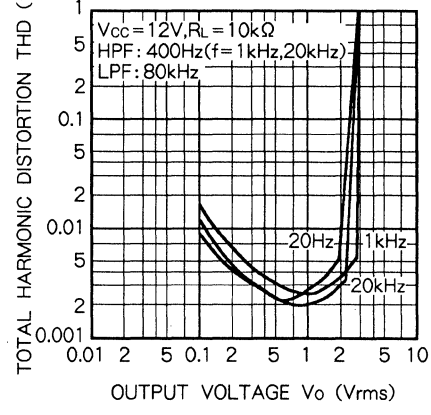
OFFSET VOLTAGE VS. SUPPLY VOLTAGE



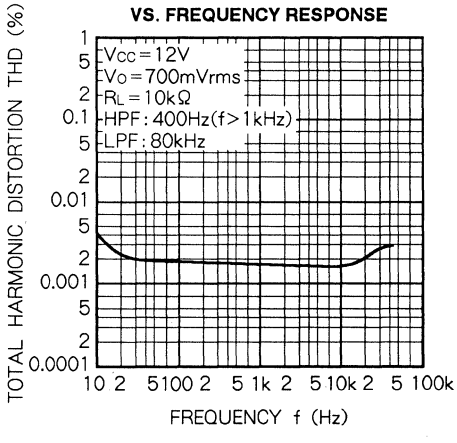
OFFSET VOLTAGE VS. AMBIENT TEMPERATURE



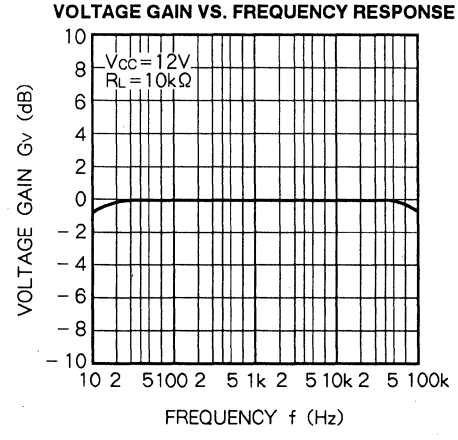
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



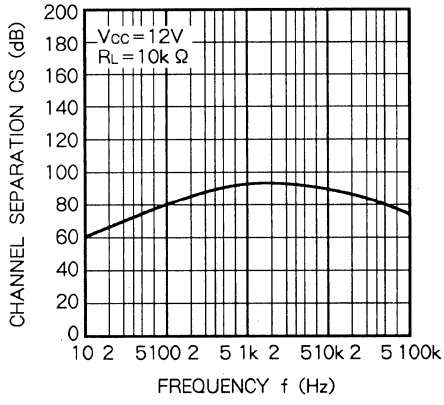
TOTAL HARMONIC DISTORTION VS. FREQUENCY RESPONSE



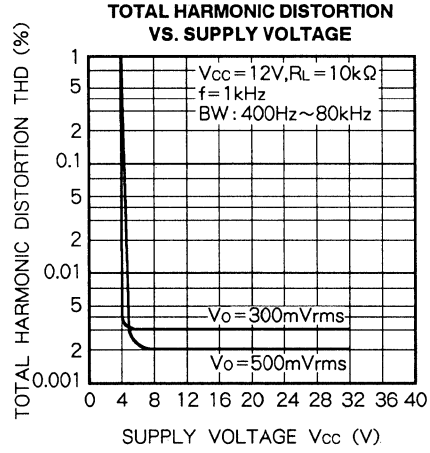
VOLTAGE GAIN VS. FREQUENCY RESPONSE



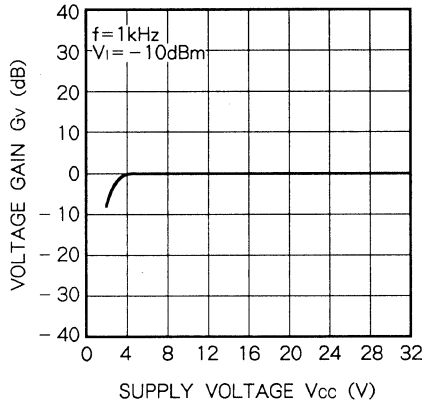
CHANNEL SEPARATION VS. FREQUENCY RESPONSE



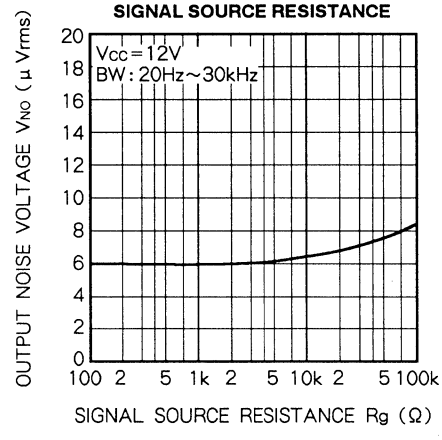
TOTAL HARMONIC DISTORTION VS. SUPPLY VOLTAGE



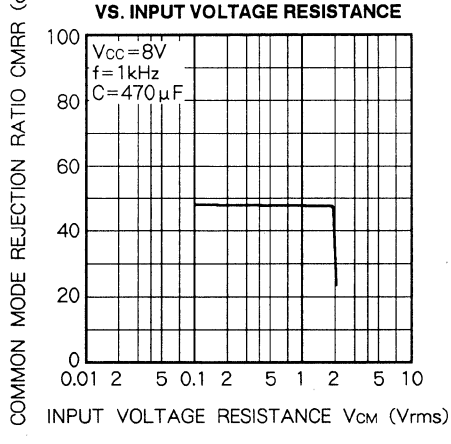
VOLTAGE GAIN VS. SUPPLY VOLTAGE



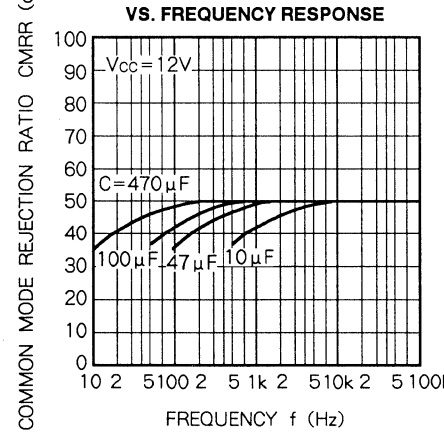
OUTPUT NOISE VOLTAGE VS. SIGNAL SOURCE RESISTANCE



COMMON MODE REJECTION RATIO VS. INPUT VOLTAGE RESISTANCE

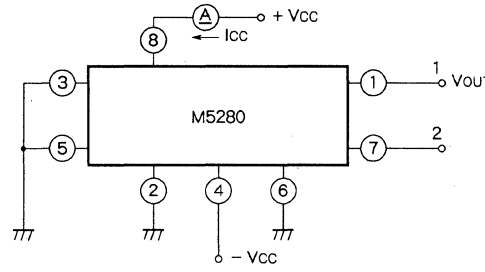


COMMON MODE REJECTION RATIO VS. FREQUENCY RESPONSE

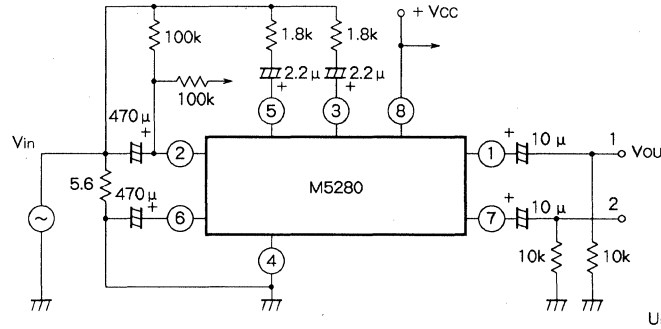


TEST CIRCUIT

1. **Circuit current I_{CC}**
   Offset voltage V_{IO}



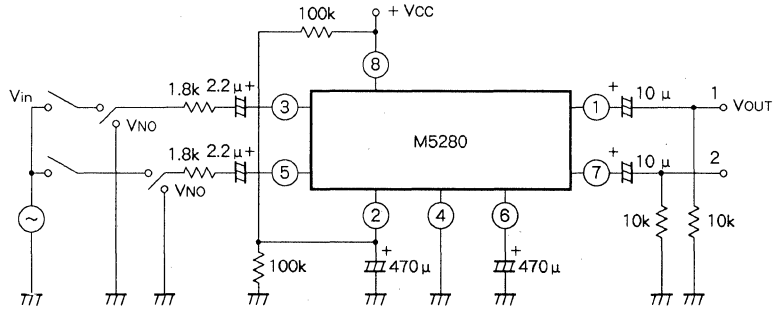
2. **Common mode rejection ratio CMRR**
   Common input voltage width $V_{CM(MAX)}$



Units Resistance : Ω
Capacitance : F

3. **Voltage gain G_V**
   Maximum output voltage V_{OM}
   Total harmonic distortion THD

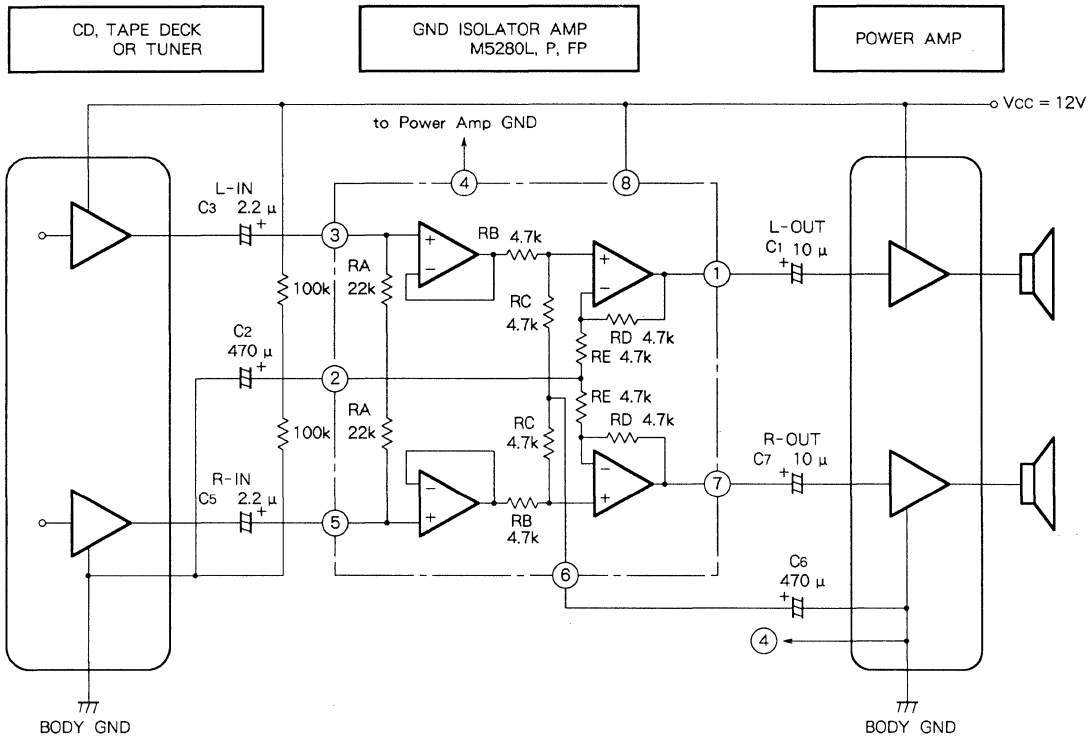
   Channel separation CS
   Output noise voltage V_{NO}



☆ Insert BPF 20Hz to 30kHz wile measuring the V_{NO}.

Units Resistance : Ω
Capacitance : F

APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F

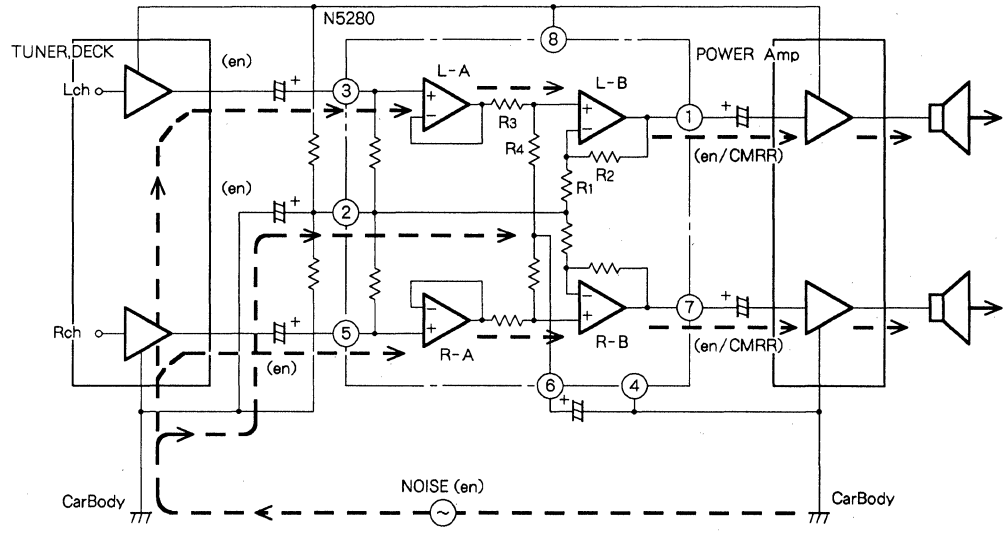
PIN DESCRIPTION

Pin No.	Symbol	Name	Function
①	OUT1	Output 1	This output terminal is biased to Vcc/2 (DC), therefore, you must use a coupling capacitor of cutting the DC.
②	VM1	Mid-point 1	Connected to the input side GND(i.e. Tuner or Deck)through capacitor C2. Bias this terminal (Vcc/2) using an external resistor to obtain the output of Vcc/2.
③	IN1	Input 1	This input terminal is biased to Vcc/2 (DC), therefore, you must use a coupling capacitor for cutting the DC.
④	GND	Ground	To be connected to the output side GND (i.e. power amplifier).
⑤	IN2	Input 2	This input terminal is biased to Vcc/2 (DC), therefore, you must use a coupling capacitor for cutting the DC.
⑥	VM2	Mid-point 2	To be connected to the output side GND(i.e. power amplifier)through capacitor C6.
⑦	OUT2	Output 2	This input terminal is biased to Vcc/2 (DC), therefore, you must use a coupling capacitor for cutting the DC.
⑧	Vcc	Power supply	Provide the single power source from a battery, etc. Generally, 12V or 24V will be supplied.
–	C1,C7	Output coupling capacitor	This capacitor removes the DC element. Generally, the capacitance of 10μF is selected.
–	C3,C5	Input coupling capacitor	This capacitor removes the DC element. Generally, the capacitance of 2.2μF is selected.
–	C2,C6	Capacitor for input signal grounding	This capacitor output in-phase signal with one-time of gain. You should select a proper value while taking the low range frequency of the common mode rejection ratio into consideration.(See the relevant graph.)

PRINCIPLE OF OPERATIONS

Since the car audios use the body as the ground, noise generated by other electric units flows into the power amplifier as the noise current. M5280 removes this noise by using the in-phase input rejection characteristics of the operational amplifier. The following describes the principle of the operation for removing the noise.

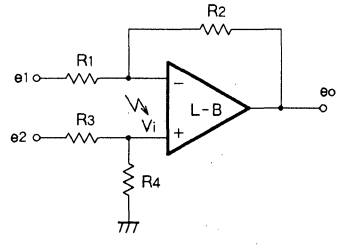
Flow of noise in an audio set



If M5280 is not used, noise will be input directly to the power amplifier. If it is used, the noise will be removed (or decreased) by the in-phase input rejection characteristics of the operational amplifiers R-B and L-B.

PRINCIPLE OF REMOVING THE NOISE

The following describes how to remove the noise using a channel (Lch). The equivalent circuit of the Lch can be written as follows because the operational amplifier L-A is an input buffer.



eo : Output voltage
e1, e2 : Noise voltage

To find the output voltage,

$$V_i = R_4/(R_3 + R_4) \cdot e_2 \quad \cdots\cdots ①$$

$$e_o = -\frac{R_2}{R_1} e_1 + \frac{R_1 + R_2}{R_1} \cdot V_i \quad \cdots\cdots ②$$

From the above equations, e_o becomes as follows :

$$e_o = -\frac{R_2}{R_1} e_1 + \frac{R_1 + R_2}{R_1} \cdot \frac{R_4}{R_3 + R_4} e_2$$

$$= -\frac{R_2}{R_1} \cdot (e_1 - e_2) + \frac{R_1R_4 - R_2R_3}{R_1 (R_3 + R_4)} e_2$$

If the following is true, the noise output voltage e_o is not generated.

$$R_1 \cdot R_4 = R_2 \cdot R_3 \left(\frac{R_1}{R_2} = \frac{R_3}{R_4}\right),\ e_1 = e_2$$

However, e_o will be generated due to the matching accuracy of resistors $R_1/R_2/$ and R_3/R_4, noise voltage difference, and the error of operational emplifiers.

M5280 shows the removable noise voltage (e_o) level as follows :

$$CMRR = 20 \log (e_o/e_i) \quad (= e_i = e_o)$$

Thus, M5280 guarantees CMRR ≧ 37dB.

M51143AL
TAPE PROGRAM SELECTOR CIRCUIT

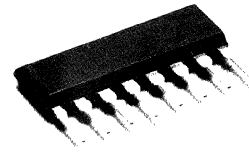
DESCRIPTION

The M51143AL is a semiconductor integrated circuit designed for use as a tape program selector with lead-in detection.

It has a built-in of a limiter amplifier, a signal detector, and a flip-flop circuit to prevent misoperation. The blank detector output is an open collector so that it is easy to make connections with counter-type integrated circuits.

FEATURES

- High-gain limiter amplifier ····· Gvo = 69dB typ (f = 1kHz)
- Built-in power-on reset circuit
- Built-in filter to prevent misoperation due to tape pop noise
- A built-in flip-flop circuit is used to shape the blank section detector output signal
- Minimum operating supply voltage ····· 3.5V



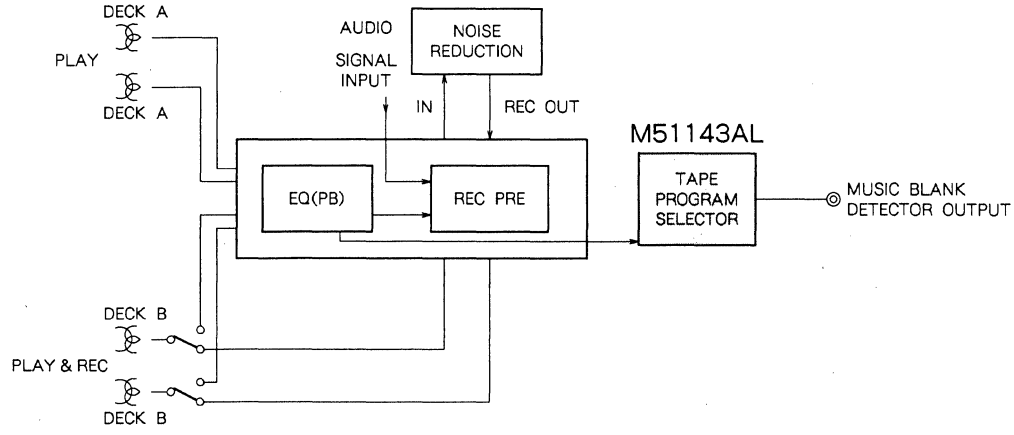
Outline 8P5

2.54mm pitch 340mil SIP
(2.8mm × 19.0mm × 6.4mm)

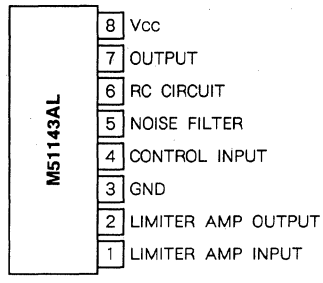
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ····· Vcc = 3.5~15V
Rated supply voltage ····· Vcc = 6V

SYSTEM CONFIGURATION

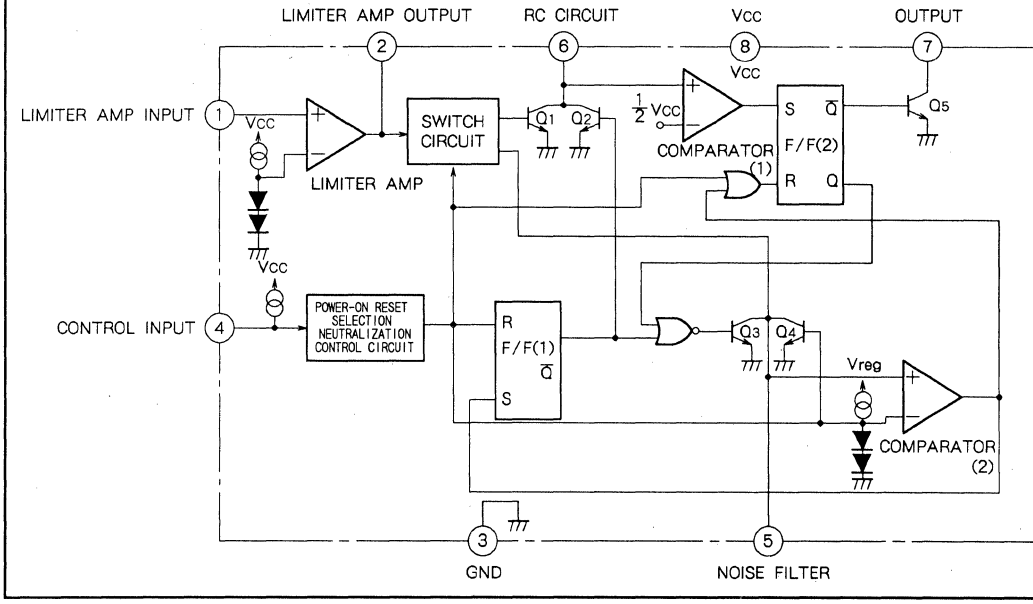


PIN CONFIGURATION



Outline 8P5

IC INTERNAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

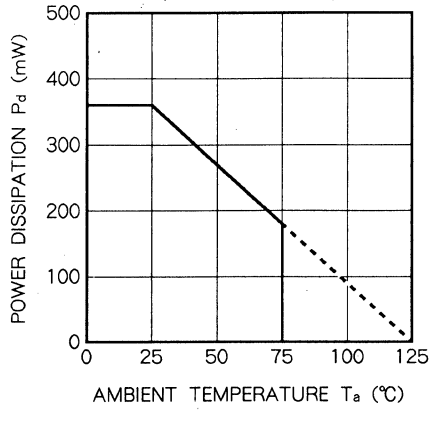
Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		16	V
I_O	Output current	V_{CC} = 6V	15	mA
P_d	Power disipation		360	mW
K_θ	Thermal derating	$T_a \geqq 25℃$	− 3.6	mW/℃
T_{opr}	Operating temperature		− 20～+ 75	℃
T_{stg}	Storage temperature		− 40～+ 125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 6V, unless otherwise noted)

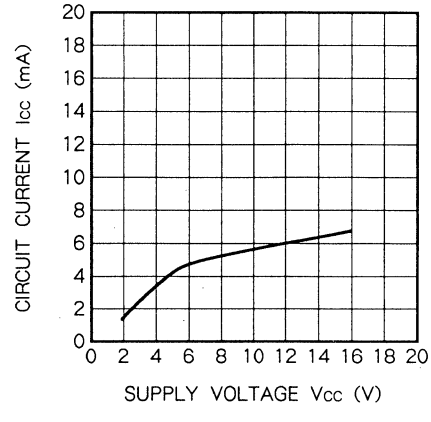
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Operating supply voltage		3.5	−	15	V
I_{CC}	Circuit current		−	3.5	6.5	mA
G_{VO}	Limiter amplifier open loop voltage gain	R_i = 10Ω, R_f = 750kΩ, f = 1kHz	64	69	−	dB
G_{VC}	Limiter amplifier closed loop voltage gain	R_i = 2kΩ, R_f = 750kΩ, f = 10kHz	47	51	54	dB
V_2	Switch circuit threshold	R_i = 2kΩ, R_f = 750kΩ, f = 10kHz	380	510	630	Vrms
I_{in}	RC circuit input current	V_6 = 1V, Quiescent condition after setting F/F(1)	−	− 0.1	− 0.6	μA
V_{th6}	Comparator (1) threshold voltage		2.5	3	3.5	V
I_{C4}	Control input charging current		3	12	30	μA
V_{th4}	Control input reset completion voltage		1.0	1.3	1.7	V
I_{C5}	Noise filter charging current		30	60	100	μA
V_{th5}	Comparator (2) threshold voltage		1.1	1.4	1.7	V
V_{OL}	Output voltage L	R_L = 1kΩ	−	−	0.4	V

TYPICAL CHARACTERISTICS

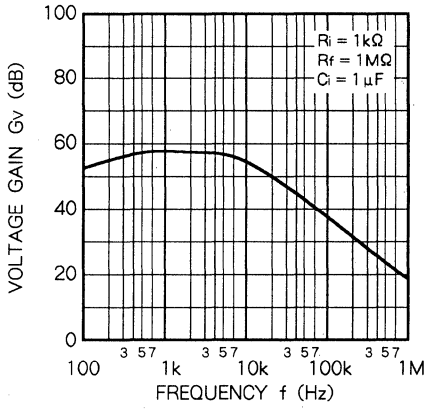
THERMAL DERATING (MAXIMUM RATING)



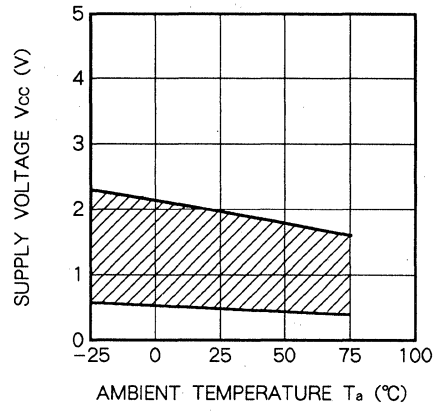
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



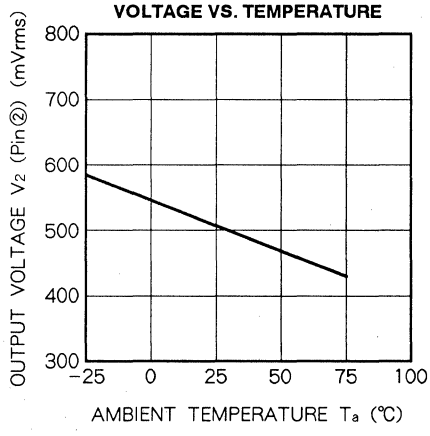
A LIMITER AMPLIFIER VOLTAGE GAIN VS. FREQUENCY



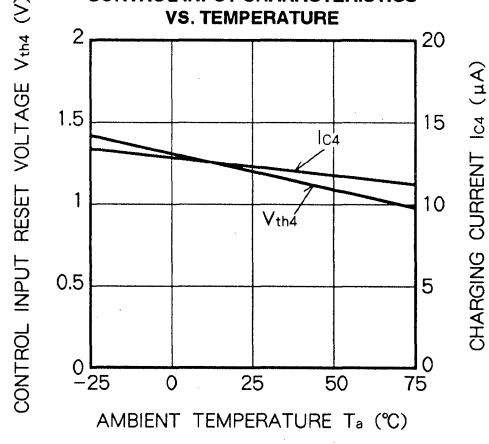
POWER-ON RESET TRANSISTOR ON REGION VS. TEMPERATURE



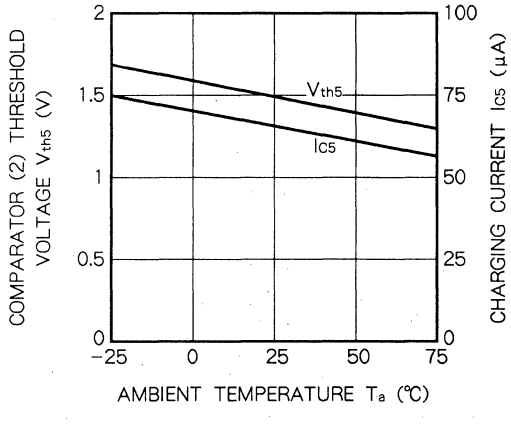
SWITCH CIRCUIT THRESHOLD VOLTAGE VS. TEMPERATURE



CONTROL INPUT CHARACTERISTICS VS. TEMPERATURE



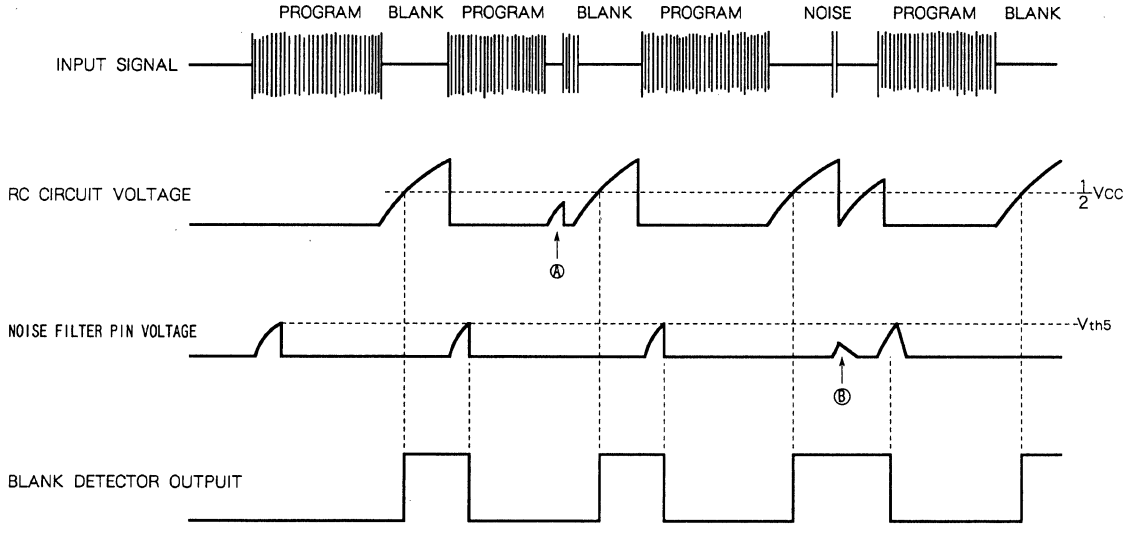
NOISE FILTER CHARACTERISTICS VS. TEMPERATURE



OPERATIONAL DESCRIPTION

1. The start of operation for the blank section detector occurs whenever the IC power supply is turned on or whenever the control input external switch has been turned off with the power applied to the device.
2. Whenever either of the above conditions occurs, the capacitor connected to the control input pin charges, and while it is charging to the control input reset completion voltage level the output of the control circuit is high, flip-fop (1) and (2) are reset, the operation of the switch circuit is disabled and the noise filter external capacitor discharges.
3. After this, the device shifts into the blank section detection mode, the input signal is accepted and the output of the limiter amplifier, when it exceeds the threshold of the switch circuit, causes the noise filter capacitor to charge. The charge on that capacitor, when it reaches the threshold voltage of comparator (2), causes comparator (2) output to go high, setting flip-flop (1) and resetting flip-flop (2).
4. When the blank section mode is started, flip-flop (1) prevents the false detection of a blank section should the startup be happening during a blank section upon turn-on. It maintains this state until the first true detection of a recorded section at which time it is set and remains set for the remaining operations, until the program selection mode is ended. This prevention of false blank sections by flip-flop (1) is accomplished by turning transistor Q_2 on.
5. When flip-flop (1) is set, the output Q of it goes low, flip-flop (2) is reset and its output Q goes low, turning transistor Q_3 on, causing the external capacitor attached to the noise filter pin to discharge.
6. When the tape is passing through a recorded selection, the operation of the switch circuit is such that the transistor Q_1 turns on and the RC circuit pin goes low.
7. When a non-recorded, blank section is reached, Q_1 goes off, capacitor C_1 discharges at the time constant of the R1C1 combination. When the charged voltage reaches 1/2 Vcc, if the tape is still passing through a non-recorded section, a true blank section has been detected and the output goes high, setting flip-flop (2).
8. When flip-flop (2) is set, its output Q goes low, turning transistor Q_5 off, whose open collector output then goes high, outputing the information that a blank section has been detected.
9. The state of the IC returns to step 3 above until the selection mode is ended by the circuit connected to the ICs output.

TIMING DIAGRAM



- The section Ⓐ is too short to be detected as a true blank section.
- There was a capacitor charge up due to the noise encountereed a Ⓑ but the charged voltage did not reach the threshold Vth5, so the blank detector output does not invert to a low level.

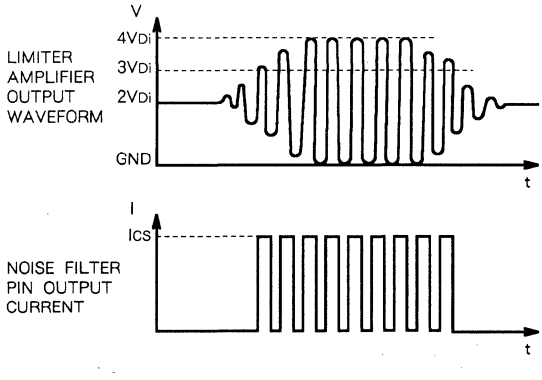
PIN DESCRIPTION

1. Limiter amplifier input (pin ①)

The limiter amplifier is a PNP transistor input operational amplifier. The pin 1 input corresponds to the inverting input of the amplifier. The non-inverting input is biased internally to a voltage of $2V_{Di}$ (approximately 1.4V), making the DC voltage on this pin also approximately 1.4V. The voltage gain of the limiter amplifier is determined by the ratio of the feedback resistance Rf presented between output pin 2 to the input pin and the signal input resistance Ri, as expressed in the equation $G_V = 20 \log (R_f / R_i)(dB)$. The capacitor connected between the input resistance and the equalizer amplifier is a DC blocking capacitor Ci and forms a high-pass filter in combination with the input resistance, which has a cutoff of $1/(2\pi CiRi)$. For use with stereo equipment, it is necessary to provide mixing, using two input resistors. For this reason, a switch must be used to disable the program selection function when not required by using either an external mechanical switch of NPN transistor switch. If the limiter amplifier gain is set to below about 20dB there is a danger of it going into oscillation, so a capacitance should be connected in parallel with the feedback resistance.

2. Limiter amplifier output (pin ②)

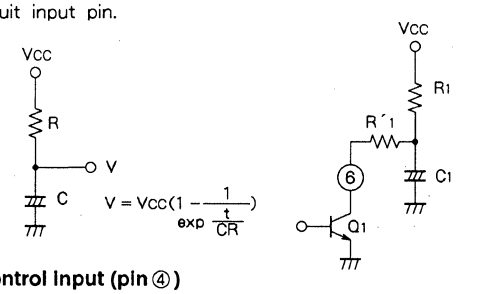
With a non-inverting input bias of $2V_{Di}$ (approximately 1.4V), the limiter amplifier output becomes the quiescent value about which the output signal switngs. The output varies from ground to $4V_{Di}$ (approximately 2.8V) and is limited to this range by the circuit. Internally, a switch circuit consisting of a switch and a comparator is connected to this pin. The comparator threshold is set to $3V_{Di}$ (approximately 2.1V) so that when the limiting amplifier output exceeds this level, the transistor Q_1 is turned on simultaneously with the output of a constant charging current for the noise filter pin. The diagram illustrates how this constant current output begins when the limiter amplifier output reaches and exceeds the threshold.



3. RC circuit pin (pin ⑥)

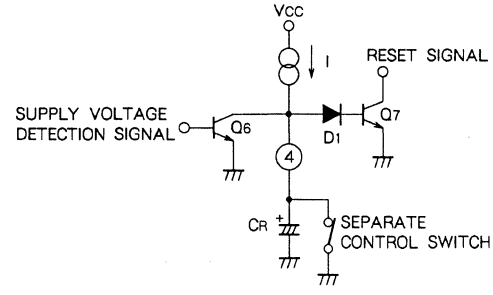
This pin allows connection of the RC circuit which determines the time constant for detection of a true blank section on the tape. Since the threshold of the time limit detector is set at 1/2 Vcc, the time required to reach 1/2Vcc from the equation below becomes $C_1R_1 \times \ln 2 = 0.69C_1R_1$ seconds.

Note that pop noise occurring before the detector threshold has been reached will cause Q_1 to turn on and cause a momentary discharge of the time constant determining capacitor, thus requiring the same time constant again before the detector output is triggered. This effectively lengthens the required time for blank sections and could result in blank sections being missed. To prevent this, an improvement in the form of a resistor R'_1 can be connected between the junction of R_1 and C_1 and the RC circuit input pin.



4. Control Input (pin ④)

This pin is provided to ensure reliable operation, whether the program selection mode is initialized by a separate control switch or simultaneously upon application of power to the circuit. For power on operation, transistor Q_6 is used. It turns on at approximately 1 to 2 volts and discharges the externally connected capacitor. For operation using a separate control switch, the capacitor is discharged when the switch is turned off. After this, the internal charging current flows through the capacitor, to charge it to the voltage at pin ④. When this voltage turns on Q_7 through the diode D_1, the reset operation is completed. A pin ④ voltage of approximately 1.1V will turn on Q_7 and the charging current is approximately 10μA so that the time for the reset operation is given approximately by the expression $C_R (V_{th4}/I_{C4})$ is approximately $0.11 \times C_R$ (μF) seconds.



5. Noise filter (pin ⑤)

The noise filter pin is provided to prevent the false interpretation of pop noise as the start of a new program. In actual operation, a charging current is provided for an externally connected capacitor when a program has been detected. When the charging causes the pin voltage to reach $2V_{Di}$, (approx. 1.3V) comparator (2) operates, as indicated in the block diagram. The charging current is approximately 1/2 of the static charge current for (I_{C5}) or 60μA (refer to section 2) so that the time required for this detection is given by the expression which follows.

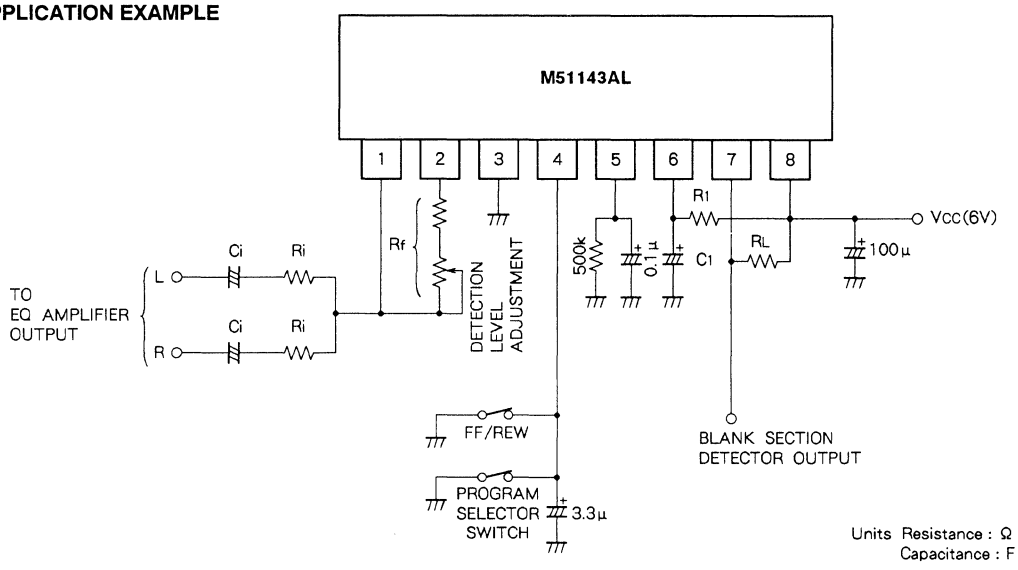
$$C_N \frac{V_{th5}}{0.5 I_{C5}} \fallingdotseq 0.04 \times CN \ (\mu F) \text{ seconds}$$

So that the type of pop noise illustrated in the figure at point Ⓑ is not falsely detected as a new program, it is recommended that a discharging resistance be connected in parallel with the external capacitor. Care should be taken however, as the use of a low value of resistance will lengthen the time required for the reset operation previously described. Note also that, depending upon the input signal level, the effective charging current may fall below 1/2 (50% duty cycle), thereby requiring more time for detection.

6. Output (pin ⑦)

This pin is used to output the signal indicating that the section between programs has been detected. It is implemented in open collector connection with an NPN transistor. When detection occurs, the transistor is turned off, driving the output high by virtue of the externally connected pull-up resistor. The timing of the output of the detector is such that it goes high when passing from a recorded program into a blank unrecorded section to a program section after the time constant determined by the noise filter pin external components. For this reason, the amount of time that the detector output is high is almost completely determined by the amount of time the recorded tape has devoted to blank spaces (unrecorded areas). If there is the danger of miscounting the blank areas because of the length of the detected output, some sort of misoperation protection must be provided. Also, for cycling of the detector upon powering up the IC, the transistor Q_5 is off for supply voltages in the range 0 through 0.8V. For the case where the load resistance is applied to an already powered up power supply, after the output voltage transits from high to low, normal program selection operation begins, If the load resistance power source is the same as that for this IC, the maximum startup error operation high-level output voltage will be about 0.8V.

APPLICATION EXAMPLE



- The limiter amplifier gain is determined by the relationship $G_V = 20 \log \left(\frac{Rf}{Ri}\right)$ (dB)
- To compensate for variations in the limiter amplifier output level and in the switch circuit threshold levels, it is desirable to make the feedback resistance value variable.
- For this example, operation of the program selector occurs whenever both the program selector switch and FF/Rewind switches are both off.
- The blank section detector output is high when a blank section has been detected.

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