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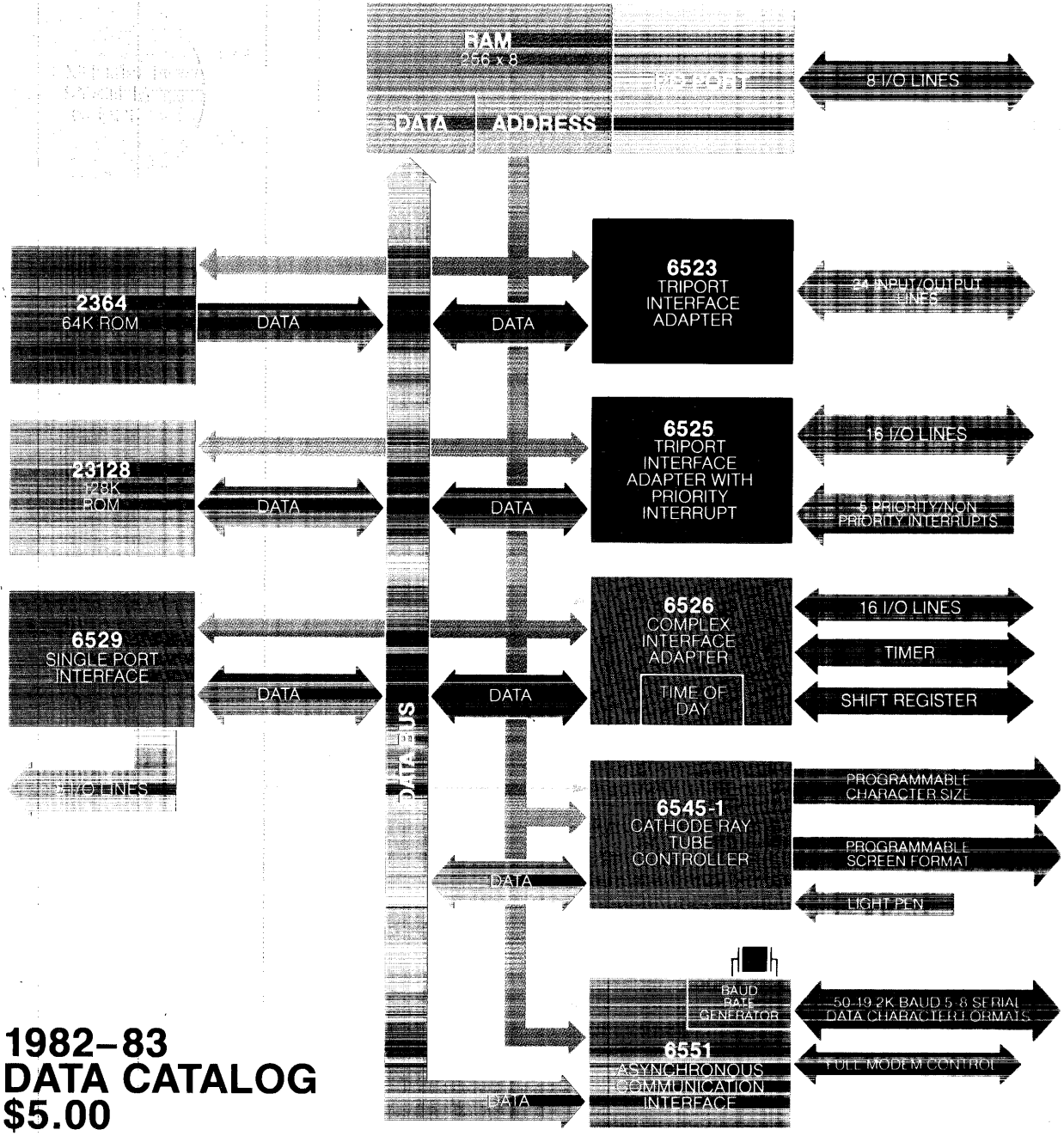
A Commodore Company

NMOS
CMOS
LCD



1982–83
DATA CATALOG
$5.00

MOS Technology
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1982
COMPONENT DATA CATALOG

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PRODUCT CROSS REFERENCE GUIDE

ROM

AMD Part No.	Commodore Replacement Part
AM9217BPC	MPS2316
AM9217BDC	MCS2316
AM9232BPC	MPS2332
AM9232BDC	MCS2332

AMI	Commodore
S68316A	MPS2316
S68332	MPS2332

EA	Commodore
EA2316B	MPS2316
EA2332	MPS2332

G.I.	Commodore
RO-3-9316B	MPS2316
RO-3-9332B	MPS2332

Intel	Commodore
P2316B	MPS2316
C2316B	MCS2316
P2332	MPS2332
C2332	MCS2332

Motorola	Commodore
MCM68316B	MPS2316
MCM68332	MPS2332

National	Commodore
MM2316B	MPS2316
MM52132	MPS2332
MM52164	MPS2364

NEC	Commodore
UPD2316B	MPS2316
UPD2332	MPS2332
UPD2364	MPS2364

Signetics Part No.	Commodore Replacement Part
2632N	MPS2332
2664N	MPS2364

T.I.	Commodore
TMS4732NL	MPS2332
TMS4732JL	MCS2332
TMS4764NL	MPS2364
TMS4764JL	MCS2364

Mostek	Commodore
MK31000N-3	MCS2316
MK31000P-3	MPS2316
MK36000P-5	MPS2364
MK36000N-5	MCS2364

MICROPROCESSORS

Synertek	Commodore
SYP=Plastic	MPS=Plastic
SYC=Ceramic	MCS=Ceramic
SYP/C6502	MPS/CS6502
SYP/C6503	MPS/CS6503
SYP/C6504	MPS/CS6504
SYC/C6505	MPS/CS6505
SYP/C6506	MPS/CS6506
SYP/C6507	MPS/CS6507
SYP/C6512	MPS/CS6512
SYP/C6513	MPS/CS6513
SYP/C6514	MPS/CS6514
SYP/C6515	MPS/CS6515
A=2MHz	A=2MHz
B=3MHz	B=3MHz
SYP/C6502A	MPS/CS6502A
SYP/C6502B	MPS/CS6502B
SYP/C6503A	MPS/CS6503A
SYP/C6503B	MPS/CS6503B
SYP/C6504A	MPS/CS6504A

Synertek Part No.	Commodore Replacement Part
SYP/C6504B	MPS/CS6504B
SYP/C6505A	MPS/CS6505A
SYP/C6505B	MPS/CS6505B
SYP/C6506A	MPS/CS6506A
SYP/C6506B	MPS/CS6506B
SYP/C6507A	MPS/CS6507A
SYP/C6507B	MPS/CS6507B
SYP/C6512A	MPS/CS6512A
SYP/C6512B	MPS/CS6512B
SYP/C6513A	MPS/CS6513A
SYP/C6513B	MPS/CS6513B
SYP/C6514A	MPS/CS6514A
SYP/C6514B	MPS/CS6514B
SYP/C6515A	MPS/CS6515A
SYP/C6515B	MPS/CS6515B
SYP6520	MPS6520
SYP6520A	MPS6520A
SYC6520	MCS6520
SYC6520A	MCS6520A
SYP6522	MPS6522
SYP6522A	MPS6522A
SYC6522	MCS6522
SYC6522A	MCS6522A
SYP6530	MPS6530
SYC6530	MCS6530
SYP6532	MPS6532
SYP6532A	MPS6532A
SYC6532	MCS6532
SYC6532A	MCS6532A
SYP6545-1	MPS6545-1
SYC6545-1	MCS6545-1
SYP6551	MPS6551
SYC6551	MCS6551

Rockwell	Commodore
R6502P	MPS6502
R6502AP	MPS6502A
R6502C	MCS6502
R6502AC	MCS6502A
R6503P	MPS6503

PRODUCT CROSS REFERENCE GUIDE

MICROPROCESSORS (CONT.)

Rockwell Part No.	Commodore Replacement Part
R6503AP	MPS6503A
R6503AC	MCS6503A
R6504P	MPS6504
R6504AP	MPS6504A
R6504C	MCS6504
R6504AC	MCS6504A
R6505P	MPS6505
R6505AP	MPS6505A
R6505C	MCS6505
R6505AC	MCS6505A
R6506P	MPS6506
R6506AP	MPS6506A
R6506C	MCS6506
R6506AC	MCS6506A
R6507P	MPS6507
R6507AP	MPS6507A
R6507C	MCS6507
R6507AC	MCS6507A
R6512P	MPS6512
R6512AP	MPS6512A
R6512C	MCS6512
R6512AC	MCS6512A
R6513P	MPS6513
R6513AP	MPS6513A
R6513C	MCS6513
R6513AC	MCS6513A
R6514P	MPS6514
R6514AP	MPS6514A
R6514C	MCS6514
R6514AC	MCS6514A
R6515P	MPS6515
R6515AP	MPS6515A
R6515C	MCS6515
R6515AC	MCS6515A
R6520P	MPS6520
R6520AP	MPS6520A
R6520C	MCS6520
R6520AC	MCS6520A
R6522P	MPS6522
R6522AP	MPS6522A
R6522C	MCS6522
R6522AC	MCS6522A
R6530P	MPS6530
R6530C	MCS6530
R6532P	MPS6532
R6532AP	MPS6532A
R6532C	MCS6532
R6532AC	MCS6532A
R6500/IP	MPS6500/I
R6500/IAP	MPS6500/IA
R6500/IC	MCS6500/I
R6500/IAC	MCS6500/IA
R6545-IP	MPS6545-I
R6545-IC	MCS6545-I
R6551P	MPS6551
R6551C	MCS6551

Motorola	Commodore
MC6820	MPS6520
MC6821	MPS6520
MC68B21	MPS6520A
MC6845	MPS6545-1

AMI	Commodore
S6821	MPS6520
S68B21	MPS6520A

SECTION 2

NMOS

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NMOS

MPS
6500/1
ONE-CHIP
MICROCOMPUTER

6500/1 ONE-CHIP MICROCOMPUTER

INTRODUCTION

The MOS Technology 6500/1 is a complete, high-performance 8-bit NMOS microcomputer on a single chip, and is totally upward/downward software compatible with all members of the 6500 family.

The 6500/1 consists of a 6502 CPU, an internal clock oscillator, 2048 bytes of Read Only Memory (ROM), 64 bytes of Random Access Memory (RAM) and flexible interface circuitry. The interface circuitry includes a 16-bit programmable counter/latch with four operating modes, 32 bidirectional input/output lines (including two edge-sensitive lines), five interrupts and a counter I/O line.

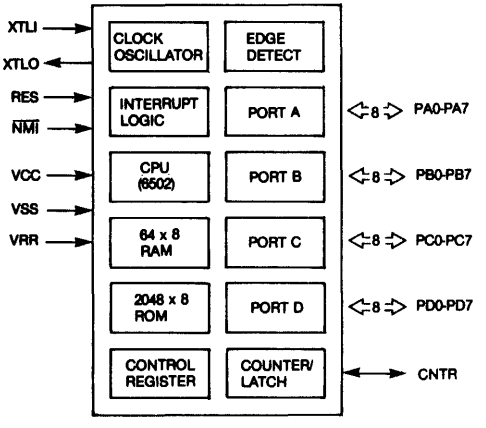
PRODUCT SUPPORT

To allow prototype circuit development, Mos Technology offers a PROM compatible 64-pin Emulator device. This device provides all 6500/1 interface lines plus routing the address bus, data bus, and associated control lines off the chip to be connected to external memory.

ORDERING INFORMATION

Order Number	Package Type	Frequency Option	Temperature Range
MPS6500/1	Plastic	1 MHz	0°C to 70°C
MCS6500/1	Ceramic	1 MHz	0°C to 70°C
MPS6500/1A	Plastic	2 MHz	0°C to 70°C
MCS6500/1A	Ceramic	2 MHz	0°C to 70°C
MCS6500/1E	Emulator Device	1MHz	
MCS6500/1EA	Emulator Device	2MHz	

Note: The RC frequency option is available only in the 1 MHz 6500/1.



Interface Diagram

FEATURES

- 6502 CPU
  - —Software upward/downward compatibility
  - —Decimal or binary arithmetic modes
  - —13 addressing modes
  - —True direct and indirect indexing
  - —Memory addressable I/O
- 2048 x 8 mask programmable ROM
- 64 x 8 static RAM
- 32 bi-directional TTL compatible I/O lines (4 ports)
- 1 bi-directional TTL compatible counter I/O line
- 16-bit programmable counter/latch with four modes
  - —Interval Timer —Event Counter
  - —Pulse Generator —Pulse Width Measurement
- Five Interrupts
  - —Reset —Two external edge sensitive
  - —Non-maskable —Counter
- 1 of 3 frequency references
  - —Crystal —Clock —RC (resistor only)
- 4 MHz max crystal or clock external frequency
- 2 MHz or 1 MHz internal clock
- 1 μs minimum instruction execution
- N-channel, silicon gate, depletion load technology
- Single +5V power supply
- 500 mW operating power
- Separate power pin for RAM
- 40 pin DIP
- 64 pin PROM compatible Emulator device

FUNCTIONAL DESCRIPTION

CENTRAL PROCESSING UNIT (CPU)

Clock Oscillator

The Clock Oscillator provides the basic timing signals used by the 6500/1 CPU. The reference frequency is provided by an external source, and can be from a crystal, clock or RC network input. The RC network mode is a mask option. The external frequency can vary from 200 kHz to 4 MHz. The internal Phase 2 (Ø2) frequency is one-half the external reference frequency. A 4.7K ohm resistor will provide nominal 2 MHz oscillation and 1 MHz internal operation in the RC mask option (±35%).

Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. Each data transfer which takes place between the registers is caused by decoding the contents of both the Instruction Register and Timing Control Logic.

Program Counter

The 16-bit Program Counter provides the addresses which step the CPU through sequential instructions in a program. The Program Counter is incremented each time an instruction or data is fetched from memory.

Instruction Register and Decode

Instructions fetched from memory are gated onto the internal Data Bus. These instructions are latched into the Instruction Register then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter).

Accumulator

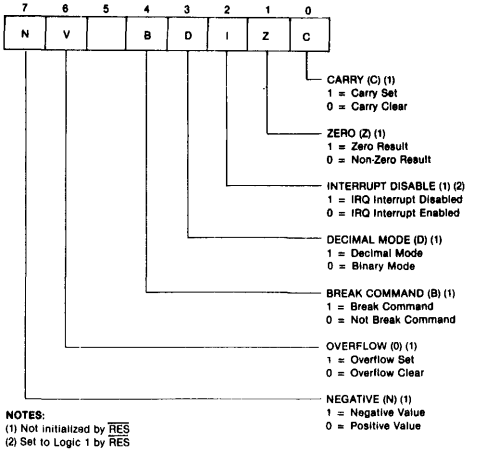
The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

Index Registers

There are two 8-bit index registers, X and Y. These registers can be used for general purpose storage, or as a displacement to modify the base address and thus obtain a new effective address. Pre- or post-indexing of indirect addresses is possible.

Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the CPU to perform stack manipulation under direction of either the program or interrupts NMI and IRQ. The stack allows simple implementation of nested subroutines and multiple level interrupts.



Processor Status Register

Processor Status Register

The 8-bit Processor Status Register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; RES, NMI and IRQ. IRQ is generated by any one of three conditions: Counter Overflow, PA0 Positive Edge Detected, and PA1 Negative Edge Detected.

MEMORY

2048 x 8 ROM

The 2048 byte Read-Only Memory (ROM) contains the program instructions and other fixed constants. These program instructions and constants are mask programmed into the ROM during fabrication of the 6500/1 device. The 6500/1 ROM is memory mapped from 800 to FFF.

64 x 8 RAM

The 64 byte Random Access Memory (RAM) is used for read/write memory during system operation, and contains the stack. This RAM is completely static in operation and requires no clock or dynamic refresh. A standby power pin, VRR, allows RAM memory to be maintained on 10% of the operating power in the event that VCC power is lost.

In order to take advantage of efficient zero page addressing capabilities, the RAM is assigned memory addresses 0 to 03F.

INPUT/OUTPUT

Bidirectional I/O Ports

The 6500/1 provides four 8-bit input/output ports (PA, PB, PC, and PD). Associated with the I/O ports are four 8-bit registers located on page zero. See the system memory map for specific addresses. Each I/O line is individually selectable as an input or an output without line grouping or port association restrictions.

An internal active transistor drives each I/O line to the low state. An internal passive resistance pulls the I/O lines to the high state, eliminating the need for external pull-up resistors.

An option is available to delete the internal pull-up resistance on 8-bit port groups or on the CNTR line at mask time. This option is employed to permanently assign an 8-bit port group to input functions, to interface with CMOS drivers, or to interface with external pull-up devices.

Inputs

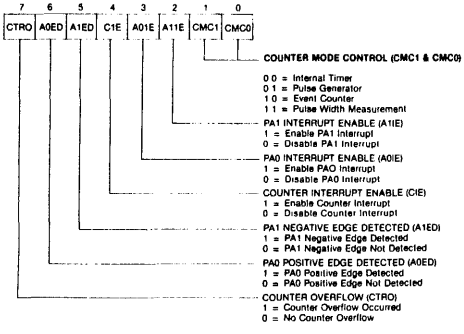
Inputs are enabled by setting the appropriate bit of the I/O port to the high state (Logic 1). A low input signal causes a logic 0 to be read. A high input signal causes a logic 1 to be read. $\overline{RES}$ loads Logic 1 into the I/O ports, thereby initializing all I/O lines as inputs.

Outputs

Outputs are set by loading the desired bit pattern into the corresponding I/O ports. A Logic 1 selects a high output; a Logic 0 selects a low output.

CONTROL REGISTER

The Control Register (CR) controls four Counter operating modes and three maskable interrupts. It also reports the status of three interrupt conditions. There are five control bits and three status bits. The control bits are set to Logic 1 or cleared to Logic 0 by writing the desired state into the respective bit positions. The Control Register is cleared to Logic 0 by the occurrence of $\overline{RES}$.



Control Register

EDGE DETECT CAPABILITY

There is an asynchronous edge detect capability on two of the Port A I/O lines. This capability exists in addition to and independently from the normal Port A I/O functions. The maximum rate at which an edge can be detected is one-half the ∅2 clock rate. The edge detect logic is continuously active. Each edge detect signal is associated with a maskable interrupt.

PA0 Positive Edge Detection

A positive (rising) edge is detectable on PA0. When this edge is detected, the PA0 Positive Edge Detected bit—Bit 6 in the Control Register—is set to Logic 1. When both this bit and the PA0 Interrupt Enable Bit—Bit 3 of the Control Register—are set to Logic 1, an $\overline{IRQ}$ interrupt request is generated. The PA0 Positive Edge Detected bit is cleared by writing to address 089.

PA1 Negative Edge Detection

A negative (falling) edge is detectable on PA1. When this edge is detected, the PA1 Negative Edge Detected bit—Bit 5 of the Control Register—is set to Logic 1. When both this bit and the PA1 Interrupt Enable bit—Bit 2 of the Control Register—are set to Logic 1, an $\overline{IRQ}$ interrupt request is generated. The PA1 Negative Edge Detected bit is cleared by writing to address 08A.

COUNTER/LATCH

The Counter/Latch consists of a 16-bit decrementing Counter and a 16-bit Latch. The Counter is comprised of two 8-bit registers. Address 086 contains the Upper Count (UC) and address 087 contains the Lower Count (LC). The Counter counts either ∅2 clock periods or occurrences of an external event, depending on the selected counter mode. The UC and LC can be read at any time without affecting counter operation.

The Latch contains the Counter preset value. The Latch consists of two 8-bit registers. Address 084 contains the Upper Latch (UL) and address 085 contains the lower latch (LL). The 16-bit Latch can hold a count from 0 to 65,535. The Latch can be accessed as two write-only memory locations.

The Latch registers can be loaded at any time by storing into UL and LL. The UL can also be loaded by writing into address 088.

The Counter can be preset at any time by writing to address 088. Presetting the Counter in this manner causes the contents of the accumulator to be stored into the UL before the 16-bit value in the Latch (UL and LL) is transferred in the Counter (UC and LC).

The Counter is preset to the Latch value when the Counter overflows. When the counter decrements from 0000, Counter overflow occurs causing the next counter value to be the Latch value, not FFFF.

When the Counter overflows, Counter Overflow bit—Bit 7 of the Control Register—is set to Logic 1. When both this bit and the Counter Interrupt Enable bit—Bit 4 of the Control Register—are set, an $\overline{IRQ}$ interrupt request is generated. The Counter Overflow bit in the Control Register can be examined in an $\overline{IRQ}$ interrupt service routine to determine that the $\overline{IRQ}$ was generated by Counter overflow.

The Counter Overflow bit is cleared when the LC is read or Counter preset is performed by writing into address 088.

COUNTER MODES

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register.

Mode	CMC 1	CMC 0
Interval Timer	0	0
Pulse Generator	0	1
Event Counter	1	0
Pulse Width Measurement	1	1

The Interval Timer, Pulse Generator, and Pulse Width Measurement Modes are ∅2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

Interval Timer (Mode 0)

In this mode the Counter is free running and decrements at the ∅2 clock rate. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value.

The CNTR line is held in the high state.

Pulse Generator (Mode 1)

In this mode the Counter is free running and decrements at the ∅2 clock rate. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value.

The CNTR line toggles from one state to the other when Counter overflow occurs. Writing to address 088 will also toggle the CNTR line.

A symmetric or asymmetic output waveform can be generated on the CNTR line in this mode. A one-shot waveform can easily be generated by changing from Mode 1 to Mode 0 after only one occurrence of the output toggle condition.

Event Counter (Mode 2)

In this mode the CNTR line is used as an event input line. The Counter decrements each time a rising edge is detected on CNTR. The maximum rate at which this edge can be detected is one-half the ∅2 clock rate. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value.

Pulse Width Measurement (Mode 3)

This mode allows the accurate measurement of the duration of a low state on the CNTR line. The Counter decrements at the ∅2 clock rate as long as the CNTR line is held in the low state. The Counter is stopped when CNTR is in the high state. If the CNTR pin is left disconnected, this mode may be selected to stop the Counter since the internal pull-up device will cause the CNTR input to be in the high state.

RESET CONSIDERATIONS

The occurrence of $\overline{RES}$ going from low to high causes initialization of various conditions in the 6500/1. All of the I/O ports (PA, PB, PC, and PD) and CNTR are forced to the high (Logic 1) state. All bits of the Control Register are reset to Logic 0, causing the Interval Timer Mode (Mode 0) to be selected and all interrupt enabled bits to be cleared. Neither the Latch nor the Counter registers are initialized by $\overline{RES}$. The Interrupt Disable bit in the CPU Processor Status Register is set and the program starts execution at the address contained in the Reset Vector location.

TEST LOGIC

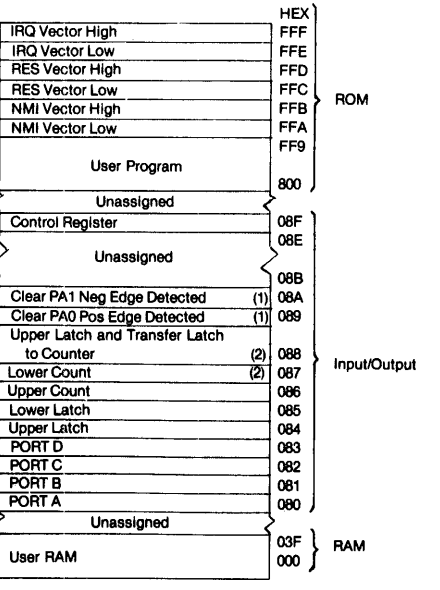
Special test logic provides a method for thoroughly testing the 6500/1. Applying a + 10V signal to the $\overline{RES}$ line places the 6500/1 in the test mode. While in this mode, all memory fetches are made from Port PC. External test equipment can use this feature to test internal CPU logic and I/O. A program can be loaded into RAM allowing the contents of the instruction ROM to be dumped to any port for external verification.

All 6500/1 microcomputers are tested by MOS Technology using this feature.

MEMORY ADDRESSABLE I/O

The I/O ports, registers, and commands are treated as memory and are assigned specific addresses. See the system memory map for the addresses. This I/O technique allows the full set of CPU instructions to be used in the generation and sampling of I/O commands and data. When an instruction is executed with an I/O address and appropriate R/W state, the corresponding I/O function is performed.

SYSTEM MEMORY MAP

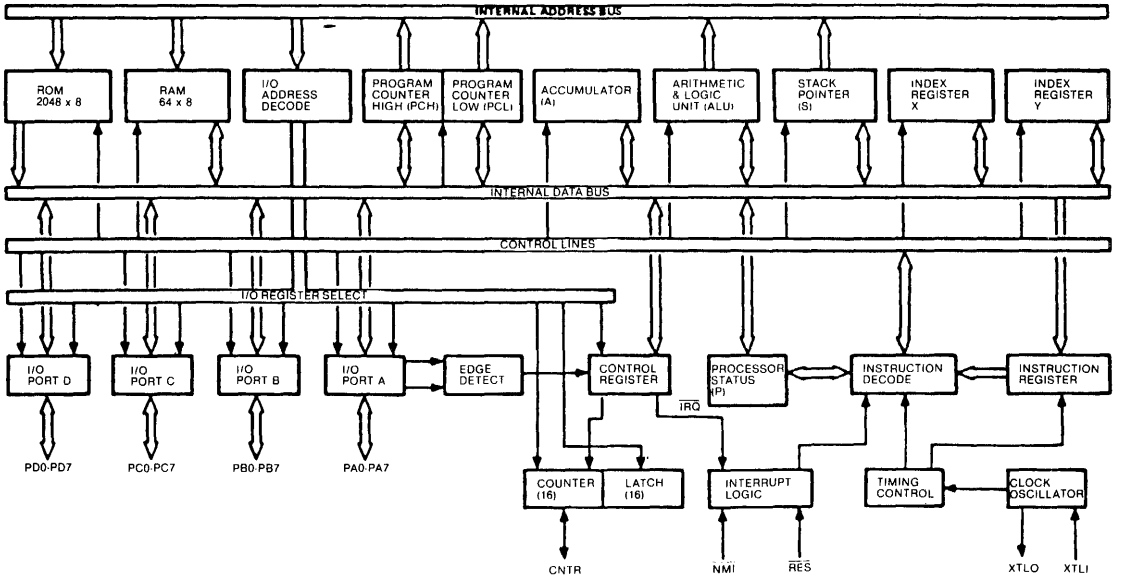


Notes:
(1) I/O command only; i.e., no stored data.
(2) Clears Counter Overflow—Bit 7 in Control Register.

INSTRUCTION SET—ALPHABETIC SEQUENCE

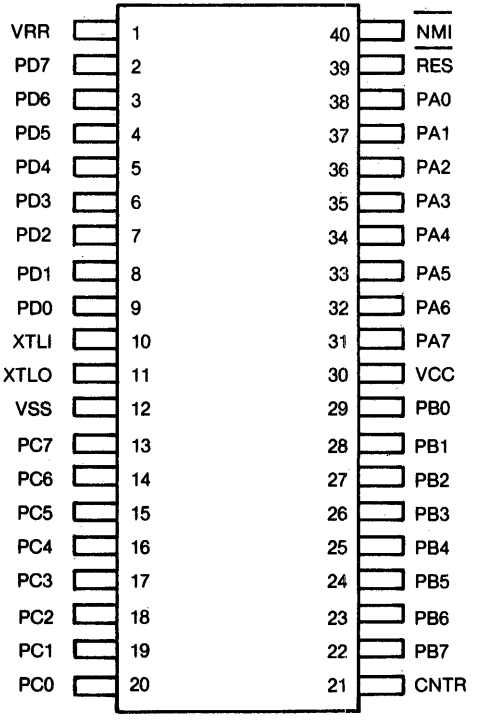
ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift Left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Register
TYA	Transfer Index Y to Accumulator

6500/1 Block Diagram



SIGNAL DESCRIPTIONS

SIGNAL NAME	PIN NO.	DESCRIPTION
VCC	30	Main power supply +5V
VRR	1	Separate power pin for RAM. In the event that VCC power is lost, this power retains RAM data.
VSS	12	Signal ground
XTLI	10	Crystal, clock or RC network input for internal clock oscillator.
XTLO	11	Crystal or RC network output from internal clock oscillator.
$\overline{RES}$	39	The Reset input is used to initialize the 6500/1. This signal must not transition from low to high for at least eight cycles after VCC reaches operating range and the internal oscillator has stabilized. +10V input enables the test mode.
$\overline{NMI}$	40	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	38-31 29-22 20-13 9-2	Four 8 bit ports used for either input/output. Each line consists of an active transistor to VSS and a passive pull-up to +5V. The two lower bits of the PA port (PA0 and PA1) also serve as edge detect inputs with maskable interrupts.
CNTR	21	This line is used as a Counter input/output line. CNTR is an input in the Event Counter and Pulse Width Measurement modes and is an output in the Interval Timer and Pulse Generator modes.



Pin Configuration

ADDRESSING MODES

ACCUMULATOR ADDRESSING—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING—In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits.

ZERO PAGE ADDRESSING—The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING—In indexed indirect addressing (referred to as [Indirect, X]), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING—In indirect indexed addressing (referred to as [Indirect, Y]), the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location are contained in the third byte of the instruction. The contents of the fully specified memory location are the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET

INSTRUCTION SET – OP CODES, Execution Time, Memory Requirements

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y			CONDITION CODES					
MNEMONIC	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										✓	✓	✓	–	–	✓
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										✓	✓	–	–	–	–
ASL	C ← 7 … 0 ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													✓	✓	✓	–	–	–
BCC	BRANCH ON C=0 (2)																															90	2	2							–	–	–	–	–	–
BCS	BRANCH ON C=1 (2)																															B0	2	2							–	–	–	–	–	–
BEQ	BRANCH ON Z=1 (2)																															F0	2	2							–	–	–	–	–	–
BIT	A ∧ M				2C	4	3	24	3	2																															M7	✓	–	–	–	M6
BMI	BRANCH ON N=1 (2)																															30	2	2							–	–	–	–	–	–
BNE	BRANCH ON Z=0 (2)																															D0	2	2							–	–	–	–	–	–
BPL	BRANCH ON N=0 (2)																															10	2	2							–	–	–	–	–	–
BRK	(See Fig. 1)													00	7	1																									–	–	–	1	–	–
BVC	BRANCH ON V=0 (2)																															50	2	2							–	–	–	–	–	–
BVS	BRANCH ON V=1 (2)																															70	2	2							–	–	–	–	–	–
CLC	0 → C													18	2	1																									–	–	0	–	–	–
CLD	0 → D													D8	2	1																									–	–	–	–	0	–
CLI	0 → I													58	2	1																									–	–	–	0	–	–
CLV	0 → V													B8	2	1																									–	–	–	–	–	0
CMP	A-M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										✓	✓	✓	–	–	–
CPX	X-M	E0	2	2	EC	4	3	E4	3	2																															✓	✓	✓	–	–	–
CPY	Y-M	C0	2	2	CC	4	3	C4	3	2																															✓	✓	✓	–	–	–
DEC	M-1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													✓	✓	–	–	–	–
DEX	X-1 → X													CA	2	1																									✓	✓	–	–	–	–
DEY	Y-1 → Y													88	2	1																									✓	✓	–	–	–	–
EOR	A ⊻ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										✓	✓	–	–	–	–
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													✓	✓	–	–	–	–
INX	X + 1 → X													E8	2	1																									✓	✓	–	–	–	–
INY	Y + 1 → Y													C8	2	1																									✓	✓	–	–	–	–
JMP	JUMP TO NEW LOC				4C	3	3																													6C	5	3				–	–	–	–	–	–
JSR	(See Fig. 2) JUMP SUB				20	6	3																																		–	–	–	–	–	–
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										✓	✓	–	–	–	–

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y			CONDITION CODES					
MNEMONIC	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3										✓	✓	–	–	–	–
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2																															✓	✓	–	–	–	–
LSR	0 → 7 … 0 → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0	✓	✓	–	–	–
NOP	NO OPERATION													EA	2	1																									–	–	–	–	–	–
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										✓	✓	–	–	–	–
PHA	A → Ms S-1 → S													48	3	1																									–	–	–	–	–	–
PHP	P → Ms S-1 → S													08	3	1																									–	–	–	–	–	–
PLA	S+1 → S Ms → A													68	4	1																									✓	✓	–	–	–	–
PLP	S+1 → S Ms → P													28	4	1																									(RESTORED)					
ROL	7 … 0 ← C				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													✓	✓	✓	–	–	–
ROR	C → 7 … 0 → C				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													✓	✓	✓	–	–	–
RTI	(See Fig. 1) RTRN INT													40	6	1																									(RESTORED)					
RTS	(See Fig. 2) RTRN SUB													60	6	1																									–	–	–	–	–	–
SBC	A-M-C̄ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										✓	✓	(3)	–	–	✓
SEC	1 → C													38	2	1																									–	–	1	–	–	–
SED	1 → D													F8	2	1																									–	–	–	–	1	–
SEI	1 → I													78	2	1																									–	–	–	1	–	–
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										–	–	–	–	–	–
STX	X → M				8E	4	3	86	3	2																															96	4	2	–	–	–	–	–	–
STY	Y → M				8C	4	3	84	3	2													94	4	2																	–	–	–	–	–	–
TAX	A → X													AA	2	1																									✓	✓	–	–	–	–
TAY	A → Y													A8	2	1																									✓	✓	–	–	–	–
TSX	S → X													BA	2	1																									✓	✓	–	–	–	–
TXA	X → A													8A	2	1																									✓	✓	–	–	–	–
TXS	X → S													9A	2	1																									–	–	–	–	–	–
TYA	Y → A													98	2	1																									✓	✓	–	–	–	–

(1) ADD 1 TO "N" IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BELOW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER

+ ADD
– SUBTRACT
∧ AND
∨ OR
⊻ EXCLUSIVE OR
✓ MODIFIED
– NOT MODIFIED
M7 MEMORY BIT 7
M6 MEMORY BIT 6
N NO CYCLES
NO BYTES

Note: MOS Technology cannot assume liability for the use of undefined OP Codes

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

Static D.C. Characteristics (V_{CC} = 5V ±5%, T_A = 0° −70° C)

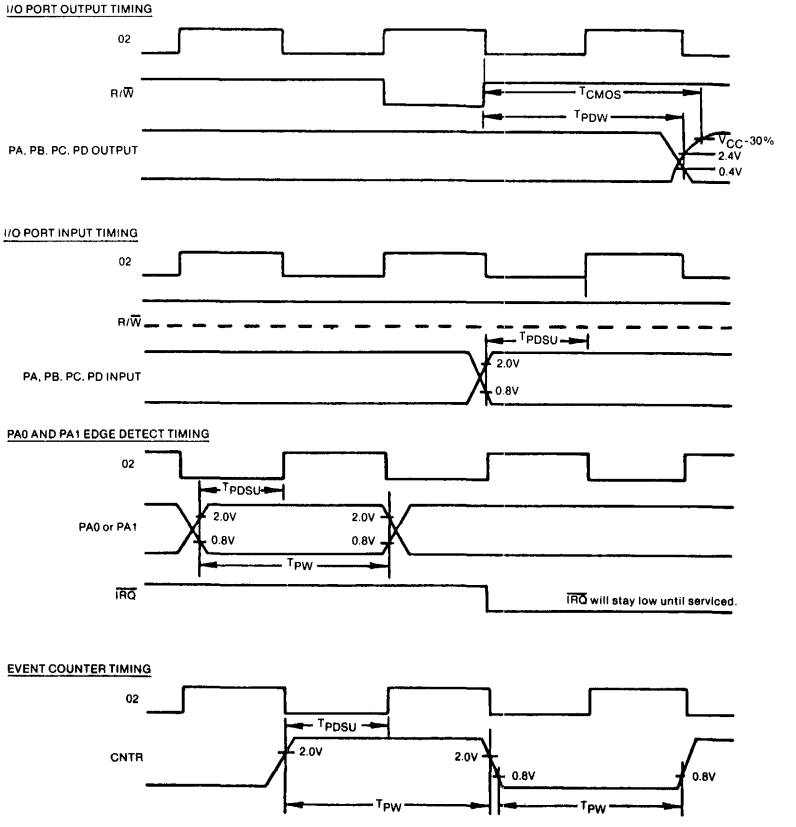
Characteristic	Symbol	Min	Typ	Max	Unit
Power Dissipation (Outputs High)	P_D	—	500	—	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.5	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode)	I_{RR}	—	10	—	mAdc
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	—	+0.8	Vdc
Input Leakage Current					
V_{in} = 0 to 5.0 Vdc	I_{IN}	—	±1.0	±2.5	μAdc
RES, NMI		—	±1.0	—	μAdc
Input High Voltage (XTLI)	V_{IHXT}	+4.0	—	V_{CC}	Vdc
Input Low Voltage (XTLI)	V_{ILXT}	−0.3	—	+0.8	Vdc
Input Low Current					
(V_{IL} = 0.4 Vdc)	I_{IL}	—	−1.0	−1.6	mAdc
Output High Voltage					
(V_{CC} = min, I_{Load} = −100 μAdc)	V_{OH}	−2.4	—	—	Vdc
Output High Voltage	V_{CMOS}	V_{CC} −30%	—	—	Vdc
(V_{CC} = min)					
Output Low Voltage					
(V_{CC} = min, I_{Load} = 1.6 mAdc)	V_{OL}	—	—	+0.4	Vdc
Output High Current (Sourcing)					
(V_{OH} = 2.4 Vdc)	I_{OH}	−100	—	—	μAdc
Output Low Current (Sinking)					
(V_{OL} = 0.4 Vdc)	I_{OL}	1.6	—	—	mAdc
Input Capacitance					
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz) PA, PB, PC, PD, CNTR	C_{in}	—	—	10	pF
XTLI, XTLO		—	—	50	pF
Output Capacitance					
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	—	—	10	pF
I/O Port Resistance	R_L	3.0	6.0	11.5	KΩ
PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, CNTR					

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

AC Characteristics (V_{CC} = 5V ± 5%, T_A = 0° to 70°C)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{cyc}	0.500	5.0	0.250	5.0	μsec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0	—	0.5	—	μsec
Internal Write to Peripheral Data Valid (CMOS)	T_{CMOS}	2.0	—	1.0	—	μsec
Peripheral Data Setup Time	T_{PDSU}	400	—	200	—	nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0	—	0.5	—	μsec

TIMING CHARACTERISTICS



PROGRAMMING INSTRUCTIONS FOR MOS TECHNOLOGY 6500/1

MOS Technology utilizes computer aided techniques to manufacture and test custom bit patterns. New custom bit data and address information is supplied on standard 80 column computer cards, 1 inch wide paper tape, or standard 1/4 inch wide audio tape cassette, or 2708/2716 EPROMS. ROM Data will also be accepted in other formats. Consult MOS Technology for details.

MOS TECHNOLOGY (6500) CARD FORMAT

All addresses and related bit patterns must be completely defined. Each deck of cards consists of: 1) Four Title Cards, 2) Address and Memory Data Records.

Positive logic is generally used on all input cards: A logic "1" is the most positive or high level (True), and logic "0" is the most negative or low level (False). This includes chip select specifications as well as bit patterns.

TITLE CARDS

	COLUMN	INFORMATION
FIRST CARD	1-4	MOS PART NUMBER (6500/1)
	5-80	BLANK (FOR MOS TECHNOLOGY USE)
SECOND CARD	1-20	CUSTOMER NAME
	21-40	CUSTOMER PART NUMBER
	41-60	CUSTOMER TECHNICAL CONTACT (PERSON)
	61-80	CUSTOMER PHONE NUMBER
THIRD CARD	1-20	DATA FORMAT (PUNCH "MOS")
	21-40	LOGIC FORMAT (PUNCH "POSITIVE" OR "NEGATIVE)
	41-60	VERIFICATION CODE (PUNCH "HOLD" IF CUSTOMER APPROVAL REQ., PUNCH "OKAY" IF FINAL APPROVAL NOT REQ.)
	61-80	BLANK (FOR MOS TECHNOLOGY USE)
FOURTH CARD	1-6	PULLUP SELECT CARD (PUNCH "PULLUP")
	7	PULLUP OPTION FOR I/O PORT A;1 = PULLUP
	8	PULLUP OPTION FOR I/O PORT B;1 = PULLUP
	9	PULLUP OPTION FOR I/O PORT C;1 = PULLUP
	10	PULLUP OPTION FOR I/O PORT D;1 = PULLUP

A set of four (4) Title Cards should accompany each data deck. These cards provide our computer programs additional information necessary to accurately produce the ROM Data. These four Title Cards must contain the above information.

MOS CARD DECK FORMAT

Output data is punched on standard 80 column cards in ASCII Hollerith Code. Each byte of data to be stored is converted to two half bytes. The half bytes (whose possible values are 0 to F_{HEX}) are translated into their ASCII equivalents and punched onto cards. Each record contains record length, memory address, and checksum information in addition to data. A column by column description of a data record follows.

COLUMN ONE —**Record Mark.** Signals start of record. ASCII character " ; " (HEX 3B)

COL. 2→3 —**Record Length.** Two ASCII characters representing a HEX number in the range 0 to 18_{HEX} (0 to 24). This is the count of actual data bytes in the record. A record length of 0 indicates end of file.

COL. 4→7 —**Load Address.** Four ASCII characters. The starting address high and starting address low are the left and right bytes respectively. The first data byte is stored in the memory location pointed to by the load address, succeeding data bytes are loaded into ascending address.

COL. 8→n —**Data.** Each 8 bit memory word is represented by two ASCII characters (0 to 9, A to F) to represent a hexadecimal number (0 to 255).

$$\left\{n = 8 + 2*\left(\frac{\text{RECORD}}{\text{LENGTH}}\right) - 1\right\}$$

COL. n+1→n+5 —**Checksum.** The sum of all 8 bit bytes in the record since the record mark (;) in four ASCII characters (HEX).

REMAINING COLUMNS —Not Used. Leave blank or use for comment or labels.

SPECIAL LAST CARD —As mentioned above, a record length of zero ("0") indicates an end of file. Following the record length on this terminal record should be a four character ASCII (HEX) count of all data records in deck. Following this is the usual checksum for this record.

See the example under heading "MOS PAPER TAPE FORMAT."
A set of four title cards should accompany each data deck.

MOS PAPER TAPE FORMAT

The paper tape which should be used is 1" wide paper tape using 7 or 8 bit ASCII code. Each byte of data to be stored is converted to two half bytes. The half bytes (whose possible values are 0 to F_{HEX}) are translated into their ASCII equivalents and written onto paper tape in this form.

Each record output begins with a semicolon (";") character (ASCII 3B) to mark the start of a valid record. The next byte transmitted (Range: 1 to 18_{HEX}) is the number of data bytes contained in the record. The record's starting address high (1 byte, 2 characters), starting address low (1 byte, 2 characters), and data (usually 24 bytes, 48 characters) follow. Each record is terminated by the record's check-sum (2 bytes, 4 characters), a carriage return (ASCII 0D), Line Feed (ASCII 0A), and six "NULL" characters (ASCII 0). No other characters, such as rubouts, are allowed anywhere.

The last record transmitted has zero data bytes (indicated by ;00). The starting address field is replaced by a four digit HEX number representing the total number of data records contained in the transmission, followed by the records usual check-sum digits. An "XOFF" character ends the transmission.

EXAMPLE:

;180000FFEEDDCCBBAA00998877665544332211223344556677889 90AFC;0000010001

All records must be punched in consecutive order and the data at each address must be completely and explicitly defined. All invalid data will be ignored and zeros substituted. Additional information as described in section entitled "TITLE CARDS" should be provided at transmission.

6500 MICROPROCESSORS

THE 6500 MICROPROCESSOR FAMILY CONCEPT —

The 6500 Series Microprocessors represent the first totally software compatible microprocessor family. This family of products includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. All of the microprocessors in the 6500 group are software compatible within the group and are bus compatible with the M6800 product offering.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for the multi processor system applications where maximum timing control is mandatory. All versions of the microprocessors are available in 1 MHz, 2 MHz ("A" suffix on product numbers), and 3 MHz ("B" suffix on product numbers) maximum operating frequencies.

FEATURES OF THE 6500 FAMILY

- Single +5 volt supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type or speed memory
- 8 BIT Bi-directional Data Bus
- Addressable memory range of up to 65K bytes
- "Ready" input (for single cycle execution)
- Direct memory access capability
- Bus compatible with M6800
- Choice of external or on-board clocks
- 1 MHz, 2 MHz, and 3 MHz operation
- On-the-chip clock options
  - * External single clock input
  - * RC time base input
  - * Crystal time base input
- Pipeline architecture

MEMBERS OF THE 6500 MICROPROCESSOR (CPU) FAMILY

Microprocessors with On-Chip Clock Oscillator

Model	Addressable Memory
R6502	65K Bytes
R6503	4K Bytes
R6504	8K Bytes
R6505	4K Bytes
R6506	4K Bytes
R6507	8K Bytes

Microprocessors with External Two Phase Clock Inputs

Model	Addressable Memory
R6512	65K Bytes
R6513	4K Bytes
R6514	8K Bytes
R6515	4K Bytes

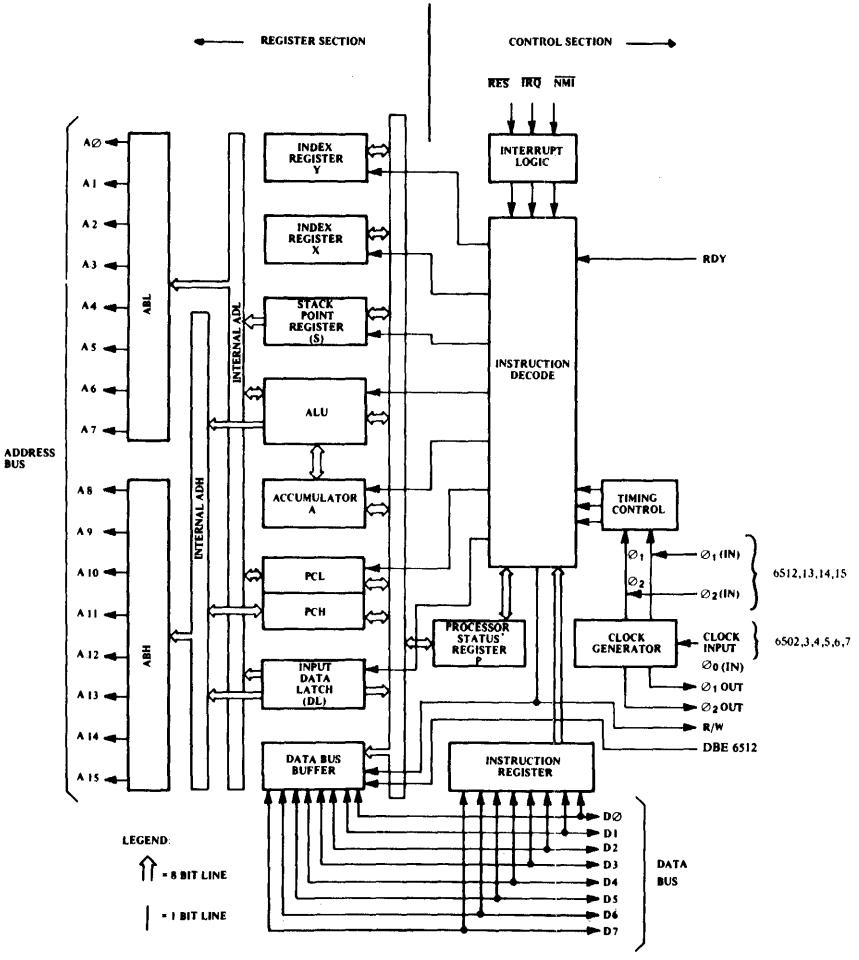
ORDER NUMBER: MXS 65XX —

- FREQUENCY RANGE
  - NO SUFFIX = 1 MHz
  - A = 2 MHz
  - B = 3 MHz
- MODEL DESIGNATOR
  - XX = 02, 03, 04, . . . 15
- PACKAGE DESIGNATOR
  - C = CERAMIC
  - P = PLASTIC

COMMENTS ON THE DATA SHEET

The data sheet is constructed to review first the basic "Common Characteristics"—those features which are common to the general family of microprocessors. Subsequent to a review of the family characteristics will be sections devoted to each member of the group with specific features of each.

COMMON CHARACTERISTICS



Note: 1. Clock Generator is not included on 6512,13,14,15

2. Addressing Capability and control options vary with each of the 6500 Products.

6500 Internal Architecture

COMMON CHARACTERISTICS

MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	Vcc	−0.3 to +7.0	Vdc
INPUT VOLTAGE	Vin	−0.3 to +7.0	Vdc
OPERATING TEMPERATURE	T_A	0 to +70	°C
STORAGE TEMPERATURE	T_{STG}	−55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, Vss = 0, T_A = 0° to + 70°C)

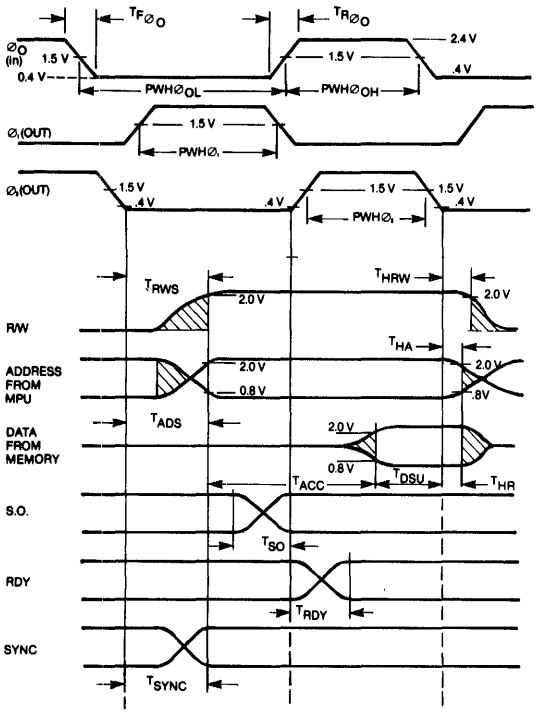
$\varnothing_1$, $\varnothing_2$ (In) applies to 6512, 13, 14, 15; $\varnothing_0$(In) applies to 6502, 03, 04, 05, 06 and 07

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage					
Logic, $\varnothing_0$ (In)	VIH	Vss + 2.4	—	Vcc	Vdc
$\varnothing_1$, $\varnothing_2$(In)		Vcc − 0.2	—	Vcc + 1.0V	Vdc
Input High Voltage					
RES, NMI, RDY, IRQ, Data, S.O.		Vss + 2.0	—	—	Vdc
Input Low Voltage					
Logic, $\varnothing_0$ (In)	VIL	Vss − 0.3	—	Vss + 0.4	Vdc
$\varnothing_1$, $\varnothing_2$(In)		Vss − 0.3	—	Vss + 0.2	Vdc
RES, NMI, RDY, IRQ, Data, S.O.		—	—	Vss + 0.8	Vdc
Input Leakage Current (V_{In} = 0 to 5.25V, Vcc = 5.25V)					
Logic (Excl. RDY,S.O.)	Iin	—	—	2.5	μA
$\varnothing_1$, $\varnothing_2$(In)		—	—	100	μA
$\varnothing_0$(In)		—	—	10.0	μA
Three State (Off State) Input Current (V_{In} = 0.4 to 2.4V, Vcc = 5.25V)					
Data Lines	ITSI	—	—	10	μA
Output High Voltage (I_{OH} = −100μAdc, Vcc = 4.75V)					
SYNC, Data, AO-A15, R/W	VOH	Vss + 2.4	—	—	Vdc
Out Low Voltage (I_{OL} = 1.6mAdc, Vcc = 4.75V)					
SYNC, Data, AO-A15, R/W	VOL	—	—	Vss + 0.4	Vdc
Power Supply Current	I_{CC}	—	70	160	mA
Capacitance (V_{In} = 0, T_A = 25°C, f = 1MHz)	C				pF
Logic	C_{in}	—	—	10	
Data		—	—	15	
AO-A15,R/W, SYNC	C_{out}	—	—	12	
$\varnothing_0$(In)	$C_{\varnothing_0(in)}$	—	—	15	
$\varnothing_1$	$C_{\varnothing_1}$	—	30	50	
$\varnothing_2$	$C_{\varnothing_2}$	—	50	80	

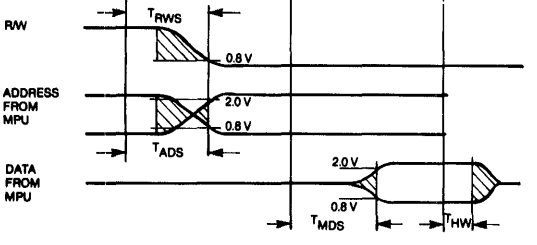
Note: IRQ and NMI require 3K pull-up resistors.

COMMON CHARACTERISTICS

Clock Timing— 6502, 03, 04, 05, 06, 07

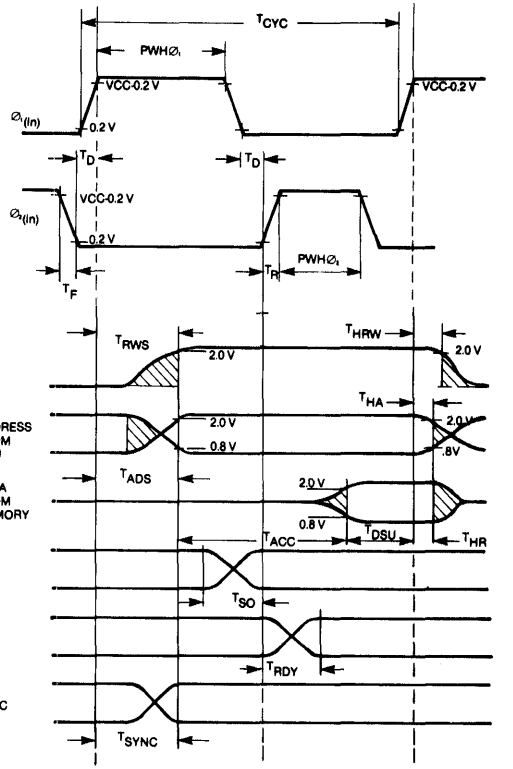


Timing for Reading Data from Memory or Peripherals

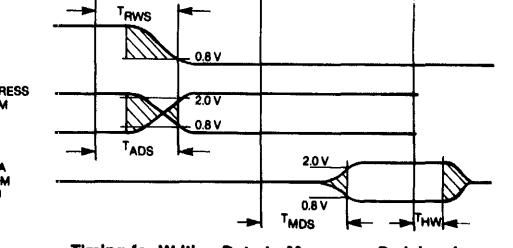


Timing for Writing Data to Memory or Peripherals

Clock Timing— 6512, 13, 14, 15



Timing for Reading Data from Memory or Peripherals



Timing for Writing Data to Memory or Peripherals

COMMON CHARACTERISTICS

1 MH_Z TIMING | **2 MH_Z TIMING** | **3 MH_Z TIMING**

Electrical Characteristics: (Vcc = 5V ± 5%, Vss = 0 V, T_A = 0°-70°C)
Minimum clock frequency = 50 KH_Z

CLOCK TIMING—6502, 03, 04, 05, 06, 07

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN	TYP.	MAX.	UNITS
Cycle Time	T_{CYC}	1000	—	—	500	—	—	333	—	—	ns
$\varnothing_{0(IN)}$ Pulse Width (measured at 1.5v)	$PWH\varnothing_0$	480	—	520	240	—	260	180	—	170	ns
$\varnothing_{0\ (IN)}$ Rise, Fall Time	$TR\varnothing_0 TF\varnothing_0$	—	—	10	—	—	10	—	—	10	ns
Delay Time between Clocks (measured at 1.5v)	T_D	5	—	—	5	—	—	5	—	—	ns
$\varnothing_{1(OUT)}$ Pulse Width (measured at 1.5v)	$PWH\varnothing_1$	$PWH\varnothing_{OL}$ – 20	—	$PWH\varnothing_{OL}$	$PWH\varnothing_{OL}$ – 20	—	$PWH\varnothing_{OL}$	$PWH\varnothing_{OL}$ – 20	—	$PWH\varnothing_{OL}$	ns
$\varnothing_{2(OUT)}$ Pulse Width (measured at 1.5v)	$PWH\varnothing_2$	$PWH\varnothing_{OH}$ – 40	—	$PWH\varnothing_{OH}$ – 10	$PWH\varnothing_{OH}$ – 40	—	$PWH\varnothing_{OH}$ – 10	$PWH\varnothing_{OH}$ – 40	—	$PWH\varnothing_{OH}$ – 10	ns
$\varnothing_{1(OUT)}$, $\varnothing_{2(OUT)}$ Rise, Fall Time (measured .8v to 2.0v) (Load ½ 30pf ½ 1 TTL)	T_R, T_F	—	—	25	—	—	25	—	—	25	ns

CLOCK TIMING—6512, 13, 14, 15

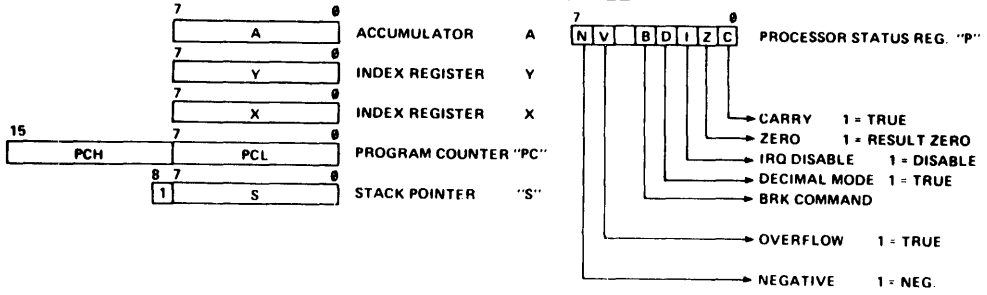
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Cycle Time	T_{CYC}	1000	—	—	500	—	—	333	—	—	ns
Clock Pulse Width Ø1	PWH Ø1	430			215			150			ns
(Measured at V_{CC} – 0.2v) Ø2	PWH Ø2	470	—	—	235	—	—	160	—	—	
Fall Time, Rise Time (Measured from 0.2v to V_{CC} – 0.2v)	T_F,T_R	—	—	25	—	—	15	—	—	15	ns
Delay Time between Clocks (Measured at 0.2v)	T_D	0	—	—	0	—	—	0	—	—	ns

READ/WRITE TIMING (LOAD = 1TTL)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Read/Write Setup Time from 6500	T_{RWS}	—	100	300	—	100	150	—	80	110	ns
Address Setup Time from 6500	T_{ADS}	—	100	300	—	100	150	—	80	125	ns
Memory Read Access Time	T_{ACC}	—	—	575	—	—	300	—	—	170	ns
Data Stability Time Period	T_{DSU}	100	—	—	50	—	—	50	—	—	ns
Data Hold Time—Read	T_{HR}	10	—	—	10	—	—	10	—	—	ns
Data Hold Time—Write	T_{HW}	30	60	—	30	60	—	10	—	—	ns
Data Setup Time from 6500	T_{MDS}	—	150	200	—	75	100	—	70	100	ns
S.O. Setup Time	$T_{S.O.}$	100	—	—	50	—	—	50	—	—	ns
SYNC Setup Time from 6500	T_{SYNC}	—	—	350	—	—	175	—	—	120	ns
Address Hold Time	T_{HA}	30	60	—	30	60	—	10	30	—	ns
R/W Hold Time	T_{HRW}	30	60	—	30	60	—	10	30	—	ns
RDY Setup Time	T_{RDY}	100	—	—	50	—	—	—	—	15	ns

COMMON CHARACTERISTICS

PROGRAMMING MODEL



INSTRUCTION SET – OP CODES, Execution Time, Memory Requirements

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND,X)			(IND),Y			Z PAGE,X			ABS,X			ABS,Y			RELATIVE			INDIRECT			Z PAGE,Y			CONDITION CODES					
MNEMONIC	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										✓	✓	✓	-	-	✓
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										✓	✓	-	-	-	-
ASL	C ← 7 0 ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													✓	✓	✓	-	-	-
BCC	BRANCH ON C=0 (2)																															90	2	2							-	-	-	-	-	-
BCS	BRANCH ON C=1 (2)																															B0	2	2							-	-	-	-	-	-
BEQ	BRANCH ON Z=1 (2)																															F0	2	2							-	-	-	-	-	-
BIT	A ∧ M				2C	4	3	24	3	2																															M_7	✓	-	-	-	M_6
BMI	BRANCH ON N=1 (2)																															30	2	2							-	-	-	-	-	-
BNE	BRANCH ON Z=0 (2)																															D0	2	2							-	-	-	-	-	-
BPL	BRANCH ON N=0 (2)																															10	2	2							-	-	-	-	-	-
BRK	(See Fig 1)													00	7	1																									-	-	-	✓	-	-
BVC	BRANCH ON V=0 (2)																															50	2	2							-	-	-	-	-	-
BVS	BRANCH ON V=1 (2)																															70	2	2							-	-	-	-	-	-
CLC	0 → C													18	2	1																									-	-	0	-	-	-
CLD	0 → D													D8	2	1																									-	-	-	-	0	-
CLI	0 → I													58	2	1																									-	-	-	0	-	-
CLV	0 → V													B8	2	1																									-	-	-	-	-	0
CMP	A-M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										✓	✓	✓	-	-	-
CPX	X-M	E0	2	2	EC	4	3	E4	3	2																															✓	✓	✓	-	-	-
CPY	Y-M	C0	2	2	CC	4	3	C4	3	2																															✓	✓	✓	-	-	-
DEC	M-1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													✓	✓	-	-	-	-
DEX	X-1 → X													CA	2	1																									✓	✓	-	-	-	-
DEY	Y-1 → Y													88	2	1																									✓	✓	-	-	-	-
EOR	A ⊻ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										✓	✓	-	-	-	-
INC	M+1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													✓	✓	-	-	-	-
INX	X+1 → X													E8	2	1																									✓	✓	-	-	-	-
INY	Y+1 → Y													C8	2	1																									✓	✓	-	-	-	-
JMP	JUMP TO NEW LOC				4C	3	3																													6C	5	3				-	-	-	-	-	-
JSR	(See Fig 2) JUMP SUB				20	6	3																																			-	-	-	-	-	-
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										✓	✓	-	-	-	-

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND,X)			(IND),Y			Z PAGE,X			ABS,X			ABS,Y			RELATIVE			INDIRECT			Z PAGE,Y			CONDITION CODES					
MNEMONIC	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3										96	4	2	✓	✓	-	-	-	-
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3															✓	✓	-	-	-	-
LSR	0 → 7 0 → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0	✓	✓	-	-	-
NOP	NO OPERATION													EA	2	1																									-	-	-	-	-	-
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										✓	✓	-	-	-	-
PHA	A → Ms S-1 → S													48	3	1																									-	-	-	-	-	-
PHP	P → Ms S-1 → S													08	3	1																									-	-	-	-	-	-
PLA	S+1 → S Ms → A													68	4	1																									✓	✓	-	-	-	-
PLP	S+1 → S Ms → P													28	4	1																									(RESTORED)					
ROL	7 0 C				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													✓	✓	✓	-	-	-
ROR	C 7 0				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													✓	✓	✓	-	-	-
RTI	(See Fig 1) RTRN INT													40	6	1																									(RESTORED)					
RTS	(See Fig 2) RTRN SUB													60	6	1																									-	-	-	-	-	-
SBC	A-M-C → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										✓	✓	(3)	-	-	✓
SEC	1 → C													38	2	1																									-	-	1	-	-	-
SED	1 → D													F8	2	1																									-	-	-	-	1	-
SEI	1 → I													78	2	1																									-	-	-	1	-	-
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										-	-	-	-	-	-
STX	X → M				8E	4	3	86	3	2																															96	4	2	-	-	-	-	-	-
STY	Y → M				8C	4	3	84	3	2													94	4	2																	-	-	-	-	-	-
TAX	A → X													AA	2	1																									✓	✓	-	-	-	-
TAY	A → Y													A8	2	1																									✓	✓	-	-	-	-
TSX	S → X													BA	2	1																									✓	✓	-	-	-	-
TXA	X → A													8A	2	1																									✓	✓	-	-	-	-
TXS	X → S													9A	2	1																									-	-	-	-	-	-
TYA	Y → A													98	2	1																									✓	✓	-	-	-	-

(1) ADD 1 TO "N" IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BELOW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER

+ ADD
- SUBTRACT
∧ AND
∨ OR
⊻ EXCLUSIVE OR
✓ MODIFIED
- NOT MODIFIED
M MEMORY BIT 7
M_6 MEMORY BIT 6
N NO CYCLES
NO BYTES

Note: MOS Technology cannot assume liability for the use of undefined OP Codes

COMMON CHARACTERISTICS

6500 SIGNAL DESCRIPTION

Clocks ($\varnothing_1$, $\varnothing_2$)
The 651X requires a two phase non-overlapping clock that runs at the Vcc voltage level.
The 650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

Address Bus (A_0-A_{15})
These outputs are TTL compatible, capable of driving one standard TTL load and 130 pf.

Data Bus (D_0-D_7)
Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130pf.

Data Bus Enable (DBE)
This TTL compatible input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two ($\varnothing_2$) clock, thus allowing data output from microprocessor only during $\varnothing_2$. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

Ready (RDY)
This input signal allows the user to single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one ($\varnothing_1$) and up to 100ns after phase two ($\varnothing_2$) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two ($\varnothing_2$) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If Ready is low during a write cycle, it is ignored until the following read operation.

Interrupt Request ($\overline{IRQ}$)
This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)
A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. $\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the interrupt mask flag status. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.
$\overline{NMI}$ also requires an external 3KΩ resister to Vcc for proper wire-OR operations.
Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupt lines that are sampled during $\varnothing_2$ (phase 2) and will begin the appropriate interrupt routine on the $\varnothing_1$ (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)
A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of $\varnothing_1$.

SYNC
This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $\varnothing_1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\varnothing_1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset
This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.
After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.
After Vcc reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (SYNC) signal will become valid.
When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

COMMON CHARACTERISTICS

ADDRESSING MODES

ACCUMULATOR ADDRESSING—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING—In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING—The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

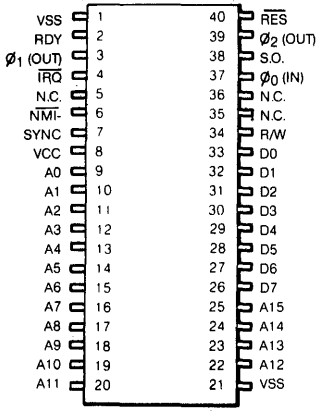
INDEXED INDIRECT ADDRESSING—In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING—In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET—ALPHABETIC SEQUENCE

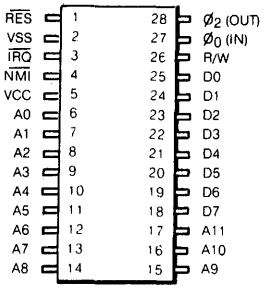
ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Register
TYA	Transfer Index Y to Accumulator



6502—40 Pin Package

Features of 6502

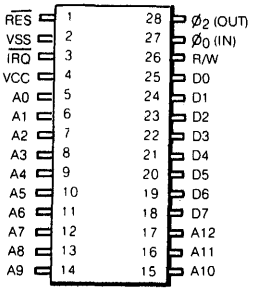
- 65K Addressable Bytes of Memory (A0-A15)
- IRQ Interrupt
- On-the-chip Clock
  - TTL Level Single Phase Input
  - RC Time Base Input
  - Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used to halt or single cycle execution)
- Two Phase Output Clock for Timing of Support Chips
- NMI Interrupt



6503—28 Pin Package

Features of 6503

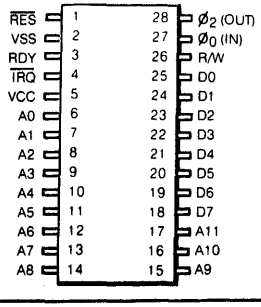
- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- IRQ Interrupt
- NMI Interrupt
- 8 Bit Bidirectional Data Bus



6504—28 Pin Package

Features of 6504

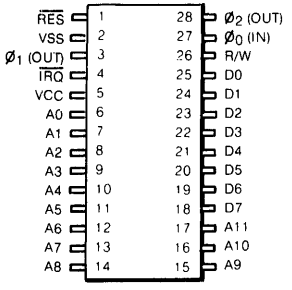
- 8K Addressable Bytes of Memory (A0-A12)
- On-the-chip Clock
- IRQ Interrupt
- 8 Bit Bidirectional Data Bus



6505—28 Pin Package

Features of 6505

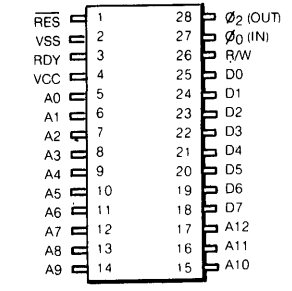
- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- IRQ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus



6506—28 Pin Package

Features of 6506

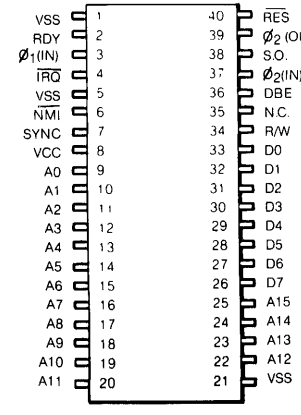
- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- Two phase output clock for timing of support chips
- 8 Bit Bidirectional Data Bus



6507—28 Pin Package

Features of 6507

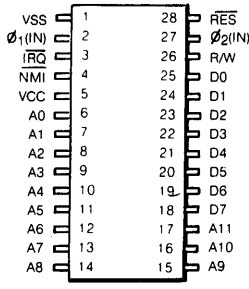
- 8K Addressable Bytes of Memory (A0-A12)
- On-the-chip Clock
- RDY Signal
- 8 Bit Bidirectional Data Bus



6512—40 Pin Package

Features of 6512

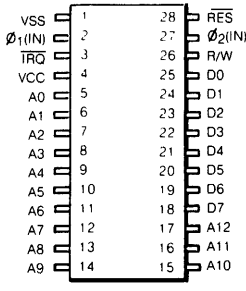
- 65K Addressable Bytes of Memory (A0-A15)
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus
- SYNC Signal
- Two phase clock input
- Data Bus Enable



6513—28 Pin Package

Features of 6513

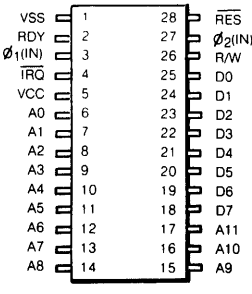
- 4K Addressable Bytes of Memory (A0-A11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- 8 Bit Bidirectional Data Bus



6514—28 Pin Package

Features of 6514

- 8K Addressable Bytes of Memory (A0-A12)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- 8 Bit Bidirectional Data Bus



6515—28 Pin Package

Features of 6515

- 4K Addressable Bytes of Memory (A0-A11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus

commodore semiconductor group

NMOS

MPS

6508

MICROPROCESSOR WITH RAM AND I/O

6508 MICROPROCESSOR WITH RAM AND I/O

MICRO PROCESSORS

DESCRIPTION

The 6508 is a low-cost microcomputer system capable of solving a broad range of small-systems and peripheral-control problems at minimum cost to the user.

One full page (256 bytes) of RAM is located (on chip) concurrently at Page 0 and Page 1, allowing Zero Page Addressing and stack operations with no additional RAM.

An 8-bit Bi-Directional I/O Port is located on-chip with the Output Register at Address 0001 and the Data-Direction Register at Address 0000. The I/O Port is bit-by-bit programmable.

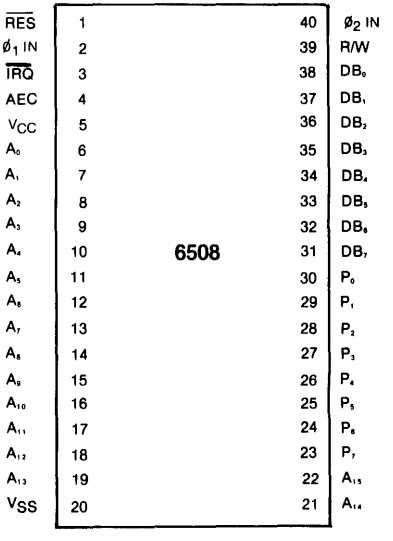
The Three-State sixteen-bit Address Bus allows Direct Memory Accessing (DMA) and multi-processor systems sharing a common memory.

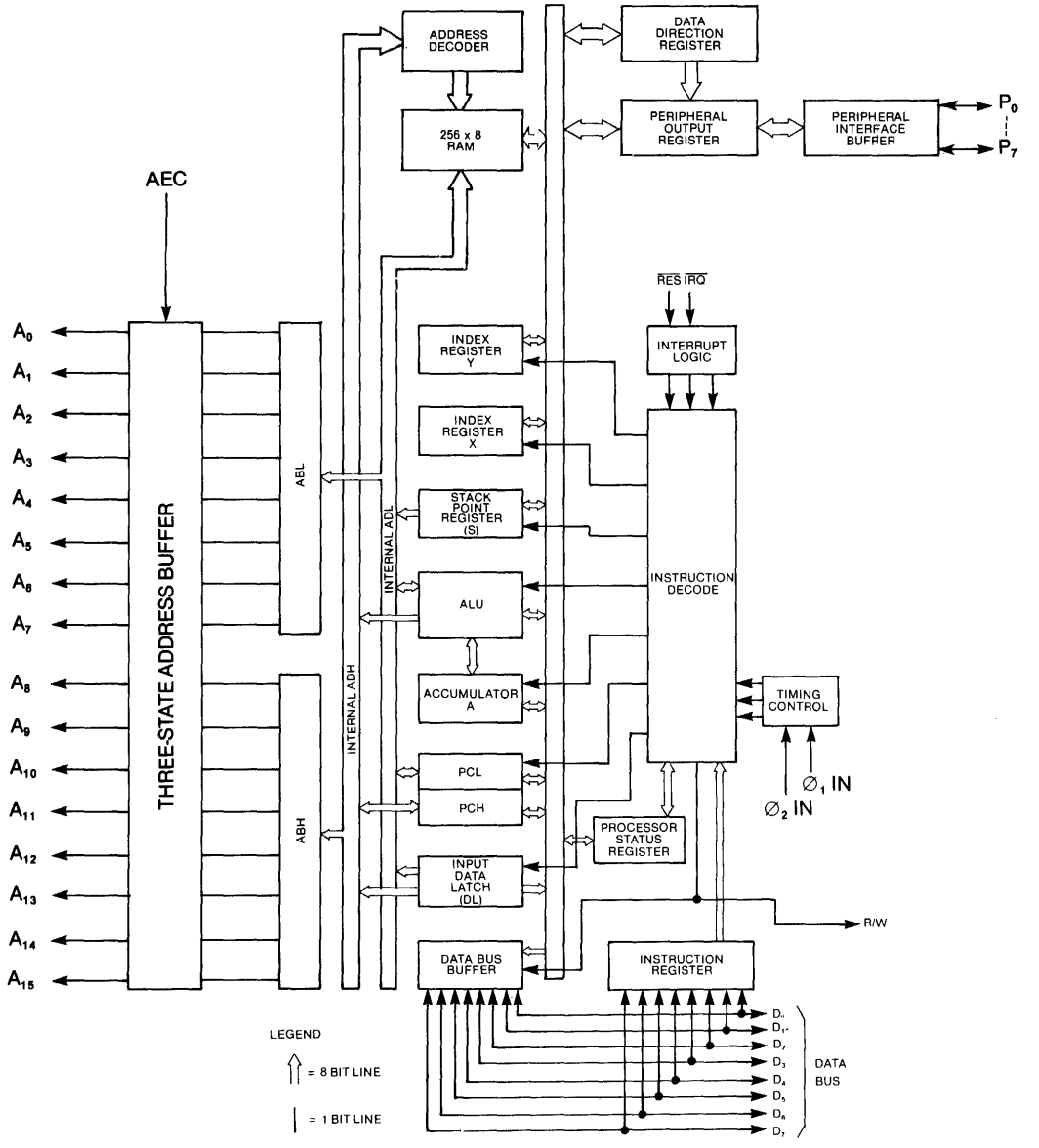
The internal processor architecture is identical to the MOS Technology 6502 to provide software compatibility.

FEATURES OF THE 6508 . . .

- 8-Bit Bi-Directional I/O Port
- 256 Bytes fully Static RAM (internal)
- Single +5 volt supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- 8 Bit Bi-Directional Data Bus
- Addressable memory range of up to 65K bytes
- Direct memory access capability
- Bus compatible with M6800
- Pipeline architecture
- 1 MHz, 2MHz (Suffix "A"), and 3MHz (Suffix "B")
- Use with any type or speed memory

6508 PIN CONFIGURATION





6508 BLOCK DIAGRAM

6508 CHARACTERISTICS

MAXIMUM RATINGS

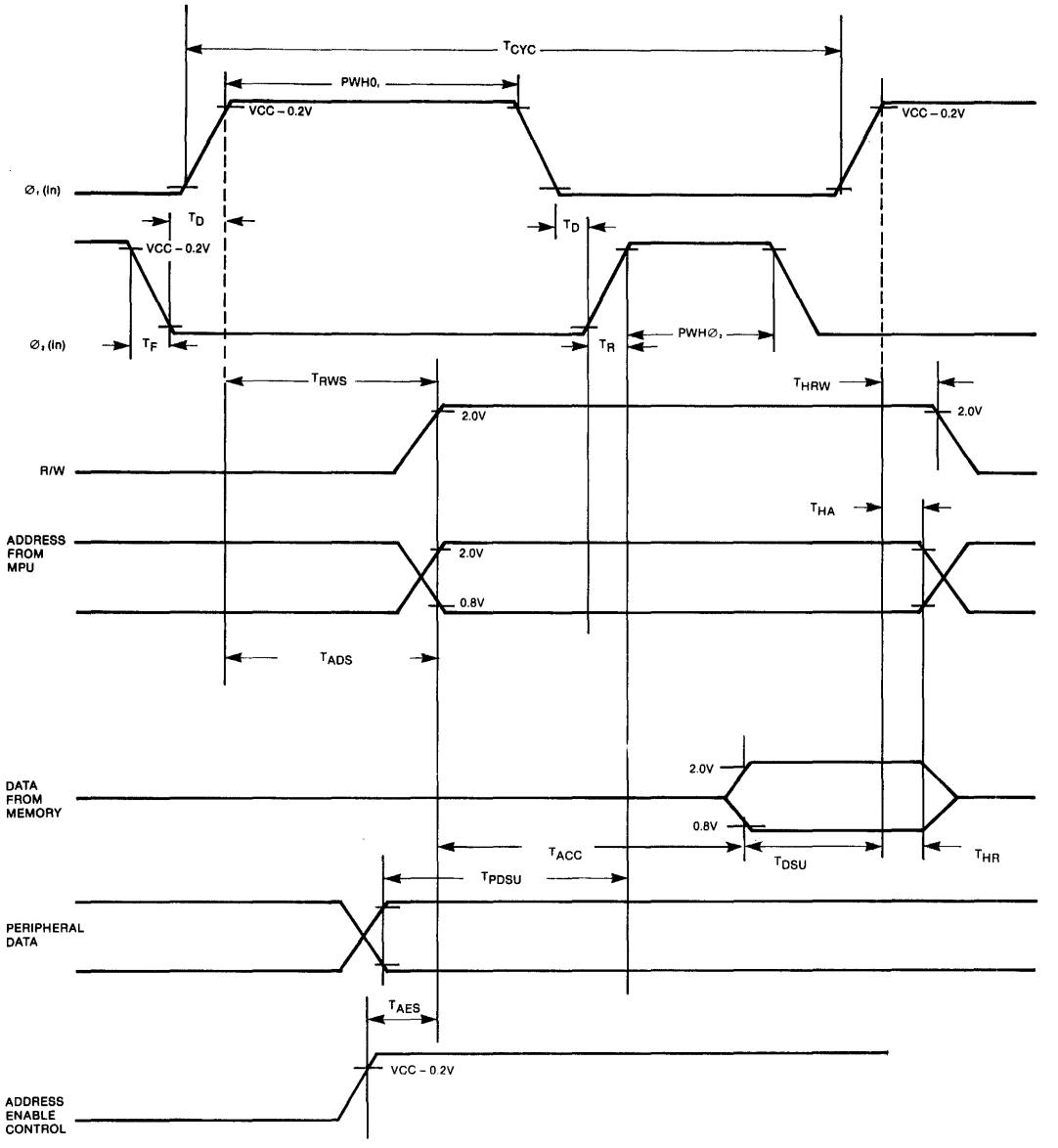
RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	Vcc	−0.3 to +7.0	Vdc
INPUT VOLTAGE	Vin	−0.3 to +7.0	Vdc
OPERATING TEMPERATURE	T_A	0 to +70	°C
STORAGE TEMPERATURE	T_{STG}	−55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum ratiag.

ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, Vss = 0, T_A = 0° to + 70°C)

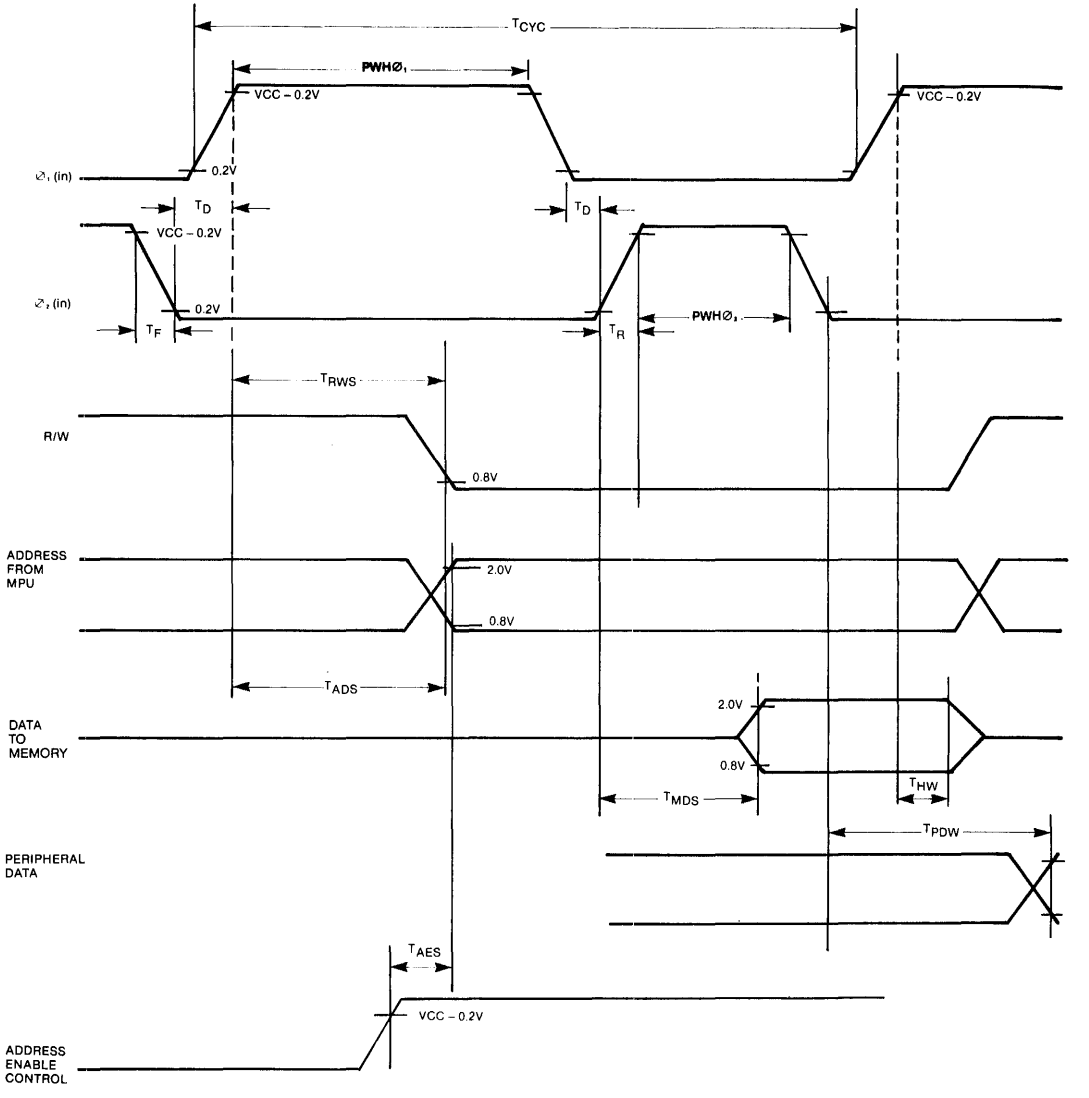
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage					
$\varnothing_1$, $\varnothing_2$(in)	VIH	Vcc - 0.2	—	Vcc + 1.0V	Vdc
Input High Voltage					
$\overline{RES}$, P_0-P,$\overline{IRQ}$, Data		Vss + 2.0	—	—	Vdc
Input Low Voltage					
$\varnothing_1$, $\varnothing_2$(in)	VIL	Vss - 0.3	—	Vss + 0.2	Vdc
$\overline{RES}$, P_0-P, $\overline{IRQ}$, Data		—	—	Vss + 0.8	Vdc
Input Leakage Current (V_{In} = 0 to 5.25V, Vcc = 5.25V)					
Logic	Iin	—	—	2.5	μA
$\varnothing_1$, $\varnothing_2$(in)		—	—	100	μA
Three State (Off State) Input Current (V_{In} = 0.4 to 2.4V, Vcc = 5.25V)					
Data Lines	ITSI	—	—	10	μA
Output High Voltage (I_{OH} = -100μAdc, Vcc = 4.75V)					
Data, A0-A15, R/W, P_0-P,	VOH	Vss + 2.4	—	—	Vdc
Out Low Voltage (I_{OL} = 1.6mAdc, Vcc = 4.75V)					
Data, A0-A15, R/W, P_0-P,	VOL	—	—	Vss + 0.4	Vdc
Power Supply Current	ICC	—	125		mA
Capacitance	C				pF
V_{In} = O, T_A = 25°C, f = 1MHz)					
Logic, P_0-P,	C_{in}	—	—	10	
Data		—	—	15	
A0-A15, R/W	C_{out}	—	—	12	
$\varnothing_1$	$C_{\varnothing_1}$	—	30	50	
$\varnothing_2$	$C_{\varnothing_2}$	—	50	80	

CLOCK TIMING



TIMING FOR READING DATA FROM MEMORY OR PERIPHERALS

CLOCK TIMING



TIMING FOR WRITING DATA TO MEMORY OR PERIPHERALS

AC CHARACTERISTICS

1 MHz TIMING **2 MHz TIMING** **3 MHz TIMING**

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{SS} = 0V, T_A = 0°–70°C)
Minimum Clock Frequency = 50 KHz

CLOCK TIMING

CHARACTERISTIC	SYMBOL	1 MHz MIN.	1 MHz TYP.	1 MHz MAX.	2 MHz MIN.	2 MHz TYP.	2 MHz MAX.	3 MHz MIN.	3 MHz TYP.	3 MHz MAX.	UNITS
Cycle Time	T_{CYC}	1000	—	—	500	—	—	333	—	—	ns
Clock Pulse Width Ø1	PWHØ1	430	—	—	215	—	—	150			ns
(Measured at VCC — 0.2V) Ø2	PWHØ2	470	—	—	235	—	—	160	—	—	
Fall Time, Rise Time (Measured from 0.2V to VCC — 0.2V)	T_F, T_R	—	—	25	—	—	15	—	—	15	ns
Delay Time between Clocks (Measured at 0.2V)	T_D	0	—	—	0	—	—	0	—	—	ns

READ/WRITE TIMING (LOAD=1TTL)

CHARACTERISTIC	SYMBOL	1 MHz MIN.	1 MHz TYP.	1 MHz MAX.	2 MHz MIN.	2 MHz TYP.	2 MHz MAX.	3 MHz MIN.	3 MHz TYP.	3 MHz MAX.	UNITS
Read/Write Setup Time from 6508	T_{RWS}	—	100	300	—	100	150	—	80	110	ns
Address Setup Time from 6508	T_{ADS}	—	100	300	—	100	150	—	80	125	ns
Memory Read Access Time	T_{ACC}	—	—	575	—	—	300	—	—	170	ns
Data Stability Time Period	T_{DSU}	100	—	—	50	—	—	50	—	—	ns
Data Hold Time-Read	T_{HR}	10	—	—	10	—	—	10	—	—	ns
Data Hold Time-Write	T_{HW}	10	30	—	10	30	—	10	—	—	ns
Data Setup Time from 6508	T_{MDS}	—	150	200	—	75	100	—	70	100	ns
Address Hold Time	T_{HA}	10	30	—	10	30	—	10	30	—	ns
R/W Hold Time	T_{HRW}	10	30	—	10	30	—	10	30	—	ns
Delay Time, Ø2 negative transition to Peripheral Data valid	T_{PDW}	—	—	1	—	—	0.5	—	—	0.333	—
Peripheral Data Setup Time	T_{PDSU}	300	—	—	150	—	—	75	—	—	ns
Address Enable Setup Time	T_{AES}	—	—	60	—	—	60	—	—	60	ns

SIGNAL DESCRIPTION

Clocks ($\varnothing_1$, $\varnothing_2$)
The 6510 requires a two phase non-overlapping clock that runs at the Vcc voltage level.

Address Bus (A_0-A_{15})
The three state outputs are TTL compatible, capable of driving one standard TTL load and 130 pf.

Data Bus (D_0-D_7)
Eight pins are used for the data bus. This is a Bi-Directional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pf.

Reset
This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After Vcc reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

Interrupt Request ($\overline{IRQ}$)
This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses.

Address Enable Control (AEC)
The Address Bus is valid only when the Address Enable Control line is high. When low, the Address Bus is in a high-impedance state. This feature allows easy DMA and multiprocessor systems.

I/O Port (P_0-P_7)
Eight pins are used for the peripheral port, which can transfer data to or from peripheral devices. The Output Register is located in RAM at Address 0001, and the Data Direction Register is at Address 0000. The outputs are capable at driving one standard TTL load and 130 pf.

Read/Write (R/W)
This signal is generated by the microprocessor to control the direction of data transfers on the Data Bus. This line is high except when the microprocessor is writing to memory or a peripheral device.

ADDRESSING MODES

ACCUMULATOR ADDRESSING—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING—In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING—The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING—In indexed indirect addressing (referred to as [Indirect, X]), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

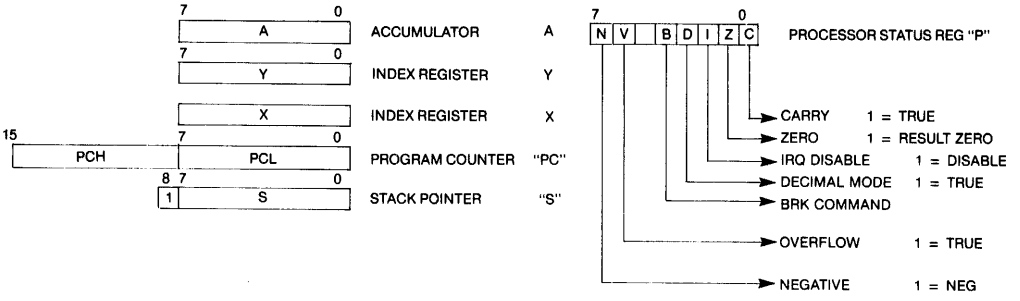
INDIRECT INDEXED ADDRESSING—In indirect indexed addressing (referred to as [Indirect, Y]). the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET—ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Register
TYA	Transfer Index Y to Accumulator

PROGRAMMING MODEL



INSTRUCTION SET – OP CODES, Execution Time, Memory Requirements

INSTRUCTIONS			IMMEDIATE			ABSOLUTE			ZEROPAGE			ACCUM			IMPLIED			(IND,X)			(IND),Y			ZPAGE,X			ABS,X			ABS,Y			RELATIVE			INDIRECT			ZPAGE,Y			CONDITION CODES					
MNEMONIC	OPERATION		OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
ADC	A+M+C→A	(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										✓	✓	✓	-	-	✓
AND	A∧M→A	(1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										✓	✓	-	-	-	-
ASL	C ← 7 0 ← 0					0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													✓	✓	✓	-	-	-
BCC	BRANCH ON C=0	(2)																															90	2	2							-	-	-	-	-	-
BCS	BRANCH ON C=1	(2)																															B0	2	2							-	-	-	-	-	-
BEQ	BRANCH ON Z=1	(2)																															F0	2	2							-	-	-	-	-	-
BIT	A ∧ M					2C	4	3	24	3	2																														M7	✓	-	-	-	M6
BMI	BRANCH ON N=1	(2)																															30	2	2							-	-	-	-	-	-
BNE	BRANCH ON Z=0	(2)																															D0	2	2							-	-	-	-	-	-
BPL	BRANCH ON N=0	(2)																															10	2	2							-	-	-	-	-	-
BRK	(See Fig 1)														00	7	1																								-	-	-	-	-	-
BVC	BRANCH ON V=0	(2)																															50	2	2							-	-	-	-	-	-
BVS	BRANCH ON V=1	(2)																															70	2	2							-	-	-	-	-	-
CLC	0→C														18	2	1																								-	-	0	-	-	-
CLD	0→D														D8	2	1																								-	-	-	-	0	-
CLI	0→I														58	2	1																								-	-	-	0	-	-
CLV	0→V														B8	2	1																								-	-	-	-	-	0
CMP	A - M	(1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										✓	✓	✓	-	-	-
CPX	X - M		E0	2	2	EC	4	3	E4	3	2																														✓	✓	✓	-	-	-
CPY	Y - M		C0	2	2	CC	4	3	C4	3	2																														✓	✓	✓	-	-	-
DEC	M - 1→M					CE	6	3	C6	5	2													D6	6	2	DE	7	3													✓	✓	-	-	-	-
DEX	X - 1→X														CA	2	1																								✓	✓	-	-	-	-
DEY	Y - 1→Y														88	2	1																								✓	✓	-	-	-	-
EOR	A⊻M→A	(1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										✓	✓	-	-	-	-
INC	M + 1→M					EE	6	3	E6	5	2													F6	6	2	FE	7	3													✓	✓	-	-	-	-
INX	X + 1→X														E8	2	1																								✓	✓	-	-	-	-
INY	Y + 1→Y														C8	2	1																								✓	✓	-	-	-	-
JMP	JUMP TO NEW LOC					4C	3	3																													6C	5	3				-	-	-	-
JSR	(See Fig 2) JUMP SUB					20	6	3																																		-	-	-	-	-	-
LDA	M→A	(1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										✓	✓	-	-	-	-
LDX	M→X	(1)	A2	2	2	AE	4	3	A6	3	2																														✓	✓	-	-	-	-
LDY	M→Y	(1)	A0	2	2	AC	4	3	A4	3	2																			B4	4	3										✓	✓	-	-	-	-
LSR	0→ 7 0 →C					4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													✓	✓	✓	-	-	-
NOP	NO OPERATION														EA	2	1																								-	-	-	-	-	-
ORA	A∨M→A		09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										✓	✓	-	-	-	-
PHA	A→M_S S-1→S														48	3	1																								-	-	-	-	-	-
PHP	P→M_S S-1→S														08	3	1																								-	-	-	-	-	-
PLA	S+1→S M_S→A														68	4	1																								✓	✓	-	-	-	-
PLP	S+1→S M_S→P														28	4	1																								(RESTORED)					
ROL	C ← 7 0 ← C					2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													✓	✓	✓	-	-	-
ROR	C → 7 0 → C					6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													✓	✓	✓	-	-	-
RTI	(See Fig 1) RTRN INT														40	6	1																								(RESTORED)					
RTS	(See Fig 2) RTRN SUB														60	6	1																								-	-	-	-	-	-
SBC	A-M-C→A	(1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										✓	✓	✓ (3)	-	-	✓
SEC	1→C														38	2	1																								-	-	1	-	-	-
SED	1→D														F8	2	1																								-	-	-	-	1	-
SEI	1→I														78	2	1																								-	-	-	1	-	-
STA	A→M					8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										-	-	-	-	-	-
STX	X→M					8E	4	3	86	3	2																														96	4	2	-	-	-	-	-	-
STY	Y→M					8C	4	3	84	3	2													94	4	2																	-	-	-	-	-	-
TAX	A→X														AA	2	1																								✓	✓	-	-	-	-
TAY	A→Y														A8	2	1																								✓	✓	-	-	-	-
TSX	S→X														BA	2	1																								✓	✓	-	-	-	-
TXA	X→A														8A	2	1																								✓	✓	-	-	-	-
TXS	X→S														9A	2	1																								-	-	-	-	-	-
TYA	Y→A														98	2	1																								✓	✓	-	-	-	-

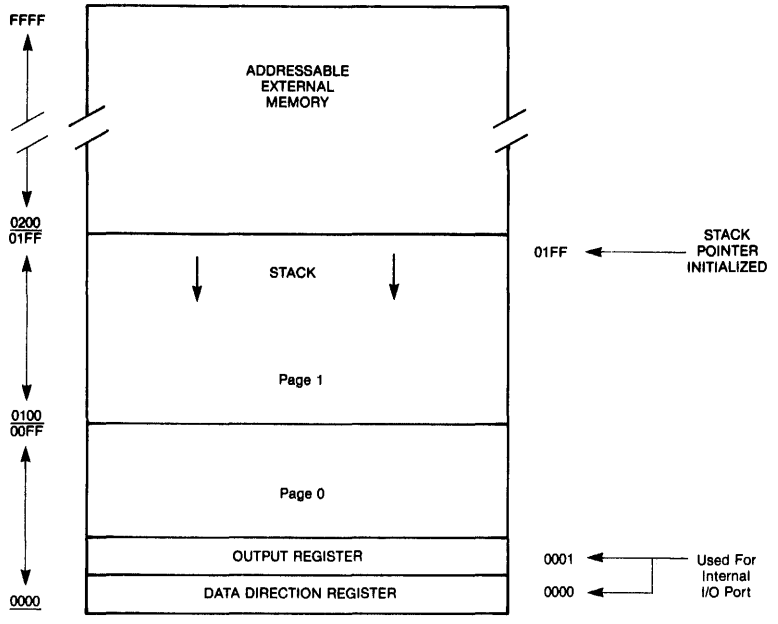
(1) ADD 1 TO N IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT BORROW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
M_S MEMORY PER STACK POINTER

+ ADD
- SUBTRACT
∧ AND
∨ OR
⊻ EXCLUSIVE OR
✓ MODIFIED
NOT MODIFIED
M_7 MEMORY BIT 7
M_6 MEMORY BIT 6

N NO CYCLES
NO BYTES

Note: Commodore Semiconductor Group cannot assume liability for the use of undefined OP Codes



6508 MEMORY MAP

APPLICATIONS NOTES

Locating the Output Register at the internal I/O Port in Page Zero enhances the powerful Zero Page Addressing instructions of the 6510.

By assigning the I/O Pins as inputs (using the Data Direction Register) the user has the ability to change the contents of address 0001 (the Output Register) using peripheral devices. The ability to change these contents using peripheral inputs, together with Zero Page Indirect Addressing instructions, allows novel and versatile programming techniques not possible earlier.

commodore semiconductor group

NMOS

MPS

6509

MICROPROCESSOR WITH MEMORY MANAGEMENT

6509 MICROPROCESSOR WITH MEMORY MANAGEMENT

DESCRIPTION

The 6509 is a low-cost microprocessor capable of solving a broad range of small systems and memory management problems at minimum cost to the user.

A memory management system allows for up to One Mega-Byte of memory for ease in down loading languages, operating systems or other data.

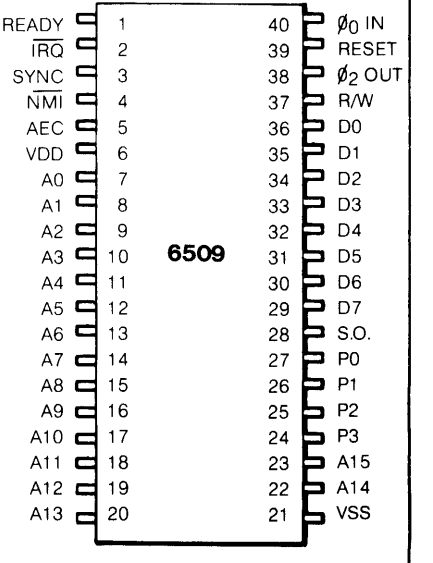
The Three-State sixteen-bit Address Bus allows Direct Memory Accessing (DMA) and multi-processor systems sharing a common memory while the Four-bit Extended Address Register allows for up to one Mega-byte of data storage.

The internal processor architecture is identical to the MOS Technology 6502 to provide software compatibility.

FEATURES OF THE 6509

- Memory management
- On board clock logic
- Addressable memory range of up to 1M bytes
- Single +5 volt supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- 8 Bit Bi-Directional Data Bus
- Program Addressable memory range of up to 65K bytes
- Direct memory access capability
- Bus compatible with M6800
- Pipeline architecture
- 1 MHz, 2 MHz and 3 MHz operation
- Use with any type or speed memory

PIN CONFIGURATION



commodore semiconductor group

NMOS

MPS
6510
MICROPROCESSOR
WITH I/O

6510 MICROPROCESSOR WITH I/O

DESCRIPTION

The 6510 is a low-cost microcomputer system capable of solving a broad range of small-systems and peripheral-control problems at minimum cost to the user.

An 8-bit Bi-Directional I/O Port is located on-chip with the Output Register at Address 0 0 0 0 and the Data-Direction Register at Address 0 0 0 1. The I/O Port is bit-by-bit programmable.

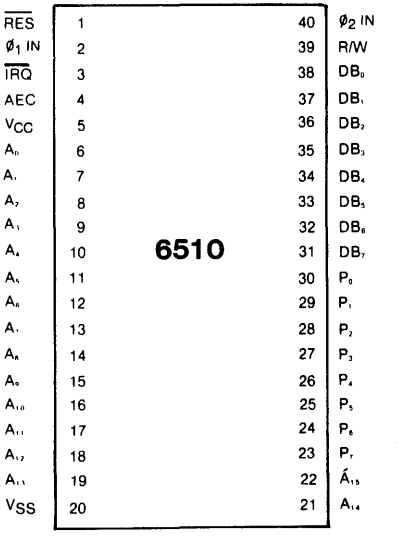
The Three-State sixteen-bit Address Bus allows Direct Memory Accessing (DMA) and multi-processor systems sharing a common memory.

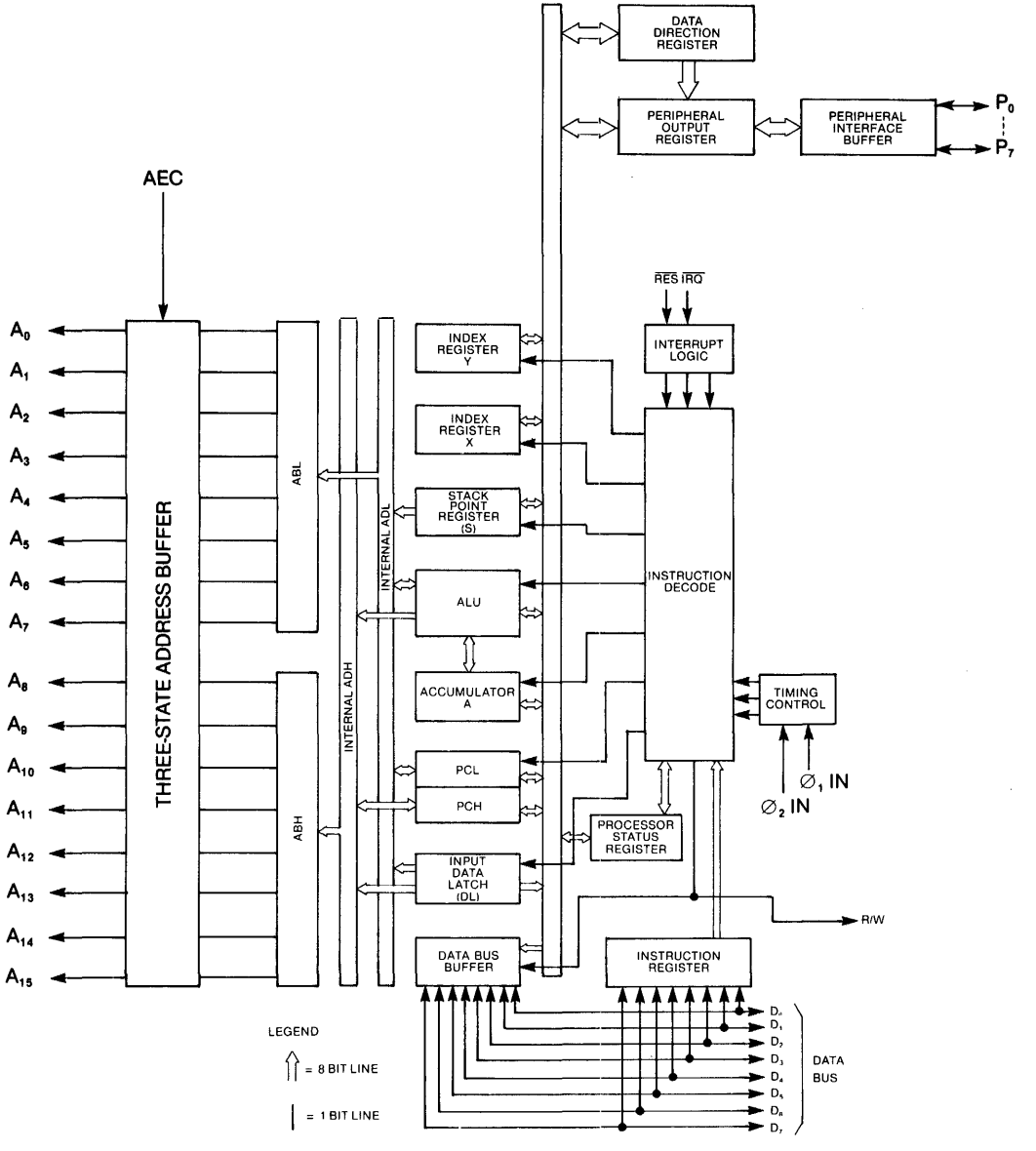
The internal processor architecture is identical to the MOS Technology 6502 to provide software compatibility.

FEATURES OF THE 6510...

- 8-Bit Bi-Directional I/O Port
- Single +5 volt supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- 8 Bit Bi-Directional Data Bus
- Addressable memory range of up to 65K bytes
- Direct memory access capability
- Bus compatible with M6800
- Pipeline architecture
- 1 MHz and 2MHz operation
- Use with any type or speed memory

PIN CONFIGURATION





6510 BLOCK DIAGRAM

6510 CHARACTERISTICS

MAXIMUM RATINGS

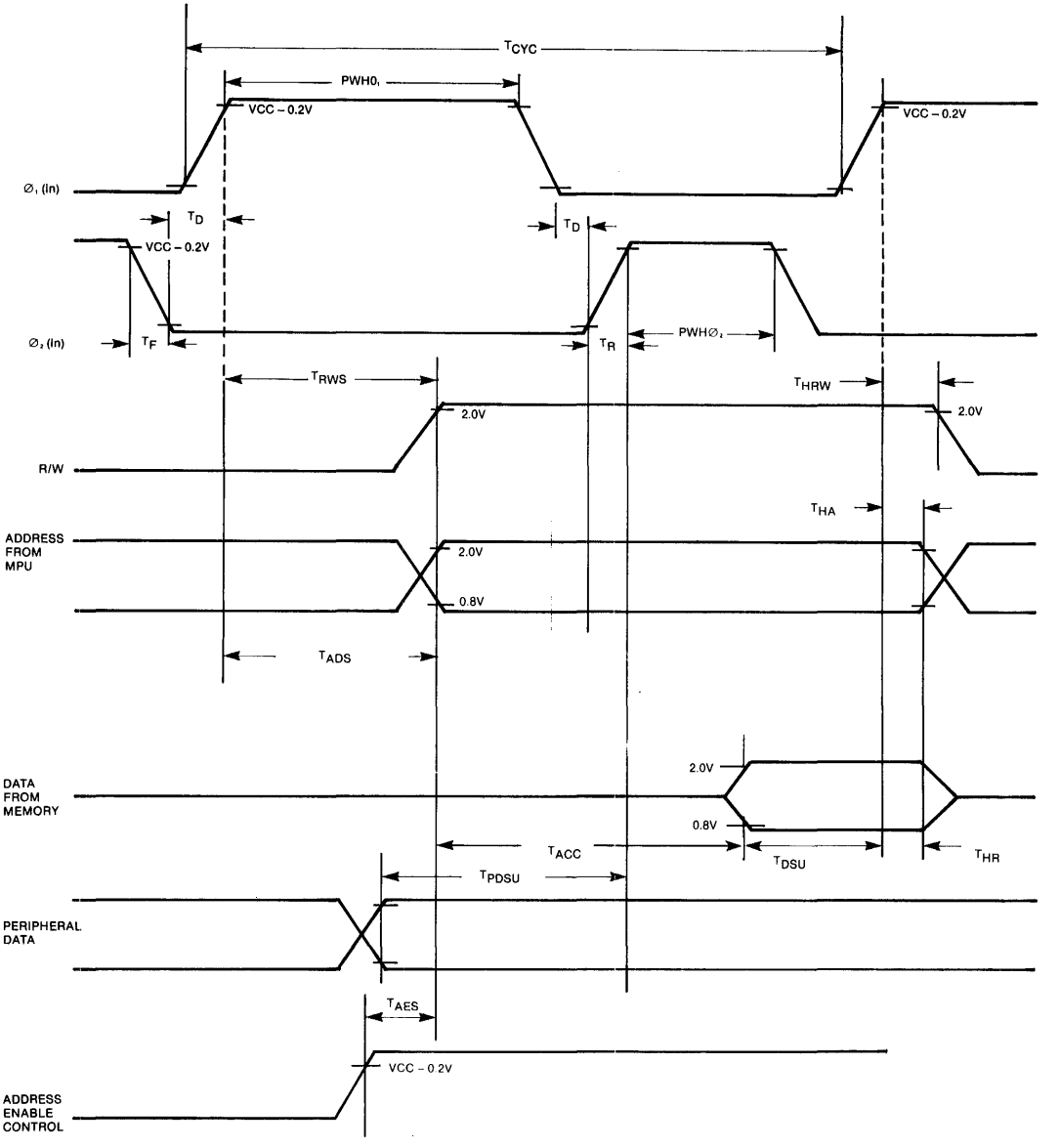
RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	Vcc	−0.3 to +7.0	Vdc
INPUT VOLTAGE	Vin	−0.3 to +7.0	Vdc
OPERATING TEMPERATURE	T_A	0 to +70	°C
STORAGE TEMPERATURE	T_{STG}	−55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, Vss = 0, T_A = 0° to + 70°C)

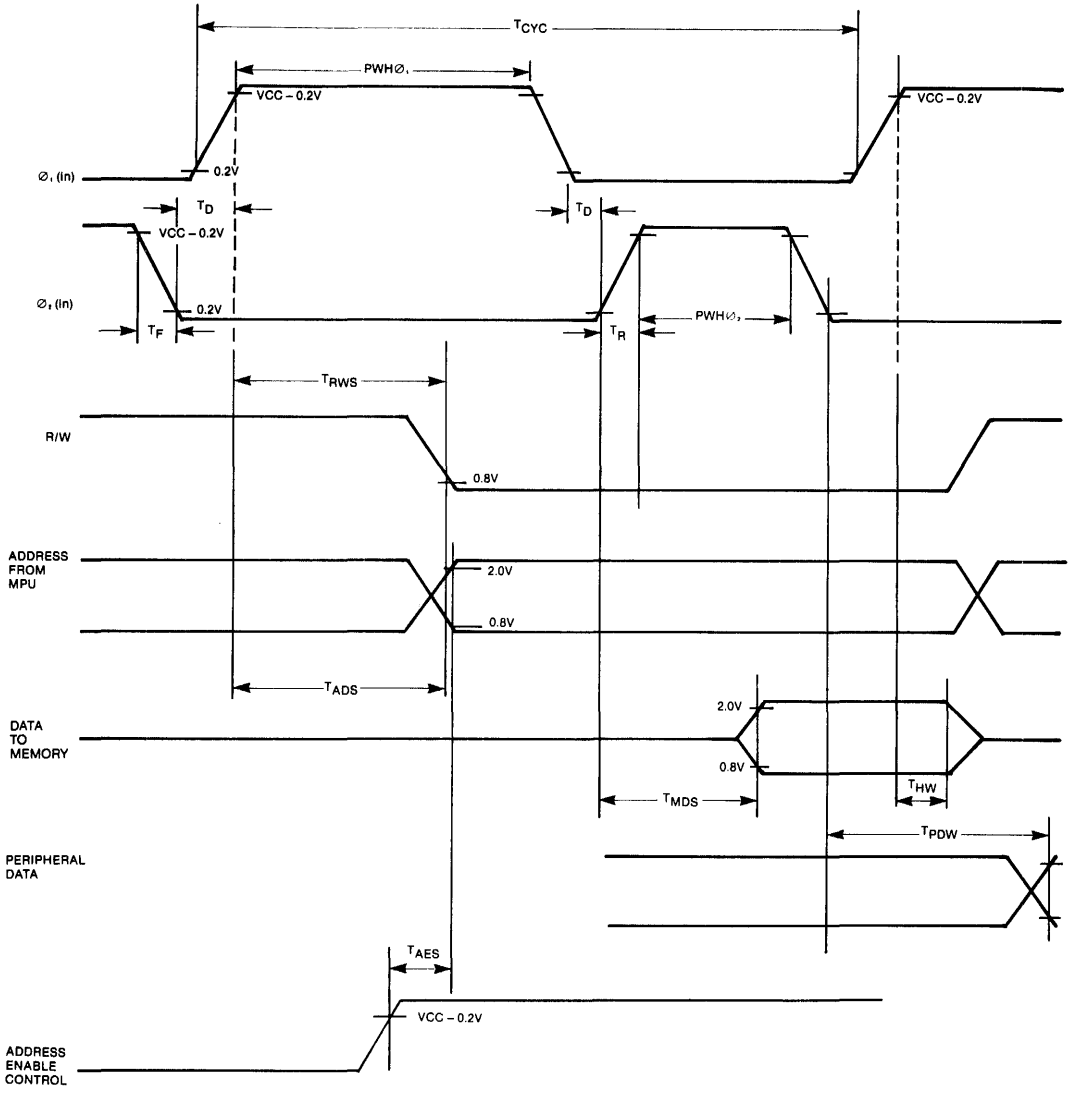
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage					
$\varnothing_1$, $\varnothing_2$(in)	VIH	Vcc - 0.2	—	Vcc + 1.0V	Vdc
Input High Voltage					
$\overline{RES}$, P_0-P, $\overline{IRQ}$, Data		Vss + 2.0	—	—	Vdc
Input Low Voltage					
$\varnothing_1$, $\varnothing_2$(in)	VIL	Vss - 0.3	—	Vss + 0.2	Vdc
$\overline{RES}$, P_0-P, $\overline{IRQ}$, Data		—	—	Vss + 0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.25V, Vcc = 5.25V)					
Logic	Iin	—	—	2.5	μA
$\varnothing_1$, $\varnothing_2$(in)		—	—	100	μA
Three State (Off State) Input Current (V_{in} = 0.4 to 2.4V, Vcc = 5.25V)					
Data Lines	ITSI	—	—	10	μA
Output High Voltage (I_{OH} = −100μAdc, Vcc = 4.75V)					
Data, A0-A15, R/W, P_0-P,	VOH	Vss + 2.4	—	—	Vdc
Out Low Voltage (I_{OL} = 1.6mAdc, Vcc = 4.75V)					
Data, A0-A15, R/W, P_0-P,	VOL	—	—	Vss + 0.4	Vdc
Power Supply Current	ICC	—	125		mA
Capacitance	C				pF
V_{in} = 0, T_A = 25°C, f = 1MHz)					
Logic, P_0-P,	C_{in}	—	—	10	
Data		—	—	15	
A0-A15, R/W	C_{out}	—	—	12	
$\varnothing_1$	$C_{\varnothing_1}$	—	30	50	
$\varnothing_2$	$C_{\varnothing_2}$	—	50	80	

CLOCK TIMING



TIMING FOR READING DATA FROM MEMORY OR PERIPHERALS

CLOCK TIMING



TIMING FOR WRITING DATA TO MEMORY OR PERIPHERALS

AC CHARACTERISTICS

1 MHz TIMING	2 MHz TIMING

ELECTRICAL CHARACTERISTICS (VCC = 5V ± 5%, VSS = 0V, T_A = 0° −70°C)
Minimum Clock Frequency = 50 KHz

CLOCK TIMING

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Cycle Time	T_{CYC}	1000	—	—	500	—	—	ns
Clock Pulse Width ∅1	PWH∅1	430	—	—	215	—	—	ns
(Measured at VCC − 0.2V) ∅2	PWH∅2	470	—	—	235	—	—	ns
Fall Time, Rise Time (Measured from 0.2V to VCC − 0.2V)	T_F, T_R	—	—	25	—	—	15	ns
Delay Time between Clocks (Measured at 0.2V)	T_D	0	—	—	0	—	—	ns

READ/WRITE TIMING (LOAD = 1TTL)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Read/Write Setup Time from 6508	T_{RWS}	—	100	300	—	100	150	ns
Address Setup Time from 6508	T_{ADS}	—	100	300	—	100	150	ns
Memory Read Access Time	T_{ACC}	—	—	575	—	—	300	ns
Data Stability Time Period	T_{DSU}	100	—	—	50			ns
Data Hold Time-Read	T_{HR}		—	—				ns
Data Hold Time-Write	T_{HW}	10	30	—	10	30		ns
Data Setup Time from 6510	T_{MDS}	—	150	200	—	75	100	ns
Address Hold Time	T_{HA}	10	30	—	10	30		ns
R/W Hold Time	T_{HRW}	10	30	—	10	30		ns
Delay Time, Address valid to ∅2 positive transition	T_{AEW}	180	—	—				ns
Delay Time, ∅2 negative transition to Peripheral Data valid	T_{PDW}	—	—	1			0.5	μs
Peripheral Data Setup Time	T_{PDSU}	300	—	—				ns
Address Enable Setup Time	T_{AES}			60			60	ns

SIGNAL DESCRIPTION

Clocks ($\varnothing_1$, $\varnothing_2$)
The 6510 requires a two phase non-overlapping clock that runs at the Vcc voltage level.

Address Bus (A_0-A_{15})
The three state outputs are TTL compatible, capable of driving one standard TTL load and 130 pf.

Data Bus (D_0-D_7)
Eight pins are used for the data bus. This is a Bi-Directional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pf.

Reset
This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After Vcc reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

Interrupt Request ($\overline{IRQ}$)
This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses.

Address Enable Control (AEC)
The Address Bus is valid only when the Address Enable Control line is high. When low, the Address Bus is in a high-impedance state. This feature allows easy DMA and multiprocessor systems.

I/O Port (P_0-P_7)
Eight pins are used for the peripheral port, which can transfer data to or from peripheral devices. The Output Register is located in RAM at Address 0001, and the Data Direction Register is at Address 0000. The outputs are capable at driving one standard TTL load and 130 pf.

Read/Write (R/W)
This signal is generated by the microprocessor to control the direction of data transfers on the Data Bus. This line is high except when the microprocessor is writing to memory or a peripheral device.

ADDRESSING MODES

ACCUMULATOR ADDRESSING—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING—In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING—The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING—In indexed indirect addressing (referred to as [Indirect, X]), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

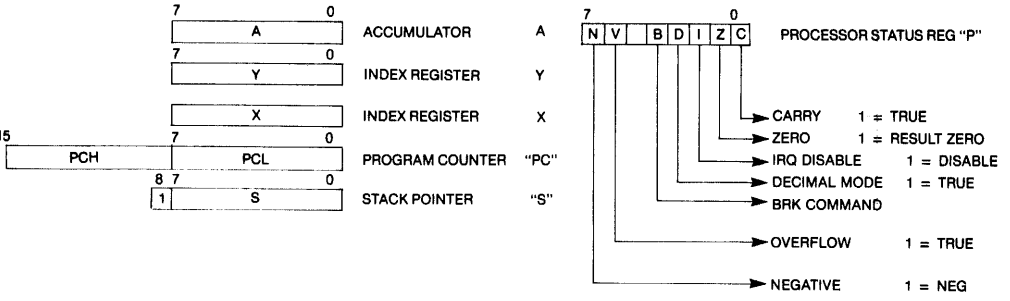
INDIRECT INDEXED ADDRESSING—In indirect indexed addressing (referred to as [Indirect, Y]). the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET—ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Register
TYA	Transfer Index Y to Accumulator

PROGRAMMING MODEL



INSTRUCTION SET – OP CODES, Execution Time, Memory Requirements

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z,PAGE X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z,PAGE Y			CONDITION CODES					
MNEMONIC	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
ADC	A+M+C→A	(1)	69	2	2	6D	4	3	65	3	2						61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3											✓	✓	✓	·	·	✓
AND	A∧M→A	(1)	29	2	2	2D	4	3	25	3	2						21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3											✓	✓	·	·	·	·
ASL	C ← 7 … 0 ← 0					0E	6	3	06	5	2	0A	2	1									16	6	2	1E	7	3													✓	✓	✓	·	·	·
BCC	BRANCH ON C=0	(2)																														90	2	2							·	·	·	·	·	·
BCS	BRANCH ON C=1	(2)																														B0	2	2							·	·	·	·	·	·
BEQ	BRANCH ON Z=1	(2)																														F0	2	2							·	·	·	·	·	·
BIT	A ∧ M					2C	4	3	24	3	2																														M7	✓	·	·	·	M6
BMI	BRANCH ON N=1	(2)																														30	2	2							·	·	·	·	·	·
BNE	BRANCH ON Z=0	(2)																														D0	2	2							·	·	·	·	·	·
BPL	BRANCH ON N=0	(2)																														10	2	2							·	·	·	·	·	·
BRK	(See Fig. 1)													00	7	1																								·	·	·	1	·	·
BVC	BRANCH ON V=0	(2)																														50	2	2							·	·	·	·	·	·
BVS	BRANCH ON V=1	(2)																														70	2	2							·	·	·	·	·	·
CLC	0→C													18	2	1																								·	·	0	·	·	·
CLD	0→D													D8	2	1																								·	·	·	·	0	·
CLI	0→I													58	2	1																								·	·	·	0	·	·
CLV	0→V													B8	2	1																								·	·	·	·	·	0
CMP	A−M	(1)	C9	2	2	CD	4	3	C5	3	2						C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3											✓	✓	✓	·	·	·
CPX	X−M		E0	2	2	EC	4	3	E4	3	2																														✓	✓	✓	·	·	·
CPY	Y−M		C0	2	2	CC	4	3	C4	3	2																														✓	✓	✓	·	·	·
DEC	M−1→M					CE	6	3	C6	5	2												D6	6	2	DE	7	3													✓	✓	·	·	·	·
DEX	X−1→X													CA	2	1																								·	✓	·	·	·	·
DEY	Y−1→Y													88	2	1																								·	✓	·	·	·	·
EOR	A⊻M→A	(1)	49	2	2	4D	4	3	45	3	2						41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3											✓	✓	·	·	·	·
INC	M+1→M					EE	6	3	E6	5	2												F6	6	2	FE	7	3													✓	✓	·	·	·	·
INX	X+1→X													E8	2	1																								·	✓	·	·	·	·
INY	Y+1→Y													C8	2	1																								·	✓	·	·	·	·
JMP	JUMP TO NEW LOC					4C	3	3																													6C	5	3				·	·	·	·	·	·
JSR	(See Fig. 2) JUMP SUB					20	6	3																																	·	·	·	·	·	·
LDA	M→A	(1)	A9	2	2	AD	4	3	A5	3	2						A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3											✓	✓	·	·	·	·
LDX	M→X	(1)	A2	2	2	AE	4	3	A6	3	2																		BE	4	3							B6	4	7	✓	✓	·	·	·	·
LDY	M→Y	(1)	A0	2	2	AC	4	3	A4	3	2												B4	4	2	BC	4	3													✓	✓	·	·	·	·
LSR	0→ 7 … 0 →C					4E	6	3	46	5	2	4A	2	1									56	6	2	5E	7	3													0	✓	✓	·	·	·
NOP	NO OPERATION													EA	2	1																								·	·	·	·	·	·
ORA	A∨M→A		09	2	2	0D	4	3	05	3	2						01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3											✓	✓	·	·	·	·
PHA	A→M$_S$ S−1→S													48	3	1																								·	·	·	·	·	·
PHP	P→M$_S$ S−1→S													08	3	1																								·	·	·	·	·	·
PLA	S+1→S M$_S$→A													68	4	1																								✓	✓	·	·	·	·
PLP	S+1→S M$_S$→P													28	4	1																								(RESTORED)					
ROL	C ← 7 … 0 ← C					2E	6	3	26	5	2	2A	2	1									36	6	2	3E	7	3													✓	✓	✓	·	·	·
ROR	C → 7 … 0 → C					6E	6	3	66	5	2	6A	2	1									76	6	2	7E	7	3													✓	✓	✓	·	·	·
RTI	(See Fig 1) RTRN INT													40	6	1																								(RESTORED)					
RTS	(See Fig 2) RTRN SUB													60	6	1																								·	·	·	·	·	·
SBC	A−M−C→A	(1)	E9	2	2	ED	4	3	E5	3	2						E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3											✓	✓	(3)	·	·	✓
SEC	1→C													38	2	1																								·	·	1	·	·	·
SED	1→D													F8	2	1																								·	·	·	·	1	·
SEI	1→I													78	2	1																								·	·	·	1	·	·
STA	A→M					8D	4	3	85	3	2						81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3											·	·	·	·	·	·
STX	X→M					8E	4	3	86	3	2																												96	4	2	·	·	·	·	·	·
STY	Y→M					8C	4	3	84	3	2												94	4	2																·	·	·	·	·	·
TAX	A→X													AA	2	1																								·	✓	·	·	·	·
TAY	A→Y													A8	2	1																								·	✓	·	·	·	·
TSX	S→X													BA	2	1																								·	✓	·	·	·	·
TXA	X→A													8A	2	1																								·	✓	·	·	·	·
TXS	X→S													9A	2	1																								·	·	·	·	·	·
TYA	Y→A													98	2	1																								·	✓	·	·	·	·

(1) ADD 1 TO N IF PAGE BOUNDARY IS CROSSED

(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE

(3) CARRY NOT = BORROW

(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

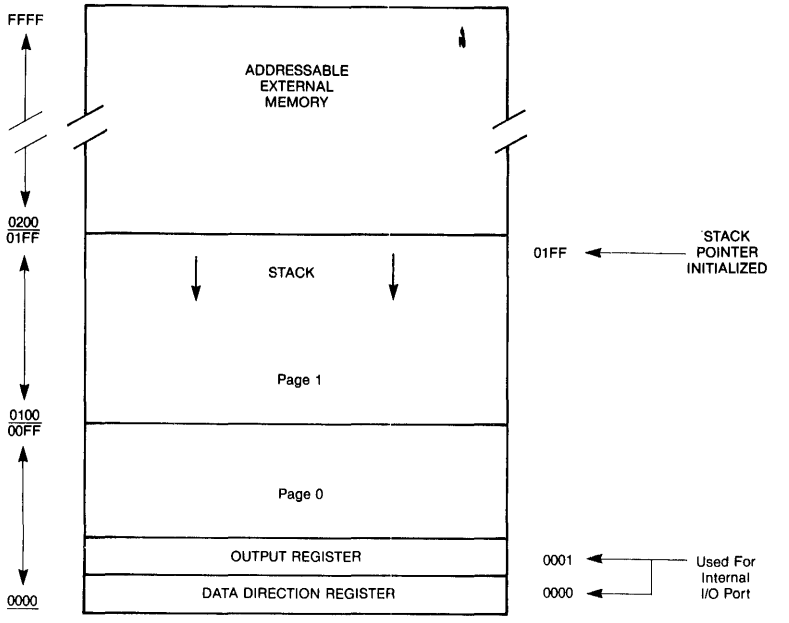
X INDEX, X
Y INDEX, Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
M$_S$ MEMORY PER STACK POINTER

+ ADD
− SUBTRACT
∧ AND
∨ OR

⊻ EXCLUSIVE OR
✓ MODIFIED
· NOT MODIFIED
M$_7$ MEMORY BIT 7
M$_6$ MEMORY BIT 6

N NO CYCLES
NO BYTES

Note: Commodore Semiconductor Group cannot assume liability for the use of undefined OP Codes



6510 MEMORY MAP

APPLICATIONS NOTES

Locating the Output Register at the internal I/O Port in Page Zero enhances the powerful Zero Page Addressing instructions of the 6510.

By assigning the I/O Pins as inputs (using the Data Direction Register) the user has the ability to change the contents of address 0001 (the Output Register) using peripheral devices. The ability to change these contents using peripheral inputs, together with Zero Page Indirect Addressing instructions, allows novel and versatile programming techniques not possible earlier.

6520 PERIPHERAL ADAPTER

DESCRIPTION

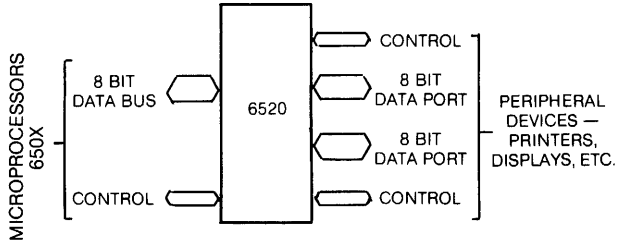
The 6520 Peripheral Adapter is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the 6500 family of microprocessors, the 6520 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or for "hand-shaking" data between the processor and a peripheral device.

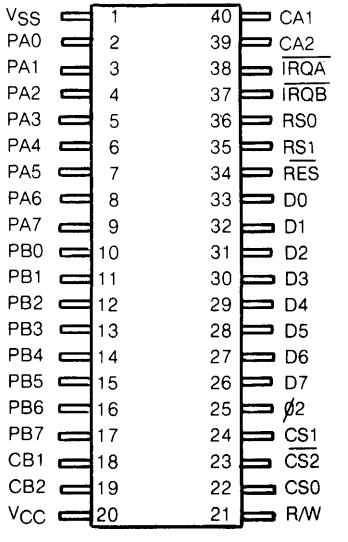
FEATURES

- High performance replacement for Motorola/AMI /MOSTEK/Hitachi peripheral adapter.
- N channel, depletion load technology, single +5V supply.
- Completely Static and TTL compatible.
- CMOS compatible peripheral control lines.
- Fully automatic "hand-shake" allows very positive control of data transfers between processor and peripheral devices.

Basic 6520 Interface Diagram



6520



SUMMARY OF 6520 OPERATION

See MOS TECHNOLOGY Microcomputer Hardware Manual for detailed description of 6520 operation.

CA1/CB1 CONTROL

CRA (CRB) Bit 1	CRA (CRB) Bit 0	Active Transition of Input Signal*	$\overline{IRQA}$ ($\overline{IRQB}$) Interrupt Outputs
0	0	negative	Disable — remain high
0	1	negative	Enable — goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	positive	Disable — remain high
1	1	positive	Enable — as explained above

*Note: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

CA2/CB2 INPUT MODES

CRA (CRB) Bit 5	CRA (CRB) Bit 4	CRA (CRB) Bit 3	Active Transition of Input Signal*	$\overline{IRQA}$ $\overline{(IRQB)}$ Interrupt Output
0	0	0	negative	Disable — remains high
0	0	1	negative	Enable — goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	positive	Disable — remains high
0	1	1	positive	Enable — as explained above

*Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

CA2 OUTPUT MODES

CRA Bit 5	CRA Bit 4	CRA Bit 3	Mode	Description
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 OUTPUT MODES

CRB Bit 5	CRB Bit 4	CRB Bit 3	Mode	Description
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.3 to +7.0V
Input Voltage, V_{IN}	−0.3 to +7.0V
Operating Temperature Range, T_A	0 to +70°C
Storage Temperature Range, T_{STG}	−55 to +150°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STATIC D.C. CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	—	+.8	Vdc
Input Threshold Voltage	V_{IT}	0.8	—	2.0	Vdc
Input Leakage Current	I_{IN}			uAdc	µAdc
V_{in} = 0 to 5.0 Vdc		—	±1.0	±2.5	
R/W, $\overline{Reset}$, RS0,RS1,CS0,CS1,$\overline{CS2}$,CA1,CB1,Ø2					
Three-State (Off State Input Current)	I_{TSI}				
(V_{in} = 0.4 to 2.4 Vdc, V_{CC} = max) D0-D7,PB0-PB7,CB2		—	±2.0	±10	µAdc
Input High Current	I_{IH}				
(V_{IH} = 2.4 Vdc) PA0-PA7,CA2		−100	−250	—	µAdc
Input Low Current	I_{IL}				
(V_{IL} = 0.4 Vdc) PA0-PA7,CA2		—	−1.0	−1.6	mAdc
Output High Voltage	V_{OH}				
(V_{CC} = min, I_{Load} = −100 uAdc)		2.4	—	—	Vdc
Output Low Voltage	V_{OL}				
(V_{CC} = min, I_{Load} = 1.6 mAdc)		—	—	+0.4	Vdc
Output High Current (Sourcing)	I_{OH}				
(V_{OH} = 2.4 Vdc)		−100	−1000	—	µAdc
(V_O = 1.5 Vdc, the current for driving other than TTL, e.g., Darlington Base) PB0-PB7,CB2		−1.0	−2.5	—	mAdc
Output Low Current (Sinking)	I_{OL}				
(V_{OL} = 0.4 Vdc)		1.6	—	—	mAdc
Output Leakage Current (Off State) $\overline{IRQA}$, $\overline{IRQB}$	I_{off}	—	1.0	10	µAdc
Power Dissipation	P_D	—	200	500	mW
Input Capacitance	C_{in}				pF
(V_{in} - 0, T_A = 25°C, f = 1.0 MHz)					
D0-D7,PA0-PA7,PB0-PB7,CA2,CB2		—	—	10	
R/W,$\overline{Reset}$,RS0,RS1,CS0,CS1,CS2,		—	—	7.0	
CA1,CB1,Ø2		—	—	20	
Output Capacitance	C_{out}				
(V_{in} - 0, T_A = 25°C, f = 1.0 MHz)		—	—	10	pF

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

FIGURE 1 — READ TIMING CHARACTERISTICS

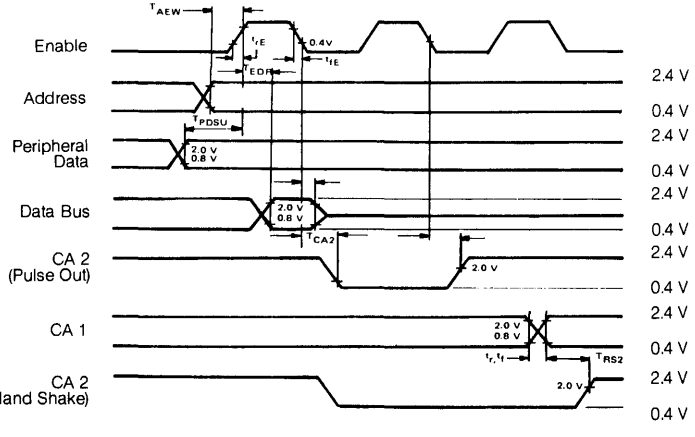
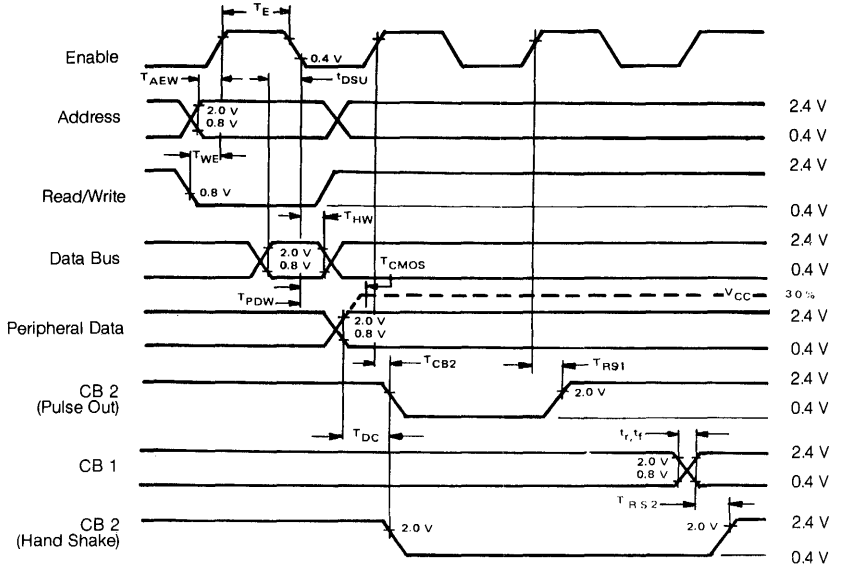


FIGURE 2 — WRITE TIMING CHARACTERISTICS



A.C. CHARACTERISTICS

Figure 1 — Read Timing Characteristics (Loading 130 pF and one TTL load)

Characteristics	Symbol	Min	Typ	Max	Unit
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	—	—	ns
Delay Time, Enable positive transition to Data valid on bus	T_{EDR}	—	—	395	ns
Peripheral Data Setup Time	T_{PDSU}	300	—	—	ns
Data Bus Hold Time	T_{HR}	10	—	—	ns
Delay Time, Enable negative transition to CA2 negative transition	T_{CA2}	—	—	1.0	µs
Delay Time, Enable negative transition to CA2 positive transition	T_{RS1}	—	—	1.0	µs
Rise and Fall Time for CA1 and CA2 input signals	t_r,t_f	—	—	1.0	µs
Delay Time from CA1 active transition to CA2 positive transition	T_{RS2}	—	—	2.0	µs
Rise and Fall Time for Enable input	t_{rE},t_{fE}	—	—	25	ns

Figure 2 — Write Timing Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Enable Pulse Width	T_E	0.470	—	25	µs
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	—	—	ns
Delay Time, Data valid to Enable negative transition	T_{DSU}	300	—	—	ns
Delay Time, Read/Write negative transition to Enable positive transition	T_{WE}	130	—	—	ns
Data Bus Hold Time	T_{HW}	10	—	—	ns
Delay Time, Enable negative transition to Peripheral Data valid	T_{PDW}	—	—	1.0	µs
Delay Time, Enable negative transition to Peripheral Data valid, CMOS (V_{CC} - 30%) PA0-PA7, CA2	T_{CMOS}	—	—	2.0	µs
Delay Time, Enable positive transition to CB2 negative transition	T_{CB2}	—	—	1.0	µs
Delay Time, Peripheral Data valid to CB2 negative transition	T_{DC}	0	—	1.5	µs
Delay Time, Enable positive transition to CB2 positive transition	T_{RS1}	—	—	1.0	µs
Rise and Fall Time for CB1 and CB2 input signals	t_r, t_f	—	—	1.0	µs
Delay Time, CB1 active transition to CB2 positive transition	T_{RS2}	—	—	2.0	µs

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NMOS

MPS

6522

VERSATILE INTERFACE ADAPTER

6522 VERSATILE INTERFACE ADAPTER

PERIPHERALS

DESCRIPTION

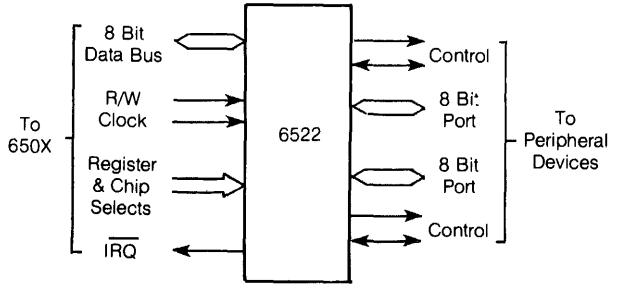
The 6522 Versatile Interface Adapter (VIA) provides all of the capability of the 6520. In addition, this device contains a pair of very powerful interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each of these lines can be programmed to act as either an input or an output. Also, several peripheral I/O lines can be controlled directly from the interval timers for generating programmable-frequency square waves and for counting externally generated pulses. To facilitate control of the many powerful features of this chip, the internal registers have been organized into an interrupt flag register, an interrupt enable register and a pair of function control registers.

FEATURES

- Very powerful expansion of basic 6520 capability.
- N channel, depletion load technology, single +5V supply.
- Completely static and TTL compatible.
- CMOS compatible peripheral control lines.
- Expanded "handshake" capability allows very positive control of data transfers between processor and peripheral devices.

6522 Interface Diagram



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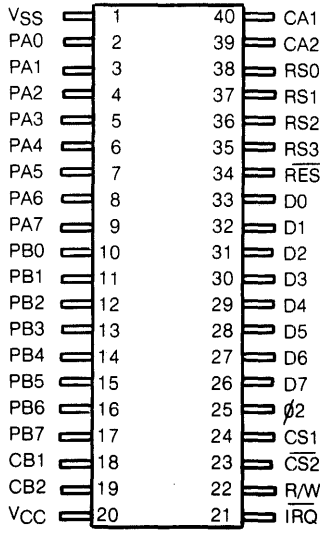


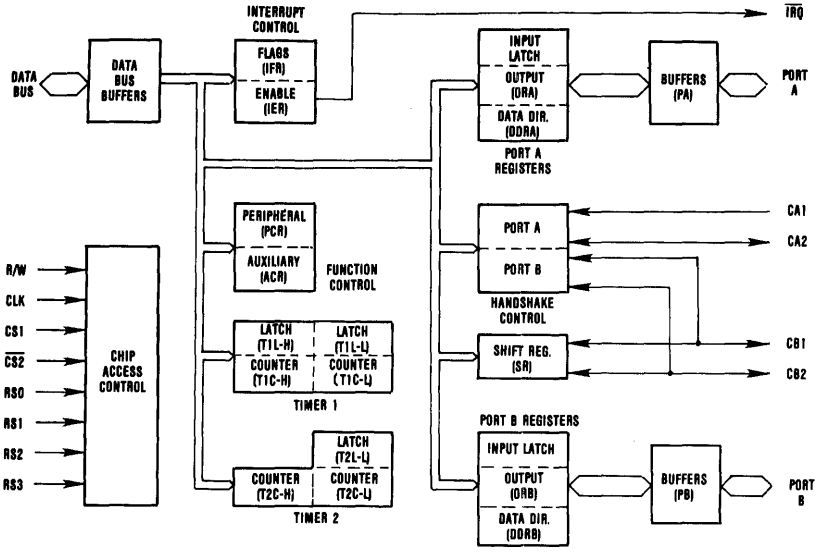


Figure 1. 6522 Block Diagram

PROCESSOR INTERFACE

This section contains a description of the buses and control lines which are used to interface the 6522 to the system processor. AC and DC parameters associated with this interface are specified on pages 21 through 24 of this document.

1. Phase Two Clock (Ø2)

Data transfers between the 6522 and the system processor take place only while the Phase Two Clock is high. In addition, Ø2 acts as the time base for the various timers, shift registers, etc. on the chip.

2. Chip Select Lines (CS1, $\overline{CS2}$)

The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected 6522 register will be accessed when CS1 is high and $\overline{CS2}$ is low.

3. Register Select Lines (RS0, RS1, RS2, RS3)

The four Register select lines are normally connected to the processor address bus lines to allow the processor to select the internal 6522 register which is to be accessed. The sixteen possible combinations access the registers as follows:

RS3	RS2	RS1	RS0	Register	Remarks
L	L	L	L	ORB	
L	L	L	H	ORA	Controls Handshake
L	L	H	L	DDRB	
L	L	H	H	DDRA	
L	H	L	L	T1L-L T1C-L	Write Latch Read Counter
L	H	H	L	T1C-H	Trigger T1L-L/ T1C-L Transf.
L	H	H	L	T1L-L	
L	H	H	H	T1L-H	
H	L	L	L	T2L-L T2C-L	Write Latch Read Counter
H	L	L	H	T2C-H	Triggers T2L-L/ T2C-L Transfer
H	L	H	L	SR	
H	L	H	H	ACR	
H	H	K	K	PCR	
H	H	L	H	IFR	
H	H	H	L	IER	
H	H	H	H	ORA	No Effect on Handshake

Note: L = 0.4V DC, H = 2.4V DC.

4. Read/Write Line (R/W)

The direction of data transfers between the 6522 and the system processor is controlled by the R/W line. If R/W is low, data will be transferred out of the processor into the selected 6522 register (write operation). If R/W is high and the chip is selected, data will be transferred out of the 6522 (read operation).

5. Data Bus (DB0-DB7)

The 8 bi-directional data bus lines are used to transfer data between the 6522 and the system processor. The internal drivers will remain in the high-impedance state except when the chip is selected (CS1 = 1, $\overline{CS2}$ = 0), Read/Write is high and the Phase Two Clock is high. At this time, the contents of the selected register are placed on the data bus. When the chip is selected, with Read/Write low and Ø2 = 1, the data on the data bus will be transferred into the selected 6522 register.

6. Reset ($\overline{RES}$)

The Reset input clears all internal registers to logic 0 (except T1, T2 and SR). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and disables interrupting from the chip.

7. Interrupt Request ($\overline{IRQ}$)

The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This output is "open-drain" to allow the interrupt request signal to be "wire-or'ed" with other equivalent signals in the system.

PERIPHERAL INTERFACE

This section contains a brief description of the buses and control lines which are used to drive peripheral devices under control of the internal 6522 registers.

1. Peripheral A Port (PA0-PA7)

The Peripheral A port consists of 8 lines which can be individually programmed to act as an input or an output under control of a Data Direction Register. The polarity of output pins is controlled by an Output Register and input data can be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode.

2. Peripheral A Control Lines (CA1, CA2)

The two peripheral A control lines act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Peripheral A Port input lines. The various modes of operation are controlled by the system processor through the internal control registers. CA1 is a high-impedance input only while CA2 represents one standard TTL load in the input mode. CA2 will drive one standard TTL load in the output mode.

3. Peripheral B Port (PB0-PB7)

The Peripheral B port consists of 8 bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the PA port. In addition, the polarity of the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 30 ma at 1.5 VDC in the output mode to allow the outputs to directly drive Darlington transistor switches.

4. Peripheral B Control Lines (CB1, CB2)

The Peripheral B control lines act as interrupt inputs or as handshake outputs. As with CA1 and CA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 1.0 ma at 1.5 VDC in the output mode to allow the outputs to directly drive Darlington transistor switches.

6522 OPERATION

This section contains a discussion of the various blocks of logic shown in Figure 1. In addition, the internal operation of the 6522 is described in detail.

A. Data Bus Buffers (DB), Peripheral A Buffers (PA), Peripheral B Buffers (PB)

The characteristics of the buffers which provide the required voltage and current drive capability were discussed in the previous section. AC and DC parameters for these buffers are specified on pages 21 through 24 of this document.

B. Chip Access Control

The Chip Access Control contains the necessary logic to detect the chip select condition and to decode the Register Select inputs to allow accessing the desired internal register. In addition, the R/W and Ø2 signals are utilized to control the direction and timing of data transfers. When writing into the 6522, data is first latched into a data input register during Ø2. Data is then transferred into the desired internal register during Ø2 · Chip Select. This allows the peripheral I/O line to change without "glitching." When the processor reads the 6522, data is transferred from the desired internal register directly onto the Data Bus during Ø2.

C. Port A Registers, Port B Registers

Three registers are used in accessing each of the 8-bit peripheral ports. Each port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A 0 in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A 1 causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register (ORA, ORB) and an Input Register (IRA, IRB). When the pin is programmed to act as an output, the voltage on the pin is controlled by the corresponding bit of the Output Register. A 1 in the Output Register causes the pin to go high, and a 0 causes the pin to go low. Data can be written into Output Register bits corresponding to pins which are programmed to act as inputs; however, the pin will be unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the data on the

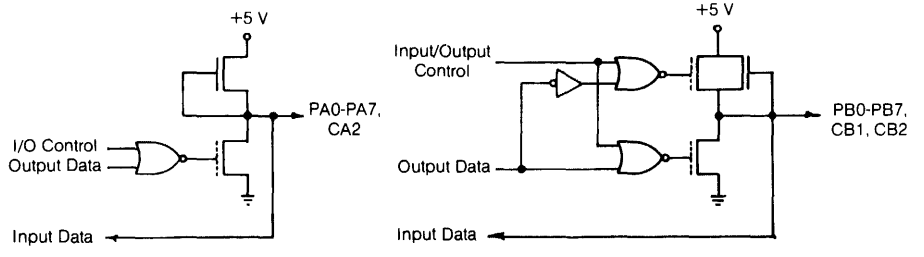


Figure 2. Peripheral Output Buffers

PA pins. With input latching enabled, IRA will reflect the contents of the Port A prior to setting the CA1 Interrupt Flag (IFR1) by an active transition on CA1.

The IRB register operates in a similar manner. However, for output pins, the corresponding IRB bit will reflect the contents of the Output Register bit instead of the actual pin. This allows proper data to be read into the processor if the output pin is not allowed to go to full voltage. With input latching enabled on Port B, setting CB1 interrupt flag will cause IRB to latch this combination of input data and ORB data until the interrupt flag is cleared.

D. Handshake Control

The 6522 allows very positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

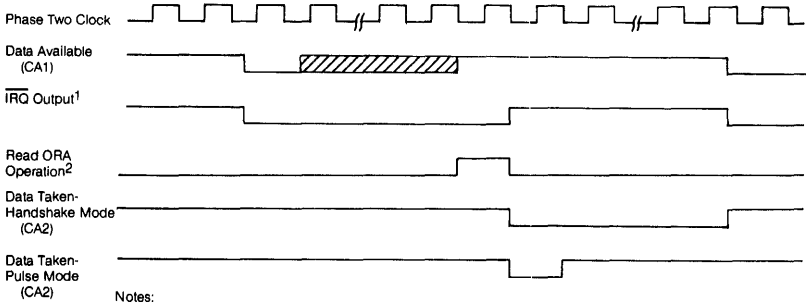
Read Handshake

Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using "Read" handshaking. In this case, the peripheral device must generate "Data Ready" to signal the processor that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the 6522, automatic "Read" handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The Data Ready signal will set an internal flag which may interrupt the processor or which can be polled under software control. The Data Taken signal can be either a pulse or a DC level which is set low by the system processor and is cleared by the Data Ready signal. These options are shown in Figure 3 which illustrates the normal Read Handshaking sequence.

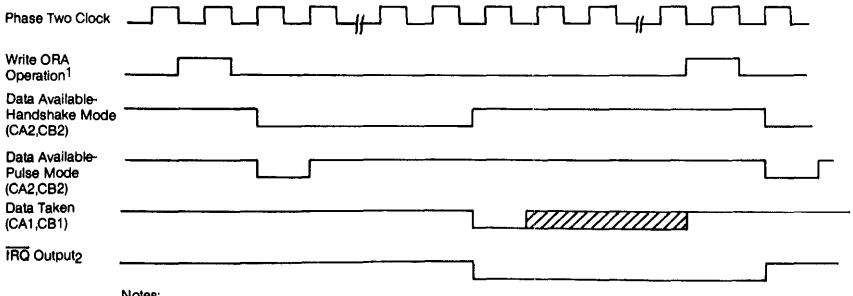
Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described in Section A for Read Handshaking. However, for "Write" handshaking, the processor must generate the "Data Ready" signal (through the 6522) and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the 6522. CA2 or CB2 acts as a Data Ready output in either the DC level or pulse mode and CA1 or CB1 accepts the "Data Taken" signal from the peripheral device, setting the interrupt flag and clearing the "Data Ready" output. This sequence is shown in Figure 4.



Notes:
1. Signals "data available" to the system processor.
2. R/W = 1, $\overline{CS2}$ = 0, CS1 = 1, RS3 = 0, RS2 = 0, RS1 = 0, RS0 = 1.

Figure 3. Read Handshake Timing Sequence



Notes:
1. R/W = 0, $\overline{CS2}$ = 0, CS1 = 1, RS3 = 0, RS2 = 0, RS1 = 0, RS0 = 1.
2. Signals "data taken" to the system processor.

Figure 4. Write Handshake Timing Sequence

TIMER 1

Introduction

Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches are used to store data which is to be loaded into the counter. After loading, the counter decrements at system clock rate, i.e., under control of the clock applied to the Phase Two input pin. Upon reaching zero, an interrupt flag will be set, and $\overline{IRQ}$ will go low. The timer will then disable any further interrupts, or will automatically transfer the contents of the latches into the counter and will continue to decrement. In addition, the timer can be instructed to invert the output signal on a peripheral pin each time it "times-out." Each of these modes is discussed separately below.

Writing the Timer 1 Registers

The operations which take place when writing to each of the four T1 addresses are as follows:

Transfer low order latch into low order

RS3	RS2	RS1	RS0	Operation (R/W = L)
L	H	L	L	Write into low order latch.
L	H	L	H	Write into high order latch. Write into high order counter. Transfer low order latch into low order counter. Reset T1 interrupt flag.
L	H	H	L	Write low order latch.
L	H	H	H	Write high order latch. Reset T1 interrupt flag.

Note that the processor does not write directly into the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes into the high order counter. In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order counter.

The second set of addresses allows the processor to write into the latch register without affecting the count-down in progress. This is discussed in detail below.

Reading the Timer 1 Registers

For reading the Timer 1 registers, the four addresses relate directly to the four registers as follows:

RS3	RS2	RS1	RS0	Operation (R/W = H)
L	H	L	L	Read T1 low order counter. Reset T1 interrupt flag.
L	H	L	H	Read T1 high order counter.
L	H	H	L	Read T1 low order latch.
L	H	H	H	Read T1 high order latch.

Timer 1 Operating Modes

Two bits are provided in the Auxiliary Control Register to allow selection of the T1 operating modes. These bits and the four possible modes are as follows:

ACR7 Output Enable	ACR6 "Free-Run" Enable	Mode
0	0	Generate a single time-out interrupt each time T1 is loaded. PB7 disabled.
0	1	Generate continuous interrupts. PB7 disabled.
1	0	Generate a single interrupt and an output pulse on PB7 for each T1 load operation.
1	1	Generate continuous interrupts and a square wave output on PB7.

Timer 1 One-Shot Mode

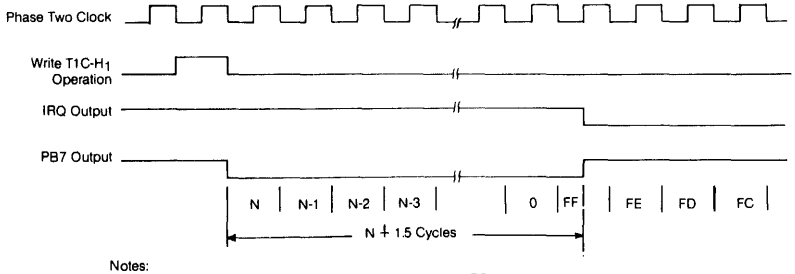
The interval timer one-shot mode allows generation of a single interrupt for each timer load operation. As with any interval timer, the delay between the "write T1C-H" operation and generation of the processor interrupt is a direct function of the data loaded into the timing counter. In addition to generating a single interrupt, Timer 1 can be programmed to produce a single negative pulse on the PB7 peripheral pin. With the output enabled (ACR&=1) a "write T1C-H" operation will cause PB7 to go low. PB7 will return high when Timer 1 times out. The result is a single programmable width pulse.

NOTE

PB7 will act as an output if DDRB7 = 1 or if ACR7 = 1. However, if both DDRB7 and ACR7 are logic 1, PB7 will be controlled from Timer 1 and ORB7 will have no effect on the pin.

In the one-shot mode, writing into the high order latch has no effect on the operation of Timer 1. However, it will be necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation. When the processor writes into the high order counter, the T1 interrupt flag will be cleared, the contents of the low order latch will be transferred into the low order counter, and the timer will begin to decrement at system clock rate. If the PB7 output is enabled, this signal will go low on the phase two following the write operation. When the counter reaches zero, the T1 interrupt flag will be set, the $\overline{IRQ}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless it has been cleared as described on page 13 of this specification.

Timing for the 6522 interval timer one-shot modes is shown in Figure 5.



Notes:
1. R/W = L, CS2 = L, CS1 = H, RS3 = L, RS2 = H, RS1 = RS0 = H.

Figure 5. Interval Timer "One-shot" Mode Timing Sequence.

Timer 1 Free-Running Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode (ACR6 = 1), the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero. However, instead of continuing to decrement from zero after a time-out, the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. The interrupt flag can be cleared by writing T1C-H, by reading T1C-L, or by writing directly into the flag as described below. However, it is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out.

All interval timers in the 6500 family devices are "re-triggerable." Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated. Timing for the free-running mode is shown in Figure 6.

TIMER 2

Timer 2 operates as an interval timer (in the "one-shot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit is provided in the Auxiliary Control Register to select between these two modes. This timer is comprised of a "write-only" low-order latch (T2L-L), a "read-only" low-order counter and a read/write high-order counter. The counter registers act as a 16-bit counter which decrements at Ø2 rate.

Timer 2 addressing can be summarized as follows:

RS3	RS2	RS1	RS0	R/W = 0	R/W = 1
H	L	L	L	Write T2L-L	Read T2C-L Clear Interrupt flag
H	L	L	H	Write T2C-H Transfer T2L-L to T2C-L Clear Interrupt flag	Read T2C-H

Timer 2 Interval Timer Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, the counter will continue to decrement. However, setting of the interrupt flag will be disabled after initial time-out so that it will not be set by the counter continuing to decrement through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 5.

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag will be set when T2 reaches zero. At this time the counter will continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on subquent down-counting operations. Timing for this mode is shown in Figure 7. The pulse must be low on the leading edge Ø2.

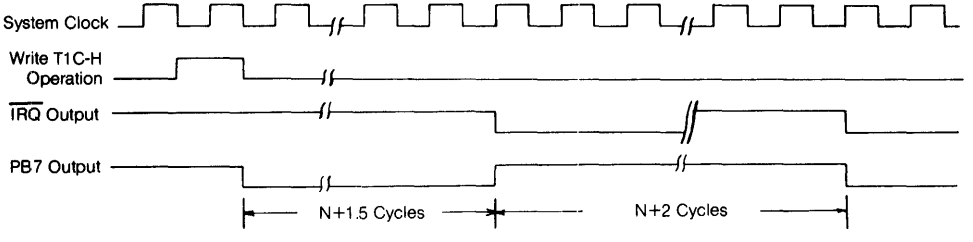


Figure 6. Timer 1 "Free-Running" Mode

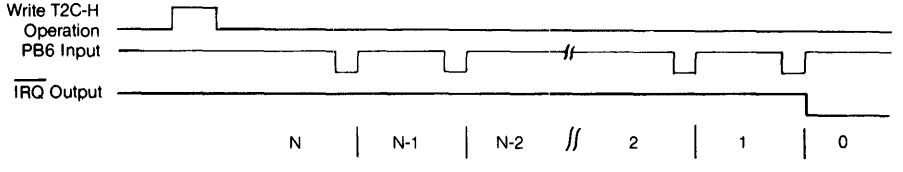


Figure 7. Timer 2 Pulse Counting Mode

SHIFT REGISTER

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling shifting in external devices.

The control bits which allow control of the various shift register operating modes are located in the Auxiliary Control Register. These bits can be set and cleared by the system processor to select one of the operating modes discussed in the following paragraphs.

Shift Register Input Modes

Bit 4 of the Auxiliary Control Register selects the input or output modes. There are three input modes and four output modes, differing primarily in the source of the pulses which control the shifting operation. With ACR4 = 0 the input modes are selected by ACR3 and ACR2 as follows:

ACR4	ACR3	ACR2	Mode
0	0	0	Shift Register *Disabled*
0	0	1	Shift in under control of Timer 2
0	1	0	Shift in at System Clock Rate.
0	1	1	Shift in under control of external input pulses

Mode 000 — Shift Register Disabled

The 000 mode is used to disable the Shift Register. In this mode the microprocessor can write or read the SR, but the shifting operation is disabled and operation of CB1 and CB2 is controlled by the appropriate bits in the Peripheral Control Register (PCR). In this mode the SR Interrupt Flag is disabled (held to a logic 0).

Mode 001 — Shift In under Control of Timer 2

In this mode the shifting rate is controlled by the low order 8 bits of T2. Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch.

The shifting operation is triggered by writing or reading the shift register. Data is shifted first into the low order bit of SR and is then shifted into the next higher order bit of the shaft register on the trailing edge of each clock pulse. As shown in Figure 8, the input data should change before the leading edge of the clock pulse. This data is loaded into the shift register during the system clock cycle following the trailing edge of the clock pulse. After 8 clock pulses, the shift register interrupt flag will be set and $\overline{IRQ}$ will go low.

Mode 010 — Shift In at System Clock Rate

In this mode the shift rate is a direct function of the system clock frequency. CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.

Mode 011 — Shift In under Control of External Clock

In this mode CB1 becomes an input. This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. However, the shift register counter does not stop the shifting operation; it acts simply as a pulse counter. Reading or

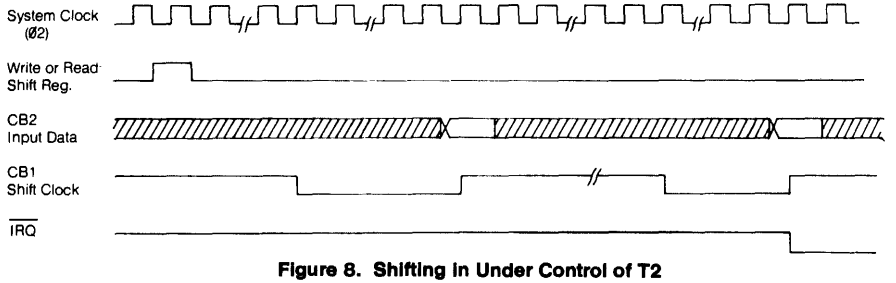


Figure 8. Shifting In Under Control of T2

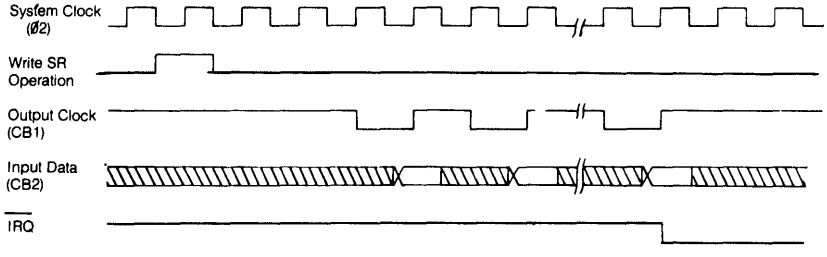


Figure 9. Timing Sequence for Shifting in at System Clock Rate

writing the Shift Register resets the Interrupt flag and initializes the SR counter to count another 8 pulses.

Note that data is shifted during the first system clock cycle following the leading edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high. Timing for this operation is illustrated in Figure 10.

Shift Register Output Modes

The four Shift Register Output Modes are selected by setting the Input/Output Control Bit (ACR4) to a logic 1 and then selecting the specific output mode with ACR3 and ACR2. In each of these modes the Shift Register shifts data out of bit 7 to the CB2 pin. At the same time the contents of bit 7 are shifted back into bit 0. As in the input modes, CB1 is used either as an output to provide shifting pulses out or as an input to allow shifting from an external pulse. The four modes are as follows:

ACR4	ACR3	ACR2	Mode
1	0	0	Shift out — Free-running mode. Shift rate controlled by T2.
1	0	1	Shift out — Shift rate controlled by T2. Shift pulses generated on CB1.
1	1	0	Shift out at system clock rate.
1	1	1	Shift out under control of an external pulse.

Mode 100 Free-Running Output

This mode is very similar to mode 101 in which the shifting rate is set by T2. However, in mode 100 the SR Counter does not stop the shifting operation. Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CB2 repetitively. In this mode the shift register counter is disabled.

Mode 101 — Shift out under Control of T2

In this mode the shift rate is controlled by T2 (as in the previous mode). However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt flag is set and CB2 goes to a state determined by the CB2 Control bit (PC5) in the Peripheral Control Register.

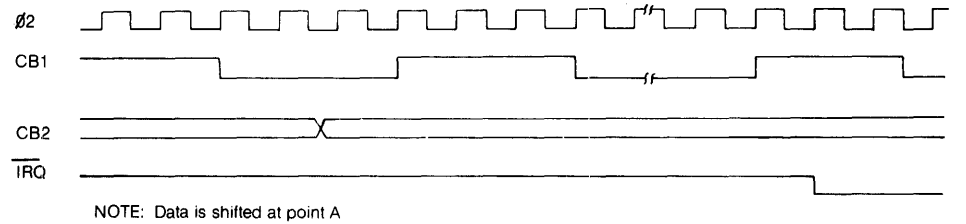
If the shift register is reloaded before the last time-out, the shifting will continue. This sequence is illustrated in Figure 11.

Mode 110 — Shifting out at System Clock Rate

In this mode the shift register operation is similar to that shown in Figure 11. However, the shifting rate is a function of the system clock on the chip enable pin (02) and is independent of T2. Timer 2 resumes its normal function as an independent interval timer. Figure 12 illustrates the timing sequence for mode 110.

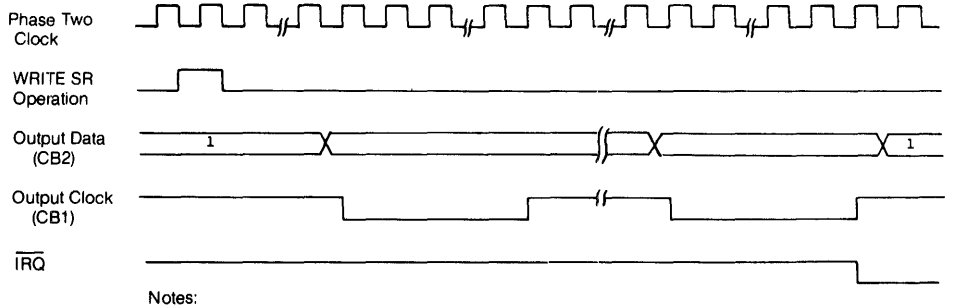
Mode 111 — Shift out under Control of an External Pulse

In this mode, shifting is controlled by pulses applied to the CB1 pin by an external device. The SR counter sets the SR Interrupt flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor writes or reads the shift register, the SR Interrupt flag is reset and the SR Counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the interrupt flag is set. The microprocessor can then load the shift register with the next byte of data.



NOTE: Data is shifted at point A

Figure 10. Timing sequence for shifting in under control of external clock



Notes:
1. Data out determined by CB2 control in PCR.

Figure 11. Shifting out under Control of T2.

INTERRUPT CONTROL

Controlling interrupts within the 6522 involves three principal operations. These are flagging the interrupts, enabling interrupts and signalling to the processor that an active interrupt exists within the chip. Interrupt flags are set by interrupting conditions which exist within the chip or on inputs to the chip. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order from highest to lowest priority. This is accomplished by reading the flag register into the processor accumulator, shifting this register either right or left and then using conditional branch instructions to detect an active interrupt.

Associated with each interrupt flag is an interrupt enable bit. This bit can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire or'ed" with other devices in the system to interrupt the processor.

In the 6522, all the interrupt flags are contained in one register. In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

	7	6	5	4	3	2	1	0
Interrupt Flag Register	IRQ	T1	T2	CB1	CB2	SR	CA1	CA2
Interrupt Enable Register	Set/ clear control	T1	T2	CB1	CB2	SR	CA1	CA2

Interrupt Flag Register

The IFR is a read/bit-clear register. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the $\overline{IRQ}$ output. This bit corresponds to the logic function: IRQ = IFR6 X IER6 + IFR5 X IER5 + IFR4 X IER4 + IFR3 X IER3 + IFR2 X IER2 + IFR1 X IER1 + IFR0 X IER0. Note: X = logic AND, + = Logic OR.

Bits six through zero are latches which are set and cleared as follows:

Bit #	Set by	Cleared by
0	Active transition of the signal on the CA2 pin.	Reading or writing the A Port Output Register (ORA) using address 0001.
1	Active transition of the signal on the CA1 pin.	Reading or writing the A Port Output Register (ORA) using address 0001.
2	Completion of eight shifts	Reading or writing the Shift Register.
3	Active transition of the signal on the CB2 pin.	Reading or writing the B Port Output Register.
4	Active transition of the signal on the CB1 pin.	Reading or writing the B Port Output Register.
5	Time-out of Timer 2.	Reading T2 low order counter. Writing T2 high order counter.
6	Time-out of Timer 1.	Reading T1 lower order counter. Writing T1 high order latch.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabiling all the active interrupts as discussed in the next section.

Interrupt Enable Register (IER)

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register. The system processor can set or clear selected bits in this register to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to address 1110 (IER address). If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Setting selected bits in the Interrupt Enable Register is accomplished by writing to the same address with bit 7 in the data word set to a logic 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of interrupts during system operation.

In addition to setting and clearing IER bits, the processor can read the contents of this register by placing the proper address on the register select and chip select inputs with the R/W line high. Bit 7 will be read as a logic 0.

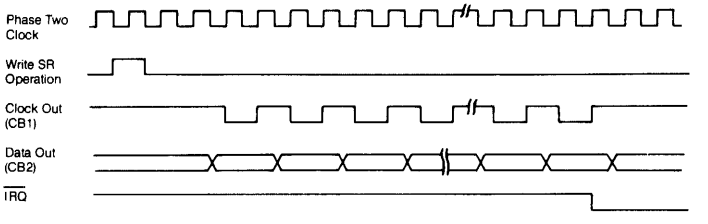


Figure 12. Shifting out under Control of System Clock

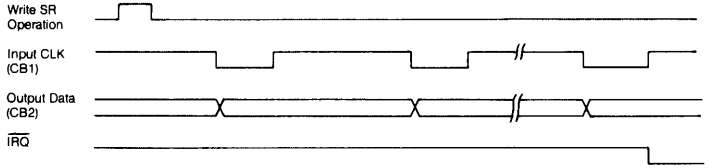


Figure 13. Shifting out under Control of External Clock

FUNCTION CONTROL

Control of the various functions and operating modes within the 6522 is accomplished primarily through two registers, the Peripheral Control Register (PCR), and the Auxiliary Control Register (ACR). The PCR is used primarily to select the operating mode for the four peripheral control pins. The Auxiliary Control Register selects the operating mode for the interval timers (T1, T2), and the serial port (SR).

Peripheral Control Register

The Peripheral Control Register is organized as follows:

Bit # —	7	6	5	4	3	2	1	0
Function—	CB2 Control			CB1 Control	CA2 Control			CA1 Control

Each of these functions is discussed in detail below.

1. CA1 Control

Bit 0 of the Peripheral Control Register selects the active transition of the input signal applied to the CA1 interrupt input pin. If this bit is a logic 0, the CA1 interrupt flag will be set by a negative transition (high to low) of the signal on the CA1 pin. If PCR0 is a logic 1, the CA1 interrupt flag will be set by a positive transition (low to high) of this signal.

2. CA2 Control

The CA2 pin can be programmed to act asn an interrupt input or as a peripheral control output. As an input, CA2 operates in two modes, differing primarily in the methods available for resetting the interrupt flag. Each of these two input modes can operate with either a positive or a negative active transition as described above for CA1.

In the output mode, the CA2 pin combines the operations performed on the CA2 and CB2 pins of the 6520. This added flexibility allows processor to perform a normal "write" handshaking in a system which uses CB1 and CB2 for the serial operations described above. The CA2 operating modes are selected as follows:

PCR3	PCR2	PCR1	Mode
0	0	0	Input mode — Set CA2 interrupt flag (IFRO) on a negative transition of the input signal. Clear IFRO on a read or write of the Peripheral A Output Register.
0	0	1	Independent interrupt input mode — Set IFRO on a negative transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag.
0	1	0	Input mode — Set CA2 interrupt flag on a positive transition of the CA2 input signal. Clear IFRO with a read or write of the Peripheral A Output Register.
0	1	1	Independent interrupt input mode — Set IFRO on a positive transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag.
1	0	0	Handshake output mode — Set CA2 output low on a read or write of the Peripheral A Output Register. Reset CA2 high with an active transition on CA1.
1	0	1	Pulse Output mode — CA2 goes low for one cycle following a read or write of the Peripheral A Output Register.
1	1	0	Manual output mode — The CA2 output is held low in this mode.
1	1	1	Manual output mode — The CA2 output is held high in this mode.

In the independent input mode, writing or reading the ORA register has no effect on the CA2 interrupt flag. This flag must be cleared by writing a logic 1 into the appropriate IFR bit. This mode allows the processor to handle interrupts which are independent of any operations taking place on the peripheral I/O ports.

The handshake and pulse output modes have been described previously. Note that the timing of the output signal varies slightly depending on whether the operation is initiated by a read or a write.

3. CB1 Control

Control of the active transition of the CB1 input signal operates in exactly the same manner as that described above for CA1. If PCR4 is a logic 0 the CB1 interrupt flag (IFR4) will be set by a negative transition of the CB1 input signal and cleared by a read or write of the ORB register. If PCR4 is a logic 1, IFR4 will be set by a positive transition of CB1.

If the Shift Register function has been enabled, CB1 will act as an input or output for the shift register clock signals. In this mode the CB1 interrupt flag will still respond to the selected transition of the signal on the CB1 pin.

4. CB2 Control

With the serial port disabled, operation of the CB2 pin is a function of the three high order bits of the PCR. The CB2 modes are very similar to those described previously for CA2. These modes are selected as follows:

PCR7	PCR6	PCR5	Mode
0	0	0	Interrupt input mode — Set CB2 interrupt flag (IFR3) on a negative transition of the CB2 input signal. Clear IFR3 on a read or write of the Peripheral B Output Register.
0	0	1	Independent interrupt input mode — Set IFR3 on a negative transition of the CB2 input signal. Reading or writing ORB does not cear the interrupt flag.
0	1	0	Input mode — Set CB2 interrupt flag on a positive transition of the CB2 input signal. Clear the CB2 interrupt flag on a read or write of ORB.
0	1	1	Independent input mode — Set IFR3 on a positive transition of the CB2 input signal. Reading or writing ORB does not clear the CB2 interrupt flag.
1	0	0	Handshake output mode — Set CB2 low on a write ORB operation. Reset CB2 high with an active transition of the CB1 input signal.
1	0	1	Pulse output mode — Set CB2 low for one cycle following a write ORB operation.
1	1	0	Manual output mode — The CB2 output is held low in this mode.
1	1	1	Manual output mode — The CB2 output is held high in this mode.

Auxiliary Control Register

Many of the functions in the Auxiliary Control Register have been discussed previously. However, a summary of this register is presented here as a convenient reference for the 6522 user. The Auxiliary Control Register is organized as follows:

Bit # —	1	6	5	4	3	2	1	0
Function—	T1 Control		T2 Control	Shift Register Control			PB Latch Enable	PA Latch Enable

1. PA Latch Enable

The 6522 provides input latching on both the PA and PB ports. In this mode, the data present on the peripheral A input pins will be latched within the chip when the CA1 interrupt flag is set. Reading the PA port will result in these latches being transferred into the processor. As long as the CA1 interrupt flag is set, the data on the peripheral pins can change without affecting the data in the latches. This input latching can be used with any of the CA2 input or output modes.

It is important to note that on the PA port, the processor always reads the data on the peripheral pins (as reflected in the latches). For output pins, the processor still reads the latches. This may or may not reflect the data currently in the ORA. Proper system operation requires careful planning on the part of the system designer if input latching is combined with output pins on the peripheral ports.

Input latching is enabled by setting bit 0 in the Auxiliary Control Register to a logic 1. As long as this bit is a 0, the latches will directly reflect the data on the pins.

2. PB Latch Enable

Input latching on the PB port is controlled in the same manner as that described for the PA port. However, with the peripheral B port the input latch will store either the voltage on the pin or the contents of the Output Register (ORB) depending on whether the pin is programmed to act as an input or an output. As with the PA port, the processor always reads the input latches.

3. Shift Register Control

The Shift Register operating mode is selected as follows:

ACR4	ACR3	ACR2	Mode
0	0	0	Shift Register Disabled.
0	0	1	Shift in under control of Timer 2.
0	1	0	Shift in under control of system clock.
0	1	1	Shift in under control of external clock pulses.
1	0	0	Free-running output at rate determined by Timer 2.
1	0	1	Shift out under control of Timer 2.
1	1	0	Shift out under control of the system clock.
1	1	1	Shift out under control of external clock pulses.

4. T2 Control

Timer 2 operates in two modes. If ACR5 = 0, T2 acts as an interval timer in the one-shot mode. If ACR5 = 1, Timer 2 acts to count a predetermined number of pulses on pin PB6.

5. T1 Control

Timer 1 operates in the one-shot or free-running mode with the PB7 output control enabled or disabled. These modes are selected as follows:

ACR7	ACR6	Mode
0	0	One-shot mode — Output to PB7 disabled.
0	1	Free-running mode — Output to PB7 disabled.
1	0	One-shot mode — Output to PB7 enabled.
1	1	Free-running mode. Output to PB7 enabled.

APPLICATION OF THE 6522

The 6522 represents a significant advance in general-purpose microprocessor I/O. Unfortunately, its many powerful features, coupled with a set of very flexible operating modes, cause this device to appear to be very complex at first glance. wever, a detailed analysis will show that the VIA is organized to allow convenient control of these powerful features. This section seeks to assist the system designer in his understanding of the 6522 by illustrating how the device can be used in microprocessor-based systems.

A. Control of 6522 Interrupts

Organization of the 6522 interrupt flags into a single register greatly facilitates the servicing of interrupts from this device. Since there is only one IRQ output for the seven possible sources of interrupt within the chip, the processor must examine these flags to determine the cause of an interrupt. This is best accomplished by first transferring the contents of the flag register into the accumulator. At this time it may be necessary to mask off those flags which have been disabled in the Interrupt Enable Register. This is particularly important for the edge detecting inputs where the flags may be set whether or not the interrupting function has been enabled. Masking off those flags can be accomplished by performing an AND operation between the IER and the accumulator or by performing an "AND IMMEDIATE." The second byte of this AND # instruction should specify those flags which correspond to interrupt functions which are to be serviced.

If the N flag is set after these operations, an active interrupt exists within the chips. This interrupt can be detected with a series of shift and branch instructions.

Clearing interrupt flags is accomplished very conveniently by writing a logic 1 directly into the appropriate bit of the Interrupt Flag Register. This can be combined with an interrupt enable or disable operation as follows:

```
LDA #@10010000      initialize accumulator
STA IFR             clear interrupt flag
STA IER             set interrupt enable flag
```

or:

```
LDA #@00001000      initialize accumulator
STA IFR             clear interrupt flag
STA IFR             disable interrupt
```

Another very useful technique for clearing interrupt flags is to simply transfer the contents of the flag register back into this register as follows:

```
LDA IFR             transfer IFR to accumulator
STA IFR             clear flags corresponding to active
                    interrupts
```

After completion of this operation the accumulator will still contain the interrupt flag information. Most important, writing into the flag register clears only those flags which are already set. This eliminates the possibility of inadvertently clearing a flag while it is being set.

B. Use of Timer 1

Timer 1 represents one of the most powerful features of the 6522. The ability to generate very evenly spaced interrupts and the ability to control the voltage on PB7 makes this timer particularly valuable in various timing, data detection and waveform generation applications.

Time-of-Day Clock Applications

An important feature of many systems is the time-of-day clock. In microprocessor-based systems the time of day is usually maintained in memory and is updated in an interrupt service routine. A regular processor interrupt will then assure that this time of day will always be available when it is needed in the main program.

Generating very regular interrupts using previously available timers presented difficulties because of the need to re-load the timer for each interrupt. Unfortunately, the time between the interrupts will fluctuate due to variations in the interrupt response time. This program is eliminated in the Timer 1 "free-running" mode. The accuracy of these "free-running" interrupts is only a function of the system clock and is not affected by interrupt response time.

Asynchronous Data Detection

The extraction of clock and data information from serial asynchronous ASCII signals or from any single channel data recording device relies on the ability to establish accurate strobes. As discussed previously, the period of these strobes can be seriously affected by the interrupt response time using conventional timers. However, T1 again allows generation of very accurate interrupts. The processor responds to these interrupts by strobing the input data. The ability to reload the T1 latches without affecting the count-down in progress is very useful in this application. This allows the strobe time to be doubled or halved during data detection. See Figure 14 for sequence of operations.

Waveform Generation with Timer 1

In addition to generating processor interrupts, Timer 1 can be used to control the output voltage on peripheral pin PB7 (output mode). In this mode a single negative pulse can be generated on PB7 (one-shot mode), or in the free-running mode, a continuous waveform can be generated. In this latter mode the voltage on PB7 will be inverted each time T1 times out.

A single solenoid can be triggered very conveniently in the one-shot mode if the PB7 signal is used to control the solenoid directly. With this configuration the solenoid can be triggered by simply writing to T1C-H.

Generating very complex waveforms can be a simple problem if T1 is used to control PB7 in the free-running mode. During any count-down process the latches can be loaded to determine the length of the next count-down period. Figure 15 shows this timing sequence for generating ASCII serial data.

An application where this mode of operation is also very powerful is in the generation of bi-phase encoded data for tape or disk storage. This encoding technique and the sequence of operations which would take place are illustrated in Figure 16.

These applications represent only a tiny portion of the potential T1 applications. Some other possibilities are pulse width modulation waveforms, sound generation for video games, A/D techniques requiring very accurate pulse widths, and waveform synthesis in electronic games.

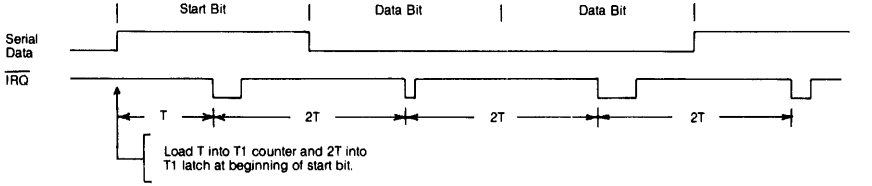
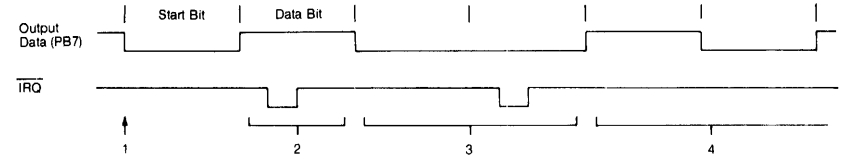
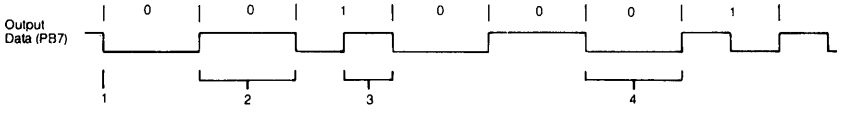


Figure 14. Detecting Asynchronous Data Using Timer 1



1. Load T into T1 counter and latch. Load T into T2 to trigger T1 latch reload.
2. Load 2T into T1 latch during this bit time. Load 2T into T2.
3. Load T into T1 latch anytime during this period. Load NT into T2. N = number of 1's or 0's which follow.
4. A series of 1's and 0's will be generated until the T1 latch is again changed. Note that the use of T2 to control reloading the T1 latch eliminates the need to interrupt on each transition.

Figure 15. ASCII Serial Data Generation Using T1



1. Load T1 counter and latch.
2. Shift T1 latch one bit to the right during this period.
3. Shift T1 latch left during this period.
4. Shift T1 latch right during this period.

Note that T1 must be accessed only when the output data changes. A string of 1's and 0's can be generated without processor intervention.

Figure 16. Generating Bi-phase Encoded Data

Using the 6522 Shift Register

The Shift Register in the 6522 is designed primarily as a synchronous serial communications port for distributed systems. These systems can be either single-processor with distributed peripheral controllers or distributed processor systems. The most important characteristic of the Shift Register in these applications is its ability to transfer information at relatively slow data rates to allow the use of R-C noise suppression techniques. This transfer can be accomplished while the processor is servicing other aspects of the system. An example of a simple 2-processor distributed system is shown in Figure 17. Use of the 6522 Shift Register allows effective communication between the two systems without the use of relatively complex asynchronous communications techniques.

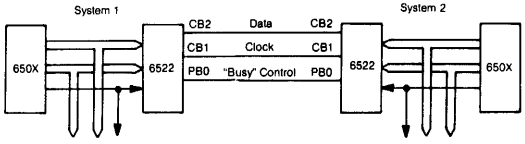


Figure 17. Using Shift Register for Inter-System Communication

In a system with distributed peripherals, the Shift Register can be used to transfer data to the peripheral interface devices. This is illustrated in Figure 18 for a system with a number of distributed status displays. These displays are serviced by stand-alone controllers which actuate the lamps in the status displays through simple drivers. The data and clock lines are wired in parallel to each unit. In addition, a single 6522 peripheral port output allows selection of the display to be loaded. These select lines can be eliminated if all displays are to contain the same information. With the system shown, the status display can be updated at any time by simply selecting the desired display and then writing to the Shift Register.

Remote input devices can be serviced in much the same manner by shifting data into the Shift Register under control of a peripheral port output as shown in Figure 18. Each set of input switches can be polled by first selecting the set to be polled and then triggering the shifting operation with a Shift Register read operation. A shift register interrupt can be used to cause the processor to read the resulting input information after shifting is complete.

The techniques described above can be utilized to expand I/O capability in a microprocessor based system. In a system with many status lamps or many input switches, simple TTL shift registers will provide the necessary I/O in a very cost effective manner. This is illustrated in Figure 19.

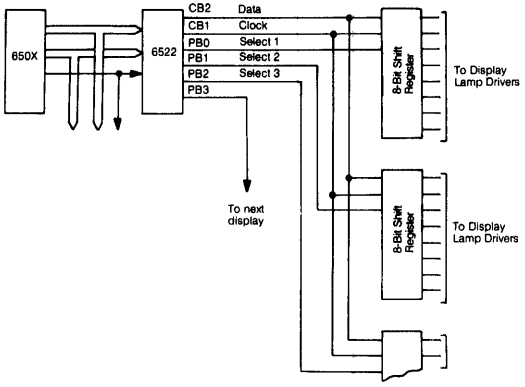


Figure 18. Using the Shift Register for Servicing Remote Status Displays

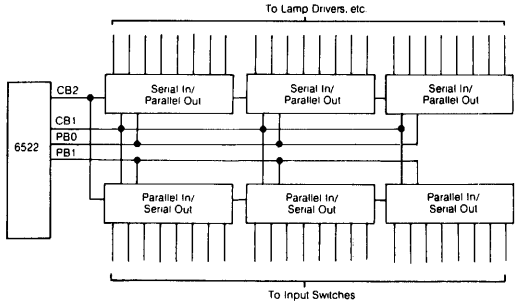
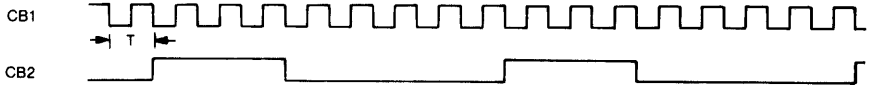


Figure 19. Expanding System I/O Using Shift Register

Clock Generation Using the Shift Register

In all output modes the data shifted out of bit 7 will also be shifted into bit 0. For this reason the Shift Register need not be re-loaded if the same data is to be shifted out each time. A Shift Register read operation can be used to trigger the shifting operation.

This capability is very useful for generating peripheral clocks in the continuous output mode. This mode allows an 8-bit pattern to be shifted out continuously. This is illustrated in Figure 20. Note that in this mode the shifting operation is controlled by Timer 2. A single bit time can therefore be up to 256 clock cycles in length.



Notes:
1. Shift Register loaded with 1110 0000_2 initially.
2. T determined by Timer 2.

Figure 20. Clock Generation Using SR Free-Running Mode

MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input/Output Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature, T_{OP}	0 C to 70 C
Storage Temperature, T_{STG}	−55 C to 150 C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STATIC D.C. CHARACTERISTICS (Vcc = 5.0 V ± 5%, Vss = 0, T_A = 0 to +70 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (normal operation)	V_{IH}	+2.4	—	Vcc	Vdc
Input low voltage (normal operation)	V_{IL}	−0.3	—	+0.4	Vdc
Input leakage current- V_{in} = 0 to 5 Vdc R/W, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, Ø2	I_{IN}	—	±1.0	±2.5	µAdc
Off-state input current- V_{in} = .4 to 2.4 V Vcc = Max, D0 to D7	I_{TSI}	—	±2.0	±10	µAdc
Input high current- V_{IH} = 2.4 V PA0-PA7, CA2, PB0-PB7, CB1, CB2	I_{IH}	−100	−250	—	µAdc
Input low current- V_{IL} = 0.4 Vdc PA0-PA7, CA2, PB0-PB7, CB1, CB2	I_{IL}	—	−1.0	−1.6	mAdc
Output high voltage Vcc = min, I_{load} = −100 µAdc PA0-PA7, CA2, PB0-PB7, CB1, CB2	V_{CH}	2.4	—	—	Vdc
Output low voltage Vcc = min, I_{load} = 1.6 mAdc	V_{OL}	—	—	+0.4	Vdc
Output high current (sourcing) V_{OH} = 2.4 V V_{OH} = 1.5 V, PB0-PB7, CB1, CB2	I_{OH}	 −100 −3.0	 −1000 −5.0	 — —	 µAdc mAdc
Output low current (sinking) V_{OL} = 0.4 Vdc.	I_{OL}	1.6	—	—	mAdc
Output leakage current (off state) $\overline{IRQ}$	I_{OFF}	—	1.0	10	µAdc
Input Capacitance- T_A = 25 °C, f = 1 MHz R/W, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$ D0-D7, PA0-PA7, CA2, PB0-PB7, CB1, CB2 Ø2 input	C_{IN}	 — — —	 — — —	 7.0 10 20	 pF pF pF
Output capacitance- T_A = 25 °C, f = 1 MHz	C_{OUT}	—	—	10	pF
Power dissipation	P_D	—		1000	MW

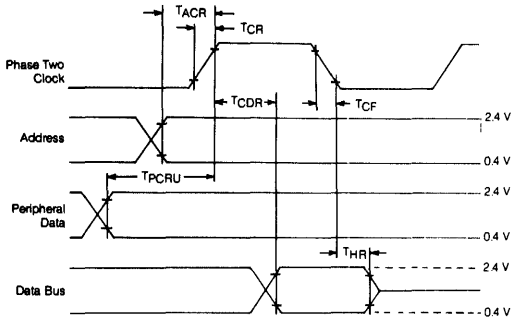


Figure 21. Read Timing Characteristics

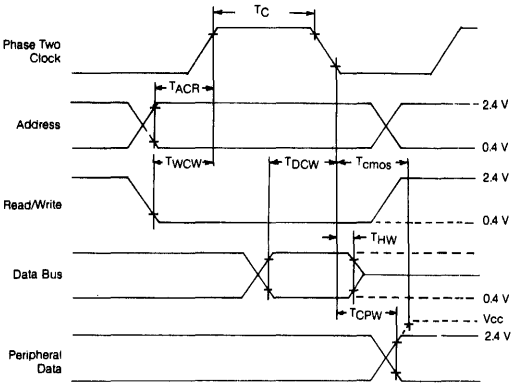


Figure 22. Write Timing Characteristics

A.C. CHARACTERISTICS

Read Timing Characteristics (loading 130 pF and one TTL load)

Characteristic	Symbol	Min	Typ	Max	Unit
Delay time, address valid to clock positive transition	T_{ACR}	180	—	—	nS
Delay time, clock positive transition to data valid on bus	T_{CDR}	—	—	395	nS
Peripheral data setup time	T_{PCR}	300	—	—	nS
Data bus hold time	T_{HR}	10	—	—	nS
Rise and fall time for clock input	T_{RC} T_{RF}	—	—	25	nS

Write Timing Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Enable pulse width	T_C	0.47	—	25	μS
Delay time, address valid to clock positive transition	T_{ACW}	180	—	—	nS
Delay time, data valid to clock negative transition	T_{DCW}	300	—	—	nS
Delay time, read/write negative transition to clock positive transition	T_{WCW}	180	—	—	nS
Data bus hold time	T_{HW}	10	—	—	nS
Delay time, Enable negative transition to peripheral data valid	T_{CPW}	—	—	1.0	μS
Delay time, clock negative transition to peripheral data valid CMOS (Vcc — 30%)	T_{CMOS}	—	—	2.0	μS

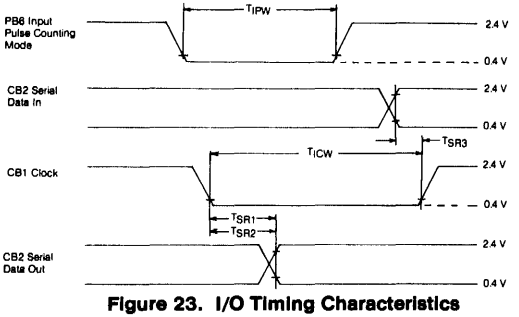


Figure 23. I/O Timing Characteristics

Peripheral Interface Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Rise and fall time for CA1, CB1, CA2 and CB2 input signals.	T_{RF}	—	—	1.0	µS
Delay time, clock negative transition to CA2 negative transition (read handshake or pulse mode).	T_{CA2}	—	—	1.0	µS
Delay time, clock negative transition to CA2 positive transition (pulse mode).	T_{RS1}	—	—	1.0	µS
Delay time, CA1 active transition to CA2 positive transition (handshake mode).	T_{RS2}	—	—	2.0	µS
Delay time, clock positive transition to CA2 or CB2 negative transition (write handshake).	T_{WHS}	—	—	1.0	µS
Delay time, peripheral data valid to CB2 negative transition.	T_{DC}	0	—	1.5	µS
Delay time, clock positive transition to CA2 or CB2 positive transition (pulse mode).	T_{RS3}	—	—	1.0	µS
Delay time, CB1 active transition to CA2 or CB2 positive transition (handshake mode).	T_{RS4}	—	—	2.0	µS
Delay time, peripheral data valid to CA1 or CB1 active transition (input latching).	T_{IL}	300	—	—	nS
Delay time, CB1 negative transition to CB2 data valid (internal SR clock, shift out).	T_{SR1}	—	—	300	nS
Delay time, negative transition of CB1 input clock to CB2 data valid (external clock, shift out).	T_{SR2}	—	—	300	nS
Delay time, CB2 data valid to positive transition of CB1 clock (shift in, internal or external clock)	T_{SR3}	—	—	300	nS
Pulse Width — PB6 Input Pulse	T_{IPW}	2	—	—	µS
Pulse Width — CB1 Input Clock	T_{ICW}	2	—	—	µS
Pulse Spacing — PB6 Input Pulse	I_{IPS}	2	—	—	µS
Pulse Spacing — CB1 Input Pulse	I_{ICS}	2	—	—	µS

commodore semiconductor group

NMOS

MPS
6523
TRI-PORT
INTERFACE

6523 TRI-PORT INTERFACE

PERIPHERALS

CONCEPT . . .

The 6523 TRI-PORT Interface (TPI) is designed to simplify the implementation of complex I/O operations in microcomputer systems. It has three dedicated 8-bit I/O ports which provide 24 individually programmable I/O lines.

FEATURES:

- 24 individually programmable I/O lines
- Completely static operation
- Two TTL Drive Capability
- 6 directly addressable registers
- 1 MHz, 2MHz and 3MHz operation

6523 REGISTERS

*000	R0	PRA — Port Register A
001	R1	PRB — Port Register B
010	R2	PRC — Port Register C
011	R3	DDRA — Data Direction Register A
100	R4	DDRB — Data Direction Register B
101	R5	DDRC — Data Direction Register
110	}	Illegal States
111	}	Illegal States

*NOTE: RS2, RS1, RS0 respectively

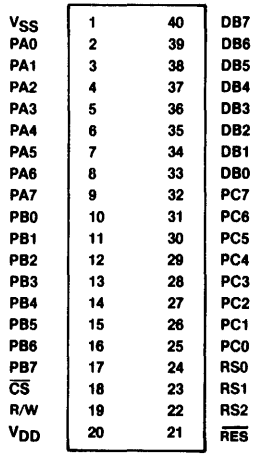
ORDER NUMBER:

MXS 6523

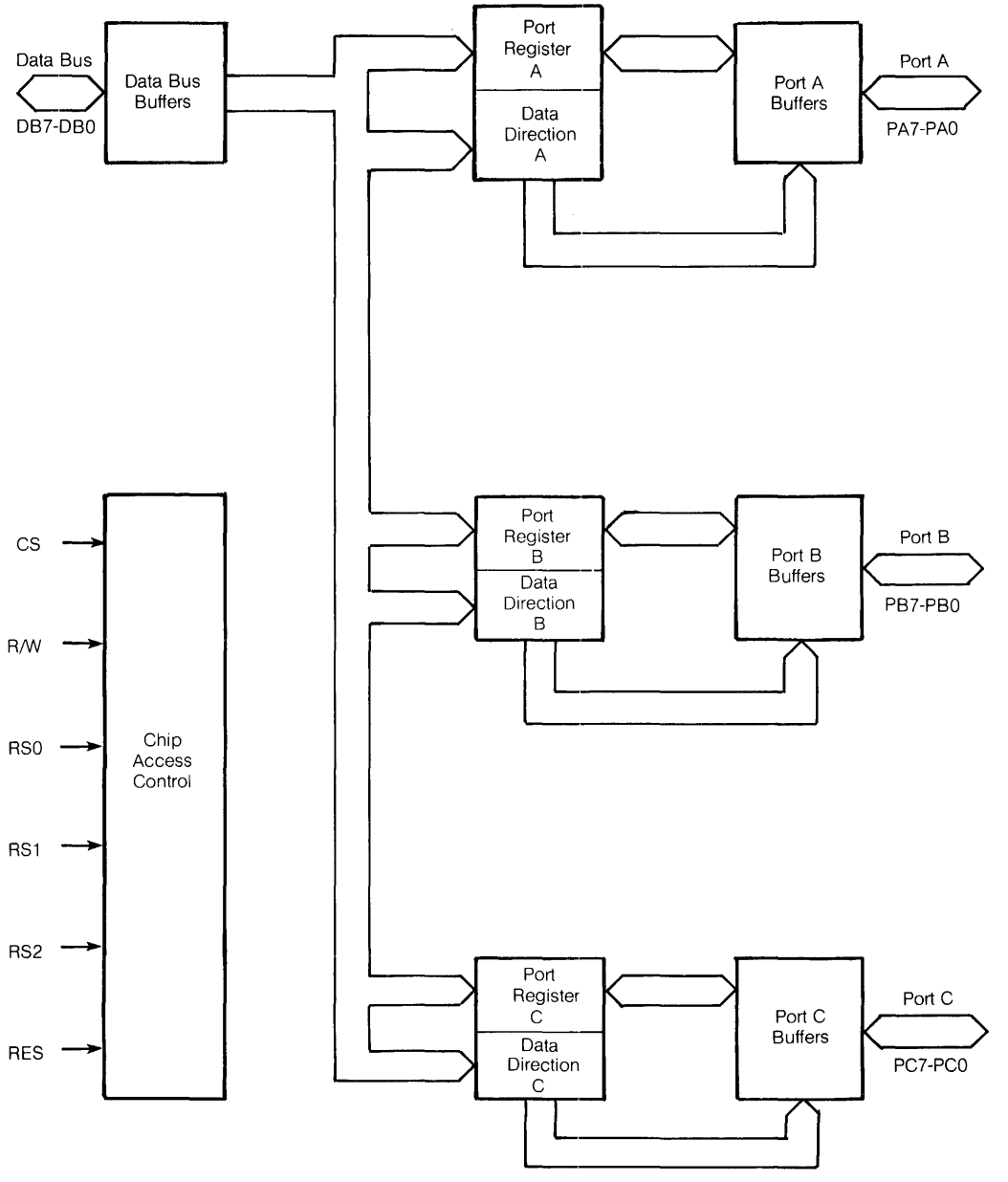
SPEED RANGE
NO SUFFIX = 450 ns
A = 225 ns
B = 165 ns

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

6523 PIN CONFIGURATION



6523 INTERNAL ARCHITECTURE



MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input/Output Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	−55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

COMMENT

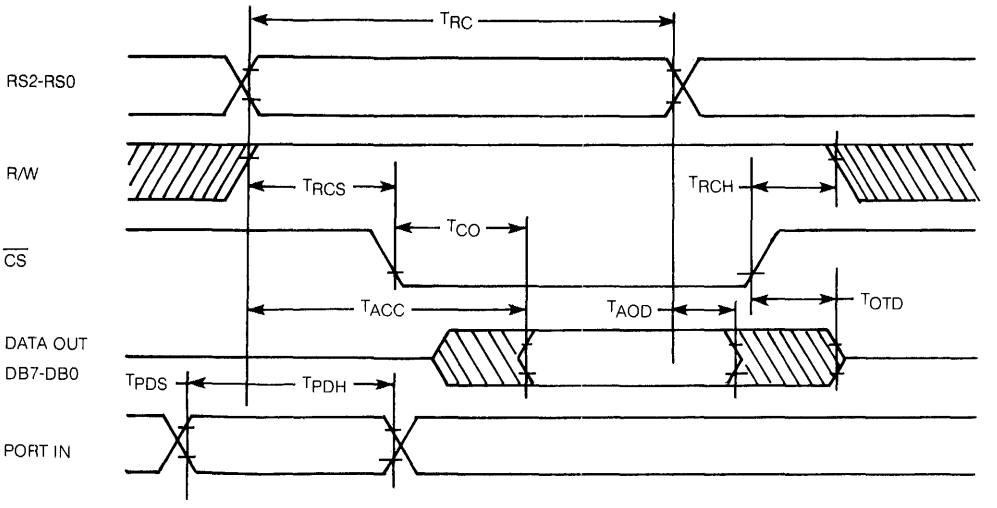
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0V, T_A = 0° to 70°C)

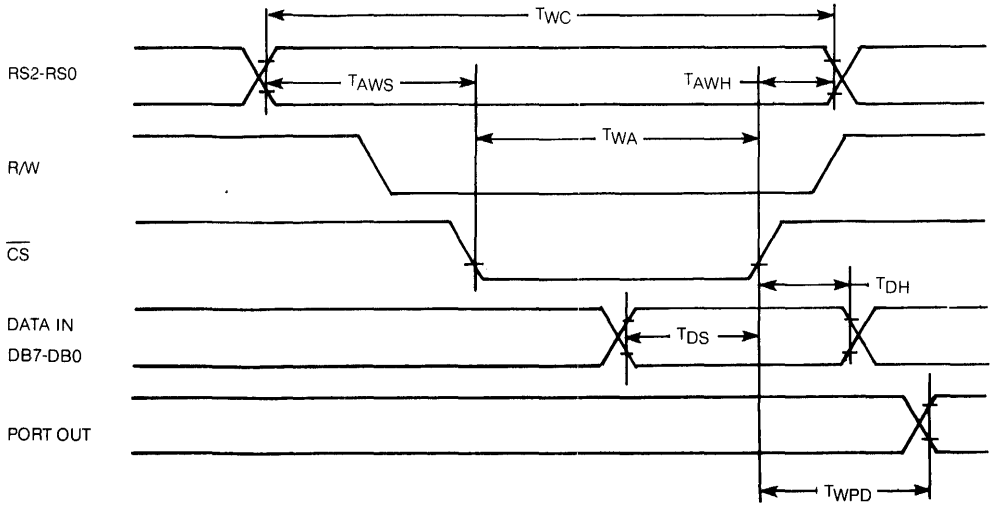
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Input High Voltage (Normal Operating Levels)	V_{IH}	+ 2.0		V_{CC}	V
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3		+0.8	V
Input Leakage Current (V_{in} = 0 to 5.0 V) WRITE, RES, CS, RS2-RS0	I_{IN}	0	± 1.0	± 2.5	μA
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 V V_{CC} = max) D0-D7, PA0-P7, PB0-PB7, PC0-PC7	I_{TSI}	0	± 2.0	± 10	μA
Output High Voltage (V_{CC} = min, Load = 200 μA)	V_{OH}	2.4	3.5	V_{CC}	V
Output Low Voltage (V_{CC} = min, Load = 3.2 mA)	V_{OL}	V_{SS}	0.2	0.4	V
Output High Current (Sourcing) (V_{OH} = 2.4 V)	I_{OH}	−200	−1000	—	μA
Output Low Current (Sinking) (V_{OL} = 0.4 V)	I_{OL}	3.2	—	—	mA
Supply Current	I_{CC}	—	50	100	mA
Input Capacitance (V_{in} 0V, T_A = 25°C, f = 1.0 MHz) D0-D7, PA0-PA7, PB0-PB7, PC0-PC7 WRITE, RES, RS2-RS0, CS	C_{in}	—	7	10	pF
Output Capacitance (V_{in} = 0V, T_A = 25°C, f = 1.0 MHz)	C_{out}	—	7	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

READ CYCLE



WRITE CYCLE



Note: All timings referenced to V_{IL}max, V_{IH} min on inputs and V_{OL} max, V_{OH} min on outputs.

READ CYCLE TIMING

SYMBOL	CHARACTERISTIC	6523		6523A		6523B		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
T_{RC}	Read Cycle	450	—	225	—	165	—	ns
T_{ACC}	Access Time[1]	—	450	—	225	—	165	ns
T_{CO}	$\overline{CS}$ to Output Valid	—	270	—	120	—	70	ns
T_{RCS}	R/W high to $\overline{CS}$ Setup	0	—	0	—	0	—	ns
T_{RCH}	R/W high to $\overline{CS}$ Hold	0	—	0	—	0	—	ns
T_{OTD}	$\overline{CS}$ to Output Off Delay	20	120	20	120	20	120	ns
T_{AOD}	Address to Output Delay	50	—	50	—	50	—	ns
T_{PDS}	Port Input Setup	120	—	60	—	40	—	ns
T_{PDH}	Port Input Hold	150	—	150	—	150	—	ns

Note 1: Access Time measured from later of $\overline{WRITE}$ high or RS stable.

WRITE CYCLE TIMING

SYMBOL	CHARACTERISTIC	6523		6523A		6523B		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
T_{WC}	Write Cycle	450	—	225	—	165	—	ns
T_{WA}	Write Active Time[2]	420	—	200	—	150	—	ns
T_{AWS}	Address to R/W low Setup	0	—	0	—	0	—	ns
T_{AWH}	Address to R/W low Hold	0	—	0	—	0	—	ns
T_{DS}	Data bus in Setup	150	—	100	—	50	—	ns
T_{DH}	Data bus in Hold	0	—	0	—	0	—	ns
T_{WPD}	Write active to Port out Delay	—	1000	—	500	—	330	ns

Note 2: T_{WA} is the time while both $\overline{CS}$ and R/W are low.

6523 FUNCTIONAL DESCRIPTION

Three 8 bit bi-directional ports (A, B, C) are available on the 6523. Each port has two associated read/write registers:

Data Direction Registers (DDRA, DDRB, DDRC)

Each bit of the data direction registers controls the corresponding pin of the associated port as follows:

DDR bit	Direction of port pin
0	Input (Output driver disabled)
1	Output (Output driver enabled)

Port Registers (PRA, PRB, PRC)

Reading the Port Register returns the logic states of the associated port pins. The pin voltage levels must meet the V_{IH} and V_{IL} specification limits to ensure valid data. (Excessive loading of the output driver may cause the data read to differ from the expected output.) If the port pin is programmed as an output by the DDR, the output driver is set to the last data written to the corresponding PR bit.

6523 INTERFACE SIGNALS

$\overline{CS}$ — Chip Select Input

The $\overline{CS}$ input controls the activity of the 6523. A low level on $\overline{CS}$ causes the device to respond to signals on the R/W and address (RS) lines. A high on $\overline{CS}$ prevents these lines from controlling the 6523. The $\overline{CS}$ line is normally activated (low) by the appropriate address combination from the processor.

R/W — Read/Write Input

The R/W signal is normally supplied by the microprocessor and controls the direction of data transfers of the 6523. A high on R/W indicates a read (data transfer out of the 6523), while a low indicates a write (data transfer into the 6523).

RS_2-RS_0 — Address Inputs

The address inputs select the internal registers (in conjunction with $\overline{CS}$ and R/W) as indicated by the register table.

DB7-DB0 — Data Bus Inputs/Outputs

The eight data bus pins transfer information between the 6523 and the system data bus. These pins are high impedance inputs unless $\overline{CS}$ is low and R/W is high, to read the device. During this read, the data bus output buffers are enabled, driving the data from the selected register onto the system data bus.

$\overline{RES}$ — Reset Input

A low on the RES pin clears internal registers. This sets all three ports as inputs (floating), preventing any conflicts on the bi-directional port lines. For port pins to be used as outputs, the desired output data may be written to the port register before enabling the output driver. This sequence can eliminate undesired output conditions when the outputs are enabled via the DDR.

commodore semiconductor group

NMOS

MPS
65245
OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

65245 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

DESCRIPTION

The 65245 is an octal bus transceiver designed for asynchronous, bi-directional communication between data busses.

The level of the Direction input (DIR) allows data transmission from bus A to bus B or from bus B to bus A. The Enable input ($\overline{E}$) can be used to provide isolation between the busses.

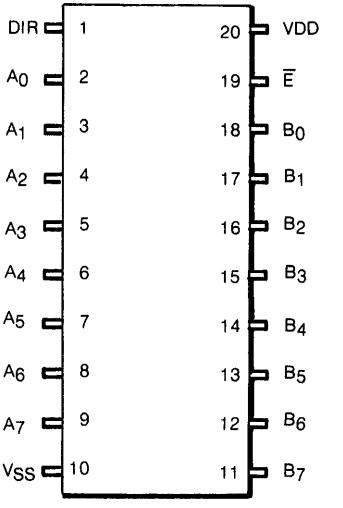
The device is fully TTL and CMOS compatible, and is pin-for-pin compatible with the 74LS245.

TRUTH TABLE

$\overline{E}$	DIR	OUTPUT
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

L = LOW level
H = HIGH level
X = Irrelevant

PIN CONFIGURATION 65245



MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	Vcc	−0.3 to +7.0	Vdc
INPUT VOLTAGE	Vin	−0.3 to +7.0	Vdc
OPERATING TEMPERATURE	T_A	0 to +70	°C
STORAGE TEMPERATURE	T_{STG}	−55 to +150	°C

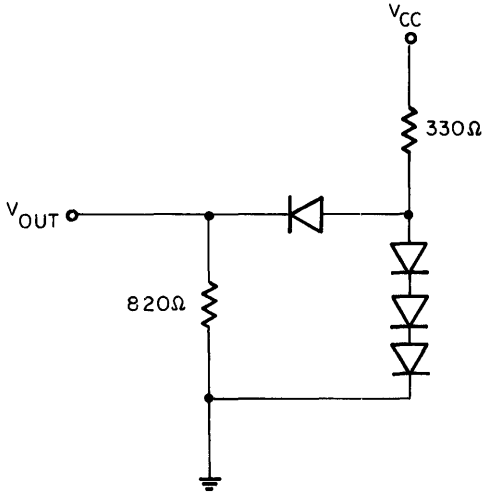
This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, Vss = 0, T_A = 0° to + 70°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	VIH	2.0	—	—	Vdc
Input Low Voltage	VIL	—	—	0.8	Vdc
Output High Voltage Vcc=MIN, VIH=2.0V IOH= −3mA IOH= −15mA	VOH	 2.4 2.0	 — —	 — —	Vdc
Output Low Voltage Vcc=MIN, VIL = 0.8V IOL = 12mA IOL = 24mA	VOL	—	— —	0.4 0.5	Vdc
High-Impedance Output Current $\overline{E}$ = 2.0V, Vcc = MAX V_{out} = 2.7V	IOZH	—	—	50	µA
High-Impedance Output Current $\overline{E}$ = 2.0V, Vcc = MAX V_{out} = 0.4V	IOZL	—	—	−50	µA
High-Level Input Current Vcc=MAX, VIH = 2.7V	IIH	—	20	100	nA
Low-Level Input Current Vcc = MAX, VIL = 0.4V	IIL	—	20	−100	nA
High-Level Output Current Vcc=NOM, V_{out} = 2.4V	IOH	—	—	−15	mA
Low-Level Output Current Vcc = NOM, V_{out} = 0.4V	IOL	—	—	24	mA
Power Supply Current Outputs High Outputs Low Outputs Hi-Z	ICC	—	 47 44 56	 64 100 105	mA

AC CHARACTERISTICS (VCC=5.0V, VSS=OV, T_A=+25°C)

CHARACTERISTIC	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Propagation Delay Data to Output	TPLH TPHL	SEE BELOW	— —	— —	40 40	ns ns
Output Enable Time	TPZH TPZL		— —	— —	40 40	ns ns
Output Disable Time	TPHZ TPLZ		— —	— —	40 40	ns ns



commodore semiconductor group

NMOS

MPS
6525
TRI-PORT
INTERFACE

6525 TRI-PORT INTERFACE

PERIPHERALS

CONCEPT . . .

The 6525 TRI-PORT Interface (TPI) is designed to simplify the implementation of complex I/O operations in microcomputer systems. It combines two dedicated 8-bit I/O ports with a third 8-bit port programmable for either normal I/O operation or priority interrupt/handshaking control. Depending on the mode selected, the 6525 can provide 24 individually programmable I/O lines or 16 I/O lines, 2 handshake lines and 5 priority interrupt inputs.

FEATURES:

- 24 individually programmable I/O lines or 16 I/O lines, 2 handshake lines and 5 interrupt inputs.
- Priority or non-priority interrupts
- Automatic handshaking
- Completely static operation
- Two TTL Drive Capability
- 8 directly addressable registers
- 1 MHz, 2MHz and 3MHz operation

6525 REGISTERS

*000	R0	PRA – Port Register A
001	R1	PRB – Port Register B
010	R2	PRC – Port Register C
011	R3	DDRA – Data Direction Register A
100	R4	DDRB – Data Direction Register B
101	R5	DDRC – Data Direction Register C
110	R6	CR – Control Register
111	R7	AIR – Active Interrupt Register

*NOTE: RS2, RS1, RS0 respectively

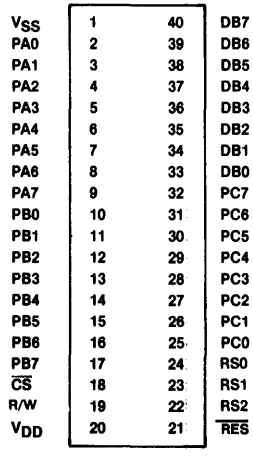
ORDER NUMBER:

MXS 6525 ____

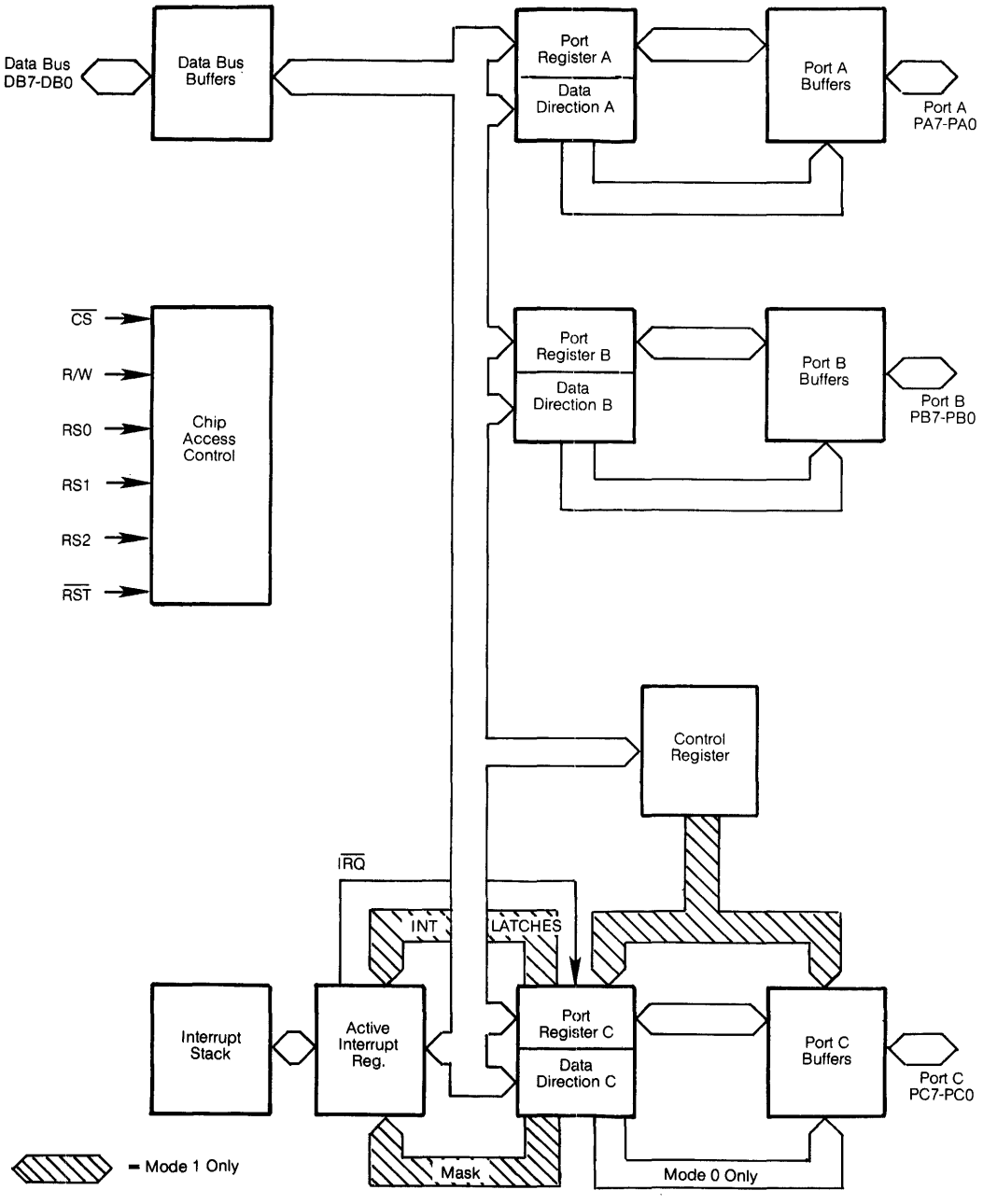
SPEED RANGE
NO SUFFIX = 450 ns
A = 225 ns
B = 155 ns

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

6525 PIN CONFIGURATION



6525 INTERNAL ARCHITECTURE



MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input/Output Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	−55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

COMMENT

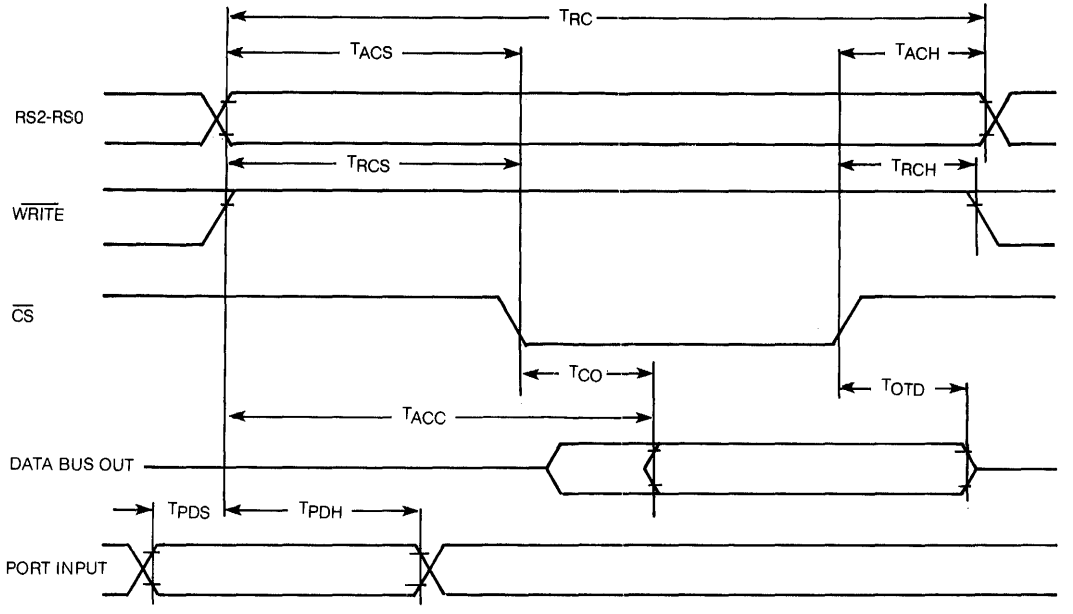
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0V, T_A = 0° to 70°C)

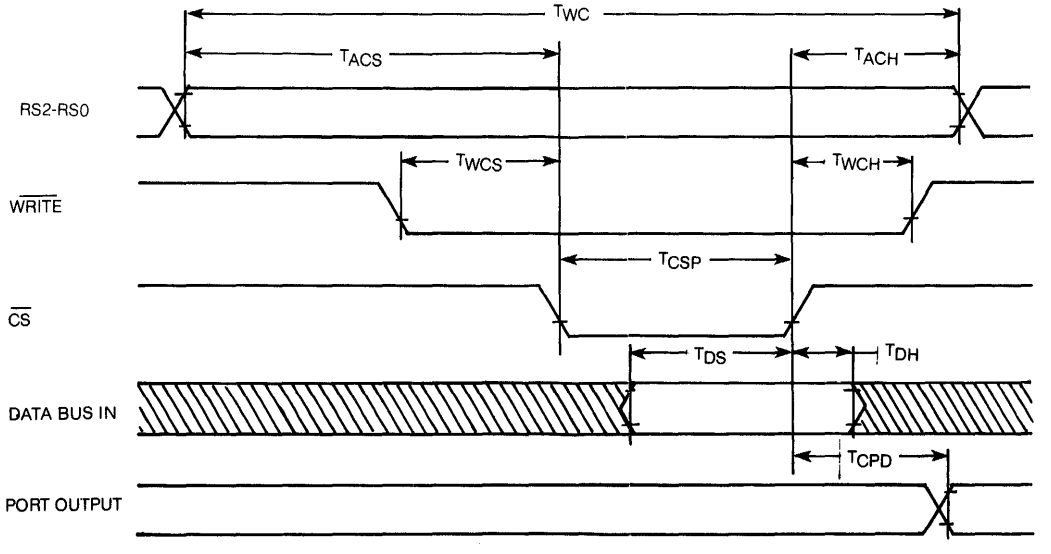
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Input High Voltage (Normal Operating Levels)	V_{IH}	+ 2.0	1.5	V_{CC}	V
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	1.2	+0.8	V
Input Leakage Current V_{in} = 0 to 5.0 V $\overline{WRITE}$, $\overline{RES}$, $\overline{CS}$, RS2-RS0	I_{IN}	0	± 1.0	± 2.5	μA
Three-State (Off-State) Input Current (V_{in} = 0.4 to 2.4 V V_{CC} = max) D0-D7, PA0-P7, PB0-PB7, PC0-PC7	I_{TSI}	0	± 2.0	± 10	μA
Output High Voltage (V_{CC} = min, Load = 200 μA)	V_{OH}	2.4	3.5	V_{CC}	V
Output Low Voltage (V_{CC} = min, Load = 3.2 mA)	V_{OL}	V_{SS}	0.2	0.4	V
Output High Current (Sourcing) (V_{OH} = 2.4 V)	I_{OH}	−200	−1000	—	μA
Output Low Current (Sinking) (V_{OL} = 0.4 V)	I_{OL}	3.2	—	—	mA
Supply Current	I_{CC}	—	50	100	mA
Input Capacitance (V_{in} 0V, T_A = 25°C, f = 1.0 MHz) D0-D7, PA0-PA7, PB0-PB7, PC0-PC7 $\overline{WRITE}$, $\overline{RES}$, RS2-RS0, $\overline{CS}$	C_{in}	—	7	10	pF
Output Capacitance (V_{in} = 0V, T_A = 25°C, f = 1.0 MHz)	C_{out}	—	7	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

READ CYCLE TIMING



WRITE CYCLE TIMING



Note: All timings referenced to V_{IL} max, V_{IH} min on inputs and V_{OL} max, V_{OH} min on outputs.

READ CYCLE TIMING

Symbol	Characteristic	6525		6525A		6525B		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
T_{RC}	Read Cycle	450	—	225	—	165	—	ns
T_{ACC}	Access Time[1]	—	450	—	225	—	155	ns
T_{CO}	$\overline{CS}$ to Output Valid	—	270	—	120	—	70	ns
T_{ACS}	RS to $\overline{CS}$ Set Up	0	—	0	—	0	—	ns
T_{ACH}	RS to $\overline{CS}$ Hold	0	—	0	—	0	—	ns
T_{RCS}	R/W high to CS Set Up	0	—	0	—	0	—	ns
T_{RCH}	R/W high to $\overline{CS}$ Hold	0	—	0	—	0	—	ns
T_{OTD}	$\overline{CS}$ to Output off Delay	20	120	20	120	20	100	ns
T_{PDS}	Port Input Set Up	120	—	60	—	40	—	ns
T_{PDH}	Port Input Hold	150	—	150	—	150	—	ns

NOTE 1 — Access time measured from later of R/W high or RS stable.

WRITE CYCLE TIMING

Symbol	Characteristic	6525		6525A		6525B		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
T_{WC}	Write Cycle	450	—	225	—	165	—	ns
T_{ACS}	RS to $\overline{CS}$ Set Up	0	—	0	—	0	—	ns
T_{ACH}	RS to $\overline{CS}$ Hold	0	—	0	—	0	—	ns
T_{WCS}	R/W low to $\overline{CS}$ Set Up	0	—	0	—	0	—	ns
T_{WCH}	R/W low to $\overline{CS}$ Hold	0	—	0	—	0	—	ns
T_{DS}	Data Bus to $\overline{CS}$ Set Up	150	—	100	—	50	—	ns
T_{DH}	Data Bus to $\overline{CS}$ Hold	0	—	0	—	0	—	ns
T_{CPD}	$\overline{CS}$ to Port Out Delay	—	1000	—	500	—	330	ns
T_{CSP}	$\overline{CS}$ Pulse Width	420	—	200	—	150	—	ns

6525 INTERNAL REGISTERS

ADDRESS				REGISTER BITS								REGISTER NAME	COMMENT
RS2	RS1	RS0	MC	D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	X	PA_7	PA_6	PA_5	PA_4	PA_3	PA_2	PA_1	PA_0	Port Register A (PRA)	
0	0	1	X	PB_7	PB_6	PB_5	PB_4	PB_3	PB_2	PB_1	PB_0	Port Register B (PRB)	
0	1	0	0	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	Port Register C (PRC)	
0	1	0	1	CB	CA	$\overline{IRQ}$	IL_4	IL_3	IL_2	IL_1	IL_0	Port Register C (PRC)	Handshake and Interrupt Latches (MODE 1)
0	1	1	X	DA_7	DA_6	DA_5	DA_4	DA_3	DA_2	DA_1	DA_0	Data Direction Register A (DDRA)	0=Input; 1=Output
1	0	0	X	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Data Direction Register B (DDRB)	0=Input; 1=Output
1	0	1	0	DC_7	DC_6	DC_5	DC_4	DC_3	DC_2	DC_1	DC_0	Data Direction Register C (DDRC)	0=Input; 1=Output (MODE 0)
1	0	1	1	—	—	—	M_4	M_3	M_2	M_1	M_0	Interrupt Mask Register	0=Mask; 1=Enable (MODE 1)
1	1	0	X	CB_1	CB_0	CA_1	CA_0	IE_4	IE_3	IP	MC	Control Register (CR)	Mode Selected by MC
1	1	1	1	—	—	—	AI_4	AI_3	AI_2	AI_1	AI_0	Active Interrupt Register (AIR)	

6525 FUNCTIONAL DESCRIPTION

Control Register (CR)

The bits of the control register select the various operating modes of the 6525. Although the exact function of each bit is explained throughout the functional description, the functions are summarized here for convenience.

CONTROL REGISTER BIT	7	6	5	4	3	2	1	0
FUNCTIONAL DESIGNATION	CB_1	CB_0	CA_1	CA_0	IE_4	IE_3	IP	MC

CB Line Control
CA Line Control
I4 Active Edge Select
I3 Active Edge Select
Interrupt Priority Enable
Mode Control

MODE 0 — (MC=0)

In Mode 0, three 8 bit bi-directional ports (A, B, C) are available on the 6525. Each port has two associated read/write registers:

Data Direction Registers (DDRA, DDRB, DDRC)

Each bit of the data direction registers controls the corresponding pin of the associated port as follows:

DDR bit	Direction of port pin
0	Input (Output driver disabled)
1	Output (Output driver enabled)

Port Registers (PRA, PRB, PRC)

Reading the Port Register returns the logic states of the associated port pins. The pin voltage levels must meet the V_{IH} and V_{IL} specification limits to ensure valid data. (Excessive loading of the output driver may cause the data read to differ from the expected output.) If the port pin is programmed as an output by the DDR, the output driver is set to the last data written to the corresponding PR bit.

MODE 1 — (MC=1)

In Mode 1, the 6525 provides 2 8-bit bi-directional ports (A and B) as in Mode 0. By writing MC=1, Port C is automatically converted to a 5 level priority interrupt controller with interrupt output ($\overline{IRQ}$) and a handshake control line for each port (CA and CB).

MODE 0 PIN NAMES	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
MODE 1 PIN NAMES	CB	CA	$\overline{IRQ}$	I4	I3	I2	I1	I0

Port Register C — PRC (Mode 1)

All bits of the PRC can be read as in Mode 0 but the state of the interrupt latches, rather than the interrupt pins, is returned in the five low order bits of PRC. Writing "0" to a PRC bit clears the corresponding interrupt latch but has no effect on the CA, CB, or $\overline{IRQ}$ outputs. Writing "1" to a PRC bit has no effect on Mode 1.

MODE 0 BIT NAMES	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0
MODE 1 BIT NAMES	CB	CA	$\overline{IRQ}$	IL_4	IL_3	IL_2	IL_1	IL_0

CA and CB Outputs — (PC6 and PC7)

CA and CB may be used as general purpose outputs or as data transfer signals for ports A and B. The operation of CA and CB is selected as follows:

CA_1	CA_0	CA OUTPUT MODE	CB_1	CB_0	CB OUTPUT MODE
0	0	Set high by active transition of I3. Reset low by reading PRA	0	0	Set low by writing PRB. Reset high by active transition of I4.
0	1	Pulses low for at least 500 ns after reading PRA.	0	1	Pulses low for at least 500 ns after writing PRB.
1	0	CA low	1	0	CB low
1	1	CA high	1	1	CB high

$\overline{IRQ}$ Output — (PC5)

The Interrupt Request is set low when an unmasked interrupt (see below) is activated. $\overline{IRQ}$ is reset high by reading the Active Interrupt Register (AIR). The $\overline{IRQ}$ output has an open drain to allow wire AND tying of multiple outputs.

I4, I3, I2, I1, I0 Inputs — (PC4-PC0)

The five low order pins of Port C are interrupt inputs in Mode 1. A negative (high to low) transition on I2, I1 or I0 sets the corresponding latch in PRC to indicate an interrupt, while either transition of I3 or I4 can be selected to set its latch as follows:

IE3	I3 EDGE SELECTION	IE4	I4 EDGE SELECTION
0	I3 sets IL_3 latch on negative (hi—low) transition.	0	I4 sets IL_4 latch on negative transition.
1	I3 sets IL_3 latch as positive (low—hi) transition.	1	I4 sets IL_4 latch on positive transition.

Interrupt Mask Register (DDRC in Mode 1)

In Mode 1, the five low order bits of the DDRC are utilized as interrupt mask bits of the five corresponding interrupt latches. Writing a "1" to the mask register enables the corresponding interrupt latch to initiate an interrupt while a "0" masks the interrupt latch output. Masking does not prevent the interrupt latch from being set by an active input transition. The interrupt mask register can be read and written.

Active Interrupt Register (AIR)

The five low order bits of the AIR contain the present interrupt status of the 6525. A "1" in a bit of the AIR indicates that the corresponding interrupt is active. Reading the AIR clears all AIR bits and resets any interrupt latch which had set a bit in the AIR. READING AND WRITING OF THE AIR AFFECTS THE INTERRUPT PRIORITY STACK. Therefore, the AIR should be accessed only in strict accordance to the following rules:

1. READ THE AIR ONLY TO INDICATE BEGINNING OF INTERRUPT SERVICE.
2. WRITE THE AIR ONLY TO INDICATE CONCLUSION OF INTERRUPT SERVICE.

DESCRIPTION OF PRIORITY INTERRUPT OPERATION

No Priority Operation Selected — (IP=0)

When an active transition occurs on an interrupt input (see I4-I0), the corresponding interrupt latch is set. If this latch is not masked, the corresponding bit of the AIR is set, $\overline{IRQ}$ (PC5) is activated low, and other interrupt latches are prevented from setting new bits in the AIR. After reading the AIR, the interrupt latch corresponding with the bit set in the AIR is cleared to await new input and $\overline{IRQ}$ is reset high. Any interrupt latches remaining set will now restart this interrupt sequence. If multiple interrupts have been received in the interim, multiple bits will be set in the AIR and all corresponding interrupt latches will be cleared when the AIR is read. Therefore, software must recognize the occurrence of multiple interrupts when no priority operation is selected.

Priority Operation Selected — (IP=1)

The five interrupt inputs have a fixed priority: I4 > I3 > I2 > I1 > I0. When priority operation is selected, only the highest priority interrupt is placed in the AIR, ensuring only one bit set in the AIR at any time. When an interrupt occurs, the corresponding interrupt latch is set as before but is then compared with the present active interrupt, the new bit in the AIR is set and $\overline{IRQ}$ is activated low. When AIR is read, the contents of the AIR are pushed onto a 5 level stack for comparison with subsequent interrupts and AIR is cleared.

After servicing the new interrupt, the processor must write to the AIR (clearing the AIR) to instruct the 6525 that this interrupt service is complete. The previous interrupt status is then recalled (popped) to the top of the stack to be used for evaluating new interrupt inputs. Interrupts of lesser priority than the active interrupt are masked until all higher level interrupts are acknowledged and completed by the processor (as indicated by AIR reads and writes). When all higher priority interrupts have been serviced, the 6525 will allow a lower priority interrupt to indicate a new interrupt sequence.

The following examples illustrate the priority interrupt operation:

A. Single Interrupt
   1. Interrupt received by negative transition on I1.
   2. Interrupt latch 1 (IL_1) is set.
   3. Bit A_1 set in AIR.
   4. $\overline{IRQ}$ activated low.
   5. Processor responds by reading AIR to determine which interrupt occurred.
   6. AIR is pushed onto interrupt stack and latch 1 is cleared.
   7. AIR is cleared and $\overline{IRQ}$ reset high.
   8. Upon completion of service, processor writes to AIR.
   9. Interrupt stack is popped, restoring previous interrupt status.

PERIPHERALS

B. Lower priority interrupt received during active interrupt
   1. I1 received and latched.
   2. A_1 is set and $\overline{IRQ}$ activated low.
   3. Processor reads AIR to determine I1 is active.
   4. AIR pushed onto stack and IL_1 cleared.
   5. AIR cleared and $\overline{IRQ}$ reset high.
   6. Processor is servicing I1 while I0 occurs and sets IL_0.
   7. Interrupt stack prevents lower priority IL_0 from initiating a new interrupt.
   8. Upon completion of I1 service, processor writes to AIR, popping I1 interrupt out of stack.
   9. IL_0 is now permitted to initiate a new interrupt service.

C. Higher priority interrupt received during active interrupt
   1. Interrupt I1 received and latched.
   2. A_1 is set and $\overline{IRQ}$ activated low.
   3. Processor reads AIR to determine I1 is active.
   4. AIR is pushed onto stack and IL_1 cleared.
   5. AIR cleared and $\overline{IRQ}$ reset high.
   6. Processor is servicing I1 when I2 occurs and sets IL_2.
   7. A_2 is set and $\overline{IRQ}$ activated low because IL_2 has higher priority than I1 in stack.
   8. Processor recognizes interrupt request and calls interrupt service routine.
   9. Processor reads AIR to determine I2 is active.
   10. New AIR is pushed onto interrupt stack and IL_2 cleared.
   11. AIR cleared and $\overline{IRQ}$ reset high.
   12. Processor services I2.
   13. Upon completion of I2 service, processor writes to AIR popping I2 interrupt from stack, restoring I1 status to top of stack (still preventing an I0 interrupt).
   14. Processor return from interrupt resumes services of suspended I1 routine.
   15. Upon completion of I1, processor writes to AIR, popping I1 interrupt from stack, leaving no active interrupts.

6525 INTERFACE AND CONTROL

Initialization

A low on the $\overline{RES}$ pin clears all 6525 internal registers. This puts the 6525 in Mode 0 with all three ports selected as inputs (floating), preventing any conflicts on the bi-directional port lines. For port pins to be used as outputs, the desired output data may be written to the port register before enabling the output driver. This sequence can eliminate undesired output conditions when the outputs are enabled via the DDR.

When selecting Mode 1, all interrupt inputs and IE3, IE4 must be stable before writing MC bit to "1." If this can not be ensured, the interrupt latches (PRC_4-PRC_0) should be cleared by writing 0 to PRC after MC=1 and before unmasking the interrupt latches. Similarly, if CA and CB are to be used as data transfer handshake lines, no PRA reads or PRB writes should occur after RES or before actual data transfers are to begin.

Processor Interface

The 6525 is a fully static device with interface characteristics similar to a static RAM. To read, the RS and R/W lines are stabilized and then $\overline{CS}$ is switched low, gating the desired register onto the system data bus. (In 650X systems, $\overline{CS}$ may be gated with Ø2). The system timing must accommodate both the T_{ACC} (address) and T_{CO} (chip select) delays before requiring valid data. To write to the 6525, similar timing is required, with the processor providing valid write data at least $_{DS}$ before $\overline{CS}$ switches high. To guarantee proper operation of the 6525, THE R/W LINE MUST BE STABLE ANY TIME $\overline{CS}$ IS LOW.

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6526

COMPLEX INTERFACE ADAPTER (CIA)

6526 COMPLEX INTERFACE ADAPTER (CIA)

PERIPHERALS

DESCRIPTION

The 6526 Complex Interface Adapter (CIA) is a 65XX bus compatible peripheral Interface device with extremely flexible timing and I/O capabilities.

FEATURES

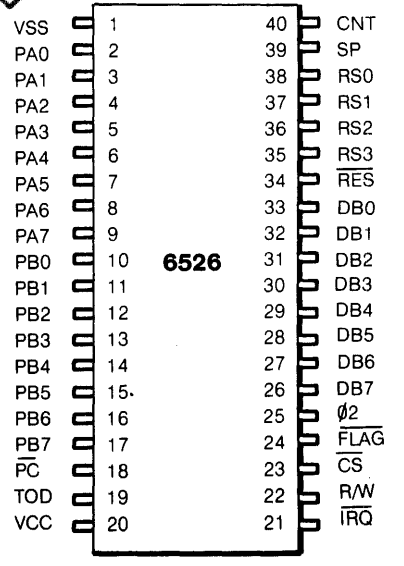
- 16 Individually programmable I/O lines
- 8 or 16-Bit handshaking on read or write
- 2 independent, linkable 16-Bit interval timers
- 24-hour (AM/PM) time of day clock with programmable alarm
- 8-Bit shift register for serial I/O
- 2TTL Load capability
- CMOS compatible I/O lines
- 1 or 2 MHz operation available

ORDERING INFORMATION

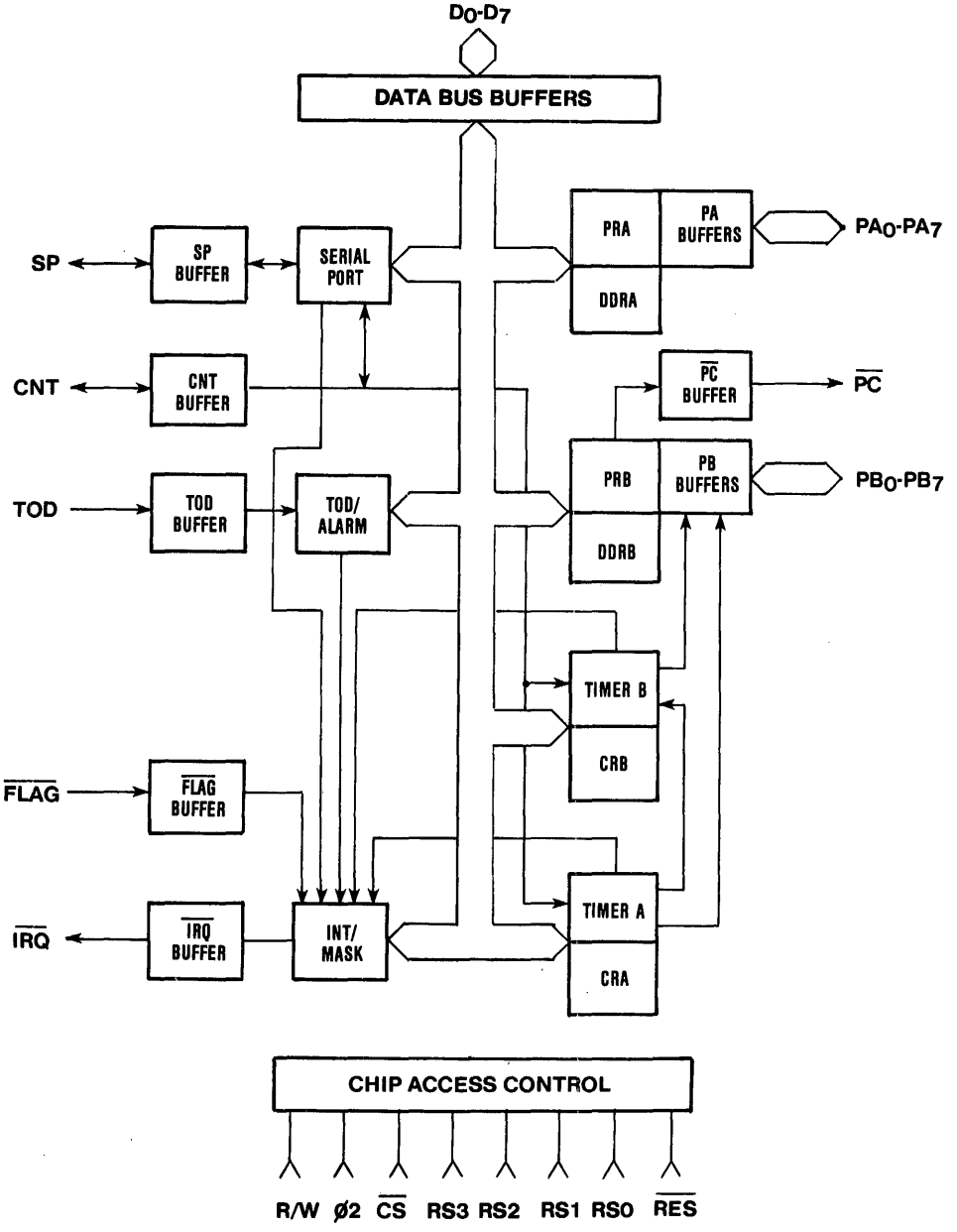
MXS 6526 ___

- FREQUENCY RANGE
  - NO SUFFIX = 1MHz
  - A = 2MHz
- PACKAGE DESIGNATOR
  - C = CERAMIC
  - P = PLASTIC

PIN CONFIGURATION



6526
BLOCK DIAGRAM



MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input/Output Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	−55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

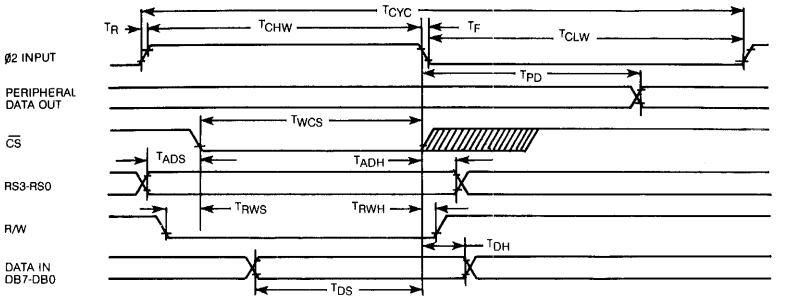
COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

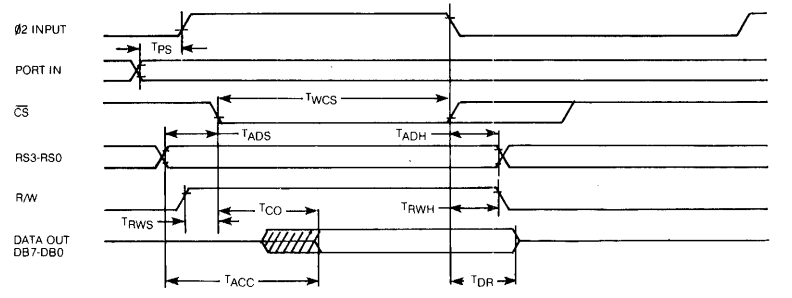
ELECTRICAL CHARACTERISTICS (V_{CC} ± 5%, VSS = 0v, T_A = 0-70°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	+ 2.4	—	V_{CC}	V
Input Low Voltage	V_{IL}	− 0.3	—	+0.8	V
Input Leakage Current; V_{IN} = V_{SS} + 5v (TOD, R/W, $\overline{FLAG}$, Ø2, $\overline{RES}$, RS0-RS3, $\overline{CS}$)	I_{IN}	—	1.0	2.5	μA
Port Input Pull-up Resistance	R_{PI}	3.1	5.0	—	KΩ
Output Leakage Current for High Impedance State (Three State); V_{IN} = 4v to 2.4v; (DB0-DB7, SP, CNT, $\overline{IRQ}$)	I_{TSI}	—	± 1.0	± 10.0	μA
Output High Voltage VCC=MIN, I_{LOAD} < −200μA (PA0-PA7, $\overline{PC}$ PB0-PB7, DB0-DB7)	V_{OH}	+ 2.4	—	V_{CC}	V
Output Low Voltage VCC = MIN, I_{LOAD} < 3.2mA	V_{OL}	—	—	+ 0.40	V
Output High Current (Sourcing); VOH > 2.4v (PA0-PA7, PB0-PB7, PC, DB0-DB7)	I_{OH}	−200	−1000	—	μA
Output Low Current (Sinking); VOL < .4 v (PA0-PA7, $\overline{PC}$, PB0-PB7, DB0-DB7)	I_{OL}	3.2	—	—	mA
Input Capacitance	C_{IN}	—	7	10	pf
Output Capacitance	C_{OUT}	—	7	10	pf
Power Supply Current	I_{CC}	—	70	100	mA

6526 WRITE TIMING DIAGRAM



6526 READ TIMING DIAGRAM



6526 INTERFACE SIGNALS

Ø2 — Clock Input

The Ø2 clock is a TTL compatible input used for internal device operation and as a timing reference for communicating with the system data bus.

CS — Chip Select Input

The CS input controls the activity of the 6526. A low level on CS while Ø2 is high causes the device to respond to signals on the R/W and address (RS) lines. A high on CS prevents these lines from controlling the 6526. The CS line is normally activated (low) at Ø2 by the appropriate address combination.

R/W — Read/Write Input

The R/W signal is normally supplied by the microprocessor and controls the direction of data transfers of the 6526. A high on R/W indicates a read (data transfer out of the 6526), while a low indicates a write (data transfer into the 6526).

RS3-RS0 — Address Inputs

The address inputs select the internal registers as described by the Register Map.

DB7-BD0 — Data Bus Inputs/Outputs

The eight data bus pins transfer information between the 6526 and the system data bus. These pins are high impedance inputs unless CS is low and R/W and Ø2 are high, to read the device. During this read, the data bus output buffers are enabled, driving the data from the selected register onto the system data bus.

IRQ — Interrupt Request Output

IRQ is an open drain output normally connected to the processor interrupt input. An external pullup resistor holds the signal high, allowing multiple IRQ outputs to be connected together. The IRQ output is normally off (high impedance) and is activated low as indicated in the functional description.

RES — Reset Input

A low on the RES pin resets all internal registers. The port pins are set as inputs and port registers to zero (although a read of the ports will return all highs because of passive pullups). The timer control registers are set to zero and the timer latches to all ones. All other registers are reset to zero.

6526 TIMING CHARACTERISTICS

Symbol	Characteristic	1MHz MIN	1MHz MAX	2MHz MIN	2MHz MAX	Unit
	ϕ_2 Clock					
T_{CYC}	Cycle Time	1,000	20,000	500	20,000	nS
T_R, T_F	Rise and Fall Time	—	25	—	25	nS
T_{CHW}	Clock Pulse Width (High)	420	10,000	200	10,000	nS
T_{CLW}	Clock Pulse Width (Low)	420	10,000	200	10,000	nS
	Write Cycle					
T_{PD}	Output Delay From ϕ_2	—	1,000	—	500	nS
T_{WCS}	$\overline{CS}$ low while ϕ_2 high	420	—	200	—	nS
T_{ADS}	Address Setup Time	0	—	0	—	nS
T_{ADH}	Address Hold Time	10	—	5	—	nS
T_{RWS}	R/W Setup Time	0	—	0	—	nS
T_{RWH}	R/W Hold Time	0	—	0	—	nS
T_{DS}	Data Bus Setup Time	150	—	75	—	nS
T_{DH}	Data Bus Hold Time	0	—	0	—	nS
	Read Cycle					
T_{PS}	Port Setup Time	300	—	150	—	nS
T_{WCS}(2)	$\overline{CS}$ low while ϕ_2 high	420	—	200	—	nS
T_{ADS}	Address Setup Time	0	—	0	—	nS
T_{ADH}	Address Hold Time	10	—	5	—	nS
T_{RWS}	R/W Setup Time	0	—	0	—	nS
T_{RWH}	R/W Hold Time	0	—	0	—	nS
T_{ACC}	Data Access from RS3-RS0	—	550	—	275	nS
T_{CO}(3)	Data Access from $\overline{CS}$	—	320	—	150	nS
T_{DR}	Data Release Time	50	—	25	—	nS

NOTES: 1 — All timings are referenced from V_{IL} max and V_{IH} min on inputs and V_{OL} max and V_{OH} min on outputs.
2 — T_{WCS} is measured from the later of ϕ2 high or $\overline{CS}$ low. $\overline{CS}$ must be low at least until the end of ϕ2 high.
3 — T_{CO} is measured from the later of ϕ2 high or $\overline{CS}$ low.
Valid data is available only after the later of T_{ACC} or T_{CO}.

REGISTER MAP

RS3	RS2	RS1	RS0	REG		
0	0	0	0	0	PRA	PERIPHERAL DATA REG A
0	0	0	1	1	PRB	PERIPHERAL DATA REG B
0	0	1	0	2	DDRA	DATA DIRECTION REG A
0	0	1	1	3	DDRB	DATA DIRECTION REG B
0	1	0	0	4	TA LO	TIMER A LOW REGISTER
0	1	0	1	5	TA HI	TIMER A HIGH REGISTER
0	1	1	0	6	TB LO	TIMER B LOW REGISTER
0	1	1	1	7	TB HI	TIMER B HIGH REGISTER
1	0	0	0	8	TOD 10THS	10THS OF SECONDS REGISTER
1	0	0	1	9	TOD SEC	SECONDS REGISTER
1	0	1	0	A	TOD MIN	MINUTES REGISTER
1	0	1	1	B	TOD HR	HOURS — AM/PM REGISTER
1	1	0	0	C	SDR	SERIAL DATA REGISTER
1	1	0	1	D	ICR	INTERRUPT CONTROL REGISTER
1	1	1	0	E	CRA	CONTROL REG A
1	1	1	1	F	CRB	CONTROL REG B

6526 FUNCTIONAL DESCRIPTION

I/O Ports (PRA, PRB, DDRA, DDRB)

Ports A and B each consist of an 8-bit Peripheral Data Register (PR) and an 8-bit Data Direction Register (DDR). If a bit in the DDR is set to a one, the corresponding bit in the PR is an output, if a DDR bit is set to a zero, the corresponding PR bit is defined as an input. On a READ, the PR reflects the information present on the actual port pins (PA0-PA7, PB0-PB7) for both input and output bits. Port A and Port B have passive pull-up devices as well as active pull-ups, providing both CMOS and TTL compatibility. Both ports have two TTL load drive capability. In addition to normal I/O operation, PB6 and PB7 also provide timer output functions.

Handshaking

Handshaking on data transfers can be accomplished using the $\overline{PC}$ output pin and the $\overline{FLAG}$ input pin. $\overline{PC}$ will go low for one cycle following a read or write of PORT B. This signal can be used to indicate "data ready" at PORT B or "data accepted" from PORT B. Handshaking on 16-bit data transfers (using both PORT A and PORT B) is possible by always reading or writing PORT A first. $\overline{FLAG}$ is a negative edge sensitive input which can be used for receiving the $\overline{PC}$ output from another 6526, or as a general purpose interrupt input. Any negative transition on $\overline{FLAG}$ will set the $\overline{FLAG}$ interrupt bit.

REG	NAME	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	PRA	PA_7	PA_6	PA_5	PA_4	PA_3	PA_2	PA_1	PA_0
1	PRB	PB_7	PB_6	PB_5	PB_4	PB_3	PB_2	PB_1	PB_0
2	DDRA	DPA_7	DPA_6	DPA_5	DPA_4	DPA_3	DPA_2	DPA_1	DPA_0
3	DDRB	DPB_7	DPB_6	DPB_5	DPB_4	DPB_3	DPB_2	DPB_1	DPB_0

Interval Timers (Timer A, Timer B)

Each interval timer consists of a 16-bit read-only Timer Counter and a 16-bit write-only Timer Latch. Data written to the timer are latched in the Timer Latch, while data read from the timer are the present contents of the Timer Counter. The timers can be used independently or linked for extended operations. The various timer modes allow generation of long time delays, variable width pulses, pulse trains and variable frequency waveforms. Utilizing the CNT input, the timers can count external pulses or measure frequency, pulse width and delay times of external signals. Each timer has an associated control register, providing independent control of the following functions:

Start/Stop
A control bit allows the timer to be started or stopped by the microprocessor at any time.

PB On/Off:
A control bit allows the timer output to appear on a PORT B output line (PB6 for TIMER A and PB7 for TIMER B). This function overrides the DDRB control bit and forces the appropriate PB line to an output.

Toggle/Pulse
A control bit selects the output applied to PORT B. On every timer underflow the output can either toggle or generate a single positive pulse of one cycle duration. The Toggle output is set high whenever the timer is started and is set low by $\overline{RES}$.

One-Short/Continuous
A control bit selects either timer mode. In one-shot mode, the timer will count down from the latched value to zero, generate an interrupt, reload the latched value, then stop. In continuous mode, the timer will count from the latched value to zero, generate an interrupt, reload the latched value and repeat the procedure continuously.

Force Load
A strobe bit allows the timer latch to be loaded into the timer counter at any time, whether the timer is running or not.

Input Mode:
Control bits allow selection of the clock used to decrement the timer. TIMER A can count Ø2 clock pulses or external pulses applied to the CNT pin. TIMER B can count Ø2 pulses, external CNT pulses, TIMER A underflow pulses or TIMER A underflow pulses while the CNT pin is held high.

The timer latch is loaded into the timer on any timer underflow, on a force load or following a write to the high byte of the prescaler while the timer is stopped. If the timer is running, a write to the high byte will load the timer latch, but not reload the counter.

READ (TIMER)

REG	NAME								
4	TA LO	TAL_7	TAL_6	TAL_5	TAL_4	TAL_3	TAL_2	TAL_1	TAL_0
5	TA HI	TAH_7	TAH_6	TAH_5	TAH_4	TAH_3	TAH_2	TAH_1	TAH_0
6	TB LO	TBL_7	TBL_6	TBL_5	TBL_4	TBL_3	TBL_2	TBL_1	TBL_0
7	TB HI	TBH_7	TBH_6	TBH_5	TBH_4	TBH_3	TBH_2	TBH_1	TBH_0

WRITE (PRESCALER)

REG	NAME								
4	TA LO	PAL_7	PAL_6	PAL_5	PAL_4	PAL_3	PAL_2	PAL_1	PAL_0
5	TA HI	PAH_7	PAH_6	PAH_5	PAH_4	PAH_3	PAH_2	PAH_1	PAH_0
6	TB LO	PBL_7	PBL_6	PBL_5	PBL_4	PBL_3	PBL_2	PBL_1	PBL_0
7	TB HI	PBH_7	PBH_6	PBH_5	PBH_4	PBH_3	PBH_2	PBH_1	PBH_0

Time of Day Clock (TOD)

The TOD clock is a special purpose timer for real-time applications. TOD consists of a 24-hour (AM/PM) clock with 1/10th second resolution. It is organized into 4 registers: 10ths of seconds, Seconds, Minutes and Hours. The AM/PM flag is in the MSB of the Hours register for easy bit testing. Each register reads out in BCD format to simplify conversion for driving displays, etc. The clock requires an external 60 Hz or 50 Hz (programmable) TTL level input on the TOD pin for accurate time-keeping. In addition to time-keeping, a programmable ALARM is provided for generating an interrupt at a desired time. The ALARM registers are located at the same addresses as the corresponding TOD registers. Access to the ALARM is governed by a Control Register bit. The ALARM is write-only; any read of a TOD address will read time regardless of the state of the ALARM access bit.

A specific sequence of events must be followed for proper setting and reading of TOD. TOD is automatically stopped whenever a write to the Hours register occurs. The clock will not start again until after a write to the 10ths of seconds register. This assures TOD will always start at the desired time. Since a carry

from one stage to the next can occur at any time with respect to a read operation, a latching function is included to keep all Time Of Day information constant during a read sequence. All four TOD registers latch on a read of Hours and remain latched until after a read of 10ths of seconds. The TOD clock continues to count when the output registers are latched. If only one register is to be read, there is no carry problem and the register can be read "on the fly," provided that any read of Hours is followed by a read of 10ths of seconds to disable the latching.

READ

REG	NAME								
8	TOD 10THS	0	0	0	0	T_8	T_4	T_2	T_1
9	TOD SEC	0	SH_4	SH_2	SH_1	SL_8	SL_4	SL_2	SL_1
A	TOD MIN	0	MH_4	MH_2	MH_1	ML_8	ML_4	ML_2	ML_1
B	TOD HR	PM	0	0	HH	HL_8	HL_4	HL_2	HL_1

WRITE
CRB_7=0 TOD
CRB_7=1 ALARM
(SAME FORMAT AS READ)

Serial Port (SDR)

The serial port is a buffered, 8-bit synchronous shift register system. A control bit selects input or output mode. In input mode, data on the SP pin is shifted into the shift register on the rising edge of the signal applied to the CNT pin. After 8 CNT pulses, the data in the shift register is dumped into the Serial Data Register and an interrupt is generated. In the output mode, TIMER A is used for the baud rate generator. Data is shifted out on the SP pin at ½ the underflow rate of TIMER A. The maximum baud rate possible is Ø2 divided by 4, but the maximum useable baud rate will be determined by line loading and the speed at which the receiver responds to input data. Transmission will start following a write to the Serial Data Register (provided TIMER A is running and in continuous mode). The clock signal derived from TIMER A appears as an output on the CNT pin. The data in the Serial Data Register will be loaded into the shift register then shift out to the SP pin when a CNT pulse occurs. Data shifted out becomes valid on the falling edge of CNT and remains valid until the next falling edge. After 8 CNT pulses, an interrupt is generated to indicate more data can be sent. If the Serial Data Register was loaded with new information prior to this interrupt, the new data will automatically be loaded into the shift register and transmission will continue. If the microprocessor stays one byte ahead of the shift register, transmission will be continuous. If no further data is to be transmitted, after the 8th CNT pulse, CNT will return high and SP will remain at the level of the last data bit transmitted. SDR data is shifted out MSB first and serial input data should also appear in this format.

The bidirectional capability of the Serial Port and CNT clock allows many 6526 devices to be connected to a common serial communication bus on which one 6526 acts as a master, sourcing data and shift clock, while all other 6526 chips act as slaves. Both CNT and SP outputs are open drain to allow such a common bus. Protocol for master/slave selection can be transmitted over the serial bus, or via dedicated handshaking lines.

REG	NAME								
C	SDR	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Interrupt Control (ICR)

There are five sources of interrupts on the 6526: underflow from TIMER A, underflow from TIMER B, TOD ALARM, Serial Port full/empty and $\overline{FLAG}$. A single register provides masking and interrupt information. The Interrupt Control Register consists of a write-only MASK register and a read-only DATA register. Any interrupt will set the corresponding bit in the DATA register. Any interrupt which is enabled by the MASK register will set the IR bit (MSB) of the DATA register and bring the $\overline{IRQ}$ pin low. In a multi-chip system, the IR bit can be polled to detect which chip has generated an interrupt request. The interrupt DATA register is cleared and the $\overline{IRQ}$ line returns high following a read of the DATA register. Since each interrupt sets an interrupt bit regardless of the MASK, and each interrupt bit can be selectively masked to prevent the generation of a processor interrupt, it is possible to intermix polled interrupts with true interrupts. However, polling the IR bit will cause the DATA register to clear, therefore, it is up to the user to preserve the information contained in the DATA register if any polled interrupts were present.

The MASK register provides convenient control of individual mask bits. When writing to the MASK register, if bit 7 (SET/$\overline{CLEAR}$) of the data written is a ZERO, any mask bit written with a one will be cleared, while those mask bits written with a zero will be unaffected. If bit 7 of the data written is a ONE, any mask bit written with a one will be set, while those mask bits written with a zero will be unaffected. In order for an interrupt flag to set IR and generate an Interrupt Request, the corresponding MASK bit must be set.

READ (INT DATA)

REG	NAME								
D	ICR	IR	0	0	FLG	SP	ALRM	TB	TA

WRITE (INT MASK)

REG	NAME								
D	ICR	S/$\overline{C}$	X	X	FLG	SP	ALRM	TB	TA

PERIPHERALS

CONTROL REGISTERS

There are two control registers in the 6526, CRA and CRB. CRA is associated with TIMER A and CRB is associated with TIMER B. The register format is as follows:

CRA:

Bit	Name	Function
0	START	1=START TIMER A, 0=STOP TIMER A. This bit is automatically reset when underflow occurs during one-shot mode.
1	PBON	1=TIMER A output appears on PB6, 0=PB6 normal operation.
2	OUTMODE	1=TOGGLE, 0=PULSE
3	RUNMODE	1=ONE-SHOT, 0=CONTINUOUS
4	LOAD	1=FORCE LOAD (this is a STROBE input, there is no data storage, bit 4 will always read back a zero and writing a zero has no effect).
5	INMODE	1=TIMER A counts positive CNT transitions, 0=TIMER A counts Ø2 pulses.
6	SPMODE	1=SERIAL PORT output (CNT sources shift clock), 0=SERIAL PORT input (external shift clock required).
7	TODIN	1=50 Hz clock required on TOD pin for accurate time, 0=60 Hz clock required on TOD pin for accurate time.

CRB:

Bit	Name	Function
		(Bits CRB0-CRB4 are identical to CRA0-CRA4 for TIMER B with the exception that bit 1 controls the output of TIMER B on PB7).
5,6	INMODE	Bits CRB5 and CRB6 select one of four input modes for TIMER B as: CRB6 CRB5 0 0 TIMER B counts Ø2 pulses. 0 1 TIMER B counts positive CNT transistions. 1 0 TIMER B counts TIMER A underflow pulses. 1 1 TIMER B counts TIMER A underflow pulses while CNT is high.
7	ALARM	1=writing to TOD registers sets ALARM, 0=writing to TOD registers sets TOD clock.

REG	NAME	TOD IN	SP MODE	IN MODE	LOAD	RUN MODE	OUT MODE	PB ON	START
E	CRA	0=60Hz	0=INPUT	0=Ø2	1=FORCE LOAD	0=CONT.	0=PULSE	0=PB6 OFF	0=STOP
		1=50Hz	1=OUTPUT	1=CNT	(STROBE)	1=O.S.	1=TOGGLE	1=PB6 ON	1=START

TA

REG	NAME	ALARM	IN MODE		LOAD	RUN MODE	OUT MODE	PB ON	START
F	CRB	0=TOD	0	0=Ø2	1=FORCE LOAD	0=CONT.	0=PULSE	0=PB7 OFF	0=STOP
			0	1=CNT					
			1	0=TA					
		1= ALARM	1	1=CNT•TA	(STROBE)	1=O.S.	1=TOGGLE	1=PB7 ON	1=START

TB

All unused register bits are unaffected by a write and are forced to zero on a read.

commodore semiconductor group

NMOS

MPS
6529
SINGLE-PORT
INTERFACE

6529 SINGLE PORT INTERFACE

PERIPHERALS

DESCRIPTION

The 6529 is a static microprocessor compatible, 8-bit I/O Port with passive output pull-up devices. Data is written to the port when $\overline{CS}$ and R/W are low. Data is read from the port when $\overline{CS}$ is low and R/W is high. The passive output pull-ups allow a single bit to act as either an input or an output without I/O mode switching.

This device is provided with special circuitry to provide power-on reset. Under normal fast power-on conditions the outputs will initialize in the input high impedance state. With very slow or noisy power-up, there is some possibility the device will initialize with outputs driven low. It is recommended that the 6529 be interfaced to open collector output type devices.

TRUTH TABLE

CS	R/W	D_0-D_7
L	L	DATA BUS TO PORT
L	H	PORT TO DATA BUS
H	X	ISOLATION

L = LOW Level
H = HIGH Level
X = Irrelevant

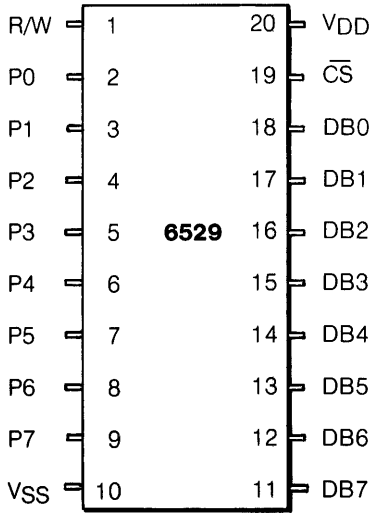
ORDER INFORMATION

MXS 6529 ___

FREQUENCY RANGE
NO SUFFIX = 1 MHz
A = 2 MHz
B = 3 MHz

PACKAGE DESIGNATOR
C = Ceramic
P = Plastic

PIN CONFIGURATION



MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	V_{CC}	−0.3 to +7.0	Vdc
INPUT VOLTAGE	V_{in}	−0.3 to +7.0	Vdc
OPERATING TEMPERATURE RANGE	T_A	0 to + 70	°C
STORAGE TEMPERATURE RANGE	T_{stg}	−55 to +150	°C

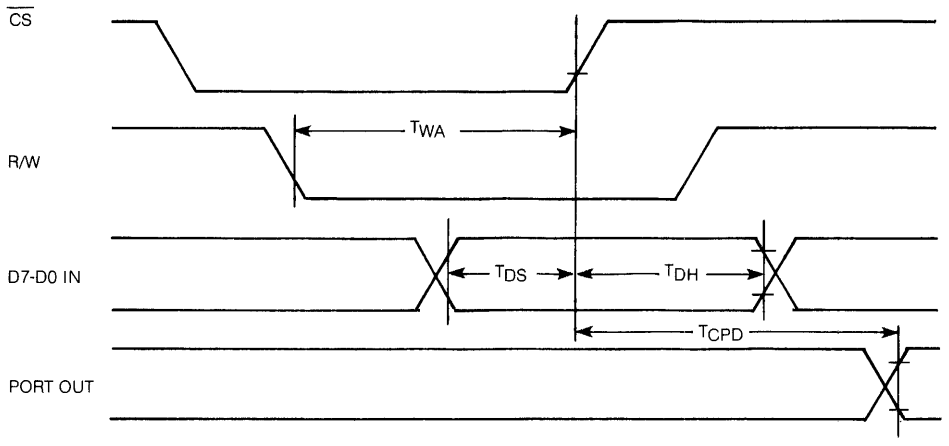
This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0V, T_A = 0° to 70°C)

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	+0.8	Vdc
Input Leakage Current V_{in} = 0 to 5.0Vdc $\overline{WRITE}$, $\overline{CS}$	I_{IN}	—	±2.5	μAdc
Three-State (Off State Input Current) (V_{in} = 0.4 to 2.4 Vdc, V_{CC} = Max) D_0-D_7	I_{TSI}	—	±10	μAdc
Output High Voltage (V_{CC} = Min, Load = −600μAdc, P_0-P_7) (V_{CC} = Min, Load = −200μAdc, D_0D_7)	V_{OH}	2.4	—	Vdc
Output Low Voltage (V_{CC} = Max, Load = 6.4mAdc, P_0-P_7) (V_{CC} = Max, Load = 3.2mA, D_0-D_7)	V_{OL}	—	+0.4	Vdc
Output High Current (Sourcing) P_0-P_7 (V_{OH} = 2.4 Vdc) D_0-D_7	I_{OH} I_{OH}	−600 −200	−	μAdc μAdc
Output Low Current (Sinking) P_0-P_7 (V_{OL} = 0.4 Vdc) D_0-D_7	I_{OL} I_{OL}	6.4 3.2	−	mAdc mAdc
Supply Current	I_{CC}	−	80	mA

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

6529 WRITE CYCLE TIMING DIAGRAM



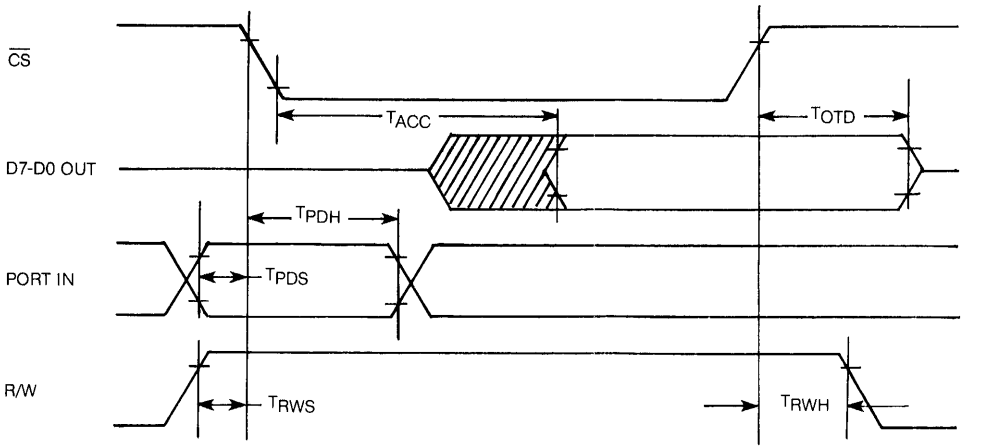
Note: All timings referred to V_{IL}max, V_{IH} min for inputs and V_{OL} max, V_{OH} min for outputs.

6529 WRITE CYCLE CHARACTERISTICS

Symbol	Characteristic	1 MHz		2 MHz		3 MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
T_{WA}*	Write Active	450	—	225	—	160	—	ns
T_{CPD}	$\overline{CS}$ to Port Out Delay	—	1000	—	500	—	330	ns
T_{DS}	Data to $\overline{CS}$ Setup	150	—	100	—	100	—	ns
T_{DH}	Data to $\overline{CS}$ Hold	0	—	0	—	0	—	ns

*T_{WA} is the time while both $\overline{CS}$ and R/W are low

6529 READ CYCLE DIAGRAM



Note: All timings referenced to V_{IL} max, V_{IH} min for inputs and V_{OL} max, V_{OH} min for outputs.

6529 READ CYCLE CHARACTERISTICS

Symbol	Characteristic	1 MHz		2 MHz		3 MHz		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
T_{ACC}	Access Time	—	450	—	225	—	160	ns
T_{PDS}	Port Input Setup	120	—	60	—	40	—	ns
T_{PDH}	Port Input Hold	30	—	30	—	30	—	ns
T_{RCS}	R/W to $\overline{CS}$ Setup	0	—	0	—	0	—	ns
T_{RCH}	R/W to $\overline{CS}$ Setup	0	—	0	—	0	—	ns
T_{OTD}	$\overline{CS}$ to Output Off Delay	20	120	20	120	20	120	ns

commodore semiconductor group

NMOS

MPS
6530
MEMORY,
I/O, TIMER
ARRAY

6530 (MEMORY, I/O, TIMER ARRAY)

PERIPHERALS

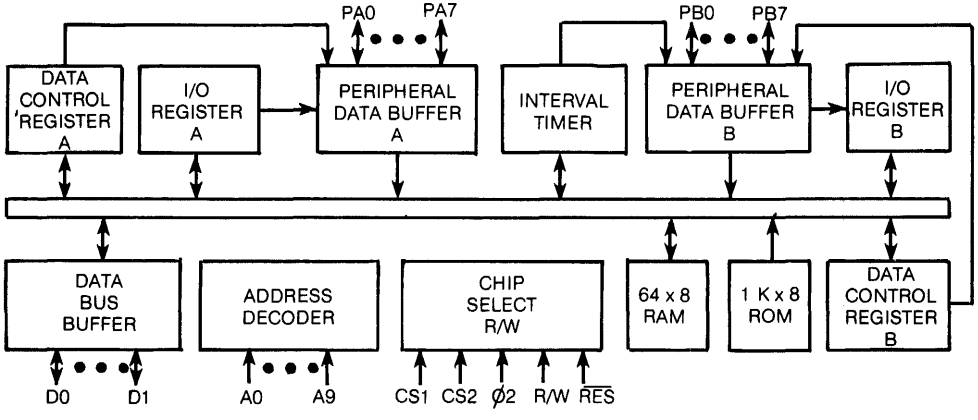
DESCRIPTION

The 6530 is designed to operate in conjunction with the 650X Microprocessor Family. It is comprised of a mask programmable 1024 x 8 ROM, a 64 x 8 static RAM, two software controlled 8 bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, and a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods.

FEATURES

- 8 bit bi-directional Data Bus for direct communication with the microprocessor
- 1024 x 8 ROM
- 64 x 8 static RAM
- Two 8 bit bi-directional data ports for interface to peripherals
- Two programmable I/O Peripheral Data Direction Registers
- Programmable Interval Timer
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Pins
- Allows up to 7K contiguous bytes of ROM with no external decoding

Figure 1. 6530 Block Diagram



MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input/Output Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature, T_{OP}	0 C to 70 C
Storage Temperature, T_{STG}	−55 C to 150 C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC}=5.0v±5%, V_{SS}=0v, T_A=25° C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}	V_{SS}+2.4		VCC	V
Input Low Voltage	V_{IL}	V_{SS}−.3		V_{SS}+.4	V
Input Leakage Current; V_{IN}=V_{SS}+5v A0-A9, RS, R/W, $\overline{RES}$, Ø2, PB6*, PB5*	I_{IN}		1.0	2.5	μA
Input Leakage Current for High Impedance State (Three State); V_{IN}=.4v to 2.4v; D0-D7	I_{TSI}		±1.0	±10.0	μA
Input High Current; V_{IN}=2.4v PA0-PA7, PB0-PB7	I_{IH}	−100.	−300.		μA
Input Low Current; V_{IN}=.4v PA0-PA7, PB0-PB7	I_{IL}		−1.0	−1.6	MA
Output High Voltage VCC=MIN, I_{LOAD} ≤ −100μA(PA0-PA7,PB0-PB7,D0-D7) I_{LOAD} ≤ −3 MA (PA0-PB0)	V_{OH}	VSS+2.4 VSS+1.5			V
Output Low Voltage VCC=MIN, I_{LOAD} ≤ 1.6MA	V_{OL}			VSS+.4	V
Output High Current (Sourcing); VOH ≥ 2.4v (PA0-PA7,PB0-PB7,D0-D7) ≥ 1.5v Available for other than TTL (Darlingtons) (PA0,PB0)	I_{OH}	−100 −3.0	−1000 −5.0		uA MA
Output Low Current (Sinking); VOL ≤ .4v (PA0-PA7) (PB0-PB7)	I_{OL}	1.6			MA
Clock Input Capacitance	C_{Clk}			30	pF
Input Capacitance	C_{IN}			10	pF
Output Capacitance	C_{OUT}			10	pF
Power Dissipation	P_D		500	1000	MW

*When programmed as address pins. All values are D.C. readings.

WRITE TIMING CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Period	TCYC	1		10	μS
Rise & Fall Times	TR, TF			25	NS
Clock Pulse Width	TC	470			NS
R/W valid before positive transition of clock	TWCW	180			NS
Address valid before positive transition of clock	TACW	180			NS
Data Bus valid before negative transition of clock	TDCW	300			NS
Data Bus Hold Time	THW	10			NS
Peripheral data valid after negative transition of clock	TCPW			1	μS
Peripheral data valid after negative transition of clock driving CMOS (Level=VCC−30%)	TCMOS			2	μS

READ TIMING CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
R/W valid before positive transition of clock	TWCR	180			NS
Address valid before positive transition of clock	TACR	180			NS
Peripheral data valid before positive transition of clock	TPCR	300			NS
Data Bus valid after positive transition of clock	TCDR			395	NS
Data Bus Hold Time	THR	10			NS
$\overline{IRQ}$ (Interval Timer Interrupt) valid before positive transition of clock	TIC	200			NS

Loading= 30 pF + 1 TTL load for PA0-PA7, PB0-PB7
=130 pF + 1 TTL load for D0-D7

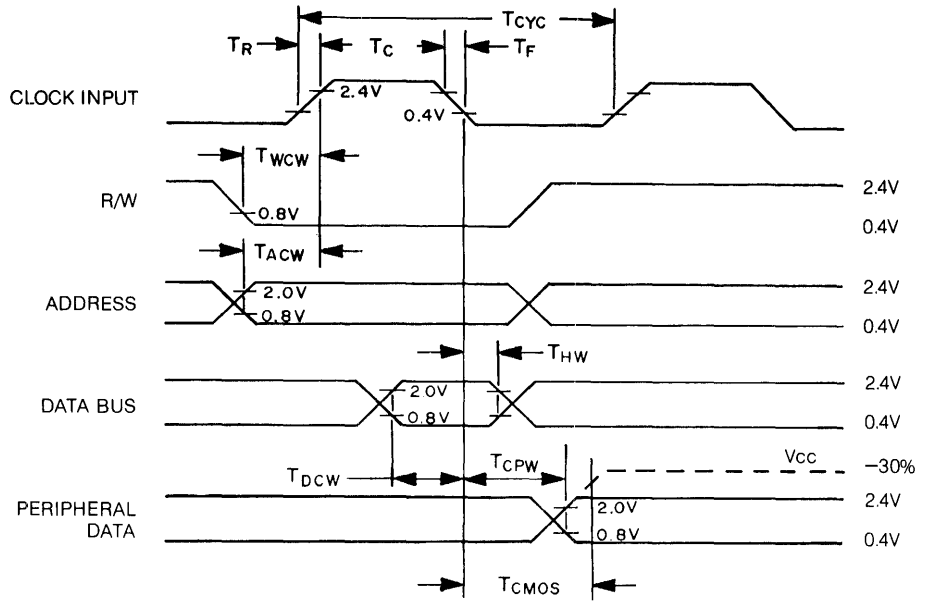


Figure 2 Write Timing Characteristics

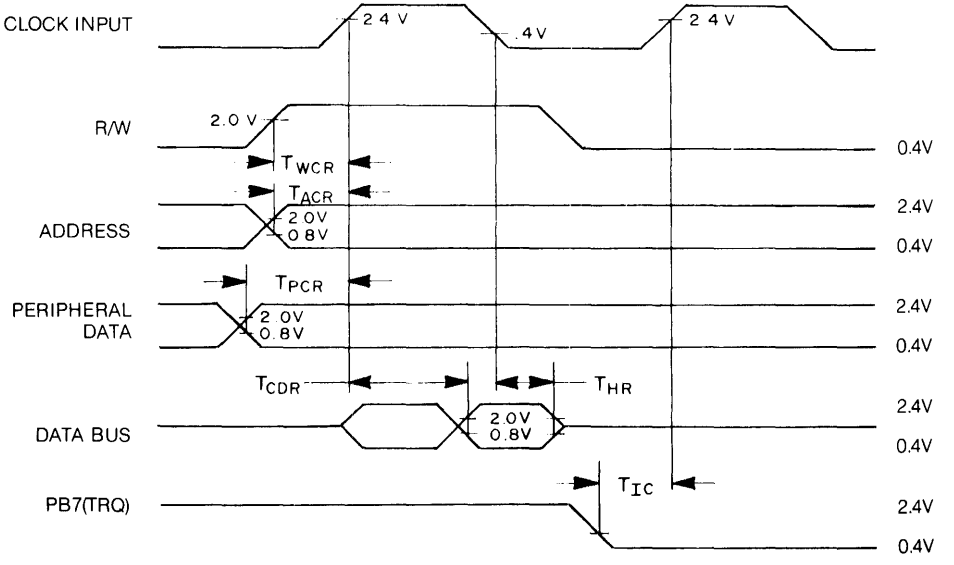


Figure 3 Read Timing Characteristics

INTERFACE SIGNAL DESCRIPTION

Reset ($\overline{RES}$)

During system initialization a Logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

Input Clock

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL} < 0.4, V_{IH} > 2.4$) or high level clock ($V_{IL} < 0.2, V_{IH} = Vcc^{+.3}_{-.2}$).

Read/Write (R/W)

The R/W signal is supplied by the microprocessor array and is used to control the transfer of data to and from the microprocessor array and the 6530. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the 6530. A low on the R/W pin allows a write (with proper addressing) to the 6530.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interval timer. This same pin, if not used as an interrupt, can be used as a peripheral I/O pin (PB7). When used as an interrupt, the pin should be set up as an input by the data direction register. The pin will be normally high with a low indicating an interrupt from the 6530. An external pull-up device is not required; however, if collector-OR'd with other devices, the internal pullup may be omitted with a mask option.

Data Bus (D0-D7)

The 6530 has eight bi-directional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor array. The output buffers remain in the off state except when a Read operation occurs.

Peripheral Data Ports

The 6530 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into 2 8-bit ports, PA0-PA7 and PB0-PB7. PB5, PB6 and PB7 also have other uses which are discussed in later sections. The pins are set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and a pull-up device acts as less than one TTL load to the periphera data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the 6530 it receives data stored in the data register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volts for a "0" as the peripheral pins are all TTL compatible. Pins PA0 and PB0 are also capable of sourcing 3 ma at 1.5v, thus making them capable of Darlington drive.

Address Lines (A0-A9)

There are 10 address pins. In addition to these 10, there is the ROM SELECT pin. The above pins, A0-A9 and ROM SELECT, are always used as addressing pins. There are 2 additional pins which are mask programmable and can be used either individually or together as CHIP SELECTS. They are pins PB5 and PB6. When used as peripheral data pins they cannot be used as chip selects.

INTERNAL ORGANIZATION

A block diagram of the internal architecture is shown in Figure 1. The 6530 is divided into four basic sections, RAM, ROM, I/O and TIMER. The RAM and ROM interface directly with the microprocessor through the system data bus and address lines. The I/O section consists of 2 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O Register.

ROM 1K Byte (8K Bits)

The 8K ROM is in a 1024 x 8 configuration. Address lines A0-A9, as well as RS0 are needed to address the entire ROM. With the addition of CS1 and CS2, seven 6530's may be addressed, giving 7168 x 8 bits of contiguous ROM.

RAM — 64 Bytes (512 Bits)

A 64 x 8 static RAM is contained on the 6530. It is addressed by A0-A5 (Byte Select), RS0, A6, A7, A8, A9 and, depending on the number of chips in the system, CS1 and CS2.

Internal Peripheral Registers

There are four internal registers, two data direction registers and two peripheral I/O data registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral buffer pin as an output. Therefore, anything then written into the I/O Register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data to or from the I/O Register. For example, a "1" loaded into data direction register A, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and remain in the high state. The two data I/O registers are used to latch data from the Data Bus during a Write operation until the peripheral device can read the data supplied by the microprocessor array.

During a read operation the microprocessor is not reading the I/O Registers but in fact is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the I/O Register. The only way the I/O Register data can be changed is by a microprocessor Write operation. The I/O Register is not affected by a Read of the data on the peripheral pins.

Interval Timer

The Timer section of the 6530 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic. These are illustrated in Figure 4.

The interval timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1." After the interrupt flag is set the internal clock begins counting down to a maximum of −255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

The 8 bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., $A_3 = 1$ enables IRQ on PB7, $A_3 = 0$ disables IRQ on PB7. When PB7 is to be used as an interrupt flag with the interval timer it should be programmed as an input. If PB7 is enabled by A3 and an interrupt occurs PB7 will go low. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the timer has counted down to 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 28T. The value read is in two's complement.

Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1
ADD 1 = 0 0 0 1 1 1 0 0 = 28.

Thus, to arrive at the **total** elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divided by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After the interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flag is read on DB7 all other DB outputs (DB0 thru DB6) go to "0". Figure 5 illustrates an example of interrupt.

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write timer operation.

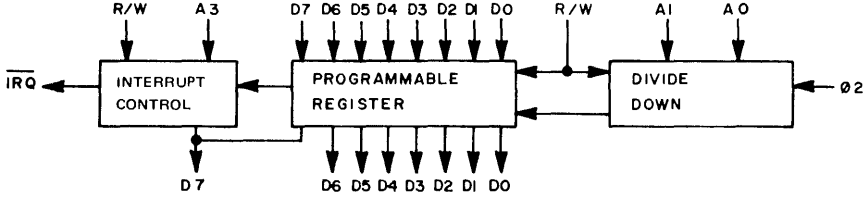
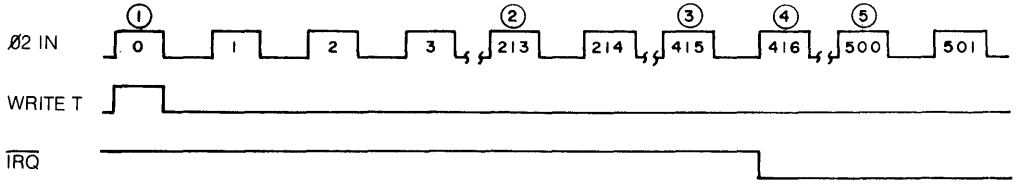


Figure 4. Basic Elements of Interval Timer



1. Data written into interval timer is 0 0 1 1 0 1 0 0 = 52_{10}
2. Data in Interval timer is 0 0 0 1 1 0 0 1 = 25_{10}
   $52 - \frac{213}{8} - 1 = 52\text{-}26\text{-}1 = 25$
3. Data in Interval timer is 0 0 0 0 0 0 0 0 = 0_{10}
   $52 - \frac{415}{8} - 1 = 52\text{-}51\text{-}1 = 0$
4. Interrupt has occurred at $Ø_2$ pulse #416
   Data in Interval timer = 1 1 1 1 1 1 1 1
5. Data in Interval timer is 1 0 1 0 1 1 0 0
   two's complement is 0 1 0 1 0 1 0 0 = 84_{10}
   $84 + (52 \times 8) = 500_{10}$

Figure 5

ADDRESSING

Addressing of the 6530 offers many variations to the user for greater flexibility. The user may configure his system with RAM in lower memory, ROM in higher memory, and I/O registers with interval timers between the extremes. There are 10 address lines (A0-A9). In addition, there is the possibility of 3 additional address lines to be used as chip-selects and to distinguish between ROM, RAM, I/O and interval timer. Two of the additional lines are chip-selects 1 and 2 (CS1 and CS2). The chip-select pins can also be PB5 and PB6. Whether the pins are used as chip-selects or peripheral I/O pins is a mask option and must be specified when ordering the part. Both pins act independently of each other in that either or both pins may be designated as a chip-select. The third additional address line is RS0. The 6502 and 6530 in a 2-chip system would use RS0 to distinguish between ROM and non-ROM sections of the 6530. With the addressing pins available, a total of 7K contiguous ROM may be addressed with no external decode. Below is an example of a 1-chip and a 7-chip 6530 Addressing Scheme.

One-Chip Addressing

Figure 6 illustrates a 1-chip system decode for the 6530.

Seven-Chip Addressing

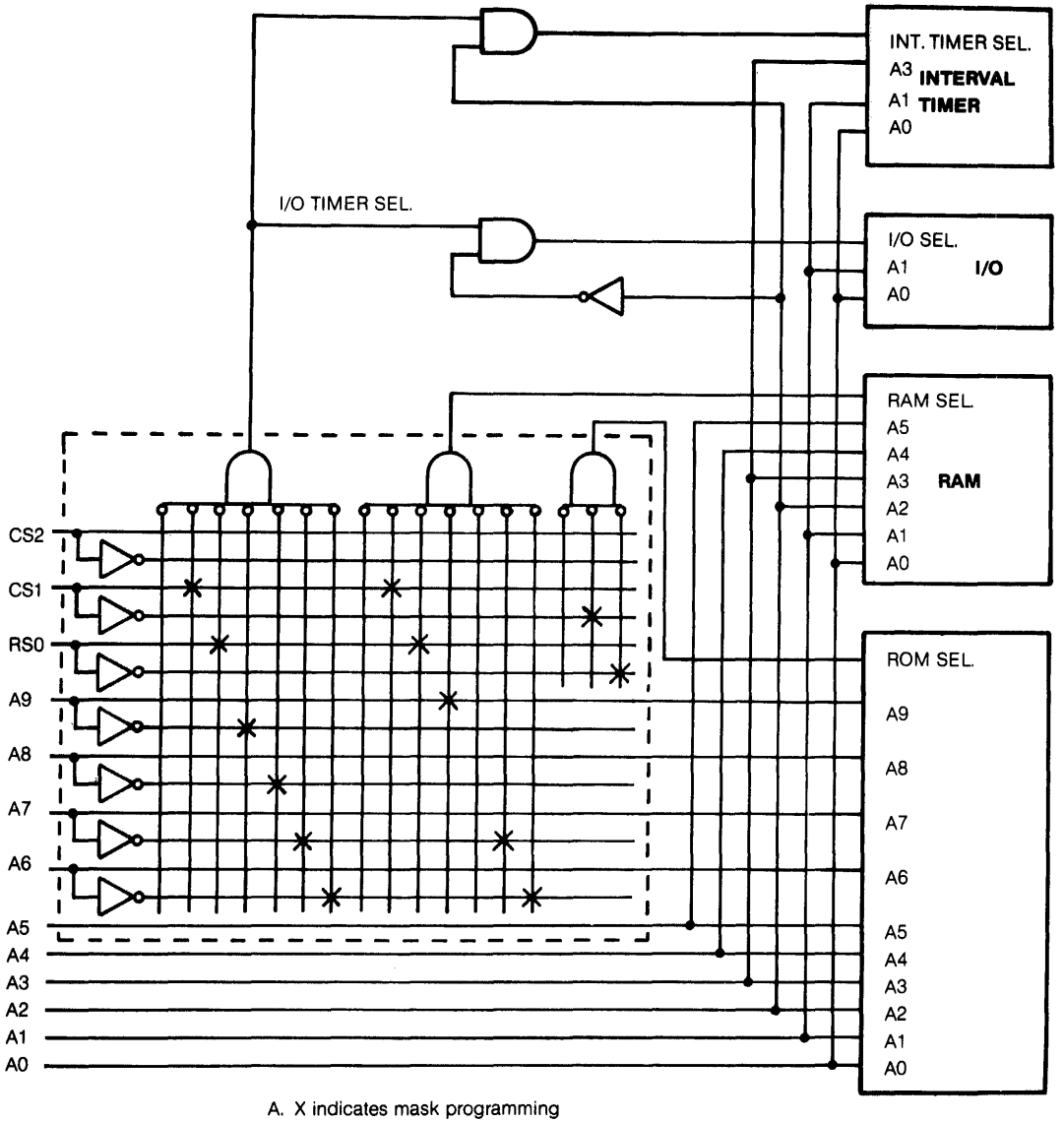
In the 7-chip system the objective would be to have 7K of contiguous ROM, with RAM in low order memory. The 7K of ROM could be placed between addresses 65,535 and 1024. For this case, assume A13, A14 and A15 are all 1 when addressing ROM, and 0 when addressing RAM or I/O. This would place the 7K ROM between Addresses 65,535 and 58,367. The 2 pins designated as chip-select or I/O would be masked programmed as chip-select pins. Pin RS0 would be connected to address line A10. Pins CS1 and CS2 would be connected to address lines A11 and A12 respectively. See Figure 7.

The two examples shown would allow addressing of the ROM and RAM; however, once the I/O or timer has been addressed, further decoding is necessary to select which of the I/O registers are desired, as well as the coding of the interval timer.

I/O Register — Timer Addressing

Figure 8 illustrates the address decoding for the internal elements and timer programming. Address lines A2 distinguishes I/O registers from the timer. When A2 is high and I/O timer select is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected A1 and A0 decode the divide by matrix. This decoding is defined in Figure 8. In addition, Address A3 is used to enable the interrupt flag to PB7.



A. X indicates mask programming
   i.e. ROM select=$\overline{CS1} \bullet RS0$
   RAM select=$\overline{CS1} \bullet \overline{RS0} \bullet \overline{A9} \bullet A7 \bullet A6$
   I/O TIMER SELECT=$\overline{CS1} \bullet \overline{RS0} \bullet A9 \bullet A8 \bullet A7 \bullet A6$
B. Notice that A8 is a don't care for RAM select
C. CS2 can be used as PB5 in this example.

Figure 6. 6530 One Chip Address Encoding Diagram

The addressing of the ROM select, RAM select and I/O Timer select lines would be as follows:

		CS2 A12	CS1 A11	RS0 A10	A9	A8	A7	A6
6530 #1,	ROM SELECT	0	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	0
	I/O TIMER	0	0	0	1	0	0	0
6530 #2,	ROM SELECT	0	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	1
	I/O TIMER	0	0	0	1	0	0	1
6530 #3,	ROM SELECT	0	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	0
	I/O TIMER	0	0	0	1	0	1	0
6530 #4,	ROM SELECT	1	0	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	1
	I/O TIMER	0	0	0	1	0	1	1
6530 #5,	ROM SELECT	1	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	0
	I/O TIMER	0	0	0	1	1	0	0
6530 #6,	ROM SELECT	1	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	1
	I/O TIMER	0	0	0	1	1	0	1
6530 #7,	ROM SELECT	1	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	1	0
	I/O TIMER	0	0	0	1	1	1	0

*RAM select for 6530 #5 would read = $\overline{A12} \bullet \overline{A11} \bullet \overline{A10} \bullet \overline{A9} \bullet A8 \bullet \overline{A7} \bullet \overline{A6}$

Figure 7. 6530 Seven Chip Addressing Scheme

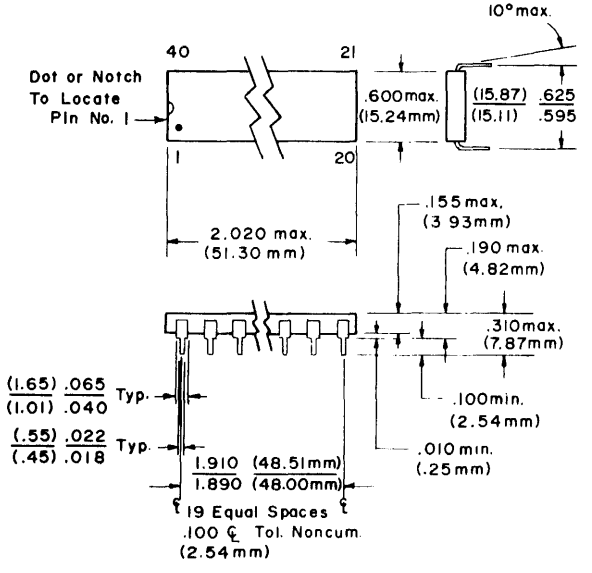
ADDRESSING DECODE

	ROM SELECT	RAM SELECT	I/O TIMER SELECT	R/W	A3	A2	A1	A0
READ ROM	1	0	0	1	X	X	X	X
WRITE RAM	0	1	0	0	X	X	X	X
READ RAM	0	1	0	1	X	X	X	X
WRITE DDRA	0	0	1	0	X	0	0	1
READ DDRA	0	0	1	1	X	0	0	1
WRITE DDRB	0	0	1	0	X	0	1	1
READ DDRB	0	0	1	1	X	0	1	1
WRITE PER. REG. A	0	0	1	0	X	0	0	0
READ PER. REG. A	0	0	1	1	X	0	0	0
WRITE PER. REG. B	0	0	1	0	X	0	1	0
READ PER. REG. B	0	0	1	1	X	0	1	0
WRITE TIMER								
÷ 1T	0	0	1	0	*	1	0	0
÷ 8T	0	0	1	0	*	1	0	1
÷ 64T	0	0	1	0	*	1	1	0
÷ 1024T	0	0	1	0	*	1	1	1
READ TIMER	0	0	1	1	*	1	X	0
READ INTERRUPT FLAG	0	0	1	1	X	1	X	1

*A_3 = 1 Enables IRQ to PB7

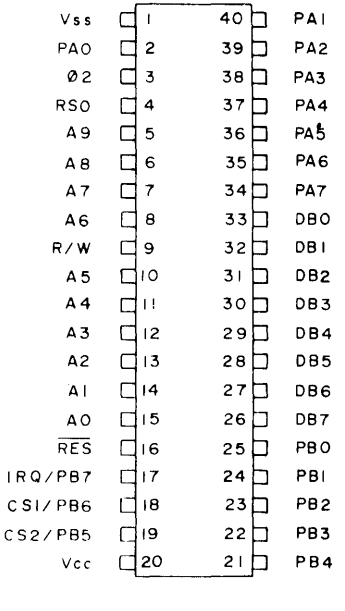
A_3 = 0 Disables IRQ to PB7

Figure 8. Addressing Decode for I/O Register and Timer



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

PACKAGE OUTLINE



6530 PIN DESIGNATION

commodore semiconductor group

NMOS

MPS

6532

MEMORY, I/O, TIMER ARRAY

6532 (MEMORY, I/O, TIMER ARRAY)

THE 6532 CONCEPT—

The 6532 is designed to operate in conjunction with the MCS650X Microprocessor Family. It is comprised of a 128 x 8 static RAM, two software controlled 8 bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, a software programmable interval timer with interrupt capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge detect circuit.

FEATURES OF THE 6532

- 8 bit bi-directional Data Bus for direct communication with the microprocessor
- Programmable edge-sensitive interrupt
- 128 x 8 static RAM
- Two 8 bit bi-directional data ports for interface to peripherals
- Two programmable I/O Peripheral Data Direction Registers
- Programmable Interval Timer
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Pins
- 1MHz, 2MHz and 3MHz operation

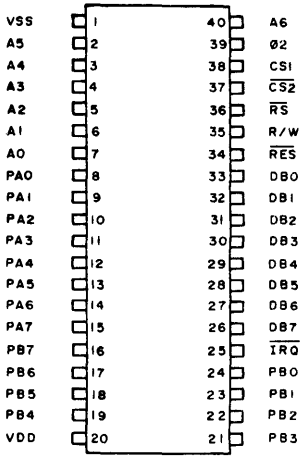
ORDERING INFORMATION

MXS 6532 ___

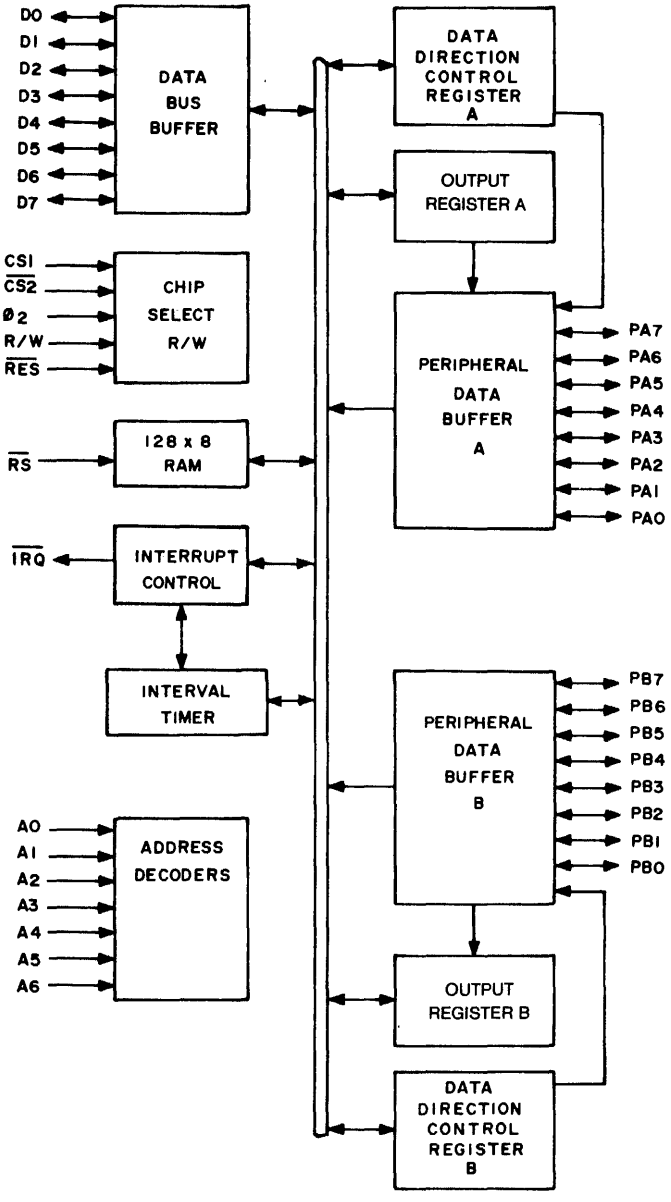
FREQUENCY RANGE
NO SUFFIX = 1 MHz
A = 2 MHz

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

6532 PIN DESIGNATION



BLOCK DIAGRAM



MAXIMUM RATINGS

RATING	SYMBOL	VOLTAGE	UNIT
Supply Voltage	VCC	−.3 to +7.0	V
Input/Output Voltage	V_{IN}	−.3 to +7.0	V
Operating Temperature Range	T_{OP}	0 to 70	°C
Storage Temperature Range	T_{STG}	−55 to +150	°C

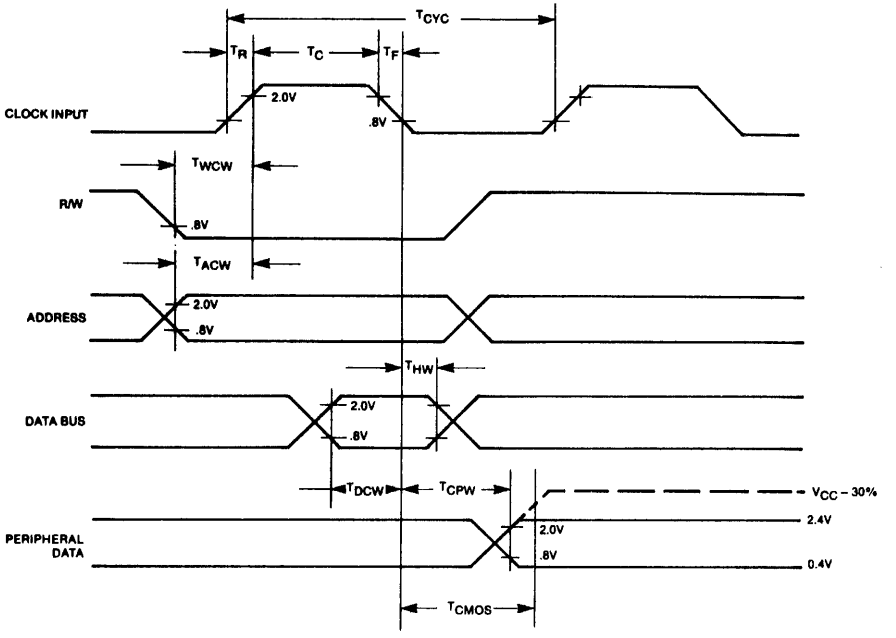
All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specified range.

ELECTRICAL CHARACTERISTICS (VCC = 5.0v ± 5%, VSS = 0v, T_A = 0-70°C)

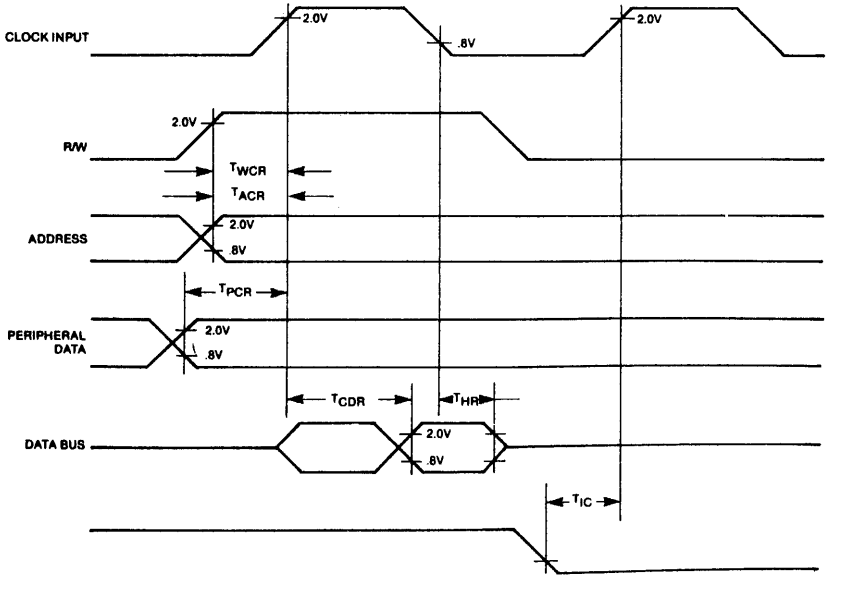
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}	V_{SS} + 2.4	1.3	VCC	V
Input Low Voltage	V_{IL}	V_{SS} − .3	1.1	V_{SS} + .8	V
Input Leakage Current; V_{IN} = V_{SS} + 5v A0-A6, $\overline{RS}$, R/W, $\overline{RES}$, Ø2, CS1, $\overline{CS2}$	I_{IN}	—	1.0	2.5	μA
Input Leakage Current for High Impedance State (Three State); V_{IN} = .4v to 2.4v; D0-D7	I_{TSI}	—	±1.0	±10.0	μA
Input High Current; V_{IN} = 2.4v PA0-PA7, PB0-PB7	I_{IH}	−100.	−300.	—	μA
Input Low Current; V_{IN} = .4v PA0-PA7, PB0-PB7	I_{IL}	—	−1.0	−1.6	mA
Output High Voltage VCC = MIN, $I_{LOAD} \leq$ · 100μA(PA0-PA7, PB0-PB7, D0-D7)	V_{OH}	VSS + 2.4	3.5	VCC	V
Output Low Voltage VCC = MIN, $I_{LOAD} \leq$ 1.6MA	V_{OL}	V_{SS}	.2	VSS + .4	V
Output High Current (Sourcing); VOH ≥ 2.4v (PA0-PA7, PB0-PB7, D0-D7)	I_{OH}	−100	−1000	—	μA
Output Low Current (Sinking); VOL ≤ .4v (PA0-PA7) (PB0-PB7)	I_{OL}	1.6	3.0	--	mA
Clock Input Capacitance	C_{Clk}	—	18	30	pf
Input Capacitance	C_{IN}	—	7	10	pf
Output Capacitance	C_{OUT}	—	7	10	pf
Power Dissipation	P_D	—	500	1000	mW

PERIPHERALS

WRITE TIMING CHARACTERISTICS



READ TIMING CHARACTERISTICS



WRITE TIMING CHARACTERISTICS

CHARACTERISTIC	SYMBOL	1MHz		2MHz		3MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Clock Period	T_{CYC}	1	20	.5	10	0.33	10	μS
Rise & Fall Times	T_R, T_F	—	25	—	25	—	25	nS
Clock Pulse Width	T_C	.470	10	.235	5	0.160	5	μS
R/W valid before positive transition of clock	T_{WCW}	180	—	90	—	60	—	nS
Address valid before positive transition of clock	T_{ACW}	180	—	90	—	60	—	nS
Data Bus valid before negative transition of clock	T_{DCW}	300	—	150	—	100	—	nS
Data Bus Hold Time	T_{HW}	10	—	10	—	10	—	nS
Peripheral data valid after negative transition of clock	T_{CPW}	—	1	—	.500	—	.333	μS
Peripheral data valid after negative transition of clock driving CMOS (Level=VCC−30%)	T_{CMOS}	—	2	—	1	—	.666	μS

READ TIMING CHARACTERISTICS

CHARACTERISTIC	SYMBOL	1MHz		2MHz		3MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
R/W valid before positive transition of clock	T_{WCR}	180	—	90	—	60	—	nS
Address valid before positive transition of clock	T_{ACR}	180	—	90	—	60	—	nS
Peripheral data valid before positive transition of clock	T_{PCR}	300	—	150	—	100	—	nS
Data Bus valid after positive transition of clock	T_{CDR}	—	400	—	200	—	135	nS
Data Bus Hold Time	T_{HR}	10	—	10	—	10	—	nS
$\overline{IRQ}$ valid before positive transition of clock	T_{IC}	200	—	100	—	75	—	nS

Loading = 30 pf + 1 TTL load

INTERNAL ORGANIZATION

A block diagram of the internal architecture is shown in Figure 1. The 6532 is divided into four basic sections, RAM, I/O, TIMER, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O Register.

RAM—128 Bytes (1024 Bits)

The 128 x 8 Read/Write memory acts as a conventional static RAM. Data can be written into the RAM from the microprocessor by selecting the chip ($CS1 = 1$, $\overline{CS2} = 0$) and by setting $\overline{RS}$ to a logic 0 (0.4v). Address lines A0 through A6 are then used to select the desired byte of storage.

Internal Peripheral Registers

The Peripheral A I/O port consists of eight lines which can be individually programmed to act as either an input or an output. A logic zero in a bit of the Data Direction Register (DDRA) causes the corresponding line of the PA port to act as an input. A logic one causes the corresponding PA line to act as an output. The voltage on any line programmed to be an output is determined by the corresponding bit in the Output Register (ORA).

Data is read directly from the PA pins during any read operation. For any output pin, the data transferred into the processor will be the same as that contained in the Output Register if the voltage on the pin is allowed to go to 2.4v for a logic one. Note that for input lines, the processor can write into the corresponding bit of the Output Register. This will not affect the polarity on the pin until the corresponding bit of DDRA is set to a logic one to allow the peripheral pin to act as an output.

In addition to acting as a peripheral I/O line, the PA7 line can be used as an edge-detecting input. In this mode, an active transition will set the internal interrupt flag (bit 6 of the Interrupt Flag register). Setting the interrupt flag will cause $\overline{IRQ}$ output to go low if the PA7 interrupt has been enabled. The PA7 line should be set up as an input for this mode.

Control of the PA7 edge detecting mode is accomplished by writing to one of four addresses. In this operation, A0 controls the polarity of the active transition and A1 acts to enable or disable interrupting of the processor. The data which is placed on the Data Bus during this operation is discarded and has no effect on the control of PA7.

Setting of the PA7 interrupt flag will occur on an active transition even if the pin is being used as a normal input or as a peripheral control output. The flag will also be set by an active transition if interrupting from PA7 is disabled. The reset signal ($\overline{RES}$) will disable the PA7 interrupt and will set the active transition to negative (high to low). During the system initialization routine, it is possible to set the interrupt flag by a negative transition. It may also be set by changing the polarity of the active interrupt. It is therefore recommended that the interrupt flag be cleared before enabling interrupting from PA7.

Clearing of the PA7 Interrupt Flag occurs when the microprocessor reads the Interrupt Flag Register.

The operation of the Peripheral B Input/Output port is exactly the same as the normal I/O operation of the Peripheral A port. The eight lines can each be programmed to act as either an input or as an output by placing a 0 or a 1 into the Data Direction register (DDRB). In the output mode, the voltage on a peripheral pin is controlled by the Output Register (ORB).

The primary difference between the PA and the PB ports is in the operation of the output buffers which drive these pins. The buffers are push-pull devices which are capable of sourcing 3 ma at 1.5v. This allows these pins to directly drive transistor switches. To assure that the microprocessor will read proper data on a "Read PB" operation, sufficient logic is provided in the chip to allow the microprocessor to read the Output Register instead of reading the peripheral pin as on the PA port.

INTERFACE SIGNAL DESCRIPTION

Reset ($\overline{RES}$)

During system initialization a logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

Input Clock

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL} < 0.4$, $V_{IL} > 2.4$) or high level clock ($V_{IL} < 0.2$, $V_{IH} = Vcc \begin{smallmatrix}+.3\\-.2\end{smallmatrix}$)

Read/Write (R/W)

The R/W signal is supplied by the microprocessor array and is used to control the transfer of data to and from the microprocessor array and the 6532. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the 6532. A low on the R/W pin allows a write (with proper addressing) to the 6532.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interrupt control logic. The pin will be normally high with a low indicating an interrupt from the 6532. An external pull-up device is required. The $\overline{IRQ}$ pin may be activated by a transition on PA7 or timeout of the interval timer.

Data Bus (D0-D7)

The 6532 has eight bi-directional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor array. The output buffers remain in the off state except when a Read operation occurs and are capable of driving one standard TTL load and 130 pf.

Peripheral Data Ports

The 6532 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into 2 8-bit ports, PA0-PA7 and PB0-PB7. PA7 also has other uses which are discussed in later sections. The pins are set as inputs by writing a "0" into the corresponding bit of the data direction register. A "1" into the data direction register will cause the corresponding pin to be an output. When in the input mode, the peripheral output buffers are in the "1" state and pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the 6532 it receives data stored in the data register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volts for a "0" as the peripheral pins are all TTL compatible. Pins PB0-PB7 are also capable of sourcing 3 ma at 1.5v, thus making them capable of Darlington drive.

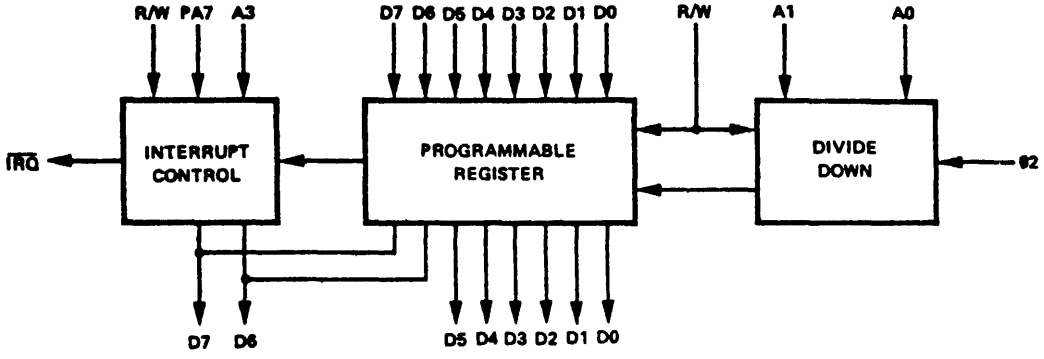
Address Lines (A0-A6)

There are 7 address pins. In addition to these 7, there is a $\overline{\text{RAM SELECT}}$ pin. These pins, A0-A6 and $\overline{\text{RAM SELECT}}$, are always used as addressing pins. There are two additional pins which are used as CHIP SELECTS. They are pins CS1 and $\overline{CS2}$.

Interval Timer

The Timer section of the 6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic.

Figure 2. BASIC ELEMENTS OF INTERVAL TIMER



The interval time can be programmed to count up to 255 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock begins counting down to a maximum of – 255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

The 8 bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability; i.e., A_3 = 1 enables $\overline{IRQ}$, A_3 = 0 disables $\overline{IRQ}$. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the timer has counted thru 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is in two's complement, but remember that interrupt occurred on count number. Therefore, we must subtract 1.

Value read = 1 1 1 0 0 1 0 0

Complement = 0 0 0 1 1 0 1 1

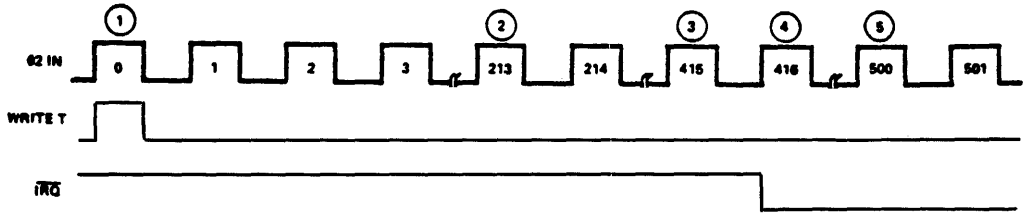
ADD 1 = 0 0 0 1 1 1 0 0 = 28 Equals two's complement of register

SUB 1 = 0 0 0 1 1 0 1 1 = 27

Thus, to arrive at the total elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (= 52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After the interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flags are read (DB7 for the timer, DB6 for edge detect) data bus lines D0-D5 go to 0.

Figure 3. TIMER INTERRUPT TIMING



1. Data written into interval timers is 0 0 1 1 0 1 0 0 = 52_{10}
2. Data in interval timer is 0 0 0 1 1 0 0 1 = 25_{10}

   $52-\frac{213}{8}-1 = 52-26-1 = 25$

3. Data in interval timer is 0 0 0 0 0 0 0 0 = 0_{10}

   $52-\frac{415}{8}-1 = 52-51-1 = 0$

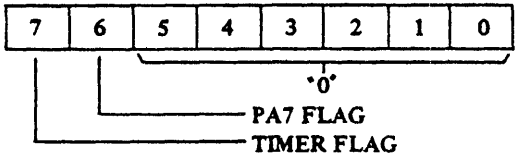
4. Interrupt has occurred at 02 pulse #416
   Data in interval timer = 1 1 1 1 1 1 1 1
5. Data in interval timer is 1 0 1 0 1 1 0 0
   two's complement is 0 1 0 1 0 1 0 0 = 84_{10}
   $84 + (52x8) = 500_{10}$

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write operation.

Interrupt Flag Register

The Interrupt Flag Register consists of two bits: the timer interrupt flag and the PA7 interrupt flag. When a read operation is performed on the Interrupt Flag Register, the bits are transferred to the processor on the data bus, as the diagram below, indicates.

Figure 4. INTERRUPT FLAG REGISTER



The PA7 flag is cleared when the Interrupt Flag Register is read. The timer flag is cleared when the timer register is either written or read.

PERIPHERALS

ADDRESSING

Addessing of the 6532 is accomplished by the 7 addressing pins, the $\overline{RS}$ pin and the two chip select pins CS1 and $\overline{CS2}$. To address the RAM, CS1 must be high with $\overline{CS2}$ and $\overline{RS}$ low. To address the I/O and Interval timer CS1 and $\overline{RS}$ must be high with $\overline{CS2}$ low. As can be seen to access the chip CS1 is high and $\overline{CS2}$ is low. To distinguish between RAM or I/O Timer the $\overline{RS}$ pin is used. When this pin is low the RAM is addressed, when high the I/O interval timer section is addressed. To distinguish between timer and I/O address line A2 is utilized. When A2 is high the interval timer is accessed. When A2 is low the I/O section is addressed. Table 1 illustrates the chip addressing.

Edge Sense Interrupt

In addition to its use as a peripheral I/O line, the PA7 pin can function as an edge sensitive input. In this mode, an active transition on PA7 will set the internal interrupt flag (bit 6 of the Interrupt Flag Register). When this occurs, and providing the PA7 interrupt is enabled, the $\overline{IRQ}$ output will go low.

Control of the PA7 edge detecting logic is accomplished by performing a write operation for one of four addresses. The data lines for this operation are "don't care" and the addresses to be used are found in Figure 4.

The setting of the internal interrupt flag by an active transition on PA7 is always enabled, no matter whether PA7 is set up as an input or an output.

The $\overline{RES}$ signal disables the PA7 interrupt and sets the active transition to the negative edge-detect state. During the reset operation, the interrupt flag may be set by a negative transition. It may, therefore, be necessary to clear the flag before its normal use as an edge detecting input is enabled. This can be achieved by reading the Interrupt Flag Register, as defined by Figure 4 immediately after reset.

I/O Register—Timer Addressing

Table 1 illustrates the address decoding for the internal elements and timer programming. Address line A2 distinguishes I/O registers from the timer. When A2 is low and $\overline{RS}$ is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected A1 and A0 decode the "divide-by" matrix. This decoding is defined in Table 1. In addition, Address A3 is used to enable the interrupt flag to $\overline{IRQ}$.

Table 1: ADDRESSING DECODE

OPERATION	$\overline{RS}$	R/W	A4	A3	A2	A1	A0
Write RAM	0	0	—	—	—	—	—
Read RAM	0	1	—	—	—	—	—
Write DDRA	1	0	—	—	0	0	1
Read DDRA	1	1	—	—	0	0	1
Write DDRB	1	0	—	—	0	1	1
Read DDRB	1	1	—	—	0	1	1
Write Output Reg A	1	0	—	—	0	0	0
Read Output Reg A	1	1	—	—	0	0	0
Write Output Reg B	1	0	—	—	0	1	0
Read Output Reg B	1	1	—	—	0	1	0
Write Timer							
÷1T	1	0	1	(a)	1	0	0
÷8T	1	0	1	(a)	1	0	1
÷64T	1	0	1	(a)	1	1	0
÷1024T	1	0	1	(a)	1	1	1
Read Timer	1	1	—	(a)	1	—	0
Read Interrupt Flag(s)	1	1	—	—	1	—	1
Write Edge Detect Control	1	0	0	—	1	(b)	(c)

NOTES:— = Don't Care, "1" = High level (>2.4V),"0" = Low level (<0.4V)

(a) A3 = 0 to disable interrupt from timer to $\overline{IRQ}$
A3 = 1 to enable interrupt from timer to $\overline{IRQ}$
(b) A1 = 0 to disable interrupt from PA7 to $\overline{IRQ}$
A1 = 1 to enable interrupt from PA7 to $\overline{IRQ}$
(c) A0 = 0 for negative edge-detect
A0 = 1 for positive edge-detect

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NMOS

MPS

6545-1

CRT CONTROLLER (CRTC)

6545-1 CRT Controller (CRTC)

CONCEPT

The 6545-1 is a CRT Controller intended to provide capability for interfacing the 6500/6800 microprocessor families to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

FEATURES:

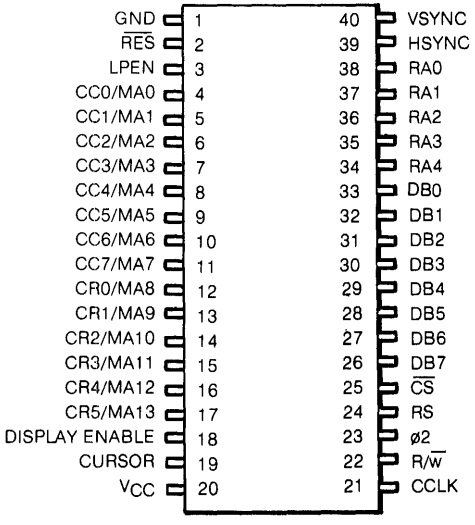
- Single +5 volt (±5%) power supply.
- Alphanumeric and limited graphics capabilities.
- Fully programmable display (rows, columns, blanking, etc.).
- Non-interlaced scan.
- 50/60 Hz operation.
- Fully programmable cursor.
- External light pen capability.
- Capable of addressing up to 16K character video display RAM.
- No DMA required.
- Pin-compatible with MC6845.
- Row/Column or straight-binary addressing for video display RAM.
- Internal 8-bit status register.

ORDERING INFORMATION

MXS 6545-1 1 MHz
MXS 6545A-1 2 MHz

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

6545-1 PIN DESIGNATION



MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input/Output Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	−55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

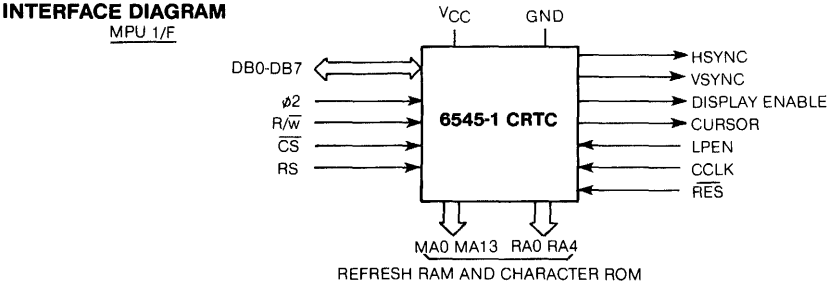
COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

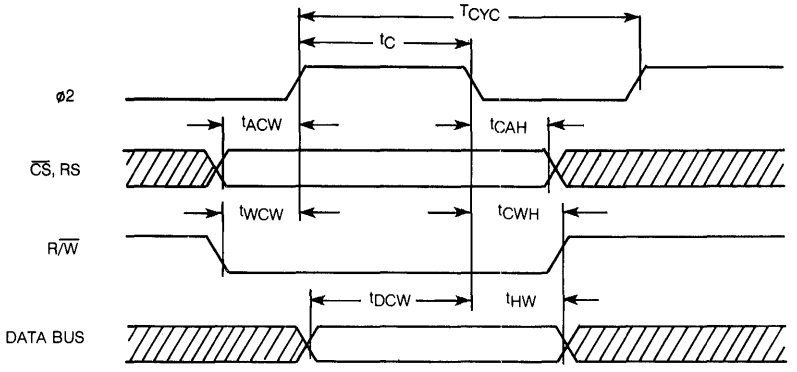
Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage	2.0	V_{CC}	V
V_{IL}	Input Low Voltage	−0.3	0.8	V
I_{IN}	Input Leakage (ø2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	—	2.5	µA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	—	10.0	µA
V_{OH}	Output High Voltage I_{LOAD} = 205µA (DB0-DB7) I_{LOAD} = 100µA (all others)	2.4	V_{CC}	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	V_{SS}	0.4	V
P_D	Power Dissipation	—	1000	mW
C_{IN}	Input Capacitance ø2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK DB0-DB7	— —	10.0 12.5	pF pF
C_{OUT}	Output Capacitance	—	10.0	pF

INTERFACE DIAGRAM



MPU BUS INTERFACE CHARACTERISTICS

WRITE CYCLE



WRITE TIMING CHARACTERISTICS

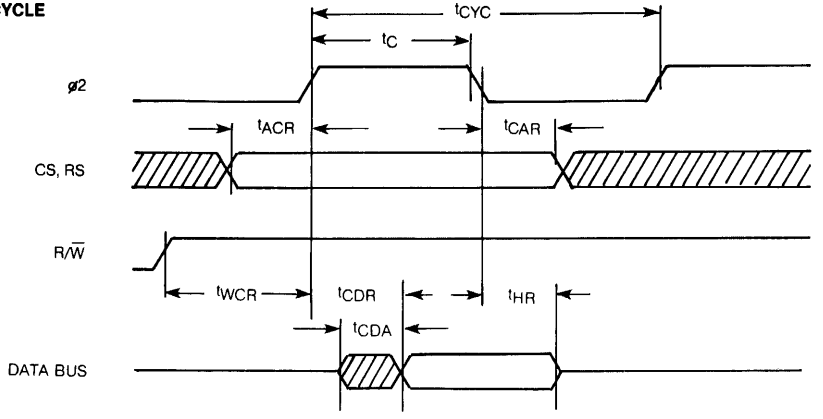
(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Symbol	Characteristic	6545-1		6545A-1		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	40	0.5	40	µs
t_C	ø2 Pulse Width	470	—	235	—	ns
t_{ACW}	Address Set-Up Time	180	—	90	—	ns
t_{CAH}	Address Hold Time	0	—	0	—	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	180	—	90	—	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	—	0	—	ns
t_{DCW}	Data Bus Set-Up Time	265	—	100	—	ns
t_{HW}	Data Bus Hold Time	10	—	10	—	ns

(t_r and t_f = 10 to 30 ns)

MPU BUS INTERFACE CHARACTERISTICS

READ CYCLE



READ TIMING CHARACTERISTICS

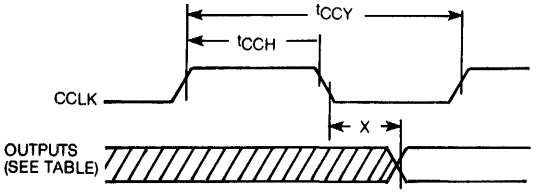
(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Symbol	Characteristic	6545-1		6545A-1		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	40	0.5	40	µs
t_C	ø2 Pulse Width	470	—	235	—	ns
t_{ACR}	Address Set-Up Time	180	—	90	—	ns
t_{CAR}	Address Hold Time	0	—	0	—	ns
t_{WCR}	R/$\overline{w}$ Set-Up Time	180	—	90	—	ns
t_{CDR}	Read Access Time	—	340	—	150	ns
t_{HR}	Read Hold Time	10	—	10	—	ns
t_{CDA}	Data Bus Active Time (Invalid Data)	40	—	40	—	ns

(t_r and t_f = 10 to 30 ns)

MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)



SYSTEM TIMING

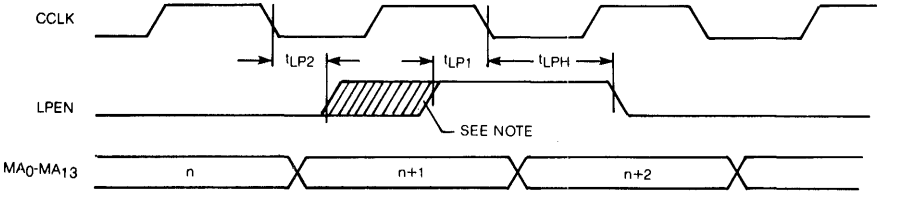
Output	Parameter
MA0-MA13	t_{MAD}
RA0-RA4	t_{RAD}
DISPLAY-ENABLE	t_{DTD}
HSYNC	t_{HSD}
VSYNC	t_{VSD}
CURSOR	t_{CDD}

SYSTEM TIMING PARAMETERS (V_{CC} = 5.0V + 5%, T_A = 0 to 70°C, unless otherwise noted)

Symbol	Characteristics	6545-1		6545A-1		Unit
		Min.	Max.	Min.	Max.	
t_{CCY}	Character Clock Cycle Time	0.40	40	0.40	40	µs
t_{CCH}	Character Clock Pulse Width	200	—	200	—	ns
t_{MAD}	MA0-MA13 Propagation Delay	—	300	—	300	ns
t_{RAD}	RA0-RA4 Propagation Delay	—	300	—	300	ns
t_{DTD}	DISPLAY ENABLE Propagation Delay	—	375	—	375	ns
t_{HSD}	HSYNC Propagation Delay	—	375	—	375	ns
t_{VSD}	VSYNC Propagation Delay	—	375	—	375	ns
t_{CDD}	CURSOR Propagation Delay	—	375	—	375	ns
t_{LPH}	LPEN Hold Time	100	—	100	—	ns
t_{LP1}	LPEN Set-up Time	20	—	20	—	ns
t_{LP2}	CCLK to LPEN Delay	0	—	0	—	ns

t_r, t_f = 20 ns (max)

LIGHT PEN STROBE TIMING DEFINITIONS



NOTE: "Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.

MPU INTERFACE SIGNAL DESCRIPTION

ø2 (Clock)

The input clock is the system ø2 clock and is used to trigger all data transfers between the system microprocessor and the 6545-1.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the 6545-1; a low on the R/$\overline{W}$ pin allows a write to the 6545-1.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The 6545-1 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes into the Address Register and reads from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

DB_0-DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the 6545-1. These lines are bi-directional and are normally high-impedance except during read cycles when the chip is selected.

VIDEO INTERFACE SIGNAL DESCRIPTION

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the 6545-1 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal. Display Enable can be delayed by one character time by setting bit 4 of R8 to a "1".

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The CURSOR position may be delayed by one character time by setting bit 5 of R8 to a "1."

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

MEMORY ADDRESS SIGNAL DESCRIPTION

MA0-MA13 (Refresh RAM Address Lines)

These signals are active-high outputs and are used to address the Refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

In the *straight binary* mode, characters are stored in successive memory locations. Thus, the software must be designed so that row and column character co-ordinates are translated into sequentially-numbered addresses. In the *row/column* mode MA0-MA7 become column addresses CC0-CC7 and MA8-MA13 become row addresses CR0-CR5. In this case, the software can manipulate characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-CC7 and CR0-CR5 addresses into a memory efficient binary address scheme.

RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

DESCRIPTION OF INTERNAL REGISTERS

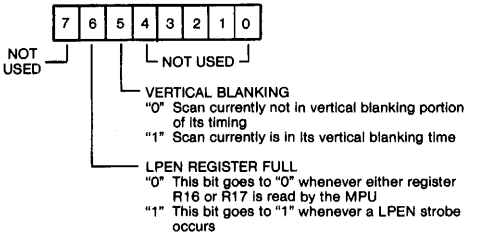
Figure 1 illustrates the format of a typical video display and is necessary to understand the functions of the various 6545-1 internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct 6545-1 data transfers to and from the system MPU. Its contents is the number of the desired register (0-31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

Status Register

This register is used to monitor the status of the CRTC, as follows:



Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)

This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

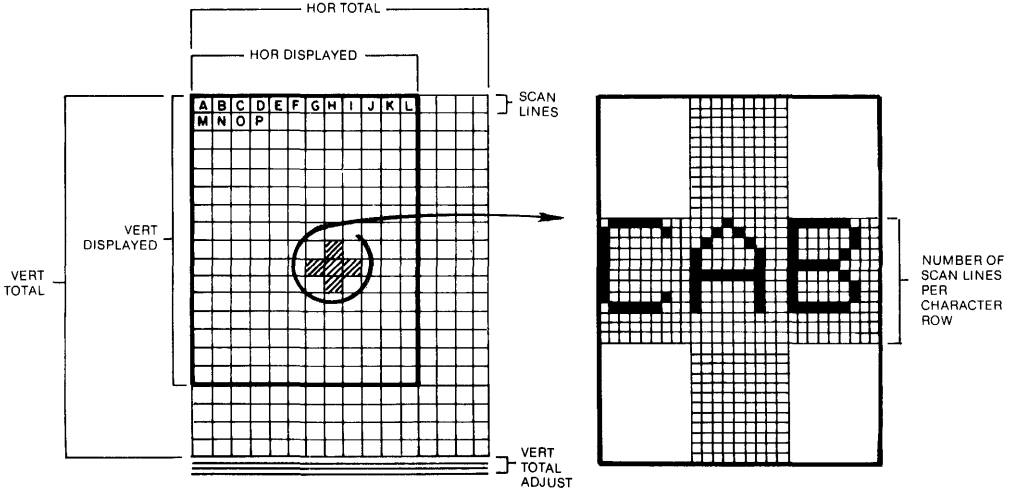


Figure 1. Video Display Format

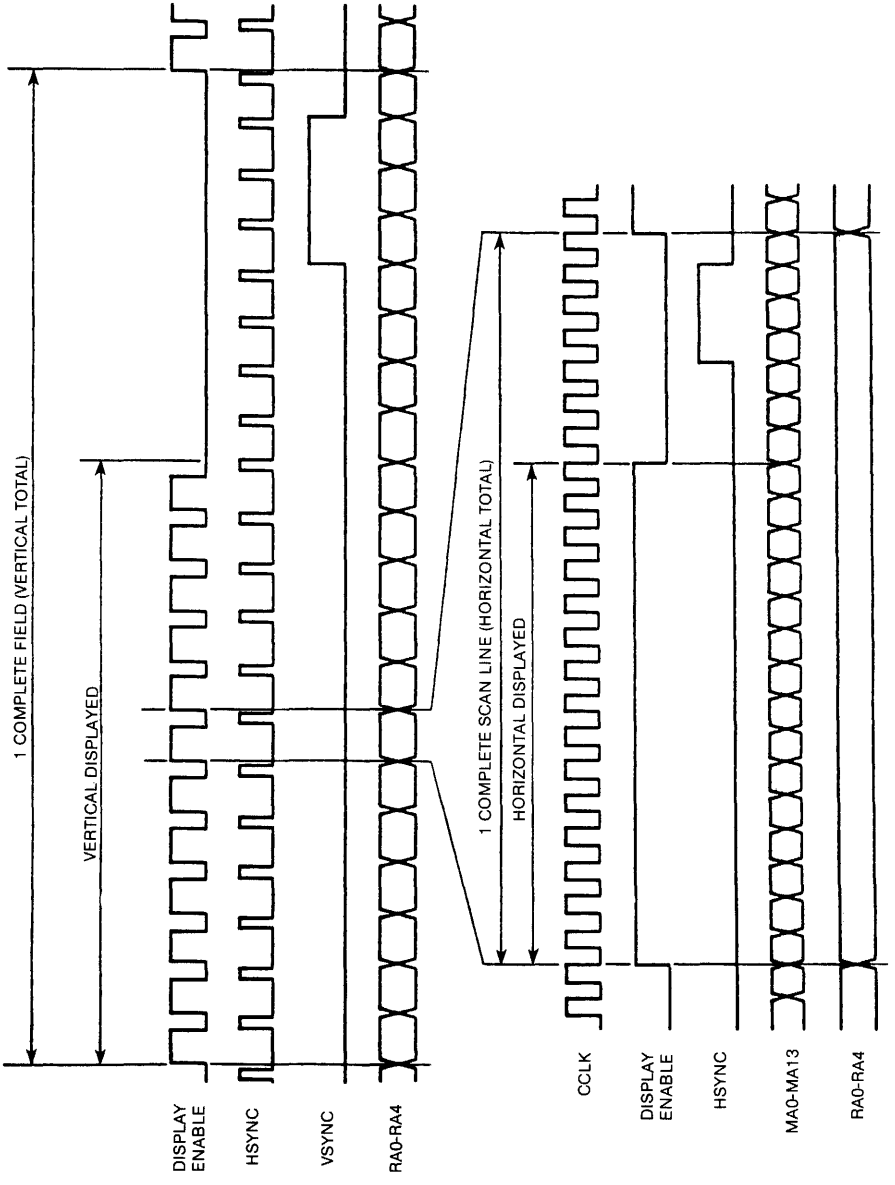
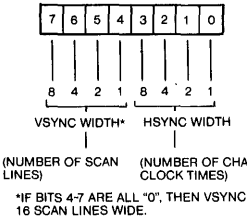


Figure 2. Vertical and Horizontal Timing

Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



Control of these parameters allows the 6545-1 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one-shot timing.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

$\overline{CS}$	RS	Address Reg 4	3	2	1	0	Reg. No.	Register Name	Stored Info	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1	—	—	—	—	—	—	—				✓	X	X	X	X	X	X	X	X
0	0	—	—	—	—	—	—	Address Reg.	Reg. No.		✓	X	X	X	A_4	A_3	A_2	A_1	A_0
0	0	—	—	—	—	—	—	Status Reg.		✓		U	L	V	X	X	X	X	X
0	1	0	0	0	0	0	R0	Horiz. Total	# Charac.		✓	■	■	■	■	■	■	■	■
0	1	0	0	0	0	1	R1	Horiz. Displayed	# Charac.		✓	■	■	■	■	■	■	■	■
0	1	0	0	0	1	0	R2	Horiz. Sync Position	# Charac.		✓	■	■	■	■	■	■	■	■
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	# Scan Lines & # Char. Times		✓	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert. Total	# Charac. Row		✓	X	■	■	■	■	■	■	■
0	1	0	0	1	0	1	R5	Vert. Total Adjust.	# Scan Lines		✓	X	X	X	■	■	■	■	■
0	1	0	0	1	1	0	R6	Vert. Displayed	# Charac. Rows		✓	X	■	■	■	■	■	■	■
0	1	0	0	1	1	1	R7	Vert. Sync Position	# Charac. Rows		✓	X	■	■	■	■	■	■	■
0	1	0	1	0	0	0	R8	Mode Control			✓	■	■	■	■	■	■	■	■
0	1	0	1	0	0	1	R9	Scan Line	# Scan Lines		✓	X	X	X	■	■	■	■	■
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		✓	X	B_1	B_0	■	■	■	■	■
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		✓	X	X	X	■	■	■	■	■
0	1	0	1	1	0	0	R12	Display Start Addr (H)			✓	X	X	■	■	■	■	■	■
0	1	0	1	1	0	1	R13	Display Start Addr (L)			✓	■	■	■	■	■	■	■	■
0	1	0	1	1	1	0	R14	Cursor Position (H)		✓	✓	X	X	■	■	■	■	■	■
0	1	0	1	1	1	1	R15	Cursor Position (L)		✓	✓	■	■	■	■	■	■	■	■
0	1	1	0	0	0	0	R16	Light Pen Reg. (H)		✓		X	X	■	■	■	■	■	■
0	1	1	0	0	0	1	R17	Light Pen Reg. (L)		✓		■	■	■	■	■	■	■	■

Notes ■ Designates binary bit
X Designates unusued bit. Reading this bit is always "O", except for R31, which does not drive the data bus at all, and for CS "1" which operates likewise.

Figure 3. Internal Register Summary

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

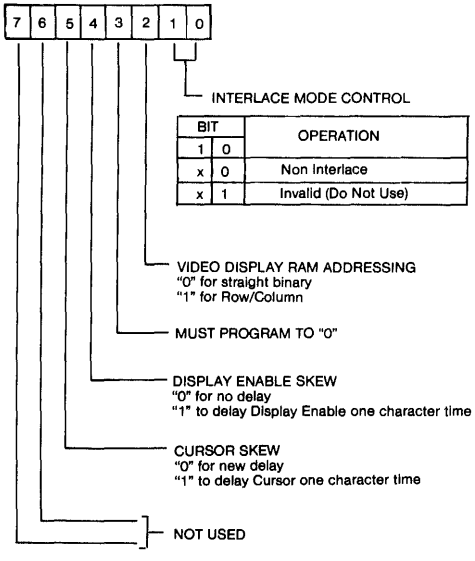
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

Mode Control (R8)

This register is used to select the operating modes of the 6545-1 and is outlined as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT		CURSOR MODE
6	5	
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 1/16 field rate
1	1	Blink at 1/32 field rate

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the 6545-1 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

DETAILED DESCRIPTION OF OPERATION

Register Formats

Register pairs R12/R13, R14/R15, and R16/R17 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/Column if register R8, bit 2 is a "1". In this case the low byte is the Character Column and the high byte is the Character Row.

Figure 4 illustrates the address sequence for the video display control for each mode.

Note from Figure 4 that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, but gaps exist. This requires that the system be equipped with more memory than is actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

In this way, the user may select whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column requires minimum software.

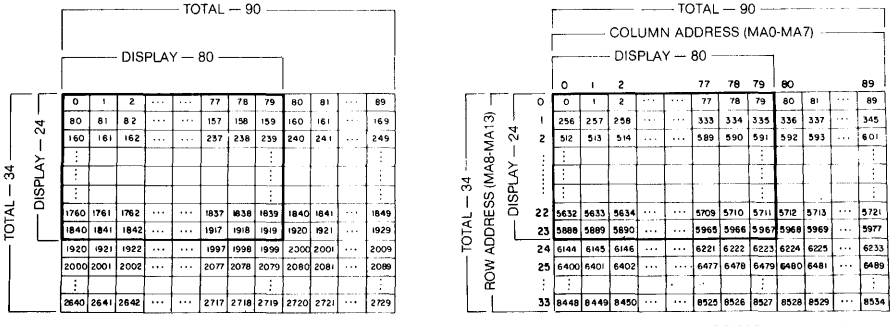
Memory Contention Schemes for Memory Addressing

From the diagram of Figure 4, it is clear that both the 6545-1 and the system MPU must be capable of addressing the video display memory. The 6545-1 repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirements are apparent:

- MPU Priority

  In this technique, the address lines to the video display memory are normally driven by the 6545-1 unless the MPU needs access, in which case the MPU addresses immediately override those from the 6545-1 and the MPU has immediate access.

- ø1/ø2 Memory Interleaving
  This method permits both the 6545-1 and the MPU access to the video display memory by time-sharing via the system o1 and ø2 clocks. During the ø1 portion of each cycle (the time when ø2 is low), the 6545-1 address



STRAIGHT BINARY ADDRESSING SEQUENCE **ROW/COLUMN ADDRESSING SEQUENCE**

Figure 4. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

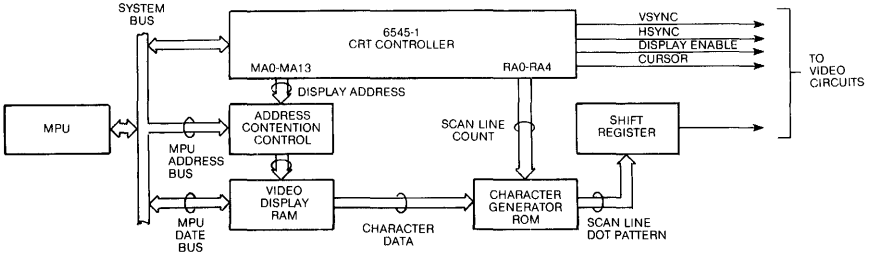


Figure 5. Typical System Configuration

outputs are gated to the video display memory. In the ø2 time, the MPU address lines are switched in. In this way, both the 6545-1 and the MPU have unimpeded access to the memory. Figure 6 illustrates the timings.

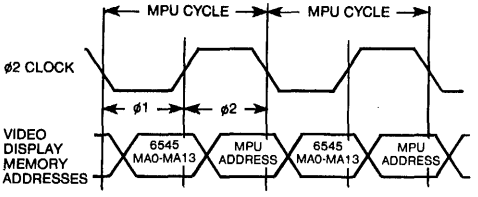


Figure 6. ø1/ø2 Interleaving

- Vertical Blanking

  With this approach, the address circuitry is identical to the case for MPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a "1"). In this way, no visible screen perturbations result.

Cursor and Display Enable Skew Control

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 7 illustrates the effect of the delays.

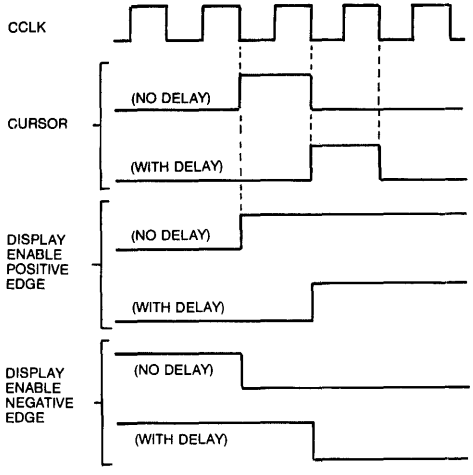


Figure 7. Cursor and Display Enable Skew

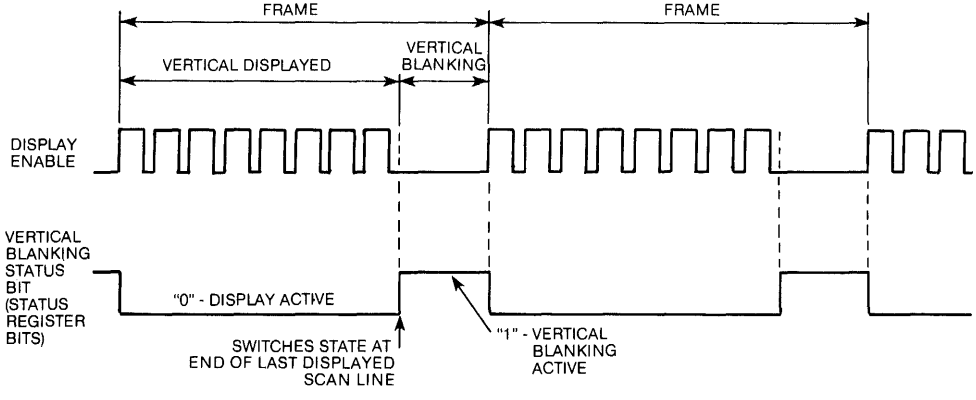


Figure 8. Operation of Vertical Blanking Status Bit

commodore semiconductor group

NMOS

MPS

6551

ASSYNCHRONOUS COMMUNICATION INTERFACE ADAPTER

6551 ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER

PERIPHERALS

CONCEPT:

The 6551 is an Asynchronous Communication Adapter (ACIA) intended to provide for interfacing the 6500/6800 microprocessor families to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

FEATURES:

- On-chip baud rate generator: 15 programmable baud rates derived from a standard 1.8432 MHz external crystal (50 to 19,200 baud).
- Programmable interrupt and status register to simplify software design.
- Single +5 volt power supply.
- Serial echo mode.
- False start bit detection.
- 8-bit bi-directional data bus for direct communication with the microprocessor.
- External 16x clock input for non-standard baud rates (up to 125 Kbaud).
- Programmable: word lengths; number of stop bits; and parity bit generation and detection.
- Data set and modem control signals provided.
- Parity: (odd, even, none, mark, space).
- Full-duplex or half-duplex operation.
- 5, 6, 7, 8 and 9 bit transmission.

ORDER NUMBER

MXS 6551 —

- FREQUENCY RANGE
  - NO SUFFIX = 1 MHz
  - A = 2 MHz
  - B = 3 MHz
- PACKAGE DESIGNATOR
  - C = CERAMIC
  - P = PLASTIC

6551 PIN CONFIGURATION

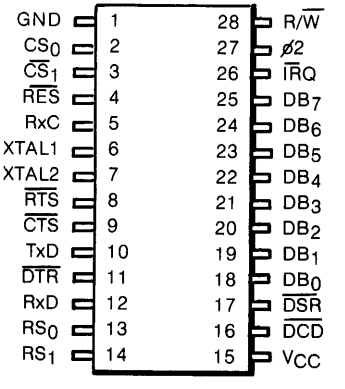
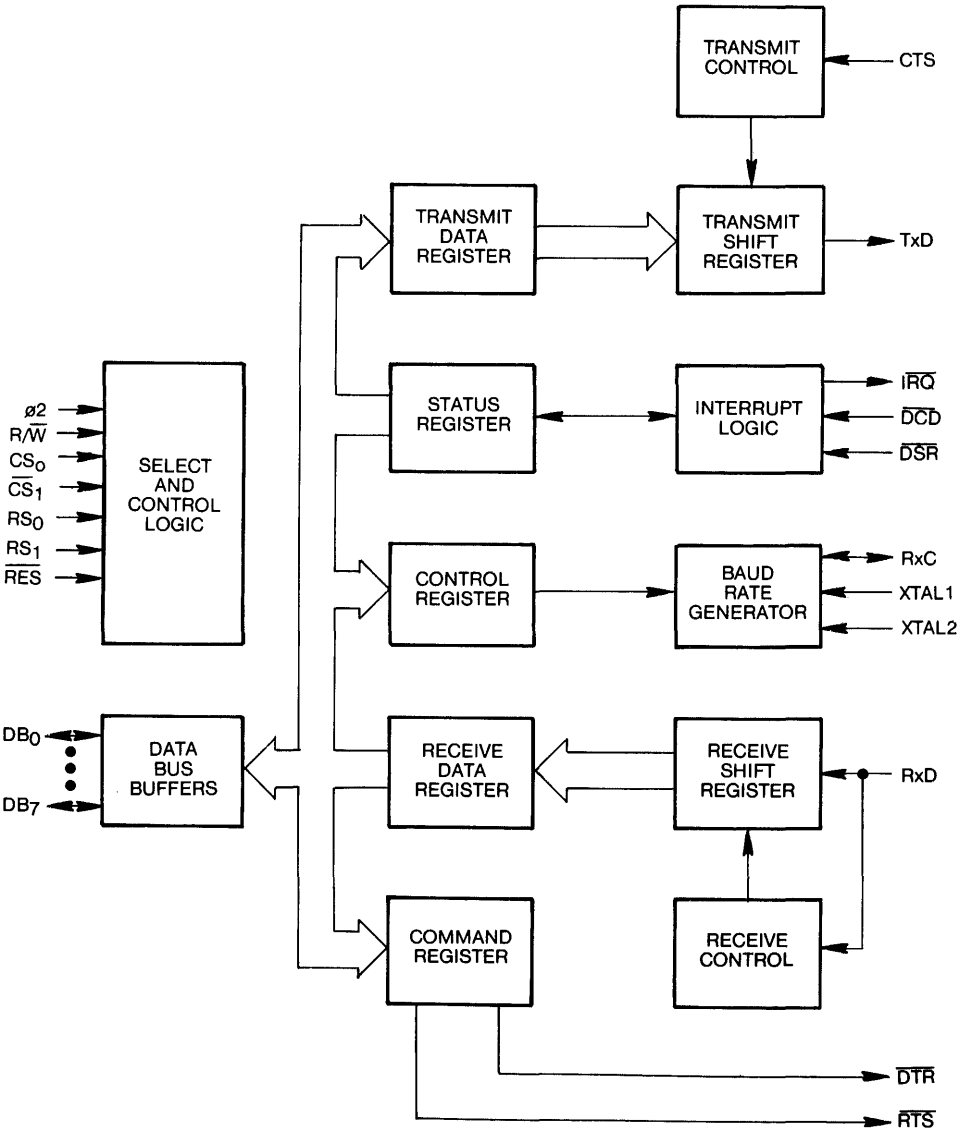


Figure 1. Block Diagram



MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input/Output Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	−55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

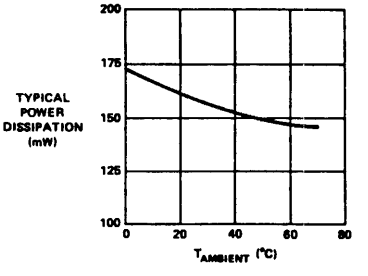
COMMENT

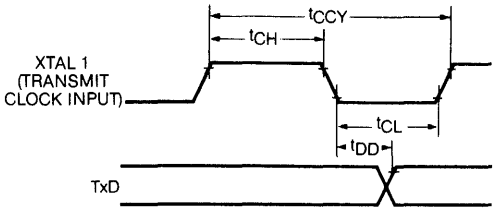
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V + 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Input Leakage Current: V_{IN}=0 to 5V. (ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS_0}$, CS_1, RS_0, RS_1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	I_{IN}	—	±1.0	±2.5	µA
Input Leakage Current for High Impedance State (Three State)	I_{TSI}	—	±2.0	±10.0	µA
Output High Voltage: I_{LOAD}=−100µA	V_{OH}	2.4	—	—	V
Output Low Voltage: I_{LOAD} = 1.6mA (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	V_{OL}	—	—	0.4	V
Output High Current (Sourcing): V_{OH}=2.4V	I_{OH}	−250	—	—	µA
Output Low Current (Sinking): V_{OL}=0.4V	I_{OL}	1.6	—	—	µA
Output Leakage Current (off state): V_{OUT}=5V ($\overline{IRQ}$)	I_{OFF}	—	1.0	10.0	µA
Clock Capacitance (ø2)	C_{CLK}	—	—	20	pF
Input Capacitance (except XTAL1 and XTAL2)	C_{IN}	—	—	10	pF
Output Capacitance	C_{OUT}	—	—	10	pF
Power Dissipation	P_D	—	170	300	mw

Power Dissipation vs Temperature





NOTE: TxD rate is 1/16 TxC rate.

Figure 4a. Transmit Timing with External Clock

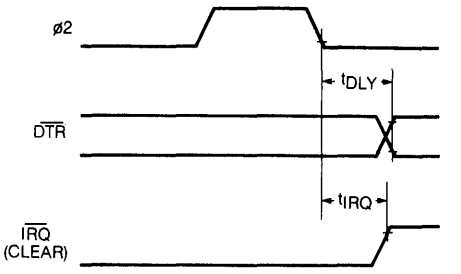
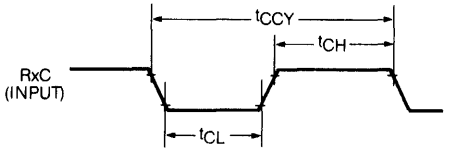


Figure 4b. Interrupt and RTS Timing



NOTE: RxD rate is 1/16 RxC rate.

Figure 4c. Receive External Clock Timing

TRANSMIT/RECEIVE CHARACTERISTICS

Characteristic	Symbol	6551 Min	6551 Max	6551A Min	6551A Max	Unit
Transmit/Receive Clock Rate	t_{CCY}	400*	—	400*	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	175	—	ns
Transmit/Receive Clock Low Time	t_{CL}	175	—	175	—	ns
XTAL1 to TxD Propagation Delay	t_{DD}	—	500	—	500	ns
$\overline{RTS}$ Propagation Delay	t_{RTS}	—	500	—	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	500	—	500	ns

(t_r, t_f = 10 to 30 nsec)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

INTERFACE SIGNAL DESCRIPTION

$\overline{RES}$ (Reset)
During system initialization a low on the $\overline{RES}$ input will cause internal registers to be cleared.

ø2 (Input Clock)
The input clock is the system ø2 clock and is used to trigger all data transfers between the system microprocessor and the 6551.

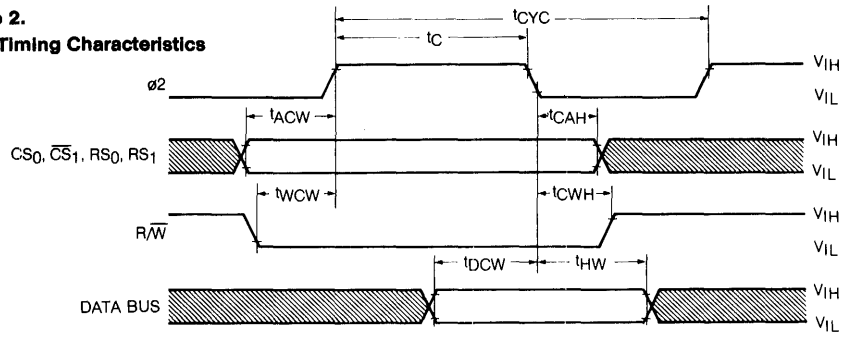
R/$\overline{W}$ (Read/Write)
The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the 6551. A low on the R/$\overline{W}$ pin allows a write to the 6551.

$\overline{IRQ}$ (Interrupt Request)
The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0 — DB_7(Data Bus)
The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the 6551. These lines are bi-directional and are normally high-impedance except during Read cycles when selected.

CS_0, $\overline{CS_1}$ (Chip Selects)
The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The 6551 is selected when CS_0 is high and $\overline{CS_1}$ is low.

Figure 2.
Write Timing Characteristics



(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	6551 Min	6551 Max	6551A Min	6551A Max	Unit
Cycle Time	t_{CYC}	1.0	40	0.5	40	µs
ø2 Pulse Width	t_C	470	—	235	—	ns
Address Set-Up Time	t_{ACW}	180	—	90	—	ns
Address Hold Time	t_{CAH}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	180	—	90	—	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	300	—	150	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	ns

(t_r and t_f = 10 to 30 ns)

Clock Generation

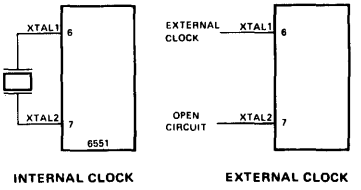
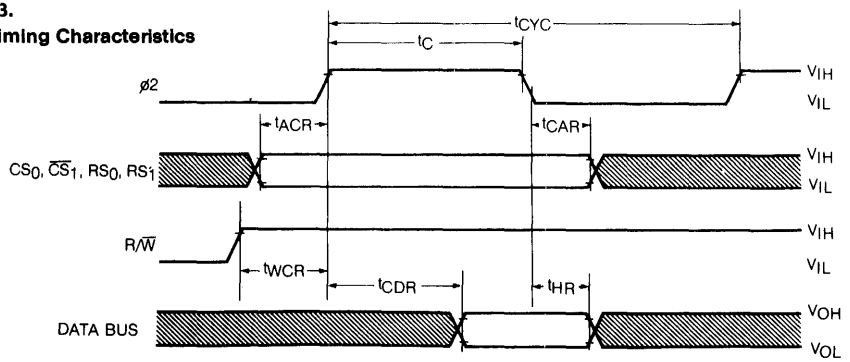


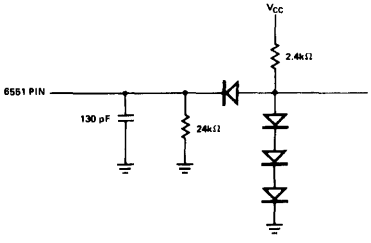
Figure 3.
Read Timing Characteristics



(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	6551 Min	6551 Max	6551A Min	6551A Max	Unit
Cycle Time	t_{CYC}	1.0	40	0.5	40	µs
Pulse Width (ø2)	t_C	470	—	235	—	ns
Address Set-Up Time	t_{ACR}	180	—	90	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCR}	180	—	90	—	ns
Read Access Time	t_{CDR}	—	395	—	200	ns
Read Hold Time	t_{HR}	10	—	10	—	ns

(t_r and t_f = 10 to 30 ns)



Test Load for Data Bus (DB_0-DB_7)
$\overline{T}$ x D, $\overline{DTR}$, RTS Outputs

RS_0, RS_1 (Register Selects)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various 6551 internal registers. The following table indicates the internal register select coding:

RS_1	RS_0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear the 6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$) and these differences are described in the individual register definitions.

ACIA/MODEM INTERFACE SIGNAL DESCRIPTION

XTAL1, XTAL2 (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin, in which case the XTAL2 pin must float. XTAL1 is the input pin for the transmit clock.

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ outpin pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready)

This ouput pin is used to indicate the status of the 6551 to the modem. A low on $\overline{DTR}$ indicates the 6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input pin is used to indicate to the 6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready." $\overline{DSR}$ is a high-impedance input and must not be a no-connect. If unused, it should be driven high or low, but not switched.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{DSR}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 6 will reflect the new level. The state of DSR does not affect either Transmitter or Receiver operation.

$\overline{DCD}$ (Data Carrier Detect)

The $\overline{DCD}$ input pin is used to indicate to the 6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that is is not. $\overline{DCD}$, like $\overline{DSR}$, is a high-impedance input and must not be a no-connect.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{DCD}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 5 will reflect the new level. The state of $\overline{DCD}$ does not affect Transmitter operation, but must be low for the Receiver to operate.

INTERNAL ORGANIZATION

The Transmitter/Receiver sections of the 6551 are depicted by the block diagram in Figure 5.

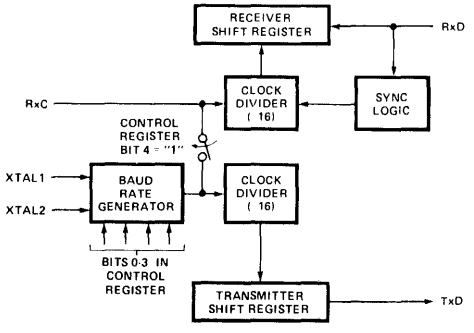


Figure 5. Transmitter/Receiver Clock Circuits

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the 6551.

CONTROL REGISTER

The Control Register is used to select the desired mode for the 6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 6.

CONTROL REGISTER

7	6	5	4	3	2	1	0

STOP BITS

0 = 1 Stop Bit
1 = 2 Stop Bits
1 Stop Bit if Word Length = 8 Bits and Parity*
1½ Stop Bits if Word Length = 5 Bits and No Parity.

WORD LENGTH

BIT 6	BIT 5	DATA WORD LENGTH
0	0	8
0	1	7
1	0	6
1	1	5

RECEIVER CLOCK SOURCE

0 = External Receiver Clock
1 = Baud Rate Generator

BAUD RATE GENERATOR

0	0	0	0	16x EXTERNAL CLOCK
0	0	0	1	50 BAUD
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

*This allows for 9-bit transmission (8 data bits plus parity).

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	–	–	–	–	–

Figure 6. Control Register Format

COMMAND REGISTER

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 7.

COMMAND REGISTER

7	6	5	4	3	2	1	0

PARITY CHECK CONTROLS

BIT 7	BIT 6	BIT 5	OPERATION
–	–	0	Parity Disabled - No Parity Bit Generated - No Parity Bit Received
0	0	1	Odd Parity Receiver and Transmitter
0	1	1	Even Parity Receiver and Transmitter
1	0	1	Mark Parity Bit Transmitted, Parity Check Disabled
1	1	1	Space Parity Bit Transmitted, Parity Check Disabled

DATA TERMINAL READY

0 = Disable Receiver and All Interrupts ($\overline{DTR}$ high)
1 = Enable Receiver and All Interrupts ($\overline{DTR}$ low)

RECEIVER INTERRUPT ENABLE

0 = $\overline{IRQ}$ Interrupt Enabled from Bit 3 of Status Register
1 = $\overline{IRQ}$ Interrupt Disabled

TRANSMITTER CONTROLS

BIT 3	BIT 2	TRANSMIT INTERRUPT	$\overline{RTS}$ LEVEL	TRANSMITTER
0	0	Disabled	High	Off
0	1	Enabled	Low	On
1	0	Disabled	Low	On
1	1	Disabled	Low	Transmit BRK

NORMAL/ECHO MODE FOR RECEIVER

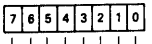
0 = Normal
1 = Echo (Bits 2 and 3 must be "0")

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	0	0	0	0	0

Figure 7. Command Register Format

STATUS REGISTER

The Status Register is used to indicate to the processor the status of various 6551 functions and is outlined in Figure 8.



STATUS	SET BY	CLEARED BY
Parity Error*	0 = No Error 1 = Error	Self Clearing**
Framing Error*	0 = No Error 1 = Error	Self Clearing**
Overrun*	0 = No Error 1 = Error	Self Clearing**
Receive Data Register Full	0 = Not Full 1 = Full	Read Receive Data Register
Transmit Data Register Empty	0 = Not Empty 1 = Empty	Write Transmit Data Register
$\overline{DCD}$	0 = $\overline{DCD}$ Low 1 = $\overline{DCD}$ High	Not Resettable Reflects $\overline{DCD}$ State
$\overline{DSR}$	0 = $\overline{DSR}$ Low 1 = $\overline{DSR}$ High	Not Resettable Reflects $\overline{DSR}$ State
IRQ	0 = No Interrupt 1 = Interrupt	Read Status Register

*NO INTERRUPT GENERATED FOR THESE CONDITIONS.
**CLEARED AUTOMATICALLY AFTER A READ OF RDR AND THE NEXT ERROR FREE RECEIPT OF DATA.

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	–	–	1	0	0	0	0
PROGRAM RESET	–	–	–		–	0	–	

Figure 8. Status Register Format

TRANSMIT AND RECEIVE DATA REGISTERS

These registers are used as temporary data storage for the 6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Figure 9 illustrates a single transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

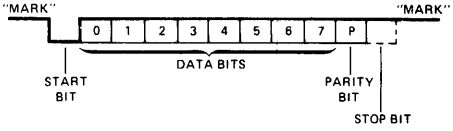


Figure 9 Serial Data Stream Example

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NMOS

MPS

2316

STATIC READ ONLY MEMORY (2048x8)

2316 STATIC READ ONLY MEMORY (2048x8)

DESCRIPTION

The 2316 high performance read only memory is organized 2048 words by 8 bits with access times of less than 350 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations.

The 2316 operates totally asynchronously. No clock input is required. The three programmable chip select inputs allow eight 16K ROMS to be OR-tied without external decoding.

Designed to replace two 2708 8K EPROMS, the 2316 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMS after prototyping with EPROMS.

- 400mV Noise Immunity on Inputs
- 2048 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 450 ns, 350 ns
- Totally Static Operation
- TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- Pin Compatible with 2716 EPROM
- Replacement for two 2708s
- 2708/2716 EPROMS Accepted as Program Data Inputs

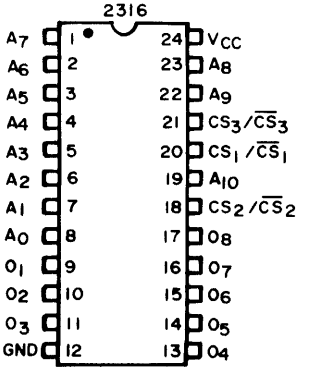
ORDERING INFORMATION

MXS 2316 ____

FREQUENCY RANGE
NO SUFFIX = 450ns
A = 350ns

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

PIN CONFIGURATION



ROMS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	°C to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
Applied Output Voltage	−0.5V to +7.0V
Applied Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D. C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%, unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_{CC1}	Power Supply Current		100	mA	$V_{IN} = V_{CC}, V_O$ = Open, T_A = 0°C
I_{CC2}	Power Supply Current		95	mA	$V_{IN} = V_{CC}, V_O$ = Open, T_A = 25°C
I_O	Output Leakage Current		10	μA	Chip Deselected, V_O = 0 to V_{CC}
I_I	Input Load Current		10	μA	V_{CC} = Max. V_{IN} = 0 to V_{CC}
V_{OL}	Output Low Voltage		0.4	Volts	V_{CC} = Min. I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4		Volts	V_{CC} = Min. I_{OH} = −400μA
V_{IL}	Input Low Voltage	−0.5	0.8	Volts	See Note 1
V_{IH}	Input High Voltage	2.0	V_{CC}+1	Volts	

A. C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%, unless otherwise specified)

		2316		2316A			
Symbol	Parameter	Min.	Max.	Min.	Max.	Units	Test Conditions
t_{ACC}	Address Access Time		450		350	ns	
t_{CO}	Chip Select Delay		200		200	ns	
t_{DF}	Chip Deselect Delay		175		175	ns	See Note 2
t_{OH}	Previous Data Valid After Address Change Delay	40		40		ns	

CAPACITANCE (T_A = 25°C, f = 1.0MHz, See Note 3)

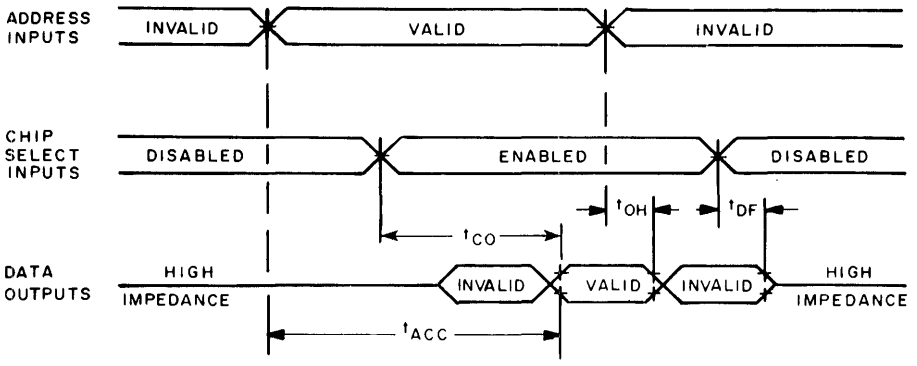
Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_{IN}	Input Capacitance		8	pF	All Pins except Pin under
C_{OUT}	Output Capacitance		10	pF	Test Tied to AC Ground

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

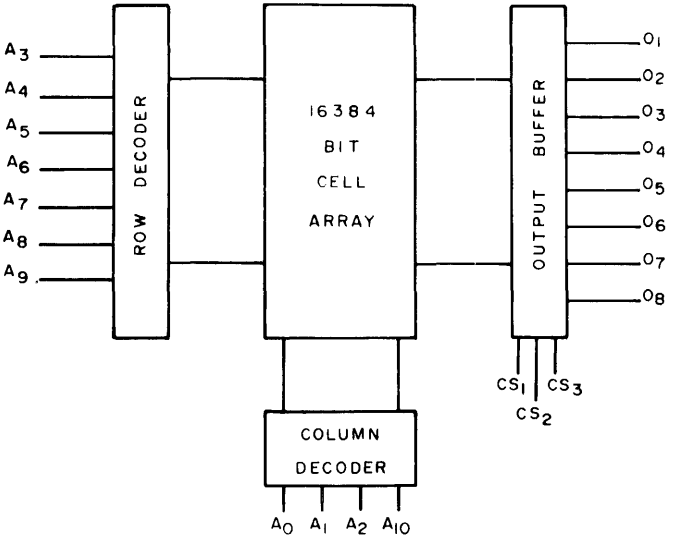
Note 2: Loading 1 TTL + 100 pF, input transition time: 20 ns
Timing measurement levels: input 1.5V, output 0.8V and 2.0V.

Note 3: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAMS

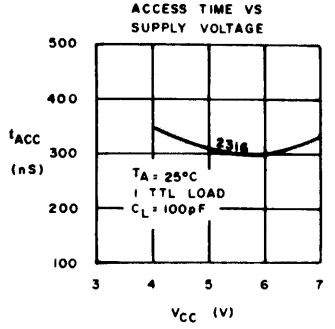


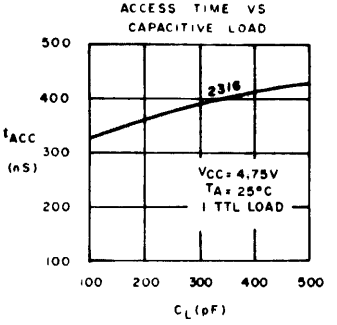
BLOCK DIAGRAM

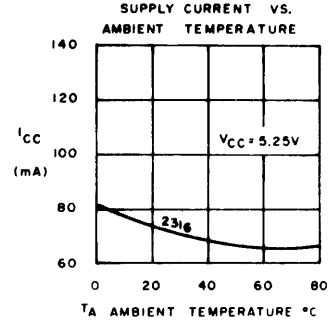


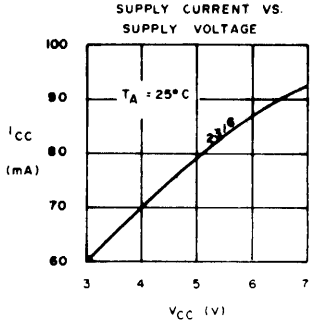
ROMs

TYPICAL CHARACTERISTICS





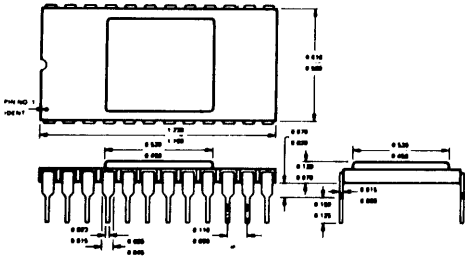




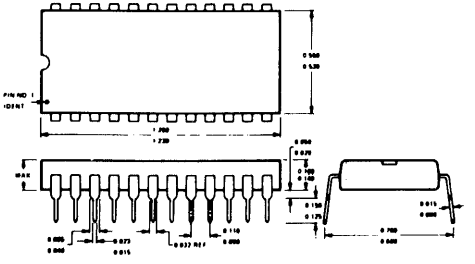
ROMS

PACKAGING DIAGRAM

CERAMIC PACKAGE



MOLDED PACKAGE



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NMOS

MPS

2332

STATIC READ ONLY MEMORY (4096x8)

2332 STATIC READ ONLY MEMORY (4096x8)

DESCRIPTION

The 2332 high performance read only memory is organized 4096 words by 8 bits with access times of less than 350 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels.

The 2332 operates totally asynchronously. No clock input is required. The two programmable chip select inputs allow four 32K ROMS to be OR-tied without external decoding.

Designed to replace two 2716 16K EPROMS, the 2332 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMS after prototyping with EPROMS.

- 4096 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 2332 450 ns
  2332A 350 ns
- Completely TTL Compatible
- Totally Static Operation
- Three-State Outputs for Wire-OR Expansion
- Two Programmable Chip Selects
- Pin Compatible with 2716 & 2732 EPROM
- Replacement for Two 2716s
- 2708/2716 EPROMS Accepted as Program Data Inputs
- 400mV Noise Immunity on Inputs

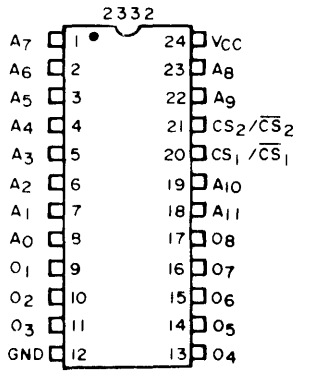
ORDERING INFORMATION

MXS 2332 ___

FREQUENCY RANGE
NO SUFFIX = 450ns
A = 350ns

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

PIN CONFIGURATION



ROMs

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0° to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
Applied Output Voltage	−0.5V to +7.0V
Applied Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_{CC1}	Power Supply Current		100	mA	$V_{IN} = V_{CC}$, V_O = Open, T_A = 0°C
I_{CC2}	Power Supply Current		95	mA	$V_{IN} = V_{CC}$, V_O = Open, T_A = 25°C
I_O	Output Leakage Current		10	µA	Chip Deselected, V_O = O to V_{CC}
I_I	Input Load Current		10	µA	V_{CC} = Max. V_{IN} = O to V_{CC}
V_{OL}	Output Low Voltage		0.4	Volts	V_{CC} = Min. I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4		Volts	V_{CC} = Min. I_{OH} = −400µA
V_{IL}	Input Low Voltage	−0.5	0.8	Volts	See note 1
V_{IH}	Input High Voltage	2.0	V_{CC}+1	Volts	

A. C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% (unless otherwise specified)

Symbol	Parameter	2332		2332A		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{ACC}	Address Access Time		450		350	ns	See Note 2
t_{CO}	Chip Select Delay		200		200	ns	
t_{DF}	Chip Deselect Delay		175		175	ns	
t_{OH}	Previous Data Valid After Address Change Delay	40		40		ns	

CAPACITANCE

T_A = 25°C, f = 1.0MHz, See Note 3

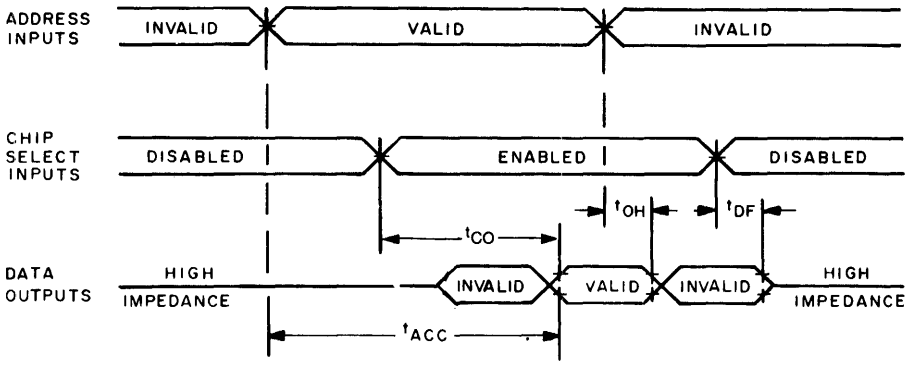
Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_{IN}	Input Capacitance		8	pF	All Pins except Pin under Test Tied to AC Ground
C_{OUT}	Output Capacitance		10	pF	

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

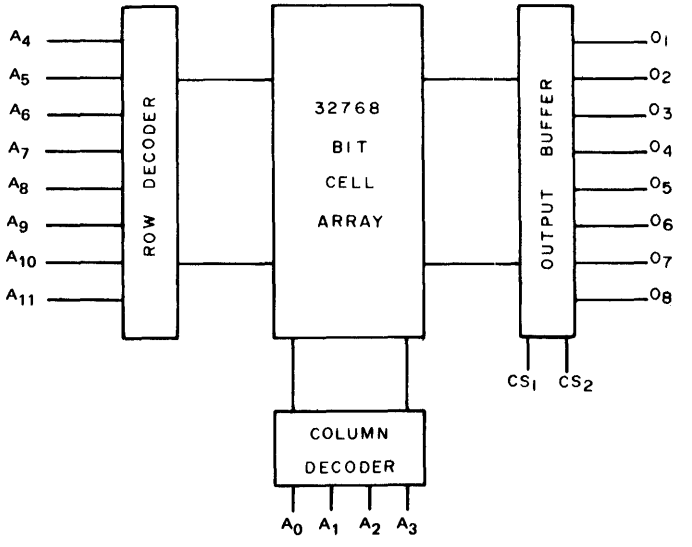
Note 2: Loading 1 TTL + 100 pF, input transition time: 20 ns.
Timing measurement levels: input 1.5V, output 0.8V and 2.0V. C_L = 100 pF.

Note 3: This parameter is periodically sampled and is not 100% tested.

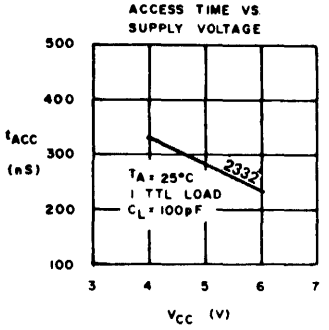
TIMING DIAGRAM

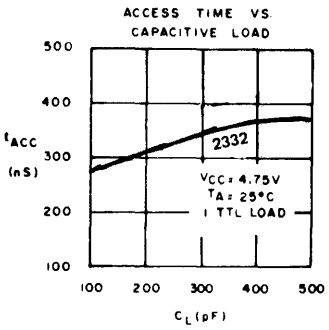


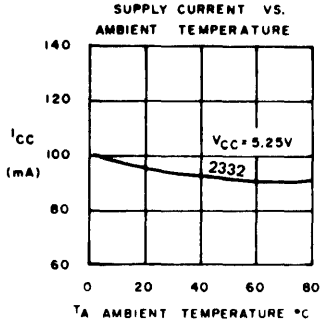
BLOCK DIAGRAM

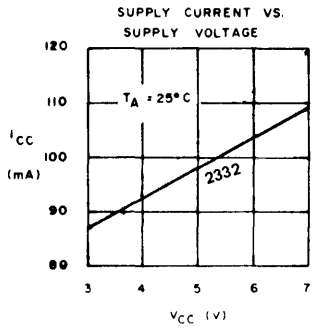


TYPICAL CHARACTERISTICS









commodore semiconductor group

NMOS

MPS

2333

STATIC READ ONLY MEMORY (4096x8)

2333 STATIC READ ONLY MEMORY (4096x8)

DESCRIPTION

The 2333 high performance read only memory is organized 4096 words by 8 bits with access times of less than 350 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels.

The 2333 operates totally asynchronously. No clock input is required. The two programmable chip select inputs allow four 32K ROMS to be OR-tied without external decoding.

Designed to replace two 2716 16K EPROMS, the 2333 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMS after prototyping with EPROMS.

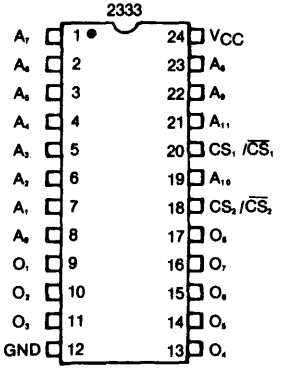
- 4096 x 8 Bit Organization
- Single +5 Volt Supply
- Three Week Prototype Turnaround
- Access Time—2333 450 ns
  2333A 350 ns
- Completely TTL Compatible
- Totally Static Operation
- Three-State Outputs for Wire-OR Expansion
- Two Programmable Chip Selects
- Pin Compatible with 2716 & 2732 (INTEL) EPROMS
- Replacement for Two 2716s
- 2708/2716 EPROMS Accepted as Program Data Inputs
- 400 mV Noise Immunity on Inputs

ORDERING INFORMATION:

Part Number*	Package Type	Access Time	Temperature Range
MPS2333	Molded	450 ns	0°C to +70°C
MPS2333A	Molded	350 ns	0°C to +70°C
MCS2333	Ceramic	450 ns	0°C to +70°C
MCS2333A	Ceramic	350 ns	0°C to +70°C

*Final Part Number will be assigned by manufacturer

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0° to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
Applied Output Voltage	−0.5V to +7.0V
Applied Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_{CC1}	Power Supply Current		125	mA	$V_{IN} = V_{CC}$, V_O = Open, T_A = 0 C
I_{CC2}	Power Supply Current		120	mA	$V_{IN} = V_{CC}$, V_O = Open, T_A = 25 C
I_O	Output Leakage Current		10	µA	Chip Deselected, V_O = O to V_{CC}
I_I	Input Load Current		10	µA	V_{CC} = Max. V_{IN} = O to V_{CC}
V_{OL}	Output Low Voltage		0.4	Volts	V_{CC} = Min. I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4		Volts	V_{CC} = Min. I_{OH} = −400µA
V_{IL}	Input Low Voltage	−0.5	0.8	Volts	See note 1
V_{IH}	Input High Voltage	2.0	V_{CC}+1	Volts	

A. C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% (unless otherwise specified)

Symbol	Parameter	2333		2333A		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{ACC}	Address Access Time		450		350	ns	See Note 2
t_{CO}	Chip Select Delay		200		200	ns	
t_{DF}	Chip Deselect Delay		175		175	ns	
t_{OH}	Previous Data Valid After Address Change Delay	40		40		ns	

CAPACITANCE

T_A = 25°C, f = 1.0MHz, See Note 3

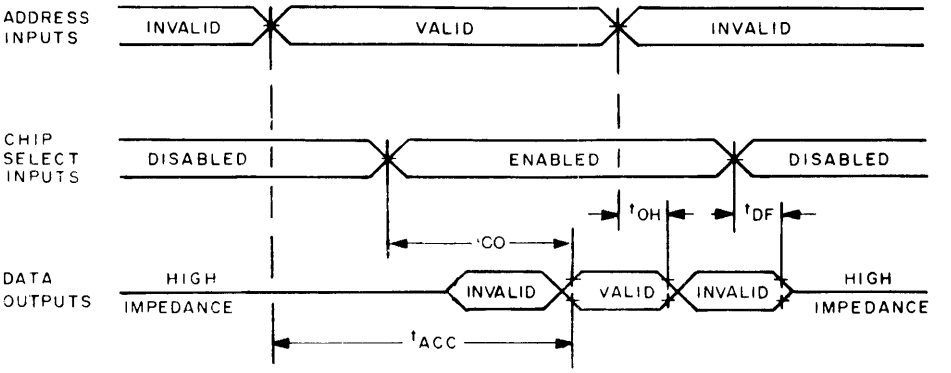
Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_{IN}	Input Capacitance		8	pF	All Pins except Pin under Test Tied to AC Ground
C_{OUT}	Output Capacitance		10	pF	

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

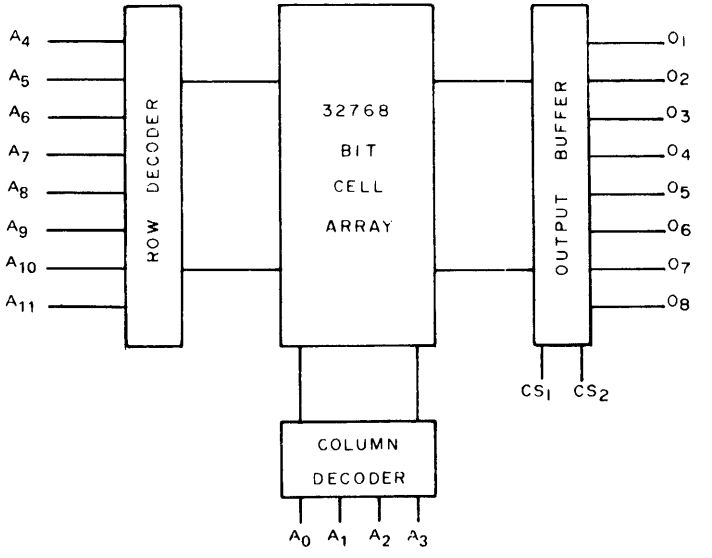
Note 2: Loading 1 TTL + 100 pF, input transition time: 20 ns.
Timing measurement levels: input 1.5V, output 0.8V and 2.0V. C_L = 100 pF.

Note 3: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM

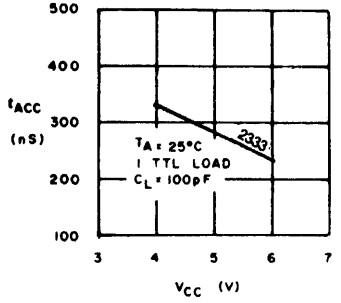


BLOCK DIAGRAM

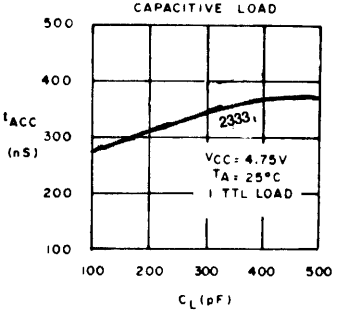


TYPICAL CHARACTERISTICS

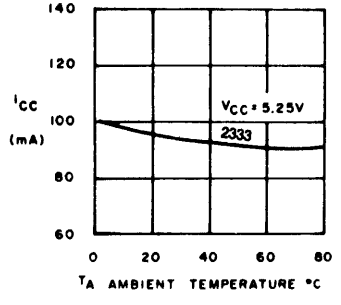
ACCESS TIME VS. SUPPLY VOLTAGE



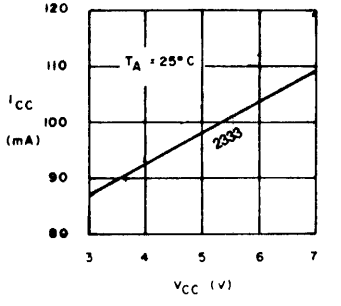
ACCESS TIME VS. CAPACITIVE LOAD



SUPPLY CURRENT VS. AMBIENT TEMPERATURE



SUPPLY CURRENT VS. SUPPLY VOLTAGE



ROMs

commodore semiconductor group

NMOS

MPS

2364

STATIC READ ONLY MEMORY (8192x8)

2364 STATIC READ ONLY MEMORY (8192x8)

DESCRIPTION

The 2364 high performance read only memory is organized 8192 words by 8 bits with access times of less than 350 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels.

The 2364 operates totally asynchronously. No clock input is required. The programmable chip select input allows two 64K ROMS to be OR-tied without external decoding.

Designed to replace two 2732 32K EPROMS, the 2364 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMS after prototyping with EPROMS.

- 8192 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 450 ns, 350 ns
- Completely TTL Compatible
- Totally Static Operation
- Three-State Outputs for Wire-OR Expansion
- One Programmable Chip Select
- Pin Compatible with 2716 & 2732 EPROM
- Replacement for Two 2732s
- 2716/2732 EPROMS Accepted as Program Data Inputs
- 400mV Noise Immunity on Inputs

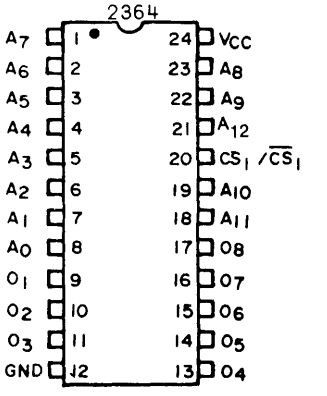
ORDERING INFORMATION

MXS 2364 ____

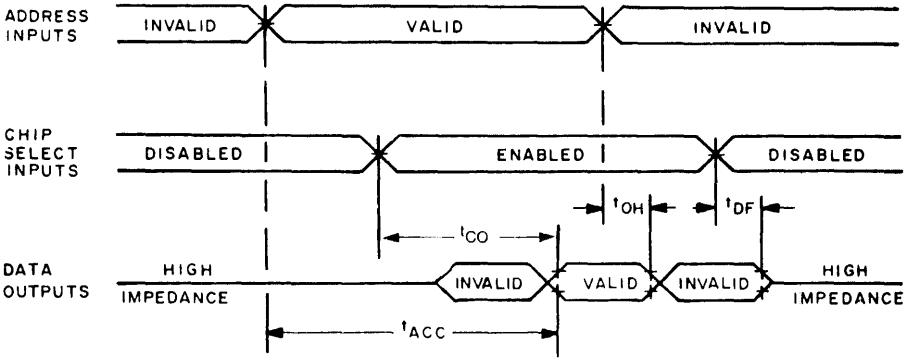
FREQUENCY RANGE
NO SUFFIX = 450ns
A = 350ns

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

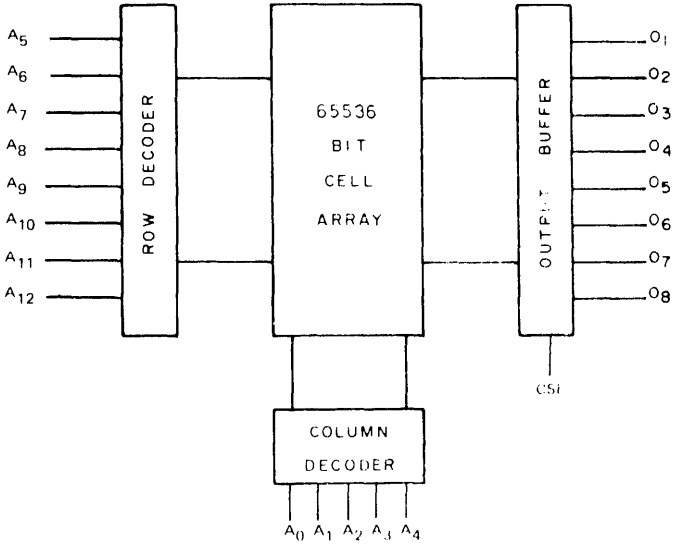
PIN CONFIGURATION



TIMING DIAGRAM



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	°C to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
Applied Output Voltage	−0.5V to +7.0V
Applied Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D. C. CHARACTERISTICS (T_A = 0 C to +70 C, V_{CC} = 5.0V ± 5%, unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_{CC1}	Power Supply Current		100	mA	$V_{IN} = V_{CC}, V_O$ = Open, T_A = 0°C
I_{CC2}	Power Supply Current		95	mA	$V_{IN} = V_{CC}, V_O$ = Open, T_A = 25°C
I_O	Output Leakage Current		10	µA	Chip Deselected, V_O = 0 to V_{CC}
I_I	Input Load Current		10	µA	V_{CC} = Max. V_{IN} = 0 to V_{CC}
V_{OL}	Output Low Voltage		0.4	Volts	V_{CC} = Min. I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4		Volts	V_{CC} = Min. I_{OH} = −400µA
V_{IL}	Input Low Voltage	−0.5	0.8	Volts	See Note 1
V_{IH}	Input High Voltage	2.0	V_{CC}+1	Volts	

A. C. CHARACTERISTICS (T_A = 0 C to +70 C, V_{CC} = 5.0V ± 5%, unless otherwise specified)

		2364		2364A			
Symbol	Parameter	Min.	Max.	Min.	Max.	Units	Test Conditions
t_{ACC}	Address Access Time		450		350	ns	
t_{CO}	Chip Select Delay		200		200	ns	
t_{DF}	Chip Deselect Delay		175		175	ns	See Note 2
t_{OH}	Previous Data Valid After Address Change Delay	40		40		ns	

CAPACITANCE (T_A = 25 C, f = 1.0MHz, See Note 3)

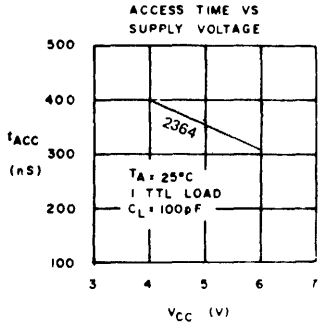
Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_{IN}	Input Capacitance		8	pF	All Pins except Pin under
C_{OUT}	Output Capacitance		10	pF	Test Tied to AC Ground

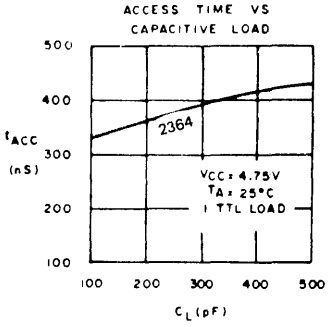
Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

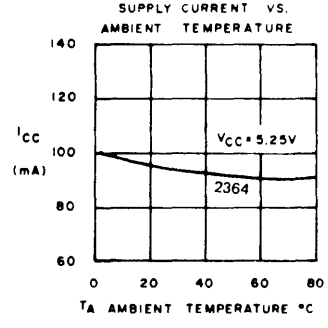
Note 2: Loading 1 TTL + 100 pF, input transition time: 20 ns
Timing measurement levels: input 1.5V, output 0.8V and 2.0V. C_L = 100 pF

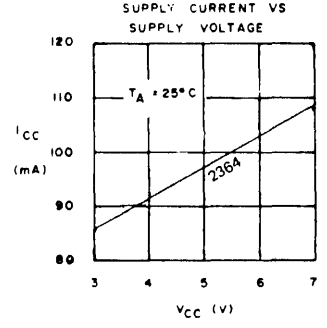
Note 3: This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS









commodore semiconductor group

NMOS

MPS

23128

128K STATIC READ ONLY MEMORY (19384x8)

23128 — 128K STATIC READ ONLY MEMORY (16384x8)

DESCRIPTION

The 23128 high performance read only memory is organized as 16384 words by 8 bits. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels.

The 23128 operates totally asynchronously. No clock input is required. The 23128 access time is 250 ns max.

The 23128 offers a power down feature which is controlled by $\overline{CE}$. When the $\overline{CE}$ pin goes high the device will automatically power down and remain in a low power mode as long as $\overline{CE}$ remains high.

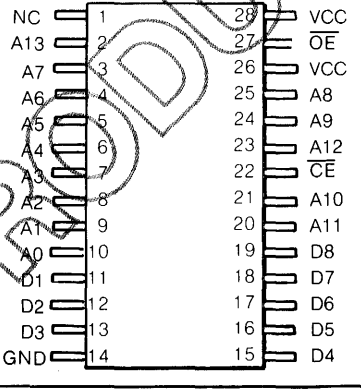
Designed to replace two 64K EPROMs, the 23128 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

FEATURES

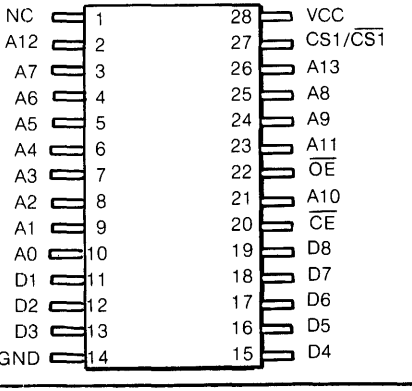
- Output Enable Function ($\overline{OE}$)
- 16384x8 Bit organization
- Single +5 Volt Supply
- Completely TTL Compatible
- Totally Static Operation
- Three State Outputs for Wire-OR Expansion
- Pin Compatible with both 25XX and 27XX EPROM families
- 23128 is pin compatible with 27128 (JEDEC Standard)
- 2328 is pin compatible with 2528 (TI version)
- 400 mV Noise Immunity on Inputs
- Automatic power down ($\overline{CE}$)

PIN CONFIGURATION

2328



23128



commodore semiconductor group

NMOS

MMS
6508-1
MPS 6508
BASED
MICROMODULE
BOARD

MMS 6508-1 MICROMODULE BOARD

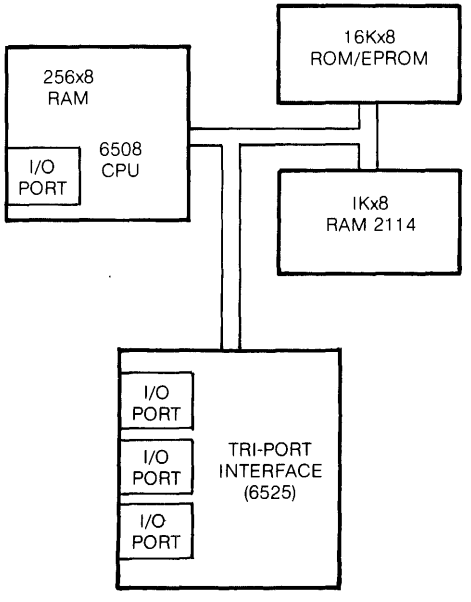
Description

The MMS 6508-1 is the first in a family of single board microcomputers, designed for easy system development. The heart of this micromodule is the new 6508 microprocessor. It has as enhancements, an on-chip eight-bit I/O port, 256 bytes of RAM, and a tri-state address bus.

The micromodule board has four sockets that allow the user to have from 8 to 16K bytes of program memory. The sockets are designed to accept ROMs, as well as 2716 or 2532 EPROMS, using +5v supply.

The micromodule board also features the new 6525 tri-port interface. This chip has three eight-bit I/O ports that are bit programmable as twenty-four I/O lines, or sixteen I/O lines, five priority interrupts and two handshake lines.

Block Diagram



Features

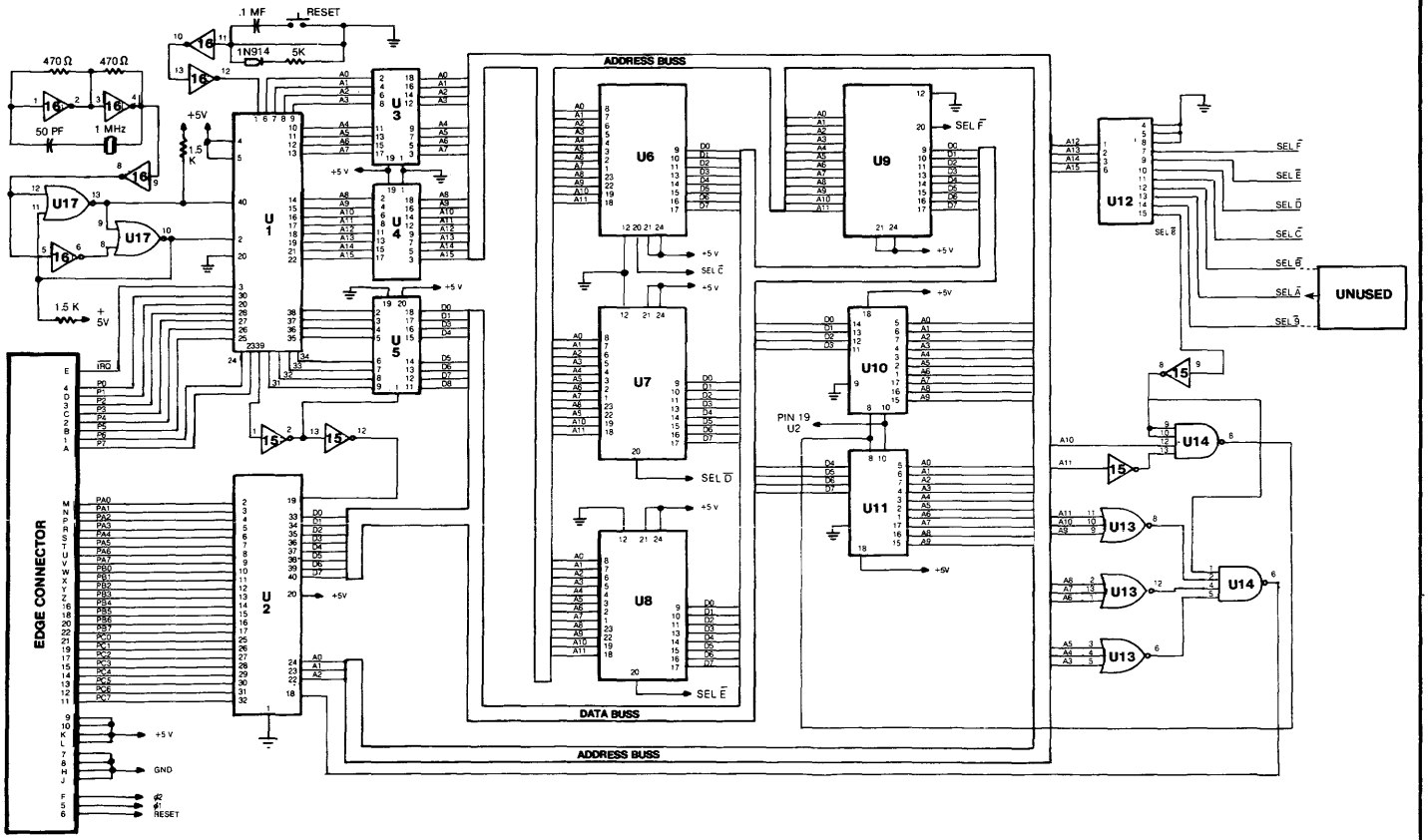
- Use +5v/2A power supply
- 1 MHz Operation
- 32 I/O lines or 24 I/O lines and 5 prioritized interrupts
- 16K ROM/EPROM Area
- 1K External RAM
- 256 bytes RAM on 6508

Edge Connector

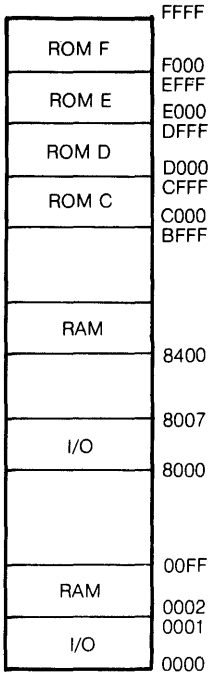
Pin	Assignment		Pin	Assignment	
1	P6	6508 Port	A	P7	6508 Port
2	P4		B	P5	
3	P2		C	P3	
4	P0		D	P1	
5	01 In		E	IRQ	
6	Reset		F	02 In	
7	GND		H	GND	
8	GND		J	GND	
9	+5v		K	+5v	
10	+5v		L	+5v	
11	PC7	6525 Port	M	PA0	6525 Port
12	PC6		N	PA1	
13	PC5		P	PA2	
14	PC4		R	PA3	
15	PC3		S	PA4	
16	PB4		T	PA5	
17	PC2		U	PA6	
18	PB5		V	PA7	
19	PC1		W	PB0	
20	PB6		X	PB1	
21	PC0		Y	PB2	
22	PB7		Z	PB3	

BOARDS

6508 (MMS/1) LOGIC DIAGRAM

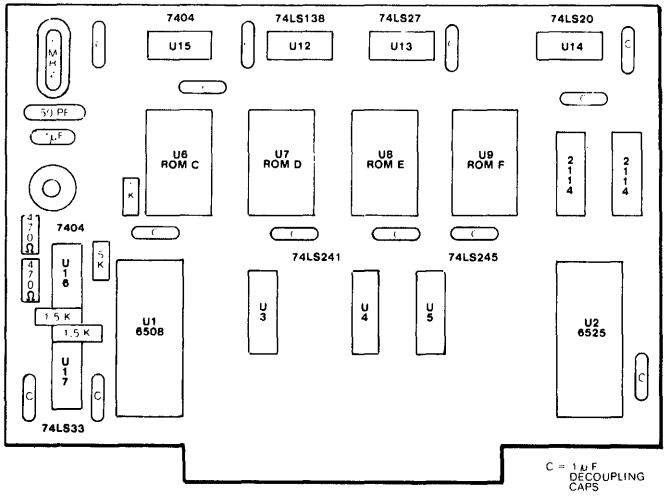


MEMORY MAP



I/O Port	Address	Assignment
PORT A	8000	PORT REGISTER A
	8003	DATA DIRECTION REGISTER A
PORT B	8001	PORT REGISTER B
	8004	DATA DIRECTION REGISTER B
PORT C	8002	PORT REGISTER C
	8005	DATA DIRECTION REGISTER C/ INTERRUPT MASK REGISTER
	8006	CONTROL REGISTER
	8007	ACTIVE INTERRUPT REGISTER
PORT M	0001	OUTPUT REGISTER
	0000	DATA DIRECTION REGISTER

BOARD LAYOUT



SECTION 3

CMOS

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CMOS

MPS

65C00

MICROPROCESSORS

65C00 MICROPROCESSORS

THE 65C00 MICROPROCESSOR FAMILY CONCEPT —

The 65C00 Series Microprocessors represent the first totally software compatible microprocessor family. This family of products includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. All of the microprocessors in the 65C00 group are software compatible within the group and are bus compatible with the M6800 product offering.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for the multi processor system applications where maximum timing control is mandatory. All versions of the microprocessors are available in 1 MHz maximum operating frequencies.

FEATURES OF THE 6500 FAMILY

- Single +5 volt supply
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type or speed memory
- 8 BIT Bi-directional Data Bus
- Addressable memory range of up to 65K bytes
- "Ready" input (for single cycle execution)
- Direct memory access capability
- Bus compatible with M6800
- Choice of external or on-board clocks
- 1 MHz operation
- On-the-chip clock options
  *External single clock input
  *RC time base input
  *Crystal time base input
- Pipeline architecture

MEMBERS OF THE 65C00 MICROPROCESSOR (CPU) FAMILY

Microprocessors with On-Chip Clock Oscillator

Model	Addressable Memory
MPS65C02	65K Bytes
MPS65C03	4K Bytes
MPS65C04	8K Bytes
MPS65C05	4K Bytes
MPS65C06	4K Bytes
MPS65C07	8K Bytes

Microprocessors with External Two Phase Clock Inputs

MPS65C12	65K Bytes
MPS65C13	4K Bytes
MPS65C14	8K Bytes
MPS65C15	4K Bytes

ORDER NUMBER:

MXS 65CXX

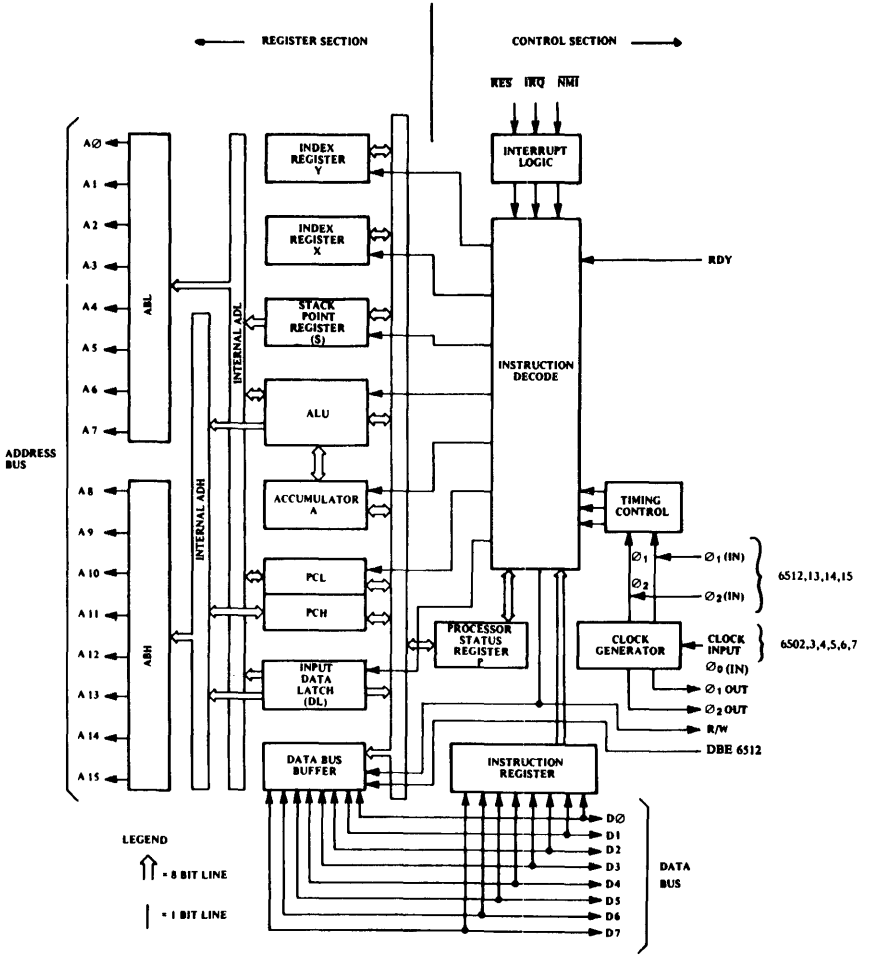
MODEL DESIGNATOR
XX = 02, 03, 04, . . . 15

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

COMMENTS ON THE DATA SHEET

The data sheet is constructed to review first the basic "Common Characteristics"—those features which are common to the general family of microprocessors. Subsequent to a review of the family characteristics will be sections devoted to each member of the group with specific features of each.

COMMON CHARACTERISTICS



Note 1. Clock Generator is not included on 65C12,13,14,15
2. Addressing Capability and control options vary with each of the 65C00 Products.

65C00 Internal Architecture

COMMON CHARACTERISTICS

MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	Vcc	−0.3 to +7.0	Vdc
INPUT VOLTAGE	Vin	−0.3 to +7.0	Vdc
OPERATING TEMPERATURE	T_A	0 to +70	°C
STORAGE TEMPERATURE	T_{STG}	−55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, Vss = 0, T_A = 0° to + 70°C)

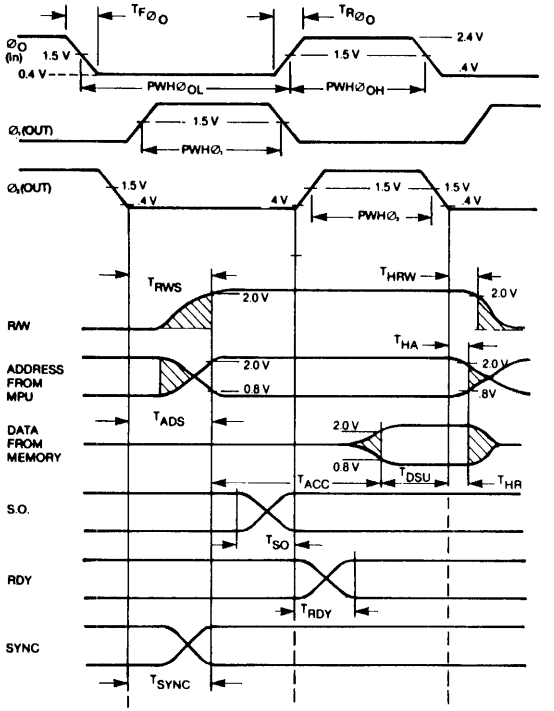
$Ø_1$, $Ø_2$ (in) applies to 65C12, 13, 14, 15; $Ø_0$ (in) applies to 65C02, 03, 04, 05, 06 and 07

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage					
Logic, $Ø_0$ (in)	VIH	Vss + 2.4	—	Vcc	Vdc
$Ø_1$, $Ø_2$ (in)		Vcc − 0.2	—	Vcc + 1.0V	Vdc
Input High Voltage					
RES, NMI, RDY, IRQ, Data, S.O.		Vss + 2.0	—	—	Vdc
Input Low Voltage					
Logic, $Ø_0$ (in)	VIL	Vss − 0.3	—	Vss + 0.4	Vdc
$Ø_1$, $Ø_2$ (in)		Vss − 0.3	—	Vss + 0.2	Vdc
RES, NMI, RDY, IRQ, Data, S.O.		—	—	Vss + 0.8	Vdc
Input Leakage Current					
(V_{In} = 0 to 5.25V, Vcc = 5.25V)					
Logic (Excl. RDY,S.O.)	Iin	—	—	2.5	μA
$Ø_1$, $Ø_2$ (in)		—	—	100	μA
$Ø_0$ (in)		—	—	10.0	μA
Three State (Off State) Input Current					
(V_{In} = 0.4 to 2.4V, Vcc = 5.25V)					
Data Lines	ITSI	—	—	10	μA
Output High Voltage					
(I_{OH} = −100μAdc, Vcc = 4.75V)					
SYNC, Data, AO-A15, R/W	VOH	Vss + 2.4	—	—	Vdc
Out Low Voltage					
(I_{OL} = 1.6mAdc, Vcc = 4.75V)					
SYNC, Data, AO-A15, R/W	VOL	—	—	Vss + 0.4	Vdc
Supply Current	I_{CC}	—		20	mA
Capacitance	C				pF
(V_{In} = O, T_A = 25°C, f = 1MHz)					
Logic	C_{in}	—	—	10	
Data		—	—	15	
AO-A15,R/W, SYNC	C_{out}	—	—	12	
$Ø_0$ (in)	$C_{Ø_0(in)}$	—	—	15	
$Ø_1$	$C_{Ø_1}$	—	30	50	
$Ø_2$	$C_{Ø_2}$	—	50	80	

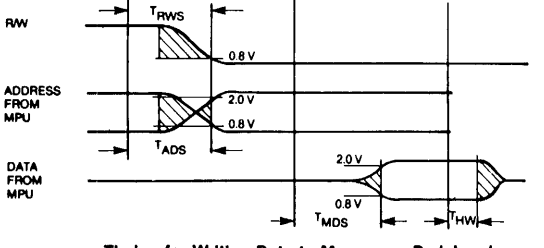
Note: IRQ and NMI require 3K pull-up resistors.

COMMON CHARACTERISTICS

Clock Timing — 65C02, 03, 04, 05, 06, 07

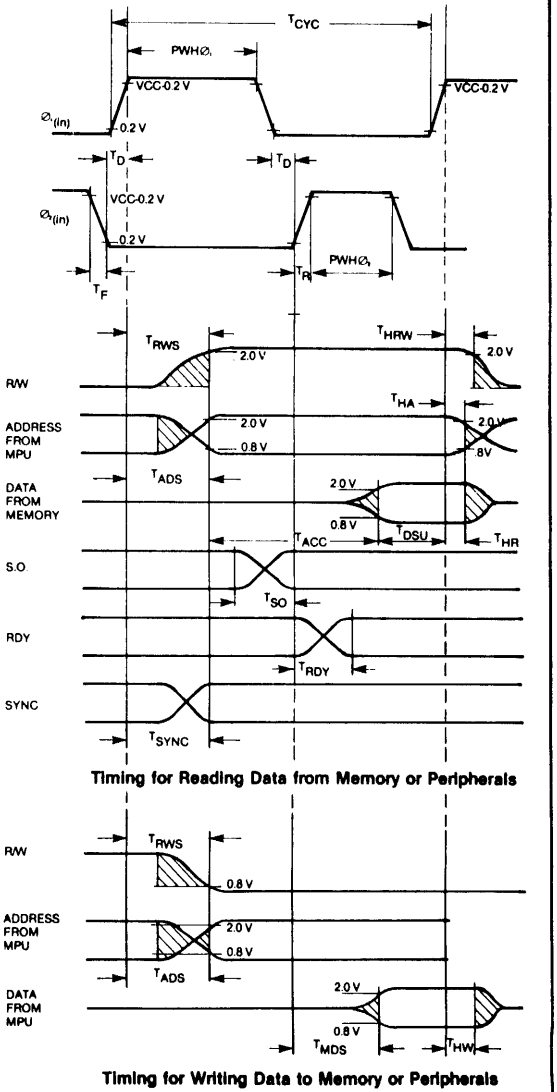


Timing for Reading Data from Memory or Peripherals



Timing for Writing Data to Memory or Peripherals

Clock Timing — 65C13, 14, 15



Timing for Reading Data from Memory or Peripherals

Timing for Writing Data to Memory or Peripherals

COMMON CHARACTERISTICS

1 MHz TIMING

Electrical Characteristics: (Vcc = 5V ± 5%, Vss = 0 V, T_A = 0°-70°C)

CLOCK TIMING — 65C02, 03, 04, 05

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.
Cycle Time	T_{CYC}	1000	—	—
$Ø_{0(IN)}$ Pulse Width (measured at 1.5v)	$PWHØ_0$	460	—	520
$Ø_{0\ (IN)}$ Rise, Fall Time	$TRØ_0$,$TFØ_0$	—	—	10
Delay Time between Clocks (measured at 1.5v)	T_D	5	—	—
$Ø_{1(OUT)}$ Pulse Width (measured at 1.5v)	$PWHØ_1$	$PWHØ_{OL}$-20	—	$PWHØ_{OL}$
$Ø_{2(OUT)}$ Pulse Width (measured at 1.5v)	$PWHØ_2$	$PWHØ_{OH}$-40	—	$PWHØ_{OH}$-10
$Ø_{1(OUT)}$, $Ø_{2(OUT)}$ Rise, Fall Time (measured .8v to 2.0v) (Load ½ 30pf ½ 1 TTL)	T_R, T_F	—	—	25

CLOCK TIMING: 65C12, 13, 14, 15

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.
Cycle Time	T_{CYC}	1000	—	—
Clock Pulse Width Ø1	PWH Ø1	430		
(Measured at V_{CC} — 0.2v) Ø2	PWH Ø2	470	—	—
Fall Time, Rise Time (Measured from 0.2v to V_{CC} — 0.2v)	T_F, T_R	—	—	25
Delay Time between Clocks (Measured at 0.2v)	T_D	0	—	—

READ/ WRITE TIMING (LOAD = ITTL)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.
Read/ Write Setup Time from 65C00	T_{RWS}	—	100	300
Address Setup Time from 65C00	T_{ADS}	—	100	300
Memory Read Access Time	T_{ACC}	—	—	575
Data Stability Time Period	T_{DSU}	100	—	—
Data Hold Time — Read	T_{HR}	10	—	—
Data Hold Time — Write	T_{HW}	30	60	—
Data Setup Time from 65C00	T_{MDS}	—	150	200
S.O. Setup Time	$T_{S.O.}$	100	—	—
SYNC Setup Time from 6500	T_{SYNC}	—	—	350
Address Hold Time	T_{HA}	30	60	—
R/W Hold Time	T_{HRW}	30	60	—
RDY Setup Time	T_{RDY}	100	—	—

COMMON CHARACTERISTICS

65C00 SIGNAL DESCRIPTION

Clocks ($\varnothing_1$, $\varnothing_2$)
The 65C1X requires a two phase non-overlapping clock that runs at the Vcc voltage level.
The 65C0X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

Address Bus (A_0-A_{15})
These outputs are TTL compatible, capable of driving one standard TTL load and 130 pf.

Data Bus (D_0-D_7)
Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130pf.

Data Bus Enable (DBE)
This TTL compatible input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two ($\varnothing_2$) clock, thus allowing data output from microprocessor only during $\varnothing_2$. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

Ready (RDY)
This input signal allows the user to single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one ($\varnothing_1$) and up to 100ns after phase two ($\varnothing_2$) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two ($\varnothing_2$) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If Ready is low during a write cycle, it is ignored until the following read operation.

Interrupt Request ($\overline{IRQ}$)
This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)
A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. $\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the interrupt mask flag status. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.
$\overline{NMI}$ also requires an external 3KΩ resister to Vcc for proper wire-OR operations.
Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupt lines that are sampled during $\varnothing_2$ (phase 2) and will begin the appropriate interrupt routine on the $\varnothing_1$ (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)
A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of $\varnothing_1$.

SYNC
This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $\varnothing_1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\varnothing_1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset
This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.
After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.
After Vcc reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (SYNC) signal will become valid.
When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

COMMON CHARACTERISTICS

ADDRESSING MODES

ACCUMULATOR ADDRESSING—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING—In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING—The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to + 127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING—In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING—In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

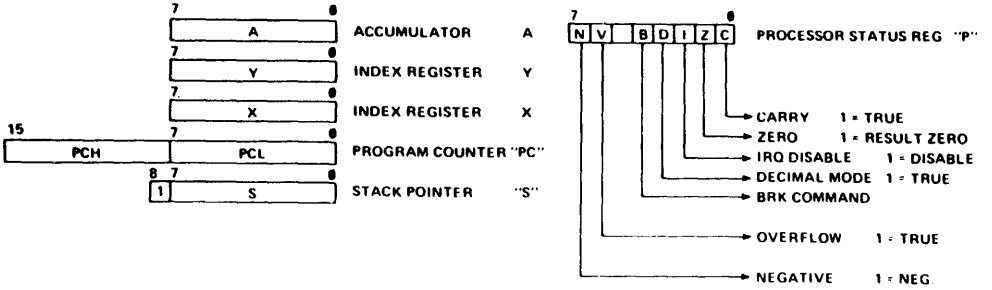
ABSOLUTE INDIRECT—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET—ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Register
TYA	Transfer Index Y to Accumulator

COMMON CHARACTERISTICS

PROGRAMMING MODEL



INSTRUCTION SET – OP CODES, Execution Time, Memory Requirements

		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM.			IMPLIED			(IND,X)			(IND),Y			ZPG,X			ABS,X			ABS,Y			RELATIVE			INDIRECT			ZPG,Y			CONDITION CODES					
	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
ADC	A + M + C → A	(4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										✓	✓	✓			✓
AND	A ∧ M → A	(1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										✓	✓				
ASL	C ← 7 0 ← 0					0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													✓	✓	✓			
BCC	BRANCH ON C=0	(2)																															90	2	2											
BCS	BRANCH ON C=1	(2)																															B0	2	2											
BEQ	BRANCH ON Z=1	(2)																															F0	2	2											
BIT	A ∧ M					2C	4	3	24	3	2																														M₇	✓				M₆
BMI	BRANCH ON N=1	(2)																															30	2	2											
BNE	BRANCH ON Z=0	(2)																															D0	2	2											
BPL	BRANCH ON N=0	(2)																															10	2	2											
BRK	(See Fig. 11)													00	7	1																											1		
BVC	BRANCH ON V=0	(2)																															50	2	2											
BVS	BRANCH ON V=1	(2)																															70	2	2											
CLC	0 → C													18	2	1																												0		
CLD	0 → D													D8	2	1																													0	
CLI	0 → I													58	2	1																												0		
CLV	0 → V													B8	2	1																														0
CMP	A - M	(1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										✓	✓	✓			
CPX	X - M		E0	2	2	EC	4	3	E4	3	2																																✓	✓	✓			
CPY	Y - M		C0	2	2	CC	4	3	C4	3	2																																✓	✓	✓			
DEC	M - 1 → M					CE	6	3	C6	5	2													D6	6	2	DE	7	3													✓	✓				
DEX	X - 1 → X													CA	2	1																											✓	✓				
DEY	Y - 1 → Y													88	2	1																											✓	✓				
EOR	A ⊻ M → A	(1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										✓	✓				
INC	M + 1 → M					EE	6	3	E6	5	2													F6	6	2	FE	7	3													✓	✓				
INX	X + 1 → X													E8	2	1																											✓	✓				
INY	Y + 1 → Y													C8	2	1																											✓	✓				
JMP	JUMP TO NEW LOC					4C	3	3																													6C	5	3							
JSR	(See Fig. 2) JUMP SUB					20	6	3																																							
LDA	M → A	(1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										✓	✓				

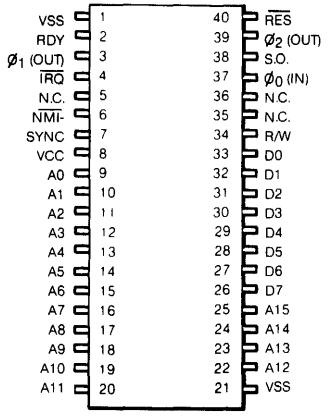
		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM.			IMPLIED			(IND,X)			(IND),Y			ZPG,X			ABS,X			ABS,Y			RELATIVE			INDIRECT			ZPG,Y			CONDITION CODES					
	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
LDX	M → X	(1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3										✓	✓				
LDY	M → Y	(1)	A0	2	2	AC	4	3	A4	3	2													84	4	2	BC	4	3													✓	✓				
LSR	0 → 7 0 → C					4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0	✓	✓			
NOP	NO OPERATION													EA	2	1																														
ORA	A ∨ M → A		09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										✓	✓				
PHA	A → Ms S-1 → S													48	3	1																														
PHP	P → Ms S-1 → S													08	3	1																														
PLA	S+1 → S Ms → A													68	4	1																											✓	✓				
PLP	S+1 → S Ms → P													28	4	1																											(RESTORED)					
ROL	7 0 C					2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													✓	✓	✓			
ROR	C 7 0					6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													✓	✓	✓			
RTI	(See Fig. 11) RTRN INT													40	6	1																													(RESTORED)			
RTS	(See Fig. 2) RTRN SUB													60	6	1																														
SBC	A-M-C̄ → A	(1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										✓	✓	(3)			✓
SEC	1 → C													38	2	1																												1		
SED	1 → D													F8	2	1																													1	
SEI	1 → I													78	2	1																													1		
STA	A → M					8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3														
STX	X → M					8E	4	3	86	3	2																																				
STY	Y → M					8C	4	3	84	3	2													94	4	2																				
TAX	A → X													AA	2	1																												✓	✓				
TAY	A → Y													A8	2	1																												✓	✓				
TSX	S → X													BA	2	1																												✓	✓				
TXA	X → A													8A	2	1																												✓	✓				
TXS	X → S													9A	2	1																																
TYA	Y → A													98	2	1																												✓	✓				

(1) ADD 1 TO 'N' IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO 'N' IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO 'N' IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER

+ ADD
- SUBTRACT
∧ AND
∨ OR
⊻ EXCLUSIVE OR
- NOT MODIFIED
✓ MODIFIED
M MEMORY BIT 7
M MEMORY BIT 6
N NO. CYCLES
NO. BYTES

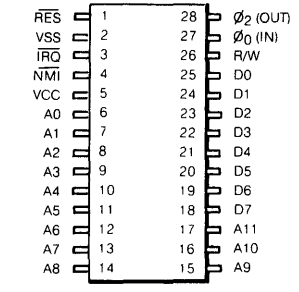
Note: MOS Technology cannot assume liability for the use of undefined OP Codes



65C02 — 40 Pin Package

Features of 65C02

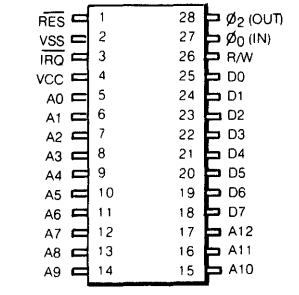
- 65K Addressable Bytes of Memory (A0-A15)
- IRQ Interrupt
- On-the-chip Clock
  - TTL Level Single Phase Input
  - RC Time Base Input
  - Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used to halt or single cycle execution)
- Two Phase Output Clock for Timing of Support Chips
- NMI Interrupt



65C03 — 28 Pin Package

Features of 65C03

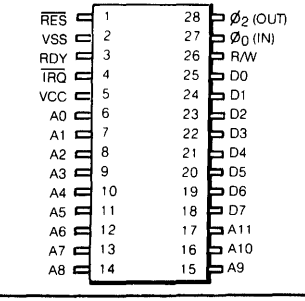
- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- IRQ Interrupt
- NMI Interrupt
- 8 Bit Bidirectional Data Bus



65C04 — 28 Pin Package

Features of 65C04

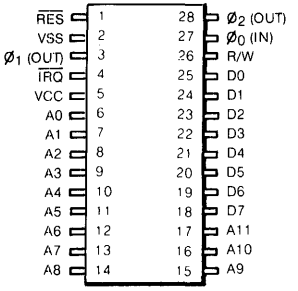
- 8K Addressable Bytes of Memory (A0-A12)
- On-the-chip Clock
- IRQ Interrupt
- 8 Bit Bidirectional Data Bus



65C05 — 28 Pin Package

Features of 65C05

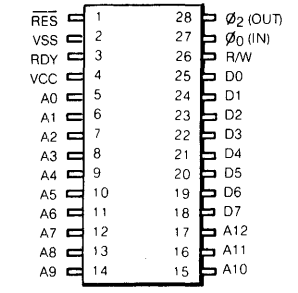
- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- IRQ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus



65C06 — 28 Pin Package

Features of 65C06

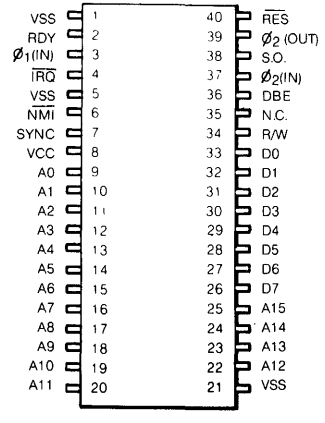
- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- Two phase output clock for timing of support chips
- 8 Bit Bidirectional Data Bus



65C07 — 28 Pin Package

Features of 65C07

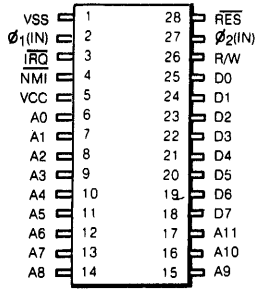
- 8K Addressable Bytes of Memory (A0-A12)
- On-the-chip Clock
- RDY Signal
- 8 Bit Bidirectional Data Bus



65C12 — 40 Pin Package

Features of 65C12

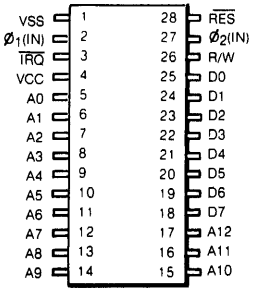
- 65K Addressable Bytes of Memory (A0-A15)
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus
- SYNC Signal
- Two phase clock input
- Data Bus Enable



65C13 — 28 Pin Package

Features of 65C13

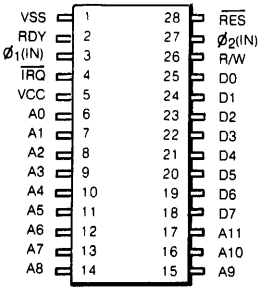
- 4K Addressable Bytes of Memory (A0-A11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- 8 Bit Bidirectional Data Bus



65C14 — 28 Pin Package

Features of 65C14

- 8K Addressable Bytes of Memory (A0-A12)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- 8 Bit Bidirectional Data Bus



65C15 — 28 Pin Package

Features of 65C15

- 4K Addressable Bytes of Memory (A0-A11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus

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65C23

TRI-PORT INTERFACE

65C23 TRI-PORT INTERFACE

CONCEPT . . .

The 65C23 TRI-PORT Interface (TPI) is designed to simplify the implementation of complex I/O operations in microcomputer systems. It has three dedicated 8-bit I/O ports which provide 24 individually programmable I/O lines.

FEATURES:

- 24 individually programmable I/O lines
- Completely static operation
- Two TTL Drive Capability
- 6 directly addressable registers
- 1 MHz operation

65C23 Addressing

65C23 REGISTERS (Direct Addressing)

*000	R0	PRA — Port Register A
001	R1	PRB — Port Register B
010	R2	PRC — Port Register C
011	R3	DDRA — Data Direction Register A
100	R4	DDRB — Data Direction Register B
101	R5	DDRC — Data Direction Register C
110	}	Illegal States
111	}	Illegal States

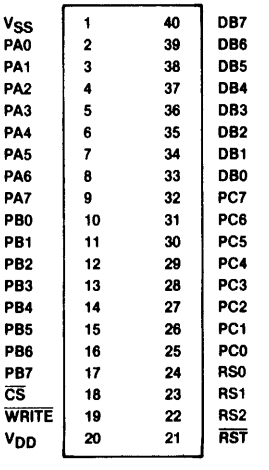
*NOTE: RS2, RS1, RS0 respectively

ORDER NUMBER:

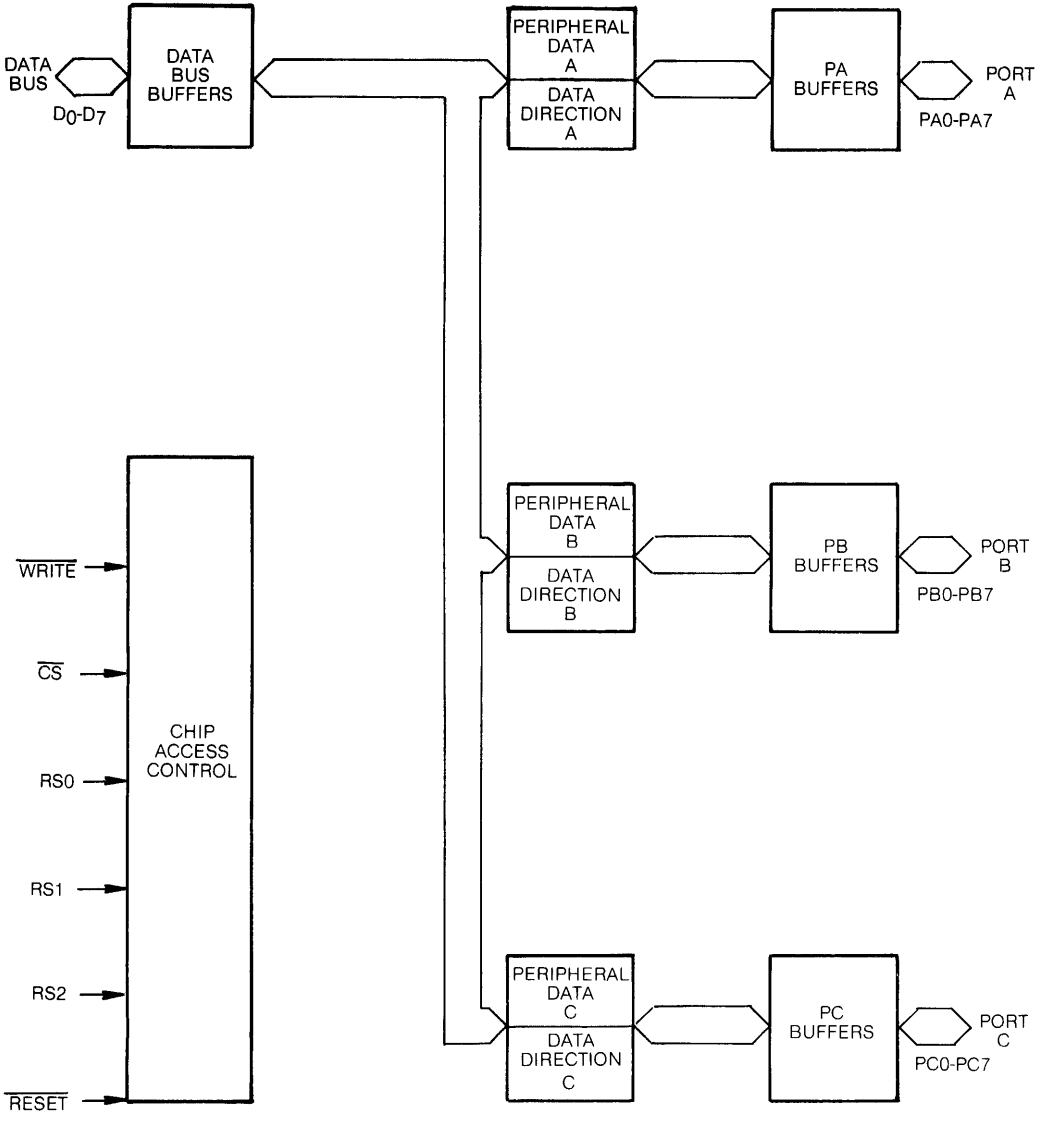
MXS 65C23

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

65C23 PIN CONFIGURATION



65C23 INTERNAL ARCHITECTURE



MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	V_{CC}	−0.3 to +7.0	V_{dc}
INPUT VOLTAGE	V_{in}	−0.3 to +7.0	V_{dc}
OPERATING TEMPERATURE RANGE	T_A	0 to +70	°C
STORAGE TEMPERATURE RANGE	T_{stg}	−55 to +150	°C

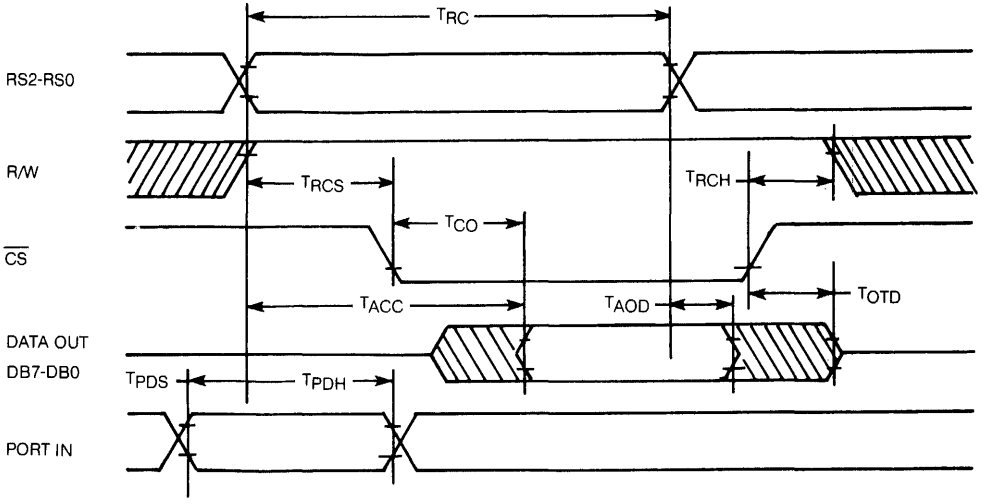
This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0V, T_A = 0° to 70°C)

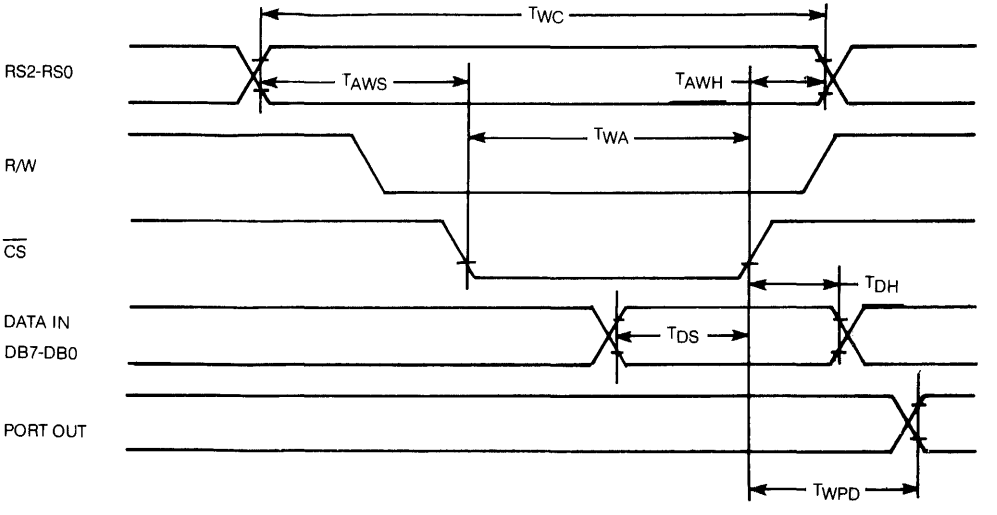
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	—	+.8	Vdc
Input Leakage Current V_{in} = 0 to 5.0 Vdc $\overline{WRITE}$ $\overline{RST}$, $\overline{CS}$, RS_0-RS_2	I_{IN}	0	±1.0	±2.5	μAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 Vdc, V_{CC} = max) D0-D7, PA0-PA7, PB0-PB7, PC0-PC7	I_{TSI}	0	±2.0	±10	μAdc
Output High Voltage (V_{CC} = min, Load = 200 μAdc)	V_{OH}	2.4	3.5	V_{CC}	Vdc
Output Low Voltage (V_{CC} = min, Load = 3.2 mAdc)	V_{OL}	V_{SS}	0.2	+0.4	Vdc
Output High Current (Sourcing) (V_{OH} = 2.4 Vdc)	I_{OH}	−200	−1000	—	μAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	I_{OL}	3.2	—	—	mAdc
Supply Current	I_{CC}	—		10	mA
Input Capacitance (V_{in} = 0V, T_A = 25°C, f = 1.0 MHz) D0-D7, PA0-PA7, PB0-PB7, PC0-PC7 $\overline{WRITE}$ $\overline{RST}$, RS_0-RS_2, $\overline{CS}$	C_{in}	—	7	10	pF
Output Capacitance (V_{in} − 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	—	7	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

READ CYCLE



WRITE CYCLE



Note: All timings referenced to V_{IL}max, V_{IH} min on inputs and V_{OL} max, V_{OH} min on outputs.

READ CYCLE

Symbol	Parameter	MIN	MAX	UNITS
T_{RC}	Read Cycle	450	—	nS
T_{ACC}	Access Time[1]	—	450	nS
T_{CO}	$\overline{CS}$ to Output Valid	—	270	nS
T_{RCS}	R/W high to $\overline{CS}$ Setup	0	—	nS
T_{RCH}	R/W high to $\overline{CS}$ Hold	0	—	nS
T_{OTD}	$\overline{CS}$ to Output Off Delay	20	120	nS
T_{AOD}	Address to Output Delay	50	—	nS
T_{PDS}	Port Input Setup	120	—	nS
T_{PDH}	Port Input Hold	150	—	nS

Note 1: Access Time measured from later of $\overline{WRITE}$ high or RS stable.

WRITE CYCLE

Symbol	Parameter	MIN	MAX	UNITS
T_{WC}	Write Cycle	450	—	nS
T_{WA}	Write Active Time[2]	420	—	nS
T_{AWS}	Address to R/W low Setup	0	—	nS
T_{AWH}	Address to R/W low Hold	0	—	nS
T_{DS}	Data bus in Setup	150	—	nS
T_{DH}	Data bus in Hold	0	—	nS
T_{WPD}	Write active to Port out Delay	—	1000	nS

Note 2: T_{WA} is the time while both $\overline{CS}$ and R/W are low.

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23C16

STATIC READ ONLY MEMORY (2048x8)

23C16 STATIC READ ONLY MEMORY (2048x8)

DESCRIPTION

The 23C16 high performance read only memory is organized 2048 words by 8 bits with access times of less than 450 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations.

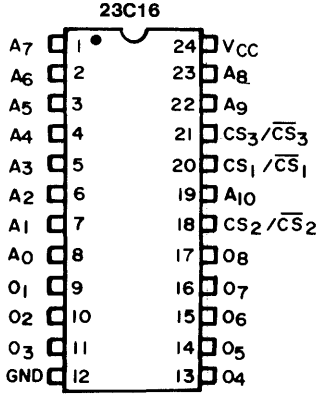
The 23C16 operates totally asynchronously. No clock input is required. The three programmable chip select inputs allow eight 16K ROMS to be OR-tied without external decoding.

Designed to replace two 2708 8K EPROMS, the 23C16 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMS after prototyping with EPROMS.

- 400mV Noise Immunity on Inputs
- 2048 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 450 ns
- Totally Static Operation
- TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- Pin Compatible with 2716 EPROM
- Replacement for two 2708s
- 2708/2716 EPROMS Accepted as Program Data Inputs

MXS-23C16

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC



ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	°C to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
Applied Output Voltage	−0.5V to +7.0V
Applied Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D. C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%, unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_{CC}	Power Supply Current		10	mA	F = 1 MHz
I_{CCS}	Stand-by Power Supply Current		10	µA	Chip Deselected
I_O	Output Leakage Current		10	µA	Chip Deselected
I_I	Input Load Current		10	µA	V_{CC} = Max. Gnd ≤ V_{IN} ≤ V_{CC}
V_{OL}	Output Low Voltage		0.4	Volts	V_{CC} = Min. I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4		Volts	V_{CC} = Min. I_{OH} = −400µA
V_{IL}	Input Low Voltage	−0.5	0.8	Volts	See Note 1
V_{IH}	Input High Voltage	2.0	V_{CC}+1	Volts	

A. C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%, unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{ACC}	Address Access Time		450	ns	
t_{CO}	Chip Select Delay		200	ns	
t_{DF}	Chip Deselect Delay		100	ns	See Note 2
t_{OH}	Previous Data Valid After Address Change Delay	40		ns	

CAPACITANCE (T_A = 25°C, f = 1.0MHz, See Note 3)

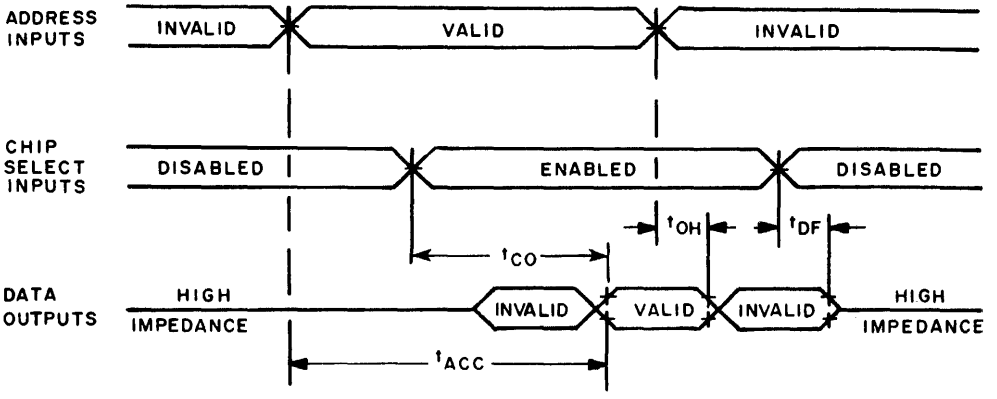
Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_{IN}	Input Capacitance		8	pF	All Pins except Pin under
C_{OUT}	Output Capacitance		10	pF	Test Tied to AC Ground

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

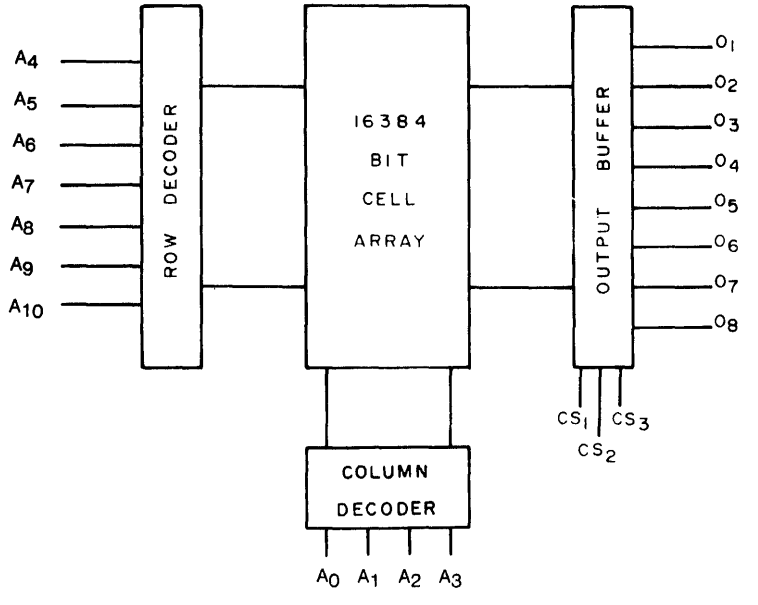
Note 2: Loading 1 TTL + 100 pF, input transition time: 20 ns
Timing measurement levels: input 1.5V, output 0.8V and 2.0V.

Note 3: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAMS

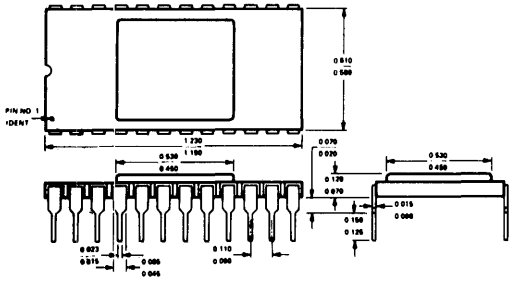


BLOCK DIAGRAM

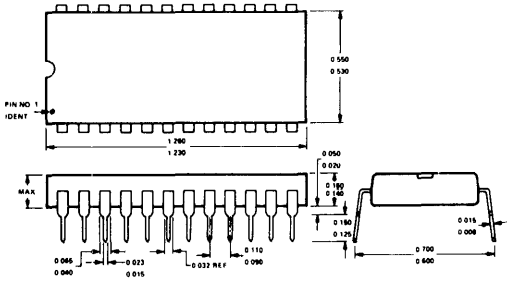


PACKAGING DIAGRAM

CERAMIC PACKAGE



MOLDED PACKAGE



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23C32

STATIC READ ONLY MEMORY
(4096x8)

23C32 STATIC READ ONLY MEMORY (4096x8)

DESCRIPTION

The 23C32 high performance read only memory is organized 4096 words by 8 bits with access times of less than 450 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations.

The 23C32 operates totally asynchronously. No clock input is required. The two programmable chip select inputs allow four 32K ROMS to be OR-tied without external decoding.

Designed to replace two 2716 16K EPROMS, the 23C32 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMS after prototyping with EPROMS.

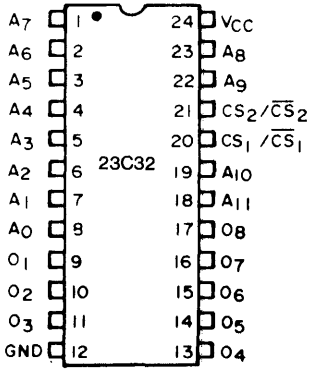
- 400mV Noise Immunity on Inputs
- 4096 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 450 ns
- Totally Static Operation
- TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Two Programmable Chip Selects
- Pin Compatible with 2716 & 2532 EPROM
- Replacement for 2716
- 2708/2716 EPROMS Accepted as Program Data Inputs

ORDERING INFORMATION:

MXS 23C32

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	°C to +70°C
Storage Temperature	−65 C to +150°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
Applied Output Voltage	−0.5V to +7.0V
Applied Input Voltage	−0.5V to +7.0V

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D. C. CHARACTERISTICS (T_A = 0 C to +70 C, V_{CC} = 5.0V ± 5%, unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_{CC}	Power Supply Current		17	mA	F = 1 MHz
I_{CCS}	Stand-by Power Supply Current		10	μA	Chip Deselected
I_O	Output Leakage Current		10	μA	Chip Deselected
I_I	Input Load Current		10	μA	V_{CC} = Max. Gnd ≤ V_{IN} ≤ V_{CC}
V_{OL}	Output Low Voltage		0.4	Volts	V_{CC} = Min. I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4		Volts	V_{CC} = Min. I_{OH} = −400μA
V_{IL}	Input Low Voltage	−0.5	0.8	Volts	See Note 1
V_{IH}	Input High Voltage	2.0	V_{CC}+1	Volts	

A. C. CHARACTERISTICS (T_A = 0 C to +70 C, V_{CC} = 5.0V ± 5%, unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{ACC}	Address Access Time		450	ns	
t_{CO}	Chip Select Delay		200	ns	
t_{DF}	Chip Deselect Delay		100	ns	See Note 2
t_{OH}	Previous Data Valid After Address Change Delay	40		ns	

CAPACITANCE (T_A = 25°C, f = 1.0MHz, See Note 3)

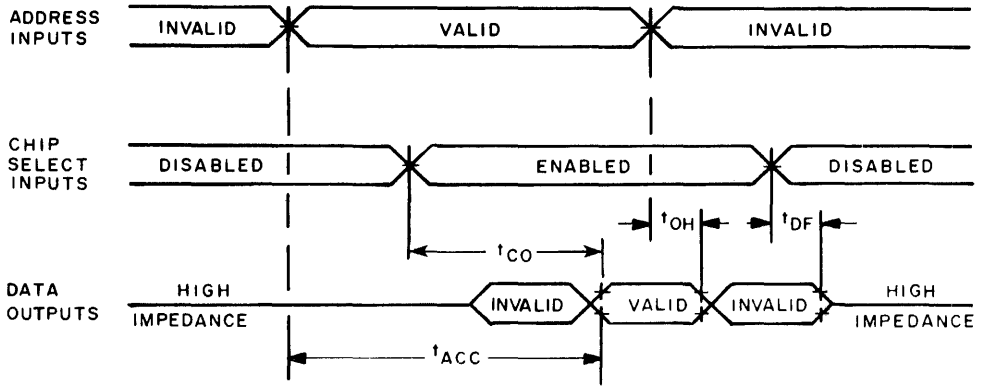
Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_{IN}	Input Capacitance		8	pF	All Pins except Pin under
C_{OUT}	Output Capacitance		10	pF	Test Tied to AC Ground

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

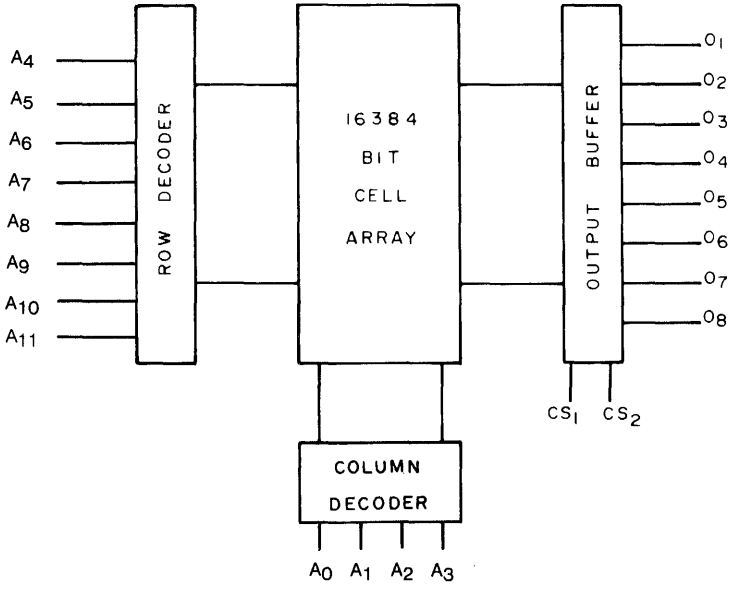
Note 2: Loading 1 TTL + 100 pF, input transition time: 20 ns
Timing measurement levels: input 1.5V, output 0.8V and 2.0V.

Note 3: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAMS

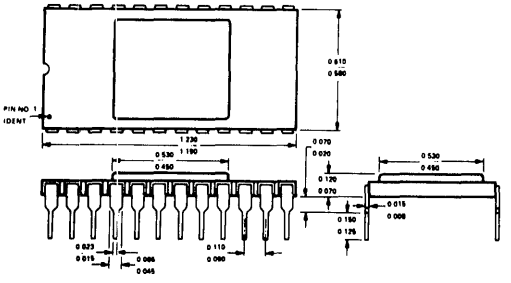


BLOCK DIAGRAM

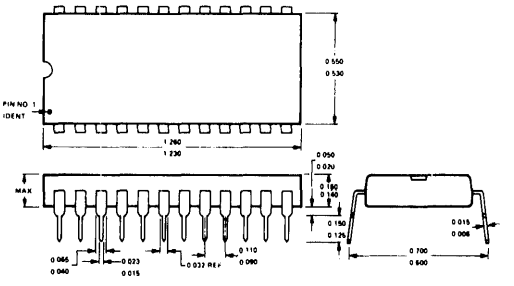


PACKAGING DIAGRAM

CERAMIC PACKAGE



MOLDED PACKAGE



SECTION 4

LCD

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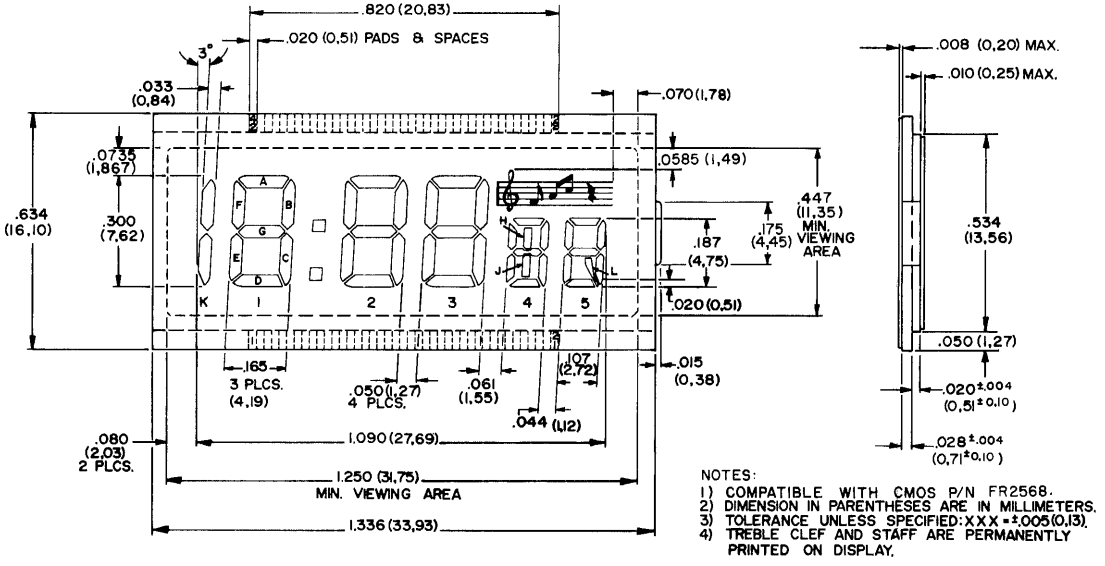
LCD

Model
4002K
5½ DIGIT DIRECT DRIVE
MELODY ALARM CLOCK
DISPLAY

MODEL 4002K 5½ DIGIT DIRECT DRIVE MELODY ALARM CLOCK DISPLAY



NOTES:
1) COMPATIBLE WITH CMOS P/N FR2568.
2) DIMENSION IN PARENTHESES ARE IN MILLIMETERS.
3) TOLERANCE UNLESS SPECIFIED: XXX = ±.005 (0,13).
4) TREBLE CLEF AND STAFF ARE PERMANENTLY PRINTED ON DISPLAY.

Pin Schedule

1	Half Digit	12	Seg E_4	23	Seg B_5	34	Seg G_3
2	Seg E_1	13	Seg J_4	24	Seg A_5	35	Seg B_2
3	Seg D_1	14	Seg D_4	25	Seg F_5	36	Seg A_2
4	Seg C_1	15	Seg C_4	26	Seg B_4	37	Seg F_2
5	Colon	16	Seg E_5	27	Seg A_4	38	Seg G_2
6	Seg E_2	17	Seg D_5	28	Seg H_4	39	Seg B_1
7	Seg D_2	18	Seg L_5	29	Seg F_4	40	Seg A_1
8	Seg C_2	19	Seg C_5	30	Seg G_4	41	Seg F_1
9	Seg E_3	20	Seg G_5	31	Seg B_3	42	Seg G_1
10	Seg D_3	21	Backplane	32	Seg A_3		
11	Seg C_3	22	Melody	33	Seg F_3		

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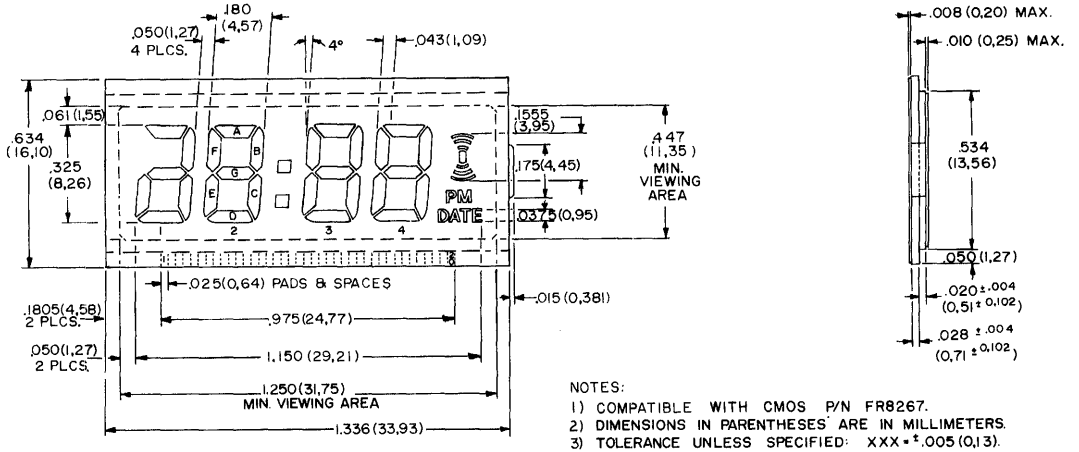
Model

4003K

4 DIGIT BIPLEXED ALARM CLOCK DISPLAY WITH ALARM, PM, AND DATA FLAG.

MODEL 4003K 4 DIGIT BIPLEXED ALARM CLOCK DISPLAY WITH ALARM, PM, AND DATE FLAGS



NOTES:
1) COMPATIBLE WITH CMOS P/N FR8267.
2) DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS.
3) TOLERANCE UNLESS SPECIFIED: XXX = ±.005 (0,13).

Pin Schedule

	BP A	BP B		BP A	BP B
1)	BP A		11)	A2	COLON
2)	BLANK	ALARM	12)	F3	E3
3)	BLANK	BLANK	13)	G3	D3
4)	BLANK	BLANK	14)	B3	C3
5)	BLANK	BLANK	15)	F4	E4
6)	A,G,E,D1	BLANK	16)	G4	D4
7)	B1	C1	17)	B4	C4
8)	F2	E2	18)	A4	DATE
9)	G2	D2	19)	A3	PM
10)	B2	C2	20)		BP B

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Model

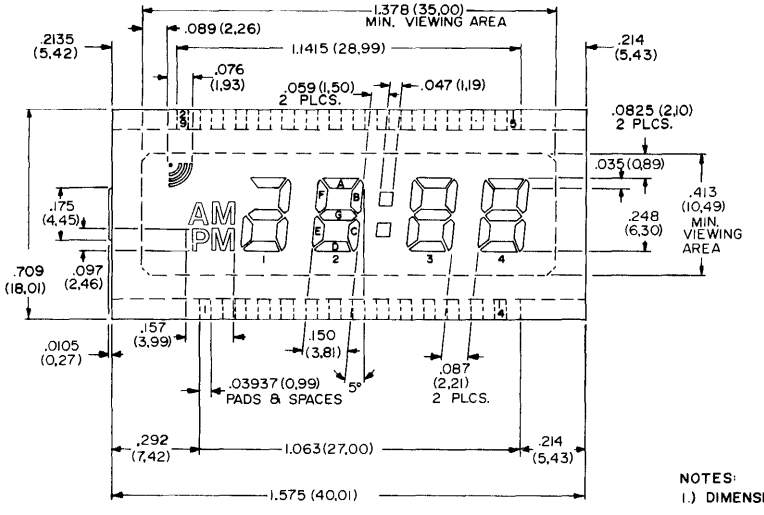
4004L

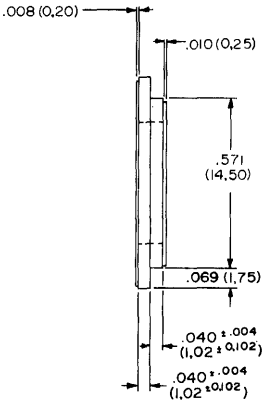
4 DIGIT DIRECT DRIVE CLOCK DISPLAY WITH ALARM, AM AND PM FLAGS

MODEL 4004L 4 DIGIT DIRECT DRIVE CLOCK DISPLAY WITH ALARM, AM AND PM FLAGS.

Outside Dimensions .709 (18,01) x 1.575 (40,01)
Digit Height .248 (6,30)

REV 00





NOTES:
1.) DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS.
2.) TOLERANCE UNLESS SPECIFIED: XXX = ±.005 (0,13)

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Model

4005N

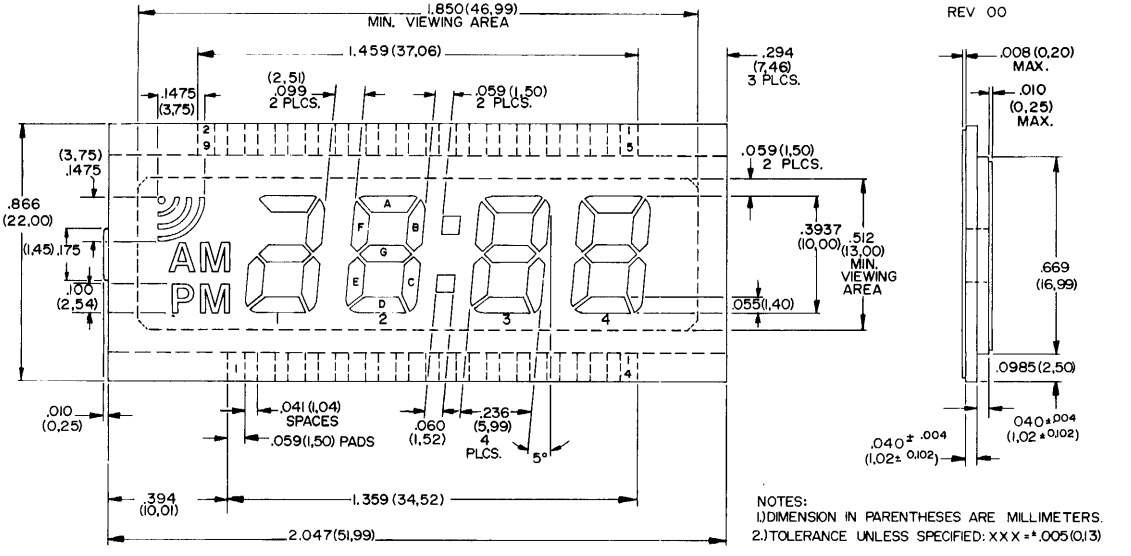
4 DIGIT DIRECT DRIVE ALARM CLOCK WITH AM AND PM FLAGS.

MODEL 4005N 4 DIGIT DIRECT DRIVE ALARM CLOCK WITH AM AND PM FLAGS.

Outside Dimensions .866 (22,00) x 2.047 (51,99)
Digit Height .3937 (10,00)

PRELIMINARY

REV 00



NOTES:
1.)DIMENSION IN PARENTHESES ARE MILLIMETERS.
2.)TOLERANCE UNLESS SPECIFIED: XXX = ±.005(0,13)

Pin Schedule

1	COMMON	9	Seg E3	16	Seg A4	23	Seg B2
2	Seg PM	10	Seg D3	17	Seg F4	24	Seg A2
3	Seg A,G,E,D1	11	Seg C3	18	Seg G4	25	Seg F2
4	Seg C1	12	Seg E4	19	Seg B3	26	Seg G2
5	Seg E2	13	Seg D4	20	Seg A3	27	Seg B1
6	Seg D2	14	Seg C4	21	Seg F3	28	AM
7	Seg C2	15	Seg B4	22	Seg G3	29	ALARM
8	COLON						

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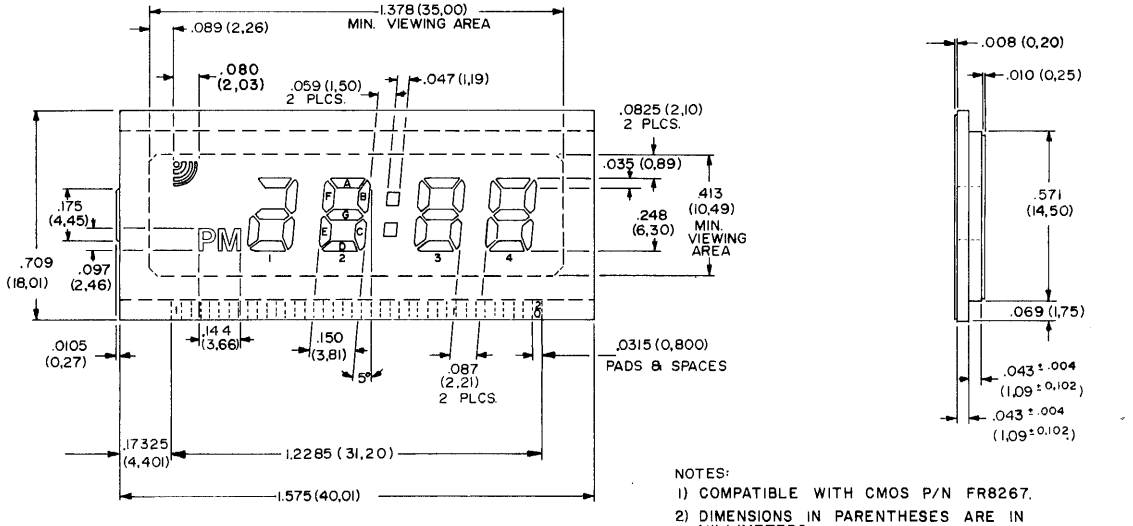
Model

4006L

4 DIGIT BIPLEXED CLOCK DISPLAY WITH ALARM AND PM FLAGS

MODEL 4006L 4 DIGIT BIPLEXED CLOCK DISPLAY WITH ALARM AND PM FLAGS



NOTES:

1) COMPATIBLE WITH CMOS P/N FR8267.
2) DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS.
3) TOLERANCE UNLESS SPECIFIED: .XXX ± .005 (0,13).

Pin Schedule

	BP A	BP B		BP A	BP B
1)	BP A		11)	A2	COLON
2)	BLANK	ALARM	12)	F3	E3
3)	BLANK	BLANK	13)	G3	D3
4)	BLANK	BLANK	14)	B3	C3
5)	BLANK	BLANK	15)	F4	E4
6)	A,G,E,D1	BLANK	16)	G4	D4
7)	B1	C1	17)	B4	C4
8)	F2	E2	18)	A4	BLANK
9)	G2	D2	19)	A3	PM
10)	B2	C2	20)		BP B

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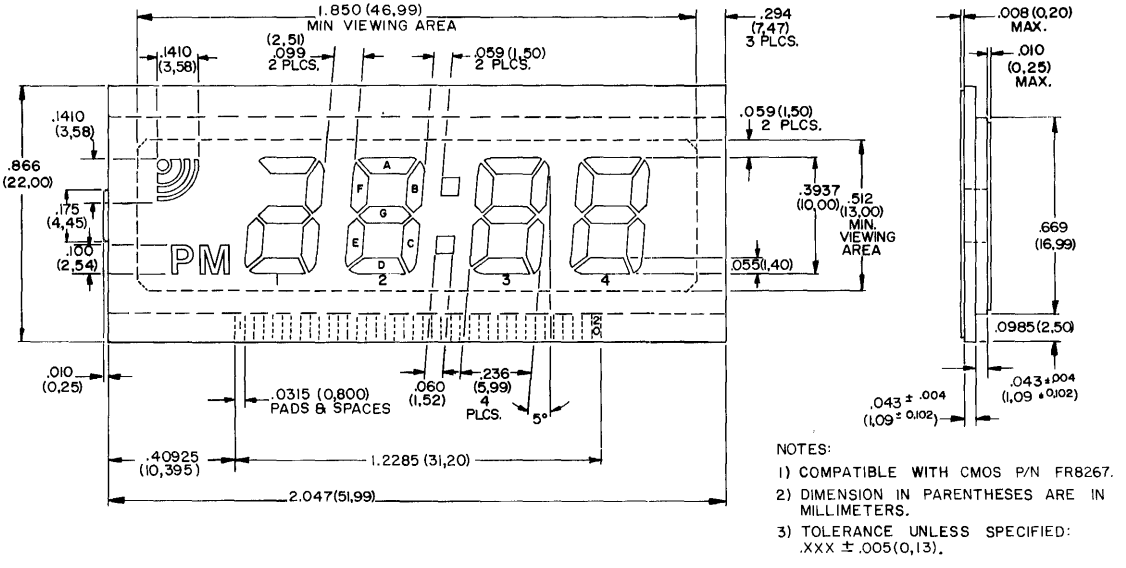
Model

4007N

4 DIGIT BIPLEXED ALARM CLOCK DISPLAY WITH PM AND ALARM FLAGS

MODEL 4007N 4 DIGIT BIPLEXED ALARM CLOCK DISPLAY WITH PM AND ALARM FLAGS



NOTES:

1) COMPATIBLE WITH CMOS P/N FR8267.
2) DIMENSION IN PARENTHESES ARE IN MILLIMETERS.
3) TOLERANCE UNLESS SPECIFIED: .XXX ± .005 (0,13).

Pin Schedule

	BP A	BP B		BP A	BP B
1)	BP A		11)	A2	COLON
2)	BLANK	ALARM	12)	F3	E3
3)	BLANK	BLANK	13)	G3	D3
4)	BLANK	BLANK	14)	B3	C3
5)	BLANK	BLANK	15)	F4	E4
6)	A,G,E,D1	BLANK	16)	G4	D4
7)	B1	C1	17)	B4	C4
8)	F2	E2	18)	A4	BLANK
9)	G2	D2	19)	A3	PM
10)	B2	C2	20)		BP B

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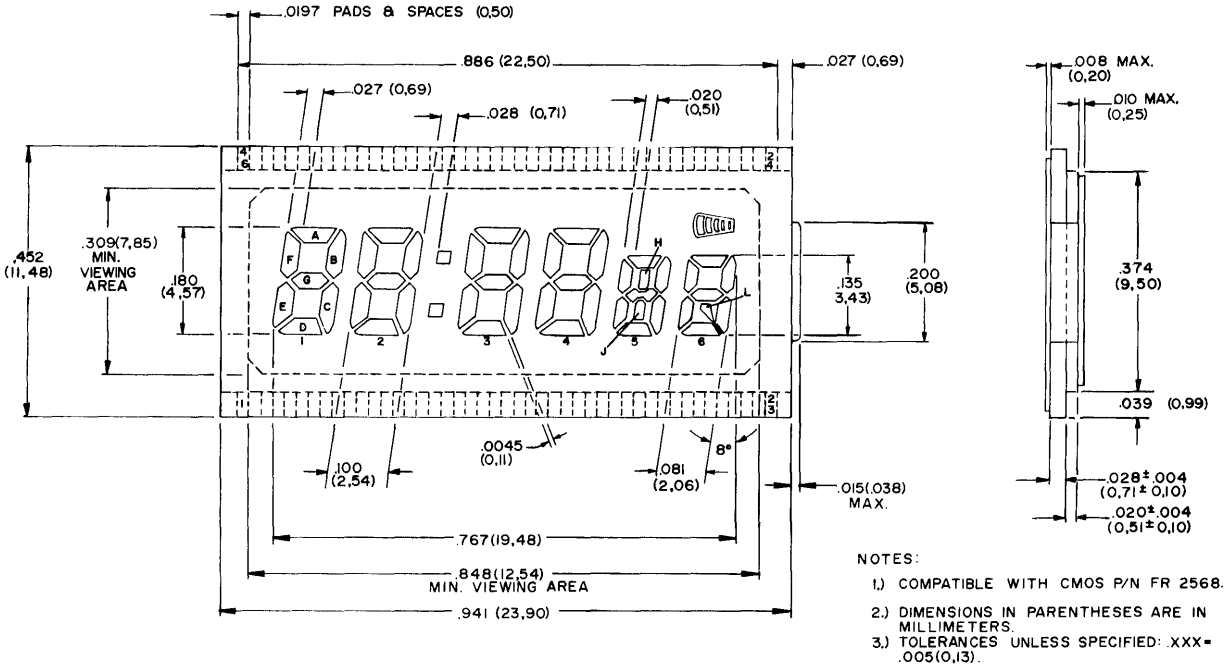
Model

5015F

MEN'S 6 DIGIT DIRECT DRIVE WATCH DISPLAY WITH ALARM FLAGS

MODEL 5015F MEN'S 6 DIGIT DIRECT DRIVE WATCH DISPLAY WITH ALARM FLAG



NOTES:

1.) COMPATIBLE WITH CMOS P/N FR 2568.

2.) DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS.

3.) TOLERANCES UNLESS SPECIFIED: .XXX= .005(0,13).

Pin Schedule

1	Seg E_1	13	Seg C_4	25	Seg B_6	37	Seg B_3
2	Seg D_1, A_1	14	Seg E_5	26	Seg A_6	38	Seg F_3
3	Seg C_1	15	Seg J_5	27	Seg F_6	39	Seg G_3
4	Seg E_2	16	Seg D_5	28	Seg B_5	40	Seg B_2
5	Seg D_2	17	Seg C_5	29	Seg A_5	41	Seg A_2
6	Seg C_2	18	Seg E_6	30	Seg H_5	42	Seg F_2
7	Colon	19	Seg D_6	31	Seg F_5	43	Seg G_2
8	Seg E_3	20	Seg L_6	32	Seg G_5	44	Seg B_1
9	Seg A_3, D_3	21	Seg C_6	33	Seg B_4	45	Seg F_1
10	Seg C_3	22	Seg G_6	34	Seg A_4	46	Seg G_1
11	Seg E_4	23	Backplane	35	Seg F_4		
12	Seg D_4	24	Alarm	36	Seg G_4		

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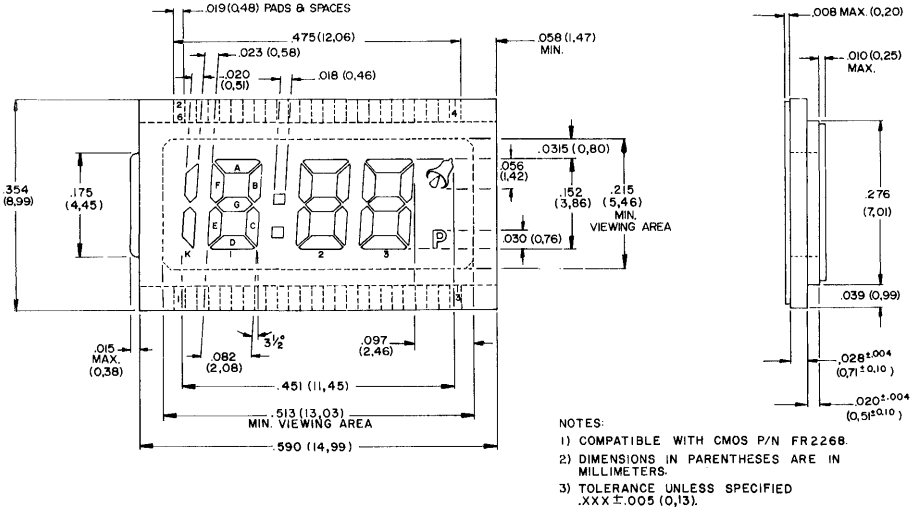
Model

5017B

LADIES' 3½ DIGIT DIRECT DRIVE WATCH DISPLAY WITH ALARM AND PM FLAGS.

MODEL 5017B LADIES' 3½ DIGIT DIRECT DRIVE WATCH DISPLAY WITH ALARM AND PM FLAGS



NOTES:

1) COMPATIBLE WITH CMOS P/N FR2268.
2) DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS.
3) TOLERANCE UNLESS SPECIFIED .XXX ±.005 (0,13).

Pin Schedule

1	Backplane	8	Seg D_2	15	Seg B_3	22	Seg G_2
2	Half Digit	9	Seg C_2	16	Seg A_3	23	Seg B_1
3	Seg E_1	10	Seg E_3	17	Seg F_3	24	Seg A_1
4	Seg D_1	11	Seg D_3	18	Seg G_3	25	Seg F_1
5	Seg C_1	12	Seg C_3	19	Seg B_2	26	Seg G_1
6	Colon	13	PM	20	Seg A_2		
7	Seg E_2	14	Alarm	21	Seg F_2		

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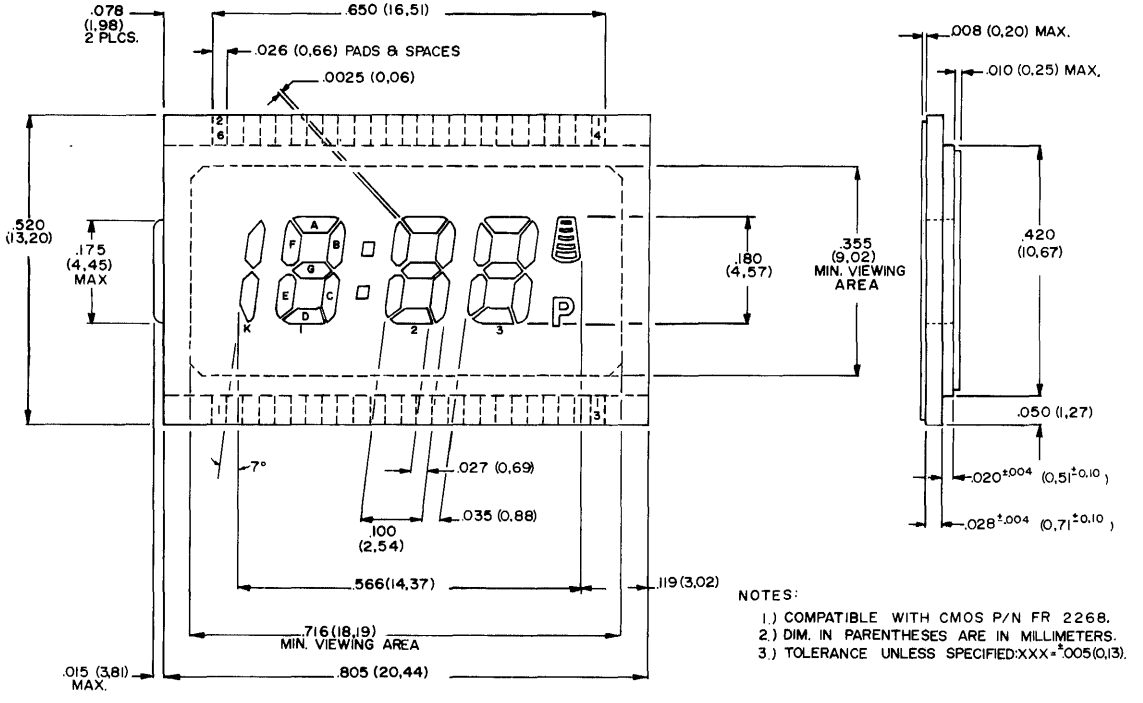
LCD

Model

5018E

MEN'S 3½ DIGIT DIRECT DRIVE WATCH DISPLAY WITH ALARM AND PM FLAGS

MODEL 5018E MEN'S 3½ DIGIT DIRECT DRIVE WATCH DISPLAY WITH ALARM AND PM FLAGS



Pin Schedule

1	Backplane	8	Seg D_2	15	Seg B_3	22	Seg G_2
2	Half Digit	9	Seg C_2	16	Seg A_3	23	Seg B_1
3	Seg E_1	10	Seg E_3	17	Seg F_3	24	Seg A_1
4	Seg D_1	11	Seg D_3	18	Seg G_3	25	Seg F_1
5	Seg C_1	12	Seg C_3	19	Seg B_2	26	Seg G_1
6	Colon	13	PM	20	Seg A_2		
7	Seg E_2	14	Alarm	21	Seg F_2		

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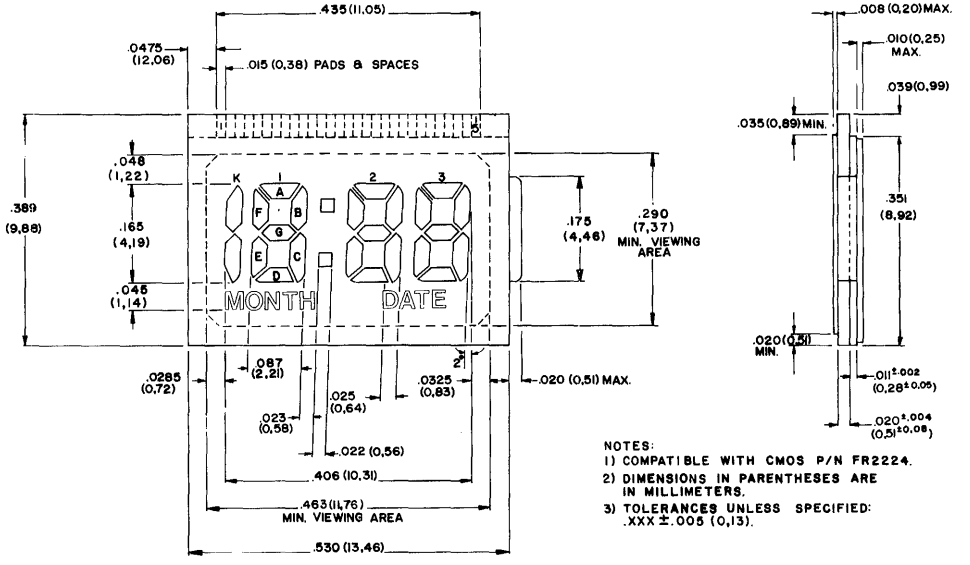
Model

5053BB

LADIES' 3½ DIGIT BIPLEXED WATCH DISPLAY

MODEL 5053BB LADIES' 3½ DIGIT BIPLEXED WATCH DISPLAY



NOTES:
1) COMPATIBLE WITH CMOS P/N FR2224.
2) DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS.
3) TOLERANCES UNLESS SPECIFIED: .XXX ±.005 (0,13).

Pin Schedule

	A	B		A	B
1	Backplane		9.	Seg A_2	Seg B_2
2	Half Digit	Seg E_1	10.	–OFF–	Seg E_3
3	Seg F_1	Seg D_1	11.	Seg F_3	Seg D_3
4	Seg G_1	Seg C_1	12.	Seg G_3	Seg C_3
5	Seg A_1	Seg B_1	13.	Seg A_3	Seg B_3
6	Colon	Seg E_2	14.	Month-Date	–OFF–
7	Seg F_2	Seg D_2	15.		Backplane
8	Seg G_2	Seg C_2			

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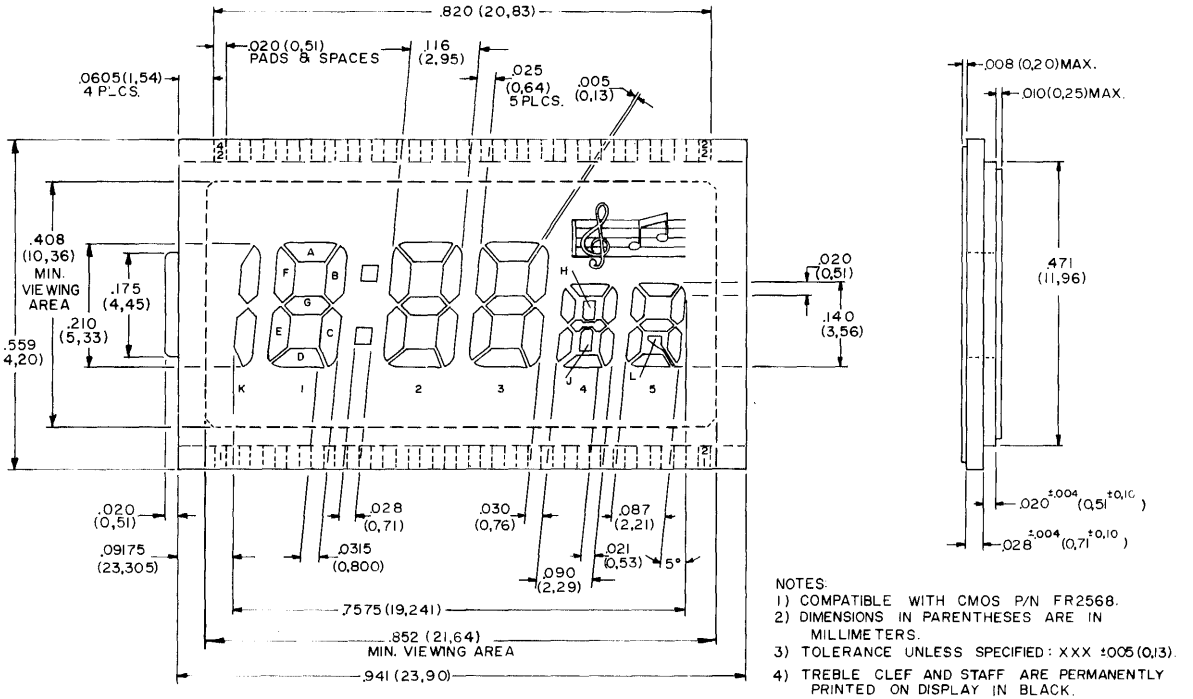
Model

5056 I

MEN'S 5½ DIGIT DIRECT DRIVE WATCH DISPLAY UNIT MELODY ALARM FLAG.

MODEL 5056 I MEN'S 5½ DIGIT DIRECT DRIVE WATCH DISPLAY WITH MELODY ALARM FLAG



NOTES:
1) COMPATIBLE WITH CMOS P/N FR2568.
2) DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS.
3) TOLERANCE UNLESS SPECIFIED: XXX ±005 (0,13).
4) TREBLE CLEF AND STAFF ARE PERMANENTLY PRINTED ON DISPLAY IN BLACK.

Pin Schedule

1	Half Digit	12	Seg E_4	23	Seg B_5	34	Seg G_3
2	Seg E_1	13	Seg J_4	24	Seg A_5	35	Seg B_2
3	Seg D_1	14	Seg D_4	25	Seg F_5	36	Seg A_2
4	Seg C_1	15	Seg C_4	26	Seg B_4	37	Seg F_2
5	Colon	16	Seg E_5	27	Seg A_4	38	Seg G_2
6	Seg E_2	17	Seg D_5	28	Seg H_4	39	Seg B_1
7	Seg D_2	18	Seg L_5	29	Seg F_4	40	Seg A_1
8	Seg C_2	19	Seg C_5	30	Seg G_4	41	Seg F_1
9	Seg E_3	20	Seg G_5	31	Seg B_3	42	Seg G_1
10	Seg D_3	21	Backplane	32	Seg A_3		
11	Seg C_3	22	Melody	33	Seg F_3		

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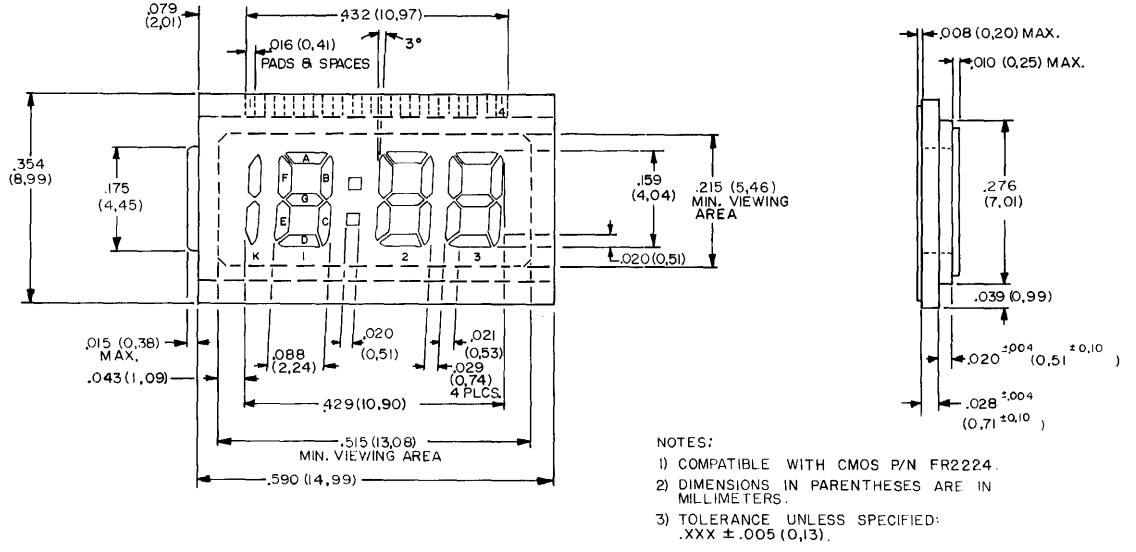
Model

5060B

LADIES' 3½ DIGIT BIPLEXED WATCH DISPLAY

MODEL 5060B LADIES' 3½ DIGIT BIPLEXED WATCH DISPLAY



NOTES:

1) COMPATIBLE WITH CMOS P/N FR2224.
2) DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS.
3) TOLERANCE UNLESS SPECIFIED: .XXX ± .005 (0,13).

Pin Schedule

	A	B		A	B
1	Backplane		8	Seg G_2	Seg C_2
2	Half Digit	Seg E_1	9	Seg A_2	Seg B_2
3	Seg F_1	Seg D_1	10	–OFF–	Seg E_3
4	Seg G_1	Seg C_1	11	Seg F_3	Seg D_3
5	Seg A_1	Seg B_1	12	Seg G_3	Seg C_3
6	Colon	Seg E_2	13	Seg A_3	Seg B_3
7	Seg F_2	Seg D_2	14		Backplane

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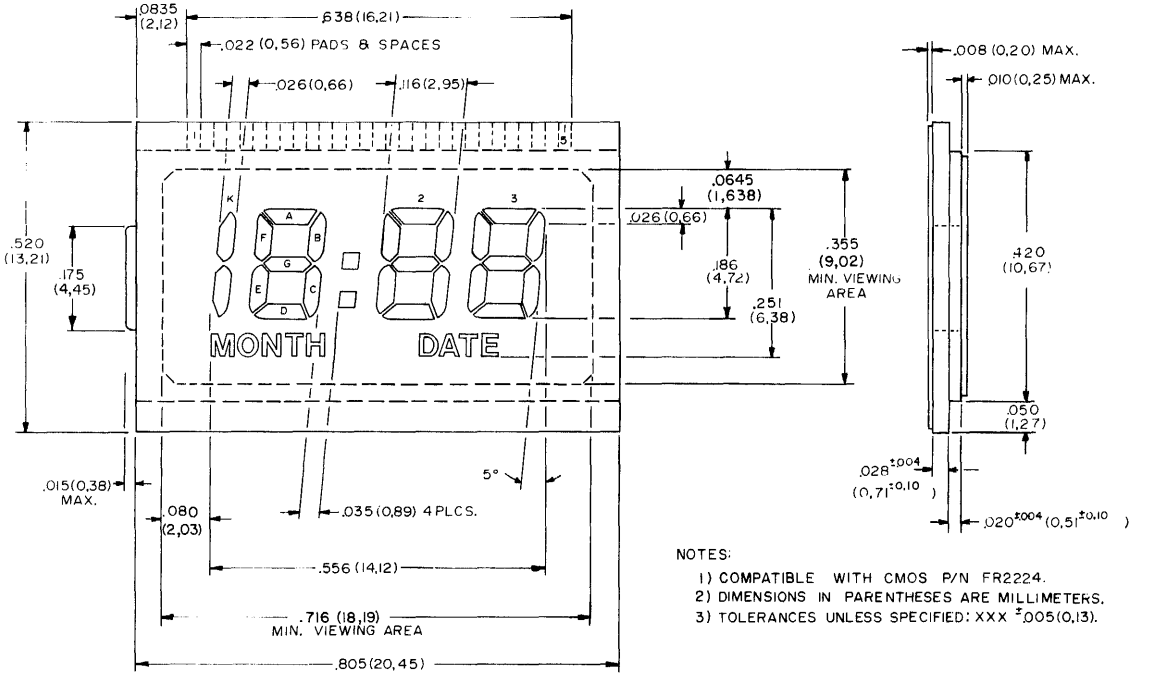
Model

5061E

MEN'S 3½ DIGIT BIPLEXED WATCH DISPLAY.

MODEL 5061E MEN'S 3½ DIGIT BIPLEXED WATCH DISPLAY



NOTES:

1) COMPATIBLE WITH CMOS P/N FR2224.
2) DIMENSIONS IN PARENTHESES ARE MILLIMETERS.
3) TOLERANCES UNLESS SPECIFIED: XXX ±.005 (0,13).

Pin Schedule

	A	B		A	B
1	Backplane		9.	Seg A_2	Seg B_2
2	Half Digit	Seg E_1	10.	–OFF–	Seg E_3
3	Seg F_1	Seg D_1	11.	Seg F_3	Seg D_3
4	Seg G_1	Seg C_1	12.	Seg G_3	Seg C_3
5	Seg A_1	Seg B_1	13.	Seg A_3	Seg B_3
6	Colon	Seg E_2	14.	Month-Date	–OFF–
7	Seg F_2	Seg D_2	15.		Backplane
8	Seg G_2	Seg C_2			

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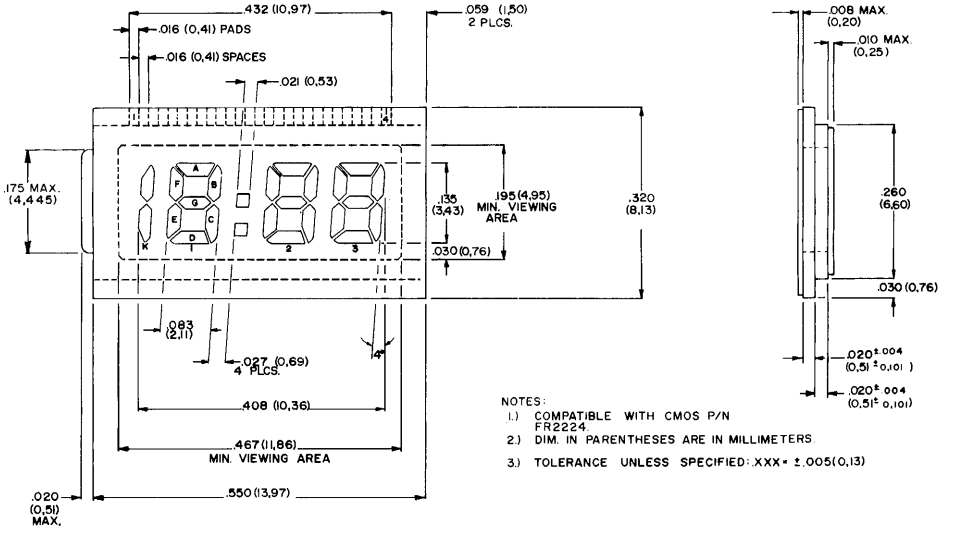
Model

5075A

3½ DIGIT BIPLEXED PEN DISPLAY

MODEL 5075A 3½ DIGIT BIPLEXED PEN DISPLAY



Pin Schedule

	A	B		A	B
1	Backplane		8	Seg G_2	Seg C_2
2	Half Digit	Seg E_1	9	Seg A_2	Seg B_2
3	Seg F_1	Seg D_1	10	–OFF–	Seg E_3
4	Seg G_1	Seg C_1	11	Seg F_3	Seg D_3
5	Seg A_1	Seg B_1	12	Seg G_3	Seg C_3
6	Colon	Seg E_2	13	Seg A_3	Seg B_3
7	Seg F_2	Seg D_2	14		Backplane

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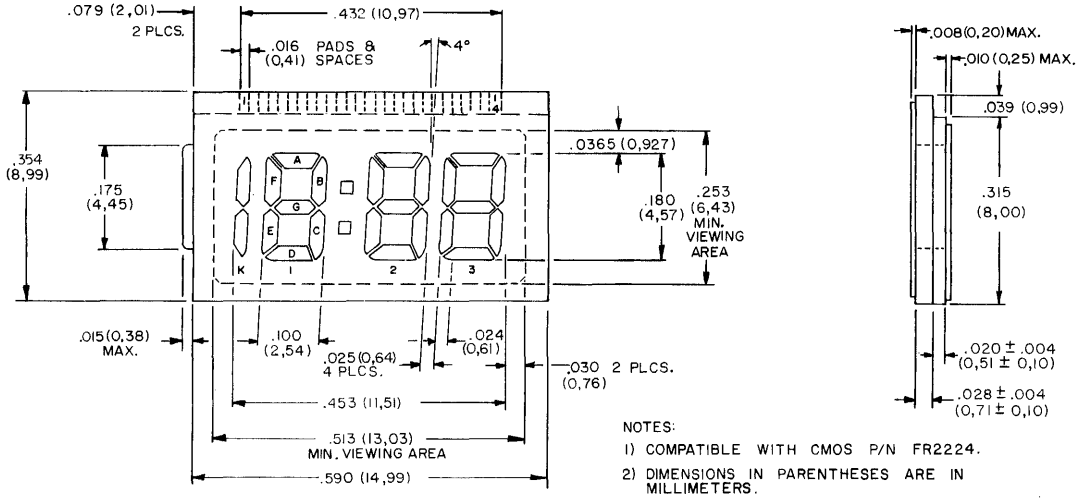
MODEL

5101C

LADIES' 3½ LARGE DIGIT BIPLEXED WATCH DISPLAY

MODEL 5101C LADIES' 3½ LARGE DIGIT BIPLEXED WATCH DISPLAY



NOTES:

1) COMPATIBLE WITH CMOS P/N FR2224.
2) DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS.
3) TOLERANCE UNLESS SPECIFIED: .XXX ± .005 (0,13).

Pin Schedule

	A	B		A	B
1	Backplane		8	Seg G_2	Seg C_2
2	Half Digit	Seg E_1	9	Seg A_2	Seg B_2
3	Seg F_1	Seg D_1	10	–OFF–	Seg E_3
4	Seg G_1	Seg C_1	11	Seg F_3	Seg D_3
5	Seg A_1	Seg B_1	12	Seg G_3	Seg C_3
6	Colon	Seg E_2	13	Seg A_3	Seg B_3
7	Seg F_2	Seg D_2	14		Backplane

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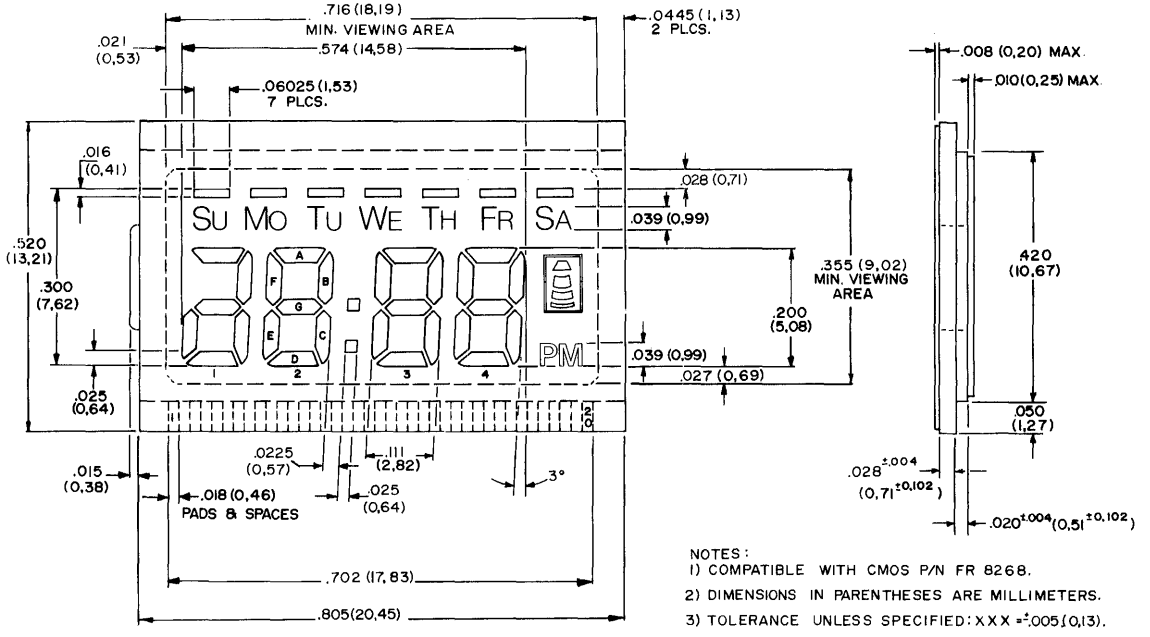
LCD

Model

5102E

MEN'S BIPLEXED WATCH DISPLAY WITH PM, ALARM, AND DAY FLAGS.

MODEL 5102E MEN'S BIPLEXED WATCH DISPLAY WITH PM, ALARM, AND DAY FLAGS.



NOTES:
1) COMPATIBLE WITH CMOS P/N FR 8268.
2) DIMENSIONS IN PARENTHESES ARE MILLIMETERS.
3) TOLERANCE UNLESS SPECIFIED: XXX = ±.005 (0,13).
4) SU PERMANENTLY PRINTED ON DISPLAY IN RED.
5) DAYS OF WEEK AND ALARM FRAME PERMANENTLY PRINTED ON DISPLAY IN BLACK.

Pin Schedule

	BP A	BP B		BP A	BP B
1)	BP A		11)	A2	COLON
2)	SU	ALARM	12)	F3	E3
3)	MO	SA	13)	G3	D3
4)	TU	FR	14)	B3	C3
5)	WE	TH	15)	F4	E4
6)	A,G,E,D1	BLANK	16)	G4	D4
7)	B1	C1	17)	B4	C4
8)	F2	E2	18)	A4	BLANK
9)	G2	D2	19)	A3	PM
10)	B2	C2	20)		BP B

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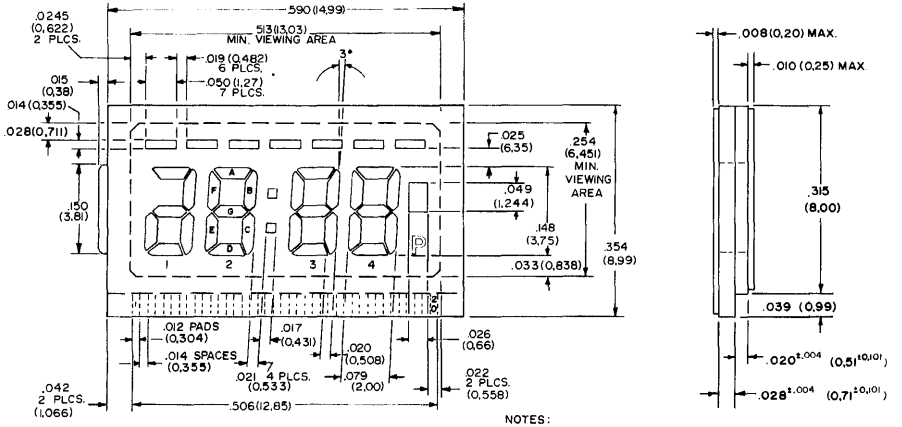
LCD

Model

5103C

LADIES 4 DIGIT BIPLEXED WATCH DISPLAY WITH ALARM, PM, AND DAY FLAGS.

MODEL 5103C LADIES' 4 DIGIT BIPLEXED WATCH DISPLAY WITH ALARM, PM, AND DAY FLAGS



NOTES:

1.) COMPATIBLE WITH CMOS P/N FR 8222,8223, OR 8268.

2.) DIMENSIONS IN PARENTHESES ARE MILLIMETERS.

3.) TOLERANCE UNLESS SPECIFIED: XXX = ±.005 (0,13)

Pin Schedule

BP A		BP B		BP A		BP B
1)	BP A		11)	A2		COLON
2)	SU	ALARM	12)	F3		E3
3)	MO	SA	13)	G3		D3
4)	TU	FR	14)	B3		C3
5)	WE	TH	15)	F4		E4
6)	A,G,E,D1	BLANK	16)	G4		D4
7)	B1	C1	17)	B4		C4
8)	F2	E2	18)	A4		BLANK
9)	G2	D2	19)	A3		PM
10)	B2	C2	20)			BP B

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LCD

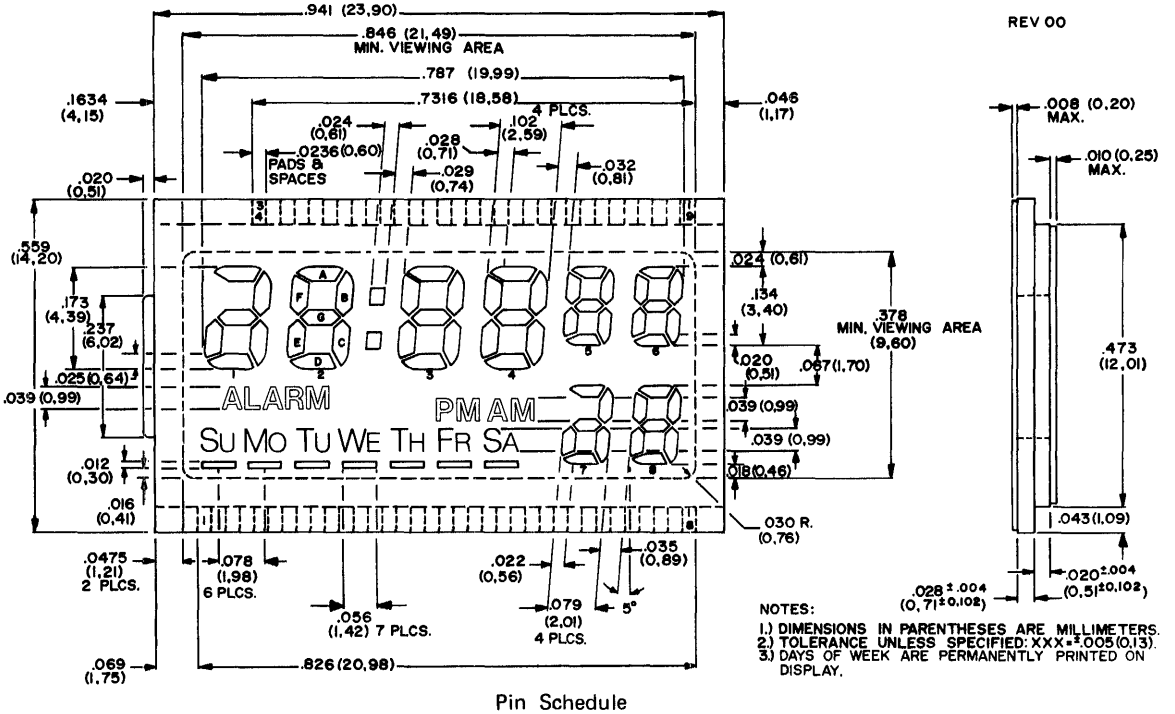
Model

5104 I

MEN'S 8 DIGIT BIPLEXED WATCH DISPLAY WITH AM, PM, ALARM, AND DAY FLAGS.

MODEL 5104 I MEN'S 8 DIGIT BIPLEXED WATCH DISPLAY WITH PM, AM, ALARM, AND DAY FLAGS.

Outside Dimensions .599 (14,20) x .941 (23,90)
Digit Height .173 (4,39)
.134 (3,40)



NOTES:
1.) DIMENSIONS IN PARENTHESES ARE MILLIMETERS.
2.) TOLERANCE UNLESS SPECIFIED: XXX = ±.005 (0,13).
3.) DAYS OF WEEK ARE PERMANENTLY PRINTED ON DISPLAY.

Pin Schedule

	A	B		A	B
1	Seg A,G,E,D_1	Seg B_1	18	BACKPLANE	
2	ALARM	Seg C_1	19		BACKPLANE
3	SU	Seg D_2	20	Seg C_6	Seg E_6
4	MO	COLON	21	Seg B_6	Seg G_6
5	TU	Seg D_3	22	Seg A_6	Seg F_6
6	WE	Seg D_4	23	Seg C_5	Seg E_5
7	BLANK	BLANK	24	Seg B_5	Seg G_5
8	TH	Seg D_5	25	Seg A_5	Seg F_5
9	FR	Seg D_6	26	Seg C_4	Seg E_4
10	SA	Seg A_8	27	Seg B_4	Seg G_4
11	BLANK	BLANK	28	Seg A_4	Seg F_4
12	PM	AM	29	Seg C_3	Seg E_3
13	Seg E_7	Seg A,G,D_7	30	Seg B_3	Seg G_3
14	Seg C_7	Seg B_7	31	Seg A_3	Seg F_3
15	Seg D_8	Seg E_8	32	Seg C_2	Seg E_2
16	Seg C_8	Seg G_8	33	Seg B_2	Seg G_2
17	Seg B_8	Seg F_8	34	Seg A_2	Seg F_2

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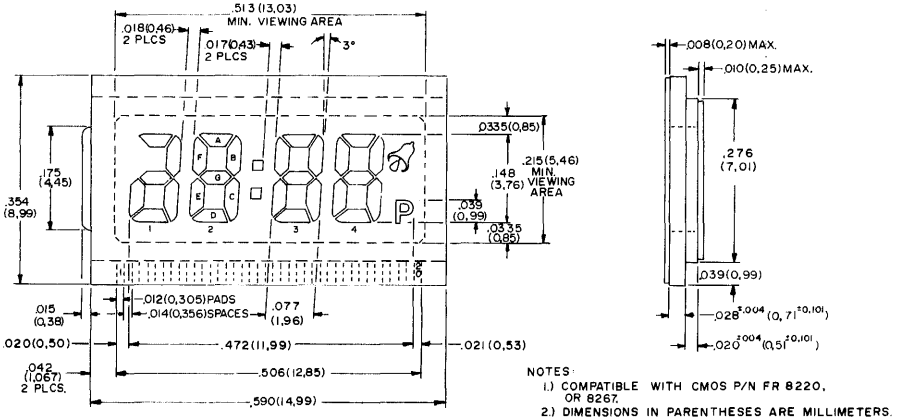
LCD

Model

5107B

LADIES' 4 DIGIT BIPLEXED WATCH DISPLAY WITH ALARM AND PM FLAGS

MODEL 5107B LADIES' 4 DIGIT BIPLEXED WATCH DISPLAY WITH ALARM AND PM FLAGS



NOTES:
1.) COMPATIBLE WITH CMOS P/N FR 8220, OR 8267.
2.) DIMENSIONS IN PARENTHESES ARE MILLIMETERS.
3.) TOLERANCE UNLESS SPECIFIED: .XXX ± .005(0,13)

Pin Schedule

	BP A	BP B		BP A	BP B
1)	BP A		11)	A2	COLON
2)	BLANK	ALARM	12)	F3	E3
3)	BLANK	BLANK	13)	G3	D3
4)	BLANK	BLANK	14)	B3	C3
5)	BLANK	BLANK	15)	F4	E4
6)	A,G,E,D1	BLANK	16)	G4	D4
7)	B1	C1	17)	B4	C4
8)	F2	E2	18)	A4	BLANK
9)	G2	D2	19)	A3	PM
10)	B2	C2	20)		BP B

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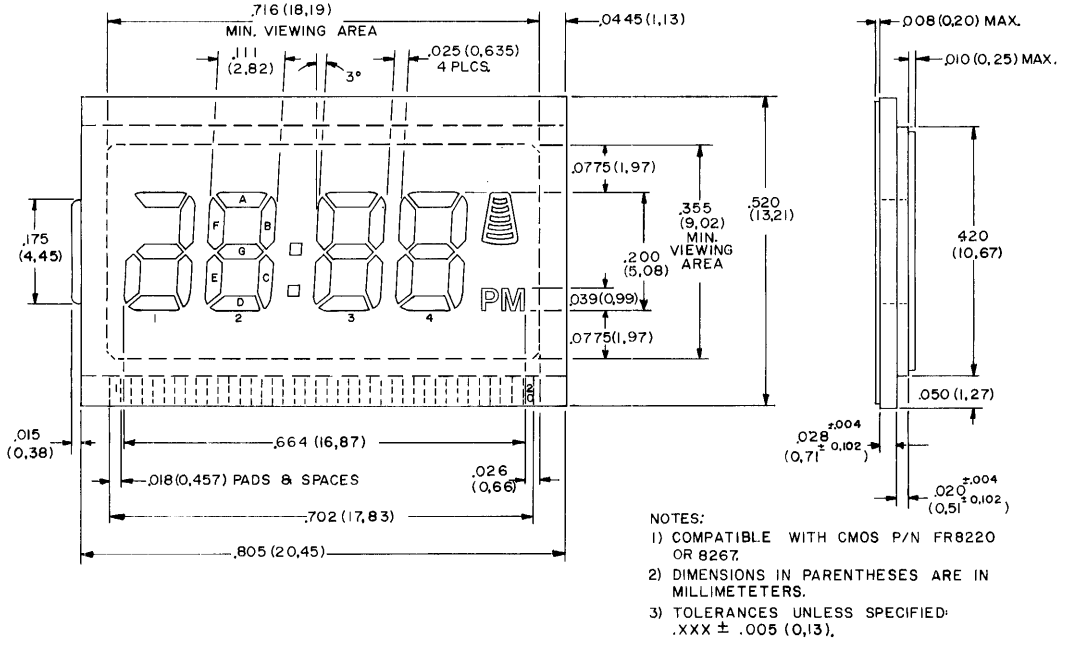
Model

5108E

MEN'S BIPLEXED WATCH DISPLAY WITH PM AND ALARM FLAGS

MODEL 5108E MEN'S BIPLEXED WATCH DISPLAY WITH PM AND ALARM FLAGS



NOTES:
1) COMPATIBLE WITH CMOS P/N FR8220 OR 8267.
2) DIMENSIONS IN PARENTHESES ARE IN MILLIMETETERS.
3) TOLERANCES UNLESS SPECIFIED: .XXX ± .005 (0,13).

Pin Schedule

	BP A	BP B		BP A	BP B
1)	BP A		11)	A2	COLON
2)	BLANK	ALARM	12)	F3	E3
3)	BLANK	BLANK	13)	G3	D3
4)	BLANK	BLANK	14)	B3	C3
5)	BLANK	BLANK	15)	F4	E4
6)	A,G,E,D1	BLANK	16)	G4	D4
7)	B1	C1	17)	B4	C4
8)	F2	E2	18)	A4	BLANK
9)	G2	D2	19)	A3	PM
10)	B2	C2	20)		BP B

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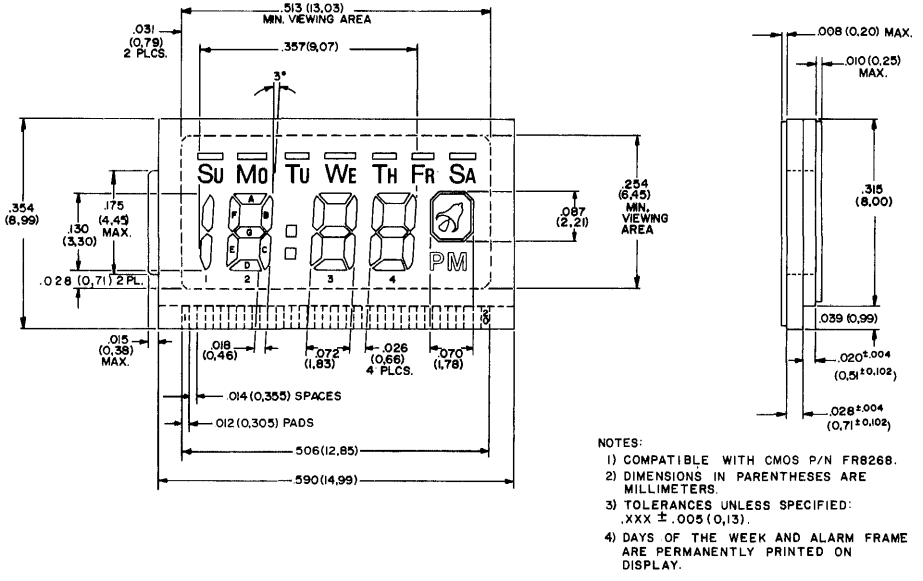
Model

5109C

LADIES' 3½ DIGIT BIPLEXED WATCH DISPLAY WITH ALARM, PM, AND DAY FLAGS.

MODEL 5109C LADIES' 3½ DIGIT BIPLEXED WATCH DISPLAY WITH ALARM, PM, AND DAY FLAGS



NOTES:

1) COMPATIBLE WITH CMOS P/N FR8268.
2) DIMENSIONS IN PARENTHESES ARE MILLIMETERS.
3) TOLERANCES UNLESS SPECIFIED: .XXX ± .005 (0,13).
4) DAYS OF THE WEEK AND ALARM FRAME ARE PERMANENTLY PRINTED ON DISPLAY.

Pin Schedule

	BP A	BP B		BP A	BP B
1)	BP A		11)	A2	COLON
2)	SU	ALARM	12)	F3	E3
3)	MO	SA	13)	G3	D3
4)	TU	FR	14)	B3	C3
5)	WE	TH	15)	F4	E4
6)	BLANK	BLANK	16)	G4	D4
7)	B1	C1	17)	B4	C4
8)	F2	E2	18)	A4	BLANK
9)	G2	D2	19)	A3	PM
10)	B2	C2	20)		BP B

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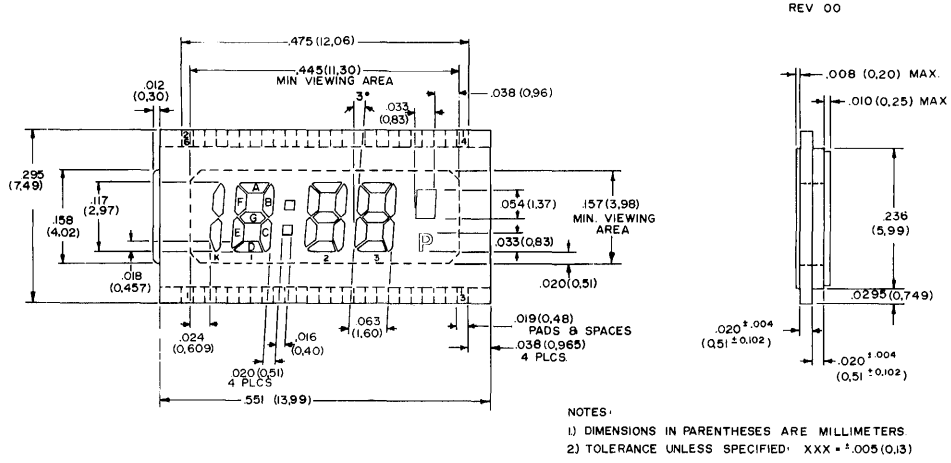
Model

5111AA

3½ DIGIT DIRECT DRIVE PEN DISPLAY WITH ALARM AND PM FLAGS.

MODEL 5111AA 3½ DIGIT DIRECT DRIVE PEN DISPLAY WITH ALARM AND PM FLAGS

Outside Dimensions .551 (13,99) x .295 (7,49)
Digit Height .117 (2,97)



Pin Schedule

1	Backplane	8	Seg D_2	15	Seg B_3	22	Seg G_2
2	Half Digit	9	Seg C_2	16	Seg A_3	23	Seg B_1
3	Seg E_1	10	Seg E_3	17	Seg F_3	24	Seg A_1
4	Seg D_1	11	Seg D_3	18	Seg G_3	25	Seg F_1
5	Seg C_1	12	Seg C_3	19	Seg B_2	26	Seg G_1
6	Colon	13	PM	20	Seg A_2		
7	Seg E_2	14	Alarm	21	Seg F_2		

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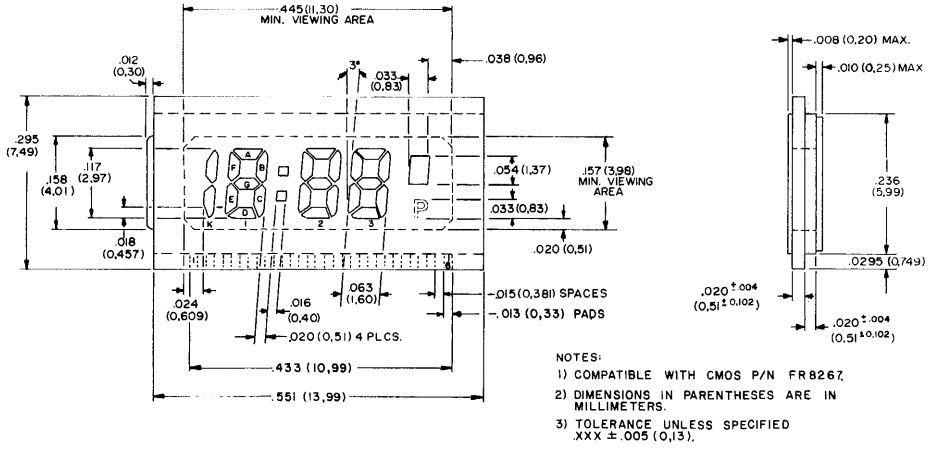
Model

5112AA

3½ DIGIT BIPLEXED PEN DISPLAY WITH ALARM AND PM FLAGS.

MODEL 5112AA 3½ DIGIT BIPLEXED PEN DISPLAY WITH ALARM AND PM FLAGS



Pin Schedule

	BP A	BP B		BP A	BP B
1)	BP A		9)	G3	D3
2)	BLANK	ALARM	10)	B3	C3
3)	B1	C1	11)	F4	E4
4)	F2	E2	12)	G4	D4
5)	G2	D2	13)	B4	C4
6)	B2	C2	14)	A4	BLANK
7)	A2	COLON	15)	A3	PM
8)	F3	E3	16)		BP B

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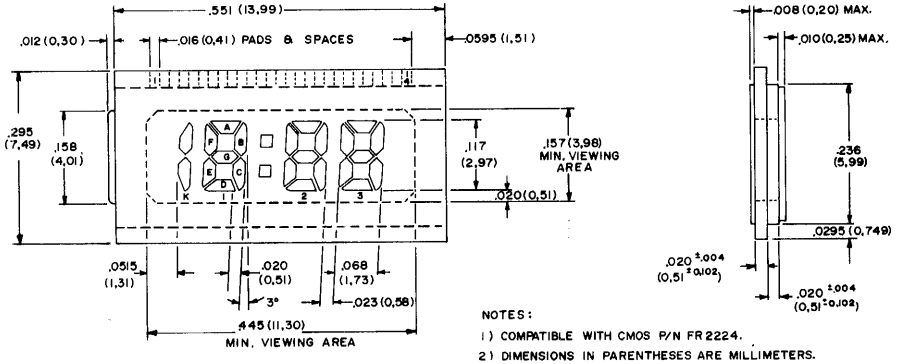
Model

5114AA

3½ DIGIT BIPLEXED PEN DISPLAY

MODEL 5114AA 3½ DIGIT BIPLEXED PEN DISPLAY



Pin Schedule

	A	B		A	B
1	Backplane		8	Seg G_2	Seg C_2
2	Half Digit	Seg E_1	9	Seg A_2	Seg B_2
3	Seg F_1	Seg D_1	10	–OFF–	Seg E_3
4	Seg G_1	Seg C_1	11	Seg F_3	Seg D_3
5	Seg A_1	Seg B_1	12	Seg G_3	Seg C_3
6	Colon	Seg E_2	13	Seg A_3	Seg B_3
7	Seg F_2	Seg D_2	14		Backplane

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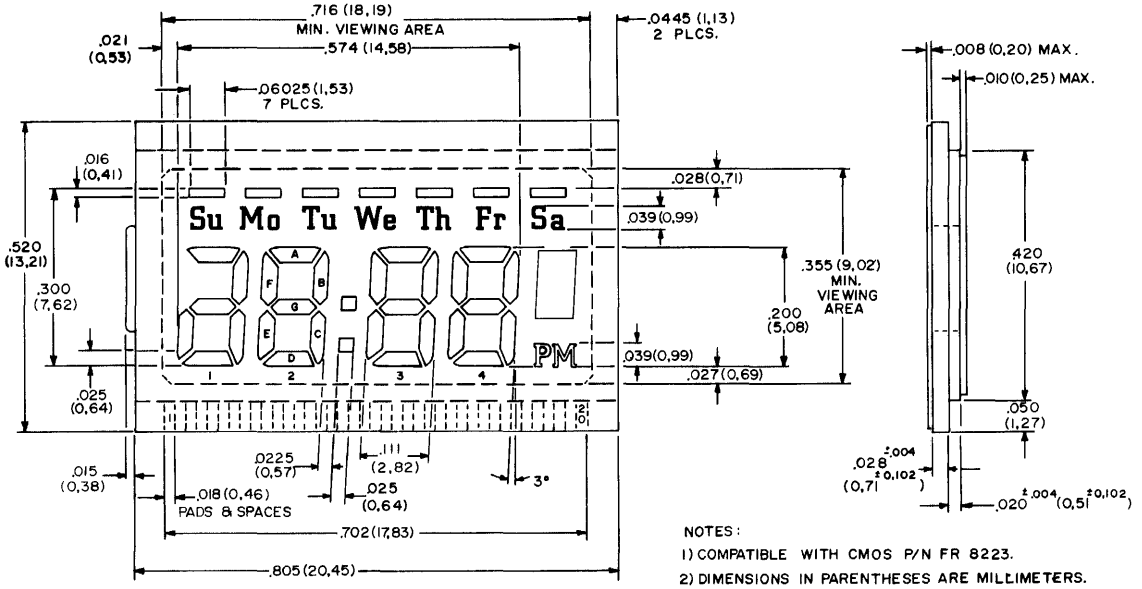
Model

5115E

MEN'S BIPLEXED WATCH DISPLAY WITH PM, ONE SECOND INTERNAL STOP-WATCH AND DAY FLAGS.

MODEL 5115E MEN'S BIPLEXED WATCH DISPLAY WITH PM, ONE SECOND INTERVAL STOPWATCH, AND DAY FLAGS.



NOTES:

1) COMPATIBLE WITH CMOS P/N FR 8223.
2) DIMENSIONS IN PARENTHESES ARE MILLIMETERS.
3) TOLERANCES UNLESS SPECIFIED: XXX = ±.005 (0,13).
4) SU PERMANENTLY PRINTED ON DISPLAY IN RED.
5) DAYS OF THE WEEK ARE PERMANENTLY PRINTED ON DISPLAY IN BLACK.

Pin Schedule

	BP A	BP B		BP A	BP B
1)	BP A		11)	A2	COLON
2)	SU	STOPWATCH	12)	F3	E3
3)	MO	SA	13)	G3	D3
4)	TU	FR	14)	B3	C3
5)	WE	TH	15)	F4	E4
6)	A,G,E,D1	BLANK	16)	G4	D4
7)	B1	C1	17)	B4	C4
8)	F2	E2	18)	A4	BLANK
9)	G2	D2	19)	A3	PM
10)	B2	C2	20)		BP B

SECTION 5

Packaging Information

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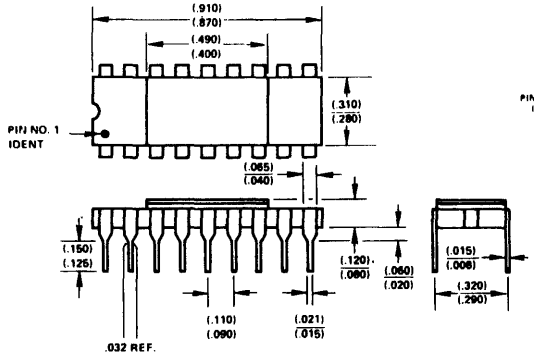
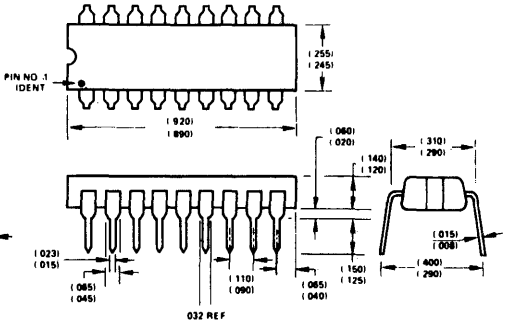
PACKAGING INFORMATION

18-PIN PACKAGE

CERAMIC

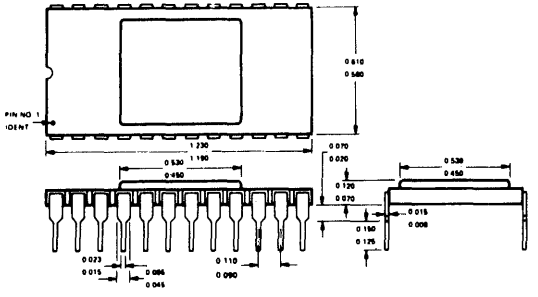


MOLDED

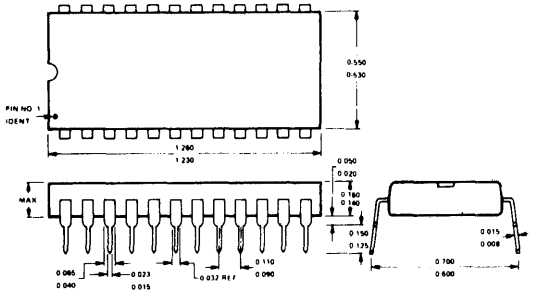


24-PIN PACKAGE

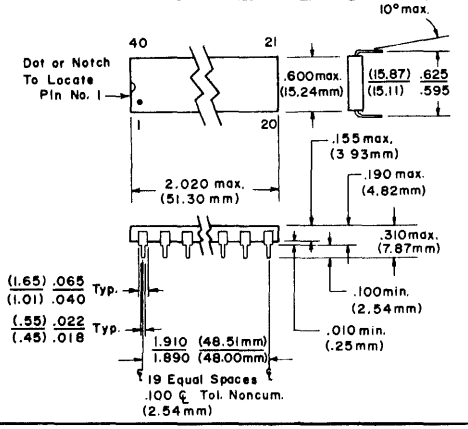
CERAMIC



MOLDED



40-PIN PACKAGE



SECTION 6

Application Notes

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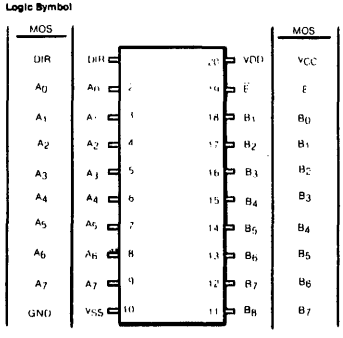
Application Brief # 1

OCTAL BUS TRANSCEIVER, OUR EQUIVALENT ASYNCHRONOUS TWO-WAY COMMUNICATOR, TTL-CMOS COMPATIBLE

65245 MOS	SYMBOL	SN74LS245 TI, MMI, FCI, MOT, SIG
The Same (OK)	Package	20 PIN DIP
The Same (OK)	I_{OL} Fan Out	I_{OL} 12ma Vol. .4V I_{OL} 24ma Vol. .5V
Typical Bad 47ma Better 44ma Better 56ma	Power I_{CC} Supply Current	Typical 25ma Total Outputs Hi 62ma Total Outputs Low 64ma Outputs at HiZ
Typical Better 20na Better 20na	Input Current I_{IH} I_{IL}	Typical 20µa −200µa
Our Best 20na, Typical Our Worst 47ns, Typical	Speed tpHL tpZL	8ns Typical (Their Best) 25ns Typical (Their Worst)

SUMMATION: Generally, we are better in supply current and input current, but slower in speed.



MPS 6525 VERSUS MC6821/ 8255

The MPS 6525 Tri-Port Interface Adapter combines three 8-bit I/O ports providing 24 individually programmable I/O lines. The third port is programmable for normal I/O operation or priority interrupt/handshaking control. The 6525 essentially has two basic modes: 1) 24 individually programmable I/O lines; or 2) 16 I/O lines, 2 handshake and 5 priority interrupt inputs.

This device is designed to offer enhancements over similar type circuits through flexibility and greater I/O capabilities. Table 1 compares the MPS 6525 to its competitors.

TABLE 1

	MPS 6525	MC6821	8255A
I/O	24	16	24*
Static	Yes	Yes	Yes
Control Lines	2	4	8**
Priority Interrupt	Yes (5)***	No	No
Frequency	1, 2, 3MHZ	1, 1.5, 2MHZ	****

*Port A and Port B Byte I/O programmable; Port C Nibble I/O programmable. All three ports of MPS 6525 are Bit I/O programmable through data direction registers.

**For control lines Port C is totally dedicated to this function.

***Port C will be dedicated if priority interrupts are used.

****Read Access 150 nsec (max.) for 8255A.
100 nsec (Max.) for 8255A-5 from $\overline{RD}$ high to low.

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Application Brief #3

HANDLING THE 'RDY' LINE IN 6500 CPUs

The 6500 series of CPUs use two phase clocks ϕ_1 and ϕ_2. Since clock stretching is not possible, the only way of interfacing with slow memories, performing dynamic refresh and Direct Memory Access is through the use of the RDY line.

The RDY line allows the user to insert one or more wait machine cycles between two instruction execution machine cycles.

To cause the CPU to insert wait cycles, the RDY line must make high to low transition during ϕ_1, high clock pulse. This transition may occur during any non write cycle. Wait machine cycles will be inserted until the RDY line is sensed high during a ϕ_2 high pulse.

If the RDY high to low transition occurs during a write cycle, the wait cycle will be inserted following the next non write cycle.

An important point of note is the fact that in the 6500 series of CPUs, an acknowledge signal is not available. To insure that the machine cycle following the RDY high to low transition is a WAIT, the user has to make sure that the negative transition occurs on a non write cycle. Figure 1 shows a simple circuit to guarantee this. The timing is illustrated in Figure 2.

The wait cycles generated can then be utilized to give the slow memories time to respond and dynamic memories can be refreshed.

Direct Memory Access is also possible during this time. Since Address and Data buses are not floated, alternate address and data paths are provided through the use of tristate buffers.

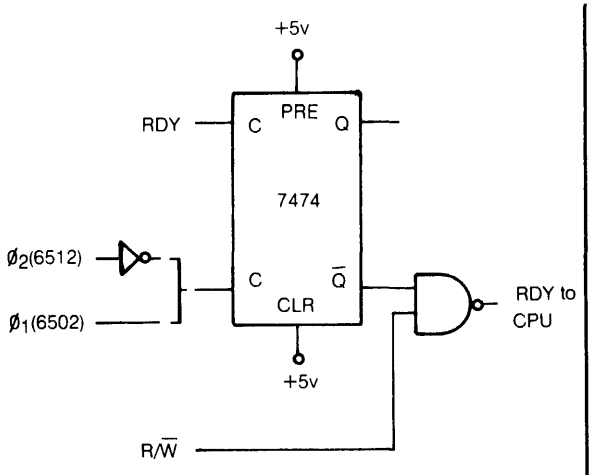

FIGURE 1

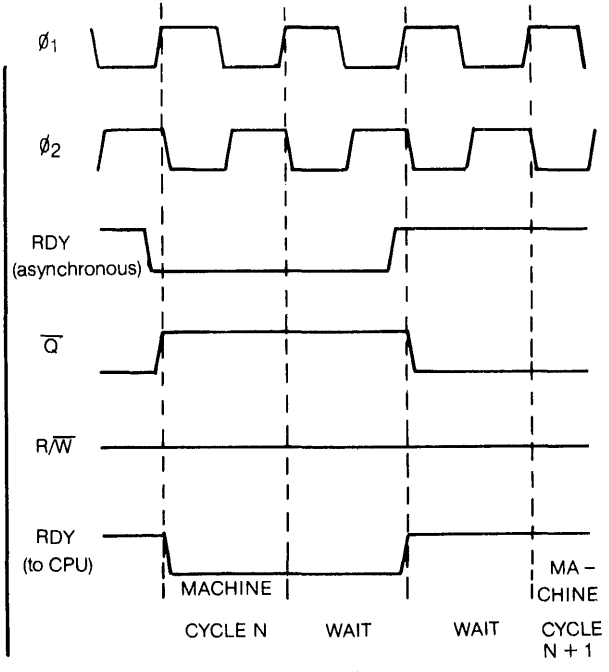

FIGURE 2

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Application Brief #4

MPS 6520 VERSUS MC6820/MC6821

The MPS 6520 Peripheral Adapter is a 16 line (2 port) bi-directional I/O device with four peripheral control/interrupt lines. The MPS 6520 is pin and funcitonally compatible with the MC6820 Peripheral Interface Adapter from Motorola/Hitachi. The MPS 6520 is pin compatible with the MC6821 PIA, but the functional differences are outlined in the table below.

CHARACTERISTIC	MPS 6520 MAX	MC6821 MAX
I_{IL}, Input Low Current PAØ-PA7, CA2 (V_{IL} = 0.4Vdc)	−1.6mAdc	−2.4mAdc
I_{LOAD} (V_{CC} = min., V_{OL} = 0.4Vdc max.)	1.6mAdc	3.2mAdc

The other functional difference between the MPS 6520 and the MC6821 is that the 6520 has a max. enable cycle time of 25μ sec. while the MC6821 is fully static. If the above differences are not critical to the user, than the MPS 6520 may be substituted for the MC6821 as well as the MC6820.

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Application Brief #5

DUAL PROCESSOR CONFIGURATION WITH THE MPS 6508

The MPS 6508 has been designed with a non-overlapping two phase clock. The potential behind this may not be apparent until one examines a control line that is available on the 6508 — the AEC. What this means to the user is the power to design a dual processor system capable of running at full speed with virtually no overhead.

The AEC line can be used to tri-state the address bus. Since data is valid only during phase two high, with minimal logic, it will be possible for two 6508s to access common memory on opposite phase of the same clock.

Figure 1 shows a simple block diagram connecting two processors together. The timings are illustrated in Figure 2.

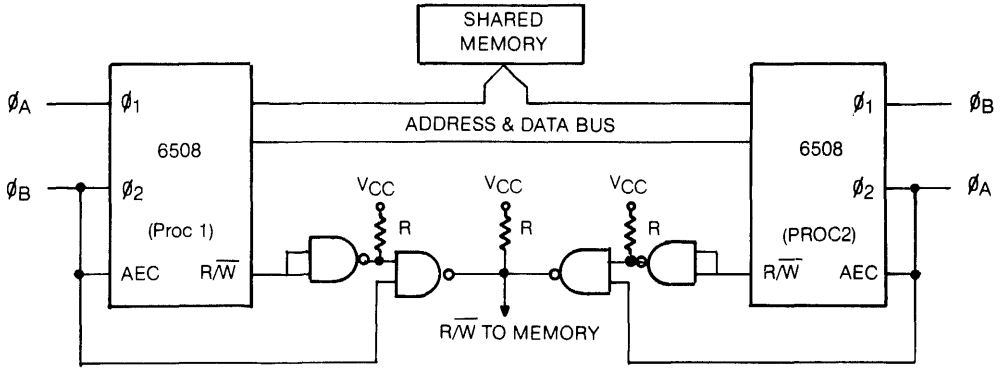
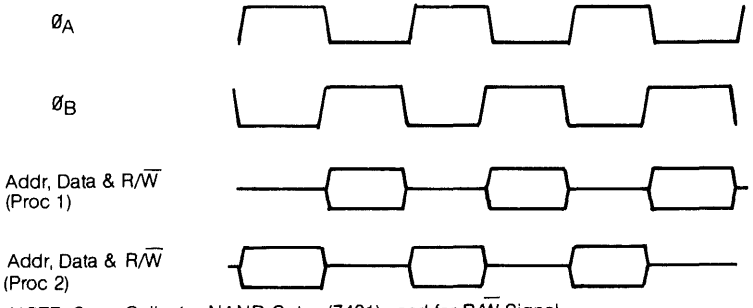


FIGURE 1



NOTE: Open Collector NAND Gates (7401) used for R/W Signal.

FIGURE 2

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Application Brief # 6

6551 VERSUS 6850

The MPS 6551 is an enhanced version of the MC6850. On chip baud rate generation represents the principal enhancement. Baud rate can be generated internally by either connecting a crystal across the XTAL1 and XTAL2 pins or by inputting a clock signal through XTAL1. Various baud rates can then be generated under program control. In both cases, the device outputs a clock signal through RxC pin at 16 times the programmed baud rate. This can be used to synchronize a multiple 6551 System.

The 6551 also has all five Standard Modem Control Signals, unlike the 6850 which has only three. Thus, in the 6551 the $\overline{RTS}$ (Request-to-Send) does not have to double up for the $\overline{DSR}$ (Data Set Ready) like the 6850. The $\overline{DSR}$ is a signal used by many modems.

The 6551 has four addressable locations against the two provided by the 6850. Thus, the 6551 through these additional locations offers many more software programmable options to the user.

To add to all this, the 6551 offers a hardware master reset in addition to the software reset offered by the 6850.

From all of the above, it can be seen that the 6551 is a superior device to the 6850.

6551 VERSUS COMPETITION

	6551	6850	8251[1]
Baud Rate Generator [2] (On-Board)	Yes	No	No
5 - 8 Bit[3] Characters	Yes	No	No
XTAL Oscillator (On-Board)	Yes	No	No
Full Modem Controls	Yes	No	Yes
Baud Rates (Programmable)	50-19.2 K Baud	N/A[4]	To 19.2K Baud

1 Includes synchronous operation.
2 1.8432 MHZ external crystal attaches directly to 6551 pins for 15 programmable baud rates.
3 6551 includes 9-Bit character transmission.
4 Spec. Max. BPS (Bits Per Second) through external clock input.

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Application Brief # 7

MEMORY EXPANSION WITH THE 6508

How often is it that you have wished for an additional address line or two in your system? The MPS 6508 offers the user the flexibility of accessing up to 16 MBYTES of address space in segments of 64K with almost no overhead.

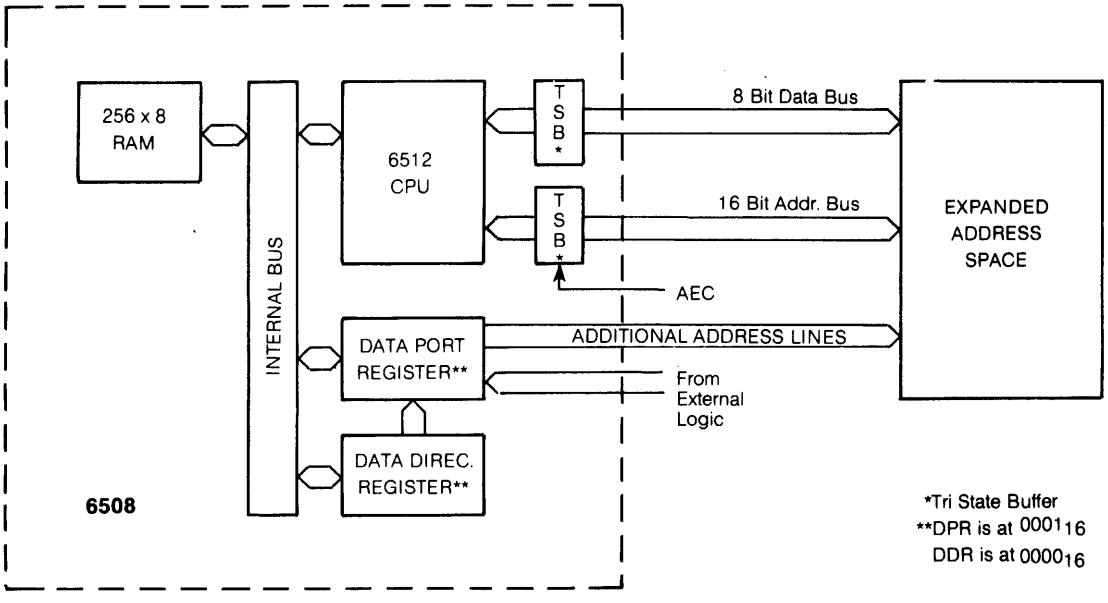
The 6508 has on board, an eight bit data port. This port is accessible through two registers, a data direction register and a data port register. By setting up a few of the I/O lines as output, and loading the port with the segment value, it will be possible to address a unique 64K of address space. Reloading the data port with a different value now enables the addressing of a different 64K address space.

The additional software needed is fairly trivial and is given below:

```
LDA #Config.   ;  Config. is used to set up
                  individual lines as input
                  or output.
STA DDR        ;  Store in Data Direction
                  Register.
LDA # SEG      ;  SEG is a number from 0 to
                  255 that decides 64K segment
                  being accessed.
STA DPR        ;  Store in Data Port Register.
```

After this, any time a new 64K segment has to be accessed, only the last 2 lines of code have to be executed.

This expanded addressing capability along with ability for external hardware to decide the address segment to be accessed gives the user a powerful microprocessor.



MPS 6508 — EXPANDED MEMORY CONFIGURATION

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Application Brief #8

MPS 6545-1 VERSUS COMPETITION

The MPS 6545-1 CRT Controller is an enhanced version of the MC6845. The major improvements are the addition of a status register and the ability to program the type of screen memory addressing desired (linear or row/column). The status register is used to monitor the status of the MPS 6545-1. There is a vertical blanking status bit which can be tested to determine when the vertical retrace is occurring. At this time, the microprocessor can access screen memory since the MPS 6545 does not require access to screen memory during vertical retrace. There is also a light pen full bit. This bit is used to determine when a new value has been stored in the light pen position register. No provision for this is available on the MC6845.

As can be seen in the chart, the MPS 6545-1 stacks up favorably against the MC6845 as well as the other CRT controllers on the market.

	MPS 6545-1 COMMODORE/ MOS TECHNOLOGY	**6845 MOTOROLA**	**8275 INTEL**	**DP8350 NSC**	**5027 SMC**
Display Format Characters/Row Row/Frame Scan Lines/Row	 1-256 1-128 1-32	 1-256 1-128 1-32	 1-80 1-64 1-16	 5-110 1-64 1-16	 20-132 1-64 1-16
Screen Memory Addressing	Linear or Row/Column	Linear	Linear	Linear	Row/Column
Light Pen Logic	Yes	Yes	Yes	No	No
Accessible Registers	Screen Format Timing Cursor Light Pen Top-of-Page Status	Screen Format Timing Cursor Light Pen Top-of-Page	Cursor Status Light Pen	Cursor Top-of-Page New Row	Cursor Scroll Top-of-Page
Interlaced Mode	No*	Yes	No	No	Yes

*MOS MPS 6545 has interlaced mode

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Application Brief #9

MPS 6508
AN 'ACTIVE' CPU DURING BLOCK DMA

A big problem faced with most users is that during Direct Memory access (DMA), the processor is idle. Thus, when processing speed is critical, in most systems the use of DMA block transfer mode is not recommended. However, with an MPS 6508 based system, it is possible for the processor to be executing even during DMA.

The 6508 has an AEC input pin which has to be sensed low in order for the processor to float its address bus. During this time, DMA is possible. The 6508 has on board 256 bytes of RAM which reside concurrently in page zero and page one. The processor also has an 8 bit I/O port which is accessible through a Data Direction Register at address 0000_{16} and a Data Port Restister at address 0001_{16}.

Even though the external bus has been tristated, the processor still has an active internal bus through which it can function off the internal RAM and communicate with the external world through the I/O port.

Thus, in any system where handling block transfers is essential and high processor thorughput is desirable, the MPS 6508 will prove to be a wise choice.

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Application Brief # **10**

FR208X
THE 'MELODY' CHIP

The FR208X is a musical chip that comes in several versions. In essence, the 208X is capable of playing musical notes for up to about a minute. The chip can be used either in a stand alone mode or with many common alarm chips. In order to get longer tunes (i.e., greater than a minute), it is possible to cascade the chip with no interface logic being required.

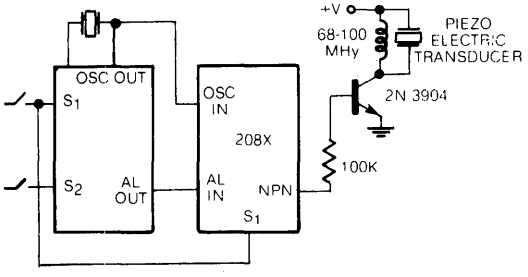
The main difference between the various versions of this chip are given below:

VERSION	FEATURE
FR2081	Single Tune Chip
FR2082	Dual Tune Chip — User selects desired tune
FR2083	Custom Dual Tune Chip
FR2084	Dual Tune Chip — Alternates between tune A and tune B each time the alarm triggers the 2084

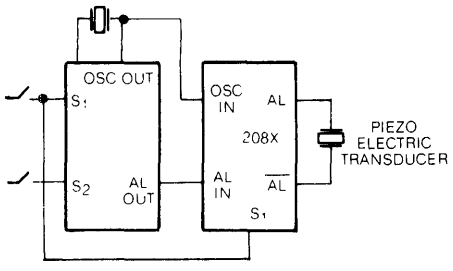
The FR208X is designed in metal gate C-MOS, and draws current in the low microampere range, while standby current is less that one microampere. This chip should, therefore, find a comfortable place in the low cost, low power consumer application market.

A list of all the standard tunes available can be obtained by contacting the factory.

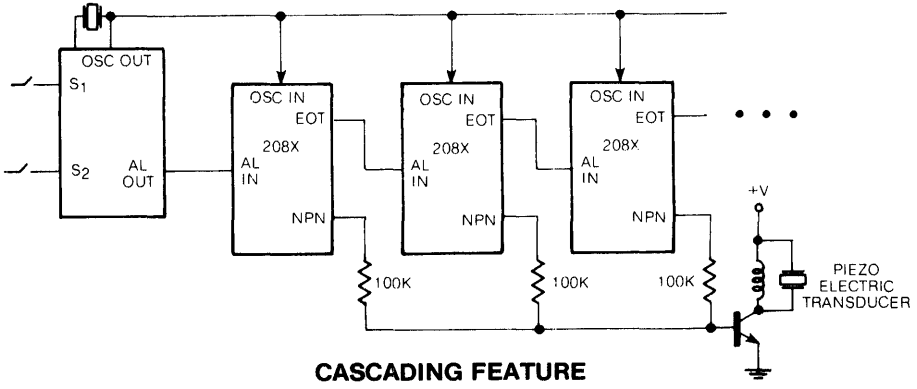
The figures below illustrate some simple ways of using the melody chip.



NPN DRIVE



DIRECT DRIVE



CASCADING FEATURE

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Application Brief # 11

MPS 6508
HANDLING VECTORED INTERRUPTS

In many microprocessor systems, handling multiple interrupts is an adventure into the realm of complex peripheral chips -- Priority Interrupt Controllers, Parallel I/O Devices and so on. The MPS 6508 offers a simple solution for the user who is conscious about his on board real estate.

The 6508 has available on the chip, an eight bit I/O port, accessible through a Data Direction Register and a Data Port Register. This port can be configured very flexibly to handle a variety of interrupt processing.

In this applications brief, we will consider Vectored Interrupts and Priority Control. Most systems that use a vectored interrupt structure work off a jump table for processing the interrupt. In such a case, the peripheral requesting the interrupt needs to supply only the low byte of the interrupt vector, the interrupt vector that resides at FFFE and FFFF being the base address of the jump table. The number of I/O lines being dedicated as inputs will be a function of the number of peripherals capable of requesting interrupt processing.

Interrupt priority handling is a useful, if not essential part of any interrupt based system. Instead of using a complex and expensive peripheral for arbitration, the I/O port of the 6508 can be set up to do the job. After sensing an interrupt, the 6508 could read the port to see which peripherals were requesting an interrupt. Based on priority arbitration software, a few I/O lines programmed as outputs could then be used to indicate to the peripherals which one is being selected.

From the above, we can immediately see the potential of the MPS 6508 and its wide application in many systems where low cost and board space are a premium.

MPS 6525
A TWO IN ONE DEAL

The MPS 6525 in its simplest form can be looked upon as a triport I/O chip. It provides the user with 24 I/O lines that can be programmed individually, organized as three 8 bit ports.

The device is accessed through eight contiguous locations in the systems address space ... 3 Data Direction Registers, 3 Data Port Registers, a Control Register, and an Active Interrupt Register. This in itself provides the user with a chip that has more I/O capability than almost anything else available.

However, the MPS 6525 does not stop there. Through a bit in the control register, the device can be set up to behave as an Interrupt Controller.

In this mode, two ports are still dedicated to I/O while the third port is set up to handle upto five interrupts. The interrupt controller can be set up to be either prioritized or non prioritized. In the prioritized mode, through the use of a built in interrupt stack, the 6525 makes writing software a piece of cake. Also, when used as an interrupt controller, this device provides the user with two dedicated lines for handshaking ... one on data in and one on data out.

What in essence this does is enable the user to replace two chips, the MC6821 (Peripheral Interface Adaptor) and the MC6828 (Priority Interrupt Controller) in most applications, thus giving him a reduction in both cost and space.

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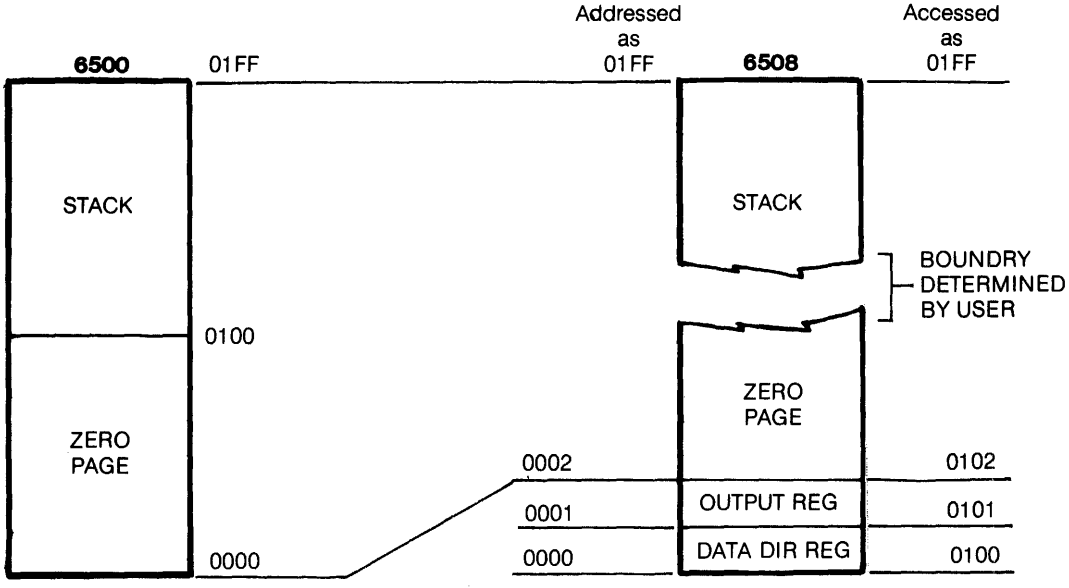
Application Brief # 13

THE 6508 RAM — TWO PLACES AT ONCE?

How can a processor have both page zero and page one with only 256 bytes of RAM? One way is to combine both pages into one, and this is what the 6508 does.

On the 6508, the 256 bytes are actually located at 0100_{16} to $01FF_{16}$, or the normal 6500 family stack area. Internal logic decodes the zero page instructions so that they appear to begin at 0102_{16} (0100_{16} and 0101_{16} are used by the I/O port registers). The stack area starts at $01FF_{16}$ and grows down. Care must be taken so that the stack does not become large enough to overwrite the zero page area. This, however, is not a problem with most applications.



6508 Internal RAM Memory Map

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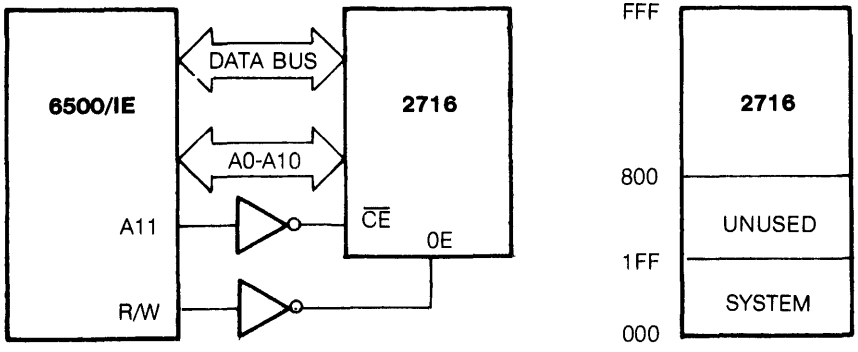
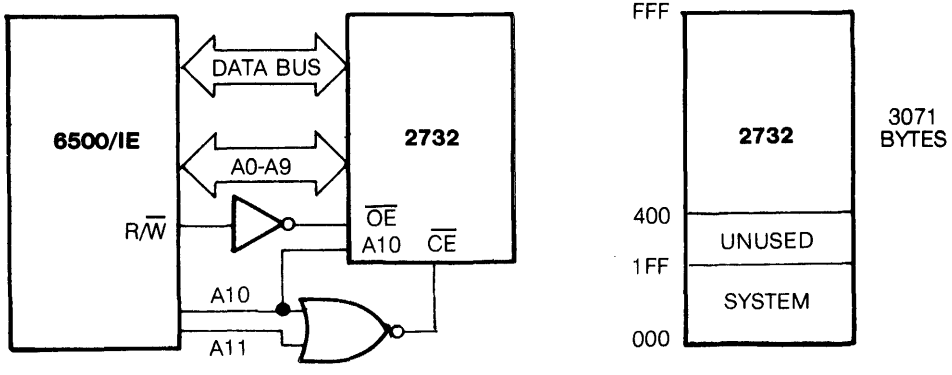
Application Brief # 14

MPS 6500/1E — EPROM APPLICATIONS

The MPS 6500/1E is the 64 pin emulator version of the MPS 6500/1 single-chip microcomputer. It is electrically identical except there is no ROM on-chip. The extra pins are used to connect to the internal processor bus so that external eproms may be used for system development. This brief presents two eprom connection schemes. Example 1 is a 2K 2716 version, while example 2 is a 3K 2732 application. Both schemes are designed with a minimum part count in mind.



Example 1. 2716 EPROM (2k Bytes)



Example 2. 2732 EPROM (3k Bytes)

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Application Brief # 15

MPS 6500/1 — RAM MEMORY EXPANSION

The MPS 6500/1 is a single-chip microcomputer containing 2K bytes of ROM and 64 bytes of RAM. The RAM is used for both data storage and stack memory. In most applications, this is an adequate amount of memory; however, in some cases, it may be desired to expand the RAM memory beyond 64 bytes. This brief describes a simple way to achieve this.

It is possible to attach conventional static RAMS directly to the MPS 6500/1 I/O lines and perform read and write operations with simple software steps. This approach will not work for stack expansion and cannot be adapted to program memory (ROM), since these elements require a direct connection to the processor busses.

The example presented here will provide 1024 bytes of RAM storage using two 2114's. No other hardware is needed.

Some observations are noteworthy:

- Port A of the MPS 6500/1 is the first 8 bits of the address for the RAM. All pins are outputs.
- Port B of the MPS 6500/1 contains bits 8 and 10 of the address; bits PB0 and PB1 respectively. Also, bit PB7 is used to supply the R/W signal to the memory. Pins PB0, PB1 and PB7 are outputs; all other pins are free.
- Port C is used for the bi-directional data bus.
- The $\overline{CE}$ for 2114 is tied to system ground, so the memory is always enabled.

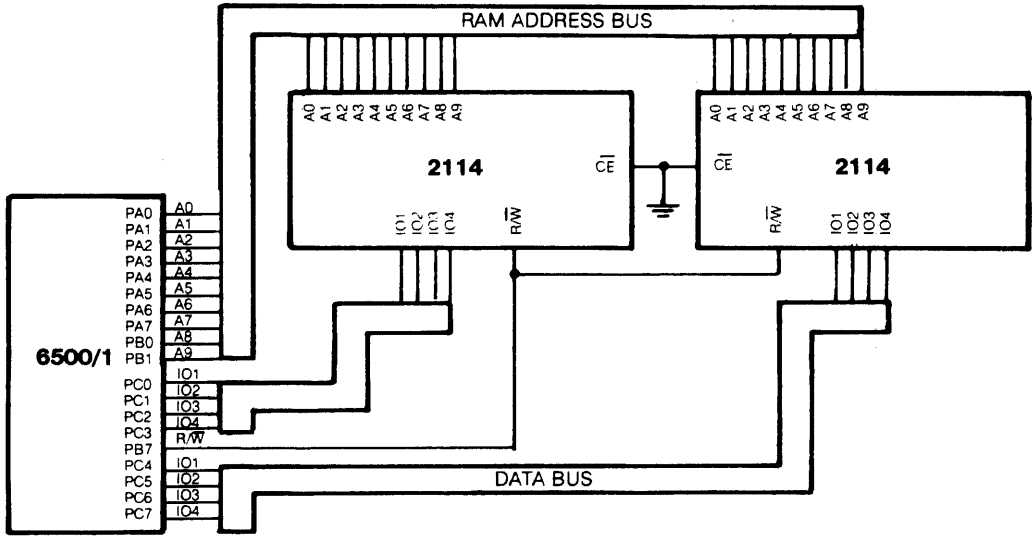

Figure 1 — Schematic for 1K Byte Expansion

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APPLICATIONS BRIEF # 16

SIMPLE CLOCK GENERATION FOR THE MPS 6500 MICROPROCESSOR FAMILY

Clock generation for the MPS 6500 family microprocessor can easily be accomplished with only a handful of components by using one of the following circuits.

Figure 1 illustrates a single phase clock. This clock can be used to drive the 6502, 6503, 6504, 6505, 6506 and 6507. Figure 2 is a two-phase clock, which is used for the 6508, 6510, 6512, 6513, 6514 and 6515.

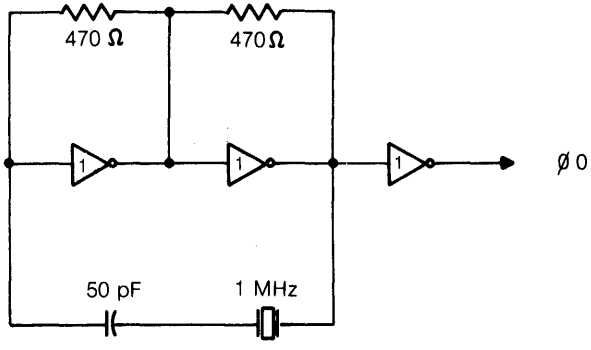
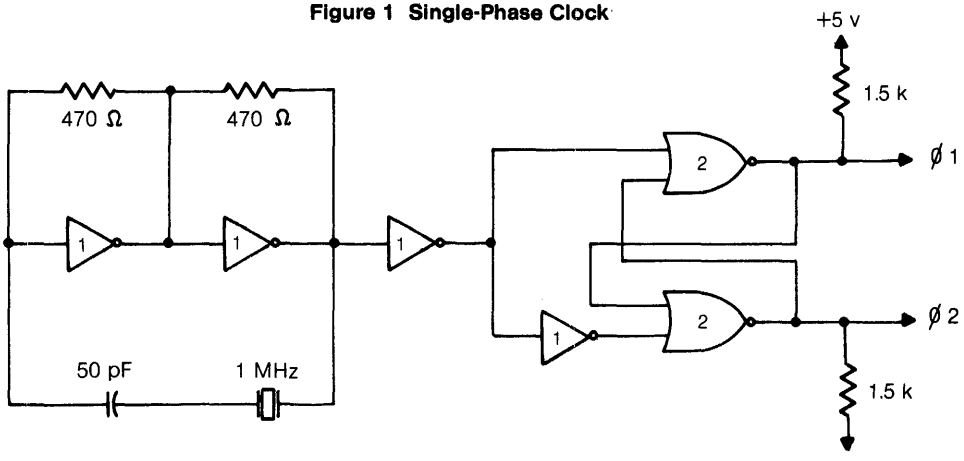


Figure 1 Single-Phase Clock



Device
① 7404
② 74LS33

Figure 2 Two-Phase Clock

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APPLICATIONS BRIEF

CMOS/LCD WATCH-CLOCK CIRCUITS

APPLICATION NOTE

COMMODORE LOW POWER/LOW COST TIMEKEEPING COMPONENTS

As one of the world's leading suppliers of state-of-the-art timekeeping circuits and LCD displays, Commodore introduces a new family of low power, low cost multiplexed components for watch, clock, and general timekeeping applications.

COMMODORE/FRONTIER CMOS/LSI multiplexed timekeeping circuits operate from 1.3-1.7 volts with currents typically in the 1.0μA-1.5μA range. All parts have been designed for low cost and ease of application as well. The following is a brief description of available multiplexed circuits and matching LCD displays from **COMMODORE OPTOELECTRONICS:**

PART NUMBER		
CMOS	**LCD**	**DESCRIPTION**
2224	5060,5061,5075	3½ Digits 5 Functions
8220	5107,5108	4 Digits, 5 Functions
8221	5107,5108	4 Digits, 5 Functions, Stopwatch
8222	5102,5103	4 Digits, 6 Functions, (Day Flags)
8223	5102,5103	4 Digits, 6 Functions, Stopwatch
8267	5107,5108,5112	4 Digits, 5 Functions, Alarm
8268	5102,5103,5109	4 Digits, 6 Functions (Day Flags), Alarm
8668	5104	8 Digits, 5 Functions (Day Flags)
8868	5104	8 Digits, 6 Functions, Alarm
887X	In Development	8 Digits, 5 Functions, Alarm, Day Flag, Programmable Animation

Note: All products have 12/24 HR option excepting 2224. All Alarms have Snooze feature.

PRODUCT DESCRIPTIONS:

1. 2224 - 3½ digits and 5 functions (Hours: Minutes, Month, Date,: Seconds).

   This circuit is the most basic unit available. One button controls the viewing of the three sets of information; the use of another button allows for setting. Typical current drain is less than 1.0μA operating with a watch display. Applications utilizing larger displays will tend to draw somewhat greater current. This part has a total of 27 pins.

   Some available Commodore displays for this part are:

   5060 B Ladies' Watch Display
   5061 E Men's Watch Display
   5075 A Smaller display for miniature applications such as LCD pens.

2. 8220-4 digits and 5 functions with 12/24 hour option. The part functions similar to the 2224; 24 hour (military) time format option is present. This part has a total of 30 active pins.

   Some available Commodore displays for this part are:
   5107 B Ladies' Watch Display
   5108 E Men's Watch Display

3. 8221 - 4 digits and 5 functions with 1 second accuracy stopwatch and 12/24 hour option. The stopwatch is accessible by use of a third switch and measures elapsed time. The part otherwise operates like a two switch 8220. This part has a total of 30 active pins. The available displays are the same as for 8820.

4. 8222 - 4 digits and 6 functions (Hours: Minutes and Day of Week Flags, Month Date and Day of Week Flags, and: Seconds with Day Flags). The part operates like an 8220 with the addition of the Day indicators for the sixth function. The part has a total of 33 pins.

   Some available Commodore displays for this part are:
   5102 E Men's Watch Display
   5103 C Ladies' Watch Display

5. 8223 - 4 digits and 6 functions with 1 second accuracy Stopwatch and 12/24 hour option. This part operates like the 8221 with the addition of the Day indicators for the sixth function. The part has a total of 33 pins. The available displays are the same as for 8222.

6. 8268/8368 - 4 digits, 6 functions with Alarm, Day Flags, and 12/24 hour option. This part operates as a simple two button Alarm watch or clock. The Alarm functions (viewing, setting and arming/disarming) are extremely simple and modeled after other popular Commodore Alarm chips. This part has a total of 34 active pins. Note: The 8368 will be identical to the 8268 except that the 3 second delay entering the set mode will be eliminated.

   Some available commodore displays for this part are:

   5102 E Men's Watch Display
   5103 C Ladies' Watch Display
   5109 C Ladies' Watch Display

7. 8267/8367 - 4 digits, 5 function with Alarm and 12/24 hour option. The part operates like the 8268/8368 with no Day Flags; it has 31 active pins. The available displays are:

   5107 B Ladies' Watch Display
   5108 E Men's Watch Display
   5112 AA Miniature Pen Display
   4003 K Large Digit Clock Display
   4006 L Large Digit Clock Display
   4007 N Large Digit Clock Display

8. 8668 - 8 digits 5 functions with 12/24 hour option. This watch displays Hours: Minutes, Seconds, Date and Day of Week Flags simultaneously. This type of timepiece has been dubbed "No Hands" because all essential functions are displayed simultaneously. The part has a total of 44 pins.

   Some available commodore displays for this part are:
   5104 I Men's Watch Display

9. 8868 - 8 digits 6 functions with alarm, Snooze and 12/24 hour option. This part displays all information of the 8668 "No Hands" with the additional feature of an Alarm. The Alarm is operated in a manner identical to 8267 and 8268. The part has a total of 46 pins. The available display is the same as for the 8668.

10. 887X - 8 digits, 5 functions with Alarm and 7 programmable flags for Animation. The chip will allow the design of very novel and unique products combining LCD animated motion under switch or alarm control with time. Toys, watches, clocks, promotional items etc. are among the many target markets. This part has a total of 46 pins.

The implementation of any of the above circuits is illustrated in Figure 1. Note that fundamental timekeeping is accomplished with the following basic parts:

A. 1 chip on PC Board
B. 1 LCD Display
C. 1 32KHZ Quartz Crystal
D. 3 Capacitors
E. 1 Trimmer Cap
F. 2 Switches
G. 1-2 "Zebra" interconnecting Strips
H. 1 1.5-1.6V Battery

The addition of an Alarm can be accomplished with as little as a piezo electric transducer. The addition of an NPN transistor and coil allows the Alarm sound to be greatly enhanced. Musical alarms are also possible with the addition of the 208X.

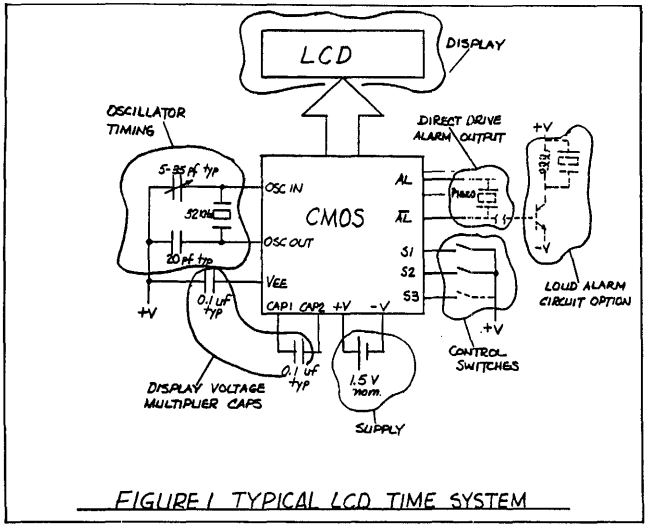

FIGURE 1 TYPICAL LCD TIME SYSTEM

With all of the above products, the dramatic advances in technology and high volumes inherent in the timekeeping industry allow the potential introduction of Time with multi-features into numerous new, low cost applications. A few such applications are:

1. LCD Clocks for automotive accessories having Alarm or Stopwatch for trip timing.
2. LCD Alarm Clocks as an added feature cooking aid for outdoor BBQ/Gas grills.
3. Low cost time functions for games.
4. Low cost time functions for telephones; stopwatch for timing long distance calls.
5. Low cost time functions for appliances (e.g. Radios, TV, Stereo equipment etc.).
6. Timekeeping promotional items (e.g. paper weights, penholders etc.). This field may be especially good for watches with "customized" musical alarms which play music such as company or product theme songs.

Although the above circuits and displays are most commonly available and utilized in die form on hybrid circuit substrates, Commodore will gladly quote the above components in any form suitable to the customer (i.e. raw die or packaged parts) Inquiries regarding special applications for chips and/or LCD displays are always welcomed.

In any form, Commodore's many years of experience and long term dedication to the field of timekeeping are assurance of continuing competitive, cost-effective products.

SECTION 7

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153 Main St.
Salem, NH 03079
(603) 893-5521

Upstate New York

Techmark/Upstate Assoc.
P.O. Box 173
Mendon, NY 14506
(716) 624-3840

Techmark/Upstate Assoc.
2 Andrews Way
Canandaigua, NY 14425
(716) 396-2498

Techmark/Upstate Assoc.
P.O. Box 120
Endicott, NY 13760
(607) 748-7473

Metro New York
North New Jersey

J-Square Marketing, Inc.
P.O. Box 103
Jericho, NY 11753
(516) 935-3200

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Maryland
Washington, D.C.
Virginia
West Virginia

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3701 Old Court Rd. #14
Baltimore, MD 21208
(301) 484-3647

Massachusetts
Rhode Island
Vermont
Maine
New Hampshire

Minuteman Marketing, Inc.
279 Cambridge Street
1 Colonial Park, Suite 102
Burlington, MA 01803
(617) 272-0035

Pennsylvania
South New Jersey

The Rep Force
18 East Commerce Street, Suite A
Bridgeton, NJ 08302
(609) 455-0891

Florida

HAI
10212 W. Sample Road
Coral Springs, FL 33065
(305) 752-7520/7550

HAI
10312 136 Street North
Largo, FL 33540
(813) 595-8170

North Carolina
South Carolina
East Tennessee

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Raleigh, NC 27609
(919) 782-8433

Missouri
Kansas
Nebraska
Southern Illinois
Iowa

R&D Sales, Inc.
13013 St. Andrews Drive
Kansas City, MO 64145
(816) 941-9280

REPRESENTATIVES

Michigan (except Berrien County)
Ohio

Jim Finnegan and Co.
P.O. Box 8825
Cleveland, OH 44136
(216) 238-5905

Jim Finnegan and Co.
1236 Clubview Blvd.
Worthington, OH 43085
(614) 436-7227

Jim Finnegan and Co.
5527 Fawn Court
West Chester, OH 45069
(513) 874-5937

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Arkansas
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Arlington, TX 76011
(817) 640-9101

W. Pat Fralia Company
300 E. Huntland Blvd., Suite 210
Huntland Professional Building
Austin, TX 78752
(512) 451-3325

W. Pat Fralia Company
4411 Bluebonnett
Stafford, TX 77477
(713) 491-9336

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Des Plaines, IL 60018
(312) 298-9330

Janus, Inc.
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Milwaukee, WI 53226
(414) 476-9104

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Criterion
3350 Scott Boulevard
Building #44
Santa Clara, CA 95051
(408) 988-6300

Colorado

High Tech Associates
2950 S. Jamaica Court, Suite 100
Aurora, CO 80014
(303) 695-1900

New Mexico

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8016-A Zuni Road SE
Albuquerque, NM 87108
(505) 266-7951

Oregon
Washington
W. Idaho

Quest
15 S. Grady Way, Suite 203
Kenton, WA 98055
(206) 223-1541

Quest
6220 S.W. 130th, #10
Beaverton, OR 97005
(503) 644-8077

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7204 Main Street
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(604) 324-0505

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14101 Yorba Street, Suite 104
Tustin, CA 92680
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